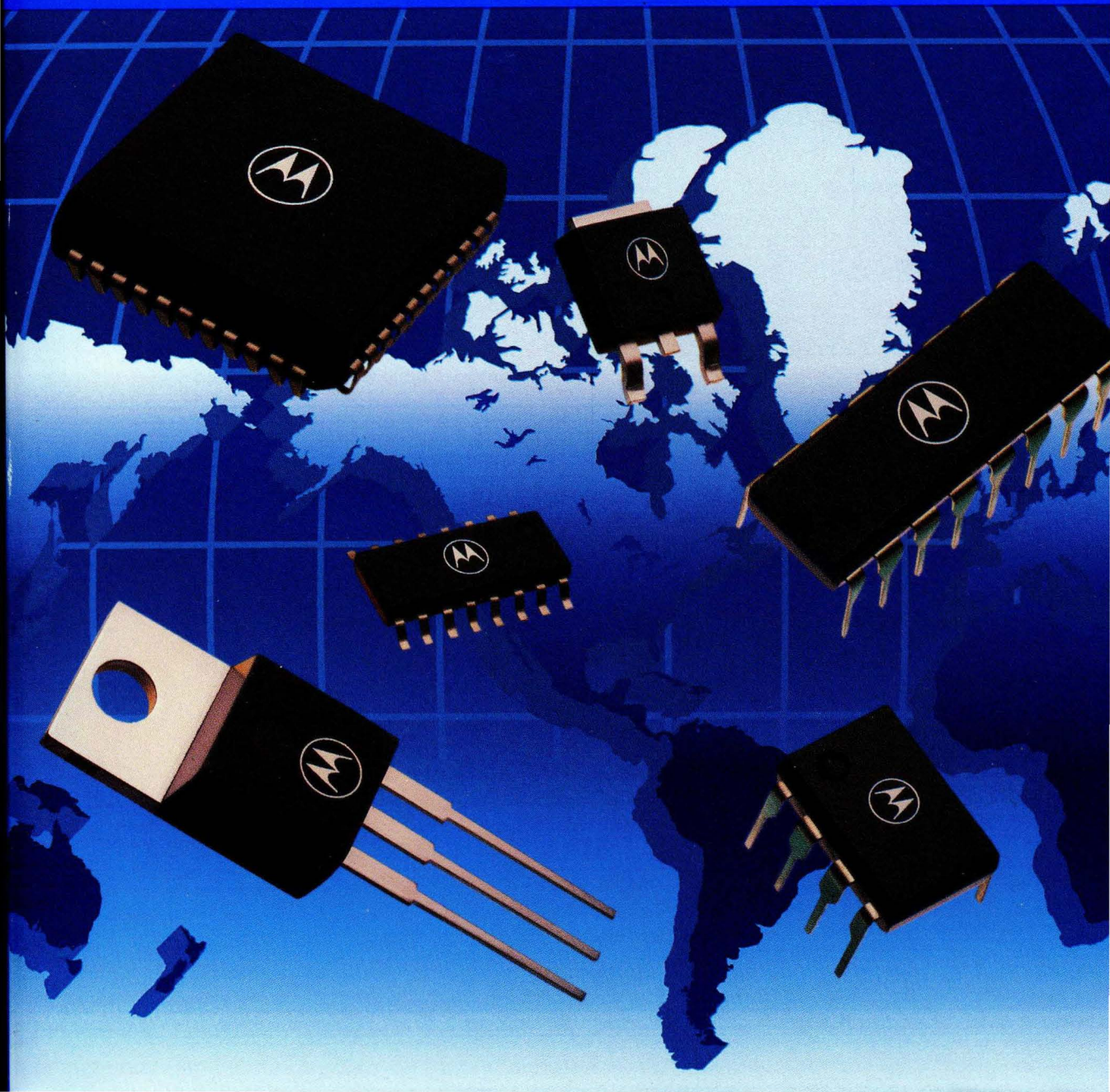
MOTOROLA

DL128/D
REV 4

Linear/Interface ICs

Device Data

Vol. II



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- TDA3330
- TDA4601
- TL061
- ULN2074B

New Product Literature (Referenced)

- AN1046
- AN1077
- AN1122
- AN1203
- AN1510

MOTOROLA

LINEAR/INTERFACE ICs DEVICE DATA

This publication presents technical information for the broad line of Linear and Interface Integrated Circuit products. Complete device specifications are provided in the form of **Data Sheets** which are categorized by product type into ten chapters for easy reference. **Selector Guides** by product family are provided in the beginning of each Chapter to enable quick comparisons of performance characteristics. A **Cross Reference** chapter lists Motorola nearest replacement and functional equivalent part numbers for other industry products.

A chapter is provided to illustrate **Package Outline** and includes information on Surface Mount Devices (SMD).

Additionally, chapters are provided with information on **Quality** program concepts, high-reliability processing, and abstracts of available **Technical Literature**.

The information in this book has been carefully checked and is believed to be accurate; however, no responsibility is assumed for inaccuracies.

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Series H
First Printing

Printed in U.S.A.

New Product Literature

Chapter 2 has an addendum providing applications information on operational amplifiers.

The applications information which formerly appeared in the *Motorola Linear/Switchmode Voltage Regulator Handbook* (HB206) is now included as an addendum to Chapter 3.

An addendum covering RF applications information has been added to Chapter 8.

The Surface Mount Technology in Chapter 12 has been expanded to include Multiple Package Quantity (MPQ) information for surface mount and TO-92 packages shipped in Tape and Reel or Ammo Pack Styles. Mechanical Polarization drawings for the TO-92 (TO-226AA) in tape and reel plus the ammo pack styles have also been added to Chapter 12.

Data Classification

Product Preview

This heading on a data sheet indicates that the device is in the formative stages or in design (under development). The disclaimer at the bottom of the first page reads: "This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice."

Advance Information

This heading on a data sheet indicates that the device is in sampling, pre-production, or first production stages. The disclaimer at the bottom of the first page reads: "This document contains information on a new product. Specifications and information herein are subject to change without notice."

Fully Released

A fully released data sheet contains neither a classification heading nor a disclaimer at the bottom of the first page. This document contains information on a product in full production. Guaranteed limits will not be changed without written notice to your local Motorola Semiconductor Sales Office.

Index and Cross Reference

In Brief . . .

Motorola linear and interface integrated circuits cover a much broader range of products than the traditional op amps, regulators and consumer-image associated with linear suppliers. Linear circuit technology currently influences the design and architecture of equipment for all major markets. As with other integrated circuit technologies, linear circuit design techniques and processes have been continually refined and updated to meet the needs of these diversified markets.

Operational amplifiers have utilized JFET inputs for improved performance, plus innovative design and trimming concepts have evolved for improved high performance and precision characteristics. In linear power ICs, basic voltage regulators have been refined to include higher current levels and more precise three-terminal fixed and adjustable voltages. The power area continues to expand into switching regulators, power supply control and supervisory circuits, and motor controllers.

Linear designs also offer a wide array of line drivers, receivers and transceivers for many of the EIA, European, IEEE and IBM interface standards. Peripheral drivers for a variety of devices are also offered. In addition to these key interface functions, a variety of magnetic and semiconductor memory read, write, sense and RAM control circuits are also available.

In data conversion, the original A-D and D-A converters have been augmented with high performance video speed and multiplying designs. Linear circuit technology has also provided precision low voltage references for use in data conversion and other low temperature drift applications.

A host of special purpose linear devices have also been developed. These circuits find applications in telecommications, radio, television, automotive, RF communications, and data transmission. These products have reduced the cost of RF communications, and have provided capabilities in telecommunications which make the telephone line convenient for both voice and data communications. Linear developments have also reduced the many discrete components formerly required for consumer functions to a few IC packages, and have made significant contributions to the rapidly growing market for electronics in automotive applications.

The table of contents provides a perspective of the many markets served by linear/interface ICs and of Motorola's involvement in these areas.

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Cross Reference

The following table represents a cross reference guide for all of Analog devices which are manufactured by Motorola. Where the Motorola part number differs from the industry part number, the Motorola device is a "form, fit and function" replacement for the industry part number. However, some differences in characteristics and/or specifications may exist.

Industry Part Number	Motorola Nearest Replacement	Motorla Similar Replacement
55110DM		MC75S110L
75107ADC	MC75107L	
75107APC	MC75107P	
75107BDC		MC75107L
75107BPC		MC75107P
75108ADC	MC75108L	
75108APC	MC75108P	
75108BDC		MC75108L
75108BPC		MC75108P
75110DC	MC75S110L	
75110PC	MC75S110P	
75207DC		MC75107L
75207PC		MC75108P
75208DC		MC75108L
75208PC		MC75108P
8216		MC8T26AL
9614DC		MC75S110L
9614DM		MC75S110L
9615DC		MC75108L
9616CDC		MC1488L
9616DM		MC1488L
90616EDC		MC1488L
9617DC		MC1489AL
9620DC		MC75S110L
9620DM		MC75S110L
9621DC		MC75108L
9627DC		MC1489AL
9627DM		MC1489AL
9636AT	MC3488AP	
9637T		MC3486P
9638T		MC3487P
9640DC	MC26S10L	
9640PC	MC26S10P	
9665DC	MC1411L	
9665PC	MC1411P	
9666DC	MC1412L	
9666PC	MC1412P	
9667DC	MC1413L	
9667PC	MC1413P	
9668DC	MC1416L	
9668PC	MC1416P	
AD1403AN		MC1403AU
AD1508-8D	MC1508L8	
AD530		MC1595L
AD531		MC1595L
AD532L		MC1595L
AD580J		MC1403U
AD580K		MC1403P1
AD580M		MC1403AP1
AD580S		MC1503U
AD580T		MC1503AU
AD589J		LM385Z-1.2
AD589K		LM385Z-1.2
AD589L		LM385Z-1.2
AD589M		LM385BZ-1.2
ADDAC-08CQ	DAC-08CQ	
ADDAC-08ED	DAC-08EQ	

Industry Part Number	Motorola Nearest Replacement	Motorla Similar Replacement
ADDAC-08HD	DAC-08HQ	
AM107	LM111J	
AM201AD		LM201AN
AM201D		LM201AN
AM26LS30D	AM26LS30D	
AM26LS30L	AM26LS30L	
AM26ALS30P	AM26LS30P	
AM26LS31CJ	AM26LS31PC	
AM26LS31CN	AM26LS31PC	
AM26LS31DS	AM26LS31DS	
AM26LS31P	AM26LS31P	
AM26LS32ACJ	AM26LS32D	
AM26LS32ACN	AM26LS32APC	
AM26LS32PC	AM26LS32PC	
AM26LS32P	AM26LS32PC	
AM26LS33DC		MC3486L
AM26LS33PC		MC3486P
AM26S10DC	MC26S10L	
AM301AD		LM301AJ
AM301D		LM301AJ
AM311D	LM311J-8	
AM723DC	MC1723CL	
AM723DM	MC1723L	
AM723P	MC1723CP	
AM741DC		MC1741CU
AM741DM		MC1741U
AM747DC	MC1747CL	
AM747DM	MC1747L	
AN5150		MC34129P
AN5151		MC13001P
CA081AE		TL081ACP
CA081AS		TL081ACJG
CA081CS		TL081CJG
CA081E		TL081CP
CA081S		TL081MJG
CA082AE		TL082ACP
CA082AS		TL082ACJG
CA082CS		TL082CJG
CA082E		TL082CP
CA082S		TL082MJG
CA084AE		TL084ACN
CA084E		TL084CN
CA084S		TL084MJ
CA1391E	MC1391P	
CA139AG	LM139AJ	
CA139G	LM139J	
CA1458S	MC1458CP1	
CA1558S		MC1558U
CA239AE	LM239AN	
CA239AG	LM239AJ	
CA239E	LM239N	
CA239G	LM239J	
CA3026		CA3054
CA3045F		MC3346P
CA3045		MC3346P
CA3046	MC3346P	
CA3048		MC3301P

Cross Reference (continued)

Industry Part Number	Motorola Nearest Replacement	Motorola Similar Replacement
CA3052		MC3301P
CA3054	CA3054	
CA3058		CA3059
CA3059	CA3059	
CA3079	CA3079	
CA3085AF		MC1723L
CA3086F		MC3346P
CA308AS	LM308N	
CA3091D		MC1594L
CA3136A		MC3346P
CA3146D		CA3146D
CA3146		MC3346P
CA3201E		TDA3301B
CA3210E		MC13001P
CA3217E		TDA3301B
CA3302E	MC3302N	
CA339AE	LM339AN	
CA339AG	LM339AJ	
CA339E	LM339N	
CA339G	LM339J	
CA3401E	MC3401P	
CA723CE	MC1723CP	
CA723E	MC1723L	
CA741CS	MC1741CP1	
CA741S	MC1741U	
CA747CE	MC1747CL	
CA747CF	MC1747CL	
CA747E	MC1747L	
CA747F	MC1747L	
CA748CS	MC1748CP1	
CS2842AD	UC2842BD1	
CS2843AD	UC2843BD1	
CS2844D	UC2844BD1	
CS2845D	UC2845BD1	
CS3471	MC3471P	
CS3842AD	UC3842BD1	
CS3843AD	UC3843DB1	
CS3844D	UC3844BD1	
CS3845D	UC3845BD1	
D8216		MC8T26AL
D8226		MC8T26L
DAC-08CD	DAC-08CD	
DAC-08CN		DAC-08CP
DAC-08CP	DAC-08CP	
DAC08CQ	DAC-08CQ	
DAC-08ED	DAC-08ED	
DAC-08EN		DAC-08EP
DAC-08EP	DAC-08EP	
DAC-08EQ	DAC-08EQ	
DAC-08HN		DAC-08HP
DAC-08HP	DAC-08HP	
DAC-08HQ	DAC-08HQ	
DAC0800LCJ	DAC-08EQ	
DAC0800LCN	DAC-08EP	
DAC0801LCJ	DAC-08CQ	
DAC0801LCN	DAC-08CP	
DAC0802LCJ	DAC-08HQ	
DAC0802LCN	DAC-08HP	
DAC0808LCJ	MC1408L8	
DAC0808LCN	MC1408P8	
DAC0808LD	MC1508L8	

Industry Part Number	Motorola Nearest Replacement	Motorola Similar Replacement
DM7822J		MC1489AL
DM7837J		MC3437L
DM8822J		MC1489AL
DM8822N		MC1489AP
DM8837N	MC3437P	
DS1488J	MC1488L	
DS1488N	MC1488P	
DS1489AJ	MC1489AL	
DS1489AN	MC1489AP	
DS1489J	MC1489L	
DS1489N	MC1489P	
DS26LS31N	AM26LS31P	
DS26LS32N	AM26LS32P	
DS26S10CJ	MC26S10L	
DS26S10CN	MC26S10P	
DS3486J	MC3486L	
DS3486N	MC3486P	
DS3487J	MC3487L	
DS3487N	MC3487P	
DS3612H		MC1472U
DS3612N		MC1472P1
DS3632H	MC1472U	
DS3632J	MC1472U	
DS3632N	MC1472P1	
DS3650J	MC3450L	
DS3650N	MC3450P	
DS3651J	MC3430L	
DS3651N	MC3430P	
DS3652J	MC3452L	
DS3652N	MC3452P	
DS3653J	MC3432L	
DS3653N	MC3432P	
DS55107W		MC75107L
DS55110J		MC75S110L
DS75107J	MC75107L	
DS75107N	MC75107P	
DS75108J	MC75108L	
DS75108N	MC75108P	
DS75110J	MC75S110L	
DS75110N	MC75S110P	
DS75207J		MC75107L
DS75207N		MC75107P
DS75208J		MC75108L
DS75208N		MC74108P
DS7837J		MC3437L
DS7837W		MC3437L
DS8834J		MC8T26AL
DS8834N		MC8T26AP
DS8835J		MC8T26AL
DS8835N		MC8T26AP
DS8837J	MC3437L	
DS8837N	MC3437P	
DS8922A		MC34051P
DS8923A		MC34050P
DS9636ACN	MC3488AP1	
ICL741CLNPA		MC1741CP1
ICL741CLNTY		MC1741CP1
ICL8001CTZ		LM111J
ICL8001MTZ		LM111J
ICL8008CPA		LM301AN
ICL8808CTY		LM301AN

Cross Reference (continued)

Industry Part Number	Motorola Nearest Replacement	Motorla Similar Replacement
ICL8013A		MC1594L
ICL8013B		MC1594L
ICL8013C		MC1594L
ICL8017CTW		LM301AN
ICL8017MTW		LM301AN
ICL8069CCZR		LM384BZ-1.2
ICL8069DCZR		LM385BZ-1,2
IP33063N	MC33063AP1	
IP34060AN	MC34060AP	
IP34063N	MC34063AP1	
IP35063J	MC35063AU	
IP3525AJ	SG3525AJ	
IP3525AN	SG3525AN	
IP3526J	SG3526J	
IP3526N	SG3526N	
IP3527AJ	SG3527AJ	
IP3527AN	SG3527AN	
IP494ACJ		TL594IN
IP494ACN		TL594CN
IP494AJ		TL594MJ
ITT3710		MC1391P
ITT652	MC1411P	
ITT654	MC1412P	
ITT656	MC1413P	
L144AP		LM324N
L201	MC1411P	
L202	MC1412P	
L203	MC1413P	
L387		MC33267
L583		MC3484S2
LF347BN	LF347BN	
LF347N	LF347N	
LF351AN		MC34001AP
LF351BN		MC34001BP
LF351N	LF351N	
LF352D		LF355J
LF353AN	MC34002AP	
LF353BN	MC34002BP	
LF353D	LF353D	
LF353N	LF353N	
LF356BJ	LF356BJ	
LF356BN		LF356J
LF356JG		LF356J
LF356J	LF356J	
LF356N		LF356J
LF356P		LF356J
LF357BJ	LF357BJ	
LD357BN		LF357BJ
LD357JG		LF357J
LF357J	LF357J	
LF357N		LF357J
LF357P		LF357J
LF411CD	LF411CD	
LF411CH		MC34001AG
LF412CD	LF411CD	
LF412CH		MC34002AG
LF441CD	LF441CD	
LF441CN	LF441CN	
LF442CD	LF442CD	
LF442CN	LF442CN	

Industry Part Number	Motorola Nearest Replacement	Motorla Similar Replacement
LF444CD	LF444CD	
LF444CN	LF444CN	
LF351AN		MC34001AP
LM101AJ-14		LM101AJ
LM101AJG	LM101AJ	
LM101AJ	LM101AJ	
LM101D		LM101AJ
LM101J-14		LM101AJ
LM1035		TCA5550
LM107L	MC1741L	
LM111J-8	LM111J-8	
LM111JG	LM111J-8	
LM11CLN	LM11CLN	
LM11CN	LM11CN	
LM124AD		LM124J
LM124AJ		LM124J
LM124J	LM124J	
LM124N	LM124N	
LM139AJ	LM139AJ	
LM139J	LM139J	
LM139N	MC1391P	
LM1408J8		MC1408L8
LM1408N8		MC1408P8
LM1489AN	MC1489AP	
LM1489J	MC1489L	
LM1489N	MC1489P	
LM1496J	MC1496L	
LM1496N	MC1496P	
LM149J		MC4741L
LM158JG		LM158J
LM158J	LM158J	
LM1558J	MC1558U	
LM1596J	MC1596L	
LM163J		MC3450L
LM1849A		MC3484S2
LM1889		MC1374P
LM1900D		MC3301P
LM1981		MC13020P
LM201AD	LM201AD	
LM201AJ-14		LM201AJ
LM201AJG	LM201AJ	
LM201AJ	LM201AJ	
LM201AN	LM201AN	
LM201AP		LM201AN
LM201J-14		LM201AJ
LM201J	LM201AJ	
LM211D	LM211D	
LM211J-8	LM211J-8	
LM211JG	LM211J-8	
LM211M	LM211D	
LM212H		MC1456U
LM224AF		LM224J
LM224AJ		LM224J
LM224D	LM224D	
LM224J	LM224J	
LM224M	LM224D	
LM224N	LM224N	
LM239AJ	LM239AJ	
LM239AN	LM239AN	
LM239D	LM239D	

Cross Reference (continued)

Industry Part Number	Motorola Nearest Replacement	Motorla Similar Replacement
LM239J	LM239J	
LM239M	LM239D	
LM239N	LM239N	
LM240LAZ-12		MC78L12ACP
LM240LAZ-15		MC78L15ACP
LM240LAZ-18		MC78L18ACP
LM240LAZ-24		MC78L24ACP
LM240LAZ-5.0		MC78L05ACP
LM204LAZ-6.0		MC78L05ACP
LM240LAZ-8.0		MC78L08ACP
LM248J	LM248J	
LM248N	LM248N	
LM249J		MC4741L
LM249N		MC4741P
LM258D	LM258D	
LM258J	LM258J	
LM258M	LM258D	
LM258N	LM258N	
LM285Z-1.2	LM258Z-1.2	
LM285Z-2.5	LM258Z-2.5	
LM2900N	LM2900N	
LM2901D	LM2901D	
LM2901M	LM2901D	
LM2901N	LM2901N	
LM2902D	LM2902D	
LM2902J	LM2902J	
LM2902M	LM2902D	
LM2902N	LM2902N	
LM2903D	LM2903D	
LM2903M	LM2903D	
LM2903N	LM2903N	
LM2903P	LM2903N	
LM2904J	LM2904J	
LM2904M	LM2904D	
LM2904N	LM2904N	
LM2905N		MC1455P1
LM2931ACT	LM2931ACT	
LM2931AD-5.0	LM2931AD-5.0	
LM2931AT-5.0	LM2931AT-5.0	
LM2931AZ-5.0	LM2931AZ-5.0	
LM2931CD	LM2931CD	
LM2931CM	LM2931CD	
LM2931CT	LM2931CT	
LM2931D-5.0	LM2931D-5.0	
LM2931D	LM2931D	
LM2931T-5.0	LM2931T-5.0	
LM2931Z-5.0	LM2931Z-5.0	
LM2935T	MC2935T	
LM293D	LM293D	
LM301AD	LM301AD	
LM301AJG	LM301AJ	
LM301AJ	LM301AJ	
LM301AM	LM301AD	
LM301AN	LM301AN	
LM301AP		LM301AN
LM3026		CA3054
LM3045		MC3346P
LM3046N	MC3346P	
LM3054	CA3054	
LM307N	LM307N	
LM307P		LM307N

Industry Part Number	Motorola Nearest Replacement	Motorla Similar Replacement
LM3089		MC3356P
LM311D	LM311D	
LM311J-8	LM311J-8	
LM331JG	LM311J-8	
LM311M	LM311D	
LM311N-14		LM311J-8
LM311N	LM311N	
LM311P	LM311N	
LM3146A		MC3346P
LM3146		MC3346P
LM317KC	LM317T	
LM317KD		LM317T
LM317LD	LM317LD	
LM317LZ	LM317LZ	
LM317MP		LM317MT
LM317P		LM317T
LM317T	LM317T	
LM3189		MC3356P
LM320LZ-12		MC79L12ACP
LM320LZ-15		MC79L15ACP
LM320LZ-5.0		MC79L05ACP
LM320MP-12		MC7912CT
LM320MP-15		MC7915CT
LM320MP-18		MC7918CT
LM320MP-24		MC7924CT
LM320MP-5.0		MC7905CT
LM320MP-5.2		MC7905.2CT
LM320MP-6.0		MC7906CT
LM320MP-8.0		MC7908CT
LM320T-12		MC7912CT
LM320T-15		MC7915CT
LM320T-5.0		MC7905CT
LM320T-5.2		MC7905.2CT
LM322N		MC1455P1
LM323AT	LM323AT	
LM323T	LM323T	
LM324AD	LM324AD	
LM324AJ		LM324J
LM324AN	LM324AN	
LM324D	LM324D	
LM324J	LM324J	
LM324M	LM324D	
LM324N	LM324N	
LM325AN		MC1468L
LM325N		MC1468L
LM326N		MC1468L
LM328AN		MC1468L
LM328N		MC1468L
LM3301N	MC3301L	
LM3302J	MC3302L	
LM3302N	MC3302P	
LM337MP		LM337MT
LM337MT	LM337MT	
LM337T	LM337T	
LM339AD	LM339AD	
LM339AJ	LM339AJ	
LM339AM	LM339AD	
LM339AN	LM339AN	
LM339D	LM339D	
LM339J	LM339J	
LM339N	LM339N	

Cross Reference (continued)

Industry Part Number	Motorola Nearest Replacement	Motorla Similar Replacement
LM339P		LM339N
LM3401N	MC3401P	
LM340AT-12	LM340AT-12	
LM340AT-15	LM340AT-15	
LM340AT-5.0	LM340AT-5.0	
LM340KC-12	LM340T-12	
LM340KC-15	LM340T-15	
LM340LAZ-12		MC78L12ACP
LM340LAZ-18		MC78L18ACP
LM340LAZ-24		MC78L24ACP
LM340LAZ-5.0		MC78L05ACP
LM340LAZ-8.0		MC78L08ACP
LM340T-12	LM340T-12	
LM340T-15	LM340T-15	
LM340T-18	LM340T-18	
LM340T-24	LM340T-24	
LM340T-5.0	LM340T-5.0	
LM340T-6.0	LM340T-6.0	
LM340T-8.0	LM340T-8.0	
LM341P-12		MC78M12CT
LM341P-15		MC78M15CT
LM341P-18		MC78M18CT
LM341P-24		MC78M24CT
LM341P-5.0		MC78M05CT
LM341P-6.0		MC78M06CT
LM341P-8.0		MC78M08CT
LM342P-12		MC78M12CT
LM342P-15		MC78M15CT
LM342P-18		MC78M18CT
LM342P-24		MC78M24CT
LM342P-5.0		MC78M05CT
LM342P-6.0		MC78M06CT
LM342P-8.0		MC78M08CT
LM348D	LM348D	
LM348J	LM348J	
LM348M	LM348D	
LM348N	LM348N	
LM349J		MC4741CL
LM349N		MC4741CP
LM350T	LM350T	
LM358AN		LM358N
LM358D	LM358D	
LM358JG	LM358J	
LM358J	LM358J	
LM358M	LM358D	
LM358N	LM358N	
LM363AJ		MC3450L
LM363AN		MC3450P
LM363J		MC3450L
LM363N		MC3450P
LM385BZ-1.2	LM385BZ-1.2	
LM385BZ-2.5	LM385BZ-2.5	
LM385D-1.2	LM385D-1.2	
LM385D-2.5	LM385D-2.5	
LM385M-1.2	LM385D-1.2	
LM385M-2.5	LM385D-2.5	
LM385Z-1.2	LM385Z-1.2	
LM385Z-2.5	LM385Z-2.5	
LM386N		MC34119P
LM3900D	LM3900D	
LM3900J	LM3900J	

Industry Part Number	Motorola Nearest Replacement	Motorla Similar Replacement
LM3900N	LM3900N	
LM3905N		MC1455P1
LM393AN	LM393AN	
LM393D	LM393D	
LM393JG		LM393N
LM393M	LM393D	
LM393N	LM393N	
LM4250CN		MC1776CP1
LM55109J		MC75S110L
LM55110J		MC75S110L
LM555CN	MC1455P1	
LM556CD	MC3456L	
LM556CJ	MC3456L	
LM556CN	MC3456P	
LM556L	MC3456L	
LM703LN		MC1350P
LM723CD	MC1723CL	
LM723CJ	MC1723CL	
LM723CN	MC1723CP	
LM723J	MC1723L	
LM741CD	MC1741CL	
LM741CJ-14	MC1741CL	
LM741EJ		MC1741CU
LM741EN		MC1741CP1
LM747CD	MC1747CL	
LM748CN	MC1748CP1	
LM75107AN	MC75107P	
LM75108AJ	MC75108L	
LM75108AN	MC75108P	
LM75110J	MC75S110L	
LM75110N	MC75S110P	
LM75207L		MC75107L
LM75207N		MC75107P
LM75208J		MC75108L
LM75208N		MC75108P
LM7805CT	MC7805CT	
LM7812CT	MC7812CT	
LM7815CT	MC7815CT	
LM78L05ACZ	MC78L05ACP	
LM78L05CZ	MC78L05CP	
LM78L08ACZ	MC78L08ACP	
LM78L08CZ	MC78L08CP	
LM78L12ACZ	MC78L12ACP	
LM78L12CZ	MC78L12CP	
LM78L15ACZ	MC78L15ACP	
LM78L15CZ	MC78L15CP	
LM78L18ACZ	MC78L18ACP	
LM78L18CZ	MC78L18CP	
LM78L24ACZ	MC78L24ACP	
LM78L24CZ	MC78L24CP	
LM78M06CP		MC78M05CT
LM78M12CP		MC78M12CT
LM78M15CP		MC78M15CT
LM7905CT	MC7905CT	
LM7912CT	MC7912CT	
LM7915CT	MC7915CT	
LM79L05ACZ	MC79L05ACP	
LM79L12ACZ	MC79L12ACP	
LM79L15ACZ	MC78L15ACP	
LM79M05CP		MC79M05CT
LM79M12CP		MC79M12CT

Cross Reference (continued)

Industry Part Number	Motorola Nearest Replacement	Motorla Similar Replacement
LM79M15CP		MC79M15CT
LM833D	LM833D	
LM833N	LM833N	
LM833P	LM833N	
LM837N		MC33079P
LMC6482D		MC33202D
LMC6482P		MC33202P
LMC6484D		MC33204D
LMC6484P		MC33204P
LT1083		MC34268
MB3759	TL494CN	
MP5531CP	MC1404U5	
MP5531DP	MC1404U5	
MP5532CP	MC1404U10	
MP5532DP	MC1404U10	
N5558F	MC1458U	
N5558V	MC1458P1	
N5595A	MC1495L	
N5595F	MC1495L	
N5596A	MC1496L	
N5723A		MC1723CP
N5741A		MC1741CP1
N5741V	MC1741CP1	
N5747A	MC1747CL	
N5747F	MC1747CL	
N8T15A		MC1488L
N8T15F		MC1488L
N8T16A		MC1489L
N8T26AB	MC8T26AP	
N8T26AE	MC8T26AL	
N8T26AJ	MC8T26AL	
N8T26AN	MC8T26AP	
N8T26B	MC8T26AP	
N8T26J	MC8T26AL	
N8T26N	MC8T26AP	
N8T37A	MC3437P	
N8T97B	MC8T97P	
N8T97F	MC8T97L	
N8T97N	MC8T97P	
N8T98B	MC8T98P	
N8T98F	MC8T98L	
N8T98N	MC8T98P	
NE550A		MC1723CP
NE555JG	MC1455U	
NE555D	MC1455D	
NE555V	MC1455P1	
NE556D	NE556D	
NE556F	MC3456L	
NE5561FE		MC34060AL
NE5561N		MC34060P
NE5234D		MC33204D
NE5234P		MC33204P
OP-01P		MC1436P1
PWM125CK	SG3525AJ	
RC1458DN	MC1458P1	
RC1488DC	MC1488L	
RC1489ADC	MC1489AL	
RC1489DC	MC1489L	
RC3302DB	MC3302P	
RC4136DP		MC3403P
RC4136D		MC3403L

Industry Part Number	Motorola Nearest Replacement	Motorla Similar Replacement
RC4136J		MC3403L
RC4136N		MC3403P
RC4194DC		MC1468L
RC4195NB		MC1468L
RC4558DN	MC4558CP1	
RC4558JG	MC4558CU	
RC4458P	MC4558CP1	
RC723DB	MC1723CP	
RC723DC	MC1723CL	
RC723D	MC1723CL	
RC741DN	MC1741CP1	
RC747D	MC1747CL	
RC75107ADP	MC75107P	
RC75107AD	MC75107L	
RC75108ADP	MC75108P	
RC75108AD	MC75108L	
RC75109DP		MC75S110P
RC75109D		MC75S110L
RC75110DP	MC75S110P	
RC75110D	MC75S110L	
REF-01CJ		MC1404U10
REF-01CP	MC1404U10	
REF-01CZ	MC1404U10	
REF-01DJ		MC1404U10
REF-01DP	MC1404U10	
REF-01DZ	MC1404U10	
REF-02CJ		MC1404U5
REF-02CP	MC1404U5	
REF-02CZ	MC1404U5	
REF-02DJ		MC1404U5
REF-02DP	MC1404U5	
REF-02DZ	MC1404U5	
RM4136D		MC3503L
RM4136J		MC3503L
RM4194DC		MC1568L
RM4558D	MC4558U	
RM4558JG	MC4558U	
RM723DC	MC1723L	
RM723D	MC1723L	
RM741DP	MC1741L	
RM747D	MC1747L	
RV3301DB	MC3301P	
S5558E	MC1558U	
S5596F	MC1596L	
SA555N	MC1455BP1	
SAA1042A		SAA1042AV
SAA1042		SAA1042V
SG107J		MC1741L
SG107T		MC1741L
SG111D	LM111J	
SG124J	LM124J	
SG1402N		MC1594L
SG1402T		MC1594L
SG1436M	MC1436U	
SG1458M	MC1458P1	
SG1468J	MC1468L	
SG1468N		MC1468L
SG1495D	MC1495L	
SG1495N		MC1495L
SG1496D	MC1496L	
SG1496N	MC1496P	

Cross Reference (continued)

Industry Part Number	Motorola Nearest Replacement	Motorla Similar Replacement
SG1501AD		MC1568L
SG1501AJ		MC1568L
SG1501AJ	MC1568L	
SG1502D		MC1568L
SG1502J		MC1568L
SG1502N		MC1568L
SG1503T		MC1503U
SG1503Y		MC1503U
SG1524J		TL494MJ
SG1568J	MC1568L	
SG1595D	MC1595L	
SG1596D	MC1596L	
SG201AM	LM201AN	
SG201AN		LM201AN
SG201M	LM201AN	
SG201N		LM201AN
SG211D	LM211J-8	
SG211M	LM211J-8	
SG224J	LM224J	
SG224N	LM224N	
SG2402N		MC1494L
SG2402T		MC1494L
SG2501AD		MC1468L
SG2501D	MC1468L	
SG2501J		MC1468L
SG2501N		MC1468L
SG2502J		MC1468L
SG2502N		MC1468L
SG2503M		MC1403AU
SG2503T		MC1403AU
SG2503Y		MC1403AU
SG300N		MC1723CP
SG301AM	LM301AN	
SG301AN		LM301AN
SG307J		LM307N
SG307M	LM307N	
SG307N		LM307N
SG308AM	LM308AN	
SG311D	LM311J	
SG311M	LM311N	
SG317P	LM317T	
SG317R		LM317T
SG324J	LM324J	
SG324N	LM324N	
SG337P	LM337T	
SG337R		LM337T
SG3402N		MC1494L
SG3402T		MC1494L
SG3423M		MC3423P1
SG3423Y		MC3423U
SG3501AD		MC1468L
SG3501AJ		MC1468L
SG3501AN		MC1468L
SG3501D		MC1468L
SG3501J		MC1468L
SG3501N		MC1468L
SG3502D		MC1468L
SG3502J		MC1468L
SG3502N		MC1468L
SG3503M		MC1403U
SG3503T		MC1403U

Industry Part Number	Motorola Nearest Replacement	Motorla Similar Replacement
SG3503Y	MC1403U	
SG3523Y		MC3523U
SG3524J		TL494CJ
SG3525AJ	SG3525AJ	
SG3525AN	SG3525AN	
SG3526J	SG3526J	
SG3526N	SG3526N	
SG3527AJ	SG3527AJ	
SG3527AN	SG3527AN	
SG3561	MC34261	
SG4194CJ		MC1468L
SG4194J		MC1568L
SG4250CM		MC1775CP1
SG4501D	MC1468L	
SG4501J		MC1468L
SG4501N		MC1468L
SG555CM	MC1455P1	
SG556CJ		MC3456L
SG556CN	MC3456P	
SG556J	MC3456L	
SG723CD		MC1723CL
SG723CJ	MC1723CL	
SG723CN	MC1723CP	
SG723D		MC1723L
SG723J	MC1723L	
SG741CM	MC1741CP1	
SG747CJ	MC1747CL	
SG747CN	MC1747CP2	
SG747J	MC1747L	
SG748CD		MC1748CP1
SG748CM		MC1748CP1
SG748CN		MC1748CP1
SG777CN		LM308AN
SG7805ACP	MC7805ACT	
SG7805ACR		MC7805ACT
SG7805ACT		MC7805ACT
SG7805CP	MC7805CT	
SG7806ACP	MC7806ACT	
SG7806ACR		MC7806ACT
SG7806ACT		MC7806ACT
SG7806CP	MC7806CT	
SG7806CR		MC7806CT
SG7808ACP	MC7808ACT	
SG7808ACT		MC7808ACT
SG7808CP	MC7808CT	
SG7808CR		MC7808CT
SG7812ACP	MC7812ACT	
SG7812ACR		MC7812ACT
SG7812ACT		MC7812ACT
SG7812CP	MC7812CT	
SG7812CR		MC7812CT
SG7815ACP	MC7815ACT	
SG7815ACR		MC7815ACT
SG7815ACT		MC7815ACT
SG7815CP	MC7815CT	
SG7815CR		MC7815CT
SG7815CT		MC7815CT
SG7818ACP	MC7818ACT	
SG7818ACR		MC7818ACT
SG7818ACT		MC7818ACT
SG7818CP	MC7818CT	

Cross Reference (continued)

Industry Part Number	Motorola Nearest Replacement	Motorla Similar Replacement
SG7818CR		MC7818CT
SG7824ACP	MC7824ACT	
SG7824ACR		MC7824ACT
SG7824ACT		MC7824ACT
SG7824CP	MC7824CT	
SG7824CR		MC7824CT
SG7905.2CP	MC7905.2CT	
SG7905.2CR		MC7905.2CT
SG7905.2CT		MC7905.2CT
SG7905ACP	MC7905ACT	
SG7905ACR		MC7905ACT
SG7905ACT		MC7905ACT
SG7905CP	MC7905CT	
SG7905CR		MC7905CT
SG7905CT		MC7905CT
SG7908CP	MC7908CT	
SG7908CR		MC7908CT
SG7908CT		MC7908CT
SG7912ACP	MC7912ACT	
SG7912ACR		MC7912ACT
SG7912ACT		MC7912ACT
SG7912CP	MC7912CT	
SG7912CR		MC7912CT
SG7912CT		MC7912CT
SG7915ACP	MC7915ACT	
SG7915ACR		MC7915ACT
SG7915ACT		MC7915ACT
SG7915CP	MC7915CT	
SG7915CR		MC7915CT
SG7915CT		MC7915CT
SG7918CP	MC7918CT	
SH8090FM		MC1508L8
SN75107AJ	MC75107L	
SN75107AN	MC75107P	
SN75107BJ		MC75107L
SN75107BN		MC75107P
SN75108AJ	MC75108L	
SN75108AN	MC75108P	
SN75108BJ		MC75108L
SN75108BN		MC75108P
SN75110AJ	MC75S110L	
SN75110AN	MC75S110P	
SN75121J		MC3481/5L
SN75121N		MC3481/5P
SN75125N		MC3481/5L
SN75126J		MC3481/5L
SN75126N		MC3481/5P
SN75150J		MC1488L
SN75150N		MC1488P
SN75154J		MC1489L
SN75154N		MC1489P
SN75160J		MC3447L
SN75160N		MC3447P/P3
SN75172N	MC75172BP	
SN75173J	SN75173J	
SN75173N	SN75173N	
SN75174N	MC75174BP	
SN75175J	SN75175J	
SN75175N	SN75175N	
SN75188J	MC1488L	
SN75188N	MC1488P	

Industry Part Number	Motorola Nearest Replacement	Motorla Similar Replacement
SN75189AJ	MC1489AL	
SN75189AN	MC1489AP	
SN75189J	MC1489L	
SN75189N	MC1489P	
SN75207J		MC75107L
SN75207N		MC75107P
SN75208J		MC75108L
SN75208N		MC75108P
SN75251N		MC3471P
SN75466J	MC1411L	
SN75466N	MC1411P	
SN75467J	MC1412L	
SN75467N	MC1412P	
SN75468J	MC1413L	
SN75468N	MC1413P	
SN75475JG	MC1472U	
SN75475P	MC1472P1	
SN76514N	MC1496P	
SN76591P	MC1391P	
SN76600P	MC1350P	
SSS140BA-8Z	MC1408L8	
SSS150BA-8Z	MC1508L8	
SSS201AP	LM201AN	
SSS301AP	LM301AN	
SSS747BP		MC1747L
SSS747CP		MC1747CL
SSS747GP		MC1747L
SSS747P		MC1747L
TA7179P	MC1468L	
TA7504P	MC1741CP1	
TA7506P	LM301AN	
TA75071P		MC34001P
TA75072P		MC34002P
TA75074F		MC34004P
TA75339F	LM339D	
TA75339P	LM339N	
TA75358CF	LM358D	
TA75358CP	LM358N	
TA75393F	LM393D	
TA75393P	LM393N	
TA75458F	MC1458D	
TA75458P	MC1458CP1	
TA75558P	MC4558CP1	
TA7555F	MC1455D	
TA7555P	MC1455P1	
TA75902F	LM324D	
TA76494P		TL494IN
TA78005AP	MC7805CT	
TA78006AP	MC7806CT	
TA78008AP	MC7808CT	
TA78012AP	MC7812CT	
TA78015AP	MC7815CT	
TA78018AP	MC7818CT	
TA78024AP	MC7824CT	
TA78L005AP		MC78L05ACP
TA78L005P		MC78L05CP
TA78L008AP		MC78L08ACP
TA78L008P		MC78L08CP
TA78L012AP		MC78L12ACP
TA78L012P		MC78L12CP
TA78L015AP		MC78L15ACP

Cross Reference (continued)

Industry Part Number	Motorola Nearest Replacement	Motorla Similar Replacement
TA78L015P		MC78L15CP
TA78L018AP		MC78L18ACP
TA78L018P		MC78L18CP
TA78L024AP		MC78L24ACP
TA78L024P		MC78L24CP
TA78M05P	MC78M05CT	
TA78M06P	MC78M06CT	
TA78M08P	MC78M08CT	
TA78M12P	MC78M12CT	
TA78M18P	MC78M18CT	
TA78M20P	MC78M20CT	
TA78M24P	MC78M24CT	
TA79005P	MC7905CT	
TA79006P	MC7906CT	
TA79008P	MC7908CT	
TA79012P	MC7912CT	
TA79015P	MC7915CT	
TA79018P	MC7918CT	
TA79024P	MC7924CT	
TA79L005P		MC79L05CP
TA79L012P		MC79L12P
TA79L015P		MC79L15P
TA79L018P		MC79L18P
TA79L024P		MC79L24P
TB920		MC1391P
TBA920S		MC1391P
TCA5600	TCA5600	
TCF5600	TCF5600	
TD62001P/AP	MC1411P	
TD62002P/AP	MC1412P	
TD62003P/AP	MC1413P	
TD62477P	MC1472P	
TD62479P	MC1374P	
TDA1085A	TDA1085A	
TDA1085C	TDA1085C	
TDA1085	TDA1085C	
TDA1185A	TDA1185A	
TDA3301B	TDA3301B	
TDA4817	MC34261	
TDC1048		MC10319P
TLC2272D		MC33202D
TLC2272P		MC33202P
TLC2274D		MC33204D
TLC2274P		MC33204P
TL022CJG		LM358J
TL022CP		LM358N
TL022MJG		LM158J
TL044CJ		LM324N
TL044MJ		LM124J
TL062ACP	TL062ACP	
TL062CD	TL062CD	
TL062CP	TL062CP	
TL062MJG	TL062MJG	
TL062VP	TL062VP	
TL064ACD	TL064ACD	
TL064ACN	TL064ACN	
TL064CD	TL064CD	
TL064CN	TL064CN	
TL064MJ	TL064MJ	
TL064VN	TL064VN	
TL071ACD	TL071ACD	

Industry Part Number	Motorola Nearest Replacement	Motorla Similar Replacement
TL071ACJG	TL071ACJG	
TL071ACP	TL071ACP	
TL071CD	TL071CD	
TL071CJG	TL071CJG	
TL071CP	TL071CP	
TL071MJG	TL071MJG	
TL072ACD	TL072ACD	
TL072ACJG	TL072ACJG	
TL072ACP	TL072ACP	
TL072CD	TL072CD	
TL072CJG	TL072CJG	
TL072CP	TL072CP	
TL072MJG	TL072MJG	
TL074ACJ	TL074ACJ	
TL074ACN	TL074ACN	
TL074CJ	TL074CJ	
TL074CN	TL074CN	
TL074MJ	TL074MJ	
TL081ACD	TL081ACD	
TL081ACJG	TL081ACJG	
TL081ACP	TL081ACP	
TL081CD	TL081CD	
TL081CJG	TL081CJG	
TL081CP	TL081CP	
TL081MJG	TL081MJG	
TL082ACJG	TL082ACJG	
TL082ACP	TL082ACP	
TL082CD	TL082CD	
TL082CJG	TL082CJG	
TL082CP	TL082CP	
TL082MJG	TL082MJG	
TL084ACJ	TL084ACJ	
TL084ACN	TL084ACN	
TL084CJ	TL084CJ	
TL084CN	TL084CN	
TL084MJ	TL084MJ	
TL1431		TL431
TL431CD	TL431CD	
TL431CJG	TL431CJG	
TL431CLP	TL431CLP	
TL431CP	TL431CP	
TL431IJG	TL431IJG	
TL431ILP	TL431ILP	
TL431IP	TL431IP	
TL431MJG	TL431MJG	
TL494CJ	TL494CJ	
TL494CN	TL494CN	
TL494IJ	TL494IJ	
TL494IN	TL494IN	
TL494MJ	TL494MJ	
TL497CJ		MC34063AU
TL497CN		MC34063AP1
TL497MJ		MC35063AU
TL594CN	TL594CN	
TL594IN	TL594IN	
TL594MJ	TL594MJ	
TL780-05CKC	TL780-05CKC	
TL780-12CKC	TL780-12CKC	
TL780-15CKC	TL780-15CKC	
TL7805ACKC	MC7805ACT	
µA0802DC-1	MC1408L8	

Cross Reference (continued)

Industry Part Number	Motorola Nearest Replacement	Motorla Similar Replacement
µA0802DC-2	MC1408L8	
µA0802DC-3	MC1408L8	
µA0802DM-1	MC1508L8	
µA0802PC-1	MC1408P8	
µA0802PC-2	MC1408P8	
µA0802PC-3	MC1408P8	
µA101AD		LM101AJ
µA101AF		LM101AJ
µA101D		LM101AJ
µA101F		LM101AJ
µA1391PC	MC1391P	
µA1458CP	MC1458CP1	
µA1458CRC	MC1458CU	
µA1458CTC	MC1458CP1	
µA1458P	MC1458P1	
µA1458RC	MC1458U	
µA1458TC	MC1458P1	
µA201AD		LM201AJ
µA201AF		LM201AJ
µA201D		LM201AJ
µA201F		LM201AJ
µA2240DC		MC1455U
µA2240PC		MC1455P1
µA301AD		LM301AJ
µA301AT	LM301AN	
µA3026HM		CA3054
µA3045		MC3346P
µA3046DC	MC3346P	
µA3054DC	CA3054P	
µA307T	LM307N	
µA311T	LM311N	
µA317UC	LM317T	
µA3301P	MC3301P	
µA3302P	MC3302P	
µA3303P	MC3303P	
µA3401P	MC3401P	
µA3403D	MC3403L	
µA3403P	MC3403P	
µA4136DC		MC4741CL
µA4136DM		MC4741L
µA4136PC		MC4741CP
µA431AWC	TL431CP	
µA4558TC	MC4558CP1	
µA494DC	TL494CJ	
µA494DM	TL494MJ	
µA494PC	TL494CN	
µA555TC	MC1455P1	
µA556DC	MC3456L	
µA556PC	MC3456P	
µA723CF	MC1723CL	
µA723CJ	MC1723CL	
µA723CN	MC1723CP	
µA723DC	MC1723CL	
µA723DM	MC1723L	
µA723F	MC1723L	
µA723MJ	MC1723L	
µA723PC	MC1723CP	
µA734DC		LM311J
µA734DM		LM311J
µA741ADM		MC1741L
µA741CJG	MC1741CU	

Industry Part Number	Motorola Nearest Replacement	Motorla Similar Replacement
µA741CP	MC1741CP1	
µA741MJG	MC1741U	
µA741RC	MC1741CU	
µA741RM	MC1741U	
µA742DC		CA3059
µA747ADM		MC1747L
µA747CN	MC1747CP2	
µA747DC	MC1747CL	
µA747DM	MC1747L	
µA747EDC	MC1747CL	
µA747MJ	MC1747L	
µA747PC	MC1747CP2	
µA748CP	MC1748CP1	
µA748TC	MC1748CP1	
µA757DC		MC1350P
µA757DM		MC1350P
µA775DC	LM339J	
µA775DM	LM339J	
µA775PC	LM339N	
µA776TC	MC1776CP1	
µA7805CKC	MC7805CT	
µA7805UC	MC7805CT	
µA7805UV	MC7805BT	
µA7806CKC	MC7806CT	
µA7806UC	MC7806CT	
µA7806UV	MC7806BT	
µA7808CKC	MC7808CT	
µA7808UC	MC7808CT	
µA7808UV	MC7808BT	
µA7812CKC	MC7812CT	
µA7812UC	MC7812CT	
µA7812UV	MC7812BT	
µA7815CKC	MC7815CT	
µA7815UC	MC7815CT	
µA7815UV	MC7815BT	
µA7818CKC	MC7818CT	
µA7818UC	MC7818CT	
µA7818UV	MC7818BT	
µA7824CKC	MC7824CT	
µA7824UC	MC7824CT	
µA7824UV	MC7824BT	
µA78GU1C		LM317T
µA78GUC		LM317T
µA78L05ACLP	MC78L05ACP	
µA78L05AWC		MC78L05ACP
µA78L05CLP	MC78L05CP	
µA78L05WC		MC78L05CP
µA78L08ACLP	MC78L08ACP	
µA78L08AWC		MC78L08ACP
µA78L08CLP	MC78L08CP	
µA78L12ACLP	MC78L12ACP	
µA78L12AWC		MC78L12ACP
µA78L12CLP	MC78L12CP	
µA78L12WC		MC78L12CP
µA78L15ACLP	MC78L15ACP	
µA78L15AWC		MC78L15ACP
µA78L15CLP	MC78L15CP	
µA78L15WC		MC78L15CP
µA78L18AWC		MC78L18ACP
µA78L24AWC	MC78L24ACP	
µA78M05CKC	M78M05CT	

Cross Reference (continued)

Industry Part Number	Motorola Nearest Replacement	Motorola Similar Replacement
µA78M05CKD		MC78M05CT
µA78M05UC	MC78M05CT	
µA78M06CKC	MC78M06CT	
µA78M06CKD		MC78M06CT
µA78M06UC	MC78M06CT	
µA78M08CKC	MC78M08CT	
µA78M08CKD		MC78M08CT
µA78M08UC	MC78M08CT	
µA78M12CKC	MC78M12CT	
µA78M12CKD		MC78M12CT
µA78M12UC	MC78M12CT	
µA78M15CKC	MC78M15CT	
µA78M15CKD		MC78M15CT
µA78M15UC	MC78M15CT	
µA78M18UC	MC78M18CT	
µA78M20CKC	MC78M20CT	
µA78M20CKD		MC78M20CT
µA78M20UC	MC78M20CT	
µA78M24CKC	MC78M24CT	
µA78M24CKD		MC78M24CT
µA78M24UC	MC78M24CT	
µA78MGT2C		LM317T
µA78MGU1C		LM317T
µA78MGUC		LM317MT
µA78S40DC	µA78S40DC	
µA78S40DM	µA78S40DM	
µA78S40PC	µA78S40PC	
µA78S40PV	µA78S40PV	
µA7905.2CKC	MC7905.2CT	
µA7905CKC	MC7905CT	
µA7905UC	MC7905CT	
µA7906CKC	MC7906CT	
µA7906UC	MC7906CT	
µA7908CKC	MC7908CT	
µA7912CKC	MC7912CT	
µA7912UC	MC7912CT	
µA7915CKC	MC7915CT	
µA7915UC	MC7915CT	
µA7918CKC	MC7918CT	
µA7918UC	MC7818CT	
µA7924CKC	MC7924CT	
µA7924UC	MC7924CT	
µA796DC	MC1496L	
µA796DM	MC1596L	
µA798RC	MC3458U	
µA798RM	MC3558U	
µA798TC	MC3458P1	
µA79L05AWC	MC79L05ACP	
µA79L05WC	MC79L05CP	
µA79L12AWC	MC79L12ACP	
µA79L12WC	MC79L12CP	
µA79L15AWC	MC79L15ACP	
µA79L15WC	MC79L15CP	
µA79M05AUC	MC79M05CT	
µA79M05CKC	MC79M05CT	
µA79M06AUC		MC7906CT
µA79M06CKC		MC7906CT
µA79M06UC		MC7906CT
µA79M08AUC		MC7908CT
µA79M08CKC		MC7908CT
µA79M08UC		MC7908CT

Industry Part Number	Motorola Nearest Replacement	Motorola Similar Replacement
µA79M12AUC	MC79M12CT	
µA79M12CKC	MC79M12CT	
µA79M18AUC		MC7918CT
µA79M18UC		MC7918CT
µA79M24AUC		MC7924CT
µA79M24CKC		MC7924CT
µA79M24UC		MC7924CT
µA9636ATC	MC3488AP1	
UAA1016B	UAA1016B	
UC2842AD	UC2842AD	
UC2842AJ	UC2842AJ	
UC2842AN	UC2842AN	
UC2842BD	UC2842BD	
UC2842BN	UC2842BN	
UC2842D	UC2842AD	
UC2842N	UC2842AN	
UC2843AD	UC2843AD	
UC2843AJ	UC2843AJ	
UC2843AN	UC2843AN	
UC2843BD	UC2843BD	
UC2843BN	UC2843BN	
UC2843D	UC2843AD	
UC2843N	UC2843AN	
UC2844BD	UC2844BD	
UC2844BN	UC2844BN	
UC2844D	UC2844D	
UC2844J	UC2844J	
UC2844N	UC2844N	
UC2845BD	UC2845BD	
UC2845BN	UC2845BN	
UC2845D	UC2845D	
UC2845J	UC2845J	
UC2845N	UC2845N	
UC317T	LM317T	
UC337T	LM337T	
UC3525AJ	SG3525AJ	
UC3525AN	SG3525AN	
UC3526J	SG3526J	
UC3526N	SG3526N	
UC3527AJ	SG3527AJ	
UC3527AN	SG3527AN	
UC3823		MC34023
UC3825		MC34025
UC3842AD	UC3842AD	
UC3842AN	UC3842AN	
UC3842BD	UC3842BD	
UC3842BN	UC3842BN	
UC3842D	UC3842AD	
UC3842N	UC3842AN	
UC3843AD	UC3843AD	
UC3843AN	UC3843AN	
UC3843BD	UC3843BD	
UC3843BN	UC3843BN	
UC3843D	UC3843AD	
UC3843N	UC3843AN	
UC3844BD	UC3844BD	
UC3844BN	UC3844BN	
UC3844D	UC3844D	
UC3844J	UC3844J	
UC3844N	UC3844N	
UC3845BD	UC3845BD	

Cross Reference (continued)

Industry Part Number	Motorola Nearest Replacement	Motorla Similar Replacement
UC3845BN	UC3845BN	
UC3845D	UC3845D	
UC3845N	UC3845N	
UC494ACN		TL594CN
UC494AJ		TL594MJ
UC494CN		TL494CN
UC494J		TL494MJ
UCN5816A	MC34142	
UDN5712M	MC1472P1	
ULN2068BB	ULN2068B	
ULN2068NE	ULN2068B	
ULN2151H	MC1741CP1	
ULN2151M		MC1741CP1
ULN2747A		MC1747CL
ULN2801A	ULN2801A	
ULN2802A	ULN2802A	
ULN2803A	ULN2803A	
ULN2804A	ULN2804A	

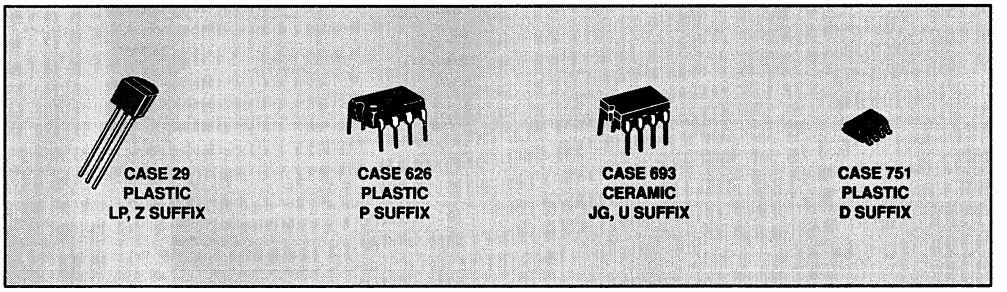
Industry Part Number	Motorola Nearest Replacement	Motorla Similar Replacement
ULN8126A	SG3526N	
ULN8126R	SG3526J	
ULQ8126R	SC3526J	
ULS2151M		MC1741CP1
ULS2157A		MC1558U
ULS2157H		MC1558U
ULX8161M		MC34060P
UPC1373		MC3373P
UPD6950C		MC10319P
UVC3101		MC10319P
XR082CN	TL082CJG	
XR082CP	TL082CP	
XR082M	TL082MJG	
XR084CN	TL084CJ	
XR084CP	TL084CN	
XR084M	TL084MJ	
XR3470A	MC3470AP	

Voltage References

5

In Brief . . .

Motorola's line of precision voltage references is designed for applications requiring high initial accuracy, low temperature drift, and long term stability. Initial accuracies of ± 1.0%, and ± 2.0% mean production line adjustments can be eliminated. Temperature coefficients of 25 ppm/°C maximum (typically, 10 ppm/°C) provide excellent stability. Uses for the references include D/A converters, A/D converters, precision power supplies, voltmeter systems, temperature monitors, and many others.



Precision Low Voltage References

5

A family of precision low voltage bandgap reference devices designed for applications requiring low temperature drift.

Precision Low Voltage References

V_{out} (V) Typ	I_O (mA) Max	V_{out}/T ppm/°C Max	Device		Reg_{line} (mV) Max	Reg_{load} (mV) Max	Suffix/ Package
			0° to + 70°C	– 55° to +125°C – 40° to + 85°C			
1.235 ± 12 mV 1.235 ± 25 mV	20	80 Typ	LM385BZ-1.2 LM385Z-1.2	LM285Z-1.2 (–40° to +85°C)	(Note 1)	1.0 (Note 2)	Z/29
2.5 ± 38 mV 2.5 ± 75 mV			LM385BZ-2.5 LM385Z-2.5	LM285Z-2.5 (–40° to +85°C)		2.0 (Note 3)	
2.5 ± 25 mV	10	25	MC1403A	MC1503A	3.0/4.5 (Note 4)	10 (Note 6)	U/693, D/751
		40	MC1403	—			
		55	—	MC1503			
5.0 ± 50 mV		25	MC1404AU5	—	6.0 (Note 5)		U/693
		40	MC1404U5	—			
		55	—	MC1504U5			
6.25 ± 60 mV		25	MC1404AU6	—			
		40	MC1404U6	—			
		55	—	MC1504U6			
10 ± 100 mV		25	MC1404AU10	—			
		40	MC1404U10	—			
		55	—	MC1504U10			
2.5 to 37	100	50 Typ	TL431C, AC, BC	TL431I, AI, BI (–40° to +85°C)	Shunt Reference Dynamic Impedance (z) ≤ 0.5 Ω		LP/29, P/626 JG/693, D/751
				TL431M			JG/693

Notes: 1. Micropower Reference Diode Dynamic Impedance (z) ≤ 1.0 Ω at I_R = 100 μA
2. 10 μA ≤ I_R ≤ 1.0 mA
3. 20 μA ≤ I_R ≤ 1.0 mA
4. 4.5 V ≤ V_{in} ≤ 15 V/15 V ≤ V_{in} ≤ 40V
5. (V_{out} + 2.5 V) ≤ V_{in} ≤ 40V
6. 0 mA ≤ I_L ≤ 10 mA

Voltage References

LM285
LM385

MICROPOWER VOLTAGE REFERENCE DIODES

SILICON MONOLITHIC INTEGRATED CIRCUIT

5

MICROPOWER VOLTAGE REFERENCE DIODES

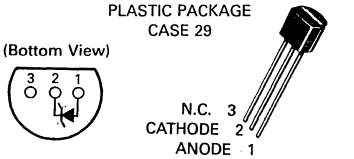
The LM285/LM385 series are micropower two-terminal band-gap voltage regulator diodes. Designed to operate over a wide current range of 10 μA to 20 mA, these devices feature exceptionally low dynamic impedance, low noise and stable operation over time and temperature. Tight voltage tolerances are achieved by on-chip trimming. The large dynamic operating range enables these devices to be used in applications with widely varying supplies with excellent regulation. Extremely low operating current make these devices ideal for micropower circuitry like portable instrumentation, regulators and other analog circuitry where extended battery life is required.

The LM285/LM385 series are packaged in a low cost TO-226AA plastic case and are available in two voltage versions of 1.235 and 2.500 volts as denoted by the device suffix (see ordering information table). The LM285 is specified over a −40°C to +85°C temperature range while the LM385 is rated from 0°C to +70°C.

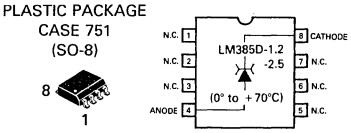
The LM385 is also available in a surface mount plastic package in voltages of 1.235 and 2.500 volts.

- Operating Current from 10 μA to 20 mA
- 1.0%, 1.5%, 2.0% and 3.0% Initial Tolerance Grades
- Low Temperature Coefficient
- 1.0 Ω Dynamic Impedance
- Surface Mount Package Available

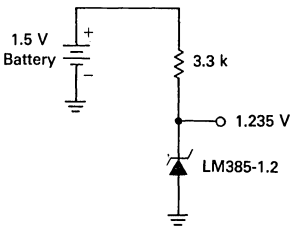
Z SUFFIX
PLASTIC PACKAGE
CASE 29



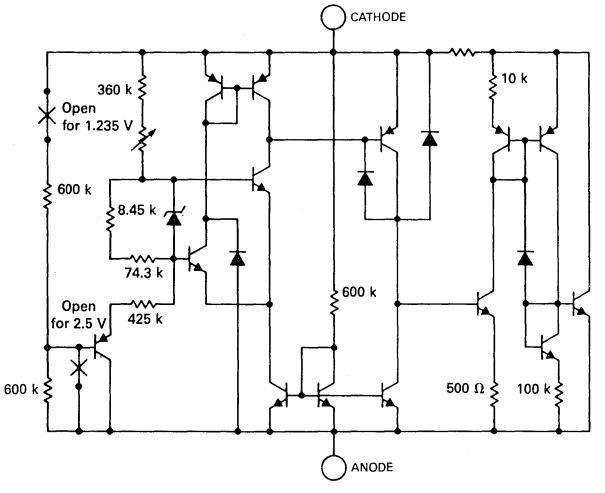
D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO-8)



STANDARD APPLICATION



EQUIVALENT CIRCUIT SCHEMATIC



ORDERING INFORMATION

Device	Temp. Range	Reverse Breakdown Voltage	Tolerance
LM285D-1.2 LM285Z-1.2	−40°C to +85°C	1.235 Volts	±1.0%
LM285D-2.5 LM285Z-2.5		2.500 Volts	±1.5%
LM385BD-1.2 LM385BZ-1.2	0°C to +70°C	1.235 Volts	±1.0%
LM385D-1.2 LM385Z-1.2		1.235 Volts	±2.0%
LM385BD-2.5 LM385BZ-2.5		2.500 Volts	±1.5%
LM385D-2.5 LM385Z-2.5		2.500 Volts	±3.0%

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Reverse Current	I_R	30	mA
Forward Current	I_F	10	mA
Operating Ambient Temperature Range LM285 LM385	T_A	 −40 to +85 0 to +70	°C
Operating Junction Temperature	T_J	+150	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	LM285-1.2 Min	LM285-1.2 Typ	LM285-1.2 Max	LM385-1.2/LM385B-1.2 Min	LM385-1.2/LM385B-1.2 Typ	LM385-1.2/LM385B-1.2 Max	Unit
Reverse Breakdown Voltage $I_{Rmin} \leq I_R \leq 20$ mA	$V_{(BR)R}$							V
LM285-1.2/LM385B-1.2		1.223	1.235	1.247	1.223	1.235	1.247	
$T_A = T_{low}$ to T_{high} (Note 1)		1.200	—	1.270	1.210	—	1.260	
LM385-1.2		—	—	—	1.205	1.235	1.260	
$T_A = T_{low}$ to T_{high} (Note 1)		—	—	—	1.192	—	1.273	
Minimum Operating Current	I_{Rmin}							μA
T_A = 25°C		—	8.0	10	—	8.0	15	
$T_A = T_{low}$ to T_{high} (Note 1)		—	—	20	—	—	20	
Reverse Breakdown Voltage Change with Current	$\Delta V_{(BR)R}$							mV
$I_{Rmin} \leq I_R \leq 1.0$ mA, T_A = +25°C		—	—	1.0	—	—	1.0	
$T_A = T_{low}$ to T_{high} (Note 1)		—	—	1.5	—	—	1.5	
1.0 mA $\leq I_R \leq$ 20 mA, T_A = +25°C		—	—	10	—	—	20	
$T_A = T_{low}$ to T_{high} (Note 1)		—	—	20	—	—	25	
Reverse Dynamic Impedance I_R = 100 μA, T_A = +25°C	Z	—	0.6	—	—	0.6	—	Ω
Average Temperature Coefficient 10 μA $\leq I_R \leq$ 20 mA, $T_A = T_{low}$ to T_{high} (Note 1)	$\Delta V_{(BR)}/\Delta T$	—	80	—	—	80	—	ppm/°C
Wideband Noise (RMS) I_R = 100 μA, 10 Hz ≤ f ≤ 10 kHz	n	—	60	—	—	60	—	μV
Long Term Stability I_R = 100 μA, T_A = +25°C ± 0.1°C	S	—	20	—	—	20	—	ppm/kHR

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	LM285-2.5 Min	LM285-2.5 Typ	LM285-2.5 Max	LM385-2.5/LM385B-2.5 Min	LM385-2.5/LM385B-2.5 Typ	LM385-2.5/LM385B-2.5 Max	Unit
Reverse Breakdown Voltage $I_{Rmin} \leq I_R \leq 20$ mA	$V_{(BR)R}$							V
LM285-2.5/LM385B-2.5		2.462	2.5	2.538	2.462	2.5	2.538	
$T_A = T_{low}$ to T_{high} (Note 1)		2.415	—	2.585	2.436	—	2.564	
LM385-2.5		—	—	—	2.425	2.5	2.575	
$T_A = T_{low}$ to T_{high} (Note 1)		—	—	—	2.400	—	2.600	
Minimum Operating Current	I_{Rmin}							μA
T_A = 25°C		—	13	20	—	13	20	
$T_A = T_{low}$ to T_{high} (Note 1)		—	—	30	—	—	30	
Reverse Breakdown Voltage Change with Current	$\Delta V_{(BR)R}$							mV
$I_{Rmin} \leq I_R \leq 1.0$ mA, T_A = +25°C		—	—	1.0	—	—	2.0	
$T_A = T_{low}$ to T_{high} (Note 1)		—	—	1.5	—	—	2.5	
1.0 mA $\leq I_R \leq$ 20 mA, T_A = +25°C		—	—	10	—	—	20	
$T_A = T_{low}$ to T_{high} (Note 1)		—	—	20	—	—	25	
Reverse Dynamic Impedance I_R = 100 μA, T_A = +25°C	Z	—	0.6	—	—	0.6	—	Ω
Average Temperature Coefficient 20 μA $\leq I_R \leq$ 20 mA, $T_A = T_{low}$ to T_{high} (Note 1)	$\Delta V_{(BR)}/\Delta T$	—	80	—	—	80	—	ppm/°C
Wideband Noise (RMS) I_R = 100 μA, 10 Hz ≤ f ≤ 10 kHz	n	—	120	—	—	120	—	μV
Long Term Stability I_R = 100 μA, T_A = +25°C ± 0.1°C	S	—	20	—	—	20	—	ppm/kHR

Note: 1. T_{low} = −40°C for LM285-1.2, LM285-2.5
= 0°C for LM385-1.2, LM385B-1.2, LM385-2.5, LM385B-2.5
T_{high} = +85°C for LM285-1.2, LM285-2.5
= +70°C for LM385-1.2, LM385B-1.2, LM385-2.5, LM385B-2.5

TYPICAL PERFORMANCE CURVES FOR LM285-1.2/385-1.2/385B-1.2

FIGURE 1 — REVERSE CHARACTERISTICS

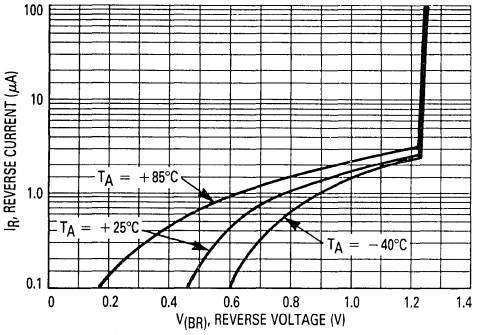


FIGURE 2 — REVERSE CHARACTERISTICS

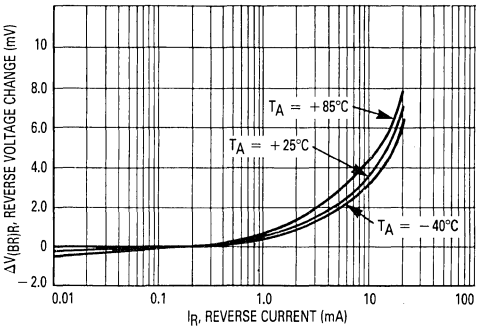


FIGURE 3 — FORWARD CHARACTERISTICS

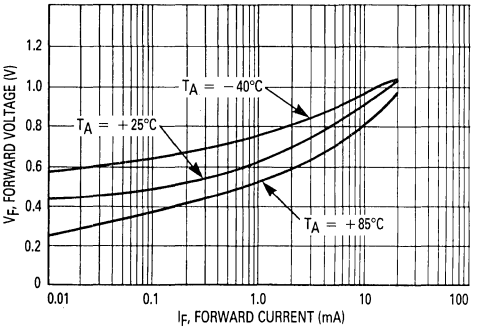


FIGURE 4 — TEMPERATURE DRIFT

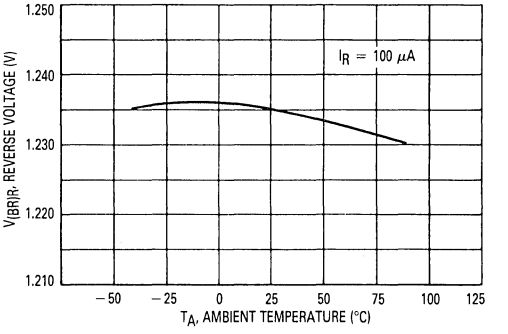


FIGURE 5 — NOISE VOLTAGE

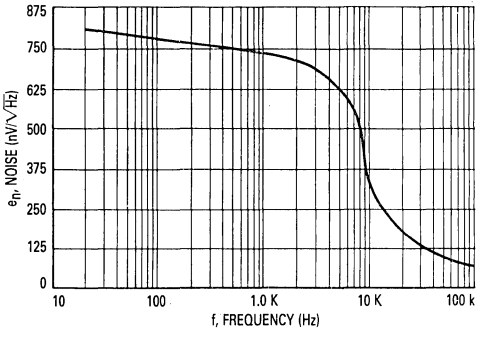
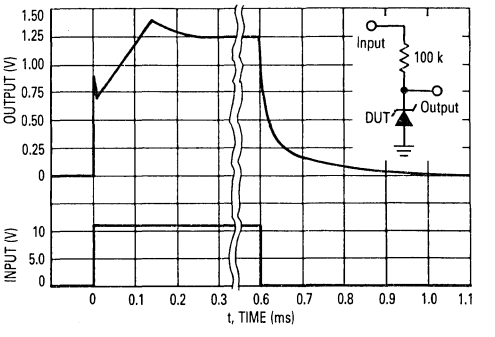


FIGURE 6 — RESPONSE TIME



TYPICAL PERFORMANCE CURVES FOR LM285-2.5/385-2.5/385B-2.5

FIGURE 7 — REVERSE CHARACTERISTICS

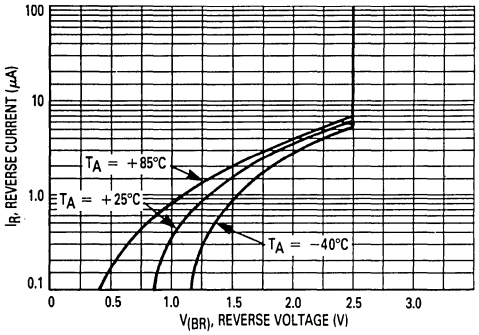


FIGURE 8 — REVERSE CHARACTERISTICS

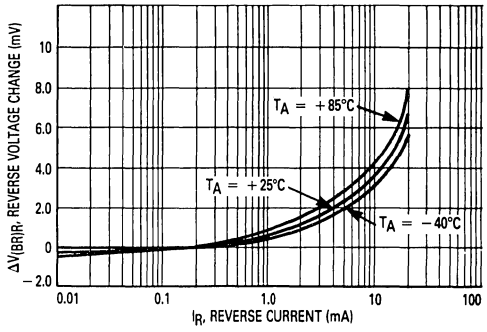


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FIGURE 9 — FORWARD CHARACTERISTICS

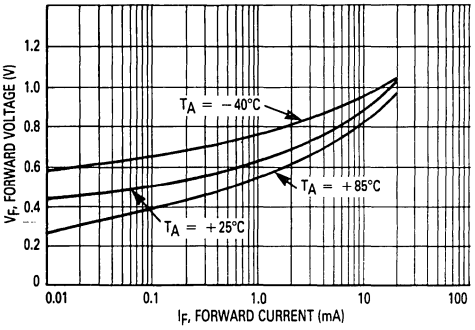


FIGURE 10 — TEMPERATURE DRIFT

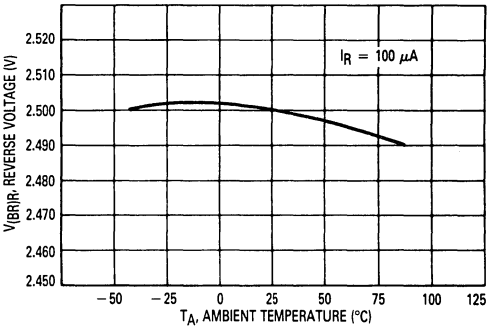


FIGURE 11 — NOISE VOLTAGE

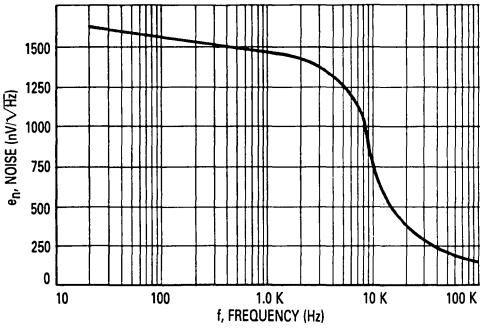
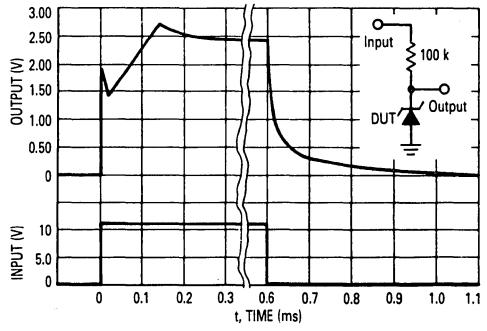


FIGURE 12 — RESPONSE TIME



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC1403,A
MC1503

LOW VOLTAGE REFERENCE

A precision band-gap voltage reference designed for critical instrumentation and D/A converter applications. This unit is designed to work with Motorola MC1508 and MC3510 D/A converters, and MC14433 A/D systems. Low temperature drift is a prime design consideration.

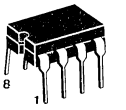
- Output Voltage: 2.5 V ±25 mV
- Input Voltage Range: 4.5 V to 40 V
- Quiescent Current: 1.2 mA Typ
- Output Current: 10 mA
- Temperature Coefficient: 10 ppm/°C Typ
- Guaranteed Temperature Drift Specification
- Equivalent to AD580
- Standard 8-Pin DIP, and 8-Pin SOIC Package

Typical Applications

- Voltage Reference for 8–12 Bit D/A Converters
- Low T_C Zener Replacement
- High Stability Current Reference
- Voltmeter System Reference

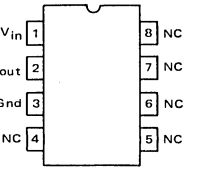
PRECISION LOW VOLTAGE REFERENCE

LASER TRIMMED INTEGRATED CIRCUIT



U SUFFIX
CERAMIC PACKAGE
CASE 693

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO-8)



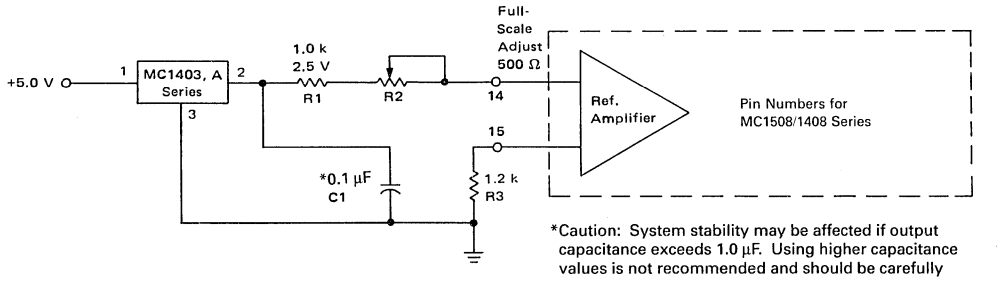
MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage	V_I	40	V
Storage Temperature	T_{stg}	−65 to 150	°C
Junction Temperature	T_J	+175	°C
Operating Ambient Temeprature Range MC1503 MC1403,A	T_A	 −55 to +125 0 to +70	 °C °C

ORDERING INFORMATION

Device	Temperature Range	Package
MC1503U	−55 to +125°C	Ceramic DIP
MC1403D	0 to +70°C	SO-8
MC1403U		Ceramic DIP
MC1403AU		Ceramic DIP
MC1403BD		SO-8

FIGURE 1 – A REFERENCE FOR MOTOROLA MONOLITHIC D/A CONVERTERS



*Caution: System stability may be affected if output capacitance exceeds 1.0 μF. Using higher capacitance values is not recommended and should be carefully considered.

PROVIDING THE REFERENCE CURRENT FOR MOTOROLA MONOLITHIC D/A CONVERTERS

The MC1403/1503 makes an ideal reference for the Motorola monolithic D/A converters. The MC1408/1508 converter requires a stable current reference of nominally 2.0 mA. This can be easily obtained from the MC1403/1503 with the addition of a series resistor, R1. A variable resistor, R2, is recommended to provide means for full-scale adjust on the D/A converter.

The resistor R3 improves temperature performance by matching the impedance on both inputs of the D/A reference amplifier. The capacitor decouples any noise present on the reference line. It is essential if the D/A converter is located any appreciable distance from the reference.

A single MC1403/1503 reference can provide the required current input for up to five of the monolithic D/A converters.

ELECTRICAL CHARACTERISTICS (V_{in} = 15 V, T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (I_O = 0 mA)	V_{OUT}	2.475	2.5	2.525	V
Temperature Coefficient of Output Voltage	$\Delta V_O/\Delta T$				ppm/°C
MC1503		—	—	55	
MC1403*		—	10	40	
MC1403A		—	10	25	
Output Voltage Change (over specified temperature range)	ΔV_O				mV
MC1503 −55°C to +125°C		—	—	25	
MC1403* 0°C to +70°C		—	—	7.0	
MC1403A		—	—	4.4	
Line Regulation (I_O = 0 mA)	Reg_{line}				mV
(15 V ≤ V_I ≤ 40 V)		—	1.2	4.5	
(4.5 V ≤ V_I ≤ 15 V)		—	0.6	3.0	
Load Regulation (0 mA < I_O < 10 mA)	Reg_{load}	—	—	10	mV
Quiescent Current (I_O = 0 mA)	I_Q	—	1.2	1.5	mA

*This test is not applicable to the MC1403D surface mount device.

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FIGURE 2 – MC1403/1503 SCHEMATIC

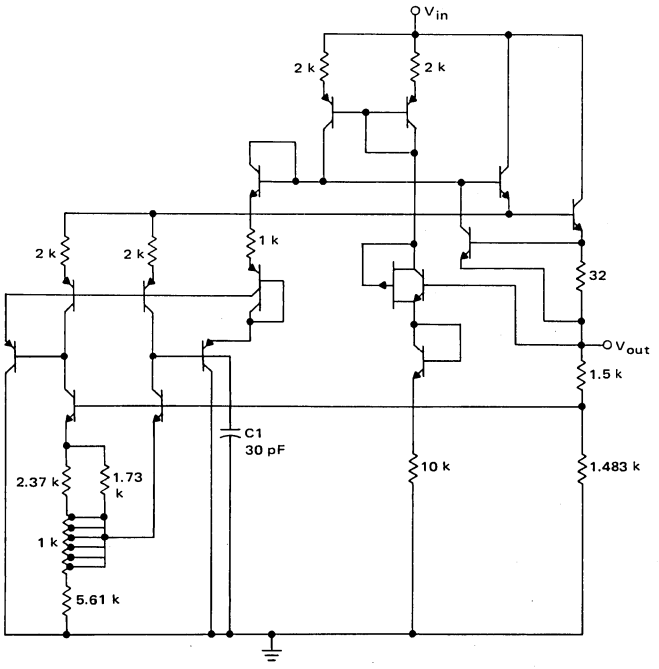


FIGURE 3 – TYPICAL CHANGE IN V_{out} versus V_{in}
(NORMALIZED TO V_{in} = 15 V @ T_C = 25°C)

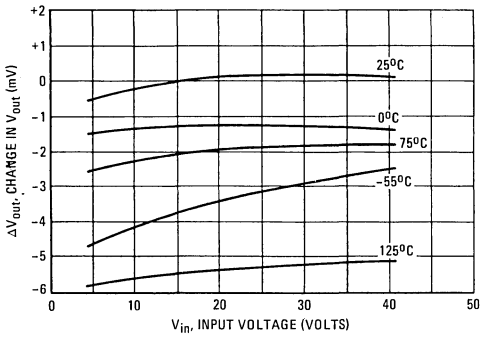


FIGURE 4 – CHANGE IN OUTPUT VOLTAGE
versus LOAD CURRENT
(NORMALIZED TO V_{out} @ V_{in} = 15 V, I_{out} = 0 mA)

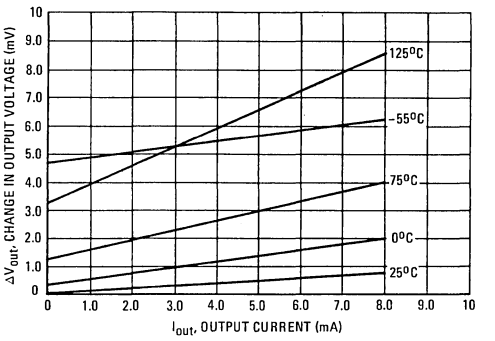


FIGURE 5 – QUIESCENT CURRENT versus TEMPERATURE
(V_{in} = 15 V, I_{out} = 0 mA)

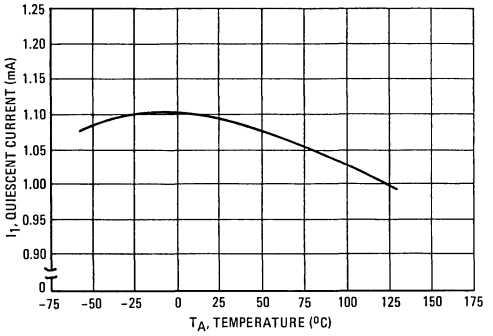


FIGURE 6 – CHANGE IN V_{out} versus TEMPERATURE
(NORMALIZED TO V_{out} @ V_{in} = 15 V)

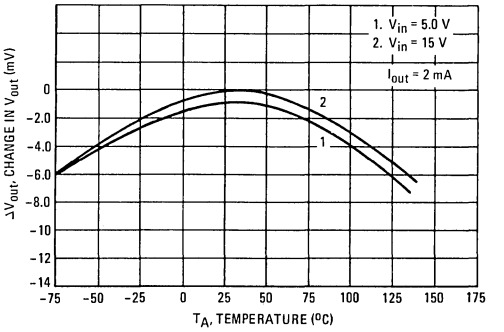
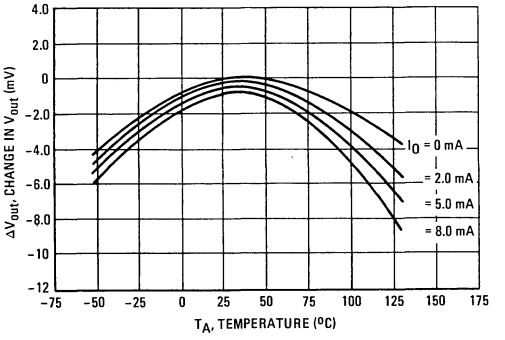


FIGURE 7 – CHANGE IN V_{out} versus TEMPERATURE
(NORMALIZED TO T_A = I_O, V_{in} = 15 V, I_{out} = 0 mA)



3-1/2-DIGIT VOLTMETER – COMMON ANODE DISPLAYS, FLASHING OVERRANGE

An example of a 3-1/2-digit voltmeter using the MC14433 is shown in the circuit diagram of Figure 8. The reference voltage for the system uses an MC1403 2.5 V reference IC. The full scale potentiometer can calibrate for a full scale of 199.9 mV or 1.999 V. When switching from 2 V to 200 mV operation, R_I is also changed, as shown on the diagram.

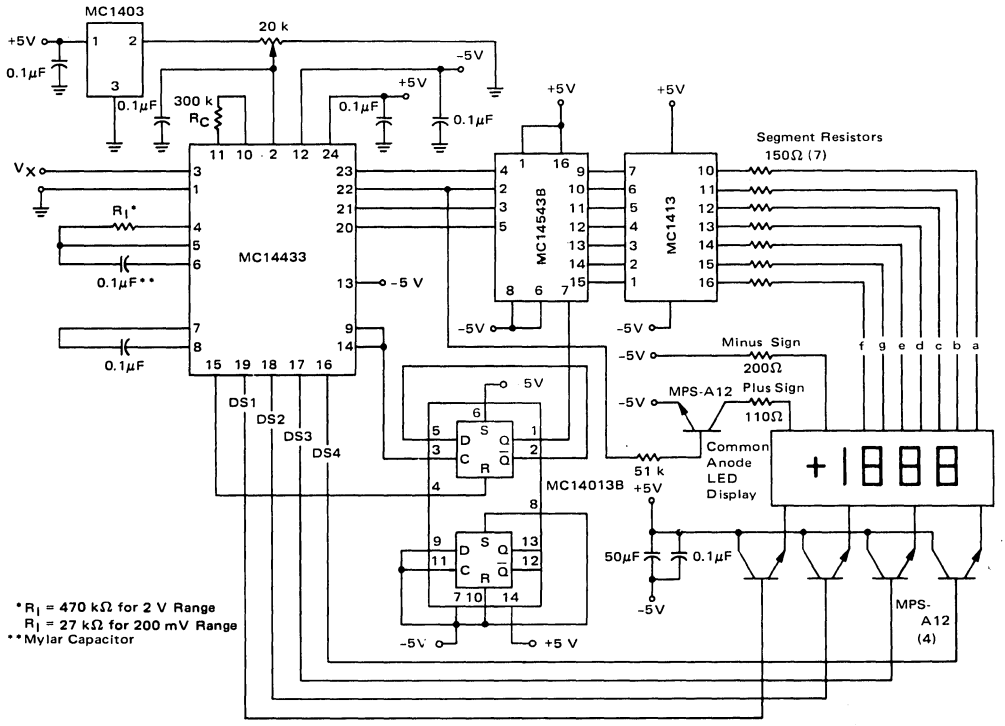
When using R_C equal to 300 kΩ, the clock frequency for the system is about 66 kHz. The resulting conversion time is approximately 250 ms.

When the input is overrange, the display flashes on and off. The flashing rate is one-half the conversion rate. This is done by dividing the EOC pulse rate by 2 with 1/2 MC14013B flip-flop and blanking the display using the blanking input of the MC14543B.

The display uses an LED display with common anode digit lines driven with an MC14543B decoder and an MC1413 LED driver. The MC1413 contains 7 Darlington transistor drivers and resistors to drive the segments of the display. The digit drive is provided by four MPS-A12 Darlington transistors operating in an emitter-follower configuration. The MC14543B, MC14013B and LED displays are referenced to V_{EE} via pin 13 of the MC14433. This places the full power supply voltage across the display. The current for the display may be adjusted by the value of the segment resistors shown as 150 ohms in Figure 8.

5

FIGURE 8 – 3-1/2-DIGIT VOLTMETER



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC1404
MC1404A
MC1504

PRECISION LOW DRIFT
VOLTAGE REFERENCES

5.0, 6.25, and 10-VOLT OUTPUT VOLTAGES

LASER TRIMMED SILICON
MONOLITHIC INTEGRATED CIRCUIT

5

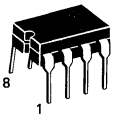
VOLTAGE REFERENCE FAMILY

The MC1404 series of ICs is a family of temperature-compensated voltage references for precision data conversion applications, such as A/D, D/A, V/F, and F/V. Advances in laser-trimming and ion-implanted devices, as well as monolithic fabrication techniques, make these devices stable and accurate to 12 bits over both military and commercial temperature ranges. In addition to excellent temperature stability, these parts offer excellent long-term stability and low noise.

- Output Voltages: Standard, 5.0 V, 6.25 V, 10 V
- Trimmable Output: > ±6%
- Wide Input Voltage Range: V_{ref} + 2.5 V to 40 V
- Low Quiescent Current: 1.25 mA Typical
- Temperature Coefficient: 10 ppm/°C Typical
- Low Output Noise: 12 μV p-p Typical
- Excellent Ripple Rejection: > 80 dB Typical

TYPICAL APPLICATIONS

- Voltage Reference for 8 – 12 Bit D/A Converters
- Low T_C Zener Replacement
- High Stability Current Reference
- MPU D/A and A/D Applications



U SUFFIX
CERAMIC PACKAGE
CASE 693

PIN ASSIGNMENTS

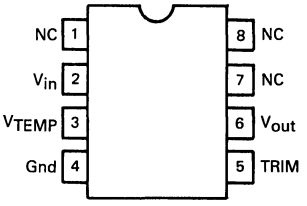
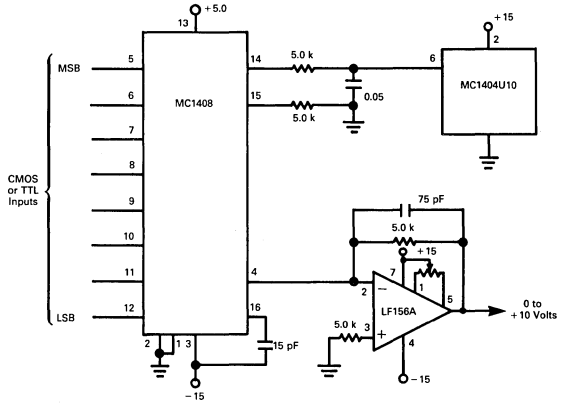


FIGURE 1 — VOLTAGE OUTPUT 8-BIT DAC USING MC1404U10



ORDERING INFORMATION

PACKAGE Ceramic DIP	
Device	**Temperature Range**
5.0 Volts	
MC1504U5	–55°C to +125°C
MC1404U5	0°C to +70°C
MC1404AU5	0°C to +70°C
6.25 Volts	
MC1504U6	–55°C to +125°C
MC1404U6	0°C to +70°C
MC1404AU6	0°C to +70°C
10 Volts	
MC1504U10	–55°C to +125°C
MC1404U10	0°C to +70°C
MC1404AU10	0°C to +70°C

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage	V_{in}	40	V
Storage Temperature	T_{stg}	−65 to +150	°C
Junction Temperature	T_J	+175	°C
Operating Ambient Temperature Range MC1504 MC1404,A	T_A	 −55 to +125 0 to +70	°C

ELECTRICAL CHARACTERISTICS (V_{in} = 15 Volts, T_A = 25°C and Trim Terminal not connected unless otherwise noted)

Characteristic	Symbol	MC1404,A			MC1504			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (I_O = 0 mA) MC1404U5, AU5/MC1504U5 MC1404U6, AU6/MC1504U6 MC1404U10, AU10/MC1504U10	V_O	 4.95 6.19 9.9	 5.0 6.25 10	 5.05 6.31 10.1	 4.95 6.19 9.9	 5.0 6.25 10	 5.05 6.31 10.1	Volt
Output Voltage Tolerance	—	—	±0.1	±1.0	—	±0.1	±1.0	%
Output Trim Range (Figure 10) (R_P = 100 kΩ)	ΔV_{TRIM}	±6.0	—	—	±6.0	—	—	%
Output Voltage Temperature Coefficient, Over Full Temperature Range MC1404, MC1504 MC1404A	$\Delta V_O/\Delta T$	 — —	 10 10	 40 25	 — —	 — —	 55 —	ppm/°C
Maximum Output Voltage Change Over Temperature Range MC1404U5, MC1504U5 MC1404AU5 MC1404U6, MC1504U6 MC1404AU6 MC1404U10, MC1504U10 MC1404AU10	ΔV_O	 — — — — — —	 — — — — — —	 14 9.0 17.5 11 28 18	 — — — — — —	 — — — — — —	 50 — 62 — 99 —	mV
Line Regulation (1) (V_{in} = V_{out} + 2.5 V to 40 V, I_{out} = 0 mA)	Reg_{line}	—	2.0	6.0	—	2.0	6.0	mV
Load Regulation (1) (0 ≤ I_O ≤ 10 mA)	Reg_{load}	—	—	10	—	—	10	mV
Quiescent Current (I_O = 0 mA)	I_Q	—	1.2	1.5	—	1.2	1.5	mA
Short Circuit Current	I_{sc}	—	20	45	—	—	45	mA
Long Term Stability	—	—	25	—	—	25	—	ppm/1000 hrs

Note 1: Includes thermal effects.

DYNAMIC CHARACTERISTICS (V_{in} = 15 V, T_A = 25°C all voltage ranges unless otherwise noted)

Characteristic	Symbol	MC1404,A			MC1504			Unit
		Min	Typ	Max	Min	Typ	Max	
Turn-On Settling Time (to ±0.01%)	t_S	—	50	—	—	50	—	μs
Output Noise Voltage — P to P (Bandwidth 0.1 to 10 Hz)	V_n	—	12	—	—	12	—	μV
Small-Signal Output Impedance 120 Hz 500 Hz	r_o	 — —	 0.15 0.2	 — —	 — —	 0.15 0.2	 — —	Ω
Power Supply Rejection Ratio	PSRR	70	80	—	70	80	—	dB

TYPICAL CHARACTERISTICS

FIGURE 2 – SIMPLIFIED DEVICE DIAGRAM

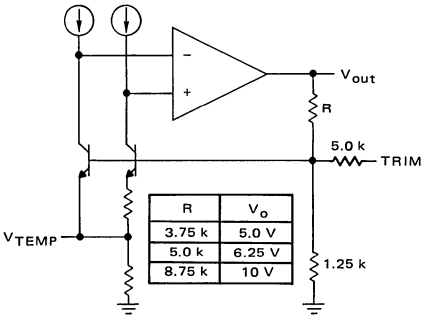


FIGURE 3 – LINE REGULATION versus TEMPERATURE

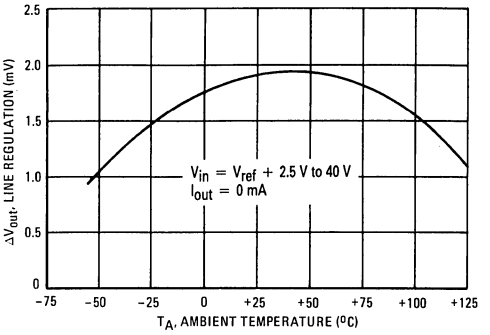


FIGURE 4 – OUTPUT VOLTAGE versus TEMPERATURE
MC1404U10

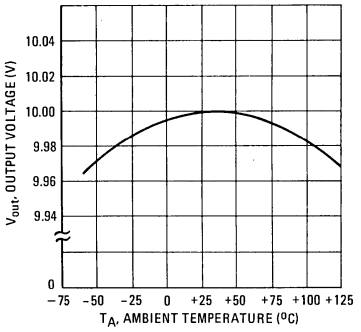


FIGURE 5 – LOAD REGULATION versus TEMPERATURE

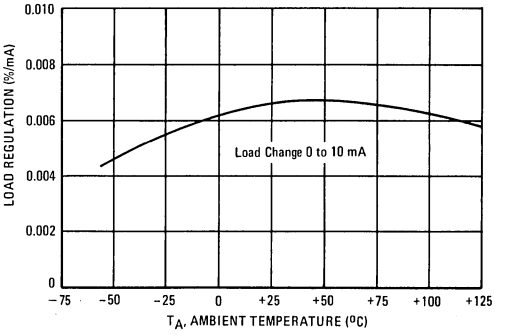


FIGURE 6 – POWER SUPPLY REJECTION RATIO
versus FREQUENCY

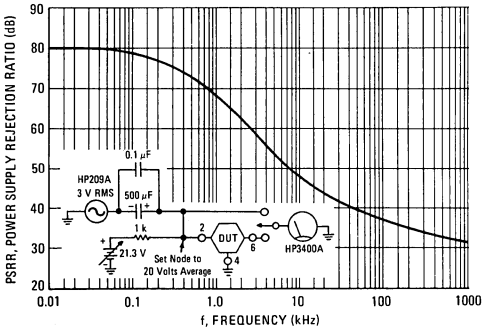


FIGURE 7 – QUIESCENT CURRENT versus TEMPERATURE

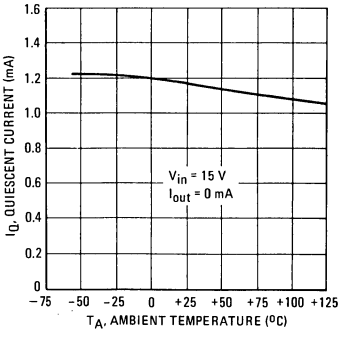


FIGURE 8 – SHORT CIRCUIT CURRENT versus TEMPERATURE

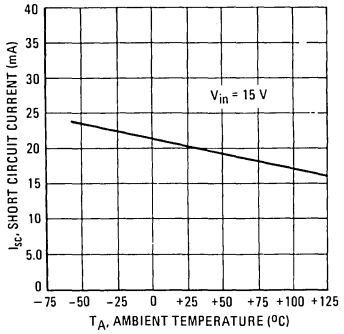


FIGURE 9 – V_{TEMP} OUTPUT versus TEMPERATURE

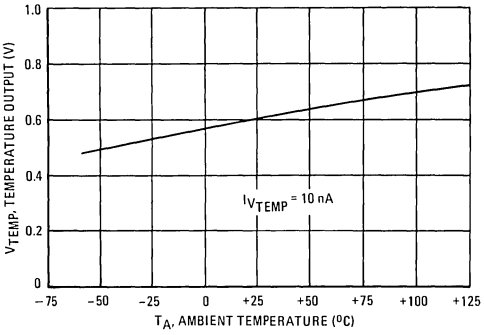
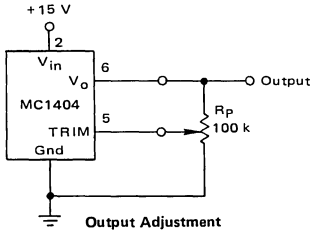


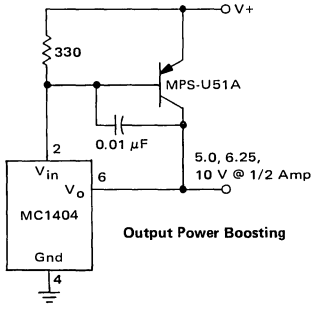
FIGURE 10 – OUTPUT TRIM CONFIGURATION



The MC1404 trim terminal can be used to adjust the output voltage over a ±6% range. For example, the output can be set to 10.000 V or to 10.240 V for binary applications. For trimming, Bourns type 3059, 100 kΩ or 200 kΩ trimpot is recommended.

Although Figure 10 illustrates a wide trim range, temperature coefficients may become unpredictable for trim > ±6.0%.

FIGURE 11 – PRECISION SUPPLY USING MC1404



The addition of a power transistor, a resistor, and a capacitor converts the MC1404 into a precision supply with one ampere current capability. At V+ = 15 V, the MC1404 can carry in excess of 14 mA of load current with good regulation. If the power transistor current gain exceeds 75, a one ampere supply can be realized.

FIGURE 12 – ULTRA STABLE REFERENCE FOR MC1723 VOLTAGE REGULATOR

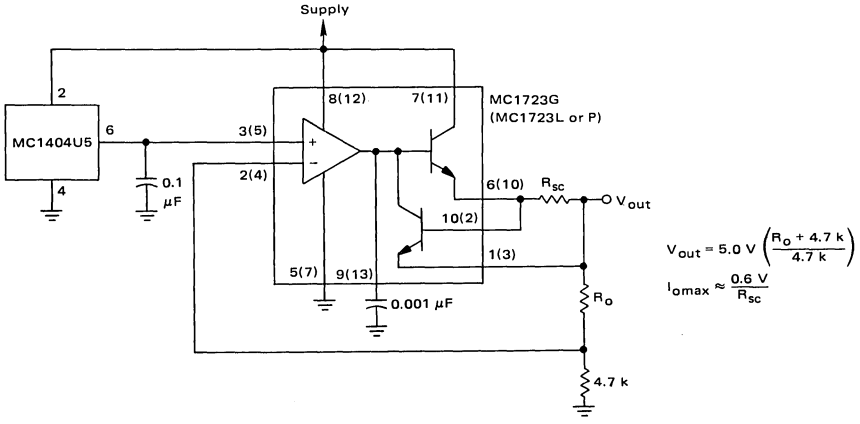


FIGURE 13 – 5.0 V, 6.0 AMP, 25 kHz SWITCHING REGULATOR WITH SEPARATE ULTRA-STABLE REFERENCE

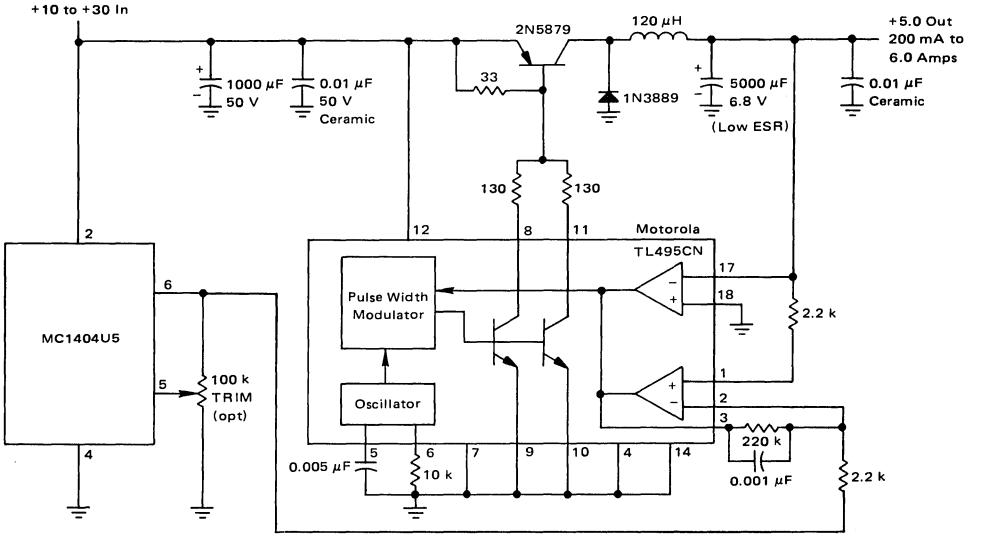
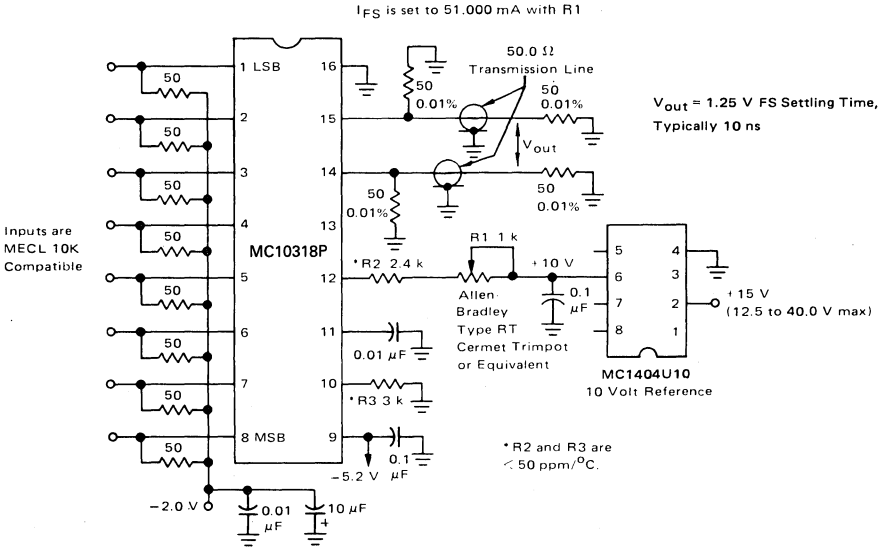


FIGURE 14 – HIGH SPEED 8-BIT D/A CONVERTER USING MC1404U10



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

TL431, A, B Series

PROGRAMMABLE PRECISION REFERENCES

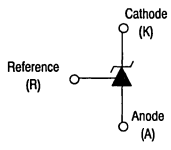
SILICON MONOLITHIC INTEGRATED CIRCUIT

Programmable Precision References

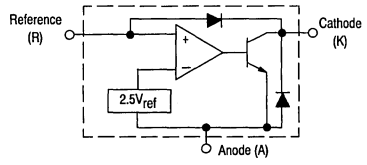
The TL431, A, B integrated circuits are three-terminal programmable shunt regulator diodes. These monolithic IC voltage references operate as a low temperature coefficient zener which is programmable from V_{ref} to 36 V with two external resistors. These devices exhibit a wide operating current range of 1.0 mA to 100 mA with a typical dynamic impedance of 0.22 Ω. The characteristics of these references make them excellent replacements for zener diodes in many applications such as digital voltmeters, power supplies, and op amp circuitry. The 2.5 V reference makes it convenient to obtain a stable reference from 5.0 V logic supplies, and since the TL431, A, B operates as a shunt regulator, it can be used as either a positive or negative voltage reference.

- Programmable Output Voltage to 36 V
- Voltage Reference Tolerance: ± 0.4%, Typ @ 25°C (TL431B)
- Low Dynamic Output Impedance, 0.22 Ω Typical
- Sink Current Capability of 1.0 mA to 100 mA
- Equivalent Full-Range Temperature Coefficient of 50 ppm/°C Typical
- Temperature Compensated for Operation over Full Rated Operating Temperature Range
- Low Output Noise Voltage

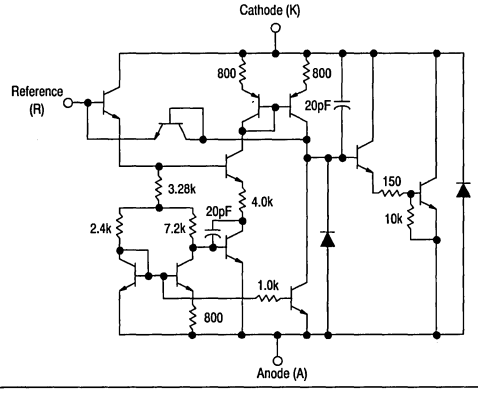
SYMBOL



FUNCTIONAL BLOCK DIAGRAM

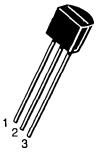


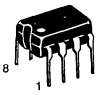
INTERNAL SCHEMATIC
Component values are nominal



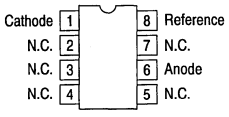
LP SUFFIX
CASE 29
(TO-92)

Pin 1. Reference
2. Anode
3. Cathode



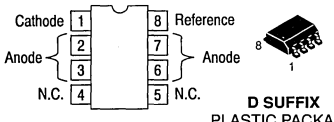


P SUFFIX
PLASTIC PACKAGE
CASE 626



(Top View)

JG SUFFIX
CERAMIC PACKAGE
CASE 693



(Top View)

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SOP-8)

ORDERING INFORMATION

Device	Temperature Range	Package
TL431CLP, ACLP, BCLP	0° to + 70°C	TO-92
TL431CP, ACP, BCP		Plastic
TL431CD, ACD, BCD		SOP-8
TL431CJG		Ceramic
TL431ILP, AILP, BILP	–40° to + 85°C	TO-92
TL431IP, AIP, BIP		Plastic
TL431ID, AID, BID		SOP-8
TL431IJG		Ceramic
TL431MJG	–55° to + 125°C	Ceramic

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MAXIMUM RATINGS (Full operating ambient temperature range applies, unless otherwise noted.)

Rating	Symbol	Value	Unit
Cathode to Anode Voltage	V_{KA}	37	V
Cathode Current Range, Continuous	I_K	–100 to +150	mA
Reference Input Curent Range, Continuous	I_{ref}	–0.05 to +10	mA
Operating Junction Temperature	T_J	150	°C
Operating Ambient Temperature Range TL431M TL431I, TL431AI, TL431BI TL431C, TL431AC, TL431BC	T_A	 –55 to +125 –40 to +85 0 to +70	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C Ambient Temperature D, LP Suffix Plastic Package P Suffix Plastic Package JG Suffix Ceramic Package	P_D	 0.70 1.10 1.25	W
Total Power Dissipation @ T_C = 25°C Derate above 25°C Case Temperature D, LP Suffix Plastic Package P Suffix Plastic Package JG Suffix Ceramic Package	P_D	 1.5 3.0 3.3	W

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RECOMMENDED OPERATING CONDITIONS

Condition/Value	Symbol	Min	Max	Unit
Cathode to Anode Voltage	V_{KA}	V_{ref}	36	V
Cathode Current	I_K	1.0	100	mA

THERMAL CHARACTERISTICS

Characteristics	Symbol	D, LP Suffix Package	P Suffix Package	JG Suffix Package	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	178	114	100	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	83	41	38	°C/W

ELECTRICAL CHARACTERISTICS (Ambient temperature at 25°C, unless otherwise noted.)

Characteristics	Symbol	TL431M			TL431I			TL431C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Reference Input Voltage (Figure 1) $V_{KA} = V_{ref}$, I_K = 10 mA T_A = +25°C $T_A = T_{low}$ to T_{high} (Note 1)	V_{ref}	 2.44 2.396	 2.495 —	 2.55 2.594	 2.44 2.41	 2.495 —	 2.55 2.58	 2.44 2.423	 2.495 —	 2.55 2.567	V
Reference Input Voltage Deviation Over Temperature Range (Figure 1, Notes 1, 2, 4) $V_{KA} = V_{ref}$, I_K = 10 mA	ΔV_{ref}	—	15	44	—	7.0	30	—	3.0	17	mV
Ratio of Change in Reference Input Voltage to Change in Cathode to Anode Voltage I_K = 10 mA (Figure 2), ΔV_{KA} = 10 V to V_{ref} ΔV_{KA} = 36 V to 10 V	$\frac{\Delta V_{ref}}{\Delta V_{KA}}$	 — —	 –1.4 –1.0	 –2.7 –2.0	 — —	 –1.4 –1.0	 –2.7 –2.0	 — —	 –1.4 –1.0	 –2.7 –2.0	mV/V
Reference Input Current (Figure 2) I_K =10 mA, R1 = 10 k, R2 = ∞ T_A = +25°C $T_A = T_{low}$ to T_{high} (Note 1)	I_{ref}	 — —	 1.8 —	 4.0 7.0	 — —	 1.8 —	 4.0 6.5	 — —	 1.8 —	 4.0 5.2	µA
Reference Input Current Deviation Over Temperature Range (Figure 2, Note 1, 4) I_K = 10 mA, R1 = 10 k, R2 = ∞	ΔI_{ref}	—	1.0	3.0	—	0.8	2.5	—	0.4	1.2	µA
Minimum Cathode Current For Regulation $V_{KA} = V_{ref}$ (Figure 1)	I_{min}	—	0.5	1.0	—	0.5	1.0	—	0.5	1.0	mA
Off-State Cathode Current (Figure 3) V_{KA} = 36 V, V_{ref} = 0 V	I_{off}	—	2.6	1000	—	2.6	1000	—	2.6	1000	nA
Dynamic Impedance (Figure 1, Note 3) $V_{KA} = V_{ref}$, ΔI_K = 1.0 mA to 100 mA f ≤ 1.0 kHz	$\lvert Z_{ka} \rvert$	—	0.22	0.5	—	0.22	0.5	—	0.22	0.5	Ω

ELECTRICAL CHARACTERISTICS (Ambient temperature at 25°C, unless otherwise noted.)

Characteristics	Symbol	TL431AI			TL431AC			TL431B			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Reference Input Voltage (Figure 1) $V_{KA} = V_{ref}$, I_K = 10 mA T_A = +25°C $T_A = T_{low}$ to T_{high}	V_{ref}	 2.47 2.44	 2.495 —	 2.52 2.55	 2.47 2.453	 2.495 —	 2.52 2.537	 — 2.475	 — 2.495	 — 2.515	V
Reference Input Voltage Deviation Over Temperature Range (Figure 1, Notes 1, 2, 4) $V_{KA} = V_{ref}$, I_K = 10 mA	ΔV_{ref}	—	7.0	30	—	3.0	17	—	3	17	mV
Ratio of Change in Reference Input Voltage to Change in Cathode to Anode Voltage I_K = 10 mA (Figure 2), ΔV_{KA} = 10 V to V_{ref} ΔV_{KA} = 36 V to 10 V	$\frac{\Delta V_{ref}}{\Delta V_{KA}}$	 — —	 –1.4 –1.0	 –2.7 –2.0	 — —	 –1.4 –1.0	 –2.7 –2.0	 — —	 –1.4 –1.0	 –2.7 –2.0	mV/V
Reference Input Current (Figure 2) I_K =10 mA, R1 = 10 k, R2 = ∞ T_A = +25°C $T_A = T_{low}$ to T_{high} (Note 1)	I_{ref}	 — —	 1.8 —	 4.0 6.5	 — —	 1.8 —	 4.0 5.2	 — —	 1.6 —	 3.0 4.0	µA
Reference Input Current Deviation Over Temperature Range (Figure 2, Note 1) I_K = 10 mA, R1 = 10 k, R2 = ∞	ΔI_{ref}	—	0.8	2.5	—	0.4	1.2	—	0.4	1.2	µA
Minimum Cathode Current For Regulation $V_{KA} = V_{ref}$ (Figure 1)	I_{min}	—	0.5	1.0	—	0.5	1.0	—	0.5	1.0	mA
Off-State Cathode Current (Figure 3) V_{KA} = 36 V, V_{ref} = 0 V	I_{off}	—	2.6	1000	—	2.6	1000	—	0.23	0.5	nA
Dynamic Impedance (Figure 1, Note 3) $V_{KA} = V_{ref}$, ΔI_K = 1.0 mA to 100 mA f ≤ 1.0 kHz	$\lvert Z_{ka} \rvert$	—	0.22	0.5	—	0.22	0.5	—	0.14	0.3	Ω

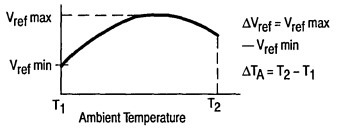
Note 1:

T_{low} = –55°C for TL431MG
= –40°C for TL431AIP TL431AILP, TL431IP, TL431ILP, TL431IJG
= 0°C for TL431ACP, TL431ACLP, TL431CP, TL431CLP, TL431CJG, TL431CD, TL431ACD

T_{high} = +125°C for TL431MJG
= +85°C for TL431AIP, TL431AILP, TL431IP, TL431ILP, TL431IJG
= +70°C for TL431ACP, TL431ACLP, TL431CP, TL431CLP, TL431CJG, TL431CD, TL431ACD

Note 2:

The deviation parameter ΔV_{ref} is defined as the difference between the maximum and minimum values obtained over the full operating ambient temperature range that applies.



The average temperature coefficient of the reference input voltage, αV_{ref}, is defined as:

$$\alpha V_{ref} \frac{ppm}{°C} = \frac{\left(\frac{\Delta V_{ref}}{V_{ref} @ 25°C}\right) \times 10^6}{\Delta T_A} = \frac{\Delta V_{ref} \times 10^6}{\Delta T_A (V_{ref} @ 25°C)}$$

αV_{ref} can be positive or negative depending on whether V_{ref} Min or V_{ref} Max occurs at the lower ambient temeperature. (Refer to Figure 6.)

Example: ΔV_{ref} = 8.0 mV and slope is positive,
V_{ref} @ 25°C =2.495 V, ΔT_A = 70°C

$$\alpha V_{ref} = \frac{0.008 \times 10^6}{70\ (2.495)} = 45.8\ ppm/°C$$

Note 3:

The dynamic impedance Z_{ka} is defined as $\lvert Z_{ka} \rvert = \frac{\Delta V_{KA}}{\Delta I_K}$

When the device is programmed with two external resistors, R1 and R2, (refer to Figure 2) the total dynamic impedance of the circuit is defined as:

$$\lvert Z_{ka}' \rvert \approx \lvert Z_{ka} \rvert \left(1 + \frac{R1}{R2}\right)$$

Figure 1. Test Circuit for $V_{KA} = V_{ref}$

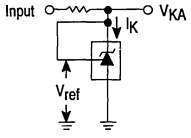
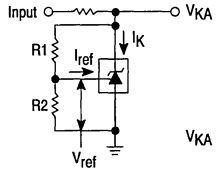


Figure 2. Test Circuit for $V_{KA} > V_{ref}$



$$V_{KA} = V_{ref}\left(1 + \frac{R1}{R2}\right) + I_{ref} \bullet R1$$

Figure 3. Test Circuit for I_{off}

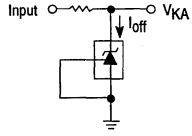


Figure 4. Cathode Current versus Cathode Voltage

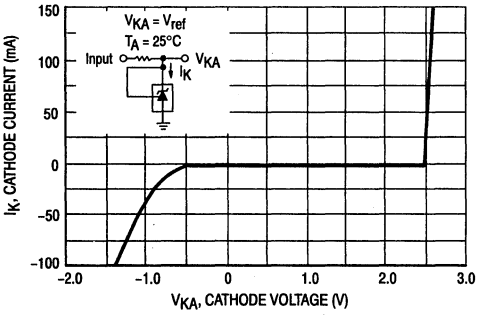


Figure 5. Cathode Current versus Cathode Voltage

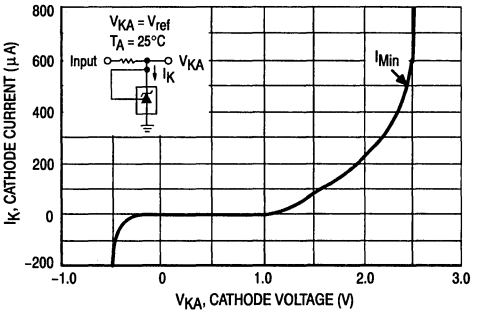


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Figure 6. Reference Input Voltage versus Ambient Temperature

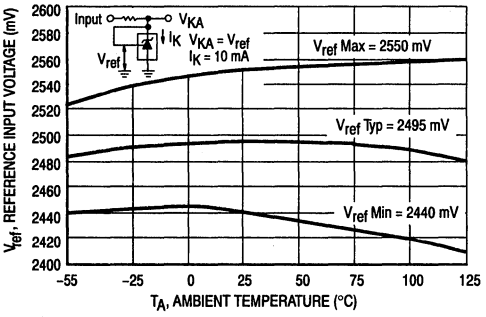

Figure 7. Reference Input Current versus Ambient Temperature

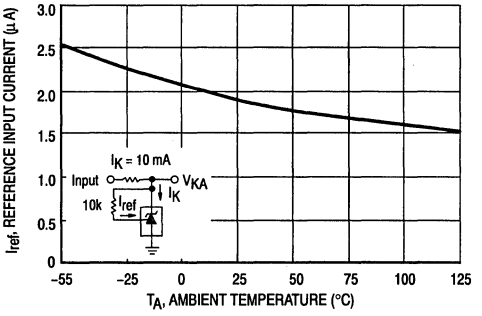

Figure 8. Change in Reference Input Voltage versus Cathode Voltage

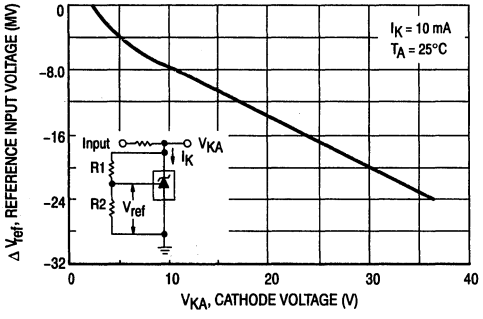

Figure 9. Off-State Cathode Current versus Ambient Temperature

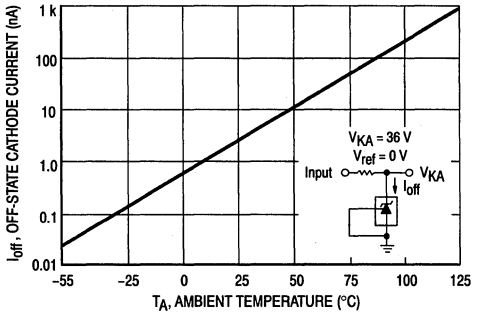

Figure 10. Dynamic Impedance versus Frequency

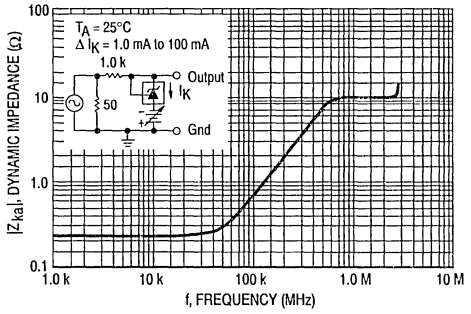

Figure 11. Dynamic Impedance versus Ambient Temperature

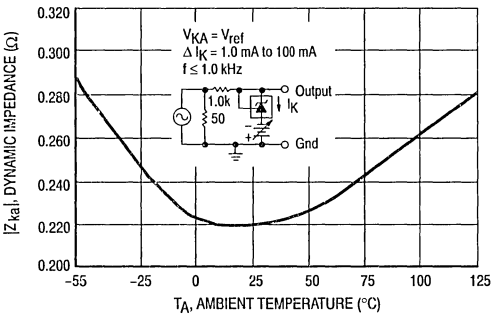

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Figure 12. Open-Loop Voltage Gain versus Frequency

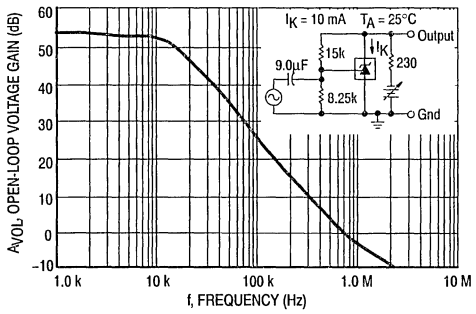


Figure 13. Spectral Noise Density

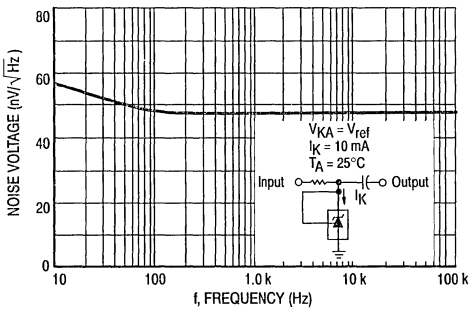


Figure 14. Pulse Response

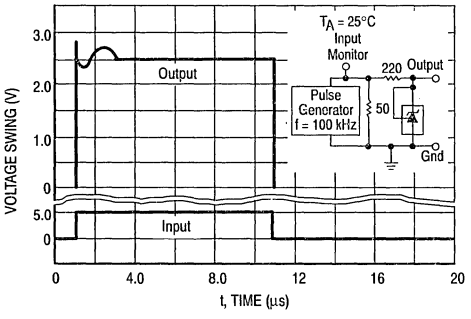


Figure 15. Stability Boundary Conditions

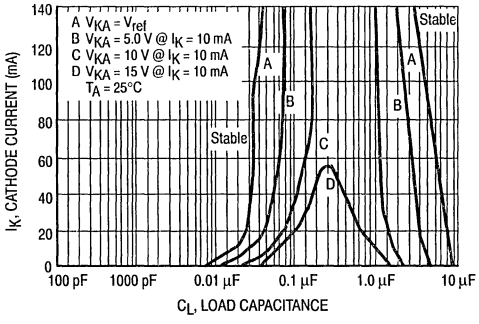


Figure 16. Test Circuit for Curve A of Stability Boundary Conditions

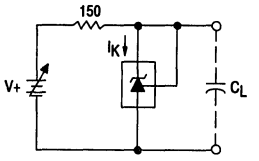
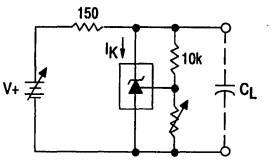


Figure 17. Test Circuit for Curves B, C, and D of Stability Boundary Conditions



TYPICAL APPLICATIONS

Figure 18. Shunt Regulator

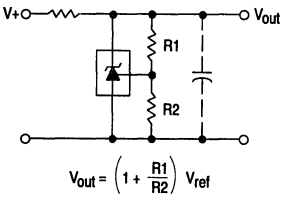


Figure 19. High Current Shunt Regulator

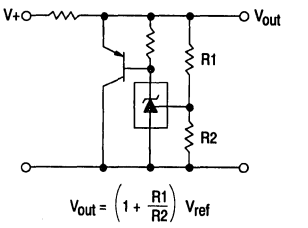


Figure 20. Output Control for a Three-Terminal Fixed Regulator

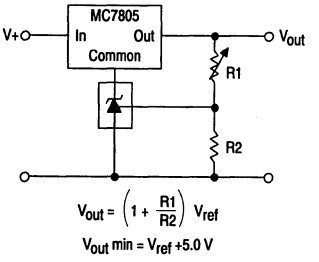


Figure 21. Series Pass Regulator

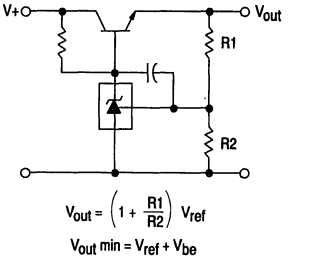


Figure 22. Constant Current Source

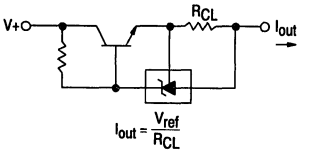


Figure 23. Constant Current Sink

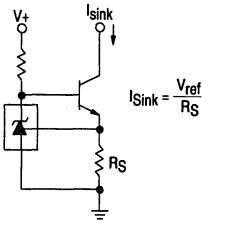


Figure 24. TRIAC Crowbar

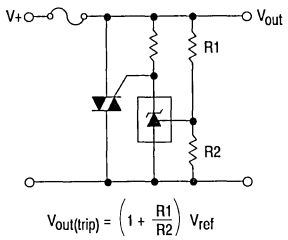


Figure 25. SCR Crowbar

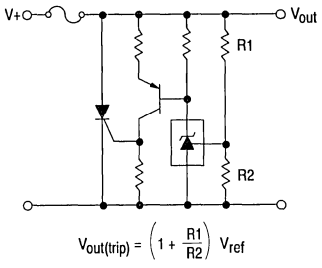
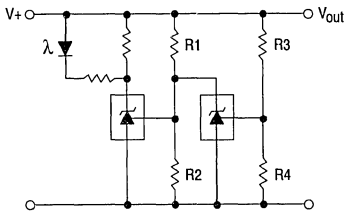


Figure 26. Voltage Monitor

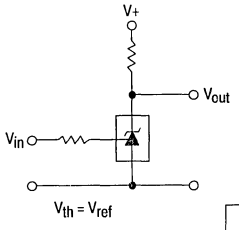


L.E.D. indicator is 'on' when V+ is between the upper and lower limits.

$$\text{Lower Limit} = \left(1 + \frac{R1}{R2}\right) V_{ref}$$

$$\text{Upper Limit} = \left(1 + \frac{R3}{R4}\right) V_{ref}$$

Figure 27. Single-Supply Comparator with Temperature-Compensated Threshold



V_{in}	V_{out}
< V_{ref}	V+
> V_{ref}	≈ 2.0V

Figure 28. Linear Ohmmeter

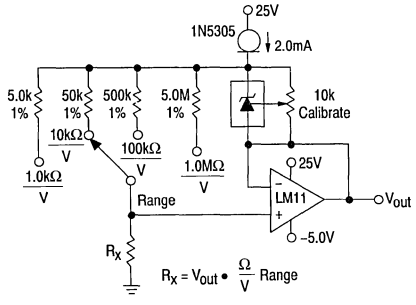


Figure 29. Simple 400 mW Phono Amplifier

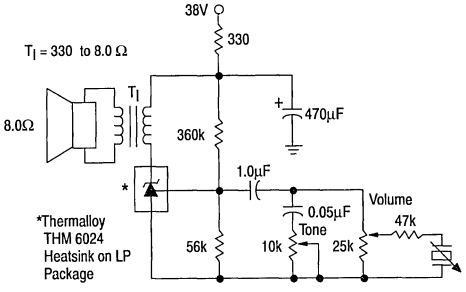
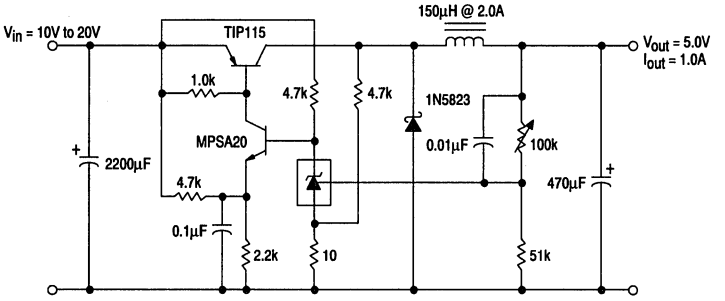


Figure 30. High Efficiency Step-Down Switching Converter



Test	Conditions	Results
Line Regulation	V_{in} = 10 V to 20 V, I_O = 1.0 A	53 mV (1.1%)
Load Regulation	V_{in} = 15 V, I_O = 0 A to 1.0 A	25 mV (0.5%)
Output Ripple	V_{in} = 10 V, I_O = 1.0 A	50 mV_{p-p} P.A.R.D.
Output Ripple	V_{in} = 20 V, I_O = 1.0 A	100 mV_{p-p} P.A.R.D.
Efficiency	V_{in} = 15 V, I_O = 1.0 A	82%

Data Conversion

In Brief . . .

Motorola's line of digital-to-analog and analog-to-digital converters includes several well established industry standards, and many are available in various linearity grades so as to suit most any application.

The A/D converters have 7 and 8-bit flash converters suitable for NTSC and PAL systems, CMOS has 8-bit to 10-bit converters, as well as other high speed digitizing applications.

The D/A converters have 6 and 8-bit devices, video speed (for NTSC and PAL) devices, and triple video DAC with on-board color palette for color graphics applications.

6

Data Conversion

The line of data conversion products which Motorola offers spans a wide spectrum of speed and resolution/accuracy. Features, including bus compatibility, minimize external parts count and provide easy interface to microprocessor systems. Various technologies, such as Bipolar and CMOS, are utilized to achieve functional capability, accuracy and production repeatability. Bipolar technology generally results in higher speed, while CMOS devices offer greatly reduced power consumption.

A-D Converters

Resolution (Bits)	Device	Nonlinearity Max	Conversion Time/Rate	Input Voltage Range	Supplies (V)	Temperature Range (°C)	Suffix/ Package	Comments
CMOS								
8	MC145040	± 1/2 LSB	10 µs	0 to V_{DD}	+5.0 ± 10%	– 40 to +85 (Suffix 2 devices)	P/738 FN/775	Requires external clock, 11-Ch MUX
	MC145041		20 µs			– 40 to +125 (Suffix 1 devices)	DW/751D	Includes internal clock, 11-Ch MUX
	MC14442					– 40 to +85	P/710 FN/776	µP compatible 11-Ch MUX S.A.R.
	MC14549B/ MC14559B	Successive Approximation Registers			+3.0 to +18	– 55 to +125 – 40 to +85	L/620 P/648	Compatible with MC1408 S.A.R. 8-bit D-A Converter
Triple 8-Bit	MC44250	1 LSB	15 MHz	1.6 to 4.6 V	+5.0 ± 10%	0 to +70	FN/777	3 separate video channels
10	MC145050	± 1 LSB	21 µs	0 to V_{DD}	+5.0 ± 10%	– 40 to +125	P/738 DW/751D	Requires external clock, 11-Ch MUX
	MC145051		44 µs					Includes internal clock, 11-Ch MUX
	MC145053						P/646 D/751A	Includes internal clock, 5-Ch MUX
8–10	MC14443/ MC14447	± 0.5% Full Scale	300 µs	Variable w/Supply	+5.0 to +18	– 40 to +85	P/648 DW/751G	µP compatible, single slope, 6-Ch MUX
3-1/2 Digit	MC14433	± 0.05% ± 1 Count	40 ms	± 2.0V ± 200 mV	+5.0 to +8.0 –2.8 to –8.0		P/709 DW/751E	Dual slope
Bipolar								
7	MC10321	± 1/2 LSB	40 ns	0 to 2.0 V_{pp} Max	+5.0 and –3.0 to –6.0	0 to +70	P/738 DW/751D	Video speed, Gray code, TTL outputs
8	MC10319	± 1 LSB					L/623 P/709 DW/751F Die Form	Video speed flash converter, internal Gray code, TTL Outputs

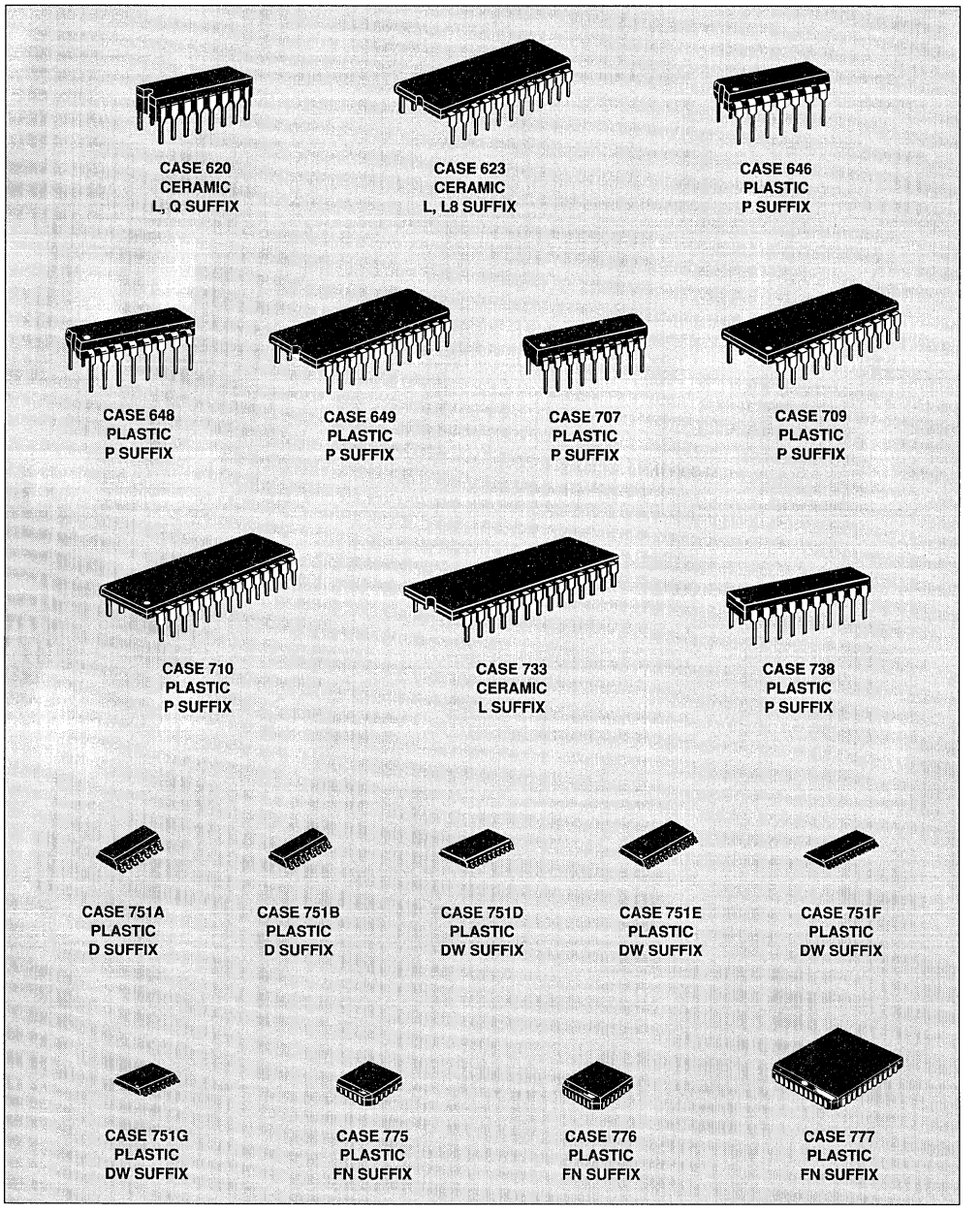
D-A Converters

Resolution (Bits)	Device	Accuracy @ 25°C Max	Max Settling Time (± 1/2 LSB)	Supplies (V)	Temperature Range (°C)	Suffix/ Package	Comments
CMOS							
6	MC144110	—	—	+5.0 to +15	0 to +85	P/707	Serial input, hex DAC, 6 outputs
						DW/751D	
	MC144111					P/646	Serial input, quad DAC, 4 outputs
						DW/751G	
Bipolar							
8	DAC-08	± 1 LSB	150 ns	±4.5 to ±18	0 to +70	EQ, HQ/620 CP, HP, EP/648 CD, ED/751B	High speed multiplying
		± 1/2 LSB					
		± 1/4 LSB	135 ns				
	MC1408	± 1/2 LSB	300 ns Typ	+5.0,	0 to +75	L8/620, P8/648	Multiplying
	MC1508			– 5.0 to –15	–55 to +125	L8/620	
4 x 3	MC10320	± 1/4 LSB	3.0 ns	+5.0 or ±5.0	0 to +70	L/733	125 MHz color graphics triple DAC
	MC10320-1						90 MHz Color
8	MC10322	± 1/2 LSB	5.0 ns	+5.0, –5.2	– 40 to +85	P/649	TTL 40 MHz minimum
	MC10324			–5.2			ECL 40 MHz minimum

A-D/D-A Converters

Resolution (Bits)	Device	Monotonicity (Bits)	Conversion Time	Input Voltage Range	Supplies (V)	Temperature Range (°C)	Suffix/ Package	Comments
CMOS — For Telecommunications								
13	MC145402	13	62.5 µs	± 3.28 V peak	± 5.0 to 6.0	–40 to +85	L/620	Digital signal processing (e.g., echo cancelling, high speed modems, phone systems with conferencing)

Data Conversion Package Overview



A-D Converters

D-A Converters

RELATED APPLICATION NOTES

App Note	Title	Related Device
EB-51	Successive Approximation BCD A-to-D Converter	**MC1408, MC1508**
AN702	High Speed Digital-to-Analog and Analog-to-Digital Techniques	**General Information**
AN926	Techniques for Improving the Steeling Time of a DAC and Op Amp Combination	**Various**

DAC-08

HIGH SPEED 8-BIT MULTIPLYING D-TO-A CONVERTER

SILICON MONOLITHIC INTEGRATED CIRCUIT

HIGH SPEED 8-BIT MULTIPLYING D-TO-A CONVERTER

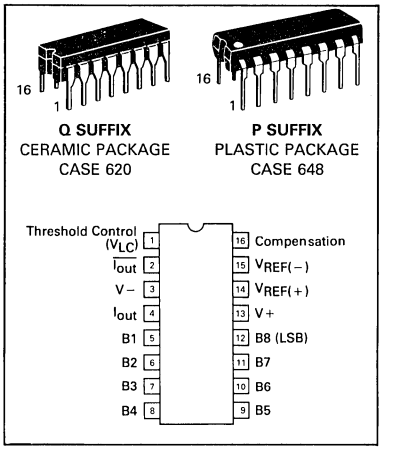
The DAC-08 series is a monolithic 8-bit high speed multiplying digital-to-analog converter, capable of settling to within 1/2 LSB (0.19%) in 85 ns. Monotonic multiplying performance is retained over a wide 40-to-1 reference current range. Full scale and reference currents are matched to within 1 LSB, therefore eliminating the need for full scale trim in most applications.

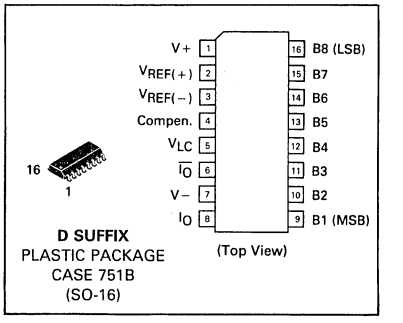
Dual complementry current outputs with high voltage compliance provide added versatility and allow differential mode of operation to effectively double the peak-to-peak output swing. In many applications, output current-to-voltage conversion can be accomplished without requiring an external op amp. Noise-immune inputs permit direct interface with TTL and DTL levels when the logic threshold control, V_{LC}, (Pin 1) is grounded. All other logic family thresholds are attainable by adjusting the voltage level of Pin 1. Performance characteristics are virtually unchanged over the entire ±4.5 V to ±18 V power supply range. Power consumption is typically 33 mW with ±5.0 V supplies.

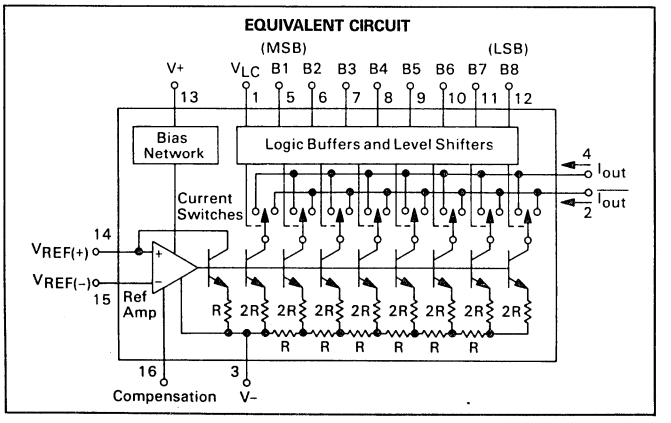
The DAC-08 is available in several versions, with nonlinearity as tight as ±0.1% (±1/4 LSB) over temperature. All versions are guaranteed monotonic over 8 bits. For an extra margin of performance, Motorola utilizes thin-film resistors permitting very accurate resistive values which are extremely stable over temperature.

High performance characteristics along with low cost, make the DAC-08 an excellent selection for applications such as CRT displays, waveform generation, high speed modems, and high speed analog-to-digital converters.

- Fast Settling Time — 85 ns
- Full Scale Current Prematched to ±1 LSB
- Nonlinearity Over Temperature to ±0.1% Max
- Differential Current Outputs
- High Voltage Compliance Outputs −10 V to +18 V
- Wide Range Multiplying Capability
- Inputs Compatable With TTL, DTL, CMOS, PMOS, ECL, HTL
- Low Full Scale Current Drift
- Wide Power Supply Range ±4.5 V to ±18 V
- Low Power Consumption
- Thin-Film Resistors
- Low Cost







ORDERING INFORMATION

Device	Nonlinearity	Temperature Range	Package
DAC-08HQ	±0.1%	0°C to +70°C	Ceramic
DAC-08EQ	±0.19%		Ceramic
DAC-08CD	±0.39%		SO-16
DAC-08ED	±0.19%		SO-16
DAC-08HP	±0.1%		Plastic
DAC-08EP	±0.19%		Plastic
DAC-08CP	±039%		Plastic

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
V+ Supply to V– Supply	V_S	36	V
Logic Inputs	—	V– to V– Plus 36	V
Logic Threshold Control	V_{LC}	V– to V+	V
Analog Current Outputs	I_{out}	See Figure 7	mA
Reference Input (V14, V15)	V_{ref}	V– to V+	V
Reference Input Differential Voltage (V14 to V15)	$V_{ref(D)}$	± 18	V
Reference Input CUrrent (I14)	I_{ref}	5.0	mA
Operating Temperature Range	T_A	0 to = 70	°C
Storage Temperate	T_{stg}	– 65 to + 150	°C
Power Dissipation Derate above 100°C	P_D $R_{\theta JA}$	500 10	mW mW/°C

ELECTRICAL CHARACTERISTICS (V_S = ±15 V, I_{ref} = 2.0 mA, T_A = 0°C to 70°C , unless otherwise noted)

Characteristic	Symbol	DAC-08H			DAC-08E			DAC-08C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Resolution	—	8	8	8	8	8	8	8	8	8	Bits
Monotonicity	—	8	8	8	8	8	8	8	8	8	Bits
Nonlinearity, T_A = 0°C to 70°C	NL	—	—	±0.1	—	—	±0.19	—	—	±0.39	%FS
Settling Time to ± 1/2 LSB (All Bits Switched On or Off T_A = 25°C) Figure 24 (Note 1)	t_s	—	85	—	—	85	—	—	85	—	ns
Propagation Delay, T_A = 25°C (Note 1) Each Bit All Bits Switched	 t_{PLH} t_{PHL}	 — —	 35 35	 — —	 — —	 35 35	 — —	 — —	 35 35	 — —	ns
Full Scale Tempco	TCI_{FS}	—	±10	—	—	±10	—	—	±10	—	ppm/°C
Output Voltage Compliance Full Scale Current Change < 1/2 LSB, R_{out} > 20 MΩ Typ.	V_{OC}	–10	—	+18	–10	—	+18	–10	—	+18	V
Full Range Current (V_{ref} = 10.000 V; R14, R15 = 5.000 kΩ T_A = 25°C	I_{FR4}	1.984	1.992	2.000	1.94	1.99	2.04	1.94	1.99	2.04	mA
Full Range Symmetry (I_{FR4} - I_{FR2})	I_{FRS}	—	±0.5	±4.0	—	±1.0	±8.0	—	±2.0	±16.0	µA
Zero Scale Current	I_{ZS}	—	0.1	1.0	—	0.2	2.0	—	0.2	4.0	µA
Output Current Range V– = – 5.0 V V– = – 8.0 V to –18 V	 I_{OR1} I_{OR2}	 0 0	 — —	 2.1 4.2	 0 0	 — —	 2.1 4.2	 0 0	 — —	 2.1 4.2	mA
Logic Input Levels (V_{LC} = 0 V) Logic "0" Logic "1"	 V_{IL} V_{IH}	 — 2.0	 — —	 0.8 —	 — 2.0	 — —	 0.8 —	 — 2.0	 — —	 0.8 —	V
Logic Input Levels (V_{LC} = 0 V) Logic "0" (V_{in} = –10 V to +0.8 V) Logic "1" (V_{in} = +2.0 V to +18 V)	 I_{IL} IH	 — —	 –2.0 0.002	 –10 10	 — —	 –2.0 0.002	 –10 10	 — —	 –2.0 0.002	 –10 10	µA
Logic Input Swing, V– = –15 V	V_{IS}	–10	—	+18	–10	—	+18	–10	—	+18	V
Logic Threshold Range, V_S = ± 15 V	V_{THR}	–10	—	+13.5	–10	—	+13.5	–10	—	+13.5	V
Reference Bias Current	I_{15}	—	–1.0	–3.0	—	–1.0	–3.0	—	–1.0	–3.0	µA
Reference Input Slew Rate Figure 19 (Note 1)	di/dt	—	8.0	—	—	8.0	—	—	8.0	—	mA/µs
Power Supply Sensitivity (I_{ref} = 1.0 mA V– = – 4.5 V to 18 V V– = – 4.5 V to –18 V	 $PSSI_{FS+}$ PSS_{FS-}	 — —	 ±0.0003 ±0.002	 ±0.01 ±0.01	 — —	 ±0.0003 ±0.002	 ±0.01 ±0.01	 — —	 ±0.0003 ±0.002	 ±0.01 ±0.01	%/%
Power Supply Current V_S = ±5.0 V, I_{ref} = 1.0 mA V_S = ±5.0 V, – 15 V, I_{ref} = 2.0 mA V_S = ± 15 V, I_{ref} = 2.0 mA	 I+ I– I+ I– I+ I–	 — — — — — —	 2.3 –4.3 2.4 –6.4 2.5 –6.5	 3.8 –5.8 3.8 –7.8 3.8 –7.8	 — — — — — —	 2.3 –4.3 2.4 –6.4 2.5 –6.5	 3.8 –25.8 3.8 –7.8 3.8 –7.8	 — — — — — —	 2.3 –4.3 2.4 –6.4 2.5 –6.5	 3.8 –5.8 3.8 –7.8 3.8 –7.8	mA
Power Dissipation V_S = ±5.0 V, I_{ref} = 1.0 mA V_S = ±5.0 V, – 15 V, I_{ref} = 2.0 mA V_S = ± 15 V, I_{ref} = 2.0 mA	P_D	 — — —	 33 108 135	 48 136 174	 — — —	 33 108 135	 48 136 174	 — — —	 33 108 135	 48 136 174	mA

Note 1. Parameter is not 100% tested; guaranteed by design.

TYPICAL PERFORMANCE CURVES

FIGURE 1 — FULL SCALE CURRENT versus REFERENCE CURRENT

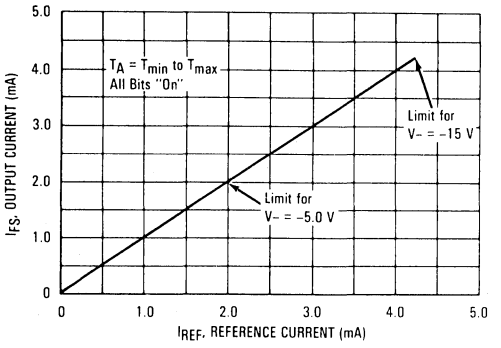
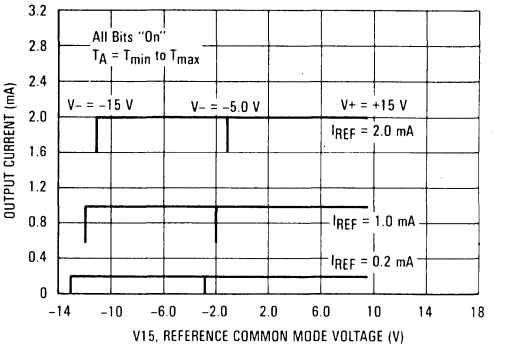


FIGURE 2 — REFERENCE AMP COMMON MODE RANGE



NOTE: Positive Common Mode Range is Always (V+) –1.5 V

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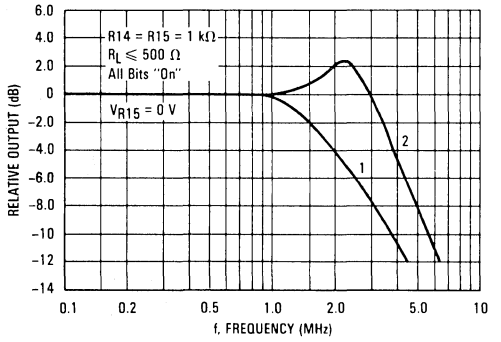
FIGURE 3 — REFERENCE INPUT FREQUENCY RESPONSE



Curve 1 — C_c = 15 pF, V_{in} = 2.0 V p-p Centered at +1.0 V (Large-Signal)
Curve 2 — C_c = 15 pF, V_{in} = 50 mV p-p Centered at +200 mV (Small-Signal)

FIGURE 4 — LSB PROPAGATION DELAY versus I_{FS}

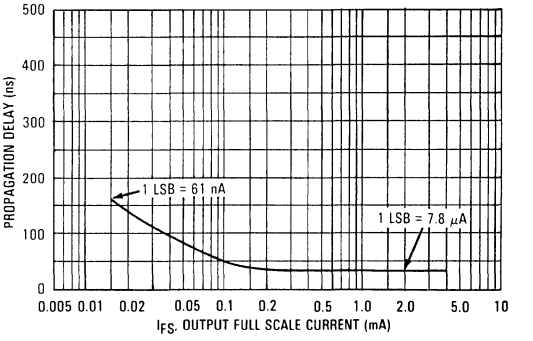


FIGURE 5 — LOGIC INPUT CURRENT versus INPUT VOLTAGE

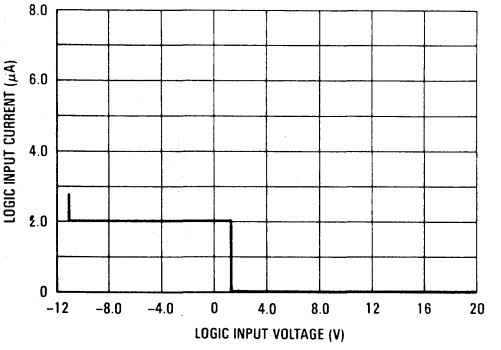
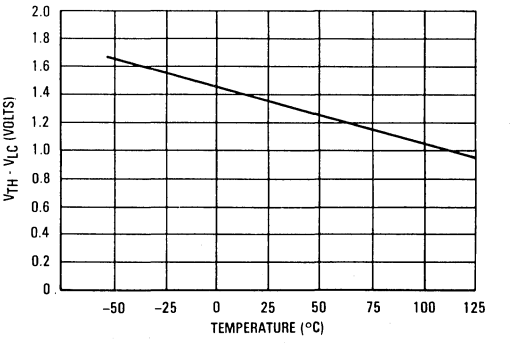


FIGURE 6 — V_{TH} - V_{LC} versus TEMPERATURE



TYPICAL PERFORMANCE CURVES

FIGURE 7 — OUTPUT CURRENT versus OUTPUT VOLTAGE (Output Voltage Compliance)

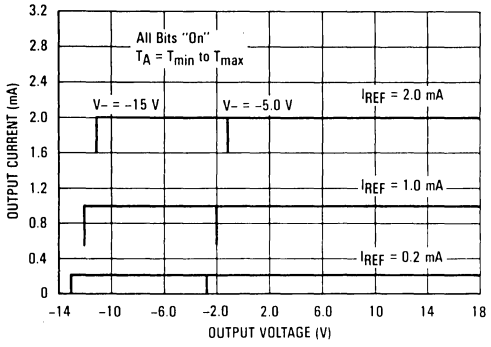


FIGURE 8 — OUTPUT VOLTAGE COMPLIANCE versus TEMPERATURE

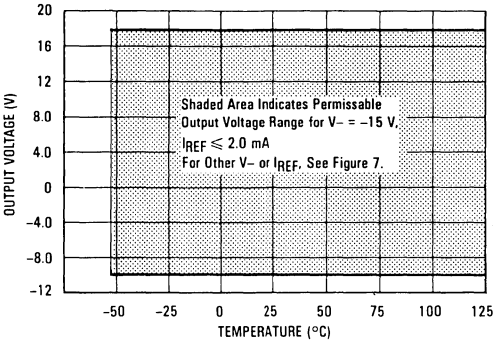
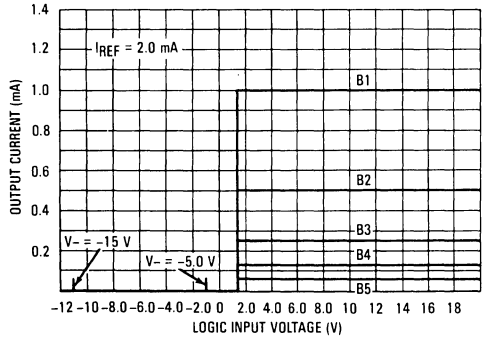


FIGURE 9 — BIT TRANSFER CHARACTERISTICS



NOTE: B1–B8 have identical transfer characteristics. Bits are fully switched with less than 1/2 LSB error, at less than ±100 mV from actual threshold. These switching points are guaranteed to lie between 0.8 V and 2.0 V over operating temperature range (V_{LC} = 0 V).

FIGURE 10 — POWER SUPPLY CURRENT versus V+

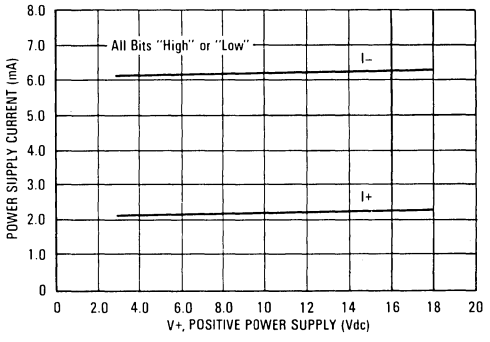


FIGURE 11 — POWER SUPPLY CURRENT versus V–

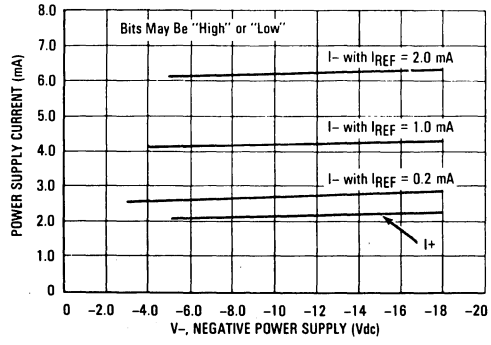
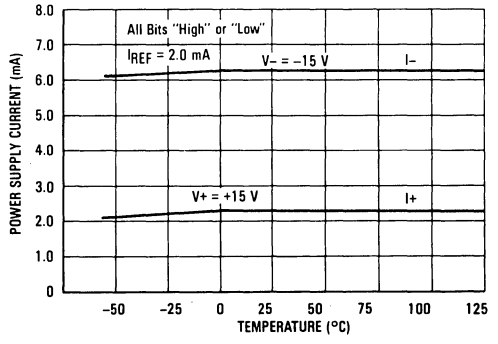


FIGURE 12 — POWER SUPPLY CURRENT versus TEMPERATURE



BASIC CIRCUIT CONFIGURATIONS

FIGURE 13 — RECOMMENDED FULL SCALE ADJUSTMENT CIRCUIT

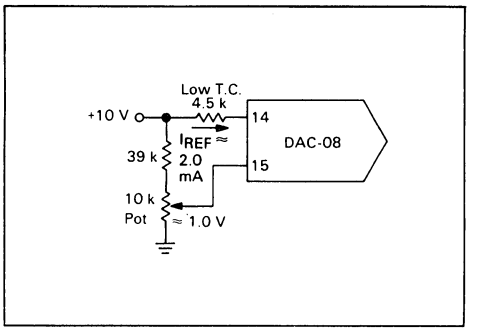
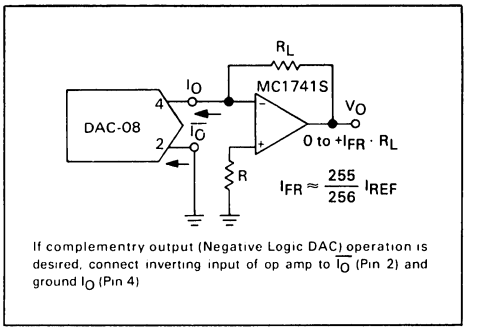


FIGURE 14 — POSITIVE LOW IMPEDANCE OUTPUT OPERATION



If complementry output (Negative Logic DAC) operation is desired, connect inverting input of op amp to $\overline{I_O}$ (Pin 2) and ground I_O (Pin 4)

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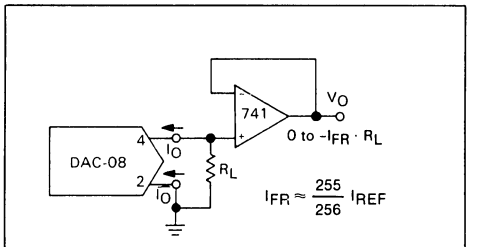
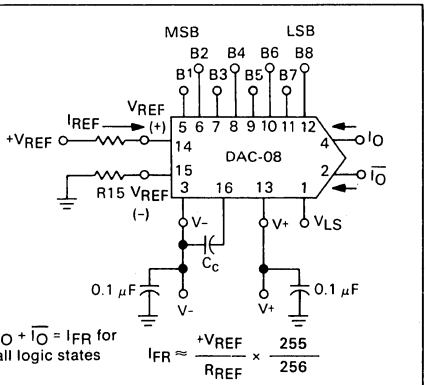
FIGURE 15 — NEGATIVE LOW IMPEDANCE OUTPUT OPERATION



If complementry output (Negative Logic DAC) is desired, connect noninverting input of op amp to $\overline{I_O}$ (Pin 2) and ground I_O (Pin 4)

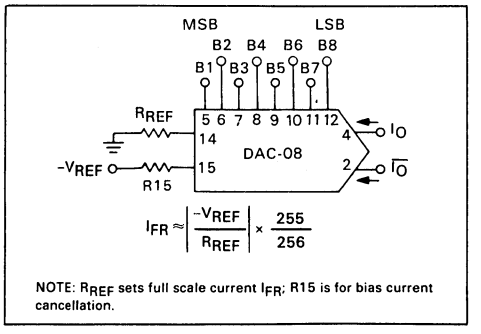
FIGURE 16 — BASIC POSITIVE REFERENCE OPERATION



For fixed reference, TTL operation, typical values are

V_{REF} = +10.000 V
R_{REF} = 5.000 k
R15 ≈ R_{REF}
C_c = 0.01μF
V_{LC} = 0 V (Ground)

FIGURE 17 — BASIC NEGATIVE REFERENCE OPERATION



NOTE: R_{REF} sets full scale current I_{FR}; R15 is for bias current cancellation.

BASIC CIRCUIT CONFIGURATIONS

FIGURE 18 — ACCOMMODATING BIPOLAR REFERENCES

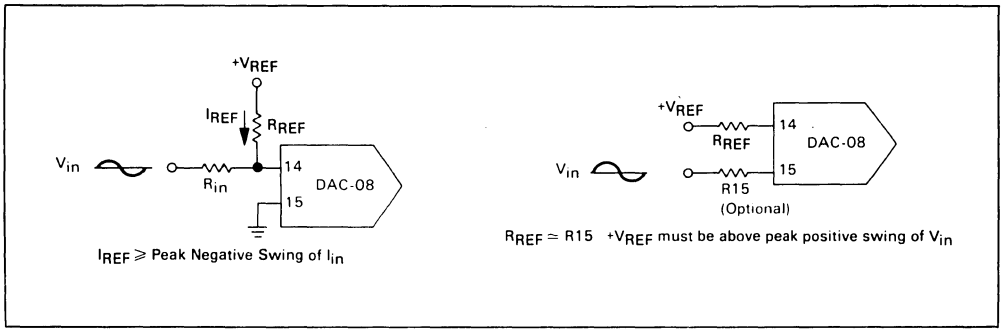


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FIGURE 19 — PULSED REFERENCE OPERATION

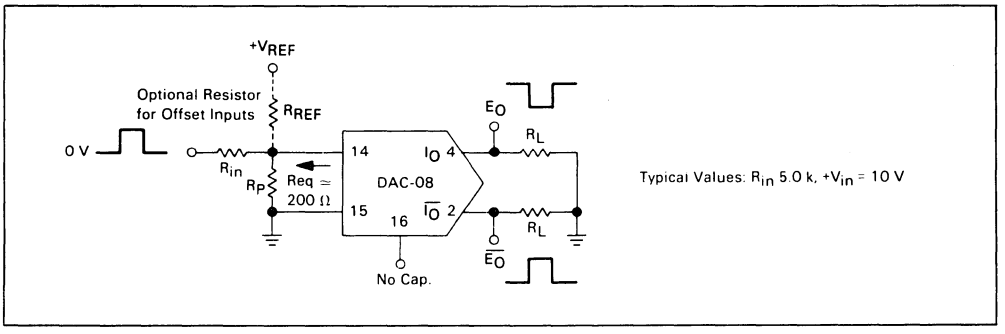
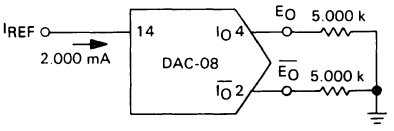


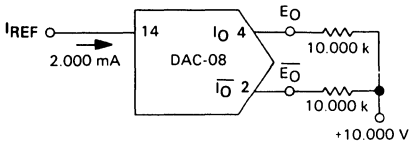
FIGURE 20 — BASIC UNIPOLAR NEGATIVE OPERATION



	B1	B2	B3	B4	B5	B6	B7	B8	I_O mA	$\overline{I_O}$ mA	E_O	$\overline{E_O}$
Full Range	1	1	1	1	1	1	1	1	1.992	0.000	−9.960	−0.000
Half Scale +LSB	1	0	0	0	0	0	0	1	1.008	0.984	−5.040	−4.920
Half Scale	1	0	0	0	0	0	0	0	1.000	0.992	−5.000	−4.960
Half Scale −LSB	0	1	1	1	1	1	1	1	0.992	1.000	−4.960	−5.000
Zero Scale +LSB	0	0	0	0	0	0	0	1	0.008	1.984	−0.040	−9.920
Zero Scale	0	0	0	0	0	0	0	0	0.000	1.992	0.000	−9.960

BASIC CIRCUIT CONFIGURATIONS

FIGURE 21 – BASIC BIPOLAR OUTPUT OPERATION



	B1	B2	B3	B4	B5	B6	B7	B8	E_O	$\overline{E_O}$
Pos Full Range	1	1	1	1	1	1	1	1	-9.920	+10.000
Pos Full Range -LSB	1	1	1	1	1	1	1	0	-9.840	+9.920
Zero Scale +LSB	1	0	0	0	0	0	0	1	-0.080	+0.160
Zero Scale	1	0	0	0	0	0	0	0	0.000	+0.080
Zero Scale -LSB	0	1	1	1	1	1	1	1	+0.080	0.000
Neg Full Scale +LSB	0	0	0	0	0	0	0	1	+9.920	-9.840
Neg Full Scale	0	0	0	0	0	0	0	0	+10.000	-9.920

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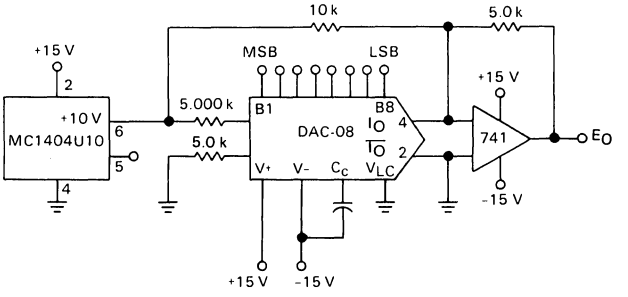
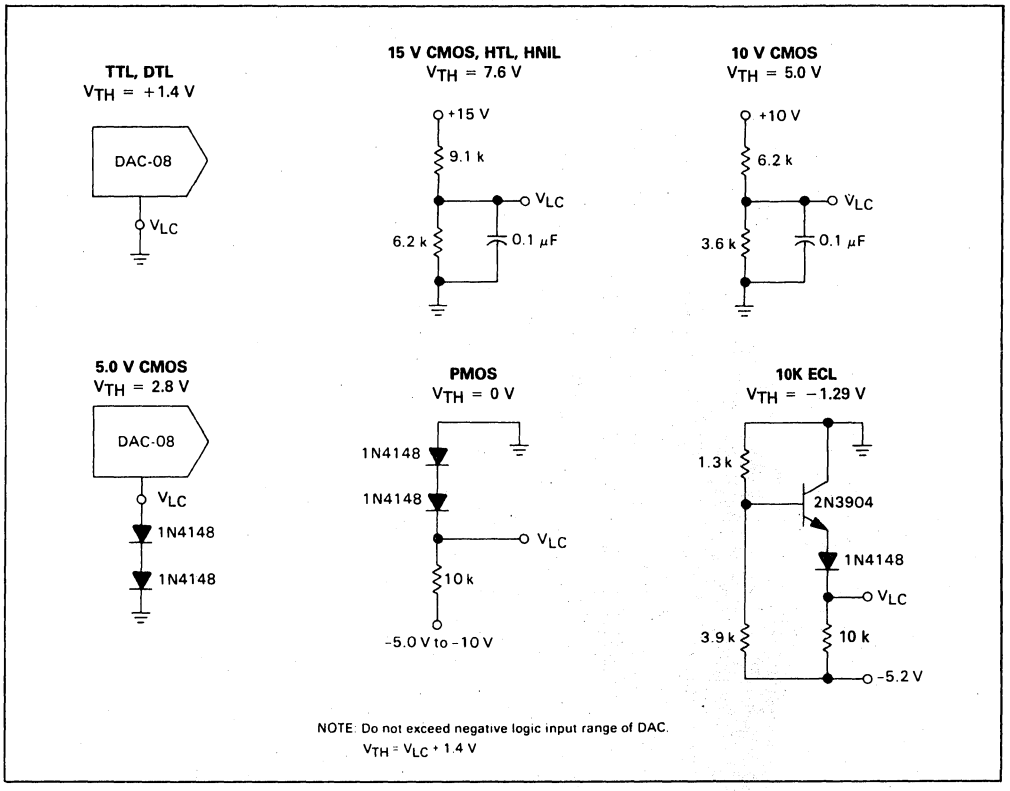
FIGURE 22 – OFFSET BINARY OPERATION



	B1	B2	B3	B4	B5	B6	B7	B8	E_O
Pos Full Range	1	1	1	1	1	1	1	1	-4.960
Zero Scale	1	0	0	0	0	0	0	0	0.000
Neg Full Scale +1 LSB	0	0	0	0	0	0	0	1	-4.960
Neg Full Scale	0	0	0	0	0	0	0	0	-5.000

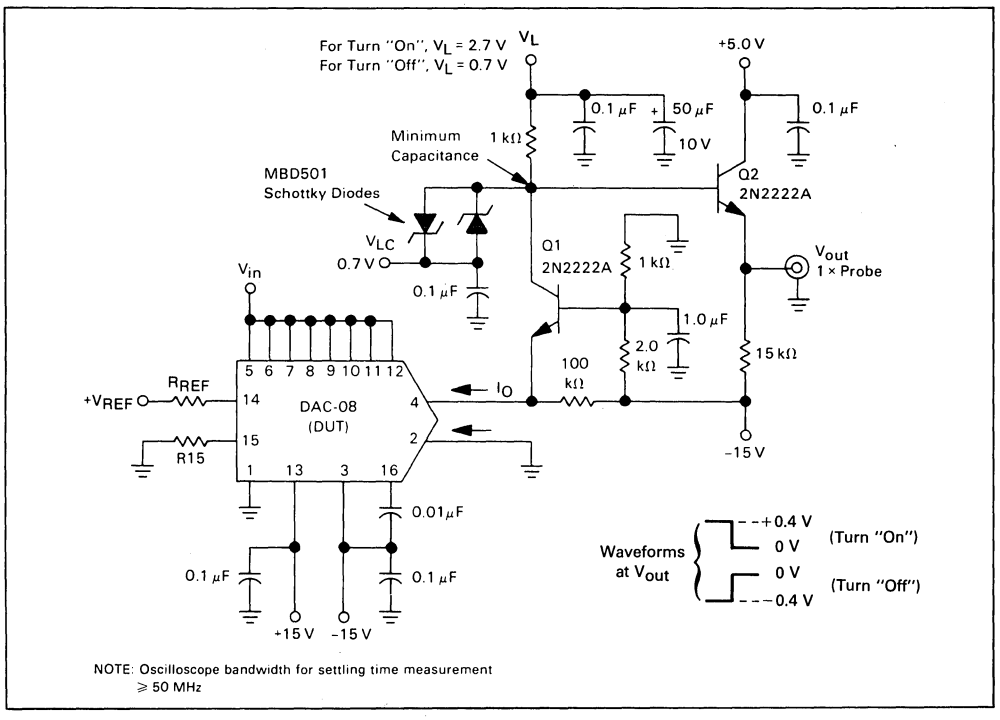
FIGURE 23 — INTERFACING WITH VARIOUS LOGIC FAMILIES



NOTE: Do not exceed negative logic input range of DAC.
$V_{TH} = V_{LC} + 1.4$ V

6

FIGURE 24 — SETTLING TIME MEASUREMENT CIRCUIT



NOTE: Oscilloscope bandwidth for settling time measurement
⩾ 50 MHz

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC1408
MC1508

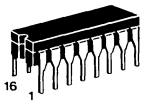
EIGHT-BIT MULTIPLYING DIGITAL-TO-ANALOG CONVERTER

. . . designed for use where the output current is a linear product of an eight-bit digital word and an analog input voltage.

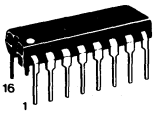
- Eight-Bit Accuracy Available in Both Temperature Ranges
  Relative Accuracy: ±0.19% Error maximum
  (MC1408L8, MC1408P8, MC1508L8)
- Seven and Six-Bit Accuracy Available with MC1408 Designated by 7 or 6 Suffix after Package Suffix
- Fast Settling Time — 300 ns typical
- Noninverting Digital Inputs are MTTL and CMOS Compatible
- Output Voltage Swing — +0.4 V to -5.0 V
- High-Speed Multiplying Input
  Slew Rate 4.0 mA/μs
- Standard Supply Voltages: +5.0 V and -5.0 V to -15 V

EIGHT-BIT MULTIPLYING DIGITAL-TO-ANALOG CONVERTER

SILICON MONOLITHIC INTEGRATED CIRCUIT



L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

6

ORDERING INFORMATION

Device	Temperature Range	Package
MC1408PB	0 to +75°C	Plastic
MC1408LB		Ceramic
MC1508LB	-55 to +1255°C	Ceramic

FIGURE 1 — D-to-A TRANSFER CHARACTERISTICS

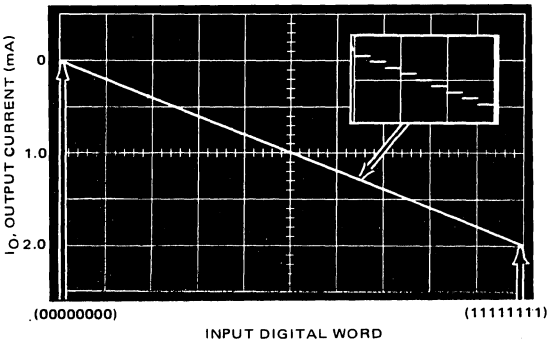
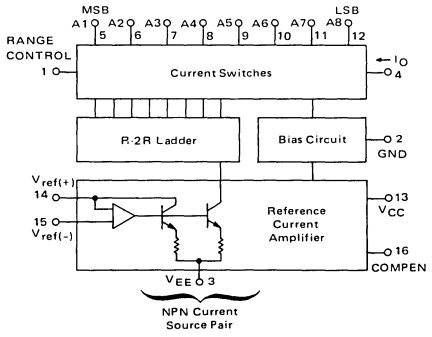


FIGURE 2 — BLOCK DIAGRAM



MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+5.5 -16.5	Vdc
Digital Input Voltage	V_5 thru V_{12}	0 to +5.5	Vdc
Applied Output Voltage	V_O	+0.5,-5.2	Vdc
Reference Current	I_{14}	5.0	mA
Reference Amplifier Inputs	V_{14},V_{15}	V_{CC},V_{EE}	Vdc
Operating Temperature Range MC1508 MC1408 Series	T_A	 -55 to +125 0 to +75	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

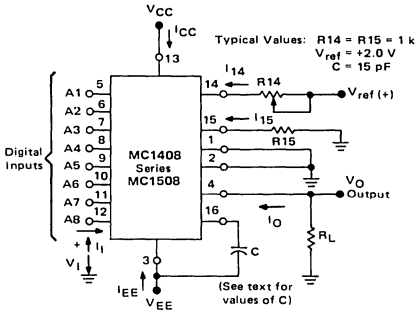
ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 Vdc, V_{EE} = -15 Vdc, $\frac{V_{ref}}{R14}$ = 2.0 mA, MC1508L8: T_A = -55°C to +125°C. MC1408L Series: T_A = 0 to + 75°C unless otherwise noted. All digital inputs at high logic level.)

Characteristics	Figure	Symbol	Min	Typ	Max	Unit
Relative Accuracy (Error relative to full scale I_O) MC1508L8, MC1408L8, MC1408P8	4	E_r	 — — —	 — — —	 ±0.19 ±0.39 ±0.78	%
Settling Time to with ±1/2 LSB (includes t_{PLH})(T_A = + 25°C) (Note 2)	5	t_s	—	300	—	ns
Propagation Delay Time T_A = + 25°C	5	t_{PHL}, t_{PHL}	—	30	100	ns
Output Full Scale Current Drift		TCI_O	—	- 20	—	PPM/°C
Digital Input Logic Levels (MSB) High Level, Logic "1" Low Level, Logic "0"	3	 V_{IH} V_{IL}	 2.0 —	 — —	 — 0.8	Vdc
Digital Input Current (MSB) High Level, V_{IH} = 5.0 V Low Level, V_{IL} = 0.8 V	3	 I_{IH} I_{IL}	 — —	 0 - 0.4	 0.04 - 0.8	mA
Reference Input Bias Current (Pin 15)	3	I_{15}	—	- 1.0	- 5.0	µA
Output Current Range V_{EE} = -5.0 V V_{EE} = - 15 V, T_A = 25°C	3	I_{OR}	 0 0	 2.0 2.0	 2.1 4.2	mA
Output Current V_{REF} = 2.000 V, R14 = 1000 Ω	3	I_O	 1.9	 1.99	 2.1	mA
Output Current (All Bits Low)	3	$I_{O(min)}$	—	0	4.0	µA
Output Voltage Compliance (E_r ≤ 0.19% at T_A = + 25°C) Pin 1 Grounded Pin 1 Open, V_{EE} below - 10 V	3	V_O	 — —	 — —	 -0.55, +0.4 -5.0, +0.4	Vdc
Reference Current Slew Rate	6	SR I_{ref}	—	4.0	—	mA/µs
Output Current Power Supply Sensitivity		PSRR(-)	—	0.5	2.7	µA/V
Power Supply Current (All Bits Low)	3	I_{CC} I_{EE}	— —	+ 13.5 - 7.5	+ 22 - 13	mA
Power Supply Voltage Range (T_A = + 25°C)	3	V_{CCR} V_{EER}	+ 4.5 - 4.5	+ 5.0 - 15	+ 5.5 - 16.5	Vdc
Power Dissipation All Bits Low V_{EE} = - 5.0 Vdc V_{EE} = -15 Vdc All Bits High V_{EE} = - 5.0 Vdc V_{EE} = -15 Vdc	3	P_D	 — — — —	 105 190 90 160	 170 305 — —	mW

Notes: 1. All current switches are tested to guarantee at least 50% of rated output current.
2. All bits switched.

TEST CIRCUITS

FIGURE 3 – NOTATION DEFINITIONS TEST CIRCUIT



V_I and I_I apply to inputs A1 thru A8

The resistor tied to pin 15 is to temperature compensate the bias current and may not be necessary for all applications.

$$I_O = K \left\{ \frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \frac{A4}{16} + \frac{A5}{32} + \frac{A6}{64} + \frac{A7}{128} + \frac{A8}{256} \right\}$$

where $K \cong \frac{V_{ref}}{R14}$

and A_N = "1" if A_N is at high level
A_N = "0" if A_N is at low level

FIGURE 4 – RELATIVE ACCURACY TEST CIRCUIT

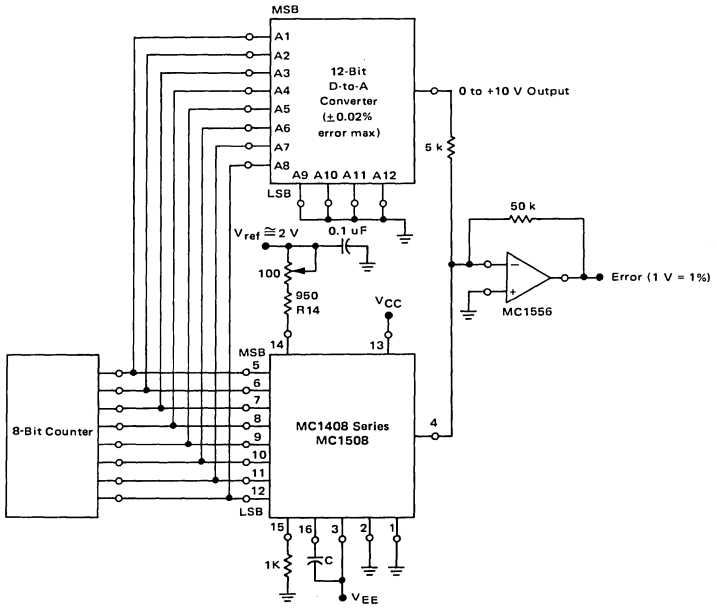
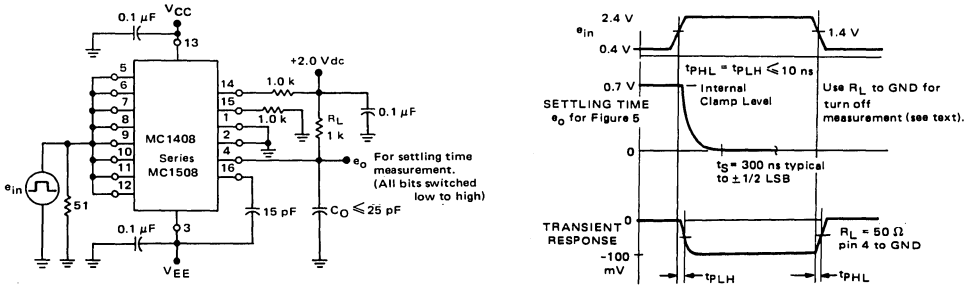


FIGURE 5 – TRANSIENT RESPONSE and SETTLING TIME



TEST CIRCUITS (continued)

FIGURE 6 – REFERENCE CURRENT SLEW RATE MEASUREMENT

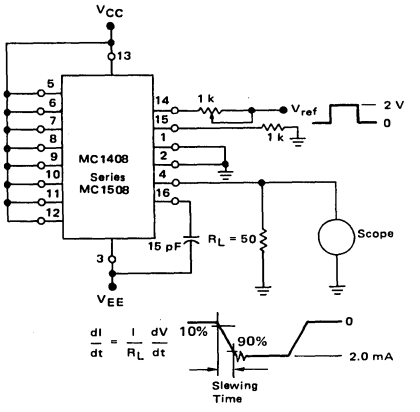


FIGURE 7 – POSITIVE V_{ref}

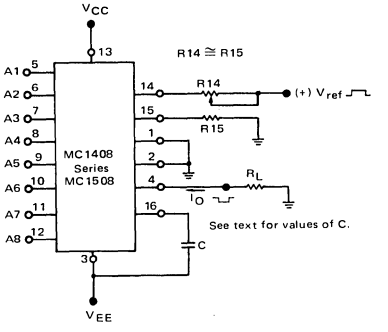


FIGURE 8 – NEGATIVE V_{ref}

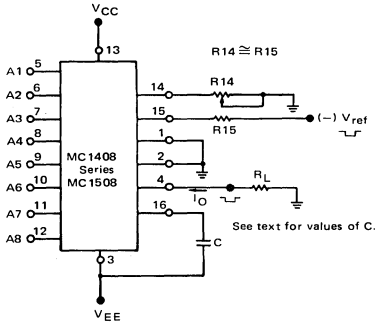
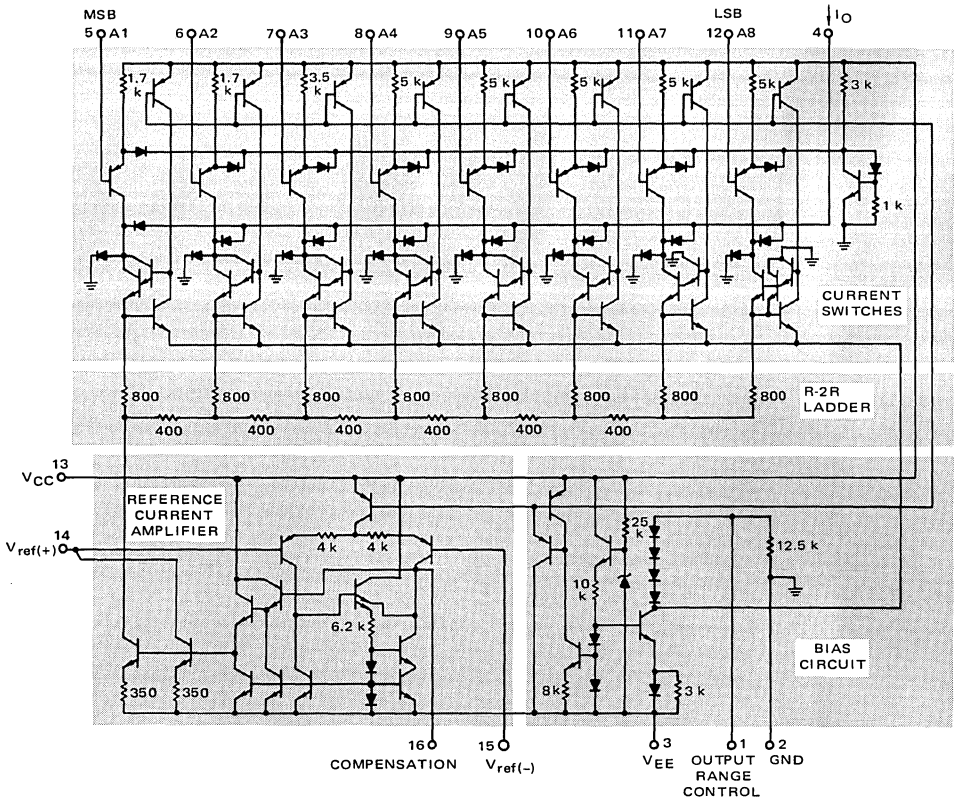


FIGURE 9 – MC1408, MC1508 SERIES EQUIVALENT CIRCUIT SCHEMATIC



CIRCUIT DESCRIPTION

The MC1408 consists of a reference current amplifier, an R-2R ladder, and eight high-speed current switches. For many applications, only a reference resistor and reference voltage need be added.

The switches are noninverting in operation, therefore a high state on the input turns on the specified output current component. The switch uses current steering for high speed, and a termination amplifier consisting of an active load gain stage with unity gain feedback. The termination amplifier holds the parasitic capacitance of the ladder at a constant voltage during switching, and provides a low impedance termination of equal voltage for all legs of the ladder.

The R-2R ladder divides the reference amplifier current into binarily-related components, which are fed to the switches. Note that there is always a remainder current which is equal to the least significant bit. This current is shunted to ground, and the maximum output current is 255/256 of the reference amplifier current, or 1.992 mA for a 2.0 mA reference amplifier current if the NPN current source pair is perfectly matched.

GENERAL INFORMATION

Reference Amplifier Drive and Compensation

The reference amplifier provides a voltage at pin 14 for converting the reference voltage to a current, and a turn-around circuit or current mirror for feeding the ladder. The reference amplifier input current, I14, must always flow into pin 14 regardless of the setup method or reference voltage polarity.

Connections for a positive reference voltage are shown in Figure 7. The reference voltage source supplies the full current I14. For bipolar reference signals, as in the multiplying mode, R15 can be tied to a negative voltage corresponding to the minimum input level. It is possible to eliminate R15 with only a small sacrifice in accuracy and temperature drift. Another method for bipolar inputs is shown in Figure 25.

The compensation capacitor value must be increased with increases in R14 to maintain proper phase margin; for R14 values of 1.0, 2.5 and 5.0 kilohms, minimum capacitor values are 15, 37, and 75 pF. The capacitor should be tied to V_{EE} as this increases negative supply rejection.

A negative reference voltage may be used if R14 is grounded and the reference voltage is applied to R15 as shown in Figure 8. A high input impedance is the main advantage of this method. Compensation involves a capacitor to V_{EE} on pin 16, using the values of the previous paragraph. The negative reference voltage must be at least 3.0-volts above the V_{EE} supply. Bipolar input signals may be handled by connecting R14 to a positive reference voltage equal to the peak positive input level at pin 15.

When a dc reference voltage is used, capacitive bypass to ground is recommended. The 5.0-V logic supply is not recommended as a reference voltage. If a well regulated 5.0-V supply which drives logic is to be used as the reference, R14 should be decoupled by connecting it to +5.0 V through another resistor and bypassing the junction of the two resistors with 0.1 μF to ground. For reference voltages greater than 5.0 V, a clamp diode is recommended between pin 14 and ground.

If pin 14 is driven by a high impedance such as a transistor current source, none of the above compensation methods apply and the amplifier must be heavily compensated, decreasing the overall bandwidth.

Output Voltage Range

The voltage on pin 4 is restricted to a range of -0.55 to +0.4 volts at +25°C, due to the current switching methods employed in the MC1408. When a current switch is turned "off", the positive voltage on the output terminal can turn "on" the output diode and increase the output current level. When a current switch is turned "on", the negative output voltage range is restricted. The base of the termination circuit Darlington transistor is one diode voltage below ground when pin 1 is grounded, so a negative voltage below the specified safe level will drive the low current device of the Darlington into saturation, decreasing the output current level.

The negative output voltage compliance of the MC1408 may be extended to -5.0 V volts by opening the circuit at pin 1. The negative supply voltage must be more negative than -10 volts. Using a full scale current of 1.992 mA and load resistor of 2.5 kilohms between pin 4 and ground will yield a voltage output of 256 levels between 0 and -4.980 volts. Floating pin 1 does not affect the converter speed or power dissipation. However, the value of the load resistor determines the switching time due to increased voltage swing. Values of R_L up to 500 ohms do not significantly affect performance, but a 2.5-kilohm load increases "worst case" settling time to 1.2 μs (when all bits are switched on). Refer to the subsequent text section on Settling Time for more details on output loading.

If a power supply value between -5.0 V and -10 V is desired, a voltage of between 0 and -5.0 V may be applied to pin 1. The value of this voltage will be the maximum allowable negative output swing.

Output Current Range

The output current maximum rating of 4.2 mA may be used only for negative supply voltages typically more negative than -8.0 volts, due to the increased voltage drop across the 350-ohm resistors in the reference current amplifier.

Accuracy

Absolute accuracy is the measure of each output current level with respect to its intended value, and is dependent upon relative accuracy and full scale current drift. Relative accuracy is the measure of each output current level as a fraction of the full scale current. The relative accuracy of the MC1408 is essentially constant with temperature due to the excellent temperature tracking of the monolithic resistor ladder. The reference current may drift with temperature, causing a change in the absolute accuracy of output current. However, the MC1408 has a very low full scale current drift with temperature.

The MC1408/MC1508 Series is guaranteed accurate to within ±1/2 LSB at +25°C at a full scale output current of 1.992 mA. This corresponds to a reference amplifier output current drive to the ladder network of 2.0 mA, with the loss of one LSB = 8.0 μA which is the ladder remainder shunted to ground. The input current to pin 14 has a guaranteed value of between 1.9 and 2.1 mA, allowing some mismatch in the NPN current source pair. The accuracy test circuit is shown in Figure 4. The 12-bit converter is calibrated for a full scale output current of 1.992 mA. This is an optional step since the MC1408 accuracy is essentially the same between 1.5 and 2.5 mA. Then the MC1408 circuits' full scale current is trimmed to the same value with R14 so that a zero value appears at the error amplifier output. The counter is activated and the error band may be displayed on an oscilloscope, detected by comparators, or stored in a peak detector.

Two 8-bit D-to-A converters may not be used to construct a 16-bit accurate D-to-A converter. 16-bit accuracy implies a total error of ±1/2 of one part in 65, 536, or ±0.00076%, which is much more accurate than the ±0.19% specification provided by the MC1408x8.

Multiplying Accuracy

The MC1408 may be used in the multiplying mode with eight-bit accuracy when the reference current is varied over a range of 256:1. The major source of error is the bias current of the termination amplifier. Under "worst case" conditions, these eight amplifiers can contribute a total of 1.6 μA extra current at the output terminal. If the reference current in the multiplying mode ranges from 16 μA to 4.0 mA, the 1.6 μA contributes an error of 0.1 LSB. This is well within eight-bit accuracy referenced to 4.0 mA.

A monotonic converter is one which supplies an increase in current for each increment in the binary word. Typically, the MC1408 is monotonic for all values of reference current above 0.5 mA. The recommended range for operation with a dc reference current is 0.5 to 4.0 mA.

GENERAL INFORMATION (Continued)

Settling Time

The "worst case" switching condition occurs when all bits are switched "on", which corresponds to a low-to-high transition for all bits. This time is typically 300 ns for settling to within ±1/2 LSB, for 8-bit accuracy, and 200 ns to 1/2 LSB for 7 and 6-bit accuracy. The turn off is typically under 100 ns. These times apply when $R_L \leqslant 500$ ohms and $C_O \leqslant 25$ pF.

The slowest single switch is the least significant bit, which turns "on" and settles in 250 ns and turns "off" in 80 ns. In applications where the D-to-A converter functions in a positive-going ramp mode, the "worst case" switching condition does not occur, and a settling time of less than 300 ns may be realized. Bit A7 turns "on" in 200 ns and "off" in 80 ns, while bit A6 turns "on" in 150 ns and "off" in 80 ns.

The test circuit of Figure 5 requires a smaller voltage swing for the current switches due to internal voltage clamping in the MC-1408. A 1.0-kilohm load resistor from pin 4 to ground gives a typical settling time of 400 ns. Thus, it is voltage swing and not the output RC time constant that determines settling time for most applications.

Extra care must be taken in board layout since this is usually the dominant factor in satisfactory test results when measuring settling time. Short leads, 100 μF supply bypassing for low frequencies, and minimum scope lead length are all mandatory.

TYPICAL CHARACTERISTICS

(V_{CC} = +5.0 V, V_{EE} = -15 V, T_A = +25°C unless otherwise noted.)

6

FIGURE 10 – LOGIC INPUT CURRENT versus INPUT VOLTAGE

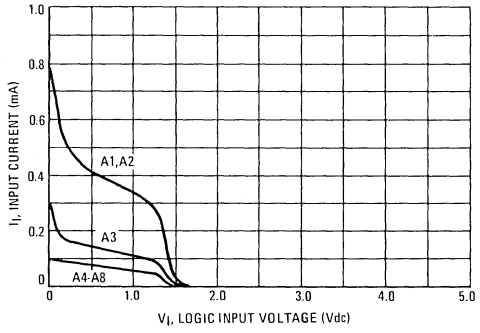


FIGURE 11 – TRANSFER CHARACTERISTIC versus TEMPERATURE (A5 thru A8 thresholds lie within range for A1 thru A4)

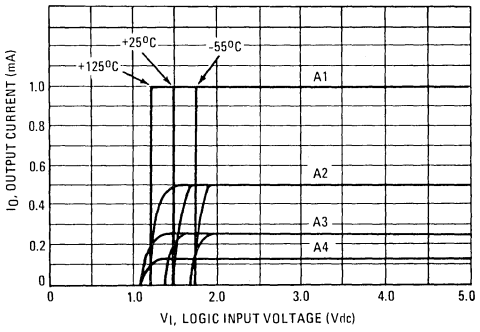


FIGURE 12 – OUTPUT CURRENT versus OUTPUT VOLTAGE (See text for pin 1 restrictions)

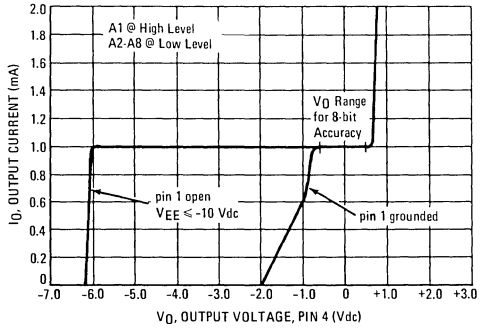
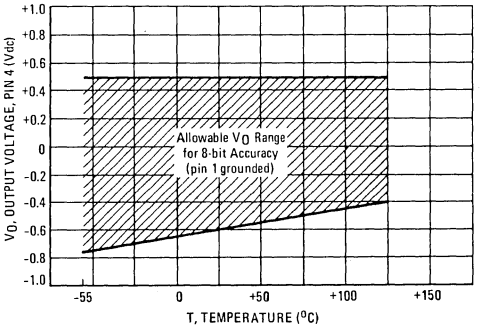


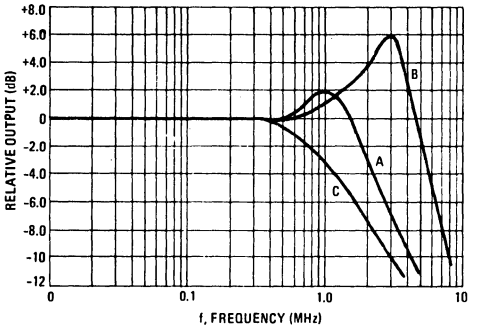
FIGURE 13 – OUTPUT VOLTAGE versus TEMPERATURE (Negative range with pin 1 open is -5.0 Vdc over full temperature range)



TYPICAL CHARACTERISTICS (continued)

(V_{CC} = +5.0 V, V_{EE} = -15 V, T_A = +25°C unless otherwise noted.)

FIGURE 14 – REFERENCE INPUT FREQUENCY RESPONSE



Unless otherwise specified:

R14 = R15 = 1.0 kΩ
C = 15 pF, pin 16 to V_{EE}
R_L = 50 Ω, pin 4 to GND

Curve A: Large Signal Bandwidth
Method of Figure 7
V_{ref} = 2.0 V(p-p) offset 1.0 V above GND

Curve B: Small Signal Bandwidth
Method of Figure 7 R_L = 250 Ω
V_{ref} = 50 mV(p-p) offset 200 mV above GND

Curve C: Large and Small Signal Bandwidth
Method of Figure 25 (no op-ampl, R_L = 50 Ω)
R_S = 50 Ω
V_{ref} = 2.0 V
V_S = 100 mV(p-p) centered at 0 V

FIGURE 15 – TYPICAL POWER SUPPLY CURRENT versus TEMPERATURE (all bits low)

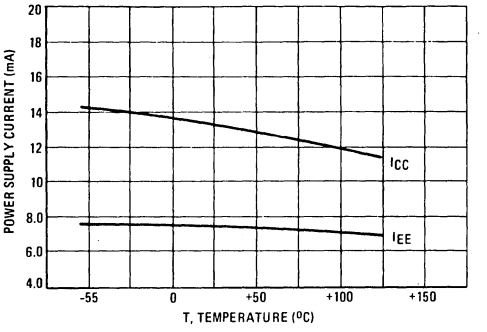
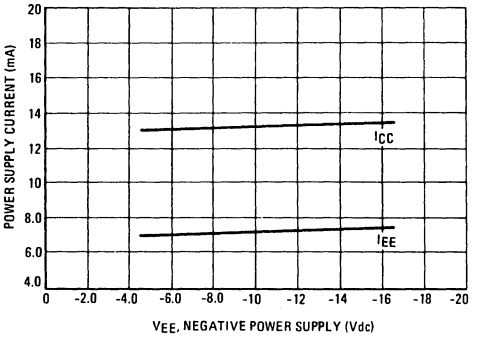
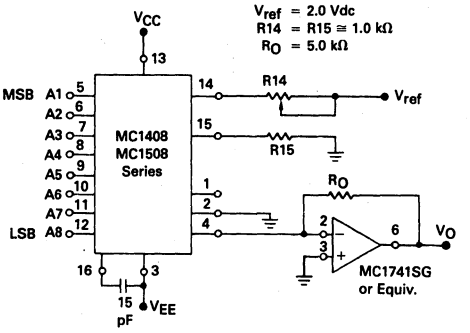


FIGURE 16 – TYPICAL POWER SUPPLY CURRENT versus V_{EE} (all bits low)



APPLICATIONS INFORMATION

FIGURE 17 – OUTPUT CURRENT TO VOLTAGE CONVERSION



Theoretical V_O

$$V_O = \frac{V_{ref}}{R14}(R_O)\left[\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \frac{A4}{16} + \frac{A5}{32} + \frac{A6}{64} + \frac{A7}{128} + \frac{A8}{256}\right]$$

Adjust V_{ref}, R14 or R_O so that V_O with all digital inputs at high level is equal to 9.961 volts.

$$V_O = \frac{2\ V}{1\ k}(5\ k)\left[\frac{1}{2} + \frac{1}{4} + \frac{1}{8} + \frac{1}{16} + \frac{1}{32} + \frac{1}{64} + \frac{1}{128} + \frac{1}{256}\right]$$

$$= 10\ V\left[\frac{255}{256}\right] = 9.961\ V$$

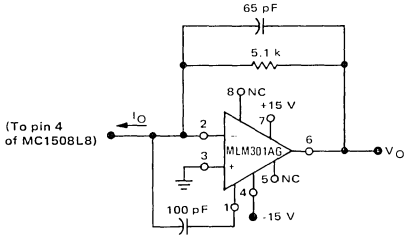
APPLICATIONS INFORMATION (continued)

Voltage outputs of a larger magnitude are obtainable with this circuit which uses an external operational amplifier as a current to voltage converter. This configuration automatically keeps the output of the MC1408 at ground potential and the operational amplifier can generate a positive voltage limited only by its positive supply voltage. Frequency response and settling time are primarily determined by the characteristics of the operational amplifier. In addition, the operational amplifier must be compensated for unity gain, and in some cases overcompensation may be desirable.

Note that this configuration results in a positive output voltage only, the magnitude of which is dependent on the digital input.

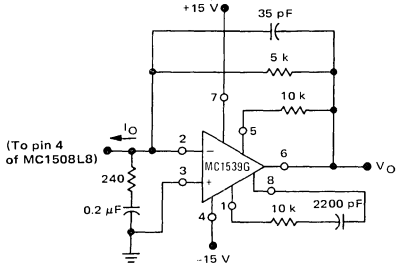
The following circuit shows how the MLM301AG can be used in a feedforward mode resulting in a full scale settling time on the order of 2.0 μs.

FIGURE 18



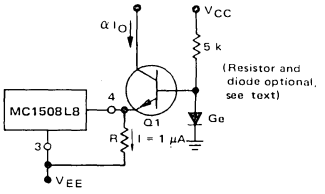
An alternative method is to use the MC1539G and input compensation. Response of this circuit is also on the order of 2.0 μs. See Motorola Application Note AN-459 for more details on this concept.

FIGURE 19



The positive voltage range may be extended by cascading the output with a high beta common base transistor, Q1, as shown.

FIGURE 20 – EXTENDING POSITIVE VOLTAGE RANGE



The output voltage range for this circuit is 0 volts to BV_{CBO} of the transistor. If pin 1 is left open, the transistor base may be grounded, eliminating both the resistor and the diode. Variations in beta must be considered for wide temperature range applications. An inverted output waveform may be obtained by using a load resistor from a positive reference voltage to the collector of the transistor. Also, high-speed operation is possible with a large output voltage swing, because pin 4 is held at a constant voltage. The resistor (R) to V_{EE} maintains the transistor emitter voltage when all bits are "off" and insures fast turn-on of the least significant bit.

Combined Output Amplifier and Voltage Reference

For many of its applications the MC1408 requires a reference voltage and an operational amplifier. Normally the operational amplifier is used as a current to voltage converter and its output need only go positive. With the popular MC1723G voltage regulator both of these functions are provided in a single package with the added bonus of up to 150 mA of output current. See Figure 21. The MC1723G uses both a positive and negative power supply. The reference voltage of the MC1723G is then developed with respect to the negative voltage and appears as a common-mode signal to the reference amplifier in the D-to-A converter. This allows use of its output amplifier as a classic current-to-voltage converter with the non-inverting input grounded.

Since ±15 V and +5.0 V are normally available in a combination digital-to-analog system, only the -5.0 V need be developed. A resistor divider is sufficiently accurate since the allowable range on pin 5 is from -2.0 to -8.0 volts. The 5.0 kilohm pulldown resistor on the amplifier output is necessary for fast negative transitions.

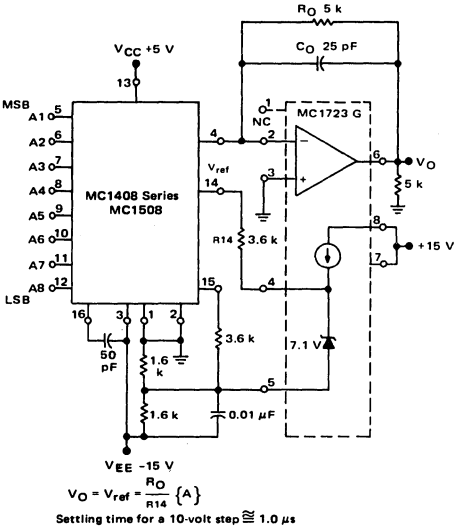
Full scale output may be increased to as much as 32 volts by increasing R_O and raising the +15 V supply voltage to 35 V maximum. The resistor divider should be altered to comply with the maximum limit of 40 volts across the MC1723G. C_O may be decreased to maintain the same R_OC_O product if maximum speed is desired.

APPLICATIONS INFORMATION (continued)

Programmable Power Supply

The circuit of Figure 21 can be used as a digitally programmed power supply by the addition of thumbwheel switches and a BCD-to-binary converter. The output voltage can be scaled in several ways, including 0 to +25.5 volts in 0.1-volt increments, ±0.05 volt; or 0 to 5.1 volts in 20 mV increments, ±10 mV.

FIGURE 21 – COMBINED OUTPUT AMPLIFIER and VOLTAGE REFERENCE CIRCUIT



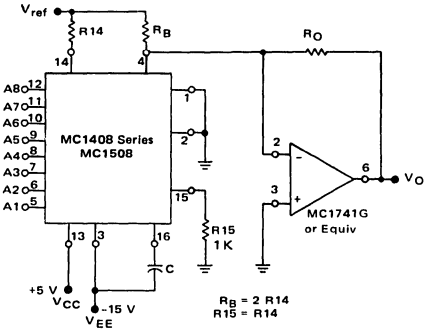
$$V_O = V_{ref} \frac{R_O}{R14} \{A\}$$

Settling time for a 10-volt step ≅ 1.0 µs

Bipolar or Negative Output Voltage

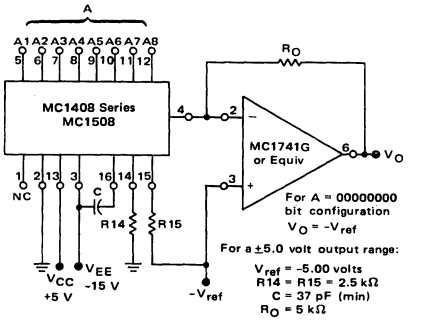
The circuit of Figure 22 is a variation from the standard voltage output circuit and will produce bipolar output signals. A positive current may be sourced into the summing node to offset the output voltage in the negative direction. For example, if approximately 1.0 mA is used a bipolar output signal results which may be described as a 8-bit "1's" complement offset binary. V_{ref} may be used as this auxiliary reference. Note that R_O has been doubled to 10 kilohms because of the anticipated 20 V(p-p) output range.

FIGURE 22 – BIPOLAR OR NEGATIVE OUTPUT VOLTAGE CIRCUIT



$$V_O = \frac{V_{ref}}{R14}(R_O)\left[\frac{A1}{2}+\frac{A2}{4}+\frac{A3}{8}+\frac{A4}{16}+\frac{A5}{32}+\frac{A6}{64}+\frac{A7}{128}+\frac{A8}{256}\right] - \frac{V_{ref}}{R_B}(R_O)$$

FIGURE 23 – BIPOLAR OR INVERTED NEGATIVE OUTPUT VOLTAGE CIRCUIT



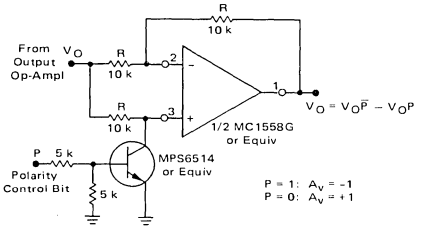
Decrease R_O to 2.5 kΩ for a 0 to -5.0-volt output range. This application provides somewhat lower speed, as previously discussed in the Output Voltage Range section of the General Information.

APPLICATIONS INFORMATION (continued)

Polarity Switching Circuit, 8-Bit Magnitude Plus Sign D-to-A Converter

Bipolar outputs may also be obtained by using a polarity switching circuit. The circuit of Figure 24 gives 8-bit magnitude plus a sign bit. In this configuration the operational amplifier is switched between a gain of +1.0 and -1.0. Although another operational amplifier is required, no more space is taken when a dual operational amplifier such as the MC1558G is used. The transistor should be selected for a very low saturation voltage and resistance.

FIGURE 24 – POLARITY SWITCHING CIRCUIT
(8-Bit Magnitude Plus Sign D-to-A Converter)



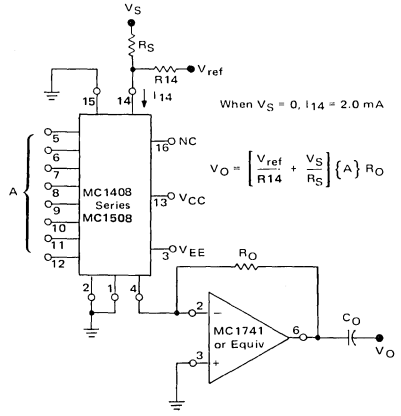
Programmable Gain Amplifier or Digital Attenuator

When used in the multiplying mode the MC1408 can be applied as a digital attenuator. See Figure 25. One advantage of this technique is that if R_S = 50 ohms, no compensation capacitor is needed. The small and large signal bandwidths are now identical and are shown in Figure 14.

The best frequency response is obtained by not allowing I_{14} to reach zero. However, the high impedance node, pin 16, is clamped to prevent saturation and insure fast recovery when the current through R14 goes to zero. R_S can be set for a ±1.0 mA variation in relation to I_{14}. I_{14} can never be negative.

The output current is always unipolar. The quiescent dc output current level changes with the digital word which makes ac coupling necessary.

FIGURE 25 – PROGRAMMABLE GAIN AMPLIFIER OR DIGITAL ATTENUATOR CIRCUIT



Panel Meter Readout

The MC1408 can be used to read out the status of BCD or binary registers or counters in a digital control system. The current output can be used to drive directly an analog panel meter. External meter shunts may be necessary if a meter of less than 2.0 mA full scale is used. Full scale calibration can be done by adjusting R14 or V_{ref}.

FIGURE 26 – PANEL METER READOUT CIRCUIT

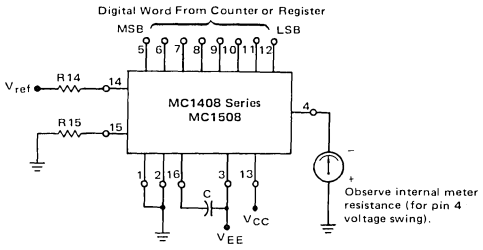
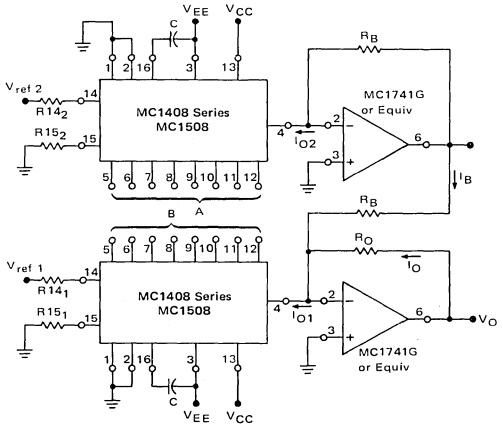


FIGURE 27 – DC COUPLED DIGITAL ATTENUATOR and DIGITAL SUBTRACTION



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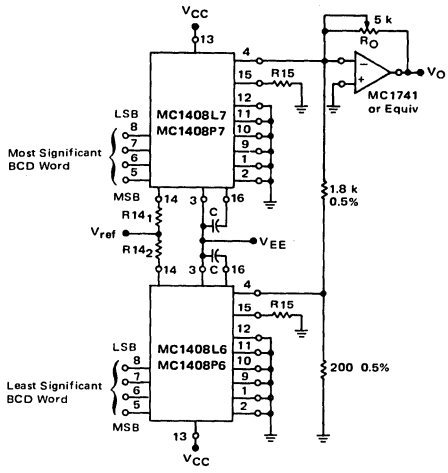
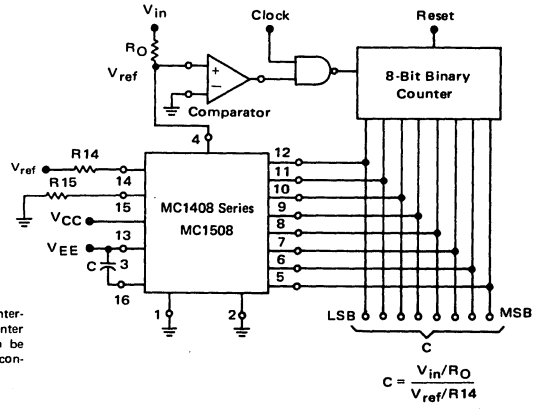
APPLICATIONS INFORMATION (continued)

FIGURE 36 – TWO-DIGIT BCD CONVERSION



Two 8-bit, D-to-A converters can be used to build a two digit BCD D-to-A or A-to-D converter. If both outputs feed the virtual ground of an operational amplifier, 10:1 current scaling can be achieved with a resistive current divider. If current output is desired, the units may be operated at full scale current levels of 4.0 mA and 0.4 mA with the outputs connected to sum the currents. The error of the D-to-A converter handling the least significant bits will be scaled down by a factor of ten and thus an MC1408L6 may be used for the least significant word.

FIGURE 37 – DIGITAL QUOTIENT OF TWO ANALOG VARIABLES or ANALOG-TO-DIGITAL CONVERSION



The circuit shown is a simple counter-ramp converter. An UP/DOWN counter and dual threshold comparator can be used to provide faster operation and continuous conversion.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC10319

HIGH SPEED 8-BIT ANALOG-TO-DIGITAL FLASH CONVERTER

SILICON MONOLITHIC INTEGRATED CIRCUIT

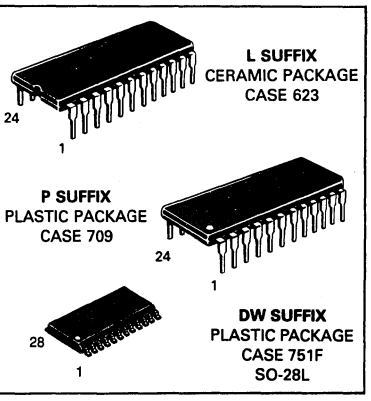
HIGH SPEED 8-BIT ANALOG-TO-DIGITAL CONVERTER

The MC10319 is an 8-bit high speed parallel flash A/D converter. The device employs an internal Gray Code structure to eliminate large output errors on fast slewing input signals. It is fully TTL compatible, requiring a +5.0 V supply and a wide tolerance negative supply of −3.0 to −6.0 V. Three-state TTL outputs allow direct drive of a data bus or common I/O memory.

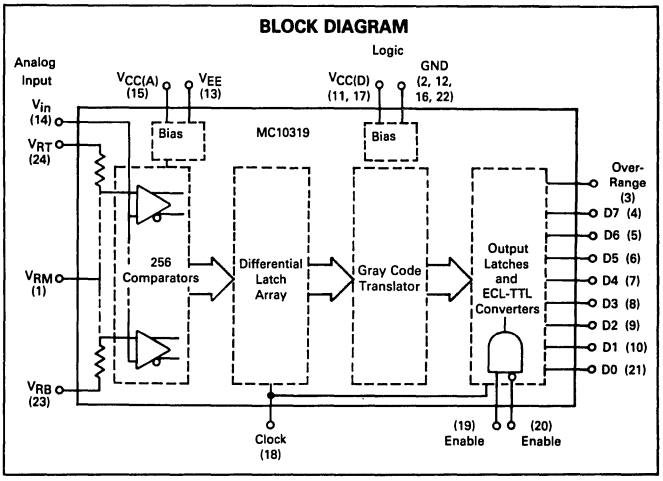
The MC10319 contains 256 parallel comparators across a precision input reference network. The comparator outputs are fed to latches and then to an encoder network, to produce an 8-bit data byte plus an overrange bit. The data is latched and converted to 3-state LS-TTL outputs. The overrange bit is always active to allow for either sensing of the overrange condition or ease of interconnecting a pair of devices to produce a 9-bit A/D converter.

Applications include Video Display and Radar processing, high speed instrumentation and TV Broadcast encoding.

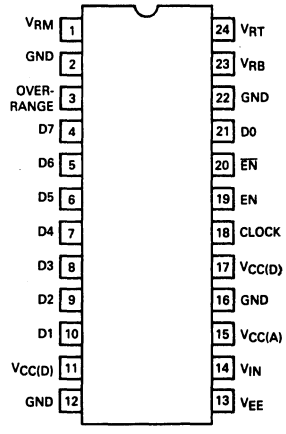
- Internal Gray Code for Speed and Accuracy, Binary Outputs
- 8-Bit Resolution/9-Bit Typical Accuracy
- Easily Interconnected for 9-Bit Conversion
- 3-State LS-TTL Outputs with True and Complement Enable Inputs
- 25 MHz Sampling Rate
- Wide Input Range: 1.0–2.0 V_{p-p} Between ±2.0 V
- Low Input Capacitance: 50 pF
- Low Power Dissipation: 618 mW
- No Sample/Hold Required for Video Bandwidth Signals
- Single Clock Cycle Conversion



BLOCK DIAGRAM



PIN DIAGRAM
(L and P only)



ORDERING INFORMATION

Device	Temperature Range	Package
MC10319DW MC10319L MC10319P	0° to +70°C	SO-28L Ceramic Plastic

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Supply Voltage	$V_{CC(A),(D)}$ V_{EE}	+7.0 −7.0	Vdc
Positive Supply Voltage Differential	$V_{CC(D)}-V_{CC(A)}$	−0.3 to +0.3	Vdc
Digital Input Voltage (Pins 18–20)	$V_{I(D)}$	−0.5 to +7.0	Vdc
Analog Input Voltage (Pins 1, 14, 23, 24)	$V_{I(A)}$	−2.5 to +2.5	Vdc
Reference Voltage Span (Pin 24–Pin 23)	—	2.3	Vdc
Applied Output Voltage (Pins 4–10, 21 in 3-State)	—	−0.3 to +7.0	Vdc
Junction Temperature	T_J	+150	°C
Storage Temperature	T_{stg}	−65 to +150	°C

Devices should not be operated at these values. The "Recommended Operating Limits" provide guidelines for actual device operation.

RECOMMENDED OPERATING LIMITS

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Voltage (Pin 15) (Pins 11, 17)	$V_{CC(A)}$ $V_{CC(D)}$	+4.5	+5.0	+5.5	Vdc
$V_{CC(D)} - V_{CC(A)}$	ΔV_{CC}	−0.1	0	+0.1	Vdc
Power Supply Voltage (Pin 13)	V_{EE}	−6.0	−5.0	−3.0	Vdc
Digital Input Voltages (Pins 18–20)	$V_{I(D)}$	0	—	+5.0	Vdc
Analog Input (Pin 14)	$V_{I(A)}$	−2.1	—	+2.1	Vdc
Voltage @ V_{RT} (Pin 24)	V_{RT}	−1.0	—	+2.1	Vdc
Voltage @ V_{RB} (Pin 23)	V_{RB}	−2.1	—	+1.0	Vdc
$V_{RT} - V_{RB}$	ΔV_R	+1.0	—	+2.1	Vdc
$V_{RB} - V_{EE}$	—	1.3	—	—	Vdc
Applied Output Voltage (Pins 4–10, 21 in 3-State)	V_o	0	—	5.5	Vdc
Clock Pulse Width — High Low	t_{CKH} t_{CKL}	5.0 15	20 20	— —	ns
Clock Frequency	f_{CLK}	0	—	25	MHz
Operating Ambient Temperature	T_A	0	—	+70	°C

ELECTRICAL CHARACTERISTICS ($0° < T_A < 70°C$, V_{CC} = 5.0 V, V_{EE} = −5.2 V, V_{RT} = +1.0 V, V_{RB} = −1.0 V, except where noted.)

Parameter	Symbol	Min	Typ	Max	Unit
TRANSFER CHARACTERISTICS (f_{CKL} = 25 MHz)					
Resolution	N	—	—	8.0	Bits
Monotonicity	MON	Guaranteed			Bits
Integral Nonlinearity	INL	—	±1/4	±1.0	LSB
Differential Nonlinearity	DNL	—	—	±1.0	LSB
Differential Phase (See Figure 16)	DP	—	1.0	—	Deg.
Differential Gain (See Figure 16)	DG	—	1.0	—	%
Power Supply Rejection Ratio (4.5 V < V_{CC} < 5.5 V, V_{EE} = −5.2 V) (−6.0 V < V_{EE} < −3.0 V, V_{CC} = +5.0 V)	PSRR	 — —	 0.1 0	 — —	LSB/V

ELECTRICAL CHARACTERISTICS — continued ($0° < T_A < 70°C$, V_{CC} = 5.0 V, V_{EE} = −5.2 V, V_{RT} = +1.0 V, V_{RB} = −1.0 V, except where noted.)

Parameter	Symbol	Min	Typ	Max	Unit
ANALOG INPUT (PIN 14)					
Input Current @ $V_{in} = V_{RB}$ (See Figure 5)	I_{INL}	−100	0	—	μA
Input Current @ $V_{in} = V_{RT}$ (See Figure 5)	I_{INH}	—	60	150	μA
Input Capacitance ($V_{RT} - V_{RB}$ = 2.0 V, See Figure 4)	C_{in}	—	36	—	pF
Input Capacitance ($V_{RT} - V_{RB}$ = 1.0 V, See Figure 4)	C_{in}	—	55	—	pF
Bipolar Offset Error	V_{OS}	—	0.1	—	LSB
REFERENCE					
Ladder Resistance (V_{RT} to V_{RB}, T_A = 25°C)	R_{ref}	104	130	156	Ω
Temperature Coefficient	T_C	—	+0.29	—	%/°C
Ladder Capacitance (Pin 1 open)	C_{ref}	—	25	—	pF
ENABLE INPUTS (V_{CC} = 5.5 V) (See Figure 6)					
Input Voltage — High (Pins 19–20)	V_{IHE}	2.0	—	—	V
Input Voltage — Low (Pins 19–20)	V_{ILE}	—	—	0.8	V
Input Current @ 2.7 V	I_{IHE}	—	0	20	μA
Input Current @ 0.4 V @ $\overline{EN}$ (0 < EN < 5.0 V)	I_{IL1}	−400	−100	—	μA
Input Current @ 0.4 V @ EN ($\overline{EN}$ = 0 V)	I_{IL2}	−400	−100	—	μA
Input Current @ 0.4 V @ EN ($\overline{EN}$ = 2.0 V)	I_{IL3}	−20	−2.0	—	μA
Input Clamp Voltage (I_{IK} = −18 mA)	V_{IKE}	−1.5	−1.3	—	V
CLOCK INPUT (V_{CC} = 5.5 V)					
Input Voltage High	V_{IHC}	2.0	—	—	Vdc
Input Voltage Low	V_{ILC}	—	—	0.8	Vdc
Input Current @ 0.4 V (See Figure 7)	I_{ILC}	−400	−80	—	μA
Input Current @ 2.7 V (See Figure 7)	I_{IHC}	−100	−20	—	μA
Input Clamp Voltage (I_{IK} = −18 mA)	V_{IKC}	−1.5	−1.3	—	Vdc
DIGITAL OUTPUTS					
High Output Voltage (I_{OH} = −400 μA, V_{CC} = 4.5 V, See Figure 8)	V_{OH}	2.4	3.0	—	V
Low Output Voltage (I_{OL} = 4.0 mA, See Figure 9)	V_{OL}	—	0.35	0.4	V
Output Short Circuit Current* (V_{CC} = 5.5 V)	I_{SC}	—	35	—	mA
Output Leakage Current (0.4 < V_O < 2.4 V, See Figure 3, V_{CC} = 5.5 V, D0–D7 in 3-State Mode)	I_{LK}	−50	—	+50	μA
Output Capacitance (D0–D7 in 3-State Mode)	C_{out}	—	9.0	—	pF
POWER SUPPLIES					
$V_{CC(A)}$ Current (4.5 V < $V_{CC(A)}$ < 5.5 V) (Outputs unloaded)	$I_{CC(A)}$	10	17	25	mA
$V_{CC(D)}$ Current (4.5 V < $V_{CC(D)}$ < 5.5 V) (Outputs unloaded)	$I_{CC(D)}$	50	90	133	mA
V_{EE} Current (−6.0 V < V_{EE} < −3.0 V)	I_{EE}	−14	−10	−6.0	mA
Power Dissipation ($V_{RT} - V_{RB}$ = 2.0 V) (Outputs unloaded)	P_D	—	618	995	mW

*Only one output is to be shorted at a time, not to exceed 1 second.

6

TIMING CHARACTERISTICS (T_A = 25°C, V_{CC} = +5.0 V, V_{EE} = −5.2 V, V_{RT} = +1.0 V, V_{RB} = −1.0 V, See System Timing Diagram.)

Parameter	Symbol	Min	Typ	Max	Unit
INPUTS					
Min Clock Pulse Width — High	t_{CKH}	—	5.0	—	ns
Min Clock Pulse Width — Low	t_{CKL}	—	15	—	ns
Max Clock Rise, Fall Time	$t_{R,F}$	—	100	—	ns
Clock Frequency	f_{CLK}	0	30	25	MHz
OUTPUTS					
New Data Valid from Clock Low	t_{CKDV}	—	19	—	ns
Aperture Delay	t_{AD}	—	4.0	—	ns
Hold Time	t_H	—	6.0	—	ns
Data High to 3-State from Enable Low*	t_{EHZ}	—	27	—	ns
Data Low to 3-State from Enable Low*	t_{ELZ}	—	18	—	ns
Data High to 3-State from $\overline{\text{Enable}}$ High*	$t_{\overline{E}HZ}$	—	32	—	ns
Data Low to 3-State from $\overline{\text{Enable}}$ High*	$t_{\overline{E}LZ}$	—	18	—	ns
Valid Data from Enable High (Pin 20 = 0 V)*	t_{EDV}	—	15	—	ns
Valid Data from $\overline{\text{Enable}}$ Low (Pin 19 = 5.0 V)*	$t_{\overline{E}DV}$	—	16	—	ns
Output Transition Time* (10%–90%)	t_{tr}	—	8.0	—	ns

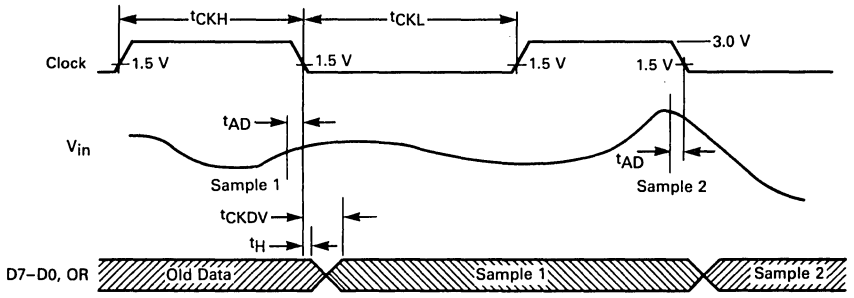
*See Figure 2 for output loading.

6

PIN DESCRIPTIONS

Symbol	Pin L,P Suffix	DW Suffix	Description
V_{RM}	1	1	The midpoint of the reference resistor ladder. Bypassing can be done at this point to improve performance at high frequencies.
GND	2, 12 16, 22	2, 13, 17 18, 25, 26	Digital ground. The pins should be connected directly together, and through a low impedance path to the power supply.
OVR	3	3	Overrange output. Indicates V_{in} is more positive than V_{RT} 1/2 LSB. This output does not have 3-state capability.
D7–DØ	4–10, 21	4–10, 24	Digital Outputs. D7 (Pin 4) is the MSB. DØ (Pin 21 or 24) is the LSB. LSTTL compatible with 3-state capability.
$V_{CC(D)}$	11, 17	11, 12 19, 20	Power supply for the digital section. +5.0 V, ±10% required. Reference to digital ground.
V_{EE}	13	14	Negative Power supply. Nominally −5.2 V, it can range from −3.0 to −6.0 V, and must be more negative than V_{RB} by >1.3 V. Reference to analog gnd.
V_{in}	14	15	Signal voltage input. This voltage is compared to the reference to generate a digital equivalent. Input impedance is nominally 16–33K in parallel with 36 pF.
$V_{CC(A)}$	15	16	Power supply for the analog section. +5.0 V, ±10% required. Reference to analog ground.
CLK	18	21	Clock input. TTL compatible.
EN	19	22	Enable input. TTL compatible, a logic 1 (and $\overline{\text{EN}}$ at a logic 0) enables the data outputs. A logic 0 puts the outputs in a 3-state mode.
$\overline{\text{EN}}$	20	23	$\overline{\text{Enable}}$ input. TTL compatible, a logic 0 (and EN at a logic 1) enables the data outputs. A logic 1 puts the outputs in a 3-state mode.
V_{RB}	23	27	The bottom (most negative point) of the internal reference resistor ladder.
V_{RT}	24	28	The top (most positive point) of the internal reference resistor ladder.

FIGURE 1 — SYSTEM TIMING DIAGRAM



t_{CKDV} and t_H measured at output levels of 0.8 and 2.4 volts.

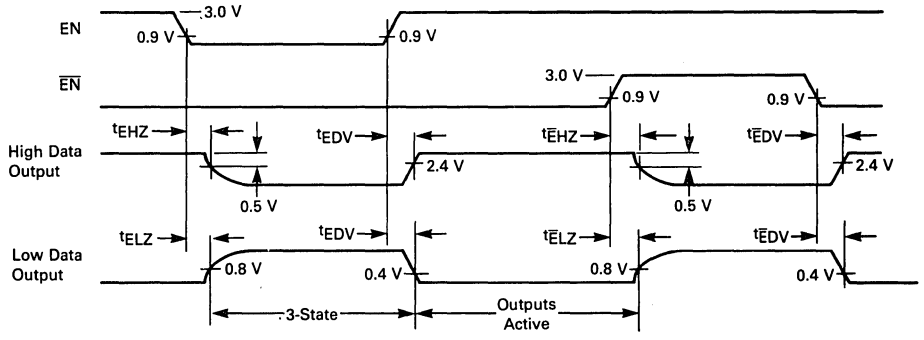
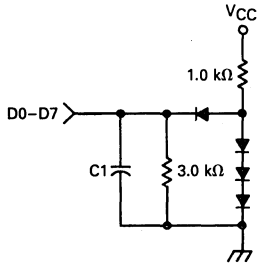


FIGURE 2 — DATA OUTPUT TEST CIRCUIT



Diodes = 1N914 or equivalent, C1 ≈ 15 pF

FIGURE 3 — OUTPUT 3-STATE LEAKAGE CURRENT

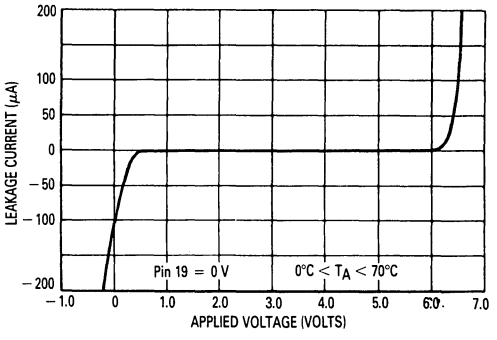


FIGURE 4 — INPUT CAPACITANCE @ V_{IN} (PIN 14)

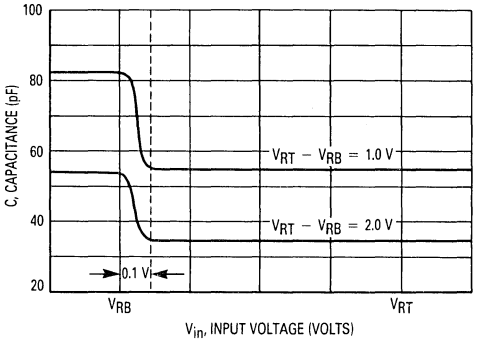


FIGURE 5 — INPUT CURRENT @ V_{IN} (PIN 14)

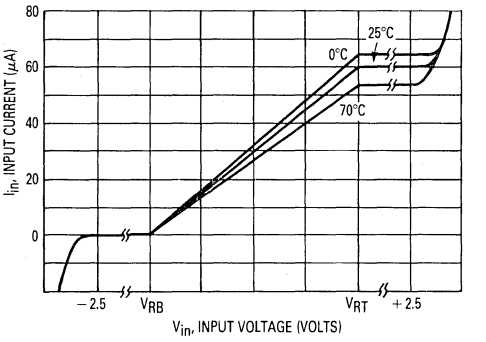


FIGURE 6 — INPUT CURRENT @ ENABLE, $\overline{\text{ENABLE}}$

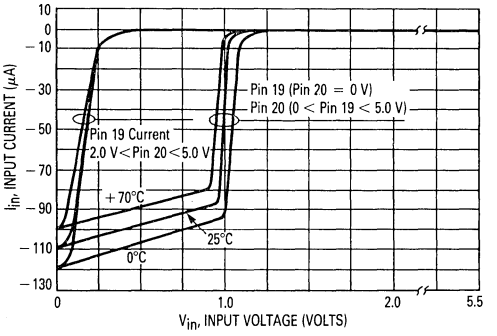


FIGURE 7 — CLOCK INPUT CURRENT

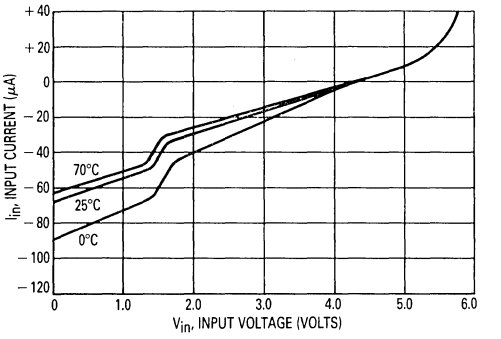


FIGURE 8 — OUTPUT VOLTAGE versus OUTPUT CURRENT

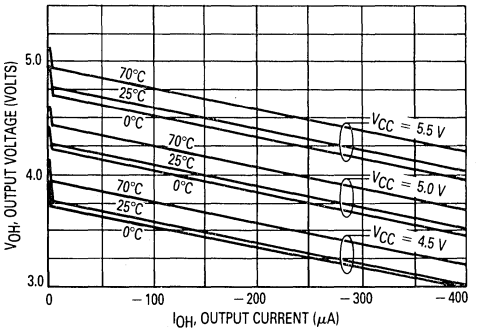


FIGURE 9 — OUTPUT VOLTAGE versus OUTPUT CURRENT

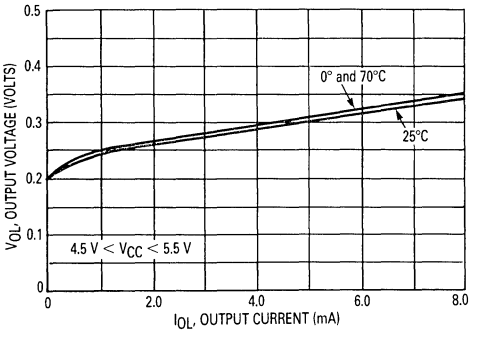


FIGURE 10 — SUPPLY CURRENT versus TEMPERATURE

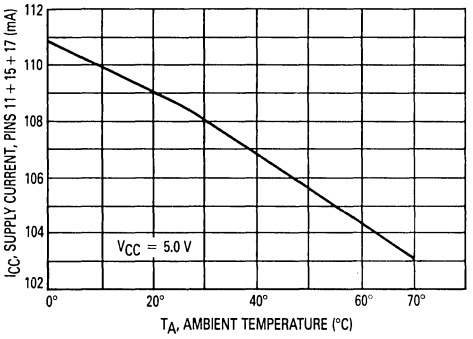


FIGURE 11 — SUPPLY CURRENT versus TEMPERATURE

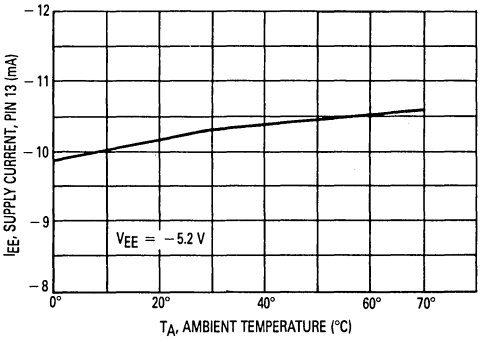


FIGURE 12 — DIFFERENTIAL LINEARITY ERROR

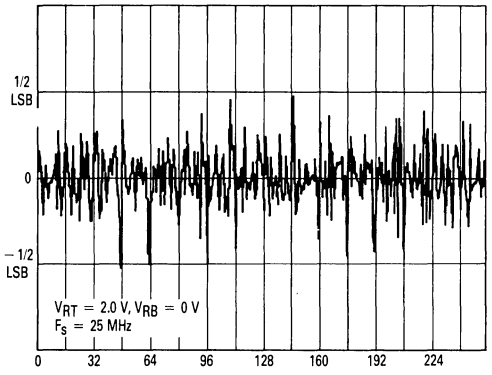


FIGURE 13 — INTEGRAL LINEARITY ERROR

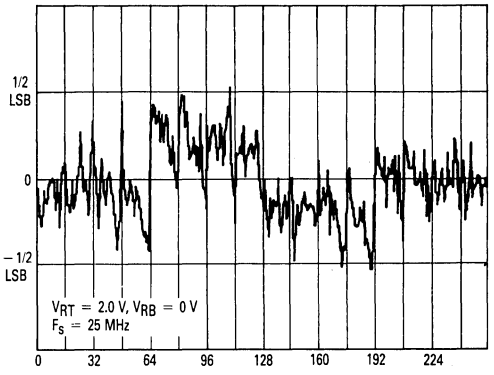


FIGURE 14 — DIFFERENTIAL LINEARITY ERROR

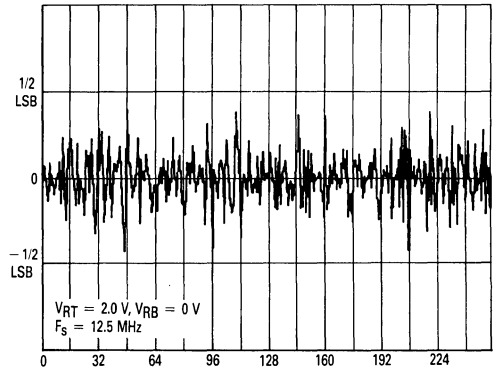
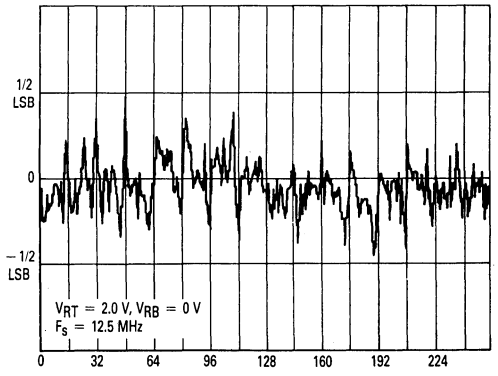


FIGURE 15 — INTEGRAL LINEARITY ERROR



DESIGN GUIDELINES

INTRODUCTION

The MC10319 is a high-speed, 8-bit, parallel ("Flash") type analog-to-digital converter containing 256 comparators at the front end. See Figure 17 for a block diagram. The comparators are arranged such that one input of each is referenced to evenly spaced voltages, derived from the reference resistor ladder. The other input of the comparators is connected to the input signal (V_{in}). Some of the comparator's differential outputs will be "true," while other comparators will have "not true" outputs, depending on their relative position. Their outputs are then latched, and converted to an 8-bit Grey code by the Differential Latch Array. The Grey code ensures any input errors due to cross talk, feed-thru, or timing disparaties, result in glitches at the output of only a few LSBs, rather than the more traditional 1/2 scale and 1/4 scale glitches.

The Grey code is then translated to an 8-bit binary code, and the differential levels are translated to TTL levels before being applied to the output latches. ENABLE inputs at this final stage permit the TTL outputs (except Overrange) to be put into a high impedance (3-state) condition.

6

ANALOG SECTION

SIGNAL INPUT

The signal voltage to be digitized (V_{in}) is applied simultaneously to one input of each of the 256 comparators through Pin 14. The other inputs of the comparators are connected to 256 evenly spaced voltages derived from the reference ladder. The output code depends on the relative position of the input signal and the reference voltages. The comparators have a bandwidth of >50 MHz, which is more than sufficient for the allowable (Nyquist theory) input frequency of 12.5 MHz.

The current into Pin 14 varies linearly from 0 (when $V_{in} = V_{RB}$) to ≈60 μA (when $V_{in} = V_{RT}$). If V_{in} is taken below V_{RB} or above V_{RT}, the input current will remain at the value corresponding to V_{RB} and V_{RT} respectively (see Figure 5). However, V_{in} must be maintained within the absolute range of ±2.5 volts (with respect to ground) — otherwise excessive currents will result at Pin 14, due to internal clamps.

The input capacitance at Pin 14 is typically 36 pF if [$V_{RT} - V_{RB}$] is 2.0 volts, and increases to 55 pF if [$V_{RT} - V_{RB}$] is reduced to 1.0 volt (see Figure 4). The capacitance is constant as V_{in} varies from V_{RT} down to ≈0.1 volt above V_{RB}. Taking V_{in} to V_{RB} will show an increase in the capacitance of ≈50%. If V_{in} is taken above V_{RT}, or below V_{RB}, the capacitance will stay at the values corresponding to V_{RT} and V_{RB}, respectively.

The source impedance of the signal voltage should be maintained below 100 Ω (at the frequencies of interest) in order to avoid sampling errors.

REFERENCE

The reference resistor ladder is composed of a string of equal value resistors so as to provide 256 equally spaced voltages for the comparators (see Figure 17 for the actual configuration). The voltage difference between adjacent comparators corresponds to 1 LSB of the input range. The first comparator (closest to V_{RB}) is referenced 1/2 LSB above V_{RB}, and the 256th comparator (for the overrange) is referenced 1/2 LSB below V_{RT}. The total resistance of the ladder is nominally 130 Ω, ±20%, requiring 15.4 mA @ 2.0 volts, and 7.7 mA @ 1.0 volt. There is a nominal warm-up change of ≈ +9.0% in the ladder resistance due to the +0.29%/°C temperature coefficient.

The minimum recommended span [$V_{RT} - V_{RB}$] is 1.0 volt. A lower span will allow offsets and nonlinearities to become significant. The maximum recommended span is 2.1 volts due to power limitations of the resistor ladder. The span may be anywhere within the range of −2.1 to +2.1 volts with respect to ground, and V_{RB} must be at least 1.3 volts more positive than V_{EE}. The reference voltages must be stable and free of noise and spikes, since the accuracy of a conversion is directly related to the quality of the reference.

In most applications, the reference voltages will remain fixed. In applications involving a varying reference for modulation or signal scrambling, the modulating signal may be applied to V_{RT}, or V_{RB}, or both. The output will vary inversly with the reference signal, introducing a nonlinearity into the transfer function. The addition of the modulating signal and the dc level applied to the reference must be such that the absolute voltage at V_{RT} and V_{RB} are maintained within the values listed in the Recommended Operating Limits. The RMS value of the span must be maintained ≤2.1 volts.

V_{RM} (Pin 1) is the midpoint of the resistor ladder, excluding the Overrange comparator. The voltage at V_{RM} is:

$$\frac{V_{RT} + V_{RB}}{2.0} - 1/2 \text{ LSB}$$

In most applications, bypassing this pin to ground (0.1 μF) is sufficient to maintain accuracy. In applications involving very high frequencies, and where linearity is critical, it may be necessary to trim the voltage at the midpoint. A means for accomplishing this is indicated in Figure 18.

POWER SUPPLIES

$V_{CC(A)}$ is the positive power supply for the comparators, and $V_{CC(D)}$ is the positive power supply for the digital portion. Both are to be +5.0 volts, ±10%, and the two are to be within 100 millivolts of each other. There is indirect internal coupling between $V_{CC(D)}$ and $V_{CC(A)}$. If they are powered separately, and one supply fails, there will be current flow through the MC10319 to the failed supply.

$I_{CC(A)}$ is nominally 17 mA, and does not vary with clock frequency or with V_{in}. It does vary linearly with $V_{CC(A)}$. $I_{CC(D)}$ is nominally 90 mA, and is independent of clock frequency. It does vary, however, by 6–7 mA as V_{in} is changed, with the lowest current occuring when $V_{in} = V_{RT}$. It varies linearly with $V_{CC(D)}$.

V_{EE} is the negative power supply for the comparators, and is to be within the range −3.0 to −6.0 volts. Additionally, V_{EE} must be at least 1.3 volts more negative than V_{RB}. I_{EE} is a nominal −10 mA, and is independent of clock frequency, V_{in}, and V_{EE}.

For proper operation, the supplies **must** be bypassed **at the IC.** A 10 μF tantalum, in parallel with a 0.1 μF ceramic is recommended for each supply to ground.

DIGITAL SECTION

CLOCK

The Clock input is TTL compatible with a typical frequency range of 0 to 30 MHz. There is no duty cycle limitations, but the minimum low and high times must be adhered to. See Figure 7 for the input current requirements.

The conversion sequence is shown in Figure 19, and is as follows:

- On the rising edge, the data output latches are latched with old data, and the comparator output latches are released to follow the input signal (V_{in}).
- During the high time, the comparators track the input signal. The data output latches retain the old data.
- On the falling edge, the comparator outputs are latched with the data immediately prior to this edge. The conversion to digital occurs within the device, and the data output latches are released to indicate the new data within 20 ns.
- During the clock low time, the comparator outputs remain latched, and the data output latches remain transparent.

A summary of the sequence is that data present at V_{in} just prior to the Clock falling edge is digitized and available at the data outputs immediately after that same falling edge.

The comparator output latches provide the circuit with an effective sample-and-hold function, eliminating the need for an external sample-and-hold.

ENABLE INPUTS

The two Enable inputs are TTL compatible, and are used to change the data outputs (D7–D0) from active to 3-state. This capability allows cascading two MC10319s into a 9-bit configuration, flip-flopping two MC10319s into a 50 MHz configuration, connecting the outputs directly to a data bus, multiplexing multiple converters, etc. See the Applications Information section for more details. For the outputs to be active, Pin 19 must be a Logic "1," and Pin 20 must be a Logic "0." Changing either input will put the outputs into the high impedance mode. The Enable inputs affect **only** the state of the outputs — they do not inhibit a conversion. The input current into Pins 19 and 20 is shown in Figure 6, and the input — output timing is shown in Figure 1 and 20. Leaving either pin open is equivalent to a Logic "1," although good design practice dictates that an input should never be left open.

The Overrange output (Pin 3) is not affected by the Enable inputs as it does not have 3-state capability.

OUTPUTS

The data outputs are TTL level outputs with high impedance capabilility. Pin 4 is the MSB (D7), and Pin 21 is the LSB (D0). The eight outputs are active as long as the Enable inputs are true (Pin 19 = high, Pin 20 = low). The timing of the outputs relative to the Clock input and the Enable inputs is shown in Figures 1 and 20. Figures 8 and 9 indicate the output voltage versus load current, while Figure 3 indicates the leakage current when in the high impedance mode.

The output code is natural binary, depicted in the table below.

The Overrange output (Pin 3) goes high when the input, V_{in}, is more positive than V_{RT} − 1/2 LSB. This output is always active — it does not have high impedance capability. Besides being used to indicate an input overrange, it is additionally used for cascading two MC10319s to form a 9-bit A/D converter (see Figure 27).

Input	V_{RT}, V_{RB} (volts)			Output Code	Overrange
	2.048 V, 0 V	+1.0 V, −1.0 V	+1.0 V, 0 V		
$>V_{RT}$ − 1/2 LSB	>2.044 V	>0.9961 V	>0.9980 V	FF_H	1
V_{RT} − 1/2 LSB	2.044 V	0.9961 V	0.9980 V	FF_H	0 ↔ 1
V_{RT} − 1 LSB	2.040 V	0.992 V	0.9961 V	FF_H	0
V_{RT} − 1-1/2 LSB	2.036 V	0.988 V	0.9941 V	$FE_H \leftrightarrow FF_H$	0
Midpoint	1.024 V	0.000 V	0.5000 V	80_H	0
V_{RB} + 1/2 LSB	4.0 mV	−0.9961 V	1.95 mV	$00_H \leftrightarrow 01_H$	0
$<V_{RB}$	<0 V	<−1.0 V	<0 V	00_H	0

APPLICATIONS INFORMATION

POWER SUPPLIES, GROUNDING

The PC board layout, and the quality of the power supplies and the ground system **at the IC** are very important in order to obtain proper operation. Noise, from any source, coming into the device on V_{CC}, V_{EE}, or ground can cause an incorrect output code due to interaction with the analog portion of the circuit. At the same time, noise generated within the MC10319 can cause incorrect operation if that noise does not have a clear path to ac ground.

Both the V_{CC} and V_{EE} power supplies must be decoupled to ground **at the IC** (within 1" max) with a 10 μF tantalum and a 0.1 μF ceramic. Tantalum capacitors are recommended since electrolytic capacitors simply have too much inductance at the frequencies of interest. The quality of the V_{CC} and V_{EE} supplies should then be checked at the IC with a high frequency scope. Noise spikes (always present when digital circuits are present) can easily exceed 400 mV peak, and if they get into the analog portion of the IC, the operation can be disrupted. Noise can be reduced by inserting resistors and/or inductors between the supplies and the IC.

If switching power supplies are used, there will usually be spikes of 0.5 volts or greater at frequencies of 50–200 kHz. These spikes are generally more difficult to reduce because of their greater energy content. In extreme cases, 3-terminal regulators (MC78L05ACP, MC7905.2CT), with appropriate high frequency filtering, should be used and dedicated to the MC10319.

The ripple content of the supplies should not allow their magnitude to exceed the values in the Recommended Operating Limits.

The PC board tracks supplying V_{CC} and V_{EE} to the MC10319 should preferably not be at the tail end of the bus distribution, after passing through a maze of digital circuitry. The MC10319 should be close to the power supply, or the connector where the supply voltages enter the board. If the V_{CC} and V_{EE} lines are supplying considerable current to other parts of the boards, then it is preferable to have dedicated lines from the supply or connector directly to the MC10319.

The four ground pins (2, 12, 16, 22) must be connected directly together. Any long path beween them can cause stability problems due to the inductance (@25 MHz) of the PC tracks. The ground return for the signal source must be noise free.

REFERENCE VOLTAGE CIRCUITS

Since the accuracy of the conversion is directly related to the quality of the references, it is imperative that accurate and stable voltages be provided to V_{RT} and V_{RB}. If the reference span is 2 volts, then 1/2 LSB is only 3.9 millivolts, and it is desireable that V_{RT} and V_{RB} be accurate to within this amount, and furthermore, that they do not drift more than this amount once set. Over the temperature range of 0 to 70°C, a maximum temperature coefficient of 28 ppm/°C is required.

The voltage supplies used for digital circuits should preferably **not** be used as a source for generating V_{RT} and V_{RB}, due to the noise spikes (50–400 mV) present on the supplies and on their ground lines. Generally $\pm$15 volts, or $\pm$12 volts, are available for analog circuits, and are usually clean compared to supplies used for digital circuits, although ripple may be present in varying amounts. Ripple is easier to filter out than spikes, however, and so these supplies are preferred.

Figure 21 depicts a circuit which can provide an extremely stable voltage to V_{RT} **at the current required** (the maximum reference current is 19.2 mA @ 2.0 volts). The MC1403 series of reference sources has very low temperature coefficients, good noise rejection, and a high initial accuracy, allowing the circuit to be built without an adjustment pot if the V_{RT} voltage is to remain fixed at one value. Using 0.1% wirewound resistors for the divider provides sufficient accuracy and stability in many cases. Alternately, resistor networks provide high ratio accuracies, and close temperature tracking. If the application requires V_{RT} to be changed periodically, the two resistors can be replaced with a 20 turn, cermet potentiometer. Wirewound potentiometers should not be used for this type of application since the pot's slider jumps from winding to winding, and an exact setting can be difficult to obtain. Cermet pots allow for a smooth continuous adjustment.

In Figure 21, R1 reduces the power dissipation in the transistor, and can be carbon composition. The 0.1 μF capacitor in the feedback path provides stability in the unity gain configuration. Recommended op amps are: LM358, MC34001 series, LM308A, LM324, and LM11C. Offset drift is the key parameter to consider in choosing an op amp, and the LM308A has the lowest drift of those mentioned. Bypass capacitors are not shown in Figure 21, but should always be provided at the input to the 2.5 volt reference, and at the power supply pins of the op amp.

Figure 22 shows a simpler and more economical circuit, using the LM317LZ regulator, but with lower initial accuracy and temperature stability. The op amp/current booster is not needed since the LM317LZ can supply the current directly. In a well controlled environment, this circuit will suffice for many applications. Because of the lower initial accuracy, an adjustment pot is a necessity.

Figure 23 shows two circuits for providing the voltage to V_{RB}. The circuits are similar to those of Figures 21 and 22, and have similar accuracy and stability. The output transistor is a PNP in this case since the circuit must sink the reference current.

VIDEO APPLICATIONS

The MC10319 is suitable for digitizing video signals directly without signal conditioning, although the standard 1 volt p-p video signal can be amplified to a 2.0 volt p-p signal for slightly better accuracy. Figure 24 shows the input (top trace) and reconstructed output of a standard NTSC test signal, sampled at 25 MSPS, consisting of a sync pulse, 3.58 MHz color burst, a 3.58 MHz signal in a Sin^2x envelope, a pulse, a white level signal, and a black level signal. Figure 25 shows a Sin^2x pulse that has been digitized and reconstructed at 25 MSPS. The width of the pulse is ≈450 ns at the base. Figure 26 shows an application circuit for digitizing video.

9-BIT A/D CONVERTER

Figure 27 shows how two MC10319s can be connected to form a 9-bit converter. In this configuration, the outputs (D7–D0) of the two 8-bit converters are paralleled. The outputs of one device are active, while the outputs of other are in the 3-state mode. The selection is made by the Overrange output of the lower MC10319, which controls Enable inputs on the two devices. Additionally, this output provides the 9th bit.

The reference ladders are connected in series, providing the 512 steps required for 9 bits. The input voltage range is determined by V_{RT} of the upper MC10319, and V_{RB} of the lower device. A minimum of 1.0 volt is required across each converter. The 500 Ω pot (20 turn cermet) allows for adjustment of the midpoint since the reference resistors of the two MC10319s may not be identical in value. Without the adjustment, a non-equal voltage division would occur, resulting in a nonlinear conversion. If the references are to be symmetrical about ground (e.g., ±1.0 volt), the adjustment can be eliminated, and the midpoint connected to ground.

The use of latches on the outputs is optional, depending on the application.

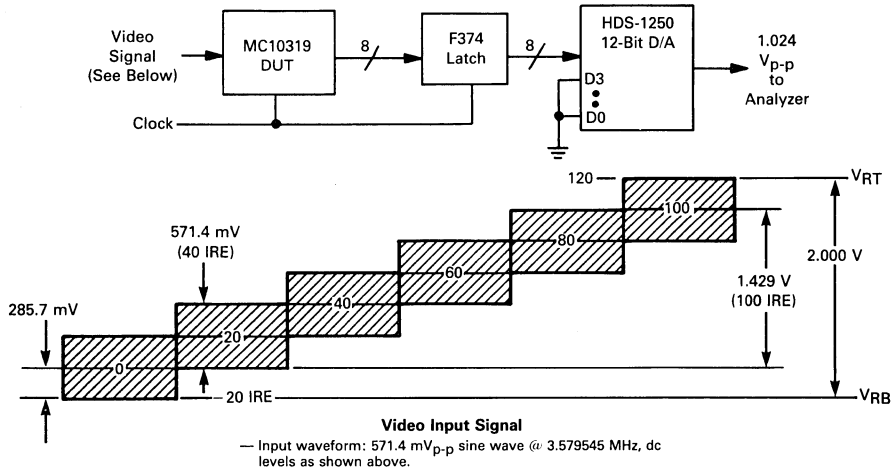
50 MHz, 8-BIT A/D CONVERTER

Figure 28 shows how two MC10319s can be connected together in a flip-flop arrangement in order to have an effective conversion speed of 50 MHz. The 74F74 D-type flip-flop provides a 25 MHz clock to each converter, and at the same time, controls the ENABLES so as to alternately enable and disable the outputs. The Overranges do not have 3-state capability, and so cannot be paralleled. Instead they are OR'd together. The use of latches is optional, and depends on the application. Data should be latched, or written to RAM (in a DMA operation), on the high-to-low transition of the 50 MHz clock.

NEGATIVE VOLTAGE REGULATOR

In the cases where a negative power supply is not available — neither the −3.0 to −6.0 volts, nor a higher negative voltage from which to derive it — the circuit of Figure 29 can be used to generate −5.0 volts from the +5.0 volts supply. The PC board space required is small (≈2.0 in^2), and it can be located physically close to the MC10319. The MC34063 is a switching regulator, and in Figure 29 is configured in an inverting mode of operation. The regulator operating specifications are also given.

FIGURE 16 — DIFFERENTIAL PHASE AND GAIN TEST



Video Input Signal

— Input waveform: 571.4 mV_{p-p} sine wave @ 3.579545 MHz, dc levels as shown above.
— MC10319 clock at 14.31818 MHz (4x) asynchronous to input.
— Differential gain: p-p output @ each IRE level compared to that at 0 IRE.
— Differential phase: Phase @ each IRE level compared to that @ 0 IRE.

FIGURE 17 — MC10319

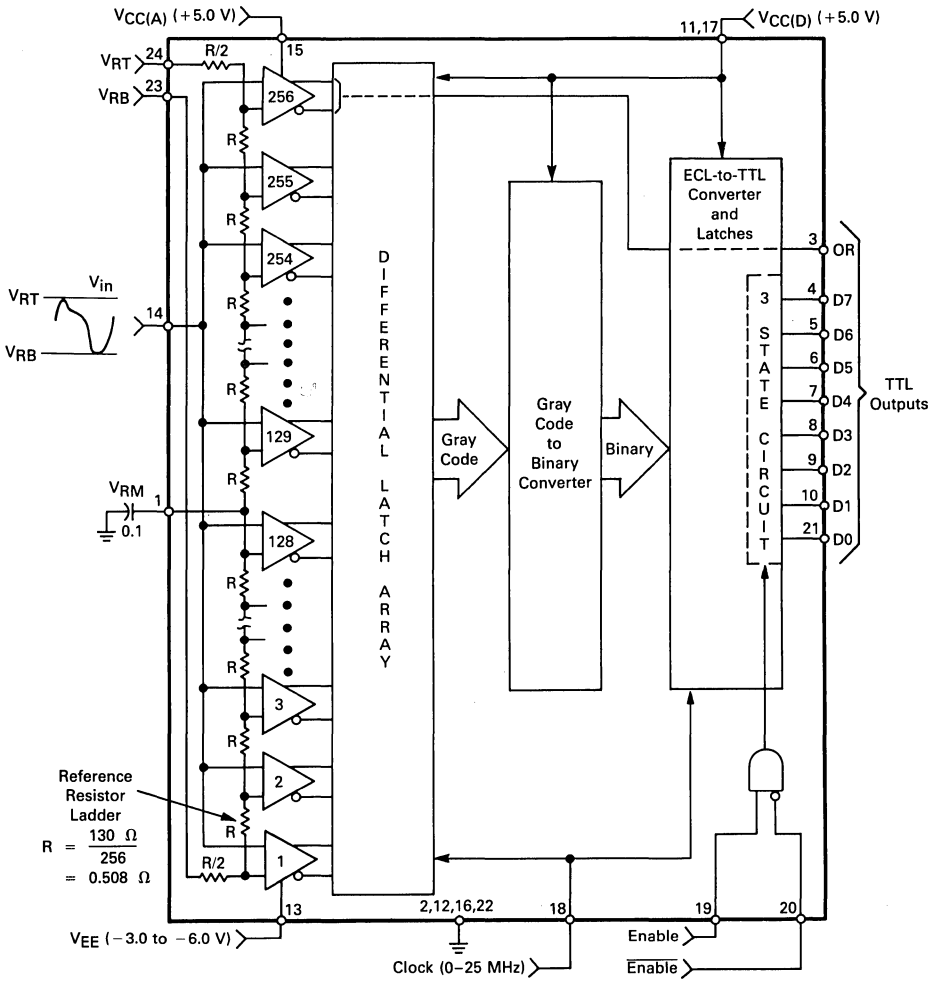


FIGURE 18 — ADJUSTING V_{RM} FOR IMPROVED LINEARITY

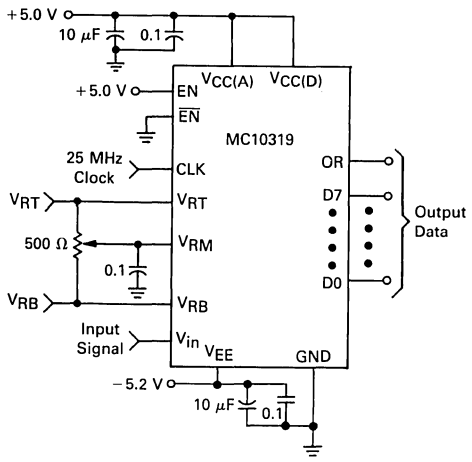


FIGURE 19 — CONVERSION SEQUENCE

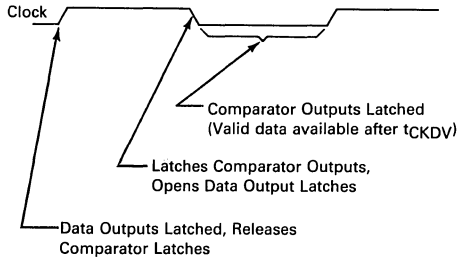
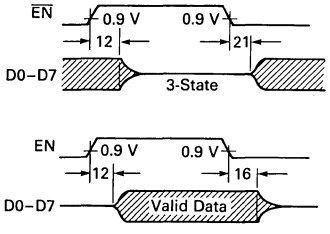


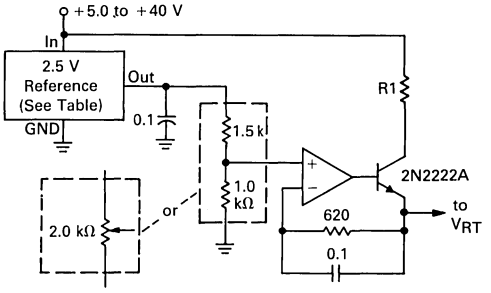
FIGURE 20 — ENABLE TO OUTPUT CRITICAL TIMING



Timing @ D7–D0 measured where waveform starts to change.
Indicated time values are typical @ 25°C, and are in ns.

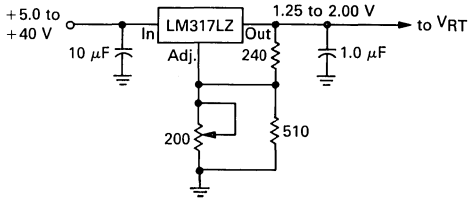
FIGURE 21 — PRECISION V_{RT} VOLTAGE SOURCE

R1 = 100 Ω for +5.0 V
620 Ω for +15 V



2.5 V References	MC1403U	MC1403AU
Line Regulation	0.5 mV	0.5 mV
T_C (ppm/°C) max	40	25
ΔV_{out} for 0–70°C	7.0 mV	4.4 mV
Initial Accuracy	±1%	±1%

FIGURE 22 — V_{RT}, VOLTAGE SOURCE



LM317LZ	
Line Regulation	1.0 mV
T_C (ppm/°C) max	60
ΔV_{out} for 0–70°C	8.4 mV
Initial Accuracy	±4%

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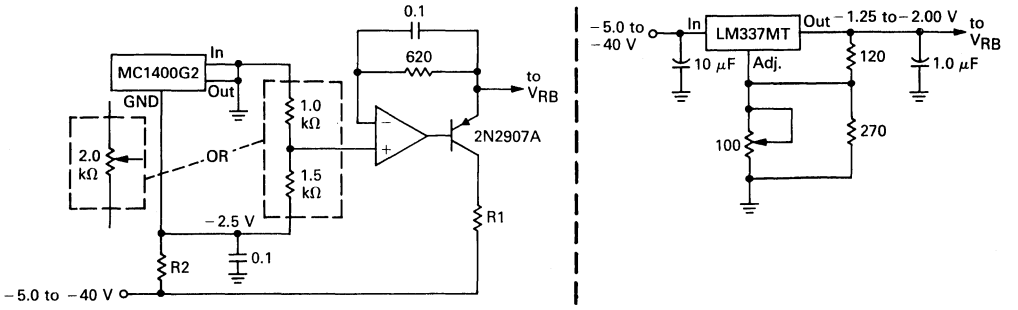
FIGURE 23 — V_{RB} VOLTAGE SOURCES



	MC1400G2	LM337MT
Line Regulation	1.0 mV	1.0 mV
T_C (ppm/°C) max	25	48
ΔV_{out} for 0–70°C	4.4 mV	6.7 mV
Initial Accuracy	±0.2%	±4%

R1 = 100 Ω for −5.0 V
620 Ω for −15 V
R2 = 620 Ω for −5.0 V
3.0 kΩ for −15 V

6

FIGURE 24 — COMPOSITE VIDEO WAVEFORM

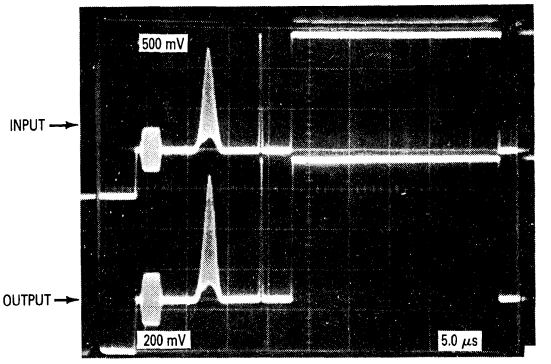


FIGURE 25 — SIN^2 X WAVEFORM

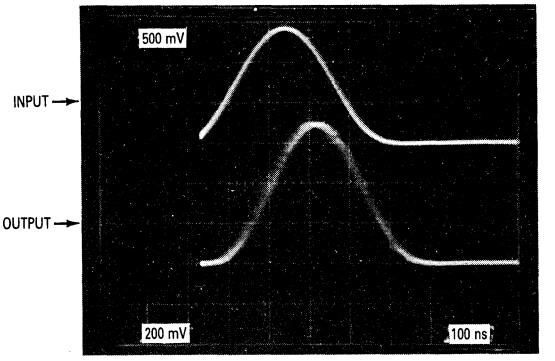
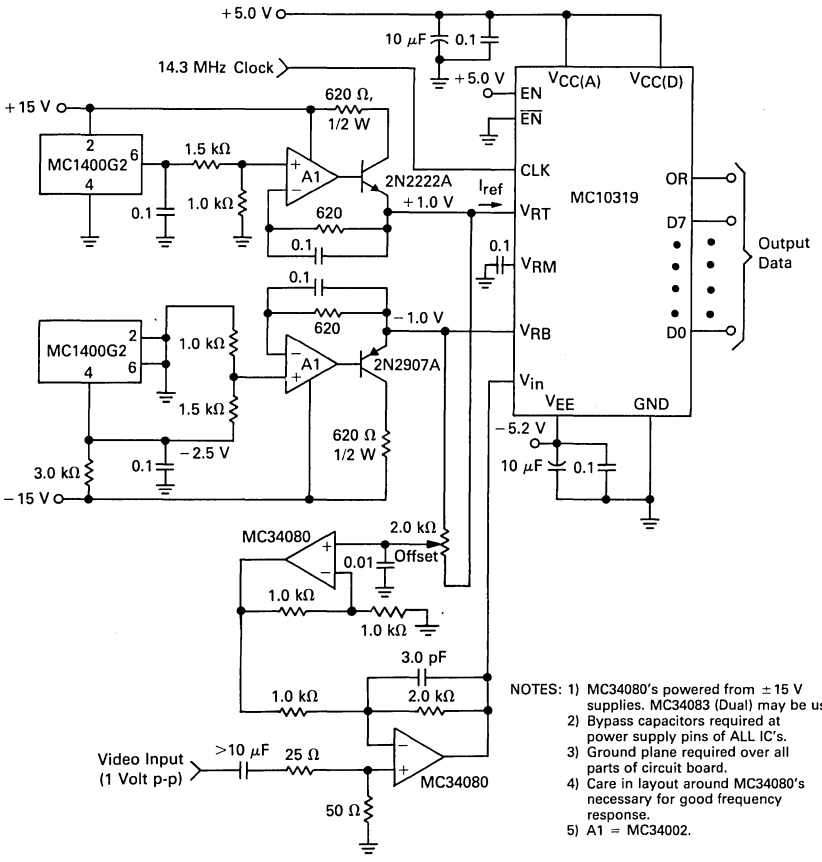


FIGURE 26 — APPLICATION CIRCUIT FOR DIGITIZING VIDEO



NOTES: 1) MC34080's powered from ±15 V supplies. MC34083 (Dual) may be used.
2) Bypass capacitors required at power supply pins of ALL IC's.
3) Ground plane required over all parts of circuit board.
4) Care in layout around MC34080's necessary for good frequency response.
5) A1 = MC34002.

6

FIGURE 27 — 9-BIT A/D CONVERTER

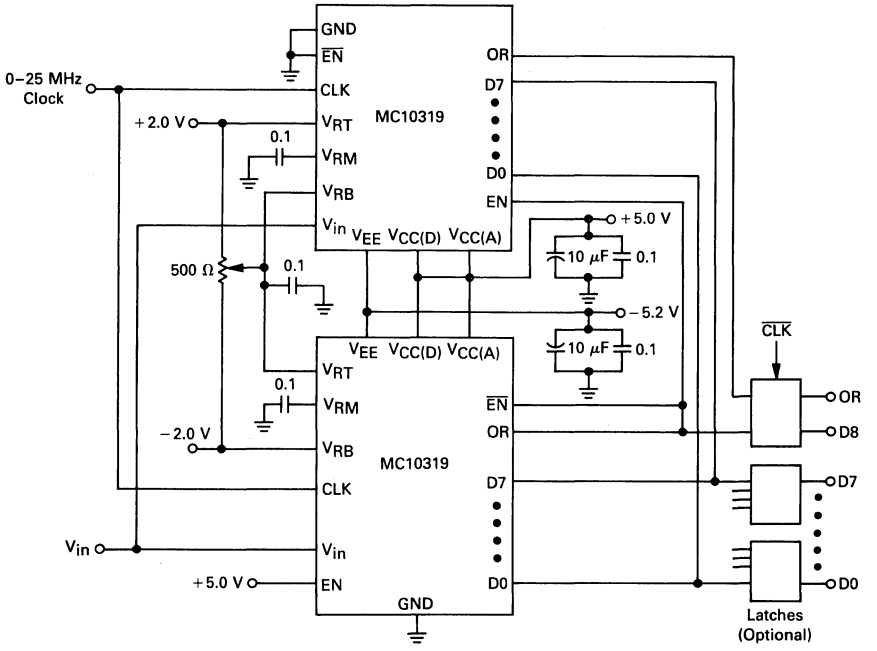


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FIGURE 28 — 50 MHz 8-BIT A/D CONVERTER

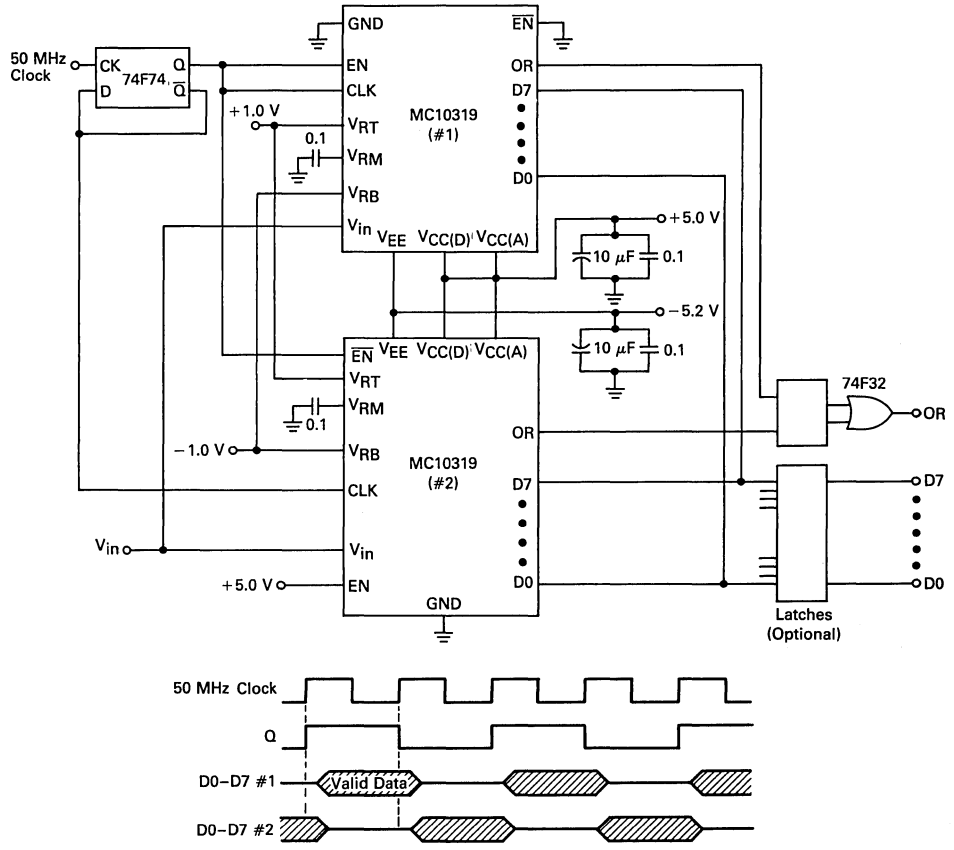
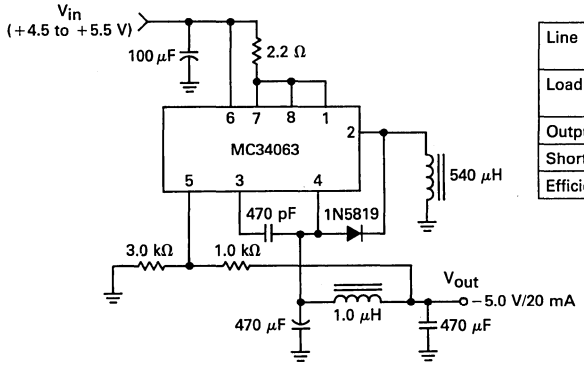


FIGURE 29 — −5.0 VOLT REGULATOR



Line Regulation	4.5 V < V_{in} < 5.5 V, I_{out} = 10 mA	0.16%
Load Regulation	V_{in} = 5.0 V, 8.0 mA < I_{out} < 20 mA	0.4%
Output Ripple	V_{in} = 5.0 V, I_{out} = 20 mA	2 mV_{p-p}
Short Circuit I_{out}	V_{in} = 5.0 V, R1 = 0.1 Ω	140 mA
Efficiency	V_{in} = 5.0 V, I_{out} = 50 mA	52%

GLOSSARY

APERTURE DELAY — The time difference between the sampling signal (typically a clock edge) and the actual analog signal converted. The actual signal converted may occur before or after the sampling signal, depending on the internal configuration of the converter.

BIPOLAR INPUT — A mode of operation whereby the analog input (of an A-D), or output (of a DAC), includes both negative and positive values. Examples are −1.0 to +1.0 V, −5.0 to +5.0 V, −2.0 to +8.0 V, etc.

BIPOLAR OFFSET ERROR — The difference between the actual and ideal locations of the 00_H to 01_H transition, where the ideal location is 1/2 LSB above the most negative reference voltage.

BIPOLAR ZERO ERROR — The error (usually expressed in LSBs) of the input voltage location (of an A-D) of the 80_H to 81_H transition. The ideal location is 1/2 LSB above zero volts in the case of an A-D setup for a symmetrical bipolar input (e.g., −1.0 to +1.0 V).

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DIFFERENTIAL NONLINEARITY — The maximum deviation in the actual step size (one transition level to another) from the ideal step size. The ideal step size is defined as the Full Scale Range divided by 2^n (n = number of bits). This error must be within ±1 LSB for proper operation.

ECL — Emitter coupled logic.

FULL SCALE RANGE (ACTUAL) — The difference between the actual minimum and maximum end points of the analog input (of an A-D).

FULL SCALE RANGE (IDEAL) — The difference between the actual minimum and maximum end points of the analog input (of an A-D), plus one LSB.

GAIN ERROR — The difference between the actual and expected gain (end point to end point), with respect to the reference, of a data converter. The gain error is usually expressed in LSBs.

GREY CODE — Also known as *reflected binary code,* it is a digital code such that each code differs from adjacent codes by only one bit. Since more than one bit is never changed at each transition, race condition errors are eliminated.

INTEGRAL NONLINEARITY — The maximum error of an A-D, or DAC, transfer function from the ideal straight line connecting the analog end points. This parameter is sensitive to dynamics, and test conditions must be specified in order to be meaningfull. This parameter is the best overall indicator of the device's performance.

LSB — Least Significant Bit. It is the lowest order bit of a binary code.

LINE REGULATION — The ability of a voltage regulator to maintain a certain output voltage as the input to the regulator is varied. The error is typically expressed as a percent of the nominal output voltage.

LOAD REGULATION — The ability of a voltage regulator to maintain a certain output voltage as the load current is varied. The error is typically expressed as a percent of the nominal output voltage.

MONOTONICITY — The characteristic of the transfer function whereby increasing the input code (of a DAC), or the input signal (of an A-D), results in the output never decreasing.

MSB — Most Significant Bit. It is the highest order bit of a binary code.

NATURAL BINARY CODE — A binary code defined by:

$$N = A_n2^n + \ldots + A_32^3 + A_22^2 + A_12^1 + A_02^0$$

where each "A" coefficient has a value of 1 or 0. Typically, all zeroes correspond to a zero input voltage of an A-D, and all ones correspond to the most positive input voltage.

NYQUIST THEORY — See Sampling Theorem.

OFFSET BINARY CODE — Applicable only to bipolar input (or output) data converters, it is the same as Natural Binary, except that all zeroes correspond to the most negative input voltage (of an A-D), while all ones correspond to the most positive input.

POWER SUPPLY SENSITIVITY — The change in a data converter's performance with changes in the power supply voltage(s). This parameter is usually expressed in percent of full scale versus ΔV.

QUANTITIZATION ERROR — Also known as digitization error or uncertainty. It is the inherent error involved in digitizing an analog signal due to the finite number of steps at the digital output versus the infinite number of values at the analog input. This error is a minimum of ±1/2 LSB.

RESOLUTION — The smallest change which can be discerned by an A-D converter, or produced by a DAC. It is usually expressed as the number of bits, n, where the converter has 2^n possible states.

SAMPLING THEOREM — Also known as the Nyquist Theorem. It states that the sampling frequency of an A-D must be no less than 2x the highest frequency (of interest) of the analog signal to be digitized in order to preserve the information of that analog signal.

UNIPOLAR INPUT — A mode of operation whereby the analog input range (of an A-D), or output range (of a DAC), includes values of a signal polarity. Examples are 0 to +2.0 V, 0 to −5.0 V, +2.0 to +8.0 V, etc.

UNIPOLAR OFFSET ERROR — The difference between the actual and ideal locations of the 00_H to 01_H transition, where the ideal location is 1/2 LSB above the most negative input voltage.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC10321

HIGH SPEED 7-BIT ANALOG-TO-DIGITAL FLASH CONVERTER

The MC10321 is a 7-bit high speed parallel flash A/D converter, which employs an internal Grey Code structure to eliminate large output errors on fast slewing input signals. It is fully TTL compatible, requiring a +5.0 volt supply, and a negative supply between −3.0 and −6.0 volts. Three-state TTL outputs allow direct connection to a data bus or common I/O memory.

The MC10321 contains 128 parallel comparators wired along a precision input reference network. The comparator outputs are fed to latches, and then to an encoder network which produces a 7-bit data byte, plus an overrange bit. The data is latched and converted to three-state LSTTL levels. Enable inputs permit setting the outputs to a three-state condition. The overrange bit is always active to allow for sensing of the overrange condition, and to ease the interconnection of two MC10321s into an 8-bit configuration.

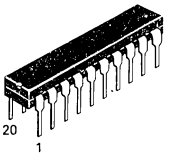
The MC10321 is available in a 20-pin standard plastic and SOIC packages.

Applications include Video displays (digital TV, picture-in-picture, special effects), radar processing, high speed instrumentation, and TV broadcast.

- Internal Grey Code for Speed and Accuracy
- 25 MHz Sampling Rate
- 7-Bit Resolution with 8-Bit Accuracy
- Easily Cascadable into an 8-Bit System
- Three-State LSTTL Outputs with True and Complement Enable Inputs
- Low Input Capacitance: 25 pF
- No Clock Kick-Out Currents on Input or Reference
- Wide Input Range: 1.0–2.1 Volts within a ±2.1 Volt Range
- No Sample and Hold Required for Video Applications
- Edge Triggered Conversion — No Pipeline Delay
- True and Complement Enable Inputs for Three-State Control
- Standard DIP and Surface Mount Packages Available
- Operating Temperature Range: −40° to +85°C

HIGH SPEED 7-BIT ANALOG-TO-DIGITAL FLASH CONVERTER

SILICON MONOLITHIC INTEGRATED CIRCUIT

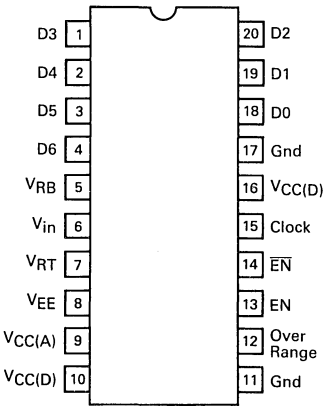


P SUFFIX
PLASTIC PACKAGE
CASE 738

DW SUFFIX
PLASTIC PACKAGE
CASE 751D
(SO-20)

PIN CONNECTIONS

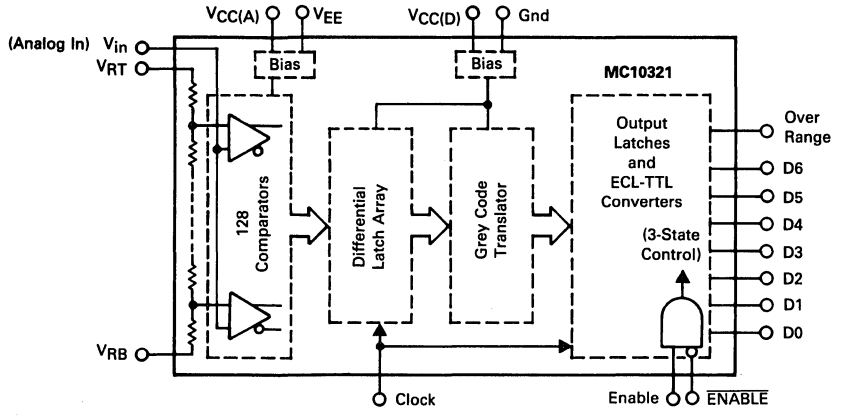
(Top View)



ORDERING INFORMATION

Device	Temperature Range	Package
MC10321P	−40° to +85°C	Plastic DIP
MC10321DW		SO-20

BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Units
Supply Voltage	$V_{CC(A)}$, $V_{CC(D)}$ V_{EE}	+7.0 −7.0	Vdc
Positive Supply Voltage Differential	$V_{CC(D)}-V_{CC(A)}$	−0.3, +0.3	Vdc
Digital Input Voltage (Pins 13–15)	$V_{I(D)}$	−0.5, +7.0	Vdc
Analog Input Voltage (Pins 5, 6, 7)	$V_{I(A)}$	−2.5, +2.5	Vdc
Reference Voltage Span (Pin 7–Pin 5)	—	+2.3	Vdc
Applied Output Voltage (D0–D6 in 3-State)	—	−0.3, +7.0	Vdc
Junction Temperature	T_J	+150	°C
Storage Temperature	T_{stg}	−65, +150	°C

Devices should not be operated at these values. The "Recommended Operating Limits" provide guidelines for actual device operation.

RECOMMENDED OPERATING LIMITS

Parameter	Symbol	Min	Typ	Max	Units
Power Supply Voltage (Pin 9) Power Supply Voltage (Pins 10, 16) $V_{CC(D)}-V_{CC(A)}$	$V_{CC(A)}$ $V_{CC(D)}$ ΔV_{CC}	+4.5 +4.5 −0.1	+5.0 +5.0 0	+5.5 +5.5 +0.1	Vdc
Power Supply Voltage (Pin 8)	V_{EE}	−6.0	−5.0	−3.0	Vdc
Digital Input Voltages (Pins 13–15)	—	0	—	$V_{CC(D)}$	Vdc
Analog Input (Pin 6)	V_{in}	−2.1	—	+2.1	Vdc
Voltage @ V_{RT} (Pin 7) @ V_{RB} (Pin 5) $V_{RT}-V_{RB}$ $V_{RB}-V_{EE}$	V_{RT} V_{RB} ΔV_R —	−1.0 −2.1 +1.0 1.3	— — — —	+2.1 +1.0 +2.1 —	Vdc
Applied Output Voltage (Pins D0–D6 in 3-State)	V_O	0	—	$V_{CC(D)}$	Vdc
Clock Pulse Width — High — Low	t_{CKH} t_{CKL}	5.0 15	— —	— —	ns
Clock Frequency	f_{CLK}	0	—	25	MHz
Operating Ambient Temperature	T_A	−40	—	+85	°C

All limits are not necessarily functional concurrently.

ELECTRICAL CHARACTERISTICS (T_A = +25°C, V_{CC} = 5.0 V, V_{EE} = −5.2 V, V_{RT} = +1.0 V, V_{RB} = −1.0 V, except where noted)

Characteristic	Symbol	Min	Typ	Max	Units
TRANSFER CHARACTERISTICS (f_{CKL} = 25 MHz)					
Resolution	N	—	—	7.0	Bits
Monotonicity	MON		Guaranteed		Bits
Integral Nonlinearity Differential Nonlinearity	INL DNL	— —	±1/4 —	±1.0 ±1.0	LSB
Differential Phase (See Figure 11) Differential Gain (See Figure 11)	DP DG	— —	2.0 2.0	— —	Deg. %
Power Supply Rejection Ratio (4.5 V < V_{CC} < 5.5 V, V_{EE} = −5.2 V) (−6.0 V < V_{EE} < −3.0 V, V_{CC} = +5.0 V)	PSRR	 — —	 0.02 0	 — —	LSB/V
ANALOG INPUT (Pin 6)					
Input Current @ V_{in} = V_{RB} − 0.1 V (See Figure 4) @ V_{in} = V_{RT} + 0.1 V (See Figure 4)	I_{INL} I_{INH}	— —	+1.0 +60	+5.0 +150	μA
Input Capacitance (1.0 V < (V_{RT} − V_{RB}) < 2.0 V)	C_{in}	—	22	—	pF
Bipolar Offset Error	V_{OS}	—	0.1	—	LSB
REFERENCE					
Ladder Resistance (V_{RT} to V_{RB}, T_A = 25°C)	R_{ref}	100	140	175	Ω
Temperature Coefficient	T_C	—	+0.29	—	%/°C
Ladder Capacitance (Pin 1 Open)	C_{ref}	—	5.0	—	pF
ENABLE INPUTS (V_{CC} = 5.5 V)					
Input Voltage — High — Low	V_{IHE} V_{ILE}	2.0 —	— —	— 0.8	V
Input Current @ 2.4 Volts (See Figure 5) @ 0.4 Volts (See Figure 5)	I_{IHE} I_{ILE}	— −200	+0.2 −120	2.0 —	μA
Input Clamp Voltage (I_{IK} = −18 mA)	V_{IKE}	−1.5	−1.3	—	V
CLOCK INPUT (V_{CC} = 5.5 V)					
Input Voltage — High — Low	V_{IHC} V_{ILC}	2.0 —	— —	— 0.8	Vdc
Input Current @ 0.4 V (See Figure 6) @ 2.7 V (See Figure 6)	I_{ILC} I_{IHC}	−150 −80	−80 −40	— —	μA
Input Clamp Voltage (I_{IK} = −18 mA)	V_{IKC}	−1.5	−1.3	—	Vdc
DIGITAL OUTPUTS					
High Output Voltage (I_{OH} = −400 μA @ D6–D0, OR, V_{CC} = 4.5 V, See Figure 7)	V_{OH}	2.4	3.0	—	V
Low Output Voltage (I_{OL} = 4.0 mA @ D6–D0, OR, V_{CC} = 4.5 V, See Figure 8)	V_{OL}	—	0.3	0.4	V
Output Short Circuit Current* (D6–D0, OR, V_{CC} = 5.5 V)	I_{SC}	—	−35	—	mA
Output Leakage Current (0.4 < V_O < 2.4 V, See Figure 3, V_{CC} = 5.5 V, D0–D6 in 3-State Mode)	I_{LK}	−10	—	+10	μA
Output Capacitance (D0–D6 in 3-State Mode)	C_{out}	—	5.0	—	pF

*Only one output to be shorted at a time, not to exceed 1 second.

POWER SUPPLIES					
$V_{CC(A)}$ Current (4.5 V < $V_{CC(A)}$ < 5.5 V, Outputs Unloaded) $V_{CC(D)}$ Current (4.5 V < $V_{CC(D)}$ < 5.5 V, Outputs Unloaded) V_{EE} Current (−6.0 V < V_{EE} < −3.0 V)	$I_{CC(A)}$ $I_{CC(D)}$ I_{EE}	10 40 −16	13 60 −13	16 80 −8.0	mA
Power Dissipation (V_{RT} − V_{RB} = 2.0 V, Outputs Unloaded)	P_D	—	459	668	mW

TIMING CHARACTERISTICS (T_A = 25°C, V_{CC} = +5.0 V, V_{EE} = −5.2 V, V_{RT} = +1.0 V, V_{RB} = −1.0 V, See System Timing Diagram)

Parameter	Symbol	Min	Typ	Max	Units
INPUTS					
Min Clock Pulse Width — High — Low	t_{CKH} t_{CKL}	— —	5.0 15	— —	ns
Max Clock Rise, Fall Time	$t_{R,F}$	—	100	—	ns
Clock Frequency	f_{CLK}	0	30	25	MHz
OUTPUTS					
New Data Valid from Clock Low	t_{CKDV}	—	22	—	ns
Aperture Delay	t_{AD}	—	3.0	—	ns
Hold Time	t_H	—	6.0	—	ns
Data High to 3-State from Enable Low*	t_{EHZ}	—	22	—	ns
Data Low to 3-State from Enable Low*	t_{ELZ}	—	17	—	ns
Data High to 3-State from $\overline{\text{ENABLE}}$ High*	$t_{E'HZ}$	—	27	—	ns
Data Low to 3-State from $\overline{\text{ENABLE}}$ High*	$t_{E'LZ}$	—	19	—	ns
Valid Data from Enable High (Pin 14 = 0 V)*	t_{EDV}	—	13	—	ns
Valid Data from $\overline{\text{ENABLE}}$ Low (Pin 13 = 5.0 V)*	$t_{E'DV}$	—	20	—	ns
Output Transition Time (10%–90%)*	t_{tr}	—	6.0	—	ns

*See Figure 2 for output loading.

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TEMPERATURE CHARACTERISTICS

Parameter	Typical Value @ 25°C	Typical Change −40 to +85°C
I_{CC} (+5.0 V Supply Current)	73 mA	−100 μA/°C
I_{EE} (−5.2 V Supply Current)	−13 mA	+7.0 μA/°C
Ladder Resistance	140 Ω	+0.29%/°C
V_{OL} (Output Low Voltage @ 4.0 mA)	0.3 V	+8.0 μV/°C
V_{OH} (Output High Voltage @ −400 μA)	3.0 V	2.1 mV/°C
Differential Nonlinearity	—	−0.0008 LSB/°C
Integral Nonlinearity	0.25 LSB	−0.001 LSB/°C

PIN DESCRIPTIONS

Symbol	Pin	Description
GND	11,17	Power supply ground. The two pins should be connected directly together, and through a low impedance path to the power supply.
OR	12	Overrange output. Indicates V_{in} is more positive than V_{RT}-1/2 LSB. This output does not have 3-state capability, and therefore is always active.
D6–D0	1–4, 18–20	Digital Outputs. D6 (Pin 4) is the MSB, D0 (Pin 18) is the LSB. LSTTL compatible with 3-state capability.
$V_{CC(D)}$	10,16	Power supply for the digital section. +5.0 V, ±10% required.
V_{EE}	8	Negative Power supply. Nominally −5.2 V, it can range from −3.0 to −6.0 V, and must be more negative than V_{RB} by >1.3 V.
V_{in}	6	Signal voltage input. This voltage is compared to the reference to generate a digital equivalent. Input impedance is nominally 16–33 kΩ (See Figure 4) in parallel with 22 pF.

PIN DESCRIPTIONS

Symbol	Pin	Description
$V_{CC(A)}$	9	Power supply for the analog section. +5.0 V, ±10% required.
CLK	15	Clock input, TTL compatible, and can range from dc to 25 MHz. Conversion occurs on the negative edge of the clock.
EN	13	Enable input. TTL compatible, a Logic "1" (and Pin 14 a Logic "0") enables the data outputs. A Logic "0" sets the outputs (except Overrange) to a 3-state mode.
$\overline{\text{EN}}$	14	$\overline{\text{ENABLE}}$ input. TTL compatible, a Logic "0" (and Pin 13 a Logic "1") enables the data outputs. A Logic "1" sets the outputs (except Overrange) to a 3-state mode.
V_{RB}	5	The bottom (most negative point) of the internal reference resistor ladder. The ladder resistance is typically 140 Ω to V_{RT}.
V_{RT}	7	The top (most positive point) of the internal reference resistor ladder.

Pin assignments are the same for the standard DIP package and the surface mount package.

FIGURE 1 — SYSTEM TIMING DIAGRAM

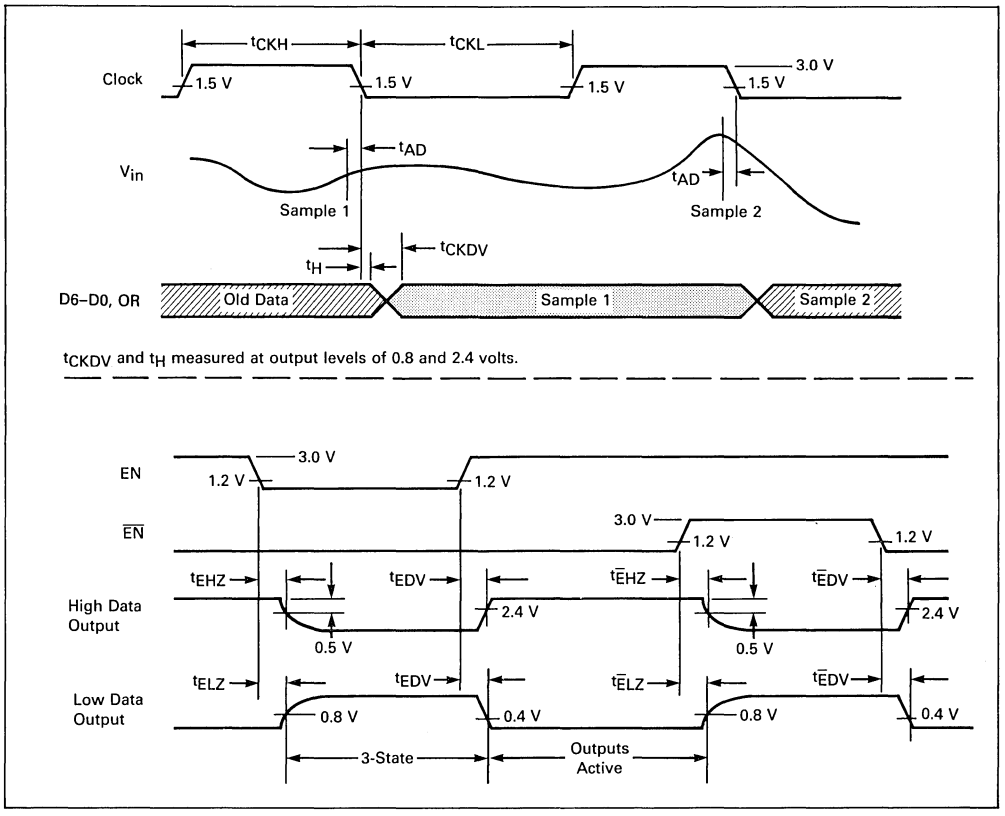


FIGURE 2 — DATA OUTPUT TEST CIRCUIT

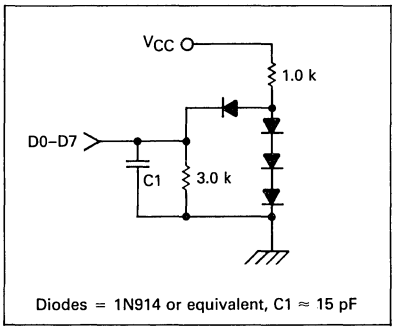


FIGURE 3 — OUTPUT 3-STATE LEAKAGE CURRENT

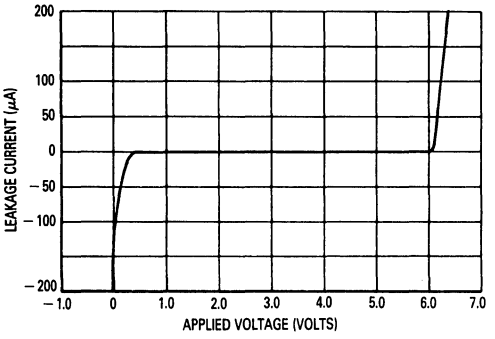


FIGURE 4 — INPUT CURRENT @ V_{in}

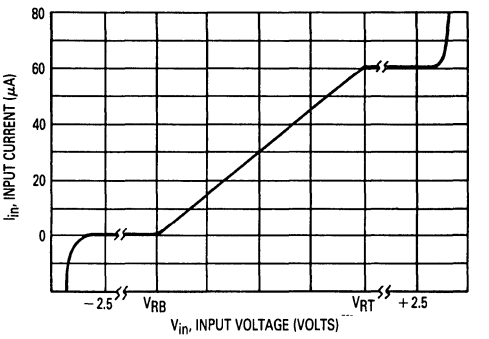


FIGURE 5 — INPUT CURRENT AT ENABLE, $\overline{\text{ENABLE}}$

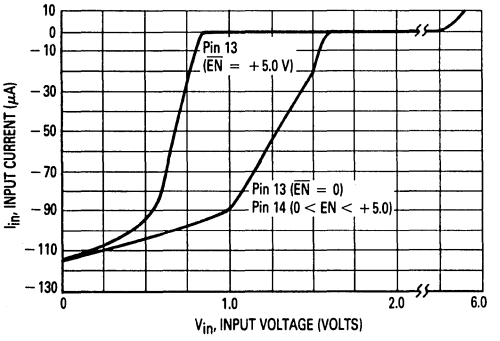


FIGURE 6 — CLOCK INPUT CURRENT

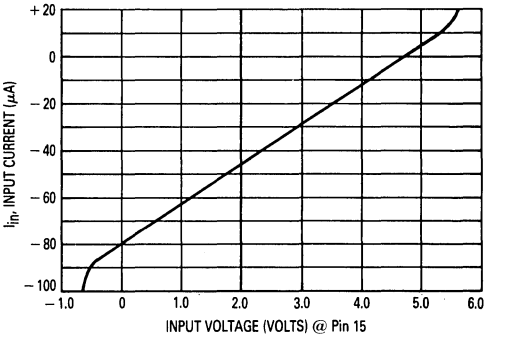


FIGURE 7 — OUTPUT VOLTAGE versus OUTPUT CURRENT

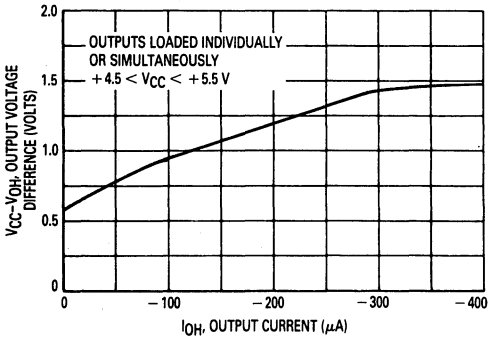


FIGURE 8 — OUTPUT VOLTAGE versus OUTPUT CURRENT

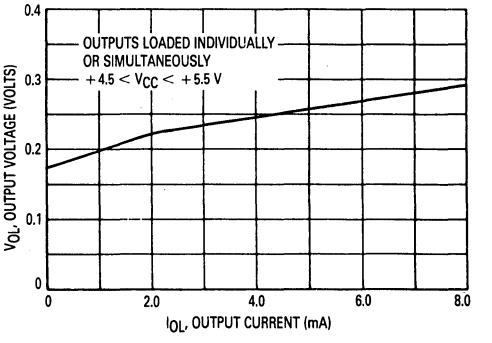


FIGURE 9 — INTEGRAL LINEARITY ERROR IN LSBs versus CODE

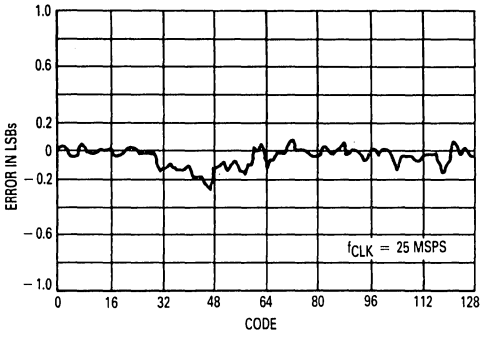
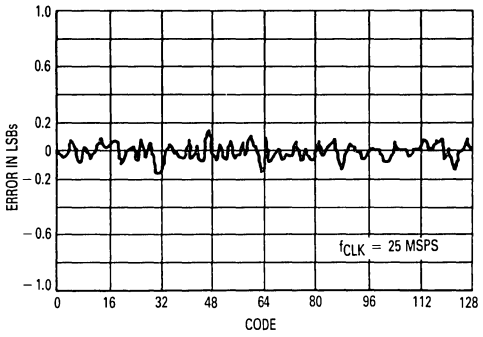


FIGURE 10 — DIFFERENTIAL LINEARITY ERROR IN LSBs versus LOWER CODE



DESIGN GUIDELINES

INTRODUCTION

The MC10321 is a high speed, 7-bit parallel ("Flash") type Analog-to-Digital converter containing 128 comparators at the front end. See Figure 12 for a block diagram. The comparators are arranged such that one input of each is referenced to evenly spaced voltages, derived from the reference resistor ladder. The other input of each of the comparators is connected to the input signal (V_{in}). Some of the comparator's differential outputs will be "true," while other comparators will have "not true" outputs, depending on their relative position. Their outputs are then latched, and converted to a 7-bit Grey code by the Differential Latch Array. The Grey code ensures that errors caused at the input stage, due to cross talk, feed-thru, or timing disparaties, result in glitches at the output of only a few LSBs, rather than the more traditional 1/2 scale and 1/4 scale glitches.

The Grey code is then translated to a 7-bit binary code, and the differential levels are translated to TTL levels before being applied to the output latches. ENABLE inputs (EN and $\overline{EN}$) at this final stage permit the TTL outputs (except Overrange) to be put into a high impedance (3-state) condition.

ANALOG SECTION

SIGNAL INPUT

The signal voltage to be digitized (V_{in}) is applied simultaneously to one input of each of the 128 comparators through Pin 6. The other inputs of the comparators are connected to 128 evenly spaced voltages derived from the reference ladder. The output code depends on the relative position of the input signal to the reference voltages. The comparators have a bandwidth of >50 MHz, which is more than sufficient for the allowable (Nyquist theory) input frequency of 12.5 MHz.

The current into Pin 6 varies linearly from 0 (when $V_{in} = V_{RB}$) to ≈60 μA (when $V_{in} = V_{RT}$). If V_{in} is taken below V_{RB} or above V_{RT}, the input current will remain at the value corresponding to V_{RB} and V_{RT} respectively (see Figure 4). However, V_{in} must be maintained within the absolute range of ±2.5 volts (with respect to ground) — otherwise excessive currents will result at Pin 6.

The input capacitance at Pin 6 is typically 22 pF, and is constant as V_{in} varies from V_{RT} to V_{RB}.

The source impedance of the signal voltage should be maintained below 100 Ω (at the frequencies of interest) in order to avoid sampling errors.

REFERENCE

The reference resistor ladder is composed of a string of equal value resistors so as to provide 128 equally spaced voltages for the comparators (see Figure 12 for the actual configuration). The voltage difference between adjacent comparators corresponds to 1 LSB of the input range. The first comparator (closest to V_{RB}) is referenced 1/2 LSB above V_{RB}, and the 128th comparator (for the overrange) is referenced 1/2 LSB below V_{RT}. The total resistance of the ladder is nominally 140 Ω, ±25%, requiring 14.3 mA @ 2.0 volts and 7.14 mA @ 1.0 volt. There is a nominal warm up change of ≈ +8.0% in the ladder resistance due to the +0.29%/°C temperature coefficient.

The minimum recommended span [$V_{RT} - V_{RB}$] is 1.0 volt. A lower span will allow offsets and nonlinearities to become significant. The maximum recommended span is 2.1 volts due to power limitations of the resistor ladder. The span may be anywhere within the range of −2.1 to +2.1 volts with respect to ground, and V_{RB} must be at least 1.3 volts more positive than V_{EE}. The reference voltages must be stable and free of noise and spikes, since the accuracy of a conversion is directly related to the quality of the reference.

In most applications, the reference voltages will remain fixed. In applications involving a varying reference for modulation or signal scrambling, the modulating signal may be applied to V_{RT}, or V_{RB}, or both. The output will vary inversely with the reference signal, introducing a nonlinearity into the transfer function. The addition of the modulating signal and the dc level

applied to the reference must be such that the absolute voltage at V_{RT} and V_{RB} are maintained within the values listed in the Recommended Operating Limits. The RMS value of the span must be maintained ≤2.1 volts.

POWER SUPPLIES

$V_{CC(A)}$ (Pin 9) is the positive power supply for the comparators, and $V_{CC(D)}$ (Pins 10, 16) is the positive power supply for the digital portion. Both are to be +5.0 volts, ±10%, and the two are to be within 100 millivolts of each other. There is indirect internal coupling between $V_{CC(D)}$ and $V_{CC(A)}$. If they are powered separately, and one supply fails, there will be current flow through the MC10321 to the failed supply.

$I_{CC(A)}$ is nominally 13 mA, and does not vary with clock frequency or with V_{in}, but does vary slightly with $V_{CC(A)}$. $I_{CC(D)}$ is nominally 60 mA, and is independent of clock frequency. It does vary, however, by 4–5 mA as V_{in} is varied from V_{RT} to V_{RB}, and varies directly with $V_{CC(D)}$.

V_{EE} is the negative power supply for the comparators, and is to be within the range −3.0 to −6.0 volts. Additionally, V_{EE} must be at least 1.3 volts more negative than V_{RB}. I_{EE} is a nominal −13 mA, and is independent of clock frequency, V_{in} and V_{EE}.

For proper operation, the supplies **must** be bypassed **at the IC.** A 10 μF tantalum, in parallel with a 0.1 μF ceramic is recommended for each supply to ground.

DIGITAL SECTION

CLOCK

The Clock input (Pin 15) is TTL compatible with a typical frequency range of 0 to 30 MHz. There is no duty cycle limitation, but the minimum low and high times must be adhered to. See Figure 6 for the input current requirements.

The conversion sequence is shown in Figure 13, and is as follows:

— On the rising edge, the data output latches are latched with old data, and the comparator output latches are released to follow the input signal (V_{in}).

— During the high time, the comparators track the input signal. The data output latches retain the old data.

— On the falling edge, the comparator outputs are latched with the data immediately prior to this edge. The conversion to digital occurs within the device, and the data output latches are released to indicate the new data in ≈22 ns.

— During the clock low time, the comparator outputs remain latched, and the data output latches remain transparent.

A summary of the sequence is that data present at V_{in} just prior to the Clock falling edge is digitized and available at the data outputs immediately after that same falling edge. The minimum amount of time the data must be present prior to the clock falling edge (aperture delay) is 2.0–6.0 ns, typically 3.0 ns.

The comparator output latches provide the circuit with an effective sample-and-hold function, eliminating the need for an external sample-and-hold.

ENABLE INPUTS

The two Enable inputs (Pins 13, 14) are TTL compatible, and are used to change the data outputs (D6–D0) from active to 3-state. This capability allows cascading two MC10321s into an 8-bit configuration, connecting the outputs directly to a data bus, multiplexing multiple converters, etc. See the Applications Information section for more details. For the outputs to be active, Pin 13 must be Logic "1," and Pin 14 must be a Logic "0." Changing either input will put the outputs into the high impedance mode. The Enable inputs affect **only** the state of the outputs — they do not inhibit a conversion. Both pins have a nominal threshold of ≈1.2 volts, their input currents are shown in Figure 5, and their input-output timing is shown in Figure 1 and 14. Leaving either pin open is equivalent to a Logic "1," although good design practice dictates that an input should never be left open.

The Overrange output (Pin 12) is not affected by the Enable inputs as it does not have 3-state capability.

OUTPUTS

The data outputs (Pins 1–4, 12, 18–20) are TTL level outputs with high impedance capability (except Overrange). Pin 4 is the MSB (D6), and Pin 18 is the LSB (D0). The seven outputs are active as long as the Enable inputs are true (EN = high, $\overline{EN}$ = low). The timing of the outputs relative to the Clock input and the Enable inputs is shown in Figures 1 and 14. Figures 7 and 8 indicate the output voltage versus load current, while Figure 3 indicates the leakage current when in the high impedance mode.

The output code is natural binary, depicted in Table 1.

The Overrange output (Pin 12) goes high when the input, V_{in}, is more positive than V_{RT} − 1/2 LSB. This output is always active — it does not have high impedance capability. Besides used to indicate an input overrange, it is additionally used for cascading two MC10321s to form an 8-bit A/D converter (see Figure 21).

TABLE 1

Input	V_{RT}, V_{RB} (Volts)			Output Code	Overrange
	2.048, 0	+1.0 V, −1.0 V	+1.0 V, 0 V		
$>V_{RT}$ − 1/2 LSB	>2.040 V	>0.9922 V	>0.9961 V	$7F_H$	1
V_{RT} − 1/2 LSB	2.040 V	0.9922 V	0.9961 V	$7F_H$	0 ↔ 1
V_{RT} − 1 LSB	2.032 V	0.9844 V	0.9922 V	$7F_H$	0
V_{RT} − 1 1/2 LSB	2.024 V	0.9766 V	0.9883 V	$7E_H \leftrightarrow 7F_H$	0
Midpoint	1.024 V	0.000 V	0.5000 V	40_H	0
V_{RB} + 1/2 LSB	8.0 mV	−0.9922 V	3.9 mV	$00_H \leftrightarrow 01_H$	0
$< V_{RB}$ + 1/2 LSB	<8.0 mV	<−0.9922 V	<3.9 mV	00_H	0

APPLICATIONS INFORMATION

POWER SUPPLIES, GROUNDING

The PC board layout, and the quality of the power supplies and the ground system **at the IC** are very important in order to obtain proper operation. Noise, from any source, coming into the device on V_{CC}, V_{EE}, or ground can cause an incorrect output code due to interaction with the analog portion of the circuit. At the same time, noise generated within the MC10321 can cause incorrect operation if that noise does not have a clear path to ac ground.

Both the V_{CC} and V_{EE} power supplies must be decoupled to ground **at the IC** (within 1" max) with a 10 μF tantalum and a 0.1 μF ceramic. Tantalum capacitors are recommended since electrolytic capacitors simply have too much inductance at the frequencies of interest. The quality of the V_{CC} and V_{EE} supplies should then be checked at the IC with a high frequency scope. Noise spikes (always present when digital circuits are present) can easily exceed 400 mV peak, and if they get into the analog portion of the IC, the operation can be disrupted. Noise can be reduced by inserting resistors and/or inductors between the supplies and the IC.

If switching power supplies are used, there will usually be spikes of 0.5 volts or greater at frequencies of 50–200 kHz. These spikes are generally more difficult to reduce because of their greater energy content. In extreme cases, 3-terminal regulators (MC78L05ACP, MC7905.2CT), with appropriate high frequency filtering, should be used and dedicated to the MC10321.

The ripple content of the supplies should not allow their magnitude to exceed the values in the Recommended Operating Limits.

The PC board tracks supplying V_{CC} and V_{EE} to the MC10321 should preferably not be at the tail end of the bus distribution, after passing through a maze of digital circuitry. The MC10321 should be close to the power supply, or the connector where the supply voltages enter the board. If the V_{CC} and V_{EE} lines are supplying considerable current to other parts of the boards, then it is preferable to have dedicated lines from the supply or connector directly to the MC10321.

The two ground pins (11, 17) must be connected directly together. Any long path between them can cause stability problems due to the inductance (@ 25 MHz) of the PC tracks. The ground return for the signal source must be noise free.

REFERENCE VOLTAGE CIRCUITS

Since the accuracy of the conversion is directly related to the quality of the references, it is imperative that accurate and stable voltages be provided to V_{RT} and V_{RB}. If the reference span is 2.0 volts, then 1/2 LSB is only 7.8 millivolts, and it is desireable that V_{RT} and V_{RB} be accurate to within this amount, and furthermore, that they do not drift more than this amount once set. Over the temperature range of −40 to +85°C, a maximum temperature coefficient of 31 ppm/°C is required.

The voltage supplies used for digital circuits should preferably **not** be used as a source for generating V_{RT} and V_{RB}, due to the noise spikes (up to 500 mV) present on the supplies and on their ground lines. Generally ±15 volts, or ±12 volts, are available for analog circuits, and are usually clean compared to supplies used for digital circuits, although ripple may be present in varying amounts. Ripple is easier to filter out than spikes, however, and so these supplies are preferred.

Figure 15 depicts a circuit which can provide an extremely stable voltage to V_{RT} **at the current required** (the maximum reference current is 20 mA @ 2.0 volts). The MC1403 series of references have very low temperature coefficients, good noise rejection, and a high initial accuracy, allowing the circuit to be built without an adjustment pot if the V_{RT} voltage is to remain fixed at one value. Using 0.1% wirewound resistors for the divider provides sufficient accuracy and stability in many cases. Alternately, resistor networks provide high ratio accuracies, and close temperature tracking. If the application requires V_{RT} to be changed periodically, the two resistors can be replaced with a 20 turn, cermet potentiometer. Wirewound potentiometers should not be used for this type of application since the pot's slider jumps from winding to winding, and an exact setting can be difficult to obtain. Cermet pots allow for a smooth continuous adjustment.

In Figure 15, R1 reduces the power dissipation in the transistor, and can be carbon composition. The 0.1 μF capacitor in the feedback path provides stability in the unity gain configuration. Recommended op amps are: LM358, MC34001 series, LM308A, LM324, and LM11C. Offset drift is the key parameter to consider in choosing an op amp, and the LM308A has the lowest drift of those mentioned. Bypass capacitors are not shown in Figure 15, but should always be provided at the input to the 2.5 volt reference, and at the power supply pins of the op amp.

Figure 16 shows a simpler and more economical circuit, using the LM317LZ regulator, but with lower initial accuracy and temperature stability. The op amp/current booster is not needed since the LM317LZ can supply the current directly. In a well controlled environment, this circuit will suffice for many applications. Because of the lower initial accuracy, an adjustment pot is a necessity.

Figure 17 shows two circuits for providing the voltage to V_{RB}. The circuits are similar to those of Figures 15 and 16, and have similar accuracy and stability. The MC1403 reference is used in conjunction with an op amp configured as an inverter, providing the negative voltage. The output transistor is a PNP in this case since the circuit must sink the reference current.

VIDEO APPLICATIONS

The MC10321 is suitable for digitizing video signals directly without signal conditioning, although the standard 1.0 volt p-p video signal can be amplified to a 2.0 volt p-p signal for slightly better accuracy. Figure 18 shows the input (top trace) and reconstructed output of a standard NTSC test signal, sampled at 25 MSPS, consisting of a sync pulse, 3.58 MHz color burst, a 3.58 MHz signal in a Sin^2x envelope, a pulse, a white level signal, and a black level signal. Figure 19 shows a Sin^2x pulse that has been digitized and reconstructed at 25 MSPS. The width of the pulse is ≈225 ns at the base. Figure 20 shows an application circuit for digitizing video.

8-BIT A/D CONVERTER

Figure 21 shows how two MC10321s can be connected to form an 8-bit converter. In this configuration, the outputs (D6–D0) of the two 7-bit converters are paralleled. The outputs of one device are active, while the outputs of other are in the 3-state mode. The selection is made by the OVERRANGE output of the lower MC10321, which controls Enable inputs on the two devices. Additionally, this output provides the 8th bit.

The reference ladders are connected in series, providing the 256 steps required for 8 bits. The input voltage range is determined by V_{RT} of the upper MC10321, and V_{RB} of the lower device. A minimum of 1.0 volt is required across each converter. The 500 Ω pot (20 turn cermet) allows for adjustment of the midpoint since the reference resistors of the two MC10321s may not be identical in value. Without the adjustment, a nonequal voltage division could occur, resulting in a nonlinear conversion. If the references are to be symmetrical about ground (e.g., ±1.0 volt or ±2.0 volts), the adjustment can be eliminated, and the midpoint connected to ground.

The use of latches on the outputs is optional, depending on the application. If latches are required, SN74LS173As are recommended.

50 MHz, 7 BIT A/D CONVERTER

Figure 22 shows how two MC10321s can be connected together in a flip-flop arrangement in order to have an effective conversion speed of 50 MHz. The 74F74D-type flip-flop provides a 25 MHz clock to each converter, and at the same time, controls the SELECT input to the MC74F257 multiplexers to alternately select the outputs of the two converters. A brief timing diagram is shown in the figure.

NEGATIVE VOLTAGE REGULATOR

In the cases where a negative power supply is not available — neither the −3.0 to −6.0 volts, nor a higher negative voltage from which to derive it — the circuit of Figure 23 can be used to generate −5.0 volts from the +5.0 volts supply. The PC board space required is small (≈2.0 in^2), and it can be located physically close to the MC10321. The MC34063 is a switching regulator, and in Figure 23 is configured in an inverting mode of operation. The regulator operating specifications are given in the figure.

GLOSSARY

APERTURE DELAY — The time difference between the sampling signal (typically a clock edge) and the actual analog signal converted. The actual signal converted may occur before or after the sampling signal, depending on the internal configuration of the converter.

BIPOLAR INPUT — A mode of operation whereby the analog input (of an A-D), or output (of a DAC), includes both negative and positive values. Examples are −1.0 to +1.0 V, −5.0 to +5.0 V, −2.0 to +8.0 V, etc.

BIPOLAR OFFSET ERROR — The difference between the actual and ideal locations of the 00_H to 01_H transition, where the ideal location is 1/2 LSB above the most negative reference voltage.

BIPOLAR ZERO ERROR — The error (usually expressed in LSBs) of the input voltage location (of a 7-bit A/D) of the 40_H to 41_H transition. The ideal location is 1/2 LSB above zero volts in the case of an A/D set up for a symmetrical bipolar input (e.g., −1.0 to +1.0 V).

DIFFERENTIAL NONLINEARITY — The maximum deviation in the actual step size (one transition level to another) from the ideal step size. The ideal step size is defined as the Full Scale Range divided by 2^n (n = number of bits). This error must be within ±1 LSB for proper operation.

FULL SCALE RANGE (ACTUAL) — The difference between the actual minimum and maximum end points of the analog input (of an A-D).

FULL SCALE RANGE (IDEAL) — The difference between the actual minimum and maximum end points of the analog input (of an A-D), plus one LSB.

GAIN ERROR — The difference between the actual and expected gain (end point to end point), with respect to the reference of a data converter. The gain error is usually expressed in LSBs.

GREY CODE — Also known as **reflected binary code,** it is a digital code such that each code differs from adjacent codes by only one bit. Since more than one bit is never changed at each transition, race condition errors are eliminated.

INTEGRAL NONLINEARITY — The maximum error of an A/D, or DAC, transfer function from the ideal straight line connecting the analog end points. This parameter is sensitive to dynamics, and test conditions must be specified in order to be meaningfull. This parameter is the best overall indicator of the device's performance.

LSB — Least Significant Bit. It is the lowest order bit of a binary code.

LINE REGULATION — The ability of a voltage regulator to maintain a certain output voltage as the input to the regulator is varied. The error is typically expressed as a percent of the nominal output voltage.

LOAD REGULATION — The ability of a voltage regulator to maintain a certain output voltage as the load current is varied. The error is typically expressed as a percent of the nominal output voltage.

MONOTONICITY — The characteristic of the transfer function whereby increasing the input code (of a DAC), or the input signal (of an A/D), results in the output never decreasing.

MSB — Most Significant Bit. It is the highest order bit of a binary code.

NATURAL BINARY CODE — A binary code defined by:

$$N = A_n 2^n + \ldots + A_3 2^3 + A_2 2^2 + A_1 2^1 + A_0 2^0$$

where each "A" coefficient has a value of 1 or 0. Typically, all zeroes corresponds to a zero input voltage of an A/D, and all ones corresponds to the most positive input voltage.

NYQUIST THEORY — See Sampling Theorem.

OFFSET BINARY CODE — Applicable only to bipolar input (or output) data converters, it is the same as Natural Binary, except that all zeroes corresponds to the most negative input voltage (of an A/D), while all ones corresponds to the most positive input.

POWER SUPPLY SENSITIVITY — The change in a data converters performance with changes in the power supply voltage(s). This parameter is usually expressed in percent of full scale versus ΔV.

QUANTITIZATION ERROR — Also known as digitization error or uncertainty. It is the inherent error involved in digitizing an analog signal due to the finite number of steps at the digital output versus the infinite number of values at the analog input. This error is a minimum of ±1/2 LSB.

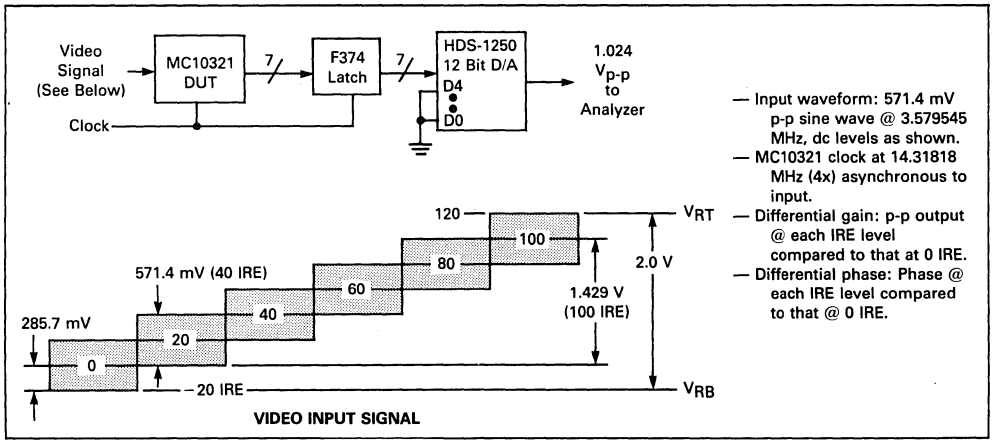
RESOLUTION — The smallest change which can be discerned by an A/D converter, or produced by a DAC. It is usually expressed as the number of bits, n, where the converter has 2^n possible states.

SAMPLING THEOREM — Also known as the Nyquist Theorem. It states that the sampling frequency of an A/D must be no less than 2x the highest frequency (of interest) of the analog signal to be digitized in order to preserve the information of that analog signal.

UNIPOLAR INPUT — A mode of operation whereby the analog input range (of an A/D), or output range (of a DAC), includes values of a single polarity. Examples are 0 to +2.0 V, 0 to −5.0 V, +2.0 to +8.0 V, etc.

UNIPOLAR OFFSET ERROR — The difference between the actual and ideal locations of the 00_H to 01_H transition, where the ideal location is 1/2 LSB above the most negative input voltage.

FIGURE 11 — DIFFERENTIAL PHASE AND GAIN TEST



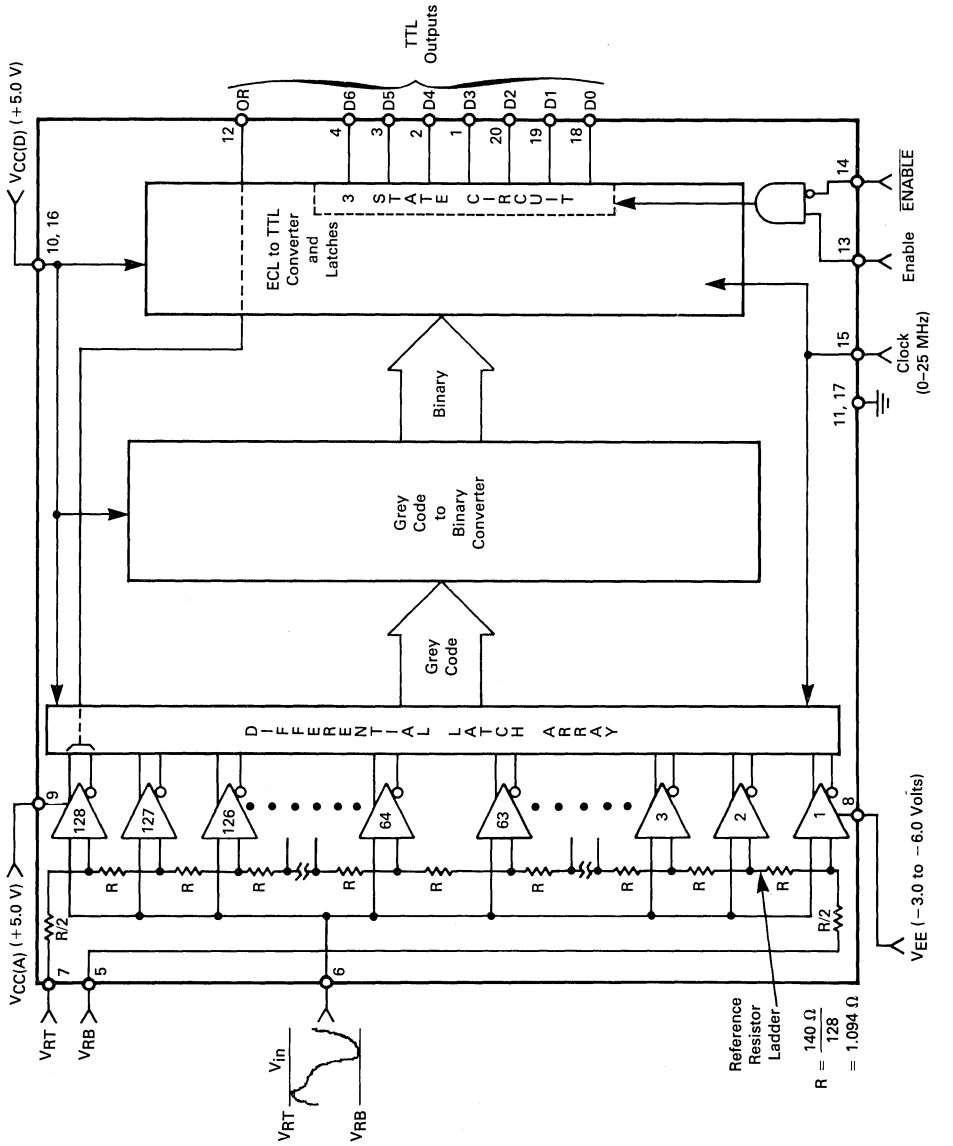


FIGURE 12 — MC10321

FIGURE 13 — CONVERSION SEQUENCE

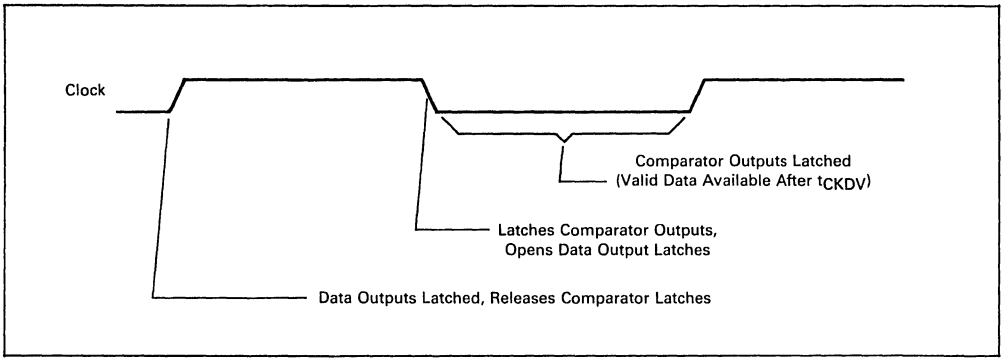
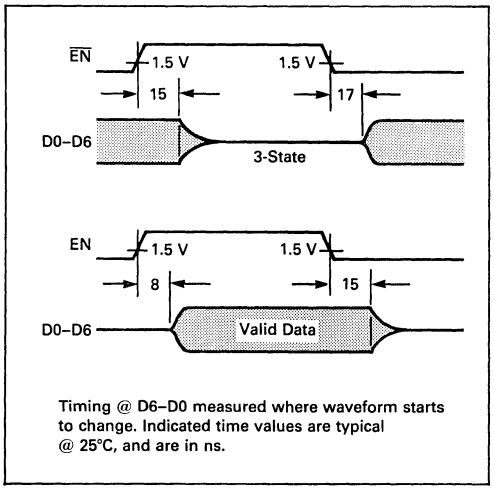
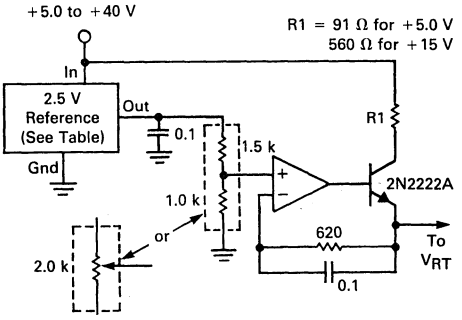


FIGURE 14 — ENABLE TO OUTPUT CRITICAL TIMING



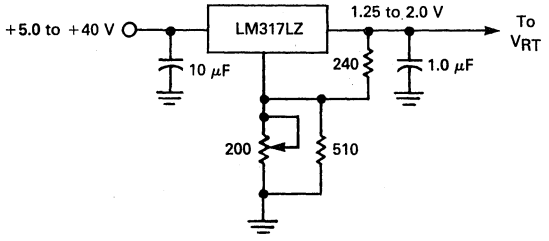
Timing @ D6–D0 measured where waveform starts to change. Indicated time values are typical @ 25°C, and are in ns.

FIGURE 15 — PRECISION V_{RT} VOLTAGE SOURCE



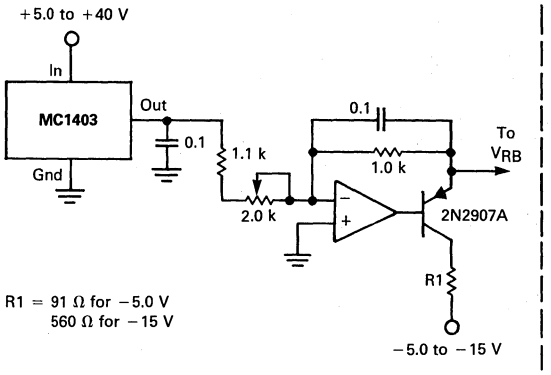
2.5 V References	MC1403U	MC1403AU
Line Regulation	0.5 mV	0.5 mV
TC (ppm/°C) max	40	25
ΔV_{out} for 0–70°C	7.0 mV	4.4 mV
Initial Accuracy	±1.0%	±1.0%

FIGURE 16 — V_{RT} VOLTAGE SOURCE



LM317LZ	
Line Regulation	1.0 mV
TC (ppm/°C) max	60
ΔV_{out} for 0–70°C	8.4 mV
Initial Accuracy	±4.0%

FIGURE 17 — V_{RB} VOLTAGE SOURCES



Reference	MC1403U	MC1403AU	LM337MT
Line Regulation	0.5 mV	0.5 mV	1.0 mV
TC (ppm/°C) max	40	25	48
ΔV_{out} for 0–70°C	7.0 mV	4.4 mV	6.7 mV
Initial Accuracy	±1.0%	±1.0%	±4.0%

6

FIGURE 18

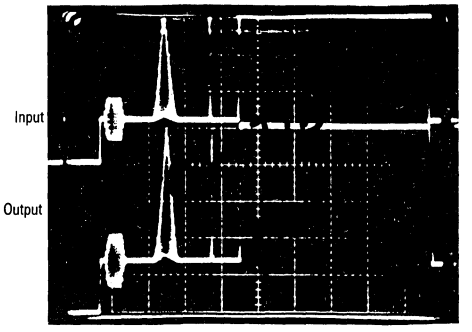


FIGURE 19

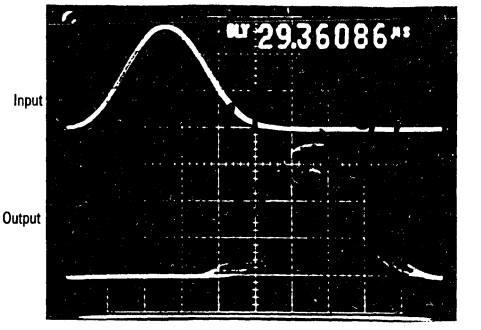
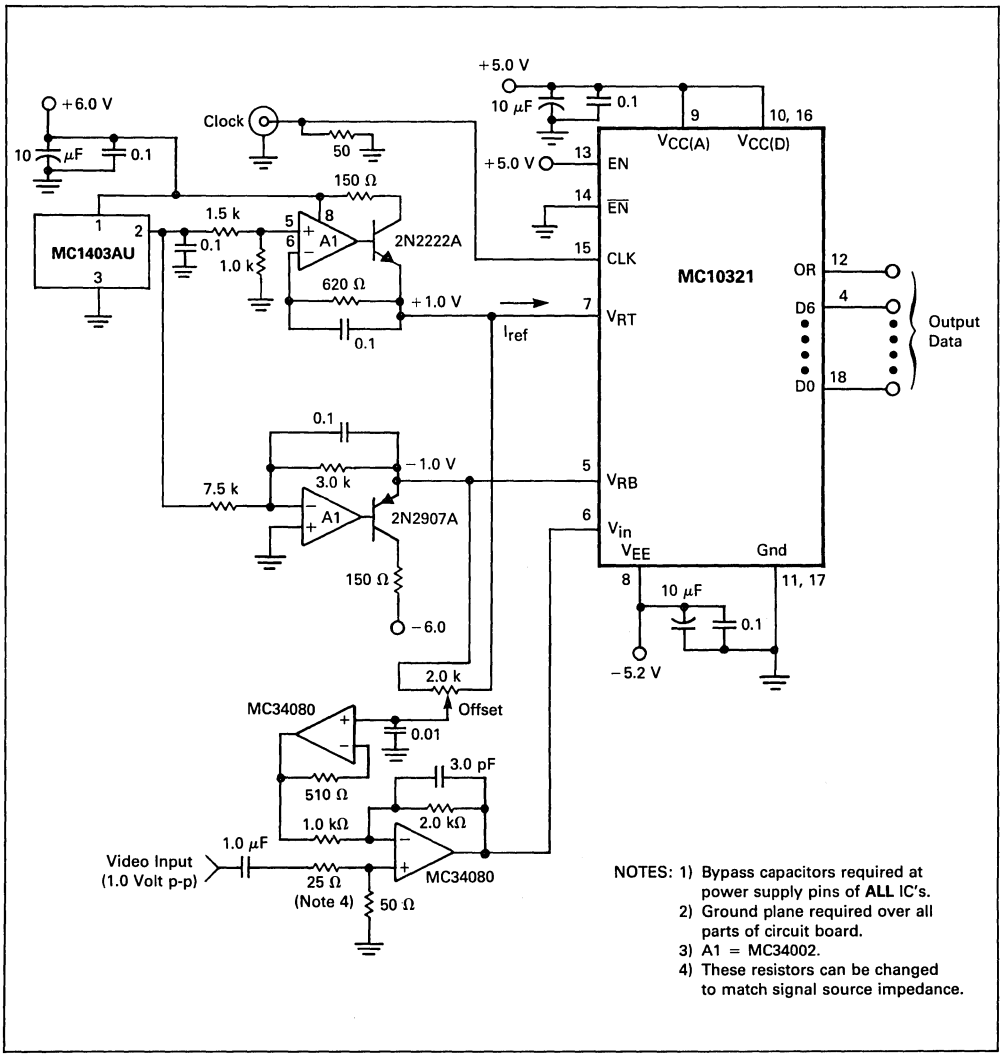


FIGURE 20 — APPLICATION CIRCUIT FOR DIGITIZING VIDEO



NOTES: 1) Bypass capacitors required at power supply pins of **ALL** IC's.
2) Ground plane required over all parts of circuit board.
3) A1 = MC34002.
4) These resistors can be changed to match signal source impedance.

FIGURE 21 — 8-BIT A/D CONVERTER

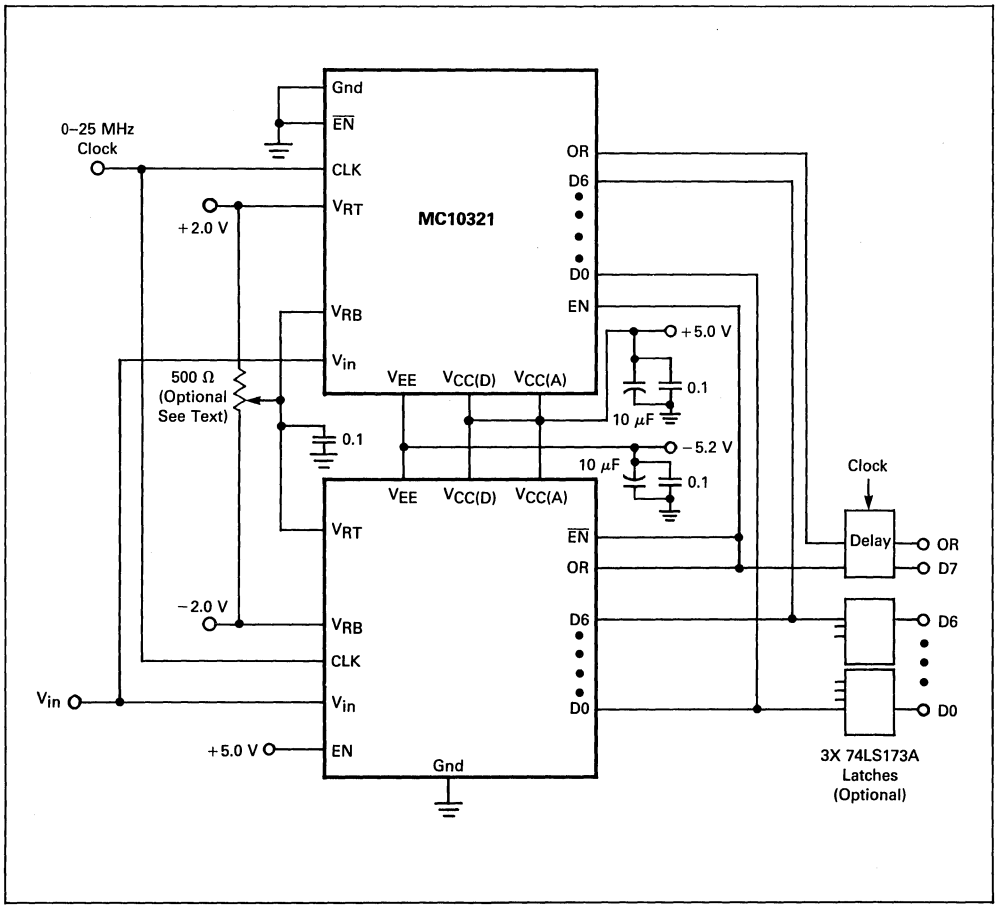


FIGURE 22 — 50 MHz 7 BIT A/D CONVERTER

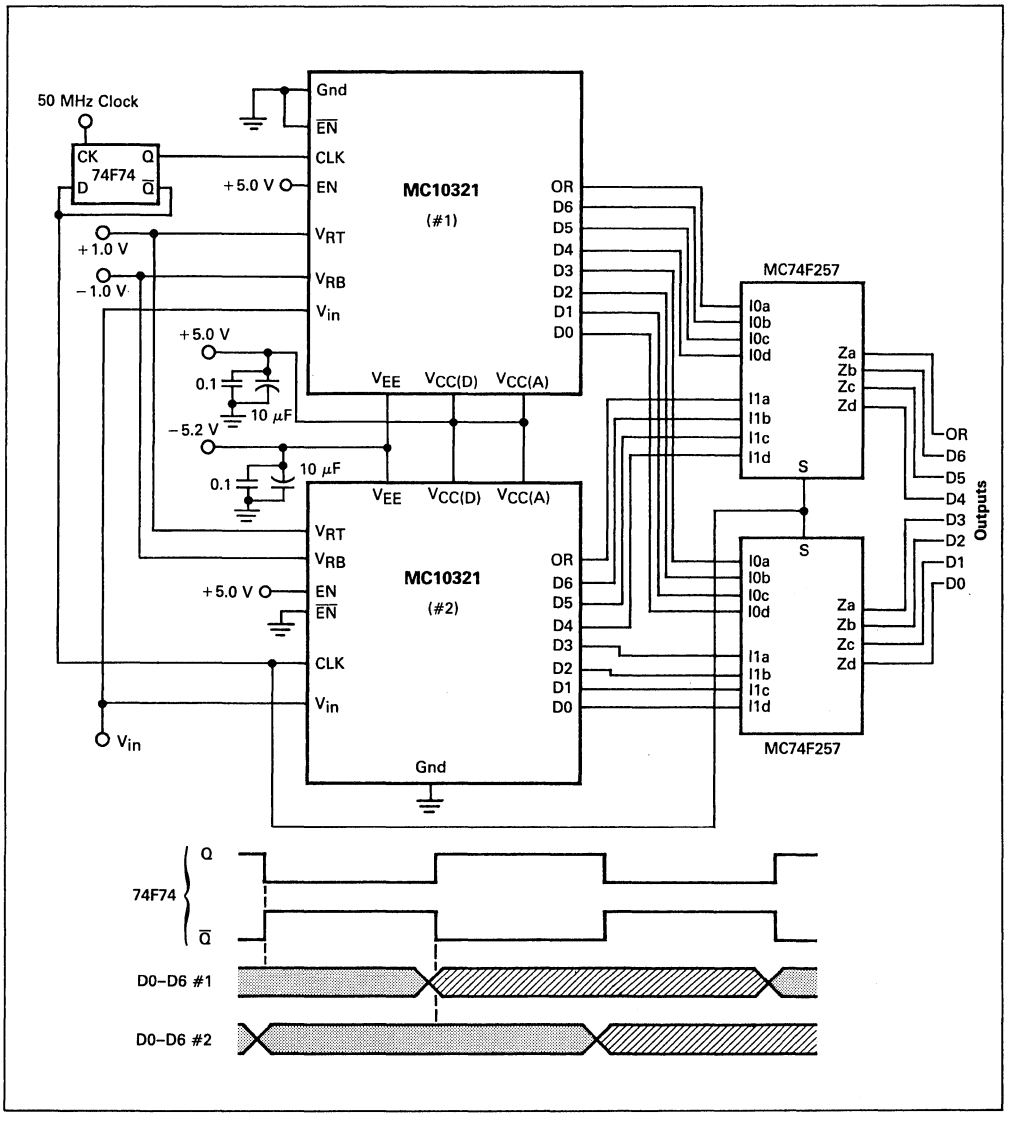
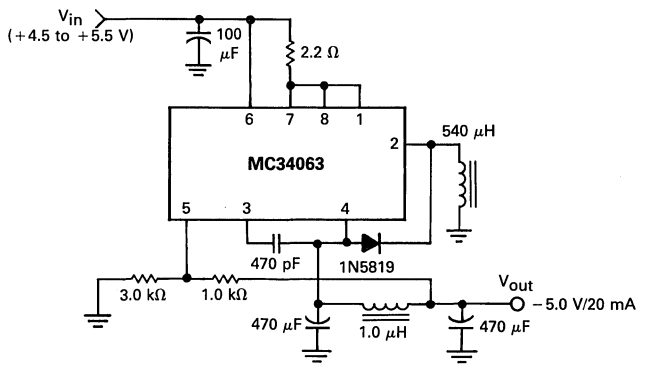


FIGURE 23 — −5.0 VOLT REGULATOR



Line Regulation	4.5 V < V_{in} < 5.5 V, I_{out} = 10 mA	0.16%
Load Regulation	V_{in} = 5.0 V, 8.0 mA < I_{out} < 20 mA	0.4%
Output Ripple	V_{in} = 5.0 V, I_{out} = 20 mA	2.0 mV p-p
Short Circuit I_{out}	V_{in} = 5.0 V, R_L = 0.1 Ω	140 mA
Efficiency	V_{in} = 5.0 V, I_{out} = 50 mA	52%

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MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC10322

Advance Information

8-Bit Video DAC with TTL Inputs

8-BIT VIDEO DAC with TTL INPUTS

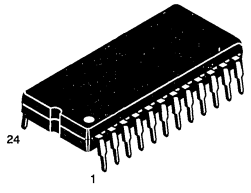
SILICON MONOLITHIC INTEGRATED CIRCUIT

The MC10322 is a 40 MegaSample Per Second (MSPS) 8-bit Video DAC capable of directly driving a 75 Ω cable, with appropriate terminations, to EIA-170 and EIA-343-A video levels. The logic inputs (data and controls) are TTL compatible. Input registers negate the need for external latches unless the transparent mode is selected.

Video controls (Force High, Blank, Bright, and Sync) permit an easy interface to standard video systems. The Clock (Convert) inputs can be differential or single-ended. Complementary outputs are provided for custom displays or special effects.

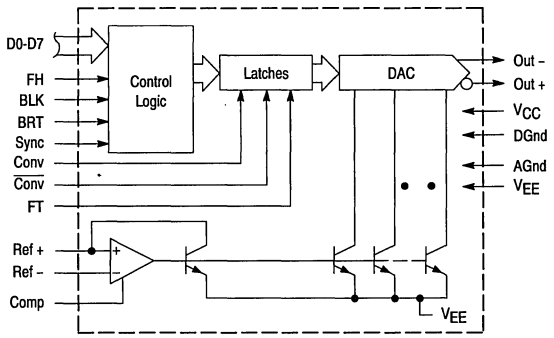
The MC10322 is fabricated with Motorola's MOSAIC™ process which provides high speed with low power consumption. The MC10322 is available in a 24 pin plastic DIP package.

- 40 MSPS Minimum Conversion Rate
- TTL Compatible Inputs
- 8-Bit Linearity
- Latched Data and Video Control Inputs, or Transparent Mode
- Video Controls: Force High, Blank, Bright, Sync
- Each Differential Current Outputs Can Swing 2.0 V
- Modulation Capability (Multiplying Mode)
- PSRR > 60 dB
- Operates from + 5.0 and – 5.2 V Power Supplies
- Power Dissipation: Typically 344 mW
- Available in 24 Pin Plastic DIP Package
- Available with ECL Inputs (MC10324)

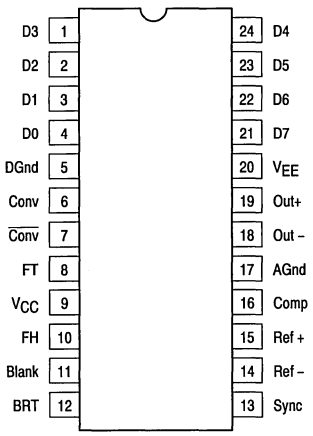


P SUFFIX
PLASTIC PACKAGE
CASE 649

Simplified Block Diagram



PIN CONNECTIONS

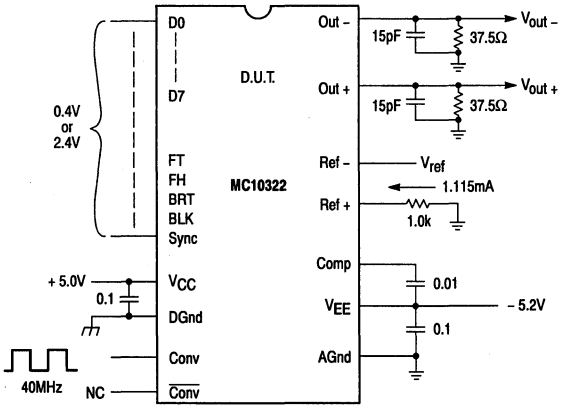


(Top View)

PIN FUNCTION DESCRIPTION

Symbol	Pin	Description
D0-D7	1-4, 21-24	Data inputs. D0 is the LSB and D7 is the MSB. Inputs are TTL compatible. Maximum update rate is typically 60 MHz. The eight bits control the Gray Scale amplitude only, and do not involve the Sync or Blank levels.
DGnd	5	Connect to system digital ground. This pin must be within 100 mV of AGnd (Pin 17).
Conv	6	Convert input. The rising edge latches data and controls if FT = 0. May be used single-ended (with Pin 7 at a fixed voltage), or differentially with Pin 7.
$\overline{\text{Conv}}$	7	$\overline{\text{Convert}}$ input. The falling edge latches data and controls if FT = 0. May be used single-ended (with Pin 6 at a fixed voltage), or differentially with Pin 6.
FT	8	Feedthrough. When high, the internal latches are transparent, and Pins 6 and 7 are unused. When low, data and controls are latched by Pins 6 and 7.
V_{CC}	9	Connect to + 5.0 V, ± 10%. This pin powers the digital portion of the IC.
FH	10	Force High. A logic high internally sets data inputs = 1, overriding external data inputs.
Blank	11	A logic high overrides data inputs, sets the outputs to the video blanking level.
BRT	12	Bright. A logic high increases the Gray Scale output level by ≈ 11%, providing an enhanced display. Does not affect Sync or Blank.
Sync	13	A logic high overrides all other inputs, and sets the output to video sync level.
Ref –	14	Inverting Reference input. A high impedance input, normally set to a negative DC voltage in the range of – 0.8 to –1.7 V. Can be used to modulate the output.
Ref +	15	Noninverting Reference input. A virtual ground, current supplied to this pin (between 0.5 and 1.7 mA) sets the maximum output current.
Comp	16	Compensation. A capacitor between this pin and Pin 20 stabilizes the reference amplifier.
AGnd	17	Connect to system analog ground. This pin must be within 100 mV of DGnd (Pin 5).
Out –	18	A high impedance current output. Video voltage levels are produced when connected to a 75 Ω cable with appropriate terminations. This output provides a "sync down" waveform. If unused, connect to Pin 17.
Out +	19	Complementary output provides a "sync up" waveform. If unused, connect to Pin 17.
V_{EE}	20	Connect to – 5.2 V, ± 10%. This supply should be referenced to analog ground.

Figure 1. Test Circuit



MAXIMUM RATINGS

Characteristics	Value	Unit
V_{CC} (with respect to DGnd and AGnd)	+ 7.0, – 0.5	Vdc
DGnd (with respect to AGnd)	–1.0 to + 0.5	Vdc
V_{EE} (with respect to AGnd)	– 7.0, + 0.5	Vdc
Logic Input Voltage (with respect to DGnd)	– 0.5	Vdc
Logic Input Voltage (with respect to V_{CC})	+ 0.5	Vdc
Voltage at Reference Amp Inputs	+ 0.5, V_{EE}	Vdc
Current Into Ref +	+ 6.0, 0	mA
Voltage Applied to Out +, Out – (Normal Operation)	+ 0.5, – 2.0	Vdc
Voltage Applied to Out +, Out – (V_{CC}, V_{EE} = 0)	+ 0.5, – 1.2	Vdc
Junction Temperature	– 65 to +150	°C

Devices should not be operated at these values. The "Recommended Operating Conditions" table provides conditions for actual device operation.

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC} — DGnd DGnd — AGnd V_{EE} — AGnd	4.5 – 0.1 – 5.72	5.0 0 – 5.2	5.5 + 0.1 – 4.68	Vdc
Logic Input Voltage	V_{in}	DGnd	—	V_{CC}	Vdc
Reference Current (for Video Standard Output) (for all other applications)	I_{ref}	— 0.5	1.115 —	— 1.7	mA
Voltage at Ref –	V_{ref}	–1.7	—	– 0.8	Vdc
Output Load Impedance	R_L	0	37.5	—	Ω
Output Compliance (with respect to AGnd)	V_O	–1.7	—	+ 0.3	Vdc
Convert Frequency (FT = 0) Data Update Frequency (FT = 1)	f_s	0 0	60 60	40 40	MHz
Convert, $\overline{\text{Convert}}$ Common Mode Range	V_{CM}	DGnd +1.3	—	V_{CC} – 2.0	Vdc
Operating Ambient Temperature	T_A	– 40	—	+ 85	°C

All limits are not necessarily functional concurrently.

ELECTRICAL CHARACTERISTICS (T_A = 25°C, I_{ref} = 1.115 mA, Load = 37.5 Ω to AGnd, V_{CC} = + 5.0 V, V_{EE} = – 5.2 V, see Figure 1.)

Characteristic	Symbol	Min	Typ	Max	Unit
REFERENCE AMPLIFIER					
Input Offset (Ref + to Ref –)	V_{OS}	–15	±5.0	+15	mV
Bias Current Into Ref –	I_{BR}	—	1.4	5.0	µA
Bandwidth (C_C = 250 pF, V_{ref} – = 10 mVp-p)	BW	—	3.0	—	MHz
DIGITAL INPUTS					
Low Voltage	V_{IL}	0	—	0.8	Vdc
High Voltage	V_{IH}	2.0	—	V_{CC}	Vdc
Low Current (Data, Controls @ 0.4 V)	I_{IL}	—	10	25	µA
High Current (Data, Controls @ 2.4 V)	I_{IH}	—	65	110	µA
Low Current (Conv, $\overline{\text{Conv}}$ @ 0.4 V)	I_{IL}	– 200	–144	—	µA
High Current (Conv, $\overline{\text{Conv}}$ @ 2.4 V)	I_{IH}	—	100	140	µA
Input Capacitance	C_{in}	—	3.0	—	pF

NOTES: 1. Current into a pin is designated as positive, current out of a pin as negative.
2. Controls = FH, BRT, BLK, Sync, and FT.

ELECTRICAL CHARACTERISTICS (T_A = 25°C, I_{ref} = 1.115 mA, Load = 37.5 Ω to AGnd, V_{CC} = + 5.0 V, V_{EE} = – 5.2 V, see Figure 1.)

Characteristic	Symbol	Min	Typ	Max	Unit
TRANSFER CHARACTERISTICS					
Resolution	Res	8.0	8.0	8.0	Bits
Integral Nonlinearity	INL	–1/2	0	+1/2	LSB
Differential Nonlinearity	DNL	–1/2	0	+1/2	LSB
Monotonicity	—		Guaranteed*		
Differential Gain	DG	—	1.0	—	%
Differential Phase	DP	—	0.5	—	Deg
OUTPUTS					
Output Current at Out – (Control Inputs = 0 Except as Noted)					µA
Enhanced White (FH = BRT = 1)	I_{EH-}	0	18	100	
Normal White (FH = 1 or D0 – D7 = 1)	I_{NW-}	1.75	1.94	2.13	mA
Normal Black (D0 – D7 = 0) Referred to Normal White	I_{NB-}	16.6	17.7	18.7	
Blank Referred to Normal Black (BLK = 1)	I_{BLN-}	1.32	1.43	1.54	
Sync Referred to Blank (SYNC = 1)	I_{SYNC-}	7.1	7.7	8.3	
Output Voltage at Out – (Control Inputs = 0 Except as Noted)					mV
Enhanced White (FH = BRT = 1)	V_{EH-}	0	– 0.67	– 3.75	
Normal White (FH = 1 or D0 – D7 = 1)	V_{NW-}	– 67.8	– 73	– 77.6	
Normal Black (D0 – D7 = 0) Referred to Normal White	V_{NB-}	– 626	– 663	– 694	
Blank Referred to Normal Black (BLK = 1)	V_{BLN-}	– 50.6	– 53.6	– 56.6	
Sync Referred to Blank (SYNC = 1)	V_{SYNC-}	– 270	– 288	– 308	
Output Current at Out + (Control Inputs = 0 Except as Noted)					mA
Enhanced White (FH = BRT = 1)	I_{EH+}	26.8	28.8	30.6	
Normal White (FH = 1 or D0 – D7 = 1)	I_{NW+}	25	26.8	28.5	
Normal Black (D0 – D7 = 0) Referred to Normal White	I_{NB+}	–16.6	–17.7	–18.7	
Blank Referred to Normal Black (BLK = 1)	I_{BLN+}	–1.32	–1.43	–1.54	
Sync Referred to Blank (SYNC = 1)	I_{SYNC+}	– 7.1	– 7.7	– 8.3	
Output Voltage at Out + (Control Inputs = 0 Except as Noted)					mV
Enhanced White (FH = BRT = 1)	V_{EH+}	–1016	–1080	–1132	
Normal White (FH = 1 or D0 – D7 = 1)	V_{NW+}	– 949	–1005	–1057	
Normal Black (D0 – D7 = 0) Referred to Normal White	V_{NB+}	626	663	694	
Blank Referred to Normal Black (BLK = 1)	V_{BLN+}	50.6	53.6	56.6	
Sync Referred to Blank (SYNC = 1)	V_{SYNC+}	270	288	308	
Output Matching ($\lvert I_{NB+} \rvert - \lvert I_{NB-} \rvert$)	I_{FSER}	– 50	0	+ 50	µA
Gain Error (Gray Scale at Out –)	G_{ER}	– 50	0	+ 5.0	%
Output Impedance (Gray Scale, –1.7 V < V_O < 0.3 V)	Z_O	25	100	—	kΩ
Output Capacitance	C_O	—	16	—	pF
Glitch Energy (Clocked Mode)					pV-sec
At Midscale Transition (D0 – D7 = 127↔128)	E_{GM}	—	18	—	
Due to Clock Feedthrough (D0 – D7 = Constant)	E_{GC}	—	2.0	—	
Due to Data Feedthrough (Clock = Constant)	E_{GD}	—	25	—	
Peak Glitch Current (Clocked Mode)					
At Midscale Transition (D0 – D7 = 127↔128)	I_{GM}	—	0.2	—	mA
Due to Clock Feedthrough (D0 – D7 = Constant)	I_{GC}	—	55	—	µA
Due to Data Feedthrough (Clock = Constant)	I_{GD}	—	0.5	—	mA
POWER SUPPLIES					
Supply Current					mA
(V_{CC} = + 5.5 V)	I_{CC}	—	22	28	
(V_{EE} = – 5.72 V, I_{ref} = 1.115 mA)	I_{EE}	– 55	– 45	—	
Power Dissipation	P_D	—	344	469	mW
Power Supply Sensitivity at Outputs					µA/V
(V_{EE} = – 5.2 V, 4.5 < V_{CC} < 5.5 V)	PSSD	– 25	1.0	+ 25	
(V_{CC} = + 5.0 V, – 5.72 < V_{EE} < – 4.68 V)	PSSA	–100	20	+100	
V_{CC} Supply Rejection (V_{CC} = + 5.0 V, V_{EE} = – 5.2 V, f = 10 kHz)	PSRRD	—	85	—	dB
V_{EE} Supply Rejection (V_{CC} = + 5.0 V, V_{EE} = – 5.2 V, f = 10 kHz)	PSRRA	—	65	—	dB

*Guaranteed by linearity tests.

TIMING CHARACTERISTICS (T_A = 25°C, I_{ref} = 1.115 mA, Load = 37.5 Ω//15 pF, V_{CC} = + 5.0 V, V_{EE} = – 5.2 V, see Figures 2, 3.)

Characteristic	Symbol	Min	Typ	Max	Unit
Maximum Conversion or Update Rate	F_S	40	60	—	MHz
Clocked Mode (FT = 0)					ns
Clock to Output Delay (Data, Controls)	t_{COD}	—	10	—	
Setup Time — Data to Conv Rising Edge	t_{SD}	—	8.0	—	
FH, Sync to Conv Rising Edge	t_{SFS}	—	5.0	—	
BRT, BLK to Conv Rising Edge	t_{SB}	—	4.0	—	
Hold Time — All Inputs (After Conv Rising Edge)	t_H	—	0	—	
Minimum Clock Width (High or Low)	t_{PW}	—	6.0	—	
Transparent Mode (FT = 1)					ns
Data to Output Delay	t_{DO}	—	16	—	
Sync to Output Delay	t_{SO}	—	13	—	
BLK to Output Delay	t_{BO}	—	14	—	
FH to Output Delay	t_{FO}	—	16	—	
BRT to Output Delay	t_{RO}	—	12	—	
Output Rise/Fall Time — 10 to 90% of Gray Scale	t_{RFG}	—	2.0	—	ns
Enhanced White to Sync Level	t_{RFF}	—	3.0	—	
Output Settling Time	t_{SET}	—	4.0	—	ns

FUNCTIONAL DESCRIPTION

Introduction

The MC10322 is an 8-bit DAC intended for video applications, employing TTL inputs for the data (natural binary code) and video controls, and outputs capable of directly driving a standard 50 Ω or 75 Ω monitor. Its use is not limited to video, however, any application requiring a high speed (typically 60 MHz) DAC, or a DAC with high output current capability (up to 44 mA) can use the MC10322. The input data and controls may be clocked into the internal registers, or the MC10322 may be used in the transparent mode eliminating the need for the clock.

The MC10322 may be used in the multiplying mode by varying the reference current along with the digital inputs producing the product of the two at the outputs. The reference current can be varied over a range of 0.5 to 1.7 mA. Standard power supplies are required: + 5.0 V and – 5.2 V, both ± 10%. Power consumption is nominally 344 mW.

DAC Outputs

The outputs of the MC10322 are high impedance constant current sinks whose values depends on the reference current (I_{ref}), the binary value of the digital word at D0 – D7, and the status of the video controls (Sync, BLK, FH, and BRT). Complementary outputs are provided allowing an increased output swing (when used differentially), or for creation of special effects required by the application. For a given reference current, the sum of the two output currents is a constant equal to:

$$(I_{O}-) + (I_{O}+) = I_{ref} \times 25.86$$

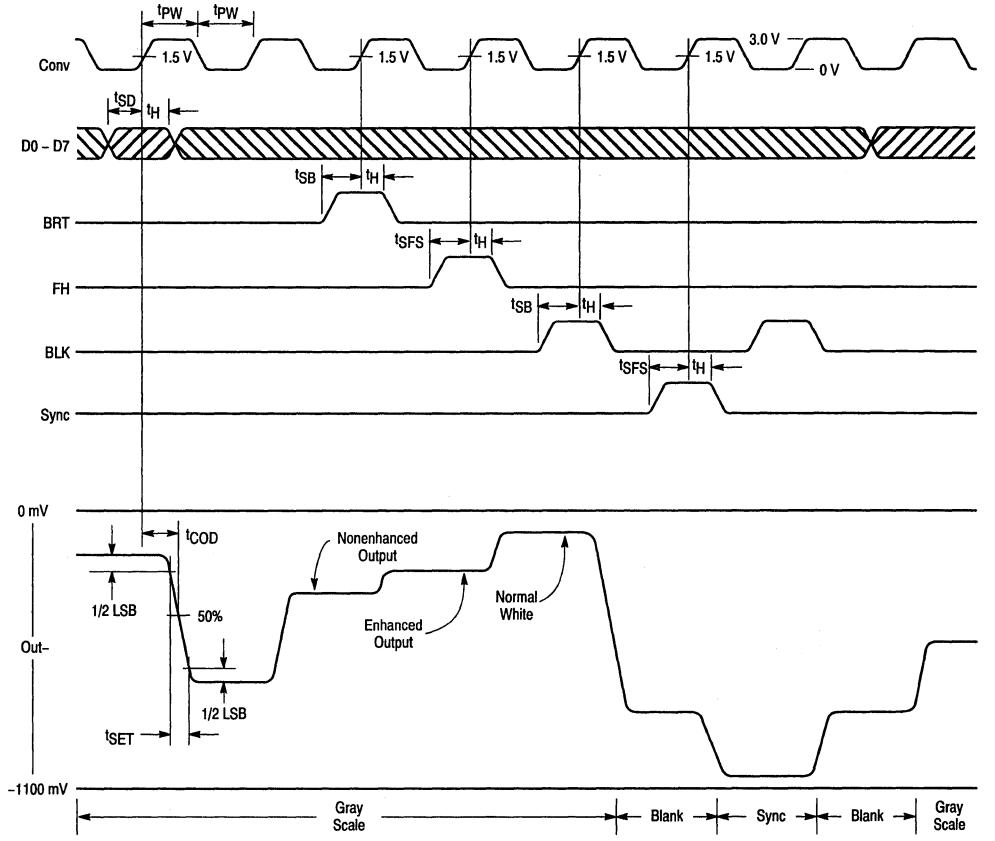
The Out – output provides a "sync down" waveform, while the Out + output provides a "sync up" waveform (see Table 1). Current flow is **into** each of the outputs. Each output's impedance is typically 100 kΩ over the compliance range of –1.7 to + 0.3 V, and the output capacitance is typically 16 pF. An unused output cannot be left open — both outputs must be connected to a voltage within the compliance range. Both outputs should be equally loaded for best accuracy.

Table 1. Output Levels

mV	BRT = 0		BRT = 1	
	Out –	Out +	Out –	Out +
0		Sync	Enhanced White	Sync
–100	Normal White			
– 200				
– 300		Blank	Enhanced	Blank
– 400	Gray Scale	Normal Black	Gray Scale	
– 500				Enhanced Black
– 600				
– 700	Normal Black	Gray Scale	Enhanced Black	Enhanced
– 800	Blank		Blank	Gray Scale
– 900				
–1000		Normal White		Enhanced White
–1100	Sync		Sync	

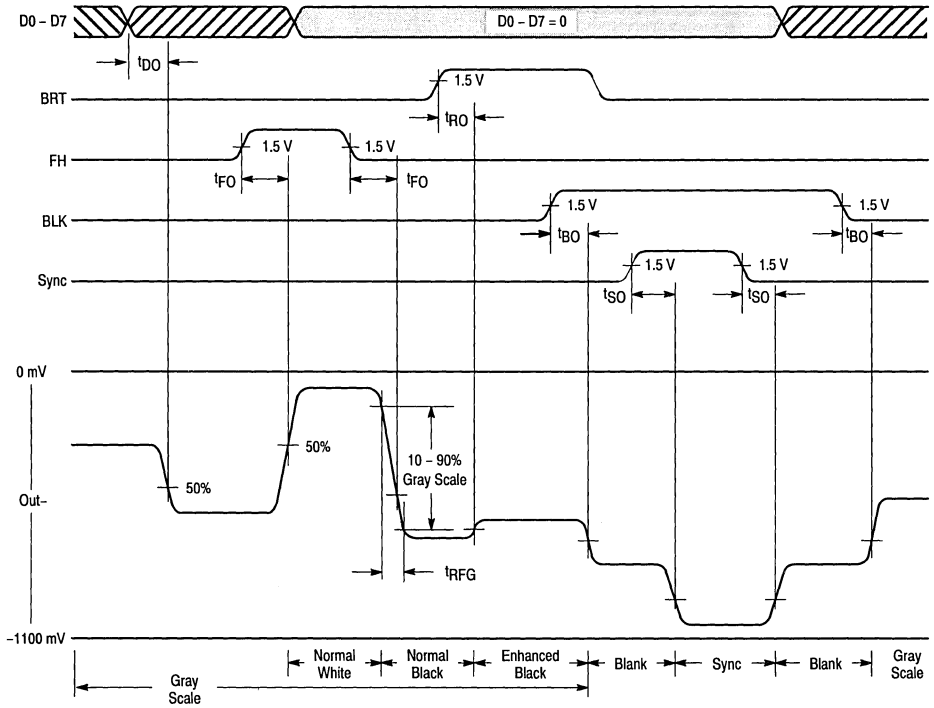
I_{ref} = 1.115 mA, R_L = 37.5 Ω.

Figure 2. Timing Diagram, Clocked Mode (FT = 0)



NOTES: 1. Single-ended clock used in production testing.
2. If differential clock is used, timing would be determined from the crossover point of the two clock signals.
3. If $\overline{\text{Convert}}$ is used in single-ended mode, timing would be measured from its falling edge.
4. Timing to output from data and controls is from Convert rising edge (threshold) to where the output has changed to 50% of final value.
5. Reference current = 1.115 mA. Output load = 37.5 Ω.
6. Waveform at Out + is inverted from that shown above.

Figure 3. Timing Diagram, Transparent Mode (FT = 1)



NOTES: 1. Reference current = 1.115 mA. Output load = 37.5 Ω.
2. Waveform at Out + is inverted from that shown above.
3. Timing from D0 – D7 and Controls is to where output has changed to 50% of final value.

TRUTH TABLE

Inputs					Outputs				
Controls				Data	Out –		Out +		
Sync	Blank	Force High	Bright	D7 – D0	(mA)	(mV)	(mA)	(mV)	Condition
1	X	X	X	X	28.8	–1080	0	0	Sync
0	1	X	X	X	21.1	– 790	7.7	– 289	Blank
0	0	0	0	000..	19.6	– 736	9.1	– 341	Normal Black
0	0	0	1	000..	17.7	– 663	11.1	– 416	Enhanced Black
0	0	1	0	X	1.94	– 73	26.8	–1005	Normal White
0	0	0	0	111..	1.94	– 73	26.8	–1005	Normal White
0	0	0	1	111..	0	0	28.8	–1080	Enhanced White
0	0	1	1	X	0	0	28.8	–1080	Enhanced White

NOTES: 1. Current flow is into the output pins.
2. Output voltage measured across a 37.5 Ω resistor to AGnd.
3. Waveform at Out + is inverted from that at Out –.
4. Reference Current = 1.115 mA.

DAC Gray Scale (D0 – D7)

Within the Gray Scale (all 4 video controls = 0), the current at Out – is controlled by the data inputs (D0 – D7) according to the following equation:

$$I_{O-}(GS) = \frac{I_{ref} \times (255-A)}{16} + (I_{ref} \times 1.74)$$

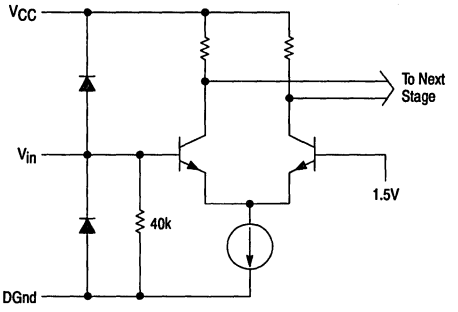
The current at Out + in the Gray Scale is determined by:

$$I_{O+}(GS) = \frac{I_{ref} \times A}{16} + (I_{ref} \times 8.18)$$

For the test value of I_{ref} = 1.115 mA, I_{O-} varies from 19.6 mA to 1.94 mA as the digital inputs (A) vary from 0 to 255 (00_H to FF_H), and I_{O+} will vary from 9.12 mA to 26.8 mA. The data inputs are overridden by Sync, BLK, or FH.

Figure 4 depicts a typical input stage configuration, and Figure 8 indicates the typical input current. The input's threshold is ≈ +1.5 V, independent of V_{CC}. An open input is equivalent to a logic low, but good design practices dictate that inputs should never be left open. The inputs must be kept within the range of V_{CC} and DGnd. If an input is taken more than 0.5 V above VCC or below Gnd excessive currents will flow, and the DAC output waveform will be distorted.

Figure 4. Typical Input Stage



DAC – Video Controls

The four video controls (Sync, BLK, FH, and BRT) are logic level inputs, TTL compatible, which permit setting the outputs to standard video levels. All four are active high. The Truth Table on page 7 indicates their priority.

The Force High input (FH) overrides the data inputs (D0 – D7), setting the DAC inputs to all 1s (FF_H). In most applications, this is equivalent to the normal white level. FH can be used with the BRT input to create an enhanced white, but is overridden by Sync or BLK.

The Bright input (BRT) shifts the Gray Scale by ≈11% in the high (white) direction. Typically this function is used to provide an enhanced, or brighter display so as to highlight certain portions of the screen. A highlighted cursor is a typical example.

The current change at each output is equal to:

$$\Delta I_{O(BRT)} = I_{ref} \times 1.74$$

The current at I_{O-} decreases in magnitude, while the current at I_{O+} increases, when BRT is asserted. BRT is ineffective when Sync or BLK are asserted, but can be used at any point within the Gray Scale.

The Blank input (BLK) sets the output currents to the blanking level used during horizontal and vertical retrace. The current at Out – is:

$$I_{O-}(BLK) = I_{ref} \times 18.96$$

The current at Out + is:

$$I_{O+}(BLK) = I_{ref} \times 6.9$$

The BLK input will override the data inputs, FH and BRT, but is overridden by Sync. Therefore, the BLK input may be left asserted during the sync time.

The Synchronizing input (Sync) sets the output currents to the sync level used for normal horizontal and vertical picture synchronization.
The current at Out – is:

$$I_{O-}(Sync) = I_{ref} \times 25.86$$

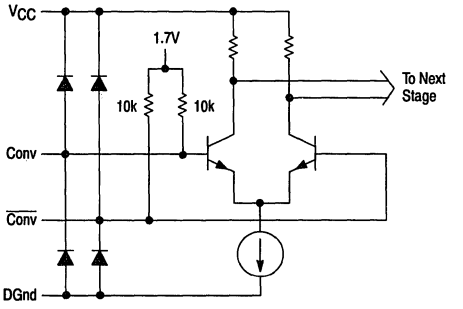
The current at Out + will be leakage current only, typically < 20 μA. The Sync input will override all other control inputs as well as data inputs.

Feedthrough (FT) Input

With FT low, the internal registers are active, and the data and video controls are clocked through to the DAC on the rising edge of Pin 6 (Conv), or on the falling edge of Pin 7. In this mode, the data bits (D7 – D0) which may appear asynchronously to the MC10322 are then presented synchronously to the DAC, reducing output glitches and noise. This mode is also useful for synchronizing control functions with other events. While hold times are typically 0 ns for all inputs, the setup times prior to the clock edge must be observed.

With FT high, the registers are transparent and the data and video controls feed through directly to the DAC. This mode may be used if the data is presented to the MC10322 from external latches, which ensure minimum skew among the data bits. In this mode Pins 6 and 7 are not used.

Figure 5. Convert Input Stage



Convert Inputs

The Convert inputs (Pins 6 and 7) are used to clock in data and the video controls to the internal registers only if FT (Pin 8) is low. The input stage for these pins is shown in Figure 5. The pins are internally biased at ≈ +1.6 V with a nominal input impedance of 10 kΩ. The inputs may be driven from complementary TTL clock signals with the clocking action occurring on the rising edge of Conv and the falling edge of $\overline{\text{Conv}}$ as the signals cross each other in voltage.

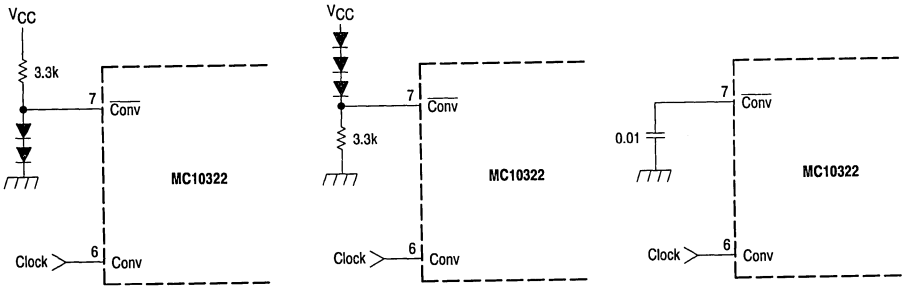
A single-ended clock source may be used by connecting either Pin 6 or 7 to a fixed voltage to set the threshold and applying the clock signal to the other pin. If done this way, the fixed voltage must be within the range of +1.3 V to V_{CC} – 2.0 V. Figure 6 shows three positive edge triggered examples. Interchanging Pins 6 and 7 provides negative edge triggered operation.

The input current required at each pin is shown in Figure 9, and is independent of the clocking mode used.

If FT is high, the Convert pins are nonfunctional, and **must** be connected to **different** voltages (e.g., V_{CC} and DGnd). Leaving the pins open can result in high frequency oscillations or spurious noise.

Conv and $\overline{\text{Conv}}$ must be kept within the range of V_{CC} and DGnd. If taken more than 0.5 V above V_{CC} or below Gnd excessive currents will flow, and the DAC output waveform will be distorted.

Figure 6. Single-Ended Clock Input



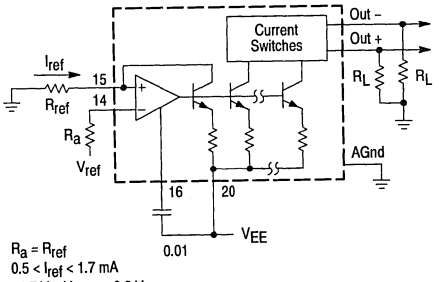
Reference Amplifier

The reference amplifier (Pins 14 to 16) is used to accept the externally supplied reference current for the DAC current switches (see Figure 7).

Ref + (Pin 15) is a low impedance (virtual ground) input into which the reference current flows (current cannot flow out of this pin). Due to the op amp's internal feedback, the voltage at Ref + is the same as that set at Ref –, with a typical input offset of ± 5.0 mV. The current into Ref + should be within the range of 0.5 mA to 1.7 mA to maintain 8-bit linearity and accuracy. A reference current of 1.115 mA is recommended to obtain EIA-170 and EIA-343-A voltage levels at the outputs if they are terminated with 37.5 Ω (double 75 Ω terminations).

Ref – is a high impedance input (>10 MΩ) which must be set to a voltage within the range of – 0.8 to –1.7 V. A nominal bias current of ≈1.4 μA will flow into this pin. In Figure 7, $I_{ref} = V_{ref}/R_{ref}$.

Figure 7. Reference Amplifier



Power Supplies

The MC10322 requires both a + 5.0 V and a − 5.2 V supply, both ± 10%. Nominal current requirements are 22 mA and 45 mA, respectively, (including a total output current of 29 mA). The supply current required at V_{EE} is dependent on the total output current (Pin 18 + Pin19). The + 5.0 V supply powers only the digital portion of the IC (control logic and latches), and should be referenced to Digital Ground (Pin 5). The − 5.2 V supply powers the analog portion of the IC (reference amplifier and the DAC's current sources), and should be referenced to Analog Ground (Pin 17). See the Applications Section for additional information on power supplies, bypassing and PC board layout.

Timing

Figures 2 and 3 are the timing diagrams for the MC10322. Figure 2 is for the clocked mode where data and control inputs are latched into the input registers by the Convert (and/or $\overline{\text{Convert}}$) inputs. If the clock signal is single-ended, the data and control latching occurs on the rising edge of Convert, or the falling edge of $\overline{\text{Convert}}$. If a differential clock is used, latching occurs at the cross-over point of the two signals. The hold time for the data and controls is 0, but the setup times must be observed. The clock duty cycle is not important as long as the minimum pulse widths are observed.

Figure 3 is for the transparent (non-clocked) mode. The output responds to the application of new data or control inputs without the need for a clocking edge. The propagation delay to the output is different for each of the data and control signals. To prevent large glitches at the outputs, it is imperative that the data bits (D0 – D7) arrive at the MC10322 simultaneously with minimum skew. If the synchronism of the 8-bits cannot be guaranteed, either an 8-bit latch should be used (F373 or F374 type), or the MC10322 should be used in the clocked mode.

Figure 8. Input Current, Data and Controls

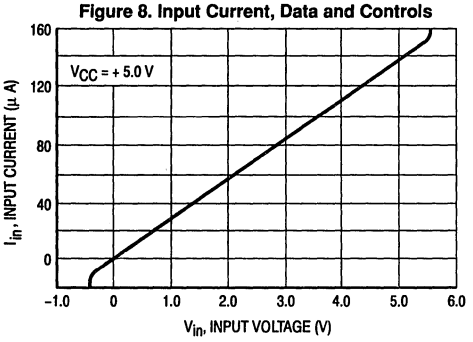
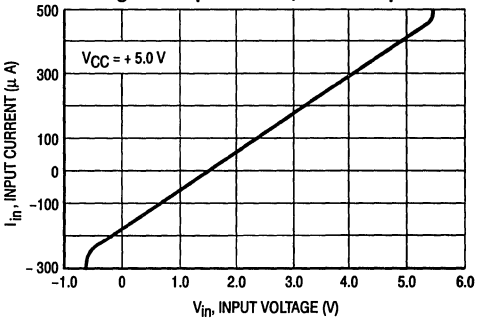


Figure 9. Input Current, Convert Inputs



APPLICATIONS INFORMATION

Power Supplies, Grounding

The PC board layout and the quality of the power supplies and the ground system **at the IC** are very important in order to obtain proper operation. Noise from any source coming into the device on V_{CC}, V_{EE}, or ground can cause an incorrect output code due to interaction with the analog portion of the circuit. At the same time, noise generated within the MC10322 can cause incorrect operation if that noise does not have a clear path to AC ground.

Both the V_{CC} and V_{EE} power supplies must be decoupled to the appropriate ground **at the IC** (within 1″ max) with a 10 μF tantalum and a 0.1 μF ceramic. Tantalum capacitors are recommended since electrolytic capacitors simply have too much inductance at the frequencies of interest. The quality of the V_{CC} and V_{EE} supplies should then be checked at the IC with a high frequency scope. Noise spikes (whenever digital circuits are present) can easily exceed 400 mV peak, and if they get into the analog portion of the IC, the operation can be disrupted. Noise can be reduced by inserting resistors and/or inductors between the supplies and the IC.

If switching power supplies are used, there will usually be spikes of 0.5 V or greater at frequencies of 50 kHz to 1.0 MHz. These spikes are generally more difficult to reduce because of their greater energy content. In extreme cases three terminal regulators (MC78L05ACP, MC7905.2CT), with appropriate high frequency filtering should be used and dedicated to the MC10322.

The ripple content of the supplies should not allow their magnitude to exceed the values in the Recommended Operating Conditions.

The PC board tracks supplying V_{CC} and V_{EE} to the MC10322 should preferably not be at the tail end of the bus distribution after passing through a maze of digital circuitry. The MC10322 should be close to the power supply, or the connector where the supply voltages enter the board. If the V_{CC} and V_{EE} lines are supplying considerable current to other parts of the board, then it is preferable to have dedicated lines from the supply or connector directly to the MC10322.

The two ground pins (DGnd and AGnd) must eventually be connected together, usually near the power supply, although the specific board layout may dictate a different "best point", V_{CC} must be referenced to DGnd, and V_{EE} must be referenced to AGnd.

PC Board Layout

Due to the high frequencies involved, and in particular, the fast edges of the various digital signals, proper PC board layout is imperative. A solid ground plane is strongly recommended in order to have known transmission characteristics, and also to minimize coupling of the digital signals into the analog section. Use of wire wrapped boards should definitely be avoided.

Each PC track should be considered a transmission line, and if they are of any considerable length (more than a few inches), they should be terminated according to transmission line theory. Otherwise reflections back to the signal sources can occur, disrupting their operation. Additionally, the overshoots and undershoots which will occur at the MC10322's input pins can cause its operation to be disrupted, resulting in a noisy or incorrect output.

Additional information regarding the transmission characteristics of PC board tracks can be found in Motorola's MECL System Design Handbook (HB205).

Reference Circuits

Since the accuracy of the outputs are directly related to the accuracy and quality of the reference current and voltage, it is imperative that accurate and stable references be used at Pins 14 and 15. The voltage supply used for the digital circuitry should preferably **not** be used as a source for either the reference current or voltage due to the noise spikes and ripple present on the supply and its ground lines.

Figure 10 indicates a method for generating the reference signals from a positive supply. The MC1403 reference is a stable 2.5 V bandgap regulator (± 1%), with a maximum temperature coefficient of 40 ppm/°C, and good ripple and high frequency noise rejection. In the figure, the circuit supplies –1.48 V to Pin 14, and a current of 1.113 mA to Pin 15. If the outputs of the MC10322 are terminated with 37.5 Ω, the voltage levels will be well within the allowable range specified by EIA-170 and EIA-343-A.

Figure 10. Reference Supply

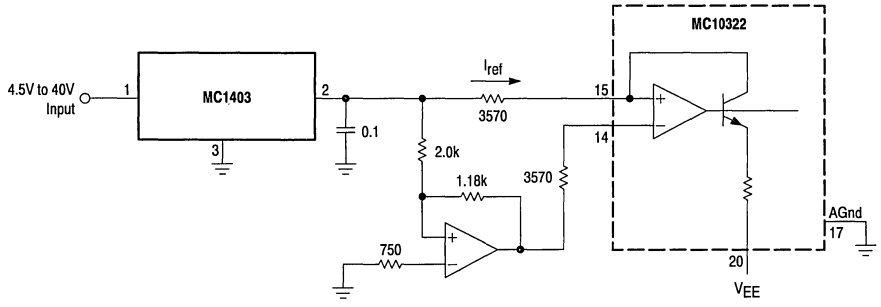


Figure 11. Reference Supply

If the analog – 5.2 V supply is fairly clean and free of digital noise the circuit of Figure 11 may be used. The TL431 is a stable 2.5 V bandgap reference (± 1%) with an effective temperature coefficient of 50 ppm/°C. The 5 k pot allows adjustment for precise output levels, or it may be replaced with a precision resistor which provides the correct voltage at Pin 14.

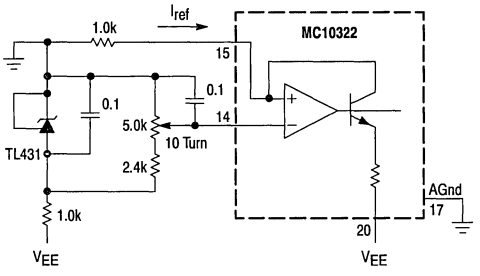
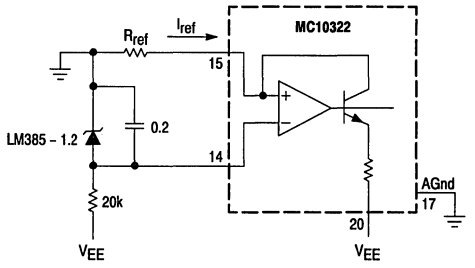


Figure 12 indicates another reference circuit using the LM385–1.2 reference diode. R_{ref} is chosen to provide the desired reference current to Pin 15 knowing that it is set at –1.235 V. The LM385 is a bandgap type reference with a ± 2% initial accuracy. The 20 k resistor biases the diode at approximately 200 μA for minimum temperature variations. The 0.2 μF capacitor, with the 20 k resistor, filters out noise above ≈ 40 Hz.

Figure 12. Reference Supply



6

Digitally Modulating an Analog Signal

The MC10322 may be used to digitally modulate (or attenuate) an analog signal by applying the analog signal to the reference amplifier. Three methods of doing this are shown in Figures 13 to 15.

Figure 13. Applying an Analog Signal Directly

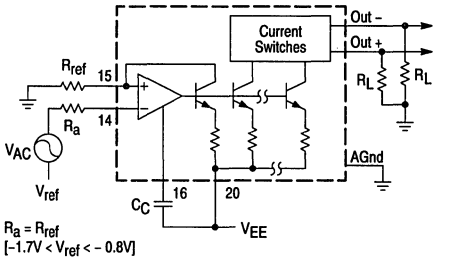


Figure 14. Capacitor Coupling the AC Voltage

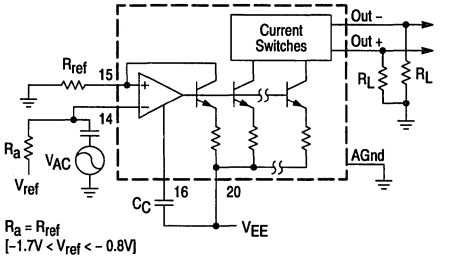
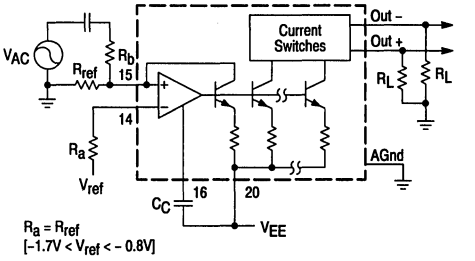


Figure 15. Applying a Modulating Current



In all three examples the DC reference current is V_{ref}/R_{ref}. In Figure 13 the AC signal source is referenced to a negative voltage source (V_{ref}). In Figures 13 and 14 the AC reference current is equal to V_{AC} divided by R_{ref}. In Figure 15 the AC reference current is equal to V_{AC} divided by R_b. The AC signal at Out – and Out + is determined by the following equations:

$$V_{O-(AC)} = \frac{I_{ref(AC)} \times (255\text{-}A) \times R_L}{16}$$

$$V_{O+(AC)} = \frac{I_{ref(AC)} \times A \times R_L}{16}$$

where "A" is the value of the digital word at D0 – D7 (0 to 255).

When implementing any of the above schemes, or any other method of feeding an AC signal to the reference amplifier, the following operating limits must be observed:

1) The peak values of the reference current (AC + DC) must be within the range of 0.5 mA to 1.7 mA into Pin 15;
2) The peak values of the voltage at Ref + and Ref – must be within the range of – 0.8 V to –1.7 V;
3) The peak values of the voltage at Out – and Out + must be within the range of –1.7 V to + 0.3 V.

The maximum frequency which can be handled by the reference amplifier is dependent on the compensation capacitor (C_C) at Pin 16, and the signal amplitude according to the following equation:

$$f_{max} = \frac{1.59 \times 10^{-8}}{C_C \times I_{pk}}$$

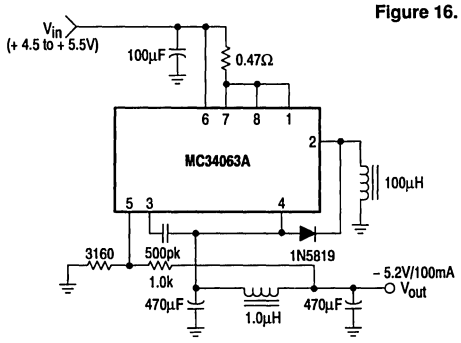
where I_{pk} is the peak value of the AC reference current (1/2 of the peak-to-peak value). The small signal bandwidth of the reference amplifier is ≈ 3.0 MHz.

Components associated with the reference amplifier (Pins 14 – 16) should be physically close to the pins. The board layout should be neat, preventing unwanted stray capacitive coupling between the outputs and the reference amplifier. If C_C is smaller than 5000 pF a ground plane is strongly recommended. C_C should not be smaller than 250 pF.

Negative Voltage Regulator

In the case where a negative power supply is not available, neither the – 5.2 V, nor a higher negative voltage from which to derive it, the circuit of Figure 16 can be used to generate – 5.2 V from the + 5.0 V supply. The PC board space required is small (≈ 2.0 in^2), and it can be located physically close to the MC10322. The MC34063A is a switching regulator, and in Figure 16 is configured in an inverting mode of operation. The regulator operating specifications are given in Figure 16.

Figure 16. – 5.2 V Regulator



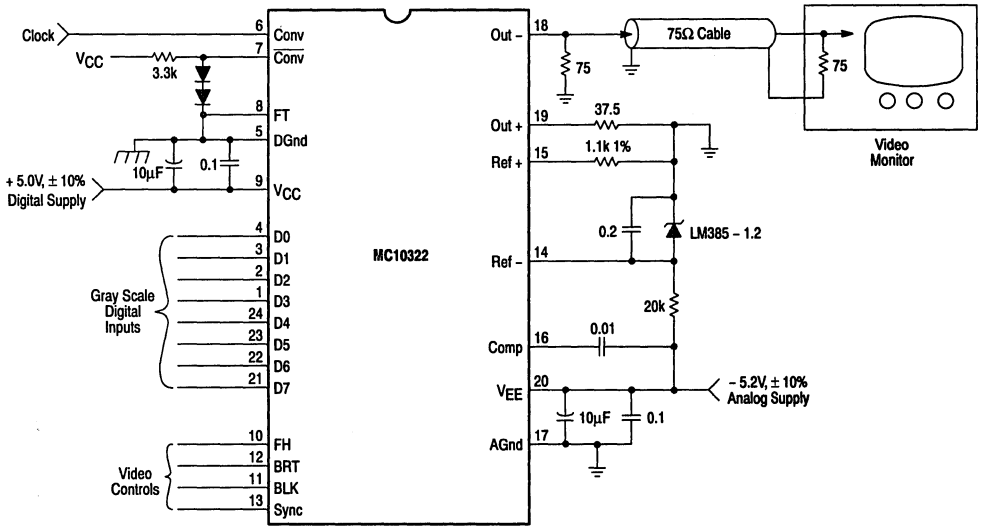
Line Regulation	4.5 V < V_{in} < 5.5 V, I_{out} = 50 mA	0.04%
Load Regulation	V_{in} = 5.0 V, 15 mA < I_{out} < 85 mA	1.5%
Output Ripple	V_{in} = 5.0 V, I_{out} = 85 mA	4.0 mVp-p
Short Circuit I_{out}	V_{in} = 5.0 V, R_L = 1.0 Ω	620 mA
Efficiency	V_{in} = 5.0 V, I_{out} = 50 mA	48%

6

TYPICAL APPLICATION CIRCUITS

Figure 17 shows a typical video application circuit using the MC10322 in the clocked mode. The clock is single-ended, and the circuit updates the output on the rising edge of the clock. The Out - pin feeds a standard 75 Ω monitor through a 75 Ω cable, which is terminated at both ends. The reference voltage is supplied by an LM385–1.2 regulator.

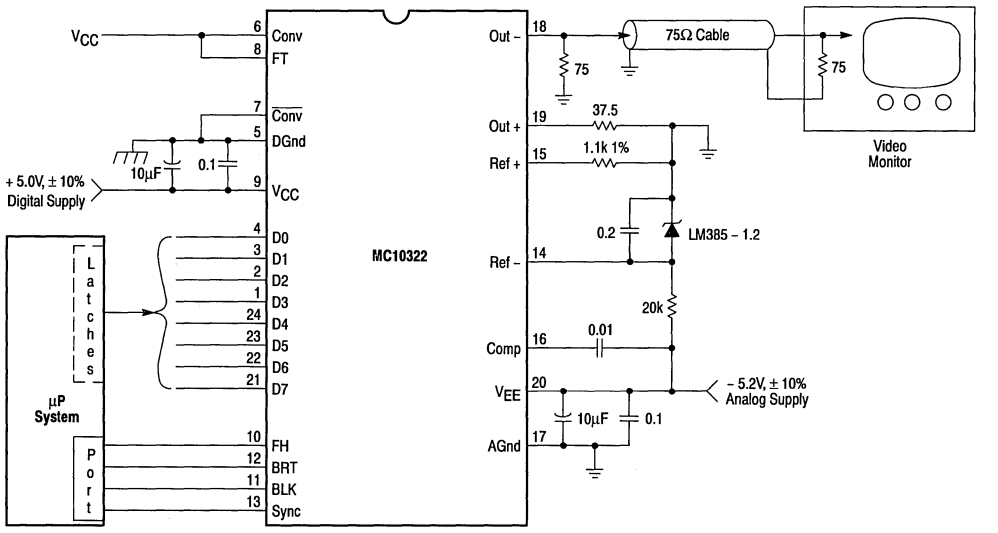
Figure 17. Clocked Mode



NOTES: 1. Gray Scale inputs, video controls, and clock are to be referenced to digital ground.
2. Outputs and reference circuitry are to be referenced to analog ground.
3. PC board layout to be such that digital noise does not get into the analog side circuitry.
4. Analog and digital grounds to be connected together. Location of this connection is board layout dependent,and is to be such that digital ground noise does not show up in the analog signals.

Figure 18 shows a circuit similar to that of Figure 17, except the MC10322 is used in the transparent mode. The source of the data bits must provide the 8-bits simultaneously, with minimum skew, to keep output glitches to a minimum. If latches, or other antiskew circuitry, are not available within the microprocessor circuitry, a set of 8-bit latches between it and the MC10322 is recommended, or the MC10322 should be used in the clocked mode.

Figure 18. Transparent Mode



NOTES: 1. Gray Scale inputs and video controls are to be referenced to digital ground.
2. Outputs and reference circuitry are to be referenced to analog ground.
3. PC board layout to be such that digital noise does not get into the analog side circuitry.
4. Analog and digital grounds to be connected together. Location of this connection is board layout dependent,and is to be such that digital ground noise does not show up in the analog signals.

GLOSSARY

Bandgap Reference – A voltage reference circuit based on the predictable base-emitter voltage of a transistor. The silicon bandgap voltage of ≈1.2 V is the basis for generating other voltages which are stable with time and temperature.

Bipolar Input – A mode of operation whereby the analog input (of an A-D), or output (of a DAC), includes both negative and positive values. Examples are: – 5.0 V to + 5.0 V, – 2.0 V to + 8.0 V, etc.

DAC Current Gain – The internal gain the DAC applies to the reference current to determine the full scale output current. The actual maximum current out of a DAC is one LSB less than the full scale current.

Differential Gain – In video systems, differential gain is a component's change in gain as a function of luminance level. In a color picture, contrast will be affected if the differential gain is not zero.

Differential Nonlinearity – The maximum deviation in the actual step size (one transition level to another) from the ideal step size. The ideal step size is defined as the Full Scale Range divided by 2^n. This error must be within ± 1 LSB for proper operation.

Differential Phase – In video systems, differential phase is the change in the phase modulation of the chrominance as a function of the luminance level. The hue in a color picture will be distorted if the differential phase is not zero.

Full Scale Range – The difference between the minimum and maximum end points of the analog input (of an A/D), or output (of a DAC), plus one LSB.

Gain Error – The difference between the actual and expected gain (end point to end point), with respect to the reference, of a data converter. The gain error is usually expressed in LSBs, or percent.

Glitch Area – The energy content of a glitch, specifically in volt-seconds. It is the area under the curve of the glitch waveform. For a symmetrical glitch, the area and the energy can be zero.

Gray Code – Also known as *reflected binary code*, it is a digital code such that each code differs from adjacent codes by only one bit. Since more than one bit is never changed at each transition, race condition errors are eliminated.

Integral Nonlinearity – The maximum error of an A/D or DAC, transfer function from the ideal straight line connecting the analog end points. This parameter is sensitive to dynamics, and test conditions must be specified in order to be meaningful. This parameter is the best overall indicator of the device's performance.

LSB – Least Significant Bit. It is the lowest order bit of a binary code.

Line Regulation – The ability of a voltage regulator to maintain a certain output voltage as the input to the regulator is varied. The error is typically expressed as a percent of the nominal output voltage.

Load Regulation – The ability of a voltage regulator to maintain a certain output voltage as the load current is varied. The error is typically expressed as a percent of the nominal output voltage.

Monotonicity – The characteristic of the transfer function whereby increasing the input code (of a DAC), or the input signal (of and A/D), results in the output never decreasing. Nonmonotonicity occurs if the differential nonlinearity exceeds ± 1 LSB.

MSB – Most Significant Bit. It is the highest order bit of a binary code.

Natural Binary Code – A binary code defined by:

$N = A_n2^n + ... + A_32^3 + A_22^2 + A_12^1 + A_02^0$

where each "A" coefficient has a value of 1 or 0. Typically, all zeros correspond to a zero input voltage of an A/D, and all ones correspond to the most positive input voltage.

Nyquist Theory – See Sampling Theorem.

Offset Binary Code – Applicable only to bipolar input (or output) data converters, it is the same as Natural Binary code, except that all zeros correspond to the most negative output signal (of a D/A), while all ones correspond to the most positive output.

Output Compliance – The maximum voltage range to which the DAC outputs can be subjected, and still meet all specifications.

Power Supply Rejection Ratio – The ability of a device to reject noise and/or ripple on the power supply pins from appearing at the outputs. An AC measurement, this parameter is usually expressed in dB rejection.

Power Supply Sensitivity – The change in a data converter's performance with changes in the power supply voltage(s). This parameter is usually expressed in percent of full scale versus ΔV.

Propagation Delay – For a DAC, the time from when the clock input crosses its threshold to when the DAC output(s) changes.

Quantitization Error – Also known as *digitization error* or uncertainty. It is the inherent error involved in digitizing an analog signal due to the finite number of steps at the digital output versus the infinite number of values at the analog input. This error is a minimum of ± 1/2 LSB.

Resolution – The smallest change which can be discerned by an A/D converter, or produced by a DAC. It is usually expressed as the number of bits (n), where the converter has 2^n possible states.

Sampling Theorem – Also known as the *Nyquist Theorem.* It states that the sampling frequency of an A/D must be no less than 2x the highest frequency (of interest) of the analog signal to be digitized in order to preserve the information of that analog signal.

Settling Time – For a DAC, the time required for the output to change (and settle in) from an initial ±1/2 LSB error band to the final ± 1/2 LSB error band.

TTL – Transistor-transistor logic.

Two's Complement Code – A binary code applicable to bipolar operation, in which the positive and negative codes of the same analog magnitude sum to all zeros, plus a carry. It is the same as *offset binary code*, with the MSB inverted.

Unipolar Input – A mode of operation whereby the analog input range (of an A/D), or output range (of a D/A), includes values of a single polarity. Examples are:
0 to +10 V, 0 to – 5.0 V, + 2.0 V to + 8.0 V, etc.

Additional information regarding the transmission characteristics of PC board tracks can be found in Motorola's MECL System Design Handbook (HB205).

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC10324

Advance Information

8-Bit Video DAC with ECL Inputs

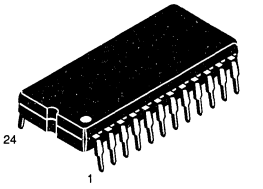
8-BIT VIDEO DAC with ECL INPUTS

SILICON MONOLITHIC INTEGRATED CIRCUIT

The MC10324 is a 40 MegaSample Per Second (MSPS) 8-bit Video DAC capable of directly driving a 75 Ω cable, with appropriate terminations, to EIA-170 and EIA-343-A video levels. The logic inputs (data and controls) are ECL compatible. Input registers negate the need for external latches unless the transparent mode is selected.

Video controls (Force High, Blank, Bright, and Sync) permit an easy interface to standard video systems. The Clock (Convert) inputs can be differential or single-ended. Complementary outputs are provided for custom displays or special effects.

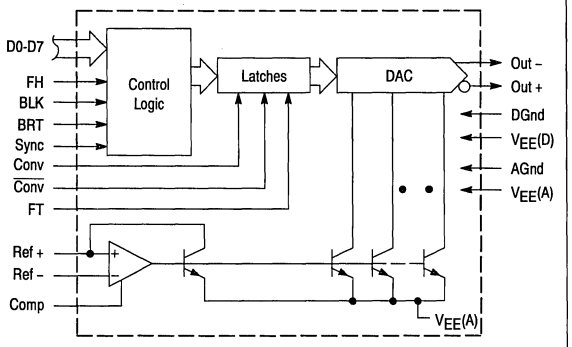
The MC10324 is fabricated with Motorola's MOSAIC™ process which provides high speed with low power consumption. The MC10324 is available in a 24 pin plastic DIP package.



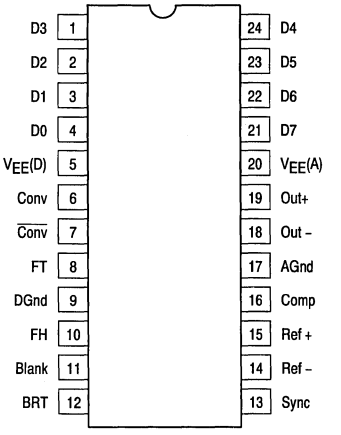
P SUFFIX
PLASTIC PACKAGE
CASE 649

- 40 MSPS Minimum Conversion Rate
- ECL Compatible Inputs
- 8-Bit Linearity
- Latched Data and Video Control Inputs, or Transparent Mode
- Video Controls: Force High, Blank, Bright, Sync
- Each Differential Current Outputs Can Swing 2.0 V
- Modulation Capability (Multiplying Mode)
- PSRR > 60 dB
- Standard Power Supply: – 5.2 V
- Power Dissipation: Typically 338 mW
- Pin Compatible with TRW's TDC1018
- Available with TTL Inputs (MC10322)

Simplified Block Diagram



PIN CONNECTIONS

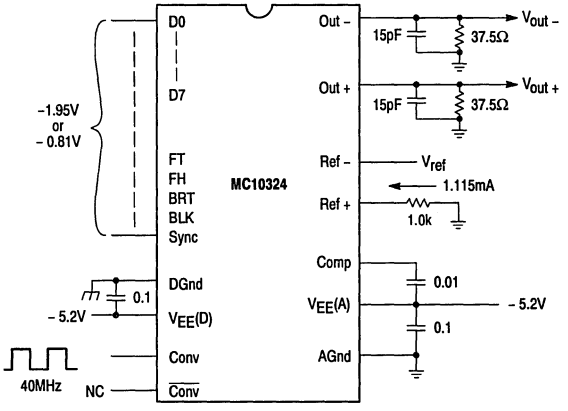


(Top View)

PIN FUNCTION DESCRIPTION

Symbol	Pin	Description
D0-D7	1-4, 21-24	Data inputs. D0 is the LSB and D7 is the MSB. Inputs are ECL compatible. Maximum update rate is typically 60 MHz. The eight bits control the Gray Scale amplitude only, and do not involve the Sync or Blank levels.
V_{EE}(D)	5	Connect to – 5.2 V, ± 10%. This supply should be referenced to digital ground.
Conv	6	Convert input. The rising edge latches data and controls if FT = 0. May be used single-ended (with Pin 7 at a fixed voltage), or differentially with Pin 7.
$\overline{\text{Conv}}$	7	$\overline{\text{Convert}}$ input. The falling edge latches data and controls if FT = 0. May be used single-ended (with Pin 6 at a fixed voltage), or differentially with Pin 6.
FT	8	Feedthrough. When high, the internal latches are transparent, and Pins 6 and 7 are unused. When low, data and controls are latched by Pins 6 and 7.
DGnd	9	Connect to system digital ground. This pin must be within 100 mV of AGnd (Pin 17).
FH	10	Force High. A logic high internally sets data inputs = 1, overriding external data inputs.
Blank	11	A logic high overrides data inputs, sets the outputs to the video blanking level.
BRT	12	Bright. A logic high increases the Gray Scale output level by ≈ 11%, providing an enhanced display. Does not affect Sync or Blank.
Sync	13	A logic high overrides all other inputs, and sets the output to video sync level.
Ref –	14	Inverting Reference input. A high impedance input, normally set to a negative DC voltage in the range of – 0.8 to –1.7 V. Can be used to modulate the output.
Ref +	15	Noninverting reference input. A virtual ground, current supplied to this pin sets the maximum output current.
Comp	16	Compensation. A capacitor between this pin and Pin 20 stabilizes the reference amp.
AGnd	17	Connect to system analog ground. This pin must be within 100 mV of DGnd (Pin 9).
Out –	18	A high impedance current output. Video voltage levels are produced when connected to a 75 Ω cable with appropriate terminations. This output provides a "sync down" waveform. If unused, connect to Pin 17.
Out +	19	Complementary output provides a "sync up" waveform. If unused, connect to Pin 17.
V_{EE}(A)	20	Connect to – 5.2 V, ± 10%. This supply should be referenced to analog ground.

Figure 1. Test Circuit



MAXIMUM RATINGS

Characteristics	Value	Unit
V_{EE}(D) (with respect to DGnd)	– 7.0, + 0.5	Vdc
DGnd (with respect to AGnd)	–1.0, + 0.5	Vdc
V_{EE}(A) (with respect to AGnd)	– 7.0, + 0.5	Vdc
Logic Input Voltage (with respect to DGnd)	+ 0.5	Vdc
Logic Input Voltage (with respect to V_{EE}(D))	– 0.5	Vdc
Voltage at Reference Amp Inputs	+ 0.5, V_{EE}(A)	Vdc
Current Into Ref +	+ 6.0, 0	mA
Voltage Applied to Out +, Out – (Normal Operation)	+ 0.5, – 2.0	Vdc
Voltage Applied to Out +, Out – (V_{EE}(D), V_{EE}(A) = 0)	+ 0.5, – 1.2	Vdc
Junction Temperature	– 65 to +150	°C

Devices should not be operated at these values. The "Recommended Operating Conditions" table provides conditions for actual device operation.

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{EE}(D) — DGnd DGnd — AGnd V_{EE}(A) — AGnd	– 5.72 – 0.1 – 5.72	– 5.2 0 – 5.2	– 4.68 + 0.1 – 4.68	Vdc
Logic Input Voltage	V_{in}	V_{EE}(D)	—	DGnd	Vdc
Reference Current (for Video Standard Output) (for all other applications)	I_{ref}	— 0.5	1.115 —	— 1.7	mA
Voltage at Ref –	V_{ref} –	–1.7	—	– 0.8	Vdc
Output Load Impedance	R_L	0	37.5	—	Ω
Output Compliance (with respect to AGnd)	V_O	–1.7	—	+ 0.3	Vdc
Convert Frequency (FT = 0) Data Update Frequency (FT = 1)	f_s	0 0	60 60	40 40	MHz
Convert, $\overline{\text{Convert}}$ Common Mode Range	V_{CM}	V_{EE}(D)+1.3	—	DGnd – 0.3	Vdc
Operating Ambient Temperature	T_A	– 40	—	+ 85	°C

All limits are not necessarily functional concurrently.

ELECTRICAL CHARACTERISTICS (T_A = 25°C, I_{ref} = 1.115 mA, Load = 37.5 Ω to AGnd, V_{CC} = V_{EE} = – 5.2 V, see Figure 1.)

Characteristic	Symbol	Min	Typ	Max	Unit
REFERENCE AMPLIFIER					
Input Offset (Ref + to Ref –)	V_{OS}	–15	± 5.0	+15	mV
Bias Current Into Ref –	I_{BR}	—	1.4	5.0	µA
Bandwidth (C_C = 250 pF, V_{ref} – = 10 mVp-p)	BW	—	3.0	—	MHz
DIGITAL INPUTS					
Low Voltage	V_{IL}	–1.95	—	–1.6	Vdc
High Voltage	V_{IH}	–1.13	—	– 0.81	Vdc
Low Current (Data, Controls @ –1.95 V)	I_{IL}	—	90	150	µA
High Current (Data, Controls @ – 0.81)	I_{IH}	—	120	200	µA
Low Current (Conv, $\overline{\text{Conv}}$ @ –1.95)	I_{IL}	–150	– 60	—	µA
High Current (Conv, $\overline{\text{Conv}}$ @ – 0.81)	I_{IH}	—	80	150	µA
Input Capacitance	C_{in}	—	5.0	—	pF

NOTES: 1. Current into a pin is designated as positive, current out of a pin as negative.
2. Controls = FH, BRT, BLK, Sync, and FT.

ELECTRICAL CHARACTERISTICS (T_A = 25°C, I_{ref} = 1.115 mA, Load = 37.5 Ω to AGnd, V_{CC} = V_{EE} = – 5.2 V, see Figure 1.)

Characteristic	Symbol	Min	Typ	Max	Unit
TRANSFER CHARACTERISTICS					
Resolution	Res	8.0	8.0	8.0	Bits
Integral Nonlinearity	INL	–1/2	0	+1/2	LSB
Differential Nonlinearity	DNL	–1/2	0	+1/2	LSB
Monotonicity	—		Guaranteed*		
Differential Gain	DG	—	1.0	—	%
Differential Phase	DP	—	0.5	—	Deg
					*Guaranteed by linearity tests.
OUTPUTS					
Output Current at Out – (Control Inputs = 0 Except as Noted)					
Enhanced White (FH = BRT = 1)	I_{EH-}	0	18	100	µA
Normal White (FH = 1 or D0 – D7 = 1)	I_{NW-}	1.75	1.94	2.13	mA
Normal Black (D0 – D7 = 0) Referred to Normal White	I_{NB-}	16.6	17.7	18.7	
Blank Referred to Normal Black (BLK = 1)	I_{BLN-}	1.32	1.43	1.54	
Sync Referred to Blank (SYNC = 1)	I_{SYNC-}	7.1	7.7	8.3	
Output Voltage at Out – (Control Inputs = 0 Except as Noted)					mV
Enhanced White (FH = BRT = 1)	V_{EH-}	0	– 0.67	– 3.75	
Normal White (FH = 1 or D0 – D7 = 1)	V_{NW-}	– 67.8	– 73	– 77.6	
Normal Black (D0 – D7 = 0) Referred to Normal White	V_{NB-}	– 626	– 663	– 694	
Blank Referred to Normal Black (BLK = 1)	V_{BLN-}	– 50.6	– 53.6	– 56.6	
Sync Referred to Blank (SYNC = 1)	V_{SYNC-}	– 270	– 288	– 308	
Output Current at Out + (Control Inputs = 0 Except as Noted)					mA
Enhanced White (FH = BRT = 1)	I_{EH+}	26.8	28.8	30.6	
Normal White (FH = 1 or D0 – D7 = 1)	I_{NW+}	25	26.8	28.5	
Normal Black (D0 – D7 = 0) Referred to Normal White	I_{NB+}	–16.6	–17.7	–18.7	
Blank Referred to Normal Black (BLK = 1)	I_{BLN+}	–1.32	–1.43	–1.54	
Sync Referred to Blank (SYNC = 1)	I_{SYNC+}	– 7.1	– 7.7	– 8.3	
Output Voltage at Out + (Control Inputs = 0 Except as Noted)					mV
Enhanced White (FH = BRT = 1)	V_{EH+}	–1016	–1080	–1132	
Normal White (FH = 1 or D0 – D7 = 1)	V_{NW+}	– 949	–1005	–1057	
Normal Black (D0 – D7 = 0) Referred to Normal White	V_{NB+}	626	663	694	
Blank Referred to Normal Black (BLK = 1)	V_{BLN+}	50.6	53.6	56.6	
Sync Referred to Blank (SYNC = 1)	V_{SYNC+}	270	288	308	
Output Matching ($\lvert I_{NB+} \rvert - \lvert I_{NB-} \rvert$)	I_{FSER}	– 50	0	+ 50	µA
Gain Error (Gray Scale at Out –)	G_{ER}	– 50	0	+ 5.0	%
Output Impedance (Gray Scale, –1.7 V < V_O < 0.3 V)	Z_O	25	100	—	kΩ
Output Capacitance	C_O	—	16	—	pF
Glitch Energy (Clocked Mode)					pV-sec
At Midscale Transition (D0 – D7 = 127↔128)	E_{GM}	—	18	—	
Due to Clock Feedthrough (D0 – D7 = Constant)	E_{GC}	—	2.0	—	
Due to Data Feedthrough (Clock = Constant)	E_{GD}	—	25	—	
Peak Glitch Current (Clocked Mode)					
At Midscale Transition (D0 – D7 = 127↔128)	I_{GM}	—	0.2	—	mA
Due to Clock Feedthrough (D0 – D7 = Constant)	I_{GC}	—	55	—	µA
Due to Data Feedthrough (Clock = Constant)	I_{GD}	—	0.5	—	mA
POWER SUPPLIES					
Supply Current $V_{EE}(D)$ = $V_{EE}(A)$ = – 5.72 V	$I_{EE}(D)$	– 80	– 65	—	mA
Power Dissipation	P_D	—	338	458	mW
Power Supply Sensitivity at Outputs (– 5.72 < $V_{EE}(D)$, $V_{EE}(A)$ < – 4.68 V)	PSSD	–100	20	+100	µA/V
$V_{EE}(D)$ Supply Rejection ($V_{EE}(D)$ = $V_{EE}(A)$ = – 5.2 V, f = 10 kHz)	PSRRD	—	100	—	dB
$V_{EE}(A)$ Supply Rejection ($V_{EE}(D)$ = $V_{EE}(A)$ = – 5.2 V, f = 10 kHz)	PSRRA	—	60	—	dB

(continued)

TIMING CHARACTERISTICS (T_A = 25°C, I_{ref} = 1.115 mA, Load = 37.5 Ω//15 pF, V_{CC} = V_{EE} = – 5.2 V, see Figures 2, 3.)

Characteristic	Symbol	Min	Typ	Max	Unit
Maximum Conversion or Update Rate	F_S	40	60	—	MHz
Clocked Mode (FT = 0)					ns
Clock to Output Delay (Data, Controls)	t_{COD}	—	10	—	
Setup Time — Data to Conv Rising Edge	t_{SD}	—	8.0	—	
FH, Sync to Conv Rising Edge	t_{SFS}	—	5.0	—	
BRT, BLK to Conv Rising Edge	t_{SB}	—	4.0	—	
Hold Time — All Inputs (After Conv Rising Edge)	t_H	—	0	—	
Minimum Clock Width (High or Low)	t_{PW}	—	6.0	—	
Transparent Mode (FT = 1)					ns
Data to Output Delay	t_{DO}	—	16	—	
Sync to Output Delay	t_{SO}	—	13	—	
BLK to Output Delay	t_{BO}	—	14	—	
FH to Output Delay	t_{FO}	—	16	—	
BRT to Output Delay	t_{RO}	—	12	—	
Output Rise/Fall Time — 10 to 90% of Gray Scale	t_{RFG}	—	2.0	—	ns
Enhanced White to Sync Level	t_{RFF}	—	3.0	—	
Output Settling Time	t_{SET}	—	4.0	—	ns

FUNCTIONAL DESCRIPTION

Introduction

The MC10324 is an 8-bit DAC intended for video applications, employing ECL inputs for the data (natural binary code) and video controls, and outputs capable of directly driving a standard 50 Ω or 75 Ω monitor. Its use is not limited to video, however, any application requiring a high speed DAC (typically 60 MHz) or a DAC with high output current capability (up to 44 mA) can use the MC10324. The input data and controls may be clocked into the internal registers, or the MC10324 may be used in the transparent mode eliminating the need for the clock.

The MC10324 may be used in the multiplying mode by varying the reference current along with the digital inputs producing the product of the two at the outputs. The reference current can be varied over a range of 0.5 to 1.7 mA. The MC10324 requires – 5.2 V, ± 10% for both the analog and digital supply pins. Power consumption is nominally 338 mW.

DAC Outputs

The outputs of the MC10324 are high impedance constant current sinks whose values depends on the reference current (I_{ref}), the binary value of the digital word at D0 – D7, and the status of the video controls (Sync, BLK, FH, and BRT). Complementary outputs are provided allowing an increased output swing (when used differentially), or for creation of special effects required by the application. For a given reference current, the sum of the two output currents is a constant equal to:

$$(I_O -) + (I_O +) = I_{ref} \times 25.86$$

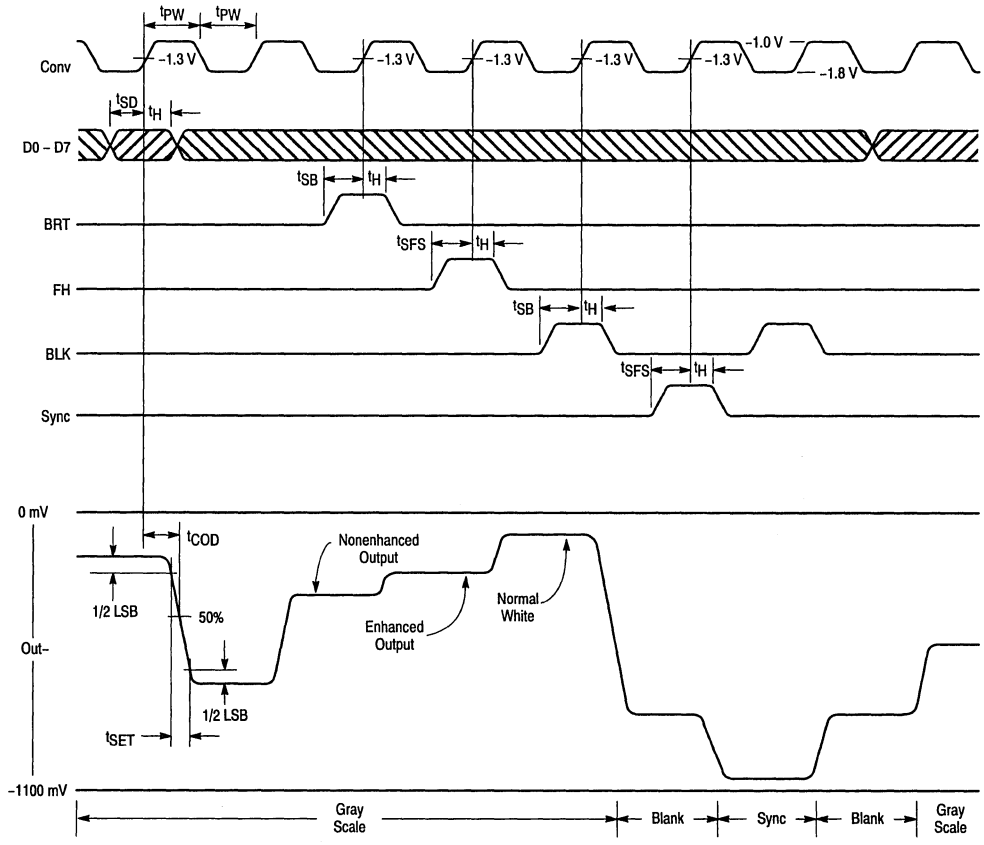
The Out – output provides a "sync down" waveform, while the Out + output provides a "sync up" waveform (see Table 1). Current flow is **into4** each of the outputs. Each output's impedance is typically 100 kΩ over the compliance range of –1.7 to + 0.3 V, and the output capacitance is typically 16 pF. An unused output cannot be left open — both outputs must be connected to a voltage within the compliance range. Both outputs should be equally loaded for best accuracy.

Table 1. Output Levels

	BRT = 0		BRT = 1	
mV	Out –	Out +	Out –	Out +
0		Sync	Enhanced White	Sync
–100	Normal White			
– 200				
– 300		Blank	Enhanced	Blank
– 400	Gray Scale	Normal Black	Gray Scale	
– 500				Enhanced Black
– 600				
– 700	Normal Black	Gray Scale	Enhanced Black	Enhanced
– 800	Blank		Blank	Gray Scale
– 900				
–1000		Normal White		Enhanced White
–1100	Sync		Sync	

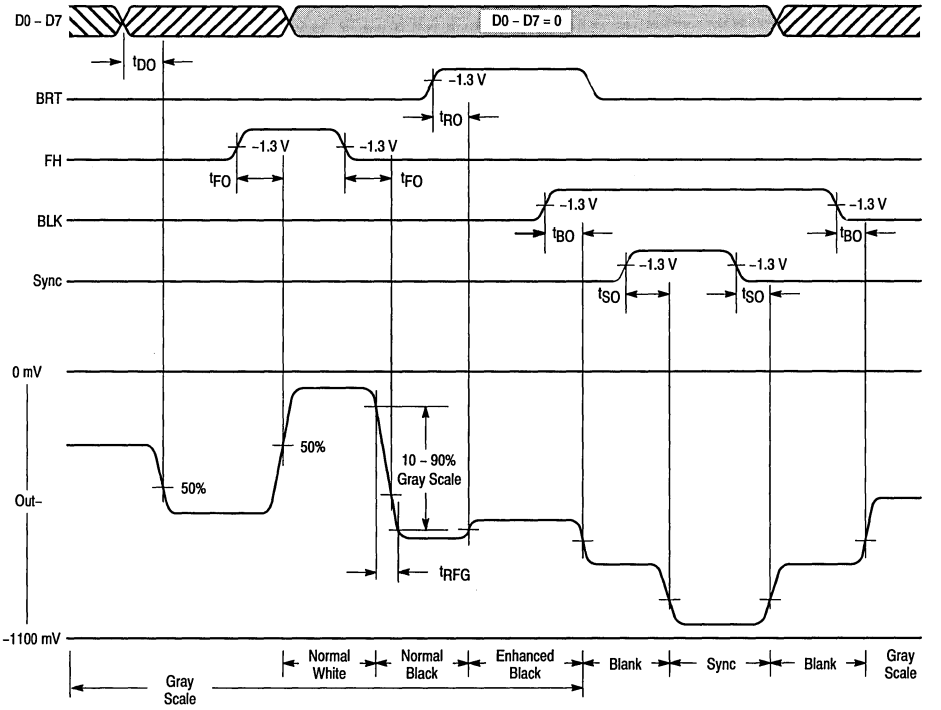
I_{ref} = 1.115 mA, R_L = 37.5 Ω.

Figure 2. Timing Diagram, Clocked Mode (FT = 0)



NOTES:
1. Single-ended clock used in production testing.
2. If differential clock is used, timing would be determined from the crossover point of the two clock signals.
3. If $\overline{\text{Convert}}$ is used in single-ended mode, timing would be measured from its falling edge.
4. Timing to output from data and controls is from Convert rising edge (threshold) to where the output has changed to 50% of final value.
5. Reference current = 1.115 mA. Output load = 37.5 Ω.
6. Waveform at Out + is inverted from that shown above.

Figure 3. Timing Diagram, Transparent Mode (FT = 1)



NOTES: 1. Reference current = 1.115 mA. Output load = 37.5 Ω.
2. Waveform at Out + is inverted from that shown above.
3. Timing from D0 – D7 and Controls is to where output has changed to 50% of final value.

TRUTH TABLE

Inputs					Outputs				
Controls				Data	Out –		Out +		
Sync	Blank	Force High	Bright	D7 – D0	(mA)	(mV)	(mA)	(mV)	Condition
1	X	X	X	X	28.8	–1080	0	0	Sync
0	1	X	X	X	21.1	– 790	7.7	– 289	Blank
0	0	0	0	000..	19.6	– 736	9.1	– 341	Normal Black
0	0	0	1	000..	17.7	– 663	11.1	– 416	Enhanced Black
0	0	1	0	X	1.94	– 73	26.8	–1005	Normal White
0	0	0	0	111..	1.94	– 73	26.8	–1005	Normal White
0	0	0	1	111..	0	0	28.8	–1080	Enhanced White
0	0	1	1	X	0	0	28.8	–1080	Enhanced White

NOTES: 1. Current flow is into the output pins.
2. Output voltage measured across a 37.5 Ω resistor to AGnd.
3. Waveform at Out + is inverted from that at Out –.
4. Reference Current = 1.115 mA.

DAC Gray Scale (D0 – D7)

Within the Gray Scale (all 4 video controls = 0), the current at Out – is controlled by the data inputs (D0 – D7) according to the following equation:

$$I_O - (GS) = \frac{I_{ref} \times (255\text{-}A)}{16} + (I_{ref} \times 1.74)$$

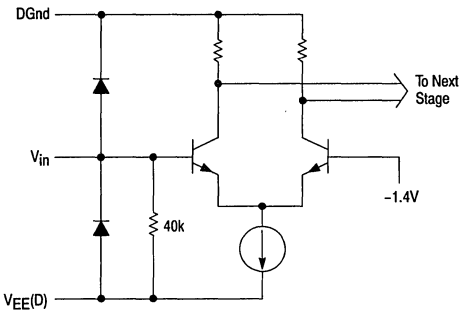
The current at Out + in the Gray Scale is determined by:

$$I_O + (GS) = \frac{I_{ref} \times A}{16} + (I_{ref} \times 8.18)$$

for the test value of I_{ref} = 1.115 mA, I_{O-} varies from 19.6 mA to 1.94 mA as the digital inputs (A) vary from 0 to 255 (00_H to FF_H), and I_{O+} will vary from 9.12 mA to 26.8 mA. The data inputs are overridden by Sync, BLK, or FH.

Figure 4 depicts a typical input stage configuration, and Figure 8 indicates the typical input current. The threshold is ≈ –1.4 V, independent of $V_{EE}(D)$. An open input is equivalent to a logic low, but good design practices dictate that inputs should never be left open. The inputs must be kept within the range of $V_{EE}(D)$ and DGnd. If an input is taken more than 0.5 V above Gnd or below $V_{EE}(D)$ excessive currents will flow, and the DAC output waveform will be distorted.

Figure 4. Typical Input Stage



DAC – Video Controls

The four video controls (Sync, BLK, FH, and BRT) are logic level inputs, ECL compatible, which permit setting the outputs to standard video levels. All four are active high. The Truth Table on page 7 indicates their priority.

The Force High input (FH) overrides the data inputs (D0 – D7), setting the DAC inputs to all 1s (FF_H). In most applications, this is equivalent to the normal white level. FH can be used with the BRT input to create an enhanced white, but is overridden by Sync or BLK.

The Bright input (BRT) shifts the Gray Scale by ≈11% in the high (white) direction. Typically this function is used to provide an enhanced, or brighter display so as to highlight certain portions of the screen. A highlighted cursor is a typical example.

The current change at each output is equal to:

$$\Delta I_{O(BRT)} = I_{ref} \times 1.74$$

The current at I_{O-} decreases in magnitude, while the current at I_{O+} increases, when BRT is asserted. BRT is ineffective when Sync or BLK are asserted, but can be used at any point within the Gray Scale.

The Blank input (BLK) sets the output currents to the blanking level used during horizontal and vertical retrace. The current at Out – is:

$$I_O - (BLK) = I_{ref} \times 18.96$$

The current at Out + is:

$$I_O + (BLK) = I_{ref} \times 6.9$$

The BLK input will override the data inputs, FH and BRT, but is overridden by Sync. Therefore, the BLK input may be left asserted during the sync time.

The Synchronizing input (Sync) sets the output currents to the sync level used for normal horizontal and vertical picture synchronization. The current at Out – is:

$$I_O - (Sync) = I_{ref} \times 25.86$$

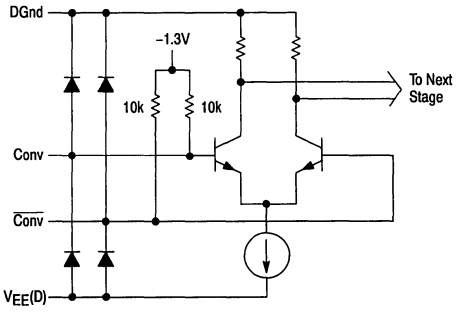
The current at Out + will be leakage current only, typically < 20 μA. The Sync input will override all other control inputs as well as data inputs.

Feedthrough (FT) Input

With FT low, the internal registers are active, and the data and video controls are clocked through to the DAC on the rising edge of Pin 6 (Conv), or on the falling edge of Pin 7. In this mode the data bits (D7 – D0) which may appear asynchronously to the MC10324 are then presented synchronously to the DAC, reducing output glitches and noise. This mode is also useful for synchronizing control functions with other events. While hold times are typically 0 ns for all inputs, the setup times prior to the clock edge must be observed.

With FT high, the registers are transparent and the data and video controls feed through directly to the DAC. This mode may be used if the data is presented to the MC10324 from external latches, which ensure minimum skew among the data bits. In this mode Pins 6 and 7 are not used.

Figure 5. Convert Input Stage

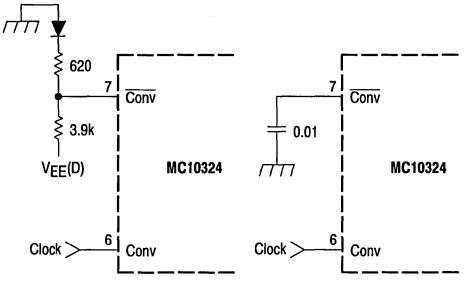


Convert Inputs

The Convert inputs (Pins 6 and 7) are used to clock in data and the video controls to the internal registers only if FT (Pin 8) is low. The input stage for these pins is shown in Figure 5. The pins are internally biased at ≈ –1.5 V with a nominal input impedance of 10 kΩ. The inputs may be driven from complementary ECL clock signals with the clocking action occurring on the rising edge of Conv and the falling edge of $\overline{\text{Conv}}$ as the signals cross each other in voltage.

A single-ended clock source may be used by connecting either Pin 6 or 7 to a fixed voltage to set the threshold and applying the clock signal to the other pin. If done this way, the fixed voltage must be within the range of – 0.3 V to V_{EE}(D) +1.3 V. Figure 6 shows three positive edge triggered examples. Interchanging Pins 6 and 7 provides negative edge triggered operation. Alternately the V_{BB} reference of another ECL circuit may be used to set the MC10324's clock reference.

Figure 6. Single-Ended Clock Input



The input current required at each pin is shown in Figure 9, and is independent of the clocking mode used.

If FT is high, the Convert pins are nonfunctional, and **must** be connected to **different** voltages (e.g., V_{EE}(D) and DGnd). Leaving the pins open can result in high frequency oscillations or spurious noise.

Conv and $\overline{\text{Conv}}$ must be kept within the range of DGnd and V_{EE}(D). If taken more than 0.5 V above DGnd or below V_{EE}(D) excessive currents will flow, and the DAC output waveform will be distorted.

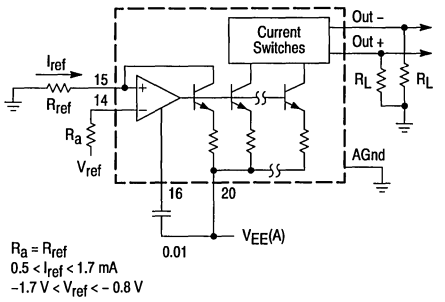
Reference Amplifier

The reference amplifier (Pins 14 to 16) is used to accept the externally supplied reference current for the DAC current switches (see Figure 7).

Ref + (Pin 15) is a low impedance (virtual ground) input into which the reference current flows (current cannot flow out of this pin). Due to the op amp's internal feedback, the voltage at Ref + is the same as that set at Ref –, with a typical input offset of ± 5.0 mV. The current into Ref + should be within the range of 0.5 mA to 1.7 mA to maintain 8-bit linearity and accuracy. A reference current of 1.115 mA is recommended to obtain EIA-170 and EIA-343-A voltage levels at the outputs if they are terminated with 37.5 Ω (double 75 Ω terminations).

Ref – is a high impedance input (>10 MΩ) which must be set to a voltage within the range of – 0.8 to –1.7 V. A nominal bias current of ≈1.4 μA will flow into this pin. In Figure 7, $I_{ref} = V_{ref}/R_{ref}$.

Figure 7. Reference Amplifier



Timing

Figures 2 and 3 are the timing diagrams for the MC10324. Figure 2 is for the Clocked Mode where data and control inputs are latched into the input registers by the Convert (and/or $\overline{\text{Convert}}$) inputs. If the clock signal is single-ended, the data and control latching occurs on the rising edge of Convert, or the falling edge of $\overline{\text{Convert}}$. If a differential clock is used, latching occurs at the cross-over point of the two signals. The hold time for the data and controls is 0, but the setup times must be observed. The clock duty cycle is not important as long as the minimum pulse widths are observed.

Figure 3 is for the transparent (non-clocked) mode. The output responds to the application of new data or control inputs without the need for a clocking edge. The propagation delay to the output is different for each of the data and control signals. To prevent large glitches at the outputs, it is imperative that the data bits (D0 – D7) arrive at the MC10324 simultaneously with minimum skew. If the synchronism of the 8-bits cannot be guaranteed, either external latches should be used (MC10H176 type), or the MC10324 should be used in the clocked mode.

Power Supplies

The MC10324 requires a – 5.2 V supply for both V_{EE}(A) and V_{EE}(D), both ± 10%. Nominal current requirements are 47 mA and 19 mA, respectively, (including a total output current of 29 mA). The supply current required at V_{EE}(A) is dependent on the total output current (Pin 18 plus Pin 19). V_{EE}(D) powers only the digital portion of the IC (control logic and latches), and should be referenced to Digital Ground (Pin 9). V_{EE}(A) powers the analog portion of the IC (reference amplifier and the DAC's current sources), and should be referenced to Analog Ground (Pin 17). See the Applications Section for additional information on power supplies, bypassing and PC board layout.

Figure 8. Input Current, Data and Controls

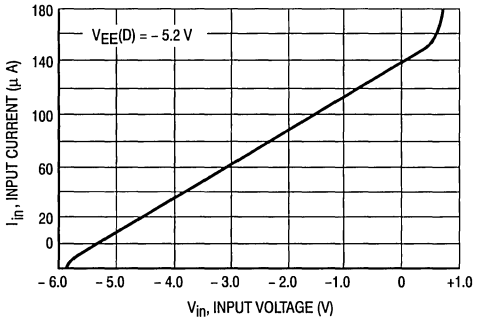
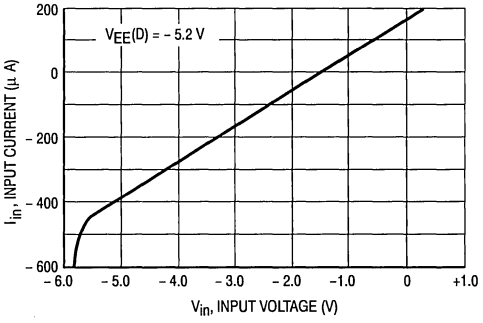


Figure 9. Input Current, Convert Inputs



6

APPLICATIONS INFORMATION

Power Supplies, Grounding

The PC board layout and the quality of the power supplies and the ground system **at the IC** are very important in order to obtain proper operation. Noise from any source coming into the device on the V_{EE} supply pins, or ground can cause an incorrect output code due to interaction with the analog portion of the circuit. At the same time, noise generated within the MC10324 can cause incorrect operation if that noise does not have a clear path to AC ground.

Both the analog and digital power supplies must be decoupled to the appropriate ground **at the IC** (within 1″ max) with a 10 μF tantalum and a 0.1 μF ceramic. Tantalum capacitors are recommended since electrolytic capacitors simply have too much inductance at the frequencies of interest. The quality of the supplies should then be checked at the IC with a high frequency scope. Noise spikes (always present when digital circuits are present) can easily exceed 400 mV peak, and if they get into the analog portion of the IC, the operation can be disrupted. Noise can be reduced by inserting resistors and/or inductors between the supplies and the IC.

If switching power supplies are used, there will usually be spikes of 0.5 V or greater at frequencies of 50 kHz to 1.0 MHz. These spikes are generally more difficult to reduce because of their greater energy content. In extreme cases three terminal regulators (MC7905.2CT), with appropriate high frequency filtering should be used and dedicated to the MC10324.

The ripple content of the supplies should not allow their magnitude to exceed the values in the Recommended Operating Conditions.

The PC board tracks supplying – 5.2 V to the MC10324 should preferably not be at the tail end of the bus distribution after passing through a maze of digital circuitry. The MC10324 should be close to the power supply, or the connector where the supply voltages enter the board. If the supply lines are supplying considerable current to other parts of the board, then it is preferable to have dedicated lines from the supply or connector directly to the MC10324.

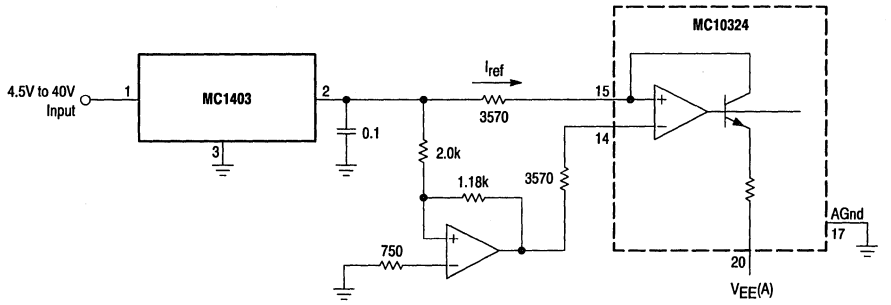
The two ground pins (DGnd and AGnd) must eventually be connected together, usually near the power supply, although the specific board layout may dictate a different "best point." V_{EE}(D) must be referenced to DGnd, and V_{EE}(A) must be referenced to AGnd.

PC Board Layout

Due to the high frequencies involved, and in particular, the fast edges of the various digital signals, proper PC board layout is imperative. A solid ground plane is strongly recommended in order to have known transmission characteristics, and also to minimize coupling of the digital signals into the analog section. Use of wire wrapped boards should definitely be avoided.

Each PC track should be considered a transmission line, and if they are of any considerable length (more than a few inches), they should be terminated according to transmission line theory. Otherwise reflections back to the signal sources can occur, disrupting their operation. Additionally, the overshoots and undershoots which will occur at the MC10324's input pins can cause its operation to be disrupted, resulting in a noisy or incorrect output.

Figure 10. Reference Supply



Reference Circuits

Since the accuracy of the outputs are directly related to the accuracy and quality of the reference current and voltage, it is imperative that accurate and stable references be used at Pins 14 and 15. The voltage supply used for the digital circuitry should preferably *not* be used as a source for either the reference current or voltage due to the noise spikes and ripple present on the supply and its ground lines.

Figure 10 indicates a method for generating the reference signals from a positive supply. The MC1403 reference is a stable 2.5 V bandgap regulator (± 1%), with a maximum temperature coefficient of 40 ppm/°C, and good ripple and high frequency noise rejection. In the figure the circuit supplies –1.48 V to Pin 14, and a current of 1.113 mA to Pin 15. If the outputs of the MC10324 are terminated with 37.5 Ω, the voltage levels will be well within the allowable range specified by EIA-170 and EIA-343-A.

If the analog – 5.2 V supply (V_{EE}(A)) is fairly clean and free of digital noise the circuit of Figure 11 may be used. The TL431 is a stable 2.5 V bandgap reference (± 1%) with an effective temperature coefficient of 50 ppm/°C. The 5 k pot allows adjustment for precise output levels, or it may be replaced with a precision resistor which provides the correct voltage at Pin 14.

Figure 12 indicates another reference circuit using the LM385–1.2 reference diode. R_{ref} is chosen to provide the desired reference current to Pin 15 knowing that it is set at –1.235 V. The LM385 is a bandgap type reference with a ± 2% initial accuracy. The 20 k resistor biases the diode at approximately 200 μA for minimum temperature variations. The 0.2 μF capacitor, with the 20 k resistor, filters out noise above ≈ 40 Hz.

Figure 11. Reference Supply

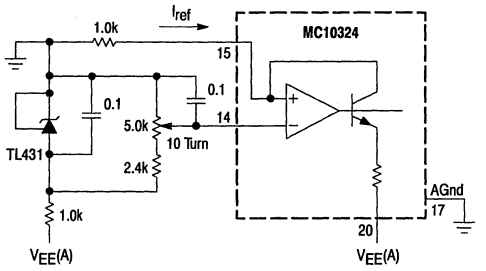
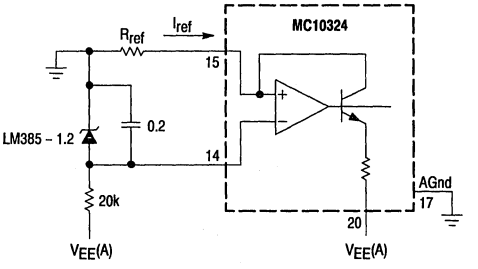


Figure 12. Reference Supply



Digitally Modulating an Analog Signal

The MC10324 may be used to digitally modulate (or attenuate) an analog signal by applying the analog signal to the reference amplifier. Three methods of doing this are shown in Figures 13 to 15.

Figure 13. Applying an Analog Signal Directly

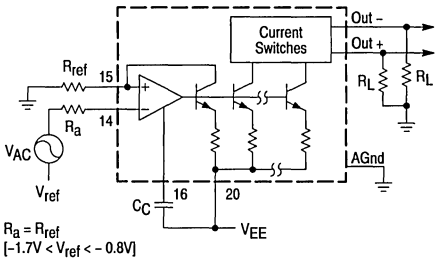


Figure 14. Capacitor Coupling the AC Voltage

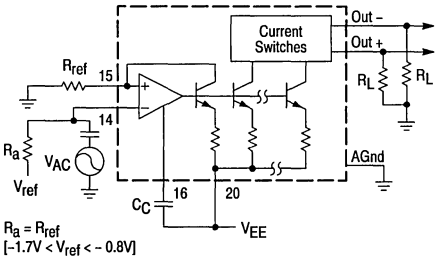
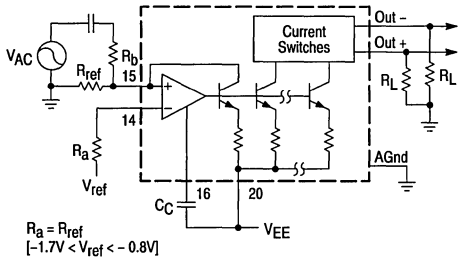


Figure 15. Applying a Modulating Current



In all three examples the DC reference current is V_{ref}/R_{ref}. In Figure 13 the AC signal source is referenced to a negative voltage source (V_{ref}). In Figures 13 and 14 the AC reference current is equal to V_{AC} divided by R_{ref}. In Figure 15 the AC reference current is equal to V_{AC} divided by R_b. The AC signal at Out – and Out + is determined by the following equations:

$$V_{O-(AC)} = \frac{I_{ref(AC)} \times (255-A) \times R_L}{16}$$

$$V_{O+(AC)} = \frac{I_{ref(AC)} \times A \times R_L}{16}$$

where "A" is the value of the digital word at D0 – D7 (0 to 255).

When implementing any of the above schemes, or any other method of feeding an AC signal to the reference amplifier, the following operating limits must be observed:

1) The peak values of the reference current (AC + DC) must be within the range of 0.5 mA to 1.7 mA into Pin 15;
2) The peak values of the voltage at Ref + and Ref – must be within the range of – 0.8 V to –1.7 V;
3) The peak values of the voltage at Out – and Out + must be within the range of –1.7 V to + 0.3 V.

The maximum frequency which can be handled by the reference amplifier is dependent on the compensation capacitor (C_C) at Pin 16, and the signal amplitude according to the following equation:

$$f_{max} = \frac{1.59 \times 10^{-8}}{C_C \times I_{pk}}$$

where I_{pk} is the peak value of the AC reference current (1/2 of the peak-to-peak value). The small signal bandwidth of the reference amplifier is ≈ 3.0 MHz.

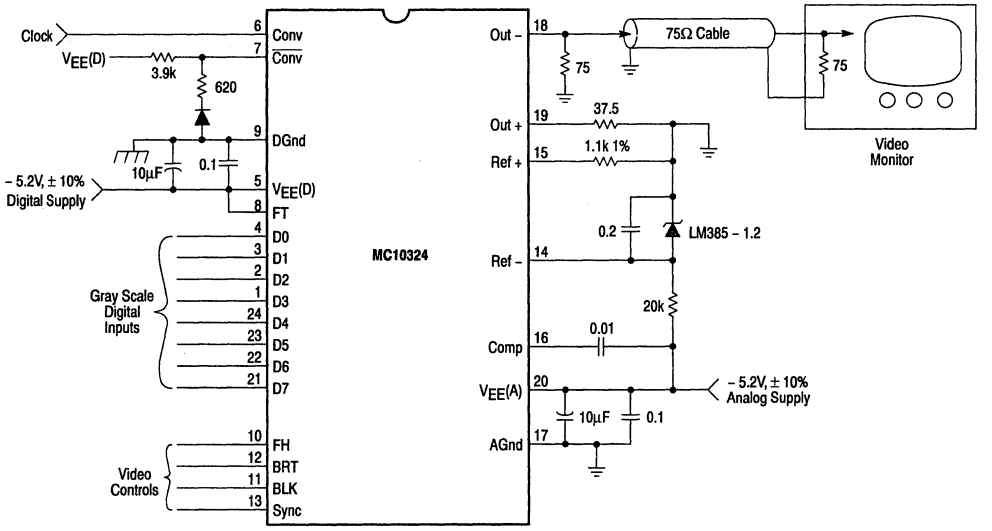
Components associated with the reference amplifier (Pins 14 – 16) should be physically close to the pins. The board layout should be neat, preventing unwanted stray capacitive coupling between the outputs and the reference amplifier. If C_C is smaller than 5000 pF a ground plane is strongly recommended. C_C should not be smaller than 250 pF.

TYPICAL APPLICATION CIRCUITS

Figure 16 shows a typical video application circuit using the MC10324 in the clocked mode. The clock is single-ended, and the circuit updates the output on the rising edge of the clock. The Out – pin feeds a standard 75 Ω monitor through a 75 Ω cable, which is terminated at both ends. The reference voltage is supplied by an LM385–1.2 regulator.

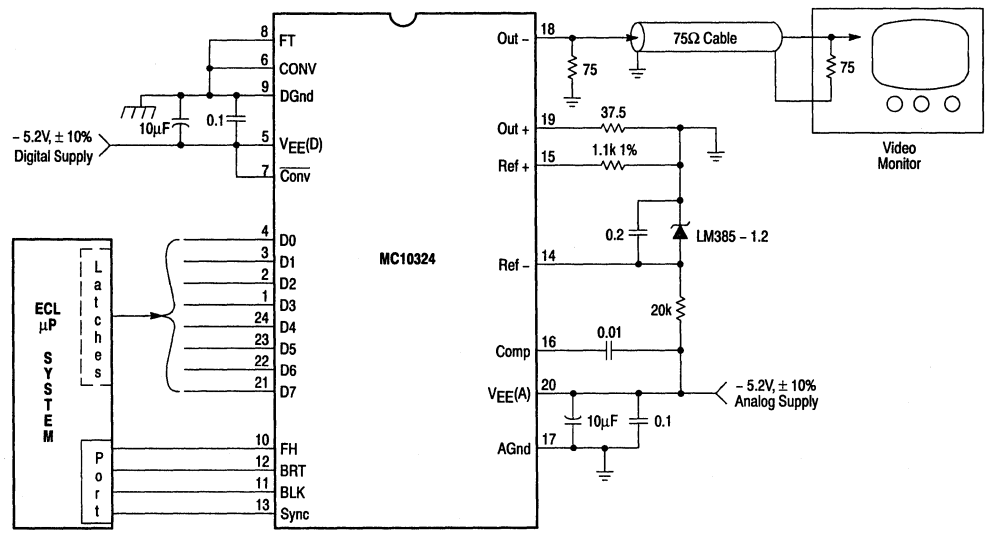
Figure 17 shows a circuit similar to that of Figure 16, except the MC10324 is used in the transparent mode. The source of the data bits must provide the 8-bits simultaneously, with minimum skew, to keep output glitches to a minimum. If latches, or other antiskew circuitry, are not available within the microprocessor circuitry, a set of 8-bit latches between it and the MC10324 is recommended, or the MC10324 should be used in the clocked mode.

Figure 16. Clocked Mode



NOTES: 1. Gray Scale inputs, video controls, and clock are to be referenced to digital ground.
2. Outputs and reference circuitry are to be referenced to analog ground.
3. PC board layout to be such that digital noise does not get into the analog side circuitry.
4. Analog and digital grounds to be connected together. Location of this connection is board layout dependent,and is to be such that digital ground noise does not show up in the analog signals.
5. ECL termination required at all inputs per ECL system requirements.

Figure 17. Transparent Mode



GLOSSARY

Bandgap Reference – A voltage reference circuit based on the predictable base-emitter voltage of a transistor. The silicon bandgap voltage of ≈1.2 V is the basis for generating other voltages which are stable with time and temperature.
Bipolar Input – A mode of operation whereby the analog input (of an A-D), or output (of a DAC), includes both negative and positive values. Examples are: – 5.0 V to + 5.0 V, – 2.0 V to + 8.0 V, etc.
DAC Current Gain – The internal gain the DAC applies to the reference current to determine the full scale output current. The actual maximum current out of a DAC is one LSB less than the full scale current.
Differential Gain – In video systems, differential gain is a component's change in gain as a function of luminance level. In a color picture, contrast will be affected if the differential gain is not zero.
Differential Nonlinearity – The maximum deviation in the actual step size (one transition level to another) from the ideal step size. The ideal step size is defined as the Full Scale Range divided by 2^n. This error must be within ± 1 LSB for proper operation.
Differential Phase – In video systems, differential phase is the change in the phase modulation of the chrominance as a function of the luminance level. The hue in a color picture will be distorted if the differential phase is not zero.
ECL – Emitter coupled logic.
Full Scale Range – The difference between the minimum and maximum end points of the analog input (of an A/D), or output (of a DAC), plus one LSB.
Gain Error – The difference between the actual and expected gain (end point to end point), with respect to the reference, of a data converter. The gain error is usually expressed in LSBs, or percent.
Glitch Area – The energy content of a glitch, specifically in volt-seconds. It is the area under the curve of the glitch waveform. For a symmetrical glitch, the area and the energy can be zero.
Gray Code – Also known as *reflected binary code*, is a digital code such that each code differs from adjacent codes by only one bit. Since more than one bit is never changed at each transition, race condition errors are eliminated.
Integral Nonlinearity – The maximum error of an A/D or DAC, transfer function from the ideal straight line connecting the analog end points. This parameter is sensitive to dynamics, and test conditions must be specified in order to be meaningful. This parameter is the best overall indicator of the device's performance.
LSB – Least Significant Bit. It is the lowest order bit of a binary code.
Line Regulation – The ability of a voltage regulator to maintain a certain output voltage as the input to the regulator is varied. The error is typically expressed as a percent of the nominal output voltage.
Load Regulation – The ability of a voltage regulator to maintain a certain output voltage as the load current is varied. The error is typically expressed as a percent of the nominal output voltage.
Monotonicity – The characteristic of the transfer function whereby increasing the input code (of a DAC), or the input signal (of and A/D), results in the output never decreasing. Nonmonotonicity occurs if the differential nonlinearity exceeds ± 1 LSB.
MSB – Most Significant Bit. It is the highest order bit of a binary code.
Natural Binary Code – A binary code defined by:

$$N = A_n 2^n + \ldots + A_3 2^3 + A_2 2^2 + A_1 2^1 + A_0 2^0$$

where each "A" coefficient has a value of 1 or 0. Typically, all zeros correspond to a zero input voltage of an A/D, and all ones correspond to the most positive input voltage.
Nyquist Theory – See Sampling Theorem.
Offset Binary Code – Applicable only to bipolar input (or output) data converters, it is the same as Natural Binary code, except that all zeros correspond to the most negative output signal (of a D/A), while all ones correspond to the most positive output.
Output Compliance – The maximum voltage range to which the DAC outputs can be subjected, and still meet all specifications.
Power Supply Rejection Ratio – The ability of a device to reject noise and/or ripple on the power supply pins from appearing at the outputs. An AC measurement, this parameter is usually expressed in dB rejection.
Power Supply Sensitivity – The change in a data converter's performance with changes in the power supply voltage(s). This parameter is usually expressed in percent of full scale versus ΔV.
Propagation Delay – For a DAC, the time from when the clock input crosses its threshold to when the DAC output(s) changes.
Quantization Error – Also known as *digitization error* or uncertainty. It is the inherent error involved in digitizing an analog signal due to the finite number of steps at the digital output versus the infinite number of values at the analog input. This error is a minimum of ± 1/2 LSB.
Resolution – The smallest change which can be discerned by an A/D converter, or produced by a DAC. It is usually expressed as the number of bits (n), where the converter has 2^n possible states.
Sampling Theorem – Also known as the *Nyquist Theorem*. It states that the sampling frequency of an A/D must be no less than 2x the highest frequency (of interest) of the analog signal to be digitized in order to preserve the information of that analog signal.
Settling Time – For a DAC, the time required for the output to change (and settle in) from an initial ±1/2 LSB error band to the final ± 1/2 LSB error band.
Two's Complement Code – A binary code applicable to bipolar operation, in which the positive and negative codes of the same analog magnitude sum to all zeros, plus a carry. It is the same as *offset binary code*, with the MSB inverted.
Unipolar Input – A mode of operation whereby the analog input range (of an A/D), or output range (of a D/A), includes values of a single polarity. Examples are:
0 to +10 V, 0 to – 5.0 V, + 2.0 V to + 8.0 V, etc.

Additional information regarding the transmission characteristics of PC board tracks can be found in Motorola's MECL System Design Handbook (HB205).

Interface Circuits

In Brief . . .

Described in this section is Motorola's line of interface circuits, which provide the means for interfacing microprocessor or digital systems to the external world, or to other systems.

Also included are devices which allow a micro- processor to communicate with its own array of memory and peripheral I/O circuits.

The line drivers, receivers, and transceivers permit communications between systems over cables of several thousand feet in length, and at data rates of up to several megahertz. The common EIA data transmission standards, several European standards, IEEE-488, and IBM 360/370 are addressed by these devices.

The peripheral drivers are designed to handle high current loads such as relay coils, lamps, stepper motors, and others. Input levels to these drivers can be TTL, CMOS, high voltage MOS, or other user defined levels. The display drivers are designed for LCD or LED displays, and provide various forms of decoding.

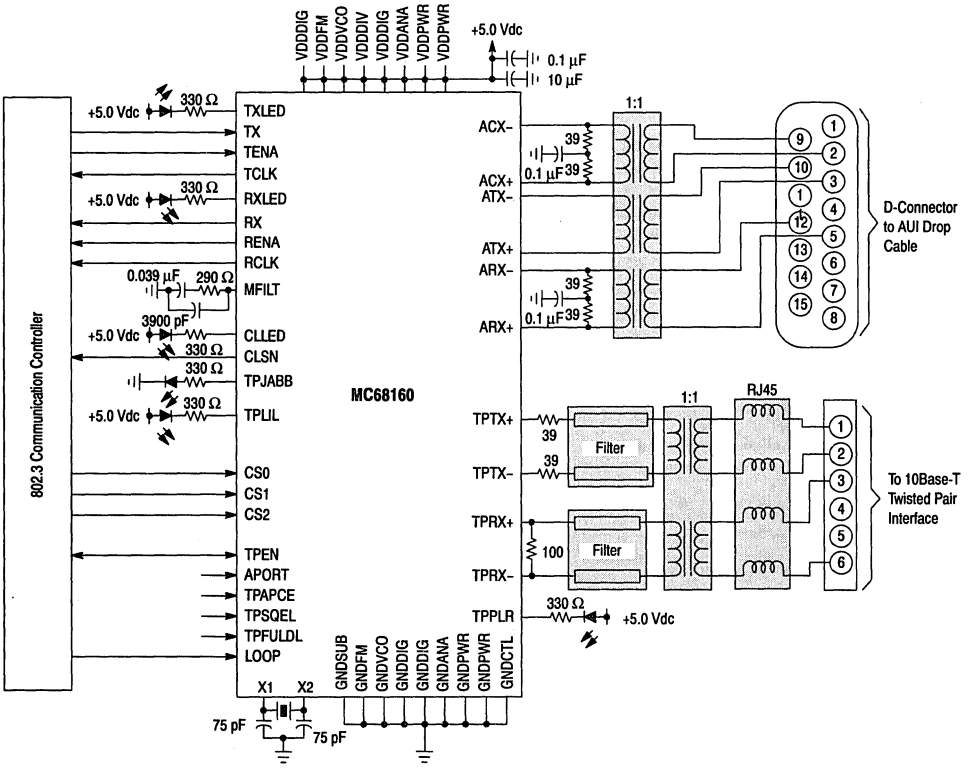
Enhanced Ethernet Serial Transceiver (EEST)

MC68160P

T_A = 0° to +70°C, Case 848D

The MC68160 is a BiCMOS integrated circuit for use in ethernet applications. The IC integrates the Attachment Unit Interface (AUI), the 10BASE-T interface and the communications controller interface. The communications interface is compatible with Motorola, AMD, Intel, National Semiconductor, Fujitsu, Western Digital controllers and is set by the bias of external pins.

Connection to the twisted pair media is accomplished with common 10BASE-T filters and transformers. The AUI requires standard transformers. (The EEST is packaged in a 52-pin Thin Quad Flat Pack.)



Communication Controller Selection

CS0	CS1	CS2	802.3 Communication Controller
1	1	0	Motorola MC68360, AMD 7990 & 79C900
0	1	0	Intel 8256, 82590, 82593, 82596
1	0	0	Fujitsu MB86950, MB86960
0	0	0	National 8390, 83C690, 83932B
1	1	1	Standby Low Current Mode

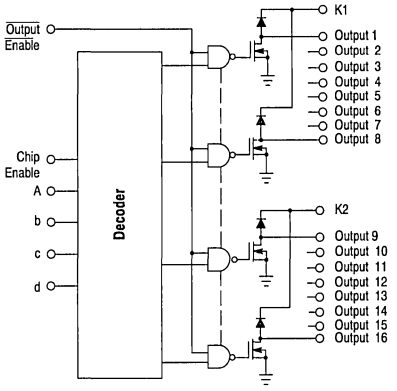
High Performance Decoder Driver/Sink Driver

MC34142DW, FN

T_A = 0° to +70°C, Case 751F, 776

The MC34142 is a high performance 4 to 16 multiplexed driver. This integrated circuit features a 4 to 16 decoder, 16 open drain N-channel MOS output devices with clamp diodes. The outputs are controlled by 4 address inputs, an output enable, and a chip enable.

Typical applications include solenoid drivers, LED drivers, lamp drivers, and relay drivers.

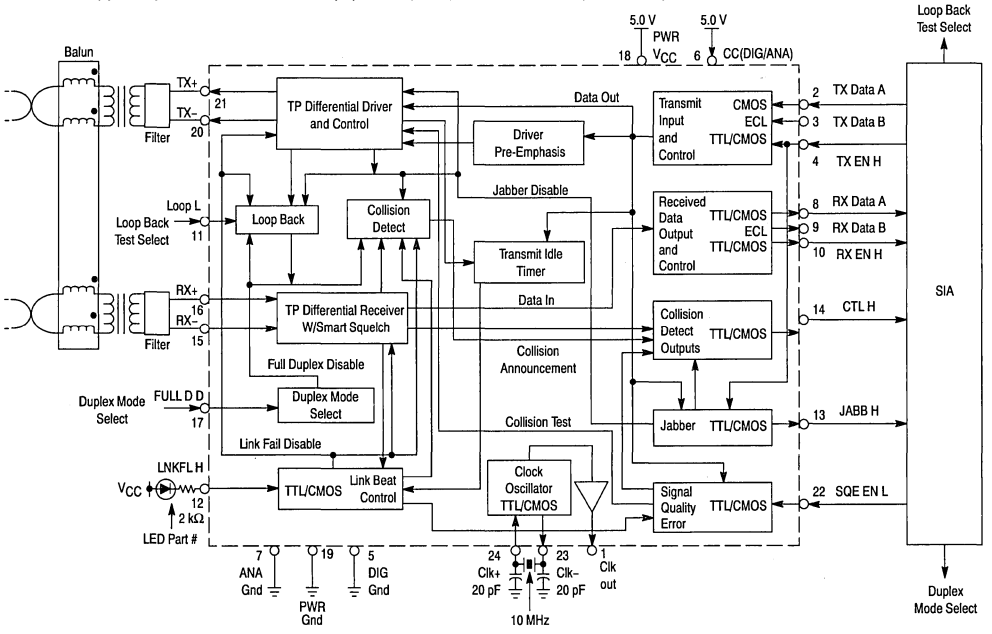


ISO 8802-3[IEEE 802.3] 10BASE-T Transceiver

MC34055DW, P

T_A = 0° to +70°C, Case 751E, 724

The Motorola 10BASE-T transceiver, designed to comply with the ISO 8802-3[IEEE 802.3] 10BASE-T specification, will support a Medium Dependent Interface (MDI) in an embedded Media Attachment Unit (MAU). The interface supporting the Data Terminal Equipment (DTE) is TTL, CMOS, and raised ECL compatible, and the interface to the Twisted Pair (TP) media is supported through standard 10BASE-T filters and transformers. Differential data intended for the TP media is provided a 50 ns pre-emphasis and data at the TP receiver, is screened by Smart Squelch circuitry for specific threshold, pulse width, and sequence requirements.



Microprocessor Bus Interface

Motorola offers a spectrum of line drivers and receivers which provide interfaces to many industry standard specifications. Many of the devices add key operational features, such as hysteresis, short circuit protection, clamp diode protection, or special control functions.

Address and Control Bus Extenders

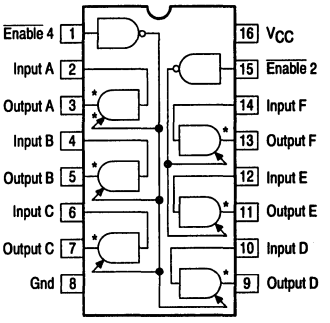
These devices are designed to extend the drive capabilities of today's standard microprocessors. All devices are fabricated with Schottky TTL technology for high speed.

V_{OL} @ 48 mA Max	V_{OH} @ –5.2 mA Min	Propagation Delay Max (ns)	Buffers Per Package	Device	Suffix/ Package	Comments
0.5	2.4	13	6	MC8T97/ MC6887	L/620 P/648	Noninverting
		11		MC8T98/ MC6888		Inverting

Hex 3-State Buffers/Inverters
T_A = 0° to +75°C

The noninverting MC8T97/MC6887 and inverting MC8T98/ MC6888 provide two Enable inputs, one controlling four buffers and the other controlling the remaining two buffers.

MC8T97/MC6887(1) — Noninverting
MC8T98/MC6888(1) — Inverting
(1)These devices may be ordered by either of the paired numbers.



*Add Inverter for MC6888/MC8T98.

Microprocessor Data Bus Extenders

Driver Characteristics		Receiver Characteristics				
Output Current (mA)	Propagation Delay Max (ns)	Propagation Delay Max (ns)	Transceivers Per Package	Device	Suffix/ Package	Comments
48	14	14	4	MC8T26A (MC6880A)	P/648 L/620	Inverting Logic

Magnetic Read/Write

Device	Comments	T_A (°C)	Suffix/ Package
MC3471	Tunnel/Straddle Erase Controller. Provides entire interface between floppy disk heads and the head control and write data signals for straddle erase heads.	0 to + 70	P/738
MC3470, A	Floppy Disk Read Amplifier System. A monolithic read amplifier system for reading differential AC signals from the magnetic head and converting to a digital output.		P/707
MC34167	Magnetic Tape Sense Amplifier. Trace independent preamplifiers with individual gain control. Optimized for use with 9-track magnetic tape memory systems.		

Single-Ended Bus Transceivers

For Instrumentation Bus, Meets GPIB/IEEE Standard 488

Driver Characteristics		Receiver Characteristics					
Output Current (mA)	Propagation Delay Max (ns)	Propagation Delay Max (ns)	Transceivers Per Package	Device	Suffix/ Package	Comments
48	30	50	8	MC3447	P3/724 L/623 P/649	Input hysteresis, open collector, 3-state outputs with terminations
	17	25	4	MC3448A	P/648 D/751B L/620	Input hysteresis, open collector, 3-state outputs with terminations

For High Current Party-Line Bus for Industrial and Data Communications

Driver Characteristics		Receiver Characteristics				
Output Current (mA)	Propagation Delay Max (ns)	Propagation Delay Max (ns)	Transceivers Per Package	Device	Suffix/ Package	Comments
100	15	15	4	MC26S10	P/648 D/751B L/620	Open collector, outputs, common enable

Line Receivers

7

General Purpose

S = Single Ended D = Differential	Type (1) of Output	t_{prop} Delay Time Max (ns)	Party Line Operation	Strobe or Enable	Power Supplies (V)	Device	Suffix/ Package	Receivers Per Package	Companion Drivers	Comments
D	TP OC	25	✓	✓	±5.0	MC3450 MC3452	D/751B P/648 L/620	4	MC3453	Quad version of MC75107/108
	TP OC		✓	✓		MC75107 MC75108	P/646 L/632	2	MC75S110	Dual version of MC3450/2
S	TP	30	✓	✓	+5.0	MC3437	P/648 L/620	6		Input hysteresis

(1)OC = Open Collector, TP = Totem-pole output

EIA Standard

S = Single Ended D = Differential	Type of Output	t_{prop} Delay Time Max (ns)	Party Line Operation	Strobe or Enable	Power Supplies (V)	Device	Suffix/ Package	Receivers Per Package	Companion Drivers	Comments
S	TP	4000	—	—	+5.0	MC14C89B MC14C89B	P/646 D/751A	4	MC14C88B	EIA-232-D/ EIA-562
S	R(2)	85	—	—		MC1489 MC1489A	D/751A P/646 L/632		MC1488	EIA-232-D
S, D	TP	30	✓	✓		AM26LS32 MC3486	P/648 D/751B L/620		AM26LS31 MC3487	EIA-422/423
		35	✓	✓		SN75173 SN75175	N/648 D/751B		MC75172B MC75174B	EIA-422/423/ 485

(2)R = Resistor Pull-up, TP = Totem-pole output

Line Drivers

General Purpose

Output Current Capability (mA)	t_{prop} Delay Time Max (ns)	S = Single Ended D = Differential	Party Line Operation	Strobe or Enable	Power Supplies (V)	Device	Suffix/ Package	Receivers Per Package	Companion Drivers	Comments
15	15	D	✓	✓	±5.0	MC3453	P/648 L/620	4	MC3450 MC3452	Quad version of MC75S110
			✓	✓		MC75S110	P/646 L/632	2	MC75107 MC75108	Dual version of MC3453

360/370 I/O Interface

60	45	S	✓	✓	+5.0	MC3481	P/648 L/620	4		Short circuit Fault flag
			✓	✓		MC3485	P/648			

EIA Standard

Output Current Capability (mA)	t_{prop} Delay Time Max (ns)	S = Single Ended D = Differential	Party Line Operation	Strobe or Enable	Power Supplies (V)	Device	Suffix/ Package	Receivers Per Package	Companion Drivers	Comments
85	35	D	✓	✓	+5.0	MC75172B MC75174B	N/648 J/620	4	SN75173 SN75175	EIA-485
48	20		✓	✓		MC3487	P/648 D/751B L/620		MC3486	EIA-422 with 3-state outputs
			✓	✓		AM26LS31	PC/648 DC/620		AM26LS32	
						MC26LS31	D/751B		MC26LS32	
20		S	—	—	±12	MC3488A (μA9636A)	P1/626 D/751B U/693	2	MC3486 AM26L532	EIA-423/232-D
15	3500				±7.0 to ±12	MC14C88B	P/646 D/751A	4	MC14C89B MC14C89B	EIA-232-D/ EIA-562
10	350				±9.0 to ±12	MC1488	P/646 D/751A L/632		MC1489 MC1489A	EIA-232-D
60	300	S/D		422 ✓ 423 —	±5.0	AM26LS30	PC/648	2 (422) 4 (423)	AM26LS32 MC3486	EIA-422 EIA-423
						MC26LS30	D/751B		MC26LS32	Switchable

Line Transceivers

Driver Prop Delay (Max ns)	Receiver Prop Delay Max (ns)	DE = Driver Enable RE = Receiver Enable	Party Line Operation	Power Supplies (V)	Device	Suffix/ Package	Drivers Per Package	Receivers Per Package	EIA Standard
20	30	DE, RE	✓	+5.0	MC34050	D/751B P/648	2	2	EIA-422
		DE	✓		MC34051	D/751B P/648			

EIA-232-D/V.28 CMOS Drivers/Receivers

Device	Suffix/Package	Pins	Drivers	Receivers	Power Supplies (V)	Features
MC145403	P/738 DW/751D	20	3	5	± 5.0 to ± 12	
MC145404	P/738 DW/751D		4	4		
MC145405			5	3		
MC145406	P/648 DW/751G	16	3			
MC145407	P/738 DW/751D	20			+ 5.0	Charge Pump
MC145408	P/724 DW/751E	24	5	5	± 5.0 to ± 12	
MC145705	P/738 DW/751D	20	2	3	+ 5.0	Charge Pump, Power Down
MC145706	P/738 DW/751D		3	2		
MC145707	P/724 DW/751E	24		3		

Peripheral Drivers

Output Current Capability (mA)	Input Capability	Propagation Delay Time Max (µs)	Output Clamp Diode	Off State Voltage Max (V)	Device	Drivers Per Package	Suffix/ Package	Logic Function
300	TTL, DTL	1.0	✓	70	MC1472	2	P1/626	NAND
500	TTL, CMOS, PMOS				ULN2801	8	A/707	Invert
	14 V to 25 V PMOS			50	ULN2802			
	TTL, CMOS				ULN2803			
	6.0 V to 15 V MOS				ULN2804			
	TTL, CMOS PMOS				MC1411,B (ULN2001A)	7	P/648	
	14 V to 25 V PMOS				MC1412,B (ULN2002A)			
	TTL, 5.0 V CMOS				MC1413,B (ULN2003A)			
	8.0 V to 18 V MOS				MC1416,B (ULN2004A)			
	TTL, 5.0 V CMOS	0.15		35	MC34142	16	FN/776 DW/751F	1 of 16 Power Decoder
1500	TTL, 5.0 V CMOS	1.0		50	ULN2068B	4	B/648C	Invert

IEEE 802.3 Transceivers

Device	Power Supply	10 BaseT	NRZ	IEEE	Comments	Suffix/Package
MC34055	+ 5.0 Vdc	Transmit and Receive over 4 Pins	Raised ECL, CMOS	802.3 Type 10BaseT	Transceiver with non-return to zero (NRZ) interface. Intended for but not restricted to concentrators and repeator applications.	DW/751E P/724
MC68160	+ 5.0 Vdc	Transmit and Receive over 4 Pins	TTL, CMOS	802.3 Type 10BaseT/ AUI/NRZ	Interfaces gluelessly to Motorola's MC68360 communications controller.	P/648

CMOS Display Drivers

These CMOS devices include digit as well as matrix drivers for LEDs, LCDs, and VFDs. They find applications over a wide range of end equipment such as instruments, automotive dash boards, home computers, appliances, radios and clocks.

Display Drivers

Display Type	Input Format	Drive Capability Per Package	On-Chip Latch	Display Control	Segment Drive Current	Device
LCD (Direct Drive)	Parallel BCD	7 Segments	✓	Blank	≈ 1.0 mA	MC14543B
				Blank, Ripple Blank		MC14544B
	Serial Binary [Compatible with the Serial Peripheral Interface (SPI) on CMOS MCUs]	33 Segments or Dots			20 µA	MC145453
Muxed LCD (1/4 Mux)		48 Segments or Dots			≈ 200 µA	MC145000
		44 Segments or Dots				MC145001
LED, Incandescent, Fluorescent(1)	Parallel BCD	7 Segments		Blank, Lamp Test	25 mA	MC14511B
				Blank, Ripple Blank, Lamp Test		MC14513B
				Blank	65 mA	MC14547B
Muxed LED (1/4 Mux)	Serial Binary [Compatible with the Serial Peripheral Interface (SPI) on CMOS MCUs]	4 Digits + Decimals	✓	Oscillator (Scanner)	50 mA (Peak)	MC14499
(1/5 Mux)		5 Characters + Decimals or 25 Lamps		Oscillator (Scanner), Low-Power Mode, Dimming	0 to 35 mA (Peak) Adjustable	MC14489
LED (Direct Drive)	Parallel Hex	7 Segments + A thru F Indicator			10 mA(2)	MC14495♦1
(Interfaces to Display Drivers)	Parallel BCD	7 Segments		Ripple Blank, Enable		MC14558B

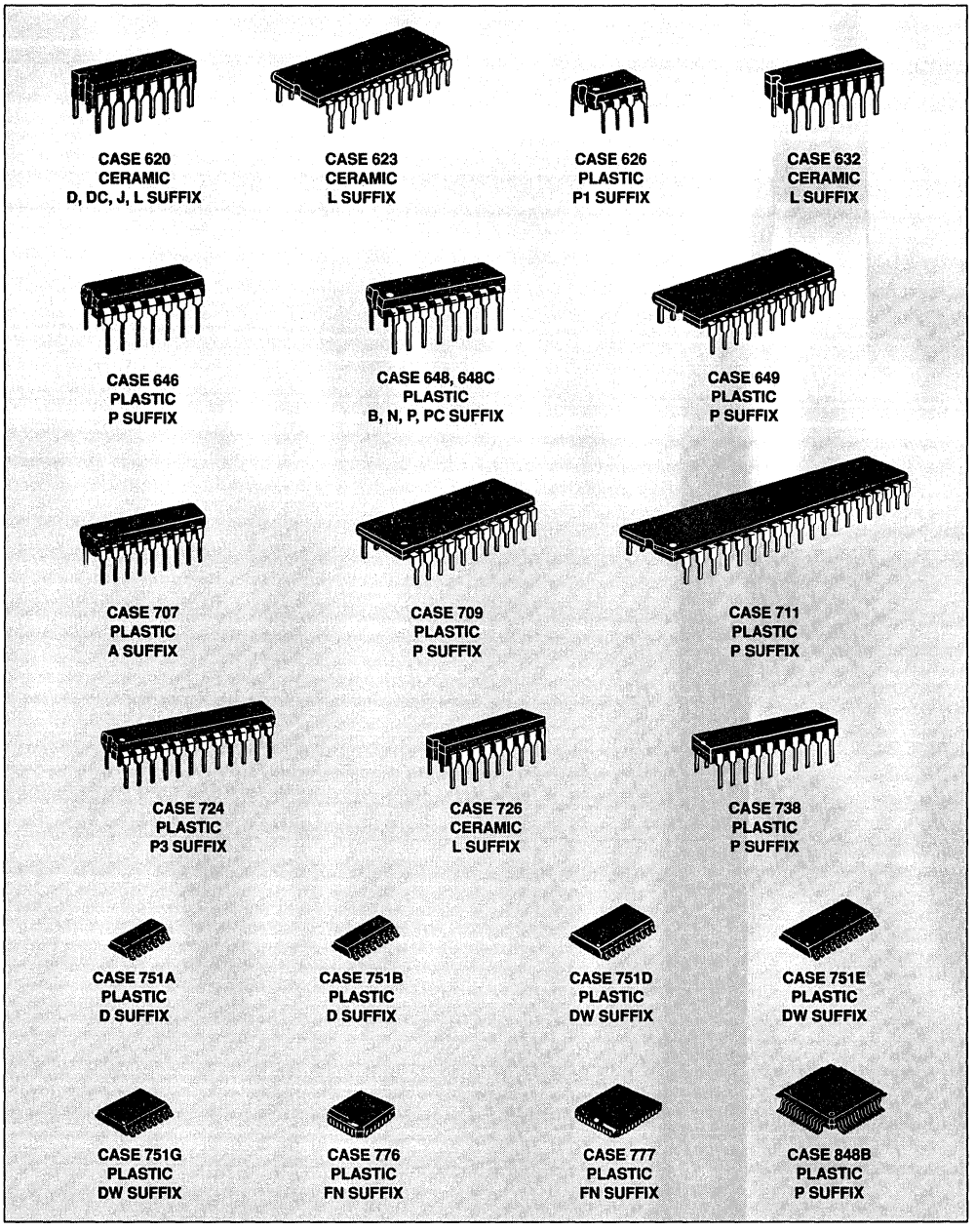
(1) Absolute maximum working voltage = 18 V
(2) On-chip current-limiting resistor

Functions

Device	Function	Package
MC14489	Multi-Character LED Display/Lamp Driver	738, 751D
MC14495♦1	Hexadecimal-to-7 Segment Latch/Decoder ROM/Driver	648, 751G
MC14499	4-Digit 7-Segment LED Display Decoder/Driver with Serial Interface	707, 751D
MC14511B	BCD-to-7-Segment Latch/Decoder/Driver	620, 648
MC14513B	BCD-to-7-Segment Latch/Decoder/Driver with Ripple Blanking	726, 707
MC14543B	BCD-to-7-Segment Latch/Decoder/Driver for Liquid Crystals	620, 648
MC14544B	BCD-to-7-Segment Latch/Decoder/Driver with Ripple Blanking	726, 707
MC14547B	High-Current BCD-to-7-Segment Decoder/Driver	620, 648
MC14558B	BCD-to-7-Segment Decoder	620, 648
MC145000	48-Segment Serial Input Multiplexed LCD Driver (Master)	709, 776
MC145001	44-Segment Serial Input Multiplexed LCD Driver (Slave)	707, 776
MC145453	33-Segment, Non-Multiplexed LCD Driver with Serial Interface	711, 777

♦Replace ♦ with package identifier (see product data).

Interface Package Overview



Interface Circuits

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

AM26LS30

Advance Information

Dual Differential (EIA-422-A)/ Quad Single-Ended (EIA-423-A) Line Drivers

DUAL DIFFERENTIAL/ QUAD SINGLE-ENDED LINE DRIVERS

SILICON MONOLITHIC INTEGRATED CIRCUIT

The AM26LS30 is a low power Schottky set of line drivers which can be configured as two differential drivers which comply with EIA-422-A standards, or as four single-ended drivers which comply with EIA-423-A standards. A mode select pin and appropriate choice of power supplies determine the mode. Each driver can source and sink currents in excess of 50 mA.

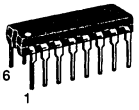
In the differential mode (EIA-422-A), the drivers can be used up to 10 Mbaud. A disable pin for each driver permits setting the outputs into a high impedance mode within a ±10 V common mode range.

In the single-ended mode (EIA-423-A) each driver has a slew rate control pin which permits setting the slew rate of the output signal so as to comply with EIA-423-A and FCC requirements and to reduce crosstalk. When operated from symmetrical supplies (±5.0 V), the outputs exhibit zero imbalance.

The AM26LS30 is available in a 16-pin plastic DIP and surface mount package. Ambient operating temperature range is –40° to +85°C.

- Operates as Two Differential EIA-422-A Drivers, or Four Single-Ended EIA-423-A Drivers
- High Impedance Outputs in Differential Mode
- Short Circuit Limit In Both Source and Sink Modes
- ± 10 V Common Mode Range on High Impedance Outputs
- ± 15 V Range on Inputs
- Low Current PNP Inputs Compatible with TTL, CMOS, and MOS Outputs
- Individual Output Slew Rate Control in Single-Ended Mode
- Replacement for the AMD AM25LS30 and National Semiconductor DS3691

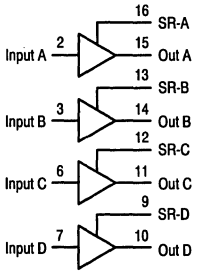
PC SUFFIX
PLASTIC PACKAGE
CASE 648



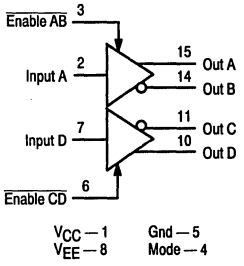
D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO-16)

BLOCK DIAGRAMS

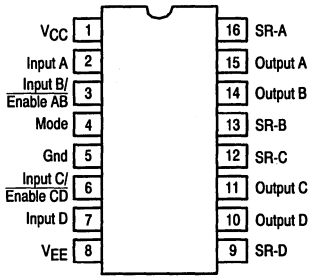
SINGLE-ENDED MODE EIA-423-A



DIFFERENTIAL MODE EIA-422-A



PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Part No.	Ambient Temperature Range	Package Type
AM26LS30PC MC26LS30D	–40° to +85°C	Plastic DIP SO-16

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MAXIMUM OPERATING CONDITIONS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	–0.5, +7.0 –7.0, +0.5	Vdc
Input Voltage (All Inputs)	V_{in}	–0.5, +20	Vdc
Applied Output Voltage when in High Impedance Mode (V_{CC} = 5.0 V, Pin 4 = Logic 0, Pins 3, 6 = Logic 1)	V_{za}	±15	Vdc
Output Voltage with V_{CC}, V_{EE} = 0 V	V_{zb}	±15	
Output Current	I_O	Self limiting	—
Junction Temperature	T_J	–65, +150	°C

Devices should not be operated at these limits. The "Recommended Operating Conditions" table provides conditions for actual device operation.

RECOMMENDED OPERATING CONDITIONS

Rating	Symbol	Min	Typ	Max	Unit
Power Supply Voltage (Differential Mode)	V_{CC} V_{EE}	+4.75 –0.5	5.0 0	+5.25 +0.3	Vdc
Power Supply Voltage (Single-Ended Mode)	V_{CC} V_{EE}	+4.75 –5.25	+5.0 –5.0	+5.25 –4.75	
Input Voltage (All Inputs)	V_{in}	0	—	+15	Vdc
Applied Output Voltage (when in High Impedance Mode)	V_{za}	–10	—	+10	
Applied Output Voltage, V_{CC} = 0	V_{zb}	–10	—	+10	
Output Current	I_O	–65	—	+65	mA
Operating Ambient Temperature (See text)	T_A	–40	—	+85	°C

All limits are not necessarily functional concurrently.

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ELECTRICAL CHARACTERISTICS (EIA-422-A differential mode, Pin 4 ≤ 0.8 V, –40°C < T_A < +85°C, +4.75 V ≤ V_{CC} ≤ +5.25 V, V_{EE} = Gnd, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Unit	Unit
Output Voltage (see Figure 1)					
Differential, R_L = ∞, V_{CC} = 5.25 V	$\|V_{OD1}\|$	—	4.2	6.0	Vdc
Differential, R_L = 100 Ω, V_{CC} = 4.75 V	$\|V_{OD2}\|$	2.0	2.6	—	Vdc
Change in Differential Voltage, R_L = 100 Ω (Note 4)	$\|\Delta V_{OD2}\|$	—	10	400	mVdc
Offset Voltage, R_L = 100 Ω	V_{OS}	—	2.5	3.0	Vdc
Change in Offset Voltage*, R_L = 100 Ω	$\|\Delta V_{OS}\|$	—	10	400	mVdc
Output Current (each output)					
Power Off Leakage, V_{CC} = 0, –10 V ≤ V_O ≤ +10 V	I_{OLK}	–100	0	+100	µA
High Impedance Mode, V_{CC} = 5.25 V, –10 V ≤ V_O ≤ +10 V	I_{OZ}	–100	0	+100	
Short Circuit Current (Note 2)					
High Output Shorted to Pin 5 (T_A = 25°C)	I_{SC-}	–150	–95	–60	mA
High Output Shorted to Pin 5 (–40°C < T_A < +85°C)	I_{SC-}	–150	—	–50	
Low Output Shorted to +6.0 V (T_A = 25°C)	I_{SC+}	60	75	150	
Low Output Shorted to +6.0 V (–40°C < T_A < +85°C)	I_{SC+}	50	—	150	
Inputs					
Low Level Voltage	V_{IL}	—	—	0.8	Vdc
High Level Voltage	V_{IH}	2.0	—	—	Vdc
Current @ V_{in} = 2.4 V	I_{IH}	—	0	40	µA
Current @ V_{in} = 15 V	I_{IHH}	—	0	100	
Current @ V_{in} = 0.4 V	I_{IL}	–200	–8.0	—	
Current, 0 ≤ V_{in} ≤ 15 V, V_{CC} = 0	I_{IX}	—	0	—	
Clamp Voltage (I_{in} = –12 mA)	V_{IK}	–1.5	—	—	Vdc
Power Supply Current (V_{CC} = +5.25 V, Outputs Open) (0 ≤ Enable ≤ V_{CC})	I_{CC}	—	16	30	mA

NOTES: 1. All voltages measured with respect to Pin 5.
2. Only one output shorted at a time, for not more than 1 second.
3. Typical values established at +25°C, V_{CC} = +5.0 V, V_{EE} = –5.0 V.
4. V_{in} switched from 0.8 to 2.0 V.
5. Imbalance is the difference between $|V_{O2}|$ with V_{in} < 0.8 V and $|V_{O2}|$ with V_{in} > 2.0 V.

TIMING CHARACTERISTICS (EIA-422-A differential mode, Pin 4 ≤ 0.8 V, T_A = +25°C, V_{CC} = +5.0 V, V_{EE} = Gnd, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Differential Output Rise Time (Figure 3)	t_r	—	70	200	ns
Differential Output Fall Time (Figure 3)	t_f				
Propagation Delay Time — Input to Differential Output					ns
Input Low to High (Figure 3)	t_{PDH}	—	90	200	
Input High to Low (Figure 3)	t_{PDL}	—	90	200	
Skew Timing (Figure 3)					ns
$\|t_{PDH}$ to $t_{PDL}\|$ for Each Driver	t_{SK1}	—	9.0	—	
Max to Min t_{PDH} Within a Package	t_{SK2}	—	2.0	—	
Max to Min t_{PDL} Within a Package	t_{SK3}	—	2.0	—	
Enable Timing (Figure 4)					ns
Enable to Active High Differential Output	t_{PZH}	—	150	300	
Enable to Active Low Differential Output	t_{PZL}	—	190	350	
Enable to 3-State Output From Active High	t_{PHZ}	—	80	350	
Enable to 3-State Output From Active Low	t_{PLZ}	—	110	300	

ELECTRICAL CHARACTERISTICS (EIA-423-A single-ended mode, Pin 4 ≥ 2.0 V, –40°C < T_A < +85°C, +4.75 V ≤ $\|V_{CC}\|$, $\|V_{EE}\|$ ≤ 5.25 V, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (V_{CC} = $\|V_{EE}\|$ = 4.75 V)					Vdc
Single-Ended Voltage, R_L = ∞ (Figure 2)	$\|V_{O1}\|$	4.0	4.2	6.0	
Single-Ended Voltage, R_L = 450 Ω (Figure 2)	$\|V_{O2}\|$	3.6	3.95	6.0	
Voltage Imbalance (Note 5), R_L = 450 Ω	$\|\Delta V_{O2}\|$	—	0.05	0.4	
Slew Control Current (Pins 16, 13, 12, 9)	I_{SLEW}	—	±120	—	µA
Output Current (Each Output)					
Power Off Leakage, V_{CC} = V_{EE} = 0, –6.0 V ≤ V_O ≤ +6.0 V	I_{OLK}	–100	0	+100	µA
Short Circuit Current (Output Short to Ground, Note 2)					
V_{in} ≤ 0.8 V (T_A = 25°C)	I_{SC+}	60	80	150	mA
V_{in} ≤ 0.8 V (–40°C < T_A < +85°C)	I_{SC+}	50	—	150	
V_{in} ≥ 2.0 V (T_A = 25°C)	I_{SC-}	–150	–95	–60	
V_{in} ≥ 2.0 V (–40°C < T_A < +85°C)	I_{SC-}	–150	—	–50	
Inputs					
Low Level Voltage	V_{IL}	—	—	0.8	Vdc
High Level Voltage	V_{IH}	2.0	—	—	Vdc
Current @ V_{in} = 2.4 V	I_{IH}	—	0	40	µA
Current @ V_{in} = 15 V	I_{IHH}	—	0	100	
Current @ V_{in} = 0.4 V	I_{IL}	–200	–8.0	—	
Current, 0 ≤ V_{in} ≤ 15 V, V_{CC} = 0	I_{IX}	—	0	—	
Clamp Voltage (I_{in} = –12 mA)	V_{IK}	–1.5	—	—	Vdc
Power Supply Current (Outputs Open)	I_{CC}	—	17	30	mA
V_{CC} = +5.25 V, V_{EE} = –5.25 V, V_{in} = 0.4 V	I_{EE}	–22	–8.0	—	

TIMING CHARACTERISTICS (EIA-423-A single-ended mode, Pin 4 ≥ 2.0 V, T_A = 25°C, V_{CC} = +5.0 V, V_{EE} = –5.0 V, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Timing (Figure 5)					
Output Rise Time, C_C = 0	t_r	—	65	300	ns
Output Fall Time, C_C = 0	t_f	—	65	300	
Output Rise Time, C_C = 50 pF	t_r	—	3.0	—	µs
Output Fall Time, C_C = 50 pF	t_f	—	3.0	—	
Rise Time Coefficient (Figure 16)	C_{rt}	—	0.06	—	µs/pF
Propagation Delay Time, Input to Single Ended Output (Figure 5)					ns
Input Low to High, C_C = 0	t_{PDH}	—	100	300	
Input High to Low, C_C = 0	t_{PDL}	—	100	300	
Skew Timing, C_C = 0 (Figure 5)					ns
$\|t_{PDH}$ to $t_{PDL}\|$ for Each Driver	t_{SK4}	—	15	—	
Max to Min t_{PDH} Within a Package	t_{SK5}	—	2.0	—	
Max to Min t_{PDL} Within a Package	t_{SK6}	—	5.0	—	

Table 1

Operation	V_{CC}	V_{EE}	Inputs					Outputs			
			Mode	A	B	C	D	A	B	C	D
Differential (EIA-422-A)	+5.0	Gnd	0	0	0	0	0	0	1	1	0
			0	1	0	0	1	1	0	0	1
			0	X	1	0	1	Z	Z	0	1
			0	1	0	0	0	1	0	1	0
			0	0	0	0	1	0	1	0	1
			0	1	0	1	X	1	0	Z	Z
Single-Ended (EIA-423-A)	+5.0	−5.0	1	0	0	0	0	0	0	0	0
			1	1	0	0	0	1	0	0	0
			1	0	1	0	0	0	1	0	0
			1	0	0	1	0	0	0	1	0
			1	0	0	0	1	0	0	0	1
X	0	X	X	X	X	X	X	Z	Z	Z	Z

X = Don't Care
Z = High Impedance (Off)

Figure 1. Differential Output Test

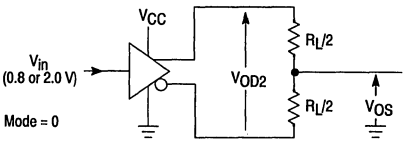


Figure 2. Single-Ended Output Test

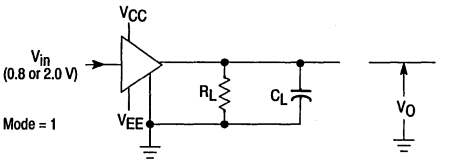
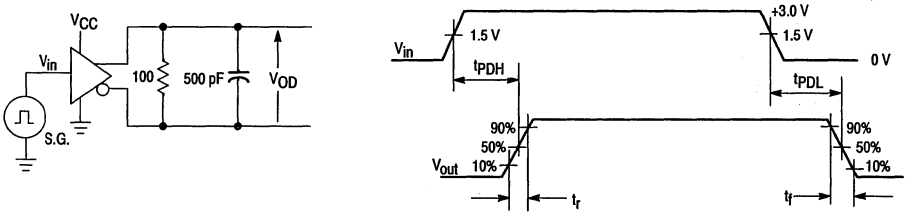
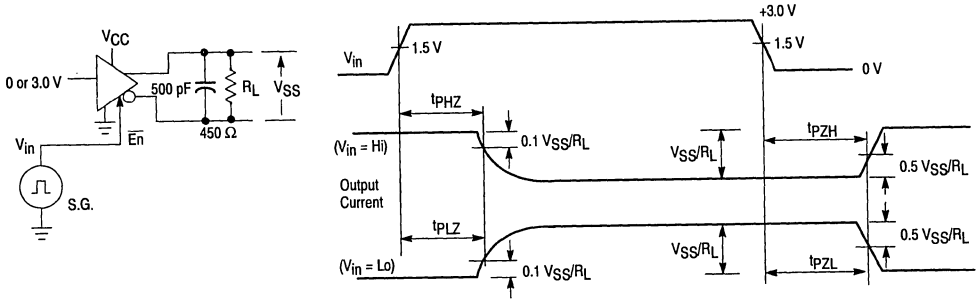


Figure 3. Differential Mode Rise/Fall Time and Data Propagation Delay



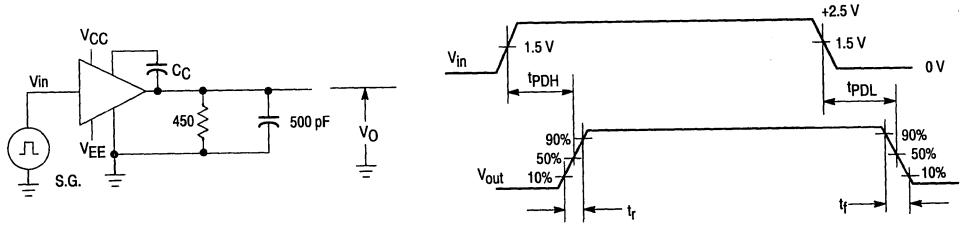
NOTES:
1. S.G. set to: f ≤ 1.0 MHz; duty cycle = 50%; t_r, t_f, ≤ 10 ns.
2. $t_{SK1} = |t_{PDH} - t_{PDL}|$ for each driver.
3. t_{SK2} computed by subtracting the shortest t_{PDH} from the longest t_{PDH} of the 2 drivers within a package.
4. t_{SK3} computed by subtracting the shortest t_{PDL} from the longest t_{PDL} of the 2 drivers within a package.

Figure 4. Differential Mode Enable Timing



NOTES:
1. S.G. set to: f ≤ 1.0 MHz; duty cycle = 50%; t_r, t_f, ≤ 10 ns.
2. Above tests conducted by monitoring output current levels.

Figure 5. Single-Ended Mode Rise/Fall Time and Data Propagation Delay



NOTES:
1. S.G. set to: f ≤ 100 kHz; duty cycle = 50%; t_r, t_f, ≤ 10 ns.
2. $t_{SK4} = |t_{PDH} - t_{PDL}|$ for each driver.
3. t_{SK5} computed by subtracting the shortest t_{PDH} from the longest t_{PDH} of the 4 drivers within a package.
4. t_{SK6} computed by subtracting the shortest t_{PDL} from the longest t_{PDL} of the 4 drivers within a package.

7

Figure 6. Differential Output Voltage versus Load Current

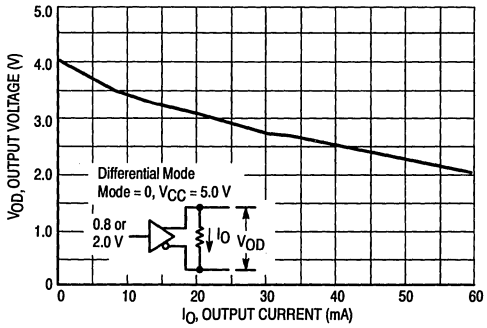


Figure 7. Internal Bias Current versus Load Current

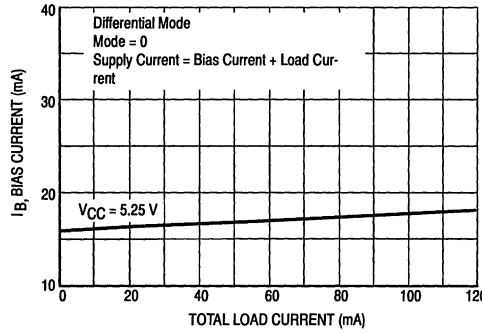


Figure 8. Short Circuit Current versus Output Voltage

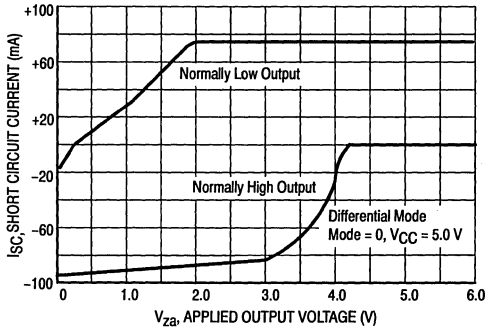


Figure 9. Input Current versus Input Voltage

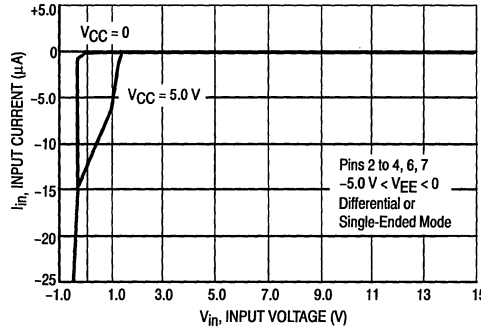


Figure 10. Output Voltage versus Output Source Current

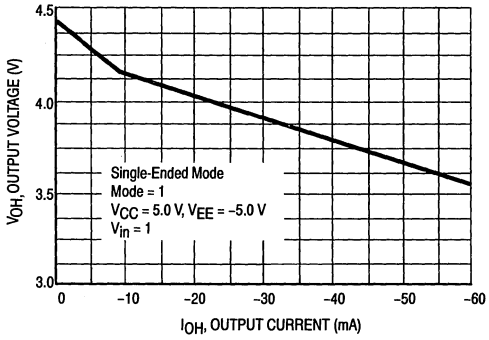


Figure 11. Output Voltage versus Output Sink Current

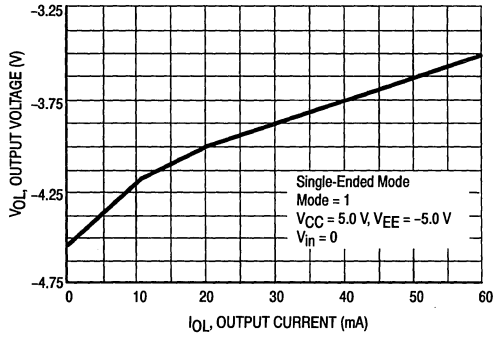


Figure 12. Internal Positive Bias Current versus Load Current

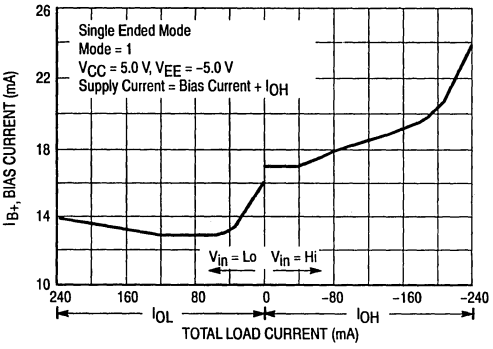


Figure 13. Internal Negative Bias Current versus Load Current

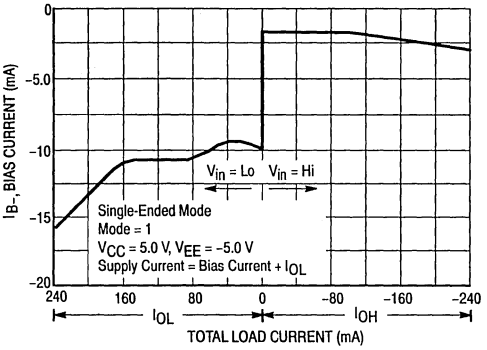


Figure 14. Short Circuit Current versus Output Voltage

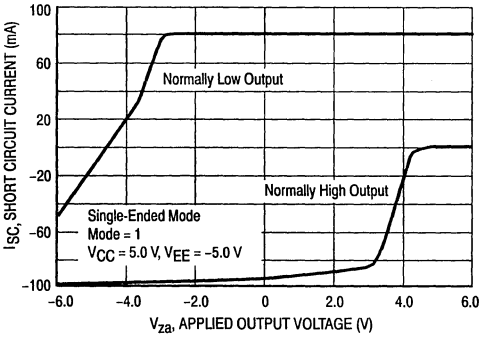


Figure 15. Short Circuit Current versus Temperature

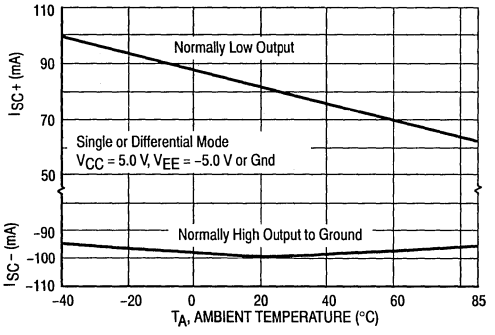
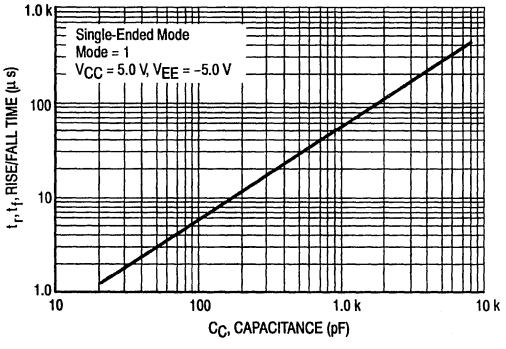


Figure 16. Rise/Fall Time versus Capacitance



APPLICATIONS INFORMATION

Description

The AM26LS30 is a dual function line driver – it can be configured as two differential output drivers which comply with EIA-422-A Standard, or as four single-ended drivers which comply with EIA-423-A Standard. The mode of operation is selected with the Mode pin (Pin 4) and appropriate power supplies (see Table 1). Each of the four outputs is capable of sourcing and sinking 60 to 70 mA while providing sufficient voltage to ensure proper data transmission.

As differential drivers, data rates to 10 Mbaud can be transmitted over a twisted pair for a distance determined by the cable characteristics. EIA-422-A Standard provides guidelines for cable length versus data rate. The advantage of a differential (balanced) system over a single-ended system is greater noise immunity, common mode rejection, and higher data rates.

Where extraneous noise sources are not a problem, the AM26LS30 may be configured as single-ended drivers transmitting data rates to 100 Kbaud. Crosstalk among wires within a cable is controlled by the use of the slew rate control pins on the AM26LS30.

Mode Selection

(Differential Mode)

In this mode (Pins 4 and 8 at ground), only a +5.0 V supply ±5% is required at V_{CC}. Pins 2 and 7 are the driver inputs, while Pins 10, 11, 14 and 15 are the outputs (see Block Diagram on page 1). The two outputs of a driver are always complementary and the differential voltage available at each pair of outputs is shown in Figure 6 for V_{CC} = 5.0 V. The differential output voltage will vary directly with V_{CC}. A "high" output can only source current, while a "low" output can only sink current (except for short circuit current – see Figure 8).

The two outputs will be in a high impedance mode when the respective Enable input (Pin 3 or 6) is high, or if $V_{CC} \leq 1.1$ V. Output leakage current over a common mode range of ±10 V is typically less than 1.0 µA.

The outputs have short circuit current limiting, typically, less than 100 mA over a voltage range of 0 to +6.0 V (see Figure 8). Short circuits should not be allowed to last indefinitely as the IC may be damaged.

Pins 9, 12, 13, and 16 are normally not used when in this mode, and should be left open.

(Single-Ended Mode)

In this mode (Pin 4 $\geq$ 2.0 V) V_{CC} requires +5.0 V, and V_{EE} requires –5.0 V, both ±5%. Pins 2, 3, 6, and 7 are inputs for the four drivers, and Pins 15, 14, 11, and 10 (respectively) are the outputs. The four drivers are independent of each other, and each output will be at a positive or a negative voltage depending on its input state, the load current, and the supply voltage. Figures 10 & 11 indicate the high and low output voltages for V_{CC} = 5.0 V, and V_{EE} = –5.0 V. The graph of Figure 10 will vary directly with V_{CC}, and the graph of Figure 11 will vary directly with V_{EE}. A "high" output can only source current, while a "low" output can only sink current (except short circuit current – see Figure 14).

The outputs will be in a high impedance mode only if $V_{CC} \leq 1.1$ V. Changing V_{EE} to 0 V does not set the outputs to a high impedance mode. Leakage current over a common mode range of ±10 V is typically less than 1.0 µA.

The outputs have short circuit current limiting, typically, less than 100 mA over a voltage range of ±6.0 V (see Figure 14). Short circuits should not be allowed to last indefinitely as the IC may be damaged.

Capacitors connected between Pins 9, 12, 13, and 16 and their respective outputs will provide slew rate limiting of the output transition. Figure 16 indicates the required capacitor value to obtain a desired rise or fall time (measured between the 10% and 90% points). The positive and negative transition times will be within ≈ ±5% of each other. Each output may be set to a different slew rate if desired.

Inputs

The five inputs determine the state of the outputs in accordance with Table 1. All inputs (regardless of the operating mode) have a nominal threshold of +1.3 V, and their voltage must be kept within the range of 0 V to +15 V for proper operation. If an input is taken more than 0.3 V below ground, excessive currents will flow, and the proper operation of the drivers will be affected. An open pin is equivalent to a logic high, but good design practices dictate that inputs should never be left open. Unused inputs should be connected to ground. The characteristics of the inputs are shown in Figure 9.

Power Supplies

V_{CC} requires +5.0 V, ±5%, regardless of the mode of operation. The supply current is determined by the IC's internal bias requirements, and the total load current. The internally required current is a function of the load current and is shown in Figure 7 for the differential mode.

In the single-ended mode, V_{EE} must be –5.0 V, ±5% in order to comply with EIA-423-A Standards. Figures 12 and 13 indicate the internally required bias currents as a function of total load current (the sum of the four output loads). The discontinuity at 0 load current exists due to a change in bias current when the inputs are switched. The supply currents vary ≈ ±2.0 mA as V_{CC} and V_{EE} are varied from |4.75 V| to |5.25 V|.

Sequencing of the supplies during power-up/power-down is not required.

Bypass capacitors (0.1 µF minimum on each supply pin) are recommended to ensure proper operation. Capacitors reduce noise induced onto the supply lines by the switching action of the drivers, particularly where long P.C. board tracks are involved. Additionally, the capacitors help absorb transients induced onto the drivers' outputs from the external cable (from ESD, motor noise, nearby computers, etc.).

Operating Temperature Range

The maximum ambient operating temperature, listed as +85°C, is actually a function of the system use (i.e., specifically how many drivers within a package are used) and at what current levels they are operating. The maximum power which may be dissipated within the package is determined by:

$$P_{Dmax} = \frac{T_{Jmax} - T_A}{R_{\theta JA}}$$

where $R_{\theta JA}$ = package thermal resistance which is typically:
67°C/W for the DIP (PC) package,
120°C/W for the SOIC (D) package,
T_{Jmax} = max. allowable junction temperature (150°C)
T_A = ambient air temperature near the IC package.

1) Differential Mode Power Dissipation

For the differential mode, the power dissipated within the package is calculated from:

$P_D = [(V_{CC} - V_{OD}) \bullet I_O]$(each driver) + $(V_{CC} \bullet I_B)$

where: V_{CC} = the supply voltage
V_{OD} = is taken from Figure 6 for the known value of I_O
I_B = the internal bias current (Figure 7)

As indicated in the equation, the first term (in brackets) must be calculated and summed for each of the two drivers, while the last term is common to the entire package. Note that the term $(V_{CC} - V_{OD})$ is constant for a given value of I_O and does not vary with V_{CC}. For an application involving the following conditions:

T_A = +85°C, I_O = –60 mA (each driver), V_{CC} = 5.25 V, the suitability of the package types is calculated as follows.

The power dissipated is:

P_D = [3.0 V • 60 mA • 2] + (5.25 V • 18 mA)
P_D = 454 mW

The junction temperature calculates to:

T_J = 85°C + (0.454 W • 67°C/W) = 115°C for the DIP package,
T_J = 85°C + (0.454 W • 120°C/W) = 139°C for the SOIC package.

Since the maximum allowable junction temperature is not exceeded in any of the above cases, either package can be used in this application.

2) Single-Ended Mode Power Dissipation

For the single-ended mode, the power dissipated within the package is calculated from:

$$P_D = (I_{B+} \bullet V_{CC}) + (I_{B-} \bullet V_{EE}) + [(I_O \bullet (V_{CC} - V_{OH})]$$(each driver)

The above equation assumes I_O has the same magnitude for both output states, and makes use of the fact that the absolute value of the graphs of Figures 10 and 11 are nearly identical. I_{B+} and I_{B-} are obtained from the right half of Figures 12 and 13, and $(V_{CC} - V_{OH})$ can be obtained from Figure 10. Note that the term $(V_{CC} - V_{OH})$ is constant for a given value of I_O and does not vary with V_{CC}. For an application involving the following conditions:

T_A = +85°C, I_O = –60 mA (each driver), V_{CC} = 5.25 V, V_{EE} = –5.25 V, the suitability of the package types is calculated as follows.

The power dissipated is:

P_D = (24 mA • 5.25 V) + (–3.0 mA • –5.25 V) + [60 mA • 1.45 V • 4.0]
P_D = 490 mW

The junction temperature calculates to:

T_J = 85°C + (0.490 W • 67°C/W) = 118°C for the DIP package,
T_J = 85°C + (0.490 W • 120°C/W) = 144°C for the SOIC package.

Since the maximum allowable junction temperature is not exceeded in any of the above cases, either package can be used in this application.

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SYSTEM EXAMPLES

Differential System

An example of a typical EIA-422-A system is shown in Figure 17. Although EIA-422-A does not specifically address multiple driver situations, the AM26LS30 can be used in this manner since the outputs can be put into a high impedance mode. It is, however, the system designer's responsibility to ensure the Enable pins are properly controlled so as to prevent two drivers on the same cable from being "on" at the same time.

The limit on the number of receivers and drivers which may be connected on one system is determined by the input current of each receiver, the maximum leakage current of each "off" driver, and the DC current through each terminating resistor. The sum of these currents must not exceed the capability of the "on" driver (≈60 mA). If the cable is of any significant length, with receivers at various points along its length, the common mode voltage may vary along its length, and this parameter must be considered when calculating the maximum driver current.

The cable requirements are defined not only by the AC characteristics and the data rate, but also by the DC resistance. The maximum resistance must be such that the minimum voltage across any receiver inputs is never less than 200 mV.

The ground terminals of each driver and receiver in Figure 17 must be connected together by a dedicated wire (or the shield) in the cable so as to provide a common reference. Chassis grounds or power line grounds should not be relied on for this common connection as they may generate significant common mode differences. Additionally, they usually do not provide a sufficiently low impedance at the frequencies of interest.

Single-Ended System

An example of a typical EIA-423-A system is shown in Figure 18. Multiple drivers on a single data line are not possible since the drivers cannot be put into a high impedance mode. Although each driver is shown connected to a single receiver, multiple receivers can be driven from a single driver as long as the total load current of the receivers and the terminating resistor does not exceed the capability of the driver (≈60 mA). If the cable is of any significant length, with receivers at various points along its length, the common mode voltage may vary along its length, and this parameter must be considered when calculating the maximum driver current.

The cable requirements are defined not only by the AC characteristics and the data rate, but also by the DC resistance. The maximum resistance must be such that the minimum voltage across any receiver inputs is never less than 200 mV.

The ground terminals of each driver and receiver in Figure 18 must be connected together by a dedicated wire (or the shield) in the cable so as to provide a common reference. Chassis grounds or power line grounds should not be relied on for this common connection as they may generate significant common mode differences. Additionally, they usually do not provide a sufficiently low impedance at the frequencies of interest.

Additional Modes of Operation

If compliance with EIA-422-A or EIA-423-A Standard is not required in a particular application, the AM26LS30 can be operated in two other modes.

1) The device may be operated in the differential mode (Pin 4 = 0) with V_{EE} connected to any voltage between ground and –5.25 V. Outputs in the low state will be referenced to V_{EE}, resulting in a differential output voltage greater than that shown in Figure 6. The Enable pins will operate the same as previously described.

2) The device may be operated in the single-ended mode (Pin 4 = 1) with V_{EE} connected to any voltage between ground and –5.25 V. Outputs in the high state will be at a voltage as shown in Figure 10, while outputs in a low state will be referenced to V_{EE}.

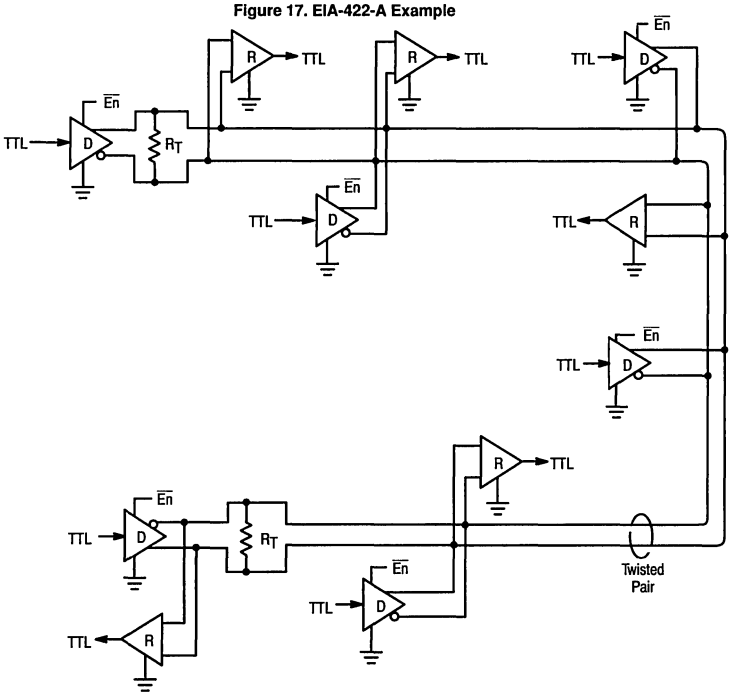
Termination Resistors

Transmission line theory states that, in order to preserve the shape and integrity of a waveform traveling along a cable, the cable must be terminated in an impedance equal to its characteristic impedance. In a system such as that depicted in Figure 17, in which data can travel in both directions, both physical ends of the cable must be terminated. Stubs leading to each receiver and driver should be as short as possible.

In a system such as that depicted in Figure 18, in which data normally travels in one direction only, a terminator is theoretically required only at the receiving end of the cable. However, if the cable is in a location where noise spikes of several volts can be induced onto it, then a terminator (preferably a series resistor) should be placed at the driver end to prevent damage to the driver.

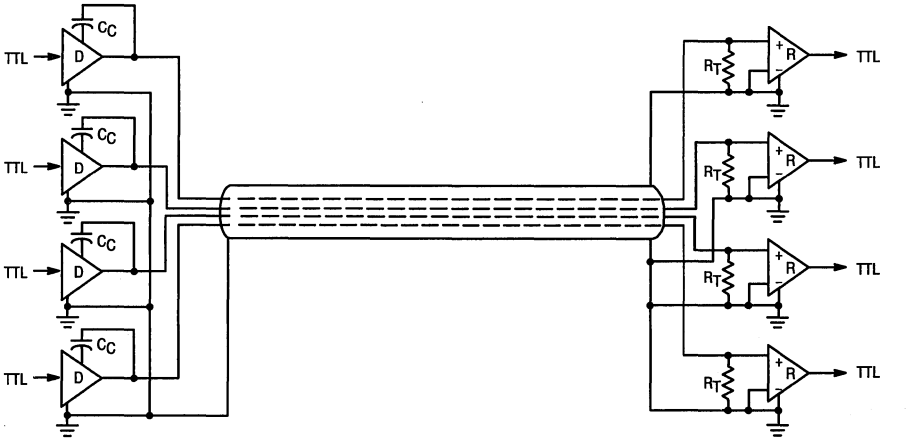
Leaving off the terminations will generally result in reflections which can have amplitudes of several volts above V_{CC} or several volts below ground or V_{EE}. These overshoots/undershoots can disrupt the driver and/or receiver, create false data, and in some cases, damage components on the bus.

Figure 17. EIA-422-A Example



NOTES:
1. Terminating resistors R_T should be located at the physical ends of the cable.
2. Stubs should be as short as possible.
3. Receivers = AM26LS32, MC3486, MC75173 or MC75175.
4. Circuit grounds must be connected together through a dedicated wire.

Figure 18. EIA-423-A Example



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

AM26LS31

QUAD LINE DRIVER WITH NAND ENABLED THREE-STATE OUTPUTS

The Motorola AM26LS31 is a quad differential line driver intended for digital data transmission over balanced lines. It meets all the requirements of EIA-422 Standard and Federal Standard 1020.

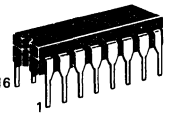
The AM26LS31 provides an enable/disable function common to all four drivers as opposed to the split enables on the MC3487 EIA-422 driver.

The high impedance output state is assured during power down.

- Full EIA-422 Standard Compliance
- Single +5.0 V Supply
- Meets Full V_O = 6.0 V, V_{CC} = 0 V, I_O < 100 μA Requirement
- Output Short Circuit Protection
- Complementary Outputs for Balanced Line Operation
- High Output Drive Capability
- Advanced LS Processing
- PNP Inputs for MOS Compatibility

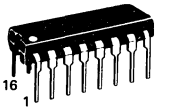
QUAD EIA-422 LINE DRIVER WITH THREE-STATE OUTPUTS

SILICON MONOLITHIC INTEGRATED CIRCUIT



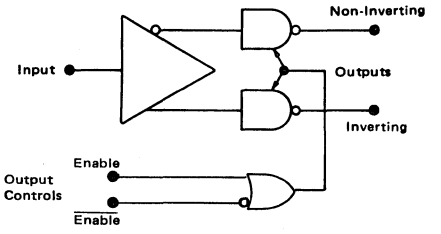
DC SUFFIX
CERAMIC PACKAGE
CASE 620

D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO-16)

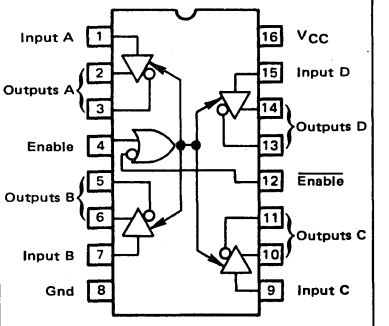


PC SUFFIX
PLASTIC PACKAGE
CASE 648

DRIVER BLOCK DIAGRAM



PIN CONNECTIONS



TRUTH TABLE

Input	Control Inputs (E/$\overline{E}$)	Non-Inverting Output	Inverting Output
H	H/L	H	L
L	H/L	L	H
X	L/H	Z	Z

L = Low Logic State
H = High Logic State
X = Irrelevant
Z = Third-State (High Impedance)

ORDERING INFORMATION

Device	Temperature Range	Package
AM26LS31DC	0 to 70°C	Ceramic DIP
AM26LS31PC		Plastic DIP
MC26LS31D*		SO-16

*Note that the surface mount MC26LS31D devices use the same die as in the ceramic and plastic DIP AM26LS31DC devices, but with an MC prefix to prevent confusion with the package suffixes.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	8.0	Vdc
Input Voltage	V_I	5.5	Vdc
Operating Ambient Temperature Range	T_A	0 to +70	°C
Operating Junction Temperature Range Ceramic Package Plastic Package	T_J	 175 150	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (Unless otherwise noted specifications apply 4.75 V ≤ V_{CC} ≤ 5.25 V and 0°C ≤ T_A ≤ 70°C. Typical values measured at V_{CC} = 5.0 V, and T_A = 25°C.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Voltage — Low Logic State	V_{IL}	—	—	0.8	Vdc
Input Voltage — High Logic State	V_{IH}	2.0	—	—	Vdc
Input Current — Low Logic State (V_{IL} = 0.4 V)	I_{IL}	—	—	−360	μA
Input Current — High Logic State (V_{IH} = 2.7 V) (V_{IH} = 7.0 V)	I_{IH}	 — —	 — —	 +20 +100	μA
Input Clamp Voltage (I_{IK} = −18 mA)	V_{IK}	—	—	−1.5	V
Output Voltage — Low Logic State (I_{OL} = 20 mA)	V_{OL}	—	—	0.5	V
Output Voltage — High Logic State (I_{OH} = −20 mA)	V_{OH}	2.5	—	—	V
Output Short Circuit Current (V_{IH} = 2.0 V) Note 1	I_{OS}	−30	—	−150	mA
Output Leakage Current — Hi-Z State (V_{OL} = 0.5 V, $V_{IL(E)}$ = 0.8 V, $V_{IH(\overline{E})}$ = 2.0 V) (V_{OH} = 2.5 V, $V_{IL(E)}$ = 0.8 V, $V_{IH(\overline{E})}$ = 2.0 V)	$I_{O(Z)}$	 — —	 — —	 −20 +20	μA
Output Leakage Current — Power OFF (V_{OH} = 6.0 V, V_{CC} = 0 V) (V_{OL} = −0.25 V, V_{CC} = 0 V)	$I_{O(off)}$	 — —	 — —	 +100 −100	μA
Output Offset Voltage Difference, Note 2	$V_{OS}-\overline{V}_{OS}$	—	—	±0.4	V
Output Differential Voltage, Note 2	V_{OD}	2.0	—	—	V
Output Differential Voltage Difference, Note 2	$\lvert\Delta V_{OD}\rvert$	—	—	±0.4	V
Power Supply Current (Output Disabled) Note 3	I_{CCX}	—	60	80	mA

1. Only one output may be shorted at a time.
2. See EIA Specification EIA-422 for exact test conditions.
3. Circuit in three-state condition.

SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Times High to Low Output Low to High Output	 t_{PHL} t_{PLH}	 — —	 — —	 20 20	ns
Output Skew		—	—	6.0	ns
Propagation Delay — Control to Output (C_L = 10 pF, R_L = 75 Ω to Gnd) (C_L = 10 pF, R_L = 180 Ω to V_{CC}) (C_L = 30 pF, R_L = 75 Ω to Gnd) (C_L = 30 pF, R_L = 180 Ω to V_{CC})	 $t_{PHZ(E)}$ $t_{PLZ(E)}$ $t_{PZH(E)}$ $t_{PZL(E)}$	 — — — —	 — — — —	 30 35 40 45	ns

7

FIGURE 1 — THREE-STATE ENABLE TEST CIRCUIT AND WAVEFORMS

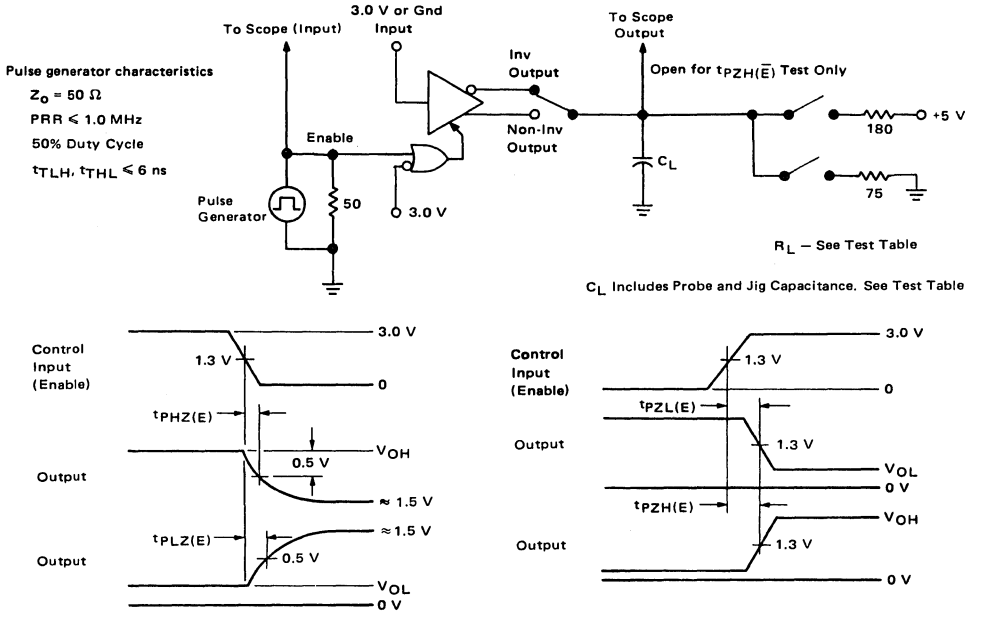
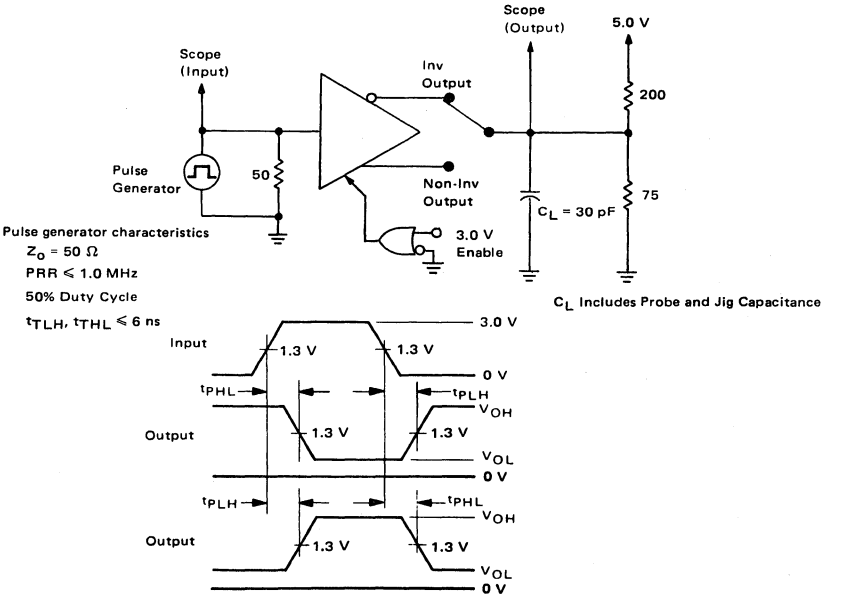


FIGURE 2 — PROPAGATION DELAY TIMES INPUT TO OUTPUT WAVEFORMS AND TEST CIRCUIT



AM26LS32

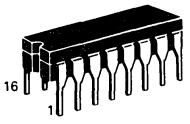
QUAD EIA-422/423 LINE RECEIVER

Motorola's Quad EIA-422/3 Receiver features four independent receiver chains which comply with EIA Standards for the Electrical Characteristics of Balanced/Unbalanced Voltage Digital Interface Circuits. Receiver outputs are 74LS compatible, three-state structures which are forced to a high impedance state when Pin 4 is a Logic "0" and Pin 12 is a Logic "1." A PNP device buffers each output control pin to assure minimum loading for either Logic "1" or Logic "0" inputs. In addition, each receiver chain has internal hysteresis circuitry to improve noise margin and discourage output instability for slowly changing input waveforms. A summary of AM26LS32 features include:

- Four Independent Receiver Chains
- Three-State Outputs
- High Impedance Output Control Inputs (PIA Compatible)
- Internal Hysteresis — 30 mV (Typ) @ Zero Volts Common Mode
- Fast Propagation Times — 25 ns (Typ)
- TTL Compatible
- Single 5 V Supply Voltage
- Fail-Safe Input-Output Relationship. Output Always High When Inputs Are Open, Terminated or Shorted
- 6 k Minimum Input Impedance

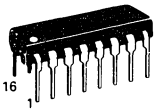
QUAD EIA-422/3 LINE RECEIVER WITH THREE-STATE OUTPUTS

SILICON MONOLITHIC INTEGRATED CIRCUIT



DC SUFFIX
CERAMIC PACKAGE
CASE 620

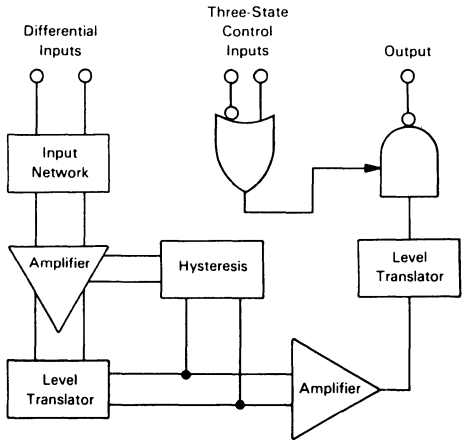
D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO-16)



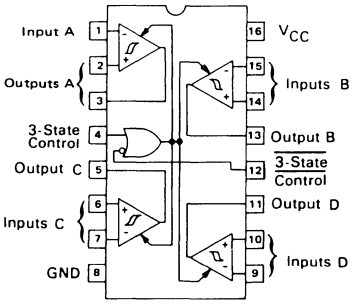
PC SUFFIX
PLASTIC PACKAGE
CASE 648

7

RECEIVER CHAIN BLOCK DIAGRAM



PIN CONNECTIONS



ORDERING INFORMATION

Device	Temperature	Package
AM26LS32DC	0 to 70°C	Ceramic DIP
AM26LS32PC		Plastic DIP
MC26LS32D*		SO-16

*Note that the surface mount MC26LS32D devices use the same die as in the ceramic and plastic DIP AM26LS32DC devices, but with an MC prefix to prevent confusion with the package suffixes.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	7.0	Vdc
Input Common Mode Voltage	V_{ICM}	±25	Vdc
Input Differential Voltage	V_{ID}	±25	Vdc
Three-State Control Input Voltage	V_I	7.0	Vdc
Output Sink Current	I_O	50	mA
Storage Temperature	T_{stg}	−65 to +150	°C
Operating Junction Temperature	T_J		°C
Ceramic Package		+175	
Plastic Package		+150	

RECOMMENDED OPERATING CONDITIONS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	4.75 to 5.25	Vdc
Operating Ambient Temperature	T_A	0 to +70	°C
Input Common Mode Voltage Range	V_{ICR}	−7.0 to +7.0	Vdc
Input Differential Voltage Range	V_{IDR}	6.0	Vdc

ELECTRICAL CHARACTERISTICS (Unless otherwise noted minimum and maximum limits apply over recommended temperature and power supply voltage ranges. Typical values are for T_A = 25°C, V_{CC} = 5.0 V and V_{IC} = 0 V. See Note 1.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Voltage — High Logic State (Three-State Control)	V_{IH}	2.0	–	–	V
Input Voltage — Low Logic State (Three-State Control)	V_{IL}	–	–	0.8	V
Differential Input Threshold Voltage (Note 2)	$V_{TH(D)}$				V
(−7.0 V ≤ V_{IC} ≤ 7.0 V, V_{IH} = 2.0 V)					
(I_O = −0.4 mA, V_{OH} ≥ 2.7 V)		–	–	0.2	
(I_O = 8.0 mA, V_{OL} ≤ 0.45 V)		–	–	-0.2	
Input Bias Current	$I_{IB(D)}$				mA
(V_{CC} = 0 V or 5.25) (Other Inputs at −15 V ≤ V_{in} ≤ +15 V)					
V_{in} = +15 V		–	–	2.3	
V_{in} = −15 V		–	–	-2.8	
Input Resistance (−15 V ≤ V_{in} ≤ +15 V)	R_{in}	6.0 K	–	–	Ohms
Input Balance and Output Level					V
(−7.0 V ≤ V_{IC} ≤ 7.0 V, V_{IH} = 2.0 V, See Note 3)					
(I_O = -0.4 mA, V_{ID} = 0.4 V)	V_{OH}	2.7	–	–	
(I_O = 8.0 mA, V_{ID} = -0.4 V)	V_{OL}	–	–	0.45	
Output Third State Leakage Current	I_{OZ}				μA
($V_{I(D)}$ = +3.0 V, V_{IL} = 0.8 V, V_O = 0.4 V)		–	–	-20	
($V_{I(D)}$ = −3.0 V, V_{IL} = 0.8 V, V_O = 2.4 V)		–	–	20	
Output Short Circuit Current ($V_{I(D)}$ = 3.0 V, V_{IH} = 2.0 V, V_O = 0 V, See Note 4)	I_{OS}	−15	–	-85	mA
Input Current — Low Logic State (Three-State Control) (V_{IL} = 0.4 V)	I_{IL}	–	–	-360	μA
Input Current — High Logic State (Three-State Control)	I_{IH}				μA
(V_{IH} = 2.7 V)		–	–	20	
(V_{IH} = 5.5 V)		–	–	100	
Input Clamp Diode Voltage (Three-State Control)	V_{IK}	–	–	-1.5	V
(I_{IC} = −18 mA)					
Power Supply Current (V_{IL} = 0 V) (All Inputs Grounded)	I_{CC}	–	–	70	mA

NOTES:
1. All currents into device pins are shown as positive, out of device pins are negative. All voltages referenced to ground unless otherwise noted.
2. Differential input threshold voltage and guaranteed output levels are done simultaneously for worst case.
3. Refer to EIA-422/3 for exact conditions. Input balance and guaranteed output levels are done simultaneously for worst case.
4. Only one output at a time should be shorted.

SWITCHING CHARACTERISTICS (Unless otherwise noted, V_{CC} = 5.0 V and T_A = 25°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Time — Differential Inputs to Output					ns
(Output High to Low)	$t_{PHL(D)}$	–	–	30	
(Output Low to High)	$t_{PLH(D)}$	–	–	30	
Propagation Delay Time — Three-State Control to Output					ns
(Output Low to Third State)	t_{PLZ}	–	–	35	
(Output High to Third State)	t_{PHZ}	–	–	35	
(Output Third State to High)	t_{PZH}	–	–	30	
(Output Third State to Low)	t_{PZL}	–	–	30	

SWITCHING TEST CIRCUIT AND WAVE FOR FIGURE 1 - PROPAGATION DELAY DIFFERENTIAL INPUT TO OUTPUT

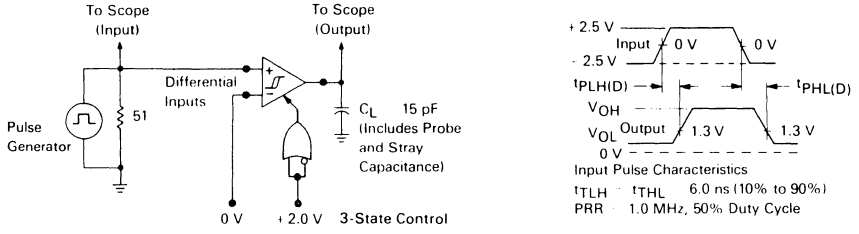
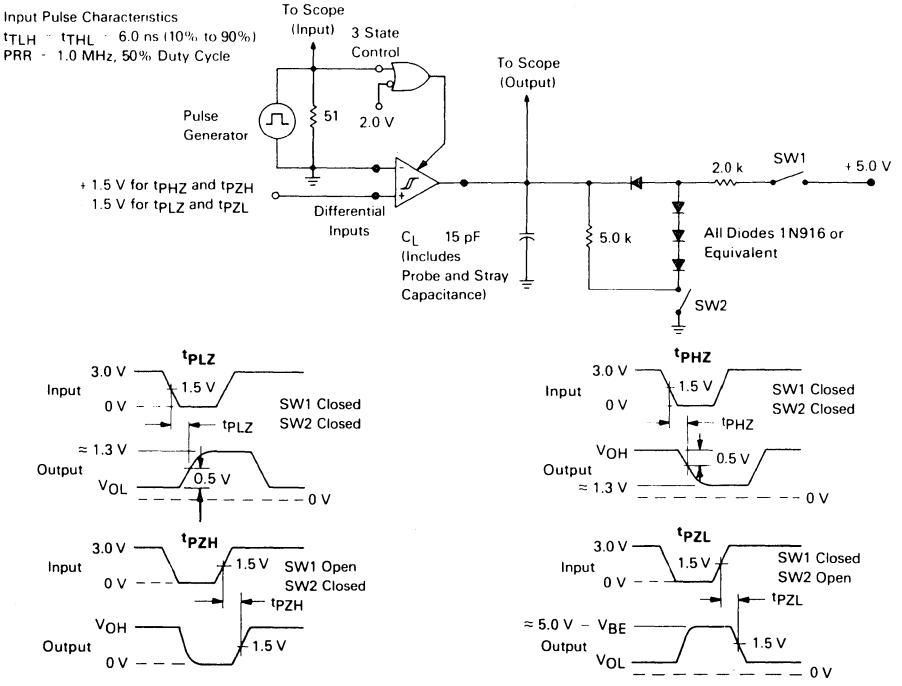


FIGURE 2 — PROPAGATION DELAY THREE-STATE CONTROL INPUT TO OUTPUT



MC8T26A
(MC6880A)

QUAD THREE-STATE BUS TRANSCEIVER

This quad three-state bus transceiver features both excellent MOS or MPU compatibility, due to its high impedance PNP transistor input, and high-speed operation made possible by the use of Schottky diode clamping. Both the −48 mA driver and −20 mA receiver outputs are short-circuit protected and employ three-state enabling inputs.

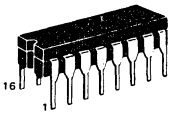
The device is useful as a bus extender in systems employing the M6800 family or other comparable MPU devices. The maximum input current of 200 μA at any of the device input pins assures proper operation despite the limited drive capability of the MPU chip. The inputs are also protected with Schottky-barrier diode clamps to suppress excessive undershoot voltages.

The MC8T26A is identical to the NE8T26A and it operates from a single +5 V supply.

- High Impedance Inputs
- Single Power Supply
- High Speed Schottky Technology
- Three-State Drivers and Receivers
- Compatible with M6800 Family Microprocessor

QUAD THREE-STATE BUS TRANSCEIVER

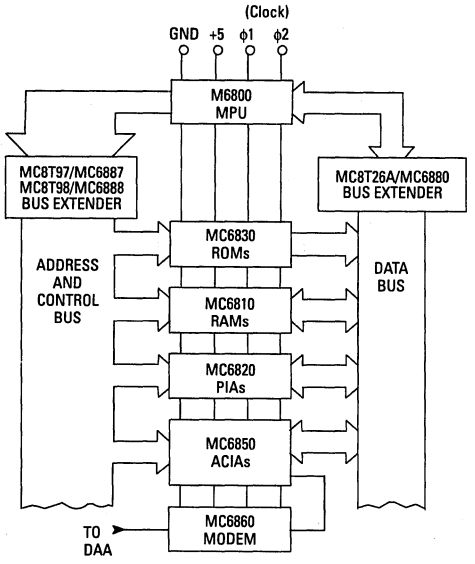
MONOLITHIC SCHOTTKY INTEGRATED CIRCUITS



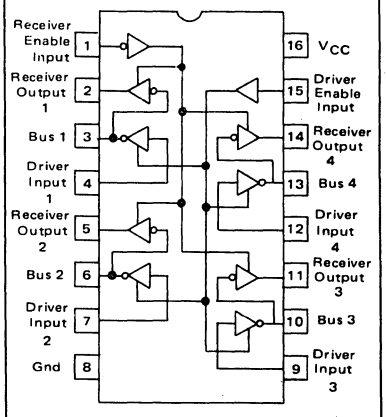
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

MICROPROCESSOR BUS EXTENDER APPLICATION



PIN CONNECTIONS — MC8T26A (MC6880A)



ORDERING INFORMATION

Device	Alternate	Temperature Range	Package
MC8T26AL	MC6880AL	0 to +75°C	Ceramic DIP
MC8T26AP	MC6880AP		Plastic DIP

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	8.0	Vdc
Input Voltage	V_I	5.5	Vdc
Junction Temperature Ceramic Package Plastic Package	T_J	 175 150	°C
Operating Ambient Temperature Range	T_A	0 to +75	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (4.75 V ≤ V_{CC} ≤ 5.25 V and 0°C ≤ T_A ≤ 75°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Current – Low Logic State					
(Receiver Enable Input, $V_{IL(RE)}$ = 0.4 V)	$I_{IL(\overline{RE})}$	–	–	-200	μA
(Driver Enable Input, $V_{IL(DE)}$ = 0.4 V)	$I_{IL(DE)}$	–	–	-200	
(Driver Input, $V_{IL(D)}$ = 0.4 V)	$I_{IL(D)}$	–	–	-200	
(Bus (Receiver) Input, $V_{IL(B)}$ = 0.4 V)	$I_{IL(B)}$	–	–	-200	
Input Disabled Current – Low Logic State					
(Driver Input, $V_{IL(D)}$ = 0.4 V)	$I_{IL(D)\ DIS}$	–	–	-25	μA
Input Current-High Logic State					
(Receiver Enable Input, $V_{IH(RE)}$ = 5.25 V)	$I_{IH(\overline{RE})}$	–	–	25	μA
(Driver Enable Input, $V_{IH(DE)}$ = 5.25 V)	$I_{IH(DE)}$	–	–	25	
(Driver Input, $V_{IH(D)}$ = 5.25 V)	$I_{IH(D)}$	–	–	25	
(Receiver Input, $V_{IH(B)}$ = 5.25 V)	$I_{IH(B)}$	–	–	100	
Input Voltage – Low Logic State					
(Receiver Enable Input)	$V_{IL(\overline{RE})}$	–	–	0.85	V
(Driver Enable Input	$V_{IL(DE)}$	–	–	0.85	
(Driver Input)	$V_{IL(D)}$	–	–	0.85	
(Receiver Input)	$V_{IL(B)}$	–	–	0.85	
Input Voltage – High Logic State					
(Receiver Enable Input)	$V_{IH(\overline{RE})}$	2.0	–	–	V
(Driver Enable Input)	$V_{IH(DE)}$	2.0	–	–	
(Driver Input)	$V_{IH(D)}$	2.0	–	–	
(Receiver Input)	$V_{IH(B)}$	2.0	–	–	
Output Voltage – Low Logic State					
(Bus Driver) Output, $I_{OL(B)}$ = 48 mA)	$V_{OL(B)}$	–	–	0.5	V
(Receiver Output, $I_{OL(R)}$ = 20 mA)	$V_{OL(R)}$	–	–	0.5	
Output Voltage – High Logic State					
(Bus (Driver) Output, $I_{OH(B)}$ = –10 mA)	$V_{OH(B)}$	2.4	3.1	–	V
(Receiver Output, $I_{OH(R)}$ = –2.0 mA)	$V_{OH(R)}$	2.4	3.1	–	
(Receiver Output, $I_{OH(R)}$ = –100 μA, V_{CC} = 5.0 V)		3.5	–	–	
Output Disabled Leakage Current – High Logic State					
(Bus Driver) Output, $V_{OH(B)}$ = 2.4 V)	$I_{OHL(B)}$	–	–	100	μA
(Receiver Output, $V_{OH(R)}$ = 2.4 V)	$I_{OHL(R)}$	–	–	100	
Output Disabled Leakage Current – Low Logic State					
(Bus Output, $V_{OL(B)}$ = 0.5 V)	$I_{OLL(B)}$	–	–	–100	μA
(Receiver Output, $V_{OL(R)}$ = 0.5 V)	$I_{OLL(R)}$	–	–	–100	
Input Clamp Voltage					
(Driver Enable Input $I_{ID(DE)}$ = –12 mA)	$V_{IC(DE)}$	–	–	-1.0	V
(Receiver Enable Input $I_{IC(RE)}$ = +12 mA)	$V_{IC(RE)}$	–	–	-1.0	
(Driver Input $I_{IC(D)}$ = –12 mA)	$V_{IC(D)}$	–	–	-1.0	
Output Short Circuit Current, V_{CC} = 5.25 V, Note 1					
(Bus (Driver) Output)	$I_{OS(B)}$	-50	–	-150	mA
(Receiver Output)	$I_{OS(R)}$	-30	–	-75	
Power Supply Current (V_{CC} = 5.25 V)	I_{CC}	–	–	87	mA

Note 1. Only one output may be short-circuited at a time.

SWITCHING CHARACTERISTICS (Unless otherwise noted, specifications apply at $T_A = 25^oC$ and $V_{CC} = 5.0$ V)

Characteristic	Symbol	Figure	Min	Max	Unit
Propagation Delay Time from Receiver (Bus) Input to High Logic State Receiver Output	$t_{PLH(R)}$	1	–	14	ns
Propagation Delay Time from Receiver (Bus) Input to Low Logic State Receiver Output	$t_{PHL(R)}$	1	–	14	ns
Propagation Delay Time from Driver Input to High Logic State Driver (Bus) Output	$t_{PLH(D)}$	2	–	14	ns
Propagation Delay Time from Driver Input to Low Logic State Driver (Bus) Output	$t_{PHL(D)}$	2	–	14	ns
Propagation Delay Time from $\overline{\text{Receiver Enable}}$ Input to High Impedance (Open) Logic State Receiver Output	$t_{PLZ(RE)}$	3	–	15	ns
Propagation Delay Time from $\overline{\text{Receiver Enable}}$ Input to Low Logic Level Receiver Output	$t_{PZL(RE)}$	3	–	20	ns
Propagation Delay Time from Driver Enable Input to High Impedance Logic State Driver (Bus) Output	$t_{PLZ(DE)}$	4	–	20	ns
Propagation Delay Time from Driver Enable Input to Low Logic State Driver (Bus) Output	$t_{PZL(DE)}$	4	–	25	ns

FIGURE 1 – TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY FROM BUS (RECEIVER) INPUT TO RECEIVER OUTPUT, $t_{PLH(R)}$ AND $t_{PHL(R)}$

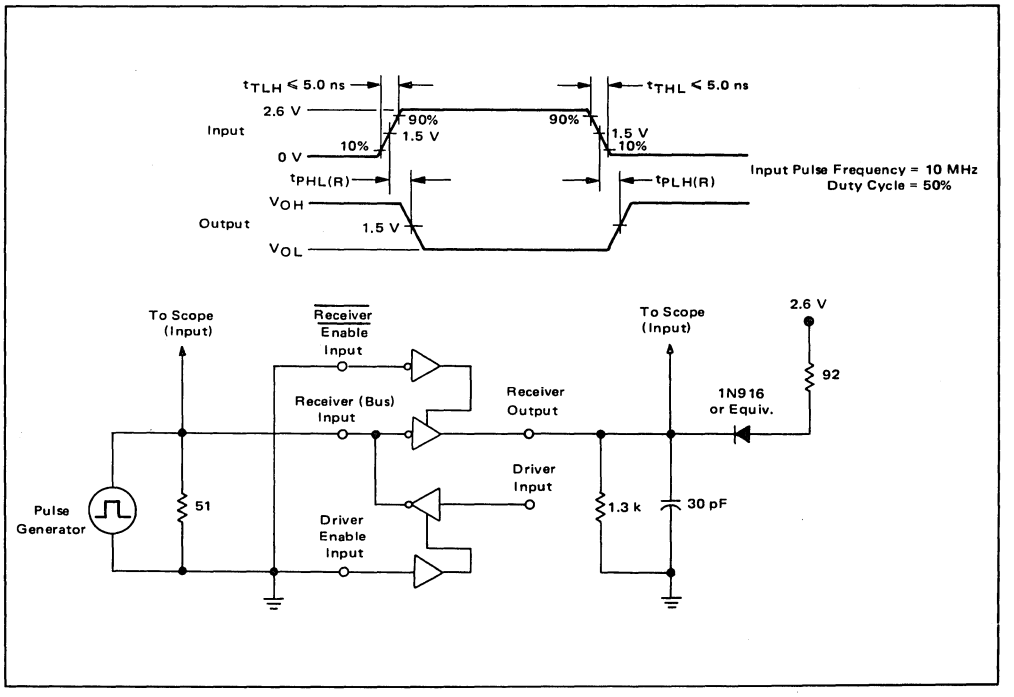


FIGURE 2 – TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY TIME FROM DRIVER INPUT TO BUS (DRIVER) OUTPUT, $t_{PLH(D)}$ AND $t_{PHL(D)}$

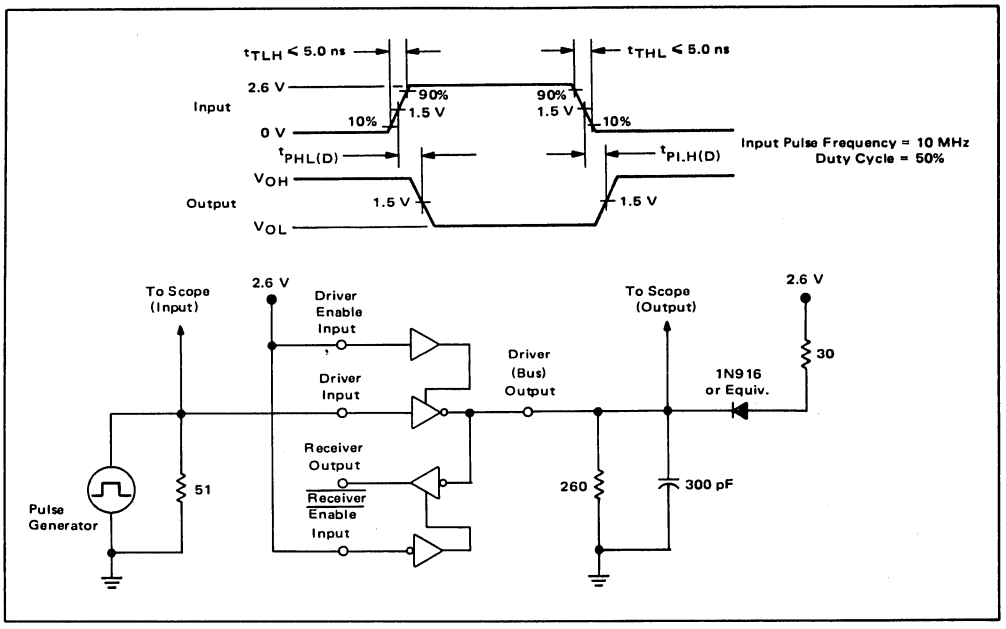


FIGURE 3 – TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY TIME FROM RECEIVER ENABLE INPUT TO RECEIVER OUTPUT, $t_{PLZ(RE)}$ AND $t_{PZL(RE)}$

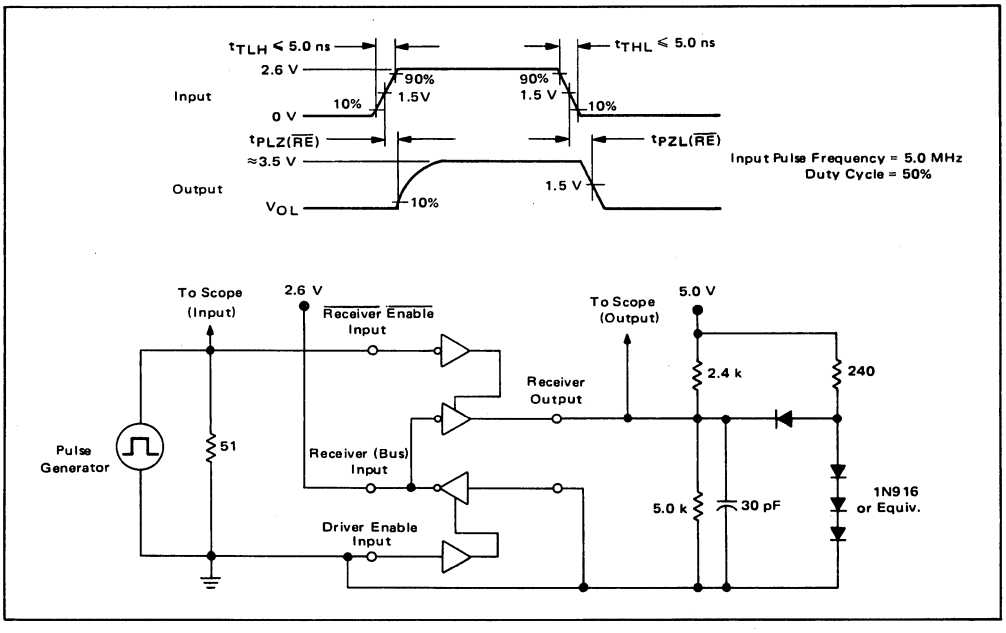


FIGURE 4 – TEST CIRCUIT AND WAVEFORMS FOR PROPAGATION DELAY TIMES FROM DRIVER ENABLE INPUT TO DRIVER (BUS) OUTPUT, $t_{PLZ(DE)}$ AND $t_{PZL(DE)}$

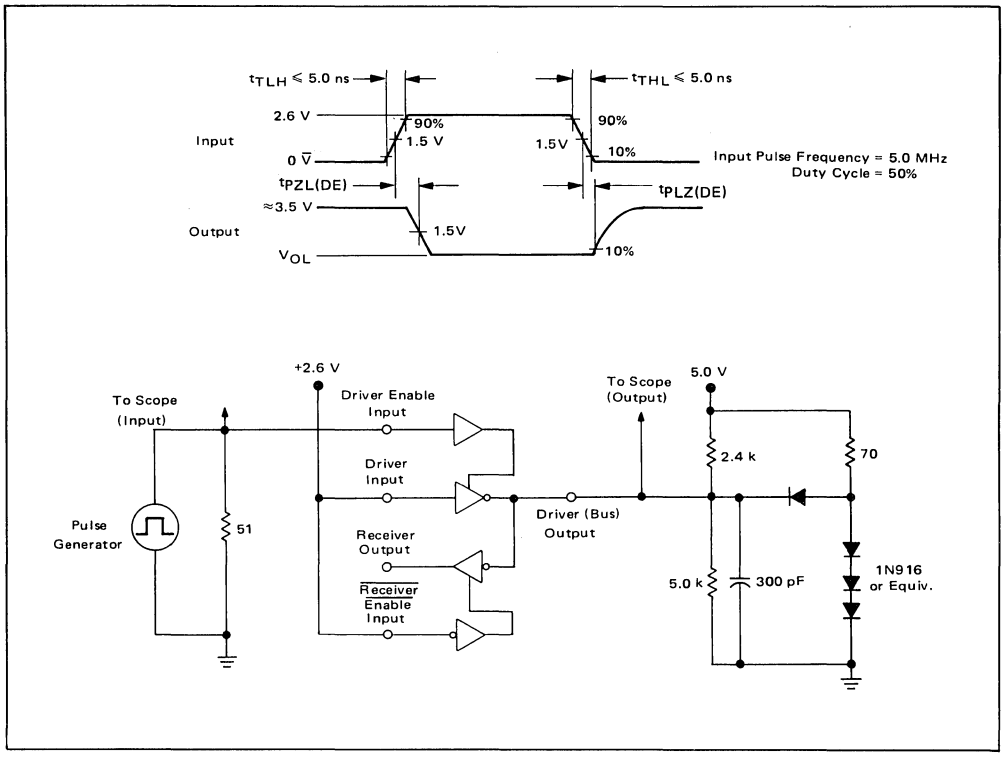
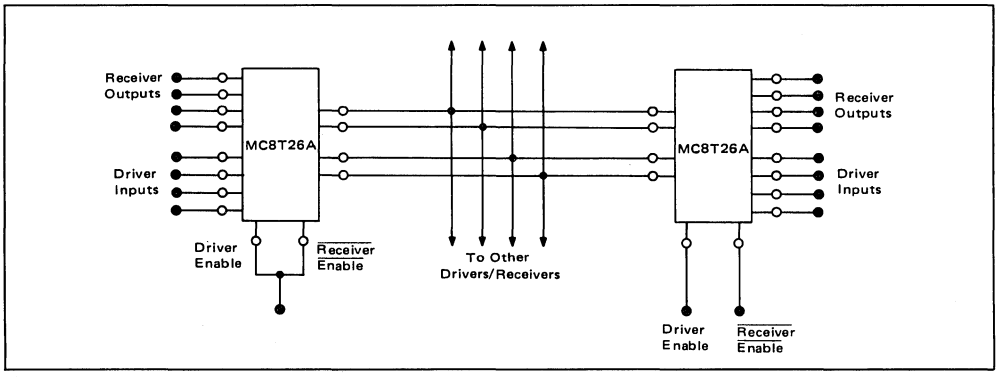


FIGURE 5 – BIDIRECTIONAL BUS APPLICATIONS



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC8T97 (MC6887)
MC8T98 (MC6888)

HEX THREE-STATE BUFFER INVERTERS

HEX THREE-STATE BUFFER/INVERTERS

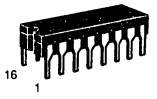
MONOLITH SCHOTTSKY INTEGRATED CIRCUITS

This series of devices combines three features usually found desirable in bus-oriented systems: 1) High impedance logic inputs insure that these devices do not seriously load the bus; 2) Three-state logic configuration allows buffers not being utilized to be effectively removed from the bus; 3) Schottky technology allows high-speed operation.

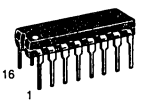
The noninverting MC8T97/MC6887 and inverting MC&t98/MC6888 provide two Enable inputs — one controlling four buffers and the other controlling the remaining two buffers.

The units are well-suited for Address buffers on the MC6800 or similar microprocessor application.

- High Speed — 8.0 ns (Typ)
- Three-State Logic Configuration
- Single +5 V Power Supply Requirement
- Compatible with 74LS Logic or MC6800 Microprocessor Systems
- High Impedance PNP Inputs Assure Minimal Loading of the Bus

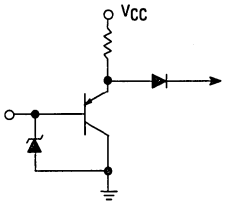


L SUFFIX
CERAMIC PACKAGE
CASE 620

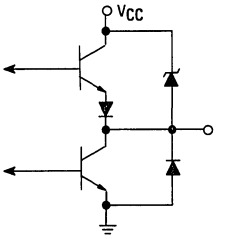


P SUFFIX
PLASTIC PACKAGE
CASE 648

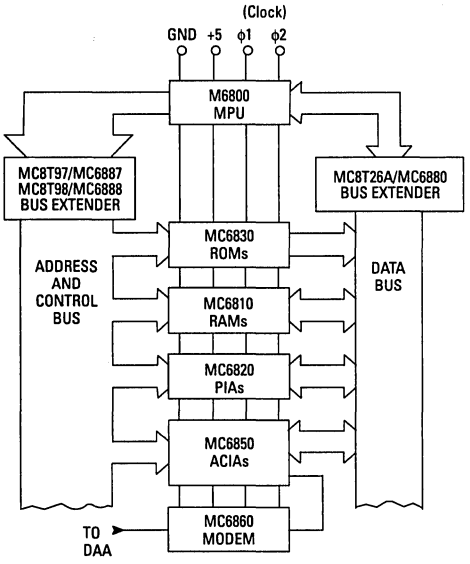
INPUT EQUIVALENT CIRCUIT



OUTPUT EQUIVALENT CIRCUIT



MICROPROCESSOR BUS EXTENDER APPLICATION



ORDERING INFORMATION
(Temperature Range = 0 to + 75°C)

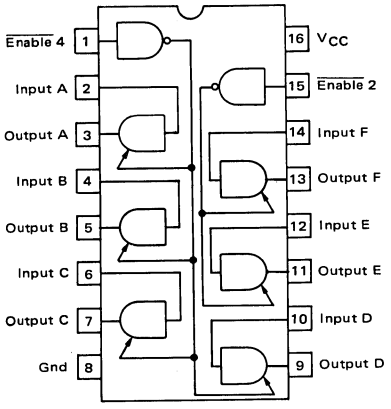
Device	Alternate	Package
MC8T97L	MC6887L	Ceramic DIP
MC8T98L	MC6888L	Ceramic DIP
MC8T97P	MC6887P	Plastic DIP
MC8T98P	MC6888P	Plastic DIP

7

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	8.0	Vdc
Input Voltage	V_I	5.5	Vdc
Operating Ambient Temperature Range	T_A	0 to +75	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Operating Junction Temperature Plastic Package Ceramic Package	T_J	 150 175	°C

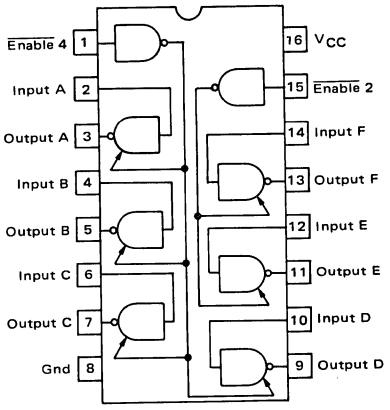
MC8T97/MC6887



Enable	Input	Output
L	L	L
L	H	H
H	X	Z

L = Low Logic State
H = High Logic State
Z = Third (High Impedance) State
X = Irrelevant

MC8T98/MC6888



Enable	Input	Output
L	L	H
L	H	L
H	X	Z

7

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, $0°C \le T_A \le 75°C$ and $4.75\ V \le V_{CC} \le 5.25\ V$)

Characteristics	Symbol	Min	Typ	Max	Unit
Input Voltage High Logic State (V_{CC} = 4.75 V, T_A = 25°C) Low Logic State (V_{CC} = 4.75 V, T_A = 25°C)	 V_{IH} V_{IL}	 2.0 —	 — —	 — 0.8	V
Input Current — High Logic State (V_{CC} = 5.25 V, V_{IH} = 2.4 V) Low Logic State (V_{CC} = 5.25 V, V_{IL} = 0.5 V, $V_{IL(\overline{E})}$ = 0.5 V) High Impedance State (V_{CC} = 5.25 V, V_{IL} = 0.5 V, $V_{IH(\overline{E})}$ = 2.0 V)	 I_{IH} I_{IL} $I_{IH(\overline{E})}$	 — — —	 — — —	 40 –400 –40	µA
Output Voltage High Logic State (V_{CC} = 4.75 V, I_{OH} = –5.2 mA) Low Logic State (I_{OL} = 48 mA)	 V_{OH} V_{OL}	 2.4 —	 — —	 — 0.5	V
Output Voltage — High Impedance State (V_{CC} = 5.25 V, V_{OH} = 2.4 V) (V_{CC} = 5.25 V, V_{OL} = 0.5 V)	I_{OZ}	 — —	 — —	 40 –40	µA
Output Short Circuit Current (V_{CC} = 5.25 V, V_O = 0, only one output can be shorted at a time)	I_{OS}	 –40	 –80	 –115	mA
Power Supply Current (V_{CC} = 5.25 V) MC8T97, MC6887 MC8T98, MC6888	I_{CC}	 — —	 65 59	 98 89	mA
Input Clamp Voltage (V_{CC} = 4.75 V, I_{IC} = –12 mA)	V_{IC}	 —	 —	 –1.5	V
Input Voltage (I_I = 1.0 mA)	V_I	 5.5	 —	 —	V
Output V_{CC} Clamp Voltage (V_{CC} = 0, I_{OC} = 12 mA)	V_{OC}	 —	 —	 1.5	V
Output Gnd Clamp Voltage (V_{CC} = 0, I_{OC} = 12 mA)	V_{OC}	 —	 —	 –1.5	

SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	MC8T97 MC6887 Min	MC8T97 MC6887 Typ	MC8T97 MC6887 Max	MC8T98 MC6888 Min	MC8T98 MC6888 Typ	MC8T98 MC6888 Max	Unit
Propagation Delay Time — High-to-Low State (C_L = 50 pF) (C_L = 250 pF) (C_L = 375 pF) (C_L = 500 pF)	t_{PHL}	 3.0 — — —	 — 16 20 23	 12 — — —	 4.0 — — —	 — 15 18 22	 11 — — —	ns
Propagation Delay Time — Low-to-High State (C_L = 50 pF) (C_L = 250 pF) (C_L = 375 pF) (C_L = 500 pF)	t_{PLH}	 3.0 — — —	 — 25 33 42	 13 — — —	 3.0 — — —	 — 22 28 35	 10 — — —	ns
Transition Time — High-to-Low State (C_L = 250 pF) (C_L = 375 pF) (C_L = 500 pF)	t_{THL}	 — — —	 10 11 14	 — — —	 — — —	 10 13 15	 — — —	ns
Transition Time — Low-to-High State (C_L = 250 pF) (C_L = 375 pF) (C_L = 500 pF)	t_{TLH}	 — — —	 32 42 60	 — — —	 — — —	 28 38 53	 — — —	ns
Propagation Delay Time — High State-to-Third State (C_L = 5.0 pF)	$t_{PHZ(\overline{E})}$	—	—	10	—	—	10	ns
Propagation Delay Time — Low State-to-Third State (C_L = 5.0 pF)	$t_{PLZ(\overline{E})}$	—	—	12	—	—	16	
Propagation Delay Time — Third State-to-High State (C_L = 50 pF)	$t_{PZH(\overline{E})}$	—	—	25	—	—	22	ns
Propagation Delay Time — Third State-to-Low State (C_L = 50 pF)	$t_{PZL(\overline{E})}$	—	—	25	—	—	24	

7

FIGURE 1 – TEST CIRCUIT FOR SWITCHING CHARACTERISTICS

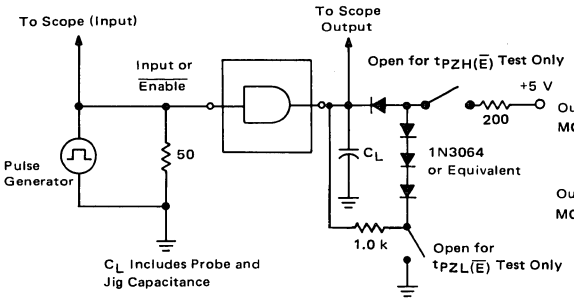


FIGURE 2 – WAVEFORMS FOR PROPAGATION DELAY TIMES INPUT TO OUTPUT

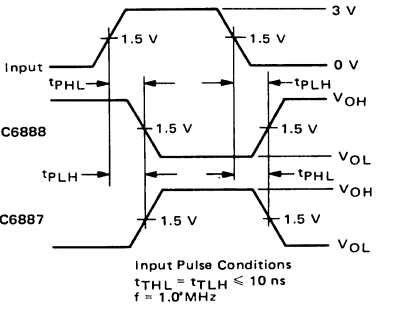
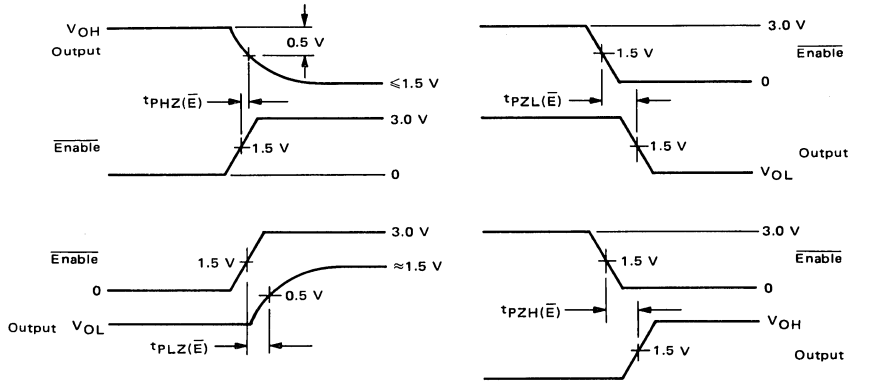


FIGURE 3 – WAVEFORMS FOR PROPAGATION DELAY TIMES – $\overline{\text{ENABLE}}$ TO OUTPUT



H = High-Logic State, L = Low-Logic State, Z = High Impedance State

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC1411,B
MC1412,B
MC1413,B
MC1416,B

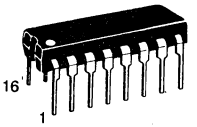
PERIPHERAL DRIVER ARRAYS

SILICON MONOLITHIC INTEGRATED CIRCUITS

HIGH VOLTAGE, HIGH CURRENT DARLINGTON TRANSISTOR ARRAYS

The seven NPN Darlington connected transistors in these arrays are well suited for driving lamps, relays, or printer hammers in a variety of industrial and consumer applications. Their high breakdown voltage and internal suppression diodes insure freedom from problems associated with inductive loads. Peak inrush currents to 600 mA permit them to drive incandescent lamps.

The MC1411,B device is a general purpose array for use with DTL, TTL, PMOS, or CMOS Logic. The MC1412,B contains a zener diode and resistor in series with the input to limit input current for use with 14 to 25 Volt PMOS Logic. The MC1413,B with a 2.7 kΩ series input resistor is well suited for systems utilizing a 5 Volt TTL or CMOS Logic. The MC1416,B uses a series 10.5 kΩ resistor and is useful in 8 to 18 Volt MOS systems.



P SUFFIX
PLASTIC PACKAGE
CASE 648

D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO-16)

7

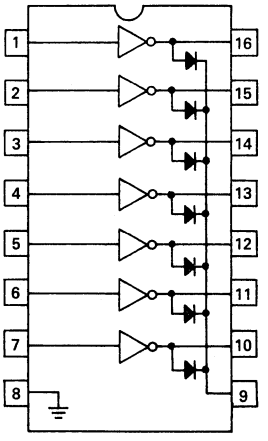
MAXIMUM RATINGS (T_A = 25°C and rating apply to any one device in the package unless otherwise noted.)

Rating	Symbol	Value	Unit
Output Voltage	V_O	50	V
Input Voltage (Except MC1411)	V_I	30	V
Collector Current — Continuous	I_C	500	mA
Base Current — Continuous	I_B	25	mA
Operating Ambient Temperature Range MC1411-16 MC1411B-16B	T_A	 −20 to +85 −40 to +85	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C
Junction Temperature	T_J	150	°C
Thermal Resistance — Junction-to-Ambient Case 648, P Suffix Case 751B, D Suffix	θ_{JA}	 67 100	°C/W

ORDERING INFORMATION

Plastic DIP	SOIC	Ambient Temperature Range
MC1411P (ULN2001A) MC1412P (ULN2002A) MC1413P (ULN2003A) MC1416P (ULN2004A)	MC1411D MC1412D MC1413D MC1416D	−20° to +85°C
MC1411BP MC1412BP MC1413BP MC1416BP	MC1411BD MC1412BD MC1413BD MC1416BD	−40° to +85°C

PIN CONNECTIONS



ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Output Leakage Current		I_{CEX}				μA
(V_O = 50 V, T_A = +85°C)	All Types		—	—	100	
(V_O = 50 V, T_A = +25°C)	All Types		—	—	50	
(V_O = 50 V, T_A = +85°C, V_I = 6.0 V)	MC1412,B		—	—	500	
(V_O = 50 V, T_A = +85°C, V_I = 1.0 V)	MC1416,B		—	—	500	
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$				V
(I_C = 350 mA, I_B = 500 μA)	All Types		—	1.1	1.6	
(I_C = 200 mA, I_B = 350 μA)	All Types		—	0.95	1.3	
(I_C = 100 mA, I_B = 250 μA)	All Types		—	0.85	1.1	
Input Current — On Condition		$I_{I(on)}$				mA
(V_I = 17 V)	MC1412,B		—	0.85	1.3	
(V_I = 3.85 V)	MC1413,B		—	0.93	1.35	
(V_I = 5.0 V)	MC1416,B		—	0.35	0.5	
(V_I = 12 V)	MC1416,B		—	1.0	1.45	
Input Voltage — On Condition		$V_{I(on)}$				V
(V_{CE} = 2.0 V, I_C = 300 mA)	MC1412,B		—	—	13	
(V_{CE} = 2.0 V, I_C = 200 mA)	MC1413,B		—	—	2.4	
(V_{CE} = 2.0 V, I_C = 250 mA)	MC1413,B		—	—	2.7	
(V_{CE} = 2.0 V, I_C = 300 mA)	MC1413,B		—	—	3.0	
(V_{CE} = 2.0 V, I_C = 125 mA)	MC1416,B		—	—	5.0	
(V_{CE} = 2.0 V, I_C = 200 mA)	MC1416,B		—	—	6.0	
(V_{CE} = 2.0 V, I_C = 275 mA)	MC1416,B		—	—	7.0	
(V_{CE} = 2.0 V, I_C = 350 mA)	MC1416,B		—	—	8.0	
Input Current — Off Condition (I_C = 500 μA, T_A = +85°C)	All Types	$I_{I(off)}$	50	100	—	μA
DC Current Gain (V_{CE} = 2.0 V, I_C = 350 mA)	MC1411,B	h_{FE}	1000	—	—	—
Input Capacitance		C_I	—	15	30	pF
Turn-On Delay Time (50% E_I to 50% E_O)		t_{on}	—	0.25	1.0	μs
Turn-Off Delay Time (50% E_I to 50% E_O)		t_{off}	—	0.25	1.0	μs
Clamp Diode Leakage Current	T_A = +25°C	I_R	—	—	50	μA
(V_R = 50 V)	T_A = +85°C		—	—	100	
Clamp Diode Forward Voltage (I_F = 350 mA)		V_F	—	1.5	2.0	V

7

TYPICAL PERFORMANCE CURVES — T_A = 25°C

FIGURE 1 — OUTPUT CURRENT versus INPUT VOLTAGE

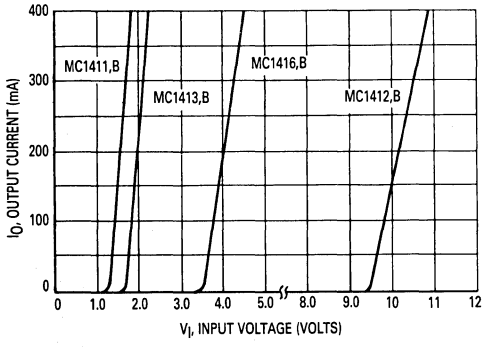
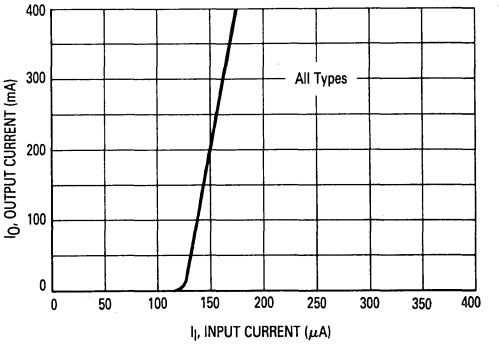


FIGURE 2 — OUTPUT CURRENT versus INPUT CURRENT



TYPICAL CHARACTERISTIC CURVES – T_A = 25°C (continued)

FIGURE 3 — TYPICAL OUTPUT CHARACTERISTICS

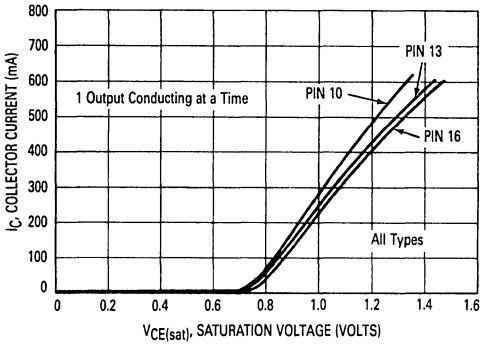


FIGURE 4 — INPUT CHARACTERISTICS — MC1412,B

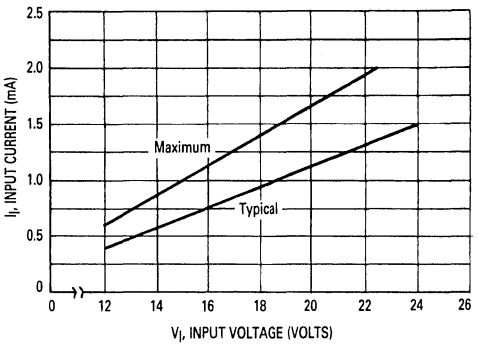


FIGURE 5 — INPUT CHARACTERISTICS — MC1413,B

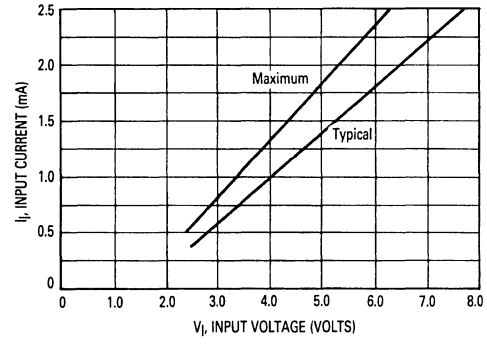


FIGURE 6 — INPUT CHARACTERISTICS — MC1416,B

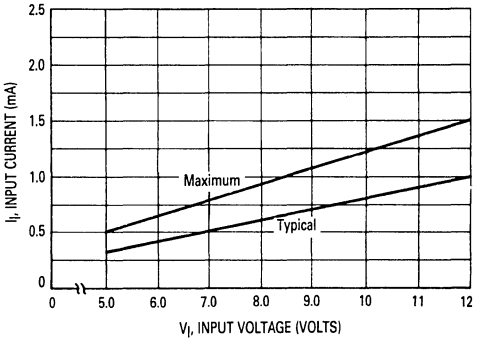


FIGURE 7 — MAXIMUM COLLECTOR CURRENT versus DUTY CYCLE (AND NUMBER OF DRIVERS IN USE)

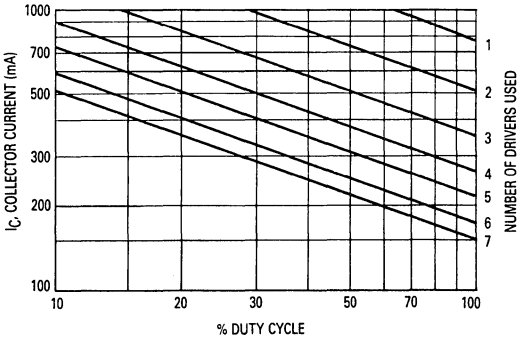
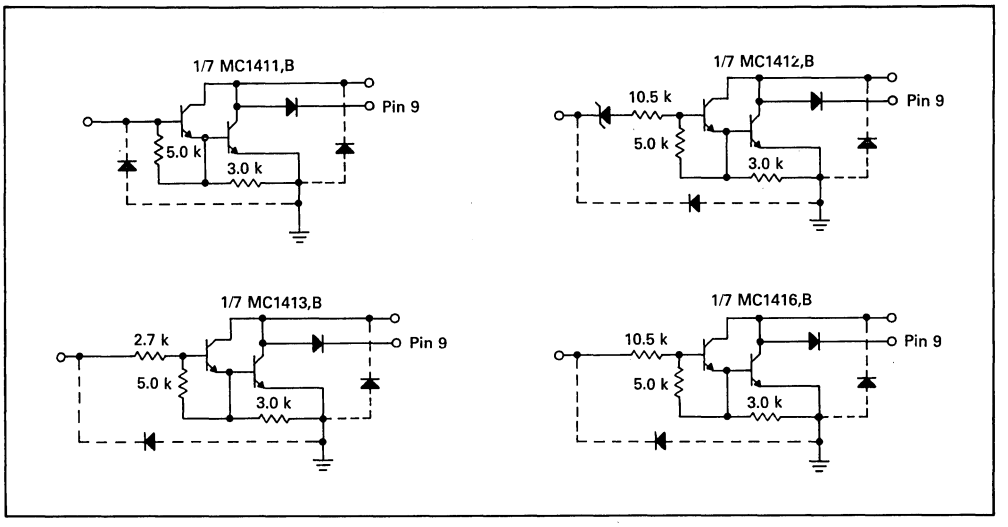


FIGURE 8 — REPRESENTATIVE CIRCUIT SCHEMATICS



7

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC1472

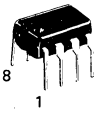
DUAL PERIPHERAL POSITIVE "NAND" DRIVER

SILICON MONOLITHIC
INTEGRATED CIRCUITS

DUAL PERIPHERAL-HIGH-VOLTAGE POSITIVE "NAND" DRIVER

The dual driver consists of a pair of PNP buffered AND gates connected to the bases of a pair of high voltage NPN transistors. They are similar to the MC75452 drivers but with the added advantages of: 1) 70 Volt capability 2) output suppression diodes and 3) PNP buffered inputs for MOS compatibility. These features make the MC1472 ideal for mating MOS logic or microprocessors to lamps, relays, printer hammers and incandescent displays.

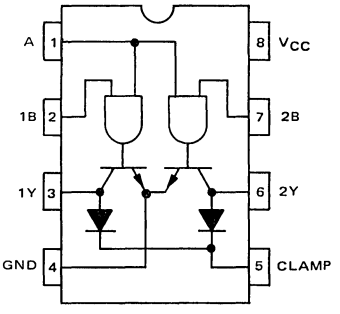
- 300 mA Output Capability (each transistor)
- 70 Vdc Breakdown Voltage
- Internal Output Clamp Diodes
- Low Input Loading for MOS Compatibility (PNP buffered)



P1 SUFFIX
PLASTIC PACKAGE
CASE 626

7

PIN CONNECTIONS



Positive Logic: Y=AB*

MAXIMUM RATINGS (T_A = 25°C)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	7.0	V
Input Voltage	V_{in}	5.5	V
Output Voltage	V_{out}	80	V
Clamp Voltage	V_C	80	V
Output Current (Continuous)	I_O	399	mA
Operating Junction Temperature	T_J	+ 150	°C
Storage Temperature Range	T_{stg}	− 65 to + 150	°C

RECOMMENDED OPERATING CONDITIONS

Rating	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	4.5	5.5	Volts
Operating Ambient Temperature	T_A	0	70	°C
Output Voltage	V_O	V_{CC}	70	Volts
Clamp Voltage	V_C	V_O	70	Volts

ORDERING INFORMATION

Device	Temperature Range	Package
MC1472P1	0 to + 70°C	Plastic DIP

TRUTH TABLE

A	B	Y
L	L	H ("OFF" STATE)
L	H	
H	L	
H	H	L ("ON" STATE)

H = Logic One
L = Logic Zero

ELECTRICAL CHARACTERISTICS (Unless otherwise noted min/max limits apply across the 0°C to 70°C temperature range with 4.5 V ≤ V_{CC} ≤ 5.5 V. All typical values are for T_A = 25°C, V_{CC} = 5.0 Volts.)

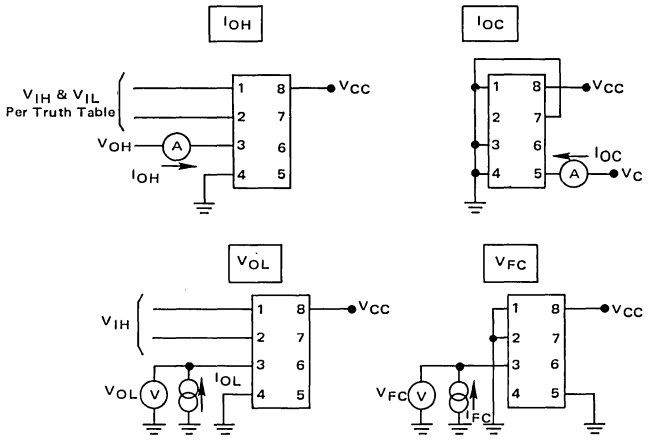
Characteristic	Symbol	Min	Typ	Max	Unit
Input Voltage — High Logic State	V_{IH}	2.0	—	5.5	Vdc
Input Voltage — Low Logic State	V_{IL}	0	—	0.8	Vdc
Input Current — Low Logic State (V_{IL} = 0.4 V) A Input B Input	I_{IL}	 —	 —	 −0.3 −0.15	mA
Input Current — High Logic State (V_{IH} = 2.4 V) A Input B Input (V_{IH} = 5.5 V) A Input B Input	I_{IH}	 — — — —	 — — — —	 40 20 200 100	μA
Input Clamp Voltage (I_{CC} = −12 mA)	V_{IK}	—	—	−1.5	V
Output Leakage Current — High Logic State (V_O = 70 V, See Test Figure)	I_{OH}		—	100	μA
Output Voltage — Low Logic State (I_{OL} = 100 mA) (I_{OL} = 300 mA)	V_{OL}	 — —	 — —	 0.4 0.7	V
Output Clamp Diode Leakage Current (V_C = 70 V, See Test Figure)	I_{OC}	—	—	100	V
Output Clamp Forward Voltage (I_{FC} = 300 mA, See Test Figure)	V_{FC}	—	—	1.7	V
Power Supply Current (All Inputs at V_{IH}) (All Inputs at V_{IL})	I_{CC}	 — —	 — —	 70 15	mA

NOTE: All currents into device pins are shown as positive, out of device pins as negative. All voltages referenced to ground unless otherwise noted.

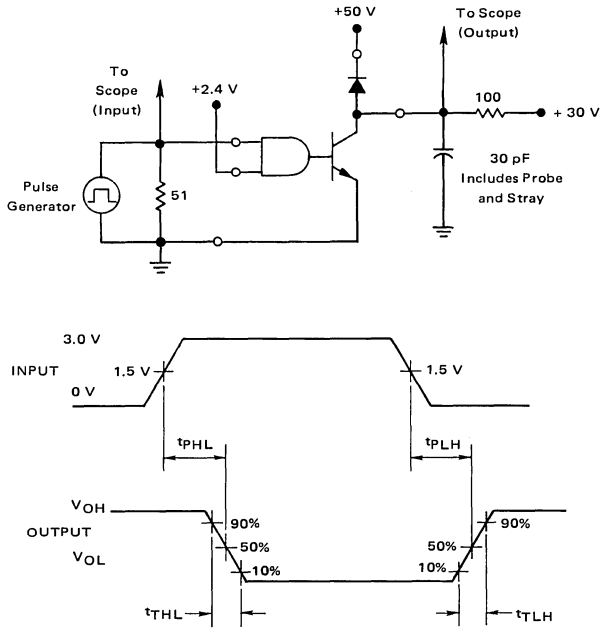
SWITCHING CHARACTERISTICS V_{CC} = 5.0V, T_A = 25°C

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Time Output High to Low Output Low to High	 t_{PHL} t_{PLH}	 – –	 – –	 1.0 0.75	μs
Output Transition Time Output High to Low Output Low to High	 t_{THL} t_{TLH}	 – –	 – –	 0.1 0.1	μs

TEST CIRCUITS



SWITCHING TEST CIRCUIT AND WAVEFORM



7

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC1488

QUAD LINE DRIVER

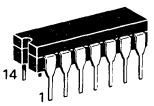
The MC1488 is a monolithic quad line driver designed to interface data terminal equipment with data communications equipment in conformance with the specifications of EIA Standard No. EIA-232D.

Features:

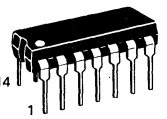
- Current Limited Output
  ±10 mA typ
- Power-Off Source Impedance
  300 Ohms min
- Simple Slew Rate Control with External Capacitor
- Flexible Operating Supply Range
- Compatible with All Motorola MDTL and MTTL Logic Families

QUAD MDTL LINE DRIVER
EIA-232D

SILICON MONOLITHIC INTEGRATED CIRCUIT



L SUFFIX
CERAMIC PACKAGE
CASE 632



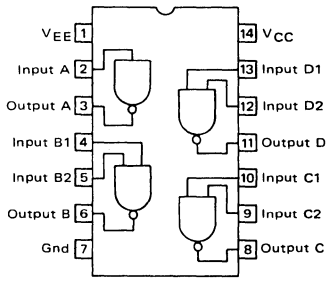
P SUFFIX
PLASTIC PACKAGE
CASE 646

D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO-14)

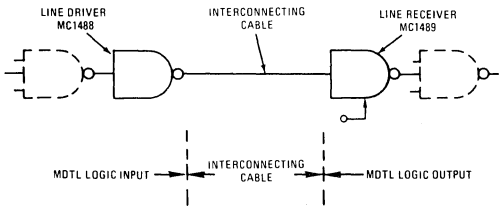
ORDERING INFORMATION

Device	Temperature Range	Package
MC1488P	0 to + 75°C	Plastic
MC1488D		SO-14
MC1488L		Ceramic

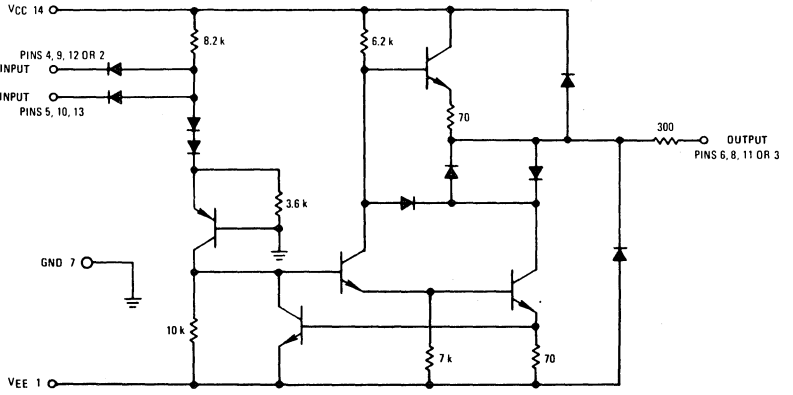
PIN CONNECTIONS



TYPICAL APPLICATION



CIRCUIT SCHEMATIC
(1/4 OF CIRCUIT SHOWN)



7

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+15 −15	Vdc
Input Voltage Range	V_{IR}	$-15 \leq V_{IR} \leq 7.0$	Vdc
Output Signal Voltage	V_O	±15	Vdc
Power Derating (Package Limitation, Ceramic and Plastic Dual-In-Line Package) Derate above T_A = +25°C	P_D $1/R_{\theta JA}$	1000 6.7	mW mW/°C
Operating Ambient Temperature Range	T_A	0 to +75	°C
Storage Temperature Range	T_{stg}	−65 to +175	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +9.0 ±1% Vdc, V_{EE} = −9.0 ±1% Vdc, T_A = 0 to 75°C unless otherwise noted.)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Input Current — Low Logic State (V_{IL} = 0)	1	I_{IL}	—	1.0	1.6	mA
Input Current — High Logic State (V_{IH} = 5.0 V)	1	I_{IH}	—	—	10	μA
Output Voltage — High Logic State (V_{IL} = 0.8 Vdc, R_L = 3.0 kΩ, V_{CC} = +9.0 Vdc, V_{EE} = −9.0 Vdc) (V_{IL} = 0.8 Vdc, R_L = 3.0 kΩ, V_{CC} = +13.2 Vdc, V_{EE} = −13.2 Vdc)	2	V_{OH}	 +6.0 +9.0	 +7.0 +10.5	 — —	Vdc
Output Voltage — Low Logic State (V_{IH} = 1.9 Vdc, R_L = 3.0 kΩ, V_{CC} = +9.0 Vdc, V_{EE} = −9.0 Vdc) (V_{IH} = 1.9 Vdc, R_L = 3.0 kΩ, V_{CC} = +13.2 Vdc, V_{EE} = −13.2 Vdc)	2	V_{OL}	 −6.0 −9.0	 −7.0 −10.5	 — —	Vdc
Positive Output Short-Circuit Current, Note 1	3	I_{OS+}	+6.0	+10	+12	mA
Negative Output Short-Circuit Current, Note 1	3	I_{OS-}	−6.0	−10	−12	mA
Output Resistance (V_{CC} = V_{EE} = 0, $\|V_O\|$ = ±2.0 V)	4	r_o	300	—	—	Ohms
Positive Supply Current (R_l = ∞) (V_{IH} = 1.9 Vdc, V_{CC} = +9.0 Vdc) (V_{IL} = 0.8 Vdc, V_{CC} = +9.0 Vdc) (V_{IH} = 1.9 Vdc, V_{CC} = +12 Vdc) (V_{IL} = 0.8 Vdc, V_{CC} = +12 Vdc) (V_{IH} = 1.9 Vdc, V_{CC} = +15 Vdc) (V_{IL} = 0.8 Vdc, V_{CC} = +15 Vdc)	5	I_{CC}	 — — — — — —	 +15 +4.5 +19 +5.5 — —	 +20 +6.0 +25 +7.0 +34 +12	mA
Negative Supply Current (R_L = ∞) (V_{IH} = 1.9 Vdc, V_{EE} = −9.0 Vdc) (V_{IL} = 0.8 Vdc, V_{EE} = −9.0 Vdc) (V_{IH} = 1.9 Vdc, V_{EE} = −12 Vdc) (V_{IL} = 0.8 Vdc, V_{EE} = −12 Vdc) (V_{IH} = 1.9 Vdc, V_{EE} = −15 Vdc) (V_{IL} = 0.8 Vdc, V_{EE} = −15 Vdc)	5	I_{EE}	 — — — — — —	 −13 — −18 — — —	 −17 −500 −23 −500 −34 −2.5	mA μA mA μA mA mA
Power Consumption (V_{CC} = 9.0 Vdc, V_{EE} = −9.0 Vdc) (V_{CC} = 12 Vdc, V_{EE} = −12 Vdc)		P_C	 — —	 — —	 333 576	mW

SWITCHING CHARACTERISTICS (V_{CC} = +9.0 ±1% Vdc, V_{EE} = −9.0 ±1% Vdc, T_A = +25°C.)

Propagation Delay Time	(z_l = 3.0 k and 15 pF)	6	t_{PLH}	—	275	350	ns
Fall Time	(z_l = 3.0 k and 15 pF)	6	t_{THL}	—	45	75	ns
Propagation Delay Time	(z_l = 3.0 k and 15 pF)	6	t_{PHL}	—	110	175	ns
Rise Time	(z_l = 3.0 k and 15 pF)	6	t_{TLH}	—	55	100	ns

Note 1. Maximum Package Power Dissipation may be exceeded if all outputs are shorted simultaneously.

CHARACTERISTIC DEFINITIONS

FIGURE 1 – INPUT CURRENT

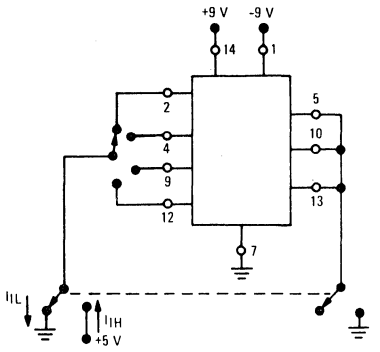


FIGURE 2 – OUTPUT VOLTAGE

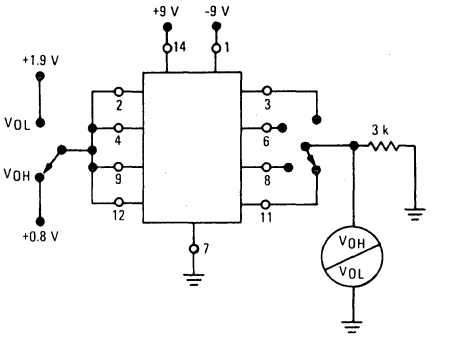


FIGURE 3 – OUTPUT SHORT-CIRCUIT CURRENT

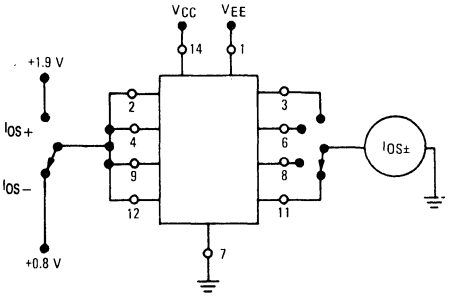


FIGURE 4 – OUTPUT RESISTANCE (POWER-OFF)

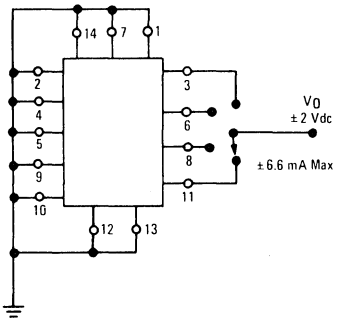


FIGURE 5 – POWER-SUPPLY CURRENTS

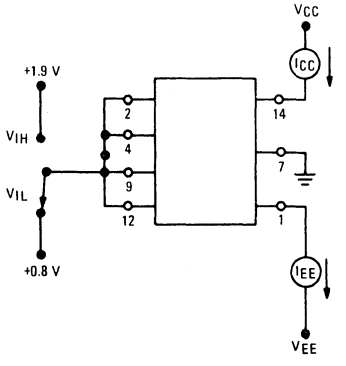
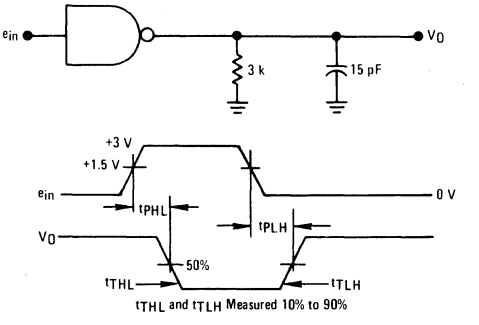


FIGURE 6 – SWITCHING RESPONSE



TYPICAL CHARACTERISTICS

(T_A = +25°C unless otherwise noted.)

FIGURE 7 — TRANSFER CHARACTERISTICS versus POWER-SUPPLY VOLTAGE

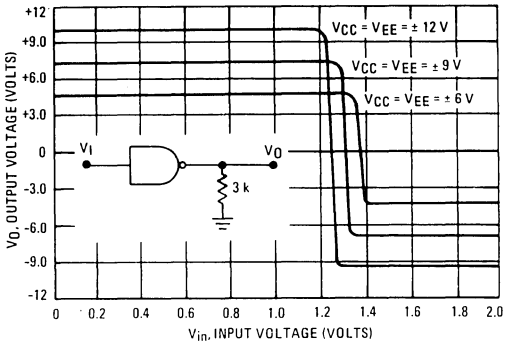


FIGURE 8 — SHORT-CIRCUIT OUTPUT CURRENT versus TEMPERATURE

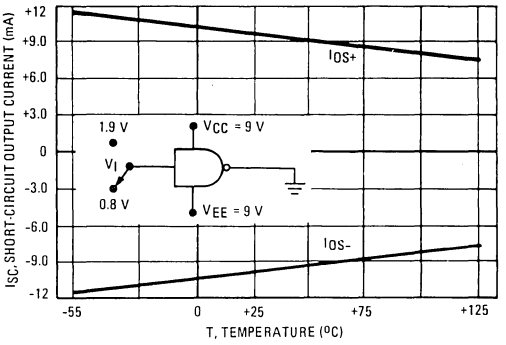


FIGURE 9 — OUTPUT SLEW RATE versus LOAD CAPACITANCE

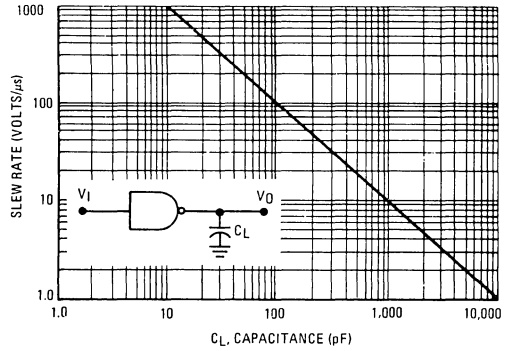


FIGURE 10 — OUTPUT VOLTAGE AND CURRENT-LIMITING CHARACTERISTICS

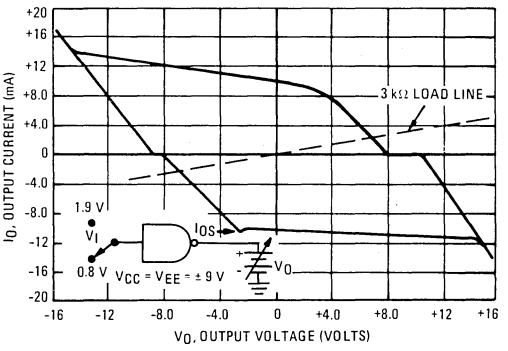
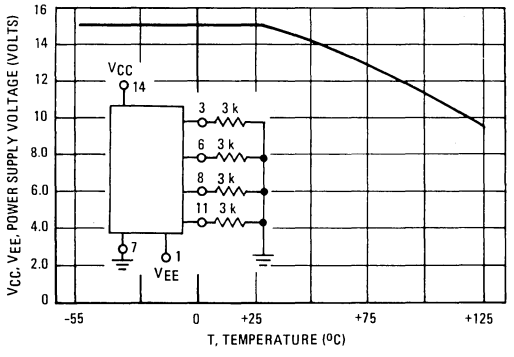


FIGURE 11 — MAXIMUM OPERATING TEMPERATURE versus POWER-SUPPLY VOLTAGE



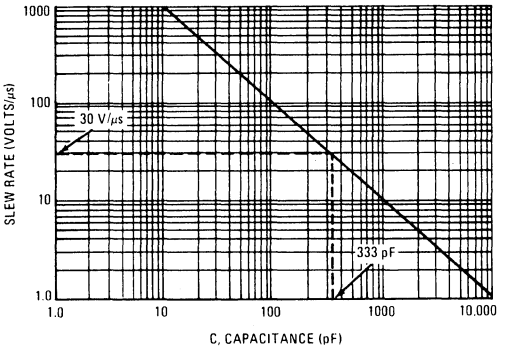
APPLICATIONS INFORMATION

The Electronic Industries Association EIA-232D specification detail the requirements for the interface between data processing equipment and data communications equipment. This standard specifies not only the number and type of interface leads, but also the voltage levels to be used. The MC1488 quad driver and its companion circuit, the MC1489 quad receiver, provide a complete interface system between DTL or TTL logic levels and the EIA-232D defined levels. The EIA-232D requirements as applied to drivers are discussed herein.

The required driver voltages are defined as between 5 and 15-volts in magnitude and are positive for a Logic "0" and negative for a Logic "1." These voltages are so defined when the drivers are terminated with a 3000 to 7000-ohm resistor. The MC1488 meets this voltage requirement by converting a DTL/TTL logic level into EIA-232D levels with one stage of inversion.

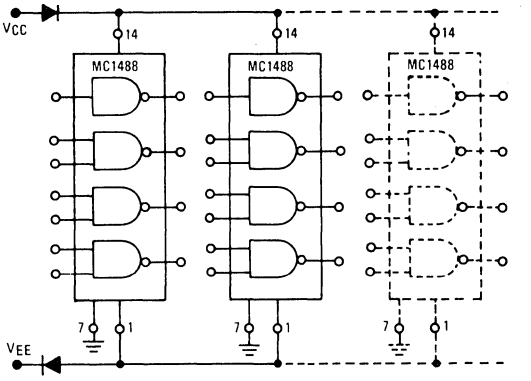
The EIA-232D specification further requires that during transitions, the driver output slew rate must not exceed 30 volts per microsecond. The inherent slew rate of the MC1488 is much too fast for this requirement. The current limited output of the device can be used to control this slew rate by connecting a capacitor to each driver output. The required capacitor can be easily determined by using the relationship $C = I_{OS} \times \Delta T/\Delta V$ from which Figure 12 is derived. Accordingly, a 330 pF capacitor on each output will guarantee a worst case slew rate of 30 volts per microsecond.

FIGURE 12 – SLEW RATE versus CAPACITANCE FOR I_{SC} = 10 mA



The interface driver is also required to withstand an accidental short to any other conductor in an interconnecting cable. The worst possible signal on any conductor would be another driver using a plus or minus 15 volt, 500 mA source. The MC1488 is designed to indefinitely withstand such a short to all four outputs in a package as long as the power-supply voltages are greater than 9.0 volts (i.e., $V_{CC} \geq 9.0$ V; $V_{EE} \leq -9.0$ V). In some power-supply designs, a loss of system power causes a low impedance on the power-supply outputs. When this occurs, a low impedance to ground would exist at the power inputs to the MC1488 effectively shorting the 300 ohm output resistors to ground. If all four outputs were then shorted to plus or minus 15 volts, the power dissipation in these resistors would be excessive. Therefore, if the system is designed to permit low impedances to ground at the power-supplies of the drivers, a diode should be placed in each power-supply lead to prevent overheating in this fault condition. These two diodes, as shown in Figure 13, could be used to decouple all the driver packages in a system. (These same diodes will allow the MC1488 to withstand momentary shorts to the ±25 volt limits specified in the earlier Standard EIA-232B.) The addition of the diodes also permits the MC1488 to withstand faults with power-supplies of less than the 9.0 volts stated above.

FIGURE 13 – POWER-SUPPLY PROTECTION TO MEET POWER-OFF FAULT CONDITIONS



The maximum short-circuit current allowable under fault conditions is more than guaranteed by the previously mentioned 10 mA output current limiting.

Other Applications

The MC1488 is an extremely versatile line driver with a myriad of possible applications. Several features of the drivers enhance this versatility:

1. Output Current Limiting — this enables the circuit designer to define the output voltage levels independent of power-supplies and can be accomplished by diode clamping of the output pins. Figure 14 shows the MC1488 used as a DTL to MOS translator where the high level voltage output is clamped one diode above ground. The resistor divider shown is used to reduce the output voltage below the 300 mV above ground MOS input level limit.

2. Power Supply Range — as can be seen from the schematic drawing of the drivers, the positive and negative driving elements of the device are essentially independent and do not require matching power-supplies. In fact, the positive supply can vary from a minimum seven volts (required for driving the negative pulldown section) to the maximum specified 15 volts. The negative supply can vary from approximately −2.5 volts to the minimum specified −15 volts. The MC1488 will drive the output to within 2 volts of the positive or negative supplies as long as the current output limits are not exceeded. The combination of the current-limiting and supply-voltage features allow a wide combination of possible outputs within the same quad package. Thus if only a portion of the four drivers are used for driving EIA-232D lines, the remainder could be used for DTL to MOS or even DTL to DTL translation. Figure 15 shows one such combination.

FIGURE 14 – MDTL/MTTL-TO-MOS TRANSLATOR

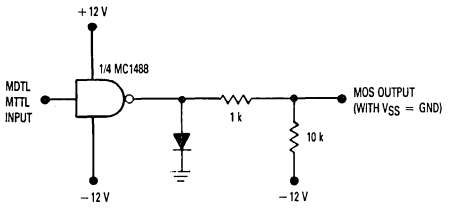
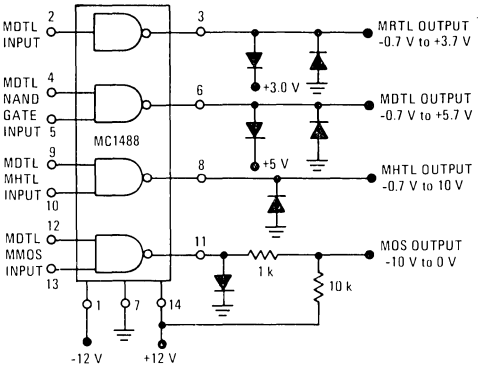


FIGURE 15 – LOGIC TRANSLATOR APPLICATIONS



7

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC1489
MC1489A

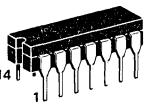
QUAD LINE RECEIVERS

QUAD MDTL LINE RECEIVERS EIA-232D

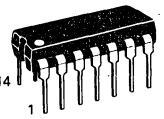
SILICON MONOLITHIC INTEGRATED CIRCUIT

The MC1489 monolithic quad line receivers are designed to interface data terminal equipment with data communications equipment in conformance with the specifications of EIA Standard No. EIA-232D.

- Input Resistance – 3.0 k to 7.0 kilohms
- Input Signal Range – ±30 Volts
- Input Threshold Hysteresis Built In
- Response Control
  a) Logic Threshold Shifting
  b) Input Noise Filtering



L SUFFIX
CERAMIC PACKAGE
CASE 632



P SUFFIX
PLASTIC PACKAGE
CASE 646

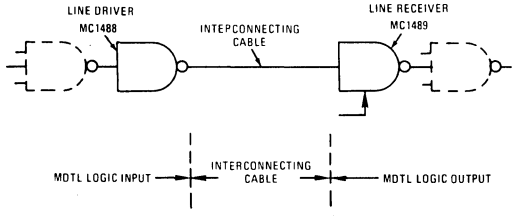
D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO-14)

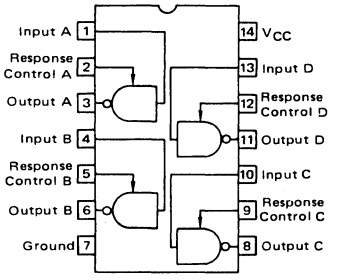
ORDERING INFORMATION

Device	Temperature Range	Package
MC1489P,AP	0 to + 75°C	Plastic
MC1489D,AD		SO-14
MC1489L,AL		Ceramic

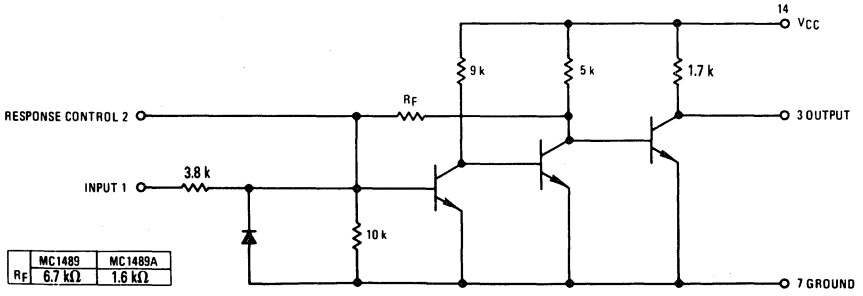
7

TYPICAL APPLICATION





EQUIVALENT CIRCUIT SCHEMATIC (1/4 OF CIRCUIT SHOWN)



	MC1489	MC1489A
RF	6.7 kΩ	1.6 kΩ

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	10	Vdc
Input Voltage Range	V_{IR}	±30	Vdc
Output Load Current	I_L	20	mA
Power Dissipation (Package Limitation, Ceramic and Plastic Dual In-Line Package) Derate above T_A = +25°C	P_D $1/\theta JA$	1000 6.7	mW mW/°C
Operating Ambient Temperature Range	T_A	0 to +75	°C
Storage Temperature Range	T_{stg}	−65 to +175	°C

ELECTRICAL CHARACTERISTICS (Response control pin is open.) (V_{CC} = +5.0 Vdc ±10%, T_A = 0 to +75°C unless otherwise noted)

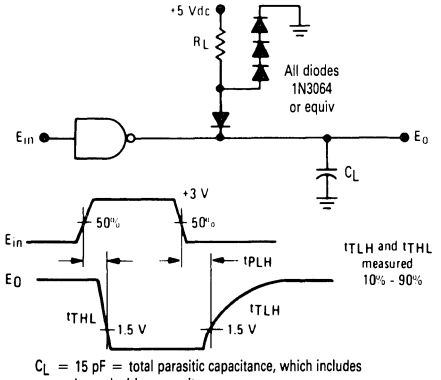
Characteristics		Symbol	Min	Typ	Max	Unit
Positive Input Current	(V_{IH} = +25 Vdc) (V_{IH} = +3.0 Vdc)	I_{IH}	3.6 0.43	— —	8.3 —	mA
Negative Input Current	(V_{IL} = −25 Vdc) (V_{IL} = −3.0 Vdc)	I_{IL}	−3.6 −0.43	— —	−8.3 —	mA
Input Turn-On Threshold Voltage (T_A = +25°C, V_{OL} ≤ 0.45 V)	MC1489 MC1489A	V_{IH}	1.0 1.75	— 1.95	1.5 2.25	Vdc
Input Turn-Off Threshold Voltage (T_A = +25°C, V_{OH} ≥ 2.5 V, I_L = −0.5 mA)	MC1489 MC1489A	V_{IL}	0.75 0.75	— 0.8	1.25 1.25	Vdc
Output Voltage High	(V_{IH} = 0.75 V, I_L = −0.5 mA) (Input Open Circuit, I_L = −0.5 mA)	V_{OH}	2.5 2.5	4.0 4.0	5.0 5.0	Vdc
Output Voltage Low	(V_{IL} = 3.0 V, I_L = 10 mA)	V_{OL}	—	0.2	0.45	Vdc
Output Short-Circuit Current		I_{OS}	—	−3.0	−4.0	mA
Power Supply Current (All Gates "on," I_{out} = 0 mA, V_{IH} = +5.0 Vdc)		I_{CC}	—	16	26	mA
Power Consumption	(V_{IH} = +5.0 Vdc)	P_C	—	80	130	mW

SWITCHING CHARACTERISTICS (V_{CC} = 5.0 Vdc ±1%, T_A = +25°C, See Figure 1.)

Propagation Delay Time	(R_L = 3.9 kΩ)	t_{PLH}	—	25	85	ns
Rise Time	(R_L = 3.9 kΩ)	t_{TLH}	—	120	175	ns
Propagation Delay Time	(R_L = 390 kΩ)	t_{PHL}	—	25	50	ns
Fall Time	(R_L = 390 kΩ)	t_{THL}	—	10	20	ns

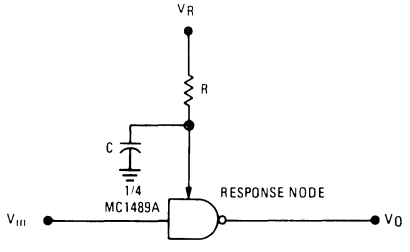
TEST CIRCUITS

FIGURE 1 — SWITCHING RESPONSE



C_L = 15 pF = total parasitic capacitance, which includes probe and wiring capacitances

FIGURE 2 — RESPONSE CONTROL NODE



C, capacitor is for noise filtering.
R, resistor is for threshold shifting.

TYPICAL CHARACTERISTICS

(V_{CC} = 5.0 Vdc, T_A = +25°C unless otherwise noted)

FIGURE 3 — INPUT CURRENT

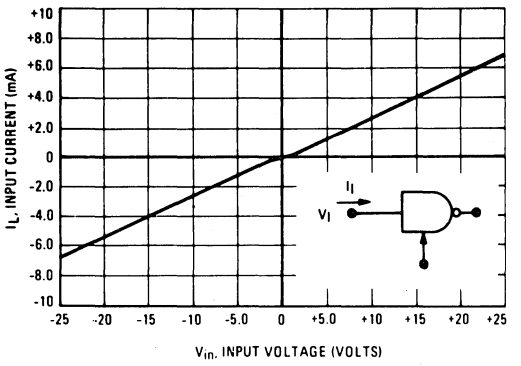


FIGURE 4 — MC1489 INPUT THRESHOLD VOLTAGE ADJUSTMENT

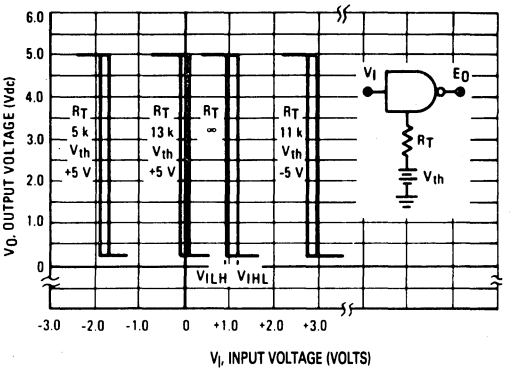


FIGURE 5 — MC1489A INPUT THRESHOLD VOLTAGE ADJUSTMENT

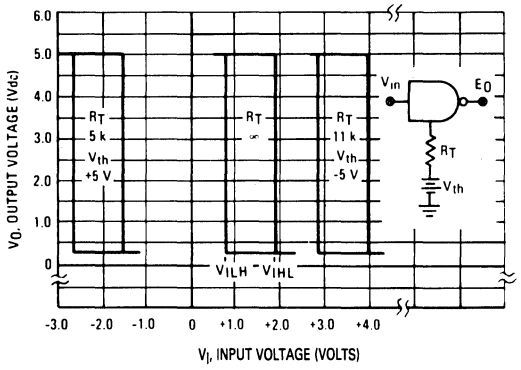


FIGURE 6 — INPUT THRESHOLD VOLTAGE versus TEMPERATURE

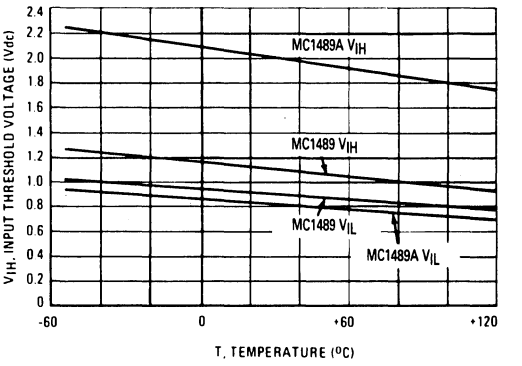
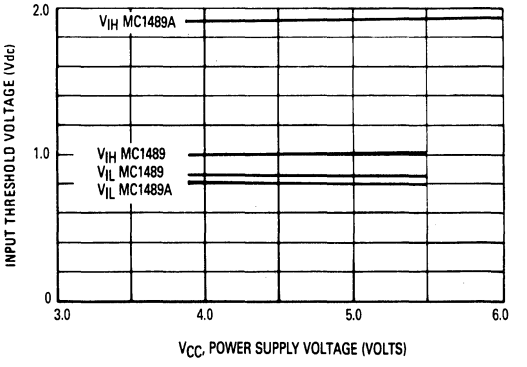


FIGURE 7 — INPUT THRESHOLD versus POWER-SUPPLY VOLTAGE



APPLICATIONS INFORMATION

General Information

The Electronic Industries Association (EIA) has released the EIA-232D specification detailing the requirements for the interface between data processing equipment and data communications equipment. This standard specifies not only the number and type of interface leads, but also the voltage levels to be used. The MC1488 quad driver and its companion circuit, the MC1489 quad receiver, provide a complete interface system between DTL or TTL logic levels and the EIA-232D defined levels. The EIA-232D requirements as applied to receivers are discussed herein.

The required input impedance is defined as between 3000 ohms and 7000 ohms for input voltages between 3.0 and 25 volts in magnitude; and any voltage on the receiver input in an open circuit condition must be less than 2.0 volts in magnitude. The MC1489 circuits meet these requirements with a maximum open circuit voltage of one V_{BE}.

The receiver shall detect a voltage between −3.0 and −25 volts as a Logic "1" and inputs between +3.0 and +25 volts as a Logic "0." On some interchange leads, an open circuit of power "OFF" condition (300 ohms or more to ground) shall be decoded as an "OFF" condition or Logic "1." For this reason, the input hysteresis thresholds of the MC1489 circuits are all above ground. Thus an open or grounded input will cause the same output as a negative or Logic "1" input.

Device Characteristics

The MC1489 interface receivers have internal feedback from the second stage to the input stage providing input hysteresis for noise rejection. The MC1489 input has typical turn-on voltage of 1.25 volts and turn-off of 1.0 volt for a typical hysteresis of 250 mV. The MC1489A has typical turn-on of 1.95 volts and turn-off of 0.8 volt for typically 1.15 volts of hysteresis.

Each receiver section has an external response control node in addition to the input and output pins, thereby allowing the designer to vary the input threshold voltage levels. A resistor can be connected between this node and an external power supply. Figures 2, 4 and 5 illustrate the input threshold voltage shift possible through this technique.

This response node can also be used for the filtering of high-frequency, high energy noise pulses. Figures 8 and 9 show typical noise-pulse rejection for external capacitors of various sizes.

These two operations on the response node can be combined or used individually for many combinations of interfacing applications. The MC1489 circuits are particularly useful for interfacing between MOS circuits and MDTL/MTTL logic systems. In this application, the input threshold voltages are adjusted (with the appropriate supply and resistor values) to fall in the center of the MOS voltage logic levels. (See Figure 10)

The response node may also be used as the receiver input as long as the designer realizes that he may not drive this node with a low impedance source to a voltage greater than one diode above ground or less than one diode below ground. This feature is demonstrated in Figure 11 where two receivers are slaved to the same line that must still meet the EIA-232D impedance requirement.

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FIGURE 8 — TYPICAL TURN-ON THRESHOLD versus CAPACITANCE FROM RESPONSE CONTROL PIN TO GND

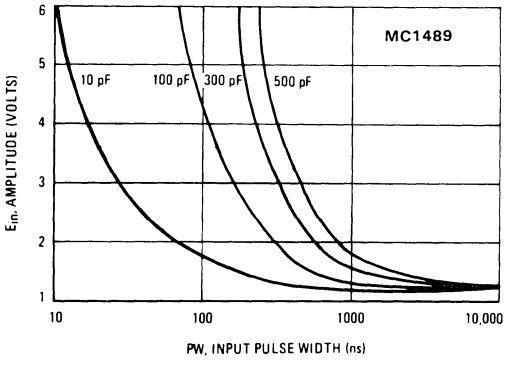


FIGURE 9 — TYPICAL TURN-ON THRESHOLD versus CAPACITANCE FROM RESPONSE CONTROL PIN TO GND

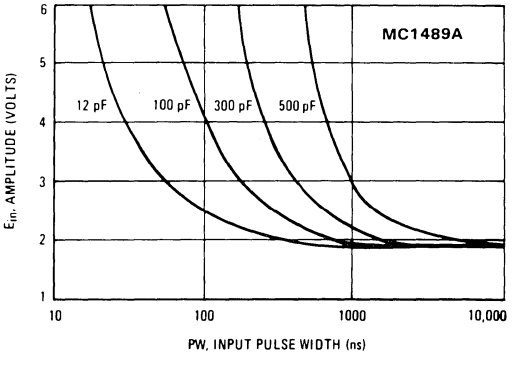


FIGURE 10 — TYPICAL TRANSLATOR APPLICATION — MOS TO DTL OR TTL

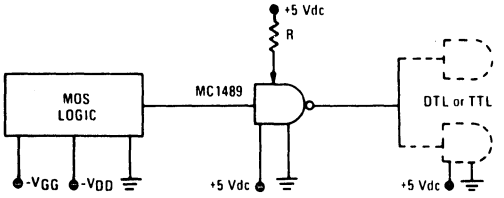
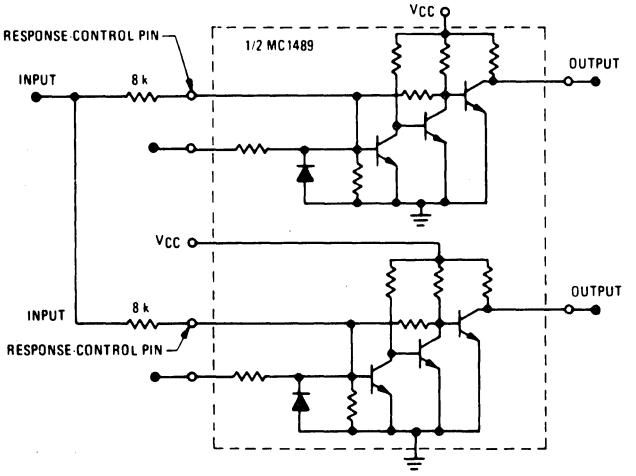


FIGURE 11 — TYPICAL PARALLELING OF TWO MC1489,A RECEIVERS TO MEET EIA-232D



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MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC14C88B

Advance Information

Quad Low Power Line Driver

QUAD LOW POWER LINE DRIVER

SILICON MONOLITHIC INTEGRATED CIRCUIT

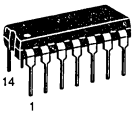
The MC14C88B is a low power monolithic quad line driver, using BiMOS technology, which conforms to EIA-232-D, EIA-562, and CCITT V.28. The inputs feature TTL and CMOS compatibility with minimal loading. The outputs feature internally controlled slew rate limiting, eliminating the need for external capacitors. Power off output impedance exceeds 300 Ω, and current limiting protects the outputs in the event of short circuits.

Power supply current is less than 160 μA over the supply voltage range of ±4.5 to ±15 V. EIA-232-D performance is guaranteed with a minimum supply voltage of ±6.5 V.

The MC14C88B is pin compatible with the MC1488, SN75188, SN75C188, DS1488, and DS14C88. This device is available in 14 pin plastic DIP, and surface mount packaging.

Features:

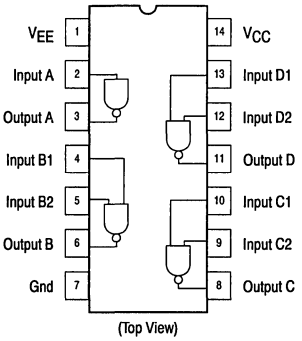
- BiMOS Technology for Low Power Operation (<5.0 mW)
- Meets Requirements of EIA-232-D, EIA-562, and CCITT V.28
- Quiescent Current Less Than 160 μA
- TTL/CMOS Compatible Inputs
- Minimum 300 Ω Output Impedance when Powered Off
- Supply Voltage Range: ±4.5 to ±15 V
- Pin Equivalent to MC1488
- Current Limited Output: 10 mA Minimum
- Operating Ambient Temperature: –40° to 85°C



P SUFFIX
PLASTIC PACKAGE
CASE 646

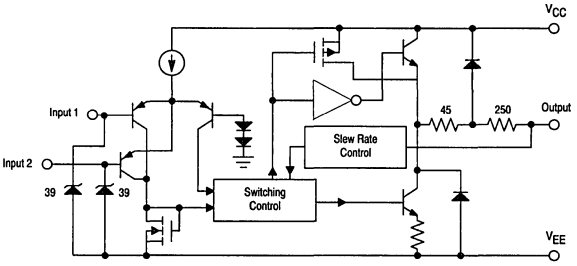
D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO-14)

PIN CONNECTIONS



(Top View)

Simplified Block Diagram
(Each Driver)



ORDERING INFORMATION

Device	Temperature Range	Package
MC14C88BP	–40° to +85°C	Plastic DIP
MC14C88BD		SO-14

MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage V_{CC}(max) V_{EE}(min) ($V_{CC} - V_{EE}$)max	 V_{CC} V_{EE} $V_{CC} - V_{EE}$	 +17 –17 34	Vdc
Input Voltage (All Inputs)	V_{in}	V_{EE}–0.3, V_{EE}+39	Vdc
Applied Output Voltage, when V_{CC}=V_{EE}≠0 V Applied Output Voltage, when V_{CC}=V_{EE}=0 V	V_X	V_{EE}–6.0 V, V_{CC}+6.0 V ±15	Vdc
Output Current	I_O	Self Limiting	mA
Operating Junction Temperature	T_J	–65, +150	°C

Devices should not be operated at these limits. The "Recommended Operating Conditions" table provides for actual device operation.

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	V_{CC} V_{EE}	+4.5 –15	— —	+15 –4.5	Vdc
Input Voltage (All Inputs)	V_{in}	0	—	V_{CC}	Vdc
Applied Output Voltage (V_{CC}=V_{EE}=0 V)	V_O	–2.0	0	+2.0	Vdc
Output DC Load	R_L	3.0	—	7.0	kΩ
Operating Ambient Temperature Range	T_A	–40	—	+85	°C

All limits are not necessarily functional concurrently.

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ELECTRICAL CHARACTERISTICS (–40°C ≤ T_A ≤ +85°C, unless otherwise noted.)*

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Current (I_{out} = 0, see Figure 2) I_{CC} @ 4.75 V ≤ V_{CC}, –V_{EE} ≤ 15 V Outputs High Outputs Low I_{EE} Outputs High Outputs Low	 I_{CC} (OH) I_{CC} (OL) I_{EE} (OH) I_{EE} (OL)	 — — –160 –160	 — — — —	 160 160 — —	µA
Output Voltage – High, V_{in} ≤ 0.8 V (R_L = 3.0 kΩ, see Figure 3) V_{CC} = +4.75 V, V_{EE} = –4.75 V V_{CC} = +5.0 V, V_{EE} = –5.0 V V_{CC} = +6.5 V, V_{EE} = –6.5 V V_{CC} = +12 V, V_{EE} = –12 V V_{CC} = +13.2 V, V_{EE} = –13.2 V (R_L = ∞) Output Voltage – Low, V_{in} ≥ 2.0 V V_{CC} = +4.75 V, V_{EE} = –4.75 V V_{CC} = +5.0 V, V_{EE} = –5.0 V V_{CC} = +6.5 V, V_{EE} = –6.5 V V_{CC} = +12 V, V_{EE} = –12 V V_{CC} = +13.2 V, V_{EE} = –13.2 V (R_L = ∞)	V_{OH} V_{OL} 	 3.7 4.0 5.0 10 — — — — — –13.2	 3.8 4.3 6.1 10.5 13.2 –3.8 –4.2 –6.0 –10.5 –13.2	 — — — — 13.2 –3.7 –4.0 –5.0 –10 —	Vdc
Output Short Circuit Current** (see Figure 4) (V_{CC} = |V_{EE}| = 15 V) Normally High Output, shorted to ground Normally Low Output, shorted to ground	I_{OS}	 –35 +10	 — —	 –10 +35	mA
Output Source Resistance (V_{CC} = V_{EE} = 0 V, –2.0 V ≤ V_{out} ≤ +2.0 V)	R_O	300	—	—	Ω
Input Voltage Low Level High Level	 V_{IL} V_{IH}	 0 2.0	 — —	 0.8 V_{CC}	Vdc

* Typicals reflect performance @ T_A = 25°C
** Only one output shorted at a time, for not more than 1 second.

ELECTRICAL CHARACTERISTICS CONTINUED ($-40°C \le T_A \le +85°C$, unless otherwise noted.)*

Characteristic	Symbol	Min	Typ	Max	Unit
Input Current	I_{in}				μA
V_{in} = 0 V, V_{CC} = $\|V_{EE}\|$ = 4.75 V		–10	–0.1	0	
V_{in} = 0 V, V_{CC} = $\|V_{EE}\|$ = 15 V		–10	–0.1	0	
V_{in} = 4.5 V, V_{CC} = $\|V_{EE}\|$ = 4.75 V		0	+0.1	+10	
V_{in} = 4.5 V, V_{CC} = $\|V_{EE}\|$ = 15 V		0	+0.1	+10	

TIMING CHARACTERISTICS ($-40°C \le T_A \le +85°C$, unless otherwise noted.)*

Characteristic	Symbol	Min	Typ	Max	Unit
Output Rise Time					μs
V_{CC} = 4.75 V, V_{EE} = –4.75 V					
–3.3 V ≤ V_O ≤ 3.3 V	t_{R1}				
C_L = 15 pF		0.22	0.66	2.1	
C_L = 1000 pF		0.22	1.52	2.1	
–3.0 V ≤ V_O ≤ 3.0 V	t_{R2}				
C_L = 15 pF		0.20	0.51	1.5	
C_L = 1000 pF		0.20	1.16	1.5	
V_{CC} = 12.0 V, V_{EE} = –12.0 V					
–3.0 V ≤ V_O ≤ 3.0 V					
C_L = 15 pF		0.20	0.62	1.5	
C_L = 2500 pF		0.20	0.82	1.5	
10% ≤ V_O ≤ 90%	t_{R3}				
C_L = 15 pF		0.53	1.41	3.2	
Output Fall Time					μs
V_{CC} = 4.75 V, V_{EE} = –4.75 V					
3.3 V ≤ V_O ≤ –3.3 V	t_{F1}				
C_L = 15 pF		0.22	0.93	2.1	
C_L = 1000 pF		0.22	1.28	2.1	
3.0 V ≤ V_O ≤ –3.0 V	t_{F2}				
C_L = 15 pF		0.20	0.72	1.5	
C_L = 1000 pF		0.20	1.01	1.5	
V_{CC} = 12.0 V, V_{EE} = –12.0 V					
3.0 V ≤ V_O ≤ –3.0 V					
C_L = 15 pF		0.20	0.70	1.5	
C_L = 2500 pF		0.20	0.94	1.5	
90% ≤ V_O ≤ 10%	t_{F3}				
C_L = 15 pF		0.53	1.71	3.2	
Output Slew Rate, 3.0 kΩ < R_L < 7.0 kΩ, 15 pF < C_L < 2500 pF	S_R	4.0	—	30	V/μs
Propagation Delay A (C_L = 15 pF, see Figure 1)					μs
V_{CC} = 12.0 V, V_{EE} = –12.0 V					
Input to Output – Low to High	t_{PLH}	—	0.9	3.0	
Input to Output – High to Low	t_{PHL}	—	2.3	3.5	
Propagation Delay B (C_L = 15 pF, see Figure 1)					
V_{CC} = 4.75 V, V_{EE} = –4.75 V					
Input to Output – Low to High	t_{PLH}	—	0.4	2.0	
Input to Output – High to Low	t_{PHL}	—	1.5	2.5	

* Typicals reflect performance @ T_A = 25°C

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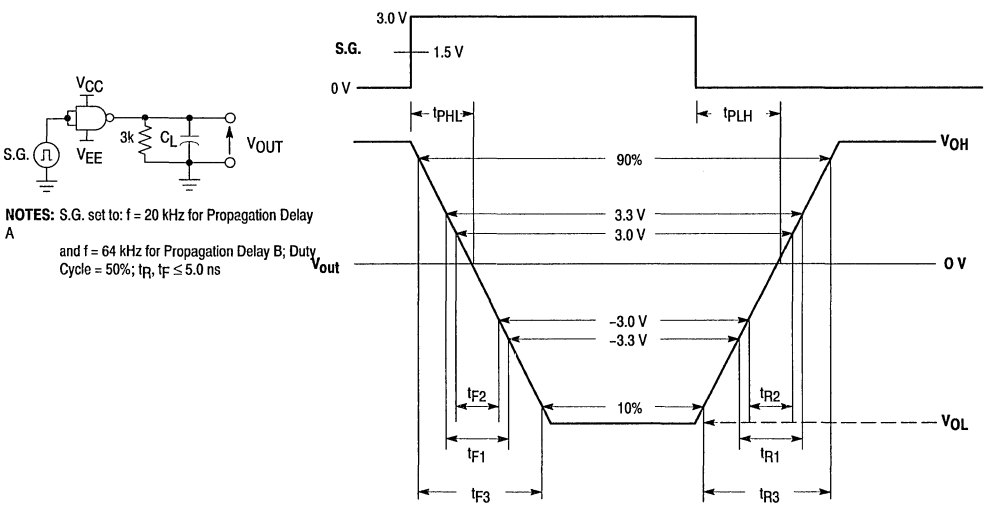
Figure 1. Timing Diagram



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STANDARDS COMPLIANCE

The MC14C88 is designed to comply with EIA-232-D (formerly RS-232), the newer EIA-562 (which is a higher speed version of the EIA-232), and CCITT's V.28. EIA-562 was written around modern integrated circuit technology, whereas EIA-232 retains many of the specs written around the electro-mechanical circuitry in use at the time of its creation. Yet the user will find enough similarities to allow a certain amount of compatibility among equipment built to the two standards. Following is a summary of the key specifications relating to the systems and the drivers.

Parameter	EIA-232-D	EIA-562
Maximum Data Rate	20 kbaud	38.4 kbaud Asynchronous 64 kbaud Synchronous
Maximum Cable Length	50 feet	Based on cable capacitance/data rate
Maximum Slew Rate	≤ 30 V/μs anywhere on the waveform	≤ 30 V/μs anywhere on the waveform ≥ 4.0 V/μs between +3.0 and –3.0 V
Transition Region	–3.0 to +3.0 V	–3.3 to +3.3 V
Transition Time	For UI ≥ 25 ms, t_R ≤ 1.0 ms For 25 ms > UI > 125 μs, t_R ≤ 4% UI For UI < 125 μs, t_R ≤ 5.0 μs	For UI ≥ 50 μs, 220 ns < t_R ≤ 3.1 μs For UI < 50 μs, 220 ns < t_R ≤ 2.1 μs (within the transition region)
MARK (one, off)	More negative than –3.0 V	More negative than –3.3 V
Space (zero, on)	More positive than +3.0 V	More positive than +3.3 V
Short Circuit Proof ?	Yes, to any system voltage	Yes, to ground
Short Circuit Current	≤ 500 mA to any system voltage	≤ 60 mA to ground
Open Circuit Voltage	$\|V_{OC}\|$ ≤ 25 V	$\|V_{OC}\|$ < 13.2 V
Loaded Output Voltage	5.0 V ≤ $\|V_O\|$ ≤ 15 V for loads between 3.0 kΩ and 7.0 kΩ	$\|V_O\|$ ≥ 3.7 V for a load of 3.0 kΩ
Power Off Input Source Impedance	≥ 300 Ω for $\|V_O\|$ ≤ 2.0 V	≥ 300 Ω for $\|V_O\|$ ≤ 2.0 V

NOTE: UI = Unit Interval, or bit time.
V.28 standard has the same specifications as EIA-232, with the exception of transition time which is listed as "less than 1.0 ms, or 3% of the UI, whichever is less".

Figure 2. Typical Supply Current versus Supply Voltage

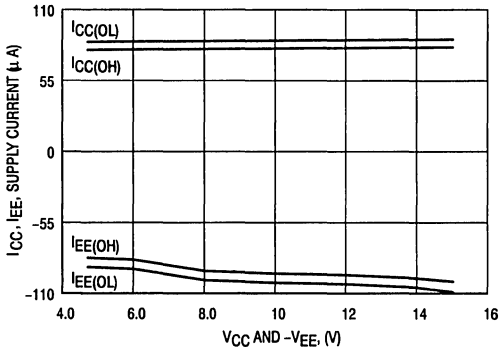


Figure 3. Typical Output Voltage versus Supply Voltage

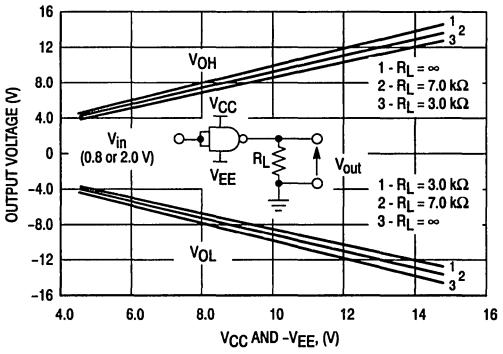


Figure 4. Typical Short Circuit Current versus Supply Voltage

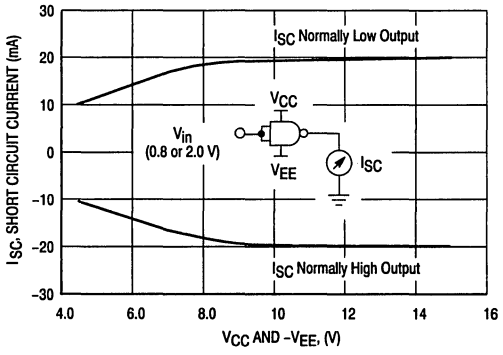
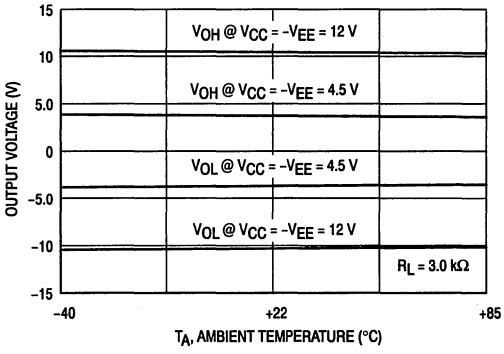


Figure 5. Typical Output Voltage versus Temperature



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APPLICATIONS INFORMATION

Description

The MC14C88 was designed to be a direct replacement for the MC1488 in that it meets all EIA-232 specifications. However, use is extended as the MC14C88 also meets the faster EIA-562 and CCITT V.28 specifications. Slew rate limited outputs conform to the mentioned specifications and eliminate the need for external output capacitors. Low power consumption is made possible by BiMOS technology. Power supply current is limited to less than 160 μA, plus load currents over the supply voltage range of ±4.5 V to ±15 V (see Figure 2).

Outputs

The output low or high voltage depends on the state of the inputs, the load current, and the supply voltage (see Table 1 and Figure 3). The graphs apply to each driver regardless of how many other drivers within the package are supplying load current.

Table 1. Function Tables

Driver 1

Input A	Output A
H	L
L	H

Drivers 2 through 4

Input *1	Input *2	Output*
H	H	L
L	X	H
X	L	H

H = High level, L = Low level, X = Don't care.

Driver Inputs

The driver inputs determine the state of the outputs in accordance with Table 1. The nominal threshold voltage for the inputs is 1.4 Vdc, and for proper operation, the input voltages should be restricted to the range Gnd to V_{CC}. Should the input voltage drop below V_{EE} by more than 0.3 V or rise above V_{EE} by more than 39 V, excessive currents will flow at the input pin. Open input pins are equivalent to logic high, but good design practices dictate that inputs should never be left open.

Operating Temperature Range

The ambient operating temperature range is listed as –40° to +85°C and meets EIA-232-D, EIA-562 and CCITT V.28 specifications over this temperature range. The maximum ambient temperature is listed as +85°C. However, a lower ambient may be required depending on system use, i.e. specifically how many drivers within a package are used, and at what current levels they are operating. The maximum power which may be dissipated within the package is determined by:

$$P_{Dmax} = \frac{T_{Jmax} - T_A}{R_{\theta JA}}$$

where: $R_{\theta JA}$ = the package thermal resistance (typically, 100°C/W for the DIP package, 125°C/W for the SOIC package);
T_{Jmax} = the maximum operating junction temperature (150°C); and
T_A = the ambient temperature.

$$P_D = \{ [(V_{CC} - V_{OH}) \bullet |I_{OH}|] \text{ or } [(V_{OL} - V_{EE}) \bullet |I_{OL}|] \}_{\text{each driver}} + (V_{CC} \bullet I_{CC}) + (V_{EE} \bullet I_{EE})$$

where: V_{CC} and V_{EE} are the positive and negative supply voltages;
V_{OH} and V_{OL} are measured or estimated from Figure 3;
I_{CC} and I_{EE} are the quiescent supply currents measured or estimated from Figure 2.

As indicated, the first term (in brackets) must be calculated and summed for each of the four drivers, while the last terms are common to the entire package.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC14C89B
MC14C89AB

Advance Information

Quad Low Power Line Receiver

QUAD LOW POWER LINE RECEIVER

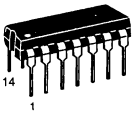
The MC14C89B and MC14C89AB are low power monolithic quad line receivers, using bipolar technology, which conform to the EIA-232-E, EIA-562 and CCITT V.28 Recommendations. The outputs feature LSTTL and CMOS compatibility for easy interface to +5.0 V digital systems. Internal time-domain filtering eliminates the need for external filter capacitors in most cases.

The MC14C89B has an input hysteresis of 0.35 V, while the MC14C89AB hysteresis is 0.95 V. The response control pins allow adjustment of the threshold level if desired. Additionally, an external capacitor may be added for additional noise filtering.

The MC14C89B and MC14C89AB are each available in a 14 pin dual-in-line plastic DIP and SOIC package.

Features:

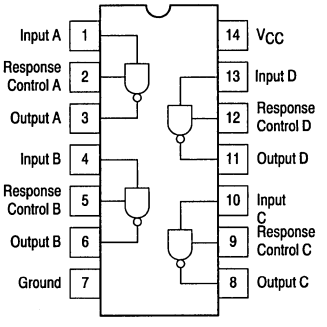
- Low Power Consumption
- Meets EIA-232-E, EIA-562, and CCITT V.28 Recommendations
- TTL/CMOS Compatible Outputs
- Standard Power Supply: + 5.0 V ± 10%
- Pin Equivalent to MC1489, MC1489A, TI's SN75C189/A, SN75189/A and National Semiconductor's DS14C89/A
- External Filtering Not Required in Most Cases
- Threshold Level Externally Adjustable
- Hysteresis: 0.35 V for MC14C89B, 0.95 V for MC14C89AB
- Available in Plastic DIP, and Surface Mount Packaging
- Operating Ambient Temperature: -40° to +85°C



P SUFFIX
PLASTIC PACKAGE
CASE 646

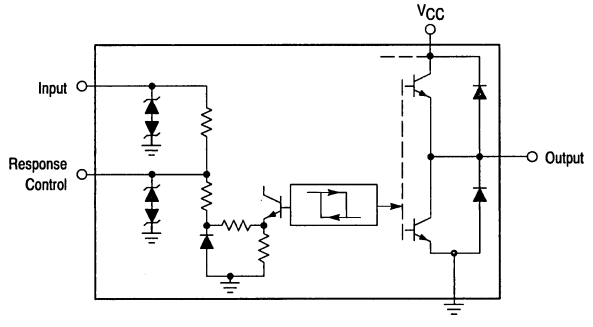
D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO-14)

PIN CONNECTIONS



(Top View)

Simplified Block Diagram
(Each Receiver)



ORDERING INFORMATION

Device	Temperature Range	Package
MC14C89BP	–40° to +85°C	Plastic DIP
MC14C89BD		SO-14
MC14C89ABP		Plastic DIP
MC14C89ABD		SO-14

7

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage $V_{CC(max)}$ $V_{CC(min)}$	V_{CC}	 +7.0 −0.5	Vdc
Input Voltage	V_{in}	±30	Vdc
Output Load Current	I_O	Self-Limiting	—
Junction Temperature	T_J	−65, +150	°C

Devices should not be operated at these limits. The "Recommended Operating Conditions" table provides for actual device operation.

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	V_{CC}	4.5	5.0	5.5	Vdc
Input Voltage	V_{in}	−25	—	25	Vdc
Output Current Capability	I_O	−7.5	—	6.0	mA
Operating Ambient Temperature	T_A	−40	—	85	°C

All limits are not necessarily functional concurrently.

ELECTRICAL CHARACTERISTICS ($-40°C \le T_A \le 85°C$, unless otherwise noted.)*

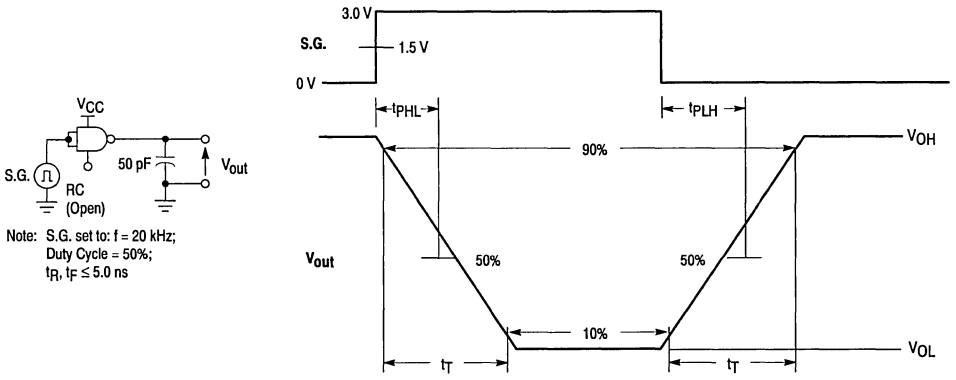
Characteristic	Symbol	Min	Typ	Max	Unit
Supply Current (I_{out} = 0) I_{CC} @ +4.5 V ≤ V_{CC} ≤ +5.5 V	I_{CC}	 —	 330	 700	µA
Output Voltage — High, V_{in} ≤ 0.4 V (See Figures 2 and 3)	V_{OH}				Vdc
I_{out} = −20 µA V_{CC} = 4.5 V		3.5	3.8	—	
V_{CC} = 5.5 V		3.5	4.8	—	
I_{out} = −3.2 mA V_{CC} = 4.5 V		2.5	3.7	—	
V_{CC} = 5.5 V		2.5	4.7	—	
Output Voltage — Low, V_{in} ≥ 2.4 V	V_{OL}				
I_{out} = 3.2 mA V_{CC} = 4.5 V		—	0.1	0.4	
V_{CC} = 5.5 V		—	0.1	0.4	
Output Short Circuit Current** (V_{CC} = 5.5 V, see Figure 4)	I_{OS}				mA
Normally High Output shorted to ground		−35	−13.9	—	
Normally Low Output shorted to V_{CC}		—	+10.3	35	
Input Threshold Voltage (V_{CC} = 5.0 V)					
(MC14C89AB, see Figure 5) Low Level	V_{IL}	0.75	0.95	1.25	Vdc
High Level	V_{IH}	1.6	1.90	2.25	
(MC14C89B, see Figure 6) Low Level	V_{IL}	0.75	0.95	1.25	
High Level	V_{IH}	1.0	1.3	1.5	
Input Impedance (+4.5 V < V_{CC} < +5.5 V −25 V < V_{in} < +25 V)		3.0	5.5	7.0	kΩ

* Typicals reflect performance @ T_A = 25°C
** Only one output shorted at a time, for not more than 1.0 seconds.

TIMING CHARACTERISTICS (T_A = +25°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Transition Time (10% to 90%) 4.5 V ≤ V_{CC} ≤ 5.5 V	t_T	 —	 0.08	 0.30	µs
Propagation Delay Time 4.5 V ≤ V_{CC} ≤ 5.5 V					
Output Low-to-High	t_{PLH}	—	3.35	6.0	µs
Output High-to-Low	t_{PHL}	—	2.55	6.0	
Input Noise Rejection (see Figure 9)		1.0	1.5	—	µs

Figure 1. Timing Diagram



STANDARDS COMPLIANCE

The MC14C89B and MC14C89AB are designed to comply with EIA-232-E (formerly RS-232), the newer EIA-562 (which is a higher speed version of the EIA-232), and CCITT V.28 Recommendations. EIA-562 was written around modern integrated circuit technology, whereas EIA-232 retains many of the specifications written around the electro-mechanical circuitry in use at the time of its creation. Yet the user will find enough similarities to allow a certain amount of compatibility among equipment built to the two standards. Following is a summary of the key specifications relating to the systems and the receivers.

Parameter	EIA-232-E	EIA-562
Max Data Rate	20 kBaud	38.4 kBaud Asynchronous 64 kBaud Synchronous
Max Cable Length	50 feet	Based on cable capacitance/data rate
Transition Region	–3.0 V to +3.0 V	–3.0 V to +3.0 V
MARK (one, off)	More negative than –3.0 V	More negative than –3.3 V
SPACE (zero, on)	More positive than +3.0 V	More positive than +3.3 V
Fail Safe	Output = Binary 1	Output = Binary 1
Open Circuit Input Voltage	< |2.0|V	Not Specified
Slew Rate (at the driver)	≤ 30 V/µs anywhere on the waveform	≤ 30 V/µs anywhere on the waveform, ≥ 4.0 V/µs between +3.0 V and –3.0 V
Loaded Output Voltage (at the driver)	5.0 V ≤ |VO| ≤ 15 V for loads between 3.0 kΩ and 7.0 kΩ	|VO| ≥ 3.7 V for a load of 3.0 kΩ

Figure 2. Typical Output versus Supply Voltage

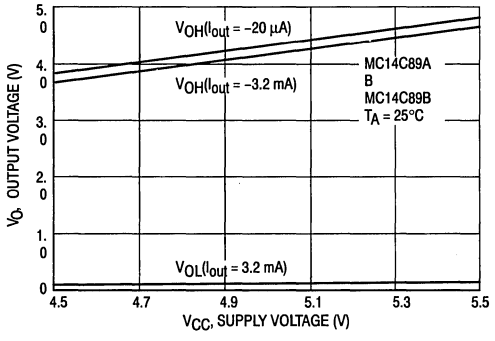


Figure 3. Typical Output Voltage versus Temperature

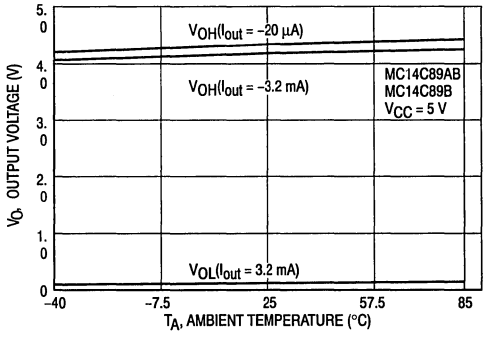


Figure 4. Typical Short Circuit Current versus Temperature

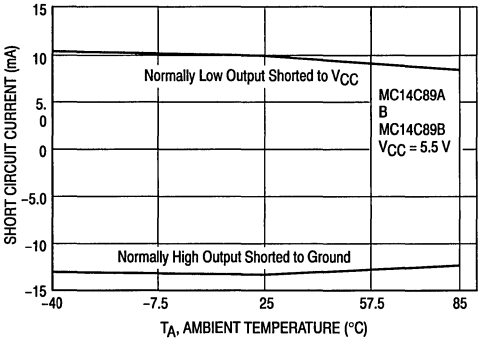


Figure 5. Typical Threshold Voltage versus Temperature

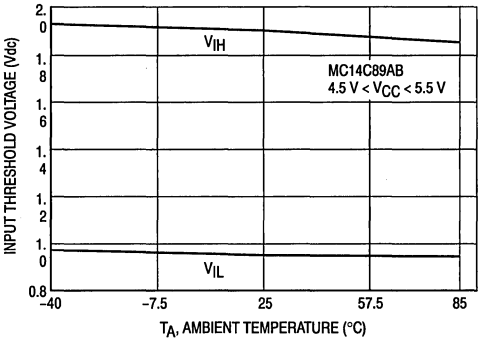


Figure 6. Typical Threshold Voltage versus Temperature

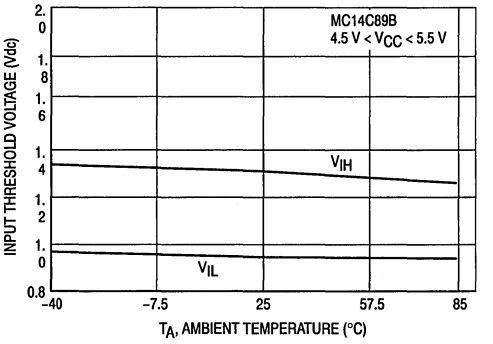


Figure 7. Typical Effect of Response Control Pin Bias

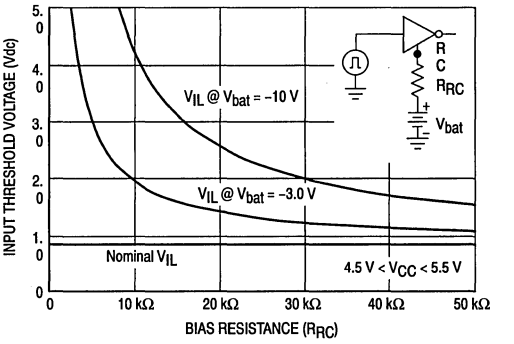
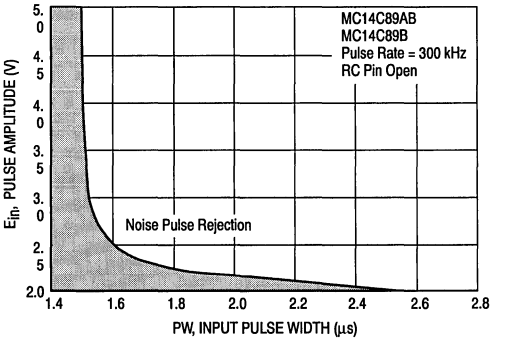


Figure 8. Typical Noise Pulse Rejection



APPLICATIONS INFORMATION

Description

The MC14C89AB and MC14C89B are designed to be direct replacements for the MC1489A and MC1489. Both devices meet all the EIA-232 specifications and also the faster EIA-562 and CCITT V.28 specifications. Noise pulse rejection circuitry eliminates the need for most response control filter capacitors but does not exclude the possibility as filtering is still possible at the Response Control (RC) pins. Also, the Response Control pins allow for a user defined selection of the threshold voltages. The MC14C89AB and MC14C89B are manufactured with a bipolar technology using low power techniques and consume at most 700 μA, plus load currents with a +5.0 V supply.

Outputs

The output low or high voltage depends on the state of the inputs, the load current, the bias of the Response Control pins, and the supply voltage. Table 1 applies to each receiver, regardless of how many other receivers within the package are supplying load current.

Table 1. Function Table

Receivers

Input *	Output *
H	L
L	H

*The asterisk denotes A, B, C, or D.

Receiver Inputs and Response Control

The receiver inputs determine the state of the outputs in accordance with Table 1. The nominal V_{IL} and V_{IH} thresholds are 0.95 V and 1.90 V respectively for the MC14C89AB. For the MC14C89B, the nominal V_{IL} and V_{IH} thresholds are 0.95 and 1.30, respectively. The inputs are able to withstand ± 30 V referenced to ground. Should the input voltage exceed ground by more than ± 30 V, excessive currents will flow at the input pin. Open input pins will generate a logic high output, but good design practices dictate that inputs should never be left open.

The Response Control (RC) pins are coupled to the inputs through a resistor string. The RC pins provide for adjustment of the threshold voltages of the IC while preserving the amount of hysteresis. Figure 10 shows a typical application to adjust the threshold voltages. The RC pins also provide access to an internal resistor string which permits low pass filtering of the input signal within the IC. Like the input pins, the RC pins should not be taken above or below ground by more than ± 30 V or excessive currents will flow at these pins. The dependence of the low level threshold voltage (V_{IL}) upon R_{RC} and V_{bat} can be described by the following equation,

$$V_{IL} \simeq \left\{V_{0.09} - V_{bat}\left[\frac{505\ \Omega}{R_{RC}\ (1.6) + 2.02\ k\Omega}\right]\right\} \left(\frac{5.32\ k\Omega + \frac{6.67 \times 10^6\ \Omega^2}{R_{RC}}}{505\ \Omega}\right) \quad (1)$$

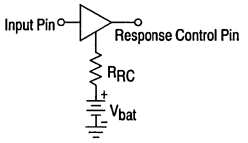
V_{IH} can be found by calculating for V_{IL} using equation (1) then adding the hysteresis for each device (0.35 for the MC14C89B or 0.95 V for the MC14C89AB). Figure 7 plots equation (1) for two values of V_{bat} and a range of R_{RC}.

If an RC pin is to be used for low pass filtering, the capacitor chosen can be calculated by the equation,

$$C_{RC} \simeq \frac{1}{2.02\ k\Omega\ 2\pi\ f_{-3\ dB}} \quad (2)$$

where $f_{-3\ dB}$ represents the desired –3 dB roll-off frequency of the low pass filter.

Figure 10. Application to Adjust Thresholds



Another feature of the MC14C89AB and MC14C89B is input noise rejection. The inputs have the ability to ignore pulses which exceed the V_{IH} and V_{IL} thresholds but are less than 1.0 μs in duration. As the duration of the pulse exceeds 1.0 μs, the noise pulse may still be ignored depending on its amplitude. Figure 8 is a graph showing typical input noise rejection as a function of pulse amplitude and pulse duration. Figure 8 reflects data taken for an input with an unconnected RC pin and applied to the MC14C89AB and MC14C89B.

Operating Temperature Range

The ambient operating temperature range is listed as –40°C to +85°C, and the devices are designed to meet the EIA-232-E, EIA-562 and CCITT V.28 specifications over this temperature range. The Timing Characteristics are guaranteed to meet the specifications at +25°C. The maximum ambient operating temperature is listed as +85°C. However, a lower ambient may be required depending on system use, (i.e., specifically how many receivers within a package are used) and at what current levels they are operating. The maximum power which may be dissipated within the package is determined by:

$$P_{D(max)} = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

where: $R_{\theta JA}$ = thermal resistance (typ., 100°C/W for the DIP and 125°C/W for the SOIC packages);
$T_{J(max)}$ = maximum operating junction temperature (150°C); and
T_A = ambient temperature.

$$P_D = \{[(V_{CC} - V_{OH}) \bullet |I_{OH}|] \text{ or } [(V_{OL}) \bullet |I_{OL}|]\}_{\text{each receiver}} + (V_{CC} \bullet I_{CC})$$

where: V_{CC} = positive supply voltage;
V_{OH}, V_{OL} = measured or estimated from Figure 2 and 3;
I_{CC} = measured quiescent supply current.

As indicated, the first term (in brackets) must be calculated and summed for each of the four receivers, while the last term is common to the entire package.

MC26S10

QUAD OPEN-COLLECTOR BUS TRANSCEIVER

This quad transceiver is designed to mate Schottky TTL or NMOS logic to a low impedance bus. The $\overline{\text{Enable}}$ and Driver inputs are PNP buffered to ensure low input loading. The Driver (Bus) output is open-collector and can sink up to 100 mA at 0.8 V, thus the bus can drive impedances as low as 100 Ω. The receiver output is active pull-up and can drive ten Schottky TTL loads.

An active-low $\overline{\text{Enable}}$ controls all four drivers allowing the outputs of different device drivers to be connected together for party-line operation. The line can be terminated at both ends and still give considerable noise margin at the receiver. Typical receiver threshold is 2.0 V.

Advanced Schottky processing is utilized to assure fast propagation delay times. Two ground pins are provided to improve ground current handling and allow close decoupling between V_{CC} and ground at the package. Both ground pins should be tied to the ground bus external to the package.

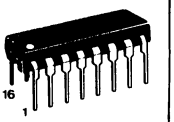
- Driver Can Sink 100 mA at 0.8 V (Max)
- PNP Inputs for Low-Logic Loading
- Typical Driver Delay = 10 ns
- Typical Receiver Delay = 10 ns
- Schottky Processing for High Speed
- Inverting Driver

QUAD OPEN-COLLECTOR BUS TRANSCEIVER

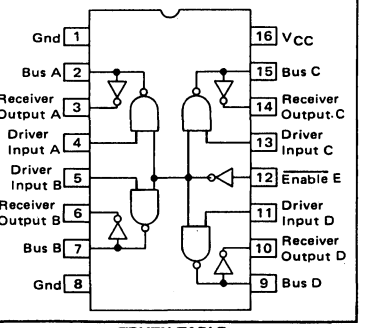
SCHOTTKY
SILICON MONOLITHIC
INTEGRATED CIRCUIT

D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO-16)

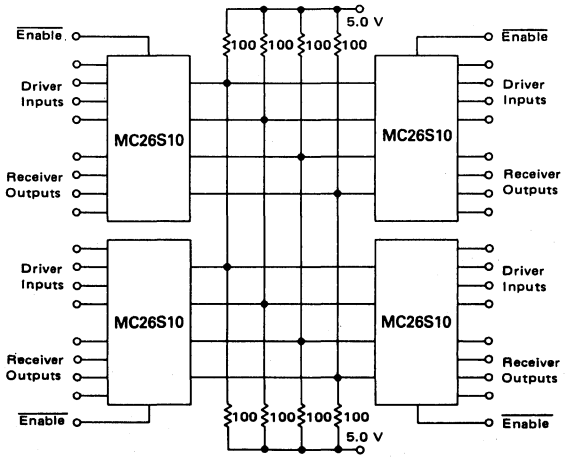
P SUFFIX
PLASTIC PACKAGE
CASE 648



PIN CONNECTIONS



TYPICAL APPLICATION



TRUTH TABLE

$\overline{\text{Enable}}$	Driver Input	Bus	Receiver Output
L	L	H	L
L	H	L	H
H	X	Y	

L = Low Logic State
H = High Logic State
X = Irrelevant
Y = Assumes condition controlled by other elements on the bus

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	–0.5 to +7.0	Vdc
Input Voltage	V_I	–0.5 to +5.5	Vdc
Input Current	I_I	–3.0 to +5.0	mA
Output Voltage — High Impedance State	$V_{O\ (Hi\text{-}z)}$	–0.5 to V_{CC}	V
Output Current — Bus	$I_{O(B)}$	200	mA
Output Current — Receiver	$I_{O(R)}$	30	mA
Operating Ambient Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	–65 to +150	°C
Junction Temperature	T_J	150	°C

ELECTRICAL CHARACTERISTICS (Unless otherwise noted V_{CC} = 4.75 to 5.25 V and T_A = 0 to +70°C. Typical values measured at V_{CC} = 5.0 V and T_A = 25°C.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Voltage — Low Logic State (Driver and $\overline{\text{Enable}}$ Inputs)	V_{IL}	–	–	0.8	V
Input Voltage — High Logic State (Driver and $\overline{\text{Enable}}$ Inputs)	V_{IH}	2.0	–	–	V
Input Clamp Voltage (Driver and Enable Inputs) (I_{IK} = -18 mA)	V_{IK}	–	–	-1.2	V
Input Current — Low Logic State (V_{IL} = 0.4 V)	I_{IL}				mA
($\overline{\text{Enable}}$ Input)		–	–	-0.36	
(Driver Inputs)		–	–	-0.54	
Input Current — High Logic State (V_{IH} = 2.7 V)	I_{IH}				μA
($\overline{\text{Enable}}$ Input)		–	–	20	
(Driver Inputs)		–	–	30	
Input Current — Maximum Voltage (V_{IH1} = 5.5 V) ($\overline{\text{Enable}}$ or Driver Inputs)	I_{IH1}	–	–	100	μA
Driver Output Voltage — Low Logic State	$V_{OL(D)}$				V
(I_{OL} = 40 mA)		–	0.33	0.5	
(I_{OL} = 70 mA)		–	0.42	0.7	
(I_{OL} = 100 mA)		–	0.51	0.8	
Driver (Bus) Leakage Current	$I_{O(D)}$				μA
(V_{OH} = 4.5 V)		–	–	100	
(V_{OL} = 0.8 V)		–	–	-50	
Driver (Bus) Leakage Current (V_{CC} = 0 V, V_{OH} = 4.5 V)	$I_{O1(D)}$	–	–	100	μA
Receiver Input High Threshold ($V_{IH(\overline{E})}$ = 2.4 V)	$V_{TH(R)}$	2.25	2.0	–	V
Receiver Input Low Threshold ($V_{IH(\overline{E})}$ = 2.4 V)	$V_{TL(R)}$	–	2.0	1.75	V
Receiver Output Voltage — Low Logic State (I_{OL} = 20 mA)	$V_{OL(R)}$	–	–	0.5	V
Receiver Output Voltage — High Logic State (I_{OH} = -1.0 mA)	$V_{OH(R)}$	2.7	3.4	–	V
Receiver Output Short-Circuit Current (Note 1)	$I_{OS(R)}$	-18	–	-60	mA
Power Supply Current — Output Low State ($V_{IL(\overline{E})}$ = 0 V)	I_{CC}	–	45	70	mA

NOTE 1: One output shorted at a time. Duration not to exceed 1.0 second.

SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Time Driver Input to Output	$t_{PLH(D)}$	—	10	15	ns
	$t_{PHL(D)}$	—	10	15	
Propagation Delay Time $\overline{\text{Enable}}$ Input to Output	$t_{PLH(\overline{E})}$	—	14	18	ns
	$t_{PHL(\overline{E})}$	—	13	18	
Propagation Delay Time Bus to Receiver Output	$t_{PLH(R)}$	—	10	15	ns
	$t_{PHL(R)}$	—	10	15	
Rise and Fall Time of Driver Output	$t_{TLH(D)}$	4.0	10	—	ns
	$t_{THL(D)}$	2.0	4.0	—	

7

SWITCHING WAVEFORMS AND CIRCUITS

FIGURE 1 — DATA INPUT TO BUS OUTPUT (DRIVER)

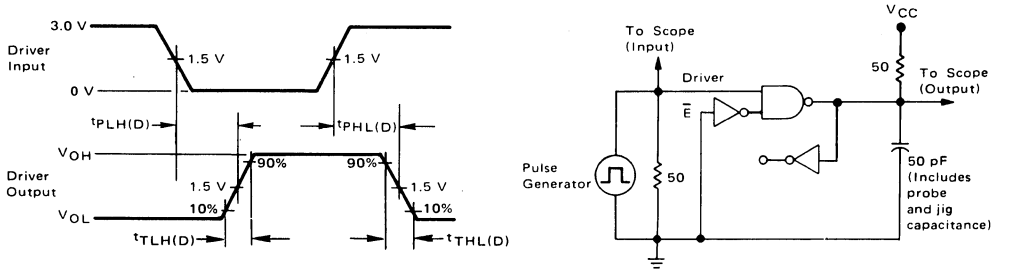


FIGURE 2 — ENABLE INPUT TO BUS OUTPUT (DRIVER)

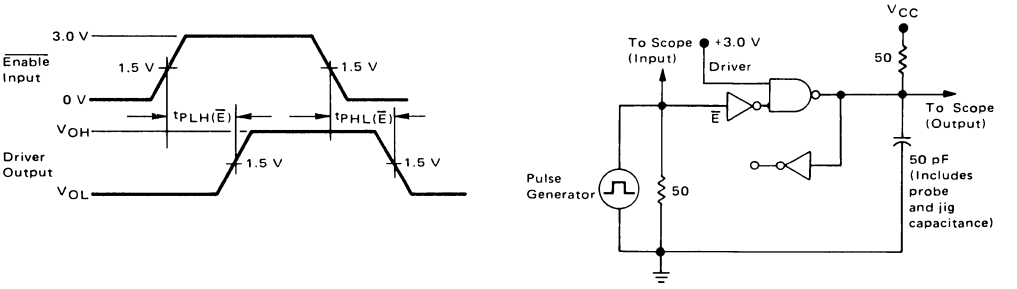
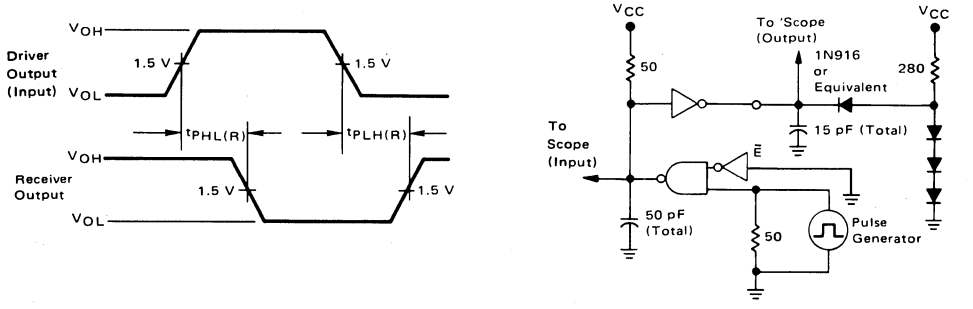


FIGURE 3 — BUS INPUT TO RECEIVER OUTPUT



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC3437

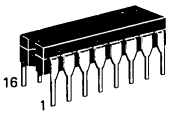
HEX BUS RECEIVER

SILICON MONOLITHIC
INTEGRATED CIRCUIT

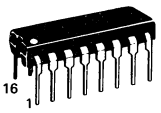
HEX BUS RECEIVER WITH INPUT HYSTERESIS

These high-speed bus receivers are useful in bus organized data transmission systems employing terminated 120 Ω lines. The receivers feature input hysteresis to obtain improved noise immunity. The receivers low input current requirement allows up to 27 driver/receiver pairs to share a common bus. A pair of Disable Inputs are provided. These Disable Inputs along with the receiver outputs are MTTL compatible.

- Built in receiver hysteresis
- Receiver input threshold is not affected by temperature
- Propagation delay time— 20 ns (Typ)
- Direct Replacement for DM8837

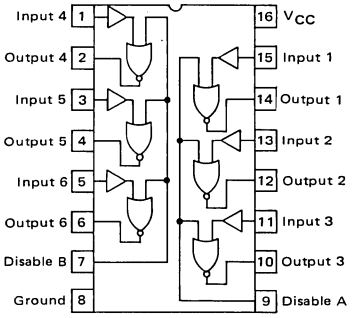


L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

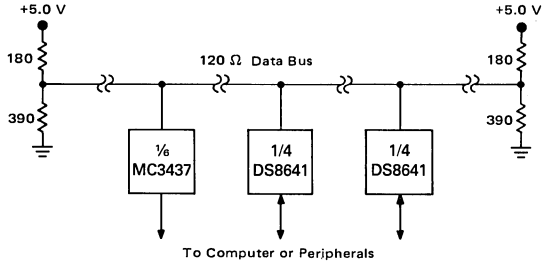
PIN CONNECTIONS



MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	7.0	Vdc
Input Voltage	V_I	5.5	Vdc
Power Dissipation Derate above 25°C	P_D	625 3.85	mW mW/°C
Operating Ambient Temperature Range	T_A	0 to 70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

FIGURE 1 — TYPICAL APPLICATION



TRUTH TABLE

Input	Disable	Output
O	L	H
O	H	L
I	L	L
I	H	L

O = < 1.05 V
I = > 2.5 V
H = High Logic State
L = Low Logic State

7

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, specifications apply for $0 \leq T_A \leq 70^oC$ and $4.75\ V \leq V_{CC} \leq 5.25\ V$.)

Characteristic	Symbol	Min	Typ	Max	Unit
Receiver Input Threshold Voltage — High Logic State ($V_{I(DA)} = 0.8\ V$, $I_{OL} = 16\ mA$, $V_{OL} \leq 0.4\ V$)	$V_{ILH(R)}$	1.80	2.25	2.50	V
Receiver Input Threshold Voltage — Low Logic State ($V_{I(DA)} = 0.8\ V$, $I_{OH} = -400\ \mu A$, $V_{OH} \geq 2.4\ V$)	$V_{IHL(R)}$	1.05	1.30	1.55	V
Receiver Input Current ($V_{I(R)} = 4.0\ V$, $V_{CC} = 5.25\ V$) ($V_{I(R)} = 4.0\ V$, $V_{CC} = 0\ V$)	$I_{I(R)}$	 – –	 15 1.0	 50 50	μA
Disable Input Voltage — High Logic State ($V_{I(R)} = 0.5\ V$, $V_{OL} \leq 0.4\ V$, $I_{OL} = 16\ mA$)	$V_{IH(DA)}$	2.0	–	–	V
Disable Input Voltage — Low Logic State ($V_{I(R)} = 0.5\ V$, $V_{OH} \geq 2.4\ V$, $I_{OH} = -400\ \mu A$)	$V_{IL(DA)}$	–	–	0.8	V
Output Voltage — High Logic State ($V_{I(R)} = 0.5\ V$, $V_{IL(DA)} = 0.8\ V$, $I_{OH} = -400\ \mu A$)	V_{OH}	2.4	–	–	V
Output Voltage — Low Logic State ($V_{I(R)} = 4.0\ V$, $V_{IL(DA)} = 0.8\ V$, $I_{OL} = 16\ mA$)	V_{OL}	–	0.25	0.4	V
Disable Input Current — High Logic State ($V_{IH(DA)} = 2.4\ V$) ($V_{IH(DA)} = 5.5\ V$)	$I_{IH(DA)}$	 – –	 – –	 80 2.0	 μA mA
Disable Input Current — Low Logic State ($V_{I(R)} = 4.0\ V$, $V_{IL(DA)} = 0.4\ V$)	$I_{IL(DA)}$	–	–	-3.2	mA
Output Short Circuit Current ($V_{I(R)} = 0.5\ V$, $V_{IL(DA)} = 0\ V$, $V_{CC} = 5.25\ V$)	I_{OS}	-18	–	-55	mA
Power Supply Current ($V_{I(R)} = 0.5\ V$, $V_{IL(DA)} = 0\ V$)	I_{CC}	–	45	65	mA
Input Clamp Diode Voltage ($I_{I(R)} = -12\ mA$, $I_{I(DA)} = -12\ mA$,	V_I	–	-1.0	-1.5	V

SWITCHING CHARACTERISTICS ($T_A = 25^oC$, $V_{CC} = 5.0\ V$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Time from Receiver Input to High Logic State Output	$t_{PLH(R)}$	–	20	30	ns
Propagation Delay Time from Receiver Input to Low Logic State Output	$t_{PHL(R)}$	–	18	30	ns
Propagation Delay Time from Disable Input to High Logic State Output	$t_{PLH(DA)}$	–	9.0	15	ns
Propagation Delay Time from Disable Input to Low Logic State Output	$t_{PHL(DA)}$	–	4.0	15	ns

FIGURE 2 — SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS

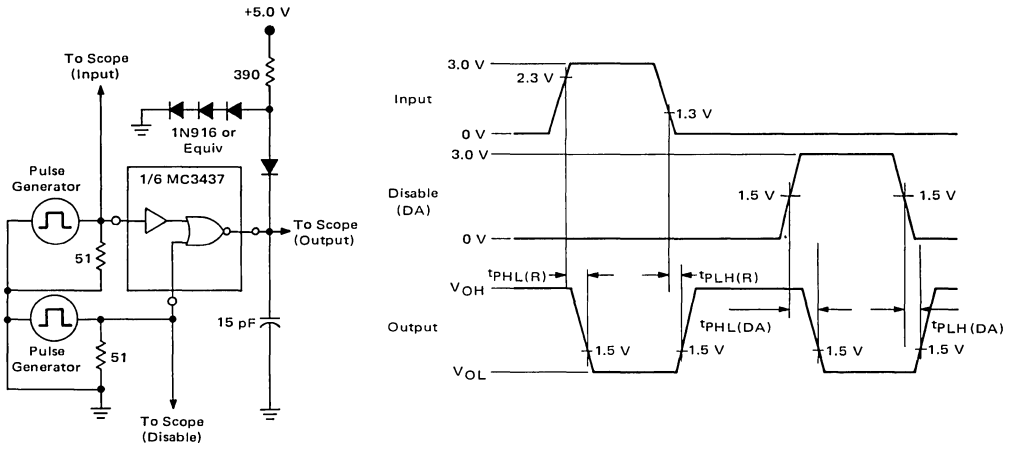


FIGURE 3 — TYPICAL HYSTERESIS

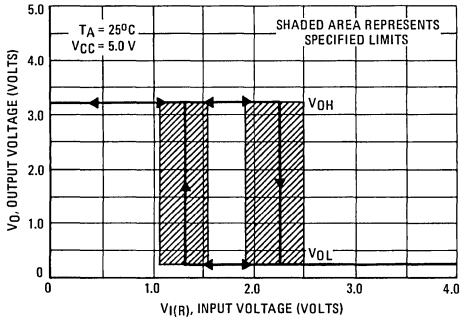
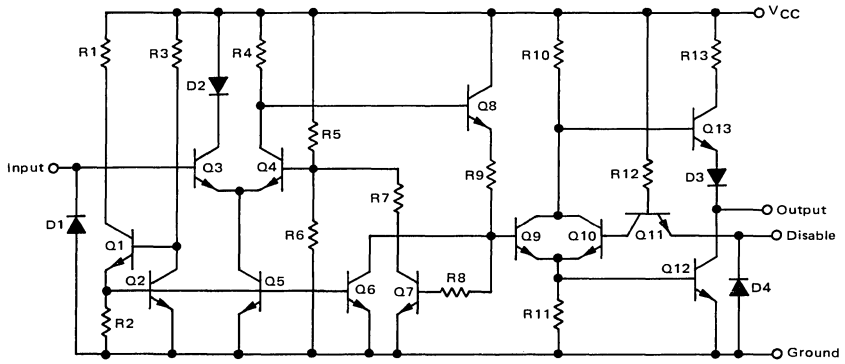


FIGURE 4 — REPRESENTATIVE CIRCUIT SCHEMATIC
(1/6 Shown)



MC3447

BIDIRECTIONAL INSTRUMENTATION BUS (GPIB) TRANSCEIVER

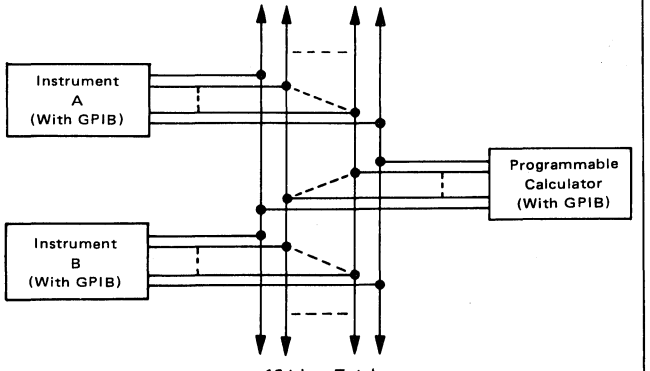
This bidirectional bus transceiver is intended as the interface between TTL or MOS logic and the IEEE Standard Instrumentation Bus (488-1978, often referred to as GPIB). The required bus termination is internally provided.

Low power consumption has been achieved by trading a minimum of speed for low current drain on non-critical channels. A fast channel is provided for critical ATN and EOI paths.

Each driver/receiver pair forms the complete interface between the bus and an instrument. Either the driver or the receiver of each channel is enabled by a Send/Receive input with the disabled output of the pair forced to a high impedance state. The receivers have input hysteresis to improve noise margin, and their input loading follows the bus standard specifications.

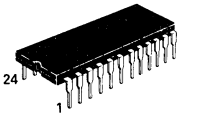
- Low Power —
  Average Power Supply Current = 30 mA Listening
  75 mA Talking
- Eight Driver/Receiver Pairs
- Three-State Outputs
- High Impedance Inputs
- Receiver Hysteresis — 600 mV (Typ)
- Fast Propagation Times — 15–20 ns (Typ)
- TTL Compatible Receiver Outputs
- Single +5 Volt Supply
- Open Collector Driver Output with Terminations
- Power Up/Power Down Protection
  (No Invalid Information Transmitted to Bus)
- No Bus Loading When Power is Removed From Device
- Terminations Provided: Termination Removed When Device is Unpowered

TYPICAL MEASUREMENT SYSTEM APPLICATION

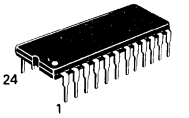


OCTAL BIDIRECTIONAL BUS TRANSCEIVER WITH TERMINATION NETWORKS

SILICON MONOLITHIC INTEGRATED CIRCUIT

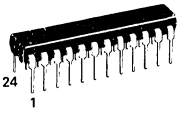


L SUFFIX
CERAMIC PACKAGE
CASE 623

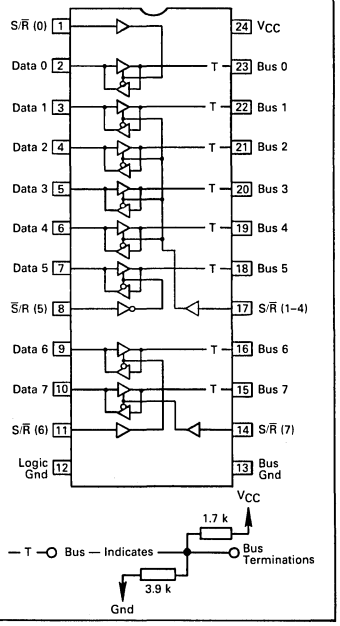


P SUFFIX
PLASTIC PACKAGE
CASE 649

P3 SUFFIX
PLASTIC PACKAGE
CASE 724



PIN CONNECTIONS



MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	7.0	Vdc
Input Voltage	V_I	5.5	Vdc
Driver Output Current	$I_{O(D)}$	150	mA
Junction Temperature	T_J	150	°C
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS

(Unless otherwise noted 4.50 V ≤ V_{CC} ≤ 5.50 V and 0 ≤ T_A ≤ 70°C; typical values are at T_A = 25°C, V_{CC} = 5.0 V)

Characteristic — Note 1	Symbol	Min	Typ	Max	Unit
Bus Voltage					V
(Bus Pin Open) ($V_{I(S/\overline{R})}$ = 0.8 V)	$V_{(Bus)}$	2.5	–	3.7	
($I_{(Bus)}$ = −12 mA)	$V_{IC(Bus)}$	–	–	−1.5	
Bus Current	$I_{(Bus)}$				mA
(5.0 V ≤ $V_{(Bus)}$ ≤ 5.5 V)		0.7	–	2.5	
($V_{(Bus)}$ = 0.5 V)		−1.3	–	−3.2	
(V_{CC} = 0 V, 0 V ≤ $V_{(Bus)}$ ≤ 2.75 V)		–	–	+0.04	
Receiver Input Hysteresis ($V_{I(S/\overline{R})}$ = 0.8 V)	–	400	600	–	mV
Receiver Input Threshold					V
($V_{I(S/\overline{R})}$ = 0.8 V) Low to High	$V_{ILH(R)}$	–	1.6	2.0	
High to Low	$V_{IHL(R)}$	0.8	1.0	–	
Receiver Output Voltage — High Logic State ($V_{I(S/\overline{R})}$ = 0.8 V, $I_{OH(R)}$ = −200 μA, $V_{(Bus)}$ = 2.0 V)	$V_{OH(R)}$	2.4	–	–	V
Receiver Output Voltage — Low Logic State ($V_{I(S/\overline{R})}$ = 0.8 V, $I_{OL(R)}$ = 4.0 mA, $V_{(Bus)}$ = 0.8 V	$V_{OL(R)}$	–	–	0.5	V
Receiver Output Short Circuit Current ($V_{I(S/\overline{R})}$ = 0.8 V, $V_{(Bus)}$ = 2.0 V)	$I_{OS(R)}$	−4.0	–	−20	mA
Driver Input Voltage — High Logic State ($V_{I(S/\overline{R})}$ = 2.0 V)	$V_{IH(D)}$	2.0	–	–	V
Driver Input Voltage — Low Logic State ($V_{I(S/\overline{R})}$ = 2.0 V)	$V_{IL(D)}$	–	–	0.8	V
Driver Input Current — Data Pins ($V_{I(S/\overline{R})}$ = 2.0 V)					μA
(0.5 ≤ $V_{I(D)}$ ≤ 2.7 V)	$I_{I(D)}$	−100	–	40	
($V_{I(D)}$ = 5.5 V)	$I_{IB(D)}$	–	–	200	
Input Current — Send/Receive					μA
(0.5 ≤ $V_{I(S/R)}$ ≤ 2.7 V)	$I_{I(S/\overline{R})}$	−250	–	20	
($V_{I(S/\overline{R})}$ = 5.5 V)	$I_{IB(S/\overline{R})}$	–	–	100	
Driver Input Clamp Voltage ($V_{I(S/\overline{R})}$ = 2.0 V, $I_{IC(D)}$ = −18 mA)	$V_{IC(D)}$	–	–	−1.5	V
Driver Output Voltage — High Logic State ($V_{IS/\overline{R})}$ = 2.0 V, $V_{IH(D)}$ = 2.0 V)	$V_{OH(D)}$	2.5	–	–	V
Driver Output Voltage — Low Logic State (Note 2) ($V_{I(S/\overline{R})}$ = 2.0 V, $V_{IL(D)}$ = 0.8 V, $I_{OL(D)}$ = 48 mA)	$V_{OL(D)}$	–	–	0.5	V
Power Supply Current					mA
(Listening Mode — All Receivers On)	I_{CCL}	–	30	45	
(Talking Mode — All Drivers On)	I_{CCH}	–	75	95	

SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C unless otherwise noted)

Propagation Delay of Driver					ns
(Output Low to High)	$t_{PLH(D)}$	–	7.0	15	
(Output High to Low)	$t_{PHL(D)}$	–	16	30	
Propagation Delay of Receiver (Channels 0 to 5, 7)					ns
(Output Low to High)	$t_{PLH(R)}$	–	28	50	
(Output High to Low)	$t_{PHL(R)}$	–	15	30	
Propagation Delay of Receiver (Channel 6, Note 3)					ns
(Output Low to High)	$t_{PLH(R)}$	–	17	30	
(Output High to Low)	$t_{PHL(R)}$	–	12	22	

NOTES: 1. Specified test conditions for $V_{I(S/\overline{R})}$ are 0.8 V (Low) and 2.0 V (High). Where $V_{I(S/\overline{R})}$ is specified as a test condition, $V_{I(\overline{S}/R)}$ uses the opposite logic levels.
2. The IEEE 488-1979 Bus Standard changes $V_{OL(D)}$ from 0.4 to 0.5 V maximum to permit the use of Schottky technology.
3. In order to meet the IEEE 488-1978 Standard for total system delay on the ATN and EOI channels, a fast receiver has been provided on Channel 6 (Pins 9 and 16).

SWITCHING CHARACTERISTICS (continued) (V_{CC} = 5.0 V, T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Time — Send/Receiver to Data					ns
Logic High to Third State	$t_{PHZ(R)}$	–	15	30	
Third State to Logic High	$t_{PZH(R)}$	–	15	30	
Logic Low to Third State	$t_{PLZ(R)}$	–	15	25	
Third State to Logic Low	$t_{PZL(R)}$	–	10	25	
Propagation Delay Time — Send/Receiver to Bus					ns
Logic Low to Third State	$t_{PLZ(D)}$	–	13	25	
Third State to Logic Low	$t_{PZL(D)}$	–	30	50	

PROPAGATION DELAY TEST CIRCUITS AND WAVEFORMS

FIGURE 1 – BUS INPUT TO DATA OUTPUT (RECEIVER)

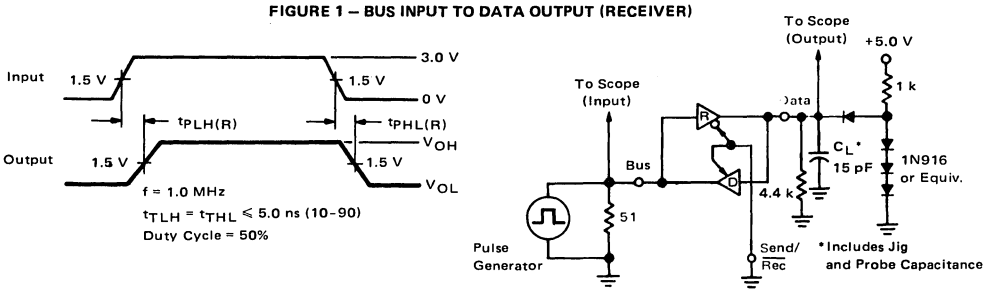


FIGURE 2 – DATA INPUT TO BUS OUTPUT (DRIVER)

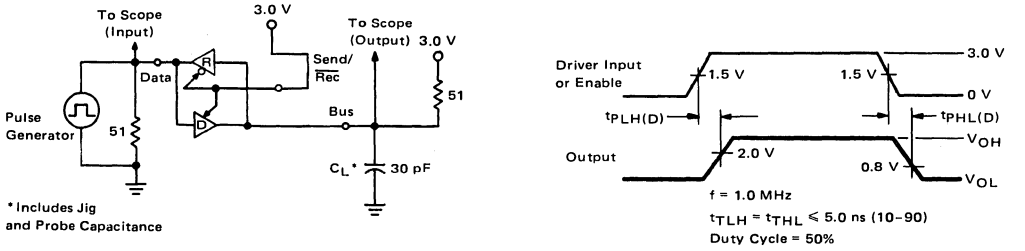
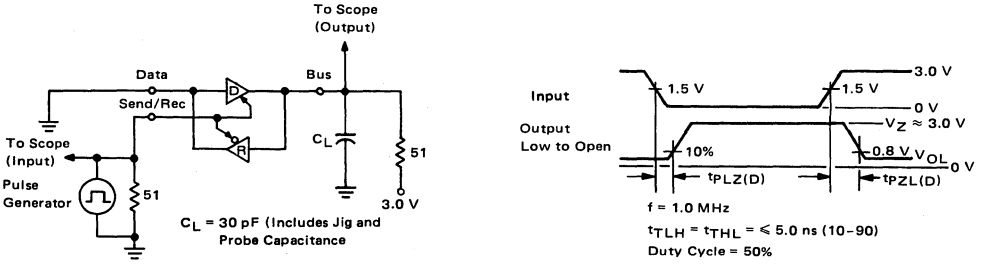


FIGURE 3 – SEND/$\overline{\text{RECEIVE}}$ INPUT TO BUS OUTPUT (DRIVER)



7

FIGURE 4 – SEND/$\overline{\text{RECEIVE}}$ INPUT TO DATA OUTPUT (RECEIVER)

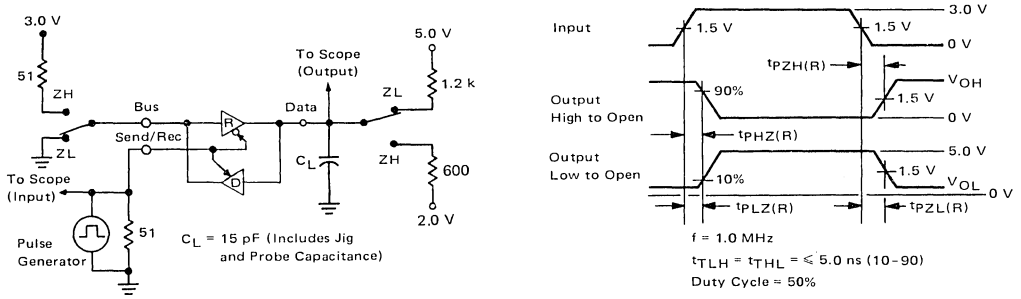


FIGURE 5 – TYPICAL RECEIVER HYSTERESIS CHARACTERISTICS

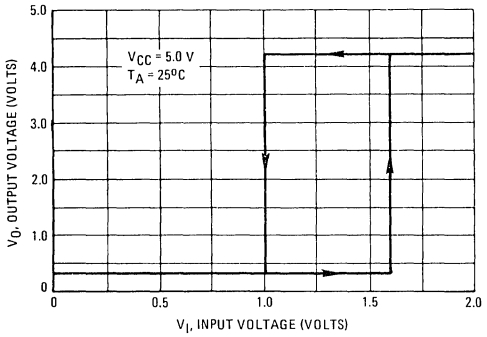


FIGURE 6 – TYPICAL BUS LOAD LINE

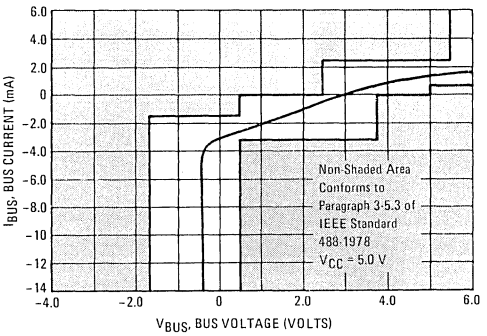


FIGURE 7 – SUGGESTED PRINTED CIRCUIT BOARD LAYOUT USING MC3447s AND MC68488

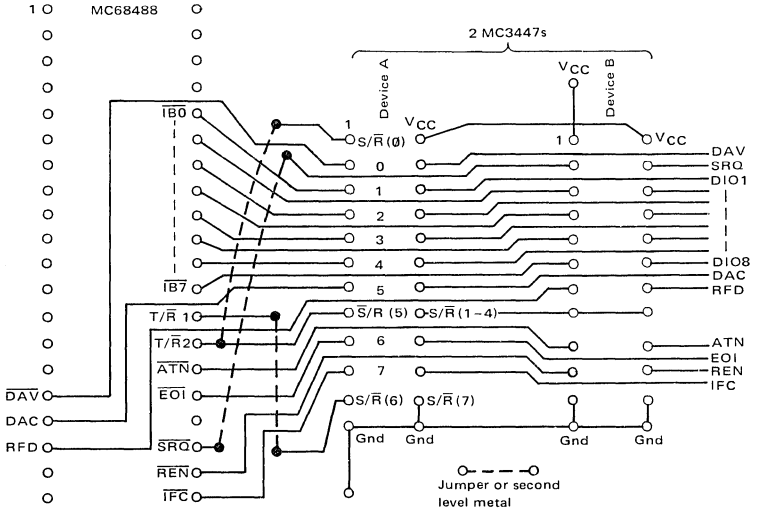
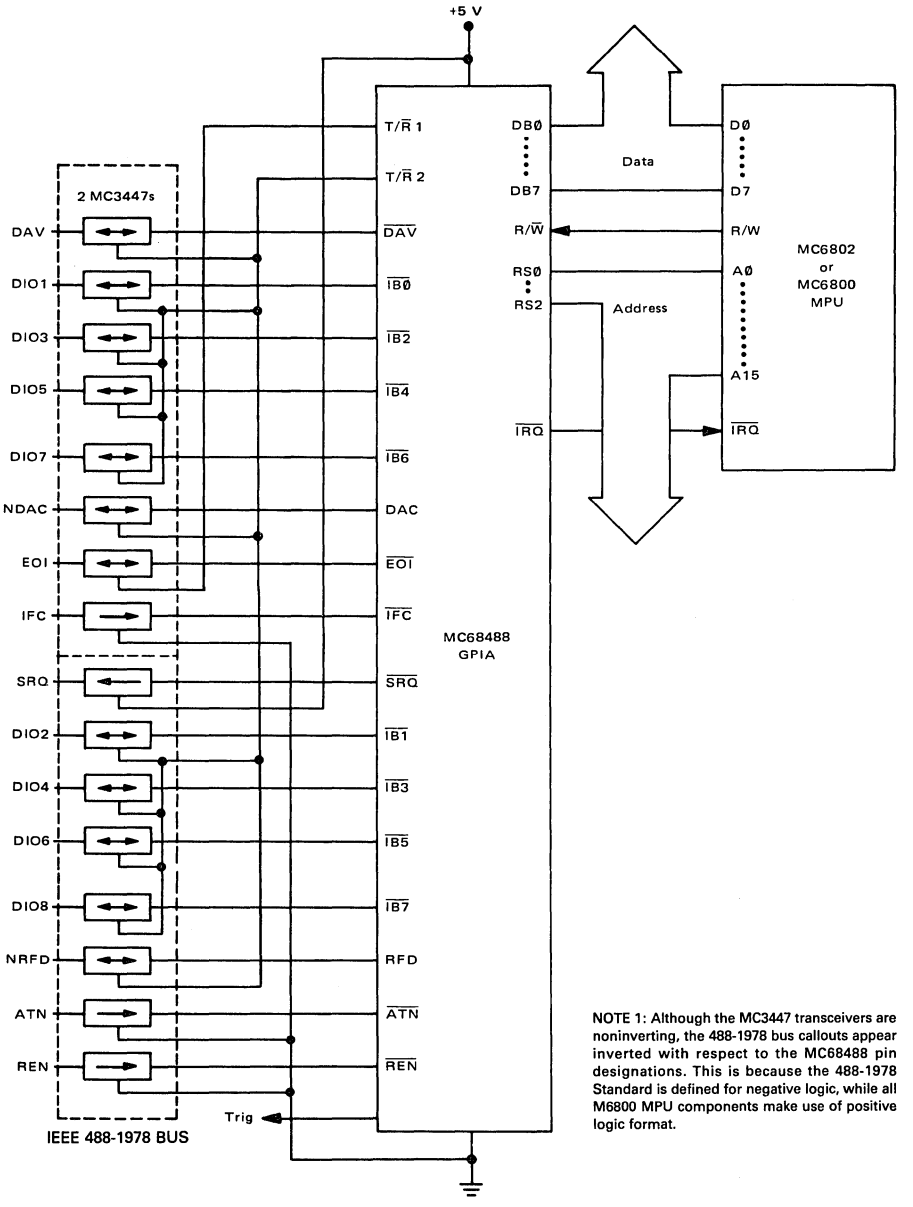


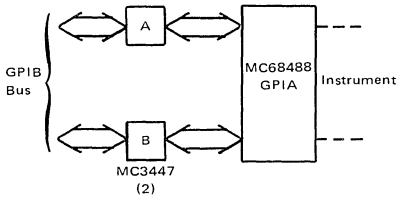
FIGURE 8 – SIMPLE SYSTEM CONFIGURATION



NOTE 1: Although the MC3447 transceivers are noninverting, the 488-1978 bus callouts appear inverted with respect to the MC68488 pin designations. This is because the 488-1978 Standard is defined for negative logic, while all M6800 MPU components make use of positive logic format.

FIGURE 9 – SUGGESTED PIN DESIGNATIONS FOR USE WITH MC68488

MC68488 Connections		MC3447 Pin Designations					MC68488 Connections	
A	B						A	B
T/$\overline{R}$ 2	V_{CC}	S/$\overline{R}$ (0)	1		24	V_{CC}	V_{CC}	V_{CC}
$\overline{DAV}$	$\overline{SRQ}$	Data 0 0	2		23	Bus 0	DAV	SRQ
$\overline{IB0}$	$\overline{IB1}$	Data 1	3		22	Bus 1	DIO 1	DIO 2
$\overline{IB2}$	$\overline{IB3}$	Data 2	4		21	Bus 2	DIO 3	DIO 4
$\overline{IB4}$	$\overline{IB5}$	Data 3	5		20	Bus 3	DIO 5	DIO 6
$\overline{IB6}$	$\overline{IB7}$	Data 4	6	Octal GPIB	19	Bus 4	DIO 7	DIO 8
DAC	RFD	Data 5	7	Transceiver	18	Bus 5	NDAC	NRFD
T/$\overline{R}$ 2	T/$\overline{R}$ 2	S/$\overline{R}$ (5)	8		17	S/$\overline{R}$ (1–4)	T/$\overline{R}$ 2	T/$\overline{R}$ 2
$\overline{EOI}$	$\overline{ATN}$	Data 6	9		16	Bus 6	EOI	ATN
$\overline{IFC}$	$\overline{REN}$	Data 7	10		15	Bus 7	IFC	REN
T/$\overline{R}$ 1	Gnd	S/$\overline{R}$ (6)	11		14	S/$\overline{R}$ (7)	Gnd	Gnd
Gnd	Gnd	Logic Gnd	12		13	Bus Gnd	Gnd	Gnd



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC3448A

BIDIRECTIONAL INSTRUMENTATION BUS (GPIB) TRANSCEIVER

QUAD THREE-STATE BUS TRANSCEIVER WITH TERMINATION NETWORKS

SILICON MONOLITHIC INTEGRATED CIRCUIT

This bidirectional bus transceiver is intended as the interface between TTL or MOS logic and the IEEE Standard Instrumentation Bus (488-1978, often referred to as GPIB). The required bus termination is internally provided.

Each driver/receiver pair forms the complete interface between the bus and an instrument. Either the driver or the receiver of each channel is enabled by its corresponding Send/Receive input with the disabled output of the pair forced to a high impedance state. An additional option allows the driver outputs to be operated in an open collector(1) or active pull-up configuration. The receivers have input hysteresis to improve noise margin, and their input loading follows the bus standard specifications.

- Four Independent Driver/Receiver Pairs
- Three-State Outputs
- High Impedance Inputs
- Receiver Hysteresis — 600 mV (Typ)
- Fast Propagation Times — 15–20 ns (Typ)
- TTL Compatible Receiver Outputs
- Single +5 Volt Supply
- Open Collector Driver Output Option(1)
- Power Up/Power Down Protection
  (No Invalid Information Transmitted to Bus)
- No Bus Loading When Power Is Removed From Device
- Terminations Provided: Termination Removed When Device is Unpowered

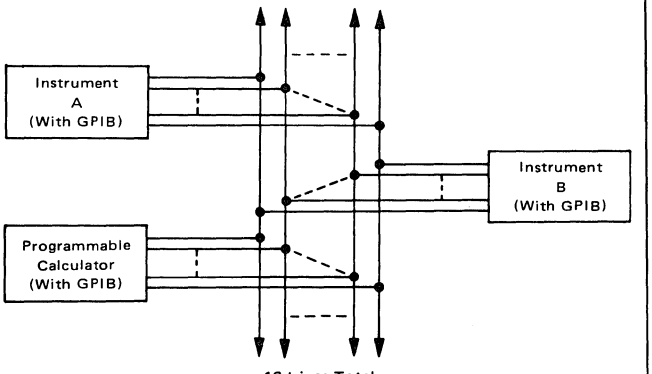
(1) Selection of the "Open Collector" configuration, in fact, selects an open collector device with a passive pull-up load/termination which conforms to Figure 7, IEEE 488-1978 Bus Standard.

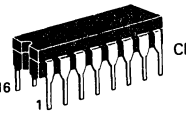
TRUTH TABLE

Send/Rec.	Enable	Info. Flow	Comments
0	X	Bus → Data	—
1	1	Data → Bus	Active Pull-Up
1	0	Data → Bus	Open Col.

X = Don't Care

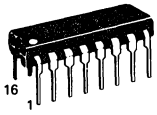
TYPICAL MEASUREMENT SYSTEM APPLICATION





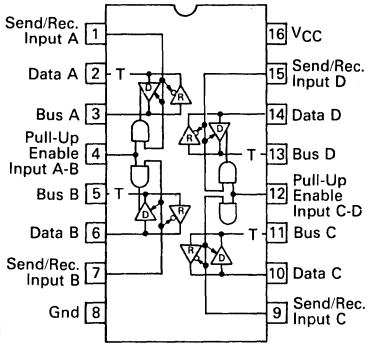
L SUFFIX
CERAMIC PACKAGE
CASE 620

D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO-16)

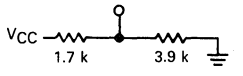


P SUFFIX
PLASTIC PACKAGE
CASE 648

PIN CONNECTIONS



–T– = Bus Termination



MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	7.0	Vdc
Input Voltage	V_I	5.5	Vdc
Driver Output Current	$I_{O(D)}$	150	mA
Junction Temperature	T_J	150	°C
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS

(Unless otherwise noted 4.75 V ≤ V_{CC} ≤ 5.25 V and 0 ≤ T_A ≤ 70°C; typical values are at T_A = 25°C, V_{CC} = 5.0 V)

Characteristic	Symbol	Min	Typ	Max	Unit
Bus Voltage					V
(Bus Pin Open)($V_{I(S/R)}$ = 0.8 V)	$V_{(BUS)}$	2.75	–	3.7	
($I_{(BUS)}$ = -12 mA)	$V_{IC(BUS)}$	–	–	-1.5	
Bus Current	$I_{(BUS)}$				mA
(5.0 V ≤ $V_{(BUS)}$ ≤ 5.5 V)		0.7	–	2.5	
($V_{(BUS)}$ = 0.5 V)		-1.3	–	-3.2	
(V_{CC} = 0 V, 0 V ≤ $V_{(BUS)}$ ≤ 2.75 V)		–	–	+0.04	
Receiver Input Hysteresis ($V_{I(S/R)}$ = 0.8 V)	–	400	600	–	mV
Receiver Input Threshold					V
($V_{I(S/R)}$ = 0.8 V, Low to High)	$V_{ILH(R)}$	–	1.6	1.8	
($V_{I(S/R)}$ = 0.8 V, High to Low)	$V_{IHL(R)}$	0.8	1.0	–	
Receiver Output Voltage — High Logic State ($V_{I(S/R)}$ = 0.8 V, $I_{OH(R)}$ = -800 μA, $V_{(BUS)}$ = 2.0 V)	$V_{OH(R)}$	2.7	–	–	V
Receiver Output Voltage — Low Logic State ($V_{I(S/R)}$ = 0.8 V, $I_{OL(R)}$ = 16 mA, $V_{(BUS)}$ = 0.8 V)	$V_{OL(R)}$	–	–	0.5	V
Receiver Output Short Circuit Current ($V_{I(S/R)}$ = 0.8 V, $V_{(BUS)}$ = 2.0 V)	$I_{OS(R)}$	-15	–	-75	mA
Driver Input Voltage — High Logic State ($V_{I(S/R)}$ = 2.0 V)	$V_{IH(D)}$	2.0	–	–	V
Driver Input Voltage — Low Logic State ($V_{I(S/R)}$ = 2.0 V)	$V_{IL(D)}$	–	–	0.8	V
Driver Input Current — Data Pins ($V_{I(S/R)}$ = $V_{I(E)}$ = 2.0 V)					μA
(0.5 ≤ $V_{I(D)}$ ≤ 2.7 V)	$I_{I(D)}$	-200	–	40	
($V_{I(D)}$ = 5.5 V)	$I_{IB(D)}$	–	–	200	
Input Current — Send/Receive					μA
(0.5 ≤ $V_{I(S/R)}$ ≤ 2.7 V)	$I_{I(S/R)}$	-100	–	20	
($V_{I(S/R)}$ = 5.5 V)	$I_{IB(S/R)}$	–	–	100	
Input Current — Enable					μA
(0.5 ≤ $V_{I(E)}$ ≤ 2.7 V)	$I_{I(E)}$	-200	–	20	
($V_{I(E)}$ = 5.5 V)	$I_{IB(E)}$	–	–	100	
Driver Input Clamp Voltage ($V_{I(S/R)}$ = 2.0 V, $I_{IC(D)}$ = -18 mA)	$V_{IC(D)}$	–	–	-1.5	V
Driver Output Voltage — High Logic State ($V_{I(S/R)}$ = 2.0 V, $V_{IH(D)}$ = 2.0 V, $V_{IH(E)}$ = 2.0 V, I_{OH} = -5.2 mA)	$V_{OH(D)}$	2.5	–	–	V
Driver Output Voltage — Low Logic State (Note 1) ($V_{I(S/R)}$ = 2.0 V, $I_{OL(D)}$ = 48 mA)	$V_{OL(D)}$	–	–	0.5	V
Output Short Circuit Current ($V_{I(S/R)}$ = 2.0 V, $V_{IH(D)}$ = 2.0 V, $V_{IH(E)}$ = 2.0 V)	$I_{OS(D)}$	-30	–	-120	mA
Power Supply Current					mA
(Listening Mode — All Receivers On)	I_{CCL}	–	63	85	
(Talking Mode — All Drivers On)	I_{CCH}	–	106	125	

SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C unless otherwise noted)

Propagation Delay of Driver					ns
(Output Low to High)	$t_{PLH(D)}$	–	–	15	
(Output High to Low)	$t_{PHL(D)}$	–	–	17	
Propagation Delay of Receiver					ns
(Output Low to High)	$t_{PLH(R)}$	–	–	25	
(Output High to Low)	$t_{PHL(R)}$	–	–	23	

NOTE 1. A modification of the IEEE 488-1978 Bus Standard changes $V_{OL(D)}$ from 0.4 to 0.5 V maximum to permit the use of Schottky technology.

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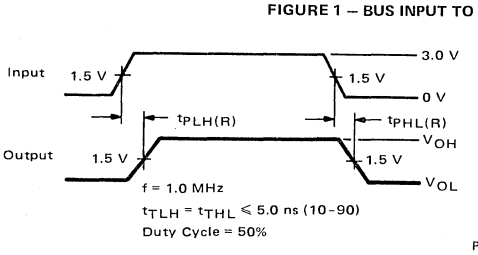
SWITCHING CHARACTERISTICS (continued) (V_{CC} = 5.0 V, T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Time — Send/Receive to Data					ns
Logic High to Third State	$t_{PHZ(R)}$	—	—	30	
Third State to Logic High	$t_{PZH(R)}$	—	—	30	
Logic Low to Third State	$t_{PLZ(R)}$	—	—	30	
Third State to Logic Low	$t_{PZL(R)}$	—	—	30	
Propagation Delay Time — Send/Receive to Bus					ns
Logic High to Third State	$t_{PHZ(D)}$	—	—	30	
Third State to Logic High	$t_{PZH(D)}$	—	—	30	
Logic Low to Third State	$t_{PLZ(D)}$	—	—	30	
Third State to Logic Low	$t_{PZL(D)}$	—	—	30	
Turn-On Time — Enable to Bus					ns
Pull-Up Enable to Open Collector	$t_{POFF(E)}$	—	—	30	
Open Collector to Pull-Up Enable	$t_{PON(E)}$	—	—	20	

PROPAGATION DELAY TEST CIRCUITS AND WAVEFORMS

FIGURE 1 — BUS INPUT TO DATA OUTPUT (RECEIVER)



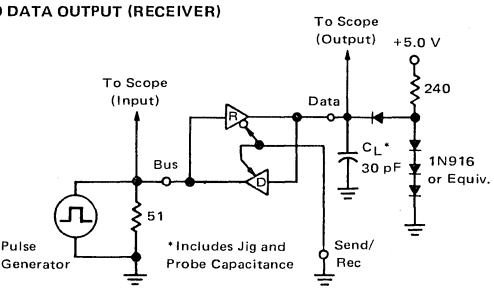
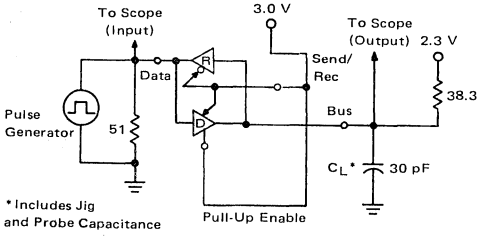


FIGURE 2 — DATA INPUT TO BUS OUTPUT (DRIVER)



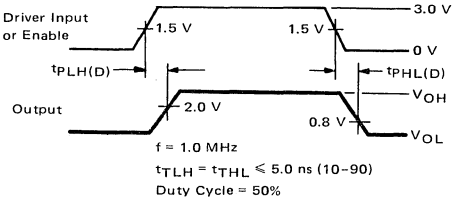
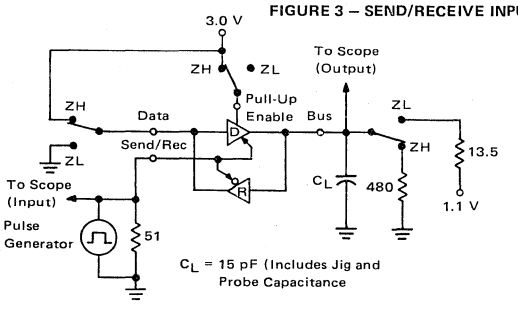


FIGURE 3 — SEND/RECEIVE INPUT TO BUS OUTPUT (DRIVER)



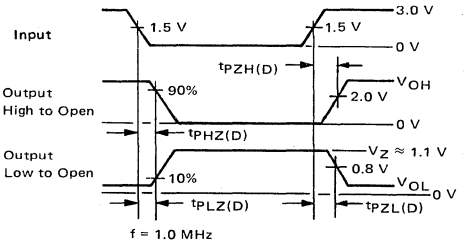


FIGURE 4 – SEND/RECEIVE INPUT TO DATA OUTPUT (RECEIVER)

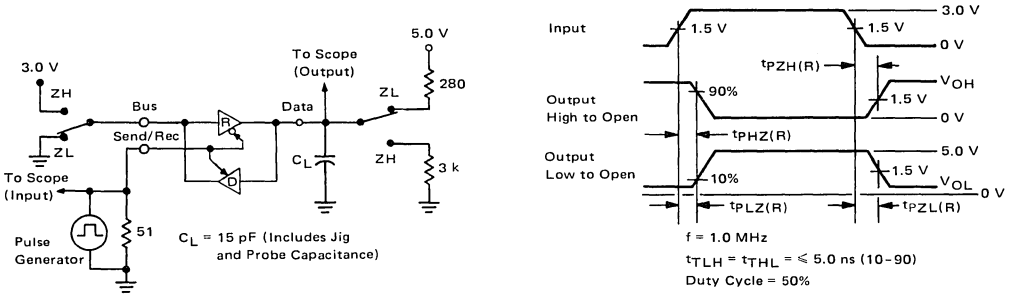


FIGURE 5 – ENABLE INPUT TO BUS OUTPUT (DRIVER)

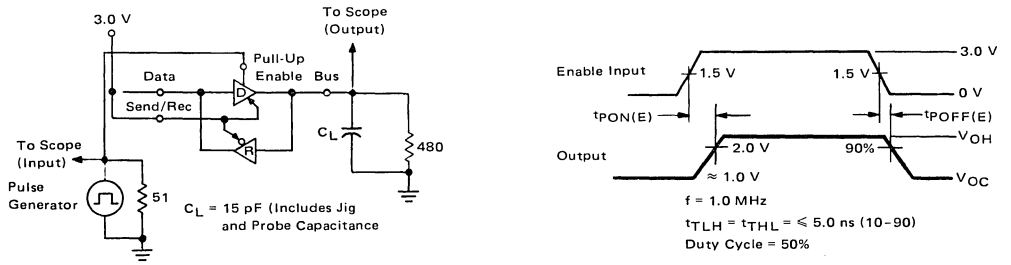


FIGURE 6 – TYPICAL RECEIVER HYSTERESIS CHARACTERISTICS

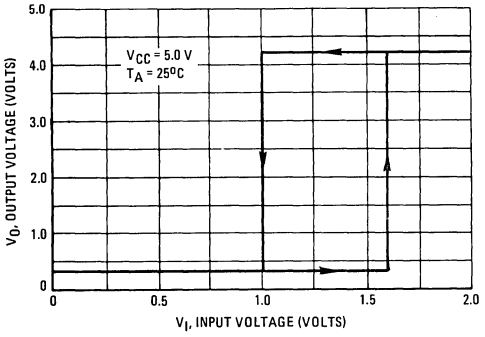


FIGURE 7 – TYPICAL BUS LOAD LINE

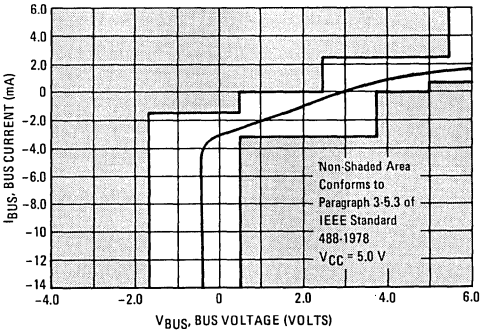
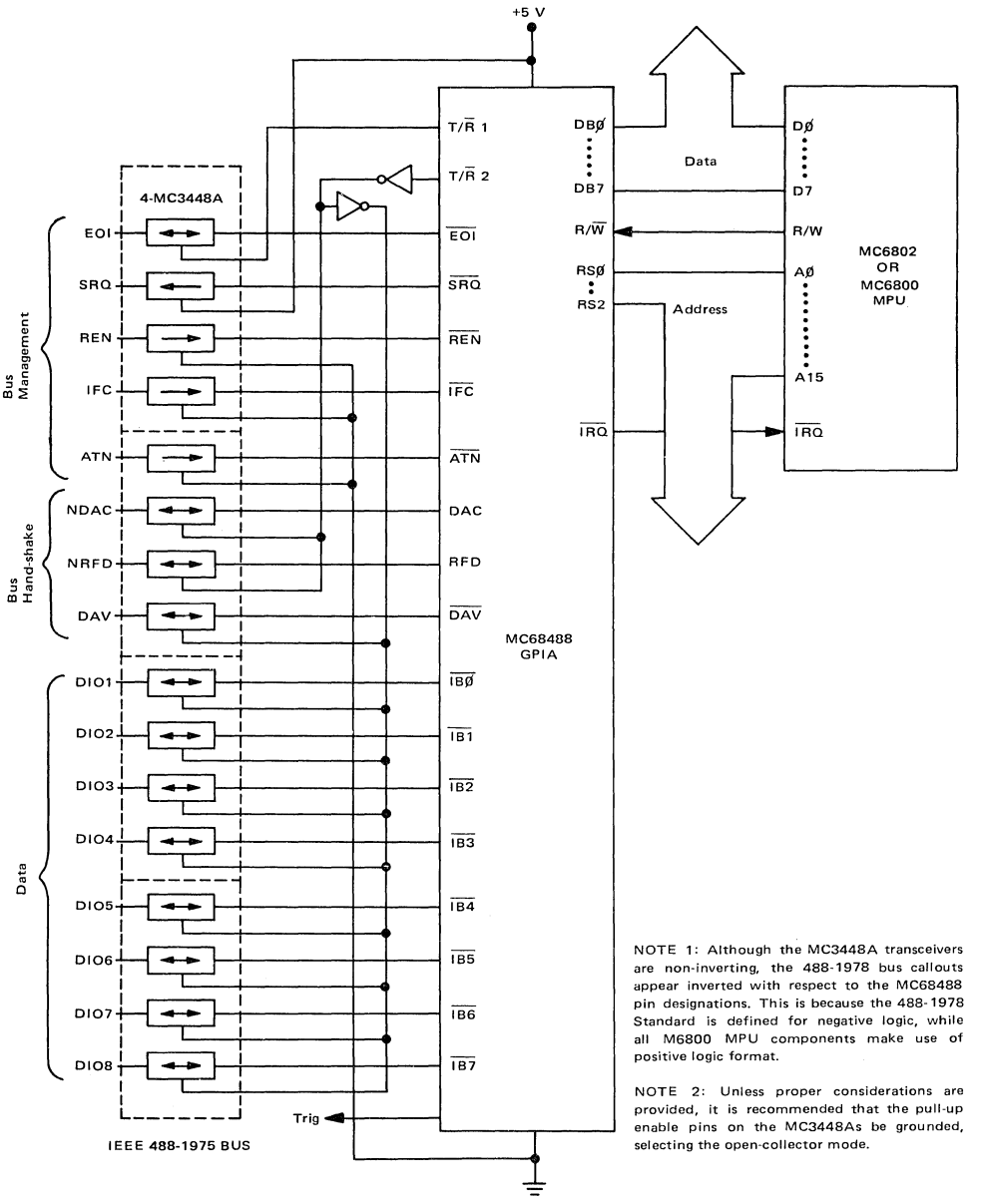


FIGURE 8 – SIMPLE SYSTEM CONFIGURATION



NOTE 1: Although the MC3448A transceivers are non-inverting, the 488-1978 bus callouts appear inverted with respect to the MC68488 pin designations. This is because the 488-1978 Standard is defined for negative logic, while all M6800 MPU components make use of positive logic format.

NOTE 2: Unless proper considerations are provided, it is recommended that the pull-up enable pins on the MC3448As be grounded, selecting the open-collector mode.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC3450
MC3452

QUAD LINE RECEIVERS WITH COMMON THREE-STATE STROBE INPUT

SILICON MONOLITHIC INTEGRATED CIRCUITS

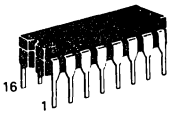
QUAD MTTL COMPATIBLE LINE RECEIVERS

The MC3450 features four MC75107 type active pullup line receivers with the addition of a common three-state strobe input. When the strobe input is at a logic zero, each receiver output state is determined by the differential voltage across its respective inputs. With the strobe high, the receiver outputs are in the high impedance state.

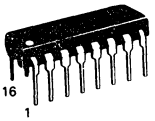
The MC3452 is the same as the MC3450 except that the outputs are open collector which permits the implied "AND" function.

The strobe input on both devices is buffered to present a strobe loading factor of only one for all four receivers and inverted to provide best compatability with standard decoder devices.

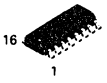
- Receiver Performance Identical to the Popular MC75107/MC75108 Series
- Four Independent Receivers with Common Strobe Input
- Implied "AND" Capability with Open Collector Outputs
- Useful as a Quad 1103 type Memory Sense Amplifier



L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648



D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO-16)

PIN CONNECTIONS

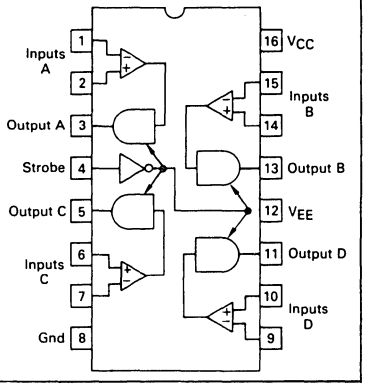
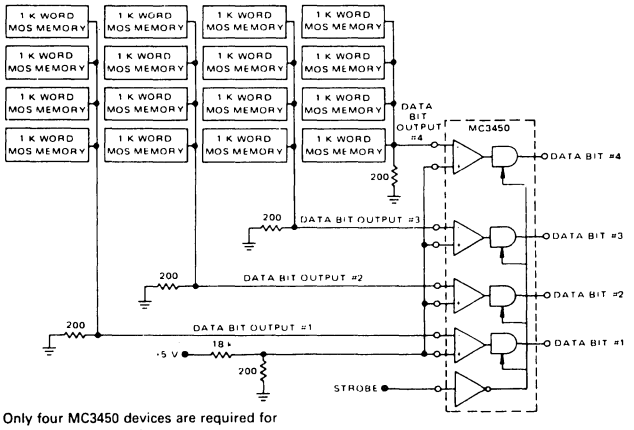


FIGURE 1 — A TYPICAL MOS MEMORY SENSING APPLICATION FOR A 4 k WORD BY 4-BIT MEMORY ARRANGEMENT EMPLOYING 1103 TYPE MEMORY DEVICES



Only four MC3450 devices are required for a 4 k word by 16-bit memory system.

TRUTH TABLE

Input	Strobe	Output MC3450	Output MC3452
$V_{ID} \geq +25$ mV	L	H	Off
	H	Z	Off
-25 mV $\leq V_{ID} \leq +25$ mV	L	I	I
	H	Z	Off
$V_{ID} \leq -25$ mV	L	L	L
	H	Z	Off

L = Low Logic State
H = High Logic State
Z = Third (High Impedance) State
I = Indeterminate State

MAXIMUM RATINGS (T_A = 0 to +70°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltages	V_{CC}, V_{EE}	±7.0	Vdc
Differential Mode Input Signal Voltage Range	V_{IDR}	±6.0	Vdc
Common Mode Input Voltage Range	V_{ICR}	±5.0	Vdc
Strobe Input Voltage	$V_{I(S)}$	5.5	Vdc
Power Dissipation (Package Limitation) Ceramic Dual In-Line Package Derate above T_A = +25°C Plastic Dual In-Line Package Derate above T_A = +25°C	P_D	 1000 6.6 1000 6.6	 mW mW/°C mW mW/°C
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Voltages	V_{CC} V_{EE}	+4.75 -4.75	+5.0 -5.0	+5.25 -5.25	Vdc
Output Load Current	I_{OL}	–	–	16	mA
Differential Mode Input Voltage Range	V_{IDR}	-5.0	–	+5.0	Vdc
Common Mode Input Voltage Range	V_{ICR}	-3.0	–	+3.0	Vdc
Input Voltage Range (any input to Ground)	V_{IR}	-5.0	–	+3.0	Vdc

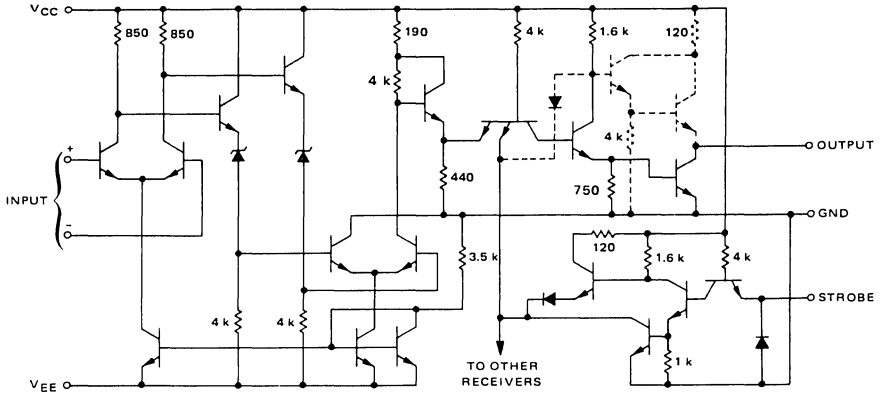
ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 Vdc, V_{EE} = -5.0 Vdc, T_A = 0 to +70°C unless otherwise noted.)

Characteristic	Symbol	Fig.	MC3450			MC3452			Unit
			Min	Typ	Max	Min	Typ	Max	
High Level Input Current to Receiver Input	$I_{IH(I)}$	7	–	–	75	–	–	75	μA
Low Level Input Current to Receiver Input	$I_{IL(I)}$	8	–	–	-10	–	–	-10	μA
High Level Input Current to Strobe Input $V_{IH(S)}$ = +2.4 V $V_{IH(S)}$ = +5.25 V	$I_{IH(S)}$	5	 – –	 – –	 40 1.0	 – –	 – –	 40 1.0	 μA mA
Low Level Input Current to Strobe Input $V_{IL(S)}$ +0.4 V	$I_{IL(S)}$	5	–	–	-1.6	–	–	-1.6	mA
High Level Output Voltage	V_{OH}	3	2.4	–	–	–	–	–	Vdc
High Level Output Leakage Current	I_{CEX}	3	–	–	–	–	–	250	μA
Low Level Output Voltage	V_{OL}	3	–	–	0.5	–	–	0.5	Vdc
Short-Circuit Output Current	I_{OS}	6	-18	–	-70	–	–	–	mA
Output Disable Leakage Current	I_{off}	9	–	–	40	–	–	–	μA
High Logic Level Supply Current from V_{CC}	I_{CCH}	4	–	45	60	–	45	60	mA
High Logic Level Supply Current from V_{EE}	I_{EEH}	4	–	-17	-30	–	-17	-30	mA

SWITCHING CHARACTERISTICS (V_{CC} = +5.0 Vdc, V_{EE} = -5.0 Vdc, T_A = +25°C unless otherwise noted.)

Characteristic	Symbol	Fig.	MC3450			MC3452			Unit
			Min	Typ	Max	Min	Typ	Max	
High to Low Logic Level Propagation Delay Time (Differential Inputs)	$t_{PHL(D)}$	10	–	–	25	–	–	25	ns
Low to High Logic Level Propagation Delay Time (Differential Inputs)	$t_{PLH(D)}$	10	–	–	25	–	–	25	ns
Open State to High Logic Level Propagation Delay Time (Strobe)	$t_{PZH(S)}$	11	–	–	21	–	–	–	ns
High Logic Level to Open State Propagation Delay Time (Strobe)	$t_{PHZ(S)}$	11	–	–	18	–	–	–	ns
Open State to Low Logic Level Propagation Delay Time (Strobe)	$t_{PZL(S)}$	11	–	–	27	–	–	–	ns
Low Logic Level to Open State Propagation Delay Time (Strobe)	$t_{PLZ(S)}$	11	–	–	29	–	–	–	ns
High Logic to Low Logic Level Propagation Delay Time (Strobe)	$t_{PHL(S)}$	12	–	–	–	–	–	25	ns
Low Logic to High Logic Level Propagation Delay Time (Strobe)	$t_{PLH(S)}$	12	–	–	–	–	–	25	ns

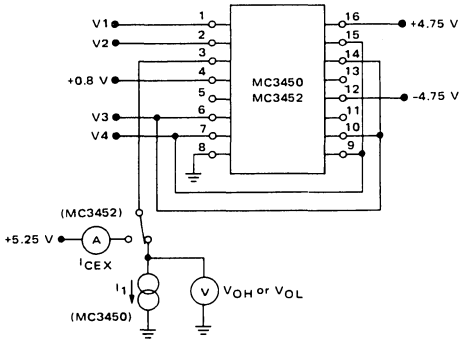
FIGURE 2 – CIRCUIT SCHEMATIC
(1/4 Circuit Shown)



Dashed components apply to the MC3450 circuit only.

TEST CIRCUITS

FIGURE 3 – I_{CEX}, V_{OH}, AND V_{OL}



TEST TABLE

	V1		V2		V3		V4		
	MC3450	MC3452	MC3450	MC3452	MC3450	MC3452	MC3450	MC3452	I1
V_{OH}	+2.975 V	-	+3.0 V	-	+3.0 V	-	GND	-	+0.4 mA
	-3.0 V	-	-2.975 V	-	GND	-	-3.0 V	-	
I_{CEX}		+2.975 V	-	+3.0 V	-	+3.0 V	-	GND	-
		-3.0 V		-2.975 V		GND	-	-3.0 V	-
V_{OL}	+3.0 V	+3.0 V	+2.975 V	+2.975 V	GND	GND	+3.0 V	+3.0 V	-16 mA
	-2.975 V	-2.975 V	-3.0 V	-3.0 V	-3.0 V	-3.0 V	GND	GND	

Channel A shown under test. Other channels are tested similarly.

FIGURE 4 – I_{CCH} AND I_{EEH}

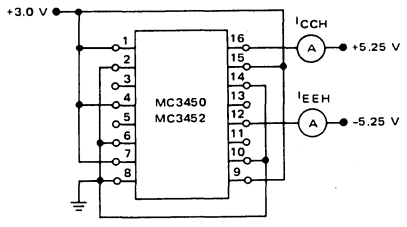
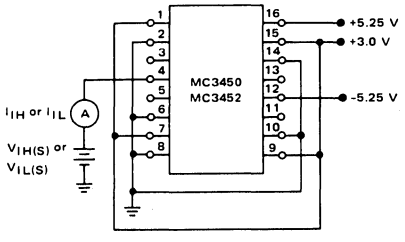
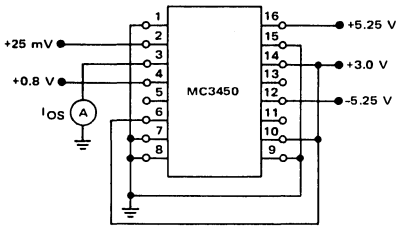


FIGURE 5 – $I_{IH(S)}$ AND $I_{IL(S)}$



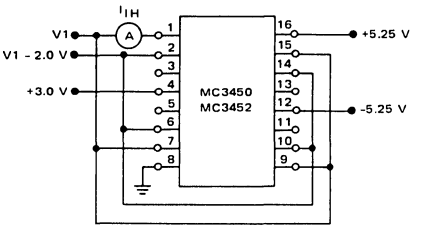
TEST CIRCUITS (continued)

FIGURE 6 – I_{OS}



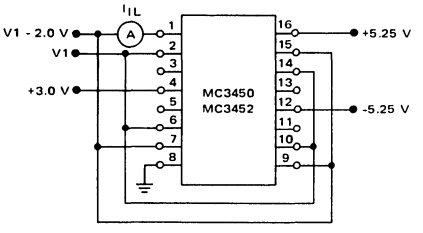
Channel A shown under test, other channels are tested similarly.
Only one output shorted at a time.

FIGURE 7 – I_{IH}



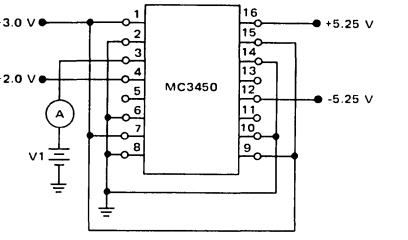
Channel A(-) shown under test, other channels are tested similarly. Devices are tested with V1 from +3.0 V to –3.0 V.

FIGURE 8 – I_{IL}



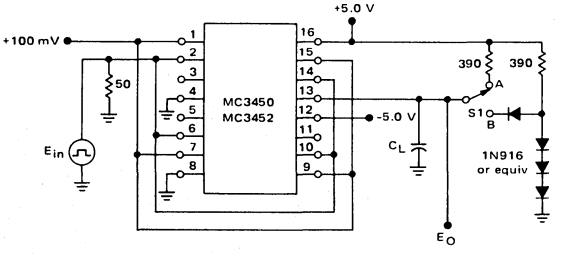
Channel A(-) shown under test, other channels are tested similarly. Devices are tested with V1 from +3.0 V to -3.0 V.

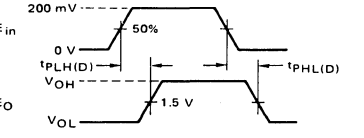
FIGURE 9 – I_{off}



Output of Channel A shown under test, other outputs are tested similarly for V1 = 0.4 V and +2.4 V.

FIGURE 10 – RECEIVER PROPAGATION DELAY $t_{PLH(D)}$ AND $t_{PHL(D)}$





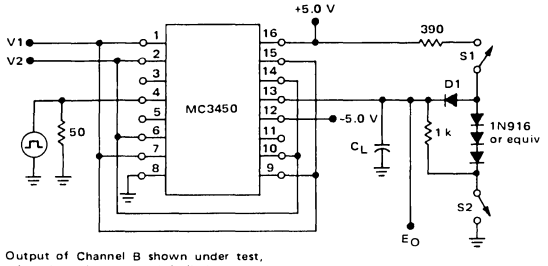
Output of Channel B shown under test, other channels are tested similarly.

S1 at "A" for MC3452
S1 at "B" for MC3450
C_L = 15 pF total for MC3452
C_L = 50 pF total for MC3450

E_{in} waveform characteristics:
t_{TLH} and $t_{THL} \leqslant 10$ ns measured 10% to 90%
PRR = 1.0 MHz
Duty Cycle = 500 ns

TEST CIRCUITS (continued)

FIGURE 11 – STROBE PROPAGATION DELAY TIMES $t_{PLZ(S)}$; $t_{PZL(S)}$ $t_{PHZ(S)}$ and $t_{PZH(S)}$



Output of Channel B shown under test, other channels are tested similarly.

	V1	V2	S1	S2	C_L
$t_{PLZ(S)}$	100 mV	GND	Closed	Closed	15 pF
$t_{PZL(S)}$	100 mV	GND	Closed	Open	50 pF
$t_{PHZ(S)}$	GND	100 mV	Closed	Closed	15 pF
$t_{PZH(S)}$	GND	100 mV	Open	Closed	50 pF

C_L includes jig and probe capacitance.
E_{in} waveform characteristics:
t_{TLH} and $t_{THL} \leq 10$ ns measured 10% to 90%.
PRR = 1.0 MHz
Duty Cycle = 50%

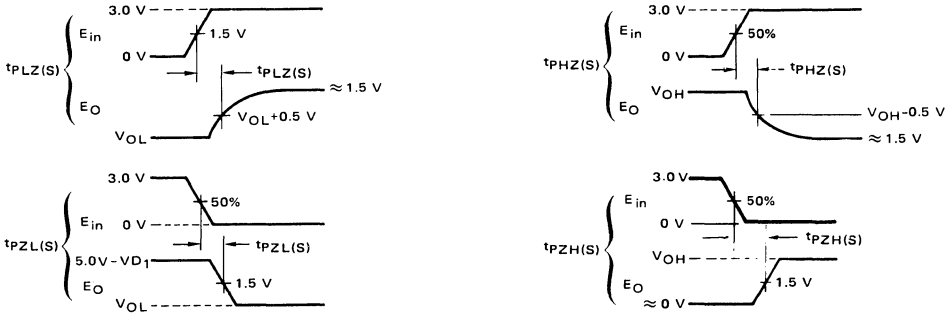
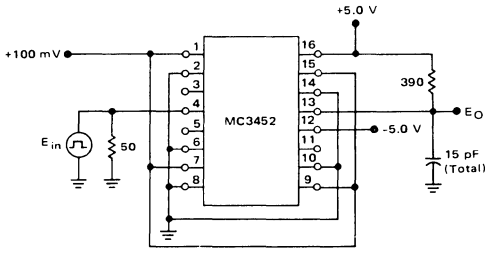
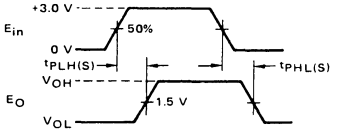


FIGURE 12 – STROBE PROPAGATION DELAY $t_{PLH(S)}$ AND $t_{PHL(S)}$



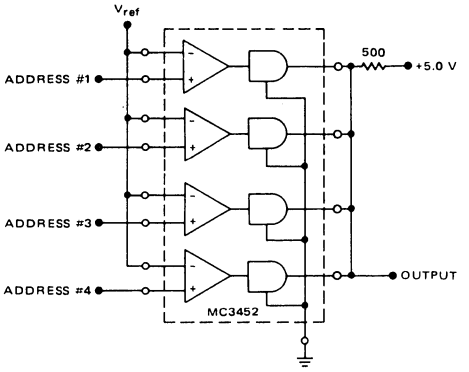
Output of Channel B shown under test, other channels are tested similarly.



E_{in} waveform characteristics:
t_{TLH} and $t_{THL} \leq 10$ ns measured 10% to 90%
PRR = 1.0 MHz
Duty Cycle = 500 ns

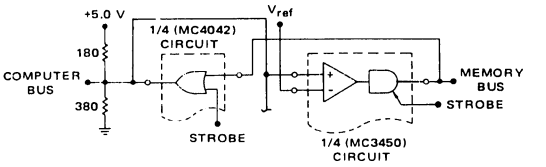
APPLICATIONS INFORMATION

FIGURE 13 – IMPLIED "AND" GATING



The MC3452 can be used for address decoding as illustrated above. All outputs of the MC3452 are tied together through a common resistor to +5.0 volts. In this configuration the MC3452 provides the "AND" function. All addresses have to be true before the output will go high. This scheme eliminates the need for an "AND" gate and enhances speed throughput for address decoding.

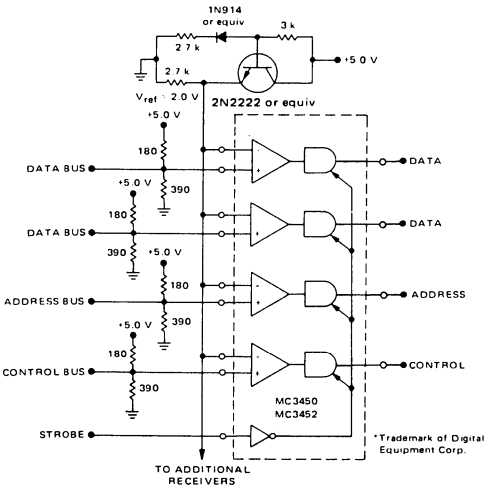
FIGURE 14 – BIDIRECTIONAL DATA TRANSMISSION



The three-state capability of the MC3450 permits bidirectional data transmission as illustrated.

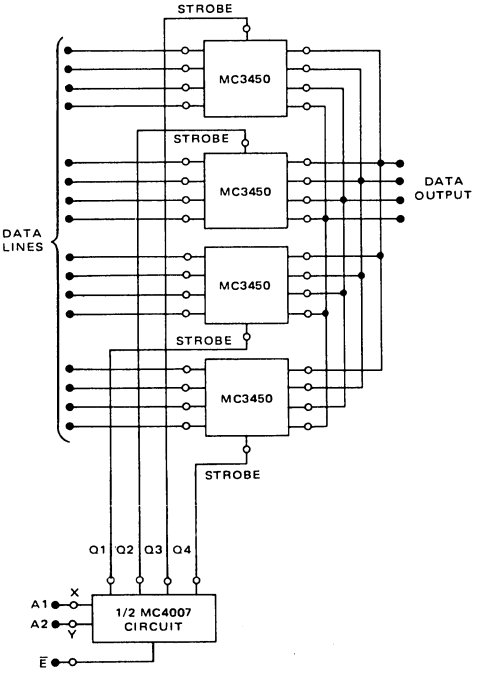
7

FIGURE 15 – SINGLE-ENDED UNI-BUS* LINE RECEIVER APPLICATION FOR MINICOMPUTERS



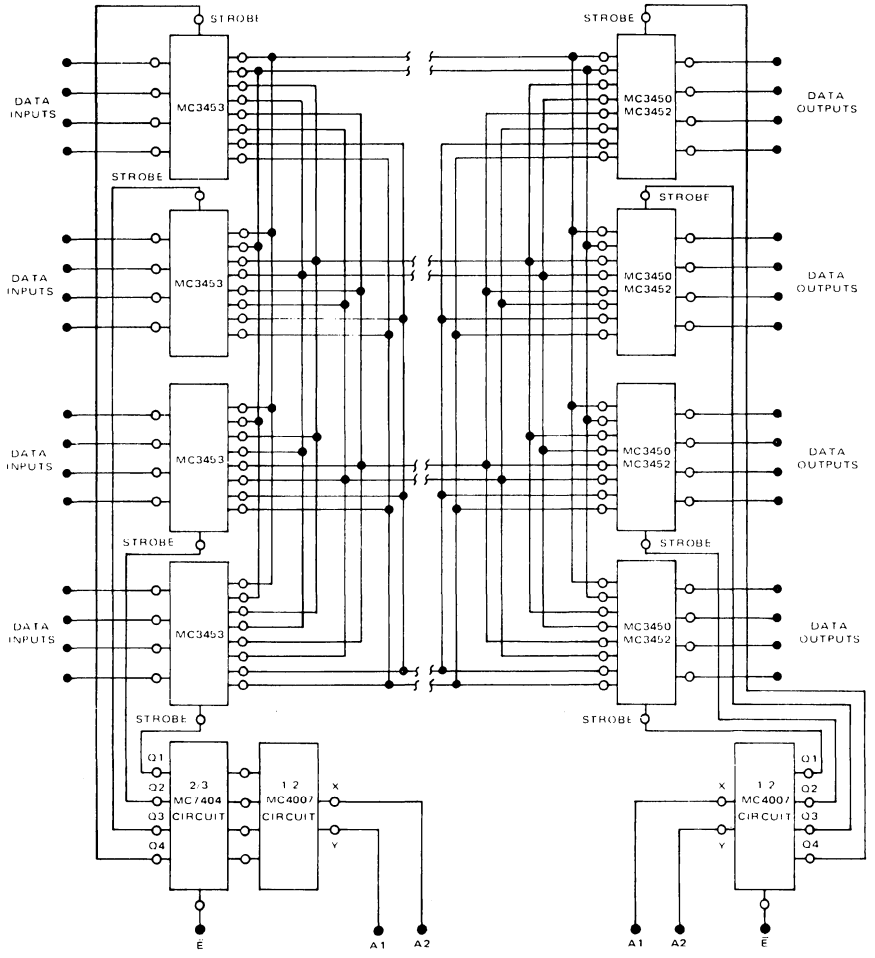
The MC3450/3452 can be used for single-ended as well as differential line receiving. For single-ended line receiver applications, such as are encountered in minicomputers, the configuration shown in Figure 15 can be used. The voltage source, which generates V_{ref}, should be designed so that the V_{ref} voltage is halfway between V_{OH}(min) and V_{OL}(max). The maximum input overdrive required to guarantee a given logic state is extremely small, 25 mV maximum. This low-input overdrive enhances differential noise immunity. Also the high-input impedance of the line receiver permits many receivers to be placed on a single line with minimum load effects.

FIGURE 16 – WIRED "OR" DATA SELECTION USING THREE-STATE LOGIC



APPLICATIONS INFORMATION (continued)

FIGURE 17 – PARTY-LINE DATA TRANSMISSION SYSTEM WITH MULTIPLEX DECODING



MC3453

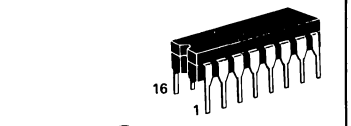
QUAD LINE DRIVER WITH COMMON INHIBIT INPUT

SILICON MONOLITHIC INTEGRATED CIRCUIT

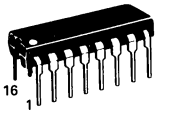
MTTL COMPATIBLE QUAD LINE DRIVER

The MC3453 features four SN75110 type line drivers with a common inhibit input. When the inhibit input is high, a constant output current is switched between each pair of output terminals in response to the logic level at that channel's input. When the inhibit is low, all channel outputs are nonconductive (transistors biased to cut-off). This minimizes loading in party-line systems where a large number of drivers share the same line.

- Four Independent Drivers with Common Inhibit Input
- −3.0 Volts Output Common-Mode Voltage Over Entire Operating Range
- Improved Driver Design Exceeds Performance of Popular SN75110

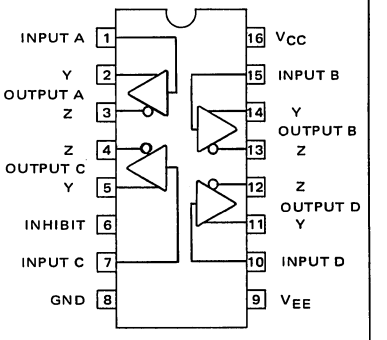


L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

PIN CONNECTIONS

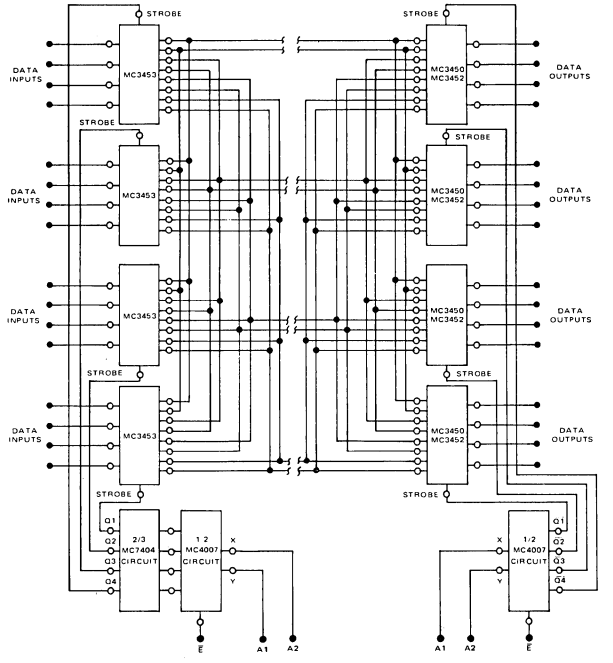


TRUTH TABLE
(positive logic)

Logic Input	Inhibit Input	Output Current	
		Z	Y
H	H	On	Off
L	H	Off	On
H	L	Off	Off
L	L	Off	Off

L = Low Logic Level
H = High Logic Level

FIGURE 1 – PARTY-LINE DATA TRANSMISSION SYSTEM WITH MULTIPLEX DECODING



MAXIMUM RATINGS (T_A = 0 to +70°C unless otherwise noted.)

	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+7.0 -7.0	Volts
Logic and Inhibitor Input Voltages	V_{in}	5.5	Volts
Common-Mode Output Voltage Range	V_{OCR}	-5.0 to +12	Volts
Power Dissipation (Package Limitation) Plastic and Ceramic Dual In-Line Packages Derate above T_A = +25°C	P_D	 1000 6.6	 mW mW/°C
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range Plastic and Ceramic Dual In-Line Packages	T_{stg}	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS (See Notes 1 and 2.)

Characteristic	Symbol	Min	Nom	Max	Unit
Power Supply Voltages	V_{CC} V_{EE}	+4.75 -4.75	+5.0 -5.0	+5.25 -5.25	Volts
Common-Mode Output Voltage Range Positive Negative	V_{OCR}	 0 0	 – –	 +10 -3.0	Volts

Notes: 1. These voltage values are in respect to the ground terminal.
2. When not using all four channels, unused outputs **must** be grounded.

DEFINITIONS OF INPUT LOGIC LEVELS*

Characteristic	Symbol	Min	Max	Unit
High-Level Input Voltage (at any input)	V_{IH}	2.0	5.5	Volts
Low-Level Input Voltage (at any input)	V_{IL}	0	0.8	Volts

*The algebraic convention, where the most positive limit is designated maximum, is used with Logic Level Input Voltage Levels only.

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ELECTRICAL CHARACTERISTICS (T_A = 0 to +70°C unless otherwise noted.)

Characteristic##	Symbol	Min	Typ#	Max	Unit
High-Level Input Current (Logic Inputs) (V_{CC} = Max, V_{EE} = Max, V_{IH_L} = 2.4 V) (V_{CC} = Max, V_{EE} = Max, V_{IH_L} = V_{CC} Max)	I_{IH_L}	 – –	 – –	 40 1.0	 µA mA
Low-Level Input Current (Logic Inputs) (V_{CC} = Max, V_{EE} = Max, V_{IL_L} = 0.4 V)	I_{IL_L}	–	–	-1.6	mA
High-Level Input Current (Inhibit Input) (V_{CC} = Max, V_{EE} = Max, V_{IH_I} = 2.4 V) (V_{CC} = Max, V_{EE} = Max, V_{IH_I} = V_{CC} Max)	I_{IH_I}	 – –	 – –	 40 1.0	 µA mA
Low-Level Input Current (Inhibit Input) (V_{CC} = Max, V_{EE} = Max, V_{IL_I} = 0.4 V)	I_{IL_I}	–	–	-1.6	mA
Output Current ("on" state) (V_{CC} = Max, V_{EE} = Max) (V_{CC} = Min, V_{EE} = Min)	$I_{O(on)}$	 – 6.5	 11 11	 15 –	mA
Output Current ("off" state) (V_{CC} = Min, V_{EE} = Min)	$I_{O(off)}$	–	5.0	100	µA
Supply Current from V_{CC} (with driver enabled) (V_{IL_L} = 0.4 V, V_{IH_I} = 2.0 V)	$I_{CC(on)}$	–	35	50	mA
Supply Current from V_{EE} (with driver enabled) (V_{IL_L} = 0.4 V, V_{IH_I} = 2.0 V)	$I_{EE(on)}$	–	65	90	mA
Supply Current from V_{CC} (with driver inhibited) (V_{IL_L} = 0.4 V, V_{IL_I} = 0.4 V)	$I_{CC(off)}$	–	35	50	mA
Supply Current from V_{EE} (with driver inhibited) (V_{IL_L} = 0.4 V, V_{IL_I} = 0.4 V)	$I_{EE(off)}$	–	25	40	mA

#All typical values are at V_{CC} = +5.0 V, V_{EE} = -5.0 V, T_A = +25°C.
##For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable device type.
Ground unused inputs and outputs.

SWITCHING CHARACTERISTICS (V_{CC} = +5.0 V, V_{EE} = -5.0 V, T_A = +25°C.)

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Time from Logic Input to Output Y or Z (R_L = 50 ohms, C_L = 40 pF)	t_{PLH_L}	–	9.0	17	ns
	t_{PHL_L}	–	9.0	17	
Propagation Delay Time from Inhibit Input to Output Y or Z (R_L = 50 ohms, C_L = 40 pF)	t_{PLH_I}	–	16	25	ns
	t_{PHL_I}	–	20	25	

FIGURE 2 – LOGIC INPUT TO OUTPUTS PROPAGATION DELAY TIME WAVEFORMS

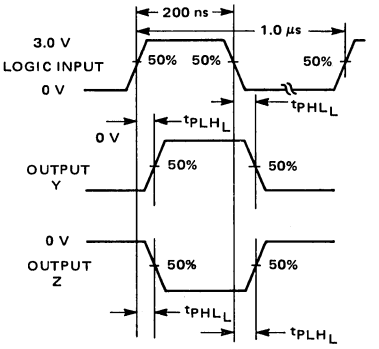
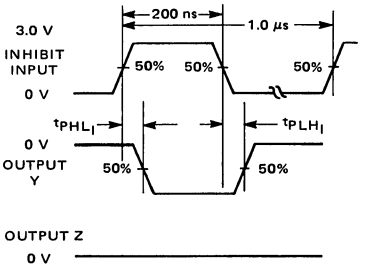


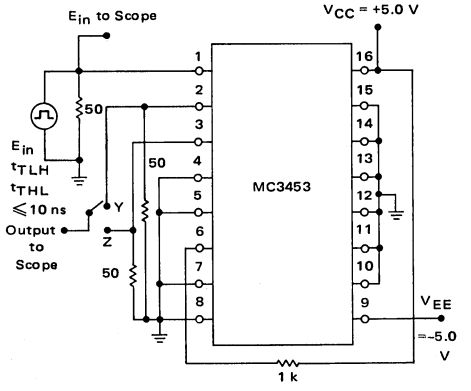
FIGURE 3 – INHIBIT INPUT TO OUTPUTS PROPAGATION DELAY TIME WAVEFORMS



7

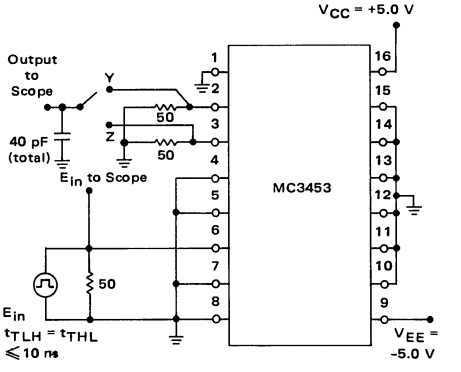
TEST CIRCUITS

FIGURE 4 – LOGIC INPUT TO OUTPUT PROPAGATION DELAY TIME TEST CIRCUIT



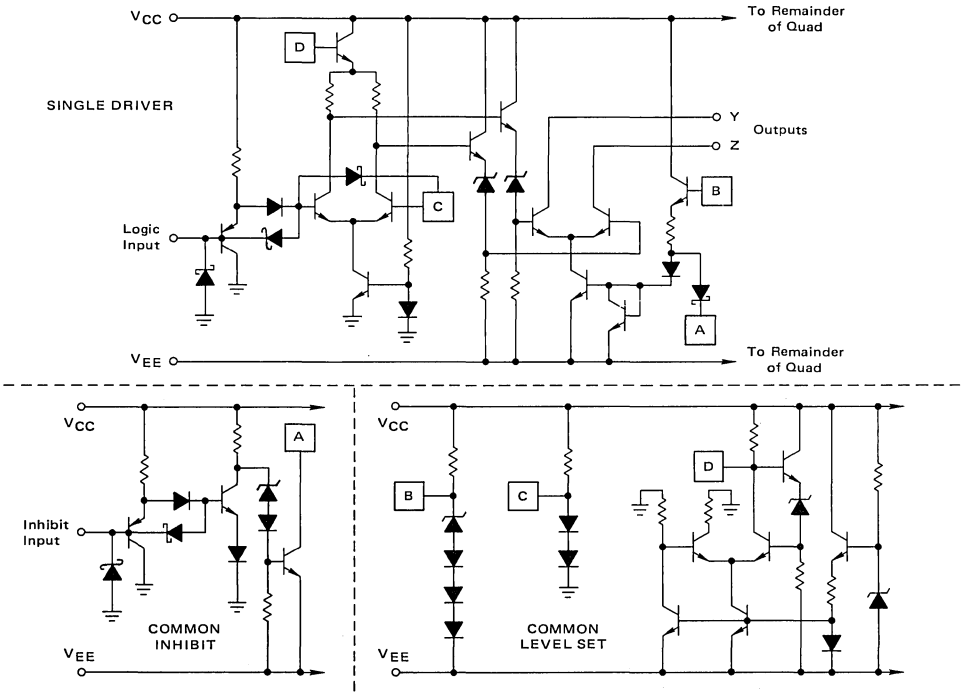
Channel A shown under test, the other channels are tested similarly.

FIGURE 5 – INHIBIT INPUT TO OUTPUT PROPAGATION DELAY TIME TEST CIRCUIT



Channel A shown under test, the other channels are tested similarly.

FIGURE 6 – CIRCUIT SCHEMATIC
(1/4 Circuit Shown)



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC3467

TRIPLE MAGNETIC TAPE MEMORY PREAMPLIFIER

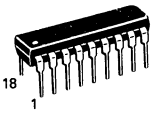
SILICON MONOLITHIC
INTEGRATED CIRCUIT

TRIPLE WIDEBAND PREAMPLIFIER WITH ELECTRONIC GAIN CONTROL (EGC)

The MC3467 provides three independent preamplifiers with individual electronic gain control in a single 18-pin package. Each preamplifier has differential inputs and outputs allowing operation in completely balanced systems. The device is optimized for use in 9-track magnetic tape memory systems where low noise and low distortion are paramount objectives.

The electronic gain control allows each amplifier's gain to be set anywhere from essentially zero to a maximum of approximately 100 V/V.

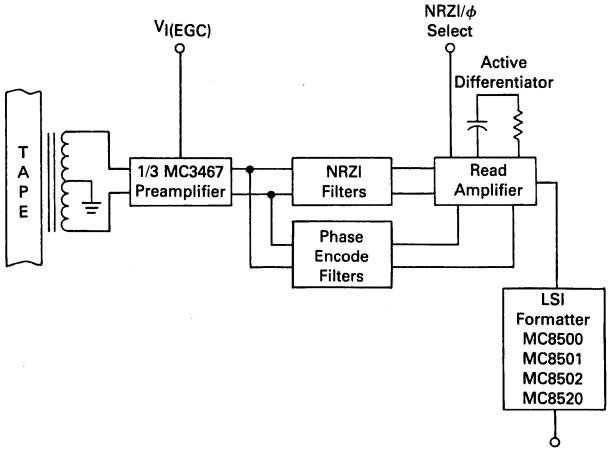
- Wide Bandwidth – 15 MHz (Typ)
- Individual Electronic Gain Control
- Differential Input/Output



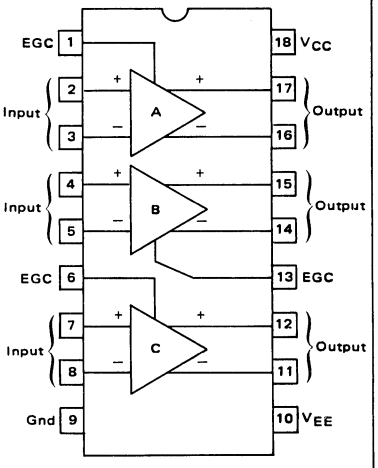
P SUFFIX
PLASTIC PACKAGE
CASE 707

7

TYPICAL APPLICATION
HIGH PERFORMANCE 9-TRACK OPEN REEL TAPE SYSTEM



PIN CONNECTIONS



MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltages Positive Supply Voltage Negative Supply Voltage	 V_{CC} V_{EE}	 6.0 −9.0	V
EGC Voltages (Pins 1, 6 and 13)	$V_{I(EGC)}$	−5.0 to V_{CC}	V
Input Differential Voltage	V_{ID}	±5.0	V
Input Common-Mode Voltage	V_{IC}	±5.0	V
Amplifier Output Short Circuit Duration (to Ground)	t_{sc}	10	s
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Junction Temperature	T_J	+150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, V_{EE} = −6.0 V, f = 100 kHz, T_A = 0 to +70°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Voltage Range Positive Supply Voltage Negative Supply Voltage Operating EGC Voltage	 V_{CCR} V_{EER} $V_{I(EGC)}$	 4.75 −5.5 0	 5.0 −6.0 –	 5.25 −7.0 V_{CC}	 V V V
Differential Voltage Gain (Balanced) ($V_{I(EGC)}$ = 0, e_i = 25 mVp-p) (See Figure 1)	A_{VD}	85	100	120	V/V
Differential Voltage Gain ($V_{I(EGC)}$ = V_{CC})	A_{VD}	–	0.5	2.0	V/V
Maximum Input Differential Voltage (Balanced) (T_A = 25°C)	V_{IDR}	0.2	–	–	V_{pp}
Output Voltage Swing (Balanced) (Figure 1) (e_i = 200 mVp-p)	V_{OR}	6.0	8.0	–	V_{pp}
Input Common-Mode Range	V_{ICR}	±1.5	±2.0	–	V
Differential Output Offset Voltage (T_A = 25°C)	V_{OOD}	–	500	–	mV
Common-Mode Output Offset Voltage (T_A = 25°C)	V_{OOC}	–	500	–	mV
Common Mode Rejection Ratio (Figure 2) $V_{I(EGC)}$ = 0, V_{CM} = 1.0 V_{pp} (f = 100 kHz) (f = 1.0 MHz)	CMRR	 60 40	 100 100	 – –	dB
Small-Signal Bandwidth (Figure 1) (−3.0 dB, e_i = 1.0 mVp-p, T_A = 25°C)	BW	10	15	–	MHz
Input Bias Current	I_{IB}	–	5.0	15	μA
Output Sink Current (Figure 5)	I_{OS}	1.0	1.4	–	mA
Differential Noise Voltage Referred to Input (Figure 3) ($V_{I(EGC)}$ = 0, R_S = 50 Ω, BW = 10 Hz to 1.0 MHz, T_A = 25°C)	e_n	–	3.5	–	μV_{RMS}
Positive Power Supply Current (Figure 4)	I_{CC}	–	30	40	mA
Negative Power Supply Current (Figure 4)	I_{EE}	–	−30	−40	mA
Input Resistance (T_A = 25°C)	r_i	12	25	–	kΩ
Input Capacitance (T_A = 25°C)	C_i	–	2.0	–	pF
Output Resistance (Unbalanced) (T_A = 25°C)	r_o	–	30	–	Ohms

7

FIGURE 1 – DIFFERENTIAL VOLTAGE GAIN, BANDWIDTH AND OUTPUT VOLTAGE SWING TEST CIRCUIT
(Channel A under test, other channels tested similarly)

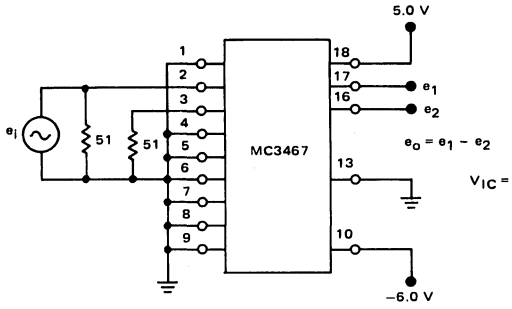


FIGURE 2 – COMMON-MODE REJECTION RATIO
(Channel A under test, other amplifiers tested similarly)

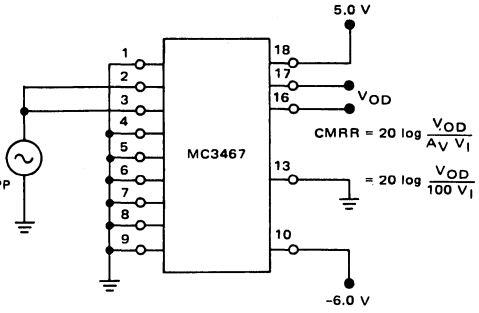


FIGURE 3 – DIFFERENTIAL NOISE VOLTAGE REFERRED TO THE INPUT

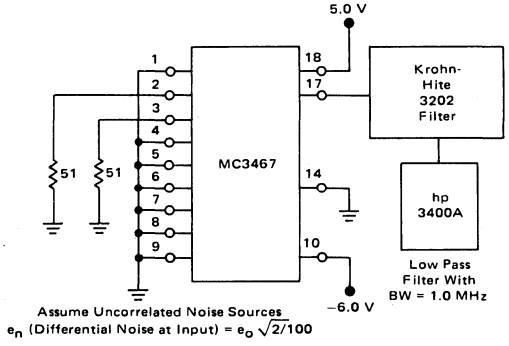


FIGURE 4 – POWER SUPPLY CURRENT TEST CIRCUIT

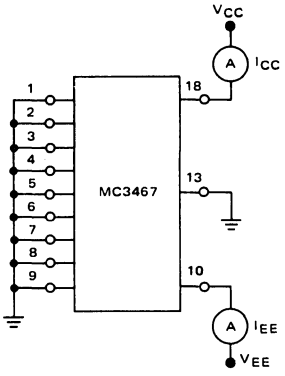


FIGURE 5 – OUTPUT SINK CURRENT TEST CIRCUIT
(Channel A under test, other channels tested similarly)

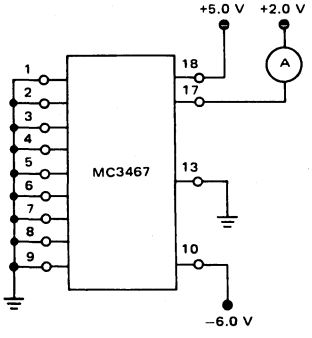
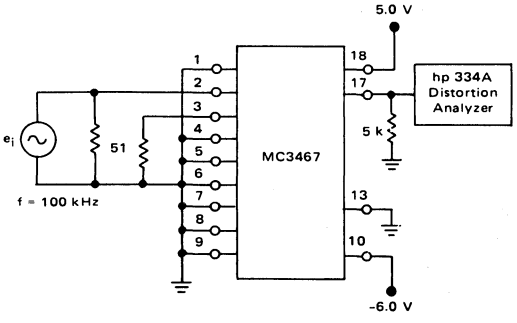


FIGURE 6 – TOTAL HARMONIC DISTORTION TEST CIRCUIT
(Channel A under test, other channels tested similarly)



TYPICAL CHARACTERISTICS
(V_{CC} = 5.0 V, V_{EE} = -6.0 V, T_A = 25° unless otherwise noted)

FIGURE 7 – TOTAL HARMONIC DISTORTION (THD) versus INPUT VOLTAGE

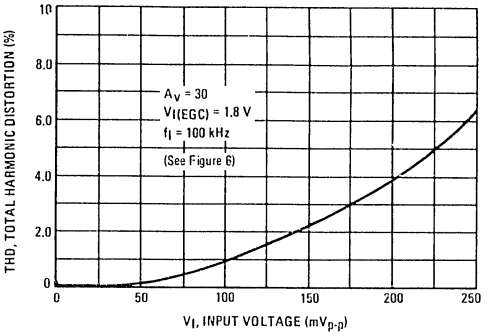


FIGURE 8 – NORMALIZED VOLTAGE GAIN versus FREQUENCY

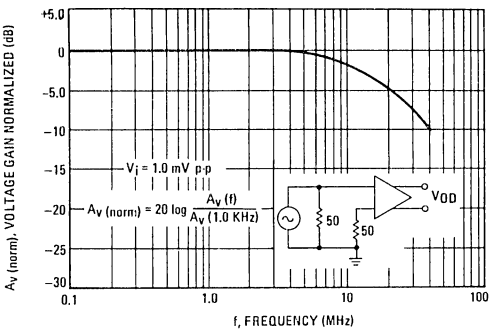


FIGURE 9 – NORMALIZED VOLTAGE GAIN versus AMBIENT TEMPERATURE

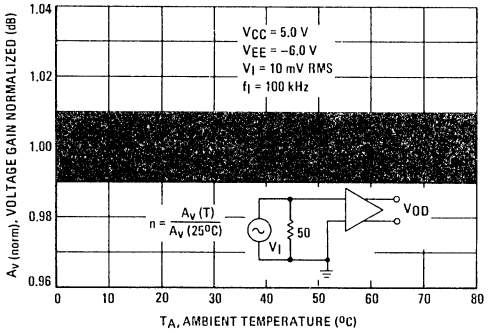


FIGURE 10 – NORMALIZED POSITIVE POWER SUPPLY CURRENT versus POSITIVE POWER SUPPLY VOLTAGE

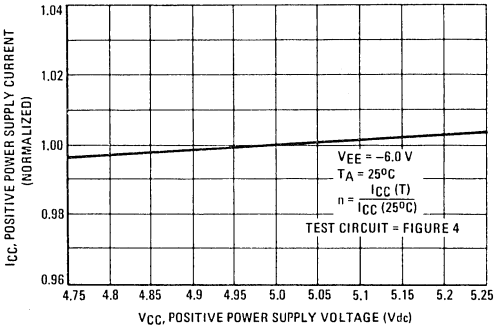


FIGURE 11 – NORMALIZED NEGATIVE POWER SUPPLY CURRENT versus NEGATIVE POWER SUPPLY VOLTAGE

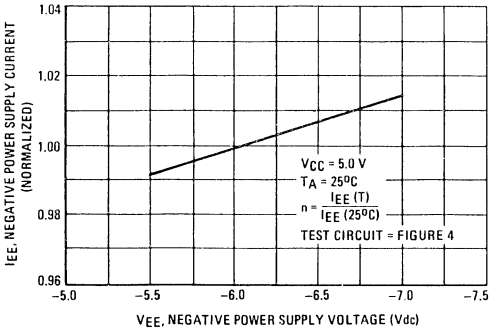


FIGURE 12 – NORMALIZED POWER SUPPLY CURRENTS versus AMBIENT TEMPERATURE

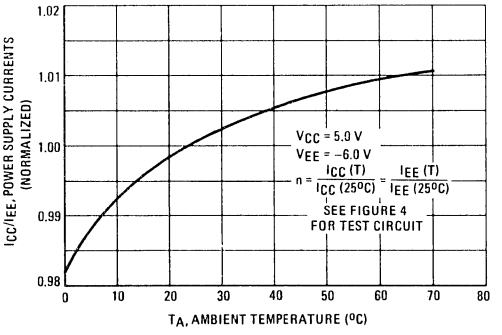


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FIGURE 13 – DIFFERENTIAL VOLTAGE GAIN versus ELECTRONIC GAIN CONTROL VOLTAGE ($V_{I(EGC)}$)

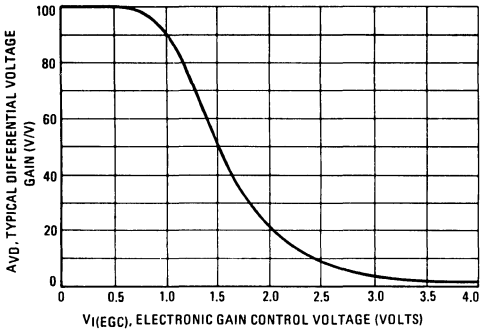


FIGURE 14 – COMMON-MODE REJECTION RATIO (CMRR) versus FREQUENCY

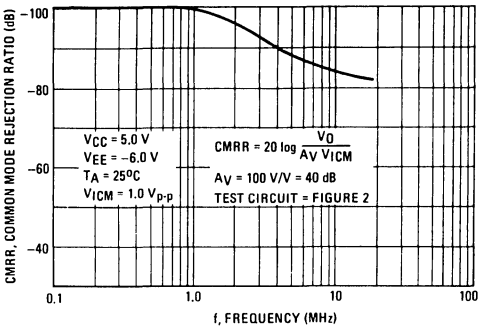


FIGURE 15 – PHASE SHIFT versus FREQUENCY

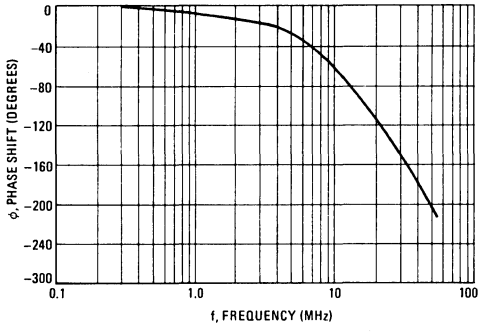
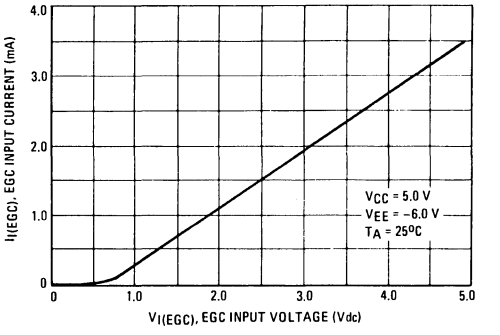
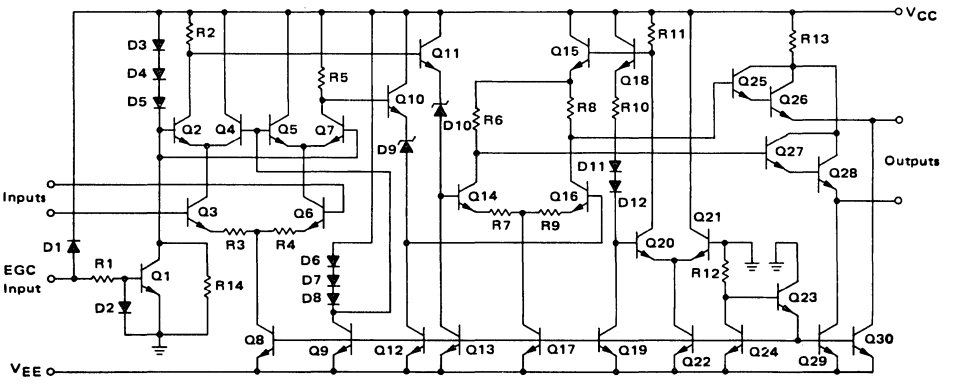


FIGURE 16 – TYPICAL EGC INPUT CURRENT versus EGC INPUT VOLTAGE



REPRESENTATIVE CIRCUIT SCHEMATIC

1/3 MC3467



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC3469

FLOPPY DISK WRITE CONTROLLER

The MC3469 is a monolithic WRITE Current Controller designed to provide the entire interface between floppy disk heads and the head control and write data signals for stradle-erase heads.

Provisions are made for selecting a range of accurately controlled write currents and for head selection during both read and write operation. Additionally, provisions are included for externally adjusting degauss period and inner/outer track compensation.

- Head Selection — Current Steering Through Write Head and Erase Coil in Write Mode
- Provides High Impedance (Read Data Enable) During Read Mode
- Head Current (Write) Guaranteed Using Laser Trimmed Internal Resistor (3.0 mA using R_{ext} = 10 kΩ)
- IRW Select Input Provides for Inner/Outer Track Compensation
- Degauss Period Externally Adjustable
- Specified With ±10% Logic Supply and Head Supply (V_{BB}) from 10.8 V to 26.4 V
- Minimizes External Components
- See Application Note AN917 for Further Information

FLOPPY DISK WRITE CONTROLLER

SILICON MONOLITHIC INTEGRATED CIRCUIT

P SUFFIX
PLASTIC PACKAGE
CASE 648

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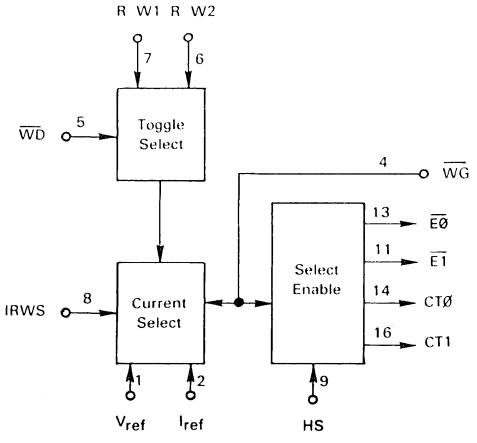
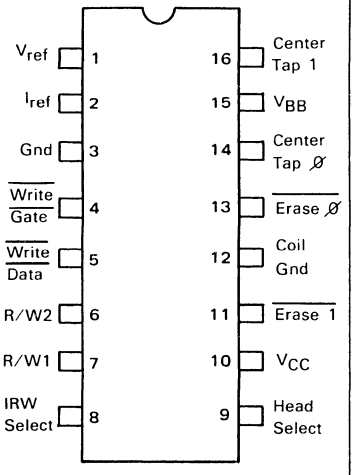
BLOCK DIAGRAM



PIN CONNECTIONS



MAXIMUM RATINGS (T_A = 25°C)

Rating	Symbol	Value	Unit
Power Supply Voltage (Pin 10)	V_{CC}	7.0	Vdc
Power Supply Voltage (Pin 15)	V_{BB}	30	Vdc
Input Voltage (Pins 4, 5, 8, 9)	V_I	5.75	Vdc
Storage Temperature	T_{stg}	-55 to +150	°C
Operating Junction Temperature	T_J	150	°C

RECOMMENDED OPERATING CONDITIONS

Rating	Symbol	Value	Unit
Power Supply Voltage (Pin 10)	V_{CC}	+4.5 to +5.5	Vdc
Power Supply Voltage (Pin 15)	V_{BB}	+10.8 to +26.4	Vdc
Operating Ambient Temperature Range	T_A	0 to +70	°C

ELECTRICAL CHARACTERISTICS (T_A = 0 to +70°C, V_{CC} = 4.5 to 5.5 V, V_{BB} = 10.8 to 26.4 V unless otherwise noted. Typicals given for V_{CC} = 5.0 V, V_{BB} = 12 V and T_A = 25°C unless otherwise noted.)

Characteristics	Pins	Symbol	Min	Typ	Max	Unit
DIGITAL INPUT VOLTAGES						
Power Supply Current — V_{CC} V_{BB}		I_{CC} I_{BB}	— —	22 15	50 30	mA
High Level Input Voltage (V_{CC} = 4.5 V)	4, 8, 9	V_{IH}	2.0	—	—	V
Low Level Input Voltage (V_{CC} = 5.5 V)	4, 8, 9	V_{IL}	—	—	0.8	V
Input Clamp Voltage (I_{IK} = −12 mA)	4, 5, 8, 9	V_{IK}	—	-0.87	-1.5	V
Positive Threshold (V_{CC} = 5.0)	5	$V_{T(+)}$	1.5	1.75	2.0	V
Negative Threshold (V_{CC} = 5.0)	5	$V_{T(-)}$	0.7	0.98	1.3	V
Hysteresis ($V_{T(+)} - V_{T(-)}$) T_A = 0°C to +70°C T_A = 25°C		V_{HTS}	 0.2 0.4	 — 0.76	 — —	V
DIGITAL INPUT CURRENTS						
High Level Input Current (V_{CC} = 5.5 V, V_{BB} = 26.4 V, V_I = 2.4 V)	4, 5, 8, 9	I_{IH}	—	0.1	40	μA
Low Level Input Current (V_{CC} = 5.5 V, V_{BB} = 26.4 V, T_A = 25°C unless noted below)	4, 5, 8, 9	I_{IL}	—	—	-1.6	mA
V_{BB} = 12 V	4		—	0.36	—	
V_{BB} = 24 V	4		—	0.76	—	
V_{CC} = 5.0 V	5		—	0.46	—	
V_{CC} = 5.0 V	8, 9		—	0.39	—	

ELECTRICAL CHARACTERISTICS (continued) (T_A = 0 to +70°C, V_{CC} = 4.5 to 5.5 V, V_{BB} = 10.8 to 26.4 V unless otherwise noted. Typicals given for V_{CC} = 5.0 V, V_{BB} = 12 V and T_A = 25°C unless otherwise noted.)

Characteristics	Pins	Symbol	Min	Typ	Max	Unit
CENTER-TAP and ERASE OUTPUTS						
Output High Voltage (See Figure 9) (I_{OH} = −100 mA, V_{CC} = 4.5 V) V_{BB} = 10.8 to 26.4 V	14, 16	V_{OH}	 V_{BB}-1.5	 V_{BB}-1.0	 —	V
Output Low Voltage (See Figure 9) (I_{OL} = 1.0 mA) V_{BB} = 12 V V_{BB} = 24 V	14, 16	V_{OL}	 — —	 70 70	 150 150	mV
Output High Leakage (V_{OH} = 24 V, V_{CC} = 4.5 V, V_{BB} = 24 V)	11, 13	I_{OH}	—	0.01	100	μA
Output Low Voltage (See Figure 10) (I_{OL} = 90 mA, V_{CC} = 4.5 V) V_{BB} = 12 V V_{BB} = 24 V	11, 13	V_{OL}	 — —	 0.27 0.27	 0.60 0.60	V
CURRENT SOURCE						
Reference Voltage	1	V_{ref}	—	5.7	—	V
Degauss Voltage (See Text) (Voltage Pin 1 − Voltage Pin 2)	1	V_{DEG}	—	1.0	—	V
Bias Voltage	2	V_F	—	0.7	—	V
Write Current Off Leakage (V_{OH} = 35 V)	6, 7	I_{OH}	—	0.03	15	μA
Saturation Voltage (V_{BB} = 12 V)	6, 7	V_{sat}	—	0.85	2.7	V
Current Sink Compliance (For $V_{6,7}$ = 4.0 V to 24 V, $V_{\overline{WG}}$ = 0.8 V)	6, 7	ΔI/RW2, 1	—	15	40	μA
Average Value Write Current ($\frac{I_{Pin\ 6} + I_{Pin\ 7}}{2}$ for V_{BB} = 10.8 to 26.4 V) @ $I_{R/W} = I_{LOW}$, R = 10 k T_A = 25°C T_A = 0 to +70°C @ $I_{R/W} = I_{LOW}$, R = 5.0 k T_A = 25°C T_A = 0 to +70°C @ $I_{R/W} = I_{HI}$, R = 10 k ($I_{HI} = I_{LOW}$ + % I_{LOW}) T_A = 25°C T_A = 0 to +70°C	6, 7	 $\overline{I_{R/W(L)}}$ $\overline{\Delta I_{R/W(H)}}$	 2.91 2.84 5.64 5.51 31.3 30.3	 3.0 — 5.89 — 33.3 33.3	 3.09 3.16 6.14 6.28 35.5 36.6	 mA %
Difference in Write Current ($\lvert I_{Pin\ 6} - I_{Pin\ 7}\rvert$ @ $I_{R/W} = I_{LOW}$, V_{BB} = 10.8 V to 26.4 V) R = 10 k T_A = 25°C T_A = 0 to +70°C R = 5.0 k T_A = 25°C T_A = 0 to +70°C	6, 7	 $I_{R/W\Delta}$	 — — — —	 0.003 — — —	 0.015 0.023 0.030 0.046	 mA

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AC SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C, V_{BB} = 24 V, I_{RWS} = 0.4 and $I_{R/W}$ = 3.0 mA unless otherwise noted — refer to Figure 2 and Figure 11.)

Characteristics (Note 1)	f_{in} (Note 3)	Min	Typ	Max	Unit
1. Delay from Head Select going low through 0.8 V to CT0 going high through 20 V.	HS, Pin 9	—	1.6	4.0	μs
2. Delay from Head Select going low through 0.8 V to CT1 going low through 1.0 V.	HS, Pin 9	—	2.1	4.0	μs
3. Delay from Head Select going high through 2.4 V to CT0 going low through 1.0 V.	HS, Pin 9	—	1.7	4.0	μs
4. Delay from Head Select going high through 2.4 V to CT1 going high through 20 V.	HS, Pin 9	—	1.4	4.0	μs
5. Delay from $\overline{WG}$ going low through 0.8 V to CT0 going low through 1.0 V.	$\overline{WG}$, Pin 4	—	1.3	4.0	μs
6. Delay from $\overline{WG}$ going low through 0.8 V to CT1 going high through 20 V.	$\overline{WG}$, Pin 4	—	0.8	4.0	μs
7. Delay from $\overline{WG}$ going low through 0.8 V to CT0 going high through 20 V.	$\overline{WG}$, Pin 4	—	0.75	4.0	μs
8. Delay from $\overline{WG}$ going low through 0.8 V to CT1 going low through 1.0 V.	$\overline{WG}$, Pin 4	—	1.2	4.0	μs
9. After $\overline{WG}$ goes high, delay from R/W1 turning off through 10% to CT0 going high through 20 V.	$\overline{WG}$, Pin 4	20	750	—	ns
10. After $\overline{WG}$ goes high, delay from R/W1 turning off through 10% to CT1 going low through 1.0 V.	$\overline{WG}$, Pin 4	20	1200	—	ns
11. After $\overline{WG}$ goes high, delay from R/W2 turning off through 10% to CT0 going low through 1.0 V.	$\overline{WG}$, Pin 4	20	1200	—	ns
12. After $\overline{WG}$ goes high, delay from R/W2 turning off through 10% to CT1 going high through 20 V.	$\overline{WG}$, Pin 4	20	600	—	ns
13. Delay from $\overline{WG}$ going low through 0.8 V to $\overline{E0}$ going low through 1.0 V.	$\overline{WG}$, Pin 4	—	0.085	4.0	μs
14. Delay from $\overline{WG}$ going low through 0.8 V to $\overline{E1}$ going low through 1.0 V.	$\overline{WG}$, Pin 4	—	0.085	4.0	μs
15. Delay from $\overline{WG}$ going high through 2.0 V to $\overline{E0}$ going high through 23 V.	$\overline{WG}$, Pin 4	—	0.7	4.0	μs
16. Delay from $\overline{WG}$ going high through 2.0 V to $\overline{E1}$ going high through 23 V.	$\overline{WG}$, Pin 4	—	0.7	4.0	μs
17. After $\overline{WG}$ goes low, delay from CT0 going low through 1.0 V to R/W1 turning on through 10%.	$\overline{WG}$, Pin 4	20	750	—	ns
18. After $\overline{WG}$ goes low, delay from CT1 going low through 1.0 V to R/W2 turning on through 10%.	$\overline{WG}$, Pin 4	20	750	—	ns
19. After $\overline{WG}$ goes low, fall time (10% to 90%) of R/W1.	$\overline{WG}$, Pin 4	—	5.0	200	ns
20. After $\overline{WG}$ goes low, fall time (10% to 90%) of R/W2.	$\overline{WG}$, Pin 4	—	5.0	200	ns
21. Setup time, Head Select going low before $\overline{WG}$ going low.	$\overline{WG}$, Pin 4	4.0	—	—	μs
22. $\overline{\text{Write Data}}$ low Hold Time	$\overline{WD}$, Pin 5	200	—	—	ns
23. $\overline{\text{Write Data}}$ high Hold Time	$\overline{WD}$, Pin 5	500	—	—	ns
24. Delay from $\overline{WG}$ going high through 2.0 V to R/W 1 turning off through 10% of on value.	$\overline{WG}$, Pin 4	—	3.9	—	μs

Notes 1. Test numbers refer to encircled numbers in Figure 2.
2. AC test waveforms applied to the designated pins as follows:

Pin	f_{in}	Amplitude	Duty Cycle
HS, Pin 9	50 kHz	0.4 to 2.4 V	50%
$\overline{WG}$, Pin 4	50 kHz	0.4 to 2.4 V	50%
$\overline{WD}$, Pin 5	1.0 MHz	0.2 to 2.4 V	50%

3. Test numbers refer to encircled numbers in Figure 4.
f_{in} = 1.0 MHz, 50% Duty Cycle and Amplitude of 0.2 V to 2.4 V.

AC SWITCHING CHARACTERISTICS (continued)
(V_{CC} = 5.0 V, T_A = 25°C, V_{BB} = 24 V, $\overline{WG}$ = 0.4 unless otherwise noted — refer to Figure 3 and Figure 11.)

Characteristics (Note 3)	Min	Typ	Max	Unit
1. Delay from $\overline{\text{Write Data}}$ going low through 0.9 V to R/W1 turning on through 50%.	—	85	—	ns
2. Delay skew, difference of R/W1 turning off and R/W2 turning on through 50% after $\overline{\text{Write Data}}$ going low through 0.9 V.	—	1.0	±40	ns
3. Delay from $\overline{\text{Write Data}}$ going low through 0.9 V to R/W1 turning off through 50%.	—	80	—	ns
4. Delay skew, difference of R/W1 turning on and R/W2 turning off 50% after $\overline{\text{Write Data}}$ going low through 0.9 V.	—	1.0	±40	ns
5. Rise time, 10% to 90%, of R/W1	—	1.7	200	ns
6. Rise time, 10% to 90%, of R/W2	—	1.7	200	ns
7. Fall time, 90% to 10%, of R/W1	—	12	200	ns
8. Fall time, 90% to 10%, of R/W2	—	12	200	ns

PIN DESCRIPTION TABLE

Name	Symbol	Pin	Description
Head Select	HS	9	Head Select input selects between the head I/O pins: center-tap, erase, and read/write. A HIGH selects Head 0 and a LOW selects Head 1.
$\overline{\text{Write Gate}}$	$\overline{WG}$	4	$\overline{\text{Write Gate}}$ input selects the mode of operation. HIGH selects the read mode, while LOW selects the Write Control mode and forces the write current.
$\overline{\text{Write Data}}$	$\overline{WD}$	5	$\overline{\text{Write Data}}$ input controls the turn on/off of the write current. The internal divide-by-two flip-flop toggles on the negative going edge of this input to direct the current alternately to the two halves of the head coils.
IRW Select	IRWS	8	IRW Select input selects the amount of write current to be used. When LOW, the current equals the value found in Figure 5, according to the external resistor. When HIGH, the current equals the low current + 33%.
V_{ref} I_{ref}	V_{ref} I_{ref}	1 2	A resistor between these pins sets the write current. Laser trimming reliably produces 3 mA of current for a 10 k resistor. A capacitor from V_{ref} to Gnd will adjust the Degauss period.
Center-tap 0	CT0	14	Center-tap 0 output is connected to the center tap of Head 0. It will be pulled to Gnd or V_{BB} (+12 or +24) depending on mode and head selection.
$\overline{\text{Erase 0}}$	$\overline{E0}$	13	$\overline{\text{Erase 0}}$ will be LOW for writing on Head 0, and floating for other conditions.
Center-tap 1	CT1	16	Center-tap 1 output is connected to the center tap of Head 1. It will be pulled to Gnd or V_{BB} (+12 or +24) depending on mode and head selection.
$\overline{\text{Erase 1}}$	$\overline{E1}$	11	$\overline{\text{Erase 1}}$ will be LOW for writing on Head 1, and floating for other conditions.
R/W2	R/W2	6	R/W2 input is one of the differential inputs that sinks current during writing, being the opposite phase of R/W1. It will be connected to one side of the heads.
R/W1	R/W1	7	R/W1 input is one of the differential inputs that sinks current during writing, being the opposite phase of R/W2. It will be connected to one side of the heads.
	V_{CC}	10	+5 V Power
	V_{BB}	15	+12 V or + 24 V Power
	Gnd	12	Coil grounds
	Gnd	3	Reference and logic ground

FIGURE 1 — LOGIC DIAGRAM

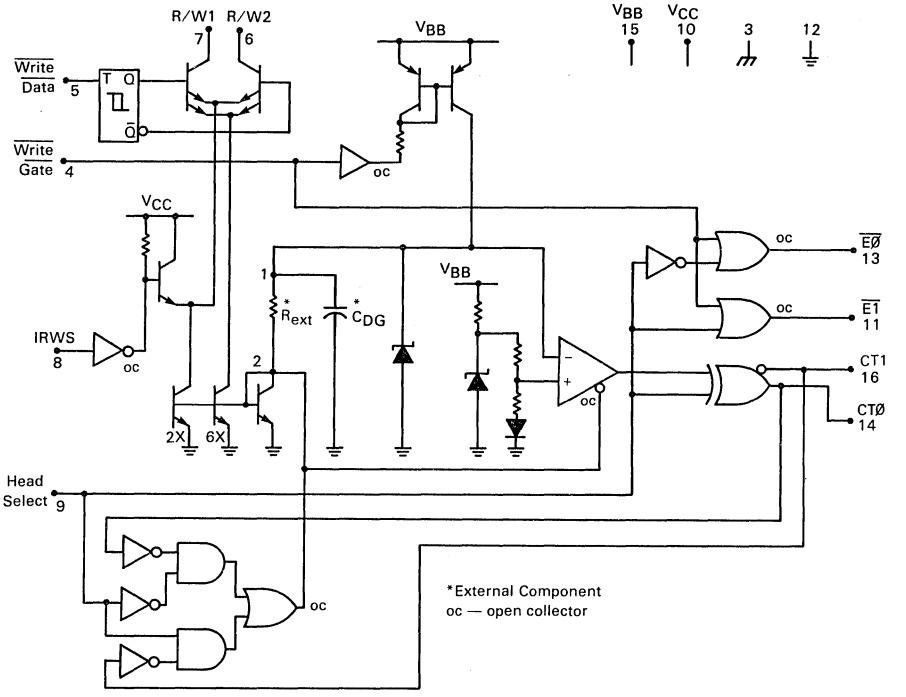

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FIGURE 2 — AC TIMING DIAGRAM

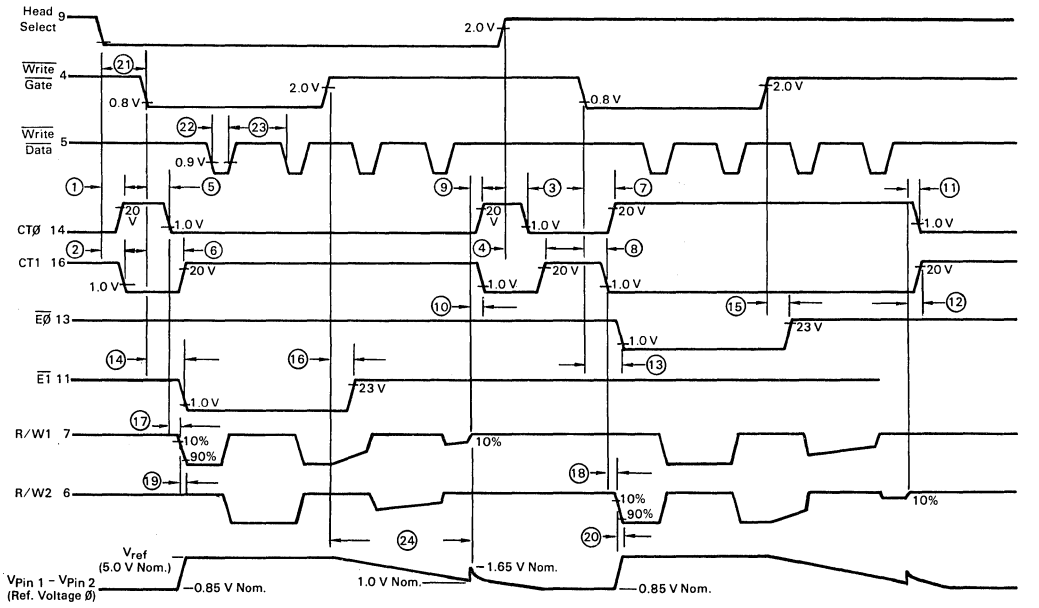
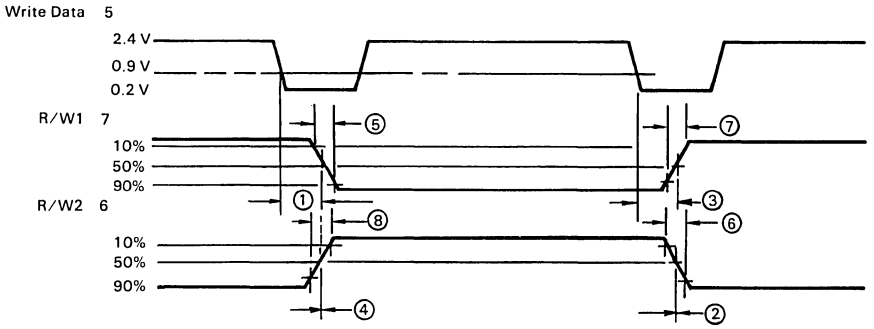


FIGURE 3 — R/W1 AND R/W2 RELATIONSHIP



APPLICATION INFORMATION

The MC3469P serves as a complete interface between the Write Control functional signals (Head Select, Write Data, Write Gate and inner track compensation, IRWS) and the head itself. A typical configuration is shown in Figure 4. L_E's are erase coils.

WRITE CURRENT SELECTION

Although the MC3469P has been specified for 3.0 mA write current (with a 10 kΩ external resistor), a range of write current values can be chosen by varying R_{ext} using the plot in Figure 5. This current can also be derived using the relationship $I_{Write}\,(mA) = \frac{30}{R_{ext}(k\Omega)}$

I_{Ref}, the current flowing in R_{ext} (required only for dissipation calculations) can be worst case using the fact that the differential voltage between Pins 1 and 2 (V_{Ref}) shown in Figure 3 never exceeds 5.0 volts. With a low value of R_{ext} = 1.0 kΩ, P_D = 25 mW.

WRITE CURRENT DAMPING

Referring to Figure 4, resistors R_D are used to dampen any ringing that results from applying the relatively fast risetime write current pulse to the inductive head load. Values chosen will be a funciton of head characteristics and the desired damping. R_P serves as a common pullup resistor to the head supply V_{BB}.

7

FIGURE 4 — TYPICAL APPLICATION

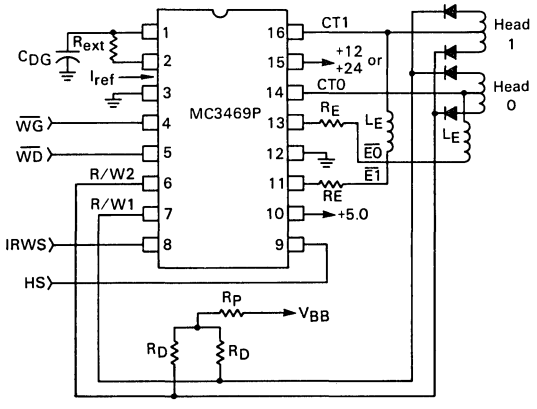
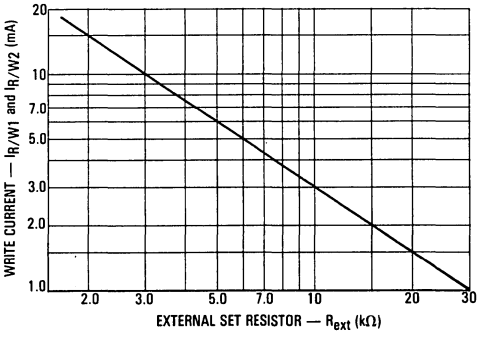


FIGURE 5 — WRITE CURRENT versus R_{ext}



DEGAUSS PERIOD

Degauss of the read/write head can be accomplished at the end of each write operation by attaching a capacitor from pin 1 to ground. The timing relationship that results is shown in Figure 7. A simplified diagram of this function is shown in Figure 6.

While $\overline{WG}$ is low, the selected write current flows into pin 6 or pin 7 (R/W1 or R/W2) and is mirrored through the external resistor, R_{ext}. The degauss capacitor, C_{DG}, will be charged to approximately 5.7 volts. After $\overline{WG}$ goes high, the voltage on C_{DG} begins to decay toward 0.7 V. When the voltage reaches the comparator threshold of 1.7 V, the comparator output triggers the internal logic to completely turn off the write current. At this point, the pulse amplitude on the R/W1 and R/W2 pins has returned to 10% of its maximum value.

Figure 7, Degauss Period shows the relationship between C_{DG} and Degauss Period for R_{ext} = 10 kΩ. This period is equal to the exponential delay time for the voltage as mentioned plus some internal delay times.

POWER-UP WRITE CURRENT CONTROL

During power-up, under certain conditions (V_{BB} comes up first while $\overline{WG}$ is low), there can be a write current transient on Pins 6 and 7 (R/W1 and R/W2) of sufficient magnitude to cause writing to occur if the head is loaded.

This transient can be eliminated by placing a capacitor from Pin 2 to ground. This also delays the write current when $\overline{WG}$ goes low and this delay must be accounted for when the capacitor on Pin 2 is used. The delay is 3.0 μs for a 2700 pF capacitor, and R_{ext} = 10 kΩ. Values up to 7000 pF may be used.

FIGURE 6 — SIMPLIFIED DEGAUSS CIRCUIT

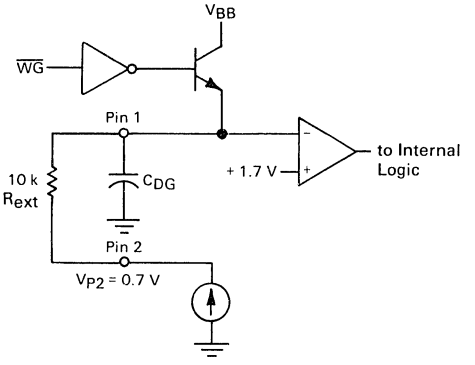


FIGURE 7 — DEGAUSS PERIOD versus CAPACITANCE (C_{DG})

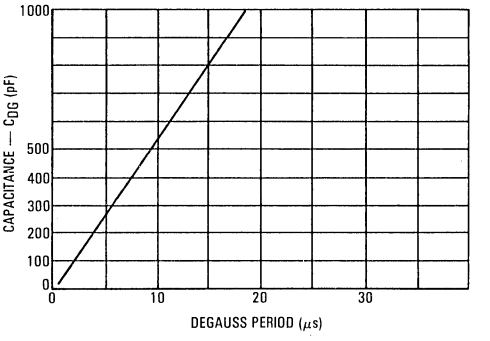
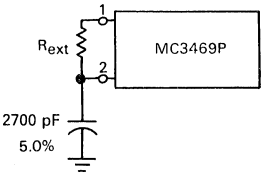
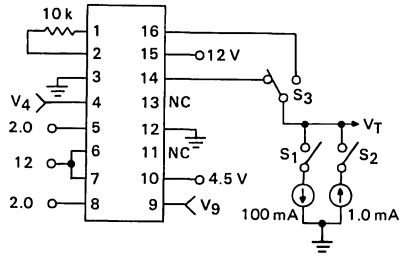


FIGURE 8 — TURN-ON WRITE PROTECTION



TEST FIGURES

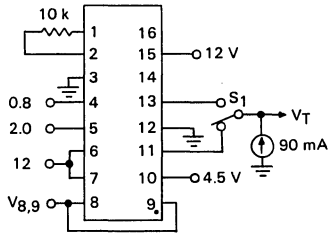
FIGURE 9 — CENTER TAP OUTPUT VOLTAGE (PINS 14 AND 16)



Measure V_T	CONDITIONS Set S_1	S_2	S_3	V_4*	V_9*
V_{OH} (P14)	On	Off	P14	0.8	2.0
				2.0	0.8
V_{OH} (P16)	On	Off	P16	2.0	2.0
				0.8	0.8
V_{OL} (P14)	Off	On	P14	0.8	0.8
				2.0	2.0
V_{OL} (P16)	Off	On	P16	2.0	0.8
				0.8	2.0

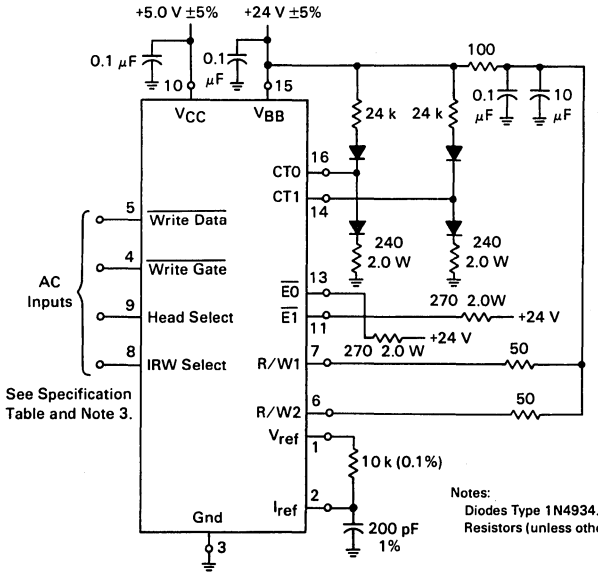
*Volts

FIGURE 10 — ERASE OUTPUT LOW VOLTAGE (PINS 11 AND 13)



Measure V_T	CONDITIONS Set S_1	$V_{8,9}$
V_{OL} (P11)	P11	0.8V
V_{OL} (P13)	P13	2.0 V

FIGURE 11 — TIMING TEST CIRCUIT



Notes:
Diodes Type 1N4934.
Resistors (unless otherwise noted) are 1/4 W, 5%.

ERASE CURRENT

The value of R_E, the erase current set resistor, is found by referring to Figure 12 and selecting the desired erase current.

Looking at the simplified erase current path in Figure 12, when writing, CTO will be high ($V_{OH(min)}$ = 21 V) and EO will be low ($V_{OL(max)}$ = 0.6 V). If the erase coil resistance is 10 Ω and 40 mA of erase current is desired, then:

$$(R_E + 10\ \Omega) \times 40\ mA = (21 - 0.6)\ V$$

or

$$R_E = \frac{20.4\ V}{0.04\ A} - 10\ \Omega = 500\ \Omega$$

$$P_D = (0.04)(20.4) = 0.816\ W \text{ or } 1.0\ W$$

This gives the minimum value R_E for worst case V_{OH}/V_{OL} conditions. It is also recommended that a diode be used as required for inductive back emf suppression.

Erase timing is provided internally and is active during Write Gate low for the selected head.

FIGURE 12 — ERASE CURRENT (R_E Selection)

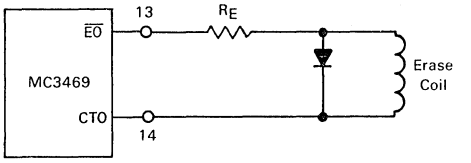
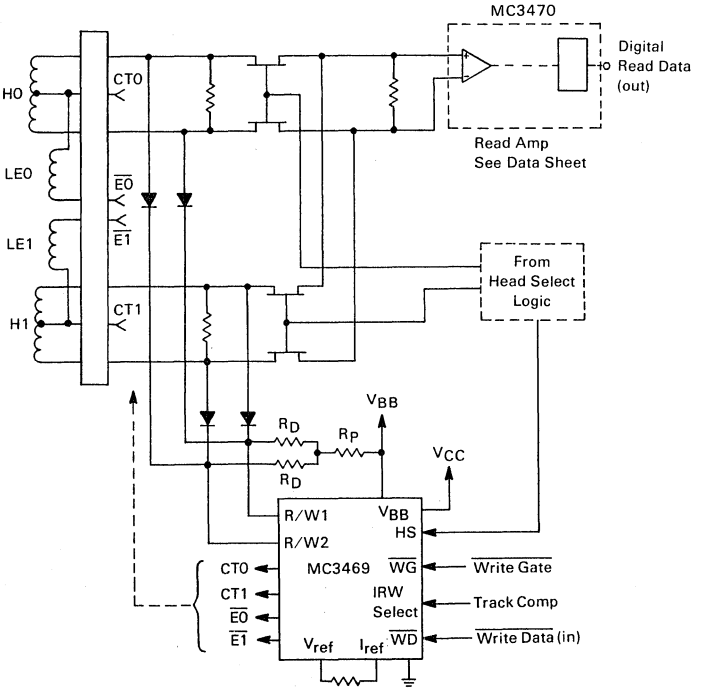


FIGURE 13 — TYPICAL DUAL HEAD FLOPPY DISK SYSTEM USING FET GATE READ CHANNEL SELECTION AND MC3469/MC3470



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC3470
MC3470A

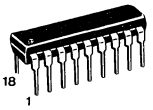
FLOPPY DISK READ AMPLIFIER

The MC3470 is a monolithic READ Amplifier System for obtaining digital information from floppy disk storage. It is designed to accept the differential ac signal produced by the magnetic head and produce a digital output pulse that corresponds to each peak of the input signal. The gain stage amplifies the input waveform and applies it to an external filter network, enabling the active differentiator and time domain filter to produce the desired output.

- Combines All the Active Circuitry To Perform the Floppy Disk Read Amplifier Function in One Circuit
- Guaranteed Maximum Peak Shift of 2.0% — MC3470A
- Improved (Positive) Gain T_C and Tolerance
- Improved Input Common Mode
- See Application Note AN917 for Further Information

FLOPPY DISK
READ AMPLIFIER SYSTEM

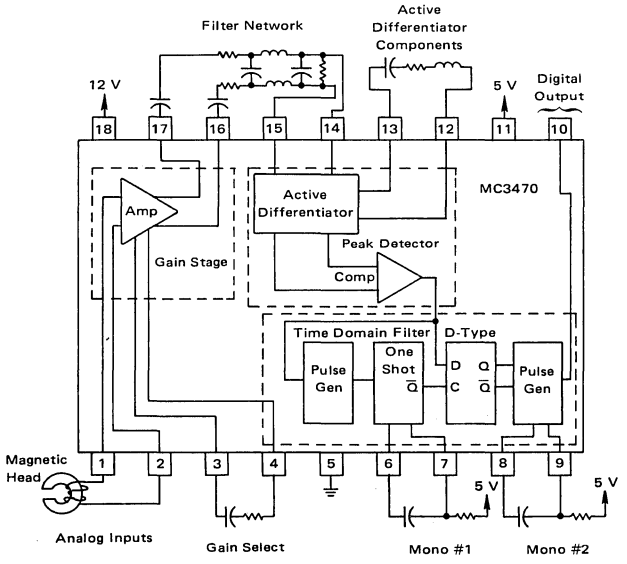
SILICON MONOLITHIC
INTEGRATED CIRCUIT



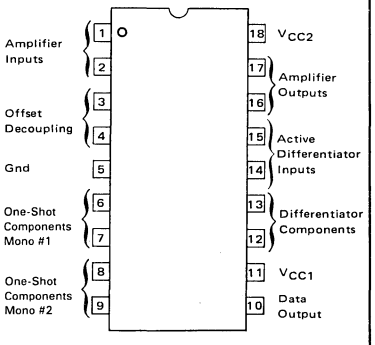
P SUFFIX
PLASTIC PACKAGE
CASE 707

7

TYPICAL APPLICATION



PIN CONNECTION



MAXIMUM RATINGS (T_A = 25°C)

Rating	Symbol	Value	Unit
Power Supply Voltage (Pin 11)	V_{CC1}	7.0	Vdc
Power Supply Voltage (Pin 18)	V_{CC2}	16	Vdc
Input Voltage (Pins 1 and 2)	V_I	-0.2 to +7.0	Vdc
Output Voltage (Pin 10)	V_O	-0.2 to +7.0	Vdc
Operating Ambient Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	-65 to +150	°C
Operating Junction Temperature Plastic Package	T_J	150	°C

RECOMMENDED OPERATING CONDITIONS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	V_{CC1} + 4.75 to +5.25 V_{CC2} +10 to +14	Vdc
Operating Ambient Temperature Range	T_A	0 to +70	°C

ELECTRICAL CHARACTERISTICS (T_A = 0 to +70°C, V_{CC1} = 4.75 to 5.25 V, V_{CC2} = 10 to 14 V unless otherwise noted)

Characteristic		Figure	Symbol	Min	Typ	Max	Unit
Differential Voltage Gain (f = 200 kHz, V_{iD} = 5.0 mV(RMS))	MC3470 MC3470A	2	A_{VD}	80 100	100 110	130 130	V/V
Input Bias Current		3	I_{IB}	—	-10	-25	μA
Input Common Mode Range Linear Operation (5% max THD)			v_{iCM}	-0.1	—	1.5	V
Differential Input Voltage Linear Operation (5% max THD)			v_{iD}	—	—	25	mVp-p
Output Voltage Swing Differential		2	v_{oD}	3.0	4.0	—	Vp-p
Output Source Current, Toggled			I_O	—	8.0	—	mA
Output Sink Current, Pins 16 and 17		4	I_{OS}	2.8	4.0	—	mA
Small Signal Input Resistance (T_A = 25°C)			r_i	100	250	—	kΩ
Small Signal Output Resistance, Single-Ended (T_A = 25°C, V_{CC1} = 5.0 V, V_{CC2} = 12 V)			r_o	—	15	—	Ω
Bandwidth, -3.0 dB (v_{iD} = 2.0 mV(RMS), T_A = 25°C V_{CC1} = 5.0 V, V_{CC2} = 12 V)		2, 17	BW	10	—	—	MHz
Common Mode Rejection Ratio (T_A = 25°C, f = 100 kHz, A_{VD} = 40 dB, v_{in} = 200 mVp-p, V_{CC1} = 5.0 V, V_{CC2} = 12 V)		5	CMRR	50	—	—	dB
V_{CC1} Supply Rejection Ratio (T_A = 25°C, V_{CC2} = 12 V, 4.75 ≤ V_{CC1} ≤ 5.25 V, A_{VD} = 40 dB)			—	50	—	—	dB
V_{CC2} Supply Rejection Ratio (T_A = 25°C, V_{CC1} = 5.0 V, 10 V ≤ V_{CC2} ≤ 14 V, A_{VD} = 40 dB)			—	60	—	—	dB
Differential Output Offset (T_A = 25°C, v_{iD} = v_{in} = 0 V)			V_{DO}	—	—	0.4	V
Common Mode Output Offset (v_{iD} = V_{in} = 0 V, Differential and Common Mode)			V_{CO}	—	3.0	—	V
Differential Noise Voltage Referred to Input (BW = 10 Hz to 1.0 MHz, T_A = 25°C)		22	e_n	—	15	—	μV(RMS)
Supply Currents (V_{CC1} = 5.25 V, S_1 to Pin 12 or Pin 13) (V_{CC2} = 14 V)		1	I_{CC1} I_{CC2}	— —	40 4.8	— —	mA

ELECTRICAL CHARACTERISTICS (continued) (T_A = 0 to +70°C, V_{CC1} = 4.75 to 5.25 V, V_{CC2} = 10 to 14 V unless otherwise noted)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
ACTIVE DIFFERENTIATOR SECTION						
Differentiator Output Sink Current, Pins 12 and 13 (V_{OD} = V_{CC1})	6	I_{OD}	1.0	1.4	—	mA
Peak Shift (f = 250 kHz, v_{iD} = 1.0 Vp-p, i_{cap} = 500 μA, where PS = $1/2 \frac{t_{PS1}-t_{PS2}}{t_{PS1}+t_{PS2}} \times 100\%$, V_{CC1} = 5.0 V, V_{CC2} = 12 V) MC3470	7, 8	PS	—	—	5.0	%
MC3470A			—	—	2.0	
Differentiator Input Resistance, Differential		r_{iD}	—	30	—	kΩ
Differentiator Output Resistance, Differential (T_A = 25°C)		r_{oD}	—	40	—	Ω
DIGITAL SECTION						
Output Voltage High Logic Level, Pin 10 (V_{CC1} = 4.75 V, V_{CC2} = 12 V, I_{OH} = -0.4 mA)	9	V_{OH}	2.7	—	—	V
Output Voltage Low Logic Level, Pin 10 (V_{CC1} = 4.75 V, V_{CC2} = 12 V, I_{OL} = 8.0 mA)	10	V_{OL}	—	—	0.5	V
Output Rise Time, Pin 10	11, 12	t_{TLH}	—	—	20	ns
Output Fall Time, Pin 10	11, 12	t_{THL}	—	—	25	ns
Timing Range Mono #1 (t_{1A} and t_{1B})	13	$t_{1A, B}$	500	—	4000	ns
Timing Accuracy Mono #1 (t1 = 1.0 μs = 0.625 R1C1 + 200 ns) (R1 = 6.4 kΩ, C1 = 200 pF) Accuracy guaranteed for R1 in the range 1.5 kΩ ≤ R1 ≤ 10 kΩ and C1 in the range 150 pF ≤ C1 ≤ 680 pF. Note: To minimize current transients, C1 should be kept as small as is convenient.	12, 13	E_{t1}	85	—	115	%
Timing Range Mono #2	11, 12	t2	150	—	1000	ns
Timing Accuracy Mono #2 (t2 = 200 ns = 0.625 R2C2) (R2 = 1.6 kΩ, C2 = 200 pF) Accuracy guaranteed for 1.5 kΩ ≤ R2 ≤ 10 kΩ, 100 pF ≤ C2 ≤ 800 pF	12, 13	E_{t2}	85	—	115	%

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MC3470 CIRCUIT SCHEMATIC

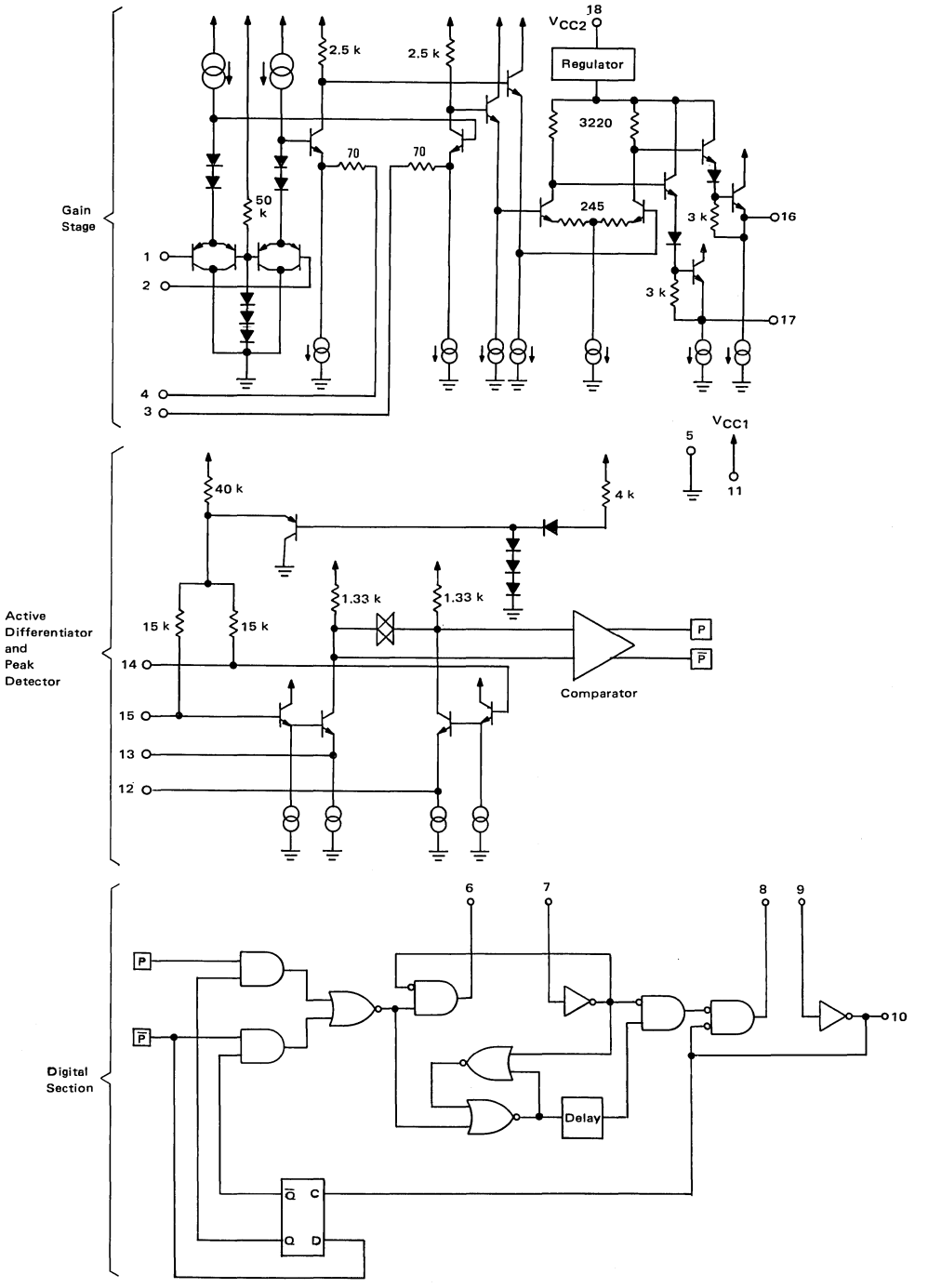

FIGURE 1 – POWER SUPPLY CURRENTS, I_{CC1} AND I_{CC2}

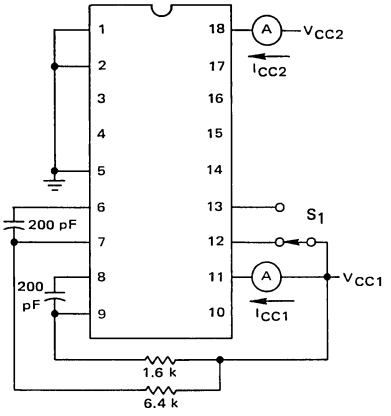

FIGURE 2 – VOLTAGE GAIN, BANDWIDTH, OUTPUT VOLTAGE SWING

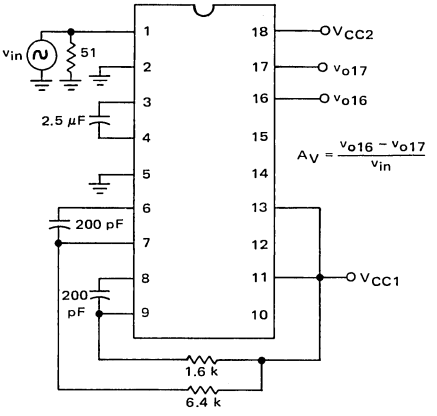

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FIGURE 3 – AMPLIFIER INPUT BIAS CURRENT, I_{IB}

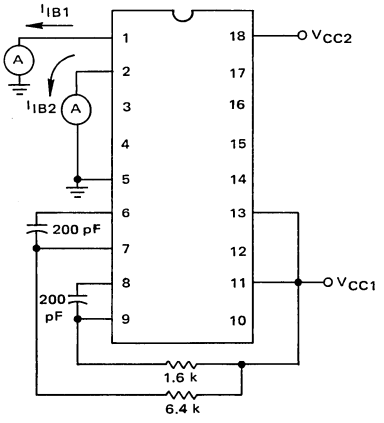


FIGURE 4 – AMPLIFIER OUTPUT SINK CURRENT, PINS 16 AND 17

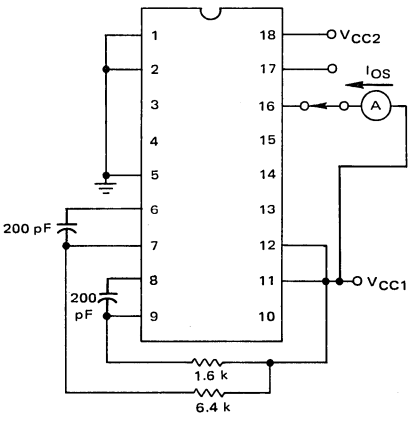
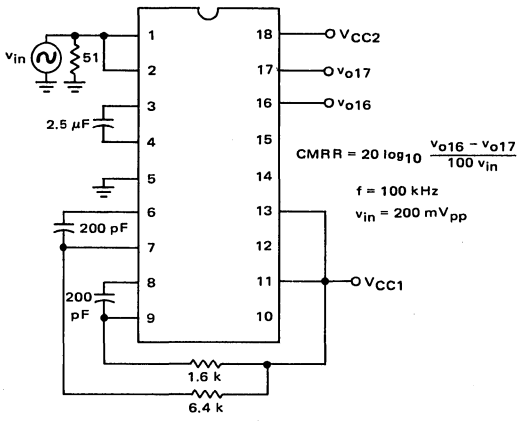


FIGURE 5 – AMPLIFIER COMMON MODE REJECTION RATIO, CMRR



NOTE: Measurements may be made with vector voltmeter hp 8405A or equivalent at 1.0 MHz to guarantee 100 kHz performance.

FIGURE 6 – DIFFERENTIATOR OUTPUT SINK CURRENT, PINS 12 AND 13

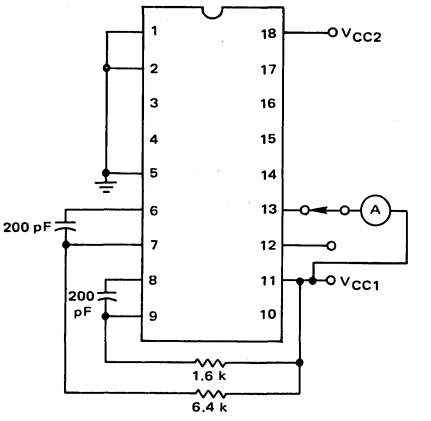


FIGURE 7 – PEAK SHIFT, PS

See Figure 8 for Output Waveform

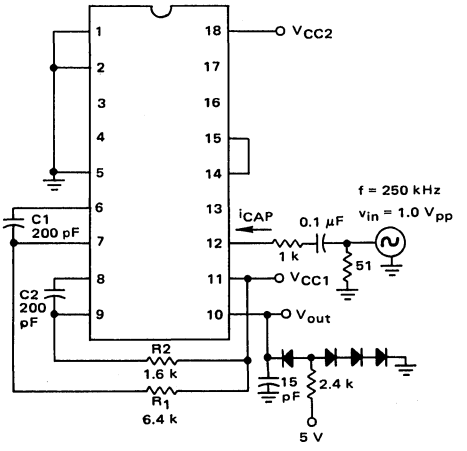
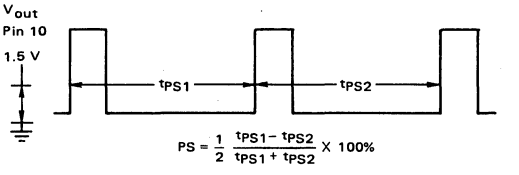


FIGURE 8 – PEAK SHIFT, PS

V_{in} = 1.0 V_{pp} f = 250 kHz

Test schematic on Figure 7



$$PS = \frac{1}{2} \frac{t_{PS1} - t_{PS2}}{t_{PS1} + t_{PS2}} \times 100\%$$

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FIGURE 9 – DATA OUTPUT VOLTAGE HIGH, PIN 10

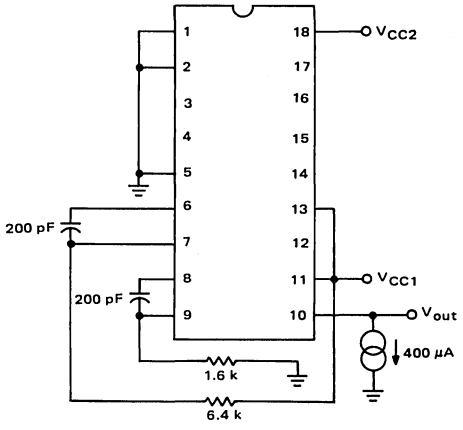

FIGURE 10 – DATA OUTPUT VOLTAGE LOW, PIN 10

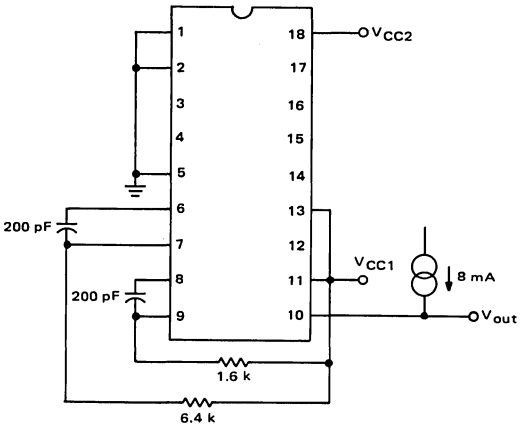

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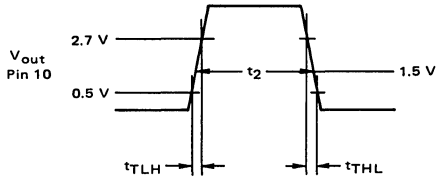
FIGURE 11 – DATA OUTPUT RISE TIME, t_{TLH}
DATA OUTPUT FALL TIME, t_{THL}
TIMING ACCURACY MONO #2, E_{t2}

V_{in} is same as shown on Figure 13, test schematic on Figure 12



$$E_{t2} = \frac{t_2}{200\ ns} \times 100\%$$

FIGURE 12 – TIMING ACCURACY, E_{t1} AND E_{t2}
DATA OUTPUT RISE AND FALL TIMES, t_{TLH} AND t_{THL}

V_{in} shown on Figure 13

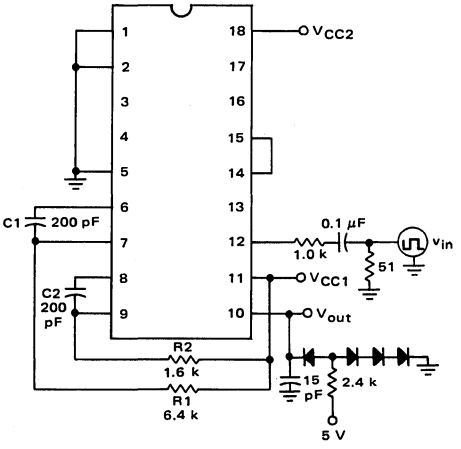
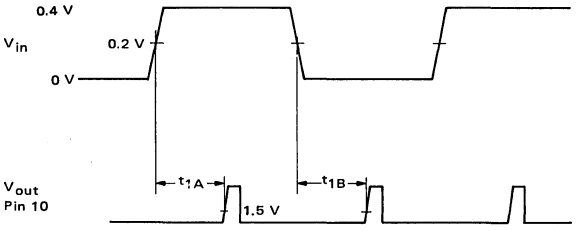


FIGURE 13 – TIMING ACCURACY MONO #1, E_{t1}

$t_{TLH} = t_{THL} < 10$ ns f = 250 kHz 50% Duty Cycle

Test Schematic on Figure 12

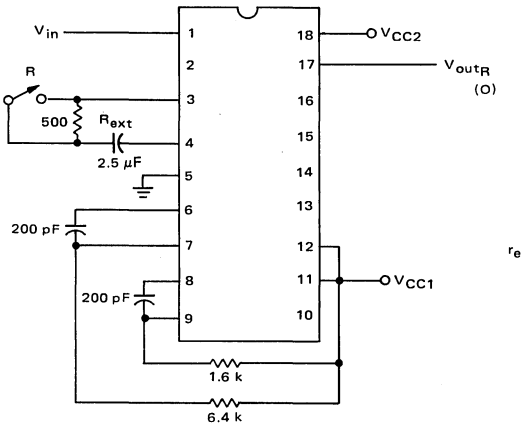


$$E_{t1A} = \frac{t_{1A}}{1000\ ns} \times 100\%$$

$$E_{t1B} = \frac{t_{1B}}{1000\ ns} \times 100\%$$

FIGURE 14 – AMPLIFIER OFFSET DECOUPLING IMPEDANCE, PINS 3 AND 4

$R_e + r_e$ and A_V with $R_{ext} = 500\ \Omega$



f = 250 kHz

V_{in} = 5 mV(RMS)

$$\frac{A_{VD}}{2} = \frac{V_{out}}{V_{in}}$$

$$r_e + R_e = \frac{R_{ext}}{2\left(\frac{A_{V_O}}{A_{V_R}} - 1\right)}$$

$$= \frac{500\ \Omega}{2\left(\frac{V_{out_O}}{V_{out_R}} - 1\right)}$$

FIGURE 15 – NORMALIZED POWER SUPPLY CURRENT (I_{CC}/I_{CC} 25°C) versus TEMPERATURE

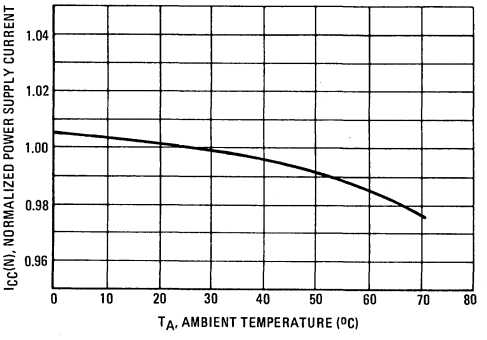


FIGURE 16 – NORMALIZED VOLTAGE GAIN (A_V/A_V 25°C) versus TEMPERATURE

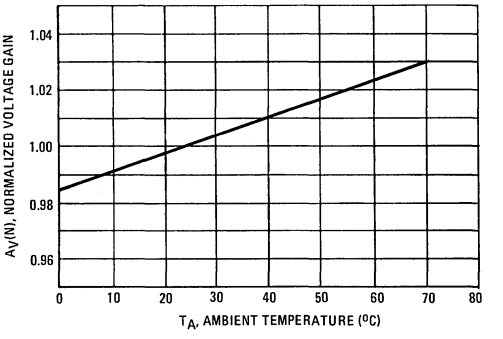


FIGURE 17 – PHASE AND NORMALIZED VOLTAGE GAIN versus FREQUENCY

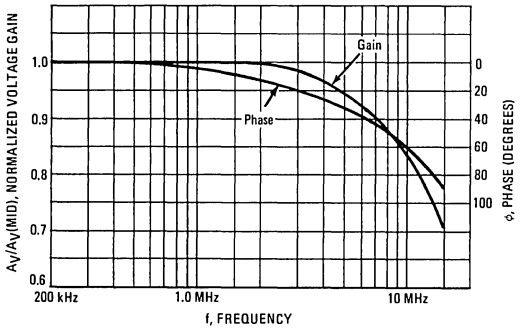


FIGURE 18 – NORMALIZED TIME DELAY t_1 versus TEMPERATURE

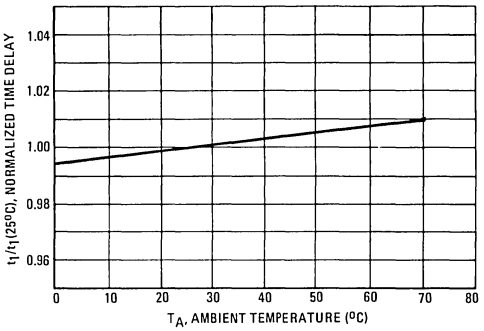


FIGURE 19 – NORMALIZED OUTPUT PULSE WIDTH, t_2/t_2 25°C

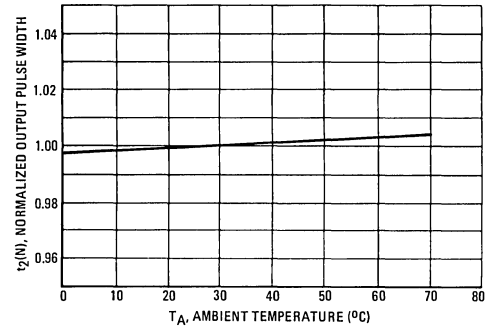


FIGURE 20 – NORMALIZED VOLTAGE GAIN, A_{VR}/A_{VR} 25°C

See Figure 14, Switch Position R

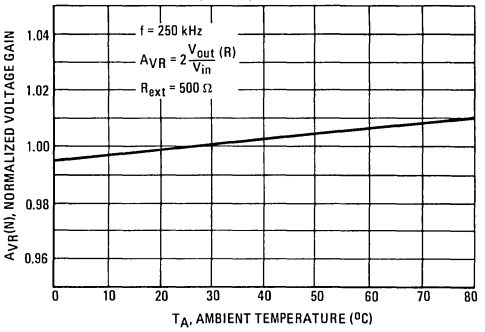


FIGURE 21 – EFFECTIVE EMITTER RESISTANCE DISTRIBUTION, PINS 3 AND 4

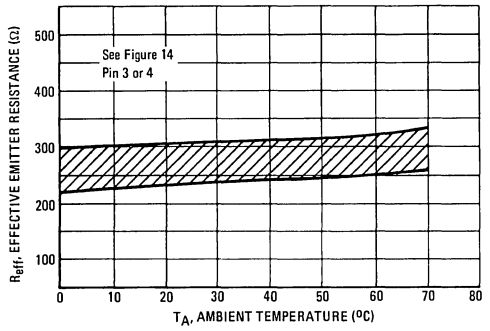
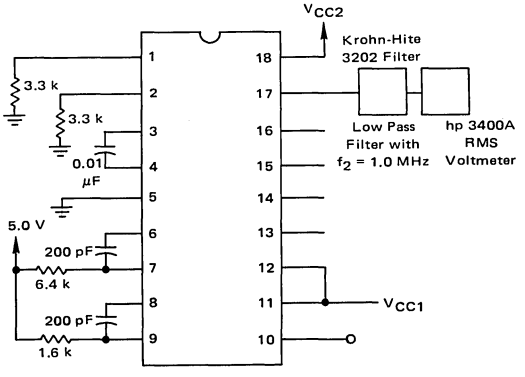


FIGURE 22 – DIFFERENTIAL NOISE VOLTAGE



NOTE: Assume uncorrelated noise sources

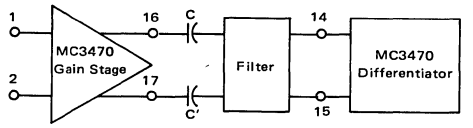
e_n (differential noise at input) = $e_o\sqrt{2/100}$

7

APPLICATION INFORMATION

The MC3470 is designed to accept a differential ac input from the magnetic head of a floppy disk drive and produce a digital output pulse that corresponds to each peak of the ac input. The gain stage amplifies the input waveform and applies it to a filter network (Figure 23a),

FIGURE 23a – BLOCKING CAPACITORS USED TO ISOLATE THE DIFFERENTIATOR



enabling the active differentiator and time domain filter to produce the desired output.

FILTER CONSIDERATIONS

The filter is used to reduce any high frequency noise present on the desired signal. Its characteristics are dictated by the floppy disk system parameters as well as the coupling requirements of the MC3470. The filter design parameters are affected by the read head characteristics, maximum and minimum slew rates, system transient response, system delay distortion, filter center frequency, and other system parameters. This design criteria varies between manufacturers; consequently, the filter configuration also varies. The coupling requirements of the MC3470 are a result of the output structure of the gain stage and the input structure of the differentiator, and must be adhered to regardless of the filter configuration.

The differentiator has an internal biasing network on each input. Therefore, any dc voltage applied to these inputs will perturbate the bias level. Disturbing the bias level does not affect the waveform at the differentiator inputs, but it does cause peak shifting in the digital output (Pin 10). Since the output of the gain stage has an associated dc voltage level, it, as well as any biasing introduced in the filter, must be isolated from the differentiator via series blocking capacitors. The transient response is minimized if the blocking capacitors C and C′ are placed before the filter as shown in Figure 23a. The charging and discharging of C and C′ is controlled by the filter termination resistor instead of the high input impedance of the differentiator.

The filter design must also include the current-sinking capacity of the amplifier output. The current source in the output structure (see circuit schematic – Pins 16 and 17) is guaranteed to sink a current of 2.8 mA. If the current requirement of the filter exceeds 2.8 mA, the current source will saturate, the output waveform will be distorted, and inaccurate peak detection will occur in the differentiator. Therefore, the total impedance of the filter must be greater than Z_{min} as calculated from

$$Z_{min} = \frac{(E_p A_{VD})\ max}{2.8\ mA}$$

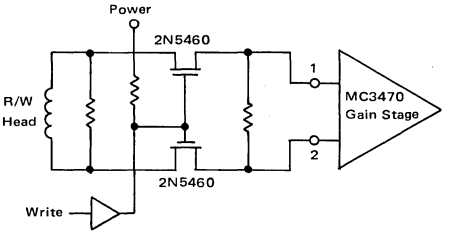
where E_p is the peak differential input voltage to the MC3470.

TRANSIENT RESPONSE

The worst-case transient response of the read channel occurs when dc switching at the amplifier input causes its output to be toggled. The dc voltage changes are a consequence of diode switching that takes place when control is transferred from the write channel to the read channel.

If the diode network is balanced, the dc change is a common mode input voltage to the amplifier. The switching of an unbalanced diode network creates a differential input voltage and a corresponding amplified swing in the outputs. The output swing will charge the blocking capacitor resulting in peak shifting in the digital output until the transient has decayed. Eliminating the differential dc changes at the amplifier input by matching the diode network or by coupling the read head to the amplifier via FET switches, as shown in Figure 23b, will minimize the filter transient response.

FIGURE 23b – FET SWITCHES USED TO COUPLE THE R/W HEAD TO THE MC3470



Two of the advantages FET switches have over diode switching are:

1. They isolate the read channel from dc voltage changes in the system; therefore, the transient response of the filter does not influence the system transient response.
2. The low voltage drop across the FETs keeps the input signal below the amplifier's internal clamp voltage; whereas, the voltage dropped across a diode switching network adds a dc bias to the input signal which may exceed the clamp voltage.

AMPLIFIER GAIN

For some floppy systems, it may become necessary to either reduce the gain of the amplifier or reduce the

See Application Note AN917 for further information.

signal at the input to avoid exceeding the output swing capability of the amplifier. The voltage gain of the amplifier can be reduced by putting a resistor in series with the capacitor between Pins 3 and 4 (Figure 14). The relationship between the gain and the external resistor is given by

$$A_{VR} = A_{VO} \cdot \frac{2(r_e + R_e)}{2(r_e + R_e) + R_{ext}}$$

where $A_{VO} \triangleq$ voltage gain with the external resistor = 0,
$A_{VR} \triangleq$ voltage gain with the external resistor in,
$R_{ext} \triangleq$ the external resistor, and
$r_e + R_e \triangleq$ the resistance looking into Pin 3 or Pin 4.

Thus,

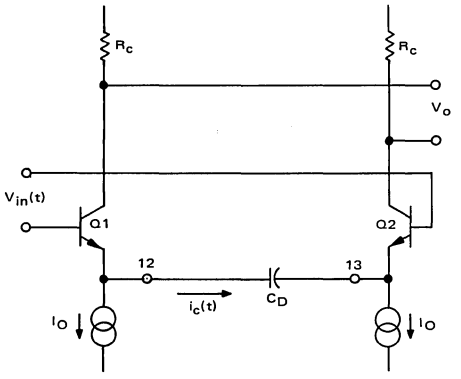
$$R_{ext} = 2\left(\frac{A_{VO}}{A_{VR}} - 1\right)(r_e + R_e).$$

A plot of $(r_e + R_e)$ versus temperature is shown in Figure 21. Figure 20 shows the normalized voltage gain versus temperature with the external resistor equal to 500 ohms.

ACTIVE DIFFERENTIATOR

The active differentiator in the MC3470 (simplified circuit shown in Figure 24), is implemented by coupling

FIGURE 24 – ACTIVE DIFFERENTIATOR NETWORK



the emitters of a differential amplifier with a capacitor resulting in a collector current that will be the derivative of the input voltage,

$$I = C\,dv/dt$$

If the output voltage is taken across a resistor through which the collector current is flowing, the resulting voltage will be the derivative of the input voltage.

$$V_o = 2Ri_c = 2RC\frac{dv_{in}(t)}{dt}$$

V_o is applied to a comparator which will provide zero crossing detection of the current waveform. Since the capacitor shifts the current 90° from the input voltage, the comparator performs peak detection of the input voltage.

The following terms will be used in determining the value of C to be used in the differentiator:

$E_p \triangleq$ peak differential voltage applied to MC3470 amplifier input.

$E_p \sin\omega t \triangleq$ voltage waveform applied to MC3470 amplifier input (for purposes of discussion, assume a sine wave).

$A_{VD} \triangleq$ differential voltage gain of input amplifier.

$v_{in}(t) \triangleq$ differential voltage waveform applied to the differentiator inputs.

$= E_p A_{VD} \sin\omega t$ (Note: The filter is assumed to be lossless.)

$i_c(t) \triangleq$ current through capacitor C_D.

$R_O \triangleq$ output resistance of Q1 (Q2) at Pin 12 (13).

If $v_{in}(t) = E_p A_{VD} \sin\omega t$, then the current through the capacitor C_D is given by

$$i_c(t) = C_D A_{VD} E_p \omega \cos\omega t$$

$$\text{and } V_O(t) = 2R_C C_D A_{VD} E_p \omega \cos\omega t.$$

Accurate zero crossing detection of $V_O(t)$ [peak detection of $v_{in}(t)$] occurs when the current waveform $i_c(t)$ crosses through zero in a minimum amount of time. This condition is satisfied by maximizing current slew rate. For a given value of ω, the maximum slew rate occurs for the maximum value of i_c or $\cos\omega t = 1$. Therefore,

$$i_c = C_D A_{VD} E_p \omega$$

The MC3470 current-sourcing capacity will determine the maximum value i_c; therefore, C_D must be chosen such that the maximum i_c occurs at the maximum $A_{VD}E_p\omega$ product.

$$C_D = \frac{i_{c\,max}}{(A_{VD}E_p\omega)_{max}} = \frac{1\text{ mA}}{(120)(E_p\omega)_{max}}$$

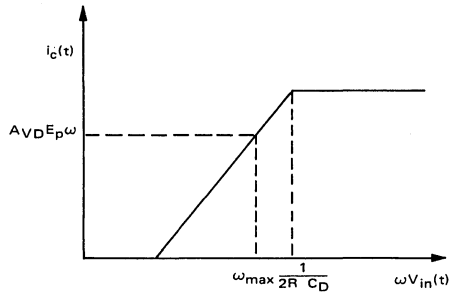
If the peak value specified for i_c is exceeded, the current source (I_O in Figure 24) will saturate and distort the waveform at Pins 12 and 13. Consequently, the differentiator will not accurately locate the peaks and peak shifting will occur in the digital output.

The effective output resistance R_O of Q1 (Q2) will create a pole (as shown in Figure 25) at $1/2\,R_OC_D$. If this pole is ten times greater than the maximum operating frequency (ω_{max}), the phase shift approaches 84°. Locating the pole at a frequency much greater than 10 ω_{max} needlessly extends the noise bandwidth thus:

$$2R_O = \frac{1}{C_D\,10\,\omega_{max}}.$$

If R_O is not large enough to satisfy this condition, a series

FIGURE 25 – RESPONSE OF DIFFERENTIATOR USING ONLY C_D

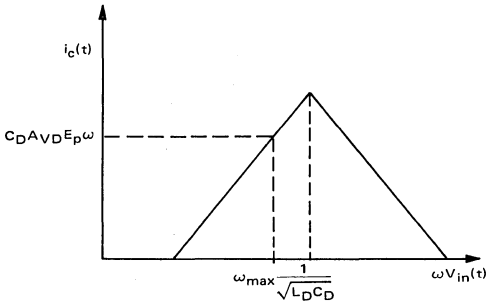


resistor can be added so that

$$R = 2R_O + R_D = \frac{1}{C_D\,10\,\omega_{max}}.$$

To further reduce the noise bandwidth, a second pole can be added (as shown in Figure 26) by putting an

FIGURE 26 – COMPLETE RESPONSE OF DIFFERENTIATOR



inductor in series with the resistor and the capacitor. The values of R and L are determined by choosing the center frequency (ω_o) and the damping ratio (δ) to meet the systems requirements where

$$\omega_o = \frac{1}{\sqrt{LC_D}}$$

$$\delta = \frac{RC_D}{2\sqrt{LC_D}}$$

$$\omega_o = 10\,\omega_{max} = \frac{1}{\sqrt{LC_D}}$$

where C_D is chosen for maximum i_c as shown previously.

Solving for L gives:

$$L = \frac{1}{100\,C_D(\omega_{max})^2}$$

Using this value for L gives:

$$\delta = \frac{RC_D}{\frac{2}{10}\sqrt{\frac{C_D}{C_D(\omega_{max})^2}}}$$

Solving for R gives:

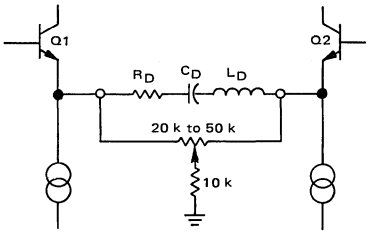
$$R = \frac{\delta}{5\,C_D\,\omega_{max}}$$

The total resistance (R) is the effective output resistance (R_O) plus the resistor added in the differentiator (R_D). Values of δ from 0.3 to 1 produce satisfactory results.

PEAK SHIFT CONSIDERATIONS

Peak shift, resulting from current imbalance in the differentiator, offset voltage in the comparator, etc., can be eliminated by nulling the current in the emitters of the differentiator with a potentiometer as shown in Figure 27.

FIGURE 27 – PEAK SHIFT COMPENSATION



The potentiometer across the differentiator components is adjusted until a symmetrical digital output cycle is obtained at Pin 10 for a sinusoidal input with the minimum anticipated $E_p\omega$ product.

DESIGN EQUATIONS FOR ONE-SHOTS

As shown in Figure 28, the MC3470 input waveform may have distortion at zero crossing, which can result in false triggering of the digital output. The time domain filter in the MC3470 can be used to eliminate the distortion by properly setting the period (t_1) of the one-shot timing elements on Pins 6 and 7. The following equation will optimize immunity to this signal distortion at zero crossing of the read head signal.

The timing equation for the time domain filter's one-shot is:

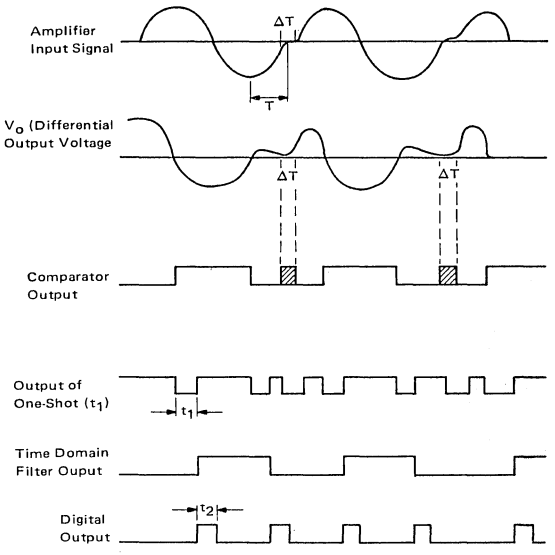
$$t_1 = R_1C_1K_1 + T_o$$

where $K_1 = 0.625$, $T_o = 200$ ns.

Actual time will be within ±15% of t_1 due to variations in the MC3470.

If ΔT is the maximum period of distortion (see Figure

FIGURE 28 – WAVEFORMS THROUGH THE READ CIRCUIT



28), then choose t_1 such that

$$\Delta T < t_1 < T - \frac{\Delta T}{2}$$

where $T = \frac{1}{4f_{(max)}}$.

The width of the digital output pulse t_2 (Pin 10) is determined by

$$t_2 = R_2C_2K_2$$

where $K_2 = 0.625$.

Actual pulse width will be within ±15% of t_2 due to variations in the MC3470.

To preserve the specified accuracy of the MC3470, R_1, R_2, C_1, and C_2 should remain in the ranges shown in the Electrical Characteristics. Also, to minimize current transients, it is important to keep the values of C_1 and C_2 as small as is convenient. For t_1 = 1 μs and t_2 = 200 ns, suggested good values for the capacitors are

C_1 = 250 pF

C_2 = 160 pF

BOARD LAYOUT AND TESTING CONSIDERATIONS

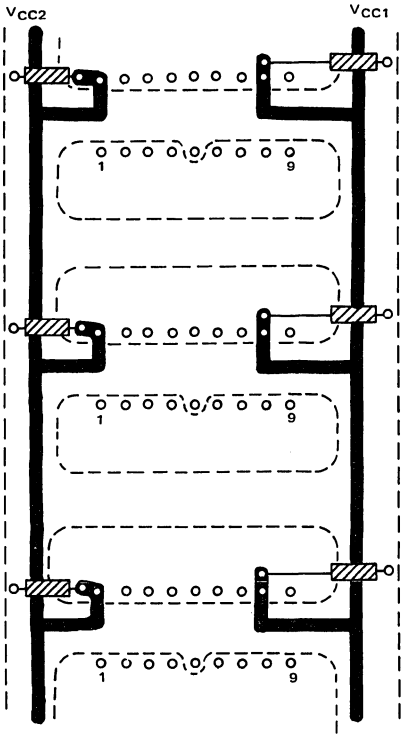
An LSI package has many input/output pins in close proximity, some carrying high level signals and others low level signals. As carefully as the on-chip isolation of the devices connected to these pins is implemented by the manufacturer, the coupling of signals or noise between external wires is under the control of the end-user who designs the integrated circuit into a piece of equipment. The designer should be familiar with the following layout procedures which will optimize the performance of the device. See Figure 29.

1. Build all circuits on printed circuit boards (including breadboards). Transmission line theory for flat conductors in a plane quite convincingly proves that coupling is far less than for round conductors in three dimensions.
2. Use a ground plane under the IC and over as much of the printed circuit board surface as possible without exceeding practical limits.
3. Avoid signal runs under the IC. Also avoid parallel runs of 1 inch or greater on the opposite or same side of board.
4. Use monolithic ceramic 0.1 μF capacitors for decoupling power supply transients: one from V_{CC1} to ground and one from V_{CC2} to ground for each IC package. Keep lead lengths to 1/4 inch or less and place in close proximity to the IC.
5. Keep all signal runs as short as possible.

When evaluating the device for phase jitter and frequency response, a special test jig should be designed to reduce ground loops and coupling caused by instrumentation. Instrumentation test setups must be calibrated

at each test frequency and differential equipment utilized where required. A valid evaluation of the performance of any read amplifier chain requires considerable care and thought.

FIGURE 29 – POWER AND GROUND DISTRIBUTION FOR MC3470 PRINTED CIRCUIT BOARD LAYOUT



NOTE: Dotted lines outline ground plane on back side of printed circuit board.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC3471

FLOPPY DISK WRITE CONTROLLER/HEAD DRIVER

FLOPPY DISK WRITE CONTROLLER (WITH ERASE DELAY)

SILICON MONOLITHIC INTEGRATED CIRCUIT

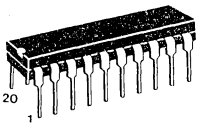
The MC3471 is a monolithic integrated Write Controller/Head Driver designed to provide the entire interface between the write data and head control signals and the heads (write and erase) for either Tunnel or straddle-erase floppy disk systems.

Provisions are made for selecting a range of accurately controlled write currents and for head selection during both read and write operation. Additionally, provisions are included for externally adjusting degauss period, inner/outer track compensation, and the delay from write gate to erase turn-on and turn-off.

Erase Delays are controlled by driving the delay inputs D1 and D2 with standard TTL open-collector logic (microprocessor compatible) or by using the external RC mode in which case the delay is one τ (K factor = 1.0).

In addition, an $\overline{\text{Inhibit}}$ output is provided which indicates that the heads are active during write, degauss, or erase.

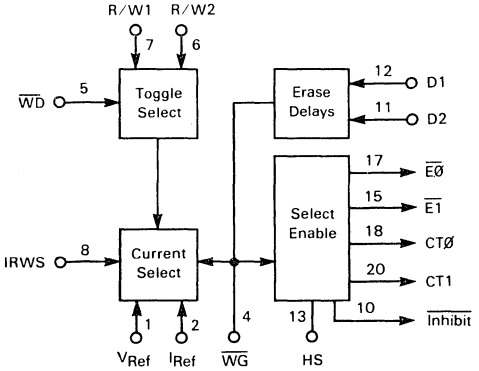
- Head Selection — Current Steering Through Write Head and Erase Coil in Write Mode
- Adjustable On-Chip Delay of Erase Timing — Stable K Factor
- Delay Pins Logic Compatible for Direct Microprocessor Compatibility
- $\overline{\text{Inhibit}}$ Output Provided to Disable Read or Step During Head Active Time
- Provides High Impedance (Read Data Enable) During Read Mode
- Head Current (Write) Guaranteed ±3% (3.0 mA using R_{ext} = 10 kΩ)
- IRW Select Input Provides for Inner/Outer Track Compensation
- Degauss Period Externally Adjustable
- Specified With Head Supply (V_{BB}) from 10.8 V to 26.4 V
- Minimizes External Components
- See Application Note AN917 for Further Information



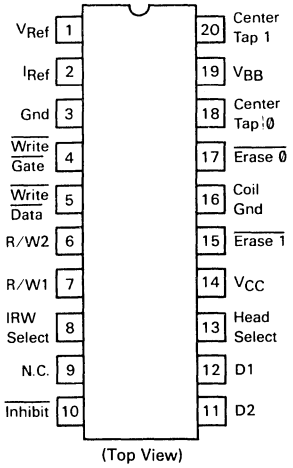
P SUFFIX
PLASTIC PACKAGE
CASE 738

7

BLOCK DIAGRAM



PIN CONNECTIONS



(Top View)

MAXIMUM RATINGS (T_A = 25°C)

Rating	Symbol	Value	Unit
Power Supply Voltage (Pin 14)	V_{CC}	7.0	Vdc
Power Supply Voltage (Pin 19)	V_{BB}	30	Vdc
Input Voltage (Pins 4, 5, 8, 13)	V_I	5.75	Vdc
Output Applied Voltage (Pin 10)	V_O	7.0	Vdc
Open-Collector Sink Current (Pin 10)	I_O	25	mA
Storage Temperature	T_{stg}	-55 to +150	°C
Operating Junction Temperature	T_J	150	°C

RECOMMENDED OPERATING CONDITIONS

Rating	Symbol	Value	Unit
Power Supply Voltage (Pin 14)	V_{CC}	+4.75 to +5.25	Vdc
Power Supply Voltage (Pin 19)	V_{BB}	+10.8 to +26.4	Vdc
Operating Ambient Temperature Range	T_A	0 to +70	°C

ELECTRICAL CHARACTERISTICS (T_A = 0 to +70°C, V_{CC} = 4.75 to 5.25 V, V_{BB} = 10.8 to 26.4 V unless otherwise noted. Typicals given for V_{CC} = 5.0 V, V_{BB} = 12 V and T_A = 25°C unless otherwise noted.)

Characteristics	Pins	Symbol	Min	Typ	Max	Unit
DIGITAL INPUT VOLTAGES						
Power Supply Current — V_{CC} V_{BB}		I_{CC} I_{BB}	— —	22 15	60 30	mA
High Level Input Voltage (V_{CC} = 4.75 V)	4, 8, 13	V_{IH}	2.0	—	—	V
Low Level Input Voltage (V_{CC} = 5.25 V)	4, 8, 13	V_{IL}	—	—	0.8	V
Input Clamp Voltage (I_{IK} = -12 mA)	4, 5, 8, 13	V_{IK}	—	-0.87	-1.5	V
Positive Threshold (V_{CC} = 5.0)	5	$V_{T(+)}$	1.5	1.75	2.0	V
Negative Threshold (V_{CC} = 5.0)	5	$V_{T(-)}$	0.7	0.98	1.3	V
Hysteresis ($V_{T(+)} - V_{T(-)}$) T_A = 0°C to +70°C T_A = 25°C	5	V_{HTS}	 0.2 0.4	 — 0.76	 — —	V
DIGITAL INPUT CURRENTS						
High Level Input Current (V_{CC} = 5.25 V, V_{BB} = 26.4 V, V_I = 2.4 V)	4, 5, 8, 13	I_{IH}	—	0.1	40	μA
Low Level Input Current (V_{CC} = 5.25 V, V_{BB} = 26.4 V, T_A = 25°C unless noted below) V_{BB} = 12 V V_{BB} = 24 V V_{CC} = 5.0 V V_{CC} = 5.0 V	4, 5, 8, 13 4 4 5 8, 13	I_{IL}	 — — — —	 — 0.36 0.76 0.46 0.39	 -1.6 — — — —	mA

ELECTRICAL CHARACTERISTICS (continued) (T_A = 0 to +70°C, V_{CC} = 4.75 to 5.25 V, V_{BB} = 10.8 to 26.4 V unless otherwise noted. Typicals given for V_{CC} = 5.0 V, V_{BB} = 12 V and T_A = 25°C unless otherwise noted.)

Characteristics	Pins	Symbol	Min	Typ	Max	Unit
CENTER-TAP and ERASE OUTPUTS						
Output High Voltage (See Figure 14) (I_{OH} = −100 mA, V_{CC} = 4.75 V) V_{BB} = 10.8 to 26.4 V	18, 20	V_{OH}	V_{BB}-1.5	V_{BB}-1.0	—	V
Output Low Voltage (See Figure 14) (I_{OL} = 1.0 mA) V_{BB} = 12 V V_{BB} = 24 V	18, 20	V_{OL}	 — —	 70 70	 150 150	mV
Output High Leakage Current (V_{OH} = 24 V, V_{CC} = 4.75 V, V_{BB} = 24 V)	15, 17	I_{OH}	—	0.01	100	μA
Output Low Voltage (See Figure 15) (I_{OL} = 90 mA, V_{CC} = 4.75 V) V_{BB} = 12 V V_{BB} = 24 V	15, 17	V_{OL}	 — —	 0.27 0.27	 0.60 0.60	V
DIGITAL OUTPUT LEVEL ($\overline{\text{Inhibit}}$)						
High Level Output Current (V_{OH} = 7.0 V, V_{CC} = 4.75 V)	10	I_{OH}	—	—	100	μA
Low Level Output Voltage (I_{OL} = 4.0 mA, V_{CC} = 4.75 V)	10	V_{OL}	—	—	0.5	V
CURRENT SOURCE						
Reference Voltage	1	V_{Ref}	—	5.7	—	V
Degauss Voltage (See Text) (Voltage Pin 1 - Voltage Pin 2)	1	V_{DEG}	—	1.0	—	V
Bias Voltage	2	V_F	—	0.7	—	V
Write Current Off Leakage (V_{OH} = 30 V)	6, 7	I_{OH}	—	0.03	15	μA
Saturation Voltage (V_{BB} = 12 V)	6, 7	V_{sat}	—	0.85	2.7	V
Current Sink Compliance (For $V_{6,7}$ = 4.0 V to 24 V, $V_{\overline{WG}}$ = 0.8 V)	6, 7	$\triangle I/RW2, 1$	—	15	40	μA
Average Value Write Current $\left(\frac{I_{Pin\ 6} + I_{Pin\ 7}}{2}\right.$ for V_{BB} = 10.8 to 26.4 V) @ $I_{R/W} = I_{LOW}$, R = 10 k T_A = 25°C T_A = 0 to +70°C @ $I_{R/W} = I_{LOW}$, R = 5.0 k T_A = 25°C T_A = 0 to +70°C @ $I_{R/W} = I_{HI}$, R = 10 k ($I_{HI} = I_{LOW}$ + % I_{LOW}) T_A = 25°C T_A = 0 to +70°C	6, 7	 $\overline{I_{R/W(L)}}$ $\overline{\Delta I_{R/W(H)}}$ 	 2.91 2.84 5.64 5.51 31.3 30.3	 3.0 — 5.89 — 33.3 33.3	 3.09 3.16 6.14 6.28 35.5 36.6	 mA %
Difference in Write Current ($\lvert I_{Pin\ 6} - I_{Pin\ 7} \rvert$ @ $I_{R/W} = I_{LOW}$, V_{BB} = 10.8 V to 26.4 V) R = 10 k T_A = 25°C T_A = 0 to +70°C R = 5.0 k T_A = 25°C T_A = 0 to +70°C	6, 7	$I_{R/W\Delta}$	 — — — —	 0.003 — — —	 0.015 0.023 0.030 0.046	mA

ERASE DELAY ACCURACY (V_{CC} = 4.75 to 5.25 V, T_A = 0 to +70°C, V_{BB} = 10.8 to 26.4 V, — refer to Figure 9.)

Characteristics	Test	Min	Typ	Max	Unit
Delay Error, Pin 11, 12 D1, D2 = RC $\pm E_{D1,2}$, 30 kΩ ≤ R ≤ 300 kΩ	$E_{D1,2}$	—	—	15	%

AC SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C, V_{BB} = 24 V, I_{RWS} = 0.4 and $I_{R/W}$ = 3.0 mA unless otherwise noted.)

Characteristics (Note 1)	f_{in} (Note 2)	Min	Typ	Max	Unit
1. Delay from Head Select going low through 0.8 V to CTØ going high through 20 V.	HS, Pin 13	—	1.6	4.0	µs
2. Delay from Head Select going low through 0.8 V to CT1 going low through 1.0 V.	HS, Pin 13	—	2.1	4.0	µs
3. Delay from Head Select going high through 2.0 V to CTØ going low through 1.0 V.	HS, Pin 13	—	1.7	4.0	µs
4. Delay from Head Select going high through 2.0 V to CT1 going high through 20 V.	HS, Pin 13	—	1.4	4.0	µs
5. Delay from $\overline{WG}$ going low through 0.8 V to CT0 going low through 1.0 V.	$\overline{WG}$, Pin 4	—	1.3	4.0	µs
6. Delay from $\overline{WG}$ going low through 0.8 V to CT1 going high through 20 V.	$\overline{WG}$, Pin 4	—	0.8	4.0	µs
7. Delay from $\overline{WG}$ going low through 0.8 V to CT0 going high through 20 V.	$\overline{WG}$, Pin 4	—	0.75	4.0	µs
8. Delay from $\overline{WG}$ going low through 0.8 V to CT1 going low through 1.0 V.	$\overline{WG}$, Pin 4	—	1.2	4.0	µs
9. After $\overline{WG}$ goes high, delay from R/W1 turning off through 10% to CTØ going high through 20 V.	$\overline{WG}$, Pin 4	20	750	—	ns
10. After $\overline{WG}$ goes high, delay from R/W1 turning off through 10% to CT1 going low through 1.0 V.	$\overline{WG}$, Pin 4	20	1200	—	ns
11. After $\overline{WG}$ goes high, delay from R/W2 turning off through 10% to CTØ going low through 1.0 V.	$\overline{WG}$, Pin 4	20	1200	—	ns
12. After $\overline{WG}$ goes high, delay from R/W2 turning off through 10% to CT1 going high through 20 V.	$\overline{WG}$, Pin 4	20	600	—	ns
13. After $\overline{WG}$ goes low, delay from CTØ going low through 1.0 V to R/W1 turning on through 10%.	$\overline{WG}$, Pin 4	20	750	—	ns
14. After $\overline{WG}$ goes low, delay from CT1 going low through 1.0 V to R/W2 turning on through 10%.	$\overline{WG}$, Pin 4	20	750	—	ns
15. After $\overline{WG}$ goes low, fall time (10% to 90%) of R/W1.	$\overline{WG}$, Pin 4	—	5.0	200	ns
16. After $\overline{WG}$ goes low, fall time (10% to 90%) of R/W2.	$\overline{WG}$, Pin 4	—	5.0	200	ns
17. Setup time, Head Select going low before $\overline{WG}$ going low.	$\overline{WG}$, Pin 4	4.0	—	—	µs
18. $\overline{\text{Write Data}}$ low Hold Time	$\overline{WD}$, Pin 5	200	—	—	ns
19. $\overline{\text{Write Data}}$ high Hold Time	$\overline{WD}$, Pin 5	500	—	—	ns
20. Delay from $\overline{WG}$ going high through 2.0 V to R/W 1 turning off through 10% of on value.	$\overline{WG}$, Pin 4	—	3.9	—	µs
21. Delay from $\overline{WG}$ going low thru 0.8 V to $\overline{\text{Inhibit}}$ going low thru 0.5 V	$\overline{WG}$, Pin 4	—	0.08	4.0	µs
22. After $\overline{WG}$ goes high, delay from R/W1 turning off thru 10% to $\overline{\text{Inhibit}}$ going high thru 1.5 V (10 k pullup on Inhibit, Note 3)	$\overline{WG}$, Pin 4	20	750	—	ns
23. After $\overline{WG}$ goes high, delay from $\overline{E1}$ going high thru 23 V to $\overline{\text{Inhibit}}$ going high thru 1.5 V (10 k pullup on Inhibit, Note 3)	$\overline{WG}$	20	750	—	ns

Notes:
1. Test numbers refer to encircled numbers in Figures 3 & 16.
2. AC test waveforms applied to the designated pins as follows:

Pin	f_{in}	Amplitude	Duty Cycle
HS, Pin 13	50 kHz	0.4 to 2.4 V	50%
$\overline{WG}$, Pin 4	50 kHz	0.4 to 2.4 V	50%
$\overline{WD}$, Pin 5	1.0 MHz	0.2 to 2.4 V	50%

3. Test Conditions 22, or 23, whichever produces the longer delay, will control Inhibit.

AC SWITCHING CHARACTERISTICS (continued)
(V_{CC} = 5.0 V, T_A = 25°C, V_{BB} = 24 V, $\overline{WG}$ = 0.4 unless otherwise noted)

Characteristics (Note 4)	Min	Typ	Max	Unit
1. Delay from $\overline{\text{Write Data}}$ going low through 0.9 V to R/W1 turning on through 50%.	—	85	—	ns
2. Delay skew, difference of R/W1 turning off and R/W2 turning on through 50% after $\overline{\text{Write Data}}$ going low through 0.9 V.	—	1.0	±40	ns
3. Delay from $\overline{\text{Write Data}}$ going low through 0.9 V to R/W1 turning off through 50%.	—	80	—	ns
4. Delay skew, difference of R/W1 turning on and R/W2 turning off 50% after $\overline{\text{Write Data}}$ going low through 0.9 V.	—	1.0	±40	ns
5. Fall time, 10% to 90%, of R/W1	—	1.7	200	ns
6. Fall time, 10% to 90%, of R/W2	—	1.7	200	ns
7. Rise time, 90% to 10%, of R/W1	—	12	200	ns
8. Rise time, 90% to 10%, of R/W2	—	12	200	ns

Note 4. Test numbers refer to encircled numbers in Figures 2 & 15.
f_{in} = 1.0 MHz, 50% Duty Cycle and Amplitude of 0.2 V to 2.4 V.

PIN DESCRIPTION TABLE

Name	Symbol	Pin	Description
Head Select	HS	13	Head Select input selects between the head I/O pins; center-tap, erase, and read/write. A HIGH selects Head 0 and a LOW selects Head 1.
$\overline{\text{Write Gate}}$	$\overline{WG}$	4	$\overline{\text{Write Gate}}$ input selects the mode of operation. HIGH selects the read mode, while LOW selects the Write Control mode and forces the write current.
$\overline{\text{Write Data}}$	$\overline{WD}$	5	$\overline{\text{Write Data}}$ input controls the turn on/off of the write current. The internal divide-by-two flip-flop toggles on the negative going edge of this input to direct the current alternately to the two halves of the head coils.
IRW Select	IRWS	8	IRW Select input selects the amount of write current to be used. When LOW, the current equals the value found in Figure 5, according to the external resistor. When HIGH, the current equals the low current + 33%.
V_{Ref} I_{Ref}	V_{Ref} I_{Ref}	1 2	A resistor between these pins sets the write current. (Refer to Figure 4.) A capacitor from V_{Ref} to Gnd will adjust the Degauss period.
Center-Tap 0	CT0	18	Center-Tap 0 output is connected to the center tap of Head 0. It will be pulled to Gnd or V_{BB} (+12 or +24) depending on mode and head selection.
$\overline{\text{Erase 0}}$	$\overline{E0}$	17	$\overline{\text{Erase 0}}$ will be LOW for writing on Head 0, and floating for other conditions.
Center-Tap 1	CT1	20	Center-Tap 1 output is connected to the center tap of Head 1. It will be pulled to Gnd or V_{BB} (+12 or +24) depending on mode and head selection.
$\overline{\text{Erase 1}}$	$\overline{E1}$	15	$\overline{\text{Erase 1}}$ will be LOW for writing on Head 1, and floating for other conditions.
R/W2	R/W2	6	R/W2 input is one of the differential inputs that sinks current during writing, being the opposite phase of R/W1. It will be connected to one side of the heads.
R/W1	R/W1	7	R/W1 input is one of the differential inputs that sinks current during writing, being the opposite phase of R/W2. It will be connected to one side of the heads.
	V_{CC}	14	+5.0 V Power
	V_{BB}	19	+12 V or + 24 V Power
	Gnd	16	Coil grounds
	Gnd	3	Reference and logic ground
Delay 1	D1	12	Erase Turn-On Delay adjust (RC or Logic)
Delay 2	D2	11	Erase Turn-Off Delay adjust (RC or Logic)
Inhibit	$\overline{\text{Inhibit}}$	10	Active low open-collector output provided to indicate heads are active in the write, degauss or erase mode. (Used for step or read inhibit.)

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FIGURE 1 — LOGIC DIAGRAM

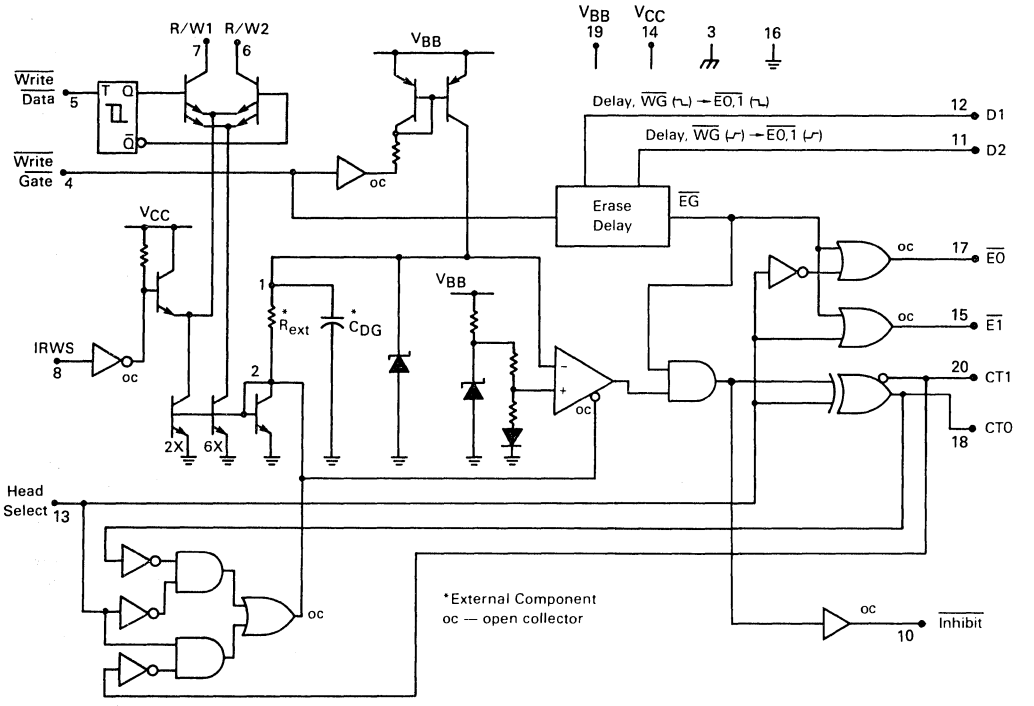


FIGURE 2 — R/W1 AND R/W2 RELATIONSHIP

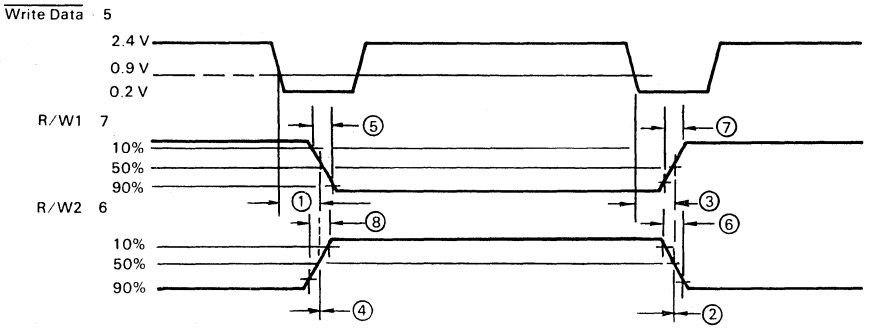


FIGURE 3 — AC TIMING DIAGRAM

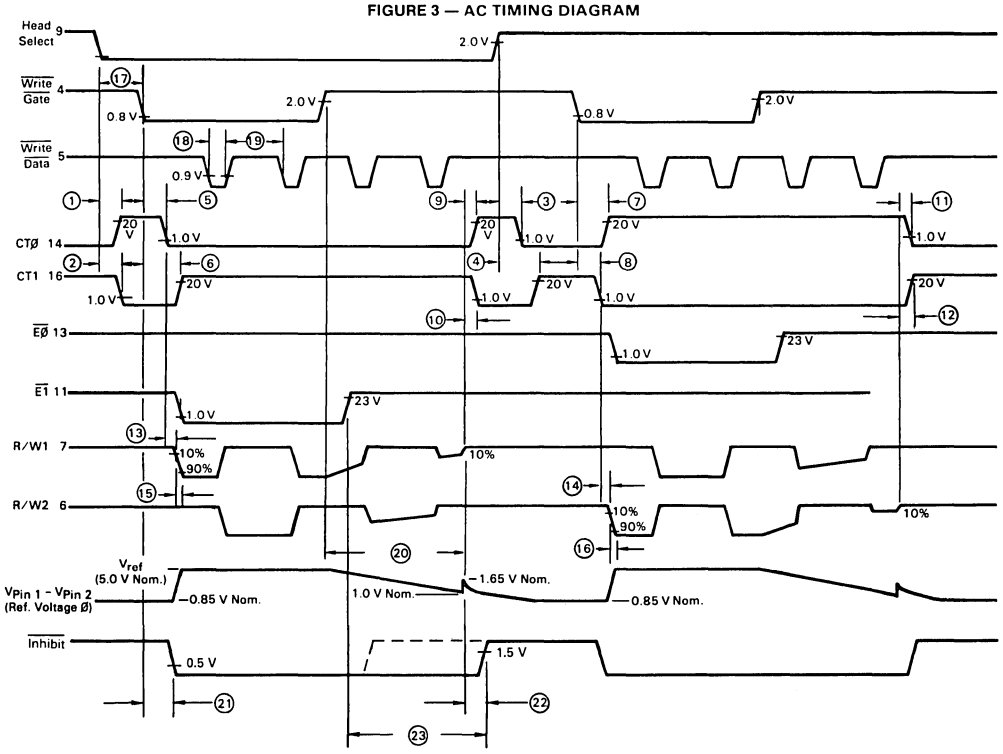
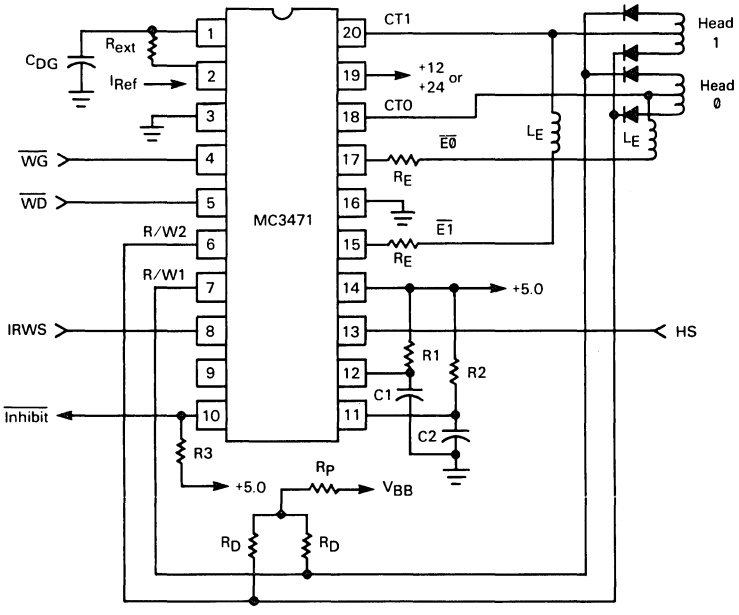


FIGURE 4 — TYPICAL APPLICATION



APPLICATION INFORMATION

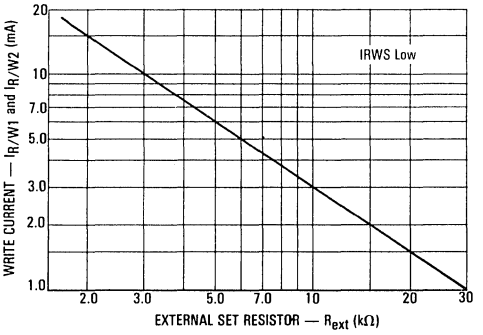
The MC3471P serves as a complete interface between the Write Control functional signals (Head Select, Write Data, Write Gate and inner track compensation, IRWS) and the head itself. A typical configuration is shown in Figure 4. L_E's are erase coils.

WRITE CURRENT SELECTION

Although the MC3471P has been specified for 3.0 mA write current (with a 10 kΩ external resistor), a range of write current values can be chosen by varying R_{ext} using the plot in Figure 5. This current can also be derived using the relationship $I_{Write}\,(mA) = \frac{30}{R_{ext(k\Omega)}}$

I_{Ref}, the current flowing in R_{ext} (required only for dissipation calculations) can be worst case using the fact that the differential voltage between Pins 1 and 2 (V_{Ref}) shown in Figure 3 never exceeds 5.0 volts. With a low value of R_{ext} = 1.0 kΩ, P_D = 25 mW.

FIGURE 5 — WRITE CURRENT versus R_{ext}



WRITE CURRENT DAMPING

Referring to Figure 4, resistors R_D are used to dampen any ringing that results from applying the relatively fast risetime write current pulse to the inductive head load. Values chosen will be a funciton of head characteristics and the desired damping. R_P serves as a common pullup resistor to the head supply V_{BB}.

DEGAUSS PERIOD

Degauss of the read/write head can be accomplished at the end of each write operation by attaching a capacitor from Pin 1 to ground. The time relationship that results is shown in Figure 7. A simplified diagram of this function is shown in Figure 6.

While $\overline{WG}$ is low, the selected write current flows into Pin 6 or Pin 7 (R/W1 or R/W2) and is mirrored through the external resistor, R_{ext}. The degauss capacitor, C_{DG}, will be charged to approximately 5.7 volts. After $\overline{WG}$ goes high, the voltage on C_{DG} begins to decay toward 0.7 V. When the voltage reaches the comparator threshold of 1.7 V, the comparator output triggers the internal logic to completely turn off the write current. At this point, the pulse amplitude on the R/W1 and R/W2 pins has returned to 10% of its maximum value.

Figure 7, Degauss Period shows the relationship between C_{DG} and Degauss Period for R_{ext} = 10 kΩ. This period is equal to the exponential delay time for the voltage as mentioned plus internal delay times.

FIGURE 6 — SIMPLIFIED DEGAUSS CIRCUIT

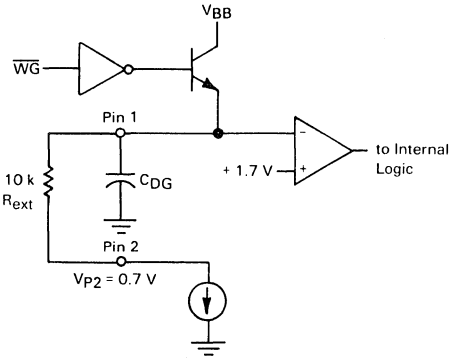
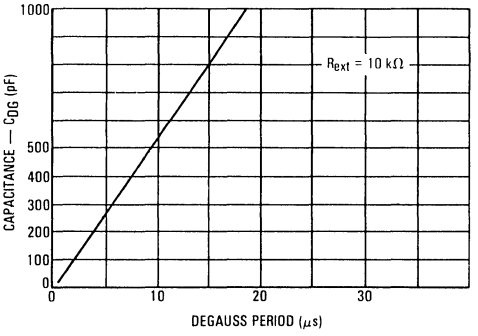


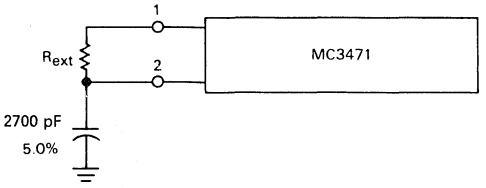
FIGURE 7 — DEGAUSS PERIOD versus CAPACITANCE (C_{DG})



POWER-UP WRITE CURRENT CONTROL

During power-up, under certain conditions (V_{BB} comes up first while $\overline{WG}$ is low), there can be a write current transient on Pins 6 and 7 (R/W1 and R/W2) of sufficient magnitude to cause writing to occur if the head is loaded.

This transient can be eliminated by placing a capacitor from Pin 2 to ground. This also delays the write current when $\overline{WG}$ goes low and this delay must be accounted for when the capacitor on Pin 2 is used. The delay is 3.0 μs for a 2700 pF capacitor, and R_{ext} = 10 kΩ. Values up to 7000 pF may be used.



See Application Note AN917 for further information.

ERASE DELAY

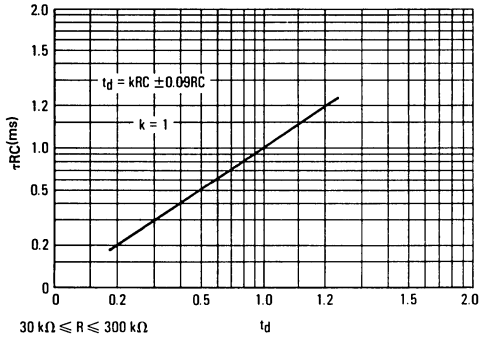
The MC3471P can be used with both straddle and tunnel erase heads. When using the tunnel erase heads, it is necessary to delay the erase current in time with respect to $\overline{WG}$ due to the physical placement of the erase gap behind the R/W gap on the heads. The amount of delay required depends upon the disk rotation velocity, recording density and format. Turn-on delay and turn-off delay must also be independent to guarantee erase is on for the entire block.

Nominal delays of 500 μs turn-on; and 1.0 ms turn-off are available by adjusting the value of R1, R2 and C1, C2 shown in Figure 4. These delays are adjustable over a broad range as shown in Figure 9 to achieve any practical delay required. By using 5% capacitors and 1% resistors, total timing accuracy is better than ± 15% over temperature and supply. Timing is shown in Figure 10.

In applications using logic or microprocessor controlled delays, the D1 and D2 inputs can be used directly to turn-on and turn-off the erase current. (Controlling outputs should be Open-collector w/10 k pullup). Figure 11 shows the relative timing involved for the microprocessor and logic controlled applications.

In straddle erase systems, the erase delays can be eliminated by pulling D1 and D2 high thru a 10 kΩ pullup resistor to +5.0 V.

FIGURE 9 — TYPICAL $\overline{WG}$ TO E0, 1 DELAY versus RC



ERASE CURRENT

The value of R_E, the erase current set resistor, is found by referring to Figure 12 and selecting the desired erase current.

Looking at the simplified erase current path in Figure 12, when writing, CT0 will be high ($V_{OH(min)}$ = 22.5 V) and E0 will be low ($V_{OL(max)}$ = 0.6 V). If the erase coil resistance is 10 Ω and 40 mA of erase current is desired then:

$$(R_E + 10\ \Omega) \times 40\ mA = (22.5 - 0.6)\ V$$

or

$$R_E = \frac{21.9\ V}{0.04\ A} - 10\ \Omega = 537\ \Omega$$

$$P_D = (537)\ (0.04)^2 = 0.86\ W$$

This gives the minimum value R_E for worst case V_{OH}/V_{OL} conditions. It is also recommended that a diode be used as indicated for inductive back emf suppression.

FIGURE 10 — DELAY INPUT FUNCTION/TIMING WITH RC ELEMENTS

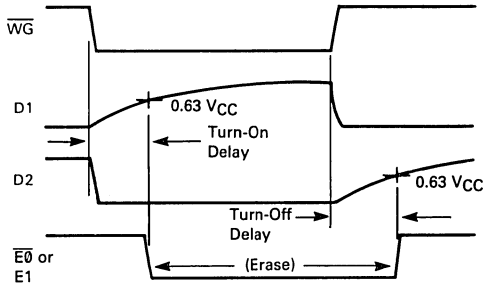


FIGURE 11 — DELAY INPUT FUNCTION/TIMING WITH LOGIC CONTROL

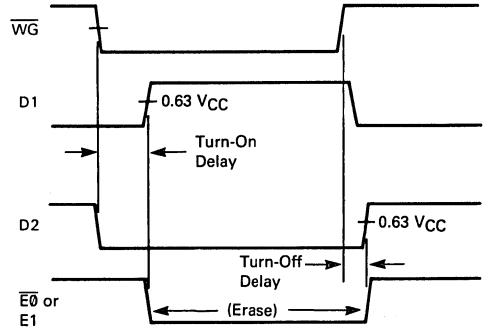


FIGURE 12 — ERASE CURRENT (R_E Selection)

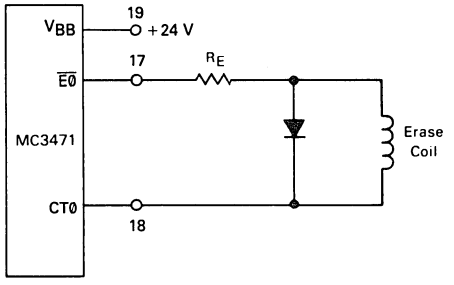
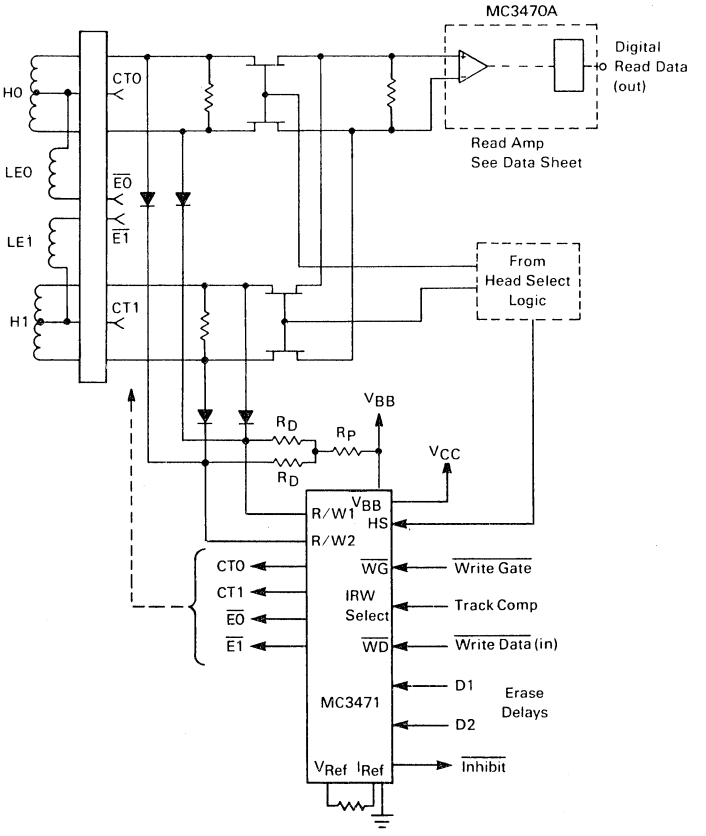


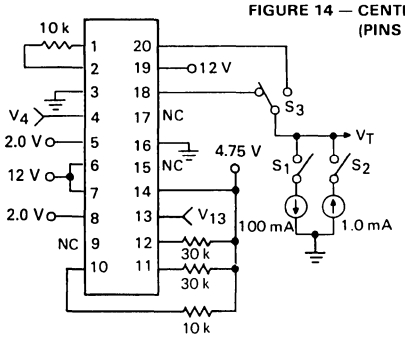
FIGURE 13 — TYPICAL DUAL HEAD FLOPPY DISK SYSTEM USING FET GATE READ CHANNEL SELECTION AND MC3471/MC3470A



Function	CT0	CT1	E0	E1
Write 0	V_{BB}	0 V	On	Off
Write 1	0 V	V_{BB}	Off	On
Read 0	0 V	V_{BB}	Off	Off
Read 1	V_{BB}	0 V	Off	Off

TEST FIGURES

FIGURE 14 — CENTER TAP OUTPUT VOLTAGE (PINS 18 AND 20)

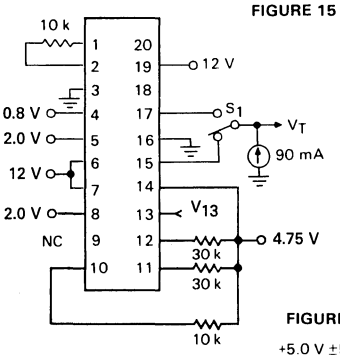


CONDITIONS

Measure V_T	Set S_1	S_2	S_3	V_4*	V_{13}*
V_{OH} (P18)	On	Off	P 18	0.8	2.0
				2.0	0.8
V_{OH} (P20)	On	Off	P 20	2.0	2.0
				0.8	0.8
V_{OL} (P18)	Off	On	P 18	0.8	0.8
				2.0	2.0
V_{OL} (P20)	Off	On	P 20	2.0	0.8
				0.8	2.0

*Volts

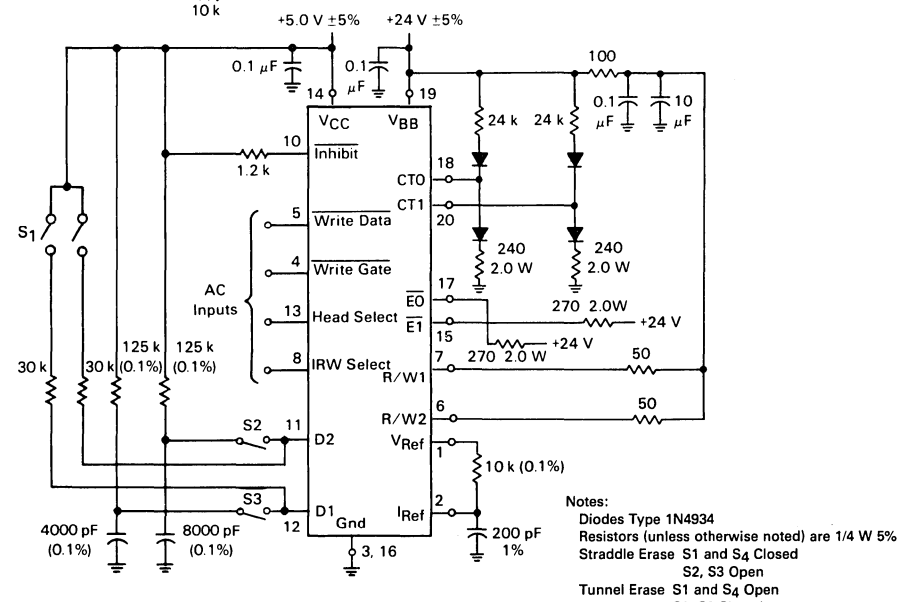
FIGURE 15 — ERASE OUTPUT LOW VOLTAGE (PINS 15 AND 17)



CONDITIONS

Measure V_T	Set S_1	V_{13}
V_{OL} (P15)	P15	0.8V
V_{OL} (P17)	P17	2.0 V

FIGURE 16 — TIMING TEST CIRCUIT



Notes:
Diodes Type 1N4934
Resistors (unless otherwise noted) are 1/4 W 5%
Straddle Erase S1 and S_4 Closed
S2, S3 Open
Tunnel Erase S1 and S_4 Open
S2, S3 Closed

7

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC3481
MC3485

IBM 360/370
QUAD LINE DRIVER

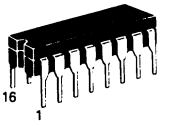
SILICON MONOLITHIC
INTEGRATED CIRCUIT

QUAD SINGLE-ENDED LINE DRIVER

The MC3481 and MC3485 are quad single-ended line drivers specifically designed to meet the IBM 360/370 I/O specification (GA22-6974-3).

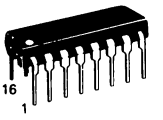
Output levels are guaranteed over the full range of output load and fault conditions. Compliance with the IBM requirements for fault protection, flagging, and power up/power down protection for the bus make this an ideal line driver for party line operations.

- Separate Enable and Fault Flags — MC3481
- Common Enable and Fault Flag — MC3485
- Power Up/Down Does Not Disturb Bus
- Schottky Circuitry for High-Speed — PNP Inputs
- Internal Bootstraps for Faster Rise Times
- Driver Output Current Foldback Protection
- MC3485 has LS Totem Pole Driver Output

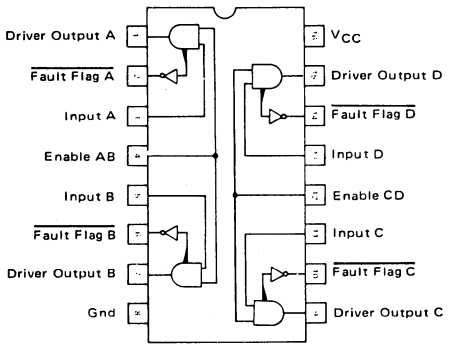


L SUFFIX
CERAMIC PACKAGE
CASE 620

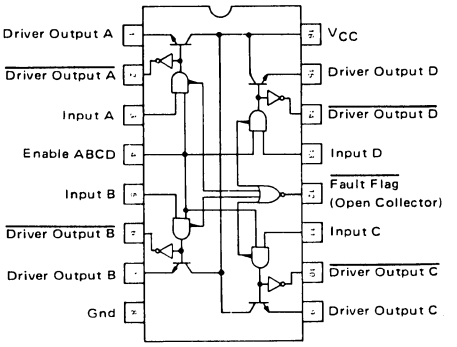
P SUFFIX
PLASTIC PACKAGE
CASE 648



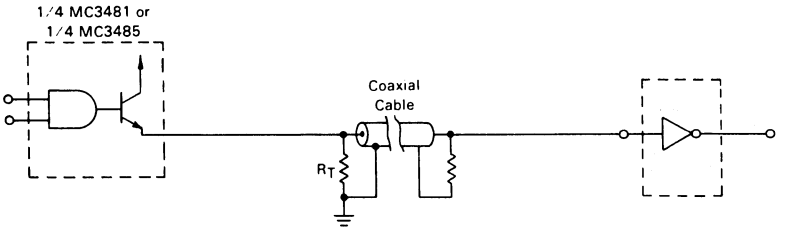
MC3481
DUAL ENABLE
INDIVIDUAL FAULT FLAG



MC3485
COMMON ENABLE
COMMON FAULT FLAG



TYPICAL APPLICATION



MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+7.0	V
Input Voltage	V_I	10	V
Driver Output Voltage	V_O	5.5	V
Power Dissipation (Package Limitation) Ceramic Package Plastic Package Derate Above T_A = 25°C	P_D $1/R_{\theta JA}$	 1150 962 7.7	 mW mW/°C
Operating Ambient Temperature Range	T_A	0 to +70	°C
Junction Temperature Ceramic Package Plastic Package	T_J	+175 +150	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	V_{CC}	4.5	5.0	5.95	Vdc
High Level Output Current	I_{OH}	—	—	−59.3	mA
Operating Ambient Temperature Range	T_A	0	—	+70	°C

SWITCHING CHARACTERISTICS (See Note 1. Unless otherwise noted, these specifications apply over recommended temperature range. I/O Driver characteristics are guaranteed for V_{CC} = 5.0 V ±10% and Select-Out Driver characteristics are guaranteed for V_{CC} = 5.25 to 5.95 V. Typical values measured at T_A = 25°C and V_{CC} = 5.0 V. See Tables 1 and 2, Figures 1 and 2 for load conditions.)

Characteristics	Symbol	Min	Typ	Max	Unit
Propagation Delay Time					ns
High-to-Low-Level, Driver Output					
As I/O Driver	$t_{PHL(D)}$	—	18	—	
As Select-Out Driver	$t_{PHL(DS)}$	—	19	—	
Low-to-High-Level, Driver Output					
As I/O Driver	$t_{PLH(D)}$	—	20	—	
As Select-Out Driver	$t_{PLH(DS)}$	—	21	—	
High-to-Low-Level, $\overline{\text{Driver Output}}$					
As I/O Driver	$t_{PHL(\overline{D})}$	—	25	—	
As Select-Out Driver	$t_{PHL(\overline{DS})}$	—	26	—	
Low-to-High-Level, $\overline{\text{Driver Output}}$					
As I/O Driver	$t_{PLH(\overline{D})}$	—	25	—	
As Select-Out Driver	$t_{PLH(\overline{DS})}$	—	26	—	
High-to-Low-Level, $\overline{\text{Fault Flag}}$ — MC3481					
As I/O Driver	$t_{PHL(\overline{F})}$	—	45	—	
As Select-Out Driver	$t_{PHL(\overline{FS})}$	—	47	—	
Low-to-High-Level, $\overline{\text{Fault Flag}}$ — MC3481					
As I/O Driver	$t_{PLH(\overline{F})}$	—	40	—	
As Select-Out Driver	$t_{PLH(\overline{FS})}$	—	42	—	
Ratio of Propagation Delay Times As I/O Driver	$\frac{t_{PLH(D)}}{t_{PHL(D)}}$	—	1.0	—	

Notes 1. Reference IBM specification GA22-6974-3 for test terminology.

2. The fault protection circuitry of the MC3481/85 requires relatively clean input voltage waveforms for current operation. Noise pulses which enter the threshold region (0.8 to 2.0 V) may cause the output to enter the fault protect mode. To exit the protect mode, it is necessary to gate an input of the effected driver to the low logic state.

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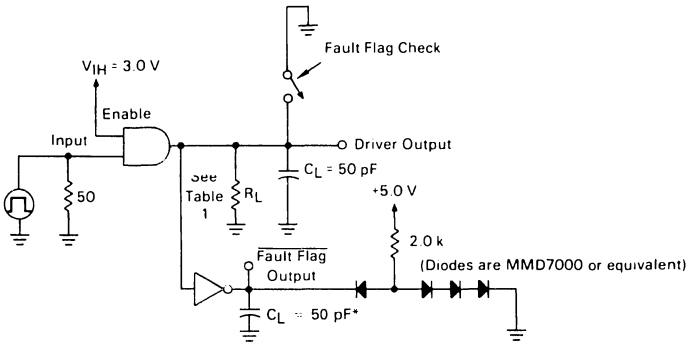
ELECTRICAL CHARACTERISTICS (Unless otherwise noted, these specifications apply over recommended power supply and temperature ratings. Typical values measured at T_A = 25°C and V_{CC} = +5.0 V)

Characteristic	Symbol	MC3481			MC3485			Unit
		Min	Typ	Max	Min	Typ	Max	
High-Level Input Voltage Note 2	V_{IH}	2.0	—	—	2.0	—	—	V
Low-Level Input Voltage Note 2	V_{IL}	—	—	0.8	—	—	0.8	V
High-Level Input Current	I_{IH}							μA
(V_{CC} = 4.5 V, V_{IH} = 2.7 V) - Input		—	—	20	—	—	20	
Enable		—	—	40	—	—	80	
(V_{CC} = 4.5 V, V_{IH} = 5.5 V) - Input		—	—	100	—	—	100	
Enable		—	—	200	—	—	400	
Low-Level Input Current	I_{IL}							μA
(V_{CC} = 5.95 V, V_{IL} = 0.4 V) - Input		—	—	-250	—	—	-250	
Enable		—	—	-500	—	—	-1000	
Input Clamp Voltage	V_{IC}							V
(I_{IC} = -18 mA)		—	—	-1.5	—	—	-1.5	
High-Level Driver Output Voltage								V
(V_{CC} = 4.5 V, V_{IH} = 2.0 V, I_{OH} = -59.3 mA)	$V_{OH(D)}$	3.11	3.6	—	3.11	3.6	—	
(V_{CC} = 5.25 V, V_{IH} = 2.0 V, I_{OH} = -41 mA)	$V_{OH(DS)}$	3.9	—	—	3.9	—	—	
Low-Level Driver Output Voltage								V
(V_{CC} = 5.5 V, V_{IL} = 0.8 V, I_{OL} = -240 μA)	$V_{OL(D)}$	—	—	+0.15	—	—	+0.15	
(V_{CC} = 5.95 V, V_{IL} = 0.8 V, I_{OL} = -1.0 mA)	$V_{OL(DS)}$	—	—	+0.15	—	—	+0.15	
Driver Output Short Circuit Current								mA
(V_{CC} = 5.5 V, V_{IH} = 2.0 V, V_{OS} = 0 V)	$I_{OS(D)}$	—	—	-5.0	—	—	-5.0	
(V_{CC} = 5.95 V, V_{IH} = 2.0 V, V_{OS} = 0 V)	$I_{OS(DS)}$	—	—	-5.0	—	—	-5.0	
Driver Output Reverse Leakage Current								μA
(V_{CC} = 4.5 V, V_{IL} = 0 V, V_O = 3.11 V)	I_{OR1}	—	—	+100	—	—	+100	
(V_{CC} = 0 V, V_{IL} = 0 V, V_O = 3.11 V)	I_{OR2}	—	—	+200	—	—	+200	
High-Level $\overline{\text{Driver Output}}$ Voltage	$V_{OH(\overline{D})}$	—	—	—	2.5	3.0	—	V
(V_{CC} = 4.5 V, V_{IL} = 0.8 V, I_{OH} = -400 μA)								
Low-Level $\overline{\text{Driver Output}}$ Voltage	$V_{OL(\overline{D})}$	—	—	—	—	—	0.5	V
(V_{CC} = 4.5 V, V_{IH} = 2.0 V, I_{OL} = +8.0 mA)								
$\overline{\text{Driver Output}}$ Short Circuit Current								mA
(V_{CC} = 5.5 V, V_{OS} = 0 V, only one output shorted at a time)	$I_{OS(\overline{D})}$	—	—	—	-15	-60	-100	
(V_{CC} = 5.95 V, V_{OS} = 0 V, only one output shorted at a time)	$I_{OS(\overline{D}S)}$	—	—	—	-15	—	-110	
High-Level $\overline{\text{Fault Flag}}$ Output Voltage	$V_{OH(\overline{F})}$	2.5	3.0	—	—	—	—	V
(V_{CC} = 4.5 V, I_{OH} = -400 μA)								
Low-Level $\overline{\text{Fault Flag}}$ Output Voltage	$V_{OL(\overline{F})}$	—	—	0.5	—	—	0.5	V
(V_{CC} = 4.5 V, V_{IH} = 2.0 V, I_{OL} = +8.0 mA, Driver Output shorted to Ground								
$\overline{\text{Fault Flag}}$ Output Short Circuit Current								mA
(V_{CC} = 5.5 V, V_{OS} = 0 V, only one output shorted at a time)	$I_{OS(\overline{F})}$	-15	—	-100	—	—	—	
(V_{CC} = 5.95 V, V_{OS} = 0 V, only one output shorted at a time)	$I_{OS(\overline{F}S)}$	-15	—	-110	—	—	—	
High-Level $\overline{\text{Fault Flag}}$ Output Current	$I_{OH(\overline{F})}$	—	—	—	—	—	+100	μA
(V_{CC} = 5.95 V, V_{OH} = 5.95 V)								
High-Level Power Supply Current								mA
(V_{CC} = 5.5 V, V_{IH} = 2.0 V, no output loading)	I_{CCH}	—	50	70	—	55	75	
(V_{CC} = 5.95 V, V_{IH} = 2.0 V, no output loading)	I_{CCHS}	—	—	80	—	—	85	
Low-Level Power Supply Current								mA
(V_{CC} = 5.5 V, V_{IL} = 0.8 V, no output loading)	I_{CCL}	—	35	55	—	35	55	
(V_{CC} = 5.95 V, V_{IL} = 0.8 V, no output loading)	I_{CCLS}	—	—	70	—	—	70	

7

FIGURE 1 — MC3481 AC TEST CIRCUIT AND WAVEFORMS



* Load Capacitance shown includes Fixture and Probe Capacitance

Table 1	Driver Application	
	I/O	Select-Out
V_{OH}	3.11 V	3.9 V
Input Frequency	5 MHz	1 MHz
Input Pulse Width	100 ns	500 ns
Input Amplitude	0 V to 4 V	0 V to 4 V
Input t_{TLH}	≤6 ns	≤ 6 ns
Input t_{THL}	≤6 ns	≤6 ns
Load Resistance (R_L)	50	90

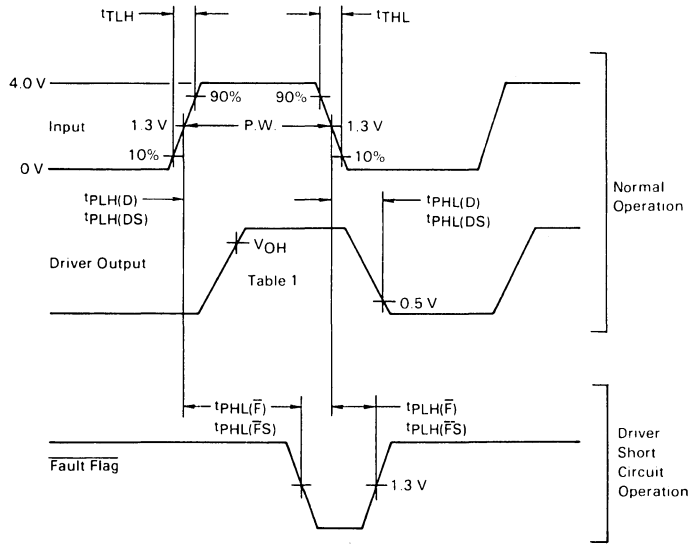


FIGURE 2 — MC3485 AC TEST CIRCUIT AND WAVEFORMS

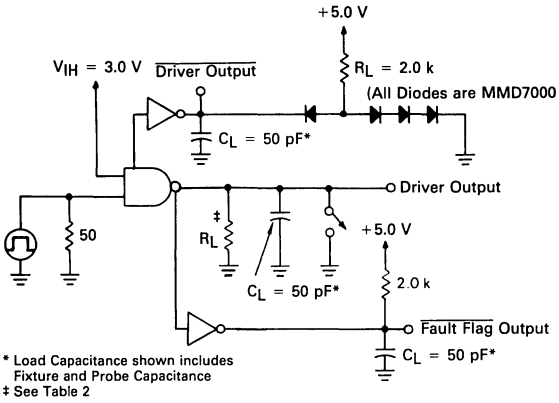


Table 2	Driver Application	
	I/O	Select-Out
V_{OH}	3.11 V	3.9 V
Input Frequency	5 MHz	1 MHz
Input Pulse Width	100 ns	500 ns
Input Amplitude	0 V to 4 V	0 V to 4 V
Input t_{TLH}	≤6 ns	≤6 ns
Input t_{THL}	≤6 ns	≤6 ns
Load Resistance (R_L)	50	90

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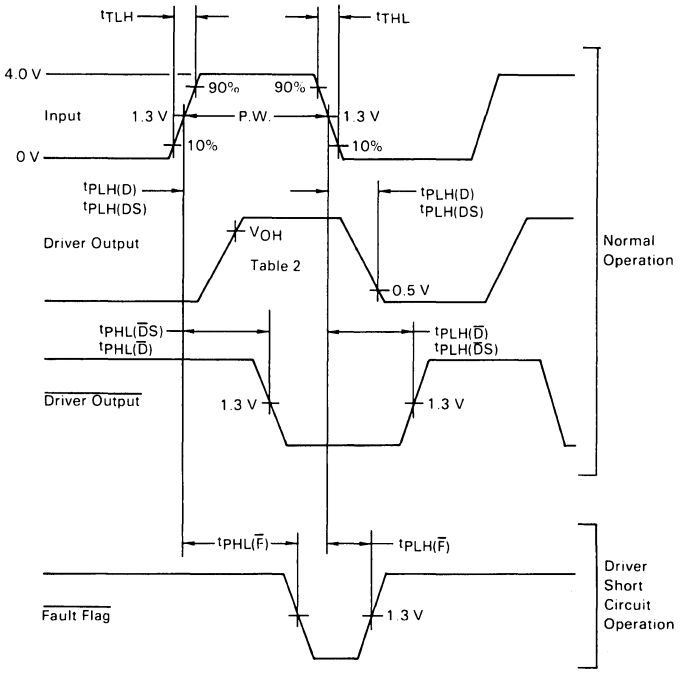


MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC3486

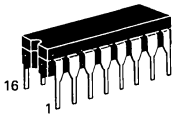
QUAD EIA-422/3 LINE RECEIVER WITH THREE-STATE OUTPUTS

SILICON MONOLITHIC INTEGRATED CIRCUIT

QUAD EIA-422/423 LINE RECEIVER

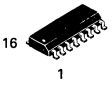
Motorola's Quad EIA-422/3 Receiver features four independent receiver chains which comply with EIA Standards for the Electrical Characteristics of Balanced/Unbalanced Voltage Digital Interface Circuits. Receiver outputs are 74LS compatible, three-state structures which are forced to a high impedance state when the appropriate output control pin reaches a logic zero condition. A PNP device buffers each output control pin to assure minimum loading for either logic one or logic zero inputs. In addition, each receiver chain has internal hysteresis circuitry to improve noise margin and discourage output instability for slowly changing input waveforms. A summary of MC3486 features include:

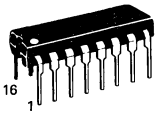
- Four Independent Receiver Chains
- Three-State Outputs
- High Impedance Output Control Inputs (PIA Compatible)
- Internal Hysteresis −30 mV (Typ) @ Zero Volts Common Mode
- Fast Propagation Times −25 ns (Typ)
- TTL Compatible
- Single 5.0 V Supply Voltage
- DS 3486 Provides Second Source



L SUFFIX
CERAMIC PACKAGE
CASE 620

D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO-16)

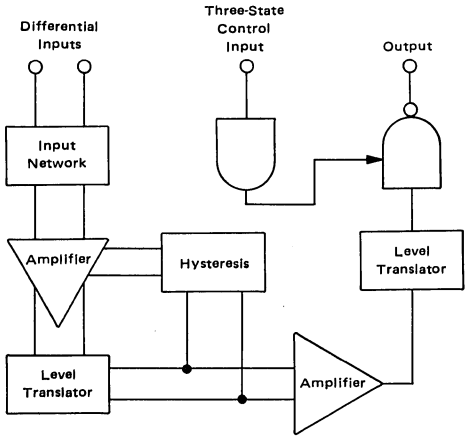




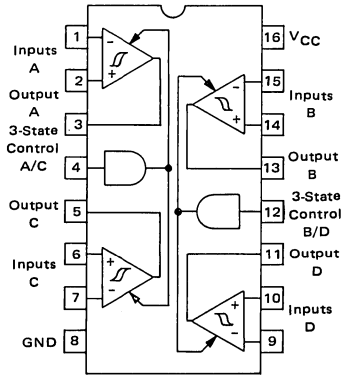
P SUFFIX
PLASTIC PACKAGE
CASE 648

7

RECEIVER CHAIN BLOCK DIAGRAM



PIN CONNECTIONS



ORDERING INFORMATION

Device	Temperature Range	Package
MC3486L	0 to +70°C	Ceramic DIP
MC3486P		Plastic DIP
MC3486D		SO-16

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	8.0	Vdc
Input Common Mode Voltage	V_{ICM}	±15	Vdc
Input Differential Voltage	V_{ID}	±25	Vdc
Three-State Control Input Voltage	V_I	8.0	Vdc
Output Sink Current	I_O	50	mA
Storage Temperature	T_{stg}	-65 to +150	°C
Operating Junction Temperature Ceramic Package Plastic Package	T_J	 +175 +150	°C

RECOMMENDED OPERATING CONDITIONS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	4.75 to 5.25	Vdc
Operating Ambient Temperature	T_A	0 to +70	°C
Input Common Mode Voltage Range	V_{ICR}	-7.0 to +7.0	Vdc
Input Differential Voltage Range	V_{IDR}	6.0	Vdc

ELECTRICAL CHARACTERISTICS (Unless otherwise noted minimum and maximum limits apply over recommended temperature and power supply voltage ranges. Typical values are for T_A = 25°C, V_{CC} = 5.0 V and V_{IK} = 0 V. See Note 1.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Voltage — High Logic State (Three-State Control)	V_{IH}	2.0	—	—	V
Input Voltage — Low Logic State (Three-State Control)	V_{IL}	—	—	0.8	V
Differential Input Threshold Voltage, Note 2 (−7.0 V ≤ V_{IC} ≤ 7.0 V, V_{IH} = 2.0 V) (I_O = −0.4 mA, V_{OH} ≥ 2.7 V) (I_O = 8.0 mA, V_{OL} ≥ 0.5 V)	$V_{TH(D)}$	 — —	 — —	 0.2 −0.2	V
Input Bias Current (V_{CC} = 0 V or 5.25) (Other Inputs at 0 V) (V_I = −10 V) (V_I = −3.0 V) (V_I = +3.0 V) (V_I = +10 V)	$I_{IB(D)}$	 — — — —	 — — — —	 −3.25 −1.50 +1.50 +3.25	mA
Input Balance and Output Level (−7.0 V ≤ V_{IC} ≤ 7.0 V, V_{IH} = 2.0 V, Note 3) (I_O = −0.4 mA, V_{ID} = 0.4 V) (I_O = 8.0 mA, V_{ID} = −0.4 V)	 V_{OH} V_{OL}	 2.7 —	 — —	 — 0.5	V
Output Third State Leakage Current ($V_{I(D)}$ = +3.0 V, V_{IL} = 0.8 V, V_{OL} = 0.5 V) ($V_{I(D)}$ = −3.0 V, V_{IL} = 0.8 V, V_{OH} = 2.7 V)	I_{OZ}	 — —	 — —	 −40 40	μA
Output Short-Circuit Current ($V_{I(D)}$ = 3.0 V, V_{IH} = 2.0 V, V_O = 0 V, Note 4)	I_{OS}	−15	—	−100	mA
Input Current — Low Logic State (Three-State Control) (V_{IL} = 0.5 V)	I_{IL}	—	—	−100	μA
Input Current — High Logic State (Three-State Control) (V_{IH} = 2.7 V) (V_{IH} = 5.25 V)	I_{IH}	 — —	 — —	 20 100	μA
Input Clamp Diode Voltage (Three-State Control) (I_{IK} = −10 mA)	V_{IK}	—	—	−1.5	V
Power Supply Current (V_{IL} = 2.0 V)	I_{CC}	—	—	85	mA

NOTES:
1. All currents into device pins are shown as positive, out of device pins are negative. All voltages referenced to ground unless otherwise noted.
2. Differential input threshold voltage and guaranteed output levels are done simultaneously for worst case.
3. Refer to EIA-422/3 for exact conditions. Input balance and guaranteed output levels are done simultaneously for worst case.
4. Only one output at a time should be shorted.

SWITCHING CHARACTERISTICS (Unless otherwise noted, V_{CC} = 5.0 V and T_A = 25°C.)

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Time — Differential Inputs to Output					ns
(Output High to Low)	$t_{PHL(D)}$	–	–	35	
(Output Low to High)	$t_{PLH(D)}$	–	–	30	
Propagation Delay time — Three-State Control to Output					ns
(Output Low to Third State)	t_{PLZ}	–	–	35	
(Output High to Third State)	t_{PHZ}	–	–	35	
(Output Third State to High)	t_{PZH}	–	–	30	
(Output Third State to Low)	t_{PZL}	–	–	30	

FIGURE 1 — SWITCHING TEST CIRCUIT AND WAVEFORMS

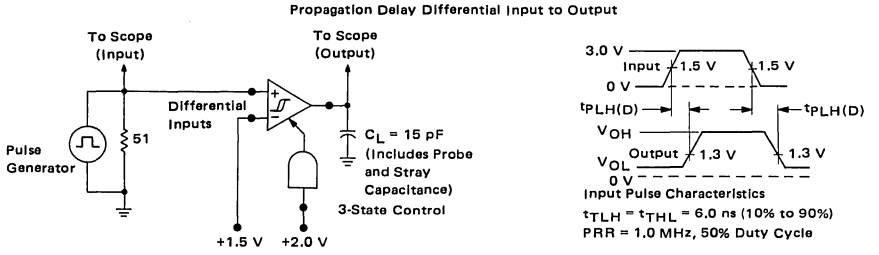
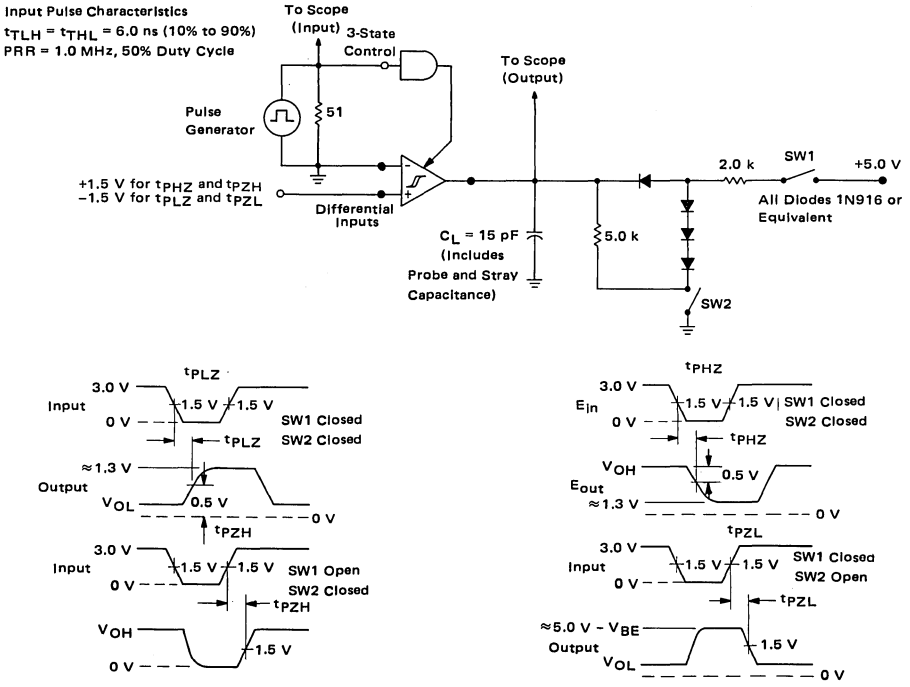


FIGURE 2 — PROPAGATION DELAY THREE-STATE CONTROL INPUT TO OUTPUT



MC3487

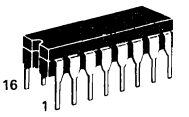
QUAD EIA-422 LINE DRIVER WITH THREE-STATE OUTPUTS

SILICON MONOLITHIC INTEGRATED CIRCUIT

QUAD LINE DRIVER WITH THREE-STATE OUTPUTS

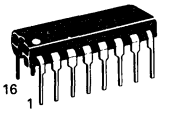
Motorola's Quad EIA-422 Driver features four independent driver chains which comply with EIA Standards for the Electrical Characteristics of Balanced Voltage Digital Interface Circuits. The outputs are three-state structures which are forced to a high impedance state when the appropriate output control pin reaches a logic zero condition. All input pins are PNP buffered to minimize input loading for either logic one or logic zero inputs. In addition, internal circuitry assures a high impedance output state during the transition between power up and power down. A summary of MC3487 features include:

- Four Independent Driver Chains
- Three-State Outputs
- PNP High Impedance Inputs (PIA Compatible)
- Fast Propagation Times (Typ 15 ns)
- TTL Compatible
- Single 5 V Supply Voltage
- Output Rise and Fall Times Less Than 20 ns
- DS 3487 Provides Second Source



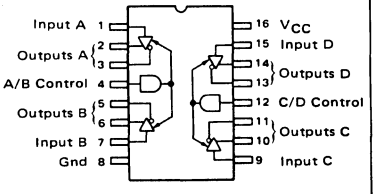
L SUFFIX
CERAMIC PACKAGE
CASE 620

D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO-16)

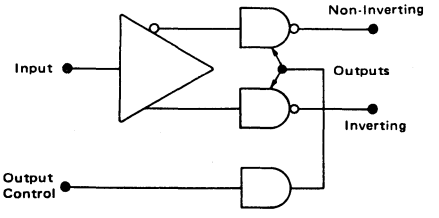


P SUFFIX
PLASTIC PACKAGE
CASE 648

PIN CONNECTIONS



DRIVER BLOCK DIAGRAM



TRUTH TABLE

Input	Control Input	Non-Inverting Output	Inverting Output
H	H	H	L
L	H	L	H
X	L	Z	Z

L = Low Logic State
H = High Logic State
X = Irrelevant
Z = Third-State (High Impedance)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	8.0	Vdc
Input Voltage	V_I	5.5	Vdc
Operating Ambient Temperature Range	T_A	0 to +70	°C
Operating Junction Temperature Range Ceramic Package Plastic Package	T_J	 175 150	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (Unless otherwise noted specifications apply 4.75 V ≤ V_{CC} ≤ 5.25 V and 0°C ≤ T_A ≤ 70°C. Typical values measured at V_{CC} = 5.0 V, and T_A = 25°C.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Voltage – Low Logic State	V_{IL}	–	–	0.8	Vdc
Input Voltage – High Logic State	V_{IH}	2.0	–	–	Vdc
Input Current – Low Logic State (V_{IL} = 0.5 V)	I_{IL}	–	–	-400	μA
Input Current – High Logic State	I_{IH}				μA
(V_{IH} = 2.7 V)		–	–	+50	
(V_{IH} = 5.5 V)		–	–	+100	
Input Clamp Voltage (I_{IK}=-18 mA)	V_{IK}	–	–	-1.5	V
Output Voltage – Low Logic State (I_{OL} = 48 mA)	V_{OL}	–	–	0.5	V
Output Voltage – High Logic State (I_{OH} = -20 mA)	V_{OH}	2.5	–	–	V
Output Short-Circuit Current (V_{IH} = 2.0 V, Note 1)	I_{OS}	-40	–	-140	mA
Output Leakage Current – Hi-Z State	$I_{OL(Z)}$				μA
(V_{IL} = 0.5 V, $V_{IL(Z)}$ = 0.8 V)		–	–	±100	
(V_{IH} = 2.7 V, $V_{IL(Z)}$ = 0.8 V)		–	–	±100	
Output Leakage Current – Power OFF	$I_{OL(off)}$				μA
(V_{OH} = 6.0 V, V_{CC} = 0 V)		–	–	+100	
(V_{OL} = -0.25 V, V_{CC} = 0 V)		–	–	-100	
Output Offset Voltage Difference (Note 2)	$V_{OS}-\overline{V_{OS}}$	–	–	±0.4	V
Output Differential Voltage (Note 2)	V_{OD}	2.0	–	–	V
Output Differential Voltage Difference (Note 2)	$\lvert\Delta V_{OD}\rvert$	–	–	±0.4	V
Power Supply Current					mA
(Control Pins = Gnd, Note 3)	I_{CCX}	–	–	105	
(Control Pins = 2.0 V)	I_{CC}	–	–	85	

Notes: 1. Only one output may be shorted at a time.
2. See EIA Specification EIA-422 for exact test conditions.
3. Circuit in three-state condition.

SWITCHING CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Times					ns
High to Low Output	t_{PHL}	–	–	20	
Low to High Output	t_{PLH}	–	–	20	
Output Transition Times – Differential					ns
High to Low Output	t_{THL}	–	–	20	
Low to High Output	t_{TLH}	–	–	20	
Propagation Delay – Control to Output					ns
(R_L = 200 Ω, C_L = 50 pF)	$t_{PHZ(E)}$	–	–	25	
(R_L = 200 Ω, C_L = 50 pF)	$t_{PLZ(E)}$	–	–	25	
(R_L = ∞, C_L = 50 pF)	$t_{PZH(E)}$	–	–	30	
(R_L = 200 Ω, C_L = 50 pF)	$t_{PZL(E)}$	–	–	30	

FIGURE 1 – THREE-STATE ENABLE TEST CIRCUIT AND WAVEFORMS

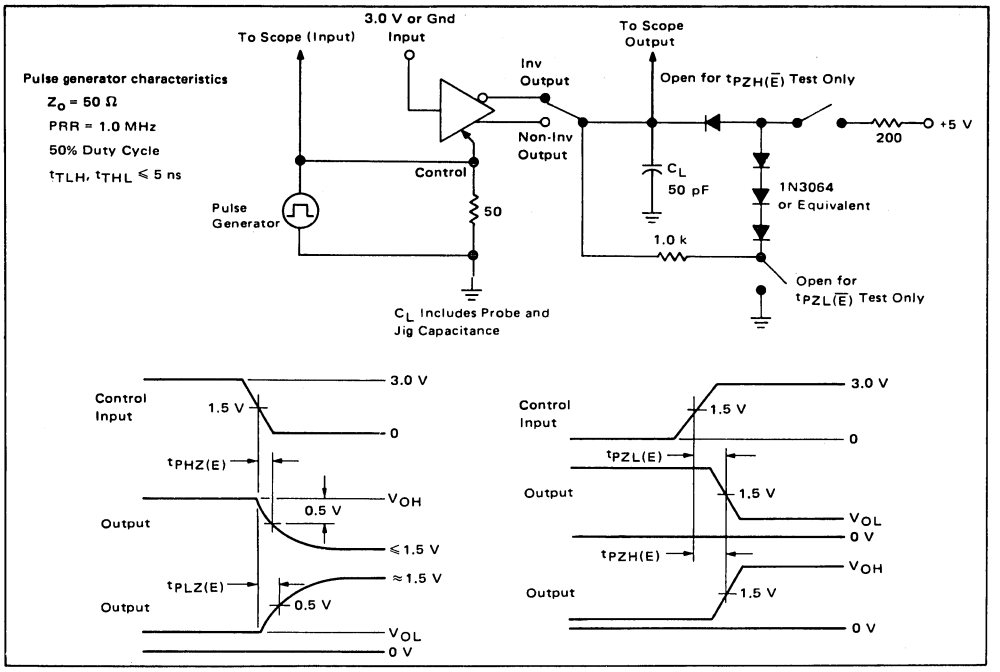


FIGURE 2 – PROPAGATION DELAY TIMES INPUT TO OUTPUT WAVEFORMS AND TEST CIRCUIT

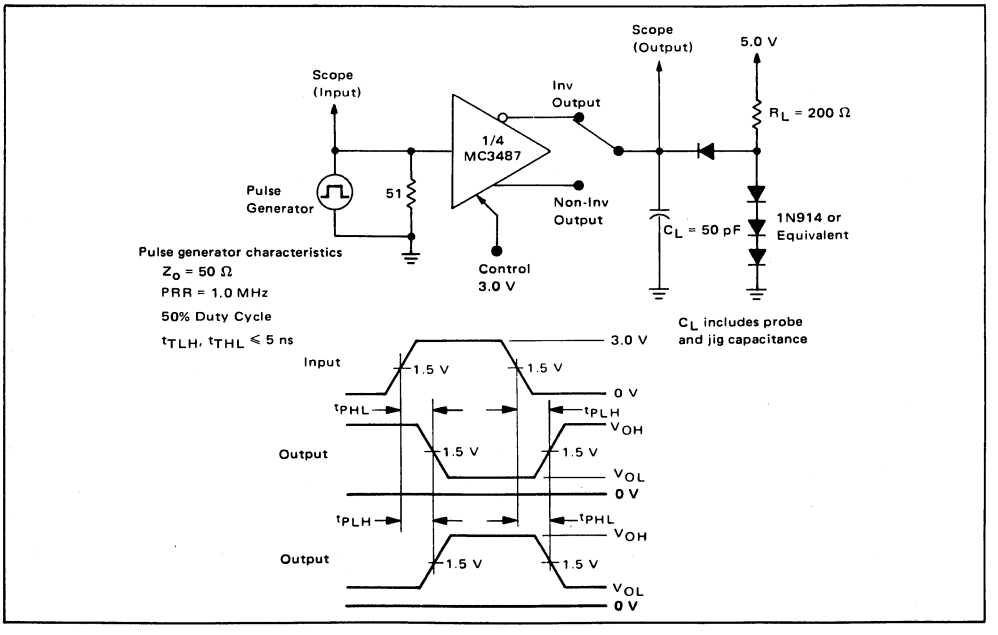


FIGURE 3 – OUTPUT TRANSITION TIMES TEST CIRCUIT AND WAVEFORMS

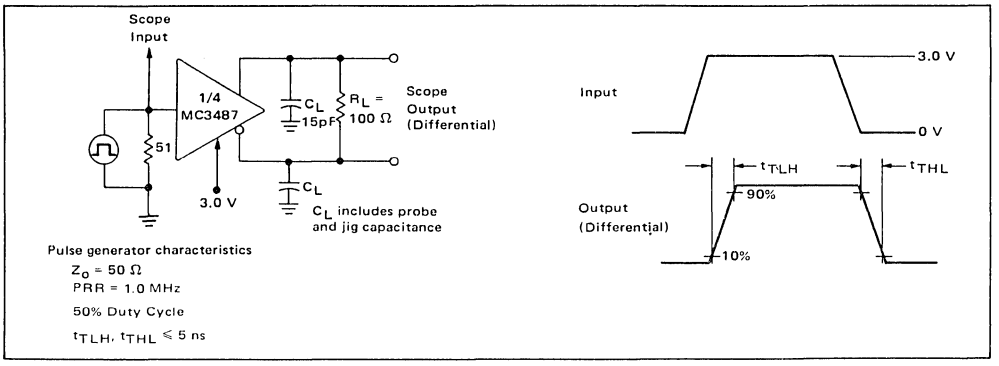


FIGURE 4 – OUTPUT CURRENT versus OUTPUT VOLTAGE

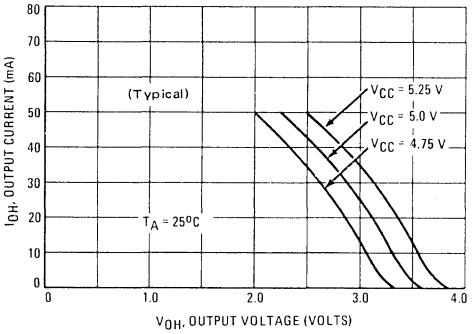
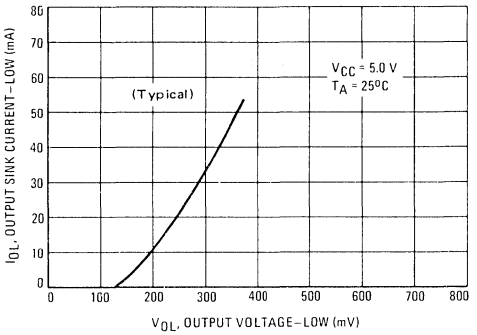


FIGURE 5 – OUTPUT SINK CURRENT versus OUTPUT VOLTAGE

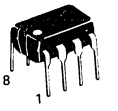


7

MC3488A

DUAL EIA-423/EIA-232D DRIVER

SILICON MONOLITHIC INTEGRATED CIRCUIT



P1 SUFFIX
PLASTIC PACKAGE
CASE 626

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO-8)

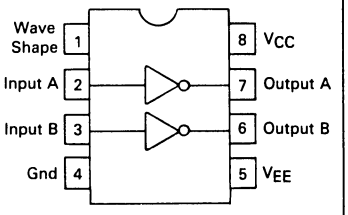
DUAL EIA-423/EIA-232D LINE DRIVER

The MC3488A dual single-ended line driver has been designed to satisfy the requirements of EIA standards EIA-423 and EIA-232D, as well as CCITT X.26, X.28 and Federal Standard FIDS1030. It is suitable for use where signal wave shaping is desired and the output load resistance is greater than 450 ohms. Output slew rates are adjustable from 1.0 μs to 100 μs by a single external resistor. Output level and slew rate are insensitive to power supply variations. Input undershoot diodes limit transients below ground and output current limiting is provided in both output states.

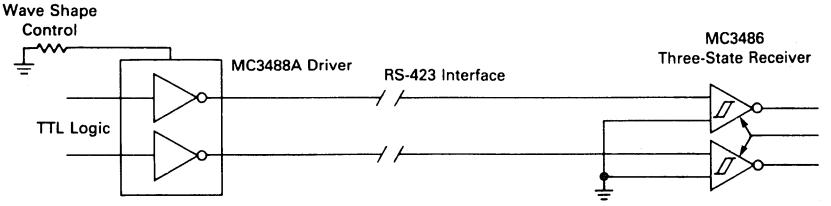
The MC3488A has a standard 1.5 V input logic threshold for TTL or NMOS compatibility.

- PNP Buffered Inputs to Minimize Input Loading
- Short Circuit Protection
- Adjustable Slew Rate Limiting
- MC3488A Equivalent to 9636A
- Output Levels and Slew Rates are Insensitive to Power Supply Voltages
- No External Blocking Diode Required for V_{EE} Supply
- Second Source μA9636A

PIN CONNECTIONS



TYPICAL APPLICATION



MAXIMUM RATINGS (Note 1)

Rating	Symbol	Value	Unit
Power Supply Voltages	V_{CC} V_{EE}	+15 −15	V
Output Current Source Sink	 I_{O+} I_{O-}	 +150 −150	mA
Operating Ambient Temperature	T_A	0 to +70	°C
Junction Temperature Range Ceramic Package Plastic Package	T_J	 175 150	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Voltages	V_{CC} V_{EE}	10.8 −13.2	12 −12	13.2 −10.8	V
Operating Temperature Range	T_A	0	25	70	°C
Wave Shaping Resistor	R_{WS}	10	—	1000	kΩ

TARGET ELECTRICAL CHARACTERISTICS (Unless otherwise noted specifications apply over recommended operating conditions)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Voltage — Low Logic State	V_{IL}	—	—	0.8	V
Input Voltage — High Logic State	V_{IH}	2.0	—	—	V
Input Current — Low Logic State (V_{IL} = 0.4 V)	I_{IL}	−80	—	—	μA
Input Current — High Logic State (V_{IH} = 2.4 V) (V_{IH} = 5.5 V)	 I_{IH1} I_{IH2}	 — —	 — —	 10 100	μA
Input Clamp Diode Voltage (I_{IK} = −15 mA)	V_{IK}	−1.5	—	—	V
Output Voltage — Low Logic State (R_L = ∞) EIA-423 (R_L = 3.0 kΩ) EIA-232D (R_L = 450 Ω) EIA-423	V_{OL}	 −6.0 −6.0 −6.0	 — — —	 −5.0 −5.0 −4.0	V
Output Voltage — High Logic State (R_L = ∞) EIA-423 (R_L = 3.0 kΩ) EIA-232D (R_L = 450 Ω) EIA-423	V_{OH}	 5.0 5.0 4.0	 — — —	 6.0 6.0 6.0	V
Output Resistance ($R_L \geq$ 450 Ω)	R_O	—	25	50	Ω
Output Short-Circuit Current (Note 2) (V_{in} = V_{out} = 0 V) (V_{in} = $V_{IH(Min)}$, V_{out} = 0 V)	 I_{OSH} I_{OSL}	 −150 +15	 — —	 −15 +150	mA
Output Leakage Current (Note 3) (V_{CC} = V_{EE} = 0 V, −6.0 V ≤ V_o ≤ 6.0 V)	I_{ox}	−100	—	100	μA
Power Supply Currents (R_W = 100 kΩ, R_L = ∞, $V_{IL} \leq V_{in} \leq V_{IH}$)	I_{CC} I_{EE}	— −18	— —	+18 —	mA

Note 1: Devices should not be operated at these values. The "Electrical Characteristics" provide conditions for actual device operation.
2: One output shorted at a time.
3: No V_{EE} diode required.

TRANSITION TIMES (Unless otherwise noted, C_L = 30 pF, f = 1.0 kHz, V_{CC} = $-V_{EE}$ = 12.0 V ± 10%, T_A = 25°C, R_L = 450 Ω. Transition times measured 10% to 90% and 90% to 10%)

Characteristic	Symbol	Min	Typ	Max	Unit
Transition Time, Low-to-High State Output	t_{TLH}				μs
(R_W = 10 kΩ)		0.8	—	1.4	
(R_W = 100 kΩ)		8.0	—	14	
(R_W = 500 kΩ)		40	—	70	
(R_W = 1000 kΩ)		80	—	140	
Transition Time, High-to-Low State Output	t_{THL}				μs
(R_W = 10 kΩ)		0.8	—	1.4	
(R_W = 100 kΩ)		8.0	—	14	
(R_W = 500 kΩ)		40	—	70	
(R_W = 1000 kΩ)		80	—	140	

FIGURE 1 — TEST CIRCUIT AND WAVEFORMS FOR TRANSITION TIMES

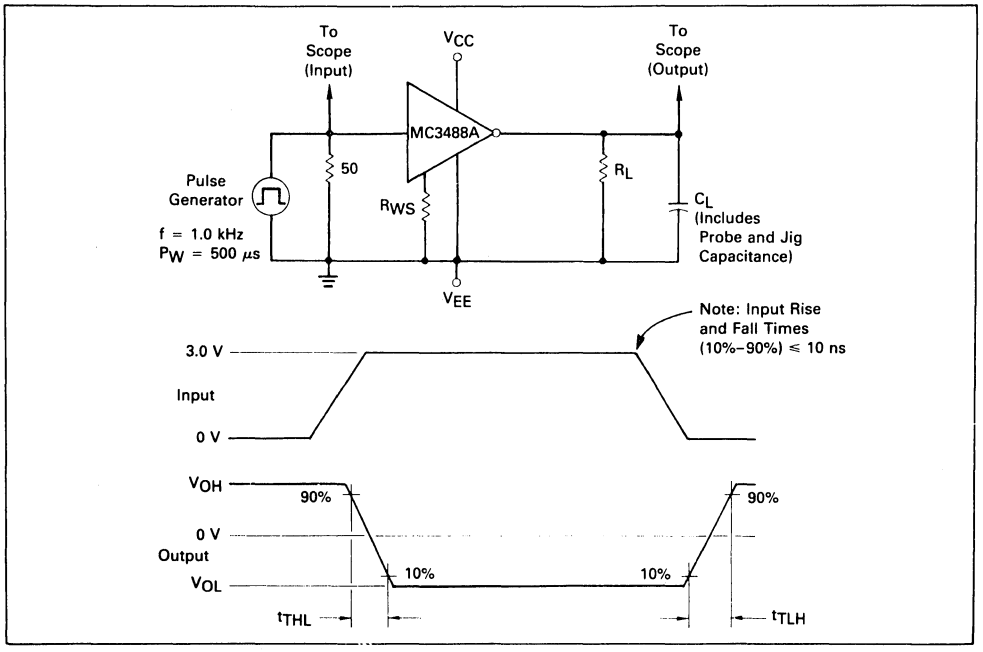


FIGURE 2 — OUTPUT TRANSISTION TIMES versus WAVE SHAPE RESISTOR VALUE

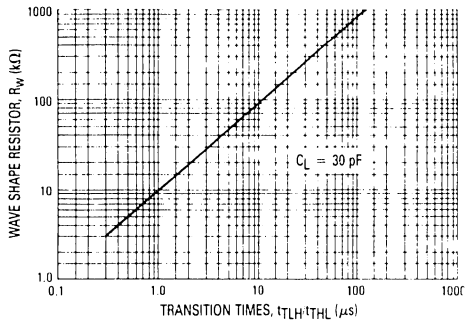


FIGURE 3 — INPUT/OUTPUT CHARACTERISTICS versus TEMPERATURE

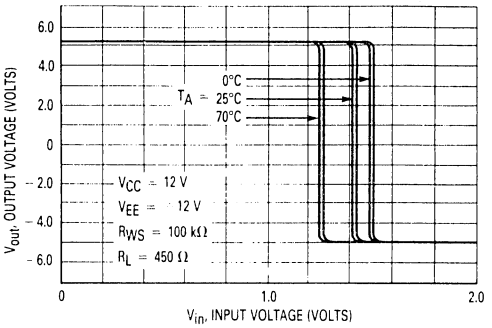
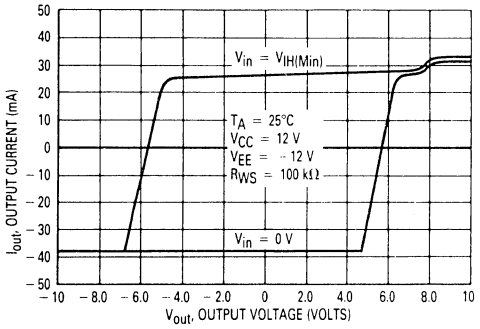


FIGURE 4 — OUTPUT CURRENT versus OUTPUT VOLTAGE

POWER-ON



POWER-OFF

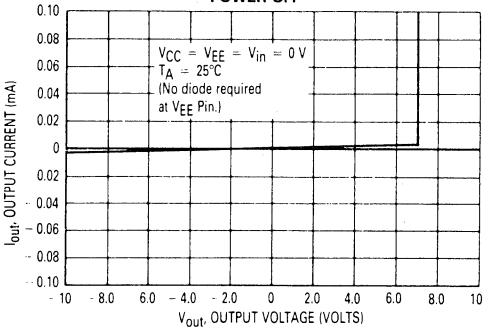


FIGURE 5 — SUPPLY CURRENT versus TEMPERATURE

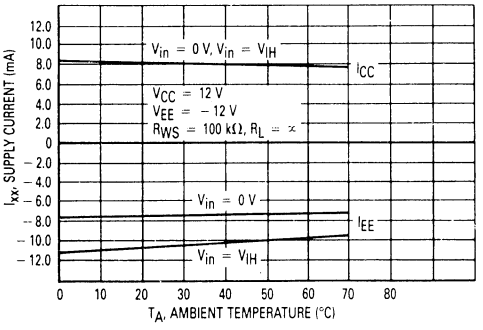
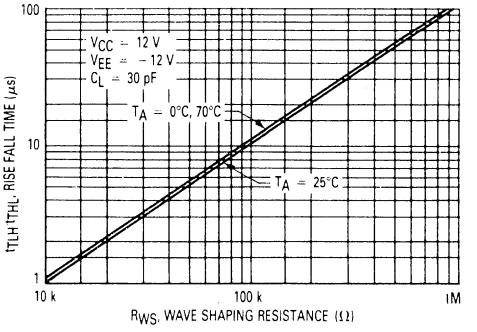


FIGURE 6 — RISE/FALL TIME versus R_{WS}



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC6875
MC6875A

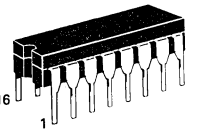
M6800 TWO-PHASE CLOCK GENERATOR/DRIVER

SCHOTTKY MONOLITHIC
INTEGRATED CIRCUIT

M6800 CLOCK GENERATOR

Intended to supply the non-overlapping $\phi 1$ and $\phi 2$ clock signals required by the microprocessor, this clock generator is compatible with 1.0, 1.5, and 2.0 MHz versions of the MC6800. Both the oscillator and high capacitance driver elements are included along with numerous other logic accessory functions for easy system expansion.

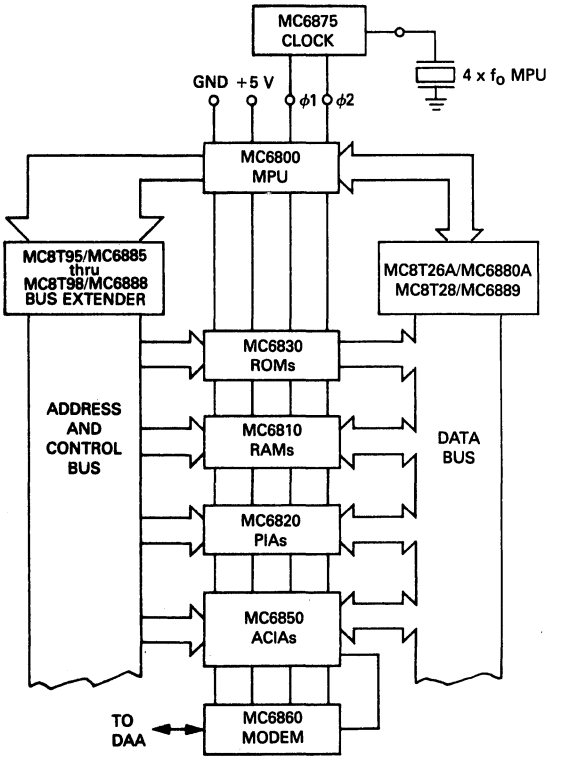
Schottky technology is employed for high speed and PNP-buffered inputs are employed for NMOS compatibility. A single +5 V power supply, and a crystal or RC network for frequency determination are required.



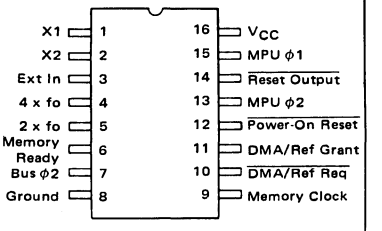
L SUFFIX
CERAMIC PACKAGE
CASE 620

7

Typical MPU System with Bus Extenders



PIN CONNECTIONS



ORDERING INFORMATION

Device	Temperature Range	Package
MC6875L	0 to +70°C	Ceramic DIP
MC6875AL	−55 to +125°C	

MAXIMUM RATINGS (Unless otherwise noted $T_A = 25^oC$.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+7.0	Vdc
Input Voltage	V_I	+5.5	Vdc
Operating Ambient Temperature Range MC6875L MC6875AL	T_A	 0 to +70 -55 to +125	^oC
Storage Temperature Range	T_{stg}	-65 to +150	^oC
Operating Junction Temperature	T_J	175	^oC

NOTE:
Operation of the MC6875AL over the full military temperature range (to maximum T_A) will result in excessive operating junction temperature.

The use of a clip on 16 pin heat sink similar to AAVID Engineering, Inc., Model 5007 ($R_{\theta CA}$ = 18°C/W) is recommended above $T_A \approx 95°C$.

Contact AAVID Engineering, Inc.
30 Cook Court
Laconia, New Hampshire 03246
Tel. (603) 524-4443

RECOMMENDED OPERATING CONDITIONS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+4.75 to +5.25	Vdc

ELECTRICAL CHARACTERISTICS
(Unless otherwise noted specifications apply over recommended power supply and temperature ranges. Typical values measured at V_{CC} = 5.0 V and $T_A = 25^oC$.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage — High Logic State					
MPU $\phi1$ and $\phi2$ Outputs					V
(V_{CC} = 4.75 V, I_{OHM} = -200 μA)	V_{OHM}	V_{CC} - 0.6	–	–	
(V_{CC} = 5.25 V, I_{OHMK} = +5.0 mA)	V_{OHMK}	–	–	V_{CC} + 1.0	
Bus $\phi2$ Output					V
(V_{CC} = 4.75 V, I_{OHB} = -10 mA)	V_{OHB}	2.4	–	–	
(V_{CC} = 5.25 V, I_{OHBK} = +5.0 mA)	V_{OHBK}	–	–	V_{CC} + 1.0	
4 x fo Output					V
(V_{CC} = 4.75 V, V_{IH} = 2.0 V, I_{OH4X} = -500 μA)	V_{OH4X}	2.4	–	–	
2 x fo, DMA/Refresh Grant and Memory Clock Outputs (V_{CC} = 4.75 V, I_{OH} = -500 μA)	V_{OH}	2.4	–	–	V
$\overline{\text{Reset}}$ Output (V_{CC} = 4.75 V, V_{IH} = 3.3 V, $I_{OH\overline{R}}$ = -100 μA)	$V_{OH\overline{R}}$	2.4	–	–	V
Output Voltage — Low Logic State					
MPU $\phi1$ and $\phi2$ Outputs					V
(V_{CC} = 4.75 V, I_{OLM} = +200 μA)	V_{OLM}	–	–	0.4	
(V_{CC} = 4.75 V, I_{OLMK} = -5.0 mA)	V_{OLMK}	–	–	-1.0	
Bus $\phi2$ Output					V
(V_{CC} = 4.75 V, I_{OLB} = +48 mA)	V_{OLB}	–	–	0.5	
(V_{CC} = 4.75 V, I_{OLBK} = -5.0 mA)	V_{OLBK}	–	–	-1.0	
4 x fo Output					V
(V_{CC} = 4.75 V, V_{IL} = 0.8 V, I_{OL4X} = 16 mA)	V_{OL4X}	–	–	0.5	
2 x fo, DMA/Refresh Grant and Memory Clock Outputs (V_{CC} = 4.75 V, I_{OL} = 16 mA)	V_{OL}	–	–	0.5	V
$\overline{\text{Reset}}$ Output (V_{CC} = 4.75 V, V_{IL} = 0.8 V, $I_{OL\overline{R}}$ = 3.2 mA)	$V_{OL\overline{R}}$	–	–	0.5	V
Input Voltage — High Logic State					V
Ext. In, Memory Ready and $\overline{\text{DMA/Refresh Request}}$ Inputs	V_{IH}	2.0	–	–	
Input Voltage — Low Logic State					V
Ext. In, Memory Ready and $\overline{\text{DMA/Refresh Request}}$ Inputs	V_{IL}	–	–	0.8	
Input Thresholds — $\overline{\text{Power-On Reset}}$ Input (See Figure 2)					V
Output Low to High	V_{ILH}	–	2.8	3.6	
Output High to Low	V_{IHL}	0.8	1.4	–	
Input Clamp Voltage MC6875L	V_{IK}	–	–	-1.0	V
(V_{CC} = 4.75 V, I_{IC} = -5.0 mA) MC6875AL		–	–	-1.5	
Input Current — High Logic State					
Ext. In, Memory Ready and $\overline{\text{DMA/Refresh Request}}$ Inputs (V_{CC} = 4.75 V, V_{IH} = 5.0 V)	I_{IH}	–	–	25	μA
$\overline{\text{Power-On Reset}}$ (V_{CC} = 5.0 V, $V_{IH\overline{R}}$ = 5.0 V)	$I_{IH\overline{R}}$	–	–	50	μA
Input Current — Low Logic State					
Ext. In, Memory Ready and $\overline{\text{DMA/Refresh Request}}$ Inputs (V_{CC} = 5.25 V, V_{IL} = 0.5 V)	I_{IL}	–	–	-250	μA
$\overline{\text{Power-On Reset}}$ Input[1] (V_{CC} = 5.25 V, V_{IL} = 0.5 V)	$I_{IL\overline{R}}$	–	–	-250	μA

OPERATING DYNAMIC POWER SUPPLY CURRENT

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Currents (V_{CC} = 5.25 V, f_{osc} = 8.0 MHz, V_{IL} = 0 V, V_{IH} = 3.0 V)					
Normal Operation (Memory Ready and $\overline{\text{DMA/Refresh Request}}$ Inputs at High Logic State)	I_{CCN}	–	–	150	mA
Memory Ready Stretch Operation (Memory Ready Input at Low Logic State; $\overline{\text{DMA/Refresh Request}}$ Input at High Logic State)	I_{CCMR}	–	–	135	mA
$\overline{\text{DMA/Refresh Request}}$ Stretch Operation (Memory Ready Input at High Logic State; $\overline{\text{DMA/Refresh Request}}$ Input at Low Logic State)	I_{CCDR}	–	–	135	mA

SWITCHING CHARACTERISTICS

(These specifications apply whether the Internal Oscillator (see Figure 9) or an External Oscillator is used (see Figure 10). Typical values measured at V_{CC} = 5.0 V, T_A = 25°C, fo = 1.0 MHz (see Figure 8).

Characteristic	Symbol	Min	Typ	Max	Unit
MPU ϕ1 AND ϕ2 CHARACTERISTICS					
Output Period (Figure 3)	t_o	500	–	–	ns
Pulse Width (Figure 3)	t_{PWM}				ns
(fo = 1.0 MHz)		400	–	–	
(fo = 1.5 MHz)		230	–	–	
(fo = 2.0 MHz)		180	–	–	
Total Up Time (Figure 3)	t_{UPM}				ns
(fo = 1.0 MHz)		900	–	–	
(fo = 1.5 MHz)		600	–	–	
(fo = 2.0 MHz)		440	–	–	
Delay Time Referenced to Output Complement (Figure 3)					
Output High to Low State (Clock Overlap at 1.0 V)	t_{PLHM}	0	–	–	ns
Delay Times Referenced to 2 x fo (Figure 4 MPU ϕ2 only)					
Output Low to High Logic State	t_{PLHM2X}	–	–	85	ns
Output High to Low Logic State	t_{PHLM2X}	–	–	70	ns
Transition Times (Figure 3)					
Output Low to High Logic State	t_{TLHM}	–	–	25	ns
Output High to Low Logic State	t_{THLM}	–	–	25	ns
BUS ϕ2 CHARACTERISTICS					
Pulse Width – Low Logic State (Figure 4)	t_{PWLB}				ns
(fo = 1.0 MHz)		430	–	–	
(fo = 1.5 MHz)		280	–	–	
(fo = 2.0 MHz)		210	–	–	
Pulse Width – High Logic State	t_{PWHB}				ns
(fo = 1.0 MHz)		450	–	–	
(fo = 1.5 MHz)		295	–	–	
(fo = 2.0 MHz)		235	–	–	
Delay Times – (Referenced to MPU ϕ1) (Figure 4)					
Output Low to High Logic State	t_{PLHBM1}				ns
(fo = 1.0 MHz)		480	–	–	
(fo = 1.5 MHz)		320	–	–	
(fo = 2.0 MHz)		240	–	–	
Output High to Low Logic State	t_{PHLBM1}				
(C_L = 300 pF)		–	–	25	
(C_L = 100 pF)		–	–	20	
Delay Times (Referenced to MPU ϕ2) (Figure 4)					
Output Low to High Logic State	t_{PLHBM2}	-30	–	+25	ns
Output High to Low Logic State	t_{PHLBM2}	0	–	+40	ns
Transition Times (Figure 4)					
Output Low to High Logic State	t_{TLHB}	–	–	20	ns
Output High to Low Logic State	t_{THLB}	–	–	20	ns

SWITCHING CHARACTERISTICS (continued)

Characteristic	Symbol	Min	Typ	Max	Unit
MEMORY CLOCK CHARACTERISTICS					
Delay Times (Referenced to MPU ϕ2) (Figure 4)					
Output Low to High Logic State	t_{PLHCM}	-50	–	+25	ns
Output High to Low Logic State	t_{PHLCM}	0	–	+40	ns
Delay Times (Referenced to 2 x fo) (Figure 4)					
Output Low to High Logic State	t_{PLHC2X}	–	–	65	ns
Output High to Low Logic State	t_{PHLC2X}	–	–	85	ns
Transition Times (Figure 4)					
Output Low to High State	t_{TLHC}	–	–	25	ns
Output High to Low State	t_{THLC}	–	–	25	ns
2 x fo CHARACTERISTICS					
Delay Times (Referenced to 4 x fo) (Figure 4)					
Output Low to High Logic State	t_{PLH2X}	–	–	50	ns
Output High to Low Logic State	t_{PHL2X}	–	–	65	ns
Delay Time (Referenced to MPU ϕ1) (Figure 4)					
Output High to Low Logic State	$t_{PHL2XM1}$				ns
(fo = 1.0 MHz)		365	–	–	
(fo = 1.5 MHz)		220	–	–	
Transition Times (Figure 4)					
Output Low to High Logic State	t_{TLH2X}	–	–	25	ns
Output High to Low Logic State	t_{THL2X}	–	–	25	ns
4 x fo CHARACTERISTICS					
Delay Times (Referenced to Ext. In) (Figure 4)					
Output Low to High Logic State	t_{PLH4X}	–	–	50	ns
Output High to Low Logic State	t_{PHL4X}	–	–	30	ns
Transition Time (Figure 4)					
Output Low to High Logic State	t_{TLH4X}	–	–	25	ns
Output High to Low Logic State	t_{THL4X}	–	–	25	ns
MEMORY READY CHARACTERISTICS					
Set-Up Times (Figure 5)					
Low Input Logic State	t_{SMRL}	55	–	–	ns
High Input Logic State	t_{SMRH}	75	–	–	ns
Hold Time (Figure 5)					
Low Input Logic State	t_{HMRL}	10	–	–	ns
$\overline{\text{DMA/REFRESH REQUEST}}$ CHARACTERISTICS					
Set-Up Times (Figure 6)					
Low Input Logic State	t_{SDRL}	65	–	–	ns
High Input Logic State	t_{SDRH}	75	–	–	ns
Hold Time (Figure 6)					
Low Input Logic State	t_{HDRL}	10	–	–	ns
DMA/REFRESH GRANT CHARACTERISTICS					
Delay Time Referenced to Memory Clock (Figure 6)					
Output Low to High Logic State	t_{PLHG}	-15	–	+25	ns
Output High to Low Logic State	t_{PHLG}	-25	–	+15	ns
Transition Times (Figure 6)					
Output Low to High Logic State	t_{TLHG}	–	–	25	ns
Output High to Low Logic State	t_{THLG}	–	–	25	ns
$\overline{\text{RESET}}$ CHARACTERISTICS					
Delay Time Referenced to $\overline{\text{Power-On Reset}}$ (Figure 7)					
Output Low to High Logic State	$t_{PLH\overline{R}}$	–	–	1000	ns
Output High to Low Logic State	$t_{PHL\overline{R}}$	–	–	250	ns
Transition Times (Figure 7)					
Output Low to High Logic State	$t_{TLH\overline{R}}$	–	–	100	ns
Output High to Low Logic State	$t_{THL\overline{R}}$	–	–	50	ns

DESCRIPTION OF PIN FUNCTIONS

- $4 \times f_o$ — A free running oscillator at four times the MPU clock rate useful for a system sync signal.
- $2 \times f_o$ — A free running oscillator at two times the MPU clock rate.
- $\overline{\text{DMA/REF REQ}}$ — An asynchronous input used to freeze the MPU clocks in the ϕ1 high, ϕ2 low state for dynamic memory refresh or cycle steal DMA (Direct Memory Access).
- REF GRANT — A synchronous output used to synchronize the refresh or DMA operation to the MPU.
- MEMORY READY — An asynchronous input used to freeze the MPU clocks in the ϕ1 low, ϕ2 high state for slow memory interface.
- MPU ϕ1, MPU ϕ2 — Capable of driving the ϕ1 and ϕ2 inputs on two MC6800s.
- BUS ϕ2 — An output nominally in phase with MPU ϕ2 having MC8T26A type drive capability.
- MEMORY CLOCK — An output nominally in phase with MPU ϕ2 which free runs during a refresh request cycle.
- $\overline{\text{POWER-ON RESET}}$ — A Schmitt trigger input which controls $\overline{\text{Reset}}$. A capacitor to ground is required to set the desired time constant. Internal 50 k resistor to V_{CC}. See General Design Suggestions for Manual Reset Operation.
- $\overline{\text{RESET}}$ — An output to the MPU and I/O devices.
- X1, X2 — Provision to attach a series resonant crystal or RC network.
- EXT IN — Allows driving by an external TTL signal to synchronous the MPU to an external system.

FIGURE 1 – BLOCK DIAGRAM

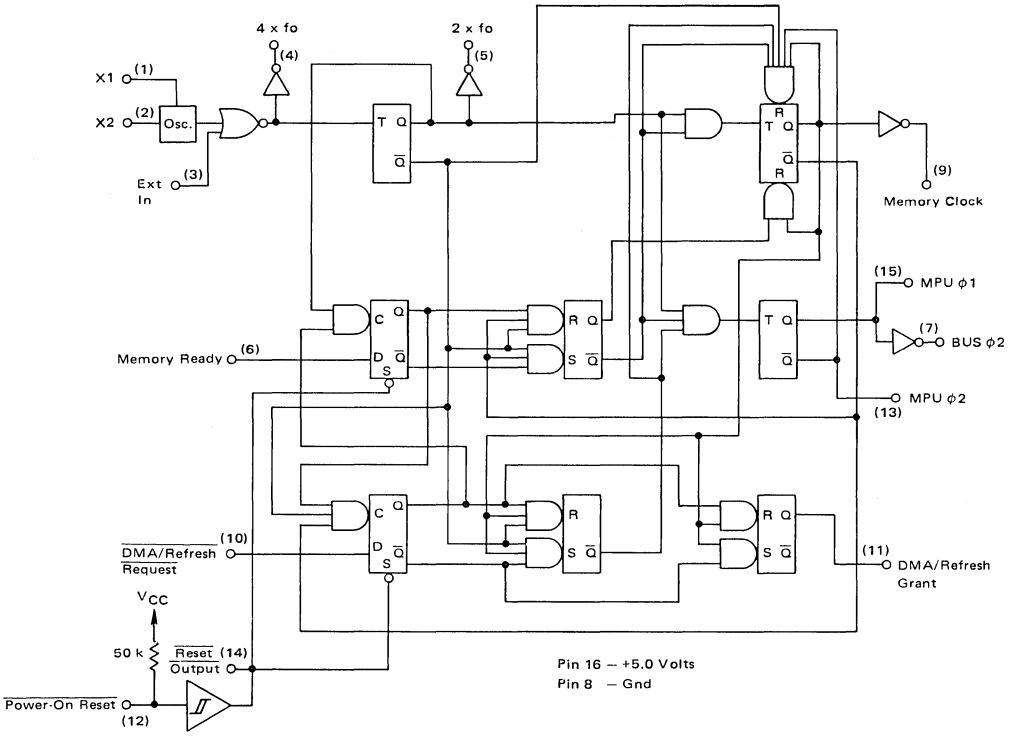


FIGURE 2 – TYPICAL HYSTERESIS CHARACTERISTIC OF $\overline{\text{RESET}}$ FUNCTION

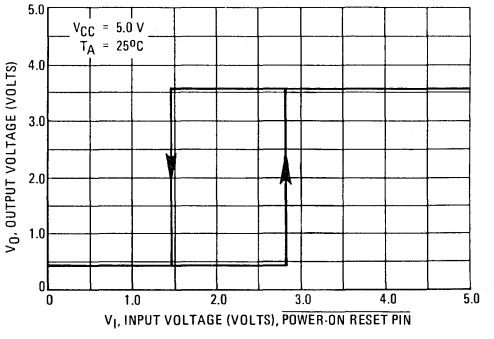
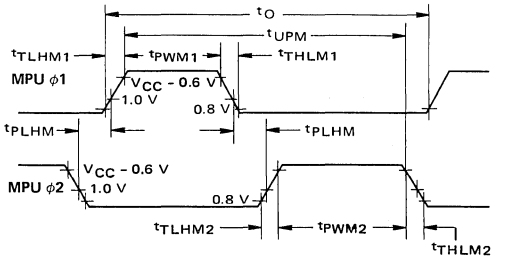


FIGURE 3 – TIMING DIAGRAM FOR MPU ϕ1 AND ϕ2



V_{OV} = 1.0 V = Clock Overlap measurement point

FIGURE 4 – TIMING DIAGRAM FOR NON-STRETCHED OPERATION
(Memory Ready and DMA/Refresh Request held high continuously)
Ext. In Input Voltage: 0 V to 3.0 V, f = 8.0 MHz, Duty Cycle = 50%, $t_{TLHEX} = t_{THLEX} = 5.0$ ns

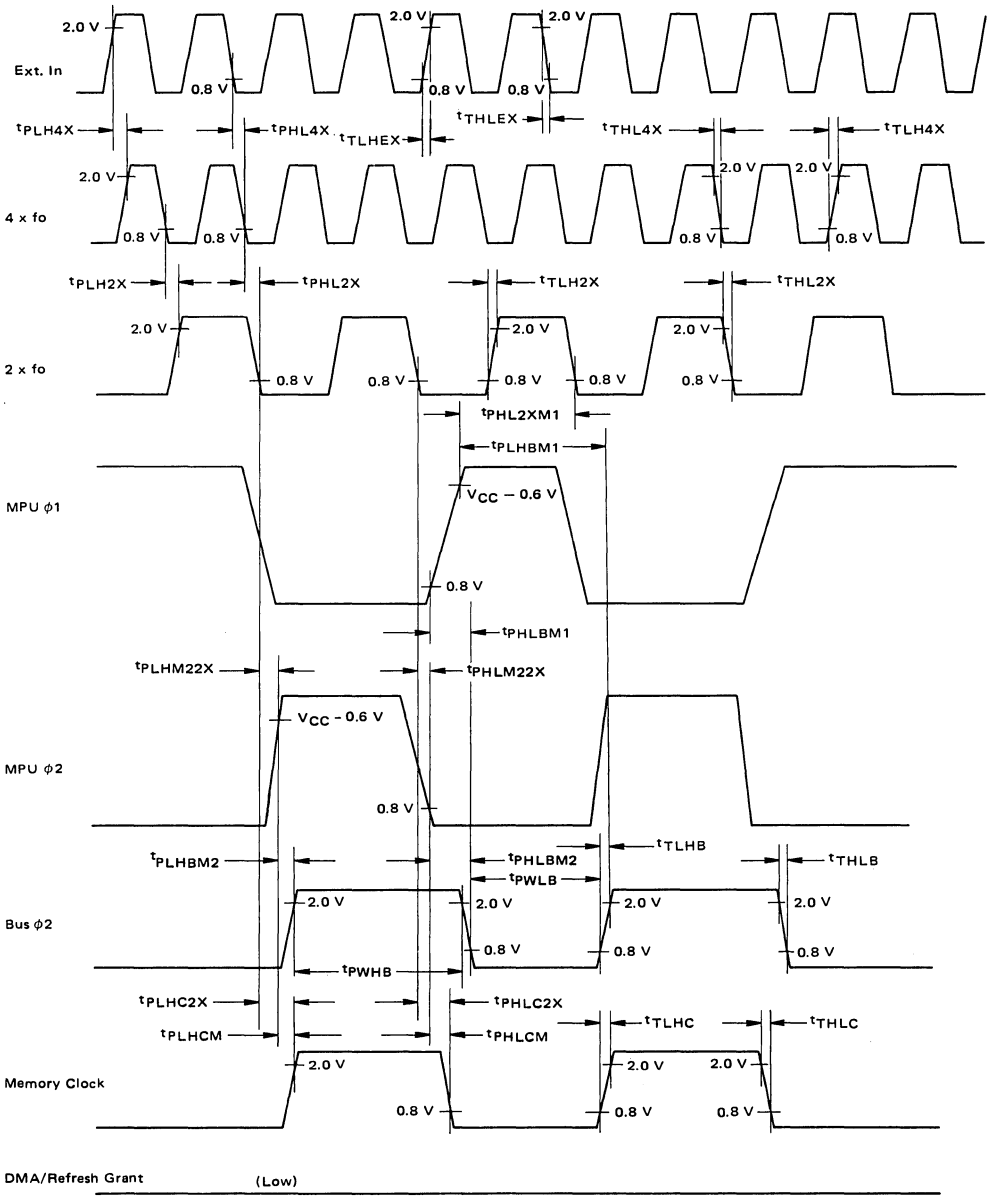


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FIGURE 5 – TIMING DIAGRAM FOR MEMORY READY STRETCH OPERATION
(Minimum Stretch Shown)
Input Voltage: 3.0 to 0 V, $t_{THLMR} = t_{TLHMR} = 5.0$ ns

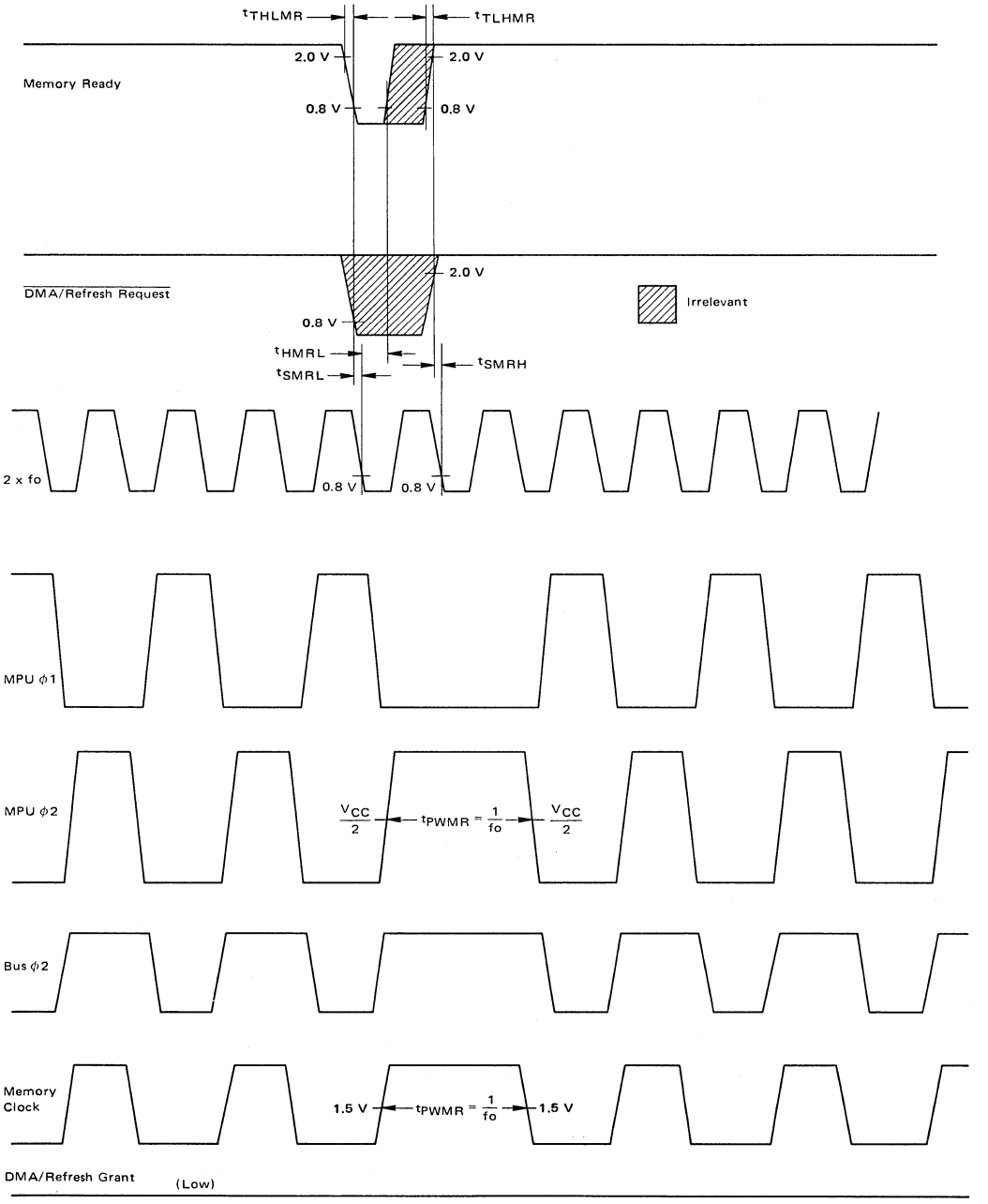

FIGURE 6 – TIMING DIAGRAM FOR $\overline{\text{DMA/REFRESH REQUEST}}$ STRETCH OPERATION
(Minimum Stretch Shown)
Input Voltage: 3.0 to 0 V, $t_{THLDR} = t_{TLHDR} = 5.0$ ns

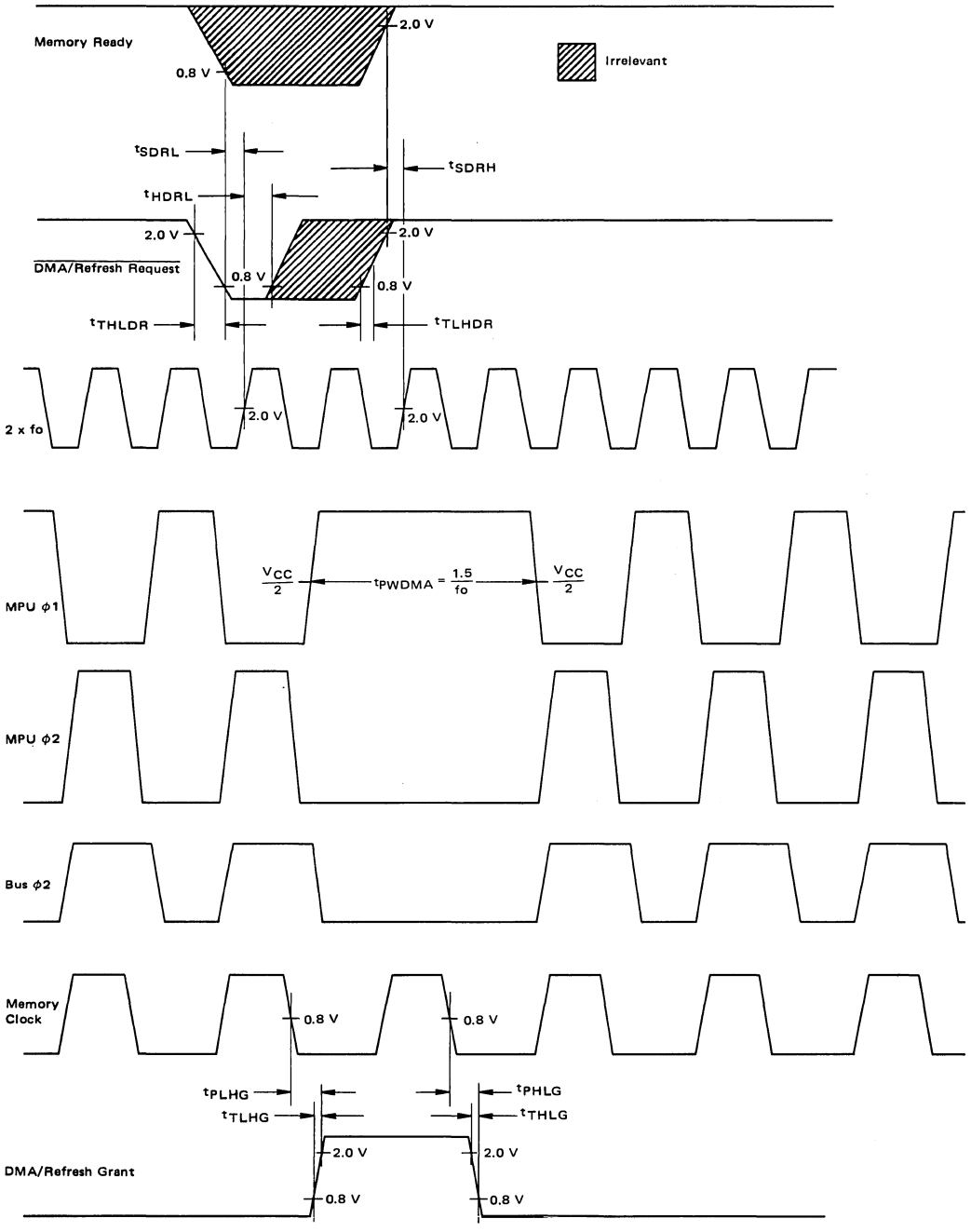

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FIGURE 7 – $\overline{\text{POWER ON RESET}}$

Input Voltage: 0 to 5.0 V, f = 100 kHz – Pulse Width = 1.0 μs, $t_{TLH} = t_{THL}$ = 25 ns

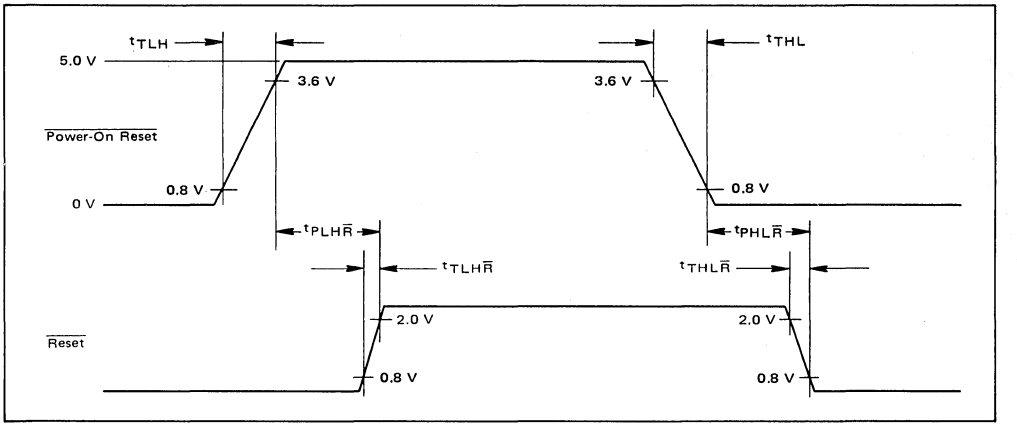
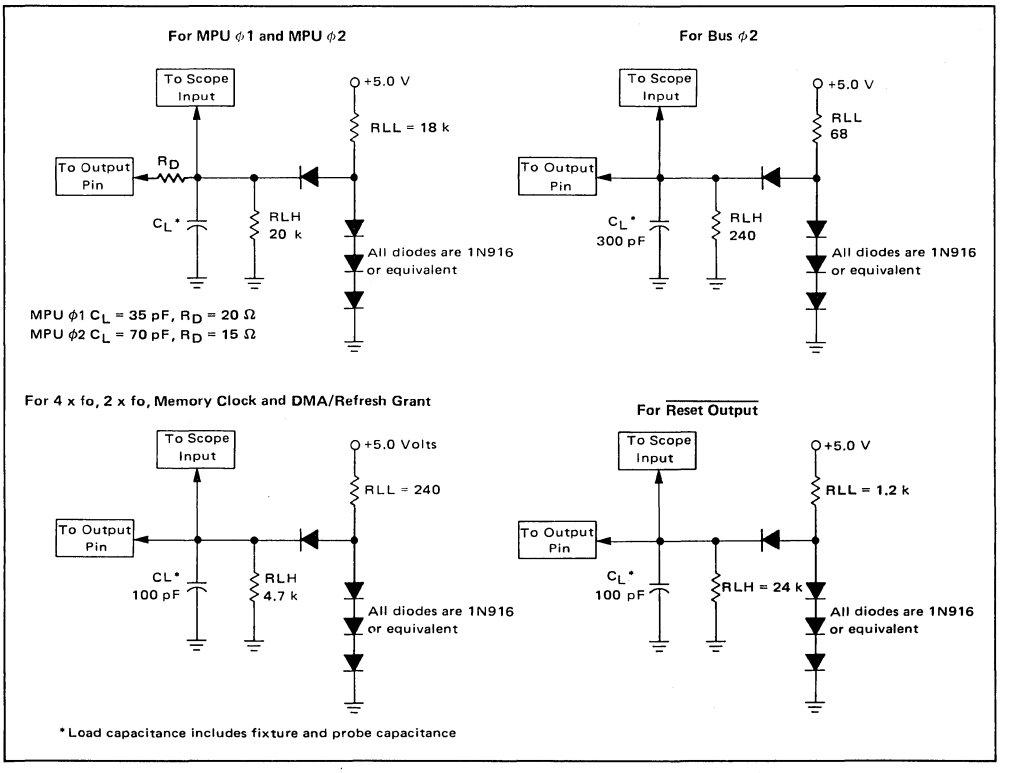


FIGURE 8 – LOAD CIRCUITS



APPLICATIONS INFORMATION

FIGURE 9 – TYPICAL RC FREQUENCY versus VOLTAGE

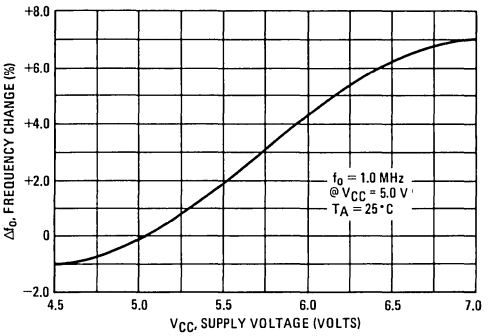


FIGURE 10 – TYPICAL RC FREQUENCY versus TEMPERATURE

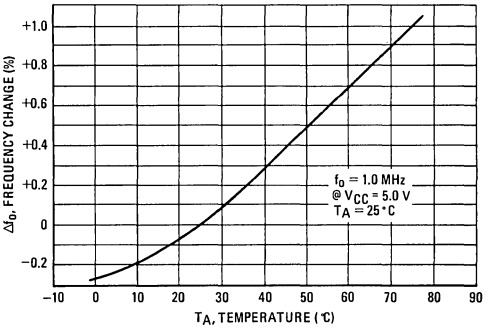
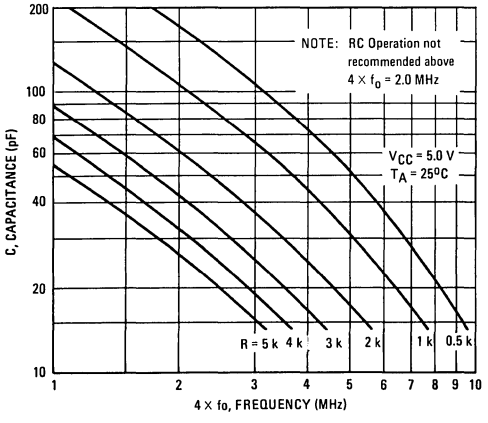


FIGURE 11 – TYPICAL FREQUENCY versus RESISTANCE FOR C VARIABLE



GENERAL

The MC6875 Clock Generator/Driver should be located on the same board and within two inches of the MC6800 MPU. Series damping resistors of 10-30 ohms may be utilized between the MC6875 and the MC6800 on the $\phi 1$ and $\phi 2$ clocks to suppress overshoot and reflections.

The V_{CC} pin (pin 16) of the MC6875 should be bypassed to the ground pin (pin 8) at the package with a 0.1 μF capacitor. Because of the high peak currents associated with driving highly capacitive loads, an adequately large ground strip to pin 8 should be used on the MC6875. Grounds should be carefully routed to minimize coupling of noise to the sensitive oscillator inputs. Unnecessary grounds or ground planes should be avoided near pin 2 or the frequency determining components. These components should be located as near as possible to the respective pins of the MC6875. Stray capacitance near pin 2 or the crystal, can affect the frequency. The can of the crystal should not be grounded. The ground side of the crystal or the C of the R-C oscillator should be connected as directly as possible to pin 8.

Unused inputs should be connected to V_{CC} or ground. Memory Ready, DMA/Refresh Request and Power-On Reset should be connected to V_{CC} when not used. The External Input should be connected to ground when not used.

OSCILLATOR

A tank circuit tuned to the desired crystal frequency connected between terminals X_1 and X_2 as shown in Figure 12, is recommended to prevent the oscillator from starting at other than the desired frequency. The 1kΩ resistor reduces the Q sufficiently to maintain stable crystal control. Crystal manufacturers may recommend a capacitance (C_L) to be used in series with the crystal for optimum performance at series resonance.

See Figures 9 and 10 for typical oscillator temperature and V_{CC} supply dependence for R-C operation.

FIGURE 12 – OSCILLATOR–CRYSTAL OPERATION

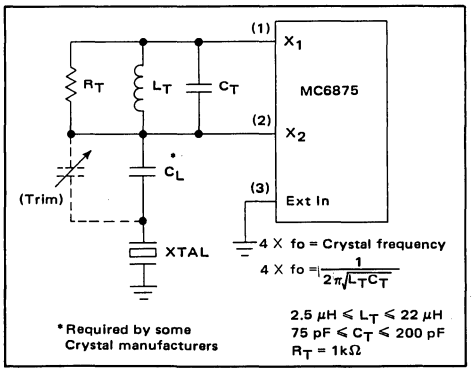


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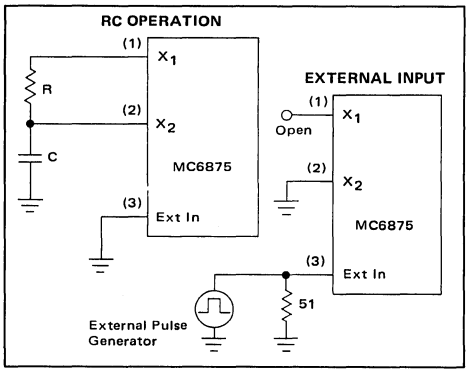
TABLE 1 – OSCILLATOR COMPONENTS

TANK CIRCUIT PARAMETERS		APPROXIMATE CRYSTAL PARAMETERS				CTS KNIGHTS 400 REIMANN AVE. SANDWICH, IL 60548 (815) 786-8411	McCOY ELECT. CO. WATTS & CHESTNUTS STS. MT. HOLLY SPRING, PA 17065 (717) 486-3411	TYCO CRYSTAL PRODUCTS 3940 W. MONTECITO PHOENIX, AZ 85019 (602) 272-7945
L_T μH	C_T pF	R_S Ohms	Co pF	C_1 mpF	fo MHz			
10	150	15-75	3-6	12	4.0	MP-04A * 390 pF	113-31	150-3260
4.7	82	8-45	4-7	23	8.0	MP-080 * 47 pF	113-32	150-3270

Inductors may be obtained from: Coilcraft, Cary, IL 60013 (312) 639-2361

FIGURE 13



To precisely time a crystal to desired frequency, a variable trimmer capacitor in the range of 7 to 40 pF would typically be used. Note it is not a recommended practice to tune the crystal with a parallel load capacitance.

The table above shows typical values for C_T and L_T, typical crystal characteristics, and manufacturers' part numbers for 4.0 and 8.0 megahertz operation.

The MC6875 will function as an R-C oscillator when connected as shown in Figure 13. The desired output frequency (Mϕ1) is approximately:

Formula

$$4 \times fo \approx \frac{320}{C\,(R + .27) + 23}$$

C in picofarads
R in K ohms
4 x fo in Megahertz

(See Figure 11)

It would be desirable to select a capacitor greater than 15 pF to minimize the effects of stray capacitance. It is also desirable to keep the resistor in the 1 to 5 k Ω range. There is a nominal 270 Ω resistor internally at X_1 which is in series with the external R. By keeping the external R as large as possible, the effects due to process variations of the internal resistor on the frequency will be reduced. There will, however, still be some variation in frequency in a production lot both from the resistance variations, external and internal, and process variations of the input switching thresholds. Therefore, in a production system, it is recommended a potentiometer be placed in series with a fixed R between X_1 and X_2.

POWER-ON RESET

As the power to the MC6875 comes up, the Reset Output will be in a high impedance state and will not give a solid V_{OL} output level until V_{CC} has reached 3.5 to 4.0 V. During this time transients may appear on the clock outputs as the oscillator begins to start. This happens at approximately V_{CC} = 3 V. At some V_{CC} level above that, where Reset Output goes low, all the clock outputs will begin functioning normally. This phenomenon of the start-up sequence should not cause any problems except possibly in systems with battery back-up memory. The transients on the clock lines during the time the Reset Output is high impedance could initiate the system in some unknown mode and possibly write into the backup memory system. Therefore in battery backup systems, more elaborate reset circuitry will be required.

Please note that the Power-On Reset input pin of the MC6875 is not suitable for use with a manual MPU reset switch if the DMA/Ref Req or Memory Ready inputs are going to be used. The power on reset circuitry is used to initialize the internal control logic and whenever the input is switched low, the MC6875 is irresponsive to the DMA/Ref Req or Memory Ready inputs. This may result in the loss of dynamic memory and/or possibly a byte of slow static memory. The circuit of Figure 14 is recommended for applications which do not utilize the DMA/Ref Req or Memory Ready inputs. The circuit of Figure 15 is recommended for those applications that do.

FIGURE 14 – MANUAL RESET FOR APPLICATIONS NOT USING DMA/REFRESH REQUEST OR MEMORY READY INPUTS

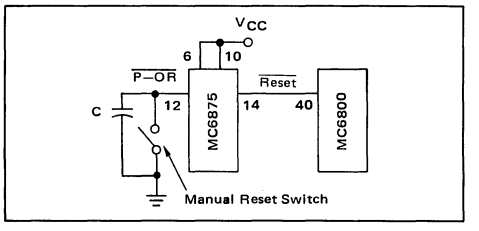
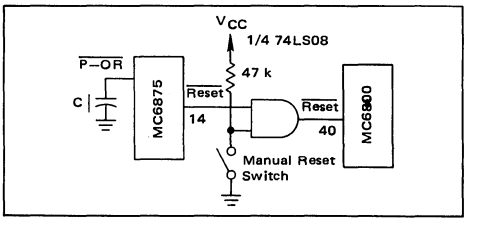


FIGURE 15 – MANUAL RESET FOR SYSTEMS USING DYNAMIC RAM OR SLOW STATIC RAM IN CONJUNCTION WITH MEMORY READY OR DMA/REFRESH REQUEST INPUTS



7

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC34050
MC34051

DUAL EIA-422/423 TRANSCEIVER

DUAL EIA-422/423 TRANSCEIVER

SILICON MONOLITHIC INTEGRATED CIRCUIT

The MC34050/51 are dual transceivers which comply with EIA Standards EIA-422 (Balanced line) and EIA-423 (Unbalanced line). Each device contains two drivers and two receivers.

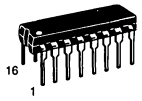
The MC34050 has a DRIVER ENABLE (for both drivers) and a $\overline{\text{RECEIVER ENABLE}}$ (for both receivers). Connecting the two ENABLES together provides Driver-to-Receiver switching from a single line.

The MC34051 has a DRIVER ENABLE for each driver. The two receivers are permanently enabled.

The Driver inputs, Receiver outputs, and Enable inputs are 74LS TTL compatible.

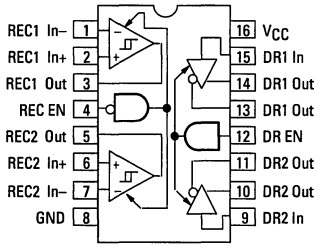
- Two Independent Drivers and Receivers Per Package
- 3-State Outputs
- Single 5.0 V Supply
- Internal Hysteresis (50 mV Typical) on Receivers
- Receivers Provide Fail-Safe Function. Output Stays High if Inputs are Open, Shorted (floating), or Terminated (floating)
- Receivers May Be Used in EIA-422 or 423 Systems
- Drivers Meet Full EIA-422 Standards

D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO-16)

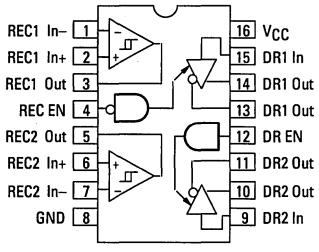


P SUFFIX
PLASTIC PACKAGE
CASE 648

PIN CONNECTIONS

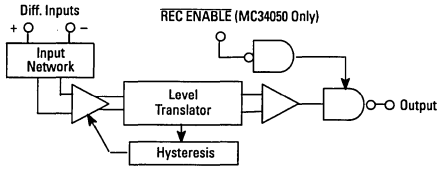


(MC34050)

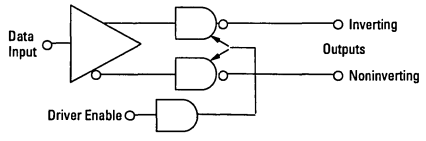


(MC34051)

RECEIVER BLOCK DIAGRAM



DRIVER BLOCK DIAGRAM



Driver				Receiver		
Data	EN	Inv. Out	Noninv. Out	Input	$\overline{\text{EN}}$	Output
L	H	H	L	> + 0.2 V Diff.	L	H
H	H	L	H	< – 0.2 V Diff.	L	L
X	L	Z	Z	X	H	Z

ORDERING INFORMATION

Device	Temperature Range	Package
MC34050D	0° to + 70°C	SO-16
MC34050P		Plastic DIP
MC34051P		Plastic DIP

7

MAXIMUM RATINGS

Parameter	Value	Units
Power Supply Voltage (V_{CC})	7.0	Vdc
Input Common Mode Voltage (Receivers)	±25	Vdc
Input Differential Voltage (Receivers)	±25	Vdc
Output Sink Current (Receivers)	50	mA
Enable Input Voltage (Drivers and Receivers)	5.5	Vdc
Input Voltage (Drivers)	5.5	Vdc
Applied Output Voltage (3-State mode) — Receivers	−1.0 to +7.0	Vdc
Applied Output Voltage (3-State mode) — Drivers	−1.0 to +7.0	Vdc
Junction Temperature	−65 to +150	°C
Storage Temperature	−65 to +150	°C

Devices should not be operated at these values.

The "Recommended Operating Limits" provide for actual device operation.

RECOMMENDED OPERATING LIMITS

Parameter	Min	Typ	Max	Units
Power Supply Voltage	+4.75	+5.0	+5.25	Vdc
Input Common Mode Voltage (Receivers)	−7.0	—	+7.0	Vdc
Input Differential Voltage (Receivers)	−6.0	—	+6.0	Vdc
Enable Input Voltage (Drivers and Receivers)	0	—	+5.25	Vdc
Input Voltage (Drivers)	0	—	+5.25	Vdc
Ambient Temperature Range	0	—	+70	°C

7

ELECTRICAL CHARACTERISTICS (Unless otherwise noted specifications apply for $4.75 < V_{CC} < 5.25$ volts, and $0° < T_A < 70°C$).

Parameter	Symbol	Min	Typ	Max	Units
DRIVERS					
Input Voltage — Low	V_{ILD}	—	—	0.8	Vdc
Input Voltage — High	V_{IHD}	2.0	—	—	Vdc
Input Current @ V_{IL} = 0.4 V	I_{ILD}	−360	—	—	μA
Input Current @ V_{IH} = 2.7 V V_{IH} = 5.25 V	I_{IHD}	— —	— —	+20 +100	μA
Input Clamp Voltage (I_{IK} = −18 mA)	V_{IKD}	−1.5	—	—	Vdc
Output Voltage — Low (I_{OL} = 20 mA)	V_{OLD}	—	—	0.5	Vdc
Output Voltage — High (I_{OH} = −20 mA)	V_{OHD}	2.5	—	—	Vdc
Output Offset Voltage Difference (Note 1)	V_{OSD}	−0.4	—	+0.4	Vdc
Output Differential Voltage (Note 1)	V_T	2.0	—	—	Vdc
Output Differential Voltage Difference (Note 1)	V_{TD}	−0.4	—	+0.4	Vdc
Short Circuit Current (V_{CC} = 5.25 V) (From High Output, Note 2)	I_{OSD}	−150	—	−30	mA
Output Leakage Current — Hi-Z State (V_{out} = 0.5 V, DR EN = 0.8 V) (V_{out} = 2.7 V, DR EN = 0.8 V)	I_{OZD}	 −100 −100	 — —	 +100 +100	μA
Output Leakage — Power Off (V_{out} = −0.25 V, V_{CC} = 0 V) (V_{out} = 6.0 V, V_{CC} = 0 V)	$I_{O(off)}$	 −100 —	 — —	 — +100	μA

Notes: 1) See EIA Standard EIA-422 and Figure 1 for exact test conditions.
2) Only one output in a package should be shorted at a time, for no longer than 1 second.

ELECTRICAL CHARACTERISTICS (Unless otherwise noted specifications apply for $4.75 < V_{CC} < 5.25$ volts, and $0° < T_A < 70°C$).

Parameter	Symbol	Min	Typ	Max	Units
RECEIVERS					
Differential Input Threshold Voltage (Note 3) (-7.0 V $< V_{ICM} < +7.0$, $V_{out} \geq 2.7$ V) (-7.0 V $< V_{ICM} < +7.0$, $V_{out} \leq 0.45$ V)	V_{THR}	 — −0.2	 — —	 +0.2 —	Vdc
Input Bias Current ($0 \leq V_{CC} \leq 5.25$ V, $V_{in} = +15$ V) ($0 \leq V_{CC} \leq 5.25$ V, $V_{in} = -15$ V)	I_{IBR}	 — −2.8	 — —	 +2.3 —	mA
Input Balance and Output Level ($-7.0 \leq V_{ICM} \leq +7.0$ V) ($V_{ID} = +0.4$ V, $I_O = -400$ μA) ($V_{ID} = -0.4$ V, $I_O = 8.0$ mA)	 V_{OHR} V_{OLR}	 2.7 —	 — —	 — 0.45	Vdc
Output Leakage Current — 3-State (Pin 4 = 2.0 V, MC34050 only) ($V_{ID} = +3.0$ V, $V_O = 0.4$ V) ($V_{ID} = -3.0$ V, $V_O = 2.4$ V)	I_{OZR}	 −100 −100	 — —	 +100 +100	μA
Output Short Circuit Current (Note 2, $V_{CC} = 5.25$ V) ($V_{ID} = +3.0$ V, MC34050 Pin 4 = 0.4 V, $V_O = 0$ V)	I_{OSR}	−85	—	−15	mA
ENABLES					
Input Voltage — Low	V_{ILE}	—	—	0.8	Vdc
Input Voltage — High	V_{IHE}	2.0	—	—	Vdc
Input Current @ $V_{IL} = 0.4$ V (Receiver EN) (Driver EN)	I_{ILER} I_{ILED}	−100 −360	— —	— —	μA
Input Current @ $V_{IH} = 2.7$ V $V_{IH} = 5.25$ V	I_{IHE}	 —	 —	+20 +100	μA
Input Clamp Voltage ($I_{IK} = -18$ mA)	V_{IKE}	−1.5	—	—	Vdc
POWER SUPPLY					
Power Supply Current @ $V_{CC} = 5.25$ V	I_{CC}	—	55	80	mA

Notes: 1) See EIA Standard EIA-422 and Figure 1 for exact test conditions.
2) Only one output in a package should be shorted at a time, for no longer than 1 second.
3) Differential input threshold voltage and guaranteed output levels are done simultaneously for worst case.
4) All currents into a device pin are positive, those out of a pin are negative. Voltages are referenced to ground. Algebraic convention rather than magnitude is used to define limits.

DRIVER SWITCHING CHARACTERISTICS ($V_{CC} = 5.0$ V, $T_A = 25°C$, See Figure 2)

Parameter	Symbol	Min	Typ	Max	Units
Propagation Delay					ns
Data Input to Output High-to-Low	t_{PHLD}	—	—	20	
Data Input to Output Low-to-High	t_{PLHD}	—	—	20	
Output Skew ($\lvert t_{PHL} - t_{PLH} \rvert$ each driver)	t_{SKD}	—	—	8	
Enable Input to Output					
$C_L = 10$ pF, $R_L = 75\ \Omega$ to Gnd	t_{PHZD}	—	—	30	
$C_L = 10$ pF, $R_L = 180\ \Omega$ to V_{CC}	t_{PLZD}	—	—	35	
$C_L = 30$ pF, $R_L = 75\ \Omega$ to Gnd	t_{PZHD}	—	—	40	
$C_L = 30$ pF, $R_L = 180\ \Omega$ to V_{CC}	t_{PZLD}	—	—	45	
Maximum Data Input Transition Time (10–90%)	t_{TRD}	—	50	—	ns

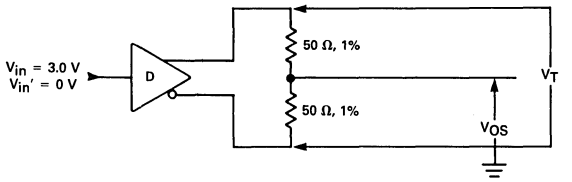
RECEIVER SWITCHING CHARACTERISTICS ($V_{CC} = 5.0$ V, $T_A = 25°C$, Figure 3)

Parameter	Symbol	Min	Typ	Max	Units
Propagation Delay					ns
Differential Input to Output — High-to-Low	t_{PHLR}	—	—	30	
Differential Input to Output — Low-to-High	t_{PLHR}	—	—	30	
Enable Input — Output Low to 3-State	t_{PLZR}	—	—	35	
Enable Input — Output High to 3-State	t_{PHZR}	—	—	35	
Enable Input — Output 3-State to High	t_{PZHR}	—	—	30	
Enable Input — Output 3-State to Low	t_{PZLR}	—	—	30	

MC34050 Only

*MC34050 Only.

FIGURE 1 — DRIVER OUTPUT TEST CIRCUIT

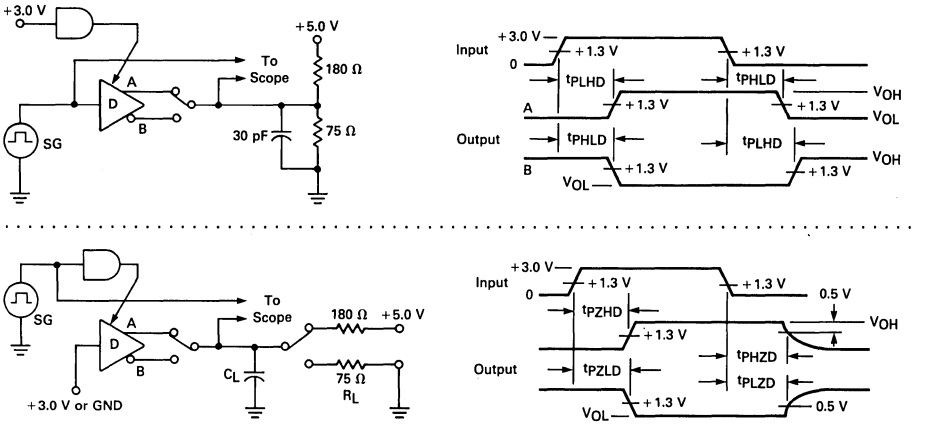


$$V_{OSD} = \left| V_{OS} - V_{OS'} \right|;$$

$$V_{ODD} = \left| |V_T| - |V_{T'}| \right|$$

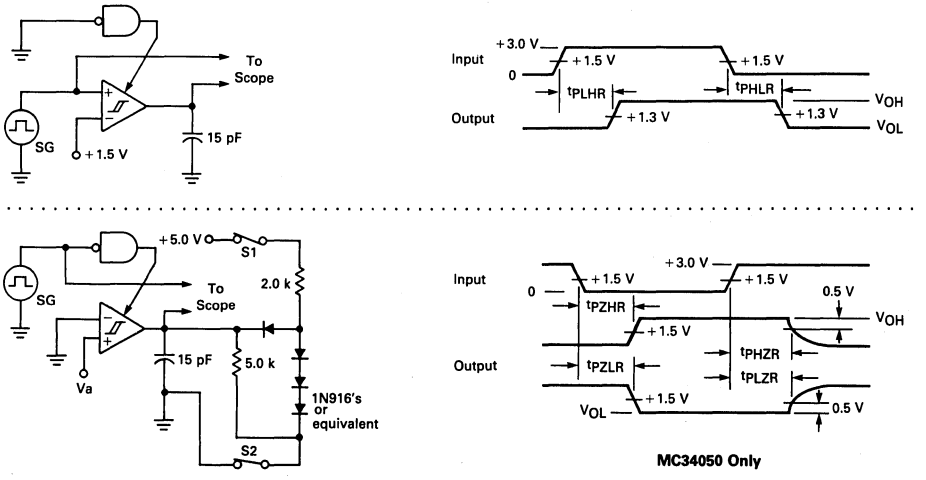
Circuit per EIA-422-A, Dec. 1978

FIGURE 2 — DRIVER SWITCHING TEST CIRCUITS



SG: 1.0 MHz, 50% duty cycle, t_R, t_F = 6.0 ns (10–90%)
R_L = 75 Ω to GND for t_{PZHD} and t_{PHZD}, 180 Ω to V_{CC} for t_{PZLD} and t_{PLZD};
C_L = 10 pF for t_{PHZD} and t_{PLZD}, 30 pF for t_{PZHD} and t_{PZLD}.

FIGURE 3 — RECEIVER SWITCHING TEST CIRCUITS



MC34050 Only

SG: 1.0 MHz, 50% duty cycle, t_R, t_F = 6.0 ns (10–90%)
Va = +1.5 V for t_{PHZ}, t_{PZH}; Va = −1.5 V for t_{PLZ}, t_{PZL}.
S1, S2 closed for t_{PHZ}, t_{PLZ}; S1 open, S2 closed for t_{PZH}; S1 closed, S2 open for t_{PZL}.

FIGURE 4 — DRIVER INPUT CHARACTERISTICS

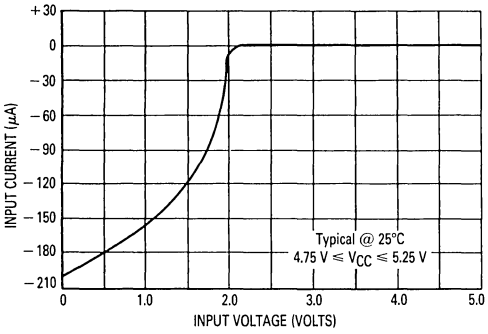


FIGURE 5 — DRIVER DIFFERENTIAL OUTPUT CHARACTERISTICS

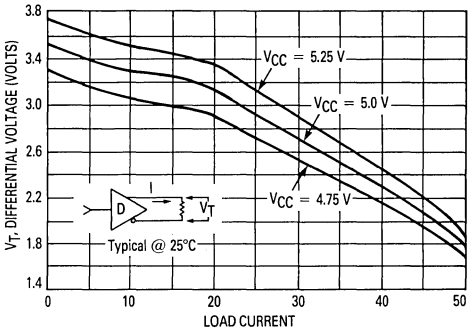


FIGURE 6 — DRIVER OUTPUT VOLTAGE

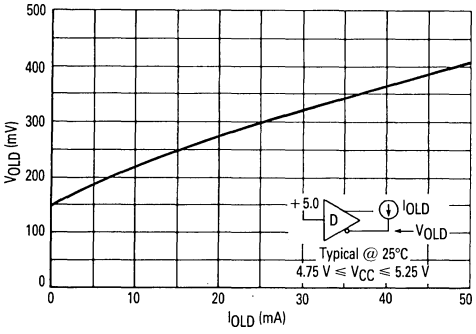


FIGURE 7 — DRIVER OUTPUT VOLTAGE

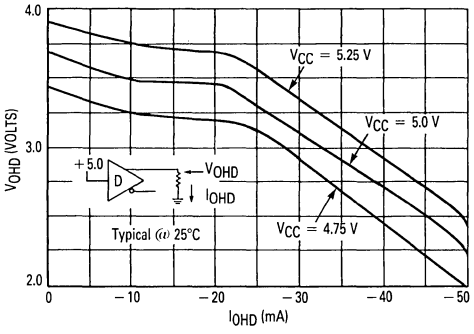


FIGURE 8 — RECEIVER OUTPUT VOLTAGE

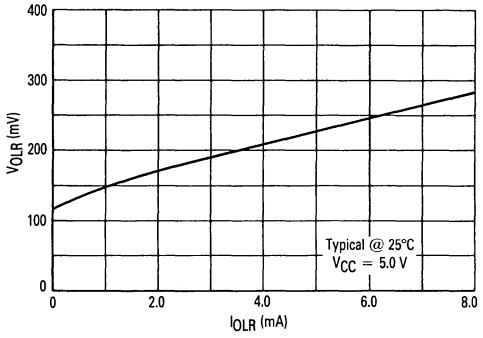


FIGURE 9 — RECEIVER OUTPUT VOLTAGE

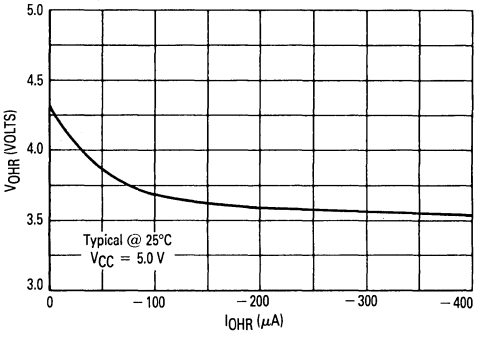


FIGURE 10 — RECEIVER INPUT CHARACTERISTICS

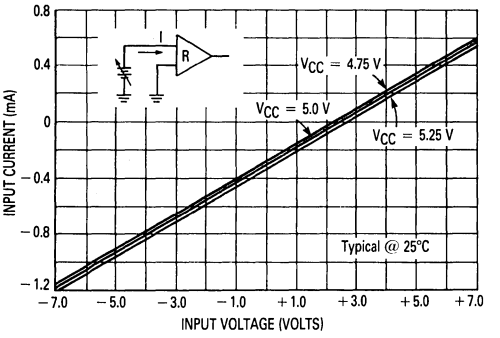


FIGURE 11 — ENABLE INPUT CHARACTERISTICS

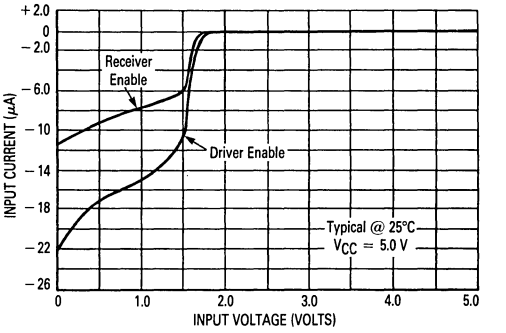


FIGURE 12 — RECEIVER INPUT CHARACTERISTICS

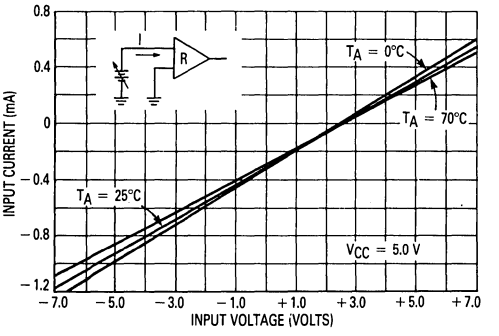


FIGURE 13 — RECEIVER OUTPUT LEAKAGE

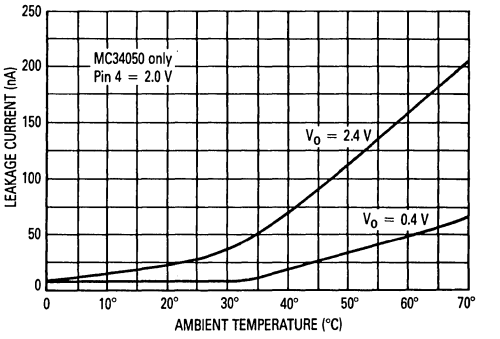


FIGURE 14 — DRIVER OUTPUT VOLTAGE

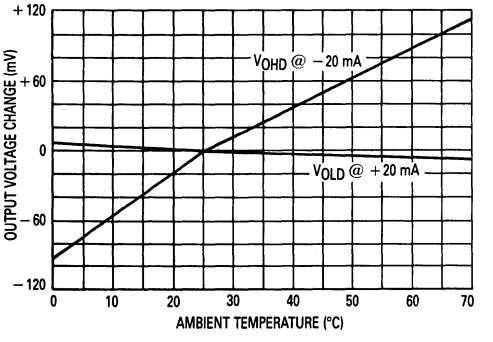


FIGURE 15 — DRIVER OUTPUT LEAKAGE

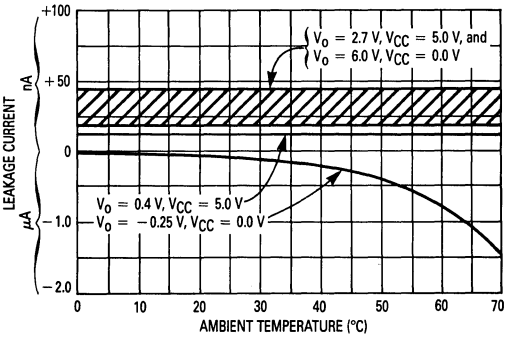


FIGURE 16 — EIA-422 APPLICATION

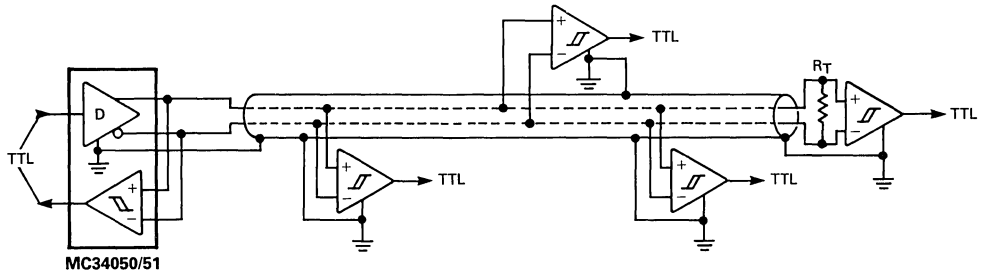
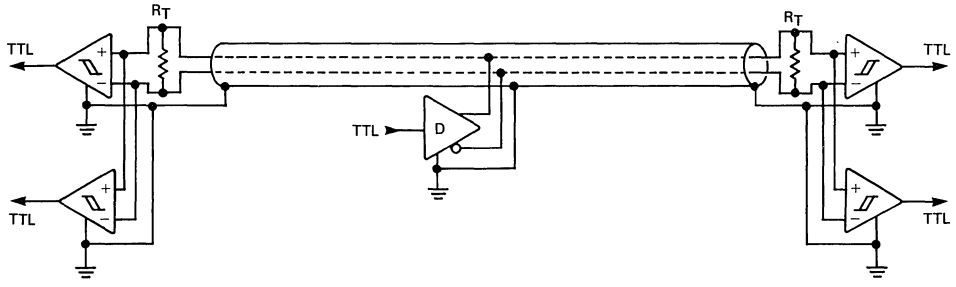


FIGURE 17 — EIA-422 APPLICATION



Notes: 1) R_T must equal characteristic impedance of the cable.
2) Individual receivers may be MC34050, MC34051, MC3486, or AM26LS32.
3) System ground may be made through cable shield as shown, or through chassis ground. Common mode differences and signal quality must be considered when choosing a ground path.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC34142

Advance Information

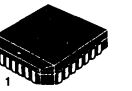
High Performance Decoder/ Sink Driver

The MC34142 is a high performance 4 to 16 multiplexed driver. This integrated circuit features a 4 to 16 decoder, 16 open drain N-channel MOS output devices with clamp diodes. The outputs are controlled by 4 address inputs, an output enable, and a chip enable.

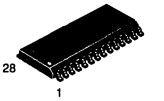
Typical applications include solenoid drivers, LED drivers, lamp drivers, and relay drivers.

This device is offered in a PLCC and a wide body surface mount package.

- SMARTMOS™ Technology
- 35 V Maximum Output Off-State Voltage
- 500 mA Maximum Output Sink Current
- Regulated Output Saturation Voltage
- 16 Open Drain MOS Outputs
- 4 Input CMOS Decoder
- Chip Select and Output Enable Input Pins
- Internal Freewheel Diodes
- Functional Equivalent to the UCN5816A

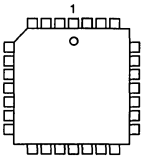


FN SUFFIX
PLASTIC PACKAGE
CASE 776



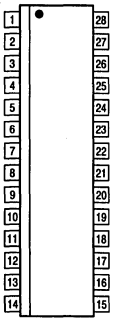
DW SUFFIX
PLASTIC PACKAGE
CASE 751F
(SO-28L)

PIN CONNECTIONS



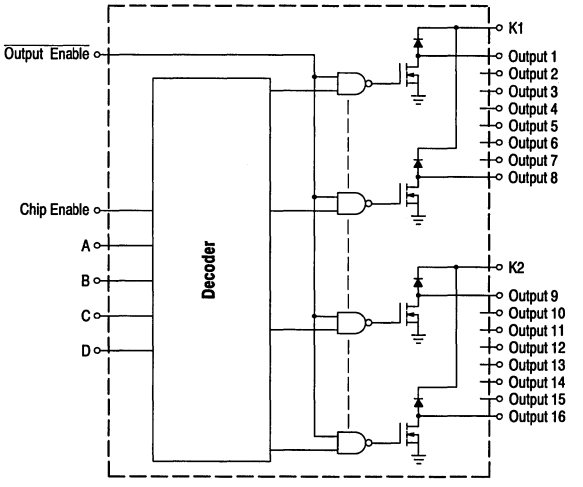
(Top View)

Pin 1.	Chip Enable	11. Output 6	20. Output 13
2.	N.C.	12. Output 7	21. Output 14
3.	V_{CC}	13. Output 8	22. Output 15
4.	Output Enable	14. Ground	23. Output 16
5.	K1	15. Ground	24. K2
6.	Output 1	16. Output 9	25. Input A
7.	Output 2	17. Output 10	26. Input B
8.	Output 3	18. Output 11	27. Input C
9.	Output 4	19. Output 12	28. Input D
10.	Output 5		



(Top View)

Simplified Block Diagram



ORDERING INFORMATION

Device	Temperature Range	Package
MC34142FN	0° to + 70°C	PLCC
MC34142DW		SO-28L

MAXIMUM RATING

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	7.0	V
Output Voltage	V_O	35	V
Drive Output Sink Current (Note 1) Continuous Pulsed (10 μs)	I_O	 500 1000	mA
Power Dissipation and Thermal Characteristics FN Suffix, Plastic Package, Case 776 T_A = 25°C Thermal Resistance, Junction to Air DW Suffix, Plastic Package, Case 751F T_A = 25°C Thermal Resistance, Junction to Air	 P_D $R_{\theta JA}$ P_D $R_{\theta JA}$	 1.9 66 1.5 80	 W °C/W W °C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature MC34142	T_A	 0 to + 70	°C
Storage Temperature	T_{stg}	− 55 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, for typical values T_A = 25°C, for min/max values T_A = 0° to + 70°C.)

Characteristic	Symbol	Min	Typ	Max	Unit
POWER SUPPLY SECTION					
Logic Supply Voltage	V_{CC}	4.75	5.0	5.25	V
Supply Current Outputs Off Outputs On	I_{CC}	 — —	 — —	 0.5 4.0	mA
LOGIC INPUT SECTION					
Input Threshold Voltage — High State Logic 1 — Low State Logic 0	V_{IH} V_{IL}	2.2 —	— —	— 0.8	V
Input Current (V_{in} = 5.0 V)	I_{IN}	—	—	20	μA
OUTPUT SECTION					
Output Saturation Voltage I_{Sink} = 100 mA I_{Sink} = 400 mA	V_{Sat}	 1.1 1.2	 — —	 1.3 1.4	V
Output Leakage Current (V_O = 35)	I_{Leak}	—	—	100	μA
Clamp Diode Leakage Current (V_R = 35 V)	I_R	—	—	100	μA
Clamp Diode Forward Voltage $I_{forward}$ = 100 mA $I_{forward}$ = 400 mA	V_F	 0.8 1.1	 — —	 1.2 1.6	V
SWITCHING CHARACTERISTICS (T_A = 25°C)					
Output Rise Time	t_r	—	40	—	ns
Output Fall Time	t_f	—	40	—	ns
Propagation Delay Time $\overline{\text{Output Enable}}$ Low to Output Low $\overline{\text{Output Enable}}$ High to Output High	 t_{pll} t_{phh}	 50 50	 — —	 150 150	ns
Setup Time, Data to $\overline{\text{Output Enable}}$	t_{su}	—	40	—	ns
Hold Time, $\overline{\text{Output Enable}}$ to Data	t_h	—	40	—	ns

APPLICATION CIRCUIT INFORMATION

The MC34142 is a high performance 4 x 16 multiplexed driver. This integrated circuit features a 4 x 16 decoder, 16 open-drain output devices with clamp diodes, an output enable, and a chip enable. Typical applications include solenoid drivers, LED drivers, lamp drivers, and relay drivers.

The inputs to this device are TTL/CMOS compatible, making them ideal to be driven from a microcomputer. Table 1 is a truth table for the input logic versus the appropriate activated output. Notice, for a specific input, only one output can be activated.

The outputs on the MC34142 are open drain DMOS power MOSFETs. Each output is capable of sinking in excess of 500 mA. The outputs have been uniquely designed to control the "on-resistance" of the power MOSFET. The voltage drop across the MOSFET is regulated and temperature compensated to give a consistent saturation voltage characteristic over load and temperature. Figure 2 shows a curve of the Output Saturation Voltage versus Sink Current.

Each output also has a flyback diode clamp to protect the device from inductive load kickbacks. Special care should be taken when laying out the printed circuit board to use these clamp diodes effectively. A capacitor should be placed close to the K1 and K2 clamp outputs.

Figure 1. Typical Application

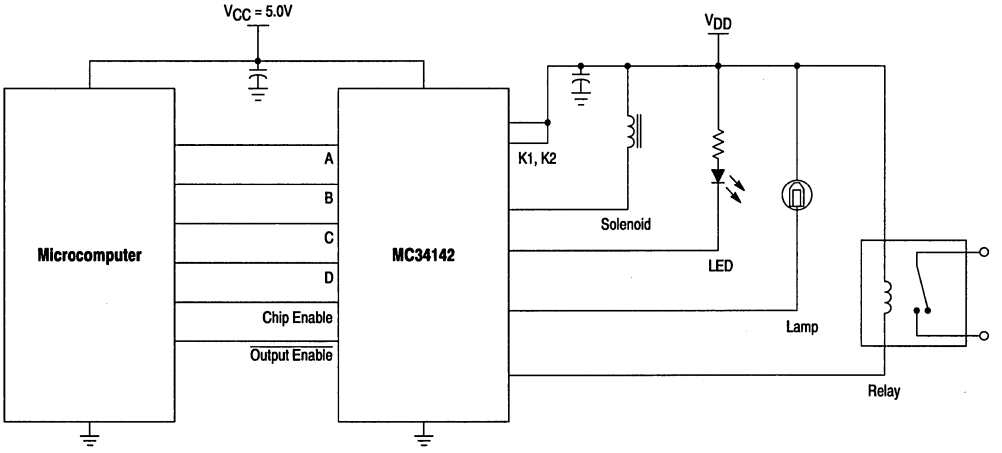


Figure 2. Output Saturation Voltage versus Load Current

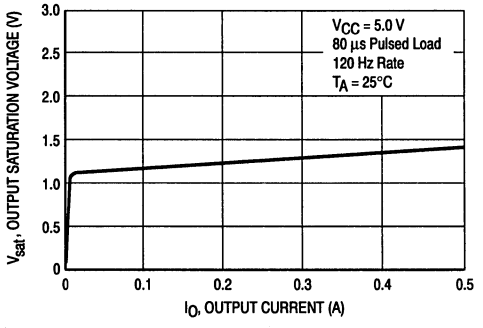


Figure 3. Propagation Delay

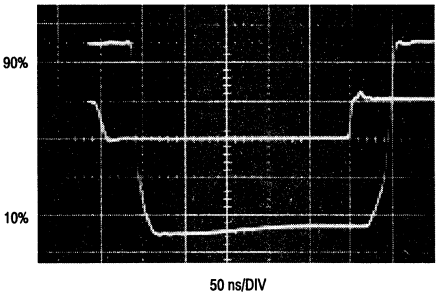


Figure 4. Output "Turn-On" Time

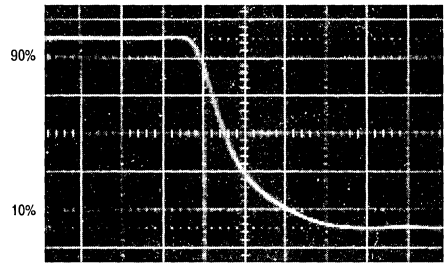


Figure 5. Output "Turn-Off" Time

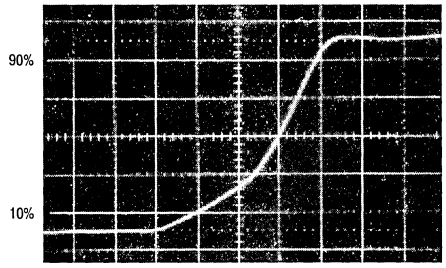


Table 1. Truth Table

$\overline{\text{Output Enable}}$	Chip Enable	Data Inputs D	C	B	A	Selected Output Active Low
0	1	0	0	0	0	Output 1
0	1	0	0	0	1	Output 2
0	1	0	0	1	0	Output 3
0	1	0	0	1	1	Output 4
0	1	0	1	0	0	Output 5
0	1	0	1	0	1	Output 6
0	1	0	1	1	0	Output 7
0	1	0	1	1	1	Output 8
0	1	1	0	0	0	Output 9
0	1	1	0	0	1	Output 10
0	1	1	0	1	0	Output 11
0	1	1	0	1	1	Output 12
0	1	1	1	0	0	Output 13
0	1	1	1	0	1	Output 14
0	1	1	1	1	0	Output 15
0	1	1	1	1	1	Output 16
x	0	x	x	x	x	All Outputs High
1	x	x	x	x	x	

MC75107
MC75108

DUAL LINE RECEIVERS

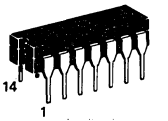
The MC75107 and MC75108 are MTTL compatible dual line receivers featuring independent channels with common voltage supply and ground terminals. The MC75107 circuit features an active pull-up (totem-pole) output. The MC75108 circuit features an open-collector output configuration that permits the Wired-OR logic connection with similar outputs (such as the MC5401/MC7401 MTTL gate or additional MC75108 receivers). Thus a level of logic is implemented without extra delay.

The MC75107 and MC75108 circuits are designed to detect input signals of greater than 25 millivolts amplitude and convert the polarity of the signal into appropriate MTTL compatible output logic levels.

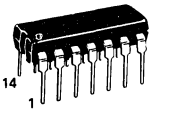
- High Common-Mode Rejection Ratio
- High Input Impedance
- High Input Sensitivity
- Differential Input Common-Mode Voltage Range of ±3.0 V
- Differential Input Common-Mode Voltage of More Than ± 15 V Using External Attenuator
- Strobe Inputs for Receiver Selection
- Gate Inputs for Logic Versatility
- MTTL or MDTL Drive Capability
- High DC Noise Margins
- MC55107 Available as JM38510/10401

DUAL LINE RECEIVERS

SILICON MONOLITHIC
INTEGRATED CIRCUITS

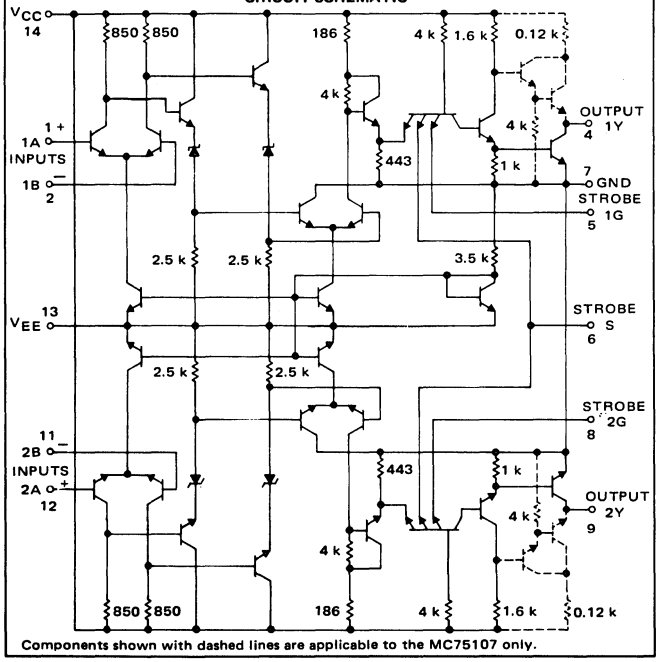


L SUFFIX
CERAMIC PACKAGE
CASE 632



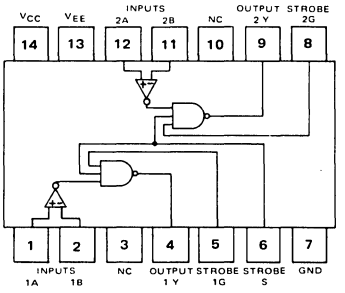
P SUFFIX
PLASTIC PACKAGE
CASE 646

CIRCUIT SCHEMATIC



Components shown with dashed lines are applicable to the MC75107 only.

PIN CONNECTIONS



TRUTH TABLE

Differential Inputs A-B	Strobes G	Strobes S	Output Y
$V_{ID} \geq 25$ mV	L or H	L or H	H
-25 mV $< V_{ID} <$ 25 mV	L or H	L	H
	L	L or H	H
	H	H	Indeterminate
$V_{ID} \leq -25$ mV	L or H	L	H
	L	L or H	H
	H	H	L

MAXIMUM RATINGS (T_A = 0°C to +70°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltages	V_{CC} V_{EE}	+7.0 −7.0	Vdc
Differential-Mode Input Signal Voltage Range	V_{ID}	±6.0	Vdc
Common-Mode Input Voltage Range	V_{ICR}	±5.0	Vdc
Strobe Input Voltage	$V_{I(S)}$	5.5	Vdc
Power Dissipation (Package Limitation) Plastic and Ceramic Dual-In-Line Packages Derate above T_A = +25°C	P_D	 625 3.85	 mW mW/°C
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Voltages	V_{CC} V_{EE}	+4.75 −4.75	+5.0 −5.0	+5.25 −5.25	Vdc
Output Sink Current	I_{OS}	—	—	−16	mA
Differential-Mode Input Voltage Range	V_{IDR}	−5.0	—	+5.0	Vdc
Common-Mode Input Voltage Range	V_{ICR}	−3.0	—	+3.0	Vdc
Input Voltage Range, any differential input to ground	V_{IR}	−5.0	—	+3.0	Vdc
Operating Temperature Range	T_A	0	—	+70	°C

DEFINITIONS OF INPUT LOGIC LEVELS

Characteristic	Symbol	Test Fig.	Min	Max	Unit
High-Level Input Voltage (between differential inputs)	V_{IDH}	1	0.025	5.0	Vdc
Low-Level Input Voltage (between differential inputs)	V_{IDL}	1	−5.0†	−0.025	Vdc
High-Level Input Voltage (at strobe inputs)	$V_{IH(S)}$	3	2.0	5.5	Vdc
Low-Level Input Voltage (at strobe inputs)	$V_{IL(S)}$	3	0	0.8	Vdc

†The algebraic convention, where the most positive limit is designated maximum, is used with Low-Level Input Voltage Level (V_{IDL})

ELECTRICAL CHARACTERISTICS (T_A = 0°C to +70°C unless otherwise noted)

Characteristic	Symbol	Test Fig.	Min	Typ #	Max	Unit
High-Level Input Current to 1A or 2A Input (V_{CC} = Max, V_{EE} = Max, V_{ID} = 0.5 V, V_{IC} = −3.0 V to +3.0 V) (1)	I_{IH}	2	—	30	75	μA
Low-Level Input Current to 1A or 2A Input (V_{CC} = Max, V_{EE} = Max, V_{ID} = −2.0 V, V_{IC} = −3.0 V to +3.0 V) (1)	I_{IL}	2	—	—	−10	μA
High-Level Input Current to 1G or 2G Input (V_{CC} = Max, V_{EE} = Max, $V_{IH(S)}$ = 2.4 V) (1) (V_{CC} = Max, V_{EE} = Max, $V_{IH(S)}$ = V_{CC} Max) (1)	I_{IH}	4	— —	— —	40 1.0	μA mA
Low-Level Input Current to 1G or 2G Input (V_{CC} = Max, V_{EE} = Max, $V_{IL(S)}$ = 0.4 V) (1)	I_{IL}	4	—	—	−1.6	mA
High-Level Input Current to S Input (V_{CC} = Max, V_{EE} = Max, $V_{IH(S)}$ = 2.4 V) (1) (V_{CC} = Max, V_{EE} = Max, $V_{IH(S)}$ = V_{CC} Max) (1)	I_{IH}	4	— —	— —	80 2.0	μA mA
Low-Level Input Current to S Input (V_{CC} = Max, V_{EE} = Max, $V_{IL(S)}$ = 0.4 V) (1)	I_{IL}	4	—	—	−3.2	mA
High-Level Outut Voltage (V_{CC} = Min, V_{EE} = Min, I_{load} = −400 μA, V_{IC} = −3.0 V to +3.0 V) (1)	V_{OH}	3	—	—	—	V
Low-Level Output Voltage (V_{CC} = Min, V_{EE} = Min, I_{sink} = 16 mA, V_{IC} = −3.0 V to +3.0 V) (1)	V_{OL}	3	—	—	0.4	V
High-Level Leakage Current (V_{CC} = Min, V_{EE} = Min, V_{OH} = V_{CC} Max) (1)	I_{CEX}	3	—	—	250	μA
Short-Circuit Output Current (3) (V_{CC} = Max, V_{EE} = Max) (1)	I_{OSC}	5	—	—	—	mA
High Logic Level Supply Current from V_{CC} (V_{CC} = Max, V_{EE} = Max, V_{ID} = 25 mV, T_A = +25°C) (1)	I_{CCH+}	6	—	18	30	mA
High Logic Level Supply Current from V_{EE} (V_{CC} = Max, V_{EE} = Max, V_{ID} = 25 mV, T_A = +25°C) (1)	I_{CCH-}	6	0	8.4	−15	mA

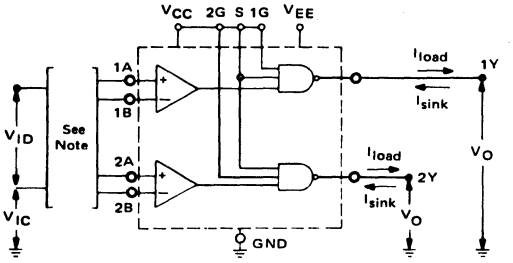
NOTES:
1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. All typical values are at V_{CC} = +5.0 V, V_{EE} = −5.0 V, T_A = +25°C.
3. Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (V_{CC} = +5.0 V, V_{EE} = -5.0 V, T_A = +25°C)

Characteristic	Symbol	Test Fig.	Min	Typ	Max	Unit
Propagation Delay Time, low-to-high level from differential inputs A and B to output	$t_{PLH(D)}$	7				ns
(R_L = 390 Ω, C_L = 50 pF)			–	–	–	
(R_L = 390 Ω, C_L = 15 pF)			–	19	25	
Propagation Delay Time, high-to-low level from differential inputs A and B to output	$t_{PHL(D)}$	7				ns
(R_L = 390 Ω, C_L = 50 pF)			–	–	–	
(R_L = 390 Ω, C_L = 15 pF)			–	19	25	
Propagation Delay Time, low-to-high level, from strobe input G or S to output	$t_{PLH(S)}$	7				ns
(R_L = 390 Ω, C_L = 50 pF)			–	–	–	
(R_L = 390 Ω, C_L = 15 pF)			–	13	15	
Propagation Delay Time, high-to-low level, from strobe input G or S to output	$t_{PHL(S)}$	7				ns
(R_L = 390 Ω, C_L = 50 pF)			–	–	–	
(R_L = 390 Ω, C_L = 15 pF)			–	13	20	15

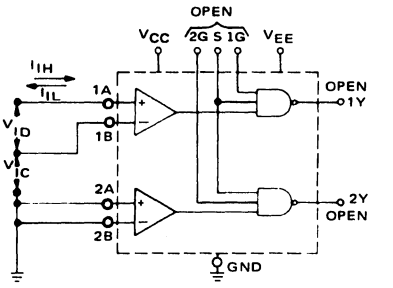
TEST CIRCUITS

FIGURE 1 – V_{IDH} and V_{IDL}



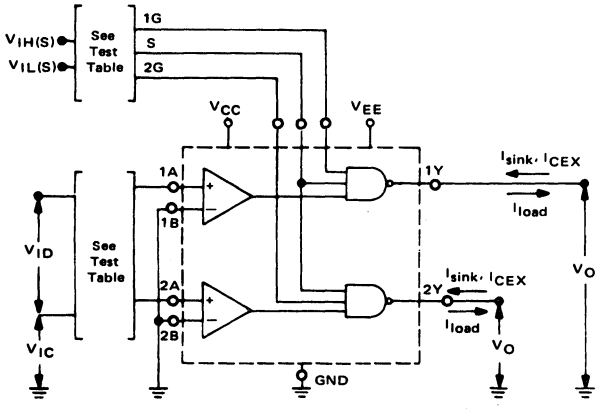
NOTE: When testing one channel, the inputs of the other channel are grounded.

FIGURE 2 – I_{IH} and I_{IL}



NOTE: Each pair of differential inputs is tested separately. The inputs of the other pair are grounded

FIGURE 3 – $V_{IH(S)}$, $V_{IL(S)}$, V_{OH}, V_{OL}, and I_{OH}



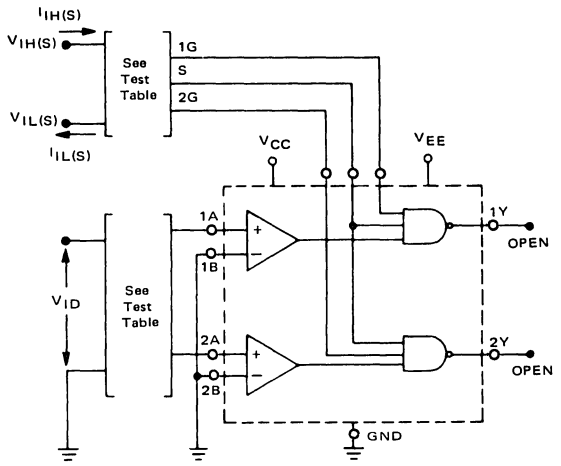
TEST TABLE

MC75107	MC75108	V_{ID}	STROBE 1G or 2G	STROBE S
TEST		APPLY		
V_{OH}	I_{CEX}	+25 mV	$V_{IH(S)}$	$V_{IH(S)}$
V_{OH}	I_{CEX}	-25 mV	$V_{IL(S)}$	$V_{IH(S)}$
V_{OH}	I_{CEX}	-25 mV	$V_{IH(S)}$	$V_{IL(S)}$
V_{OL}	V_{OL}	-25 mV	$V_{IH(S)}$	$V_{IH(S)}$

NOTES: 1. V_{IC} = -3.0 V to +3.0 V.
2. When testing one channel, the inputs of the other channel should be grounded.

TEST CIRCUITS (continued)

FIGURE 4 – $I_{IH(G)}$, $I_{IL(G)}$, $I_{IH(S)}$, and $I_{IL(S)}$



TEST	INPUT 1A	INPUT 2A	STROBE 1G	STROBE S	STROBE 2G
I_{IH} at Strobe 1G	+25 mV	Gnd	$V_{IH(S)}$	Gnd	Gnd
I_{IH} at Strobe 2G	Gnd	+25 mV	Gnd	Gnd	$V_{IH(S)}$
I_{IH} at Strobe S	+25 mV	+25 mV	Gnd	$V_{IH(S)}$	Gnd
I_{IL} at Strobe 1G	-25 mV	Gnd	$V_{IL(S)}$	4.5 V	Gnd
I_{IL} at Strobe 2G	Gnd	-25 mV	Gnd	4.5 V	$V_{IL(S)}$
I_{IL} at Strobe S	-25 mV	-25 mV	4.5 V	$V_{IL(S)}$	4.5 V

FIGURE 5 – I_{OS}

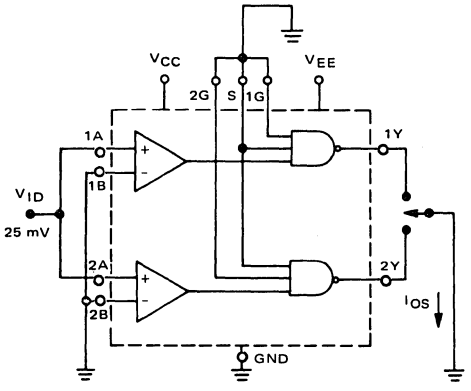
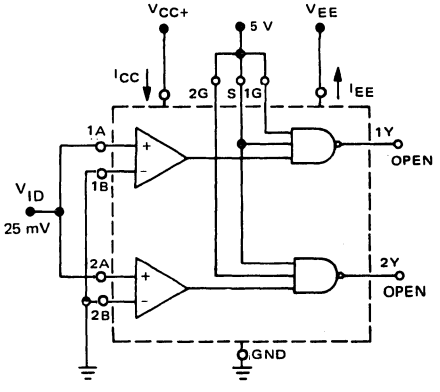


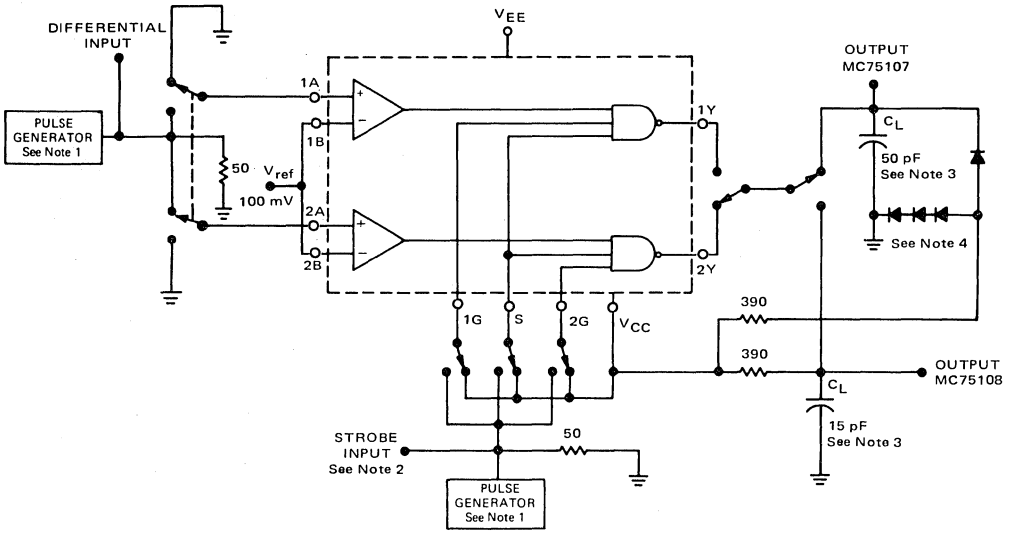
FIGURE 6 – I_{CC} and I_{EE}

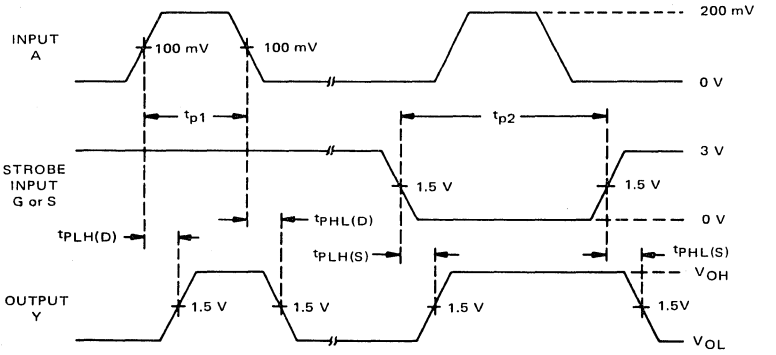


NOTES: 1. Each channel is tested separately.
2. Not more than one output should be tested at one time.

TEST CIRCUITS (continued)

FIGURE 7 – PROPAGATION DELAY TIME TEST CIRCUIT AND WAVEFORMS





NOTES: 1. The pulse generators have the following characteristics: $z_o = 50\ \Omega$, $t_r = t_f = 10 \pm 5$ ns, $t_{p1} = 500$ ns, PRR = 1 MHz $t_{p2} = 1\ \mu s$, PRR = 500 kHz.
2. Strobe input pulse is applied to Strobe 1G when Inputs 1A-1B are being tested, to Strobe S when Inputs 1A-1B or 2A-2B are being tested, and to Strobe 2G when inputs 2A-2B are being tested.
3. C_L includes probe and jig capacitance.
4. All diodes are 1N916 or equivalent.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC75S110

MONOLITHIC DUAL LINE DRIVERS

DUAL LINE DRIVERS

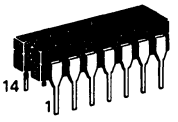
SILICON MONOLITHIC INTEGRATED CIRCUIT

The MC75S110 dual line driver features independent channels with common voltage supply and ground terminals. Each driver circuit provides a constant output current that switches to either of two output terminals subject to the appropriate logic levels at the input.terminals. Output current can be switched "off" (inhibited) by appropriate logic levels at the inhibit inputs. Output current is nominally twelve milliamperes.

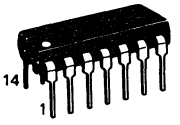
The inhibit feature permits use in party-line or data-bus applications. A strobe or inhibitor, common to both drivers, is included to increase driver-logic versatility. With output current in the inhibited mode, $I_{O(off)}$ is specified so that minimum line loading occurs when the driver is used in a party-line system with other drivers. Output impedance of the driver in inhibited mode is very high (the output impedance of a transistor biased to cutoff).

All driver outputs have a common-mode voltage range of −3.0 volts to +3.0 volts, allowing common-mode voltage on the line without affecting driver performance.

- Insensitive to Supply Variations Over the Entire Operating Range
- MTTL Input Compatibility
- Current-Mode Output (12 mA Typical)
- High Output Impedance
- Common-Mode Output Voltage Range (−3.0 V to +3.0 V)
- Inhibitor Available for Driver Selection



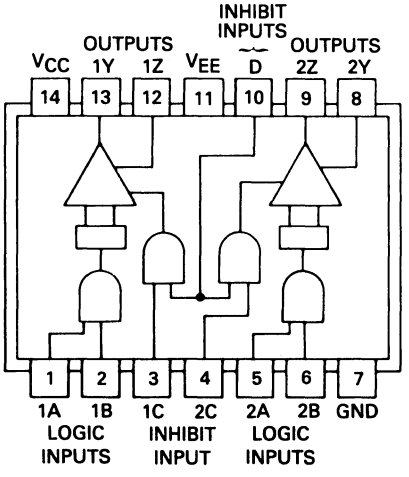
L SUFFIX
CERAMIC PACKAGE
CASE 632



P SUFFIX
PLASTIC PACKAGE
CASE 646

7

PIN CONNECTIONS



TRUTH TABLE

LOGIC INPUTS		INHIBITOR INPUTS		OUTPUTS	
A	B	C	D	Y	Z
L or H	L or H	L	L or H	H	H
L or H	L or H	L or H	L	H	H
L	L or H	H	H	L	H
L or H	L	H	H	L	H
H	H	H	H	H	L

Low output represents the "on" state.
High output represents the "off" state.

MAXIMUM RATINGS (T_A = 0 to +70°C unless otherwise noted.)

Ratings	Symbol	Value	Unit
Power Supply Voltages (See Note 1)	V_{CC} V_{EE}	+7.0 −7.0	Volts
Logic and Inhibitor Input Voltages (See Note 1)	V_{in}	5.5	Volts
Common-Mode Output Voltage Range (See Note 1)	V_{OCR}	−5.0 to +7.0	Volts
Power Dissipation (Package Limitation) Plastic and Ceramic Dual In-Line Packages Derate above T_A = +25°C	P_D	 1000 3.85	 mW mW/°C
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

NOTE 1. These voltage values are with respect to the ground terminal.

RECOMMENDED OPERATING CONDITIONS (See Notes 1 and 2.)

Characteristic	Symbol	Min	Nom	Max	Unit
Power Supply Voltages	V_{CC} V_{EE}	+4.75 −4.75	+5.0 −5.0	+5.25 −5.25	Volts
Common-Mode Output Voltage Range	V_{OCR}	−3.0	—	+3.0	Volts

NOTE 2. When using only one channel of the line drivers, the other channel should be inhibited and/or its outputs grounded.

DEFINITIONS OF INPUT LOGIC LEVELS*

Characteristic	Symbol	Test Figure	Min	Max	Unit
High-Level Input Voltage (at any input)	V_{IH}	1,2	2.0	5.25	Volts
Low-Level Input Voltage (at any input)	V_{IL}	1,2	0	0.8	Volts

* The algebraic convention, where the most positive limit is designated maximum, is used with Logic Level Input Voltage Levels only.

THERMAL INFORMATION

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature, can be found from the equation:

$$P_{D(T_A)} = \frac{T_{J(max)} - T_A}{R_{\theta JA}\ (Typ)}$$

Where: $P_{D(T_A)}$ = Power Dissipation allowable at a given operating ambient temperature. This must be greater than the sum of the products of the supply voltages and supply currents at the worst case operating condition.

$T_{J(max)}$ = Maximum Operating Junction Temperature as listed in the Maximum Ratings Section

T_A = Maximum Desired Operating Ambient Temperature

$R_{\theta JA}$ (Typ) = Typical Thermal Resistance Junction to Ambient

ELECTRICAL CHARACTERISTICS (T_A = 0 to +70°C unless otherwise noted.)

Characteristic**	Symbol	Test Figure	Min	Typ*	Max	Unit
High-Level Input Current to 1A, 1B, 2A or 2B (V_{CC} = Max, V_{EE} = Max, V_{IH_L} = 2.4 V)* (V_{CC} = Max, V_{EE} = Max, V_{IH_L} = V_{CC} Max)	I_{IH_L}	1	 — —	 — —	 40 1.0	 μA mA
Low-Level Input Current to 1A, 1B, 2A or 2B (V_{CC} = Max, V_{EE} = Max, V_{IL_L} = 0.4 V)	I_{IL_L}	1	—	—	−3.0	mA
High-Level Input Current into 1C or 2C (V_{CC} = Max, V_{EE} = Max, V_{IH_I} = 2.4 V) (V_{CC} = Max, V_{EE} = Max, V_{IH_I} = V_{CC} Max)	I_{IH_I}	1	 — —	 — —	 40 1.0	 μA mA
Low-Level Input Current into 1C or 2C (V_{CC} = Max, V_{EE} = Max, V_{IL_I} = 0.4 V)	I_{IL_I}	1	—	—	−3.0	mA
High-Level Input Current into D (V_{CC} = Max, V_{EE} = Max, V_{IH_I} = 2.4 V) (V_{CC} = Max, V_{EE} = Max, V_{IH_I} = V_{CC} Max)	I_{IH_I}	1	 — —	 — —	 80 2.0	 μA mA
Low-Level Input Current into D (V_{CC} = Max, V_{EE} = Max, V_{IL_I} = 0.4 V)	I_{IL_I}	1	—	—	−6.0	mA
Output Current ("on" state) (V_{CC} = Max, V_{EE} = Max) (V_{CC} = Min, V_{EE} = Min)	$I_{O(on)}$	2	 — 6.5	 12 —	 15 —	mA
Output Current ("off" state) (V_{CC} = Max, V_{EE} = Max) (V_{CC} = Min, V_{EE} = Min)	$I_{O(off)}$	2	 — —	 — —	 100 100	μA
Supply Current from V_{CC} (with driver enabled) (V_{IL_L} = 0.4 V, V_{IH_I} = 2.0 V)	$I_{CC(on)}$	3	—	—	35	mA
Supply Current from V_{EE} (with driver enabled) (V_{IL_L} = 0.4 V, V_{IH_I} = 2.0 V)	$I_{EE(on)}$	3	—	—	−50	mA
Supply Current from V_{CC} (with driver inhibited) (V_{IL_L} = 0.4 V, V_{IL_I} = 0.4 V)	$I_{CC(off)}$	3	—	—	35	mA
Supply Current from V_{EE} (with driver inhibited) (V_{IL_L} = 0.4 V, V_{IL_I} = 0.4 V)	$I_{EE(off)}$	3	—	—	−50	mA

*All typical values are at V_{CC} = +5.0 V, V_{EE} = −5.0 V.
**For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions.

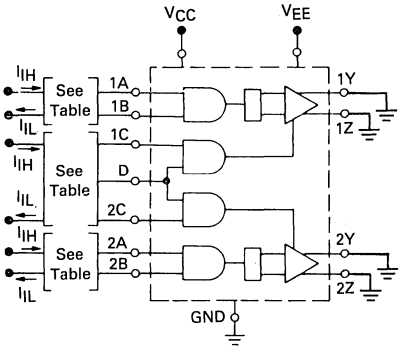
SWITCHING CHARACTERISTICS (V_{CC} = +5.0 V, V_{EE} = −5.0 V, T_A = +25°C.)

Characteristic	Symbol	Test Figure	Min	Typ	Max	Unit
Propagation Delay Time from Logic Input A or B to Output Y or Z (R_L = 50 ohms, C_L = 40 pF)	t_{PLH_L} t_{PHL_L}	4	— —	9.0 9.0	15 15	ns
Propagation Delay Time from Inhibitor Input C or D to Output Y or Z (R_L = 50 ohms, C_L = 40 pF)	t_{PLH_I} t_{PHL_I}	4	— —	16 13	25 25	ns

7

TEST CIRCUITS

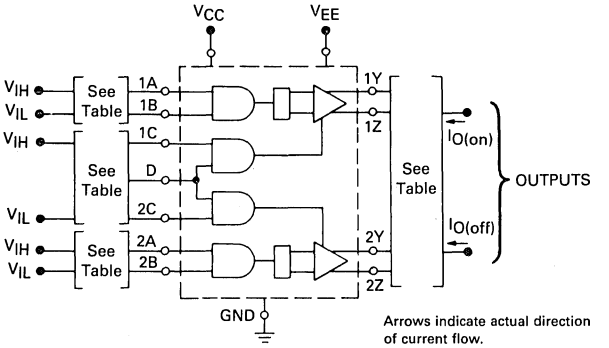
FIGURE 1 — I_{IH}, I_{IL}



TEST TABLE

TEST AT ANY INPUT	ADJACENT INPUTS NOT UNDER TEST
I_{IH}	GND
I_{IL}	4.5 V

FIGURE 2 — $I_{O(on)}$ and $I_{O(off)}$



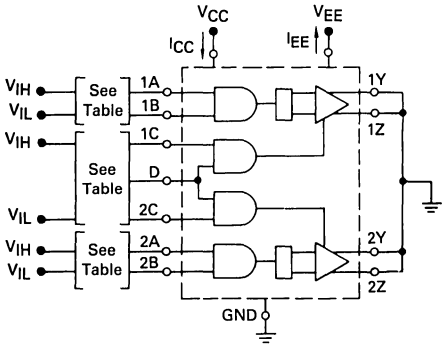
Arrows indicate actual direction of current flow.

TEST TABLE

TEST Ground all output pins not under test.		LOGIC INPUTS		INHIBITOR INPUTS	
		1A or 2A	1B or 2B	1C or 2C	D
$I_{O(on)}$	at output 1Y or 2Y	V_{IL}	V_{IL}	V_{IH}	V_{IH}
		V_{IL}	V_{IH}		
		V_{IH}	V_{IL}		
$I_{O(on)}$	at output 1Z or 2Z	V_{IH}	V_{IH}	V_{IH}	V_{IH}
$I_{O(off)}$	at output 1Y or 2Y	V_{IH}	V_{IH}	V_{IH}	V_{IH}
$I_{O(off)}$	at output 1Z or 2Z	V_{IL}	V_{IL}	V_{IH}	V_{IH}
		V_{IL}	V_{IH}		
		V_{IH}	V_{IL}		
$I_{O(off)}$	at output 1Y, 2Y, 1Z, or 2Z	Either state	Either state	V_{IL}	V_{IL}
				V_{IL}	V_{IH}
				V_{IH}	V_{IL}

TEST CIRCUITS (continued)

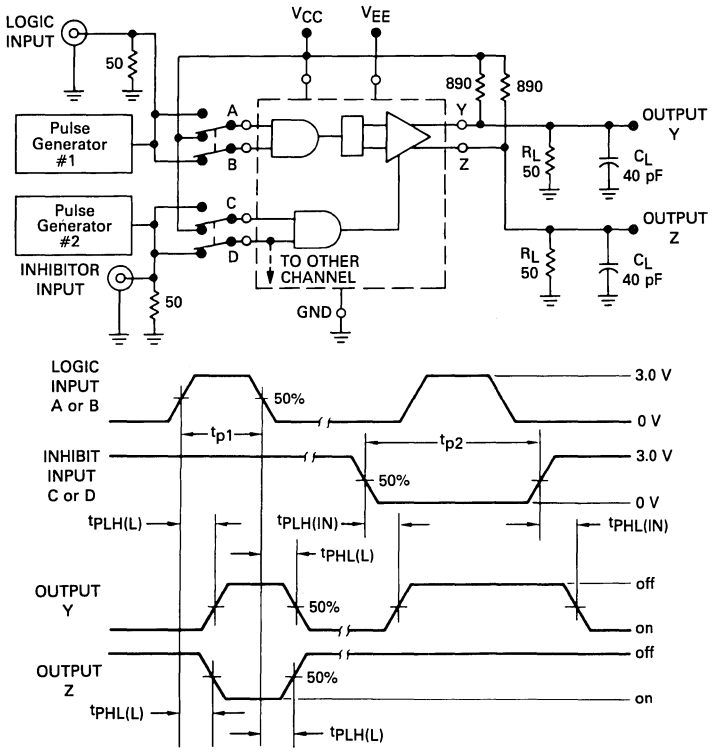
FIGURE 3 — I_{CC} and I_{EE}



TEST TABLE

TEST		ALL LOGIC INPUTS	ALL INHIBITOR INPUTS
I_{CC}(on)	Driver enabled	V_{IL}	V_{IH}
I_{EE}(on)	Driver enabled	V_{IL}	V_{IH}
I_{CC}(off)	Driver inhibited	V_{IL}	V_{IL}
I_{EE}(off)	Driver inhibited	V_{IL}	V_{IL}

FIGURE 4 — PROPAGATION DELAY TIMES TEST CIRCUIT AND WAVEFORMS



NOTES: 1. The pulse generators have the following characteristics: z_o = 50 Ω, t_r = t_f = 10 ± 5.0 ns t_{p1} = 500 ns, PRR = 1.0 MHz, t_{p2} = 1.0 ms, PRR = 500 kHz.
2. C_L includes probe and jig capacitance.
3. For simplicity, only one channel and the inhibitor connections are shown.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC75172B
MC75174B

Advance Information

Quad EIA-485 Line Drivers with Three-State Outputs

QUAD EIA-485 LINE DRIVERS

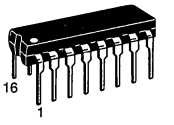
SILICON MONOLITHIC INTEGRATED CIRCUIT

The Motorola MC75172B/174B Quad Line drivers are differential high speed drivers designed to comply with the EIA-485 Standard. Features include three-state outputs, thermal shutdown, and output current limiting in both directions. These devices also comply with EIA-422-A, and CCITT Recommendations V.11 and X.27.

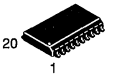
The MC75172B/174B are optimized for balanced multipoint bus transmission at rates in excess of 10 MBPS. The outputs feature wide common mode voltage range, making them suitable for party line applications in noisy environments. The current limit and thermal shutdown features protect the devices from line fault conditions. These devices offer optimum performance when used with the MC75173 and MC75175 line receivers.

Both devices are available in 16-pin plastic DIP and 20-pin wide body surface mount packages.

- Meets EIA-485 Standard for Party Line Operation
- Meets EIA-422-A and CCITT Recommendations V.11 and X.27
- Operating Ambient Temperature: –40°C to +85°C
- High Impedance Outputs
- Common Mode Output Voltage Range: –7 to +12 V
- Positive and Negative Current Limiting
- Transmission Rates in Excess of 10 MBPS
- Thermal Shutdown at 150°C Junction Temperature, (±20°C)
- Single +5.0 V Supply
- Pin Compatible with TI SN75172/4 and NS μA96172/4
- Interchangeable with MC3487 and AM26LS31 for EIA-422-A Applications



P SUFFIX
PLASTIC PACKAGE
CASE 648



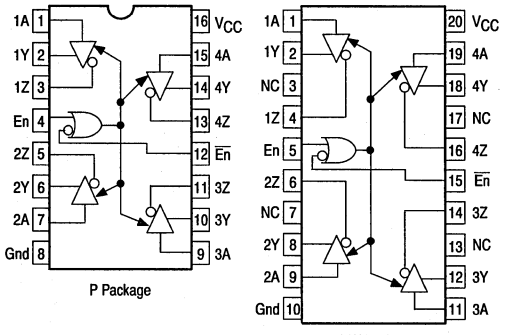
D SUFFIX
PLASTIC PACKAGE
CASE 751D
(SO-20L)

ORDERING INFORMATION

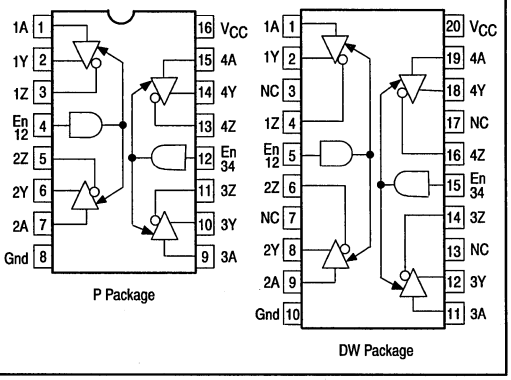
Device	Temperature Range	Package
MC75172BDW	– 40° to +85°C	SO-20L
MC75172BP		Plastic DIP
MC75174BDW		SO-20L
MC75174BP		Plastic DIP

SIMPLIFIED BLOCK DIAGRAM

MC75172B



MC75174B



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5, +7.0	Vdc
Input Voltage (Data, Enable)	V_{in}	+7.0	Vdc
Input Current (Data, Enable)	I_{in}	−24	mA
Applied Output Voltage, when in 3-State Condition (V_{CC} = 5.0 V)	V_{za}	−10, +14	Vdc
Applied Output Voltage, when V_{CC} = 0 V	V_{zb}	±14	
Output Current	I_O	Self-Limiting	—
Storage Temperature	T_{stg}	−65, +150	°C

Devices should not be operated at these limits. The "Recommended Operating Conditions" table provides for actual device operation.

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	V_{CC}	+4.75	+5.0	+5.25	Vdc
Input Voltage (All Inputs)	V_{in}	0	—	V_{CC}	Vdc
Output Voltage in 3-State Condition, or when V_{CC} = 0 V	V_{cm}	−7.0	—	+12	Vdc
Output Current (Normal data transmission)	I_O	−65	—	+65	mA
Operating Ambient Temperature (see text) EIA-485 EIA-422	T_A	 −40 0	 — —	 +85 +85	°C

All limits are not necessarily functional concurrently.

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ELECTRICAL CHARACTERISTICS (−40°C ≤ T_A ≤ +85°C, +4.75 V ≤ V_{CC} ≤ +5.25 V, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage Single-Ended Voltage					Vdc
I_O = 0	V_O	0	—	6.0	
High @ I_O = −33 mA	V_{OH}	—	4.0	—	
Low @ I_O = +33 mA	V_{OL}	—	1.6	—	
Differential Voltage					
Open Circuit (I_O = 0)	$\|V_{OD1}\|$	1.5	3.4	6.0	
R_L = 54 Ω (Figure 1)	$\|V_{OD2}\|$	1.5	2.3	5.0	
Change in Differential*, R_L = 54 Ω (Figure 1)	$\|\Delta V_{OD2}\|$	—	5.0	200	mVdc
Differential Voltage, R_L = 100 Ω (Figure 1)	$\|V_{OD2A}\|$	—	2.2	—	Vdc
Change in Differential*, R_L = 100 Ω (Figure 1)	$\|\Delta V_{OD2A}\|$	—	5.0	200	mVdc
Differential Voltage, −7.0 V ≤ V_{cm} ≤ +12 V (Figure 2)	$\|V_{OD3}\|$	1.5	—	5.0	Vdc
Change in Differential*, −7.0 V ≤ V_{cm} ≤ +12 V (Figure 2)	$\|\Delta V_{OD3}\|$	—	5.0	200	mVdc
Offset Voltage, R_L = 54 Ω (Figure 1)	V_{OS}	—	2.9	—	Vdc
Change in Offset*, R_L = 54 Ω (Figure 1)	$\|\Delta V_{OS}\|$	—	5.0	200	mVdc
Output Current (Each Output) Power Off Leakage, V_{CC} = 0, −7.0 V ≤ V_O ≤ +12 V	$I_{O(off)}$	−50	0	+50	µA
Leakage in 3-State Mode, −7.0 V ≤ V_O ≤ +12 V	I_{OZ}	−50	0	+50	
Short Circuit Current to Ground	I_{OSR}	−150	—	+150	mA
Short Circuit Current, −7.0 V ≤ V_O ≤ +12 V	I_{OS}	−250	—	+250	

*V_{in} switched from 0.8 to 2.0 V.
Typical values determined at +25°C ambient and +5.0 V supply.

ELECTRICAL CHARACTERISTICS ($-40°C \le T_A \le +85°C$, $+4.75\ V \le V_{CC} \le +5.25\ V$, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Inputs					Vdc
Low Level Voltage (Pins 4 & 12, MC75174B only)	$V_{IL(A)}$	0	—	0.7	
Low Level Voltage (All Other Pins)	$V_{IL(B)}$	0	—	0.8	
High Level Voltage (All Inputs)	V_{IH}	2.0	—	V_{CC}	
Current @ V_{in} = 2.7 V (All Inputs)	I_{IH}	—	0.2	20	μA
Current @ V_{in} = 0.5 V (All Inputs)	I_{IL}	–100	–15	—	
Clamp Voltage (All Inputs, I_{in} = –18 mA)	V_{IK}	–1.5	—	—	Vdc
Thermal Shutdown Junction Temperature	T_{jts}	—	+150	—	°C
Power Supply Current (Outputs Open, V_{CC} = +5.25 V)	I_{CC}				mA
Outputs Enable		—	60	70	
Outputs Disabled		—	30	40	

TIMING CHARACTERISTICS (T_A = +25°C, V_{CC} = +5.0 V)

Characteristics	Symbol	Min	Typ	Max	Unit
Propagation Delay — Input to Single-ended Output (Figure 3)					ns
Output Low-to-High	t_{PLH}	—	23	30	
Output High-to-Low	t_{PHL}	—	18	30	
Propagation Delay — Input to Differential Output (Figure 4)					ns
Input Low-to-High	$t_{PLH(D)}$	—	15	25	
Input High-to-Low	$t_{PHL(D)}$	—	17	25	
Differential Output Transition Time (Figure 4)	t_{dr}, t_{df}	—	19	25	ns
Skew Timing					ns
$\lvert t_{PLHD} - t_{PHLD} \rvert$ for Each Driver	t_{SK1}	—	0.2	—	
Max – Min t_{PLHD} Within a Package	t_{SK2}	—	1.5	—	
Max – Min t_{PHLD} Within a Package	t_{SK3}	—	1.5	—	
Enable TIming					ns
Single-ended Outputs (Figure 5)					
Enable to Active High Output	$t_{PZH(E)}$	—	48	60	
Enable to Active Low Output	$t_{PZL(E)}$	—	20	30	
Active High to Disable (using Enable)	$t_{PHZ(E)}$	—	35	45	
Active Low to Disable (using Enable)	$t_{PLZ(E)}$	—	30	50	
$\overline{\text{Enable}}$ to Active High Output (MC75172B only)	$t_{PZH(E)}$	—	58	70	
$\overline{\text{Enable}}$ to Active Low Output (MC75172B only)	$t_{PZL(E)}$	—	28	35	
Active High to Disable (using $\overline{\text{Enable}}$, MC75172B only)	$t_{PHZ(E)}$	—	38	50	
Active Low to Disable (using $\overline{\text{Enable}}$, MC75172B only)	$t_{PLZ(E)}$	—	36	50	
Differential Outputs (Figure 6)					ns
Enable to Active Output	$t_{PZD(E)}$	—	47	—	
$\overline{\text{Enable}}$ to Active Output (MC75172B only)	$t_{PZD(E)}$	—	56	—	
Enable to 3-State Output	$t_{PDZ(E)}$	—	32	—	
$\overline{\text{Enable}}$ to 3-State Output (MC75172B only)	$t_{PDZ(E)}$	—	40	—	

Figure 1. V_{DD} Measurement

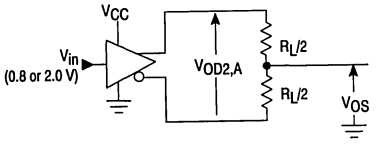


Figure 2. Common Mode Test

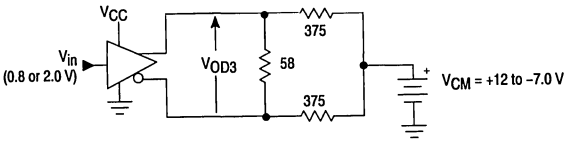


Figure 3. Propagation Delay, Single-Ended Outputs

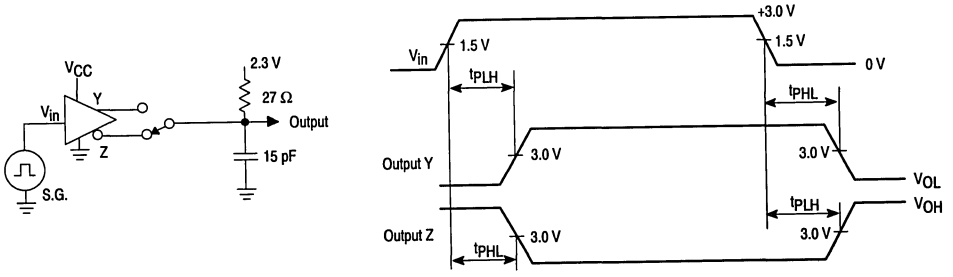
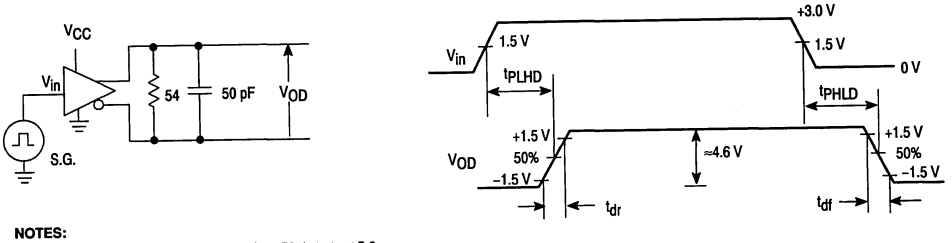


Figure 4. Propagation Delay, Differential Outputs



NOTES:

1) S.G. set to: f ≤ 1.0 MHz; duty cycle = 50%; t_r, t_f, ≤ 5.0 ns.
2) $t_{SK1} = |t_{PLHD} - t_{PHLD}|$ for each driver.
3) t_{SK2} computed by subtracting the shortest t_{PLHD} from the longest t_{PLHD} of the 4 drivers within a package.
4) t_{SK3} computed by subtracting the shortest t_{PHLD} from the longest t_{PHLD} of the 4 drivers within a package.

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Figure 5. Enable Timing, Single-Ended Outputs

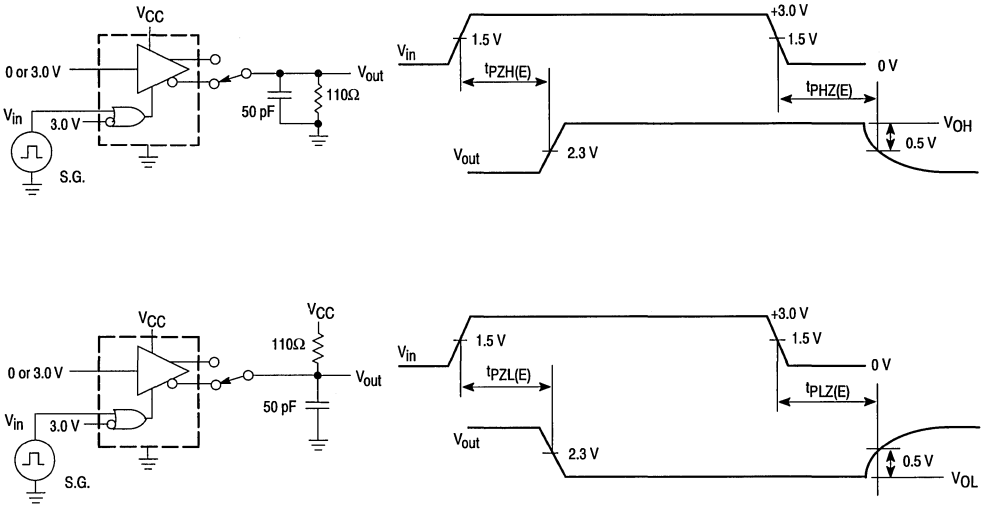
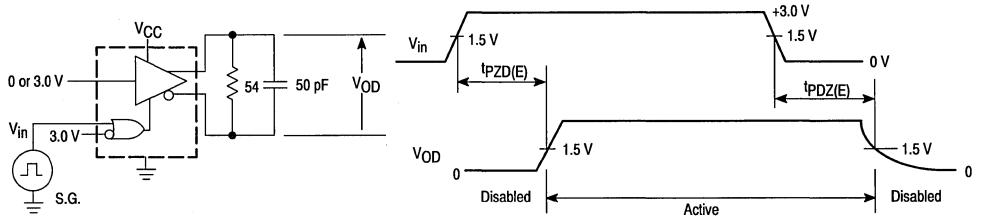


Figure 6. Enable Timing, Differential Outputs



NOTES:
1) S.G. set to: f ≤ 1.0 MHz; duty cycle = 50%; t_r, t_f, ≤ 5.0 ns.
2) V_{in} is inverted for $\overline{\text{Enable}}$ measurements.

Figure 7. Single–Ended Output Voltage versus Output Sink Current

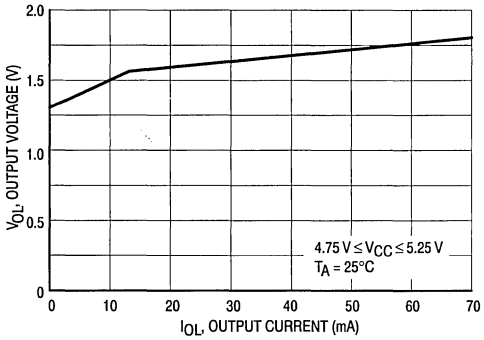


Figure 8. Single–Ended Output Voltage versus Temperature

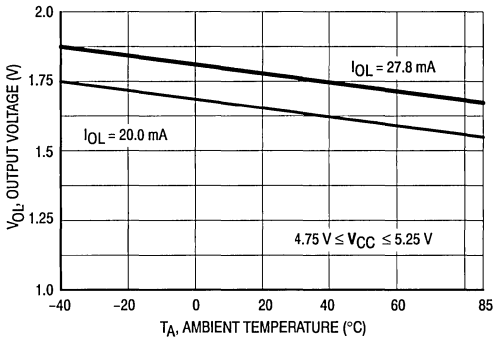


Figure 9. Single–Ended Output Voltage versus Output Source Current

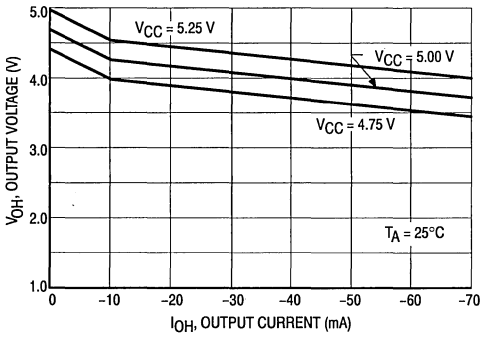


Figure 10. Single-Ended Output Voltage versus Temperature

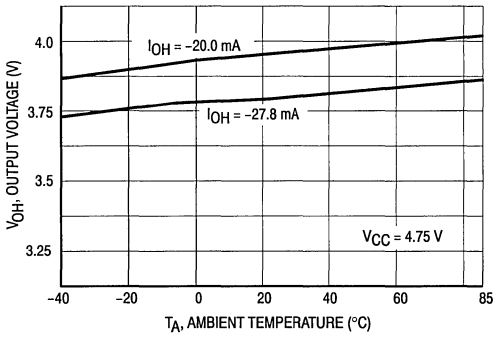


Figure 11. Output Differential Voltage versus Load Current

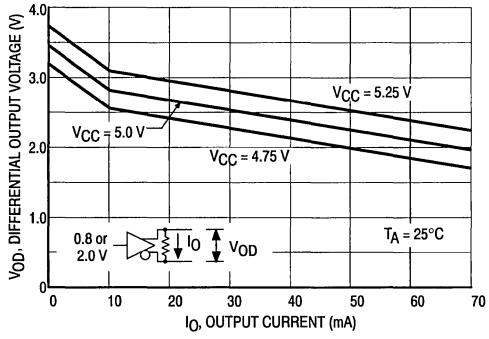


Figure 12. Output Differential Voltage versus Temperature

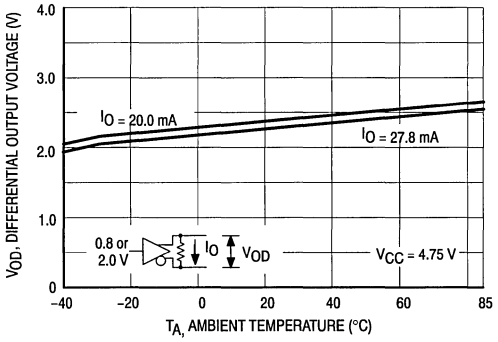


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Figure 13. Output Leakage Current versus Output Voltage

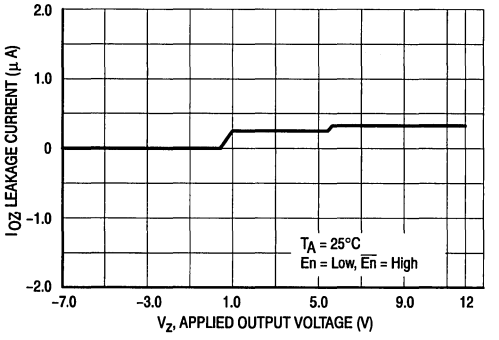


Figure 14. Output Leakage Current versus Temperature

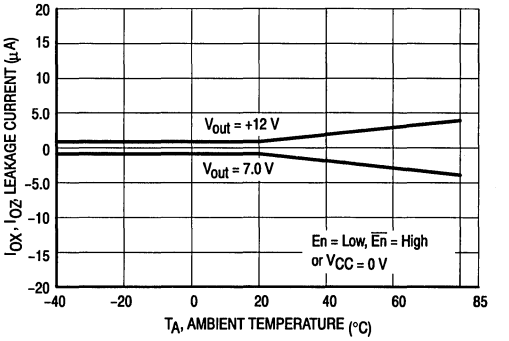


Figure 15. Input Current versus Input Voltage

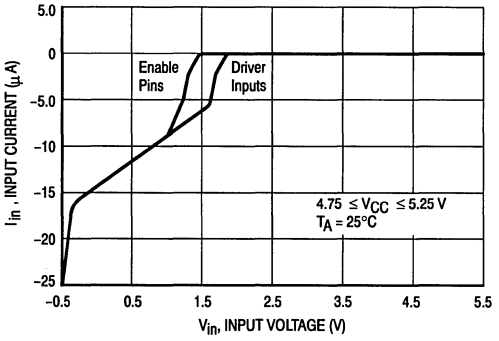
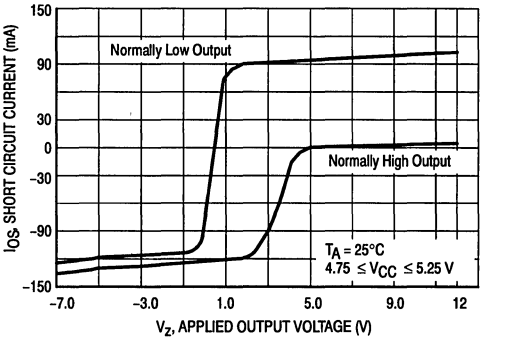


Figure 16. Short Circuit Current versus Common Mode Voltage



7

APPLICATIONS INFORMATION

Description

The MC75172B and MC75174B are differential line drivers designed to comply with EIA-485 Standard (April 1983) for use in balanced digital multipoint systems containing multiple drivers. The drivers also comply with EIA-422-A and CCITT Recommendations V.11 and X.27. The drivers meet the EIA-485 requirement for protection from damage in the event that two or more drivers attempt to transmit data simultaneously on the same cable. Data rates in excess of 10 MBPS are possible, depending on the cable length and cable characteristics. A single power supply, +5.0 V, ±5%, is required at a nominal current of 60 mA, plus load currents.

Outputs

Each output (when active) will be a low or a high voltage, which depends on the input state and the load current (see Table 1, 2 and Figures 7 to 10). The graphs apply to each driver, regardless of how many other drivers within the package are supplying load current.

Table 1. MC75172B Truth Table

Data Input	Enables		Outputs	
	EN	$\overline{EN}$	Y	Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

Table 2. MC75174B Truth Table

Data Input	Enable	Outputs	
		Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z

H = Logic high, L = Logic low, X = Irrelevant, Z = High impedance

The two outputs of a driver are always complementary. A "high" output can only source current out, while a "low" output can only sink current (except for short circuit current — see Figure 16).

The outputs will be in the high impedance mode when:

a) the Enable inputs are set according to Table 1 or 2;

b) V_{CC} is less than 1.5 V;

c) the junction temperature exceeds the trip point of the thermal shutdown circuit (see below). When in this condition, the output's source and sink capability are shut off, and only leakage currents will flow (see Figures 13, 14). Disabled outputs may be taken to any voltage between –7.0 V and +12 V without damage.

The drivers are protected from short circuits by two methods:

a) Current limiting is provided at each output, in both the source and sink direction, for shorts to any voltage within the range of +12 V to –7.0 V, with respect to circuit ground (see Figure 16). The short circuit current will flow until the fault is removed, or until the thermal shutdown circuit activates (see below). The current limiting circuit has a negative temperature coefficient and requires no resetting upon removal of the fault condition.

b) A thermal shutdown circuit disables the outputs when the junction temperature reaches +150°C, ± 20°C. The thermal shutdown circuit has a hysteresis of ≈ 12°C to prevent oscillations. When this circuit activates, the output stage of each driver is put into the high impedance mode, thereby shutting off the output currents. The remainder of the internal circuitry remains biased. The outputs will become active once again as the IC cools down.

Driver Inputs

The driver inputs determine the state of the outputs in accordance with Tables 1 and 2. The driver inputs have a nominal threshold of 1.2 V, and their voltage must be kept within the range of 0 V to V_{CC} for proper operation. If the voltage is taken more than 0.5 V below ground, excessive currents will flow, and proper operation of the drivers will be affected. An open pin is equivalent to a logic high, but good design practices dictate that inputs should never be left open. The characteristics of the driver inputs are shown in Figure 15. This graph is not affected by the state of the Enable pins.

Enable Logic

Each driver's outputs are active when the Enable inputs (Pins 4 and 12) are true according to Tables 1 and 2.

The Enable inputs have a nominal threshold of 1.2 V and their voltage must be kept within the range of 0 V to V_{CC} for proper operation. If the voltage is taken more than 0.5 V below ground, excessive currents will flow, and proper operation of the drivers will be affected. An open pin is equivalent to a logic high, but good design practices dictate that inputs should never be left open. The Enable input characteristics are shown in Figure 15.

Operating Temperature Range

The minimum ambient operating temperature is listed as –40°C to meet EIA–485 specifications, and 0°C to meet EIA-422-A specifications. The higher V_{OD} required by EIA-422-A is the reason for the narrower temperature range.

The maximum ambient operating temperature (applicable to both EIA-485 and EIA-422-A) is listed as +85°C. However, a lower ambient may be required depending on system use (i.e. specifically how many drivers within a package are

used) and at what current levels they are operating. The maximum power which may be dissipated within the package is determined by:

$$PD_{max} = \frac{T_{Jmax} - T_A}{R\phi_{JA}}$$

where: $R_{\theta JA}$ = package thermal resistance (typ. 70°C/W for the DIP package, 85°C/W for SOIC package);
T_{Jmax} = max. operating junction temperature, and
T_A = ambient temperature.

Since the thermal shutdown feature has a trip point of +150°C, ± 20°C, T_{Jmax} is selected to be +130°C. The power dissipated within the package is calculated from:

PD = {[($V_{CC} - V_{OH}$) • I_{OH}] + V_{OL} • I_{OL})} each driver + (V_{CC} • I_{CC})

where: V_{CC} = the supply voltage;
V_{OH}, V_{OL} are measured or estimated from Figures 7 to 10;
I_{CC} = the quiescent power supply current (typ. 60 mA).

As indicated in the equation, the first term (in brackets) must be calculated and summed for each of the four drivers, while the last term is common to the entire package.

Example 1: T_A = +25°C, I_{OL} = I_{OH} = 55 mA for each driver, V_{CC} = 5.0 V, DIP package. How many drivers per package can be used?

Maximum allowable power dissipation is:

$$PD_{max} = \frac{130°C - 25°C}{70°C/W} = 1.5\ W$$

Since the power supply current of 60 mA dissipates 300 mW, that leaves 1.2 W (1.5 W – 0.3 W) for the drivers. From Figures 7 and 9, V_{OL} ≈1.75 V, and V_{OH} ≈3.85 V. The power dissipated in each driver is:

{(5.0 – 3.85) • 0.055} + (1.75 • 0.055) = 160 mW.

Since each driver dissipates 160 mW, the four drivers per package could be used in this application

Example 2: T_A = +85°C, I_{OL} = 27.8 mA, I_{OH} = 20 mA for each driver, V_{CC} = 5.0 V, SOIC package. How many drivers per package can be used?

Maximum allowable power dissipation is:

$$PD_{max} = \frac{130°C - 85°C}{85°C/W} = 0.53\ W$$

Since the power supply current of 60 mA dissipates 300 mW, that leaves 230 mW (530 mW – 300 mW) for the drivers. From Figures 8 and 10 (adjusted for V_{CC} = 5.0 V), V_{OL} ≈1.38 V, and V_{OH} ≈4.27 V. The power dissipated in each driver is:

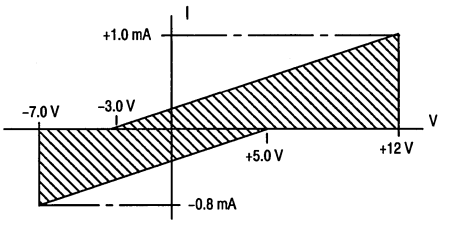
{(5.0 – 4.27) • 0.020} + (1.38 • 0.0278) = 53 mW

Since each driver dissipates 53 mW, the use of all four drivers in a package would be marginal. Options include reducing the load current, reducing the ambient temperature, and/or providing a heat sink.

System Requirements

EIA–485 requires each driver to be capable of transmitting data differentially to at least 32 unit loads, plus an equivalent DC termination resistance of 60Ω, over a common mode voltage of –7.0 to +12 V. A unit load (U.L.), as defined by EIA–485, is shown in Figure 17.

Figure 17. Unit Load Definition



Reprinted from EIA–485, Electronic Industries Association, Washington,DC.

A load current within the shaded regions represents an impedance of less than one U.L., while a load current of a magnitude outside the shaded area is greater than one U.L. A system's total load is the sum of the unit load equivalents of each receiver's input current, and each disabled driver's output leakage current. The 60Ω termination resistance mentioned above allows for two 120Ω terminating resistors.

Using the EIA-485 requirements (worst case limits), and the graphs of Figures 7 and 9, it can be determined that the maximum current an MC75172B or (MC75174B) driver will source or sink is ≈65 mA.

System Example

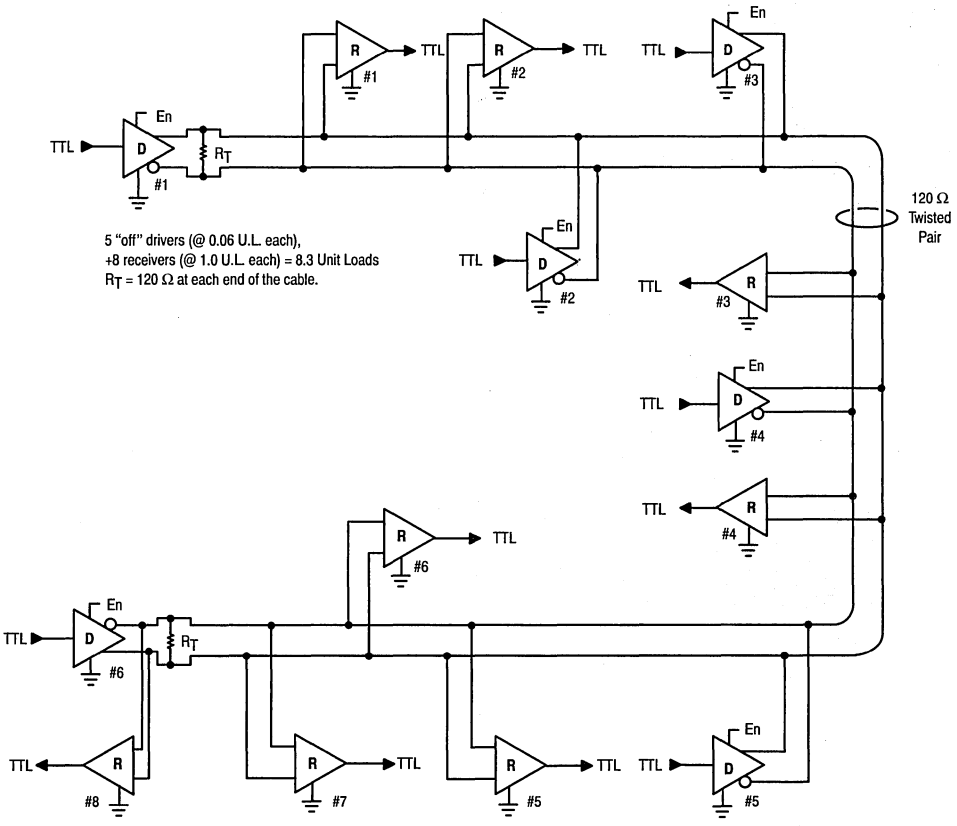
An example of a typical EIA-485 system is shown in Figure 18. In this example, it is assumed each receiver's input characteristics correspond to 1.0 U.L. as defined in Figure 17. Each "off" driver, with a maximum leakage of ±50 µA over the common mode range, presents a load of ≈0.06 U.L. The total load for the active driver is therefore 8.3 unit loads, plus the parallel combination of the two terminating resistors (60Ω). It is up to the system software to control the driver Enable pins to ensure that only one driver is active at any time.

Termination Resistors

Transmission line theory states that, in order to preserve the shape and integrity of a waveform traveling along a cable, the cable must be terminated in an impedance equal to its characteristic impedance. In a system such as that depicted in Figure 18, in which data can travel in both directions, both physical ends of the cable must be terminated. Stubs, leading to each receiver and driver, should be as short as possible.

Leaving off the terminations will generally result in reflections which can have amplitudes of several volts above V_{CC} or below ground. These overshoots and undershoots can disrupt the driver and/or receiver operation, create false data, and in some cases damage components on the bus.

Figure 18. Typical EIA-485 System



NOTES:
1) Terminating resistors R_T must be located at the physical ends of the cable.
2) Stubs should be as short as possible.
3) Circuit ground of all drivers and receivers must be connected via a dedicated wire within the cable. Do not rely on chassis ground or power line ground.

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Comparing System Requirements

	Symbol	EIA-485	EIA-422-A	V.11 and X.27
GENERATOR (Driver)				
Output Impedance (Note 1)	Z_{out}	Not Specified	< 100 Ω	50 to 100 Ω
Open Circuit Voltage Differential Single-Ended	 V_{OCD} V_{OCS}	 1.5 to 6.0 V < 6.0 V	 ≤ 6.0 V ≤ 6.0 V	 ≤ 6.0 V, w/3.9 kΩ, Load ≤ 6.0 V, w/3.9 kΩ, Load
Loaded Differential Voltage	V_{OD}	1.5 to 5.0 V, w/54 Ω load	≥ 2.0 V or ≥ 0.5 V_{OCD}, w/100 Ω load	≥ 2.0 V or ≥ 0.5 V_{OCD}, w/100 Ω load
Differential Voltage Balance	ΔV_{OD}	<200 mV	≤ 400 mV	< 400 mV
Output Common Mode Range	V_{CM}	–7.0 to +12 V	Not Specified	Not Specified
Offset Voltage	V_{OS}	–1.0 < V_{OS} < 3.0 V	≤ 3.0 V	≤ 3.0 V
Offset Voltage Balance	ΔV_{OS}	< 200 mV	≤ 400 mV	< 400 mV
Short Circuit Current	I_{OS}	≤ 250 mA from –7.0 to +12 V	≤ 150 mA to ground	≤ 150 mA to ground
Leakage Current (V_{CC} = 0)	I_{OLK}	Not Specified	≤ 100 µA to –0.25 V thru +6.0 V	≤ 100 µA to ± 0.25 V
Output Rise/Fall Time (Note 2)	t_r, t_f	≤ 0.3 T_B, w/54 Ω//1150 pF load	≤ 0.1 T_B or ≤ 20 ns, w/100 Ω load	≤ 0.1 T_B or ≤ 20 ns, w/100 Ω load
RECEIVER				
Input Sensitivity	V_{th}	± 200 mV	± 200 mV	± 300 mV
Input Bias Voltage	V_{bias}	≤ 3.0 V	≤ 3.0 V	≤ 3.0 V
Input Common Mode Range	V_{cm}	–7.0 to +12 V	–7.0 to +7.0 V	–7.0 to +7.0 V
Dynamic Input Impedance	R_{in}	Spec number of U.L.	≥ 4 kΩ	≥ 4 kΩ

NOTES:
1) Compliance with V.11 and X.27 (Blue book) output impedance requires external resistors in series with the outputs of the MC75172B and MC75174B.
2) T_B = Bit time.

Additional Information

Copies of the EIA Recommendations (EIA-485 and EIA-422-A) can be obtained from the Electronics Industries Association, Washington, D.C. (202-457-4966). Copies of the CCITT Recommendations (V.11 and X.27) can be obtained from the United States Department of Commerce, Springfield, VA (703-487-4600).

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

SN75173
SN75175

QUAD EIA-485 LINE RECEIVERS

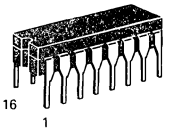
The Motorola SN75173/175 are monolithic quad differential line receivers with three-state outputs. They are designed specifically to meet the requirements of EIA-485, EIA-422A/23A Standards and CCITT recommendations.

The devices are optimized for balanced multipoint bus transmission at rates up to 10 megabits per second. They also feature high input impedance, input hysteresis for increased noise immunity, and input sensitivity of ±200 millivolts over a common mode input voltage range of −12 volts to 12 volts. The SN75173/175 are designed for optimum performance when used with the SN75172 or SN75174 quad differential line drivers.

- Meets EIA Standards EIA-422A and EIA-423A, EIA-485
- Meets CCITT Recommendations V.10, V.11, X.26, and X.27
- Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments
- 3-State Outputs
- Common-Mode Input Voltage Range . . . −12 V to 12 V
- Input Sensitivity . . . ±200 mV
- Input Hysteresis . . . 50 mV Typ
- High Input Impedance . . . 1 EIA-485 Unit Load
- Operates from Single 5.0 V Supply
- Low Power Requirements
- Plug-In Replacement for MC3486 (SN75175) AM26LS32 (SN75173)

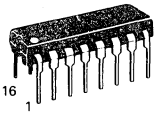
QUAD EIA-485 LINE RECEIVERS WITH THREE-STATE OUTPUTS

SILICON MONOLITHIC INTEGRATED CIRCUITS



J SUFFIX
CERAMIC PACKAGE
CASE 620

D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO-16)

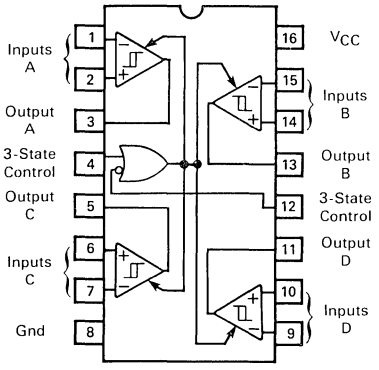


N SUFFIX
PLASTIC PACKAGE
CASE 648

7

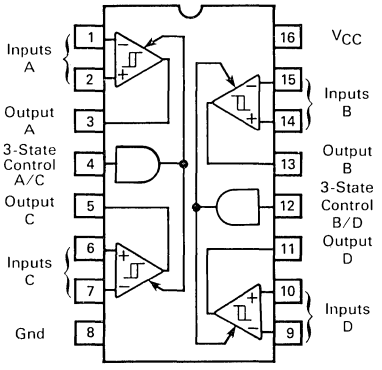
PIN CONNECTIONS

SN75173



ORDERING INFORMATION		
Device	Temperature	Package
SN75173J	0 to +70°C	Ceramic DIP
SN75173N	0 to +70°C	Plastic DIP

SN75175



ORDERING INFORMATION		
Device	Temperature	Package
SN75175J	0 to +70°C	Ceramic DIP
SN75175N	0 to +70°C	Plastic DIP

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	7.0	Vdc
Input Common Mode Voltage	V_{ICM}	±25	Vdc
Input Differential Voltage	V_{ID}	±25	Vdc
Three-State Control Input Voltage	V_I	7.0	Vdc
Output Sink Current	I_O	50	mA
Storage Temperature	T_{stg}	-65 to +150	°C
Operating Junction Temperature — Ceramic Package — Plastic Package	T_J	+175 +150	°C

RECOMMENDED OPERATING CONDITIONS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	4.75 to 5.25	Vdc
Operating Ambient Temperature	T_A	0 to +70	°C
Input Common Mode Voltage Range	V_{ICM}	-12 to +12	Vdc
Input Differential Voltage Range	V_{IDR}	-12 to +12	Vdc

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, minimum and maximum limits apply over recommended temperature and power supply voltage ranges. Typical values are for T_A =25°C, V_{CC} = 5.0 V and V_{ICM} = 0 V) (Note 1)

Characteristic	Symbol	Min	Typ	Max	Unit
Differential Input Threshold Voltage (Note 2)	$V_{TH(D)}$				V
(-12 V ≤ V_{ICM} ≤ 12 V, V_{IH} = 2.0 V)					
(I_O = -0.4 mA, V_{OH} ≥ 2.7 V)		—	—	0.2	
(I_O = 16 mA, V_{OL} ≤ 0.5 V)		—	—	-0.2	
Input Hysteresis	$V_{T+} - V_{T-}$	—	50	—	mV
Input Line Current (Differential Inputs) (Unmeasured Input at 0 V — Note 3)	I_I				mA
(V_I = +12 V)		—	—	1.0	
(V_I = -7.0 V)		—	—	-0.8	
Input Resistance (Note 4)	r_i	1 Unit Load	—	—	
Input Balance and Output Level (Note 3)					V
(-12 V ≤ V_{ICM} ≤ 12 V, V_{IH} = 2.0 V)					
(I_O = -0.4 mA, V_{ID} = 0.2 V)	V_{OH}	2.7	—	—	
(I_O = 8.0 mA, V_{ID} = -0.2 V)	V_{OL}	—	—	0.45	
(I_O = 16 mA, V_{ID} = -0.2 V)	V_{OL}	—	—	0.5	
Input Voltage — High Logic State (Three-State Control)	V_{IH}	2.0	—	—	V
Input Voltage — Low Logic State (Three-State Control)	V_{IL}	—	—	0.8	V
Input Current — High Logic State (Three-State Control)	I_{IH}				μA
(V_{IH} = 2.7 V)		—	—	20	
(V_{IH} = 5.5 V)		—	—	100	
Input Current — Low Logic State (Three-State Control) (V_{IL} = 0.4 V)	I_{IL}	—	—	-100	μA
Input Clamp Diode Voltage (Three-State Control) (I_{IK} = -18 mA)	V_{IK}	—	—	-1.5	V
Output Third State Leakage Current	I_{OZ}				μA
($V_{I(D)}$ = 3.0 V, V_{IL} = 0.8 V, V_O = 0.4 V)		—	—	-20	
($V_{I(D)}$ = -3.0 V, V_{IL} = 0.8 V, V_O = 2.4 V)		—	—	20	
Output Short-Circuit Current (Note 5) ($V_{I(D)}$ = 3.0 V, V_{IH} = 2.0 V, V_O = 0 V)	I_{OS}	-15	—	-85	mA
Power Supply Current (V_{IL} = 0 V) (All Inputs Grounded)	I_{CC}	—	—	70	mA

NOTES:
1. All currents into device pins are shown as positive, out of device pins are negative. All voltages referenced to ground unless otherwise noted.
2. Differential input threshold voltage and guaranteed output levels are done simultaneously for worst case.
3. Refer to EIA-485 for exact conditions. Input balance and guaranteed output levels are done simultaneously for worst case.
4. Input resistance should be derived from input line current specifications and is shown for reference only. See EIA-485 and input line current specifications for more specific input resistance information.
5. Only one output at a time should be shorted.

SWITCHING CHARACTERISTICS (Unless otherwise noted, V_{CC} = 5.0 V and T_A = 25°C)

Characteristic	Symbol	SN75173			SN75175			Unit
		Min	Typ	Max	Min	Typ	Max	
Propagation Delay Time — Differential Inputs to Output								ns
(Output High to Low)	$t_{PHL(D)}$	—	25	35	—	25	35	
(Output Low to High)	$t_{PLH(D)}$	—	25	35	—	25	35	
Propagation Delay Time — Three-State Control to Output								ns
(Output Low to Third State)	t_{PLZ}	—	20	40	—	16	35	
(Output High to Third State)	t_{PHZ}	—	20	30	—	19	35	
(Output Third State to High)	t_{PZH}	—	16	22	—	11	30	
(Output Third State to Low)	t_{PZL}	—	16	25	—	11	30	

SN75173

FUNCTION TABLE (EACH RECEIVER)

Differential Inputs	3-State Control		Output Y
	4	12	
$V_{ID} \geq 0.2$ V	H	X	H
	X	L	H
-0.2 V $< V_{ID} < 0.2$ V	H	X	?
	X	L	?
$V_{ID} \leq -0.2$ V	H	X	L
	X	L	L
X	L	H	Z

SN75175

FUNCTION TABLE (EACH RECEIVER)

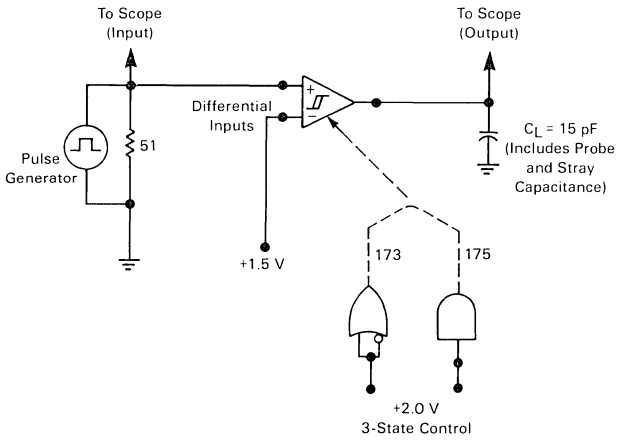
Differential Inputs	3-State Control	Output Y
$V_{ID} \geq 0.2$ V	H	H
-0.2 V $< V_{ID} < 0.2$ V	H	?
$V_{ID} \leq -0.2$ V	H	L
X	L	Z

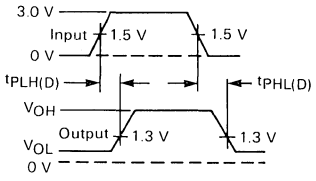
H = high level
L = low level
X = irrelevant
? = indeterminate
Z = high-impedance (off)

7

SWITCHING TEST CIRCUIT AND WAVEFORMS

FIGURE 1 — PROPAGATION DELAY, DIFFERENTIAL INPUT TO OUTPUT

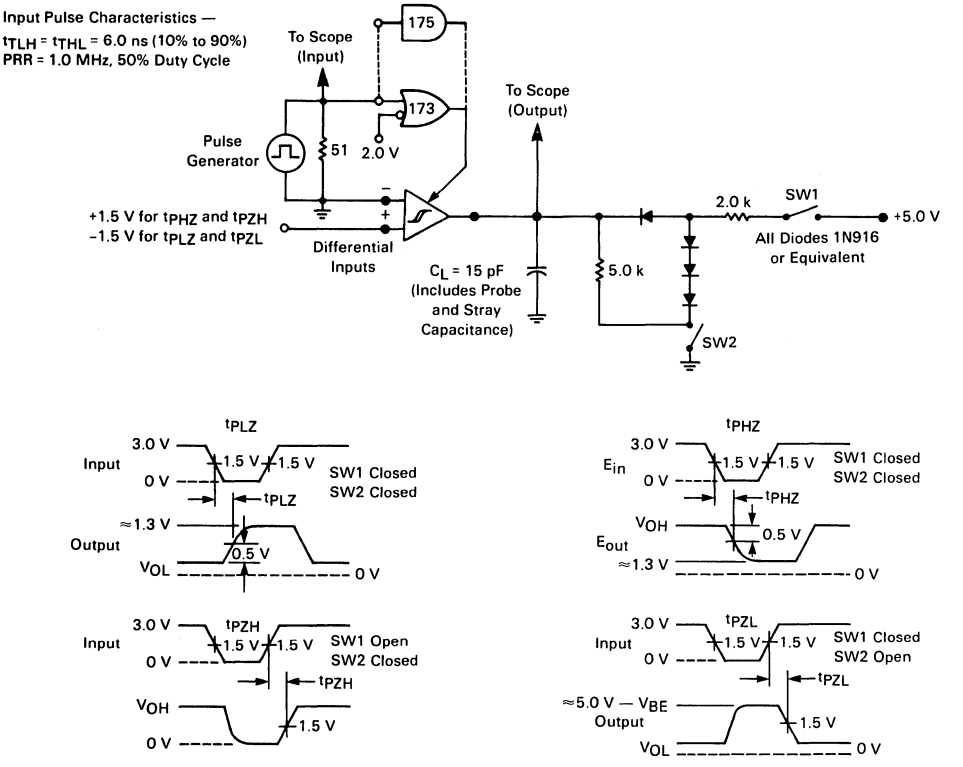




Input Pulse Characteristics —
$t_{TLH} = t_{THL}$ = 6.0 ns (10% to 90%)
PRR = 1.0 MHz, 50% Duty Cycle

SWITCHING TEST CIRCUIT AND WAVEFORMS (continued)

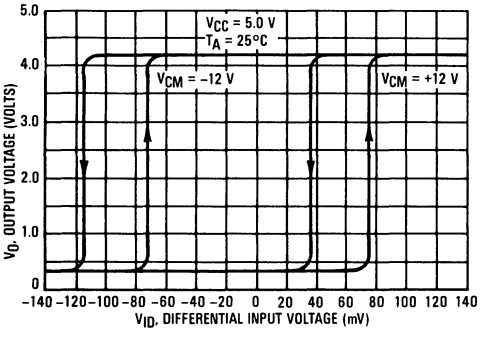
FIGURE 2 — PROPAGATION DELAY, THREE-STATE CONTROL INPUT TO OUTPUT



TYPICAL CHARACTERISTICS

(Both Device Types, Unless Otherwise Noted)

FIGURE 3 — OUTPUT VOLTAGE versus DIFFERENTIAL INPUT VOLTAGE



TYPICAL CHARACTERISTICS (continued)

FIGURE 4 — OUTPUT VOLTAGE versus 3-STATE CONTROL VOLTAGE

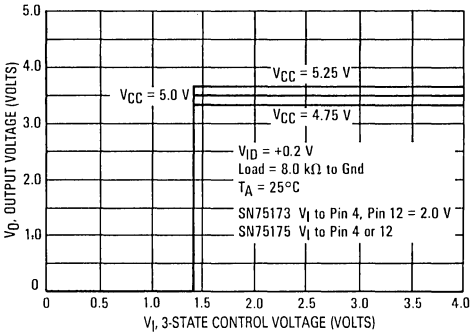


FIGURE 5 — OUTPUT VOLTAGE versus (INVERTED) 3-STATE CONTROL VOLTAGE — SN75173

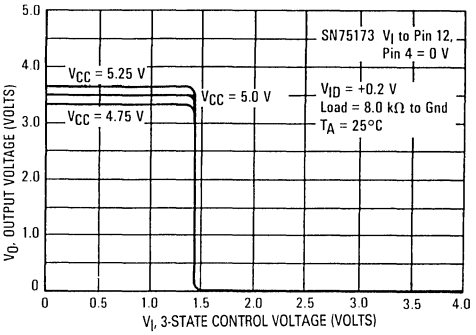


FIGURE 6 — HIGH LEVEL OUTPUT VOLTAGE versus OUTPUT CURRENT

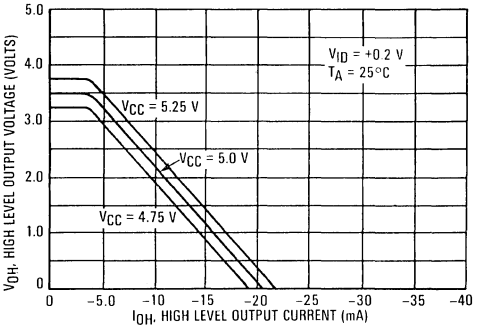


FIGURE 7 — LOW LEVEL OUTPUT VOLTAGE versus OUTPUT CURRENT

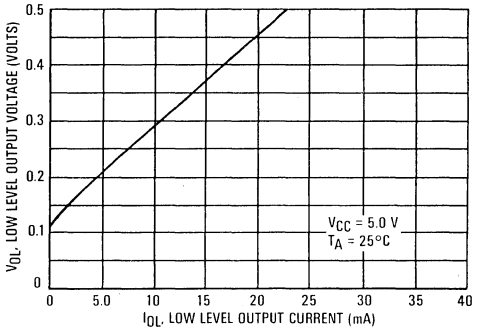


FIGURE 8 — HIGH LEVEL OUTPUT VOLTAGE versus TEMPERATURE

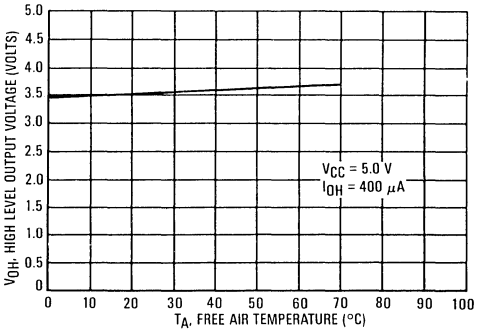
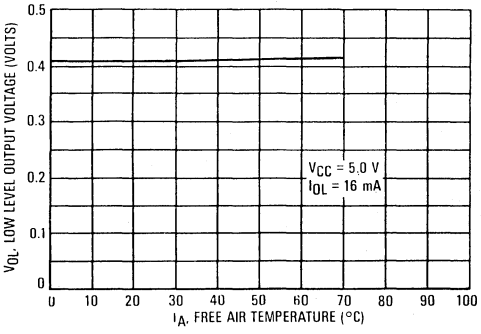


FIGURE 9 — LOW LEVEL OUTPUT VOLTAGE versus TEMPERATURE



7

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

ULN2068B

QUAD 1.5 A SINKING HIGH CURRENT SWITCH

The ULN2068B is a high-voltage, high-current quad Darlington switch array designed for high current loads, both resistive and reactive, up to 300 watts.

It is intended for interfacing between low level (TTL, DTL, LS and 5.0 V CMOS) logic families and peripheral loads such as relays, solenoids, dc and stepping motors, multiplexer LED and incandescent displays, heaters, or other high voltage, high current loads.

The Motorola ULN2068B is specified with minimum guaranteed breakdown of 50 V and is 100% tested for safe area using an inductive load. It includes integral transient suppression diodes. Use of a predriver stage reduces input current while still allowing the device to switch 1.5 Amps.

It is supplied in an improved 16-Pin plastic DIP package with heat sink contact tabs (Pins 4, 5 and 12, 13). A copper alloy lead frame allows maximum power dissipation using standard cooling techniques. The use of the contact tab lead frame facilitates attachment of a DIP heat sink while permitting the use of standard layout and mounting practices.

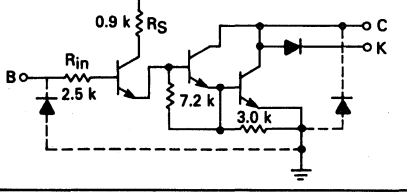
- TTL, DTL, LS, CMOS Compatible Inputs
- 1.5 Amp Maximum Output Current
- Low Input Current
- Internal Freewheeling Clamp Diodes
- 100% Inductive Load Tested
- Heat Tab Copper Alloy Lead Frame for Increased Dissipation

MAXIMUM RATINGS (T_A = 25°C and ratings apply to any one device in the package unless otherwise noted)

Rating	Symbol	Value	Unit
Output Voltage	V_O	50	V
Input Voltage (Note 1)	V_I	15	V
Supply Voltage	V_S	10	V
Collector Current (Note 2)	I_C	1.75	A
Input Current (Note 3)	I_I	25	mA
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C
Junction Temperature	T_J	150	°C

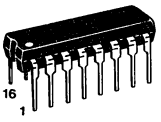
Notes:
1. Input voltage referenced to ground.
2. Allowable output conditions shown in Figures 11 and 12.
3. May be limited by max input voltage.

V_S PARTIAL SCHEMATIC



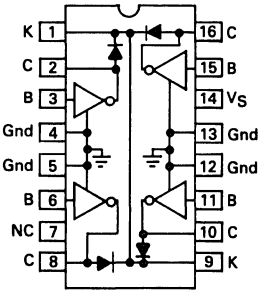
QUAD 1.5 A DARLINGTON SWITCH

SILICON MONOLITHIC INTEGRATED CIRCUIT



B SUFFIX
PLASTIC PACKAGE
CASE 648C

PIN CONNECTIONS



ORDERING INFORMATION*

Device	Temperature Range	Package
ULN2068B	0°C to +70°C	Plastic DIP

*Other options of this ULN2060/2070 series are available for volume applications. Contact your local Motorola Sales Representative.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Characteristic	Fig.	Symbol	Min	Typ	Max	Unit
Output Leakage Current (V_{CE} = 50 V) (V_{CE} = 50 V, T_A = 70°C)	1	I_{CEX}	— —	— —	100 500	µA
Collector-Emitter Saturation Voltage (I_C = 500 mA (I_C = 750 mA (I_C = 1.0 A (I_C = 1.25 A V_{in} = 2.4 V)	2	$V_{CE(sat)}$	— — — —	— — — —	1.13 1.25 1.40 1.60	V
Input Current — On Condition (V_I = 2.4 V) (V_I = 3.75 V)	4	$I_{I(on)}$	— —	— —	0.25 1.0	mA
Input Voltage — On Condition (V_{CE} = 2.0 V, I_C = 1.5 A)	5	$V_{I(on)}$	—	—	2.4	V
Inductive Load Test (V_S = 5.5 V, V_{CC} = 24.5 V, t_{PW} = 4.0 ms)	3	ΔV_{out}	—	—	100	mV
Supply Current (I_C = 500 mA, V_{in} = 2.4 V, V_S = 5.5 V)	8	I_S	—	—	6.0	mA
Turn-On Delay Time (50% E_I to 50% E_O)	—	t_{PHL}	—	—	1.0	µs
Turn-Off Delay Time (50% E_I to 50% E_O)	—	t_{PLH}	—	—	4.0	µs
Clamp Diode Leakage Current (V_R = 50 V) (V_R = 50 V, T_A = 70°C)	6	I_R	— —	— —	50 100	µA
Clamp Diode Forward Voltage (I_F = 1.0 A) (I_F = 1.5 A)	7	V_F	— —	— —	1.75 2.0	V

7

TEST FIGURES

FIGURE 1

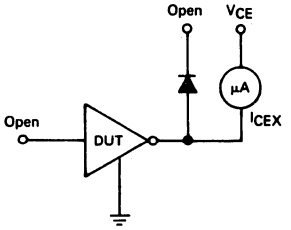


FIGURE 2

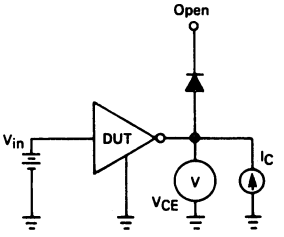


FIGURE 3

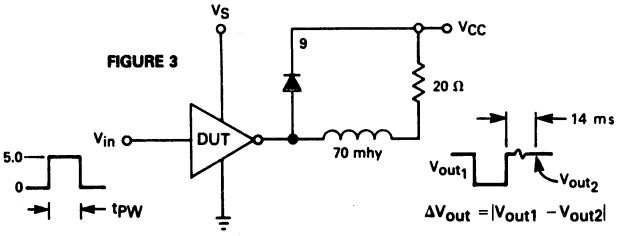
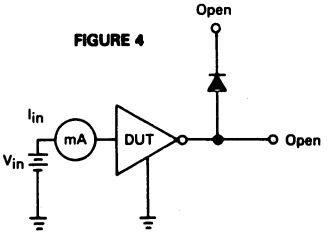


FIGURE 4



TEST FIGURES (CONTINUED)

FIGURE 5

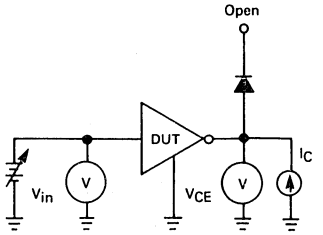


FIGURE 6

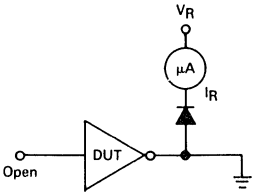


FIGURE 7

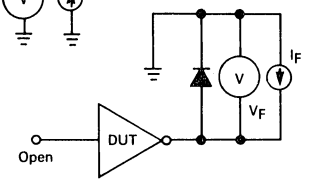
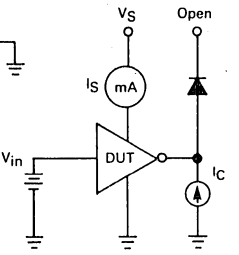


FIGURE 8



TYPICAL CHARACTERISTIC CURVES — T_A = 25°C

FIGURE 9 — INPUT CURRENT versus INPUT VOLTAGE

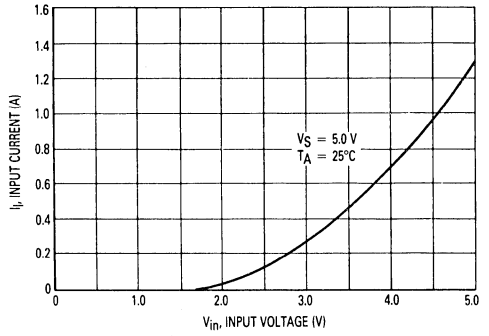


FIGURE 10 — COLLECTOR CURRENT versus INPUT CURRENT

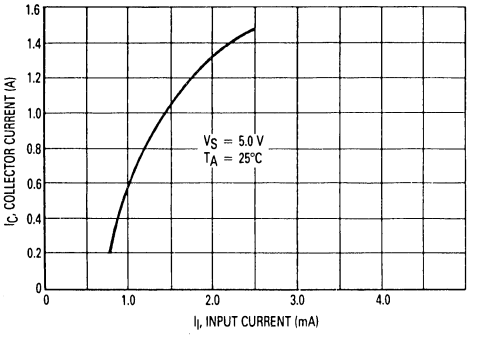


FIGURE 11 — T_A = 70°C w/o HEAT SINK

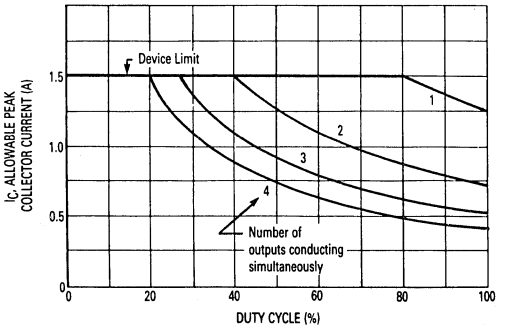


FIGURE 12 — T_A = 70°C w/STAVER V-8 HEAT SINK (37.5 °C/W)

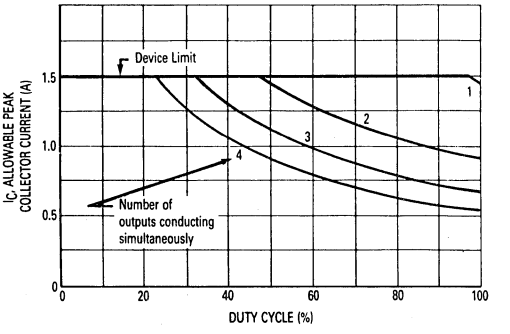


FIGURE 13 — T_A = 70°C w/STAVER V-7 HEAT SINK (27.5 °C/W)

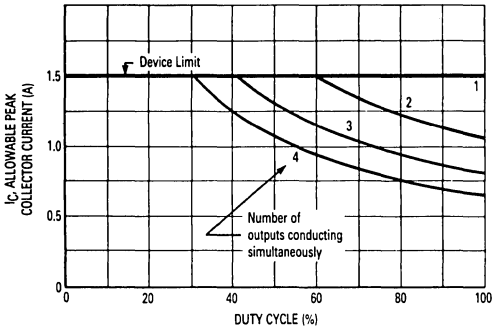


FIGURE 14 — T_A = 50°C w/o HEAT SINK

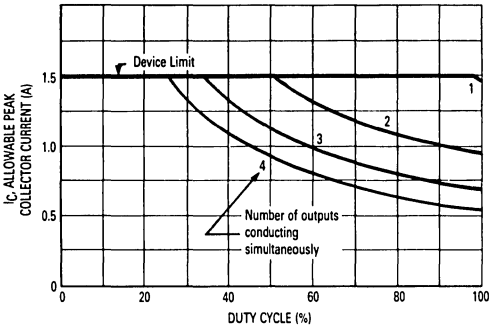


FIGURE 15 — T_A = 50°C w/STAVER V-8 HEAT SINK (37.5 °C/W)

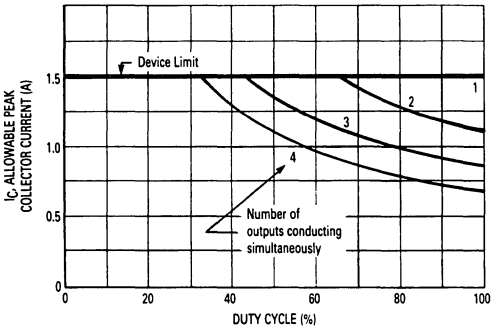
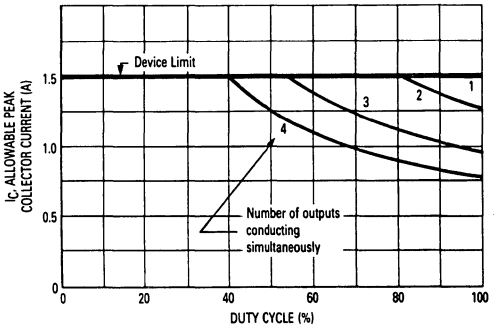


FIGURE 16 — T_A = 50°C w/ STAVER V-7 HEAT SINK (27.5 °C/W)



7

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

ULN2801
ULN2802
ULN2803
ULN2804

OCTAL PERIPHERAL DRIVER ARRAYS

SILICON MONOLITHIC INTEGRATED CIRCUITS

OCTAL HIGH VOLTAGE, HIGH CURRENT DARLINGTON TRANSISTOR ARRAYS

The eight NPN Darlington connected transistors in this family of arrays are ideally suited for interfacing between low logic level digital circuitry (such as TTL, CMOS or PMOS/NMOS) and the higher current/voltage requirements of lamps, relays, printer hammers or other similar loads for a broad range of computer, industrial, and consumer applications. All devices feature open-collector outputs and free wheeling clamp diodes for transient suppression.

The ULN2801 is a general purpose device for use with CMOS, PMOS or TTL logic. The ULN2802 contains a zener diode and resistor in series with the input to limit input currents and assure compatibility with 14 to 25 volt PMOS logic. The ULN2803 is designed to be compatible with standard TTL families while the ULN2804 is optimized for 6 to 15 volt high level CMOS or PMOS.

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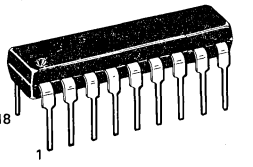


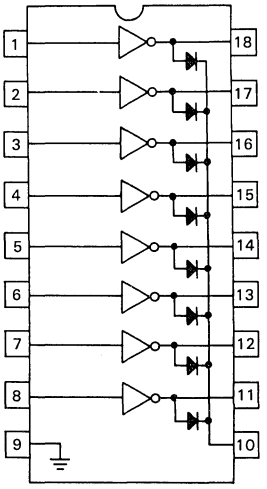
A SUFFIX
PLASTIC PACKAGE
CASE 707

MAXIMUM RATINGS (T_A = 25°C and rating apply to any one device in the package unless otherwise noted.)

Rating	Symbol	Value	Unit
Output Voltage	V_O	50	V
Input Voltage (Except ULN2801)	V_I	30	V
Collector Current — Continuous	I_C	500	mA
Base Current — Continuous	I_B	25	mA
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C
Junction Temperature	T_J	125	°C

$R_{\theta JA}$ = 55°C/W
Do not exceed maximum current limit per driver.

PIN CONNECTIONS



ORDERING INFORMATION

Device	Characteristics		
	Input Compatibility	V_{CE}(Max)/I_C(Max)	T_A
ULN2801A	General Purpose CMOS, PMOS	50 V/500 mA	0 to +70°C
ULN2802A	14–25 Volt PMOS		
ULN2803A	TTL, 5.0 V CMOS		
ULN2804A	6–15 V CMOS, PMOS		

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Fig.	Symbol	Min	Typ	Max	Unit
Output Leakage Current		1	I_{CEX}				μA
(V_O = 50 V, T_A = +70°C)	All Types			—	—	100	
(V_O = 50 V, T_A = +25°C)	All Types			—	—	50	
(V_O = 50 V, T_A = +70°C, V_I = 6.0 V)	ULN2802			—	—	500	
(V_O = 50 V, T_A = +70°C, V_I = 1.0 V)	ULN2804			—	—	500	
Collector-Emitter Saturation Voltage		2	$V_{CE(sat)}$				V
(I_C = 350 mA, I_B = 500 μA)	All Types			—	1.1	1.6	
(I_C = 200 mA, I_B = 350 μA)	All Types			—	0.95	1.3	
(I_C = 100 mA, I_B = 250 μA)	All Types			—	0.85	1.1	
Input Current — On Condition		4	$I_{I(on)}$				mA
(V_I = 17 V)	ULN2802			—	0.82	1.25	
(V_I = 3.85 V)	ULN2803			—	0.93	1.35	
(V_I = 5.0 V)	ULN2804			—	0.35	0.5	
(V_I = 12 V)	ULN2804			—	1.0	1.45	
Input Voltage — On Condition		5	$V_{I(on)}$				V
(V_{CE} = 2.0 V, I_C = 300 mA)	ULN2802			—	—	13	
(V_{CE} = 2.0 V, I_C = 200 mA)	ULN2803			—	—	2.4	
(V_{CE} = 2.0 V, I_C = 250 mA)	ULN2803			—	—	2.7	
(V_{CE} = 2.0 V, I_C = 300 mA)	ULN2803			—	—	3.0	
(V_{CE} = 2.0 V, I_C = 125 mA)	ULN2804			—	—	5.0	
(V_{CE} = 2.0 V, I_C = 200 mA)	ULN2804			—	—	6.0	
(V_{CE} = 2.0 V, I_C = 275 mA)	ULN2804			—	—	7.0	
(V_{CE} = 2.0 V, I_C = 350 mA)	ULN2804			—	—	8.0	
Input Current — Off Condition (I_C = 500 μA, T_A = +70°C)	All Types	3	$I_{I(off)}$	50	100	—	μA
DC Current Gain (V_{CE} = 2.0 V, I_C = 350 mA)	ULN2801	2	h_{FE}	1000	—	—	—
Input Capacitance			C_I	—	15	25	pF
Turn-On Delay Time (50% E_I to 50% E_O)			t_{on}	—	0.25	1.0	μs
Turn-Off Delay Time (50% E_I to 50% E_O)			t_{off}	—	0.25	1.0	μs
Clamp Diode Leakage Current (V_R = 50 V)	T_A = +25°C T_A = +70°C	6	I_R	—	—	50 100	μA
Clamp Diode Forward Voltage (I_F = 350 mA)		7	V_F	—	1.5	2.0	V

7

TEST FIGURES

(SEE FIGURE NUMBERS IN ELECTRICAL CHARACTERISTICS TABLES)

FIGURE 1

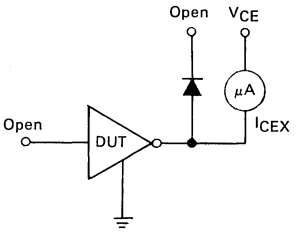


FIGURE 2

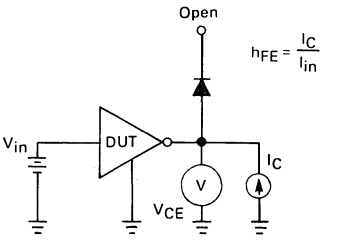


FIGURE 3

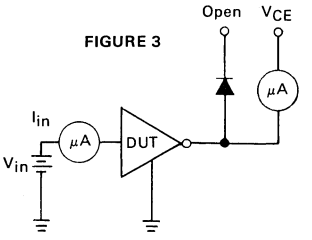


FIGURE 4

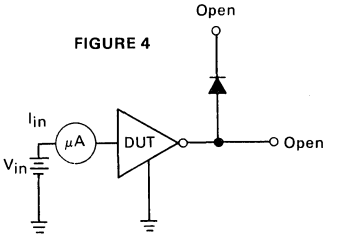


FIGURE 5

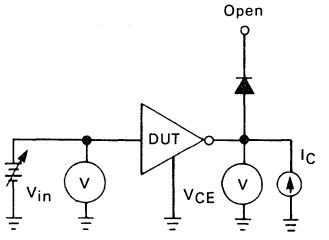


FIGURE 6

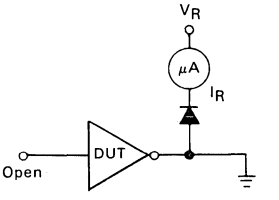
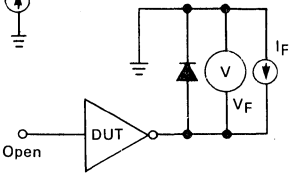


FIGURE 7



TYPICAL CHARACTERISTIC CURVES — T_A = 25°C
(unless otherwise noted)

OUTPUT CHARACTERISTICS

FIGURE 8 — OUTPUT CURRENT versus SATURATION VOLTAGE

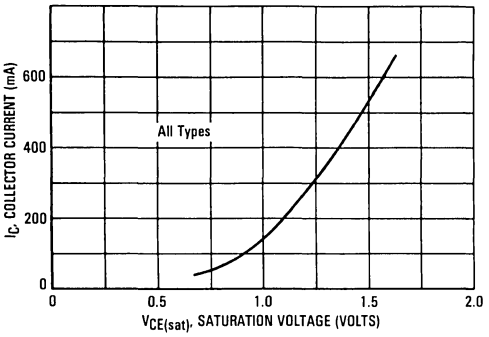
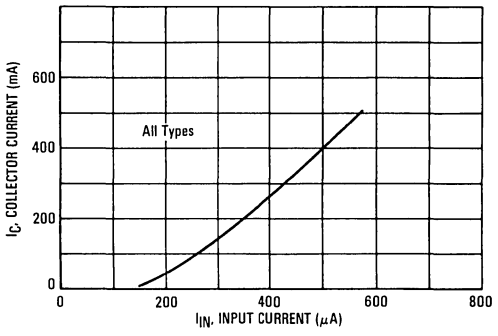


FIGURE 9 — OUTPUT CURRENT versus INPUT CURRENT



INPUT CHARACTERISTICS

FIGURE 10 — ULN2802 INPUT CURRENT versus INPUT VOLTAGE

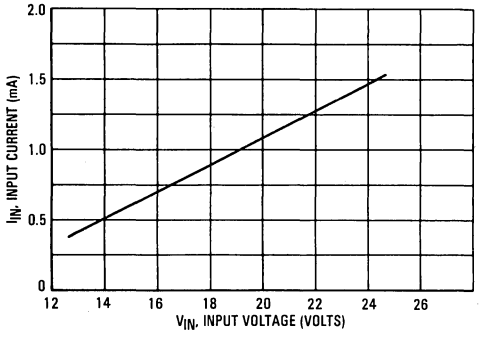


FIGURE 11 — ULN2803 INPUT CURRENT versus INPUT VOLTAGE

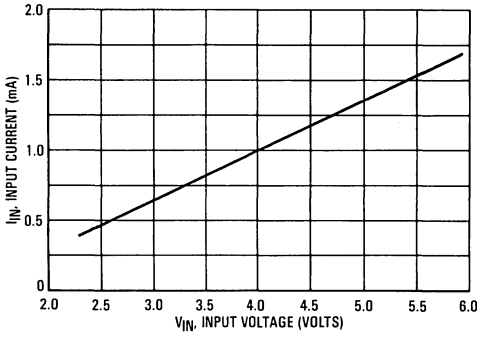
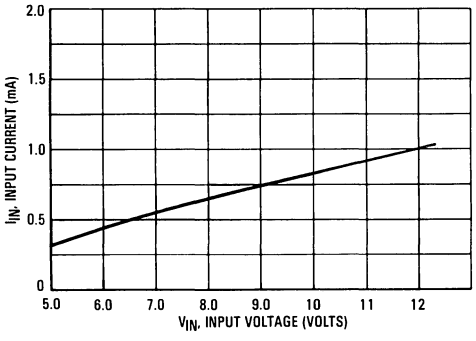
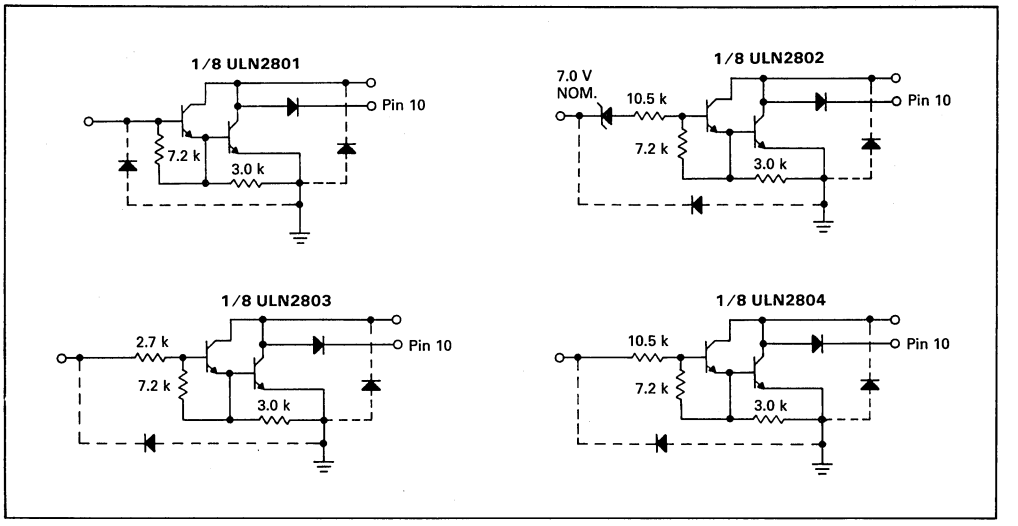


FIGURE 12 — ULN2804 INPUT CURRENT versus INPUT VOLTAGE



REPRESENTATIVE CIRCUIT SCHEMATICS



7

Communication Circuits

In Brief . . .

RF

Radio communication has greatly expanded its scope in the past several years. Once dominated by public safety radio, the 30 to 1000 MHz spectrum is now packed with personal and low cost business radio systems. The vast majority of this equipment uses FM or FSK modulation and is targeted at short range applications. From mobile phones and VHF marine radios to garage door openers and radio controlled toys, these new systems have become a part of our lifestyle. Motorola Linear has focused on this technology, adding a wide array of new products including complete receivers processed in our exclusive 3.0 GHz MOSAIC® 1.5 process. New surface mount packages for high density assembly are available for all of these products, as is a growing family of supporting applications notes and development kits.

Telephone & Voice/Data

Traditionally, an office environment has utilized two distinctly separate wired communications systems — Telecommunications and Data communications. Each had its individual hardware components complement, and each required its own independent transmission line system: twisted wire pairs for Telecom and relatively high priced coaxial cable for Datacom. But times have changed. Today, Telecom and Datacom coexist comfortably on inexpensive twisted wire pairs and use a significant number of components in common. This has led to the development and enhancement of PBX (Private Branch Exchanges) to the point where the long heralded "office of the future," with simultaneous voice and data communications capability at each station, is no longer of the future at all. The capability is here today!

Motorola Semiconductor serves a wide range of requirements for the voice/data marketplace. We offer both CMOS and Linear technologies, each to its best advantage, to upgrade the conventional analog voice systems and establish new capabilities in digital communications. Early products, such as the solid-state single-chip crosspoint switch; the more recent monolithic Subscriber Loop Interface Circuit (SLIC); a single-chip Codec/Filter (Mono-Circuit); the Universal Digital Loop Transceivers (UDLT); basic rate ISDN (Integrated Services Digital Network), and single-chip telephone circuits are just a few examples of Motorola leadership in the voice/data area.

RF Communications

Wideband (FM/FSK) IFs

Device	V_{CC}	I_{CC}	Sensitivity (Typ)	IF	Mute	RSSI	Max Data Rate	Notes	Suffix/ Case
MC13055	3–12 V	25 mA	20 μV	40 MHz	✓	✓	2.0 Mb	Wideband Data IF	P/648 D/751B
MC13155	3–6 V	10 mA	100 μV	70 MHz	—		12 Mb	Video Speed FM IF	D/751B

Wideband Single Conversion Receivers — VHF

Device	V_{CC}	I_{CC}	Sensitivity (Typ)	RF Input	IF	Mute	RSSI	Max Data Rate	Notes	Suffix/ Case
MC3356	3–9 V	25 mA	30 μV	200 MHz	10.7 MHz	✓	✓	500 kb	Includes front end mixer/L.O.	P/738 DW/751D
MC13156	2–7 V	3.0 mA	2.0 μV		21.4 MHz	—			CT-2 FM/Demodulator	DW/751E

Narrowband Single Conversion Receivers — VHF

Device	V_{CC}	I_{CC}	12 dB SINAD Sensitivity (Typ)	RF Input	IF	Mute	RSSI	Max Data Rate	Notes	Suffix/ Case
MC3357	4–8 V	5.0 mA	5.0 μV	45 MHz	455 kHz	✓	—	>4.8 kb	Ceramic Quad Detector/Resonator	P/648
MC3359	4–9 V	7.0 mA	2.0 μV						Scan output option	P/707 DW/751D
MC3361B	2–8 V	6.0 mA		60 MHz					Lowest cost receiver	P648 D/751B
MC3367	1–5 V	1.0 mA	1.0 μV	75 MHz			—	1.2 kb	1 Cell Operation	DW/751F
MC3371	2–8 V	6.0 mA		60 MHz			✓	>4.8 kb	RSSI	P/648 D/751B
MC3372									RSSI, Ceramic Quad Detector/Resonator	

Narrowband Dual Conversion Receivers — FM/FSK — VHF

Device	V_{CC}	I_{CC}	12 dB SINAD Sensitivity (Typ)	RF Input	IF1	IF2 (Limiter In)	Mute	RSSI	Data Rate	Notes	Suffix/ Case
MC3362	2.0 V to 7.0 V	3.0 mA	0.7 μV	180 MHz	10.7 MHz	455 kHz	—	✓	> 4.8 kb	Includes buffered VCO output	P/724 DW/751E
MC3363		4.0 mA	0.4 μV				✓			Includes RF amp/mute	DW/751F
MC3335			0.7 μV							Low cost version	DW/751D
MC13135		3.5 mA		200 MHz			—		> 50 kb	Voltage buffered RSSI	DW/751E
MC13136										High level IF resonator drive	

Transmitters — AM/FM/FSK

Device	V_{CC}	I_{CC}	P_{out}	Max RF Freq Out	Max Mod Freq	Notes	Suffix/ Case
MC2831A	3.0 V to 8.0 V	5.0 mA	–30 dBm	50 MHz	50 kHz	FM transmitter. Includes low battery checker, tone oscillator	P/648 D/751B
MC2833		10 mA	–30 dBm to +10 dBm	150 MHz		FM transmitter. Includes two frequency multiplier/amplifier transistors	
MC13175	2.0 V to 5.0 V	40 mA	8.0 dBm	500 MHz	5.0 MHz	AM/FM transmitter. Single frequency PLL $f_{out} = 8 \times f_{ref}$	D/751B
MC13176				1.0 GHz		$f_{out} = 32 \times f_{ref}$	

Balanced Modulator/Demodulator

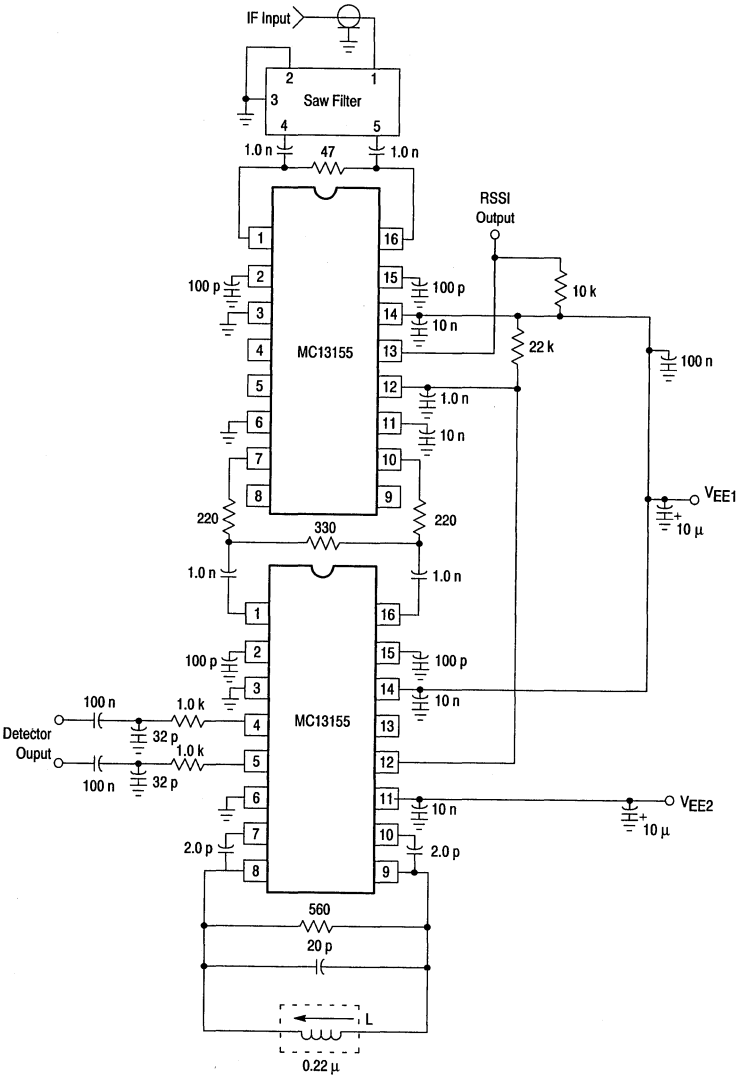
Device	V_{CC}	I_{CC}	Function		Suffix/ Case
MC1596 MC1496	5.0 V to 30 V	10 mA	Carrier Balance >50 dB	General purpose balanced modulator/ demodulator for AM, SSB, FM detection	L/632 P/646 D/751A

Wideband FM IF

MC13155D T_A = 40° to +85°C, Case 648, 751B

The MC13155D is a complete wideband FM detector designed for satellite TV and other wideband data and analog FM applications. Devices may be cascaded for higher IF gain and extended Receive Signal Strength Indicator (RSSI) range.

- 12 MHz Video/Baseband Demodulator
- Ideal for Wideband Data and Analog FM Systems
- Limiter Output for Cascade Operation
- Low Drain Current: 7.0 mA
- Low Supply Voltage: 3.0 to 6.0 V
- Operates to 300 MHz



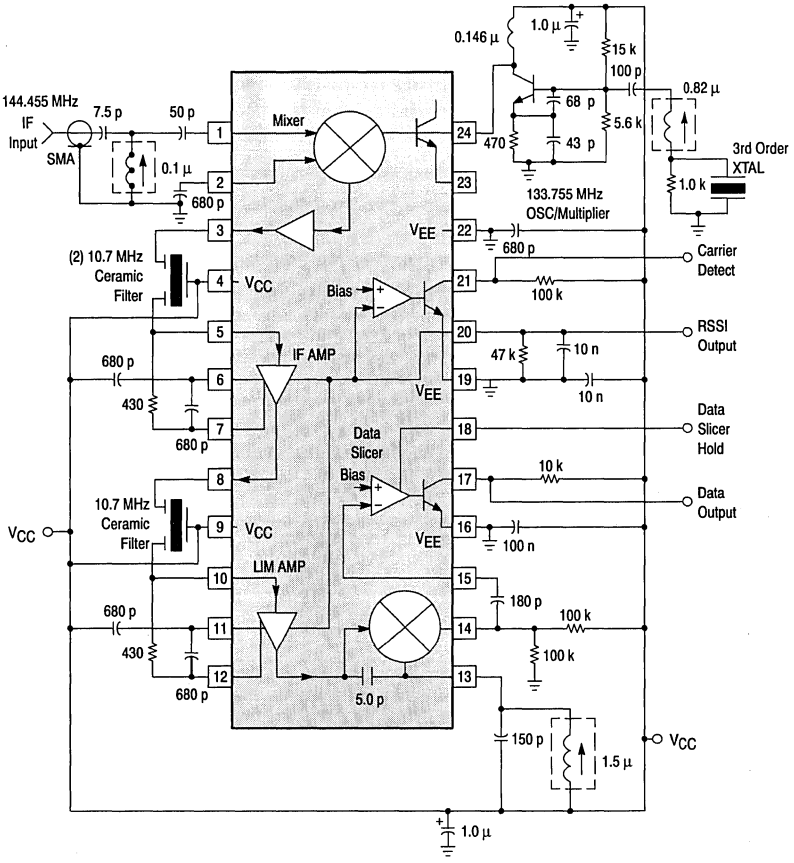
Wideband FM IF System

MC13156DW T_A = –40° to +85°C, Case 751E

The MC13156 is a wideband FM IF subsystem targeted at high performance data and analog applications. Excellent high frequency performance is achieved, with low cost, through use of Motorola's MOSAIC 1.5™ RF bipolar process. The MC13156 has an onboard Colpitts VCO for PLL controlled multichannel operation. The mixer is useful to beyond 200 MHz and may be used in a differential, balanced, or single-ended configuration. The IF amplifier is split to accommodate two low cost cascaded filters. RSSI output is derived by summing the output of both IF sections. A precision data shaper has a hold function to preset the shaper for fast recovery of new data.

Applications for the MC13156 include CT-2, wideband data links, and other radio systems utilizing GMSK, FSK or FM modulation.

- 2.0 to 6.0 Vdc Operation
- Typical Sensitivity of 6.0 μV for 12 dB SINAD
- RSSI Range of Greater than 70 dB
- High Performance Data Shaper for Enhanced CT-2 Operation
- Internal 300 Ω and 1.4 kΩ Terminations for 10.7 MHz and 455 kHz Filters
- Split IF for Improved Filtering and Extended RSSI Range

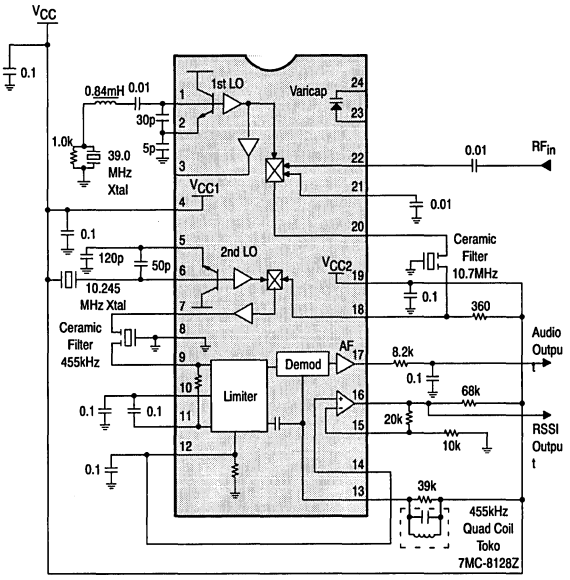


Narrowband FM Receiver

MC13135/136P, DW T_A = –40° to +85°C, Case 724, 751E

The MC13135 is a full dual conversion receiver with oscillators, mixers, Limiting IF Amplifier, Quadrature Discriminator, and RSSI circuitry. It is designed for use in security systems, cordless phones, and VHF mobile and portable radios. Its wide operating supply voltage range and low current make it ideal for battery applications. The Received Signal Strength Indicator (RSSI) has 65 dB of dynamic range with a voltage output, and an operational amplifier is included for a DC buffered output. Also, an improved mixer third order intercept enables the MC13135 to accommodate larger input signal levels.

- Complete Dual Conversion Circuitry
- Low Voltage: 2.0 to 6.0 Vdc
- RSSI with Op Amp: 65 dB Range
- Low Drain Current: 3.5 mA Typical
- Improved First and Second Mixer 3rd Order Intercept
- Detector Output Impedance: 25 Ω Typically

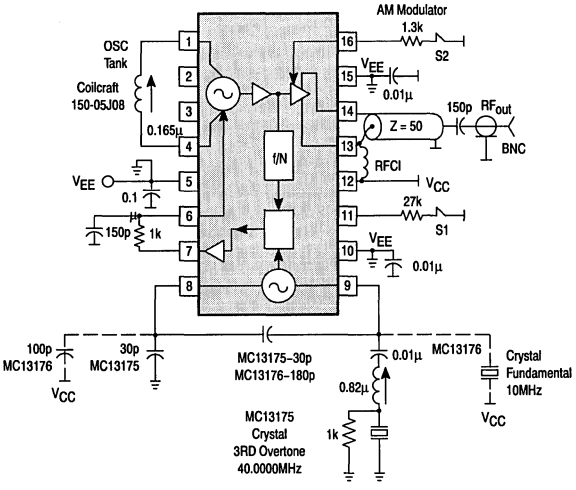


UHF, FM/AM Transmitter

MC13175/176D T_A = 0° to +70°C, Case 751B

The MC13175 and MC13176 are one chip FM/AM transmitter subsystems designed for AM/FM communication systems operating in the 260 to 470 MHz band covered by FCC Title 47; Part 15. They include a Colpitts crystal reference oscillator, UHF oscillator, ÷8 (MC13175) or ÷32 (MC13176) prescaler, and phase detector forming a versatile PLL system. Another application is as a local oscillator in a UHF or 900 MHz receiver. MC13175/176 offer the following features:

- Power Down Feature
- UHF Current Controlled Oscillator
- Use Easily Available 3rd Overtone or Fundamental Crystals for Reference
- Low Number of External Parts Required
- Low Operating Supply Voltage (1.8–5.0 Vdc)
- Low Supply Drain Currents
- Power Output Adjustable (Up to +10 dBm)
- ASK Modulated by Switching Output On and Off
- Differential Output for Loop Antenna or Balun Transformer Networks
- MC13175 — $f_o = 8 \times f_{ref}$
- MC13176 — $f_o = 32 \times f_{ref}$

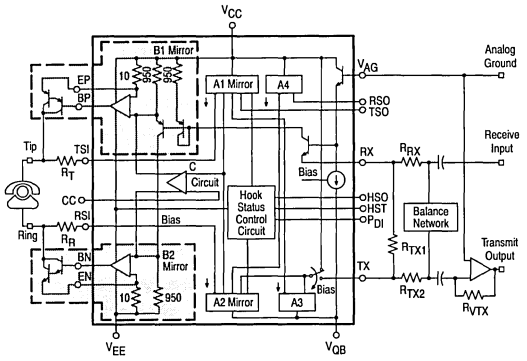


Subscriber Loop Interface Circuits (SLIC)

MC3419-1L T_A = 0° to +70°C, Case 726

The replacement of two-to-four wire conversion hybrid transformers in Central Office, PBX, and Subscriber Carrier equipment with the SLIC has resulted in major improvement in telephone equipment. The SLIC family performs this task, along with most other **BORSHT** functions required by signal transmission. These include the provision of DC power to the telephone (**B**attery); **O**vervoltage protection; **R**ing trip detection; **S**upervisory features such as hook status and dial pulsing; 2-to-4 wire conversion, suppression of longitudinal signals (**H**ybrid).

- All Key Parameters Externally Programmable
- Current Sensing Outputs Monitor Status of both Tip and Ring Leads
- On-Hook Power Below 5.0 mW
- Digital Hook Status Output
- Power Down Input
- Ground Fault Protection
- Size and Weight Reduction over Conventional Approaches
- The sale of this product is licensed under Patent No. 4,004,109. All royalties related to this patent are included in the unit price.



MC33120/1P, FN T_A = –40° to +85°C, Case 738, 776

With a guaranteed minimum longitudinal balance of 58 dB, the MC33120/1 is ideally suited for Central Office applications, as well as PBXs, and other related equipment. Protection and sensing components on the two-wire side can be non-precision while achieving required system performance. Most BORSHT functions are provided while maintaining low power consumption, and a cost effective design. Size and weight reduction over conventional transformer designs permit a higher density system.

- All key parameters externally programmable with resistors:
  - Transmit and Receive Gains
  - Transhybrid Loss
  - Return Loss
  - DC Loop Current Limit and Battery Feed Resistance
  - Longitudinal Impedance
- Single and Double Fault Sensing and Protection
- Minimum 58 dB Longitudinal Balance (2-wire and 4-wire) Guaranteed
- Digital Hook Status and Fault Outputs
- Power Down Input
- Loop Start or Ground Start Operation
- Size & Weight Reduction Over Conventional Approaches
- Available in 20 Pin DIP and 28 Pin PLCC Packages
- Battery Voltage: –42 V to –58 V (for MC33120), –21.6 V to –42 V (for MC33121)

MC33122 T_A = –40° to +85°C, Case *TBD

The MC33122 is designed to provide the interface between the four-wire side of a Central Office or remote terminal and the two-wire subscriber line. Interface functions include battery feed, proper loop termination AC impedance, adjustable transmit, receive and transhybrid gains, hookswitch and ring trip detection. Additionally, the MC33122 provides a minimum of 58 dB of longitudinal balance.

The transmit and receive signals are referenced to analog ground (VAG), easing the interface to Codecs, filters, etc. The logic interface is TTL and CMOS compatible.

Internal loop current power transistors sink and source current at tip and ring. Thermal shutdown is provided to protect against line faults. A switching regulator is used to reduce power dissipation and enhance reliability, and a clock input allows synchronization to minimize noise.

The MC33122 will be fabricated on a standard high voltage (90 V) BiMOS process to increase protection during lightning surges. It will be available in a 52 pin PLCC and 64 pin QFP package.

- Designed in Accordance with TR-000057 and TA-000909 Bellcore Objectives
- Suitable for CO, Digital Loop Carrier Systems (DLCS), and PBX
- Full On-Hook Transmission Capability
- On-Chip Loop Current Power Transistors
- Reduced Power Dissipation with Switching Regulator
- Minimum 58 dB Longitudinal Balance
- Externally Adjustable Impedance, Tx, Rx and Transhybrid Gains
- Current Limit Externally Adjustable to 50 mA
- Hook Switch Detection and Ring Tip Capability, Adjustable
- Polarity Reversal and Power Down Capability
- Ground Start Sequence Controls
- Two Relay Drivers

8

PBX Architecture (Analog Transmission)

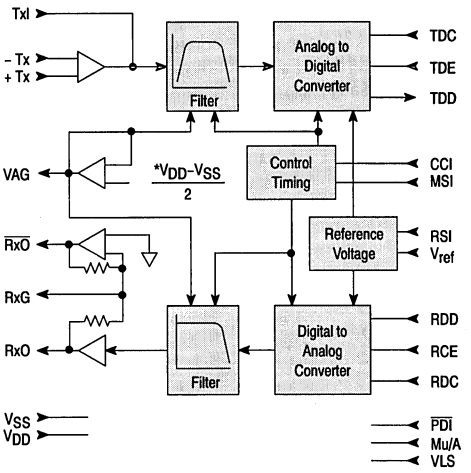
PCM Mono-Circuits Codec-Filters (CMOS LSI)

MC145500 Series Case 620, 648, 708, 726, 736, 751, 776

The Mono-circuits perform the digitizing and restoration of the analog signals. In addition to these important functions, Motorola's family of pulse-code modulation mono-circuits also provides the band-limiting filter functions — all on a single monolithic CMOS chip with extremely low power dissipation.

The Mono-circuits require no external components. They incorporate the bandpass filter required for antialiasing and 60 Hz rejection, the A/D–D/A conversion functions for either U.S. Mu-Law or European A-Law companding formats, the low-pass filter required for reconstruction smoothing, an on-board precision voltage reference, and a variety of options that lend flexibility to circuit implementations. Unique features of Motorola's Mono-circuit family include wide power supply range (6 to 13 V) selectable on-board voltage reference (2.5, 3.1, or 3.8 V), and TTL or CMOS I/O interface.

Motorola supplies five versions in this series. The MC145500, MC145503 and MC145505 are general-purpose devices in 16 pin packages designed to operate in digital telephone or line card applications. The MC145501 is the same device (in an 18 pin package) that offers the capability of selecting from three peak overload voltages (2.5, 3.15 and 3.78 V). The MC145502 is the full-feature device that presents all of the options available on the chip. This device is packaged in a 22 pin DIP and 28 pin chip carrier package.



8

PCM Mono-Circuits Codec-Filters

MC145554/57/64/67 Case 620, 648, 732, 738, 751D, 751G

These per channel PCM Codec-filters perform the voice digitization and reconstruction as well as the band limiting and smoothing required for PCM systems. They are designed to operate in both synchronous and asynchronous applications and contain an on-chip precision voltage reference. The MC145554 (Mu-Law) and MC145557 (A-Law) are general purpose devices that are offered in 16 pin packages. The MC145564 (Mu-Law) and MC145567 (A-Law), offered in 20 pin packages, add the capability of analog loop-back and push-pull power amplifiers with adjustable gain.

All four devices include the transmit bandpass and receive lowpass filters on-chip, as well as active RC pre-filtering and post-filtering. Fully differential analog circuit design assures lowest noise. Performance is specified over the extended temperature range of –40° to +85°C.

These PCM Codec-filters accept both industry standard clock formats. They also maintain compatibility with Motorola's family of MC3419/MC33120 SLIC products.

MC145480 Case 738, 751D

This 5.0 V, general purpose per channel PCM Codec-filter offers selectable Mu-Law or A-Law companding in 20 pin DIP and SOG packages. It performs the voice digitization and reconstruction as well as the band limiting and smoothing required for PCM systems. It is designed to operate in both synchronous and asynchronous applications and contains an on-chip precision reference voltage (1.575 V).

The transmit bandpass and receive lowpass filters, and the active RC pre-filtering and post-filtering are incorporated, as well as fully differential analog circuit design for lowest noise. Push-pull 300 Ω power drivers with external gain adjust are also included.

The MC145480 PCM Codec-filter accepts a variety of clock formats, including short-frame sync, long-frame sync, IDL, and GCI timing environments. This device also maintains compatibility with Motorola's family of Telecom products, including the MC145472 U Interface Transceiver, MC145474/75 S/T Interface Transceiver, MC145532 ADPCM Transcoder, MC145422/26 UDLT-I, MC145421/25 UDLT-II, and MC3419/MC33120 SLIC.

Also Available — Filters:

MC145414

Dual Tuneable Low-Pass Sampled Data Filter

MC145432

2600 Hz Tone Signalling Filter

Crosspoint Switches

Crosspoint switches implemented with semiconductor technology take the place of the huge banks of mechanical relay matrices once utilized in Central Offices and PBXs.

Motorola's crosspoint switches have latches to control the state of any particular switch in order to route analog or digital signals. These ICs find applications in PBXs, key systems, and test equipment.

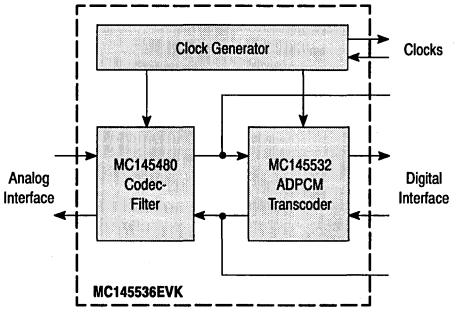
Device	Description	Suffix/ Case
MC142100	4 × 4 × 1 Analog Switch • 4.2 to 18 V operation • Low on-state resistance	CL/620 CP/648 DW/751G
MC145100	4 × 4 × 1 Analog Switch • 4.2 to 18 V operation • Low on-state resistance • Power-on reset	CP/648

Codec-Filter/ADPCM Transcoder Evaluation Kits

MC145536EVK

The MC145536EVK is the primary tool for evaluation and demonstration of the MC145480 Single +5.0 V supply PCM Codec-Filter and the MC145532 ADPCM Transcoder (see "Telephone Accessory Circuits"). The MC145536EVK provides the necessary hardware needed to evaluate the many separate operating modes under which the MC145480 and MC145532 are intended to operate.

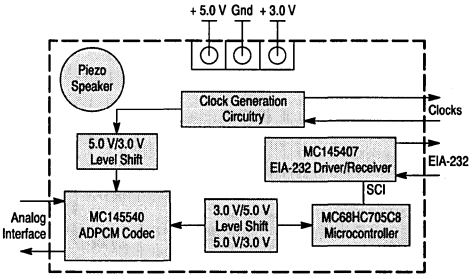
- Provides Stand Alone Evaluation on a Single Board
- Easily Interfaced to test Equipment, Customer System, or second MC145536EVK
- Convenient access to Key Signals
- Generous wire-wrap area for Application Development
- The kit provides Analog-to-Analog, Analog-to-Digital, or Digital-to-Analog connections — with Digital connections being 64 kbps PCM; 32, 24, or 16 kbps Motorola. Proprietary ADPCM
- Compatible Handset included
- Schematics, Data Sheets, and User's Manual included.



MC145537EVK

The MC145537EVK is the primary tool for evaluation and demonstration of the MC145540 ADPCM Codec. It provides the necessary hardware and software interface to access the many features and operational modes of the MC145540 ADPCM Codec.

- Provides Stand Alone Evaluation on Single Board
- The kit provides Analog-to-Analog, Analog-to-Digital or Digital-to-Analog connections — with Digital connections being 64 kbps PCM; 32 or 24 kbps ADPCM; 16 kbps CCITT G.726 or Motorola Proprietary ADPCM
- +5.0 V only Power Supply, or 5.0 V plus 2.7 to 5.25 V Supply
- Easily Interfaced to test Equipment, Customer System, Second MC145537EVK or MC145536EVK (5.0 V only) for Full Duplex Operation
- Convenient Access to Key Signals
- Piezo Loudspeaker
- EIA-232 Serial Computer Terminal Interface for Control of the MC145540 ADPCM Codec Features
- Compatible Handset Provided
- Schematics, Data Sheets, and User's Manual Included



Dual Tone Multiple Frequency Receiver

MC145436 Case 646, 751

This device contains the filter and decoder for detection of a pair of tones conforming to the DTMF standard with outputs in hexadecimal. Switched capacitor filter technology is used together with digital circuitry for the timing control and output circuits. The MC145436 provides excellent power-line noise and dial tone rejection.

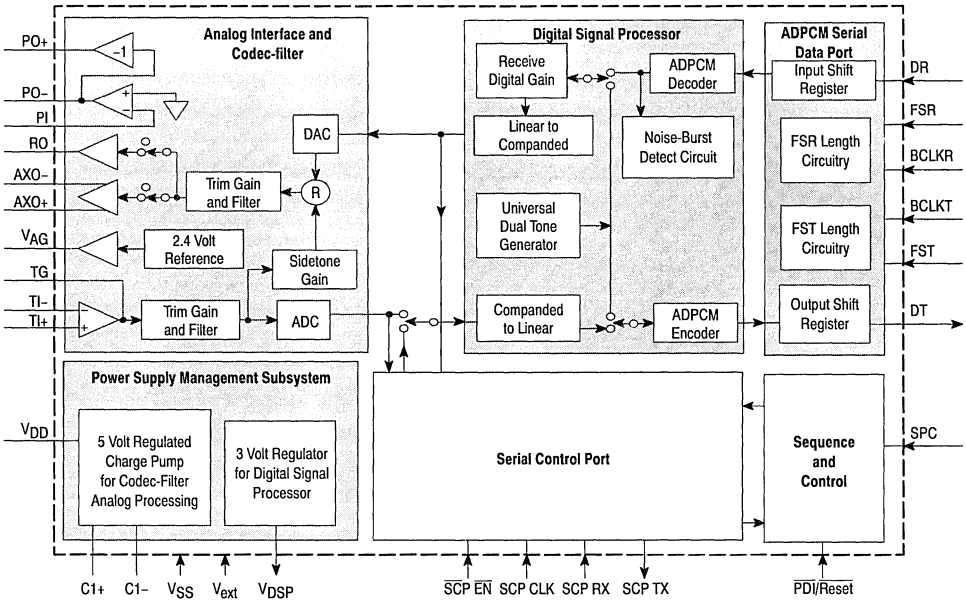
ADPCM Codec

MC145540 Case 710, 751F

The MC145540 ADPCM Codec is a single chip implementation of a PCM codec-filter and an ADPCM encoder/decoder, and therefore provides an efficient solution for applications requiring the digitization and compression of voiceband signals. This device is designed to operate over a wide voltage range, 2.7 V to 5.25 V, and as such is ideal for battery powered as well as AC powered applications. The MC145540 ADPCM Codec also includes a serial control port and internal control and status registers that permit a microcomputer to exercise many built-in features.

The ADPCM Codec is designed to meet the 32 kbps ADPCM conformance requirements of CCITT Recommendation G.721 and ANSI T1.301. It also meets ANSI T1.303 and CCITT Recommendation G.723 for 24 kbps ADPCM operation, and the 16 kbps ADPCM standard, CCITT Recommendation G.726. This device also meets the PCM conformance specification of the CCITT G.714 Recommendation.

Block Diagram



8

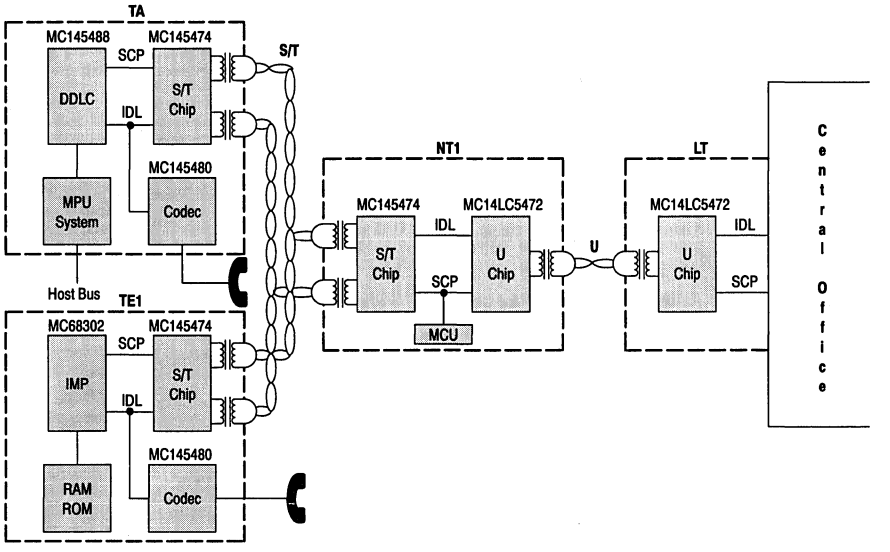
ISDN Voice/Data Circuits

Integrated Services Digital Network

ISDN is the revolutionary concept of converting the present analog telephone networks to an end-to-end global digital network. ISDN standards make possible a wide variety of services and capabilities that are revolutionizing communications in virtually every industry.

Motorola's ISDN product family includes: the MC145472 U-Interface Transceiver; the MC145474/75 S/T-Interface Transceivers; MC145488 Dual Data Link Controller; and the MC68302 Integrated Multi-Protocol Processor. These are supported by a host of related devices including: the MC145480 +5.0 V PCM Codec-Filter; MC145532 ADPCM Transcoder; MC145540 ADPCM Codec; MC145500 family of single-chip Codec/filters; MC145436 DTMF Decoder; MC33120 Subscriber Loop Interface Circuit; MC34129 Switching Power Supply Controller; MC145611 PCM Conference Circuit; and the MC145406/07 CMOS EIA 232-D Driver/ Receiver family.

Motorola's key ISDN devices fit into four ISDN network applications: a digital subscriber line card, an NT1 network termination, an ISDN terminal adapter, and an ISDN terminal. Digital subscriber line cards are used in central offices, remote concentrators, channel banks, T1 multiplexers, and other switching equipment. The NT1 network termination block illustrates the simplicity of remote U to S/T-interface conversion. The ISDN terminal adapter and ISDN terminal block show how Motorola ICs are used to combine voice and data in PC compatible boards, digital telephones, and other terminal equipment. Expanded applications such as a PBX may include these and other Motorola ISDN circuits. Many "non-ISDN" uses, such as pairgain applications, are appropriate for Motorola's ISDN devices as well.



U-Interface Transceivers

MC145472 Case 847B
MC14LC5472 Case 847B, 847

The MC145472/MC14LC5472 fully conforms to ANSI T1.601-1991, the North American standard for ISDN Basic Access on a single twisted-wire pair. The transceiver achieves a remarkable 10^{-7} bit error rate performance on all ANSI specified test loops with worst-case impairments present. The state-of-the-art 1.2 micron single-chip solution uses advanced design techniques to combine precision analog signal processing elements with three digital signal coprocessors to build an adaptively equalized echo cancelling receiver.

Two modes of handling U-interface maintenance functions are provided on the MC145472/MC14LC5472. In the automatic maintenance mode the U-interface transceiver handles all ANSI specified maintenance and channel procedures internally to minimize your software development effort. Automatic procedures include generating and monitoring the cyclic redundancy check, reporting and counting far end block errors (near end block errors too), handling the ACT and DEA bits, as well as monitoring and appropriately responding to embedded operations channel messages.

The optional manual maintenance mode lets you choose an inexpensive microcontroller, such as a member of Motorola's MC68HC05 family, to control and augment the standard maintenance channel functions. This flexible feature also allows for easy implementation of proprietary maintenance functions.

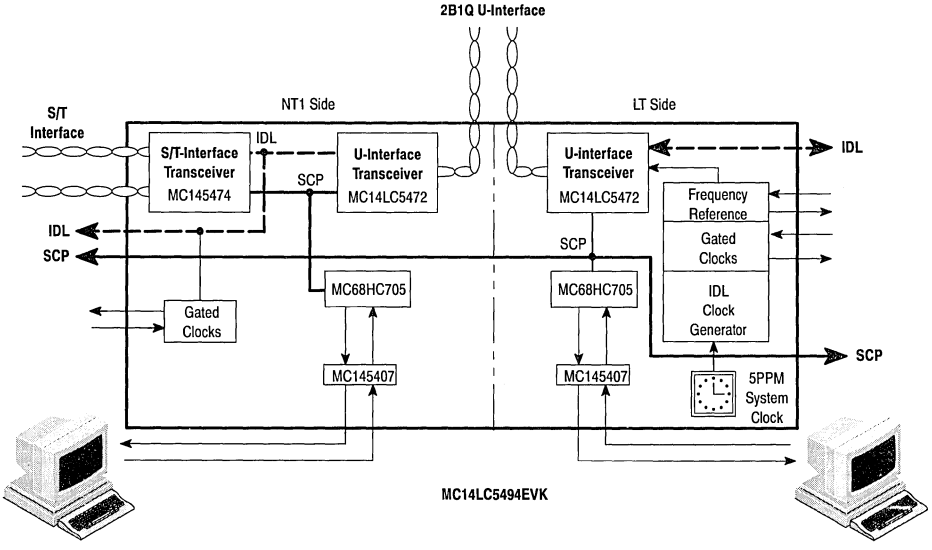
U-Interface Transceiver Evaluation Kit

MC14LC5494EVK

This kit provides the hardware and software to evaluate the many configurations under which the MC14LC5472 is able to operate. Used as a whole, it operates as both ends of the two-wire U-Interface that extends from the customer premises (NT1) to the switch line card (LT). The two halves of the board can be physically and functionally separated, providing independent NT1 and LT evaluation capability.

The kit provides the ability to interactively manipulate status registers in the MC14LC5472 U-Interface Transceiver or in the MC145474/75 S/T-Interface Transceiver with the aid of an external terminal. The device can also be controlled using the MC68302 Integrated Multiprotocol Processor application development system to complete a total Basic Rate ISDN evaluation solution.

A generous wire-wrap area is available to assist application development.



Dual Data Link Controller

MC145488 Case 779

The MC145488 features two full-duplex serial HDLC channels with an on-chip Direct Memory Access (DMA) controller. The DMA controller minimizes the number of microprocessor interrupts from the communications channels, freeing the microprocessor's resources for other tasks. The DMA controller can access up to 64 k bytes of memory, and transfers either 8-bit bytes or 16-bit words to or from memory. The MC145488 DDLC is compatible with Motorola's MC68000 and other microprocessors.

In a typical ISDN terminal application, one DDLC communications channel supports the D-channel (LAPD) while the other supports the B-channel (LAPB). While the DDLC is ideally suited for ISDN applications, it can support many other HDLC protocol applications as well.

Some of the powerful extras found on the DDLC include automatic abort and retransmit of D-channel collisions in S/T-interface applications, address recognition, automatic recovery mechanisms for faulty frame correction, and several system test modes. Address recognition provides a reduction in the host microprocessor load by filtering data frames not addressed to the host. The DDLC can compare either SAPI or TEI fields of LAPD frames. For LAPD (Q.921) applications, both A and B addresses may be checked.

S/T-Interface Transceivers

MC145474 Case 736A
MC145475 Case 710, 751F

The MC145474/75 S/T-Interface Transceivers provide a CCITT I.430 compatible interface for use in line card, network termination, and ISDN terminal equipment applications. Manufactured with Motorola's advanced 1.5 micron CMOS mixed analog and digital process technology, the MC145474/75 is a physical layer device capable of operating in point-to-point or point-to-multipoint passive bus arrangements. In addition, the MC145475 can implement the optional NT1 Star topology.

This device features outstanding transmission performance. It reliably transmits over 2.5 kilometers in a point-to-point application with specifications of 1 kilometer. Comparable performance is achieved in all other topologies as well. Other features include pin selectable terminal or network operating modes, industry standard microprocessor serial control port, full support of the multiframing S and Q channels, a full range of loopbacks, and low power CMOS operation.

Voice/Data Communication (Digital Transmission)

2-Wire Universal Digital Loop Transceiver (UDLT)

MC145422 Master Station Case 708, 736, 751E
MC145426 Slave Station Case 708, 736, 751E

The UDLT family of transceivers allows the use of existing twisted-pair telephone lines (between conventional telephones and a PBX) for the transmission of digital data. With the UDLT, every voice-only telephone station in a PBX system can be upgraded to a digital telephone station that handles the complex voice/data communications with no increase in cabling costs.

In implementing a UDLT-based system the A/D to D/A conversion function associated with each telset is relocated from the PBX directly to the telset. The SLIC (or its equivalent circuit) is eliminated since its signaling information is transmitted digitally between two UDLTs.

The UDLT master-slave system incorporates the modulation/demodulation functions that permit data communications over a distance up to 2 kilometers. It also provides the sequence control that governs the exchange of information between master and slave. Specifically, the master resides on the PBX line card where it transmits and receives data over the wire pair to the telset. The slave is located in the telset and interfaces the mono-circuit to the wire pair. Data transfer occurs in 10-bit bursts (8 bits of data and 2 signaling bits), with the master transmitting first, and the slave responding in a synchronized half-duplex transmission format.

UDLTs utilize a 256 kilobaud Modified Differential Phase Shift Keyed (MDPSK) burst modulation technique for transmission to minimize radio frequency, electromagnetic, and crosstalk interference. Implementation through CMOS technology takes advantage of low-power operation, increased reliability, and the proven capabilities to perform complex telecommunications functions.

Functional Features

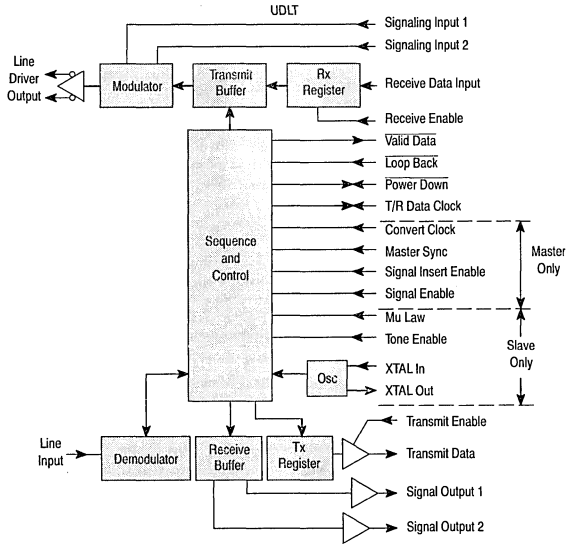
- Provides Synchronous Duplex 64 kbits/Second Voice/Data Channel and Two 8 kbits/Second Signaling Data Channels Over One 26 AWG Wire Pair Up to 2 km.
- Compatible with Existing and Evolving Telephone Switch Architectures and Call Signaling Schemes
- Automatic Detection Threshold Adjustment for Optimum Performance Over Varying Signal Attenuations
- Protocol Independent
- Single 5.0 V to 8.0 V Power Supply

MC145422 Master UDLT

- 2.048 MHz Master Clock
- Pin Controlled Power-Down and Loop-Back Features
- Variable Data Clock — 64 kHz to 2.56 MHz
- Pin Controlled Insertion/Extraction of 8 kbits/Seconds Channel into LSB of 64 kbits/Second Channel for Simultaneous Routing of Voice and Data Through PCM Voice Path of Telephone Switch

MC145426 Slave UDLT

- Compatible with MC145500 Series and Later PCM Mono-Circuits
- Automatic Power-Up/Down Feature
- On-Chip Data Clock Recovery and Generation
- Pin Controlled 500 Hz D3 or CCITT Format PCM Tone Generator for Audible Feedback Applications



2-Wire ISDN Universal Digital Loop Transceiver II (UDLT II)

MC145421 Master Case 623, 709, 751E
MC145425 Slave Case 623, 709, 751E

Similar to the MC145422/26 UDLT, but provide 160 kbps in two 64 kbps and two 16 kbps (2B + 2D) format.

Data Set Interface Circuit (DSI)

MC145428 T_A = –40° to + 85°C, Case 738, 751D

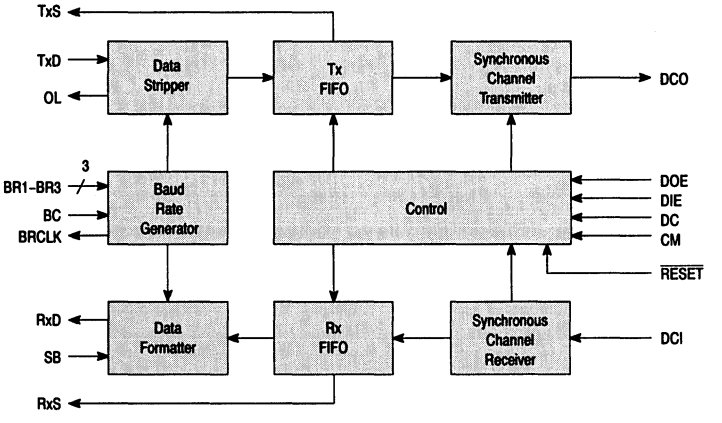
This new CMOS LSI circuit provides asynchronous-to-synchronous data conversion. It is particularly well-suited for use in conjunction with a UDLT-based integrated voice/data system. The MC145428 DSI provides EIA-232-to-time slot data conversion that permits direct interface between existing data equipment and the UDLT without modifications. With this interactive component, digitized voice information from the PCM Mono-Circuit and asynchronous data from computers or terminals can be transmitted simultaneously through a synchronous switching network.

DSI circuits are also suited for data multiplexers, concentrators and deconcentrators, data rate changers, data-only switching, and PBX-based local area networks.

- Up to 128 kbps asynchronous data rate operation
- 0 up to 2.1 Mbps synchronous data rate operation
- On-board bit rate clock generator with pin selectable bit rates of 300, 1200, 2400, 4800, 9600, 19200, and 38400 bps or an externally supplied 16 times bit rate clock may be used
- Accepts asynchronous data words of 8 or 9 bits
- False start detection provided
- Automatic sync insertion and checking

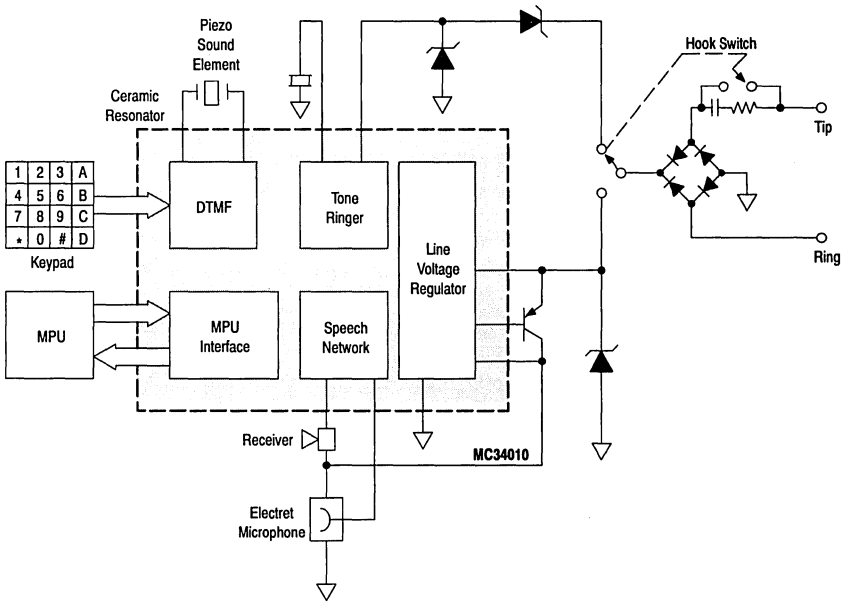
8

Data Set Interface Circuit



Complete Electronic Telephone Circuit

MC34010P, FN T_A = –20° to +60°C, Case 711, 777



The conventional transformer-driven telephone handset is undergoing major innovations. The bulky transformer is disappearing. So are many of its discrete components, including the familiar telephone bell. They are being replaced with integrated circuits that perform all the major handset functions simply, reliably and inexpensively . . . functions such as 2-to-4 wire conversion, DTMF dialing, tone ringing, and a variety of related activities.

The culmination of these capabilities is the Electronic Telephone Circuit, the MC34010. These ICs place all of the above mentioned functions on a single monolithic chip.

These telephone circuits utilize advanced bipolar linear (I^2L) technology and provide all the necessary elements of a modern tone-dialing telephone. The MC34010 even incorporates an MPU interface circuit for the inclusion of automatic dialing in the final system.

- Provides all basic telephone functions, including DTMF dialer, tone ringer, speech network and line voltage regulator.
- DTMF generator uses low cost ceramic resonator with accurate frequency synthesis technique.
- Tone ringer drives piezoelectric transducer and satisfies EIA-470 requirements
- Speech network provides 2-to-4 wire conversion with adjustable sidetone utilizing an electret transmitter
- On-chip regulator insures stable operation over wide range of loop lengths
- I^2L technology provides low 1.4 V operation and high static discharge immunity
- Microprocessor interface port for automatic dialing features

Also Available

A broad line of additional telephone components for customizing systems design.

Audio Control Circuit

MC145429

Telset audio interface circuit for MPU-controlled independent adjustment of ear piece, speaker and ringer volume.

Dial Circuits

MC145412/13/16

Integrated Tone/Pulse 10-number Repertory Dialer.

MC145512/13

Integrated Tone/Pulse 10-number Repertory Dialer.

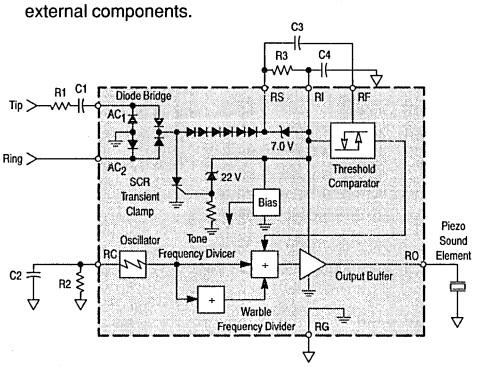
Tone Ringers

The MC34012, MC34017, and MC34117 Tone Ringers are designed to replace the bulky bell assembly of a telephone, while providing the same function and performance under a variety of conditions. The operational requirements spelled out by the FCC and EIA-470, simply stated, are that a ringer circuit MUST function when a ringing signal is provided, and MUST NOT ring when other signals (speech, dialing, noise) are on the line. The tone ringers described below were designed to meet those requirements with a minimum of external components.

MC34012P, D

T_A = –20° to +60°C, Case 626, 751

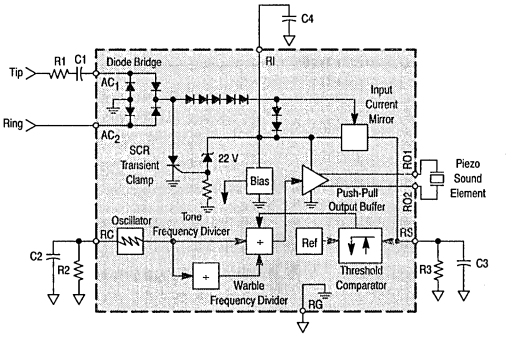
- Complete Telephone Bell Replacement
- On-Chip Diode Bridge and Transient Protection
- Single-Ended Output to Piezo Transducer
- Input Impedance Signature Meets Bell and EIA Standards
- Rejects Rotary Dial and Hook Switch Transients
- Adjustable Base Frequencies
- Output Frequency to Warble Ratio — MC34012-1:80
  MC34012-2:160
  MC34012-3:40



MC34017P, D

T_A = –20° to +60°C, Case 626, 751

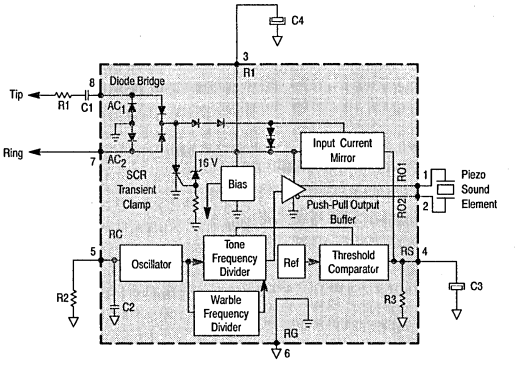
- Complete Telephone Bell Replacement
- On-Chip Diode Bridge and Transient Protection
- Differential Output to Piezo Transducer for Louder Sound
- Input Impedance Signature Meets Bell and EIA Standards
- Rejects Rotary Dial and Hook Switch Transients
- Output Frequency to Warble Ratio — MC34017-1:80
  MC34017-2:160
  MC34017-3:40



MC34217P, D

T_A = –20° to +60°C, Case 626, 751

- Complete Telephone Bell Replacement
- On-Chip Diode Bridge
- Internal Transient Protection
- Differential Output to Piezo Transducer for Louder Sound
- Input Impedance Signature Meets Bell and EIA Standards
- Rejects Rotary Dial and Hook Switch Transients
- Base Frequency and Warble Frequencies are Independently Adjustable
- Adjustable Base Frequency
- Reduced Number of Externals



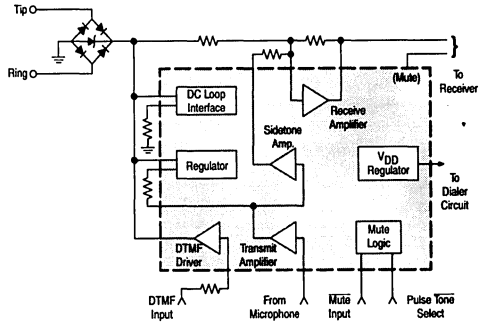
Speech Networks

Speech Network with Dialer Interface

MC34014P, DW T_A = –20° to +60° C, Case 707, 751D

The MC34014 is a Telephone Speech Network integrated circuit which incorporates adjustable transmit, receive, and sidetone functions, line interface circuit, dialer interface, and a regulated output voltage for a dialer circuit. It includes an equalization circuit to compensate for various line lengths and the conversion from 2-to-4 wire is accomplished with supply voltages as low as 1.5 V.

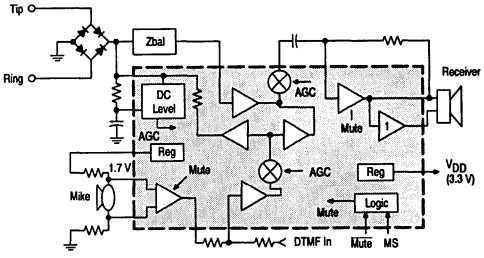
- Transmit, Receive, and Sidetone Gains Set by External Resistors
- Loop Length Equalization for Transmit, Receive, and Sidetone Functions
- Operates Down to 1.5 V (V +) in Speech Mode
- Provides Regulated Voltage for CMOS Dialer
- Speech Amplifiers Muted During Pulse and Tone Dialing
- DTMF Output Level Adjustable with a Single Resistor
- Compatible with 2-Terminal Electret Microphones
- Operates with Receiver Impedances of 150 Ω and Higher



Telephone Speech Network with Dialer Interface

MC34114P, DW T_A = –20° to +70° C, Case 707, 751D

- Operation Down to 1.2 V
- Adjustable Transmit, Receive, and Sidetone Gains by External Resistors
- Differential Microphone Amplifier Input Minimizes RFI
- Transmit, Receive, and Sidetone Equalization on both Voice and DTMF Signals
- Regulated 1.7 V Output for Biasing Microphone
- Regulated 3.3 V Output for Powering External Dialer
- Microphone and Receive Amplifiers Muted During Dialing
- Differential Receive Amplifier Output Eliminates Coupling Capacitor
- Operates with Receiver Impedances of 150 Ω and Higher



8

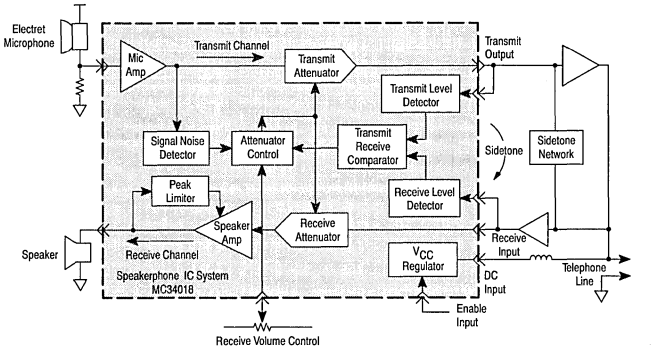
Speakerphone

Voice Switched Speakerphone Circuit

MC34018P, DW T_A = –20° to +60°C, Case 710, 751F

The MC34018 Speakerphone integrated circuit incorporates the necessary amplifiers, attenuators, and control functions to produce a high quality hands-free speakerphone system. Included are a microphone amplifier, a power audio amplifier for the speaker, transmit and receive attenuators, a monitoring system for background sound level, and an attenuation control system which responds to the relative transmit and receive levels as well as the background level. Also included are all necessary regulated voltages for both internal and external circuitry, allowing line-powered operation (no additional power supplies required). A Chip Select pin allows the chip to be powered down when not in use. A volume control function may be implemented with an external potentiometer. MC34018 applications include speakerphones for household and business uses, intercom systems, automotive telephones, and others.

- All Necessary Level Detection and Attenuation Controls for a Hands-Free Telephone in a Single Integrated Circuit
- Background Noise Level Monitoring with Long Time Constant
- Wide Operating Dynamic Range Through Signal Compression
- On-Chip Supply and Reference Voltage Regulation
- Typical 100 mW Output Power (into 25 Ω) with Peak Limiting to Minimize Distortion
- Chip Select Pin for Active/Standby Operation
- Linear Volume Control Function



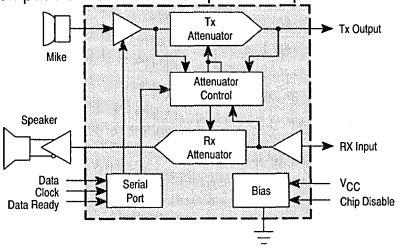
Voice Switched Speakerphone with μProcessor Interface

MC33218P, DW T_A = –40° to +85°C, Case 724, 751E

The MC33218 Voice Switched Speakerphone circuit incorporates the necessary amplifiers, attenuators, level detectors, and control algorithm to form the heart of a high quality hands-free speakerphone system. Included are a microphone amplifier with adjustable gain, and mute control, transmit and receive attenuators which operate in a complementary manner, and level detectors and background noise monitors for both paths. A dial tone detector prevents dial tone from being attenuated by the receive background noise monitor. A Chip Disable pin permits powering down the entire circuit to conserve power.

Also included is an 8-bit serial μprocessor port for controlling the receive volume, microphone mute, attenuator gain, and operation mode (force to transmit, force to receive, etc.). Data rate can be up to 1.0 MHz. The MC33218 can be operated from a power supply, or from the telephone line, requiring typically 3.8 mA. It can also be used in intercoms and other voice-activated applications.

- Low Voltage Operation: 2.5 to 6.0 V
- 2-Point Sensing, Background Noise Monitor in Each Path
- Chip Disable Pin for Active/Standby Operation
- Microphone Amplifier Gain Set by External Resistors, Mute Function Included
- Dial Tone Detector to Inhibit Receive Idle Mode During Dial Tone Presence
- Microprocessor port for controlling:
  - Receive Volume Level (16 Steps)
  - Attenuator Range (26 or 52 dB, Selectable)
  - Microphone Mute
  - Force to Transmit, Receive, Idle or Normal Voice Switched Operation
- Compatible with MC34119 Speaker Amplifier



Voice Switched Speakerphone Circuit

MC34118P, DW T_A = –20° to +60°C, Case 710, 751F

The MC34118 Voice Switched Speakerphone circuit incorporates the necessary amplifiers, attenuators, level detectors, and control algorithm to form the heart of a high quality hands-free speakerphone system. Included are a microphone amplifier with adjustable gain and mute control, Transmit and Receive attenuators which operate in a complementary manner, level detectors at input and output of both attenuators,and background noise monitors for both the transmit and receive channels. A dial tone detector prevents the dial tone from being attenuated by the Receive background noise monitor circuit. Also included are two line driver amplifiers which can be used to form a hybrid network in conjunction with an external coupling transformer. A high-pass filter can be used to filter out 60 Hz noise in the receive channel, or for other filtering functions. A Chip Disable pin permits powering down the entire circuit to conserve power on long loops where loop current is at a minimum.

The MC34118 may be operated from a power supply, or it can be powered from the telephone line, requiring typically 5.0 mA. The MC34118 can be interfaced directly to Tip and Ring (through a coupling transformer) for stand-alone operation, or it can be used in conjunction with a handset speech network and/or other features of a featurephone.

- Improved Attenuator Gain Range: 52 dB between Transmit and Receive
- Low Voltage Operation for Line-Powered Applications (3.0 to 6.5 V)
- 4-Point Signal Sensing for Improved Sensitivity
- Background Noise Monitors for both Transmit and Receive Paths
- Microphone Amplifier Gain set by External Resistors, Mute Function included.
- Chip Disable for Active/Standby Operation
- On Board Filter Pinned-Out for User Defined Function
- Dial Tone Detector Inhibits Receive Idle Mode during Dial Tone presence
- Compatible with MC34119 Speaker Amplifier

Motorola Family of Speakerphone Integrated Circuits

MC34018	MC34118	MC33218
Two point sensing with slow idle, background noise monitor in Tx path only	Four point sensing with both fast and slow idle modes, background noise monitors in both Rx and Tx paths	Two point sensing with slow idle, background noise monitors in both Rx and Tx paths
No dial tone detector in receive path	Receive path has dial tone detector	Receive path has dial tone detector
Attenuator Characteristics: • Range: 44 dB • Tolerance: ±4 dB • Gain tracking not specified • White noise is constant	Attenuator Characteristics: • Range: 52 dB • Tolerance: ±2 dB • Gain Tracking: <1 dB • White noise reduces with volume	Attenuator Characteristics: • Range: 52 or 26 dB (selectable) • Tolerance: ±3 dB • Gain Tracking: <1 dB • White noise reduces with volume
External hybrid required	Hybrid amplifiers on board	External hybrid required
Speaker amplifier is on board (34 dB, 100 mW)	External speaker amplifier required (MC34119)	External speaker amplifier required (MC34119)
Filtering is external	Configurable filter on board	Filtering is external
Microphone amplifier has fixed gain and no muting	Microphone amplifier has adjustable gain and mute input	Microphone amplifier has adjustable gain, and can be muted through µP port
Supply Voltage: 4.0 V to 11 V	Supply Voltage: 2.8 V to 6.5 V	Supply Voltage: 2.5 V to 6.5 V
Supply Current: 6.5 mA typ., 9.0 mA max	Supply Current: 5.5 mA typ., 8.0 mA max	Supply Current: 4.0 mA typ., 5.0 mA max
Speaker amplifier reduces gain to prevent clipping	Receive gain is reduced as supply voltage falls to prevent clipping	Receive gain is reduced as supply voltage falls to prevent clipping
Volume control is linear. Cannot override voice switched operation except through additional circuitry. Attenuator gain is fixed at 44 dB (slightly variable). No microphone mute.	Volume control is linear, and microphone mute has separate pin. Cannot override voice switched operation except through additional circuitry. Attenuator gain is fixed at 52 dB.	8-bit µP serial port controls: • Volume control (16 steps) • Microphone mute • Range selection (26 dB or 52 dB) • Force to transmit, idle, receive, or normal voice switched operation
28 Pin DIP and SOIC packages	28 Pin DIP and SOIC packages	24 Pin narrow DIP and SOIC packages
External Required: • 12 Resistors • 11 Capacitors (≤1.0 µF) • 8 Capacitors (>1.0 µF)	External Required: • 14 Resistors • 12 Capacitors (≤1.0 µF) • 9 Capacitors (>1.0 µF)	External Required: • 12 Resistors • 11 Capacitors (≤1.0 µF) • 4 Capacitors (>1.0 µF)
Temperature Range: –20° to +60 °C	Temperature Range: –20° to +60 °C	Temperature Range: –40° to +85 °C

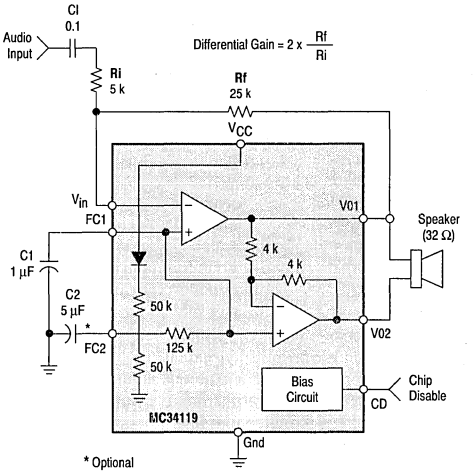
Telephone Accessory Circuits

Audio Amplifier

MC34119P, D T_A = 0° to +70°C, Case 626, 751

A low power audio amplifier circuit intended (primarily) for telephone applications, such as speakerphones. Provides differential speaker outputs to maximize output swing at low supply voltages (2.0 V min.). Coupling capacitors to the speaker, and snubbers, are not required. Overall gain is externally adjustable from 0 to 46 dB. A Chip Disable pin permits powering-down to mute the audio signal and reduce power consumption.

- Drives a Wide Range of Speaker Loads (16 to 100 Ω)
- Output Power Exceeds 250 mW with 32 Ω Speaker
- Low Distortion (THD = 0.4% Typical)
- Wide Operating Supply Voltage (2.0 V to 16 V) — Allows Telephone Line Powered Applications.
- Low Quiescent Supply Current (2.5 mA Typical)
- Low Power-Down Quiescent Current (60 μA Typical)



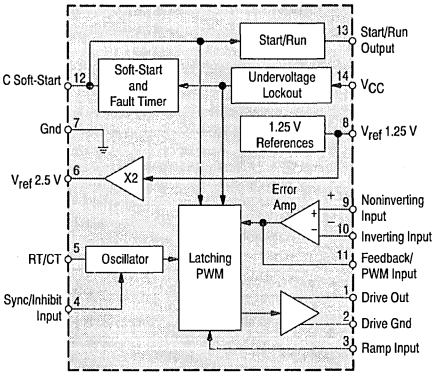
Current Mode Switching Regulator

MC34129P, D T_A = 0° to +70°C, Case 646, 751A
MC33129P, D T_A = 0° to +70°C, Case 646, 751A

High performance current mode switching regulator for low-power digital telephones. Unique internal fault timer provides automatic restart for overload recovery. A start/run comparator is included to implement bootstrapped operation of V_{CC}.

Although primarily intended for digital telephone systems, these devices can be used cost effectively in many other applications. On-chip functions and features include:

- Current Mode Operation to 300 kHz
- Automatic Feed Forward Compensation
- Latching PWM for Cycle-By-Cycle Current Limiting
- Latched-Off or Continuous Retry after Fault Timeout
- Soft-Start with Maximum Peak Switch Current Clamp
- Internally Trimmed 2% Bandgap Reference
- Input Undervoltage Lockout



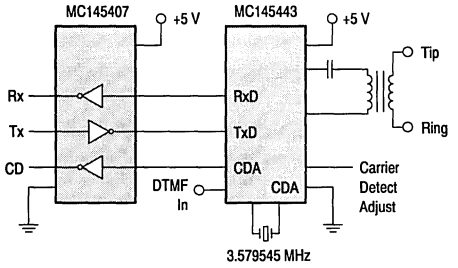
300 Baud FSK Modems

MC145442 Modem (CCITT V.21) Case 738, 751D
MC145443 Modem (Bell 103) Case 738, 751D

This powerful modem combines a complete FSK modulator/demodulator and an accompanying transmit/receive filter system on a single silicon chip. Designed for bidirectional transmission over the telephone network, the modem operates at 300 baud and can be obtained for compatibility with CCITT V.21 and Bell 103 specifications.

The modem contains an on-board carrier-detect circuit that allows direct operation on a telephone line (through a simple transformer), providing simplex, half-duplex, and full-duplex data communications. A built-in power amplifier is capable of driving –9.0 dBm onto a 600 Ω line in the transmit mode.

CMOS processing keeps power dissipation to a very low 45 mW, with a power-down dissipation of only 1.0 mW . . . from a single 5.0 V power supply. Available in a 20 pin dual-in-line P suffix, and a wide body surface mount DW suffix.



MC145444 (CCITT V.21) Case 804, 751D

This device includes the DTMF generator and call progress tone detector (CPTD) as well as the other circuitry needed for full-duplex, half-duplex, or simplex 300 baud data communication over a pair of telephone lines. It is intended for use with telemeter system or remote control system applications.

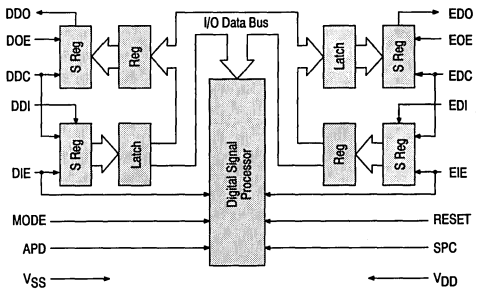
The differential line driver is capable of driving 0 dBm into a 600 Ω load. The transmit attenuator is programmable in 1 dB steps.

ADPCM Transcoder

MC145532 Case 620, 751G

The MC145532 Adaptive Differential Pulse Code Modulation (ADPCM) Transcoder provides a low cost, full-duplex, single-channel transcoder to (from) a 64 kbps PCM channel from (to) either a 16 kbps, 24 kbps, 32 kbps, or 64 kbps channel.

- Complies with CCITT Recommendation G.721 (Geneva 1986)
- Complies with the American National Standard (T1.301-1987)
- Full-Duplex, Single-Channel Operation
- Mu-Law or A-Law Coding is Pin Selectable
- Synchronous or Asynchronous Operation
- Easily Interfaces with any Member of Motorola's PCM Codec-Filter Mono-Circuit Family or Other Industry Standard Codecs
- Serial PCM and ADPCM Data Transfer Rate from 64 kbps to 5.12 Mbps
- Power Down Capability for Low Cost Consumption
- The Reset State is Automatically Initiated when the Reset Pin is Released.
- Simple Time Slot Assignment Timing for Transcoder Applications
- Single 5.0 V Power Supply
- Evaluation Kit MC145536 EVK Supports the MC145532 as well as the MC145480 PCM Codec-Filter. (See PBX Architecture Pages for More Information.)



Bit Rate Generators

MC14411 Case 709, 623

Internal (crystal controlled) 1.843 MHz oscillator and subsequent divider networks provide 16 different output clocks rates ranging from 75 Hz to 1.843 MHz for data communications equipment such as teleprinters, printers, CRT terminals and microprocessor systems.

MC145411 Case 648

Similar to the MC14411, this device utilizes a 1.843 MHz or 3.6864 MHz crystal frequency input divided to provide nine different output clock rates from 150 Hz to 1.843 MHz, or 300 Hz to 3.6864 MHz, respectively.

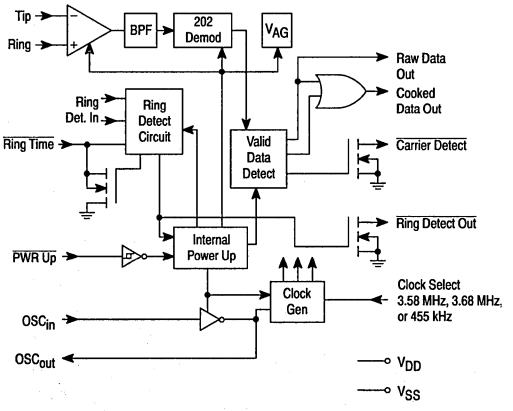
Calling Line Identification (CLID) Receiver with Ring Detector

MC145447 Case 648, 751G

The MC145447 is designed to demodulate Bell 202 1200 baud FSK asynchronous data. Its primary application is in products that will be used to receive and display the calling number, or the message waiting indicator sent to subscribers from participating central office facilities of the public switched network. The device also contains a carrier detect circuit and telephone ring detector which may be used to power up the device.

Applications include adjunct boxes, answering machines, feature phones, fax machines, and computer interface products.

- Ring Detector On-Chip
- Ring Detect Output for MCU Interrupt
- Power-Down Mode less than 1.0 µA
- Single Supply: 3.5 V to 6.0 V
- Pin Selectable Clock Frequencies: 3.68 MHz, 3.58 MHz, or 455 kHz
- Two-Stage Power-Up for Power Management Control

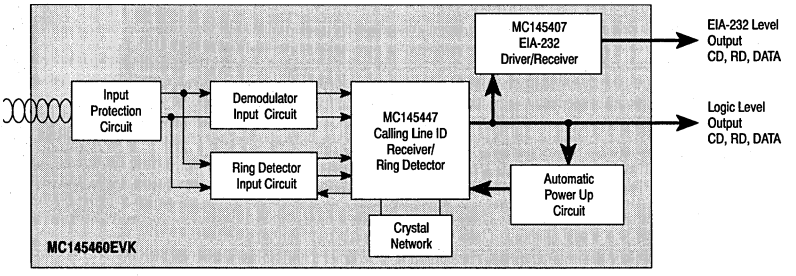


Calling Line ID Receiver

MC145460EVK Evaluation Kit

The MC145460EVK is a low cost evaluation platform for the MC145447. The MC145460EVK facilitates development and testing of products that support the Bellcore customer premises equipment (CPE) data interface, which enables services such as Calling Number Delivery (CND). The MC145447 can be easily incorporated into any telephone, FAX, PBX, key system, answering machine, CND adjunct box or other telephone equipment with the help of the MC145460EVK development kit.

- Easy Clip-On Access to Key MC145447 Signals
- Generous Prototype Area
- Configurable for MC145447 Automatic or External Power Up Control
- EIA-232 and Logic Level Ports for Connection to any PC or MCU Development Platform
- Carrier Detect, Ring Detect and Data Status LEDs
- Optional Tip and Ring Input Protection Network
- MC145460EVK User Guide, MC145447 Data Sheet, and additional MC145447 Sample included.



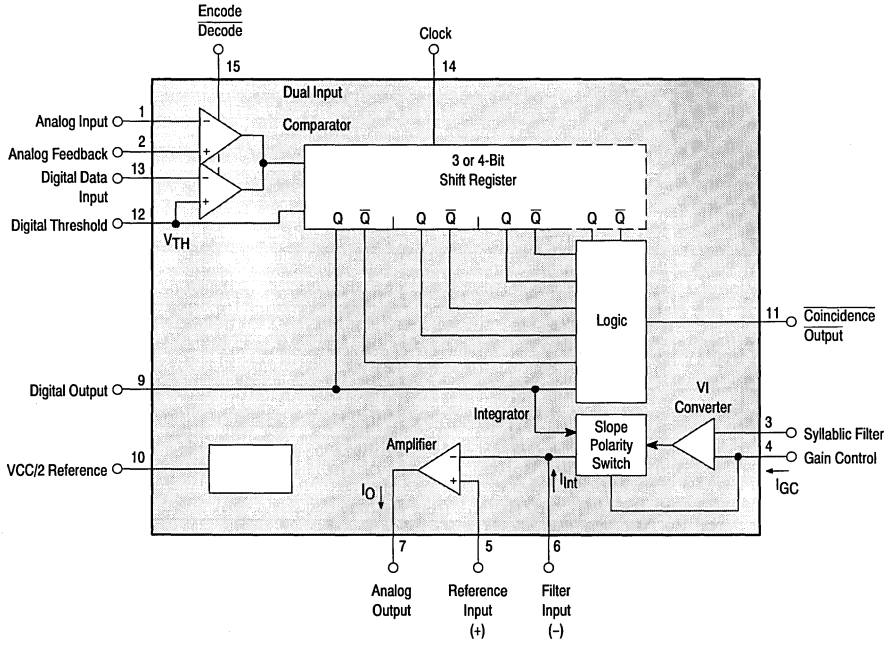
Continuously Variable Slope Delta (CVSD) Modulator/Demodulator

MC34115P T_A = 0° to +70°C, Case 648
MC3417/18L T_A = 0° to +70°C, Case 620
MC3517/18L T_A = −55° to +125°C, Case 620

Provides the A/D-D/A function of voice communications by digital transmission.

The MC3517/18 series of CVSDs is designed for military secure communications and commercial telephone applications. A single IC provides both encoding and decoding functions in a 16 pin package.

- Encode and Decode Functions on the same Chip with a Digital Input for Selection
- CMOS Compatible Digital Output
- Digital Input Threshold Selectable (V_{CC}/2 Reference provided On-Chip)
- MC3417/MC3517/MC34115 have a 3-Bit Algorithm (General Communications)
- MC3418/MC3518 have a 4-Bit Algorithm (Commercial Telephone)



8

Telecommunications

Summary of Bipolar Telecom Circuits

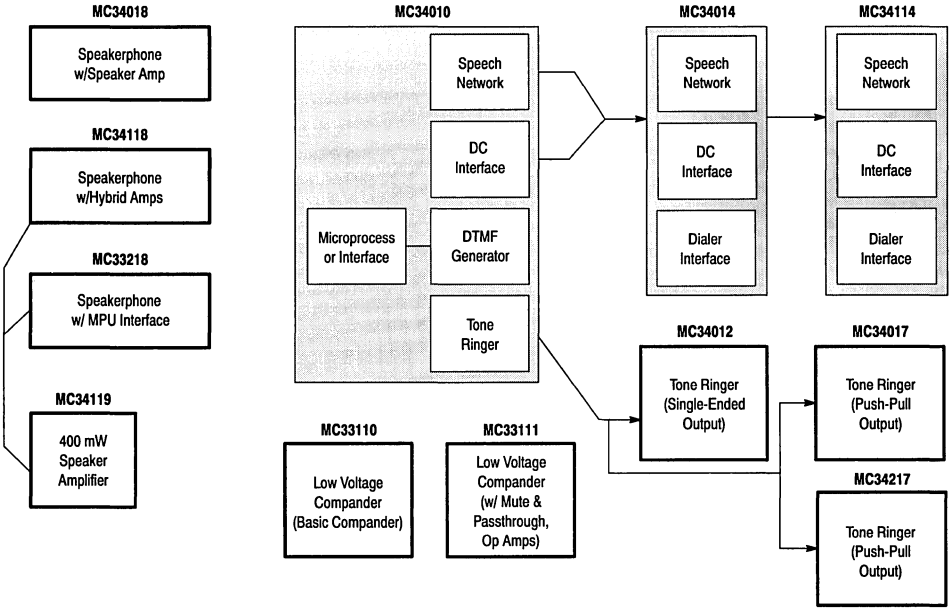
Function	Features	Suffix/ Case	Device
SLICs			
PBX Applications	All gains externally programmable, most BORSHT functions, current limit adjustable to 100 mA.	L726	MC3419-1
Central Office, Remote Terminals, PBX Applications	All gains externally programmable, most BORSHT functions, current limit adjustable to 50 mA, 58 dB Longitudinal Balance, –21.6 V to –42 V.	P/738 FN/776	MC33121
Central Office, Remote Terminals, PBX Applications	All gains externally programmable, most BORSHT functions, current limit adjustable to 50 mA, 58 dB Longitudinal Balance, –42 V to –58 V.	P/738 FN/776	MC33120
Central Office, Remote Terminals, PBX Applications	All gains externally programmable, most BORSHT functions, current limit adjustable to 50 mA, 58 dB Longitudinal Balance, –21.6 V to –58 V, ring trip, on-hook transmission, polarity reversal.	TBD(1)	MC33122
Complete Telephone Circuit			
POTS Circuit + MPU Dialing	Speech network, tone ringer, DC loop current interface, DTMF dialer with serial port control.	P/711 FN/777	MC34010
Tone Ringers			
Adjustable Tone Ringer	Single-ended output, meets FCC requirements, adjustable REN, different warble rates.	P/626 D751	MC34012-1, 2, 3
Adjustable Tone Ringer	Differential output, meets FCC requirements, adjustable REN, different warble rates.	P/626 D751	MC34017-1, 2, 3
Adjustable Tone Ringer	Differential output, meets FCC requirements, adjustable REN, single warble rates.	P/626 D751	MC34217
Speech Networks			
Basic Phone Line Interface	Loop current interface, speech network, line length compensation, speech/dialing modes, Bell System compliant.	P/707 DW/751D	MC34014
Basic Phone Line Interface	Loop current interface, speech network, line length compensation, speech/dialing modes, Bell System and foreign countries.	P/707 DW/751D	MC34114
Speakerphone Circuits			
Complete Speaker Phone with Speaker Amplifier	All level detection (2 pt.), attenuators, and switching controls, mike and speaker amp.	P/710 DW751F	MC34018
Complete Speaker Phone with Hybrid, Filter	All level detection (4 pt.), attenuators, and switching controls, mike amp with mute, hybrid, and filter.	P/710 DW751F	MC34118
Complete Speaker Phone with MPU Interface	All level detection, attenuators, and switching controls, mike amp, MPU interface for: volume control, mode selection, mike mute.	P/724 DW751E	MC33218
Audio Amplifiers			
1 Watt Audio Amp	1.0 W output power into 16 Ω, 35 V maximum.	D/751	MC13060
Low Voltage Audio Amp	400 mW, 8.0 Ω to 100 Ω, 2.0 V to 16 V, differential outputs, chip-disable input pin.	P/626 D751	MC34119
Companders			
Basic Compander	2.1 V to 7.0 V, no precision externals, 80 dB range, –40° to +85°C, independent compressor and expander.	P/646 D/751A	MC33110
Compander with Features	3.0 V to 7.0 V, no precision externals, 80 dB range, –40° to +85°C, independent compressor and expander, pass through and mute functions, two op amps.	P/648 D/751B	MC33111

(1) To Be Determined

Summary of Bipolar Telecom Circuits (continued)

Function	Features	Suffix/ Case	Device
Switching Regulator			
Current Mode Regulator	For phone line power applications, soft-start, current limiting, 2% accuracy.	P/646 D/751A	MC34129
Voice Encoder/Decoders			
Continuously Variable Slope Modulator/Demodulator (CVSD)	Telephone quality voice encoding/decoding, variable clock rate, 3-bit coding, for secure communications, voice storage/retrieval, answering machines, 0° to 70°C.	P/738 DW/751G	MC34115
	Same as above except 4-bit coding.	P/738 DW751G	MC3418
	Same as MC34115, –55° to 125°C temperature range.	L/620	MC3517
	Same as MC3418, –55° to 125°C temperature range.	L/620	MC3518

Motorola Family of Bipolar Handset Telecom Integrated Circuits



8

Phase-Locked Loop Components

Motorola offers a choice of phase-locked loop components ranging from complete functional frequency synthesizers for dedicated applications to a wide selection of general purpose PLL circuit elements. Technologies include CMOS for lowest power consumption and bipolar for high speed operation. Typical applications include TV, CATV, radios, scanners, cordless telephones plus home and personal computers.

PLL Frequency Synthesizers

Divider Programming Format	External Prescaler Modulus	Single-Ended (3-State) Phase Detector Output	Double-Ended Phase Detector Output	f_{max} (MHz)	Functional Supply Range (V)	Device	Suffix/ Case
Serial	Single	✓	✓	20	3.0 to 9.0	MC145155-2	P/707, DW/751D, FN/775
		✓	✓	20	3.0 to 9.0	MC145157-2	P/648, DW/751D, FN/775
	Dual	✓ ✓ (1)	—	15	3.0 to 9.0	MC145149	P/738, DW/751D
		✓	✓	20	3.0 to 9.0	MC145156-2	P/738, DW/751D, FN/775
		✓	✓	20	3.0 to 9.0	MC145158-2	P/648, DW/751D, FN/775
	Dual	Frequency Detector	Analog Detector	15	3.0 to 9.0	MC145159-1	P/738, DW/751D, FN/775
	Not Required	✓ ✓ (1)	—	60	2.5 to 5.5	MC145161	P/648, DW/751G
		✓ ✓ (1)	—	60	2.5 to 5.5	MC145167	P/648, DW/751G
		✓ ✓ (1)	—	60	2.5 to 5.5	MC145169	P/648, DW/751G
		✓	✓	160(2)	2.5 to 6.0	MC145170	P/648, D/751B
		✓	✓	1100	4.5 to 5.5	MC145191	F/751J
		✓	✓	1100	2.7 to 5.0	MC145192	F/751J
Parallel	Single	✓	—	4.0	4.5 to 12	MC145106	P/707, DW/751D, FN/775
		✓	✓	20	3.0 to 9.0	MC145151-2	P/710, FN/776, DW/751F
	Dual	—	✓	20	3.0 to 9.0	MC145152-2	P/710, FN/776, DW/751F
	Not Required	✓ ✓ (1)	—	60	2.5 to 5.5	MC145160	P/707, DW/751D
		✓ ✓ (1)		60	2.5 to 5.5	MC145166	P/648, DW/751G
		✓ ✓ (1)		60	2.5 to 5.5	MC145168	P/648, DW/751G
4-Bit Bus	Single	✓	✓	20	3.0 to 9.0	MC145145-2	P/707, DW/751D
	Dual	✓	✓	20	3.0 to 9.0	MC145146-2	P/738, DW/751D

(1) Accommodates two loops per package.
(2) 180 MHz version available, see data sheet.

Intended Applications

General Purpose	Cordless Phones
MC145106	MC145160
MC145145-2	MC145161
MC145146-2	MC145166
MC145149	MC145167
MC145151-2	MC145168
MC145152-2	MC145169
MC145155-2	
MC145156-2	
MC145157-2	
MC145158-2	
MC145159-1	
MC145170	
MC145191	
MC145192	

Additional Phase-Locked Loop Functions

Function	Family	Devices (0° to 70°C)	Suffix/Case
Oscillators			
Crystal Oscillator	MECL	MC12061	P/648, L/620
Voltage-Controller Oscillator	MECL	MC1648(3)	P/646, L/632, F/607
Voltage-Controlled Multivibrator	MECL	MC1658(3)	P/648, L/620
Dual Voltage-Controlled Multivibrator	TTL	MC4024/ MC4324(1)	P/648, L/632, F/607
Voltage-Controller Oscillators	TTL/LS	SN74LS724	P.626, L/693
Phase Detectors			
Digital Mixer	MECL	MC12000	P/646, L/632
Phase-Frequency Detector	MECL	MC12040	
Phase-Frequency Detector	TTL	MC4044 MC4344(1)	P/646, L/632, F/607
Analog Mixer, Double Balanced	MECL	MC12002(3)	P/646, L/632
Modulator/Demodulator	Linear	MC1496(2)/ MC1596(1)	P/646, L/632
Control Functions			
Counter-Control Logic	MECL	MC12014	P/648, L/620
Prescalers/Counters			
UHF — 2,500 MHz	MECL	MC1690(3)	F/650, L/620
2-Modulus ÷ 5/ ÷ 6, 600 MHz	MECL	MC12009(3)	P/648, L/620
2-Modulus ÷ 8/ ÷ 9, 600 MHz	MECL	MC12011(3)	
2-Modulus ÷ 10/ ÷ 11, 600 MHz	MECL	MC12013(3)	
Low Power 2-Modulus ÷ 32/ ÷ 33, 225 MHz	MECL	MC12015(4)	P/626, D/751
Low Power 2-Modulus ÷ 40/ ÷ 41, 225 MHz	MECL	MC12016(4)	
Low Power 2-Modulus ÷ 64/ ÷ 65, 225 MHz	MECL	MC12017(4)	
Low Power 2-Modulus ÷ 128/ ÷ 129, 520 MHz	MECL	MC12018(4)	
Low Power 2-Modulus ÷ 20/ ÷ 21, 225 MHz	MECL	MC12019(4)	
Low Power 2-Modulus ÷ 64/ ÷ 65, ÷ 128/ ÷ 129 Pos. Edge 1.1 GHz	MECL	MC12022A(4)	
Low Power 2-Modulus ÷ 64/ ÷ 65, ÷ 128/ ÷ 129 Neg. Edge 1.1 GHz	MECL	MC12022B(4)	
Low Power ÷ 64 Prescaler, 225 MHz 3.2 to 5.5 V_{CC}	MECL	MC12023	
Low Power ÷ 64 Prescaler, 1.1 GHz	MECL	MC12073	
Low Power ÷ 256 Prescaler, 1.1 GHz	MECL	MC12074	
UHF ÷ 2 Prescaler, 750 MHz	MECL	MC12090	P/648, L/620, F/650
Programmable ÷ N Decade	TTL	MC4316/ MC4316(1)	P/648, L/620, F/650

(1)T_A = −55° to +125°C (3)T_A = −30° to +85°C
(2)T_A = 0° to 70°C (4)T_A = −40° to +85°C
Plastic packages available for commercial temperature range only.
NOTE: For more information see SG366/D

RF Communications

Telecommunications

8

*See *Telecommunications Device Data* (DL136)

RELATED APPLICATION NOTES

App Note	Title	Related Device
AN531	MC1596 Balanced Modulator	**MC1596**
AN933	A Variety of Usese for the MC34012/MC34017 Tone Ringers	**MC34012-1,-2,-3 MC34017**
AN937	A Telephone Ringer which Complies with FCC and EIA Impedance Standards	**MC34012, MC34017**
AN957	Interfacing the Speakerphone to the MC34010/11/13 Speech Networks	**MC34010, MC34011A**
AN958	Transmit Gain Adjustments for the MC34014 Speech Network	**MC34014**
AN959	A Speakerphone with Receive Idle Mode	**MC34018**
AN960	Equalization of DTMF Signals Using the MC34014	**MC34014**
AN976	A New High Performance Current Mode Controller Teams Up with Current Sensing Power MOSFETs	**MC34129**
AN980	Low Power FM Dual Conversion Receivers	**MC3362, MC3363**
AN1002	A Handsfree Featurephone Design Using the MC34114 Speech Network and the MC34018 Speakerphone ICs	**MC34018 MC34114**
AN1003	A Featurephone Design, with Tone Ringer and Dialer, Using the MC34118 Speakerphone IC	**MC34118, MC34017, MC145412, MC34119**
AN1004	A Handsfree Featurephone Design Using the MC34114 Speech Network and the MC34118 Speakerphone ICs	**MC34114, MC34118, MC34119, MC3417, MC145412**
AN1006	Linearize the Volume Control of the MC34118 Speakerphone	**MC34118**
AN1077	Adding Digital Volume Control to Speakerphone Circuits	**MC34018, MC34118**
AN1081	Minimize the "Pop" in the MC34119 Power Audio Amplifiers	**MC34119**
AN1510	A Mode Indicator for the MC34118 Speakerphone Circuit	**MC34118**
DL136	Telecommunications Device Data	
SG98	Linear Telecom Cross Reference	

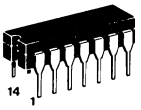
MC1496
MC1596

BALANCED MODULATOR/DEMODULATOR

BALANCED MODULATOR/ DEMODULATOR

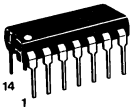
These devices were designed for use where the output voltage is a product of an input voltage (signal) and a switching function (carrier). Typical applications include suppressed carrier and amplitude modulation, synchronous detection, FM detection, phase detection, and chopper applications. See Motorola Application Note AN531 for additional design information.

- Excellent Carrier Suppression — 65 dB typ @ 0.5 MHz
  — 50 dB typ @ 10 MHz
- Adjustable Gain and Signal Handling
- Balanced Inputs and Outputs
- High Common Mode Rejection – 85 dB typ



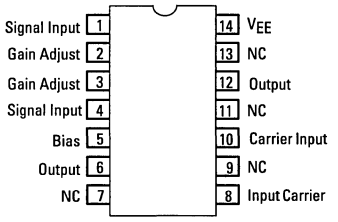
L SUFFIX
CERAMIC PACKAGE
CASE 632

D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO-14)



P SUFFIX
PLASTIC PACKAGE
CASE 646

PIN ASSIGNMENTS



ORDERING INFORMATION

Device	Temperature Range	Package
MC1496D	0°C to +70°C	SO-14
MC1496L		Ceramic DIP
MC1496P		Plastic DIP
MC1596L	–55°C to +125°C	Ceramic DIP

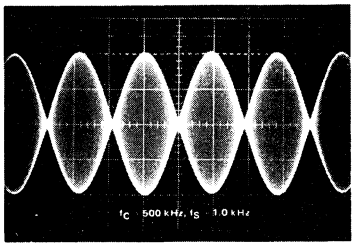


FIGURE 1 – SUPPRESSED CARRIER OUTPUT WAVEFORM

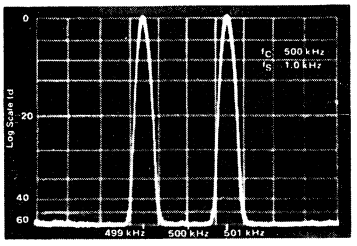


FIGURE 2 – SUPPRESSED CARRIER SPECTRUM

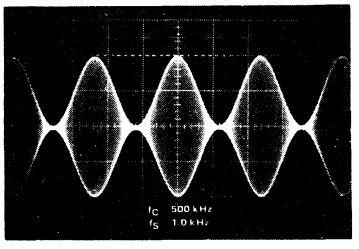
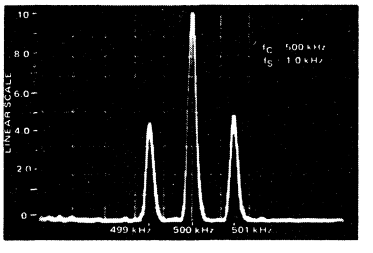


FIGURE 3 – AMPLITUDE MODULATION OUTPUT WAVEFORM

FIGURE 4 – AMPLITUDE-MODULATION SPECTRUM



MAXIMUM RATINGS* (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Applied Voltage ($V_6 - V_8$, $V_{10} - V_1$, $V_{12} - V_8$, $V_{12} - V_{10}$, $V_8 - V_4$, $V_8 - V_1$, $V_{10} - V_4$, $V_6 - V_{10}$, $V_2 - V_5$, $V_3 - V_5$)	ΔV	30	Vdc
Differential Input Signal	$V_8 - V_{10}$ $V_4 - V_1$	+5.0 ±(5+I_5R_e)	Vdc
Maximum Bias Current	I_5	10	mA
Thermal Resistance, Junction to Air Ceramic Dual In-Line Package Plastic Dual In-Line Package Metal Package	$R_{\theta JA}$	 100 100 160	°C/W
Operating Temperature Range MC1496 MC1596	T_A	 0 to +70 −55 to +125	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = +12 Vdc, V_{EE} = −8.0 Vdc, I_5 = 1.0 mAdc, R_L = 3.9 kΩ, R_e = 1.0 kΩ, T_A = +25°C, all input and output characteristics are single-ended, unless otherwise noted.)

Characteristic	Fig.	Note	Symbol	MC1596 Min	MC1596 Typ	MC1596 Max	MC1496 Min	MC1496 Typ	MC1496 Max	Unit
Carrier Feedthrough	5	1	V_{CFT}							μV(rms)
V_C = 60 mV(rms) sine wave and f_C = 1.0 kHz				—	40	—	—	40	—	
offset adjusted to zero f_C = 10 MHz				—	140	—	—	140	—	
V_C = 300 mVp-p square wave:										mV(rms)
offset adjusted to zero f_C = 1.0 kHz				—	0.04	0.2	—	0.04	0.4	
offset not adjusted f_C = 1.0 kHz				—	20	100	—	20	200	
Carrier Suppression	5	2	V_{CS}							dB
f_S = 10 kHz, 300 mV(rms)										
f_C = 500 kHz, 60 mV(rms) sine wave				50	65	—	40	65	—	
f_C = 10 MHz, 60 mV(rms) sine wave				—	50	—	—	50	—	k
Transadmittance Bandwidth (Magnitude) (R_L = 50 ohms)	8	8	BW_{3dB}							MHz
Carrier Input Port, V_C = 60 mV(rms) sine wave				—	300	—	—	300	—	
f_S = 1.0 kHz, 300 mV(rms) sine wave										
Signal Input Port, V_S = 300 mV(rms) sine wave				—	80	—	—	80	—	
$\|V_C\|$ = 0.5 Vdc										
Signal Gain	10	3	A_{VS}	2.5	3.5	—	2.5	3.5	—	V/V
V_S = 100 mV(rms), f = 1.0 kHz; $\|V_C\|$ = 0.5 Vdc										
Single-Ended Input Impedance, Signal Port, f = 5.0 MHz	6	—								
Parallel Input Resistance			r_{ip}	—	200	—	—	200	—	kΩ
Parallel Input Capacitance			c_{ip}	—	2.0	—	—	2.0	—	pF
Single-Ended Output Impedance, f = 10 MHz	6	—								
Parallel Output Resistance			r_{op}	—	40	—	—	40	—	kΩ
Parallel Output Capacitance			c_{oo}	—	5.0	—	—	5.0	—	pF
Input Bias Current	7	—								μA
$I_{bS} = \frac{I_1 + I_4}{2}$; $I_{bC} = \frac{I_8 + I_{10}}{2}$			I_{bS} I_{bC}	— —	12 12	25 25	— —	12 12	30 30	
Input Offset Current	7	—								μA
$I_{ioS} = I_1 - I_4$; $I_{ioC} = I_8 - I_{10}$			$\|I_{ioS}\|$ $\|I_{ioC}\|$	— —	0.7 0.7	5.0 5.0	— —	0.7 0.7	7.0 7.0	
Average Temperature Coefficient of Input Offset Current (T_A = −55°C to +125°C)	7	—	$\|TC_{Iio}\|$	—	2.0	—	—	2.0	—	nA/°C
Output Offset Current ($I_6 - I_9$)	7	—	$\|I_{oo}\|$	—	14	50	—	14	80	μA
Average Temperature Coefficient of Output Offset Current (T_A = −55°C to +125°C)	7	—	$\|TC_{Ioo}\|$	—	90	—	—	90	—	nA/°C
Common-Mode Input Swing, Signal Port, f_S = 1.0 kHz	9	4	CMV	—	5.0	—	—	5.0	—	Vp-p
Common-Mode Gain, Signal Port, f_S = 1.0 kHz, $\|V_C\|$ = 0.5 Vdc	9	—	ACM	—	−85	—	—	−85	—	dB
Common-Mode Quiescent Output Voltage (Pin 6 or Pin 9)	10	—	V_{out}	—	8.0	—	—	8.0	—	Vp-p
Differential Output Voltage Swing Capability	10	—	V_{out}	—	8.0	—	—	8.0	—	Vp-p
Power Supply Current	7	6								mAdc
$I_6 + I_{12}$			I_{CC}	—	2.0	3.0	—	2.0	4.0	
I_{14}			I_{EE}	—	3.0	4.0	—	3.0	5.0	
DC Power Dissipation	7	5	P_D	—	33	—	—	33	—	mW

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GENERAL OPERATING INFORMATION

Carrier Feedthrough

Carrier feedthrough is defined as the output voltage at carrier frequency with only the carrier applied (signal voltage = 0).

Carrier null is achieved by balancing the currents in the differential amplifier by means of a bias trim potentiometer (R_1 of Figure 5).

Carrier Suppression

Carrier suppression is defined as the ratio of each sideband output to carrier output for the carrier and signal voltage levels specified.

Carrier suppression is very dependent on carrier input level, as shown in Figure 22. A low value of the carrier does not fully switch the upper switching devices, and results in lower signal gain, hence lower carrier suppression. A higher than optimum carrier level results in unnecessary device and circuit carrier feedthrough, which again degenerates the suppression figure. The MC1596 has been characterized with a 60 mV(rms) sinewave carrier input signal. This level provides optimum carrier suppression at carrier frequencies in the vicinity of 500 kHz, and is generally recommended for balanced modulator applications.

Carrier feedthrough is independent of signal level, V_S. Thus carrier suppression can be maximized by operating with large signal levels. However, a linear operating mode must be maintained in the signal-input transistor pair — or harmonics of the modulating signal will be generated and appear in the device output as spurious sidebands of the suppressed carrier. This requirement places an upper limit on input-signal amplitude (see Figure 20). Note also that an optimum carrier level is recommended in Figure 22 for good carrier suppression and minimum spurious sideband generation.

At higher frequencies circuit layout is very important in order to minimize carrier feedthrough. Shielding may be necessary in order to prevent capacitive coupling between the carrier input leads and the output leads.

Signal Gain and Maximum Input Level

Signal gain (single-ended) at low frequencies is defined as the voltage gain,

$$A_{VS} = \frac{V_o}{V_S} = \frac{R_L}{R_e + 2r_e} \text{ where } r_e = \frac{26\text{ mV}}{I_5\text{ (mA)}}$$

A constant dc potential is applied to the carrier input terminals to fully switch two of the upper transistors "on" and two transistors "off" (V_C = 0.5 Vdc). This in effect forms a cascode differential amplifier.

Linear operation requires that the signal input be below a critical value determined by R_E and the bias current I_5.

$$V_S \leq I_5 R_E \text{ (Volts peak)}$$

Note that in the test circuit of Figure 10, V_S corresponds to a maximum value of 1 volt peak.

Common Mode Swing

The common-mode swing is the voltage which may be applied to both bases of the signal differential amplifier, without saturating the current sources or without saturating the differential amplifier itself by swinging it into the upper switching devices. This swing is variable depending on the particular circuit and biasing conditions chosen.

Power Dissipation

Power dissipation, P_D, within the integrated circuit package should be calculated as the summation of the voltage-current products at each port, i.e. assuming $V_{12} = V_6$, $I_5 = I_6 = I_{12}$ and ignoring base current, $P_D = 2\,I_5\,(V_6 - V_{14}) + I_5)\,V_5 - V_{14}$ where subscripts refer to pin numbers.

Design Equations

The following is a partial list of design equations needed to operate the circuit with other supply voltages and input conditions.

A. Operating Current

The internal bias currents are set by the conditions at pin 5. Assume:

$$I_5 = I_6 = I_{12},$$

$$I_B << I_C \text{ for all transistors}$$

then:

$$R_5 = \frac{V - -\phi}{I_5} - 500\ \Omega$$

where: R_5 is the resistor between pin 5 and ground

ϕ = 0.75 V at T_A = +25°C

The MC1596 has been characterized for the condition I_5 = 1.0 mA and is the generally recommended value.

B. Common-Mode Quiescent Output Voltage

$$V_6 = V_{12} = V^+ - I_5 R_L$$

Biasing

The MC1596 requires three dc bias voltage levels which must be set externally. Guidelines for setting up these three levels include maintaining at least 2 volts collector-base bias on all transistors while not exceeding the voltages given in the absolute maximum rating table;

$$30\text{ Vdc} \geq [(V_6, V_{12}) - (V_8, V_{10})] \geq 2\text{ Vdc}$$

$$30\text{ Vdc} \geq [(V_8, V_{10}) - (V_1, V_4)] \geq 2.7\text{ Vdc}$$

$$30\text{ Vdc} \geq [(V_1, V_4) - (V_5)] \geq 2.7\text{ Vdc}$$

The foregoing conditions are based on the following approximations:

$$V_6 = V_{12},\ V_8 = V_{10},\ V_1 = V_4$$

Bias currents flowing into pins 1, 4, 8, and 10 are transistor base currents and can normally be neglected if external bias dividers are designed to carry 1.0 mA or more.

Transadmittance Bandwidth

Carrier transadmittance bandwidth is the 3 dB bandwidth of the device forward transadmittance as defined by:

$$\gamma_{21C} = \left.\frac{i_o\text{ (each sideband)}}{v_s\text{ (signal)}}\right| V_o = 0$$

Signal transadmittance bandwidth is the 3 dB bandwidth of the device forward transadmittance as defined by:

$$\gamma_{21S} = \left.\frac{i_o\text{ (signal)}}{v_s\text{ (signal)}}\right| V_c = 0.5\text{ Vdc},\ V_o = 0$$

Coupling and Bypass Capacitors

Capacitors C_1 and C_2 (Figure 5) should be selected for a reactance of less than 5.0 Ω at the carrier frequency.

Output Signal

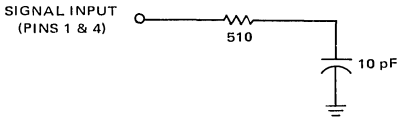
The output signal is taken from Pins 6 and 12 either balanced or single-ended. Figure 11 shows the output levels of each of the two output sidebands resulting from variations in both the carrier and modulating signal inputs with a single-ended output connection.

Negative Supply

V_{EE} should be dc only. The insertion of an RF choke in series with V_{EE} can enhance the stability of the internal current sources.

Signal Port Stability

Under certain values of driving source impedance, oscillation may occur. In this event, an RC suppression network should be connected directly to each input using short leads. This will reduce the Q of the source-tuned circuits that cause the oscillation.



An alternate method for low-frequency applications is to insert a 1.0 kΩ resistor in series with the input (Pins 1, 4). In this case input current drift may cause serious degradation of carrier suppression.

TEST CIRCUITS

FIGURE 5 – CARRIER REJECTION AND SUPPRESSION

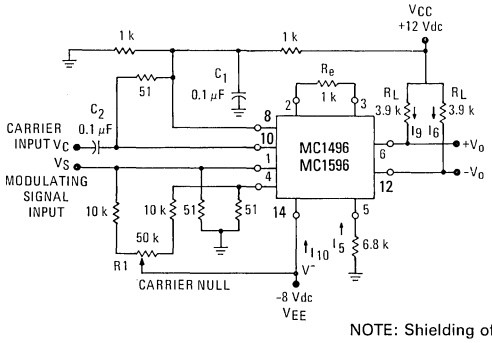
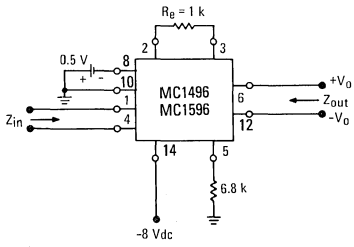


FIGURE 6 – INPUT-OUTPUT IMPEDANCE



NOTE: Shielding of input and output leads may be needed to properly perform these tests.

FIGURE 7 – BIAS AND OFFSET CURRENTS

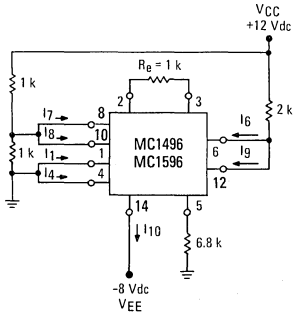


FIGURE 8 – TRANSCONDUCTANCE BANDWIDTH

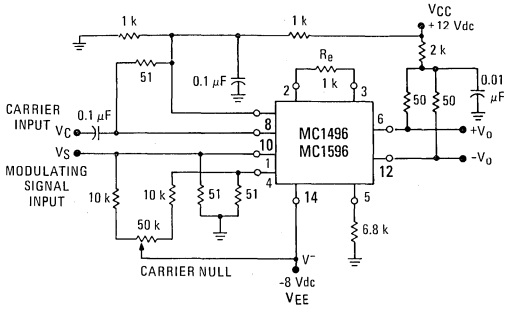


FIGURE 9 – COMMON MODE GAIN

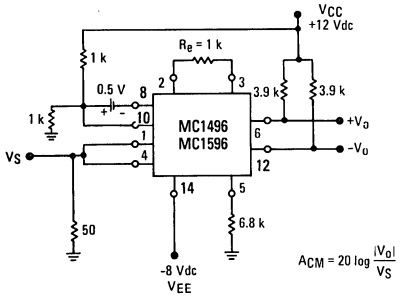
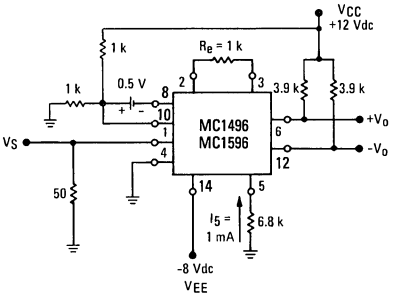


FIGURE 10 – SIGNAL GAIN AND OUTPUT SWING



TYPICAL CHARACTERISTICS

Typical characteristics were obtained with circuit shown in Figure 5, f_C = 500 kHz (sine wave), V_C = 60 mV(rms), f_S = 1 kHz, V_S = 300 mV(rms), T_A = +25°C unless otherwise noted.

FIGURE 11 – SIDEBAND OUTPUT versus CARRIER LEVELS

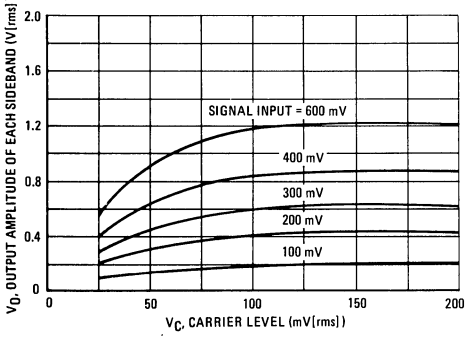


FIGURE 12 – SIGNAL-PORT PARALLEL-EQUIVALENT INPUT RESISTANCE versus FREQUENCY

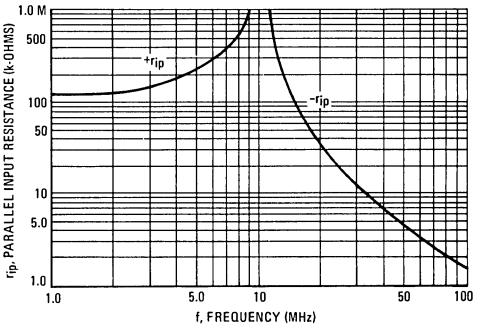


FIGURE 13 – SIGNAL-PORT PARALLEL-EQUIVALENT INPUT CAPACITANCE versus FREQUENCY

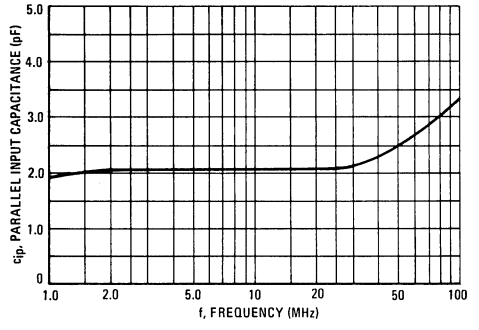
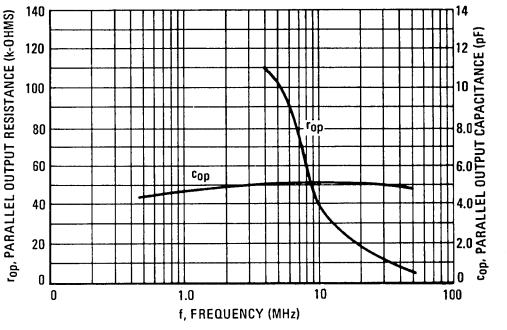


FIGURE 14 – SINGLE-ENDED OUTPUT IMPEDANCE versus FREQUENCY



TYPICAL CHARACTERISTICS (continued)

Typical characteristics were obtained with circuit shown in Figure 5, f_C = 500 kHz (sine wave), V_C = 60 mV(rms), f_S = 1 kHz, V_S = 300 mV(rms), T_A = +25°C unless otherwise noted.

FIGURE 15 – SIDEBAND AND SIGNAL PORT TRANSADMITTANCES versus FREQUENCY

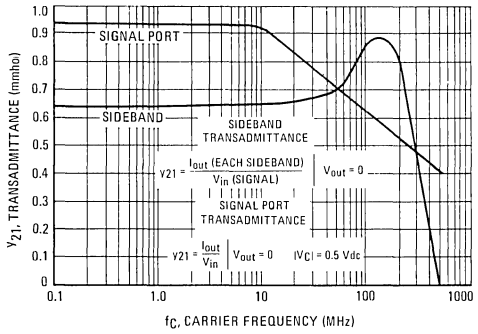


FIGURE 16 – CARRIER SUPPRESSION versus TEMPERATURE

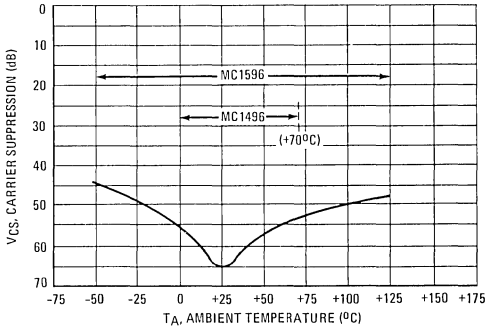


FIGURE 17 – SIGNAL-PORT FREQUENCY RESPONSE

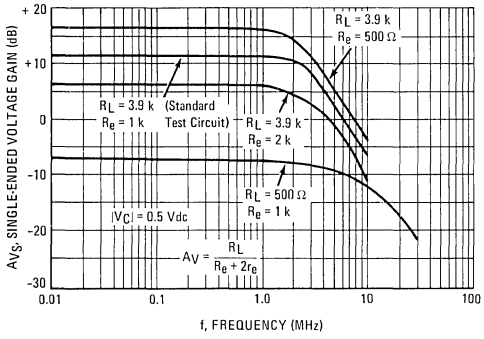


FIGURE 18 – CARRIER SUPPRESSION versus FREQUENCY

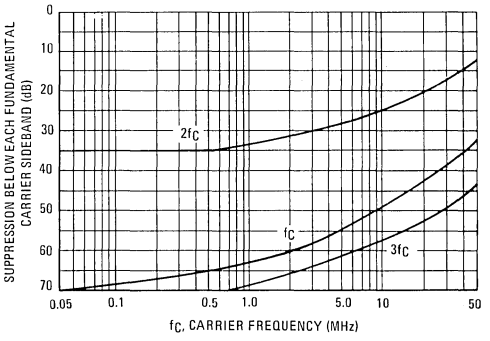


FIGURE 19 – CARRIER FEEDTHROUGH versus FREQUENCY

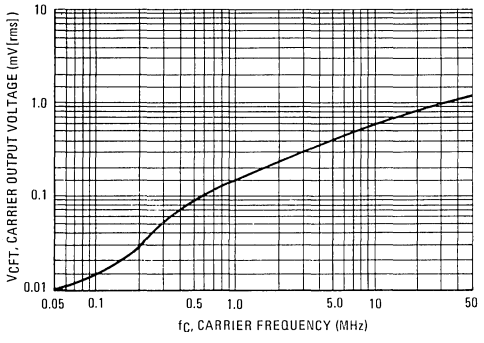


FIGURE 20 – SIDEBAND HARMONIC SUPPRESSION versus INPUT SIGNAL LEVEL

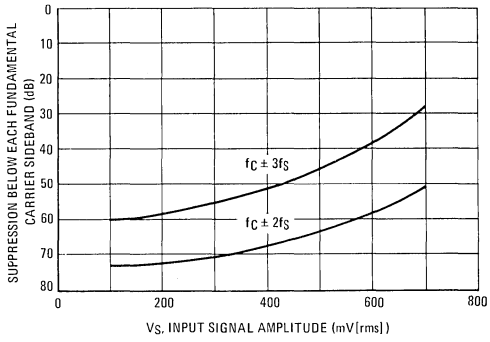


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FIGURE 21 – SUPPRESSION OF CARRIER HARMONIC SIDEBANDS versus CARRIER FREQUENCY

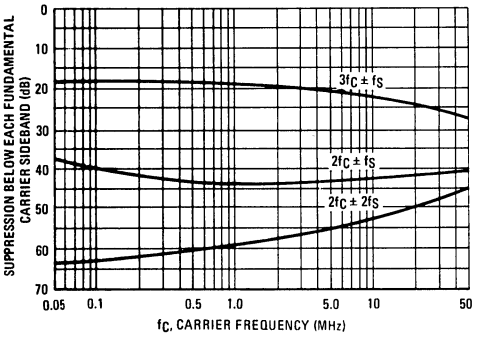
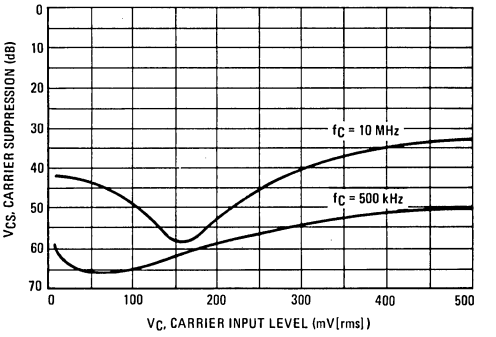


FIGURE 22 – CARRIER SUPPRESSION versus CARRIER INPUT LEVEL



OPERATIONS INFORMATION

The MC1596/MC1496, a monolithic balanced modulator circuit, is shown in Figure 23.

This circuit consists of an upper quad differential amplifier driven by a standard differential amplifier with dual current sources. The output collectors are cross-coupled so that full-wave balanced multiplication of the two input voltages occurs. That is, the output signal is a constant times the product of the two input signals.

Mathematical analysis of linear ac signal multiplication indicates that the output spectrum will consist of only the sum and difference of the two input frequencies. Thus, the device may be used as a balanced modulator, doubly balanced mixer, product detector, frequency doubler, and other applications requiring these particular output signal characteristics.

The lower differential amplifier has its emitters connected to the package pins so that an external emitter resistance may be used. Also, external load resistors are employed at the device output.

FIGURE 23 – CIRCUIT SCHEMATIC

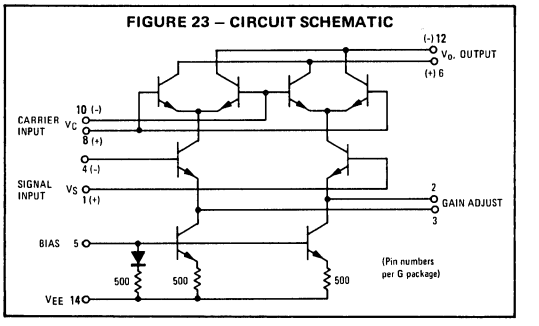
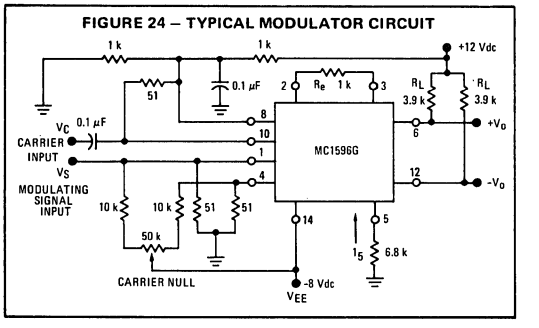


FIGURE 24 – TYPICAL MODULATOR CIRCUIT



Signal Levels

The upper quad differential amplifier may be operated either in a linear or a saturated mode. The lower differential amplifier is operated in a linear mode for most applications.

For low-level operation at both input ports, the output signal will contain sum and difference frequency components and have an amplitude which is a function of the product of the input signal amplitudes.

For high-level operation at the carrier input port and linear operation at the modulating signal port, the output signal will contain sum and difference frequency components of the modulating signal frequency and the fundamental and odd harmonics of the carrier frequency. The output amplitude will be a constant times the modulating signal amplitude. Any amplitude variations in the carrier signal will not appear in the output.

The linear signal handling capabilities of a differential amplifier are well defined. With no emitter degeneration, the maximum input voltage for linear operation is approximately 25 mV peak. Since the upper differential amplifier has its emitters internally connected, this voltage applies to the carrier input port for all conditions.

Since the lower differential amplifier has provisions for an external emitter resistance, its linear signal handling range may be adjusted by the user. The maximum input voltage for linear operation may be approximated from the following expression:

$$V = (I_5)(R_E) \text{ volts peak.}$$

This expression may be used to compute the minimum value of R_E for a given input voltage amplitude.

FIGURE 25 – TABLE 1
VOLTAGE GAIN AND OUTPUT FREQUENCIES

Carrier Input Signal (V_C)	Approximate Voltage Gain	Output Signal Frequency(s)
Low-level dc	$\frac{R_L V_C}{2(R_E + 2r_e)\left(\frac{KT}{q}\right)}$	f_M
High-level dc	$\frac{R_L}{R_E + 2r_e}$	f_M
Low-level ac	$\frac{R_L V_C(rms)}{2\sqrt{2}\left(\frac{KT}{q}\right)(R_E + 2r_e)}$	$f_C \pm f_M$
High-level ac	$\frac{0.637\, R_L}{R_E + 2r_e}$	$f_C \pm f_M$, $3f_C \pm f_M$, $5f_C \pm f_M$, . . .

The gain from the modulating signal input port to the output is the MC1596/MC1496 gain parameter which is most often of interest to the designer. This gain has significance only when the lower differential amplifier is operated in a linear mode, but this includes most applications of the device.

As previously mentioned, the upper quad differential amplifier may be operated either in a linear or a saturated mode. Approximate gain expressions have been developed for the MC1596/MC1496 for a low-level modulating signal input and the following carrier input conditions:

1) Low-level dc
2) High-level dc
3) Low-level ac
4) High-level ac

These gains are summarized in Table 1, along with the frequency components contained in the output signal.

NOTES:
1. Low-level Modulating Signal, V_M, assumed in all cases. V_C is Carrier Input Voltage.
2. When the output signal contains multiple frequencies, the gain expression given is for the output amplitude of each of the two desired outputs, $f_C + f_M$ and $f_C - f_M$.
3. All gain expressions are for a single-ended output. For a differential output connection, multiply each expression by two.
4. R_L = Load resistance.
5. R_E = Emitter resistance between pins 2 and 3.
6. r_e = Transistor dynamic emitter resistance, at +25°C;

$$r_e \approx \frac{26 \text{ mV}}{I_5 \text{ (mA)}}$$

7. K = Boltzmann's Constant, T = temperature in degrees Kelvin, q = the charge on an electron.

$$\frac{KT}{q} \approx 26 \text{ mV at room temperature}$$

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APPLICATIONS INFORMATION

Double sideband suppressed carrier modulation is the basic application of the MC1596/MC1496. The suggested circuit for this application is shown on the front page of this data sheet.

In some applications, it may be necessary to operate the MC1596/MC1496 with a single dc supply voltage instead of dual supplies. Figure 26 shows a balanced modulator designed for operation with a single +12 Vdc supply. Performance of this circuit is similar to that of the dual supply modulator.

AM Modulator

The circuit shown in Figure 27 may be used as an amplitude modulator with a minor modification.

All that is required to shift from suppressed carrier to AM operation is to adjust the carrier null potentiometer for the proper amount of carrier insertion in the output signal.

However, the suppressed carrier null circuitry as shown in Figure 27 does not have sufficient adjustment range. Therefore, the modulator may be modified for AM operation by changing two resistor values in the null circuit as shown in Figure 28.

Product Detector

The MC1596/MC1496 makes an excellent SSB product detector (see Figure 29).

This product detector has a sensitivity of 3.0 microvolts and a dynamic range of 90 dB when operating at an intermediate frequency of 9 MHz.

The detector is broadband for the entire high frequency range. For operation at very low intermediate frequencies down to 50 kHz the 0.1 μF capacitors on pins 8 and 10 should be increased to 1.0 μF. Also, the output filter at pin 12 can be tailored to a specific intermediate frequency and audio amplifier input impedance.

As in all applications of the MC1596/MC1496, the emitter resistance between pins 2 and 3 may be increased or decreased to adjust circuit gain, sensitivity, and dynamic range.

This circuit may also be used as an AM detector by introducing carrier signal at the carrier input and an AM signal at the SSB input.

The carrier signal may be derived from the intermediate frequency signal or generated locally. The carrier signal may be introduced with or without modulation, provided its level is sufficiently high to saturate the upper quad differential amplifier. If the carrier signal is modulated, a 300 mV(rms) input level is recommended.

Doubly Balanced Mixer

The MC1596/MC1496 may be used as a doubly balanced mixer with either broadband or tuned narrow band input and output networks.

The local oscillator signal is introduced at the carrier input port with a recommended amplitude of 100 mV(rms).

Figure 30 shows a mixer with a broadband input and a tuned output.

Frequency Doubler

The MC1596/MC1496 will operate as a frequency doubler by introducing the same frequency at both input ports.

Figures 31 and 32 show a broadband frequency doubler and a tuned output very high frequency (VHF) doubler, respectively.

Phase Detection and FM Detection

The MC1596/MC1496 will function as a phase detector. High-level input signals are introduced at both inputs. When both inputs are at the same frequency the MC1596/MC1496 will deliver an output which is a function of the phase difference between the two input signals.

An FM detector may be constructed by using the phase detector principle. A tuned circuit is added at one of the inputs to cause the two input signals to vary in phase as a function of frequency. The MC1596/MC1496 will then provide an output which is a function of the input signal frequency.

TYPICAL APPLICATIONS

FIGURE 26 – BALANCED MODULATOR
(+12 Vdc SINGLE SUPPLY)

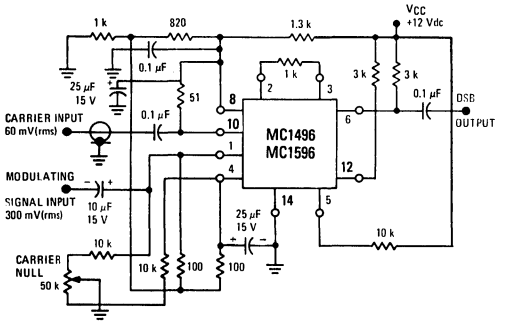


FIGURE 27 – BALANCED MODULATOR-DEMODULATOR

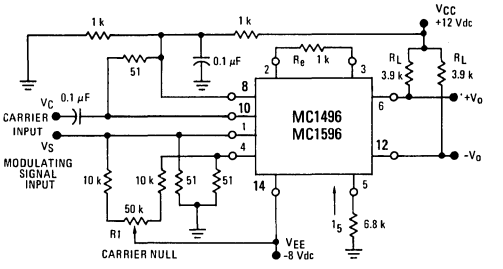


FIGURE 28 – AM MODULATOR CIRCUIT

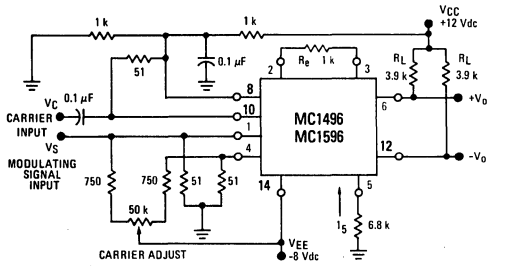


FIGURE 29 – PRODUCT DETECTOR
(+12 Vdc SINGLE SUPPLY)

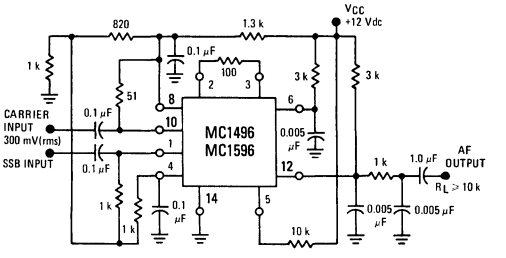
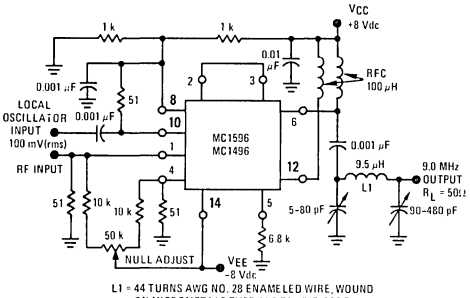


FIGURE 30 – DOUBLY BALANCED MIXER
(BROADBAND INPUTS, 9.0 MHz TUNED OUTPUT)



L1 = 44 TURNS AWG NO. 28 ENAMELED WIRE, WOUND ON MICROMETALS TYPE 44-6 TOROID CORE.

FIGURE 31 – LOW-FREQUENCY DOUBLER

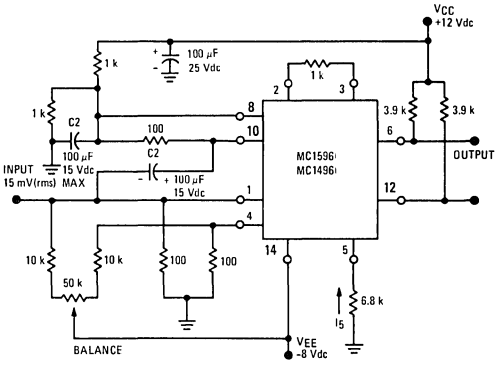
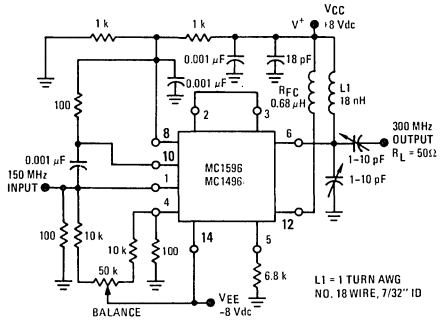
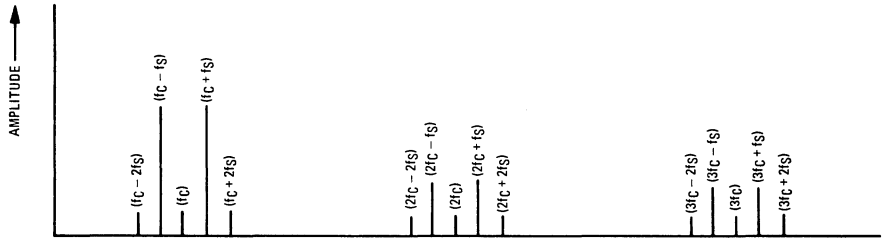


FIGURE 32 – 150 to 300 MHz DOUBLER



L1 = 1 TURN AWG NO. 18 WIRE, 7/32" ID



DEFINITIONS

f_C	CARRIER FUNDAMENTAL	$f_C \pm nf_S$	FUNDAMENTAL CARRIER SIDEBAND HARMONICS
f_S	MODULATING SIGNAL	nf_C	CARRIER HARMONICS
$f_C \pm f_S$	FUNDAMENTAL CARRIER SIDEBANDS	$nf_C \pm nf_S$	CARRIER HARMONIC SIDEBANDS

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MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC2830

Product Preview

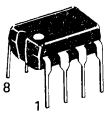
VOICE ACTIVATED SWITCH

The MC2830 circuit incorporates a microphone amplifier (MIC AMP), automatic level control (ALC) and a voice activated switch. The voice activated switch circuit has the ability to distinguish a voice from the background noise and trigger the switch output circuit by the voice signal. Therefore, the switching operation is highly reliable in noisy environments. The ALC range of the microphone amplifier is over 50 dB and can be adjusted by an external resistor. This device is particularly suitable for applications such as radio transceivers, car radios, message storage recorders, and voice controlled toys.

- Microphone Amplifier with External Feedback
- External Resistor Adjust ALC Over 50 dB
- Voice Activated Switch with Externally Controlled Sensitivity
- Low Voltage Operation from 1.8 to 8.0 V

VOICE ACTIVATED SWITCH

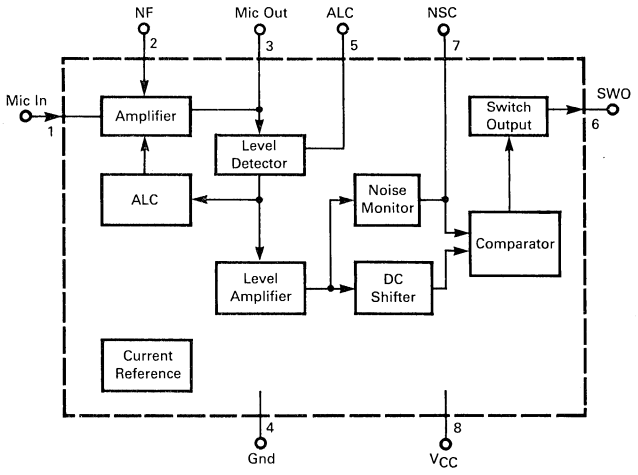
SILICON MONOLITHIC INTEGRATED CIRCUIT



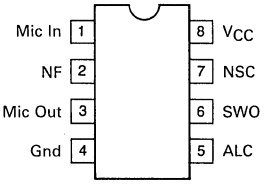
P SUFFIX
PLASTIC PACKAGE
CASE 626

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO-8)

FIGURE 1 — FUNCTIONAL BLOCK DIAGRAM



PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Temperature Range	Package
MC2830D MC2830P	0 to +70°C	SO-8 Plastic DIP

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	10	V
Operation Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Loading Current: Pin 3 Pin 6	I_O I_{SWO}	200 2.0	μA mA

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, Input Frequency = 1.0 kHz, Loading Resistor = 50 kOhm, T_A = 25°C)

Characteristic	Pin	Symbol	Min	Typ	Max	Unit
Supply Voltage	8	V_{CC}	1.8	—	8.0	V
Quiescent Current	8	I_D	—	—	2.0	mA
MIC AMP Open Loop Gain		A_{VOL}	—	80	—	dB
Total Harmonic Distortion of MIC AMP (V_O = 0.1 Vrms)	3	THD	—	1.0	—	%
Maximum MIC AMP Output Swing	3	V_O	—	0.16	—	Vrms
ALC Range (−6.0 dB, R1 = 33 k, V_{in} = 1.0 V)	3	ALC	40	50	—	dB
Ripple Rejection	3	RR	—	55	—	dB
Voice Trigger Level Above Noise		$V_{s/n}$	—	3.0	—	dB
Switch Output Current	6	I_{SWO}	—	—	2.0	mA
Switch Output Voltage (I_{SWO} = 2.0 mA) High Low	6	V_{SWO}	 4.6 —	 — —	 — 0.4	V

PIN FUNCTION DESCRIPTION

Pin No.	Function	Description
1	MIC IN	Input of the microphone amplifier. The gain of the amplifier is set by the external components of the R_f, R2, and C2 (See formula 2).
2	NF	This is the negative feedback input pin of the microphone amplifier.
3	MIC OUT	Output of the microphone amplifier. It is designed to drive a maximum load current of 200 μA.
4	GND	The ground pin.
5	ALC	This pin is for the ALC level detector filter. An RC is connected to this pin.
6	SWO	This is the output pin of the voice activated switch. A resistor at this pin sets the voice trigger level above the noise level. The current drain of this pin is around 20 μA typical with a switch "off" state. The maximum output voltage level is V_{CC}-V_{CES} with a maximum output current of 2.0 mA. As shown in Figure 3, this output is used to connect a switch time delay circuit to unify the "on" time. In Figure 3, C5 is the time delay capacitor which controls the "on" time of TR1.
7	NSC	The Noise Storing Capacitor at this pin sets the rise time and decay time. The rise time is determined by the constant of the R5C4.
8	V_{CC}	This pin has a low voltage operation from 1.8 to 8.0 Volts.

FIGURE 2 — TEST CIRCUIT

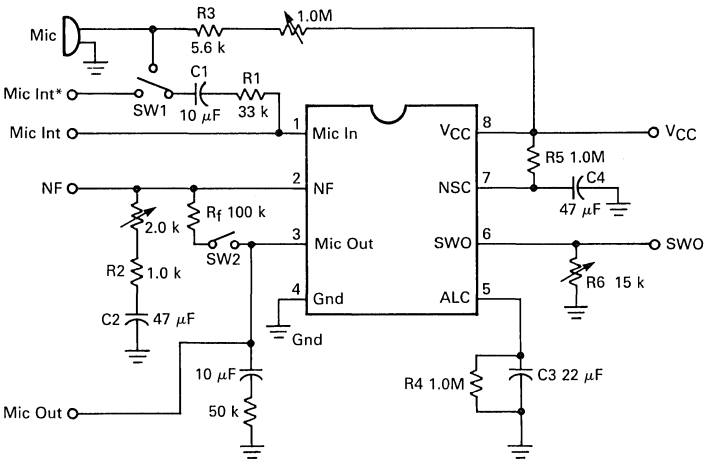
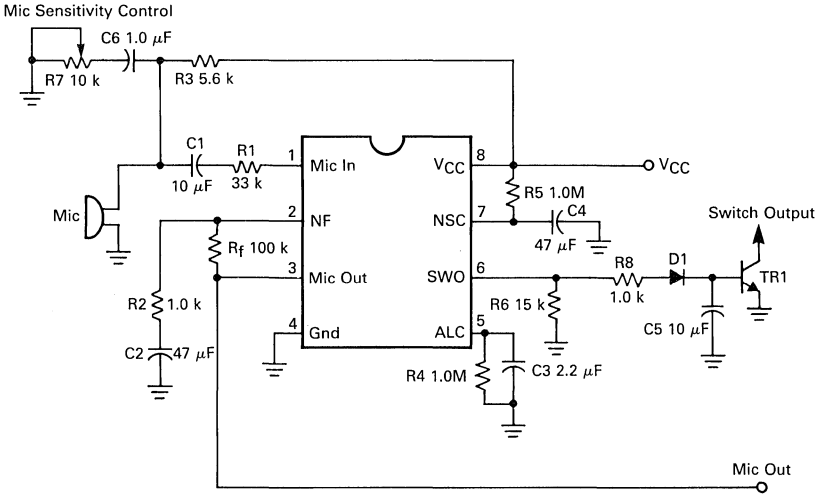


FIGURE 3 — TYPICAL APPLICATION CIRCUIT



FUNCTIONAL DESCRIPTION

As shown in the block diagram, the features provided by the MC2830 are the microphone amplifier with ALC and voice switch circuit. The detailed functional circuitry is described below.

Microphone Amplifier

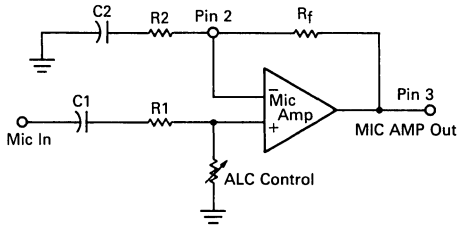
The MIC AMP is a noninverting amplifier as shown in Figure 4. An ALC controlled resistance is connected to the input pin of the MIC AMP to accomplish ALC function. The voltage gain and ALC attenuation ratio are given in formulas (1) and (2):

$$\text{Voltage Gain} = 1 + \frac{R_f}{R2 = 1/\omega C2} \quad (1)$$

$$\text{ALC} = 20 \log \left(\frac{R1 + R_{alc}}{R_{alc}} \right) \quad (2)$$

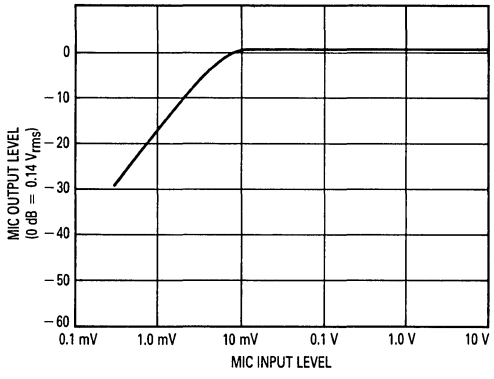
Replacing R_f by a Z_f network can be formed as a band pass, low pass or high pass network for various applications.

FIGURE 4 — MIC AMPLIFIER WITH ALC



A typical application circuit is shown in Figure 3, the ALC performance of the microphone amplifier is shown in Figure 5.

FIGURE 5 — ALC CHARACTERISTICS

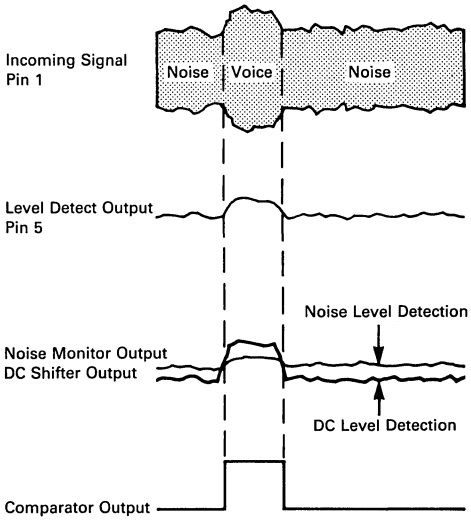


Voice Detection and Switching

A traditional voice activated circuit design is unable to distinguish between voice and noise in the incoming signal. In a noisy environment, the switch is often mistriggered by noise, or the activation sensitivity must be reduced. The MC2830 voice activated circuit has overcome this weakness in traditional designs. The switch is activated by voice level above the noise and is not affected by the background noise level. This is accomplished by utilizing the differences in voice and noise waveforms. Voice waveforms generally have a wide range of variation in amplitude, whereas noise waveforms are more stable. With this in mind, the NOISE MONITOR in Figure 1 was designed to have an output characteristic which has a slow attack time but a fast decay time. When the envelope of incoming signal, which consists of voice and noise, is passing through it, the voice will not be stable during the long time constant of RC (approx. 45 seconds) and it is therefore degraded. Whereas the noise content of incoming signal is delayed at the rising edge of its envelope, as in Figure 6. Meanwhile, the envelope of the incoming signal is passing through the DC SHIFTER path, which does not introduce any time constant or amplification, but gives the incoming signal envelope a dc offset set by resistor R6.

By comparing the two signals from the output of the DC SHIFTER and the NOISE MONITOR, as in Figure 6, the voice is distinguished from the incoming signal and activates the switch circuit. The sensitivity of voice activation depends on the value of R6. The voice activation sensitivity is reduced from 3.0 dB to 8.0 dB above the noise if R6 changes from 14 k to 7.0 k.

FIGURE 6 — WAVEFORMS OF VOICE DETECTION AND SWITCHING



8

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC2831A

LOW POWER FM TRANSMITTER SYSTEM

The MC2831A is a one-chip FM transmitter subsystem designed for cordless telephone and FM communication equipment. It includes a Microphone Amplifier, Pilot Tone Oscillator, Voltage Controlled Oscillator and Battery Monitor.

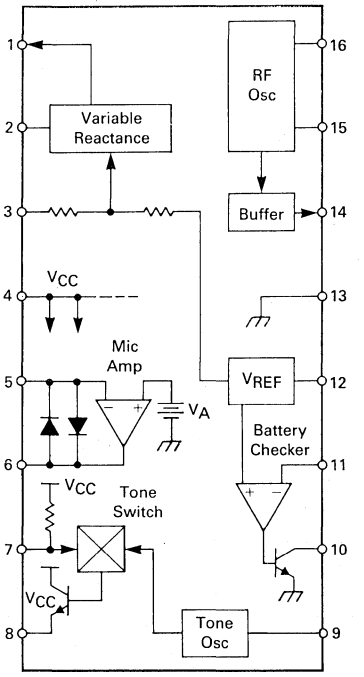
- Wide Range of Operating Supply Voltage (3.0 V–8.0 V)
- Low Drain Current (4.0 mA Typ Full Operation at V_{CC} = 4.0 V)
- Battery Checker (290 μA Typ at V_{CC} = 4.0 V)
- Low Number of External Parts Required
- Users Must Comply with Local Regulations on R.F. Transmission (FCC, DOT, P.T.T., etc)

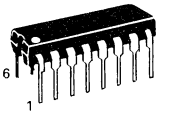
LOW POWER FM TRANSMITTER SYSTEM

SILICON MONOLITHIC INTEGRATED CIRCUIT

8

FUNCTIONAL BLOCK DIAGRAM

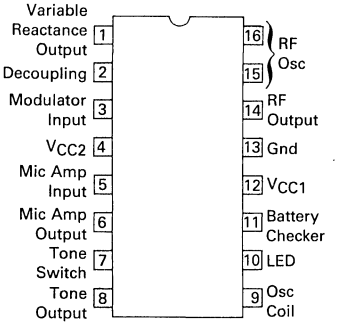




P SUFFIX
PLASTIC PACKAGE
CASE 648

D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO-16)

PIN ASSIGNMENTS



ORDERING INFORMATION

Device	Temperature Range	Package
MC2831AD	−30°C to +75°C	SO-16
MC2831AP		Plastic DIP

MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	10	Vdc
Operating Supply Voltage Range	V_{CC}	3.0 to 8.0	Vdc
Battery Checker Output Sink Current	I_{LED}	25	mA
Junction Temperature	T_J	+150	°C
Operating Ambient Temperature Range	T_A	−30 to +75	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

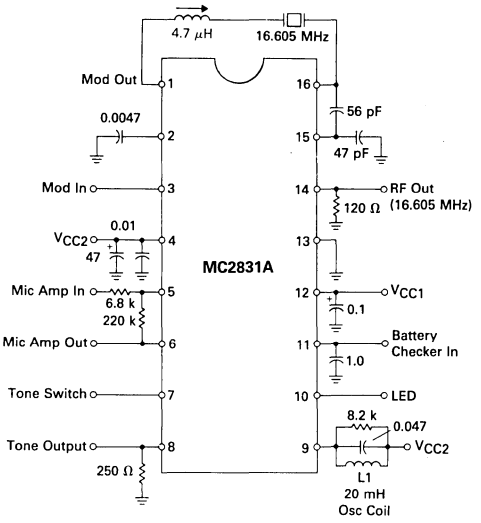
ELECTRICAL CHARACTERISTICS (V_{CC1} = 4.0 Vdc, V_{CC2} = 4.0 Vdc, T_A = 25°C, unless otherwise noted)

Characteristic	Symbol	Pin	Min	Typ	Max	Unit
Drain Current	I_{CC1}	12	150	290	420	μA
Drain Current	I_{CC2}	4	2.2	3.6	6.5	mA
BATTERY CHECKER						
Threshold Voltage (LED Off → On)	V_{TB}	11	1.0	1.2	1.4	Vdc
Output Saturation Voltage (Pin 11 = 0 V, Pin 10 Sink Current = 5.0 mA)	V_{OSAT}	10	—	0.15	0.5	Vdc
MIC AMPLIFIER						
Voltage Gain, Closed Loop (V_{in} = 1.0 mV_{rms}, f_{in} = 1.0 kHz)	A_V	5, 6	27	30	33	dB
Output DC Voltage	V_{Odc}	6	1.1	1.4	1.7	Vdc
Output Swing (V_{in} = 30 mV_{rms}, f_{in} = 1.0 kHz)	V_{Op-p}	6	0.8	1.2	1.6	Vp-p
Total Harmonic Distortion (V_O = 31 mV_{rms}, f_{in} = 1.0 kHz)	THD	6	—	0.7	—	%
PILOT TONE OSCILLATOR (250 Ω LOADING)						
Output AF Voltage (f_o = 5.0 kHz)	V_{AFO}	8	—	50	—	mV_{rms}
Output DC Voltage	V_{Odc}	8	—	1.4	—	Vdc
Total Harmonic Distortion (f_o = 5.0 kHz, V_{AF} = 150 mV_{rms})	THD	8	—	1.8	5.0	%
Tone Switch Threshold	—	7	1.1	1.4	1.7	Vdc
FM MODULATOR (120 Ω LOADING)						
Output RF Voltage (f_o = 16.6 MHz)	VRFO	14	—	40	—	mV_{rms}
Output DC Voltage	V_{Odc}	14	—	1.3	—	Vdc
Modulation Sensitivity (Note 1) (V_{in} = 1.0 V ± 0.2 V)	SEN	3, 14	6.0	10	18	Hz/mVdc
Maximum Deviation (Note 1) (V_{in} = 0 V to +2.0 V)	F_{dev}	3, 14	±2.5	±5.0	±12.5	kHz
RF Frequency Range	—	14	—	—	60	MHz

Note 1. Modulation sensitivity and maximum deviation are measured at 49.815 MHz, which is the third harmonic of the crystal frequency.

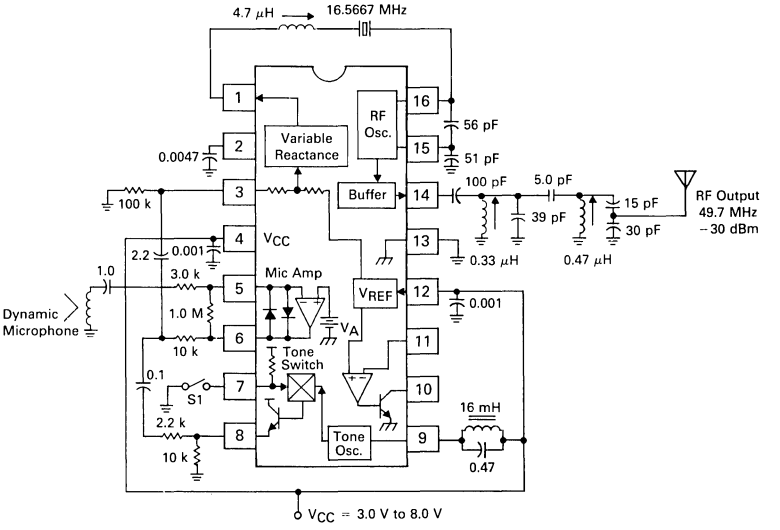
8

FIGURE 1 — TEST CIRCUIT



L1 Toko America
7PA Type
126AN — 6708X

FIGURE 2 — SINGLE CHIP FM VHF TRANSMITTER AT 49.7 MHz



NOTES:

S1 is a normally closed push button type switch.

The crystal used is fundamental mode, calibrated for parallel resonance with a 32 pF load. The 49.7 MHz output is generated in the output buffer, which generates useful harmonics to 60 MHz.

The network on the output at Pin 14 provides output tuning and impedance matching to 50 Ω at 49.7 MHz. Harmonics are suppressed by more than 25 dB.

Battery checker circuit (Pins 10, 11) is not used in this application.

All capacitors in microfarads, inductors in Henries and resistors in Ohms, unless otherwise specified.

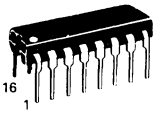
MC2833

LOW POWER FM TRANSMITTER SYSTEM

MC2833 is a one-chip FM transmitter subsystem designed for cordless telephone and FM communication equipment. It includes a microphone amplifier, voltage controlled oscillator and two auxiliary transistors.

- Wide Range of Operating Supply Voltage (2.8–9.0 V)
- Low Drain Current (I_{CC} = 2.9 mA Typ)
- Low Number of External Parts Required
- −30 dBm Power Output to 60 MHz Using Direct RF Output
- +10 dBm Power Output Attainable Using On-Chip Transistor Amplifiers
- Users Must Comply with Local Regulations on R.F. Transmission (FCC, DOT, P.T.T., etc)

LOW POWER FM TRANSMITTER SYSTEM

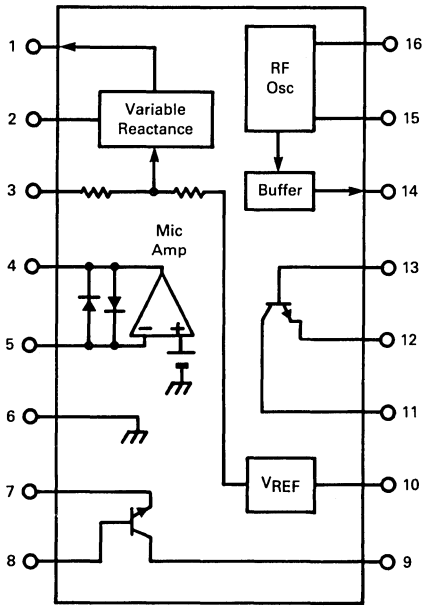


P SUFFIX
PLASTIC PACKAGE
CASE 648

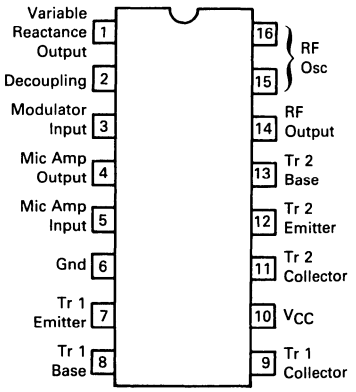
D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO-16)

8

FUNCTIONAL BLOCK DIAGRAM



PIN ASSIGNMENTS



MAXIMUM RATINGS

Ratings	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	10 (max)	V
Operating Supply Voltage Range	V_{CC}	2.8–9.0	V
Junction Temperature	T_J	+150	°C
Operating Ambient Temperature	T_A	−30 to +75	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 4.0 V, T_A = 25°C, unless otherwise noted)

Characteristics	Symbol	Pin	Min	Typ	Max	Unit
Drain Current (No input signal)	I_{CC}	10	1.7	2.9	4.3	mA
FM MODULATOR						
Output RF Voltage (f_o = 16.6 MHz)	V_{out} RF	14	60	90	130	mVrms
Output DC Voltage (No input signal)	Vdc	14	2.2	2.5	2.8	V
Modulation Sensitivity (f_o = 16.6 MHz) (V_{in} = 0.8 V to 1.2 V)	SEN	3.0 14	7.0 —	10 —	15 —	Hz/mVdc
Maximum Deviation (f_o = 16.6 MHz) (V_{in} = 0 V to 2.0 V)	Fdev	3.0 14	3.0 —	5.0 —	10 —	kHz
MIC AMPLIFIER						
Closed Loop Voltage Gain (V_{in} = 3.0 mVrms) (f_{in} = 1.0 kHz)	A_V	4.0 5.0	27 —	30 —	33 —	dB
Output DC Voltage (No input signal)	V_{out} dc	4.0	1.1	1.4	1.7	V
Output Swing Voltage (V_{in} = 30 mVrms) (f_{in} = 1.0 kHz)	V_{out} p-p	4.0	0.8	1.2	1.6	Vp-p
Total Harmonic Distortion (V_{in} = 3.0 mVrms) (f_{in} = 1.0 kHz)	THD	4.0	—	0.15	2.0	%

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AUXILIARY TRANSISTOR STATIC CHARACTERISTICS

Characteristics	Symbol	Min	Typ	Max	Unit
Collector Base Breakdown Voltage (I_C = 5.0 μA)	$V_{(BR)CBO}$	15	45	—	V
Collector Emitter Breakdown Voltage (I_C = 200 μA)	$V_{(BR)CEO}$	10	15	—	V
Collector Substrate Breakdown Voltage (I_C = 50 μA)	$V_{(BR)CSO}$	—	70	—	V
Emitter Base Breakdown Voltage (I_E = 50 μA)	$V_{(BR)EBO}$	—	6.2	—	V
Collector Base Cut Off Current (V_{CB} = 10 V) (I_E = 0)	I_{CBO}	—	—	200	nA
DC Current Gain (I_C = 3.0 mA) (V_{CE} = 3.0 V)	h_{FE}	40	150	—	—

AUXILIARY TRANSISTOR DYNAMIC CHARACTERISTICS

Current Gain Bandwidth Product (V_{CE} = 3.0 V) (I_C = 3.0 mA)	f_T	—	500	—	MHz
Collector Base Capacitance (V_{CE} = 3.0 V) (I_C = 0)	C_{CB}	—	2.0	—	pF
Collector Substrate Capacitance (V_{CS} = 3.0 V) (I_C = 0)	C_{CS}	—	3.3	—	pF

FIGURE 1 — TEST CIRCUIT

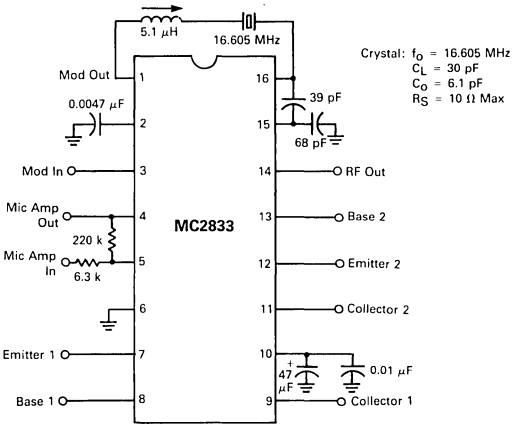
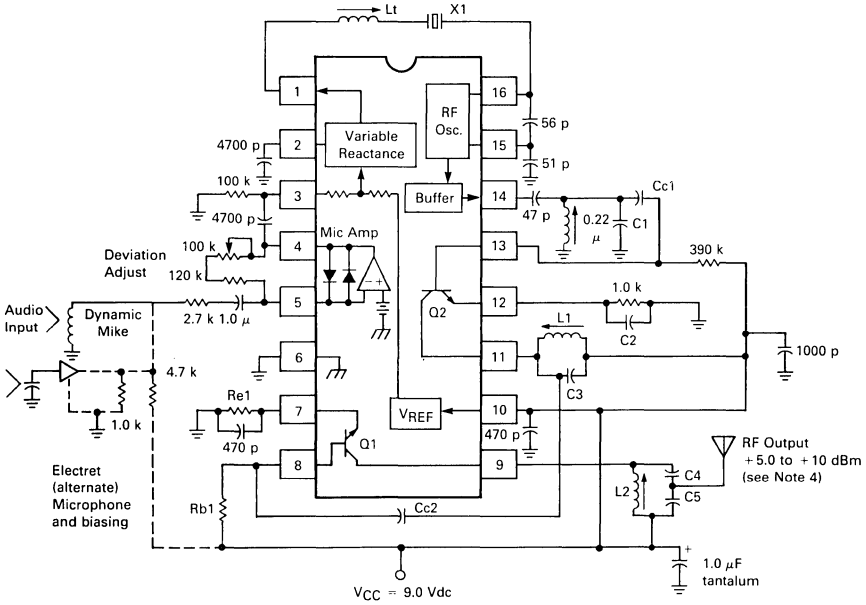


FIGURE 2 — SINGLE CHIP VHF NARROWBAND FM TRANSMITTER



NOTES:

1. Components versus output frequency:

Output RF	X1 (MHz)	Lt (μH)	L1 (μH)	L2 (μH)	Re1	Rb1	Cc1	Cc2	C1	C2	C3	C4	C5
50 MHz	16.6667	3.3–4.7	0.22	0.22	330	390 k	33 p	33 p	33 p	470 p	33 p	47 p	220 p
76 MHz	12.6000	5.1	0.22	0.22	150	300 k	68 p	10 p	68 p	470 p	12 p	20 p	120 p
144 MHz	12	5.6	0.15	0.10	150	220 k	47 p	10 p	68 p	1000 p	18 p	12 p	33 p

2. Crystal X1 is fundamental mode, calibrated for parallel resonance with a 32 pF load. The final output frequency is generated by frequency multiplication within the MC2833 IC. The RF output buffer (Pin 14) and Q2 transistor are used as a frequency tripler and doubler, respectively, in the 76 and 144 MHz transmitters. The Q1 output transistor is a linear amplifier in the 49.7 MHz and 76 MHz transmitters, and a frequency doubler in the 144 MHz transmitter.

3. All coils used are 7 mm shielded inductors,CoilCraft series M1175A, M1282A–M1289A, M1312A or equivalent

4. Power output is ≈ + 10 dBm for 50 MHz and 76 MHz transmitters, and ≈ + 5.0 dBm for the 144 MHz transmitter at V_{CC} = 8.0 V. Power output drops with lower V_{CC}.

5. All capacitors in microfarads, inductors in Henries and resistors in Ohms unless otherwise specified.

6. Other frequency combinations may be set-up by simple scaling of the 3 examples shown.

FIGURE 3 — BUFFER/MULTIPLIER (X3, PIN 14)
(16 MHz FUNDAMENTAL)

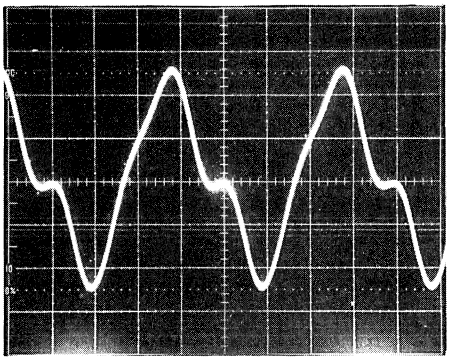


FIGURE 4 — INPUT TO DOUBLER (PIN 13)
(50 MHZ x 3 COMPONENT)

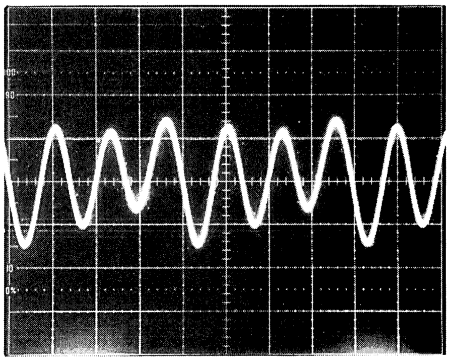


FIGURE 5 — DOUBLER OUTPUT 76 MHz (PIN 11)

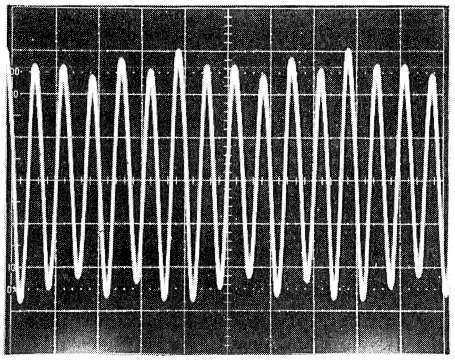


FIGURE 6 — SPECTRUM

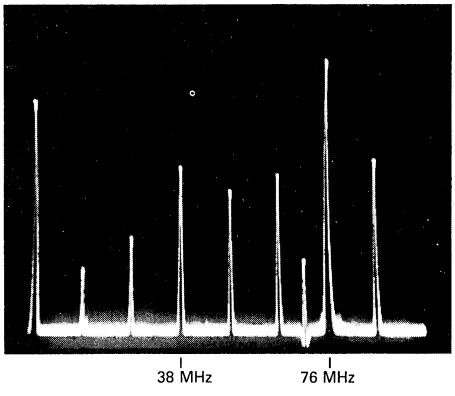


FIGURE 7 — OUTPUT SPECTRUM (50 MHz)

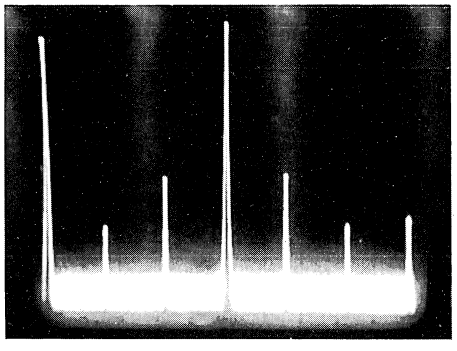


FIGURE 8 — MODULATION SPECTRUM
(1.0 kHz SHOWING CARRIER NULL)

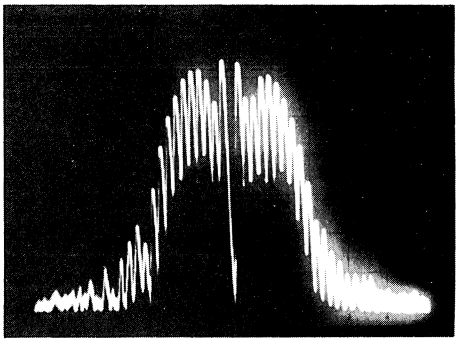


FIGURE 9 — 144 MHz/X12 MULTIPLIER

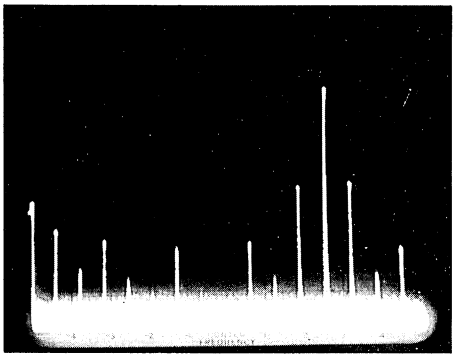


FIGURE 10 — CIRCUIT SIDE VIEW

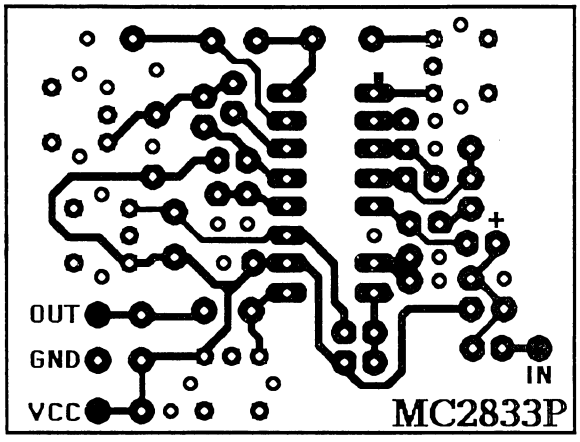


FIGURE 11 — GROUND PLANE ON COMPONENT SIDE

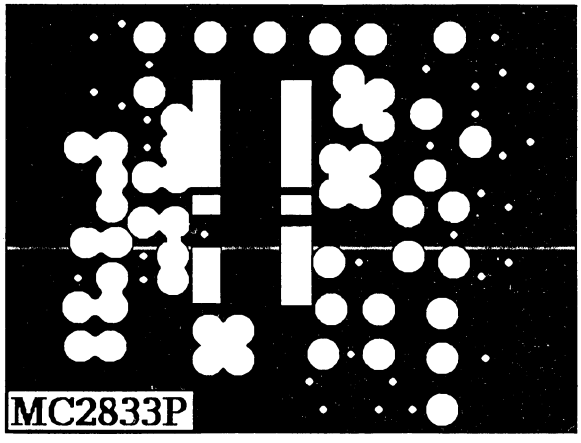
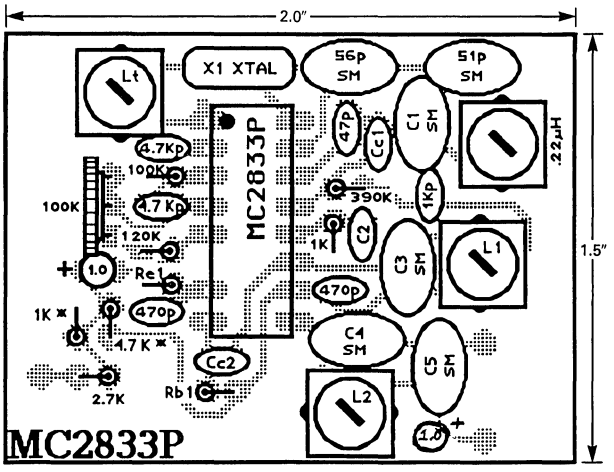


FIGURE 12 — COMPONENT VIEW



8

NOTES:

- Positive artwork povided.
- Drill holes must be plated to ensure making all groung (V_{EE}) connections!
- Resistors labelled * are used for biasing of electret microphone if used.
- Capacitors labelled "SM" are silver mica.
- Final board size is 1.5" x 2.0".

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC3335

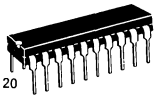
LOW POWER NARROWBAND FM RECEIVER

. . . includes dual FM conversion with Oscillators, Mixers, Quadrature Discriminator, and Meter Drive/Carrier Detect Circuitry. The MC3335 also has a comparator circuit for FSK detection.

- Complete Dual Conversion Circuitry
- Low Voltage: V_{CC} = 2.0 to 6.0 Vdc
- Low Drain Current (Typical 3.6 mA with V_{CC} = 3.0 Vdc)
- Excellent Sensitivity: −3.0 dB Input Limiting = 0.7 μV
- Externally Adjustable Carrier Detect Function
- Separate Data Shaping Output Circuitry
- Data Rate Up to 35000 Baud Detectable
- 60 dB RSSI Range
- Low Number of External Parts Required
- Manufactured in Motorola's MOSAIC Process Technology
- MC13135 is Preferred for New Designs

LOW POWER DUAL CONVERSION FM RECEIVER

SILICON MONOLITHIC INTEGRATED CIRCUIT

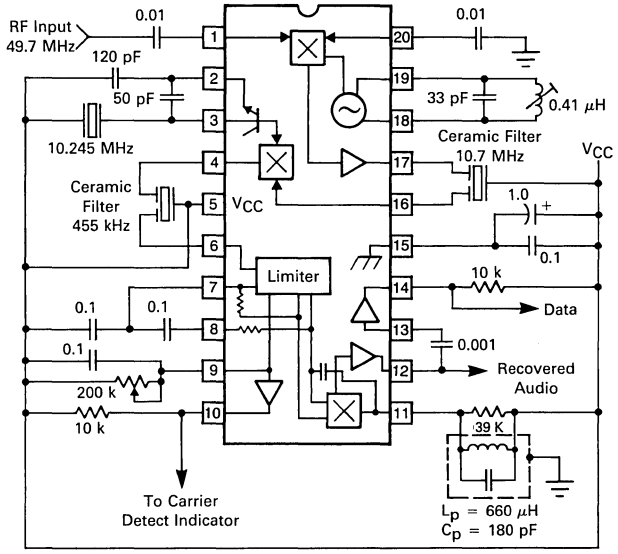


P SUFFIX
PLASTIC PACKAGE
CASE 738

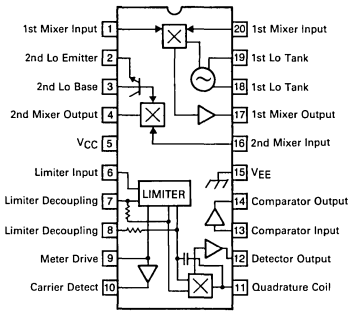
DW SUFFIX
PLASTIC PACKAGE
CASE 751D
(SO-20L)

8

TYPICAL APPLICATION AS A FIXED RECEIVER



PIN CONNECTION AND FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Device	Temperature Range	Package
MC3335DW	−40° to +85°C	SO-20
MC3335P		Plastic DIP

MOSAIC is a trademark of Motorola, Inc.

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage	5	$V_{CC(max)}$	7.0	Vdc
Operating Supply Voltage Range (Recommended)	5	V_{CC}	2.0 to 6.0	Vdc
Input Voltage (V_{CC} > 5.0 Vdc)	1,20	V1–20	1.0	Vrms
Junction Temperature	—	T_J	150	°C
Operating Ambient Temperature Range	—	T_A	−40 to +85	°C
Storage Temperature Range	—	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc, f_o = 49.7 MHz, Deviation = 3.0 kHz, T_A = 25°C, test circuit of Figure 2, unless otherwise noted.)

Characteristic	Pin	Min	Typ	Max	Unit
Drain Current	5	—	4.5	7.0	mAdc
Input for −3.0 dB Limiting	—	—	0.7	2.0	μVrms
Recovered Audio (RF Signal Level = 1.0 mV)	12	—	250	—	mVrms
Noise Output (RF Signal Level = 0 mV)	12	—	250	—	mVrms
Carrier Detect Threshold (below V_{CC})	9	—	0.64	—	Vdc
Meter Drive Slope	9	—	100	—	μA/dB
Input for 20 dB (S+N/N)	—	—	1.3	—	μVrms
First Mixer 3rd Order Intercept (Input)	—	—	−20	—	dBm
First Mixer Input Resistance (R_p)	—	—	690	—	Ω
First Mixer Input Capacitance (C_p)	—	—	7.2	—	pF
First Mixer Conversion Voltage Gain	—	—	18	—	dB
Second Mixer Conversion Voltage Gain	—	—	21	—	dB
Detector Output Resistance	12	—	1.4	—	kΩ

8

FIGURE 1 — TEST CIRCUIT

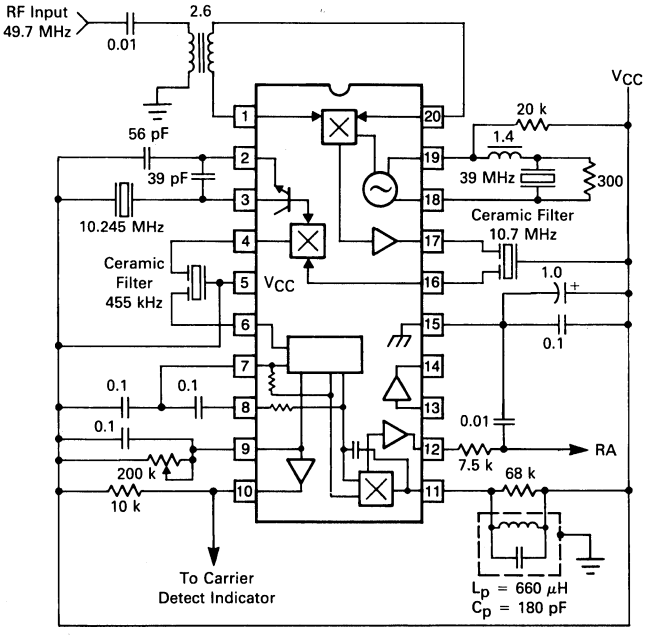


FIGURE 2 — I_{meter} versus INPUT

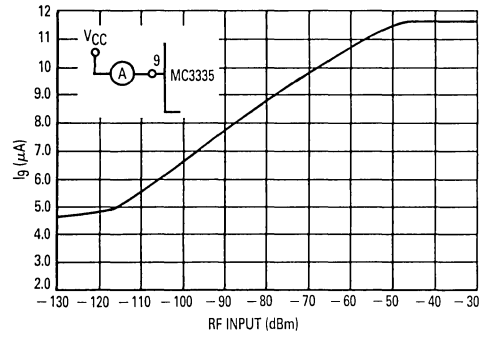


FIGURE 3 — DRAIN CURRENT, RECOVERED AUDIO versus SUPPLY

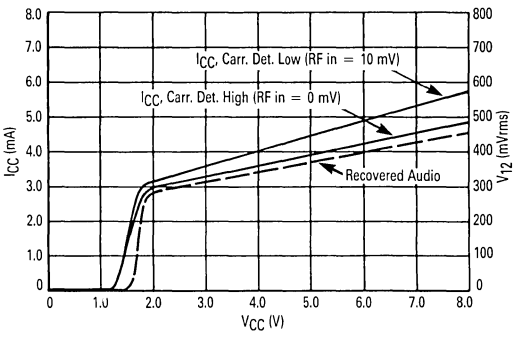


FIGURE 4 — (S+N), N OF 2ND MIXER

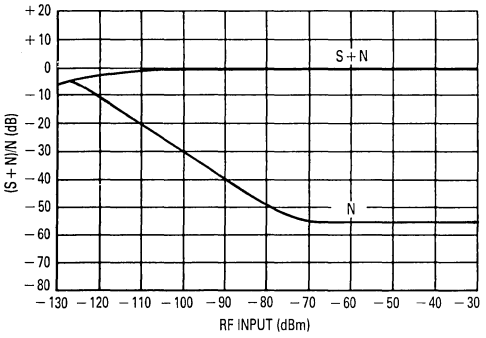


FIGURE 5 — (S+N)/N versus INPUT

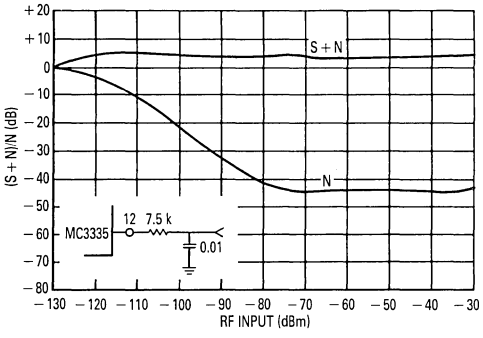


FIGURE 6 — 1ST MIXER 3RD ORDER INTERMODULATION

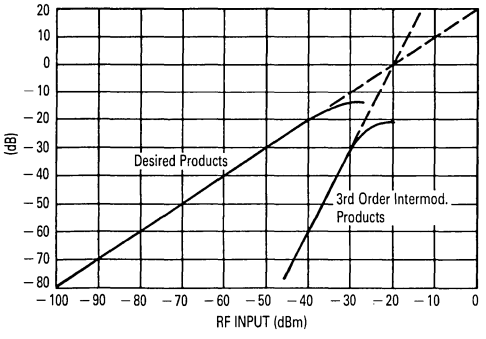
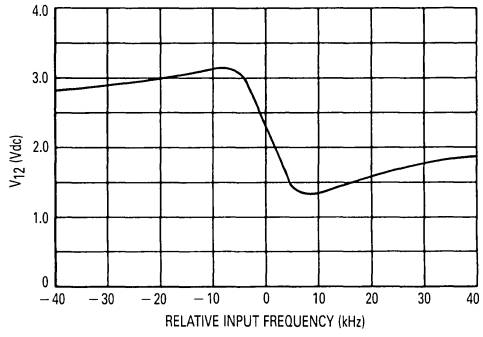


FIGURE 7 — DETECTOR OUTPUT versus FREQUENCY



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CIRCUIT DESCRIPTION

The MC3335 is a complete FM narrowband receiver from antenna input to audio preamp output. The low voltage dual conversion design yields low power drain, excellent sensitivity and good image rejection in narrowband voice and data link applications.

In the typical application diagram, the first mixer amplifies the signal and converts the RF input to 10.7 MHz. This IF signal is filtered externally and fed into the second mixer, which further amplifies the signal and converts it to a 455 kHz IF signal. After external bandpass filtering, the low IF is fed into the limiting amplifier and detection circuitry. The audio is recovered using a conventional quadrature detector. Twice-IF filtering is provided internally.

The input signal level is monitored by meter drive circuitry which detects the amount of limiting in the limiting amplifier. The voltage at the meter drive pin determines the state of the carrier detect output which is active low.

APPLICATION

The first local oscillator can be run using a free running LC tank, as a VCO using PLL synthesis, or driven from an external crystal oscillator. At higher V_{CC} values (6.0–7.0 V), it has been run to 170 MHz. The second local oscillator is a common base Colpitts type which is typically run at 10.245 MHz under crystal control.

The mixers are doubly balanced to reduce spurious responses. The first and second mixers have conversion gains of 18 dB and 22 dB (typical), respectively. Mixer gain is stable with respect to supply voltage. For both conversions, the mixer impedances and pin layout are designed to allow the user to employ low cost, readily available ceramic filters. Overall sensitivity is shown in Figure 5. The input level for 20 dB (S+N)/N is 1.3 μV using the two-pole post-detection filter is demonstrated.

Following the first mixer, a 10.7 MHz ceramic bandpass filter is recommended. The 10.7 MHz filtered signal is then fed into one second mixer input pin, the other input pin being connected to V_{CC}. Pin 5 (V_{CC}) is treated as a common point for emitter-driven signals.

The 455 kHz IF is typically filtered using a ceramic bandpass filter, then fed into the limiter input pin. The limiter has 10 μV sensitivity for −3.0 dB limiting, flat to 1.0 MHz.

The output of the limiter is internally connected to the quadrature detector, including a quadrature capacitor. A parallel LC tank is needed externally from Pin 11 to V_{CC}. A 39 kΩ shunt resistance is included which determines the peak separation of the quadrature detector; a smaller value will increase the spacing and linearity but decrease recovered audio and sensitivity.

A data shaping circuit is available and can be coupled to the recovered audio output of Pin 12. The circuit is a comparator which is designed to detect zero crossings of FSK modulation. Data rates of up to 35000 baud are detectable using the typical application. Hysteresis is available by connecting a high-valued resistor from Pin 13 to Pin 14. Values below 120 kΩ are not recommended as the input signal cannot overcome the hysteresis.

The meter drive circuitry detects input signal level by monitoring the limiting of the limiting amplifier stages. Figure 2 shows the unloaded current at Pin 9 versus input power. The meter drive current can be used directly (RSSI) or can be used to trip the carrier detect circuit at a specified input power. To do this, pick an RF trip level in dBm. Read the corresponding current from Figure 2 and pick a resistor such that:

$$R9 = 0.64\ Vdc / I9$$

Hysteresis is available by connecting a high-valued resistor RH between Pin 9 and 10. The formula is:

$$\text{Hysteresis} = V_{CC}/(RH \times 10^{-7})\ dB$$

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC3356

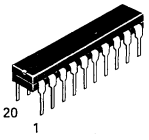
WIDEBAND FSK RECEIVER

SILICON MONOLITHIC
INTEGRATED CIRCUIT

WIDEBAND FSK RECEIVER

... includes Oscillator, Mixer, Limiting IF Amplifier, Quadrature Detector, Audio Buffer, Squelch, Meter Drive, Squelch Status output, and Data Shaper comparator. The MC3356 is designed for use in digital data communications equipment.

- Data Rates up to 500 kilobaud
- Excellent Sensitivity: −3 dB Limiting Sensitivity
  30 μVrms @ 100 MHz
- Highly versatile, full function device, yet few external parts are required
- Down Converter Can be Used Independently — Similar to NE602



P SUFFIX
PLASTIC PACKAGE
CASE 738

DW SUFFIX
PLASTIC PACKAGE
CASE 751D
(SO-20L)

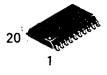


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FIGURE 1 — FUNCTIONAL BLOCK DIAGRAM

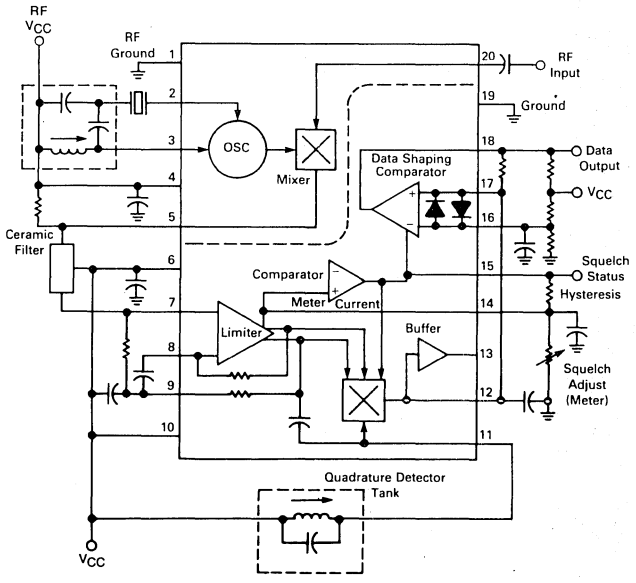
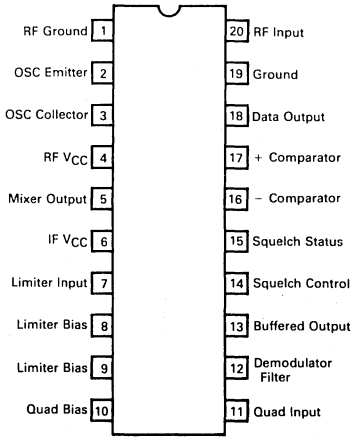


FIGURE 2 — PIN CONNECTIONS



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	$V_{CC(max)}$	15	Vdc
Operating Power Supply Voltage Range (Pins 6, 10)	V_{CC}	3.0 to 9.0	Vdc
Operating RF Supply Voltage Range (Pin 4)	RF V_{CC}	3.0 to 12.0	Vdc
Junction Temperature	T_J	150	°C
Operating Ambient Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Power Dissipation, Package Rating	P_D	1.25	W

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc, f_o = 100 MHz, f_{osc} = 110.7 MHz, Δf = ±75 kHz, f_{mod} = 1.0 kHz, 50 Ω source, T_A = 25°C, test circuit of Figure 3, unless otherwise noted.)

Characteristics	Min	Typ	Max	Unit
Drain Current Total, RF V_{CC} and V_{CC}	—	20	25	mAdc
Input for −3 dB limiting	—	30	—	μVrms
Input for 50 dB quieting $\left(\frac{S+N}{N}\right)$	—	60	—	μVrms
Mixer Voltage Gain, Pin 20 to Pin 5	2.5	—	—	
Mixer Input Resistance, 100 MHz	—	260	—	Ω
Mixer Input Capacitance, 100 MHz	—	5.0	—	pF
Mixer/Oscillator Frequency Range (Note 1)	—	0.2 to 150	—	MHz
IF/Quadrature Detector Frequency Range (Note 1)	—	0.2 to 50	—	MHz
AM Rejection (30% AM, RF V_{in} = 1.0 mVrms)	—	50	—	dB
Demodulator Output, Pin 13	—	0.5	—	Vrms
Meter Drive	—	7.0	—	μA/dB
Squelch Threshold	—	0.8	—	Vdc

Note 1: Not taken in Test Circuit of Figure 3; new component values required.

FIGURE 3 — TEST CIRCUIT

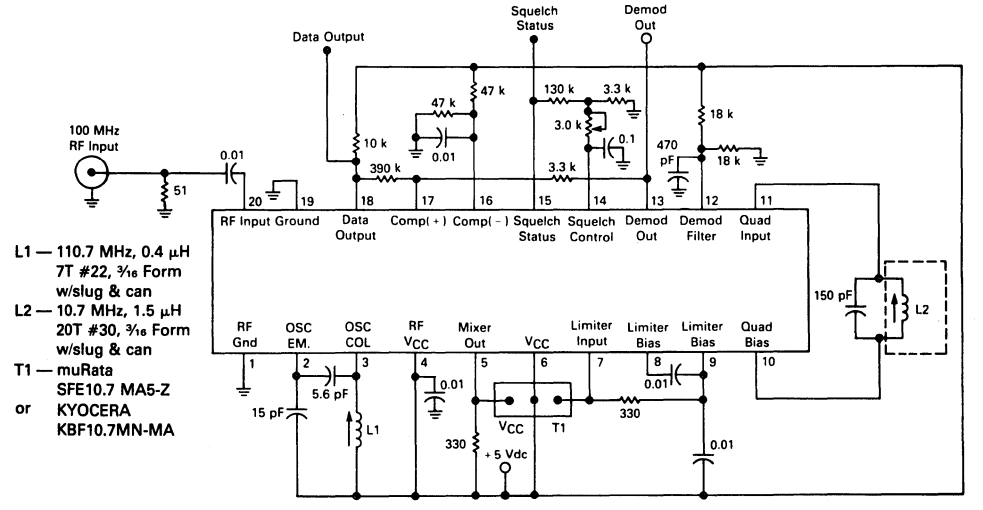


FIGURE 4 — OUTPUT COMPONENTS OF SIGNAL, NOISE, AND DISTORTION

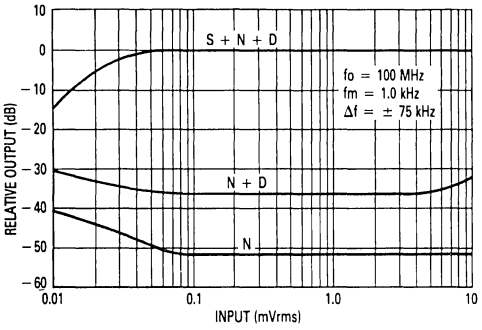
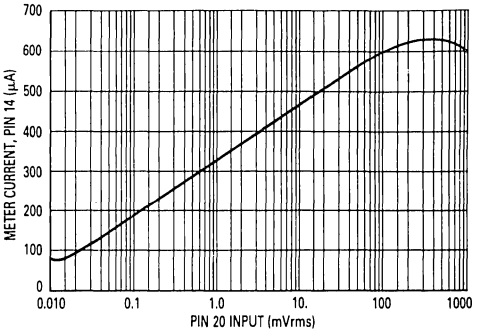


FIGURE 5 — METER CURRENT versus SIGNAL INPUT



GENERAL DESCRIPTION

This device is intended for single and double conversion VHF receiver systems, primarily for FSK data transmission up to 500 K baud (250 kHz). It contains an oscillator, mixer, limiting IF, quadrature detector, signal strength meter drive, and data shaping amplifier.

The oscillator is a common base Colpitts type which can be crystal controlled, as shown in Figure 1, or L-C controlled as shown in the other figures. At higher V_{CC}, it has been operated as high as 200 MHz. A mixer/oscillator voltage gain of 2 up to approximately 150 MHz, is readily achievable.

The mixer functions well from an input signal of 10 μVrms, below which the squelch is unpredictable, up to about 10 mVrms, before any evidence of overload. Operation up to 1.0 Vrms input is permitted, but nonlinearity of the meter output is incurred, and some oscillator pulling is suspected. The AM rejection above 10 mVrms is degraded.

The limiting IF is a high frequency type, capable of being operated up to 50 MHz. It is expected to be used at 10.7 MHz in most cases, due to the availability of standard ceramic resonators. The quadrature detector is internally coupled to the IF, and a 5.0 pF quadrature capacitor is internally provided. The −3dB limiting sensitivity of the IF itself is approximately 50 μV (at Pin 7), and the IF can accept signals up to 1.0 Vrms without distortion or change of detector quiescent dc level.

The IF is unusual in that each of the last 5 stages of the 6 state limiter contains a signal strength sensitive, current sinking device. These are parallel connected and buffered to produce a signal strength meter drive which is fairly linear for IF input signals of 10 μV to 100 mVrms. (See Figure 5.)

A simple squelch arrangement is provided whereby the meter current flowing through the meter load resistance flips a comparator at about 0.8 Vdc above ground. The signal strength at which this occurs can be adjusted by changing the meter load resistor. The comparator(+) input and output are available to permit control of hysteresis. Good positive action can be obtained for IF input signals of above 30 μVrms. The 130 kΩ resistor shown in the test circuit provides a small amount of hysteresis. Its connection between the 3.3 k resistor to ground and the 3.0 k pot, permits adjustment of squelch level without changing the amount of hysteresis.

The squelch is internally connected to both the quadrature detector and the data shaper. The quadrature detector output, when squelched, goes to a dc level approximately equal to the zero signal level, unsquelched. The squelch causes the data shaper to produce a high (V_{CC}) output.

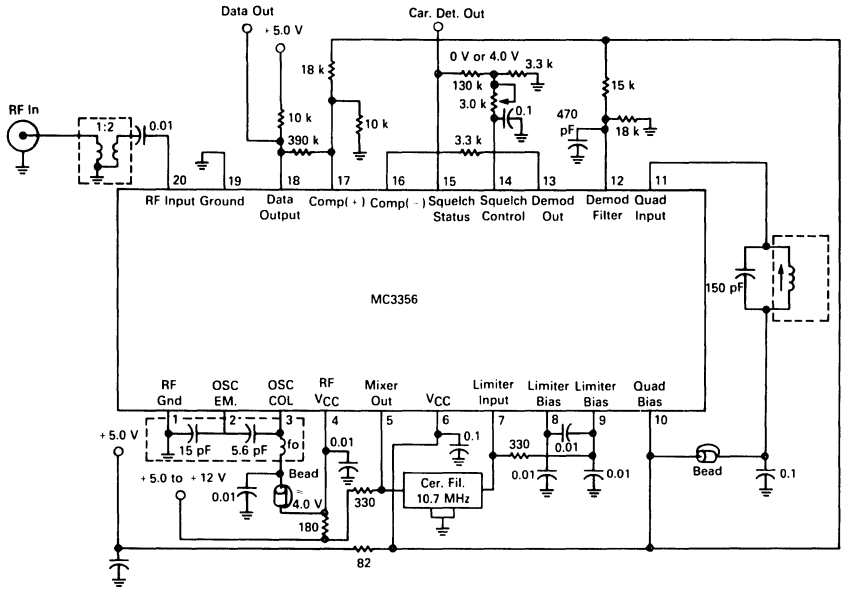
The data shaper is a complete "floating" comparator, with back to back diodes across its inputs. The output of the quadrature detector can be fed directly to either input of this amplifier to produce an output that is either at V_{CC} or V_{EE}, depending upon the received frequency. The impedance of the biasing can be varied to produce an amplifier which "follows" frequency detuning to some degree, to prevent data pulse width changes.

When the data shaper is driven directly from the demodulator output, Pin 13, there may be distortion at Pin 13 due to the diodes, but this is not important in the data application. A useful note in relating high/low input frequency to logic state: low IF frequency corresponds to low demodulator output. If the oscillator is above the incoming RF frequency, then high RF frequency will produce a logic low. (Input to (+)input of Data Shaper as shown in figures 1 and 3.)

APPLICATION NOTES

The MC3356 is a high frequency/high gain receiver that requires following certain layout techniques in designing a stable circuit configuration. The objective is to minimize or eliminate, if possible, any unwanted feedback.

FIGURE 6 — APPLICATION WITH FIXED BIAS ON DATA SHAPER



8

APPLICATION NOTES (continued)

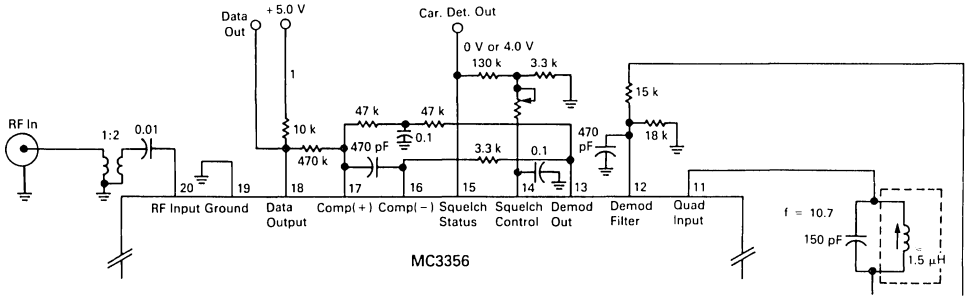
Shielding, which includes the placement of input and output components, is important in minimizing electrostatic or electromagnetic coupling. The MC3356 has its pin connections such that the circuit designer can place the critical input and output circuits on opposite ends of the chip. Shielding is normally required for inductors in tuned circuits.

The MC3356 has a separate V_{CC} and ground for the RF and IF sections which allows good external circuit isolation by minimizing common ground paths.

Note that the circuits of Figures 1 and 3 have RF, Oscillator, and IF circuits predominantly referenced to the plus supply rails. Figure 6, on the other hand, shows a suitable means of ground referencing. The two methods produce identical results when carefully executed. It is important to treat Pin 19 as a ground node for either approach. The RF input should be "grounded" to Pin 1 and then the input and the mixer/oscillator grounds (or RF V_{CC} bypasses) should be connected by a low inductance path to Pin 19. IF and detector sections should also have their bypasses returned by a **separate** path to Pin 19. V_{CC} and RF V_{CC} can be decoupled to minimize feedback, although the configuration of Figure 3 shows a successful implementation on a common 5.0 V supply. Once again, the message is: define a supply node and a ground node and return each section to those nodes by separate, low impedance paths.

The test circuit of Figure 3 has a 3 db limiting level of 30 μV which can be lowered 6 db by a 1:2 untuned transformer at the input as shown in figures 6 and 7. For applications that require additional sensitivity, an RF amplifier can be added, but with no greater than 20 db gain. This will give a 2.0 to 2.5 μV sensitivity and any additional gain will reduce receiver dynamic range without improving its sensitivity. Although the test circuit operates at +5.0 V, the mixer/oscillator optimum performance is at +8.0 V to 12 V. A minimum of +8.0 V is recommended in high frequency applications (above 150 MHz), or in PLL applications where the oscillator drives a prescaler.

FIGURE 7 — APPLICATION WITH SELF-ADJUSTING BIAS ON DATA SHAPER



APPLICATION NOTES (continued)

Depending on the external circuit, inverted or non-inverted data is available at Pin 18. Inverted data makes the higher frequency in the FSK signal a 'one' when the local oscillator is above the incoming RF. Figure 6 schematic shows the comparator with hysteresis. In this circuit the dc reference voltage at Pin 17 is about the same as the demodulated output voltage (Pin 13) when no signal is present. This type circuit is preferred for systems where the data rates can drop to zero. Some systems have a low frequency limit on the data rate, such as systems using the MC3850 ACIA that has a start or stop bit. This defines the low frequency limit that can appear in the data stream. Figure 6 circuit can then be changed to a circuit configuration as shown in Figure 7. In Figure 7 the reference voltage for the comparator is derived from the demodulator output through a low pass circuit where τ is much lower than the lowest frequency data rate. This and similar circuits will compensate for small tuning changes (or drift) in the quadrature detector.

Squelch status (Pin 15) goes high (squelch off) when the input signal becomes greater than some preset level set by the resistance between Pin 14 and ground. Hysteresis is added to the circuit externally by the resistance from Pin 14 to Pin 15.

8

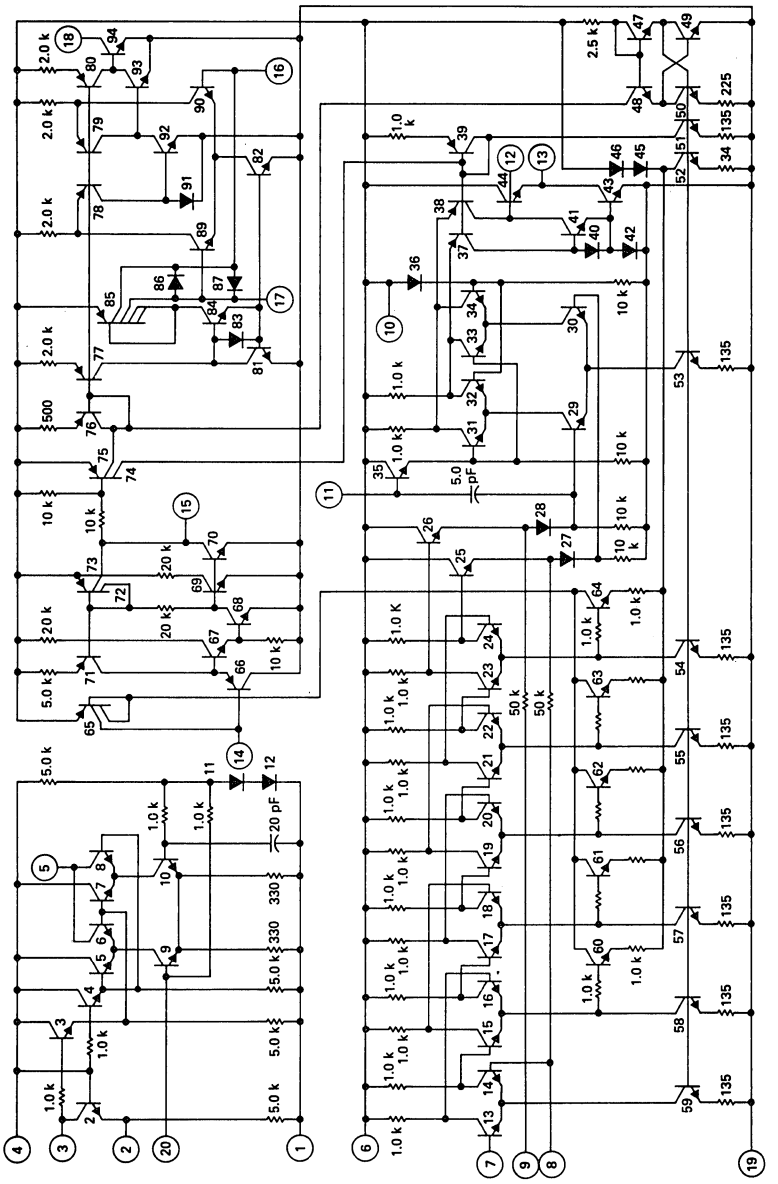


FIGURE 8 — INTERNAL SCHEMATIC

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC3357

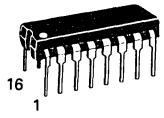
LOW POWER NARROWBAND FM IF

. . . includes Oscillator, Mixer, Limiting Amplifier, Quadrature Discriminator, Active Filter, Squelch, Scan Control, and Mute Switch. The MC3357 is designed for use in FM dual conversion communications equipment.

- Low Drain Current (3.0 mA (Typ) @ V_{CC} = 6.0 Vdc)
- Excellent Sensitivity: Input Limiting Voltage — (-3.0 dB) = 5.0 μV (Typ)
- Low Number of External Parts Required
- Recommend MC3372 for Replacement/Upgrade

LOW POWER FM IF

SILICON MONOLITHIC INTEGRATED CIRCUIT

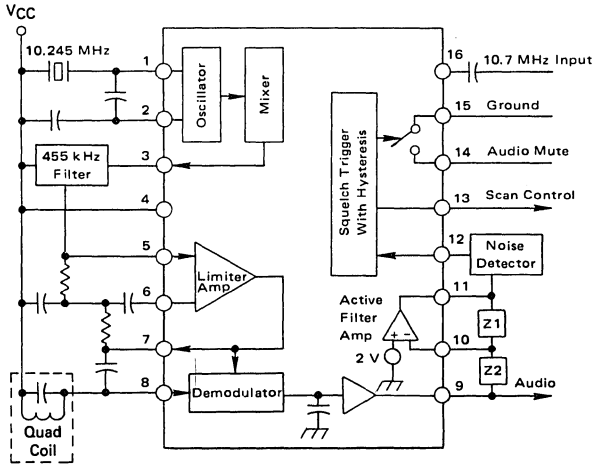


P SUFFIX
PLASTIC PACKAGE
CASE 648

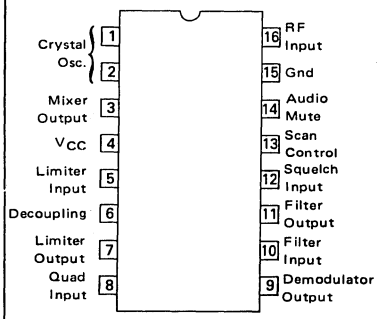
D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO-16)

8

FIGURE 1 — FUNCTIONAL BLOCK DIAGRAM



PIN CONNECTIONS



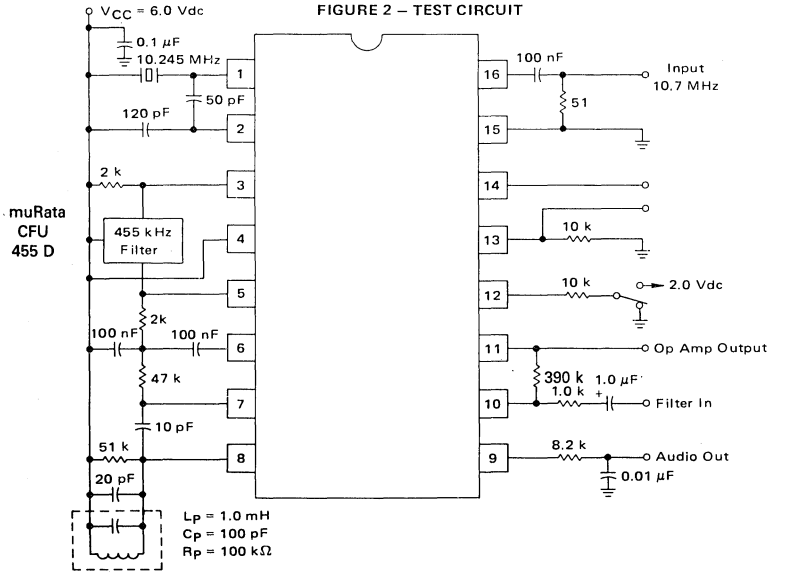
MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted)

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage	4	V_{CC}(max)	12	Vdc
Operating Supply Voltage Range	4	V_{CC}	4 to 8	Vdc
Detector Input Voltage	8	–	1.0	Vp-p
Input Voltage ($V_{CC} \geq$ 6.0 Volts)	16	V_{16}	1.0	V_{RMS}
Mute Function	14	V_{14}	-0.5 to 5.0	V_{pk}
Junction Temperature	–	T_J	150	°C
Operating Ambient Temperature Range	–	T_A	-30 to +70	°C
Storage Temperature Range	–	T_{stg}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 6.0 Vdc, fo = 10.7 MHz, Δf = ± 3.0 kHz, f_{mod} = 1.0 kHz, T_A = 25°C unless otherwise noted.)

Characteristic	Pin	Min	Typ	Max	Unit
Drain Current	4				mA
Squelch Off		–	2.0	–	
Squelch On		–	3.0	5.0	
Input Limiting Voltage (–3 dB Limiting)	16	–	5.0	10	μV
Detector Output Voltage	9	–	3.0	–	Vdc
Detector Output Impedance	–	–	400	–	Ω
Recovered Audio Output Voltage (V_{in} = 10 mV)	9	200	350	–	mVrms
Filter Gain (10 kHz) (V_{in} = 5 mV)	–	40	46	–	dB
Filter Output Voltage	11	1.8	2.0	2.5	Vdc
Trigger Hysteresis	–	–	100	–	mV
Mute Function Low	14	–	15	50	Ω
Mute Function High	14	1.0	10	–	MΩ
Scan Function Low (Mute Off) (V_{12} = 2 Vdc)	13	–	0	0.5	Vdc
Scan Function High (Mute On) (V_{12} = Gnd)	13	5.0	–	–	Vdc
Mixer Conversion Gain	3	–	20	–	dB
Mixer Input Resistance	16	–	3.3	–	kΩ
Mixer Input Capacitance	16	–	2.2	–	pF

FIGURE 2 – TEST CIRCUIT



CIRCUIT DESCRIPTION

The MC3357 is a low power FM IF circuit designed primarily for use in voice communication scanning receivers.

The mixer-oscillator combination converts the input frequency (e.g., 10.7 MHz) down to 455 kHz, where, after external bandpass filtering, most of the amplification is done. The audio is recovered using a conventional quadrature FM detector. The absence of an input signal is indicated by the presence of noise above the desired audio frequencies. This "noise band" is monitored by an active filter and a detector. A squelch trigger circuit indicates the presence of noise (or a tone) by an output which can be used to control scanning. At the same time, an internal switch is operated which can be used to mute the audio.

The oscillator is an internally-biased Colpitts type with the collector, base, and emitter connections at Pins 4, 1, and 2 respectively. A crystal can be used in place of the usual coil.

The mixer is doubly-balanced to reduce spurious responses. The input impedance at Pin 16 is set by a 3.0 kΩ internal biasing resistor and has low capacitance, allowing the circuit to be preceded by a crystal filter. The collector output at Pin 3 must be dc connected to B+, below which it can swing 0.5 V.

After suitable bandpass filtering (ceramic or LC) the signal goes to the input of a five-stage limiter at Pin 5. The output of the limiter at Pin 7 drives a multiplier, both internally directly, and externally through a quadrature coil, to detect the FM. The output at Pin 7 is also used to supply dc feedback to Pin 5. The other side of the first limiter stage is decoupled at Pin 6.

The recovered audio is partially filtered, then buffered giving an impedance of around 400 Ω at Pin 9. The signal still requires de-emphasis, volume control and further amplification before driving a loudspeaker.

A simple inverting op amp is provided with an output at Pin 11 providing dc bias (externally) to the input at Pin 10 which is referred internally to 2.0 V. A filter can be made with external impedance elements to discriminate between frequencies. With an external AM detector the filtered audio signal can be checked for the presence of noise above the normal audio band, or a tone signal. This information is applied to Pin 12.

An external positive bias to Pin 12 sets up the squelch trigger circuit such that Pin 13 is low at an impedance level of around 60 kΩ, and the audio mute (Pin 14) is open circuit. If Pin 12 is pulled down to 0.7 V by the noise or tone detector, Pin 13 will rise to approximately 0.5 Vdc below supply where it can support a load current of around 500 μA and Pin 14 is internally short-circuited to ground. There is 100 mV of hysteresis at Pin 12 to prevent jitter. Audio muting is accomplished by connecting Pin 14 to a high-impedance ground-reference point in the audio path between Pin 9 and the audio amplifier.

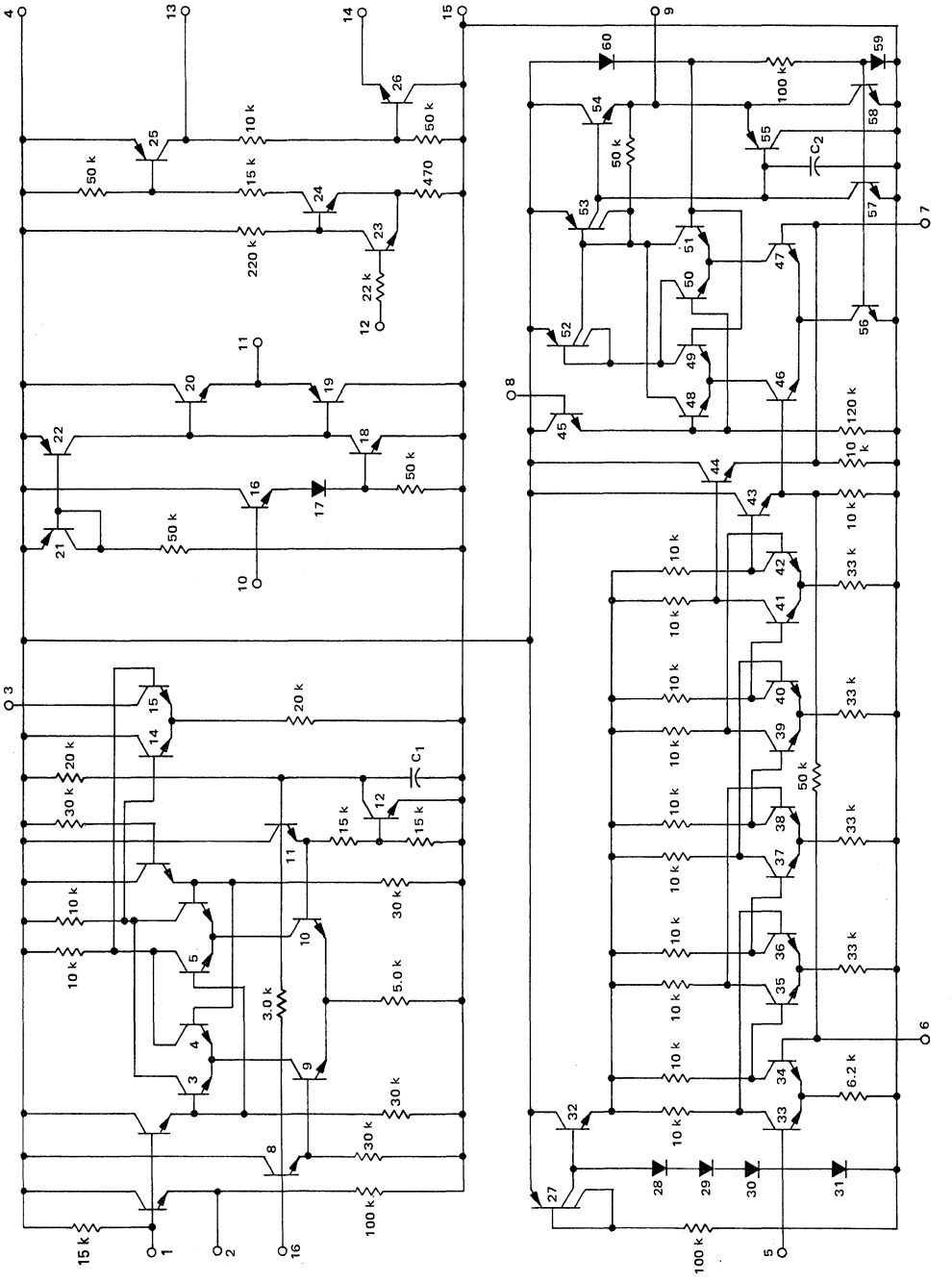


FIGURE 3 – CIRCUIT SCHEMATIC

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC3359

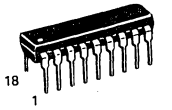
HIGH GAIN LOW POWER FM IF

SILICON MONOLITHIC INTEGRATED CIRCUIT

LOW POWER NARROWBAND FM IF

. . . includes oscillator, mixer, limiting amplifier, AFC, quadrature discriminator, op/amp, squelch, scan control, and mute switch. The MC3359 is designed to detect narrowband FM signals using a 455 kHz ceramic filter for use in FM dual conversion communications equipment. The MC3359 is similar to the MC3357 except that the MC3359 has an additional limiting IF stage, an AFC output, and an opposite polarity Broadcast Detector. The MC3359 also requires fewer external parts. For low cost applications requiring V_{CC} below 6.0 V, the MC3361BP,BD are recommended. For applications requiring a fixed, tuned, ceramic quadrature resonator, use the MC3357. For applications requiring dual conversion and RSSI, refer to these devices; MC3335, MC3362 and MC3363.

- Low Drain Current: 3.6 mA (Typ) @ V_{CC} = 6.0 Vdc
- Excellent Sensitivity: Input Limiting Voltage — −3.0 dB = 2.0 μV (Typ)
- Low Number of External Parts Required
- For Low Voltage and RSSI, use the MC3371



P SUFFIX
PLASTIC PACKAGE
CASE 707

DW SUFFIX
PLASTIC PACKAGE
CASE 751D
(SO-20L)

FIGURE 1 — TYPICAL APPLICATION IN A SCANNER RECEIVER

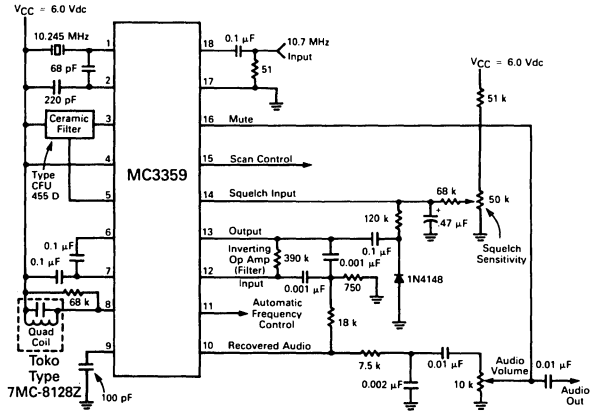
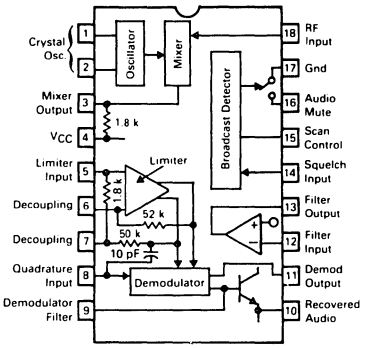
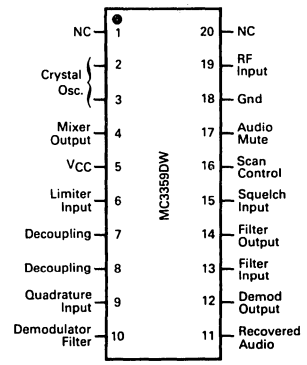


FIGURE 2 — PIN CONNECTIONS AND FUNCTIONAL BLOCK DIAGRAM



CASE 707



CASE 751D

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MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted)

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage	4	V_{CC}(max)	12	Vdc
Operating Supply Voltage Range	4	V_{CC}	6 to 9	Vdc
Input Voltage (V_{CC} ≥ 6.0 Volts)	18	V_{18}	1.0	V_{rms}
Mute Function	16	V_{16}	−0.7 to 12	V_{pk}
Junction Temperature	—	T_J	150	°C
Operating Ambient Temperature Range	—	T_A	−30 to +70	°C
Storage Temperature Range	—	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 6.0 Vdc, f_o = 10.7 MHz, Δf = ±3.0 kHz, f_{mod} = 1.0 kHz, 50 Ω source, T_A = 25°C test circuit of Figure 3, unless otherwise noted)

Characteristics		Min	Typ	Max	Units
Drain Current (Pins 4 and 8)	Squelch Off Squelch On	— —	3.6 5.4	6.0 7.0	mA
Input for 20 dB Quieting		—	8.0	—	μVrms
Input for −3.0 dB Limiting		—	2.0	—	μVrms
Mixer Voltage Gain (Pin 18 to Pin 3, Open)		—	46	—	
Mixer Third Order Intercept, 50 Ω Input		—	−1.0	—	dBm
Mixer Input Resistance		—	3.6	—	kΩ
Mixer Input Capacitance		—	2.2	—	pF
Recovered Audio, Pin 10 (Input Signal 1.0 mVrms)		450	700	—	mVrms
Detector Center Frequency Slope, Pin 10		—	0.3	—	V/kHz
AFC Center Slope, Pin 11, Unloaded		—	12	—	V/kHz
Filter Gain (test circuit of Figure 3)		40	51	—	dB
Squelch Threshold, Through 10K to Pin 14		—	0.62	—	Vdc
Scan Control Current, Pin 15	Pin 14 — High — Low	— 2.0	0.01 2.4	1.0 —	μA mA
Mute Switch Impedance Pin 16 to Ground	Pin 14 — High — Low	—	5.0 1.5	10 —	Ω MΩ

8

FIGURE 3 — TEST CIRCUIT

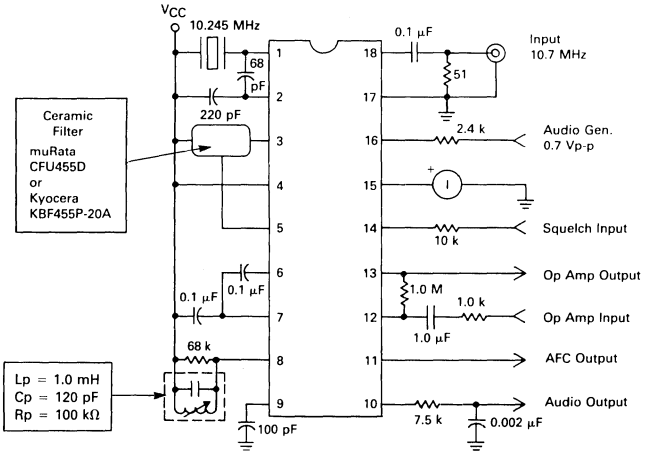

FIGURE 4 — MIXER VOLTAGE GAIN

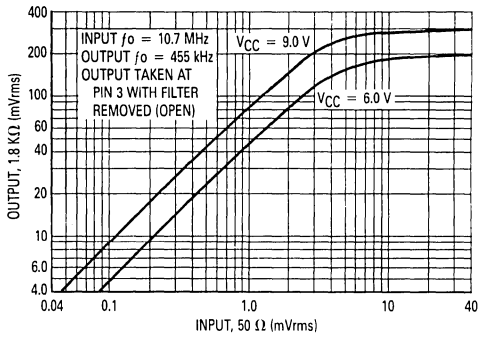

FIGURE 5 — LIMITING I.F. FREQUENCY RESPONSE

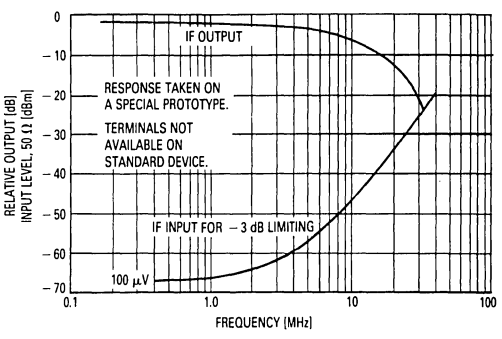

FIGURE 6 — MIXER THIRD ORDER INTERMODULATION PERFORMANCE

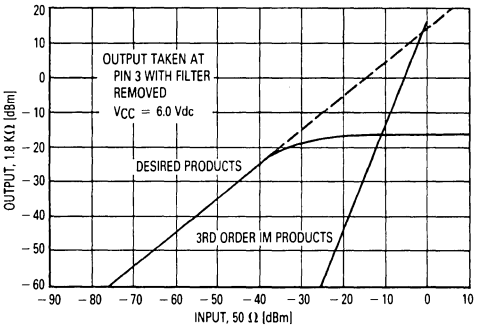

FIGURE 7 — DETECTOR AND AFC RESPONSES

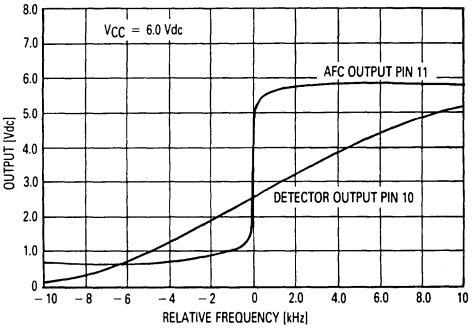

FIGURE 8 — RELATIVE MIXER GAIN

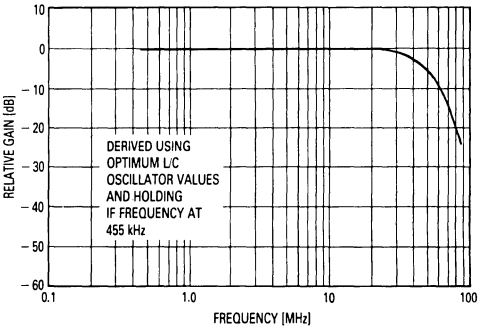

FIGURE 9 — OVERALL GAIN, NOISE, AND A.M. REJECTION

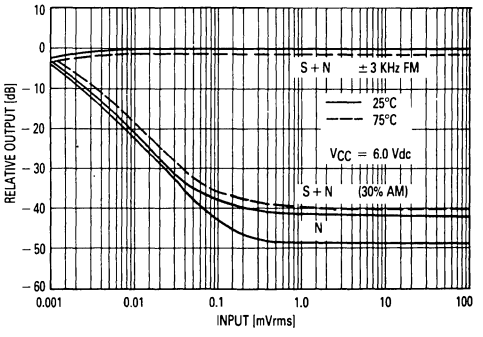

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FIGURE 10 — OUTPUT COMPONENTS OF SIGNAL, NOISE, AND DISTORTION

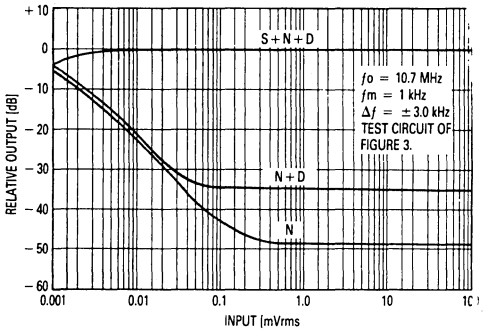


FIGURE 11 — AUDIO OUTPUT AND TOTAL CURRENT DRAIN versus SUPPLY VOLTAGE

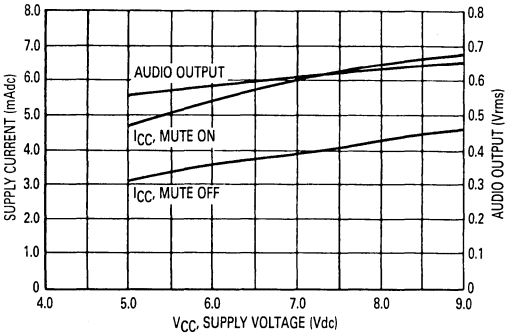


FIGURE 12 — L/C OSCILLATOR, TEMPERATURE AND POWER SUPPLY SENSITIVITY

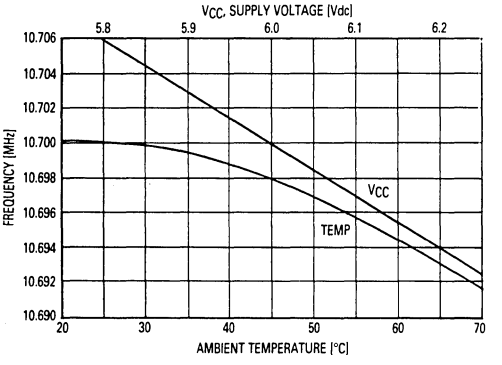


FIGURE 13 — OP AMP GAIN AND PHASE RESPONSE

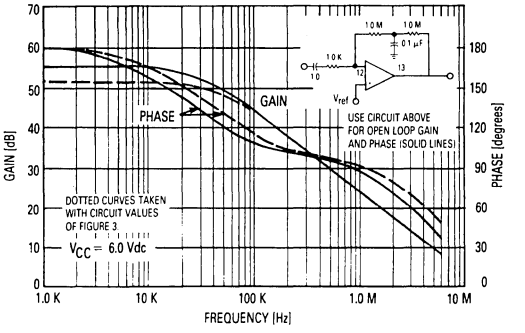


FIGURE 14 — L/C OSCILLATOR RECOMMENDED COMPONENT VALUES

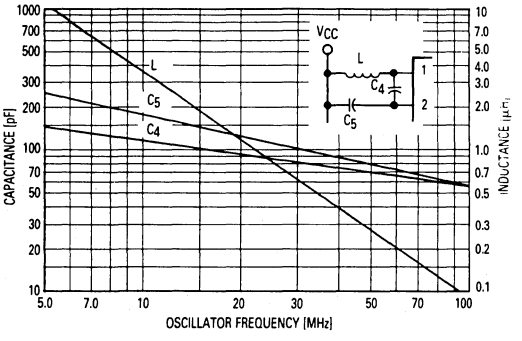
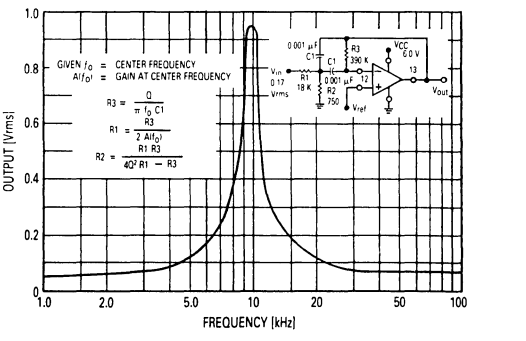


FIGURE 15 — THE OP AMP AS A BANDPASS FILTER



8

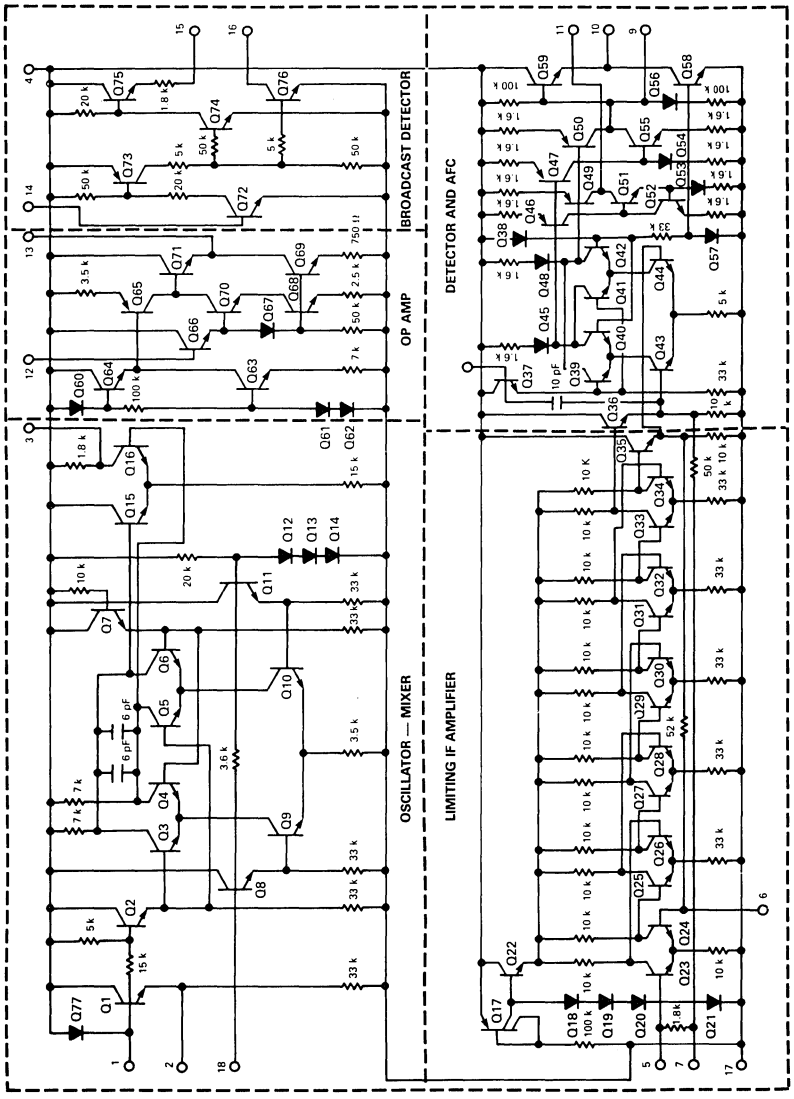


FIGURE 16 — CIRCUIT SCHEMATIC

CIRCUIT DESCRIPTION

The MC3359 is a low-power FM IF circuit designed primarily for use in voice-communication scanning receivers. It is also finding a place in narrowband data links.

In the typical application (Figure 1), the mixer-oscillator combination converts the input frequency (10.7 MHz) down to 455 kHz, where, after external bandpass filtering, most of the amplification is done. The audio is recovered using a conventional quadrature FM detector. The absence of an input signal is indicated by the presence of noise above the desired audio frequencies. This "noise band" is monitored by an active filter and a detector. A squelch-trigger circuit indicates the presence of noise (or a tone) by an output which can be used to control scanning. At the same time, an internal switch is operated which can be used to mute the audio.

APPLICATION

The oscillator is an internally biased Colpitts type with the collector, base, and emitter connections at Pin 4, 1, and 2, respectively. The crystal is used in fundamental mode, calibrated for parallel resonance at 32 pF load capacitance. In theory this means that the two capacitors in series should be 32 pF, but in fact much larger values do not significantly affect the oscillator frequency, and provide higher oscillator output.

The oscillator can also be used in the conventional L/C Colpitts configuration without loss of mixer conversion gain. This oscillator is, of course, much more sensitive to voltage and temperature as shown in Figure 12. Guidelines for choosing L and C values are given in Figure 14.

The mixer is doubly balanced to reduce spurious responses. The mixer measurements of Figure 4 and 6 were made using an external 50 Ω source and the internal 1.8 k at Pin 3. Voltage gain curves at several V_{CC} voltages are shown in Figure 4. The Third Order Intercept curves of Figure 6 are shown using the conventional dBm scales. Measured power gain (with the 50 Ω input) is approximately 18 dB but the useful gain is much higher because the mixer input impedance is over 3 kΩ. Most applications will use a 330 Ω 10.7 MHz crystal filter ahead of the mixer. For higher frequencies, the relative mixer gain is given in Figure 8.

Following the mixer, a ceramic bandpass filter is recommended. The 455 kHz types come in bandwidths from ±2 kHz to ±15 kHz and have input and output impedances of 1.5 k to 2.0 k. For this reason, the Pin 5 input to the 6 stage limiting IF has an internal 1.8 k resistor. The IF has a 3 dB limiting sensitivity of approximately 100 μV at Pin 5 and a useful frequency range of about 5 MHz as shown in Figure 5. The frequency limitation is due to the high resistance values in the IF, which were necessary to meet the low power requirement. The output of the limiter is internally connected to the quadrature detector, including the 10 pF quadrature capacitor. Only a parallel L/C is needed externally from Pin 8 to V_{CC}. A shunt resistance can be added to widen the peak separation of the quadrature detector.

The detector output is amplified and buffered to the audio output, Pin 10, which has an output impedance of approximatley 300 Ω. Pin 9 provides a high impedance (50 k) point in the output amplifier for application of a filter or de-emphasis capacitor. Pin 11 is the AFC output, with high gain and high output impedance (1 M). If not needed, it should be grounded, or it can be connected to Pin 9 to double the recovered audio. The detector and AFC responses are shown in Figure 7.

Overall performance of the MC3359 from mixer input to audio output is shown in Figure 9 and 10. The MC3359 can also be operated in "single conversion" equipment; i.e., the mixer can be used as a 455 kHz amplifier. The oscillator is disabled by connecting Pin 1 to Pin 2. In this mode the overall performance is identical to the 10.7 MHz results of Figure 9.

A simple inverting op amp is provided with an output at Pin 13 providing dc bias (externally) to the input at Pin 12, which is referred internally to 2.0 V. A filter can be made with external impedance elements to discriminate between frequencies. With an external AM detector, the filtered audio signal can be checked for the presence of either noise above the normal audio, or a tone signal.

The open loop response of this op amp is given in Figure 13. Bandpass filter design information is provided in Figure 15.

A low bias to Pin 14 sets up the squelch-trigger circuit such that Pin 15 is high, a source of at least 2.0 mA, and the audio mute (Pin 16) is open-circuit. If Pin 14 is raised to 0.7 V by the noise or tone detector, Pin 15 becomes open circuit and Pin 16 is internally short circuited to ground. There is no hysteresis. Audio muting is accomplished by connecting Pin 16 to a high-impedance ground-reference point in the audio path between Pin 10 and the audio amplifier. No dc voltage is needed, in fact it is not desirable because audio "thump" would result during the muting function. Signal swing greater than 0.7 V below ground on Pin 16 should be avoided.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC3361B

Advance Information

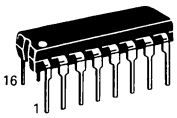
LOW POWER FM IF

SILICON MONOLITHIC INTEGRATED CIRCUIT

LOW POWER NARROWBAND FM IF

The MC3361B includes an Oscillator, Mixer, Limiting Amplifier, Quadrature Discriminator, Active Filter, Squelch, Scan Control, and Mute Switch. This device is designed for use in FM dual conversion communications equipment.

- Operates From 2.0 V to 8.0 V Supply
- Low Drain Current 3.9 mA Typ @ V_{CC} = 4.0 Vdc
- Excellent Sensitivity: Input Limiting Voltage — −3.0 dB = 2.6 μV Typ
- Low Number of External Parts Required
- Operating Frequency Up to 60 MHz

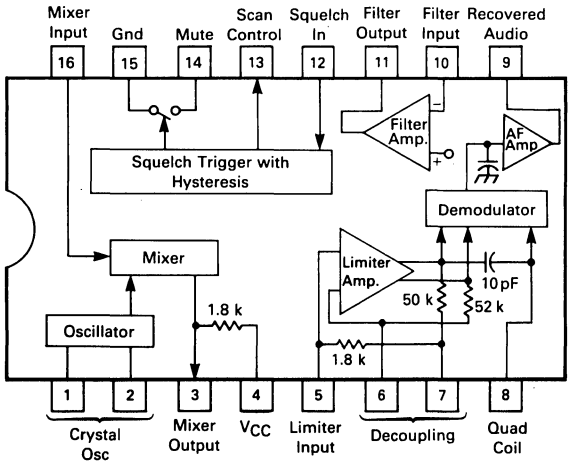


P SUFFIX
PLASTIC PACKAGE
CASE 648

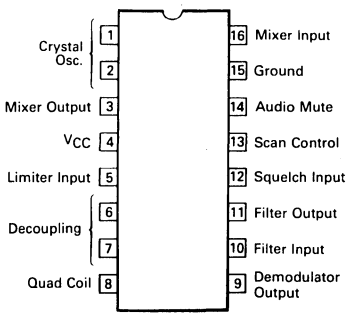
D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO-16)

8

FIGURE 1 — FUNCTIONAL BLOCK DIAGRAM



PIN CONNECTIONS



ORDERING INFORMATION

MC3361BD	−30° to +70°C	SO-16
MC3361BP		Plastic DIP

MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted)

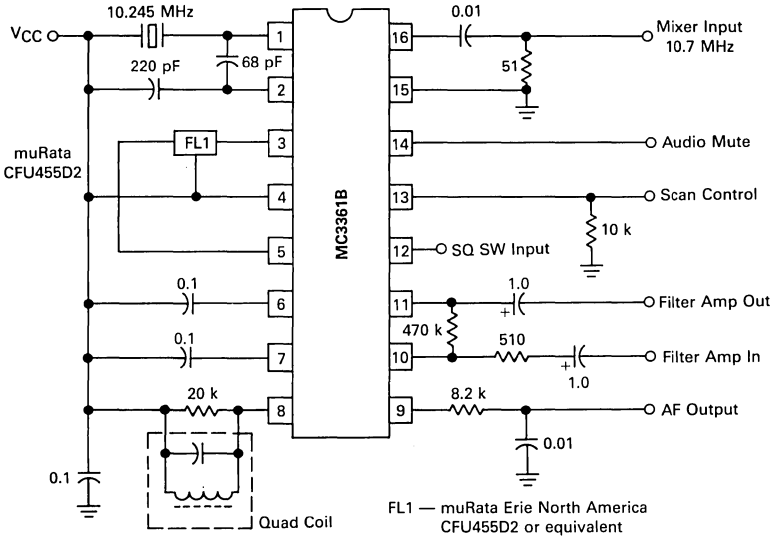
Rating	Pin	Symbol	Value	Unit
Power Supply Voltage	4	V_{CC}(max)	10	Vdc
Operating Supply Voltage Range	4	V_{CC}	2.0 to 8.0	Vdc
Detector Input Voltage	8	—	1.0	Vp-p
Input Voltage ($V_{CC} \geq$ 4.0 Volts)	16	V_{16}	1.0	V_{RMS}
Mute Function	14	V_{14}	−0.5 to +5.0	V_{pk}
Junction Temperature	—	T_J	150	°C
Operating Ambient Temperature Range	—	T_A	−30 to +70	°C
Storage Temperature Range	—	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 4.0 Vdc, f_o = 10.7 MHz, Δf = ±3.0 kHz, f_{mod} = 1.0 kHz, T_A = 25°C, unless otherwise noted.)

Characteristic	Pin	Min	Typ	Max	Unit
Drain Current (No Signal)	4				mA
Squelch Off		2.9	3.9	4.9	
Squelch On		4.4	5.4	6.4	
Recovered Audio Output Voltage (V_{in} = 10 mV_{RMS})	9	130	160	200	mV_{RMS}
Input Limiting Voltage (−3.0 dB Limiting)	16	—	2.6	6.0	μV
Total Harmonic Distortion	9	—	0.86	—	%
Recovered Output Voltage (No Input Signal)	9	60	120	250	mV_{RMS}
Drop Voltage AF Gain Loss	9	−3.0	−0.6	—	dB
Detector Output Impedance	—	—	450	—	Ω
Filter Gain (10 kHz) (V_{in} = 0.3 mV_{RMS})	—	40	50	—	dB
Filter Output Voltage	11	1.0	1.3	1.6	Vdc
Mute Function Low	14	—	30	50	Ω
Mute Function High	14	1.0	11	—	MΩ
Scan Function Low (Mute Off) (V_{12} = 1.0 Vdc)	13	—	0	0.4	Vdc
Scan Function High (Mute On) (V_{12} = Gnd)	13	3.0	3.5	—	Vdc
Trigger Hysteresis	—	—	45	100	mV
Mixer Conversion Gain	3	—	28	—	dB
Mixer Input Resistance	16	—	3.3	—	kΩ
Mixer Input Capacitance	16	—	2.2	—	pF

8

FIGURE 2 — TEST CIRCUIT



FL1 — muRata Erie North America CFU455D2 or equivalent

Quadrature Coil — Toko America Type 7MC-8128Z or equivalent

C — μF, unless noted

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FIGURE 3 — AUDIO OUTPUT, DISTORTION versus SUPPLY VOLTAGE

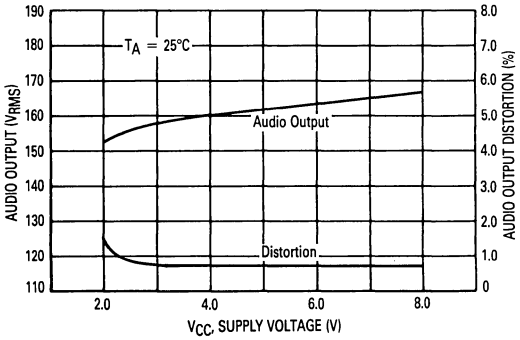


FIGURE 4 — AUDIO OUTPUT, DISTORTION versus TEMPERATURE

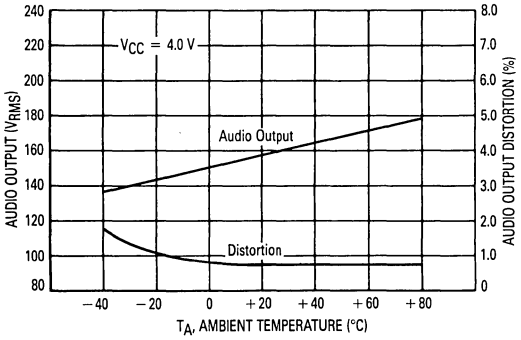
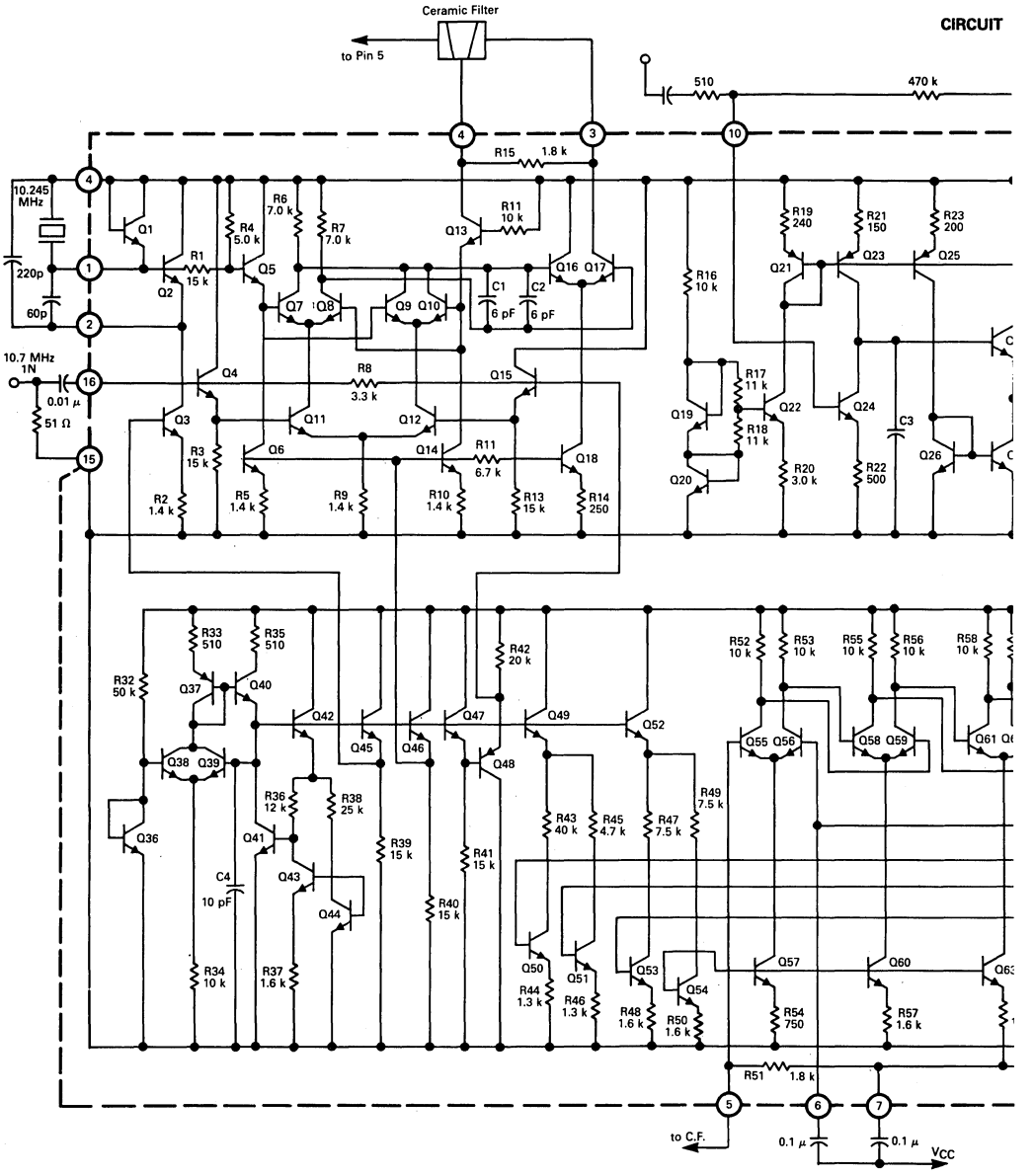


FIGURE 5 — LOW NARROW CIRCUIT



VOLTAGE LOW POWER BAND FM IF

SCHEMATIC

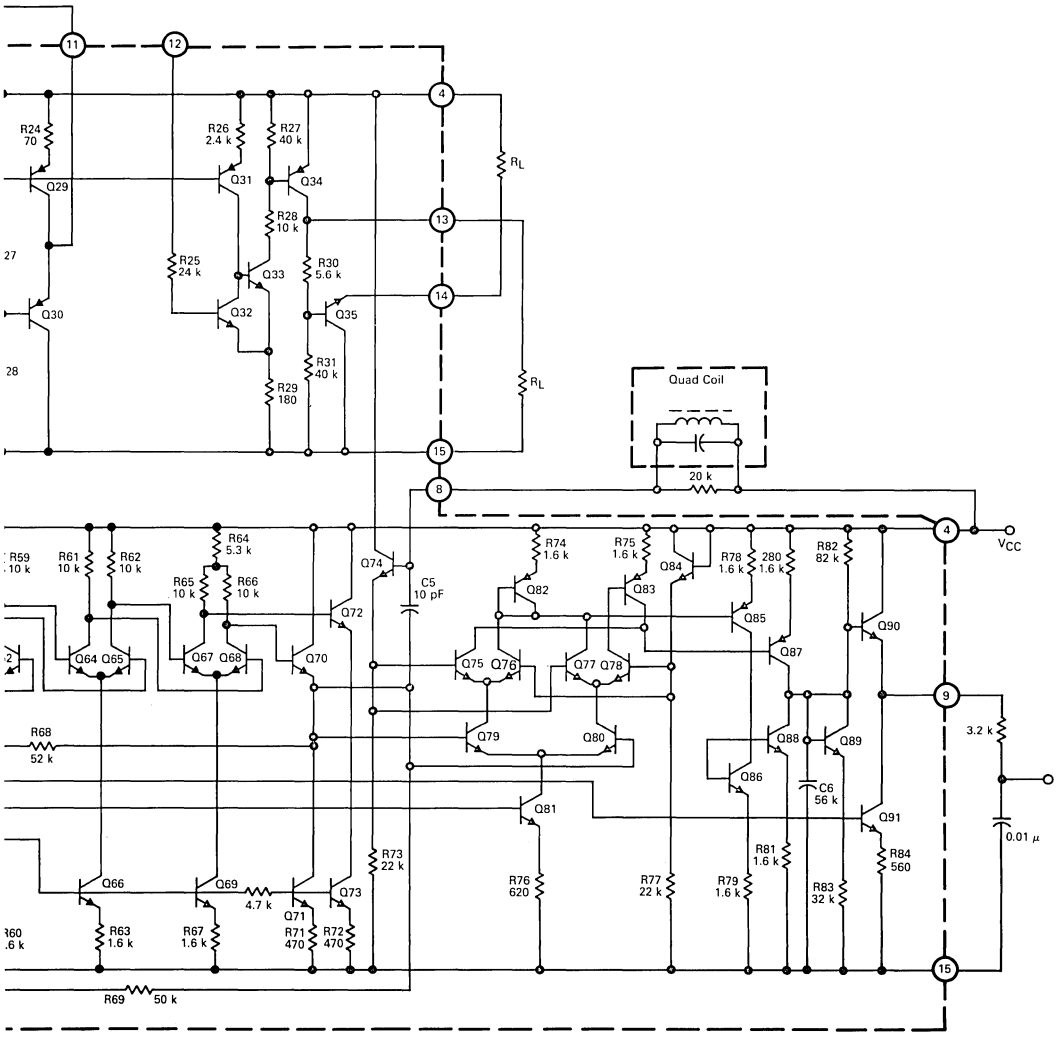


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FIGURE 6 — INPUT LIMITING VOLTAGE

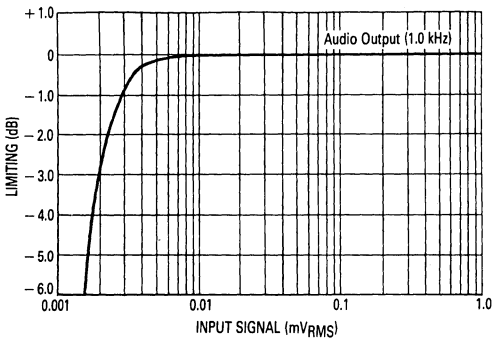


FIGURE 7 — OVERALL GAIN, NOISE, AND AM REJECTION

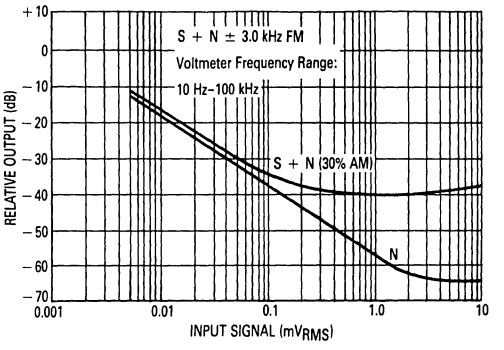


FIGURE 8 — FILTER AMP RESPONSE

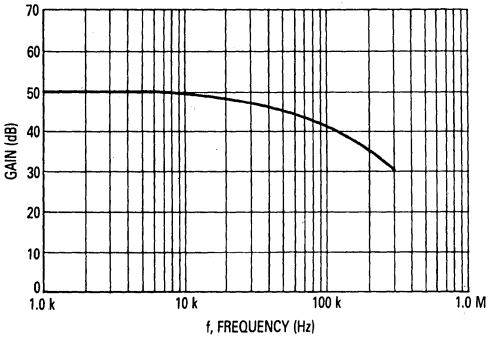


FIGURE 9 — FILTER AMP GAIN

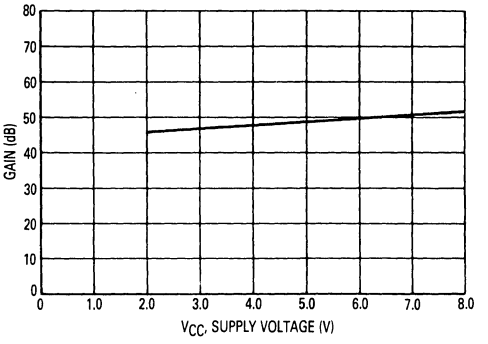


FIGURE 10 — SUPPLY CURRENT

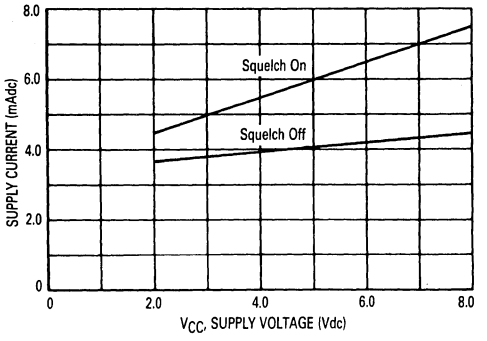
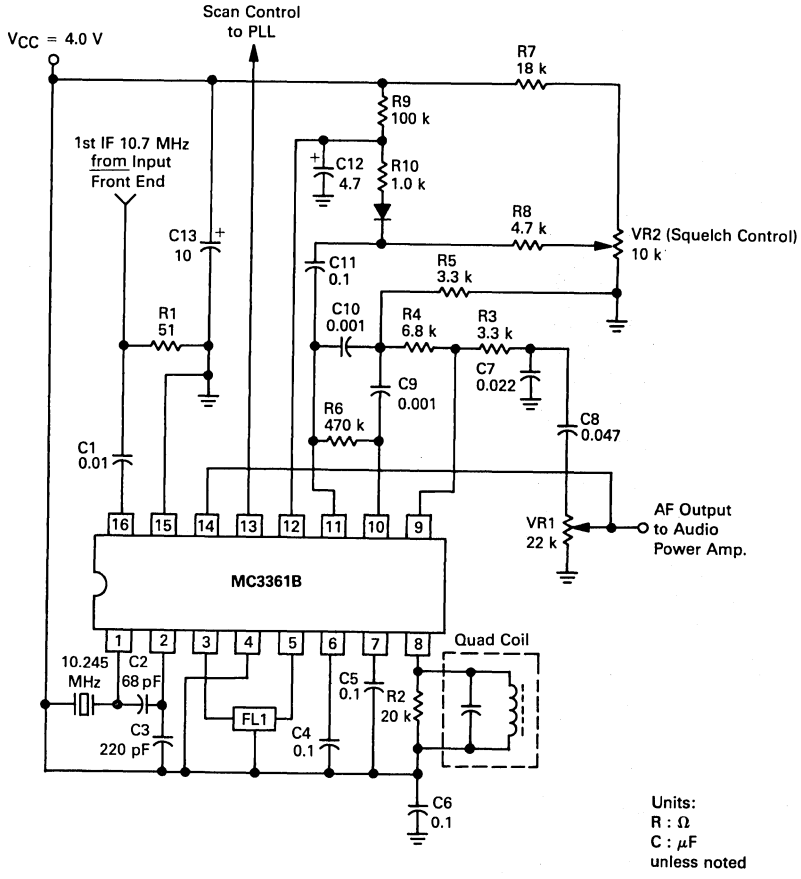


FIGURE 11 — TYPICAL APPLICATION



FL1 — muRata Erie North America
Type CFU455D2 or equivalent

Quadrature Coil — Toko America
Type 7MC-8128Z or equivalent

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MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC3362

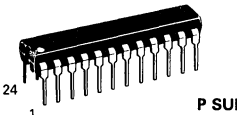
LOW-POWER DUAL CONVERSION FM RECEIVER

SILICON MONOLITHIC INTEGRATED CIRCUIT

LOW-POWER NARROWBAND FM RECEIVER

. . . includes dual FM conversion with oscillators, mixers, quadrature discriminator, and meter drive/carrier detect circuitry. The MC3362 also has buffered first and second local oscillator outputs and a comparator circuit for FSK detection.

- Complete Dual Conversion Circuitry
- Low Voltage: V_{CC} = 2.0 to 6.0 Vdc
- Low Drain Current (3.6 mA (Typ) @ V_{CC} = 3.0 Vdc)
- Excellent Sensitivity: Input Voltage 0.6 μVrms (Typ) for 12 dB SINAD
- Externally Adjustable Carrier Detect Function
- Low Number of External Parts Required
- Manufactured Using Motorola's MOSAIC® Process Technology
- MC13135 is Preferred for New Designs



P SUFFIX
PLASTIC PACKAGE
CASE 724

DW SUFFIX
PLASTIC PACKAGE
CASE 751E
(SO-24L)

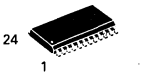


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FIGURE 1 — TYPICAL APPLICATION IN A PLL FREQUENCY SYNTHESIZED RECEIVER

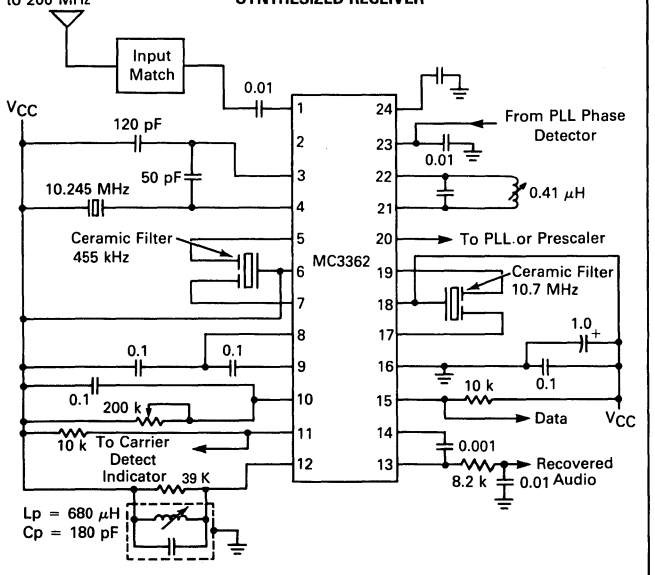
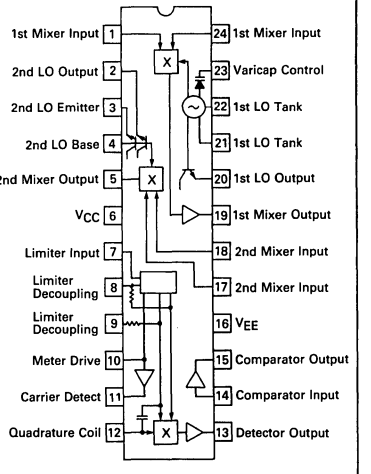


FIGURE 2 — PIN CONNECTIONS AND FUNCTIONAL BLOCK DIAGRAM



MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted)

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage (See Diagram)	6	$V_{CC(max)}$	7.0	Vdc
Operating Supply Voltage Range (Recommended)	6	V_{CC}	2.0 to 6.0	Vdc
Input Voltage ($V_{CC} \geq$ 5.0 Vdc)	1, 24	V_{1-24}	1.0	Vrms
Junction Temperature	—	T_J	150	°C
Operating Ambient Temperature Range	—	T_A	−40 to +85	°C
Storage Temperature Range	—	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc, f_o = 49.7 MHz, Deviation = 3.0 kHz, T_A = 25°C, Test Circuit of Figure 3 unless otherwise noted)

Characteristic	Pin	Min	Typ	Max	Units
Drain Current (Carrier Detect Low — See Figure 5)	6	—	4.5	7.0	mA
Input for −3.0 dB Limiting		—	0.7	2.0	μVrms
Input for 12 dB SINAD (See Figure 9)		—	0.6	—	μVrms
Series Equivalent Input Impedence		—	450−j350	—	Ω
Recovered Audio (RF signal level = 10 mV)	13	—	350	—	mVrms
Noise Output (RF signal level = 0 mV)	13	—	250	—	mVrms
Carrier Detect Threshold (below V_{CC})	10	—	0.64	—	Vdc
Meter Drive Slope	10	—	100	—	nA/dB
Input for 20 dB (S + N)/N (See Figure 7)		—	0.7	—	μVrms
First Mixer 3rd Order Intercept (Input)		—	−22	—	dBm
First Mixer Input Resistance (Rp)		—	690	—	Ω
First Mixer Input Capacitance (Cp)		—	7.2	—	pF
Conversion Voltage Gain, First Mixer		—	18	—	dB
Conversion Voltage Gain, Second Mixer		—	21	—	
Dector Output Resistance	13	—	1.4	—	kΩ

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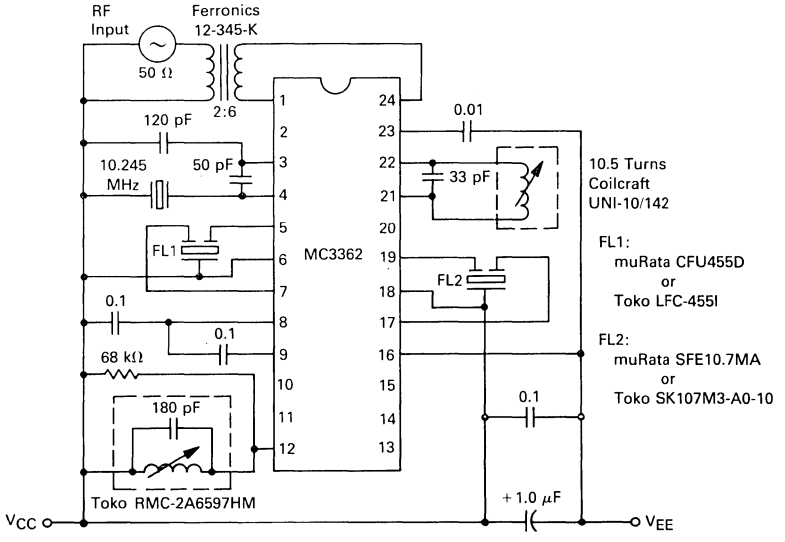
FIGURE 3 — TEST CIRCUIT



NOTE: See AN980 for Additional Design Information.

FIGURE 4 — I_{METER} versus INPUT

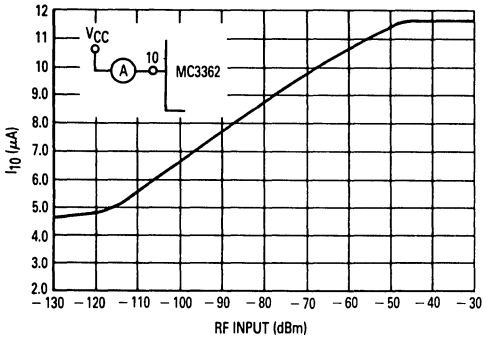


FIGURE 5 — DRAIN CURRENT, RECOVERED AUDIO versus SUPPLY

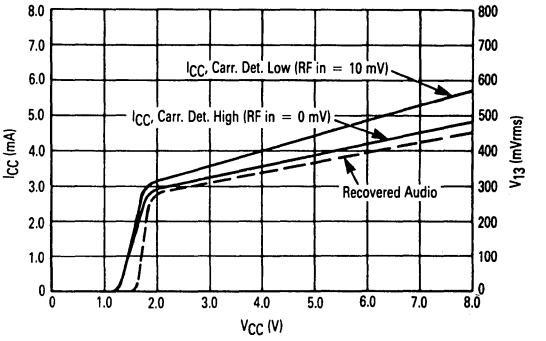


FIGURE 6 — SIGNAL LEVELS

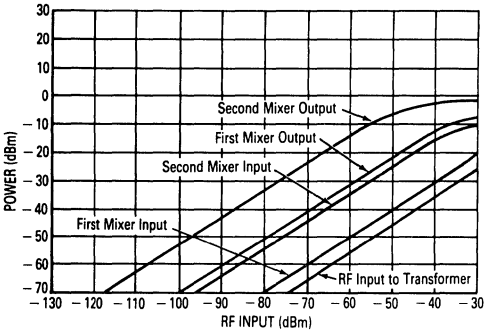


FIGURE 7 — S+N, N, AMR versus INPUT

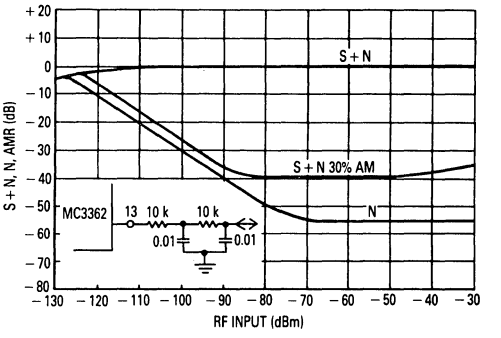


FIGURE 8 — 1ST MIXER 3RD ORDER INTERMODULATION

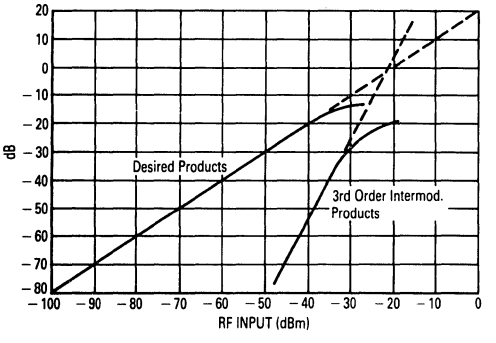


FIGURE 9 — DETECTOR OUTPUT versus FREQUENCY

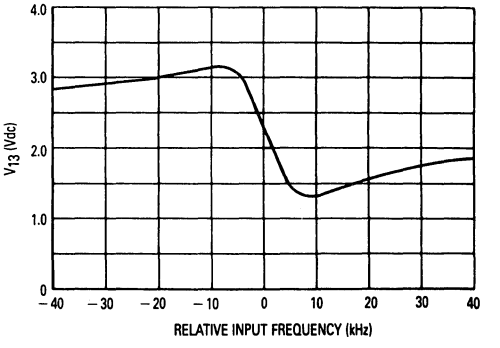


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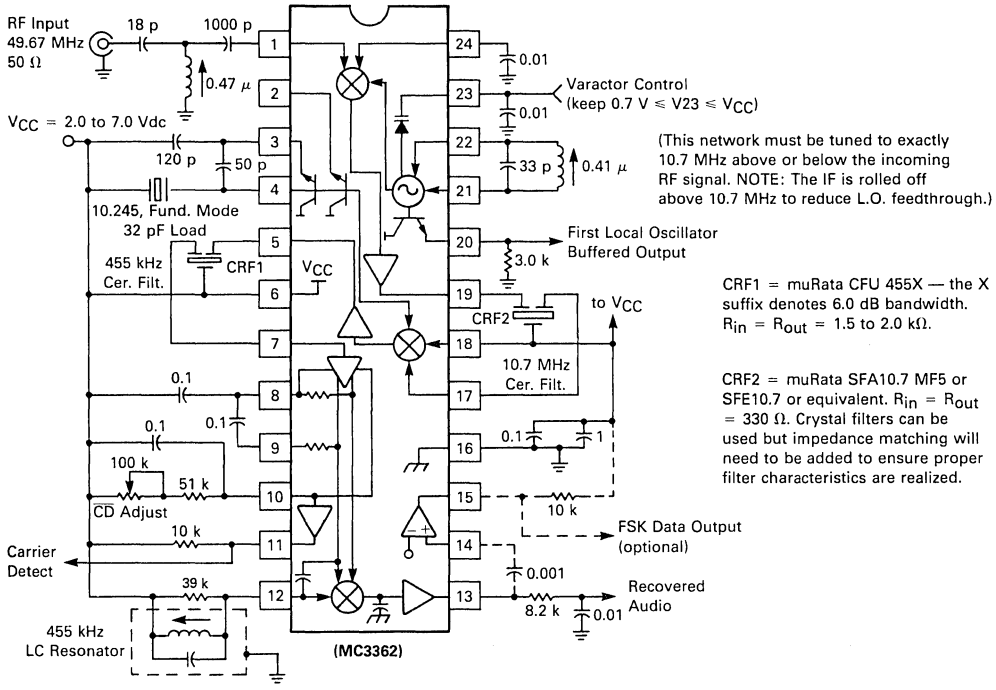
FIGURE 10 — PC BOARD TEST CIRCUIT
(LC Oscillator Configuration Used in PLL Synthesized Receiver)

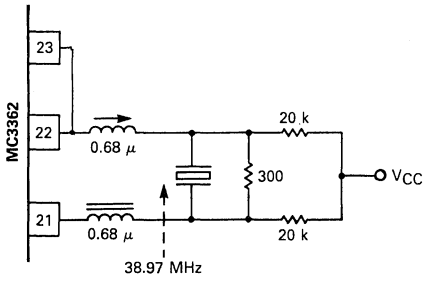


(This network must be tuned to exactly 10.7 MHz above or below the incoming RF signal. NOTE: The IF is rolled off above 10.7 MHz to reduce L.O. feedthrough.)

CRF1 = muRata CFU 455X — the X suffix denotes 6.0 dB bandwidth. R_{in} = R_{out} = 1.5 to 2.0 kΩ.

CRF2 = muRata SFA10.7 MF5 or SFE10.7 or equivalent. R_{in} = R_{out} = 330 Ω. Crystal filters can be used but impedance matching will need to be added to ensure proper filter characteristics are realized.

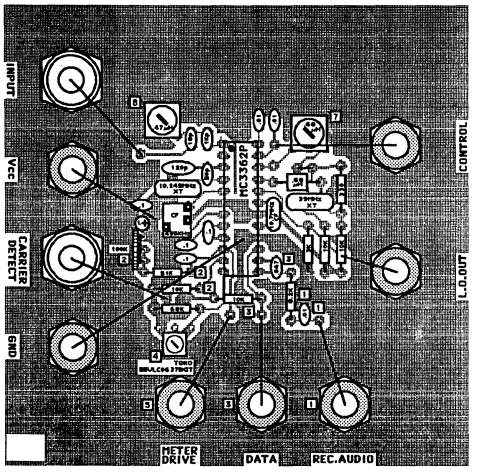
FIGURE 10A — CRYSTAL OSCILLATOR CONFIGURATION FOR SINGLE CHANNEL APPLICATION



Crystal used is series mode resonant (no load capacity specified), 3rd overtone. This method has not proven adequate for fundamental mode, 5th or 7th overtone crystals. The inductor and capacitor will need to be changed for other frequency crystals. See AN980 for further information.

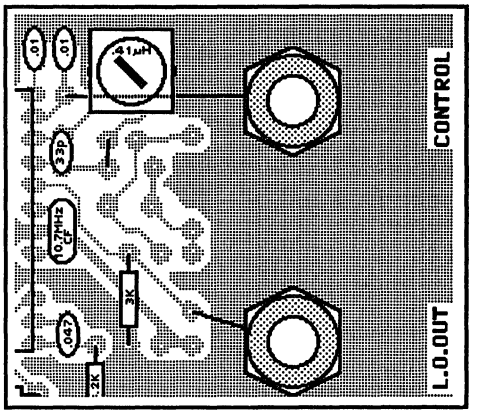
8

FIGURE 11 — COMPONENT PLACEMENT VIEW SHOWING CRYSTAL OSCILLATOR CIRCUIT



NOTES:
1. Recovered Audio components may be deleted when using data output.
2. Carrier Detect components must be deleted in order to obtain linear Meter Drive output. With these components in place the Meter Drive outputs serve only to trip the Carrier Detect indicator.
3. Data Output components should be deleted in applications where only audio modulation is used. For combined audio/data applications, the 0.047 μF coupling capacitor will add distortion to the audio, so a pull-down resistor at pin 13 may be required.
4. Use Toko 7MC81282 Quadrature coil.

FIGURE 11A — LC OSCILLATOR COMPONENT VIEW



5. Meter Drive cannot be used simultaneously with Carrier Detect output. For analog meter drive, remove components labelled "2" and measure meter current (4–12 μA) through ammeter to V_{CC}.
6. Either type of oscillator circuit may be used with any output circuit configuration.
7. LC Oscillator Coil: Coilcraft UNI 10/42 10.5 turns, 0.41 μH Crystal Oscillator circuit: trim coil, 0.68 μH. Coilcraft M1287–A.
8. 0.47 H, Coilcraft M1286-A. Input LC network used to match first mixer input impedance to 50 Ω.

8

CIRCUIT DESCRIPTION

The MC3362 is a complete FM narrowband receiver from antenna input to audio preamp output. The low voltage dual conversion design yields low power drain, excellent sensitivity and good image rejection in narrowband voice and data link applications.

In the typical application (Figure 1), the first mixer amplifies the signal and converts the RF input to 10.7 MHz. This IF signal is filtered externally and fed into the second mixer, which further amplifies the signal and converts it to a 455 kHz IF signal. After external bandpass filtering, the low IF is fed into the limiting amplifier and detection circuitry. The audio is recovered using a conventional quadrature detector. Twice-IF filtering is provided internally.

The input signal level is monitored by meter drive circuitry which detects the amount of limiting in the limiting amplifier. The voltage at the meter drive pin determines the state of the carrier detect output, which is active low.

APPLICATION

The first local oscillator can be run using a free-running LC tank, as a VCO using PLL synthesis, or driven from an external crystal oscillator. It has been run to 190 MHz.* A buffered output is available at Pin 20. The second local oscillator is a common base Colpitts type which is typically run at 10.245 MHz under crystal control. A buffered output is available at Pin 2. Pins 2 and 3 are interchangeable.

The mixers are doubly balanced to reduce spurious responses. The first and second mixers have conversion gains of 18 dB and 22 dB (typical), respectively, as seen in Figure 6. Mixer gain is stable with respect to supply voltage. For both conversions, the mixer impedances and pin layout are designed to allow the user to employ low cost, readily available ceramic filters. Overall sensitivity and AM rejection are shown in Figure 7. The input level for 20 dB (S+N)/N is 0.7 μV using the two-pole post-detection filter pictured.

*If the first local oscillator (Pins 21 and/or 22) is driven from a strong external source (100 mVrms), the mixer can be used to over 450 MHz.

Following the first mixer, a 10.7 MHz ceramic bandpass filter is recommended. The 10.7 MHz filtered signal is then fed into one second mixer input pin, the other input pin being connected to V_{CC}. Pin 6 (V_{CC}) is treated as a common point for emitter-driven signals.

The 455 kHz IF is typically filtered using a ceramic bandpass filter then fed into the limiter input pin. The limiter has 10 μV sensitivity for −3.0 dB limiting, flat to 1.0 MHz.

The output of the limiter is internally connected to the quadrature detector, including a quadrature capacitor. A parallel LC tank is needed externally from Pin 12 to V_{CC}. A 39 kΩ shunt resistance is included which determines the peak separation of the quadrature detector; a smaller value will increase the spacing and linearity but decrease recovered audio and sensitivity.

A data shaping circuit is available and can be coupled to the recovered audio output of Pin 13. The circuit is a comparator which is designed to detect zero crossings of FSK modulation. Data rates are typically limited to 1200 baud to ensure data integrity and avoid adjacent channel "splatter." Hysteresis is available by connecting a high valued resistor from Pin 15 to Pin 14. Values below 120 kΩ are not recommended as the input signal cannot overcome the hysteresis.

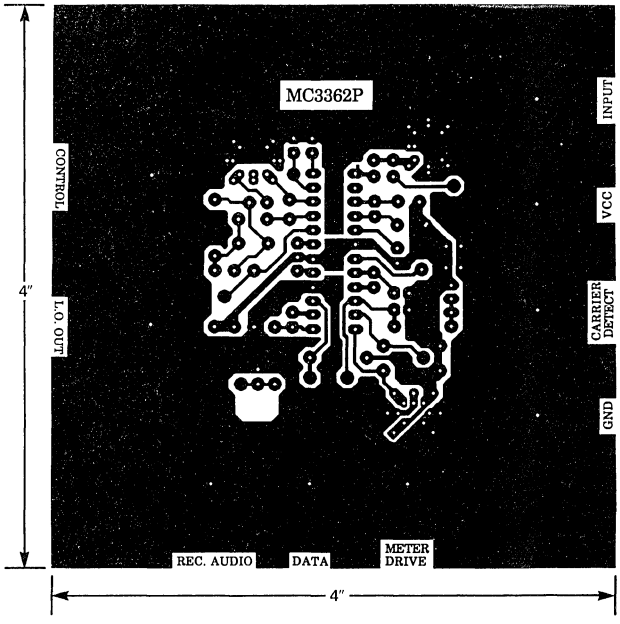
The meter drive circuitry detects input signal level by monitoring the limiting amplifier stages. Figure 4 shows the unloaded current at Pin 10 versus input power. The meter drive current can be used directly (RSSI) or can be used to trip the carrier detect circuit at a specified input power. To do this, pick an RF trip level in dBm. Read the corresponding current from Figure 4 and pick a resistor such that:

$$R_{10} \simeq 0.64\ \text{Vdc} / I_{10}$$

Hysteresis is available by connecting a high valued resistor R_H between Pins 10 and 11. The formula is:

$$\text{Hysteresis} = V_{CC}/(R_H \times 10^{-7})\ \text{dB}$$

FIGURE 12 — CIRCUIT SIDE VIEW



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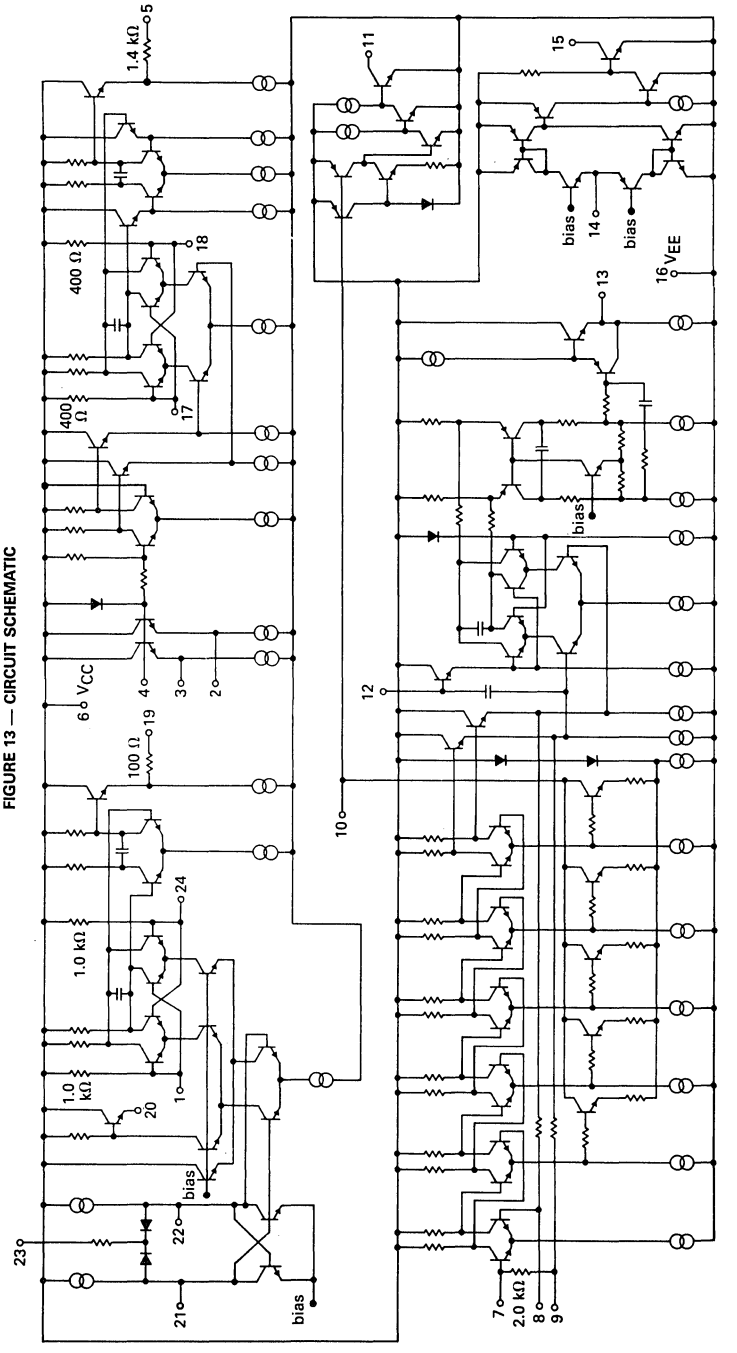

FIGURE 13 — CIRCUIT SCHEMATIC

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MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC3363

LOW POWER DUAL CONVERSION FM RECEIVER

LOW POWER DUAL CONVERSION FM RECEIVER

SILICON MONOLITHIC INTEGRATED CIRCUIT

The MC3363 is a single chip narrowband VHF FM radio receiver. It is a dual conversion receiver with RF amplifier transistor, oscillators, mixers, quadrature detector, meter drive/carrier detect and mute circuitry. The MC3363 also has a buffered first local oscillator output for use with frequency synthesizers, and a data slicing comparator for FSK detection.

- Wide Input Bandwidth — 200 MHz Using Internal Local Oscillator
  — 450 MHz Using External Local Oscillator
- RF Amplifier Transistor
- Muting Operational Amplifier
- Complete Dual Conversion
- Low Voltage: V_{CC} = 2.0 V to 6.0 Vdc
- Low Drain Current: I_{CC} = 3.6 mA (Typ) at V_{CC} = 3.0 V, Excluding RF Amplifier Transistor
- Excellent Sensitivity: Input 0.3 μV (Typ) for 12 dB SINAD Using Internal RF Amplifier Transistor
- Data Shaping Comparator
- Received Signal Strength Indicator (RSSI) with 60 dB Dynamic Range
- Low Number of External Parts Required
- Manufactured in Motorola's MOSAIC Process Technology

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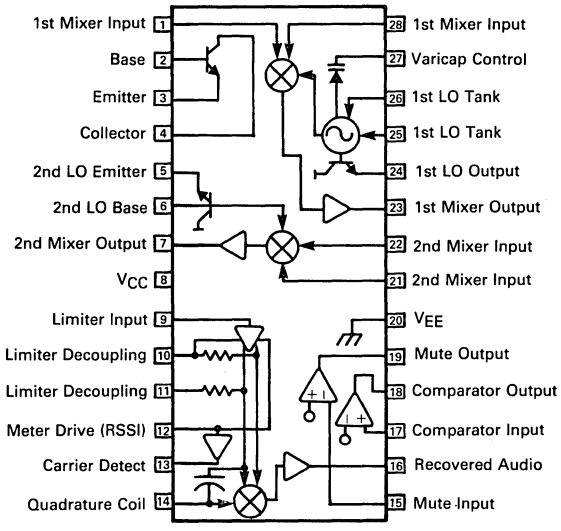
FIGURE 1 — PIN CONNECTIONS AND FUNCTIONAL BLOCK DIAGRAM



MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage	8	$V_{CC(max)}$	7.0	Vdc
Operating Supply Voltage Range (Recommended)	8	V_{CC}	2.0 to 6.0	Vdc
Input Voltage (V_{CC} = 5.0 Vdc)	1, 28	V_{1-28}	1.0	Vrms
Mute Output Voltage	19	V_{19}	−0.7 to 8.0	Vpk
Junction Temperature	—	T_J	150	°C
Operating Ambient Temperature Range	—	T_A	−40 to +85	°C
Storage Temperature Range	—	T_{stg}	−65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc, f_o = 49.7 MHz, Deviation = ±3.0 kHz, T_A = 25°C, Mod 1.0 kHz, test circuit of Figure 2 unless otherwise noted)

Characteristic	Pin	Min	Typ	Max	Units
Drain Current (Carrier Detect Low)	8	—	4.5	8.0	mA
−3.0 dB Limiting Sensitivity (RF Amplifier Not Used)		—	0.7	2.0	µVrms
Input For 12 dB SINAD		—	0.3	—	
20 dB S/N Sensitivity (RF Amplifier Not Used)		—	1.0	—	
1st Mister Input Resistance (Parallel — Rp)	1, 28	—	690	—	Ω
1st Mixer Input Capacitance (Parallel — Cp)	1, 28	—	7.2	—	pF
1st Mixer Conversion Voltage Gain (A_{vc1}, Open Circuit)		—	18	—	dB
2nd Mixer Conversion Voltage Gain)A_{vc2}, Open Circuit)		—	21	—	
2nd Mixer Input Sensitivity (20 dB S/N) (10.7 MHz i/p)	21	—	10	—	µVrms
Limiter Input Sensitivity (20 dB S/N) (455 kHz i/p)	9	—	100	—	
RF Transistor DC Current Drain	4	1.0	1.5	2.5	mAdc
Noise Output Level (RF Signal = 0 mV)	16	—	70	—	mVrms
Recovered Audio (RF Signal Level = 1.0 mV)	16	120	200	—	mVrms
THD of Recovered Aduio (RF Signal = 1.0 mV)	16	—	2%	—	%
Detector Output Impedance	16	—	400	—	Ω
Series Equivalent Input Impedence	1	—	450–j350	—	
Data (Comparator) Output Voltage — High — Low	18	— 0.1	— 0.1	V_{CC} —	Vdc
Data (Comparator) Threshold Voltage Difference	17	70	110	150	mV
Meter Drive Slope	12	70	100	135	nA/dB
Carrier Detect Threshold (Below V_{CC})	12	0.53	0.64	0.77	Vdc
Mute Output Impedance — High — Low	19	— —	10 25	— —	MΩ

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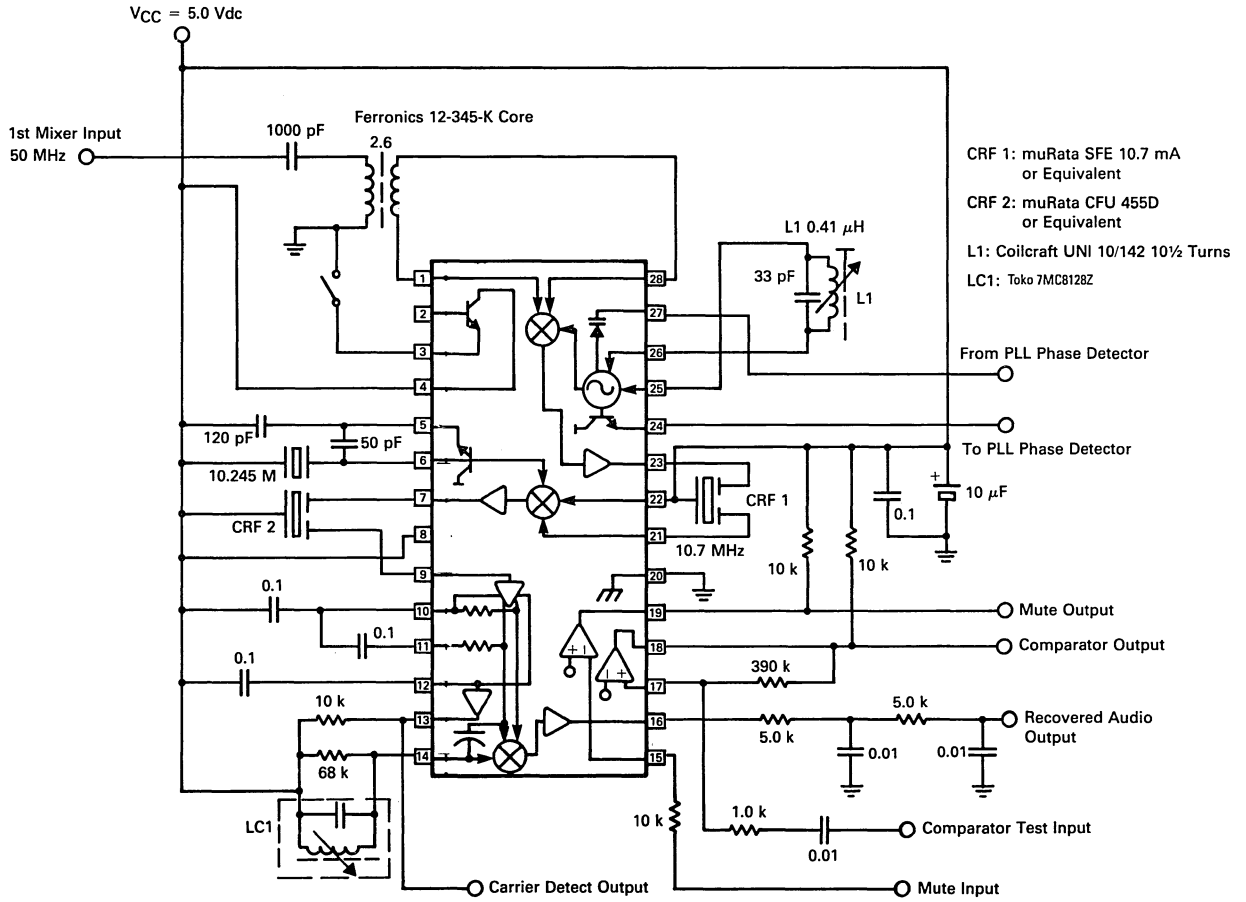
FIGURE 2 — TEST CIRCUIT



CIRCUIT DESCRIPTION

The MC3363 is a complete FM narrowband receiver from RF amplifier to audio preamp output. The low voltage dual conversion design yields low power drain, excellent sensitivity and good image rejection in narrowband voice and data link applications.

In the typical application, the input RF signal is amplified by the RF transistor and then the first mixer amplifies the signal and converts the RF input to 10.7 MHz. This IF signal is filtered externally and fed into the second mixer, which further amplifies the signal and converts it to a 455 kHz IF signal. After external bandpass filtering, the low IF is fed into the limiting amplifier and detection circuitry. The audio is recovered using a conventional quadrature detector. Twice-IF filtering is provided internally.

The input signal level is monitored by meter drive circuitry which detects the amount of limiting in the limiting amplifier. The voltage at the meter drive pin determines the state of the carrier detect output, which is active low.

APPLICATION

The first local oscillator is designed to serve as the VCO in a PLL frequency synthesized receiver. The MC3363 can operate together with the MC145166/7 to provide a two-chip ten channel frequency synthesized receiver in the 46/49 cordless telephone band. The MC3363 can also be used with the MC14515X series of CMOS PLL synthesizers and MC120XX series of ECL prescalers in VHF frequency synthesized applications to 200 MHz.

For single channel applications the first local oscillator can be crystal controlled. The circuit of Figure 4 has been used successfully up to 60 MHz. For higher frequencies an external oscillator signal can be injected into Pins 25 and/or 26 — a level of approximately 100 mVrms is recommended. The first mixer's transfer characteristic is essentially flat to 450 MHz when this approach is used (keeping a constant 10.7 MHz IF frequency). The second local oscillator is a Colpitts type which is typically run at 10.245 MHz under crystal control.

The mixers are doubly balanced to reduce spurious responses. The first and second mixers have conversion gains of 18 dB and 21 dB (typical), respectively. Mixer gain is stable with respect to supply voltage. For both conversions, the mixer impedances and pin layout are designed to allow the user to employ low cost, readily available ceramic filters.

Following the first mixer, a 10.7 MHz ceramic bandpass filter is recommended. The 10.7 MHz filtered signal is then fed into the second mixer input Pin 21, the other input Pin 22 being connected to V_{CC}.

The 455 kHz IF is filtered by a ceramic narrow bandpass filter then fed into the limiter input Pin 9. The limiter has 10 μV sensitivity for −3.0 dB limiting, flat to 1.0 MHz.

NOTE: For further application and design information, refer to AN980.

The output of the limiter is internally connected to the quadrature detector, including a quadrature capacitor. A parallel LC tank is needed externally from Pin 14 to V_{CC}. A 68 kOhm shunt resistance is included which determines the peak separation of the quadrature detector; a smaller value will lower the Q and expand the deviation range and linearity, but decrease recovered audio and sensitivity.

A data shaping circuit is available and can be coupled to the recovered audio output of Pin 16. The circuit is a comparator which is designed to detect zero crossings of FSK modulation. Data rates of up to 35000 baud are detectable using the comparator. Best sensitivity is obtained when data rates are limited to 1200 baud maximum. Hysteresis is available by connecting a high-valued resistor from Pin 17 to Pin 18. Values below 120 kOhm are not recommended as the input signal cannot overcome the hysteresis.

The meter drive circuitry detects input signal level by monitoring the limiting of the limiting amplifier stages. Figure 5 shows the unloaded current at Pin 12 versus input power. The meter drive current can be used directly (RSSI) or can be used to trip the carrier detect circuit at a specified input power.

A muting op amp is provided and can be triggered by the carrier detect output (Pin 13). This provides a carrier level triggered squelch circuit which is activated when the RF input at the desired input frequency falls below a preset level. The level at which this occurs is determined by the resistor placed between the meter drive output (Pin 12) and V_{CC}. Values between 80–130 kOhms are recommended. This type of squelch is pictured in Figures 3 and 4.

Hysteresis is available by connecting a high-valued resistor Rh between Pins 12 and 13. The formula is:

$$\text{Hyst} = V_{CC}/(\text{Rh} \times 10^{-7})\ \text{dB}$$

The meter drive can also be used directly to drive a meter or to provide AGC. A current to voltage converter or other linear buffer will be needed for this application.

A second possible application of the op amp would be in a noise triggered squelch circuit, similiar to that used with the MC3357/MC3359/MC3361B FM IFs. In this case the op amp would serve as an active noise filter, the output of which would be rectified and compared to a reference on a squelch gate. The MC3363 does not have a dedicated squelch gate, but the NPN RF input stage or data shaping comparator might be used to provide this function if available. The op amp is a basic type with the inverting input and the output available. This application frees the meter drive to allow it to be used as a linear signal strength monitor.

The circuit of Figure 4 is a complete 50 MHz receiver from antenna input to audio preamp output. It uses few components and has good performance. The receiver operates on a single channel and has input sensitivity of <0.3 μV for 12 dB SINAD.

FIGURE 3 — TYPICAL APPLICATION IN A PLL FREQUENCY SYNTHESIZED RECEIVER

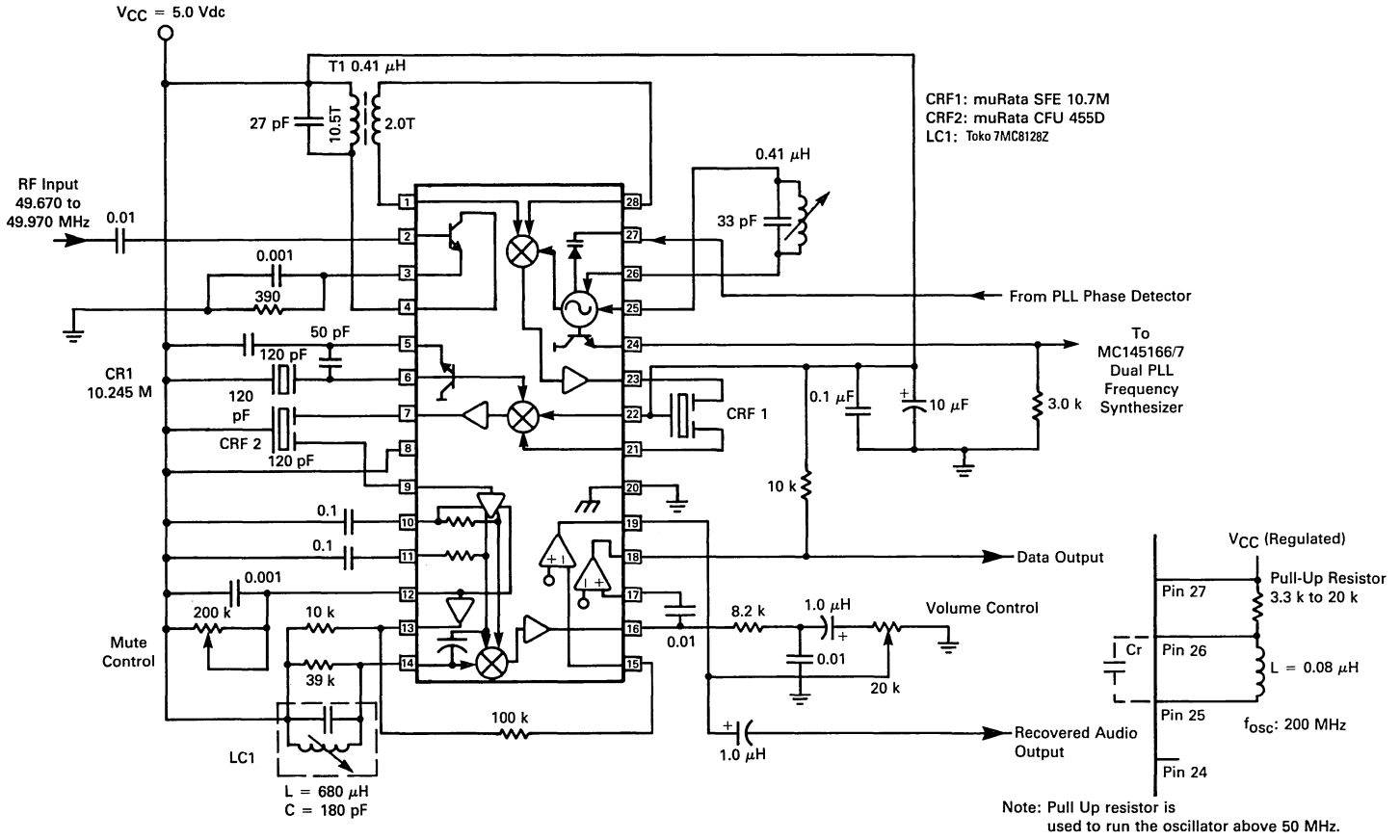
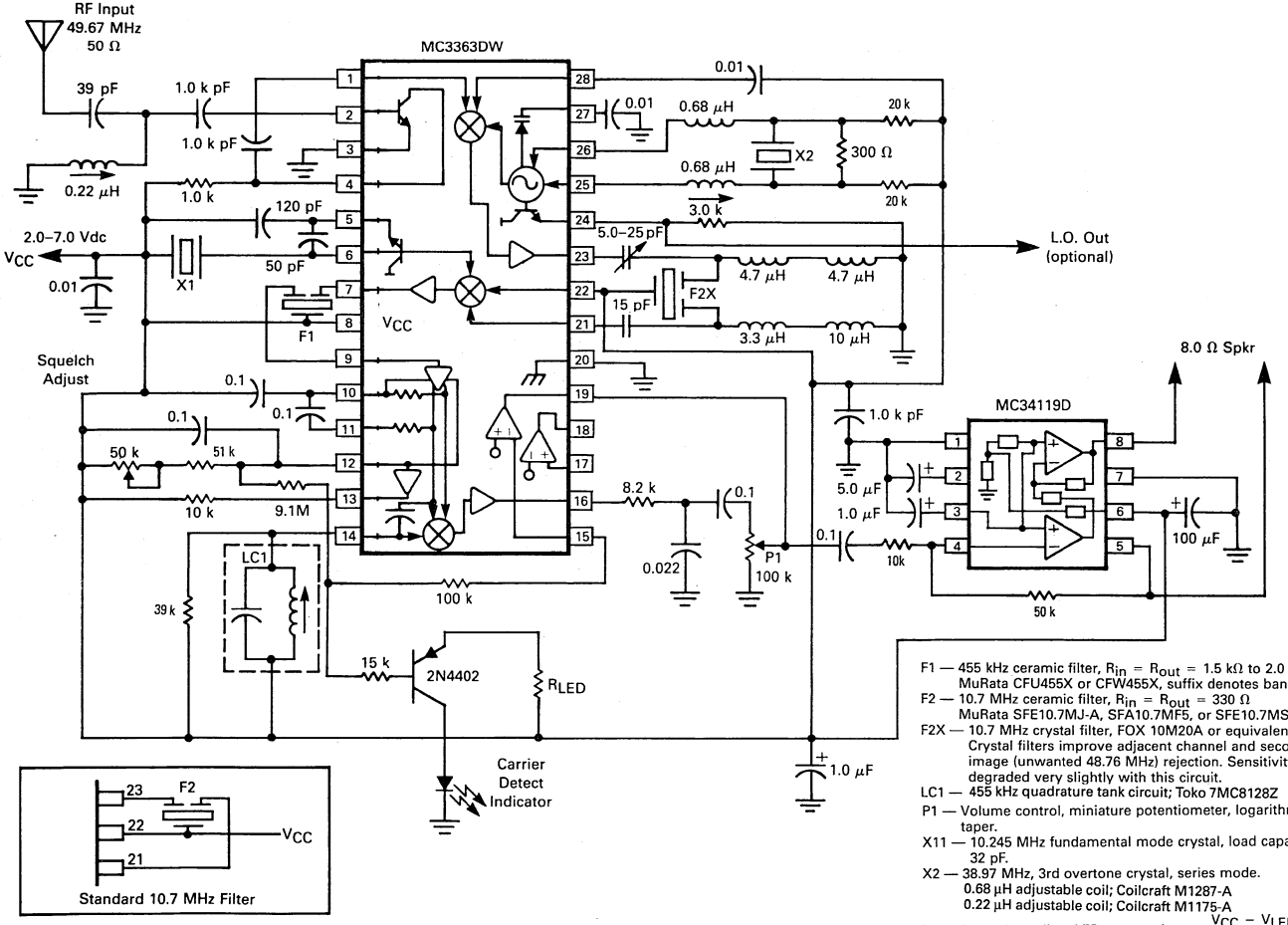


FIGURE 4 — SINGLE CHANNEL NARROWBAND FM RECEIVER AT 49.67 MHz



F1 — 455 kHz ceramic filter, R_{in} = R_{out} = 1.5 kΩ to 2.0 kΩ
MuRata CFU455X or CFW455X, suffix denotes bandwidth
F2 — 10.7 MHz ceramic filter, R_{in} = R_{out} = 330 Ω
MuRata SFE10.7MJ-A, SFA10.7MF5, or SFE10.7MS2A.
F2X — 10.7 MHz crystal filter, FOX 10M20A or equivalent.
Crystal filters improve adjacent channel and second image (unwanted 48.76 MHz) rejection. Sensitivity is degraded very slightly with this circuit.
LC1 — 455 kHz quadrature tank circuit; Toko 7MC8128Z
P1 — Volume control, miniature potentiometer, logarithmic taper.
X11 — 10.245 MHz fundamental mode crystal, load capacity 32 pF.
X2 — 38.97 MHz, 3rd overtone crystal, series mode.
0.68 μH adjustable coil; Coilcraft M1287-A
0.22 μH adjustable coil; Coilcraft M1175-A

R_{LED} is used to adjust LED current: $I_{LED} \approx \frac{V_{CC} - V_{LED}}{R_{LED}}$

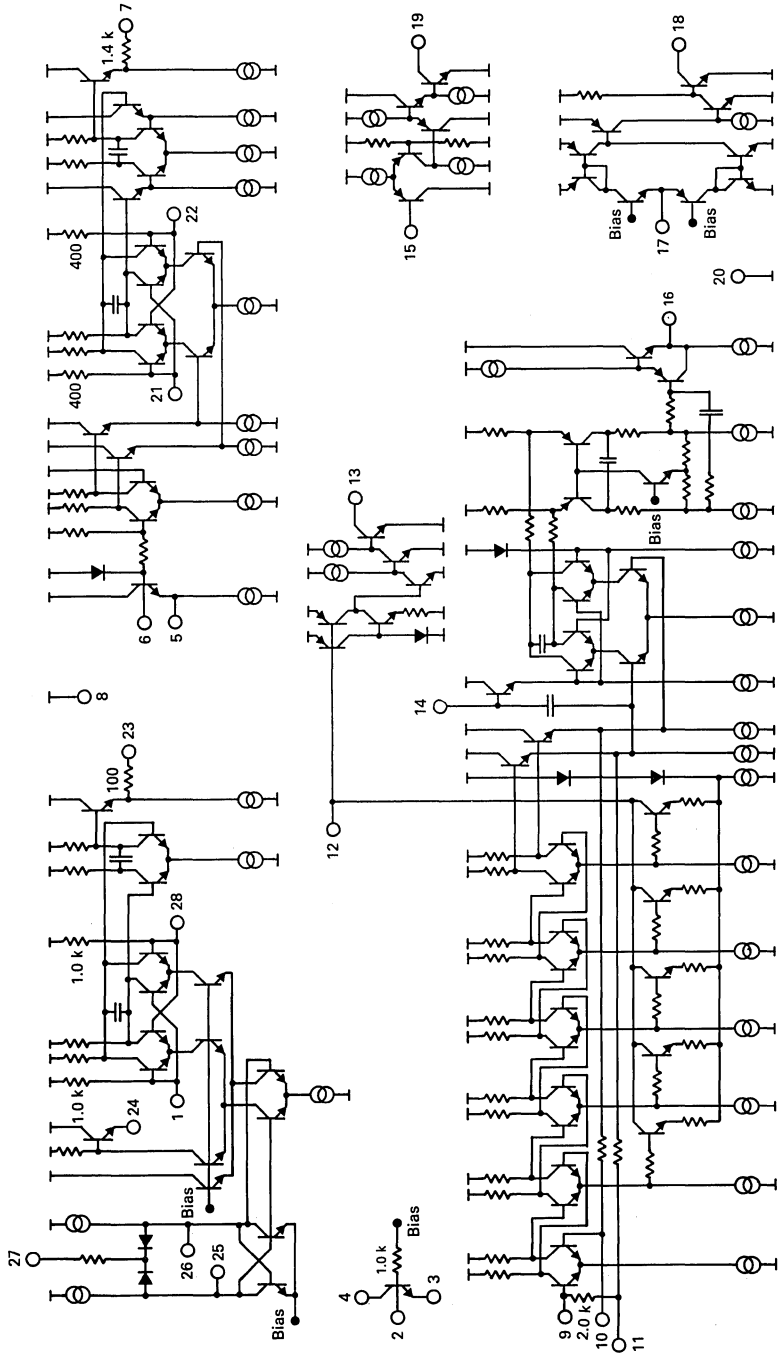


FIGURE 5 — CIRCUIT SCHEMATIC

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FIGURE 6 — PC BOARD COMPONENT VIEW WITH HIGH PERFORMANCE CRYSTAL FILTER

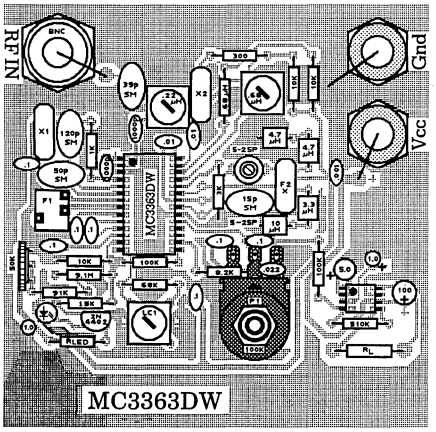


FIGURE 7 — PC BOARD CIRCUIT SIDE VIEW

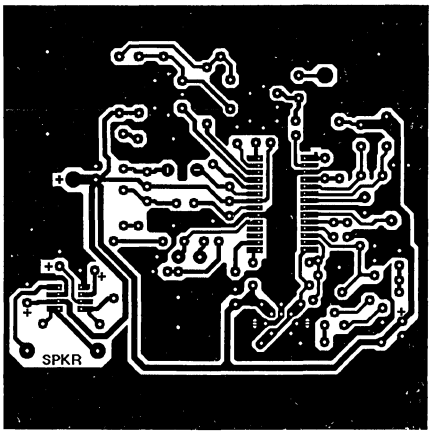
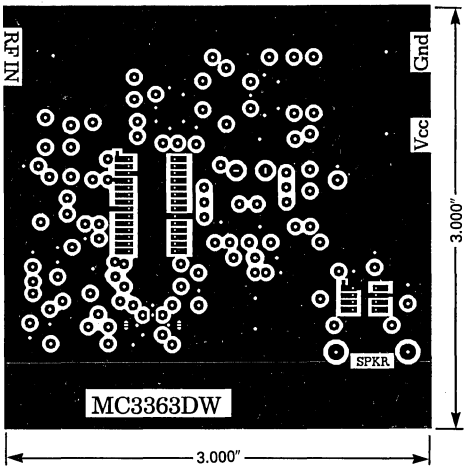


FIGURE 8 — PC BOARD COMPONENT SIDE GROUND PLANE



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC3367

LOW VOLTAGE FM NARROWBAND RECEIVER

. . . with single conversion circuitry including oscillator, mixer, IF amplifiers, limiting IF circuitry, and quadrature discriminator. The MC3367 is perfect for narrowband audio and data applications up to 75 MHz which require extremely low power consumption. Battery powered applications down to V_{CC} = 1.1 V are possible. The MC3367 also includes an on-board voltage regulator, low battery detection circuitry, a receiver enable allowing a power down "sleep mode," two undedicated buffer amplifiers to allow simultaneous audio and data reception, and a comparator for enhancing FSK (Frequency Shift Keyed) data reception to 1200 baud.

- Low Supply Voltage: V_{CC} = 1.1 to 3.0 Vdc
- Low Power Consumption: P_D = 1.5 to 5.0 mW
- Input Bandwidth 75 MHz
- Excellent Sensitivity: Input Limiting Voltage for 12 dB Sinad = 0.5 μVrms from Conjugated Matched Source
- Voltage Regulator Available (Source Capability 3.0 mA)
- Receiver Enable to Allow Active/Standby Operation
- Low Battery Detection Circuitry
- Self Biasing Audio Buffer with Nominal Gain A_V = 4.0
- Data Buffer with Nominal Gain A_V = 3.2
- FSK Data Shaping Comparator Included
- Standard 28-Lead Surface Mount (SOIC) Package

LOW VOLTAGE SINGLE CONVERSION FM RECEIVER

SILICON MONOLITHIC INTEGRATED CIRCUIT

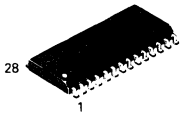


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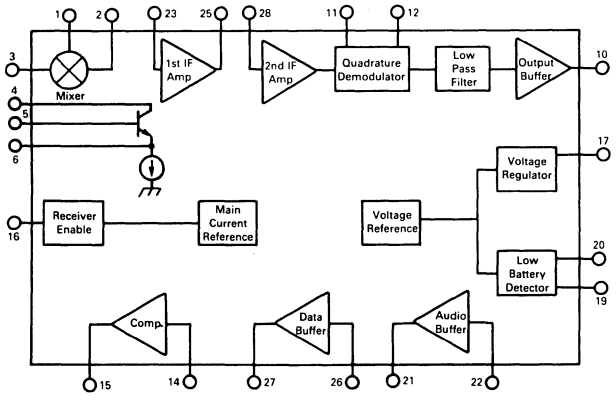
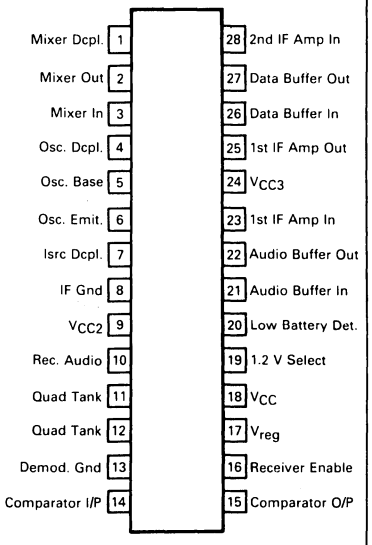
FIGURE 1 — BLOCK DIAGRAM



PIN CONNECTIONS



MAXIMUM RATINGS (Voltages with respect to Pins 8 and 13; T_A = 25°C)

Rating	Pin	Value	Unit
Supply Voltage	18	5.0	Vdc
RF Input Signal	3	1.0	Vrms
Audio Buffer Input	21	1.0	Vrms
Data Buffer Input	26	1.0	Vrms
Comparator Input	14	1.0	Vrms
Junction Temperature	—	150	°C
Storage Temperature	—	−65 to +150	°C

Devices should not be operated at or outside these values. The "Recommended Operating Limits" provide for actual device operation.

RECOMMENDED OPERATING CONDITIONS

Parameter	Pin	Value	Unit
Supply Voltage	18	1.1 to 3.0	Vdc
Receiver Enable Voltage	16	0 or V_{CC}	Vdc
1.2 V Select Voltage	19	Open or V_{CC}	Vdc
RF Input Signal Level	3	0.001 to 100	mVrms
RF Input Frequency	3	0 to 75	MHz
Intermediate Frequency (IF)	—	455	kHz
Audio Buffer Input	21	0 to 75	mVrms
Data Buffer Input	26	0 to 75	mVrms
Comparator Input	14	10 to 300	mVrms
Ambient Temperature	—	0 to 70	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 1.3 V, f_o = 10.7 MHz, f_{mod} = 1.0 kHz, Deviation = 3.0 kHz, T_A = 25°C, Test Circuit of Figure 2 unless otherwise noted)

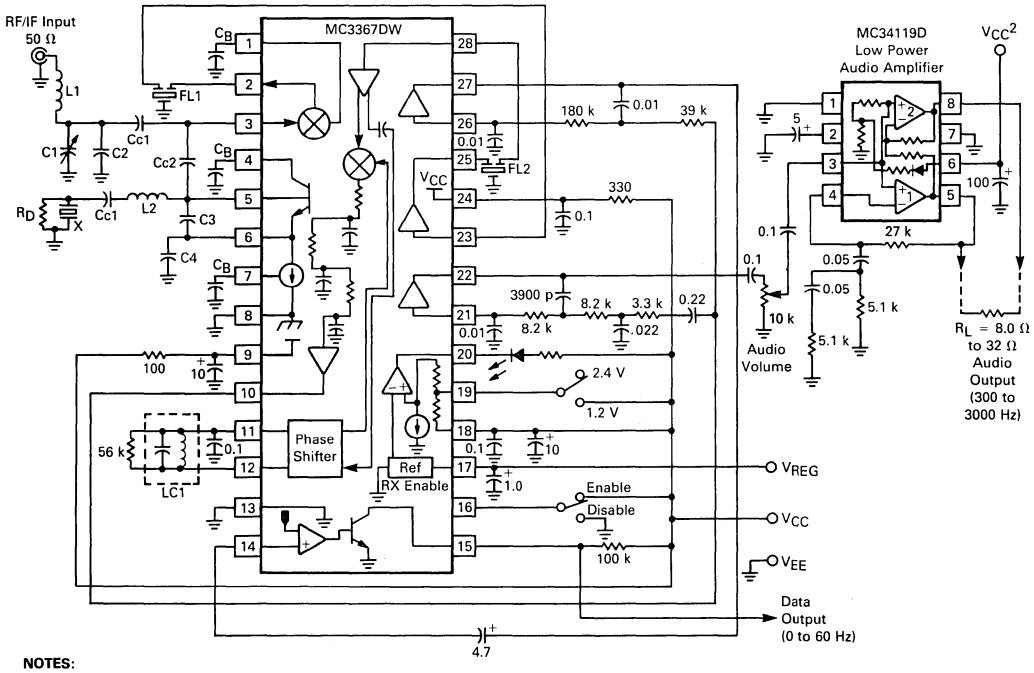
Characteristic	Pin	Min	Typ	Max	Units
OVERALL MC3367 PERFORMANCE					
Drain Current — Pin 15 = V_{CC}	—	—	1.4	3.0	mA
— Pin 15 = 0 Vdc	—	—	0.5	—	μA
Recovered Audio (RF Input = 10 mV)	10	—	13	—	mVrms
Noise Output (RF Input = 0 mV)	10	—	4.5	—	mVrms
Input for −3.0 dB Limiting	3	—	0.2	—	μVrms
MIXER					
Mixer Input Resistance (Rp)	3	—	3.0	—	kΩ
Mixer Input Capacitance (Cp)	3	—	9.0	—	pF
FIRST IF AMPLIFIER					
First IF Amp Voltage Gain	—	—	25	—	dB
AUDIO BUFFER					
Voltage Gain	—	—	4.0	—	V/V
Input Resistance	21	—	125	—	kΩ
Maximum Input for Undistorted Output	21	—	70	—	mVrms
Maximum Output Swing	22	—	800	—	mVpp
Output Resistance	22	—	680	—	Ω
DATA BUFFER					
Voltage Gain	—	—	3.2	—	V/V
Input Resistance	26	—	8.0	—	MΩ
Maximum Input for Undistorted Output (< 3% THD)	26	—	70	—	mVrms
Maximum Output Swing	27	—	600	—	mVpp
Output Resistance	27	—	1.5	—	kΩ

(continued)

ELECTRICAL CHARACTERISTICS — continued (V_{CC} = 1.3 V, f_o = 10.7 MHz, f_{mod} = 1.0 kHz, Deviation = 3.0 kHz, T_A = 25°C, Test Circuit of Figure 2 unless otherwise noted)

Characteristic	Pin	Min	Typ	Max	Units
COMPARATOR					
Minimum Input for Triggering	14	—	7.0	—	mVrms
Maximum Input Frequency (R_L = 100 kΩ)	14	—	25	—	kHZ
Rise Time (10–90%; R_L = 100 kΩ)	15	—	5.0	—	μs
Fall Time (90–10%; R_L = 100 kΩ)	15	—	0.4	—	μs
LOW BATTERY DETECTOR					
Low Battery Trip Point	18	—	1.09	—	Vdc
Low Battery Output — V_{CC} = 0.9 V	20	—	0.2	—	Vdc
— V_{CC} = 1.3 V	20	—	V_{CC}	—	Vdc
VOLTAGE REGULATOR					
Regulated Output (see Figure 6)	17	—	0.95	—	Vdc
Source Capability	17	—	—	3.0	mA

FIGURE 2 — EVALUATION CIRCUIT



NOTES:

1. FL1 and FL2 are 455 kHz ceramic bandpass filters, which should have input and output impedances of 1.5 kΩ to 2.0 kΩ. Suggested part numbers are muRata CFU455X or CFW455X — the "X" suffix denotes bandwidth.
2. LC1 is a 455 kHz resonator. Recommended part number are Toko America 7M8128Z. The evaluation board layout shown provides for use of either resonator. **Ceramic discriminator elements cannot be used with the MC3367 due to their low input impedance.** The damping resistor value can be raised to increase the recovered audio or lowered to increase the quadrature detector's bandwidth and linearity — practical limits are approximately 27 kΩ to 75 kΩ. Typically the quadrature detector's bandwidth should match the low IF filter's bandwidth
3. The data buffer is set up as a low-pass filter with a corner frequency of approximately 200 Hz. The audio buffer is a bandpass filter with corner frequencies of 300 Hz and 3.0 kHz. The audio amplifier provides bass suppression.
4. Cc1 and Cc3 are RF coupling capacitors and should have ≤ 20 Ω impedance at the desired input and oscillator frequencies.
5. Cc2 provides "light coupling" of the oscillator signal into the mixer, and should have a ≈ 3.0 kΩ to 5.0 kΩ impedance at the desired local oscillator frequency.
6. Capacitors labelled C_B are bypass capacitors and should have ≤ 20 Ω impedance at the desired RF and local oscillator frequencies.
7. The network of L1, C1 and C2 provides impedance matching of the mixer input (nominally 3.0 kΩ shunted by 9.0 pF) to 50 Ω at the desired RF/IF input frequency. This will allow for bench testing of the receiver from typical RF signal generators or radio service monitors, but additional or different matching will be required to maximize receiver sensitivity when used in conjunction with an antenna, RF preamplifier or mixer.

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FIGURE 3 — RECOVERED AUDIO versus SUPPLY

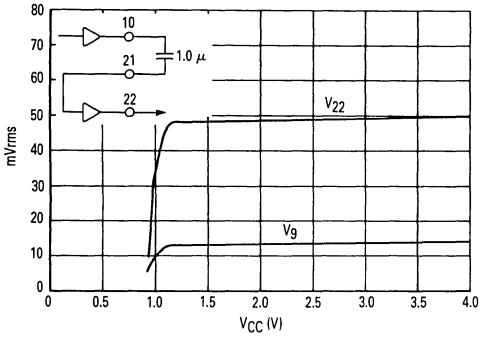

FIGURE 4 — DRAIN versus SUPPLY

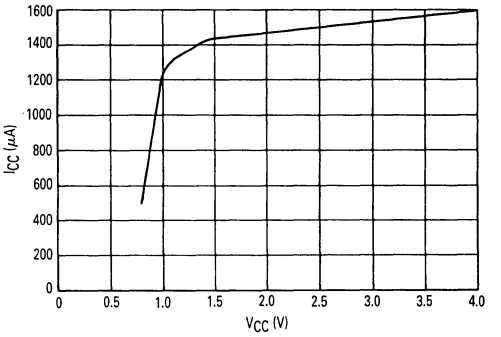

FIGURE 5 — S+N, N versus INPUT

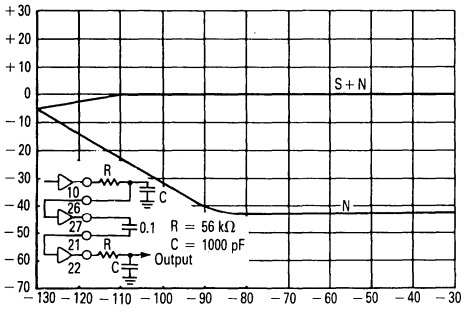

FIGURE 6 — V_{REG} versus SUPPLY

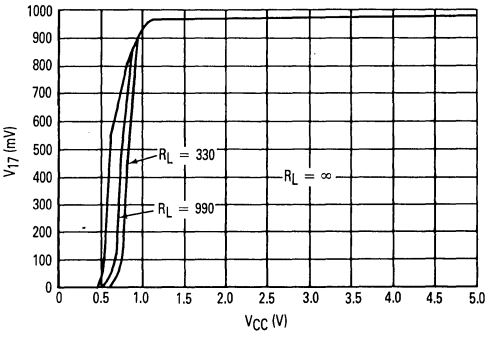

FIGURE 7 — REGULATED OUTPUT AND RECOVERED AUDIO versus TEMPERATURE

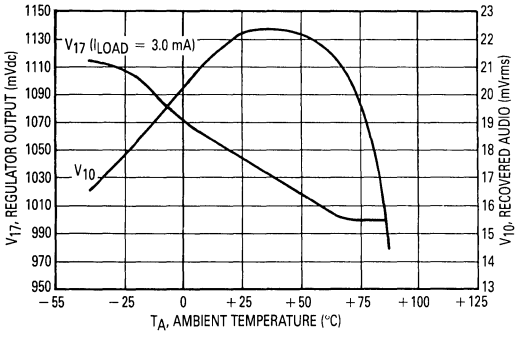

FIGURE 8 — BUFFER AMPLIFIER GAINS versus TEMPERATURE

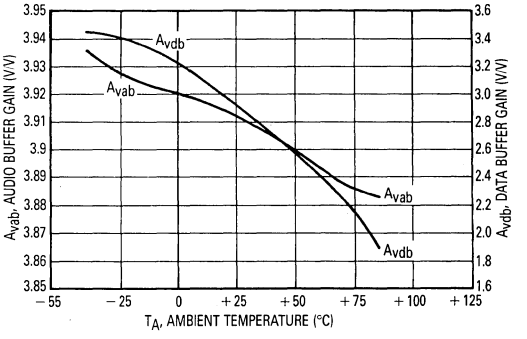

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FIGURE 9 — CURRENT DRAIN versus TEMPERATURE

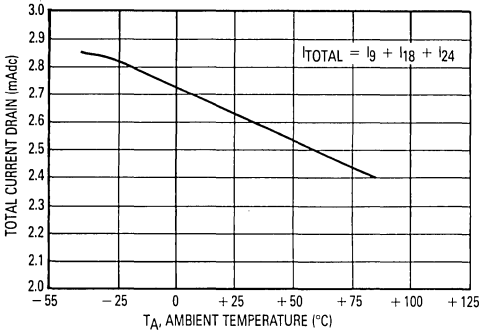
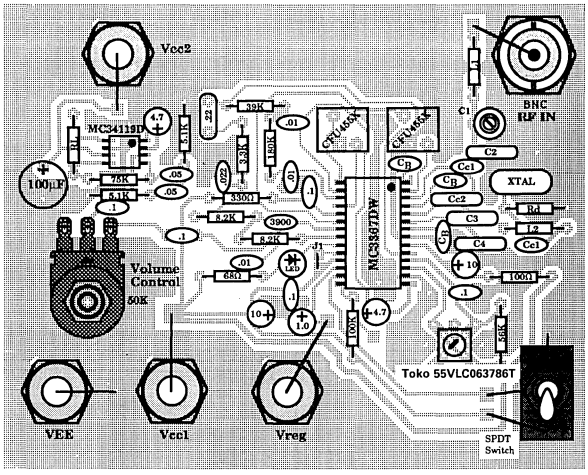
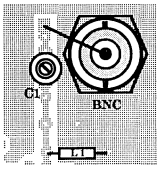


FIGURE 10 — MC3367DW DEMONSTRATION RECEIVER





Alternate input circuit for 72 MHz receiver.

In. Freq.	L1	L2	C1	C2	C3	C4	Cc1	Cc2	C_B	R_D
10.7 MHz	6.8 μH	Short	2–82 pF	10 pF	120 pF	50 pF	1.0 k pF	5.0 pF	0.1 μF	Open
45 MHz	0.68 μH	1.2 μH	5–25 pF	Open	30 pF	5.0 pF	1.0 k pF	1.0 pF	1.0 k pF	1.0 k
72 MHz	0.22 μH	0.22 μH	5–25 pF	Open	18 pF	3.0 pF	470 pF	1.0 pF	470 pF	1.0 k

Volume Control: CRL B12503SL
V_{CC1}: 1.1 V to 3.0 V
V_{CC2}: 2.0 V to 16 V
Speaker: 8.0 Ω to 32 Ω
J1: Jumper — install for 1.2 V operation. Leave open for 2.4 V operation.
ICs mount on circuit side (back) of PC board.
C3, C4 must be 5% silver mica

FIGURE 11 — BOTTOM (CIRCUIT) SIDE

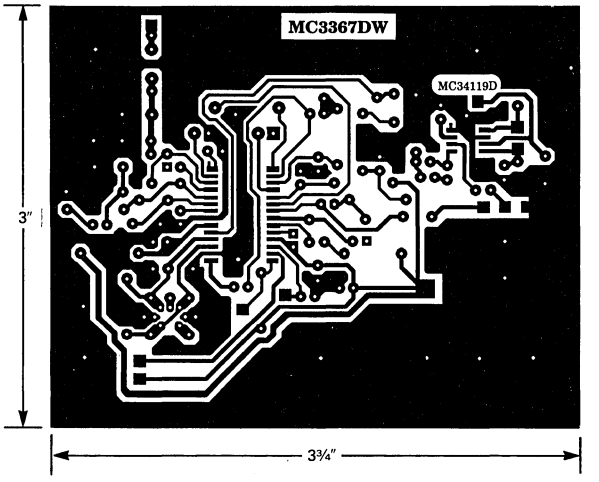
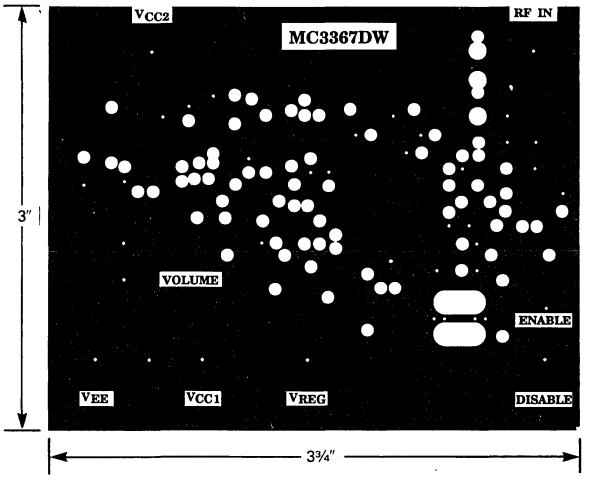


FIGURE 12 — TOP (COMPONENT/GROUND PLANE) SIDE



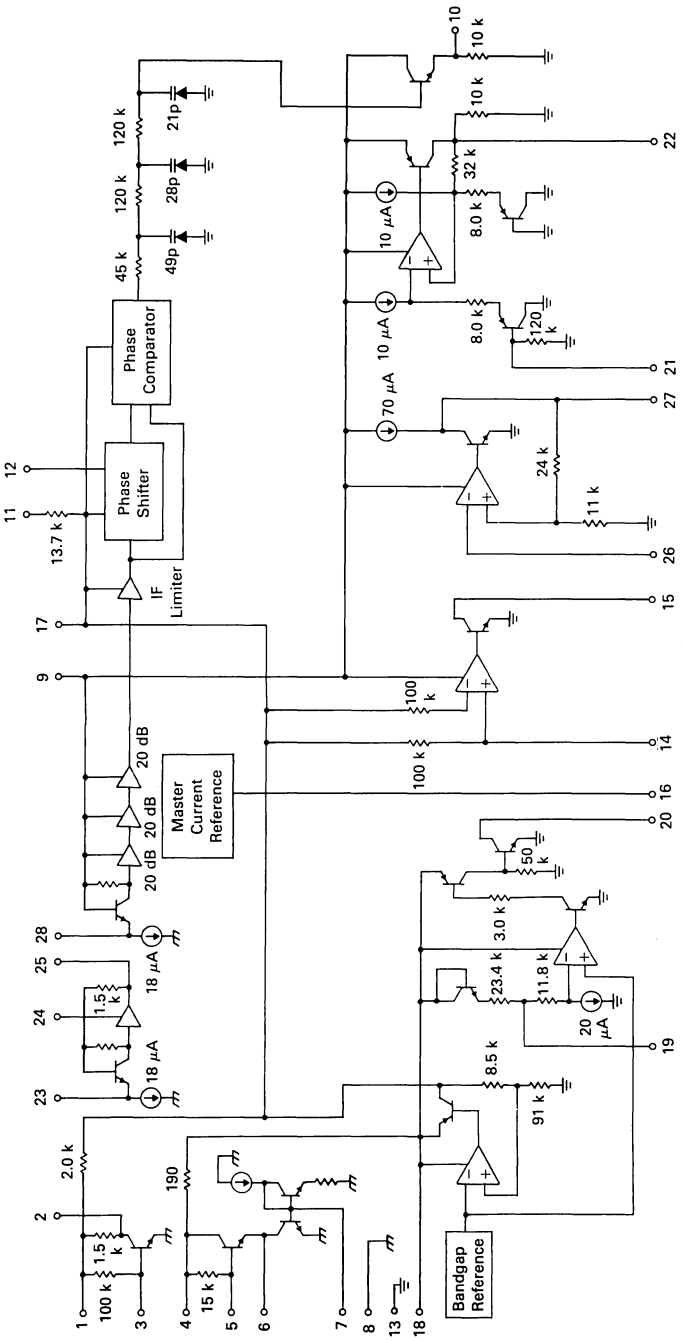


FIGURE 13 — CIRCUIT SCHEMATIC

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CIRCUIT DESCRIPTION

The MC3367 is an FM narrowband receiver capable of operation to 75 MHz. The low voltage design yields low power drain and excellent sensitivity in narrowband voice and data link applications. In the typical application the mixer amplifies the incoming RF or IF signal and converts this frequency to 455 kHz. The signal is then filtered by a 455 kHz ceramic filter and applied to the first intermediate frequency (IF) amplifier input, before passing through a second ceramic filter. The modulated IF signal is then applied to the limiting IF amplifier and detector circuitry. Modulation is recovered by a conventional quadrature detector. The typical modulation bandwidth available is 3.0 to 5.0 kHz.

Features available include buffers for audio/data amplification and active filtering, on board voltage regulator, low battery detection circuitry with programmable level, and receiver disable circuitry. The MC3367 is an FM utility receiver to be used for voice and/or narrowband data reception. It is especially suitable where extremely low power consumption and high design flexibility are required.

APPLICATION

The MC3367 can be used as a high performance FM IF for use in low power dual conversion receivers. Because of the MC3367's extremely good sensitivity (0.6 μV for 20 dB (S+N)/N, see Figure 5), it can also be used as a stand alone single conversion narrowband receiver to 75 MHz for applications not sensitive to image frequency interference. An RF preamplifier will likely be needed to overcome preselector losses.

The oscillator is a Colpitts type which must be run under crystal control. For fundamental mode crystals choose resonators, parallel resonant, for a 32 pF load. For higher frequencies, use a 3rd overtone series mode type. The coil (L2) and R_D resistor are needed to ensure proper operation.

The best adjacent channel and sensitivity response occur when two 455 kHz ceramic filters are used, as shown in Figure 2. Either can be replaced by a 0.1 μF coupling capacitor to reduce cost, but some degradation in sensitivity and/or stability is suspected.

The detector is a quadrature type, with the connection from the limiter output to the detector input provided internally as with the MC3359 and the MC3361. A 455 kHz LC tank circuit must be provided externally. One of the tank pins (Pin 11) must be decoupled using a 0.1 μF capacitor. The 56 kΩ damping resistor (see Figure 2), determines the peak separation of the detector (and thus its bandwidth). Smaller values will increase the separation and bandwidth but decrease recovered audio and sensitivity.

The data buffer is a noninverting amplifier with a nominal voltage gain of 3.2 V/V. This buffer needs its dc bias (approx. 250 mV) provided externally or else debiasing will occur. A single-pole RC filter, as shown in Figure 5, connecting the recovered audio output to the data buffer input provides the necessary dc bias and some post detection filtering. The buffer can also be used as an active filter.

The audio buffer is a noninverting amplifier with a nominal voltage gain of 4.0 V/V. This buffer is self-biasing so its input should be ac coupled. The two buffers, when applied as active filters, can be used together to allow simultaneous audio and very low speed data reception. Another possible configuration is to receive audio only and include a noise-triggered squelch.

The comparator is a noninverting type with an open collector output. Typically, the pull-up resistor used between Pin 15 and V_{CC} is 100 kΩ. With R_L = 100 kΩ the comparator is capable of operation up to 25 kHz. This circuit is self-biasing, so its input should be ac coupled.

The regulator is a 0.95 V reference capable of sourcing 3.0 mA. This pin (Pin 17) needs to be decoupled using a 1.0–10 μF capacitor to maintain stability of the MC3367.

All three V_{CC}s on the MC3367 (V_{CC}, V_{CC2}, V_{CC3}) run on the same supply voltage. V_{CC} is typically decoupled using capacitors only. V_{CC2} and V_{CC3} should be bypassed using the RC bypasses shown in Figure 2. Eliminating the resistors on the V_{CC2} and V_{CC3} bypasses may be possible in some applications, but a reduction in sensitivity and quieting will likely occur.

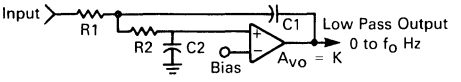
The low battery detection circuit gives an NPN open collector output at Pin 20 which drops low when the MC3367 supply voltage drops below 1.1 V. Typically it would be pulled up via a 100 kΩ resistor to supply.

The 1.2 V Select pin, when connected to the MC3367 supply, programs the low battery detector to trip at V_{CC} < 1.1 V. Leaving this pin open raises the trip voltage on the low battery detector.

Pin 16 is a receiver enable which is connected to V_{CC} for normal operation. Connecting this pin to ground shuts off receiver and reduces current drain to I_{CC} < 0.5 μA.

APPENDIX

Design of 2nd Order Sallen-Key Low Pass Filters



The audio and data buffers can easily be configured as active low pass filters using the circuit configuration shown above. The circuit has a center frequency (f_o) and quality factor (Q) given by the following:

$$f_o = \frac{1}{2\pi\sqrt{R1R2C1C2}}$$

$$Q = \frac{1}{\sqrt{\frac{R2C2}{R1C1}} + \sqrt{\frac{R1C2}{R2C1}} + (1-K)\sqrt{\frac{R1C1}{R2C2}}}$$

If possible, let R1 = R2 or C1 = C2 to simplify the above equations. Be sure to avoid a negative Q value to prevent instability. Setting Q = $1/\sqrt{2}$ = 0.707 yields a maximally flat filter response.

Data Buffer Design

The data buffer is designed as follows:

f_o = 200 Hz

C1 = C2 = 0.01 μF

Q = 0.707 (target)

K = 3.2 (data buffer open loop voltage gain)

Setting C1 = C2 yields:

$$f_o = \frac{1}{2\pi C1\sqrt{R1R2}}$$

$$Q = \frac{1}{\sqrt{\frac{R2}{R1}} + (2-K)\sqrt{\frac{R1}{R2}}}$$

Iteration yields R2 = 4.2 (R1) to make Q = 0.707.

Substitution into the equation for f_o yields:

R1 = 38 kΩ (use 39 kΩ)

R2 = 4.2 (R1) = 180 kΩ

C1 = C2 = 0.01 μF

Audio Buffer Design

The audio buffer is designed as follows:

f_o = 3000 Hz

R1 = R2 = 8.2 kΩ

Q = 0.707 (target)

K = 4.0 (audio buffer open loop voltage gain)

Setting R1 = R2 yields:

$$f_o = \frac{1}{2\pi R1\sqrt{C1C2}}$$

$$Q = \frac{1}{2\sqrt{\frac{C2}{C1}} + (1-K)\sqrt{\frac{C1}{C2}}}$$

Iteration yields C2 = 2.65 (C1) to make Q = 0.707.

Substitution into the equation for f_o yields:

C1 = 3900 pF

C2 = 2.65 (C1) = 0.01 μF

R1 = R2 = 8.2 kΩ

8

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC3371
MC3372

Advance Information

Low Power Narrowband FM IF

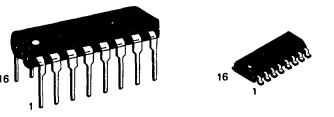
LOW POWER FM IF

SILICON MONOLITHIC INTEGRATED CIRCUIT

The MC3371 and MC3372 perform single conversion FM reception and consist of an oscillator, mixer, limiting IF amplifier, quadrature discriminator, active filter, squelch switch, and meter drive circuitry. These devices are designed for use in FM dual conversion communication equipment. The MC3371/MC3372 are similar to the MC3361/MC3357 FM IFs, except that a signal strength indicator replaces the scan function controlling driver which is in the MC3361/MC3357. The MC3371 is designed for the use of parallel LC components, while the MC3372 is designed for use with either a 455 kHz ceramic discriminator, or parallel LC components.

These devices also require fewer external parts than earlier products. The MC3371 and MC3372 are available in dual-in-line and surface mount packaging.

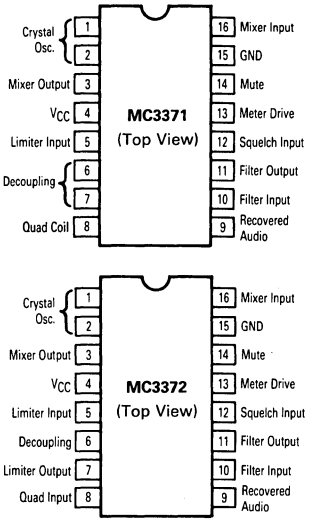
- Wide Operating Supply Voltage Range: V_{CC} = 2.0 to 9.0 V
- Input Limiting Voltage Sensitivity of −3.0 dB
- Low Drain Current: I_{CC} = 3.2 mA, @ V_{CC} = 4.0 V, Squelch Off
- Minimal Drain Current Increase When Squelched
- Signal Strength Indicator: 60 dB Dynamic Range
- Mixer Operating Frequency Up to 100 MHz
- Fewer External Parts Required than Earlier Devices



P SUFFIX
PLASTIC PACKAGE
CASE 648

D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO-16)

PIN CONNECTIONS



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MAXIMUM RATINGS

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage	4	V_{CC}(max)	10	Vdc
RF Input Voltage (V_{CC} ≥ 4.0 Vdc)	16	V_{16}	1.0	Vrms
Detector Input Voltage	8	V_8	1.0	V_{p-p}
Squelch Input Voltage (V_{CC} ≥ 4.0 Vdc)	12	V_{12}	6.0	Vdc
Mute Function	14	V_{14}	−0.7 to 10	V_{pk}
Mute Sink Current	14	I_{14}	50	mA
Junction Temperature	—	T_J	150	°C
Storage Temperature Range	—	T_{stg}	−65 to +150	°C

Devices should not be operated at these values. The "Recommended Operating Conditions" table provides conditions for actual device operation.

RECOMMENDED OPERATING CONDITIONS

Rating	Pin	Symbol	Value	Unit
Supply Voltage (@ T_A = 25°C) ($-30°C \le T_A \le +75°C$)	4	V_{CC}	2.0 to 9.0 2.4 to 9.0	Vdc
RF Input Voltage	16	V_{rf}	0.0005 to 10	mVrms
RF Input Frequency	16	f_{rf}	0.1 to 100	MHz
Oscillator Input Voltage	1	V_{local}	80 to 400	mVrms
Intermediate Frequency	—	f_{if}	455	kHz
Limiter Amp Input Voltage	5	V_{if}	0 to 400	mVrms
Filter Amp Input Voltage	10	V_{fa}	0.1 to 300	mVrms
Squelch Input Voltage	12	V_{sq}	0 or 2	Vdc
Mute Sink Current	14	I_{sq}	0.1 to 30	mA
Ambient Temperature Range	—	T_A	−30 to +70	°C

ORDERING INFORMATION

Device	Temperature Range	Package
MC3371D	−30° to +70°C	SO-16
MC3371P		Plastic DIP
MC3372D		SO-16
MC3372P		Plastic DIP

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 4.0 Vdc, f_o = 58.1125 MHz, df = ±3.0 kHz, f_{mod} = 1.0 kHz, 50 Ω source, f_{local} = 57.6575 MHz, V_{local} = 0 dBm, T_A = 25°C unless otherwise noted)

Characteristic	Pin	Symbol	Min	Typ	Max	Unit
Input for 12 dB SINAD	—	V_{SIN}				μVrms
Matched Input — (See Figures 10, 11 & 12)			—	1.0	—	
Unmatched Input — (See Figures 7A & 7B)			—	5.0	15	
Input for 20 dB NQS	—	V_{NQS}	—	3.5	—	μVrms
Recovered Audio Output Voltage	—	AF_O				mVrms
V_{rf} = −30 dBm			120	200	320	
Recovered Audio Drop Voltage Loss	—	AF_{loss}				dB
V_{rf} = −30 dBm, V_{CC} = 4.0 V to 2.0 V			−8.0	−1.5	—	
Meter Drive Output Voltage (No Modulation)	13	M_{Drv}				Vdc
V_{rf} = −100 dBm		MV1	—	0.3	0.5	
V_{rf} = −70 dBm		MV2	1.1	1.5	1.9	
V_{rf} = −40 dBm		MV3	2.0	2.5	3.1	
Filter Amp Gain	—	$A_{V(Amp)}$				dB
R_S = 600 Ω, f_S = 10 kHz, V_{fa} = 1.0 mVrms			47	50	—	
Mixer Conversion Gain	—	$A_{V(Mix)}$				dB
V_{rf} = −40 dBm, R_L = 1.8 kΩ			14	20	—	
Signal to Noise Ratio	—	s/n				dB
V_{rf} = −30 dBm			36	67	—	
Total Harmonic Distortion	—	THD				%
V_{rf} = −30 dBm, BW = 400 Hz to 30 kHz			—	0.6	3.4	
Detector Output Impedance	9	Z_O	—	450	—	Ω
Detector Output Voltage (No Modulation)	9	DV_O				Vdc
V_{rf} = −30 dBm			—	1.45	—	
Meter Drive	13	M_O				μA/dB
V_{rf} = −100 to −40 dBm			—	0.8	—	
Meter Drive Dynamic Range	13	MVD				dB
RF_{In}			—	60	—	
IF_{In} (455 kHz)			—	80	—	
Mixer Third Order Input Intercept Point	—	ITO_{Mix}				dBm
f1 = 58.125 MHz						
f2 = 58.1375 MHz			—	−22	—	
Mixer Input Resistance	16	R_{in}	—	3.3	—	kΩ
Mixer Input Capacitance	16	C_{in}	—	2.2	—	pF

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 4.0 Vdc, T_A = 25°C, unless otherwise noted)

Characteristic	Pin	Symbol	Min	Typ	Max	Unit
Drain Current (No Input Signal)	4					mA
Squelch Off, V_{sq} = 2.0 Vdc		Icc1	—	3.2	4.2	
Squelch On, V_{sq} = 0 Vdc		Icc2	—	3.6	4.8	
Squelch Off, V_{CC} = 2.0 to 9.0 V		dIcc1	—	1.0	2.0	
Detector Output (No Input Signal)	9	V_9				Vdc
DC Voltage, V8 = V_{CC}			0.9	1.6	2.3	
Filter Output (No Input Signal)	11					Vdc
DC Voltage		V_{11}	1.5	2.5	3.5	
Voltage Change, V_{CC} = 2.0 to 9.0 V		dV_{11}	2.0	5.0	8.0	
Trigger Hysteresis	—	Hys	34	57	80	mV

8

TYPICAL CURVES (UNMATCHED INPUT)

FIGURE 1 — TOTAL HARMONIC DISTORTION versus TEMPERATURE

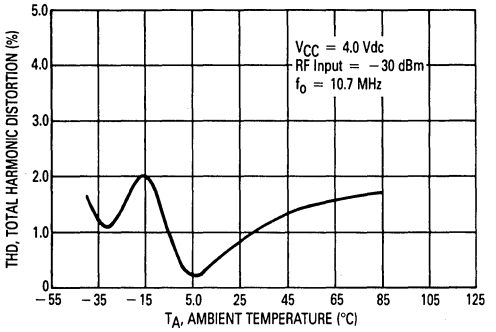

FIGURE 2 — RSSI versus RF INPUT

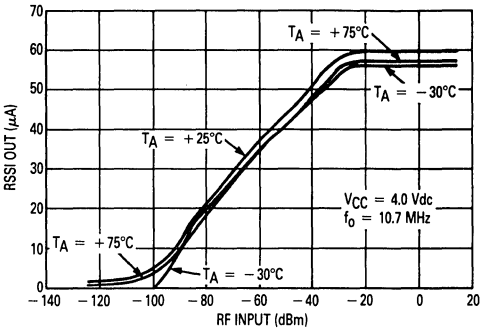

FIGURE 3 — RSSI OUTPUT versus TEMPERATURE

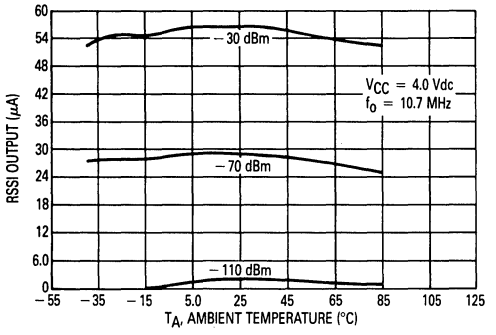

FIGURE 4 — MIXER OUTPUT versus RF INPUT

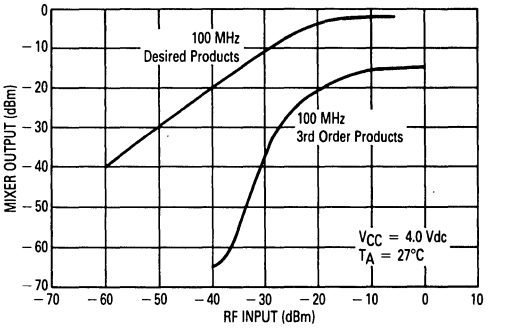

FIGURE 5 — MIXER GAIN versus SUPPLY VOLTAGE

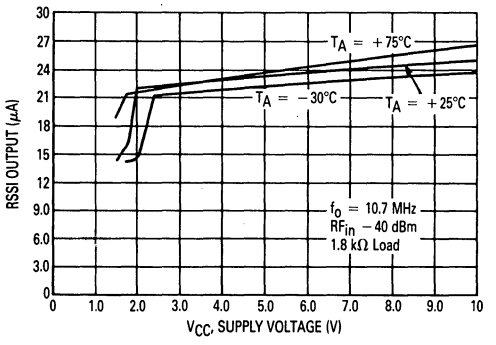

FIGURE 6 — MIXER GAIN versus FREQUENCY

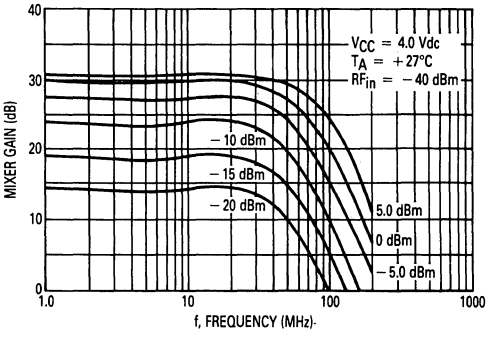

FIGURE 7A — MC3371 FUNCTIONAL BLOCK DIAGRAM AND TEST FIXTURE SCHEMATIC

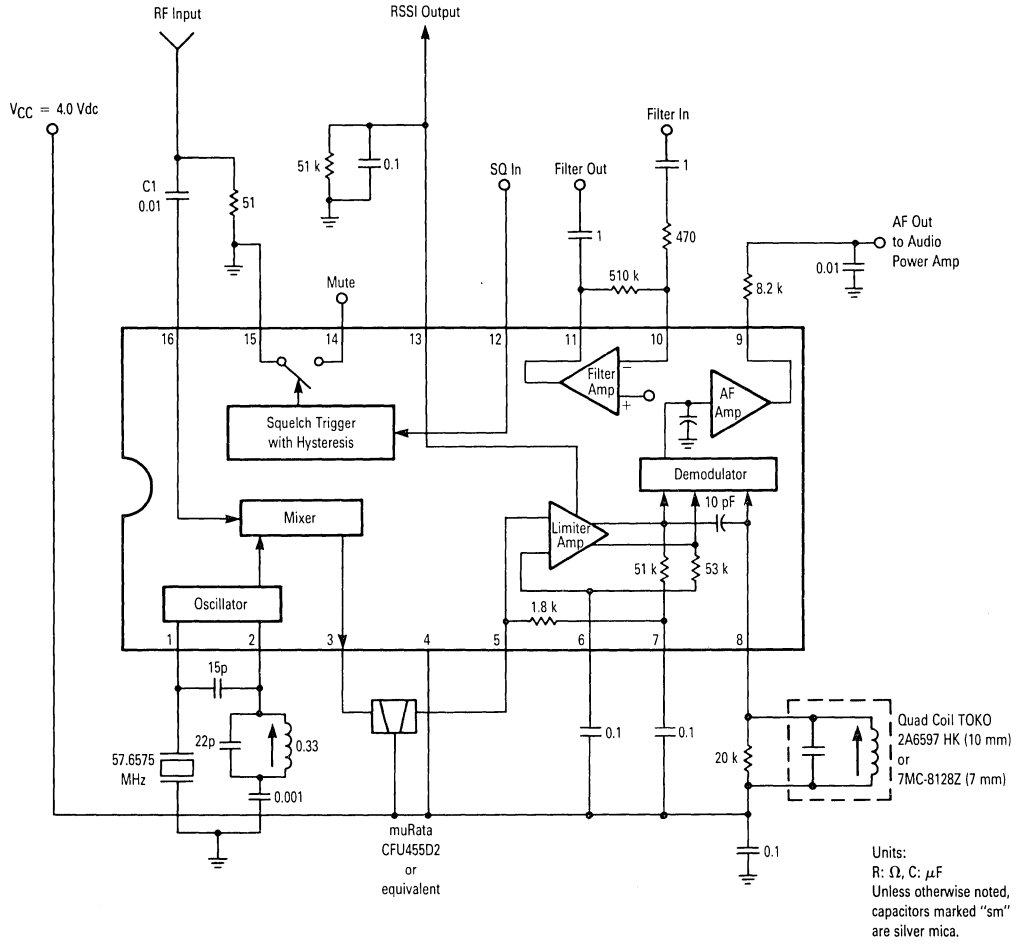

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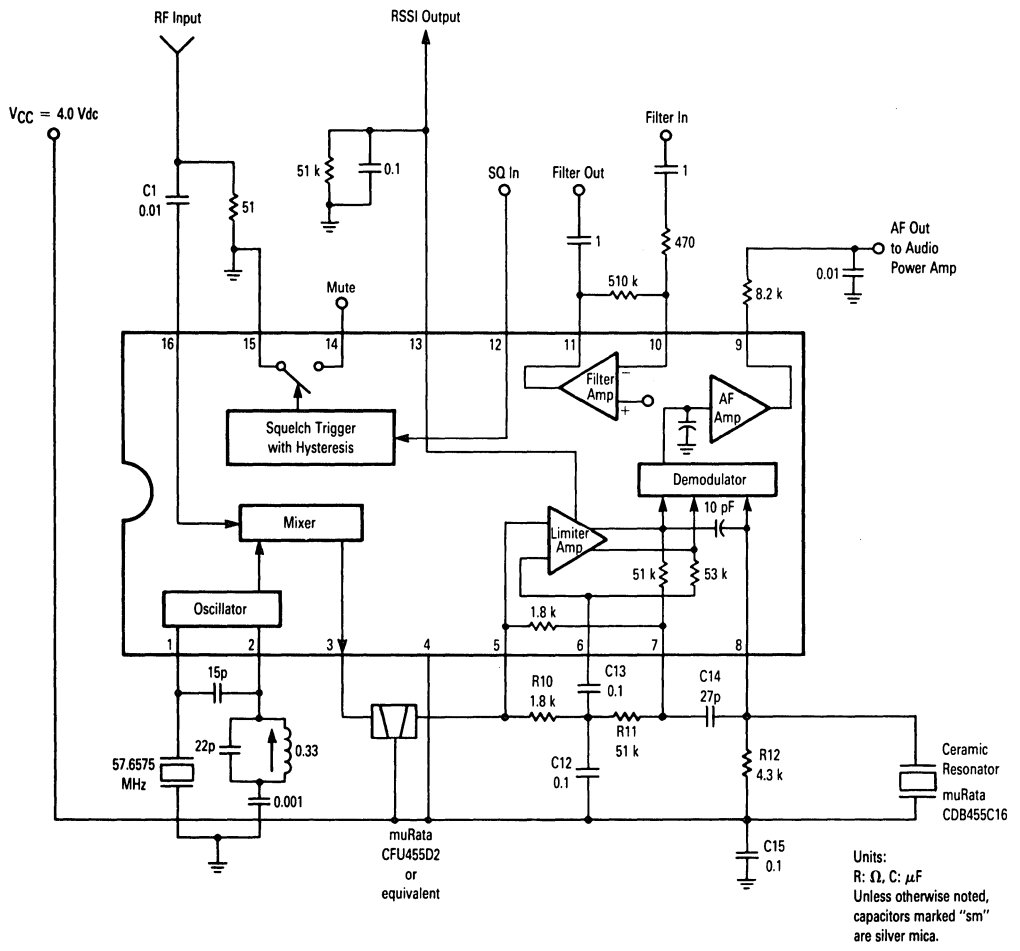
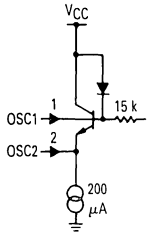
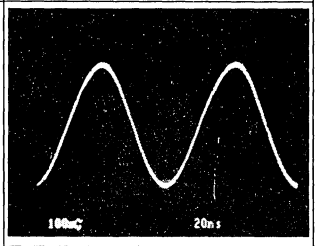
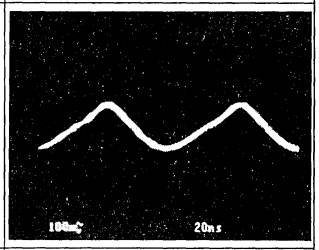
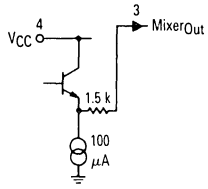
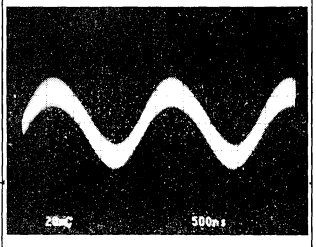
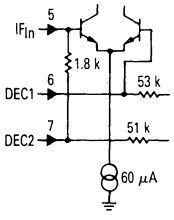
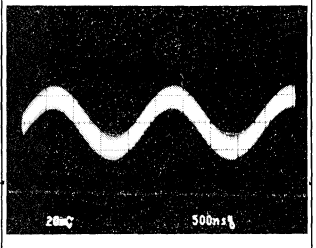
FIGURE 7B — MC3372 FUNCTIONAL BLOCK DIAGRAM AND TEST FIXTURE SCHEMATIC



8

PIN DESCRIPTION

OPERATING CONDITIONS V_{CC} = 4.0 Vdc, RF_{In} = 100 μV, f_{mod} = 1.0 kHz, f_{dev} = 3.0 kHz. MC3371 at f_{RF} = 10.7 MHz (see Figure 10).

Pin	Symbol	Internal Equivalent Circuit	Description	Waveform
1	OSC1		The base of the Colpitts oscillator. Use a high impedance and low capacitance probe or a "sniffer" to view the waveform without altering the frequency. Typical level is 450 mVp-p.	
2	OSC2		The emitter of the Colpitts oscillator. Typical signal level is 200 mVp-p. Note that the signal is somewhat distorted compared to that on pin 1.	
3	MX_{Out}		Output of the Mixer. Riding on the 455 kHz is the RF carrier component. The typical level is approximately 60 mVp-p.	
4	V_{CC}		Supply Voltage — 2.0 to 9.0 Vdc is the operating range. V_{CC} is decoupled to ground.	
5	IF_{In}		Input to the IF amplifier after passing through the 455 kHz ceramic filter. The signal is attenuated by the filter. The typical level is approximately 50 mVp-p.	
6 7	DEC1 DEC2		IF Decoupling. External 0.1 μF capacitors connected to V_{CC}.	

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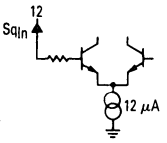
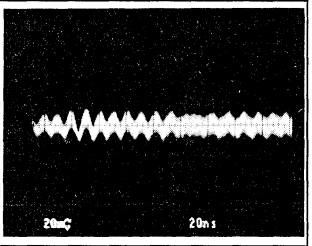
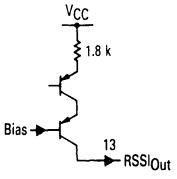
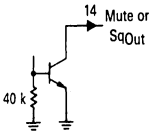
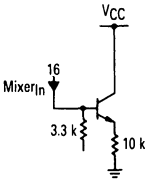
PIN DESCRIPTION

OPERATING CONDITIONS V_{CC} = 4.0 Vdc, RF_{In} = 100 μV, f_{mod} = 1.0 kHz, f_{dev} = 3.0 kHz. MC3371 at f_{RF} = 10.7 MHz (see Figure 10).

Pin	Symbol	Internal Equivalent Circuit	Description	Waveform
12	Sq_{In}		Squelch Input. See discussion in application text.	
13	RSSI		RSSI Output. Referred to as the Received Signal Strength Indicator or RSSI. The chip sources up to 60 μA over the linear 60 dB range. This pin may be used many ways, such as: AGC, meter drive and carrier triggered squelch circuit.	
14	MUTE		Mute Output. See discussion in application text.	
15	GND		Ground. The ground area should be continuous and unbroken. In a two-sided layout, the component side has the ground plane. In a one-sided layout, the ground plane fills around the traces on the circuit side of the board and is not interrupted.	
16	MIX_{In}		Mixer Input — Series Input Impedance: @ 10 MHz: 309 − j33 Ω @ 45 MHz: 200 − j13 Ω	

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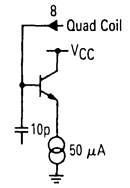
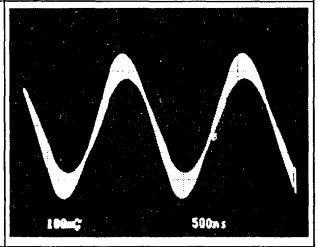
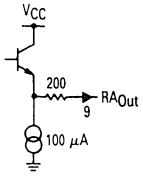
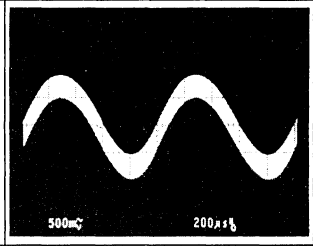
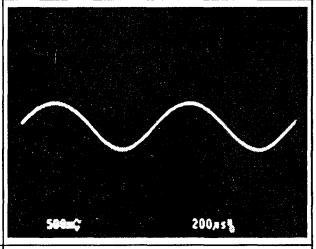
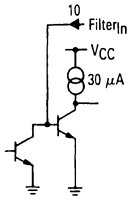
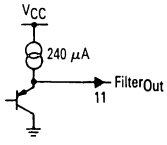
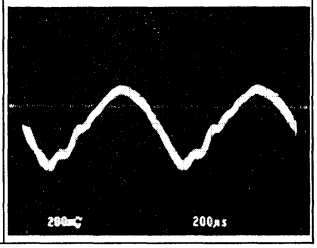
PIN DESCRIPTION

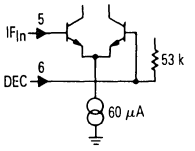
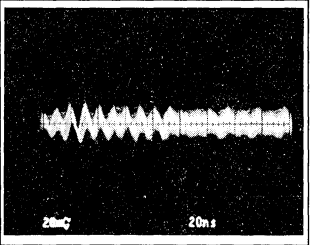
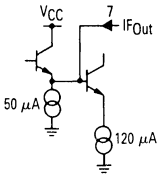
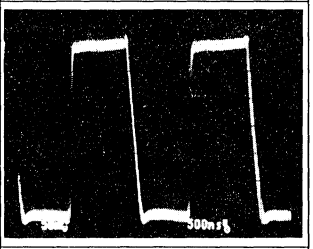
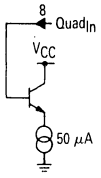
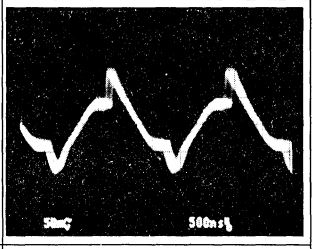
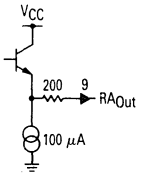
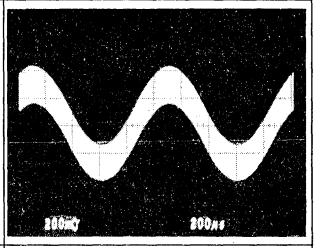
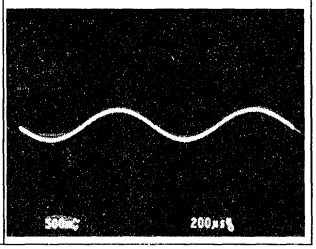
OPERATING CONDITIONS V_{CC} = 4.0 Vdc, RF_{In} = 100 μV, f_{mod} = 1.0 kHz, f_{dev} = 3.0 kHz. MC3371 at f_{RF} = 10.7 MHz (see Figure 10).

Pin	Symbol	Internal Equivalent Circuit	Description	Waveform
8	Quad Coil		Quadrature Tuning Coil. Composite (not yet demodulated) 455 kHz IF signal is present. The typical level is 500 mVp-p.	
9	RA		Recovered Audio. This is a composite FM demodulated output having signal and carrier component. The typical level is 1.4 Vp-p.	
			The filtered recovered audio has the carrier component removed and is typically 800 mVp-p.	
10	Fil_{In}		Filter Amplifier Input	
11	Fil_{Out}		Filter Amplifier Output. The typical signal level is 400 mVp-p.	

8

PIN DESCRIPTION

OPERATING CONDITIONS V_{CC} = 4.0 Vdc, RF_{In} = 100 μV, f_{mod} = 1.0 kHz, f_{dev} = 3.0 kHz. MC3372 at f_{RF} = 45 MHz (see Figure 12).

Pin	Symbol	Internal Equivalent Circuit	Description	Waveform
5	IF_{In}		IF Amplifier Input	
6	DEC1		IF Decoupling. External 0.1 μF capacitors connected to V_{CC}.	
7	IF_{Out}		IF Amplifier Output Signal level is typically 300 mVp-p.	
8	$Quad_{In}$		Quadrature Detector Input. Signal level is typically 150 mVp-p.	
9	RA		Recovered Audio. This is a composite FM demodulated output having signal and carrier components. Typical level is 800 mVp-p.	
			The filtered recovered audio has the carrier signal removed and is typically 500 mVp-p.	

*Other pins are the same as pins in MC3371.

FIGURE 8 — MC3371 CIRCUIT SCHEMATIC

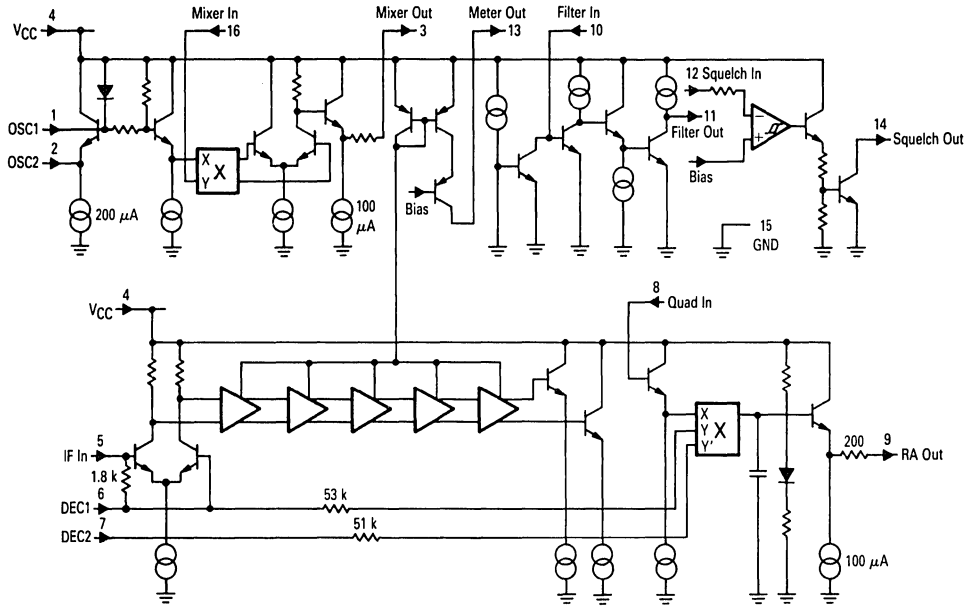
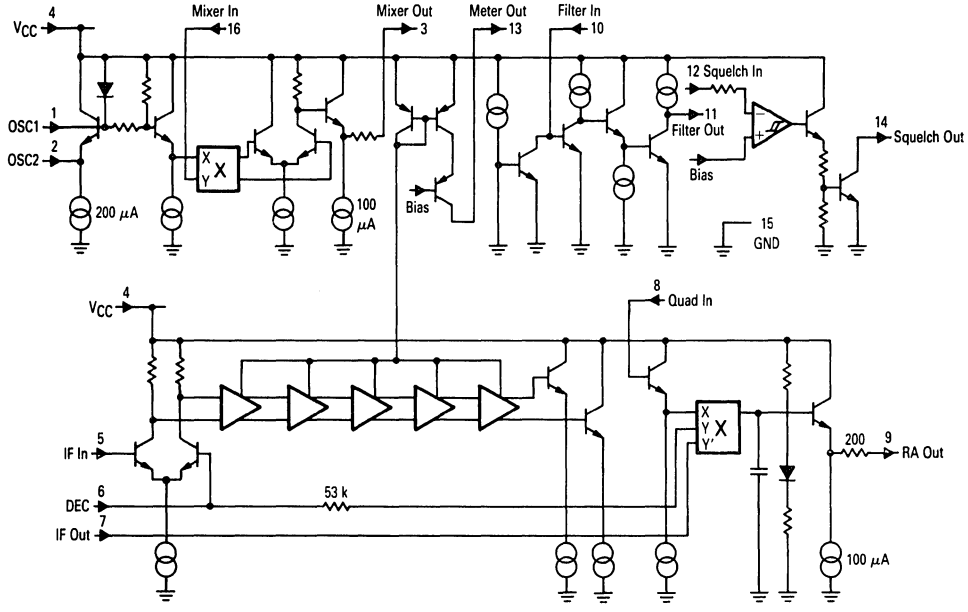


FIGURE 9 — MC3372 CIRCUIT SCHEMATIC



8

CIRCUIT DESCRIPTION

The MC3371 and MC3372 are low power narrowband FM receivers with an operating frequency of up to 60 MHz. Its low voltage design provides low power drain, excellent sensitivity, and good image rejection in narrowband voice and data link applications.

This part combines a mixer, an IF (intermediate frequency) limiter with a logarithmic response signal strength indicator, a quadrature detector, an active filter and a squelch trigger circuit. In a typical application, the mixer amplifier converts an RF input signal to a 455 kHz IF signal. Passing through an external bandpass filter, the IF signal is fed into a limiting amplifier and detection circuit where the audio signal is recovered. A conventional quadrature detector is used.

The absence of an input signal is indicated by the presence of noise above the desired audio frequencies. This "noise band" is monitored by an active filter and a detector. A squelch switch is used to mute the audio when noise or a tone is present. The input signal level is monitored by a meter drive circuit which detects the amount of IF signal in the limiting amplifier.

APPLICATION

The oscillator is an internally biased Colpitts type with the collector, base, and emitter connections at Pins 4, 1 and 2 respectively. This oscillator can be run under crystal control. For fundamental mode crystals use crystal characterized parallel resonant for 32 pF load. For higher frequencies, use 3rd overtone series mode type crystals. The coil (L2) and resistor RD (R13) are needed to ensure proper and stable operation at the LO frequency (see Figure 12, 45 MHz application circuit).

The mixer is doubly balanced to reduce spurious radiation. Conversion gain stated in the AC Electrical Characteristics table is typically 20 dB. This power gain measurement was made under stable conditions using a 50 Ω source at the input and an external load provided by a 455 kHz ceramic filter at the mixer output which is connected to the V_{CC} (Pin 4) and IF input (Pin 5). The filter impedance closely matches the 1.8 kΩ internal load resistance at Pin 3 (mixer output). Since the input impedance at Pin 16 is strongly influenced by a 3.3 kΩ internal biasing resistor and has a low capacitance, the useful gain is actually much higher than shown by the standard power gain measurement. The Smith Chart plot in Figure 16 shows the measured mixer input impedance versus input frequency with the mixer input matched to a 50 Ω source impedance at the given frequencies. In order to assure stable operation under matched conditions, it is necessary to provide a shunt resistor to ground. Figures 10, 11 and 12 show the input networks used to derive the mixer input impedance data.

Following the mixer, a ceramic bandpass filter is recommended for IF filtering (i.e. 455 kHz types having a bandwidth of ±2.0 kHz to ±15 kHz with an input and output impedance from 1.5 kΩ to 2.0 kΩ). The 6 stage limiting IF amplifier has approximately 92 dB of gain. The MC3371 and MC3372 are different in the limiter and quadrature detector circuits. The MC3371 has a 1.8 kΩ and a 51 kΩ resistor providing internal DC biasing and the output of the limiter is internally connected, both directly and through a 10 pF capacitor to the quadrature detector; whereas, in the MC3372 these components are not provided internally. Thus, in the MC3371, no external components are necessary to match the 455 kHz ceramic filter, while in the MC3372, external 1.8 kΩ and 51 kΩ biasing resistors are needed between Pins 5 and 7, respectively (see Figures 11 and 12).

In the MC3371, a parallel LCR quadrature tank circuit is connected externally from Pin 8 to V_{CC} (similar to the MC3361). In the MC3372, a quadrature capacitor is needed externally from Pin 7 to Pin 8 and a parallel LC or a ceramic discriminator with a damping resistor is also needed from Pin 8 to V_{CC} (similar to the MC3357). The above external quadrature circuitry provides 90° phase shift at the IF center frequency and enables recovered audio.

The damping resistor determines the peak separation of the detector and is somewhat critical. As the resistor is decreased, the separation and the bandwidth is increased but the recovered audio is decreased. Receiver sensitivity is dependent on the value of this resistor and the bandwidth of the 455 kHz ceramic filter.

On the chip the composite recovered audio, consisting of carrier component and modulating signal, is passed through a low pass filter amplifier to reduce the carrier component and then is fed to Pin 9 which has an output impedance of 450 Ω. The signal still requires further filtering to eliminate the carrier component, deemphasis, volume control, and further amplification before driving a loudspeaker. The relative level of the composite recovered audio signal at Pin 9 should be considered for proper interaction with an audio post amplifier and a given load element. The MC13060 is recommended as a low power audio amplifier.

The meter output indicates the strength of the IF level and the output current is proportional to the logarithm of the IF input signal amplitude. A maximum source current of 60 μA is available and can be used to drive a meter and to detect a carrier presence. This is referred to as a Received Strength Signal Indicator (RSSI). The output at Pin 13 provides a current source. Thus, a resistor to ground yields a voltage proportional to the input carrier signal level. The value of this resistor is estimated by (V_{CC}(Vdc) − 1.0 V)/60 μA; so for V_{CC} = 4.0 Vdc, the resistor is approximately 50 kΩ and provides a maximum voltage swing of about 3.0 V.

A simple inverting op amp has an output at Pin 11 and the inverting input at Pin 10. The noninverting input is connected to 2.5 V. The op amp may be used as a noise triggered squelch or as an active noise filter. The bandpass filter is designed with external impedance elements to discriminate between frequencies. With an external AM detector, the filtered audio signal is checked for a tone signal or for the presence of noise above the normal audio band. This information is applied to Pin 12.

An external positive bias to Pin 12 sets up the squelch trigger circuit such that the audio mute (Pin 14) is open or connected to ground. If Pin 12 is pulled down to 0.9 V or below by the noise or tone detector, Pin 14 is internally shorted to ground. There is about 57 mV of hyteresis at Pin 12 to prevent jitter. Audio muting is accomplished by connecting Pin 14 to the appropriate point in the audio

path between Pin 9 and an audio amplifier. The voltage at Pin 14 should not be lower than −0.7 V; this can be assured by connecting Pin 14 to the point that has no dc component.

Another possible application of the squelch switch may be as a carrier level triggered squelch circuit, similar to the MC3362/MC3363 FM receivers. In this case the meter output can be used directly to trigger the squelch switch when the RF input at the input frequency falls below the desired level. The level at which this occurs is determined by the resistor placed between the meter drive output (Pin 13) and ground (Pin 15).

FIGURE 10 — TYPICAL APPLICATION FOR MC3371 AT 10.7 MHz

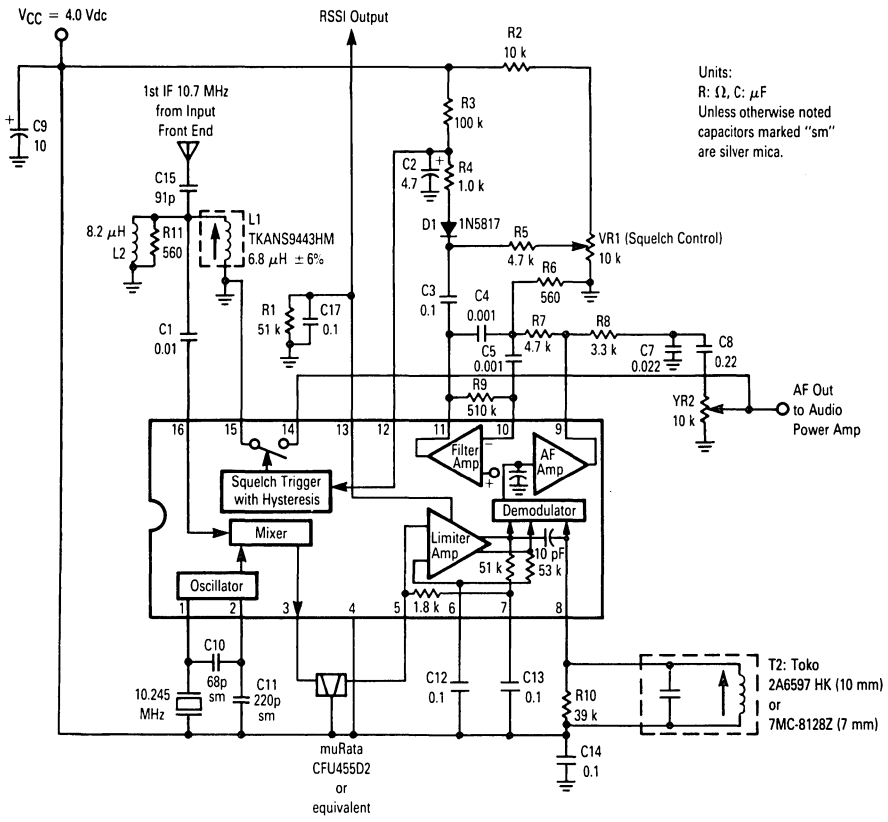


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FIGURE 11 — TYPICAL APPLICATION FOR MC3372 AT 10.7 MHz

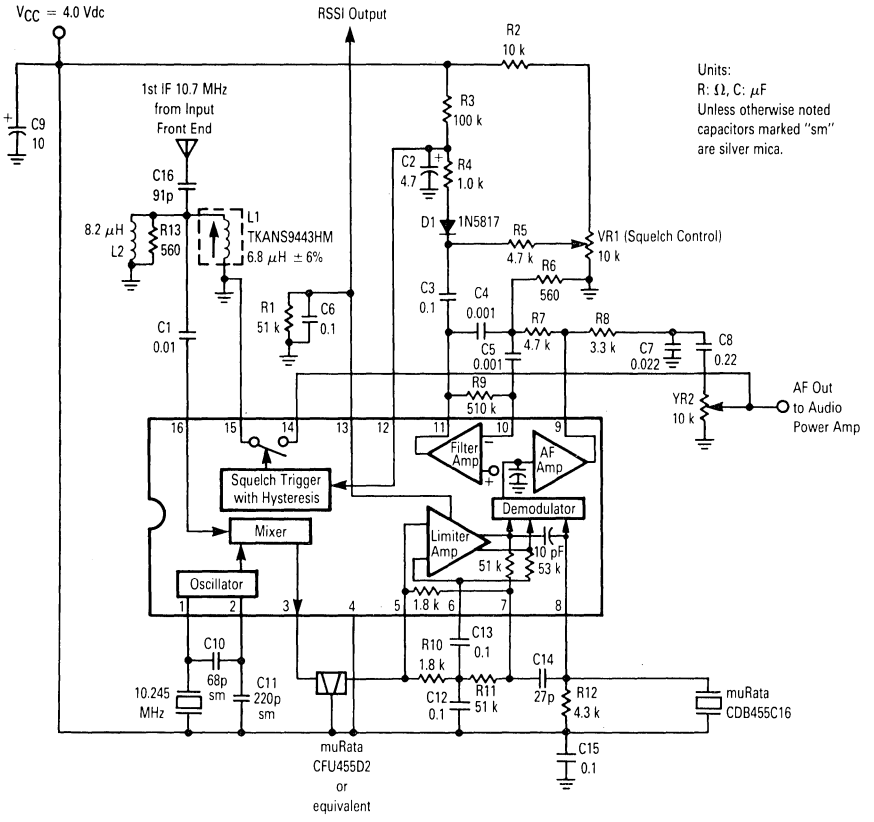

FIGURE 12 — TYPICAL APPLICATION FOR MC3372 AT 45 MHz

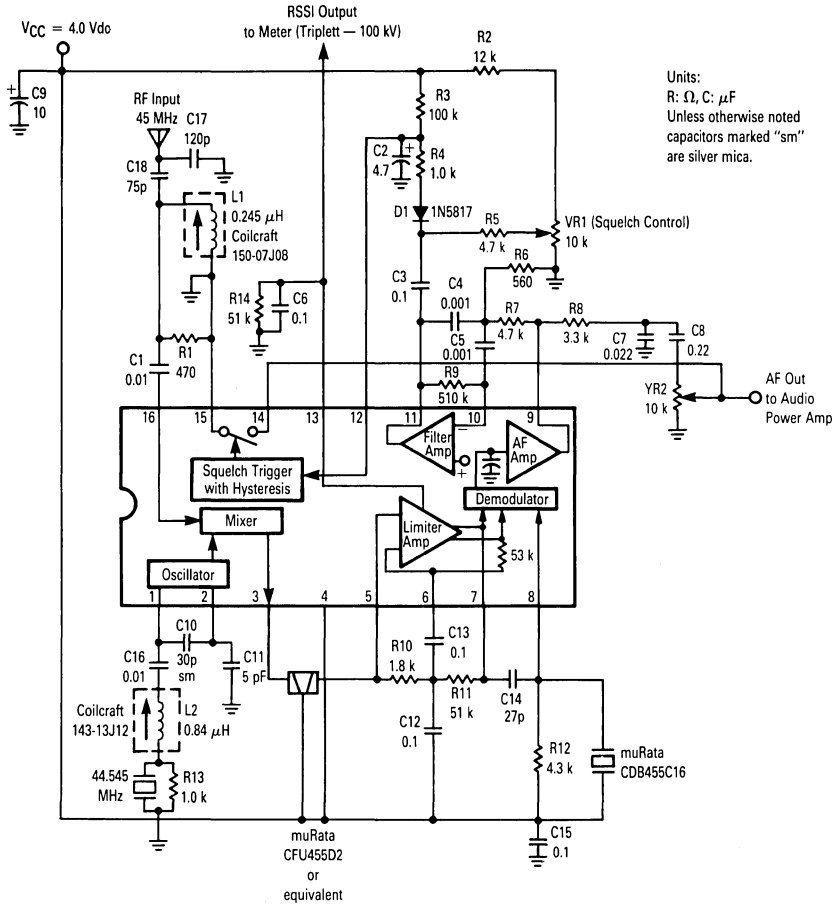

FIGURE 13 — RSSI OUTPUT versus RF INPUT

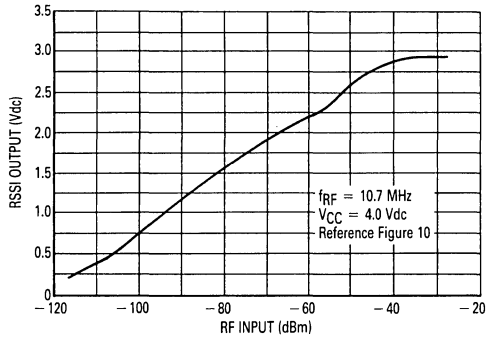

FIGURE 14 — RSSI OUTPUT versus RF INPUT

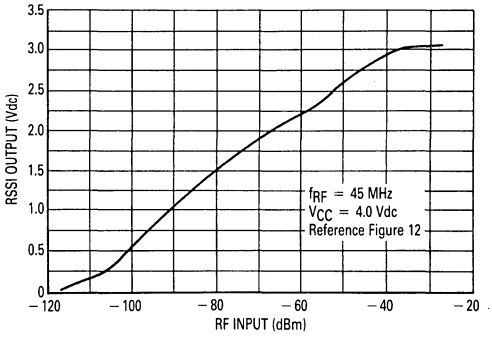

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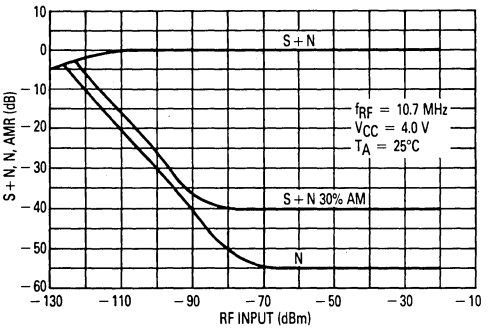
FIGURE 15 — S+N, N, AMR versus INPUT



*REFERENCE FIGURES 10, 11 & 12

FIGURE 16 — MIXER INPUT IMPEDANCE versus FREQUENCY

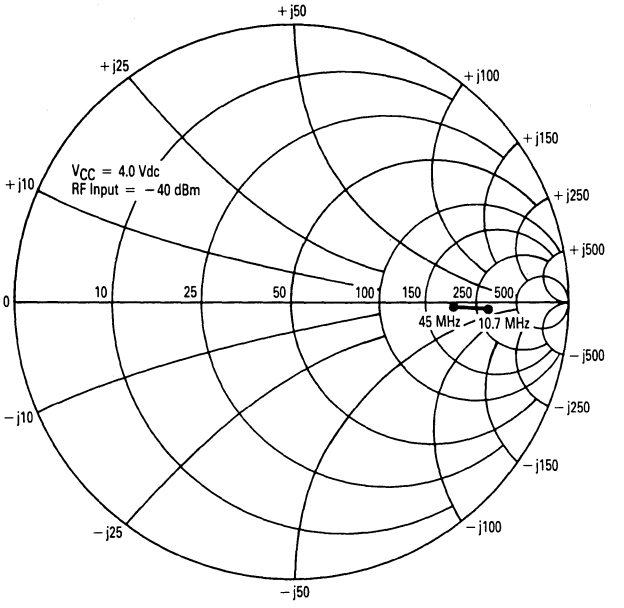


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FIGURE 17 — MC3371P PC BOARD COMPONENT VIEW WITH MATCHED INPUT AT 10.7 MHz

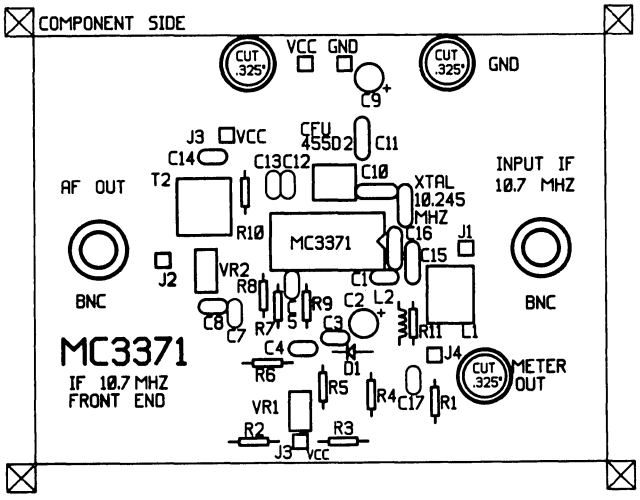

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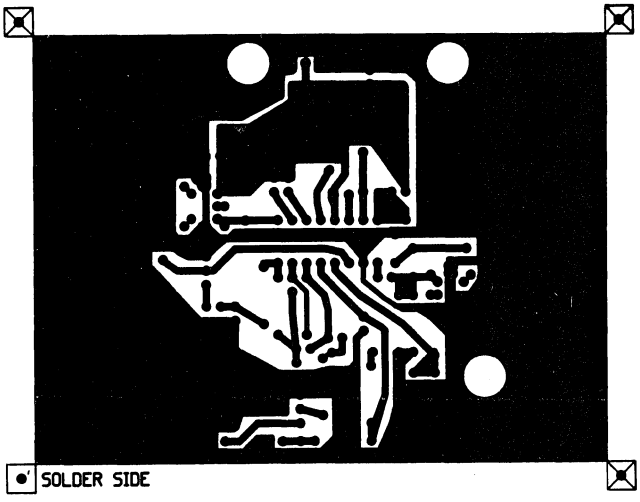
FIGURE 18 — MC3371P PC BOARD CIRCUIT OR SOLDER SIDE AS VIEWED THRU COMPONENT SIDE



Above PC Board is laid out for the circuit in Figure 10.

FIGURE 19 — MC3372P PC BOARD COMPONENT VIEW WITH MATCHED INPUT AT 10.7 MHz

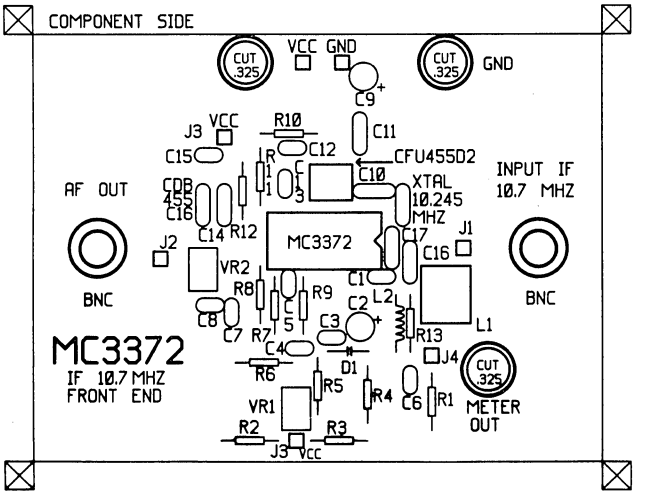


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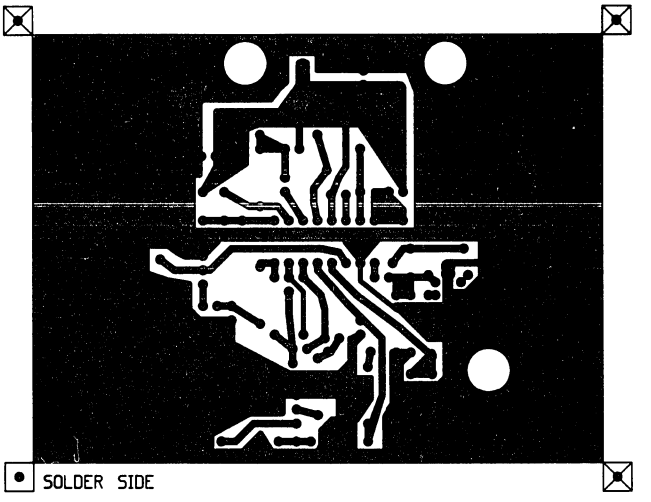
FIGURE 20 — MC3372P PC BOARD CIRCUIT OR SOLDER SIDE AS VIEWED THRU COMPONENT SIDE



Above PC Board is laid out for the circuit in Figure 11.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC13055

WIDEBAND FSK RECEIVER

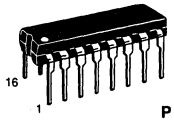
MONOLITHIC SILICON INTEGRATED CIRCUIT

Advance Information

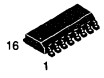
Wideband FSK Receiver

The MC13055 is intended fo RF data link systems using carrier frequencies up to 40 MHz and FSK (frequency shift keying) data rates up to 2.0 M Baud (1.0 MHz). This design is similar to the MC3356, except that it does not include the oscillator/mixer. The IF bandwidth has been increased and the detector output has been revised to a balanced configuration. The received signal strength metering circuit has been retained, as has the versatile data slicer/comparator.

- Input Sensitivity 20 µV @ 40 MHz
- Signal Strength Indicator Linear Over 3 Decades
- Available in Surface Mount Package
- Easy Application, Few Peripheral Components

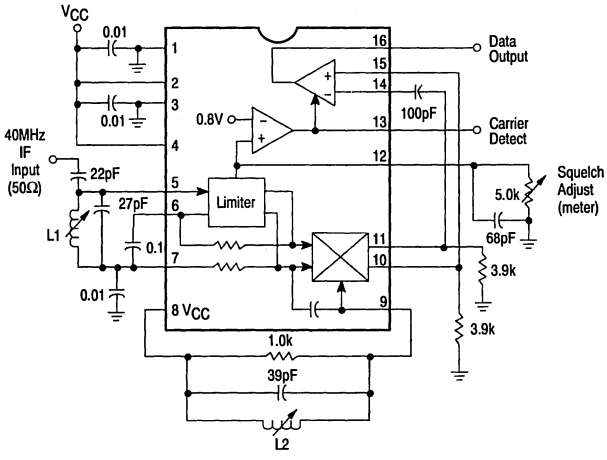


P SUFFIX
PLASTIC PACKAGE
CASE 648

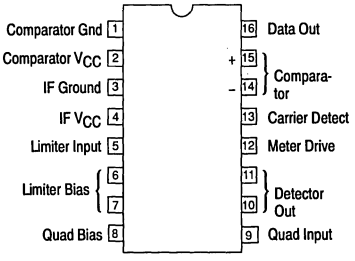


D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO-16)

Figure 1. Block Diagram and Application Circuit



PIN CONNECTIONS



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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	$V_{CC(max)}$	15	Vdc
Operating Supply Voltage Range	V2, V4	3.0 to 12	Vdc
Junction Temperature	T_J	150	°C
Operating Ambient Temperature Range	T_A	–40 to +85	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Power Dissipation, Package Rating	P_D	1.25	W

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc, f_o = 40 MHz, f_{mod} = 1.0 MHz, Δf = ±1.0 MHz, T_A = 25°C, test circuit of Figure 2.)

Characteristics		Measure	Min	Typ	Max	Unit
Total Drain Current		12 + 14	—	20	25	mA
Data Comparator Pull-Down Current		I16	—	10	—	mA
Meter Drive Slope versus Input		I12	4.5	7.0	9.0	µA/dB
Carrier Detect Pull-Down Current		I13	—	1.3	—	mA
Carrier Detect Pull-Up Current		I13	—	500	—	µA
Carrier Detect Threshold Voltage		V12	700	800	900	mV
DC Output Current		I10, I11	—	430	—	µA
Recovered Signal		V10 – V11	—	350	—	mVrms
Sensitivity for 20 dB S + N/N, BW = 5.0 MHz		VIN	—	20	—	µVrms
S + N/N at V_{in} = 50 µV		V10 – V11	—	30	—	dB
Input Impedance @ 40 MHz	R_{in}	Pin 5, Ground	—	4.2	—	kΩ
	C_{in}		—	4.5	—	pF
Quadrature Coil Loading	R_{in}	Pin 9 to 8	—	7.6	—	kΩ
	C_{in}		—	5.2	—	pF

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Figure 2. Test Circuit

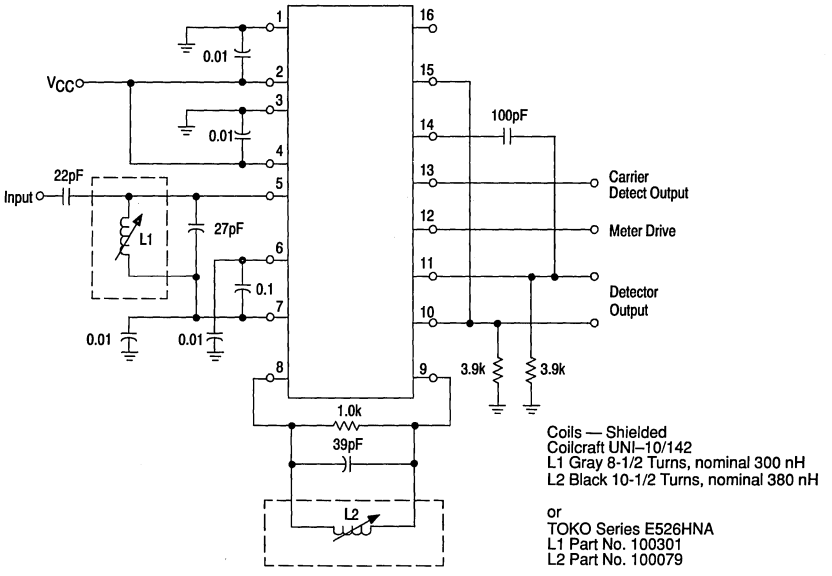

Figure 3. Overall Gain, Noise, AM Rejection

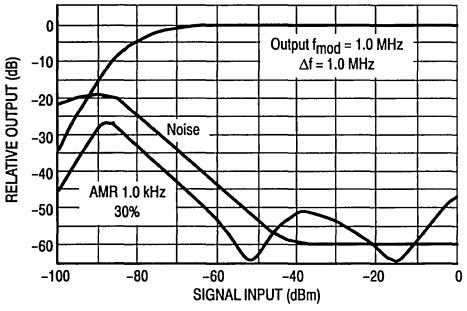

Figure 4. Meter Current versus Signal

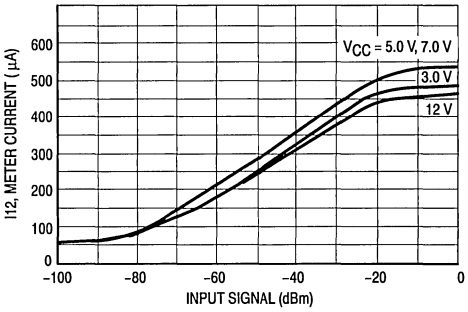

Figure 5. Untuned Input: Limiting Sensitivity versus Frequency

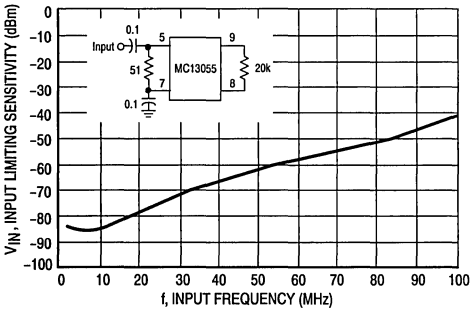

Figure 6. Untuned Input: Meter Current versus Frequency

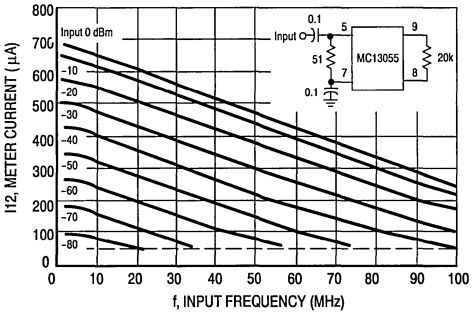

Figure 7. Limiting Sensitivity and Detuning versus Supply Voltage

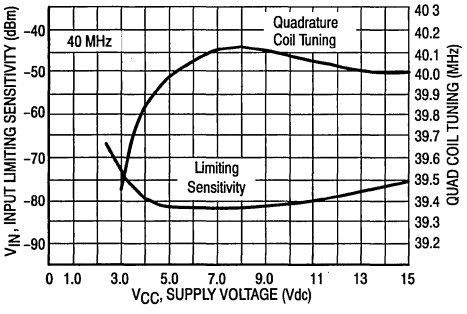

Figure 8. Detector Current and Power Supply Current versus Supply Voltage

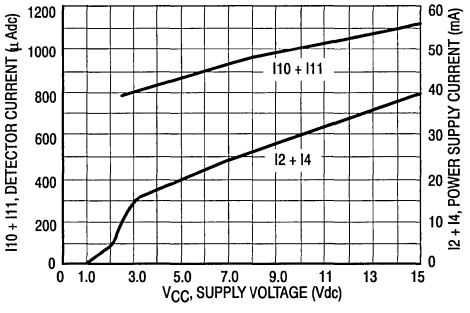

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Figure 9. Recovered Audio versus Temperature

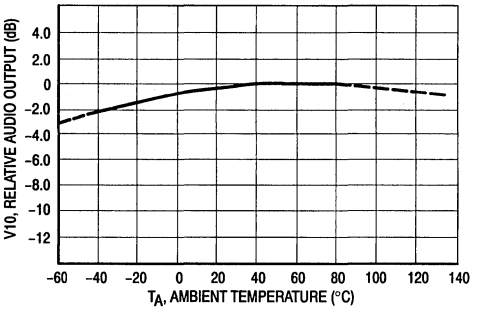

Figure 10. Carrier Detect Threshold versus Temperature

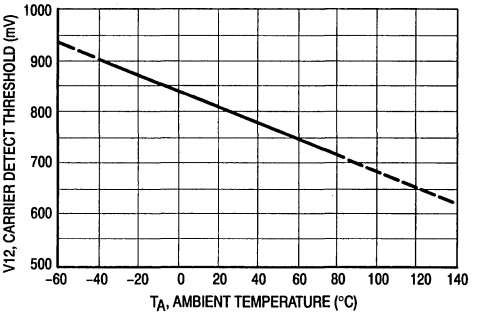

Figure 11. Meter Current versus Temperature

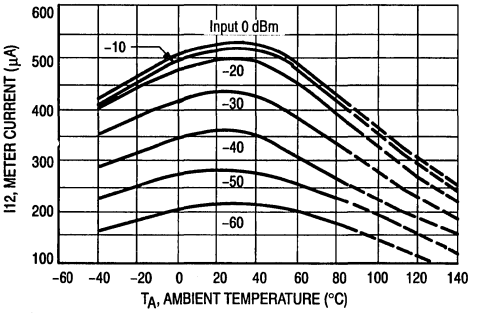

Figure 12. Input Limiting versus Temperature

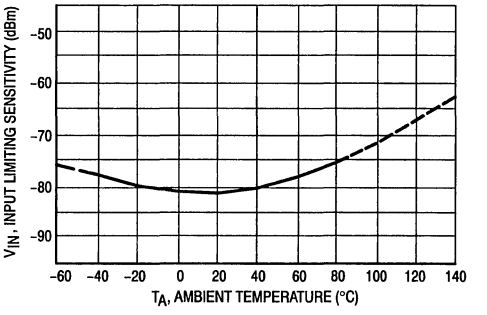

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Figure 13. Input Impedance, Pin 5

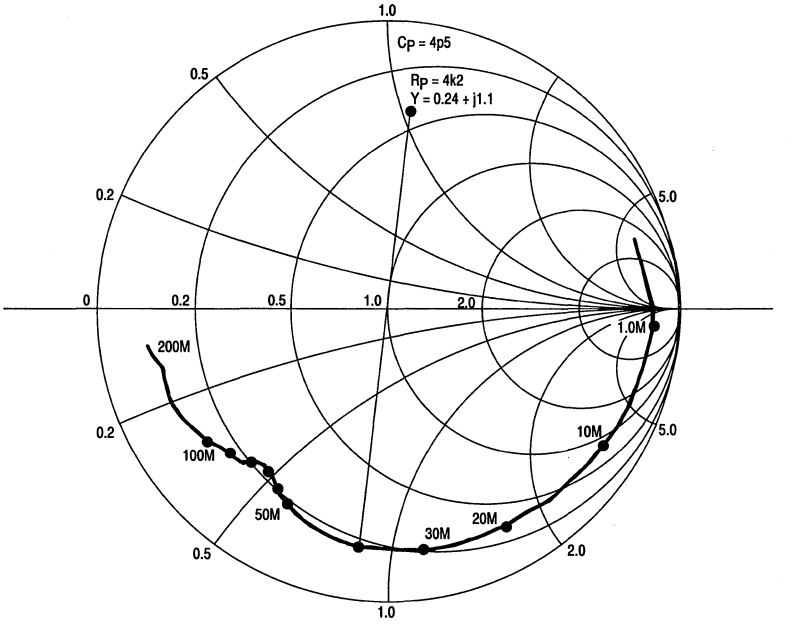
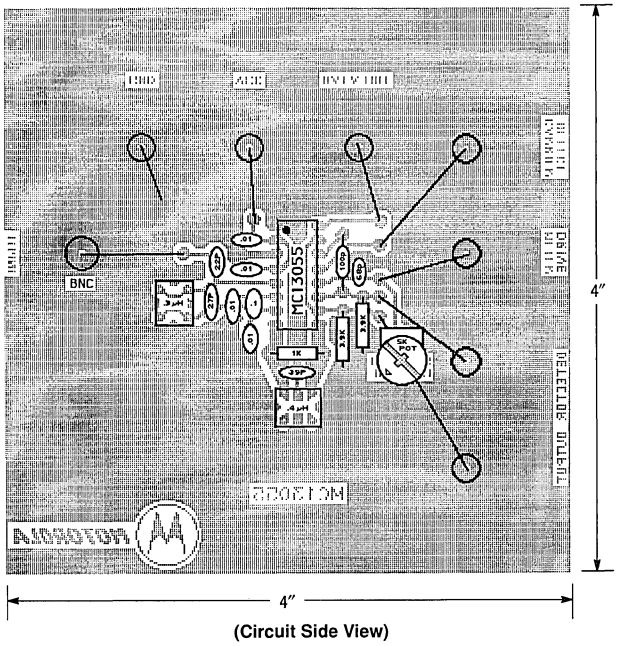
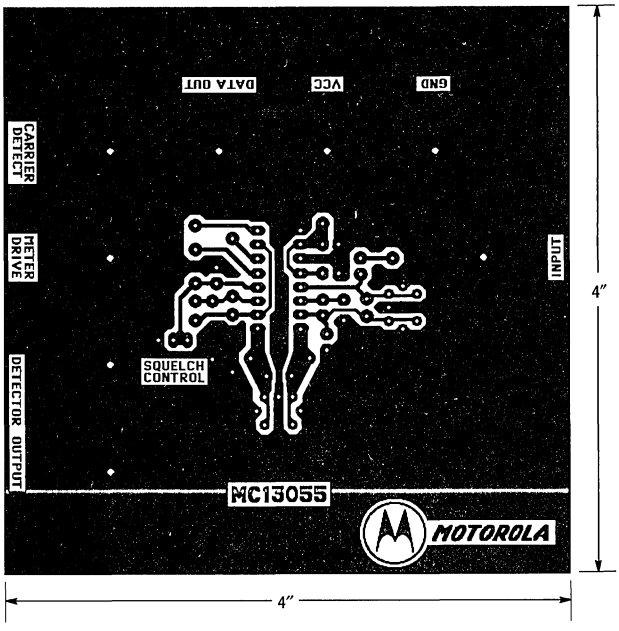


Figure 14. Test Fixture
(Component Layout)



(Circuit Side View)



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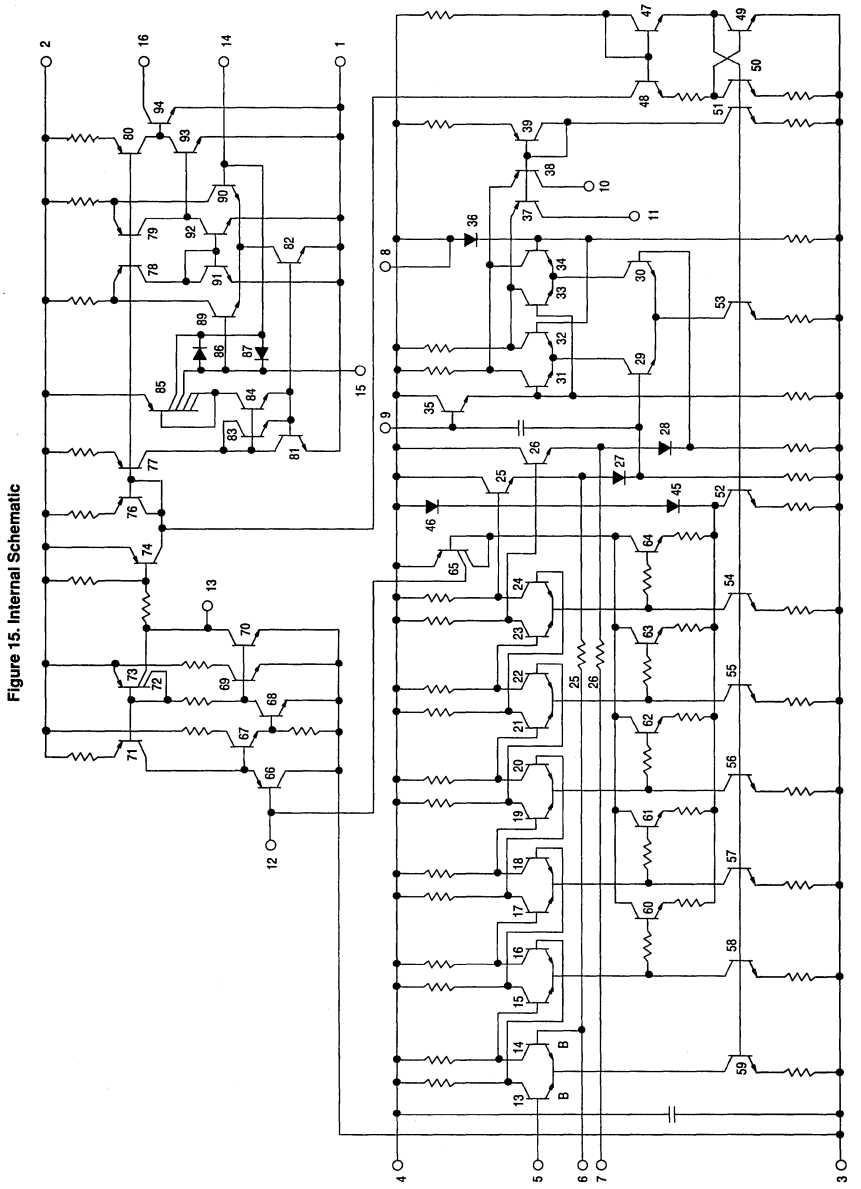


Figure 15. Internal Schematic

GENERAL DESCRIPTION

The MC13055 is an extended frequency range FM IF, quadrature detector, signal strength detector and data shaper. It is intended primarily for FSK data systems. The design is very similar to MC3356 except that the oscillator/mixer has been removed, and the frequency capability of the IF has been raised about 2:1. The detector output configuration has been changed to a balanced, open-collector type to permit symmetrical drive of the data shaper (comparator). Meter drive and squelch features have been retained.

The limiting IF is a high frequency type, capable of being operated up to 100 MHz. It is expected to be used at 40 MHz in most cases. The quadrature detector is internally coupled to the IF, and a 2.0 pF quadrature capacitor is internally provided. The 20 dB quieting sensitivity is approximately 20 μV, tuned input, and the IF can accept signals up to 220 mVrms without distortion or change of detector quiescent DC level.

The IF is unusual in that each of the last 5 stages of the 6 stage limiter contains a signal strength sensitive, current sinking device. These are parallel connected and buffered to produce a signal strength meter drive which is fairly linear for IF input signals of 20 μV to 20 mVrms. (See Figure 4.)

A simple squelch arrangement is provided whereby the meter current flowing through the meter load resistance flips a comparator at about 0.8 Vdc above ground. The signal strength at which this occurs can be adjusted by changing the meter load resistor. The comparator (+) input and output are available to permit control of hysteresis. Good positive action can be obtained for IF input signals of above 20 μVrms. A resistor (R) from Pin 13 to Pin 12 will provide V_{CC}/R of feedback current. This current can be correlated to an amount of signal strength hysteresis by using Figure 4.

The squelch is internally connected to the data shaper. Squelch causes the data shaper to produce a high (V_{CC}) output.

The data shaper is a complete "floating" comparator, with diodes across its inputs. The outputs of the quadrature detector can be fed directly to either or preferably both inputs of the comparator to produce a squared output swinging from V_{CC} to ground in inverted or noninverted form.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC13104
MC13105

Product Preview

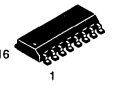
1.0 GHz Receiver LNA/Mixer/VCO

1.0 GHz RECEIVER LNA/MIXER/VCO

SILICON MONOLITHIC INTEGRATED CIRCUIT

The MC13104/13105 are fully integrated UHF down converters intended for use in receivers operating in the 800 MHz to 1.0 GHz frequency range. The design utilizes Motorola's advanced Mosaic® 3 RF bipolar process to yield high gain, low noise, low current drain in a cost effective monolithic device. The basic receiver functions of low noise amplifier, mixer and AGC are included in both devices, while the MC13104 also includes a VCO with two buffered outputs which permit simple interfacing to multichannel PLL/prescaler frequency synthesized systems. Applications for the MC13104/13105 include CT-2 cordless telephones, security monitor receivers, remote control, video and audio short range links, field disturbance receivers, and low cost cellular radios. A power down control to minimize current drain with minimum recovery/turn-on time.

- Low Cost Silicon Bipolar Design
- Internal VCO
- VCO Buffer to Drive Prescalar
- Low Drain Current: Nominal 10 mA Current Drain (ON)
- Power Down Current: Nominal 10 μA
- LNA Has AGC Input with Nominal ≥ 20 dB Range
- Performance Optimized for CT-2 and Similar Systems
- Target Noise Figure of 5.0 dB Overall at 1.0 GHz
- Input Impedance: Nominal 50 Ω



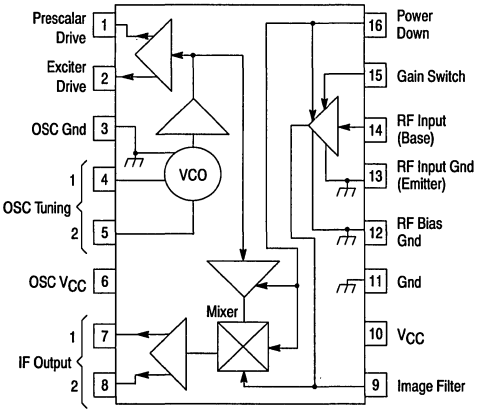
D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO-16)

ORDERING INFORMATION

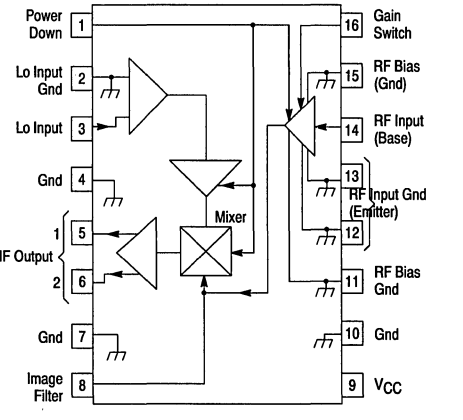
Device	Temperature Range	Package
MC13104D	– 20° to +70°C	SO-16
MC13105D		SO-16

PIN CONNECTIONS AND BLOCK DIAGRAMS

(MC13104)



(MC13105)



MC13135
MC13136

DUAL CONVERSION NARROWBAND FM RECEIVERS

SILICON MONOLITHIC INTEGRATED CIRCUIT

Advance Information

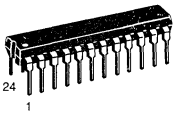
FM Communications Receivers

The MC13135/MC13136 are the second generation of single chip, dual conversion FM communications receivers developed by Motorola. Major improvements in signal handling, RSSI and first oscillator operation have been made. In addition, recovered audio distortion and audio drive have improved. Using Motorola's MOSAIC™ 1.5 process, these receivers offer low noise, high gain and stability over a wide operating voltage range.

Both the MC13135 and MC13136 include a Colpitts oscillator, VCO tuning diode, low noise first and second mixer and LO, high gain limiting IF, and RSSI. The MC13135 is designed for use with an LC quadrature detector and has an uncommitted op amp that can be used either for an RSSI buffer or as a data comparator. The MC13136 can be used with either a ceramic discriminator or an LC quad coil and the op amp is internally connected for a voltage buffered RSSI output.

These devices can be used as stand-alone VHF receivers or as the lower IF of a triple conversion system. Applications include cordless telephones, short range data links, walkie-talkies, low cost land mobile, amateur radio receivers, baby monitors and scanners.

- Complete Dual Conversion FM Receiver – Antenna Input to Audio Output
- Voltage Buffered RSSI with 70 dB of Usable Range
- Low Voltage Operation – 2.0 to 6.0 Vdc (2 Cell NiCad Supply)
- Low Current Drain – 3.5 mA Typ
- Low Impedance Audio Output < 25 Ω
- VHF Colpitts First LO for Crystal or VCO Operation
- Isolated Tuning Diode
- Buffered First LO Output to Drive CMOS PLL Synthesizer



P SUFFIX
PLASTIC PACKAGE
CASE 724

DW SUFFIX
PLASTIC PACKAGE
CASE 751E
(SO-24L)

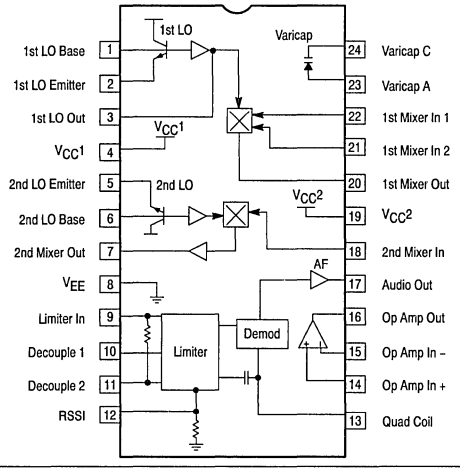
ORDERING INFORMATION

Device	Temperature Range	Package
MC13135P	– 40° to +85°C	Plastic DIP
MC13135DW		SO-24L
MC13136P		Plastic DIP
MC13136DW		SO-24L

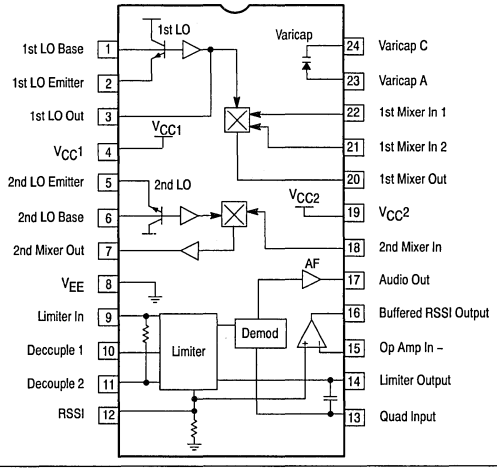
8

PIN CONNECTIONS

MC13135



MC13136



MAXIMUM RATINGS

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage	4, 19	V_{CC} (max)	6.5	Vdc
RF Input Voltage	22	RF_{in}	1.0	Vrms
Junction Temperature	—	T_J	+150	°C
Storage Temperature Range	—	T_{stg}	– 65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage	4, 19	V_{CC}	2.0 to 6.0	Vdc
Maximum 1st IF	—	f_{IF1}	21	MHz
Maximum 2nd IF	—	f_{IF2}	3.0	MHz
Ambient Temperature Range	—	T_A	– 40 to + 85	°C

ELECTRICAL CHARACTERISTICS (T_A=25°C, V_{CC}=4.0 Vdc, f_o=49.7 MHz, f_{MOD}=1.0 kHz, Deviation=±3.0 kHz, f_{1stLO}=39 MHz, $f_{2nd\ LO}$=10.245 MHz, IF1=10.7 MHz, IF2=455 kHz, unless otherwise noted. All measurements performed in the test circuit of Figure 1.)

Characteristic	Condition	Symbol	Min	Typ	Max	Unit
Total Drain Current	No Input Signal	I_{CC}	—	4.0	6.0	mAdc
Sensitivity (Input for 12 dB SINAD)	Matched Input	V_{SIN}	—	1.0	—	µVrms
Recovered Audio MC13135 MC13136	V_{RF} = 1.0 mV	AF_O	 170 215	 220 265	 270 315	mVrms
Limiter Output Level (Pin 14, MC13136)		V_{LIM}	—	130	—	mVrms
1st Mixer Conversion Gain	V_{RF} = – 40 dBm	MX_{gain1}	—	12	—	dB
2nd Mixer Conversion Gain	V_{RF} = – 40 dBm	MX_{gain2}	—	13	—	dB
First LO Buffered Output	—	V_{LO}	—	100	—	mVrms
Total Harmonic Distortion	V_{RF} = – 30 dBm	THD	—	1.2	3.0	%
Demodulator Bandwidth	—	BW	—	50	—	kHz
RSSI Dynamic Range	—	RSSI	—	70	—	dB
First Mixer 3rd Order Intercept (Input) Matched Unmatched		TOI_{Mix1}	 — —	 –17 –11	 — —	dBm
Second Mixer 3rd Order Intercept (RF Input)	Matched Input	TOI_{Mix2}	—	– 27	—	dBm
First LO Buffer Output Resistance	—	R_{LO}	—	—	—	Ω
First Mixer Parallel Input Resistance	—	R	—	722	—	Ω
First Mixer Parallel Input Capacitance	—	C	—	3.3	—	pF
First Mixer Output Impedance	—	ZO	—	330	—	Ω
Second Mixer Input Impedance	—	Z_I	—	40	—	kΩ
Second Mixer Output Impedance	—	ZO	—	1.8	—	kΩ
Detector Output Impedance	—	ZO	—	25	—	Ω

8

TEST CIRCUIT INFORMATION

Although the MC13136 can be operated with a ceramic discriminator, the recovered audio measurements for both the MC13135 and MC13136 are made with an LC quadrature detector. The typical recovered audio will depend on the external circuit; either the Q of the quad coil, or the RC matching network for the ceramic discriminator. On the MC13136, an external capacitor between Pins 13 and 14 can be used with a quad coil for slightly higher recovered audio. See Figures 10 through 13 for additional information.

Since adding a matching circuit to the RF input increases the signal level to the mixer, the third order intercept (TOI) point is better with an unmatched input (50 Ω from Pin 21 to Pin 22). Typical values for both have been included in the Electrical Characterization Table. TOI measurements were taken at the pins with a high impedance probe/spectrum analyzer system. The first mixer input impedance was measured at the pin with a network analyzer.

Figure 1a. MC13135 Test Circuit

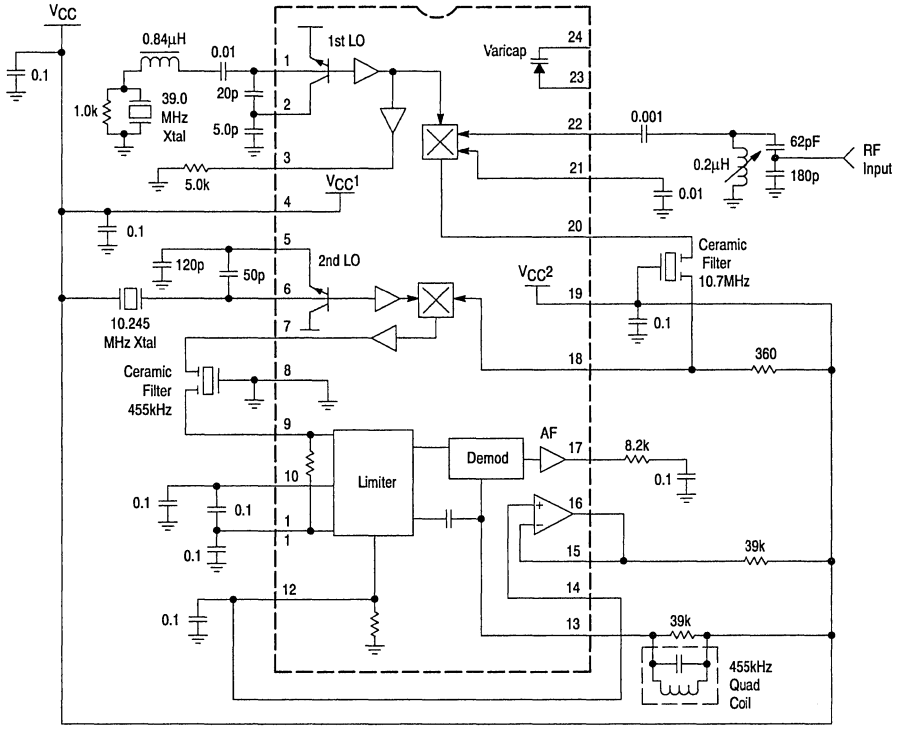


Figure 1b. MC13136 Quad Detector Test Circuit

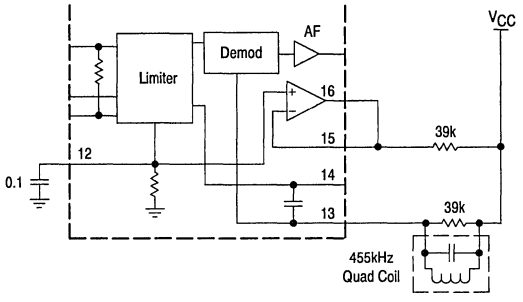


Figure 2. Supply Current versus Supply Voltage

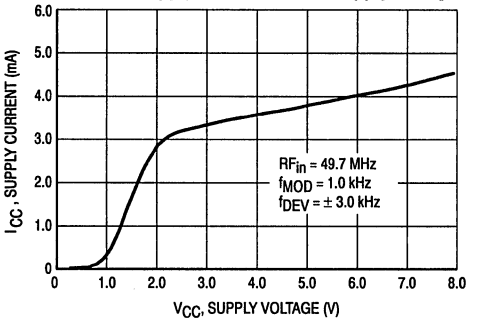


Figure 3. RSSI Output versus RF Input

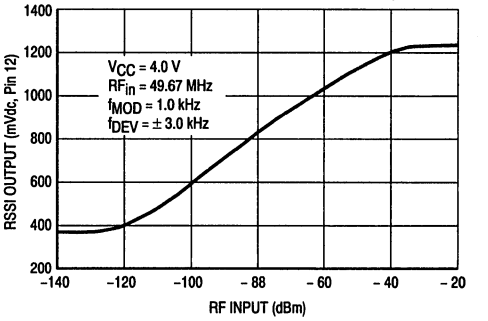


Figure 4. Varactor Capacitance, Resistance versus Bias Voltage

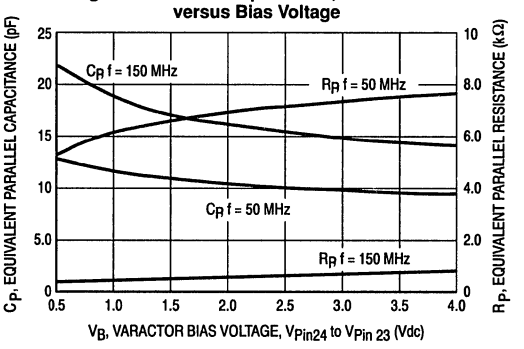


Figure 5. Oscillator Frequency versus Varactor Bias

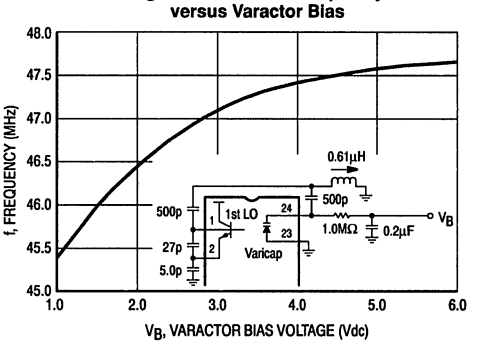


Figure 6. Signal Levels versus RF Input

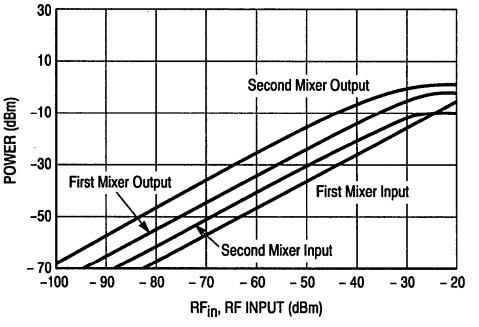


Figure 7. Signal + Noise, Noise, and AM Rejection versus Input Power

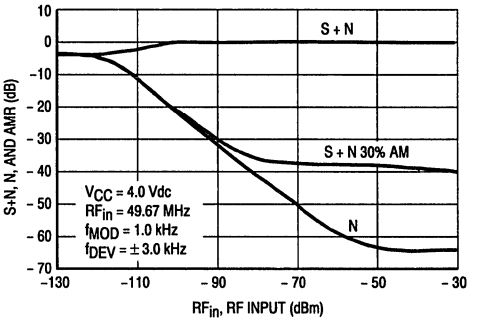


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Figure 8. Op Amp Gain and Phase versus Frequency

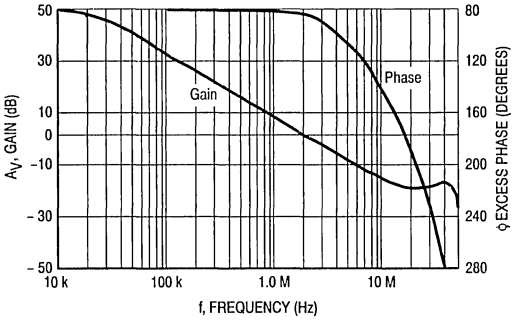


Figure 9. First Mixer Third Order Intermodulation (Unmatched Input)

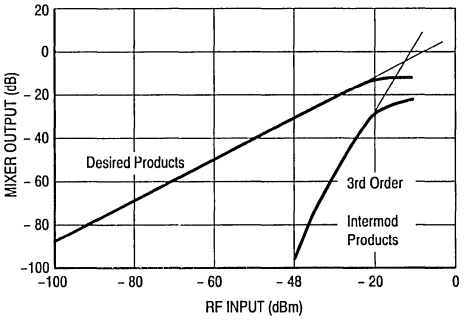


Figure 10. Recovered Audio versus Deviation for MC13135

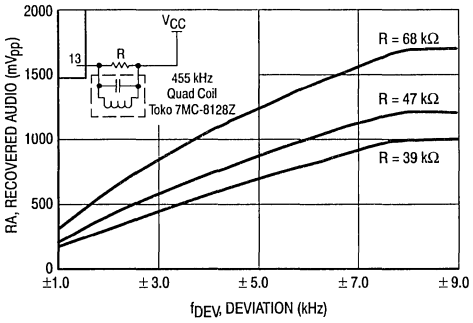


Figure 11. Distortion versus Deviation for MC13135

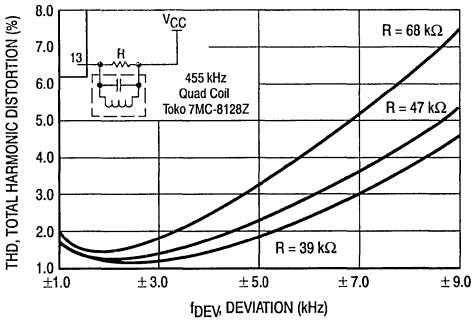


Figure 12. Recovered Audio versus Deviation for MC13136

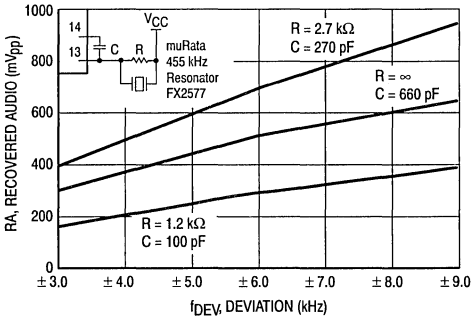
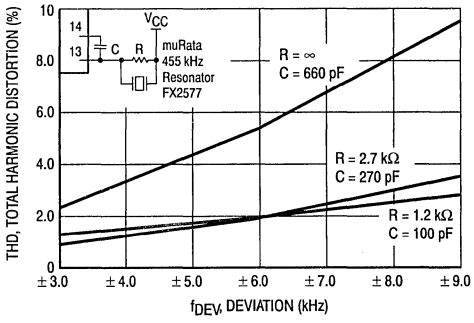


Figure 13. Distortion versus Deviation for MC13136



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CIRCUIT DESCRIPTION

The MC13135/13136 are complete dual conversion receivers. They include two local oscillators, two mixers, a limiting IF amplifier and detector, and an op amp. Both provide a voltage buffered RSSI with 70 dB of usable range, isolated tuning diode and buffered LO output for PLL operation, and a separate V_{CC} pin for the first mixer and LO. Improvements have been made in the temperature performance of both the recovered audio and the RSSI.

V_{CC}

Two separate V_{CC} lines enable the first LO and mixer to continue running while the rest of the circuit is powered down. They also isolate the RF from the rest of the internal circuit.

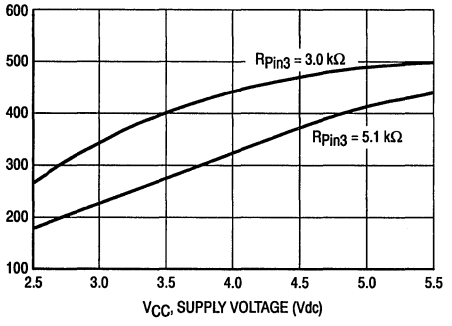
Local Oscillators

The local oscillators are grounded collector Colpitts, which can be easily crystal-controlled or VCO controlled with the on-board varactor and external PLL. The first LO transistor is internally biased, but the emitter is pinned-out and I_Q can be increased for high frequency or VCO operation. The collector is not pinned out, so for crystal operation, the LO is generally limited to 3rd overtone crystal frequencies; typically around 60 MHz. For higher frequency operation, the LO can be provided externally as shown in Figure 16.

Buffer

The buffer on the 1st LO output converts the single-ended LO output to a differential signal to drive the mixer. Capacitive coupling between the LO and buffer minimizes the effects of the change in oscillator current on the mixer. The buffered LO output is pinned-out for use with a PLL, with a typical output voltage of 320 mVp-p at V_{CC} = 4.0 V and with a 5.1 k resistor from Pin 3 to ground. As seen in Figure 14, the buffered LO output varies with the supply voltage and a smaller external resistor may be needed for low voltage operation. The LO buffer operates up to 60 MHz, typically.

Figure 14. Buffered LO Output Voltage versus Supply Voltage



Mixers

The first and second mixer are of similar design. Both are double balanced to suppress the LO and input frequencies to give only the sum and difference frequencies out. This configuration typically provides 40 to 60 dB of LO suppression. New design techniques provide improved mixer linearity and third order intercept without increased noise. The gain on the output of the 1st mixer starts to roll off at about 20 MHz, so this receiver could be used with a 21 MHz first IF. It is designed for use with a ceramic filter, with an output impedance of 330 Ω. A series resistor can be used to raise the impedance for use with a crystal filter, which typically has an input impedance of 4.0 kΩ. The second mixer input impedance is approximately 4.0 kΩ; it requires an external 360 Ω parallel resistor for use with a standard ceramic filter.

Limiting IF Amplifier and Detector

The limiter has approximately 110 dB of gain, which starts rolling off at 2.0 MHz. Although not designed for wideband operation, the bandwidth of the audio frequency amplifier has been widened to 50 kHz, which gives less phase shift and enables the receiver to run at higher data rates. However, care should be taken not to exceed the bandwidth allowed by local regulations.

The MC13135 is designed for use with an LC quadrature detector, and does not have sufficient drive to be used with a ceramic discriminator. The MC13136 was designed to use a ceramic discriminator, but can also be run with an LC quad coil, as mentioned in the Test Circuit Information section. The data shown in Figures 12 and 13 was taken using a muRata FX2577 ceramic discriminator which has been specially matched to the MC13136. Both the choice of discriminators and the external matching circuit will affect the distortion and recovered audio.

RSSI/Op Amp

The Received Signal Strength Indicator (RSSI) on the MC13135/13136 has about 70 dB of range. The resistor needed to translate the RSSI current to a voltage output has been included on the internal circuit, which gives it a tighter tolerance. A temperature compensated reference current also improves the RSSI accuracy over temperature. On the MC13136, the op amp on board is connected to the output to provide a voltage buffered RSSI. On the MC13135, the op amp is not connected internally and can be used for the RSSI or as a data slicer (see Figures 17c and 20b).

8

Figure 15. PLL Controlled Narrowband FM Receiver at 46/49 MHz

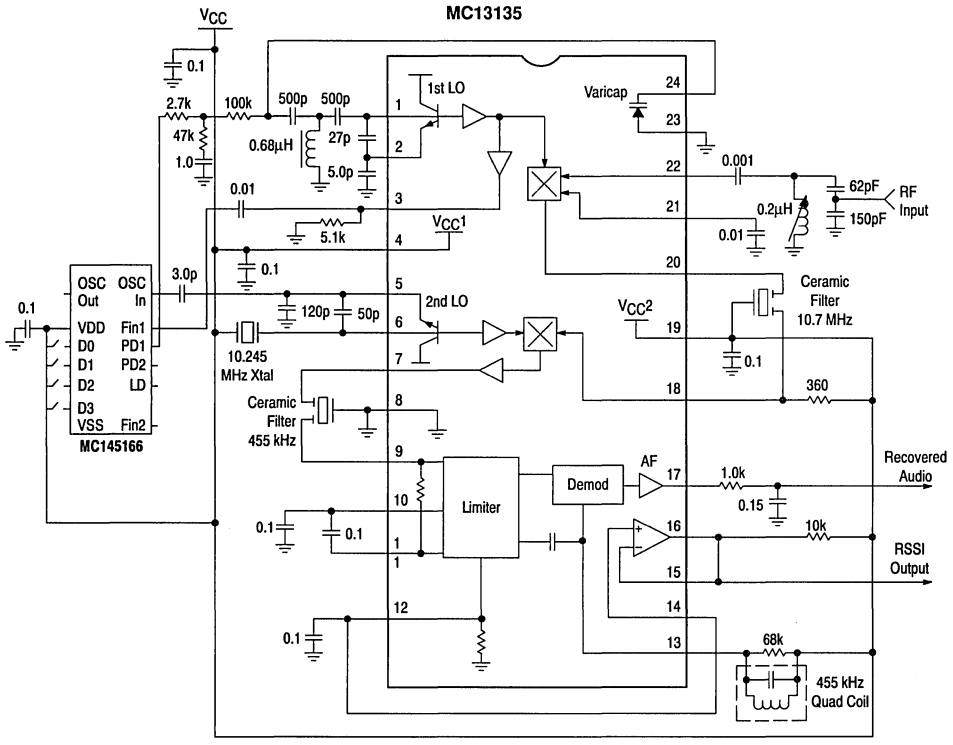
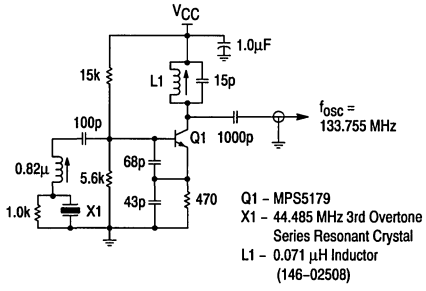


Figure 16. 144 MHz Single Channel Application Circuit

1st LO External Oscillator Circuit



Preamp for MC13135 at 144.455 MHz

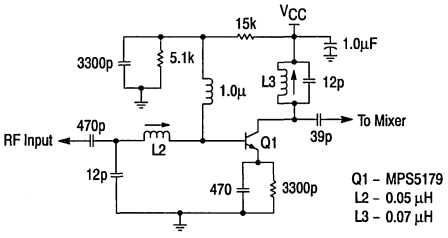


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Figure 17a. Single Channel Narrowband FM Receiver at 49.7 MHz

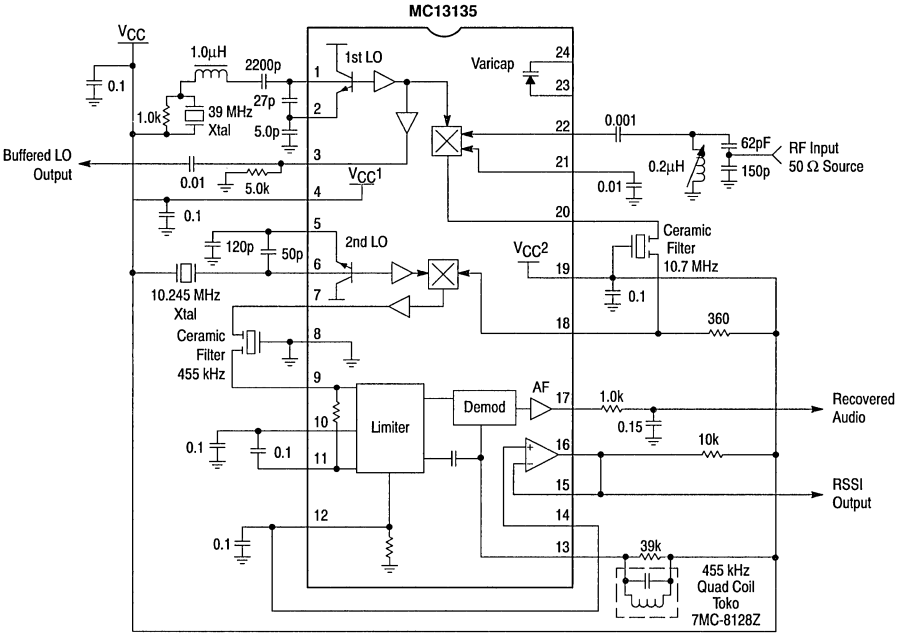


Figure 17b. PC Board Component View

NOTES: 1. 0.2 µH tunable (unshielded) inductor
2. 39 MHz Series mode resonant 3rd Overtone Crystal
3. 1.5 µH tunable (shielded) inductor
4. 10.245 MHz Fundamental mode crystal, 32 pF load
5. 455 kHz ceramic filter, muRata CFU 455B or equivalent
6. Quadrature coil, Toko 7MC-8128Z (7mm) or Toko RMC-2A6597HM (10mm)
7. 10.7 MHz ceramic filter, muRata SFE10.7MJ-A or equivalent

Figure 17c. Optional Data Slicer Circuit
(Using Internal Op Amp)

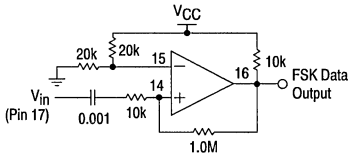
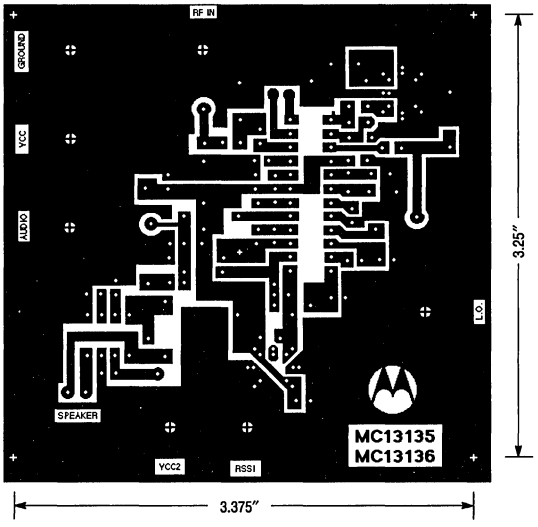


Figure 18. PC Board Solder Side View



(Circuit Side View)

Figure 19. PC Board Component View

8

NOTES: 1. 0.2 µH tunable (unshielded) inductor
2. 39 MHz Series mode resonant 3rd Overtone Crystal
3. 1.5 µH tunable (shielded) inductor
4. 10.245 MHz Fundamental mode crystal, 32 pF load
5. 455 kHz ceramic filter, muRata CFU 455B or equivalent
6. Ceramic discriminator, muRata FX2577 or equivalent
7. 10.7 MHz ceramic filter, muRata SFE10.7MJ-A or equivalent

Figure 20a. Single Channel Narrowband FM Receiver at 49.7 MHz

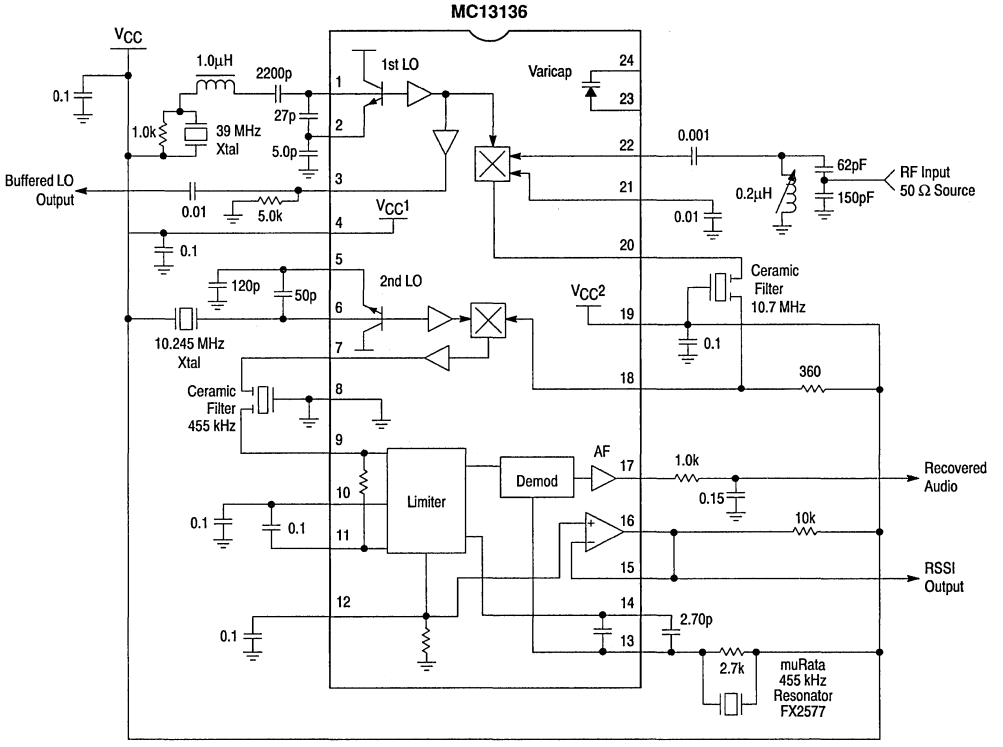


Figure 20b. Optional Audio Amplifier Circuit

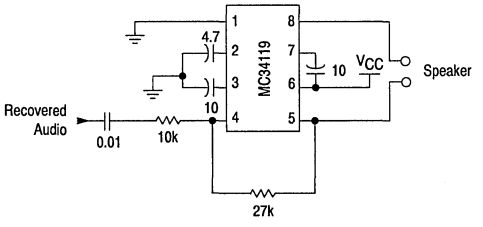


Figure 21. MC13135 Internal Schematic

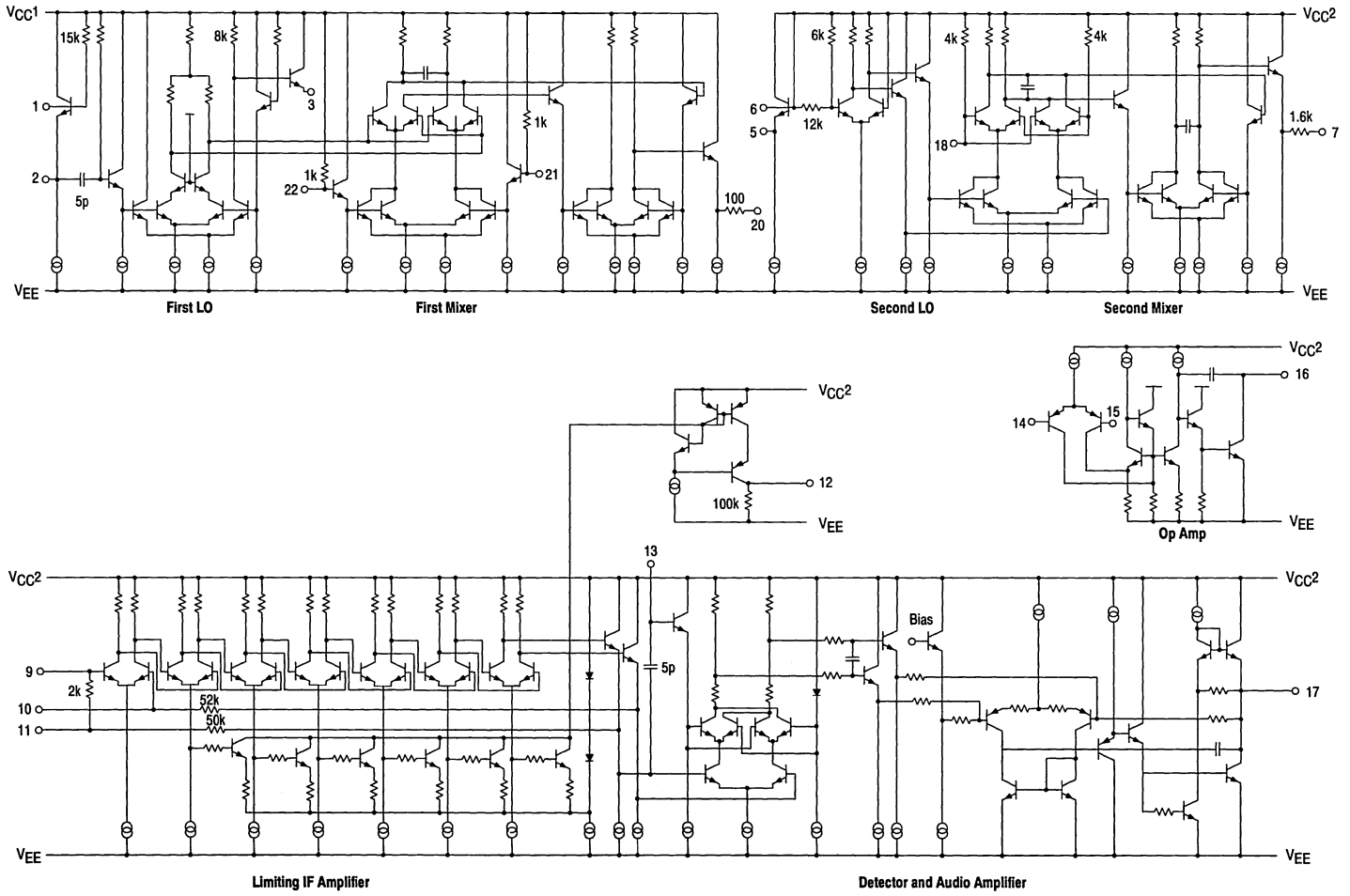
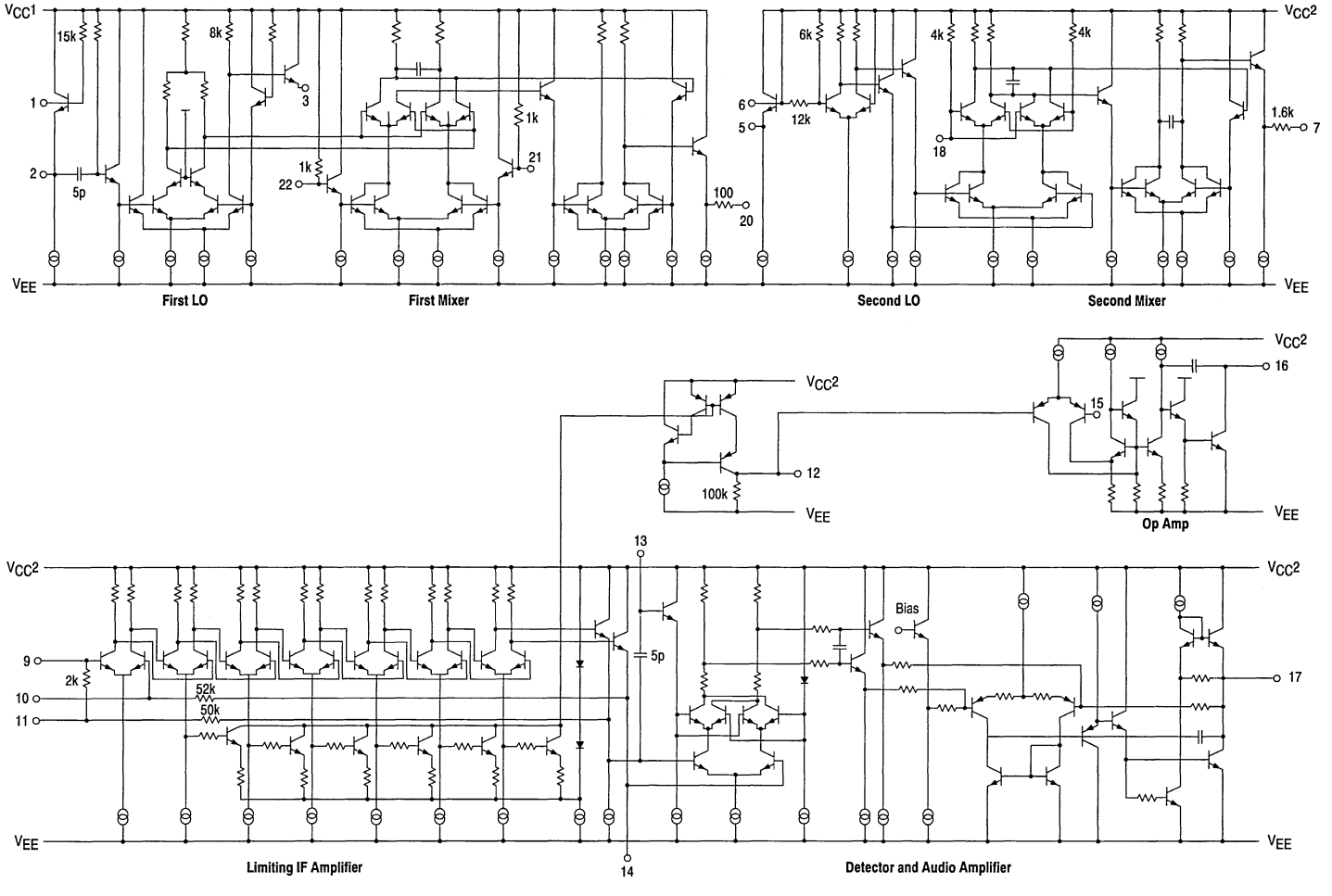


Figure 22. MC13136 Internal Schematic



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC13155

Advance Information

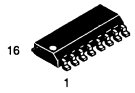
Wideband FM IF

The MC13155 is a complete wideband FM detector designed for satellite TV and other wideband data and analog FM applications. This device may be cascaded for higher IF gain and extended Receive Signal Strength Indicator (RSSI) range.

- 12 MHz Video/Baseband Demodulator
- Ideal for Wideband Data and Analog FM Systems
- Limiter Output for Cascade Operation
- Low Drain Current: 7.0 mA
- Low Supply Voltage: 3.0 to 6.0 V
- Operates to 300 MHz

WIDEBAND FM IF

SILICON MONOLITHIC INTEGRATED CIRCUIT



D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO-16)

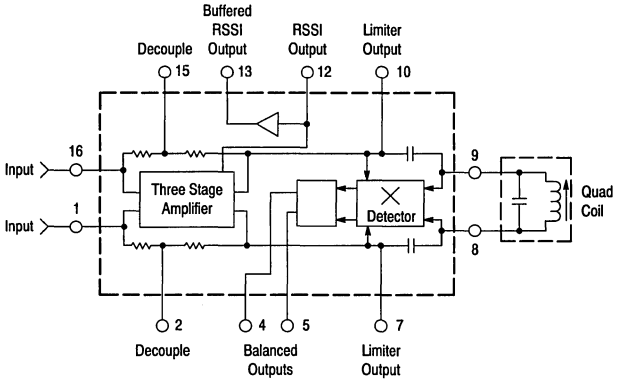
8

MAXIMUM RATINGS

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage	11, 14	V_{EE} (max)	6.5	Vdc
Input Voltage	1, 16	V_{in}	1.0	Vrms
Junction Temperature	—	T_J	+150	°C
Storage Temperature Range	—	T_{stg}	– 65 to +150	°C

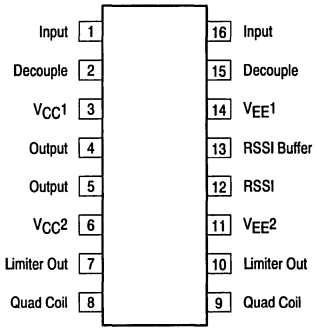
NOTE: Devices should not be operated at or outside these values. The "Recommended Operating Conditions" provide for actual device operation.

Simplified Block Diagram



NOTE: This device requires careful layout and decoupling to ensure stable operation.

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Temperature Range	Package
MC13155D	– 40° to + 85°C	SO-16

RECOMMENDED OPERATING CONDITIONS

Rating	Pin	Symbol	Value	Unit
Power Supply Voltage (T_A= 25°C) – 40°C ≤ T_A ≤ 85°C	11, 14 3, 6	V_{EE} V_{CC}	– 3.0 to – 6.0 Grounded	Vdc
Maximum Input Frequency	1, 16	f_{in}	300	MHz
Ambient Temperature Range	—	T_J	– 40 to + 85	°C

DC ELECTRICAL CHARACTERISTICS (T_A = 25°C, no input signal.)

Characteristic	Pin	Symbol	Min	Typ	Max	Unit
Drain Current (V_{EE} = – 5.0 Vdc) (V_{EE} = – 5.0 Vdc)	11 14 14	I_{11} I_{14} I_{14}	2.0 3.0 3.0	2.8 4.3 4.3	4.0 6.0 6.0	mA
Drain Current Total (see Figure 3) (V_{EE} = – 5.0 Vdc) (V_{EE} = – 6.0 Vdc) (V_{EE} = – 3.0 Vdc)	11, 14	I_{Total}	5.0 5.0 5.0 4.7	7.1 7.5 7.5 6.6	10 10.5 10.5 9.5	mA

AC ELECTRICAL CHARACTERISTICS (T_A = 25°C, f_{IF} = 70 MHz, V_{EE} = – 5.0 Vdc Figure 2, unless otherwise noted.)

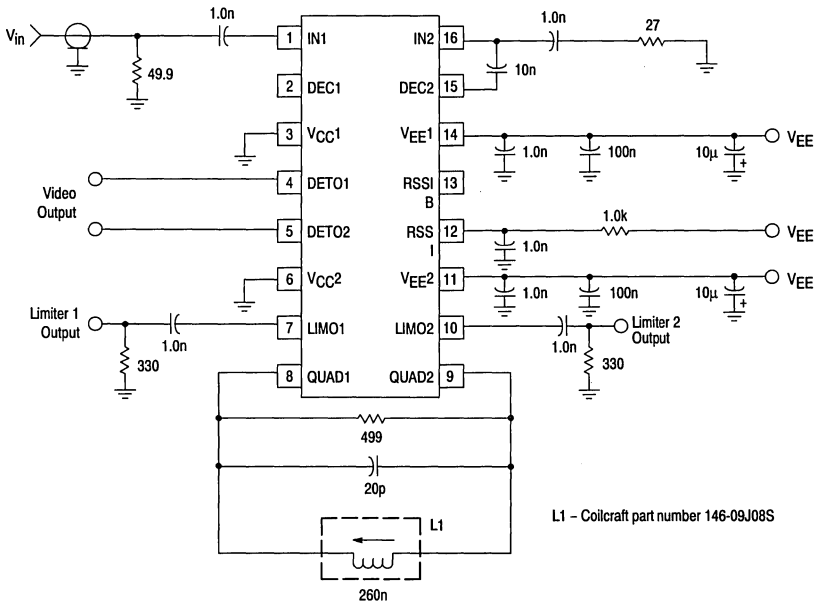
Characteristic	Pin	Min	Typ	Max	Unit
Input for - 3 dB Limiting Sensitivity	1, 16	—	1.0	2.0	mVrms
Differential Detector Output Voltage (V_{in} = 10 mVrms) (f_{dev} = ± 3.0 MHz) (V_{EE} = – 6.0 Vdc) (V_{EE} = – 5.0 Vdc) (V_{EE} = – 3.0 Vdc)	4, 5	 470 450 380	 590 570 500	 700 680 620	mV_{p-p}
Detector DC Offset Voltage	4, 5	– 250	—	250	mVdc
RSSI Slope	13	1.4	2.1	2.8	µA/dB
RSSI Dynamic Range	13	31	35	39	dB
RSSI Output (V_{in} = 100 µVrms) (V_{in} = 1.0 mVrms) (V_{in} = 10 mVrms) (V_{in} = 100 mVrms) (V_{in} = 500 mVrms)	12	 — — 16 — —	 2.1 2.4 24 65 75	 — — 36 — —	µA
RSSI Buffer Maximum Output Current (V_{in} = 10 mVrms)	13	—	2.3	—	mAdc
Differential Limiter Output (V_{in} = 1.0 mVrms) (V_{in} = 10 mVrms)	7, 10	100 —	140 180	— —	mVrms
Demodulator Video 3.0 dB Bandwidth	4, 5	—	12	—	MHz
Input Impedance (Figure 14) @ 70 MHz Rp (V_{EE} = – 5.0 Vdc) Cp (C_2=C_{15} = 100 p)	1, 16	 — —	 450 4.8	 — —	 Ω pF
Differential IF Power Gain	1, 7, 10, 16	—	46	—	dB

NOTE: Positive currents are out of the pins of the device.

CIRCUIT DESCRIPTION

The MC13155 consists of a wideband three-stage limiting amplifier, a wideband quadrature detector which may be operated up to 200 MHz, and a received signal strength indicator (RSSI) circuit which provides a current output linearly proportional to the IF input signal level for approximately 35 dB range of input level.

Figure 2. Test Circuit



APPLICATION INFORMATION

Evaluation PC Board

The evaluation PCB shown in Figures 19 and 20 is very versatile and is designed to cascade two ICs. The center section of the board provides an area for attaching all surface mount components to the circuit side and radial leaded components to the component ground side of the PCB (see Figures 17 and 18). Additionally, the peripheral area surrounding the RF core provides pads to add supporting and interface circuitry as a particular application dictates. This evaluation board will be discussed and referenced in this section.

Limiting Amplifier

Differential input and output ports interfacing the three stage limiting amplifier provide a differential power gain of typically 46 dB and useable frequency range of 300 MHz. The IF gain flatness may be controlled by decoupling of the internal feedback network at Pins 2 and 15.

Scattering parameter (S-parameter) characterization of the IF as a two port linear amplifier is useful to implement maximum stable power gain, input matching, and stability over a desired bandpass response and to ensure stable operation outside the bandpass as well. The MC13155 is unconditionally stable over most of its useful operating frequency range; however, it can be made unconditionally stable over its entire operating range with the proper decoupling of Pins 2 and 15. Relatively small decoupling capacitors of about 100 pF have a significant effect on the wideband response and stability. This is shown in the scattering parameter tables where S-parameters are shown for various values of C2 and C15 and at V_{EE} of – 3.0 and – 5.0 Vdc.

TYPICAL PERFORMANCE AT TEMPERATURE
(See Figure 2. Test Circuit)

Figure 3. Drain Current versus Supply Voltage

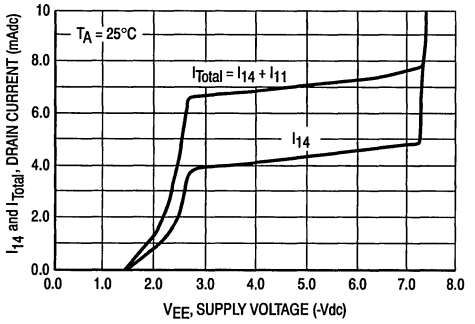


Figure 4. RSSI Output versus Frequency and Input Signal Level

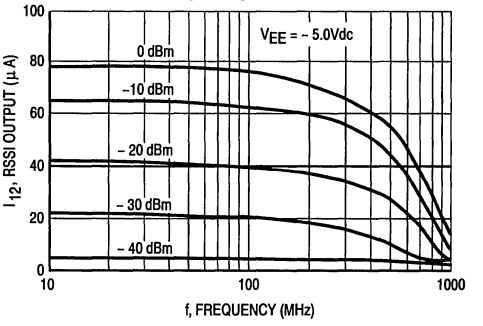


Figure 5. Total Drain Current versus Ambient Temperature and Supply Voltage

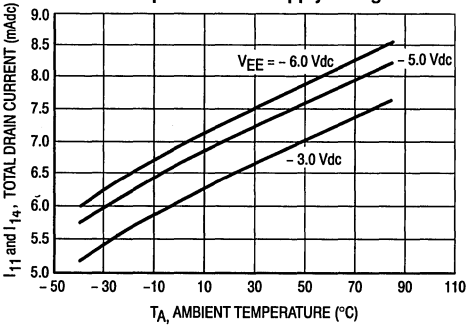


Figure 6. Detector Drain Current and Limiter Drain Current versus Ambient Temperature

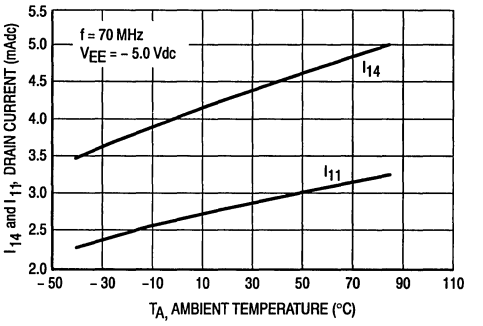


Figure 7. RSSI Output versus Ambient Temperature and Supply Voltage

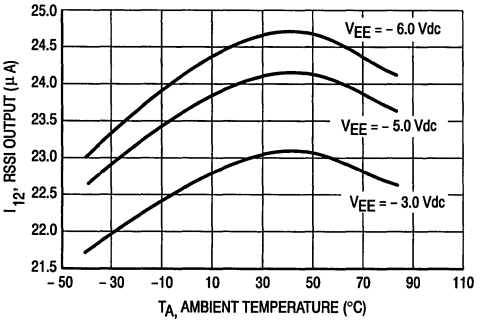


Figure 8. RSSI Output versus Input Signal Voltage
(V_{in} at Temperature)

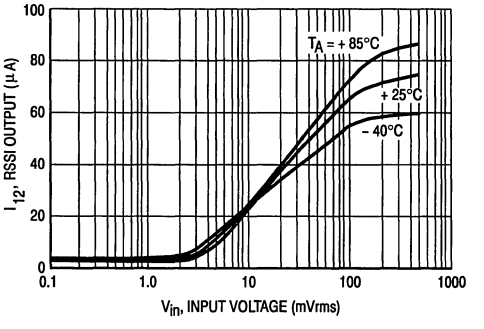


Figure 9. Differential Detector Output Voltage versus Ambient Temperature and Supply Voltage

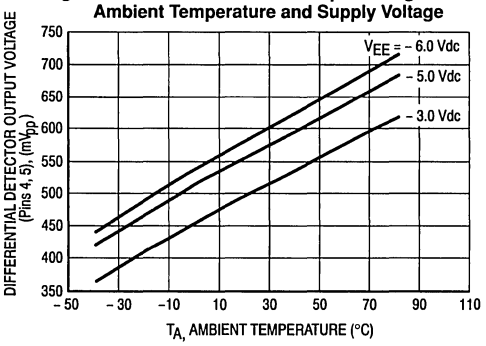


Figure 10. Differential Limiter Output Voltage versus Ambient Temperature (V_{in} = 1 and 10 mVrms)

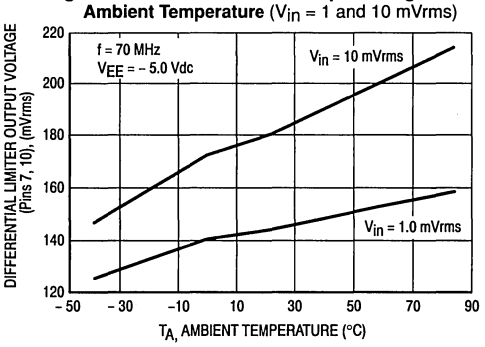


Figure 11A. Differential Detector Output Voltage versus Q of Quadrature LC Tank

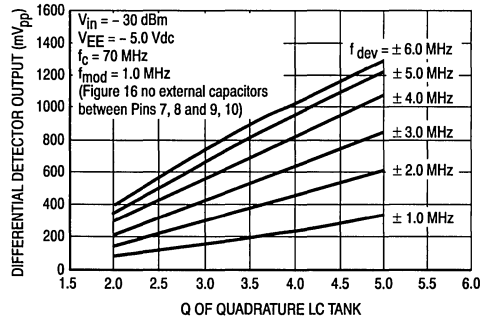


Figure 11B. Differential Detector Output Voltage versus Q of Quadrature LC Tank

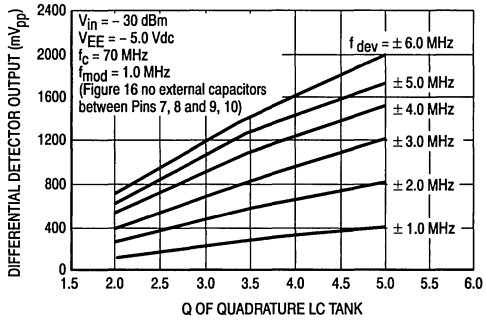


Figure 12. RSSI Output Voltage versus IF Input

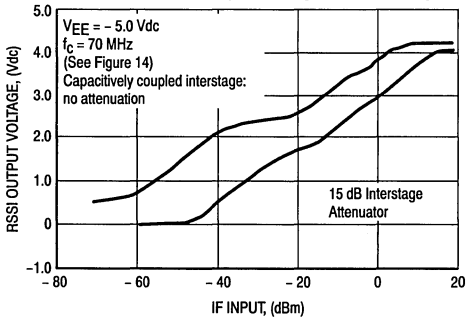
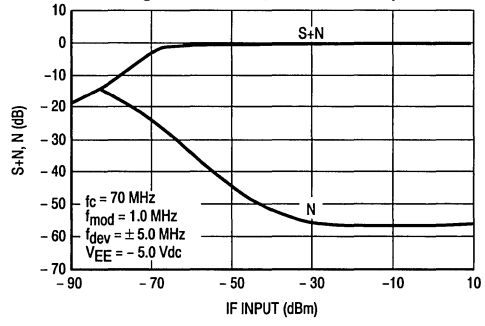


Figure 13. – S+N, N versus IF Input



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In the S-parameters measurements, the IF is treated as a two-port linear class A amplifier. The IF amplifier is measured with a single-ended input and output configuration in which the Pins 16 and 7 are terminated in the series combination of a 47 Ω resistor and a 10 nF capacitor to V_{CC} ground (see Figure 11– S-Parameter Test Circuit).

The S-parameters are in polar form as the magnitude (MAG) and angle (ANG). Also listed in the tables are the calculated values for the stability factor (K) and the Maximum Available Gain (MAG). These terms are related in the following equations:

$$K = (1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2) / (2 |S_{12} S_{21}|)$$

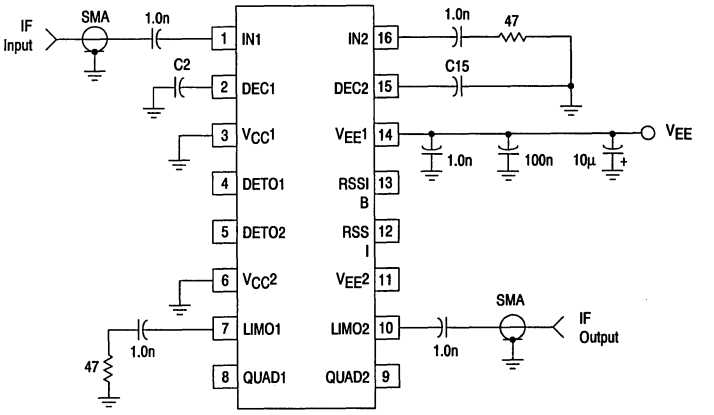
where: $|\Delta| = |S_{11} S_{22} - S_{12} S_{21}|$.

$$MAG = 10 \log |S_{21}| / |S_{12}| + 10 \log |K - (K^2 - 1)^{1/2}|$$

where: K > 1. The necessary and sufficient conditions for unconditional stability are given as K > 1:

$$B1 = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2 > 0$$

Figure 14. S-Parameter Test Circuit



S-Parameters (V_{EE} = – 5.0 Vdc, T_A = 25°C, C_2 and C_{15} = 0 pF)

Frequency	Input S11		Forward S21		Rev S12		Output S22		K	MAG
MHz	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG	MAG	dB
1.0	0.94	–13	8.2	143	0.001	7.0	0.87	– 22	2.2	32
2.0	0.78	– 23	23.5	109	0.001	– 40	0.64	– 31	4.2	33.5
5.0	0.48	1.0	39.2	51	0.001	– 97	0.34	–17	8.7	33.7
7.0	0.59	15	40.3	34	0.001	– 41	0.33	–13	10.6	34.6
10	0.75	17	40.9	19	0.001	– 82	0.41	–1.0	5.7	36.7
20	0.95	7.0	42.9	– 6.0	0.001	– 42	0.45	0	1.05	46.4
50	0.98	–10	42.2	– 48	0.001	– 9.0	0.52	– 3.0	0.29	—
70	0.95	–16	39.8	– 68	0.001	112	0.54	–16	1.05	46.4
100	0.93	– 23	44.2	– 93	0.001	80	0.53	– 22	0.76	—
150	0.91	– 34	39.5	–139	0.001	106	0.50	– 34	0.94	—
200	0.87	– 47	34.9	–179	0.002	77	0.42	– 44	0.97	—
500	0.89	–103	11.1	– 58	0.022	57	0.40	–117	0.75	—
700	0.61	–156	3.5	–164	0.03	0	0.52	179	2.6	13.7
900	0.56	162	1.2	92	0.048	- 44	0.47	112	4.7	4.5
1000	0.54	131	0.8	42	0.072	- 48	0.44	76	5.1	0.4

S-Parameters (V_{EE} = – 5.0 Vdc, T_A = 25°C, C_2 and C_{15} = 100 pF)

Frequency	Input S11		Forward S21		Rev S12		Output S22		K	MAG
MHz	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG	MAG	dB
1.0	0.98	–15	11.7	174	0.001	–14	0.84	– 27	1.2	37.4
2.0	0.50	– 2.0	39.2	85.5	0.001	–108	0.62	– 35	6.0	35.5
5.0	0.87	8.0	39.9	19	0.001	100	0.47	– 9.0	4.2	39.2
7.0	0.90	5.0	40.4	9.0	0.001	– 40	0.45	– 8.0	3.1	40.3
10	0.92	3.0	41	1.0	0.001	– 40	0.44	– 5.0	2.4	41.8
20	0.92	– 2.0	42.4	–14	0.001	– 87	0.49	– 6.0	2.4	41.9
50	0.91	– 8.0	41.2	– 45	0.001	85	0.50	– 5.0	2.3	42
70	0.91	–11	39.1	– 63	0.001	76	0.52	– 4.0	2.2	41.6
100	0.91	–15	43.4	– 84	0.001	85	0.50	–11	1.3	43.6
150	0.90	– 22	38.2	–126	0.001	96	0.43	– 22	1.4	41.8
200	0.86	– 33	35.5	–160	0.002	78	0.43	– 21	1.3	39.4
500	0.80	– 66	8.3	– 9.0	0.012	75	0.57	– 63	1.7	23.5
700	0.62	– 96	2.9	– 95	0.013	50	0.49	–111	6.3	12.5
900	0.56	–120	1.0	–171	0.020	53	0.44	–150	13.3	2.8
1000	0.54	–136	0.69	154	0.034	65	0.44	–179	12.5	– 0.8

S-Parameters (V_{EE} = – 5.0 Vdc, T_A = 25°C, C_2 and C_{15} = 680 pF)

Frequency	Input S11		Forward S21		Rev S12		Output S22		K	MAG
MHz	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG	MAG	dB
1.0	0.74	4.0	53.6	110	0.001	101	0.97	– 35	0.58	—
2.0	0.90	3.0	70.8	55	0.001	60	0.68	– 34	1.4	45.6
5.0	0.91	0	87.1	21	0.001	–121	0.33	– 60	1.1	49
7.0	0.91	0	90.3	11	0.001	–18	0.25	– 67	1.2	48.4
10	0.91	– 2.0	92.4	2.0	0.001	33	0.14	– 67	1.5	47.5
20	0.91	– 4.0	95.5	–16	0.001	63	0.12	–15	1.3	48.2
50	0.90	– 8.0	89.7	– 50	0.001	– 43	0.24	26	1.8	46.5
70	0.90	–10	82.6	–70	0.001	92	0.33	21	1.4	47.4
100	0.91	–14	77.12	–93	0.001	23	0.42	–1.0	1.05	49
150	0.94	– 20	62.0	–122	0.001	96	0.42	– 22	0.54	—
200	0.95	– 33	56.9	–148	0.003	146	0.33	– 62	0.75	—
500	0.82	– 63	12.3	–12	0.007	79	0.44	– 67	1.8	26.9
700	0.66	– 98	3.8	–107	0.014	84	0.40	–115	4.8	14.6
900	0.56	–122	1.3	177	0.028	78	0.39	–166	8.0	4.7
1000	0.54	–139	0.87	141	0.048	76	0.41	165	7.4	0.96

S-Parameters (V_{EE} = – 3.0 Vdc, T_A = 25°C, C_2 and C_{15} = 0 pF)

Frequency	Input S11		Forward S21		Rev S12		Output S22		K	MAG
MHz	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG	MAG	dB
1.0	0.89	–14	9.3	136	0.001	2.0	0.84	– 27	3.2	30.7
2.0	0.76	– 22	24.2	105	0.001	– 90	0.67	– 37	3.5	34.3
5.0	0.52	5.0	35.7	46	0.001	– 32	0.40	–13	10.6	33.3
7.0	0.59	12	38.1	34	0.001	– 41	0.40	–10	9.1	34.6
10	0.78	15	37.2	16	0.001	– 92	0.40	–1.0	5.7	36.3
20	0.95	5.0	38.2	– 9.0	0.001	47	0.51	– 4.0	0.94	—
50	0.96	–11	39.1	– 50	0.001	–103	0.48	– 6.0	1.4	43.7
70	0.93	–17	36.8	– 71	0.001	– 76	0.52	–13	2.2	41.4
100	0.91	– 25	34.7	– 99	0.001	–152	0.51	–19	3.0	39.0
150	0.86	– 37	33.8	–143	0.001	53	0.49	– 34	1.7	39.1
200	0.81	– 49	27.8	86	0.003	76	0.55	– 56	2.4	35.1
500	0.70	– 93	6.2	– 41	0.015	93	0.40	–110	2.4	19.5
700	0.62	–144	1.9	–133	0.049	56	0.40	–150	3.0	8.25
900	0.39	–176	0.72	125	0.11	–18	0.25	163	5.1	–1.9
1000	0.44	166	0.49	80	0.10	– 52	0.33	127	7.5	– 4.8

S-Parameters (V_{EE} = - 3.0 Vdc, T_A = 25°C, C_2 and C_{15} = 100 pF)

Frequency	Input S11		Forward S21		Rev S12		Output S22		K	MAG
MHz	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG	MAG	dB
1.0	0.97	–15	11.7	171	0.001	– 4.0	0.84	– 27	1.4	36.8
2.0	0.53	2.0	37.1	80	0.001	– 91	0.57	– 31	6.0	34.8
5.0	0.88	7.0	37.7	18	0.001	– 9.0	0.48	– 7.0	3.4	39.7
7.0	0.90	5.0	37.7	8.0	0.001	–11	0.49	– 7.0	2.3	41
10	0.92	2.0	38.3	1.0	0.001	– 59	0.51	– 9.0	2.0	41.8
20	0.92	– 2.0	39.6	–15	0.001	29	0.48	– 3.0	1.9	42.5
50	0.91	– 8.0	38.5	– 46	0.001	– 21	0.51	– 7.0	2.3	41.4
70	0.91	–11	36.1	– 64	0.001	49	0.50	– 8.0	2.3	40.8
100	0.91	–15	39.6	– 85	0.001	114	0.52	–13	1.7	37.8
150	0.89	– 22	34.4	–128	0.001	120	0.48	– 23	1.6	40.1
200	0.86	– 33	32	–163	0.002	86	0.40	– 26	1.7	37.8
500	0.78	– 64	7.6	–12	0.013	94	0.46	– 71	1.9	22.1
700	0.64	– 98	2.3	–102	0.027	58	0.42	–109	4.1	10.1
900	0.54	–122	0.78	179	0.040	38.6	0.35	–147	10.0	– 0.14
1000	0.53	–136	0.47	144	0.043	23	0.38	–171	15.4	– 4.52

S-Parameters (V_{EE} = – 3.0 Vdc, T_A = 25°C, C_2 and C_{15} = 680 pF)

Frequency	Input S11		Forward S21		Rev S12		Output S22		K	MAG
MHz	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG	MAG	dB
1.0	0.81	3.0	37	101	0.001	–19	0.90	– 32	1.1	43.5
2.0	0.90	2.0	47.8	52.7	0.001	– 82	0.66	– 39	0.72	—
5.0	0.91	0	58.9	20	0.001	104	0.37	– 56	2.3	44
7.0	0.90	–1	60.3	11	0.001	– 76	0.26	– 55	2.04	44
10	0.91	– 2.0	61.8	3.0	0.001	105	0.18	– 52	2.2	43.9
20	0.91	– 4.0	63.8	– 15	0.001	59	0.11	–13	2.0	44.1
50	0.90	– 8.0	60.0	– 48	0.001	96	0.22	33	2.3	43.7
70	0.90	–11	56.5	– 67	0.001	113	0.29	15	2.3	43.2
100	0.91	–14	52.7	– 91	0.001	177	0.36	5.0	2.0	43
150	0.93	– 21	44.5	–126	0.001	155	0.35	–17	1.8	42.7
200	0.90	– 43	41.2	–162	0.003	144	0.17	– 31	1.6	34.1
500	0.79	– 65	7.3	–13	0.008	80	0.44	– 75	3.0	22
700	0.65	– 97	2.3	–107	0.016	86	0.38	–124	7.1	10.2
900	0.56	–122	0.80	174	0.031	73	0.38	–174	12	0.37
1000	0.55	–139	0.52	137	0.50	71	0.41	157	11.3	– 3.4

8

DC Biasing Considerations

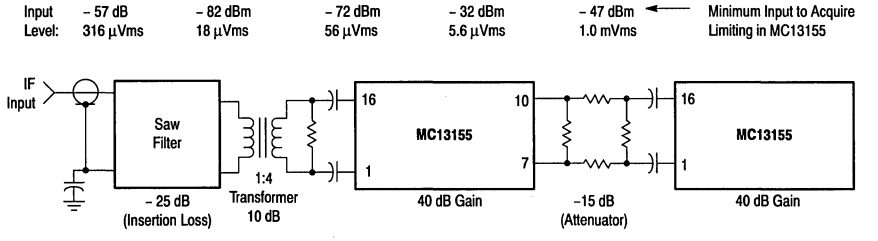
The DC biasing scheme utilizes two V_{CC} connections (Pins 3 and 6) and two V_{EE} connections (Pins 14 and 11). $V_{EE}1$ (Pin 14) is connected internally to the IF and RSSI circuits' negative supply bus while $V_{EE}2$ (Pin 11) is connected internally to the quadrature detector's negative bus. Under positive ground operation, this unique configuration offers the ability to bias the RSSI and IF separately from the quadrature detector. When two ICs are cascaded as shown in the 70 MHz application circuit and provided by the PCB (see Figures 17 and 18), the first MC13155 is used without biasing its quadrature detector, thereby saving approximately 3.0 mA. A total current of 7.0 mA is used to fully bias each IC, thus the total current in the application circuit is approximately 11 mA. Both V_{CC} pins are biased by the same supply. $V_{CC}1$ (Pin 3) is connected internally to the positive bus of the first half of the IF limiting amplifier, while $V_{CC}2$ is internally connected to the positive bus of the RSSI, the quadrature detector circuit, and the second half of the IF limiting amplifier (see Figure 15). This distribution of the V_{CC} enhances the stability of the IC.

RSSI Circuitry

The RSSI circuitry provides typically 35 dB of linear dynamic range and its output voltage swing is adjusted by selection of the resistor from pin 12 to V_{EE}. The RSSI slope is typically 2.1 μA/dB ; thus, for a dynamic range of 35 dB, the current output is approximately 74 μA. A 47 k resistor will yield a RSSI output voltage swing of 3.5 Vdc. The RSSI buffer output at Pin 13 is an emitter-follower and needs an external emitter resistor of 10 k to V_{EE}.

In a cascaded configuration (see circuit application in Figure 16), only one of the RSSI Buffer outputs (Pin 13) is used; the RSSI outputs (Pin 12 of each IC) are tied together and the one closest to the V_{EE} supply trace is decoupled to V_{CC} ground. The two pins are connected to V_{EE} through a 47 k resistor. This resistor sources a RSSI current which is proportional to the signal level at the IF input; typically, 1.0 mVrms (– 47 dBm) is required to place the MC13155 into limiting. The measured RSSI output voltage response of the application circuit is shown in Figure 12. Since the RSSI current output is dependent upon the input signal level at the IF input, a careful accounting of filter losses, matching and other losses and gains must be made in the entire receiver system. In the block diagram of the application circuit shown below, an accounting of the signal levels at points throughout the system shows how the RSSI response in Figure 12 is justified.

Block Diagram of 70 MHz Video Receiver Application Circuit

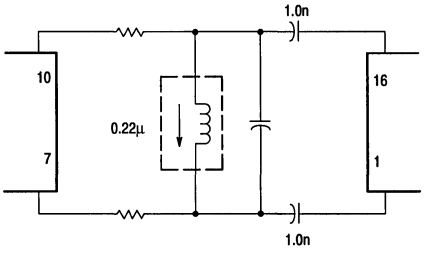


Cascading Stages

The limiting IF output is pinned-out differentially, cascading is easily achieved by AC coupling stage to stage. In the evaluation PCB, AC coupling is shown, however, interstage filtering may be desirable in some applications. In which case, the S-parameters provide a means to implement a low loss interstage match and better receiver sensitivity.

Where a linear response of the RSSI output is desired when cascading the ICs, it is necessary to provide at least 10 dB of interstage loss. Figure 12 shows the RSSI response with and without interstage loss. A 15 dB resistive attenuator is an inexpensive way to linearize the RSSI response. This has its drawbacks since it is a wideband noise source that is dependent upon the source and load impedance and the amount of attenuation that it provides. A better, although more costly, solution would be a bandpass filter designed to the desired center frequency and bandpass response while carefully selecting the insertion loss. A network topology shown below may be used to provide a bandpass response with the desired insertion loss.

Network Topology



Quadrature Detector

The quadrature detector is coupled to the IF with internal 2.0 pF capacitors between Pins 7 and 8 and Pins 9 and 10. For wideband data applications, such as FM video and satellite receivers, the drive to the detector can be increased with additional external capacitors between these pins, thus, the recovered video signal level output is increased for a given bandwidth (see Figure 11A and Figure 11B).

The wideband performance of the detector is controlled by the loaded Q of the LC tank circuit. The following equation defines the components which set the detector circuit's bandwidth:

$$Q = R_T/X_L \quad (1)$$

where: R_T is the equivalent shunt resistance across the LC Tank and X_L is the reactance of the quadrature inductor at the IF frequency ($X_L = 2\pi fL$).

The inductor and capacitor are chosen to form a resonant LC Tank with the PCB and parasitic device capacitance at the desired IF center frequency as predicted by:

$$fc = (2\pi \sqrt{(LC_p)})^{-1} \quad (2)$$

where: L is the parallel tank inductor and C_p is the equivalent parallel capacitance of the parallel resonant tank circuit.

The following is a design example for a wideband detector at 70 MHz and a loaded Q of 5. The loaded Q of the quadrature detector is chosen somewhat less than the Q of the IF bandpass. For an IF frequency of 70 MHz and an IF bandpass of 10.9 MHz, the IF bandpass Q is approximately 6.4.

Example:

Let the external Cext = 20 pF. (The minimum value here should be greater than 15 pF making it greater than the internal device and PCB parasitic capacitance, Cint ≈ 3.0 pF).

$$C_p = Cint + Cext = 23\ pF$$

Rewrite Equation 2 and solve for L:

$L = (0.159)^2/(C_p\ fc^2)$

L = 198 nH, thus, a standard value is chosen.

L = 0.22 μH (tunable shielded inductor).

The value of the total damping resistor to obtain the required loaded Q of 5 can be calculated by rearranging Equation 1:

$$R_T = Q(2\pi fL)$$

$R_T = 5\ (2\pi)(70)(0.22) = 483.8\ \Omega$.

The internal resistance, Rint between the quadrature tank Pins 8 and 9 is approximately 3200 Ω and is considered in determining the external resistance, Rext which is calculated from:

$Rext = ((R_T)(Rint))/(Rint - R_T)$

Rext = 570, thus, choose the standard value.

Rext =560 Ω.

SAW Filter

In wideband video data applications, the IF occupied bandwidth may be several MHz wide. A good rule of thumb is to choose the IF frequency about 10 or more times greater than the IF occupied bandwidth. The IF bandpass filter is a SAW filter in video data applications where a very selective response is needed (i.e., very sharp bandpass response). The evaluation PCB is laid out to accommodate two SAW filter package types: 1) A five-leaded plastic SIP package. Recommended part numbers are Siemens X6950M which operates at 70 MHz; 10.4 MHz 3 dB passband, X6951M (X252.8) which operates at 70 MHz; 9.2 MHz 3 dB passband; and X6958M which operates at 70 MHz, 6.3 MHz 3 dB passband, and 2) A four-leaded TO-39 metal can package. Typical insertion loss in a wide bandpass SAW filter is 25 dB.

The above SAW filters require source and load impedances of 50 Ω to assure stable operation. On the PC board layout, space is provided to add a matching network, such as a 1:4 surface mount transformer between the SAW filter output and the input to the MC13155. A 1:4 transformer, made by Coilcraft and Mini Circuits, provides a suitable interface (see Figures 16, 17 and 18). In the circuit and layout, the SAW filter and the MC13155 are differentially configured with interconnect traces which are equal in length and symmetrical. This balanced feed enhances RF stability, phase linearity, and noise performance.

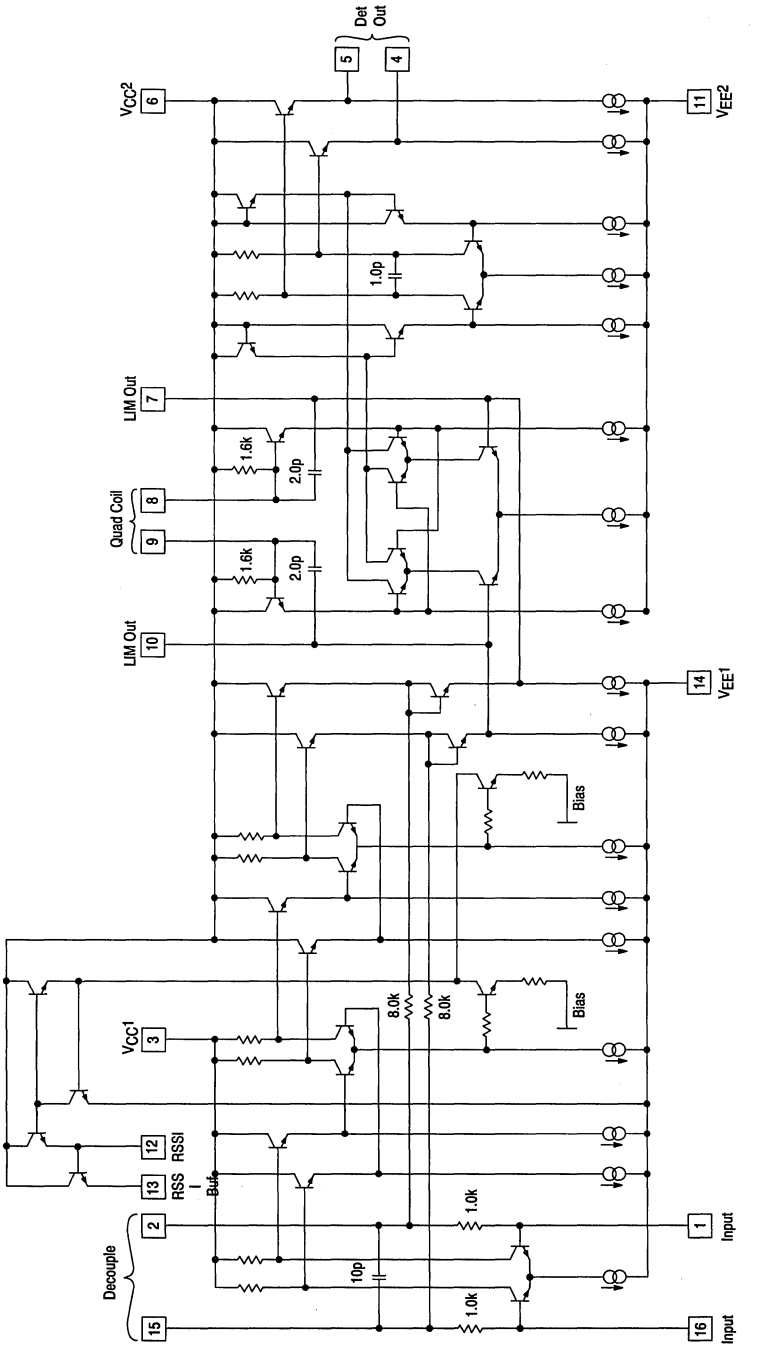


Figure 15. Simplified Internal Circuit Schematic

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Figure 16. 70 MHz Video Receiver Application Circuit

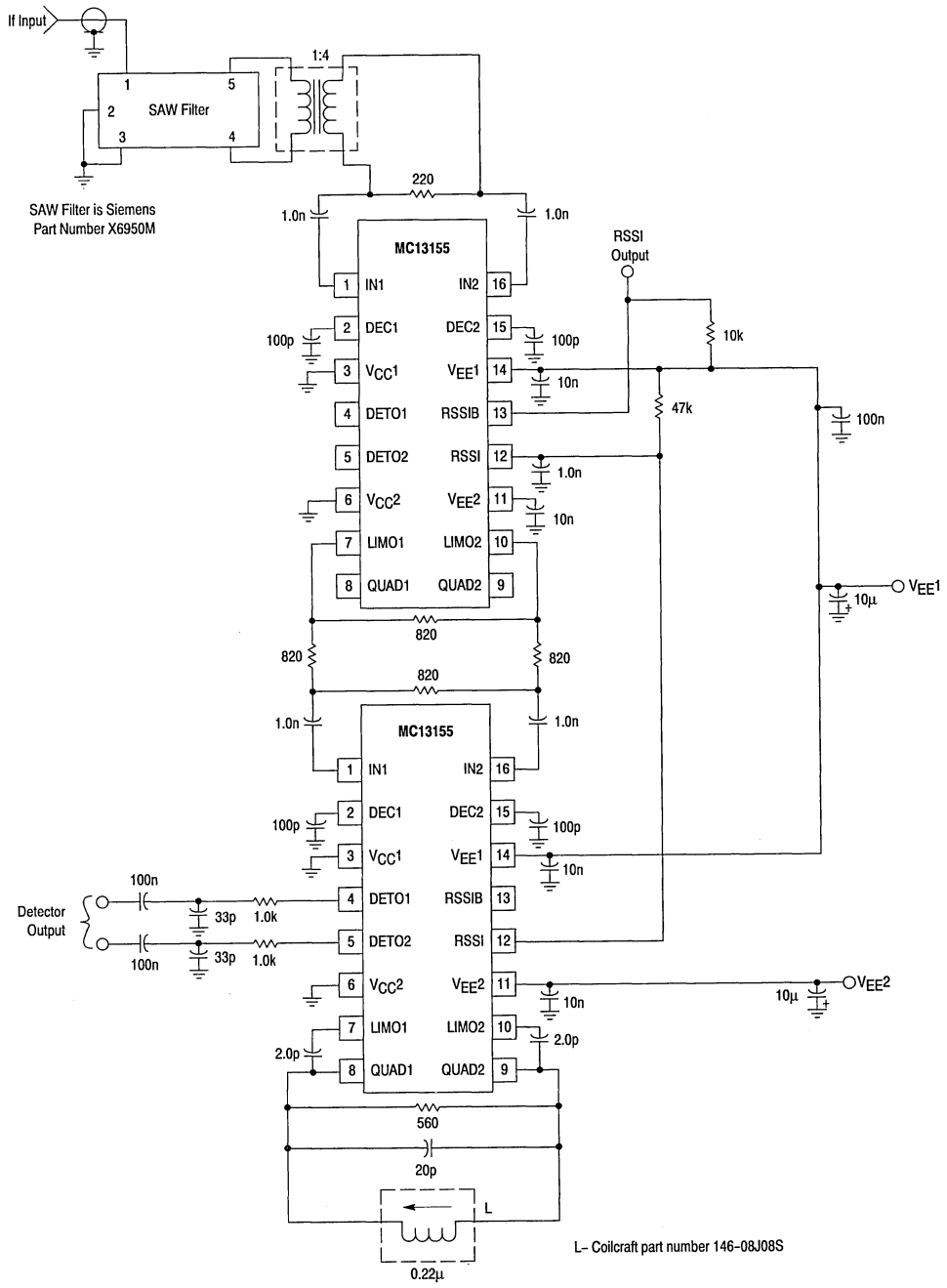

Figure 17. Component Placement (Circuit Side)

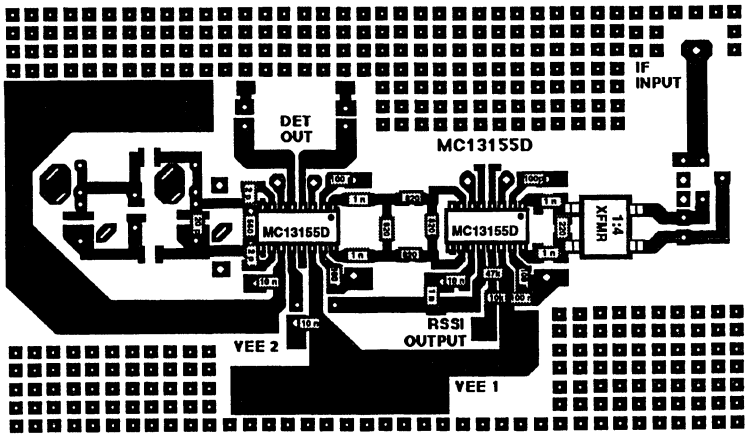

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Figure 18. Component Placement (Ground Side)

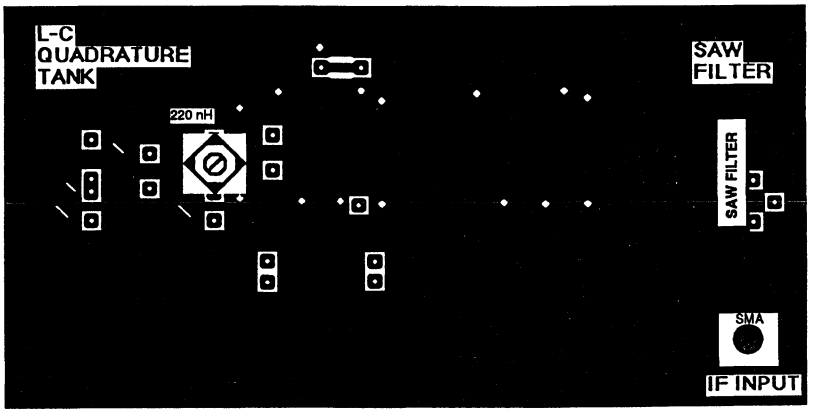

Figure 19. Circuit Side View

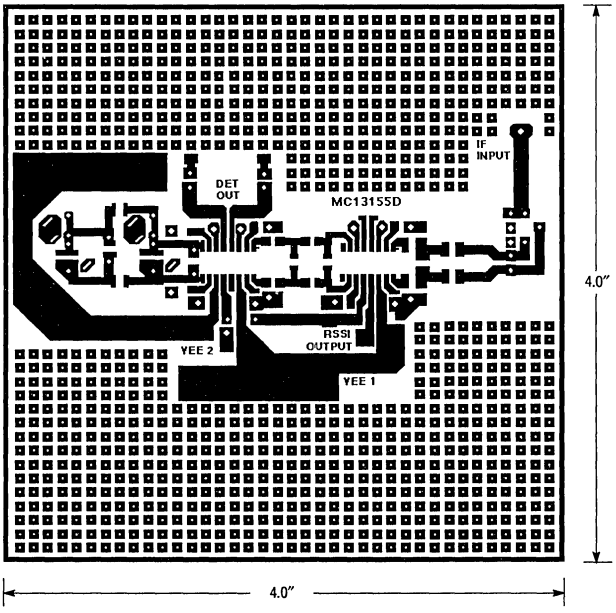

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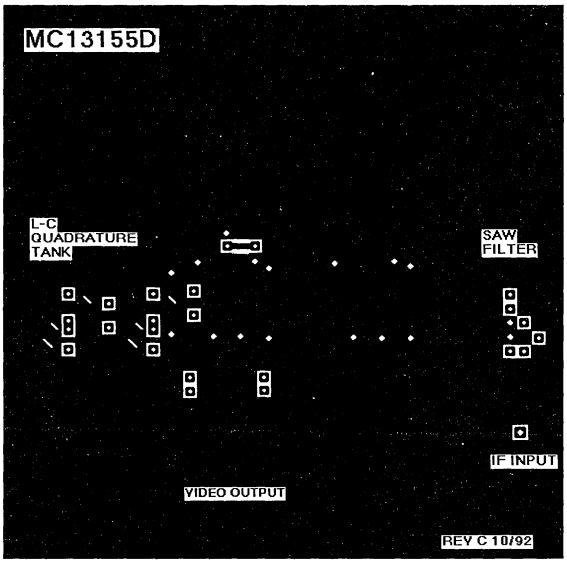
Figure 20. Ground Side View



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC13156

Product Preview

Wideband FM IF System

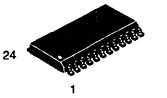
WIDEBAND FM IF SYSTEM for DIGITAL and ANALOG APPLICATIONS

SILICON MONOLITHIC INTEGRATED CIRCUIT

The MC13156 is a wideband FM IF subsystem targeted at high performance data and analog applications. Excellent high frequency performance is achieved, with low cost, through use of Motorola's MOSAIC 1.5™ RF bipolar process. The MC13156 has an onboard Colpitts VCO for PLL controlled multichannel operation. The mixer is useful to beyond 200 MHz and may be used in a differential, balanced, or single-ended configuration. The IF amplifier is split to accommodate two low cost cascaded filters. RSSI output is derived by summing the output of both IF sections. A precision data shaper has a hold function to preset the shaper for fast recovery of new data.

Applications for the MC13156 include CT–2, wideband data links, and other radio systems utilizing GMSK, FSK or FM modulation.

- 3.0 to 6.0 Vdc Operation
- Typical Sensitivity at 200 MHz of 6.0 μV for 12 dB SINAD
- RSSI Range of >70 dB
- High Performance Data Shaper for Enhanced CT-2 Operation
- Internal 330 Ω Termination for 10.7 MHz Filters
- Split IF for Improved Filtering and Extended RSSI Range
- 3rd Order Intercept (Input) Target of –10 dBm



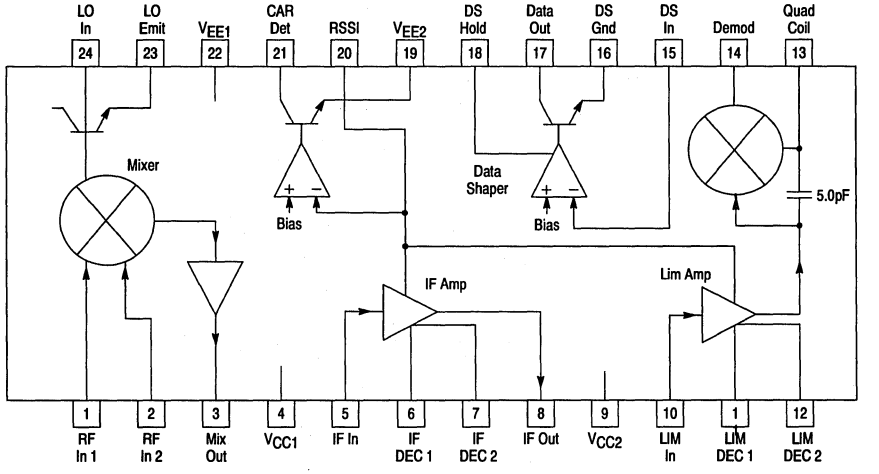
DW SUFFIX
PLASTIC PACKAGE
CASE 751E
(SO-24L)

ORDERING INFORMATION

Device	Temperature Range	Package
MC13156DW	– 40° to + 85°C	SO-24L

8

Pin Connections and Block Diagram



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC13173

Product Preview

Infrared Integrated Transceiver System

INFRARED INTEGRATED TRANSCEIVER SYSTEM

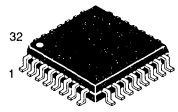
SILICON MONOLITHIC INTEGRATED CIRCUIT

The MC13173 is a low power integrated infrared (IR) transceiver system. It is a unique blend of a split IF wideband FM receiver and a specialized infrared LED transmitter. This device was designed to provide communications between portable computers via a half-duplex infrared link. It is capable of data rates over 40 kbps.

The receiver includes a mixer, IF amplifier and limiter, and data slicer. The IF amplifier is split to accommodate two low cost cascaded filters. The RSSI output is derived by summing the output of both IF sections.

The transmitter section includes a frequency synthesizer, FSK modulator, harmonic low-pass filter and an IR LED driver.

- Transmitter Operates in Two Modes:
  - On/Off Pulsing for Remote Control
  - FSK Modulation at 1.4 MHz for Data Communications
- Over 70 dB of RSSI Range
- Split IF for Improved Filtering and Extended RSSI Range
- Digitally Controlled Via a Six Line Interface Bus
- Individual Circuit Blocks can be Powered Down when not in Use for Power Conservation



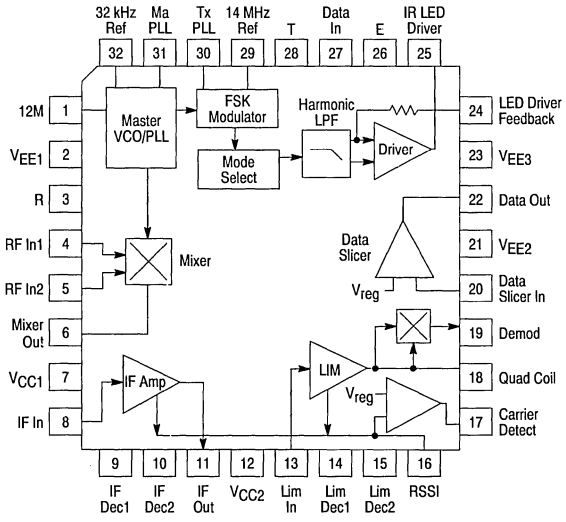
FU SUFFIX
PLASTIC QFP PACKAGE
CASE 873

ORDERING INFORMATION

Device	Temperature Range	Package
MC13173FU	– 40° to + 85°C	32 Pin QFP

8

MC13173 Pin Out/Simplified Block Diagram



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC13175
MC13176

Advance Information

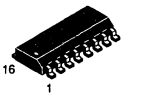
UHF FM/AM Transmitter

UHF FM/AM TRANSMITTER

SILICON MONOLITHIC INTEGRATED CIRCUIT

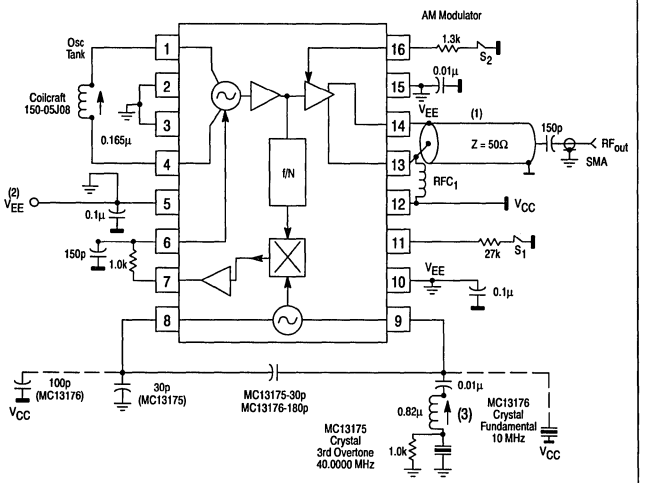
The MC13175 and MC13176 are one chip FM/AM transmitter subsystems designed for AM/FM communication systems. They include a Colpitts crystal reference oscillator, UHF oscillator, ÷ 8 (MC13175) or ÷ 32 (MC13176) prescaler and phase detector forming a versatile PLL system. Targeted applications are in the 260 to 470 MHz band and 902 to 928 MHz band covered by FCC Title 47; Part 15. Other applications include local oscillator sources in UHF and 900 MHz receivers, UHF and 900 MHz video transmitters, RF Local Area Networks (LANs), and high frequency clock drivers. The MC13175/76 offer the following features:

- UHF Current Controlled Oscillator
- Uses Easily Available 3rd Overtone or Fundamental Crystals for Reference
- Fewer External Parts Required
- Low Operating Supply Voltage (1.8 to 5.0 Vdc)
- Low Supply Drain Currents
- Power Output Adjustable (Up to +10 dBm)
- Differential Output for Loop Antenna or Balun Transformer Networks
- Power Down Feature
- ASK Modulated by Switching Output On and Off
- (MC13175) $f_o = 8 \times f_{ref}$; (MC13176) $f_o = 32 \times f_{ref}$



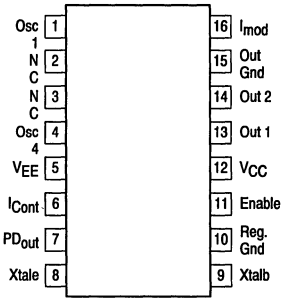
D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO-16)

Figure 1. Typical Application as 320 MHz AM Transmitter



NOTES: 1. 50 Ω coaxial balun, 1/10 wavelength at 320 MHz equals 1.5 inches.
2. Pins 5, 10 & 15 are ground and connected to V_{EE} which is the component/DC ground plane side of PCB. These pins must be decoupled to V_{CC}; decoupling capacitors should be placed as close as possible to the pins.
3. The crystal oscillator circuit may be adjusted for frequency with the variable inductor (MC13175); recommended source is Coilcraft "slot seven" 7mm tuneable inductor, Part #7M3-821. 1.0k resistor. Shunting the crystal prevents it from oscillating in the fundamental mode.

PIN CONNECTIONS



ORDERING INFORMATION

Device	Temperature Range	Package
MC13175D	– 40° to +85°C	SO-16
MC13176D		SO-16

8

MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted.)

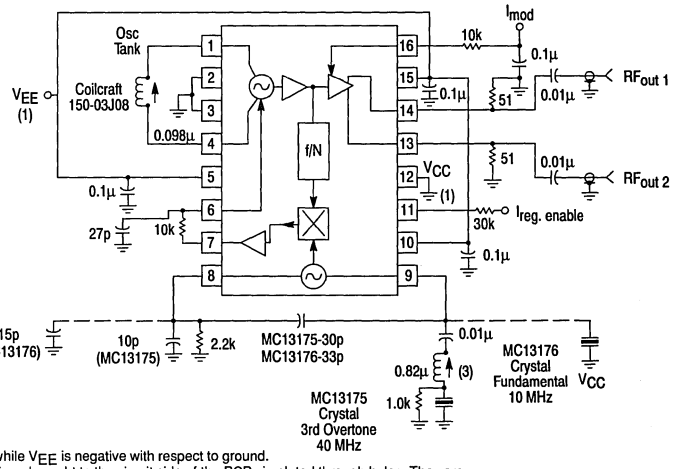
Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	7.0 (max)	Vdc
Operating Supply Voltage Range	V_{CC}	1.8 to 5.0	Vdc
Junction Temperature	T_J	+150	°C
Operating Ambient Temperature	T_A	– 40 to + 85	°C
Storage Temperature	T_{stg}	– 65 to +150	°C

ELECTRICAL CHARACTERISTICS (Figure 2; V_{EE} = – 3.0 Vdc, T_A = 25°C, unless otherwise noted.)*

Characteristic	Pin	Symbol	Min	Typ	Max	Unit
Supply Current (Power down: I_{11} & I_{16} = 0)	—	I_{EE1}	– 0.5	—	—	µA
Supply Current (Enable [Pin 11] to V_{CC} thru 30 k, I_{16} = 0)	—	I_{EE2}	–18	–14	—	mA
Total Supply Current (Transmit Mode) (I_{mod} = 2.0 mA; f_o = 320 MHz)	—	I_{EE3}	– 39	– 34	—	mA
Differential Output Power (f_o = 320 MHz; V_{ref} [Pin 9] = 500 mV_{p-p}; f_o = N x f_{ref}) I_{mod} = 2.0 mA (see Figure 7, 8) I_{mod} = 0 mA	13 & 14	P_{out}	 2.0 —	 + 4.7 – 45	 — —	dBm
Hold-in Range (± Δf_{ref} x N) MC13175 (see Figure 7) MC13176 (see Figure 8)	13 & 14	± Δf_H	 3.5 4.0	 6.5 8.0	 — —	MHz
Phase Detector Output Error Current MC13175 MC13176	7	I_{error}	 20 22	 25 27	 — —	µA
Oscillator Enable Time (see Figure 22b)	11, 8	t_{enable}	—	4.0	—	ms
Amplitude Modulation Bandwidth (see Figure 24)	16	BW_{AM}	—	25	—	MHz
Spurious Outputs (I_{mod} = 2.0 mA) Spurious Outputs (I_{mod} = 0 mA)	13 & 14 13 & 14	P_{son} P_{soff}	— —	– 50 – 50	— —	dBc
Maximum Divider Input Frequency Maximum Output Frequency	— 13 & 14	f_{div} f_o	— —	950 950	— —	MHz

* For testing purposes, V_{CC} is ground (see Figure 2).

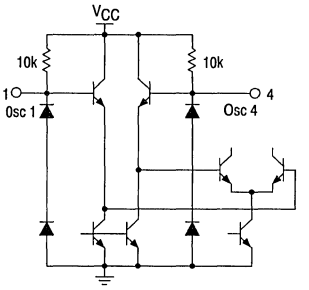
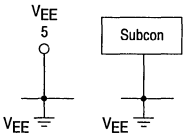
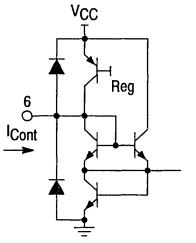
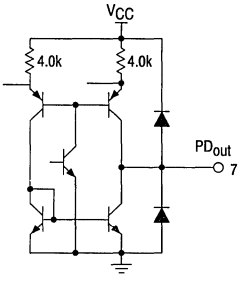
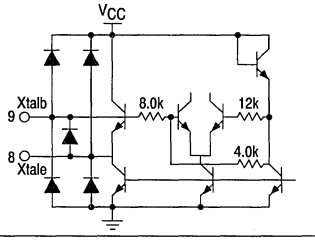
Figure 2. 320 MHz Test Circuit



NOTES: 1. V_{CC} is ground; while V_{EE} is negative with respect to ground.
2. Pins 5, 10 and 15 are brought to the circuit side of the PCB via plated through holes. They are connected together with a trace on the PCB and each Pin is decoupled to V_{CC} (ground).
3. Recommended source is Coilcraft "slot seven" inductor, part number 7M3-821.

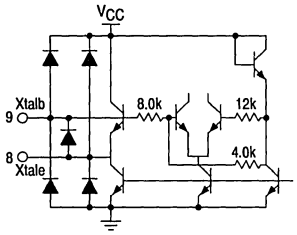
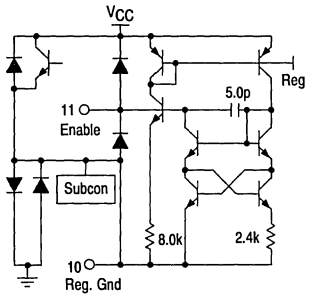
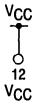
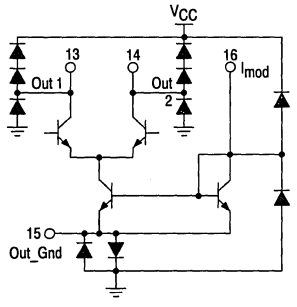
8

PIN DESCRIPTIONS

Pin	Symbol	Internal Equivalent Circuit	Description/External Circuit Requirements
1 & 4	Osc 1, Osc 4		**CCO Inputs** The oscillator is a current controlled type. An external oscillator coil is connected to Pins 1 and 4 which forms a parallel resonance LC tank circuit with the internal capacitance of the IC and with parasitic capacitance of the PC board. Three base-emitter capacitances in series configuration form the capacitance for the parallel tank. These are the base-emitters at Pins 1 and 4 and the base-emitter of the differential amplifier. The equivalent series capacitance in the differential amplifier is varied by the modulating current from the frequency control circuit (see Pin 6, internal circuit). A more thorough discussion is found in the Applications Information section.
5	V_{EE}		**Supply Ground (V_{EE})** In the PCB layout, the ground pins (also applies to Pins 10 and 15) should be connected directly to chassis ground. Decoupling capacitors to V_{CC} should be placed directly at the ground returns.
6	I_{Cont}		**Frequency Control** For V_{CC} = 3.0 Vdc, the voltage at Pin 6 is approximately 1.55 Vdc. The oscillator is current controlled by the error current from the phase detector. This current is amplified to drive the current source in the oscillator section which controls the frequency of the oscillator. Figures 9 and 10 show the Δf_{osc} versus I_{Cont}, Figure 5 shows the Δf_{osc} versus I_{Cont} at – 40°C, + 25°C and + 85°C for 320 MHz. The CCO may be FM modulated as shown in Figure 17, MC13176 320 MHz FM Transmitter. A detailed discussion is found in the Applications Information section.
7	PD_{out}		**Phase Detector Output** The phase detector provides ± 30 µA to keep the CCO locked at the desired carrier frequency. The output impedance of the phase detector is approximately 53 kΩ. Under closed loop conditions there is a DC voltage which is dependent upon the free running oscillator and the reference oscillator frequencies. The circuitry between Pins 7 and 6 should be selected for adequate loop filtering necessary to stabilize and filter the loop response. Low pass filtering between Pin 7 and 6 is needed so that the corner frequency is well below the sum of the divider and the reference oscillator frequencies, but high enough to allow for fast response to keep the loop locked. Refer to the Applications Information section regarding loop filtering and FM modulation.
8	Xtale		**Crystal Oscillator Inputs** The internal reference oscillator is configured as a common emitter Colpitts. It may be operated with either a fundamental or overtone crystal depending on the carrier frequency and the internal prescaler. Crystal oscillator circuits and specifications of crystals are discussed in detail in the applications section. With V_{CC} = 3.0 Vdc, the voltage at Pin 8 is approximately 1.8 Vdc and at Pin 9 is approximately 2.3 Vdc. 500 to 1000 mVp-p should be present at Pin 9. The Colpitts is biased at 200 µA; additional drive may be acquired by increasing the bias to approximately 500 µA. Use 6.2 k from Pin 8 to ground.

8

PIN DESCRIPTIONS

Pin	Symbol	Internal Equivalent Circuit	Description/External Circuit Requirements
9	Xtalb		**Crystal Oscillator Inputs** The internal reference oscillator is configured as a common emitter Colpitts. It may be operated with either a fundamental or overtone crystal depending on the carrier frequency and the internal prescaler. Crystal oscillator circuits and specifications of crystals are discussed in detail in the applications section. With V_{CC} = 3.0 Vdc, the voltage at Pin 8 is approximately 1.8 Vdc and at Pin 9 is approximately 2.3 Vdc. 500 to 1000 mVp-p should be present at Pin 9. The Colpitts is biased at 200 µA; additional drive may be acquired by increasing the bias to approximately 500 µA. Use 6.2 k from Pin 8 to ground.
10	Reg. Gnd		**Regulator Ground** An additional ground pin is provided to enhance the stability of the system. Decoupling to the V_{CC} (RF ground) is essential; it should be done at the ground return for Pin 10. **Device Enable** The potential at Pin 11 is approximately 1.25 Vdc. When Pin 11 is open, the transmitter is disabled in a power down mode and draws less than 1.0 µA I_{CC} if the MOD at Pin 16 is also open (i.e., it has no current driving it). To enable the transmitter a current source of 10 µA to 90 µA is provided. Figures 3 and 4 show the relationship between I_{CC}, V_{CC} and $I_{reg.\ enable}$. Note that I_{CC} is flat at approximately 10 mA for $I_{reg.\ enable}$ = 5.0 to 100 µA (I_{mod} = 0).
11	Enable		
12	V_{CC}		**Supply Voltage (V_{CC})** The operating supply voltage range is from 1.8 Vdc to 5.0 Vdc. In the PCB layout, the V_{CC} trace must be kept as wide as possible to minimize inductive reactances along the trace; it is best to have it completely fill around the surface mount components and traces on the circuit side of the PCB.
13 & 14	Out 1 and Out 2		**Differential Output** The output is configured differentially to easily drive a loop antenna. By using a transformer or balun, as shown in the application schematic, the device may then drive an unbalanced low impedance load. Figure 6 shows how much the Output Power and Free-Running Oscillator Frequency change with temperature at 3.0 Vdc; I_{mod} = 2.0 mA. **Output Ground** This additional ground pin provides direct access for the output ground to the circuit board V_{EE}. **AM Modulation/Power Output Level** The DC voltage at this pin is 0.8 Vdc with the current source active. An external resistor is chosen to provide a source current of 1.0 to 3.0 mA, depending on the desired output power level at a given V_{CC}. Figure 23 shows the relationship of Power Output to Modulation Current, I_{mod}. At V_{CC} = 3.0 Vdc, 3.5 dBm power output can be acquired with about 35 mA I_{CC}. For FM modulation, Pin 16 is used to set the desired output power level as described above. For AM modulation, the modulation signal must ride on a positive DC bias offset which sets a static (modulation off) modulation current. External circuitry for various schemes is further discussed in the Applications Information section.
15	Out_Gnd		
16	I_{mod}		

8

Figure 3. Supply Current versus Supply Voltage

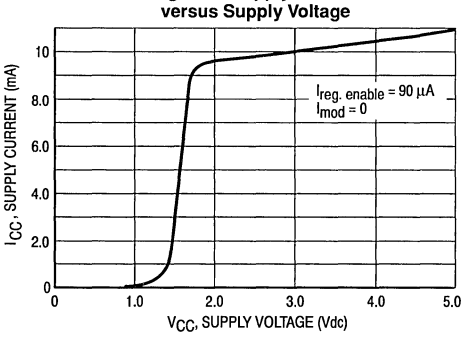


Figure 4. Supply Current versus Regulator Enable Current

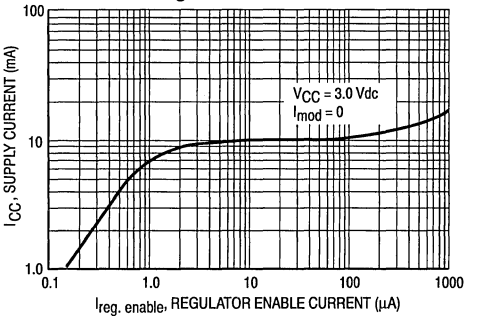


Figure 5. Change Oscillator Frequency versus Oscillator Control Current

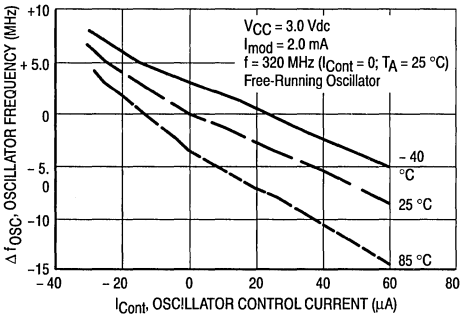


Figure 6. Change in Oscillator Frequency and Output Power versus Ambient Temperature

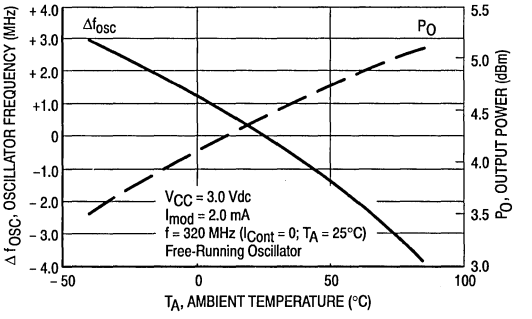


Figure 7. MC13175 Reference Oscillator Frequency versus Phase Detector Current

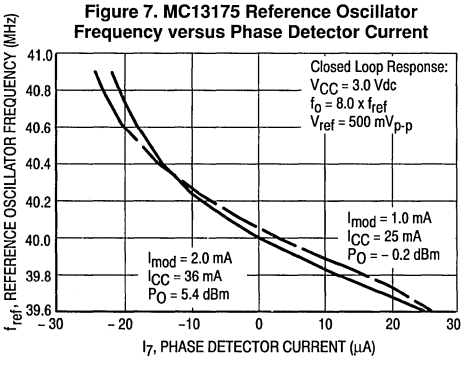


Figure 8. MC13176 Reference Oscillator Frequency versus Phase Detector Current

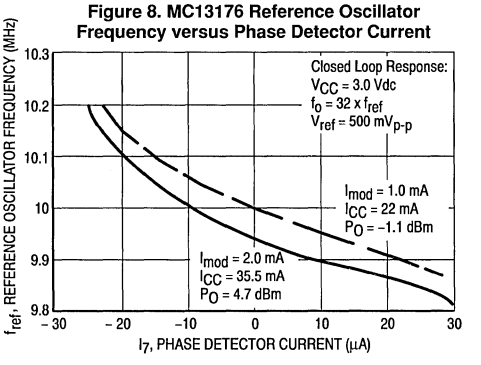


Figure 9. Change in Oscillator Frequency versus Oscillator Control Current

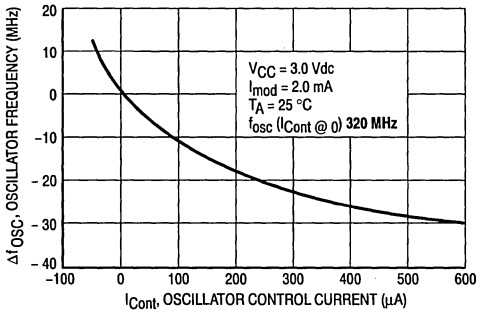
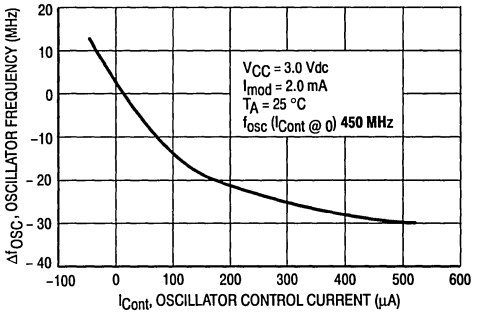


Figure 10. Change in Oscillator Frequency versus Oscillator Control Current



APPLICATIONS INFORMATION

Evaluation PC Board

The evaluation PCB, shown in Figures 26 and 27, is very versatile and is intended to be used across the entire useful frequency range of this device. The center section of the board provides an area for attaching all SMT components to the circuit side and radial leaded components to the component ground side of the PCB (see Figures 28 and 29). Additionally, the peripheral area surrounding the RF core provides pads to add supporting and interface circuitry as a particular application dictates. This evaluation board will be discussed and referenced in this section.

Current Controlled Oscillator (Pins 1 to 4)

It is critical to keep the interconnect leads from the CCO (Pins 1 and 4) to the external inductor symmetrical and equal in length. With a minimum inductor the maximum free running frequency is greater than 1.0 GHz. Since this inductor will be small, it may be either a microstrip inductor, an air wound inductor or a tuneable RF coil. An air wound inductor may be tuned by spreading the windings, whereas, tuneable RF coils are tuned by adjusting the position of an aluminum core in a threaded coilform. As the aluminum core coupling to the windings is increased, the inductance is decreased. The temperature coefficient using an aluminum core is better than a ferrite core. The UniCoil™ inductors made by Coilcraft may be obtained with aluminum cores (Part No. 51-129-169).

Ground (Pins 5, 10 and 15)

Ground Returns: It is best to take the grounds to a backside ground plane via plated through holes or eyelets at the pins. The application PCB layout implements this technique. Note that the grounds are located at or less than 100 mils from the devices pins.

Decoupling: Decoupling each ground pin to V_{CC} isolates each section of the device by reducing interaction between sections and by localizing circulating currents.

Loop Characteristics (Pins 6 and 7)

Figure 11 is the component block diagram of the MC1317XD PLL system where the loop characteristics are described by the gain constants. Access to individual components of this PLL system is limited, inasmuch as the loop is only pinned out at the phase detector output and the frequency control input for the CCO. However, this allows for characterization of the gain constants of these loop components. The gain constants K_p, K_o and K_n are well defined in the MC13175 and MC13176.

Phase Detector (Pin 7)

With the loop in lock, the difference frequency output of the phase detector is DC voltage that is a function of the phase difference. The sinusoidal type detector used in this IC has the following transfer characteristic:

$$I_e = A \sin \theta_e$$

The gain factor of the phase detector, K_p (with the loop in lock) is specified as the ratio of DC output current, I_e to phase error, θ_e:

$K_p = I_e/\theta_e$ (Amps/radians)
$K_p = A \sin \theta_e/\theta_e$
$\sin \theta_e \sim \theta_e$ for $\theta_e \leq 0.2$ radians;
thus, $K_p = A$ (Amps/radians)

Figures 7 and 8 show that the detector DC current is approximately 30 μA where the loop loses lock at $\theta_e = \pm \pi/2$ radians; therefore, K_p is 30 μA/radians.

Current Controlled Oscillator, CCO (Pin 6)

Figures 9 and 10 show the non-linear change in frequency of the oscillator over an extended range of control current for 320 and 450 MHz applications. K_o ranges from approximately 6.3×10^5 rad/sec/μA or 100 kHz/μA (Figure 9) to 8.8×10^5 rad/sec/μA or 140 kHz/μA (Figure 10) over a relatively linear response of control current (0 to 100 μA). The oscillator gain factor depends on the operating range of the control current (i.e., the slope is not constant). Included in the CCO gain factor is the internal amplifier which can sink and source at least 30 μA of input current from the phase detector. The internal circuitry at Pin 6 limits the CCO control current to 50 μA of source capability while its sink capability exceeds 200 μA as shown in Figures 9 and 10. Further information to follow shows how to use the full capabilities of the CCO by addition of an external loop amplifier and filter (see Figure 15). This additional circuitry yields at $K_o = 0.145$ MHz/μA or 9.1×10^5 rad/sec/μA.

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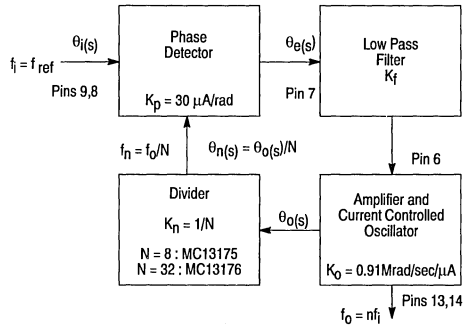
Figure 11. Block Diagram of MC1317XD PLL



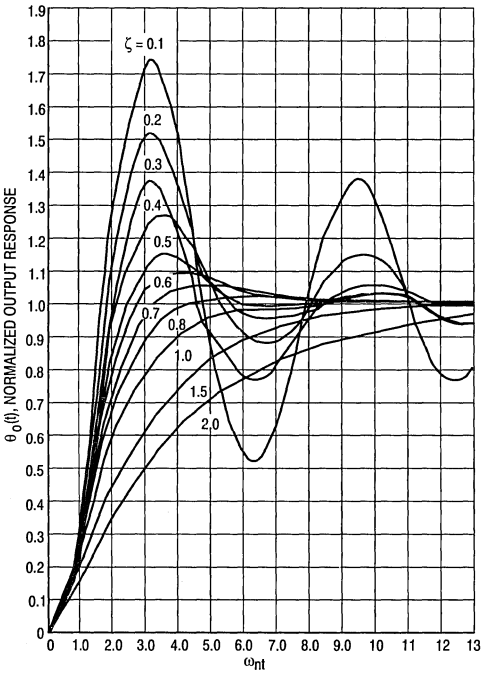
Where: K_p = Phase detector gain constant in μA/rad; K_p = 30 μA/rad
K_f = Filter transfer function
K_n = 1/N; N = 8 for the MC13175 and N = 32 for the MC13176
K_o = CCO gain constant in rad/sec/μA
K_o = 9.1 x 10^5 rad/sec/μA

Loop Filtering

The fundamental loop characteristics, such as capture range, loop bandwidth, lock-up time and transient response are controlled externally by loop filtering.

The natural frequency (ω_n) and damping factor (∂) are important in the transient response to a step input of phase or frequency. For a given ∂ and lock time, ω_n can be determined from the plot shown in Figure 12.

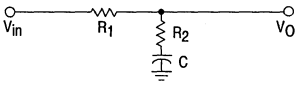
Figure 12. Type 2 Second Order Response



For ∂ = 0.707 and lock time = 1.0 ms;
then ω_n = 5.0/t = 5.0 krad/sec.

The loop filter may take the form of a simple low pass filter or a lag-lead filter which creates an additional pole at origin in the loop transfer function. This additional pole along with that of the CCO provides two pure integrators ($1/s^2$). In the lag-lead low pass network shown in Figure 13, the values of the low pass filtering parameters R_1, R_2 and C determine the loop constants ω_n and ∂. The equations $t_1 = R_1C$ and $t_2 = R_2C$ are related in the loop filter transfer functions $F(s) = 1 + t_2s/1 + (t_1 + t_2)s$.

Figure 13. Lag-Lead Low Pass Filter



The closed loop transfer function takes the form of a 2nd order low pass filter given by,

$$H(s) = K_vF(s)/s + K_vF(s)$$

From control theory, if the loop filter characteristic has F(0) = 1, the DC gain of the closed loop, K_v is defined as,

$$K_v = K_pK_oK_n$$

and the transfer function has a natural frequency,

$$\omega_n = (K_v/t_1 + t_2)^{1/2}$$

and a damping factor,

$$\partial = (\omega_n/2)\ (t_2 + 1/K_v)$$

Rewriting the above equations and solving for the MC13176 with ∂ = 0.707 and ω_n = 5.0 k rad/sec:

$$K_v = K_pK_oK_n = (30)\ (0.91 \bullet 10^6)\ (1/32) = 0.853 \bullet 10^6$$

$$t_1 + t_2 = K_v/\omega_n2 = 0.853 \bullet 10^6/(25 \bullet 106) = 34.1 \text{ ms}$$

$$t_2 = 2\partial/\omega_n = (2)\ (0.707)/(5 \bullet 10^3) = 0.283 \text{ ms}$$

$$t_1 = (K_v/\omega_n2) - t_2 = (34.1 - 0.283) = 33.8 \text{ ms}$$

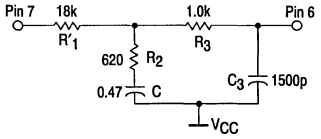
For C = 0.47 μ;
then, $R_1 = t_1/C = 33.8 \bullet 10^{-3}/0.47 \bullet 10^{-6} = 72$ k
thus, $R_2 = t_2/C = 0.283 \bullet 10^{-3}/0.47 \bullet 10^{-6} = 0.60$ k
In the above example, the following standard value components are used,

$C = 0.47\ \mu; R_2 = 620$ and $R'_1 = 72\text{ k} - 53\text{ k} \sim 18$ k

(R'_1 is defined as $R_1 - 53$ k, the output impedance of the phase detector.)

Since the output of the phase detector is high impedance (~50 k) and serves as a current source, and the input to the frequency control, Pin 6 is low impedance (impedance of the two diode to ground is approximately 500 Ω), it is imperative that the second order low pass filter design above be modified. In order to minimize loading of the R_2C shunt network, a higher impedance must be established to Pin 6. A simple solution is achieved by adding a low pass network between the passive second order network and the input to Pin 6. This helps to minimize the loading effects on the second order low pass while further suppressing the sideband spurs of the crystal oscillator. A low pass filter with $R_3 = 1.0$ k and $C_2 = 1500$ p has a corner frequency (f_c) of 106 kHz; the reference sideband spurs are down greater than – 60 dBc.

Figure 14. Modified Low Pass Loop Filter



Hold-In Range

The hold-in range, also called the lock range, tracking range and synchronization range, is the ability of the CCO frequency, f_o to track the input reference signal, $f_{ref} \bullet N$ as it gradually shifted away from the free running frequency, f_f. Assuming that the CCO is capable of sufficient frequency deviation and that the internal loop amplifier and filter are not overdriven, the CCO will track until the phase error, θ_e approaches $\pm\pi/2$ radians. Figures 5 through 8 are a direct measurement of the hold-in range (i.e. $\Delta f_{ref} \bullet N = \pm\Delta f_H \bullet 2\pi$).

Since $\sin\theta_e$ cannot exceed ±1.0, as θ_e approaches $\pm\pi/2$ the hold-in range is equal to the DC loop gain, $K_v \bullet N$.

$$\pm\Delta\omega_H = \pm K_v \bullet N$$

where, $K_v = K_p K_o K_n$.

In the above example,

$$\pm\Delta\omega_H = \pm 27.3\text{ Mrad/sec}$$

$$\pm\Delta f_H = \pm 4.35\text{ MHz}$$

Extended Hold-in Range

The hold-in range of about 3.4% could cause problems over temperature in cases where the free-running oscillator drifts more than 2 to 3% because of relatively high temperature coefficients of the ferrite tuned CCO inductor. This problem might worsen for lower frequency applications where the external tuning coil is large compared to internal capacitance at Pins 1 and 4. To improve hold-in range performance, it is apparent that the gain factors involved must be carefully considered.

K_n = is either 1/8 in the MC13175 or 1/32 in the MC13176.
K_p = is fixed internally and cannot be altered.
K_o = Figures 9 and 10 suggest that there is capability of greater control range with more current swing. However, this swing must be symmetrical about the center of the dynamic response. The suggested zero current operating point for ±100 μA swing of the CCO is at about + 70 μA offset point.
Ka = External loop amplification will be necessary since the phase detector only supplies ± 30 μA.

In the design example in Figure 15, an external resistor (R_5) of 15 k to V_{CC} (3.0 Vdc) provides approximately 100 μA of current boost to supplement the existing 50 μA internal source current. R_4 (1.0 k) is selected for approximately 0.1 Vdc across it with 100 μA. R_1, R_2 and R_3 are selected to set the potential at Pin 7 and the base of 2N4402 at approximately 0.9 Vdc and the emitter at 1.55 Vdc when error current to Pin 6 is approximately zero μA. C_1 is chosen to reduce the level of the crystal sidebands.

Figure 15. External Loop Amplifier

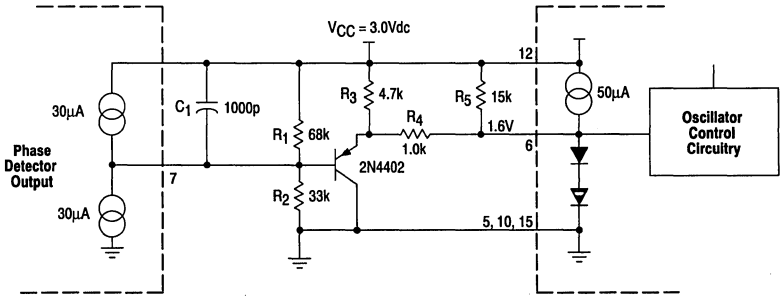
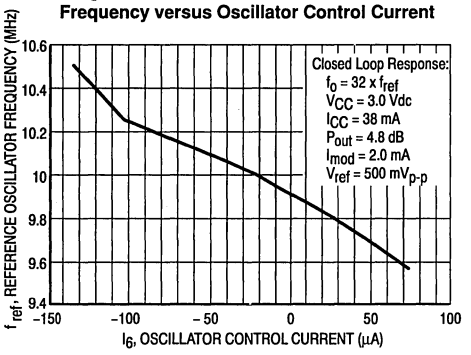


Figure 16 shows the improved hold-in range of the loop. The Δf_{ref} is moved 950 kHz with over 200 μA swing of control current for an improved hold-in range of ±15.2 MHz or ± 95.46 Mrad/sec.

Figure 16. MC13176 Reference Oscillator Frequency versus Oscillator Control Current



Lock-in Range/Capture Range

If a signal is applied to the loop not equal to free running frequency, f_f, then the loop will capture or lock-in the signal by making $f_S = f_O$ (i.e. if the initial frequency difference is not too great). The lock-in range can be expressed as $\Delta\omega_L \sim \pm 2\partial\omega_n$

FM Modulation

Noise external to the loop (phase detector input) is minimized by narrowing the bandwidth. This noise is minimal in a PLL system since the reference frequency is usually derived from a crystal oscillator. FM can be achieved by applying a modulation current superimposed on the control current of the CCO. The loop bandwidth must be narrow enough to prevent the loop from responding to the modulation frequency components, thus, allowing the CCO to deviate in frequency. The loop bandwidth is related to the natural frequency ω_n. In the lag-lead design example where the natural frequency, ω_n = 5.0 krad/sec and a damping factor, ∂ = 0.707, the loop bandwidth = 1.64 kHz. Characterization data of the closed loop responses for both the MC13175 and MC13176 at 320 MHz (Figures 7 and 8, respectively) show satisfactory performance using only a simple low-pass loop filter network. The loop filter response is strongly influenced by the high output impedance of the push-pull current output of the phase detector.

f_C = 0.159/RC;

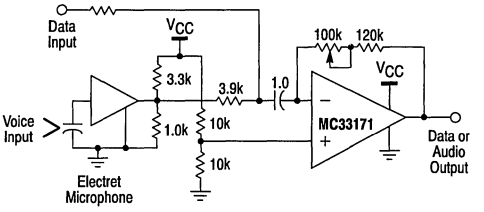
For R = 1.0 k + R_7 (R_7 = 53 k) and C = 390 pF

f_C = 7.55 kHz or ω_C = 47 krad/sec

The application example in Figure 17a of a 320 MHz FM transmitter demonstrates the FM capabilities of the IC. A high value series resistor (100 k) to Pin 6 sets up the current source to drive the modulation section of the chip. Its value is dependent on the peak to peak level of the encoding data and the maximum desired frequency deviation. The data input is AC coupled with a large coupling capacitor which is selected for the modulating frequency. The component placements on the circuit side and ground side of the PC board are shown in Figures 28 and 29, respectively. Figure 18a illustrates the input data of a 10 kHz modulating signal at 1.6 Vp-p. Figures 18b and 18c depict the deviation and resulting modulation spectrum showing the carrier null at – 40 dBc. Figure 18d shows the unmodulated carrier power output at 3.5 dBm for V_{CC} = 3.0 Vdc.

For voice applications using a dynamic or an electret microphone, an op amp is used to amplify the microphone's low level output. The microphone amplifier circuit is shown in Figure 19. Figure 17b shows an application example for NBFM audio or direct FSK in which the reference crystal oscillator is modulated.

Figure 19. Microphone Amplifier

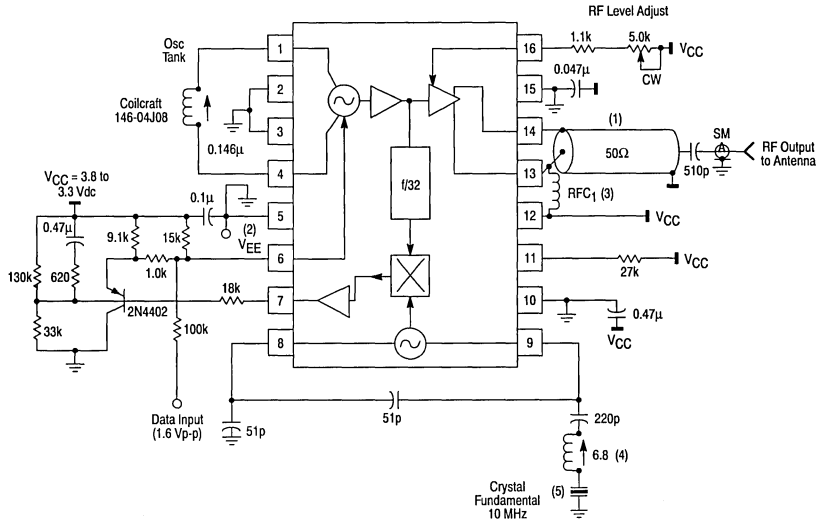


Local Oscillator Application

To reduce internal loop noise, a relatively wide loop bandwidth is needed so that the loop tracks out or cancels the noise. This is emphasized to reduce inherent CCO and divider noise or noise produced by mechanical shock and environmental vibrations. In a local oscillator application the CCO and divider noise should be reduced by proper selection of the natural frequency of the loop. Additional low pass filtering of the output will likely be necessary to reduce the crystal sideband spurs to a minimal level.

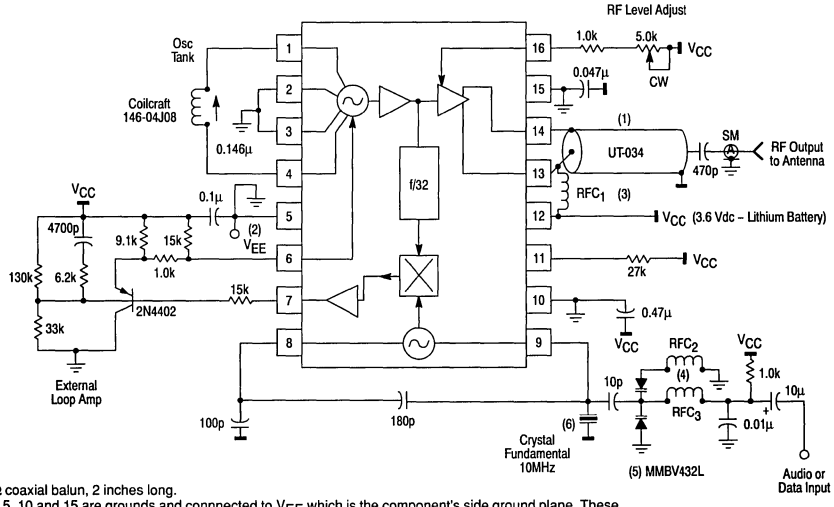
8

Figure 17a. 320 MHz MC13176D FM Transmitter



NOTES: 1. 50 Ω coaxial balun, 2 inches long.
2. Pins 5, 10 and 15 are grounds and connnected to V_{EE} which is the component's side ground plane. These pins must be decoupled to V_{CC}; decoupling capacitors should be placed as close as possible to the pins.
3. RFC_1 is 180 nH Coilcraft surface mount inductor or 190 nH Coilcraft 146-05J08.
4. Recommended source is a Coilcraft "slot seven" 7.0 mm tuneable inductor, part #7M3-682.
5. The crystal is a parallel resonant, fundamental mode calibrated with 32 pF load capacitance.

Figure 17b. 320 MHz NBFM Transmitter



NOTES: 1. 50 Ω coaxial balun, 2 inches long.
2. Pins 5, 10 and 15 are grounds and connnected to V_{EE} which is the component's side ground plane. These pins must be decoupled to V_{CC}; decoupling capacitors should be placed as close as possible to the pins.
3. RFC_1 is 180 nH Coilcraft surface mount inductor.
4. RFC_2 and RFC_3 are high impedance crystal frequency of 10 MHz; 8.2 µH molded inductor gives XL > 1000 Ω.
5. A single varactor like the MV2105 may be used whereby RFC_2 is not needed.
6. The crystal is a parallel resonant, fundamental mode calibrated with 32 pF load capacitance.

Figure 18a. Input Data Waveform

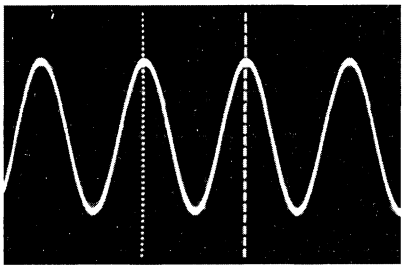


Figure 18b. Frequency Deviation

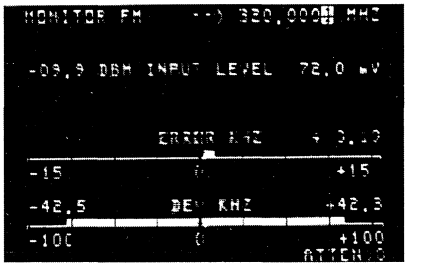


Figure 18c. Modulation Spectrum

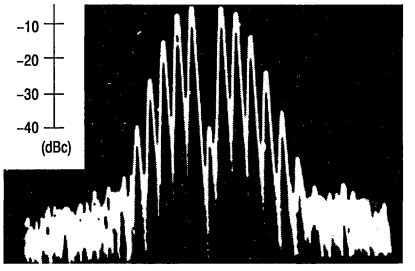
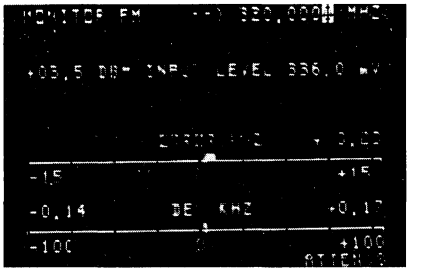


Figure 18d. Unmodulated Carrier



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Reference Crystal Oscillator (Pins 8 and 9)

Selection of Proper Crystal: A crystal can operate in a number of mechanical modes. The lowest resonant frequency mode is its fundamental while higher order modes are called overtones. At each mechanical resonance, a crystal behaves like a RLC series-tuned circuit having a large inductor and a high Q. The inductor L_S is series resonance with a dynamic capacitor, C_S determined by the elasticity of the crystal lattice and a series resistance R_S, which accounts for the power dissipated in heating the crystal. This series RLC circuit is in parallel with a static capacitance, C_p which is created by the crystal block and by the metal plates and leads that make contact with it.

Figure 20 is the equivalent circuit for a crystal in a single resonant mode. It is assumed that other modes of resonance are so far off frequency that their effects are negligible.

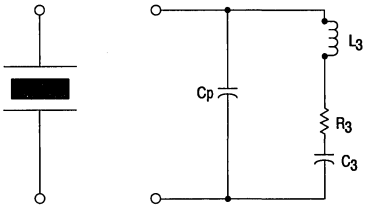
Series resonant frequency, f_S is given by;

$$f_S = 1/2\pi(L_S C_S)^{1/2}$$

and parallel resonant frequency, f_p is given by;

$$f_p = f_S(1 + C_S/C_p)^{1/2}$$

Figure 20. Crystal Equivalent Circuit



the frequency separation at resonance is given by;

$$\Delta f = f_p - f_S = f_S[1 - (1 + C_S/C_p)^{1/2}]$$

Usually f_p is less than 1% higher than f_S, and a crystal exhibits an extremely wide variation of the reactance with frequency between f_p and f_S. A crystal oscillator circuit is very stable with frequency. This high rate of change of impedance with frequency stabilizes the oscillator, because any significant change in oscillator frequency will cause a large phase shift in the feedback loop keeping the oscillator on frequency.

Manufacturers specify crystal for either series or parallel resonant operation. The frequency for the parallel mode is calibrated with a specified shunt capacitance called a "load capacitance". The most common value is 30 to 32 pF. If the load capacitance is placed in series with the crystal, the equivalent circuit will be series resonance at the specified parallel-resonant frequency. Frequencies up to 20 MHz use parallel resonant crystal operating in the fundamental mode, while above 20 MHz to about 60 MHz, a series resonant crystal specified and calibrated for operation in the overtone mode is used.

Application Examples

Two types of crystal oscillator circuits are used in the applications circuits: 1) Fundamental mode common emitter Colpitts (Figures 1, 17a, 17b, and 21). 2) Third overtone impedance inversion Colpitts (also Figures 1 and 21).

The fundamental mode common emitter Colpitts uses a parallel resonant crystal calibrated with a 32 pf load capacitance. The capacitance values are chosen to provide excellent frequency stability and output power of > 500 mVp-p at Pin 9. In Figures 1 and 21, the fundamental mode reference oscillator is fixed tuned relying on the repeatability of the crystal and passive network to maintain the frequency, while in the circuit shown in Figure 17, the oscillator frequency can be adjusted with the variable inductor for the precise operating frequency.

The third overtone impedance inversion Colpitts uses a series resonance crystal with a 25 ppm tolerance. In the application examples (Figures 1 and 21), the reference oscillator operates with the third overtone crystal at 40.0000 MHz. Thus, the MC13175 is operated at 320 MHz ($f_O/8$ = crystal; 320/8 = 40.0000 MHz. The resistor across the crystal ensures that the crystal will operate in the series resonant mode. A tuneable inductor is used to adjust the oscillation frequency; it forms a parallel resonant circuit with the series and parallel combination of the external capacitors forming the divider and feedback network and the base-emitter capacitance of the device. If the crystal is shorted, the reference oscillator should free-run at the frequency dictated by the parallel resonant LC network.

The reference oscillator can be operated as high as 60 MHz with a third overtone crystal. Therefore, it is possible to use the MC13175 up to at least 480 MHz and the MC13176 up to 950 MHz (based on the maximum capability of the divider network).

Enable (Pin 11)

The enabling resistor at Pin 11 is calculated by:

$$R_{reg.\ enable} = V_{CC} - 1.0\ Vdc / I_{reg.\ enable}$$

From Figure 4, $I_{reg.\ enable}$ is chosen to be 75 μA. So, for a V_{CC} = 3.0 Vdc $R_{reg.\ enable}$ = 26.6 kΩ, a standard value 27 kΩ resistor is adequate.

Layout Considerations

Supply (Pin 12): In the PCB layout, the V_{CC} trace must be kept as wide as possible to minimize inductive reactance along the trace; it is best that V_{CC} (RF ground) completely fills around the surface mounted components and interconnect traces on the circuit side of the board. This technique is demonstrated in the evaluation PC board.

Battery/Selection/Lithium Types

The device may be operated from a 3.0 V lithium battery. Selection of a suitable battery is important. Because one of the major problems for long life battery powered equipment is oxidation of the battery terminals, a battery mounted in a clip-in socket is not advised. The battery leads or contact post should be isolated from the air to eliminate oxide build-up. The battery should have PC board mounting tabs which can be soldered to the PCB. Consideration should be given for the peak current capability of the battery. Lithium batteries have current handling capabilities based on the composition of the lithium compound, construction and the battery size. A 1300 mA/hr rating can be achieved in the cylindrical cell battery. The Rayovac CR2/3A lithium-manganese dioxide battery is a crimp sealed, spiral wound 3.0 Vdc, 1300 mA/hr cylindrical cell with PC board mounting tabs. It is an excellent choice based on capacity and size (1.358″ long by 0.665″ in diameter).

Differential Output (Pins 13, 14)

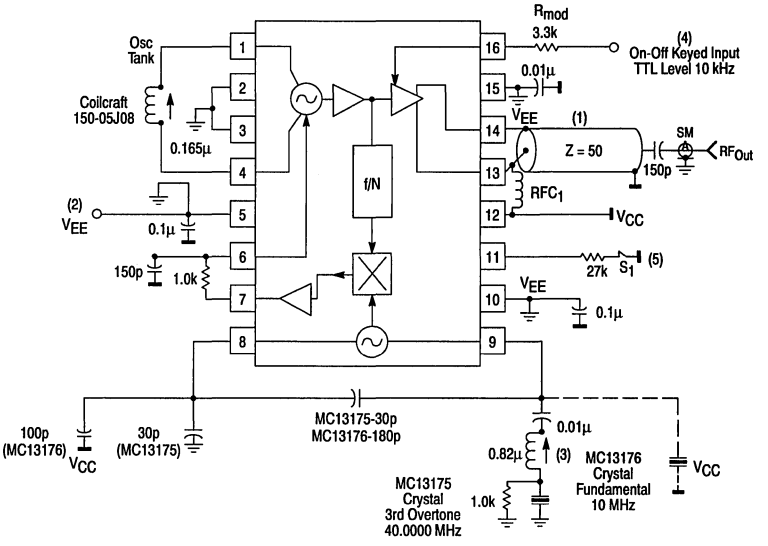
The availability of micro-coaxial cable and small baluns in surface mount and radial-leaded components allows for simple interface to the output ports. A loop antenna may be directly connected with bias via RFC or 50 Ω resistors. Antenna configuration will vary depending on the space available and the frequency of operation.

AM Modulation (Pin 16)

Amplitude Shift Key: The MC13175 and MC13176 are designed to accommodate Amplitude Shift Keying (ASK). ASK modulation is a form of digital modulation corresponding to AM. The amplitude of the carrier is switched between two or more values in response to the PCM code. For the binary case, the usual choice is On-Off Keying (often abbreviated OOK). The resultant amplitude modulated waveform consists of RF pulses called marks, representing binary 1 and spaces representing binary 0.

8

Figure 21. ASK 320 MHz Application Circuit



NOTES: 1. 50 Ω coaxial balun, 1/10 wavelength line (1.5") provides the best match to a 50 Ω load.

2. Pins 5, 10 and 15 are ground and connnected to V_{EE} which is the component/DC ground plane side of PCB. These pins must be decoupled to V_{CC}; decoupling capacitors should be placed as close as possible to the pins.

3. The crystal oscillator circuit may be adjusted for frequency with the variable inductor (MC13175); 1.0 k resistor shunting the crystal prevents it from oscillating in the fundamental mode. Recommended source is Coilcraft "slot seven" 7.0 mm tuneable inductor, part #7M3-821.

4. The On-Off keyed signal turns the output of the transmitter off and on with TTL level pulses through R_{mod} at Pin 16. The "On" power and I_{CC} is set by the resistor which sets I_{mod} = VTTL - 0.8 / R_{mod}. (see Figure 23).

5. S1 simulates an enable gate pulse from a microprocessor which will enable the transmitter. (see Figure 4 to determine precise value of the enabling resistor based on the potential of the gate pulse and the desired enable.)

Figure 21 shows a typical application in which the output power has been reduced for linearity and current drain. The current draw on the device is 16 mA I_{CC} (average) and – 22.5 dBm (average power output) using a 10 kHz modulating rate for the on-off keying. This equates to 20 mA and – 2.3 dBm "On", 13 mA and – 41 dBm "Off". In Figure 22a, the device's modulating waveform and encoded carrier are displayed. The crystal oscillator enable time is needed to set the acquisition timing. It takes typically 4.0 msec to reach full magnitude of the oscillator waveform (see Figure 22b, Oscillator Waveform, at Pin 8). A square waveform of 3.0 V peak with a period that is greater than the oscillator enable time is applied to the Enable (Pin 11).

Figure 22a. ASK Input Waveform and Modulated Carrier

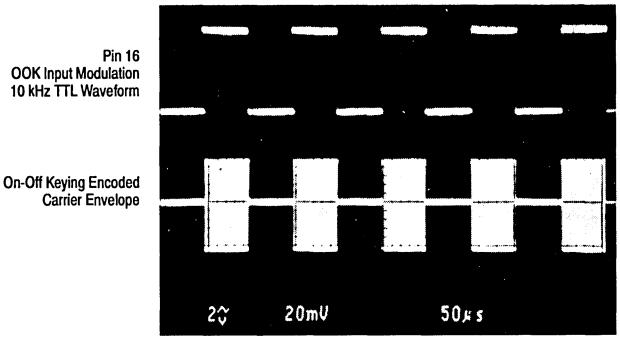


Figure 22b. Oscillator Enable Time, T_{enable}

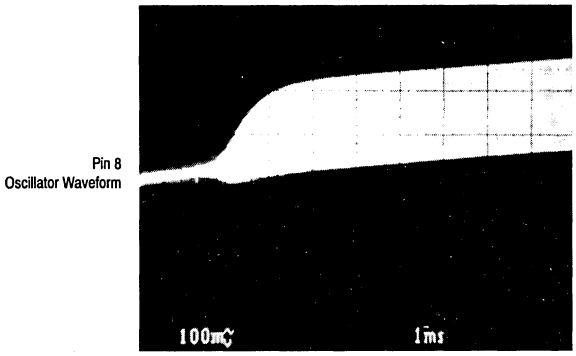
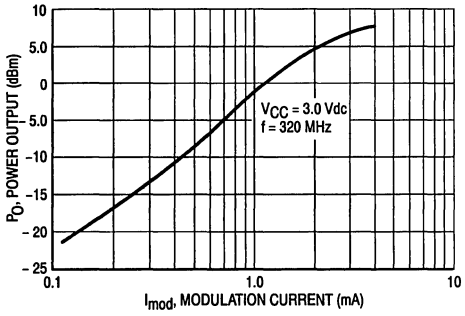


Figure 23. Power Output versus Modulation Current



Analog AM

In analog AM applications, the output amplifier's linearity must be carefully considered. Figure 23 is a plot of Power Output versus Modulation Current at 320 MHz, 3.0 Vdc. In order to achieve a linear encoding of the modulating sinusoidal waveform on the carrier, the modulating signal must amplitude modulate the carrier in the linear portion of its power output response. When using a sinewave modulating signal, the signal rides on a positive DC offset called V_{mod} which sets a static (modulation off) modulation current, I_{mod}. I_{mod} controls the power output of the IC. As the modulating signal moves around this static bias point the modulating current varies causing power output to vary or to be AM modulated. When the IC is operated at modulation current levels greater than 2.0 mAdc the differential output stage starts to saturate.

In the design example, shown in Figure 24, the operating point is selected as a tradeoff between average power output and quality of the AM.

For V_{CC} = 3.0 Vdc; I_{CC} = 18.5 mA and I_{mod} = 0.5 mAdc and a static DC offset of 1.04 Vdc, the circuit shown in Figure 24 completes the design. Figures 25a, 25b and 25c show the results of – 6.9 dBm output power and 100% modulation by the 10 kHz and 1.0 MHz modulating sinewave signals. The amplitude of the input signals is approximately 800 mVp-p.

Where R_{mod} = (V_{CC} – 1.04 Vdc)/0.5 mA = 3.92 k, use a standard value resistor of 3.9 k.

Figure 24. Analog AM Transmitter

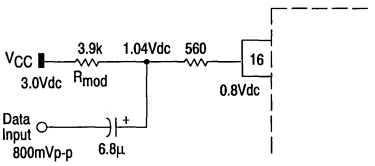


Figure 25a. Power Output of Unmodulated Carrier

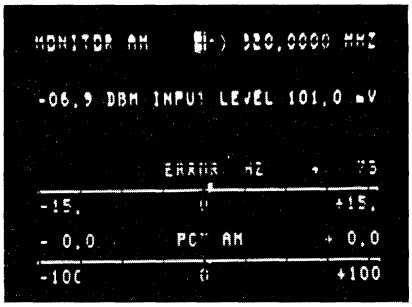


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Figure 25b. Input Signal and AM Modulated Carrier for f_{mod} = 10 kHz

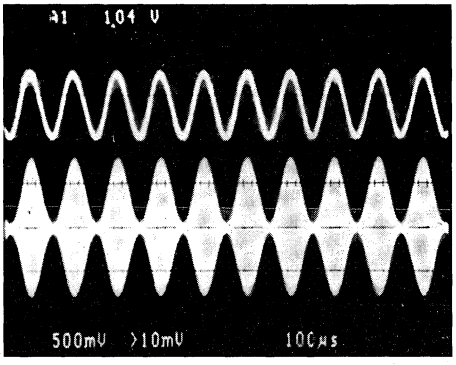


Figure 25c. Input Signal and AM Modulated Carrier for f_{mod} = 1.0 MHz

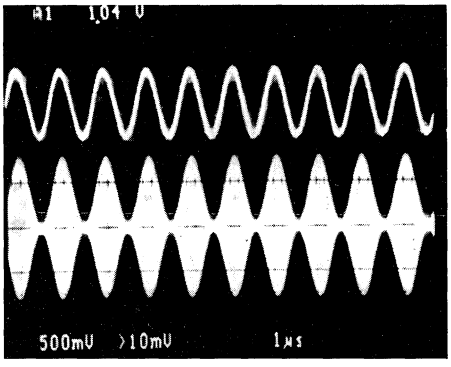


Figure 26. Circuit Side View of MC1317XD

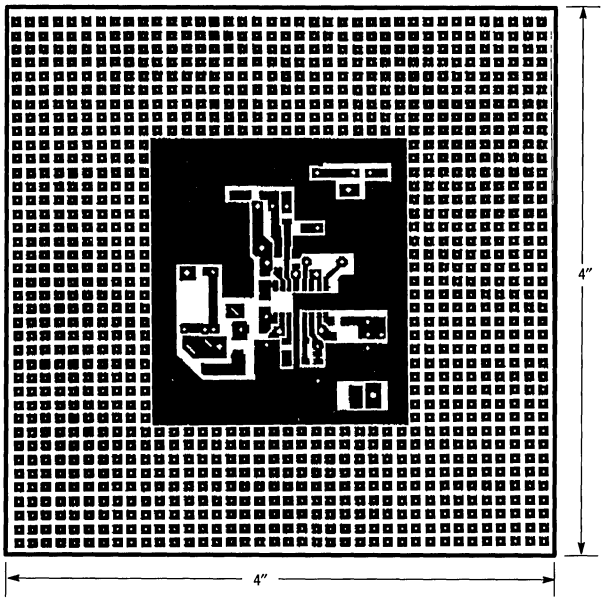


Figure 27. Ground Side View

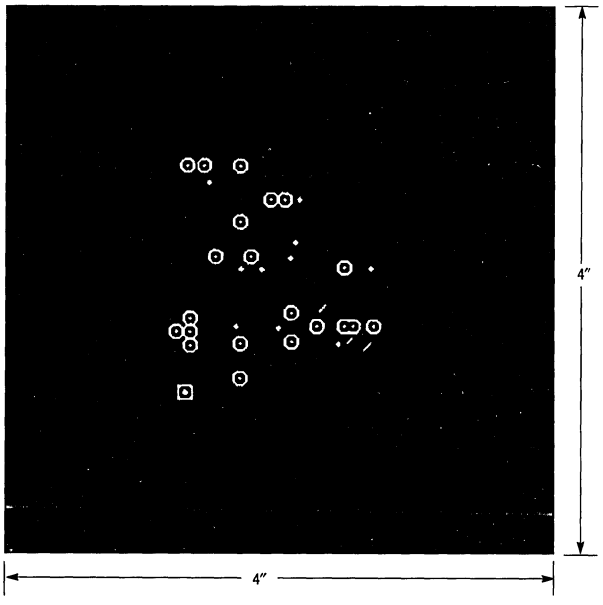


Figure 28. Surface Mounted Components Placement
(on Circuit Side)

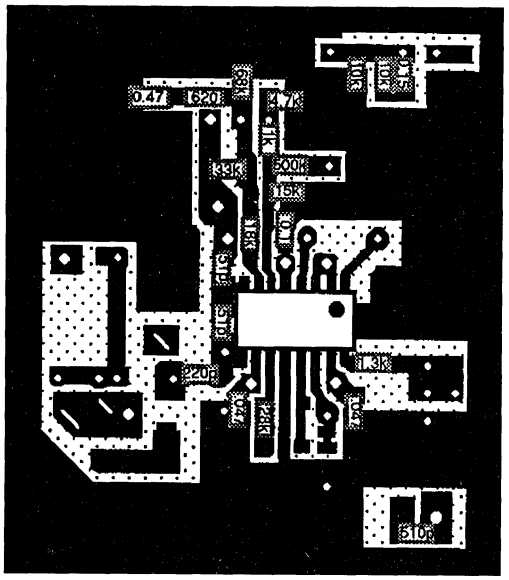
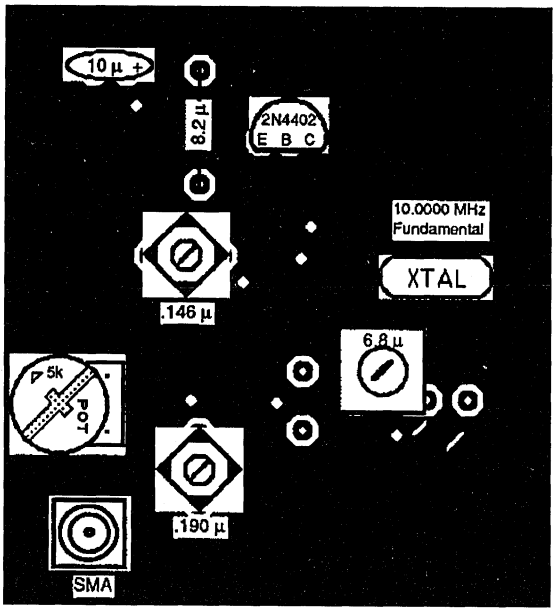


Figure 29. Radial Leaded Components Placement
(on Ground Side)



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC34055

10BASE-T TRANSCEIVER

Product Preview

ISO 8802-3[IEEE 802.3] 10BASE-T Transceiver

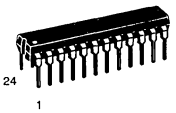
The Motorola 10BASE-T transceiver, designed to comply with the ISO 8802-3 [IEEE 802.3] 10BASE-T specification, will support a Medium Dependent Interface(MDI) in an embedded Media Attachment Unit(MAU)*. The interface supporting the Data Terminal Equipment(DTE) is TTL, CMOS, and raised ECL compatible, and the interface to the Twisted Pair(TP) media is supported through standard 10BASE-T filters and transformers. Differential data intended for the TP media is provided. A 50 ns pre-emphasis and data at the TP receiver is screened by Smart Squelch circuitry for specific threshold, pulse width, and sequence requirements.

Other features of the MC34055 include: Collision and Jabber detection status outputs, select mode pins for forcing Loop Back and Full-Duplex operation, a Signal Quality Error pin for testing the collision detect circuitry without affecting the TP output, and a LED driver for Link Integrity status. An on-chip oscillator, capable of receiving a clock input or operating under crystal control, is also provided for internal timing and driving a buffered clock output.

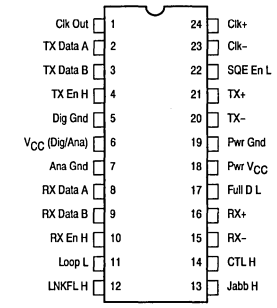
- BiCMOS technology for Low Power Operation
- Standard 5.0 V, ± 5% Power Supply
- Smart Squelch Enforcement of Threshold, Pulse Width, and Sequence Requirements
- Driver Pre-Emphasis for Output Data
- TTL, CMOS and Raised ECL Compatible
- Interfaces to TP Media with Standard 10BASE-T Filters and Transformers
- Status Outputs for Collision and Jabber Detection
- Directly Driven or Crystal Controlled Clock Oscillator
- Selectable Full-Duplex Operation
- Signal Quality Error Test Pin
- Selectable Loop Back

DW SUFFIX
PLASTIC PACKAGE
CASE 751E
(SO-24L)

P SUFFIX
PLASTIC PACKAGE
CASE 724



PIN CONNECTIONS



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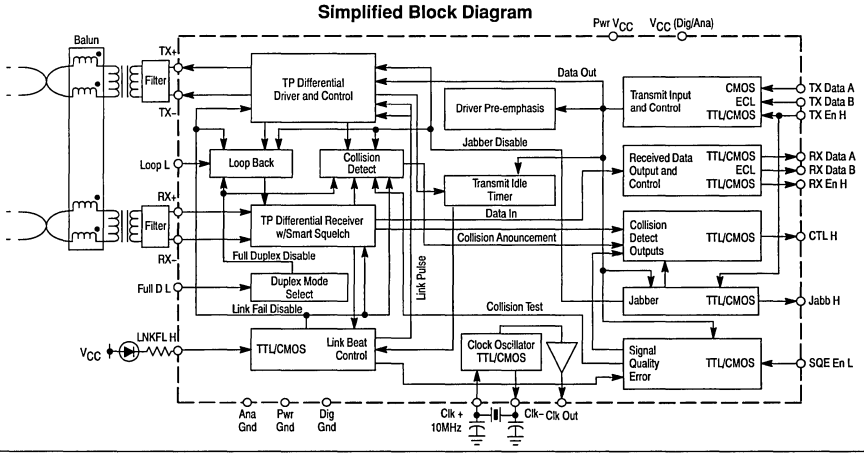
* The sale and use of this product is licensed under technology covered by one or more Digital Equipment Corporation patents.

Simplified Block Diagram



Addendum
An Introduction to Motorola RF Communications IC Applications

In Brief . . .

The RF devices described in the following chapter are targeted for the consumer communications market. In addition, most of these parts are capable of superior performance in professional and industrial applications. These devices represent the latest technology in cost effective RF and audio subsystems for cordless telephones (CT-1), RF LANs, land mobile radio, scanners, cellular telephones, remote control spread spectrum, and amateur radio. The purpose of this introduction is to help the user explore all the opportunities presented by this growing family of wireless communications ICs from Motorola Analog.

Page

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REGULATORY ISSUES

Each country has its own specific set of regulations regarding radio frequency systems and equipment built and sold within their jurisdiction. These regulations are strongly applicable to transmitting devices. The rules are based on both local needs and international treaties. The regulations are established to provide maximum utilization of the limited available radio spectrum. Motorola strongly recommends that you, the user of these communication ICs, obtain the applicable regulations and abide by them.

In the United States, the regulations of the Federal Communications Commission are published in the Code of Federal Regulations (CFR), Title 47, Parts 0 through 99. In the U.S.A. most of the consumer applications fall under CFR 47, Part 15, covering nonlicensed intentional radiators, or Part 68 which covers public network interconnections. CFR 47 may be obtained at most libraries (in the reference section) or from the U.S. Government Printing Office. You may call their office at (213) 894-5841, or (202) 274-2054 for prices and availability. In addition, private contractors such as the Rules Service Company, (301) 424-9402 can provide both the CFR data and an automatic update service. In the U.S.A., further information is available from the FCC field organization.

For the address and telephone number of the nearest office, contact the FCC at:

FCC CONSUMER OFFICE AND SMALL BUSINESS DIVISION
1919 M STREET WEST
WASHINGTON, D.C. 20554
(202) 632-7000

In other countries, the Ministry of Posts or Telecommunications should be contacted. Motorola Semiconductor does not warrant that the applications shown in this data book meet all the conditions prescribed by government regulations.

INDUSTRY STANDARDS

Throughout the world the telecommunications industry has established working standards committees to ensure equipment compatibility by setting minimum standards. These standards also help make the best use of the available radio spectrum. In the U.S.A., the Electronic Industries Association (E.I.A.) has developed a series of these recommended standards which have become the defacto global guidelines.

The following standards apply to Frequency Modulation (FM) systems.

EIA/TIA-204C	EIA STANDARD	FM/PM RECEIVER STANDARDS
EIA/TIA-152B	EIA STANDARD	FM/PM TRANSMITTER STANDARDS
EIA/TIA-316B	EIA STANDARD	TEST CONDITIONS, PORTABLE PERSONAL RADIO

For additional information and pricing, contact the E.I.A. at the following address:

ELECTRONIC INDUSTRIES ASSOCIATION
ENGINEERING DEPARTMENT
2001 EYE STREET N.W.
WASHINGTON, D.C. 20006
(202) 457-4900

COMMUNICATIONS SYSTEMS

For the most part, the devices described in Chapter 8 use frequency modulation (FM) for both analog voice and data. FM is generally considered the simplest and most cost efficient modulation type today. FM offers excellent: noise rejection; good sensitivity; reduction of interference due to the FM capture effect; simple circuitry; and an array of test equipment, most of which has spun-off the land mobile market. Direct digital transmission may also be accomplished using Frequency Shift Keying (FSK) or Amplitude Shift Keying (ASK).

The devices shown in this chapter are designed to operate at frequencies below 1.0 GHz (1000 MHz). Today, that frequency range offers the best compromise among performance, complexity and cost. Over the next decade there will be an increasing movement to 1.0 to 3.0 GHz, as the demand for more complex personal communications systems comes on-line. Motorola will add products to its line-up as these microwave applications become better defined.

Several reference books on Communications Theory and Design are listed below. These books are generally available at major public and university libraries.

THE RADIO AMATEUR'S HANDBOOK, American Radio Relay League, Newington, CT.
MICROWAVE THEORY AND APPLICATIONS, Steven F. Adam, Hewlett Packard, Prentice Hall.
SOLID STATE RADIO ENGINEERING, Herbert L. Krauss , Charles W. Bosdan, F.H. Raab, Wiley 1980.
RF CIRCUIT DESIGN, Chris Bowick, Howard Sams & Co., 1982.
INTRODUCTION TO COMMUNICATIONS SYSTEMS, Ferrel Stremler, Addison Wesley.
ARRL ANTENNA HANDBOOK, American Radio Relay League, Newington, CT.
STANDARD RADIO COMMUNICATIONS MANUAL, R.H. Kinley, CET, Prentice Hall, 1985.

In addition, you may find very timely design and component information in the following magazines:

R.F. DESIGN, Cardiff Publishing (708) 647-0756.
MICROWAVES AND RF, Penton Publishing (216) 696-7000.

PASSIVE COMPONENTS

The availability of passive components — coils, filters, crystals, capacitors, resonators, resistors, etc. — is often a larger problem than finding the RF or analog IC to meet your needs. The Motorola applications engineering team considers this a key issue when developing the circuits shown in our data sheets. Analog Applications has worked with many suppliers to develop practical and reasonably priced passive component selections. Suppliers who have a global support structure and can supply both prototype and production quantities are listed. The following table lists a number of suppliers which have been used in recent applications. You will also need information on the performance of the component as a function of temperature, frequency, solderability and reliability. Most of these suppliers have applications-engineering support who can provide a wealth of specific technical information. Motorola, however, cannot warrant these suppliers' quality, availability, or prices. Motorola suggests contacting these suppliers directly to obtain technical information and competitive quotes.

In many cases, recommendations have been made to use readily available sources such as "Radio Shack" for small parts and construction material. The user is encouraged to develop a core of dependable and local, if possible, suppliers for his or her passive components. Please note that many data sheets have specific passive components which have been used to develop and characterize the integrated circuit. Constructing a "benchmark" circuit with these components is an excellent starting point in the development of a new design.

COMPONENT SUPPLIERS

QUARTZ CRYSTALS — FREQUENCY CONTROL:

California Crystal Laboratories	(800) 333-9825
Fox Electronics	(813) 693-0099
International Crystals	(405) 236-3741
Standard Crystal Corporation	(818) 443-2121

GENERAL COMPONENTS — PROTOTYPE QUANTITIES — ASSEMBLY MATERIAL — PC BOARD MATERIAL:

Digi-Key Corporation	(800) 344-4539
Radio Shack Division, Tandy Corporation	(See local telephone directory)

INDUCTORS, COILS, RF TRANSFORMERS, FIXED AND VARIABLE:

CoilCraft	(800) 322-COIL
	(708) 639-6400
Toko America, Inc.	(708) 297-0070

CERAMIC FILTERS AND RESONATORS, IF FILTERS — AM AND FM TYPES:

muRata Erie	(404) 436-1300 (Todd Brown, Harry Moore)
TDK Corporation of America	(708) 803-6100
Toko America, Inc.	(708) 297-0070

BREADBOARDING

Breadboarding RF or other high speed analog circuits can be a very frustrating process for the newcomer or even an experienced digital designer. Most of these circuits deal with very high gain (100+ dB), very small signals (less than a few microvolts), or with very high frequencies where a wavelength may be a fraction of a meter. Once "friendly" 0.1 μF capacitors may now be inductors due to their parasitic inductance, and conventional construction methods may yield only circuits that oscillate.

What to avoid (never use these):

— Wire wrap for RF or high frequency breadboards.
— Conventional push-in prototype boards.
— Digital printed protoboards with ground and power supply bus lines.

What to use:

— Carefully laid-out double-sided groundplane PC boards.
— Grid boards with a background plane.
— Single-sided PC layouts with continuous full ground fill.
— High frequency qualified components.
— Adequate decoupling.

You will find recommended PC layouts for most of the communications circuits in this chapter. These layouts are strongly recommended as starting points for new designs. They will allow you to develop your own benchmark standard circuit to be used as a standard of comparison during further design iterations. Many Motorola communications ICs have supporting development kits which include a PC board. These boards are meant to provide performance equivalent to the data sheets specifications and are easy to modify for other uses but these boards, however, are not optimized or intended for production applications. Contact your Motorola sales office or Motorola distributor for information on the availability of these development kits.

In addition, there are many PC and Macintosh-based CAD programs available today. In general, these programs work well for digital and low frequency analog circuits, but are of very limited value in RF applications. SPICE models are not currently available for the communications circuits. Several circuits do show S-Parameter data or admittance plane information which may be used to optimize input or output matching for gain or noise. The most useful method of utilizing the applications circuits at different frequencies is simple linear scaling of the tuning and reactive elements. This method is generally applicable over a 2:1 frequency range lower than the documented application.

Many communications applications include some digital signaling, data conversion, or microcontroller interface. The RF designer must take great caution to avoid interference with the low level analog circuits in these mixed-mode systems. The receivers are particularly susceptible to noise as they respond to signals of only a few microvolts. Make sure the clock frequency is not a sub-multiple of the receiver input or IF frequencies. Keep the DC supply lines for the digital and analog circuitry separate. Avoid ground paths carrying common digital and analog currents. As much common sense as analytical skill goes into a successful RF design. A good consultant may well save many times their fee in material, lost time, and rework.

TEST EQUIPMENT

Establishing a new RF communications lab can be a very costly investment. The normal DVMs and regulated power supplies are generally acceptable if they do not generate spurious RF, and are not sensitive to RF voltages. You should pick an oscilloscope with a frequency response three or more times higher than your operating frequency. In addition, a low capacitance probe — FET probe — would be useful. Remember, while conventional probes have very high input resistance, their capacitive reactance decreases with frequency and becomes a limiting factor above 30 MHz. For most transmitter work, a basic spectrum analyzer is a must. It will help confirm power output, spurious output levels, stability, and modulation characteristics.

Rental and used equipment are often a good source of test equipment. Recently, Communications System Analyzers have become available at very moderate prices. The Motorola R2600, for example, combines 16 different instruments into one portable package. The signal generator, receiver, counter, oscilloscope and a "best-in-class" modulation meter make this package a very attractive design and production test tool. Further information, including a demonstration, are available from your local Motorola Communications and Electronics sales office.

Consumer Electronic Circuits

In Brief . . .

These integrated circuits reflect Motorola's continuing commitment to semiconductor products necessary for consumer system designs. This tabulation is arranged to simplify selection of consumer integrated circuit devices that satisfy the primary functions for home entertainment products, including television, hi-fi audio and AM/FM radio.

Entertainment Radio Receiver Circuits

Entertainment Receiver RF/IF

Function	Features	Suffix/ Case	Device
E.T.R. Front End	Mixer/VCO/AGC for Electronically Tuned AM Stereo Receivers	P/648 D751B	MC13025

C-Quam® AM Stereo Decoders

Function	Features	Suffix/ Case	Device
Basic AM Stereo Decoder	Monaural/Stereo AM Detector/Indicator, 6 to 10 V Operation	P/738	MC13020
Advanced AM Stereo Decoder	Medium Voltage 2 to 8 V, Decoder and IF Amp	DW/751F	MC13022
AM Stereo Personal Radio	Complete Low Voltage AM Stereo Receiver	P/724	MC13024
Low V AM Stereo Receiver	IF/Decoder for Advanced C-Quam Receivers	D/751B	MC13028

Audio Amplifiers

Function	P_O (Watts)	V_{CC} Vdc Max	V_{in} @ Rated P_O mV Typ	I_D mA Typ	R_L (Ohms)	Suffix/ Case	Device
Mini Watt SOIC Audio Amp	1.0 W	35	80	11	16	D/751	MC13060
Low Power Audio Amp	400 mW	16	—	2.5 mA	8–100	D/751 P/626	MC34119

Audio Attenuator

Function	V_{CC} Range (Vdc)	THD (%)	Tone Control Range dB Typ	Attenuation Range dB Typ	Suffix/ Case	Device
Electronic Attenuator	8–18	0.6 Typ	±13	80	P/626	MC3340

Video Circuits

Video Circuits

Function	Features	Suffix/ Case	Device
Encoders			
RGB to PAL/NTSC Encoder	RGB and Sync inputs, Composite Video out; PAL/NTSC selectable.	P/738 DW/751D	MC1377
Advanced RGB to PAL/NTSC Encoder	RGB and Sync inputs, Composite Video and S-VHS out; PAL/NTSC selectable; subcarrier from crystal or external source.	P/738 DW/751D	MC13077
Decoders			
TV Color Processor	PAL/NTSC input, RGB outputs; also RGB inputs, Fast blanking, ideal for text, graphics, overlay.	P/711	TDA3301B
TV Color Processor	PAL/NTSC input, RGB outputs	P/724	TDA3330
Chroma 10 Timebase and Color NTSC/PAL Decoder	PAL/NTSC input, RGB outputs; horizontal and vertical timing processors.	P/711	MC13017
Chroma 4 Multistandard Decoder (TV set)	PAL/NTSC/S-VHS input, RGB outputs; horizontal and vertical timing outputs; all digital internal filters, no external tank; μP and crystal controlled.	P/711	MC44001
Chroma 4 Multistandard Decoder (Multimedia)	PAL/NTSC/S-VHS input, RGB/YUV outputs; horizontal and vertical timing outputs; all digital internal filters, no external tanks; μP and crystal controlled.	FN/777	MC44011
Video Capture Chip Set			
Chroma 4 Multistandard Decoder (Multimedia)	PAL/NTSC/S-VHS input, RGB/YUV outputs; horizontal and vertical timing outputs; all digital internal filters, no external tanks; μP and crystal controlled.	FN/777	MC44011
PAL Digital Delay Line	For PAL applications of the MC44011 and MC44001.	P/648 D/751	MC44140
Pixel Clock PLL/Sync Sep.	PAL/NTSC sync separator, 6-40 MHz pixel clock PLL.	D/751	MC44145
Triple 8-Bit Video DAC	TTL inputs, 75 Ω drive outputs.	FB/824	MC44200
Triple 8-Bit Video A/D	Video clamps for RGB/YUV, 15 MHz, TTL outputs.	FN/777	MC44250
	Video clamps for RGB/YUV, 18 MHz, High Z TTL outputs.	FN/777	MC44251
Advanced NTSC Comb Filter	Composite Video input; YC outputs in digital and analog form; all digital internal filters.	FB/898	MC141621
Advanced PAL/NTSC Comb Filter	Composite Video input; YC outputs in digital and analog form; all digital internal filters.	FB/898	MC141625
Deflection			
Horizontal Processor	Linear balanced phase detector, oscillator and predriver, adjustable DC loop gain and duty cycle.	P/626	MC1391
Waveform Generator for Monitors	Provides geometry correction by generating 10 waveforms to modulate deflection circuitry. Supports multifrequency operation.	P/711	MC1388
Line Deflection Transistor Driver	Provides optimum drive control of the power transistor, peak current limiting, overvoltage and thermal protection.	P/648	MC44614
Waveform Generator for Projection TV Convergence Function	Provides geometry correction by generating 18 waveforms to modulate deflection circuitry. Supports multifrequency operation.	P/711	MC44615A

Video Circuits (continued)

Function	Features	Suffix/ Case	Device
Comb Filters			
Enhanced Comb Filter	Fast 8-bit A/D converter, two 8-Bit D/A Converters, two line-delay memories, utilizes NTSC subcarrier frequency clock, CMOS technology	FB/898	MC141620
Advanced NTSC Comb Filter	Composite Video input; YC outputs in digital and analog form; all digital internal filters.	FB/898	MC141621
Advanced PAL/NTSC Comb Filter	Composite Video input; YC outputs in digital and analog form; all digital internal filters.	FB/898	MC141625
IF Circuits			
Advanced Video IF	Complete video/audio IF system for high performance analog TV receivers.	P/724 DW/751F	MC44301
Video Detector	3rd IF, video detector, video buffer and AFC buffer.	P/626	MC1330A
IF Amplifier	1st and 2nd video IF amplifiers, 50 dB gain at 45 MHz, 60 dB AGC range.	D/751 P/626	MC1350
Tuner PLL Circuits			
PLL Tuning Circuits	1.3 GHz, 20 mV sensitivity, selectable prescaler, op amp, 7 band buffers, I^2C interface.	P/707	MC44802A
	1.3 GHz, 5.0 mV sensitivity, selectable prescaler, op amp, 4 band buffers, SPI interface, lock detect.	P/648 D/751	MC44807 MC44817
	1.3 GHz, 10 mV sensitivity, selectable prescaler, op amp, 7 band buffers, I^2C interface, 3 DACs.	P/738	MC44810
	1.3 GHz, 20 mV sensitivity, prescaler, 3 band buffers, I^2C interface, replacement for Siemens MPG3002.	D/751	MC44824
	1.3 GHz, 5.0 mV sensitivity, prescaler, op amp, 4 band buffers, I^2C interface, lock detect.	D/751	MC44818
Modulators			
Color TV Modulator	RF Oscillator and Modulator.	P/626	MC1373
Color TV Modulator with Sound	RF Oscillator/Modulator, and FM Sound Oscillator/Modulator.	P/646	MC1374
Video Data Converters			
Single Channel 7-Bit A/D	7-Bit, 25 MHz, 2.0 V input range, ± 5.0 V supplies, TTL output, no pipeline delay.	P/738 DW/751D	MC10321
Single Channel 7-Bit A/D	8-Bit, 25 MHz, 2.0 V input range, ± 5.0 V supplies, TTL output, no pipeline delay.	P/709 DW/751E	MC10319
Triple 8-Bit Video A/D	Video clamps for RGB/YUV, 15 MHz conversion.	FN/777	MC44250
	Video clamps for RGB/YUV, 18 MHz conversion, high Z outputs.	FN/777	MC44251
Single Channel 8-Bit Video DAC	40 MSPS, video controls ± 5.0 V, TTL inputs.	P/649	MC10322
	40 MSPS, video controls – 5.0 V, ECL inputs.	P/649	MC10324
Triple 8-Bit Video DAC	TTL inputs, 75 Ω drive outputs.	FB/824	MC44200
Television Subsystems			
Monomax Black and White TV Subsystem	IF, Video processor, horizontal and vertical timing, for NTSC applications, 525 line systems.	P/710	MC13001X
Monomax Black and White TV Subsystem	IF, Video processor, horizontal and vertical timing, for PAL applications, 625 line systems.	P/710	MC13007X

Video Circuits (continued)

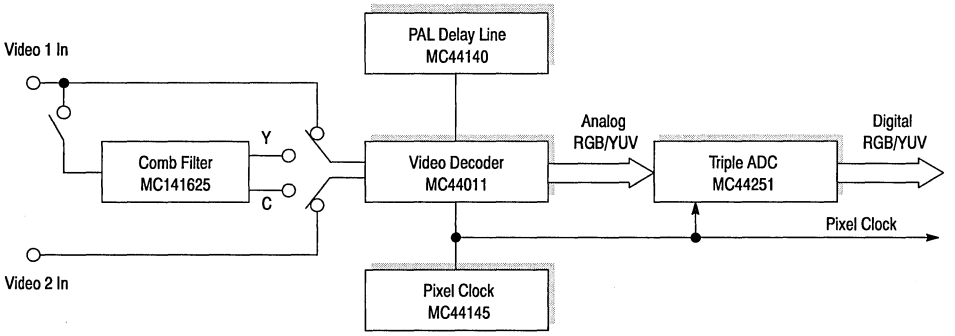
Function	Features	Suffix/ Case	Device
Monitor Subsystem			
Multimode Color Monitor Processor	Triple video amplifiers, horizontal PLLs and deflection timing, vertical ramp generator, 30 to 57 kHz.	B/0051	MC13081
Sound			
Sound IF Detector	Interchangeable with ULN2111A.	P/646	MC1357
Sound IF with Preamp	Sound IF, Low Pass Filter, FM Detector, DC Volume Control, Preamplifier, 100 μV sensitivity, 4.0 W output into 16 Ω.	P/648C	TDA3190
Miscellaneous			
Video Overlay Synchronizer	Complete Color TV Video Overlay Synchronizer, remote or local system control.	P/711 FN/777	MC1378
Subcarrier Reference Generator	Provides continuous subcarrier sine wave and 4x subcarrier, locked to incoming burst.	P/626 D/751	MC44144
Closed Caption Decoder	Conforms to FCC, NTSC standards, underline and italics control.	P/707	MC144143
Sync Separator/Pixel Clock PLL	PAL/NTSC sync separator with vertical and composite sync output, 6.0 to 40 MHz pixel clock PLL.	D/751	MC44145
Dual Video Amplifiers	Gain @ 4.43 MHz = 6 dB ±1 dB, fixed gain, internally compensated, CMOS technology.	P/626 F/904	MC14576B
	Gain @ 5.0 MHz = 10 dB maximum, 10 MHz = 6 dB maximum, adjustable gain, internally compensated, CMOS technology.	P/626 F/904	MC14577B
Transistor Array	One differential pair and 3 isolated transistors, 30 V, 50 mA.	D/751	CA3146
Transistor Array	One differential pair and 3 isolated transistors, 15 V, 50 mA.	P/626 D/751	MC3346

Bringing video into the personal computer allows a multitude of multimedia application dreams to become possible. Old applications can be done in new ways. Totally new applications, before impossible, become reality.

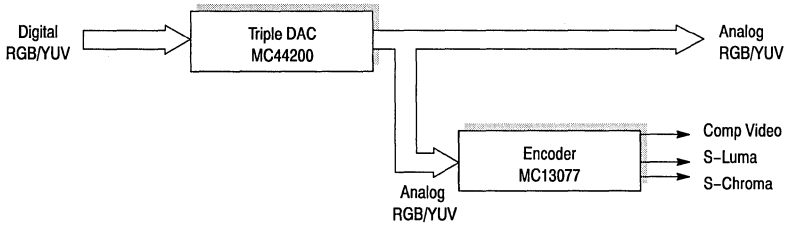
Moving beyond text and graphics to real images is what Motorola can bring to the user. Utilizing Motorola integrated circuits, video can be captured, processed and brought onto the screen where the video image can be scaled, clipped, zoomed, windowed, overlayed. or process enhanced in ways never before possible.

Also included in this selector guide you will find products for TV and other TV related functions that will allow you to produce advanced TV products. These products span the range of applications including tuner control, video decoding, closed-captioning, stereo sound decoding and video encoding and synchronizing.

Video Input Processing



Video Output Processing

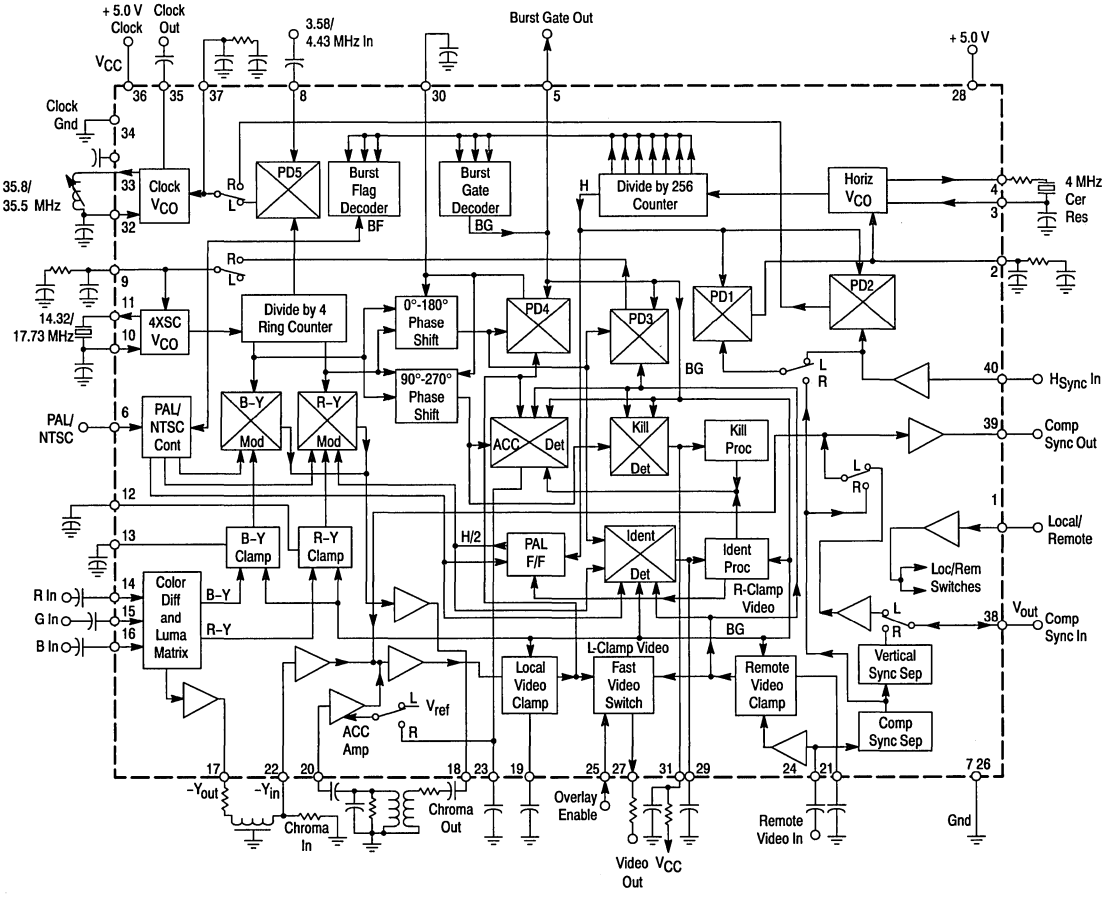


Composite Video Overlay Synchronizer

MC1378P, FN Case 711, 777

The MC1378 contains a complete encoder function, i.e. quadrature color modulators, RGB matrix, and blanking level clamps, plus a complete complement of synchronizers to lock a microcomputer based video source to any remote video source. The MC1378 can be used as a local system timing and encoding source, but it is most valuable when used to lock the microcomputer source to a remotely originated video signal.

- Contains All Needed Reference Oscillators
- Can Be Operated in PAL or NTSC Mode, 625 or 525 Line
- Wideband, Full Fidelity Color Encoding
- Local or Remote Modes of Operation
- Minimal External Components
- Single 5.0 V Supply
- Works with Non-Standard Video

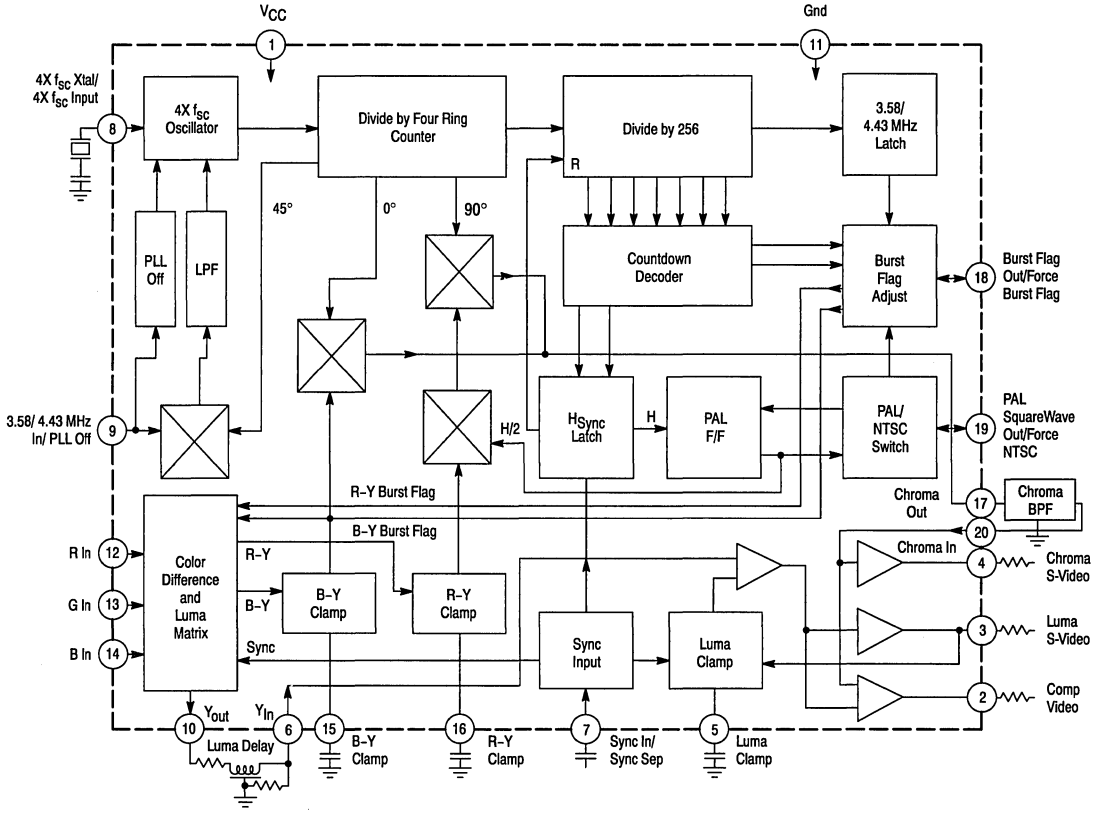


Advanced PAL/NTSC Encoder

MC13077P, DW Case 738, 751D

The MC13077 is an economical, high quality, RGB encoder for PAL or NTSC applications. It accepts red, green, blue and composite sync inputs and delivers either composite PAL or NTSC video, and S-Video Chroma and Luma outputs. The MC13077 is manufactured using Motorola's high density, bipolar MOSAIC® process.

- Single 5.0 V Supply
- Composite Output
- S-Video Outputs
- PAL/NTSC Switchable
- PAL Squarewave Output
- PAL Sequence Resettable
- Internal/External Burst Flag
- Modulator Angles Accurate to 90°
- Burst Position/Duration Determined Digitally
- Subcarrier Reference from a Crystal or External Source

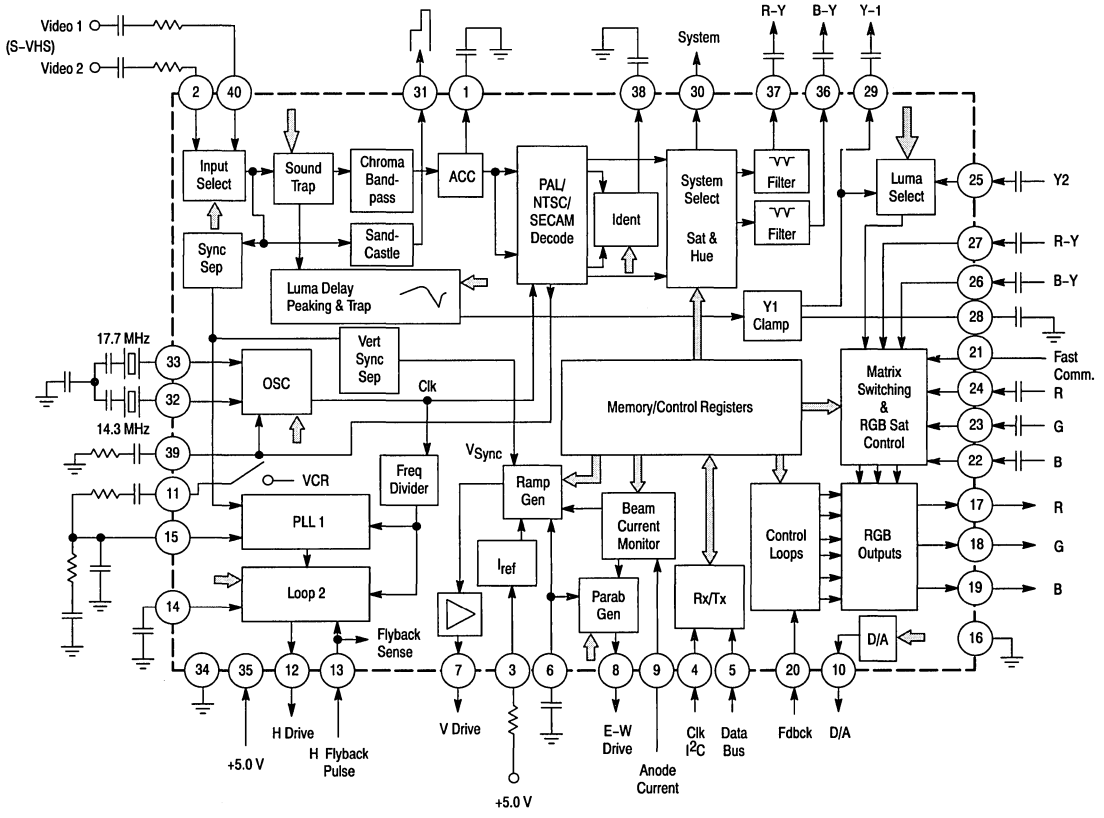


Multistandard Video/Timebase Processor

MC44001P Case 711

The MC44001 is a highly advanced circuit which performs most of the basic functions required for a color TV. All of its advanced features are under processor control via an I^2C bus, enabling potentiometer controls to be removed completely. In this way the component count may be reduced dramatically, allowing significant cost savings together with the possibility of implementing sophisticated automatic test routines. Using the MC44001, TV manufacturers will be able to build a standard chassis for anywhere in the world.

- Operation from a Single +5.0 V Supply; Typical Current Consumption only 100 mA
- Full PAL/SECAM/NTSC Capability
- Dual Composite Video or S-VHS Inputs
- All Chroma/Luma Channel Filtering, and Luma Delay Line are Integrated using Sampled Data Filters requiring no External Components
- Filters Automatically Commutate with Change of Standard
- Chroma Delay Line is Realized with Companion Device (MC44140)
- RGB Drives Incorporate Contrast and Brightness Controls and Auto Gray Scale
- Switched RGB Inputs with Separate Saturation Control
- Auxiliary Y, R-Y, B-Y Inputs
- Line Timebase Featuring H-Phase Control and Switchable Phase Detector Gain and Time Constant
- Vertical Timebase Incorporating the Vertical Geometry Corrections
- E-W Parabola Drive Incorporating the Horizontal Geometry Corrections
- Beam Current Monitor with Breathing Compensation



Digitally Controlled Video Processor for Multimedia Applications

MC44011FN Case 777

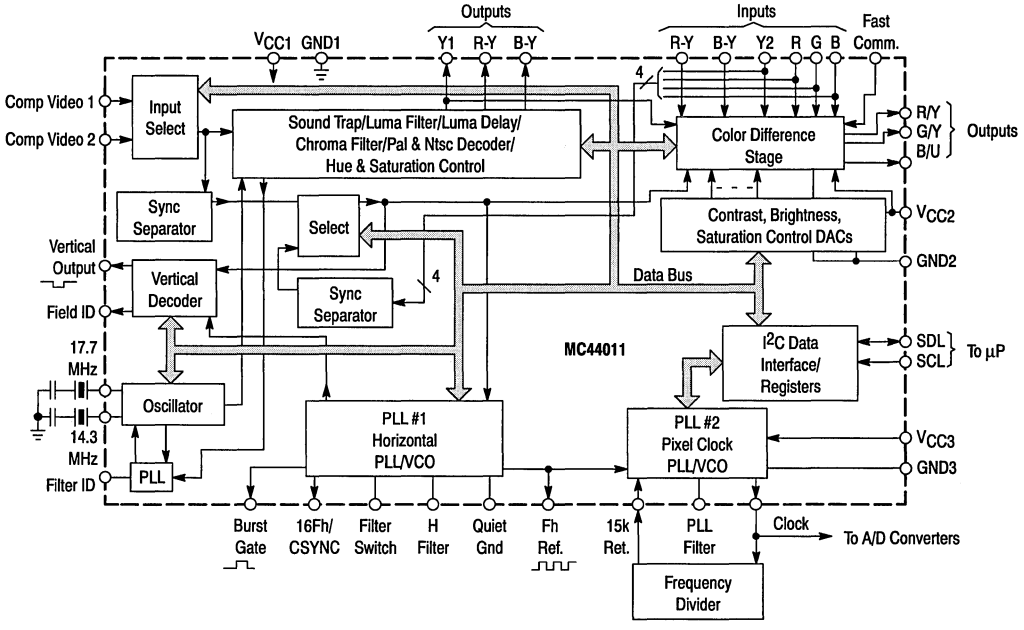
The MC44011, a member of the MC44000 Chroma 4 family, is designed to provide RGB or YUV outputs from a variety of inputs. The inputs may be either PAL or NTSC composite video (two inputs), S-VHS, RGB, and color difference (R-Y, B-Y).

The MC44011 provides a sampling clock output for use by a subsequent analog to digital converter. The sampling clock (6.0 to 40 MHz) is phase-locked to the horizontal frequency. Additional outputs include composite sync, vertical sync, field identification, luminance, burst gate, and horizontal frequency.

Control of the MC44011, and reading of status flags is accomplished via an I^2C bus.

- Multistandard Decoder, Accepts NTSC and PAL Composite Video
- Dual Composite Video or S-VHS Inputs
- All Chroma and Luma Channel Filtering, and Luma Delay Line are Integrated using Sampled Data Filters requiring no External components
- Digitally Controlled via I^2C Bus
- Auxiliary Y, R-Y, B-Y Inputs
- Switched RGB Inputs with Separate Saturation Control
- Line-Locked Sampling Clock for Digitizing Video Signals
- Burst Gate Pulse Output for External Clamping
- Vertical Sync and Field Ident Outputs
- Software Selectable YUV or RGB Outputs able to Drive A/D Converters

MC44011 Block Diagram

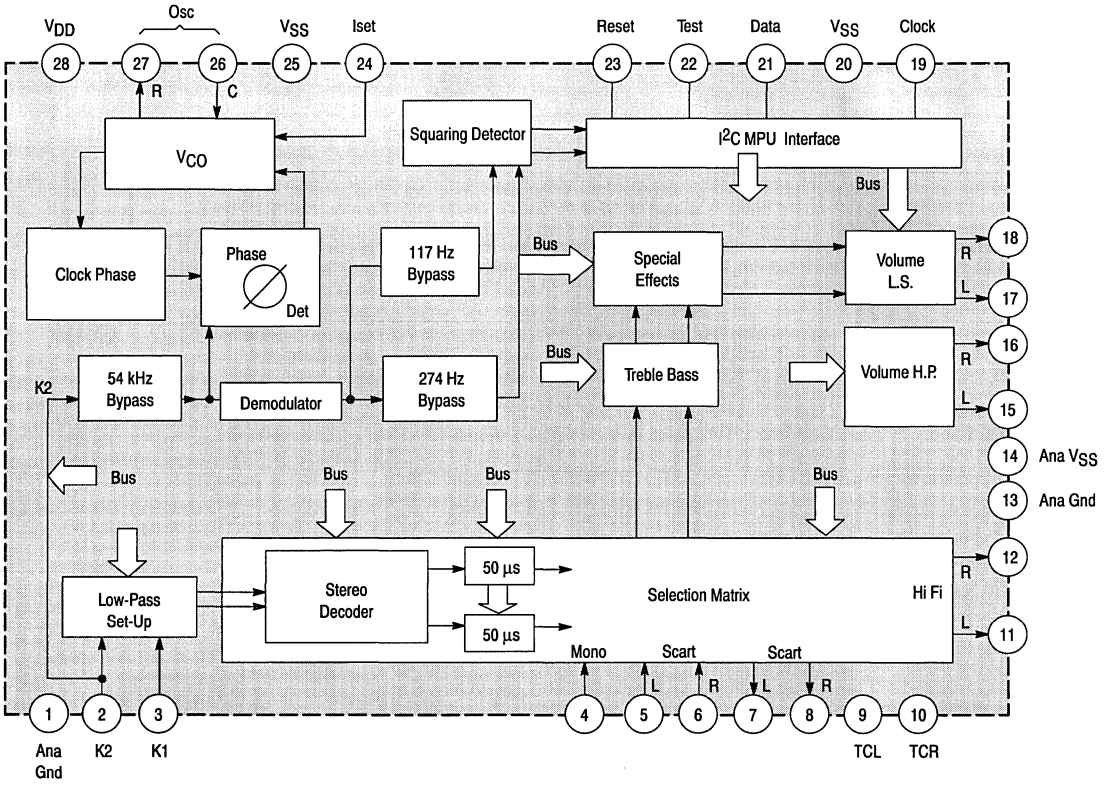


TV Stereo Decoder for NICAM and German System

MC44131P Case 710

The MC44131 combines all of the functions necessary for the decoding and sound control in accordance with the NICAM and German Standard transmission systems. It is controlled via a microprocessor and I²C bus.

- Pilot Tone Decoding
- Baseband Stereo Signal Decoding
- Signal De-emphasis
- Direct Balance Adjustment via Software
- I²C Bus Controlled Routing of the Baseband/ Monaural/SCART Inputs to Loudspeaker/Headphone/ Hi Fi/Scart Outputs
- Loudspeaker Output Control of Tone, Special Effects, Independent Left-Right Volume Control
- Headphone Output Control of Independent Left-Right Volume Control

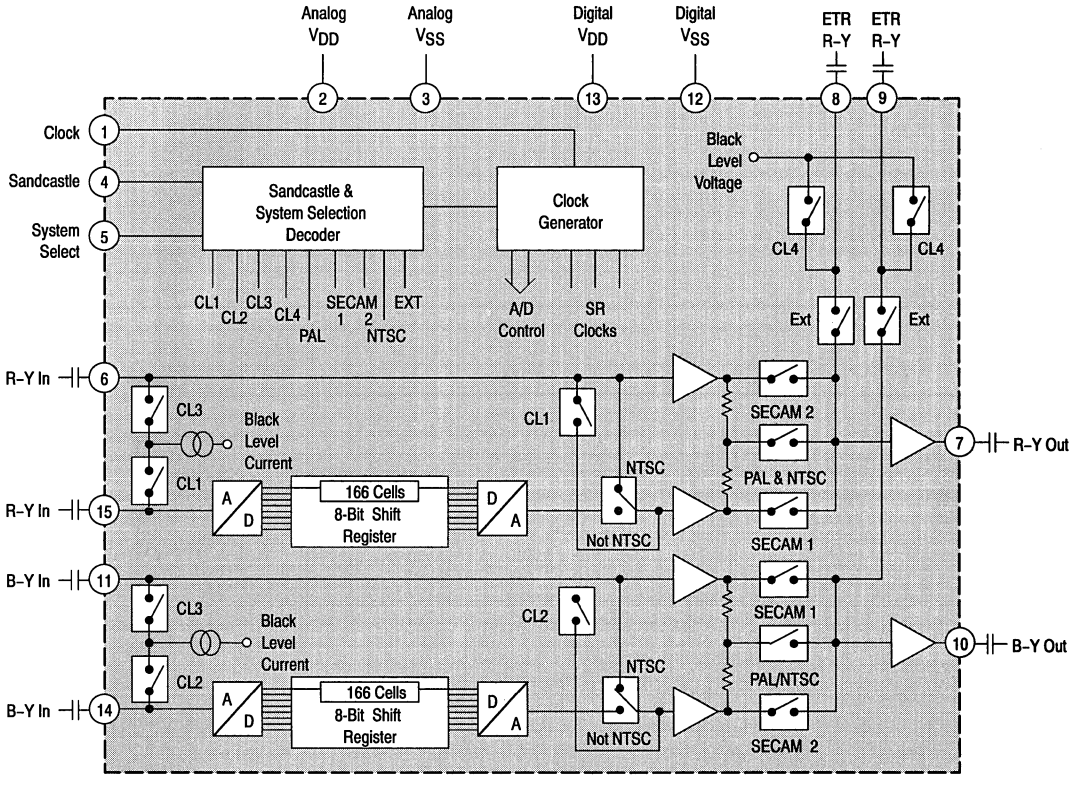


Digital Chroma Delay Line

MC44140P, DW Case 648, 751G

The MC44140 is a monolithic 64 µs delay line, intended for color TV applications. It may be used as a baseband chroma correction circuit (with PAL), or as a chroma delay line (with SECAM). The device has been designed for use with the MC44000 as part of Chroma 4, or with the MC44011, but may also be used as a general purpose delay line for other applications.

- Part of SYSTEM 4 Concept
- Works with Baseband Color Difference Signals
- PAL (4.43 MHz)/SECAM/NTSC Capability
- Uses 17.734475 MHz Clock with PAL/SECAM Signals
- 8-Bit Sampling at 1/6 Clock Frequency
- External Inputs (Satellite ...)
- Minimum Number of External Components
- Low Current (35 mA), +5.0 V Supply



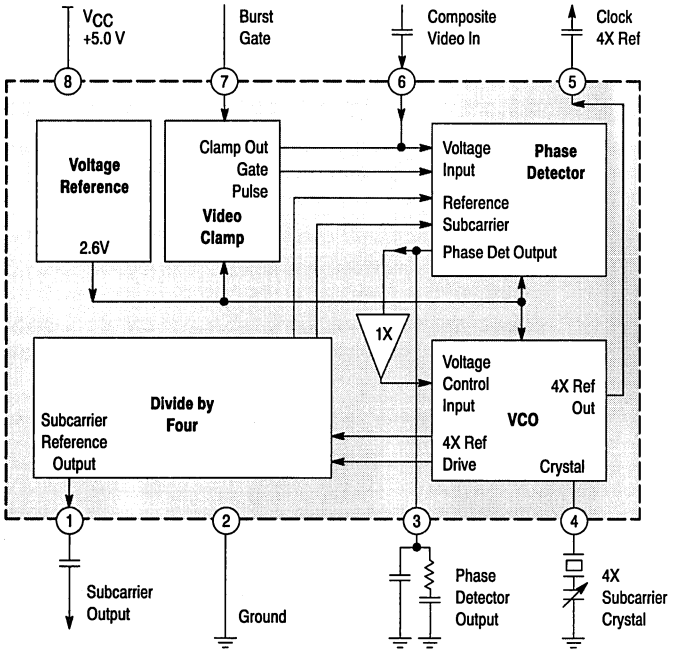
Subcarrier Reference

MC44144P, D Case 626, 751

The MC44144 is a phase-locked-loop for video applications that provides the subcarrier frequency, and 4 times subcarrier frequency locked to the color burst. It contains, on a single chip, a phase detector, voltage controlled oscillator, divide-by-four, and video clamp.

The MC44144 is manufactured using Motorola 's high density, bipolar MOSAIC® process.

- Provides 4x Frequency Locked to Color Burst
- Provides Regenerated Subcarrier Output
- 5.0 V Operation



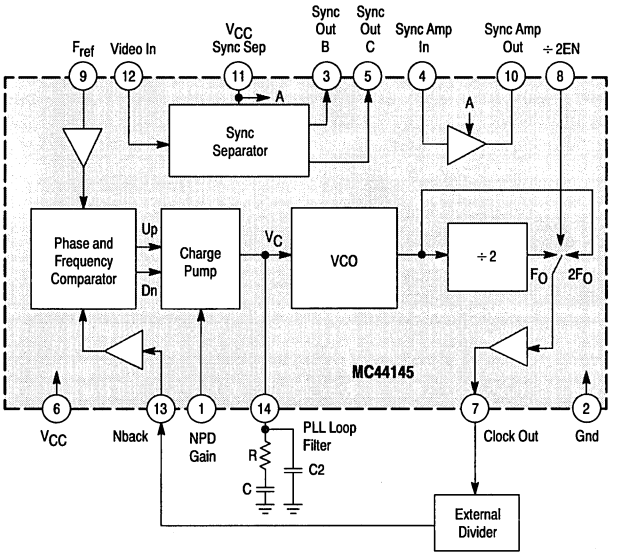
9

Pixel Clock Generator and Sync Separator

MC44145D Case 751A

The MC44145 Pixel Clock Generator is a component of the M44000 family. This device contains a sync separator with horizontal and vertical outputs, and clock generation circuitry for the digitization of any video signal, along with the necessary circuitry for clock generation such as a phase comparator and a ÷2 to provide a 50% duty cycle.

- Stand Alone PLL Circuit
- Switchable Divider for 50% Duty Cycle
- Integrated Sync Separator
- Integrated Buffer Amplifier



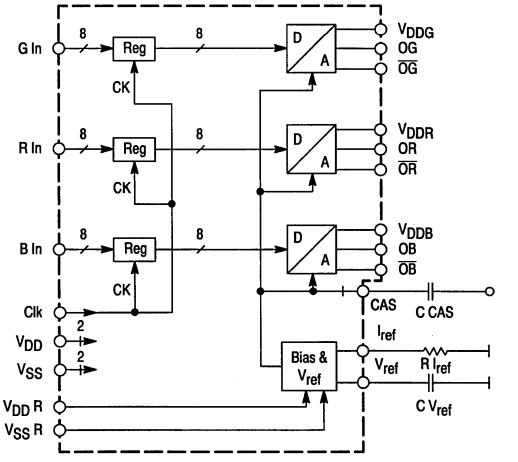
9

Triple 8-Bit D/A Converter

MC44200FB Case 824A

The MC44200 is a monolithic digital to analog converter for three independent channels fabricated in CMOS technology. The part is specifically designed for video applications. Differential outputs are provided, allowing for a large output voltage range.

- 8-Bit Resolution
- Differential Outputs
- 80 msps Conversion Speed
- Large Output Voltage Range
- Low Current Mode
- Single 5.0 V Power Supply
- TTL Compatible Inputs
- Integrated Reference Voltage



Triple 8-Bit A/D Converter

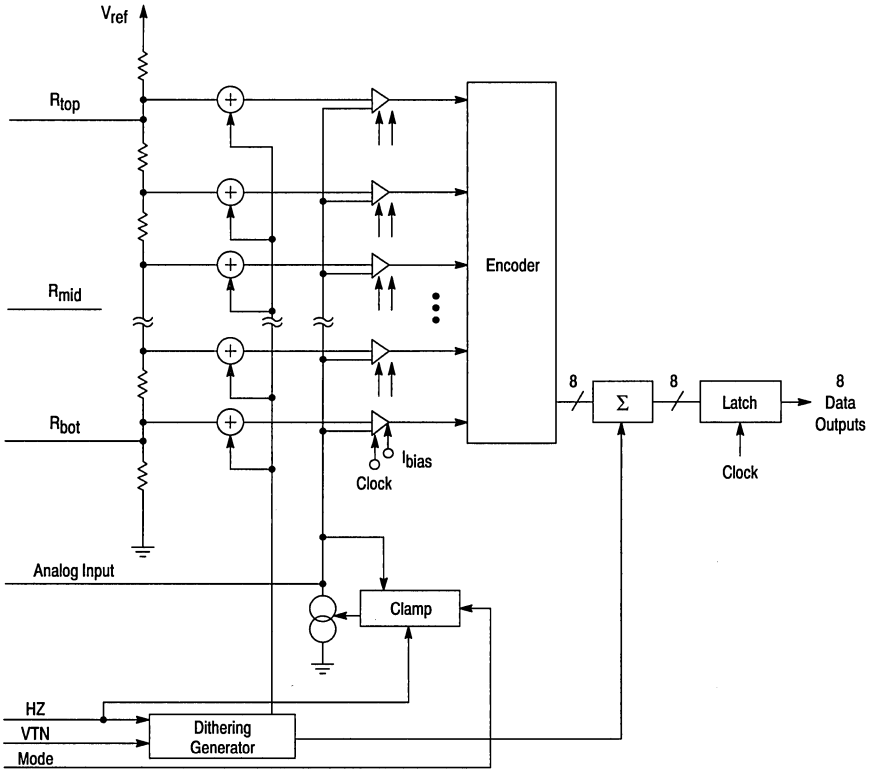
MC44250/51FN Case 777

The MC44250 and MC44251 contain three independent parallel analog to digital converters. Each ADC consists of 256 latching comparators and an encoder. Input clamps allow for AC coupling of the input signals, and DC coupling is also allowed. For video processing performance enhancements, a dither generator with subsequent digital correction is provided to each ADC. The outputs of the MC44251 can be set to a high impedance state.

These A/Ds are especially suitable as front end converters in TV picture processing.

- 15 MHz Maximum Conversion Speed (MC44250)
- 18 MHz Maximum Conversion Speed (MC44251)
- Input Clamps suitable for RGB and YUV applications
- Built-in Dither Generator with Subsequent Digital Correction
- Single 5.0 V Power Supply

Simplified Diagram of One of the ADCs

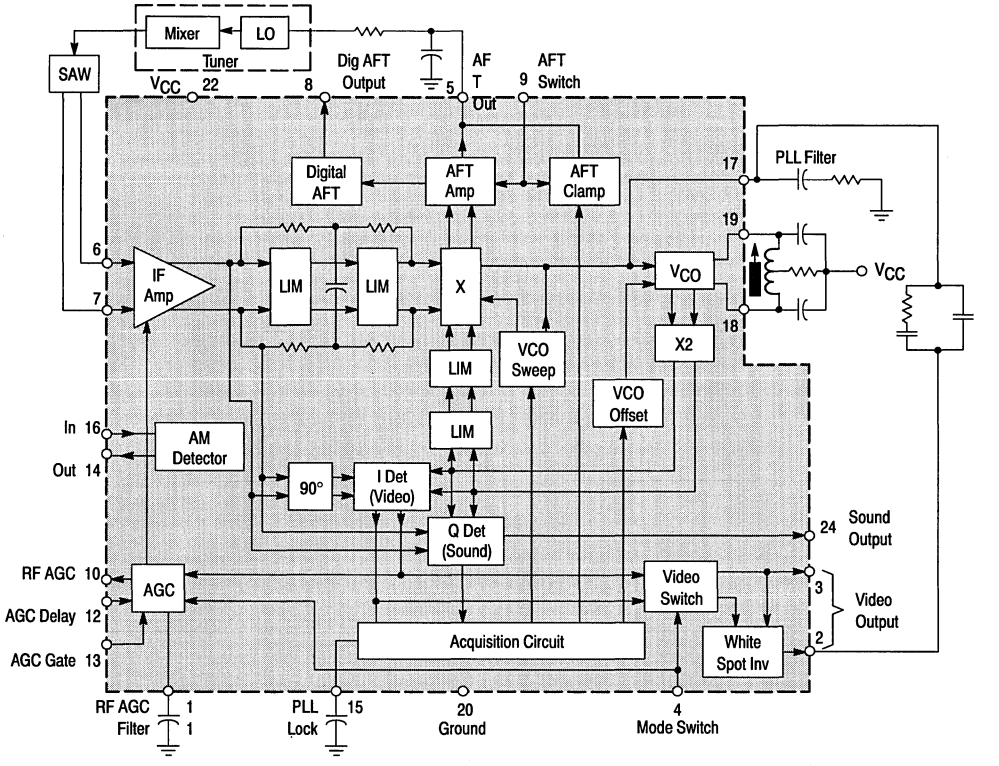


Multistandard Video IF

MC44301P, DW Case 724, 751F

The MC44301 is a single channel TV IF and PLL detector system for all standard transmission systems. This device enables the designer to produce a high quality IF system with white spot inversion, AFT and AGC. The MC44301 was designed with an emphasis on linearity to minimize sound/picture intermodulation.

- Single Coil Adjustment for AFT and PLL
- VCO at 1/2 IF for Minimum Beats
- Simple Circuitry for Low System Cost
- White Spot Inversion
- Symmetrical ± 2.0 MHz AFT Pull-In
- Demodulates Positive or Negative Modulation
- Auxiliary AM Detector for AM Sound
- Simple Alignment Procedure

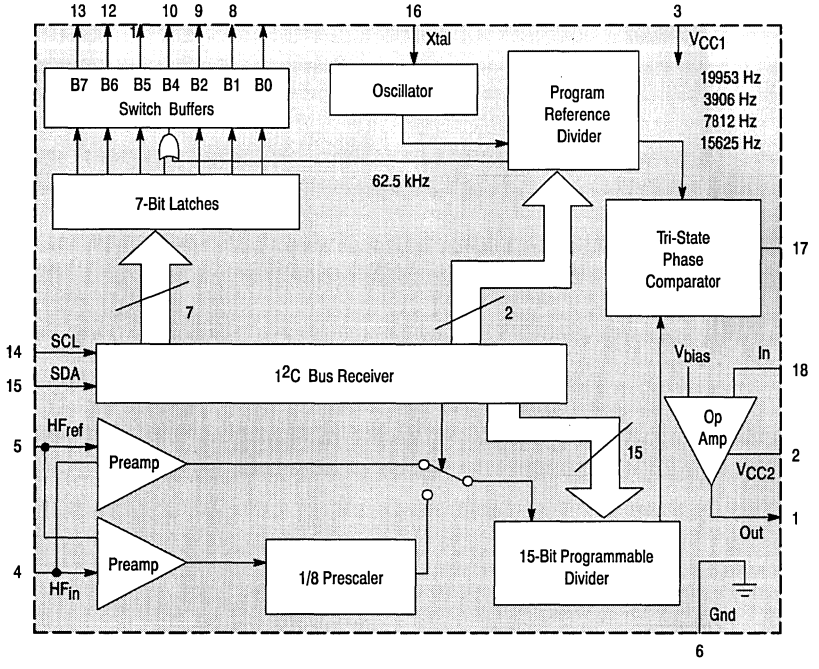


1.3 GHz Tuner PLL with I²C Control

MC44802AP Case 707

The MC44802A is a tuning circuit for TV applications. It contains, on one chip, all the functions required for PLL control of a V_{CO}. This integrated circuit also contains a high frequency prescaler (which can be bypassed by software control) and thus handle frequencies up to 1.3 GHz.

- Complete Single Chip System for MPU Control (I²C Bus)
- Selectable ÷ 8 Prescaler Accepts Frequencies Up to 1.3 GHz
- Programmable Reference Divider
- Tri-State Phase/Frequency Comparator
- Op Amp for Direct Tuning Voltage Output: 30 V
- Seven High Current Buffers: 10 mA, 12 V
- Output Options for 62.5 kHz, Reference Frequency and the Programmable Divider
- Software Compatible with the MC44810
- I²C Interface

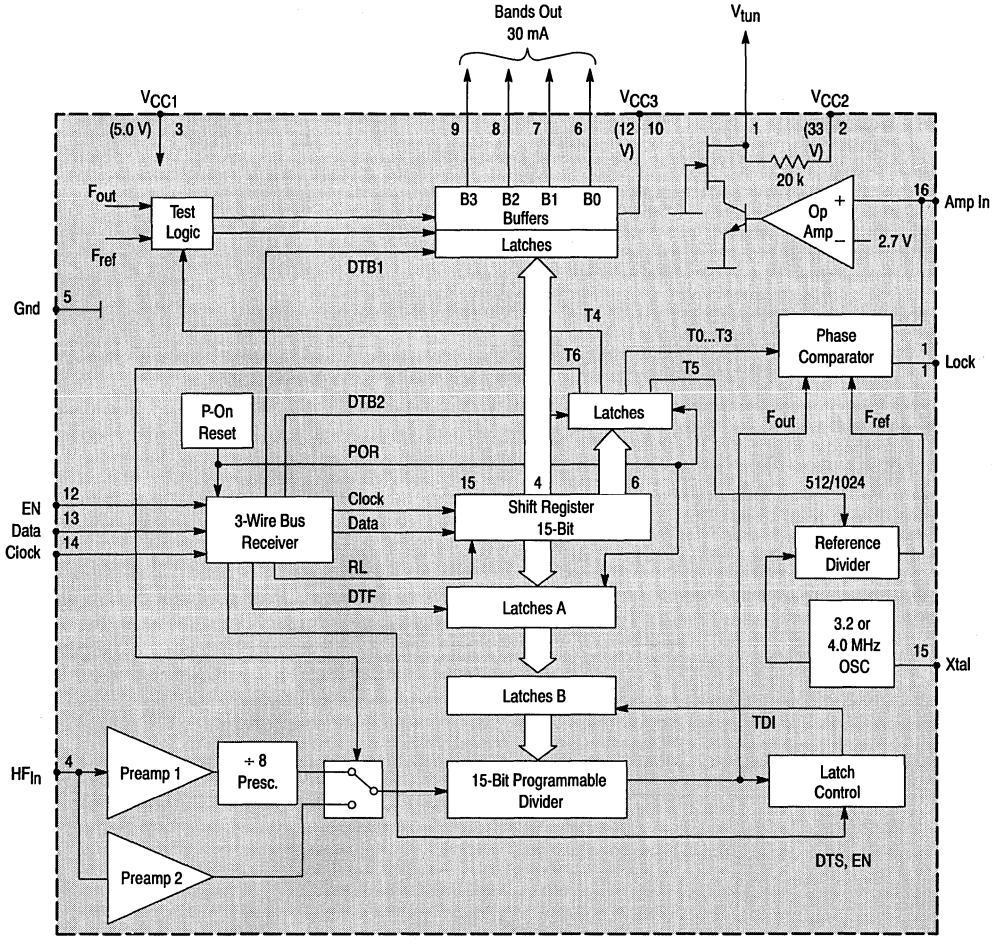


1.3 GHz Tuner PLL with 3-Wire Control

MC44807P/17D Case 648, 751B

The MC44807/17 is a tuning circuit for TV applications. It contains, on one chip, all the functions required for PLL control of a V_{CO}. This integrated circuit also contains a high frequency prescaler (which can be bypassed by software control) and thus handle frequencies up to 1.3 GHz.

- Complete Single Chip System for MPU Control (3-Wire Bus)
- ÷ 8 Prescaler Accepts Frequencies Up to 1.3 GHz
- 15-Bit Programmable Reference Divider Accepts Frequencies Up to 165 MHz
- Tri-State Phase/Frequency Comparator with Lock Detect Output
- Op Amp for Direct Tuning Voltage Output: 30 V
- Four Integrated Band Buffers for 40 mA (V_{CC1} to 14.4 V)
- Output Options for Reference Frequency and Programmable Divider
- Bus Protocol for 18 or 19-Bit Transmission
- High Input Sensitivity



PLL Tuning Circuit with DACs for Tuner Alignment

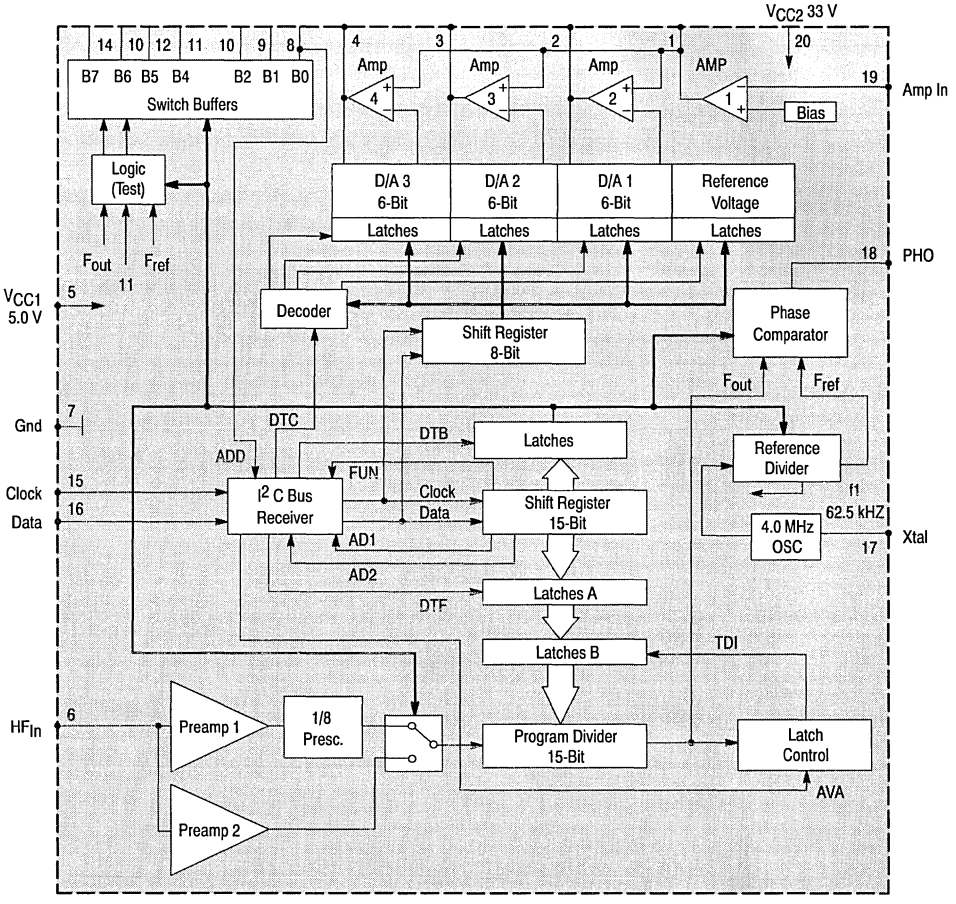
MC44810P Case 738

The MC44810 is a tuning circuit for TV applications. It contains a PLL section and a DAC section and is MPU controlled through the I²C bus.

The PLL section contains all the functions required to control the V_{CO} of a TV tuner. It generates the tuning voltage and the additional control signals. The PLL section is functionally equivalent to the MC44802A.

The DAC section generates three varactor voltages in order to feed all of the tuner varactors with their individually optimized control voltages (automatic tuner adjustment).

- Complete Single Chip System for MPU Control (I²C Bus)
- Tri-State Phase/Frequency Comparator
- Selectable ÷ 8 Prescaler accepts Frequencies up to 1.3 GHz
- 15-Bit Programmable Reference Divider accepts Frequencies up to 165 MHz
- Op Amp for Direct Tuning Voltage Output: 30 V
- Seven High Current Buffers: 10 mA, 12 V
- Output Options for 62.5 kHz, Reference Frequency and Programmable Divider
- Software Compatible with the MC44802A
- Three 6-Bit DACs for Automatic Tuner Adjustment Allowing use of Non-Matched Varactors
- 2-Chip Addresses for the PLL Section and 2 Different Chip Addresses for the DAC Section

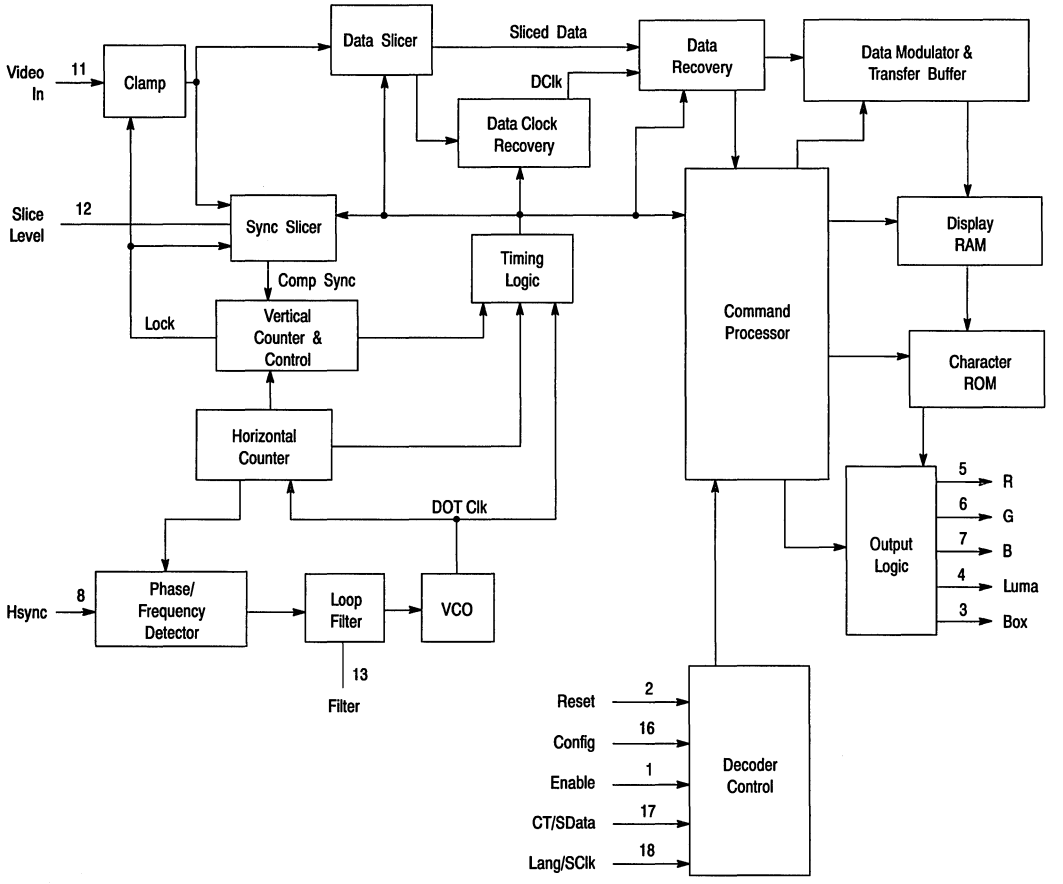


Closed-Caption Decoder

MC144143P Case 707

The MC144143 is a Line 21 closed-caption decoder for use in television receivers or set top decoders conforming to the NTSC broadcast standard. Capability for processing and displaying all of the latest standard Line 21 closed-caption format transmissions is included. The device requires a closed-caption encoded composite video signal, a horizontal sync signal, and an external keyer to produce captioned video. RGB outputs are provided, along with a luminance and a box signal, allowing simple interface to both color and black and white receivers.

- Conforms to the SCC Report and Order as Amended by the Petition for Reconsideration on Gen. Doc. 91-1
- Supports Four Different Data Channels, Time Multiplexed within the Line 21 Data Stream: Captions Utilizing Languages 1 & 2, Plus Text Utilizing Languages 1 & 2
- Output Logic Provides Hardware Underline Control and Italics Slant Generation
- Single Supply Operating Voltage Range: 4.75 to 5.25 V
- Composite Video Input Range: 0.7 to 1.4 Vp-p
- Horizontal Sync Input Polarity can be either Positive or Negative
- Internal Timing/Sync Signals Derived from On-Chip VCO

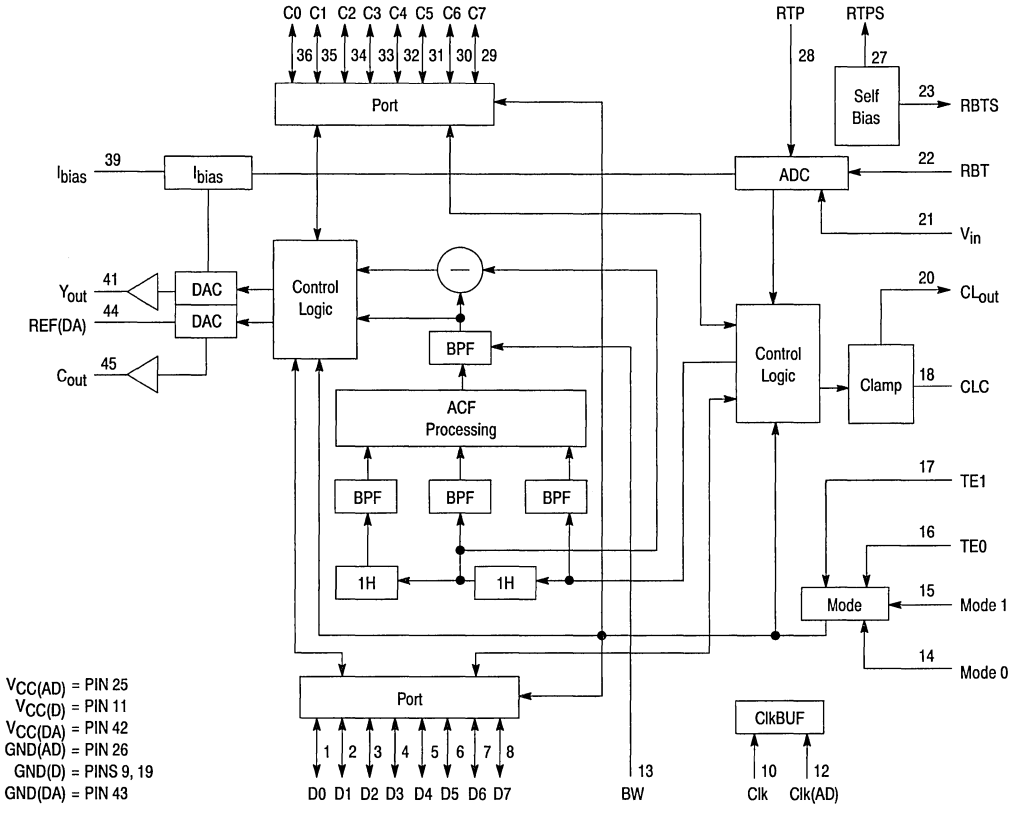


Advanced NTSC Comb Filter

MC141621FB Case 898

The MC141621 is an advanced NTSC comb filter for VCR and TV applications. It separates the luminance (Y) and chrominance (C) signals from the NTSC composite video signal by using digital signal processing techniques. This filter allows a video signal input of an extended frequency bandwidth by using a 4.0 F_{SC} clock. In addition, the filter minimizes dot crawl and cross color effects. The built-in A/D and D/A converters allow easy connections to analog video circuits.

- Built-in High Speed 8-Bit A/D Converter
- Two Line Memories (1820 Bytes)
- Advanced Combing Process
- Two 8-Bit D/A Converters
- Built-in Clamp Circuit
- On-Chip Reference Voltage Regulator for ADC
- Digital Interface Mode

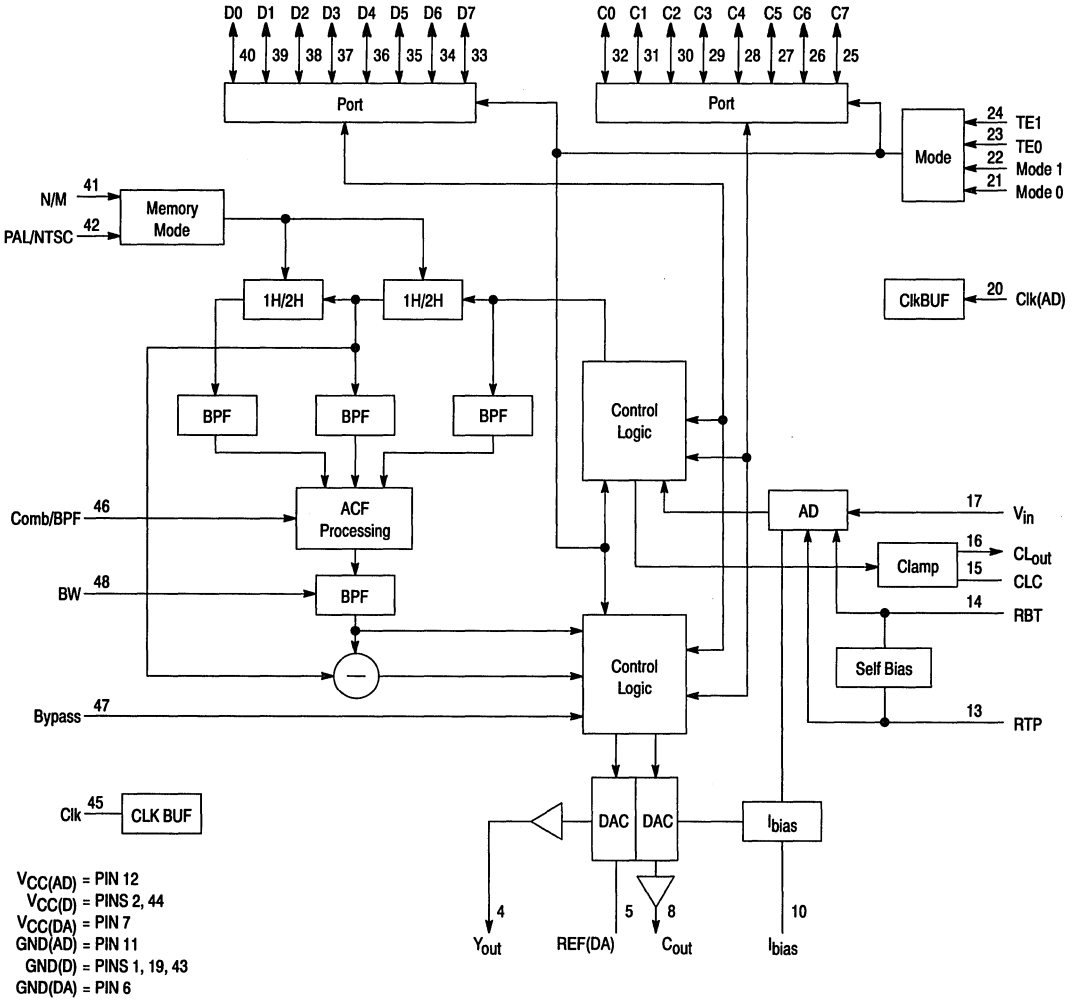


Advanced PAL/NTSC Comb Filter

MC141625AFB, FB Case 898

The MC141625 is an advanced PAL/NTSC comb filter for VCR and TV applications. It separates the luminance (Y) and chrominance (C) signals from the PAL or NTSC composite video signal by using digital signal processing techniques. This filter allows a video signal input of an extended frequency bandwidth and minimizes dot crawl and cross color effects. The built-in A/D and D/A converters allow easy connections to analog video circuits.

- Fast 8-Bit A/D Converter
- Four Line Memories (4540 Bytes)
- Advanced Combing Process
- Two 8-Bit D/A Converters
- Built-in Clamp Circuit
- On-Chip Reference Voltage Regulator for ADC
- Digital Interface Mode
- PAL/NTSC Mode



Dual Video Amplifiers

MC14576B/77BF, P Case 626, 904

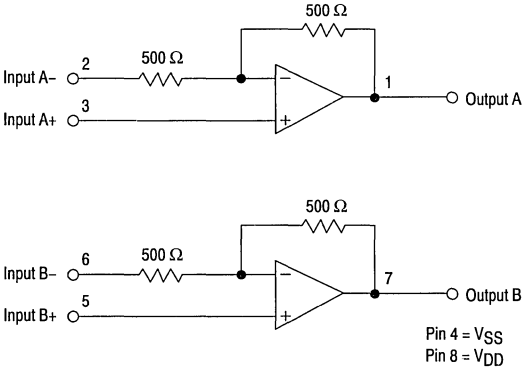
The MC14576B/77B devices each contain two amplifiers manufactured in CMOS process. Each amplifier also employs two lateral NPN bipolar transistors.

The MC14576B contains two internally compensated operational amplifiers. On-chip gain setting resistors result in a noninverting voltage gain of 6.0 dB, ±1.0 dB at 4.43 MHz for each amp. Each noninverting input of the MC14576B appears as mostly a capacitive load of approximately 10 pF.

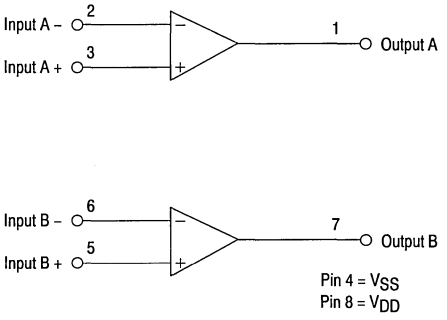
The MC14577B also contains two internally compensated operational amplifiers. However, the gain for each amplifier is adjustable with external components. All inputs of the MC14577B appear mostly as capacitive loads of approximately 10 pF.

- Direct Drive of 150 Ω Loads
- May Be Used with Single or Dual Supplies
- Guaranteed Bandwidth of 10 MHz

MC14576B



MC14577B



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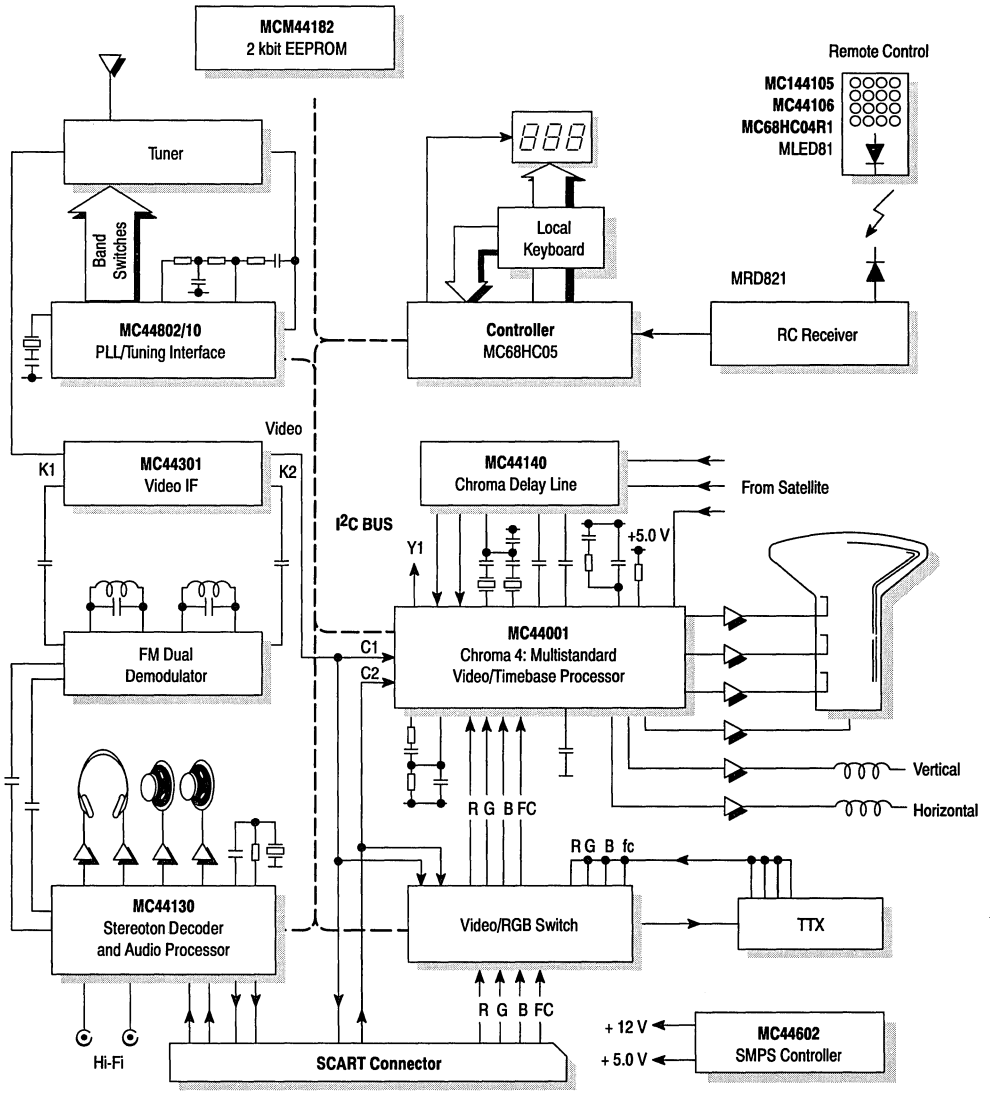
Chroma 4 Family Block Diagram



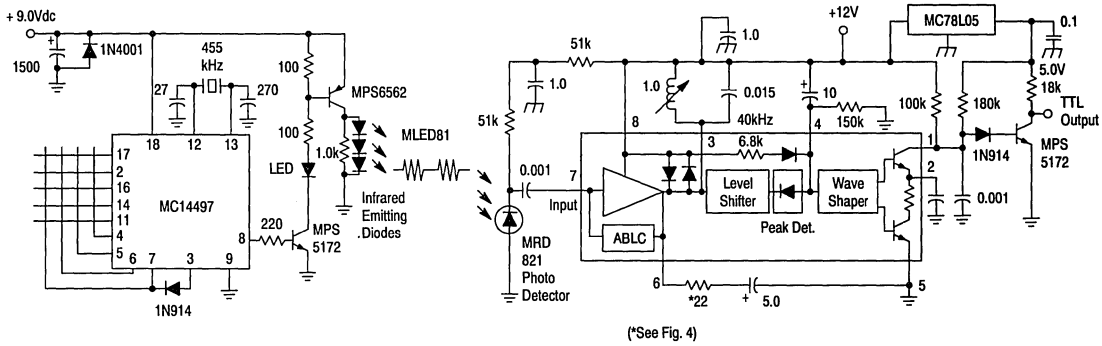
Remote Control Circuits

MC3373P Amplifier/Detector (Bipolar) Case 626

MC14497 Transmitter (CMOS) Case 707

The MC3373 remote control receiver is specifically designed for infrared link systems where high sensitivity and good noise immunity are critical. The MC3373 incorporates a high gain detector diode preamp driving an envelope detector and data wave shaper for accurate data recovery. Provision is also made to use an external L-C tank circuit at the carrier frequency, normally 30 to 60 kHz, for extended range low noise systems. Applications include TV remote control, short range data links (up to several hundred feet), door openers and security systems. The MC14497 is an ideal companion transmitter, where a simple DTMF like key-pad control is desired. The Motorola Discrete Opto Division also has several high sensitivity detectors and emitters which match up well to the MC3373 system.

Remote Control Application
40 kHz Carrier



CMOS Remote Control Functions

Function	Number of Address Lines	Maximum Number of Address Codes	Number of Data Bits	Operation	Device	Suffix/Case
Addressable UART	7	128	7/8	Full-Duplex	MC14469	P/711, FN/777
Transmitter	0	0	6	Simplex	MC14497	P/707
Encoder	Depends on Decoder(1)	Depends on Decoder(1)	Depends on Decoder(1)	Simplex	MC145026	P/648, D/751B
Decoder	5	243	4	Simplex	MC145027	P/648, DW/751G
	9	19,683	0	Simplex	MC145028	
Encoder/Decoder	9	512	0	Half-Duplex	MC145030	P/738, DW/751D
	15	32,768	0	Half-Duplex	MC145033	DW/751F
Encoder	13 or 17	131,072	4	Simplex	MC145034	
Decoder	13 or 17	131,072	4	Simplex	MC145035	

(1)See MC145027, MC145028

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Entertainment Radio Receiver Circuits

Video Circuits

Remote Control Circuit

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

CA3054

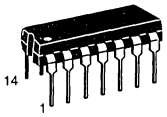
DUAL DIFFERENTIAL AMPLIFIER

Dual Independent Differential Amplifier

The CA3054 consists of two independent differential amplifiers with associated constant-current transistors on a common monolithic substrate. The six NPN transistors which comprise the amplifiers are general purpose devices useful from DC to 120 MHz.

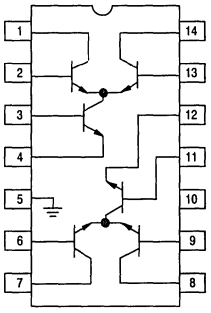
The monolithic construction of the CA3054 provides close electrical and thermal matching of the amplifiers which makes this device particularly useful in dual channel applications where matched performance of the two channels is required.

- Two Differential Amplifiers on a Common Substrate
- Independently Accessible Inputs and Outputs
- Maximum Input Offset Voltage: ±5.0 mV



P SUFFIX
PLASTIC PACKAGE
CASE 646

PIN CONNECTIONS



Pin 5 is connected to substrate and must remain at the lowest circuit potential

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage Collector-Base Voltage Emitter-Base Voltage	V_{CEO} V_{CBO} V_{EBO}	15 20 5.0	Vdc
Collector-Substrate Voltage	V_{CIO}	20	Vdc
Collector Current — Continuous	I_C	50	mAdc
Junction Temperature	T_J	150	°C
Operating Ambient Temperature Range	T_A	–40 to +85	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

ELECTRICAL CHARACTERICISTICS (T_A = 25°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
STATIC CHARACTERISTICS (For Each Differential Amplifier)					
Input Offset Voltage (V_{CB} = 3.0 Vdc)	V_{IO}	—	—	5.0	mV
Input Offset Current (V_{CB} = 3.0 Vdc)	I_{IO}	—	—	2.0	µA
Input Bias Current (V_{CB} = 3.0 Vdc)	I_{IB}	—	—	24	µA
STATIC CHARACTERISTICS (For Each Transistor)					
Base-Emitter Voltage	V_{BE}				Vdc
(V_{CB} = 3.0 Vdc, I_C = 50 µA)		—	—	0.70	
(V_{CB} = 3.0 Vdc, I_C = 1.0 mA)		—	—	0.80	
(V_{CB} = 3.0 Vdc, I_C = 3.0 mA)		—	—	0.85	
(V_{CB} = 3.0 Vdc, I_C = 10 mA)		—	—	0.90	
Collector Cutoff Current (V_{CB} = 10 Vdc, I_E = 0)	I_{CBO}	—	—	100	nA
Collector-Emitter Breakdown Voltage (I_C = 1.0 mA)	$V_{(BR)CEO}$	15	—	—	Vdc
Collector-Base Breakdown Voltage (I_C = 10 µA)	$V_{(BR)CBO}$	20	—	—	
Collector-Substrate Breakdown Voltage (I_C = 10 µA)	$V_{(BR)CIO}$	20	—	—	
Emitter-Base Breakdown Voltage (I_E = 10 µA)	$V_{(BR)EBO}$	5.0	—	—	

9

CA3146

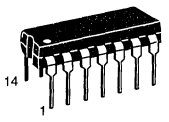
General Purpose Transistor Array
One Differentially Connected Pair and Three Isolated Transistor Arrays

GENERAL PURPOSE TRANSISTOR ARRAY

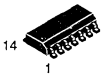
SILICON MONOLITHIC INTEGRATED CIRCUIT

The CA3146 is designed for general purpose, low power applications in the DC through VHF range.

- Guaranteed Base-Emitter Voltage Matching
- Operating Current Range Specified: 10 μA to 10 mA
- Five General Purpose Transistors in One Package



P SUFFIX
PLASTIC PACKAGE
CASE 646



D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO-14)

MAXIMUM RATINGS

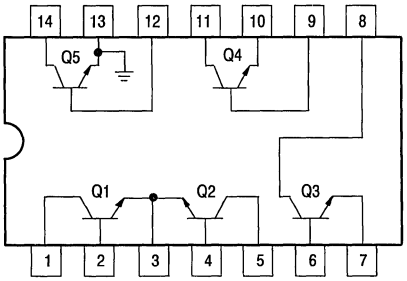
Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	130	Vdc
Collector-Base Voltage	V_{CBO}	20	Vdc
Collector-Substrate Voltage	V_{CIO}	20	Vdc
Emitter-Base Voltage	V_{EBO}	5.0	Vdc
Collector Current	I_C	50	mAdc
Operating Temperature Range	T_A	–40 to +85	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

ORDERING INFORMATION

Device	Temperature Range	Package
CA3146D	–40° to +85°C	SO-14
CA3146P		Plastic DIP

9

PIN CONNECTIONS



Pin 13 is connected to substrate and must remain at the lowest circuit potential.

ELECTRICAL CHARACTERICISTICS

Characteristics	Symbol	Min	Typ	Max	Unit
STATIC CHARACTERISTICS					
Collector-Base Breakdown Voltage (I_C = 10 μAdc)	$V_{(BR)CBO}$	40	89	—	Vdc
Collector-Emitter Breakdown Voltage (I_C = 1.0 mAdc)	$V_{(BR)CEO}$	35	45	—	Vdc
Collector-Substrate Breakdown Voltage (I_{CI} = 10 μA)	$V_{(BR)CIO}$	40	85	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 μA)	$V_{(BR)EBO}$	5.0	—	—	Vdc
Collector-Base Cutoff Current (V_{CB} = 10 Vdc, I_E = 0)	I_{CBO}	—	0.68	40	nAdc
DC Current Gain (I_C = 10 mAdc, V_{CE} = 5.0 Vdc) (I_C = 1.0 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	 — —	 171 188	 — —	—
Base-Emitter Voltage (V_{CE} = 5.0 Vdc, I_E = 1.0 mAdc)	V_{BE}	—	0.7	—	Vdc
Collector-Emitter Saturation Voltage (I_C = 10 mA, I_B = 0.4 mA)	$V_{CE(sat)}$	—	0.28	0.5	Vdc
Magnitude of Input Offset Current $\lvert I_{IO1} - I_{IO2} \rvert$ (V_{CE} = 5.0 Vdc, $I_{C1} = I_{C2}$ = 1.0 mAdc)	I_{IO}	—	0.03	2.0	μAdc
Magnitude of Input Offset Voltage $\lvert V_{BE1} = V_{BE2} \rvert$ (V_{CE} = 5.0 Vdc, I_E = 1.0 mAdc)	$\lvert V_{IO} \rvert$	—	0.13	2.0	mVdc
DYNAMIC CHARACTERICISTICS					
Low Frequency Noise Figure (V_{CE} = 5.0 Vdc, I_C = 100 μAdc, R_S = 1.0 kΩ, f = 1.0 kHz)	NF	—	3.25	—	dB
Forward Current Transfer Ratio (V_{CE} = 5.0 Vdc, I_C = 1.0 mAdc, f = 1.0 kHz)	h_{fe}	—	201.5	—	—
Short Circuit Input Impedance (V_{CE} = 5.0 Vdc, I_C = 1.0 mAdc, f = 1.0 kHz)	h_{ie}	—	6.7	—	kΩ
Open Circuit Output Impedance (V_{CE} = 5.0 Vdc, I_C = 1.0 mAdc, f = 1.0 kHz)	h_{oe}	—	15.6	—	μmho
Reverse Voltage Transfer Ratio (V_{CE} = 5.0 Vdc, I_C = 1.0 mAdc, f = 1.0 kHz)	h_{re}	—	3.5	—	$X10^{-4}$
Input Admittance (V_{CE} = 5.0 Vdc, I_C = 1.0 mAdc, f = 1.0 kHz)	Y_{ie}	—	0.14 + j0.16	—	mmho
Forward Transfer Admittance (V_{CE} = 5.0 Vdc, I_C = 1.0 mAdc, f = 1.0 kHz)	Y_{fe}	—	34.6 – j0.63	—	mmho
Reverse Transfer Admittance (V_{CE} = 5.0 Vdc, I_C = 1.0 mAdc, f = 1.0 kHz)	Y_{re}	—	62.0 – j59.4	—	μmho
Output Admittance (V_{CE} = 5.0 Vdc, I_C = 1.0 mAdc, f = 1.0 kHz)	Y_{oe}	—	0.16 + j0.14	—	mmho
Current-Gain — Bandwidth Product (V_{CE} = 5.0 Vdc, I_C = 3.0 mAdc)	f_T	300	500	—	MHz
Emitter-Base Capacitance (V_{EB} = 5.0 Vdc, I_E = 0 mAdc)	C_{EB}	—	1.17	—	pF
Collector-Base Capacitance (V_{CB} = 5.0 Vdc, I_E = 0 mAdc)	C_{CB}	—	0.68	—	pF
Collector-Substrate Capacitance (V_{CS} = 5.0 Vdc, I_C = 0 mAdc)	C_{CI}	—	1.92	—	pF

MC1330A

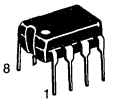
Low-Level Video Detector

The MC1330A is an integrated circuit featuring very linear video characteristics and wide bandwidth. Designed for color and monochrome television receivers, replacing the third IF, detector, video buffer and AFC buffer.

- Conversion Gain: 33 dB (Typ)
- Excellent Differential Phase and Gain
- High Rejection of IF Carrier Feedthrough
- High Video Output: 8.0 V(p-p)
- Fully Balanced Detector
- Output Temperature Compensated
- Improved Version of the MC1330

LOW-LEVEL VIDEO DETECTOR

SILICON MONOLITHIC INTEGRATED CIRCUIT

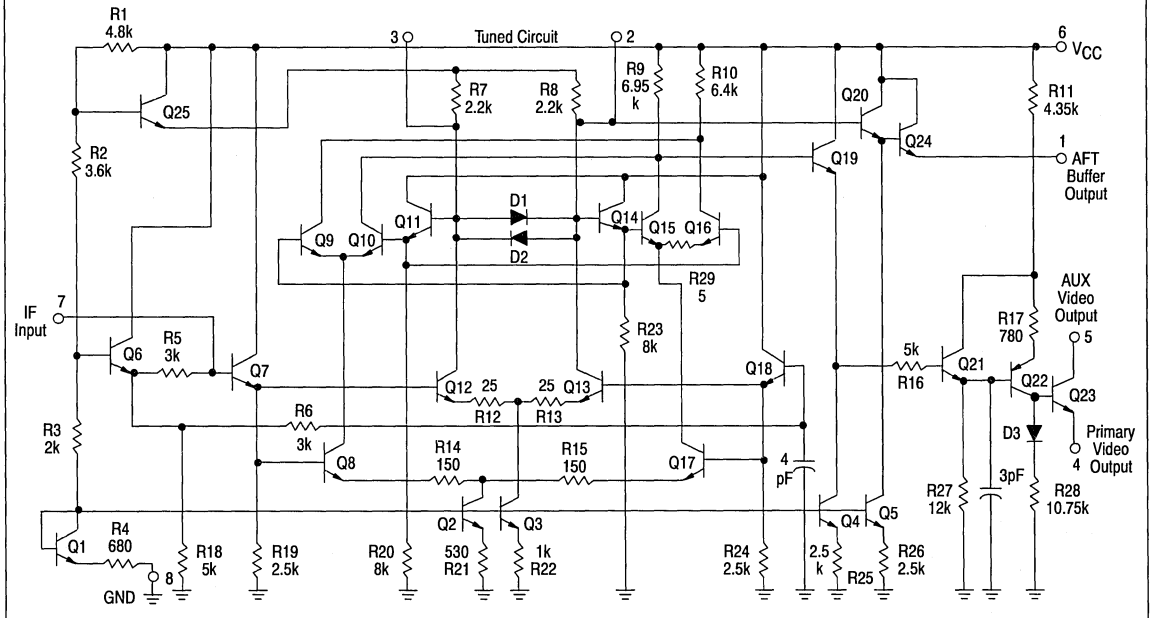


P SUFFIX
PLASTIC PACKAGE
CASE 626

MAXIMUM RATINGS

Rating	Value	Unit
Power Supply Voltage	24	Vdc
DC Video Output Current DC AFT Output Current	5.0 2.0	mAdc
Junction Temperature	150	°C
Operating Ambient Temperature Range	0 to 75	°C
Storage Temperature Range	–65 to +150	°C

Figure 1. Circuit Schematic



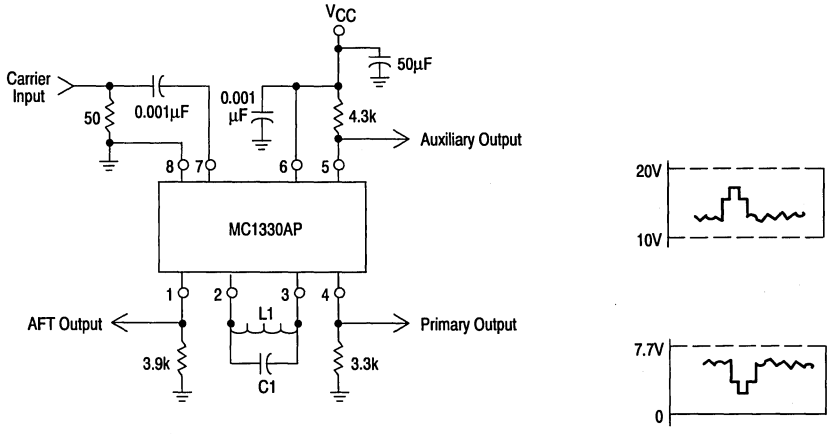
ELECTRICAL CHARACTERICISTICS (V_{CC} = +20 Vdc, Q = 40, f_c = 45.75 MHz, T_A = +25°C, unless otherwise noted.)

Characteristics	Pin	Min	Typ	Max	Unit
Zero Signal DC Output Voltage	4	7.0	—	8.7	Vdc
Supply Current	5, 6	11	17.5	24	mA
Maximum Signal DC Output Voltage	4	—	0	0.5	Vdc
Conversion Gain for 1.0 Vp-p Output (30% Modulation)	7	25	36	65	mVrms
AFT Buffer Output at Carrier Frequency	1	300	475	650	mVp-p

DESIGN CHARACTERISTICS (V_{CC} = +20 Vdc, Q = 40, f_c = 45.75 MHz, T_A = +25°C, unless otherwise noted.)

Characteristics		Pin	Typ	Unit
Input Resistance Input Capacitance		7 7	4.9 1.5	kΩ pF
Internal Resistance (Across Tuned Circuit) Internal Capacitance (Across Tuned Circuit)		2, 3 2, 3	4.4 1.0	kΩ pF
Negative Video Output Bandwidth (Figure10) Positive Video Output Bandwidth (Figure10)		4 5	10.8 2.2	MHz MHz
Differential Phase @ 3.58 MHz, 100% Modulated Staircase, 3.0 Vp-p Detected Video Pin 5 Tied to Pin 6 Differential Gain @ 3.58 MHz, 100% Modulated Staircase, 3.0 Vp-p Detected Video Pin 5 Tied to Pin 6		4 4	7.0 4.0	Degrees %
Differential Phase @ 3.58 MHz, 100% Modulated Staircase, 3.0 Vp-p Detected Video, R Pin 5 = 4.3 kΩ Differential Gain @ 3.58 MHz, 100% Modulated Staircase, 3.0 Vp-p Detected Video, R Pin 5 = 4.3 kΩ		4 4	8.0 6.0	Degrees %
920 kHz Beat Output (dB Below 100% Modulated Video, see Figure 11) 45.75 MHz = Reference 42.17 MHz = –6.0 dB 41.25 MHz = –20 dB		4	–38	dB
Video Output Resistance @ 1.0 MHz, 2.0 mA		4	94	Ω
Input Overload (Carrier Level at Input to Pin 4, Primary Output to go Positive 0.1 Vdc from Ground.)	V_{CC} = 12 Vdc V_{CC} = 15 Vdc V_{CC} = 20 Vdc V_{CC} = 24 Vdc	7	2.0 2.6 3.6 4.6	V
Power Supply Voltage Range		5	10 to 24	V

Figure 2. Test Fixture Circuit



L1, C1: See General Information Number 3, page 5 of this specification.

Figure 3. Input Admittance

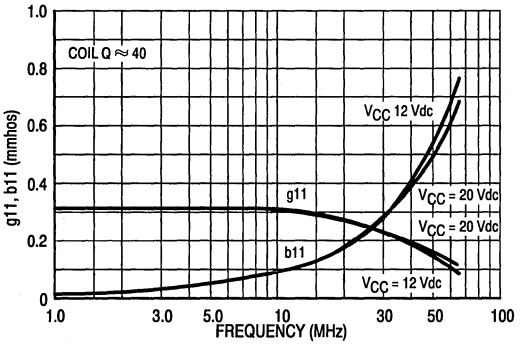
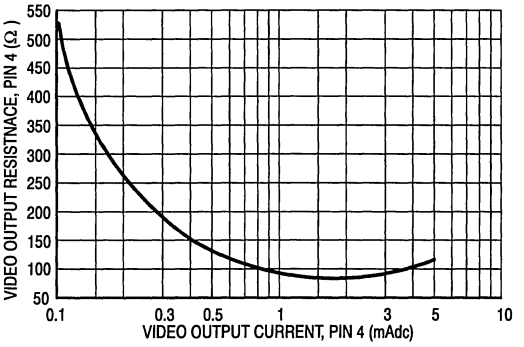


Figure 4. Video Detector Output Resistance



CIRCUIT DESCRIPTION

The MC1330A video detector is a fully balanced multiplier detector circuit that has linear amplitude and phase characteristics. The signal is divided into two channels, one a linear amplifier and the other a limiting amplifier that provides the switching carrier for the detector.

The switching carrier has a buffered output for use in providing the AFT function.

The video amplifier output is an improved design that reduces the differential gain and phase distortion associated with previous video output systems. The output is wideband, > 8.0 MHz, with normal negative polarity.

A separate narrow bandwidth, positive video output is also provided.

Figure 5. Differential Phase and Gain Test Set Up

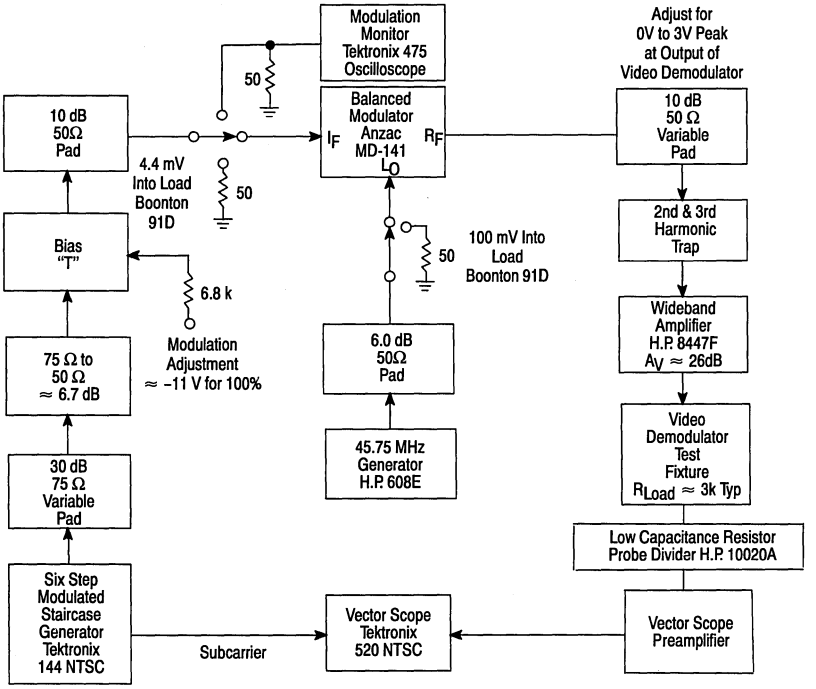


Figure 6. Output Voltage Transfer Function

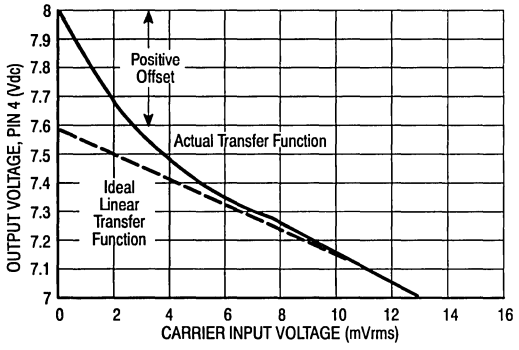


Figure 7. Output Voltage Transfer Function

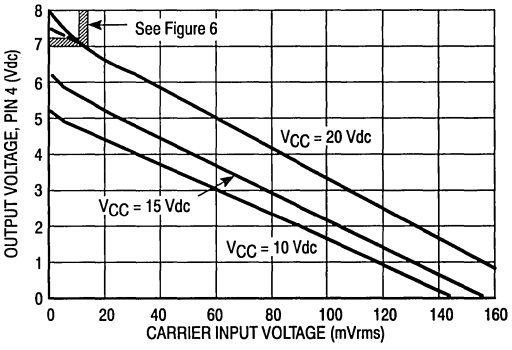


Figure 8. Output Voltage, Supply Current

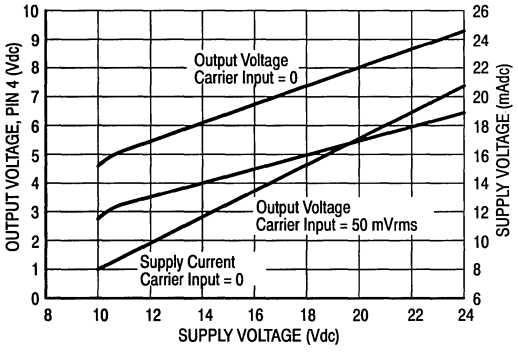


Figure 9. AFT Limiting

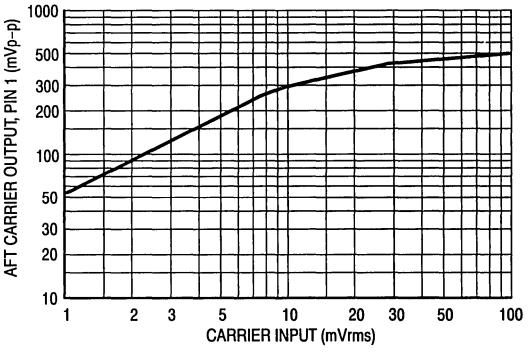


Figure 10. Video Output Response

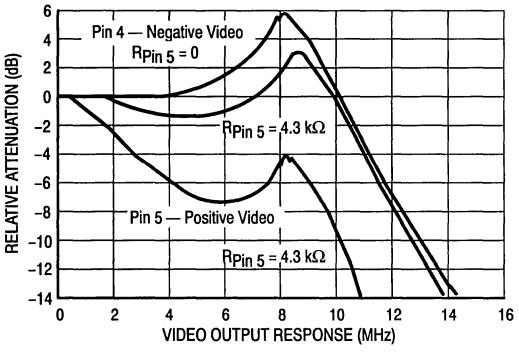
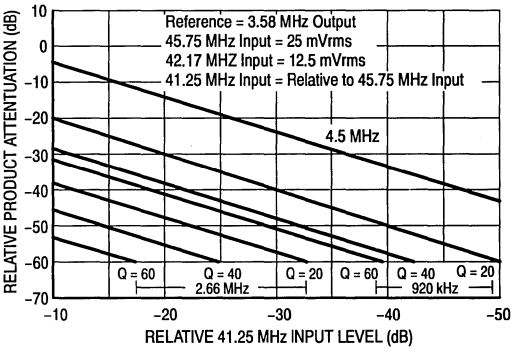


Figure 11. Video Output Products



GENERAL INFORMATION

The MC1330A offers the designer a new approach to an old problem. Now linear detection can be performed at much lower power signal levels than possible with a detector diode.

Offering a number of distinct advantages, its easy implementation should meet with ready acceptance for television designs. Some specific features and information on systems design with this device are given below:

1. The device provides excellent linearity of output versus input, as shown in Figures 6 and 7. These graphs also show that video peak-to-peak amplitude (AC) does not change with supply voltage variation. (Slopes are parallel. Visualize a given variation of input CW and use the figure as a transfer function.)

2. The DC output level does change linearly with supply voltage shown if Figure 8. This can be accommodated by regulating the supply or by referencing the subsequent video amplifier to the same power supply.

3. The choice of Q for the tuned circuit of Pin 2 and 3 is not critical. The higher the Q, the better the rejection of 920 kHz products by the more critical the tuning accuracy required (see Figure 11). Values of Q from 20 to 50 are recommended. (Note the internal resistance.)

4. A video output with positive-going sync is available at Pin 5 if required. This signal has a higher output impedance than Pin 4 so it must be handled with greater care. If not used, Pin 5 may be connected directly to the supply voltage (Pin 6). The video response will be altered somewhat (see Figure 10).

5. An AFT output (Pin 1) provides 460 mV of IF carrier output, sufficient voltage to drive an AFT ratio detector, with only one additional stage.

6. AGC lockout can occur if the input signal presented in the MC1330A is greater than that shown in the input overload section of the design characteristics shown on Page 3. If these values are exceeded, the turns ratio between the primary and secondary of T_1 should be increased. Another solution to the problem is to use an input clamp diode D_1 shown if Figure 14.

7. The total I.F. noise figure at high gain reductions can be improved by reflecting ≈ 1.0 k source impedance to the input of the MC1330A. This will cause some loss in overall IF voltage gain.

TV-IF AMPLIFIER INFORMATION

A very compact high performance IF amplifier constructed as shown in Figure 14 minimizes the number of overall components and alignment adjustments. It can be readily combined with normal tuners and input tuning-trapping circuitry to provide the performance demanded of high quality receivers. This configuration will provide approximately 93 dB voltage gain and can accommodate the usual low impedance input network or, if desired, can take advantage of an impedance step-up from tuner to MC1350 input.

The burden of selectivity, formerly found between the third IF and detector, must now be placed at the interstage. The nominal 3.0 V peak-to-peak output can be varied from 0 V to 7.0 V with excellent linearity and freedom from spurious output products.

Alignment is most easily accomplished with an AM generator, set at a carrier frequency of 45.75 MHz, modulated with a video frequency sweep. This provides the proper realistic conditions necessary to operate to low-level detector (LLD). The detector tank is first adjusted for maximum detected DC (with a CW input). Next, the video sweep modulation is applied and the interstage and input circuits aligned, step by step, as in a standard IF amplifier.

Note: A normal IF sweep generator, essentially an FM generator, will not serve properly without modification. The LLD tank attempts to "follow" the sweep input frequency, and results in variations of switching amplitude in the detector. Hence, the apparent overall response becomes modified by the response of the LLD tank, which a real signal doesn't do.

This effect can be prevented by resistively adding a 45.75 MHz CW signal to the output of the sweep generator approximately 3.0 dB greater than the sweep amplitude. See Figures 12 and 13 below. For a more detailed description of the MC1330A see application note AN545A.

Figure 12. Band Pass Displayed by Conventional Sweep

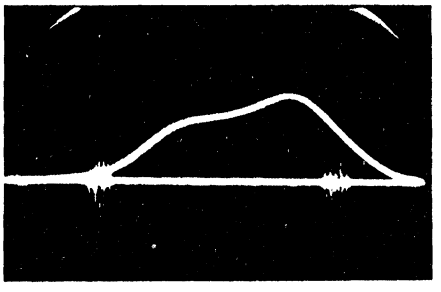


Figure 13. Band Pass Display with the Addition of Carrier Injection

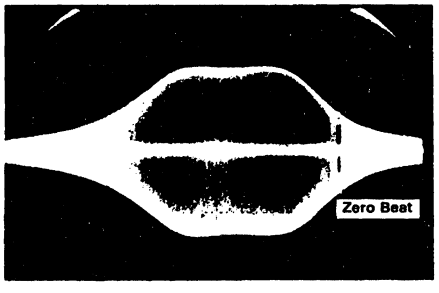
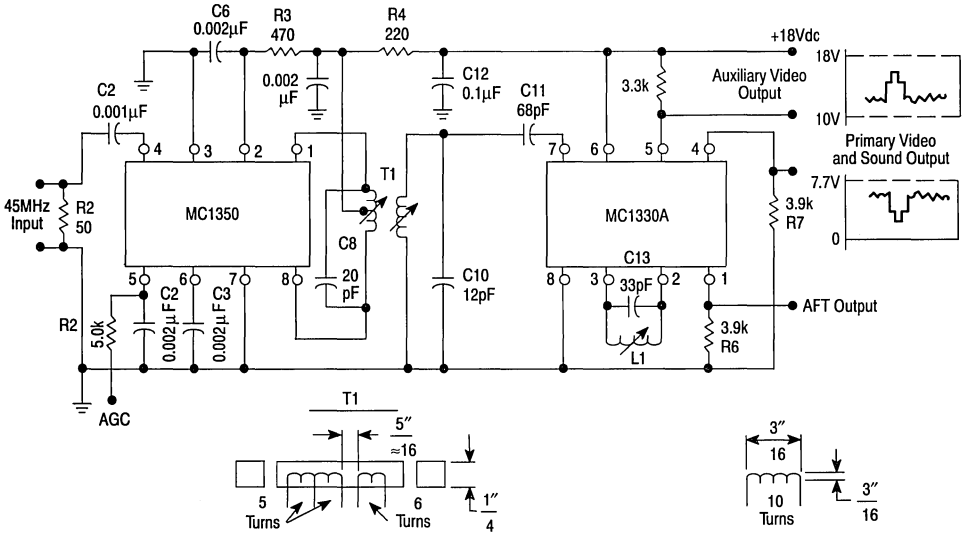


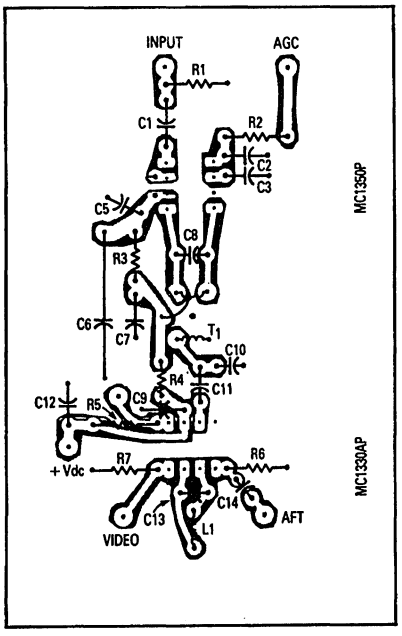
Figure 14. Typical Application of MC1350P Video if Amplifier and MC1330A Low-Level Video Detector Circuit



All windings #30 AWG tinned nylon acetate wire tuned with Carbonyl E or J slugs.

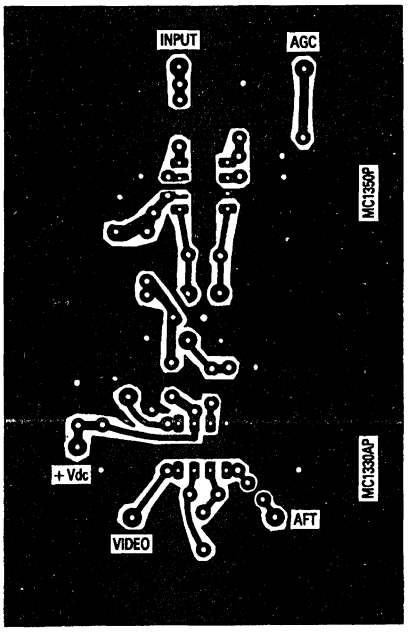
L1 wound with #26 AWG tinned nylon acetate wire tuned by distorting winding.

Figure 15. Printed Circuit Board (Parts Layout)



COPPER SIDE UP

Figure 16. Printed Circuit (Board Layout)



COPPER SIDE UP

9

MC1350

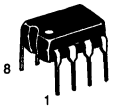
IF AMPLIFIER

SILICON MONOLITHIC
INTEGRATED CIRCUIT

Monolithic IF Amplifier

The MC1350 is an integrated circuit featuring wide range AGC for use as an IF amplifier in radio and TV over an operating temperature range of 0° to +75°C.

- Power Gain: 50 dB Typ at 45 MHZ
  50 dB Typ at 58 MHZ
- AGC Range: 60 dB Min, DC to 45 MHz
- Nearly Constant Input & Output Admittance over the Entire AGC Range
- Y_{21} Constant (–3.0 dB) to 90 MHz
- Low Reverse Transfer Admittance: < < 1.0 μmho Typ
- 12 V Operation, Single-Polarity Power Supply



P SUFFIX
PLASTIC PACKAGE
CASE 626

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO-8)

MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V+	+18	Vdc
Output Supply Voltage	V_1, V_8	+18	Vdc
AGC Supply Voltage	V_{AGC}	V+	Vdc
Differential Input Voltage	V_{in}	5.0	Vdc
Power Dissipation (Package Limitation) Plastic Package Derate above 25°C	P_D	 625 5.0	 mW mW/°C
Operating Temperature Range	T_A	0 to +75	°C

ORDERING INFORMATION

Device	Operating Temperature	Package
MC1350P	0° to +75°C	Plastic DIP
MC1350D		SO-8

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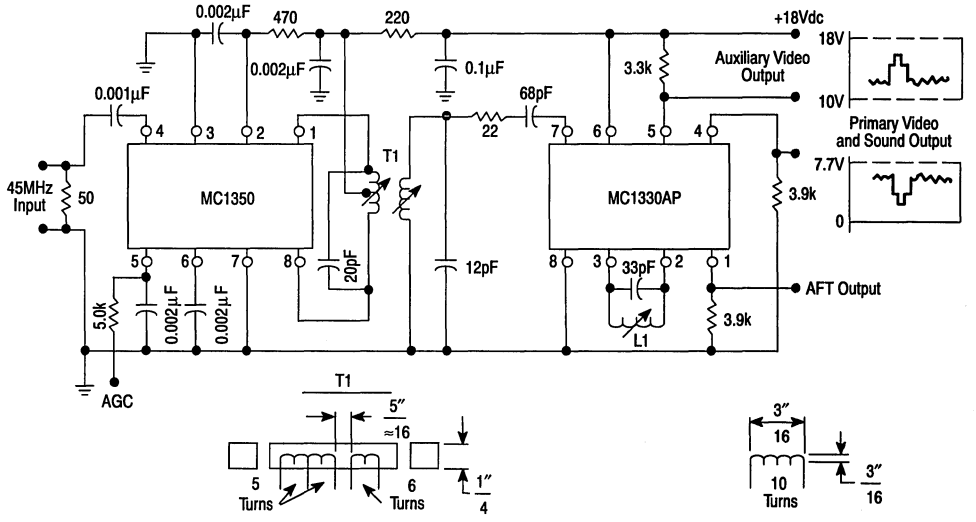
Figure 1. Typical MC1350 Video IF Amplifier and MC1330 Low-Level Video Detector Circuit



All windings #30 AWG tinned nylon acetate wire tuned with Carbonyl E or J slugs.

L1 wound with #26 AWG tinned nylon acetate wire tuned by distorting winding.

ELECTRICAL CHARACTERICISTICS (V^+ = +12 Vdc, T_A = +25°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
AGC Range, 45 MHz (5.0 V to 7.0 V) (Figure 1)		60	68	—	dB
Power Gain (Pin 5 grounded via a 5.1 kΩ resistor)	A_p				dB
f = 58 MHz, BW = 4.5 MHz See Figure 6(a)		—	48	—	
f = 45 MHz, BW = 4.5 MHz See Figure 6(a), (b)		46	50	—	
f = 10.7 MHz, BW = 350 kHz See Figure 7		—	58	—	
f = 455 kHz, BW = 20 kHz		—	62	—	
Maximum Differential Voltage Swing	V_O				V_{p-p}
0 dB AGC		—	20	—	
–30 dB AGC		—	8.0	—	
Output Stage Current (Pins 1 and 8)	$I_1 + I_8$	—	5.6	—	mA
Total Supply Current (Pins 1, 2 and 8)	I_S	—	14	17	mAdc
Power Dissipation	P_D	—	168	204	mW

DESIGN PARAMETERS, Typical Values (V^+ = +12 Vdc, T_A = +25°C, unless otherwise noted.)

Parameter	Symbol	Frequency				Unit
		455 kHz	10.7 MHz	45 MHz	58 MHz	
Single-Ended Input Admittance	g_{11}	0.31	0.36	0.39	0.5	mmho
	b_{11}	0.022	0.50	2.30	2.75	
Input Admittance Variations with AGC	Δg_{11}	—	—	60	—	µmho
(0 dB to 60 dB)	Δb_{11}	—	—	0	—	
Differential Output Admittance	g_{22}	4.0	4.4	30	60	µmho
	b_{22}	3.0	110	390	510	
Output Admittance Variations with AGC	Δg_{22}	—	—	4.0	—	µmho
(0 dB to 60 dB)	Δb_{22}	—	—	90	—	
Reverse Transfer Admittance (Magnitude)	$\lvert y_{12} \rvert$	< < 1.0	< < 1.0	< < 1.0	< < 1.0	µmho
Forward Transfer Admittance						
Magnitude	$\lvert y_{21} \rvert$	160	160	200	180	mmho
Angle (0 dB AGC)	$< y_{21}$	–5.0	–20	–80	–105	Degrees
Angle (–30 dB AGC)	$< y_{21}$	–3.0	–18	–69	–90	Degrees
Single-Ended Input Capacitance	C_{in}	7.2	7.2	7.4	7.6	pF
Differential Output Capacitance	C_O	1.2	1.2	1.3	1.6	pF

Figure 2. Typical Gain Reduction

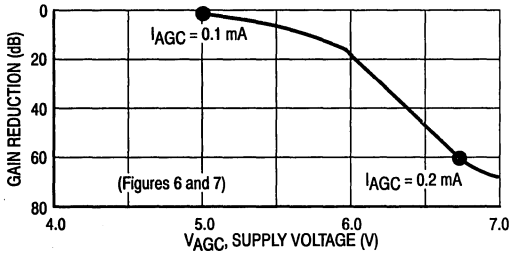
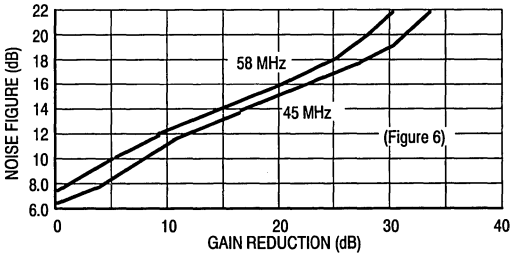


Figure 3. Noise Figure versus Gain Reduction



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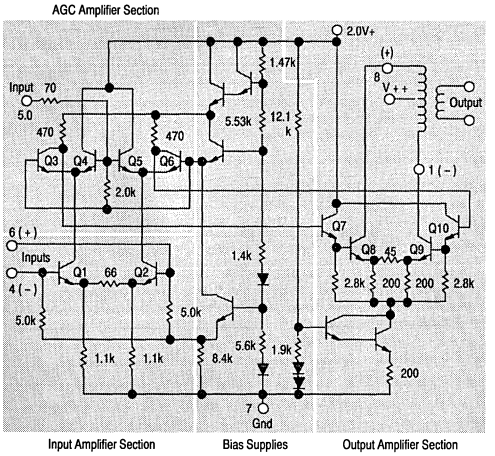
GENERAL OPERATING INFORMATION

The input amplifiers (Q1 and Q2) operate at constant emitter currents so that input impedance remains independent of AGC action. Input signals may be applied single-ended or differentially (for AC) with identical results. Terminals 4 and 6 may be driven from a transformer, but a DC path from either terminal to ground is not permitted.

Figure 4. Circuit Schematic



AGC action occurs as a result of an increasing voltage on the base of Q4 and Q5 causing these transistors to conduct more heavily thereby shunting signal current from the interstage amplifiers Q3 and Q6. The output amplifiers are supplied from an active current source to maintain constant quiescent bias thereby holding output admittance nearly constant. Collector voltage for the output amplifier must be supplied through a center-tapped tuning coil to Pins 1 and 8. The 12 V supply (V+) at Pin 2 may be used for this purpose, but output admittance remains more nearly constant if a separate 15 V supply (V+ +) is used, because the base voltage on the output amplifier varies with AGC bias.

Figure 5. Frequency Response Curve (45 MHz and 58 MHz)

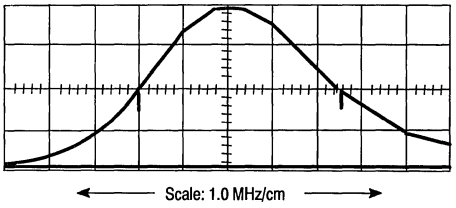
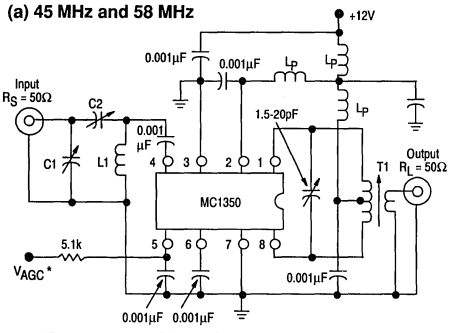


Figure 6. Power Gain, AGC and Noise Figure Test Circuits

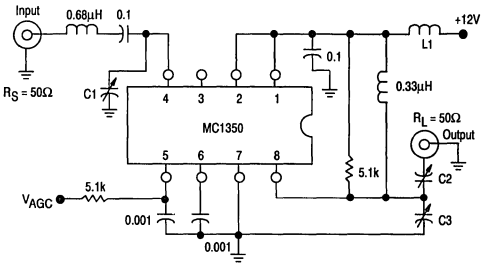
(a) 45 MHz and 58 MHz



*Connect to ground for maximum power gain test.
All power supply chokes (Lp), are self-resonant at input frequency. Lp ≥ 20 kΩ.
See Figure 5 for Frequency Response Curve.

L1 @ 45 MHz = 7 1/4 Turns on a 1/4″ coil form
@ 58 MHz = 6 Turns on a 1/4″ coil form
T1 Primary Winding = 18 Turns on a 1/4″ coil form, center-tapped, #25 AWG
Secondary Winding = 2 Turns centered over Primary Winding @ 45 MHz
= 1 Turn @ 58 MHz
Slug = Carbonyl E or J

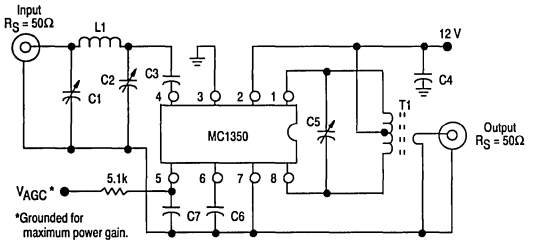
(b) Alternate 45 MHz



L1	Ferrite Core 14 Turns 28 S.W.G
C1	5–25 pF
C2	5–25 pF
C3	5–25 pF

	45 MHz		58 MHz	
L1	0.4 µH	Q ≥ 100	0.3 µH	Q ≥ 100
T1	1.3 µH to 3.4 µH	Q ≥ 100 @ 2.0 µH	1.2 µH to 3.8 µH	Q ≥ 100 @ 2.0 µH
C1	50 pF to160 pF		8.0 pF to 60 pF	
C2	8.0 pF to 60 pF		3.0 pF to 35 pF	

Figure 7. Power Gain and AGC Test Circuit (455 kHz and 10.7 MHz)



Component	Frequency	
	455 kHz	10.7 MHz
C1	'	80–450 pF
C2	—	5.0–80 pF
C3	0.05 μF	0.001 μF
C4	0.05 μF	0.05 μF
C5	0.001 μF	36 pF
C6	0.05 μF	0.05 μF
C7	0.05 μF	0.05 μF
L1	—	4.6 μF
T1	Note 1	Note 2

NOTES: 1. Primary: 120 μH (center-tapped)
Q_U = 140 at 455 kHz
Primary: Secondary turns ratio ≈ 13

2. Primary: 6.0 μH
Primary winding = 24 turns #36 AWG
(close-wound on 1/4″ dia. form)
Core = Carbonyl E or J
Secondary winding = 1-1/2 turns #36 AWG, 1/4″ dia.
(wound over center-tap)

Figure 8. Single-Ended Input Admittance

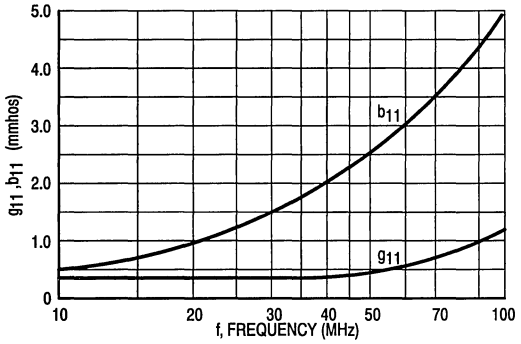


Figure 9. Forward Transfer Admittance

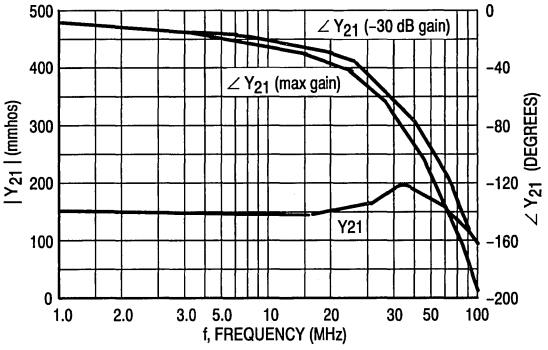


Figure 10. Differential Output Admittance

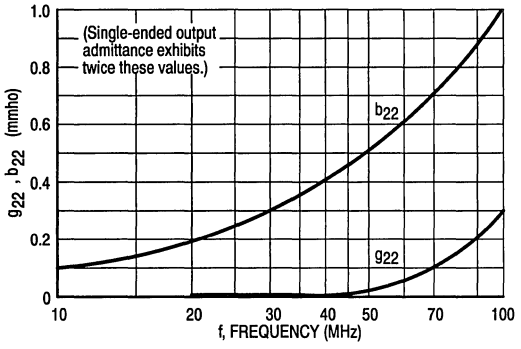
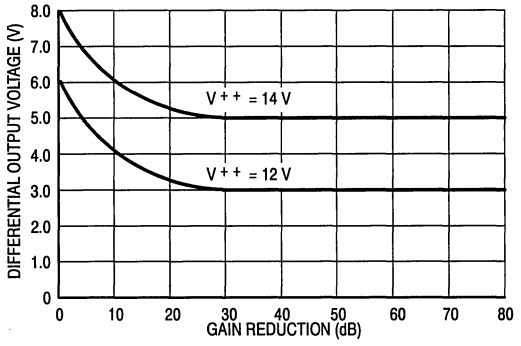


Figure 11. Differential Output Voltage



9

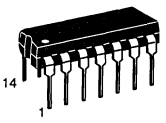
MC1357

TV Sound IF or FM IF Amplifier with Quadrature Detector

- A Direct Replacement for the ULN211A
- Greatly Simplified FM Demodulator Alignment
- Excellent Performance at V_{CC} = 8.0 Vdc

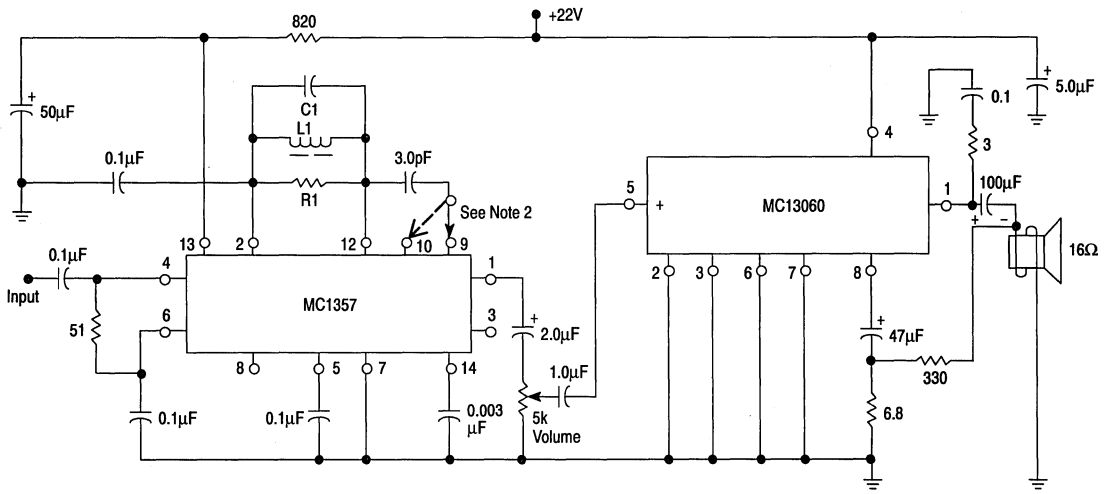
IF AMPLIFIER WITH QUADRATURE DETECTOR

SILICON MONOLITHIC INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 646

Figure 1. TV Typical Application Circuit



Typical Performance
2.0 W Output
2% Distortion
250 µV Sensitivity (3 dB Lim.)

C1 = 120 pF
L1 = 14 µH
R1 = 20 kΩ
Q = 30

MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

Rating	Value	Unit
Power Supply Voltage	16	Vdc
Input Voltage (Pin 4)	3.5	Vp
Power Dissipation (Package Limitation) Plastic Package Derate above T_A = +25°C	625 5.0	mW mW/°C
Operating Temperature Range (Ambient)	0 to +70	°C
Storage Temperature Range	−65 to +150	°C

ELECTRICAL CHARACTERICISTICS (V_{CC} = 12 Vdc, T_A = +25°C, unless otherwise noted.)

Characteristics	Pin	Min	Typ	Max	Unit
Drain Current V_{CC} = 8.0 V V_{CC} = 12 V	13	10 —	12 15	19 21	mA
Amplifier Input Reference Voltage	6	—	1.45	—	Vdc
Detector Input Reference Voltage	2	—	3.65	—	Vdc
Amplifier High Level Output Voltage	10	1.25	1.45	1.65	Vdc
Amplifier Low Level Output Voltage	9	—	0.145	0.2	Vdc
Detector Output Voltage V_{CC} = 8.0 V V_{CC} = 12 V	1	— —	3.7 5.4	— —	Vdc
Amplifier Input Resistance	4	—	5.0	—	kΩ
Amplifier Input Capacitance	4	—	11	—	pF
Detector Input Resistance	12	—	70	—	kΩ
Detector Input Capacitance	12	—	2.7	—	pF
Amplifier Output Resistance	10	—	60	—	Ω
Detector Output Resistance	1	—	200	—	Ω
De-Emphasis Resistance	14	—	8.8	—	kΩ

DYNAMIC CHARACTERICISTICS FM Modulation Frequency = 1.0 kHz, Source Resistance = 50 Ω, T_A = +25°C for all tests.

(V_{CC} = 12 Vdc, f_o = 4.5 MHz, Δf = ±25 kHz, Peak Separation = 150 kHz)

Characteristics	Pin	Min	Typ	Max	Unit
Amplifier Voltage Gain (V_{in} ≤ 50 μV[rms])	10	—	60	—	dB
AM Rejection* (V_{in} = 10 mV[rms])	1	—	36	—	dB
Input Limiting Threshold Voltage	4	—	250	—	μVrms
Recovered Audio Output Voltage (V_{in} = 10 mV[rms])	1	—	0.72	—	Vrms
Output Distortion (V_{in} = 10 mV[rms])	1	—	3.0	—	%

(V_{CC} = 12 Vdc, f_o = 5.5 MHz, Δf = ±50 kHz, Peak Separation = 260 kHz)

Amplifier Voltage Gain (V_{in} ≤ 50 μV[rms])	10	—	60	—	dB
AM Rejection* (V_{in} = 10 mV[rms])	1	—	40	—	dB
Input Limiting Threshold Voltage	4	—	250	—	μVrms
Recovered Audio Output Voltage (V_{in} = 10 mV[rms])	1	—	1.2	—	Vrms
Output Distortion (V_{in} = 10 mV[rms])	1	—	5.0	—	%

(V_{CC} = 8.0 Vdc, f_o = 10.7 MHz, Δf = ±75 kHz, Peak Separation = 550 kHz)

Amplifier Voltage Gain (V_{in} ≤ 50 μV[rms])	10	—	53	—	dB
AM Rejection* (V_{in} = 10 mV[rms])	1	—	37	—	dB
Input Limiting Threshold Voltage	4	—	600	—	μVrms
Recovered Audio Output Voltage (V_{in} = 10 mV[rms])	1	—	0.3	—	Vrms
Output Distortion (V_{in} = 10 mV[rms])	1	—	1.4	—	%

(V_{CC} = 12 Vdc, f_o = 10.7 MHz, Δf = ±75 kHz, Peak Separation = 550 kHz)

Amplifier Voltage Gain (V_{in} ≤ 50 μV[rms])	10	—	53	—	dB
AM Rejection* (V_{in} = 10 mV[rms])	1	—	45	—	dB
Input Limiting Threshold Voltage	4	—	600	—	μVrms
Recovered Audio Output Voltage (V_{in} = 10 mV[rms])	1	—	0.48	—	Vrms
Output Distortion (V_{in} = 10 mV[rms])	1	—	1.4	—	%

NOTE: *100% FM, 30% AM Modulation

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TYPICAL CHARACTERISITICS

(V_{CC} = 12 V, T_A = +25°C, unless otherwise noted.)
(Use Test Circuit of Figure 13)

Figure 2. AM Rejection

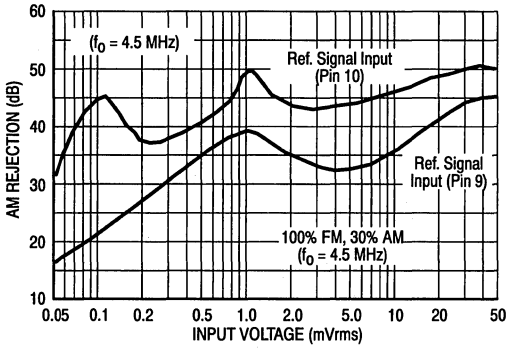


Figure 3. AM Rejection

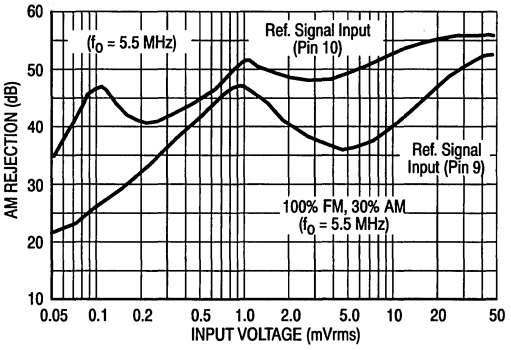


Figure 4. Detected Audio Output

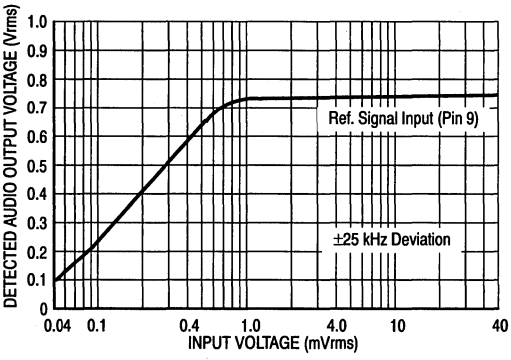


Figure 5. Detected Audio Output

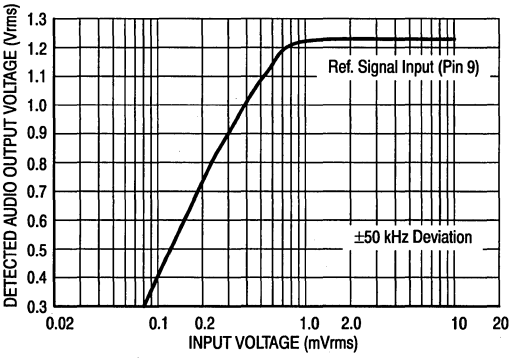


Figure 6. Detector Transfer Characteristic

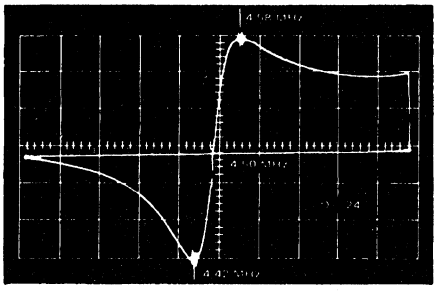
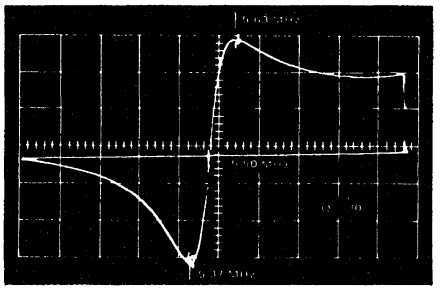


Figure 7. Detector Transfer Characteristic



TYPICAL CHARACTERISITICS (continued)
(f_o = 10.7 MHz, T_A = +25°C, unless otherwise noted.)
(Use Test Circuit of Figure 13)

Figure 8. AM Rejection

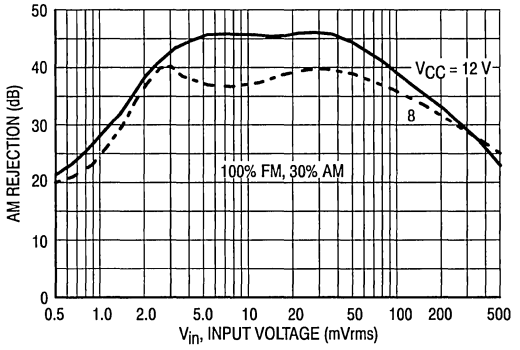


Figure 9. AFC Voltage Drift

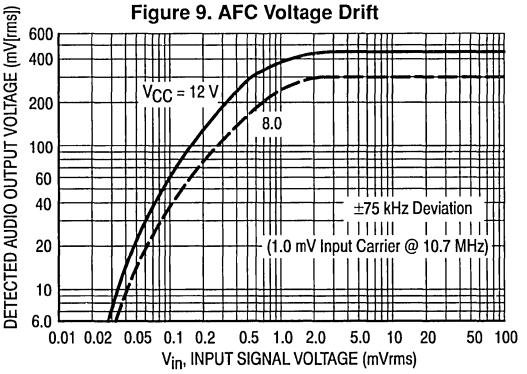


Figure 10. Limiting

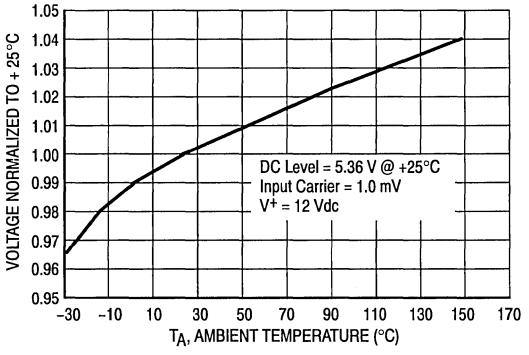


Figure 11. Signal-to-Noise Ratio

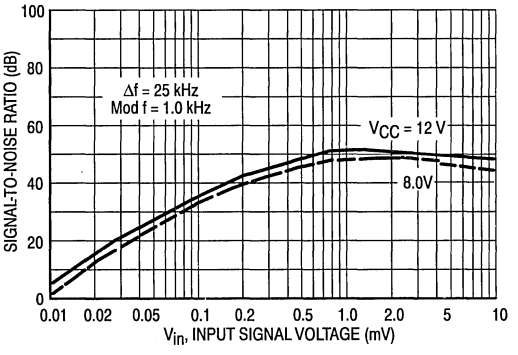


Figure 12. Detector Transfer Characteristic

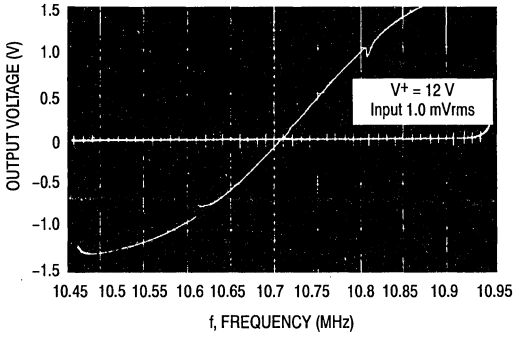
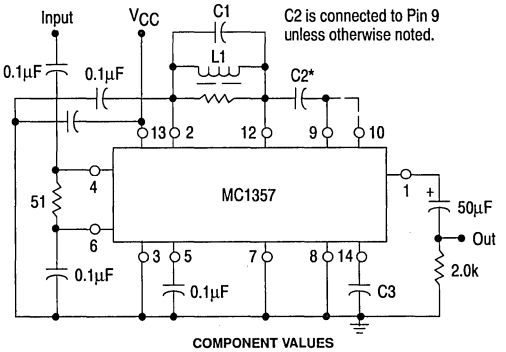


Figure 13. Test Circuit



COMPONENT VALUES

f	L1	C1	R1	Q(R1,L1)	C2	C3
MHz	µH	pF	kΩ		pF	µF
4.5	14	120	20	30	3.0	0.003
5.5	8.0	100	20	30	3.0	0.003
10.7	2.0	120	3.9	20	4.7	0.01

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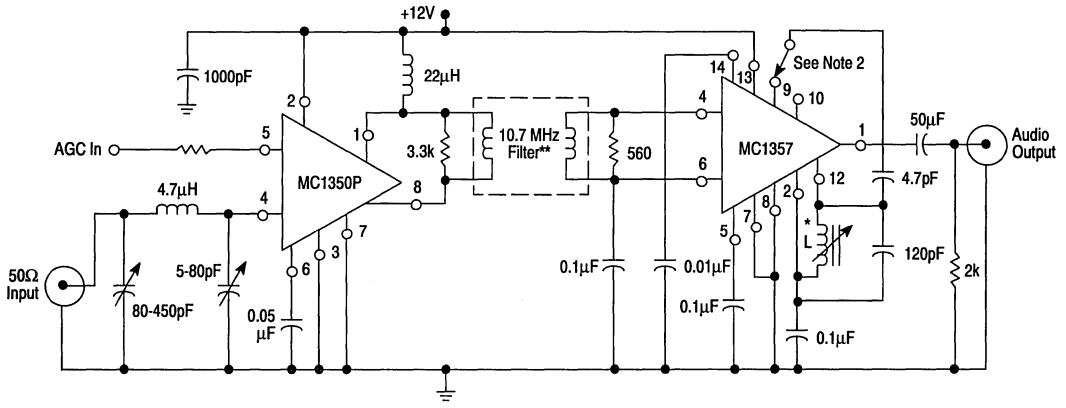
Figure 14. FM Radio Typical Application Circuit



Note 1:
Information shown in Figures 15, 16, and 17 was obtained using the circuit of Figure 14.

Note 2:
Optional input to the quadrature coil may be from either Pin 9 or Pin 10 in the application shown. Pin 9 has commonly been used on this type of part to avoid overload with various tuning techniques. For this reason, Pin 9 is used in tests on the preceding pages (except as noted). However, a significant improvement of limiting sensitivity can be obtained using Pin 10, see Figure 17, and no overload problems have been incurred with this tuned circuit configuration.

Figure 15. Output Distortion

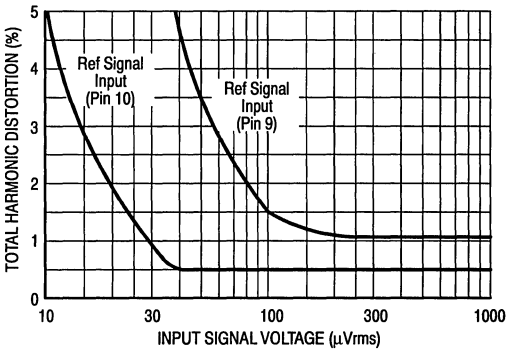


Figure 16. Signal-to-Noise Ratio

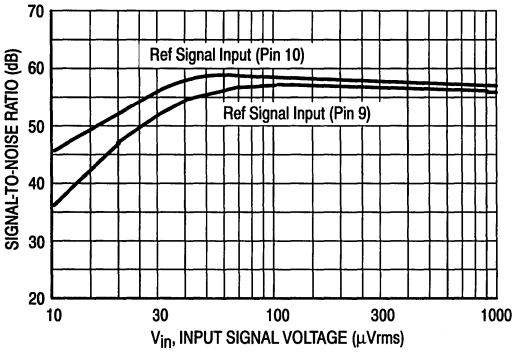


Figure 17. Recovered Audio Output

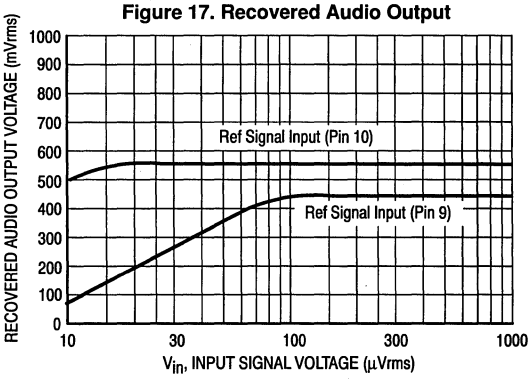
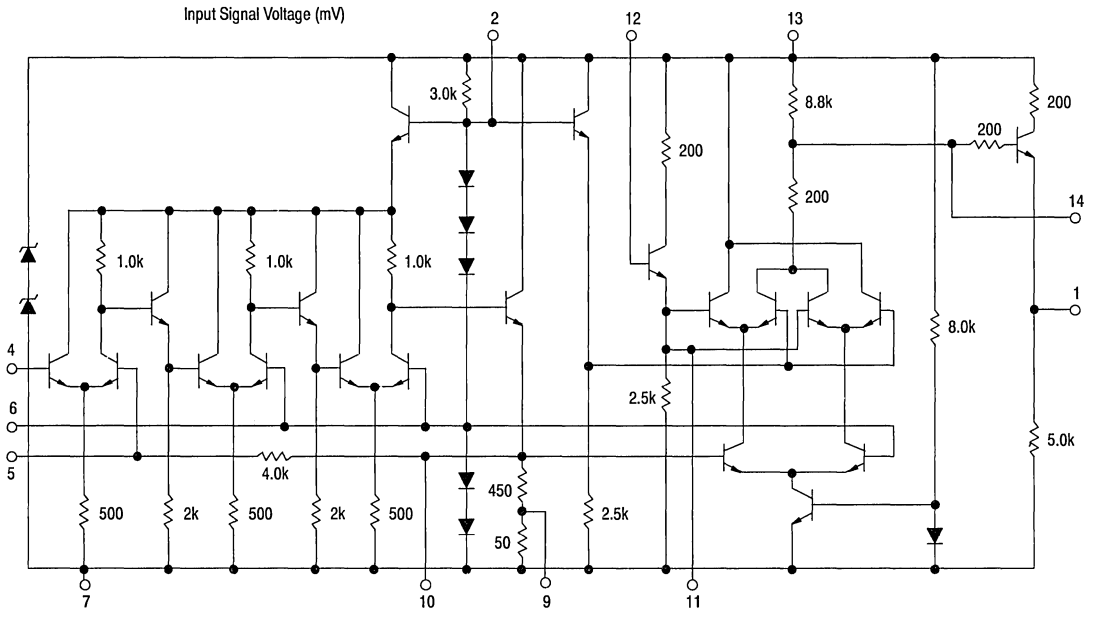


Figure 18. Circuit Schematic



MC1373

TV VIDEO MODULATOR CIRCUIT

SILICON MONOLITHIC INTEGRATED CIRCUIT

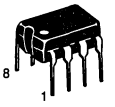
TV Video Modulator

The MC1373 is an RF oscillator and dual-input modulator to generate a TV signal from baseband video inputs.

Applications include video games, home computer display, video tape recorders, and test equipment.

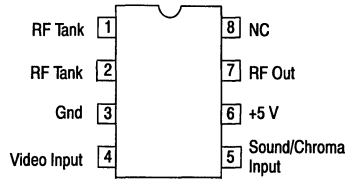
The very low level of intermodulation products, compact package and small external component count make this device superior to simple discrete circuits.

- Single 5.0 Vdc Supply
- Channel 3 or 4 Operation
- Excellent Oscillator Stability to 100 MHz
- Color and Sound Compatibility
- Dual Input Modulator for Ease of Signal Handling
- Low Intermodulation (–50 dB, 920 kHz Beat)
- Overmodulation Protection



P SUFFIX
PLASTIC PACKAGE
CASE 626

PIN CONNECTIONS

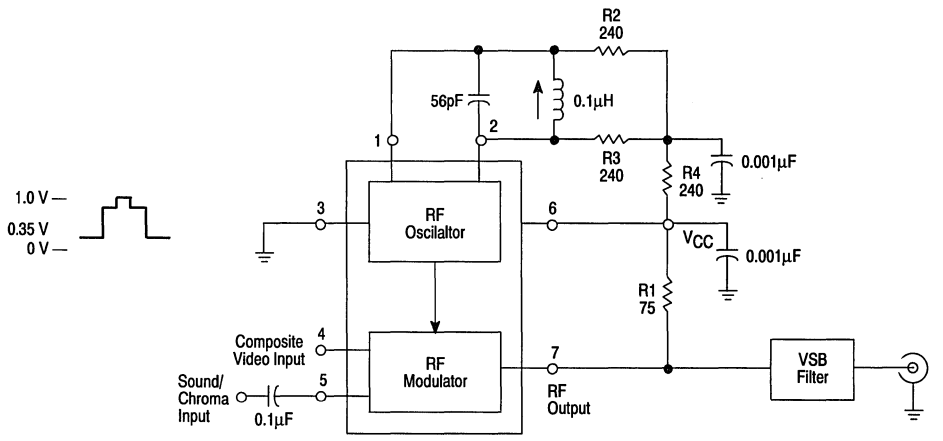


MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted.)

Rating	Value	Unit
Supply Voltage	8.0	Vdc
Operating Ambient Temperature Range	0 to +70	°C
Storage Temperature Range	–65 to +150	°C
Junction Temperature	150	°C
Power Dissipation Package Derate above 25°C	1.25 10	W mW/°C

9

Figure 1. Block Diagram and Application Circuit



RECOMMENDED OPERATING CONDITIONS

Supply Voltage	5.0	Vdc
Luma Input Voltage — Sync Tip Peak White	1.0 0.35	Vdc

ELECTRICAL CHARACTERICISTICS (V_{CC} = +5 Vdc, T_A = 25°C, Test Circuit 1 unless otherwise noted.)

Characteristics	Min	Typ	Max	Unit
Operating Supply Voltage	4.75	5.0	5.25	V
Supply Current	—	12	—	mA
RF MODULATOR				
Luma Input Dynamic Range (Pin 4, see Figure 3)	0	—	1.5	V
RF Output Voltage (f = 67.25 MHz, V4 = 1.0 V)	—	15	—	mVrms
Luma Conversion Gain (ΔV7/ΔV4, V4 = 0.1 Vdc to 1.0 Vdc) (See Figure 3)	—	0.8	—	V/V
Chroma Conversion Gain (ΔV7/ΔV5; V5 = 1.5 Vp–p;V4 = 1.0 Vdc) (See Figure 3)	—	0.95	—	V/V
Chroma Linearity (Pin 7, V5 = 1.5 Vp–p) (See Figure 3)	—	1.0	—	%
Luma Linearity (Pin 7, V4 = 0 Vdc to 1.5 Vdc) (See Figure 3)	—	2.0	—	%
Input Current (Pin 4)	—	—	–20	μA
Input Resistance (Pin 5)	—	800	—	Ω
Input Resistance (Pin 4)	100	—	—	kΩ
Input Capacitance (Pins 4, 5)	—	—	5.0	pF
Residual 920 kHz (Measure at Pin 7) (Note 1)	—	60	—	dB
Output Current (Pin 7, V4 = 0 V) (See Figure 3)	—	1.5	—	mA

TEMPERATURE CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 0° to 70°C, IC only)

RF Oscillator Deviation (f_o = 67.25 MHz)	—	±250	—	kHz

NOTES: 1. RF Reference Level = 6.0 mV @ Pin 7. Load Impedance = 75 Ω
RF + 4.5 MHz = –13 dB.
RF + 3.58 Mhz = –20 dB.

9

Figure 2. Test Circuit 1

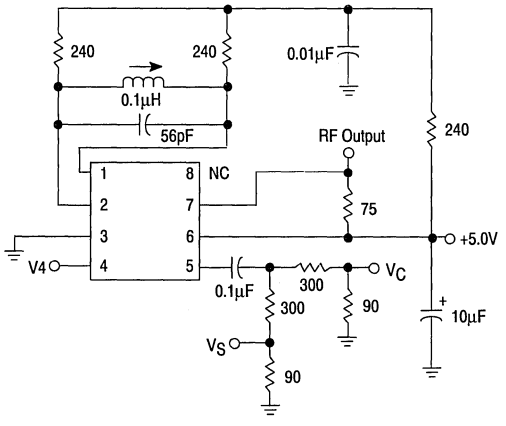


Figure 3. Test Circuit 2

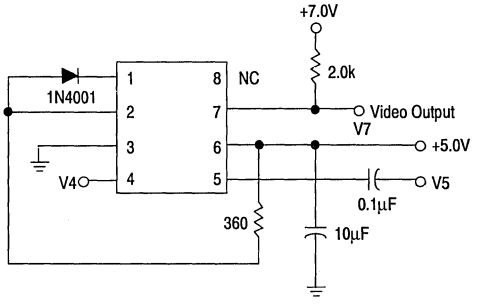
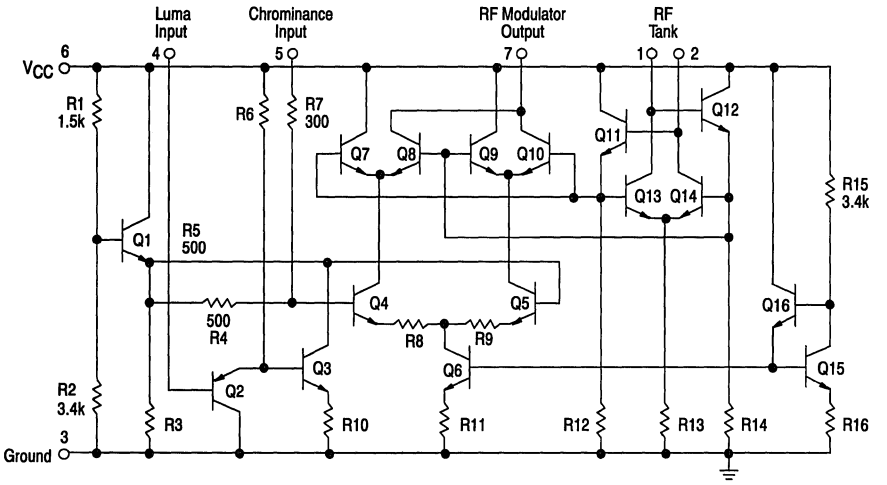


Figure 4. Schematic Diagram



SCHEMATIC DESCRIPTION

The RF oscillator consists of differential amplifier Q13 and Q14 cross-coupled through emitter followers Q11 and Q12. The oscillator will operate at the parallel resonant frequency of the network connected between Pins 1 and 2. The oscillator output is used to switch the doubly balanced RF modulator, Q4 through Q10. Transistors Q2 and Q3 provide level shifting and a high input impedance to the luminance input Pin 4. The bases of transistors Q4 and Q5 are both biased through resistors R4 and R5, respectively, to the same DC reference voltage at Q1 emitter. The base voltage at Q5 may only be offset in a negative direction by luminance signal current source Q3. This design insures that overmodulation due to the luminance signal will never occur. The chrominance signal is externally AC coupled to Pin 5 where it is reduced by resistor dividers R7 and R4, and added to the luminance signal in Q4. The resultant differential composite video currents are switched at the appropriate RF frequency in Q7 through Q10. The output signal current is presented at Pin 7.

Transistors Q15, Q16 and resistors R15, R16 provide a highly stable voltage reference for biasing the current source Q6.

OPERATIONAL DESCRIPTION

Pins 1 and 2 — RF Tank. A tuned circuit connected between these pins determines the RF oscillator frequency. The tuned circuit must provide a low DC resistance shunt. Applying a DC offset voltage between these pins results in baseband composite video at the RF Modulator Output.

Pin 3 — Ground.

Pin 4 — Luminance Input. Input to RF modulator. This pin accepts a DC coupled luminance and sync signal. The amplitude of the RF signal output increases with positive voltage applied to the pin, and ground potential results in zero output (i.e., 100% modulation). A signal with positive-going sync should be used.

Pin 5 — Chrominance/Sound Input. Input to the RF modulator. This pin accepts an AC coupled chrominance signal. The signal is reduced by and internal resistor divider before being applied to the RF modulator. The resistor divider consists of a 300 Ω series resistor and a 500 Ω shunt resistor. A 4.5 MHz FM audio signal may be added to the input by selecting an appropriate series input resistor to provide the correct Luminance:Sound ratio.

Pin 6 — V_{CC}. Positive supply voltage.

Pin 7 — RF Modulator Output. Common collector of output modulator stage. Output impedance and stage gain may be selected by choice of resistor connected between this pin and DC supply.

Pin 8 — No Connection.

APPLICATIONS INFORMATION

RF Modulator and Oscillator

The coil and capacitor connected between Pins 1 and 2 should be selected to have a parallel resonance at the carrier frequency of the desired TV channel. The values of 56 pF and 0.1 µH shown in Figure 1 were chosen for a Channel 4 carrier frequency of 67.25 MHz. For Channel 3 operation, the resonant frequency should be 61.25 MHz (C = 75 pF, L = 0.1 µH). Resistors R2 and R3 are chosen to provide an adequate amplitude of switching voltage, whereas R4 is used to lower the maximum DC level of switching voltage below V_{CC}, thus preventing saturation within the IC.

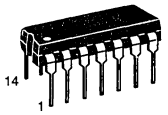
Composite Luminance and Sync should be DC coupled to Luminance Input, Pin 4. This signal must be within the Luma Input Dynamic Range to insure linearity. Since an increase in DC voltage applied to Pin 4 results in an increase in RF output, the input signal should have positive-going sync to generate an NTSC compatible signal. As long as the input signal is positive, overmodulation is prevented by the integrated circuit.

Chrominance information should be AC coupled to Chrominance Input, Pin 5. This pin is internally connected to a resistor divider consisting of a series 300 Ω and a shunt 500 Ω resistor. The input impedance is thus 800 Ω, and a coupling capacitor should be appropriately chosen.

MC1374

TV MODULATOR CIRCUIT

**SILICON MONOLITHIC
INTEGRATED CIRCUIT**



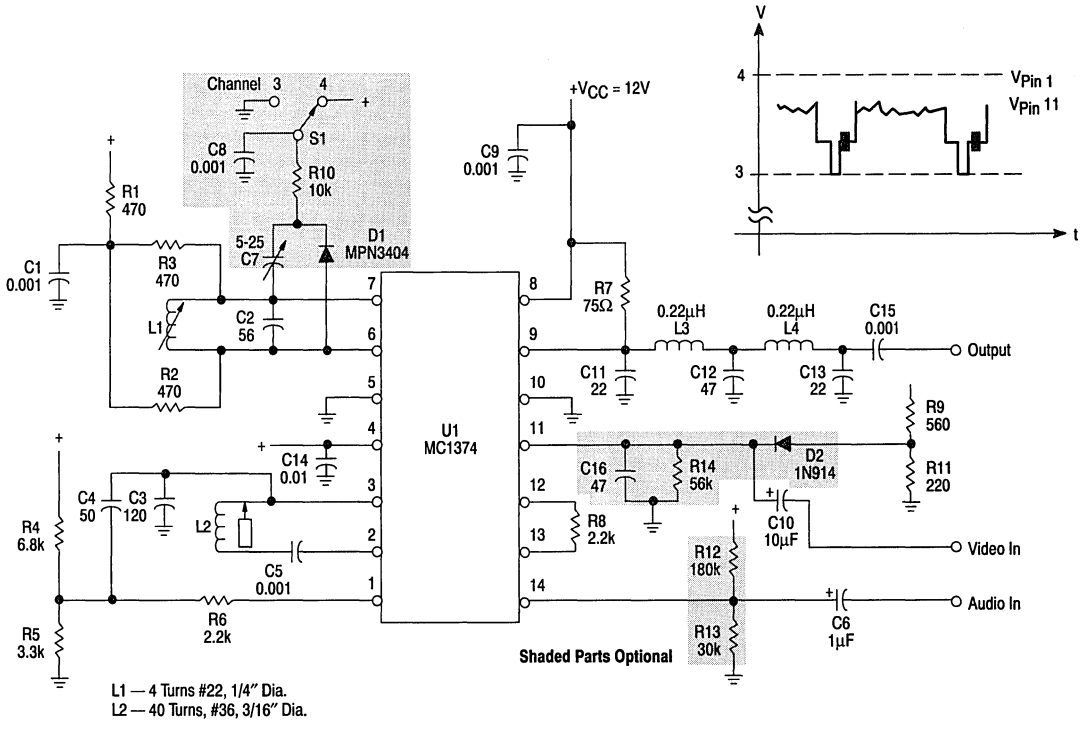
P SUFFIX
PLASTIC PACKAGE
CASE 646

TV Modulator Circuit

The MC1374 includes an FM audio modulator, sound carrier oscillator, RF oscillator, and RF dual input modulator. It is designed to generate a TV signal from audio and video inputs. The MC1374's wide dynamic range and low distortion audio make it particularly well suited for applications such as video tape recorders, video disc players, T.V. games and subscription decoders.

- Single Supply, 5 V to 12 V
- Channel 3 or 4 Operation
- Variable Gain RF Modulator
- Wide Dynamic Range
- Low Intermodulation Distortion
- Positive or Negative Sync
- Low Audio Distortion
- Few External Components

Figure 1. Typical Application



9

MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted.)

Rating	Value	Unit
Supply Voltage	14	Vdc
Operating Ambient Temperature Range	0 to +70	°C
Storage Temperature Range	–65 to +150	°C
Junction Temperature	150	°C
Power Dissipation Package Derate above 25°C	1.25 10 mW/°C	W

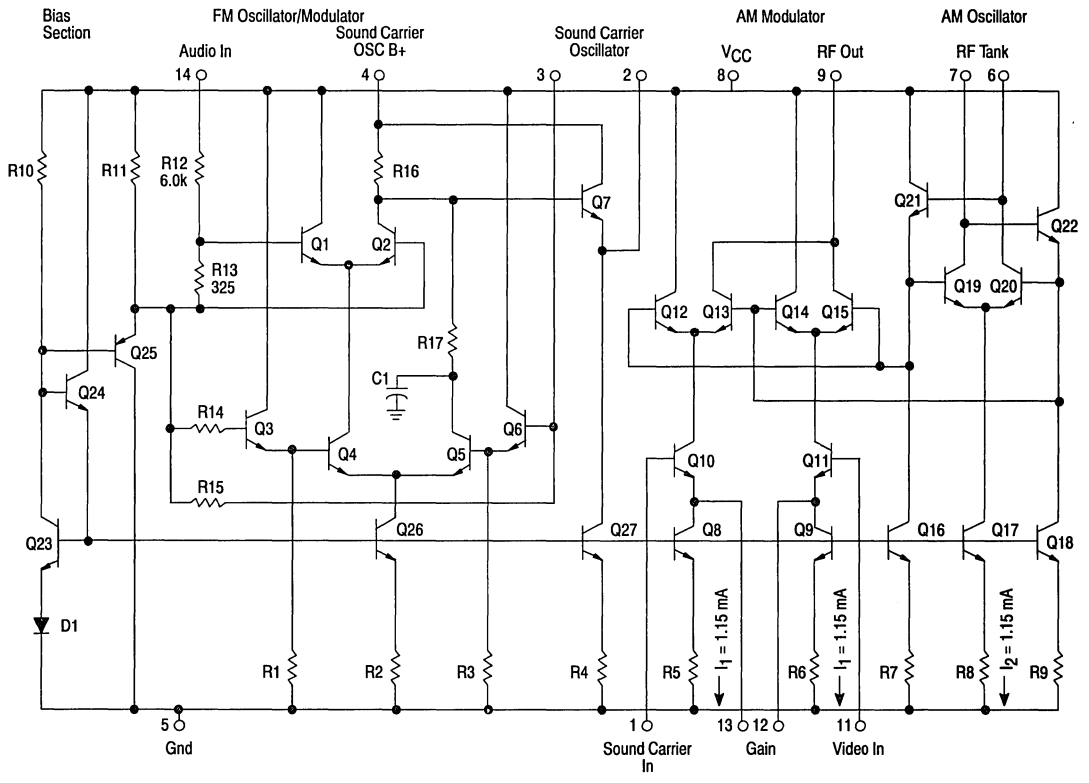
ELECTRICAL CHARACTERICISTICS (V_{CC} = 12 Vdc, T_A = 25°C, f_c = 67.25 MHz, Figure 4 circuit, unless otherwise noted.)

Characteristics	Min	Typ	Max	Unit
AM OSCILLATOR/MODULATOR				
Operating Supply Voltage	5.0	12	12	V
Supply Current (Figure 1)	—	13	—	mA
Video Input Dynamic Range (Sync Amplitude)	0.25	1.0	1.0	V Pk
RF Output (Pin 9, R7 = 75 Ω, No External Load)	—	170	—	mV pp
Carrier Suppression	36	40	—	dB
Linearity (75% to 12.5% Carrier, 15 kHz to 3.58 MHz)	—	—	2.0	%
Differential Gain Distortion (IRE Test Signal)	5.0	7.0	10	%
Differential Phase Distortion (3.58 MHz IRE Test Signal)	—	1.5	2.0	Degrees
920 kHz Beat (3.58 MHz @ 30%, 4.5 MHz @ 25%)	—	–57	—	dB
Video Bandwidth (75 Ω Input Source)	30	—	—	MHz
Oscillator Frequency Range	—	105	—	MHz
Internal Resistance across Tank (Pin 6 to Pin 7) Internal Capacitance across Tank (Pin 6 to Pin 7)	— —	1.8 4.0	— —	kΩ pF

ELECTRICAL CHARACTERICISTICS (T_A = 25°C, V_{CC} = 12 Vdc, 4.5 MHz, Test circuit of Figure 11, unless otherwise noted.)

Characteristics	Min	Typ	Max	Unit
FM OSCILLATOR/MODULATOR				
Frequency Range of Modulator Frequency Shift versus Temperature (Pin 14 open) Frequency Shift versus V_{CC} (Pin 14 open) Output Amplitude (Pin 3 not loaded) Output Harmonics, Unmodulated	14 — — — —	4.5 0.2 — 900 —	14 0.3 4.0 — –40	MHz kHz/°C kHz/V mVp–p dB
Modulation Sensitivity 1.7 MHz 4.5 MHz 10.7 MHz	— — —	0.20 0.24 0.80	— — —	MHz/V
Audio Distortion (±25 kHz Deviation, Optimized Bias Pin 14) Audio Distortion (±25 kHz Deviation, Pin 14 self biased) Incidental AM (±25 kHz FM)	— — —	0.6 1.4 2.0	1.0 — —	%
Audio Input Resistance (Pin 14 to ground) Audio Input Capacitance (Pin 14 to ground)	— —	6.0 5.0	— —	kΩ pF
Stray Tuning Capacitance (Pin 3 to ground) Effective Oscillator Source Impedance (Pin 3 to load)	— —	5.0 2.0	— —	pF kΩ

Figure 2. TV Modulator



GENERAL INFORMATION

The MC1374 contains an RF oscillator, RF modulator, and a phase-shift type FM modulator, arranged to permit good printed circuit layout of a complete T.V. modulation system. The RF oscillator is similar to the one used in MC1373, and is coupled internally in the same way. It's frequency is controlled by and external tank on Pins 6 and 7, or by a crystal circuit, and will operate to approximately 105 MHz. The video modulator is a balanced type as used in the well known MC1496. Modulated sound carrier and composite video information can be put in separately on Pins 1 and 11 to minimize unwanted crosstalk. A single resistor on Pins 12 and 13 is selected to set the modulator gain. The RF output at Pin 9 is a current source which drives a load connected from Pin 9 to V_{CC}.

The FM system was designed specifically for the T.V. intercarrier function. For circuit economy, one phase shift circuit was built into the ship. Still, it will operate from 1.4 MHz to 14 MHz, low enough to be used in a cordless telephone base station (1.76 MHz), and high enough to be used as an FM IF test signal source (10.7 MHz). AT 4.5 MHz, a deviation of ±25 kHz can be achieved with 0.6% distortion (typical).

In the circuit above devices Q1 through Q7 are active in the oscillator function. Differential amplifier Q3, Q4, Q5, and Q6 acts as a gain stage, sinking current from input section Q1, Q2 and the phase shift network R17, C1. Input amplifier Q1, Q2 can vary the amount of "in phase" Q4 current to be combined with phase shifter current in load resistor R16. The R16 voltage is applied to emitter follower Q7 which drives an external L-C circuit. Feedback from the center of the L-C circuit back to the base of Q6 closes the loop. As audio input is applied which would off-set the stable oscillatory phase, the frequency changes to counteract. The input to Pin 14 can include a DC feedback current for AFC over a limited range.

The modulated FM signal from Pin 3 is coupled to Pin 1 of the RF modulator and is then modulated onto the AM carrier.

AM Section

The AM modulator transfer function in Figure 3 shows that the video input can be of either polarity (and can be applied at either input). When the voltages on Pin 1 and Pin 11 are equal, the RF output is theoretically zero. As the difference between $V_{Pin\ 11}$ and $V_{Pin\ 1}$ increase, the RF output increases linearly until all of the current from both I_1 current sources (Q8 and Q9) is flowing in one side of the modulator. This occurs when $\pm(V_{Pin11} - V_{Pin1}) = I_1 R_G$, where I_1 is typically 1.15 mA. The peak-to-peak RF output is the $2I_1 R_L$. Usually the value of R_L is chosen to be 75 Ω to ease the design of the output filter and match into T.V. distribution systems. The theoretical range of input voltage and R_G is quite wide, but noise and available sound level limit the useful video (sync tip) amplitude to between 0.25 Vpk and 1.0 Vpk. It is recommended that the value of R_G be chosen so that only about half of the dynamic range will be used at sync tip level.

The operating window of Figure 5 shows a cross-hatched area where Pin 1 and Pin 11 voltages must always be in order to avoid saturation in any part of the modulator. The letter ϕ represents one diode drop, or about 0.75 V. The oscillator Pins 6 and 7 must be biased to a level of $V_{CC} - \phi - 2I_1 R_L$ (or lower) and the input Pins 1 and 11 must always be at least 2ϕ below that. It is permissible to operate down to 1.6 V, saturating the current sources, but whenever possible, the minimum should be 3ϕ above ground.

The oscillator will operate dependably up to about 105 MHz with a broad range of tank circuit components values. It is desirable to use a small L and a large C to minimize the dependence on IC internal capacitance. An operating Q between 10 and 20 is recommended. The values of R_1, R_2 and R_3 are chosen to produce the desired Q and to set the Pin 6 and 7 DC voltage as discussed above. Unbalanced operation; i.e., Pin 6 or 7 bypassed to ground, is not recommended. Although the oscillator will still run, and the modulator will produce a useable signal, this mode causes substantial base-band video feedthrough. Bandswitching, as Figure 1 shows, can still be accomplished economically without using the unbalanced method.

The oscillator frequency with respect to temperature in the test circuit shows less than ±20 kHz total shift from 0° to 50°C as shown in Figure 7. At higher temperatures the slope approaches 2.0 kHz/°C. Improvement in this region would require a temperature compensating tuning capacitor of the N75 family.

Crystal control is feasible using the circuit shown in Figure 21. The crystal is a 3rd overtone series type, used in series resonance. The L1, C2 resonance is adjusted well below the crystal frequency and is sufficiently tolerant to permit fixed values. A frequency shift versus temperature of less than 1.0 Hz/°C can be expected from this approach. The resistors Ra and Rb are to suppress parasitic resonances.

Coupling of output RF to wiring and components on Pins 1 and 11 can cause as much as 300 kHz shift in carrier (at 67 MHz) over the video input range. A careful layout can keep this shift below 10 kHz. Oscillator may also be inadvertently coupled to the RF output, with the undesired effect of preventing a good null when $V_{11} = V_1$. Reasonable care will yield carrier rejection ratios of 36 dB to 40 dB below sync tip level carrier.

In television, one of the most serious concerns is the prevention of the intermodulation of color (3.58 MHz) and sound (4.5 MHz) frequencies, which causes a 920 kHz signal to appear in the spectrum. Very little (3rd order) nonlinearity is needed to cause this problem. The results in Figure 6 are unsatisfactory, and demonstrate that too much of the available dynamic range of the MC1374 has been used. Figures 8 and 10 show that by either reducing standard signal level, or reducing gain, acceptable results may be obtained.

At VHF frequencies, small imbalances within the device introduce substantial amounts of 2nd harmonic in the RF output. At 67 MHz, the 2nd harmonic is only 6 dB to 8 dB below the maximum fundamental. For this reason a double pi low pass filter is shown in the test circuit of Figure 3 and works well for Channel 3 and 4 lab work. For a fully commercial application, a vestigial sideband filter will be required. The general form and approximate values are shown in Figure 19. It must be exactly aligned to the particular channel.

Figure 3. AM Modulator Transfer Function

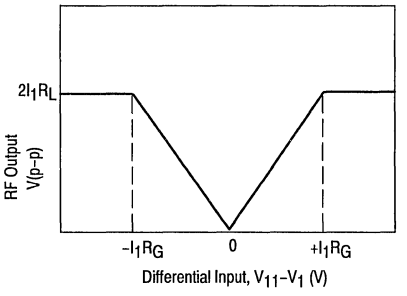


Figure 4. AM Test Circuit

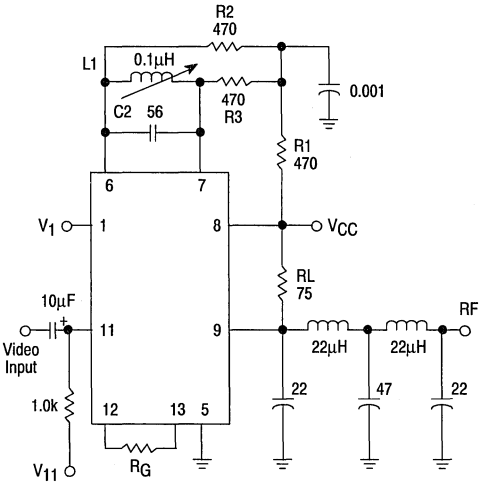


Figure 5. The Operating Window

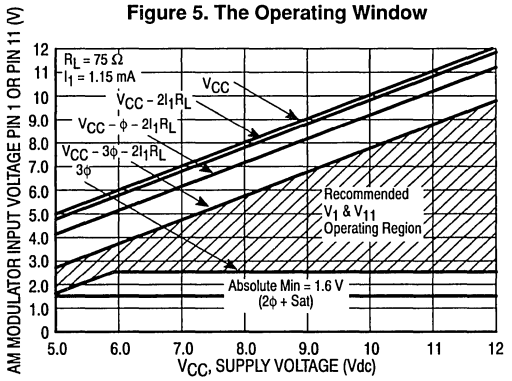


Figure 6. 920 kHz Beat

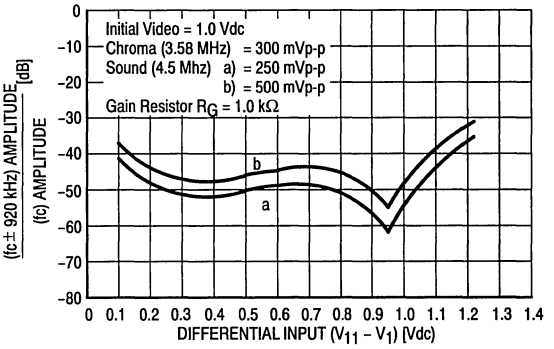


Figure 7. RF Oscillator Frequency versus Temperature

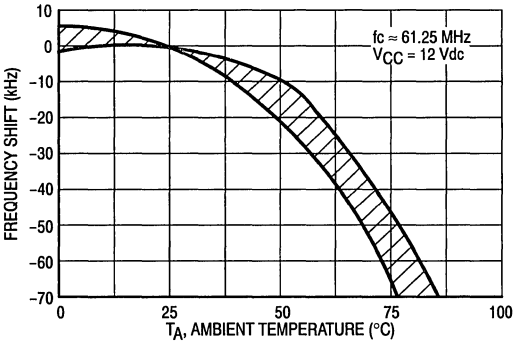


Figure 8. 920 kHz Beat

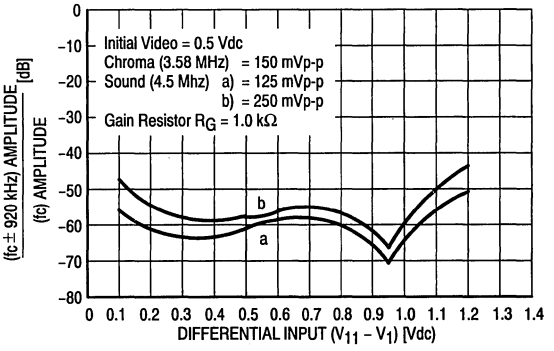


Figure 9. RF Oscillator Frequency versus Supply Voltage

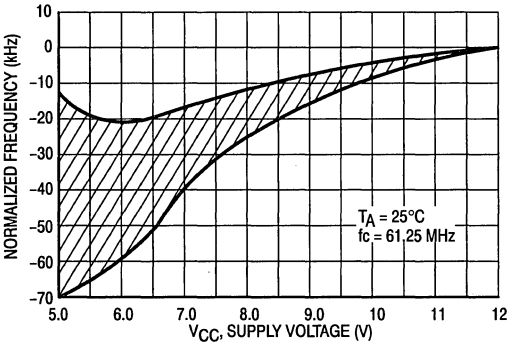
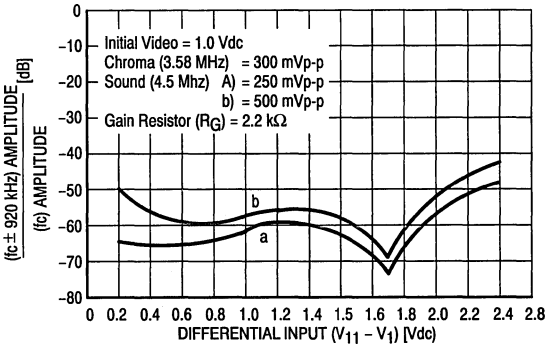


Figure 10. 920 kHz Beat



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FM Section

The oscillator center is approximately the resonance of the inductor L_2 from Pin 2 to Pin 3 and the effective capacitance C_3 from Pin 3 to ground. For overall oscillator stability, it is best to keep X_L in the range of 300 Ω to 1.0 kΩ.

The modulator transfer characteristic at 4.5 MHz is shown in Figure 15. Transfer curves at other frequencies have a very similar shape, but differ in deviation per input volt, as shown in Figures 13 and 17.

Most applications will not require DC connection to the audio input, Pin 14. However, some improvements can be achieved by the addition of biasing circuitry. The unaided device will establish its own Pin 14 bias at 4 θ, or about 3.0 V. This bias is a little too high for optimum modulation linearity. Figure 14 shows better than 2 to 1 improvement in distortion between the unaided device and pulling Pin 14 down to 2.6 V to 2.7 V. This can be accomplished by a simple divider, if the supply voltage is relatively constant.

The impedance of the divider has a bearing on the frequency versus temperature stability of the FM system. A divider of 180 kΩ and 30 kΩ (for V_{CC} = 12 V) will give good temperature stabilization results. However, as Figure 18 shows, a divider is not a good method if the supply voltage varies. The designer must make the decisions here, based on considerations of economy, distortion and temperature requirements and power supply capability. If the distortion requirements are not stringent, then no bias components are needed. If, in this case, the temperature compensation needs to be improved in the high ambient area, the tuning capacitor from Pin 3 to ground can be selected from N75 or N150 temperature compensation types.

Another reason for DC input to Pin 14 is the possibility of automatic frequency control. Where high accuracy of intercarrier frequency is required, it may be desirable to feed back the DC output of an AFC or phase detector for nominal carrier frequency control. Only limited control range could be used without adversely affecting the distortion performance, but very little frequency compensation will be needed.

One added convenience in the FM section is the separate Pin "oscillator B+" which permits disabling of the sound system during alignment of the AM section. Usually it can be hard wired to the V_{CC} source without decoupling.

Standard practice in television is to provide pre-emphasis of higher audio frequencies at the transmitter and a matching de-emphasis in the TV receiver audio amplifier. The purpose of this is to counteract the fact that less energy is usually present in the higher frequencies, and also that fewer modulation sidebands are within the deviation window. Both factors degrade signal to noise ration. Pre-emphasis of 75 µs is standard practice. For cases where it has not been provided, a suitable pre-emphasis network is covered in Figure 20.

It would seem natural to take the FM system output from Pin 2, the emitter follower output, but this output is high in harmonic content. Taking the output from Pin 3 sacrifices somewhat in source impedance but results in a clean output fundamental, with all harmonics more than 40 dB down. This choice removes the need for additional filtering components. The source impedance of Pin 3 is approximately 2.0 kΩ, and the open circuit amplitude is about 900 mV p-p for the test circuit shown in Figure 11.

The application circuit of Figure 1 shows the recommended approach to coupling the FM output from Pin 3 to the AM modulator input, Pin 1. The input impedance at Pin 1 is very high, so the intercarrier level is determined by the source impedance of Pin 3 driving through C4 into the video bias circuit impedance of R4 and R5, about 2.2 k. This provides an intercarrier level of 500 mV p-p, which is correct for the 1.0 V peak video level chosen in this design. Resistor R6 and the input capacitance of Pin 1 provide some decoupling of stray pickup of RF oscillator or AM output which may be coupled to the sound circuitry.

Figure 11. FM Test Circuit

f_0 (MHz)	C3 (pF)	L2 (µH)
10.7	12	10
4.5	120	10
1.76	200	40

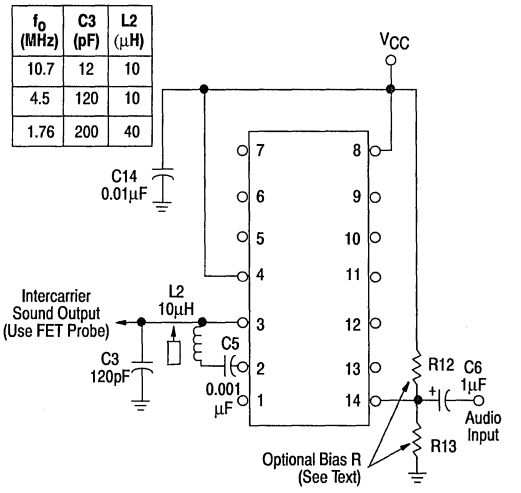

Figure 12. Modulator Sensitivity

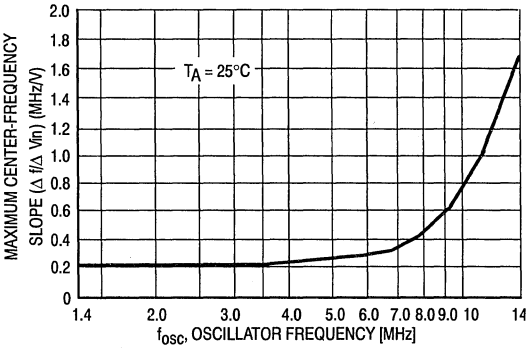

Figure 13. Modulator Transfer Function

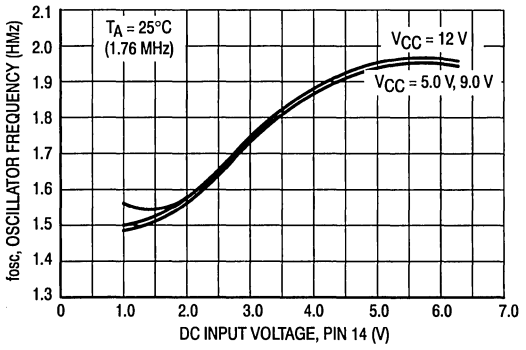

Figure 14. Distortion versus Modulation Depth

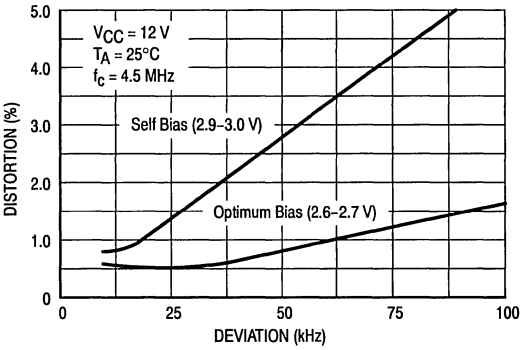

Figure 15. Modulator Transfer Function

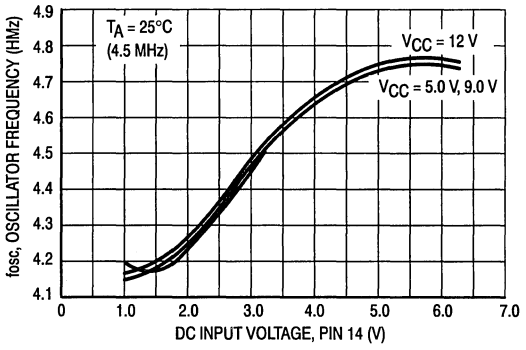

Figure 16. FM System Frequency versus Temperature

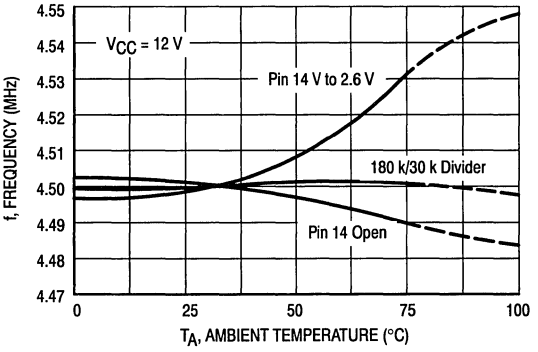

Figure 17. Modulator Transfer Function

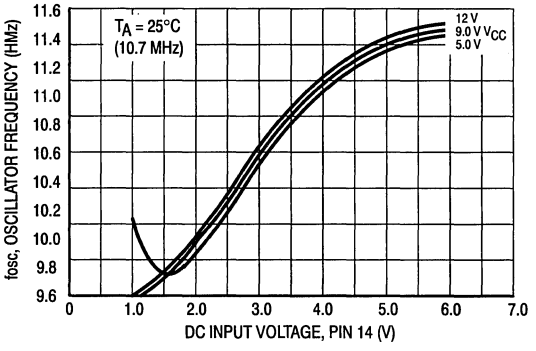

Figure 18. FM System Frequency versus V_{CC}

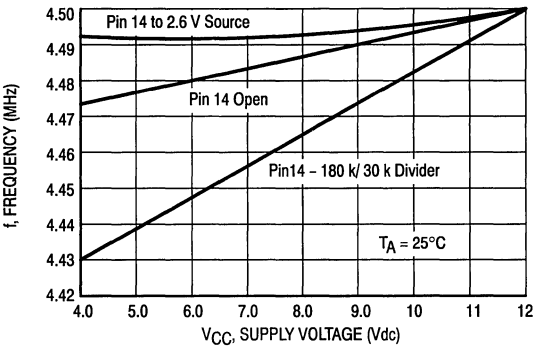

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Figure 19. A Channel 4 Vestigial Sideband Filter

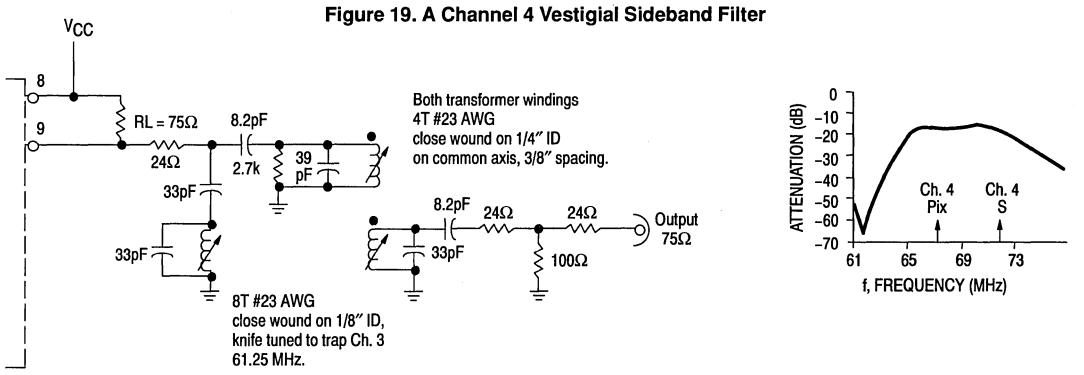


Figure 20. Audio Pre-Emphasis Circuit

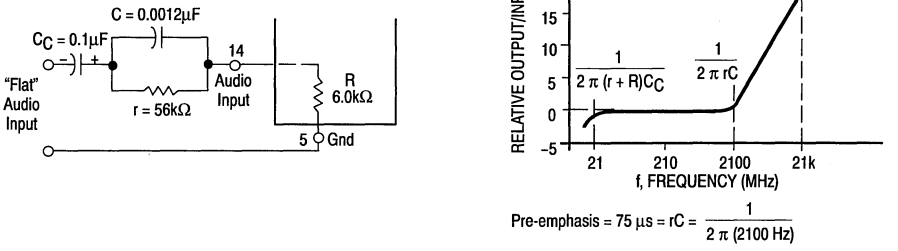
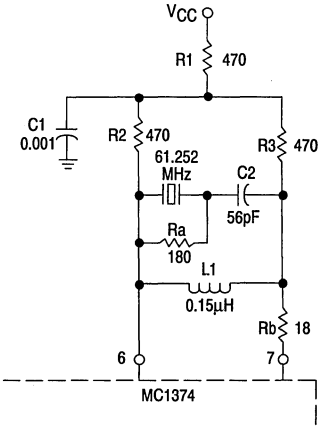


Figure 21. Crystal Controlled RF Oscillator for Channel 3, 61.25 MHz



NOTE: See Application Note AN829 for further information.

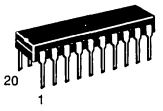
MC1377

**COLOR TELEVISION
RGB to PAL/NTSC ENCODER**

Color Television RGB to PAL/NTSC Encoder

The MC1377 will generate a composite video from baseband red, blue, green and sync inputs. On board features include: a color subcarrier oscillator; voltage controlled 90° phase shifter; two double sideband suppressed carrier (DSBSC) chroma modulators; and RGB input matrices with blanking level clamps. Such features permit system design with few external components and accordingly, system performance comparable to studio equipment with external components common in receiver systems.

- Self-contained or Externally Driven Reference Oscillator
- Chroma Axes, Nominally 90° (±5°), are Optionally Trimable
- PAL/NTSC Compatible
- Internal 8.2 V Regulator



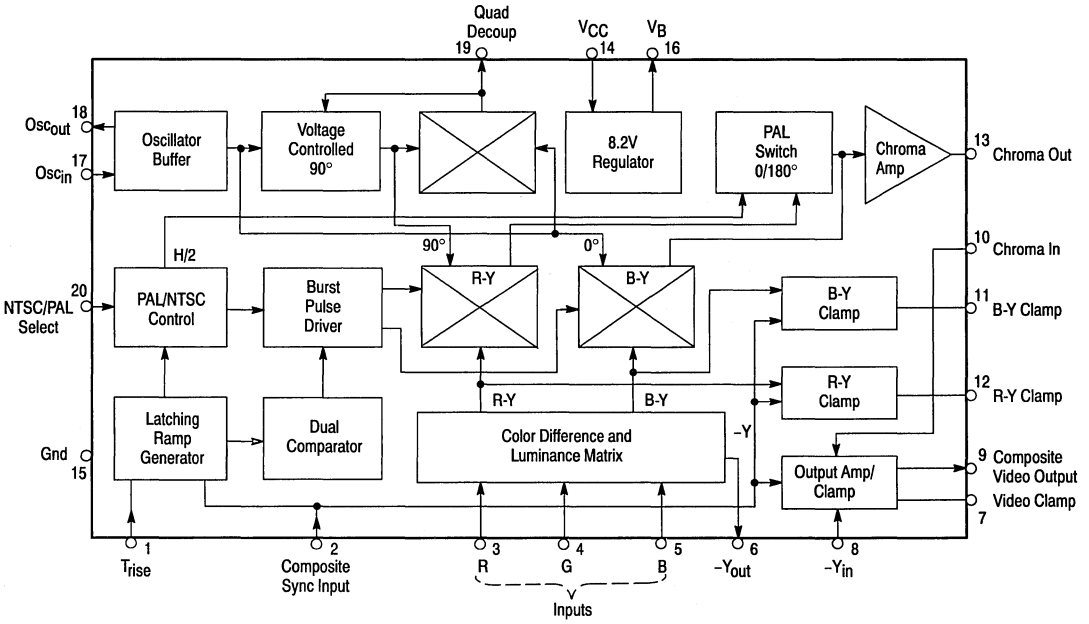
P SUFFIX
PLASTIC PACKAGE
CASE 738

DW SUFFIX
PLASTIC PACKAGE
CASE 751D
(SO-20L)

ORDERING INFORMATION

Device	Temperature Range	Package
MC1377DW	0° to +70°C	SO-20L
MC1377P		Plastic DIP

Figure 1. Simplified Block Diagram



MAXIMUM OPERATING CONDITIONS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	15	Vdc
Storage Temperature	T_{stg}	–65 to +150	°C
Power Dissipation Package Derate above 25°C	P_D	1.25 10	W mW/°C
Operating Temperature	T_A	0 to +70	°C

RECOMMENDED OPERATING CONDITIONS

Characteristics	Min	Typ	Max	Unit
Supply Voltage	10	12	14	Vdc
I_B Current (Pin 16)	0	—	–10	mA
Sync, Blanking Level (DC level between pulses, see Figure 9e) Sync Tip Level (see Figure 9e) Sync Pulse Width (see Figure 9e)	1.7 –0.5 2.5	— 0 —	8.2 0.9 5.2	Vdc µs
R, G, B Input (Amplitude) R, G, B Peak Levels for DC Coupled Inputs, with Respect to Ground	— 2.2	1.0 —	— 4.4	$V_{(p-p)}$ V
Chrominance Bandwidth (Non-comb Filtered Applications), (6 dB)	0.5	1.5	2.0	MHz
Ext. Subscarrier Input (to Pin 17) if On-Chip Oscillator is not used.	0.5	0.7	1.0	$V_{(p-p)}$

ELECTRICAL CHARACTERICISTICS (V_{CC} = 12 Vdc, T_A = 25°C, circuit of Figure 7, unless otherwise noted.)

Characteristics	Pins	Symbol	Min	Typ	Max	Unit
SUPPLY CURRENT						
Supply Current into V_{CC}, No Load, on Pin 9. Circuit Figure 7 V_{CC} = 10 V V_{CC} = 11 V V_{CC} = 12 V V_{CC} = 13 V V_{CC} = 14 V	14	I_{CC}	— — 20 — —	33 34 35 36 37	— — 40 — —	mA
VOLTAGE REGULATOR						
V_B Voltage (I_B = –10 mA, V_{CC} = 12 V, Figure 7) Load Regulation (0 < I_B ≤ 10 mA, V_{CC} = 12 V) Line Regulation (I_B = 0 mA, 10 V < V_{CC} < 14 V)	16	V_B Reg_{load} Reg_{line}	7.7 –20 —	8.2 120 4.5	8.7 +30 —	Vdc mV mV/V
OSCILLATOR AND MODULATION						
Oscillator Amplitude with 3.58 MHz/4.43 MHz crystal	17	Osc	—	0.6	—	$V_{(p-p)}$
Subcarrier Input: Resistance at 3.58 MHz 4.43 MHz	17	R_{osc}	— —	5.0 4.0	— —	kΩ
Capacitance		C_{osc}	—	2.0	—	pF
Modulation Angle (R-Y) to (B-Y) Angle Adjustment (R-Y) DC Bias Voltage	— 19 19	Ø ΔØ V_{19}	— — —	±5 0.25 6.4	— — —	Deg Deg/µA Vdc
CHROMINANCE AND LUMINANCE9						
Chroma Input DC Level Chroma Input Level for 100% Saturation	10	V_{in}	— —	4.0 0.7	— —	Vdc $V_{(p-p)}$
Chroma Input: Resistance Capacitance		R_{in} C_{in}	— —	10 2.0	— —	kΩ pF
Chroma DC Output Level Chroma Output Level at 100% Saturation	13	V_{out}	8.9 —	10 1.0	10.9 —	Vdc $V_{(p-p)}$
Chroma Output Resistance		R_{out}	—	50	—	Ω
Luminance Bandwidth (-3.0 dB), Less Delay Line	9	BW_{Luma}	—	8.0	—	MHz

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ELECTRICAL CHARACTERICISTICS (V_{CC} = 12 Vdc, T_A = 25°C, circuit of Figure 7, unless otherwise noted.)

Characteristics	Pins	Symbol	Min	Typ	Max	Unit
VIDEO INPUT						
R, G, B Input DC Levels	3, 4, 5	RGB	2.8	3.3	3.8	Vdc
R, G, B Input for 100% Color Saturation			—	1.0	—	$V_{(p-p)}$
R, G, B Input: Resistance		R_{RGB}	8.0	10	17	kΩ
Capacitance		C_{RGB}	—	2.0	—	pF
Sync Input Resistance (1.7 V < Input < 8.2)	2	Sync	—	10	—	kΩ
COMPOSITE VIDEO OUTPUT						
Composite Output, 100% Saturation (see Figure 8d) — Sync	9	CV_{out}	—	0.6	—	$V_{(p-p)}$
Luminance			—	1.4	—	
Chroma			—	1.7	—	
Burst			—	0.6	—	
Output Impedance (Note 1)		R_{video}	—	50	—	Ω
Subcarrier Leakage in Output (Note 2)		V_{lk}	—	20	—	$mV_{(p-p)}$

NOTES: 1. Output Impedance can be reduced to less than 10 Ω by using a 150 Ω output load from Pin 9 to ground. Power supply current will increase to about 60 mA.
2. Subcarrier leakage can be reduced to less than 10 mV with optional circuitry, (see Figure 12).

PIN DESCRIPTIONS

Symbol	Pin Number*	Description
t_r	1	External components at this pin set the rise time of the internal ramp function generator. See Figure 10.
Sync	2	Composite sync input. Presents 10 kΩ resistance to input.
R	3	Red signal input. Presents 10 kΩ impedance to input. 1.0 $V_{(p-p)}$ required for 100% saturation.
G	4	Green signal input. Presents 10 kΩ impedance to input. 1.0 $V_{(p-p)}$ required for 100% saturation.
B	5	Blue signal Input. Presents 10 kΩ impedance to input. 1.0 $V_{(p-p)}$ required for 100% saturation.
$-Y_{out}$	6	Luma (-Y) output. Allows external setting of luma delay time.
V_{clamp}	7	Video Clamp pin. Typical connection is a 0.01 µF capacitor to ground.
$-Y_{in}$	8	Luma (-Y) input. Presents 10 kΩ input impedance.
CV_{out}	9	Composite Video output. 50 Ω output impedance.
$Chroma_{In}$	10	Chroma input. Presents 10 kΩ input impedance.
$B\text{-}Y_{clamp}$	11	B-Y clamp. Clamps B-Y during blanking with a 0.1 µF capacitor to ground. Also used with R-Y clamp to null residual color subcarrier in output.
$R\text{-}Y_{clamp}$	12	R-Y clamp. Clamps R-Y during blanking with a 0.1 µF capacitor to ground. Also used with B-Y clamp to null residual color subcarrier in output.
$Chroma_{Out}$	13	Chroma output. 50 Ω output impedance.
V_{CC}	14	Power supply pin for the IC. +12, ± 2.0 V, required at 35 mA (typical).
Gnd	15	Ground pin.
V_B	16	+8.2 V reference from an internal regulator capable of delivering 10 mA to external circuitry.
Osc_{in}	17	Oscillator input. A transistor base presents 5 kΩ to an external subcarrier input, or is available for constructing a Colpitts oscillator. (See Figure 4)
Osc_{out}	18	Oscillator output. The emitter of the transistor, with base access at pin 17, is accessible for completing the Colpitts oscillator. See Figure 4.
$Ø_m$	19	Quad decoupler. With external circuitry, R-Y to B-Y relative angle errors can be corrected. Typically, requires a 0.01 µF capacitor to ground.
NTSC/PAL Select	20	NTSC/PAL switch. When grounded the MC1377 is in the NTSC mode; if unconnected, in the PAL mode.

*Pin designations apply to both the DIP and the SOIC package.

9

FUNCTIONAL DESCRIPTION

Figure 2. Power Supply and V_B

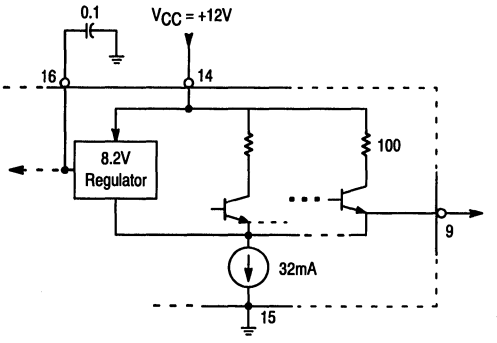


Figure 3. RGB Input Circuitry

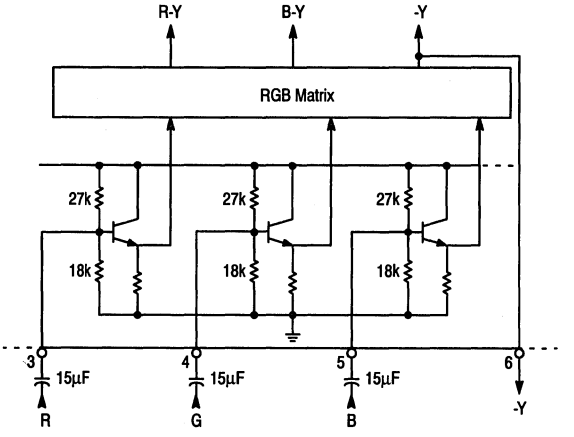
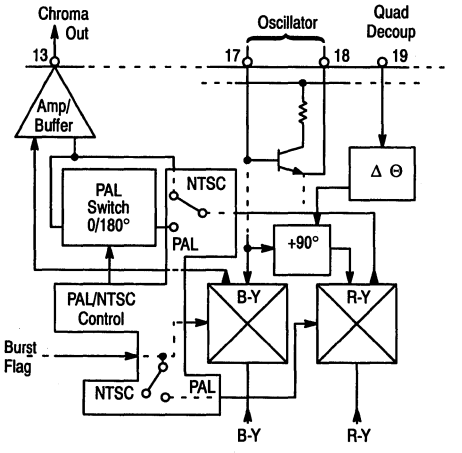


Figure 4. Chroma Section



Power Supply and V_B (8.2 V Regulator)

The MC1377 pin for power supply connection is Pin 14. From the supply voltage applied to this pin, the IC biases internal output stages and is used to power the 8.2 V internal regulator (V_B at Pin 16) which biases the majority of internal circuitry. The regulator will provide a nominal 8.2 V and is capable of 10 mA before degradation of performance. An equivalent circuit of the supply and regulator is shown in Figure 2.

R, G, B Inputs

The RGB inputs are internally biased to 3.3 V and provide 10 kΩ of input impedance. Figure 3 shows representative input circuitry at Pins 3, 4, and 5.

The input coupling capacitors of 15 µF are used to prevent tilt during the 50/60 Hz vertical period. However, if it is desired to avoid the use of the capacitors, then inputs to Pins 3, 4, and 5 can be DC coupled provided that the signal levels are always between 2.2 V and 4.4 V.

After input, the separate RGB information is introduced to the matrix circuitry which outputs the R-Y, B-Y, and -Y signals. The -Y information is routed out at Pin 6 to an external delay line (typically 400 ns).

DSBSC Modulators and 3.58 MHz Oscillator

The R-Y and B-Y outputs (see (B-Y)/(R-Y) Axes versus I/Q Axes, Figure 22) from the matrix circuitry are amplitude modulated onto the 3.58/4.43 MHz subcarrier. These signals are added and color burst is included to produce composite chroma available at Pin 13. These functions plus others, depending on whether NTSC or PAL operation is chosen, are performed in the chroma section. Figure 4 shows a block diagram of the chroma section.

The MC1377 has two double balanced mixers and regardless of which mode is chosen (NTSC or PAL), the mixers always perform the same operation. The B-Y mixer modulates the color subcarrier directly, the R-Y mixer receives a 90° phase shifted color subcarrier before being modulated by the R-Y baseband information. Additional operations are then performed on these two signals to make them NTSC or PAL compatible.

In the NTSC mode, the NTSC/PAL control circuitry allows an inverted burst of 3.58 MHz to be added only to the B-Y signal. A gating pulse or "burst flag" from the timing section permits color burst to be added to the B-Y signal. This color burst is 180° from the B-Y signal and 90° away from the R-Y signal (see Figure 22) and permits decoding of the color information. These signals are then added and amplified before being output, at Pin 13, to be bandpassed and then reintroduced to the IC at Pin 10.

In the PAL mode, NTSC/PAL control circuitry allows an inverted 4.43 MHz burst to be added to both R-Y and B-Y equally to produce the characteristic PAL 225°/135 burst phase. Also, the R-Y information is switched alternately from 180° to 0° of its original position and added to the B-Y information to be amplified and output.

Timing Circuitry

The composite sync input at Pin 2 performs three important functions: it provides the timing (but not the amplitude) for the sync in the final output; it drives the black level clamps in the modulators and output amplifier; and it triggers the ramp generator at Pin 1, which produces burst envelope and PAL switching. A representative block diagram of the timing circuitry is shown in Figure 5.

In order to produce a color burst, a burst envelope must be generated which "gates" a color subcarrier into the R-Y and B-Y modulators. This is done with the ramp generator at Pin 1.

The ramp generator at Pin 1 is an R-C type in which the pin is held low until the arrival of the *leading* edge of sync. The rising ramp function, with time constant R-C, passes through two level sensors—the first one starts the gating pulse and the second stops it (see Figure 10). Since the 'early' part of the exponential is used, the timing provided is relatively accurate from chip-to-chip and assembly-to-assembly. Fixed components are usually adequate. The ramp continues to rise for more than half of the line interval, thereby inhibiting burst generation on 'half interval' pulses on vertical front and back porches. The ramp method will produce burst on the vertical front and back 'porches' at full line intervals.

R-Y, B-Y Clamps and Output Clamp/Amplifier

The sync signal, shown in the block diagram of Figure 6, drives the R-Y and B-Y clamps which clamp the R-Y and B-Y signals to reference black during the blanking periods. The output amplifier/clamp provides this same function plus combines and amplifies the chroma and luma components for composite video output.

Application Circuit

Figure 7 illustrates the block diagram of the MC1377 and the external circuitry required for typical operation.

Figure 5. Timing Circuitry

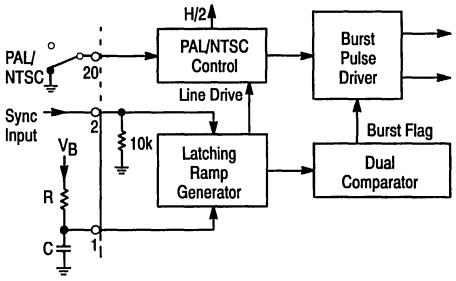


Figure 6. R-Y, B-Y and Output Amplifier Clamps

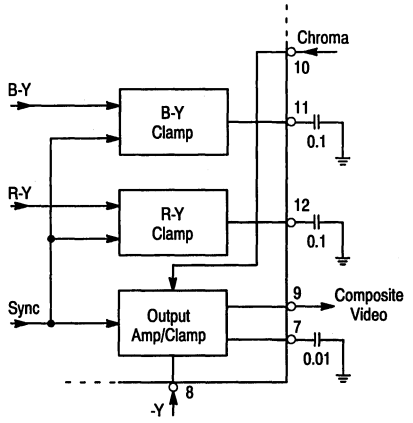


Figure 7. Block Diagram and Application Circuit

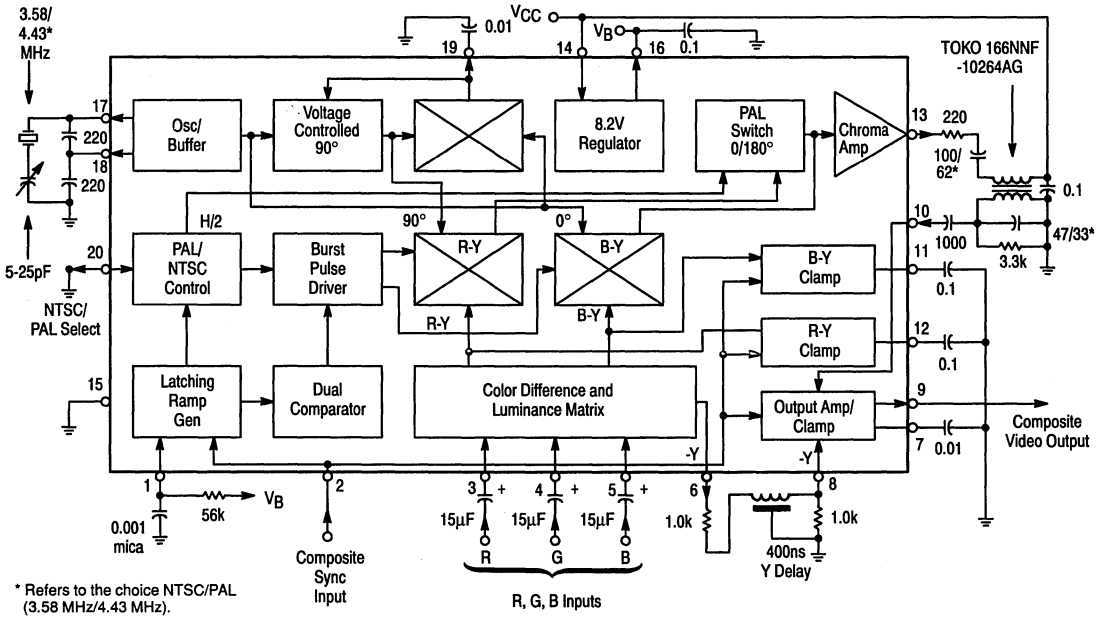
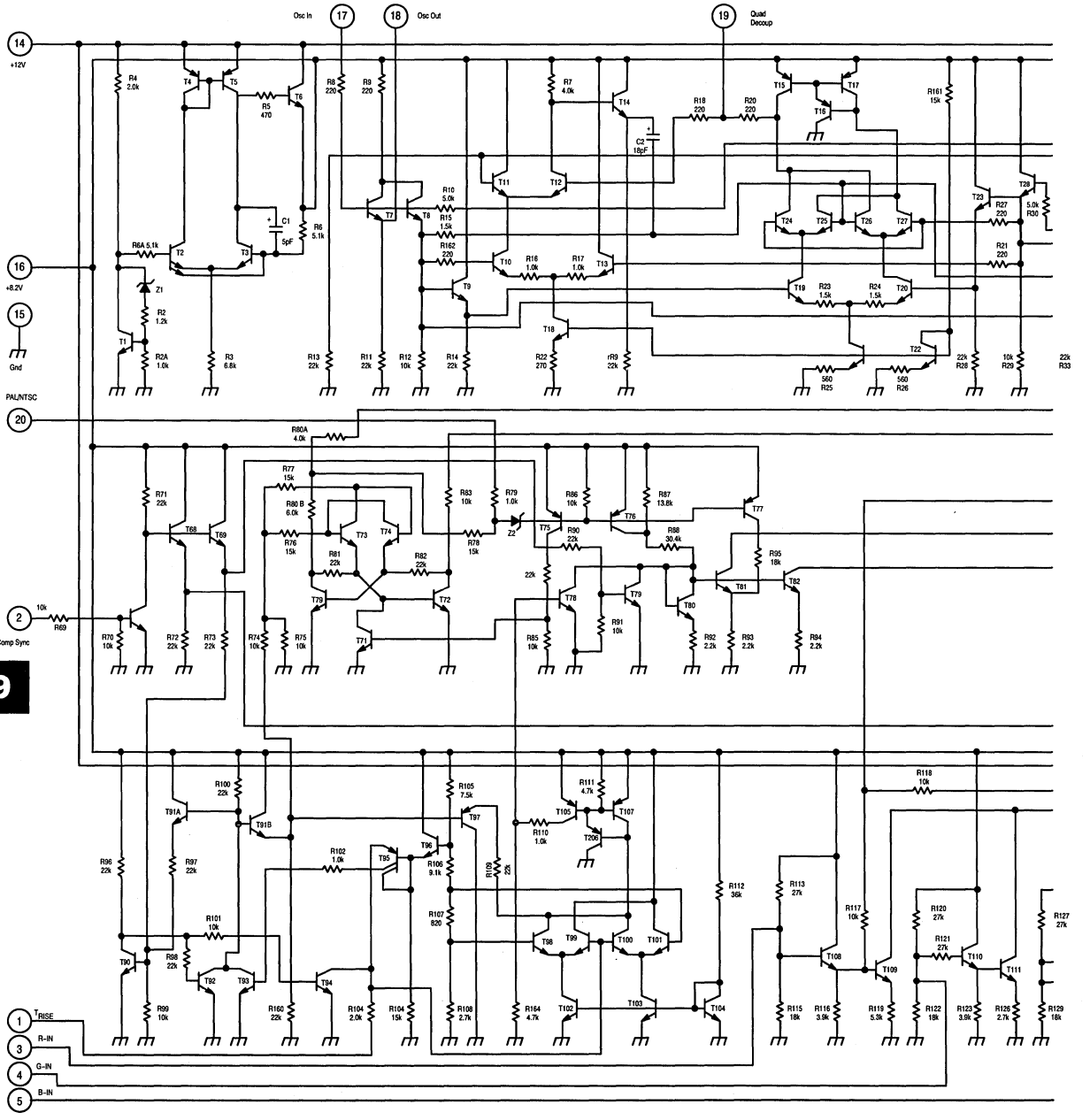


Figure 8.


14
+12V
16
+8.2V
15
Gnd
PAL/NTSC
20
2
Comp Sync
1
TRISE
3
R-IN
4
G-IN
5
B-IN
Osc In
17
18
Osc Out
19
Quad Decoup
C1
5pF
C2
18pF
Z1
Z2
R4 2.0k
R5 470
R6 5.1k
R6A 5.1k
R7 4.0k
R8 220
R9 220
R10 5.0k
R15 1.5k
R16 1.0k
R17 1.0k
R18 220
R20 220
R21 220
R22 270
R23 1.5k
R24 1.5k
R25 560
R26 560
R27 220
R28 22k
R29 10k
R30 5.0k
R33 22k
R161 15k
R162 220
R1 1.2k
R2 1.2k
R2A 1.0k
R3 6.8k
R11 22k
R12 10k
R13 22k
R14 22k
R9 22k
R80A 4.0k
R80 B 6.0k
R71 22k
R76 15k
R77 15k
R78 15k
R79 1.0k
R81 22k
R82 22k
R83 10k
R85 10k
R86 10k
R87 13.8k
R88 30.4k
R90 22k
R91 10k
R92 2.2k
R93 2.2k
R94 2.2k
R95 18k
R69 10k
R70 10k
R72 22k
R73 22k
R74 10k
R75 10k
R96 22k
R97 22k
R98 22k
R99 10k
R100 22k
R101 10k
R102 1.0k
R104 2.0k
R104 15k
R105 7.5k
R106 9.1k
R107 820
R108 2.7k
R109 22k
R110 1.0k
R111 4.7k
R112 36k
R113 27k
R115 18k
R116 3.9k
R117 10k
R118 10k
R119 5.3k
R120 27k
R121 27k
R122 18k
R123 3.9k
R126 2.7k
R127 27k
R129 18k
R160 22k
R164 4.7k
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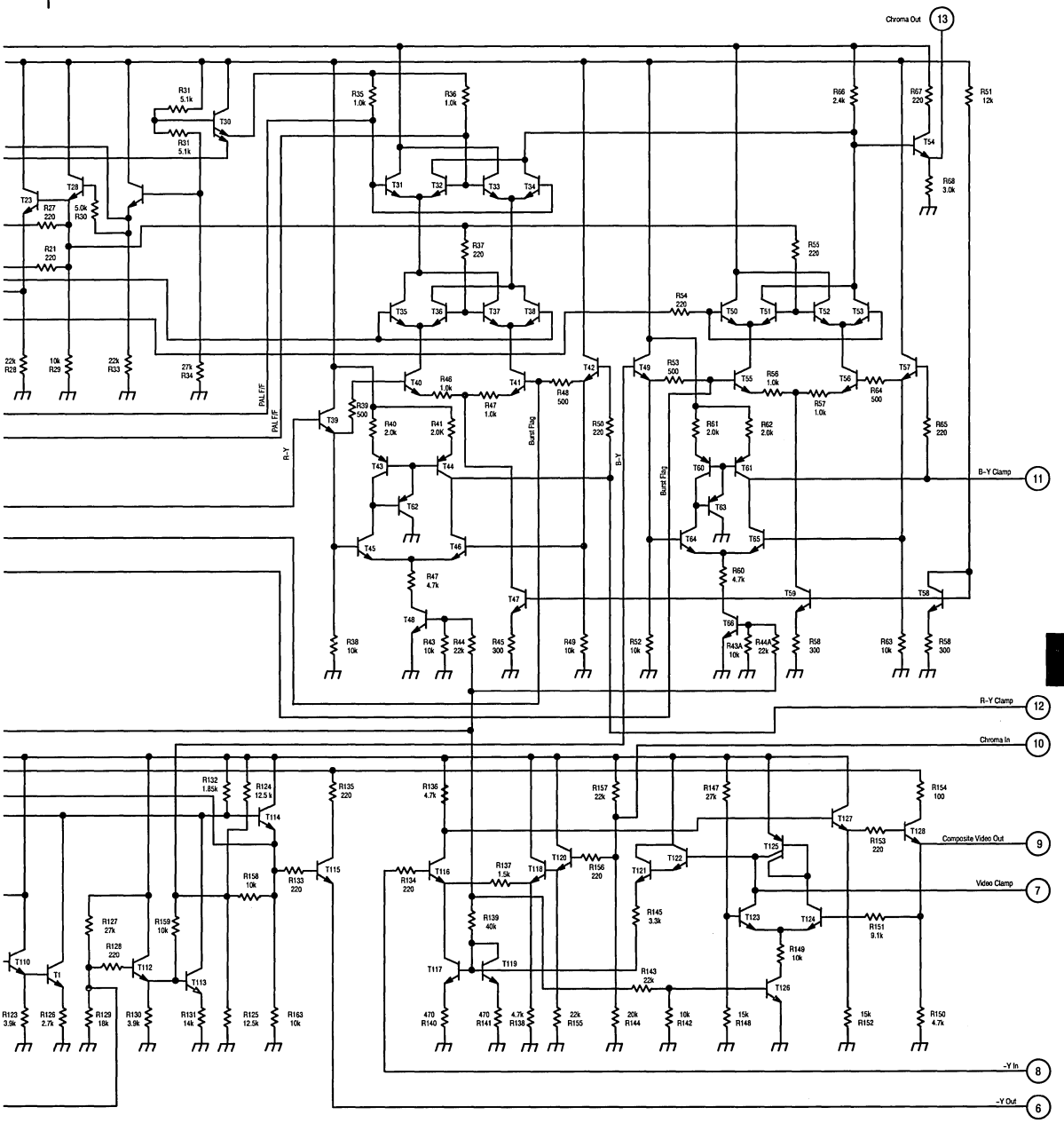
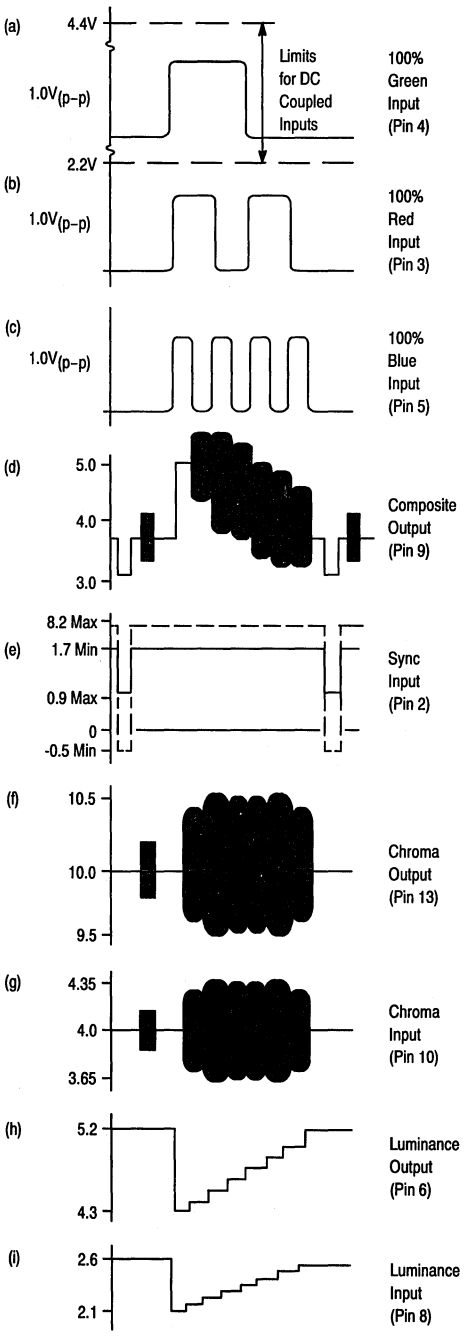
T208

Internal Schematic



APPLICATION INFORMATION

Figure 9. Signal Voltages (Circuit Values of Figure 7)



R, G, B Input Levels

The signal levels into Pins 3, 4, 5 should be 1.0 $V_{(p-p)}$ for fully saturated, standard composite video output levels as shown in Figure 9(d). The inputs require 1.0 $V_{(p-p)}$ since the internally generated sync pulse and color burst are at fixed and predetermined amplitudes.

Further, it is essential that the portion of each input which occurs during the sync interval represent black for that input since that level will be clamped to reference black in the color modulators and output stage. This implies that a refinement, such as a difference between black and blanking levels, must be incorporated in the RGB input signals.

If Y, R-Y, B-Y and burst flag components are available and the MC1377 is operating in NTSC, inputs may be as follows: the Y component can be coupled through a 15 pF capacitor to Pins 3, 4 and 5 tied together; the (–[R-Y]) component can be coupled to Pin 12 through a 0.1 μF capacitor, and the (–[B-Y]) and burst flag components can be coupled to Pin 11 in a similar manner.

Sync Input

As shown in Figure 9(e), the sync input amplitude can be varied over a wide latitude, but will require bias pull-up from most sync sources. The important requirements are:

1) The voltage level between sync pulses must be between 1.7 V and 8.2 V, see Figure 9(e).
2) The voltage level for the sync tips must be between +0.9 V and –0.5 V, to prevent substrate leakage in the IC, see Figure 9(e).
3) The width of the sync pulse should be no longer than 5.2 μs and no shorter than 2.5 μs.

For PAL operation, correctly serrated vertical sync is necessary to properly trigger the PAL divider. In NTSC mode, simplified 'block' vertical sync can be used but the loss of proper horizontal timing may cause 'top hook' or 'flag waving' in some monitors. An interesting note is that composite video can be used directly as a sync signal, provided that it meets the sync input criteria.

Latching Ramp (Burst Flag) Generator

The recommended application is to connect a close tolerance (5%) 0.001 μF capacitor from Pin 1 to ground and a resistor of 51 kΩ or 56 kΩ from Pin 1 to V_B (Pin 16). This will produce a burst pulse of 2.5 μs to 3.5 μs in duration, as shown in Figure 10. As the ramp on Pin 1 rises toward the charging voltage of 8.2 V, it passes first through a burst 'start threshold' at 1.0 V, then a 'stop threshold' at 1.3 V, and finally a ramp reset threshold at 5.0 V. If the resistor is reduced to 43 kΩ, the ramp will rise more quickly, producing a narrower and earlier burst pulse (starting approx. 0.4 μs after sync and about 0.6 μs wide). The burst will be wider and later if the resistor is raised to 62 kΩ, but more importantly, the 5.0 V reset point may not be reached in one full line interval, resulting in loss of alternate burst pulses.

As mentioned earlier, the ramp method does produce burst at full line intervals on the 'vertical porches.' If this is not desired, and the MC1377 is operating in the NTSC mode, burst flag may be applied to Pin 1 provided that the tip of the

pulse is between 1.0 Vdc and 1.3 Vdc. In PAL mode this method is not suitable, since the ramp isn't available to drive the PAL flip-flop. Another means of inhibiting the burst pulse is to set Pin 1 either above 1.3 Vdc or below 1.0 Vdc for the duration that burst is not desired.

Color Reference Oscillator/Buffer

As stated earlier in the general description, there is an on-board common collector Colpitts color reference oscillator with the transistor base at Pin 17 and the emitter at Pin 18. When used with a common low-cost tv crystal and capacitive divider, about 0.6 $V_{(p-p)}$ will be developed at Pin 17. The frequency adjustment can be done with a series 30 pF trimmer capacitor over a total range of about 1.0 kHz. Oscillator frequency should be adjusted for each unit, keeping in mind that most monitors and receivers can pull-in 1200 Hz.

If an external color reference is to be used exclusively, it must be continuous. The components on Pins 17 and 18 can be removed, and the external source capacitively coupled into Pin 17. The input at Pin 17 should be a sine wave with amplitude between 0.5 $V_{(p-p)}$ and 1.0 $V_{(p-p)}$.

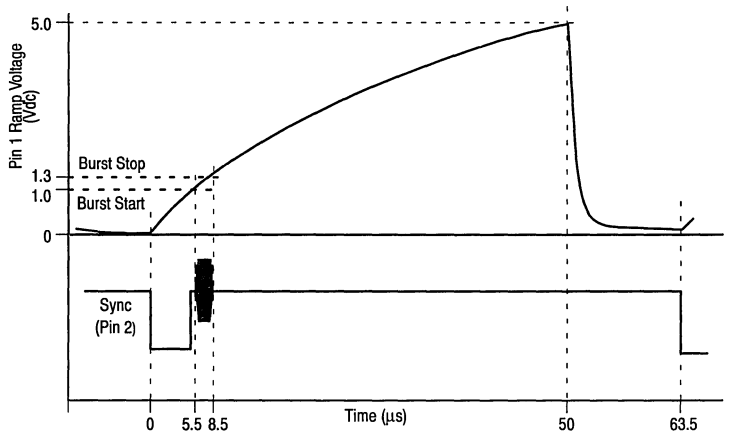
Also, it is possible to do both; i.e., let the oscillator "free run" on its own crystal and override with an external source. An extra coupling capacitor of 50 pF from the external source to Pin 17 was adequate with the experimentation attempted.

Voltage Controlled 90°

The oscillator drives the (B-Y) modulator and a voltage controlled phase shifter which produces an oscillator phase of 90° ± 5° at the (R-Y) modulator. In most situations, the result of an error of 5° is very subtle to all but the most expert eye. However, if it is necessary to adjust the angle to better accuracy, the circuit shown in Figure 11 can be used.

Pulling Pin 19 up will increase the (R-Y) to (B-Y) angle by about 0.25°/μA. Pulling Pin 19 down reduces the angle by the same sensitivity. The nominal Pin 19 voltage is about 6.3 V, so even though it is unregulated, the 12 V supply is best for good control. For effective adjustment, the simplest approach is to apply RGB color bar inputs and use a vectorscope. A simple bar generator giving R, G, and B outputs is shown in Figure 26.

Figure 10. Ramp/Burst Gate Generator



Residual Feedthrough Components

As shown in Figure 9(d), the composite output at Pin 9 for fully saturated color bars is about 2.6 $V_{(p-p)}$, output with full chroma on the largest bars (cyan and red) being 1.7 $V_{(p-p)}$. The typical device, due to imperfections in gain, matrixing, and modulator balance, will exhibit about 20 $mV_{(p-p)}$ residual color subcarrier in both white and black. Both residuals can be reduced to less than 10 $mV_{(p-p)}$ for the more exacting applications.

The subcarrier feedthrough in black is due primarily to imbalance in the modulators and can be nulled by sinking or sourcing small currents into clamp Pins 11 and 12 as shown in Figure 12. The nominal voltage on these pins is about 4.0 Vdc, so the 8.2 V regulator is capable of supplying a pull up source. Pulling Pin 11 down is in the 0° direction, pulling it up is towards 180°. Pulling Pin 12 down is in the 90° direction, pulling it up is towards 270°. Any direction of correction may be required from part to part.

White carrier imbalance at the output can only be corrected by juggling the relative levels of R, G, and B inputs for perfect balance. Standard devices are tested to be within 5% of balance at full saturation. Black balance should be adjusted first, because it affects all levels of gray scale equally. There is also usually some residual baseband video at the chroma output (Pin 13), which is most easily observed by disabling the color oscillator. Typical devices show 0.4 $V_{(p-p)}$ of residual luminance for saturated color bar inputs. This is not a major problem since Pin 13 is always coupled to Pin 10 through a bandpass or a high pass filter, but it serves as a warning to pay proper attention to the coupling network.

Figure 11. Adjusting Modulator Angle

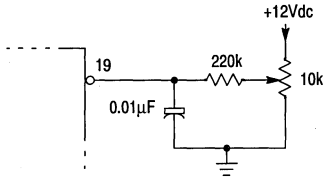


Figure 12. Nulling Residual Color in Black

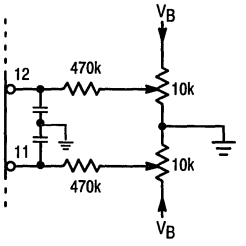
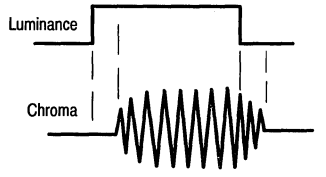


Figure 13. Delay of Chroma Information



The Chroma Coupling Circuits

With the exception of S-VHS equipped monitors and receivers, it is generally true that most monitors and receivers have color IF 6.0 dB bandwidths limited to approximately ±0.5 MHz. It is therefore recommended that the encoder circuit should also limit the chroma bandwidth to approximately ±0.5 MHz through insertion of a bandpass circuit between Pin 13 and Pin 10. However, if S-VHS operation is desired, a coupling circuit which outputs the composite chroma directly for connection to a S-VHS terminal is given in the S-VHS application (see Figure 19).

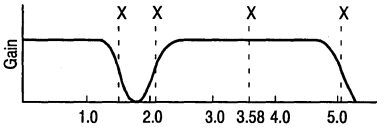
For proper color level in the video output, a ±0.5 MHz bandwidth and a midband insertion loss of 3.0 dB is desired. The bandpass circuit shown in Figure 7, using the TOKO fixed tuned transformer, couples Pin 10 to Pin 13 and gives this result. However, this circuit introduces about 350 ns of delay to the chroma information (see Figure 13). This must be accounted for in the luminance path.

A 350 ns delay results in a visible displacement of the color and black and white information on the final display. The solution is to place a delay line in the luminance path from Pins 6 to 8, to realign the two components. A normal tv receiver delay line can be used. These delay lines are usually of 1.0 kΩ to 1.5 kΩ characteristic impedance, and the resistors at Pins 6 and 8 should be selected accordingly. A very compact, lumped constant delay line is available from TDK (see Figure 25 for specifications). Some types of delay lines have very low impedances (approx. 100 Ω) and should not be used, due to drive and power dissipation requirements.

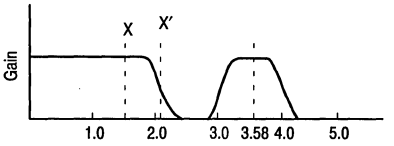
In the event of very low resolution RGB, the transformer and the delay line may be omitted from the circuit. Very low resolution for the MC1377 can be considered RGB information of less than 1.5 MHz. However, in this situation, a bandwidth reduction scheme is still recommended due to the response of most receivers.

Figure 14(a) shows the output of the MC1377 with low resolution RGB inputs. If no bandwidth reduction is employed then a monitor or receiver with frequency response shown in Figure 14(b), which is fairly typical of non-comb filtered monitors and receivers, will detect an incorrect luma sideband at X′.This will result in cross-talk in the form of chroma information in the luma channel. To avoid this situation, a simpler bandpass circuit as shown in Figure 15(a), can be used.

Figure 14. MC1377 Output with Low Resolution RGB Inputs



(a) Encoder Output with Low Resolution Inputs and No Bandpass Transformer



(b) Standard Receiver Response

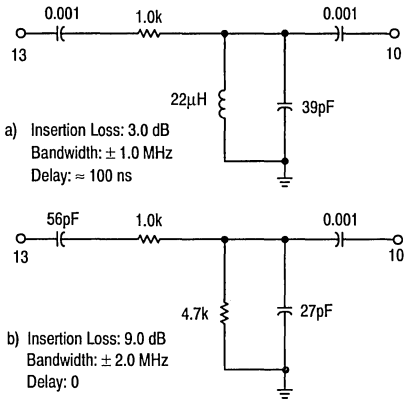
A final option is shown in Figure 15(b). This circuit provides very little bandwidth reduction, but enough to remove the chroma to luma feedthrough, and essentially no delay. There is, however, about a 9 dB insertion loss from this network.

It will be left to the designer to decide which, if any, compromises are acceptable. Color bars viewed on a good monitor can be used to judge acceptability of step luminance/chrominance alignment and step edge transients, but signals containing the finest detail to be encountered in the system must also be examined before settling on a compromise.

The Output Stage

The output amplifier normally produces about 2.0 $V_{(p-p)}$ and is intended to be loaded with 150 Ω as shown in Figure 16. This provides about 1.0 $V_{(p-p)}$ into 75 Ω, an industry standard level (RS-343). In some cases, the input to the monitor may be through a large coupling capacitor. If so, it is necessary to connect a 150 Ω resistor from Pin 9 to ground to provide a low impedance path to discharge the capacitor. The nominal average voltage at Pin 9 is over 4.0 V. The 150 Ω DC load causes the current supply to rise another 30 mA (to approximately 60 mA total into Pin 14). Under this (normal) condition the total device dissipation is about 600 mW. The calculated worst case die temperature rise is 60°C, but the typical device in a test socket is only slightly warm to the touch at room temperature. The solid copper 20-pin lead frame in a printed circuit board will be even more effectively cooled.

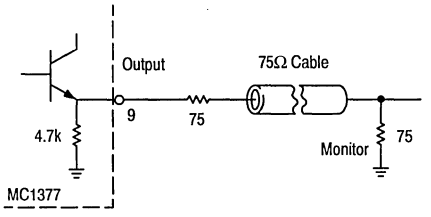
Figure 15. Optional Chroma Coupling Circuits



Power Supplies

The MC1377 is designed to operate from an unregulated 10 V to 14 V DC power supply. Device current into Pin 14 with open output is typically 35 mA. To provide a stable reference for the ramp generator and the video output, a high quality 8.2 V regulator can supply up to 10 mA for external uses, with an effective source impedance of less than 1.0 Ω. This regulator is convenient for a tracking DC reference for DC coupling the output to an RF modulator. Typical turn-on drift for the regulator is approximately –30 mV over 1 to 2 minutes in otherwise stable ambient conditions.

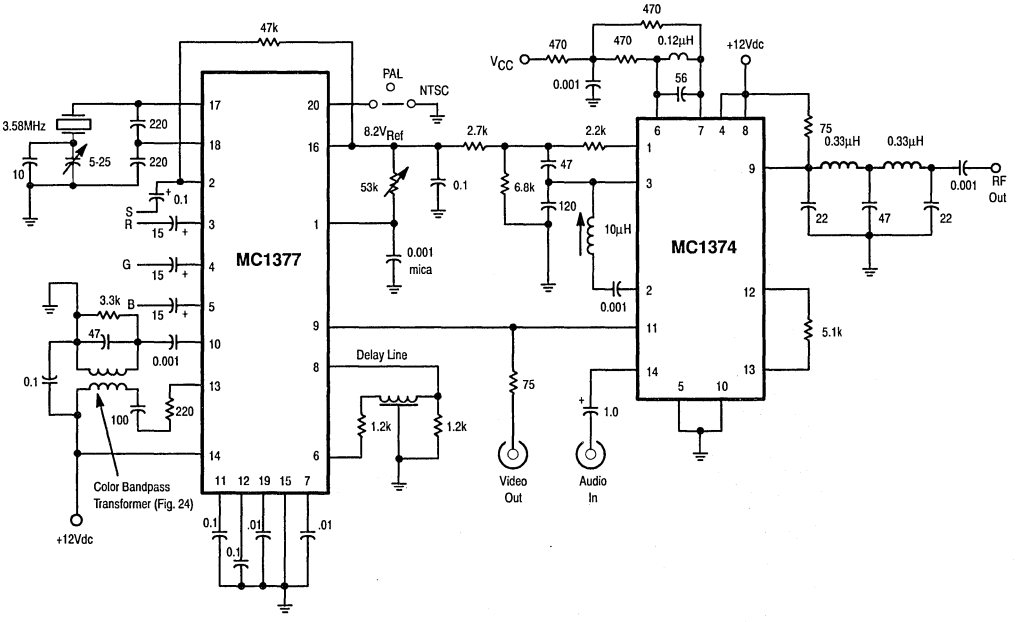
Figure 16. Output Termination



SUMMARY

The preceding information was intended to detail the application and basis of circuit choices for the MC1377. A complete MC1377 application with the MC1374 VHF modulator is illustrated in Figure 17. The internal schematic diagram of the MC1377 is provided in Figure 8. If further assistance is needed, contact Motorola Linear Applications Engineering.

Figure 17. Application with VHF Modulator



APPLICATIONS INFORMATION

S-VHS

In full RGB systems (Figure 18), three information channels are provided from the signal source to the display to permit unimpaired image resolution. The detail reproduction of the system is limited only by the signal bandwidth and the capability of the color display device. Also, higher than normal sweep rates may be employed to add more lines within a vertical period and three separate projection picture tubes can be used to eliminate the 'shadow mask' limitations of a conventional color CRT.

Figure 21 shows the 'baseband' components of a studio NTSC signal. As in the previous example, energy is concentrated at multiples of the horizontal sweep frequency. The system is further refined by precisely locating the color subcarrier midway between luminance spectral components. This places all color spectra between luminance spectra and can be accomplished in the MC1377 only if 'full interlaced' external color reference and sync are applied. The individual components of luminance and color can then be separated by the use of a comb filter in the monitor or receiver. This technique has not been widely used in consumer products, due to cost, but it is rapidly becoming less expensive and more common. Another technique which is gaining popularity is S-VHS (Super VHS).

In S-VHS, the chroma and luma information are contained on separate channels. This allows the bandwidth of both the chroma and luma channels to be as wide as the monitors ability to reproduce the extra high frequency information. An output coupling circuit for the composite chroma using the TOKO transformer is shown in Figure 19. It is composed of the bandpass transformer and an output buffer and has the frequency performance shown in Figure 20. The composite output (Pin 9) then produces the luma information as well as composite sync and blanking.

Figure 18. Spectra of a Full RGB System

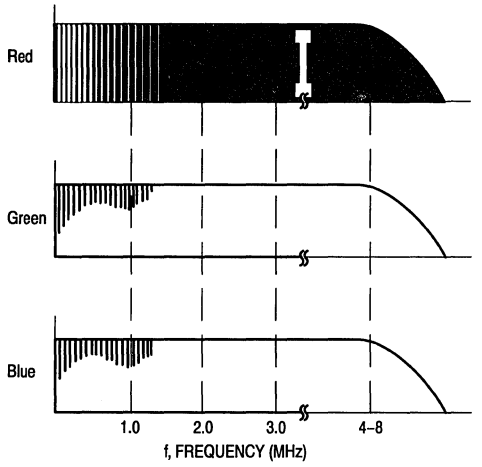
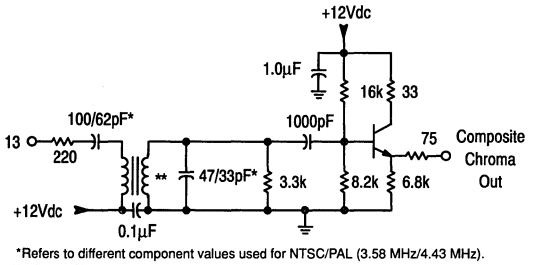
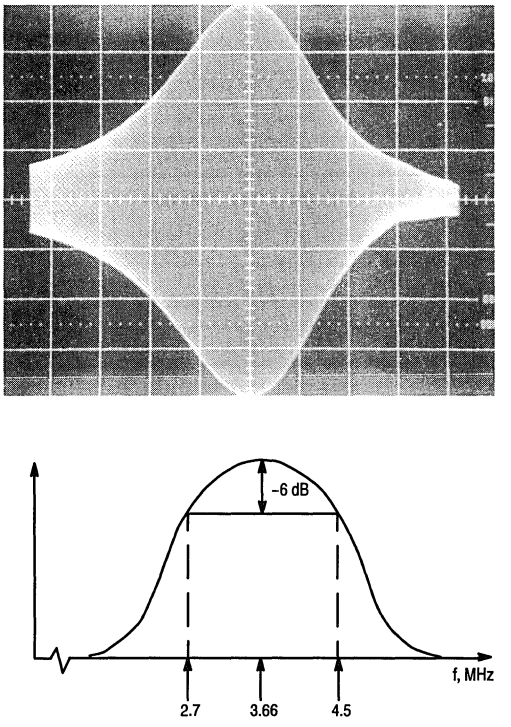


Figure 19. S-VHS Output Buffer



*Refers to different component values used for NTSC/PAL (3.58 MHz/4.43 MHz).
**Toko 166NNF-1026AG

Figure 20. Frequency Response of Chroma Coupling Circuit



I/Q System versus (R-Y)/(B-Y) System

The NTSC standard calls for unequal bandwidths for I and Q (Figure 21). The MC1377 has no means of processing the unequal bandwidths because the I and Q axes are not used (Figure 22) and because the outputs of the (R-Y) and the (B-Y) modulators are added before being output at Pin 13. Therefore, any bandwidth reduction intended for the chroma information must be performed on the composite chroma information. This is generally not a problem, however, since most monitors compromise the standard quite a bit.

Figure 23 shows the typical response of most monitors and receivers. This figure shows that some crosstalk between luma and chroma information is always present. The acceptability of the situation is enhanced by the limited ability of the CRT to display information above 2.5 MHz. If the signal from the MC1377 is to be used primarily to drive conventional non-comb filtered monitors or receivers, it would be best to reduce the bandwidth at the MC1377 to that of Figure 23 to lessen crosstalk.

Figure 21. NTSC Standard Spectral Content

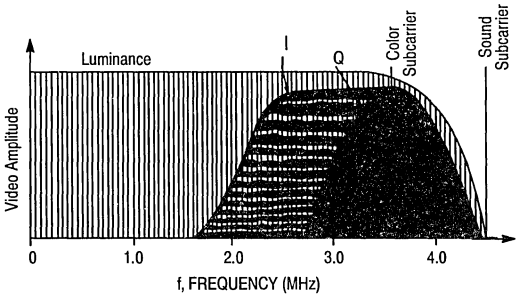


Figure 22. Color Vector Relationship (Showing Standard Colors)

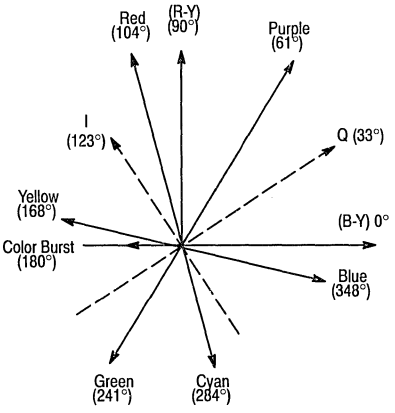


Figure 23. Frequency Response of Typical Monitor/TV

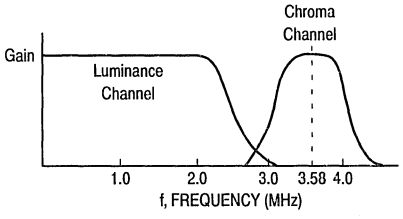
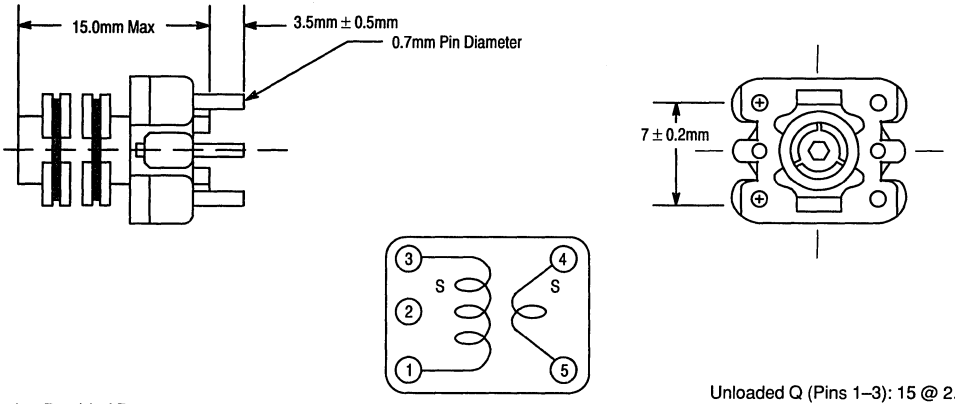


Figure 24. A Prototype Chroma Bandpass Transformer
Toko Sample Number 166NNF-10264AG

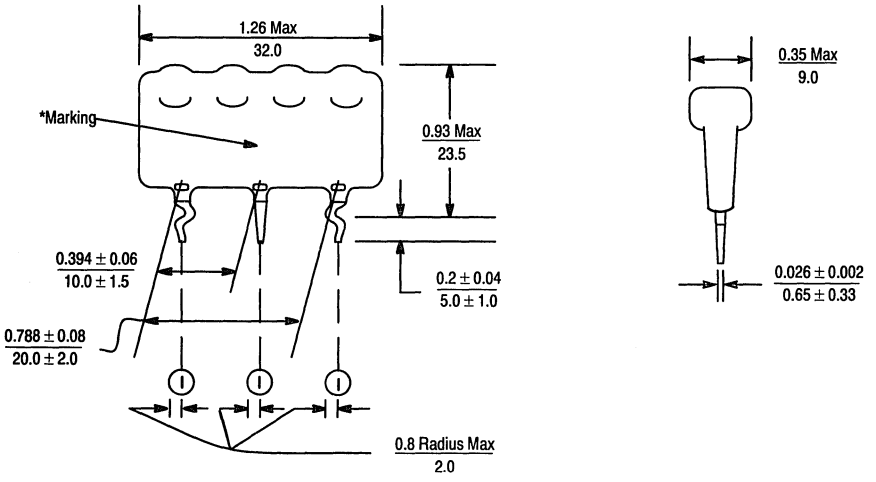


(Drawing Provided By:
Toko America, Skokie, IL)

Connection Diagram
Bottom View

Unloaded Q (Pins 1–3): 15 @ 2.5 MHz
Inductance: 30 µH ± 10% @ 2.5 MHz
Turns: 60 (each winding)
Wire: #38 AWG (0.1 m/m)

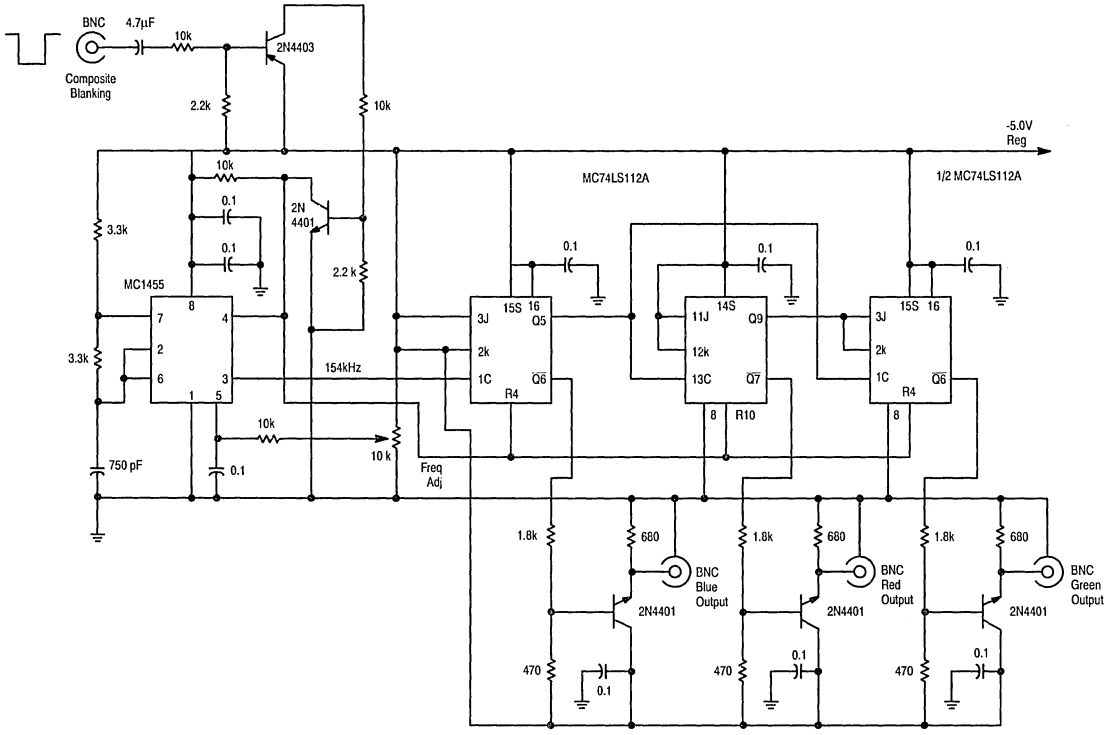
Figure 25. A Prototype Delay Line
TDK Sample Number DL122301D-1533



*Marking: Part Number, Manufacturer's Identification, Date Code and Lead Number.
Skokie, IL (TDK Corporation of America)

Item	Specifications
Time Delay	400 ns ± 10%
Impedance	1200 Ω ± 10%
Resistance	Less Than 15 Ω
Transient Response with 20 ns Rise Time Input Pulse	Preshoot: 10% Max
	Overshoot: 10% Max
	Rise Time: 120 ns Max
Attenuation	3 dB Max at 6.0 MHz

Figure 26. RGB Pulse Generator



RGB Pulse Generator Timing Diagram for NTSC

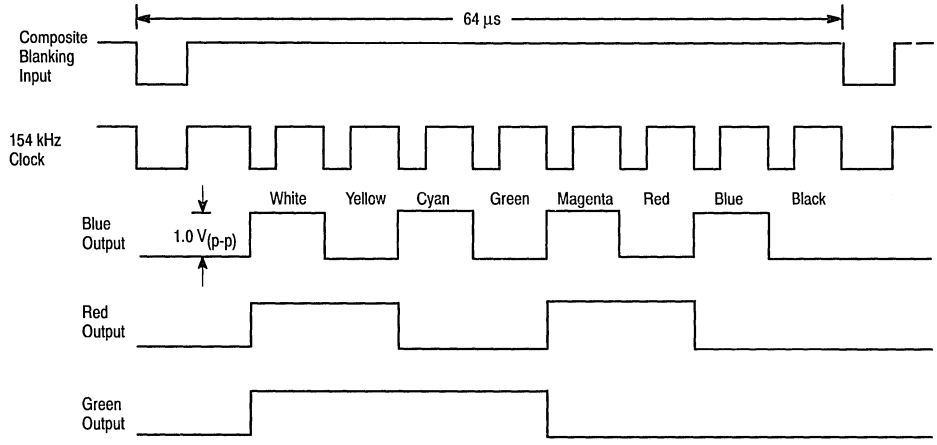
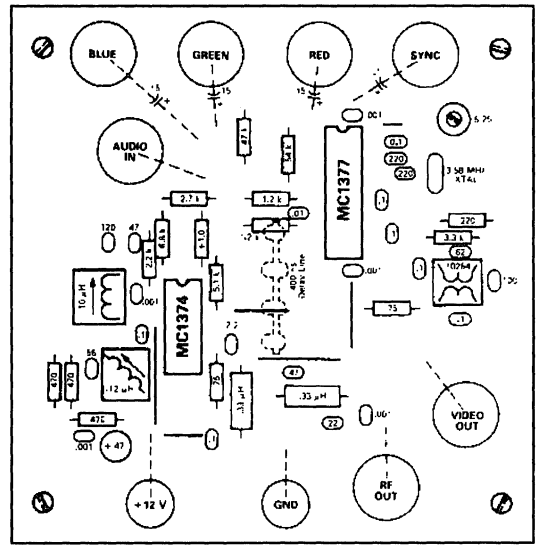


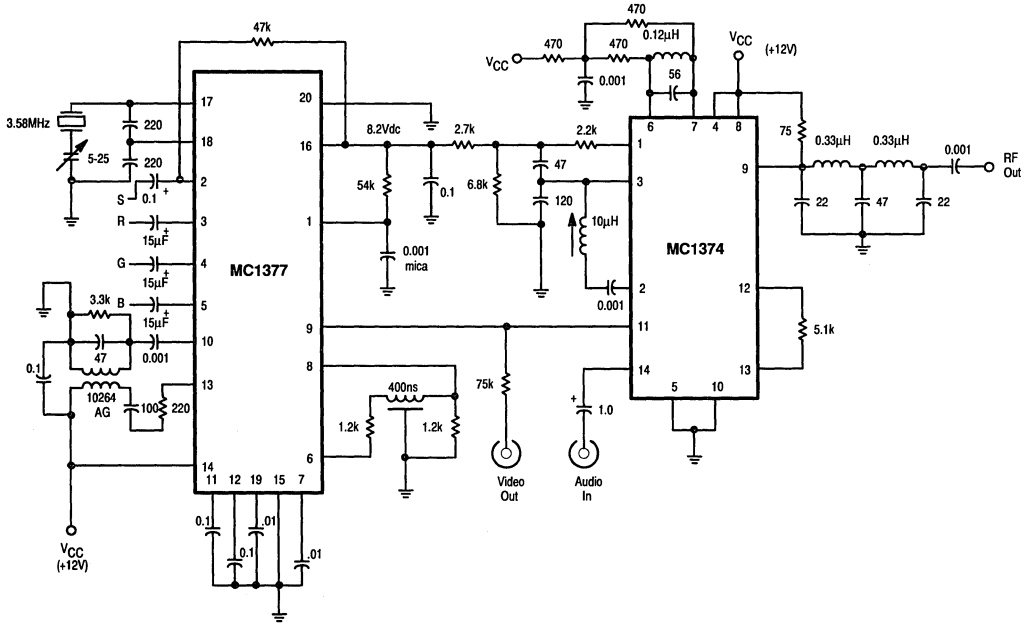
Figure 27. Printed Circuit Boards for the MC1377

(CIRCUIT SIDE)



(COMPONENT SIZE)

Figure 28. Color TV Encoder — Modulator



MC1378

COLOR TELEVISION COMPOSITE VIDEO OVERLAY SYNCHRONIZER

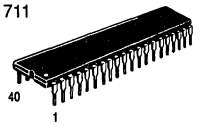
Advance Information

Color Television Composite Video Overlay Synchronizer

The MC1378 is a bipolar composite video overlay encoder and microcomputer synchronizer. The MC1378 contains the complete encoder function of the MC1377, i.e. quadrature color modulators, RGB matrix, and blanking level clamps, plus a complete complement of synchronizers to lock a microcomputer-based video source to any remote video source. The NC1378 is especially tailored to work with the Motorola RMS (Raster Memory System), but it can be applied to other controllable video sources. It can be used as a local system timing and encoding source, but it is most valuable when used to lock the microcomputer source to a remotely originated video signal.

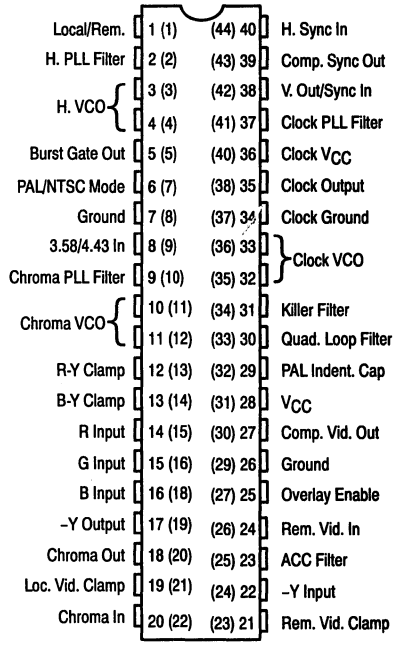
- Contains All Needed Reference Oscillators
- Can Be Operated in PAL or NTSC Mode, 625 or 525 Line
- Wideband, Full-Fidelity Color Encoding
- Local or Remote Modes of Operation
- Minimal External Components
- Designed to Operate from 5.0 V supply
- Will Work with Non-standard Video

P SUFFIX
PLASTIC PACKAGE
CASE 711



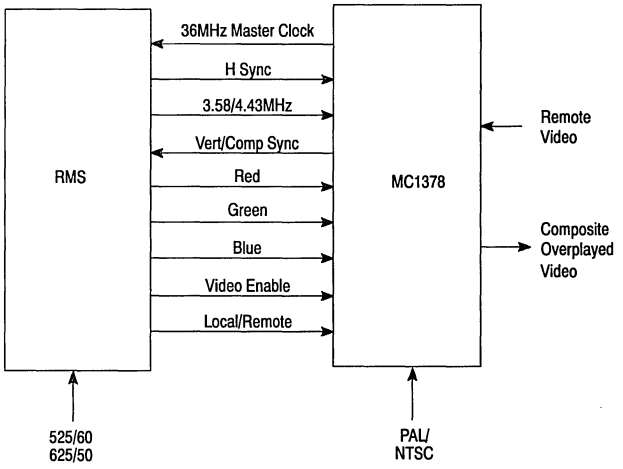
FN SUFFIX
PLASTIC PACKAGE
CASE 777
(PLCC-44)

PIN CONNECTIONS



* ( ) PLCC Pin Assignments

Figure 1. Block Diagram Typical Application



ORDERING INFORMATION

Device	Temperature Range	Package
MC1378P	0° to +70°C	Plastic DIP
MC1378FN		PLCC-44

9

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	6.0	Vdc
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	−65 to +150	°C
Junction Temperature	$T_{J(max)}$	150	°C
Power Dissipation, Package Derate above 25°C	P_D	1.25 10	W mW/°C

RECOMMENDED OPERATING CONDITIONS

Condition	Pin No.	Value	Unit
Supply Voltage	28, 36	5.4 ± 0.25	Vdc
RGB Input for 100% Saturation	14, 15, 16	1.0	Vp-p
Color Oscillator Input Level	8	0.5	Vp-p
Video Input, Positive	24	1.0	Vp-p

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, T_A = 25°C, circuit of Figure 4 or 5)

Characteristics		Pin No.	Min	Typ	Max	Unit
Supply Current		28, 36	—	100	—	mAdc
Video Output, Open Circuit, Positive		27	—	2.0	9.4	V_{p-p}
Modulation Angle (R − Y) to (B − Y)		—	87	90	93	Degrees
RGB Input Impedance		14, 15, 16	—	10	—	kΩ
Local/Remote Switch (TTL)	High Low	1	—	Remote Local	—	—
Horizontal Sync Input, Negative Going	(TTL)	40	—	4.3	—	V_{p-p}
Vertical Sync Output, Negative Going, Remote Mode	(TTL)	38	—	4.3	—	V_{p-p}
Composite Sync Output, Negative Going	(TTL)	39	—	4.3	—	V_{p-p}
Burst Gate Output, Positive Going	(TTL)	5	—	4.3	—	V_{p-p}

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Description of Operation — Refer to Figures 3, 4

Remote Mode	Local Mode
The incoming remote video signal (Pin 24) supplies all synchronizing information. A discussion of the function of the phase detectors helps to clarify the lockup method: PD1 — locks the internally counted-down 4 MHz horizontal VCO to the incoming horizontal sync. It is fast acting, to follow VCR source fluctuations. PD2 — locks the 36 MHz clock VCO, which is divided down by the RMS, to the divided down horizontal VCO. PD3 — is a gated phase detector which locks the 14 MHz crystal oscillator, divided by 4, to the incoming color burst. PD4 — controls an internal phase shifter to assure that the outgoing color burst is the same phase as incoming burst at PD3. PD5 — not used in REMOTE MODE	The MC1378 and RMS combine to provide a fully synchronized standard signal source. In this case, composite sync must be supplied by the RMS or other time base system. In the MC1378 the phase detectors operate as follows: PD1 — locks the internally counted-down 4 MHz horizontal VCO to a Horizontal Sync signal (at Pin 40) from the RMS (counted down from 36 MHz) PD2 — not used in LOCAL MODE. PD3 — not used in LOCAL MODE. PD4 — active, but providing an arbitrary phase shift setting between the color oscillator and the output burst phase. PD5 — locks the 36 MHz clock VCO (which is divided down by the RMS) to the 14 MHz (crystal) color oscillator. The 14 MHz is, therefore, the system standard in LOCAL MODE, and is not DC controlled.
Vertical lock is obtained by continuously resetting the sync generator in the RMS with separated vertical sync from the MC1378, Pin 38. This signal is TTL level vertical block sync, negative going. The horizontal sync from the RMS to Pin 40 is also TTL level with sync negative going. The local/remote switch, Pin 1, is in local mode when grounded, remote mode when taken to 5.0 V. The overlay control, Pin 25, has an analog characteristic, centered about 1.0 V, which allows fading from local to remote.	**COMPOSITE VIDEO GENERATION** The color encoding at the RGB signals is done exactly as in the MC1377. Composite chroma is looped out at Pins 18 and 20 to allow the designer to choose band shaping. Luminance is similarly brought out (Pins 17 and 22) to permit installation of the appropriate delay. Composite sync output, Pin 39, and burst gate output, Pin 5, are provided for convenience only.

Figure 2. MC1378 Internal Block Diagram

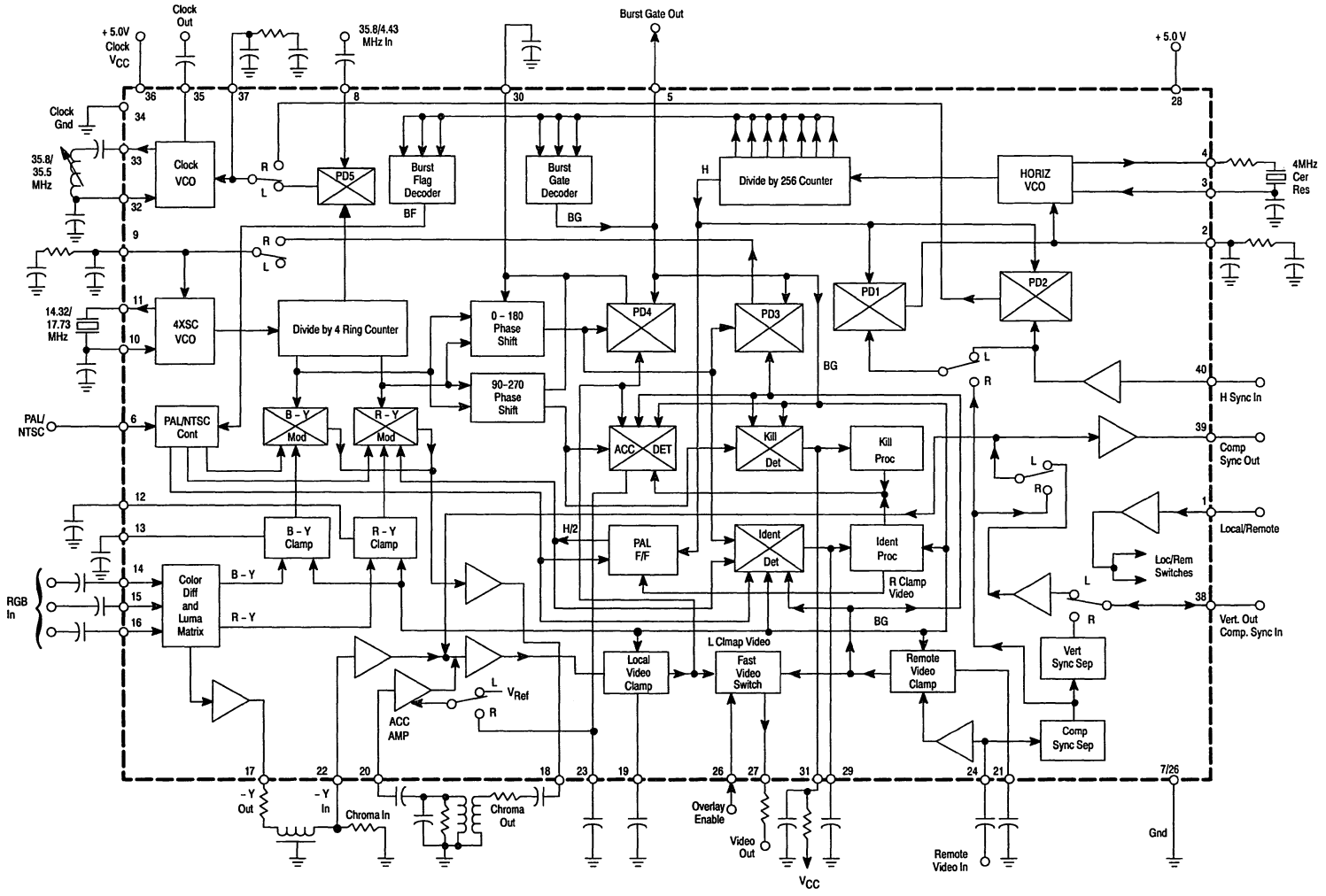


Figure 3. Remote Mode

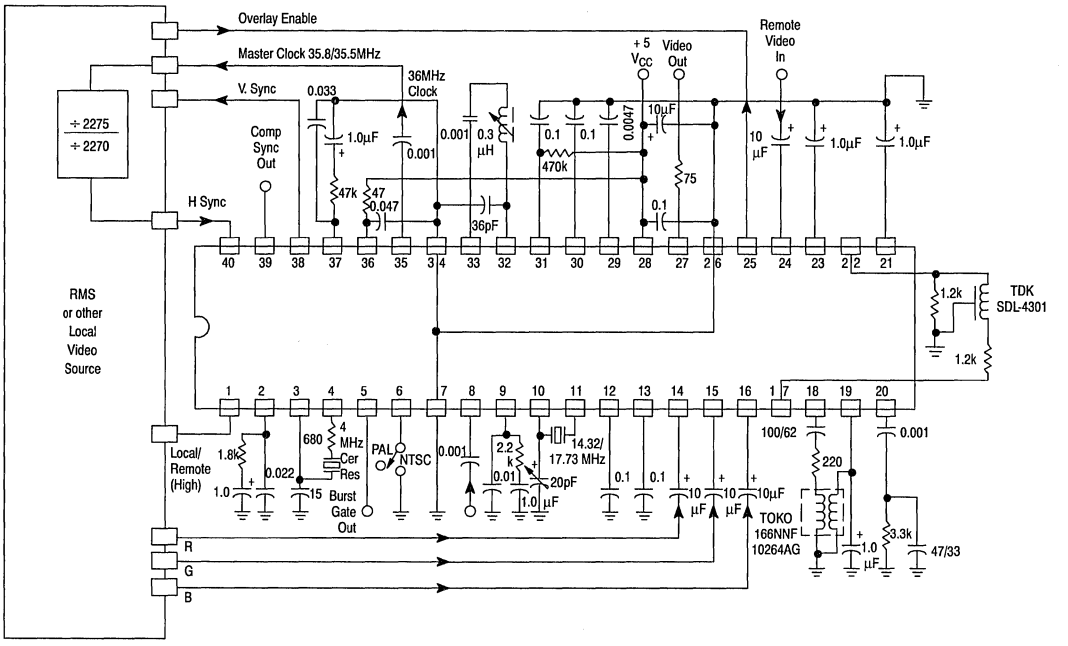
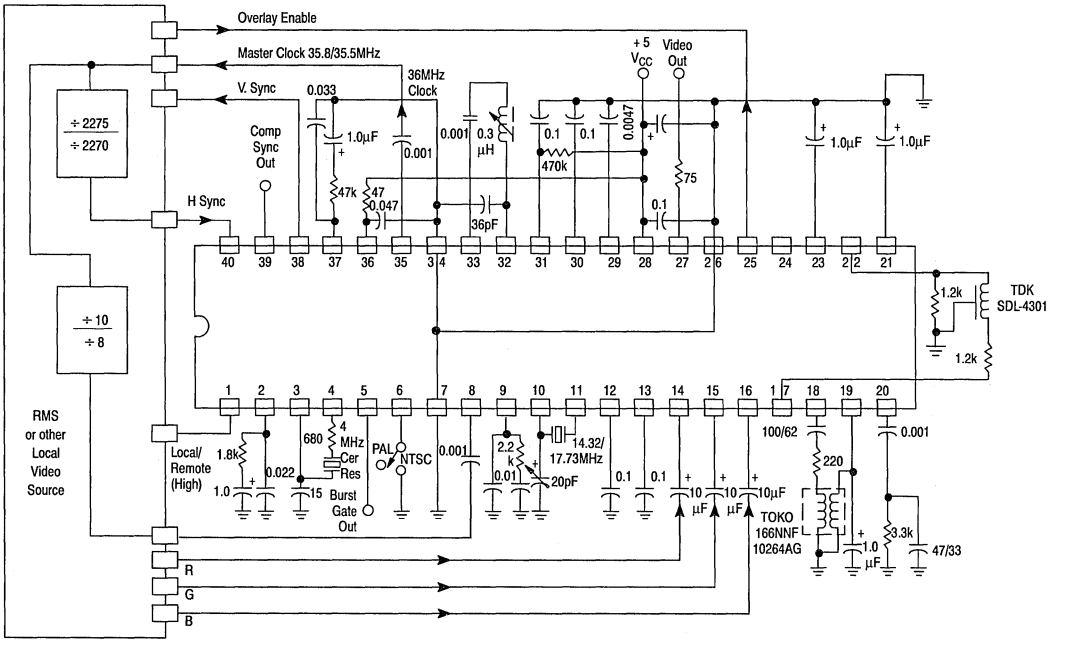


Figure 4. Local Mode



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC1388

Advance Information

Geometry Correction Waveform Generator

WAVEFORM GENERATOR IC FOR MONITOR APPLICATIONS

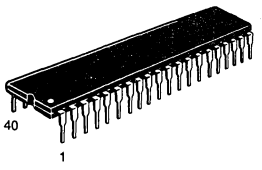
The MC1388 is a bipolar integrated circuit designed to be used with the control circuitry for geometry correction in monitors and HDTV receivers. The function of the integrated circuit is to generate the required voltage waveforms that will be applied to the control circuitry. The control circuitry will apply them in the proper amplitude and combination for use in modulating the horizontal and vertical scan currents.

Features:

- Multistandard Operation Capable (10 kHz ≤ f_H ≤ 63 kHz)(45 ≤ f_V ≤ 120 Hz)
- Constant Amplitude Outputs, Independent of Frequency
- Complementary Output Waveforms (Horizontal Parabola, Horizontal Cubic, Vertical Ramp, Vertical Parabola and Sine Functions)
- Three Input Multiplier
- Minimum of External Components Necessary
- Standard Supplies (±5 Vdc)

Functions (Ten Waveforms):

- Horizontal Ramp and Vertical Ramp
- Horizontal Parabola and Vertical Parabola
- Horizontal Cube and Cube with Accessible Inputs (H'in, V'in)
- ± Sine H
- ± Sine 2 H
- ± Sine V
- ± Sine 2 V



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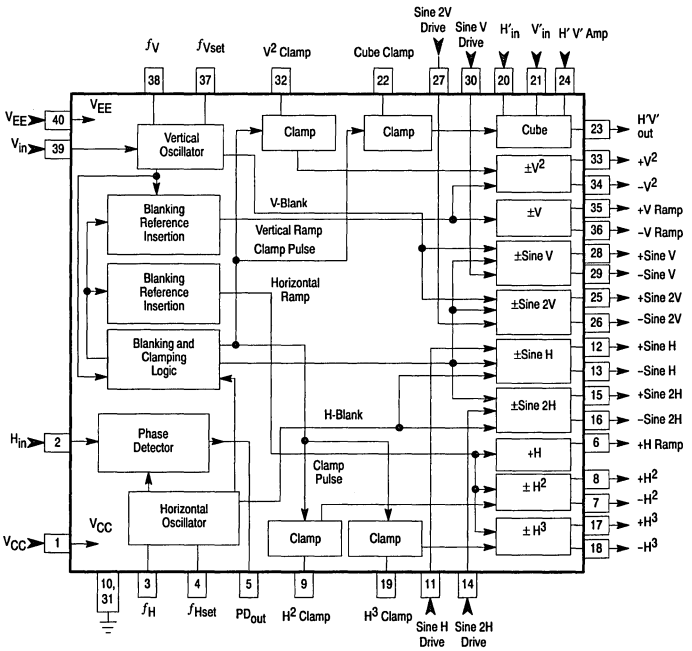
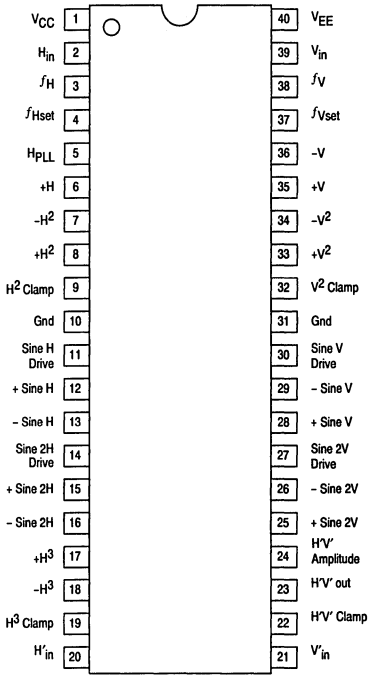
CASE 711

SIMPLIFIED BLOCK DIAGRAM



PIN CONNECTIONS
(Top View)

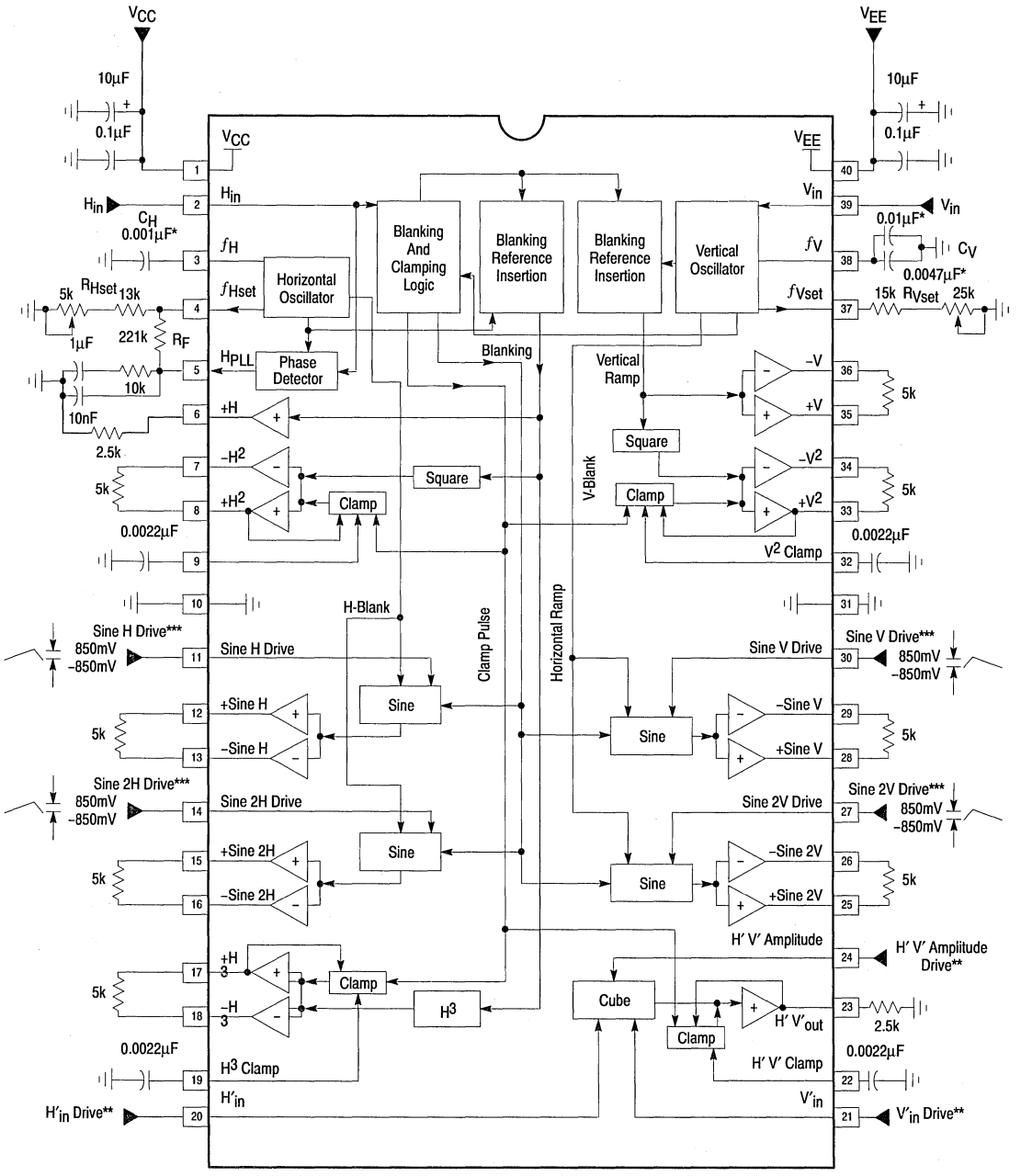


ORDERING INFORMATION

Device	Temperature Range	Package
MC1388P	0° to +70°C	Plastic DIP

9

Figure 1. Test Circuit of the MC1388



* Polystyrene
** The three input multiplier was tested by applying a DC voltage to two of the inputs while applying a 1.25 Vp-p ramp input to the third.
*** The inputs applied to the Sine Drive Inputs is a voltage ramped from –850 mV to +850 mV in 10 mV steps.

MAXIMUM OPERATING CONDITIONS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC} V_{EE}	+6.0 −6.0	Vdc
Input Voltage Maximum Minimum	V_{in}, H_{in}, H'_{in}, V'_{in}, H′ V′ Amplitude	 V_{CC} +0.5 V_{EE} −0.5	Vdc
Storage Temperature	T_{stg}	−65 to +150	°C
Junction Temperature	T_J	+150	°C

RECOMMENDED OPERATING CONDITIONS

Characteristics	Pins(s)	Symbol	Value	Unit
Power Supply Voltage	1 40	V_{CC} V_{EE}	+4.5 to +5.5 −5.5 to −4.5	Vdc
Horizontal Sync Frequency (see Figure 8) Maximum Minimum Pulse Width: Maximum Minimum Pulse Amplitude: Maximum Voltage (Tip) Minimum Voltage (Baseline) Minimum Threshold: Tip Baseline	2	H_{in}	 63 10 <1.0/(2.0f_H) 2.0 V_{CC} V_{EE} +0.5 V_{CC}/2.0 +0.2 V_{CC}/2.0 +0.2	k Hz µs Vdc
Vertical Sync Frequency (see Figure 8) Maximum Minimum Pulse Width: Maximum Minimum Pulse Amplitude: Maximum Voltage (Tip) Minimum Voltage (Baseline) Minimum Threshold: Tip Baseline	39	V_{in}	 120 45 <1.0/(2.0f_V) 2.0 V_{CC} V_{EE} +0.5 V_{CC}/2.0 +0.2 V_{CC}/2.0 +0.2	Hz µs Vdc
Sine H Drive Sine 2H Drive Sine V Drive Sine 2V Drive	11 14 30 27	Sine H Drive Sine 2H Drive Sine V Drive Sine 2V Drive	−0.85 to +0.85	Vdc
H'_{in} V'_{in} H'_{in} V'_{in} Amplitude	20 21 24	H'_{in} V'_{in} H'_{in} V'_{in} Amplitude	−1.25 to +1.25	Vdc
Peak Load Current	6, 7, 8, 12, 13, 15, 16 17, 18, 23, 25, 26, 28 29, 33, 34 35, 36	I_L	5.0	mA
Ambient Temperature		T_A	0 to +70	°C

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ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 V, V_{EE} = –5.0 V, R_L = 2.5 kΩ, T_A =25°C, f_H = 31,250 Hz, f_V = 1562.5 Hz, see Figure 1, unless otherwise noted.)

Characteristics	Pin(s)	Symbol	Min	Typ	Max	Unit
Supply Current V_{CC} = +5.0 Vdc V_{EE} = –5.0 Vdc	1 40	I_{CC} I_{EE}	29 –50	33 –42	41 –38	mA
Output DC Offset, (All outputs when blanked)	6, 7, 8, 12, 13, 15, 16 17, 18, 23, 25, 26, 28 29, 33, 34 35, 36		–100	±8	100	mV
Pull-In Range Hold In Range (C_H = 1.0 nF, R_F = 221 kΩ, H_{PLL} filter shown)	5	H_{PLL}	±1.5 ±1.5	— ±4.5	— —	kHz
Horizontal Ramp — Amplitude — Non-Symmetry Horizontal Parabola — Amplitude — Non-Symmetry	6 7,8	+H $\pm H^2$	4.4 — 2.2 —	5.0 — 2.6 —	5.3 2.0 3.1 12	Vp-p % Vp–p %
±Sine H — Amplitude (No DC Offset Input) — Zero Crossing Phase Error (Pin 11 Drive as shown in Figure 1)	12, 13	±Sine H	2.8 —	4.0 —	5.6 25	Vp-p Deg
±Sine 2H — Amplitude (No DC Offset Input) — Zero Crossing Phase Error (Pin 14 Drive as shown in Figure 1)	15, 16	±Sine 2H	2.8 —	4.0 —	5.6 25	Vp-p Deg
Horizontal Cubic — Amplitude — Non-Symmetry	17, 18	$\pm H^3$	4.1 —	5.0 —	5.9 12	Vp-p %
±Sine 2V — Amplitude (No DC Offset Input) — Zero Crossing Phase Error (Pin 27 Drive as shown in Figure 1)	25, 26	±Sine 2V	2.8 —	4.0 —	5.6 25	Vp-p Deg
±Sine V — Amplitude (No DC Offset Input) — Zero Crossing Phase Error (Pin 30 Drive as shown in Figure 1)	28, 29	±Sine V	2.8 —	4.0 —	5.6 25	Vp-p Deg
Vertical Parabola — Amplitude — Non-Symmetry	33, 34	$\pm V^2$	2.2 —	2.5 —	3.1 12	Vp-p %
Vertical Ramp — Amplitude — Non-Linearity	35, 36	±V	4.4 —	5.0 —	5.3 2.0	Vp-p %
H′ V′$_{out}$ — Amplitude — Non-Linearity	23	H′ V′$_{out}$	4.2 —	4.8 —	5.4 12	Vp-p %
H′$_{in}$ V′$_{in}$ H′ V′ — Amplitude — Multiplication Factor	20, 21, 24	H′$_{in}$ V′$_{in}$ H′ V′ Amplitude	—	1.0	—	V/V

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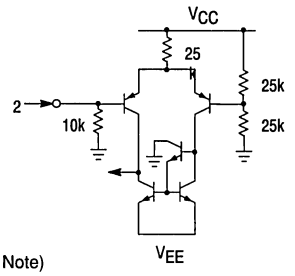
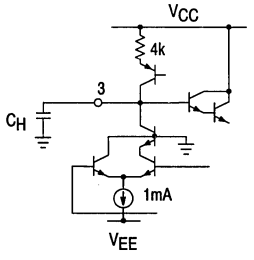
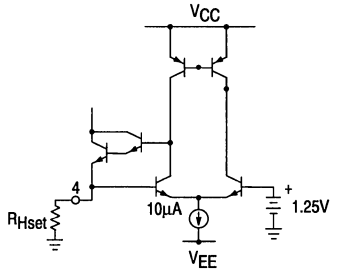
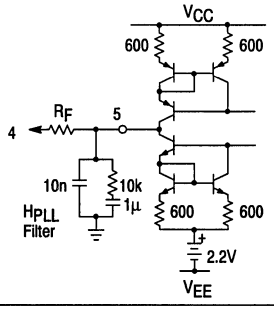
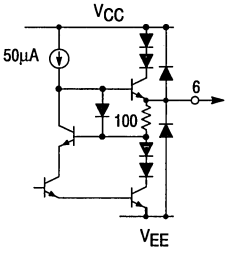
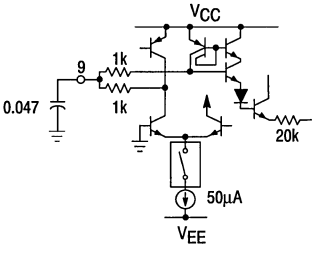
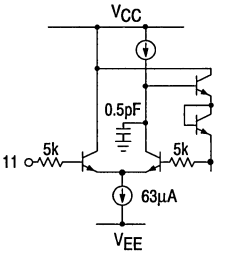
PIN DESCRIPTIONS

Pin	Symbol	Internal Equivalent Circuit	Description
1	V_{CC}		Positive Rail Voltage. Requires 33 mA at +4.5 < Vdc < +5.5
2	H_{in}	 (* See Note)	Positive Horizontal Flyback input. Input impedance is nominally 10 kΩ. Threshold is at $V_{CC}/2$. See Figure 2.
3	f_H		Horizontal Oscillator Capacitor (C_H). The charge and discharge rate of the capacitor voltage determines the horizontal frequency. Charging current set predominantly by R_{Hset} (Pin 4).
4	f_{Hset}		Horizontal Charge Current Set. An internally regulated 1.25 Vdc, and the external resistance (R_{Hset}) at this pin determines the horizontal free run charging current. Also, the feedback current from the H_{PLL} filter is input at this pin.
5	H_{PLL}		Horizontal Phase Detector output pin. An external filter circuit between this pin and Pin 5 determines the selectivity of the phase detector and provides the feedback path for the horizontal phase locked loop.

* All pins except (V_{CC} and V_{EE}) have ESD diodes between V_{CC} and V_{EE}.

PIN DESCRIPTIONS

Pin	Symbol	Internal Equivalent Circuit	Description
6	+H		Horizontal Ramp output.
7	$-H^2$	(See Pin 6)	Complement Horizontal Parabola output.
8	$+H^2$		Horizontal Parabola output. The squared result of the positive horizontal ramp.
9	H^2clamp		Horizontal Parabola Clamping pin. An external capacitor works to cancel DC offset. Typically coupled to ground with a 0.047 µF capacitor.
10	Gnd		Ground Connection.
11	Sine H Drive		Sine H Drive. A ramp waveform input here will produce a sine wave output (at Pins 12 and 13) with frequency varying with input ramp amplitude, and phase varying with ramp DC offset. Dynamic input impedance is nominally greater than 1.0 MΩ.
12	+Sine H	(See Pin 6)	+Sine H output. The sine wave output developed from the input at Pin 11.
13	–Sine H		–Sine H output. A 180° phase shifted version of +Sine H.
14	Sine 2H Drive	(See Pin 11)	Sine 2H Drive. A ramp waveform input here will produce a sine wave output (at Pins 15 and 16) with frequency varying with input ramp amplitude and phase varying with ramp DC offset. Dynamic input impedance is nominally greater than 1.0 MΩ.
15	+Sine 2H	(See Pin 6)	+Sine 2H output. The sine wave output developed from the input at Pin 14.

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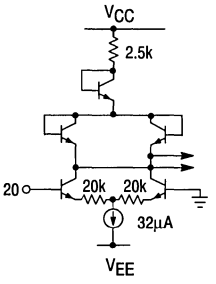
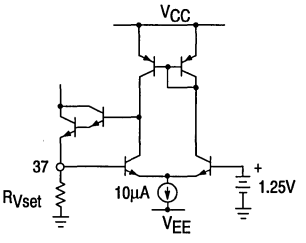
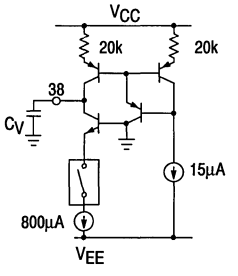
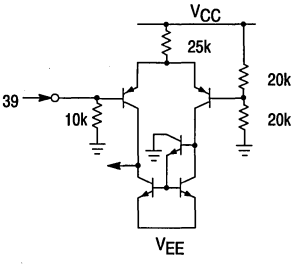
PIN DESCRIPTIONS

Pin	Symbol	Internal Equivalent Circuit	Description
16	–Sine 2H	(See Pin 6)	–Sine 2H output. A 180° phase shifted version of +Sine 2H.
17	$+H^3$		Horizontal Cubic output.
18	$-H^3$		Complement Horizontal Cubic output.
19	H^3clamp	(See Pin 9)	Cubic Clamping pin. An external capacitor works to cancel DC offset. Typically coupled to ground with a 0.047 µF capacitor.
20	H'_{in}		H′ Input. Dynamic input impedance in excess of 1.0 MΩ. Valid input voltage range is between V_{EE} and V_{CC}.
21	V'_{in}	(See Pin 20)	V′ Input. Dynamic input impedance in excess of 1.0 MΩ. Valid input voltage range is between V_{EE} and V_{CC}.
22	H′ V′ Clamp	(See Pin 9)	H'_{in}, V'_{in} and H′ V′ Amplitude Product Clamping pin. An external capacitor works to cancel DC offset. Typically coupled to ground with a 0.047 µF capacitor.
23	H′ V′ out	(See Pin 6)	H′ V′ Output Pin. The product of H'_{in}, V'_{in}, H′ V′ amplitude must be less than 1.9 Vp-p.
24	H′ V′ Amplitude	(See Pin 20)	H′ V′ Amplitude. Dynamic input impedance in excess of 1.0 MΩ. Valid input voltage range is between V_{EE} and V_{CC}.
25	+Sine 2V	(See Pin 6)	+Sine 2V output. The sine wave output developed from the input at Pin 27.
26	–Sine 2V		–Sine 2V output. A 180° phase shifted version of +Sine 2V.
27	Sine 2V Drive	(See Pin 11)	Sine 2V Drive. A ramp waveform input here will produce a sine wave output (at Pins 25 and 26) with frequency varying with input ramp amplitude, and phase varying with ramp DC offset. Input impedance is nominally greater than 1.0 MΩ.
28	+Sine V	(See Pin 6)	+Sine V output. The sine wave output developed from the input at Pin 30.
29	–Sine V		–Sine V output. A 180° phase shifted version of +Sine V.
30	Sine V Drive	(See Pin 11)	Sine V Drive. A ramp waveform input here will produce a sine wave output (at Pins 28 and 29) with frequency varying with input ramp amplitude, and phase varying with ramp DC offset. Input impedance is nominally greater than 1.0 MΩ.

PIN DESCRIPTIONS

Pin	Symbol	Internal Equivalent Circuit	Description
31	Gnd		Ground connection.
32	V^2_{clamp}	(See Pin 9)	Vertical Parabola Clamp pin. An external capacitor works to cancel DC offset. Typically coupled to ground with a 0.047 µF capacitor.
33	$+V^2$	(See Pin 6)	Vertical Parabola.
34	$-V^2$		Complement Vertical Parabola.
35	+V		Vertical Ramp.
36	–V		Complement Vertical Ramp.
37	f_{Vset}		Vertical Charge Current Set. An internally regulated 1.25 Vdc, and the external resistance (R_{Vset}) at this pin determines the charging current for the capacitor, C_V, connected to Pin 38.
38	f_V		Vertical Ramp Generator Capacitor (C_V). The charge and discharge rate of the capacitor at this pin determines the vertical ramp rate.
39	V_{in}		Positive Vertical Flyback input pin. Presents 10 kΩ to input waveform. (See Figure 3). Threshold is at $V_{CC}/2$.
40	V_{EE}		Negative Supply pin. Requires 43 mA at –5.5 < Vdc < –4.5.

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FUNCTIONAL DESCRIPTION

Introduction

The MC1388 is a multi-frequency capable integrated circuit used for geometry correction in monitors and HDTV receivers. With a few inputs the MC1388 will provide ten functions, eight with complements, as output waveforms. These waveforms can then be used by the control circuitry in any combination to modulate the horizontal and vertical deflection currents for geometry correction.

The MC1388 accomplishes multi-frequency operation by allowing external components to determine the nominal frequency of operation. This is done by choosing resistor-capacitor pairs for the desired horizontal and vertical oscillator frequencies. The horizontal and vertical sync inputs then provide the timing reference to which the output waveforms of the MC1388 adhere.

Horizontal Timing

To ensure proper horizontal timing, the MC1388 uses a phase-locked-loop to provide a reliable time base. The loop is externally accessible at the current controlled oscillator (ICO), Pins 3, 4, and at the output of the phase detector, Pin 5. Figure 2 shows relevant internal circuitry and pin connections. This allows the system designer to tailor the timing and performance of the MC1388.

The ICO is an RC type in which the horizontal frequency is determined by the charge and discharge rate of the capacitor at Pin 3. During charging, the voltage on the capacitor (CH) is increased until it reaches an internally determined trip level. At this trip level the direction of the current at Pin 3 is reversed and the discharge process begins. During discharge, circuitry diverts the current available at Pin 3 internally and the capacitor discharges quickly to the bottom trip level where control circuitry switches the direction of Pin 3 current and the cycle begins again.

The charging current at Pin 3 is determined by the current out of Pin 4, which is mirrored at Pin 3. The current out of Pin 4 is set by a nominal 1.25 V stable reference and the external resistance at this node (R_{Hset}). This also provides a means of modulating the charging current at Pin 3 by injecting the error current from the phase detector (Pin 5).

At Pin 5(H_{PLL}) are the filter components of the horizontal phase-locked-loop.These components were chosen to ensure fast tracking over the possible horizontal operating frequencies and a capture range equal to the lock range over these operating frequencies. (Refer to application notes AN553 and AN535 for information regarding design of the filter). The feedback resistor R_F, and the frequency setting capacitor C_H, are also components of the the horizontal phase-locked-loop. R_F serves two purposes, it provides the feedback path for the error current to Pin 4, and is a factor in the phase detector sensitivity which sets the amount of feedback. C_H influences the characteristics of the loop by being a factor in the oscillator sensitivity.

The error current from the phase detector is determined by the static phase error between the free running frequency and the frequency of the horizontal input at Pin 2, and the value of feedback resistance (R_F) between Pins 4 and 5. The output of the phase detector, Pin 5, will develop a voltage as a result of the phase detector error current acting on the H_{PLL} filter. This voltage difference will appear between Pins 5 and 4 and produce the error current provided to the horizontal oscillator. This error current is:

$$I_{ERROR} = \frac{(V_5 - V_4)}{R_F}$$

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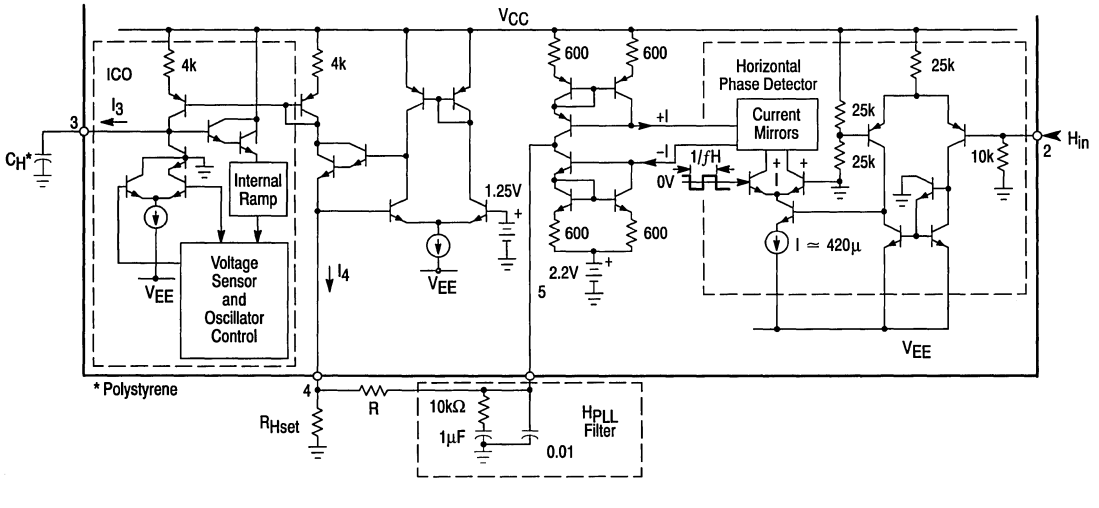
Figure 2. Horizontal Timing



The average voltage difference ($V_5 - V_4$) is capable of approximately ±2.5 V. The changing current is then defined by:

$$I_3 = I_4 = \frac{1.25\ V}{R_{Hset}} - I_{ERROR}$$

Vertical Timing

Vertical timing for the MC1388 is determined by the frequency of the input at Pin 39 and the charging rate of the capacitor at Pin 38. Representative circuitry for relevant pins is shown in Figure 3. The vertical timing is set by an injection oscillator, with the frequency of the generated ramp being determined by the current drawn out of Pin 37.That current is also set with a stable 1.25 Vdc reference and the resistance (R_{Vset}) at this pin. At the beginning of a vertical cycle, the current sourced by Pin 37 is mirrored out of Pin 38 charging the capacitor at Pin 38 with a constant current resulting in a linear ramp. *The charging current of the capacitor (C_V) must be set so the +V output (Pin 35) reaches 2.5 V just before the next vertical sync pulse arrives to trigger the discharge of the capacitor.* The current sourced by Pin 37 is then again provided to the capacitor and the cycle repeats.

WAVEFORMS

Sine Waveforms

The MC1388 has on board circuitry which is capable of producing sine wave like waveforms. Relevant circuitry is shown in Figure 4. A total of four subcircuits are available and each has a 0° and 180° phase shifted output.The sine wave generators require a ramp input which can be provided by the horizontal and vertical ramp outputs of the MC1388.

By modifying the input ramp, the output sine wave can be tailored to meet particular requirements for geometry correction. Figure 5 illustrates an example of geometry errors and the waveforms needed to correct the top to bottom geometry errors. The ramp amplitude affects the number of sine wave cycles and the ramp offset affects the phase. By doubling the peak-to-peak amplitude of an input ramp which created one complete period, a sine wave of two complete periods is produced. By adding DC offset to the input ramp, phase advance or delay is produced. Input ramps to the sine wave generators, which should be DC coupled to provide bias current, are presented to transistor bases with high dynamic impedances in excess of 1.0 MΩ. A means of applying an adjustable ramp is shown in the application section.

Figure 4. Sine Wave Generator

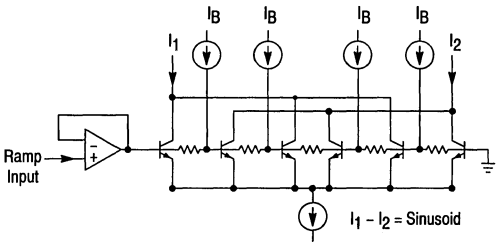


Figure 5. Sine Wave Adjustments

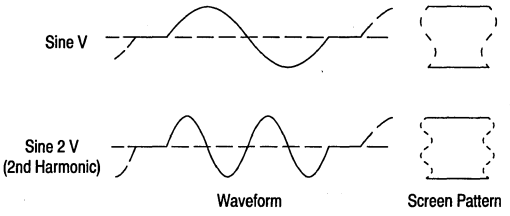
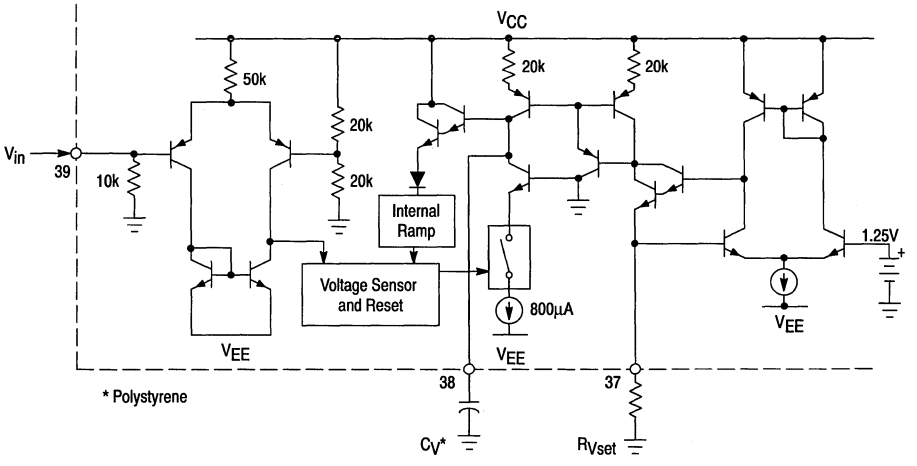


Figure 3. Vertical Timing



Three Input Multiplier (H'_{in}, V'_{in} and H' V' Amplitude)

Pins 20, 21 and 24, are the inputs to a multiplier with the output at Pin 23. All three inputs, although named differently, are the same internally and can be combined in any means to provide the desired output. However, the product of the three inputs is restricted to less than 1.9 Vp-p or the output waveform will experience current limiting. Input bias current must be provide and therefore the input waveforms require DC coupling. The output is clamped and blanked during the appropriate intervals.

Internally Generated Waveforms

Within the MC1388, operations are performed on the horizontal and vertical ramps to produce several waveforms before being provided as outputs through buffers.

Of the internally generated waveforms resulting from operations on the horizontal ramp are a blanked version of the horizontal ramp (+H, Pin 6). A blanked, clamped and squared version of the horizontal ramp ($\pm H^2$, Pins 7 and 8), and a blanked, clamped and cubed version of the horizontal ramp($\pm H^3$, Pins 17 and 18).

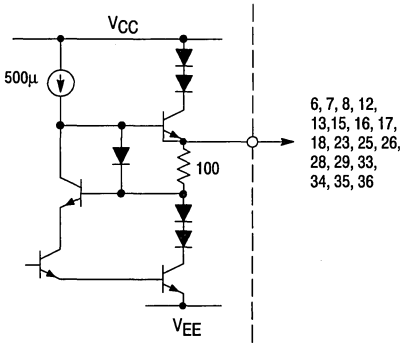
The vertical ramp is blanked and provided at Pins 35 and 36 ($\pm V$). Also, a squared, clamped, and blanked version of the vertical ramp is provided at Pins 33 and 34 ($\pm V^2$).

Blanking of the waveforms occurs once every vertical retrace. Clamping occurs during this blanked interval.

Outputs Buffers and Clamps

The 18 output waveforms are buffered and made available at the output pins. The output buffers are capable of supplying 5.0 mA. A simplified schematic of the output stage is shown in Figure 6.

Figure 6. Output Circuitry



Although all outputs are blanked once each vertical period, not all of them are clamped. Clamping is performed only on the horizontal and vertical parabola outputs ($\pm H^2$, $\pm V^2$), the horizontal cubic outputs ($\pm H^3$), and the three-input multiplier output (H' V'_{out}). Clamping occurs after the leading edge of a vertical sync pulse. Blanking logic zeros the outputs for the time spanned by the first two horizontal pulses during the vertical sync period (see Figure 7B). Clamping circuitry works for the line period between the first two horizontal blanking intervals. Clamping is done by storing a voltage on the clamp capacitor that is proportional to the current required to force the output voltage of the buffer to zero. This provides a sustained current for the next vertical period that is capable of cancelling the DC offset in the waveform. Internal circuitry present at the clamp pins is shown in Figure 7A, and a diagram showing relative timing is shown in Figure 7B.

Figure 7A. Clamp Circuitry for Output Waveforms

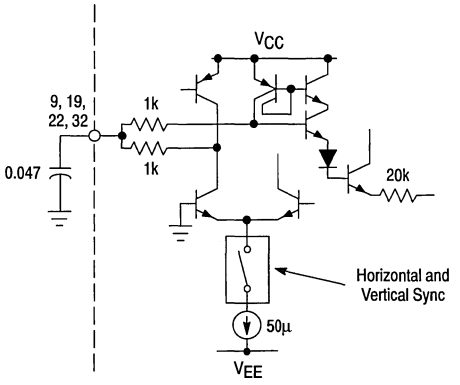
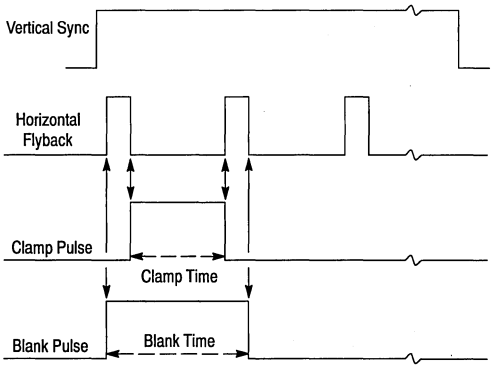


Figure 7B. Blanking and Clamping Diagram



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APPLICATION INFORMATION

The following information is provided to assist designing in the MC1388.

Horizontal and Vertical Flyback Inputs

Waveforms to the horizontal and vertical flyback inputs (Pins 2 and 39) must meet similar requirements except for the frequencies involved. The requirements can be described as follows:

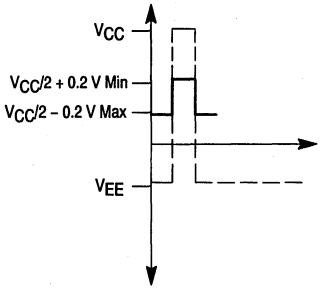
1) $V_{CC}/2.0 + 0.2\ V < V_{in}$ Peak $< V_{CC}$
2) $V_{EE} + 0.5 < V_{in}$ Baseline $\leq V_{CC}/2 - 0.2\ V$
3) $2.0\ \mu s \leq$ Pulse Width $< 1/(2\ f_H)$ (Horizontal Input)
   $2.0\ \mu s \leq$ Pulse Width $< 1/(2\ f_V)$ (Vertical Input)

and the allowable frequencies of operation are:

A) $10\ kHz \leq f_H \leq 63\ kHz$
B) $45\ Hz \leq f_V \leq 120\ Hz$

Figure 8 shows the restrictions on the voltage levels for the flyback inputs.

Figure 8. Valid Input Levels for Both the Horizontal (Pin 2) and the Vertical (Pin 39) Inputs.



Since the input pins are equipped with ESD diodes, voltages on these pins should never exceed V_{CC} or V_{EE} by more than 0.5 V.

Horizontal Oscillator and Phase-Locked-Loop

Since the charge and discharge of the capacitor at Pin 3 (C_H) is done with constant currents, the voltage waveform of the capacitor voltage is:

$$\pm\Delta V = \pm \frac{I\,\Delta t}{C}$$

,where Δt is the trace or retrace time.

The horizontal frequency is then the inverse of the sum of the charge time and the discharge time,

$$f_{horizontal} = \frac{1}{(t_{charge} + t_{discharge})}$$

where, t_{charge} = trace time and $t_{discharge}$ = retrace time. This relates the trace and retrace time to element values, internal quantities and a design variable, I_{charge}. So,

$$t_{charge} = \frac{C_H\ \Delta V_{p\text{-}p}}{I_{charge}} \text{ and } t_{discharge} = \frac{C_H\ \Delta V_{p\text{-}p}}{I_{discharge}}$$

$\Delta V_{p\text{-}p}$ and $I_{discharge}$ are fixed ($I_{discharge}$ is typically 1.0 mA and $\Delta V_{p\text{-}p}$ is $\simeq$ 2.5 $\Delta V_{p\text{-}p}$). If C_H is chosen to meet the requirements of retrace time and,

If C_H is chosen to meet the requirements of retrace time and, trace time >> retrace time, then $t_{charge} >> t_{discharge}$.

$$\text{then } f_{horizontal} \simeq \frac{1}{t_{charge}} \text{ or, } f_{horizontal} \simeq \frac{I_{charge}}{C_H\ \Delta V_{p\text{-}p}}$$

By choosing C_H and determining I_{charge} the horizontal frequency can be set, since $\Delta V_{p\text{-}p}$ is known. Referring to Figure 2, the current out of Pin 4 is the current I_{charge} and is composed of,

$$I_{charge} = \frac{1.25}{R_{Hset}} - I_{ERROR}$$

where I_{ERROR} is the current from the phase detector when the loop is locked and was determined in the FUNCTIONAL DESCRIPTION to be,

$$I_{ERROR} = \frac{(V_5 - V_4)}{R_F}$$

The horizontal frequency is now defined and is,

$$f_{horizontal} = \left\{\frac{1.25}{R_{Hset}} \pm \frac{(V_5 - V_4)}{R_F}\right\}\left(\frac{1}{C_H\ \Delta V_{p\text{-}p}}\right) \text{ or,}$$

$$f_{horizontal} = f_{free\ run} \pm \Delta f,$$

where Δf is the frequency difference between the horizontal free run frequency and the frequency of the input signal, R_{Hset} is the resistance from Pin 4 to ground, R_F is the resistor between Pins 4 and 5, and C_H is the capacitor from Pin 3 to ground. *It is to be emphasized that this equation holds true only when the loop is locked.*

The phase detector sensitivity, K_{PD}, is determined from the slope of the curve which describes the average current output from the phase detector and the phase error related to that current. It is defined by,

$$K_{PD} \simeq \frac{2\ I_{PDmax}}{SW\ 2\pi f_H}\ (A/rad) \text{ or, } \frac{900 \bullet 10^{-6}}{SW\ 2\pi f_H}\ (A/rad).$$

I_{PDmax} is the maximum current that can be sourced or sinked from the phase detector and SW is the width of the horizontal flyback input pulse in seconds. f_H is the frequency of the horizontal flyback input.

The oscillator sensitivity, K_O, defined by $\partial f_H/\partial I$ is,

$$K_O \simeq \frac{1}{2.5\ C_H}\ (Hz/A)$$

Since the maximum average voltage difference between Pins 4 and 5 is capable of about ±2.5 V, the maximum error current transfer from Pin 5 to Pin 4 is,

$$I_{ERRORmax} \leq \frac{\pm\ 2.5\ V}{R_F}.$$

And also redefines the phase detector sensitivity as,

$$K_{PD'} \simeq \frac{2.5\ V}{R_F\ \pi\ SW f_H}$$

The product of the phase detector sensitivity, the oscillator sensitivity and the maximum phase error then defines maximum possible deviation from the free run frequency. The maximum possible phase error is the phase error corresponding to one half the width of the horizontal flyback input pulse or, (SW/2), $2\pi f_H$, so the maximum deviation from the free run frequency is one half the lock range and is,

$$\pm \frac{f_{Flock}}{2} \simeq \frac{1}{C_H R_F}.$$

(The value of f_{Flock} should be kept small enough to prevent loop lock on harmonics. A general rule of thumb is f_{lock} < 10% of the desired horizontal frequency.) Then I_{ERROR} is less than 10% of I_{charge}, and the horizontal frequency is almost entirely determined by,

$$f_{horizontal} \simeq \frac{1.25}{R_{Hset} C_H \Delta V_{p\text{-}p}}, \quad \Delta V \text{ p-p} \simeq 2.5,$$

so this becomes, $f_{horizontal} \simeq \frac{1}{2 R_{Hset} C_H}$,

which is also the horizontal free run frequency. The horizontal free run frequency should be set at or very near the desired horizontal frequency since the lock range is centered about this frequency.

Calculating the external components is then based on the following requirements:

1) The value of C_H satisfies the requirements for retrace time, or $C_H \leq 5.6 \bullet 10^{-4}\ t_{discharge}$.
2) The value of the resistance from Pin 5 to ground is given by,

$$R_{Hset} \simeq \frac{1}{2 f_{horizontal} C_H}.$$

(The value of the resistor calculated for R_{Hset} should be considered approximate. The 5.0 kΩ pot shown in the application circuit of Figure 12 is recommended for optimization).

3) The resistor R_F is such that the lock range is a reasonable choice (f_H/10) given by,

$$R_F \simeq \frac{2}{C_H (\pm f_{lock})}.$$

For 15,625 Hz, recommended values are, C_H = 0.001 µF, R_{Hset} = 30 kΩ + 5.0 kΩ variable, and $R_F \geq 620$ kΩ. For 31,250 Hz, recommended values are, C_H = 0.001 µF, R_{Hset} = 13 kΩ + 5.0 kΩ variable, and $R_F \geq 300$ kΩ.

Vertical Timing

To set the vertical timing a capacitor-resistor pair must be chosen (refer to Figure 3). The vertical timing section is similar to the horizontal section in that the frequency is determined by the charge and discharge rate of a capacitor at Pin 38. However, the vertical ramp oscillator is an injection type and the proper peak-to-peak voltage must be set with R_{Vset}.

The basic equation,

$$\pm \Delta V = \pm \frac{I \Delta t}{C_V},$$

describes the capacitor voltage for the charge and discharge currents made available at Pin 38. Further, if $t_{retrace} << t_{trace}$ then,

$$f_{vertical} = fV \simeq \frac{1}{\Delta t_{trace}} = \frac{1}{\Delta t_{charge}}$$

and the vertical frequency is determined by the charging current, ΔV and the capacitor value.

The reference voltage for developing the charging current is present at Pin 37 and is nominally 1.25 V. The charging current is then defined by the resistance at this node,

$$I_{charge} = \frac{1.25}{R_{Vset}}.$$

The resistance required can be determined for a particular frequency and capacitor combination. *The capacitor voltage, ΔV, must be nominally 2.5 Vp-p for the specified full scale vertical outputs.* Using this value, the proper combination R_{Vset} and C_V, can be calculated.

The current available to discharge C_V is approximately 800 µA. So, a practical C_V value is described by, $C_V \leq 3.2 \bullet 10^{-4}\ \Delta t$, where Δt is required retrace time.

This value of C_V is next used to calculate the value R_{Vset} considering the vertical frequency desired,

$$I_{charge} = \frac{1.25}{R_{Vset}} = \frac{C_V \Delta V}{\Delta t} = C_V \Delta V f_V \text{ or,}$$

$$R_{Vset} \simeq \frac{1.25}{C_V \Delta V f_V} = \frac{1.25}{C_V 2.5 f_V} \simeq \frac{1}{2 C_V f_V}$$

(The equation given for R_{Vset} is approximate and should be used only as a starting point. The 25 kΩ pot in the applications circuit of Figure 12 is used to optimize this value.)

Sine Wave Generation

Shown in Figure 9 and 10 are two circuits which can be used to provide drive to the sine generator circuits. These circuits DC couple to the sine drive inputs providing the necessary base drive. The circuit in Figure 9 will provide adequate ramp amplitude for a single cycle of a sine wave at the horizontal or vertical frequency and the circuit in Figure 10 will provide adequate ramp amplitude for two cycles of a sine wave.

Figure 9. Sine H or V Driver

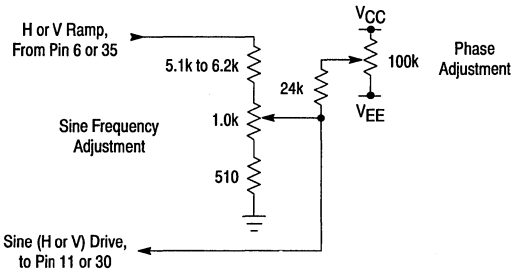
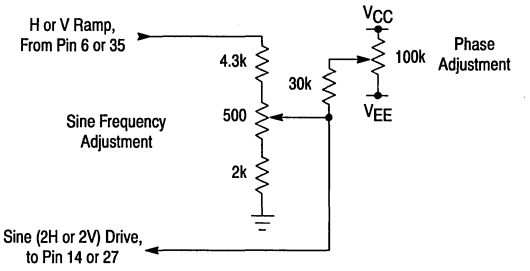


Figure 10. Sine 2H or 2V Driver



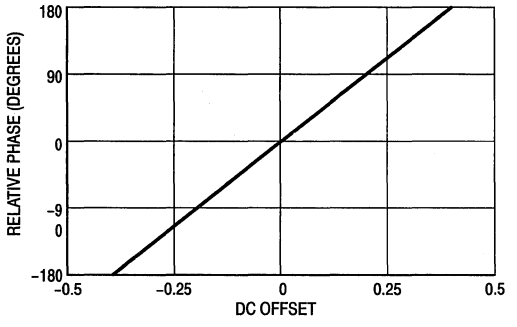
An approximate relation between the number of cycles and peak-to-peak input voltage is,

$$V_{inp\text{-}p} \approx \frac{\text{number of cycles} + 0.2}{1.25}$$

The phase of the output sine wave is a function of the input ramp DC offset. Figure 11 shows the relationship between the phase and the offset.

If a phase change is desired, it should be remembered that the input windows for the sine generators are between –850 mV and +850 mV centered about zero, therefore, a DC offset will reduce the allowable input ramp peak-to-peak amplitude.

Figure 11. Phase versus DC Offset



Multiplier Circuit

The multiplier is made up of three inputs, H'_{in}, V'_{in} and H'V' Amplitude (Pins 20, 21 and 24 respectively), which are internally equivalent. The voltage output on Pin 23 is the product of the voltage on the input pins and is restricted to a maximum output voltage of 1.9 Vp-p, or current limiting will occur. Any combination of the three inputs can be used, provided that the product of all the inputs is less than 5.0 Vp-p.

Application Circuit

Figure 12 shows an application circuit with component values applicable for,

$f_{horizontal}$ = 31.25 kHz $f_{vertical}$ = 60 Hz

$\pm f_{lock} \simeq$ 2.3 kHz $\pm f_{pull\text{-}in} \simeq$ 2.3 kHz

Figure 13 shows the timing of all the vertical waveforms for the application circuit. Figure 14 shows the timing of all the horizontal waveforms for the application circuit.

Figure 12. Application Circuit of the MC1388

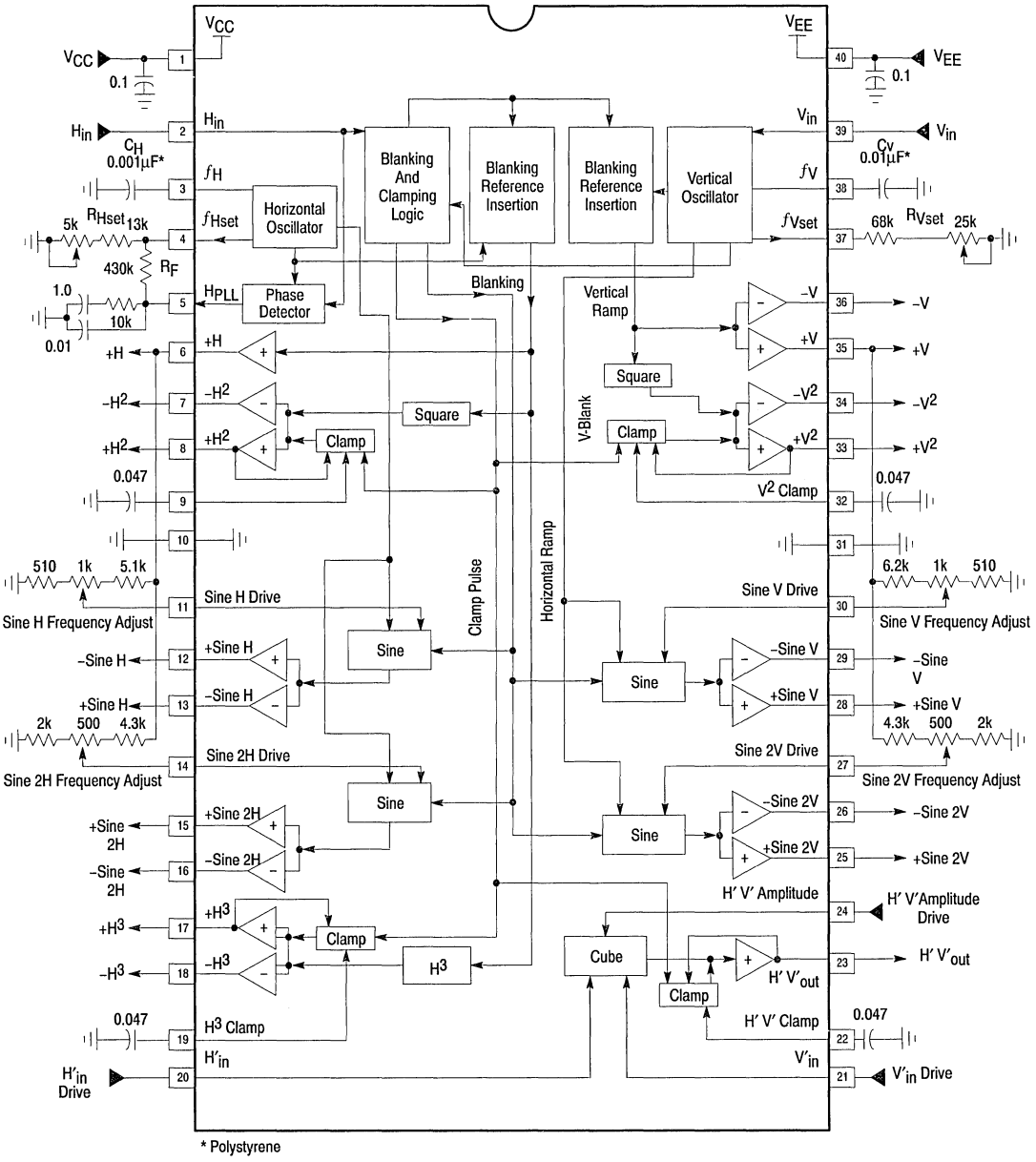


Figure 13. Vertical Timing

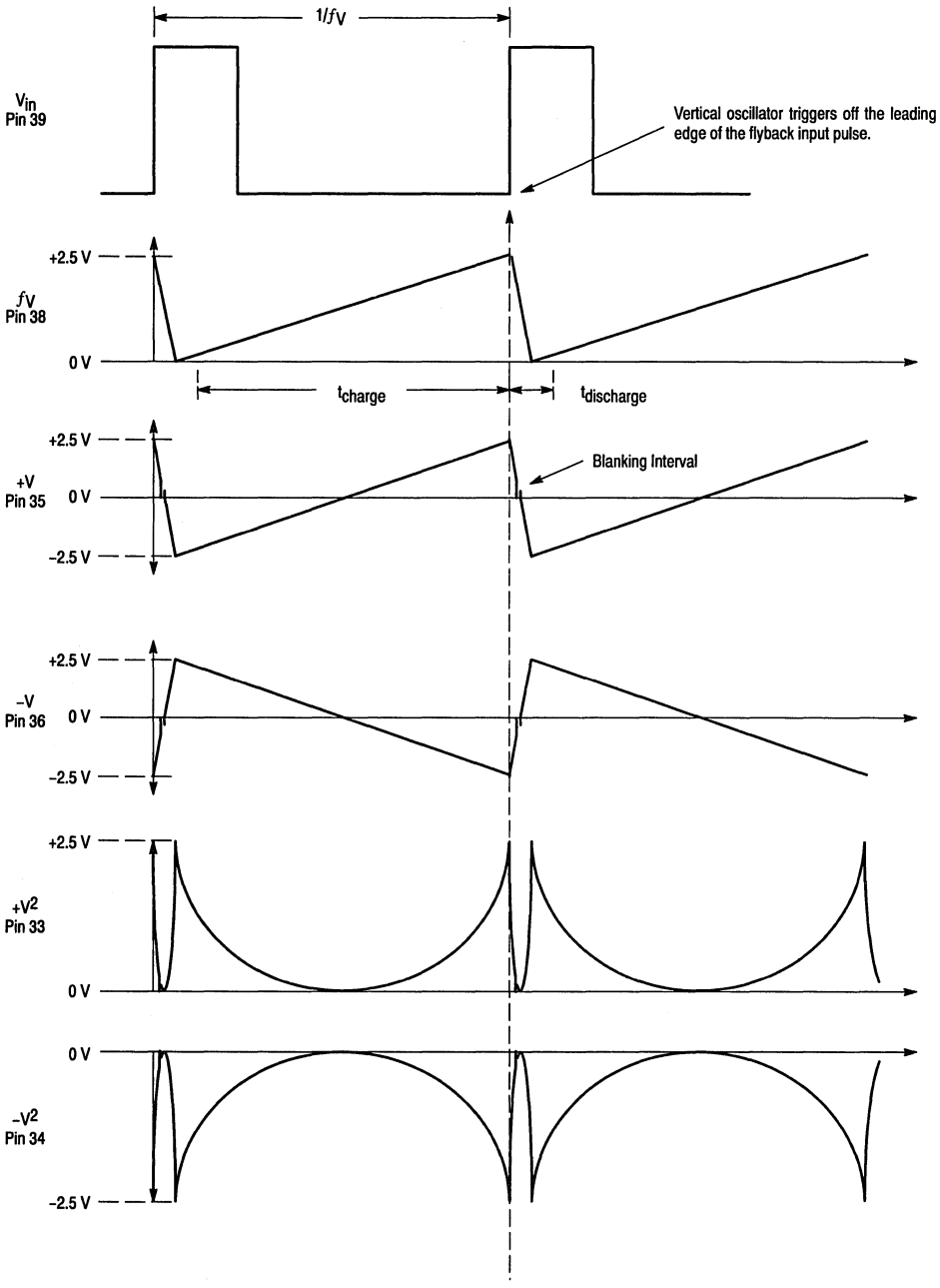


Figure 13. Vertical Timing (continued)

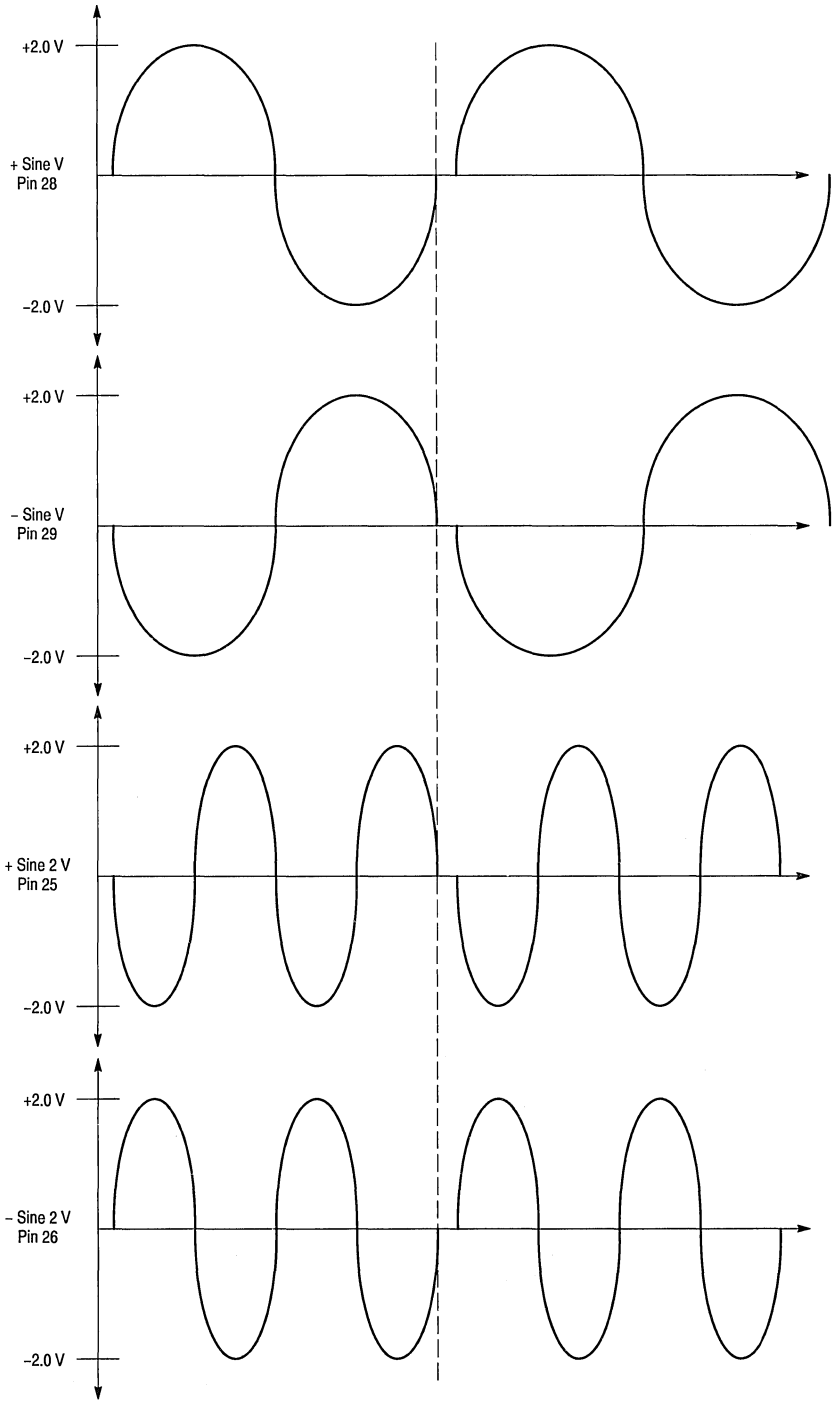


Figure 14. Horizontal Timing

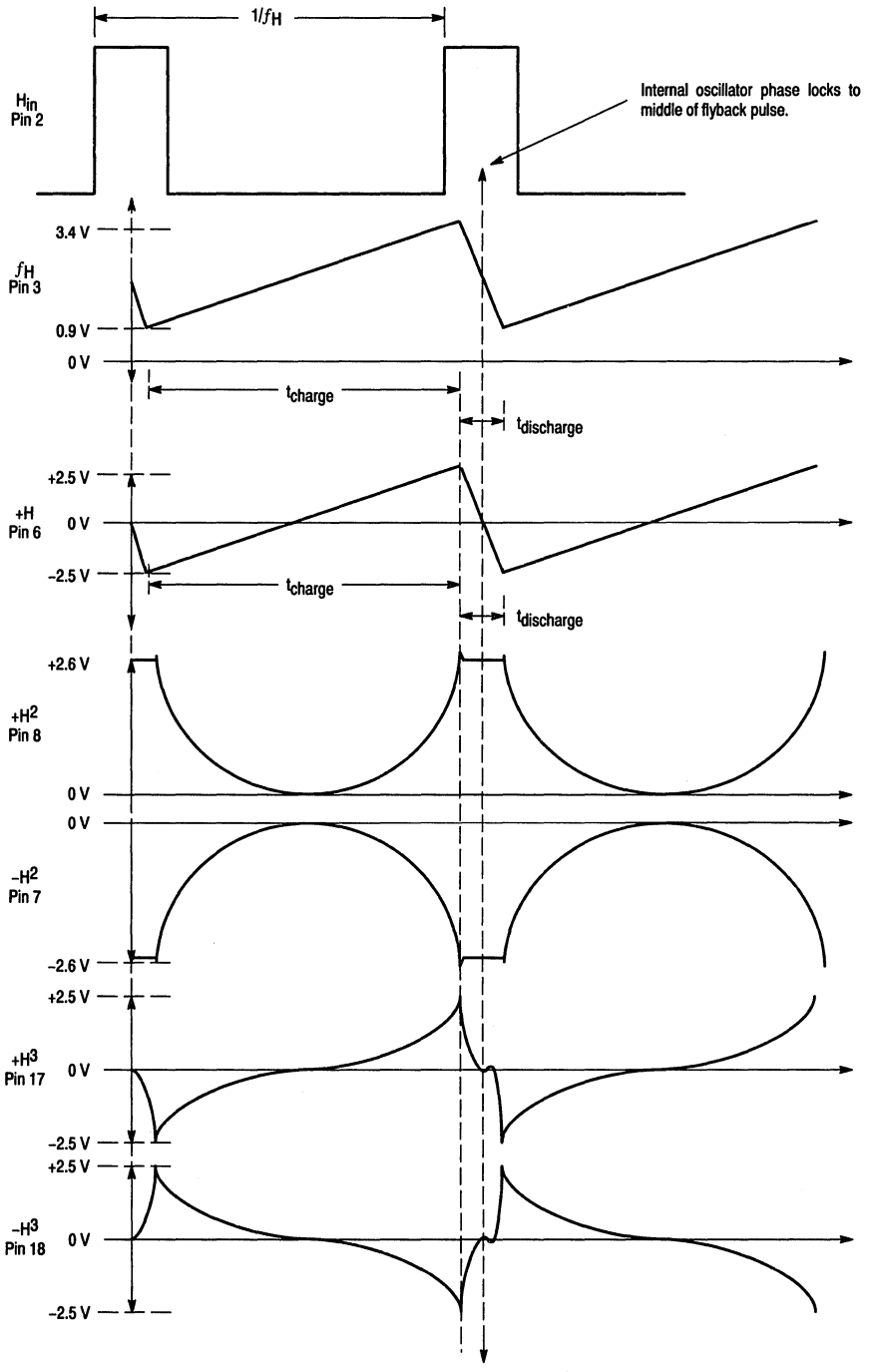
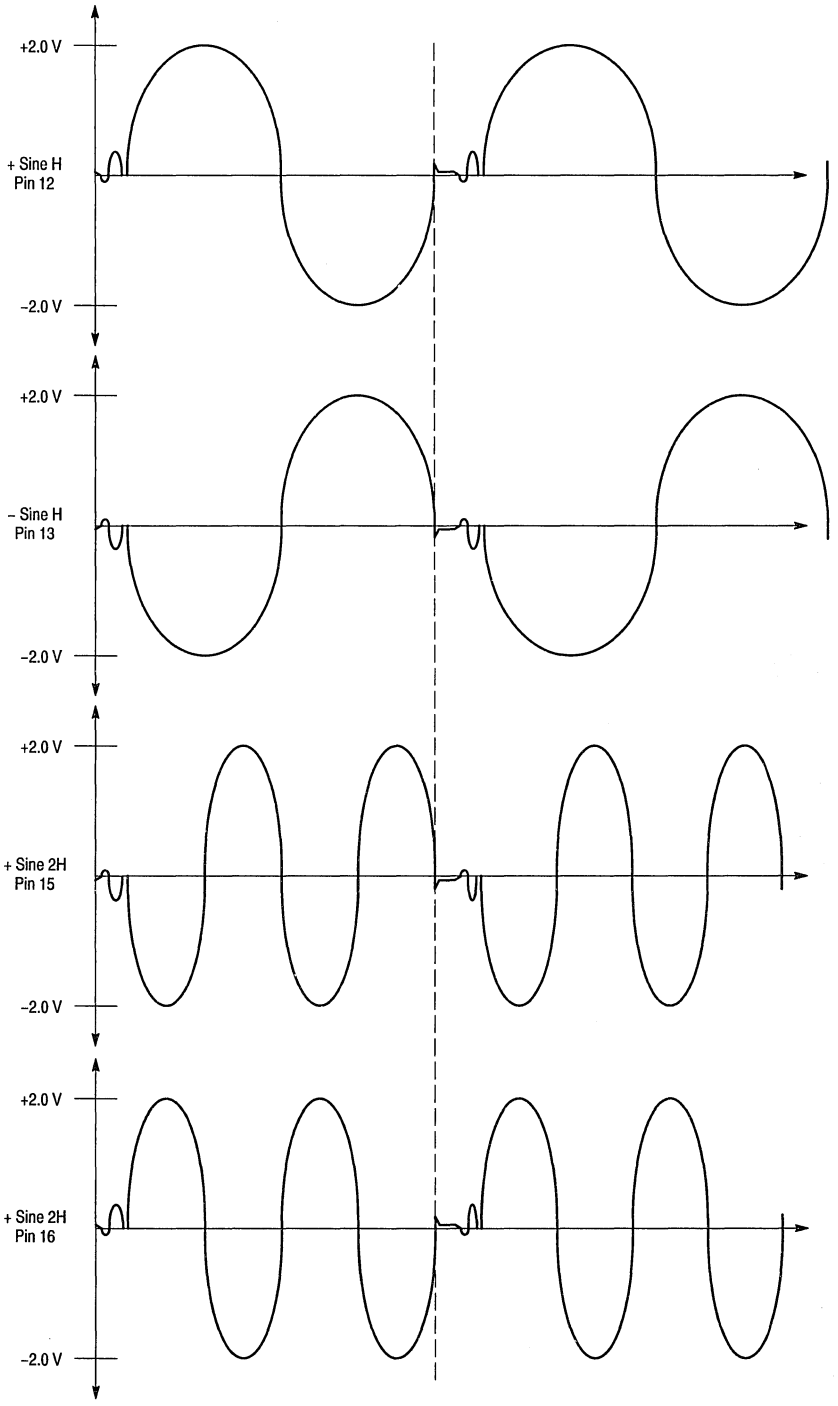


Figure 14. Horizontal Timing (continued)



MC1391

TV HORIZONTAL PROCESSOR

SILICON MONOLITHIC INTEGRATED CIRCUIT

TV HORIZONTAL PROCESSOR

The MC1391 provides low-level horizontal sections including phase detector, oscillator and pre-driver. This device was designed for use in all types of television receivers.

- Internal Shunt Regulator
- Preset Hold Control Capability
- ±300 Hz Typical Pull-In
- Linear Balanced Phase Detector
- Variable Output Duty Cycle for Driving Tube or Transistor
- Low Thermal Frequency Drift
- Small Static Phase Error
- Adjustable DC Loop Gain
- Positive Flyback Inputs

P SUFFIX
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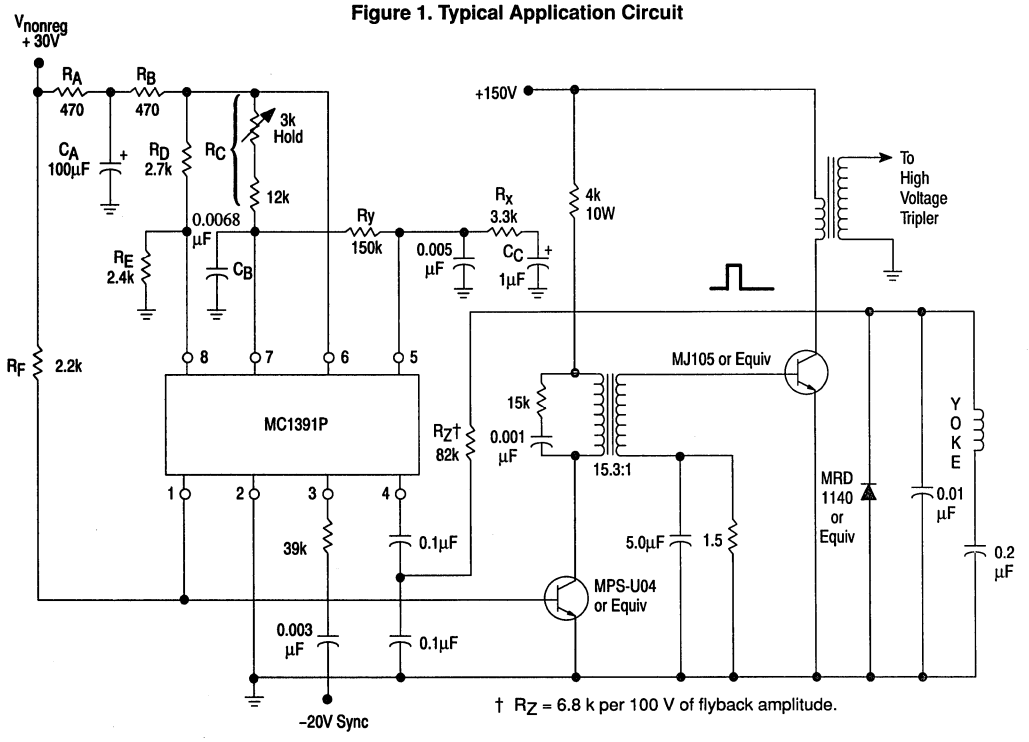
CASE 626

9

Figure 1. Typical Application Circuit



This circuit has an oscillator pull-in range of ±300 Hz, a noise bandwidth of 320 Hz, and a damping factor of 0.8.

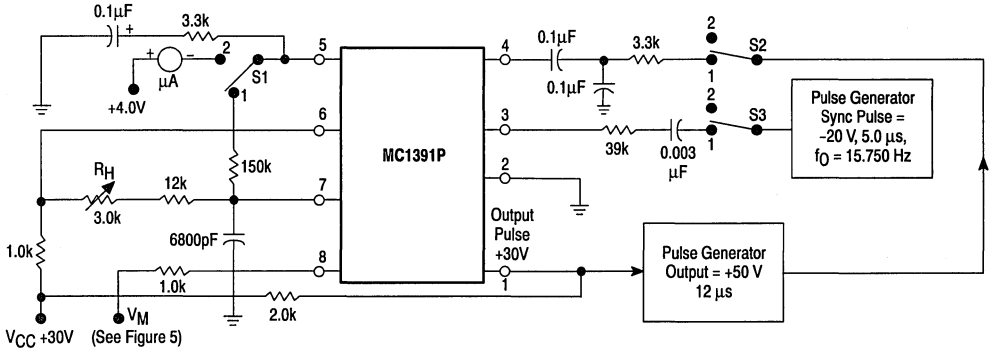
MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

Rating	Value	Unit
Supply Current	40	mAdc
Output Voltage	40	Vdc
Output Current	30	mAdc
Sync Input Voltage (Pin 3)	5.0	$V_{(p-p)}$
Flyback Input Voltage (Pin 4)	5.0	$V_{(p-p)}$
Power Dissipation (Package Limitation) Plastic Package Derate above T_A = +25°C	 625 5.0	 mW mW/°C
Operating Temperature Range (Ambient)	0 to +70	°C
Storage Temperature Range	–65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = +25°C, unless otherwise noted. See Test Circuit of Figure 2, all switches in position 1.)

Characteristics	Min	Typ	Max	Unit
Regulated Voltage (Pin 6)	8.0	8.6	9.4	Vdc
Supply Current (Pin 6)	—	20	—	mAdc
Collector-Emitter Saturation Voltage (Output Transistor Q1 in Figure 6) (I_C = 20 mA, Pin 1) Vdc	—	0.15	0.25	Vdc
Voltage (Pin 4)	—	2.0	—	Vdc
Oscillator Pull-in Range (Adjust R_H in Figure 2)	—	±300	—	Hz
Oscillator Hold-in Range (Adjust R_H in Figure 2)	—	±900	—	Hz
Static Phase Error (Δf = 300 Hz)	—	0.5	—	µs
Free-running Frequency Supply Dependance (S1 in position 2)	—	±3.0	—	Hz/Vdc
Phase Detector Leakage (Pin 5) (All switches in position 2)	—	—	±1.0	µA
Sync Input Voltage (Pin 3)	2.0	—	5.0	V(p-p)
Sawtooth Input Voltage (Pin 4)	1.0	—	3.0	V(p-p)

Figure 2. Test Circuit



TYPICAL CHARACTERISTICS

Figure 3. Frequency versus Temperature

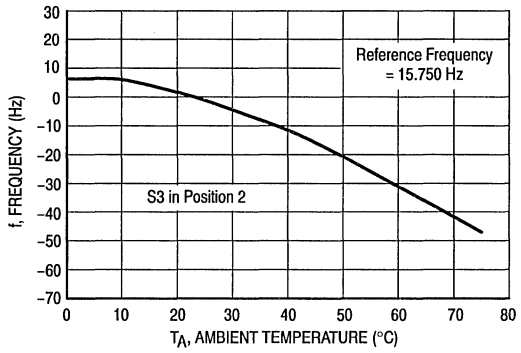


Figure 4. Frequency Drift versus Warm-Up Time

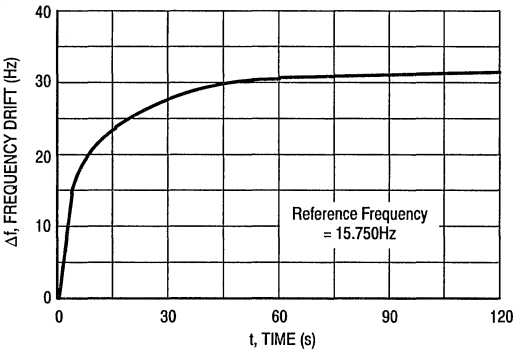


Figure 5. Mark Space Ratio

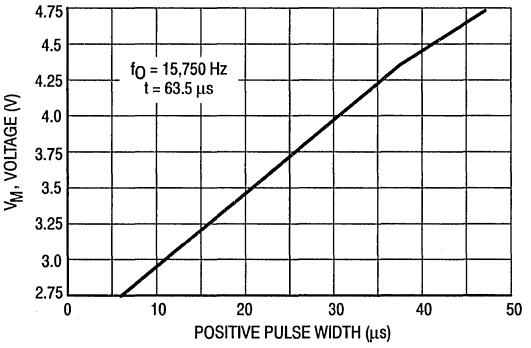
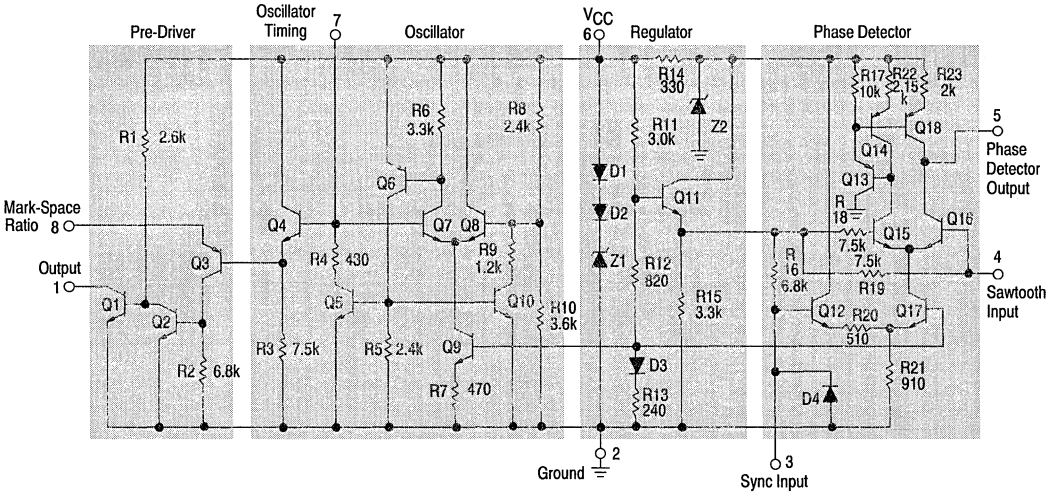


Figure 6. Circuit Schematic



CIRCUIT OPERATION

The MC1391P contains the oscillator, phase detector and predriver sections needed for a television horizontal APC loop.

The oscillator is an RC type with one pin (Pin 7) used to control the timing. The basic operation can be explained easily. If it is assumed that Q7 is initially off, then the capacitor connected from Pin 7 to ground will be charged by an external resistor (R_C) connected to Pin 6. As soon as the voltage at Pin 7 exceeds the potential set at the base of Q8 by resistors R8 and R10, Q7 will turn on and Q6 will supply base current to Q5 will discharge the capacitor through R4 until the base bias of Q7 falls below that of Q8, at which time Q7 will turn off and the cycle repeats.

The sawtooth generated at the base of Q4 will appear across R3 and turn off Q3 whenever it exceeds the bias set on Pin 8. By adjusting the potential at Pin 8, the duty cycle (MSR) at the predriver output pin (Pin 1) can be changed to accommodate either tube or transistor horizontal output stages.

The phase detector is isolated from the remainder of the circuit by R14 and Z2. The phase detector consists of the comparator Q15, Q16 and the gated current source Q17. Negative going sync pulses at Pin 3 turn off Q12 and the current division between Q15 and Q16 will be determined by the phase relationship of the sync and the sawtooth waveform at Pin 4, which is derived from the horizontal flyback pulse. If there is no phase difference between the sync and sawtooth, equal currents will flow in the collectors of Q15 and Q16 each of half the sync pulse period. The current in Q15 is turned around by Q18 so that there is no net output current at Pin 5 for balanced conditions. When a phase offset occurs, current will flow either in or out of Pin 5. This pin is connected via an external low-pass filter to Pin 7, thus controlling the oscillator.

Shunt regulation for the circuit is obtained with a zero temperature coefficient from the series combination of D1, D2 and Z1.

APPLICATION INFORMATION

Although it is an integrated circuit, the MC1391P has all the flexibility of a conventional discrete component horizontal APC loop. The internal temperature compensated voltage regulator allows a wide supply voltage variation to be tolerated, enabling operation from nonregulated power supplies. A minimum value for supply current into Pin 6 to maintain zener regulation is about 18 mA. Allowing 2.0 mA for the external dividers

$$R_A + R_B = \frac{V_{nonreg(min)} - 8.8}{20 \times 10^{-3}}$$

Components R_A, R_B and C_A are used for ripple rejection. If the supply voltage ripple is expected to be less than 100 mV (for a 30 V supply) then R_A and R_B can be combined and C_A omitted.

The output pulse width can be varied from 6.0 µs to 48 µs by changing the voltage at Pin 8 (see Figure 5). However, care should be taken to keep the lead lengths to Pin 8 as short as possible at Pin 1. The parallel impedance of R_D and R_E should be close to 1.0 kΩ to ensure stable pulse widths.

For 15 mA drive at saturation

$$R_F = \frac{V_{nonreg} - 0.3}{15 \times 10^{-3}}$$

The oscillator free-running frequency is set by R_C and C_B connected to Pin 7. For values of $R_C \geq R_{discharge}$ (R4 in Figure 6), a useful approximation for the free-running frequency is

$$f_O = \frac{1}{0.6\, R_C C_B}$$

Proper choice of R_C and C_B will give a wide range of oscillator frequencies — operation at 31.5 kHz for countdown circuits is possible for example. As long as the product $R_C C_B \approx 10^{-4}$ many combinations of values of R_C and C_B will satisfy the free-running frequency requirement of 15.734 kHz. However, the sensitivity of the oscillator (β) to control-current from the phase detector is directly dependent on the magnitude of R_C, and this provides a convenient method of adjusting the DC loop gain (fc).

For a given phase detector sensitivity (μ) = 1.60×10^{-4} A/rad

$f_c = \mu\beta$ and $\beta = 3.15 \times R_C$ Hz/mA

Increasing R_C will raise the DC loop gain and reduce the static phase error (S.P.E.) for a given frequency offset. Secondary effects are to increase the natural resonant frequency of the loop (ω_n) and give a wider pull-in range from an out-of-lock condition. The loop will also tend to be underdamped with fast pull-in times, producing good airplane flutter performance. However, as the loop becomes more underdamped impulse noise can cause shock excitation of the loop. Unlimited increase in the DC loop gain will also raise the noise bandwidth excessively causing horizontal jitter with thermal noise. Once the DC loop gain has been selected for adequate SPE performance, the loop filter can be used to produce the balance between other desirable characteristics. Damping of the loop is achieved most directly by changing the resistor R_X with respect to R_Y which modifies the AC/DC gain ration (m) of the loop. Lowering this ratio will reduce the pull-in range and noise bandwidth (fnn). (Note: very large values of R_Y will limit the control capability of the phase detector with a corresponding reduction in hold-in range.)

Static phasing can be adjusted simply by adding a small resistor between the flyback pulse integrating capacitor and ground. The sync coupling capacitor should not be too small or it can charge during the vertical pulse and this may result in picture bends at the top of the CRT.

Note: In adjusting the loop parameters, the following equations may prove useful:

$$f_{nn} = \frac{1 \times \chi^2 T\omega_C}{4\chi T} \qquad \chi = \frac{R_X}{R_Y}$$

$$\omega_n = \sqrt{\frac{\omega_C}{(1+\chi)T}} \qquad \omega_C = 2\pi f_c \qquad T = R_y C_C$$

$$K = \frac{\chi^2 T\omega_C}{4}$$

where: K = loop damping coeffecient

MC3340

ELECTRONIC ATTENUATOR

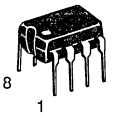
SILICON MONOLITHIC INTEGRATED CIRCUIT

ELECTRONIC ATTENUATOR

The MC3340 is a simple but very effective electronic attenuator. This device offers up to 80 dB of attenuation control for frequencies to 1.0 MHz. THD (distortion) is less than 1% — up to 15 dB attenuation and less than 3% — up to 40 dB.

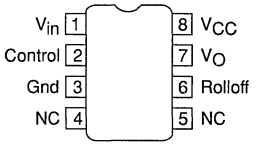
Typical uses include instrumentation control, remote control audio amplifiers, electronic games, and CATV (cable TV) set-top converter audio control.

- Designed for use in:
  - DC Operated Volume Control
  - Compression and Expansion Amplifier Applications
- Controlled by DC Voltage or External Variable Resistor
- Economical 8-Pin Dual-In-Line Package



P SUFFIX
PLASTIC PACKAGE
CASE 626

PIN CONNECTIONS

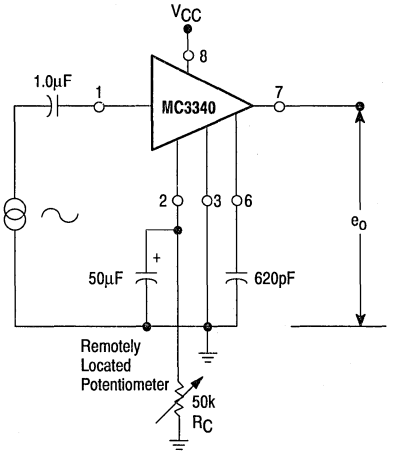


MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	20	Vdc
Power Dissipation @ T_A = 25°C Derate above T_A = 25°C	P_D	1.2 10	W mW/°C
Operating Ambient Temperature Range	T_A	0 to +75	°C

9

Figure 1. Typical DC Remote Volume Control



ELECTRICAL CHARACTERISTICS (e_{in} = 100 mVrms, f = 1.0 kHz, V_{CC} = 16 Vdc, T_A = +25°C, unless otherwise noted.)

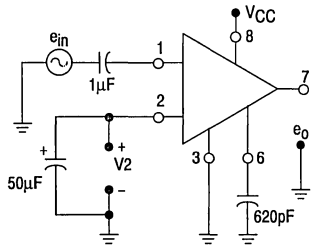
Circuit	Characteristics	Min	Typ	Max	Unit
	Operating Power Supply Voltage	0.8	—	18	Vdc
	Control Terminal Sink Current, Pin 2 (e_{in} = 0)	—	—	2.0	mAdc
	Maximum Input Voltage	—	—	0.5	Vrms
	Voltage Gain	11	13	—	dB
	Attenuation Range from Maximum Gain (V2 = 6.5 Vdc)	70	80	—	dB
	Total Harmonic Distortion (Pin 2 Gnd) (e_{in} = 100 mVrms, $e_o = A_v \bullet e_{in}$)	—	0.6	1.0	%

Figure 2. Circuit Schematic

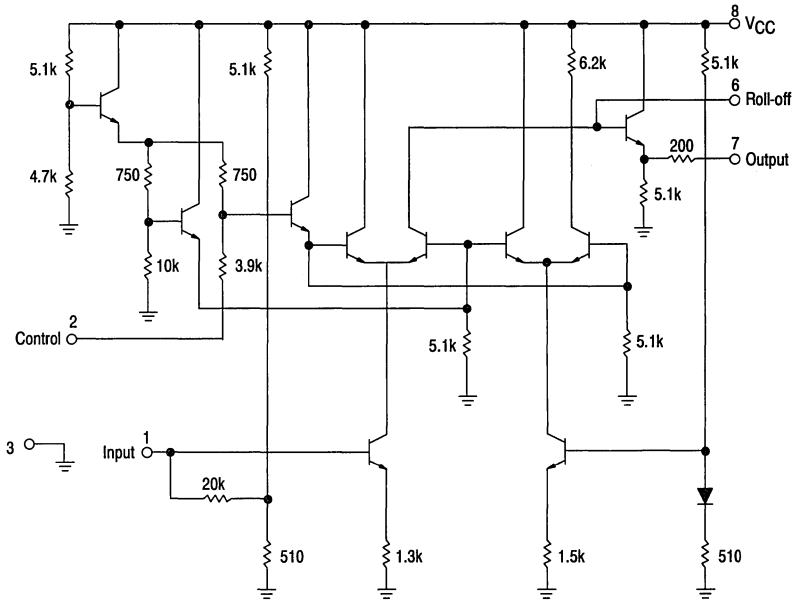


Figure 3. Attenuation versus DC Control Voltage

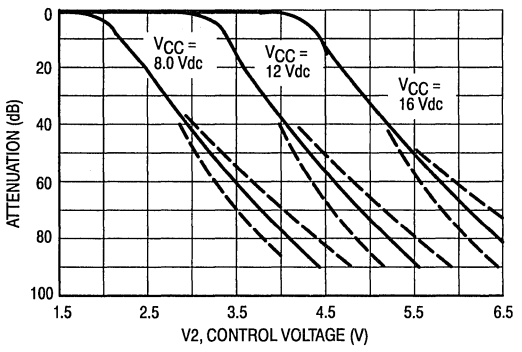


Figure 4. Attenuation versus Control Resistor

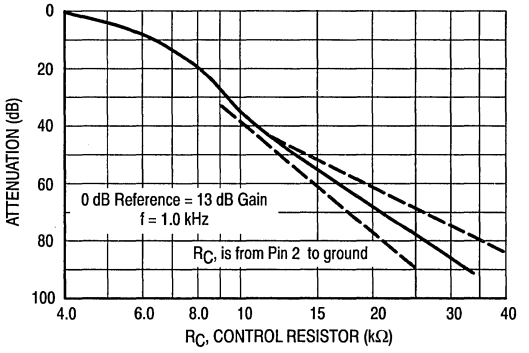


Figure 5. Frequency Response

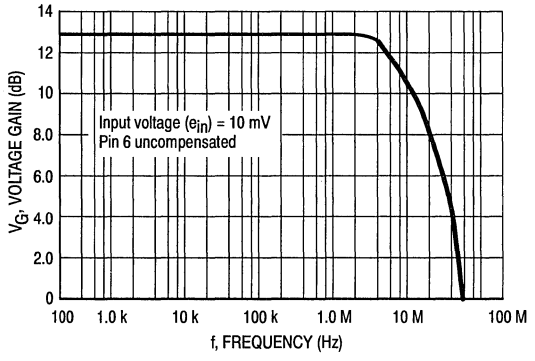


Figure 6. Output Voltage Swing

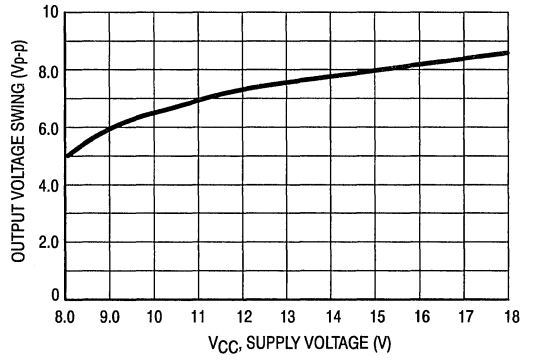
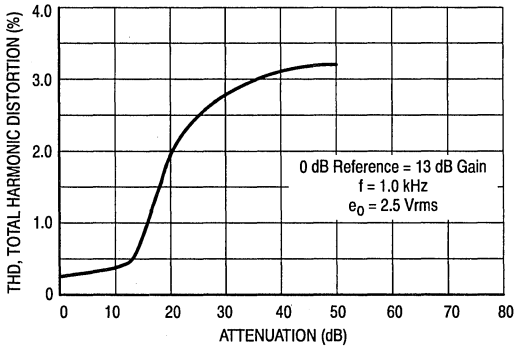


Figure 7. Total Harmonic Distortion



MC3346

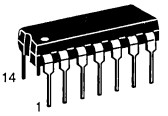
GENERAL PURPOSE TRANSISTOR ARRAY

SILICON MONOLITHIC INTEGRATED CIRCUIT

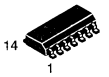
General Purpose Transistor Array One Differentially Connected Pair and Three Isolated Transistor Arrays

The MC3346 is designed for general purpose, low power applications for consumer and industrial designs,

- Guaranteed Base-Emitter Voltage Matching
- Operating Current Range Specified: 10 μA to 10 mA
- Five General Purpose Transistors in One Package



P SUFFIX
PLASTIC PACKAGE
CASE 646



D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO-14)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	15	Vdc
Collector-Base Voltage	V_{CBO}	20	Vdc
Emitter-Base Voltage	V_{EB}	5.0	Vdc
Collector-Substrate Voltage	V_{CIO}	20	Vdc
Collector Current — Continuous	I_C	50	mAdc
Total Power Dissipation @ T_A = 25°C Derate above 25°C Derate Each Transistor @ 25°C	P_D	1.2 10 300	W mW/°C mW/°C
Operating Temperature Range	T_A	–40 to +85	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

ORDERING INFORMATION

Device	Temperature Range	Package
MC3346D	–40° to +85°C	SO-14
MC3356P		Plastic DIP

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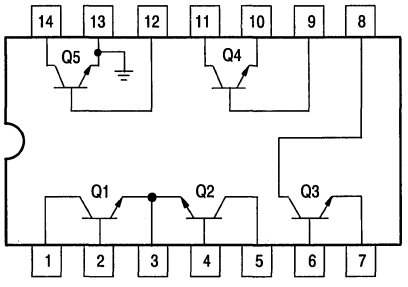
PIN CONNECTIONS



Pin 13 is connected to substrate and must remain at the lowest circuit potential.

ELECTRICAL CHARACTERISTICS (T_A = +25°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
STATIC CHARACTERISTICS					
Collector-Base Breakdown Voltage (I_C = 10 μAdc)	$V_{(BR)CBO}$	20	60	—	Vdc
Collector-Emitter Breakdown Voltage (I_C = 1.0 mAdc)	$V_{(BR)CEO}$	15	—	—	Vdc
Collector-Substrate Breakdown Voltage (I_C = 10 μA)	$V_{(BR)CIO}$	20	60	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 μAdc)	$V_{(BR)EBO}$	5.0	7.0	—	Vdc
Collector-Base Cutoff Current (V_{CB} = 10 Vdc, I_E = 0)	I_{CBO}	—	—	40	nAdc
DC Current Gain (I_C = 10 mAdc, V_{CE} = 3.0 Vdc) (I_C = 1.0 mAdc, V_{CE} = 3.0 Vdc) (I_C = 10 μAdc, V_{CE} = 3.0 Vdc)	h_{FE}	 — 40 —	 140 130 60	 — — —	—
Base-Emitter Voltage (V_{CE} = 3.0 Vdc, I_E = 1.0 mAdc) (V_{CE} = 3.0 Vdc, I_E = 10 mAdc)	V_{BE}	 — —	 0.72 0.8	 — —	Vdc
Input Offset Current for Matched Pair Q1 and Q2 (V_{CE} = 3.0 Vdc, I_C = 1.0 mAdc)	$\lvert I_{IO1} - I_{IO2} \rvert$	—	0.3	2.0	μAdc
Magnitude of Input Offset Voltage (V_{CE} = 3.0 Vdc, I_C = 1.0 mAdc)	—	—	0.5	5.0	mVdc
Temperature Coefficient of Base-Emitter Voltage (V_{CE} = 3.0 Vdc, I_C = 1.0 mAdc)	$\frac{\Delta V_{BE}}{\Delta T}$	—	–1.9	—	mV/°C
Temperature Coefficient	$\frac{\lvert \Delta V_{IO} \rvert}{\Delta T}$	—	1.0	—	μV/°C
Collector-Emitter Cutoff Current (V_{CE} = 10 Vdc, I_B = 0)	I_{CEO}	—	—	0.5	μAdc
DYNAMIC CHARACTERISTICS					
Low Frequency Noise Figure (V_{CE} = 3.0 Vdc, I_C = 100 μAdc, R_S = 1.0 kΩ, f = 1.0 kHz)	NF	—	3.25	—	dB
Forward Current Transfer Ratio (V_{CE} = 3.0 Vdc, I_C = 1.0 mAdc, f = 1.0 kHz)	h_{FE}	—	110	—	—
Short Circuit Input Impedance (V_{CE} = 3.0 Vdc, I_C = 1.0 mAdc)	h_{ie}	—	3.5	—	kΩ
Open Circuit Output Impedance (V_{CE} = 3.0 Vdc, I_C = 1.0 mAdc)	h_{oe}	—	15.6	—	μmhos
Reverse Voltage Transfer Ratio (V_{CE} = 3.0 Vdc, I_C = 1.0 mAdc)	h_{re}	—	1.8	—	$x10^{-4}$
Forward Transfer Admittance (V_{CE} = 3.0 Vdc, I_C = 1.0 mAdc, f = 1.0 MHz)	y_{fe}	—	31–j1.5	—	—
Input Admittance (V_{CE} = 3.0 Vdc, I_C = 1.0 mAdc, f = 1.0 MHz)	y_{ie}	—	0.3 + j0.04	—	—
Output Admittance (V_{CE} = 3.0 Vdc, I_C = 1.0 mAdc, f = 1.0 MHz)	y_{oe}	—	0.001 + j0.03	—	—
Current-Gain — Bandwidth Product (V_{CE} = 3.0 Vdc, I_C = 3.0 mAdc)	f_T	300	550	—	MHz
Emitter-Base Capacitance (V_{EB} = 3.0 Vdc, I_E = 0)	C_{eb}	—	0.6	—	pF
Collector-Base Capacitance (V_{CB} = 3.0 Vdc, I_C = 0)	C_{cb}	—	0.58	—	pF
Collector-Substrate Capacitance (V_{CS} = 3.0 Vdc, I_C = 0)	C_{CI}	—	2.8	—	pF

Figure 1. Collector Cutoff Current versus Temperature (Each Transistor)

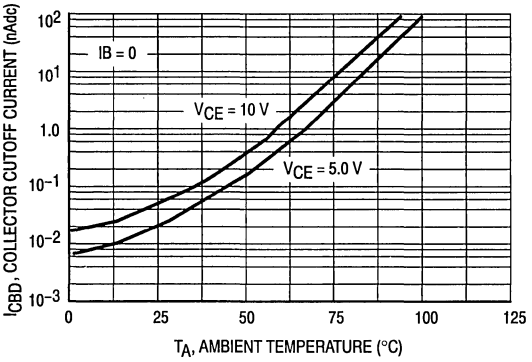


Figure 2. Collector Cutoff Current versus Temprature (Each Transistor)

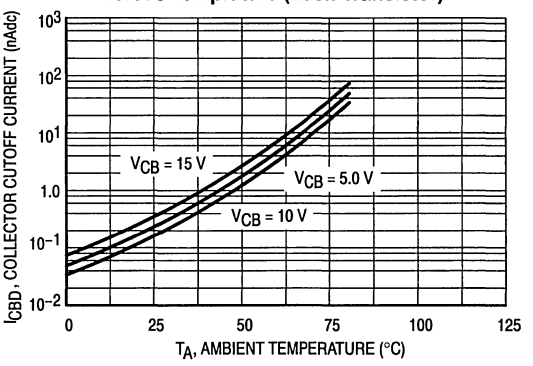


Figure 3. Input Offset Characteristics for Q1 and Q2

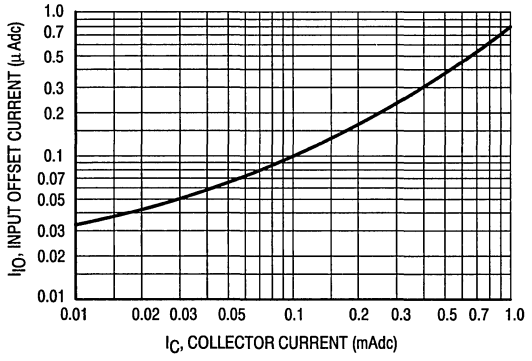


Figure 4. Base-Emitter and Input Offset Voltage Characteristics

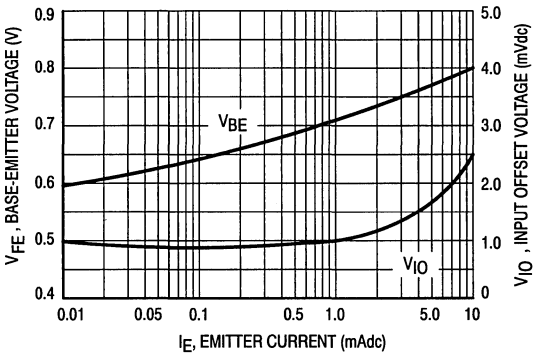
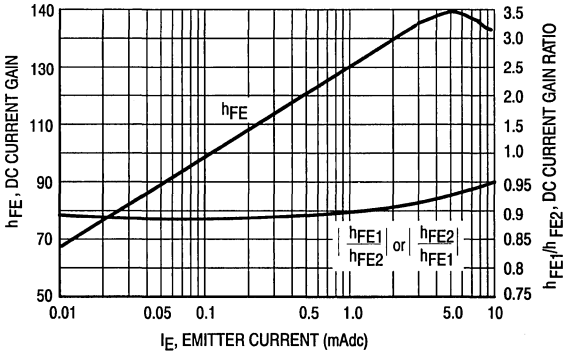


Figure 5. DC Current Gain



9

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

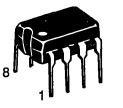
MC3373

Remote Control Amplifier/Detector

REMOTE CONTROL WIDEBAND AMPLIFIER WITH DETECTOR

The MC3373 is intended for application in infrared remote controls. It provides the high gain and pulse shaping needed to couple the signal from an IR receiver diode to the tuning control system logic.

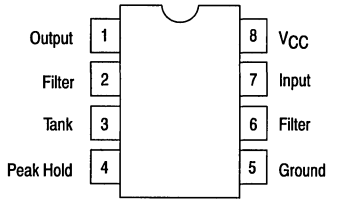
- High Gain Pre-Amp
- Envelope Detector for PCM Demodulation
- Simple Interface to Microcomputer Remote Control Decoder
- Use with Tuned Circuit for Narrow Bandwidth, Lower Noise Operation
- Minimum External Components
- Wide Operating Supply Voltage Range
- Low Current Drain
- Improved Retrofit for NEC Part No. μPC1373
- MC14497 Recommended IR Transmitter
- MLED81 Complementary Emitter
- MRD821 Complementary Detector Diode



P SUFFIX
PLASTIC PACKAGE
CASE 626

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO-8)

PIN CONNECTIONS



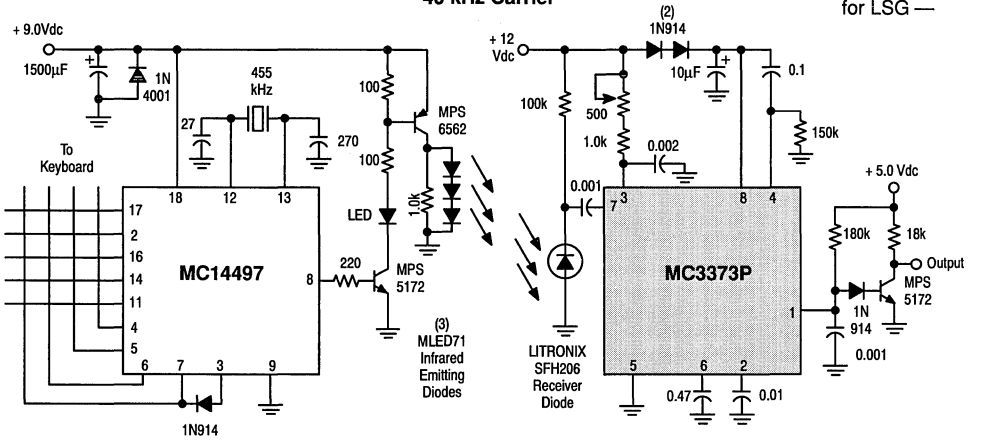
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	15	Vdc
Operating Temperature Range	T_A	0 to 75	°C
Storage Temperature Range	T_{stg}	–55 to +125	°C
Junction Temperature	T_J	150	°C
Power Dissipation, Package Rating Derate above 25°C	P_D $1/\theta_{JA}$	1.25 10	W mW/°C

9

Figure 1. Remote Control Application
40 kHz Carrier

Was this redrawn for LSG —



RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min	Typ	Max	Unit
Power Supply Voltage (25°C)	V_{CC}	4.75	—	15	Vdc
Power Supply Voltage (0°C)	V_{CC}	5.0	—	15	Vdc
Input Frequency	f_{in}	30	40	80	kHz

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V, f_{in} = 40 kHz, Test circuit of Figure 2)

Characteristics	Symbol	Min	Typ	Max	Unit
Power Supply Current	I_{CC}	1.5	2.5	3.5	mAdc
Input Terminal Voltage	V(Pin 7)	2.4	2.8	3.0	Vdc
Input Voltage Threshold	V_{in}	—	50	100	μVp-p
Input Amplifier Voltage Gain (V[Pin 3] = 500 mVp-p)	A_V	—	60	—	dB
Input Impedance	r_{in}	40	60	80	kΩ
Output Voltage, V_{in} = 1.0 mVp-p	V_{OL}	—	—	0.5	V
Output Leakage, V_{CC} = V_{OH} = 15 Vdc	I_{OH}	—	—	2.0	μA
Output Voltage, Input Open	V_{OH}	—	—	5.0	Vdc

NOTE: See AN1016 for IR System Information.

Figure 2. Test Circuit

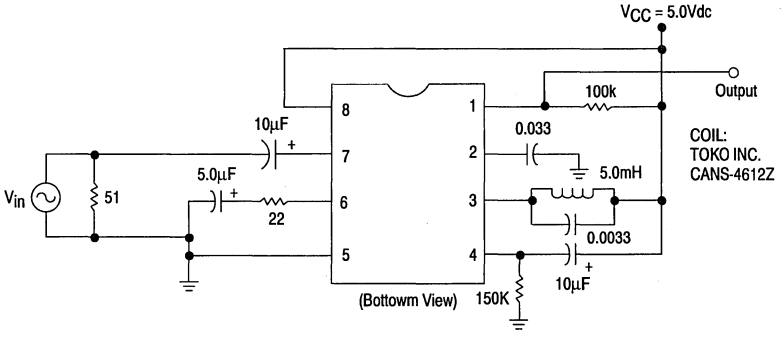


Figure 3. Block Diagram

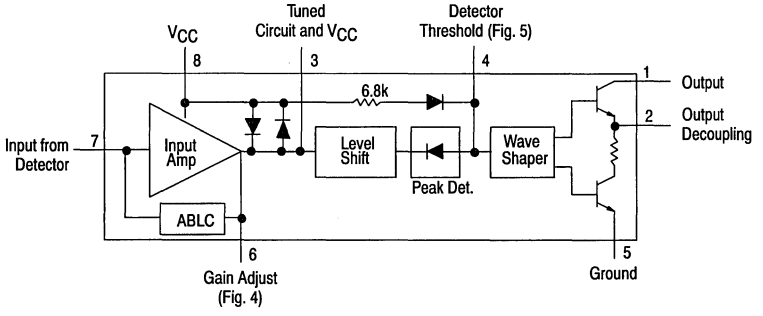


Figure 4. Input Amplifier Gain

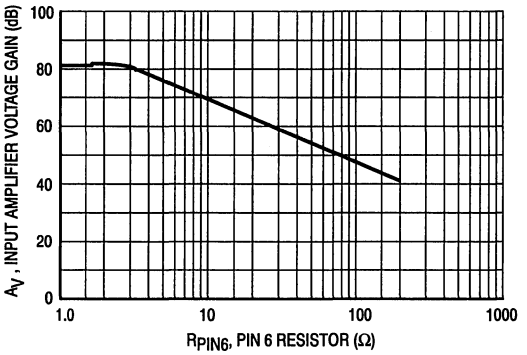
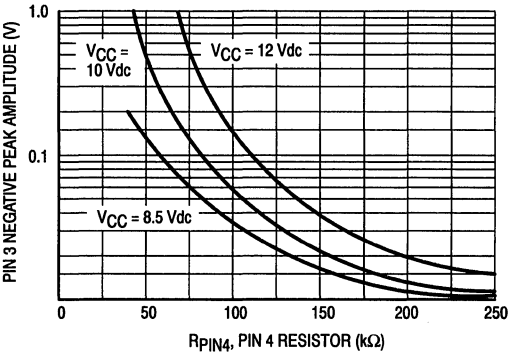


Figure 5. Detector Threshold

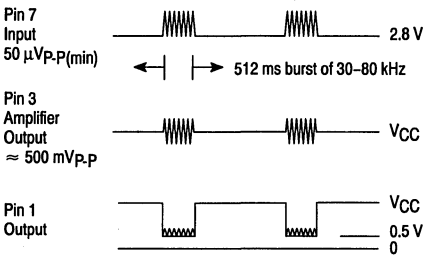


APPLICATIONS INFORMATION

The MC3373 is a specialized high gain amplifier/signal processor bipolar analog IC designed to be the core of infrared carrier signaling systems. The amplifier section has an Automatic Bias Level Control **(ABLC)** for simplified direct connection to an IR detector diode. Generally, it is operated AC coupled, utilizing an input high-pass filter to eliminate power line related noise, particularly that from florescent and gas vapor lamps. The use of a high frequency carrier is strongly recommended as opposed to simply detecting "DC" bursts of IR energy. In the carrier mode setup the MC3373 acts like an AM receiver subsystem, amplifying the incoming signal, demodulating it, and providing some basic wave shaping of the demodulated envelope. The tuned circuit at Pin 3 provides the main system selectivity reducing random noise interference and permitting multichannel operation in the same physical area without falsing. In the multichannel case the carriers must not be harmonically related. The bandwidth is determined primarily by the "Q" of the coil. Bandwidth may be increased by loading, shunting, the coil with a resistor.

Since this is a very high gain system operating at relatively high frequencies, care **must** be taken in the circuit layout and construction. Do not use wire wrap or non-ground plane protoboard. A simple single sided PCB with ground fill or a two-sided board with a solid groundplane and top side point-to-point will provide consistent high performance. There is a wide array of IR emitter/detectors available. The Motorola MLED81 and MRD821 are an excellent low cost combination to use with the MC3373. Multiple emitters are recommended for extended range. Application note AN1016 is must reading as it covers basic IR systems and specific applications.

Figure 6. Typical Signal Waveforms



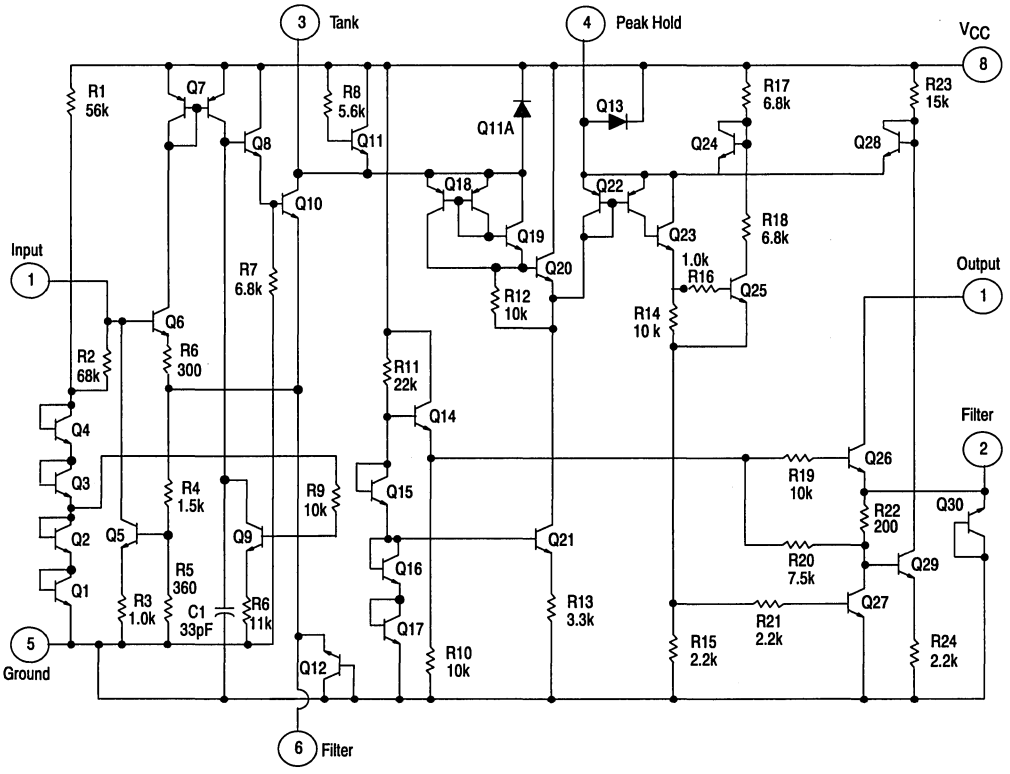
The input amplifier gain is approximately equal to the load impedance at Pin 3, divided by the resistor from Pin 6 to ground. Again, the low frequency gain can be reduced by using a small coupling capacitor in series with the Pin 6 resistor.

The load may be resistive, with only, or tuned, as in the test circuit. The amplifier output is limited by back-to-back clamping diodes, level shifted, buffered and fed to a negative peak detector. The detector threshold is set by the external resistor on Pin 4, and an internal 6.8 kΩ resistor and diode to V_{CC}. The capacitor from V_{CC} to Pin 4 quickly charges during the negative peaks and then settles toward the set-up voltage between signal bursts at a rate roughly determined by the value of the capacitor and the 6.8 k resistor. The external capacitor at Pin 2 filters the ultrasonic carrier from the pulses.

CIRCUIT DESCRIPTION

Q1 to Q4 set the bias on the amplifier input at approximately 2.8 V. Q6 to Q10 form the input amplifier, which has a gain of about 80 dB when R(Pin 6) = 0, Q5 sinks input current from the photo diode and keeps the amplifier properly biased. Q18 to Q20 level shift and buffer the signal to the negative peak detector, Q22 and Q23. Output devices Q26 and Q27 conduct during peaks and pull the output (Pin 1) low. The capacitor on Pin 2 filters out the carrier.

Figure 7. Internal Schematic



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC13001XP
MC13007XP

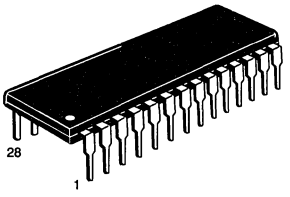
Monomax Black and White TV Subsystem

MONOMAX
BLACK AND WHITE TV SUBSYSTEM

SILICON MONOLITHIC INTEGRATED CIRCUITS

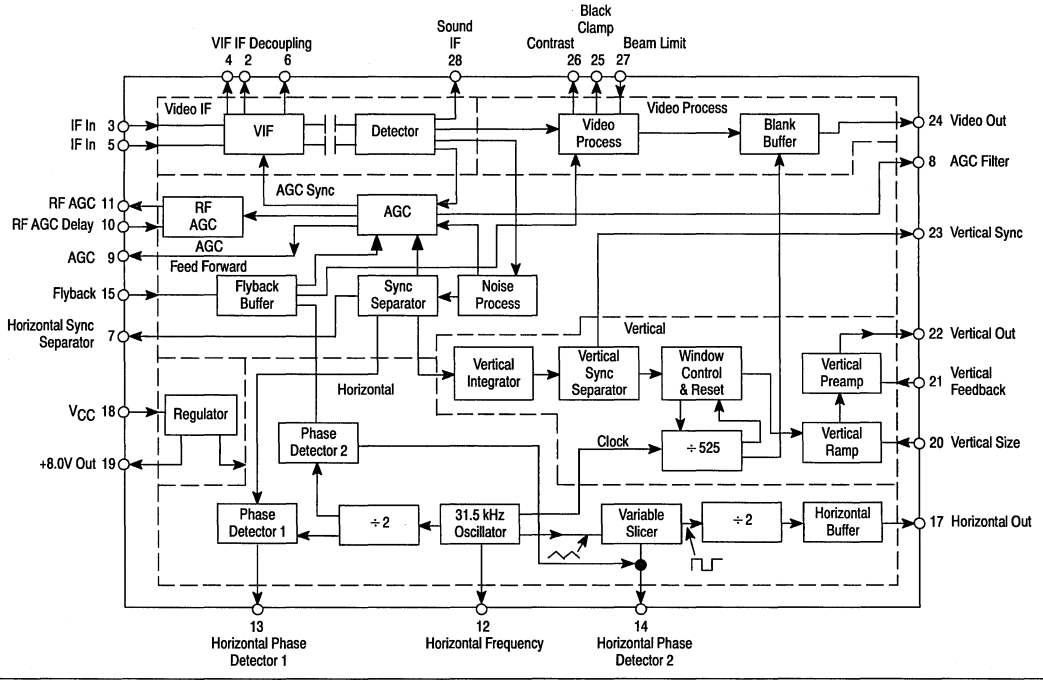
The MONOMAX is a single-chip IC that will perform the electronic functions of a monochrome TV receiver, with the exception of the tuner, sound channel, and power output stages. The MC13001XP and MC13007XP will function as a drop-in replacement for the MC13001P and MC13007P, but some external IF components can be removed for maximum benefit. IF AGC range has been increased, video output impedance lowered, and horizontal driver output current capability increased.

- Full Performance Monochrome Receiver with Noise and Video Processing (Black Level Clamp, DC Contrast, Beam Limiter)
- Video IF Detection On-Chip (No Coils, No Pins, except Inputs)
- Noise Filtering On-Chip (Minimum Pins and Externals)
- Oscillator Components On-Chip (No Precision Capacitors Required)
- MC13001XP for 525 Line NTSC and MC13007XP for 625 Line CCIR
- Low Dissipation in All Circuit Sections
- High Performance Vertical Countdown
- 2-Loop Horizontal System with Low Power Start-Up Mode
- Noise Protected Sync and Gated AGC System
- Designed to work with TDA1190P or TDA3190P Sound IF and Audio Output Devices



P SUFFIX
PLASTIC PACKAGE
CASE 710

Figure 1. Basic Elements of the System



MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage — Pin 18	V_{CC}	+16	Vdc
Power Dissipation	P_D	1.0	W
Horizontal Driver Current — Pin 17	I_{hor}	−20	mA
RF AGC Current — Pin 11	I_{RFAGC}	20	mA
Video Detector Current — Pin 24	I_{VID}	5.0	mA
Vertical Driver Current — Pin 22	I_{vert}	5.0	mA
Auxiliary Regulator Current — Pin 19	I_{reg}	35	mA
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	60	°C/W
Maximum Junction Temperature	T_J	150	°C
Storage Temperature Range	T_{stg}	−65 to + 150	°C
Operating Temperature Range	T_A	0° to + 70	°C

RECOMMENDED OPERATING CONDITIONS

Rating	Symbol	Value	Unit
Horizontal Output Drive Current	I_{hor}	≤10	mA
RF AGC Current	I_{RFAGC}	≤10	mA
Regulator Current	I_{reg}	≤20	mA

ELECTRICAL CHARACTERISTICS (V_{CC} = 11.3 V, T_A = 25°C)

Characteristics		Symbol	Min	Typ	Max	Unit
Power Supply Current	Pins 18, 19	I_{CC}	44	—	76	mA
Regulator Voltage	Pin 19	V_{reg}	7.2	8.2	8.8	Vdc

HORIZONTAL SPECIFICATIONS

Oscillator Frequency (Nominal)	Pin 12	$f_{hor(NOM)}$	13	—	19	kHz
Oscillator Sensitivity			—	230	—	Hz/μA
Start-Up Frequency (I_{18} = 4.0 mA)		f_{hor}	−10	—	+10	%
Oscillator Temperature Stability (0 ≤ TA ≤ 75°C)		—	—	50	—	Hz
Phase Detector 1 (Charge/Discharge Current) (Non-Standard Frame) (Standard Frame)		$I_{\phi 1}$	 — —	 ±900 ±400	 — —	μA
Phase Detector 2 (Charge/Discharge Current)		$V_{\phi 2}$	—	+1.0 −0.6	—	mA
Phase Detector 1 (Output Voltage Limits)		$V_{\phi 1}$	—	7.5 (max) 2.5 (min)	—	Vdc
Phase Detector 2 (Output Voltage Limits)		$V_{\phi 1}$	—	7.7 (max) 1.5 (min)	—	
Phase Detector 1 (Leakage Current)			—	—	2.0	μA
Phase Detector 2 (Leakage Current)			—	—	3.0	
Horizontal Delay Range (Sync to Flyback)			— —	18 (max) 5.0 (min)	— —	μs
Horizontal Output Saturation Voltage (I_{17} = 15 mA)		$V_{17(sat)}$	—	—	0.3	Vdc
Phase-Detector 1 (Gain Constant) (Out-of-Lock) (In-Lock)			 — —	 5.0 10	 — —	μA/μs
Horizontal Pull-In Range			±500	±750	—	Hz

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VERTICAL SPECIFICATIONS

Characteristics		Symbol	Min	Typ	Max	Unit
Output Current	Pin 22	I_{22}	–0.6	—	—	mA
Feedback Leakage Current	Pin 21	I_{21}	—	—	6.0	µA
Feedback Maximum Voltage		V_{21}	—	5.1	—	Vdc
Ramp Retrace Current	Pin 20	I_{20}	500	—	900	µA
Ramp Leakage Current	Pin 20		—	—	0.3	µA

IF SPECIFICATIONS

Regulator Voltage	V_4	—	7.5	—	Vdc
Input Bias Voltage	$V_{2,6}$	—	4.2	—	
Input Resistance	R_{in}	—	6.0	—	kΩ
Input Capacitance (V_{AGC} Pin 8 = 4.0 V)	C_{in}	—	2.0	—	pF
Sensitivity (V_8 = 0 V, 400 Hz 30% MOD, V_{28} = 0.8 V_{pp})		—	80	—	μV_{rms}
Bandwidth	BW	—	75	—	MHz

VIDEO SPECIFICATIONS

Zero Carrier Voltage (See Figure 5)	Pin 28		—	7.0	—	Vdc
Output Voltage (See Figure 6) White to Back Porch	Pin 24		—	1.4	—	V
Differential Gain			—	6	—	%
Differential Phase (IRE Test Method)				4		Degrees
Contrast Bias Current	Pin 26	I_{26}	—	10	—	µA
Contrast Control Range			—	14:1	—	
Beam Limiting Voltage	Pin 27	V_{27}	—	1.0	—	Vdc

AGC & SYNC

RF (Turner AGC Output Current (V_{11} = 5.5 V)	I_{11}	5.0	—	—	mA
AGC Delay Bias Current	I_{10}	—	–10	—	µA
AGC Feedforward Current	I_9	—	1.0	—	mA
AGC Threshold (Sync Tip at Pin 28)	V_{28}	4.7	—	5.1	Vdc
Sync Separator Operating Point	V_7	—	4.2	—	Vdc
Sync Separator Charge Current	I_7	—	5.0	—	mA

Figure 2. Monomax AGC Characteristics

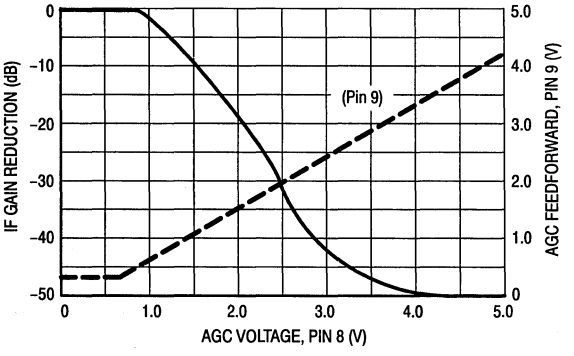
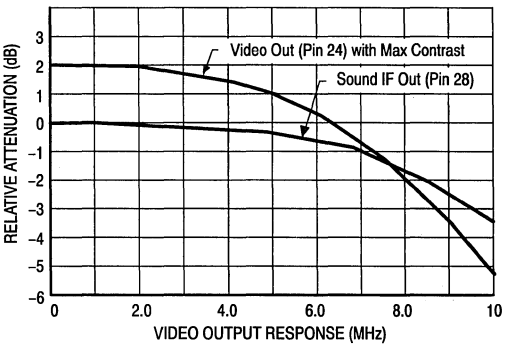


Figure 3. Video Output Response



GENERAL DESCRIPTION

The Video IF Amplifier is a four-stage design with 80 μV, sensitivity. It uses a 6.2 V supply decoupled at Pin 4. The first two stages are gain controlled, and to ensure optimum noise performance, the first stage control is delayed until the second stage has been gain reduced by 15 dB. To bias the amplifier, balanced DC feedback is used which is decoupled at Pins 2 and 6 and then fed to the input Pins 3 and 5 by internal 3.9 k resistors. The nominal bias voltage at these input pins is approximately 4.2 Vdc. The input, because of the high IF gain, should be driven from a balanced differential source. For the same reason, care must be taken with the IF decoupling.

The IF output is rectified in a full wave envelope detector and detector nonlinearity is compensated by using a similar nonlinear element in a feedback output buffer amplifier. The detected 1.9 V_{p-p} video at Pin 28 contains the sound intercarrier signal, and Pin 28 is normally used as the sound takeoff point. The video frequency response, detector to Pin 28, is shown in Figure 3 and the detector intermodulation performance can be seen by reference to Figure 4. Typical Pin 28 video waveforms and voltage levels are shown in Figure 5.

The video processing section of Monomax contains a contrast control, black level clamp, a beam current limiter and composite blanking. The video signal first passes through the contrast control. This has a range of 14:1 for a 0 V to 5.0 V change of voltage on Pin 26, which corresponds to a change of video amplitude at Pin 24 of 1.4 V to 0.1 V (black to white level). the beam current limiter operates on the contrast control, reducing the video signal when the beam current exceeds the limit set by external components. As the beam current increases, the voltage at Pin 27 moves negatively from its normal value of 1.5 V, and at 1.0 V operates the contrast control, thus initiating beam limiting action. After the contrast control, thus initiating beam limiting action. After the contrast control, the video is passed through a buffer amplifier and DC restored by the black level clamp circuit before being fed to Pin 24 where it is blanked. The black level clamp, which is gated "on" during the second half of the flyback, maintains the video black level at 2.4 V ± 0.1 V under all conditions, including changes in contrast, temperature and power supply. The loop

Figure 4. Detector Products

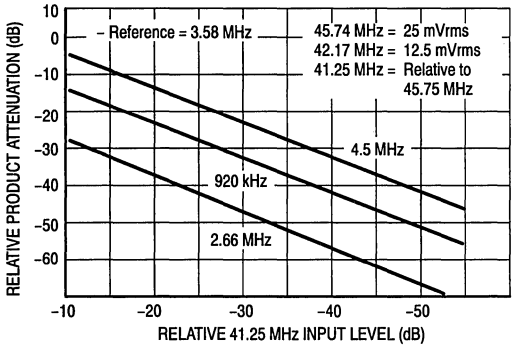


Figure 5. Pin 28 Sound Output

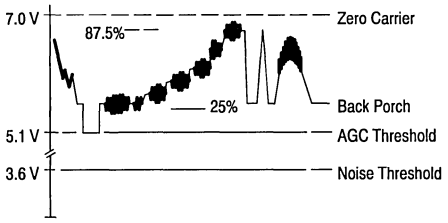
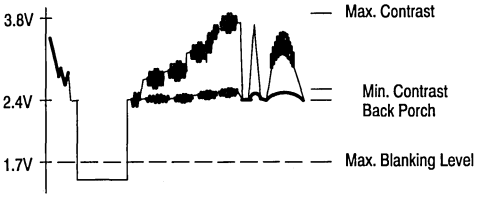


Figure 6. Pin 24 Video Output



integratng capacitor is at Pin 25 and is normally at a voltage of 3.3 V. The frequency response of the video at Pin 24 is shown in Figure 3 and it is blanked to within 0.5 V of ground.

The AGC loop is a gated system, and for all normal variations of the IF input signal maintains the sync tip of a noise filtered video signal at a reference voltage (5.1 V Pin 28). The strobe for the AGC error amplifier is formed by gating together the flyback pulse with the separated sync pulse. Integration of the error signal is performed by the capacitor at Pin 8, which forms the dominant AGC time constant. Improved noise performance is obtained by the use of a gated AGC system, noise protected by a DC coupled noise canceling circuit. The false AGC lock conditions, which can result from this combination, are prevented by an anti lockout circuit connected to the sync separator at Pin 7. AGC lockout conditions, which occur due to large rapid changes of signal level are detected at Pin 7 and recovery is ensured under these conditions by changing the AGC into a mean level system. The voltage at Pin 10 sets the point at which tuner AGC takeover occurs and positive going tuner control, suitable for an NPN RF transistor, is available at Pin 11. The maximum output is 5.5 V at 5.0 mA. A feed-forward output is provided at Pin 9. This enables the AGC control voltage to be AC coupled into the tuner takeover control at Pin 10. The coupling allows additional IF gain reduction during signal transient conditions, thus compensating for variations of AGC loop gain at the tuner AGC takeover point. In this way the AGC system stability and response are not degraded.

The previously mentioned noise protection is effected by detecting negative-going noise spikes at the video detector

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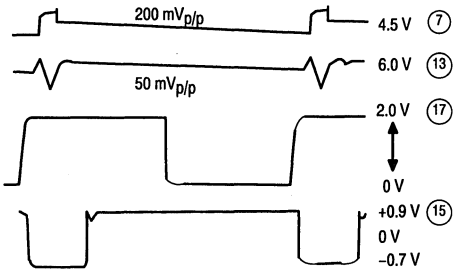
output. A DC coupled detector is used which turns on when a noise spike exceeds the video sync tip by 1.4 V. This pulse is then stretched and used to cancel the noise present on the delayed video at the input to the sync separator. Cancellation is performed by blanking the video to ground. Complete cancellation of the noise spike results from the stretching of the blanking pulse and the delay of the noise spike at the input to the sync separator. Protection of both the horizontal PLL and the AGC stems from the fact that both circuits use the noise cancelled sync for gating.

The composite sync is stripped from a delayed and filtered video in a peak detecting type of sync separator. The components connected to Pin 7 determine the slice and tilt levels of the sync separator. For ideal horizontal sync separation and to ensure correct operating of AGC anti-lockup circuit, a relatively short time constant is required at Pin 7. this time constant is less than optimum for good noise free vertical separation, giving rise to a vertical slice level near sync tip. An additional, longer, time-constant is therefore coupled to the first via a diode. With the correct choice of time constants, the diode is non conducting during the horizontal sync period, but conducts during the longer vertical period. This connects the longer time constant to the sync separator for the vertical period and stops the slice level from moving up the sync tip. The separated composite sync is integrated internally, and the time constant is such that only the longer period vertical pulses produce a significant output pulse. The output is then fed to the vertical sync separator, which further processes the vertical pulse and provides increased noise protection. The selection of the external components connected to the vertical separator at Pin 23 permits a wide range of performance options. A simple resistor divider from the 8.2 V regulated supply gives adequate performance for most conditions. The addition of an RC network will make the slice level adapt to varying sync amplitude and give improved weak signal performance. A resistor to the AGC voltage on Pin 9 enables the sync slice level to be changed as a function of signal level. This further improves the low signal level separation while at the same time giving increased impulse noise protection on strong signals.

Horizontal Oscillator

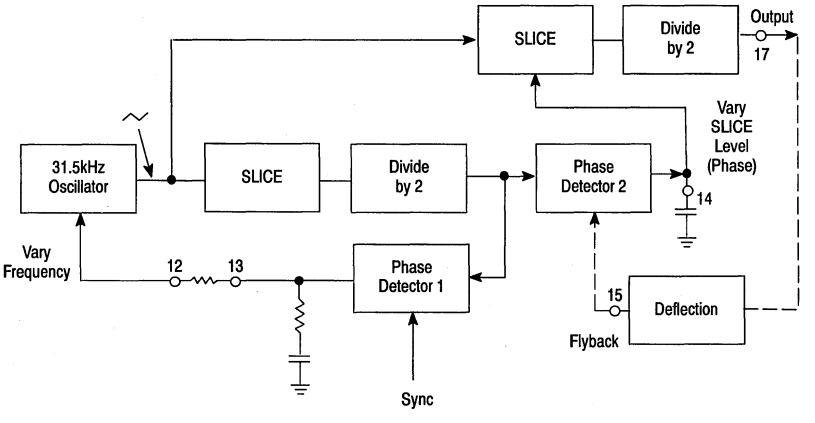
The horizontal PLL (see Figure 7) is a 2-loop system using a 31.5 kHz oscillator which after a divider stage is locked to the sync pulse using Phase Detector 1. The control signal derived from this phase detector on Pin 13 is fed via a high-value resistor to the frequency-control point on Pin 12. The same divided oscillator frequency is also fed to Phase Detector 2, where the flyback pulse is compared with it and the resulting error used to change a variable slice level on the oscillator ramp waveform. This therefore changes the timing of the output square wave from the slicer and hence the timing of the buffered horizontal output on Pin 17 (see Figure 8). The error on Phase Detector 2 is reduced until the phasing of the flyback pulse is correct with respect to the divided oscillator waveform, and hence with respect to the sync pulse.

Figure 8. Horizontal Waveforms



To improve the pull-in and noise characteristics of the first PLL, the phase detector current is increased when the vertical lock indicator signals an unlocked condition and is decreased when locked. This increases the loop bandwidth and pull-in range when out of lock and decreases the loop bandwidth when in lock, thus improving the noise performance. In addition, the phase detector current during the vertical period is reduced in order to minimize the disturbance to the horizontal caused by the longer period vertical phase detector pulses.

Figure 7. Horizontal Oscillator Systems



The oscillator itself is a novel design using an on-chip 50 pF silicon nitride capacitor which has a temperature drift of only 70 ppm/°C and negligible long term drift. This, in conjunction with an external resistor, gives a drift of horizontal frequency of less than 1.0 Hz/°C — i.e., less than 100 Hz over the full operating temperature range of the chip. The pull-in range of the PLL is about ±750 Hz, so normally this would eliminate the need for any customer adjustment of the frequency.

The second significant feature of this design is the use of a virtual ground at the frequency control point which floats at a potential derived from a divider across the power supply and this is the same divider which determines the end-points of the oscillator ramp. The frequency adjustment which is necessary to take up tolerances in the on-chip capacitor is fed in as a current to this virtual ground and when this adjustment current is derived from an external potentiometer across the same supply there is no frequency variation with supply voltage. Moreover, using the voltage from a potentiometer for the adjustment instead of the simple variable resistor normally used in RC oscillators make the frequency independent of the value of the potentiometer and hence its temperature coefficient. The frequency control current from the first phase detector is fed into this same virtual ground and as the sensitivity of the control is about 230 Hz/μA a high value resistor can be used (680 kΩ) and this can be directly connected to the phase detector filter without significant loading.

This oscillator operates with almost constant frequency to below 4.0 V and as the total PLL system consumes less than 4.0 mA at this voltage, this gives an ideal start-up characteristic for receivers using deflection-derived power supplies.

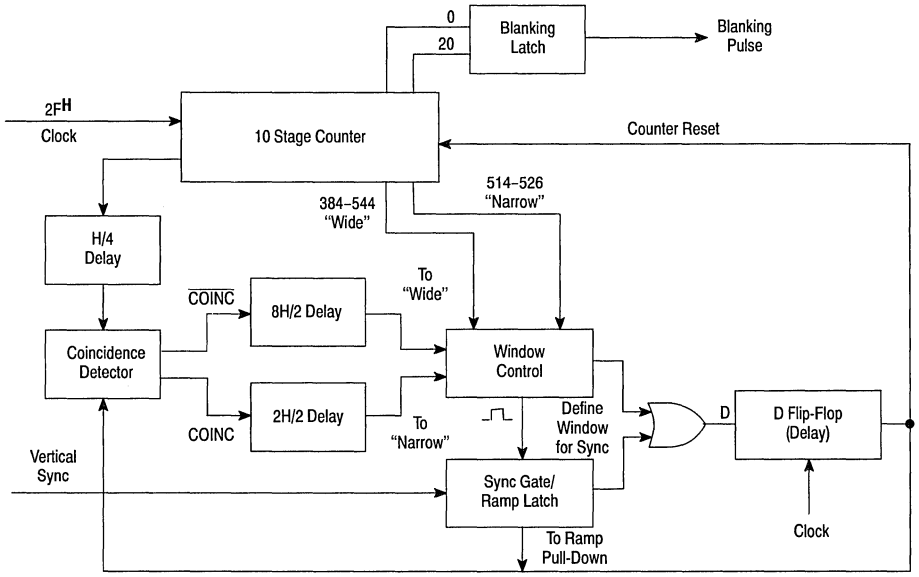
The flyback gating input is on Pin 15 which is internally clamped to 0.7 V in both directions and requires a negative input current of 0.6 mA to operate the gate circuit. This input can be a raw flyback pulse simply fed via a suitable resistor.

Vertical System

An output switching signal is taken from the 31.5 kHz oscillator to clock the vertical counter which is used in place of a conventional vertical oscillator circuit. The counter is reset by the vertical sync pulse but the period during which it is permitted to reset is controlled by the window control. Normally, when the counter is running synchronously, the window is narrow to give some protection against spurious noise pulses in the sync signal. If the counter output is not coincident with sync however, after a short period the window opens to five reset over a much wider count range, leading to a fast picture roll towards lock. At weak signal, i.e., less than 200 μV IF input, the vertical system is forced to narrow mode to give a steadier picture for commonly occurring types of noise. The vertical sync, gated by the counter, then resets a ramp generator on Pin 20 and the 1.5 V_{p-p} ramp is buffered to Pin 22 by the vertical preamplifier. A differential input to the preamp on Pin 21 compares the signal generated across the resistor in series with the deflection coils with the generated ramp and thus controls shape and amplitude of the coil current.

The basic block diagram of the countdown system is shown in Figure 9. The 31.5 kHz ($2F^H$) clock from the horizontal oscillator drives a 10-stage counter circuit which is normally reset by the vertical sync pulse via the sync gate, "OR" gate and D flip-flop. This D input is also used to initiate discharge of the ramp capacitor and hence causes picture flyback.

Figure 9. Monomax Vertical Countdown

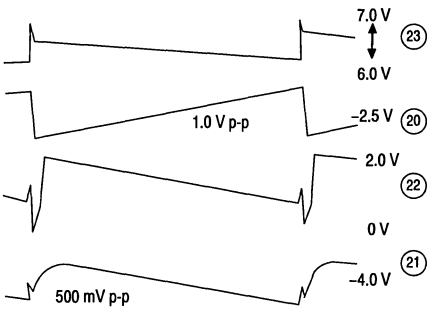


The period during which sync can reset the counter and cause flyback is determined by the window control which defines a count range during which the gate is open. One of two ranges is selected according to the condition of the signal. The normal "narrow" range is 514 to 526 counts for a 525 line system and is selected after the coincidence detector indicates that the reset is coincident, twice in succession, with the 525 count from the counter. When the detector indicates non-coincidence 8 times in succession, then the window control switches to the "wide" mode (384 to 544 counts) to achieve rapid re-synchronization. For the 625 line version the counts are 614 to 626 for narrow mode and 484 to 644 for wide mode. Note that the OR gate after the sync gate is used to terminate the count at the end of the respective window if a sync pulse has not appeared.

This method accepts non-standard signals almost in the same way as a conventional triggered RC oscillator and has a similar fast lock-in time. However, the use of a window control on the counter reset ensures that when locked with a normal standard broadcast signal the counter will reject most spurious noise pulse.

The blanking output is provided from a latch which is set by the counter reset pulse and terminated by count 20 from the counter chain.

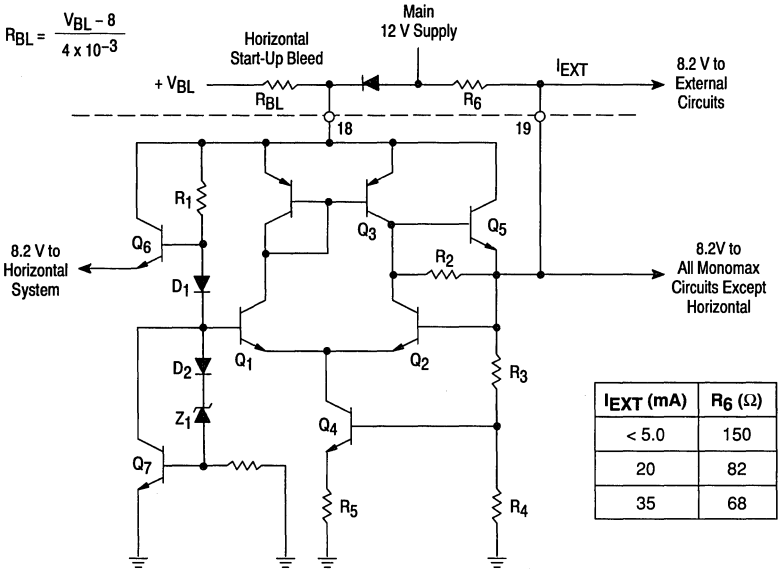
Figure 10. Vertical Waveforms



Power Supply

The power supply regulator, although of simple design, provides two independent power supplies — one for the horizontal PLL section and the other for the remainder of the chip. The supplies share the same reference voltage but the design of the main regulator is such that it can be switched on independently to give minimum loading on the "bleed" voltage source during start-up phase of a defection-derived supply system.

Figure 11. Power Supply Circuit



I_{EXT} (mA)	R_6 (Ω)
< 5.0	150
20	82
35	68

Figure 12. Test Circuit Diagram

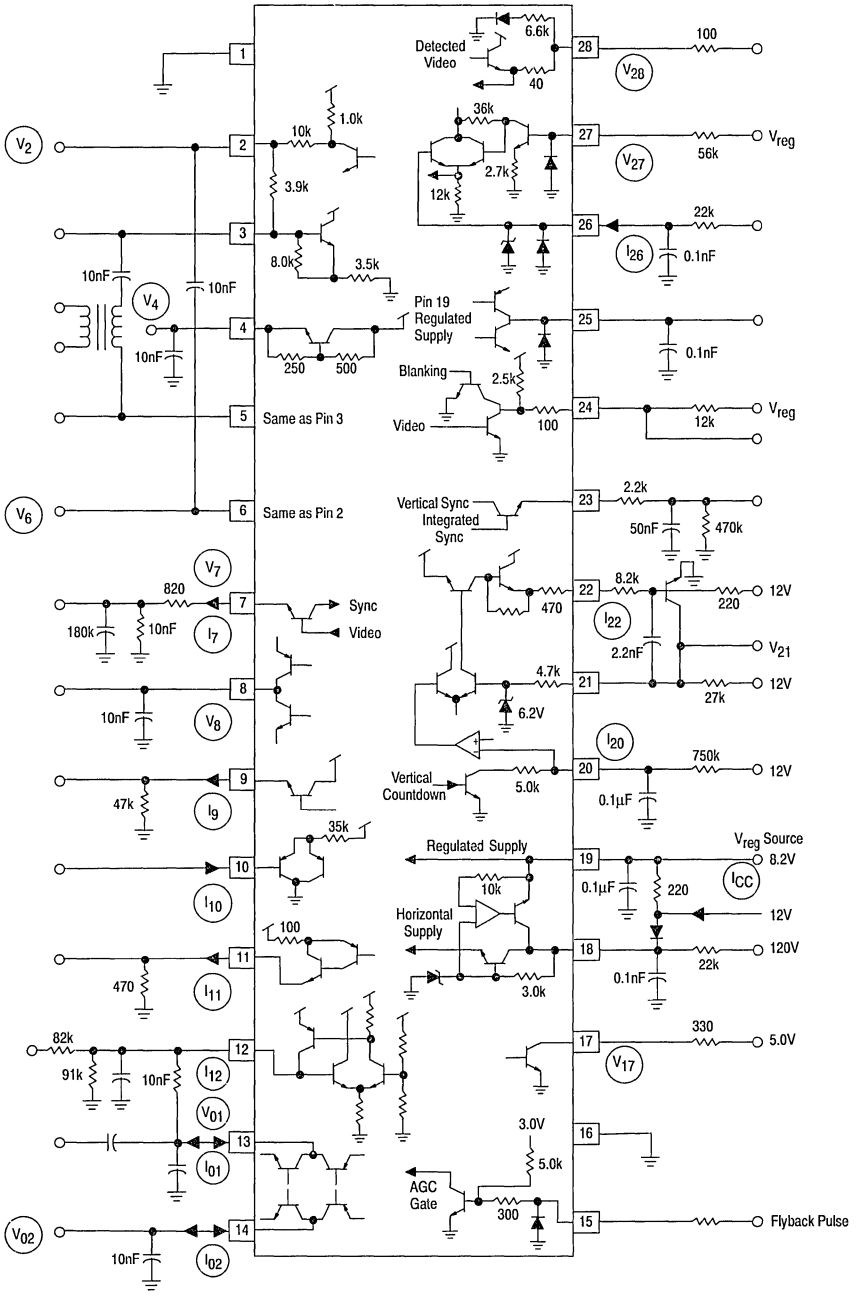
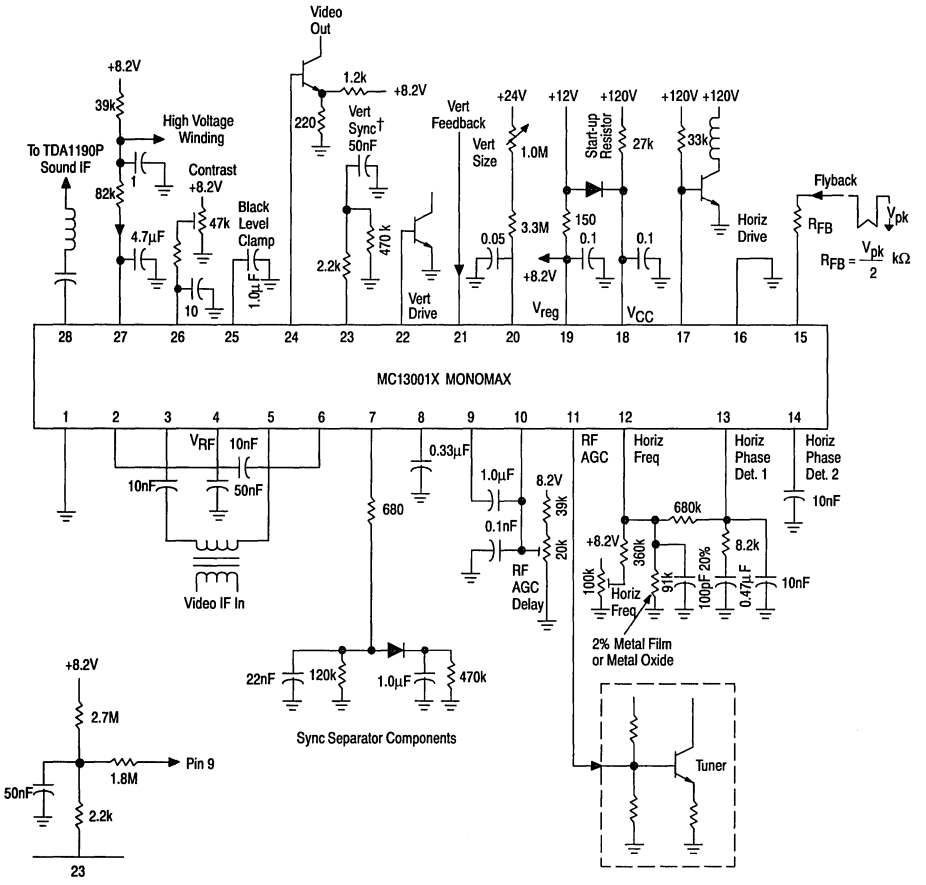


Figure 13. Typical Application



†Vertical Sync, optional components for extra performance with low signal strength.

See Application Note AN879 for further information.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC13017

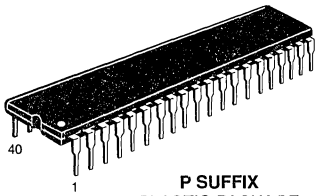
NTSC/PAL CHROMA 10 COLOR TV and TIMEBASE PROCESSOR

Product Preview

NTSC/PAL Chroma 10 Color TV and Timebase Processor

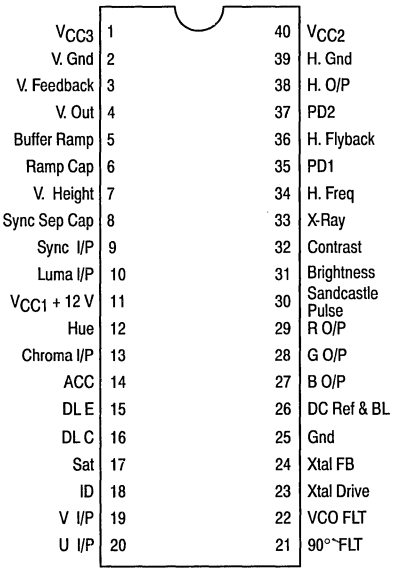
The MC13017 consists of all the necessary circuits for TV NTSC/PAL decoding and timebase processing. It forms a kit set with the MC44301 VIF and the TDA3190 Sound IF and Power for a low cost, high performance CTV system.

- On-Chip Sync Separator
- Dual Loop Horizontal Timebase
- Direct Locked Vertical Counter
- X-Ray Protection
- Noise Blanking on Sync Separator
- NTSC/PAL Color Decoding
- Direct Interface with SECAM TDA3030B
- 4.43/3.579 MHz Crystal Reference
- Three DC High Impedance Control Outputs for Contrast, Brightness, and Saturation
- 12 V Supply
- Vertical Ramp Buffer Output
- Sandcastle Output
- Hue Control



P SUFFIX
PLASTIC PACKAGE
CASE 711

PIN CONNECTIONS



(Top View)

MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltages	V_{CC1}, V_{CC3} V_{CC2}	15 10	V
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	– 55 to +125	°C
Horizontal Output Voltage Vertical Output Voltage	V_{OH} V_{OV}	8.0 4.0	V

ORDERING INFORMATION

Device	Temperature Range	Package
MC13017P	0° to + 70°C	Plastic DIP

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PIN FUNCTION DESCRIPTION

Pin	Function	Description
1	V_{CC3}	+12 V supply for V_{CC2} power regulator.
2	Vert Gnd	Vertical output analog ground.
3	Vert Feedback	The Ramp on Pin 6 is internally inverted, level shifted and subtracted from the input to Pin 3. The result appears as an output on an open collector at Pin 4.
4	Vert Out	Vertical ramp output to external vertical power drive.
5	Buffer Ramp	The vertical buffer ramp output of Pin 6.
6	Ramp Cap	The external cap is charged by a current controlled through vertical height control Pin 7 to produce a vertical ramp. The discharge of the cap is controlled internally by the vertical counter.
7	Vert Height	Current input for vertical height control.
8, 9	Sync Sep Cap, Sync I/P	Sync separator input is a NPN transistor stage with the signal presented at its base with a peak level of about 4.0 V. The emitter is brought out to Pin 8 through a 200 Ω resistor so that a capacitor with a series resistor may be connected. The circuit behaves as a peak detector with a slicing level controlled by the choice of charge and discharge resistors. An additional time constant is connected through a diode to prevent the slice level from riding up on the field sync.
11	V_{CC1}	+12 V supply for chroma.
12	Hue	This is Hue control for NTSC system. It should be connected to V_{CC1} at PAL system. When voltage at Pin 12 is smaller than 8.0 V, NTSC mode is selected.
15	DL E	Delay line drive open emitter terminal.
16	DL C	Delay line drive open collector terminal.
18	ID Filter	An external filter cap is connected at this pin for ID circuit.
19, 20	V, U	V, U inputs after delay line to detectors.
21	90° Filter	90° phase shifter filter.
22	VCO Filter	Color reference VCO filter.
23 24	Xtal 2 Xtal 1	A 4.43 MHz (PAL), or 3.579 MHz (NTSC) crystal is connected to the internal VCO for color subcarrier reference frequency.
30	Sandcastle Pulse Output	The Sandcastle Pulse Output is delivered through 200 Ω from an emitter-follower with 10 kΩ pull-down. The blanking duration is determined by the applied flyback pulse. The burst gate determined by the second half of the flyback levels are: Blanking (4.0 V), Burst Gate (11 V).
35	PD1	Horizontal phase detector current output. The PLL 1 is locked to the sync input with 2H oscillator.
36	Horiz Flyback	Horizontal flyback, a positive input pulse exceeded threshold of 1.0 V is required, input impedance is between 600 and 2.0 kΩ so that a minimum of 0.5 mA current is needed to exceed the threshold voltage. The recommended peak current is 2.0 mA.
37	PD2	Second horizontal phase detector current output. The function of PLL 2 is to adjust the horizontal drive in order to maintain the flyback in phase with the oscillator.
38	Horiz Out	This is a saturated NPN transistor with a 2.0 kΩ internal load to regulate supply V_{CC2}.
39	Horiz Gnd	Horizontal analog output grounding should be connected nearby the external horizontal output stage.
40	V_{CC2}	Regulated supply to horizontal timebase section. A diode is in series with 270 Ω from V_{CC3} + 12 V to block the high voltage start-up supply of 10 mA for horizontal oscillator.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC13020

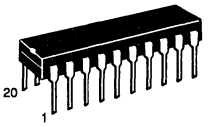
**MOTOROLA C-QUAM®
AM STEREO DECODER**

**SILICON MONOLITHIC
INTEGRATED CIRCUIT**

Motorola C-QUAM®
AM Stereo Decoder

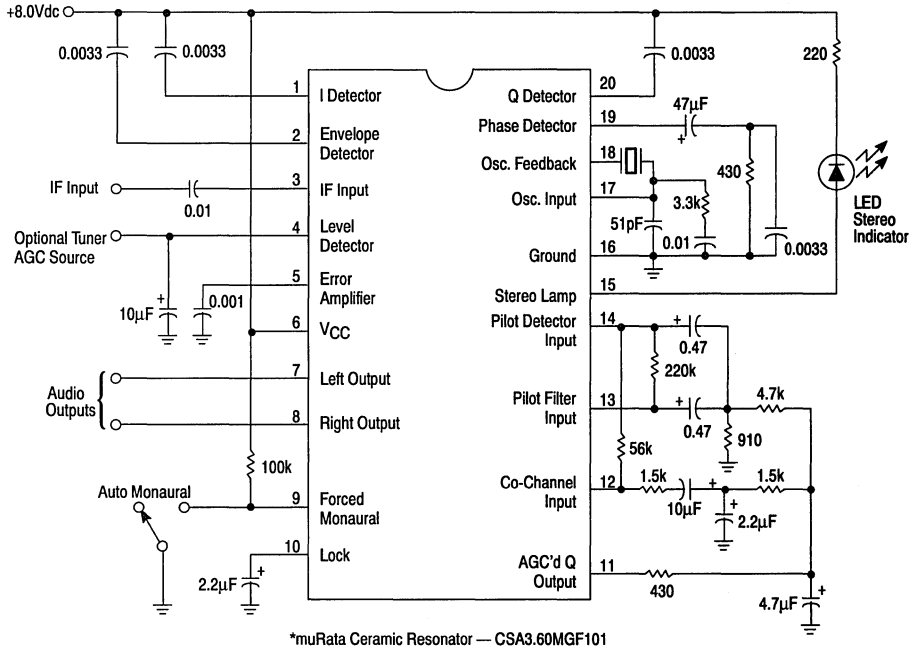
This circuit is a complete one ship, full feature AM stereo decoding and pilot detection system. It employs full-wave envelope signal detection at all times for the L + R signal, and decodes L – R signals only in the presence of valid stereo transmission.

- No Adjustments, No Coils
- Few Peripheral Components
- True Full-Wave Envelope Detection for L + R
- PLL Detection for L – R
- 25 Hz Pilot Presence Required to Receive L – R
- Pilot Acquisition Time 300 ms for Strong Signals, Time Extended for Noise Conditions to Prevent "Falsing"
- Internal Level Detector can be used as AGC Source



P SUFFIX
PLASTIC PACKAGE
CASE 738

Figure 1. Typical Application



*muRata Ceramic Resonator — CSA3.60MGF101

The purchase of the Motorola C-QUAM® AM Stereo Decoder does not carry with such purchase any license by implication, estoppel or otherwise, under any patent rights of Motorola or others covering any combination of this decoder with other elements including use in a radio receiver. Upon application by an interested party, licenses are available from Motorola on its patents applicable to AM Stereo radio receivers.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	14	Vdc
Pilot Lamp Current, Pin 15		50	mAdc
Operating Temperature	T_A	–40 to +85	°C
Storage Temperature	T_{stg}	–65 to +150	°C
Junction Temperature	$T_{J(max)}$	150	°C
Power Dissipation Derate above 25°C	P_D	1.25 10	W mW/°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 8.0 Vdc, T_A = 25°C, Input Signal = 200 mVrms. Unmodulated carrier, circuit of Figure 1, unless otherwise noted.)

Characteristics		Min	Typ	Max	Unit
Supply Line Current Drain, Pin 6		20	30	40	mAdc
Input Signal Level, Unmodulated, Pin 3, for Full Operation		112	200	357	mVrms
Audio Output Level, 50% Modulation	L only or R only Monaural	160 80	220 110	280 140	mVrms
Channel Balance, 50% Modulation, Monaural		—	—	±1.0	dB
Output THD, 50% Modulation Output THD, 90% Modulation	Monaural Stereo Monaural	— — —	— — —	0.5 1.0 1.0	%
Channel Separation, L only or R only, 50% Modulation		23	30	—	dB
Input Impedance	R_{in} C_{in}	20 —	27 6.0	— —	kΩ pF
Output Impedance		—	100	150	Ω
Pilot Acquisition Time VCO locked (after release of forced monaural) Bad Signal Condition		 — 1.48	 280 —	 300 —	 ms sec
Lock Detector Filter Voltage, Pin 10	In Lock Out of Lock	7.7 —	8.0 0.8	— 1.0	Vdc
Force to Monaural, Pin 9 Pull-Down for Monaural Mode Pull-Up for Automatic Mode		 2.0 — — —	 2.5 0.15 3.5 <0.001	 — 1.0 3.7 1.0	 Vdc µA Vdc µA

9

Figure 2. Basic Quadrature AM (QUAM)

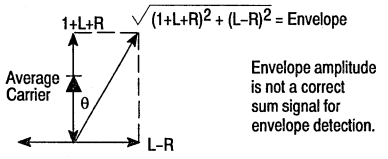


Figure 3. Motorola C-QUAM®

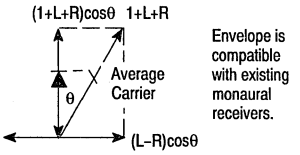
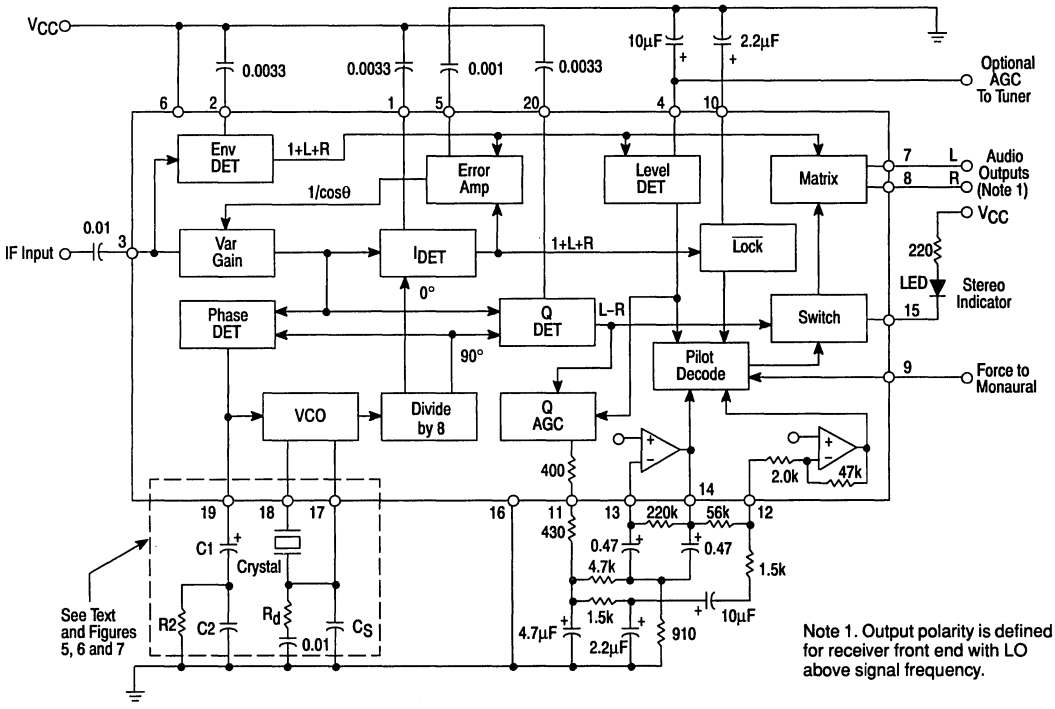


Figure 4. Block Diagram



Note 1. Output polarity is defined for receiver front end with LO above signal frequency.

MOTOROLA C-QUAM® — COMPATIBLE QUADRATURE AM STEREO

Introduction

In C-QUAM®, conventional quadrature amplitude modulation has been modified by multiplying each axis by cosθ as shown in Figures 2 and 3. The resulting carrier envelope is 1 + L + R, i.e., a correct sum signal for monaural receivers and for stereo receivers operating in monaural mode. A 25 Hz pilot signal is added to the L – R information at a 4% modulation level.

Decoder

The MC13020P takes the output of the AM IF amplifier and performs the complete C-QUAM® decoding function. In the absence of a good stereo signal, it produces an undegraded monaural output. Note in Figure 4 that the L + R information delivered to the output always comes from the envelope detector (Env DET).

The MC13020P decodes the stereo information by first converting the C-QUAM® signal to QUAM, and then detecting QUAM. The conversion is accomplished by comparing the output of the Env DET and the I DET in the Err AMP. This provides 1/cosθ correction factor, which is then multiplied by the C-QUAM® incoming signal in the Var Gain block. Thus, the output of the Var Gain block is a QUAM signal, which can then be synchronously detected by conventional means. The I and Q detectors are held at 0° and 90° relative demodulation angles by reference signals from the phase-locked, divided-down VCO. The output of the I DET is 1 + L + R, with the added benefit (over the Env DET) of being able to produce a negative output on strong co-channel or noise interference. This is used to tell the Lock circuit to go to monaural operation. The output of the Q DET is the L – R and pilot information.

VCO

The VCO operates at 8 times the IF input frequency, which ensures that it is out-of-band, even when a 260 kHz IF frequency is used. Typically, a 450 kHz IF frequency is used with synthesized front ends. This places the VCO at 3.6 MHz, which permits economic crystal and ceramic resonators. A crystal VCO is very stable, but cannot be pulled very far to follow front-end mis-tuning. Pull-in capability of ±100 Hz at 450 kHz is typical, and de-Q-ing with a resistor (see Figure 7) can increase the range only slightly. Therefore, the crystal approach can only be used with very accurate, stable front-ends. By comparison, ceramic and L – C VCO circuits offer pull-in range in the order of ±2.5 kHz (at 450 kHz). Ceramic devices accurate enough to avoid trimming adjustment can be obtained with a matched capacitor for Cs (see Figure 1 and 5).

In the PLL filter circuit on Pin 19, C1 is the primary factor in setting a loop corner frequency of 8.0 to 10 Hz, in-lock. An internally controlled fast pull-in is provided. R2 is selected to slightly overdamp the control loop, and C2 prevents high frequency instability.

The Level DET block senses carrier level and provides an optional tuner AGC source. It also operates on the Q AGC block to provide a constant amplitude of 25 Hz pilot at Pin 11, and it delivers information to the pilot decoder regarding signal strength.

Pilot and Co-Channel Filters

The Q AGC output drives a low pass filter, made up of 400 Ω internal and 430 Ω and 5 μF external. From this point, an active 25 Hz band-pass filter is coupled to the Pilot Decoder, Pin 14, and another low-pass filter is connected to the Co-channel Input, Pin 12. A 2:1 reduction of 25 Hz pilot level to the Pilot Decode circuit will cause the system to go monaural, with the components shown. Refer to Figure 8 for the formulas governing the active band-pass filter. The co-channel input signal contains any low frequency intercarrier beat notes, and, at the selected level, prevents the Pilot Decode circuit from going into stereo. The co-channel input, Pin 12, gain can be adjusted by changing the external 1.5 k resistor. The values shown set the "trip" level at about 7% modulation. The 25 Hz pilot signal at the output of the active filter is opposite in phase to the pilot signal coming from the second low-pass filter. The 56 k resistor from Pin 14 to Pin 12 causes the pilot to be cancelled at the co-channel input. This allows a more sensitive setting of the co-channel trip level.

Pilot Decoder

The Pilot Decoder has two modes of operation. When signal conditions are good, the decoder will switch to stereo after 7 consecutive cycles of the 25 Hz pilot tone. When signal conditions are bad, the detected interference changes the pilot counter so as to require 37 consecutive cycles of pilot to go to stereo. In a frequency synthesized radio. the logic that mutes the audio when tuning can be connected to Pin 9. When this pin is held low it holds the decoder in monaural mode and switches it to the short count. This pin should be held low until the synthesizer and decoder have both locked onto a new station. A 300 ms delay should be sufficient. If the synthesizer logic does not provide sufficient delay, the circuit shown in Figure 9 may be added. Once Pin 9 goes high, the Pilot Decoder starts counting. If no pilot is detected for seven consecutive counts, it is assumed to be a good monaural station and the decoder is switched to the long count. This reduces the possibility of false stereo triggering due to signal level fluctuation or noise. If the PLL goes out of lock, or interference is detected by the co-channel protection circuit before seven cycles are counted, the decoder goes into the long count mode. Each disturbance will reset the counter to zero. The Level Detector will keep the decoder from going into stereo if the IF input level drops 10 dB, but will not change the operation of the pilot counter.

Once the decoder has gone into the stereo mode, it will go instantly back to monaural if either the lock detector on Pin 10 goes low, or if the carrier level drops below the present threshold. Seven consecutive counts of no pilot will also put the decoder in monaural. In stereo, the co-channel input is disabled, and co-channel or other noise is detected by negative excursions of the I DET, as mentioned earlier. When these excursions reach a level caused by approximately 20% modulation of co-channel, the lock detector puts the system in monaural, even though the PLL may still actually be locked. This higher level of co-channel tolerance provides the hysteresis to prevent chattering in and out of stereo on a marginal signal.

When all inputs to the Pilot Decode block are correct, and it has completed its count, it turns on the Switch, sending the L – R to the Matrix, and switches the pilot lamp pin to a low impedance to ground.

Summary

It should be noted that in C-QUAM®, with both channels AM modulated, the noise increase in stereo is a maximum of 3.0 dB, less on program material. Therefore, this is not the major concern in the choice of monaural to stereo switching point as it was in FM, and blend is not needed.

PIN FUNCTION DESCRIPTION

Pin No.	Description
1, 2	Detector Filters, R_{out} = 4.3 k, recommend 0.0033 μF to V_{CC} to filter 450 kHz components.
3	IF Signal Input
4	Level Detector filter pin, R_{out} = 8.2 k, 10 μF to ground sets the AGC time constant. High impedance output, needs buffer.
5	Error Amp compensation to stabilize the Var Gain feedback loop
6	V_{CC}, 6.0 to 10 Vdc, suitable for low V_{bat} automotive operation, but must be protected from "high line" condition.
7, 8	Left and Right Outputs, NPN emitter-followers
9	Forced Monaural, MOS or TTL controllable
10	Lock detector filter, R_{out} = 27 k, recommend 2.2 μF to ground
11	AGC'd Q output, NPN emitter-follower with 400 Ω from emitter to Pin 11
12	Co-channel input, 2.0 k series in and 47 k feedback
13	Pilot Filter input to op amp, see Figure 8.
14	Pilot Decode Input (op amp output) emitter-follower, R_{out} = 100 Ω
15	Stereo Lamp, open-collector of an NPN common emitter stage, can sink 50 mA, V_{sat} = 0.3 V at 5.0 mA.
16	Ground
17	Oscillator input, R_{in} = 10k, do not DC connect to Pin 18 or ground.
18	Oscillator feedback, NPN emitter, R_{out} = 100 Ω
19	Phase Detector output, current source to filter.
20	Detector Filter, R_{out} = 4.3 k, recommend 0.0033 μF to V_{CC} to filter 450 kHz.

Figure 5. Ceramic VCO

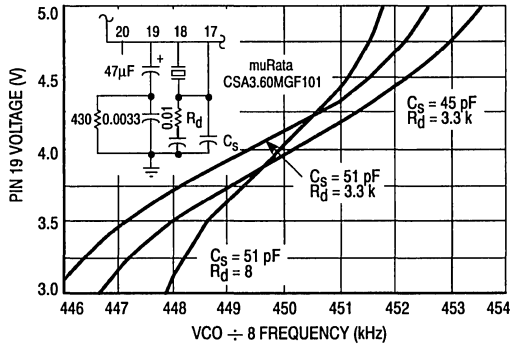


Figure 6. L–C VCO

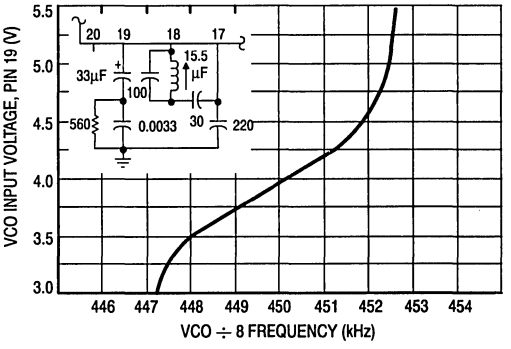


Figure 7. Crystal VCO

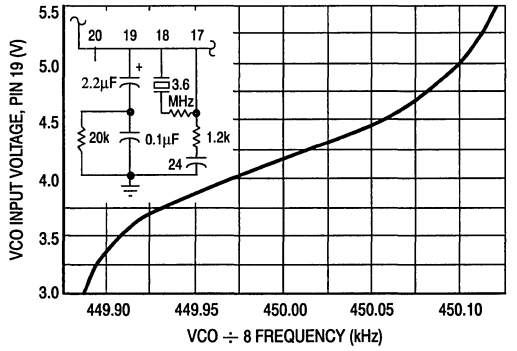


Figure 8. Forced Monaural Optional Delay Circuit

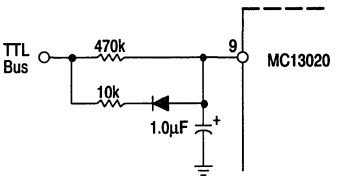
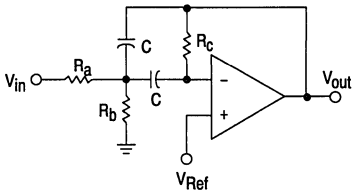


Figure 9. Active Bandpass Filter



$$R_c = \frac{Q}{\pi f_O C}$$

$$R_a = \frac{R_c}{2 A_o}$$

$$R_b = \frac{R_a R_c}{4Q^2 R_a - R_c}$$

C ± 5%	R_a ± 5%	R_b ± 1%	R_c ± 1%
0.47 µF	4.7 k	910	220 k
0.33 µF	8.2 k	1.3 k	330 k

Note: Capacitor C should be a good grade, low ESR.

Where in this application: f_O = center frequency = 25 Hz
A_o = gain at $f_O \leq 25$
$Q \leq 10$

Choose values for f_O, A_o, Q, and conveinent C, solve for resistors.

MC13022

Advance Information

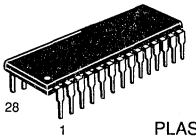
Advanced, Medium Voltage AM Stereo Decoder

C-QUAM®
ADVANCED, MEDIUM VOLTAGE AM STEREO DECODER

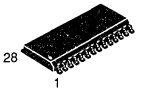
SILICON MONOLITHIC INTEGRATED CIRCUIT

The MC13022 is designed for home, portable, and automotive AM stereo radio applications. The circuits and functions included in the design allow implementation of a full-featured C-QUAM® AM stereo radio with relatively few, inexpensive external parts. It is available in either 28-lead DIP or EIAJ compatible wide-bodied 28-lead SOIC.

- Operation from 4.0 V to 10 V Supply with Current Drain of 18 mA Typ
- IF Amplifier with Two Speed AGC
- Post Detection Filters with 10 kHz Notch that Allow User or Automatic Adjustable Audio Bandwidth Control
- Signal Quality Controlled Stereo Blend and Noise Reduction
- Noise and Co-Channel Discriminating Stop-On-Station
- Signal Strength Indicator Output for RF AGC and/or Meter Drive
- Signal Strength Controlled IF Bandwidth
- Noise Immune Pilot Detector Needs no Precision Filter Components
- MC13023 Complementary Tuning System IC



P SUFFIX
PLASTIC PACKAGE
CASE 710



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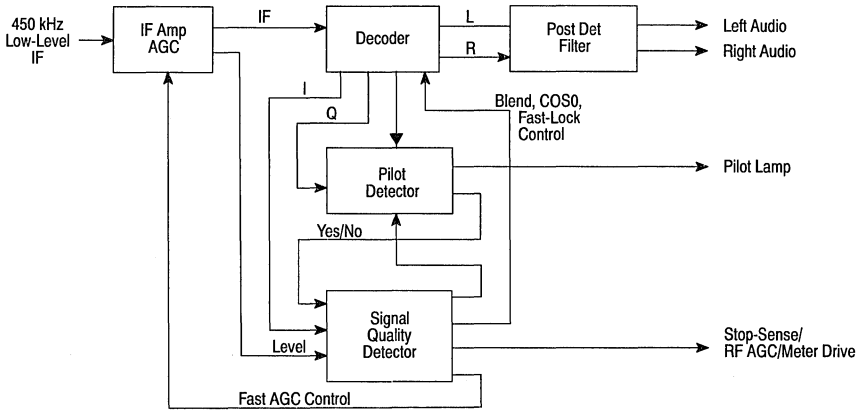
CASE 751F
(SO-28L)

9

Figure 1. Basic Elements of the System



The purchase of the Motorola C-QUAM® AM Stereo Decoder does not carry with such purchase any license by implication, estoppel or otherwise, under any patent rights of Motorola or others covering any combination of this decoder with other elements including use in a radio receiver. Upon application by an interested party, licenses are available from Motorola on its patents applicable to AM Stereo radio receivers.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	12	Vdc
Stereo Indicator Lamp Current, Pin 21		30	mAdc
Operating Temperature	T_A	–40 to +85	°C
Storage Temperature	T_{stg}	–65 to +150	°C
Junction Temperature	$T_{J(max)}$	150	°C
Power Dissipation Derate above 25°C	P_D	1.25 10	W mW/°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 8.0 V, T_A = 25°C)

Characteristics		Min	Typ	Max	Unit
Power Supply Operating Range		4.0	8.0	10	Vdc
Supply Line Current Drain, Pin 25		11	16	22	mAdc
Minimum Input Signal Level, Unmodulated, Pin 5, for Full Operation		—	5.0	—	mVrms
Audio Output Level, 50% Modulation, L only or R only	Stereo	100	140	180	mVrms
Audio Output Level, 50% Modulation	Monaural	50	70	90	mVrms
Output THD, 50% Modulation	Monaural Stereo	— —	0.3 0.5	0.5 2.0	%
Channel Separation, L only or R only, 50% Modulation	Stereo	22	35	—	dB
Pilot Acquisition Time Following BLEND Reset to 0.3 Vdc		—	—	600	ms
Audio Output Impedance at 1.0 kHz, Pin 7, 14		—	300	—	Ω
Stereo Indicator Lamp Pin Saturation Voltage at 3.0 mA Load Current — V_{sat} Pin 21		—	—	200	mVdc
Stereo Indicator Lamp Pin Leakage Current Pin 21		—	—	1.0	µAdc
Notch Filter Control Pin 15 Response versus Voltage		(See Figure 3)			

EXPLANATION OF FEATURES

Blend and Noise Reduction

Although AM stereo does not have the extreme difference in S/N between mono and stereo that FM does (typically less than 3.0 dB versus greater than 20 dB for FM), sudden switching between mono and stereo is quite apparent. Some forms of interference such as co-channel have a large L – R component that makes them more annoying than would ordinarily be expected for the measured level. The MC13022 measures the interference level and reduces L – R as interference increases, blending smoothly to mono. The pilot indicator remains on as long as a pilot signal is detected, even when interference is severe, to minimize annoying pilot light flickering.

RF AGC/Meter Drive

A DC voltage proportional to be log of signal strength is provided at Pin 6. This can be used for RF AGC, signal strength indication, and/or control of the post detection filter. Normal operation is above 2.2 V as shown is Figure 4.

Stop Sense

Multiplexed with the signal strength information is the stop sense signal. The stop sense is activated when scanning by externally pulling the blend capacitor on Pin 23 below 0.5 V. This would typically be done from the mute line in a frequency synthesizer.

If at any time Pin 23 is low and there is either no signal in the IF or a noisy signal of a predetermined interference level, Pin 6 will go low. This low can be used to tell the frequency synthesizer to immediately scan to the next channel. The interference detection prevents stopping on many unlistenable stations, a feature particularly useful at night when many frequencies may have strong signals from multiple co-channel stations.

IF Bandwidth Control

IF AGC attenuates the signal by shunting the signal at the IF input. This widens the IF bandwidth by decreasing the loaded Q of the input coupling coil as signal strength increases.

Post Detection Filtering

With weak, noisy signals, high frequency rolloff greatly improves the sound. Conventional tone controls do not attenuate the highs sufficiently to control noise without also significantly affecting the mid-range. Also, notch filters are necessary with any wide-band AM radio to eliminate the 10 kHz whistle from adjacent stations.

By using a twin-T filter with variable feedback to the normally grounded center leg, a variable Q notch filter is formed that provides both the 10 kHz notch and variable high frequency rolloff functions. Typical range of response is shown in Figure 3. Response is controlled by the DC voltage on Pin 15.

Pin 15 could interface with a DC operated tone control such as the TDA1524, or could be tied to Pin 6 for automatic audio bandwidth control as a function of signal strength.

Figure 2. Test Circuit

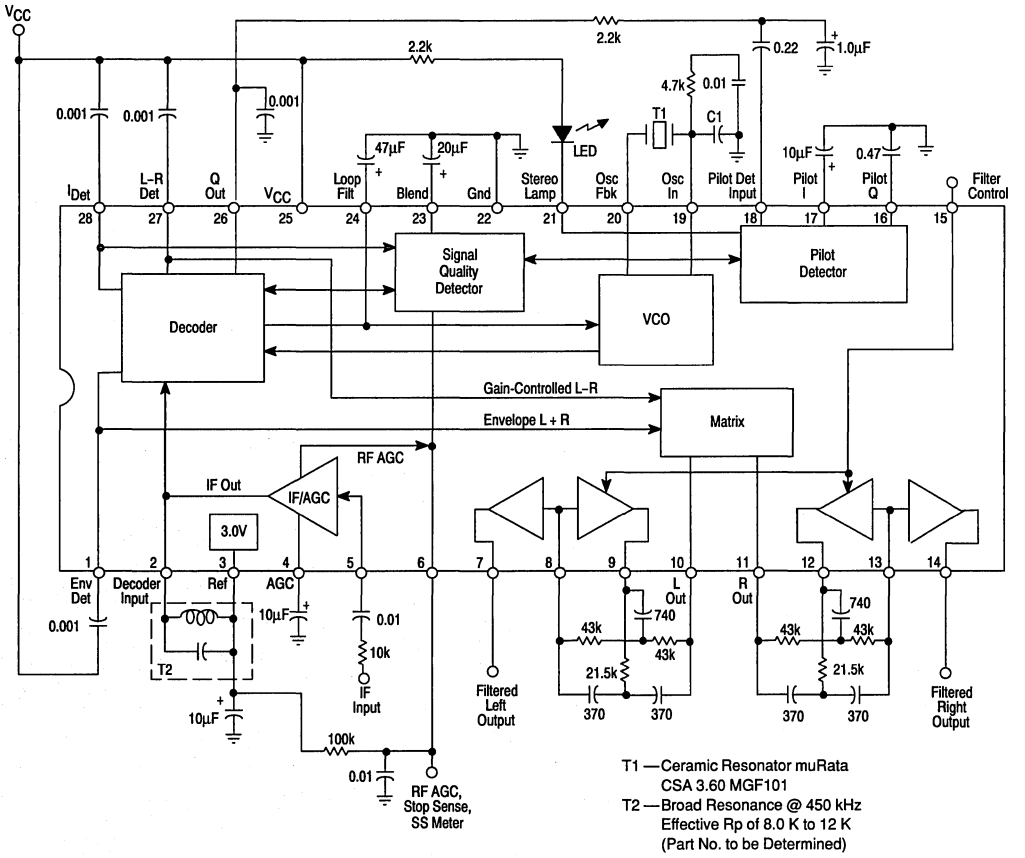


Figure 3. Overall Selectivity of a Typical Receiver versus Filter Control Voltage

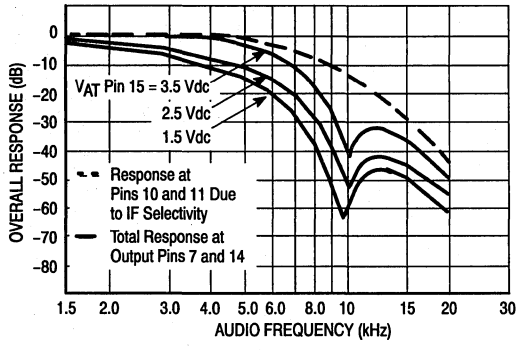


Figure 4. RF AGC/Signal Strength Output versus Input Signal

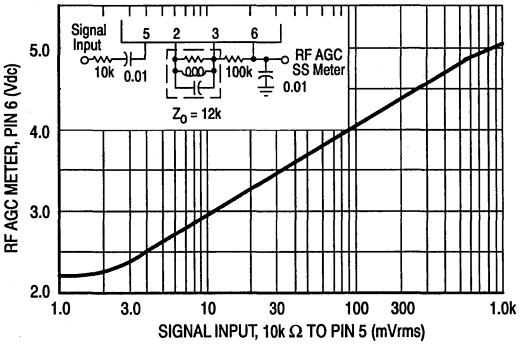
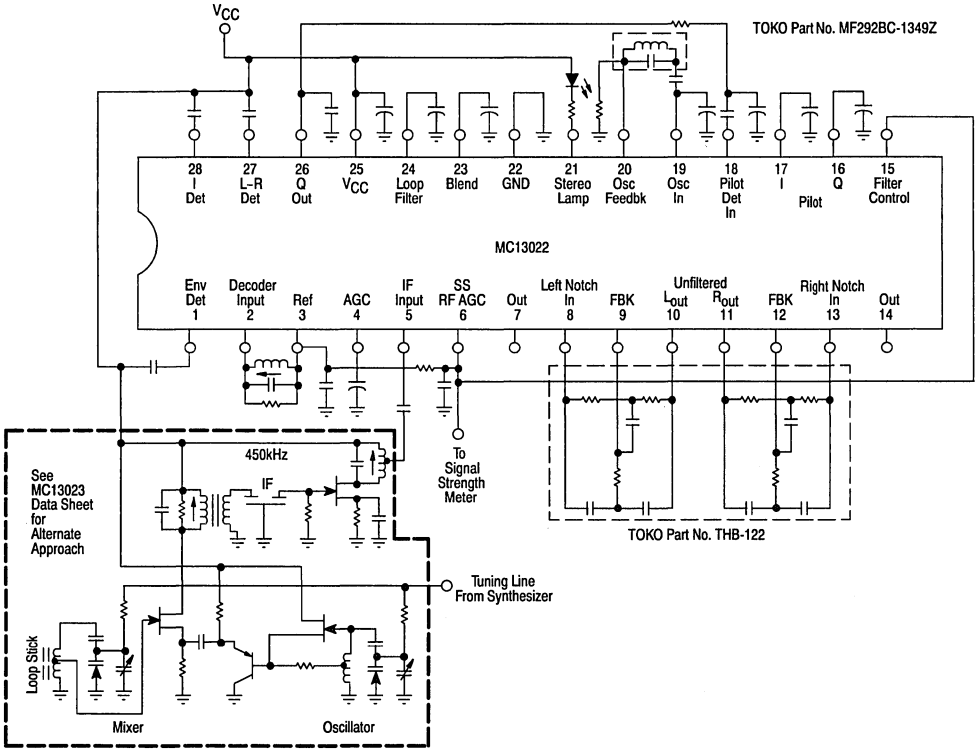


Figure 5. High Performance Home Type AM Stereo Receiver



MC13024

Advance Information

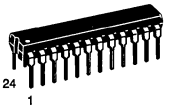
Low Voltage Motorola C-QUAM® AM Stereo Receiver

**LOW VOLTAGE
MOTOROLA C-QUAM®
AM STEREO RECEIVER**

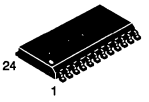
**SILICON MONOLITHIC
INTEGRATED CIRCUIT**

The MC13024 is intended to serve the manually tuned portable and pocket radio mass market. This part includes all receiver and stereo decoding functions, from antenna to Left and Right audio outputs.

- Full Operation from 1.8 V to 8.0 Vdc Supply
- Low Power, Current Drain (typ) 5.0 mA
- Typical Distortion <1% at 90% L + R or 50% Single Channel
- Typical Channel Separation >25 dB
- Pilot Tone Detector
- Combined Two Level Tuning and Stereo Indicator
- "Blend On" Stereo Mode
- High Accuracy, Fast Locking VCLO
- Controlled Return to Monaural Under Adverse Conditions
- Minimized "Tweets and Birdies"
- Minimized Tuning Transients



P SUFFIX
PLASTIC PACKAGE
CASE 724



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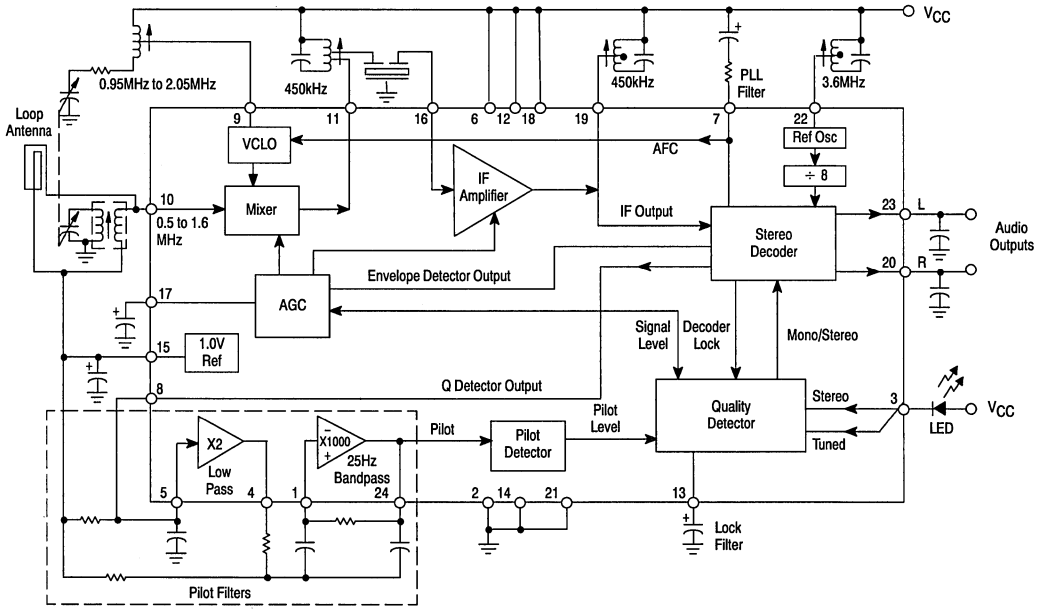
CASE 751E
(SO-24L)

Figure 1. Functional Block Diagram



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	12	Vdc
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	–65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 2.2 Vdc, T_A = 25°C, T_A = Input RF signal = 40 dBμV at 1.0 MHz directly fed to the receiver, Modulating signal = 1.0 kHz sine wave at 30% modulation, unless otherwise noted.)

Characteristics		Min	Typ	Max	Unit
Power Supply Voltage		—	1.8 to 8.0	—	Vdc
Supply Current, Excluding Current LEDs					mA
No Signal		4.0	5.4	6.5	
Monaural		5.0	6.0	6.8	
Stereo		5.0	6.0	6.8	
LED Driving Current				1.8	mA
Monaural		0.8	1.2	5.5	
Stereo		2.5	4.0		
Sensitivity, Monaural					μV
Maximum		—	5.0	—	
20 dB S/N		—	8.0	—	
S/N Ratio	Monaural	30	38	—	dB
	Stereo	28	34	—	
Channel Separation	L to R	17	25	—	dB
	R to L	17	25	—	
Recovered Audio (L or R)		9.0	13	16	mVrms
Stereo Channel Balance		—	–32	—	dB
Distortion	Monaural	—	0.9	1.3	%
	Stereo	—	1.1	2.5	

NOTE: 1. A 200 Hz high-pass filter is required at the recovered audio output to filter out the residual 25 Hz pilot frequency.

GENERAL DESCRIPTION

The MC13024 is a complete C-QUAM® AM stereo receiver, from the antenna to low level audio. All that is needed to make a complete AM stereo radio is the addition of the appropriate audio output amplifier. The MC13024 is intended for use in most types of manually tuned receivers: pocket portables, "boom boxes", table radios, etc. It will operate from 1.8 Vdc to 8.0 Vdc and requires typically 5.0 mA (not including LED). This broad supply voltage tolerance and low power consumption makes it ideal for portables using as few as 2 battery cells. The radios which can be built using this part can be quite low in cost, while still benefiting from a high degree of functional sophistication.

Features

The MC13024 contains a wide dynamic range mixer, IF, AGC, AFC, C-QUAM® decoder, stereo pilot tone detector, and a signal quality detector. The stereo decoding and pilot detection are similar to the well-established MC13020, except for reduced peripheral components, and the phase-locked loop used for the L-R detection now is looped around the entire receiver. In other words, the PLL controls the tuner local oscillator (VCLO) rather than a detector loop after the IF. The advantage of this, in manually tuned AM stereo, is significant, because it assures that the signal will always be properly centered in the IF bandpass, which is critical to good channel separation. this architecture also gives the radio an AFC tuning behavior which makes it easy to tune. The PLL has two speeds, provided by current ratios of 50:1, which give fast lock and low distortion, respectively.

A signal quality detector circuit monitors lock condition, excess in-phase modulation due to interference, pilot presence and amplitude, and the movement of the tuning element by the user. A proper level of pilot must be present for several cycles before stereo mode will be enabled. When all conditions are correct, the transition from monaural to stereo is done gradually to prevent a transient "pop." Under aberrated conditions, the audio may either blend to mono or make an immediate change to mono, depending on the detected condition. The LED pin drives a dual purpose indicator: low current for PLL lock, and full current for stereo mode. Again, the switching is done "softly" to prevent transient loading of a weak battery.

The IF gain and the mixer RF gain are each reduced, in turn, as signal strength increases, to optimize S/N and prevent overload. The receiver is capable of 20 dB S/N at 2.5 μV/50 Ω input. At weak signals, the reference oscillator and quadrature divider are shut off to minimize "tweets and birdies."

Radio Construction

Layout is not much more critical than any high performance AM receiver. Care must be taken to provide a good ground plane and short leads on signal paths. Take special care to keep the reference oscillator components close to Pin 22 and protected from coupling from the pilot bandpass output, Pin 24. Also take care with the ever present threat of RF radiation from the audio output back into the antenna. This can be controlled by proper component location and good (close) RF bypass on the amplifier V_{CC} and good snubbers on the audio outputs. Keeping in mind that this is a phase-detecting receiver, it is important to mount coils securely and avoid movable wires in tuned circuits. A lot of individual preference will go into each implementation; the components shown here are only intended to provide a good working start.

Figure 2. MC13024 Test Circuit Schematic

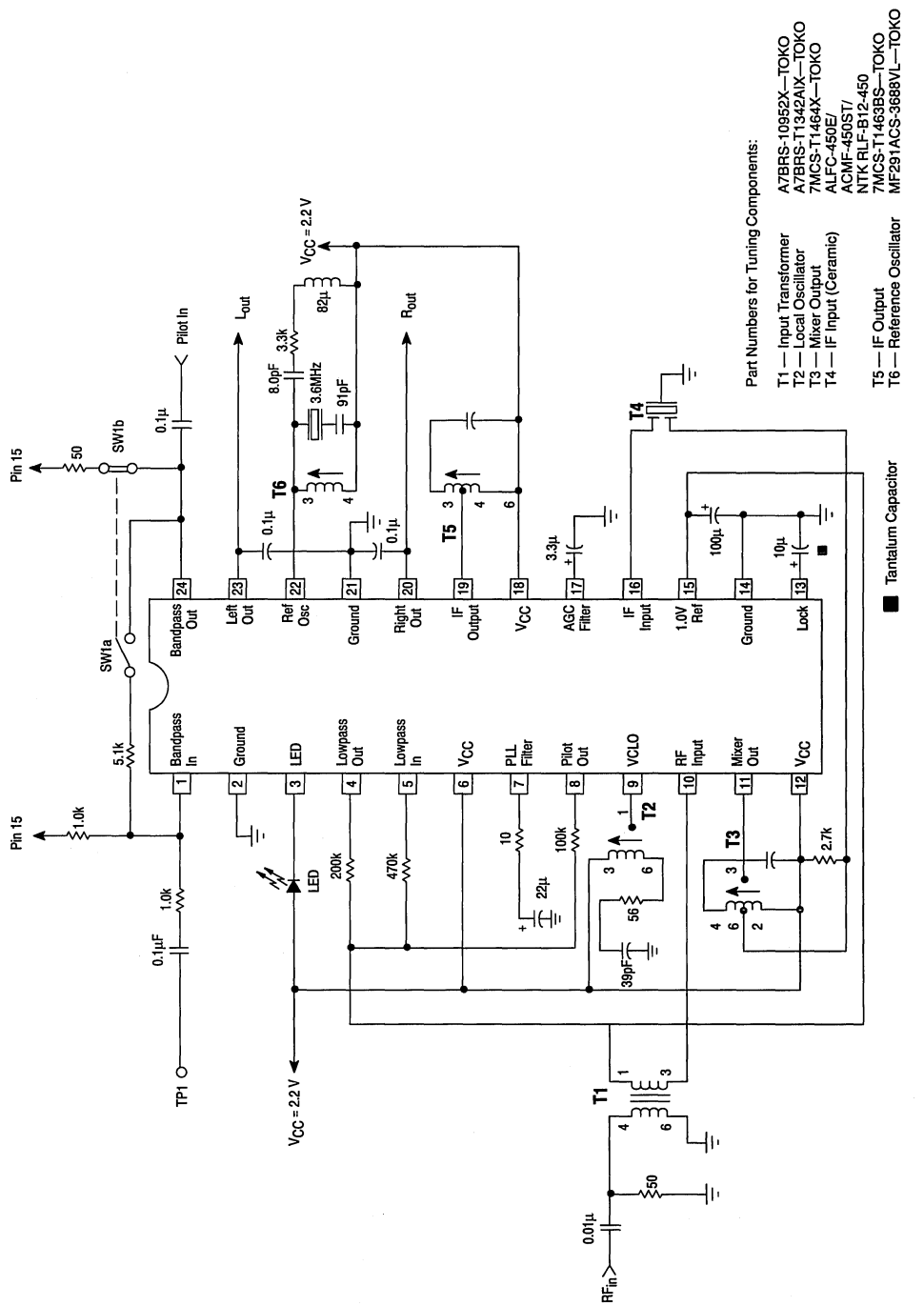
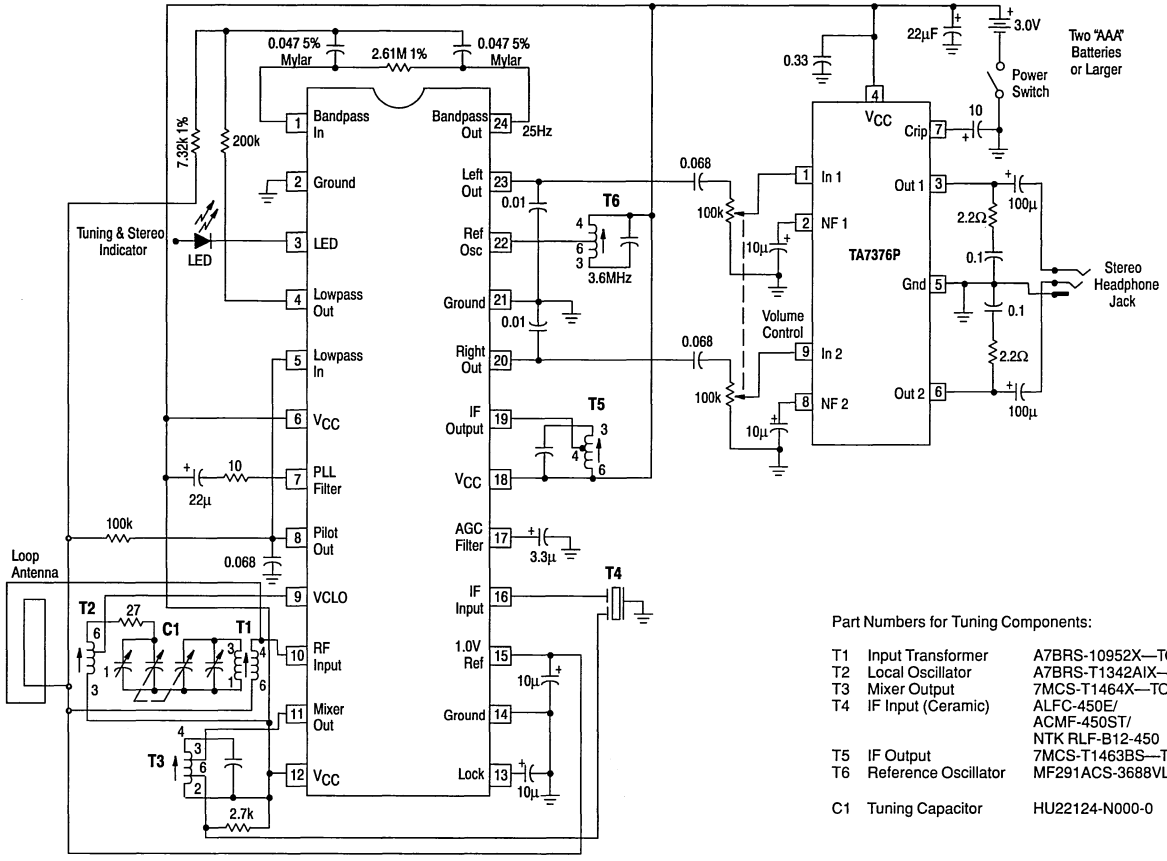


Figure 3. Application Circuit, Manually Tuned Headphone Radio



Part Numbers for Tuning Components:

T1	Input Transformer	A7BRS-10952X—TOKO
T2	Local Oscillator	A7BRS-T1342AIX—TOKO
T3	Mixer Output	7MCS-T1464X—TOKO
T4	IF Input (Ceramic)	ALFC-450E/ ACMF-450ST/ NTK RLF-B12-450
T5	IF Output	7MCS-T1463BS—TOKO
T6	Reference Oscillator	MF291ACS-3688VL—TOKO
C1	Tuning Capacitor	HU22124-N000-0

MC13025

ETR® FRONT END for C-QUAM® AM STEREO

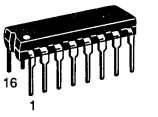
SILICON MONOLITHIC
INTEGRATED CIRCUIT

Product Preview

Electronically Tuned Radio Front End

The MC13025 is the complementary ETR® Electronically Tuned Radio front-end for the second generation MC13022 C-QUAM® AM stereo IF/decoder. The MC13025 provides a high dynamic range mixer, voltage controlled oscillator, and first IF that with the MC13022 and synthesizer form a complete digitally controlled AM stereo tuner system. This system in turn may drive a dual channel audio processor and high power amplifiers for car radio or home stereo applications. Other applications include portable radio "boom boxes", table radios and component stereo systems. The MC13025 is designed to be a simple upgrade or replacement for the older MC13023 Front End/Tuner in ETR applications.

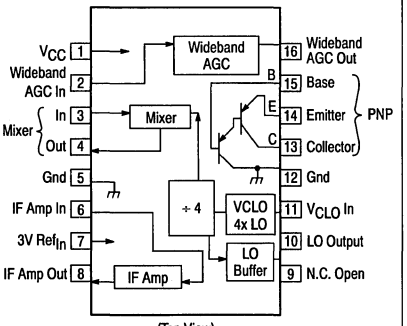
- Replaces the MC13023
- Operates Over a Wide Range of Supply Voltages: 6.0 V_{CC} to 10 V_{CC}
- Wideband AGC Voltage to RF Amp for Extended Dynamic Range
- Buffered VCO Output to Frequency Synthesizer
- No External RF Amp Needed for Most Home Stereo and Portable Radios
- IF Drive Output Matches the MC13022 for Optimum Performance
- VCO Operates at Four Times Local Oscillator Injection Frequency



P SUFFIX
PLASTIC PACKAGE
CASE 648

D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO-16)

PIN CONNECTIONS

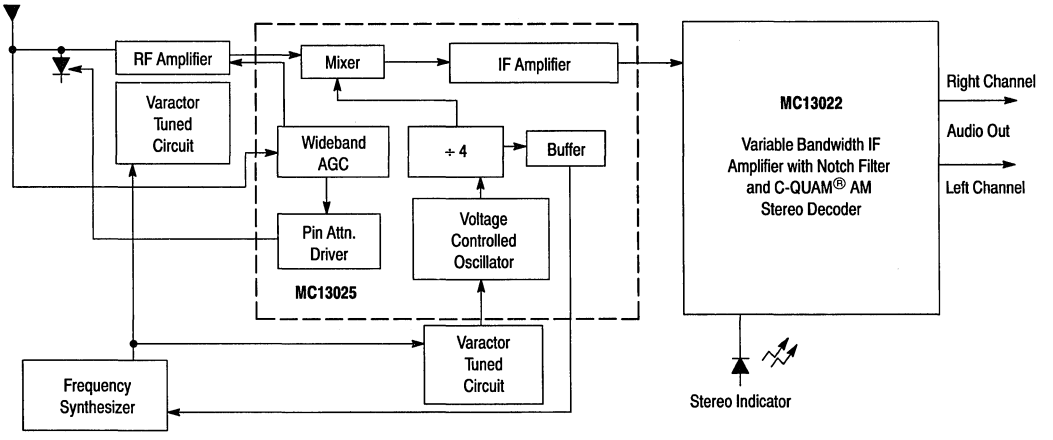


(Top View)

ORDERING INFORMATION

Device	Temperature Range	Package
MC13025P	– 40° to + 85°C	Plastic DIP
MC13025D		SO-16

Simplified Block Diagram



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	4.0 to 10	Vdc
Ambient Operating Temperature	T_A	– 40 to + 85	°C
Storage Temperature	T_{stg}	– 65 to +150	°C
Junction Temperature	T_J	150	°C
Power Dissipation Derate above 25°C	P_D	1.25 10	W mW/°C

ELECTRICAL CHARACTERISTICS (25°C, 8.0 V_{CC} test circuit as shown in Figure 2.)

Characteristics	Pin	Min	Typ	Max	Unit
Supply Current	1	7.0	8.2	10	mAdc
Regulator Current	7	– 50	7.0	90	µAdc
IF Out DC Current	8	0.9	1.05	1.2	mAdc
Mixer DC Current Output	4	0.70	0.77	0.82	mAdc
IF Output Amplitude, RF Input @ 1.7 MHz, 31.6 mV	8	270	317	350	mVrms
Local Oscillator Output	10	160	181	210	mVrms
Wideband AGC Pull-Down Current	16	0.5	1.0	1.5	mAdc
PNP Darlington Collector Current	13	– 5.0	– 4.7	– 4.5	mAdc
PNP Darlington (DC Beta @ 5.0 mA I_E)		1000	2500	5000	
PNP Darlington Collector Leakage	13	– 0.13	– 0.06	—	µAdc

Figure 1. MC13025 Test Circuit

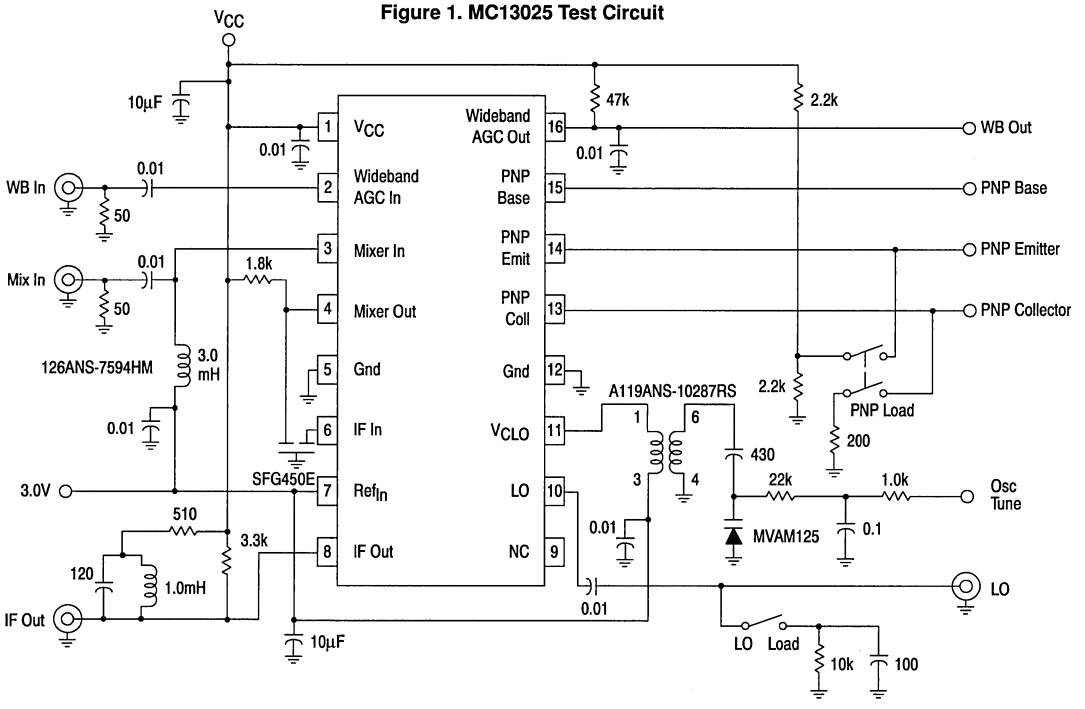


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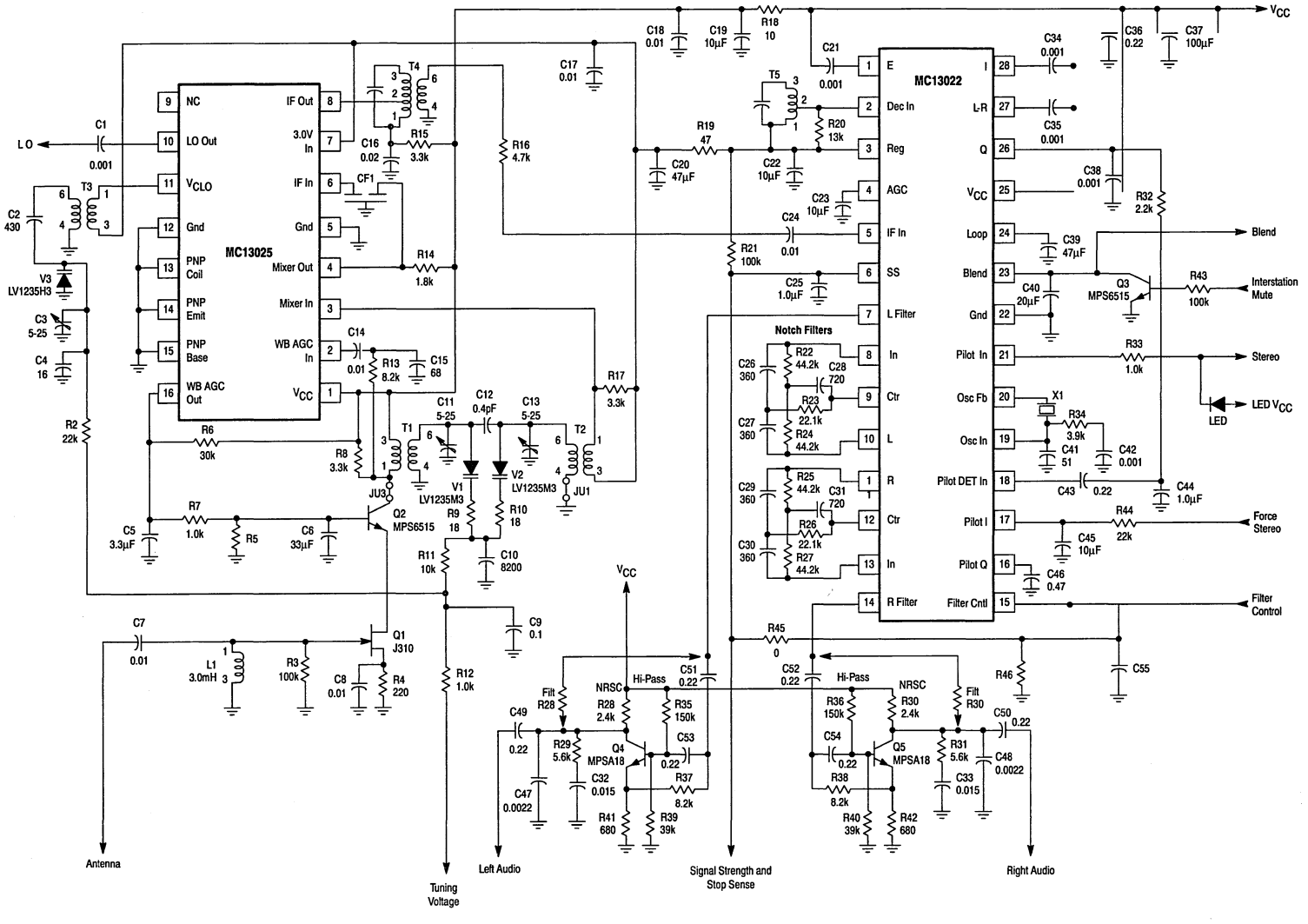
Figure 2. Cascode RF ETR Application
(NRSC — Notch Filters — Optional Pilot High Pass)



MC13060

Mini-Watt Audio Output

This device is a rugged and versatile power amplifier in a remarkable plastic power package.

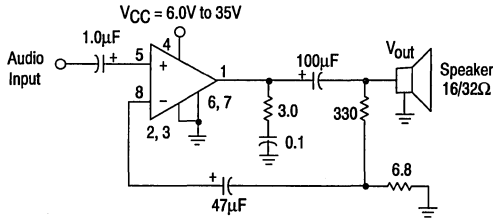
- Supply Voltages from 6.0 Vdc to 35 Vdc
- 2.0 W Output @ 70°C Ambient on PC Board with Good Copper Ground Plane
- Self Protecting Thermal Shutdown
- Easy to Apply, Few Components
- Gain Externally Determined
- Output is Independent of Supply Voltage Over a Wide Range

MINI-WATT AUDIO OUTPUT

SILICON MONOLITHIC INTEGRATED CIRCUIT

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SOP-8)

Figure 1. Typical Application



PIN CONNECTIONS

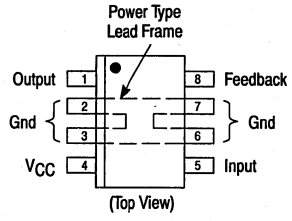
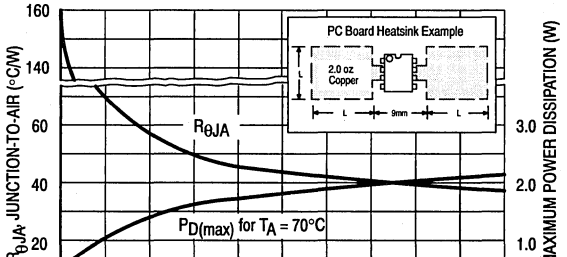


Figure 2. Thermal Resistance & Maximum Power Dissipation versus PC Board Copper



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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	35	V
Audio Input, Pin 5		1.0	V_{p-p}
Thermal Resistance, Junction to Air	$R\theta_{JA}$	160	°C/W
Thermal Resistance, Junction to Case	$R\theta_{JC}$	25	°C/W
Junction Temperature	T_J	150	°C
Operating Ambient Temperature Range	T_A	–40 to +85	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C, circuit of Figure 3, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
AUDIO SECTION					
Power Supply Current, No Signal	I_{CC}	—	13	—	mAdc
Gain	A_o	—	50	—	V/V
Distortion at 62.5 mW Output, 1.0 kHz	THD	—	0.2	1.0	%
Distortion at 900 mW Output, 1.0 kHz	THD	—	0.5	3.0	%
Quiescent Output Voltage, No Signal	$V_{Pin\ 1}$	—	8.4	—	Vdc
Input Bias	V_{Piin5}, $V_{Pin\ 8}$	—	0.7	—	Vdc
Input Resistance	R_{in}, Pin 5	—	28	—	kΩ
Output Noise (50 Hz to 15 kHz) Input 50 Ω	V_{out}	—	0.5	4.0	mVrms

9

GENERAL DESCRIPTION

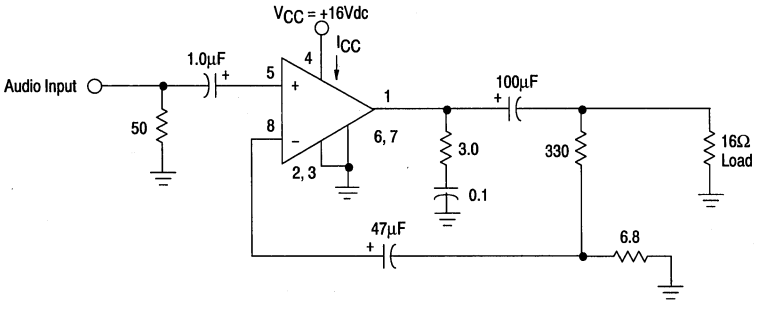
The MC13060 is a quasi-complementary audio power amplifier, mounted in the SOP 8 (power SOIC package). It is well suited to a variety of 1.0 W and 2.0 W applications in radio, TV, intercom, and other speaker driving tasks. It requires the usual external components for high frequency stability and for gain adjustment.

The output signal voltage and the power supply drain current are very linearly related, as shown in Figure 5. Both are quite constant over wide variation of the power supply voltage (above minimum V_{CC} for clipping, of course). The amplifier can best be described as a voltage source with about 1.0 A_{p-p} capability. On a good heatsink, it can deliver over 2.0 W at 70°C ambient.

The MC13060 will automatically go into shutdown at a die temperature of about 150°C, effectively protecting itself, even on fairly stiff power supplies. This eliminates the need for decoupling the power supply, which degrades performance and requires extra components.

Input Pins 5 and 8 are internally biased at 0.7 Vdc and should not be driven below ground.

Figure 3. Test Circuit



All Curves Taken in the Test Circuit of Figure 3, Unless Otherwise Noted.

Figure 4. Quiescent Supply Current and Output Voltage versus Supply Voltage

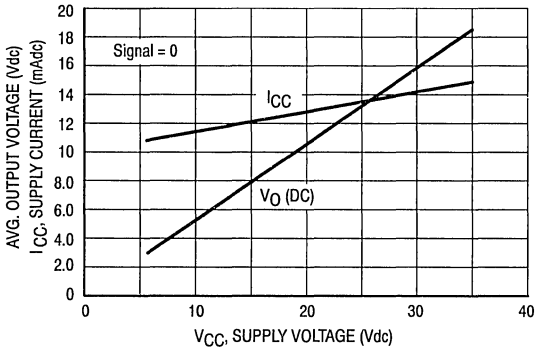


Figure 5. Supply Current versus Output

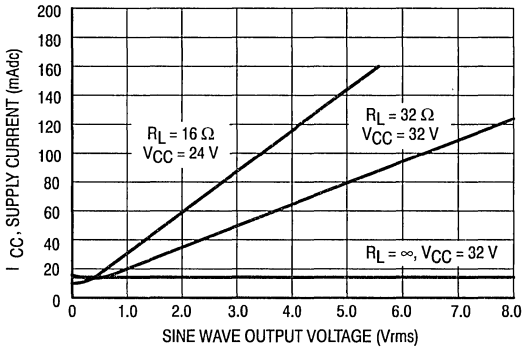


Figure 6. Distortion and Gain versus Frequency

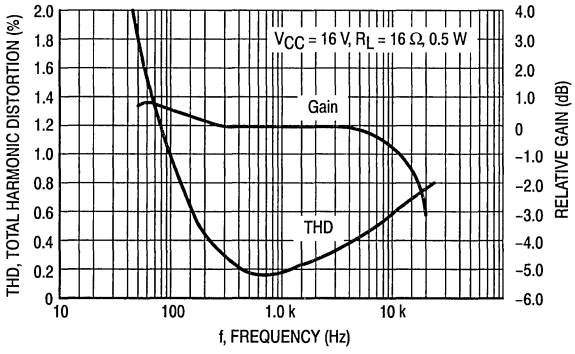


Figure 7. Distortion versus Power Output

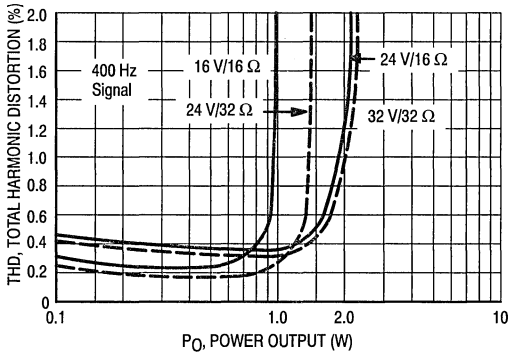


Figure 8. Dissipation versus Output Power

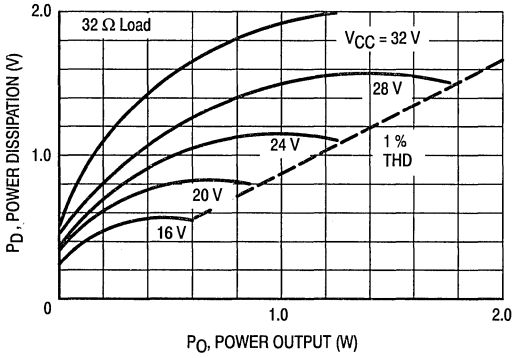


Figure 9. Dissipation versus Output Power

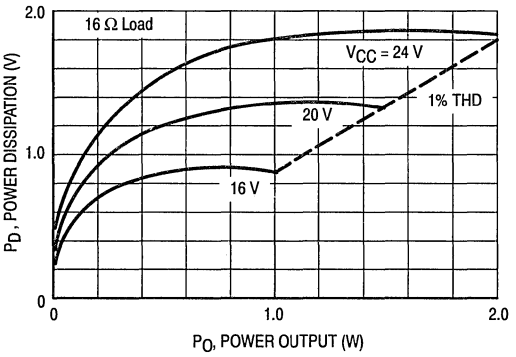


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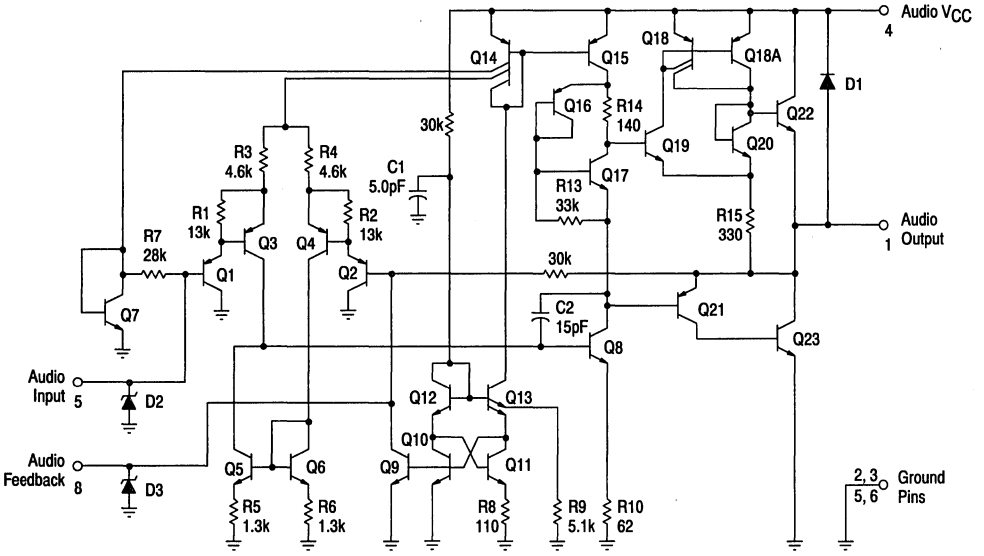
Figure 10. Internal Schematic



9

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC13077

ADVANCED PAL/NTSC ENCODER

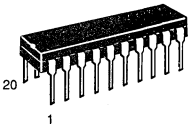
SILICON MONOLITHIC
INTEGRATED CIRCUIT

Advance Information

Advanced PAL/NTSC Encoder

The MC13077 is a high quality RGB/YUV to NTSC/PAL encoder with Composite Video and S-Video outputs. The IC integrates the color difference and luma matrix circuitry, chroma modulators, subcarrier oscillator, and logic circuitry to encode component video into a composite video signal compatible with the NTSC/PAL standards. The IC operates off a standard + 5.0 V supply and typically requires less than 75 mA, making it useful in PC environments. The high degree of integration saves board space and cost, as only passive external components are required for operation. The IC is manufactured using Motorola's MOSAIC™ process and is available in a 20 pin DIP or SOIC package.

- Single 5.0 V Supply
- Composite Output
- S-Video Outputs
- PAL/NTSC Switchable
- PAL Squarewave Output
- PAL Sequence Resettable
- Internal/External Burst Flag
- Digitally Determined Modulator Axes
- Subcarrier Reference Drive Selectable



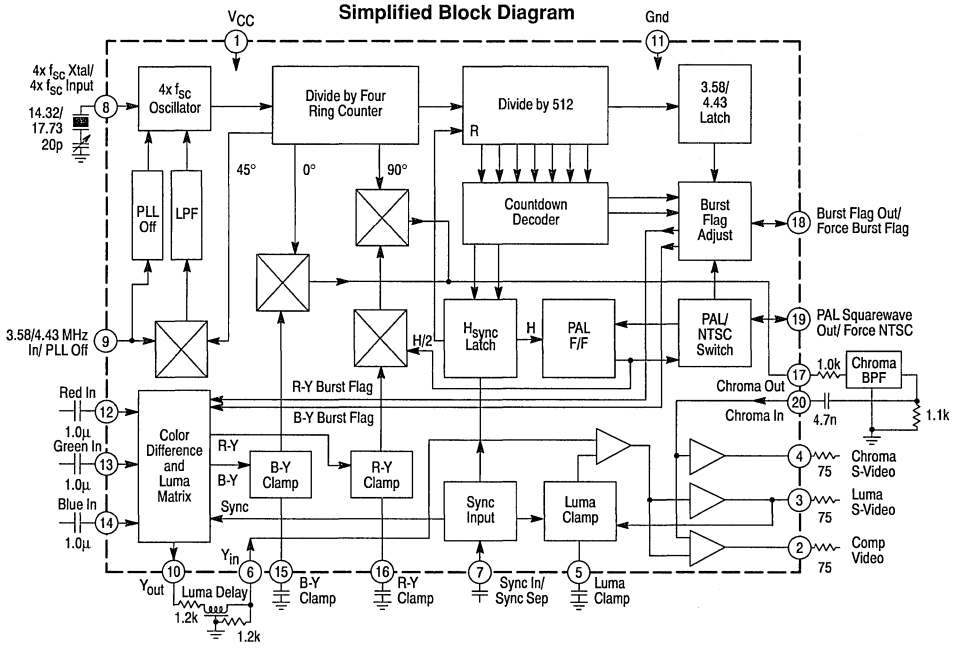
P SUFFIX
PLASTIC PACKAGE
CASE 738

DW SUFFIX
PLASTIC PACKAGE
CASE 751D
(SO-20L)

ORDERING INFORMATION

Device	Temperature Range	Package
MC13077DW	0° to + 70°C	SO-20L
MC13077P		Plastic DIP

Simplified Block Diagram



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	6.0	V
Storage Temperature	T_{stg}	– 65 to +150	°C
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature	T_A	0 to + 70	°C

RECOMMENDED OPERATING CONDITIONS

Characteristics	Min	Typ	Max	Unit
Supply Voltage	4.5	5.0	5.5	Vdc
Sync Input Threshold Equivalent (See Figure 2)	—	1.4	—	Vdc
Pulse Width	—	4.5 – 5.5	—	µs
R, G, B Input (Amplitude for 100% Saturated Video)	—	0.7	—	Vp-p
R-Y Input Amplitude at Pin 16 (for 100% Saturated Video)	—	490	—	mVp-p
B-Y Input Amplitude at Pin 15 (for 100% Saturated Video)	—	350	—	
Y Input Amplitude (without sync) at Pins 12, 13, 14 (for 100% Saturated Video)	—	700	—	
Y Input Amplitude (with sync) at Delay Line	—	1.0	—	Vp-p
External 4x Subcarrier Input to Pin 8 (If crystal is not used)	—	300	—	mVp-p
External Subcarrier Input to Pin 9	—	0.10 to 3.0	—	Vp-p
Lock Range (with 4x Subcarrier Crystal specified) at Subcarrier Frequency	—	± 400	—	Hz
Burst Flag Input Threshold (Pin 18)	—	2.5	—	Vdc
NTSC/PAL Select (Pin 19)				Vdc
PAL Switching Amplitude: High	—	4.0	—	
Low	—	1.1	—	
NTSC Select Threshold	—	0.4	—	

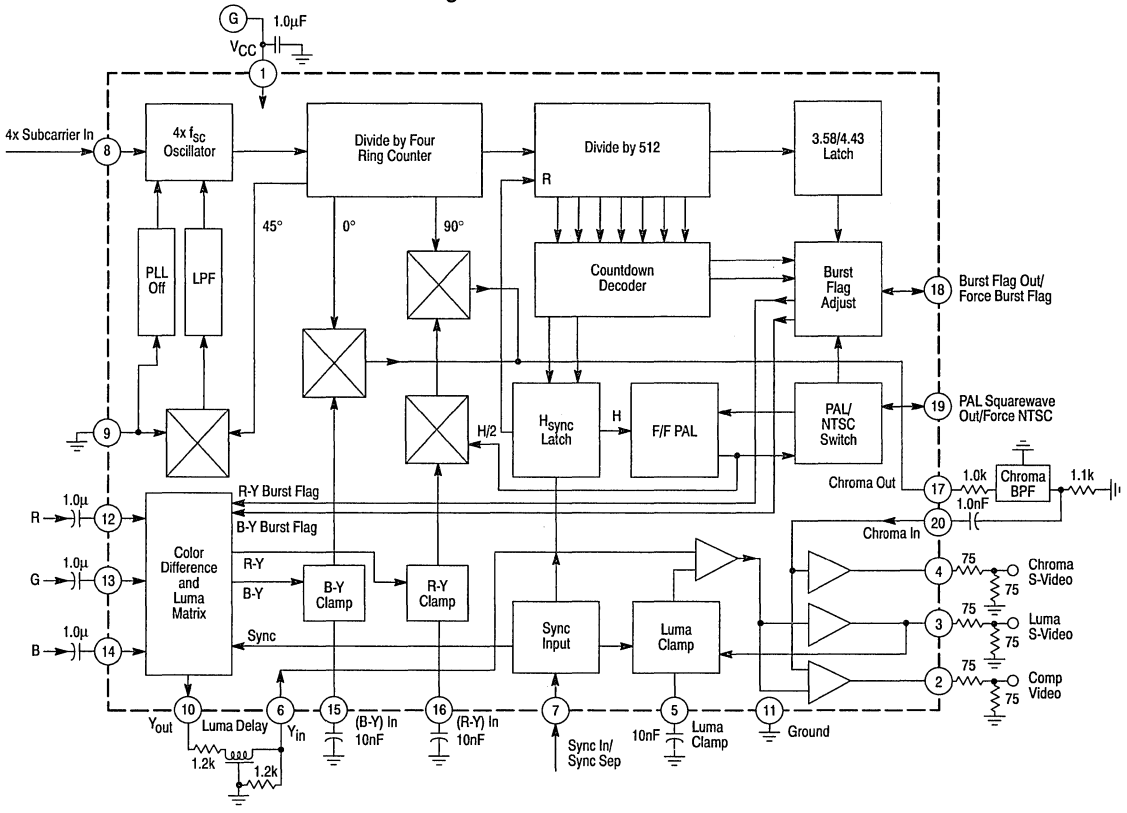
ELECTRICAL CHARACTERISTICS ($0 < T_A < 70°C$, V_{CC} = 5.0 Vdc, test circuit of Figure 1.)

Characteristics	Pin	Min	Typ	Max	Unit
Supply Current (150 Ω Load on Output Pins)	1	55	70	85	mA
Color Burst Amplitude		250	300	350	mVp-p
Line-to-Line Burst Amplitude Deviation		—	7.0	25	mV
Start after leading edge of Sync: NTSC (3.579 MHz)	2 & 4	—	5.0 to 5.3	—	µs
PAL (4.43 MHz)	(@ 75 Ω	—	5.4 to 5.6	—	
Duration: NTSC (3.579 MHz)	load)	—	9	—	Cycles
PAL (4.43 MHz)		—	10	—	
PAL Burst Phase: Line n		125	135	145	Degrees
Line n+1		215	225	235	
NTSC Burst Phase		170	180	190	
Subcarrier Leakage in Black	2 & 4	—	—	25	mV
White (100% white)	(@ 75 Ω load)	—	—	65	
Composite Video Output (100% saturated output)					
Sync Amplitude		240	281	320	mVp-p
Line-to-Line Sync Amplitude Deviation (PAL)		—	7.0	—	mV
Luminance Amplitude Error		—	—	10	%
Line-to-Line Luminance Amplitude Deviation (PAL)	2	—	3.0	—	mVp-p
Chrominance Amplitude Error	(@ 75 Ω	—	—	10	%
Line-to-Line Chroma Amplitude Deviation (PAL)	load)	—	< 14	—	mVp-p
Chrominance Phase Error		—	—	10	Degrees
Line-to-Line Chrominance Phase Error (PAL)		—	< 5.0	—	
Black Level (RGB at Black during Blanking Intervals)		—	500	—	mV
Sync Tip Clamp Level above Ground		120	200	280	

ELECTRICAL CHARACTERISTICS ($0 < T_A < 70°C$, V_{CC} = 5.0 Vdc)

Characteristics	Pin	Min	Typ	Max	Unit
Luma S-Video Output					
Sync Amplitude		240	281	320	mVp-p
Line-to-Line Sync Amplitude Deviation (PAL)	3	—	7.0	—	mV
Luminance Amplitude Error	(@ 75 Ω	—	—	10	%
Line-to-Line Luminance Amplitude Deviation (PAL)	load)	—	3.0	—	mVp-p
Black Level		—	500	—	mV
Sync Tip Clamp Level above Ground		120	200	280	
Chroma S-Video Output					
Chrominance Amplitude Error		—	—	10	%
Line-to-Line Chrominance Amplitude Deviation (PAL)	4	—	< 14	—	mVp-p
Chrominance Phase Error	(@ 75 Ω	—	—	10	Degrees
Black Level	load)	—	500	—	mV

Figure 1. Test Circuit



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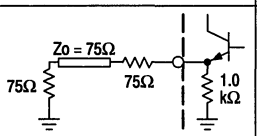
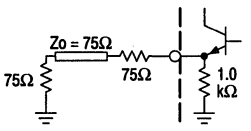
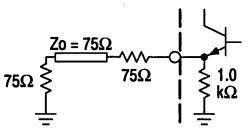
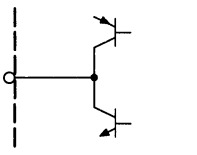
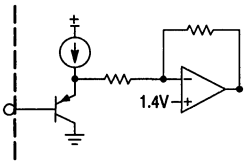
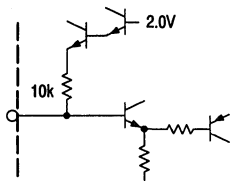
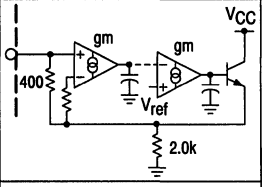
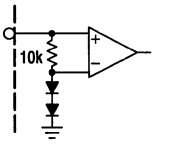
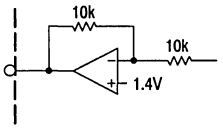
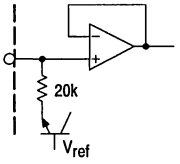
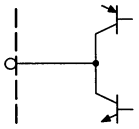
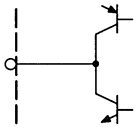
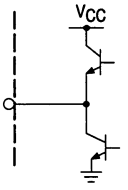
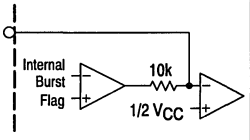
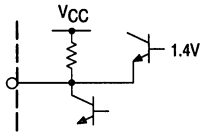
PIN DESCRIPTIONS

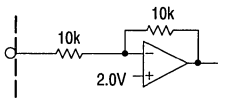
Pin	Symbol	Internal Equivalent Schematic	Description	Expected Waveforms
1	V_{CC}		Supply Voltage	+ 5.0 Vdc ±10%.
2	Comp Video		Composite Video output. The external 75 Ω series resistor determines the impedance of the output. The output will drive a 75 Ω load through a 75 Ω coax.	1.0 Vp-p (75% Color Saturation), 1.23 Vp-p (100% Color Saturation) at the 75 Ω load.
3	Luma S-Video		Luminance S-Video output. The external 75 Ω series resistor determines the impedance of the output. The output will drive a 75 Ω load through a 75 Ω coax.	1.0 Vp-p with sync (100% output) at the 75 Ω load.
4	Chroma S-Video		Chrominance S-Video output. The external 75 Ω series resistor determines the impedance of the output. The output will drive a 75 Ω load through a 75 Ω coax.	885 mVp-p (100% output) when at the 75 Ω load.
5	Luma Clamp		Luminance Output Clamp storage capacitor. A 0.01 µF capacitor should be connected from this pin to ground.	3.4 Vdc.
6	Y_{In}		Luminance input from the delay line. The delayed Luma from Pin 10 is applied at this pin.	500 mVp-p of Composite Luma when 100% saturated RGB inputs are applied.
7	Sync In/ Sync Sep		Composite Sync input. Negative going sync should be applied at this pin. The input has a threshold of 1.4 V.	The peak voltage may not exceed V_{CC}. Minimum voltage should not be less than 0 V. See Figure 2 for input requirements.
8	4x f_{SC} Xtal /4x f_{SC} In		Four times Subcarrier Frequency Crystal Oscillator pin. This pin provides for the connection of the oscillator resonant element. Pin may also be driven directly with a 4x subcarrier signal.	300 Vp-p to 600 Vp-p 4x subcarrier input if the pin is being externally driven. Approximately 40 mVp-p, if a crystal is being used.
9	3.58/ 4.43 MHz In/PLL Off		External Subcarrier Input. This pin provides an input to a Phase Detector and PLL and allows phase-lock of the 4x oscillator to an external subcarrier reference. To disable the PLL, this pin should be grounded. 400 Hz of pull-in and lock-in range is possible with a crystal.	0.10 Vp-p to 3.0 Vp-p (AC coupled) of subcarrier to phase-lock 4x oscillator or grounded to disable the PLL.

9

PIN DESCRIPTIONS

Pin	Symbol	Internal Equivalent Schematic	Description	Expected Waveforms
10	Y_{Out}		Luminance Delay Line Drive Output. A delay should be inserted between this pin and Pin 6 to match the delay incurred by the Chroma.	1.0 Vp-p with sync (100% saturated Color Bar output).
11	Gnd		Ground	Ground
12	Red_{In}		Red Video input.	0.7 Vp-p AC coupled (100% Color Bars).
13	$Green_{In}$	See Pin 12	Green Video input.	0.7 Vp-p AC coupled (100% Color Bars).
14	$Blue_{In}$	See Pin 12	Blue Video input.	0.7 Vp-p AC coupled (100% Color Bars).
15	B-Y Clamp		B-Y Clamp storage capacitor. A 0.01 µF capacitor should be connected from this pin to ground, unless the pin is used as an input.	If not used as an input the pin is clamped during sync to 2.4 Vdc. Can be used as a B-Y input (AC coupled, 350 mVp-p, 100% color saturation). Burst Flag, if disabled at Pin 18, must be inserted here with the following signal levels; –170 mV (NTSC), –121 mV (PAL).
16	R-Y Clamp		R-Y Clamp storage capacitor. A 0.01 µF capacitor should be connected from this pin to ground, unless the pin is used as an input.	If not used as an input the pin is clamped during sync to 2.4 Vdc. Can be used as a R-Y input (AC coupled, 490 mVp-p, 100% color saturation). Burst Flag, if disabled at Pin 18, must be inserted here with the following signal level; +121 mV for PAL.
17	Chroma Out		Chroma Bandpass Drive Output.	2.8 Vp-p (100% Color Bars).
18	Burst Flag Out/Force Burst Flag		Burst Flag Output Disable and Force pin. If left unconnected, internally generated color burst will appear at Pins 2 and 4. Burst Flag will appear at this pin (18). If grounded, the Burst Flag will be disabled. If externally driven from another source of burst flag, the internal flags will be overriden.	1.8 Vp-p burst flag pulses if unconnected.
19	PAL Square-wave Out/Force NTSC		PAL/NTSC system switch. If grounded, the MC13077 will encode NTSC, and if left open, PAL.	In PAL mode, a PAL squarewave appears at this pin, the phase of which can be reset by momentarily forcing the pin to ground during the high state of the squarewave.

PIN DESCRIPTIONS

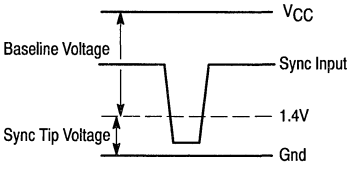
Pin	Symbol	Internal Equivalent Schematic	Description	Expected Waveforms
20	Chroma In		Chroma Bandpass input. Output from chroma bandpass filter should be applied at this pin.	1.4 Vp-p (100% Color Bars) with bandpass filter and 1.0 kΩ matching resistors.

Composite Sync Input

Other than the component video inputs to be encoded, only Composite Sync is required for encoding the components into a composite signal compatible with either the NTSC or PAL standard. The Composite Sync input is used internally for determining which standard to encode to, for driving the black level clamps, and to set the timing of the composite sync in the outputs.

The Composite Sync/Sync Separator input was designed to accept AC or DC coupled inputs making it possible to drive the sync input from a variety of sources. An interesting note is that composite video can also be used for sync input. The threshold of the sync input is 1.4 Vdc. Figure 2 shows the requirements for sync input.

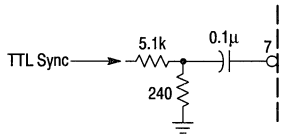
Figure 2. Sync Input Amplitude Requirements



Both serrated and block vertical sync can be used for NTSC applications. PAL applications require a serrated vertical sync. The serrations at the horizontal rate trigger the PAL flip-flop to generate the swinging burst.

Even though the sync input of the MC13077 is well suited for TTL interface, some functions of the IC are susceptible to the high energy present in such signals and may be disturbed. This disturbance may take the form of a noise spike in the video outputs and/or a disturbance of the 4x oscillator resulting in an incorrect encoding of the chroma information. Therefore, it is recommended that if TTL or other fast-edged inputs are going to be used for the sync input, then either the amplitude and/or the edge speed of the sync input pulse should be reduced. 300 mVp-p of sync without a reduction of edge speed has to be shown to produce disturbance free operation. Also, a sync input of 4.0 Vp-p and edge rates of 225 ns have been shown to produce similar results. Figure 3 shows a recommended coupling circuit for TTL type composite sync.

Figure 3. TTL Sync Input Circuit



Luma and Color Difference Clamps

Clamping for the MC13077 occurs once every horizontal line during sync. The absence of color creates a color difference component voltage of zero, this null is used to generate a reference voltage for black in the video outputs. The clamp capacitors at Pins 5, 15 and 16 are used to store the reference voltage during the line period.

RGB Inputs

To encode RGB, the component video inputs (Pins 12, 13, 14) are applied to the Luma (Y) and color difference (R-Y, B-Y) matrix. The color difference signals are then conditioned by Sallen-key low pass filters (f–3 dB = 4.0 MHz). The inputs are designed so that 700 mVp-p RGB provides 100% color saturation.

The first color difference component (R-Y) is created by matrixing the RGB components with the following weights:

$$R\text{-}Y = 0.70R - 0.59G - 0.11B \quad (1)$$

The second color difference signal (B-Y) is created in a similar fashion by the equation:

$$B\text{-}Y = 0.89R - 0.59G - 0.30B \quad (2)$$

These two components then receive burst flag before being modulated by the color subcarrier to create composite chroma.

The luma is also the result of a weighted matrixing of the RGB components. The components and corresponding weights are:

$$Y = 0.30R + 0.59G + 0.11B \quad (3)$$

Composite sync is then added to the result of Equation 3 to create composite luma.

The luma information thus created must be eventually recombined with the chroma information. However, since the chroma information created by Equations 1 and 2 is filtered internally before being modulated then bandlimited externally, the resultant encoded chroma experiences a group delay that is the sum of the delay imposed by the internal and external filtering. So, the composite luma is output at Pin 10 so that an external delay can be inserted in the path to match the delay incurred by the composite chroma. The delayed composite luma is then input back into the MC13077 at Pin 6.

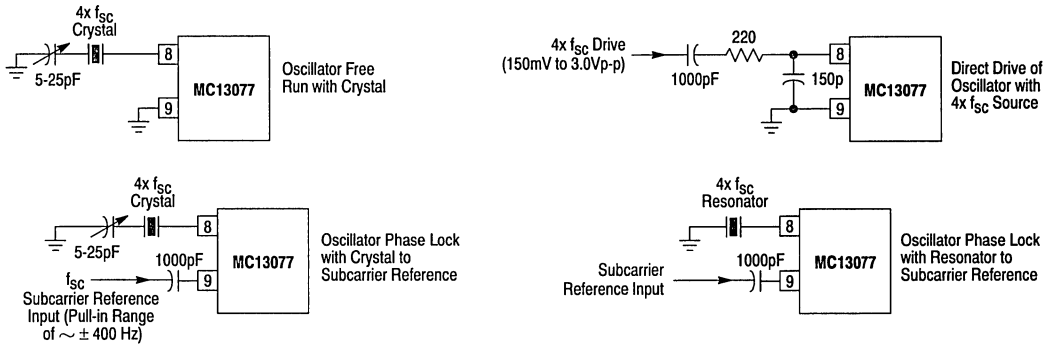
Color Difference Inputs

If the MC13077 is intended to encode color difference signals (YUV or Y, R-Y, B-Y), it becomes necessary to bypass the color difference and luma matrix circuitry. This can be accomplished by inputing directly to the color modulators the color difference signals. 491 mVp-p and 349 mVp-p should be input to the R-Y and B-Y Clamp pins (Pin 16 and Pin 15) respectively, to achieve 100% color saturation in the composite video output. The luma information can be input in

two ways. The luma can be input directly into the RGB inputs (700 mVp-p without sync), or through the delay line (1.0 Vp-p with sync, sync tip-to-peak white) in which case the RGB inputs should be cap-coupled to ground. In either case, composite sync still needs to be input to the MC13077 at Pin 7 (see Figures 11, 12 and 13).

If the R-Y and B-Y inputs also have burst flag, it can also be input along with the color difference signals at these pins. Of course, now since the color difference modulator pre-filtering is circumvented, the delay for the luma information should be matched only to the delay of the bandpass filter.

Figure 4. Versatility of the 4x f_{SC} Oscillator



4X Subcarrier Oscillator

To encode the color difference components, an accurate and reliable subcarrier source is required. The MC13077 has an on-chip single pin oscillator that will free-run with a 4x f_{SC} crystal, phase-lock to an external subcarrier reference with a 4x f_{SC} crystal or resonator, or be driven externally from a 4x f_{SC} source. If the 4x f_{SC} oscillator is going to be free run, the subcarrier input (Pin 9) should be grounded. If the 4x f_{SC} oscillator is going to be phase-locked to an external subcarrier source, the external reference should be capacitor-coupled to Pin 9. If the 4x f_{SC} oscillator is going to be driven externally, Pin 8 should be driven from a network that increases the impedance of the source at frequencies capable of producing off-frequency oscillations. The 4x f_{SC} subcarrier source, thus being defined, makes it possible to produce accurate quadrature subcarriers for the modulators. The 4x source is internally divided by a ring counter to produce the quadrature subcarrier signals. These signals in turn are provided to the color difference modulators to produce the modulated chroma. The oscillator was designed so that if a crystal is chosen as the resonant element of the 4x oscillator, the crystal specifications would be common. Crystal specifications for an adequate crystal are shown in Table 1.

Table 1. Crystal Specifications

Frequency: 14.31818 MHz (NTSC) 17.734475 MHz (PAL)
Mode: Fundamental
Frequency Tolerance (@25°C), 40 ppm
Frequency Tolerance df/dfo (0° – 70°C), 40 ppm
Load Capacitance: 20 pF
ESR: 50 Ω
C1(Internal Series Capacitance), 15 mpF

This crystal is a common variety and is specified as a parallel resonant.

Burst Flag Decoding

In order to encode to either NTSC or PAL compatibility, the MC13077 must first determine which is the intended standard. The MC13077 accomplishes this with an internal decode using the sync input and the output of the divide by 4 ring counter. Internally, the Sync separator circuitry provides an output that is sampled by the subcarrier signal from the ring counter. The result is an internal sync representative of externally input sync but synchronized to the internal subcarrier signal. This signal provides a reset for an internal 9-bit counter that provides divisions of the subcarrier signal from the ring counter at powers of 2 (i.e. $2^1, 2^2, 2^3, ...2^9 = 512$). The eighth bit of the counter gives the output, $f_{SC} \div 256$. The decision to provide burst gate timing for PAL or NTSC is based upon the state of this output after one period of the horizontal sync. Figure 5 shows the relationship between the clock and the eighth bit of the counter.

Triggering of the burst PAL flip-flop due to equalizing pulses is also inhibited by the decode circuitry. This is done by counting out beyond a half line interval before generating burst flag.

If the MC13077 is encoding 525/60 component video to NTSC and the MC13077 is generating the burst flag, the start of burst will occur 18 counts after the leading edge of sync has been sampled, and will continue until nine cycles of burst have occurred. Since the reset pulse of the 9-bit counter has a resolution of $1.0/f_{SC}$, this implies that the start of burst will occur 5.17 ± 0.1397 µs after the leading edge of sync and also that the start (and end) of burst may differ by as much as 279.4 ns from line-to-line. If the MC13077 is encoding 625/50 to PAL, the subcarrier frequency will be 4.43361875 MHz and that implies a resolution of 225.5 ns for the burst position. For PAL encoding, 24 counts of the subcarrier are necessary before burst is initiated. So ten cycles of subcarrier will occur 5.53 ± 0.1128 µs after the leading edge of sync. After the timing of the burst gate is selected, the burst gate envelope is added to the color difference components.

Another alternative to the internal determination of burst flag is the external input of burst flag. This allows the user to externally define the exact timing and duration of color burst. If external burst flag is available, it can be inserted at Pin 18. The threshold level is nominally $V_{CC}/2$ and the input should not exceed V_{CC}. Burst will begin when the leading edge of the burst flag input exceeds $V_{CC}/2$ and will stop when it falls below $V_{CC}/2$. If it is desired to disable the burst flag, Pin 18 can be pulled low. It is also possible to insert burst flag with the R-Y and B-Y components. This is done at the clamp pins with the respective color difference inputs with the internal burst flag generation disabled (Pin 18 grounded).

Chroma Band Limiting and Luma Delay

Once the color difference and burst flag envelopes have been modulated, the two components are internally summed and applied to an output buffer that will drive the external bandpass circuitry before entering the chip again at Pin 20. The sum of the color difference modulators produces an output that is high in harmonic content. For this reason, and to reduce the possibility of cross color, a chroma bandpass transformer is used to band-limit the chroma. Suggested bandpass filters and specifications for NTSC and PAL are shown in Figure 6a and 6b. For each of these filters, approximately 300 ns of group delay is experienced by the filtered chroma. There is also an internal delay on the order of 100 ns due to internal filtering that must be considered. Thus a 400 ns luma delay line is used to equalize the timing of the luma and the chroma. Suitable 400 ns delay lines are the TOKO H321LNP-1436PBAB and the TDK DL122401D-1533. The delay of the luma channel is inserted between Pins 10 and 6. Pin 10 is the buffered output of the luma from the RGB matrix. This output is capable of driving the external passive delay line with no external gain or buffering required.

Figure 6a. Group Delay and Magnitude Response of the TOKO Bandpass Filter Intended for NTSC Applications

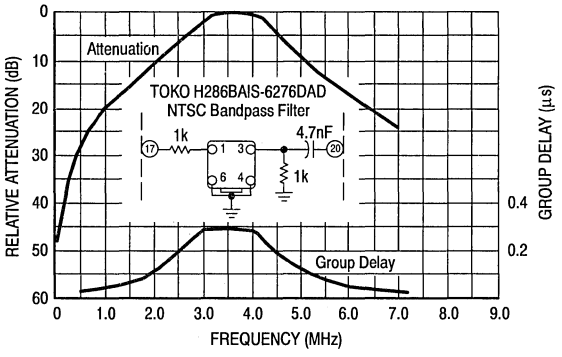
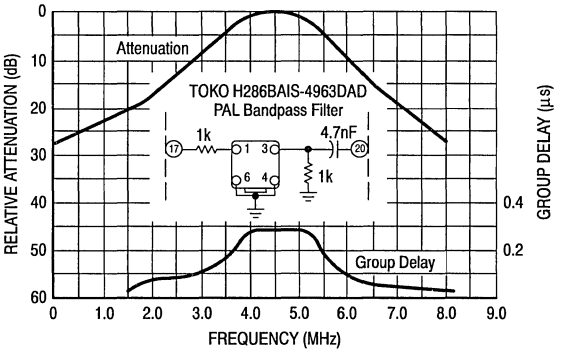


Figure 6b. Group Delay and Magnitude Response of the TOKO Bandpass Filter Intended for PAL Applications



Characteristics of TOKO Bandpass Filter (H286BAIS – 6276DAD)

Frequency (MHz)	**Attenuation** (dB)	**Group Delay** (µs)
2.0	8.0 (min)	0.12
2.8	3.0 ± 3.0	0.25
3.58	Ins. Loss 3.5 (max)	0.290 ± 0.030
4.3	3.0 ± 3.0	0.24
6.2	15 (min)	0.05

Characteristics of TOKO Bandpass Filter (H286BAIS – 4963DAD)

Frequency (MHz)	**Attenuation** (dB)	**Group Delay** (µs)
2.50	10 (min)	0.075
3.73	3.0 ± 3.0	0.24
4.43	Ins Loss 2.0 (max)	0.295 ± 0.035
5.13	3.0 ± 3.0	0.24
6.50	12 (min)	0.05

Chroma Encoding

Modulation of the color difference components is performed by two double-balanced mixers that are driven from quadrature signals provided by an internal ring counter. The quadrature signals are derived from a ring counter that is driven by the 4x oscillator, and which makes highly accurate quadrature angles possible.

If PAL encoding is selected, negative burst flag envelope is provided to both B-Y and R-Y components equally, then the R-Y envelope phase is switched positive and negative from line-to-line to provide the PAL alternating burst phase characteristic. An internal flip-flop that provides the internal $f_H/2$ switching is enabled by opening the connection at Pin 19. If enabled, the pin will exhibit the internally generated half line frequency squarewave. If it is desired to reverse the sense of the PAL swinging burst, it can be done at this pin by pulling Pin 19 low when the squarewave is high. The component envelopes with the proper PAL burst phase are then modulated to produce the composite chroma.

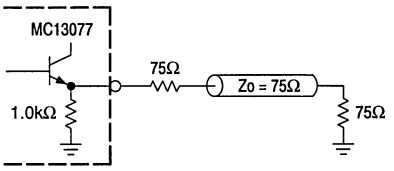
If the MC13077 is encoding to NTSC, only the B-Y color difference component is provided a negative burst flag. This envelope when modulated results in the characteristic –180° phase difference between the color burst and the subcarrier for the B-Y component. Pin 19 should be grounded for NTSC operation to disable the PAL flip-flop.

Video Outputs

After being filtered, the composite chroma is recombined with the composite luma information for the Composite Video output. The composite chroma and composite luma components are also kept separate and buffered for the chroma S-Video and luma S-Video outputs. The video outputs are provided with low impedance emitter-follower stages and, therefore, require an external 75 Ω impedance determining series resistor (see Figure 7). The outputs are designed to drive a 75 Ω load through the external 75 Ω series resistor.

The Composite Video output will provide 1.23 Vp-p of video (sync tip-to-peak chroma) for 100% saturated video at the 75 Ω load. Luma S-Video will be 1.0 Vp-p (sync tip-to-peak white) at the 75 Ω load and the Chroma S-Video output will provide 885 mVp-p at the 75 Ω load.

Figure 7. Composite S-Luma and S-Chroma Video Outputs



APPLICATIONS INFORMATION

Figures 8 through 13 are application examples showing the versatility of the MC13077.

Figure 8. Standard Encoder Application with RGB Inputs and Phase-Locked Subcarrier

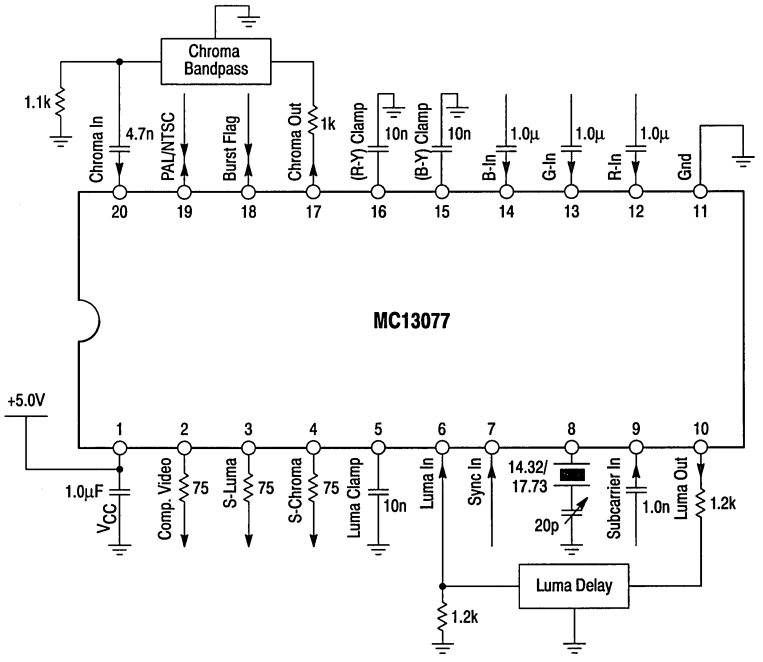


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Figure 9. Encoder with RGB Inputs and Unlocked Subcarrier

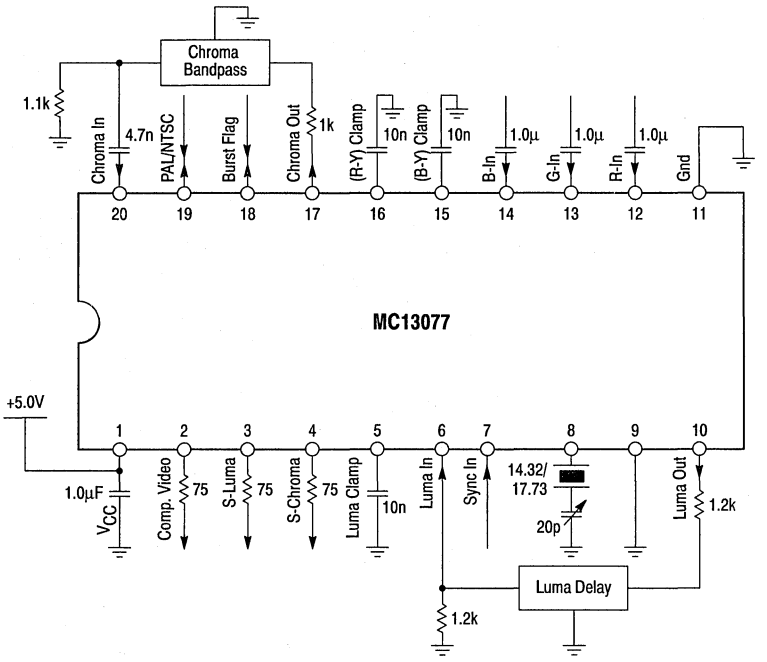


Figure 10. Encoder with RGB Inputs and 4x Subcarrier Drive

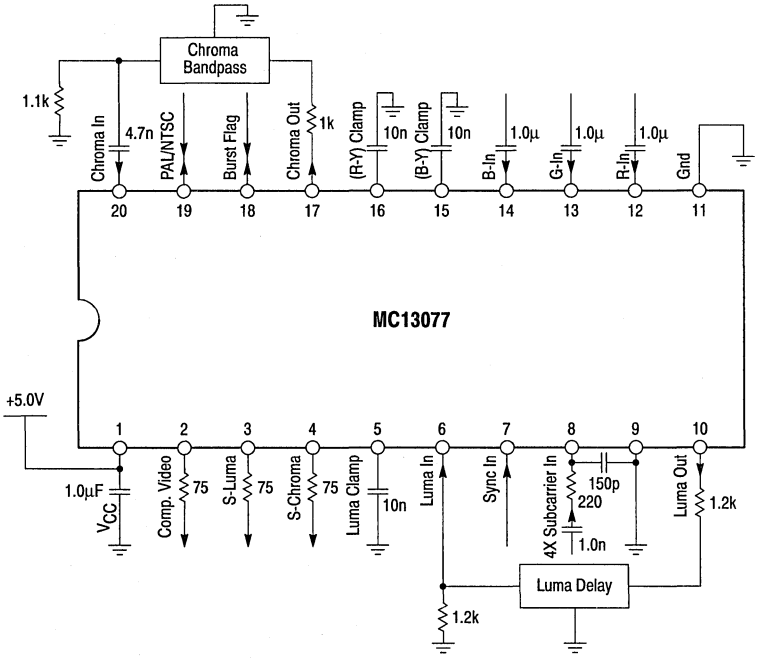


Figure 11. Encoder with Luma and Color Difference Inputs Using Phase-Locked Subcarrier

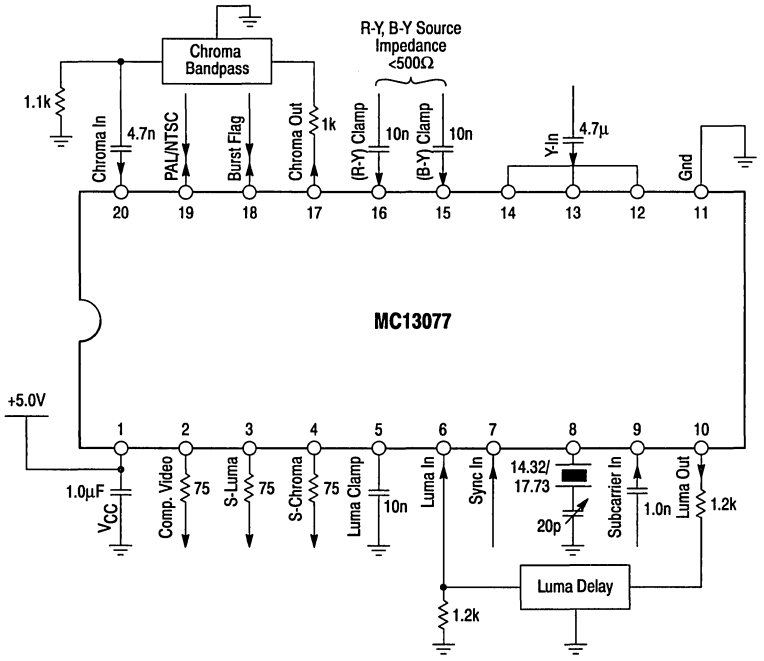


Figure 12. Encoder with Composite Luma and Color Difference Inputs Using Phase-Locked Subcarrier

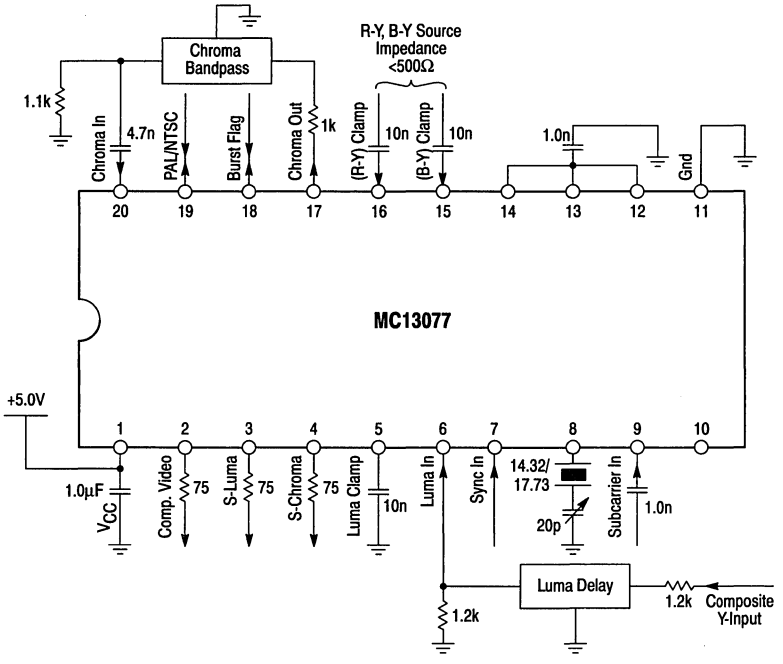
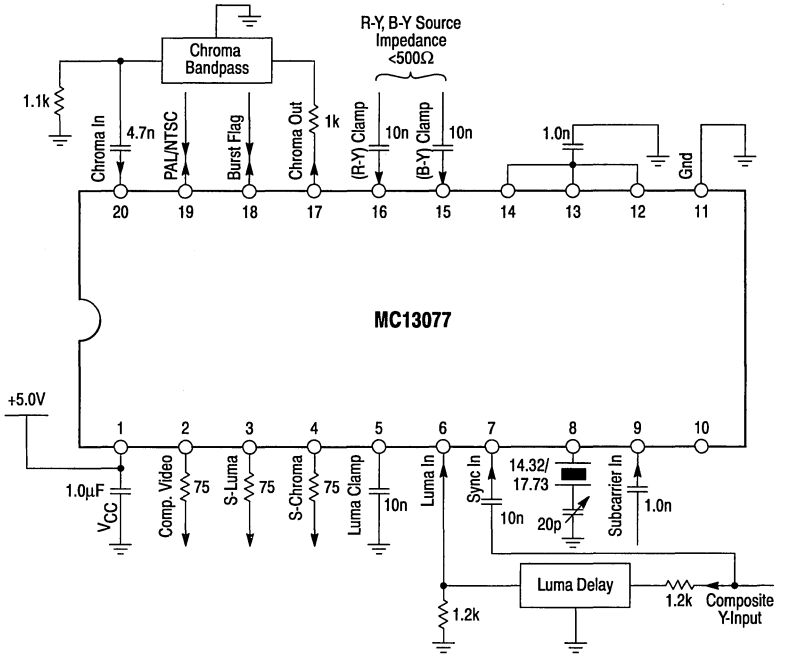


Figure 13. Encoder with Composite Luma and Color Difference Inputs Using the Sync Separator and Having Phase-Locked Subcarrier



9

Recommended Vendors

Bandpass Filters and Delay Lines

TOKO America Inc.
1250 Feehanville Drive
Mt. Prospect, IL 60056

(708) 297-0070
(708) 699-7864 (fax)

Delay Lines

TDK Corp. of America
1600 Feehanville Drive
Mt. Prospect, IL 60056

(708) 803-6100

Crystals

Fox Electronics
5570 Enterprise Pkwy
Ft. Myers, FL 33905

(813) 693-0099

Standard Crystal Corporation
9940 E. Baldwin Place
El Monte, CA 91731

(818) 443-2121

MC34119

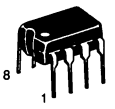
LOW POWER AUDIO AMPLIFIER

SILICON MONOLITHIC INTEGRATED CIRCUIT

Low Power Audio Amplifier

The MC34119 is a low power audio amplifier intergrated circuit intended (primarily) for telephone applications, such as in speakerphones. It provides differential speaker outputs to maximize output swing at low supply voltages (2.0 V minimum). Coupling capacitors to the speaker are not required. Open-loop gain is 80 dB, and the closed-loop gain is set with two external resistors. A Chip Disable pin permits powering down and/or muting the input signal. The MC34119 is available in standard 8-pin DIP or surface mount packaging.

- Wide Operating Supply Voltage Range (2.0 V to 16 V), Allows Telephone Line Powered Applications
- Low Quiescent Supply Current (2.7 mA Typ) for Battery Powered Applications
- Chip Disable Input to Power Down the IC
- Low Power-Down Quiescent Current (65 µA Typ)
- Drives a Wide Range of Speaker Loads (8.0 Ω and Up)
- Output Power Exceeds 250 mW with 32 Ω Speaker
- Low Total Harmonic Distortion (0.5% Typ)
- Gain Adjustable from <0 dB to >46 dB for Voice Band
- Requires Few External Components



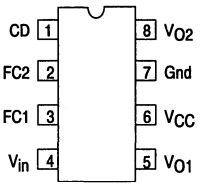
P SUFFIX
PLASTIC PACKAGE
CASE 626

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO-8)

MAXIMUM RATINGS

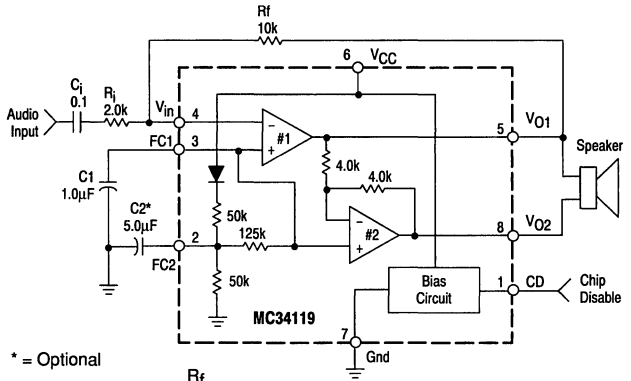
Rating	Value	Unit
Supply Voltage	–1.0 to + 18	Vdc
Maximum Output Current at V_{O1}, V_{O2}	±250	mA
Maximum Voltage @ V_{in}, FC1, FC2, CD Applied Output Voltage to V_{O1}, V_{O2} when disabled	–1.0, V_{CC} + 1.0 –1.0, V_{CC} + 1.0	Vdc
Junction Temperature	–55, + 140	°C

PIN CONNECTIONS



(Top View)

Block Diagram and Typical Application Circuit



* = Optional

Differential Gian = $2 \times \frac{R_f}{R_i}$

ORDERING INFORMATION

Device	Temperature Range	Package
MC34119P	–20° to +70°C	Plastic DIP
MC34119D		SO-8

RECOMMENDED OPERATING LIMITS

Characteristics	Symbol	Min	Max	Unit
Supply Voltage Voltage @ CD (Pin 1)	V_{CC} V_{CD}	+ 2.0 0	+ 16 V_{CC}	Vdc
Load Impedance	R_L	8.0	100	Ω
Peak Load Current	I_L	—	±200	mA
Differential Gain (5.0 kHz Bandwidth)	AVD	0	46	dB
Ambient Temperature	T_A	–20	+ 70	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Amplifiers (AC Characteristics)					
AC Input Resistance (@ V_{In})	r_i	—	>30	—	MΩ
Open-Loop Gain (Amplifier # 1, f < 100 Hz)	A_{VOL1}	80	—	—	dB
Closed-Loop Gain (Amplifier # 2, V_{CC} = 6.0 V, f = 1.0 kHz, R_L = 32 Ω)	A_{V2}	–0.35	0	+0.35	dB
Gain Bandwidth Product	GBW	—	1.5	—	MHz
Output Power; V_{CC} = 3.0 V, R_L = 16 Ω, THD ≤ 10% V_{CC} = 6.0 V, R_L = 32 Ω, THD ≤ 10% V_{CC} = 12 V, R_L = 100 Ω, THD ≤ 10%	 P_{Out3} P_{Out6} P_{Out12}	 55 250 400	 — — —	 — — —	mW
Total Harmonic Distortion (f = 1.0 kHz) (V_{CC} = 6.0 V, R_L = 32 Ω, P_{out} = 125 mW) (V_{CC} ≥ 3.0 V, R_L = 8.0 Ω, P_{out} = 20 mW) (V_{CC} ≥ 12 V, R_L = 32 Ω, P_{out} = 200 mW)	THD 	 — — —	 0.5 0.5 0.6	 1.0 — —	%
Power Supply Rejection (V_{CC} = 6.0 V, ΔVCC = 3.0 V) (C1 = ∞, C2 = 0.01 μF) (C1 = 0.1 μF, C2 = 0, f = 1.0 kHz) (C1 = 1.0 μF, C2 = 5.0 μF, f = 1.0 kHz)	PSRR 	 50 — —	 — 12 52	 — — —	dB
Muting (V_{CC} = 6.0 V, 1.0 kHz ≤ f ≤ 20 kHz, CD = 2.0 V)	GMT	—	>70	—	dB
Amplifiers (DC Characteristics)					
Output DC Level @ V_{O1}, V_{O2}, V_{CC} = 3.0 V, R_L = 16 Ω (R_f = 75 k) V_{CC} = 6.0 V V_{CC} = 12 V	$V_{O(3)}$ $V_{O(6)}$ $V_{O(12)}$	1.0 — —	1.15 2.65 5.65	1.25 — —	Vdc
Output Level (I_{out} = –75 mA, 2.0 V ≤ V_{CC} ≤ 16 V) High (I_{out} = 75 mA, 2.0 V ≤ V_{CC} ≤ 16 V) Low	 V_{OH} V_{OL}	 — —	 V_{CC} –1.0 0.16	 — —	Vdc
Output DC Offset Voltage (V_{O1}–V_{O2}) (V_{CC} = 6.0 V, R_f = 75 kΩ, R_L = 32 Ω)	ΔVO	–30	0	+30	mV
Input Bias Current @ V_{in} (V_{CC} = 6.0 V)	I_{IB}	—	–100	–200	nA
Equivalent Resistance @ FC1 (V_{CC} = 6.0 V) @ FC2 (V_{CC} = 6.0 V)	 R_{FC1} R_{FC2}	 100 18	 150 25	 220 40	kΩ
Chip Disable (Pin 1)					
Input Voltage Low High	V_{IL} V_{IH}	— 2.0	— —	0.8 —	Vdc
Input Resistance (V_{CC} = V_{CD} = 16 V)	R_{CD}	50	90	175	kΩ
Power Supply					
Power Supply Current (V_{CC} = 3.0 V, R_L = ∞, CD = 0.8 V) (V_{CC}= 16 V, R_L = ∞, CD = 0.8 V) (V_{CC} = 3.0 V, R_L = ∞, CD = 2.0 V)	 I_{CC3} I_{CC16} I_{CCD}	 — — —	 2.7 3.3 65	 4.0 5.0 100	 mA mA μA

Note: Currents into a pin are positive, currents out of a pin are negative.

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PIN FUNCTION DESCRIPTION

Symbol	Pin	Description
CD	1	Chip Disable—Digital input. A Logic "0" (<0.8 V) sets normal operation. A logic "1" (≥2.0 V) sets the power down mode. Input impedance is nominally 90 kΩ.
FC2	2	A capacitor at this pin increases power supply rejection, and affects turn-on time. This pin can be left open if the capacitor at FC1 is sufficient.
FC1	3	Analog ground for the amplifiers. A 1.0 μF capacitor at this pin (with a 5.0 μF capacitor at Pin 2) provides (typically) 52 dB of power supply rejection. Turn-on time of the circuit is affected by the capacitor on this pin. This pin can be used as an alternate input.
V_{in}	4	Amplifier input. The input capacitor and resistor set low frequency rolloff and input impedance. The feedback resistor is connected to this pin and V_{O1}.
V_{O1}	5	Amplifier Output #1. The DC level is ≈ (V_{CC} – 0.7 V)/2.
V_{CC}	6	DC supply voltage (+ 2.0 V to + 16 V) is applied to this pin.
GND	7	Ground pin for the entire circuit.
V_{O2}	8	Amplifier Output #2. This signal is equal in amplitude, but 180° out-of-phase with that at V_{O1}. The DC level is ≈ (V_{CC} – 0.7 V)/2.

TYPICAL TEMPERATURE PERFORMANCE (–20° C< T_A < + 70°C)

Function	Typical Change	Units
Input Bias Current (@ V_{in})	± 40	pA/°C
Total Harmonic Distortion (V_{CC} = 6.0 V, R_L = 32 Ω. P_{out} = 125 mW, f = 1.0 kHz)	+ 0.003	%/°C
Power Supply Current (V_{CC} = 3.0 V, R_L = ∞, CD = 0 V) (V_{CC} = 3.0 V, R_L = ∞, CD = 2.0 V)	–2.5 –0.03	μA/°C

DESIGN GUIDELINES

General

The MC34119 is a low power audio amplifier capable of low voltage operation (V_{CC} = 2.0 V minimum) such as that encountered in line-powered speakerphones. The circuit provides a differential output (V_{O1}–V_{O2}) to the speaker to maximize the available voltage swing at low voltages. The differential gain is set by two external resistors. Pins FC1 and FC2 allow controlling the amount of power supply and noise rejection, as well as providing alternate inputs to the amplifiers. The CD pin permits powering down the IC for muting purposes and to conserve power.

Amplifiers

Referring to the block diagram, the internal configuration consists of two identical operational amplifiers. Amplifier #1 has an open-loop gain of ≥80 dB (at f ≤ 100 Hz), and the closed-loop gain is set by external resistor R_f and R_i. The amplifier is unity gain stable, and has a unity gain frequency of approximately 1.5 MHz. In order to adequately cover the telephone voice band (300 Hz to 3400 Hz), a maximum closed-loop gain of 46 is recommended. Amplifier #2 is internally set to a gain of – 1.0 (0 dB).

The outputs of both amplifiers are capable of sourcing and sinking a peak current of 200 mA. The outputs can typically swing to within ≈0.4 V above ground, and to within ≈1.3 V below V_{CC}, at the maximum current. See Figures 18 and 19 for V_{OH} and V_{OL} curves.

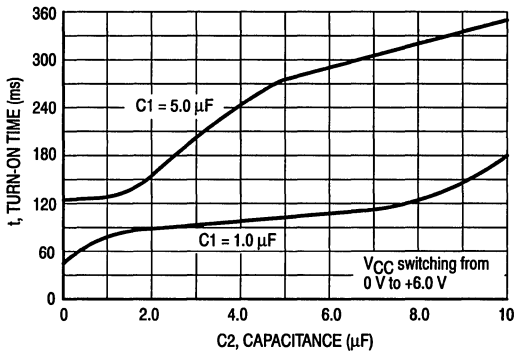
The output DC offset voltage (V_{O1}–V_{O2}) is primarily a function of the feedback resistor (R_f), and secondarily due to the amplifiers' input offset voltages. The input offset voltage of the two amplifiers will generally be similar for a particular IC, and therefore nearly cancel each other at the outputs. Amplifier #1's bias current, however, flows out of V_{in} (Pin 4) and through R_f, forcing V_{O1} to shift negative by an amount equal to [$R_f \times I_{IB}$]. V_{O2} is shifted positive an equal amount. The output offset voltage, specified in the Electrical Characteristics, is measured with the feedback resistor shown in the Typical Application Circuit, and therefore takes into account the bias current as well as internal offset voltages of the amplifiers. The bias current is constant with respect to V_{CC}.

FC1 and FC2

Power supply rejection is provided by the capacitors (C1 and C2 in the Typical Application Circuit) at FC1 and FC2. C2 is somewhat dominant at low frequencies, while C1 is dominant at high frequencies, as shown in the graphs of Figures 4 to 7. The required values of C1 and C2 depend on the conditions of each application. A line powered speakerphone, for example, will require more filtering than a circuit powered by a well regulated power supply. The amount of rejection is a function of the capacitors, and the equivalent impedance looking into FC1 and FC2 (listed in the Electrical Characteristics as R_{FC1} and R_{FC}).

In addition to providing filtering, C1 and C2 also affect the turn-on time of the circuit at power-up, since the two capacitors must charge up through the internal 50 k and 125 kΩ resistors. The graph of Figure 1 indicates the turn-on time upon application of V_{CC} of + 6.0 V. The turn-on time is ≈60% longer for V_{CC} = 3.0 V, and ≈20% less for V_{CC} = 9.0 V. Turn-off time is <10 μs upon removal of V_{CC}.

Figure 1. Turn-On Time versus C1, C2 at Power-On



Chip Disable

The Chip Disable (Pin 1) can be used to power down the IC to conserve power, or for muting, or both. When at a Logic "0" (0 V to 0.8 V), the MC34119 is enabled for normal operation. When Pin 1 is at a Logic "1" (2.0 V to V_{CC} V), the IC is disabled. If Pin 1 is open, that is equivalent to a Logic "0," although good design practice dictates that an input should never be left open. Input impedance at Pin 1 is a nominal 90 kΩ. The power supply current (when disabled) is shown in Figure 15.

Muting, defined as the change in differential gain from normal operation to muted operation, is in excess of 70 dB. The turn-off time of the audio output, from the application of the CD signal, is <2.0 µs, and turn on-time is 12 ms–15 ms. Both times are independent of C1, C2, and V_{CC}.

When the MC34119 is disabled, the voltages at FC1 and FC2 do not change as they are powered from V_{CC}. The outputs, V_{O1} and V_{O2}, change to a high impedance condition, removing the signal from the speaker. If signals from other sources are to be applied to the outputs (while disabled), they must be within the range of V_{CC} and Ground.

Power Dissipation

Figures 8 to 10 indicate the device dissipation (within the IC) for various combinations of V_{CC}, R_L, and load power. The maximum power which can safely be dissipated within the MC34119 is found from the following equation:

$$P_D = (140°C - T_A)/\theta_{JA}$$

where T_A is the ambient temperature; and θ_{JA} is the package thermal resistance (100°C/W for the standard DIP package, and 180°C/W for the surface mount package.)

The power dissipated within the MC34119, in a given application, is found from the following equation:

$$P_D = V_{CC} \times I_{CC}) + (I_{RMS} \times V_{CC}) - (R_L \times I_{RMS}^2)$$

where I_{CC} is obtained from Figure 15; and I_{RMS} is the RMS current at the load; and R_L is the load resistance.

Figures 8 to 10, along with Figures 11 to 13 (distortion curves), and a peak working load current of ±200 mA, define the operating range for the MC34119. The operating range is further defined in terms of allowable load power in Figure 14 for loads of 8.0 Ω, 16 Ω, and 32 Ω. The left (ascending) portion of each of the three curves is defined by the power level at which 10% distortion occurs. The center flat portion of each curve is defined by the maximum output current capability of the MC34119. The right (descending) portion of each curve is defined by the maximum internal power dissipation of the IC at 25°C. At higher ambient temperatures, the maximum load power must be reduced according to the above equations. Operating the device beyond the current and junction temperature limits will degrade long term reliability.

Layout Considerations

Normally a snubber is not needed at the output of the MC34119, unlike many other audio amplifiers. However, the PC board layout, stray capacitances, and the manner in which the speaker wires are configured, may dictate otherwise. Generally, the speaker wires should be twisted tightly, and not more than a few inches in length.

Figure 2. Amplifier #1 Open-Loop Gain and Phase

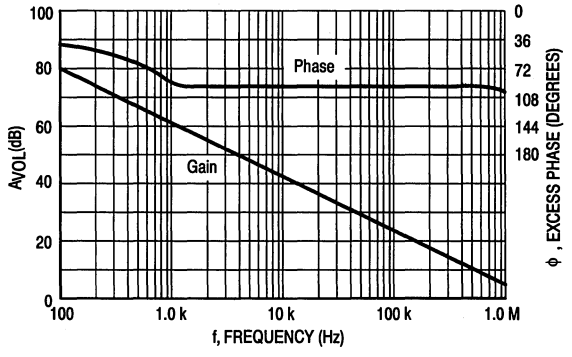


Figure 3. Differential Gain versus Frequency

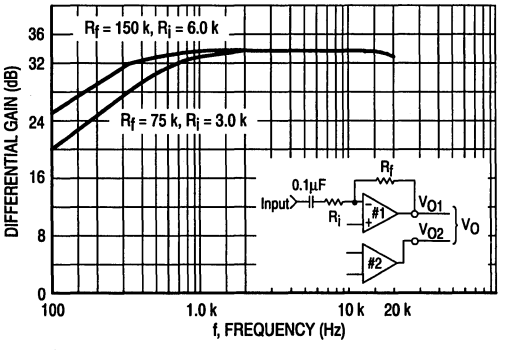


Figure 4. Power Supply Rejection versus Frequency (C2 = 10 μF)

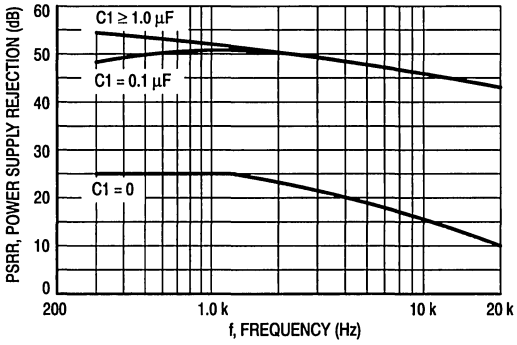


Figure 5. Power Supply Rejection versus Frequency (C2 = 5.0 μF)

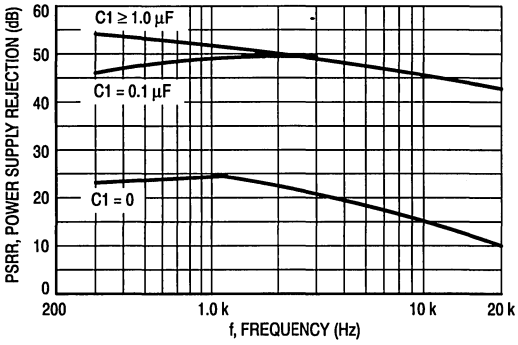


Figure 6. Power Supply Rejection versus Frequency (C2 = 1.0 μF)

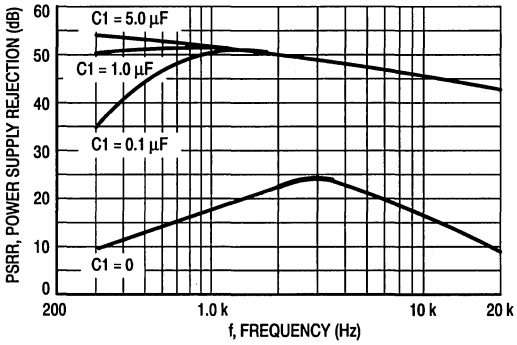


Figure 7. Power Supply Rejection versus Frequency (C2 = 0)

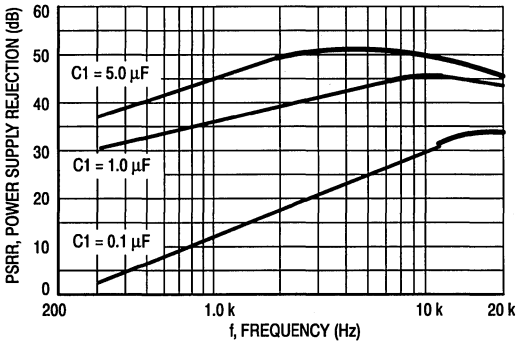


Figure 8. Device Dissipation, 8.0 Ω Load

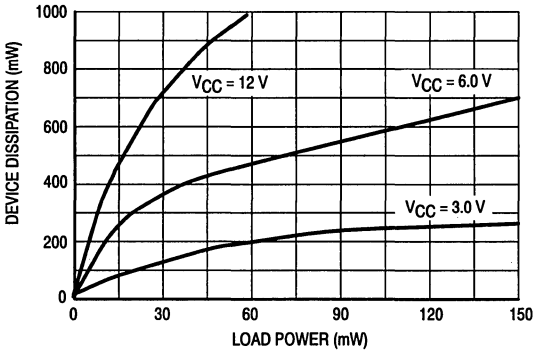


Figure 9. Device Dissipation

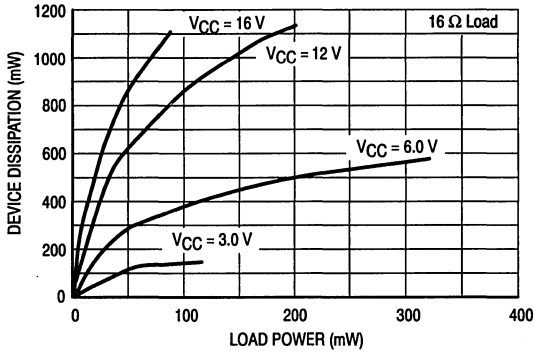


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Figure 10. Device Dissipation, 32 Ω Load

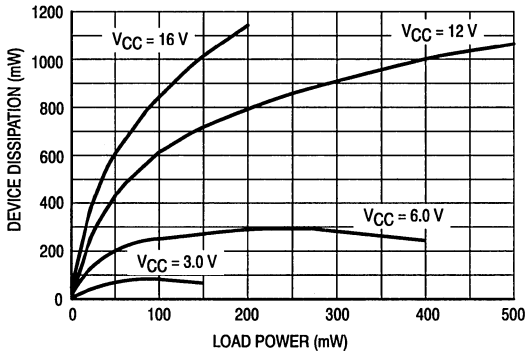

Figure 11. Distortion versus Power
(f = 1.0 kHz, AVD = 34 dB)

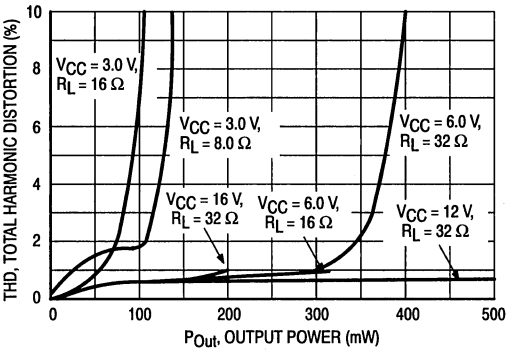

Figure 12. Distortion versus Power
(f = 3.0 kHz, AVD = 34 dB)

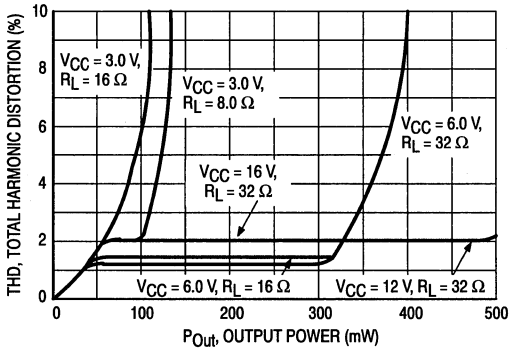

Figure 13. Distortion versus Power
(f = 1, 3.0 kHz, AVD = 12 dB)

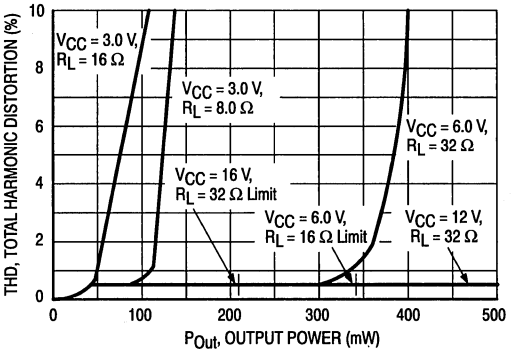

Figure 14. Maximum Allowable Load Power

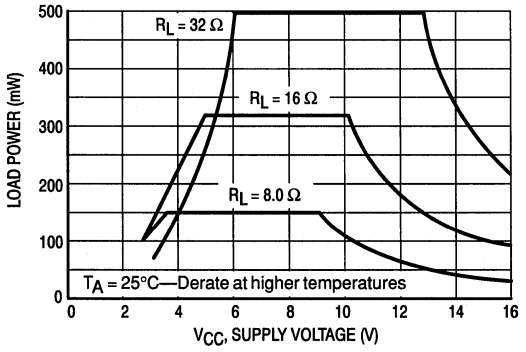

Figure 15. Power Supply Current

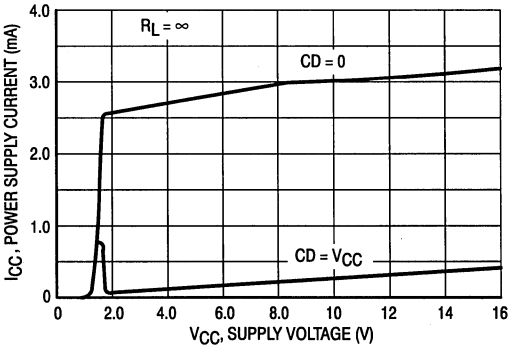

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Figure 16. Small Signal Response

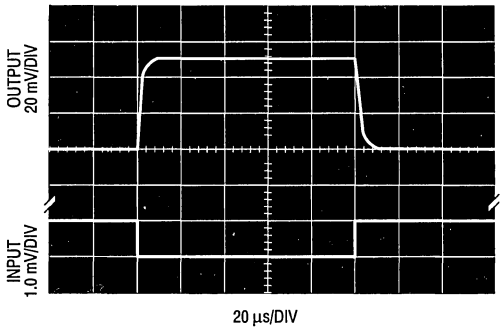


Figure 17. Large Signal Response

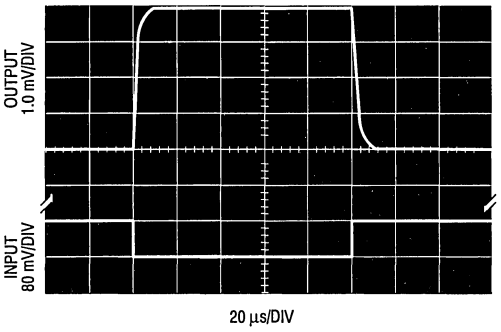


Figure 18. V_{CC}–V_{OH} @ V_{O1}, V_{O2} versus Load Current

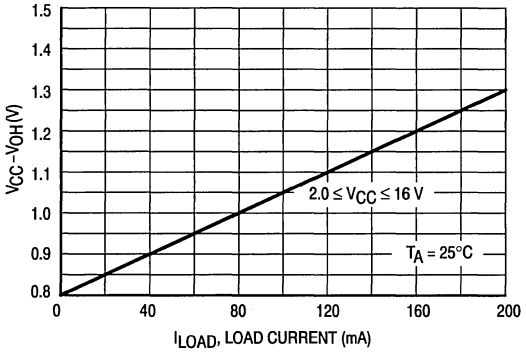


Figure 19. V_{OL} @ V_{O1}, V_{O2} versus Load Current

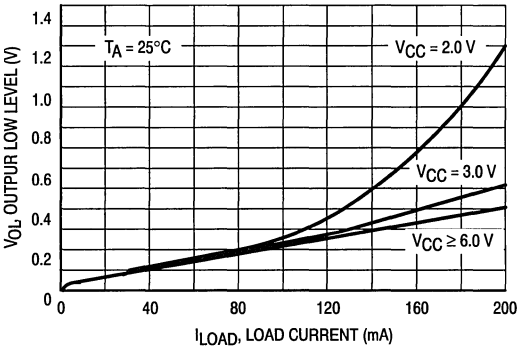


Figure 20. Input Characteristics @ CD (Pin 1)

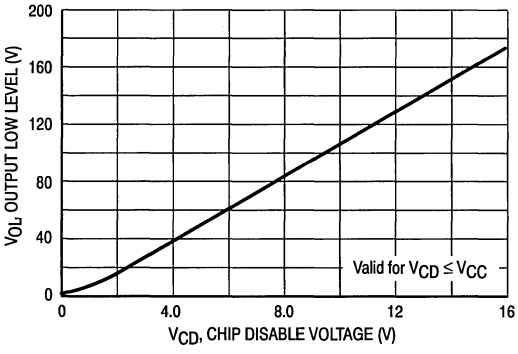
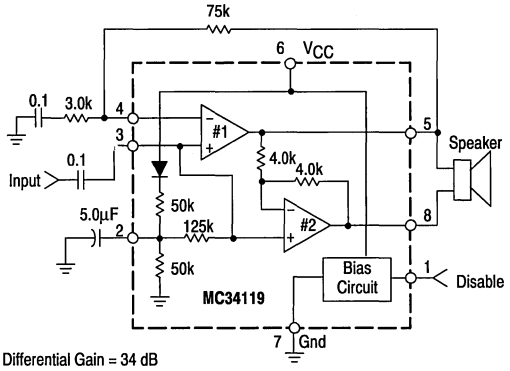


Figure 21. Audio Amplifier with High Input Impedance



Differential Gain = 34 dB
Frequency Response: See Figure 3
Input Impedance ≈ 125 kΩ
PSRR ≈ 50 dB

9

Figure 22. Audio Amplifier with Bass Suppression

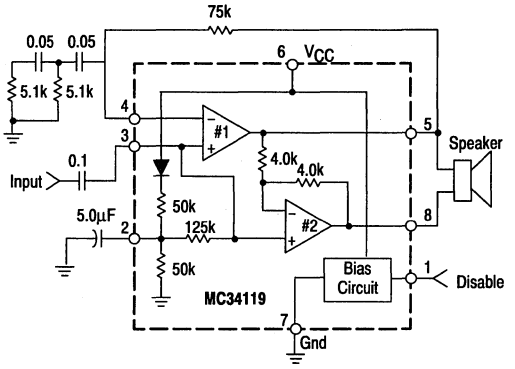


Figure 23. Frequency Response of Figure 22

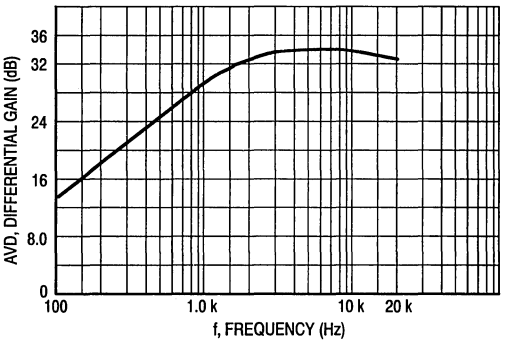


Figure 24. Audio Amplifier with Bandpass

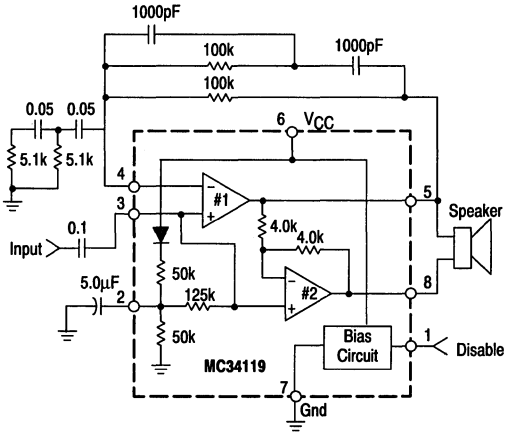


Figure 25. Frequency Response of Figure 24

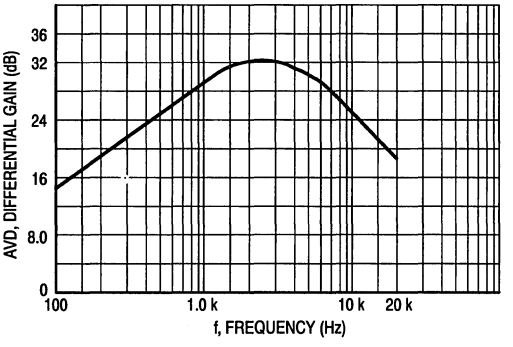
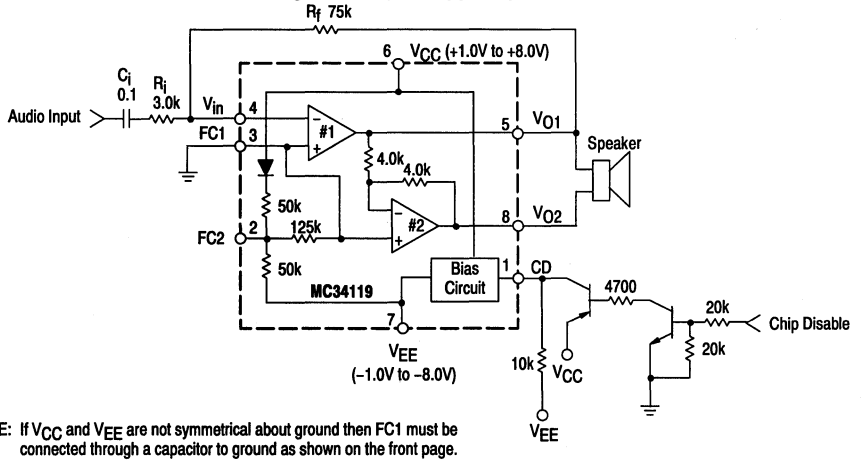


Figure 26. Split Supply Operation



NOTE: If V_{CC} and V_{EE} are not symmetrical about ground then FC1 must be connected through a capacitor to ground as shown on the front page.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC44001

Chroma 4
VIDEO PROCESSOR

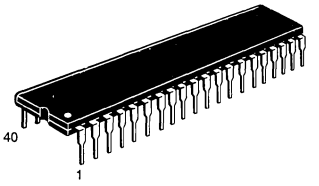
SILICON MONOLITHIC
INTEGRATED CIRCUIT

Product Preview

Chroma 4 Multistandard Video Processor

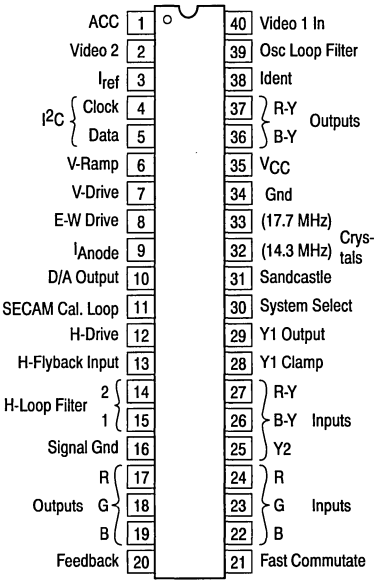
The MC44001 is a highly advanced circuit which performs most of the basic functions required for a color TV. All of its advanced features are under processor control via an I^2C bus, enabling potentiometer controls to be removed completely. In this way the component count may be reduced dramatically, allowing significant cost savings together with the possibility of implementing sophisticated automatic test routines. Using the MC44001, TV manufacturers will be able to build a standard chassis for anywhere in the world.

- Operation from a Single + 5.0 V Supply; Typical Current Consumption Only 120 mA
- Full PAL/SECAM/NTSC capability
- Dual Composite Video or S-VHS Inputs
- All Chroma/Luma Channel Filtering, and Luma Delay Line Are Integrated Using Sampled Data Filters Requiring No External Components
- Filters Automatically Commutate with Change of Standard
- Chroma Delay Line is Realized with a 16 Pin Companion Device, the MC44140
- RGB Drives Incorporate Contrast and Brightness Controls and Auto Gray Scale
- Switched RGB Inputs with Separate Saturation Control
- Auxiliary Y, R-Y, B-Y Inputs
- Line Timebase Featuring H-Phase Control, Time Constant and Switchable Phase Detector Gain
- Vertical Timebase Incorporating Vertical Geometry Corrections
- E-W Parabola Drive Incorporating Horizontal Geometry Corrections
- Beam Current Monitor with Breathing Compensation



P SUFFIX
PLASTIC PACKAGE
CASE 711

PIN CONNECTIONS



(Top View)

MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted.)*

Ratings	Pin	Symbol	Value	Unit
Supply Voltage	35	V_{CC}	6.0	Vdc
Operating Ambient Temperature	35	T_A	0 to + 70	°C
Storage Temperature	—	T_{stg}	− 65 to +150	°C
Junction Temperature	—	T_J	+150	°C
Drive Output Sink Current	12	I_{12}	2.0	mA
Applied Voltage Range:				Vdc
E-W Drive	8	V_8	0 to + 7.0	
Feedback	20	V_{20}	0 to + 7.0	
Anode Current	9	V_9	− 2.0 to V_{CC}	
All Other Pins	—	V_i	0 to V_{CC}	

* (Based on C26K, C32K, C63K and C88K geometries characterizations)

ORDERING INFORMATION

Device	Temperature Range	Package
MC44001P	0° to + 70°C	Plastic DIP

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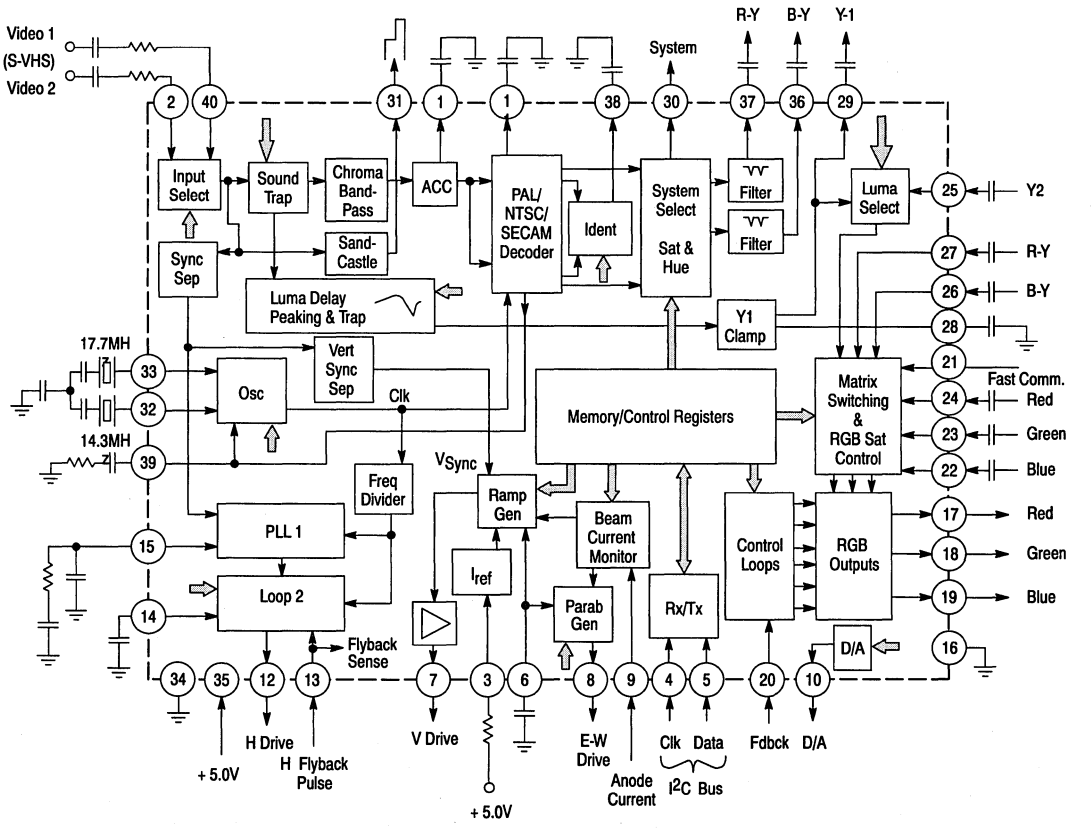
ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc, I_3 = 70 µA, T_A = 25°C, unless otherwise noted.)

Characteristic	Pin	Min	Typ	Max	Unit
Supply Voltage	35	4.75	5.0	5.12	V
Operating Current	35	90	120	180	mA
Reference Current, Input Voltage	3	1.0	1.30	1.60	V
D/A Output Offset D/A Output Register Set to 00	10	– 5.0	0	+ 5.0	µA
D/A Output Range D/A Output Register Varying from 00 to 63	10	100	300	500	µA

NOTES: Composite Video Input Signal Level = 1.0 Vpp
Black-to-White = 0.7 Vpp, Syn-to-Black = 0.3 Vpp
PAL/NTSC = 75% color bars; Burst = 300 mVpp
SECAM = 75% color bars
Horizontal Timebase started (subaddress 00)
Vertical Breathing control set to 00; V9 = 0 V
All other analog controls set to midrange 32
Video Peaking "P1, P2, P3" bits high

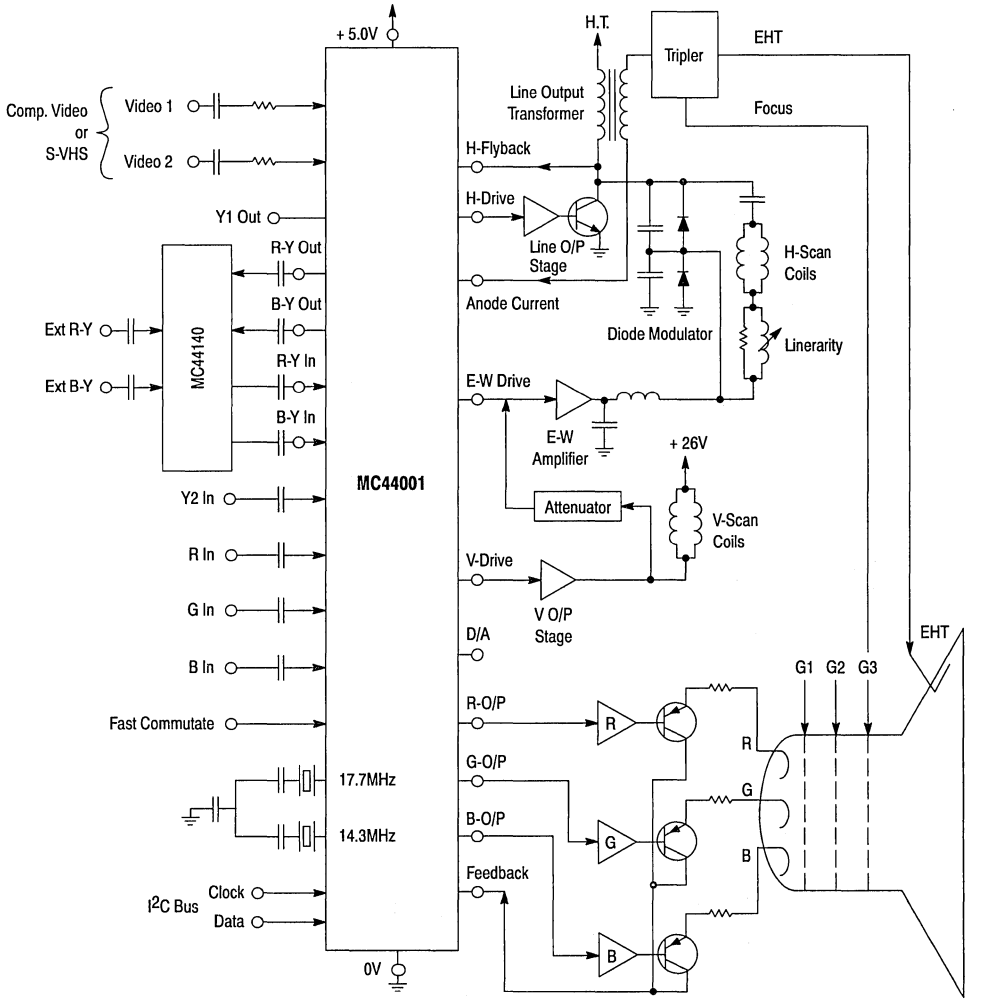
Simplified Block Diagram



GENERAL DESCRIPTION OF THE CHROMA 4 SYSTEM

Figure 1 shows a simplified block diagram representation of the basic system using the MC44001 and its companion device the MC44140 chroma delay line. The Chroma 4 has been designed to carry out all the processing of video signals, display controls and timebase functions. There are two video inputs which can be used for normal composite video or separate Y and C inputs. In either case, the inputs are interchangeable and selection is made via the I²C bus. The video is decoded within the MC44001 which involves separation, filtering and delay of the luminance part of the signal, and demodulation of the chroma into color difference signals. The luminance (called Y1) together with the demodulated R-Y and B-Y are all then brought out from the IC. The color difference signals then enter the MC44140 which performs color correction in PAL and the delay line function in SECAM. Corrected color difference signals then re-enter the MC44001.

Figure 1. Connection to TV Chassis



The next stage is called the color difference stage where a number of control functions are carried out together with matrixing of the components to derive RGB signals. At this point a number of auxiliary signals may also be switched in, again all under MCU control. External RGB (text) and Fast Commutate enter here; also an external luminance (Y2) may be used instead of Y1. External R-Y and B-Y are switched in via the delay line circuit to save pins on the main device. The Y2 and External R-Y, B-Y will obviously be of considerable benefit from the system point of view for use with either feature boxes MAC or CTI.

The final stage of video processing is the RGB outputs which drive the high voltage amplifiers connected to the tube cathodes. These outputs are controlled by a sophisticated digital servo-loop which is maintained and stabilized by a sequentially sampled beam current feedback system. Automatic gray scale control is featured as a part of this system.

Both horizontal and vertical timebases are incorporated into the MC44001 and control is via the I^2C bus. The horizontal timebase employs a dual loop system of a PLL and variable phase shifter, and the vertical uses a countdown system. For the vertical, a field rate sawtooth is available which is used to drive an external power amplifier with flyback generator (usually a single IC). The line output consists of a pulse which drives a conventional line output stage in the normal way. The line flyback pulse is sensed and used by the second loop for horizontal phase shift.

Where E-W correction is required, a parabola waveform is available for this which, with the addition of a power amplifier, can be used with a diode modulator type line output stage for dynamic width and E-W control. The bottom of the EHT overwinding is returned to the MC44001 and is used for anode current monitoring and anti-breathing correction.

A much more detailed description of each stage of the MC44001 will be found in the next section. Information on the delay line is to be found in this data sheet.

Introduction

The following information describes the basic operation of the MC44001 IC together with the MC44140 chroma delay line. The MC44001 is a highly advanced circuit which performs all the video processing, timebase and display functions needed for a modern color TV. The device employs analog circuitry but with the difference that all its advanced features are under processor control, enabling external filtering and potentiometer adjustments to be removed completely. Sophisticated feedback control techniques have been used throughout the design to ensure stable operating conditions and the absence of drift with age.

The IC described herein is one of a new generation of TV circuits, which make use of a serial data bus to carry out control functions. Its revolutionary design concept permits a level of integration and degree of flexibility never achieved before. The Chroma 4 consists of a single bipolar VLSI chip which uses a high density, high frequency, low voltage process called MOSAIC 1.5. Contained within this single 40 pin package is all the circuitry needed for the video signal processing, horizontal and vertical timebases and CRT display control for today's color TV. Furthermore, all the user controls and manufacturer's set-up adjustments are under the control of the processor I^2C bus, eliminating the need for potentiometer controls. Chroma 4 offers an enormous variety of different options configurable in software, to cater to virtually any video standard or circumstance commonly met. The decoder section offers full multistandard capability, able to handle PAL, SECAM and NTSC standards. Practically all the filtering is carried out onboard the IC by means of sampled data filters, and requires no external components or adjustment.

Digital Interface

One of the most important features of Chroma 4 is the use of processor control to replace external potentiometer and filter adjustments. Great flexibility is possible using processor control, as each user can configure the software to suit their individual application. The circuit operates on a bidirectional serial data bus, based on the well known I^2C bus. This system is rapidly becoming a world standard for the control of consumer equipment.

I²C Bus

It is not within the scope of this data sheet to describe in detail the functioning of the I²C bus. Basically, the I²C bus is a two-wire bidirectional system consisting of a clock and a serial data stream. The write cycle consists of 3 bytes of data and 3 acknowledge bits. The first byte is the Chip Address, the second the Sub-address to identify the location in the memory, and the third byte is the data. When the address' Read/Write bit is high, the second and third bytes are used to transmit status flags back to the MCU.

Figure 2 shows a block diagram of the MC44001 Bus Interface/Decoder. To begin with, the start bit is recognized by means of the data going low during CLK high. This causes the Counter and all the latches to be reset. For a write operation, the Write address ($88) is read into the Shift Register. If the correct address is identified, the Chip Address Latch is set and at CLK 9 an acknowledge is sent.

The second byte is now read into the Shift Register and is used to select the Sub-address. At CLK 18 a Sub-address Enable is sent to the memory to allow the Data in the register to be changed. Also at CLK 18 another acknowledge is sent.

The third byte is now read into the Shift Register and the Data bussed into the memory. The Data in the Sub-address location already selected is then altered. A third acknowledge is sent at CLK 27 to complete the cycle.

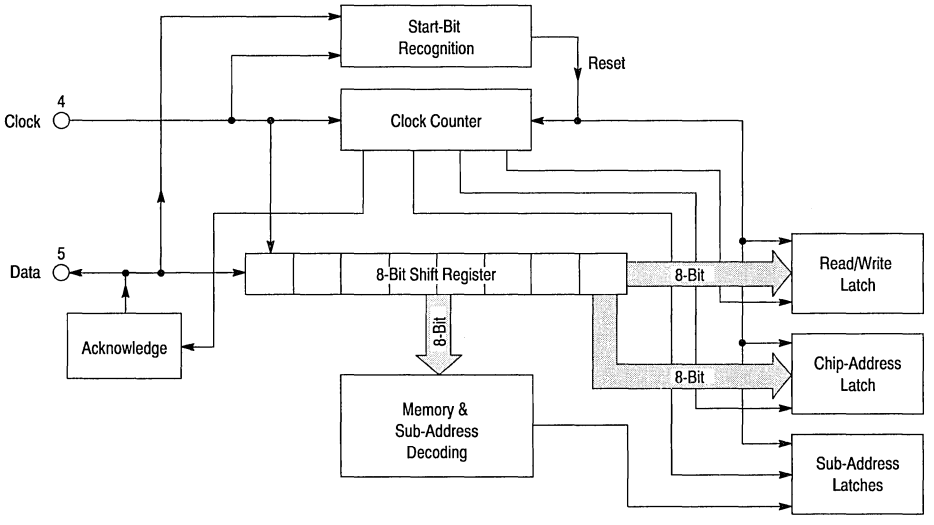
A Read address ($89) indicates that the MCU wants to read the Chroma 4 status flags. In this instance, the Read/Write Latch is set, causing the Memory Enable and Subaddress Enable to be inhibited, and the flags to be written onto the data line. Two of the status flags are permanently wired one-high and one-low (O.K. and Fault), to provide a check on the communication medium between the MC44001 and the MCU.

At start-up the Counter is automatically reset and the Data for each Sub-address is read in. Only after the entire memory contents has been transmitted, is Data 00 sent to start the Horizontal Drive.

It must be noted that Chroma 4 does not fully conform to the I²C bus specification. The protocol of the Chroma 4 bus differs from that of the I²C bus in the following respect:

When the device is in the Read mode, it starts with the Chip Address as always, but detects the Read bit high and sends an acknowledge (SDA pulled low). The first byte of data is transmitted to the MCU and an acknowledge is also given. The second byte is transmitted, again followed by an acknowledge. These two acknowledges are always transmitted, both in the Read and Write mode. In the I²C bus specification, it is normally the receiver device which provides the acknowledge, in order to indicate the validity of the transmission.

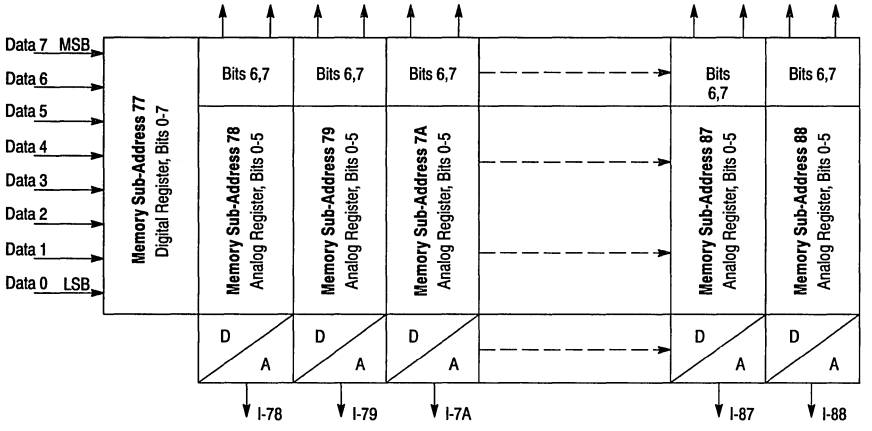
Figure 2. I²C Bus Interface and Decoder



Memory

Figure 3 shows a diagram of the MC44001 Memory Map. It has 18 bytes of memory which are located at hex sub-addresses 77 to 88. Sub-address 77 is used to set up the vertical timebase mode of the IC and for S-VHS switching, and consists of 8 separate data bits. The remaining 17 bytes use the least significant 6-bits as an analog control register. The contents of each are D/A converted, providing an analog control current which is distributed to the appropriate part of the circuit. Bits 6 and 7 are used singularly for switching control functions.

Figure 3. MC44001 Memory Map



Chroma Decoder

The main function of this section is to decode the incoming composite video, which may be in any of the PAL, NTSC or SECAM Standards, and to retrieve the luminance and color difference signals. In addition the signal filtering and luma delay line functions are carried out in this section by means of sampled data filters.

The entire decoder section operates in sampled data mode using clocks generated by external crystals. The oscillator, which is phase-locked in the usual way for PAL/NTSC modes, provides the clock function for the whole circuit. The crystals are selected by the MCU by means of a control bit. Only crystals appropriate to the standards which are going to be received need to be fitted. A 17.7 MHz crystal (4x PAL subcarrier) is used for PAL and SECAM systems (50 Hz, 625 lines); and 14.3 MHz (4x NTSC subcarrier) for the NTSC system (60 Hz, 525 lines). Nearly all the filters, together with the luma delay line and peaking, have been integrated, requiring no external components or any adjustment. The filter characteristics are entirely determined by the clocks and by capacitor ratios, and are thus completely independent of variations in the manufacturing process. The PAL/NTSC subcarrier PLL and ACC loop filters have not been integrated in order to facilitate testing. These filters consist of fixed external components.

Figure 4 is a block diagram of the main features of the chroma decoder. Selection is first made between the V1 and V2 inputs. These may be either normal composite video or separate luma and chroma which may enter the IC at either pin. Commands from the MCU are used to route the signals through the appropriate delay and filter sections. A composite video signal first passes through the sound trap filter which is of recursive design. With the 17.7 MHz crystal selected the following trap frequencies may be set by an MCU control word: 5.5 MHz, 6.0 MHz, 6.5 MHz. Next, the video enters the luma delay line and SECAM cloche filter. The PAL or NTSC chroma signal is separated out by a transversal filter receiving inputs from taps along the luma delay line, arranged in such a way that group delays in PAL and SECAM are nominally equalized. A second set of taps feeds another transversal filter whose function is to provide a chroma trap combined with luma channel peaking. In SECAM mode the trap frequency is dynamically steered to follow the instantaneous frequency of the chroma.

The high frequency luma may be peaked in 1 dB steps, up to a maximum of + 6 dB, by a control word from the MCU. Another control word is used to trim the delay in the luma channel. Five steps of 56 ns are possible, giving a total programmable delay of 280 ns. The resulting processed luma signal then proceeds to the color difference section. The luma output (Y1) is also made available at Pin 29, for use with frame store or other auxiliary function.

As all the delay and filter responses are determined by the clock, they automatically commute to the new standard when the crystal is changed over. Thus, when the 14.3 MHz clock is being used the chroma trap moves to 3.58 MHz, and the sound traps move to 4.5 MHz.

The filtered PAL/NTSC and SECAM chroma signals are decoded by their respective circuits. The PAL/NTSC decoder employs a conventional design, using ACC action for gain control and the common double balanced multipliers to retrieve the color difference signals. The SECAM decoder is discussed in a separate subsection.

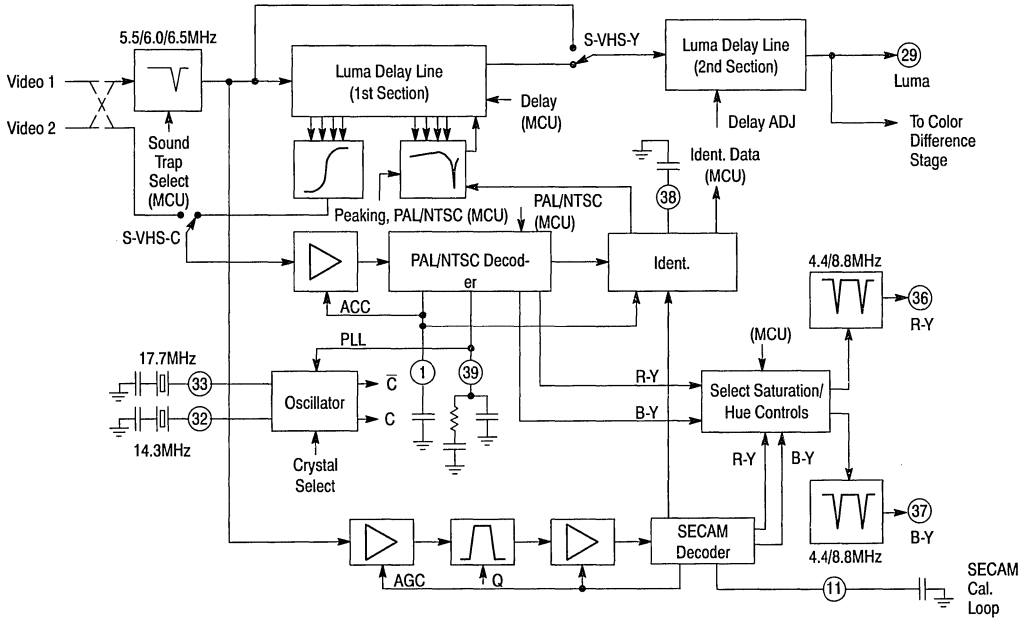
The identification signals from the PAL and SECAM decoders are set in opposition to each other, this being done as the best way to prevent misidentification between the two. The actual decision as to a signal's identity is made by the MCU based on data provided by 3 flags returned to it, namely: ACC Active, PAL Identified, and SECAM Identified.

This allows a maximum of flexibility, since the software may be written to accomodate many different sets of circumstances. For example, channel information could be taken into account if certain channels always carry signals in the same standard. Alternatively, if one standard is never going to be received, the software can be adapted to this circumstance. If none of the flags are on, color killing will be implemented by the MCU. This occurs if the net Ident Signal is too low, or if the ACC circuit is inactive due to too low a signal level.

The demodulated color difference signals now enter the Saturation/Hue control section, where selection is made between PAL/NTSC and SECAM outputs. The Saturation and Hue control is simply realized by altering the amplitudes of both color difference signals together. Hue control is only a requirement in NTSC mode and would not normally be used for other standards. The function is usually carried out prior to demodulation of the chroma by shifting the phase of the subcarrier reference, causing decoding to take place along different axes. In Chroma 4, Hue control is performed on the already demodulated color difference signals. A proportion of the R-Y signal is added or subtracted to the B-Y signal and vice-versa. This has the same effect as altering the reference phase. If desired, Chroma 4 can apply the Hue control to simple PAL signals.

After manipulation by the Saturation and Hue controls the color difference signals are finally filtered to reduce any remaining subcarrier and multiplier products. Before leaving the chip at Pins 36 and 37, the signals are blanked during line and frame intervals. The 64 µs chroma delay line is carried out by a companion device, the MC44140.

Figure 4. Chroma Decoder



SECAM Decoder

The SECAM signal from the high-pass filter enters tightly controlled AGC amplifiers wrapped around a cloche filter which is a sampled recursive type, with the AGC derived from a signal squarer. Next, the signal is blanked during the calibration gate period and a reference 4.43 MHz is inserted during this time. The SECAM signal is then passed through a limiter.

The frequency demodulator function is carried out by a frequency-locked-loop (F.L.L.). This consists of three components: a tracking filter, a phase detector and a loop filter. The center frequency of the tracking filter depends on three factors: internal R-C product, ADJUST voltage, TUNING voltage. The tracking filter is dynamically tuned by the TUNING feedback from the loop-filter forming the F.L.L. The ADJUST control calibrates the F.L.L. and compensates for variations in the R-C product. After the F.L.L. the color difference signals are passed to another block where several functions are carried out. The signals are de-emphasized and outputs are provided to the IDENT section. Another function of this section is to generate the I_{COMP} signal used for calibrating the F.L.L. This signal is blanked during the H-IG period to ensure that (R-Y) and (B-Y) output signals have a clean DC level for clamping purposes.

In addition, components are added to compensate for the R-C product, and tuning offsets are introduced during the active lines for F0R/F0B.

Calibration of the F.L.L. takes place during every field blanking interval, starting from field retrace and ending just before the SECAM vertical ident. sequence (bottles). The calibration current I_{CAL} is derived from I_{COMP} during the calibration gate (CAL) and integrated by an external capacitor on Pin 11. The resulting voltage V_{EXT} is then transformed to generate the ADJUST control voltage removing from the loop range most of the variations due to internal RC products and temperature.

Color Difference Stages

This stage accepts luminance and color difference signals, together with external R,G,B and Fast Commutation inputs and carries out various functions on them, including clamping, blanking, switching and matrixing. The outputs, consisting of processed R,G,B signals, are then passed to the Auto Gray Scale section.

A block diagram of this stage is shown in Figure 6. The Y2, R-Y, B-Y together with R, G and B are all external inputs to the chip. The Y1 signal comes from the decoder section. Each of the signals is back-porch clamped and then blanked. The Y2 and R,G,B inputs have their own simple sync separators, the output from which may be used as the primary synchronization for the chip by means of commands from the MCU.

The Fast Commutation is an active high input used to drive a high speed switch; for switching between the Y and color difference inputs and the R,G,B (text) inputs.

After blanking, the Y1 and Y2 channels go to the Luma Selector which is controlled by means of 2-bits from the MCU. From here the selected luma signal goes to the RGB matrix. The two color difference signals pass through a second saturation control, whose main function is described later. From here they go to a matrix in which G-Y is generated from the R-Y and B-Y, and lastly, to another matrix where Y is added to the three color difference signals to derive R,G,B.

The R,G,B inputs may take one of two different paths. They may either go straight to the output without further processing, or via a separate matrix and the second saturation control. The path taken is controlled in software. When the latter route is selected, the R,G,B signals undergo a matrix operation to derive Y. From this R-Y and B-Y are easily derived by subtraction from R and B; the derived color difference signals are then subjected to saturation control. The second saturation control may be disabled by the MCU if desired. This extra circuitry allows another feature to be added to the TV set, namely the ability to adjust the color saturation of the RGB inputs. This is not possible on present day receivers. After the saturation control the derived signals are processed as before.

Figure 5. SECAM Decoder

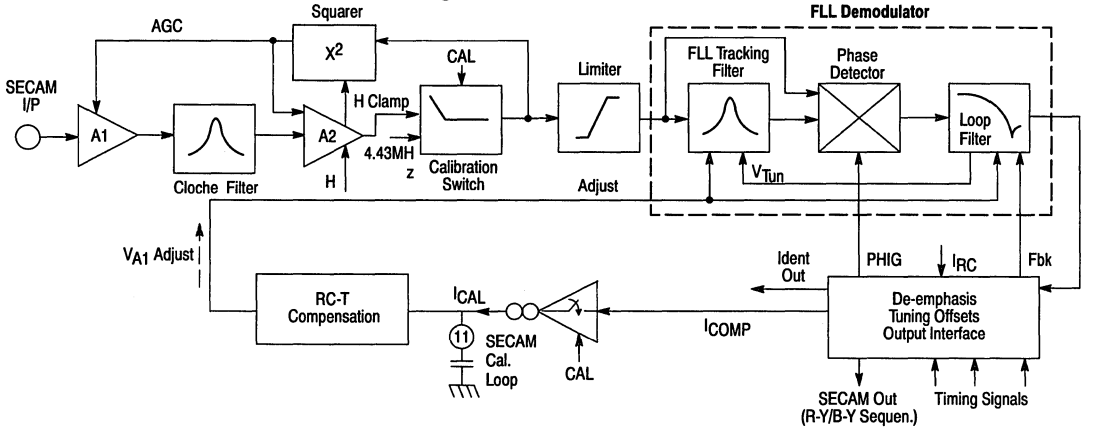
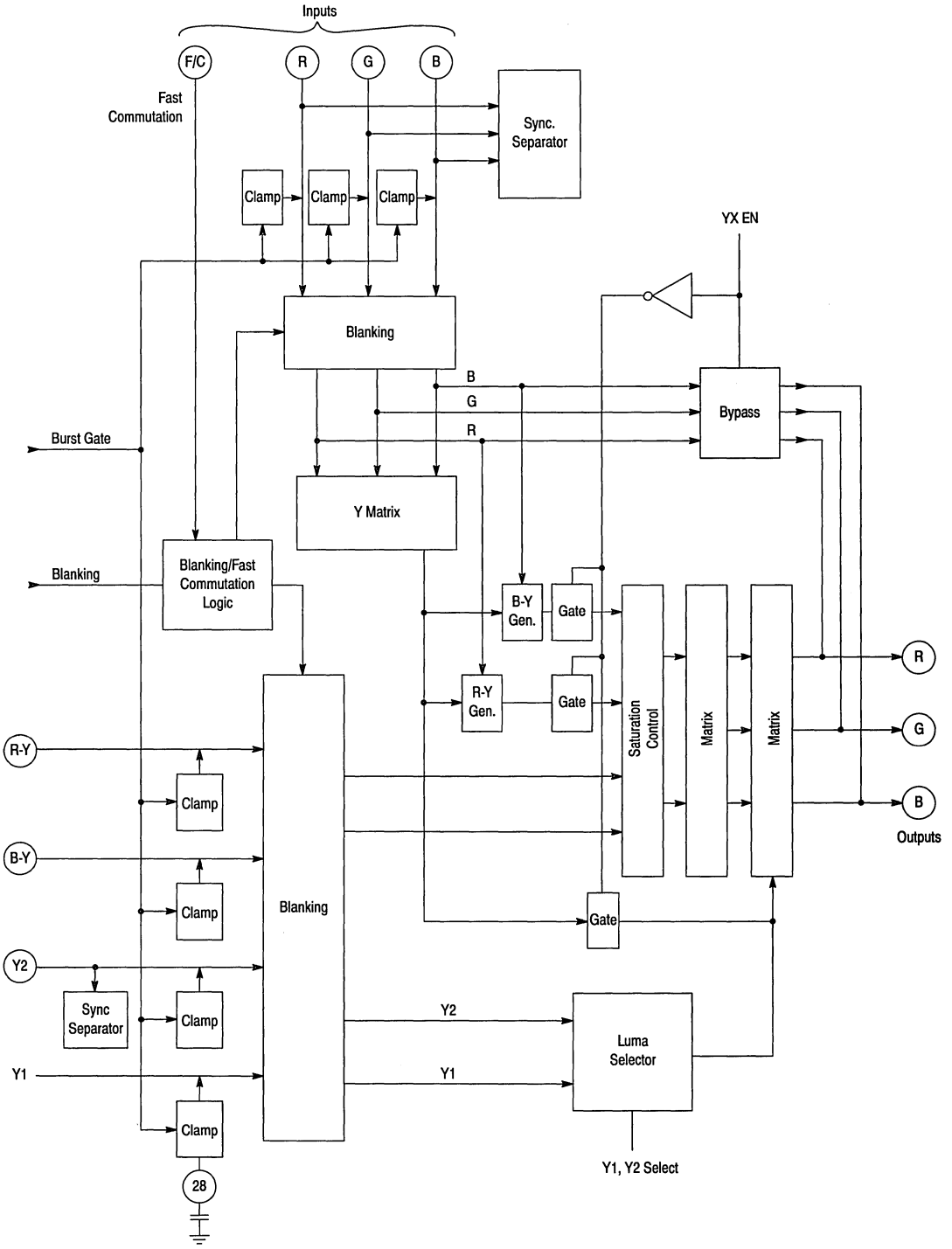


Figure 6. Color Difference Stages



Auto Gray Scale Control Loops

This section supplies current drives to the RGB cathode amplifiers and receives a signal feedback from them, proportional to the combined cathode currents. The current feedback is used to establish a set of feedback loops to control the DC and gain of the RGB drives. There are three loops to control the dark currents and another three to control the gains. During the field blanking period the video outputs are switched off and a set of references are inserted on three consecutive lines to control the R, G, and B outputs respectively. The white current reference pulses are sent first, followed by the black current reference pulses. Drives whose outputs are not being monitored are rendered nonconducting during this time.

A block diagram of the complete system is illustrated in Figure 7. Data words from the MCU which represent the RGB color temperatures selected at the factory, are stored in Latches 1,2,3 and D/A converted by DAC1,2,3 to reference currents. During, e.g., the red dark current set-up period, the reference current from DAC1 is selected and compared with the feedback current. The currents must match each other. If not, a current will flow in resistor R producing an error voltage. This is then buffered into comparators Comp1, 2 and is compared with voltage references Vref1 and Vref2. If the error voltage is greater than Vref1, Comp1 causes the counter to count up. If the error voltage is less than Vref2, Comp2 sends a count-down command. In this way a "deadband" is set up to prevent the outputs from continuously changing.

During Load the contents of the counter are loaded into Latch 6 (for red DC) and then D/A converted by DAC6. The resulting DC current is then applied as an offset to the red output amplifier, completing the loop. For white current set-up the same color temperature data is used but multiplied by a common factor. A common pulse representing a white level is applied to the RGB cathode amplifiers. The feedback loop adjusts the gains to establish a set of cathode currents scaled by a common factor to a set of black currents. Therefore, the image color will always be adjusted to match the black level color; i.e. gray scale tracking is ensured.

The Load/Backload sequencer is used to control which latch is being addressed at any given time by means of the timing signals input to it. The backload command sends the data from the appropriate latch to the Up/Down Counter, ready to be modified if necessary.

The Brightness control is affected by simply changing the DC pedestal of all three drives by the same amount, and does not form part of the feedback loop. The Contrast is adjusted to a set of values dependent on the level of the input pulse applied during the calibration time. This level is set by a control word from the MCU. Once the loops have stabilized under normal working conditions, they may be deactivated by means of a control bit from the MCU. When, however, any change is made to either contrast or brightness, the loops must be reactivated.

An extra loop has been included via Latch 4 and DAC 4, which operates during the field flyback time to compensate for offsets within the loop. This has the effect of counteracting any input offset from the Buffer/Amp and will also compensate for cathode leakage should this be needed.

A second output of the reference currents from DAC6, 8 and 10 are used to compare with preset limits, to ensure that the loops are working within their range of control. Should the limits be exceeded in either direction, flags are returned to the MCU to request that the G2 control be adjusted up or down as appropriate.

Horizontal Timebase

The horizontal timebase consists of a PLL which locks up to the incoming horizontal sync, and a phase detector and shifter whose purpose is to maintain the H-Drive in phase with the line flyback pulse.

Because of on-chip component tolerances, the free-running oscillator frequency cannot be set more accurately than ± 40%; whereas ± 5% would be a more appropriate figure for the sake of the line output stage. For this reason the free-running frequency is calibrated periodically by other means. Continuously during start-up and thence during two lines every field, the phase detector is disconnected from the VCO. A block diagram of the line timebase is given in Figure 8. The calibration loop consists of a frequency comparator driving an Up/Down Counter. The count is D/A converted to give a DC bias which is used to correct a 1.0 MHz VCO. The 1.0 MHz is divided by 64 to give line frequency and this is returned to the frequency comparator. This compares Fh from the VCO with a reference derived from dividing down the subcarrier frequency. Any difference in frequency will result in an output from the comparator, causing the counter to count up or down; and thus closing the loop.

A Coincidence Detector looks at the PLL Fh and compares it with the incoming H-sync. If they are not in lock, a flag is returned to the MCU. To allow for use with VCRs, the gain of the phase detector and the loop time constant may be switched by means of commands from the MCU.

Twice line frequency is output from the PLL which may be divided by either 1 or 2 depending on the command of the MCU. The x2 Fh will be used with Frame Store TV in the future. The phase of the Fh and flyback pulses are compared in a phase detector, whose output drives a phase shifter. A 6-bit control word and D/A converter are used to apply an offset to the phase detector giving a horizontal phase shift control. Also the phase of the horizontal drive may be shifted by 180 degrees with a control bit set by the MCU.

The presence of the horizontal flyback pulse is detected; if it is missing a warning flag is sent back to the MCU which can take appropriate action.

Vertical Timebase

The vertical timebase consists of two sections; a digital section which includes a vertical sync separator and standard recognition; and an analog section which generates a vertical ramp which may be modified under MCU control to allow for geometrical adjustments. A parabola is also generated and may be used for pin-cushion (E-W) correction and width control (see Figure 9).

The MC44001 uses a video sync separator which works using feedback, such that the threshold level of a comparator (slice level) is always maintained at the center of the sync pulse. Sync from any of the auxiliary inputs may also be used. The composite sync is fed to a vertical sync separator, where vertical sync is derived. This consists of a comparator,

up/down counter and decoder.The counter counts up when sync is high, and down when sync is low. The output of the decoder is compared with a threshold level, the threshold only being reached with a high count during the broad pulses in the field interval.

Initially the vertical timebase operates in Injection Lock mode, until a standard signal is recognized (525, 625), then it is switched to a Countdown mode. A standard recognition circuit is employed, which looks for a count of more or less than 576; the standard recognized is then indicated to the MCU. Commands from the processor may be used to force the timebase to operate only in Countdown mode at 525 or 625 lines, or stay in Injection Locked mode.

An adjustable current source is used to charge an external capacitor at Pin 6 to generate a vertical ramp. The amplitude of the ramp is varied according to the current source (Height), and is automatically adapted when the 525 standard is recognized by multiplying by 1.2. The Linearity control is achieved by squaring the ramp and either adding or subtracting a portion of it to the main linear current.

The final ramp with corrections added is then passed to a driver/amplifier and is output at Pin 7. The vertical ramp can be used to drive a separate vertical deflection power circuit with local feedback control. Vertical "S" Correction will then be made using fixed components within the feedback loop of the power op amp.

The reference ramp is squared to provide a pin-cushion correction parabola, developed across an external resistor at Pin 8. The parabola amplitude may be varied from zero to a maximum level set by the external resistor. The parabola itself is squared, giving and independent fourth order term (Corner Correction) whose level can also be varied; this is then added as a further modifying term to the E-W output. This latter correction is used for obtaining good corner geometry with flat-square tubes. A variable DC current is added to the parabola to effect a width control. Using a suitable power amplifier and a diode-modulator in the line output stage, the parabola may be used for E-W correction and dynamic width control. A further control is provided to shift the center point of the parabola up and down the screen (Parabola Tilt), to accommodate different CRTs. As with the vertical ramp output, an EHT correction is applied.

All of the vertical and horizontal signals are adjustable via 6-bit words from the MCU, and stored in latches. The adjustment controls available are:

Vertical Amplitude/Linearity/Breathing Correction
Parabola (E-W) Amplitude/Horizontal Amplitude/
Corner Correction, and Parabola Tilt

The Anode Current Sense at Pin 9 is also used as a beam current monitor. Two thresholds may be set, by the manufacturer, using external components. The first threshold sets a flag to the processor if beam current becomes excessive. The MCU could e.g. reduce brightness and/or contrast to alleviate the condition. The second threshold sets a flag warning of an overload condition where the CRT phosphor could be damaged. If such a condition were to arise, the processor would be programmed to shut down the PSU.

The vertical blanking period may be selected by means of a bit from the MCU to either 22 or 11 lines. The interlace may also be suppressed again under the control of the processor.

Vertical Countdown System

The MC44001 uses a countdown system to implement the vertical timebase function. Initially, the vertical timebase should reset to the Injection mode. This means that the timebase locks immediately to the first signal received, in exactly the same way as an old type injection locked timebase. A Coincidence Detector looks for counts of the right number (e.g., 625) and causes a 4-bit counter to count up. When there are 8 consecutive coincidences the vertical countdown is engaged, and the MSB of the counter is brought out to the set flag. Then the Auto Coundown mode should be set. Similarly, non-coincidences which will occur if synchronizing pulses are missing or in the wrong place, or if there is noise on the signals, cause the counter to count down. When the count goes back to zero, after 8 non-coincidences, the timebase automatically reverts to Injection Lock mode.

If it is known that lock will be lost (e.g., channel change), it is possible to jump straight into Injection Lock mode and not have to wait for the 8 consecutive non-coincidences. In this way the new channel will be captured rapidly. Once locked on to the new channel, "auto countdown" is then reselected by the MCU.

Under some conditions such as some VCRs in Search mode, it is possible to get signals having an incorrect number of lines, meaning that the countdown flag will go off because of successive non-coincidences. In these circumstances, if "auto countdown" is selected, the timebase will automatically lock to the signal in the Injection Lock mode. The fact that the flag is effectively saying that the vertical timebase is out of lock need not be a cause for major concern, since the horizontal timebase will still be locked to the signal, and has its own flag — "Horizontal out of lock". The vertical countdown and horizontal lock flags both perform an independent test for the presence of a valid signal. A logical OR function can be performed on the two flags, such that if either are present then by definition a valid signal is present.

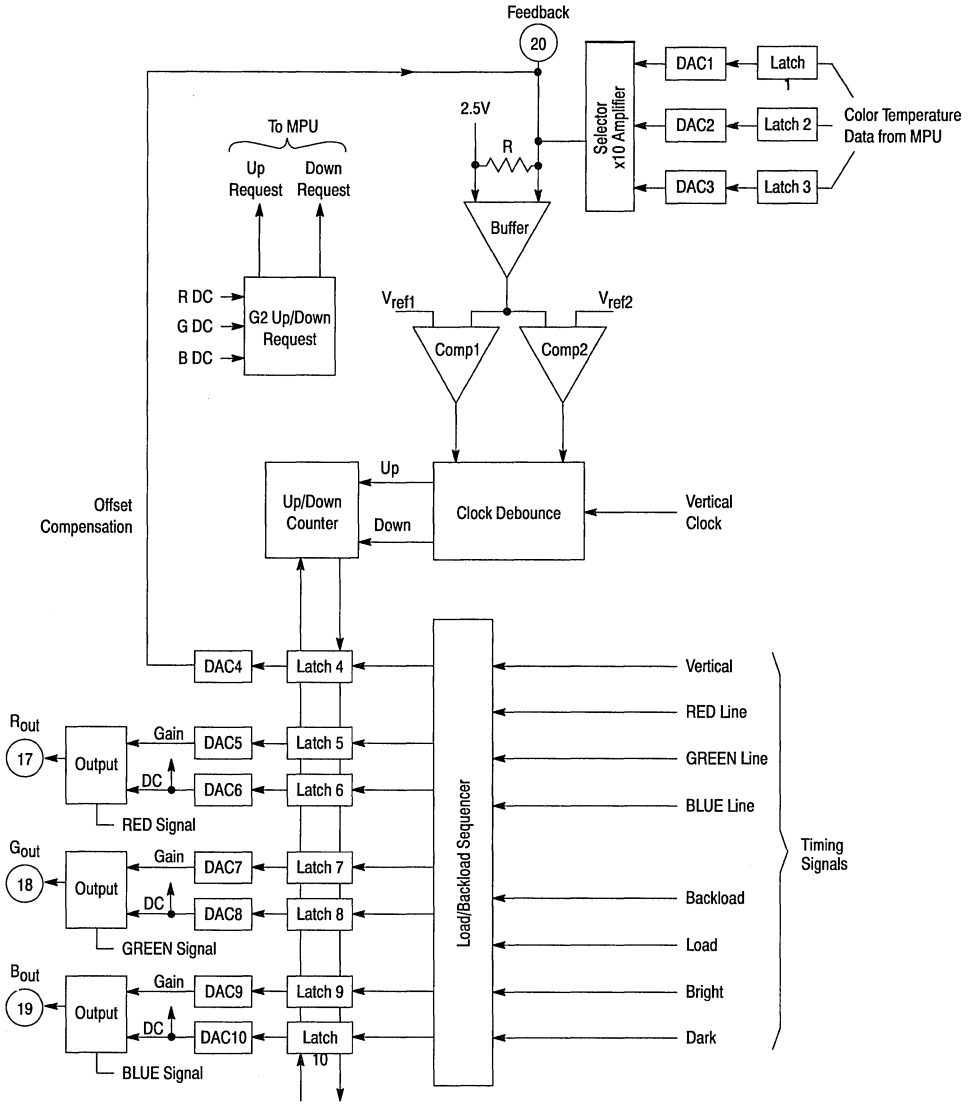
The vertical oscillator has end-stops set at two line-count decodes as given below:

$$50 \times 625 / 672 = 46.5 \text{ Hz (min)}$$
$$50 \times 625 / 512 = 61.0 \text{ Hz (max)}$$

These figures assume that the horizontal timebase is running at 15,625 Hz. When the vertical timebase is in Injection Lock mode the line counter reset is inhibited so that it ignores any sync pulses before a count of 512 is reached. This prevents any possible attempted synchronization in the middle of the picture. If the count reaches 672 lines then there is an automatic reset which effectively sets the lower frequency limit. The choice of these limits is a compromise between a wide window for rapid signal capture and a narrow window for good noise immunity.

It is also possible to run the timebase in 2V mode as there are decodes for 100 Hz (2 x 50 Hz) operation with upper and lower limits in proportion. This is, of course, intended to be used in conjunction with field and frame memory stores. The similar decodes which would be necessary to allow 120 Hz (2 x 60 Hz) operation have not, for the present, been implemented. Finally, the timebase can be forced into a count of either 625 or 525 by commands from the MCU; in this mode the input signal, if present, is ignored completely. If there is no signal present save for noise, then this feature can be used to obtain a stable raster.

Figure 7. Auto Gray Scale Control Loops



PIN FUNCTION AND EXTERNAL CIRCUIT REQUIREMENTS

The following section describes the purpose and function of each of the 40 pins on the MC44001. There is also an explanation of the external circuit component requirements for a practical application; a diagram of the small signal circuit will be found in Figure 10. One of the primary design aims for the MC44001 was to use the minimum number of external components, and where these are necessary to employ low cost and easily obtainable standard types. Thus for example, as all the video signal filtering is carried out on the IC there are no coils required whatsoever. The most common requirement is for AC coupling capacitors which are far too big to be integrated onto the chip. The time constants on certain pins are deliberately left as external components to facilitate testing and for fine tuning the performance.

ACC (Pin 1) – External filter used by ACC section. Normally a single 100 nF capacitor.

Video Inputs 1, 2 (Pin 2, 40) – Video inputs intended for a nominal 1.0 Vp-p input level of composite video. Separate Luma and Chroma components may also be used with these input pins. The external circuit requirement is for a series 100 nF and 1.0 kΩ. The input selection and adaptation for Y and C is carried out in software.

Figure 8. Horizontal Timebase

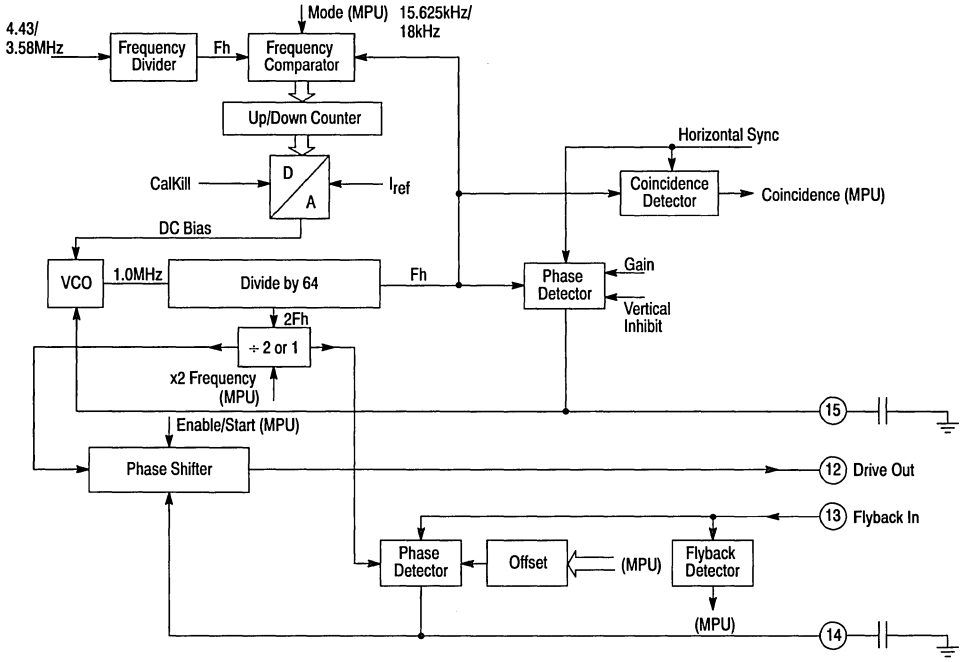
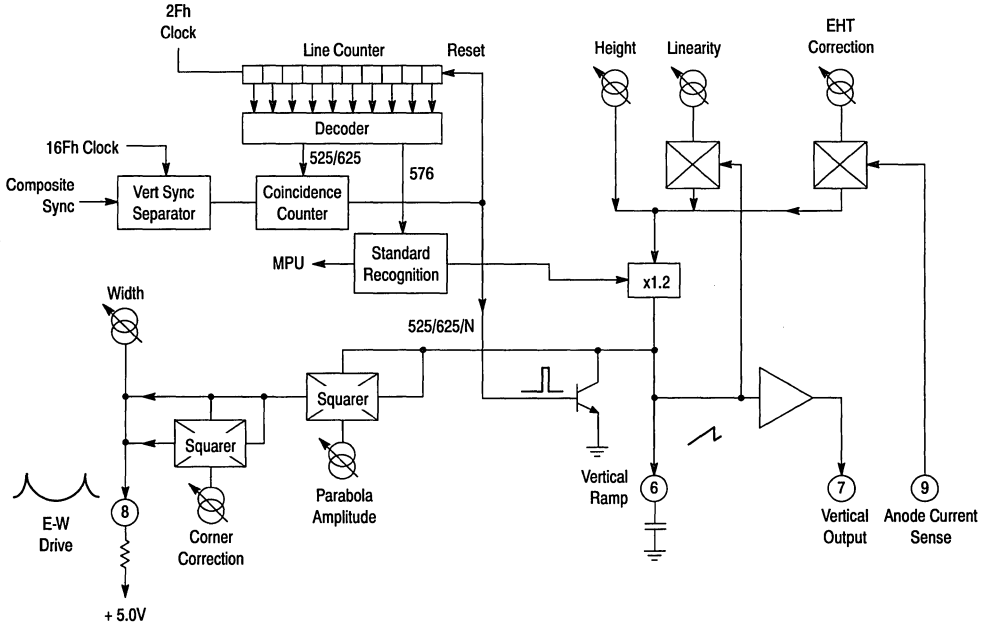


Figure 9. Vertical Timebase



Reference Current (Pin 3) – Master reference current used throughout the IC. This is programmed by means of an external pull-up resistor, as onboard resistors are not sufficiently accurate. The designated current is 70 µA. This pin should be very well decoupled to ground to avoid picking up interference from the nearby I²C bus inputs.

I²C Clock (Pin 4) – I²C bus clock input. This input can be taken straight into the IC, but in a real TV application it may be prudent to fit a series current limiting resistor nearby the pin in case of flashover.

I²C Data (Pin 5) – I²C data input. The comment above for Pin 4 also applies to this pin.

Vertical Ramp (Pin 6) – A current is used to charge an external capacitor connected to this pin, developing a voltage sawtooth with a field period.

Vertical Drive (Pin 7) – The sawtooth derived on Pin 6 is used to drive an external power amplifier vertical output stage. The amplitude and linearity of the output ramp are adjustable via the MCU.

Parabola (E-W) Drive (Pin 8) – A parabolic waveform derived by squaring the vertical ramp is used to drive an external power amplifier. In sets fitted with a diode modulator type line output stage, this provides Width Control and Pin Cushion Correction. The parabola is squared again to give a fourth order correction term required for flat square tubes. The E-W amplitude, DC level, Tilt and Corner Correction are all adjustable by means of the MCU. This is a current output and requires an external pull-up resistor to develop the voltage waveform.

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Anode Current (Pin 9) – Used as an anode current monitor whose purpose it is to: provide EHT compensation (antibreathing); and also warn of excessive and overload beam current conditions.

This pin is connected via 560 k series resistor to the bottom of the EHT overwinding. Thus increasing beam current will pull the voltage on this pin more negative. This change is sensed within the chip and used to apply a correction to the ramp and parabola amplitudes. With large beam currents, thresholds at +1 Vbe and – 2 Vbe set off warning flags to the MCU, which then has to take the appropriate action. The anode current levels at which these thresholds are reached are set up using fixed external resistors.

Grid 2 Control (Pin 10) – This consists of one of the MC44001 control registers which has been D/A converted and brought out from the IC as a current source. The current may be varied from 0 µA to 300 µA, and may be used for a number of auxiliary tasks, such as for Grid 2 control.

SECAM Calibration Loop (Pin 11) – A 100 nF capacitor on this pin is used for the SECAM Calibration Loop.

H-Drive (Pin 12) – Horizontal drive pulses having an approximately even mark-to-space ratio emerge from this pin. This is an open-collector output which can sink up to 10 mA. However, taking this much current is not recommended since there is no separate ground pin available which may be connected near the line O/P stage; noise could be injected into the signal ground on the IC. Therefore, with a transformer driven line output stage, this output has been designed to be used with an extra external transistor inverter between the IC and the line driver.

H-Flyback Input (Pin 13) – Flyback sensing input taken from the line output transformer. These pulses are used by the 2nd horizontal loop for H-phase control. A positive going pulse from 0 V to + 5.0 V amplitude is needed for correct operation. The internal impedance of the pin is about 50 kΩ. An external attenuating series resistor will also be needed.

H-Loop 2 Filter (Pin 14) – A simple external filter consisting of a 100 nF capacitor for the 2nd horizontal loop.

H-Loop 1 Filter (Pin 15) – Horizontal PLL loop time constant. The value of RC time constant is selected with external components to give a smooth recovery after the field interval disturbance.

Signal Ground (Pin 16)

R,G,B Outputs (Pin 17, 18, 19) – The R,G,B drives are current rather than voltage due to the limited headroom available with the 5.0 V supply line. The outputs themselves consist of open-collector transistors and these are used to drive the virtual ground point of the high voltage cathode amplifiers.

Feedback (Pin 20) – Current feedback sense derived from the video output amplifiers. The currents from all three guns are summed together as each is driven sequentially with known current pulses during the field interval. This feedback is then compared with internally set-up references. A low value ceramic capacitor to ground may be fitted close to this pin to help stabilize the control loops.

A secondary function of this pin is for peak beam current limiting. When the feedback voltage during picture time becomes too great (i.e., too high beam current), a threshold at V_{CC} + 2 Vbe is exceeded at which time a flag is sent to the MCU. The MCU then has to carry out the function of peak beam limiter by e.g. reducing contrast until the flag goes off. The threshold current is set externally with a fixed resistor value.

Fast Commutate (Pin 21) – A very fast active high switch (transition time 10 ns). Used with text on the R,G,B inputs, for overlaying text on picture. This hardware switch may be enabled and disabled in software.

R,G,B Inputs (Pins 22, 23, 24) – These external input signals are AC coupled into the IC via 100 nF capacitors and are clamped. The inputs have a 1.0 kΩ impedance and should be driven with 700 mVp-p signal levels.

Y2 Input (Pin 25) – Auxiliary external input to the MC44001. The pin has a 1.0 kΩ impedance and should be driven with 700 mVp-p of luminance signal. The signal must be AC coupled via an external 100 nF coupling capacitor, and is clamped internally.

B-Y and R-Y Inputs (Pin 26, 27) – Corrected color difference inputs from the MC44140. The signals are AC coupled to the MC44001 color difference section and are clamped. The input impedance is of the order of 1.0 kΩ.

Y1 Clamp (Pin 28) – External capacitor used by the circuit which clamps the Y1 signal output on Pin 29.

Y1 Output (Pin 29) – The luminance, after passing through the filter and delay line/peaking sections, is made available on this pin.

System Select (Pin 30) – A DC level output controlled in software. Used by the MC44140 for system selection.

Sandcastle (Pin 31) – A special timing pulse derived in the MC44001 for use by the MC44140.

Crystal (Pin 32, 33) – A 14.3 MHz crystal is required at Pin 32 for NTSC decoding, and a 17.7 MHz crystal is required at Pin 33 for PAL and SECAM decoding. Either crystal may be omitted if the application does not involve the associated signals. The appropriate crystal is selected by the MCU.

The crystals are parallel-driven, and require an external load capacitor of 20 pF to 30 pF. *Only crystals intended for VCO operation should be used.* The selected crystal's frequency is made available to the MC44140 by means of the external capacitor divider.

+ 5.0 V Supply (Pin 35) – Supply line, nominally + 5.0 V requiring about 120 mA. The actual voltage should be in the range of 4.75 V to 5.25 V for usable results. It is recommended to decouple the supply line using a small ceramic capacitor mounted close to the supply and ground pins.

Ground (Pin 34)

B-Y and R-Y Outputs (Pin 36, 37) – Demodulated color difference outputs. These signals are AC coupled to the MC44140 for correction and delay with PAL and SECAM, respectively. Signal levels up to a maximum of 1.0 Vp-p may be expected.

Ident (Pin 38) – External filter used by R-Y indent circuit. The filter normally consists of a single capacitor (47 nF) whose value is a compromise between rapid identification and noise rejection.

OSC Loop Filter (Pin 39) – External time constant for chroma PLL. The crystal reference oscillator is phase-locked to the incoming burst in PAL and NTSC. A low value ceramic capacitor, for good noise immunity, is normally placed in parallel with a much longer RC time constant. The PLL pull-in range is reduced when the time constant on the pin is made bigger; allowing this function to be optimized by the user.

CONTROL FUNCTIONS

General Description

As already related in the circuit description, the MC44001 has a memory of 18 bytes. All, except Sub-address 77 and 7F, use the 6 least significant bits (64 steps) as an analog control register with D/A converters within the memory section. The remaining bits are controlled individually for switching of numerous functions. Table 1 gives a listing of all the memory registers and control bits. An explanation of the function of the 16 analog control registers is given below.

Vertical Amplitude – Changes the amplitude of the vertical ramp available on Pin 7.

Vertical Breathing Correction – A correction is applied to the vertical ramp amplitude in a sense opposite to the picture expansion and contraction produced by changes in beam current. This register alters the sensitivity of the beam current sensing and hence the size of correction applied for a given change in beam current.

Parabola Amplitude – Changes the amplitude of the E-W output parabola developed across an external pull-up resistor at Pin 8.

Parabola Tilt – Shifts the point of inflection of the E-W parabola from side to side along the time axis. Also known as *keystone correction.*

Vertical Linearity – The vertical ramp is multiplied by itself to give a squared term, a part of which is either added or subtracted to the linear ramp as determined by this register.

Corner Correction – An independent 4th order term which is subtracted from the E-W parabola to achieve correct geometry with flat square tubes.

Horizontal Amplitude – A variable DC offset applied to the E-W output parabola on Pin 8.

D/A Output – A variable DC current output which may be used to drive auxiliary external circuitry under I^2C bus control.

Horizontal Phase Control – Applies a variable phase offset to the horizontal drive pulse at Pin 15 providing for a picture centering control.

B, G, R Temperature – These controls set up the current reference pulses used when sampling the beam current during field interval. The data is fixed by the TV manufacturer when setting up the CRT for correct Gray Scale tracking.

(All the above registers are for use during the test and setting up procedures; the remaining 4 registers are also user controls.)

Contrast – During bright sample time during the field interval this control varies the level of the current pulses injected into the R,G,B channels, so altering the picture contrast.

Brightness – A variable current pedestal which is added to the three drives during active picture time.

Saturation – A variable gain control for the two color difference signals (0 to 140%). There are two such controls within the MC44001, and this control acts on them both.

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Hue – Achieved by mixing a proportion of one color difference signal into the other.

Individually Adjustable Control Bits – These consist of all Sub-address 77 and bits 6 and 7 of Sub-addresses 78 to 88. Some of these are used individually to control single functions requiring just on/off switching; and some are arranged into 2 or 3-bit words (e.g., luma peaking). A list of control words and truth tables for these may be found in Table 2.

CA1, CB1 – Used to change the mode of operation of the vertical timebase to either injection lock or auto countdown, or to force it into 525 or 625 lines. Just prior to changing channel, the vertical timebase can be switched to injection lock mode and when a new channel is captured, the timebase is switched back to auto mode. In this way there is no delay in locking onto the new channel and hence no picture roll. If there is no valid signal being received the display can be stabilized by forcing the timebase into 525 or 625 lines.

IC1, IF1 – These bits are used to suppress the field interlace, which can be scanned in the nearest even or odd half line.

$\overline{H1}$, $\overline{V1}$ – Selects the type of SECAM ident when operating in this mode. Either vertical ident bursts or back porch ident can be selected individually, or ident can be taken from a combination of the two.

SSA, SSB, SSC – Used to set the DC level of the System Select output from the MC44001, Pin 30. This output is used by the MC44140 delay line in turn for changing between PAL, NTSC, SECAM and external modes of operation. In effect the MC44140 is being controlled by the I²C bus via the MC44001.

Figure 10. Basic Small Signal Circuit

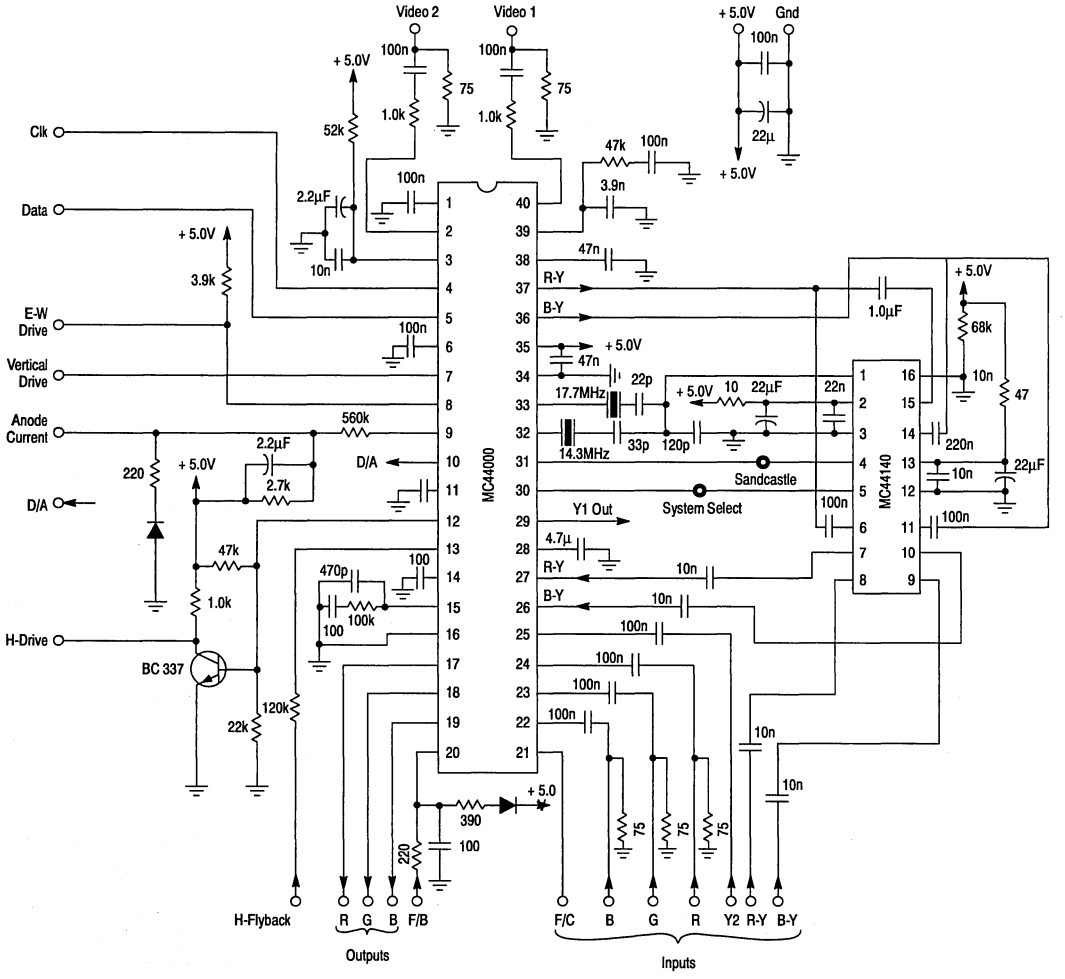


Table 1. Control Data

HEX Sub-address	MSB	Data Byte						LSB
77	S-VHS Y	S-VHS C	FSI	BAI	ICI	IFI	CBI	CAI
78	INTSEL	CALKILL	Vertical Amplitude					
79	HI	VI	Vertical Breathing Correction					
7A	XS	SSD	Parabola Amplitude					
7B	T1	T2	Parabola Tilt					
7C	SSC	SSA	Vertical Linearity					
7D	P1	SSB	Corner Correction					
7E	P3	P2	Horizontal Amplitude					
7F	D3	D1	Reserved					
80	D EN	D2	D/A Output					
81	Y2 EN	Y1 EN	Horizontal Phase Control					
82	TEST	YX EN	Blue Temperature					
83	Not Used	VCR	Green Temperature					
84	FILT	NORM	Red Temperature					
85	BRI EN	2x Fh	Contrast					
86	SSE	H EN	Brightness					
87	SS1	SAT2 EN	Saturation					
88	V1/V2	SS2	Hue					
00		Dummy – If H EN, then starts H timebase						
FF		Dummy – Resets peak beam limit flag						

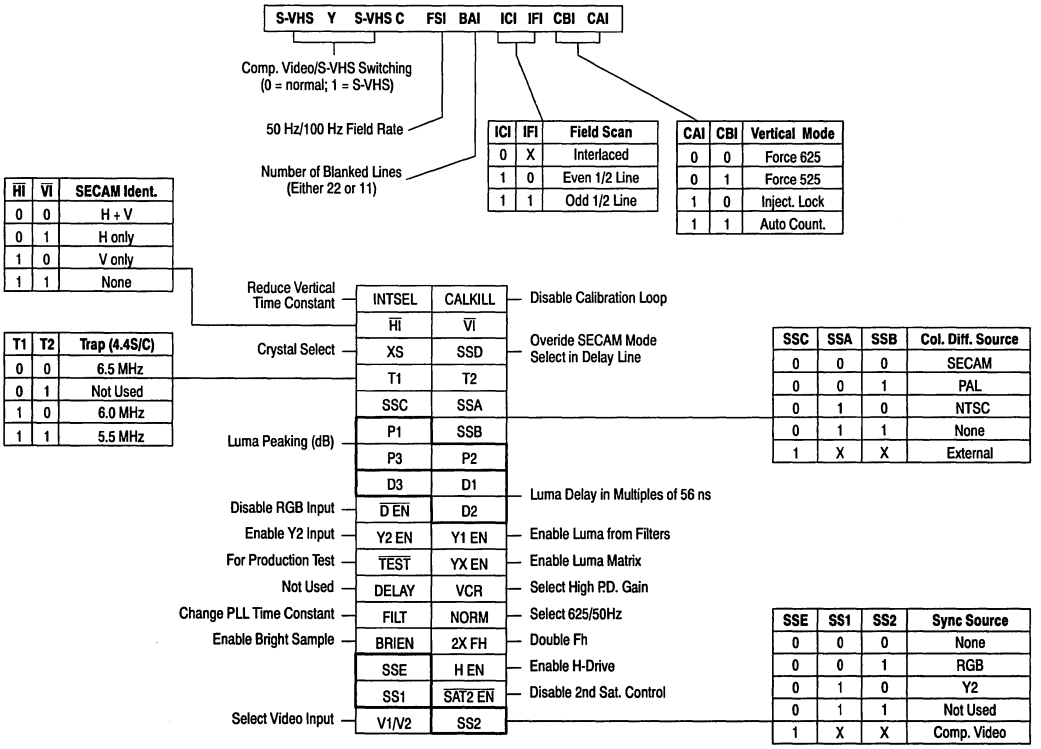


Table 2. Control Bit Truth Tables

CAI	CBI	Sync Mode
0	0	Force 625
0	1	Force 525
1	0	Injection Lock
1	1	Auto Countdown

ICI	IFI	Field Scan
0	X	Interlaced
1	0	Even Up 1/2 Line
1	1	Odd Up 1/2 Line

$\overline{HI}$	$\overline{VI}$	SECAM Ident.
0	0	H + V
0	1	H only
1	0	V only
1	1	None

T1	T2	Trap*
0	0	6.5 MHz
0	1	Not Used
1	0	6.0 MHz
1	1	5.5 MHz

SSC	SSA	SSB	Col. Diff. Source
0	0	0	SECAM
0	0	1	PAL
0	1	0	NTSC
0	1	1	None
1	X	X	External

SSE	SS1	SS2	Sync Source
0	0	0	None
0	0	1	RGB
0	1	0	Y2
0	1	1	Not Used
1	X	X	Comp. Video

P2	P1	P3	Luma Peak (dB) @ 3.0 MHz *
0	0	0	8.5
0	0	1	8.0
0	1	0	7.2
0	1	1	6.3
1	0	0	5.4
1	0	1	3.8
1	1	0	2.3
1	1	1	0.0

D1	D2	D3	Approx. Luma Delay (ns)*
0	0	0	525
0	0	1	581
0	1	0	637
0	1	1	693
1	0	0	749
1	0	1	805
1	1	0	749
1	1	1	805

*Values given with 17.7 MHz crystal selected. Frequencies and delay step size change proportionately when the 14.3 MHz crystal is selected.

SSE, SS1, SS2 – These 3 bits select the signal input from which the timebase synchronization is taken. The composite video input has a high quality sync separator which has been designed to cope with noise and interference on the video; the RGB and Y2 inputs have simple single sync separators which may also be used for synchronization.

T1, T2 – To select the center frequency of the sound trap. Either 5.5 MHz, 6.0 MHz, or 6.5 MHz center frequencies are available.

P1, P2, P3 – These 3 bits are used to adjust the luma peaking value.

D1, D2, D3 – These 3 bits are used to adjust the luma delay value.

The remaining control bits are used singularly and are listed as follows:

S-VHS Y – Selects between luminance from chroma trap/peaking section, and separate luminance which bypasses this filter section.

S-VHS C – In one mode selects chrominance from the takeoff filter which forms part of the luma delay line. The other mode accepts separate chrominance directly for the input.

FSI – Selects either 50 Hz or 100 Hz field rate. When bit is low 50 Hz operation is selected. Not usable with NTSC.

BAI – Either 22 or 11 lines may be blanked using this bit.

INTSEL – The vertical sync separator operates by starting a counter counting up at the beginning of each sync pulse, a field pulse being recognized only if the counter counts up to a sufficiently high value. The control bit INTSEL is used in taking the decision as to when a vertical sync pulse has been detected. When low, the pulse is detected after 8.0 µs; when high after 24 µs. This may find application with anti-copy techniques used with some VCRs, which rely on a modified or corrupted field sync to allow a TV with a short time constant to display a stable picture. However, a VCR having a longer time constant will be unable to lock to the vertical.

CALKILL – Enables or disables the horizontal calibration loop. The loop may be disabled so long as the horizontal timebase is locked to an incoming signal.

XS – Is used to change between the two external crystal positions (Pins 32 and 33).

SSD – Can be used to override SECAM mode in the delay line. When low, SECAM mode is enabled.

$\overline{\text{D EN}}$ – Enables or disables the RGB Fast Commutation switch for the RGB inputs. When low, RGB inputs are enabled.

Y1 EN – Switches Y1 through to the color difference stage.

Y2 EN – Switches Y2 through to the color difference stage.

$\overline{\text{Test}}$ – When bit is low, enables continuous sampling by the RGB output control loops throughout the entire field period. Used only for testing the IC.

YX EN – Enables the luma matrix when the 2nd saturation control is selected. Used in conjunction with SAT2 EN.

VCR – Is used to change the gain of the horizontal phase detector, e.g., when locking onto a new channel and operation with VCR.

FILT – Controls the time constant of the horizontal PLL. The long time constant is useful for VCR or other non-broadcast quality signals.

Norm – Alters the division ratio for the reference frequency used by the horizontal calibration loop. Always used when changing between 14.3 MHz and 17.7 MHz crystals.

BRI EN – Used to switch on or off the "bright" sampling pulses used by the RGB output loops. This feature was originally introduced to prevent any backscatter from these three bright lines in the field interval from getting into the picture. Must be enabled when adjusting to any of Contrast or Red, Green and Blue color temperatures.

2x Fh – Line drive output is either standard 15.625 kHz (15.750 kHz) or at double this rate.

H EN – Control bit enables horizontal drive pulse. This is normally done automatically after the values stored in the MCU nonvolatile memory have been read into the MC44001 memory.

SAT2 EN – When low enables operation of 2nd saturation control. Used in conjunction with YX EN.

V1/V2 – To select between Video Inputs 1 and 2.

Table 3. Control Bit Functions

Bits	Bit Low	Bit High
V1/V2	Video I/P 2 Selected	Video I/P 1 Selected
SAT2 EN	Second SAT Control Enabled	Second SAT Control Disabled
H EN	H-Drive Enabled	H-Drive Disabled
2x FH	H-Drive: 1X Fh	H-Drive: 2x Fh
BRI EN	"Bright" Sample Switched Off	"Bright" Sample Switched On
Norm	625/50 Hz	525/60 Hz
FILT	H Phase Detector Short Time Constant	H Phase Detector Long Time Constant
VCR	Low H Phase Detector Gain	High H Phase Detector Gain
YX EN	Disable Luma Matrix (2nd SAT Control)	Enable Luma Matrix (2nd SAT Control)
Test	Video O/Ps Sampled Continuously	Video O/Ps Sampled Once Per Field
Y1 EN	Luma From Filters Switched Off	Luma From Filters Switched On
Y2 EN	EXT Luma Input Switched Off	EXT Luma Input Switched On
D EN	RGB Inputs Enabled	RGB Inputs Disabled
SSD	SECAM Mode Select Enabled	SECAM Mode Select Disabled
XS	Pin 33 Crystal Selected	Pin 32 Crystal Selected
CALKILL	H Calibration Loop Enabled	H Calibration Loop Disabled
INTSEL	Fast Vertical Time Constant Selected	Slow Vertical Time Constant Selected
BAI	22 Blanked Lines Selected	11 Blanked Lines Selected
FSI	50 Hz Field Rate Selected	100 Hz Field Rate Selected
S-VHS C	Chroma From Take Off Filter Selected	Direct Chroma From I/P Selected
S-VHS Y	Luma From Notch/Peak Delay Selected	Luma By Passing Notch/Peak Delay

FLAGS RETURNED BY THE MC44001

When the Address Read/Write bit is high the last two bytes of I^2C data are read by the MCU as status flags; a listing of these may be found in Table 4. The MC44001 is designed to be part of a closed-loop system with the MCU; these flags are the feedback mechanism which allow the MCU to interact with the MC44001.

A brief description of each of the flags, its significance and possible uses are given below.

Table 4. Flags Returned

Clock #	Flag (Bit High)
10	Horizontal Flyback Present
11	Horizontal Drive Enabled
12	Horizontal Out Of Lock
13	Excess Average Beam Current
14	Less Than 576 Lines
15	Vertical Countdown Engaged
16	Overload Average Beam Current
17	Reserved
18	(Acknowledge)
19	Grid 2 Voltage Up Request
20	Grid 2 Voltage Down Request
21	OK
22	Fault
23	ACC Active
24	PAL Identified
25	SECAM Identified
26	Excess Peak Beam Current
27	(Acknowledge)

Horizontal Flyback Present – A sense of the horizontal flyback is taken via a current limiting series resistor from one of the flyback transformer secondaries to Pin 13. This is used for the H-phase shift control, but the presence of the pulse is also flagged to the MCU. Should the flag be missing after the chassis has been started up then the MCU would have to shut down the set immediately.

Horizontal Drive Enabled – Indicates that the horizontal drive pulse output at Pin 15 has been enabled. This occurs after the stored values in the nonvolatile memory have been transferred to the MC44001 memory.

Horizontal Out of Lock – This flag is high when no valid signal is being received by the MC44001. Possible action in this case would be to change the phase detector gain and time constant bits to ensure rapid capture and locking to a new signal.

Excess Average Beam Current – Is one of two conditions whose threshold levels are determined by an external component network connected to beam current sensing Pin 9. This condition indicates an excess beam current as compared to the manufacturer's set maximum level during normal usage. A typical response to this warning indicator would be for the MCU to reduce the brightness and/or contrast.

Less Than 576 Lines – Output from the line counter in the vertical timebase. If there is a count of less than 576 this is indicative of a 525 line system being received. If the flag is low then a 625 line system is being received. This information can be used as a part of an automatic system selection software.

Vertical Countdown Engaged – The vertical timebase is based on a countdown system. The timebase starts in Injection Lock mode and when vertical retrace is initiated a 4-bit counter is set to zero. A coincidence detector looks for counts of 625 lines. In Auto mode each coincidence causes the counter to count up. When eight consecutive coincidences are detected the countdown is engaged. The MSB of the counter is used to set this flag to the processor.

Overload Average Beam Current – This is the second threshold level which is set by the external component network on Pin 9. The flag warns of an overload in anode current which could damage the CRT if allowed to continue. Appropriate action in this case is therefore to shut down the set.

Grid 2 Voltage Up/Down Requests – These flags indicate when the RGB output loops are about to go out of the control range necessary for correct gray scale tracking.

OK and Fault – These two flags are included as a check on the communication line between the MCU and MC44001. The OK flag is permanently wired high and Fault is permanently wired low. The MCU can use these flags to verify that the data received is valid.

ACC Active – This flag is high when there is a sufficient level of burst present in PAL and NTSC modes during the video back porch period. The flag goes low when the level of burst falls below a set threshold or if the signal becomes too noisy. The flag is used to implement a software color killer in PAL and NTSC and is also available for system identification purposes. Since in SECAM there is line carrier present during the gating period, it is quite likely that the ACC will be on, or will flicker on and off in this mode.

*** PAL Identified** – Recognizes the line-by-line swinging phase characteristic of the PAL burst. When this flag is on together with the ACC flag, this is positive identification for a PAL signal.

*** SECAM Identified** – Senses the changing line-by-line reference frequencies (Fo1 and Fo2) present during the back porch period of the SECAM signal. This flag alone provides identification that SECAM is being received.

* These two flags are set in opposition to one another such that they can never both be on at the same time. This has been done to try to prevent misidentification from occurring. Often it is very difficult to distinguish between PAL and SECAM especially when broadcast material has been transcoded, sometimes badly, leaving e.g. large amounts of SECAM carrier in a transcoded PAL signal (also often with noise). With this method the strongest influence will win out making a misidentification much less likely.

Excess Peak Beam Current – A voltage threshold is set on the beam current feedback on Pin 20, which is also used for the RGB output loops for current sampling. When the threshold is reached the flag is set, indicating too high a peak beam current which may be in only a part of the screen. The response of the MCU might be to reduce the contrast of the picture. This flag together with the excess average beam flag already described perform the function of beam limiting. The exact way in which this is handled is left to the discretion of the user who will have their own requirements, which may be incorporated by the way in which the software is written.

READING AND WRITING TO THE MC44001

Flag reading may be done at any time during a field. However, writing to the MC44001 must be restricted to certain times. If writing of new data is done during the middle of a field, a disturbance will be seen on the screen, particularly for the four user controls. While writing during the vertical interval may appear to be the obvious solution for this, there is a limited time available due to the contrast control function which is carried out with RGB sampling loops during this interval. Writing during this particular time can cause the sampling loops to become unstable.

The time available for writing new data is approximately 1.2 ms from the beginning of the field flyback pulse to the beginning of the RGB sampling. It is only the third byte (data byte) which is restricted to this time interval. The first two bytes may be sent previous to this, or also during this time.

Table 5. System Identification

Flags From Chroma 4				Crystal (MHz)	Standard Selected By MCU
<576 Lines	ACC On	PAL	SECAM		
0	0	0	0	17.7	Kill
0	0	0	1	17.7	SECAM
0	0	1	0	17.7	Kill
0	0	1	1	17.7	I²C Bus Error
0	1	0	0	17.7	Kill
0	1	0	1	17.7	SECAM
0	1	1	0	17.7	PAL
0	1	1	1	17.7	I²C Bus Error
1	0	0	0	14.3	Kill
1	0	0	1	14.3	Kill
1	0	1	0	14.3	Kill
1	0	1	1	14.3	I²C Bus Error
1	1	0	0	14.3	NTSC
1	1	0	1	14.3	NTSC
1	1	1	0	14.3	NTSC
1	1	1	1	14.3	I²C Bus Error

NOTES: 1. The table above can be used for color standard selection between the normal PAL (I, BG), SECAM (L, BG) and NTSC (3.58 MHz – M) Standards. To detect the hybrid VCR standard (525 lines with 4.4 MHz chrominance) would entail switching back to the 17.7 MHz crystal in the event of there being no flags present with the 14.3 MHz crystal.

2. Chroma 4 could also be used for the PAL M & N Standards that are used in some parts of South America, but because the subcarrier frequencies used differ by some kHz from the normal, crystals with a different center frequency would be required.

Table 6. Mode Definitions

Mode Selected	Control Bits				
	XS*	NORM*	SSA	SSB	SSC
Kill (17.7 MHz)	0	0	1	1	0
Kill (14.3 MHz)	1	1	1	1	0
PAL (I, BG)	0	0	0	1	0
SECAM	0	0	0	0	0
NTSC (M)	1	1	1	0	0

*Control bits XS and NORM are always changed together.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC44011

BUS CONTROLLED MULTISTANDARD VIDEO PROCESSOR

SILICON MONOLITHIC INTEGRATED CIRCUIT

Advance Information

Bus Controlled Multistandard Video Processor

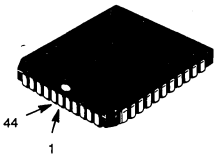
The Motorola MC44011, a member of the MC44000 Chroma 4 family, is designed to provide RGB or YUV outputs from a variety of inputs. The inputs can be composite video (two inputs), S-VHS, RGB, and color difference (R-Y, B-Y). The composite video can be PAL and/or NTSC as the MC44011 is capable of decoding both systems. Additionally, R-Y and B-Y outputs and inputs are provided for use with a delay line where needed. Sync separators are provided at all video inputs.

In addition, the MC44011 provides a sampling clock output for use by a subsequent triple A/D converter system which digitizes the RGB/YUV outputs. The sampling clock (6.0 to 40 MHz) is phase-locked to the horizontal frequency.

Additional outputs include composite sync, vertical sync, field identification, luma, burst gate, and horizontal frequency.

Control of the MC44011, and reading of status flags, is via an I^2C bus.

- Accepts NTSC and PAL Composite Video, S-VHS, RGB, and R-Y, B-Y
- Includes Luma and Chroma Filters, Luma Delay Lines, and Sound Traps
- Digitally Controlled via I^2C Bus
- R-Y, B-Y Inputs for Alternate Signal Source
- Line-Locked Sampling Clock for A/D Converters
- Burst Gate, Composite Sync, Vertical Sync and Field Identification Outputs
- RGB/YUV Outputs can provide 3.0 V_{p-p} for A/D Inputs
- Overlay Capability
- Single Power Supply: + 5.0 V, ± 5%, 550 mW (Typical)
- 44 Pin PLCC Package



FN SUFFIX
PLASTIC PACKAGE
CASE 777
(PLCC)

ORDERING INFORMATION

Device	Temperature Range	Package
MC44011FN	0° to + 70°C	PLCC-44

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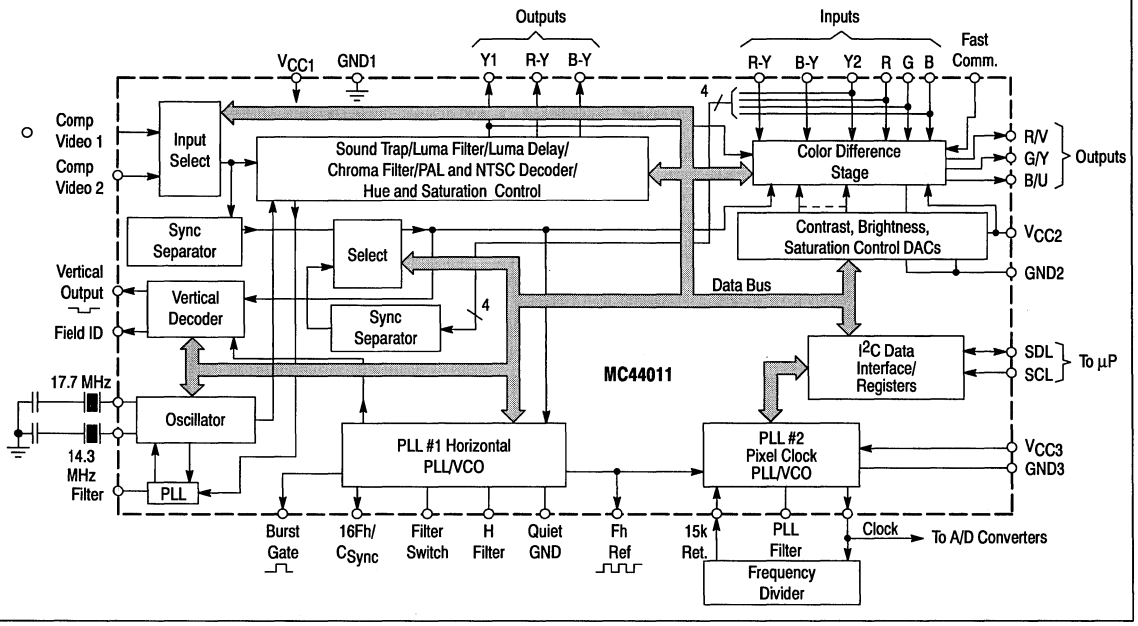
Simplified Block Diagram



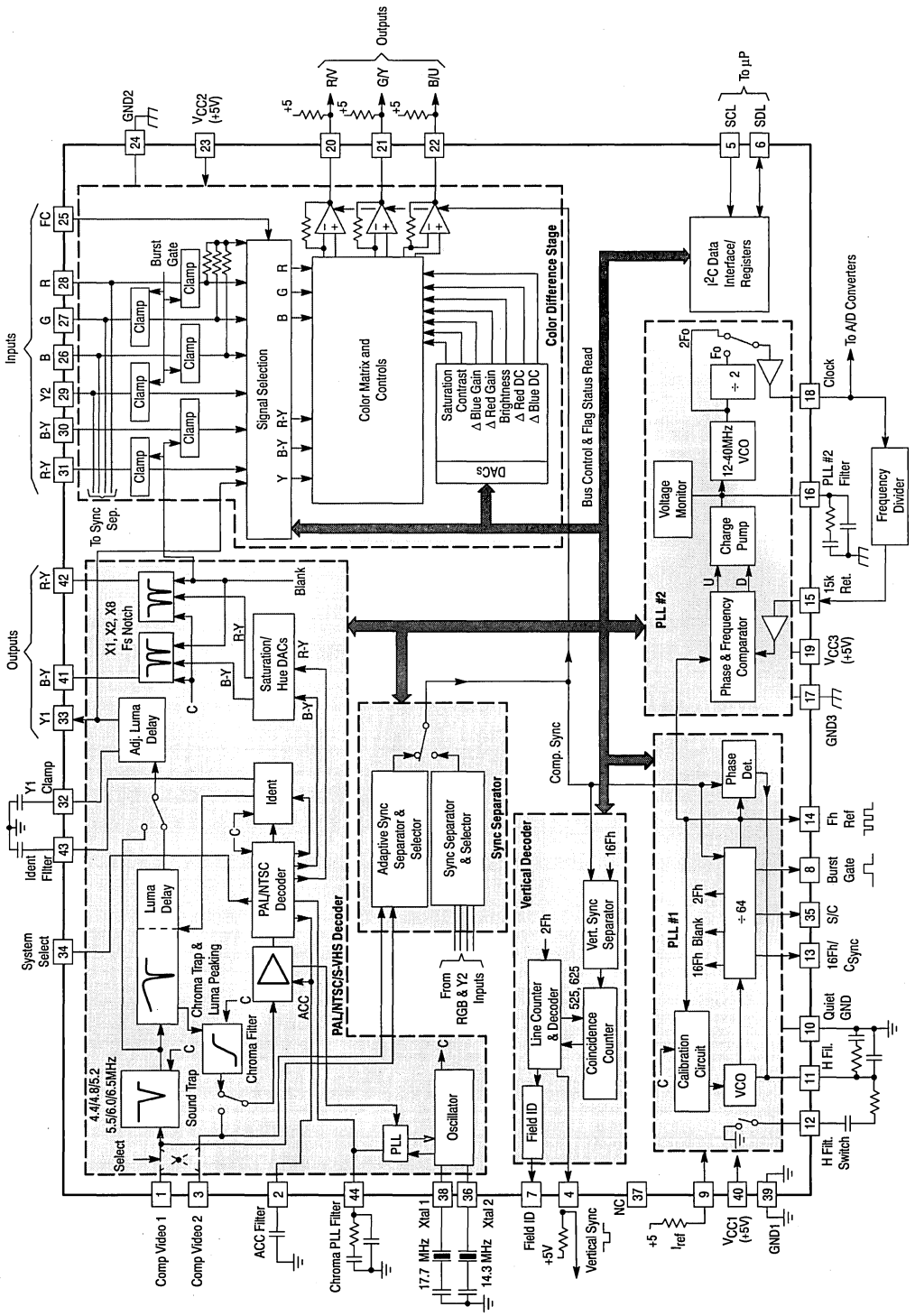


Figure 1. MC44011 Block Diagram

ELECTRICAL CHARACTERISTICS (The tested electrical characteristics are based on the conditions shown in Table 1 and 2. Composite Video input signal = 1.0 V_{p-p}, composed of: 0.7 V_{p-p} Black-to-White; 0.3 V_{p-p} Sync-to-Black; 0.3 V_{p-p} Color Burst. $V_{CC1} = V_{CC2} = V_{CC3} = +5.0$ V, $I_{ref} = 32$ µA (Pin 9), unless otherwise noted.)

Table 1. Control Bit Test Settings

Control Bit	Name	Value	Function
$77-7	S-VHS-Y	0	Composite Video input selected.
$77-6	S-VHS-C	0	Composite Video input selected.
$77-5	FSI	0	50 Hz Field Rate selected.
$77-4	$\overline{\text{L2 GATE}}$	0	PLL #2 Gating enabled.
$77-3	$\overline{\text{BLCP}}$	0	Clamp Pulse Gating enabled.
$77-2	$\overline{\text{L1 GATE}}$	0	Vertical Gating enabled.
$77-1, 0	CB1, CA1	1,1	Vertical section Auto-Countdown mode
$78-7	36/68 µs	0	Time from beginning of Line 4 to Vertical Sync is 36 µs.
$78-6	CalKill	0	Horizontal Calibration Loop enabled.
$79-7, 6	HI, VI	1,1	Normal
$7A-7	Xtal	→	0 = 17.7 MHz crystal selected, 1 = 14.3 MHz crystal selected.
$7A-6	SSD	0	Normal
$7B-7, 6	T1, T2	1,1	Sound Trap Notch filter set to 5.5 MHz (with 17.7 MHz crystal).
$7C-7	SSC	0	Permits PAL and NTSC selection.
$7C-6, $7D-6	SSA, SSB	→	0, 1 = PAL decoding, 1,0 = NTSC decoding
$7D-7, $7E-7, 6	P1, P3, P2	1, 1, 1	Sets Luma Peaking at 0 dB.
$7F-7, 6, $80-6	D3, D1, D2	0, 0, 0	Set Luma Delay to minimum
$80-7	$\overline{\text{RGB EN}}$	0	Fast Commutate input can enable RGB inputs.
$81-7	Y2 EN	0	Y2 input (Pin 29) deselected
$81-6	Y1 EN	1	Y1 luma path from PAL/NTSC decoder selected.
$82-7	YUV EN	0	RGB output mode selected
$82-6	YX EN	0	Disable luma matrix from RGB inputs.
$83-7	L2 Gain	0	Set PLL #2 Phase/Frequency detector gain high.
$83-6	L1 Gain	1	Set PLL #1 Phase Detector gain high.
$84-7	H Switch	0	Set Horizontal Phase Detector filter switch open.
$84-6	525/625	→	0= 625 lines (PAL), 1 = 525 lines (NTSC)
$85-7	$F_{osc} \div 2$	0	Select direct VCO output from PLL #2.
$85-6	C_{Sync}	0	16 Fh output selected at Pin 13.
$86-7	V_{in} Sync	1	Composite Video inputs (Pin 1 or 3) Sync Source selected.
$86-6	H EN	0	Enabled Horizontal Timebase.
$87-7	Y2 Sync	0	Y2 sync source not selected.
$88-7	V2/V1	1	Select Video 1 input (Pin 1).
$88-6	RGB Sync	0	RGB inputs Sync Source not selected.

Table 2. DAC Test Settings

DAC	Value	Function	DAC	Value	Function
$78	32	R-Y/B-Y Gain	$82	32	Red Contrast Trim
$79	32	Sub Carrier Phase	$83	32	Blue Brightness Trim
$7D	00	Blue Output DC Bias	$84	32	Main Brightness
$7E	00	Red Output DC Bias	$85	32	Red Brightness Trim
$7F	63	Pixel Clock VCO Gain	$86	32	Saturation (Color Diff.)
$80	32	Blue Contrast Trim	$87	16	Saturation (Decoder)
$81	32	Main Contrast	$88	32	Hue

Currents out of a pin are designated –, and those into a pin are designated +.

MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Power Supply Voltage	V_{CC1} V_{CC2} V_{CC3}	− 0.5 to + 6.0 − 0.5 to + 6.0 − 0.5 to + 6.0	Vdc
Power Supply Difference (Between any two V_{CC} pins)		± 0.5	Vdc
Input Voltage: Video 1, 2, SCL, SDL 15 kHz Return R-Y, B-Y, Y2, RGB, FC	V_{in}	− 0.5, V_{CC1} + 0.5 − 0.5, V_{CC3} + 0.5 − 0.5, V_{CC2} + 0.5	Vdc
Junction Temperature (Storage and Operating)	T_J	− 65 to +150	°C

Devices should not be operated at these limits. The "Recommended Operating Conditions" table provides for actual device operation.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	$V_{CC1, 2, 3}$	+ 4.75	+ 5.0	+ 5.25	Vdc
Power Supply Difference (Between any two V_{CC} pins)	ΔV_{CC}	− 0.5	0	+ 0.5	Vdc
Input Voltage: Video 1, 2 (Sync-White)	V_{in}	0.7	1.0	1.4	V_{p-p}
Chroma (S-VHS Mode)		—	—	1.2	
Y2		0.7	1.0	1.4	
RGB		0.5	0.7	1.0	
R-Y, B-Y (Pins 30, 31)		0	—	1.8	
15 kHz Return		0	—	V_{CC3}	Vdc
SCL, SDL		0	—	V_{CC1}	
FC		0	—	V_{CC2}	
Burst Signal		30	280	560	mVp-p
Sync Amplitude		60	300	V_{CC1}	mVp-p
Output Load Impedance to Ground: RGB (Pull-up = 390 Ω)	RL_{RGB}	1.0	—	∞	kΩ
B-Y, R-Y	RL_{CD}	10	—	∞	
Y1	RL_{Y1}	1.0	—	∞	
Pull-up Resistance at Vertical Sync (Pin 4)	R_{VS}	1.0	10	—	kΩ
Source Impedance: Video 1, 2		0	—	1.0	kΩ
Pins 26 to 31		0	—	1.0	
Pixel Clock Frequency (Pin 18, see PLL #2 Electrical Characteristic)	f_{px}	—	2.0 to 45	—	MHz
15 kHz Return Pulse Width (Low Time)	PW_{15k}	0.2	—	45	µs
I^2C Clock Frequency	f_{I^2C}	—	—	100	kHz
Reference Current (Pin 9)	I_{ref}	—	32	—	µA
Operating Ambient Temperature	T_A	0	—	70	°C

All limits are not necessarily functional concurrently.

ELECTRICAL CHARACTERISTICS (T_A = + 25°C, V_{CC1} = V_{CC2} = V_{CC3} = 5.0 V, unless otherwise noted.)

Parameter		Min	Typ	Max	Unit
POWER SUPPLIES					
Power Supply Current (V_{CC} = + 5.0 V)	Pin 40	75	95	115	mA
	Pin 23	6.0	9.0	12	
	Pin 19	3.5	6.0	8.0	
	Total	85	110	135	

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ELECTRICAL CHARACTERISTICS (T_A = + 25°C, V_{CC1} = V_{CC2} = V_{CC3} = 5.0 V, unless otherwise noted.)

Parameter	Min	Typ	Max	Unit
PAL/NTSC/S-VHS DECODER				
Video 1, 2 Inputs				
Crosstalk Rejection, f = 1.0 MHz (Measured at Y1 output, Luma Peaking = 0 dB, $77-7 = 1)	20	40	—	dB
DC Level: @ Selected Input	—	2.8	—	Vdc
@ Unselected Input	—	0.7	—	
Clamp Current	– 30	– 20	–10	µA
Sound Trap Rejection (See Figures 14 to 23)				
With 17.7 MHz Crystal: @ 6.5 MHz (T1, T2 = 00)	15	30	—	dB
@ 6.0 MHz (T1, T2 = 10)	15	30	—	
@ 5.5 MHz (T1, T2 = 11)	10	43	—	
@ 5.74 MHz (T1, T2 = 01)	15	26	—	
With 14.3 MHz Crystal: @ 4.44 MHz (T1, T2 = 11)	—	35	—	
R-Y, B-Y Outputs (Pins 41, 42)				
Output Amplitude (with 100% Saturated Color Bars)				
Saturation (DAC 87) = 00	—	<1.0	—	mVp-p
Saturation (DAC 87) = 16	—	1.6	—	Vp-p
Saturation (DAC 87) = 63	1.5	1.8	—	
DC Level During Blanking	—	2.4	—	Vdc
Hue Control – Minimum Phase (DAC 88 = 00)	– 30	—	—	Deg
– Maximum Phase (DAC 88 = 63)	+ 30	—	—	
Nominal Saturation (with respect to Y1 Output, Note 1)	—	100	—	%
B-Y/R-Y Ratio: Balance (DAC 78) = 63	1.35	1.69	2.06	V/V
Balance (DAC 78) = 32	0.98	1.27	1.58	
Balance (DAC 78) = 00	0.60	0.77	0.96	
Output Amplitude Variation as Burst is varied from 80 mVp-p to 600 mVp-p	—	3.0	—	dB
Color Kill Attenuation ($7C-7, 6 and $7D-6 = 011)	—	40	—	dB
Crosstalk with respect to Y1 Output (@ 1.0 MHz)	– 27	– 20	—	
Chroma Subcarrier Residual				
(Measured at Y1 Output, with 17.7 MHz Crystal)				
f = Subcarrier	—	25	60	mVp-p
2nd Harmonic Residual	—	4.0	12	
4th Harmonic Residual	—	12	30	
(Measured at R-Y, B-Y Outputs, with 17.7 or 14.3 MHz Crystal)				
f = Subcarrier	—	5.0	20	
2nd Harmonic Residual	—	5.0	20	
4th Harmonic Residual	—	15	50	
Y1 Luma Output (Pin 33)				
Clamp Level	0.4	1.1	1.8	Vdc
Output Impedance	—	300	—	Ω
Composite Video Mode ($77-6, 7 = 00)				
Output Level versus Input Level				
Delay = 000, Peaking = 111, f = 100 kHz	1.0	1.1	1.2	V/V
Delay = Min-to-Max, Peaking = Min-to-Max	—	1.1	—	
– 3 dB Bandwidth (17.7 MHz Crystal, PAL Decoding selected, Sound trap at 6.5 MHz, Peaking off)	—	2.8	—	MHz
Peaking Range ($7D-7, $7E-6/7 = 000 to 111, @ 3.0 MHz, with 17.7 MHz Crystal, Sound trap at 6.5 MHz)	5	8	10	dB
Overshoot with Minimum Peaking	—	0	—	%
Differential Non-linearity (Measured with Staircase)	—	2.0	—	%
Delay (Pin 1 or 3 to 33)				
With 14.3 MHz Crystal: Minimum	—	690	—	ns
Maximum	—	1040	—	
With 17.7 MHz Crystal: Minimum	—	594	—	
Maximum	—	876	—	

NOTE: 1. This spec indicates a correct output amplitude at Pins 41 and 42, with respect to Y1 output. For standard color bar inputs, the output amplitude is between 1.5 and 1.7 Vp-p, with the settings in Tables 1 and 2.

ELECTRICAL CHARACTERISTICS (T_A = + 25°C, V_{CC1} = V_{CC2} = V_{CC3} = 5.0 V, unless otherwise noted.)

Parameter	Min	Typ	Max	Unit
PAL/NTSC/S-VHS DECODER				
S-VHS Mode ($77-6, 7 = 11)				
Output Level versus Input Level (Delay = Min-to-Max)	1.0	1.1	1.2	V/V
– 3 dB Bandwidth (17.7 MHz crystal, PAL Decoding selected, Sound trap at 6.5 MHz)	—	4.5	—	MHz
Y/C Crosstalk Rejection	20	40	—	dB
Delay (Luma input to Pin 33)				
14.3 MHz Crystal: Minimum	—	395	—	ns
Maximum	—	745	—	
17.7 MHz Crystal: Minimum	—	350	—	
Maximum	—	632	—	
Crystal Oscillator				
PLL Pull-in range with respect to Subcarrier Frequency (Burst Level ≥ 30 mVp-p): with 17.7 MHz Crystal	—	± 350	—	Hz
with 14.3 MHz Crystal	—	± 300	—	
$4f_{SC}$ Filter (Pin 44) DC Voltage				
@ 14.3 MHz	—	2.4	—	Vdc
@ 17.7 MHz	—	3.5	—	
No Burst present	—	1.3	—	
DC Voltages				Vdc
System Select (Pin 34)				
NTSC Mode (SSA = 1, SSB = 0, SSC = 0, SSD = 0)	1.5	1.75	2.0	
PAL Mode (SSA = 0, SSB = 1, SSC = 0, SSD = 0)	0	0.075	0.4	
Color Kill Mode (SSA = 1, SSB = 1, SSC = 0, SSD = 0)	—	0.075	—	
External Mode (SSA = X, SSB = X, SSC = 1, SSD = 0)	3.7	4.0	4.3	
Ident Filter (Pin 43)				
NTSC Mode	—	1.6	—	
PAL Mode	1.2	1.5	1.8	
No Burst present	—	0.2	—	
ACC Filter (Pin 2)				
No Burst present	—	0.25	—	
Threshold for ACC Flag on	0.8	1.2	1.6	
Burst = 50 mVp-p	—	1.4	—	
Burst = 280 mVp-p	—	1.7	—	
System Select Output Impedance	—	40	100	kΩ
COLOR DIFFERENCE SECTION				
RGB/YUV Outputs				
Output Swing, Black-to-White (DAC $81 = 63)	2.0	3.0	—	Vp-p
THD (RGB Inputs to RGB Outputs @ 1.0 MHz, 0.7 Vp-p)	—	0.5	2.0	%
– 3 dB Bandwidth	—	6.0	—	MHz
Clamp Level				
RGB Outputs ($7D, 7E = 00)	—	1.4	—	Vdc
UV Outputs ($7D, 7E = 32)	—	2.3	—	
Red, Blue Clamp Level Change (DACs $7D, 7E varied from 00 to 63)	0.85	1.8	2.4	
Crosstalk Rejection				
Among RGB Outputs @ 1.0 MHz	20	40	—	dB
Y1 to Y2	20	40	—	
From RGB Outputs to Y1 or Y2	20	40	—	
Input Black Clamp Voltage at Y2, B-Y, R-Y, and RGB	2.4	3.0	3.6	Vdc
Fast Commutate Input (Pin 25)				
Switching Threshold Voltage	—	0.5	—	Vdc
Input Current @ V_{in} = 0 V	—	– 7.5	—	µA
Input Current @ V_{in} = + 5.0 V	—	0	—	
Timing: Input Low-to-High (RGB Enable)	—	50	—	ns
Input High-to-Low (RGB Disable)	—	90	—	

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ELECTRICAL CHARACTERISTICS (T_A = + 25°C, V_{CC1} = V_{CC2} = V_{CC3} = 5.0 V, unless otherwise noted.)

Parameter	Min	Typ	Max	Unit
COLOR DIFFERENCE SECTION				
Contrast (Gain)				V/V
Y1 to RGB (DAC $81 = 32, DAC $86 = 00)	1.9	2.4	3.0	
Y2 to RGB (DAC $81 = 32, DAC $86 = 00)	1.8	2.3	2.8	
Green In (Pin 27) to Green Out (Pin 21) with YX Enabled ($82-6 = 1, DAC $81 and DAC $86 = 32)	1.8	2.3	2.4	
Red-to-Green and Blue-to-Green Gain Ratio	0.8	1.0	1.2	
RGB Input to RGB Output with YX Not Enabled ($82-6 = 0, DAC $81 and DAC $86 = 32)	2.0	2.6	3.2	
Ratio (DAC $81 = 00 versus 32)	—	0.2	0.4	
Ratio (DAC $81 = 63 versus 32)	1.5	2.0	2.5	
Red and Blue Trim Control (DACs $80, 82 varied from 00 to 63)	± 5	± 30	± 60	%
Saturation (Average of R, G, B saturation levels with respect to Luma)				
Inputs at Pins 29 to 31 (DAC $86 = 32)	50	90	130	%
Ratio (DAC $86 = 00 versus 32)	—	—	5	
Ratio (DAC $86 = 63 versus 32)	150	170	190	
Inputs at Pins 26 to 28 (DAC $86 = 32, $82-6 = 1)	70	125	180	
Brightness				
Black Level Range (Brightness = 00 to 63 with respect to Brightness setting of 32)	± 0.3	± 0.5	± 0.7	Vdc
Red and Blue Trim Control (DACs $83, 85 varied from 00 to 63)	± 0.05	± 0.3	± 0.6	
Color Coefficients				
G-Y Matrix Coefficient versus B-Y	− 0.21	− 0.19	− 0.17	
G-Y Matrix Coefficient versus R-Y	− 0.56	− 0.51	− 0.46	
YX Matrix (Inputs at Pins 26 to 28, $82-6 = 1):				
Y versus R	0.28	0.30	0.32	
Y versus G	0.57	0.59	0.61	
Y versus B	0.09	0.11	0.13	
HORIZONTAL TIME BASE SECTION (PLL #1)				
Free-Running Period (Calibration mode in effect, Bit $86-6 = 1)				
17.7 MHz Crystal selected ($84-6 = 0)	62.5	64.0	65.5	µs
14.3 MHz Crystal selected ($84-6 = 1)	62.5	63.5	65.5	
VCO minimum period (Pin 11 Voltage at 1.2 V)	56	59.5	62	µs
VCO maximum period (Pin 11 Voltage at 2.8 V)	66	69.5	72	
VCO Control Gain factor	5.0	8.5	12	µs/V
Phase Detector Current				
High Gain ($83-6 = 1)	15	50	85	µA
Low Gain-to-High Gain Current Ratio	0.32	0.38	0.44	µA/µA
Noise Gate Width ($77-2 = 0, Low Gain, see Figure 26)	—	16	—	µs
Horizontal Filter Switch (Pin 12)				
Saturation Voltage (I_{12} = 20 µA)	—	10	100	mV
Dynamic Impendance ($84-7 = 1)	—	< 5.0	—	kΩ
Parallel Resistance ($84-7 = 0)	0.6	1.0	—	MΩ
Pins 8, 13, 14 Output Level				
High (I_O = − 40 µA)	2.4	4.5	—	Vdc
Low (I_O = + 800 µA)	—	0.1	0.8	
Burst Gate (Pin 8) Timing (See Figures 25, 27)				µs
Rising edge from Sync leading edge (Pins 1, 3)	4.4	5.6	6.8	
Rising edge from Sync center (Pins 26 to 29)	—	2.5	—	
Pulse Width	3.0	3.5	4.0	
16 Fh Output (Pin 13) Timing (Bit $85-6 = 0) (See Figures 25, 27)				
Rising edge from Fh rising edge	—	1.3	—	µs
Duty Cycle	—	50	—	%
Composite Sync Output (Pin 13) Timing (Bit $85-6 = 1)				µs
Input Sync center to Output Sync center (Pins 1, 3)	—	0.95	—	
Input Sync center to Output Sync center (Pins 26 to 29)	—	0.4	—	

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ELECTRICAL CHARACTERISTICS (T_A = + 25°C, V_{CC1} = V_{CC2} = V_{CC3} = 5.0 V, unless otherwise noted.)

Parameter	Min	Typ	Max	Unit
HORIZONTAL TIME BASE SECTION (PLL #1)				
Fh Reference (Pin 14) Timing (See Figures 25, 27)				
Rising edge from Sync center (Pins 1, 3)	—	1.3	—	µs
Rising edge from Sync center (Pins 26 to 29)	—	650	—	ns
Duty cycle	—	50	—	%
Sandcastle Output (Pin 35, see Figures 25, 27)				Vdc
Output Voltage – Level 1	3.7	4.0	4.3	
Output Voltage – Level 2	2.8	3.0	3.2	
Output Voltage – Level 3	—	1.55	—	
Output Voltage – Level 4	—	0.07	—	
Rising edge from Sync center (Pins 1, 3)	—	– 2.6	—	µs
Rising edge from Sync center (Pins 26 to 29)	—	– 3.3	—	
High Time	—	6.0	—	
Level 2 Time	—	5.0	—	
Reference Voltage @ Pin 9 (I_{ref} = 32 µA)	1.0	1.2	1.4	Vdc
PHASE-LOCKED PIXEL CLOCK SECTION (PLL #2)				
VCO Frequency @ Pin 18				MHz
Minimum (Pin 16 = 1.6 V, $85-7 = 1)	—	2.0	4.0	
Maximum (Pin 16 = 4.0 V, $85-7= 0)	30	45	60	
VCO Up (Flag 19) Threshold Voltage @ Pin 16	1.5	1.7	1.9	Vdc
VCO Down (Flag 20) Threshold Voltage @ Pin 16	3.1	3.3	3.5	
VCO Control Voltage Range @ Pin 16	1.2	—	3.8	Vdc
VCO Control Gain factor ($7FDAC = 00, $85-7 = 0)	4.0	8.0	12	MHz/V
Charge Pump Current (Pin 16)	25	50	75	µA
High Gain ($83-7 = 0)				
Current Ratio	0.3	0.4	0.5	µA/µA
Low Gain-to-High Gain				
Pixel Clock Output (Pin 18) (Load = 3 FAST TTL loads + 10 pF)				
Output Voltage – High	—	3.9	—	Vdc
Output Voltage – Low	—	0.15	—	
Rise Time @ 50 MHz	—	7.0	—	ns
Rise Time @ 9.0 MHz	—	17	—	
Fall Time @ 50 MHz	—	5.0	—	
Fall Time @ 9.0 MHz	—	8.0	—	
15 kHz Return (Pin 15)				
Input Threshold Voltage	—	1.5	—	Vdc
Falling edge from Fh rising edge	—	60	—	ns
Minimum Input Low Time	200	—	—	
VERTICAL DECODER				
Vertical Frequency Range	43.3	—	122	Hz
Vertical Sync Output				
Saturation Voltage (I_O = 800 µA)	—	0.1	0.8	V
Leakage Current @ 5.0 V (Output high)	—	—	40	µA
Timing from Sync polarity reversal to Pin 4 falling edge (See Figures 33, 34)				µs
($78-7 = 0)	32	36	40	
($78-7 = 1)	62	68	74	
Vertical Sync Pulse Width (Pin 4, NTSC or PAL)	490	500	510	µs
Field Ident (Pin 7) Output Voltage – High (I_O = – 40 µA)	2.4	4.5	—	Vdc
Output Voltage – Low (I_O = + 800 µA)	—	0.1	0.8	
Timing	—	Fig. 33, 34	—	
HORIZONTAL SYNC SEPARATOR				
Sync Slicing Levels (Pins 1, 3)	—	120	—	mV
From Black Level (Pins 26 to 29)	—	150	—	

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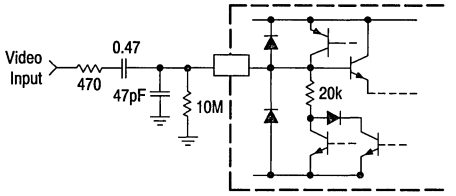
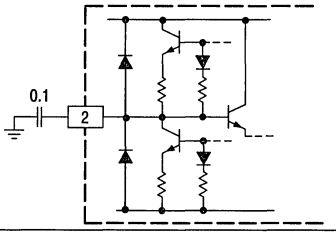
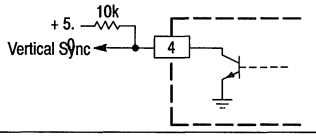
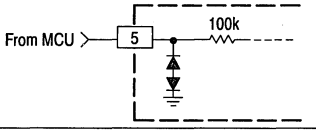
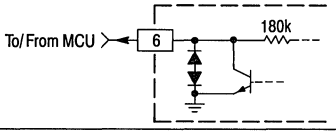
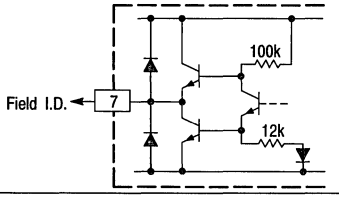
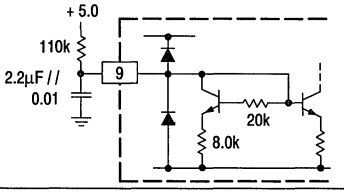
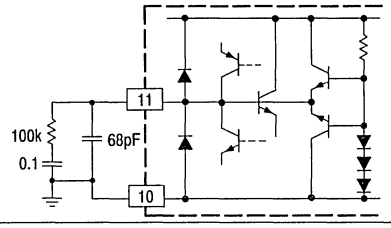
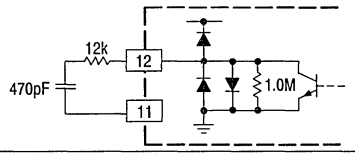
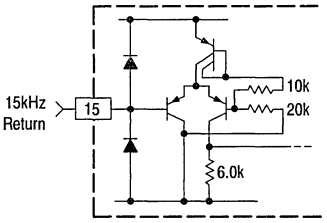
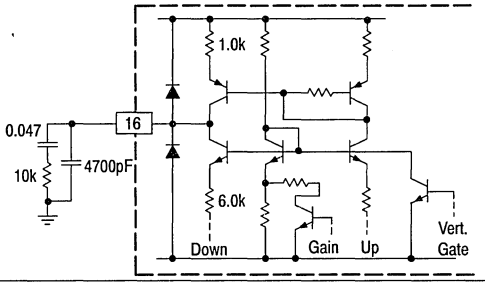
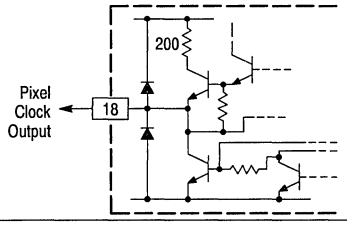
PIN FUNCTION DESCRIPTION

Pin No.	Representative Circuitry	Description
1, 3		**Video Input 1 & 2** – Video 1 (Pin 1) and Video 2 (Pin 3) are composite video inputs. Either can be NTSC or PAL. Input impedance is high, termination must be external. Also used for the luma and chroma components of an S-VHS signal. Selection of these inputs is done by software. External components protect against ESD and noise.
2		**ACC Filter** – A 0.1 µF capacitor at this pin filters the feedback loop of the chroma automatic gain control amplifier. Input chroma burst amplitude can be between 30 and 600 mV_{p-p}.
4		**Vertical Sync Output** – An open collector output requiring an external pull-up. Output is an active low pulse, 500 µs wide, occurring each field. Timing of this pulse depends on Bit $78-7.
5		**SCL** – Clock for the I^2C bus interface. See Appendix C for specifications. Maximum frequency is 100 kHz.
6		**SDL** – Bidirectional data line for the I^2C bus interface. As an output, it is an open collector. (Write Address $8A, Read Address $8B)
7		**Field ID** – TTL level output indicating Field 1 or Field 2. Polarity depends on state of Bit $78-7 (Vert. Sync Delay). See Table 11 and Figure 33 and 34.
8	(Same as Pin 7)	**Burst Gate** – TTL level output used for external clamps, as well as internally. Pulse is active high, ≈ 3.5 µs wide, with the rising edge ≈ 3.0 µs after center of selected incoming sync pulse.
9		**Reference Current Input** – Current supplied to this pin, typically 32 µA from + 5.0 V through a 110 kΩ resistor, is the reference current for the calibration circuit. Noise filtering should be done at the pin. Voltage at this pin is typically 1.2 V.
10	(See power distribution diagram at the end of this section.)	**Quiet Ground** – Ground for the horizontal PLL filter (PLL #1) at Pin 11.

PIN FUNCTION DESCRIPTION

Pin No.	Representative Circuitry	Description
11		**H Filter** – Components at this pin filter the output of the phase detector of PLL #1. This PLL becomes phase-locked to the selected incoming horizontal sync. External component values are valid for NTSC and PAL systems.
12		**H Filter Switch** – An internal switch-to-ground which permits altering the filtering action of the components at Pin 11.
13	(Same as Pin 7)	**16 Fh/C_{Sync}** – A TTL level output from PLL #1. This pin provides either a square wave equal to Fh x 16 (≈ 250 kHz), or composite sync, depending on the setting of Bit $85-6.
14	(Same as Pin 7)	**Fh Reference** – A TTL square wave output which is phase-locked to the selected incoming horizontal sync. The rising edge occurs ≈ 1.3 µs after sync center.
15		**15 kHz Return** – This TTL input receives the output of an external frequency divider which is part of PLL #2 (Pixel Clock PLL). This signal will be phase and frequency-locked to the Fh signal at Pin 14. If PLL #2 is not used, this pin should be connected to a + 5.0 V supply.
16		**PLL #2 Filter** – Components at this pin filter the output of the phase detector of PLL 2. This PLL becomes phase-locked to the Fh signal at Pin 14. Recommended values for filter components are shown. External components should be connected to ground at Pin 17. If PLL #2 is not used, this pin should be grounded.
17	(See power distribution diagram at the end of this section.)	**GND 3** – Ground for the high frequency PLL #2. Signals at Pins 15 to 19 should be referenced to this ground.
18		**Pixel Clock Output** – Sampling clock output (TTL) for external A/D converters, and for the external frequency divider. Frequency range at this pin is 6.0 to 40 MHz.
19	(See power distribution diagram at the end of this section.)	**V_{CC3}** – A + 5.0 V supply (± 5%), for the high frequency PLL #2. Decoupling must be provided from this pin to Pin 17. Ripple on this pin will affect pixel clock jitter.

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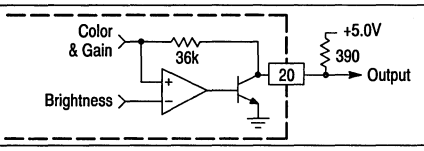
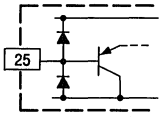
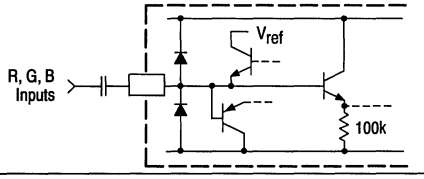
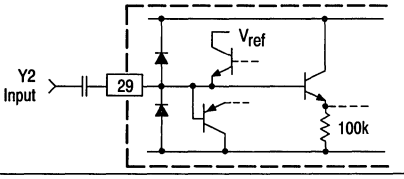
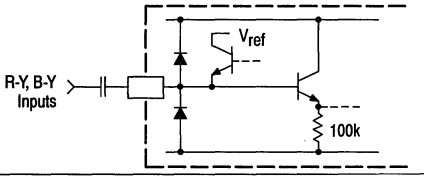
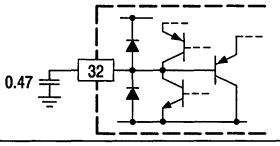
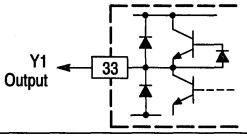
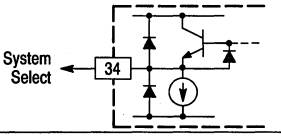
PIN FUNCTION DESCRIPTION

Pin No.	Representative Circuitry	Description
20		**R/V Output** – Red (in RGB mode), or R-Y (in YUV mode), output from the color difference stage. A pull-up (390 Ω) to + 5.0 V is required. Blank level is ≈ +1.4 Vdc. Maximum amplitude is ≈ 3.0 Vp-p, black-to-white.
21	(Same as Pin 20)	**G/Y Output** – Green (in RGB mode), or Y (in YUV mode), output from the color difference stage (same as Pin 20).
22	(Same as Pin 20)	**B/U Output** – Blue (in RGB mode), or B-Y (in YUV mode), output from the color difference stage (same as Pin 20).
23	(See power distribution diagram at the end of this section.)	V_{CC2} – A + 5.0 V supply (± 5%), for the color difference stage. Decoupling must be provided from this pin to Pin 24.
24	(See power distribution diagram at the end of this section.)	**GND 2** – Ground for the color difference stage. Signals at Pins 20 to 31 should be referenced to this pin.
25		**FC** – Fast Commutate switch. Taking this pin high (TTL level) connects the RGB inputs (Pins 26 to 28) to the RGB outputs (Pins 20 to 22), permitting an overlay function. The switch can be disabled in software (Bit $80-7).
26, 27, 28		**Blue (26), Green (27), Red (28) Inputs** – Inputs to the color difference stage. Designed to accept standard analog video levels, these input pins have a clamp and sync separator. They are selected with Pin 25 or in software (Bit $80-7).
29		**Y2 Input** – Luma #2/Composite sync input. This luma input to the color difference stage is used in conjunction with auxiliary color difference inputs, and/or as a sync input. Clamp and sync separator are provided.
30, 31		**B-Y (30), R-Y (31) Inputs** – Inputs to the color difference stage. Designed for standard color difference levels, these inputs can be capacitor coupled from the color difference outputs, from a delay line, or an auxiliary signal source. Input clamp is provided.
32		**Y1 Clamp** – A 0.47 µF capacitor at this pin provides clamping for the Luma #1 output.
33		**Y1 Output** – Luma #1 output. This output from the PAL/NTSC/S-VHS decoder is the luma component of the decoded composite video at Pin 1 or 3. It is internally directed to the color difference stage.
34		**System Select** – A multi-level DC output which indicates the color decoding system to which the PAL/NTSC detector is set by the software. This output is used by the MC44140 chroma delay line.

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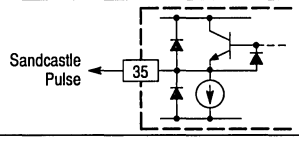
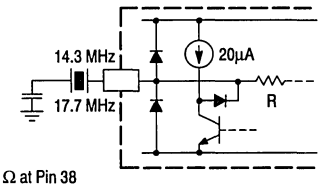
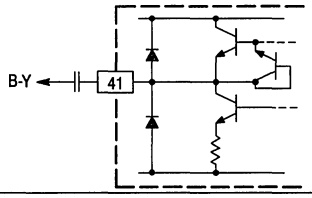
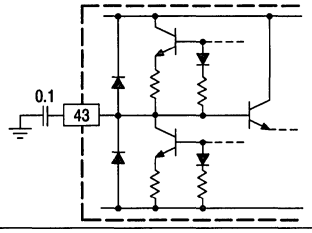
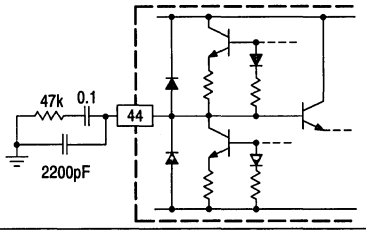
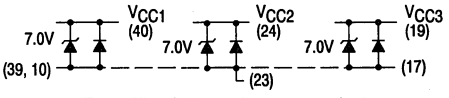
PIN FUNCTION DESCRIPTION

Pin No.	Representative Circuitry	Description
35		**Sandcastle Pulse** – A multi-level timing pulse output used by the MC44140 chroma delay line. This pulse encompasses the horizontal sync and burst time.
36, 38	 R = 400 Ω at Pin 38 R = 300 Ω at Pin 36	**Xtal 2 (36), Xtal 1 (38)** – Designed for connection of 4x subcarrier color crystals. Selection is done in software. The selected frequency is used by the PAL/NTSC detector; system identifier; all notches and traps; delay lines; and the horizontal calibration circuit. The crystal frequency should be: 14.3 MHz at Pin 36 for NTSC, 17.7 MHz at Pin 38 for PAL. (See Table 18 for crystal specs.)
37		**No Connect** – This pin is to be left open.
39	(See power distribution diagram at the end of this section.)	**Ground 1** – Ground for all sections except PLL #2 and the color difference stage.
40	(See power distribution diagram at the end of this section.)	V_{CC1} – A + 5.0 V (± 5%), supply to all sections except PLL #2 and the color difference stage.
41		**B-Y Output** – Output from the PAL/NTSC decoder, it is typically capacitor-coupled to a delay line or to the B-Y input. This pin is clamped, and filtered at the color subcarrier frequency, 2x, and 8x that frequency.
42	(Same as Pin 41)	**R-Y Output** – Output from the PAL/NTSC decoder.
43		**Ident Filter** – A 0.1 µF capacitor filters the system identification circuit in the NTSC/PAL decoder.
44		**Crystal PLL Filter** – Components at this pin filter the PLL for the crystal chroma oscillator circuit.
10, 17, 19, 23, 24, 39, 40	 (Dashed lines indicate substrate connection.)	**Power Distribution** – The three V_{CC} pins must be externally connected to + 5.0 V (± 5%) supply. The four grounds must be externally tied together, preferably to a ground plane.

9

Luma Frequency Response (14.3 MHz) Crystal, (4.5 MHz) Sound Trap

Figure 2. Comp. Video Mode

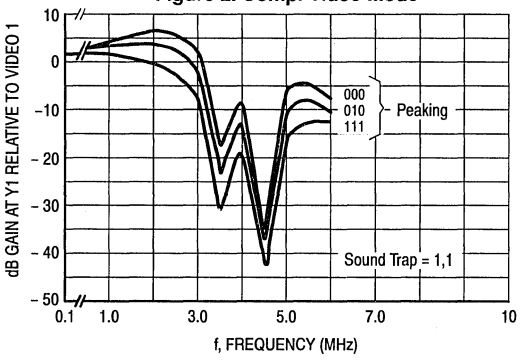
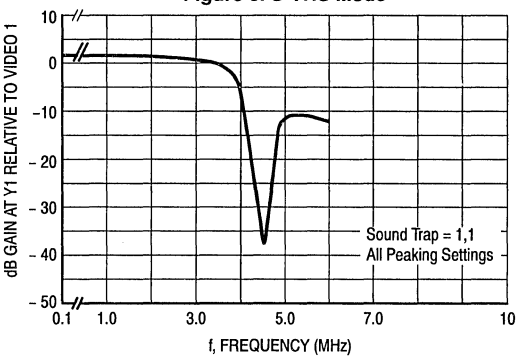


Figure 3. S-VHS Mode



Luma Frequency Response (17.7 MHz) Crystal, (5.5 MHz) Sound Trap

Figure 4. Comp. Video Mode

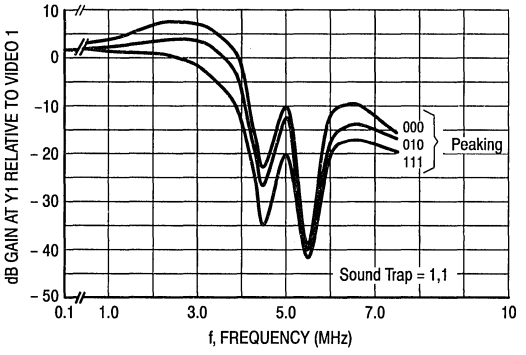
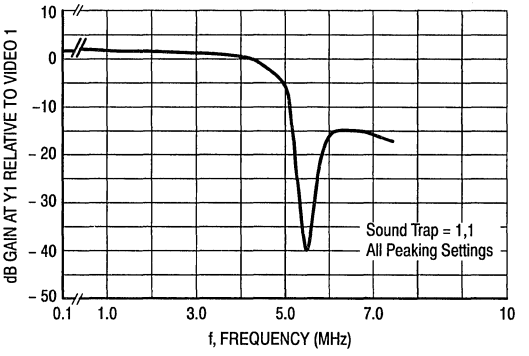


Figure 5. S-VHS Mode



Luma Frequency Response (17.7 MHz) Crystal, (5.5/5.75 MHz) Sound Trap

Figure 6. Comp. Video Mode

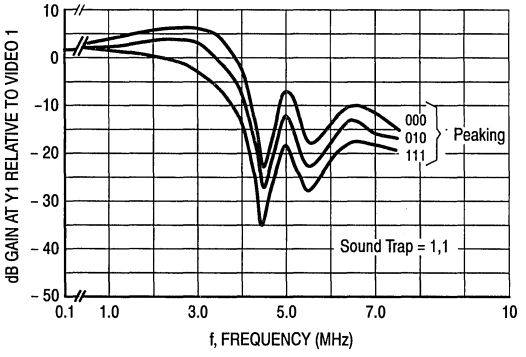
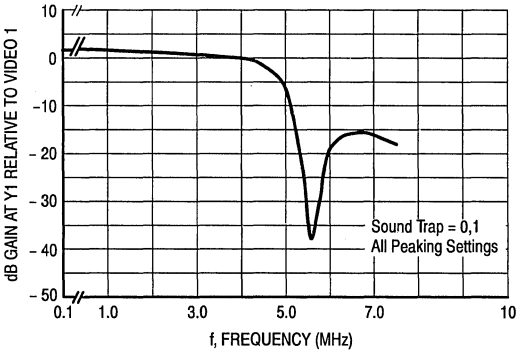


Figure 7. S-VHS Mode



9

Luma Frequency Response (17.7 MHz) Crystal, (6.0 MHz) Sound Trap

Figure 8. Comp. Video Mode

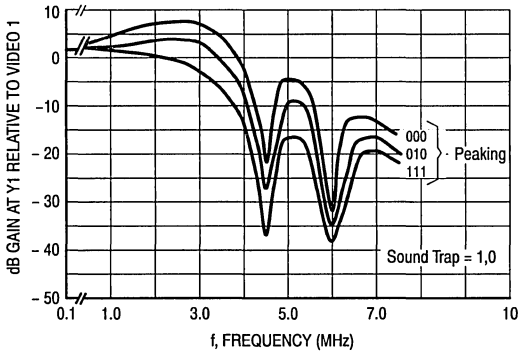
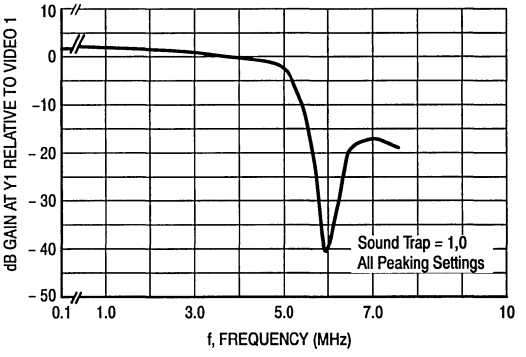


Figure 9. S-VHS Mode



Luma Frequency Response (17.7 MHz) Crystal, (6.5 MHz) Sound Trap

Figure 10. Comp. Video Mode

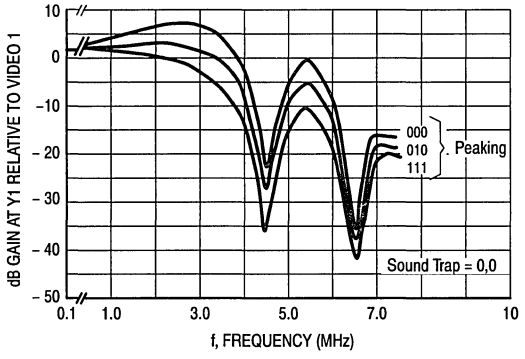


Figure 11. S-VHS Mode

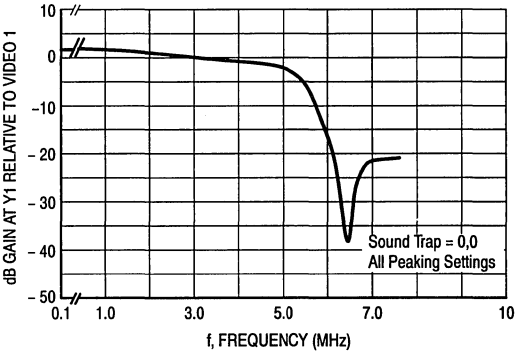


Figure 12. (3.58 MHz) Chroma Notch

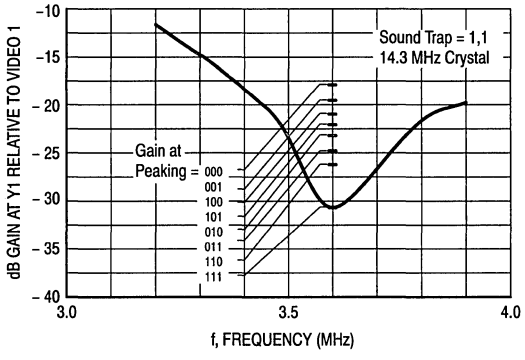
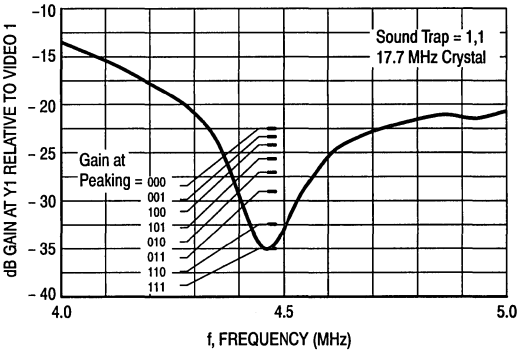


Figure 13. (4.43 MHz) Chroma Notch



9

(4.5 MHz) Sound Trap

Figure 14. Comp. Video Mode

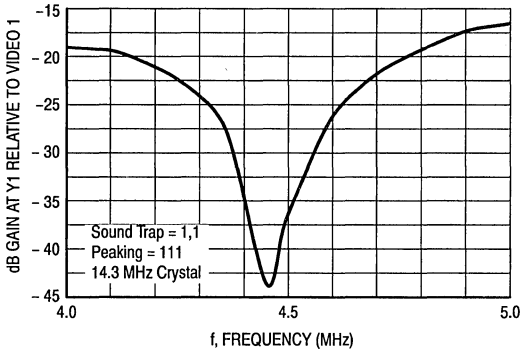
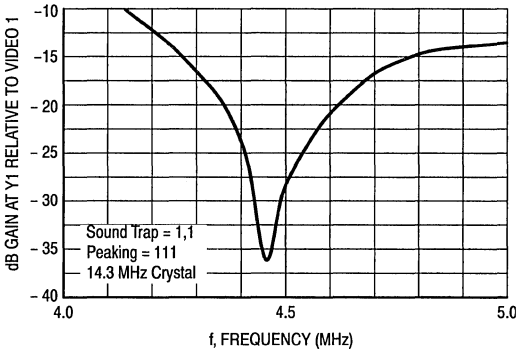


Figure 15. S-VHS Mode



(5.5 MHz) Sound Trap

Figure 16. Comp. Video Mode

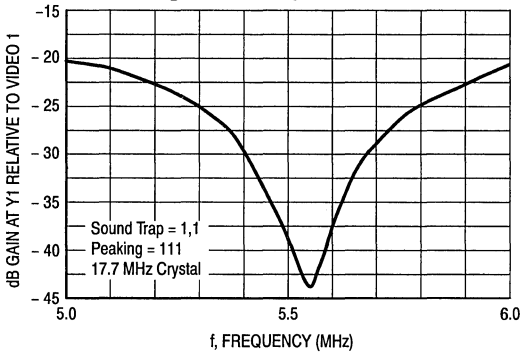
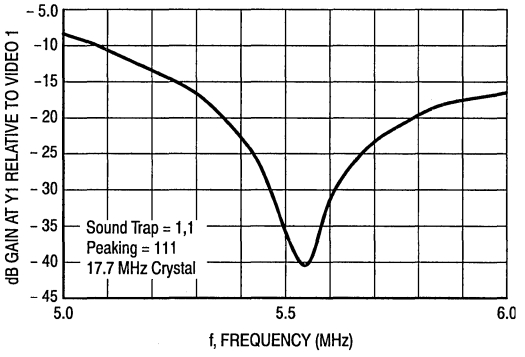


Figure 17. S-VHS Mode



(5.5 + 5.75 MHz) Sound Trap

Figure 18. Comp. Video Mode

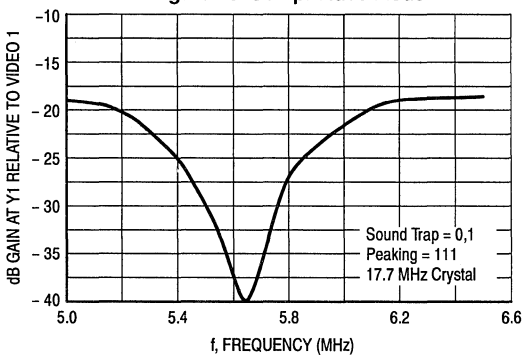
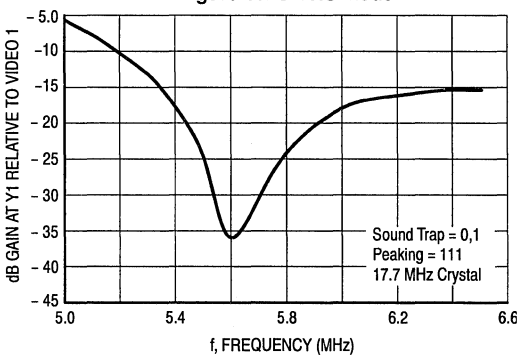


Figure 19. S-VHS Mode



9

(6.0 MHz) Sound Trap

Figure 20. Comp. Video Mode

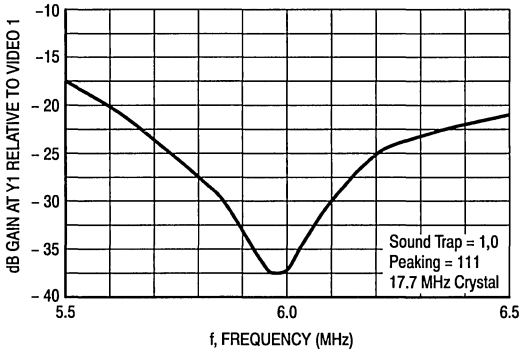
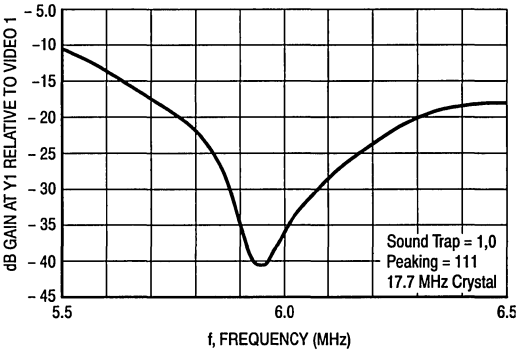


Figure 21. S-VHS Mode



(6.5 MHz) Sound Trap

Figure 22. Comp. Video Mode

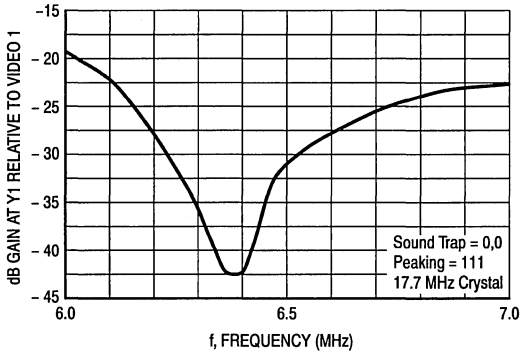


Figure 23. S-VHS Mode

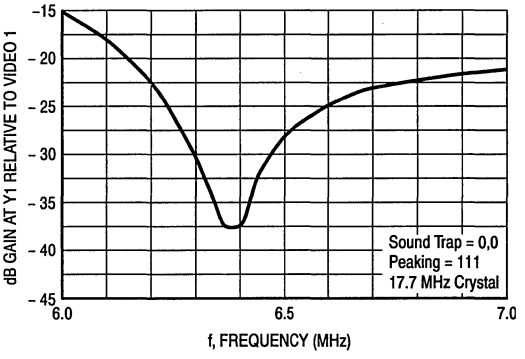


Figure 24. FC Input Current

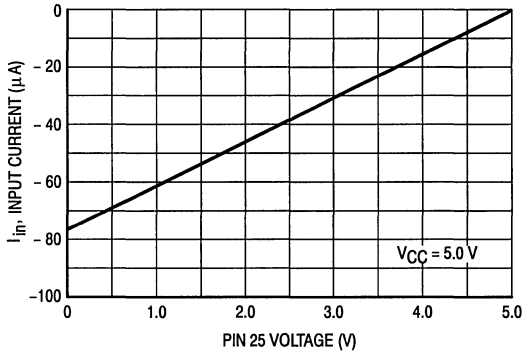
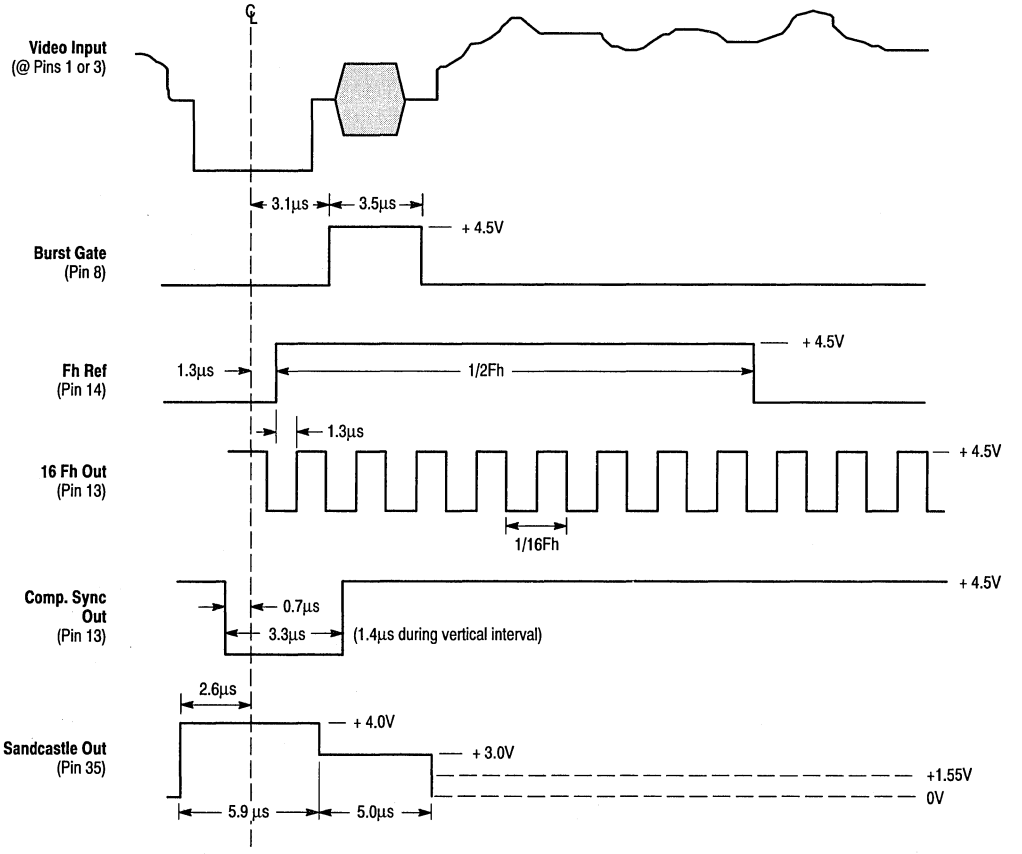


Figure 25. Horizontal PLL1 Timing/Composite Video Inputs



NOTE: In above waveforms, all timing is referenced to the **center** of the incoming Sync Pulse at Pin 1 or 3.
Above timings based on a 4.6 µs wide sync pulse.
Lower two levels of Sandcastle output alternate, based on video system in effect.
All timings are nominal, and apply to both PAL and NTSC signals.

Figure 26. Horizontal PLL1 Noise Gate and Filter Pin

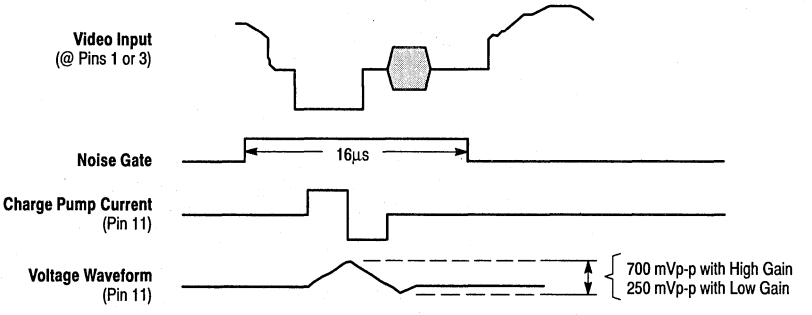
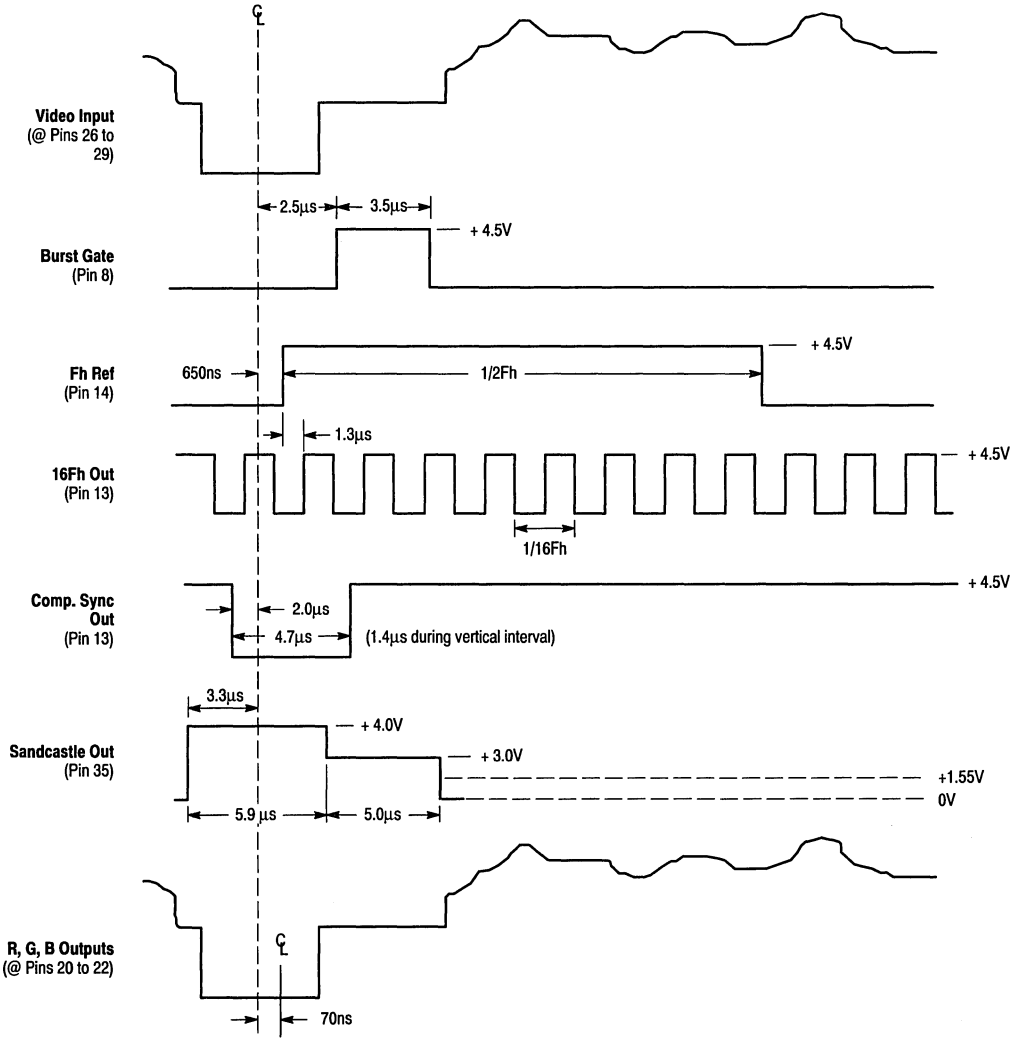


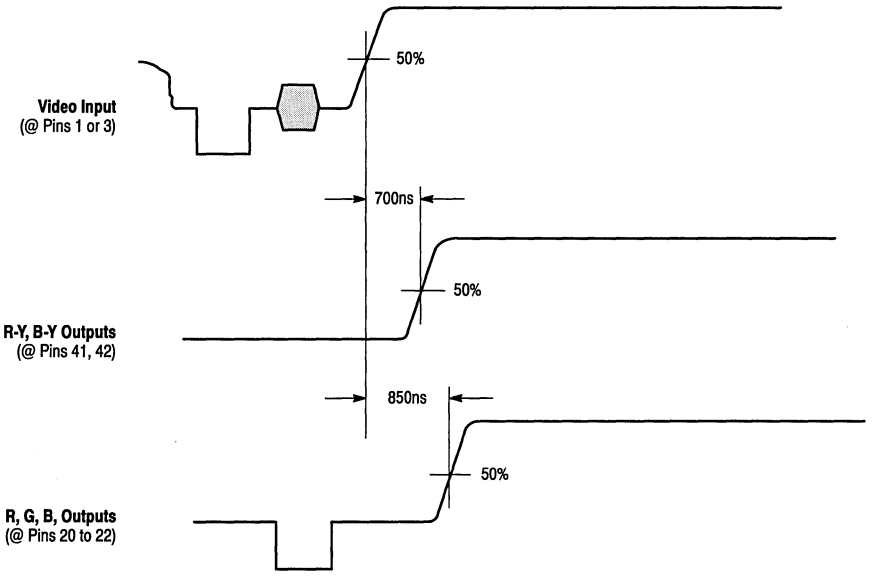
Figure 27. Horizontal PLL1 Timing/R, G, B and Y2 Inputs



NOTE: In above waveforms, all timing is referenced to the **center** of the incoming Sync Pulse at Pin 26 to 28, or 29.
Above timings based on a 4.6 µs wide sync pulse.
Lower two levels of Sandcastle output alternate, based on video system in effect.

9

Figure 28. System Timing/Video Inputs to RGB Outputs



9

Figure 29. Fast Commutate Timing

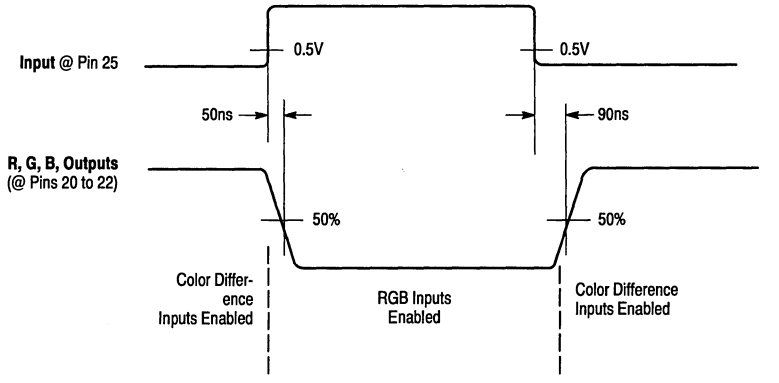


Figure 30. Horizontal Outputs versus Fields (NTSC System)

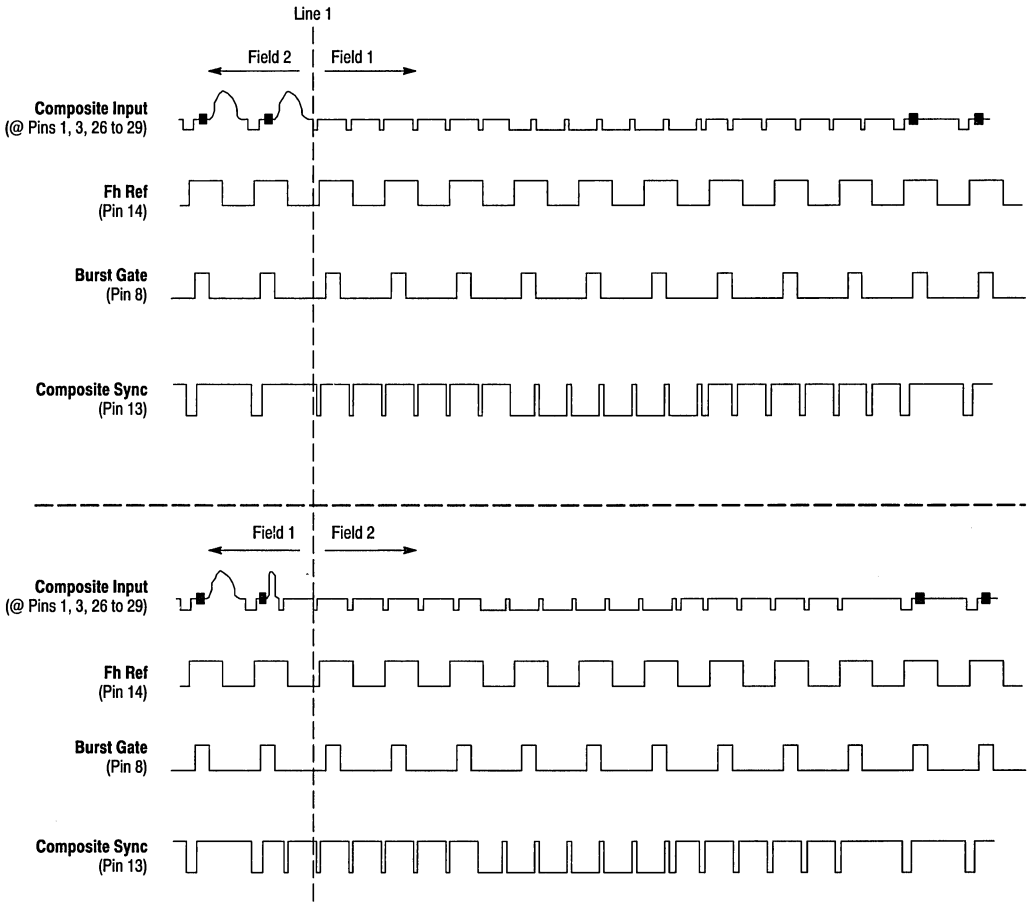


Figure 31. Horizontal Outputs versus Fields (PAL System)

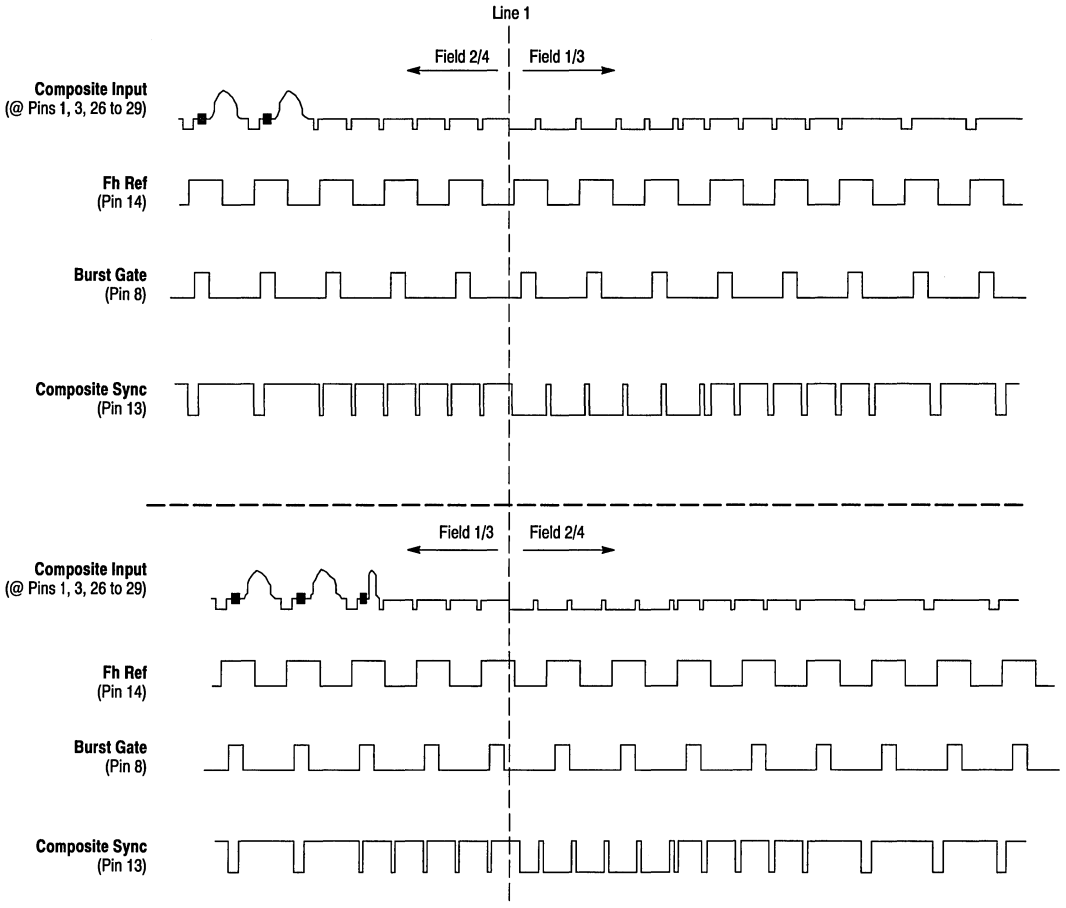


Figure 32. Horizontal PLL2 Timing

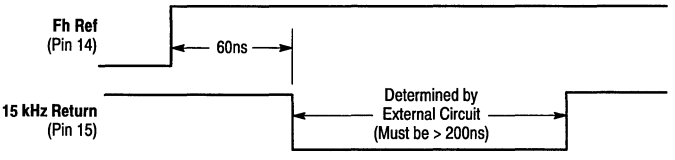
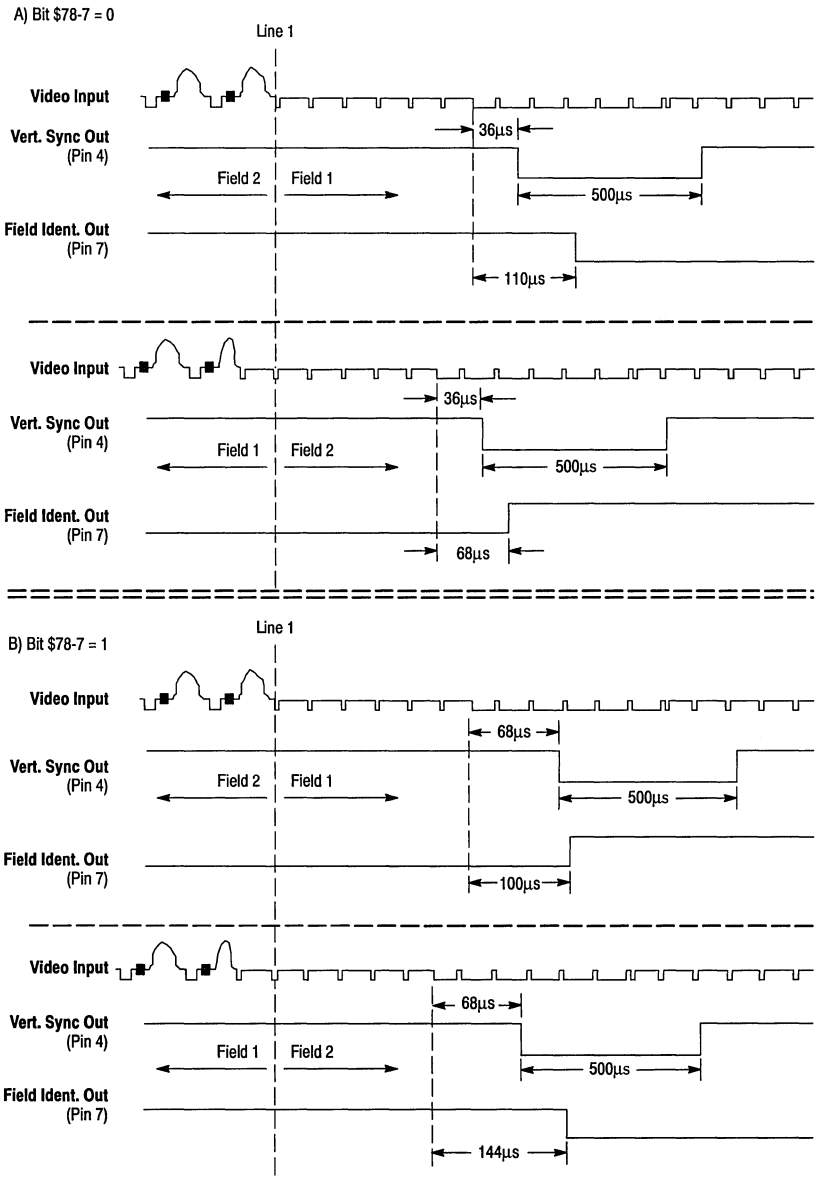
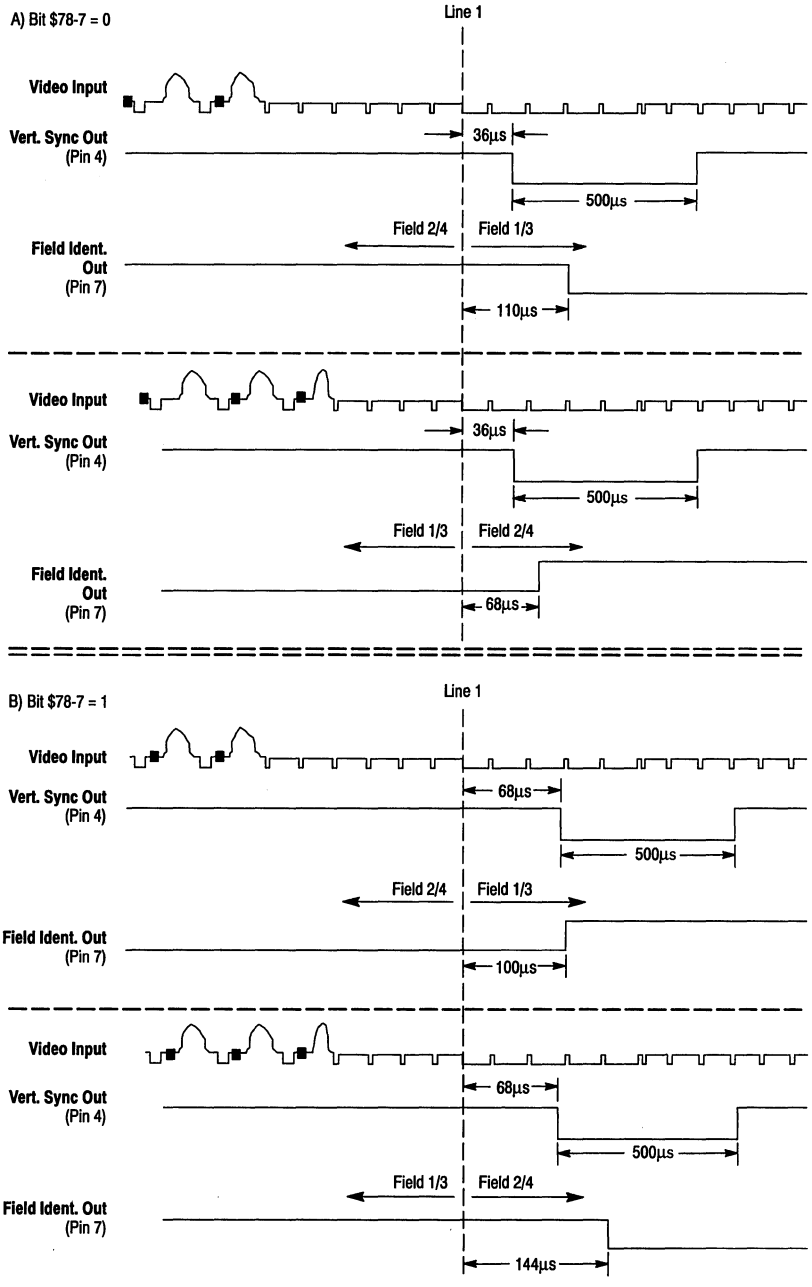


Figure 33. Vertical Timing (NTSC System)



9

Figure 34. Vertical Timing (PAL System)



FUNCTIONAL DESCRIPTION

Introduction

The MC44011, a member of the MC44000 Chroma 4 family, is a composite video decoder which has been tailored for applications involving multimedia, picture-in-picture, and frame storage (although not limited to those applications). The first stage of the MC44011 provides color difference signals (R-Y, B-Y, and Y) from one of two (selectable) composite video inputs, which are designed to receive PAL, NTSC, and S-VHS (Y,C) signals. The second stage provides either RGB or YUV outputs from the first stage's signals, or from a separate (internally selectable) set of RGB inputs, permitting an overlay function to be performed. Adjustments can be made to saturation; hue; brightness; contrast; brightness balance; contrast balance; U and V bias; subcarrier phase; and color difference gain ratio.

The above mentioned video decoding sections provide the necessary luma/delay function, as well as all necessary filters for sound traps, luma/chroma separation, luma peaking, and subcarrier rejection. External tank circuits and luma delay lines are not needed. For PAL applications, the MC44140 chroma delay line provides the necessary line-by-line corrections to the color difference signals required by that system.

The MC44011 provides a pixel clock to set the sampling rate of external A/D converters. This pixel clock, and other horizontal frequency related output signals, are phase-locked to the incoming sync. The VCO's gain is adjustable for optimum performance. The MC44011 also provides vertical sync and field identification (Field 1, Field 2) outputs.

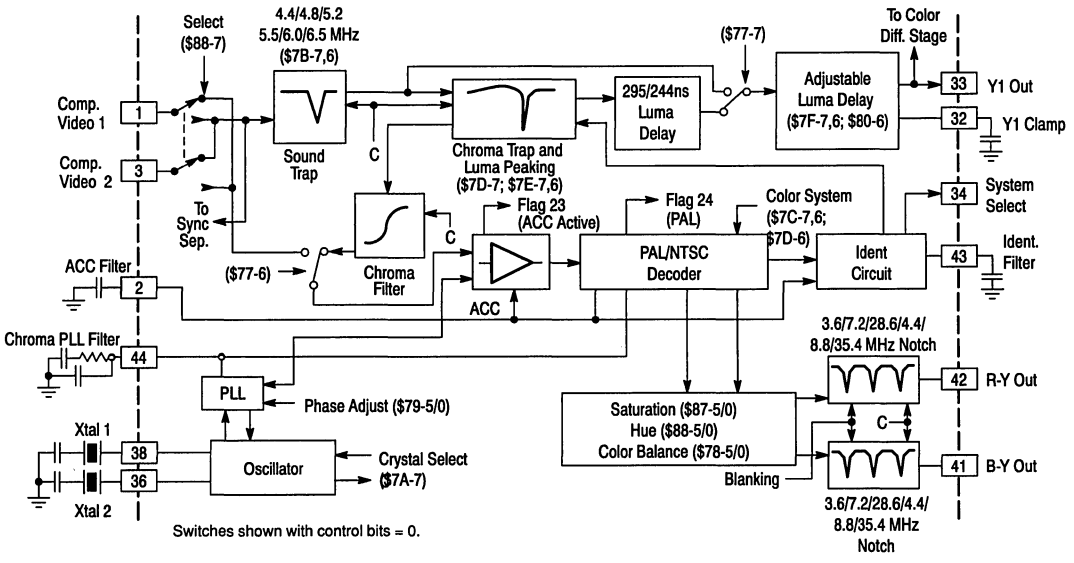
Selection of the various inputs, outputs, and functions, as well as the adjustments, is done by means of a two-wire I²C interface. The basic procedure requires the microprocessor system to read the internal flags of the MC44011, and then set the internal registers appropriately. This I²C interface eliminates the need for manual controls (potentiometers) and external switches. All of the external components for the MC44011, except for the two crystals, are standard value resistors and capacitors, and can be non-precision.

(The DACs mentioned in the following description are 6-bits wide. The settings mentioned for them are given in decimal values of 00 to 63. These are not hex values.)

PAL/NTSC/S-VHS Decoder

A block diagram of this decoder section is shown in Figure 35. This section's function is to take the incoming composite video (at Pins 1 or 3), separate it into luma and chroma information, determine if the signal is PAL or NTSC (for the flags), and then provide color difference and luma signals at the outputs. If the input is S-VHS, the luma/chroma separation is bypassed, but the other functions are still in effect.

Figure 35. PAL/NTSC/S-VHS Decoder Block Diagram



Inputs

The inputs at Pins 1 and 3 are high impedance inputs designed to accept standard 1.0 Vp-p positive video signals (with negative going sync). The inputs are to be capacitor-coupled so as not to upset the internal DC bias. When normal composite video is applied, the desired input is selected by Bit $88-7. Bits $77-6 and $77-7 must be set to 0 so that their switches are as shown in Figure 35. The selected signal passes through the sound trap, and is then separated by the chroma trap and the chroma (high pass) filter.

When S-VHS signals (Y,C) are applied to the two inputs, Bit $88-7 is used to direct the luma information to the sound trap, and the chroma information to the ACC circuit (Bit $77-6 must be set to a Logic 1). Bit $77-7 is normally set to a Logic 1 in this mode to bypass the first luma delay line and the chroma trap, but it can be left 0 if the additional delay is desired.

Sound Trap

The sound trap will filter out any residual sound subcarrier at the frequency selected by control bits T1 and T2 according to Table 3. The accuracy of the notch frequency is directly related to the selected crystal frequency.

Table 3. Sound Trap Frequency

Crystal Frequency	T1 ($7B-7)	T1 ($7B-6)	Notch Frequency
17.73 MHZ	0	0	6.5 MHz
17.73 MHZ	0	1	5.5 + 5.75 MHz
17.73 MHZ	1	0	6.0 MHz
	1	1	5.5 MHz
14.32 MHz	0	0	5.25 MHz
14.32 MHz	0	1	4.44 + 4.64 MHz
14.32 MHz	1	0	4.84 MHz
	1	1	4.44 MHz

Code 01 (for T1, T2) is used to widen the band rejection where stereo is in use. Typical rejection is 30 dB.

ACC and PAL/NTSC Decoder

The chroma filter bandpass characteristics (3.58 or 4.43 MHz) is determined by the selected crystal. The output of the chroma filter is sent to the ACC circuit which detects the burst signal, and provides automatic gain control once the crystal oscillator has achieved phase lock-up to the burst. The DC voltage at Pin 2 is ≈1.5 to 2.0 V. This will occur if the burst amplitude exceeds 30 mVp-p, and if the correct crystal is selected (Bit $7A-7). A 17.734472 MHz crystal is required for PAL, and a 14.31818 MHz crystal is required for NTSC. When Flag 23 is high, it indicates that the crystal's PLL has locked up, and the ACC circuit is active, providing automatic gain control. A small amount of phase adjustment (≈ ± 5°) of the crystal PLL, for color correction, can be made with control DAC $79-5/0. Pin 2 is the filter for the ACC loop, and Pin 44 is the filter for the crystal oscillator PLL.

The PAL/NTSC decoder then determines if the signal is PAL or NTSC by looking for the alternating phase characteristic of the PAL burst. When Flag 24 is high, PAL has been detected. Bits SSA, SSB, SSC, and SSD (Table 4) must then be sent to the decoder to set the appropriate decoding method.

Table 4. Color System Select

SSA ($7C-6)	SSB ($7D-6)	SSC ($7C-7)	SSD ($7A-6)	Color System
0	0	0	0	Not Used
0	1	0	0	PAL
1	0	0	0	NTSC
1	1	0	0	Color Kill
X	X	1	0	External

Upon receiving the SSA to SSD bits, the decoder provides the correct color difference signals, and with the Identification circuit, provides the correct level at the System Select output (Pin 34). This output is used by the MC44140 delay line.

The color kill setting (SSA = SSB = 1) should be used when the ACC flag is 0, when the color system cannot be properly determined, or when it is desired to have a black-and-white output (the ACC circuit and flag will still function if the input signal has a burst signal). The "External" setting (SSC = 1) is used when an external (alternate) source of color difference signals are applied to the MC44140 delay line. (See Miscellaneous Applications Information for more details.)

Color Difference Controls and Outputs

The color difference signals (R-Y, B-Y) from the PAL/NTSC decoder are directed to the saturation, hue and color balance controls, and then through a series of notch filters before being output at Pins 41 and 42. Blanking and clamping are applied to these outputs.

The saturation control DAC($87-5/0) varies the amplitude of the two signals from 0 Vp-p (DAC setting = 00), to a maximum of ≈1.8 Vp-p (at a DAC setting of 63). The maximum amplitude (without clipping) is ≈1.5 Vp-p, but a nominal setting is ≈1.3 Vp-p at a DAC setting of 15.

The hue control ($88-5/0) varies the relative amplitude of the two signals to provide a hue adjustment. The nominal setting for this DAC is 32.

The color balance control ($78-5/0) provides a fine adjustment of the relative amplitude of the two outputs. This provides for a more accurate color setting, particularly when NTSC signals are decoded. The nominal setting for this DAC is 32, and should be adjusted before the hue control is adjusted.

The notch filters provide filtering at the color burst frequency, and at 2x and 8x that frequency. Additionally, blanking and clamping (derived from the horizontal PLL) are applied to the signals at this stage. The nominal output DC level is ≈ 2.0 to 2.5 Vdc, and the load applied to these outputs should be >10 kΩ. Sync is not present on these outputs.

Luma Peaking, Delay Line, and Y1 Output

When composite video is applied, the luma information extracted in the chroma trap is then applied to a stage which allows peaking at ≈ 3.0 MHz with the 17.7 MHz crystal (≈ 2.2 MHz with the 14.3 MHz crystal). The amount of peaking at Y1 is with respect to the gain at the minimum peaking value (P1, P2, P3 = 111), and is adjustable with Bits $7D-7, and $7E-7,6 according to Table 5.

The luma delay lines allow for adjustment of that delay so as to correspond to the chroma delay through this section. Table 6 indicates the amount of delay using the D1-D3 bits ($7F-7,6, and $80-6). The delay indicated is the total delay from Pin 1 or 3 to the Y1 output at Pin 33. The amount of delay depends on whether Composite Video is applied, or YC signals (S-VHS) are applied.

The output impedance at Y1 is ≈ 300 Ω, and the black level clamp is at ≈ +1.1 V. Sync is present on this output. Y1 is also internally routed to the color difference stage.

Table 5. Luma Peaking

P1 ($7D-7)	P2 ($7E-6)	P3 ($7E-7)	Y1 Peaking
0	0	0	+ 9.5 dB
0	0	1	+ 8.5
1	0	0	+ 7.7
1	0	1	+ 6.5
0	1	0	+ 5.3
0	1	1	+ 3.8
1	1	0	+ 2.2
1	1	1	0

17.7 MHz Crystal, 6.5 MHz Sound Trap, Comp. Video Mode

Table 6. Luma Delay

D1 ($7F-6)	D2 ($80-6)	D3 ($7F-7)	14.3 MHz Crystal		17.7 MHz Crystal	
			Comp. Video ($77-7 = 0)	S-VHS ($77-7 = 1)	Comp. Video ($77-7 = 0)	S-VHS ($77-7 = 1)
0	0	0	690 ns	395 ns	594 ns	350 ns
0	0	1	760	465	650	406
0	1	0	830	535	707	463
0	1	1	900	605	763	519
1	0	0	970	675	819	575
1	0	1	1040	745	876	632
1	1	0	970	675	819	575
1	1	1	1040	745	876	632

9

Color Difference Stage and RGB/YUV Outputs

A block diagram of this section is shown in Figure 36. This section's function is to take the color difference input signals (Pins 30,31), or the RGB inputs (Pins 26 to 28), and output the information at Pins 20 to 22 as either RGB or YUV.

The inputs (on the left side of Figure 36) are analog RGB, or color difference signals (R-Y and B-Y) with Y1 or Y2 as the luma component. Pin 25 (Fast Commutate) is a logic level input, used in conjunction with $\overline{\text{RGB EN}}$ (Bit $80-7), to select the RGB inputs or the color difference inputs. The outputs (Pins 20 to 22) are either RGB or YUV, selected with Bit $82-7. The bit numbers adjacent to the various switches and gates indicate the bits used to control those functions. Table 7 indicates the modes of operation.

Table 7. Color Difference Input/Output Selection

FC	$\overline{\text{RGB EN}}$ $80-7	YX EN $82-6	YUV EN $82-7	Function
1	0	0	0	RGB inputs, RGB outputs, no saturation control
1	0	1	0	RGB inputs, RGB outputs, with saturation control
1	0	1	1	RGB inputs, YUV outputs, with saturation control
1	0	0	1	Not usable
FC Low and/or $\overline{\text{RGB EN}}$ Hi		X	0	R-Y, B-Y inputs, RGB outputs. Y1 or Y2 must be selected
FC Low and/or $\overline{\text{RGB EN}}$ Hi		X	1	R-Y, B-Y inputs, YUV outputs. Y1 or Y2 must be selected

In addition to Table 7, the following guidelines apply:

a) To select the RGB inputs, both FC must be high and $\overline{\text{RGB EN}}$ must be low. Therefore, the RGB inputs can be selected either by the I²C bus by leaving FC permanently high, or by the FC input by leaving Bit $80-7 permanently low. For overlay functions, where high speed, well controlled switching is necessary, the FC pin must be the controlling input.

b) When the R-Y, B-Y inputs are selected, either Y1 or Y2 must be selected, and the other must be deselected. The YX input is automatically disabled in this mode.

c) In applications where the color difference inputs are obtained from the NTSC/PAL decoder (from a composite video signal), Y1 is used. The Y2 input is normally used where alternately sourced color difference signals are applied, either through the MC44140 delay line, or through other external switching to Pins 30 and 31.

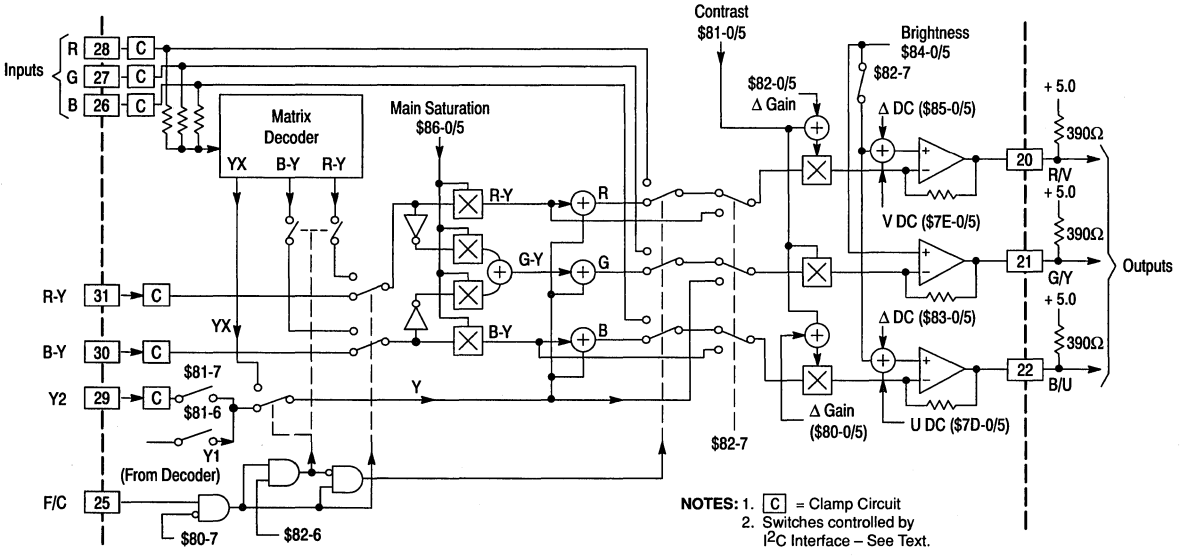
In Figure 36, the bit numbers followed by "– 0/5" indicate DAC operated controls (contrast, brightness, etc.), which are controlled by the I²C bus. The DACs have 6-bit resolution, allowing 64 adjustment steps. Table 8 provides guidelines on the DAC operation.

Table 8. DAC Operation – Color Difference Section

Function	Bits	RGB Outputs ($82-7 = 0)	YUV Outputs ($82-7 = 1)
Brightness	$84-0/5	Affects DC black and maximum levels of the three outputs, but not the clamp level, nor the amplitude.	Affects DC black and white levels of the Y output only, but not the clamp level, nor the amplitude.
Δ DC – Red Δ DC – Blue	$85-0/5 $83-0/5	Fine tune the Red and Blue brightness levels.	Allows a small amount of color tint control (not to be confused with hue).
Contrast	$81-0/5	Provides gain adjustment (black-to-white) of the three outputs.	Provides gain adjustment of the three outputs.
Δ Gain – Red Δ Gain – Blue	$82-0/5 $80-0/5	Fine tune the Red and Blue contrast levels.	Fine tune of the U and V gain levels.
V DC U DC	$7E-0/5 $7D-0/5	Must be set to 00.	Should nominally be set to 32. This sets the DC level of the U and V outputs at ≈ mid-scale.
Main Saturation	$86-0/5	Affects color saturation, except when the RGB inputs bypass this section (YX EN = 0).	Affects color saturation levels of the UV outputs. Does not affect the Y output.

9

Figure 36. Color Difference Stage and Outputs



The RGB and Y2 inputs are designed to accept standard 1.0 Vp-p analog video signals. They are not designed for TTL level signals. The color difference inputs are designed to accept signals ranging up to 1.8 Vp-p. All signals are to be capacitor-coupled as clamping is provided internally. Input impedance at these six pins is high.

For applications involving externally supplied color difference signals, sync can be supplied on the luma input (Y2), or it can be supplied separately at the RGB inputs. Where the color difference signals are obtained from the NTSC/PAL decoder, sync is provided to this section on the internal Y1 signal. See Sync Separator section for more details on injecting sync into the MC44011.

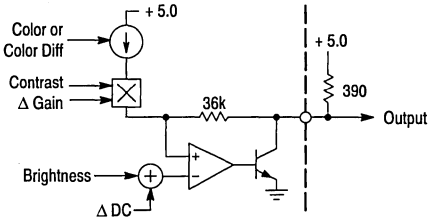
Sync is present on all three outputs in the RGB mode, and on the Y output only (Pin 21) in the YUV mode.

The Fast Commutate input (FC, Pin 25) is a logic level input with a threshold at ≈ 0.5 V. Input impedance is ≈ 67 kΩ, and the graph of Figure 24 shows the input current requirements. Propagation delay from the FC pin to the RGB/YUV outputs is ≈ 50 ns when enabling the RGB inputs, and ≈ 90 ns when disabling the inputs. (See Figure 29 Fast Commutate Timing diagram.) If Pin 25 is open, that is equivalent to a Logic 1, although good design practices dictate that inputs should never be left open. The voltage on this pin should not be allowed to go more the 0.5 V above V_{CC2} or below ground.

The three outputs (Pins 20 to 22) are open-collector, requiring an external pull-up. A representative schematic is shown in Figure 37.

The output amplitude can be varied from 100 mVp-p to 3.0 Vp-p by use of the contrast and saturation controls. Any output load to ground should be kept larger than 1.0 kΩ. In the RGB mode, DACs $7D and $7E should be set to 00, which results in clamping levels of ≈ +1.4 Vdc. In the YUV mode, DACs $7D and $7E should be set to 00, which results in clamping levels of ≈ +1.4 Vdc. In the YUV mode, the DACs should be set to 32 to bias the U and V outputs to ≈ +2.3 V. The Y output clamp will remain at ≈ +1.4 V in the YUV mode.

Figure 37. Output Stage



Horizontal PLL (PLL1)

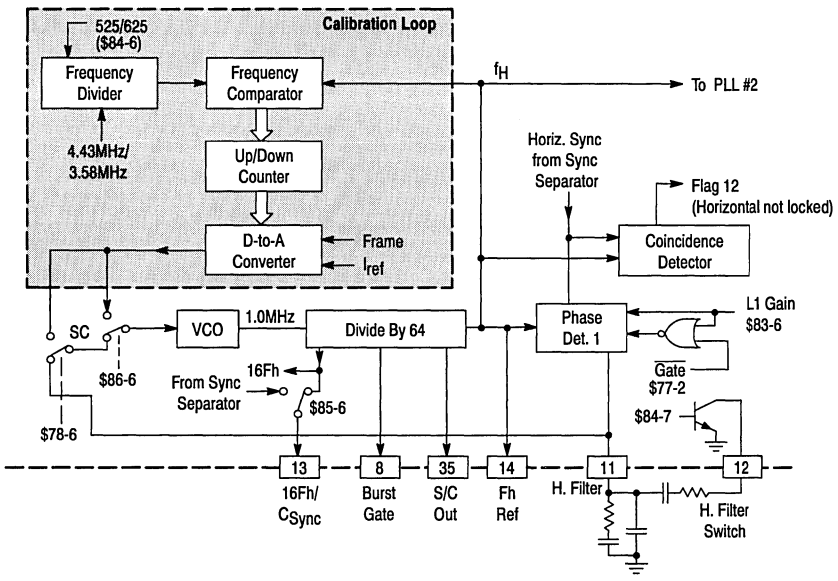
PLL1 (shown in Figure 38) provides several outputs which are phase-locked to the incoming horizontal sync. In normal operation, the two switches at the left side of Figure 38 are as shown, and (usually) the transistor at Pin 12 is off.

The phase detector compares the incoming sync (from the sync separator) to the frequency from the ÷ 64 block. The phase detector's output, filtered at Pin 11, controls the VCO to set the correct frequency (≈1.0 MHz) so that the output of the ÷ 64 is equal to the incoming horizontal frequency.

The line-locked outputs are:

1) **Fh Ref** (Pin 14) – A square wave, TTL levels, at the horizontal frequency, and phase-locked to the sync source according to the timing diagram of Figures 25 and 27.
2) **Burst Gate** (Pin 8) – This is a positive going pulse, TTL levels, coincident with the burst signal. See the timing diagram of Figures 25 and 27.

Figure 38. Horizontal PLL (PLL1)



3) **Sandcastle Output** (Pin 35) – This is a multilevel output, at the horizontal frequency, used by the MC44140 delay line. See the timing diagram of Figures 25 and 27.
4) **16Fh/C_{Sync}** (Pin 13) – This is a dual purpose output, TTL levels, user selectable. When Bit $85-6 is set to 0, Pin 13 is a square wave at 16x the horizontal frequency (250 kHz for PAL, ≈ 252 kHz for NTSC). When Bit $85-6 is set to 1, Pin 13 is negative composite sync, derived from the internal sync separator. See the timing diagram of Figures 25 and 27.

The first three outputs mentioned above, and Pin 13 when set to 16 Fh, are consistent, and do not change duty cycle or wave shape during the vertical sync interval. These four outputs will also be present regardless of the presence of a video signal at the selected input.

When Pin 13 is set to C_{Sync} output, it follows the incoming composite sync format. If there is no video signal present at the selected input, this output will be a steady logic high.

Loading on these pins should not be less than 2.0 kΩ to either ground or + 5.0 V.

Pin 11 is the filter for the PLL, and requires the components shown in Figure 38, and with the values shown in the application circuit of Figure 42. Pin 12 is a switch which allows the filtering characteristics at Pin 11 to be changed. Switching in the additional components (set $84-7 =1) increases the filter time constant, permitting better performance in the presence of noisy signals.

The gain of the phase detector may be set high or low, depending on the jitter content of the incoming horizontal frequency, by using Bit $83-6. Broadcast signals usually have a very stable horizontal frequency, in which case the low gain setting ($83-6 = 0) should be used. When the video source is, for example, a VCR, the high gain setting may be preferable to minimize instability artifacts which may show up on the screen.

The gating function ($77-2) provides additional control where the stability of the incoming horizontal frequency is in question. With this bit set to 0, gating is in effect, causing the phase detector to not respond to the incoming sync pulses during the vertical interval. This reduces disturbances in this PLL due to the half-line pulses and their change in polarity. The gating may be disabled by setting this bit to 1 where the timing of the incoming sync is known to be stable. The gating cannot be enabled if the phase detector gain is set high ($83-6 = 1).

Calibration Loop

The calibration loop (upper left portion of Figure 38) maintains a near correct frequency of this PLL in the absence of incoming sync signals. This feature minimizes re-adjustment and lock time when sync signals are re-applied. The calibration loop is similar to the PLL function, receiving one frequency from the crystal (either 4.43 MHz or 3.58 MHz) divided down to a frequency similar to the standard horizontal frequency. Bit $84-6 is used to set the frequency divider to the correct ratio, depending on which crystal is selected (see Table 9). The output of the frequency comparator operates an up/down counter, which in turn sets the D-to-A converter to drive the VCO through switch Sc. The resulting frequency at the output of the divide-by-64 block is then fed to the frequency comparator to complete the loop.

When a sync signal is not present at Phase Detector #1, and at the Coincidence Detector, as indicated by the coincidence detector's output (Flag 12), Bit $78-6 should be set to 0. This will cause the switch (Sc) to transfer to the D-to-A converter for two lines (lines 4, 5) in each vertical field, and will maintain the PLL1 at a frequency near the standard horizontal frequency (between 14 to 16 kHz). When lock to an incoming sync is established, Bit $78-6 may be set to 1, disabling the periodic recalibration function, or it may be left set to 0.

If a more accurate horizontal frequency is desired in the absence of an input signal, Bit $86-6. can be set to 1 (and Bit $84-6 set according to Table 9). This holds the horizontal frequency to ≈ 15.7 kHz. In this mode, Flag 12 will stay 0, as the PLL will not be able to lock-up to a newly applied external signal. To reset the system, set $86-6 to 0, write $00 to register $00, and then check Flag 12 to determine when the loop locks to an incoming signal.

Table 9. Calibration Loop

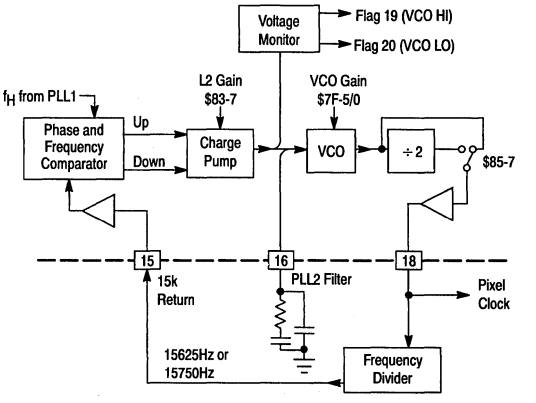
Crystal	Set Bit $84-6 to
14.3 MHz	1
17.7 MHz	0

On initial power up, Bit $86-6 (PLL1 EN) is automatically set to 1, engaging the calibration loop continuously. This condition will remain until this bit is set to 0, and $00 is written to register $00, as part of the initialization routine.

Pixel Clock PLL (PLL2)

The second PLL, depicted in Figure 39, generates a high frequency clock which is phase-locked to the horizontal frequency.

Figure 39. Pixel Clock PLL (PLL2)



The phase and frequency comparator receive inputs from PLL1 (f_H, the horizontal frequency), and the frequency returned from the external divider. Any difference between these two signals causes the Up or Down output to change the charge pump's timing. The charge pump output is composed of two equal current sources which alternately source and sink current to the filter at Pin 16. The voltage at Pin 16 (which is the input to the VCO) is therefore determined by the relative timing of those two current sources, and the filter characteristics. A coarse control of the loop gain is set with Bit $83-7. Low gain is obtained by setting this bit to a 1, which sets the charge pump's output current sources to ≈ ± 20 µA. Setting this bit to 0 sets the current sources to ≈ ± 50 µA, or high gain.

Depending on the output frequency desired, and whether or not a 50-50 square wave is needed at the pixel clock, the ÷2 may be engaged (Bit $85-7). Generally, the ÷ 2 should not be engaged for high frequencies, and should be engaged for low frequencies, so as to keep the VCO's input voltage in a comfortable range (between 1.7 and 3.3 V). If the input voltage is outside this range, Flag 19 or 20 will switch high, indicating the need to fine tune the VCO's gain (control DAC $7F). The usable adjustment range for this DAC is 00 to ≈ 50. Settings of 51 to 62 will generally produce non-square wave outputs, and can be unstable. A setting of 63 will shut off the VCO, which should be done if the pixel clock is not used. When not used, Pin 18 will be at a constant low level.

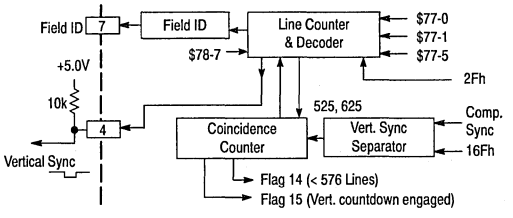
The pixel clock frequency is equal to the horizontal frequency (f_H) x the frequency divider ratio. The frequency divider can be made up of programmable counters (e.g. MC74F161A Applications Information), or it can be integrated into another device (e.g., an ASIC). The returned signal to Pin 15 must be TTL/CMOS logic levels, and must have a low time of > 200 ns. The phase comparator will phase-lock the falling edge of the returned signal with the rising edge of the f_H signal at Pin 14 (see Figure 32).

Vertical Decoder

The vertical decoder section, depicted in Figure 40, provides a vertical sync pulse and a field identification signal, as well as flags which indicate if vertical lockup has occurred, and if the number of horizontal lines per frame is greater or less than 576.

Inputs to this section consists of the composite sync from the sync separator, and horizontal related signals from the horizontal PLL (PLL1).

Figure 40. Vertical Decoder



The sync output (Pin 4) is an active low signal which starts after the horizontal half-line sync pulses change polarity (see Figures 33 and 34). The pulse width is nominally 500 µs for both PAL and NTSC signals. The position of this sync pulse's leading edge can be altered slightly with Bit $78-7, but this does not change the pulse width. Since the pulse width is generated digitally by counters, it will not vary with temperature, supply voltage, or manufacturing distribution. The sync output is an open-collector NPN output, requiring an external pull-up resistor. Minimum value for the pull-up is 1.0 kΩ, with 10 kΩ recommended for most applications.

Flag 14 (< 576 lines) is derived from the counter which compares the number of horizontal lines in each frame with a preset value of 576. This flag can be used externally to help determine whether PAL or NTSC signals are being provided to the MC44011. Flag 15 (Vertical countdown engaged) indicates that the vertical decoder has locked-up to the incoming composite sync information for eight consecutive fields (CB1, CA1 = 11).

The operation of the vertical decoder is controlled by Bits $77-0 and $77-1, according to Table 10.

Table 10. Vertical Decoder Mode

CB1 ($77-1)	CA1 ($77-0)	Vertical Sync Mode
0	0	Force 625
1	0	Force 525
0	1	Injection Lock
1	1	Auto-Count

The Injection Lock mode has a quicker response time, but less noise immunity, than the Auto-Count mode, and is normally used when attempting to lock-up to a new signal (such as when changing video input selection). Flag 15 will not switch high when in this mode. The Auto-Count mode, having a higher noise immunity, should be set once the horizontal PLL is locked-up (by reading Flag 12), and then Flag 15 should be checked after 8 fields for vertical lock-up.

The modes designated Force 525 and Force 625 can be used for those cases where it is desired to force the vertical sync pulse to occur twice every 525 or 625 lines, regardless of the incoming signal. In either of these modes, the MC44011's vertical section will not lock-up to the vertical sync information contained in the incoming composite video signal. If there is no incoming video signal, the vertical sync will still occur every 525 or 625 lines generated by the horizontal PLL. Flag 14 will indicate the number of lines selected, and Flag 15 will be a steady high.

Bit $77-5 (FSI) is used only in the PAL mode to select the vertical sync output rate. With this bit set to 0, the vertical sync pulses will be synchronized with the composite vertical sync input (every 20 ms). With this bit set to 1, the MC44011 will add a second vertical output sync pulse 10 ms after the one occurring at the vertical interval, giving a vertical sync rate of 100 Hz.

The Field ID output (Pin 7) indicates which field is being processed when interlaced signals are applied, but the polarity depends on Bit $78-7. Table 11 indicates Pin 7 output. When non-interlaced signals are being processed, Pin 7 will be a constant high level when $78-7 is set to 1, and will be a constant low level when $78-7 is set to a 0. Loading on Pin 7 should not be less than 2.0 kΩ to either ground or + 5.0 V. Figures 33 and 34 indicate the timing.

Table 11. Field ID Output

36/68 µs ($78-7)	Field	Field ID (Pin 7)
1	1	High
1	2	Low
0	1	Low
0	2	High

Sync Separator

The sync separator block provides composite sync information to the horizontal PLL, and to various other blocks within the MC44011 from one of several sources. It also provides composite sync output at Pin 13 when Bit $85-6 = 1. The sync source is selectable via the I²C bus according to Table 12.

Table 12. Sync Source

V_{in} Sync ($86-7)	Y2 Sync ($87-7)	RGB Sync ($88-6)	Sync Source
0	0	0	None
0	0	1	RGB (Pins 26 – 28)
0	1	0	Y2 (Pin 29)
1	X	X	Comp. Video (Pins 1, 3)

Setting Bit $86-7 to a 1 overrides the other bits, thereby deriving the sync from the composite video input (either Pin 1 or 3) selected by Bit $88-7.

When RGB is selected, sync information on Pins 26 to 28 is used. Sync may be applied to all three inputs, or to any one with the other two AC grounded. If RGB signals are applied to these pins, sync may be present on any one or all three.

When Y2 is selected, sync information on Pin 29 is used. The sync amplitude applied to any of the above pins must be greater than 100 mV, and it must be capacitor coupled.

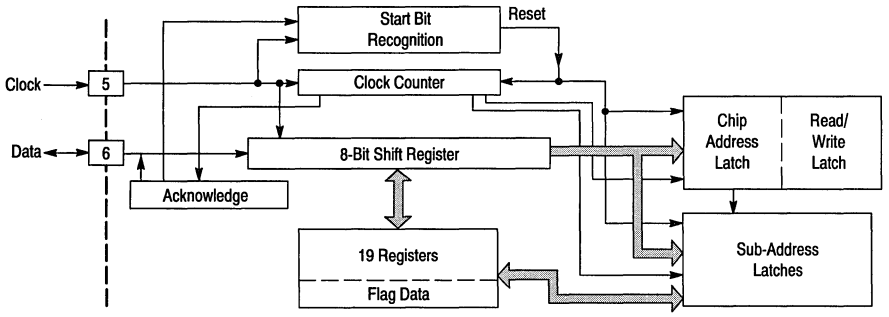
This system allows a certain amount of flexibility in using the MC44011, in that if the sync information is not present as part of the applied video signals, sync may be applied to another input. In other words, the input selected for the sync information need not be the same as the input selected for the video information.

SOFTWARE CONTROL OF THE MC44011

I²C Interface

Communication to and from the MC44011 follows the I²C interface arrangement and protocol defined by Phillips Corporation. In simple terms, I²C is a two line, multimaster bidirectional bus for data transfer. See Appendix C for a description of the I²C requirements and operation. Although an I²C system can be multimaster, the MC44011 never functions as a master.

Figure 41. I²C Bus Interface and Decoder



The MC44011 has a write address of $8A, and a flag read address of $8B. It requires that an external microprocessor read the internal flags, and then set the appropriate registers. The MC44011 does not do any automatic internal switching when applied video signals are changed. A block diagram of the I²C interface is shown in Figure 41. Since writing to the MC44011's registers can momentarily create jitter and other undesirable artifacts on the screen, writing should be done only during vertical retrace (before line 20). Reading of flags, however, can be done anytime.

Write to Control Registers

Writing should be done only during vertical retrace. A write cycle consists of three bytes (with three acknowledge bits):

1. The first byte is always the write address for the MC44011 ($8A).
2. The second byte defines the sub-address register (within the MC44011) to be operated on ($77 through $88, and $00).
3. The third byte is the data for that register.

Communication begins when a start bit (data taken low while clock is high), initiated by the master, is detected, generating an internal reset. The first byte is then entered, and if the address is correct ($8A), an acknowledge is generated by the MC44011, which tells the master to continue the communication. The second byte is then entered, followed by an acknowledge. The third byte is the operative data which is directed to the designated register, followed by a third acknowledge.

Sub-Address Registers

The sub-addresses of the 19 registers are at $77 through $88, and $00. 14 of the registers use Bits 0-5 to operate DACs which provide the analog adjustments. Most of the other bits are used to set/reset functions, and to select appropriate inputs/outputs. Table 13 indicates the assignments of the registers.

Table 13. Sub-Address Register Assignments

Sub Address	7	6	5	4	3	2	1	0
$77	S-VHS Y	S-VHS C	FSI	$\overline{\text{L2 GATE}}$	$\overline{\text{BLCP}}$	$\overline{\text{L1 GATE}}$	CBI	CAI
$78	36/38 µs	Cal Kill	(R-Y)/(B-Y) adjust DAC					
$79	HI	VI	Subcarrier balance DAC					
$7A	Xtal	SSD						
$7B	T1	T2						
$7C	SSC	SSA						
$7D	P1	SSB	Blue bias for YUV operation DAC					
$7E	P3	P2	Red bias for YUV operation DAC					
$7F	D3	D1	Pixel Clock VCO Gain adjust DAC					
$80	$\overline{\text{RGB EN}}$	D2	Blue Contrast trim DAC					
$81	Y2 EN	Y1 EN	Main Contrast DAC					
$82	YUV EN	YX EN	Red Contrast trim DAC					
$83	L2 Gain	L1 Gain	Blue Brightness trim DAC					
$84	H Switch	525/625	Main Brightness DAC					
$85	PClk/2	C Sync	Red Brightness trim DAC					
$86	V_{in} Sync	$\overline{\text{PLL1 En}}$	Main Saturation DAC (Color Difference section)					
$87	Y2 Sync	0	(R-Y)/(B-Y) Saturation balance DAC (Decoder section)					
$88	V2/V1	RGB Sync	Hue DAC					
$00	Set to $00 to start Horizontal Loop if $88-6 = 0							

Table 14 is a brief explanation of the individual control bits. A more detailed explanation of the functions is found in the block diagram description of the text (within the Functional Description section). Table 15 provides an explanation of the DACs. Each DAC is 6 bits wide, allowing 64 adjustment steps. The proper sequence and control of the bits and DACs, to achieve various system functions, is described in the Applications Information section.

Table 14. Control Bit Description

Control Bit	Name	Description
$77-7	S-VHS-Y	Set to 0 for normal Composite Video inputs at V1 and/or V2 (Pins 1, 3). Set to 1 for S-VHS (YC) operation. When 1, the Y-input at the selected video input (V1 or V2, selected by Bit $88-7) bypasses the initial luma delay line, and associated luma/chroma filters and peaking. The signal passes through the second luma delay, adjustable with Bits D1-D3. Luma is output at Pin 33.
$77-6	S-VHS-C	Set to 0 for normal Composite Video inputs at V1 and/or V2 (Pins 1, 3). Set to 1 for S-VHS (YC) operation. When 1, the chroma input at the non-selected video input (V1 or V2 by Bit $88-7) is directed to the ACC loop and PAL/NTSC detector. Color difference signals are then output at Pins 41 and 42.
$77-5	FSI	Set to 0 for a Vertical Sync output rate of 50 Hz. Set to 1 for 100 Hz. Useable in PAL systems only.
$77-4	$\overline{\text{L2 GATE}}$	When set to 0, the pixel clock charge pump (PLL2) operation is inhibited during the Vertical Retrace to minimize momentary instabilities. When set to 1, PLL2 operation is not inhibited.
$77-3	$\overline{\text{BLCP GATE}}$	When 0, Vertical Gating of the black level clamp pulse during the Vertical Retrace occurs to minimize momentary instabilities. The Vertical Gating can be inhibited by setting this bit to 1.
$77-2	$\overline{\text{L1 GATE}}$	When set to 0, the horizontal PLL's phase detector (PLL1) operation is inhibited during the Vertical Retrace to minimize momentary instabilities. When set to 1, the phase detector is not inhibited. If PLL1 gain is high (Bit $83-6 = 1), gating cannot be enabled.
$77-1, 0	CB1, CA1	Sets the Vertical Timebase operating method according to Table 10.
$78-7	36/68 µs	When 0, the time delay from the sync polarity reversal within the Composite Sync to the leading edge of the Vertical Sync output (Pin 4) is 36 µs. When 1, the time delay is 68 µs. (See Figure 33 and 34).
$78-6	CalKill	When 0, the Horizontal Calibration Loop is enabled for two lines (lines 4 and 5) in each field. When 1, the Calibration Loop is not engaged. Upon power-up, this bit is ineffective (Calibration Loop is enabled) until bit $86-6 is set to 0, and register $00 is set to $00.
$79-7	HI	This bit is not used in the MC44011, and must be set to 1.
$79-6	VI	This bit is not used in the MC44011, and must be set to 1.
$7A-7	Xtal	When 0, the crystal at Pin 38 (17.7 MHz) is selected. When 1, the crystal at Pin 36 (14.3 MHz) is selected.
$7A-6	SSD	This bit is not used in the MC44011, and must be set to 0.
$7B-7, 6	T1, T2	Used to set the Sound Trap Notch filter frequency according to Table 3.
$7C-7, 6 $7D-6	SSC, SSA, SSB	Sets the NTSC/PAL decoder to the correct system according to Table 4.
$7D-7 $7E-7, 6	P1, P2, P3	Sets the Luma Peaking in the decoder section according to Table 5. (See text).
$7F-7, 6 $80-6	D3, D1, D2	Sets the Luma Delay in the decoder section according to Table 6. (See text).
$80-7	$\overline{\text{RGB EN}}$	When 0, permits the RGB inputs (Pins 26 to 28) to be selected with the Fast Commutate (FC) input (Pin 25). When 1, the FC input is disabled, preventing the RGB inputs from being selected. When the RGB inputs are selected, the Color Difference inputs (Pins 30, 31) are deselected.
$81-7	Y2 EN	When 1, the Y2 Luma input (Pin 29) is selected. When 0, it is deselected.
$81-6	Y1 EN	When 1, the Y1 Luma Signal (provided by the decoder section to the color difference section) is selected. When 0, it is deselected.
$82-7	YUV EN	When 0, Pins 20 to 22 provide RGB output signals. When 1, those pins provide YUV output signals.
$82-6	YX EN	Effective only when the RGB inputs are selected. When 0, the RGB inputs (Pins 26 to 28) are directed to the RGB outputs (Pins 20 to 22) via the Contrast and Brightness controls. When 1, the RGB inputs are directed through the Color Difference Matrix, allowing Saturation control in addition to the Brightness and Contrast controls. See Figure 36.
$83-7	L2 Gain	When 0, the gain of the pixel clock VCO (PLL2) is high (50 µA). When 1, the gain is low (20 µA).
$83-6	L1 Gain	When 0, the Horizontal Phase Detector Gain (PLL1) is low. When 1, the gain is high.
$84-7	H Switch	When 0, Pin 12 is open. When 1, Pin 12 is internally switched to ground, allowing the PLL1 filter operation to be adjusted for noisy signals.

Table 14. Control Bit Description (continued)

Control Bit	Name	Description
$84-6	525/625	This bit sets the division ratio from the crystal for the reference frequency for the Horizontal Calibration Loop. For NTSC systems, set to 1. For PAL systems, set to 0.
$85-7	PClk/2	When 0, the PLL2 VCO provides the Pixel Clock at Pin 18 directly. When 1, the VCO output is directed through a ÷ 2 stage, and then to Pin 18.
$85-6	C Sync	When 0, Pin 13 will provide a square wave of ≈ 250 kHz (16 x Fh). When 1, Pin 13 provides a negative composite sync signal. See Figures 25, 27, 30, 31.
$86-7	V_{in} Sync	When 1, Composite Sync at the selected Video input (Pin 1 or 3) is used for all internal timing. When 0, the Sync source is selected by Bits $87-7 and $88-6. See Table 12.
$86-6	PLL1 Enable	After power up, this bit must be set to 0, and then register $00 set to $00, to enable the Horizontal Loop (PLL1). Setting this bit to a 1 will disable the Horizontal Loop, and engages the Calibration Loop.
$87-7	Y2 Sync	When 1, and $86-7 = $88-6 = 0, Composite Sync at the Y2 input (Pin 29) is used for all internal timing. When 0, the Sync source is selected by Bits $86-7 or $88-6. See Table 12.
$87-6	0	This bit must always be set to 0.
$88-7	V2/V1	When Composite Video is applied, and this bit is 0, the Video 2 input (Pin 3) is directed to the Sound Trap. When 1, the Video 1 input (Pin 1) is selected. In S-VHS applications, when 0, Pin 3 is the Y (luma) input, and Pin 1 is the chroma input. When this bit is 1, Pin 1 is the luma input, and Pin 3 is the chroma input.
$88-6	RGB Sync	When 1, and $86-7 = $87-7 = 0, Composite Sync at any or all of the RGB inputs (Pin 26 to 28) is used for all internal timing. When 0, the sync source is selected by Bits $86-7 or $87-7. See Table 12.

Table 15. Control DAC Description

Control Bits	Description
$78-5/0	This DAC allows for a relative gain adjustment of the R-Y and B-Y outputs (Pins 41, 42) as a means of adjusting the color decoding accuracy. Nominal setting is 32.
$79-5/0	Used to balance out reference errors of the color subcarrier, primarily for NTSC. Nominal setting is 32. Adjustment range is ≈ ± 5°.
$7D-5/0	Used to set the U (Pin 22) DC bias level. When in the YUV mode ($82-7 = 1), this setting should nominally be 32. When in RGB mode, set to 00.
$7E-5/0	Used to set the V (Pin 22) DC bias level. When in the YUV mode ($82-7 = 1), this setting should nominally be 32. When in RGB mode, set to 00.
$7F-5/0	Used to fine tune the gain of the Pixel Clock VCO to obtain optimum performance without instabilities. A setting of 63 will shut off the VCO. Setting 50 to 62 provide non-square wave outputs, and can be unstable. As the setting is increased from 00 to 49, the gain is increased. Changing this register does not change the Pixel Clock frequency.
$80-5/0	Used to fine tune the contrast of the Blue output when in RGB mode. In YUV mode this provides a fine tuning of the color, similar to, but not to be confused with, hue.
$81-5/0	Used to adjust the gain of the three outputs. In RGB mode this is the Contrast control.
$82-5/0	Used to fine tune the contrast of the Red output when in RGB mode. In YUV mode this provides a fine tuning of the color, similar to, but not to be confused with, hue.
$83-5/0	Used to fine tune the brightness of the Blue output when in RGB mode. In YUV mode this provides a fine tuning of the color, similar to, but not to be confused with, hue.
$84-5/0	Used to adjust the brightness of the three RGB outputs. In YUV mode this DAC affects only Y output (Pin 21).
$85-5/0	Used to fine tune the brightness of the Red output when in RGB mode. In YUV mode this provides a fine tuning of the color, similar to, but not to be confused with, hue.
$86-5/0	Used to adjust the saturation of the RGB/YUV outputs of the Color Difference section.
$87-5/0	Used to adjust the saturation of the R-Y, B-Y outputs (Pins 41, 42) of the Decoder section.
$88-5/0	Used to adjust the hue of the R-Y, B-Y outputs (Pins 41, 42). Nominal setting is 32.
$00-7/0	This register must be set to 00, after Bit $86-6 is set to 0, to enable the Horizontal Loop (PLL1) after power up, or anytime when Bit $86-6 is set to 0 after having been a 1.

The above DACs are 6-bits wide. The settings mentioned above, and in subsequent paragraphs are given in decimal values of 00 to 63. These are not hex values.

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Reading Flags

A read cycle need not be restricted to the vertical interval, but may be done anytime. A flag read cycle consists of three bytes (with three acknowledge bits):

- The first byte is always the Read address for the MC44011 ($8B).
- The second and third bytes are the flag data.

Communication begins when a start bit (data taken low while clock is high), initiated by the master (not the MC44011), is detected, generating an internal reset. The first byte (address) is then entered, and if correct, an acknowledge is generated by the MC44011. The flag bits will then exit the MC44011 as two 8 bit bytes at clock cycles 10-17 and 19-26. The master (receiving the data) is expected to generate the acknowledge bits at clocks 18 and 27. The master must then generate the stop bit.

The MC44011 flags must be read on a regular basis to determine the status of the various circuit blocks. The MC44011 does not generate interrupts. It is recommended the flags be read once per field or frame. See Table 16 for a description of the flags.

Table 16. Flag Description

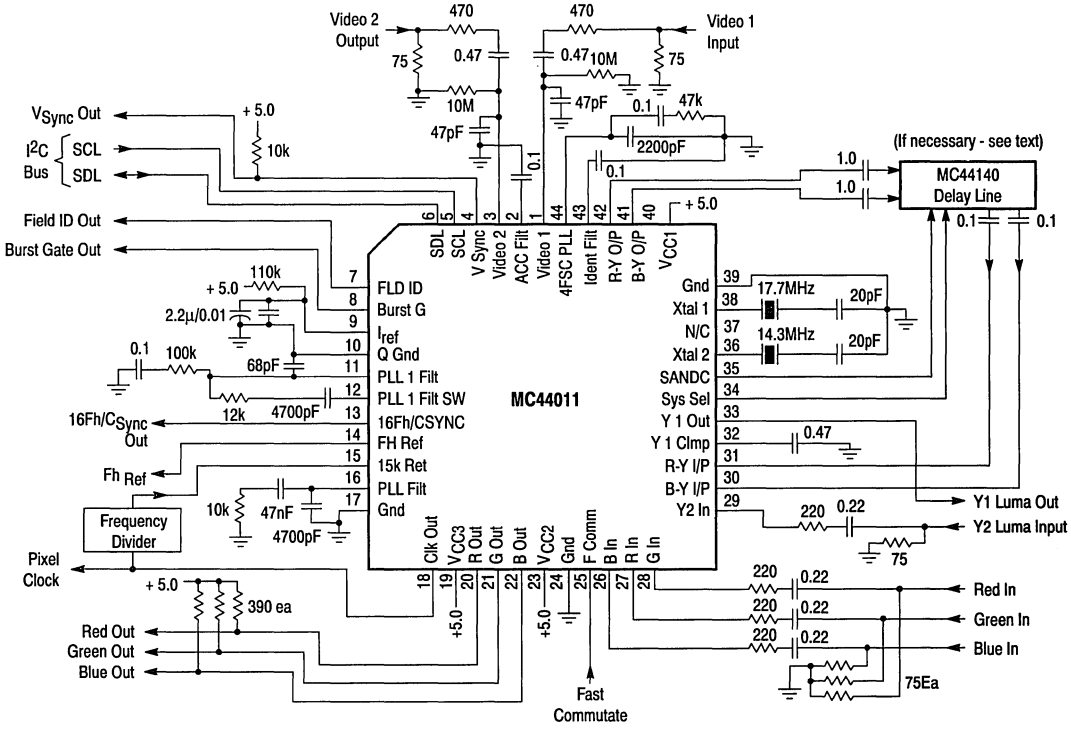
Clock No.	Description (When Flag = 1)
10	Internally set to a Logic 1.
11	Horizontal Loop (PLL1) enabled, indicating the loop can be driven by the incoming sync. This bit will be low upon power up, and will change to a 1 after initialization of control Bit $86-6 and register $00.
12	Horizontal Loop (PLL1) not locked. Lack of incoming sync, or wrong sync source selection, or the wrong horizontal frequency, will cause the Coincidence Detector to indicate a "not locked" condition.
13	Internally set to Logic 0.
14	Less than 576 horizontal lines counted per frame. This flag helps determine the applied video system. When high, a 525 line system (NTSC) is indicated. When low, a 625 line system (PAL) is indicated.
15	Vertical Countdown engaged. When high, this flag indicates the Vertical Countdown section has successfully maintained lock for 8 consecutive fields, indicating therefor a successful vertical lock-up. This flag is low in the Injection Lock mode.
16	Internally set to a Logic 1.
17	Internally set to a Logic 1.
18	(Acknowledge pulse).
19	Pixel clock VCO control voltage too low (< 1.7 V at Pin 16). This indicates the VCO may not function correctly as the control voltage is near one end of its range. The DAC setting at register $7F-5/0 must be increased, and/or the ÷ 2 block must be selected (set $85-7 = 1), to clear this flag.
20	Pixel clock VCO control voltage too high (> 3.3 V at Pin 16). This indicates the VCO may not function correctly as the control voltage is near one end of its range. The DAC setting at register $7F-5/0 must be reduced, and/or the ÷ 2 block must be deselected (set $85-7 = 0) to clear this flag. This flag will be high if the VCO is off (DAC $7F = 63).
21	Internally set to a Logic 1.
22	Internally set to a Logic 0.
23	ACC Loop is active, indicating it is locked up to the color burst signal. The Color Burst amplitude must exceed 30 mV_{p-p}, and the correct crystal selected, for lock-up to occur.
24	PAL system identified by the decoder, indicating the decoder recognizes the line-by-line change in the burst phase. When NTSC is applied, this flag is 0.
25	Not used.
26	Internally set to a Logic 0.
27	(Acknowledge pulse).

APPLICATIONS INFORMATION

Design Procedure and PC Board Layout

The external components required by the MC44011 are shown in Figure 42. Except for the crystals, all the components are standard value resistors and capacitors, and can be non-precision. Table 17 describes the external components for each pin.

Figure 42. Basic Functional Circuit



Crystal Specifications and Operation

The crystals used with the MC44011 should comply with Table 18 specifications.

Table 18. Crystal Specifications

Frequency: (4 x Subcarrier)	NTSC (14.31818 MHz) PAL (17.734472 MHz) PAL–M (14.30244 MHz)
Pull-in range:	± 1600 Hz (with respect to crystal frequency)
Tolerance:	30 ppm (with fixed load capacitor)
Temperature Coefficient:	50 ppm (with fixed load capacitor)
Operating Mode:	Fundamental series resonance
Load Capacitance:	Nominally 20 pF
Motional Capacitance:	10 to 30 fF
Series Resistance:	< 30 Ω (nominally 10 Ω)

The oscillator output resistance at Pin 36 is nominally 300 Ω for NTSC mode, and 400 Ω at Pin 38 for PAL mode. It is recommended that a stray capacitance (PC board, package pins, etc.) of 4.0 to 5.0 pF be included when selecting a crystal.

The above values for tolerance and temperature coefficent can be increased if a trimmer capacitor is used for the load capacitor.

The crystal PLL filter (Pin 44) voltage is between 1.8 and 3.8 V in normal operation. If the color output of the MC44011 is incorrect, or non-existent (ACC flag off), this voltage should be checked. If it is beyond either of the above limits, the capacitor in series with the crystal should be changed so as to allow the PLL to pull-in the crystal. The capacitor is generally specified by the crystal manufacturer, but should also comply with Table 18 specifications. If no burst is present, Pin 44 voltage will be ≈1.3 V.

The selected crystal frequency can be checked by using a scope at the non-selected crystal pin. The signal amplitude is nominally 200 to 400 mVp-p. In this way the selected crystal's frequency is not affected by the scope probe.

Table 17. External Components

Pin No.	Name	Function
1, 3	Video 1, Video 2	Input signals must be capacitor-coupled. The 470 Ω resistors protect the pins from ESD and RFI. The 75 Ω resistors are not required by the MC44011, but depend on the signal source. The 47 pF capacitors filter high frequency noise.
2	ACC Filter	The 0.1 µF ceramic capacitor filters the Automatic Gain circuit.
4	Vert. Sync	The pull-up resistor is required for this open-collector output.
5, 6	SCL, SDL	Pull-up resistors are required on each I^2C line since outputs are open-collector. They are typically located at the master device.
7	Field ID	No external components required.
8	Burst Gate	No external components required.
9	I_{ref}	The 110 kΩ resistor provides ≈ 32 µA from the + 5.0 V source. This pin must be well filtered to the Quiet Ground (Pin 10).
10	Quiet GND	This is the Reference Ground for Pin 9 and the PLL1 Filter.
11	PLL1 Filter	The 100 kΩ resistor, and the 0.1 µF and 68 pF capacitors are the filter network for this PLL. Connect to Pin 10 ground.
12	PLL1 Filt. SW	The 12 kΩ resistor and 470 pF capacitor give the filter a longer time constant when Pin 12 is switched in.
13	16 Fh/C_{Sync}	No external components required.
14	Fh Ref	No external components required.
15	15 k Return	TTL Return signal from external frequency divider.
16	PLL2 Filter	The 10 kΩ resistor and 47 nF and 4.7 nF capacitors are the filter network for this PLL. Connect to Pin 17 ground.
17	Ground	Ground for the Pixel Clock circuit.
18	Clk Out	Pixel Clock output to external frequency divider and triple A/D converter.
19	V_{CC3}	+ 5.0 V supply for the Pixel Clock circuit.
20, 21, 22	R, G, B Out	The 390 Ω pull-up resistors are required for these open-collector outputs. The pull-ups should go to a clean, well filtered + 5.0 V supply. These pins cannot drive 75 Ω directly. If required to do so, see text for suggested buffer.
23	V_{CC2}	+ 5.0 V supply for the Color Difference section.
24	Ground	Ground for the Color Difference section.
25	Fast Comm.	No external components required. This input *should not* be left open.
26, 27, 28	B, G, R In	Input signals must be capacitor-coupled. The 220 Ω resistors protect the pins from ESD and RFI.
29	Y2 Input	Input signals must be capacitor-coupled. The 220 Ω resistor protects the pin from ESD and RFI. The 75 Ω resistor is not required by the MC44011, but depends on the signal source.
30, 31	B-Y, R-Y In	Input signals must be capacitor-coupled. The MC44140 is required if PAL signals are processed (see text).
32	Y1 Clamp	The 0.1 µF ceramic capacitor provides clamping for the Y1 output.
33	Y1 Out	No external components required. This pin cannot drive 75 Ω directly. If required to do so, see text for suggested buffer.
34, 35	System Sel., Sandcastle	For use by the MC44140 delay line. No other external components required.
36, 38	Xtal 2, Xtal 1	A 17.7 MHz crystal is required (at Pin 38) for PAL signals, and a 14.3 MHz crystal is required (at Pin 36) for NTSC signals. If only one crystal is required, leave the other pin open. The series capacitor depends on the crystal manufacturer. (See Table 18 for crystal specs.)
37	N/C	No external components required.
39	Ground	Ground for Color Decoder section.
40	V_{CC1}	+ 5.0 V supply for the Color Decoder section.
41, 42	B-Y, R-Y Out	The MC44140 is required if PAL signals are processed. Otherwise, capacitor-couple to Pins 30, 31 (see text).
43	Indent. Filter	The 0.1 µF ceramic capacitor provides filtering for the Identification circuit.
44	4FSC PLL	The 47 kΩ resistor, and 0.1 µF and 2.2 nF capacitors are the filter network for the crystal PLL. Connect to Pin 39 ground.

Power Supplies and Ground

There are three V_{CC} pins (Pins 19, 23, and 40) which must be connected to a source of +5.0 V, ± 5%. Since the three pins are internally connected by diodes, none can be left open, even if a particular section (such as the Pixel Clock Generator) is to be unused. Total current required is ≈135 mA (including the RGB output load current). There are four ground pins (Pins 10, 17, 24, and 39) which must be connected together, and preferably connected to a ground plane.

Pins 19 and 17 are the V_{CC} and ground for the Pixel Clock Generator, and the circuitry associated with the Pixel Clock should be referenced to those two pins.

Pins 23 and 24 are the V_{CC} and ground for the Color Difference section, which includes the RGB outputs. The output pull-up resistors should be connected to the V_{CC} at Pin 23.

Pins 40 and 39 are the V_{CC} and ground for the Color Decoder, Sync Separator, Horizontal PLL and the Vertical Decoder. Pin 10 is the Quiet Ground for the horizontal PLL's VCO and filter, and therefore, the components on Pins 9 and 11 should be connected as close as possible to Pin 10.

Bypassing of the power supplies must be done as close as possible to each V_{CC} pin, and at the output pull-up resistors. Recommended bypassing components are a 10 µF tantalum capacitor in parallel with a 0.01µF ceramic.

Input Signals

The various video inputs, Video 1 and 2, Red In, Green In, Blue In, R-Y, B-Y, and Y2 inputs, are designed to accept standard level analog video waveforms. They are not designed for digital signals. The input impedance of the above pins is high. The need for 75 Ω terminations for those video signals depends on the video source itself. All of the above signals must be capacitor-coupled as clamping is provided internally.

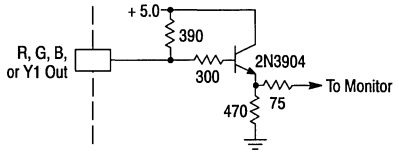
The I^2C inputs (SCL, SDL) are designed according to the I^2C specifications, which define V_{OL} as between 0 and 1.5 V, and V_{OH} as between 3.0 V to V_{CC}. See Appendix C.

The 15 k Return and Fast Commutate (Pins 15 and 25, respectively) are designed for TTL level signals. If unused, they should not be left open, but connected to + 5.0 V, or ground, as appropriate.

Output Signals

The RGB/YUV outputs are open-collector, and require pull-up resistors (typically 390 Ω) to a clean + 5.0 V (V_{CC2}). The output impedance is such that the load impedance (to ground) should be >1.5 kΩ. If it is desired to drive a 75 Ω load (e.g., a monitor) from these outputs, a simple buffer (see Figure 43) can be added.

Figure 43. Output Buffer



The Y1 output (Pin 33) has an output impedance of ≈ 300 Ω, and can be used as a monitoring point, or to drive the input of the MC44145 sync separator, or other high impedance loads (minimum load for Y1 is 1.0 kΩ). If it is to be used to drive a 75 Ω load, the buffer shown in Figure 43 can be used, *except the 390 Ω resistor must be deleted.*

The Vertical Sync output (Pin 4) is an open-collector logic level output, and requires a pull-up resistor to + 5.0 V. 10 kΩ is recommended, but it can be as low as 1.0 kΩ. The I^2C data line (SDL, Pin 6) is also open-collector when it is an output, and can sink a maximum of 3.0 mA. Only one pull-up resistor is required on the SDL line (regardless of the number of devices on that line), and it is typically near the master device. The Field ID, Burst Gate, 16 Fh/C_{Sync}, Fh Ref, and Pixel Clock outputs are logic level totem-pole outputs.

PC Board

The PC board layout should be neat and compact, and should preferably have a ground plane. If feasible, a second plane should be provided for the + 5.0 V supply, but this is not mandatory. The components at Pins 9 and 11 should be connected to the same ground track which goes to Pin 10. The V_{CC} and ground should be connected as directly as possible to the power supply, and not routed through a maze of digital circuitry before arriving at the MC44011. Since the MC44011 is intended to be used with A/D converters and high speed digital signals, it is expected digital circuitry will be on the same board. Care should be taken in the layout to prevent digital noise from entering the analog portions of the MC44011. The most sensitive pins are Pins 1,2, 3, 9, 10, 11, 12, 16, and 44, and should be protected from noise.

Initialization and Programming Information

Upon powering up the MC44011, initialization consists of first filling the registers with initial values to set a known condition. Table 19 provides recommended values for the initial settings, although these may be tailored for each application (with the exception of Bits $79-6,7, $7A-6, $86-6, and $87-6). Table 19 settings will set up the MC44011 to the following conditions:

- Composite video input at Video 1 (Pin 1), NTSC, using the crystal at Xtal 2 (Pin 36).
- Y1 enabled, RG outputs enabled, and Composite Sync at Pin 13
- RGB inputs not enabled (R-Y, B-Y inputs are enabled)
- The Sound Trap at 4.5 MHz
- The Luma Peaking at 0 dB
- The Luma Delay at minimum
- High gain and high noise rejection for the horizontal PLL
- Vertical decoder set to Injection Lock mode
- The Pixel Clock VCO is off

After the registers are initialized, then set Bit $86-6 to 0, and load register $00 with $00. This will enable the horizontal PLL, permitting normal operation.

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Table 19. Recommended Initial Settings

Sub Address	7	6	5	4	3	2	1	0
$77	S-VHS Y = 0	S-VHS C = 0	FSI = 0	$\overline{\text{L2 Gain}}$ = 0	$\overline{\text{BLCP}}$ = 0	$\overline{\text{L1 Gain}}$ = 0	CBI = 0	CAI = 1
$78	36/68 µs = 0	Calkill = 0	(R-Y)/(B-Y) Adjust DAC = 32					
$79	HI = 1	VI = 1	Subcarrier Balance DAC = 32					
$7A	Xtal =1	SSD = 0						
$7B	T1 =1	T2 = 1						
$7C	SSC = 0	SSA = 1						
$7D	P1 =1	SSB = 0	Blue Bias = 00					
$7E	P3 = 1	P2 = 1	Red Bias = 00					
$7F	D3 = 0	D1 = 0	Pixel Clock VCO Gain Adjust = 63					
$80	$\overline{\text{RGB EN}}$ = 1	D2 = 0	Blue Contrast Trim = 32					
$81	Y2 EN = 0	Y1 EN = 1	Main Contrast = 47					
$82	YUV EN = 0	YX EN = 0	Red Contrast Trim = 32					
$83	L2 Gain = 1	L1 Gain = 1	Blue Brightness Trim = 32					
$84	H Switch = 1	525/625 = 1	Main Brightness = 30					
$85	PClk/2 = 1	C_{Sync} = 1	Red Brightness Trim = 32					
$86	V_{in} Sync = 1	$\overline{\text{PLL1 EN}}$ = 1	Main Saturation (Color Difference section) = 32					
$87	Y2 Sync = 0	0	(R-Y)/(B-Y) Saturation Balance (Decoder section) = 15					
$88	V2/V1 = 1	RGB_{Sync} = 0	Hue = 32					

These settings are for power-up initialization only. Refer to the text, and Appendix B, for subsequent modifications based on the application.

Then, after selecting the desired input(s) (from Pins 1, 3, or 26 to 31), and based on the applied signals at those inputs, and by reading the flags, the registers are adjusted for the desired and proper mode of operation. A suggested routine for setting modes is given in Appendix B. The "initial values" in the Control DACs table of Appendix B are those in Table 19. The remainder of the flow chart is a recommendation only, and should be tailored for each application.

The monitoring of flags should be done on a regular basis, and it is recommended it be done once per field. See Table 16 (in the Functional Description section) for a summary of the flags. Should any flags change, the following procedures are recommended:

Flag 11 (Horizontal Enabled) – Once enabled by setting Bit $86-6 = 0, this flag should always remain a 1. Should it change to 0, reset $86-6 to 0, and write $00 to register $00 again. If the flag does not return to a 1, this indicates a possible device malfunction.

Flag 12 (Horizontal Out-of-Lock) – When 1, this indicates:

a) the wrong input is selected (Bits $88-7, $81-7, $80-7, and $77-7,6), or;

b) the wrong sync source is selected (Bits $86-7, $87-7, and $88-6), or;

c) the incoming signal is somewhat unstable, as from a VCR tape (change Bit $83-6), and/or;

d) the incoming signal is noisy (change Bit $84-7), or;

e) a loss of the incoming signal with sync.

(It is possible for this flag to flicker when the video signal is from a poor quality tape, or other poor quality source.)

Flag 14 (Less than 576 lines) – This flag, from the vertical decoder, is used to help determine if the signal is PAL or NTSC. Should it change, this indicates the incoming signal has changed format, or possibly one of the items listed under Flag 12 above.

Flag 15 (Vertical Countdown Engaged) – Bits 77-0 and 1 must be set to 1 (after Flag 12 reads 0) for this flag to indicate correctly. Then this flag will change to a 1 after 8 fields of successful synchronization of the internal counters with the incoming signal. To change to a 0 requires 8 consecutive fields of non-synchronization. If this flag changes to 0, this indicates a loss of signal, a change of signal format, or instability in the horizontal PLL.

Flags 19, 20 (VCO Control Voltage Low/High) – These flags are meaningful only if the Pixel Clock Generator is used. If Flag 19 is a 1, the gain of the pixel clock VCO needs to be increased by increasing the value of register $7F, and/or set Bit $85-7 =1. If Flag 20 is a 1, the value of the register must be decreased, and/or set Bit $85-7 = 0. If the VCO is turned off ($7F = 63), Flag 19 will be 0, and Flag 20 will be 1.

Flag 23 (ACC Active) – If this flag is a 0, it indicates the ACC loop is not active. This will happen if the burst signal is less than 30 mVp-p, if the incorrect crystal is selected ($7A-7), if the crystal PLL is not locked, or if the horizontal PLL is not locked.

Flag 24 (PAL Identified) – This flag is a 1 when PAL signals are applied, and a 0 when NTSC signals are applied, or when no burst is present.

It is recommended that the Color Decoder section, and crystal, should be set according to the state of Flags 14, 23, and 24 according to Table 20.

Table 20. Color Standard Selection Table

Flags			Bit Settings				
#14 <576 Lines	#23 ACC Active	#24 PAL Signal	Crystal	SSA ($7C-6)	SSB ($7D-6)	SSC ($7C-7)	System
X	0	X	Either	1	1	0	Color Kill
0	1	0	Either	1	1	0	Color Kill
0	1	1	17.7 MHz	0	1	0	PAL
1	1	0	14.3 MHz	1	0	0	NTSC
1	1	1	(Note 1)	0	1	0	PAL-M

NOTES: 1. PAL-M, used in Brazil and other South American countries, can be decoded by the MC44011, but requires a 14.3024 MHz crystal.
2. SSD ($7A-6) is always set to 0.

MISCELLANEOUS APPLICATIONS INFORMATION

Use of the MC44140 Delay Line

The MC44140 delay line is generally required if PAL signals are to be decoded, so as to average out the line-by-line color information associated with PAL color decoding. If the same single PAL video source is always used in a particular application, the delay line can be eliminated, and any slight phase errors can be corrected with the DAC of register $79-5/0. If, however, various video sources can be used, and/or if the video signal is less than broadcast quality, it is recommended the MC44140 delay line be included.

The MC44140 acts on the color difference signals before they enter the color difference stage of the MC44011. It will, however, pass NTSC signals through without modifications. The MC44011 uses the System Select output (Pin 34) to indicate to the delay line which signals are being processed. The System Select voltage is set when the color decoder is set with Bits SSA, SSB, SSC, SSD. The Sandcastle output (Pin 35) provides the horizontal timing signals to the delay line. In addition, the MC44140 uses the crystal frequency for the internal counters.

The MC44140 is inserted into the circuit between the Color Difference outputs and inputs of the MC44011. In addition, the MC44140 provides pins (Pins 8,9) for inserting an alternate source of color difference signals to the MC44011 by setting the System Select to external (Bit $7C-7 = 1). See Figure 44 for a suggested circuit.

If only NTSC signals are to be processed by the MC44011, the MC44140 is not needed. In this case, connect Pin 42 to Pin 31 with a 0.1µF capacitor, and similarly connect Pin 41 to Pin 30.

Figure 44. Incorporating the MC44140 Delay Line

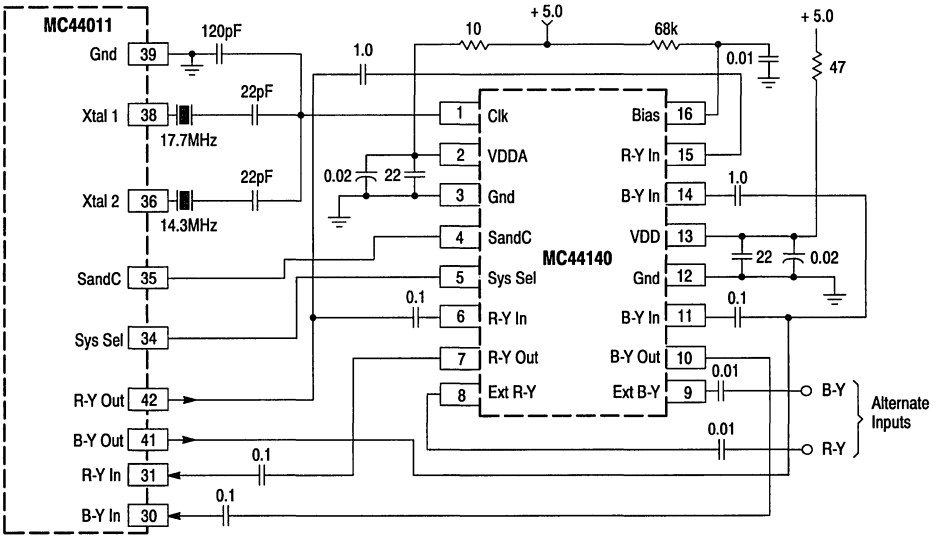
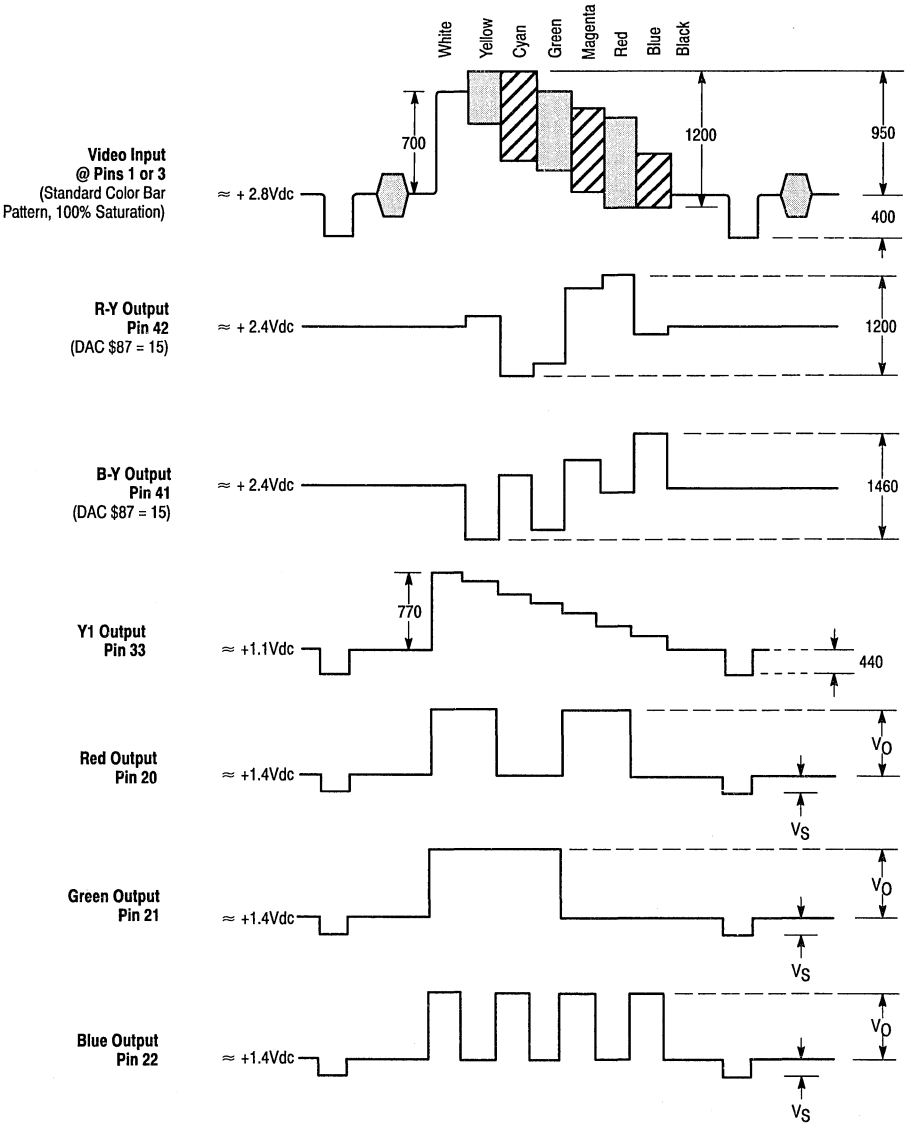


Figure 45. Typical Waveforms



DACs set per Table 19. All amplitudes in milliVolts.
Voltages are nominal, and do not represent guaranteed limits.

DAC 81	V_O	V_S
32	1725	220
47	2360	340
63	3160	440

Use of the MC44145 Pixel Clock Generator

For most applications the Pixel Clock Generator (PLL2) within the MC44011 will be suitable. In those cases, however, where the pixel clock frequency is set to within ±1.0 MHz of the selected crystal frequency (14.3 MHz or 17.7 MHz), or to within ±1.0 MHz of double the selected crystal frequencies, undesirable noise artifacts may be present on the RGB outputs. In these cases the MC44145 should be used to generate the Pixel Clock. The circuitry within the MC44145 duplicates that of the MC44011, but since it is physically removed from the circuitry within the MC44011, the interfering noise is not generated. If the MC44145 is used, the Pixel Clock Generator within the MC44011 should be shut off by setting the DAC of register $7F to 63, eliminating the components at Pin 16, and grounding Pin 16.

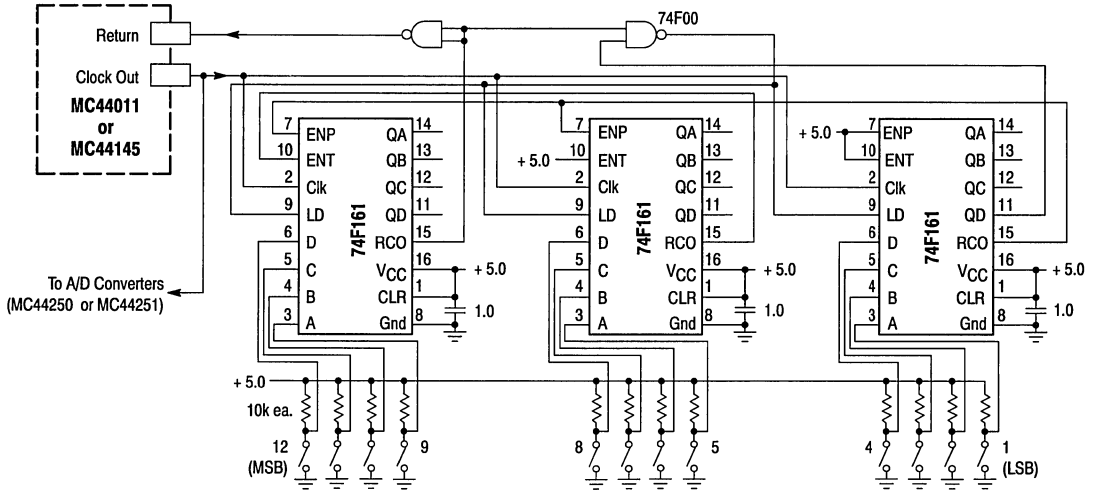
If the desired pixel clock frequency is close to the limits mentioned above, then experimentation may be used to determine the need for the MC44145.

Frequency Divider

The frequency of the Pixel Clock is determined by the horizontal frequency and an external frequency divider. The divider simply divides down the Pixel Clock Frequency so that it equals the horizontal frequency. The PLL within the MC44011 (or the MC44145) compares the horizontal frequency with the returned frequency, and adjusts the internal VCO accordingly, to achieve the proper relationship between the two. The PLL will phase-lock the negative-going edge of the returned signal with the positive-going edge of the Fh signal (Pin 14 of the MC44011). The returned signal must be TTL logic level amplitudes, and have a minimum low time of 200 ns. A suggested circuit for the divider, shown in Figure 46, uses 74F161 programmable binary counters. The 12 switches at the bottom are used to set the division ratio, and hence the Pixel Clock frequency.

The division ratio is determined by dividing the desired clock frequency by the horizontal frequency, and then using the closest whole number. After determining the binary equivalent of that number, close each switch corresponding to a 1, and leave open each switch corresponding to a 0. Alternately, the switches could be deleted, and Pins 3, 4, 5 and 6 of each 74F161 hard-wired to + 5.0 V or ground, or controlled by a microprocessor where different pixel clock frequencies are required.

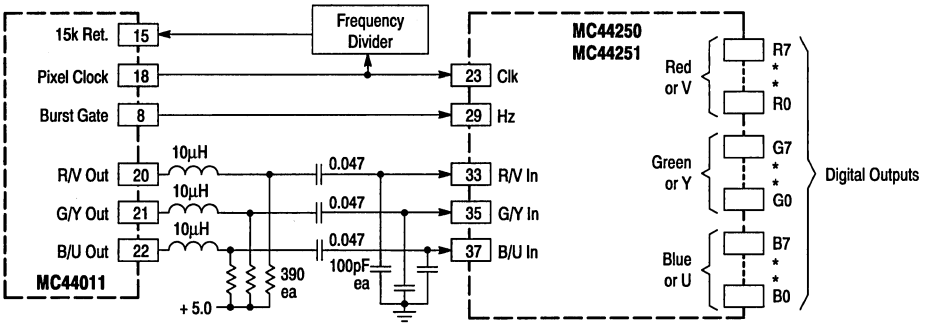
Figure 46. Suggested Frequency Divider



Connecting the MC44011 to the MC44250 or MC44251 A/D Converter

The MC44250 and MC44251 triple A/D converters are designed to accept RGB or YUV inputs, and provide 8-bit equivalents of each. Additionally, the inputs have black level clamps, allowing the input signals to be capacitor-coupled. The simplified schematic of Figure 47 shows the connections between the MC44011 and the MC44250/1, including anti-aliasing filters between the devices. Connection to other A/D converters would be done in a similar manner. Refer to the appropriate data sheet for details.

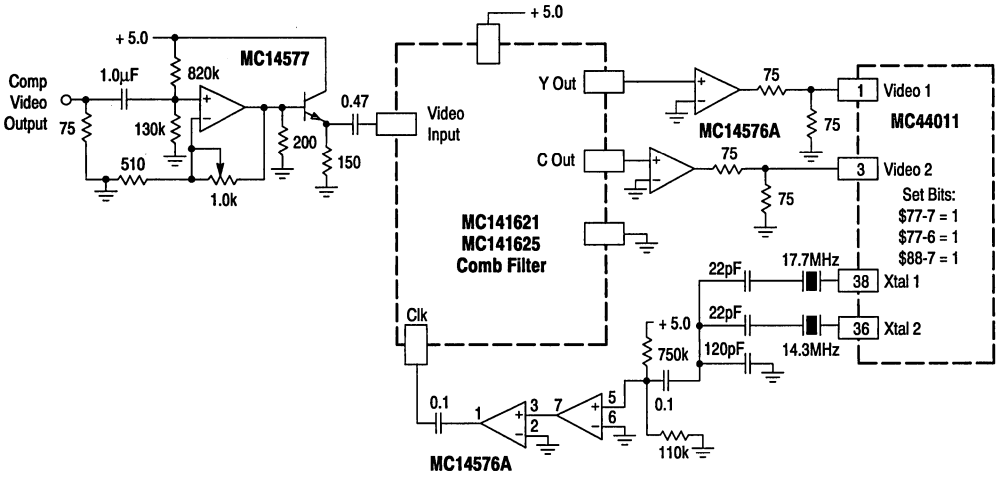
Figure 47. Connecting to a Triple A/D Converter



Connecting the MC44011 to the MC141621 or MC141625 NTSC Comb Filter

A comb filter can be used ahead of the MC44011 to enhance picture quality by providing a more accurate separation of the luma and chroma components from the composite video, without sacrificing bandwidth. The usual benefits are reduced dot crawl, and increased color purity. Figure 48 (a simplified schematic) shows the normal mode of implementing the MC141621 (NTSC) or MC141625 (PAL/NTSC) comb filter with the MC44011. The two comb filters can also provide the Y and C signals in digital format. Refer to their data sheets for details. The MC14576A op amps have an internally set gain of 2.

Figure 48. Implementing the Comb Filter



APPENDIX A

Control Bit Summary

	Bit 7	6	5	4	3	2	1	0
$77	S-VHS Y	S-VHS C	FSI	$\overline{L2\ Gate}$	$\overline{BLCP}$	$\overline{L1\ Gate}$	CBI	CAI
		0 = Comp. Video 1 = S-VHS	0 = 50 Hz 1 = 100 Hz	0 = PLL2 Gating	0 = Clamp Gating	0 = PLL1 Gating		
		Vertical Time Constant						
$78	36/68	CalKill	1 = Cal Loop Disabled					
$79	HI	V1	Set to 1, 1					
$7A	Xtal	SSD	Set to 0 1 = Pin 36 Crystal					
$7B	T1	T2						
$7C	SSC	SSA						
$7D	P1	SSB						
$7E	P3	P2						
$7F	D3	D1						
$80	$\overline{RGB\ EN}$	D2	0 = RGB Inputs Enabled					
$81	Y2 EN	Y1 EN	1 = Y1 Enabled 1 = Y2 Enabled					
$82	YUV EN	YX EN	1 = RGB Matrix Enabled 1 = YUV Outputs					
$83	L2 Gain	L1 Gain	1 = PLL1 Gain High 1 = PLL2 Gain Low					
$84	H Switch	525/625	1 = NTSC 1 = Switch Closed					
$85	PClk/2	C Sync	1 = Comp. Sync 1 = ÷ 2 Enabled					
$86	V_{in} Sync	$\overline{PLL1\ EN}$	0 = PLL1 Enabled 1 = Comp. Video Sync Source					
$87	Y2 Sync	0	Set to 0 1 = Y2 Sync Source					
$88	V2/V1	RGB Sync	1 = RGB Sync Source 1 = Pin 1 Input					

CBI	CAI	Sync Mode
0	0	Force 625
1	0	Force 525
0	1	Inj. Lock
1	1	Auto Count

Sound Trap Notch Frequency			
T1	T2	PAL	NTSC
0	0	6.5 MHz	5.25 MHz
0	1	5.5 + 5.75 MHz	4.44 + 4.64 MHz
1	0	6.0 MHz	4.84 MHz
1	1	5.5 MHz	4.44 MHz

SSA	SSB	SSC	Color System
0	0	0	Not Used
0	1	0	PAL
1	0	0	NTSC
1	1	0	Color Kill
X	X	1	External

P1	P2	P3	Y1 Peak
0	0	0	9.5 dB
0	0	1	8.5
1	0	0	7.7
1	0	1	6.5
0	1	0	5.3
0	1	1	3.8
1	1	0	2.2
1	1	1	0

			Luma Delay	
D1	D2	D3	14.3 MHz	17.7 MHz
0	0	0	690 ns	594 ns
0	0	1	760	650
0	1	0	830	707
0	1	1	900	763
1	0	0	970	819
1	0	1	1040	876
1	1	0	970	819
1	1	1	1040	876

Comp. Video Mode

Control DACs

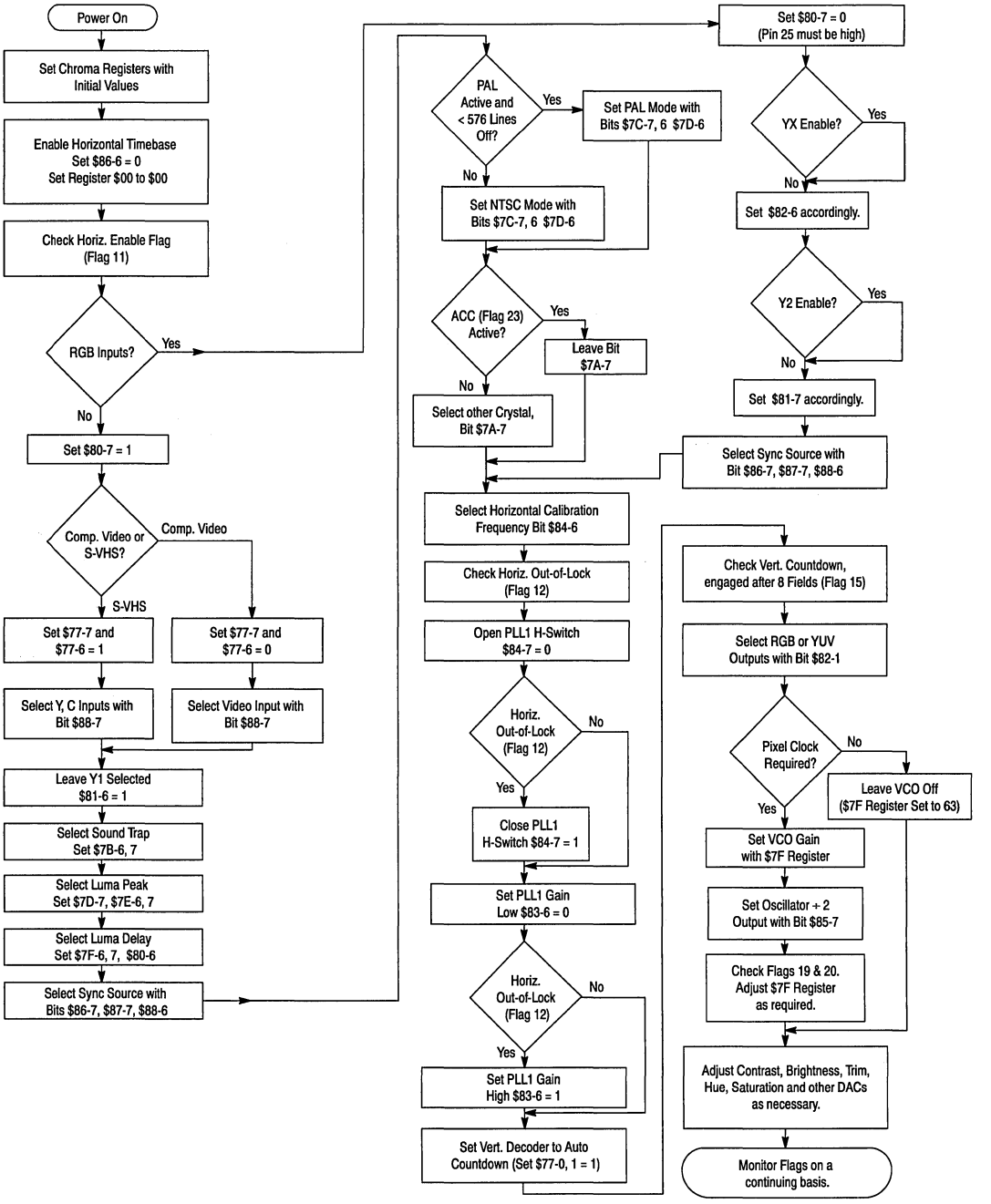
$78	R-Y/B-Y Gain Adjustment	$82	Red Contrast Trim
$79	Subcarrier Phase	$83	Blue Brightness Trim
$7D	Blue DC Bias	$84	Main Brightness
$7E	Red DC Bias	$85	Red Brightness Trim
$7F	Pixel Clock VCO Gain	$86	Saturation (Color Diff. Section)
$80	Blue Contrast Trim	$87	Saturation (Decoder)
$81	Main Contrast	$88	Hue

Flags

10	Internally Set to 1	19	Pixel Clock VCO Gain too low
11	Horizontal Loop (PLL1) Enabled	20	Pixel Clock VCO Gain too high
12	Horizontal Loop not Locked	21	Internally Set to 1
13	Internally Set to 0	22	Internally Set to 0
14	Less than 576 Lines	23	ACC Loop Active
15	Vertical Decoder Engaged	24	PAL Signals Detected
16	Internally Set to 1	25	Not Used
17	Internally Set to 1	26	Internally Set to 0

APPENDIX B

Suggested Mode Setting Routine (Simplified)



APPENDIX C

I²C Description

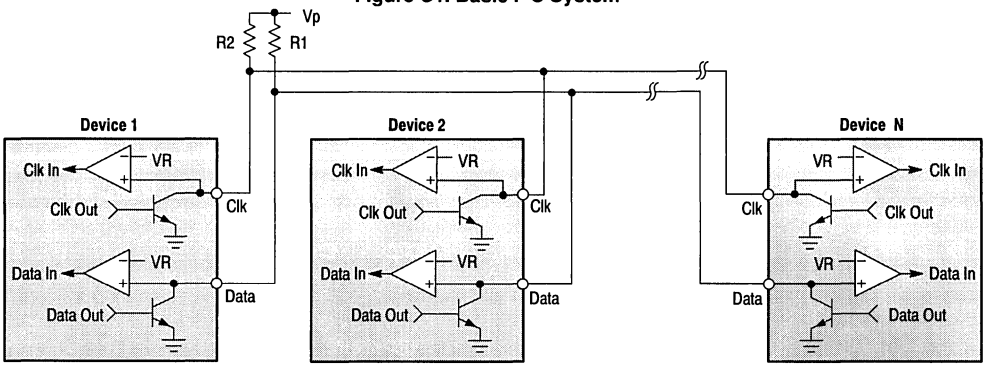
Introduction

The I²C system, a patented and proprietary system developed by Philips Corporation, defines a two-wire communication system. The number of devices in a system is limited only by the system capacitance and data rate. Each device is assigned two unique addresses — one for writing to it, and one for reading from it. Any device may act as a master by initiating a data transfer with any other device (the slave). Data transfer is in 8-bit bytes, and can be in either direction, but not in both directions in one data transfer operation.

Hardware Aspects

The system bus consists of two wires, Clock and Data. All devices must have open-collector (or open-drain) outputs. A single pull-up resistor is required on each line, as shown in Figure C1.

Figure C1. Basic I²C System



Devices such as the MC44011, which never act as a master, need not have the output drive transistor at the Clock pin. Nominal value for R1 and R2 is 10 kΩ, but can be different to account for system capacitance at high data rates. VR is a switching threshold for input signals.

The significant electrical characteristics are as follows:

- Maximum data rate (Clock frequency) is 100 kHz;
- V_{OL} max is 0.4 V when sinking 3.0 mA;
- V_{IL} max is 0.3 x Vp, but at least +1.5 V;
- V_{IH} min is + 3.0 V for a + 5.0 V system, or 0.7 x Vp for other supply voltages.
- The maximum input current at Clock and Data at V_{OL} max (when they are inputs) is −10 μA;
- The maximum input current at Clock and Data at 0.9 x Vp (when they are inputs) is +10 μA;
- The maximum pin capacitance is 10 pF;
- Maximum bus capacitance is 400 pF.

Data Transfer

Prior to initiating a data transfer, both lines must be high (all drive transistors off). A device which initiates a data transfer assumes the role of the master, and generates a START condition by taking the Data line low while Clock is still high. At this time, all other devices become listeners. The master will supply the clock for the entire sequence.

The master then sends the 8-bit address by operating both the clock and data lines. Data must be stable during the clock's high time, and can change during the clock's low time. The MSB is sent first. The address must end in a 0 if it is a Write operation (data transfer from master-to-slave), and it must end in a 1 if it is a Read operation.

At the 9th Clock Pulse, the master must release the Data line high, and the slave must provide an acknowledge bit by pulling Data low during this clock time. If the master does not receive a proper acknowledge, it can terminate the operation.

After the first acknowledge, the role of the two devices depends on whether it is a Write or a Read operation, but the master always supplies the clock.

- In a Write operation the master is the transmitter, and the slave is the receiver.
- In a Read operation the slave is the transmitter, and the master is the receiver.

The transmitter then sends the next 8-bit byte. At the 18th Clock Pulse (and every 9th clock pulse thereafter), the transmitter releases the Data line, and the receiver acknowledges by pulling Data low. There is no limit to how many bytes may be sent after the address.

When all data is transferred, the Data line must be released by the transmitter so that the master can set the STOP condition. This is done by first pulling Data low (during clock low), then releasing Data high while clock is high. After this, the bus is free for any other device to initiate a new data transfer.

Definitions

Master – The device which initiates a data transfer (regardless of the data direction), generates the clock, and terminates the transfer.

Slave – The device addressed by the master.

Transmitter – The device which supplies data to the bus.

Receiver – The device which receives data from the bus.

Notice that the master is not necessarily the transmitter, and the slave is not necessarily the receiver.

Other

For additional information on the I²C bus specifications; modes of operation; arbitration; and synchronization, contact Philips Corporation.

9

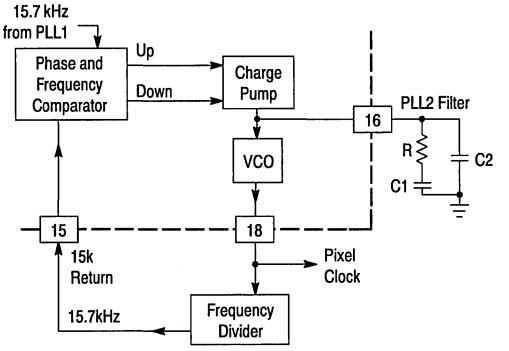
APPENDIX D

PLL Loop Theory

High Frequency Line-Locked Clock Generator

This section is not intended as a complete loop theory, its aim is merely to point out the idiosyncrasies of the loop, and provide the user with enough information for the selection of filter components. For a more in depth explanation, the references at the end of this section may be consulted.

Figure D1. PLL2 Basic Configuration



The following general remarks apply to the loop (PLL2):

- The loop frequency is ≈15.7 kHz.
- In spite of the samples nature of the loop, a continuous time approximation is possible if the loop bandwidth is sufficiently small.
- Ripple on V_C (filter pin) is a function of loop bandwidth.
- The loop is a type II, 3rd order. However, since C2 is small, the pole it creates is far removed from the low frequency dominant poles, and the loop can be analyzed as a 2nd order loop.

The following remarks apply to the Phase and Frequency Comparator:

- Phase and frequency sensitive.
- Independent of duty cycle.
- It has 3 allowed states: up, down, and off (high impedance).
- The VCO is always pulled in the right direction during acquisition.
- The Comparator's gain is higher at or near lock.

The last two remarks imply that only the higher value need be taken into account, as acquisition will be slower but always in the correct direction, whereas the higher gain will come into action as soon as the error reaches 2π.

The following values are selected and defined:
C2 = C1/10 or less, to satisfy the requirement that the effect of C2 on the low frequency response of the loop be minimal, and similar to a 2nd order loop.

ξ = 0.707 (damping factor).
ωi = 15750 x 2p = 98960 rad/sec (input frequency).
τ = RC as the loop filter
K = Ko x Ip x R/(2πN) — the loop gain
K′ = K x τ = $4\xi^2$ (the normalized loop gain)
Ko = 70 x 10^6 rad/V

Stability analysis with C2 = C1/10 and K′ = 2 (ξ = 0.707) gives a minimum value of 7.5 for the ratio ωi/K. To have some margin, a reasonable value can be 15 to 20 or higher.

Selecting ωi/K = 20 yields,
K = ωi/20 ≈ 5000.

Using the following items:
K′ = 2,
τ = 2/K = 400 µs,
K = Ko x Ip x R/(2πN)
Ip= 20 µA
N = 2000 (average value)

yields a value of 22 kΩ for R. Using a value of 400 µs for τ, C1 calculates to 18 nF, and C2 calculates to 1.8 nF.

With the above values, the loop's natural frequency (ωn), and loop bandwidth (ω3dB) can be calculated:

$\omega n = \{(Ko/N) \times Ip/(2\pi C)\}^{0.5} = 3520$ rad/sec.
fn = 3520/2π = 560 Hz.
$\omega 3dB \approx 2 \times \omega n = 1120$ Hz (valid if ξ = 0.707).

The circuit designer should be cautioned at this point that the above calculated values are not necessarily optimum for every application. Besides the fact that several assumptions were made in the discussion, the equations cannot account for items such as the PC board layout, characteristics of the external divider, and noise from various sources. The above calculated values provide for a functional circuit, which should then be tweaked to obtain minimum jitter at the pixel clock output.

When initially adjusting the filter component values, it is advisable to maintain the same general time constant (400 µs in this example), and the same x10 relationship between C1 and C2.

References:
(1) *Charge-Pump Phase-Lock-Loops* by Floyd M. Gardner, IEEE Transactions on Communications, Vol. com-28, no. 11, Nov. 1980.
(2) *Phaselock Techniques* by Floyd M. Gardner, J. Wiley & Sons, 1979.
(3) *Phase-Locked-Loops* by Roland E. Best, McGraw Hill, 1984.
(4) AN-535, *Phase-Locked-Loop Design Fundamentals*, Motorola.

GLOSSARY

Aspect Ratio – The ratio of the width of a TV screen to the height. In standard TVs, it is 4:3. In HDVT it will likely be 16:9.

Back Porch – The blanking time after the sync signal during which the color burst is inserted.

Blank, Pedestal – The signal level which is either at black, or slightly more negative than black ("blacker-than-black"), and is used to turn off the screen dot during retrace. Also referred to as the *pedestal*.

Brightness – A measure of the DC levels of the luma component. Changing brightness will change the minimum and maximum luma levels together.

Burst – The 8 to 10 cycle sine wave which is inserted in the back porch. It's frequency is the color subcarrier (3.58 MHz or 4.43 MHz), and is used as a phase reference for the color decoder.

Burst Gate – A signal identifying the time during which the burst signal occurs.

C, Chrominance – The color component of the video signal. The color is determined by the phase of the chrominance component relative to the burst signal.

Clamping – A process which establishes a fixed DC voltage level, usually during the back porch time.

Color Difference Signals – B-Y, R-Y, also designated as U and V.

Color Decoder – A circuit which separates composite video into Red, Blue, and Green, luminance, and sync signals.

Color Encoder – A circuit which combines Red, Blue, and Green, luminance, and sync signals into composite video.

Comb Filter – A multi-bandpass filter which separates the luma and chrominance components from the video signal, without sacrificing bandwidth.

Component Video, YUV – A format whereby the video information is kept as separate luma, R-Y, and B-Y signals *(YUV)*. U is the same as B-Y, and V is the same as R-Y.

Composite Sync – A sync signal which combines horizontal and vertical sync information. The waveform is made up of regularly spaced negative going pulses for the horizontal sync, and then half-line pulses and polarity reversal to indicate the vertical sync and retrace time.

Composite Video – The video signal which consists of sync, back porch, color burst, video information (luma and chroma), and front porch. This is the signal normally broadcast by TV stations.

Contrast – A measure of the difference between minimum and maximum luma amplitudes. Increasing contrast produces a "blacker" black and a "whiter" white.

dB – A power or voltage measurement unit, referred to another power or voltage. It is generally computed as:

10 x log (P1/P2) for power measurements, and
20 x log (V1/V2) for voltage measurements.

Field – One of the two or more equal parts into which a frame is divided in an interlaced system.

Frame – The information which makes up one complete picture. It consists of 525 lines in NTSC systems, and 625 lines in PAL systems. An interlaced system is typically composed of two fields.

Front Porch – The blanking time immediately before the sync signal.

Horizontal Sync – The negative going sync pulses at the beginning of each line. The pulses indicate to the circuit to begin sweeping the dot across the screen.

Hue – A measure of the correctness of the colors on a screen.

Interlaced System – A method of generating a picture on the screen whereby the even number lines are processed, and then the odd number lines are processed, thereby completing a full picture.

IRE – Abbreviation for *International Radio Engineers*, it is the amplitude unit used to define video levels. In standard NTSC signals, blank-to-white is 100 IRE units, and blank-to-sync tip is 40 IRE units. In a 1.0 Vp-p signal, one IRE unit is 7.14 mV.

Luma, Y – The brightness component of the video signal. Usually abbreviated "Y", it defines the shade of gray in a black-and-white TV set. In color systems, it is composed of 0.30 red, 0.59 green and 0.11 blue.

NTSC – *National Television System Committee*. This committee set the color encoding standards and format for television broadcast in the United States.

PAL – *Phase Alternating Line*. A color encoding system in which the burst is alternated 90° each line to help compensate for color errors which may occur during transmission. This system is popular mainly in Europe.

Pixel – The smallest picture element, or dot, on a screen. It is determined by the design of the CRT, as well as the system bandwidth.

R-Y, B-Y – Referred to as *color difference signals*. These are two of the three signals of component video. When combined with Y, the full color and luminance information is available.

Retrace – The rapid movement of the blanked dot from the screen's right edge to the left edge so it can start scanning a new line. It is also the rapid movement from the lower right corner to the upper left corner during vertical blanking.

RGB – The three main colors *(red, blue, green)* used in the acquiring, and subsequent display of a video signal.

S-VHS – A format whereby the video information is kept as separate luma and chroma signals (Y and C).

Sandcastle – A signal which indicates the horizontal blanking time. It encompasses the front porch, sync, and back porch. Two amplitudes distinguish the front porch + sync time from the back porch.

Saturation – A measure of the intensity of the color on a screen. Also related to its purity.

Sync Separator – A circuit which will detect, and output, the sync signal from a composite video waveform.

Vertical Sync – The synchronizing signal which indicates to the circuitry to drive the dot to the upper left corner of the screen, thereby starting a new field. This signal is derived from the composite sync.

MC44144

SUBCARRIER REFERENCE

SILICON MONOLITHIC INTEGRATED CIRCUIT

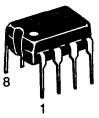
Advance Information

Subcarrier Reference

The MC44144 is a gated phase-locked-loop intended for, but not restricted to, video applications. The integrated circuit contains a gated phase detector, voltage controlled crystal oscillator, divide-by-4 circuitry, and a video clamp. This device provides a 4X reference frequency output, and a 1X reference frequency output.

The MC44144 is manufactured using Motorola's high density, bipolar MOSAIC™ process.

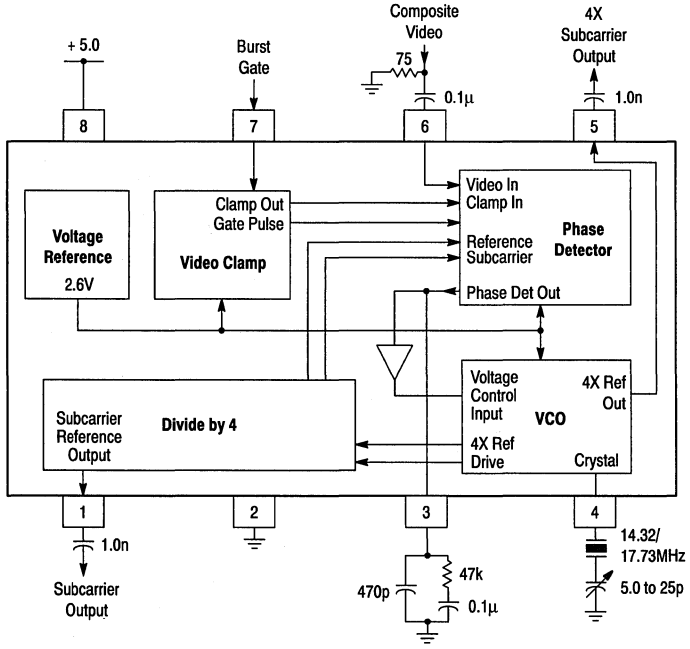
- 8-Pin DIP or Surface Mount Package
- Gated-Phase Detector
- Single Pin Voltage Controlled Crystal Oscillator
- 1X and 4X Subcarrier Output
- Operates Off of a Standard 5.0 V Supply



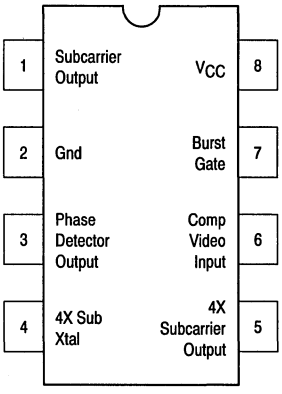
P SUFFIX
PLASTIC PACKAGE
CASE 626

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO-8)

Simplified Block Diagram



PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Temperature Range	Package
MC44144D	0° to +70°C	SO-8
MC44144P		Plastic

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	6.0	Vdc
Operating Ambient Temperature	T_A	0° to +70	°C
Storage Temperature Range	T_{stg}	– 65 to +150	°C
Operating Junction Temperature	T_J	+150	°C

RECOMMENDED OPERATING CONDITIONS

Characteristics	Pin	Symbol	Min	Typ	Max	Unit
Supply Voltage	8	V_{CC}	4.5	5.0	5.5	Vdc
Composite Video Input (Note 1) Burst Amplitude to Acquire Lock	6	—	50	300	1000	mVp-p

NOTE: 1. Total peak-to-peak voltage of video should not exceed ground or V_{CC}.

ELECTRICAL CHARACTERISTICS ($0 < T_A < 70°C$, $V_{CC} = 5.0$ Vdc)

Characteristics	Pin	Min	Typ	Max	Unit
Operating Current	8	4.0	8.0	10	mA
Burst Gate: Threshold (No Hysteresis)	7				
On/Off		—	2.2	—	Vdc
Input Current: (V_{in} = 5.0 V)		0.1	2.0	5.0	µA
(V_{in} = 0 V)		0.01	—	0.01	
4X Subcarrier	5				
Output Voltage: (14.41 MHz)		400	610	650	mVp-p
(17.73 MHz)		500	450	800	
Output Impedance: (14.3 MHz and 17.73 MHz)		—	25	—	Ω
Subcarrier Output	1				
Output Voltage: (3.58 MHz and 4.43 MHz)		200	300	350	mVp-p
Output Impedance: (3.58 MHz and 4.43 MHz)		—	200	—	Ω
Subcarrier Phase Angle (Note 2)		+ 75	– 70	– 45	Deg
Phase-Locked-Loop Pull-In Range NTSC		400	—	250	Hz
PAL		400	—	400	
Phase-Locked-Loop Hold-In Range NTSC		400	—	300	
PAL		400	—	400	

NOTE: 2. Referenced to composite video input color burst.

Figure 1. Typical VCXO Gain

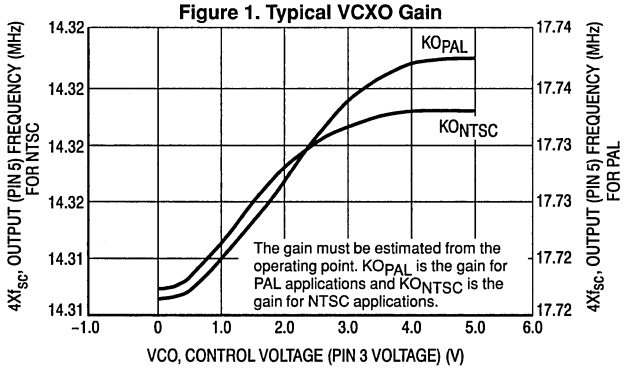
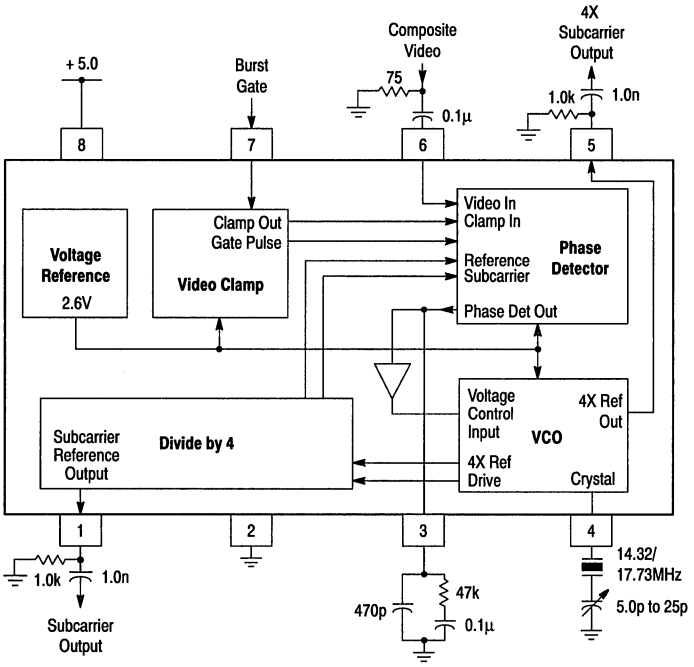


Table 1. Crystal Specifications

Frequency	14.31818 MHz (NTSC) 17.734475 MHz (PAL)
Mode	Fundamental
Frequency Tolerance @ 25°C df/dfo 0° – 70°C	40 ppm
Load Capacitance	20 pF
ESR	50 Ω
C1 (Internal Series Capacitance)	15 fF(mpF)

9

Figure 2. Test Schematic



FUNCTIONAL DESCRIPTION

The MC44144 is designed to implement the color sync function in a video system. When provided NTSC/PAL composite video or composite chroma and burst gate inputs, the IC will phase-lock a Voltage Controlled Crystal Oscillator (VCXO) to the color burst. Both 4X and 1X subcarrier frequency outputs are provided by the IC. The VCXO operates off of a 4X subcarrier crystal and is typically ± 350 Hz of pull-in.

In addition to providing the gate pulse for the MC44144 phase detector, the Burst Gate input also initiates a clamp pulse that sets up the level of the composite video at the input to the Phase Detector. The start and duration of the Gate Pulse should be timed so that the pulse envelopes the color burst of the video signal, but not so wide as to gate sync or video into the Phase Detector.

The Phase Detector is enabled when the voltage at the Burst Gate input (Pin 7) is above the nominal 2.2 V threshold. While this makes possible the ability to lock to a color burst, it does not exclude the possibility of lock to a constant reference. If a constant source is to be the reference, the Phase Detector can be permanently enabled by holding the voltage on the Phase Detector input pin higher than the threshold voltage.

The phase detector gain must be specified in two ways, for a constant reference and for a burst-locked application. The gain in a constant reference application is specified by the maximum current output with the maximum phase error. For a maximum phase error of $\pi/2$ radians the maximum current available is approximately 200 µA. So the phase detector gain is defined as,

$$KPD = 200/(\pi/2)(\mu A/rad/sec)$$

For a burst-locked application, the Phase Detector is active for only the duration of the color burst. Therefore the phase detector gain must be specified as an average gain over a line period. In this case the phase detector gain for NTSC and for PAL applications is,

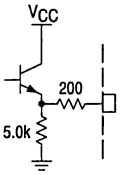
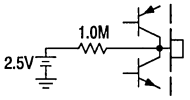
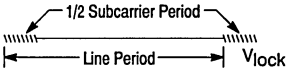
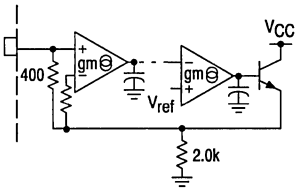
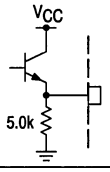
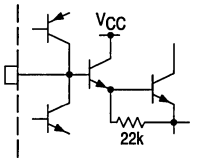
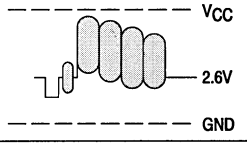
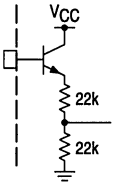
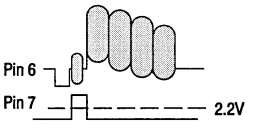
$$KPD_{NTSC} = (8/(\pi/2))(\mu A/rad/sec) \text{ and,}$$

$$KPD_{PAL} = (7/(\pi/2))(\mu A/rad/sec)$$

A suitable filter for both types of applications is shown in the test schematic Figure 2. This same filter also works for both NTSC and PAL applications.

The 4X subcarrier Voltage Controlled Crystal Oscillator (VCXO) was designed to work with a parallel resonant crystal. A suitable crystal would meet the specifications found in Table 1.

PIN FUNCTION DESCRIPTION

Name	Pin	Representative Circuitry	Description	Expected Waveforms
Subcarrier Output	1		Subcarrier Output. A phase-locked reference of the PAL or NTSC color burst is output at this pin.	A 300 mVp-p square wave is output. Some high frequency content is present.
Ground	2		Circuit Ground	
Phase Detector Output	3		The error current from the phase detector is output at this pin. A filter circuit should be connected at this pin.	A beat waveform, showing both horizontal period and half the subcarrier period, is present. 
4X Sub Xtal	4		Crystal Oscillator Pin. A 4X subcarrier parallel resonant crystal, in series with a 5.0 pF to 25 pF trimmer capacitor provides the resonant element for the Voltage Controlled Crystal Oscillator (VCXO).	Approximately 40 mVp-p. A scope probe will disturb the frequency of oscillation.
4X Subcarrier Output (or Black Burst)	5		Buffered output from the 4X voltage controlled oscillator.	The sinusoidal 4Xf_{SC} oscillator output is available at this pin. The output is nominally: 610 mVp-p for NTSC, 450 mVp-p for PAL.
Composite Video Input (Black Burst, Continuous Wave, or Composite Chroma can also be applied)	6		Composite Video Input. Color burst from the video present at this pin is used as a reference to phase lock the VCXO. Positive or negative video may be used.	Composite video should be applied at this pin. The color burst amplitude of the input video should be at least 50 mV, but no more than 1000 mV. The waveform at this pin should not exceed ground or VCC. 
Burst Gate Input	7		Input for the phase detector gate pulse. TTL compatible. The threshold is nominally 2.2 V.	A positive going gate pulse should be applied at this pin. The Burst Gate input should envelope the color burst. 
VCC	8		Power Supply Pin. 5.0 Vdc should be applied at this pin.	

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC44145

SYNC SEPARATOR/ PIXEL CLOCK GENERATOR

SILICON MONOLITHIC INTEGRATED CIRCUIT

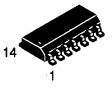
Product Preview

Sync Separator/ Pixel Clock Generator

The MC44145 Pixel Clock Generator is a component of the MC44000 family, and a spin-off of the PLL2 function of the MC44011, Digital Multistandard Video Processor.

The MC44145 contains a sync separator with horizontal and vertical outputs, and clock generation circuitry for the digitalization of any video signal along with the necessary circuitry for clock generation, such as a phase comparator and a divide-by-2 to provide a 50% duty cycle.

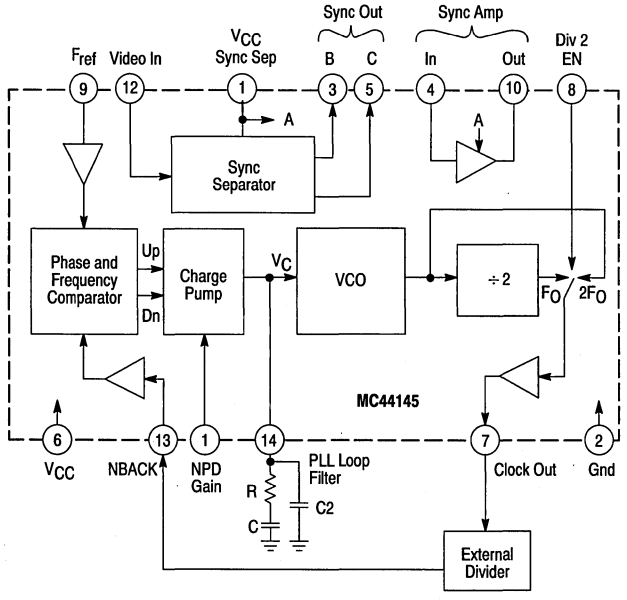
The MC44145 is available in a 14 pin package and is fabricated using Motorola's high density, low voltage, bipolar MOSAIC 1.5® process.



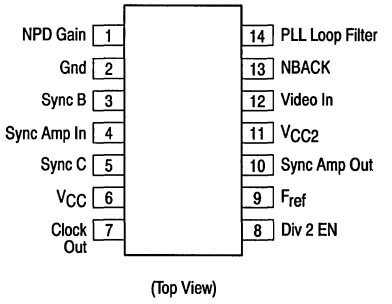
D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO-14)

9

Simplified Block Diagram



PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Temperature Range	Package
MC44145D	0° to +70°C	SO-14

CIRCUIT DESCRIPTION

Composite Sync Separator

The composite sync separation section comprises two blocks, a sync slicer and a sync amplifier, that can be used to extract the vertical sync information from a video signal.

The sync separator is an adaptive slicer in which the video signal is slightly integrated and then sliced at a ratio of 4.7 to 64 which corresponds to the sync to horizontal ratio. Two outputs are given, one of high impedance and the other low impedance.

A slicing sync inverting amplifier is also on-chip, allowing one output to be used for composite sync and the other output to be integrated and then sliced using the slicing amplifier to extract the vertical sync information.

Clock Generation

The clock generation is made up of a wide ranging emitter-coupled VCO followed by a switchable ÷ 2 to provide a 50% duty cycle wherever required, or twice the set frequency if an external divider is used. The clock generation is a PLL subsection. Its function is the generation of a high frequency, line-locked clock that is used for video sampling and digitizing.

The clock is output by a LSTTL-like buffer which has a limited drive capability of two LSTTL loads.

The VCO is driven from a charge pump circuit, with selectable current. The charge pump is driven from the phase comparator. The phase comparator is a type IV "phase and frequency comparator" sequential circuit.

The clock generator, the heart of a PLL, is to be closed by means of an external divider, thus setting the synthesized frequency. This divider could be implemented in discrete logic or be a part of an ASIC subsystem.

Phase and Frequency Comparator

The phase comparator is fed from two input buffers (F_{ref}) which expects a reference frequency at line rate and that is rising-edge sensitive, and NBACK which comes from the external divider and is falling-edge sensitive.

Charge pump current and output divider action are controlled by applying suitable voltage on the appropriate pins, respectively, NPD Gain and Div 2 EN.

PIN FUNCTION DESCRIPTION

Pin	Function	Description
1	NPD Gain	This pin sets the gain of the phase frequency detector by changing the current of the charge pump output (40 μA or 80 μA). Low current with this pin > 2.0 V, high current for < 0.5 V.
2	Ground	Ground connection common to the PLL and sync separator sections.
3	Sync B	High impedance sync output.
4	Sync Amp In	Sync amplifier input.
5	Sync C	Low impedance sync output.
6	V_{CC}	Power connection to the PLL section.
7	Clock Out	VCO clock output. Capable of limited LSTTL drive. It should not be used to drive high capacitive loads, such as long PCB traces or coaxial lines.
8	Div 2 EN	The divider is switched-in with this pin > 2.0 V; switched-out for < 0.5 V.
9	F_{ref}	Reference frequency input to the phase and frequency comparator. Typically, this will be a 15625 (15475) Hz signal. It is rising-edge sensitive. Due to the nature of the phase and frequency comparator, no missing pulse is tolerable on this input. In a typical setup, this signal can be provided by the MC44011.
10	Sync Amp Out	Sync amplifier output.
11	V_{CC2}	Power connection to the sync separator and amplifier.
12	Video In	Video signal input to the sync separator.
13	NBACK	Fed by the external clock divider. Sets the multiplication ratio of the loop in multiples of the F_{ref} frequency. Negative-edge sensitive.
14	PLL Loop Filter	Values for the loop filter components should be the same as for the MC44011.

NOTE: The two V_{CC} pins are not independent, as they are internally in relationship by means of the input protection diodes. They must always be connected to a suitable V_{CC} line.

CIRCUIT OPERATION

Composite Sync Separator

The sync separator is an adaptive slicer. It will output "raw" sync data. Two outputs are given, thus allowing one output to be used for composite sync and the other output to be integrated and then sliced using the inverting slicing amplifier provided. As the input of the slicing amplifier is external, the amplifier may be driven from either sync output, although normally the high output impedance (Sync B) would be recommended.

The positive video input signal required is nominally 1.0 V sync-to-white, but the circuit supports signals above and below this level and also is resistant to a degree of reflections on the signal. Coupling to the sync separator may be achieved by a simple capacitor of 100 nF, but better results may be obtained with a higher value in series with a resistance of 1.0 kΩ.

Clock Generator

The system is best put to use in a dual loop configuration. The first loop locks to line frequency by means of a type I phase detector (multiplier type) which is insensitive to missing pulses. This PLL is then followed by a second loop using the MC44145, performing frequency multiplication. The phase comparator of the MC44145 is frequency and phase sensitive. It is a type IV (sequential type) phase detector, which does not tolerate missing pulses. The dual loop structure makes up a noise insensitive frequency (and phase) locked loop.

The phase and frequency comparator provides two logical outputs, mutually exclusive – up or down – that are used to source or sink current to and from the loop filter. This current can be user-selected to be 40 μA or 80 μA (typical), thus providing some degree of loop gain control.

The VCO is an emitter-coupled multivibrator type, with an on-chip timing capacitor, and has been designed for low phase noise.

The divide-by-2 is included at the output of the VCO, thus allowing for a precise 50% duty cycle, hence the VCO is operating at twice the required frequency. The divider can be bypassed, bringing the VCO output directly to the output buffer.

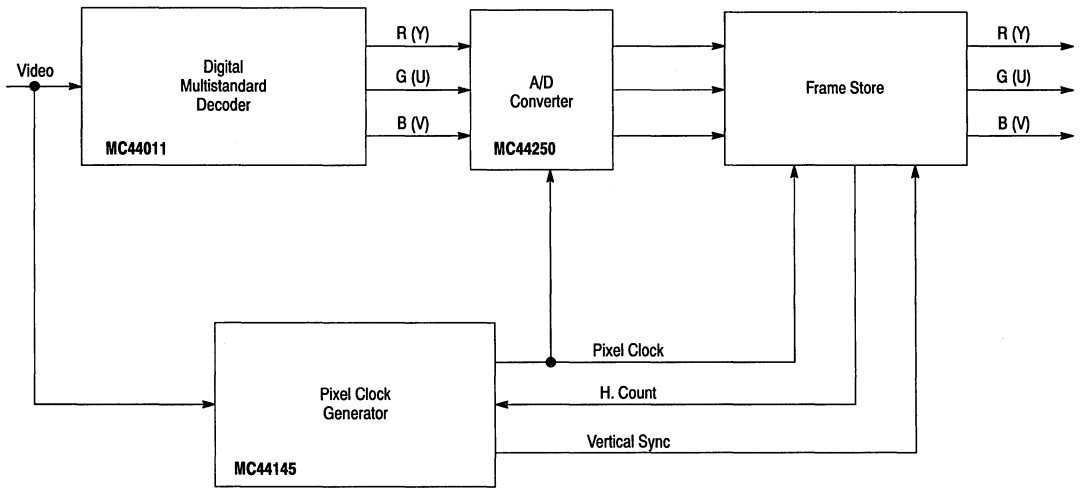
The external divider must provide a feedback pulse to close the loop. The falling edge of this pulse will be aligned (when the loop is in lock) with the rising edge of the pulse applied to the F_{ref} input. Operation of the phase comparator is insensitive to the duty cycle of both its inputs. The feedback pulse should have a minimum width of 500 ns. This can be guaranteed if it has a length of at least 16 output clock cycles (highest output frequency with the divider disabled).

APPLICATION INFORMATION

Analog video signals out of the MC44011 are sampled and converted to 8-bit digital in the A/D converter (MC44250) by means of the pixel clock generator, provided by the MC44145 (see Figure 1).

The frame store contains the memory, the necessary logic for the memory addressing, as well as the counter to set the frequency multiplication ratio of the line-locked clock generator (H. Count).

Figure 1.



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

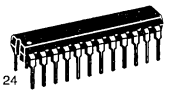
MC44301

Advance Information

High Performance Color TV IF

The MC44301 is a single channel TV IF and PLL detector system for all standard transmission systems. This device enables the designer to produce a high quality IF system with white spot inversion, AFT and AGC. The MC44301 was designed with an emphasis on linearity to minimize sound/picture intermodulation.

- Single Coil Adjustment for AFT and PLL
- VCO at 1/2 IF for Minimum Beats
- Simple Circuitry for Low System Cost
- White Spot Inversion
- Symmetrical ± 2.0 MHz Pull-in
- User Selectable Positive or Negative Modulation
- Auxiliary AM Detector for AM Sound
- Simple Alignment Procedure



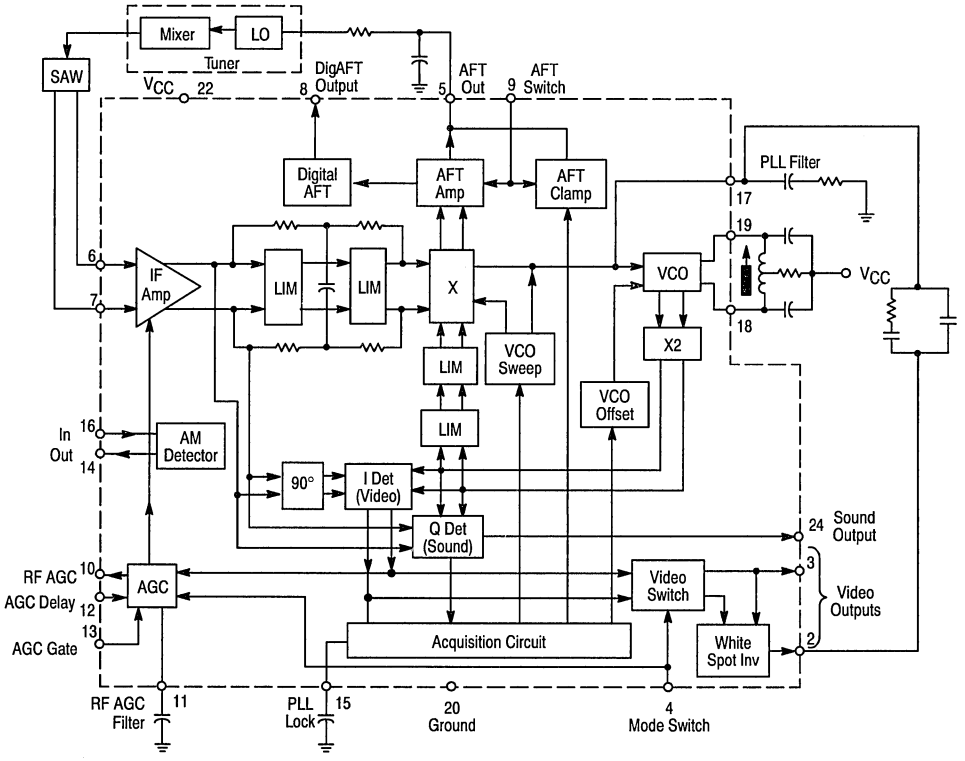
P SUFFIX
PLASTIC PACKAGE
CASE 724

DW SUFFIX
PLASTIC PACKAGE
CASE 751F
(SO-28L)

ORDERING INFORMATION

Device	Temperature Range	Package
MC44301P	0° to 70°C	Plastic DIP
MC44301DW		SO-28L

Figure 1. Block Diagram



Note: Pin numbers shown are for DIP package only. Refer to Table 1 for pin assignments.

MAXIMUM OPERATING CONDITIONS

Characteristics	Symbol	Rating	Unit
Power Supply Voltage — Pin 22	V_{CC}	7.0	V
Gating Pulse Amplitude	—	±500	μA pk
Ambient Operating Temperature (Note 1)	T_A	0 to +70	°C
Storage Temperature	T_{stg}	–65 to +150	°C
Junction Temperature	T_{Jmax}	150	°C
Power Dissipation Derate above 25°C	P_D	1.25 10	W mW/°C

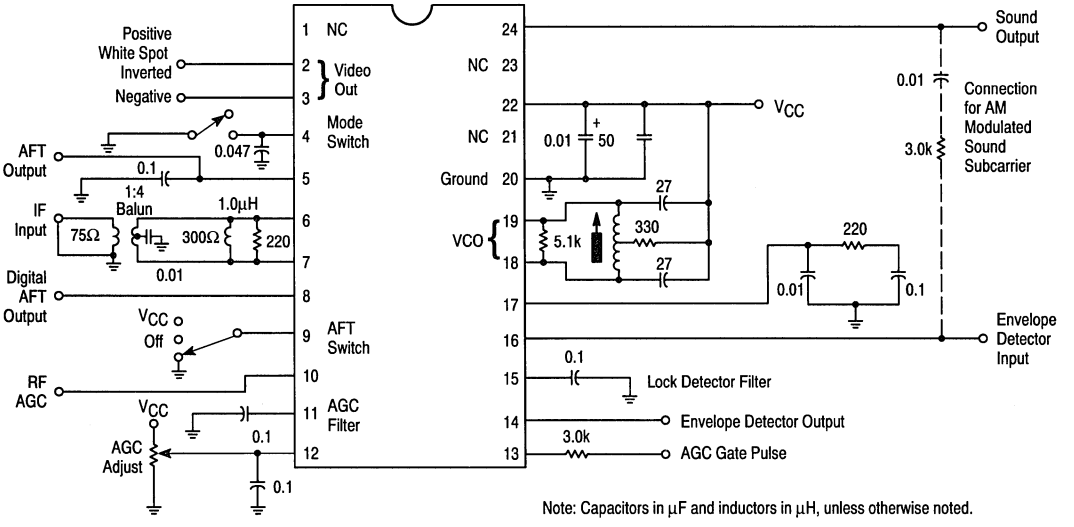
ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc, T_A = 25°C, unless noted.)

Characteristics	Pin (DIP)	Pin (SOIC)	Min	Typ	Max	Unit
Operating Supply Voltage Range Supply Current	22	27	4.5 —	— 70	5.5 —	Vdc mAdc
Differential Input Sensitivity for Full Output	6,7	7,8	—	30	—	μV_{rms}
Bandwidth Video Bandwidth	2,3	2,3	— —	120 8.0	— —	MHz
AGC Range Noise Figure (R_S = 300 Ω)			— —	80 7.0	— —	dB
Lock-up Time			—	5.0	—	ms
Video Amplitude (100% mod depth)	2,3	2,3	—	2.2	—	Vp-p
Tuner AGC Current (10 Vdc; R_{pullup} = 10 k)	10	12	0.6	0.95	—	mAdc
Differential Gain Distortion Differential Phase Distortion (Uncorrected — refer to text description)	2	2	— —	2.0 1.0	5.0 5.0	% Degrees
Sound Subcarrier Output	24	28	—	0.1	—	V_{rms}
AGC Gate Pulse (R_{pin} ≈ 5.0 k)	13	15	—	±0.3	—	mA pk
Differential Input Impedance R_{in} C_{in}	6,7	7,8	— —	3.4 3.0	— —	kΩ pF

NOTE: 1. At 0°C the device only tolerates a 5% change in minimum supply voltage (i.e. 4.75 Vdc is the minimum supply voltage at which the device will function).

9

Figure 2. Test Circuit



Note: Capacitors in μF and inductors in μH, unless otherwise noted.

TYPICAL CURVES

Figure 3. AFT Open-Loop Error versus Closed-Loop Error

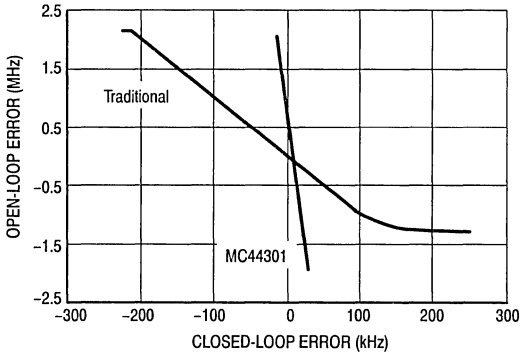


Figure 4. AGC Voltage versus Antenna Input Signal

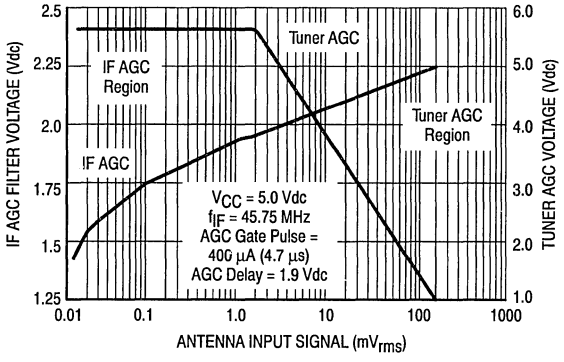


Figure 5. IF Noise Figure versus IF Input

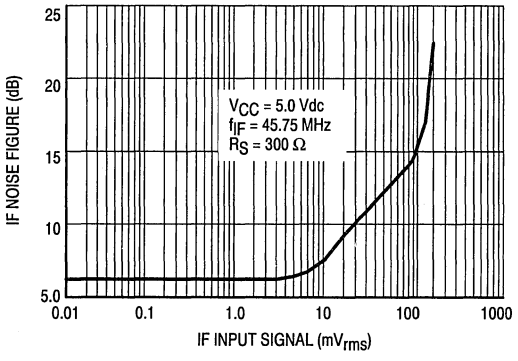
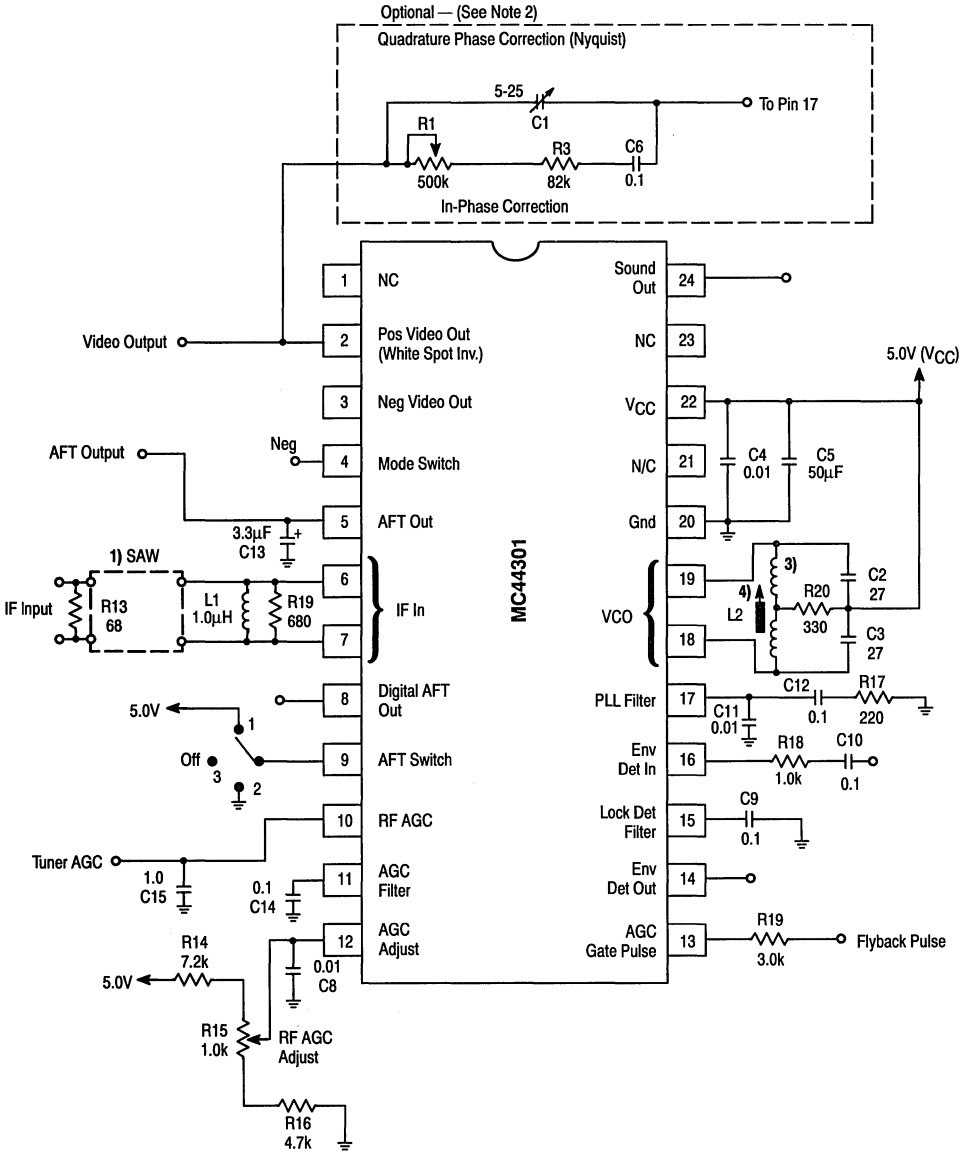


Table 1. Package/Pin Assignments

Description	24 Pin (DIP)	28 Pin (SOIC)
No Connection	1	1
Positive Video Output	2	2
Negative Video Output	3	3
No Connection		4
Mode Switch	4	5
AFT Output	5	6
IF Input (Pos)	6	7
IF Input (Neg)	7	8
Digital AFT Output	8	9
AFT Switch	9	10
No Connection		11
RF AGC	10	12
AGC Filter	11	13
AGC Adjust or Delay	12	14
AGC Gate Pulse	13	15
Envelope Detector Out	14	16
Lock Detector Filter	15	17
No Connection		18
Envelope Detector In	16	19
PLL Filter	17	20
VCO	18	21
VCO	19	22
Ground	20	23
No Connection	21	24
No Connection		25,26
V_{CC}	22	27
No Connection	23	
Sound Output	24	28

9

Figure 6. Typical 5.0 V Color TV Application



NOTES:

1) IF input assumes 75 Ω output from tuner. The SAW filter should be low loss (<20 dB) with good triple transit response. The Murata 80Z series resin mold SIP type filter has low loss and good TT response. The PCB enclosed in the evaluation kit accommodates these filters and SAF45MA80Z and Siemens M1963. The Zenith SAW filter is packaged in a metal can filter.
2) Optional circuitry to improve sound performance by providing additional quadrature and in-phase corrections.
3) The VCO coil is a shielded 10 mm center-tapped inductor, bifiliar wound. See detials in Figure 17.
4) See Figure 17 for coil details.

CIRCUIT DESCRIPTION

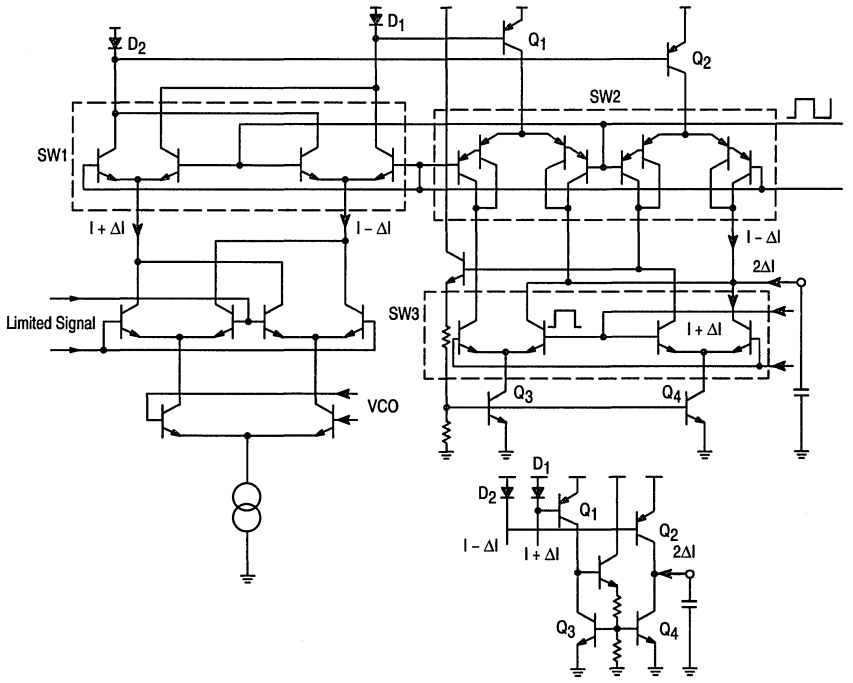
IF Amplifier and AGC

The IF amplifier is a four stage AC coupled amplifier having a sensitivity of 30 μV, thus removing the need for a SAW preamplifier when used with a suitable SAW filter and tuner. The first three stages are gain controlled, giving an extended AGC range of 80 dB with improved signal handling. The AGC to the first stage is delayed as normal so as to preserve the amplifier's noise figure. Reverse AGC is supplied to the tuner and provision is made for the usual tuner RF delay adjustment. The AGC system is gated with a positive or negative pulse. Flyback gating is used for negative modulation and the video is maintained constant by the sync tip being kept equal to an internal voltage reference. When positive modulation is selected, via the mode switch, back porch sampling pulse is used and the internal reference is altered such that the video amplitude remains unchanged. Both polarities of video are provided, and the same sense is kept at the video outputs by means of the video switches.

PLL and Demodulation

Following the IF amplifier and preceding the PLL phase detector is a two stage limiter with a gain of 100 and overall DC feedback. This contrasts with the usual single stage of limiting with no DC feedback and diodes with possibly a tuned circuit at its output. With two stages of limiting, the minimum gain required to remove amplitude modulation can be designed-in without the large voltage swings of a single stage with the same gain. Large voltage swings lead to poor differential phase performance, hence the need for diodes and a tuned circuit as used in previous designs. The DC feedback removes the effects of input offsets which are another source of differential phase. The combination of low swing per stage and DC feedback removes the need for having a tuned circuit at the limiter output and reduces the danger of IF instability and radiation. The only problem in using this technique is the potential for extra static phase shift with resultant errors in the demodulating angles at the video and sound demodulators. However, by putting a similar two stage limiter, with a matching phase shift on the oscillator side of the phase detector, the demodulating angles can be restored to the correct phases (0°, 90°). Phase errors and hence quadrature video distortion can also be caused by DC errors in the phase detector and AFT amplifier (Figure 1). Most of the DC offsets are caused by mismatches in the current mirrors of the push-pull output stage (see simplified stage Figure 7). Switches S_1, S_2 and S_3 are driven by an accurate 1:1 mark/space ratio 1.0 MHz square wave. Switches S_1 and S_2 maintain the same sense of error signal, while S_2 ensures errors due to the top PNP current mirrors average to zero on the external loop filter capacitor. In a similar way, S_3 by interchanging Q_3 and Q_4 cancels errors due to the bottom NPN mirror. With phase errors reduced to a minimum, there is no need for external phase adjustments. The output of the phase detector is filtered and controls the VCO to lock at 90°C phase to the incoming IF signal. The VCO,

Figure 7. Phase Detector

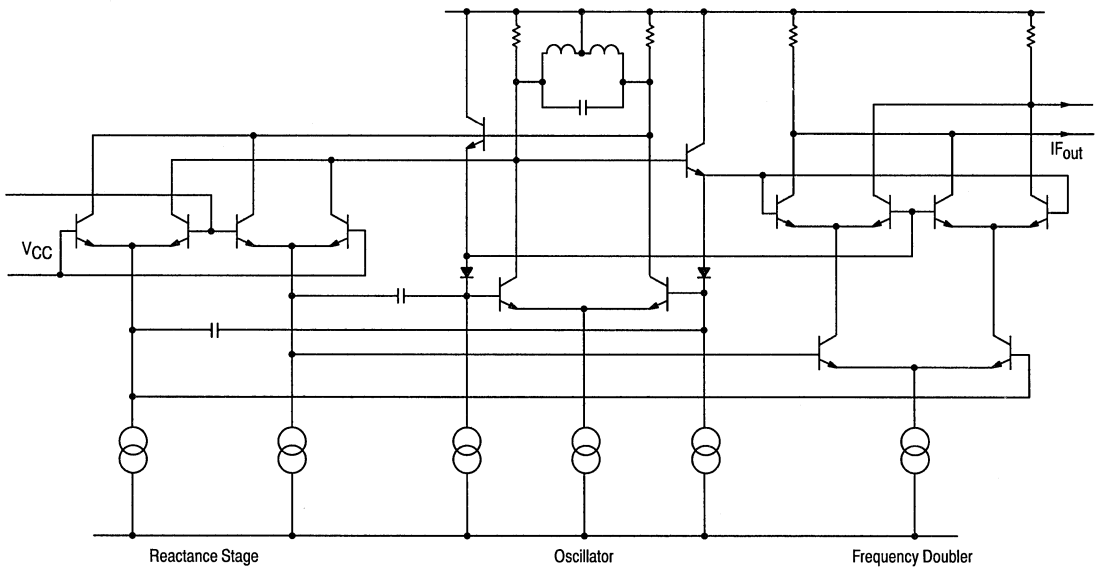


as shown in Figure 8, is a reactance tuned oscillator at "half IF". The frequency is doubled by a balanced multiplier, and signals to the multiplier's input ports are at 90° to each other. Reactance tuning enables a higher Q to be used in the oscillator tank circuit as opposed to a phase shift type of oscillator with the same tuning range. The oscillator being at "half IF" means that radiation from the external frequency-determining components will be at half frequency and so will not desensitize the system even if picked up by the amplifier input leads (PLL push-off). Running the oscillator at twice IF and dividing down, which is another way of solving this problem, has several disadvantages. First and foremost, radiation into the antenna at twice IF produces channel 6 problems in the U.S.A. and possibly channel 8 due to harmonics. It is also much more difficult to produce a stable oscillator at twice the IF frequency than at one-half IF frequency. After attaining phase lock, demodulation of the video is achieved by multiplying the 90° phase shifted signal (nonlimited) with the regenerated vision carrier (VCO) in a double balanced multiplier. The sound FM intercarrier signal is recovered in a similar way by multiplication, but in this case, the phase relationship of signal and VCO is 90° and not 0° as for the video.

Differential Phase Suppression

Even with all the care taken in this design, some residual differential phase still remains. Although low, it would degrade stereo sound performance. In addition, there is the quadrature differential phase produced by the IF filter to be considered. Both produce currents in the output of the phase detector which in turn phase modulates the VCO. This phase modulation is transferred to the sound intercarrier and hence produces video related sound interference. With the correct phase of demodulated video, these currents can be eliminated at the output of the phase detector, as shown in Figure 6, by the network connected to the PLL filter. The phase detector current, due to the in-phase differential gain, is cancelled by the resistor current, while the capacitive current cancels the quadrature component induced by the IF filter. This technique enables the level of performance to be taken to the point where the use of the parallel sound IF is now unnecessary. Here it should be pointed out that in many cases the *improved sound quality* of a parallel sound system has proved to be illusive. The gain in quality accrued by removing IF filter phase modulation is often more than offset by imperfections in the regeneration of the vision carrier (VCO).

Figure 8. VCO and Frequency Doubler



Video Demodulator and Amplifier

The video demodulator and amplifier are shown in simplified form in Figure 9. The 90° phase shift of the signal is obtained by replacing the usual emitter resistors in the differential amplifier feeding the demodulator by capacitors. The output currents are 90° with respect to the input voltage over a wide range of frequencies and small phase errors, caused by transistor small signal emitter resistances, are corrected by the cross coupled resistors. This arrangement leads to a simpler design, the ability to adjust the demodulation angle, and lower distortion than is normal at the IF amplifier/demodulator interface. The dynamic emitter resistances are now in quadrature with the capacitive reactance and therefore contribute very little to the resultant output. Although the current outputs of the demodulator are in antiphase, the voltages at A and B are forced by the feedback loop to be in phase. Level shifting from the top supply to the bottom rail is within the feedback loop, and RF components are filtered internally. The advantages of this configuration are improved linearity with lower sound/chroma beat products; differential to single-ended conversion of the demodulator output; accurate control of the peak white video level, and low levels of high frequencies at the video outputs. The positive video output is intended to be used as the actual video and is acted upon by a white spot noise inverter. This effectively removes the "whiter than white" noise produced by a true synchronous demodulator and prevents the CRT from being overdriven and defocused. The negative video output is not acted upon by a white spot noise inverter and, of course, the noise output from a synchronous detector does not contain a DC component. Hence, this drive should be used as the sync separator drive because a simple preseparator low pass noise filter will give optimum sync performance.

Sound Output

A separate quadrature demodulator is used to recover the intercarrier sound signal. The IF signal and VCO have a 90° phase relationship at the detector's input ports instead of the 0° required at the video demodulator. This ensures that the only video components appearing at the output will be high frequency components. A consequence of the quadrature relationship of the demodulator signals is that the low distortion capacitive input stage used in the video demodulator cannot be used. Instead, a new linear wideband differential stage has been designed where the distortion in the output currents, caused by emitter/base diode nonlinearities, is cancelled by the current through the R_2 resistor. A reduction in THD of 20 dB is obtained, compared to a simple differential amplifier even at 120 MHz. The combination of a linear input stage and a post demodulation feedback amplifier results in quadrature intercarrier sound demodulation having lower video interference than sound recovered in the normal way from the video channel.

Figure 9. Video Demodulator and Amplifier

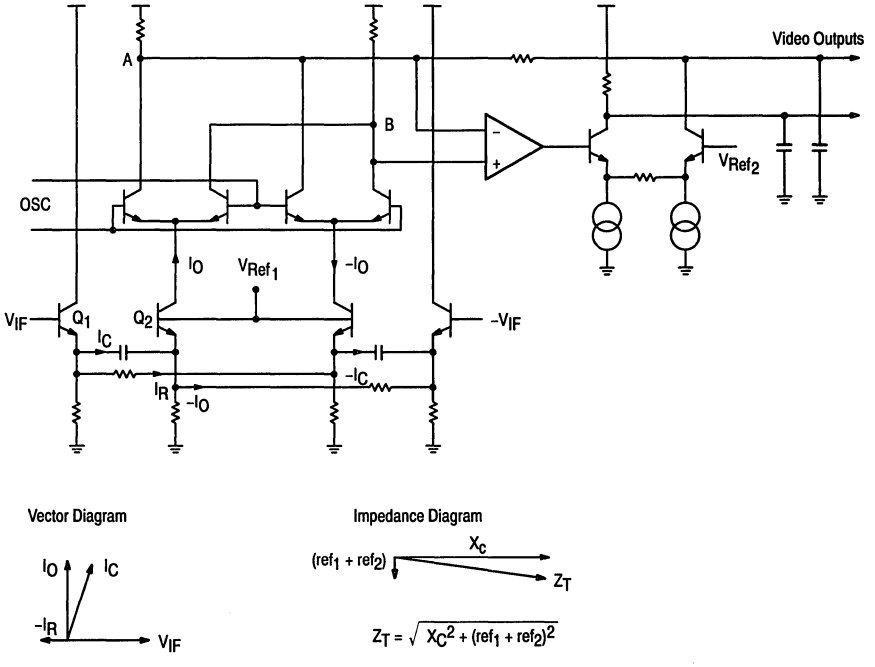
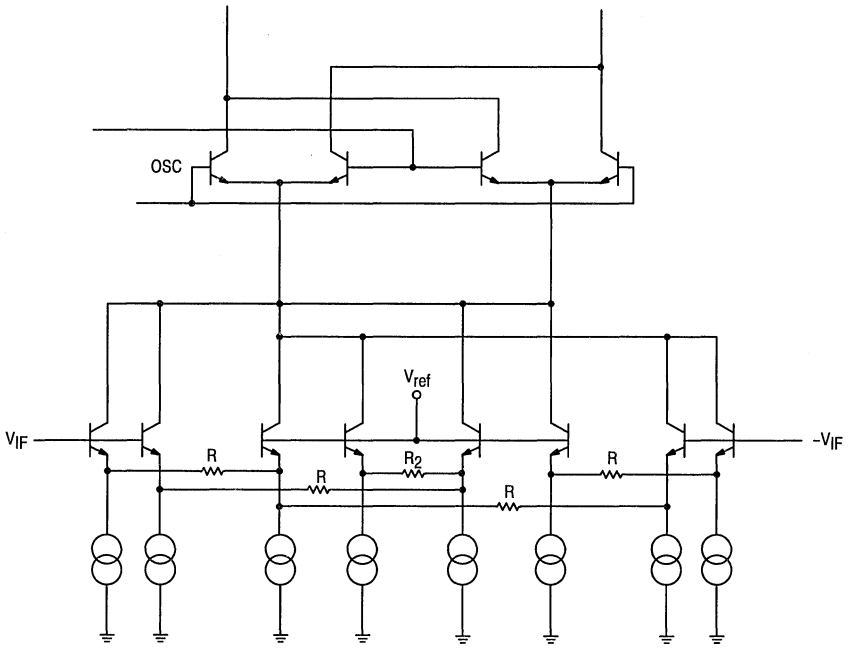


Figure 10. Sound Demodulator



AFT

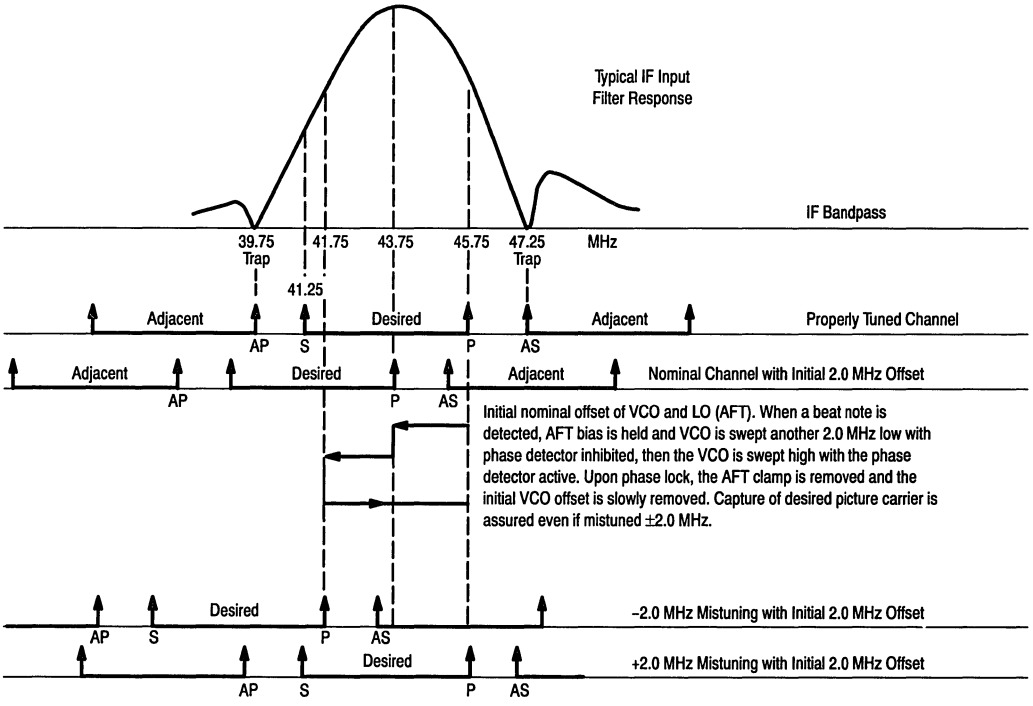
The AFT portion of the circuit is the most unconventional in form. Essentially, AFT is derived by amplifying the error signal and applying this to the local oscillator in the tuner, thus eliminating a coil and a potential IF instability problem. After acquisition (phase lock) when the circuit has reached its steady state condition, due to the much higher gain in the LO loop, the VCO will have moved a small amount (Δfv) from its nominal frequency, and almost all the original IF error (Δfe) will have been corrected by a change in the LO frequency (Δfl). In this way, provided the local VCO loop can initially be phase locked to the incoming IF signal, the VCO can be used as the frequency reference for the AFT system. It follows from the above, therefore, because the system is phase locked, that Δfe = (Δfl +Δfv). The combination of local VCO loop and the loop produced by feedback to the local oscillator forms a double-loop PLL. Analysis shows that overall system stability can be assured by treating the VCO as a stand alone PLL, provided the bandwidth is much wider than the LO loop. The VCO loop therefore is a low gain wideband loop which guarantees initial capture, while the LO loop is basically a high gain DC loop used to keep frequency and phase offsets to a minimum.

The AFT system is designed to acquire the vision carrier, without false locking to the sound or adjacent sound carriers, with an initial error of ±2.0 MHz being reduced to 10 kHz to 20 kHz when locked (U.S.A.). This contrasts with the discriminator type of AFT which has highly asymmetric lock characteristics (–2.0 MHz + 1.0 MHz), because of the effects of the IF filter, and large closed-loop errors caused by limited loop gain (see Figure 3). To achieve this level of performance without encountering the normal AFT problems associated with high loop gain (large DC offsets, etc.), a novel approach has been taken to locking up the PLL. In the absence of an IF signal, the acquisition circuitry examines the state of the video (I) and sound (Q) demodulators and detects the lack of a signal. The filtered output of the lock detector then sits at approximately 2.7 V. Under these circumstances the LO drive is clamped to a reference voltage and an offset applied to the VCO. This is done in such a way that the IF signal (should a signal appear) and the VCO are sitting in the center of the IF filter passband. Therefore, even if the LO drifts high by as much as 2.0 MHz, the signal will not be significantly attenuated by the filter. On the arrival of a signal, beat notes appear at the outputs of the demodulators, the output of the lock detector goes low and a sweep generator is switched on. The generator immediately sweeps the VCO an additional –2.0 MHz from its out of lock mid-band nominal frequency. During this negative sweep, the PLL phase detector is switched off so phase lock cannot be obtained. The VCO is then swept positive from –2.0 MHz to +2.0 MHz of the nominal out of lock frequency with the phase detector switched on. The PLL will therefore lock to the first carrier it encounters. This in fact must be the vision carrier because the sound carrier is more than 2.0 MHz below the nominal frequency and the adjacent sound carrier is higher than the vision carrier. On achieving lock, the lock detector output goes high. When this happens, the AFT

clamp is released, the VCO offset is slowly removed, the sweep generator is inhibited and the phase detector remains permanently enabled. With the AFT clamp removed, a large error voltage appears at the AFT output, driving the system back to the correct frequency. Since the LO loop is slow and the VCO loop is fast, the IF changes slowly and the VCO tracks it, maintaining phase lock until the final static conditions are reached. For large frequency errors during this period, the slew rate of the LO loop is increased but not to the extent where it would cause any VCO tracking problems. This technique allows the acquisition time of the circuit to be considerably shortened while still using a larger than normal time constant in the LO loop. In this way, any possibility of phase modulating the LO with video is removed. Figure 11 illustrates the AFT system in action.

To accommodate all types of tuners the LOs, positive or negative LO drive can be selected externally by operation of the AFT switch. The AFT switch also has a third position which disconnects the drive to the tuner. Under this condition, the TV set can be tuned in the normal manner and so appears to have a conventional type of AFT. Other PLL systems cannot be tuned manually in this way, having an abrupt capture characteristic, and because of this, have not gained general acceptance.

Figure 11. The AFT System in Action



APPLICATIONS INFORMATION

Alignment

The alignment of the MC44301 is very simple and inexpensive compared to other IF amplifier circuits, especially those using PLL demodulators. With a CW input signal of correct picture carrier frequency, the LO side of the 8.2 kΩ resistor in series with the loop is connected to a DC supply of approximately 2.5 V. The DC supply is adjusted until the output of the tuner is 45.75 MHz. The VCO coil is adjusted until lock is obtained and the voltage across the 8.2 kΩ resistor is zero. The DC supply is then removed (refer to Figure 12).

Component Selection

The IF input assumes 75 Ω output from the tuner. A SAW bandpass filter is used which has a low insertion loss while maintaining good triple transit response. Recommended sources for this filter include Murata 80Z series, SAF45MA80Z and Siemens M1963, which are packaged in a 5-pin SIP plastic package. Pinouts are identical, but the interface matching to IF will need to be modified for best performance. The evaluation PC board is laid out to accept either the SIP or a more expensive metal can filter.

The VCO coil is a bifiliar wound, center-tapped, 10 mm size shielded inductor, Figure 17 shows the construction details. Recommended sources for the (45.75 MHz IF) coil are TOKO TKANAS-T1390ADP, and Coilcraft M1300-A. For a higher IF frequency, the coil inductance must be decreased. In this case, the coil may be a custom having windings similar to the specified coil in Figure 17. Note that this coil has the same number of turns on both sides of the center-tap.

Evaluation PC Board

The evaluation PC board schematic in Figure 13 and the layout in Figures 14, 15, and 16 show a double sided board which is designed to accommodate additional external components and circuitry intended for use in 12 V systems and various tuner systems and applications. An optional sync separator circuit is recommended where a flyback pulse is not available, such as in set-top converters. Other optional circuitry is shown which helps to further improve the sound performance through additional quadrature and phase corrections. This is shown in the schematic for the Rev B evaluation PC board (Figure 13).

PCB Layout Considerations

The typical 5.0 V application circuit shown in Figure 6 uses a single sided PC board with very few external components. To maintain optimum performance, the placement and interconnection of some components such as the SAW filter and VCO tank are critical. These components are placed close to the IC to enable short trace lengths which are symmetrically placed and equal in length to avoid differential offsets and noise. In a single sided PC board layout the ground should flow around the device, and around the V_{CC} trace and other circuit traces as a continuous "sea of ground". Since the IF is very stable and immune to radiation, the device can be mounted on a single sided PC board without the customary and necessary shielding required in other IF systems. **However, do not use prototype and wire wrap construction techniques.**

9

Figure 12. Alignment Configuration

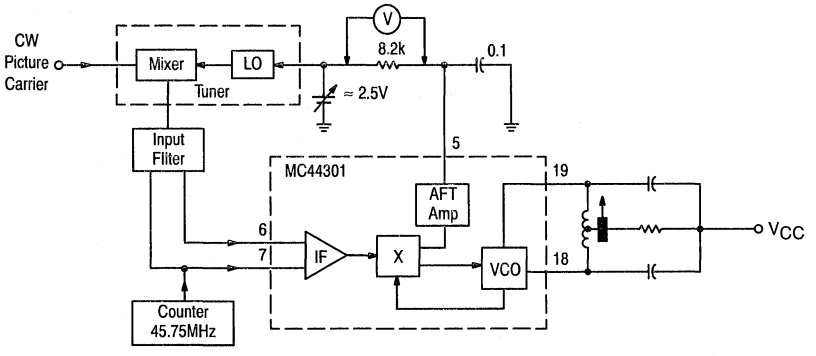
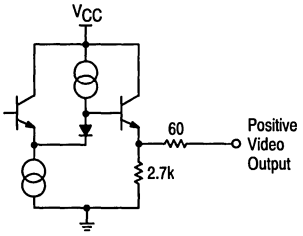
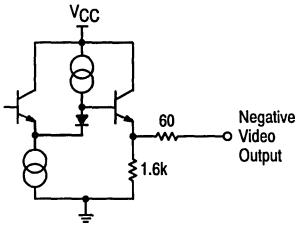
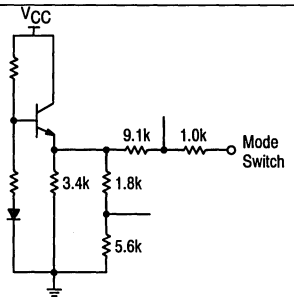
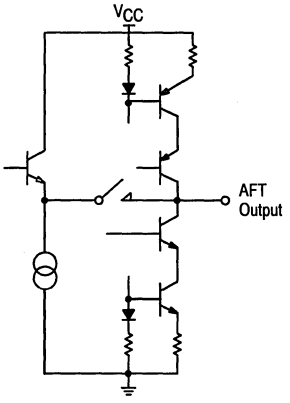
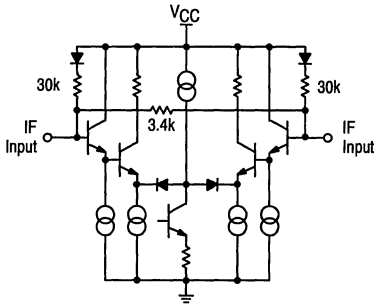
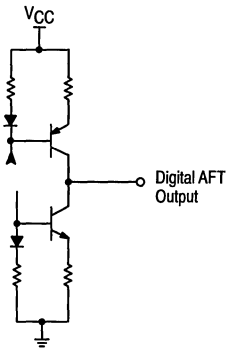
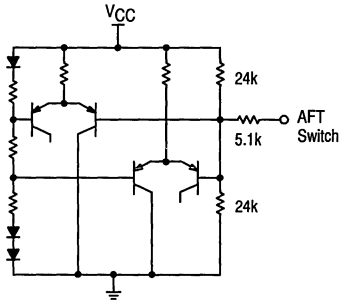
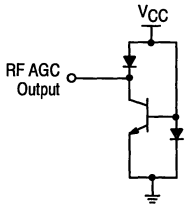


Table 2. Pin Function Desription

24 Pin (DIP)	28 Pin (SOIC)	Equivalent Internal Circuit	Functional Description/ External Circuit Requirements
1, 21, 23	1, 4, 11, 18, 24, 25, 26		**No Connection.**
2	2		**Positive Video Output With White Spot Noise Inversion** In the evaluation PCB a discrete external buffer (2N4402) is used to provide interface — this is not needed in the actual application.
3	3		**Negative Video Output Without White Spot Noise Inversion** Intended for sync separator use.
4	5		**Mode Switch** Selects positive or negative modulation. The pin is open for negative going video and grounded for positive going video.
5	6		**AFT Output** High output impedance push-pull current drive. Intended to give high AFT loop gain when used with high load impedances (i.e. direct connection to the tuner varactor diode). Drive is greatly increased for large frequency error to minimize pull-in time and clamped when PLL is not locked. External circuitry is provided in the evaluation PCB to allow adjustment of the drive to the tuner. This will not be needed in the actual application where the tuner is compatible with the IC. Polarity is controlled externally by the AFT switch.

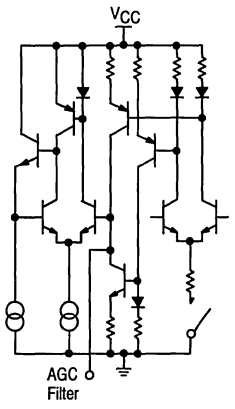
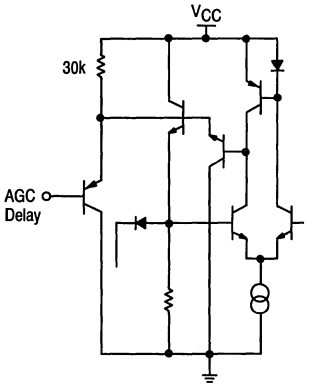
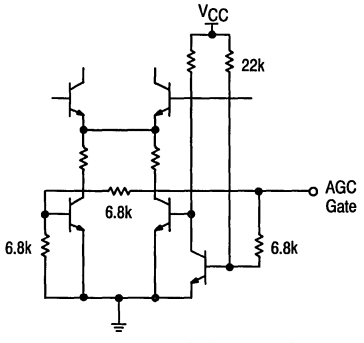
(continued)

Table 2. Pin Function Description

24 Pin (DIP)	28 Pin (SOIC)	Equivalent Internal Circuit	Functional Description/ External Circuit Requirements
6, 7	7, 8		**IF Inputs** Input leads should be kept short and symmetrical to avoid instability problems. The performance of the IF is greatly dependent upon the characteristics of the IF filter and upon the proper matching of the filter to the IF input. Refer to the evaluation circuit for recommended filters.
8	9		**Digital AFT Output** This is a tristate output having a ±300 kHz dead zone. Polarity is controlled externally by the AFT switch.
9	10		**AFT Switch** AFT is designed to accommodate all types of tuners and LOs. On the evaluation PCB, a jumper matrix provides three positions: 1) AFT switch pin to V_{CC} for positive LO drive, 2) AFT switch pin to ground for negative LO drive and 3) AFT switch pin to open which disconnects drive to the tuner.
10	12		**RF AGC Output** The output is designed for a reverse AGC tuner and will only sink about 0.8 mA maximum. At 5.0 Vdc V_{CC}, the maximum voltage on this pin is 5.8 Vdc, due to an internal clamping diode. In an application in which the tuner does not have a pull-up resistor, one must be added to the external circuit. With a tuner supply voltage at 8.0 Vdc, the load resistor should be at least 10 kΩ or greater.

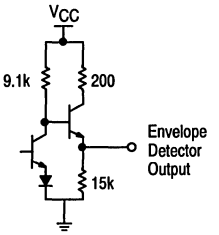
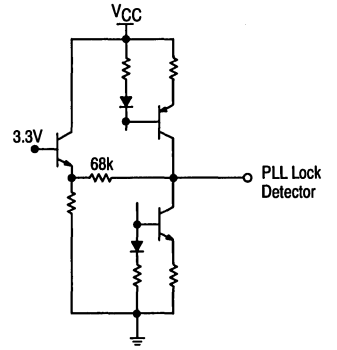
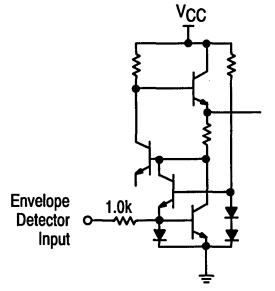
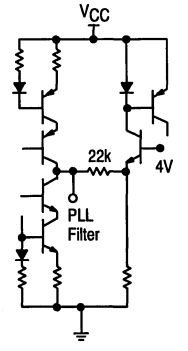
(continued)

Table 2. Pin Function Description

24 Pin (DIP)	28 Pin (SOIC)	Equivalent Internal Circuit	Functional Description/ External Circuit Requirements
11	13		**AGC Filter, AGC Control Voltage** Voltage level at this pin indicates AGC action by three gain control ranges. Increasing voltage at this pin gain reduces the tuner or IF. 0 Vdc to 2.5 Vdc is the IF initial control range, 2.5 Vdc to 4.0 Vdc is the nominal tuner RF control range, 4.0 Vdc to 5.0 Vdc further gain reduces the IF for very large signal level at the antenna.
12	14		**RF Tuner AGC Delay Adjustment** Below the potential set at this pin, the IF AGC is active and the tuner AGC is non-active. Above the potential set the IF amplifier gain is held constant while the tuner is gain reduced. The tuner takeover point normally corresponds to a 1.0 mVrms to 2.0 mVrms signal into the antenna. Thus, as the input increases beyond this level, the tuner AGC will activate, clamping the input drive into the IF at the associated 1.0 mVrms to 2.0 mVrms antenna threshold. The external AGC adjust network shown in Figure 13 provides 2.0 Vdc ± 0.2 Vdc at the AGC Adjust pin. This network may be modified for the desired range and resolution.
13	15		**AGC & Lock Gating Input** A 300 µA current pulse is required at this pin to gate on the AGC and lock systems. In most TV applications where negative modulation is used, the flyback pulse can be used to gate the AGC through a resistor. In applications where flyback is not available, the gate pulse can be acquired via a sync separator from the video output at Pin 2. The circuit shown in Figure 13 insures that the gate will be acquired in the proper time and level from the sync pulse.

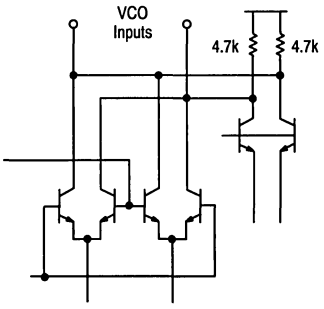
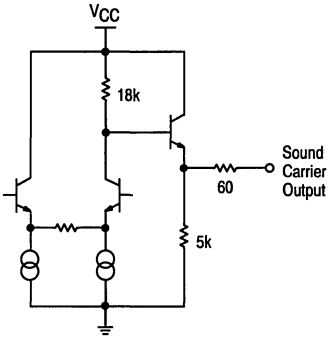
(continued)

Table 2. Pin Function Description

24 Pin (DIP)	28 Pin (SOIC)	Equivalent Internal Circuit	Functional Description/ External Circuit Requirements
14	16		**Envelope Detector Output** Detector for AM sound modulation (SECAM or descrambler signal).
15	17		**PLL Lock Detector** With 5.0 Vdc V_{CC}, lock is indicated by approximately 4.3 Vdc and zero signal is indicated by approximately 2.7 Vdc on this pin.
16	19		**Envelope Detector Input** AM sound subcarrier input.
17	20		**PLL Filter** The phase detector output after filtering produces a voltage which controls the frequency of the VCO. With 5.0 Vdc V_{CC}, there is approximately 3.2 Vdc present when VCO is locked and 3.1 Vdc when unlocked.

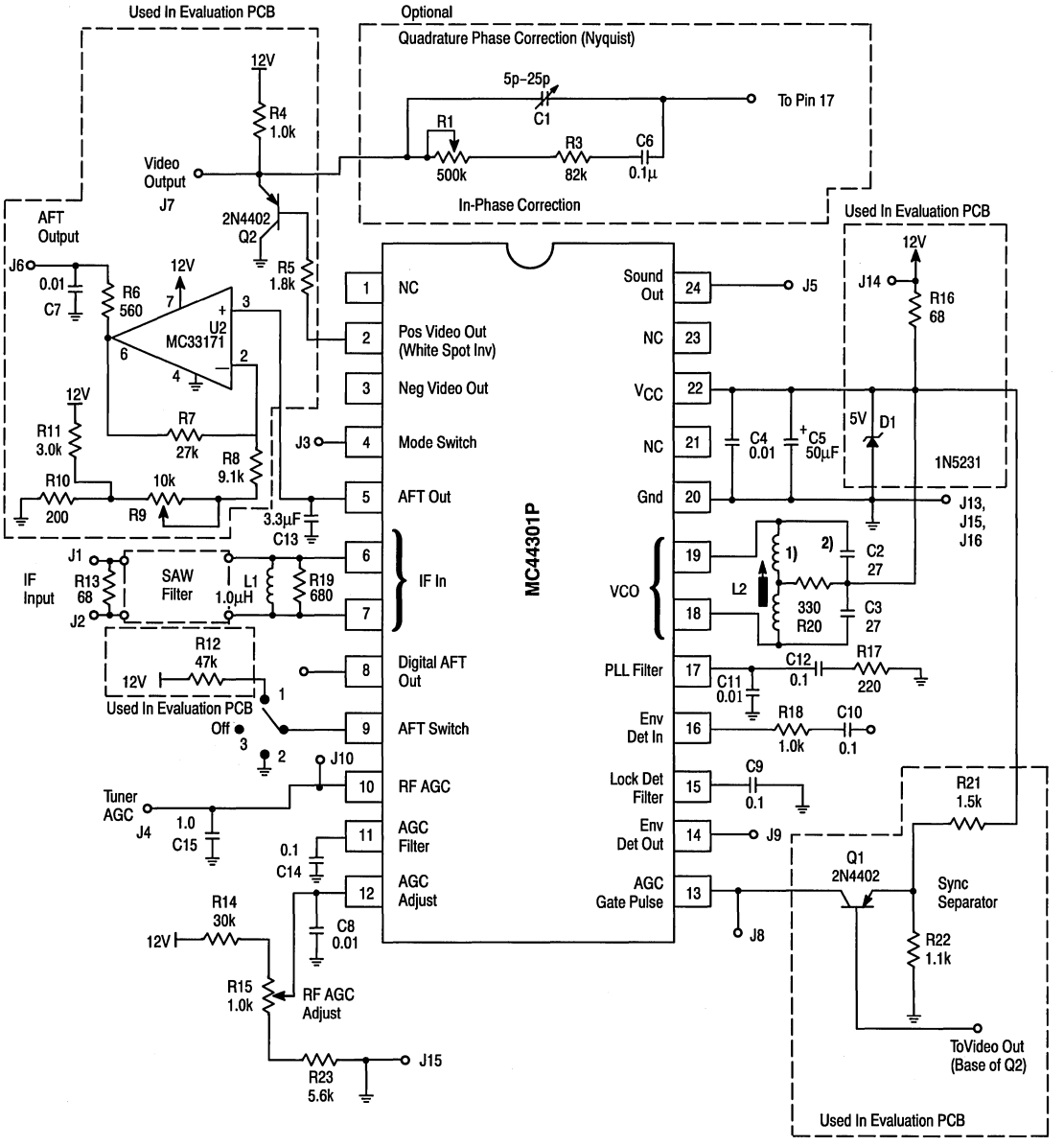
(continued)

Table 2. Pin Function Description

24 Pin (DIP)	28 Pin (SOIC)	Equivalent Internal Circuit	Functional Description/ External Circuit Requirements
18, 19	21, 22		**VCO Inputs** Care should be taken in layout by placing the VCO tank close to the IC pins with symmetrical traces to the shielded inductor. A center-tapped, bifiliar wound coil, previously defined, provides symmetrical tuning about the VCO frequency. The external VCO operates at half the IF frequency and is doubled on the IC chip.
20	23		**Supply Ground** Care should be taken to provide a continuous sea of ground or fill of the ground around the part, and traces in a single-sided PCB layout or a full ground plane on the component side of a double-sided layout.
22	27		**Supply Voltage (V_{CC})** Good RF decoupling must be provided close to this pin. At 25°C, maintain between 4.5 Vdc to 5.5 Vdc. At 0°C do not use less than 4.75 Vdc.
24	28		**Sound Carrier Output** Due to quadrature demodulation, the video components are suppressed at this output. However, with a vestigial sideband signal, high frequency video components will be present.

Note: Most pins on the IC have electrostatic protection diodes to V_{CC} and to ground. It is therefore *imperative* that no pin is taken below ground or above V_{CC} by more than one diode drop without current limiting.

Figure 13. MC44301P Universal Evaluation Circuit Schematic
Rev B — PCB



NOTES:
1) See Figure 17 for coil details.
2) Capacitors should be close tolerance, high Q components, such as silver mica — to insure dynamic frequency response and minimum bandwidth.

Figure 15. Component Placement and Silk Screen View

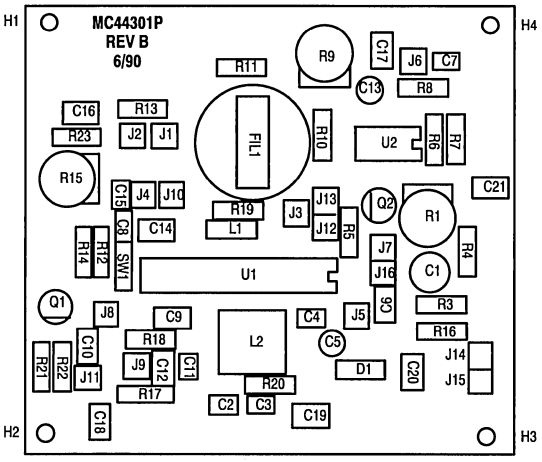


Figure 16. Component Side of PCB

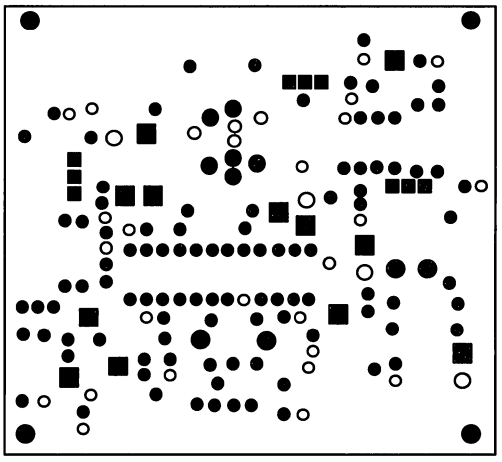
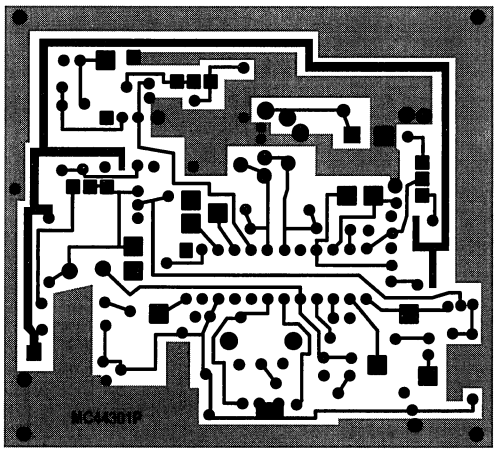


Figure 17. Circuit Side of PCB

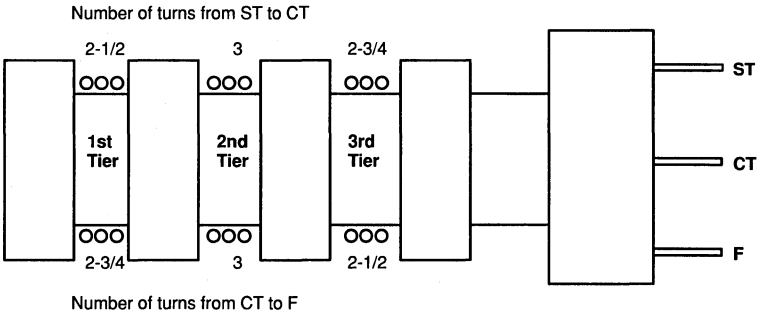


9

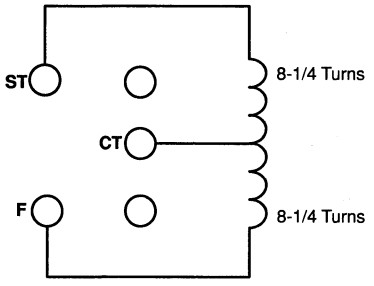
Winding Instructions

Use 38 AWG enameled wire. Start at "ST" pin, go to the top of the bobbin: wind 2-1/2 turns on the first tier; 3 turns on the second tier; 2-3/4 turns on the third tier, then go to the center tap "CT" pin. From the CT wind 2-3/4, 3 and 2-1/2 turns on the first, second and third tiers respectively, then finish the windings at the "F" pin. Wind the wire in the same direction, making sure it is wound tightly around the bobbin. The wire must be tinned to obtain the necesary solder connections. Application of solder directly to the enameled wire will remove the enamel and adequately tin it.

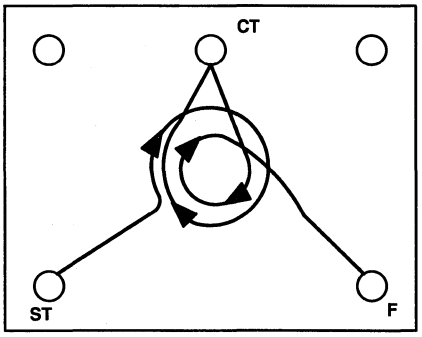
Figure 18. Winding Details for the VCO Coil



Bifiliar Wound 16-1/2 Turns



(Schematic)



(Bottom Vierw)

(TOKO Type 10 k Series or Coilcraft *Slot 10* Series Bobbin. Recommended sources for the coil are TOKO TKANAS-T1390ADP and the Coilcraft M1300-A)

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC44302

ADVANCED MULTISTANDARD TV VIDEO/SOUND IF

SILICON MONOLITHIC
INTEGRATED CIRCUIT

Product Preview

Advanced Multistandard TV Video/Sound IF

The MC44302 is a new multistandard single channel TV Video/Sound IF and PLL detector system for all standard transmission systems. This device enables the designer to produce a high quality IF system with white spot inversion, AFT and AGC. The MC44302 was designed with an emphasis on linearity to minimize sound/picture intermodulation.

Features:

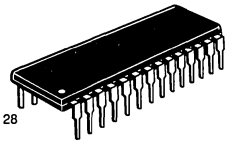
- Single Coil Adjustment for AFT and PLL
- VCO at 1/2 IF for Minimum Beats
- Simple Circuitry for Low System Cost
- White Spot Inversion
- Symmetrical ± 2.0 MHz Pull-In
- User Selectable Positive or Negative Modulation
- Simple Alignment Procedure
- AGC Gating Input Options

Sound Features:

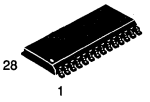
- Self-Tuning, Low Distortion FM IF Demodulator
- AM Sound IF for SECAM
- Sound Muting
- Variable and Constant Audio Outputs

Added Features Will Include:

- FM IF Demodulator
- AM Sound IF for SECAM
- AGC Gating Input Options
- Mode Select Pin for Selecting M, B-G-I, L or D2MAC
- Sound Muting



P SUFFIX
PLASTIC PACKAGE
CASE 710



DW SUFFIX
PLASTIC PACKAGE
CASE 751F
(SO-28L)

ORDERING INFORMATION

Device	Temperature Range	Package
MC44302DW	0° to + 70°C	SO-28L
MC44302P		Plastic DIP

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PRODUCT DESCRIPTION

Advanced TV Video/Sound IF for PAL, NTSC, SECAM and AM D2MAC

The MC44302 is a new multistandard TV Video/Sound IF that will have the present MC44301 as its basis. All present features and performance (with the exception of the AM detector) will be retained.

The circuit will demodulate the sound and video of all of the world's major television systems, namely PAL (system B, G, I), SECAM (system L), NTSC (system M), and AM D2MAC. Added features include self-contained AGC systems, AM and FM demodulation, volume control, and circuitry designed to meet Peri-TV socket requirements. PAL, NTSC and SECAM are selected via Pin 11 (voltage level) and AM D2MAC by grounding Pin 16 (normally used as a PLL filter).

Modes

PAL – In the PAL mode the AGC is self-gating via a horizontal PLL which is locked to the video. The gating pulse samples the video level during the sync interval.

FM sound demodulation is active in the PAL mode. The FM demodulator is self-tuning over the range of 5.5 MHz to 6.0 MHz. Other frequencies can be chosen by externally switching a capacitor on Pin 3. The FM demodulator has low distortion (approximately 0.1%) with better than 70 dB signal to noise ratio.

Two sound modes are possible in PAL; with and without sound muting. The sound output also has constant and variable audio outputs which meet the requirements of the European Peri-TV socket.

External audio can be switched through to the variable output via Pin 3. The internal variable signal is inhibited, but the internal constant audio still appears at Pin 24. This means that the external audio signal can be used internal to the TV chassis and its level adjusted via the volume control (Pin 1), while the internal audio can be taken from the constant output (Pin 24) via the Peri-TV socket to some external device such as a VCR.

SECAM – An advanced form of back porch gated AGC is used in SECAM mode. A long term peak white detector also controls the video output level over a limited range, correcting for any errors in the transmitted black level. In this way the AGC system retains the accuracy of a peak detecting system without the usual sacrifice of speed. The peak white detector uses the FM AFT filter capacitor at Pin 7. Thus the need for an extra pin and capacitor for this function is avoided.

The video switches maintain the same video sense as in PAL at the video outputs. The FM demodulator circuitry is disabled and the AM demodulator is switched on. All other aspects of the sound system are similar to PAL with regards to the audio switching.

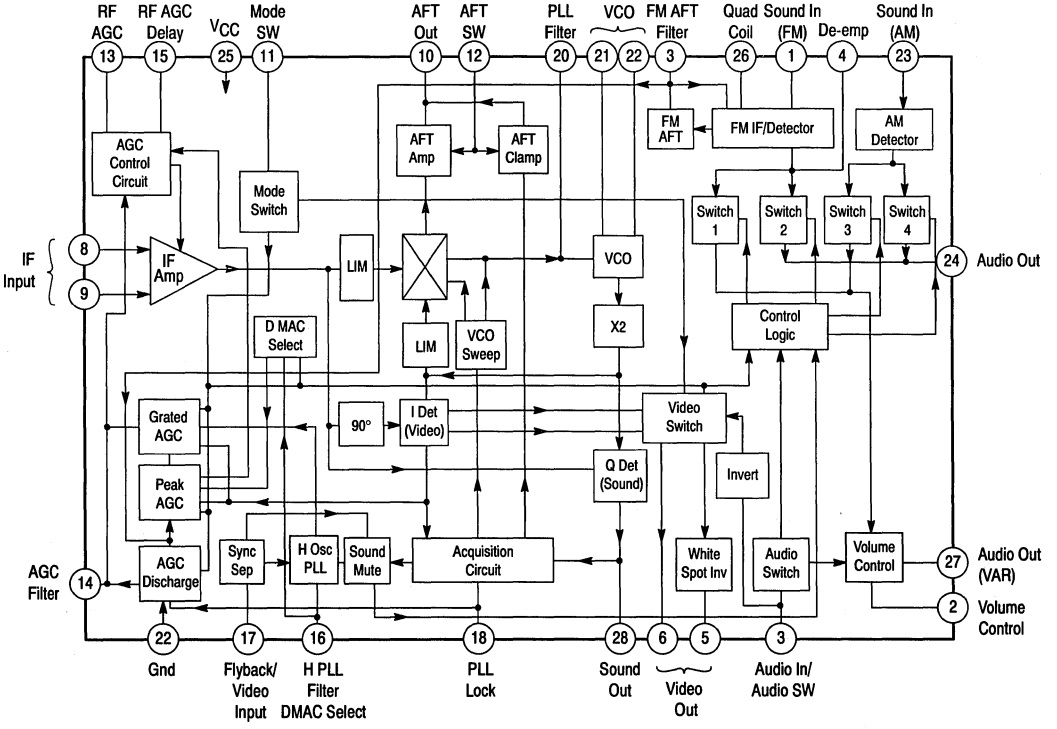
NTSC – The AGC system is the same for NTSC as in PAL mode. Both FM and AM demodulators are active when NTSC mode is activated. The demodulator FM is routed to the variable audio output to be used as the TV chassis drive for the loudspeaker. At the same time, the AM output is fed to the constant output. This can be used for suppressed sync scrambling systems, where the sync is on the sound carrier, to recover the sync signal.

Grounding Pin 3 when in the NTSC mode inverts the output video polarities. This is useful in scrambling systems that invert the video from line to line.

AM D2MAC – In this mode, the AGC system is a simple, very long time constant peak detector. The FM AFT filter capacitor at Pin 7 is used for this time constant.

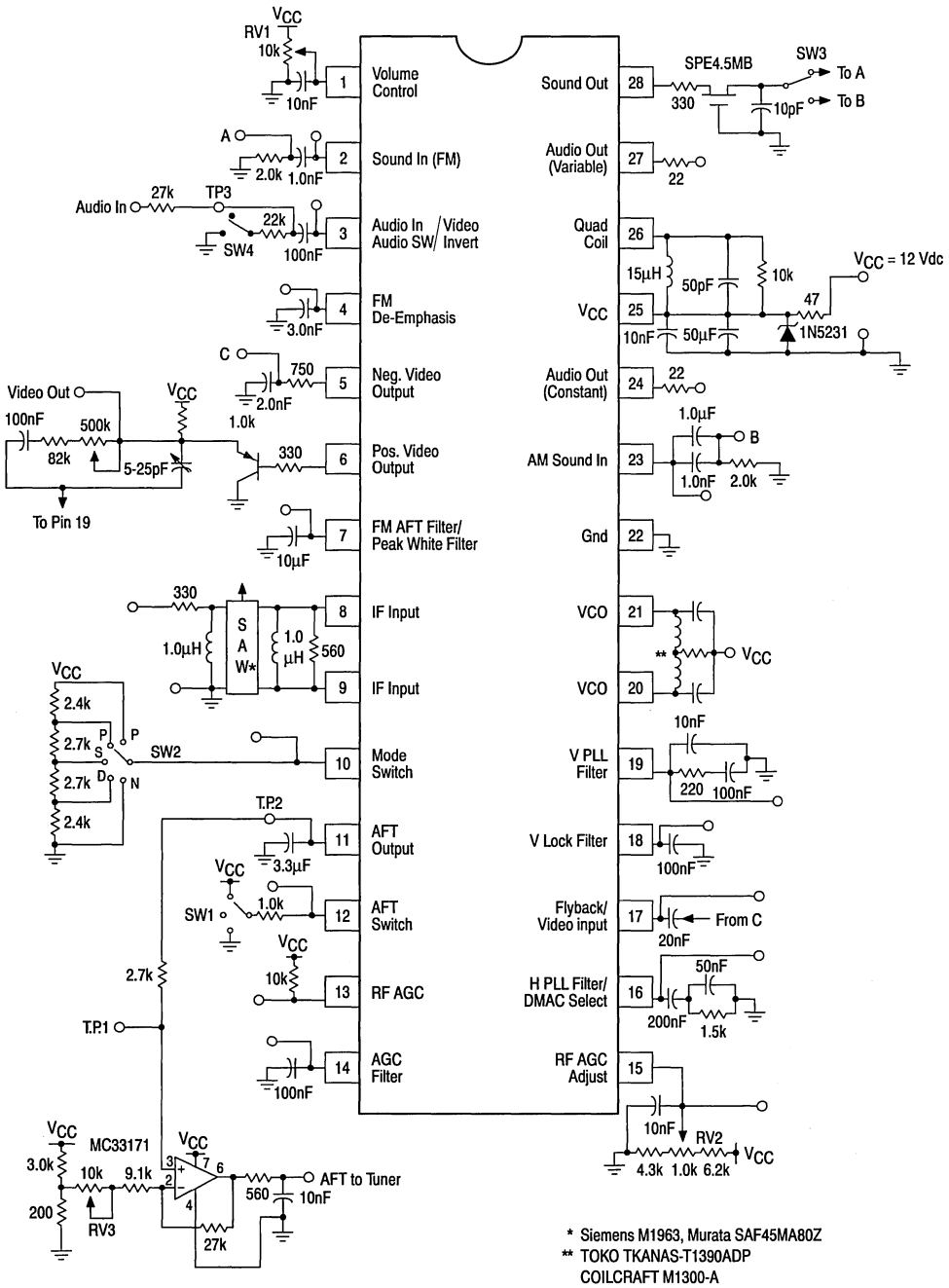
Both the FM and AM sound demodulators are switched off. This is to prevent interference with the D2MAC digital sound in the sync system.

Simplified Block Diagram



Single-sided board with GND between pins. The boards are to be single-sided, standard FR-4, with a tin-lead finish. There are no plated-thru holes and no solder mask is required.

PIN CONNECTIONS



* Siemens M1963, Murata SAF45MA80Z
** TOKO TKANAS-T1390ADP
COILCRAFT M1300-A

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC44615A

Advance Information

Convergence Waveform Generator IC for Projection TV

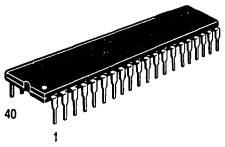
WAVEFORM GENERATOR IC FOR PROJECTION TV

The MC44615A is a bipolar integrated circuit designed to be used with the control circuitry for projection television convergence systems. The function of the integrated circuit is to generate the required voltage waveforms that will be applied to the convergence control circuitry. This control circuitry will apply them in the proper amplitude and combination for use in driving the convergence coils.

- Multistandard Operation Capable (10 kHz ≤ f_H ≤ 63 kHz) (45 ≤ f_V ≤ 120 Hz)
- Constant Amplitude Outputs, Independent of Frequency
- Complementary Output Waveforms
- Blanking Control of Output Waveforms
- Horizontal Phase Advance
- Standard Supplies (±5.0 Vdc)

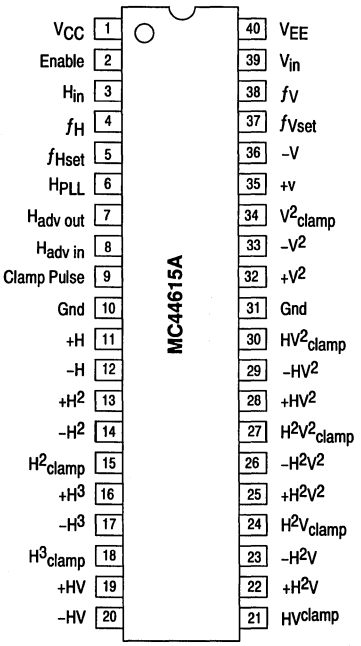
Functions (Nine Waveforms):

- Horizontal and Vertical Ramp
- Horizontal Parabola and Vertical Parabola
- Horizontal Ramp and Vertical Ramp Product
- Horizontal Parabola and Vertical Parabola Product
- Horizontal Ramp and Vertical Parabola Product
- Horizontal Parabola and Vertical Ramp Product
- Horizontal Cubic



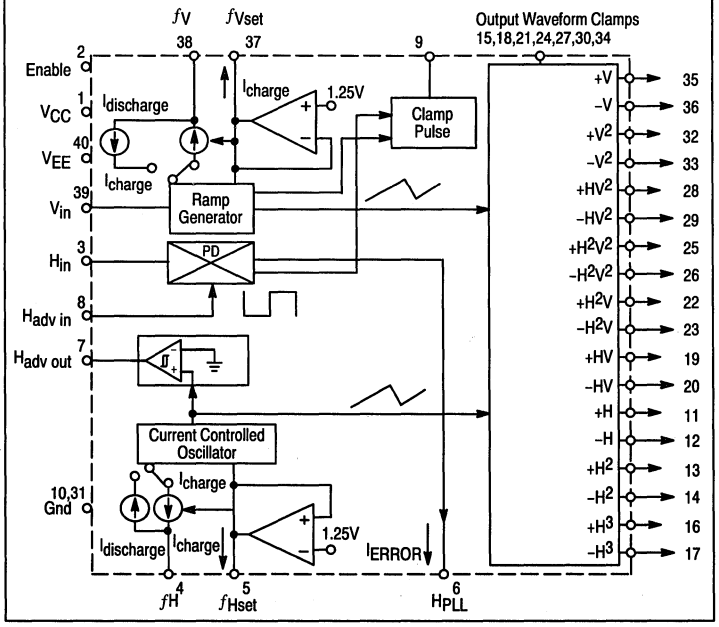
P SUFFIX
PLASTIC PACKAGE
CASE 711

PIN CONNECTIONS



(Top View)

Simplified Block Diagram

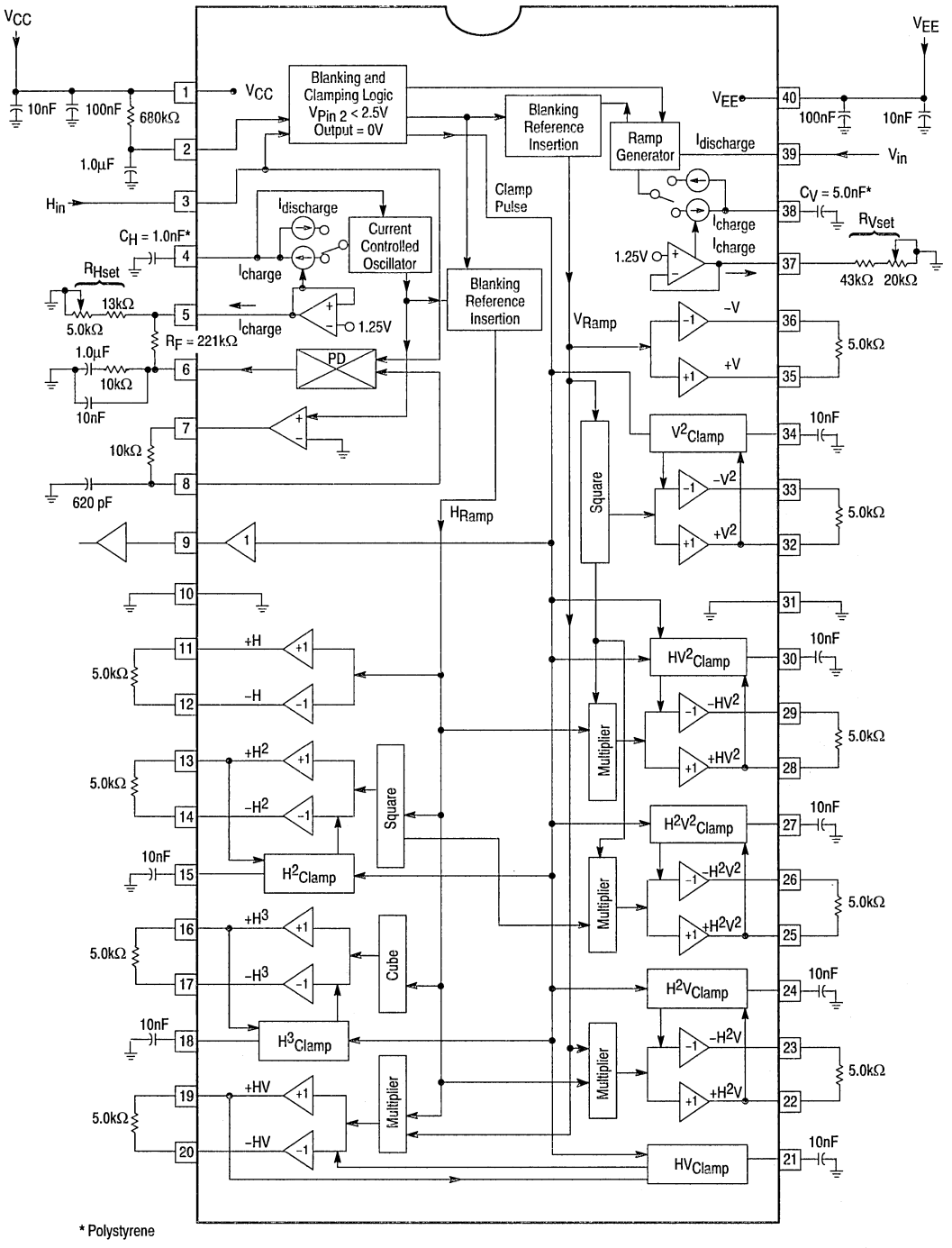


ORDERING INFORMATION

Device	Temperature Range	Package
MC44615AP	0° to +70°C	Plastic DIP

9

Figure 1. MC44615A Test Circuit



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage — Positive — Negative	V_{CC} V_{EE}	+6.0 –6.0	Vdc
Ambient Temperature	T_A	0 to 70	°C
Storage Temperature	T_{stg}	–65 to +150	°C
Junction Temperature	T_J	150	°C

RECOMMENDED OPERATING CONDITIONS

Characteristics	Pin(s)	Symbol	Value	Unit
Supply Voltage — Positive — Negative	1 40	V_{CC} V_{EE}	+4.5 to +5.5 –5.5 to –4.5	Vdc
Horizontal Sync Frequency — Max — Min	3	H_{in}	 63 10	kHz
Pulse Width — Max — Min			12 2.0	µs
Pulse Amplitude — Max Voltage (Tip) — Min Voltage (Baseline) (see Figure 2)			V_{CC} V_{EE} +0.5	Vdc
Vertical Sync Frequency — Max — Min	39	V_{in}	 120 45	Hz
Pulse Width — Max — Min			12 5.0	
Pulse Amplitude — Max Voltage (Tip) — Min Voltage (Baseline) (see Figure 2)			V_{CC} V_{EE} +0.5	Vdc
Peak Output Load Current	11–14, 16/17, 19/20, 22/23, 25/26, 28/29, 32/33, 35/36	I_L	±2.5	mA

9

FUNCTIONAL DESCRIPTION

Introduction

The MC44615A will provide 9 pairs, a function and its complement, of waveforms. These waveforms can then be used by the projection control circuitry for convergence.

The inputs of the MC44615A are the horizontal and vertical frequencies and an optional blanking input. Adapting this device to these frequencies is made by choosing external resistor – capacitor pairs. The enable input, a threshold sense that trips nominally at 2.5 V, can be used to delay the appearance of the waveforms and/or to turn off the waveforms during the blanking interval (or at any other time).

Inputs

Waveforms to the horizontal and vertical inputs (Pins 3, 39) must meet similar requirements except for the frequencies involved. The requirements can be described as follows:

$3.0\ V < V_{in}$ Peak $< 5.0\ V$;

$-4.5\ V < V_{in}$ Baseline $\leq 2.0\ V$.

$2.0\ \mu s \leq$ Pulse Width $< 1/(f_H)$ (Horizontal Input);

$2.0\ \mu s \leq$ Pulse Width $< 1/(f_V)$ (Vertical Input);

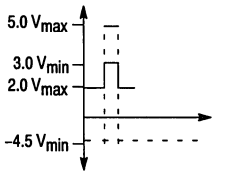
and the allowable frequencies of operation are:

$10\ kHz \leq f_H \leq 63\ kHz$,

$50\ Hz \leq f_H \leq 120\ Hz$

Figure 2 shows these requirements.

Figure 2. Valid Input Levels for Both Horizontal (Pin 3) and Vertical (Pin 39) Inputs



The blanking input, Pin 2, presents at least 500 kΩ to external signals and has a threshold of approximately +2.5 Vdc. At voltages *greater* than this threshold, the outputs are present. This pin can be biased high to keep the waveforms on, controlled by an external voltage to blank the output waveforms when desired, or charged-up with an external RC to delay the appearance of the output waveforms during power-up. During blanking, the output voltages are 0 Vdc ± 50 mV and power supply current remains unchanged. Since the input pins are all equipped with ESD diodes, voltages on these pins should never exceed V_{CC} or V_{EE} by more than 0.5 V.

ELECTRICAL CHARACTERISTICS (V_{CC} = +5.0 V, V_{EE} = −5.0 V, R_L = 2.5 kΩ, T_A = 25°C, f_H = 31,250 Hz, f_V = 31,250 Hz, see Figure 1)

Characteristics	Pin	Symbol	Min	Typ	Max	Unit
Supply Current	1 40	I_{CC} I_{EE}	25 −50	33 −43	40 −35	mA
Output DC Offset (all outputs when Pin 2 ≤ 2.0 Vdc)			−50	0	50	mV
Horizontal Delay Output Voltage Level — Low — High	7	H_{adv}	 −1.5 +0.7	 −1.1 +1.1	 −0.7 +1.5	Vdc
Timing (relative to Pin 3) (@ +750 Hz offset from $f_{Hfree\ run}$) (@ −750 Hz offset from $f_{Hfree\ run}$)			−1.5 −1.1 −1.9	0 +0.4 −0.4	+1.5 +1.9 +1.1	µs
Output Waveform Phase, Advance (involving horizontal functions) (C_{adv} = 1200 pF, R_{adv} = 10 kΩ)		t_{adv}	7.0	7.6	8.2	µs
Pull-in Range (C_H = 1.0 nF, R_F = 750 kΩ)			± 750	± 1300	—	kHz
Horizontal Ramp — Amplitude — Linearity	11, 12	±H	4.4 —	4.9 —	5.4 2.0	Vp-p %
Horizontal Parabola — Amplitude — Symmetry	13, 14	$\pm H^2$	2.25 —	2.7 —	3.3 12	Vp-p %
Cubic — Amplitude — Symmetry	16, 17	$\pm H^3$	4.1 —	4.9 —	5.9 12	Vp-p %
Vertical Ramp — Amplitude — Linearity	35, 36	±V	4.4 —	4.9 —	5.4 2.0	Vp-p %
Vertical Parabola — Amplitude — Symmetry	32, 33	$\pm V^2$	2.25 —	2.7 —	3.3 12	Vp-p %
Horizontal Ramp, Vertical Ramp Product Vertical Parabola Product	 19, 20 28, 29	 ±HV $\pm HV^2$	 4.0 4.0	 4.8 4.9	 5.8 5.8	Vp-p
Horizontal Parabola, Vertical Ramp Product Vertical Parabola Product	 22, 23 25, 26	 $\pm H^2V$ $\pm H^2V^2$	 2.1 2.0	 2.63 3.0	 3.25 3.6	Vp-p
Waveform Output Resistances All Outputs	11, 12, 13, 14, 16, 17, 19, 20, 22, 23, 25, 26, 28, 29, 32, 33, 35, 36		—	100	—	Ω

9

Horizontal Timing

To insure proper horizontal timing, the MC44615A uses a Phase-Locked-Loop to provide a reliable time base. The loop is externally accessible at the current controlled oscillator (ICO) (Pin 4, 5) and at the output of the phase detector (Pin 6). Figure 3 shows relevant internal circuitry and pin connections. This allows the system designer to tailor the timing and performance of the MC44615A.

The ICO is an RC type in which the horizontal frequency is determined by the charge and discharge rate of the capacitor at Pin 4. During charging, the voltage on the capacitor (C_H) is increased until it reaches an internally determined trip level. At this trip level the direction of the current at Pin 4 is reversed and the discharge process begins. During discharge, circuitry diverts the current available at Pin 4 internally and the capacitor discharges quickly to the bottom trip level where control circuitry switches the direction of Pin 4 current and the cycle begins again.

The charging current at Pin 4 is determined by the current *out* of Pin 5, which is mirrored at Pin 4. The current out of Pin 5 is set by a nominal 1.25 V stable reference and the resistance at this node. This also provides a means of modulating the charging current at Pin 4 by injecting the error current from the phase detector at Pin 6 to Pin 5.

At Pin 6, and connected to Pin 5 by the feedback resistor (R_F), are the filter components of the H_{PLL}. These components were chosen to insure fast tracking over the possible horizontal operating frequencies. (Refer to application notes AN553 and AN921 for information regarding design of the filter.) The effect of this filter and the other H_{PLL} components provides a capture range equal to the lock range and a stable horizontal time base over the possible horizontal operating frequencies.

The error current from the phase detector is determined by the product of the pase detector sensitivity (µ) and the phase error (ϕ_E) between the inputs H_{in} and at Pin 8. The voltage difference between Pin 6 and Pin 5 will change to accommodate the error current.

$$I_{ERROR} = \mu\ \phi_E,$$

where the phase detector sensitivity is,

$$\mu = 191E\text{-}6\ A/rad.$$

The charging current is now defined and is,

$$I_4 = I_5 = \frac{1.25\ V}{R_{Hset}} - I_{ERROR}.$$

With the MC44615A there is also the possibility of phase advancing the output waveforms to compensate for the integration effects of the horizontal convergence coils. Phase advance is done by an external RC combination at Pin 7, where a square wave at the horizontal frequency is output, and at Pin 8, the input to the horizontal phase detector, PD. The square wave provides one input to the phase detector, the input at Pin 3 is the other.

A delay to the square wave at the horizontal frequency advances the output waveforms by delaying the square wave input to the phase detector. Representative circuitry at Pins 7 and 8 is shown in Figure 4 and should be considered with Figure 3 since Pin 6 links them.

Vertical Timing

Vertical timing for the MC44615A is determined by the frequency of the input at Pin 39 and the charging rate of the capacitor at Pin 38. Representative circuitry for relevant pins is shown in Figure 5. The vertical timing is set by a ramp generator, the frequency of the generated ramp being determined by the current drawn out of Pin 37 ($1.25 / R_{Vset}$). At the beginning of a vertical cycle, the current sourced by Pin 37 is mirrored out of Pin 38, charging the capacitor at Pin 38

Figure 3. Horizontal Frequency Control

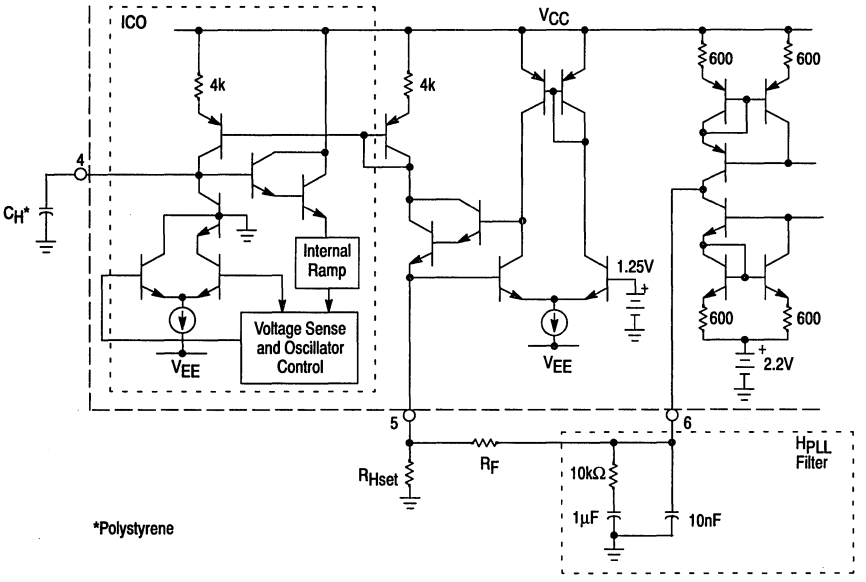


Figure 4. Horizontal Input and Phase Advance

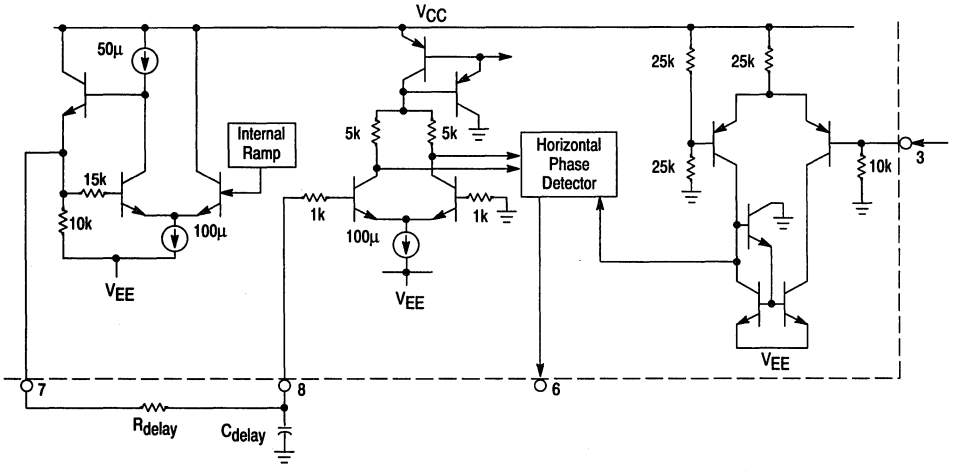
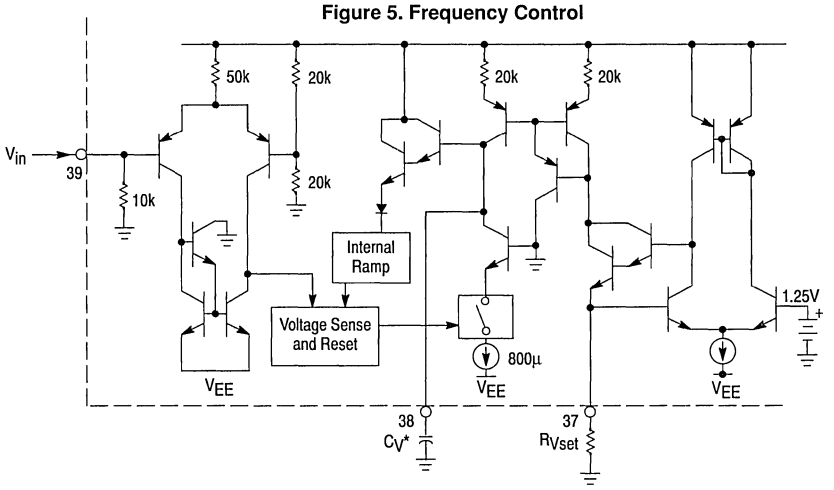


Figure 5. Frequency Control



with a constant current resulting in a linear ramp. *The charging current of the capacitor (C_V) must be set so the capacitor voltage reaches 2.5 V, when the next vertical sync pulse arrives to discharge the capacitor.* The current, sourced by Pin 37, is again provided to the capacitor and the cycle continues.

Outputs and Output Clamps

The various output waveforms are developed by internal circuitry and are the result of operations on the internal vertical and horizontal ramps. The waveforms and their complements are then made available at the output pins and are capable of supplying at least 2.5 mA per pin. A simplified schematic of the output stage is shown in Figure 6. It is clear from the figure that output voltages should never exceed V_{CC} or V_{EE} by more than 0.5 V or excessive currents will flow.

During vertical sync intervals, circuitry blanks the outputs while clamping circuitry works to cancel out DC offsets in the waveforms. After the leading edge of a vertical sync pulse, blanking logic blanks the outputs for the time spanned by the first two horizontal pulses (see Figure7B). Clamping circuitry works for the line period between the first two blanking intervals. Internal circuitry present at the clamp pins is shown in Figure 7A, and a diagram showing relative timing is shown in Figure 7B.

Figure 6. Internal Circuitry for Output Waveforms

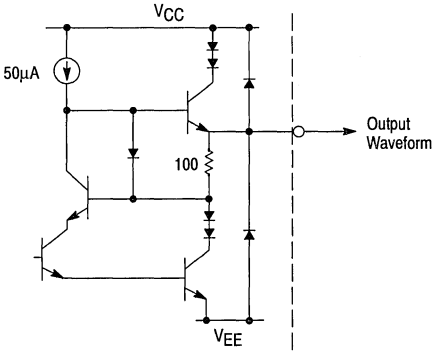


Figure 7A. Clamp Circuitry for Output Waveforms

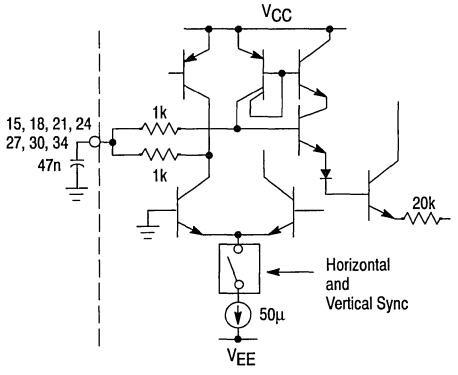
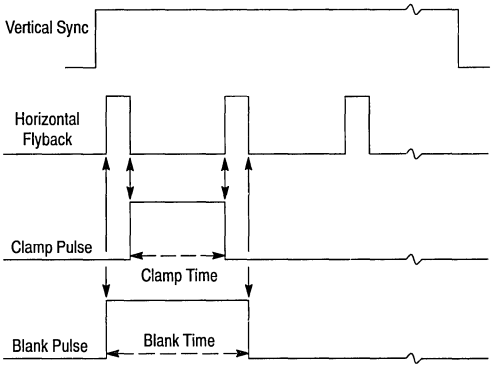


Figure 7B. Blanking and Clamping Diagram



APPLICATION INFORMATION

The following information is provided to assist designing-in the MC44615A.

Horizontal Timing

Since the charge and discharge of the capacitor at Pin 4 (C_H) is done with constant currents, the voltage waveform of the capacitor voltage is,

$$\pm\Delta V = \pm \frac{I\,\Delta t}{C} \quad \text{where, } \Delta t \text{ is the trace or retrace time.}$$

The horizontal frequency is then the inverse of the sum of the charge time and the discharge time,

$$f_{horizontal} = \frac{1}{(t_{charge} + t_{discharge})} \quad \text{where,}$$

t_{charge} = trace time, and $t_{discharge}$ = retrace time.

This relates the trace and retrace time to element values, internal quantities and a design variable, I_{charge}. So,

$$t_{charge} = \frac{C_H\,\Delta Vp\text{-}p}{I_{charge}} \quad \text{and} \quad t_{discharge} = \frac{C_H\,\Delta Vp\text{-}p}{I_{discharge}}$$

$\Delta Vp\text{-}p$ and $I_{discharge}$ are fixed ($I_{discharge}$ is typically 1.4 mA and $\Delta Vp\text{-}p$ is $\cong$ 2.5 Vp-p.). If C_H is chosen to meet the requirements of retrace time and,

trace time >> retrace time, then $t_{charge} >> t_{discharge}$,

$$\text{then, } f_{horizontal} \simeq \frac{1}{t_{charge}}, \text{ or } f_{horizontal} \simeq \frac{I_{charge}}{C_H\,\Delta Vp\text{-}p}$$

Determining the current I_{charge} then gives the horizontal frequency, since C_H and $\Delta Vp\text{-}p$ are known.

Refering to Figure 3, the current out of Pin 5 is the current I_{charge} and is composed of,

$$I_{charge} = \frac{1.25}{R_{Hset}} - I_{ERROR}$$

where I_{ERROR} is the current from the phase detector *when the loop is locked* and was determined in the **FUNCTIONAL DESCRIPTION** text to be,

$$I_{ERROR} = \mu\,\phi E$$

The horizontal frequency is now defined as,

$$f_{horizontal} = \left\{\frac{1.25}{R_{Hset}} \pm \mu\,\phi E\right\}\left(\frac{1}{C_H\,\Delta Vp\text{-}p}\right), \text{ or}$$

$$f_{horizontal} = f_{free\ run} \pm \Delta f,$$

where Δf is the frequency difference between the horizontal free run frequency and the frequency of the input signal, R_{Hset} is the resistance from Pin 5 to ground, C_H is the capacitor at Pin 4 and R_F is the resistor between Pins 5 and 6. It must be emphasized that this equation holds true only when the loop is locked.

The maximum phase error for which the loop is stable is determined experimentally and is,

$$\phi E_{max} \simeq 0.124 \text{ rad.}$$

The lock range then is defined by the product of this maximum phase error and the loop gain (K_V). The loop gain is the product of the phase detector sensitivity (μ) and the oscillator sensitivity (β).

$$\mu = 191\text{ E-}6 \qquad \beta = 1/2.5\,C_H \qquad K_V = \frac{191E\text{-}6}{2.5\,C_H}$$

$$f_{lock} = \Delta f_{max} = \pm \frac{191E\text{-}6\ 0.124}{2.5\,C_H} \simeq \pm \frac{9.5E\text{-}6}{C_H}$$

(*The value of f_{lock} should be kept small enough to prevent loop-lock on harmonics. A general rule of thumb would be f_{lock} < 10% of the desired horizontal frequency.*) Then I_{ERROR} is less than 10% of I_{charge} and so the horizontal frequency is almost entirely determined by:

$$f_{horizontal} \simeq \frac{1.25}{R_{Hset}\,C_H\,\Delta Vp\text{-}p}\ \Delta Vp\text{-}p \simeq 2.5,$$

so this becomes,

$$f_{horizontal} \simeq \frac{1}{2\,R_{Hset}\,C_H},$$

which is also the horizontal free-run frequency. The horizontal free-run frequency should be set at or very near the desired horizontal frequency since the lock range is centered about this frequency.

So a design would meet the following requirements:

1) The value of C_H satisfies the requirements for retrace time

$$\text{or, required retrace time} \geq \frac{C_H\,\Delta Vp\text{-}p}{I_{discharge}},$$

where $I_{discharge}$ is $\simeq$ 1.4 mA and $\Delta Vp\text{-}p$ is $\simeq$ 2.5 Vp-p.

2) The value of the resistance from Pin 5 to ground is given by

$$R_{Hset} \simeq \frac{1}{2\,f_{horizontal}\,C_H}$$

*(The value of the resistor calculated for R_{Hset} should be considered **approximate.** The 5.0 kΩ pot, shown in the Application Circuit of Figure 10, is recommended for optimization.)*

3) The capacitor C_H is such that the lock range is a reasonable choice given by,

$$f_{lock} \simeq \pm \frac{9.5E\text{-}6}{C_H}$$

Vertical Timing

To set the vertical timing a capacitor-resistor pair must be chosen (refer to Figure 5). The vertical timing section is similar to the horizontal section in that the frequency is determined by the charge and discharge rate of a capacitor (at Pin 38). The vertical ramp generator is an injection type, so a vertical input must be present for vertical outputs to be present. **The vertical ramp generator is not free running.**

$$\text{Again, } \pm\Delta V = \pm \frac{I\,\Delta t}{C_V}$$

describes the capacitor voltage for the charge and discharge currents made available at Pin 38. Further, if $t_{retrace} << t_{trace}$, then,

$$f_{vertical} = fV \simeq \frac{1}{\Delta t_{trace}} = \frac{1}{\Delta t_{charge}}$$

and the vertical frequency is determined by the charging current, the ΔV and the capacitor value. The reference voltage for developing the charging current is present at Pin 37 and is nominally 1.25 V. The charging current is then defined by the resistance at this node,

$$I_{charge} = \frac{1.25}{R_{Vset}}$$

The resistance required can be determined for a particular frequency and capacitor combination. **The capacitor voltage (ΔV), must be nominally 2.5 Vp-p for the specified full scale vertical outputs.** Using this value, the proper combination R_{Vset} and C_V can be calculated. The current available to discharge C_V is approximately 800 μA. So a practical C_V value is described by,

$$C_V \leq \frac{800\ \mu A\ \Delta t}{\Delta V}\text{, where } \Delta t \leq \text{required retrace time.}$$

This value of C_V is next used to calculate the value R_{Vset} considering the vertical frequency desired,

$$I_{charge} = \frac{1.25}{R_{Vset}} = \frac{C_V\,\Delta V}{\Delta t} = C_V\,\Delta V\,fV\text{, or}$$

$$R_{Vset} \simeq \frac{1.25}{C_V\,\Delta V\,fV} = \frac{1.25}{C_V\,2.5\,fV} \simeq \frac{1}{2\,C_V\,fV}\ .$$

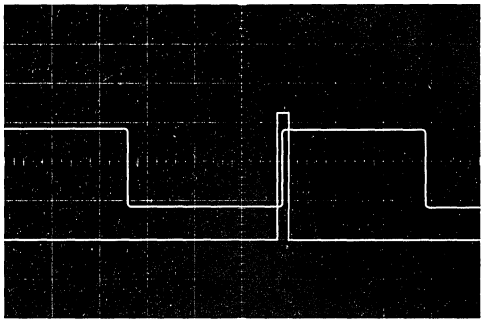
*(The equation given for R_{Vset} is **approximate** and should be used only as a starting point. The 20 kΩ pot in the applications circuit of Figure 10 is used to optimize this value.)*

Optional Horizontal Phase Advance

The MC44615A allows the output waveforms to be "advanced" relative to the incoming horizontal input at Pin 3 by delaying the internal oscillator input into the phase detector. The delay is accomplished with an external RC combination at Pins 7 and 8 (refer to Figure 6). The resistor, R_{delay}, also couples the two pins and provides the signal path to the phase detector, P_D. In any event, **whether or not delay is desired, the signal output at Pin 7 must be coupled to Pin 8.** A 10 kΩ resistor can be used to couple Pins 7 and 8, if no delay is desired.

The amount of "advance" desired can be calculated by considering the phase detector's treatment of the inputs. The inputs to the phase detector, horizontal sync and signal, injected at Pin 8, are phase-locked so that they appear as shown in Figure 8. The **center** of the horizontal sync pulse is phase-locked to the zero crossing of the internal oscillator that is output at Pin 7.

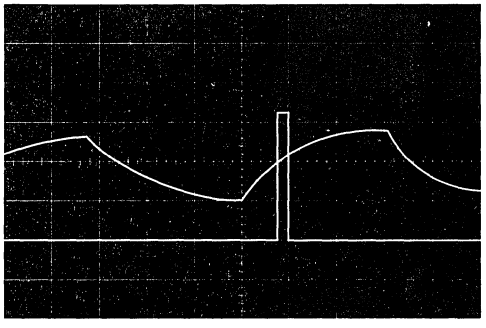
Figure 8. Phase Detector, Horizontal Sync and Signal Inputs



time base = 10 μs/Div

So a delay of the oscillator zero crossing will force the loop to lock the incoming horizontal sync input to a phase delayed representation of the internal horizontal oscillator. The outputs are not delayed, so as a result they are phase advanced. Figure 9 shows the result of about 8.0 μs of delay placed on the oscillator square wave output at Pin 7.

Figure 9. Oscillator Square Wave Output



time base = 10 μs/Div

The amount of delay or advance required is calculated according to,

$$R_{delay}\,C_{delay} = \frac{t_{advance}}{0.69}\ .$$

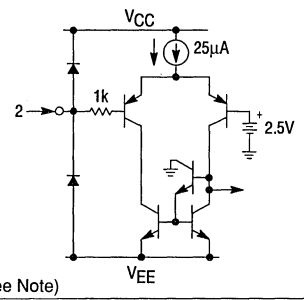
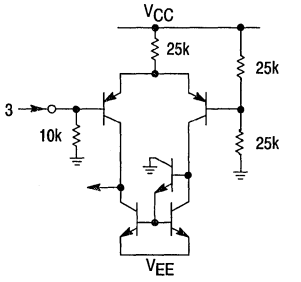
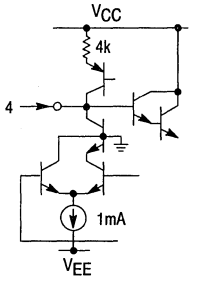
The minimum impedance coupled to ground should be greater than 4.0 kΩ and a maximum of 20 kΩ .

Optional Waveform Disable

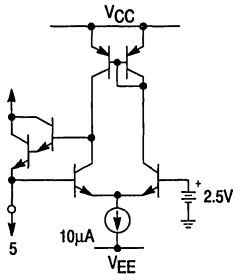
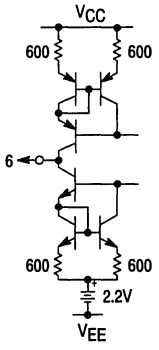
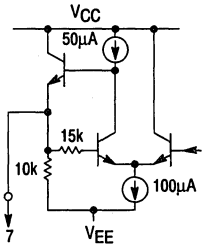
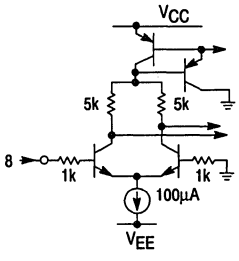
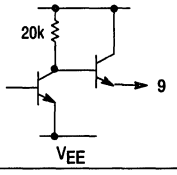
Pin 2 on the MC44615A is provided for blanking the output waveforms. When the voltage applied at this pin is less than about 2.5 V, all outputs are blanked and within 50 mV of ground. The impedance presented at this pin is > 500 kΩ. The outputs can be permanently enabled by a pull-up resistor from Pin 2 to the positive supply, V_{CC}. An external RC is anotheroption. A resistor (10 kΩ to 100 kΩ) coupled from Pin 2 to V_{CC} and a capacitor coupled from Pin 2 to ground will delay the appearance of the waveforms by an amount,

$$t_{delay} = RC\ (0.69)$$

PIN DESCRIPTION TABLE

Symbol	Pin	Internal Equivalent Circuit	Description
V_{CC}	1		Positive rail voltage. Requires 33 mA at 4.5 < Vdc < 5.5.
Waveform Blank	2	 (See Note)	Output waveform blanking pin. An external RC may be used to delay the appearance of the output waveforms. Waveforms are present when Pin 2 voltage exceeds 2.5 V. Input impedance is nominally 500 kΩ.
H_{in}	3		Positive horizontal flyback input. Input impedance is nominally 10 kΩ. (See Figure 2)
f_H	4		Horizontal oscillator capacitor (C_H). The charge and discharge rate of this capacitor's voltage determines the horizontal frequency. Charging current set predominantly by R_{Hset}. (See Figure 3)

Note: All pins (except V_{CC} and V_{EE}) have ESD diodes between V_{CC} and V_{EE}.

Symbol	Pin	Internal Equivalent Circuit	Description
f_{Hset}	5		Horizontal charge current set. An internally regulated 1.25 Vdc, and the external resistance (R_{Hset}) at this pin determines the horizontal free run charging current. Also, the feedback current from the H_{PLL} filter is input at this pin.
H_{PLL}	6		Horizontal Phase Detector output pin. An external filter circuit between this pin and Pin 5 determines the selectivity of the Phase Detector and provides the feedback path for the Horizontal Phase-Locked-Loop.
$H_{adv\ out}$	7		Square wave output at the horizontal oscillator frequency. An external RC added at this pin advances the phase of the waveforms. External impedance to ground should be > 4.0 Ω, and < 20 kΩ.
$H_{adv\ in}$	8		Horizontal phase detector input. The path between this pin and Pin 7 can be used to delay the squared output from the horizontal oscillator. This results in a phase advance of the horizontal waveforms. Input impedance is nominally 200 kΩ .
Clamp Pulse	9		Clamp Pulse output. This pulse is initiated by the vertical and horizontal flyback pulses to enable the clamp circuits. The timing of the pulse is shown in Figure 9.

Note: All pins (except V_{CC} and V_{EE}) have ESD diodes between V_{CC} and V_{EE}.

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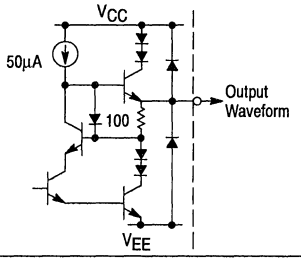
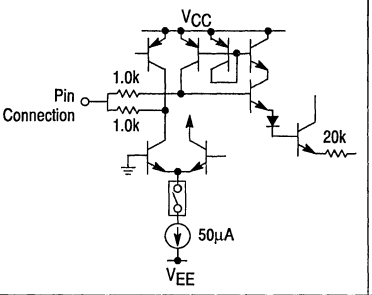
Symbol	Pin	Internal Equivalent Circuit	Description
Gnd	10		Ground connection.
+H	11		Horizontal ramp output.
–H	12	(See Pin 11)	Complement horizontal ramp output.
$+H^2$	13		Horizontal parabola output. The squared result of the positive horizontal ramp.
$-H^2$	14		Complement horizontal parabola output.
H^2Clamp	15		Horizontal parabola clamping pin. An external capacitor works to cancel DC offset. Typically, coupled to ground with a 47 nF capacitor.
$+H^3$	16	(See Pin 11)	Cubic output.
$-H^3$	17		Complement cubic output.
H^3Clamp	18	(See Pin 15)	Cubic clamping pin. An external capacitor works to cancel DC offset. Typically, coupled to ground with a 47 nF capacitor.
+HV	19	(See Pin 11)	Horizontal and vertical ramps product.
–HV	20		Complement horizontal and vertical ramps product.
HVClamp	21	(See Pin 15)	Horizontal and vertical ramp product clamping pin. An external capacitor works to cancel DC offset. Typically, coupled to ground with a 47 nF capacitor.
H^2V	22	(See Pin 11)	Positive product of horizontal parabola and vertical ramp.
$-H^2V$	23		Complement horizontal parabola and vertical ramp product.
H^2VClamp	24	(See Pin 15)	Horizontal parabola and vertical product clamping pin. An external capacitor works to cancel DC offset. Typically, coupled to ground with a 47 nF capacitor.
$+H^2V^2$	25	(See Pin 11)	Horizontal parabola and vertical parabola product.
$-H^2V^2$	26		Complement horizontal parabola and vertical parabola product.
H^2V^2Clamp	27	(See Pin 15)	Horizontal parabola and vertical parabola product clamping pin. An external capacitor works to cancel DC offset. Typically, coupled to ground with a 47 nF capacitor.
$+HV^2$	28	(See Pin 11)	Horizontal ramp and vertical parabola product.
$-HV^2$	29		Complement horizontal ramp and vertical parabola product.

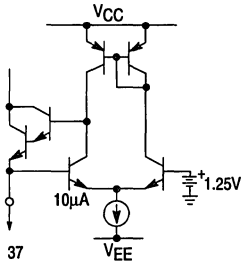
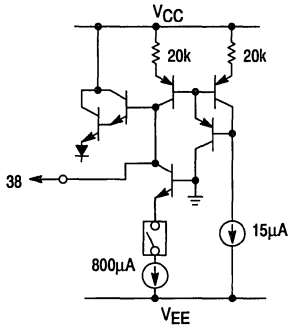
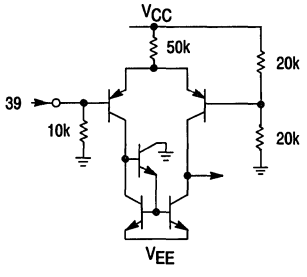
Symbol	Pin	Internal Equivalent Circuit	Description
HV^2Clamp	30	(See Pin 15)	Horizontal ramp and vertical parabola product clamping pin. An external capacitor works to cancel DC offset. Typically, coupled to ground with a 47 nF capacitor.
Gnd	31		Ground connection.
$+V^2$	32	(See Pin 11)	Vertical parabola.
$-V^2$	33		Complement vertical parabola.
V^2Clamp	34	(See Pin 15)	Vertical parabola clamp pin. An external capacitor works to cancel DC offset. Typically, coupled to ground with a 47 nF capacitor.
+V	35	(See Pin 11)	Vertical ramp.
–V	36		Complement vertical ramp.
fVset	37		Vertical charge current set. An internally regulated 1.25 Vdc, and the external resistance at this pin determines the charging current for the capacitor, C_V, connected to Pin 38.
fV	38		Vertical ramp generator capacitor (C_V). The charge and discharge rate of this capacitor determines the vertical ramp rate.
V_{in}	39		Positive vertical flyback input pin, presents 10 kΩ to input waveform. (See Figure 2)
V_{EE}	40		Negative supply pin. Requires 43 mA at –5.5<Vdc< –4.5.

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Figure 10. MC44615A Application Schematic

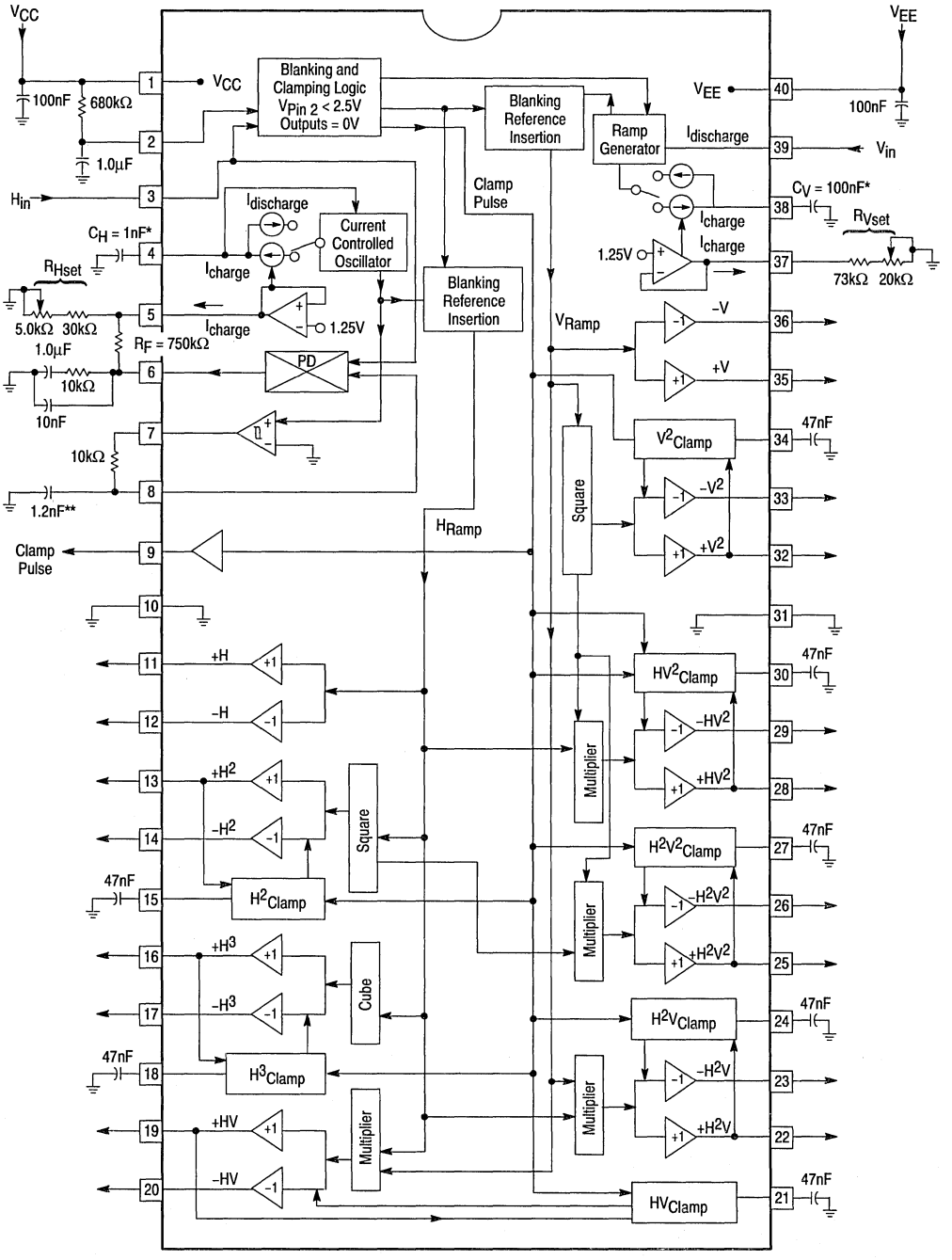


Figure 10 shows an application circuit with component values applicable for NTSC operation, or

* Polystyrene
** Silver Mica

$f_{horizontal}$ = 15,734 Hz f_{lock} = 9.5 kHz
$f_{vertical}$ = 60 Hz $f_{pull\text{-}in}$ = 1.4 kHz

Figure 11. Vertical Timing

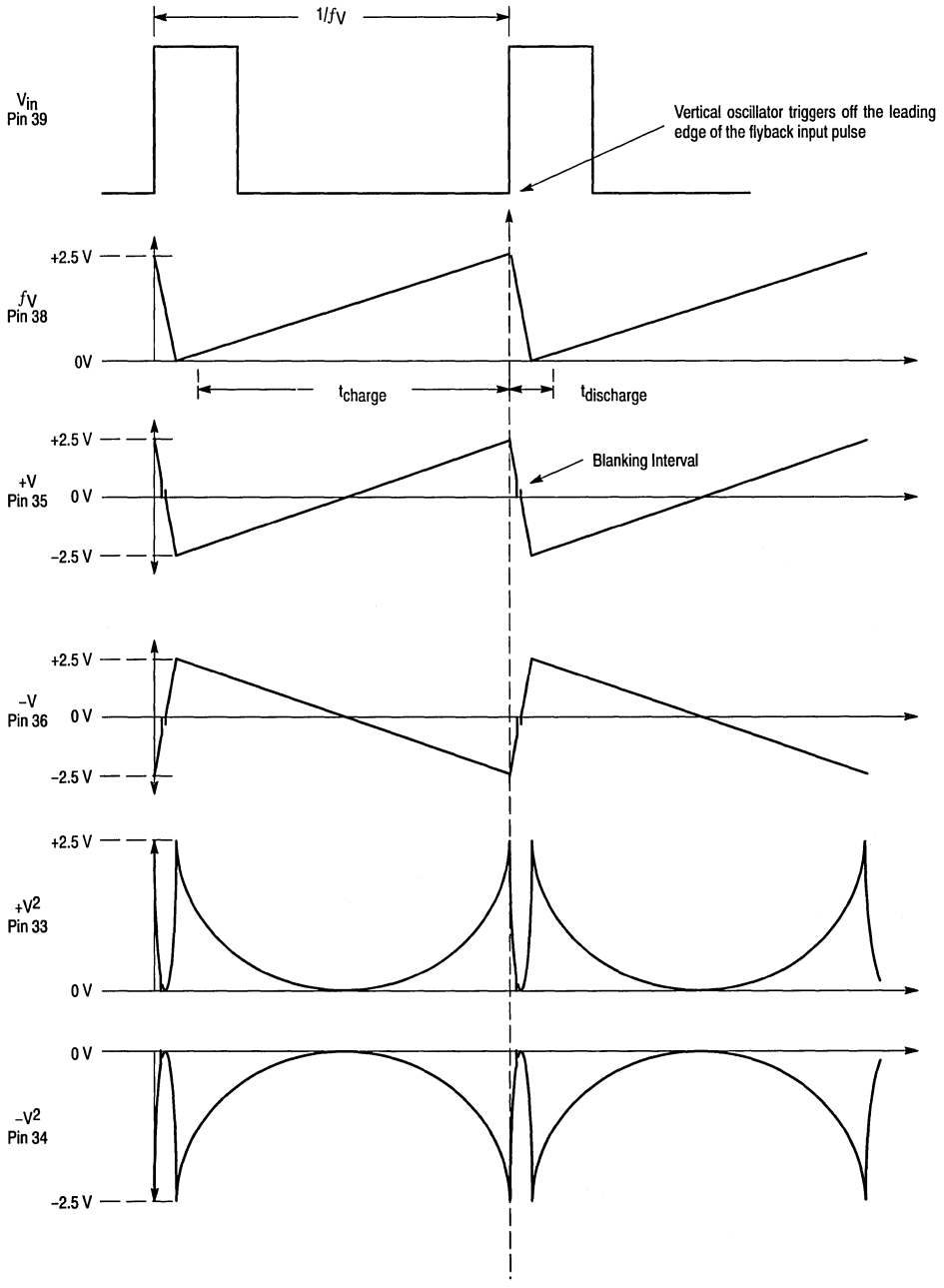


Figure 11 shows the timing of all the vertically influenced waveforms of the application circuit. Figures 12 and 13 show only the horizontal waveforms. The difference between the two is that Figure 13 shows the effect of advancing the horizontal waveforms.

Figure 11. Vertical Timing (continued)

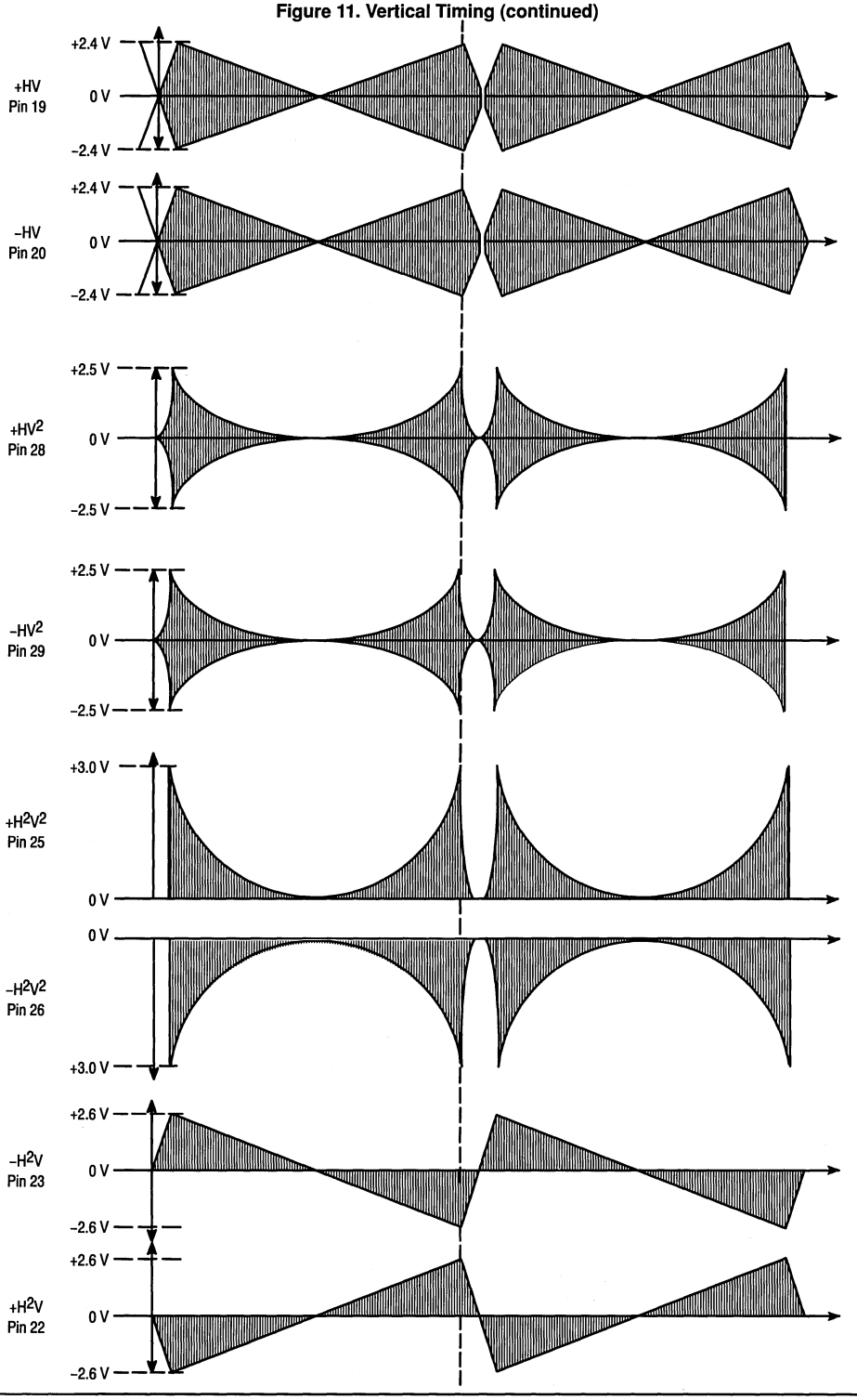


Figure 12. Horizontal Timing (No Phase Advance)

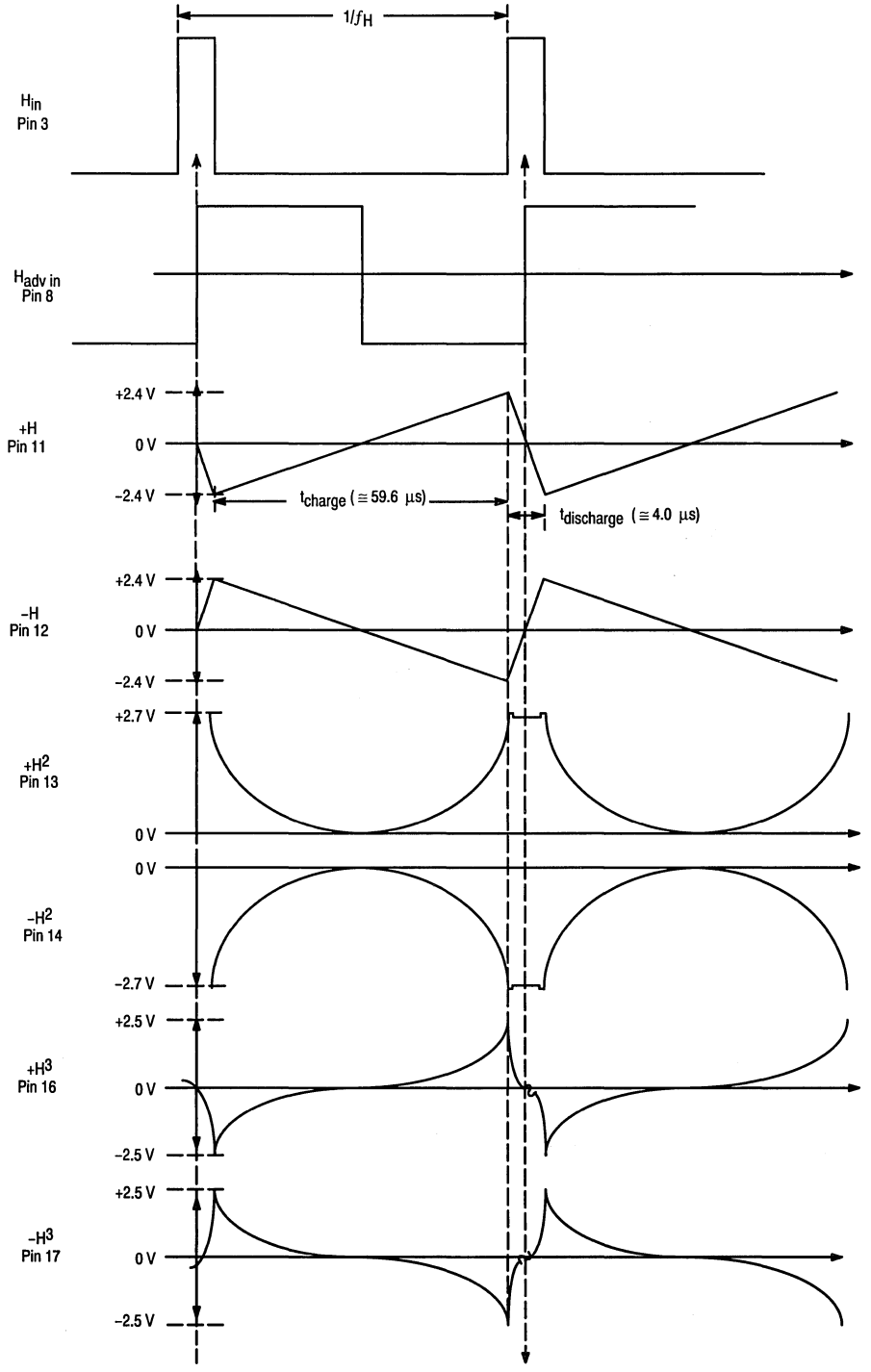
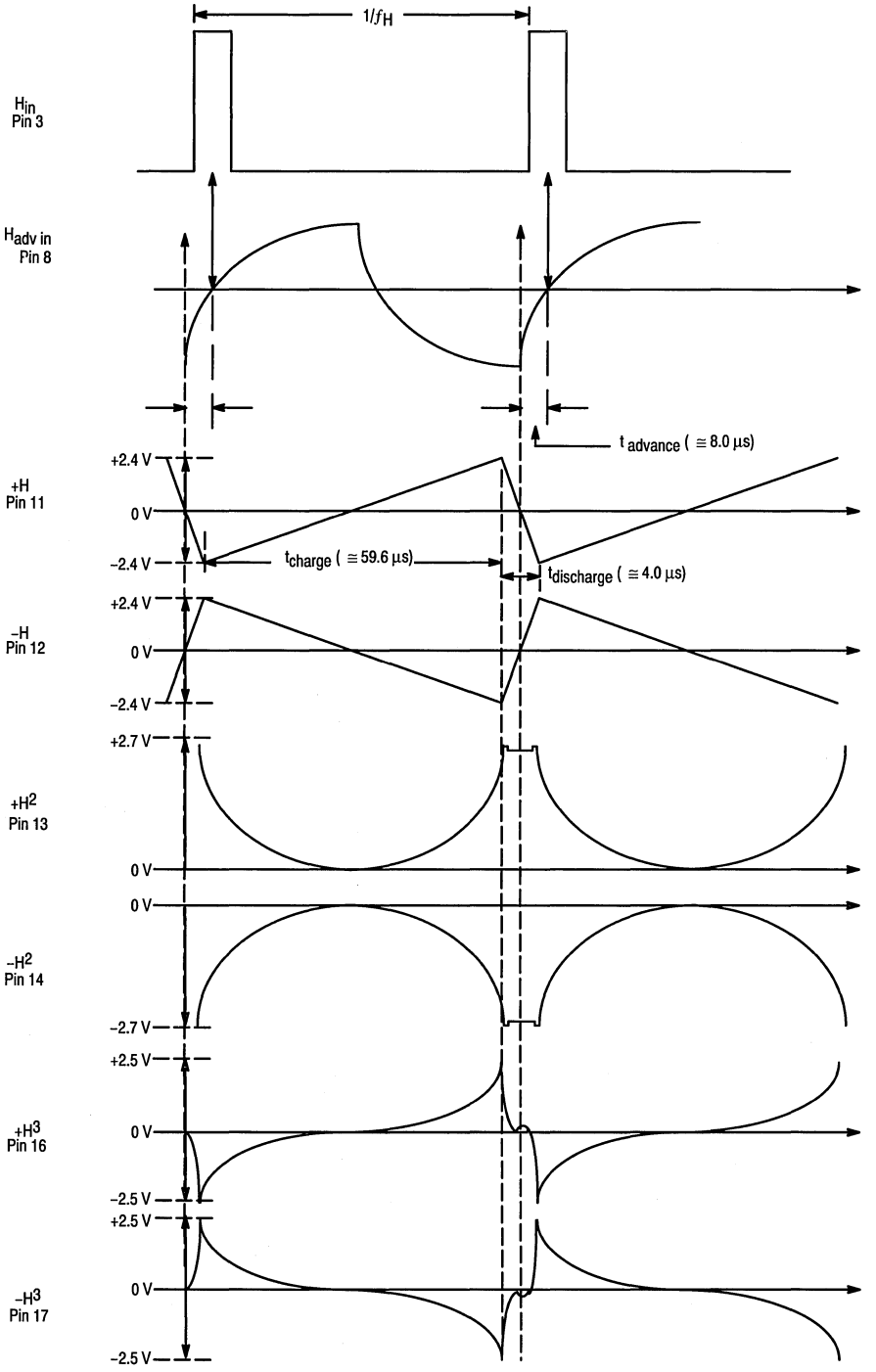


Figure 13. Horizontal Timing With Phase Advance
(Refer to Figure 10)



MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC44802A

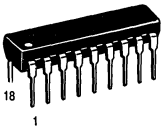
PLL Tuning Circuit with 1.3 GHz Prescaler

PLL TUNING CIRCUIT WITH 1.3 GHz PRESCALER

The MC44802A is a tuning circuit for TV applications. It contains, on one chip, all the functions required for PLL control of a VCO. This integrated circuit also contains a high frequency prescaler (which can be bypassed by software control) and thus can handle frequencies up to 1.3 GHz.

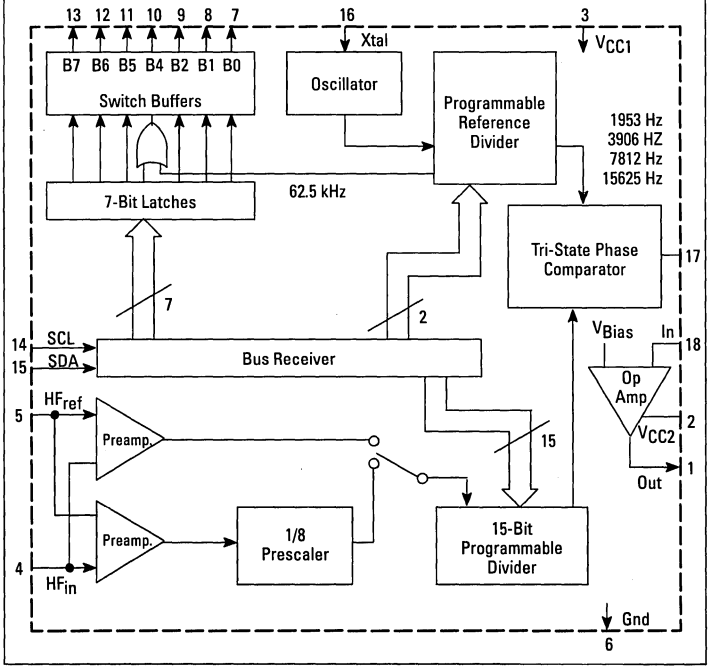
The MC44802A is manufactured on a single silicon chip using Motorola's high density bipolar, MOSAIC™ (Motorola Oxide Self Aligned Implanted Circuits) process.

- Complete Single-Chip System for MPU Control (I^2C Bus)
- Selectable Divide-by-8 Prescaler accepts Frequencies up to 1.3 GHz
- 15-Bit Programmable Divider accepts Input Frequencies up to 165 MHz
- Programmable Reference Divider
- Tri-State Phase/Frequency Comparator
- Op Amp for Direct Tuning Voltage Output (33 V)
- Seven High Current Output Buffers (10 mA, 12 V)
- Output Options for 62.5 kHz, Reference Frequency and the Programmable Divider
- Software Compatible with MC44810

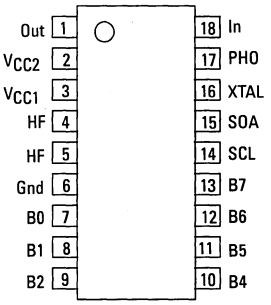


P SUFFIX
PLASTIC PACKAGE
CASE 707

SIMPLIFIED BLOCK DIAGRAM



PIN CONNECTIONS



ORDERING INFORMATION

Device	Temperature Range	Package
MC44802AP	0° to +70°C	Plastic DIP

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MAXIMUM RATINGS (T_A = 25°C unless otherwise specified)

Ratings	Pin	Value	Unit
Power Supply Voltage V_{CC1}	3	6.0	V
Band Buffer "OFF" Voltage	7 to 13	15	V
Band Buffer "ON" Current	7 to 13	15	mA
Op Amp Power Supply Voltage V_{CC2}	2	36	V
Op Amp Short Circuit Duration (0 to V_{CC2})	1	Continuous	V
Storage Temperature		−65 to +150	°C
Operating Temperature Range		0 to +70	°C

ELECTRICAL CHARACTERICISTICS (V_{CC1} = 5.0 V, V_{CC2} = 32 V, T_A = 25°C, unless otherwise specified)

Characteristics	Pin	Min	Typ	Max	Unit
V_{CC1} Supply Voltage Range	3	4.5	5.0	5.5	V
V_{CC1} Supply Current (V_{CC1} = 5.0 V) (Note 1)	3	—	45	65	mA
V_{CC2} Supply Voltage Range	2	25	30	35	V
V_{CC2} Supply Voltage Curent (Output Open)	2	—	0.8	2.0	mA
Band Buffer Leakage Current when "OFF" at 12 V	7 to 13	—	0.01	1.0	µA
Band Buffer Saturation Voltage when "ON" at 10 mA	7 to 13	—	0.6	1.0	V
Data/Clock Current at 0 V	14, 15	−10	—	0	µA
Clock Current at 5.0 V	14	0	—	1.0	µA
Data Current at 5.0 V Acknowledge "OFF"	15	0	—	1.0	µA
Data Saturation Voltage at 15 mA Acknowledge "ON"	15	—	—	1.0	V
Data/Clock Input Voltage Low	14, 15	—	—	1.5	V
Data/Clock Input Voltage High	14, 15	3.0	—	—	V
Clock Frequency Range	14	0	—	100	kHz
Oscillator Frequency Range	—	3.5	4.0	4.1	MHz
Phase Detector Tri-State Current	17	−15	0	15	nA
Phase Detector High-State Source Current (@ 1.5 V)	17	−2.0	—	−0.5	mA
Phase Detector Low-State Sink Current (@ 3.5 V)	17	0.2	—	1.7	mA
Op Amp Internal Reference Voltage	—	2.1	2.75	3.0	V
Op Amp Input Current	18	−15	0	15	nA
DC Open Loop Gain	—	2000	5000	—	
Gain Bandwidth Product (R_L = 10 k, C_L = 20 pF)	—	0.3	—	—	MHz
Phase Margin (R_L = 10 k, C_L = 20 pF)	—	50	—	—	Deg.
V_{out} Low, Sinking 50 µA	1	—	0.1	0.3	V
V_{out} High, Sourcing 50 µA, V_{out} − V_{CC2}	1	−4.0	−3.0	—	V
V_{CC1} Supply Ripple Rejection (See Figure 1a)	—	—	−54	−45	dB

HF CHARACTERISTICS (See Figure 1b)

HF In/Ref DC Bias	4, 5	—	1.6	—	V
HF Voltage Range Prescaler "OFF" 10 to150 MHz	5	20	—	315	mVrms
HF Voltage Range Prescaler "ON" 50 to 900 MHz	5	20	—	315	mVrms
HF Voltage Range Prescaler "ON" 900 to 1300 MHz	5	50	—	315	mVrms

NOTES:
1. When prescaler "OFF", typical supply current is decreased by 20 mA.

FIGURE 1a — RIPPLE REJECTION — MEASUREMENT SCHEMATIC

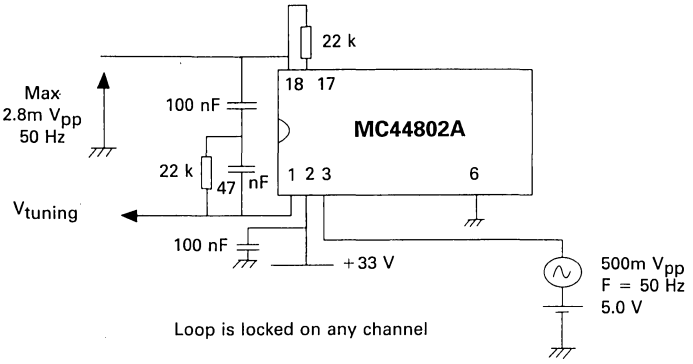
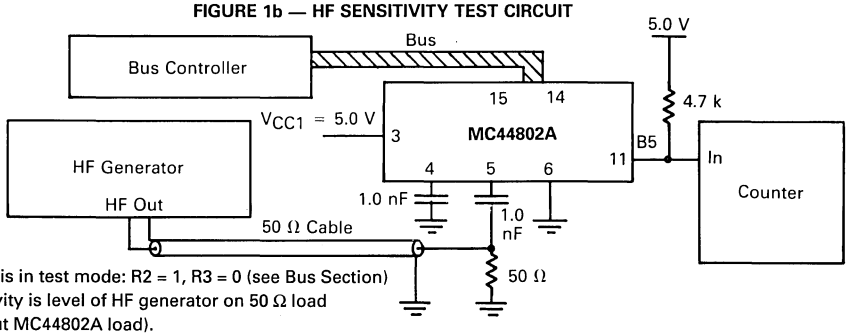
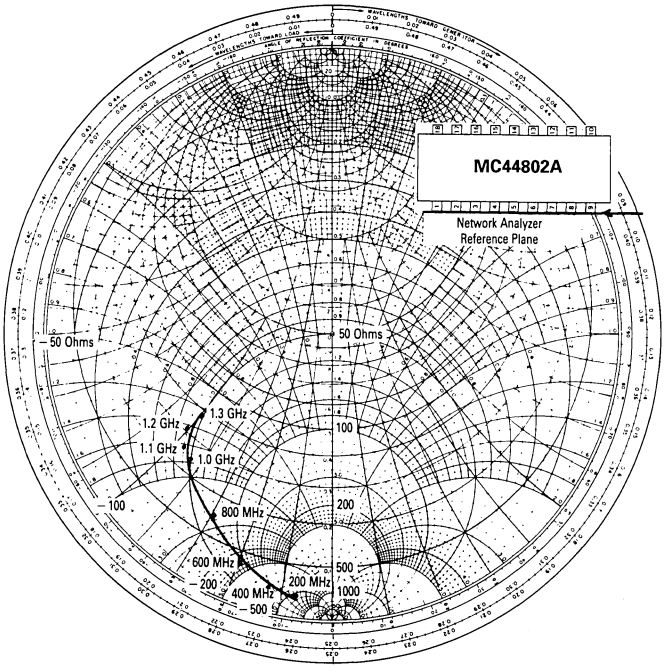


FIGURE 1b — HF SENSITIVITY TEST CIRCUIT



Device is in test mode: R2 = 1, R3 = 0 (see Bus Section)
sensitivity is level of HF generator on 50 Ω load
(without MC44802A load).

FIGURE 2 — PIN 5 INPUT IMPEDANCE (TYP)



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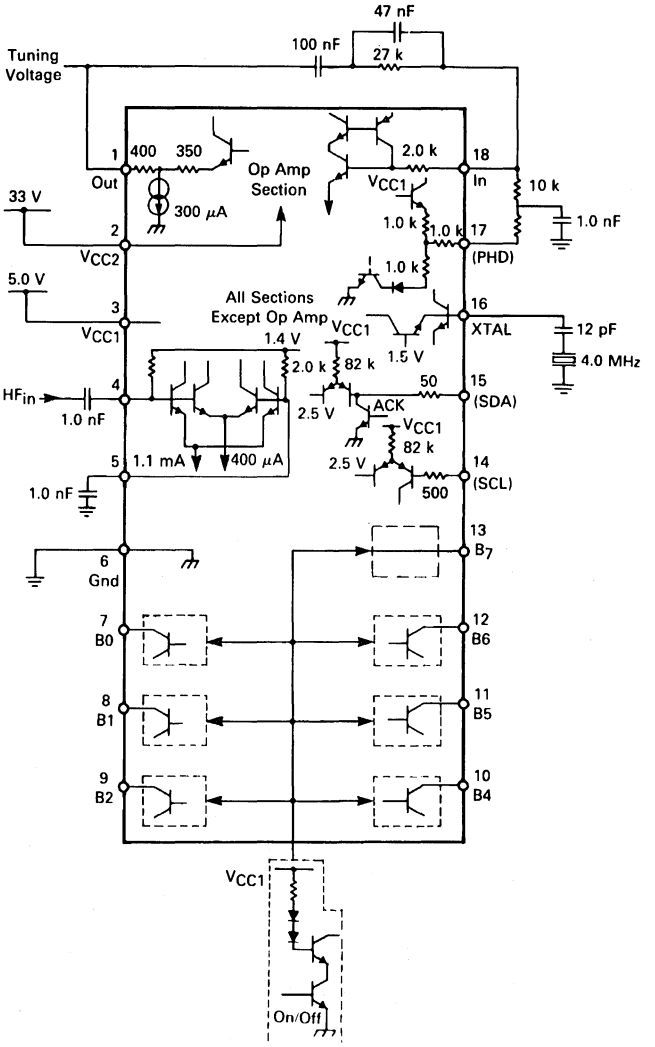
PIN FUNCTION DESCRIPTION (See Figure 3a)

Pin	Function	Description
1	Out	Operational amplifier output which provides the tuning voltage
2	V_{CC2}	Operational amplifier positive supply
3	V_{CC1}	Positive supply of the circuit (except op amp)
4	HF_{in}	HF inputs from local oscillator
5	HF_{ref}	
6	Gnd	Ground
7, 8, 9, 10, 11, 12, 13	B0, B1,.....B7	Band buffer output can drive up to 10 mA
14	SCL	Clock Input (supplied by the microprocessor via I^2C Bus)
15	SDA	Data Input (I^2C Bus)
16	XTAL	Crystal Input (Typ: 4.0 MHz)
17	PHD	Phase Comparator Output
18	In	Negative Operational Amplifier Input

FIGURE 3 — PIN CIRCUIT SCHEMATIC



FUNCTIONAL DESCRIPTION

A representative block diagram and a typical system application are shown in Figures 4 and 5. A discussion of the features and function of each of the internal blocks is given below.

FIGURE 4 — BLOCK DIAGRAM

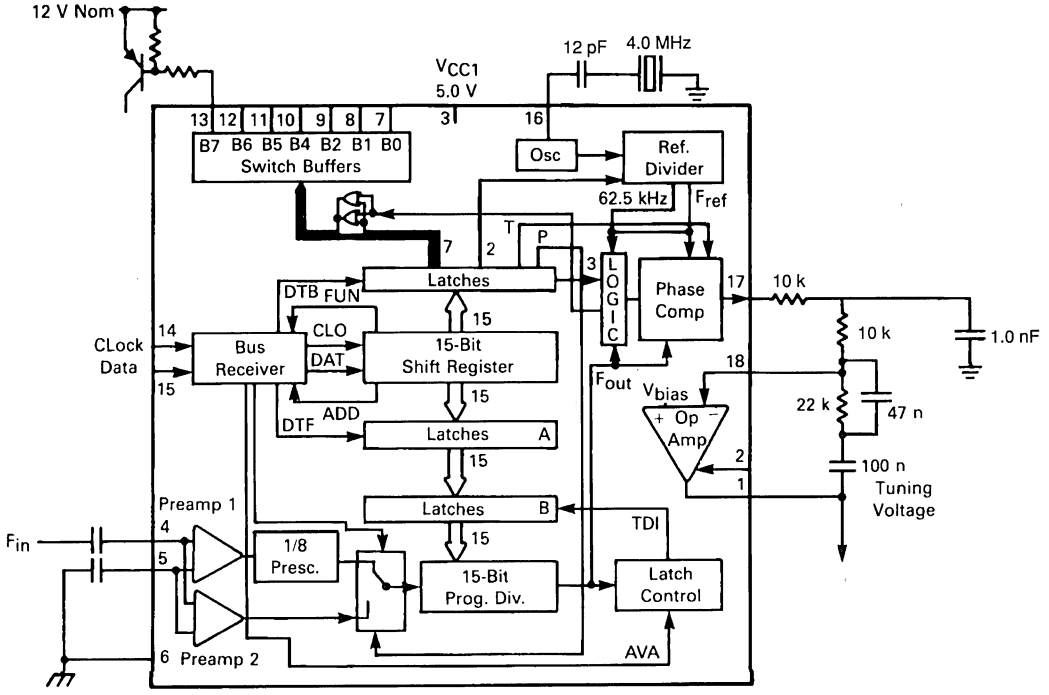
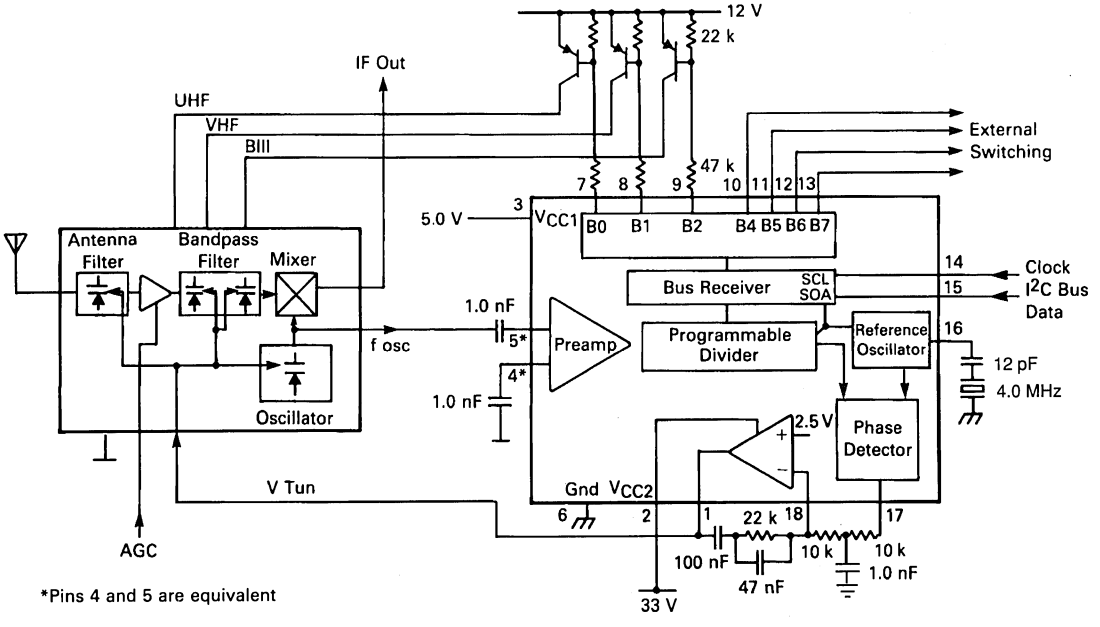


FIGURE 5 — TYPICAL TUNER APPLICATION



DATA FORMAT AND BUS RECEIVER

The circuit receives the information for tuning and control via the I²C Bus. The incoming information, consisting of a chip address byte followed by two or four data bytes, is treated in the I²C Bus receiver. The definition of the permissible bus protocol is shown below:

1_STA	CA	CO	BA	STO		
2_STA	CA	FM	FL	STO		
3_STA	CA	CO	BA	FM	FL	STO
4_STA	CA	FM	FL	CO	BA	STO

STA = Start Condition
STO = Stop Condition
CA = Chip Address Byte
CO = Data Byte for Control Information
FM = Data Byte for Frequency Information (MSBs)
FL = Data Byte for Frequency Information (LSBs)
BA = Band Information

Frequency information is preceeded by a Logic "0." If the function bit is Logic "1" the two following bytes contain control and band information where the bits have the following functions:

— Bit R0 and R1
Define the reference divider division ratio. Four ratios are available (see Table 1).

— Bit R2 and R3
Are used to switch internal signals to the buffer outputs. Pin 10 and 11 (see Table 2).

— Bit R2, R6 and T
Are used to control the phase comparator output stage (see Table 3).

— Bit P
Switches the prescaler in and out. At Logic "1" the prescaler is bypassed and the power supply of the prescaler is switched off.

COMPLETE DATA TRANSFER PROCESS

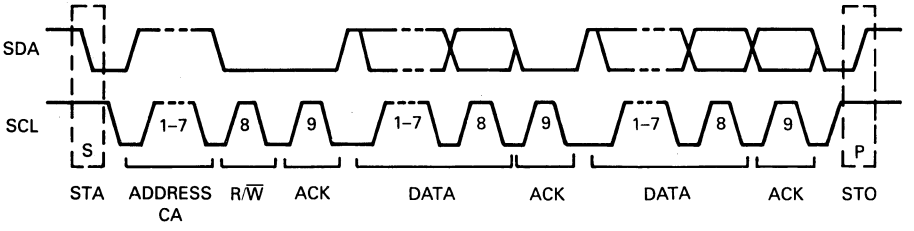


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Figure 6 shows the five bytes of information that are needed for circuit operation: there is the chip address, two bytes of control and band information and two bytes of frequency information.

After the chip address, two or four data bytes may be received: if three data bytes are received the third data byte is ignored.

If five or more data bytes are received the fifth and following data bytes are ingored and the last acknowledge pulse is sent at the end of the fourth data byte.

The first and the third data bytes contain a function bit which allow the IC to distinguish between frequency information and control plus band information.

FIGURE 6 — DEFINITION OF BYTES

CA_Chip Address	1	1	0	0	0	0	1	0	ACK
CO_Information	(1)	R6	T	P	R3	R2	R1	R0	ACK
BA_Band Info.	B7	B6	B5	B4	X	B2	B1	B0	ACK
FM_Frequency Info.	(0)	N14	N13	N12	N11	N10	N9	N8	ACK
FL_Frequency Info.	N7	N6	N5	N4	N3	N2	N1	B0	ACK

TABLE 1

Input Data		Reference Divider
R1	R0	Division Ratio
0	0	2048
0	1	1024
1	0	512
1	1	256

TABLE 2

Input Data		Test Outputs on Buffers	
R2	R3	Pin 10	Pin 11
0	0	—	—
0	1	62.5 kHz	—
1	0	F_{ref}	FBY2
1	1	—	—

Bit B4 has to be "zero" when Pin 10 is used to output 62.5 kHz.

Bit 4 and B5 have to "zero" to output F_{ref} and FBY2.

FBY2 is the programmable divider output frequency divided by two.

TABLE 3

Input Data R2	Input Data R6	Input Data T	Output State of the Phase Comparator
0	0	0	Normal Operation
0	0	1	Off (High Impedance)
0	1	0	High
0	1	1	Low
1	0	0	Normal Operation
1	0	1	Off
1	1	0	Normal Operation
1	1	1	Off

THE BAND BUFFERS

BA_Band Information

20 Pin Version

B7	B6	B5	B4	B3	B2	B1	B0	ACK

18 Pin Version

B7	B6	B5	B4	X	B2	B1	B0	ACK

The band buffers are open collector transistors and are active "low" at Bn = 1. They are designed for 10 mA with a typical on-resistance of 70 ohms. These buffers are designed to withstand relative high output voltage in the off-state.

B4 and B5 buffers (Pins 10 and 11) may also be used to output internal IC signals (reference frequency and programmable divider output frequency divided by 2) for tests purposes.

Buffer B4 may also be used to output a 62.5 kHz frequency for an intermediate stage of the reference divider. The bit B4 and/or B5 have to be zero if the buffers are used for these additional functions.

THE PROGRAMMABLE DIVIDER

The programmable divider is a presettable down counter. When it has counted to zero it takes its required division ratio out of the latches B. Latches B are loaded from latches A by means of signal TDI which is synchronous to the programmable divider output signal.

Since latches A receive the data asynchronously with the programmable divider, this double latch scheme is needed to assure correct data transfer to the counter.

The division ratio definition is given by:

$N = 16384 \times N14 + 8132 \times N13 + ... + 4 \times N2 + 2 \times N1 + N0$

Max Ratio 32767
Min Ratio 17

Where N0.....N14 are the different bits for frequency information.

The counter may be used for any ratio between 17 and 32767 and reloads correctly as long as its output frequency does not exceed 1.0 MHz.

The data transfer between latches A and B (signal TDI) is also initiated by any start condition on the IIC bus.

At power-on the whole bus receiver is reset and the programmable divider is set to a counting ratio of N = 256 or higher.

THE PRESCALER

The prescaler has a preamplifier which guarantees high input sensitivity. The prescaler may be bypassed (Bit P) and the signal then passes through preamp 2.

THE PHASE COMPARATOR

The phase comparator is phase and frequency sensitive and has very low output leakage current in the high impedance state.

THE OPERATIONAL AMPLIFIER

The operational amplifier is designed for very low noise, low input bias current and high power supply rejection. The positive input is biased internally. The op amp needs 31 V supply (V_{CC2}) as minimum voltage for a guaranteed maximum tuning voltage of 28 V.

Figure 1 shows a possible filter arrangement. The component values depend very much on the application (tuner characteristic, reference frequency, etc.);

As a starting point for optimization, the components values in Figure 1 may be used for 7.8125 kHz reference frequency in a multiband TV tuner.

THE OSCILLATOR

The oscillator uses a 4.0 MHz crystal tied to ground or V_{CC1} through a capacitor, used in the series resonance mode. The frequency range of the oscillator is 3.5 to 4.1 MHz.

The voltage at Pin 16 (crystal) has low amplitude and low harmonic distortion.

SYSTEM APPLICATION

Table 4 is a summary of the circuit applications using a 4.0 MHz crystal.

TABLE 4

Input Data R1	Input Data R0	Reference Divider Div. Ratio	Reference Frequency Hz (1)	With Internal Prescaler P = 0: Frequency Steps kHz	With Internal Prescaler P = 0: Max. Input Frequency MHz	Without Internal Prescaler P = 1: Frequency Steps kHz	Without Internal Prescaler P = 1: Max. Input Frequency MHz
0	0	2048	1953.125	15.625	512	1.953125	64
0	1	1024	3906.25	31.25	1024	3.90625	128
1	0	512	7812.5	62.5	1300(2)	7.8125	165(3)
1	1	256	15625.0	125	1300(2)	15.625	165(3)

(1) With 4.0 MHz Crystal (2) Limit of Prescaler (3) Limit of Programmable Divider

MC44807/17

**SYSTEM 4
PLL TUNING CIRCUIT
with 1.3 GHz PRESCALER
and 3-WIRE BUS**

Product Preview

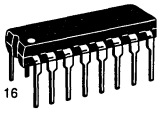
PLL Tuning Circuit with 3-Wire Bus

The MC44807/17 is a tuning circuit for TV and VCR tuner applications. It contains, on one chip, all the functions required for PLL control of a VCO. This integrated circuit also contains a high frequency prescaler and thus can handle frequencies up to 1.3 GHz.

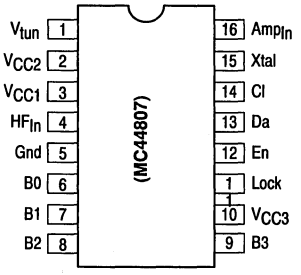
The MC44807/17 is manufactured on a single silicon chip using Motorola's high density bipolar process, MOSAIC® (Motorola Oxide Self Aligned Implanted Circuits).

- Complete Single Chip System for MPU Control (3-Wire Bus) Data and Clock Inputs are I²C Bus Compatible
- ÷ 8 Prescaler Accepts Frequencies up to 1.3 GHz
- 15 Bit Programmable Divider Accepts Input Frequencies Up to 165 MHz
- Reference Divider: Programmable for Division Ratios 512 and 1024
- Tri-State Phase/Frequency Comparator with Lock Detect Output
- Op Amp for Direct Tuning Voltage Output (30 V)
- Four Integrated PNP B and Buffers for 40 mA (V_{CC1} to 14.4 V)
- Output Options for the Reference Frequency and the Programmable Divider
- Bus Protocol for 18 or 19 Bit Transmission
- Extra Protocol for 34 Bit for Test and Further Features
- High Sensitivity
- Fully ESD Protected

P SUFFIX
PLASTIC PACKAGE
CASE 648



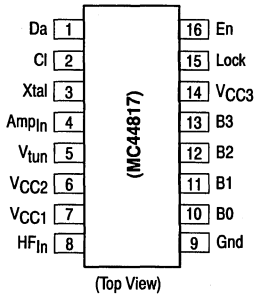
PIN CONNECTIONS



(Top View)

D SUFFIX
PLASTIC PACKAGE
CASE 751B
(SO-16)

PIN CONNECTIONS



(Top View)

MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted.)

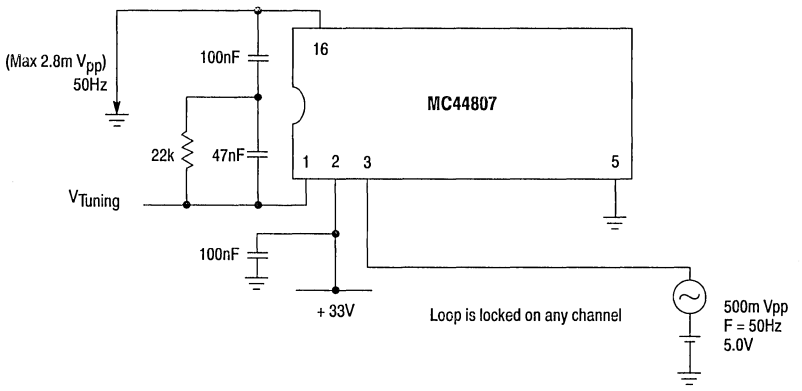
Rating	Pin(807)/(817)		Value	Unit
Power Supply Voltage (V_{CC1})	3	7	6.0	V
Band Buffer OFF Voltage	6 – 9	10 – 13	15	V
Band Buffer ON Current	6 – 9	10 – 13	50	mA
Band Buffer – Short Circuit Duration (0 to V_{CC3}) (Note 2)	6 – 9	10 – 13	Continuous	sec
Op Amp Power Supply Voltage (V_{CC2})	2	6	40	V
Op Amp Short Circuit Duration (0 to V_{CC2})	1	5	Continuous	sec
Power Supply Voltage (V_{CC3})	10	14	14.4	V
Storage Temperature	10	14	– 65 to +150	°C
Operating Temperature Range			– 20 to + 80	°C
Band Buffer Operation (Note 1) @ 50 mA each buffer. All buffers ON simultaneously	6 – 9	10 – 13	10	sec
Op Amp Output Voltage	1	5	V_{CC2}	V

NOTES: 1. At V_{CC3} = V_{CC1} to 14.4 V, and T_A = – 20° to + 80°C.
2. At V_{CC3} = V_{CC1} to 14.4 V, and T_A = – 20° to + 80°C, one buffer ON only.

ORDERING INFORMATION

Device	Temperature Range	Package
MC44807P	– 20° to + 80°C	Plastic DIP
MC44817D		SO-16

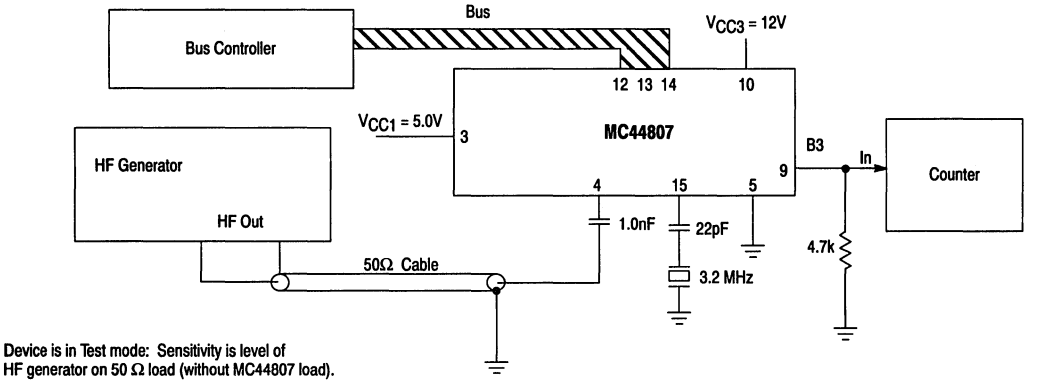
Figure 1. Ripple Rejection – Measurement Schematic (MC44807P)



PIN FUNCTION DESCRIPTION

Pin	Function	Description
MC44807P (see Block Diagram)		
1	Out	Operational amplifier output which provides the tuning voltage
2	V_{CC2}	Operational amplifier positive supply (33 V)
3	V_{CC1}	Positive supply of the circuit (5.0 V)
4	HF_{In}	HF inputs from local oscillator
5	Gnd	Ground
6, 7, 8, 9	B0, B1...B3	Band buffer outputs can drive up to 30 mA (40 mA at 0° to 80° C)
10	V_{CC3}	Positive supply for integrated band buffers (12 V)
11	LOCK	Lock detector output
12	En	Enable input (3-wire Bus)
13	DA	Data input (3-wire Bus)
14	CL	Clock input (supplied by the microprocessor via 3-wire Bus)
15	Xtal	Crystal input (typ: 3.2 MHz)
16	In	Negative operational amplifier input and charge pump
MC44817D		
1	DA	Data input (3-wire Bus)
2	CL	Clock input (supplied by the microprocessor via 3-wire Bus)
3	Xtal	Crystal oscillator (3.2 MHz)
4	In	Negative operational amplifier input and charge pump
5	Out	Operational amplifier output which provides the tuning voltage
6	V_{CC2}	Operational amplifier positive supply (33 V)
7	V_{CC1}	Positive supply of the circuit (5.0 V)
8	HF_{In}	HF input from local oscillator
9	Gnd	Ground
10, 11, 12, 13	B0, B1...B3	Band buffer outputs can drive up to 30 mA (40 mA at 0° to 80°C)
14	V_{CC3}	Positive supply for integrated band buffers (12 V)
15	LOCK	Lock detector output
16	En	Enable input (3-wire Bus)

Figure 2. HF Sensitivity Test Circuit



Device is in Test mode: Sensitivity is level of HF generator on 50 Ω load (without MC44807 load).

Figure 3. Block Diagram MC44807P

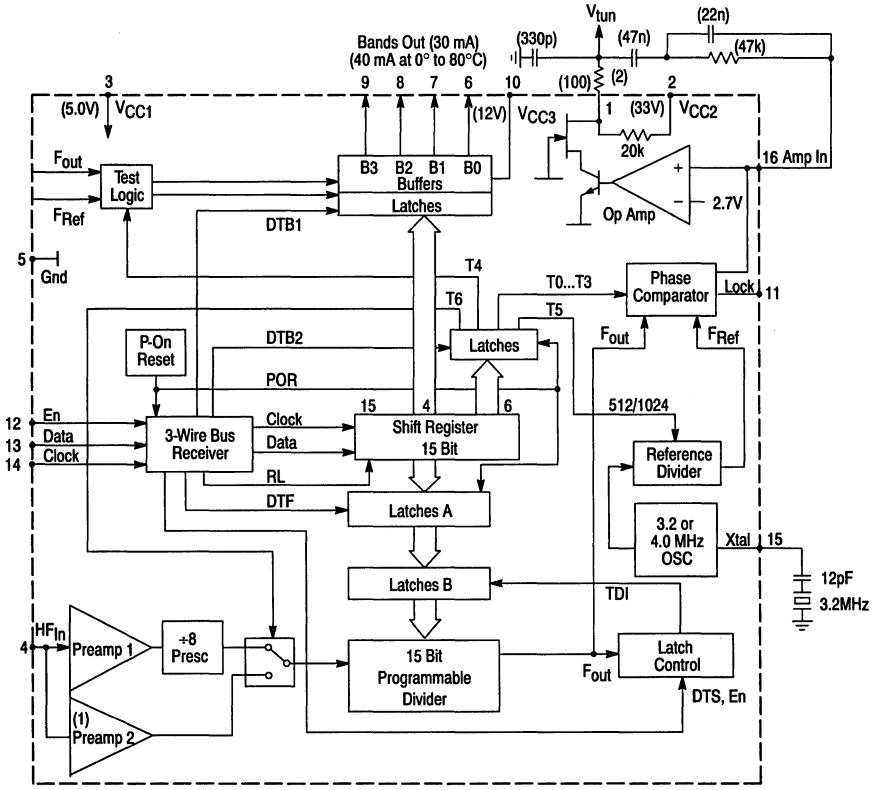
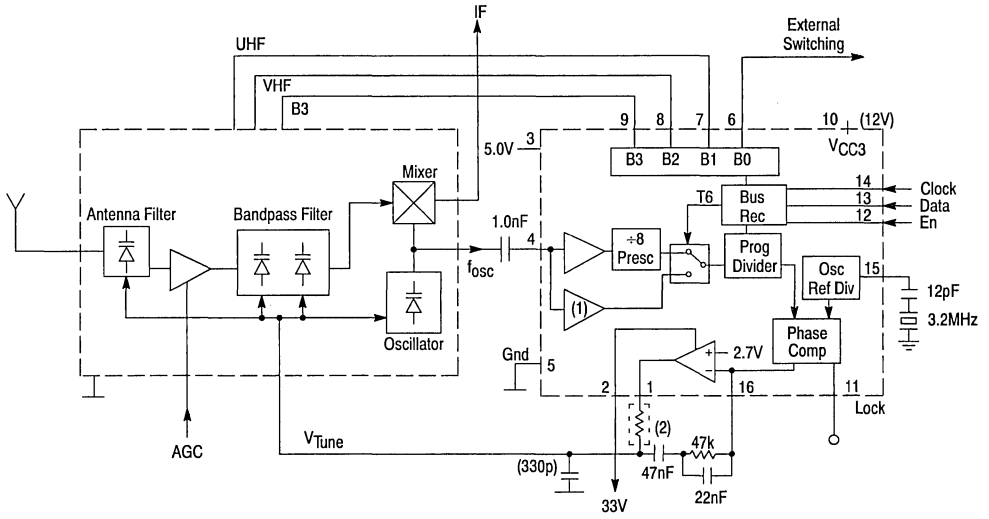


Figure 4. Typical Tuner Application



NOTE: 1. This feature needs to be characterized on the final silicon. In the case that it degrades the HF-sensitivity, it will be eliminated.
2. The 100 Ω resistor is not required any more, but does not disturb the performance.

FUNCTIONAL DESCRIPTION

A representative block diagram and a typical system application are shown in Figures 4 and 5. A brief discussion of the features and function of each of the internal blocks follows.

Data Format and Bus Receiver

The circuit is controlled by a 3-wire bus with Data (DA), Clock (CL), and Enable (En) inputs. The Data and Clock inputs may also be shared with an I²C Bus (data changes when clock is low) while the Enable is a separate signal. The circuit is compatible with 18 and 19-bit data transmission and also has a mode for 34-bit transmission for test and additional features.

The 3-wire bus receiver receives data for the internal shift register after the positive-going edge of the En signal. The data is transmitted to the band buffers on the negative-going edge of clock pulse 4 (signal DTB1).

18 and 19-Bit Data Transmission

The programmable divider may receive 14-bit (18-bit transmission) or 15-bit (19-bit transmission). The data is transmitted to the programmable divider (Latches A) on the negative-going edge of clock pulse 19 or on the negative edge of the En signal if En goes down after the 18th clock pulse (signal DTF). If the programmable divider receives 14-bit, its MSB (Bit N14) is internally reset. The reset pulse is generated only if En goes negative after the 18th clock pulse (signal RL).

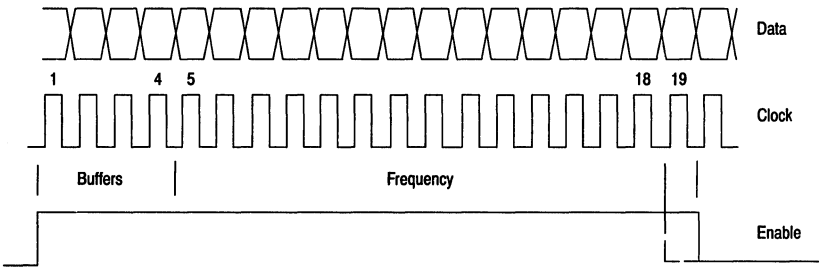
34-Bit Data Transmission

(For Test and Additional Features) In the test mode, the programmable divider receives 15-bit and the data is transferred to Latches A on the negative edge of clock pulse 19 (signal DTF). The information for test is received on clock pulses 20 to 26 and transmitted to the latches on the negative edge of pulse 34 (signal DTB2). These latches have a power-on reset. The power-on reset sets the programmable divider to a counting ratio of 256 or higher and resets the corresponding latches to test bits T0 to T6 (signal POR). The bus receiver is not disturbed if the data format is wrong. Useless bits are ignored. If, for example, the Enable signal goes low after clock pulse 9, bits 1 to 4 are accepted as valid buffer information and the other bits are ignored. If more than 34 bits are received, bit 35 and the following are ignored.

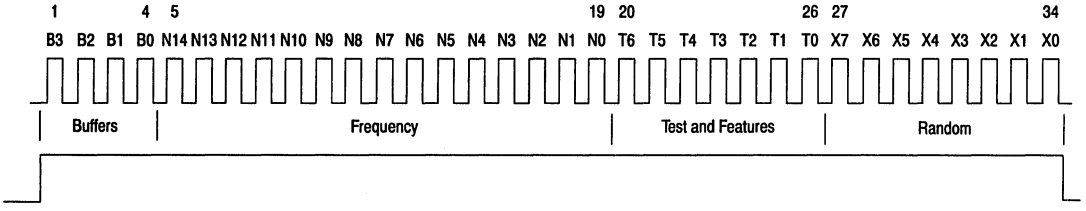
The Lock Detector output is low in lock. The output goes immediately high when an unlock condition is detected. The output goes low again when the loop is in lock during a complete period of the reference frequency.

BUS TIMING DIAGRAM

Standard Bus Protocol 18 or 19-Bit



Bus Protocol for Test and Features



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DEFINITION OF BUS PROTOCOLS

Bus Protocol for 18-Bit

B3	B2	B1	B0	N13	N12	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1	N0

Max counting ratio 16363
N14 is reset internally

Bus Protocol for 19-Bit

B3	B2	B1	B0	N14	N13	N12	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1	N0

Max counting ratio 32767:
B0, B1...B3 = Control of band buffers
N0, N1...N14 = Control of programmable divider

N14 = MSB; N0 = LSB
Min, counting ratio always 17.
B3 = First shifted bit
N0 = Last shifted bit

Bus Protocol for Test and Further Features (34-Bit)

B3	B2	B1	B0	N14...N0	T6	T5	T4	T3	T2	T1	T0	X7	X6...X1	X0

T0, T1...T3 = Control the phase comparator
T4 = Switches test signals to the buffer outputs
T5 = Division ratio of the reference divider
T6 = Bypasses the prescaler (see note Bit T6 table)
X0, X1...X7 = Are random

B3 = First shifted bit
X0 = Last shifted bit

DEFINITION OF THE BITS FOR TEST AND FEATURES

Bit T0 Defines the Charge Pump Current of the Phase Comparator

T0	Charge
0	Pump current 50 µA (Typical)
1	Pump current 15 µA (Typical)

Bits T1 and T2 Define the Digital Function of the Phase Comparator

T2	T1	State	Output Function of Phase Comparator
0	0	1	Normal Operation
0	1	2	High Impedance (Tri-State)
1	0	3	Upper Source On, Lower Source Off
1	1	4	Lower Source On, Upper Source Off

NOTE: State1 The phase comparator pulls high if the input frequency is too high and it pulls low when the input frequency is too low. (Inversion by op amp) The phase comparator generates a fixed duration offset pulse for each comparison pulse (similar to the MC44802A). This guarantees operation in the linear region. The offset pulse is a positive current pulse (upper source).

Bit T3 Defines the Offset Pulse of the Phase Comparator

T3	Offset Pulse
0	Offset pulse short (200 ns), normal mode
1	Offset pulse long (350 ns)

Bit T4 Switches the Internal Frequencies F_{ref} and FBY2 to the Buffer Outputs (B2, B3)

T4	Buffer Outputs
0	Normal operation
1	F_{Ref} switched to buffer output B2 FBY2 switched to buffer output B3

Bits B2 and B3 = have to be one in this case
F_{Ref} = reference frequency
FBY2 = output frequency of the Programmable Divider, ÷ 2

Bit T5 Defines the Division Ratio of the Reference Divider

T5	Bus Protocol
0	Division ratio 512
1	Division ratio 1024

The division ratio of the Reference Divider can only be programmed in the 34 bit bus protocol. In the standard bus protocol the division ratio is 512. (The power-up reset (POR) sets the division ratio to 512).

Bit T6 Switches the Prescaler

T6	Operation
0	Normal operation, 1.3 GHz Preamp 2 switched OFF
1	Low frequency operation, 165 MHz maximum. The prescaler is bypassed and its power supply is switched OFF. Input, 10 MHz min, 20 mVrms min.

NOTE: This feature needs to be characterized on the final silicon. In the case that it degrades the HF-sensitivity, it will be eliminated.

9

Figure 7. Equivalent Circuit of the Integrated Band Buffers

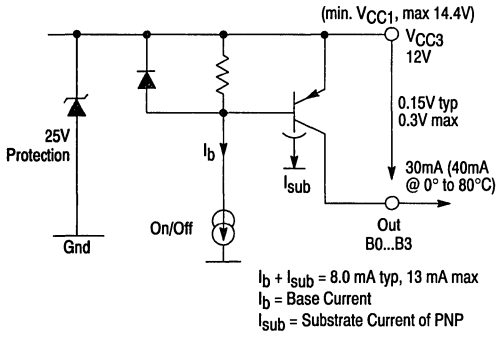
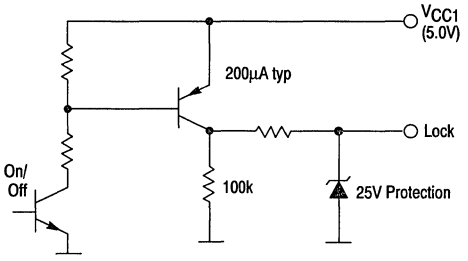


Figure 8. Equivalent Circuit of the Lock Output



Programmable Divider

The programmable divider is a presettable down counter. When it has counted to zero it takes its required division ratio out of the Latches B. Latches B are loaded from Latches A by means of signal TDI which is synchronous to the programmable divider output signal.

Since Latches A receive the data asynchronously with the programmable divider; this double latch scheme is needed to assure correct data transfer to the counter.

The division ratio definition is given by:

$$N = 16384 \times N14 + 8132 \times N13 + ... + 4 \times N2 + 2 \times N1 + N0$$

maximum ratio 32767 (16363 in case of 18-bit protocol), minimum ratio 17, where N0...N14 are the different bits for frequency information.

At power-on the whole bus receiver is reset and the programmable divider is set to a counting ratio of N = 256 or higher.

Prescaler

The prescaler has a preamplifier which guarantees high input sensitivity.

Phase Comparator

The phase comparator is phase and frequency sensitive and has very low output leakage current in the high impedance state.

Operational Amplifier

The operational amplifier is designed for very low noise, low input bias current and high power supply rejection. The positive input is biased internally. The op amp needs 28.5 V supply (V_{CC2}) as minimum voltage for a guaranteed maximum tuning voltage of 28 V.

Figure 4 shows a possible filter arrangement. The component values depend very much on the application (tuner characteristic, reference frequency, etc.).

Oscillator

The oscillator uses a 3.2 MHz to 4.0 MHz crystal tied to ground in series with a capacitor, used in the series resonance mode. The voltage at Pin 15 (or Pin 3 in SOIC package) "crystal", has low amplitude and low harmonic distortion.

MC44810

SYSTEM 4
PLL TUNING CIRCUIT with 1.3 GHz PRESCALER

Product Preview

PLL Tuning Circuit with 1.3 GHz Prescaler and D/A Section

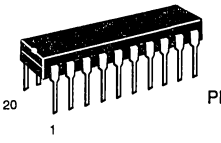
The MC44810 is a tuning circuit for TV applications. It contains a PLL section and a DAC section and is MPU controlled through the I²C Bus.

The PLL section contains all the functions required to control the VCO of a TV tuner. It generates the tuning voltage and the additional control signals (e.g. band switching voltages). The PLL section is functionally equivalent to MC44802.

The D-to-A section generates three further varactor voltages in order to feed all of the varactors of the tuner with their individually optimized control voltages (automatic tuner adjustment).

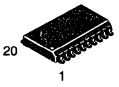
The MC44810 is manufactured on a single silicon chip using Motorola's high density bipolar MOSAIC® process (Motorola Oxide Self Aligned Implanted Circuits).

- Complete Single Chip System for MPU Control (I²C Bus)
- Selectable ÷ 8 Prescaler Accepts Frequencies Up to 1.3 GHz
- 15-Bit Programmable Divider Accepts Input Frequencies Up to 165 MHz
- Programmable Reference Divider
- Tri-State Phase/Frequency Comparator
- Op Amp for Direct Tuning Voltage Output (30 V)
- Seven Output Buffers: 10 mA, 12 V
- Output Options for 62.5 kHz, Reference Frequency and the Programmable Divider
- Software Compatible with MC44802A
- Three 6-Bit DACs for Automatic Tuner Adjustment Allowing Use of Non-Matched Varactors
- Better Tuner Performances Through Optimum Filter Response
- Two Chip Addresses for the PLL Section and Two Different Chip Addresses for the DAC Section

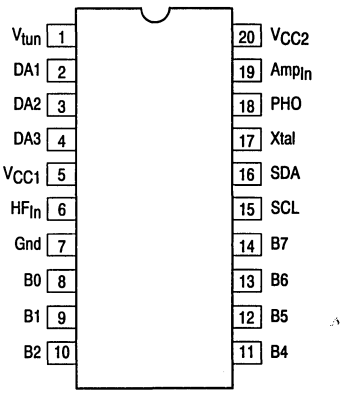


P SUFFIX
PLASTIC PACKAGE
CASE 738

DW SUFFIX
PLASTIC PACKAGE
CASE 751D
(SO-20L)



PIN CONNECTIONS



(Top View)

MAXIMUM RATINGS (T_A = 25°, unless otherwise noted.)

Ratings	Pin	Value	Unit
Power Supply Voltage (V_{CC1})	5	6.0	V
Band Buffer OFF Voltage	8 to 14	15	V
Band Buffer ON Current	8 to 14	15	mA
Op Amp Power Supply Voltage (V_{CC2})	20	36	V
Op Amp Short Circuit Duration (0 to V_{CC2})	1 to 4	Continuous	sec
Storage Temperature	—	– 65 to +150	°C
Operating Temperature Range	—	0 to + 70	°C

ORDERING INFORMATION

Device	Temperature Range	Package
MC44810P	0° to + 70°C	Plastic DIP
MC44810DW		SO-20L

Figure 1. Ripple Rejection - Measurement Schematic

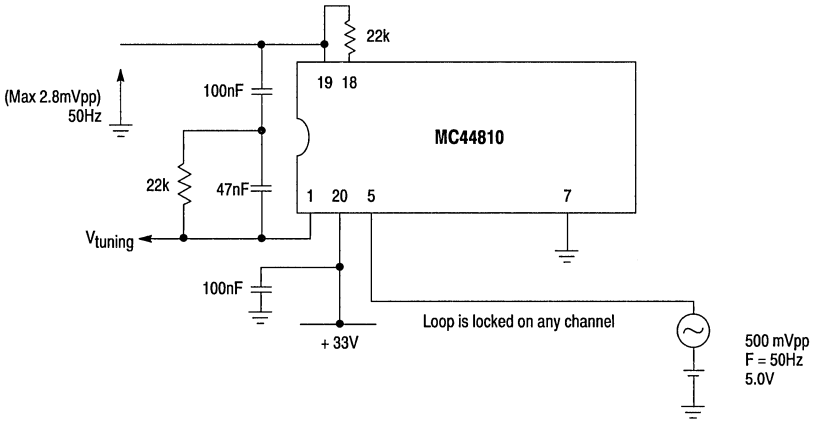
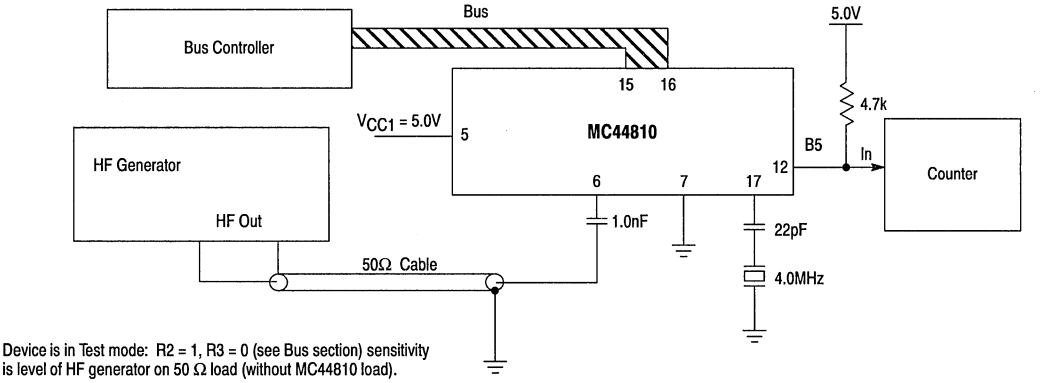


Figure 2. HF Sensitivity Test Circuit



Device is in Test mode: R2 = 1, R3 = 0 (see Bus section) sensitivity is level of HF generator on 50 Ω load (without MC44810 load).

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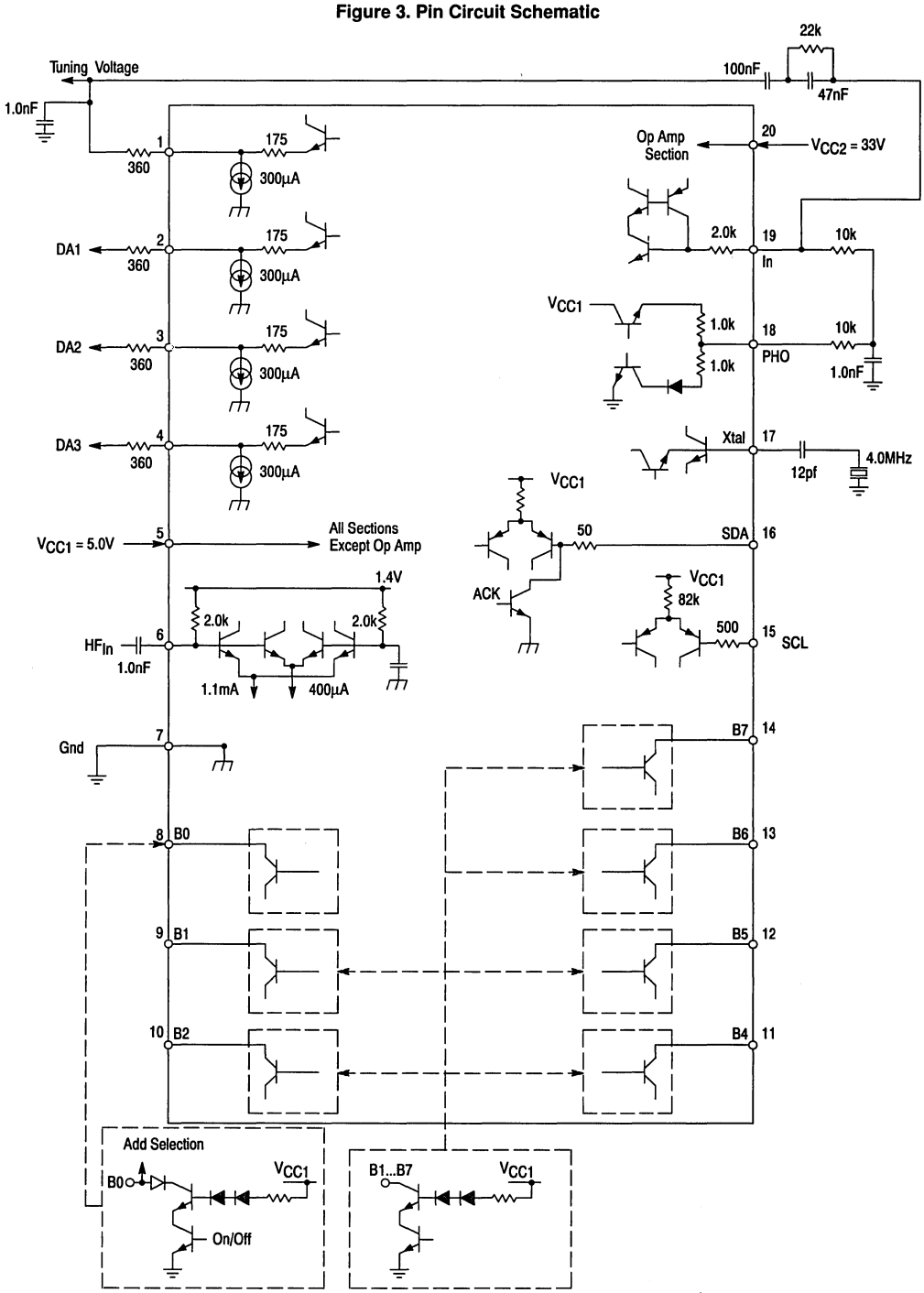
PIN FUNCTION DESCRIPTION

Pin	Function	Description
1	Out	Operational amplifier output which provides the tuning voltage
2, 3, 4	DA1, DA2, DA3	D/A output control voltages
5	V_{CC1}	Positive supply of the circuit (except op amp)
6	HF_{In}	HF inputs from local oscillator
7	Gnd	Ground
8, 9, 10, 11 12, 13, 14	B0...B2 B4...B7	Band buffer outputs can drive up to 10 mA
15	SCL	Clock input (supplied by the microprocessor via I^2C bus)
16	SDA	Data input (I^2C bus)
17	Xtal	Crystal oscillator (typ: 4.0 MHz)
18	PHO	Phase comparator output
19	In	Negative operational amplifier input
20	V_{CC2}	Operational amplifier positive supply

Figure 3. Pin Circuit Schematic



FUNCTIONAL DESCRIPTION

A representative block diagram and a typical system application are shown in Figures 4 and 5. A discussion of the features and function of each of the internal blocks is given below.

Automatic Tuner Alignment

The circuit generates the tuning voltage through the PLL in the same way as the MC44802A. The output voltage of the D/A converters are equal to the tuning voltage plus a positive or negative offset of up to 31 steps. During the automatic alignment the PLL first locks to the appropriate frequency and then searches for the optimum values of the other varactor voltages. The digital word for each voltage value is stored in a nonvolatile memory (NVM). Hence, for each frequency point to be adjusted, three times 6 bits of information have to be stored (plus 2 bits for the DAC range).

The information stored in the NVM reflects the characteristic of the individual tuner. For this reason the NVM is preferably situated inside the tuner and is also controlled by the I2C Bus. (The NVM is also needed to store the program-channel allocation).

Figure 4. Block Diagram

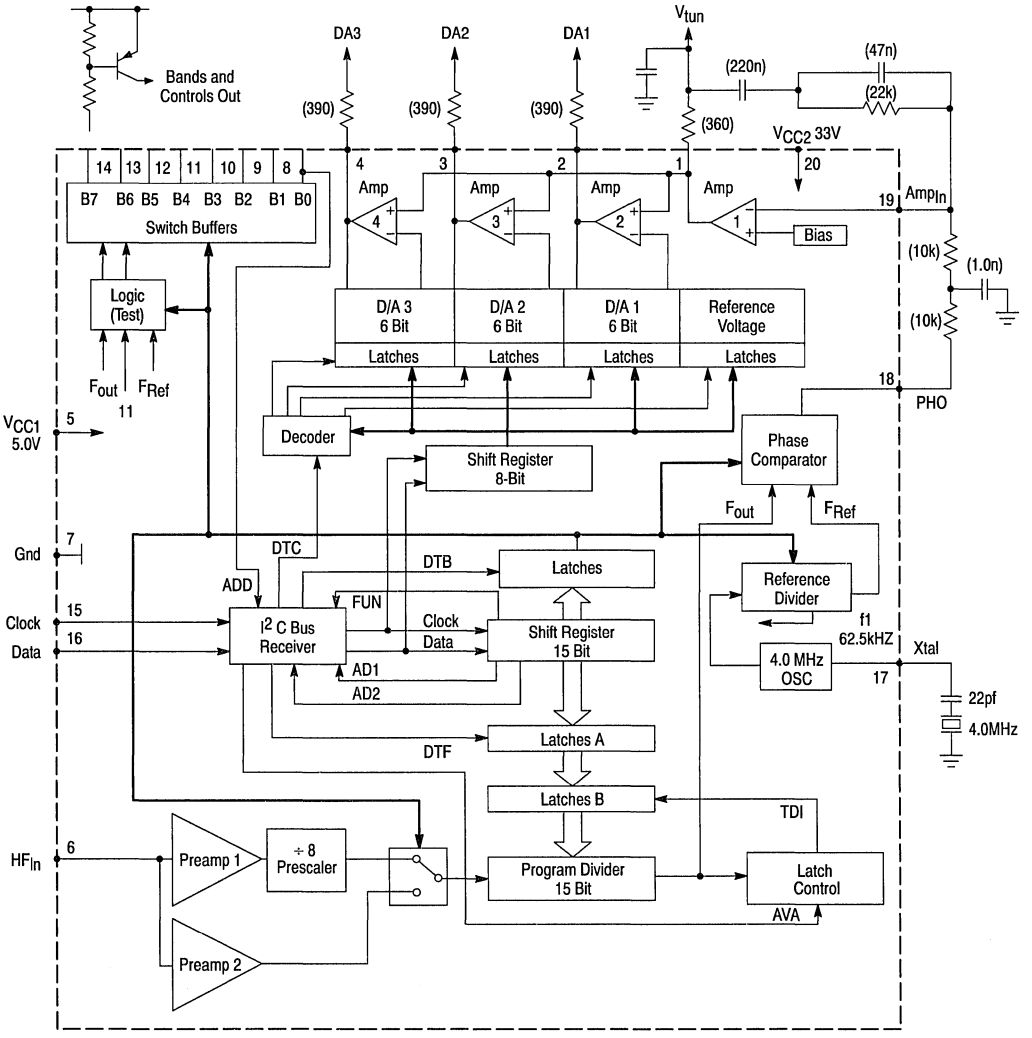
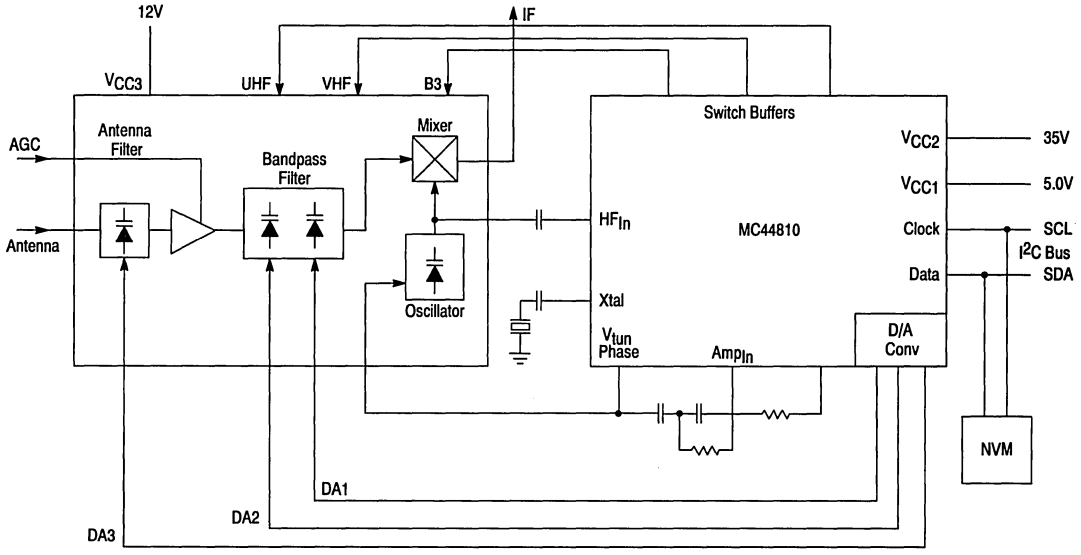


Figure 5. TV Tuner for Automatic Alignment



PLL SECTION

Data Format and Bus Receiver

The circuit receives the information for tuning and control via the I²C Bus. The incoming information is treated in the I²C bus receiver.

Bus Protocol

1_STA	CA1	CO	BA	STO		
2_STA	CA1	FM	FL	STO		
3_STA	CA1	CO	BA	FM	FL	STO
4_STA	CA1	FM	FL	CO	BA	STO

STA = Start Condition
STO = Stop Condition
CA1 = Chip Address Byte of PLL Section
CO = Data Byte for Control Information
BA = Data Byte for Band Information
FM = Data Byte for Frequency Information (MSBs)
FL = Data Byte for Frequency Information (LSBs)

Figure 6. Definition of Bytes

CA1_Chip Address	1	1	0	0	0	0/1	1	0	ACK
CO_Control Information	F=1	R6	T	P	R3	R2	R1	R0	ACK
BA_Band Information	B7	B6	B5	B4	X	B2	B1	B0	ACK
FM_Freq Info (with MSB)	F=0	N14	N13	N12	N11	N10	N9	N8	ACK
FL_Freq Info (with LSB)	N7	N6	N5	N4	N3	N2	N1	N0	ACK

Figure 6 shows the five bytes of information that are needed for circuit operation: there is the chip address, two bytes of control and band information and two bytes of frequency information.

After the chip address, two or four data bytes may be received. If three data bytes are received the third data byte is ignored. If five or more data bytes are received the fifth and following data bytes are ignored and the last acknowledge pulse is sent at the end of the fourth data byte.

The first and third data bytes contain a function bit F. If the function bit F=0, frequency information is acknowledged and if F=1, control/band information is acknowledged.

If the address is correct (signal AD1) the information is loaded into latches.

A function bit in the first and third data byte is used to pass this data either into the latches for the programmable divider (signal DTF) or into the latches for band and control information (signal DTB). The data transfer to the latches (signals DTF and DTB) is initiated after the 2nd and 4th data bytes.

A second string of latches is used for the data transfer into the programmable divider to inhibit the transfer during the preset operation (signal TDI, signal AVA is an internal "address valid" command).

The control and band information bits have the following functions:

Bit R0 and R1 (See Table 1) Define the reference divider division ratio. Four ratios are available.

Bit R2 and R3 (See Table 2) Are used to switch internal signals to the buffer outputs. Pin 11 and 12.

Bit R2, R6 and T (See Table 3) Are used to control the phase comparator output stage.

Bit P (See Table 6) Switches the prescaler in and out. At Logic "1" the prescaler is bypassed and the power supply of the prescaler is switched off.

Bits B0 to B7 (See Table 7) Controls the buffers. At logic "1" the buffers are active (low).

The circuit has two PLL chip addresses. The PLL chip address is programmable by Pin 8. When Pin 8 is open or normally used as a buffer the first PLL address is selected as follows:

MSB LSB

PLL Address 1: 1 1 0 0 0 0 1 0 = C2 (octal)

When Pin 8 is at ground the 2nd address is selected.

PLL Address 2: 1 1 0 0 0 1 1 0 = C6 (octal)

Bit B4 must be "zero" when Pin 11 is used to output 62.5 kHz. Bits B4 and B5 have to be "zero" to output F_{ref} and FBY2. FBY2 is the programmable divider output frequency divided by two.

The data transfer to the latches (signals DTF and DTB) is initiated after the 2nd and 4th data bytes. The bus receiver fulfills the standard I^2C bus specifications.

The switching levels of Clock and Data (Pins 15 and 16) are 0.5 x V_{CC1}.

Table 1

Input Data R0	Input Data R1	Reference Divider Division Ratio
0	0	2048
1	0	1024
0	1	512
1	1	256

Table 2

Input Data R2	Input Data R3	Test Outputs on Buffers Pin 11	Pin12
0	0	62.5 kHz	—
0	1	F_{Ref}	FBY2
1	0	—	—
1	1	—	—

Table 3

Input Data R2	R6	T	Output State of the Phase Comparator
0	0	0	Normal Operation
0	0	1	Off (High Impedance)
0	1	0	High
0	1	1	Low
1	0	0	Normal Operation
1	0	1	Off
1	1	0	Normal Operation
1	1	1	Off

Band Buffers – The band buffers are open collector transistors and are active "low" at Bn = 1. They are designed for 10 mA with a typical on-resistance of 70 Ω. These buffers are designed to withstand relative high output voltage in the off-state. (16 V)

B2 and B3 buffers (Pins 11 and 12) may also be used to output internal IC signals (reference frequency and programmable divider output frequency ÷ 2) for test purposes.

Buffer B2 may also be used to output a 62.5 kHz frequency from an intermediate stage of the reference divider. The bit B2 and/or B3 has to be zero if the buffers are used for these additional functions.

Buffer B0, Pin 8, is also used to select the chip address. This buffer has a higher on-voltage than the other buffers.

Programmable Divider – The programmable divider is a presettable down counter. When it has counted to zero it takes its required division ratio out of the Latches B. Latches B are loaded from Latches A by means of signal TDI which is synchronous to the programmable divider output signal.

Since Latches A receive the data asynchronously with the programmable divider, this double latch scheme is needed to assure correct data transfer to the counter.

The division ratio definition is given by:

N = 16384 x N14 + 8132 x N13 +...+ 4 x N2 + 2 x N1 + N0

Maximum ratio 32767, minimum ratio 17, where N0...N14 are the different bits for frequency information.

The counter may be used for any ratio between 17 and 32767 and reloads correctly as long as its output frequency does not exceed 1.0 MHz.

The data transfer between Latches A and B (signal TDI) is also initiated by any start condition on the I^2C Bus.

At power-on the whole bus receiver is reset and the programmable divider is set to a counting ratio of N=256 or higher.

Prescaler – The prescaler has a preamp and may be bypassed (Bit P). The signal then passes through preamp 2. Table 6 shows the frequency ranges which may be synthesized with and without prescaler.

Phase Comparator – The phase comparator is phase and frequency sensitive and has very low output leakage current in the high impedance state.

Operational Amplifier – The operational amplifier for the tuning voltage is designed for very low noise, low input bias current and high power supply rejection. The positive input is biased internally. The op amp needs 32 V supply (V_{CC2}) as minimum voltage for a guaranteed maximum tuning voltage of 28 V.

Figure 4 shows a possible filter arrangement. The component values depend very much on the application (tuner characteristic, reference frequency, etc.).

As a starting point for optimization, the component values in Figure 4 may be used for 7.8125 kHz reference frequency in a multiband TV tuner.

Oscillator – The oscillator uses a 4.0 MHz crystal tied to ground through a capacitor, used in the series resonance mode. The voltage at Pin 17 "crystal" has low amplitude and low harmonic distortion.

D/A SECTION

Basic Function

The D/A section has two separate chip addresses from the PLL section. Three D-to-A converters that have a resolution of 6 bits (5 bits plus sign) are on chip. The analog output voltages are DC. The converters are buffered to the analog outputs DA1, DA2 and DA3 by operational amplifiers with an output voltage range that is equal to the tuning voltage range (about 0 V to 30 V). The op amps are arranged such that a positive or negative offset can be generated from the tuning voltage.

Data Format

The D-to-A information consists of the D/A chip address (CA2) and four data bytes. The first two bits of the data bytes are used as the function address. Thus the bytes C1, C2 and C3 contain the address for the individual converter and the 6 bits to be converted. Bit D5 is the sign (logic = 1 positive offset, logic = 0 negative offset) and the bits D0 to D4 determine the number of steps to be made as an offset from the tuning voltage. The bits S0 and S1 in the data byte RA define the step size (Vstep) and the range of the converters (see Table 4 and 5). The range is the same for all converters.

Bus Protocols

1_STA	CA2	C1	STO			
2_STA	CA2	C1	C2	STO		
3_STA	CA2	C1	C2	C3	STO	
4_STA	CA2	C1	C2	C3	RA	STO
5_STA	CA2	RA	C1	C2	C3	STO
6_STA	CA2	C1	C1	C1	C1	STO

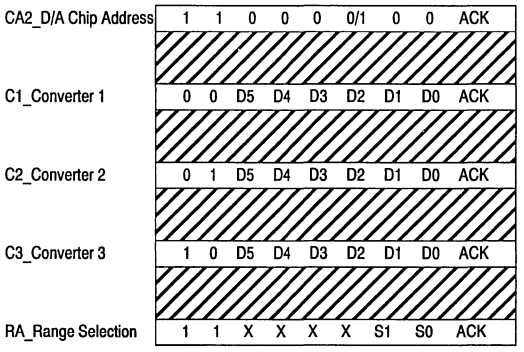
STA = Start Condition
STO = Stop Condition
CA2 = Chip Address Byte for D/A Section
C1,C2,C3 = Data Bytes for D/A Converters
RA = Data Byte for Range

The bus receiver accepts up to four data bytes in random sequences. If more than four data bytes are received, the fifth and following data bytes are ignored. The same data byte may be sent up to four times as shown in example 6.

After the chip address (CA2), up to four data bytes may be received. If more than four bytes are received the fifth and following bytes are ignored and the last acknowledged pulse is sent after the fourth data byte. The data transfer to the converters (signal DTC) is initiated each time a complete data byte is received.

Figure 7 shows some examples of the permissible bus protocols of the D-to-A section. The data bytes may be sent to the IC in random order with up to four in one sequence. The same converter may be loaded up to four times as shown in example 6 (see Bus Protocols).

Figure 7. Definition of Bytes



The D/A section has two separate chip addresses. These are programmable by Pin 8 as in the PLL section. When Pin 8 is open or normally used as a buffer, the first D/A address is selected as follows:

MSB LSB
D/A Address 1: 1 1 0 0 0 0 0 0 = C0 (octal)
When Pin 8 is at ground the second D/A address is selected.
D/A Address 2: 1 1 0 0 0 1 0 0 = C4 (octal)

Table 4. Output Voltage

VDA = Vtun ± Vstep (D0 + 2D1 + 4D2 + 8D3 + 16D4)
D5 = "1" positive sign; D5 = "0" negative sign Vtun: Tuning Voltage set by PLL Vstep: Voltage STEP (LSB) of the D/A converters

Table 5. Range Selection

Input Data S1	Input Data S0	Typ. Step Size Vstep (mV)	Guaranteed Range 31 Steps (V)
0	0	225	6.25
0	1	125	3.40
1	0	70	1.90
1	1	40	1.05

D/A Converters – The D/A converters convert 5-bit into an analog current of which the polarity is switched by the sixth bit. The reference voltage of the converters is programmed by two bits (S0, S1 of the RA-byte) to determine the scaling factor. The analog currents are then converted into voltages by means of op amps 2, 3 and 4 and the voltages are added to the tuning voltage (V_{tun}, see Figure 4) to generate the positive or negative offset.

If the data bits D0 to D5 are logic "0" the three D/A output voltages on Pins 2, 3 and 4 are equal to the tuning voltage (Pin 1) within the input offset voltages of the op amps (maximum error 0.5 LSB).

The four amplifiers have the same output characteristics with the maximum output voltage being 4.0 V lower than V_{CC2} in the worst case. The four analog outputs are short circuit protected. At power-up the D/A outputs are undetermined.

The four op amp outputs require external resistors (390 Ω) for stability.

The D/A converters are guaranteed to be monotonic with a voltage step variation of ± 0.5 LSB. The temperature stability is ± 0.5 LSB from 0° to 70°C.

Table 6

Input Data P	Prescaler Function
0	Active
1	Bypassed, Power Supply Off

Table 7

Input Data B0...B7	Band Buffers (Output State)
0	Off
1	On

Table 8. System Application (Using a 4.0 MHz Crystal)

Input Data R1	Input Data R0	Reference Divider Division Ratio	Reference Frequency (1) (Hz)	With Internal Prescaler (P=0) Frequency Steps (kHz)	With Internal Prescaler (P=0) Max Input Frequency (MHz)	Without Internal Prescaler (P=1) Frequency Steps (kHz)	Without Internal Prescaler (P=1) Max Input Frequency (MHz)
0	0	2048	1953.125	15.625	512	1.953125	64
0	1	1024	3906.25	31.25	1024	3.90625	128
1	0	512	7812.5	62.5	1300 (2)	7.8125	165 (3)
1	1	256	15625.0	125	1300 (2)	15.625	165 (3)

(1) With 4.0 MHz Crystal (2) Limit of Prescaler (3) Limit of Programmable Divider

TDA3190

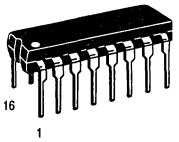
4.2 WATT
TV SOUND SYSTEM

**SILICON MONOLITHIC
INTEGRATED CIRCUIT**

TV Sound System

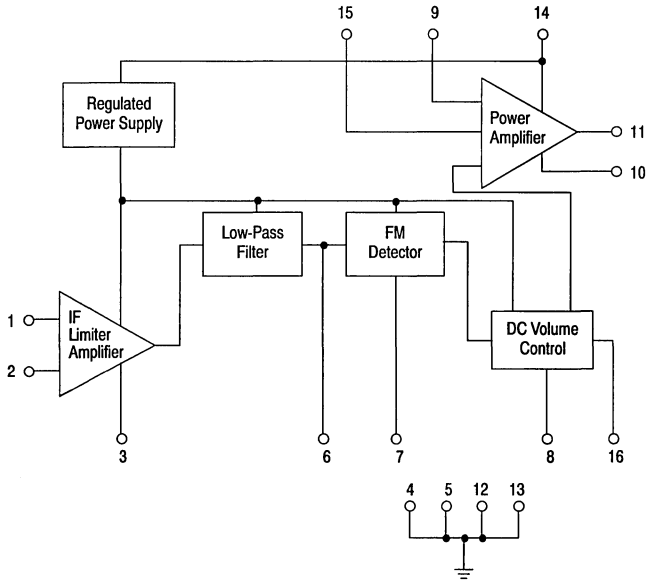
The TDA3190 is a 4.2 W sound system designed for television and related applications. Functions performed by this device includes: IF Limiting, IF amplifier, low pass filter, FM detector, DC volume control, audio preamplifier, and audio power amplifier.

- 4.2 W Output Power (V_{CC} = 24 V, R_L = 16 Ω)
- Linear Volume Control
- High AM Rejection
- Low Harmonic Distortion
- High Sensitivity

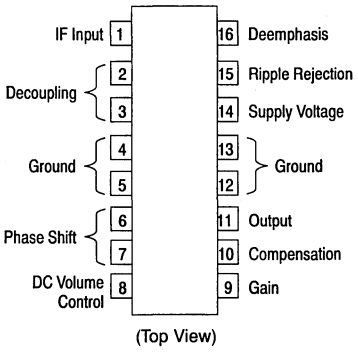


P SUFFIX
PLASTIC PACKAGE
CASE 648C

BLOCK DIAGRAM



PIN CONNECTIONS



(Top View)

9

MAXIMUM RATINGS

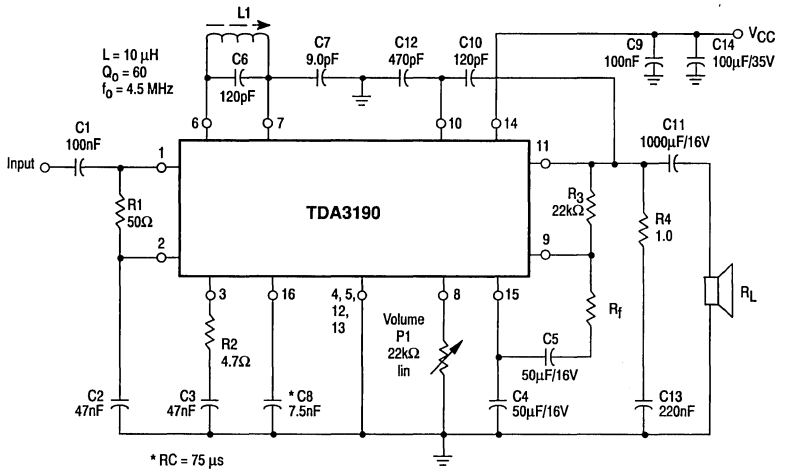
Rating	Symbol	Value	Unit
Supply Voltage Range	V_{CC}	9.0 to 28	V
Output Peak Current (Nonrepetitive) (Repetitive)	I_O	2.0 1.5	A
Input Signal Voltage	V_I	1.0	V
Operating Temperature Range	T_A	0 to + 75	°C
Junction Temperature	T_J	150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 24 V, f_o = 4.5 MHz, Δf = ±25 kHz, T_A = 25°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Quiescent Output Voltage (Pin 11) V_{CC} = 24 V	Q_O	11	12	13	V
Quiescent Drain Current (P1 = 22 kΩ) V_{CC} = 24 V	I_D	11	22	35	mA
Output Power (d = 10%, f_m = 400 Hz) V_{CC} = 24 V, R_L = 16 Ω V_{CC} = 12 V, R_L = 8.0 Ω (d = 2%, f_m = 400 Hz) V_{CC} = 24 V, R_L = 16 Ω V_{CC} = 12 V, R_L = 8.0 Ω	P_O	 — — — —	 4.2 1.5 3.5 1.4	 — — — —	W
Input Limiting Threshold Volts (–3.0 dB) at Pin 1 Δf = ±7.5 kHz, f_m = 400 Hz, set P1 for 2.0 Vrms on Pin 11	V_I	—	40	100	μV
Distortion (P_O = 50 mW, f_m = 400 Hz, Δf = ± 7.5 kHz) V_{CC} = 24 V, R_L = 16 Ω		—	0.75	—	%
Frequency Response of Audio Amplifier (–3.0 dB) (R_L = 16 Ω, C_{10} = 120 pF, C_{12} = 470 pF, P_1 = 22 kΩ) R_f = 82 Ω R_f = 47 Ω	B	 — —	 70 to 12 k 70 to 7.0 k	 — —	Hz
Recovered Audio Voltage (Pin 16) (V_I ≥ 1.0 mV, f_m = 400 Hz, Δf = ± 7.5 kHz, P_1 = 0)	V_o	—	120	—	mV
Amplitude Modulation Rejection (V_I ≥ 1.0 mV, f_m = 400 Hz, m = 30%)	AMR	—	55	—	dB
Signal and Noise to Noise Ratio (V_I ≥ 1.0 mV, V_O = 4.0 V, f_m = 400 Hz)	$\frac{S+N}{N}$	50	65	—	dB
Input Resistance (Pin 1) (V_I = 1.0 mV)	r_i	—	30	—	kΩ
Input Capacitance (Pin 1) (V_I = 1.0 mV)	C_i	—	5.0	—	pF
DC Volume Control Attenuation (P1 = 12 kΩ)		—	90	—	dB

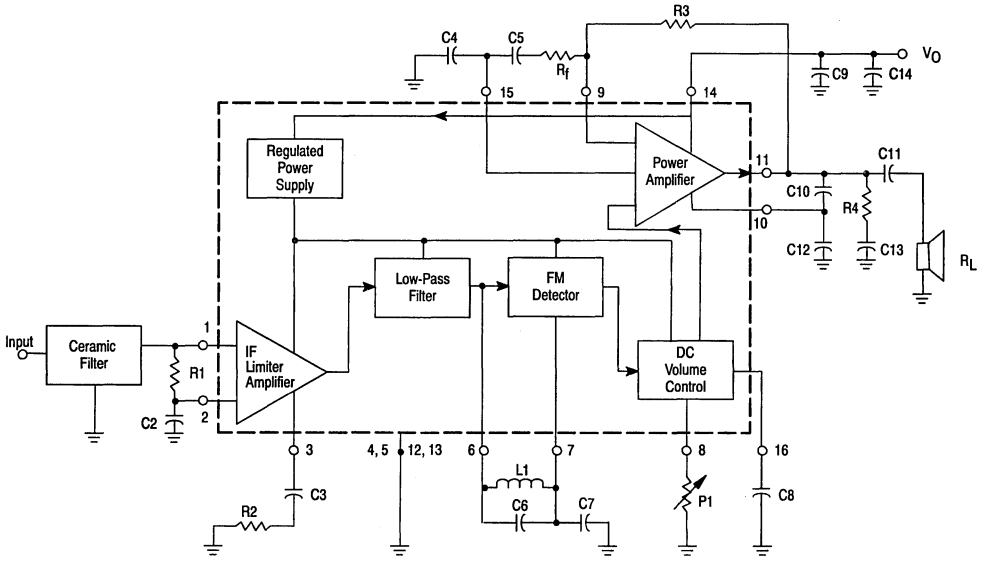
9

TEST CIRCUIT



V_{CC}	12	24	V
R_L	8	16	Ω
R_f	82	47	Ω

TYPICAL CIRCUIT CONFIGURATION



TDA3301B

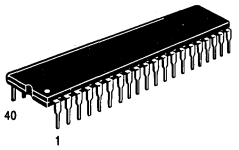
TV COLOR PROCESSOR

SILICON MONOLITHIC
INTEGRATED CIRCUIT

TV COLOR PROCESSOR

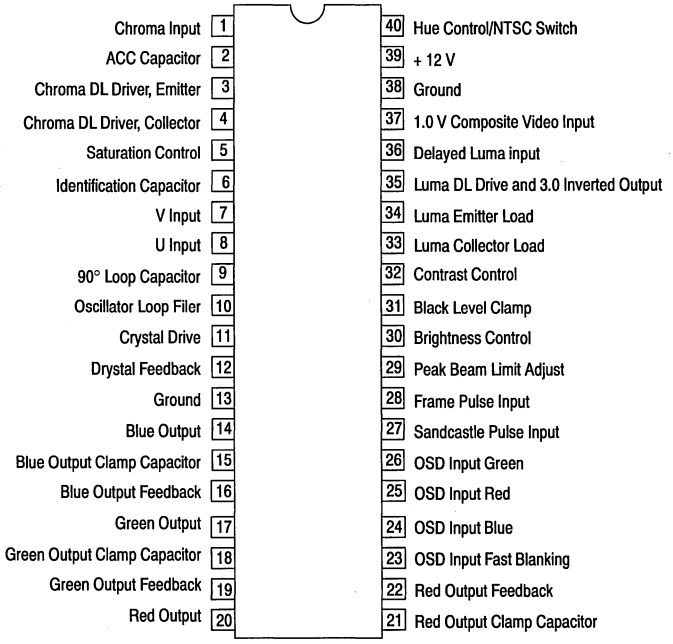
This device will accept a PAL or NTSC composite video signal and output the three color signals, needing only a simple driver amplifier to interface to the picture tube. The provision of high bandwidth on-screen display inputs makes it suitable for text display, TV games, cameras, etc. The TDA3301B has user control laws, and also a phase shift control which operates in PAL, as well as NTSC.

- Automatic Black Level Setup
- Beam Current Limiting
- Uses Inexpensive 4.43 MHz to 3.58 MHz Crystal
- No Oscillator Adjustment Required
- Three OSD Inputs Plus Fast Blanking Input
- Four DC, High Impedance User Controls
- Interfaces with TDA33030B SECAM Adaptor
- Single 12 V Supply
- Low Dissipation, Typically 600 mW



P SUFFIX
PLASTIC PACKAGE
CASE 711

PIN CONNECTIONS



MAXIMUM RATINGS (T_A = + 25°C, unless otherwise noted.)

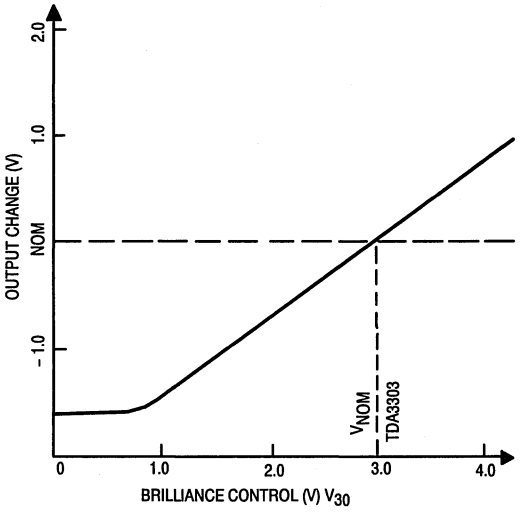
Rating	Symbol	Value	Unit
Supply Voltage (Pin 39)	V_{CC}	14	Vdc
Operating Temperature Range	T_A	0 to + 70	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

ELECTRICAL CHARACTERICISTICS (T_A = 25°C, V_{CC} = 12 V)

Characteristics	Pin	Min	Typ	Max	Unit
Supply Voltage Supply Current	39	10.8 —	12 45	13.2 60	V mA
Composite Video Input Video Input Resistance Video Gain to Pin 35 Input Window	37	— 13 2.7 0.8–3	1.0 18 3.2 0.7–3.2	— 23 3.6 —	Vp-p kΩ Vp-p V
Chrome Input (Burst) Input Resistance ACC Effectiveness	1 1 4	10 — —	100 5.0 1.2	200 — 3.0	mVp-p kΩ dB
OSD Input OSD Drive Impedance OSD Frequency Response (–3.0 dB) OSD Max Gain Gain Difference Between Any Two	24, 25, 26	0.5 — 9.0 — —	0.7 — — 7.2 —	1.0 180 — — 15	V Ω MHz %
Beam Current Ref. Threshold Differential Voltage Beam Current Ref. Input Current Differential Current	16, 19, 22	1.7 — — —	2.0 — — —	2.3 20 +1.5/–0.5 1.0	V mV µA
Luminance Gain Between Pin 36 and Outputs (Depends on R_{333} and R_{34}) Luminance Bandwidth (–3.0 dB) Output Resistance Residual Carrier (4.43 Mc/s) PAL Offset (H/2) Difference in Gain Between Y Input and any RGB o/p	14, 17, 20	— 9.0 120 — — —	4.7 — 170 30 — 5.0	— — 300 150 50 —	 MHz Ω mVp-p %
U Input Sensitivity for 5.0 V Blue Output	8	—	340	—	mVp-p
Matrix Error	14, 17, 20	—	—	10	%
Oscillator Capture Range		350	—	—	Hz
U Ref. Phase Error		—	—	5.0	Degrees
V Ref. Phase Error		—	—	5.0	Degrees
Color Kill Attenuation	14, 17, 20	50	—	—	dB
Contrast Tracking OSD/Luma/Chroma	14, 17, 20	—	—	—	dB
OSD Contrast Tracking	14, 17, 20	—	—	±2.0	dB
OSD Enable Slice Level	23	—	0.7	—	V
Sandcastle Slice Level Burst Gate Line Blanking R Input V_{27} > 7.0 V V_{27} < 7.0 V	27	 6.5 2.0 — —	 7.2 2.6 5.0 22	 8.0 3.0 — —	 V kΩ
Frame Slice Level R Input	28	2 —	2.8 15	3.6 —	V kΩ
Peak Beam Limiter Threshold (I_{29} Min = 250 µA)		3.4 x I_{29}	4 x I_{29}	4.6 x I_{29}	
Pin 29 Input Resistance	29	—	5.0	—	kΩ
Pin 29 Open Circuit Voltage	29	—	10.6	—	V

INPUT/OUTPUT FUNCTIONS

Figure 1. Brillance Control

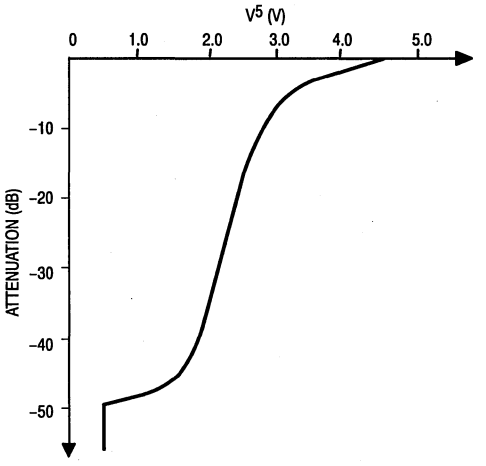


The brilliance control operates by adding a pedestal to the output signals. The amplitude of the pedestal is controlled by Pin 30.

During CRT beam current sampling a standard pedestal is substituted, its value being equivalent to the value given by V_{30} Nom Brightness at black level with V_{30} Nom is given by the sum of three gun currents at the sampling level, i.e. 3×20 µA with 100 k reference resistors on Pins 16, 19, and 22.

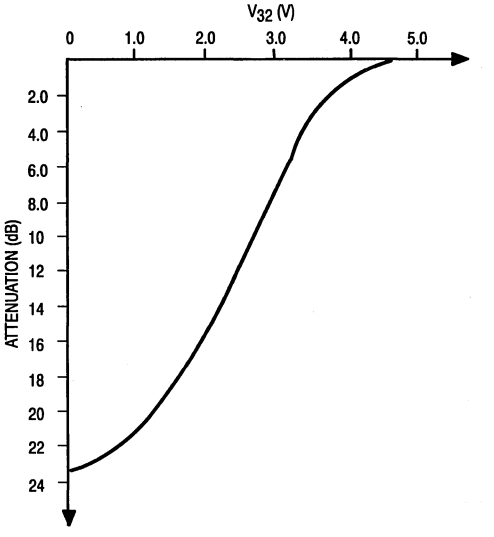
During picture blanking the brilliance pedestal is zero; therefore, the output voltage during blanking is always the minimum brilliance black level (Note: Signal channels are also gain blanked).

Figure 2. Saturation Control Voltage



Note: Nominal 100% saturation point is given by choice of R_2 which sets ACC operating point.
Pin 5 is automatically pulled to ground with a misidentified PAL signal.

Figure 3. Contrast Control



Note: Pin 32 is pulled down by the operation of the peak beam limiter.

Figure 4. Block Diagram

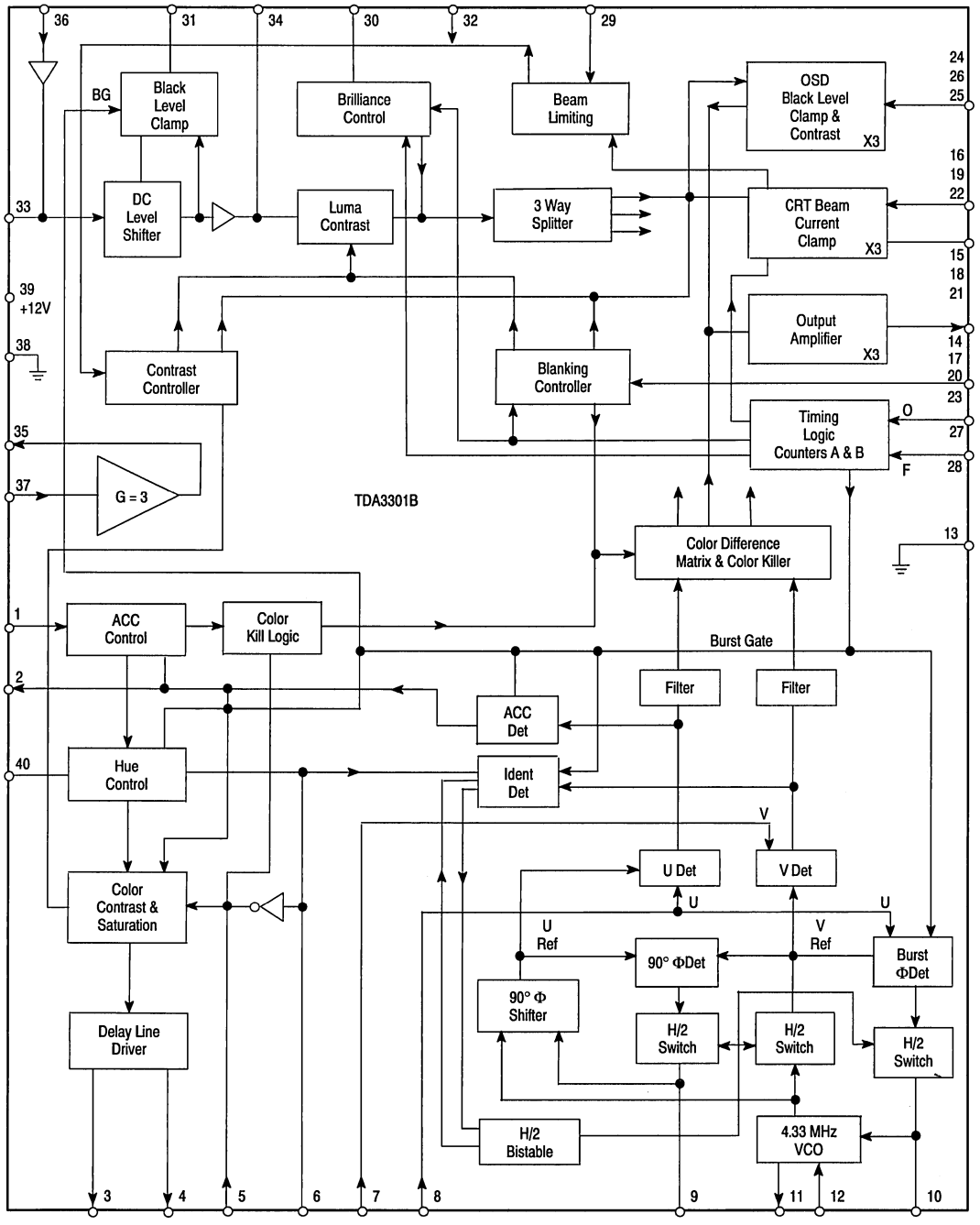
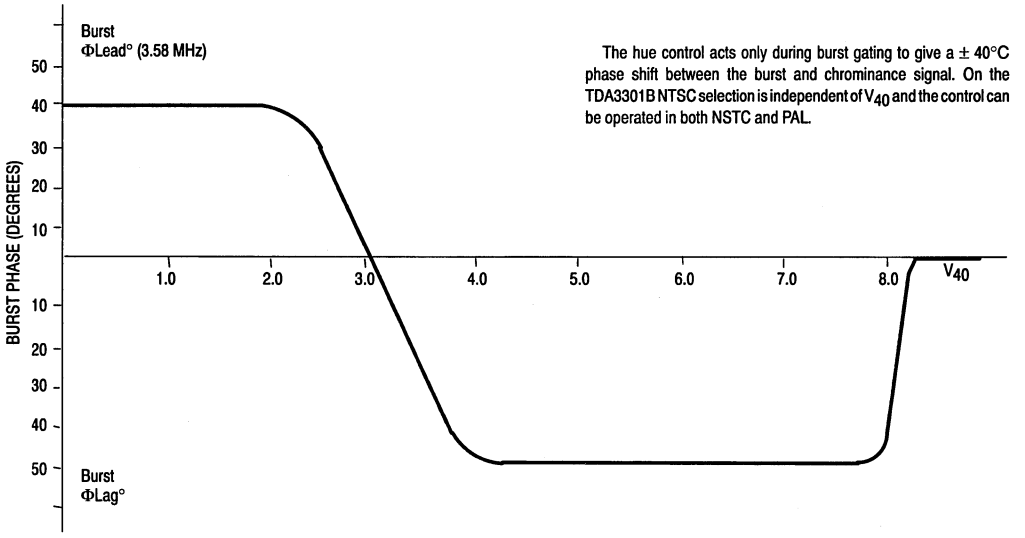


Figure 5. Hue Control



CIRCUIT OPERATION

Chrominance Decoder

The chrominance decoder section of the TDA3301B consists of the following blocks:

Phase-locked reference oscillator; Figures 6, 7 and 8.
Phase-locked 90 degree servo loop; Figures 8 and 9.
U and V axis decoders
ACC detector and identification detector; Figure 10.
Identification circuits and PAL bistable; Figure 11.
Color difference filters and matrixes with fast blanking circuits.

The major design considerations apart from optimum performance were:

- A minimum number of factory adjustments,
- A minimum number of external components,
- Compatibility with SECAM adapter TDA3030B,
- Low dissipation,
- Use of a standard 4.433618 Mhz crystal rather than a 2.0 fc crystal with a divider.

Reference Regeneration

The crystal VCO is of the phase shift variety in which the frequency is controlled by varying the phase of the feedback. A great deal of care was taken to ensure that the oscillator loop gain and the crystal loading impedance were held constant in order to ensure that the circuit functions well with low grade crystal (crystals having high magnitude spurious responses can cause bad phase jitter). It is also necessary to ensure that the gain at third harmonic is low enough to ensure absence of oscillation at this frequency.

Figure 6. Voltage Controlled Osscillator (VCO)

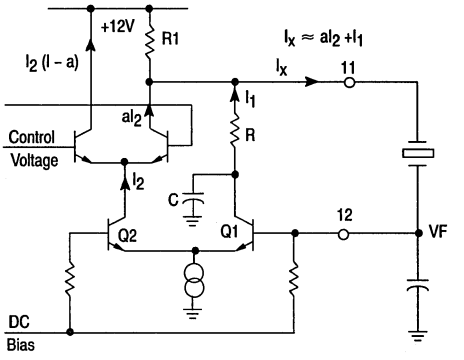
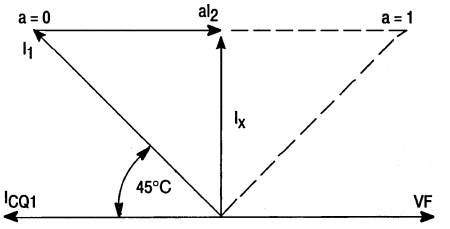


Figure 7. Vector Diagram for VCO



By referring to Figures 6 and 7 it can be seen that the necessary ± 45°C phase shift is obtained by variable addition of two currents I_1 and I_2 which are then fed into the load resistance of the crystal tuned circuit R_1. Feedback is taken from the crystal load capacitance which gives a voltage of VF lagging the crystal current by 90°.

The RC network in the T_1 collector causes I_1 to lag the collector current of T_1 by 45°.

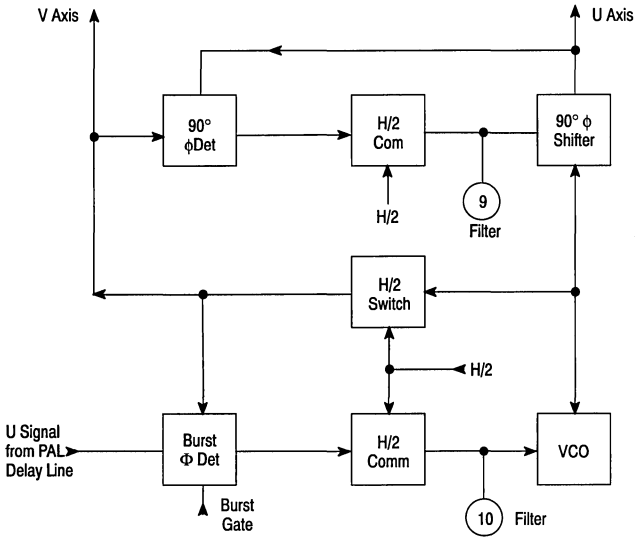
For SECAM operation, the currents I_1 and I_2 are added together in a fixed ratio giving a frequency close to nominal.

When decoding PAL there are two departures from normal chroma reference regeneration practice:

a) The loop is locked to the burst entering from the PAL delay line matrix U channel and hence there is no alternating component. A small improvement in signal noise ratio is gained but more important is that the loop filter is not compromised by the 7.8 kHz component normally required at this point for PAL identification
b) The H/2 switching of the oscillator phase is carried out before the phase detector. This implies any error signal from the phase detector is a signal at 7.8 kHz and not dc. A commutator at the phase detector output also driven from the PAL bistable coverts this ac signal to a dc prior to the loop filter. The purpose of this is that constant offsets in the phase detector are converted by the commutator to a signal at 7.8 kHz which is integrated to zero and does not give a phase error.

When used for decoding NTSC the bistable is inhibited, and slightly less accurate phasing is achieved; however, as a hue control is used on NTSC this cannot be considered to be a serious disadvantage.

Figure 8. Block Diagram of Reference Section



90° Reference Generation

To generate the U axis reference a variable all-pass network is utilized in a servo loop. The output of the all-pass network is compared with the oscillator output with a phase detector of which the output is filtered and corrects the operating point of the variable all-pass network (see Figure 9).

As with the reference loop the oscillator signal is taken after the H/2 phase switch and a commutator inserted before the filter so that constant phase detector errors are cancelled.

For SECAM operation the loop filter is grounded causing near zero phase shift so that the two synchronous detectors work in phase and not in quadrature.

The use of a 4.4 MHz oscillator and a servo loop to generate the required 90° reference signal allows the use of a standard, high volume, low cost crystal and gives an extremely accurate 90° which may be easily switched to 0° for decoding AM SECAM generated by the TDA3030B adapter.

Figure 9. Variable All-Pass Network

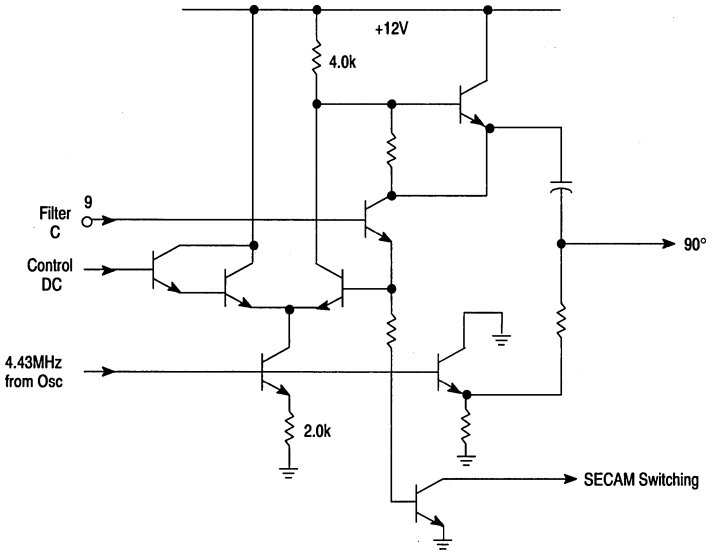
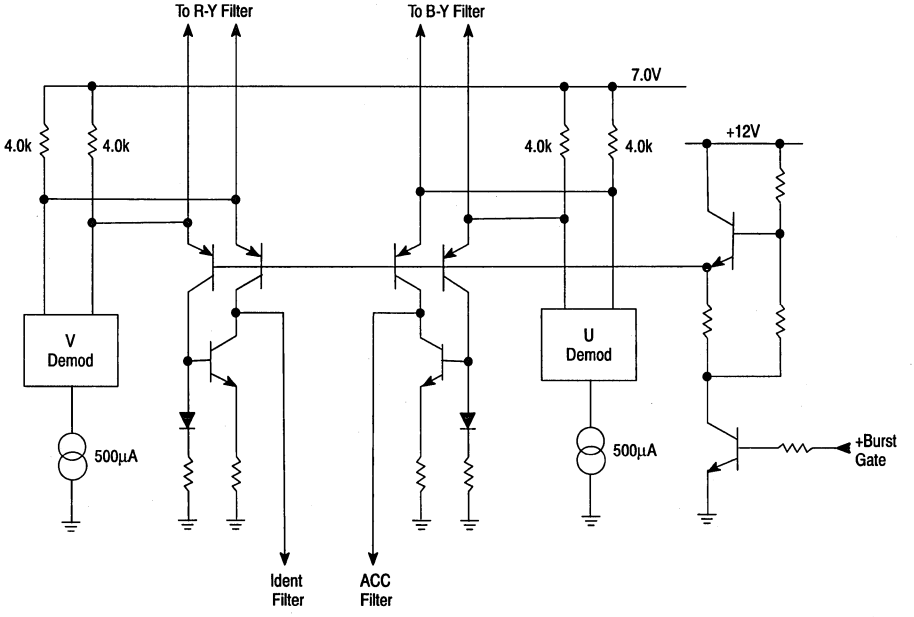


Figure 10. ACC and Identification Detectors



ACC and Identification Detectors

During burst gate time the output components of the U and also the V demodulators are steered into PNP emitters. One collector current of each PNP pair is mirrored and balanced against its twin giving push-pull current sources for driving the ACC and the identification filter capacitors.

The identification detector is given an internal offset by making the NPN current mirror emitter resistors unequal. The resistors are offset by 5% such that the identification detector pulls up on its filter capacitor with zero signal.

Identification

See Figure 11 for definitions.

Monochrome	$I_1 > I_2$
PAL Ident. OK	$I_1 < I_2$
PAL Ident. X	$I_1 > I_2$
NTSC	$I_3 > I_2$

Only for correctly identified PAL signal is the capacitor voltage held low since I_2 is then greater than I_1.

For monochrome and incorrectly identified PAL signals $I_1 > I_2$ hence voltage V_C rises with each burst gate pulse.

When $V_{ref}1$ is exceeded by 0.7 V Latch 1 is made to conduct which increases the rate of voltage rise on C. Maximum current is limited by R_1.

When $V_{ref}2$ is exceeded by 0.7 V then Latch 2 is made to conduct until C is completely discharged and the current drops to a value insufficient to hold on Latch 2.

As Latch 2 turns on Latch 1 must turn off.

Latch 2 turning on gives extra trigger pulse to bistable to correct identification.

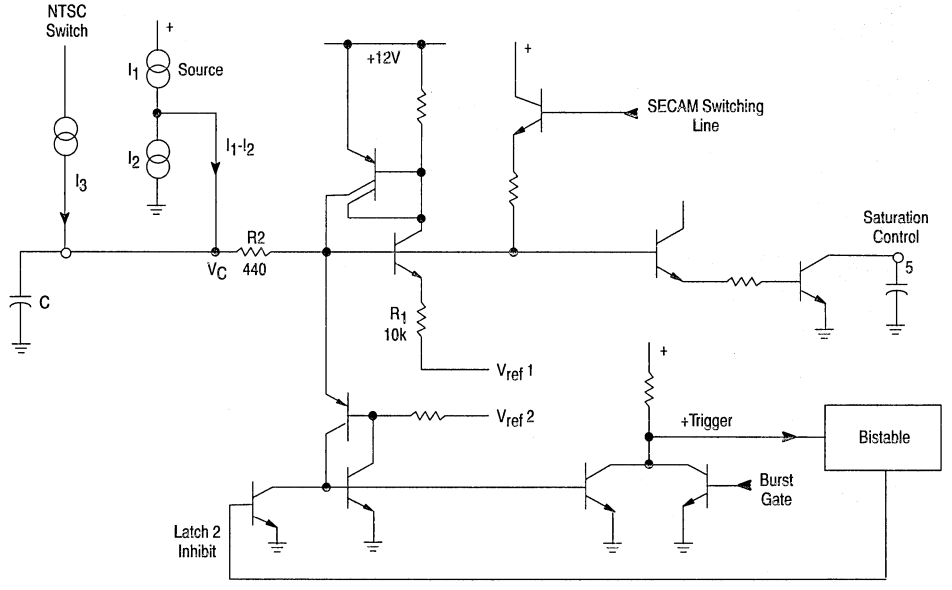
The inhibit line on Latch 2 restricts its conduction to alternate lines as controlled by the bistable. This function allows the SECAM switching line to inhibit the bistable operation by firing Latch 2 in the correct phase for SECAM. For NTSC, Latch 2 is fired by a current injected on Pin 6.

If the voltage on C is greater than 1.4 V, then the saturation is held down. Only for SECAM/NTSC with Latch 2 on, or correctly identified PAL, can the saturation control be anywhere but minimum.

NTSC Switch

NTSC operation is selected when current (I_3) is injected into Pin 6. On the TDA3301B this current must be derived externally by connecting Pin 6 to +12 V via a 27 k resistor (as on TDA3300B). For normal PAL operation Pin 40 should be connected to +12 V and Pin 6 to the filter capacitor.

Figure 11. Identification Circuit



Color Difference Matrixing, Color Killing, and Chroma Blanking

During picture time the two demodulators feed simple RC filters with emitter follower outputs. Color killing and blanking is performed by lifting these outputs to a voltage above the maximum value that the color difference signal could supply.

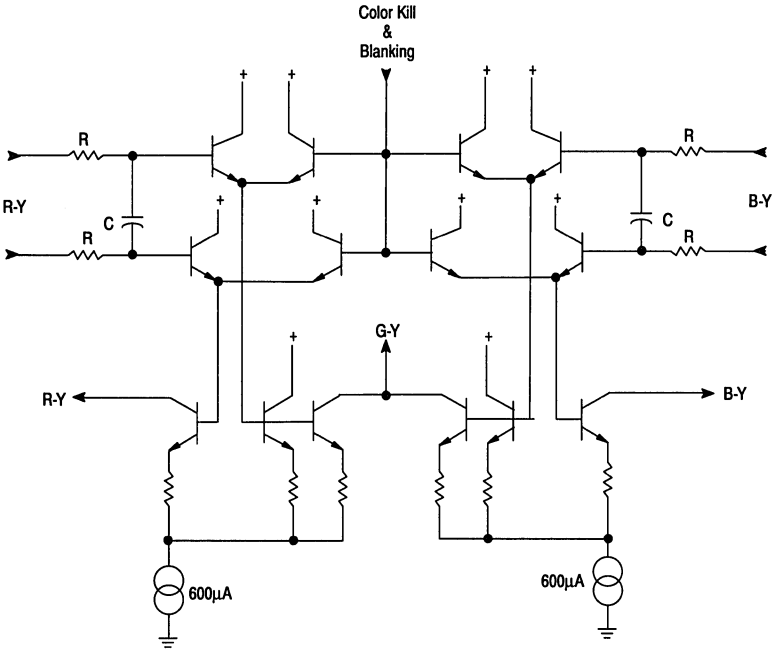
The color difference matrixing is performed by two differential amplifiers, each with one side split to give the correct values of the –(B-Y) and –(R-Y) signals. These are added to give the (G-Y) signal.

The three color difference signals are then taken to the virtual grounds of the video output stages together with luminance signal.

Sandcastle Selection

The TDA3301B may be used with a two level sandcastle and a separate frame pulse to Pin 28, or with only a three level (super) sandcastle. In the latter case, a resistor of 1.0 MΩ is necessary from + 12 V to Pin 28 and a 470 pF capacitor from Pin 28 to ground.

Figure 12. Color Difference Stages



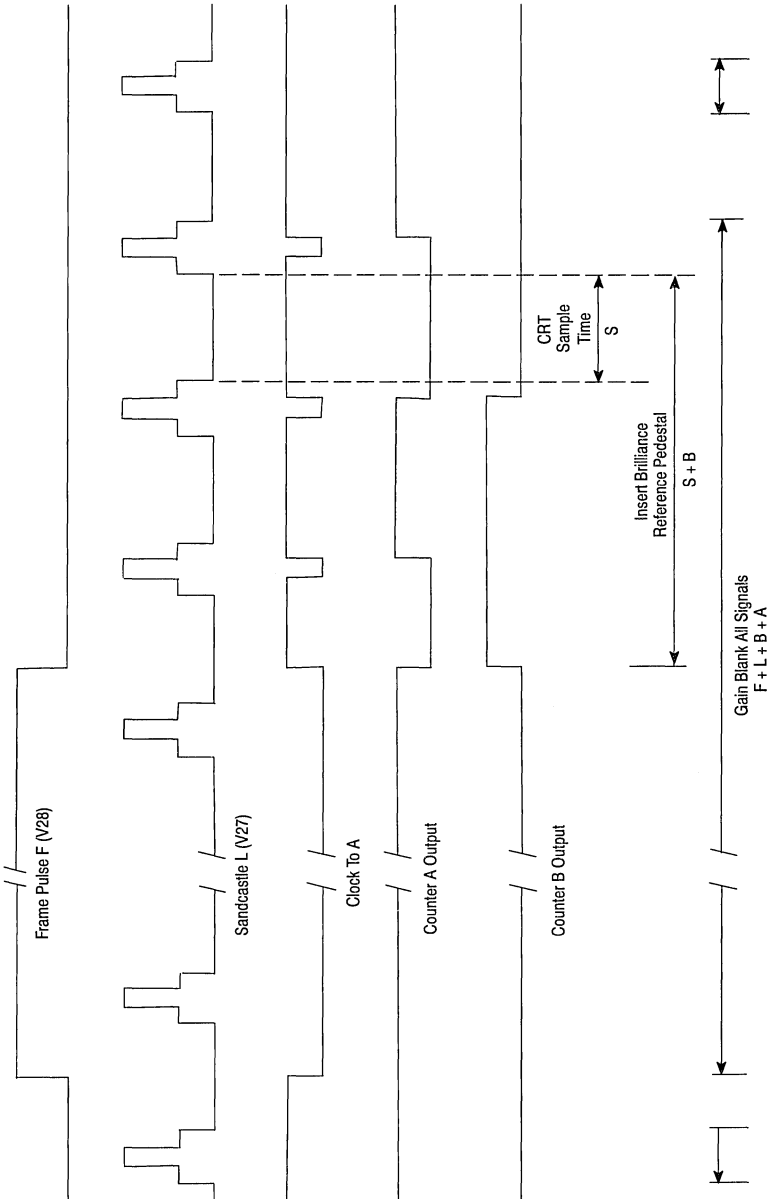


Figure 13. Timing Diagram

9

Timing Counter for Sample Control

In order to control beam current sampling at the beginning of each frame scan, two edge triggered flip-flops are used.

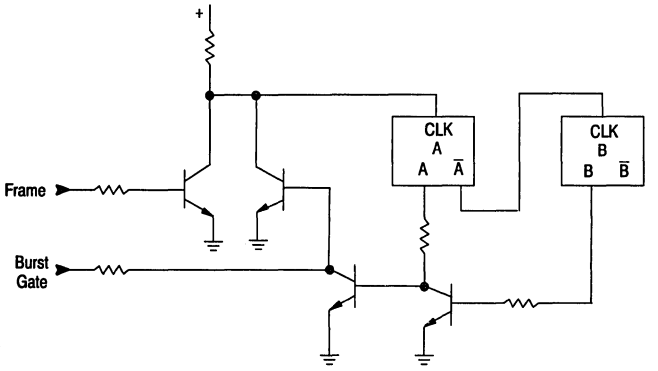
The output $\overline{A}$ of the first flip-flop A is used to clock the second flip-flop B. Clocking of A by the burst gate is inhibited by a count of $A.\overline{B}$.

The count sequence can only be initiated by the trailing edge of the frame pulse. In order to provide control signals for:

Luma/Chroma blanking
Beam current sampling
On-screen display blanking
Brilliance control

The appropriate flip-flop outputs ar matrixed with sandcastle and frame signals by an emitter-follower matrix.

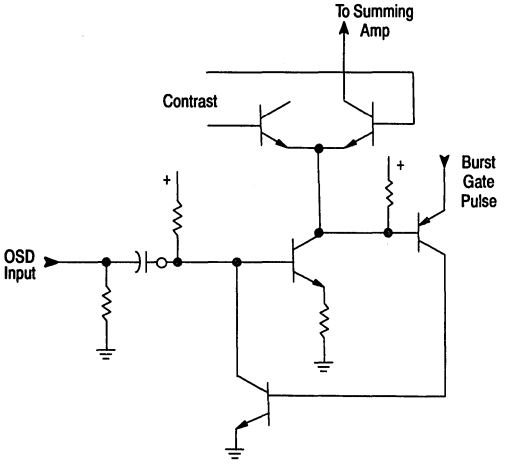
Figure 14. Timing Counter



On-Screen Display Inputs

Each section of the OSD stages consists of a common emitter input stage feeding a diversion gate controlled by the contrast control. During burst gate time a feedback loop is activated which clamps the signal at the input coupling capacitor. This ensures that the current in the diversion gate is zero at black level and the OSD black level insensitive to contrast control, also the inputs ignore signals below black, e.g. sync, pulses.

Figure 15. OSD Stage



Video Output Sections

Each video output stage consists of a feedback amplifier in which the input signal is a current drive to the virtual earth from the luminance, color difference and on-screen display stages.

A further drive current is used to control the DC operating point; this is derived from the sample and hold stage which samples the beam current after frame flyback.

Figure 16. Video Output Section

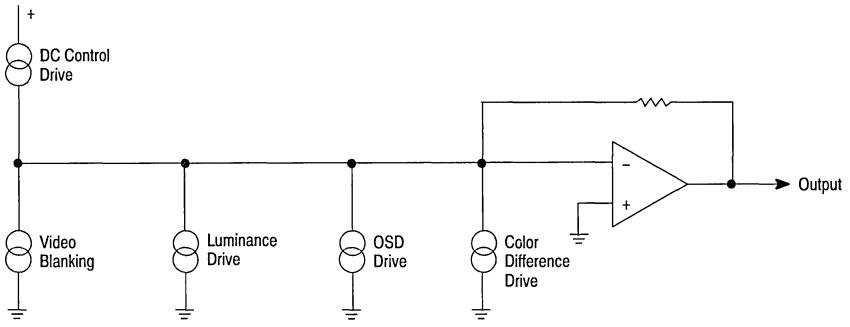
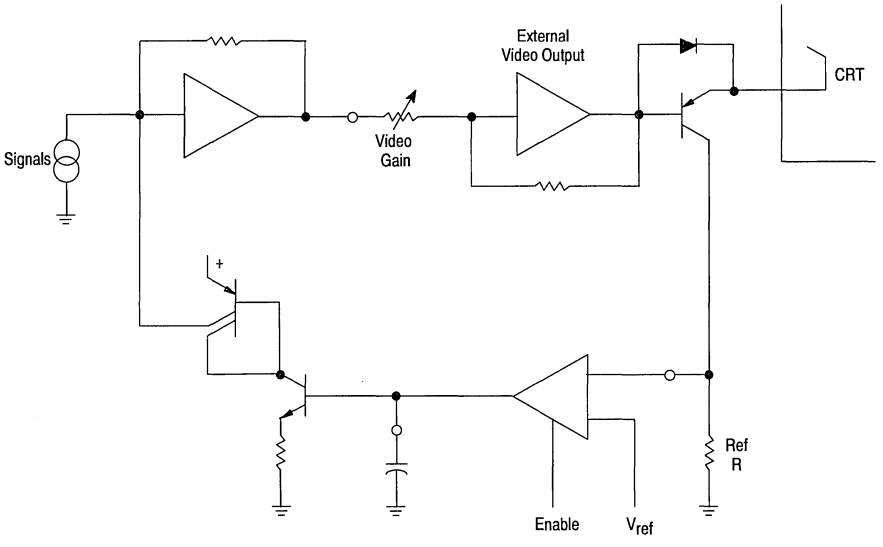
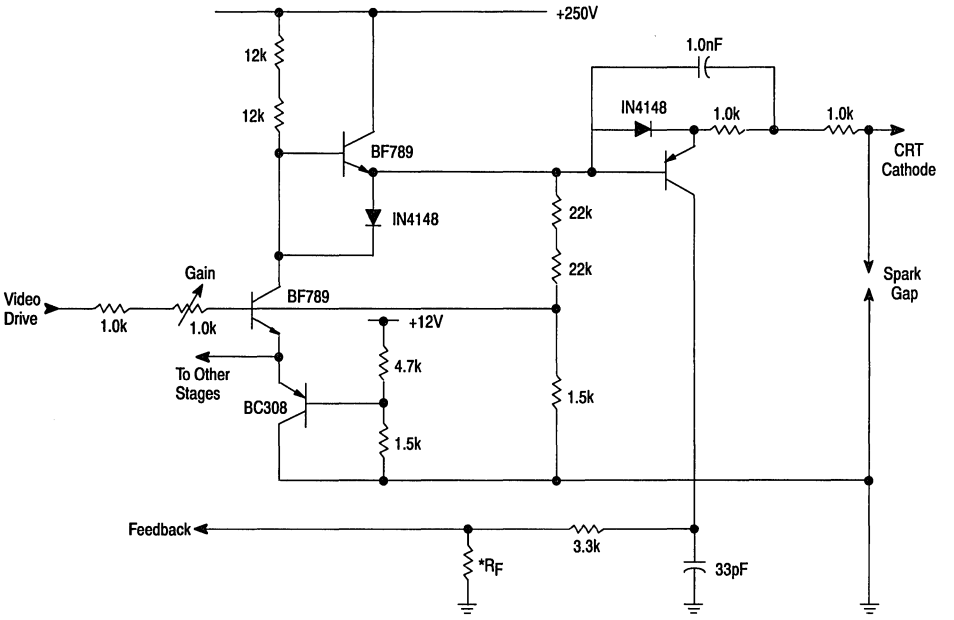


Figure 17. Complete Video Output Sections



9

Figure 18. Typical Video Output Stage



*R_F is chosen to suit CRT characteristics, typically 120 k.

9

Figure 19. Class A Video Output Stage with Direct Feedback

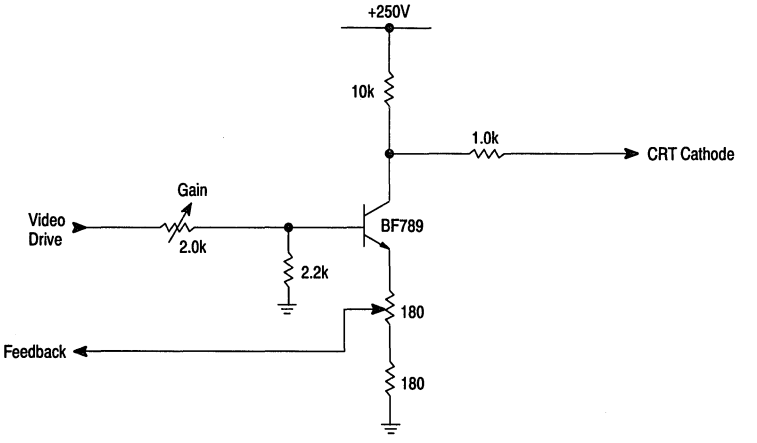
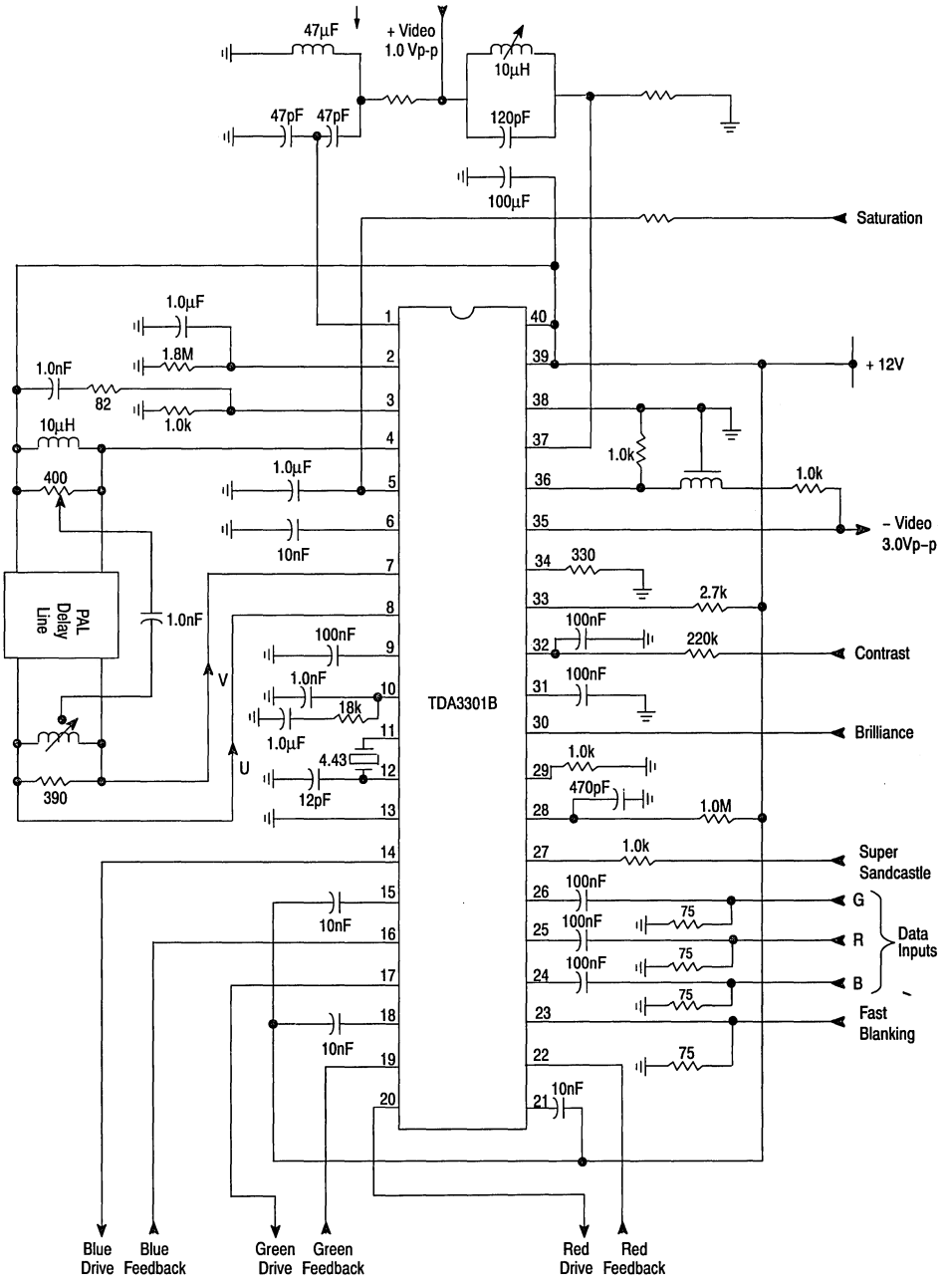


Figure 20. Typical PAL Application

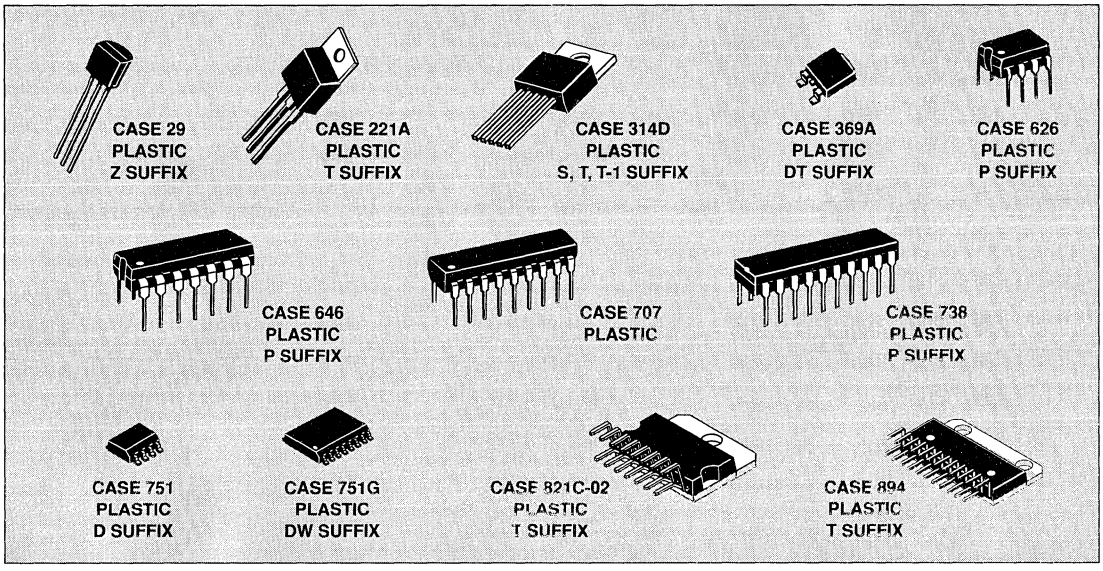


NOTE: When not using Super Sandcastle a positive vertical blanking pulse must be applied to Pin 28.

Automotive Electronic Circuits

In Brief . . .

Motorola Linear has established itself as a global leader in custom integrated circuits for the automotive market. With multiple design centers located on four continents, global process and assembly sites, and strategically located supply centers, Motorola serves the global automotive market needs. These products are key elements in the rapidly growing engine control, body, navigation, entertainment, and communication electronics portions of modern automobiles. Though Motorola is most active in supplying automotive custom designs, many of yesterday's proprietary custom devices become standard products of today available to the broad base manufactures who support this industry. Today, based on new technologies, Motorola offers a wide array of standard products ranging from rugged high current "smart" fuel injector drivers which control and protect the fuel management system, through rigors of the underhood environment, to the latest SMARTMOS™ switches and series transient protectors. Several devices are targeted to support microprocessor housekeeping and data line protection. A wide range of packaging is available from die, flip-chip, and SOICs for high density layouts, to low thermal resistance multi-pin, single-in-line types for high power control ICs.



Voltage Regulators

Function	Features	Suffix Case	Device
Low Dropout Voltage Regulator	Positive fixed and adjustable output voltage regulators which maintain regulation with very low input to output voltage differential.	Z/29, T/221A, T/314D, DT/369A	LM2931,C
Low Dropout Dual Regulator	Positive low voltage differential regulator which features dual 5.0 V outputs, with currents in excess of 750 mA (switched) and 10 mA standby, and quiescent current less than 3.0 mA.	T/314D	LM2935
Automotive Voltage Regulator	Provides load response control, duty cycle limiting, under/overvoltage and phase detection, high side MOSFET field control, voltage regulation in 12 V alternator systems.	DW/751D	MC33092
Low Dropout Voltage Regulator	Positive 5.0 V, 500 mA regulator having on-chip power-up-reset circuit with programmable delay, current limit, and thermal shutdown.	T/314	MC33267

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Electronic Ignition

Function	Features	Suffix Case	Device
Electronic Ignition Circuit	Used in high energy variable dwell electronic ignition systems with variable reluctance sensors. Dwell and spark energy are externally adjustable.	P/626, D/751	MC3334
Flip-Chip Electronic Ignition Circuit	Same as MC3334 — Mirror image die for inverted "bumped" mounting to substrate	Flip-Chip	MCCF3334
Flip-Chip Electronic Ignition Control Chip	Used in high energy electronic ignition systems requiring differential Hall Sensor control. "Bumped" die for inverted mounting to substrate.	Flip-Chip	MCCF33093
Flip-Chip Electronic Ignition Control Circuit	Used in high energy electronic ignition systems requiring single Hall Sensor control. "Bumped" die for inverted mounting to substrate.	Flip-Chip	MCCF33094
Flip-Chip Electronic Ignition Control Circuit	Used in high energy electronic ignition systems requiring single Hall Sensor control. Dwell feedback for coil variation. "Bumped" die for inverted mounting to substrate.	Flip-Chip	MCCF79076

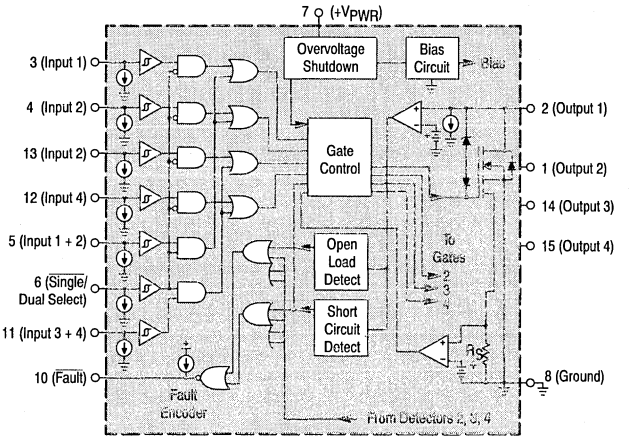
Special Functions

Function	Features	Suffix/ Case	Device
Low Side Protected Switch	Single automotive low side switch having CMOS compatible input, 1.0 A maximum rating, with overcurrent, overvoltage, and thermal protection.	T/221, T-1/314D, DW/751G	MC3392
High Side Driver Switch	Drives loads from positive side of power supply and protects against high voltage transients.	T/314D	MC3399
High Side TMOS Driver	Designed to drive and protect N-channel power MOSFETs used in high side switching applications. Has internal charge pump, externally programmed timer, and fault reporting.	P/626, D/751	MC33091
Mi-Bus Interface Stepper Motor Controller	High noise immunity serial communication using Mi-Bus protocol to control relay drivers and motors in harsh environments. Four phase signals drive two phase motors in either half or full-step modes.	DW/751G	MC33192
Quad Fuel Injector Driver	Four low side switches with parallel CMOS compatible input control, $\leq$ 7.0 mA quiescent current, 0.25 Ω $r_{ds(ON)}$ at 25°C independent outputs with 3.0 A current limiting and internal 65 V clamps.	T/821C-02	MC33293
Quad Fuel Injector Driver	Four low side switches with parallel CMOS compatible input control, $\leq$ 5.0 mA quiescent current, 0.7 Ω $r_{ds(ON)}$ at 25°C independent outputs with 3.0 A current limiting and internal 65 V clamps.	T/821C-02	MC33295
Octal Serial Output Switch	Eight low side switches having 8-bit serial CMOS compatible input control, serial fault reporting, $\leq$ 4.0 mA quiescent current, independent 0.45 Ω $r_{ds(ON)}$ at 25°C outputs with 3.0 A minimum current limiting and internal 55 V clamps.	P/738	MC33298
Integral Alternator Regulator	Control device used in conjunction with an MCCF33096 Darlington companion device to monitor and control the field current in alternator charging systems. "Bumped" die for inverted mounting to substrate.	Flip-Chip	MCCF33095
Darlington Drive Chip	Darlington companion device for MC33095 used to control the field current in alternator charging systems. "Bumped" die for inverted mounting to substrate.	Flip-Chip	MCCF33096
Peripheral Clamping Array	Protects up to six MPU I/O lines against voltage transients.	D/751	TCF6000
Automotive Direction Indicator	Detects defective lamps and protects against overvoltage and short circuit hazards in automotive turn-signal applications. Replaces UAA1041 with improved noise immunity.	P/626, D/751	UAA1041B

Quad Fuel Injector Driver

MC33293T T_J = –40° to +150°C, Case 821C

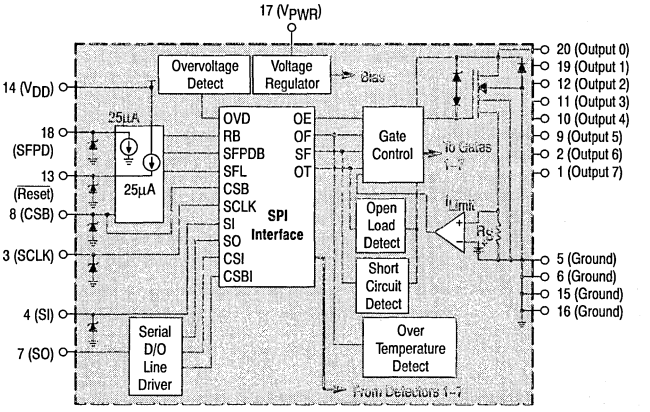
The MC33293T is a monolithic quad low-side switching device having CMOS logic, bipolar/CMOS analog circuitry, and DMOS power FETs. All inputs are CMOS compatible. Each independent output is internally clamped to 65 V, current limited to ≥ 3.0 A, and has an $r_{ds(on)}$ of ≤ 0.25 Ω with V_{PWR} ≥ 9.0 V and may be paralleled to lower $r_{ds(on)}$. $\overline{\text{Fault}}$ output reports existence of open loads (outputs On or Off), shorted loads, and over temperature condition of outputs. A shorted load condition will shut off only the specific output involved while allowing other outputs to operate normally. An overvoltage condition will shut off all outputs for the overvoltage duration. A single/dual mode select pin allows either independent input/output operation or paired output operation.



Octal Serial Switch

MC33298P T_J = –40° to +150°C, Case 738

The MC33298P is a monolithic eight output low-side switch with 8-bit serial input control. Incorporates CMOS logic, bipolar/CMOS analog circuitry, and DMOS power FETs. All inputs are CMOS compatible. It is designed to interface to a microcontroller and switch inductive or incandescent loads. Each independent output is internally clamped to 55 V, current limited to ≥ 3.0 A, and has an $r_{ds(on)}$ of ≤ 0.45 Ω with V_{PWR} ≥ 9.0 V. This device has low standby current, cascadable fault status reporting, output diagnostics, and shutdown for each output.



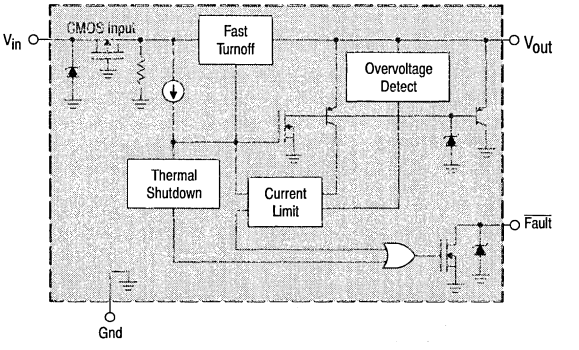
10

Low Side Protected Switch

MC3392T, T-1,DW

T_J = –40° to +150°C, Case 221A, 314D, 751G

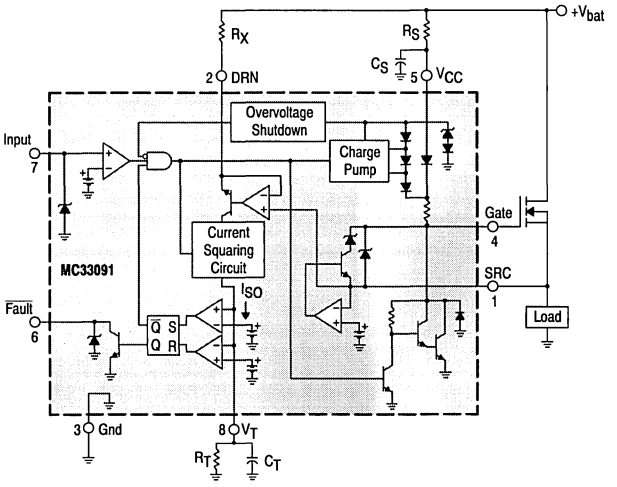
Single low side protected switch with fault reporting capability. Input is CMOS compatible. Output is short circuit protected to 1.0 A minimum with a unique current fold-back feature. Device has internal output clamp for driving inductive loads with over current, overvoltage, and thermal protection. When driving a moderate load, the MC3392 performs as an extremely high gain, low saturation Darlington transistor having a CMOS input characteristic with added protection features. In some applications, the three terminal version can replace industry standard TIP100/101 NPN power Darlington transistors.



High Side TMOS Driver

MC33091P, D T_J = –40° to +150°C, Case 626, 751

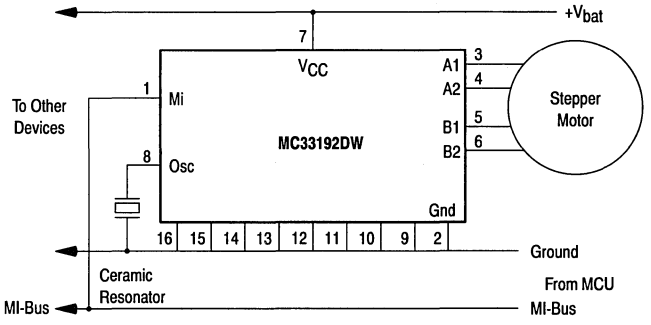
Offers an economical solution to drive and protect N-channel power TMOS devices used in high side switching configurations. Unique device monitors load resulting V_{DS}. TMOS voltage to produce a proportional current used to drive an externally programmed over current timer circuit to protect the TMOS device from shorted load conditions. Timer can be programmed to accommodate driving incandescent loads. Few external components required to drive a wide variety of N-channel TMOS devices. A $\overline{\text{Fault}}$ output is made available through the use of an open collector NPN transistor requiring a single pull-up resistor for operation. Input is CMOS compatible. Device uses ≤ 3.0 µA standby current and has an internal charge pump requiring no external components for operation.



Mi-Bus Interface Stepper Motor Controller

MC33192DW T_J = –40° to +100°C, Case 751G

Intended to control loads in harsh automotive environments using a serial communication bus. Can provide satisfactory real time control of up to eight stepper motors using Mi-Bus protocol. Use of Mi-Bus offers a noise immune system solution for difficult applications involving relays and motors. The stepper motor controller provides four phase signals to drive two phase motors in either half of full-step modes. Designed to interface to a microprocessor with minimal amount of wiring, affording an economical and versatile system.

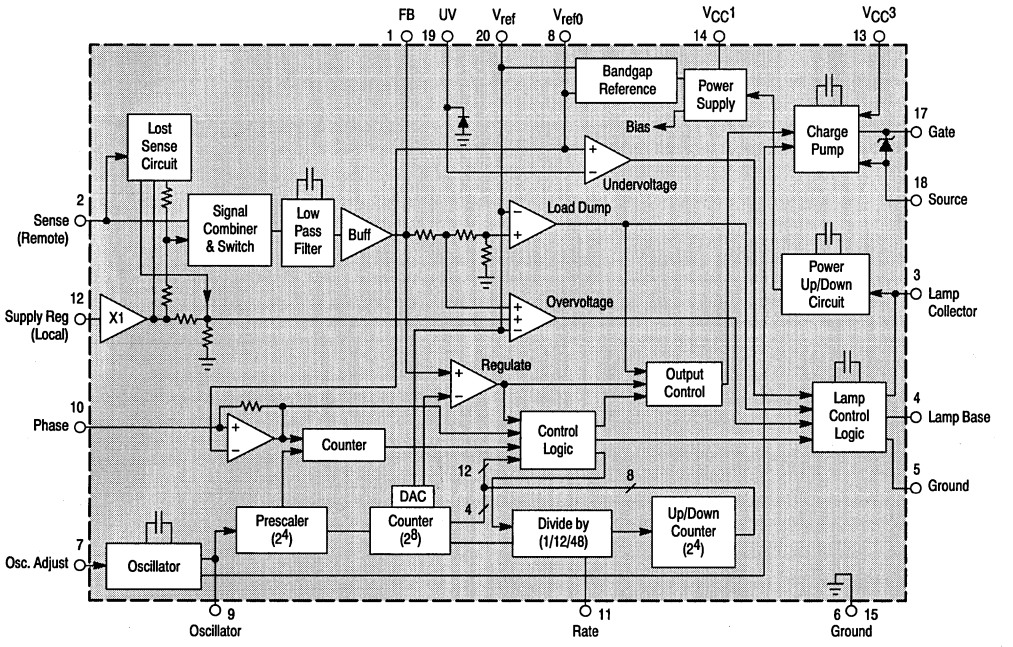


10

Alternator Voltage Regulator

MC33092DW T_J = –40° to +125°C, Case 751D

Provides voltage regulation and load response control in diode rectified 12 V alternator charging systems. Provides externally programmed load response control of the alternator output current to eliminate engine speed hunting and vibration due to sudden electrical loads. Monitors and compares the system battery voltage to an externally programmed set point value and pulse width modulates an N-channel MOSFET transistor to control the average alternator field current. In addition, has duty cycle limiting, under/overvoltage and phase detection (broken belt) protective features.



10

Voltage Regulators

Electronic Ignition

Special Functions

MC3325

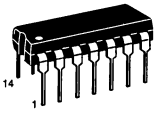
AUTOMOTIVE VOLTAGE REGULATOR

SILICON MONOLITHIC INTEGRATED CIRCUIT

Automotive Voltage Regulator

This device is designed for use in conjunction with an NPN Darlington transistor in a floating field alternator charging system.

- Overvoltage Protection
- Shut-Down on Loss of Battery Sense
- Selectable Temperature Coefficient
- Available in Chip Form for Hybrid Assembly

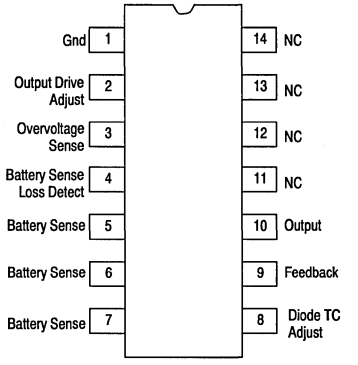


P SUFFIX
PLASTIC PACKAGE
CASE 646

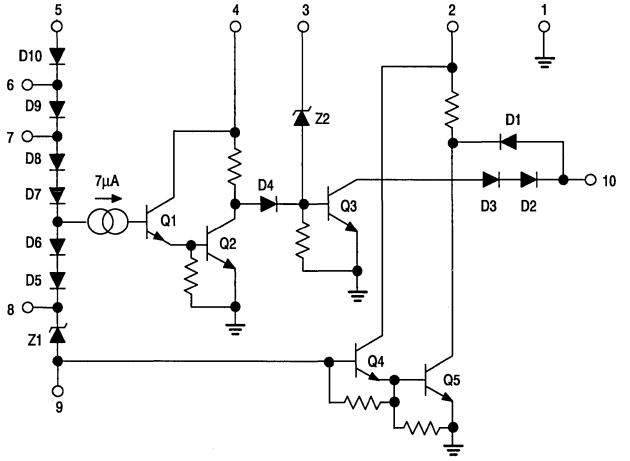
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Current Into: Pins 5, 6, and 7	I_5, I_6, or I_7	50	mA
Pin 3	I_3	20	
Pin 4	I_4	20	
Pin 2	I_2	120	
Pin 8	I_8	50	
Pin 9	I_9	50	
Pin 10	I_{10}	50	
Junction Temperature	T_J	150	°C
Operating Temperature Range	T_A	–40 to +85	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

PIN CONNECTIONS



Circuit Schematic



ORDERING INFORMATION

Device	Temperature Range	Package
MC3325P	–40° to +85°C	Plastic DIP

10

ELECTRICAL CHARACTERICISTICS (T_A = 25°C, unless otherwise noted.)

Characteristics	Figure	Symbol	Min	Max	Unit
Diode TC Adjust: Threshold Voltage on Pin 8	1	V_8	7.9	8.95	V
Battery Sense	1				V
Threshold Voltage on Pin 5		V_5	11.8	13.45	
Threshold Voltage on Pin 6		V_6	11.1	12.75	
Threshold Voltage on Pin 7		V_7	10.5	11.9	
Battery Sense Loss Detect	2				
Threshold Current Into Pin 4		I_4	—	600	μA
Threshold Voltage at Pin 4 ($I_4 \leq 400$ μA)		V_4	1.3	1.7	V
Overvoltage Sense	2				
Threshold Current Into Pin 3		I_3	—	600	μA
Threshold Voltage at Pin 3 ($I_3 \leq 400$ μA)		V_3	6.7	9.0	V
Output Drive Adjust Voltage Drop from Pin 2 to Pin 10 (I_2 = 10 mA)	3	V_2	1.9	2.4	V
Low State Output Voltage at Pin 10 (I_3 = 12 mA, I_2 = 120 mA)	4	V_{10}	—	0.7	V

Test Circuits

Figure 1

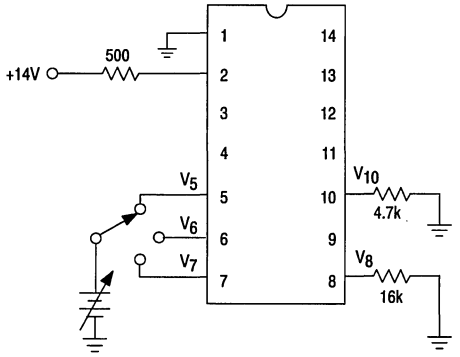


Figure 2

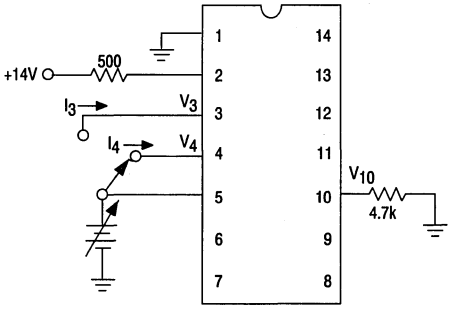


Figure 3

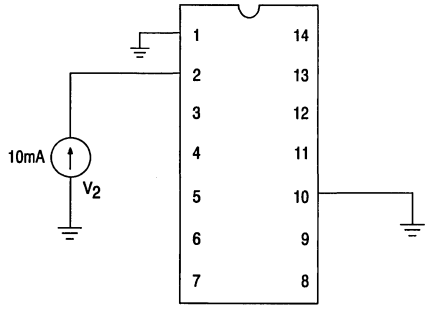
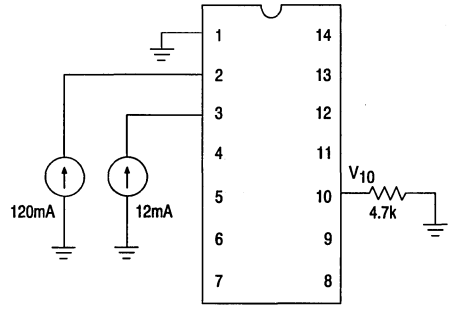


Figure 4



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Applications Circuit Information

R1 — Determines the temperature coefficient by setting the value of current in the diode string. As the value of R1 decreases, so does the effective TC. R1 should be chosen so that the current in the diode string is between 0.5 mA and 1.0 mA.

R2 — This resistor determines the output drive current. Refer to specifications for the darlington driver and select the value for R2 that will provide enough drive to the output when the diode trio voltage is at a minimum.

$$I_{Drive} \cong \frac{V_{min} - 2.8\ V}{R2 + 50\ \Omega}$$

R3 — Used as a current limiting resistor on Pin 3 in case of overvoltage at the diode trio. Voltage at Pin 3 will run approximately 7.5 V. R3 should be chosen so that the current (I_3) at maximum overvoltage is between 2.0 mA and 6.0 mA.

R4 — Used as a current limiting resistor on Pin 4 in case of an open battery voltage sense load.

R5 — This resistor determines the V_{Reg} voltage as defined by the following equation:

$$V_{Reg} = \left(1 + \frac{R5}{R1}\right) 8.4 + \left(n + \frac{R5}{5.0\ k}\right) \quad (0.7)$$

n = number of diodes used in diode string, ($4 \le n \le 6$)

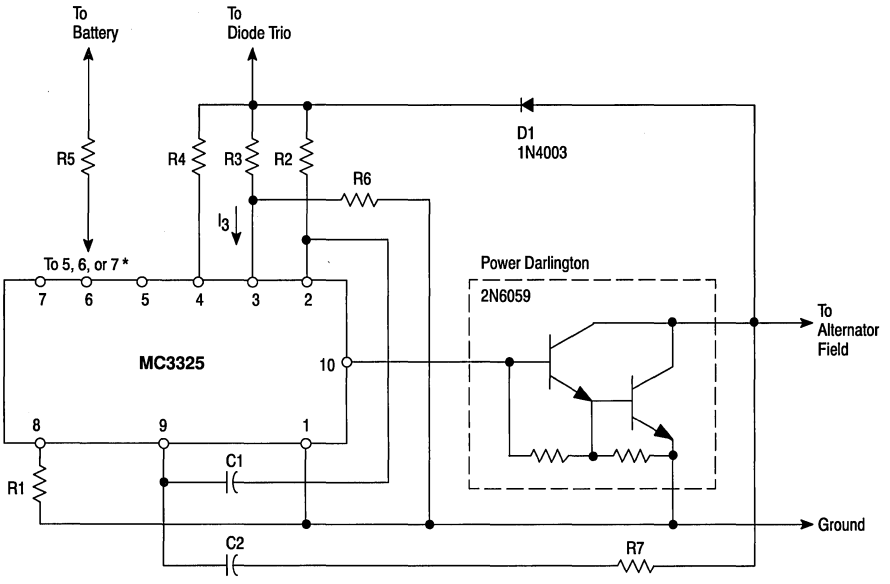
R6 — This resistor in conjunction with R3 is used to set the threshold of overvoltage action.

$$\text{Threshold} \cong \frac{R3 + R6}{R6} \quad (7.5)$$

R7 — Used for compensation (approximately 3.0 kΩ).

C1, C2 — Used for compensation (approximately 0.01 µF).

Figure 5. Application Circuit



*NOTE: The temperature coefficient of the battery voltage sense terminal is determined by the number of diodes used in the diode string (i.e., whether Pin 5, 6, or 7 is used). The approximate temperature coefficient for a diode at 1.0 mA is –2.0 mV/°C, and for a zener diode it is +3.0 mV/°C. Counting from ground (see circuit schematic) we have –2.0 mV for Q5, –2.0 mV for Q4, +3.0 mV for Z1, –8.0 mV for D5 thru D8, and an additional –2.0 mV each for D9 and D10 if used. The total temperature coefficient can be varied from approximately –9.0 mV/°C to –13 mV/°C depending on the number of the diodes in the diode string that are utilized.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC3334
MCC3334
MCCF3334

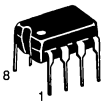
High Energy Ignition Circuit

This device is designed to use the signal from a reluctor type ignition pickup to produce a well controlled output from a power Darlington output transistor.

- Very Low Peripheral Component Count
- No Critical System Resistors
- Wide Supply Voltage Operating Range (4.0 V to 24 V)
- Overvoltage Shutdown (30 V)
- Dwell Automatically Adjusts to Produce Optimum Stored Energy without Waste
- Externally Adjustable Peak Current
- Available in Chip and Flip-Chip Form
- Transient Protected Inputs and Outputs

HIGH ENERGY IGNITION CIRCUIT

SILICON MONOLITHIC INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 626

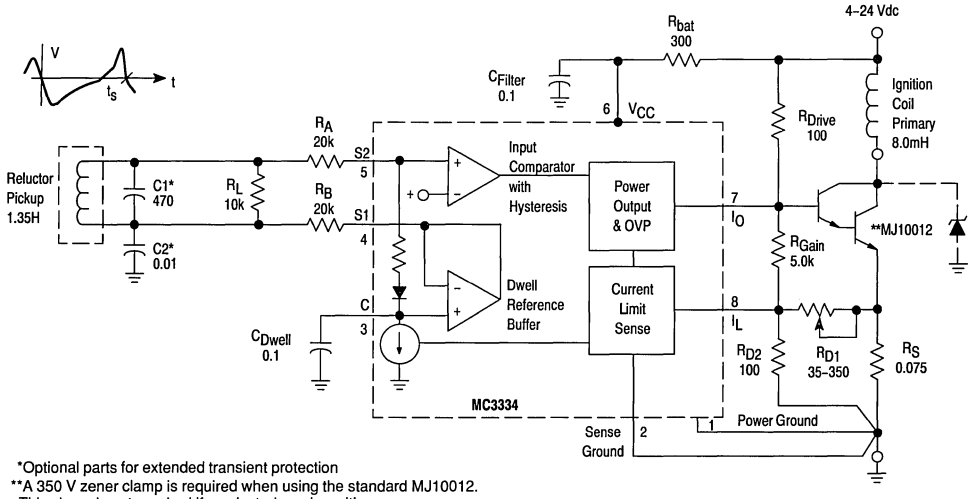
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage—Steady State Transient 300 ms or less	V_{bat}	24 90	V
Output Sink Current—Steady State Transient 300 ms or less	$I_{O(Sink)}$	300 1.0	mA A
Junction Temperature	$T_{J(max)}$	150	°C
Operating Temperature Range	T_A	–40 to +125	°C
Storage Temperature Range	Tstg	–65 to +150	°C
Power Dissipation, Plastic Package, Case 626 Derate above 25°C	P_D	1.25 10	W mW/°C

ORDERING INFORMATION

Device	Temperature Range	Package
MC3324P	–40° to +125°C	Plastic DIP
MCC3334		Chip
MCCF3334		Flip-Chip

Figure 1. Block Diagram and Typical Application



*Optional parts for extended transient protection
**A 350 V zener clamp is required when using the standard MJ10012. This clamp is not required if a selected version with $V_{CEO(sus)} \geq 550$ V is used.

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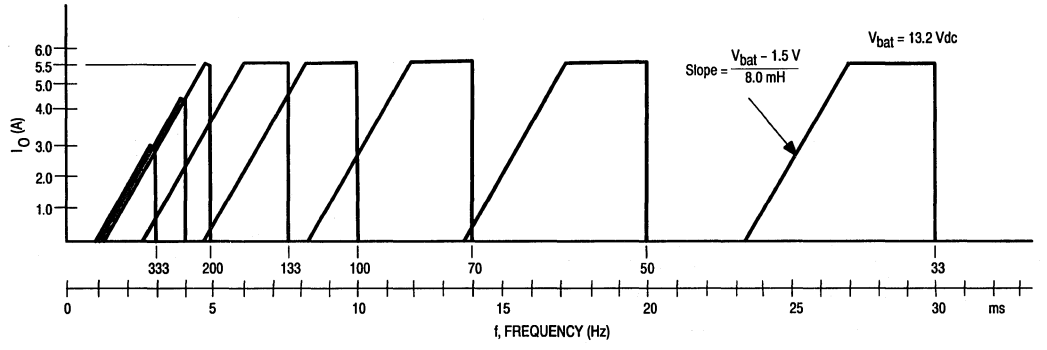
ELECTRICAL CHARACTERICISTICS (T_A = –40° to +125°C, V_{bat} = 13.2 Vdc, circuit of Figure 1, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Internal Supply Voltage, Pin 6	V_{CC}				Vdc
V_{bat}= 4.0 Vdc		—	3.5	—	
8.0 Vdc		—	7.2	—	
12.0		—	10.4	—	
14.0		—	11.8	—	
Ignition Coil Current Peak, Cranking RPM 2.0 Hz to 27 Hz	$I_{o(pk)}$				A pk
V_{bat} = 4.0 Vdc		3.0	3.4	—	
6.0		4.0	5.2	—	
8.0		4.6	5.3	—	
10.0		5.1	5.4	—	
Ignition Coil Current Peak, Normal RPM	$I_{o(pk)}$				A pk
Frequency = 33 Hz		5.1	5.5	—	
133 Hz		5.1	5.5	—	
200 Hz		4.2	5.4	—	
267 Hz		3.4	4.4	—	
333 Hz		2.7	3.4		
Ignition Coil On-Time, Normal RPM Range	t_{on}				ms
Frequency= 33 Hz		—	7.5	14.0	
133 Hz		—	5.0	5.9	
200 Hz		—	4.0	4.6	
267 Hz		—	3.0	3.6	
333 Hz		—	2.3	2.8	
Shutdown Voltage	V_{bat}	25	30	35	Vdc
Input Threshold (Static Test)	V_{S2}–V_{S1}				mVdc
Turn-on		—	360	—	
Turn-off		—	90	—	
Input Threshold Hysteresis	V_{S2}–V_{S1}	75	—	—	mVdc
Input Threshold (Active Operation)	V_{S2}				Vdc
Turn-on		—	1.8	—	
Turn-off		—	1.5	—	
Total Circuit Lag from t_S (Figure 1) until Ignition Coil Current Falls to 10%		—	60	120	µs
Ignition Coil Current Fall Time (90% to 10%)		—	4.0	—	µs
Saturation Voltage IC Output (Pin 7) (R_{DRIVE} = 100 Ω)	$V_{CE(sat)}$				mVdc
V_{bat} = 10 Vdc		—	120	—	
30 Vdc		—	280	—	
50 Vdc		—	540	—	
Current Limit Reference, Pin 8	V_{ref}	120	160	190	mVdc

Figure 2. Ignition Coil Current versus Frequency/Period



CIRCUIT DESCRIPTION

The MC3334 high energy ignition circuit was designed to serve aftermarket Delco five terminal ignition applications. This device, driving a high voltage Darlington transistor, offers an ignition system which optimizes spark energy at minimum power dissipation. The IC is pinned out to permit thick film or printed circuit module design without any crossovers.

The basic function of an ignition circuit is to permit build-up of current in the primary of a spark coil, and then to interrupt the flow at the proper firing time. The resulting flyback action in the ignition coil induces the required high secondary voltage needed for the spark. In the simplest systems, fixed dwell angle produces a fixed duty cycle, which can result in too little stored energy at high RPM, and/or wasted power at low RPM. The MC3334 uses a variable DC voltage reference, stored on C_{Dwell}, and buffered to the bottom end of the reluctor pickup (S1) to vary the duty cycle at the spark coil. At high RPM, the MC3334 holds the output "off" for approximately 1.0 ms to permit full energy discharge from the previous spark; then it switches the output Darlington transistor into full saturation. The current ramps up at a slope dictated by V_{bat} and the coil L. At very high RPM the peak current may be less than desired, but it is limited by the coil itself.

As the RPM decreases, the ignition coil current builds up and would be limited only by series resistance losses. The MC3334 provides adjustable peak current regulation sensed by R_S and set by R_{D1}, in this case at 5.5 A, as shown in Figure 2. As the RPM decreases further, the coil current is held at 5.5 A for a short period. This provides a reserve for sudden acceleration, when discharge may suddenly occur earlier than expected. The peak hold period is about 20% at medium RPM, decreasing to about 10% at very low RPM. (Note: 333 Hz = 5000 RPM for an eight cylinder four stroke engine.) At lower V_{bat}, the "on" period automatically stretches to accommodate the slower current build-up. At very low V_{bat} and low RPM, a common condition during cold starting, the "on" period is nearly the full cycle to permit as much coil current as possible.

The output stage of the IC is designed with an OVP circuit which turns it on at $V_{bat} \approx 30$ V ($V_{CC} \approx 22$ V), holding the output Darlington off. This protects the IC and the Darlington from damage due to load dump or other causes of excessive V_{bat}.

Component Values

Pickup — series resistance = 800 Ω ± 10% @ 25°C
inductance = 1.35 H @ 1.0 kHz @ 15 Vrms

Coil — leakage L = 0.6 mH
primary R = 0.43 Ω ± 5% @ 25°C
primary L = 7.5 mH to 8.5 mH @ 5.0 A

R_L — load resistor for pickup = 10 kΩ ± 20%

R_A, R_B — input buffer resistors provide additional transient protection to the already clamped inputs = 20 k ± 20%

C1, C2 — for reduction of high frequency noise and spark transients induced in pick-up and leads; optional and non-critical

R_{bat} — provides load dump protection (but small enough to allow operation at V_{bat} = 4.0 V) = 300 Ω ± 20%

C_{Filter} — transient filter on V_{CC}, non-critical

C_{Dwell} — stores reference, circuit designed for 0.1 µF ± 20%

R_{Gain} — R_{Gain}/R_{D1} sets the DC gain of the current regulator = 5.0 k ± 20%

R_{D2} — R_{D2}/R_{D1} set up voltage feedback from R_S

R_S — sense resistor (PdAg in thick film techniques) = 0.075 Ω ± 30%

R_{Drive} — low enough to supply drive to the output Darlington, high enough to keep $V_{CE(sat)}$ of the IC below Darlington turn-on during load dump = 100 Ω ± 20%, 5.0 W

R_{D1} — starting with 35 Ω assures less than 5.5 A, increasing as required to set 5.5 A

$$R_{D1} = \frac{I_{o(pk)}\, R_S - V_{ref}}{\frac{V_{ref}}{R_{D2}} - \frac{1.4}{R_{Gain}}} - \approx 100\ \Omega\ (\text{nom})$$

General Layout Notes

The major concern in the substrate design should be to reduce ground resistance problems. The first area of concern is the metallization resistance in the power ground to module ground and the output to the R_{drive} resistor. This resistance directly adds to the $V_{CE(sat)}$ of the IC power device and if not minimized could cause failure in load dump. The second concern is to reference the sense ground as close to the ground end of the sense resistor as possible in order to further remove the sensitivity of ignition coil current to ground I.R. drops.

All versions were designed to provide the same pin-out order viewed from the top (component side) of the board or substrate. This was done to eliminate conductor cross-overs. The standard MC3334 plastic device is numbered in the industry convention, counter-clockwise viewed from the top, or bonding pad side. The MCCF3334 "flip" or "bump" chip is made from reversed artwork, so it is numbered clockwise viewed from its bump side. Since this chip is mounted face down, the resulting assembly still has the same counter-clockwise order viewed from above the component surface. All chips have the same size and bonding pad spacing. See Figure 4 for dimensions.

Figure 3. Internal Schematic

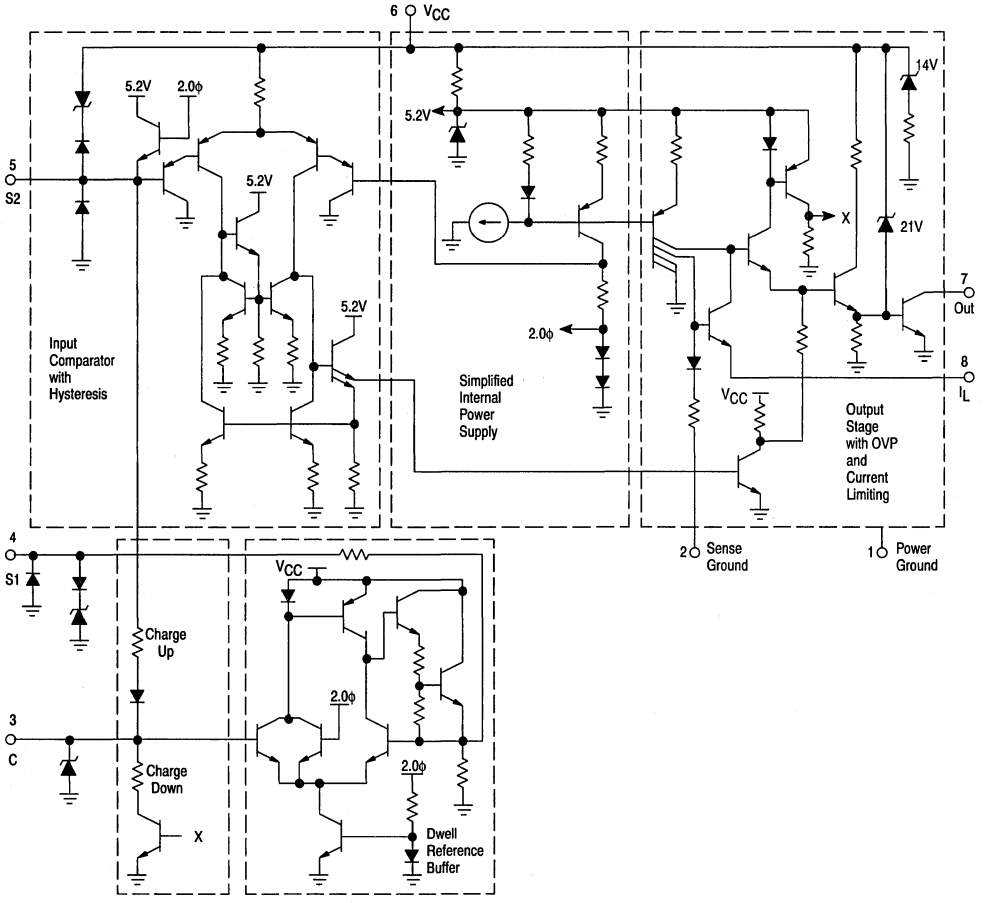


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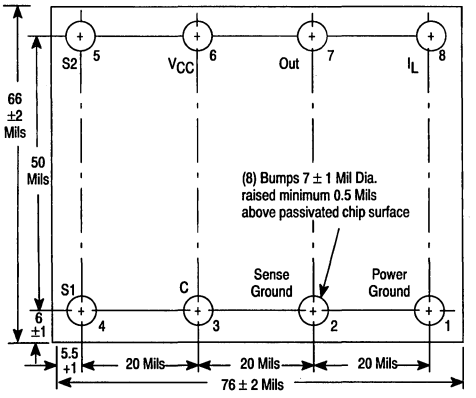
Figure 4. MCCF3334 Ignition Circuit Bump Side View



MC3391

Advance Information

Low Side Protected Switch

LOW SIDE PROTECTED SWITCH

SILICON MONOLITHIC INTEGRATED CIRCUIT

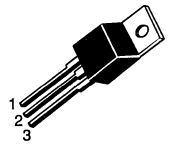
The MC3391 is a low side protected switch designed for use in harsh automotive applications which require the capability of handling high voltages attributed to load and field dump transients, in addition to reverse and double battery conditions. The three terminal TO-220 is intended to replace power Darlington transistors in new and existing switching applications when taking into account the CMOS input levels required by the MC3391. It offers improved functionality and ruggedness over power Darlingtons while retaining the same package and pin configuration, and can be used as a replacement in many applications using the industry standard TIP100/101 NPN power Darlington transistor.

The five terminal TO-220 has the added feature of having a $\overline{\text{Fault}}$ output (active low) which will indicate the existence of an over temperature, over voltage or current limit condition, including an output short to ground, or open load.

When driving a moderate load, the MC3391 performs as an extremely high gain, low saturation Darlington transistor having CMOS input levels. The primary advantage of the MC3391 over a Darlington transistor is the additional protection afforded the device and loads when driving difficult or faulty loads. This device incorporates unique internal current limit and thermal protection circuitry to safeguard itself and the associated load from catastrophic failure.

The MC3391 is available in a three and five-lead TO-220 package; the five-lead having the added diagnostic feature. The full featured MC3391 is also available in a 16 pin wide body SOIC plastic power package.

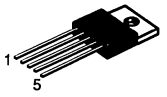
- Designed for Automotive Applications
- Can Be Used as a Replacement for TIP100/101 NPN Power Darlingtons
- Drives Inductive Loads without External Clamp Circuitry
- Withstands High Negative and Positive Transient Voltages
- Low ON Voltage
- CMOS Logic Compatible Input
- Over Current, Over Voltage, and Thermal Protection
- Extended Operating Temperature Range
- $\overline{\text{Fault}}$ Output



T SUFFIX
PLASTIC PACKAGE
CASE 221A
(TO-220)

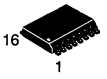
PIN 1. Input
2. Output
3. Ground

Heatsink surface connected to Pin 3 in TO-220 Package



T-1 SUFFIX
PLASTIC PACKAGE
CASE 314D
(TO-220)

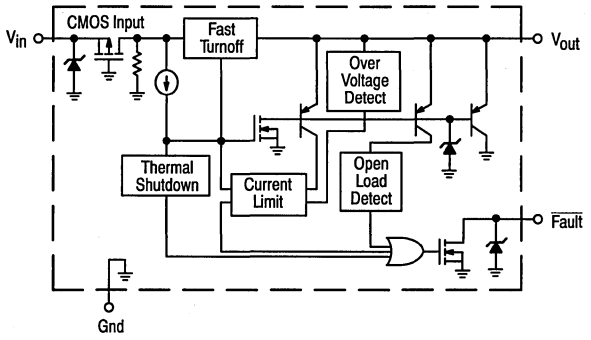
PIN 1. Input
2. $\overline{\text{Fault}}$
3. Ground
4. NC
5. Output



DW SUFFIX
PLASTIC PACKAGE
CASE 751G
(SOP-8+8L)

PIN 1. NC
2. NC
3. NC
4. Output
5. Input
6. $\overline{\text{Fault}}$
7. NC
8. NC
9–16. Ground

Simplified Block Diagram



ORDERING INFORMATION

Device	Ambient Temperature Range	Package
MC3391T	– 40° to +125°C	Plastic Power
MC3391T-1		Plastic Power
MC3391DW		SOP-8+8L

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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage Range	V_{in}	–0.5 to +6.5	V
Output Transient Breakdown Voltage — Forward — Reverse	V_{BF} V_{BR}	+60 –80	V
Short Circuit Current	I_{SC}	2.0	A
Output Avalanche Energy	E_{max}	60	mJ
Minimum ESD Voltage Capability (Note 1)	ESD	2000	V
Operating Junction Temperature Internally Limited (Note 2)	T_J	150	°C
Storage Temperature	T_{stg}	–65 to +150	°C
Operating Ambient Temperature Range	T_A	–40 to +125	°C
Thermal Resistance (Notes 3, 4) TO-220 — Junction to Ambient — Junction to Case SOIC — Junction to Ambient — Junction to Case	 θ_{JA} θ_{JC} θ_{JA} θ_{JC}	 62.5 2.5 118 59	°C/W

ELECTRICAL CHARACTERISTICS (LImit values are noted under conditions: –40°C ≤ T_A ≤ +125°C, 'Typical' denotes calculated mean value derived from 25°C parametric data, unless otherwise noted.)

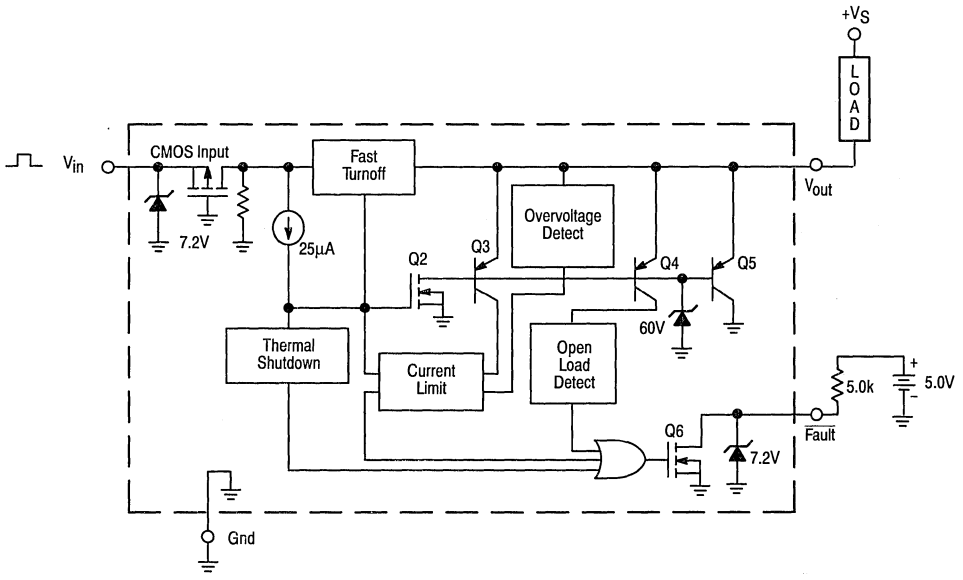
Characteristics	Figure	Symbol	Min	Typ	Max	Unit
Input Control Current V_{in} = 1.0 V V_{in} = 4.0 V V_{in} = 5.0 V	3	I_{in}	 — — —	 0.2 230 260	 10 350 500	µA
Input Voltage High (ON) Input Voltage Low (OFF)	7	V_{IH} V_{IL}	4.0 —	2.0 2.0	— 1.0	V
Output Leakage Current $+V_S$ = 28 V, R_L = 0	4	I_L	—	1.3	100	
Output Short Circuit Current $+V_S$ = 14 V, R_L = 0	5	I_{SC}	1.0	1.3	2.2	A
Output ON Voltage (V_{in} = 4.0 V, Note 5) I_O = 400 mA I_O = 800 mA	6	V_{OL}	 — —	 0.95 1.1	 1.1 1.8	V
Output Clamp Voltage I_O = 100 mA	8	V_{OC}	60	70	80	V
Reverse Leakage Current V_O = –13 V	9	I_{BR}	—	–10	–30	nA
Fault Output Sink Saturation (I_{sink} = 100 µA, V_{in} = 5.0 V)	10	$V_{DS(sat)}$	—	0.3	0.4	V
Fault Output Off-State Leakage (V_{DS} = 5.0 V)		$I_{DS(peak)}$	—	0.6	100	µA
Turn-On Time 10% to 90% of I_O (400 mA nominal) Turn-Off Time 90% to 10% of I_O (400 mA nominal) Propagation Delay Time (Turn-on, Turn-off)	11 12 —	t_r t_f t_d	 — — —	 3.3 9.7 3.0	 20 25 10	µs

NOTES: 1. ESD testing performed in accordance with Human Body Model (C_{Zap} = 100 pF, R_{Zap} = 1500 Ω).
2. This device incorporates internal circuit techniques which do not allow the internal junction temperature to reach destructive temperatures.
3. The thermal resistance case is considered to be a point located near the center of the tab and plastic body of the TO-220 or a point on one of the heatsink leads (Pins 9 to 16) of the SOIC.
4. The SOIC thermal information is based on simulation data.
5. I_O is defined as the output sink current.

PIN DESCRIPTION

Name	Pin Number			Description
	Case 221A	Case 314D	SOIC	
V_{in}	1	1	5	CMOS compatible input.
V_{out}	2	5	4	Output to load and battery, protected by a 60 V clamp against inductive load transients.
Gnd	3	3	9 to 16	Ground connection.
$\overline{Fault}$	N/A	2	6	Fault output pulled low when the IC is operating in a fault state. The open drain output requires a pull-up resistor for normal operation.

Figure 1. MC3391 Representative Block Diagram



Definition of Currents and Voltages. Positive current flow is defined as conventional current flow into the device. Negative current flow is defined as current flow out of the device. All voltages are referenced to ground. Both currents and voltages are specified as absolute (i.e., –10 V is greater than –1.0 V).

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Figure 2. Fault Output Timing Diagram

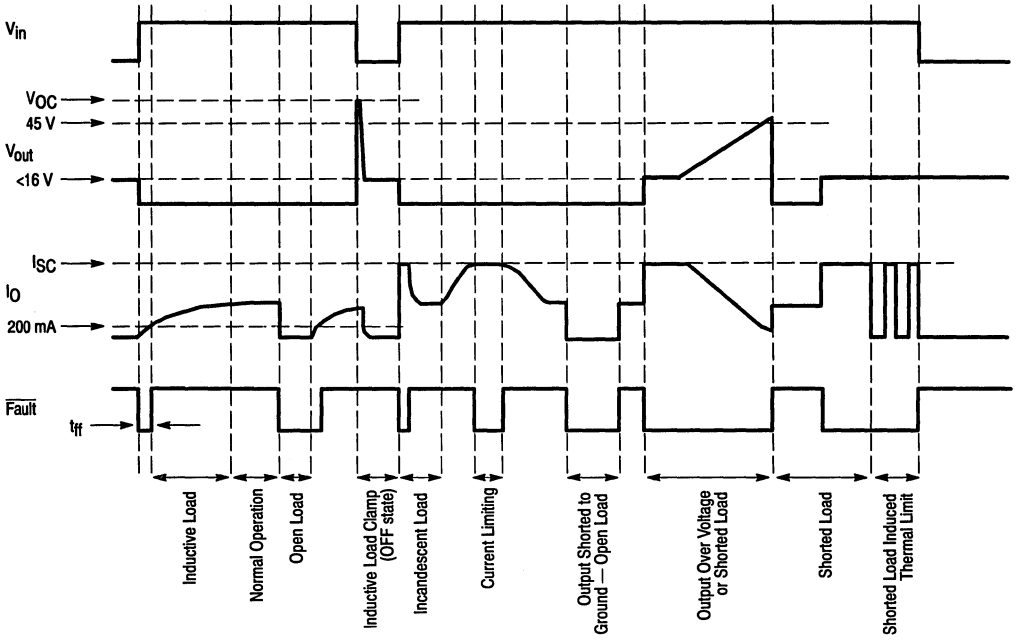

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Figure 3. Input Control Current versus Input Voltage

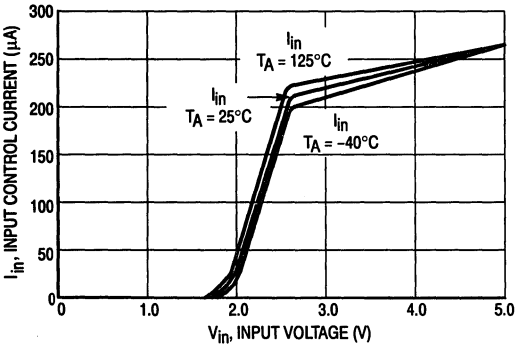

Figure 4. Output Leakage Current versus Temperature

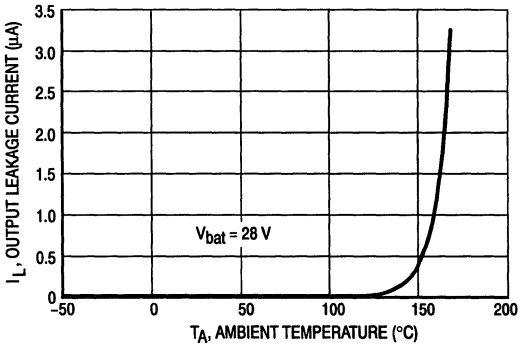

Figure 5. Output Short Circuit Current versus Temperature

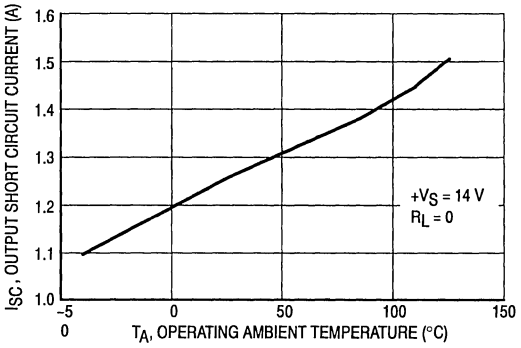

Figure 6. Output On Voltage versus Temperature

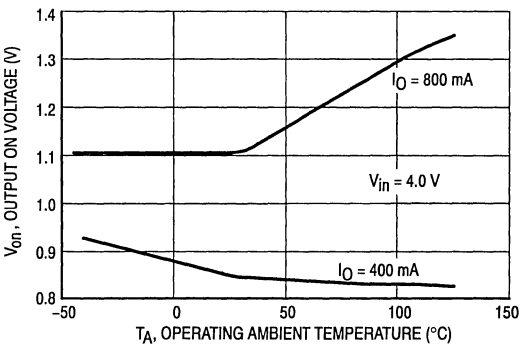

Figure 7. Input Voltage versus Temperature

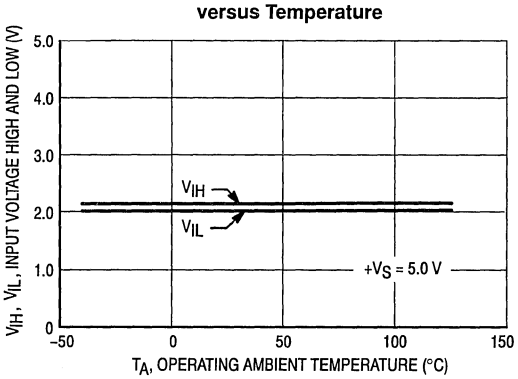

Figure 8. Output Clamp Voltage versus Temperature

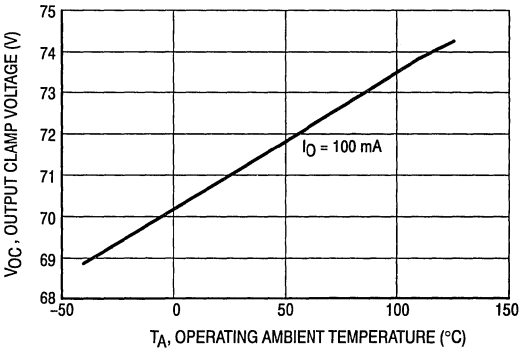

Figure 9. Reverse Breakdown Voltage versus Temperature

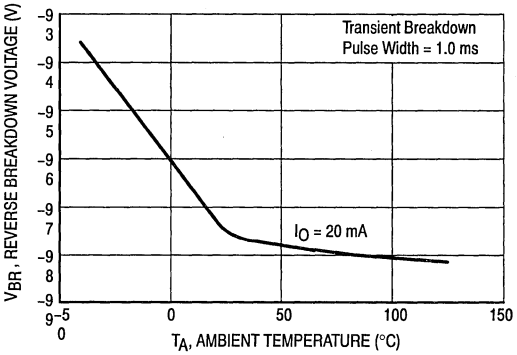

Figure 10. $\overline{\text{Fault}}$ Output Saturation versus Sink Current

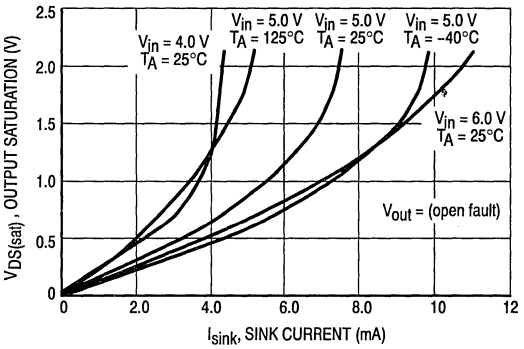

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Figure 11. Turn-On Waveform

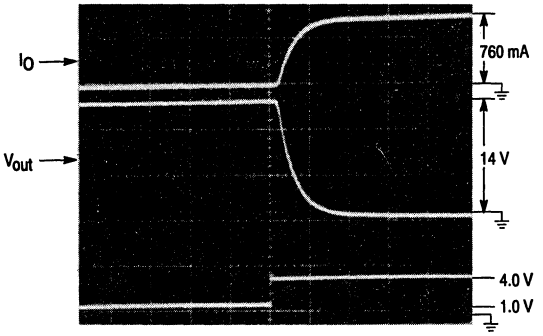

Figure 12. Turn-Off Waveform

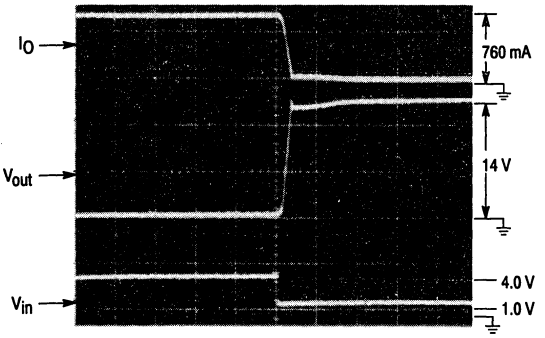

Figure 13. Output Current versus Supply Voltage

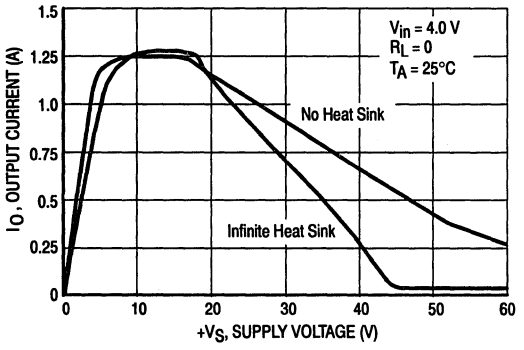

Figure 14. Maximum Load Inductance versus Output Current

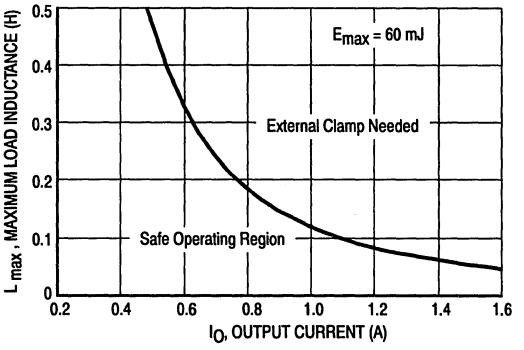

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Figure 15. Load Inductance versus Open False Fault Time

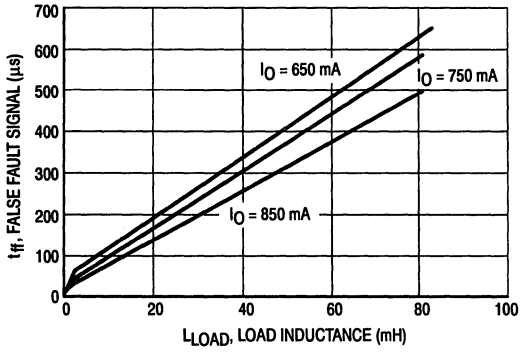
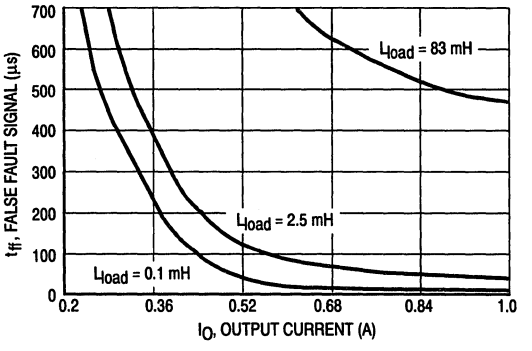


Figure 16. Output Current versus Open False Fault Time



TECHNICAL DISCUSSION

Introduction

The MC3391 is a low side protected switch incorporating many features making it ideal for use in harsh automotive applications. The protection circuitry of the MC3391 protects not only itself but also the associated load from destructive high voltage transients attributed to load and field dump, as well as, reverse and double battery conditions found in automotive applications. The MC3391 is unique in that the protection circuitry is internal and does not require additional external protection components for its operation. This makes the device very cost effective in that its application utilizes few external components, thus reducing cost and space requirements needed for the system. The MC3391 is extremely effective when used to drive solenoids, as well as, incandescent lamp loads. The following description of the device's operation is in reference to the functional blocks of the Representative Block Diagram shown in Figure 1.

CMOS Input

The input of the MC3391 is CMOS compatible. Input control performs as true logic in that when the input (V_{in}) is less than 1.0 V, the MC3391 switch is in a high impedance or OFF state and when V_{in} is greater than 4.0 V the MC3391 is in a low impedance or ON state. The switching threshold of the input is approximately 2.0 V and is graphed in Figure 7. With the input at 4.0 V, the input sink current will be approximately 250 μA. In the ON state, the internal protection circuitry is activated and all of the protection features are available for use. In the OFF state, however, it is important to note that none of the protection features are available, with the exception of the internal inductive load clamp. The input pin is afforded a minimum of 2000 V ESD protection (Human Body Model) by virtue of the 7.2 V zener diode.

Over Temperature Shutdown

Internal Thermal Shutdown Circuitry is provided to protect the MC3391 in the event the Operating Junction Temperature (T_J) exceeds 150°C. Typically, Thermal Shutdown will occur at 160° to 170°C. The Thermal Shutdown sense element is embedded within the output PNP (Q5) so as to afford very fast thermal coupling of Q5 to the sense element. Any rise in temperature due to the ambient is translated directly to Q5 and the sense element. If the junction temperature rises excessively above 150°C, the Thermal Shutdown circuit will turn ON, quickly pulling the gate of Q2 to ground, which pulls the base of Q5 to ground, turning it OFF. In addition, the Thermal Shutdown circuit simultaneously turns Q6 ON and with a suitable pull-up resistor at the $\overline{\text{Fault}}$ pin reports the presence of a fault (logic low). The output PNP will remain OFF until the junction temperature decreases to within the operating range at which time Thermal Shutdown turns OFF, ceasing to hold the gate of Q2 low, turning Q5 back ON. This process will repeat as long as the thermal over load exists. This mode of operation is a nondestructive safety feature of the device and will real time correct itself when the cause of over temperature is removed. A continued over temperature condition will thermally Pulse Width Modulate (PWM) the output and $\overline{\text{Fault}}$ and may be incorrectly interpreted as an oscillating load if one does not consider the simultaneous performance of the $\overline{\text{Fault}}$ pin.

Current Limit

The MC3391 protects itself against V_{out} to $+V_S$ hard shorts as well as any over current conditions by reducing the magnitude of output current (I_O) to that of the short circuit current limit value (I_{SC}). When the output current monitored by Q3 tries to exceed I_{SC}, the Current Limit circuit lowers the gate voltage of Q2, lowering the base of Q5, causing the load current through Q5 to diminish. Simultaneously, when the load current exceeds I_{SC}, Q6 will turn ON reporting a fault condition. If the output current is allowed to remain excessively high for the degree of heat sinking incorporated, and the junction temperature of the device is allowed to heat beyond 150°C, the Thermal Shutdown circuit will activate and the output will thermally PWM. Again, these modes of operation are safety features of the MC3391 and are not destructive.

Overvoltage Detect

This circuitry protects the MC3391 from V_{out} voltages in excess of 16 V by lowering the output current to a nondestructive value. With increasing V_{out} voltage (16 V < V_{out} < 45 V) the load current is reduced to below that of I_{SC} and produces a fold back current effect. As V_{out} increases in excess of 16 V, the output current decreases linearly until V_{out} exceeds 45 V. With an infinite heatsink and V_{out} > 45 V, I_O will be less than 100 mA. For the other extreme, no heatsink and V_{out} > 45 V, I_O can be expected to be less than about 400 mA. This behavior of I_O in relation to V_{out} is shown in Figure 13.

For the infinite heatsink case, the output current initially increases with increased voltage until V_{out} exceeds 16 V, thereafter the behavior is expressed as,

$$I_O = I_{SC}\,[1-(V_{out}-16\text{ V})\,/\,30\text{ V}].$$

Beyond 45 V, I_O is limited to less than 100 mA. Anytime the Overvoltage Detect circuit is activated, the gate of Q6 is pulled low causing Q6 to turn ON to report the fault at the $\overline{\text{Fault}}$ pin.

Inductive Load Clamp

The MC3391 has an internal inductive load clamp for protection against flyback voltages imposed on the output pin in excess of 70 V. The incorporated zener clamp can quickly dissipate up to 60 milli-Joules of inductive flyback energy. Figure 14 shows the maximum inductive load versus load current that the clamp can handle safely. As an example (using Figure 14), if operating the MC3391 to drive a 0.33 H inductor, the maximum load current should be adjusted to 600 mA or less. If the load current is too high for the inductor used, some series resistance can be added to the load to limit the current. If this is not possible, an external clamp must be used to facilitate handling the higher energy. When using an external clamp, the external clamp voltage must be less than 60 V so as to override the internal clamp. The output clamp offers protection for the output when the MC3391 is in the OFF state. During the ON state, other protection features (Overvoltage, Current, and Temperature) are available to protect the output.

Open Load Detect

This protection feature will set $\overline{\text{Fault}}$ logic low whenever I_O, monitored by Q4, is less than 200 mA. When driving inductors, voltage leads the current buildup and as a result a false $\overline{\text{Fault}}$ will be reported during initial turn-on until the load current attains at least 200 mA. The duration of the inductive false $\overline{\text{Fault}}$ (t_{ff}) will be affected by the inductance of the load (Figure 15) and also by the value of I_O (Figure 16). The data for these graphs was taken in a laboratory setup in which each inductive load was connected in series with a 10 Ω power resistor to V_S. The input was a 1.0 kHz, 5.0 V p-p square wave with a 75% high duty cycle.

When driving incandescent lamp loads, in-rush current will cause a false $\overline{\text{Fault}}$ for the duration the in-rush current exceeds I_{SC}. When 200 mA < I_O < I_{SC}, the false $\overline{\text{Fault}}$ will correct itself. The timing of the false $\overline{\text{Fault}}$ can be seen in the timing diagram of Figure 2.

During lab characterization it was noted the $\overline{\text{Fault}}$ output will operate with V_S voltages below 4.0 V but fails to allow full pull-up to the pull-up voltage. This is due to insufficient internal current available to fully turn Q6 off. This is not thought to be a problem since almost all applications use V_S voltages greater than 4.0 V.

$\overline{\text{Fault}}$ Logic

The $\overline{\text{Fault}}$ is comprised of an internal open drain FET requiring an external pull-up resistor. Typically, a 5.0 k pull-up resistor to a +5.0 V supply is satisfactory. The $\overline{\text{Fault}}$ pin is afforded a minimum of 2000 V ESD protection (Human Body Model) by virtue of the 7.2 V zener diode. The $\overline{\text{Fault}}$ will report a fault (logic low state) whenever the MC3391 experiences a fault condition. Conditions producing a fault are: I_O < 200 mA (open load); I_O > 1.3 A (over current/shorted load); T_J > 150°C (over temperature); and V_{out} > 16 V (overvoltage).

If the device goes into Thermal Shutdown, caused by environmental overheating (not resulting from another fault condition), the $\overline{\text{Fault}}$ and V_{out} will thermally PWM as the MC3391 repeatedly heats to shut off, cools, and again turns on. If a current limit fault causes the device to go into Thermal Shutdown, the output will oscillate while the $\overline{\text{Fault}}$ remains pulled low. There is no designed-in thermal hysteresis to control the PWM effect and this fault mode of operation is not destructive.

Fast Turn-Off

This circuitry enhances the MC3391 turn-off performance. Whenever V_{in} goes to a logic low state, V_{out} is held in an OFF state for approximately 15 µs. During fast turn-off, less than 30 mA of current is allowed to flow producing an abrupt turn-off. This turn-off characteristic can be seen in Figure 12, a photograph of the typical turn-off waveform.

APPLICATIONS

Solenoid Driver

The MC3391 can be used to drive a variety of solenoid applications similar to that of Figure 17. For example; driving a solenoid having an inductance of 73.8 mH and a resistance of 95 Ω from a 12 V supply will cause 240 mA of sink current to flow with the MC3391 in the ON state. The resulting current value is within the normal load current operating region and will not produce a fault. Load current is paramount in any design using the MC3391 and must be less than I_{SC} for acceptable operation. If the load current is greater than I_{SC}, a current limit fault state will exist. Operation in this state is not destructive as

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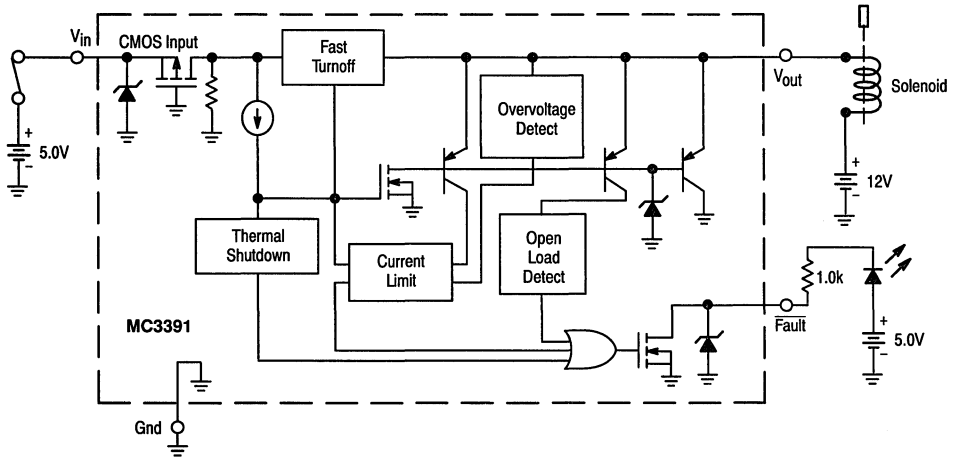
Figure 17. Solenoid Driver



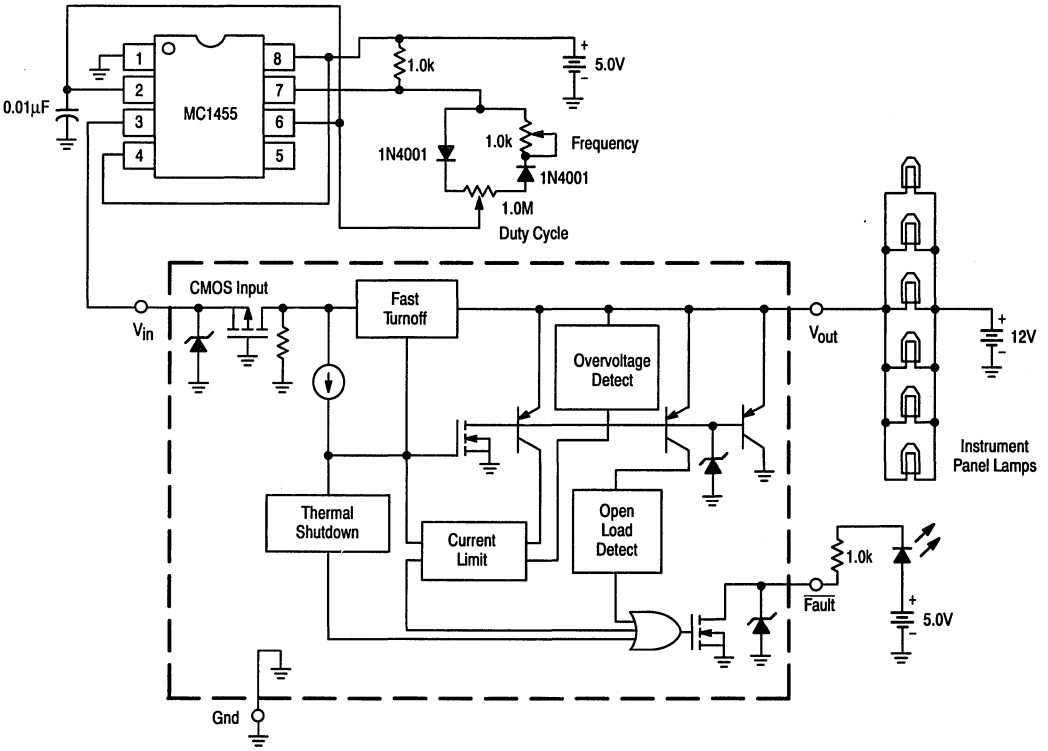
the device will turn off if the Junction Temperature (T_J) rises above 150°C. When the Junction Temperature cools below 150°C the device will again turn-on, with a repeat of the cycle. If the solenoid resistance is exceedingly large so as to cause little load current (less than 200 mA) to flow when ON, an open load fault state will exist. Careful design to acceptable load current limits should be insured for satisfactory operation of an application.

Instrument Panel Lamp Dimmer Control

The MC3391 can be used to control the dimming function associated with instrument panel lamps. The brightness of incandescent lamps can be varied by Pulse Width Modulating the input of the MC3391. The modulating signal for the MC3391 can be obtained directly from a microprocessor or, as in Figure 18, from an MC1455 timer. The MC1455 timer is configured as a free-running clock having both frequency and duty cycle control. The typical timer frequency is approximately 80 Hz when the frequency potentiometer is adjusted to 1.0 k. This frequency was chosen so as to avoid any perceptible lamp flicker. The duty cycle potentiometer controls the duty cycle over a range of approximately 3% to 97%; when at 3% duty cycle, the lamps are essentially off; when at 97% duty cycle, the lamps are essentially full lit. Six incandescent lamps are shown in this application, drawing 720 mA total current. Similar applications can be used to drive a variety of lamp loads. The total load current is the primary factor of consideration when driving lamp loads. The total value of I_O must be less than I_{SC}.

Another convenient aspect of this application is the LED. The LED can be used to denote the existence of a system fault (overvoltage, open load, current limiting, or thermal shutdown).

Figure 18. Instrument Panel Lamp Dimmer Control



MC3392

Advance Information

Low Side Protected Switch

LOW SIDE PROTECTED SWITCH

SILICON MONOLITHIC INTEGRATED CIRCUIT

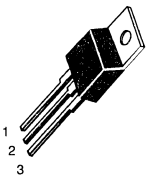
The MC3392 is a low side protected switch designed for use in harsh automotive applications which require the capability of handling high voltages attributed to load and field dump transients, in addition to reverse and double battery conditions. The three terminal TO-220 is intended to replace power Darlington transistors in new and existing switching applications when taking into account the CMOS input levels required by the MC3392. It offers improved functionality and ruggedness over power Darlingtons while retaining the same package and pin configuration, and can be used as a replacement in many applications using the industry standard TIP100/101 NPN power Darlington transistor.

The five-terminal TO-220 has the added feature of having a $\overline{\text{Fault}}$ output (active low) which will indicate the existence of an over temperature, over-voltage or current limit condition, including an output short to ground.

When driving a moderate load, the MC3392 performs as an extremely high gain, low saturation Darlington transistor having CMOS input levels. The primary advantage of the MC3392 over a Darlington transistor is the additional protection afforded the device and load when driving difficult or faulty loads. This device incorporates unique internal current limit and thermal protection circuitry to safeguard itself and the associated load from catastrophic failure.

The MC3392 is available in a three and five-lead TO-220 package; the five-lead having the added diagnostic feature. The full featured MC3392 is also available in a 16 pin wide body SOIC plastic power package.

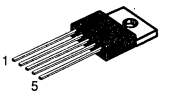
- Designed for Automotive Applications
- Can Be Used as a Replacement for TIP100/101 NPN Power Darlingtons
- Drives Inductive Loads without External Clamp Circuitry
- Withstands Negative and Positive Transient Voltages
- Low ON Voltage
- CMOS Logic Compatible Input
- Over Current, Overvoltage, and Thermal Protection
- Extended Operating Temperature Range
- $\overline{\text{Fault}}$ Output



Pin 1. Input
2. Output
3. Ground

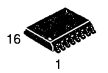
(Heatsink surface connected to Pin 3)

T SUFFIX
PLASTIC PACKAGE
CASE 221A
(TO-220)



Pin 1. Input
2. $\overline{\text{Fault}}$
3. Ground
4. NC
5. Output

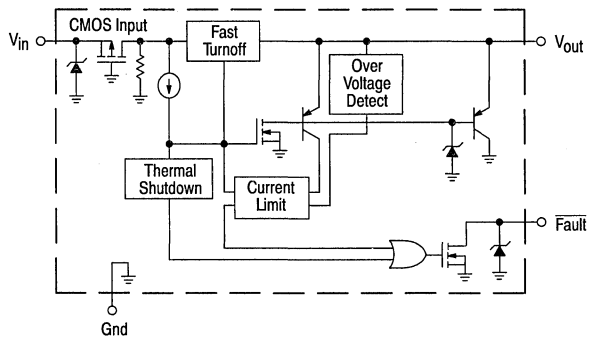
T-1 SUFFIX
PLASTIC PACKAGE
CASE 314D
(TO-220)



Pin 1. NC
2. NC
3. NC
4. Output
5. Input
6. $\overline{\text{Fault}}$
7. NC
8. NC
9–16. Ground

DW SUFFIX
PLASTIC PACKAGE
CASE 751G
SOP(8+8)L

Simplified Block Diagram



ORDERING INFORMATION

Device	Ambient Temperature Range	Package
MC3392T	– 40° to +125°C	Plastic Power
MC3392T-1		Plastic Power
MC3392DW		SOP(8+8)L

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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage Range	V_{in}	– 0.5 to + 6.5	V
Output Transient Breakdown Voltage — Forward — Reverse	V_{BF} V_{BR}	+ 60 – 80	V
Short Circuit Current	I_{SC}	2.2	A
Output Avalanche Energy (Note 1)	E_{max}	60	mJ
Minimum ESD Voltage Capability (Note 2)	ESD	2000	V
Operating Junction Temperature Internally Limited (Note 3)	T_J	150	°C
Storage Temperature	T_{stg}	– 65 to +150	°C
Operating Ambient Temperature Range	T_A	– 40 to +125	°C
Thermal Resistance (Notes 4, 5) TO-220 — Junction to Ambient — Junction to Case SOIC — Junction to Ambient — Junction to Case	 θ_{JA} θ_{JC} θ_{JA} θ_{JC}	 62.5 2.5 118 59	°C/W

ELECTRICAL CHARACTERISTICS (Limit values are noted under conditions: – 40°C ≤ T_A ≤ +125°C. Typical denotes calculated mean value derived from 25°C parametric data, unless otherwise noted.)

Characteristic	Figure	Symbol	Min	Typ	Max	Unit
Input Control Current V_{in} = 1.0 V V_{in} = 4.0 V V_{in} = 5.0 V	3	I_{in}	 — — —	 0.2 230 260	 10 350 500	µA
Input Voltage High (ON) Input Voltage Low (OFF)	7	V_{IH} V_{IL}	4.0 —	2.0 2.0	— 1.0	V
Output Leakage Current $+V_S$ = 28 V, R_L = 0	4	I_L	—	1.3	100	µA
Output Short Circuit Current $+V_S$ = 14 V, R_L = 0	5	I_{SC}	1.0	1.3	2.2	A
Output ON Voltage (V_{in} = 4.0 V, Note 6) I_O = 400 mA I_O = 800 mA	6	V_{OL}	 — —	 0.95 1.1	 1.1 1.8	V
Output Clamp Voltage I_O = 100 mA	8	V_{OC}	60	70	80	V
Reverse Leakage Current V_{out} = –13 V	9	I_{BR}	—	–10	– 30	mA
Fault Output Sink Saturation (I_{Sink} = 100 µA, V_{in} = 5.0 V)	10	$V_{DS(sat)}$	—	0.3	0.4	V
Fault Output Off-State Leakage (V_{DS} = 5.0 V)		$I_{DS(leak)}$	—	0.6	100	µA
Turn-On Time 10% to 90% of I_O (400 mA nominal) Turn-Off Time 90% to 10% of I_O (400 mA nominal) Propagation Delay Time Input to Output (Turn-on/Turn-off, 50%)	11 12 —	t_r t_f t_d	 — — —	 3.3 9.7 3.0	 20 25 10	µA

NOTES: 1. Capability for both positive and negative repetitive transient pulses.
2. ESD testing performed in accordance with Human Body Model (C_{Zap} = 100 pF, R_{Zap} = 1500 Ω).
3. This device incorporates internal circuit techniques which do not allow the internal junction temperature to reach destructive temperatures.
4. The thermal resistance case is considered to be a point located near the center of the tab and plastic body of the TO-220 or a point on one of the heatsink leads (Pins 9 to 16) of the SOIC.
5. The SOIC thermal information is based on simulation data.
6. I_O is defined as the output sink current.

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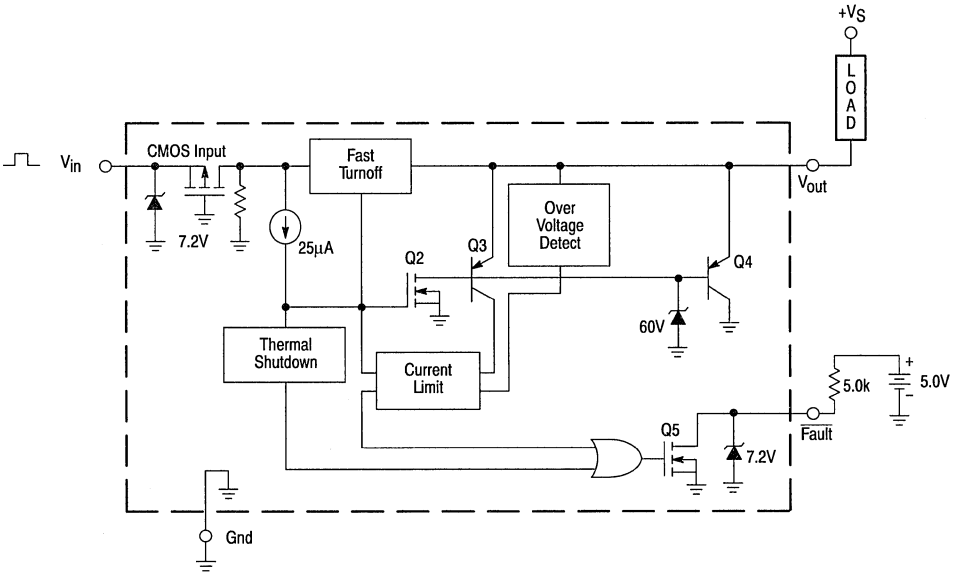
PIN FUNCTION DESCRIPTION

Name	Pin Number			Description
	Case 221A	Case 314D	SOIC	
V_{in}	1	1	5	CMOS compatible input.
V_{out}	2	5	4	Output to load and battery, protected by a 60 V clamp against inductive load transients.
Gnd	3	3	9 to 16	Ground connection.
$\overline{Fault}$	N/A	2	6	Fault output pulled low when the IC is operating in a fault state. The open drain output requires a pull-up resistor for normal operation.

Figure 1. MC3392 Representative Block Diagram



Definition of Currents and Voltages. Positive current flow is defined as conventional current flow into the device. Negative current flow is defined as current flow out of the device. All voltages are referenced to ground. Both currents and voltages are specified as absolute (i.e., –10 V is greater than –1.0 V).

Figure 2. Fault Output Timing Diagram

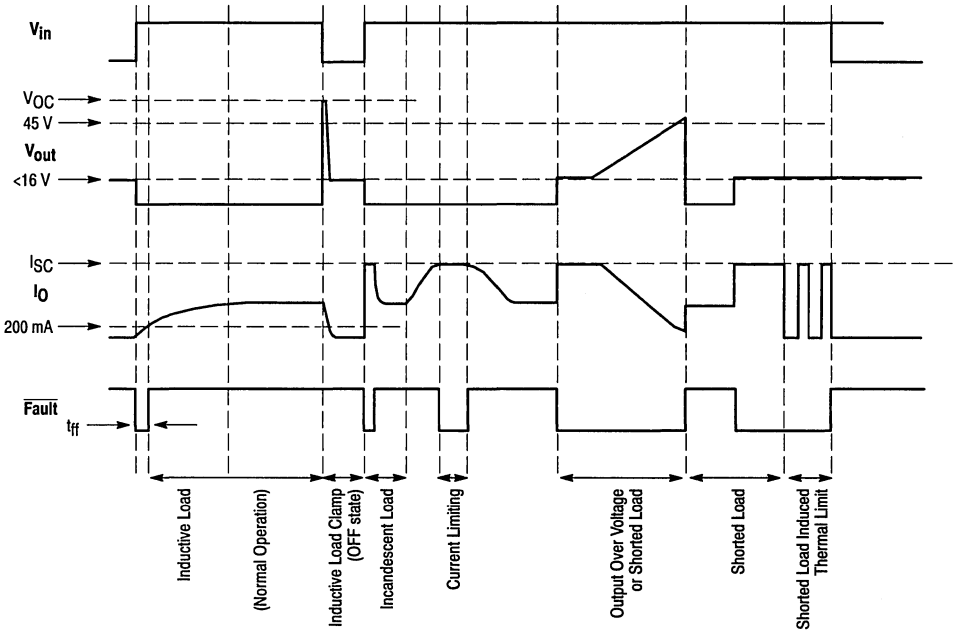


Figure 3. Input Control Current versus Input Voltage

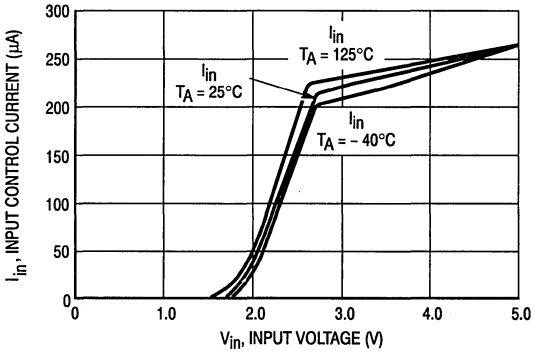


Figure 4. Output Leakage Current versus Temperature

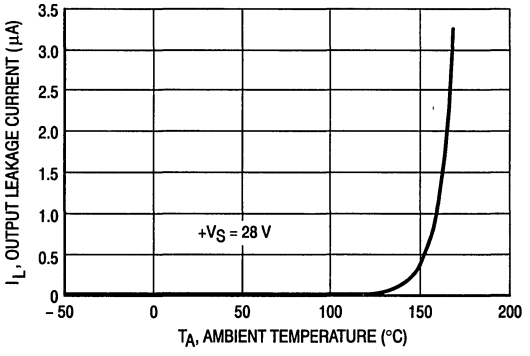


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Figure 5. Output Short Circuit Current versus Temperature

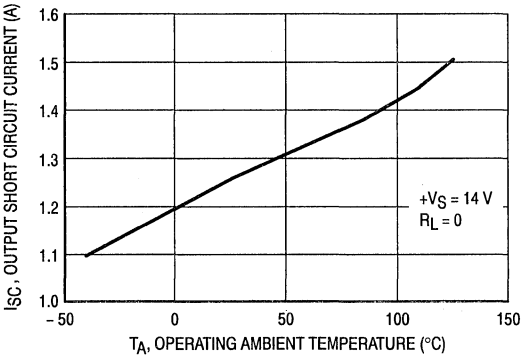

Figure 6. Output On Voltage versus Temperature

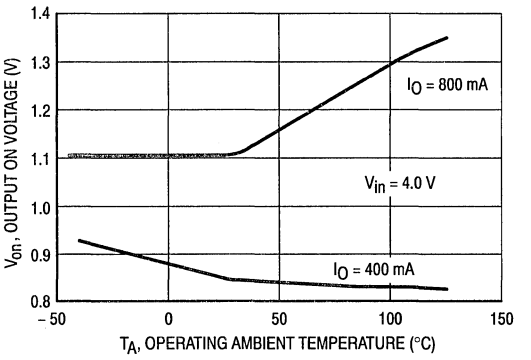

Figure 7. Input Voltage versus Temperature

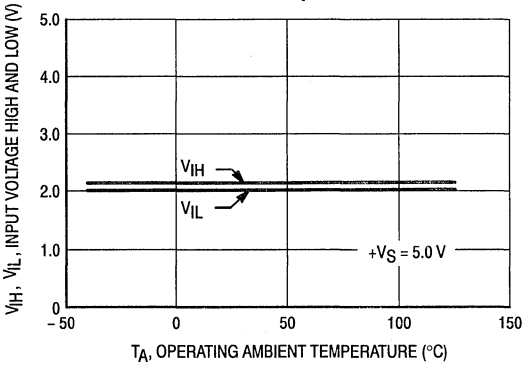

Figure 8. Output Clamp Voltage versus Temperature

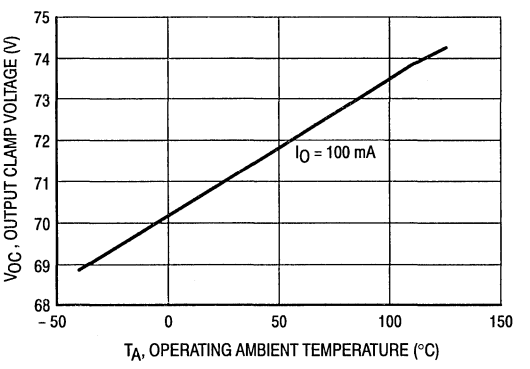

Figure 9. Reverse Breakdown Voltage versus Temperature

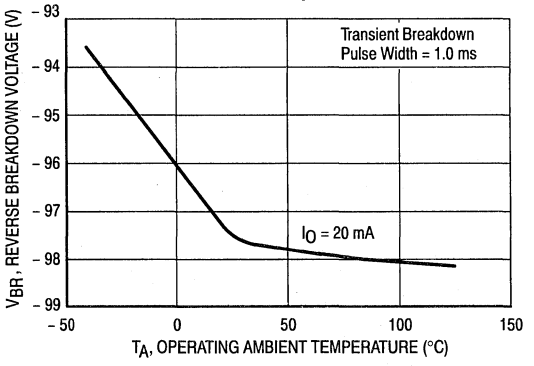

Figure 10. $\overline{\text{Fault}}$ Output Saturation versus Sink Current

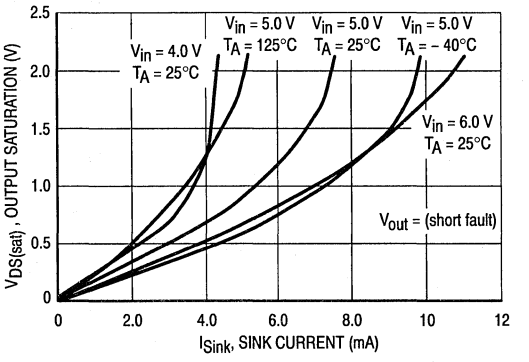

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Figure 11. Turn-On Waveform

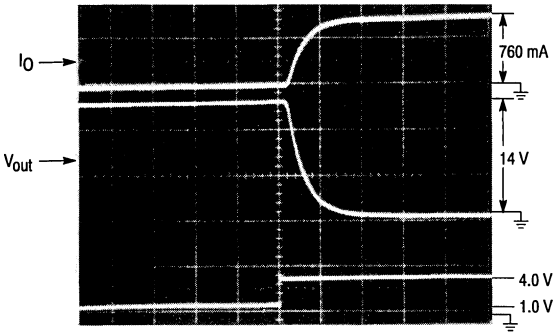


Figure 12. Turn-Off Waveform

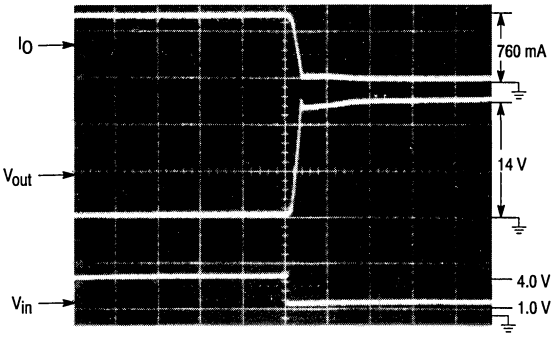


Figure 13. Output Current versus Supply Voltage

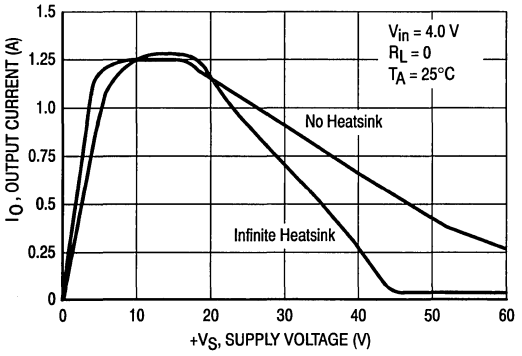
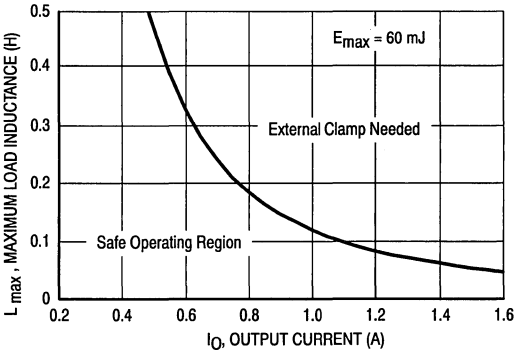


Figure 14. Maximum Load Inductance versus Output Current



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TECHNICAL DISCUSSION

Introduction

The MC3392 is a low side protected switch incorporating many features making it ideal for use in harsh automotive applications. The protection circuitry of the MC3392 protects not only itself but also the associated load from destructive voltage transients attributed to load and field dump, as well as, reverse and double battery conditions found in automotive applications. The MC3392 is unique in that the protection circuitry is internal and does not require additional external protection components for its operation. This makes the device very cost effective in that its application utilizes few external components, thus reducing cost and space requirements needed for the system. The MC3392 is extremely effective when used to drive solenoids, as well as, incandescent lamp loads. The following description of the device's operation is in reference to the functional blocks of the Representative Block Diagram shown in Figure 1.

CMOS Input

The input of the MC3392 is CMOS compatible. Input control performs as true logic in that when the input (V_{in}) is less than 1.0 V, the MC3392 switch is in a high impedance or OFF state and when V_{in} is greater than 4.0 V the MC3392 is in a low impedance or ON state. The switching threshold of the input is approximately 2.0 V and is graphed in Figure 7. With the input at 4.0 V, the input sink current will be approximately 250 μA. In the ON state, the internal protection circuitry is activated and all of the protection features are available for use. In the OFF state, however, it is important to note that none of the protection features are available, with the exception of the internal inductive load clamp. The input pin is afforded a minimum of 2000 V ESD protection (Human Body Model) by virtue of the 7.2 V zener diode.

Over Temperature Shutdown

Internal Thermal Shutdown Circuitry is provided to protect the MC3392 in the event the Operating Junction Temperature (T_J) exceeds 150°C. Typically, Thermal Shutdown will occur at 160° to 170°C. The Thermal Shutdown sense element is embedded within the output PNP (Q4) so as to afford very fast thermal coupling of Q4 to the sense element. Any rise in temperature due to the ambient is translated directly to Q4 and the sense element. If the junction temperature rises excessively above 150°C, the Thermal Shutdown circuit will turn ON, quickly pulling the gate of Q2 to ground, which pulls the base of Q4 to ground, turning it OFF. In addition, the Thermal Shutdown circuit simultaneously turns Q5 ON and with a suitable pull-up resistor at the $\overline{\text{Fault}}$ pin reports the presence of a fault (logic low). The output PNP will remain OFF until the junction temperature decreases to within the operating range at which time Thermal Shutdown turns OFF, ceasing to hold the gate of Q2 low, turning Q4 back ON. This process will repeat as long as the thermal over load exists. This mode of operation is a nondestructive safety feature of the device and will real time correct itself when the cause of over temperature is removed. A continued over temperature condition will thermally Pulse Width Modulate (PWM) the output and $\overline{\text{Fault}}$ and may be incorrectly interpreted as an oscillating load if one does not consider the simultaneous performance of the $\overline{\text{Fault}}$ pin.

Current Limit

The MC3392 protects itself against V_{out} to $+V_S$ hard shorts as well as any over current conditions by reducing the magnitude of output current (I_O) to that of the short circuit current limit value (I_{SC}). When the output current monitored by Q3 tries to exceed I_{SC}, the Current Limit circuit lowers the gate voltage of Q2, lowering the base of Q4, causing the load current through Q4 to diminish. Simultaneously, when the load current exceeds I_{SC}, Q5 will turn ON reporting a fault condition. If the output current is allowed to remain excessively high for the degree of heat sinking incorporated, and the junction temperature of the device is allowed to heat beyond 150°C, the Thermal Shutdown circuit will activate and the output will thermally PWM. Again, these modes of operation are safety features of the MC3392 and are not destructive.

Overvoltage Detect

This circuitry protects the MC3392 from V_{out} voltages in excess of 16 V by lowering the output current to a nondestructive value. With increasing V_{out} voltage ($16\text{ V} < V_{out} < 45\text{ V}$) the load current is reduced to below that of I_{SC} and produces a fold back current effect. As V_{out} increases in excess of 16 V, the output current decreases linearly until V_{out} exceeds 45 V. With an infinite heatsink and $V_{out} > 45$ V, I_O will be less than 100 mA. For the other extreme, no heatsink and $V_{out} > 45$ V, I_O can be expected to be less than about 400 mA. This behavior of I_O in relation to V_{out} is shown in Figure 13.

For the infinite heatsink case, the output current initially increases with increased voltage until V_{out} exceeds 16 V, thereafter the behavior is expressed as,

$$I_O = I_{SC}\,[1-(V_{out}-16\text{ V})\,/\,30\text{ V}]$$

Beyond 45 V, I_O is limited to less than 100 mA. Anytime the Overvoltage Detect circuit is activated, the gate of Q5 is pulled low causing Q5 to turn ON to report the fault at the $\overline{\text{Fault}}$ pin.

Inductive Load Clamp

The MC3392 has an internal inductive load clamp for protection against flyback voltages imposed on the output pin in excess of 70 V. The incorporated zener clamp can quickly dissipate up to 60 milli-Joules of inductive flyback energy. Figure 14 shows the maximum inductive load versus load current that the clamp can handle safely. As an example (using Figure 14), if operating the MC3392 to drive a 0.33 H inductor, the maximum load current should be adjusted to 600 mA or less. If the load current is too high for the inductor used, some series resistance can be added to the load to limit the current. If this is not possible, an external clamp must be used to facilitate handling the higher energy. When using an external clamp, the external clamp voltage must be less than 60 V so as to override the internal clamp. The output clamp offers protection for the output when the MC3392 is in the OFF state. During the ON state, other protection features (Overvoltage, Current, and Temperature) are available to protect the output.

$\overline{\text{Fault}}$ Logic

The $\overline{\text{Fault}}$ is comprised of an internal open drain FET requiring an external pull-up resistor. Typically, a 5.0 k pull-up resistor to a +5.0 V supply is satisfactory. The $\overline{\text{Fault}}$ pin is afforded a minimum of 2000 V ESD protection (Human Body Model) by virtue of the 7.2 V zener diode. The $\overline{\text{Fault}}$ will report a fault (logic low state) whenever the MC3392 experiences a fault condition. Conditions producing a fault are: $I_O > 1.3$ A (over current/shorted load); $T_J > 150$°C (over temperature); and $V_{out} > 16$ V (overvoltage).

If the device goes into Thermal Shutdown, caused by environmental overheating (not resulting from another fault condition), the $\overline{\text{Fault}}$ and V_{out} will thermally PWM as the MC3392 repeatedly heats to shut off, cools, and again turns on. If a current limit fault causes the device to go into Thermal Shutdown, the output will oscillate while the $\overline{\text{Fault}}$ remains pulled low. There is no designed-in thermal hysteresis to control the PWM effect and this fault mode of operation is not destructive.

Fast Turn-Off

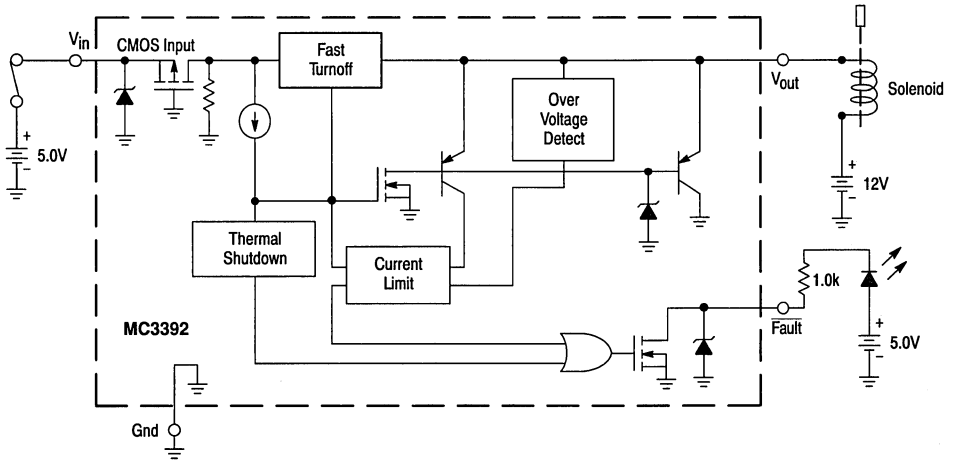
This circuitry enhances the MC3392 turn-off performance. Whenever V_{in} goes to a logic low state, V_{out} is held in an OFF state for approximately 15 µs. During fast turn-off, less than 30 mA of current is allowed to flow producing an abrupt turn-off. This turn-off characteristic can be seen in Figure 12, a photograph of the typical turn-off waveform.

APPLICATIONS INFORMATION

Solenoid Driver

The MC3392 can be used to drive a variety of solenoid applications similar to that of Figure 15. For example; driving a solenoid having an inductance of 73.8 mH and a resistance of 95 Ω from a 12 V supply will cause 240 mA of sink current to flow with the MC3392 in the ON state. The resulting current value is within the normal load current operating region and will not produce a fault. Load current is paramount in any design using the MC3392 and must be less than I_{SC} for acceptable operation. If the load current is greater than I_{SC}, a current limit fault state will exist. Operation in this state is not destructive as the device will turn off if the Junction Temperature (T_J) rises above 150°C. When the Junction Temperature cools below 150°C the device will again turn-on, with a repeat of the cycle. Careful design to acceptable load current limits should be insured for satisfactory operation of an application.

Figure 15. Solenoid Driver



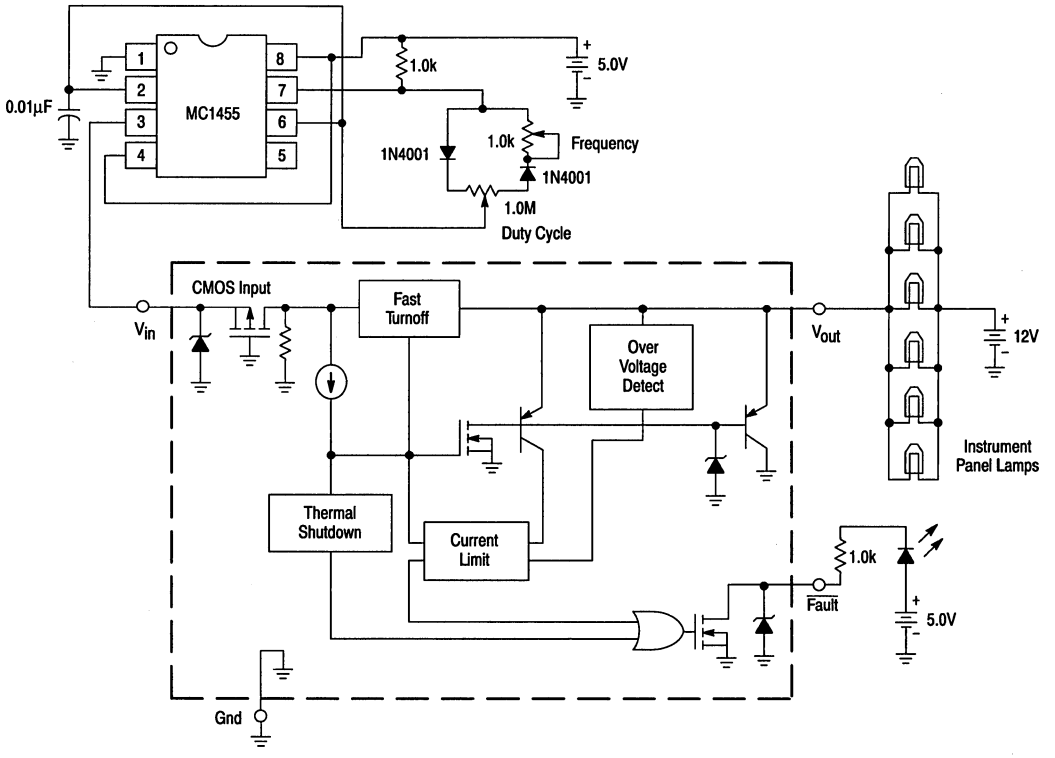
10

Instrument Panel Lamp Dimmer Control

The MC3392 can be used to control the dimming function associated with instrument panel lamps. The brightness of incandescent lamps can be varied by Pulse Width Modulating the input of the MC3392. The modulating signal for the MC3392 can be obtained directly from a microprocessor or, as in Figure 16, from an MC1455 timer. The MC1455 timer is configured as a free-running clock having both frequency and duty cycle control. The typical timer frequency is approximately 80 Hz when the frequency potentiometer is adjusted to 1.0 k. This frequency was chosen so as to avoid any perceptible lamp flicker. The duty cycle potentiometer controls the duty cycle over a range of approximately 3.0% to 97%; When at 3.0% duty cycle, the lamps are essentially off; When at 97% duty cycle, the lamps are essentially full lit. Six incandescent lamps are shown in this application drawing 720 mA total current. Similar applications can be used to drive a variety of lamp loads. The total load current is the primary factor of consideration when driving lamp loads. The total value of I_O must be less than I_{SC}.

Another convenient aspect of this application is the LED. The LED can be used to denote the existence of a system fault (overvoltage, current limiting, or thermal shutdown).

Figure 16. Instrument Panel Lamp Dimmer Control



10

MC3399

AUTOMOTIVE HIGH SIDE DRIVER SWITCH

SILICON MONOLITHIC INTEGRATED CIRCUIT

Automotive High Side Driver Switch

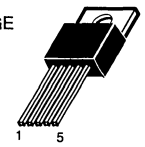
The MC3399T is a High Side Driver Switch that is designed to drive loads from the positive side of the power supply. The output is controlled by a TTL compatible Enable pin. In the ON state, the device exhibits very low saturation voltages for load currents in excess of 750 mA. The device also protects the load from positive or negative going high voltage transients by becoming an open circuit and isolating the transient for its duration from the load.

The MC3399T is fabricated on a power BIMOS process which combines the best features of Bipolar and MOS technologies. The mixed technology provides higher gain PNP output devices and results in Power Integrated Circuits with reduced quiescent current.

The device operates over a wide power supply voltage range and can withstand voltage transients (positive or negative) of ± 100 V. A rugged PNP output stage along with active clamp circuitry, current limit and thermal shutdown permits driving of all types of loads including inductive. The MC3399T is specified over a wide junction temperature of –40° to + 125°C and is ideally suited for industrial and automotive applications where harsh environments exist.

- Low Switch Voltage Drop
- Load Currents in Excess of 750 mA
- Low Quiescent Current
- Transient Protection Up to ± 100 V
- TTL Compatible Enable Input
- On-Chip Current Limit and Thermal Shutdown Circuitry

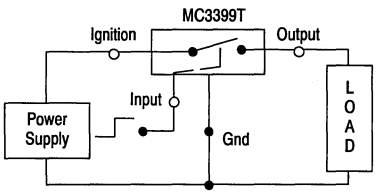
T SUFFIX
PLASTIC PACKAGE
CASE 314D



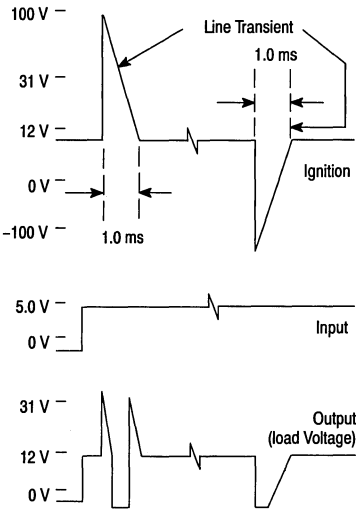
Pin 1. Ignition
2. Output
3. Output
4. Ground
5. Input

Heatsink surface connected to Pin 2

Block Diagram



Timing Diagram



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Ignition Input Voltage—Continuous	V_{IGN}	+25 –12	Vdc
Ignition Input Voltage—Transient t = 100 ms t = 1.0 ms	V_{IGN}	 ±60 ±100	V
Input Voltage	V_{in}	–0.3 to + 7.0	V
Output Current	I_O	Internally Limited	A
Power Dissipation and Thermal Characteristics T_A = + 25°C Derate above T_A = + 25°C Thermal Resistance Junction to Ambient T_C = + 25°C Derate above T_C = + 25°C Thermal Resistance Junction to Case	 P_D $1/\theta_{JA}$ θ_{JA} P_D $1/\theta_{JA}$ θ_{JA}	 2.0 16 65 25 200 5.0	 W mW/°C °C/W W mW/°C °C/W
Operating Junction Temperature Range	T_J	–40 to +125	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

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ELECTRICAL CHARACTERICISTICS (V_{IGN} = +12 V, I_L = 150 mA, –40°C ≤ T_J = +125°C, V Input = "1", unless otherwise noted.)*

Characteristics	Symbol	Min	Typ	Max	Unit
Operating Voltage	$V_{IGN(min)}$	4.5	—	—	V
Switch Voltage Drop (Saturation)	$V_{IGN}–V_O$				V
V_{IGN} = 4.5 V I_O = 150 mA T_J = 25°C		—	0.2	0.5	
I_O = 200 mA T_J = –40°C		—	0.3	0.5	
I_O = 125 mA T_J = 125°C		—	0.3	0.5	
V_{IGN} = 12 V I_O = 425 mA T_J = 25°C		—	0.3	0.7	
I_O = 550 mA T_J = –40°C		—	0.3	0.7	
V_{IGN} = 16 V I_O = 375 mA T_J = 125°C		—	0.4	0.7	
Quiescent Current	I_{GND}				mA
V_{IGN} = 12 V I_O = 150 mA T_J = 25°C		—	12	50	
I_O = 550 mA T_J = –40°C		—	25	100	
I_O = 300 mA T_J = 125°C		—	10	50	
Output Current Limit (V_O = 0 V)	I_{SC}	—	1.6	2.5	A
Output Leakage Current (V_{IGN} = 12 V, Input = "0")	I_{Leak}	—	10	150	µA
Input Voltage					V
High Logic State	V_{IH}	2.0	—	—	
Low Logic State	V_{IL}	—	—	0.8	
Input Current					µA
High Logic State (V_{IH} = 5.5 V)	I_{IH}	—	120	—	
Low Logic State (V_{IL} = 0.4 V)	I_{IL}	—	20	—	
Output Turn-On Delay Time Input = "0" → "1", T_J = +25°C (Figures 1 and 2)	$t_{DLY(on)}$	—	50	—	µs
Output Turn-Off Delay Time Input = "1" → "0", T_J = +25°C (Figures 1 and 2)	$t_{DLY(off)}$	—	5.0	—	µs
Over Voltage Shutdown Threshold	$V_{in(OV)}$	26	31	36	V
Output Turn-Off Delay Time (T_J = + 25°C) to Overvoltage Condition, V_{in} stepped from 12 V to 40 V, V ≤ 0.9 V_O (Figures 1 and 2)	t_{DLY}	—	2.0	—	µs
Output Recovery Delay Time (T_J = + 25°C) V_{IGN} stepped from 40 V to 12 V, V ≥ 0.9 V_O (Figures 1 and 2)	t_{RCVY}	—	5.0	—	µs

*Typical Values Represent Characteristics of Operation at T_J = + 25°C.

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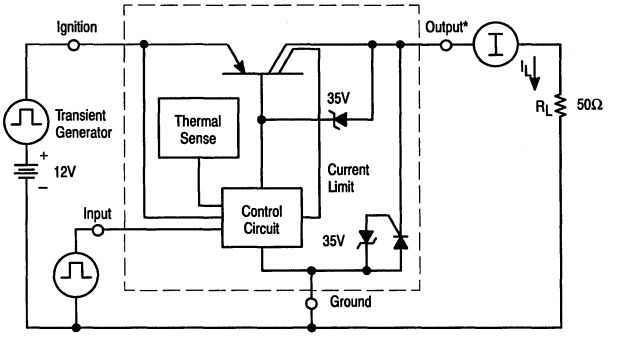
Figure 1. Transient Response Test Circuit



NOTE:
*Depending on Load Current and Transient Duration, an Output Capacitor (C_O) of sufficient value may be used to hold up Output Voltage during the Transient, and absorb Turn-off Delay Voltage Overshoot.

Figure 2. Response Time Diagram

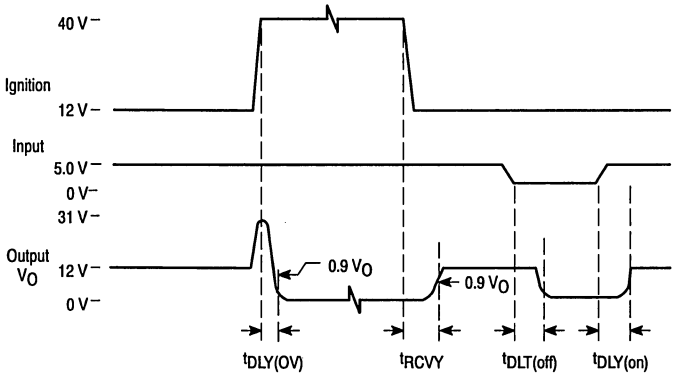


Figure 3. Switch Voltage Drop versus Load Current

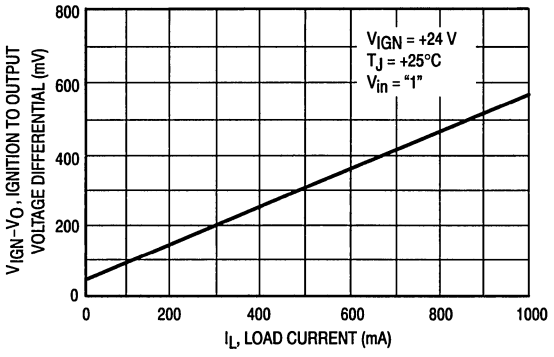
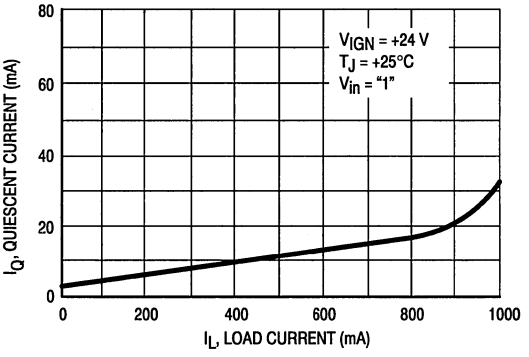


Figure 4. Quiescent Current versus Load Current



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MC3484S2-2
MC3484S4-2

SOLENOID DRIVER
2.4 A — S2
4.0 A — S4

Integrated Solenoid Driver

The MC3484 is an integrated monolithic solenoid driver. Its typical function is to apply full battery voltage to fuel injector(s) for rapid current rise, in order to produce positive injector opening. When load current reaches a preset level (4.0 A in MC3484S4 or 2.4 A in MC3484S2) the injector driver reduces the load current by a 4-to-1 ratio and operates as a constant current supply. This condition holds the injector open and reduces system dissipation. Other solenoid or relay applications could be served by the MC3484. Two high impedance inputs are provided which permit a variety of control options and can be driven by TTL or CMOS logic.

- Microprocessor Compatible Inputs
- On-Chip Power Device
  MC3484S2-2 2.4 A Peak 0.6 A Sustain
  MC3484S4-2 4.0 A Peak 1.0 A Sustain
- Low Thermal Resistance to Grounded Tab—$R_{\theta JC}$ = 2.5°C/W
- Overvoltage Protection Cutoff
- Low Saturation Voltage: $V_{CE(sat)}$ = 1.6 V Typ @ 4.0 A
- Uncompromised Performance – 40° to + 85°C Junction Temperature
- Fully Functional from V_{bat} = 4.0 V to 24 V
- High $V_{CEO(sus)}$ = 42 V min @ I_{sus}
- Alternate Lead Forms are Available

S SUFFIX
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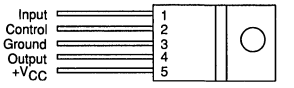
PIN CONNECTIONS



(Unformed Package)

ORDERING INFORMATION

Device	Tested Ambient Temperature Range	Peak Current
MC3484S2-2	–40° to +85°C	2.4 A
MC3484S4-2		4.0 A

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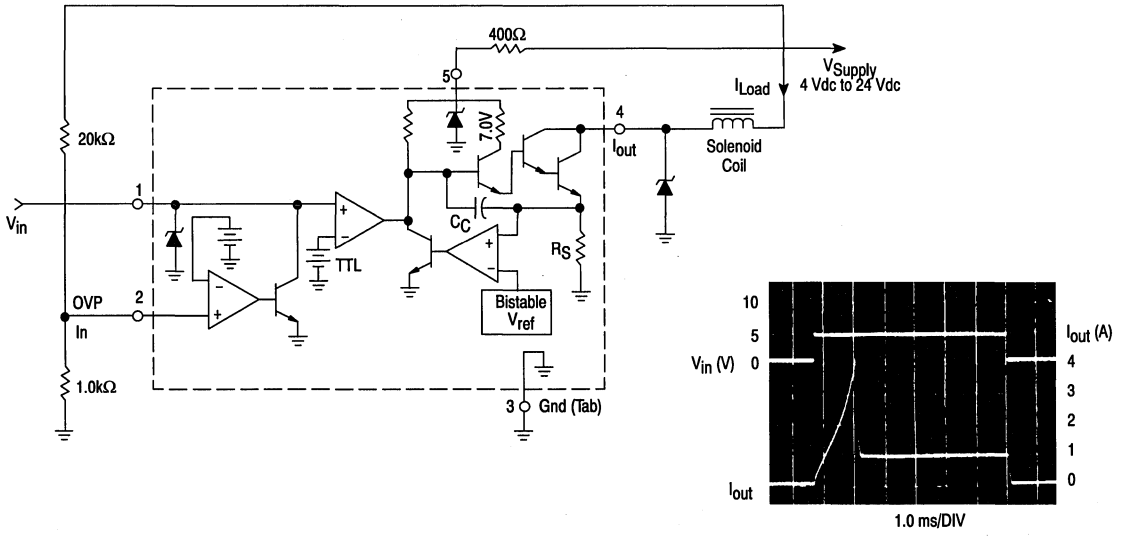
Figure 1. Typical Application
Single Injector with Overvoltage Protection at 30 V (V_{bat})



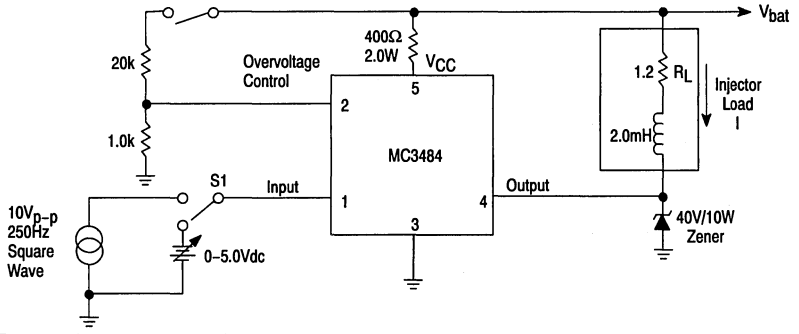
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage (V_{bat})	V_{bat}	24	V
Input (Pin 1) Control (Pin 2)	V_{in} V_{cont}	–0.3 to +6.0 0 to +5.0	V
Internal Regulator (Pin 5)	—	50	mA
Junction Temperature	T_J	150	°C
Operating Temperature (Tab Temperature)	T_A	–40 to +105	°C
Storage Temperature	T_{stg}	–65 to + 150	°C
Thermal Resistance, Junction-to-Case	θ_{JC}	2.5	°C/W

ELECTRICAL CHARACTERICISTICS (V_{bat} = 12 Vdc, T_C = –40° to +85°C, test circuit of Figure 2, unless otherwise noted.)

Characteristics		Symbol	Min	Typ	Max	Unit
Output Peak Current	S4-2 S2-2	$I_{pk(sense)}$	3.6 1.7	4.0 2.4	5.2 2.9	A
Output Sustaining Current		I_{sus}	0.95 0.50	1.0 0.6	1.3 0.7	A
$V_{CEO(sus)}$ @ 2.0 A		—	42	50	—	V
Output Voltage in Saturated Mode S2 @ 1.5 A S4 @ 3.0 A		V_{out}	 — —	 1.2 1.6	 — —	V
Internal Regulated Voltage (V_{CC}, Figure 2)		V_{reg}	—	7.1	—	V
Input "On" Threshold Voltage		V_{on}	—	1.4	2.0	V
Input "Off" Threshold Voltage		V_{off}	0.7	1.3	—	V
Input "On" Current @ V_I = 2.0 Vdc @ V_I = 5.0 Vdc		I_{in}	 — —	 50 220	 — —	µA
Control "On" Threshold Voltage		V_{cont}	—	1.5	—	V
Control "On" Current		I_{in2}	—	75	—	µA
Control Pin Impedance		V_1 Low	—	10	—	kΩ
Input Turn on Delay		t_i	—	0.5	—	µs
I_{pk} sense to I_{sus} delay		t_p	—	60	—	µs
Control Signal Delay		t_t	—	15	—	µs
Input Turn Off from Saturated Mode Delay		t_s	—	1.0	—	µs
Input Turn Off from Sustain Mode Delay		t_d	—	0.2	—	µs
Output Voltage Rise Time		t_v	—	0.4	—	µs
Output Current Fall Time	2.0 A 4.0 A	t_f	— —	0.3 0.6	— —	µs

Figure 2. Test Circuit



GENERAL INFORMATION

Inductive actuators such as automotive electronic fuel injectors, relays, solenoids and hammer drivers can be powered more efficiently by providing a high current drive until actuation (pull-in) occurs and then decreasing the drive current to a level which will sustain actuation. Pull-in and especially drop-out times of the actuators are also improved.

The fundamental output characteristic of the MC3484 provides a low impedance saturated power switch until the load current reaches a predetermined high-current level and then changes to a current source of lower magnitude until the device is turned off. This output characteristic allows the inductive load to control its actuation time during turn-on while minimizing power and stored energy during the sustain period, thereby promoting a fast turn-off time.

Automotive injectors at present come in two types. The large throttle body injectors have an impedance of about 2.0 mH and 1.2 Ω and required the MC3484S4 driver. The smaller type, popular world-wide, has an impedance of 4.0 mH and 2.4 Ω and needs about a 2.0 A pulse for good results. Some designs are planned which employ two of the smaller types in parallel. The inductance of an injector is much larger at low current, decreasing due to armature movement and core saturation to the values above at rated current.

Operating frequencies range form 5.0 Hz to 250 Hz depending on the injector location and engine type. Duty cycle in some designs reaches 80%.

APPLICATIONS INFORMATION

The MC3484 is provided with an input pin (Pin 1) which turns the injector driver "on" and "off." This pin has a nominal trip level of 1.4 V and an input impedance of 20 kΩ. It is internally protected against negative voltages and is compatible with TTL and most other logic.

There is also a control pin (Pin 2) which may be used as an overvoltage, load dump, shutdown. When a nominal 1.5 V is applied to Pin 2, via a 20:1 voltage divider the driver and circuit are set in a safe off state at 30 V (V_{bat}).

Figure 3 shows the operating waveforms for the simplest mode; i.e., with control Pin 2 grounded. When the driver is turned on, the current ramps up to the peak current sense level, where some overshoot occurs because of internal delay. The MC3484 then reduces its output to I_{sus}. The fall time of the device is very rapid (≤ 1.0 μs), but the decay of the load current takes 150 μs to 220 μs, while dumping the load energy into the protection zener clamp. It is essential that the zener voltage be lower than the $V_{CEO(sus)}$, but not so low as to greatly stretch the load current decay time. Without the zener, the discharge of the load energy would be totally into the MC3484, which, for the high current applications could cause the device to fail. (See SOA, Figure 11.)

Also in Figure 3 is the graphically derived instantaneous power dissipation of the MC3484. It shows that, for practical purposes, the worst case dissipation is less than (I_{sus}) (V_{bat}) (duty cycle).

Provided in Figures 3 and 4 are definitions of the switching intervals specified in the Electrical Characteristics. Figure 5 shows that the critical switching parameters stay under control at elevated temperatures.

Figure 3. Operating Waveforms
(Max Frequency 250 Hz, Pin 2 Grounded)

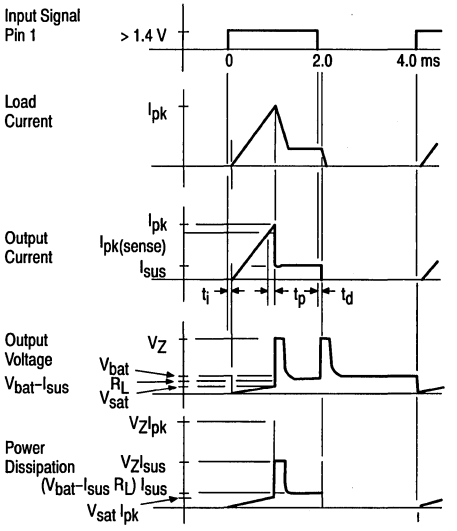


Figure 4. Switching Waveforms (Expanded Time Scale)

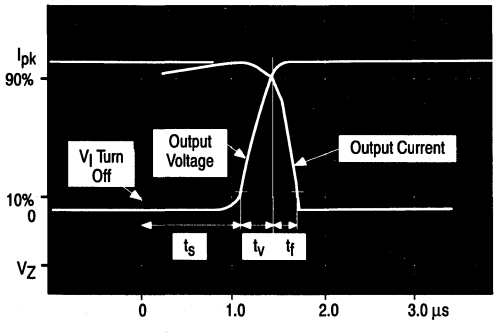
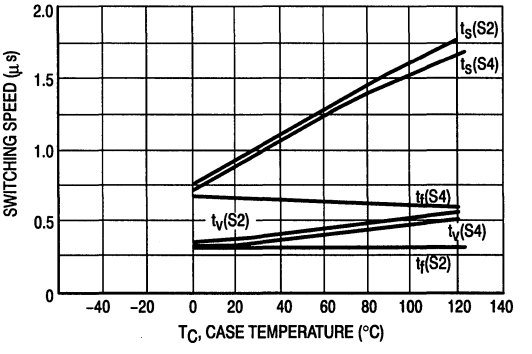


Figure 5. Switching Speed versus Temperature



TYPICAL CHARACTERISTICS

(Unless otherwise noted, test circuit of Figure 2, V_{bat} = 12 Vdc, T_C = –40° to +85°C, 250 Hz square wave input)

Figure 6. Output Current versus Temperature

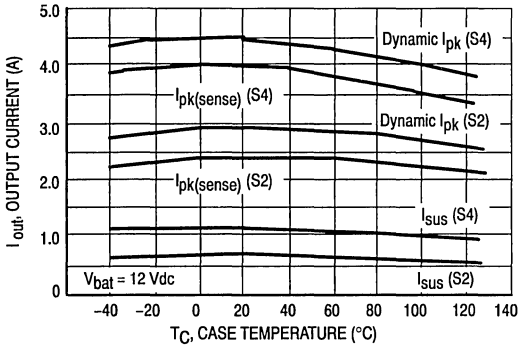


Figure 7. Saturation Voltage

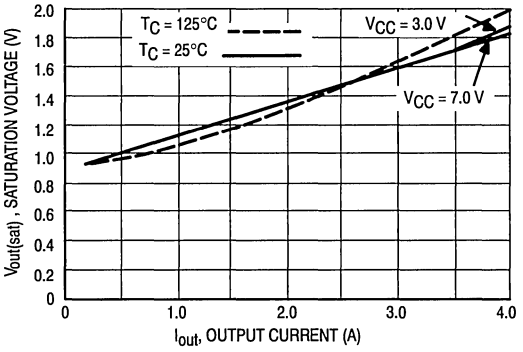


Figure 8. Output Current versus Supply Voltage

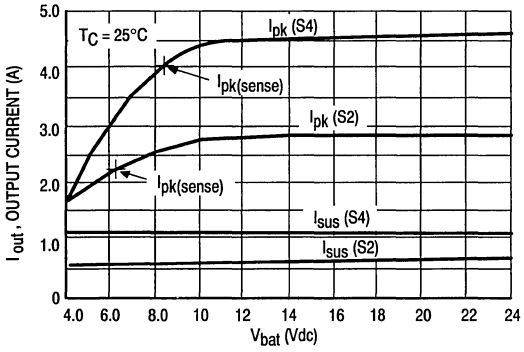


Figure 9. Operating Voltages

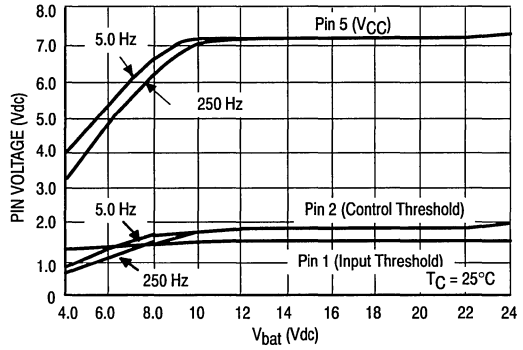


Figure 10. Breakdown Voltage versus Temperature

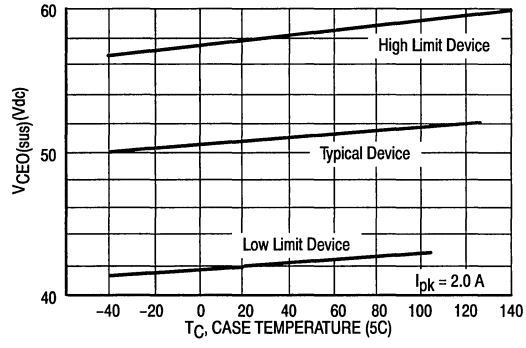
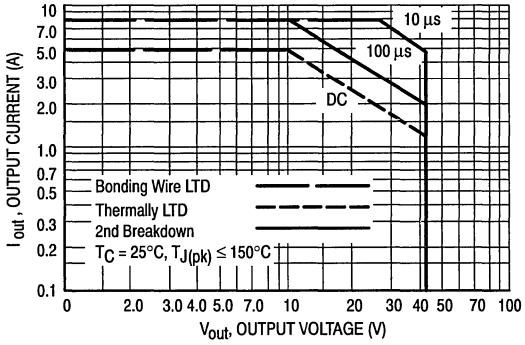


Figure 11. Safe Operating Area



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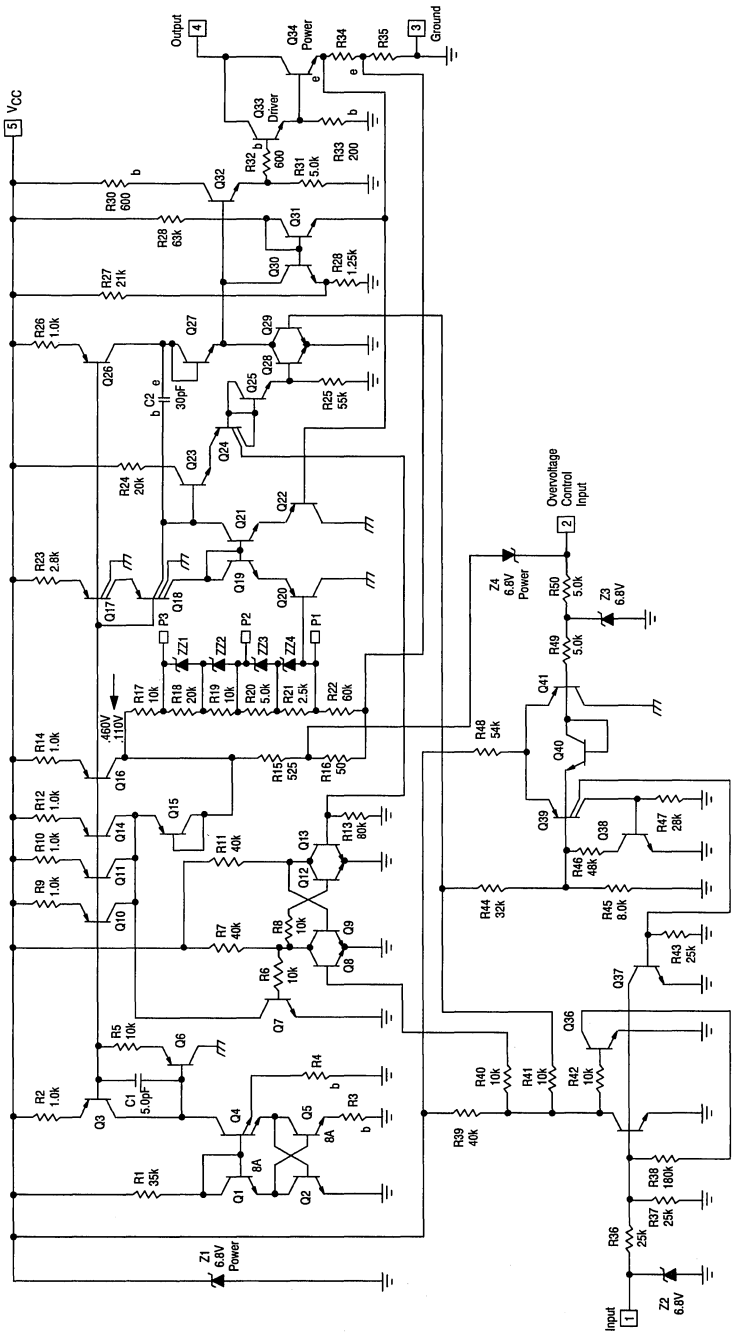

Figure 12. Internal Schematic

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MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC33091

Advance Information

High Side TMOS Driver

HIGH SIDE TMOS DRIVER

SILICON MONOLITHIC INTEGRATED CIRCUIT

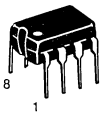
The MC33091 is a high side TMOS driver designed for use in harsh automotive switching applications which require the capability of handling high voltages attributed to load and field dump transients, as well as reverse and double battery conditions. Few external components are required to drive a wide variety of N-Channel TMOS applications. The MC33091, driving an appropriate TMOS device, offers an economical systems solution to high side switching large currents. The MC33091 has CMOS compatible input control, charge pump to drive the TMOS power transistor, basic fault detection circuit, V_{DS} monitoring circuit used to detect a shorted TMOS load, and an over current protection timer with associated current squaring circuitry.

Short circuit protection is made possible by having a unique V_{DS} voltage to current converter drive an externally programmable integrator circuit. This circuit affords quick detection of a shorted load while allowing difficult loads, such as lamps having high in-rush currents, additional time to turn on.

The $\overline{\text{Fault}}$ output is comprised of an open collector NPN transistor requiring a single pull-up resistor for operation. A fault is reported whenever the MOSFET on-current exceeds an externally programmed set level.

The MC33091 is available in the plastic 8 pin DIP as well as the 8 pin surface mount package.

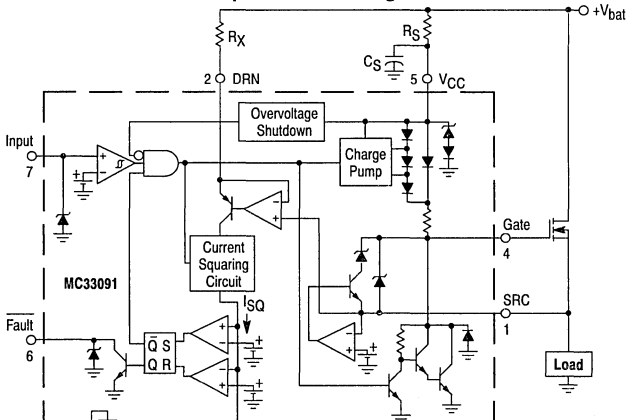
- Designed for Automotive High Side Drive Applications
- Works with a Wide Variety of N-Channel Power MOSFETs
- Drives Inductive Loads with No External Clamp Circuitry Required
- CMOS Logic Compatible Input Control
- Low Standby Current (<3.0 μA)
- On Board Charge Pump with No External Components Required
- Shorted Load Detection and Protection
- Forward Overvoltage and Reverse Battery Protection
- Load and Field Dump Protection
- Extended Operating Temperature Range
- $\overline{\text{Fault}}$ Output to Report an Over MOSFET Current Condition



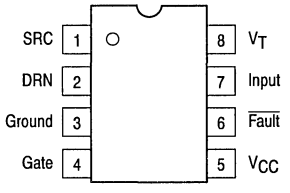
P SUFFIX
PLASTIC PACKAGE
CASE 626

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO-8)

Simplified Block Diagram



PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Temperature Range	Package
MC33091P	−40° to +125°C	Plastic DIP
MC33091D		SO-8

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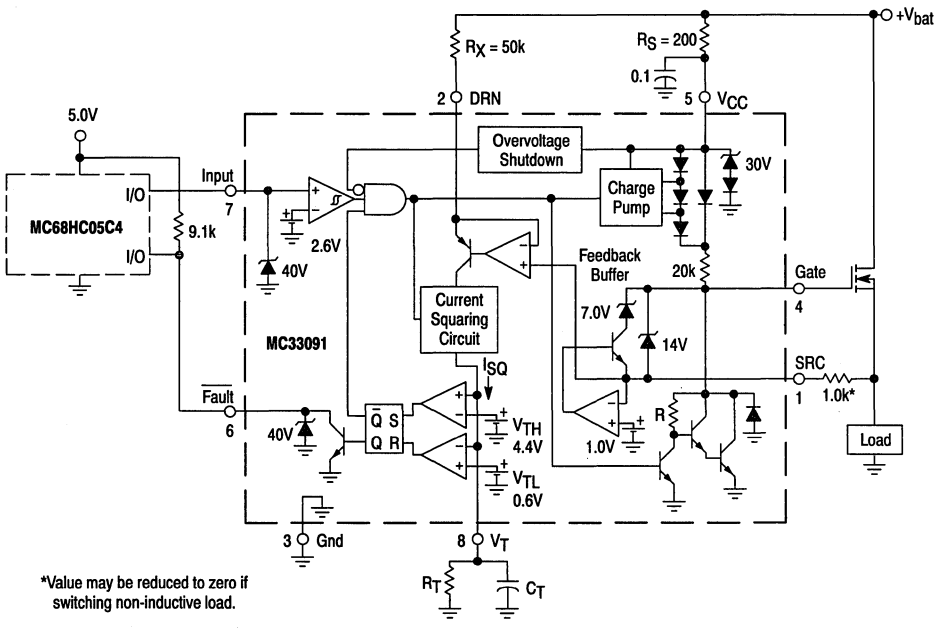
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage (Pin 5) (Note 1) Continuous (without activating clamp) Operational	V_{CC}	 –0.7 to +28 +7.0 to +28	V
Continuous Supply Clamp Current (Pin 5) DIP Package (Case 626) SO-8 Package (Case 751)	I_C	 10 1.0	mA
Input Control Voltage Range (Pin 7) Continuous	V_{in}	 –0.7 to +28	V
$\overline{\text{Fault}}$ Pull-up Voltage Range (Pin 6) Continuous	V_{out}	 –0.7 to +28	V
Minimum ESD Voltage Capability (Note 2)	ESD	2000	V
Operating Junction Temperature	T_J	150	°C
Storage Temperature	T_{stg}	–65 to +150	°C
Operating Ambient Temperature Range	T_A	–40 to +125	°C
Thermal Resistance (Junction-to-Ambient) DIP Package (Case 626) SO-8 Package (Case 751)	θ_{JA}	 100 145	°C/W

NOTES: 1. An internal zener diode is incorporated to protect the device from overvoltage transients in excess of 30 V.
2. ESD testing performed in accordance with Human Body Model (C_{Zap} = 100 pF, R_{Zap} = 1500 Ω).

Figure 1. Typical Application



ELECTRICAL CHARACTERISTICS (Values are noted under conditions of 7.0 V ≤ V_{CC} ≤ 24 V, −40°C ≤ T_A ≤ +125°C, unless otherwise noted. Typical values reflect approximate mean at T_A = 25°C at time of device characterization.)

Characteristics	Figure	Symbol	Min	Typ	Max	Unit
Supply Current (Note 1) V_{in}= 0 V V_{in} = 5.0 V (R_X = 100 k)	2	I_{CC}	 — —	 0.026 2.5	 3.0 6.0	 μA mA
Supply Clamp Voltage (Note 2)		V_Z	29	—	35	V
Gate to Source Voltage Range (Pin 4)	3,4,5,7	V_{GS}	8.0	12	15	V
Gate Current (Pin 4) V_G = V_{CC}	3,4	I_G	 30	 —	 400	μA
Short Circuit Gate Clamp Voltage (Note 4)	5	V_{GC}	6.4	7.0	7.7	V
Input Control Threshold Voltage (Pin 7)	7	 V_{IL} V_{IH}	 — 3.5	 2.7 2.7	 1.5 —	V
Input Control Current (Pin 7) (V_{in} = 5.0 V)	8	I_{in}	—	100	250	μA
Timer Current Constant (Pin 8) (R_X = 100 k, V_T = 0, V_{DS} = 1.0 V) (Note 3)	9,10	K	 0.7	 1.1	 1.5	$\mu A/V^2$
Timer (Pin 8) Lower Threshold Voltage Upper Threshold Voltage	 16,17 18,19	 V_{TL} V_{TH}	 0.4 4.1	 0.6 4.4	 1.2 4.8	V
$\overline{\text{Fault}}$ Sink Current (Pin 6) V_F = 5.0 V V_F = 0	11	 I_{OL} I_{OH}	 500 —	 — 2.0	 — 100	 μA nA
$\overline{\text{Fault}}$ Saturation Voltage (Pin 6) (I_F = 500 μA)	11	V_{OL}	—	0.2	0.8	V
Gate Saturation Voltage (I_G = 10 μA)	20,21	$V_{G(sat)}$	0	1.2	1.4	V

NOTES: 1. The total supply current into Pin 2 and Pin 5 with R_X = 100 k (from Pin 2 to supply) and 45 k pull-up resistor from Pin 6 to supply.
2. An internal zener clamp is provided to protect the device from overvoltage transients on the supply line.
3. The timer current constant is the proportionality constant of the voltage to current converter used to monitor the V_{DS} voltage developed across the FET (from Pin 1 to the supply).
4. The gate voltage will be clamped at approximately 7.0 V above the source voltage whenever the source voltage is less than approximately 1.0 V above ground.

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Figure 2. Supply Current versus Supply Voltage

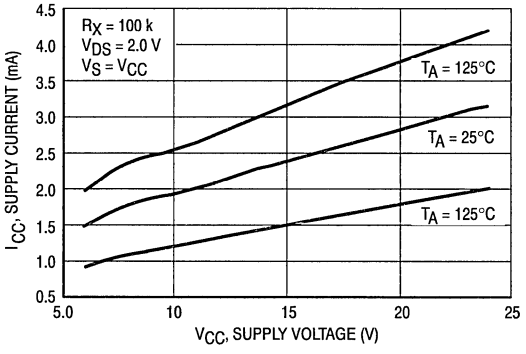

Figure 3. Gate Voltage versus Supply Voltage

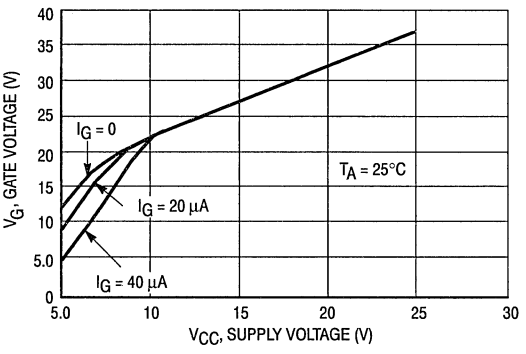

Figure 4. Gate Voltage versus Gate Current

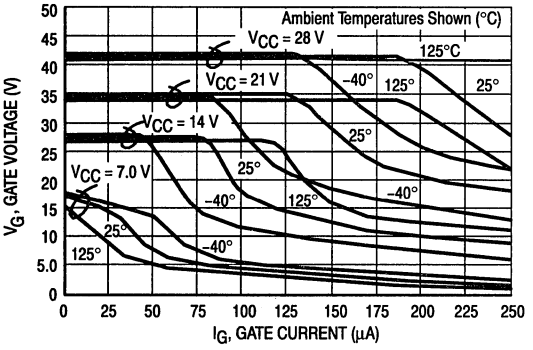

Figure 5. Gate to Source Voltage versus Source Voltage

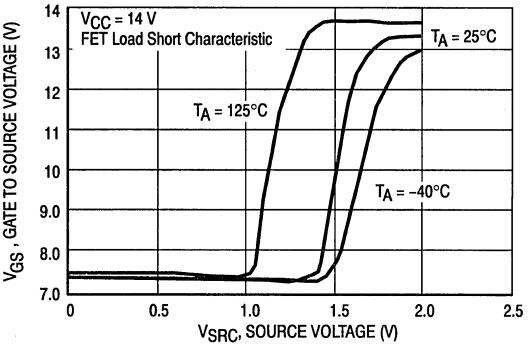

Figure 6. Gate Voltage versus Supply Voltage

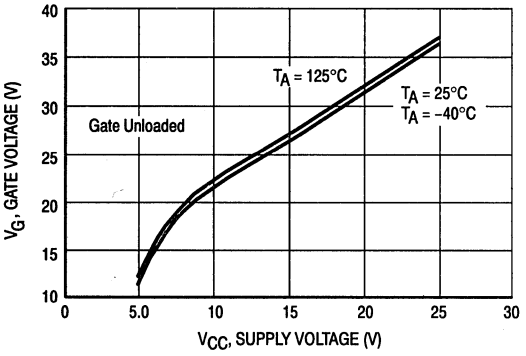

Figure 7. Gate Voltage versus Input Control Voltage

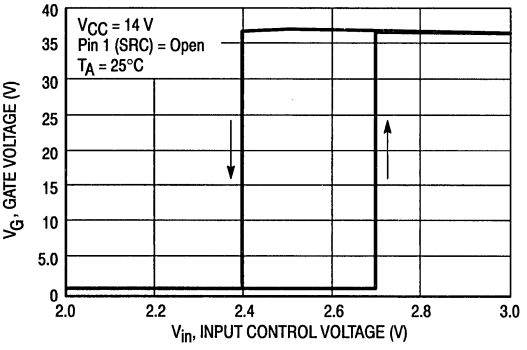

Figure 8. Input Control Current versus Input Control Voltage

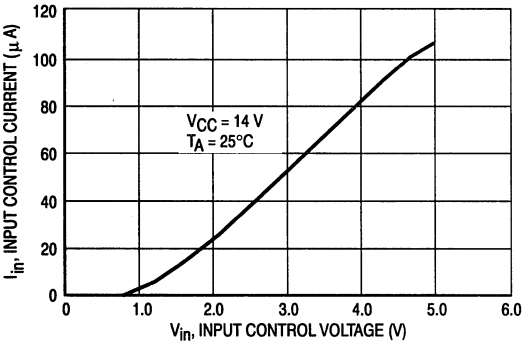

Figure 9. Squaring Constant "K" versus Supply Voltage

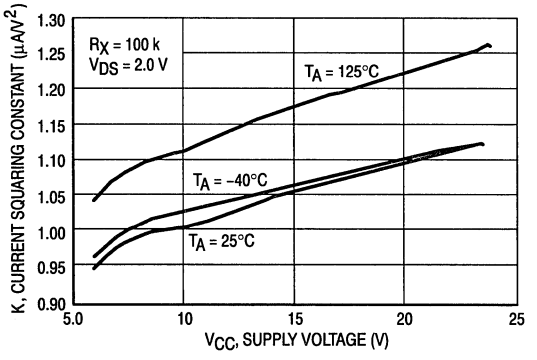

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Figure 10. Timer Current versus Drain to Source Voltage Squared

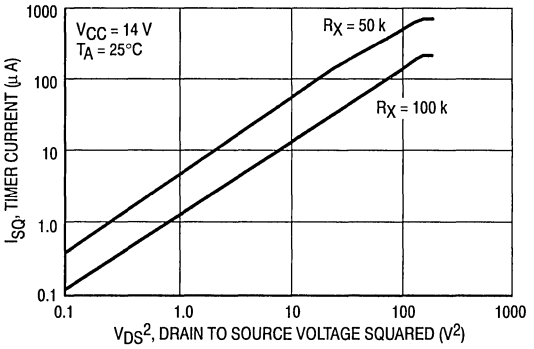

Figure 11. $\overline{\text{Fault}}$ Voltage versus $\overline{\text{Fault}}$ Sink Current

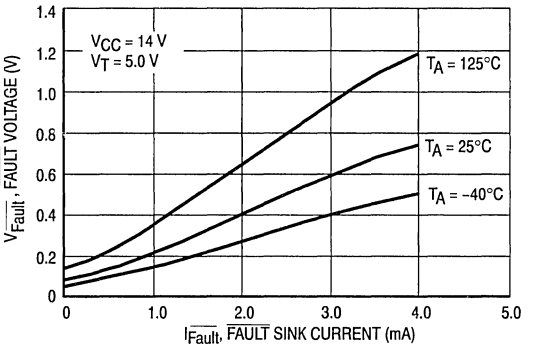

Figure 12. FET Comparison Gate Response

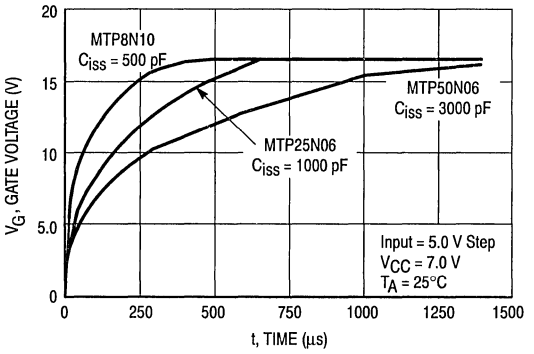

Figure 13. FET Comparison Gate Response

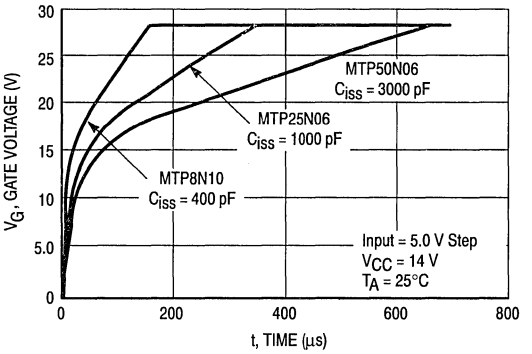

Figure 14. FET Comparison Gate Response

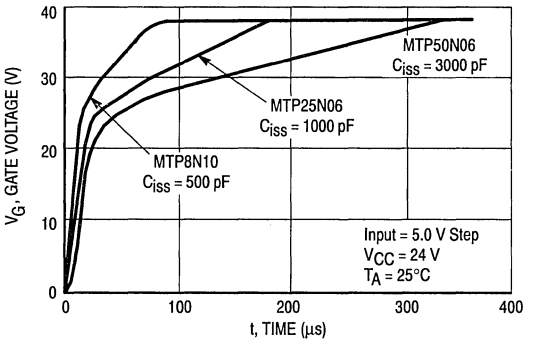

Figure 15. MTP25N06 Gate Response

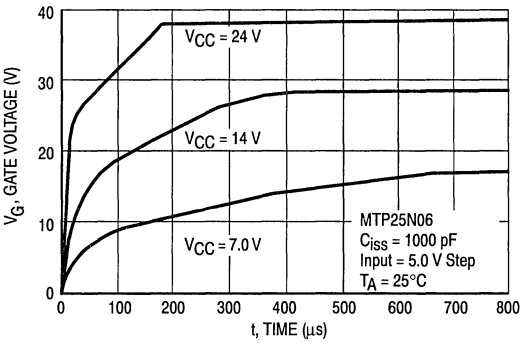

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Figure 16. Timer Lower Threshold Voltage versus Temperature

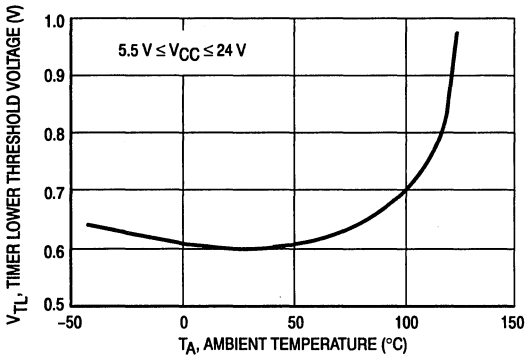

Figure 17. Timer Lower Threshold Voltage versus Supply Voltage

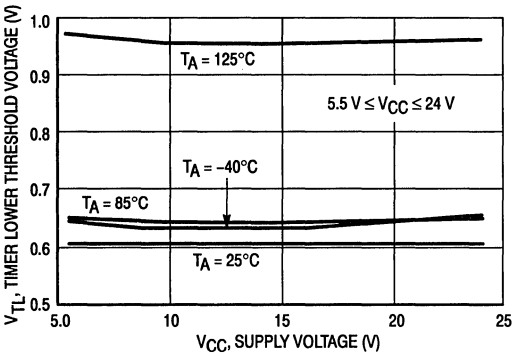

Figure 18. Timer Upper Threshold Voltage versus Temperature

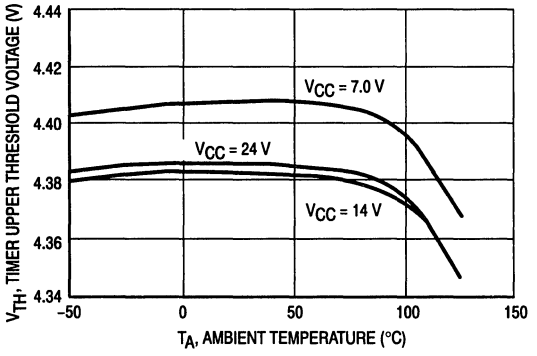

Figure 19. Timer Upper Threshold Voltage versus Supply Voltage

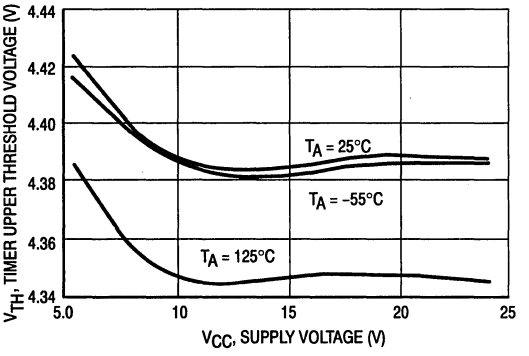

Figure 20. Gate Saturation Voltage versus Gate Current

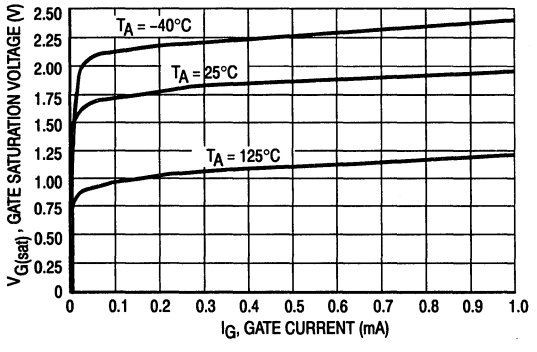

Figure 21. Gate Saturation Voltage versus Gate Current (Expanded Scale)

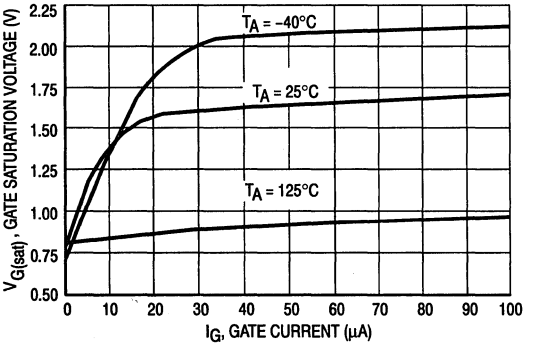

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Figure 22. Gate to Source Voltage versus External R_T Timer Resistor

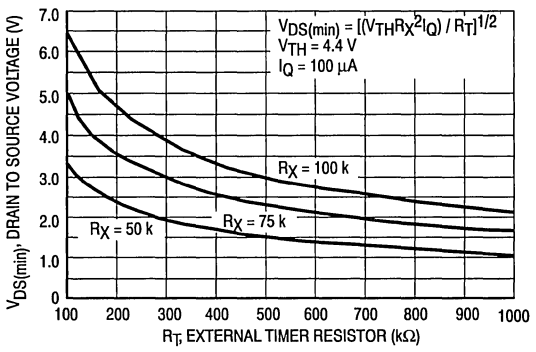


Figure 23. Timer Response versus $V_{DS(min)}/V_{bat}$ Ratio

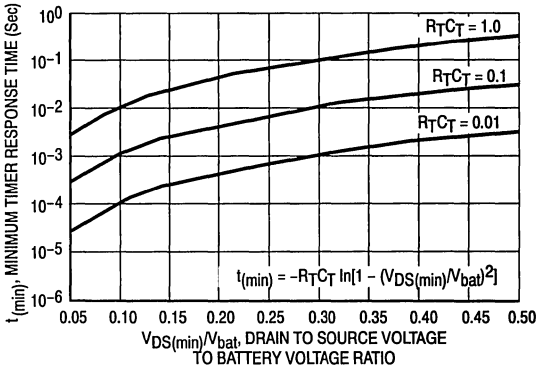
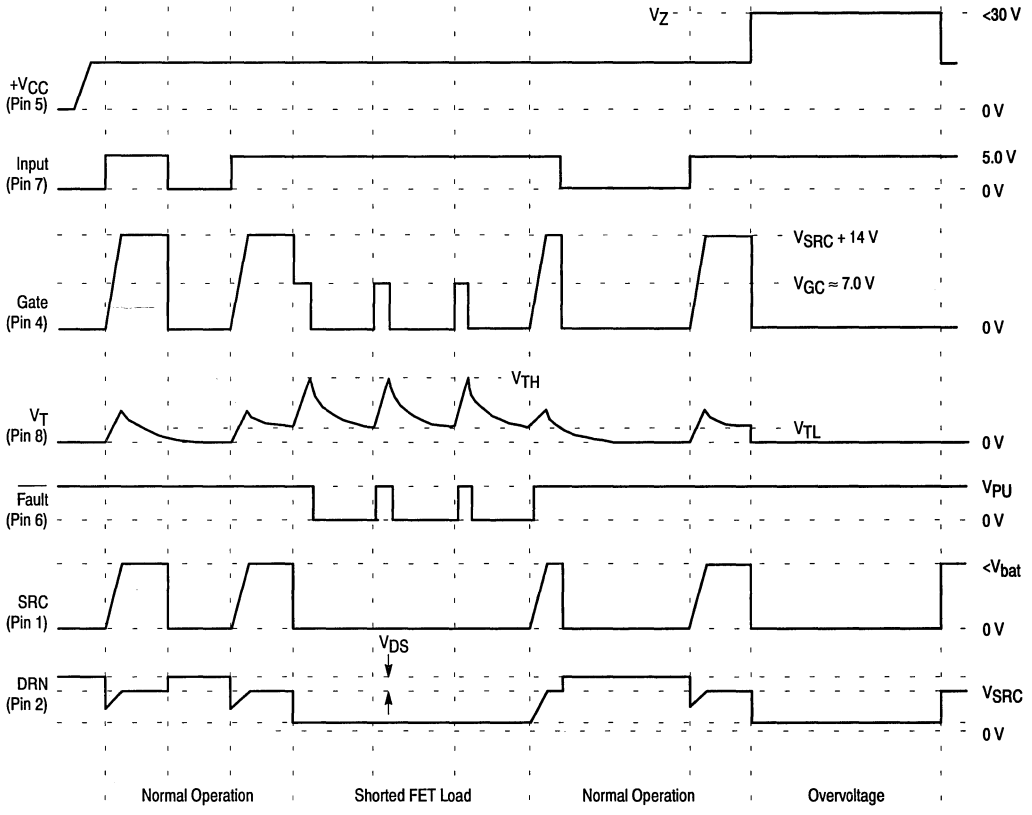


Figure 24. Descriptive Waveform Diagram



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FUNCTIONAL DESCRIPTION

Introduction

The MC33091 is designed to drive a wide variety of N-channel TMOS transistors in high side configured, low frequency switching applications. The MC33091 has an internal charge pump to fully enhance the on-state of the TMOS device. The MC33091 protects the TMOS device from shorts to ground and provides a $\overline{\text{Fault}}$ output to report the presence of an over current condition. The few additional external components required allow tailoring of the application's protection level. The protection scheme of the MC33091 uses an externally programmable, nonlinear timer that disables the TMOS device in the event the drain to source voltage exceeds a specified value for a specified duration. Both the value and duration are externally programmable allowing for flexibility in applications.

Pin Description

Figure 1 shows a typical application as well as the internal functional blocks of the MC33091. The discussion to follow references this figure.

Input (Pin 7): The logic levels of the Input are compatible with CMOS logic families. The Input enables the protection and charge pump circuitry. With the Input in a logic low state the MC33091 draws only leakage current of less than 3.0 μA and in this condition the associated TMOS device will be in the off state. When the Input is in a logic high state, the Gate voltage (Pin 4) rise is limited to a maximum of 14 V above SRC (Pin 1), due to an internal clamp diode being used. Under this condition the TMOS device is enhanced full on.

$\overline{\text{Fault}}$ (Pin 6): The $\overline{\text{Fault}}$ output is comprised of an open collector NPN transistor capable of sinking at least 500 μA when the TMOS gate is disabled due to an over current condition. When the TMOS device experiences an over current condition the $\overline{\text{Fault}}$ pin is pulled low.

SRC (Pin 1): The SRC pin senses the TMOS source voltage and is the input to the V_{DS} buffer used in conjunction with the DRN pin in monitoring the drain to source voltage developed across the TMOS device. The purpose of the 1.0 k resistor connected to this pin is to protect the SRC input from over voltage as a result of flyback voltage produced when the TMOS device is used to switch large inductive loads. This resistor can be eliminated when switching noninductive loads.

DRN (Pin 2): The DRN is used in conjunction with the SRC pin and together constitute a V_{DS} monitor of the TMOS drain to source voltage. Feedback from the SRC pin will maintain a voltage across the resistor, (R_X), equal to the V_{DS} voltage developed across the TMOS device. The series resistor, (R_X), connected between the drain of the TMOS device and DRN of the MC33091 is used in conjunction with the feedback buffer and associated PNP transistor to establish a current proportional to the drain to source voltage, (V_{DS}), of the TMOS device. This proportional current, acted upon by the current squaring circuit of the MC33091, is an important part of the TMOS protection scheme.

V_{CC} (Pin 5): The V_{CC} pin supplies operational power to the MC33091. An internal 30 V zener clamp connects to this pin provide over voltage protection of the MC33091. When the zener is activated, the MC33091 disables the TMOS device only for the duration of the overvoltage but the $\overline{\text{Fault}}$ output (Pin 6) does not change logic states. The $\overline{\text{Fault}}$ pin does not go to a logic low state during the over voltage duration since this is not an MC33091 device fault, but an external system fault.

Gate (Pin 4): The Gate pin of the MC33091 is the output of the internal charge pump which controls the TMOS device. The charge pump is a voltage tripler and requires no additional external components for operation. With the Input in a logic low state the charge pump will be turned off. When the Input is pulled to a logic high state, with no load fault existing, the charge pump turns on and pumps the TMOS gate voltage to at least 8.0 V, typically 10 V to 14 V, above V_{CC} over the supply voltage range. An internal zener clamp is incorporated so as to limit the Gate to approximately 14 V above the source so as to prevent rupture of the TMOS gate.

VT (Pin 8): The Timer Pin (V_T) is both an input to the timer window comparators and an output of the current squaring circuit. An external resistor (R_T) and capacitor (C_T) are tied to this node so as to afford programing the characteristics necessary for protection of the TMOS device.

Over Current Protection Timer

The MC33091 protection scheme is based on the ability of the MC33091 to constantly sense the voltage drop developed across the TMOS device. A low voltage drop is indicative of normal TMOS "on" operation while a large voltage drop represents the existence of an over current condition. By monitoring the TMOS drain to source voltage (V_{DS}) the MC33091 is able to detect a shorted load and react to disable the TMOS device. The circuit protection scheme is essentially based on a timer whose rate is dependent on the magnitude of V_{DS}. If the drain to source voltage is large (i.e. $V_{DS} = V_{CC}$), the timer will disable the gate drive very quickly. If V_{DS} is only slightly above the normal operating level, the timer will take much longer to disable the gate drive.

Since the power dissipated in the TMOS device is proportional to V_{DS}^2, low V_{DS} conditions can be tolerated for a longer time than high V_{DS} conditions. To enhance the system application the timer time-out of the MC33091 is inversely proportional to V_{DS}^2. This approach maximizes the TMOS operating range. The timer parameters are completely user programmable through the use of external components affording application usage of a wide variety of TMOS devices. This is intended to model the generation and dissipation of heat within the TMOS device.

The external components R_X, R_T, and C_T determine the timer characteristics. Once enabled, the MC33091 will source a current, (I_{SQ}), from the timer pin that is proportional to V_{DS}^2 such that:

$$I_{SQ} = KV_{DS}^2 \quad (1)$$

where: $K = 1/(R_X^2 I_Q)$

I_Q is an internal current source parameter of the MC33091 that has a nominal value of 100 µA and R_X is the external resistor in series with the drain of the TMOS device that establishes the value of the voltage to current proportionality constant. Since the parallel combination of R_T and C_T appear at the timer pin (V_T), the timer pin voltage, V_T, can be written as:

$$V_T(t) = I_{SQ}R_T[1-e^{-t/(R_TC_T)}] \quad (2)$$

With the Input (Pin 7) in a logic high state and no over current condition existing, the TMOS device will be in the "on" state. If the TMOS device experiences an over current condition, I_{SQ} flowing through R_T will increase causing C_T to charge up, in turn causing the timer voltage, (V_T), to exceed the threshold, (V_{TH}), of the upper comparator. This sets the latch causing the Q output of the latch to go high (and the $\overline{Q}$ output to go low), in turn causing the TMOS gate and $\overline{Fault}$ output (Pin 6) to be pulled low, disabling the TMOS device. Both the current squaring circuit (I_{SQ}) and the charge pump are disabled whenever the Q output of the latch goes low. Using Equation 2, the fault time response for an over current condition can be written as:

$$t = -R_TC_T\ \ln(1-V_{TH}/I_{SQ}R_T) \quad (3)$$

Using Equation 1 and substituting for ISQ in Equation 3:

$$t = -R_TC_T\ \ln[1-(V_{TH}R_X^2I_Q)/(V_{DS}^2R_T)] \quad (4)$$

When the timer current (I_{SQ}) is disabled, the attained V_{TH} voltage at Pin 8 decays according to the R_TC_T time constant until the V_{TL} threshold of the lower comparator is reached. At this point the latch is reset and the TMOS gate, charge pump and the current squaring circuit are again enabled, again turning on the TMOS device. The MC33091 will repeatedly duty cycle the TMOS gate in this manner so long as the over current condition exists and the input control signal remains in a high logic state. The $\overline{Fault}$ output (Pin 6) will likewise duty cycle.

Consider the case where in Equation 4 the term $(V_{TH}R_X^2I_Q) / (V_{DS}^2R_T) = 1$ such that the time period is undefined. Solving for V_{DS} for this case yields the *minimum* drain to source voltage necessary which will *not* allow V_T to charge to the V_{TH} threshold of the upper comparator. In other words, the TMOS on-time period is infinite which indicative of *no* TMOS over current condition existing. This minimum drain to source voltage for uninterrupted continuous TMOS operation is:

$$V_{DS(min)} = [(V_{TH}R_X^2I_Q)/R_T]^{1/2} = (V_{TH}/KR_T)^{1/2} \quad (5)$$

Under *normal* operating steady state TMOS "on" conditions, R_X and R_T should be chosen such that the upper comparator threshold voltage is *never* reached. This insures the TMOS device will always be in operation so long as the $V_{DS(min)}$ is not exceeded.

The minimum time required for the capacitor C_T to charge up to upper comparator threshold voltage occurs when the TMOS device experiences maximum current (I_{max}). This will occur when the load, and in turn the source, are shorted to ground resulting in the full battery voltage (V_{bat}) to appear directly across the TMOS device. This condition causes maximum I_{SQ} current to be produced by the current squaring circuit. Under this condition the maximum I_{SQ} current experienced is:

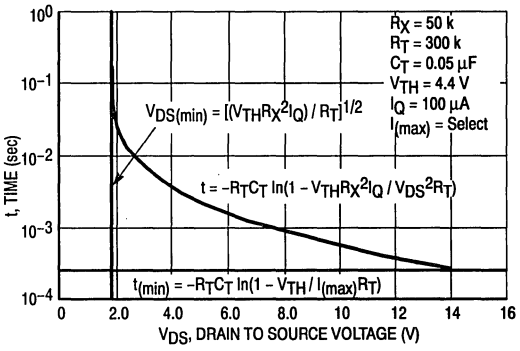
$$I_{SQ(max)} = KV_{bat}^2 = (V_{bat}/R_X)^2/I_Q \quad (6)$$

An expression for the minimum time-out is obtained by substituting I_Q of Equation 6 into Equation 3:

$$t_{(min)} = -R_TC_T\ \ln[1-V_{TH}/(I_{SQ(max)}R_T)] \quad (7)$$

Equation 4 is shown graphically along with the asymptotic limits imposed by Equations 5 and 7 in Figure 25.

Figure 25. Theoretical Fault Time versus V_{DS}



When driving incandescent lamp loads the minimum timer time-out (the time required for the V_T voltage to reach V_{TH} threshold of the upper comparator) should be set long enough so as to *not* allow the inrush current of incandescent lamp to cause a false trigger, yet short enough to afford the TMOS device survival protection against direct shorts under worst case supply and temperature conditions.

10

TMOS Driver Power Dissipation

Under load short conditions, the MC33091 will duty cycle the TMOS gate. The power dissipation in this mode can be significant. For this reason proper heatsinking of the TMOS device is essential as is the selection of compatible external components so as to protect the TMOS device from destruction. In most cases, the heatsink required to handle the TMOS power dissipation under normal operating conditions will be adequate to insure the device survives a short circuit for an indefinite time under worst case conditions.

The MC33091 can protect the TMOS device under a direct load short condition. If the source voltage is less than about 1.5 V above ground, which will normally be the case in the event of a dead short, the MC33091 will clamp the gate to source voltage at 7.0 V. This action will limit the TMOS current and power dissipated under a direct load short condition.

The data sheet for the particular TMOS device being used will normally reveal the current value, $I_{DS(max)}$, to be expected under a dead short condition. TMOS data sheets normally depict graphs of drain current versus drain to source voltage for various gate to source voltages from which the drain current at 7.0 V V_{GS}, $I_{DS(max)}$, can reasonably be approximated. Using this information, the peak TMOS power dissipation under a dead short condition is approximated to be:

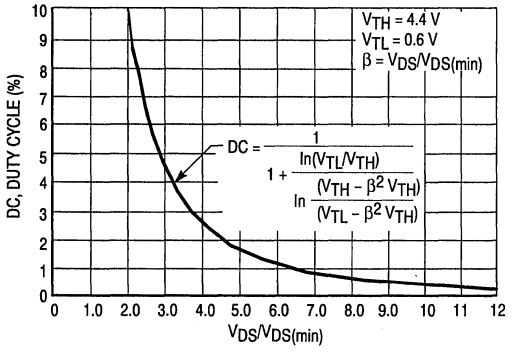
$$P_{D(peak)} = V_{bat(max)} I_{DS(max)} \quad (8)$$

The average power is equal to the peak power dissipation multiplied by the duty cycle (DC):

$$P_{D(avg)} = P_{D(peak)} DC \quad (9)$$

As long as the average power, in Equation 9, is less than the maximum power dissipation of the TMOS device under normal conditions, the short circuit protection scheme of the MC33091 will adequately protect the TMOS device. The duty cycle at which the MC33091 controls the gate can be determined by using Figure 26.

Figure 26. MC33091 Duty Cycle versus V_{DS} / $V_{DS(min)}$



As previously discussed, I_{SQ} is externally dependant on the sensed V_{DS} voltage developed across the TMOS device and R_X in accordance with Equations 1 and 2. At the onset of an overload condition, the voltage across C_T will be less than the V_{TH} threshold voltage of the upper comparator with the TMOS device in an "on" state. I_{SQ} current will increase dramatically and the timing capacitor C_T charges toward V_{TH}. When the voltage on C_T reaches the V_{TH} threshold voltage of the upper comparator, the upper comparator output goes high setting the latch output (Q) high, turning on the open collector NPN transistor and pulling the $\overline{\text{Fault}}$ output low. At the same time, I_{SQ} is switched off allowing C_T to discharge through resistor R_T to V_{TL}, at which time the TMOS device is again switched on. This action is repeated so long as the overload condition exists. The V_{TL} and V_{TH} thresholds are internally set to approximately 0.6 V and 4.4 V respectively. The charge time (t_c) of C_T can be shown as:

$$t_c = -R_T C_T \ln[1-(V_{TH}-V_{TL})/(I_{SQ}R_T-V_{TL})] \quad (10)$$

The discharge time (t_d) of C_T can be shown as:

$$t_d = -R_T C_T \ln(V_{TL}/V_{TH}) \quad (11)$$

The duty cycle is defined as charge time divided by the charge plus discharge time and represented by:

$$DC = t_c/(t_c+t_d) \quad (12)$$

Substituting Equations 10 and 11 into 12: (13)

$$DC = 1/1+\ln(V_{TL}/V_{TH})/\ln\{(V_{TH}-\beta^2 V_{TH})/(V_{TL}-\beta^2 V_{TH})\}$$

where: $\beta = V_{DS}/V_{DS(min)}$

Notice the duty cycle is dependent *only* on the ratio of the drain to source voltage, (V_{DS}), of the TMOS device to the minimum drain to source voltage ($V_{DS(min)}$), allowing uninterrupted continuous TMOS operation as calculated in Equation 5. A graph of Equation 13 is shown in Figure 26 and is valid for any ratio of V_{DS} to $V_{DS(min)}$. Knowing this ratio, the duty cycle can be determined by using Figure 26 or Equation 13 and knowing the duty cycle, the average power dissipation can be calculated by using Equation 9.

If the TMOS device experiences a hard load short to ground a minimum duty cycle will be experienced which can be calculated. When this condition exists, the TMOS device experiences a V_{DS} voltage of V_{bat} which is sensed by the MC33091. The MC33091 very rapidly charges the timing capacitor C_T to V_{TH} shutting down the TMOS device. This condition produces the minimum duty cycle for the specific system conditions. The minimum duty cycle can be calculated for any valid V_{bat} voltage by substituting the value of V_{bat} used for V_{DS} in Equation 13 and solving for the duty cycle.

Knowing the duty cycle and peak power allows determination of the average power as was pointed out in Equation 9. TMOS data sheets specify the maximum allowable junction temperature and thermal resistance, junction to case, at which the device may be operated. Knowing the average power and the device thermal information, proper heatsinking of the TMOS device can be determined.

The duty cycle graph (Figure 26) reveals lower values of $V_{DS(min)}$ produce shorter duty cycles, for a given V_{DS} voltages. The minimum duty cycle, being limited to the case where $V_{DS} = V_{bat}$, increases as higher values of V_{bat} are used.

APPLICATION

The following design approach will simplify application of the MC33091 and will insure the components chosen to be optimal for a specific application.

1. Characterize the load impedance and determine the maximum load current possible for the load supply voltage used.

2. Select a TMOS device capable of handling the maximum load current. Though the MC33091 will equally drive our competitors products, it is hoped you will select one of the many TMOS devices listed in Motorola's *TMOS Power MOSFET Selector Guide/Cross Reference*, (SG56/D).

3. Determine the maximum steady state V_{DS} voltage the TMOS device will experience under *normal* operating conditions. Typically, this is the maximum load current multiplied by the specified $r_{DS(on)}$ of the TMOS device. Junction temperature considerations should be taken into account for the $r_{DS(on)}$ value since it is significantly temperature dependent. Normally, TMOS data sheets depict the affect of junction temperature on $r_{DS(on)}$ and an $r_{DS(on)}$ value at some considered maximum junction temperature should be used. Various graphs relating to $r_{DS(on)}$ are depicted in Motorola TMOS data sheets. Though Motorola TMOS devices typically specify a maximum allowable junction temperature of 150°C, in a practical sense, the user should strive to keep junction temperature as low as possible so as to enhance the applications long term reliability. The maximum steady state V_{DS} voltage the TMOS device will experience under *normal* operating conditions is thus:

$$V_{DS(norm)} = I_{L(max)}r_{DS(on)} \quad (14)$$

4. Calculate the maximum power dissipation of the TMOS device under *normal* operating conditions:

$$P_{D(max)} = V_{DS(on)}I_{L(max)} \quad (15)$$

5. The calculated maximum power dissipation of the TMOS device dictates the required thermal impedance for the application. Knowing this, the selection of an appropriate heatsink to maintain the junction temperature below the maximum specified by the TMOS manufacture for operation can be made. The required overall thermal impedance is:

$$TR_{JA} = (T_{J(max)} - T_{A(max)})/P_{D(max)} \quad (16)$$

Where $T_{J(max)}$, the maximum allowable junction temperature, is found on the TMOS data sheet and $T_{A(max)}$, the maximum ambient temperature, is dictated by the application itself.

6. The thermal resistance (TR_{JA}), represents the maximum overall or total thermal resistance, from junction to the surrounding ambient, allowable to insure the TMOS manufactures maximum junction temperature will not be exceeded. In general, this overall thermal resistance can be considered as being made up of several separate minor thermal resistance interfaces comprised of TR_{JC}, TR_{CS}, and TR_{SA} such that:

$$TR_{JA} = TR_{JC} + TR_{CS} + TR_{SA} \quad (17)$$

Where TR_{JC}, TR_{CS}, and TR_{SA} represent the junction-to-case, case-to-heatsink, and heatsink-to-ambient thermal resistances respectively. TR_{CS} and TR_{SA} are the only parameters the device user can influence.

The case-to-heatsink thermal resistance (TR_{CS}) is material dependent and can be expressed as:

$$TR_{CS} = \rho \bullet t/A \quad (18)$$

Where "ρ" is the thermal resistivity of the heatsink material (expressed in °C/W unit thickness), "t" is the thickness of heatsink material, and "A" is the contact area of the case to heatsink. Heatsink manufactures specify the value of TR_{CS} for standard heatsinks. For nonstandard heatsinks, the user is required to calculate TR_{CS} using some form of the basic Equation 18.

The required heatsink-to-ambient thermal resistance (TR_{SA}) can easily be calculated once the terms of Equation 17 are known. Substituting TR_{JA} of Equation 16 into Equation 17 and solving for TR_{SA} produces:

$$TR_{SA} = (T_{J(max)}-T_{A(max)})/P_{D(max)}-(TR_{JC}+TR_{CS}) \quad (19)$$

Consulting the heatsink manufactures catalog will provide TR_{CS} information for various heatsinks under various mounting conditions so as to allow easy calculation of TR_{SA} in units of °C/W (or when multiplied by the power dissipation produces the heatsink mounting surface temperature rise). Furthermore, heatsink manufactures typically specify for various heatsinks, heatsink efficiency in the form of mounting surface temperature rise above the ambient conditions for various power dissipation levels. The user should insure that the heatsink selected will provide a surface temperature rise somewhat less than the maximum capability of the heatsink so as to insure the device junction temperature will not be exceeded. The user should consult the heatsink manufacturers catalog for this information.

7. Set the value of $V_{DS(min)}$ to something greater than the *normal operating* drain to source voltage, $V_{DS(norm)}$, the TMOS device will experience as calculated in Step 3 above (Equation 14). From a practical standpoint, a value twice the $V_{DS(norm)}$ expected under normal operation will prove to be a good starting point for $V_{DS(min)}$.

8. Select a value of R_T less than 1.0 MΩ for minimal timing error whose value is compatible with R_X, (R_X will be selected in Step 9 below). A recommended starting value to use for R_T would be 470 k. The consideration here is that the input impedance of the threshold comparators are approximately 10 MΩ and if R_T values greater than 1.0 MΩ are used, significant timing errors may be experienced as a result of input bias current variations of the threshold comparators.

9. Select a value of R_X which is compatible with R_T. The value of R_X should be between 50 k and 100 k. Recall in Equation 5 that $V_{DS(min)}$ was determined by the combined selection of R_X and R_T. Low values of R_X will give large values for K ($K = 4.0\ \mu A/V^2$ for R_X = 50 k) causing I_{SQ} to be very sensitive to V_{DS} variations (see Equation 1). This is desirable if a minimum V_{DS} trip point is needed in the 1.0 V range since small V_{DS} values will generate measurable currents. However, at high V_{DS} values, TMOS device currents become excessively large and the current squaring function begins to deviate slightly from the predicted value due to high level injection effects occurring in the output PNP of the current squaring circuit. These effects can be seen when I_{SQ} exceeds several hundred microamps.

10. Calculate the shorted load average power dissipation for the application using Equations 8 and 9. This involves determining the peak shorted load power dissipation of the TMOS device and gate duty cycle. The duty cycle is based on $V_{DS(min)}$, the value of V_{DS} under shorted conditions (i.e. $V_{bat(max)}$).

11. The calculated shorted load average power dissipation of Step 10 should be less than the maximum power dissipation under *normal* operating conditions calculated in Step 4. If this is not the case, there are two options.

Option one is to reduce the thermal resistance of the TMOS device heatsink, in other words, use a larger or better heatsink. This though, is not always practical to do particularly if restricted by size.

Option two is to set $V_{DS(min)}$ to the lowest practical value. If for instance $V_{DS(min)}$ is set to 4.0 V when only 2.0 V are needed, the short circuit duty cycle will be over twice as large, resulting in double the TMOS device power dissipated. Keeping $V_{DS(min)}$ to a minimum, reduces the shorted load average power.

12. Choose a value of C_T. The value of C_T can be determined either by trial and error or by characterizing the V_{DS} waveform for the load and selecting a capacitor value that generates a minimum fault time curve (see Equation 4) that encompasses the V_{DS} versus time waveform. The value of C_T has *no* effect on the duty cycle itself as was pointed out earlier. See Figure 23 for a graphical selection of C_T.

Inductive Loads

The TMOS device is turned off by pulling the gate to near ground potential. Turning off an inductive load will cause the source of the TMOS device to go below ground due to flyback voltage to the point where the TMOS device may become biased on again allowing the inductive energy to be dissipated through the load. There is an internal 14 V zener diode clamp from the gate to source pin which will limit how far the source pin can be pulled below ground. For high inductive loads, it may be necessary to have an external 10 k current limiting resistor in series with the source pin to limit the clamp current in the event the source pin is pulled more than 14 V below ground.

Transient Faults

The MC33091 is not able to withstand automotive voltage transients directly. However, by correctly sizing resistor R_S and capacitor C_S, the MC33091 can withstand load dump and other automotive type transients. The V_{CC} voltage is clamped at approximately 30 V through the use of an internal zener diode.

Under reverse battery conditions, the load will be energized in reverse due to the parasitic body diode inherent in the TMOS device. Under this condition, the drain is grounded and the MC33091 clamps the gate at 0.7 V below the battery potential. This turns the TMOS device on in reverse and minimizes the voltage across the TMOS device resulting in minimal power dissipation. Neither the MC33091 nor the TMOS device will be damaged under such a condition. In addition, if the load can tolerate a reverse polarity, the load will not be damaged. Some sensitive applications may not tolerate a reverse polarity load condition with reverse battery polarity.

There is no protection of the TMOS device during a reverse battery condition if the load itself is already shorted to ground. The MC33091 will not incur damage under this specialized reverse battery condition but the TMOS device may be damaged since there could be significant energy available from the battery to be dissipated in the TMOS device.

The MC33091 will withstand a maximum V_{CC} voltage of 28 V and with the proper TMOS device used, the system can withstand a double battery condition.

Figure 32 depicts a method of protecting the FET from positive transient voltages in excess of the rated FET breakdown voltage. The zener voltage, in this case, should be less than the FET breakdown voltage. The diode D is necessary where reverse battery protection is required to protect the gate of the FET.

EMI Concern

The gate capacitance and thus the size of the TMOS device used will determine the turn-on and turn-off times experienced. In a practical sense, smaller TMOS devices have smaller gate capacitances and give rise to higher slew rates. By way of example, the slew rate of an MPT50N06 TMOS device might be of the order of 7.5 µs while that of an MPT8N10 is 23 µs (see Figure 13). The slew rate, or speed of turn-on or turn-off can be calculated by assuming the charge pump to supply approximately 100 µA over the time the gate capacitance will transition a V_{GS} voltage of 0 V to 10 V. In reality, the V_{GS} voltage will be greater than 10 V but the additional increase in TMOS drain current will be minimal for V_{GS} voltages greater than 10 V.

Sizing of the charge pump current is such that slew rate need not be of concern in all but the most critical of applications. Where limiting of EMI is of concern, the charge pump of the MC33091 may be slew rate limited by adding an external feedback capacitor from the gate to source of the TMOS device for slow down adjustment of both turn-on and turn-off times (see Figure 29). Figures 27 through 31 depict various methods of modifying the turn-on or turn-off times.

Figure 31 depicts a method of using only six external components to decrease turn-off time and clamp the flyback voltage associated with inductive loads. $V_{GS(th)}$ used in the critical component selection criteria refers to the gate to source threshold voltage of the FET used in the application.

Caution should be exercised when slowing down the switching transition time since doing so can greatly increase the average power dissipation of the TMOS device. The resulting increase in power dissipation should be taken into account when selecting the R_TC_T time constant values in order to protect the TMOS device from any over current condition.

Figure 27. Slow Down FET Turn-On

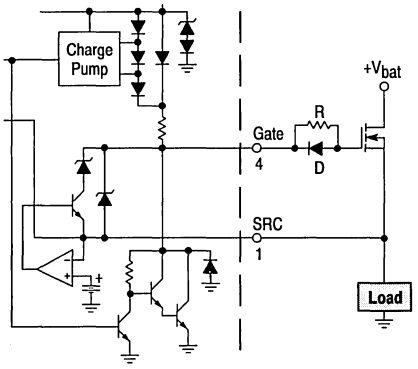


Figure 28. Slow Down FET Turn-Off

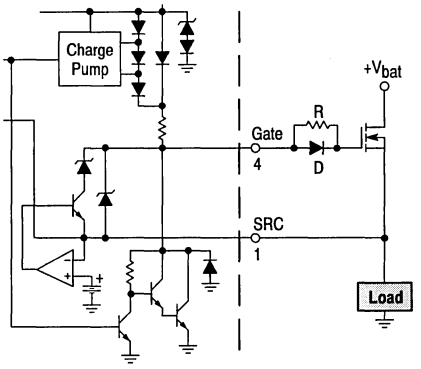


Figure 29. Slow Down Turn-On and Turn-Off of FET

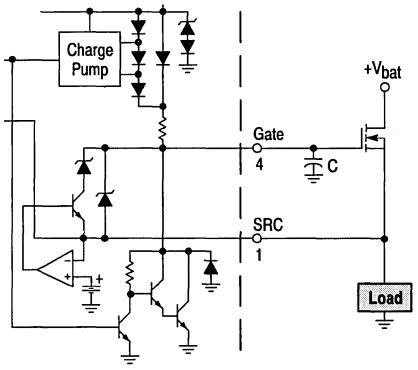


Figure 30. Independent Slow Down Adjustment of FET Turn-On and Turn-Off

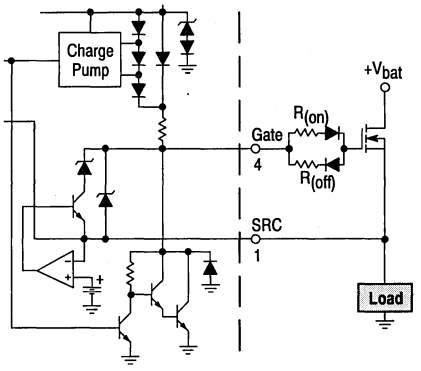


Figure 31. Decreased FET Turn-Off Time With Inductive Flyback Voltage Clamp

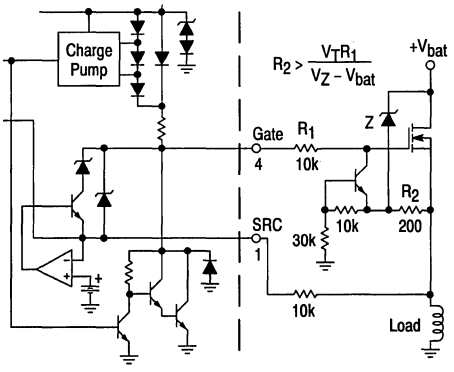
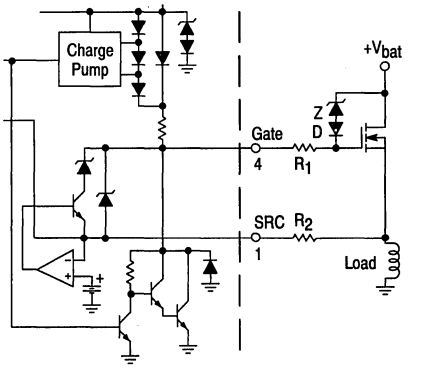


Figure 32. Overvoltage Protection of FET



10

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC33092

Advance Information

Alternator Voltage Regulator

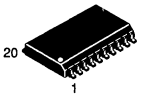
ALTERNATOR REGULATOR

SILICON MONOLITHIC INTEGRATED CIRCUIT

The MC33092 is specifically designed for voltage regulation and Load Response Control (LRC) of diode rectified alternator charging systems, as commonly found in automotive applications. The MC33092 provides load response control of the alternator output current to eliminate engine speed hunting and vibration due to sudden electrical loads which cause abrupt torque loading of the engine at low RPM. Two load response rates are selectable using Pin 11. The timing of the response rates is dependent on the oscillator frequency.

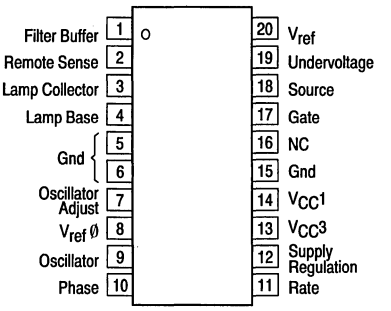
In maintaining system voltage, the MC33092 monitors and compares the system battery voltage to an externally programmed set point value and pulse width modulates an N-channel MOSFET transistor to control the average alternator field current.

- Forced Load Response Control (LRC) with Heavy Load Transitions at Low RPM
- Capable of Regulating Voltage to ± 0.1 V @ 25°C
- Operating Frequency Selectable with One External Resistor
- < 0.1 V Variation over Speed Range of 2000 to 10,000 RPM
- < 0.4 V Variation over 10% to 95% of Maximum Alternator Output
- Maintains Regulation with External Loads as Low as 1.0 A
- Load Dump Protection of Lamp, Field Control Devices, and Loads
- Duty Cycle Limit Protection
- Provides High Side MOSFET Control of a Ground Referenced Field Winding
- Controlled MOSFET and Flyback Diode Recovery Characteristics for Minimum RFI
- < 2.0 mA Standby Current from Battery @ 25°C
- < 3.0 mA Standby Current from Battery Over Temperature Range
- Optional 2.5 or 10 sec. LRC Rate Control (Osc. Freq. = 280 kHz)
- Undervoltage, Overvoltage and Phase Fault (Broken Belt) Detection



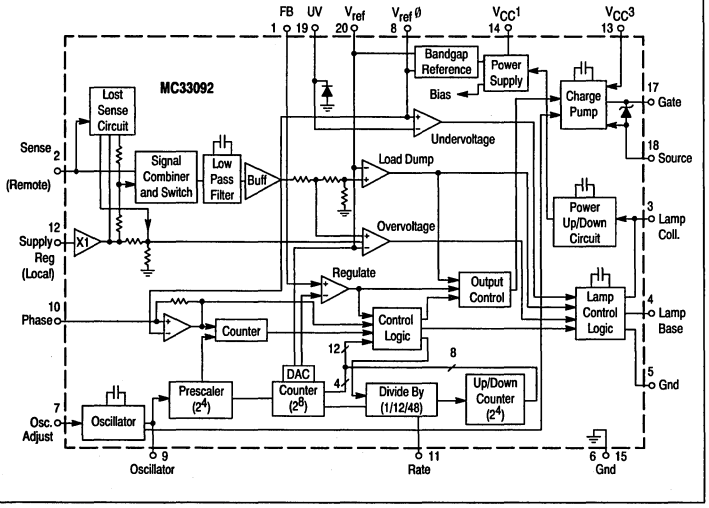
DW SUFFIX
PLASTIC PACKAGE
CASE 751D
(SO-20L)

PIN CONNECTIONS



(Top View)

Simplified Block Diagram



ORDERING INFORMATION

Device	Temperature Range	Package
MC33092DW	– 40° to +125°C	SO-20L

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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage Load Dump Transient Voltage (Note 1) Negative Voltage (Note 2)	V_{bat} $+V_{max}$ $-V_{min}$	24 40 – 2.5	V V V
Power Dissipation and Thermal Characteristics Maximum Power Dissipation @ T_A = 125°C Thermal Resistance, Junction to Ambient	 P_D $R_{\theta JA}$	 867 75	 mW °C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature Range	T_A	– 40 to +125	°C
Storage Temperature Range	T_{stg}	– 45 to +150	°C

ELECTRICAL CHARACTERISTICS (External components per Figure 1, T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC CHARACTERISTICS					
Regulation Voltage (Determined by external resistor divider)	V_{Reg}	—	14.85	—	V
Regulation Voltage Temperature Coefficient	T_C	–13	–11	– 9.0	mV/°C
Suggested Battery Voltage Operating Range	V_{bat}	11.5	14.85	16.5	V
Power Up/Down Threshold Voltage (Pin 3)	V_{PWr}	0.5	1.2	2.0	V
Standby Current, V_{bat} = 12.8 V, Ignition off, T_A = 25°C V_{bat} = 12.8 V, Ignition off, – 40°C≤T_A≤125°C	 I_{Q1} I_{Q2}	 — —	 1.3 —	 2.0 3.0	 mA mA
Zero Temperature Coefficient Reference Voltage, (Pin 8)	V_{ref} ∅	1.1	1.25	1.4	V
Band Gap Reference Voltage (Pin 20)	V_{ref}	1.7	2.0	2.3	V
Band Gap Reference Temperature Coefficient	TC	–13	–11	– 9.0	mV/°C
Sense Loss Threshold (Pin 2)	$S_{Loss(th)}$	—	0.6	1.0	V
Phase Detection Threshold Voltage (Pin 10)	P_{Th}	1.0	1.25	1.5	V
Phase Rotation Detection Frequency (Pin 10)	P_{Rot}	—	36	—	Hz
Undervoltage Threshold (Pin 19)	V_{UV}	1.0	1.25	1.5	V
Overvoltage Threshold (Pin 2, or Pin 12 if Pin 2 is not used)	V_{OV}	1.09(V_{ref})	1.12(V_{ref})	1.16(V_{ref})	V
Load Dump Threshold (Pin 2, or Pin 12 if Pin 2 is not used)	V_{LD}	1.33(V_{ref})	1.4(V_{ref})	1.48(V_{ref})	V
SWITCHING CHARACTERISTICS					
Fundamental Regulation Output Frequency, (Pin 17) (Clock oscillator frequency divided by 4096)	f	—	68	—	Hz
Suggested Clock Oscillator Frequency Range, (Pin 9) (Determined by external resistor, R_T, see Figure 6)	f_{osc}	205	280	350	kHz
Duty Cycle, (Pin 17) At Start-up During Overvoltage Condition	 $Start_{DC}$ OV_{DC}	 27 3.5	 29 4.7	 31 5.5	 % %
Low/High RPM Transition Frequency, (Pin 10)	LRC_{Freq}	247	273	309	Hz
LRC Duty Cycle Increase Rate Low RPM Mode (LRC_{Freq} < 247 Hz), Pin 11 = Open (Slow Rate) Low RPM Mode (LRC_{Freq} < 247 Hz), Pin 11 = Grounded (Fast Rate) High RPM Mode (LRC_{Freq} > 309 Hz), Pin 11 = Don't Care (LRC Mode is disabled)	 LRC_S LRC_F LRC_H	 8.5 34 409	 9.5 38 455	 10.5 42 501	 %/sec %/sec %/sec

NOTES: 1. 125 ms wide square wave pulse.
2. Maximum time = 2 minutes.

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Figure 1. MC33092 Typical Application Diagram

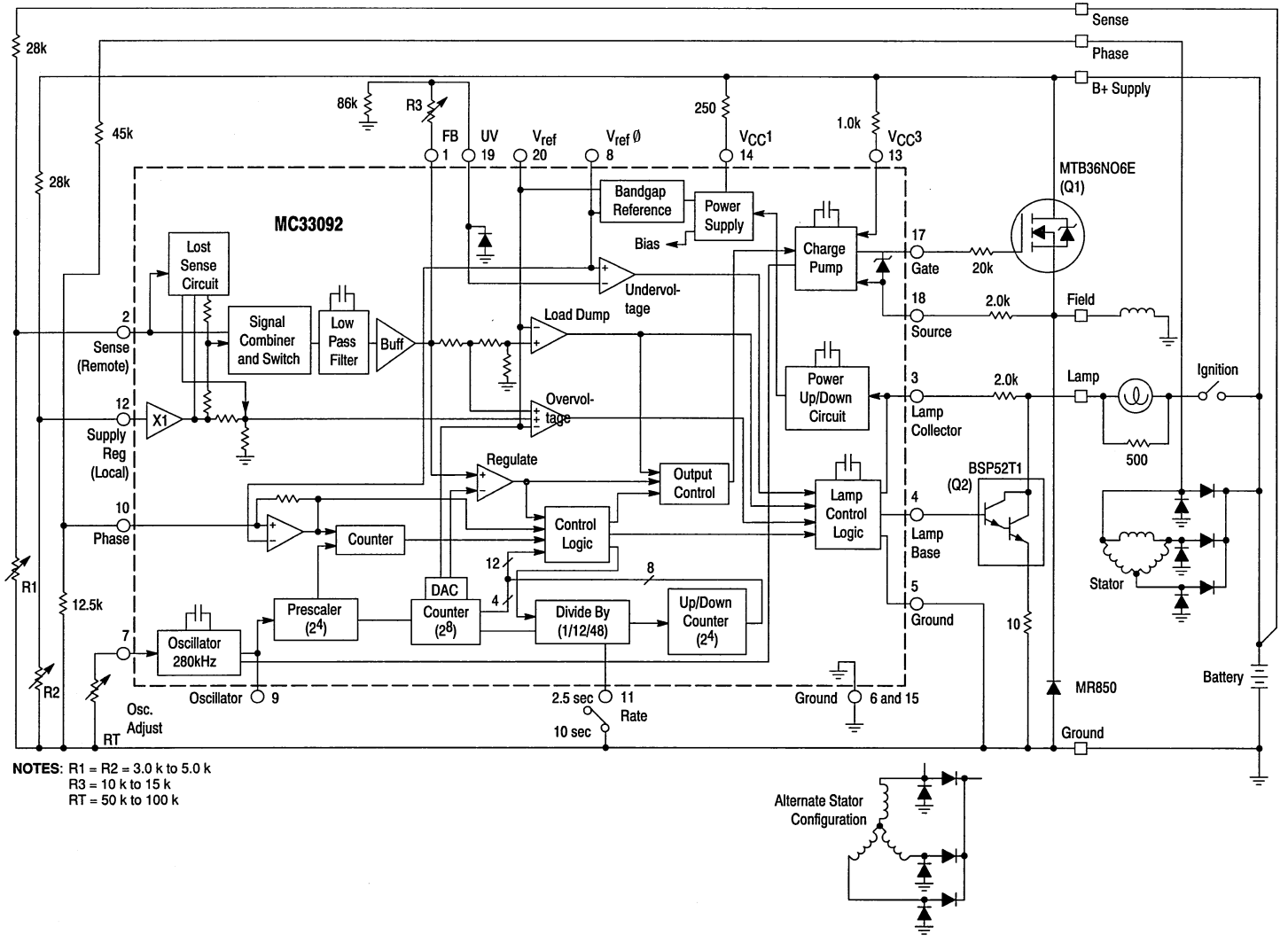


Figure 2. Standby Current versus Temperature

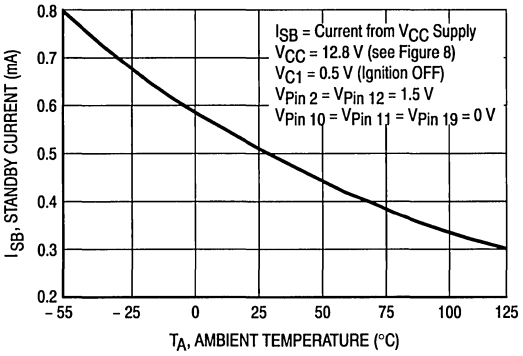


Figure 3. Turn-On Voltage versus Temperature

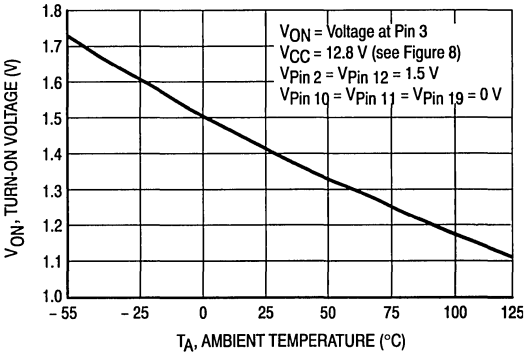


Figure 4. Reference Voltage versus Temperature

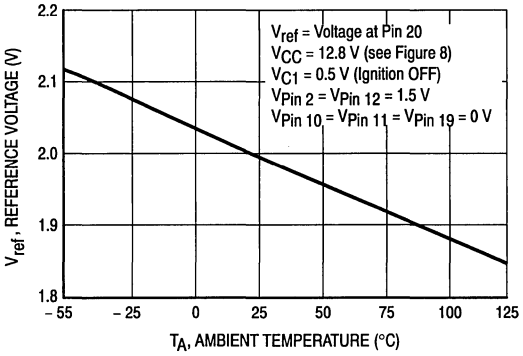


Figure 5. 0TC Reference Voltage versus Temperature

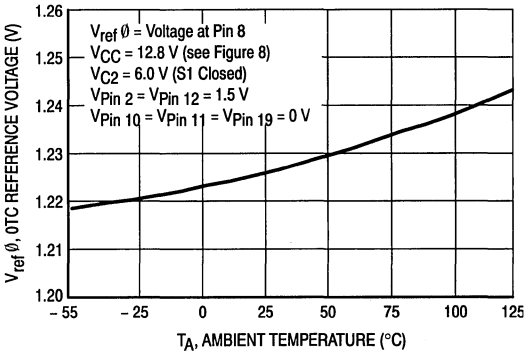


Figure 6. Oscillator Frequency versus Timing Resistor

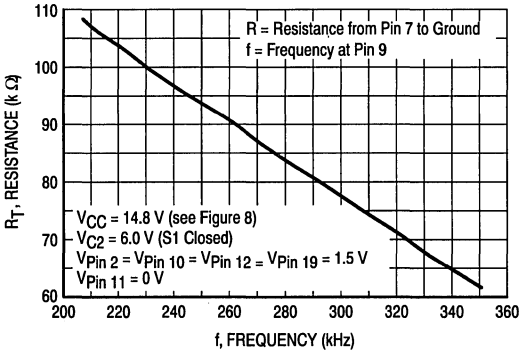
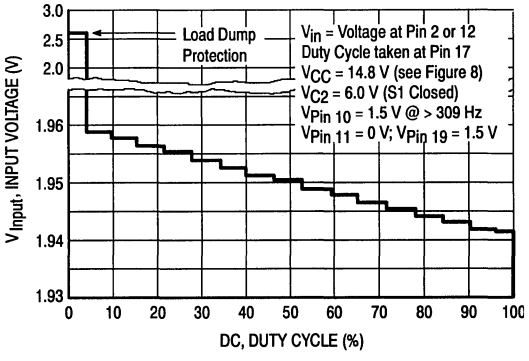


Figure 7. Input Voltage versus Output Duty Cycle



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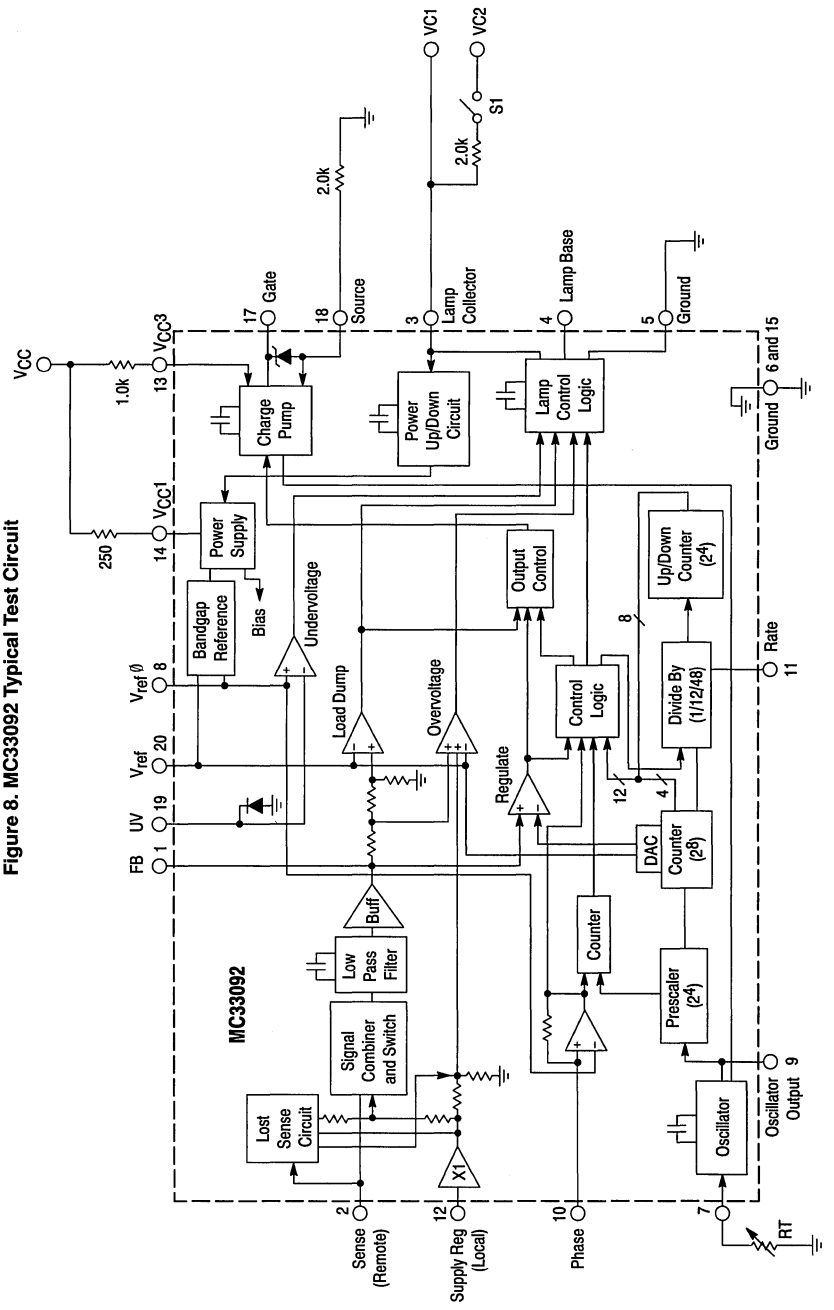

Figure 8. MC33092 Typical Test Circuit

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PIN FUNCTION DESCRIPTION

Pin No.	Function	Description
1	FB	This pin provides a filtered result of the Sense input (if the Sense input is used) or the Supply Regulation input (if the Sense input is not used).
2	Sense	The Sense input is a remote (Kelvin), low current battery voltage reference input used to give an accurate representation of the true battery voltage. This input is also used to monitor overvoltage or load dump conditions.
3	Lamp Collector and Power-Up/Down	This pin connects to the collector of the transistor (Q2) used to drive the fault lamp. It is also used to sense a closed ignition switch (voltage sense) which then turns on power to the IC.
4	Lamp Base	The Lamp Base pin provides base current to the fault lamp drive transistor (Q2).
5	Ground	Grounded to provide a ground return for the fault lamp control logic circuit.
6, 15	Ground	IC ground reference pins.
7	Oscillator Adjust	A resistor to ground on this pin adjusts the internal oscillator frequency, see Figure 6.
8	* $V_{ref\emptyset}$	This is a test point for the 1.1 V to 1.4 V reference voltage. It has a zero temperature coefficient. The reference is used internally for phase signal and undervoltage detection.
9	* Oscillator	Test point for checking the operation of the internal oscillator.
10	Phase	The Phase input detects the existence of a magnetic field rotating within the alternator.
11	Rate	The Rate pin is used to select a slow mode (floating) or fast mode (ground) Load Response Control recovery rate.
12	Supply Regulation	The voltage on the Supply Regulation pin is used as a representation of the alternator output voltage. This input also used to monitor overvoltage or load dump conditions.
13	$V_{CC}3$	Positive supply for the internal Charge Pump.
14	$V_{CC}1$	Positive supply for the entire IC except for the Charge Pump.
15, 6	Ground	Ground reference for the IC.
16	N/C	No connection.
17	Gate	Controls the Gate of the MOSFET used to energize the field winding.
18	Source	Field winding control MOSFET source reference.
19	Undervoltage	If the voltage at this pin goes below 1.0 V, the fault lamp is guaranteed to turn on. The IC will continue to function, but with limited performance.
20	* V_{ref}	Test point for the 1.7 V to 2.3 V Bandgap reference voltage. This voltage has a negative temperature coefficient of approximately –11 mV/°C.

***NOTE:** Pins 8, 9 and 20 are test points only.

APPLICATION CIRCUIT DESCRIPTION

Introduction

The MC33092, designed to operate in a 12 V system, is intended to control the voltage in an automotive system that uses a 3 phase alternator with a rotating field winding. The system shown in Figure 1 includes an alternator with its associated field coil, stator coils and rectifiers, a battery, a lamp and an ignition switch. A tap is connected to one corner of the stator windings and provides an AC signal for rotation (phase) detection.

A unique feature of the MC33092 is the Load Response Control (LRC) circuitry. The LRC circuitry is active when the stator winding AC signal frequency (phase buffer input signal, Pin 10) is lower than the Low/High RPM transition frequency. When active, the LRC circuitry dominates the basic analog control circuitry and slows the alternator response time to sudden increases in load current. This prevents the alternator from placing a sudden, high torque load on the automobile engine when a high current accessory is switched on.

The LRC circuitry is inactive when the stator winding AC signal frequency is higher than the Low/High RPM transition frequency. When the LRC circuitry is inactive, the basic analog control circuitry controls the alternator so it will supply a constant voltage that is independent of the load current.

Both the LRC and analog control circuits control the system voltage by switching ON and OFF the alternator field current using Pulse Width Modulation (PWM). The PWM approach controls the duty cycle and therefore the average field current. The field current is switched ON and OFF at a fixed frequency by a MOSFET (Q1) which is driven directly by the IC. The MC33092 uses a charge pump to drive the MOSFET in a high side configuration for alternators having a grounded field winding.

A fault detector is featured which detects overvoltage, undervoltage, slow rotation or non-rotation (broken alternator belt) conditions and indicates them through a fault lamp drive output (Pin 4).

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A Load Dump protection circuit is included. During a load dump condition, the MOSFET gate drive (Pin 17) and the fault lamp drive output are disabled to protect the MOSFET, field winding and lamp.

Power-Up/Down

Power is continuously applied to the MC33092 through $V_{CC}1$ and $V_{CC}3$. A power-up/down condition is determined by the voltage on the Lamp Collector pin (Pin 3). When this voltage is below 0.5 V the IC is guaranteed to be in a low current standby mode. When the voltage at Pin 3 is above 2.0 V, the IC is guaranteed to be fully operational. The power-up voltage is applied to Pin 3 via the ignition switch and fault lamp. In case the fault lamp opens, a 500 Ω bypass resistor should be used to ensure regulator IC power-up.

A power-up reset circuit provides a reset or set condition for all digital counter circuitry. There is also a built-in power-up delay circuit that protects against erratic power-up signals.

Battery and Alternator Output Voltage Sensing

The battery and the alternator output voltage are sensed by the remote (Sense, Pin 2), and the local (Supply Reg., Pin 12) input buffer pins, respectively, by way of external voltage dividers. The regulated system voltage is determined by the voltage divider resistor values.

Normally the remote pin voltage determines the value at which the battery voltage is regulated. In some cases the remote pin is not used. When this condition ($V_{Pin\ 2} < 0.6$ V typically) exists, a sense loss function allows the local pin voltage to determine the regulated battery voltage with no attenuation of signal. If, however, when the remote pin is used, and the voltage at this pin is approximately 25% less than the voltage at the local sense pin (but greater than 0.6 V, typically), the value at which the battery voltage is regulated is switched to the local sense pin voltage (minus the 25%). The signal combiner/switch controls this transfer function.

Low Pass Filter, DAC & Regulator Comparator

The output of the combiner/switch buffer feeds a low pass filter block to remove high frequency system noise. The filter output is buffered and compared by the regulator comparator to a descending ramp waveform generated by an internal DAC. When the two voltages are approximately equal, the output of the regulator comparator changes state and the gate of the MOSFET is pulled low (turned OFF) by the output control logic for the duration of the output frequency clock cycle. At the beginning of the next output clock cycle, the DAC begins its descending ramp waveform and the MOSFET is turned ON until the regulator comparator output again changes state. This ongoing cycle constitutes the PWM technique used to control the system voltage.

Oscillator

The oscillator block provides the clock pulses for the prescaler-counter chain and the charge control for the charge pump circuit. The oscillator frequency is set by an external resistor from Pin 7 to ground as presented in Figure 6.

The prescaler-counter divides the oscillator frequency by 2^{12} (4096) and feeds it to the output control logic and divider-up/down counter chain. The output control logic uses it as the fundamental regulation output frequency (Pin 17).

Load Response Control

The Load Response Control (LRC) circuit generates a digital control of the regulation function and is active when the stator output AC signal (Pin 10) frequency is lower than the Low/High RPM transition frequency. The LRC circuit takes the output signal of the prescaler-counter chain and with a subsequent divider and up/down counter to provide delay, controls the alternator response time to load increases on the system. The response time is pin programmable to two rates. Pin 11 programs the divider to divide by 12 or divide by 48. If Pin 11 is grounded, the signal fed to the up/down counter is divided by 12 and the response time is 12 times slower than the basic analog response time. If Pin 11 is left floating, the signal to the up/down counter is divided by 48 and the response time is 48 times slower.

The basic analog (LRC not active) and digital duty cycle control (LRC active) are OR'd such that either function will terminate drive to the gate of the MOSFET device with the shortest ON-time, i.e., lower duty cycle dominating.

The digital ON-time is determined by comparing the output of the up/down counter to a continuous counter and decoding when they are equal. This event will terminate drive to the MOSFET. A count direction shift register requires three consecutive clock pulses with a state change on the data input of the register to result in an up/down count direction change. The count will increase for increasing system load up to 100% duty cycle and count down for decreased loading to a minimum of 29% duty cycle. The analog control can provide a minimum duty cycle of 4 to 5%. The initial power-up duty cycle is 29% until the phase comparator input exceeds its input threshold voltage. Also, the IC powers up with the LRC circuit active, i.e., when the Lamp Collector pin exceeds the power-up threshold voltage.

Fault Lamp Indicator

Pins 3 and 4 control the external Darlington transistor (Q2) that drives the fault indicator lamp. A 10 Ω resistor should be placed in series with the transistor's emitter for current limiting purposes. The fault lamp is energized during any of the following fault conditions: 1) No Phase buffer (Pin 10) input due to slow or no alternator rotation, shorted phase winding, etc.; 2) Phase buffer input AC voltage less than the phase detect threshold; 3) Overvoltage on Pin 2, or Pin 12 if Pin 2 is not used, or 4) Undervoltage on Pin 19 with the phase buffer input signal higher than the Low/High RPM transition frequency.

Phase Buffer Input

A tap is normally connected to one corner of the alternator's stator winding to provide an AC voltage for rotation detection. This AC signal is fed into the phase buffer input (Pin 10) through a voltage divider. If the frequency of this signal is less than the phase rotation detect frequency (36 Hz, typically), the fault lamp is lit indicating an insufficient alternator rotation and the MOSFET drive (Pin 17) output duty cycle is restricted to approximately 29% maximum. Also, if the peak voltage of the AC signal is less than the phase detect threshold, the fault lamp is lit indicating an insufficient amount of field current and again the MOSFET drive (Pin 17) output duty cycle is restricted to approximately 29% maximum.

Undervoltage, Overvoltage and Load Dump

The low pass filter output feeds an undervoltage comparator through an external voltage divider. The voltage divider can be used to adjust the undervoltage detection level. During an undervoltage condition, the fault lamp will light only if the phase buffer input signal frequency is higher than the Low/High RPM transition frequency. This is to ensure that the undervoltage condition is caused by a true fault and not just by low alternator rotation. To help maintain system voltage regulation during an undervoltage condition, the output duty cycle is automatically increased to 100%. Even though the fault lamp may be energized for an undervoltage condition, the MC33092 will continue to operate but with limited performance.

Through an internal voltage divider, the low pass filter feeds an overvoltage comparator which monitors this output for an overvoltage condition. If the overvoltage threshold is exceeded, the fault lamp is lit and the MOSFET drive (Pin 17) output duty cycle is restricted to approximately 4% maximum.

The internal voltage divider on the input to the load dump comparator has a different ratio than the divider used on the overvoltage comparator. This allows the load dump detect threshold to be higher than the overvoltage threshold even though both comparators are monitoring the same low pass filter output. If the load dump detect threshold is exceeded, the fault lamp and MOSFET drive outputs are disabled to protect the MOSFET, field winding and lamp.

MCCF33093

Product Preview

Ignition Control Flip-Chip

Designed for automotive ignition applications. The MCCF33093 provides outstanding control of the ignition coil when used with an appropriate Motorola Power Darlington Transistor. Engine control systems utilizing the MCCF33093 exhibit exceptional fuel efficiency and low exhaust emissions. The MCCF33093 requires a differential Hall Sensor input for proper operation.

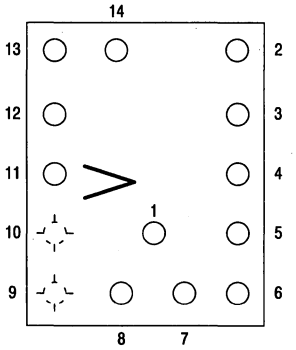
The MCCF33093 utilizes Flip-Chip Technology in which solder bumps, rather than traditional wire bonds, are created to establish mechanical and electrical contact to the chip. This process affords a unique device having improved reliability at elevated operating temperatures.

- Solder Bumped for Flip-Chip Assembly
- External Capacitors to Set Device Timing
- Overvoltage Shutdown Protection
- Auto Start-Up Capability Once Overvoltage Condition Ceases
- Allows for Push Start-Up in Automotive Applications
- Ignition Coil Current Limiting
- Ignition Coil Voltage Limiting
- Bandgap Reference for Enhanced Stability Over Temperature
- Negative Edge Filter for Hall Sensor Input Transient Protection
- Hall Sensor Inputs for RPM and Position Sensing
- $-30°C \le T_A \le +140°C$ Ambient Operating Temperature

IGNITION CONTROL FLIP-CHIP

SILICON MONOLITHIC INTEGRATED CIRCUIT

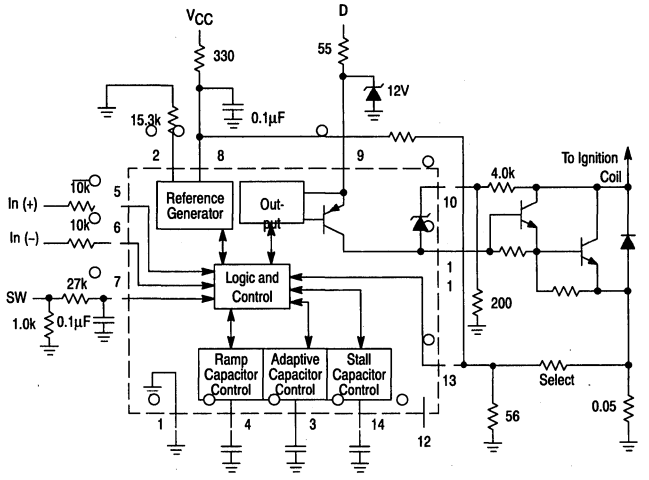
FLIP-CHIP CONFIGURATION



(Backside View)

0.116 inch x 0.091 inch
Backside orientation marking
indicated by arrow oriented as shown

Simplified Block Diagram and Application Circuit



BUMP CONNECTIONS

1. Ground
2. Master Bias
3. Adaptive Capacitor
4. Ramp Capacitor
5. Positive Hall Input
6. Negative Hall Input
7. Start
8. Supply
9. Distributor Signal
10. Coil
11. Output
12. Process Test
13. Emitter of Darlington
14. Stall Capacitor

ORDERING INFORMATION

Device	Temperature Range	Package
MCCF33093	– 30° to +140°C	Flip-Chip

10

MCCF33094

Product Preview

Ignition Control Flip-Chip

Designed for automotive ignition applications. The MCCF33094 provides outstanding control of the ignition coil when used with an appropriate Motorola Power Darlington Transistor. Engine control systems utilizing the MCCF33094 exhibit exceptional fuel efficiency and low exhaust emissions. For proper operation, the MCCF33094 requires a single Hall Sensor input signal, which is compared to an accurate internal reference.

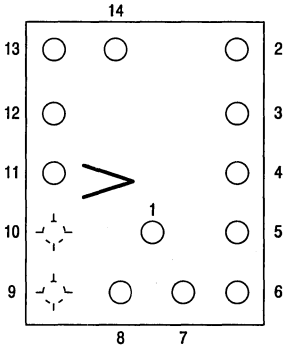
The MCCF33094 utilizes Flip-Chip Technology in which solder bumps, rather than traditional wire bonds, are created to establish mechanical and electrical contact to the chip. This process affords a unique device having improved reliability at elevated operating temperatures.

- Solder Bumped for Flip-Chip Assembly
- External Capacitors to Set Device Timing
- Overvoltage Shutdown Protection
- Auto Start-Up Capability Once Overvoltage Condition Ceases
- Allows for Push Start-Up in Automotive Applications
- Ignition Coil Current Limiting
- Ignition Coil Voltage Limiting
- Bandgap Reference for Enhanced Stability Over Temperature
- Negative Edge Filter for Hall Sensor Input Transient Protection
- Hall Sensor Inputs for RPM and Position Sensing
- $-30°C \le T_A \le +140°C$ Ambient Operating Temperature

IGNITION CONTROL FLIP-CHIP

SILICON MONOLITHIC INTEGRATED CIRCUIT

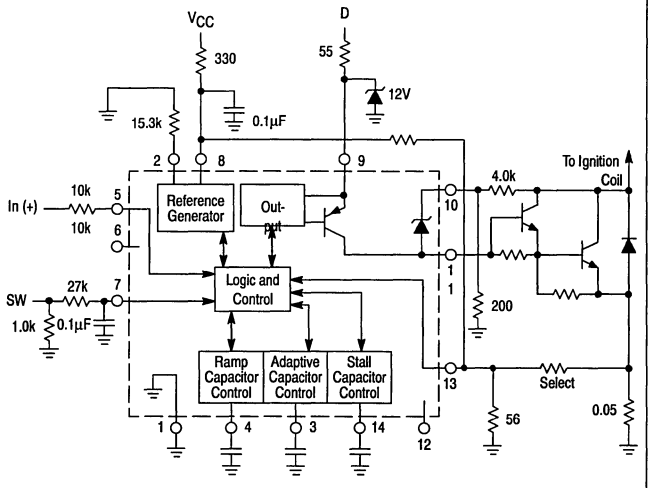
FLIP-CHIP CONFIGURATION



(Backside View)

0.116 inch x 0.091 inch
Backside orientation marking
indicated by arrow oriented as shown

Simplified Block Diagram and Application Circuit



BUMP CONNECTIONS

1. Ground
2. Master Bias
3. Adaptive Capacitor
4. Ramp Capacitor
5. Positive Hall Input
6. N.C.
7. Start
8. Supply
9. Distributor Signal
10. Coil
11. Output
12. Process Test
13. Emitter of Darlington
14. Stall Capacitor

ORDERING INFORMATION

Device	Temperature Range	Package
MCCF33094	– 30° to +140°C	Flip-Chip

10

MCCF33095

INTEGRAL ALTERNATOR REGULATOR

SILICON MONOLITHIC INTEGRATED CIRCUIT

Advance Information

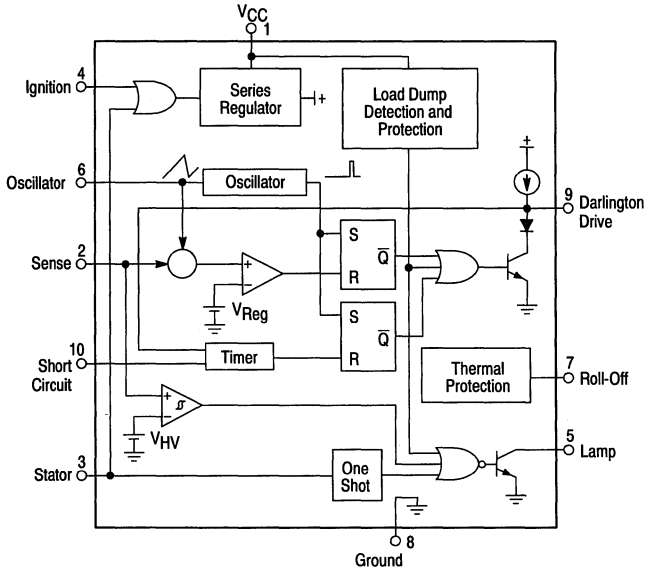
Integral Alternator Regulator

The MCCF33095 Flip-Chip is a regulator control integrated circuit designed for use with the MCCF33096 Darlington Flip-Chip in automotive alternator charging systems. Few external components are required for full system implementation when the MCCF33095 is used with the MCCF33096. This chip set combination provides control for a broad range of 12 V alternator systems when used with the appropriate Motorola Power Darlington to control the field current of the specific alternator.

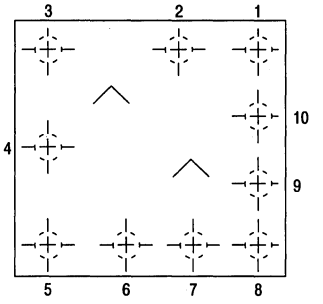
The MCCF33095 is designed to work in harsh automotive environments. Internal detection and protection features coupled with Flip-Chip Technology make the MCCF33095 able to withstand severe vibration, thermal shock, and extreme electrical variations with a high degree of reliability.

- Constant Frequency with Variable Duty Cycle Operation
- Adjusts System Charging to Compensate for Changes in Ambient Temperature
- Slew Rate Control to Reduce EMI
- Lamp Pin to Indicate Abnormal Operating Conditions
- Shorted Field Protection
- Resumes Normal Operation Once Fault Condition Ceases
- Thermal Operation from – 40° to 170°C
- Solder Bump Processed for Flip-Chip Assembly
- Minimal Space Required

Simplified Block Diagram



FLIP-CHIP CONFIGURATION



(Backside View)
Back marking is array oriented as shown

BUMP CONNECTIONS

1. V_{CC}
2. Sense
3. Stator
4. Ignition
5. Lamp
6. Oscillator
7. Roll-Off
8. Ground
9. Darlington Drive
10. Short Circuit

ORDERING INFORMATION

Device	Temperature Range	Package
MCCF33095	– 40° to +170°C	Flip-Chip

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MAXIMUM RATINGS (Note 1, 3)

Rating	Symbol	Value	Unit
Steady State V_{CC}, V_{IGN}, V_{STA}		9.0 to 24	V
V_{CC} and V_{IGN} Transient		80	V
Bump Shear Strength		8.0	Grams/Bump
Power Dissipation and Thermal Characteristics Maximum Power @ T_A = 25°C Thermal Resistance, Junction-to-Substrate	 T_{JS}	 700 29	 mW °C/W
Operating Junction Temperature	T_J	+170	°C
Ambient Temperature Range	T_A	– 40 to +170	°C

ELECTRICAL CHARACTERISTICS (Limit values are given for – 40°C ≤ T_A ≤ 150°C and typical values represent approximate mean value at T_A = 25°C. Pins 6, 7, 8, 10 = 0 V, and 12 V ≤ Pins 1, 2, 3, 4 ≤ 16 V, unless otherwise specified.)

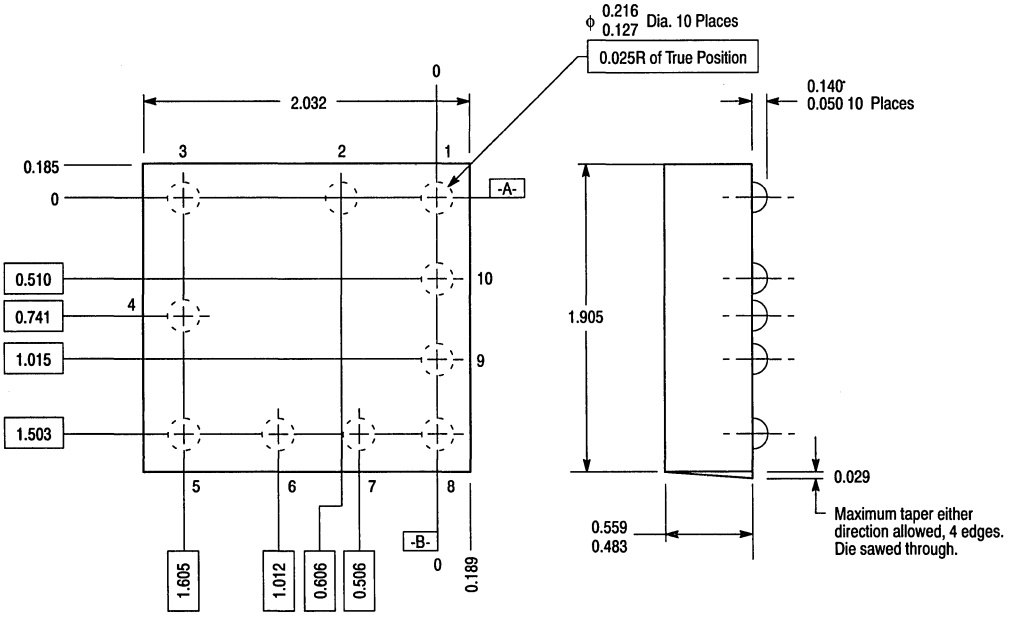
Characteristics	Symbol	Min	Typ	Max	Unit
SUPPLY (Pin 1)					
Supply Current Disabled (Pin 4 = 0.5 V, Pin 3 = 5.0 V) Enabled (Pin 1, 2 = 17 V, Pin 4 = 1.4 V)	I_{CC}	 – 50 0	 + 0.2 3.9	 + 50 25	 µA mA
Darlington Drive Overvoltage Disable Threshold (Pin 1, 4, 10 = 19 V to 29 V Ramp, Pin 3 = 10 V) Hysteresis (Pins 1, 3, 4, 10 = 29 V to 19 V Ramp)	 V_{CODD} V_{CODDH}	 19 —	 26 4.2	 28 —	V
Lamp Overvoltage Disable Threshold (Pins 1, 3, 4, 10 = 19 V to 29 V Ramp) Hysteresis	 V_{COL} V_{COLH}	 19 —	 22.3 0.3	 28 —	V
SENSE (Pin 2)					
Sense Current (Pin 6 = 2.0 V)	I_{sense}	–10	+ 0.6	+ 10	µA
Calibration Voltage (50% Duty Cycle, Note 5)	V_R	12.25	14.6	16.4	V
Lamp Comparator Detect Threshold	V_{SCD}	—	16.3	—	V
Proportional Control Range	M_V	50	187.4	350	mV
Lamp Comparator Reset Threshold	V_{HV}	15.4	15.9	16.4	V
Lamp Hysteresis	V_{hys}	20	416.6	600	mV
STATOR					
Propagation Delay Lamp-to-High (Pin 3 = 15 V to 6.0 V)	t_{STA}	 6.0	 59.4	 600	ms
Reset Threshold Voltage Lamp-to-Low (Pin 3 = 5.0 V to 11 V)	V_{IH}	 6.0	 8.8	 10	V
Input Current (Pin 2 = 18 V, Pin 6 = 2.0 V)	I_{STA}	 –10	 + 1.5	 + 10	µA
LAMP (Pin 5)					
Saturation Voltage (Pin 5 = 14 mA) (Pins 1, 2, 3, 4 = 30 V, Pin 5 = 20 mA)	V_{OLL}	 0 0	 111.8 147.4	 350 350	mV
Leakage Current (Pin 2 = 1.0 V, Pin 5 = 2.5 V)	I_{OHL}	 – 50	 + 0.8	 + 50	µA

ELECTRICAL CHARACTERISTICS (Limit values are given for – 40°C ≤ T_A ≤ 150°C and typical values represent approximate mean value at T_A = 25°C. Pins 6, 7, 8, 10 = 0 V, and 12 V ≤ Pins 1, 2, 3, 4 ≤ 16 V, unless otherwise specified.)

Characteristics	Symbol	Min	Typ	Max	Unit
DARLINGTON DRIVE (Pin 9)					
Source Current Pins 1, 2, 4 = 9.0 V, Pin 9 = V Across Power Darlington)	I_{OHDD}	5.0	7.6	20	mA
Saturation Voltage (Pin 2 = 18 V, Pin 6 = 2.0 V, Pin 9 = –100 μA)	V_{OLDD}	0	300.1	350	mV
Minimum ON Time (Pin 2 = 18 V, Note 5)	t_{DD}	200	697.8	—	μs
Frequency (Note 5)	F_{OSC}	75	174.7	325	Hz
Minimum Duty Cycle (Pin 2 = 18 V, Note 5)	DC_{DD}	—	12.2	13	%
Rise Time (10% to 90%, Note 5) Fall Time (90% to 10%, Note 5)	t_r t_f	10	21.4 23.7	50	μs
SHORT CIRCUIT					
Duty Cycle (Note 5)	DC_{SC}	0.5	1.7	5.0	%
ON Time (Note 5) (Short Circuit High, Pin 10 = 8.0 V)	PW_{SC}	50	99	660	μs

NOTES: 1. Inputs to Pin 1 applied through a 250 Ω resistor.
2. Inputs to Pin 2 applied through a 100 kΩ and 50 kΩ resistor divider to generate one-third V_{bat}.
3. Inputs to Pin 3 and Pin 4 are applied through a 20 kΩ resistor.
4. Inputs to Pin 10 applied through a 30 kΩ resistor.
5. Pin 6 connected in series with 0.022 μF capacitor to ground.

MECHANICAL DIMENSIONS



NOTE:
1. All dimensions shown indicated in millimeters.
2. ▭ Denotes basic dimension having zero tolerance and describes the theoretical exact location (true position) or contour.

Figure 1. Pins 1, 3, and 4 Field Transient Decay

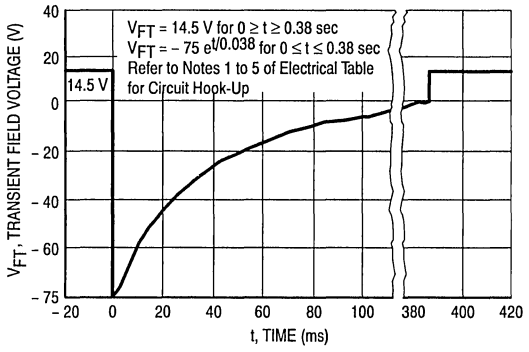


Figure 2. Pins 1 and 4 Load Dump Transient Decay

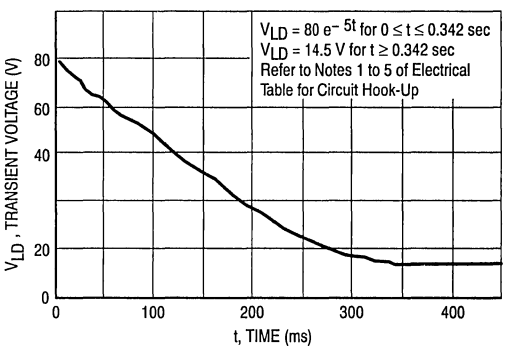


Figure 3. Temperature versus V_{bat} for 50% Duty Cycle

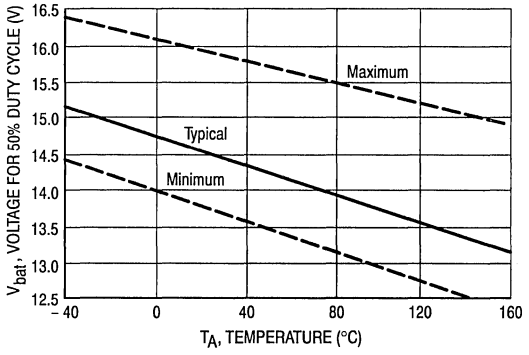


Figure 4. V_{bat} (50% Duty Cycle) versus V_{bat} (Lamp ON)

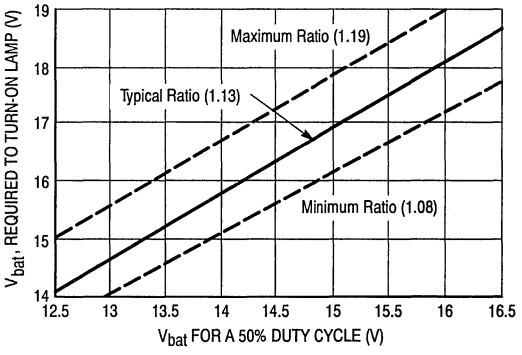


Figure 5. Field Current versus Cycle Time

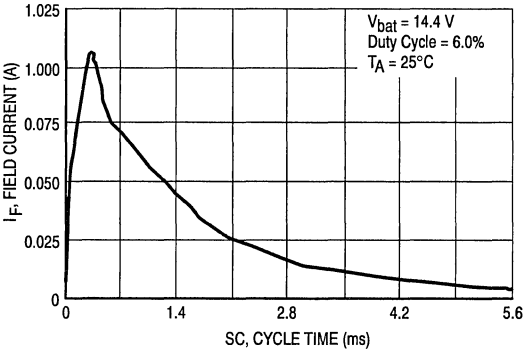


Figure 6. Field Current versus Time

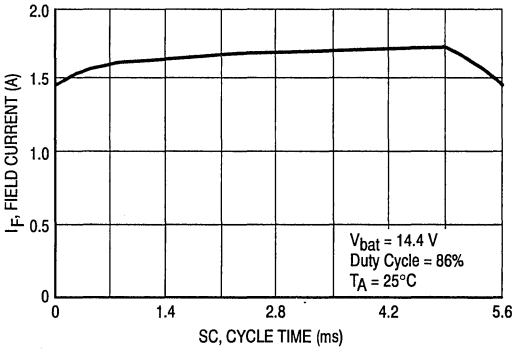


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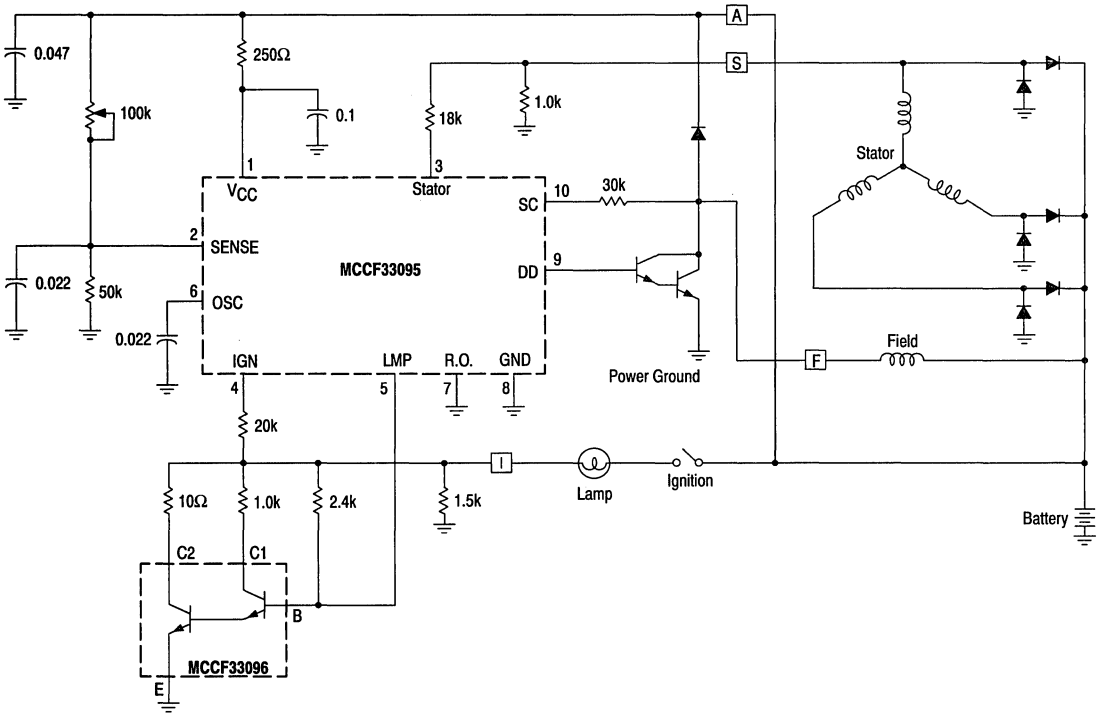
Figure 7. Integral Alternator Regulator System



FUNCTIONAL DESCRIPTION

Introduction

The MCCF33095 Flip-Chip circuit was originally designed for use in alternator charging systems. The MCCF33095 consists of many protection features which are entailed in a 10-pin flip-chip package. Device operation and application suggestions are given below.

Oscillator

The oscillator frequency is determined by the value of an external capacitor from the oscillator pin to ground (see Figure 7). The oscillator frequency in a typical application is approximately 175 Hz, but a range of 50 Hz to 500 Hz can reasonably be used. The waveform generated consists of a positive linear slope followed by relatively fast negative fall (sawtooth). The flip-flops are reset by the falling edge of the sawtooth signal as shown in the Simplified Block Diagram. The oscillator signal peaks at approximately 3.0 V and provides the timing required for the device.

Ignition

The Ignition input signal enables the device turn-on when the Pin 4 voltage is greater than 1.4 V. This signal normally originates from the ignition switch of automotive systems.

Sense

The Sense pin functions as a voltage sensor. It proportionally senses the battery voltage and determines the amount of time the Darlington transistor is high over the next cycle. A low voltage at the Sense pin will result in a long duty cycle for the Darlington and a high voltage produces a short duty cycle. Proportional control is used to determine the duty cycle time. Proportional control is defined as the difference between the alternator voltages required for 20% and 95% output duty cycles.

Lamp

The Lamp Output pin functions as a warning indicator for overvoltage and stopped engine conditions existing in the system.

Stator

The Stator pin senses the voltage from the Stator in the application circuit, and keeps the device powered up while the stator voltage is high. Furthermore, it acts as a sense for a stopped engine condition. If this condition is detected, the Stator turns ON the lamp.

Power Supply, V_{CC}

The V_{CC} pin powers the entire device and disables all outputs during any overvoltage condition.

Roll Off

The Roll Off pin provides thermal protection for the circuit. This capability exists, but has not been characterized and is not tested for at this time. Therefore, it is recommended that this pin be connected to ground.

Darlington Drive

The Darlington Drive output pin exists to turn on a power Darlington. The Sense pin voltage determines the duty cycle of the Darlington. The oscillator is set to maintain a minimum duty cycle, except during overvoltage and short circuit conditions.

Short Circuit

The Short Circuit pin monitors the field voltage. When the Darlington Drive and Short Circuit pins are simultaneously high for a duration greater than the slew rate period, a short circuit condition is noted. The detection time required prevents the device from reacting to false shorts. As a result of short circuit detection, the output is disabled. During a short circuit condition the device automatically retries with a 2% duty cycle (Darlington ON). Once the short circuit condition ceases, normal device operation resumes.

Note

A capacitor should be used in parallel with the V_{CC} pin to filter out noise transients. Likewise, a capacitor should be used in parallel with the Sense pin to create a dominant closed-loop pole. Resistors connected to inputs, as mentioned in Notes 1 through 5 of the Electrical Characteristic table, should be used.

FLIP-CHIP APPLICATION INFORMATION

Introduction

Although the packaging technology known as "flip-chip" has been available for some time, it has seen few applications outside the automotive and computer industries. Present microelectronic trends are demanding smaller chip sizes, reduced manufacturing costs, and improved reliability. Flip-chip technology satisfies all of these needs.

Conventional assembly techniques involve bonding wires to metal pads to make electrical contact to the integrated circuit. Flip-chip assembly requires further processing of the integrated circuit after final nitride deposition to establish robust solder bumps with which to make electrical contact to the circuit. A spatially identical solderable solder bump pattern, normally formed on ceramic material, serves as a substrate host for the flip-chip. The "bumped" flip-chip is aligned to, and temporally held in place through the use of soldering paste. The aligned flip-chip and substrate host are placed into an oven and the solder reflowed to establish both electrical and mechanical bonding of the flip-chip to the substrate circuit. Use of solder paste not only holds the chip in temporary placement for reflow but also enhances the reflow process to produce highly reliable bonds.

Flip-Chip Benefits

Some of the benefits of flip-chip assembly are:

1) Higher circuit density resulting in approximately one-tenth the footprint required of a conventional plastic encapsulated device.
2) Improved reliability especially in high temperature applications. This is due, in part, to the absence of wires to corrode or fatigue from extensive thermal cycling.
3) No bond wires are required that might possibly become damaged during assembly.
4) Adaptable for simultaneous assembly of multiple flip-chips, in a hybrid fashion, onto a single ceramic substrate.

The following discussion covers the flip-chip process steps performed by Motorola, and the assembly processing required by the customer, in order to attach the flip-chip onto a ceramic substrate.

MOTOROLA'S FLIP-CHIP PROCESS

Overview

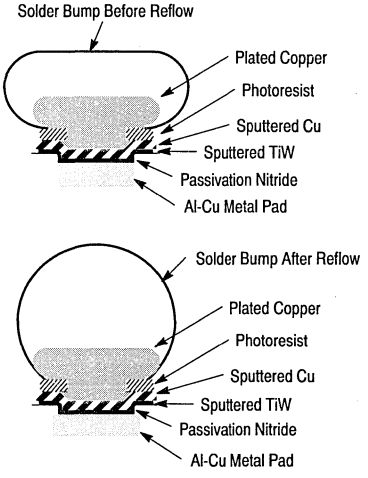
The process steps to develop an integrated circuit flip-chip are identical to that of conventional integrated circuits up to and including the deposition of the final nitride passivation layer on the front surface (circuit side). At this stage all device metal interconnects are present.

The process sequence is as follows:

1) Passivation-nitride photo resist and etch
2) Bimetal sputter (titanium (Ti) and tungsten (W) followed by copper (Cu))
3) Photo mask to define the bump area
4) Copper plate
5) Lead plate
6) Tin plate
7) Photoresist clean to remove all photo resist material
8) Bimetal etchback
9) Reflow for bump formation
10) Final inspection

The diagram below depicts the various layers involved in the bump process.

Figure 8. Plated Bump Structure and Process Flow



Initially, photoresist techniques are used to create openings in the nitride passivation layer exposing the metal pad vias. Ti/W, followed by Cu, are sputtered across the entire wafer surface. The surface is then photo patterned to define the bump areas. The sputtered metals together constitute a base metal for the next two metal depositions.

10

The Ti/W layer provides excellent intermetallic adhesion between the metal pads and the sputtered copper. In addition, the Ti/W provides a highly reliable interface to absorb mechanical shock and vibrations frequently encountered in automotive applications. The sputtered copper layer creates a platform onto which an electroplated copper layer can be built-up. Layers of Cu, Pb, and Sn are applied by plating onto the void areas of the photo resist material. The photo resist is then removed and the earlier sputtered materials are etched away. The flip-chip wafer is then put into an oven exposing it to a specific ambient temperature which causes the lead and tin to ball-up and form a solder alloy.

IC Solder Bumps

The solder consists of approximately 93% lead and 7% tin. The alloying of lead with tin provides a bump with good ductility and joint adhesion properties. Precise amounts of tin are used in conjunction with lead. Too much tin in relation to lead can cause the solder joints to become brittle and subject to fatigue failure. Motorola has established what it believes to be the optimum material composition necessary in order to achieve high bump reliability.

In the make-up of the flip-chip design, bumps are ideally spaced evenly and symmetrically along each edge of the chip allowing for stress experienced during thermal expansion and vibration to be distributed evenly from bump to bump. The bump dimensions and center-to-center spacing (pitch) are specified by the chip layout and the specific application. The nominal diameter of the bumps is 6.5 mils and the minimum center-to-center pitch is roughly 8.0 mils.

Reflow

The reflow process creates a thermally induced amalgam of the lead and tin. In the melting process the surface tension is equalized causing the melted solder to uniformly ball up as mentioned earlier.

The ideal reflow oven profile gradually ramps up in temperature to an initial plateau. The purpose of the plateau is to establish a near equilibrium temperature just below that of the solder's melting temperature. Following the preheat, a short time and higher temperature excursion is necessary. This is to ensure adequate melting of the solder materials. The temperature is then ramped down to room temperature.

An atmosphere of hydrogen is used during the reflow heat cycle. The hydrogen provides a reducing atmosphere for the removal of any surface oxides present. The formation or presence of oxides can cause degradation in the bond reliability of the product.

During the flip-chip attachment reflow onto the ceramic substrate host, the created surface tension of the molten solder aids in the alignment of the chip onto the ceramic substrate.

Reliability

Motorola is determined to bring high quality and reliable products to its customers. This is being brought about by increased automation, in-line Statistical Process Control (SPC), bump shear strength testing, thermocycling from – 40° to +140°C, process improvements such as backside laser marking of the silicon chip, and improved copper plating techniques.

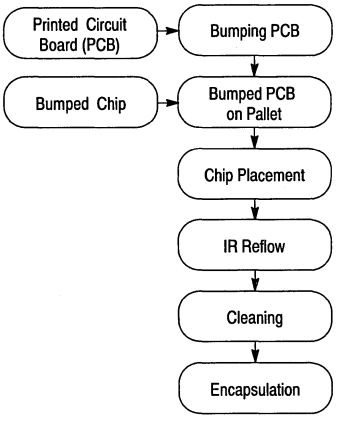
ATTACHING FLIP-CHIPS ONTO CERAMIC SUBSTRATES

Overview

The assembly or process of attaching the flip-chip onto a ceramic substrate is performed by the module fabricator. Prior to actual assembly the ceramic substrate should undergo several process steps. Care should be exercised to properly orient the flip-chip onto the substrate host in order to accommodate the appropriate solder bumps. Ideally, the flip-chip should be removed from the waffle pack with a pick and place machine utilizing a vacuum pick-up to move the die onto the ceramic substrate. Any other components to be reflow soldered onto the substrate can be placed onto the substrate in a similar manner. Flip-chip assembly onto a ceramic substrate allows for some passive components such as resistors to be formed directly into the ceramic substrate circuit pattern itself. With all surface components to be mounted in place on the ceramic substrate, the assembly is moved into the furnace where it undergoes a specified temperature variation to solder all the components onto the ceramic substrate. This is accomplished by melting (reflowing) the substrate solder bumps. The resulting assembly should, after being cooled, be cleaned to remove any flux residues. If the substrate assembly is to be mounted into a module, it is recommended the cavity of the module be filled with an appropriate silicone gel. The use of a gel coating helps to seal the individual components on the substrate from external moisture. A commonly used gel for this purpose is Dow Corning 562. As a final module assembly step, a cover is recommended to be placed over the ceramic assembly for further protection of the circuit.

It should be pointed out that the commonly used ceramic substrate material, though more expensive than other substrate materials, offers significantly superior thermal properties. By comparison, the use of ceramic material offers 33 times the thermal advantage of the second best material, Ceracom. The common FR-4 epoxy material is 100 times less thermally conductive than ceramic. For applications where dielectric constants are important and/or heat dissipation is not of real importance, other less costly materials can be used. The basic concept of the process is identical for all flip-chip substrates used.

Figure 9. Process Flow Diagram



Ceramic Substrate Preparation

The recommended ceramic substrate is aluminum oxide. These substrates come connected in what is referred to as a card. This is identical to the concept of die or chips on a wafer. Each card usually contains 8 to 16 substrates.

Initially the ceramic should be precleaned with isopropyl alcohol, followed by freon. The bump pattern is then transferred onto the substrate using a metal stencil technique using a palladium silver conducting paste, such as DuPont 9476, through a #325 mesh. Once the pattern is applied, the substrate is dried for ten minutes at 150°C and then fired for 60 minutes at a temperature increasing to a peak of 850°C for ten additional minutes. Solder paste is then stenciled onto the pads.

A metal etched stencil defining the contact areas is recommended. The use of an etched stencil affords better solder paste control than does a silk screen. The metal stencil affords a deposition of a known amount of solder paste, thereby preventing bridging caused by excess solder usage.

Solder Paste Content

It is recommended that the solder paste consist of 10% tin, 88% lead, and 2% silver alloy. However, 95/3/2 compositions have had successful results.

A rosin based flux, such as RMA (Rosin Mildly Activated) manufactured by Dupont and having spherical particles of 45 to 75 microns, should be used. The tackiness of the solder paste at room temperature helps to hold the flip-chip in place during the pick and place operation. The use of flux:

1) Prevents excess oxidation during reflow,
2) Optimizes the flow of liquid solder through the stencil,
3) Smooths the surface by reducing surface tension, and
4) Enhances the normalization of surface tension upon reflow causing the flip-chip bumps to effectively auto-align themselves to substrate bump pads.

A solder mask can be used for applications requiring high precision and is shown in Figure 10.

Figure 10a. Before Reflow

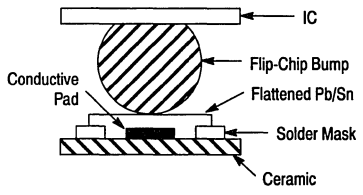
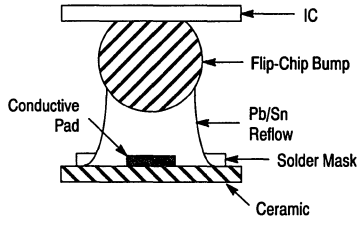


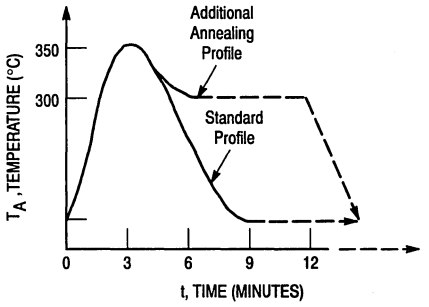
Figure 10b. After Reflow



Oven Profile

After the flip-chip is placed onto the bumped substrate, the substrate and flip-chip are ready for reflow. Initially, the flip-chip is heated to a peak temperature of around 300° to 350°C for five minutes. It is to be noted that the flip-chip bumps have a higher melting temperature than the bumps on the substrate. During assembly reflow the substrate bumps melt and create a substrate to flip-chip bump bond. After reflow the assembled part is cooled to room temperature or to some intermediate temperature point for annealing purposes.

Figure 11. Reflow Oven Profile



The oven temperature profile is established primarily to melt the solder while minimizing the alloying of the materials and keeping the flux from boiling away. It should be noted that when the flip-chip is placed onto the substrate, the material is stressed in one direction or another. The use of flux helps to reduce any surface stresses present. A reduction in the surface stress enhances solder wetting which in turn aids in the alignment of the flip-chip to the substrate. Poor solder wetting will produce misalignment as well as inferior bond strengths and reliability.

It is recommended that an inert atmosphere such as nitrogen be used during the reflow process to prevent oxidation.

Final Cleaning

The final cleaning involves removing the remaining flux from the flip-chip assembly. Three possible methods of removing flux are: ultrasonic cleaner, Terpene solvent and DI water, or vapor degreaser. The flux manufacturer should be able to recommend the proper type of vapor degreaser to be used.

Test and Reliability

Both visual inspection and shear strength testing should be performed on packaged flip-chip assemblies.

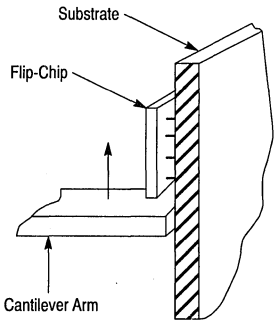
Solder reflow results which exhibit a grainy and dull appearance produce inferior bond shear strengths. Inferior bond shear strengths are visually recognizable by:

1) The presence of old or badly oxidized solder paste,
2) Insufficient amount of solderable material,
3) The contamination of bond pads with grease, oil, etc.

It should be mentioned that many contaminants are transparent and not easily detectable by visual means.

Shear strength testing should meet a 0.8 Newtons/Bump criteria. Shear strength testing should follow thermocycling of the chip from – 40° to +140°C to insure the stability of shear strength over temperature. Figure 12 depicts a test set-up which might possibly be used.

Figure 12. Shear Test Fixture



Aside from physical contamination, flip-chips, like any other chips, should not be handled directly due to the fact that electrostatic discharges can cause permanent damage to the electronic circuit. Flip-chips which do survive an electrostatic discharge can be left in a weakened condition resulting in reduced reliability of the end product. To avoid electrostatic damage of the circuit, assembly personnel should make use of a wrist strap or some other device to provide electrostatic grounding of their body. For the same reason, machinery used to assemble semiconductor circuits should be electrostaticly grounded.

Flip-chips rely primarily on the thermal path established by the bumps to remove heat from the chip as a result of internal circuit operation. Standard Motorola flip-chips have a thermal resistance of approximately 290°C/W/Bump. This figure can be used to estimate the allowed maximum power dissipation of the chip.

Cost and Equipment Manufacturers

The cost of implementing a flip-chip assembly process depends on the specific production requirements and as a result will vary over a broad range. It is possible to implement a small volume laboratory set-up for a few hundred dollars using manual operations. At the other end of the scale one could spend millions setting up a fully automated line incorporating pattern recognization, chip and substrate orientation, reflow, cleaning, and test. The module fabricator will have to make this assessment.

An assembly operator can manually accomplish the pick and place operation using a vacuum probe to pick-up and orient the flip-chip onto the substrate. Furthermore, it is possible to perform the reflow assembly operation using a simple batch process oven fabricated from a laboratory hot plate. However, the use of such process techniques will have questionable impact on the final product's reliability and quality. For this reason, it is highly recommended the module fabricator seriously consider two major pieces of equipment; a pick and place machine and an infrared solder reflow oven. Both pieces of equipment can vary over a wide cost range depending on the production requirements. A partial list of manufacturers for this equipment is given below.

Pick and Place Machine:

Universal Instruments Corp
Dover Technologies, Inc.
Binghamton, NY 13902
(607) 772-7522

Seiko
Torrance, CA 90505
(310) 517-7850

Laurier Inc.
Hudson, NH 03051
(603) 889-8800

Infrared Reflow Oven:

BTU
Bellerica, MA 01862
(508) 667-4111

Vitronics
Newmarket, NH 03857
(603) 659-6550

Additional Applications

Completed ceramic flip-chip sub-assemblies can be stacked one on top of another to produce an overall assembly by making contact connections through bumps. This technology is beginning to emerge in the computer industry where physical module size is of significant importance. Furthermore, this assembly technology, though more complex, is undergoing serious consideration within the automotive industry as well.

Applications requiring small size and high reliability at high ambient temperatures can benefit considerably through the implementation of flip-chip assembly techniques.

MCCF33096

Advance Information

Darlington Drive Flip-Chip

DARLINGTON DRIVE FLIP-CHIP

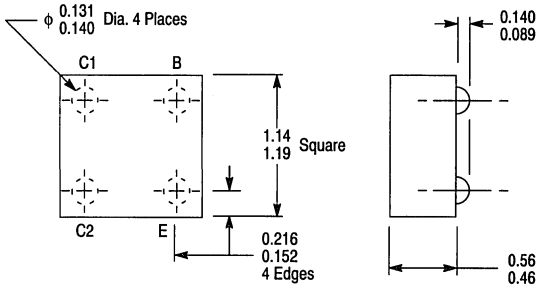
SILICON MONOLITHIC INTEGRATED CIRCUIT

The MCCF33096 is a Darlington Flip-Chip designed for use with the MCCF33095 Flip-Chip as a lamp driver in automotive charging systems. The MCCF33095 and MCCF33096, when used with an appropriate Motorola Power Darlington Transistor, provide the necessary control for automotive alternator regulator systems. The MCCF33096 is controlled by the Lamp pin output of the MCCF33095 Flip-Chip for this application.

The MCCF33096 is made using Flip-Chip Technology and has solder bumps attached. Flip-Chip Technology affords higher operating temperatures with improved reliability. The Darlington Flip-Chip can be soldered directly to an appropriate ceramic circuit board with substantial savings in space.

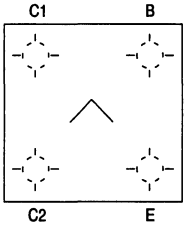
- High Reliability at Elevated Temperatures
- Thermal Operation from –40° to +170°C
- Solder Bumped for Flip-Chip Assembly
- Minimal Space Required

Mechanical Dimensions



NOTE: All dimensions shown indicated in millimeters.

FLIP-CHIP CONFIGURATION



(Backside View)
Back marking is array with arrow pointing to side with B and C1 bumps

BUMP CONNECTIONS

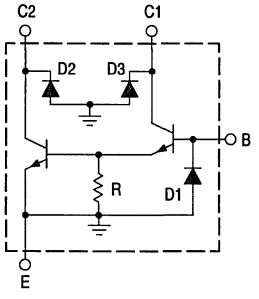
C1 = Q1 Collector

C2 = Q2 Collector

E = Emitter

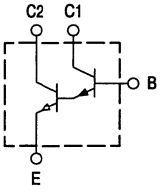
B = Base

Block Diagram



R = 200 Ω ±20%
NOTE: The emitter is connected to the substrate.

Simplified Block Diagram



ORDERING INFORMATION

Device	Temperature Range	Package
MCCF33096	–40° to +170°C	Flip-Chip

10

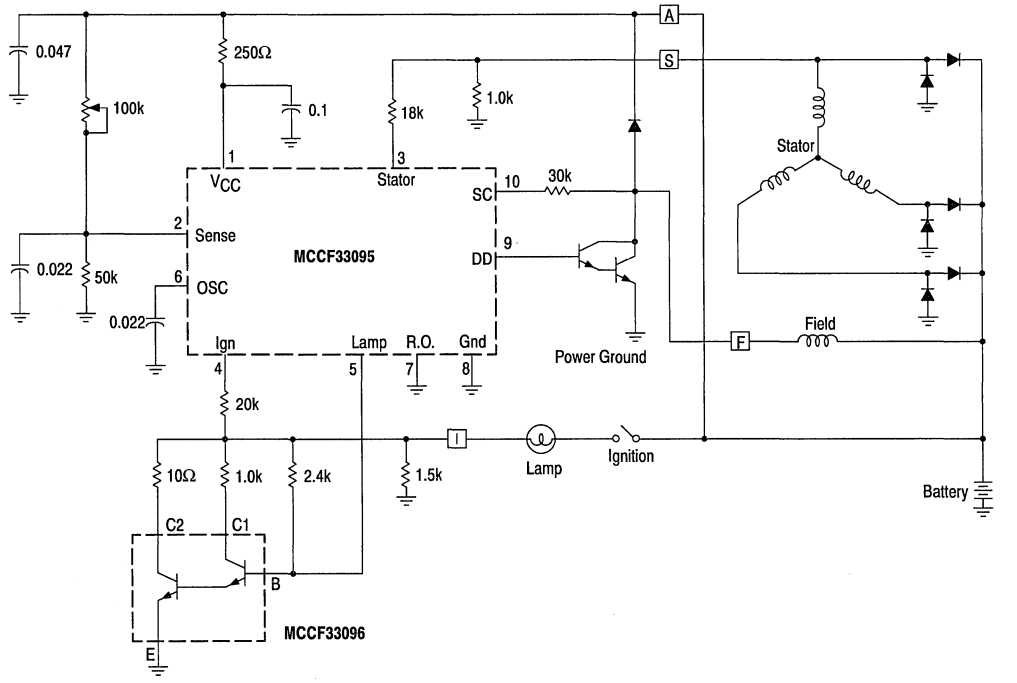
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Bump Shear Strength		8.0	Grams/Bump
Power Dissipation and Thermal Characteristics Maximum Power @ T_A = 25°C Thermal Resistance, Junction-to-Substrate	 T_{JS}	 6.0 73	 W °C/W
Operating Junction Temperature	T_J	+170	°C
Ambient Temperature Range	T_A	– 40 to +170	°C

ELECTRICAL CHARACTERISTICS (Limit values apply over – 40°C ≤ T_A ≤ +150°C and typical values at T_A = 25°C.)

Characteristics	Symbol	Min	Typ	Max	Unit
Saturation Voltage (I_{C2} = 350 mA, I_{B1} = 0.6 mA)	$VC_{E2(sat)}$	0	0.42	0.65	V
Breakdown Voltage (I_{C1} = 1.0 mA, V_{C1} = V_{C2})	$BV_{CER(sus)}$	80	—	—	V
Collector Cutoff Current (VC_{E1} = 60 V = VC_{E2})	I_{CER}	– 10	0.04	10	μA
DC Current Gain (VC_{E1} = VC_{E2} = 1.0 V, I_{B1} = 100 μA) (I_{B1} = 1.0 μA, VC_{E2} = 0 V, VC_{E1} = 1.5 V)	 H_{FE1} H_{FE2}	 1000 50	 2100 61.3	 3500 100	 — —
Turn ON Time	t_{on}	—	—	20	μs
Turn OFF Time	t_{off}	—	—	20	μs
Diode Forward Voltage I_{D1} = 25 mA I_{D2} = 250 mA I_{D3} = 25 mA	 VF_{D1} VF_{D2} VF_{D3}	 – 1.5 – 1.5 – 1.5	 — – 1.33 – 1.33	 – 0.5 – 0.5 – 0.5	V
Emitter-Base ON Voltage (I_{C2} = 350 mA, I_{B1} = 0.6 mA)	$V_{BE(on)}$	1.0	1.82	2.0	V

Figure 1. Application Circuit (Integral Alternator Regulator System)



10

MC33192

Product Preview

MI-Bus Interface Stepper Motor Controller

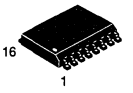
MI-BUS INTERFACE STEPPER MOTOR CONTROLLER

SILICON MONOLITHIC INTEGRATED CIRCUIT

The MC33192 Stepper Motor Controller is intended to control loads in harsh automotive environments using a serial communication bus. The MI-Bus can provide satisfactory real time control of up to eight stepper motors. MI-Bus technology offers a noise immune system solution for difficult applications involving relay drivers, motor controllers, etc.

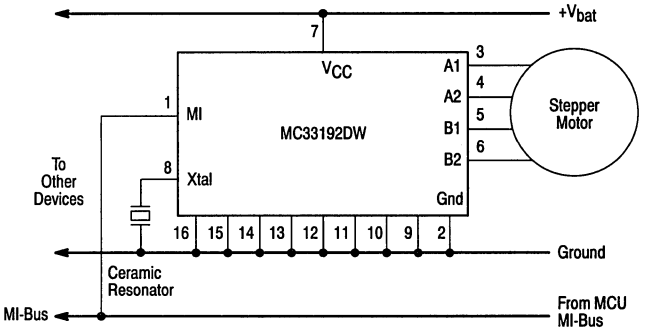
The MC33192 stepper motor controller provides four phase signals to drive two phase motors in either half or full step modes. When used with an appropriate Motorola HCMOS microprocessor it offers an economical solution for applications requiring a minimum amount of wiring while allowing a versatile system. The MC33192 is packaged in an economical 16 pin SOIC and specified at an operating voltage of 12 V for $-40°C \le T_A \le 100°C$.

- Single Wire Open Bus Capability Up to 10 Meters in Length
- Programmable Address Bus System
- Fault Detection of Half-Bridge Drivers and Motor Windings
- Ceramic Resonator for Accurate and Reliable Transmission of Data
- Sub-Multiple of Oscillator End-of-Frame Signal
- MI-Bus Signal Slew Rate Limited to 1.0 V/µs for Minimum RFI
- MI-Bus Error Diagnostics
- Non-Functioning Device Diagnostics
- Over Temperature Detection
- Address Programming Sequence Status
- Load and Double Battery (Jump Start) Protection

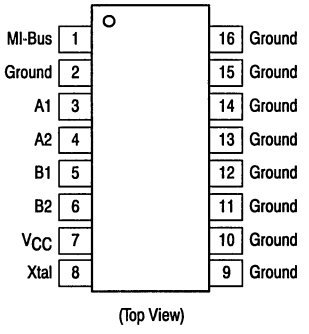


DW SUFFIX
PLASTIC PACKAGE
CASE 751G
(SO-16L)

MI-Bus Stepper Motor Controller Application



PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Temperature Range	Package
MC33192DW	– 40° to +100°C	SO-16L

10

MC33293

Product Preview

Quad Low Side Driver

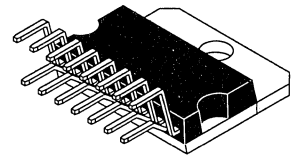
QUAD LOW SIDE DRIVER

($r_{DS(on)}$ = 0.25 Ω per Output)

SILICON MONOLITHIC INTEGRATED CIRCUIT

The MC33293 is a single monolithic integrated circuit specifically designed for quad low side switching applications. This device was initially conceived as a quad injector driver to operate in harsh automotive environments but is well suited for many other applications. The MC33293 incorporates *SMARTMOS*™ technology having CMOS logic, Bipolar/CMOS analog circuitry, and DMOS power FETs. All of the device inputs are CMOS compatible. A $\overline{\text{Fault}}$ output is provided to "flag" the existence of open loads (outputs ON or OFF), shorted loads, and over temperature condition of any output. A shorted load fault condition will shut off only the specific output involved while allowing the other outputs to operate normally. An overvoltage (V_{PWR}) condition will shut off all outputs for the overvoltage duration. All outputs are independent in operation and have internal clamp diode protection for switching inductive loads. A $\overline{\text{Single}}$/Dual Select pin is incorporated to allow either independent input/output operation or output pair operation. The MC33293 is parametrically specified over – 40°C ≤ T_A ≤ +125°C ambient temperature and 9.0 V ≥ V_{PWR} ≤ 16 V supply.

- Designed to Operate with Supply Voltages of 5.5 V to 26.5 V
- CMOS Compatible Inputs with Active Internal Pull-Downs
- Maximum 7.0 mA Quiescent Current
- Output $r_{DS(on)}$ of 0.25 Ω Maximum with V_{PWR} ≤ 9.0 V
- Outputs Internally Clamped to 65 V for Driving Inductive Loads
- Output Current Limiting of 3.0 A to Accommodate Incandescent Lamp Loads
- Output $\overline{\text{Fault}}$ Status with Interrogation Capability
- Open Load Detection (Output ON or OFF)
- Short Circuit Detection/Shutdown and Overvoltage Detection/Shutdown
- Short $\overline{\text{Fault}}$ Shutdown and Automatic Retry
- Reverse Battery Protection
- 2000 V Minimum ESD Protection (Human Body Model)

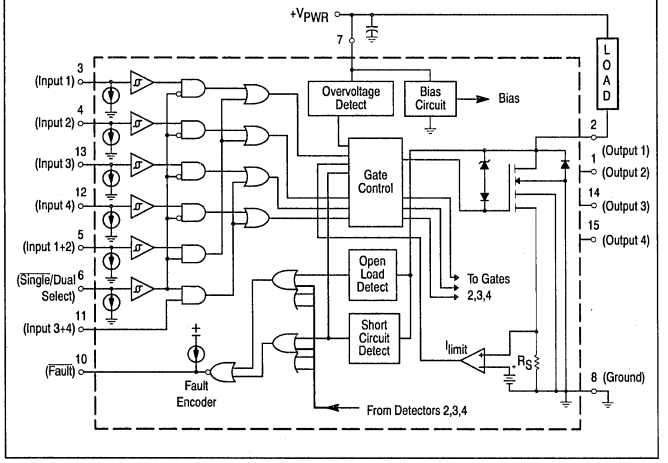


T SUFFIX
PLASTIC PACKAGE
CASE 821C
(15 Pin SIP)

PIN CONNECTIONS

PIN
1. Output 2
2. Output 1
3. Input 1
4. Input 2
5. Input 1 + 2
6. $\overline{\text{Single}}$/Dual Select
7. V_{PWR}
8. Ground
9. N.C.
10. $\overline{\text{Fault}}$
11. Input 3 + 4
12. Input 4
13. Input 3
14. Output 3
15. Output 4

Simplified Block Diagram



ORDERING INFORMATION

Device	Temperature Range	Package
MC33293T	– 40° to + 125°C	15 Pin SIP

10

MC33295

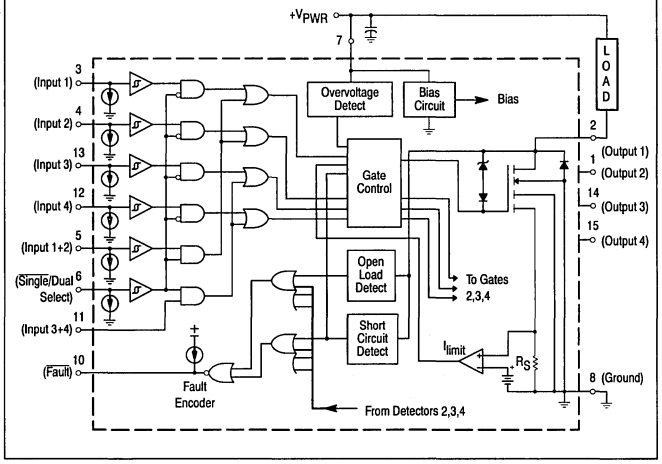
Product Preview

Quad Low Side Driver

The MC33295 is a single monolithic integrated circuit specifically designed for quad low side switching applications. This device was initially conceived as a quad injector driver to operate in harsh automotive environments but is well suited for many other applications. The MC33295 incorporates *SMARTMOS*™ technology having CMOS logic, Bipolar/CMOS analog circuitry, and DMOS power FETs. All of the device inputs are CMOS compatible. A $\overline{\text{Fault}}$ output is provided to "flag" the existence of open loads (outputs ON or OFF), shorted loads, over temperature condition of any output, and overvoltage condition. Shorted load or over temperature fault conditions will shut off only the specific outputs involved while allowing the other outputs to operate normally. An overvoltage (V_{PWR}) fault condition will shut off all outputs for the overvoltage duration. All outputs are independent in operation and have internal clamp diode protection for switching inductive loads. A $\overline{\text{Single}}$/Dual Select pin is incorporated to allow either independent input/output operation or output pair operation. The MC33295 is parametrically specified over $-40°C \le T_A \le +125°C$ ambient temperature and $5.5\ V \le V_{PWR} \le 14.5\ V$ supply.

- Designed to Operate with Supply Voltage of 5.5 V to 26.5 V
- CMOS Compatible Inputs with Active Internal Pull-Downs
- Maximum 5.0 mA Quiescent Current
- Output $r_{DS(on)}$ of 0.7 Ω Maximum with $V_{PWR} \le 9.0\ V$
- Outputs Internally Clamped to 65 V for Driving Inductive Loads
- Output Current Limiting of 3.0 A to Accommodate Incandescent Lamp Loads
- Output $\overline{\text{Fault}}$ Status with Interrogation Capability
- Open Load Detection (Output ON or OFF)
- Over Temperature Detection and Shutdown
- Short Circuit Detection/Shutdown and Overvoltage Detection/Shutdown
- Short $\overline{\text{Fault}}$ Shutdown and Automatic Retry
- Reverse Battery Protection
- 2000 V Minimum ESD Protection (Human Body Model)

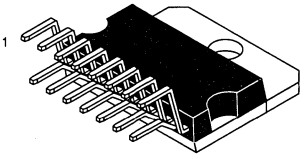
Simplified Block Diagram



QUAD LOW SIDE DRIVER

($r_{DS(on)}$ = 0.7 Ω per Output)

SILICON MONOLITHIC INTEGRATED CIRCUIT



T SUFFIX
PLASTIC PACKAGE
CASE 821C
(15 Pin SIP)

PIN CONNECTIONS

PIN 1. Output 2
2. Output 1
3. Input 1
4. Input 2
5. Input 1 + 2
6. $\overline{\text{Single}}$/Dual Select
7. V_{PWR}
8. Ground
9. N.C.
10. $\overline{\text{Fault}}$
11. Input 3 + 4
12. Input 4
13. Input 3
14. Output 3
15. Output 4

ORDERING INFORMATION

Device	Temperature Range	Package
MC33295T	– 40° to +125°C	15 Pin SIP

10

MC33298

OCTAL SERIAL SWITCH
(SPI INPUT/OUTPUT)

Advance Information

Octal Serial Switch with SPI Input/Output

The MC33298 is an eight output low side power switch with 8 bit serial input control. The MC33298 is a versatile circuit designed for automotive applications, but is well suited for other environments. The MC33298 incorporates SMARTMOS™ technology, with CMOS logic, bipolar/MOS analog circuitry, and DMOS power MOSFETs. The MC33298 interfaces directly with a microcontroller to control various inductive or incandescent loads. The circuit's innovative monitoring and protection features are: very low standby current, cascadable fault reporting, internal 65 V clamp on each output, output specific diagnostics, and independent shutdown of outputs. The MC33298 is parametrically specified over a temperature range of $-40°C \le T_A \le +125°C$ ambient temperature and $9.0\ V \le V_{PWR} \le 16\ V$ supply. The economical 20 pin DIP and SO-24 wide body surface mount plastic packages make the MC33298 very cost effective.

- Designed to Operate Over Wide Supply Voltages of 5.5 V to 26.5 V
- Interfaces Directly to Microprocessor Using SPI Protocol
- SPI Communication for Control and Fault Reporting
- 8-Bit Serial I/O is CMOS Compatible
- 3.0 A Peak Current Outputs with Maximum $r_{DS(ON)}$ of 0.45 Ω at 25°C
- Outputs are Current Limited to 3.0 A to 6.0 A for Driving Incandescent Lamp Loads
- Output Voltages Clamped to 65 V During Inductive Switching
- Maximum Sleep Current (I_{PWR}) of 50 μA with $V_{DD} \le 2.0$ V
- Maximum of 4.0 mA I_{DD} During Operation
- Maximum of 2.0 mA I_{PWR} During Operation with All Outputs ON
- Open Load Detection (Outputs OFF)
- Overvoltage Detection and Shutdown
- Each Output has Independent Over Temperature Detection and Shutdown
- Output Mode Programmable for Sustained Current Limit or Shutdown
- Short Circuit Detect and Shutdown with Automatic Retry for Every Write Cycle
- Serial Operation Guaranteed to 2.0 MHz

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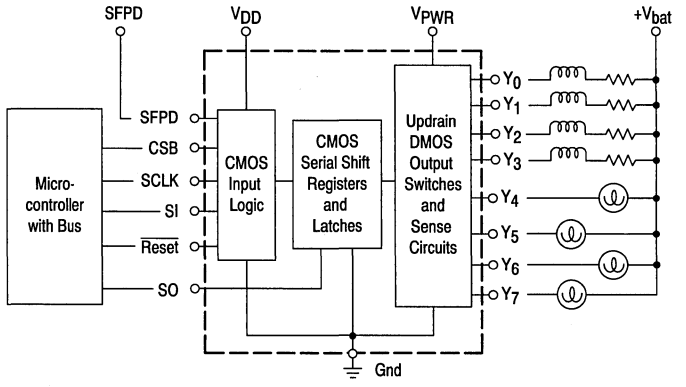
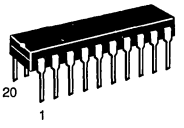
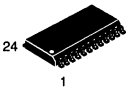
Simplified Application Schematic





P SUFFIX
PLASTIC PACKAGE
CASE 738
DIP (16+2+2)



DW SUFFIX
PLASTIC PACKAGE
CASE 751E
SOP (16+4+4)L

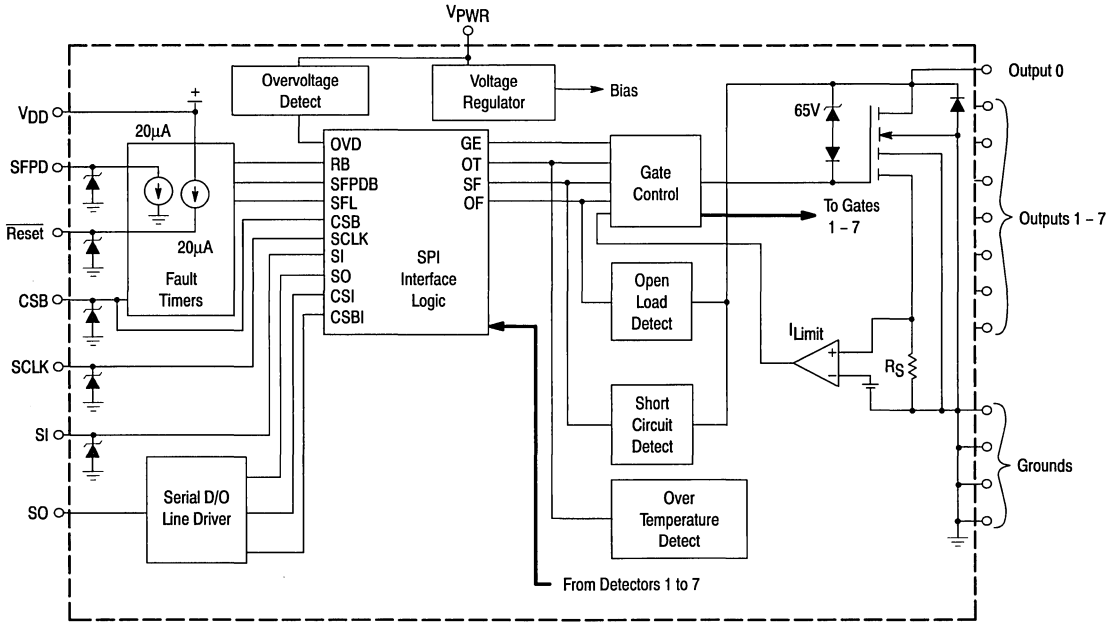
PIN CONNECTIONS

DIP	Function	SOP-24L
1	Output 7	1
2	Output 6	2
3	SCLK	3
4	SI	4
5	Ground	5
6	Ground	6
–	Ground	7
–	Ground	8
7	SO	9
8	CSB	10
9	Output 5	11
10	Output 4	12
11	Output 3	13
12	Output 2	14
13	SFPD	15
14	V_{DD}	16
15	Ground	17
16	Ground	18
–	Ground	19
–	Ground	20
17	V_{PWR}	21
18	$\overline{\text{Reset}}$	22
19	Output 1	23
20	Output 0	24

ORDERING INFORMATION

Device	Temperature Range	Package
MC33298P	– 40° to +125°C	DIP
MC33298DW		SOP-24L

Figure 1. Simplified Block Diagram



FAULT OPERATION

SERIAL OUTPUT (SO) PIN REPORTS

Overvoltage	Overvoltage condition reported
Over Temperature	Fault reported by Serial Output (SO) pin
Over Current	SO pin reports short to battery/supply or over current condition
Output ON, Open Load Fault	Not reported
Output OFF, Open Load Fault	SO pin reports output OFF open load condition

DEVICE SHUTDOWNS

Overvoltage	Total device shutdown at V_{PWR} = 28 V to 34 V. Re-operates when overvoltage is removed with all outputs assuming an off state upon recovery from overvoltage. All device registers are automatically reset (cleared) during shutdown.
Over Temperature	Only the output experiencing an over temperature shuts down.
Over Current	Only the output experiencing an over current condition shuts down at 3.0 A to 6.0 A after a 25 µs to 100 µs delay, with SFPD pin grounded. All outputs will continue to operate in a current limit mode, with no shutdown, if the SPFD pin is at 5.0 V.

MAXIMUM RATINGS (All voltages are with respect to ground, unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage			
Steady-State	$V_{PWR(sus)}$	−1.5 to 26.5	V
Transient Conditions (Note1)	$V_{PWR(pk)}$	−13 to 60	V
Logic Supply Voltage (Note 2)	V_{DD}	− 0.3 to 7.0	V
Input Pin Voltage (Note 3)	V_{in}	− 0.3 to 7.0	V
Output Clamp Voltage (Note 4)	$V_{out(off)}$		V
(I_{out} = 2.0 mA)		50 to 75	
(I_{out} = 0.5 A)		55 to 75	
Output Self-Limit Current	$I_{out(LIM)}$	3.0 to 6.0	A
Continuous Per Output Current (Note 5)	$I_{out(cont)}$	0.5	A
ESD Voltage			
Human Body Model (Note 6)	V_{ESD1}	2000	V
Machine Model (Note 7)	V_{ESD2}	200	V
Output Clamp Energy (Note 8)	E_{clamp}		
Repetitive:			
T_J = 25°C		100	mJ
T_J = 125°C		30	mJ
Non-Repetitive:			
T_J = 25°C		2.0	J
T_J = 125°C		0.5	J
Recommended Frequency of SPI Operation (Note 9)	f_{SPI}	2.0	MHz
Storage Temperature	T_{stg}	− 55 to +150	°C
Operating Case Temperature	T_C	− 40 to +105	°C
Operating Junction Temperature	T_J	− 40 to +150	°C
Power Dissipation (T_A = 25°C) (Note 10)	P_D	3.0	W
Soldering Temperature (for 10 seconds)	T_{solder}	260	°C
Thermal Resistance (Junction-to-Ambient) (Note 11)	$\varnothing_{J-A}$		°C/W
Plastic Package, Case 738:			
All Outputs ON (Note 12)		31	
Single Output ON (Note 13)		37	
SOP-24 Package, Case 751E:			
All Outputs ON (Note 12)		34	
Single Output (Note 3)		40	

NOTES: 1. Transient capability with external 100 Ω resistor connected in series with V_{PWR} pin and supply.
2. Exceeding these limits may cause a malfunction or permanent damage to the device.
3. Exceeding voltage limits on SCLK, SI, CSB, SFPD, or Reset pins may cause permanent damage to the device.
4. With output OFF.
5. Per output continuous rating with all outputs ON and equally conducting current (See Figure 21 and 22 for more details).
6. ESD1 testing is performed in accordance with the Human Body Model (C_{Zap} = 100 pF, R_{Zap} = 1500 Ω). ESD1 voltage capability of V_{PWR} pin is > 1000 V; All other device pins are as indicated.
7. ESD2 testing is performed in accordance with the Machine Model (C_{Zap} = 100 pF, R_{Zap} = 0 Ω).
8. Maximum output clamp energy capability at indicated Junction Temperature using single pulse method. See Figure 19 for more details.
9. Guaranteed and production tested for 2.0 MHz SPI operation but has been demonstrated to operate to 8.5 MHz @ 25°C.
10. Maximum power dissipation at indicated junction temperature with no heat sink used. See Figures 20, 21, and 22 for more details.
11. See Figure 20 for Thermal Model.
12. Thermal resistance from Junction-to-Ambient with all outputs ON and dissipating equal power.
13. Thermal resistance from Junction-to-Ambient with a single output ON.

STATIC ELECTRICAL CHARACTERISTICS (Characteristics noted under conditions of 4.75 V ≤ V_{DD} ≤ 5.25 V, 9.0 V ≤ V_{PWR} ≤ 16 V, – 40°C ≤ T_C ≤ 125°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
POWER INPUT					
Supply Voltage Range					V
Quasi-Functional (Note 1)	$V_{PWR(QF)}$	5.5	—	9.0	
Full Operational	$V_{PWR(FO)}$	9.0	—	26.5	
Supply Current (all Outputs ON, I_{out} = 0.5 A) (Note 2)	$I_{PWR(ON)}$	—	1.0	2.0	mA
Sleep State Supply Current (V_{DD} = 0.5 V)	$I_{PWR(SS)}$	—	1.0	50	µA
Sleep State Output Leakage Current (per Output, V_{DD} = 0.5 V)	$I_{out(SS)}$	—	—	50	µA
Overvoltage Shutdown	V_{OV}	28	—	36	V
Overvoltage Shutdown Hysteresis	$V_{OV(hys)}$	0.2	—	1.5	V
Logic Supply Voltage	V_{DD}	4.75	—	5.25	V
Logic Supply Current (with any combination of Outputs ON)	I_{DD}	—	—	4.0	mA
Logic Supply Undervoltage Lockout Threshold (Note 3)	$V_{DD(UVLO)}$	2.0	—	4.5	V
POWER OUTPUT					
Drain-to-Source ON Resistance (I_{out} = 0.5 A, T_J = 25°C)	$r_{DS(ON)}$				Ω
V_{PWR} = 5.5 V		—	—	1.0	
V_{PWR} = 9.0 V		—	0.4	0.5	
V_{PWR} = 13 V		—	0.35	0.45	
Drain-to-Source ON Resistance (I_{out}= 0.5 A, T_J = 150°C)	$r_{DS(ON)}$				Ω
V_{PWR} = 5.5 V		—	—	1.8	
V_{PWR} = 9.0 V		—	0.75	0.9	
V_{PWR} = 13 V		—	0.65	0.8	
Output Self-Limiting Current	$I_{out(Lim)}$				A
Outputs Programmed ON, V_{out} = 0.6 V_{DD}		3.0	4.0	6.0	
Output Fault Detect Threshold (Note 4)	$V_{outTH(F)}$				V_{DD}
Output Programmed OFF		0.6	0.7	0.8	
Output OFF Open Load Detect Current (Note 5)	I_{OCO}				µA
Output Programmed OFF, V_{out} = 0.6 V_{DD}		30	50	100	
Output Clamp Voltage	V_{OK}				V
I_{out} = 2.0 mA		50	65	75	
I_{out} = 0.2 A		55	—	75	
Output Leakage Current (V_{DD} ≤ 2.0 V) (Note 6)	$I_{out(LKG)}$	– 50	0	50	µA
Over Temperature Shutdown (Outputs OFF) (Note 7)	T_{Lim}	155	170	185	°C
Over Temperature Shutdown Hysteresis (Note 7)	$T_{Lim(hys)}$	—	10	20	°C

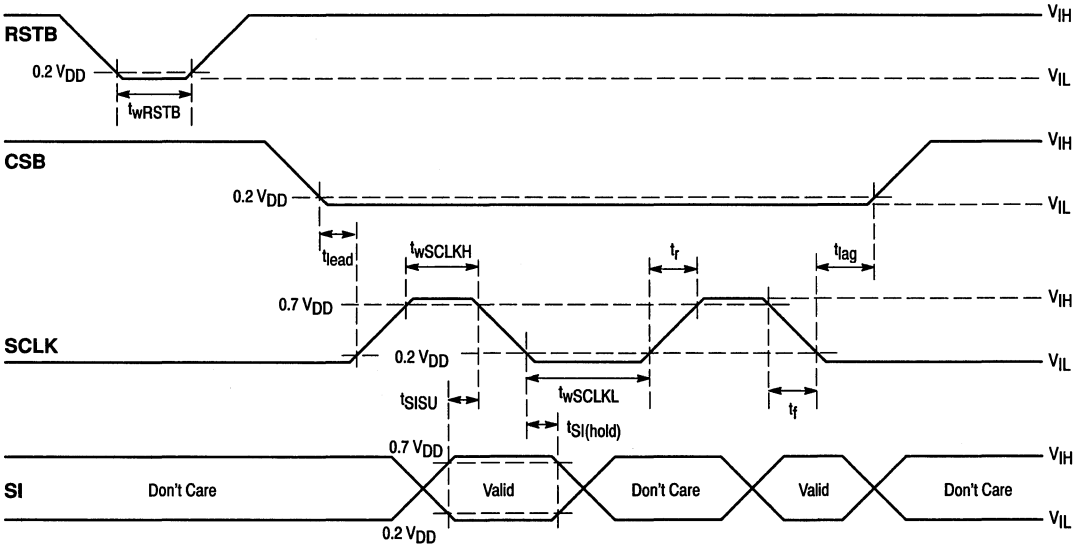
NOTES: 1. SPI inputs and outputs operational; Fault reporting may not be fully operational within this voltage range.
2. Value reflects normal operation (no faults) with all outputs ON. Each ON output contributes approximately 20 µA to I_{PWR}. Each output experiencing a "soft short" condition contributes approximately 0.5 mA to I_{PWR}. A "soft short" is defined as any load current causing the output source current to self-limit. A "hard" output short is a very low impedance short to supply.
3. For V_{DD} less than the Undervoltage Lockout Threshold voltage, all data registers are reset and all outputs are disabled.
4. Output fault detect threshold with outputs programmed OFF. Output fault detect thresholds are the same for output opens and shorts.
5. Output OFF Open Load Detect Current is the current required to flow through the load for the purpose of detecting the existence of an open condition when the specific output is commanded to be OFF.
6. Output leakage current measured with output OFF and at 16 V.
7. This parameter is guaranteed by design but is not production tested.

STATIC ELECTRICAL CHARACTERISTICS (Characteristics noted under conditions of 4.75 V ≤ V_{DD} ≤ 5.25 V, 9.0 V ≤ V_{PWR} ≤ 16 V, – 40°C ≤ T_C ≤ 125°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
DIGITAL INTERFACE					
Input Logic High Voltage (Note 1)	V_{IH}	0.7	0.5	1.0	V_{DD}
Input Logic Low Voltage (Note 2)	V_{IL}	0.0	0.5	0.2	V_{DD}
Input Logic Voltage Hysteresis (Note 3)	$V_{I(hys)}$	50	100	500	mV
Input Logic Current (Note 4)	I_{in}	–10	0	10	µA
Reset Pull-Up Current (Reset = 0.7 V_{DD})	I_{RSTB}	10	22	50	µA
SFPD Pull-Down Current (SFPD = 0.2 V_{DD})	I_{SFPD}	10	22	50	µA
SO High State Output Voltage (I_{OH} = 1.0 mA)	V_{SOH}	V_{DD} –1.0 V	V_{DD} – 0.6 V	—	V
SO Low State Output Voltage (I_{OL} = –1.6 mA)	V_{SOL}	—	0.2	0.4	V
SO Tri-State Leakage Current (CSB = 0.7 V_{DD}, 0 V ≤ V_{SO} ≤ V_{DD})	I_{SOT}	– 10	0	10	µA
Input Capacitance (0 V ≤ V_{DD} ≤ 5.25 V) (Note 5)	C_{in}	—	—	12	pF
SO Tri-State Capacitance (0 V ≤ V_{DD} ≤ 5.25 V) (Note 6)	C_{SOT}	—	—	20	pF

NOTES: 1. Upper logic threshold voltage range applies to SI, CSB, SCLK, Reset, and SFPD input signals.
2. Lower logic threshold voltage range applies to SI, CSB, SCLK, Reset, and SFPD input signals.
3. Only the SFPD and Reset inputs have hysteresis. This parameter is guaranteed by design but is not production tested.
4. Input current of SCLK, SI, and CSB logic control inputs.
5. Input capacitance of SI, CSB, SCLK, Reset, and SFPD for 0 V ≤ V_{DD} ≤ 5.25 V. This parameter is guaranteed by design, but is not production tested.
6. Tri-state capacitance of SO for 0 V ≤ V_{DD} ≤ 5.25 V. This parameter is guaranteed by design but is not production tested.

Figure 2. Input Timing Switch Characteristics



DYNAMIC ELECTRICAL CHARACTERISTICS (Characteristics noted under conditions of 4.75 V ≤ V_{DD} ≤ 5.25 V, 9.0 V ≤ V_{PWR} ≤ 16 V, – 40°C ≤ T_C ≤ 125°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
POWER OUTPUT TIMING					
Output Rise Time (V_{PWR} = 13 V, R_L = 26 Ω) (Note 1)	t_r	1.0	1.5	20	µs
Output Fall Time (V_{PWR} = 13 V, R_L = 26 Ω) (Note 1)	t_f	1.0	2.5	20	µs
Output Turn ON Delay Time (V_{PWR} = 13 V, R_L = 26 Ω) (Note 2)	$t_{DLY(ON)}$	1.0	5.0	15	µs
Output Turn OFF Delay Time (V_{PWR} = 13 V, R_L = 26 Ω) (Note 3)	$t_{DLY(off)}$	1.0	5.0	15	µs
Output Short Fault Disable Report Delay (Note 4) SFPD = 0.2 x V_{DD}	$t_{DLY(sf)}$	25	50	100	µs
Output OFF Fault Report Delay (Note 5) SFPD = 0.2 x V_{DD}	$t_{DLY(off)}$	25	50	100	µs

NOTES: 1. Output Rise and Fall time respectively measured across a 26 Ω resistive load at 10% to 90% and 90% to 10% voltage points.
2. Output Turn ON Delay time measured from rising edge of CSB to 50% of output OFF V_{out} voltage with RL = 26 Ω resistive load (see Figure 7 and 8).
3. Output Turn OFF Delay time measured from rising edge of CSB to 50% of output OFF V_{out} voltage with RL = 26 Ω resistive load (see Figure 7 and 8).
4. Output Short Fault Disable Report Delay measured from rising edge of CSB to I_{out} = 2.0 A point with output ON, V_{out} = 5.0 V, and SFPD = 0.2 x V_{DD} (see Figure 9 and 10).
5. Output OFF Fault Report Delay measured from 50% points of rising edge of CSB to rising edge of output (see Figure 8).

DYNAMIC ELECTRICAL CHARACTERISTICS (Characteristics noted under conditions of 4.75 V ≤ V_{DD} ≤ 5.25 V, 9.0 V ≤ V_{PWR} ≤ 16 V, – 40°C ≤ T_C ≤ 125°C, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
DIGITAL INTERFACE TIMING					
SCLK Clock Period	t_{pSCLK}	500	—	—	ns
SCLK Clock High Time	t_{wSCLKH}	250	—	—	ns
SCLK Clock Low Time	t_{wSCLKL}	250	—	—	ns
Required Low State Duration for Reset (V_{IL} ≤ 0.2 V_{DD}) (Note 1)	t_{wRSTB}	250	50	—	ns
Falling Edge of CSB to Rising Edge of SCLK (Required Setup Time)	t_{lead}	250	50	—	ns
Falling Edge of SCLK to Rising Edge of CSB (Required Setup Time)	t_{lag}	250	50	—	ns
SI to Falling Edge of SCLK (Required Setup Time)	t_{SISU}	125	25	—	ns
Falling Edge of SCLK to SI (Required Hold Time)	$t_{SI(hold)}$	125	25	—	ns
SO Rise Time (C_L = 120 pF)	t_{rSO}	—	25	50	ns
SO Fall Time (C_L = 120 pF)	t_{fSO}	—	25	50	ns
SI, CSB, SCLK Incoming Signal Rise Time (Note 2)	t_{rSI}	—	—	200	ns
SI, CSB, SCLK Incoming Signal Fall TIme (Note 2)	t_{fSI}	—	—	200	ns
Time from Falling Edge of CSB to SO Low Impedance (Note 3) HIgh Impedance (Note 4)	 $t_{SO(en)}$ $t_{SO(dis)}$	 — —	 — —	 200 200	ns
Time from Rising Edge of SCLK to SO Data Valid (Note 5) 0.2 V_{DD} ≤ SO ≥ 0.8 VDD, C_L = 200 pF	t_{Valid}	—	50	125	ns

NOTES: 1. Reset Low duration measured with outputs enabled and going to OFF or disabled condition.
2. Rise and Fall time of incoming SI, CSB, and SCLK signals suggested for design consideration to prevent the occurrence of double pulsing.
3. Time required for output status data to be available for use at SO.
4. Time required for output status data to be terminated at SO.
5. Time required to obtain valid data out from SO following the rise of SCLK.

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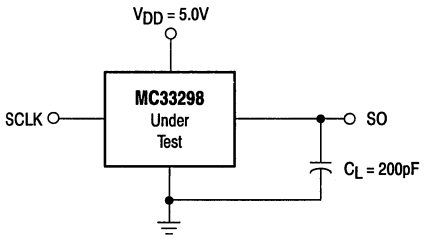
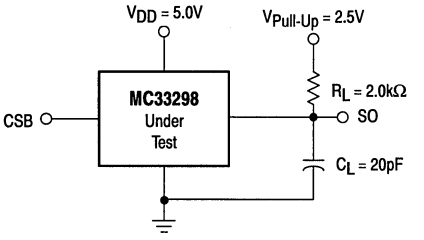
Figure 3. Valid Data Delay Time and Valid Time Test Circuit



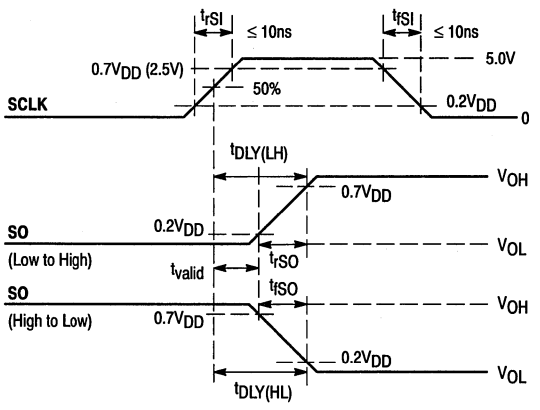
C_L represents the total capacitance of the test fixture and probe.

Figure 5. Enable and Disable Time Test Circuit



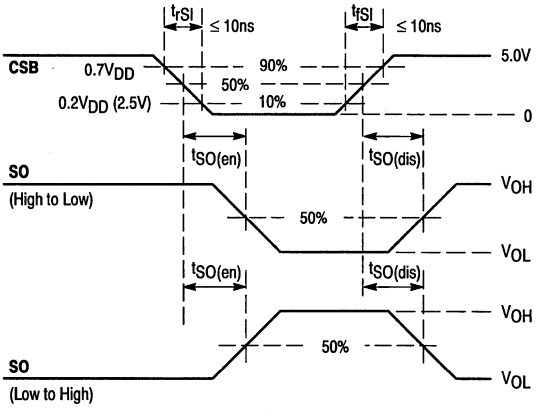
C_L represents the total capacitance of the test fixture and probe.

Figure 4. Vaild Data Delay Time and Valid Time Waveforms



SO (low-to-high) is for an output with internal conditions such that the low-to-high transition of CSB causes the SO output to switch from high to low.

Figure 6. Enable and Disable Time Waveforms



NOTES: 1. SO (high-to-low) waveform is for SO output with internal conditions such that SO output is low except when an output is disabled as a result of detecting a circuit fault with CSB in a High Logic state (e.g., open load).
2. SO (low-to-high) waveform is for SO output with internal conditions such that SO output is high except when an output is disabled as a result of detecting a circuit fault with CSB in a High Logic state (e.g., shorted load).

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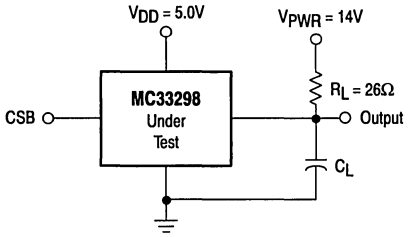
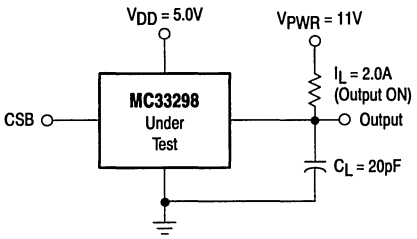
Figure 7. Switching Time Test Circuit



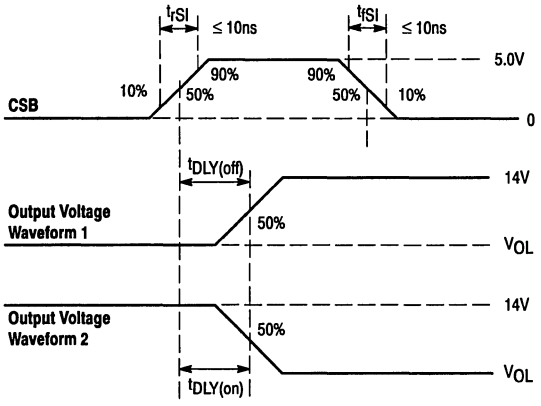
C_L represents the total capacitance of the test fixture and probe.

Figure 9. Output Fault Unlatch Disable Delay Test Circuit



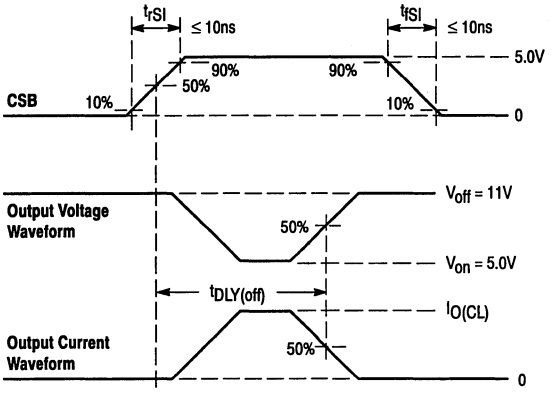
C_L represents the total capacitance of the test fixture and probe.

Figure 8. Turn-ON/OFF Waveforms



NOTES: 1. $t_{DLY(on)}$ and $t_{DLY(off)}$ are turn-on and turn-off propagation delay times.
2. Waveform 1 is an output programmed from an ON to an OFF state.
3. Waveform 2 is an output programmed from an OFF to an ON state.

Figure 10. Output Fault Unlatch Disable Delay Waveforms



NOTES: 1. $t_{pDLY(off)}$ is the output fault unlatch disable propagation delay time required to correctly report an output fault after CSB rises. Represents an output commanded ON while having an existing output short (overcurrent) to supply.
2. SFPD pin ≤ 0.2 V.

CIRCUIT DESCRIPTION

Introduction

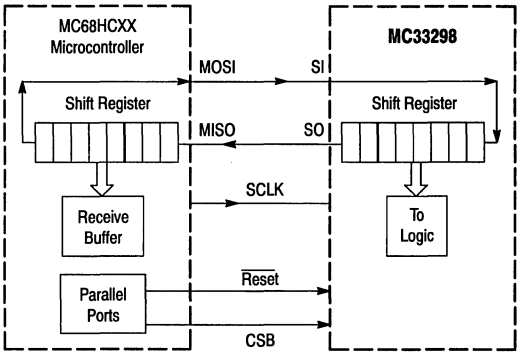
The MC33298 was conceived, specified, designed, and developed for automotive applications. It is an eight output low side power switch having 8-bit serial control. The MC33298 incorporates SMARTMOS™ technology having effective 2.0 μ CMOS logic, bipolar/MOS analog circuitry, and independent state of the art double diffused MOS (DMOS) power output transistors. Many benefits are realized as a direct result of using this mixed technology. A simplified block diagram of the MC33298 is shown in Figure 1.

Where bipolar devices require considerable control current for their operation, structured MOS devices, since they are voltage controlled, require only transient gate charging current affording a significant decrease in power consumption. The CMOS capability of the SMARTMOS™ process allows significant amounts of logic to be economically incorporated into the monolithic design. In addition, bipolar/MOS analog circuits embedded within the updrain power DMOS output transistors monitor and provide fast, independent protection control functions for each individual output. All outputs have internal 65 V at 0.5 A independent output voltage clamps to provide fast inductive turn-off and transient protection.

The MC33298 uses high efficiency updrain power DMOS output transistors exhibiting very low drain to source ON resistance values ($r_{DS(ON)} \leq 0.45\ \Omega$) and dense CMOS control logic. Operational bias currents of less than 4.0 mA (1.0 mA typical) with any combination of outputs ON are the result of using this mixed technology and would not be possible with bipolar structures. To accomplish a comparable functional feature set using a bipolar structure approach would result in a device requiring hundreds of milliamperes of internal bias and control current. This would represent a very large amount of power to be consumed by the device itself and not available for load use.

In operation the MC33298 functions as an eight output serial switch serving as a microcontroller (MCU) bus expander and buffer with fault management and fault reporting features. In doing so, the device directly relieves the MCU of the fault management functions. The MC33298 directly interfaces to an MCU and operates at system clock serial frequencies in excess of 2.0 MHz using a Synchronous Peripheral Interface (SPI) for control and diagnostic readout. Figure 12 shows the basic SPI configuration between an MCU and one MC33298.

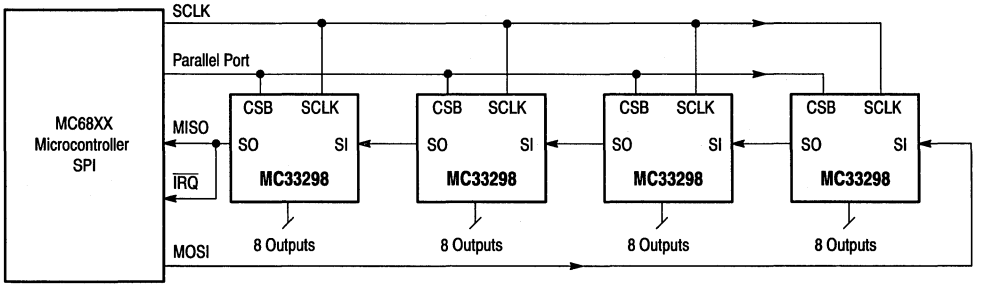
Figure 12. SPI Interface with Microcontroller



The circuit can also be used in a variety of other applications in the computer, telecommunications, and industrial fields. It is parametrically specified over an input "battery"/supply range of 9.0 V to 16 V but is designed to operate over a considerably wider range of 5.5 V to 26.5 V. The design incorporates the use of Logic Level MOSFETs as output devices. These MOSFETs are sufficiently turned ON with a gate voltage of less than 5.0 V thus eliminating the need for an internal charge pump. Each output is identically sized and independent in operation. The efficiency of each output transistor is such that with as little as 9.0 V supply (V_{PWR}), the maximum $r_{DS(ON)}$ of an output at room temperature is 0.45 Ω (0.35 Ω typical) and increases to only 1.0 Ω (0.5 Ω typical) as V_{PWR} is decreased to 5.5 V.

All inputs are compatible with 5.0 V CMOS logic levels and incorporate negative or inverted logic. Whenever an input is programmed to a logic low state (< 1.0 V) the corresponding low side switched output being controlled will be active low and turned ON. Conversely, whenever an input is programmed to a logic high state (> 3.0 V), the output being controlled will be high and turned OFF.

Figure 11. MC33298 SPI System Daisy Chain



One main advantage of the MC33298 is the serial port which when coupled to an MCU, receives ON/OFF commands from the MCU and in return transmits the drain status of the device's output switches. Many devices can be "daisy-chained" together to form a larger system (see Figure 11). Note in this example that only one dedicated MCU parallel port (aside from the required SPI) is needed for chip select to control 32 possible loads.

Multiple MC33298 devices can also be controlled in a parallel input fashion using SPI (see Figure 13). This figure shows a possible 24 loads being controlled by only three dedicated parallel MCU ports used for chip select.

Figure 13. Parallel Input SPI Control

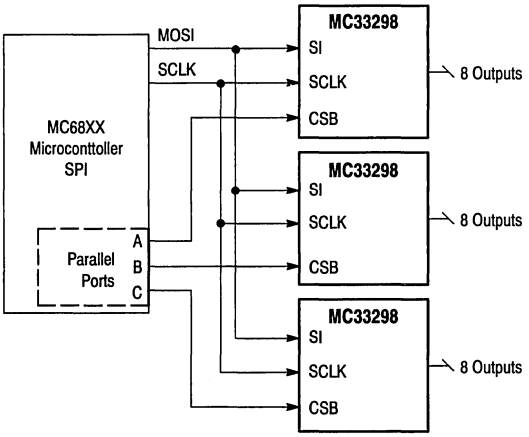


Figure 14 shows a basic method of controlling multiple MC33298 devices using two MCUs. A system can have only one master MCU at any given instant of time and one or more slave MCUs. The master MCU supplies the system clock signal (top MCU designated the master); the lower MCU being the slave. It is possible to have a system with more than one master but not at the same time. Only when the master is not communicating can a slave communicate. MCU master control is switched through the use of the slave select (SS) pin of the MCUs. A master will become a slave when it detects a logic low state on its SS pin.

These basic examples make the MC33298 very attractive for applications where a large number of loads need be controlled efficiently. The popular Synchronous Serial Peripheral Interface (SPI) protocol is incorporated, to this end, to communicate efficiently with the MCU.

SPI System Attributes

The SPI system is flexible enough to communicate directly with numerous standard peripherals and MCUs available from Motorola and other semiconductor manufacturers. SPI reduces the number of pins necessary for input/output (I/O) on the MC33298. It also offers an easy means of expanding the I/O function using few MCU pins. The SPI system of communication consists of the MCU transmitting, and in return, receiving one databit of information per clock cycle.

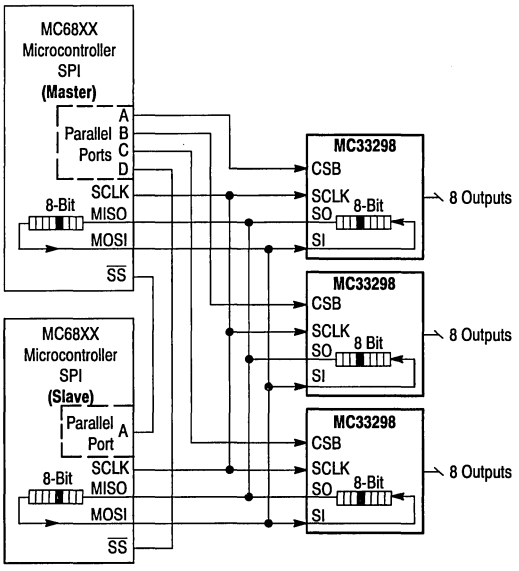
Databits of information are simultaneously transmitted by one pin, Microcontroller Out Serial In (MOSI), and received by another pin, Microcontroller In Serial Out (MISO), of the MCU.

Some features of SPI are:

- Full Duplex, Three-Wire Synchronous Data Transfer
- Each Microcontroller can be a Master or a Slave
- Provides Write Collision Flag Protection
- Provides End of Message Interrupt Flag
- Four I/Os associated with SPI (MOSI, MISO, SCLK, SS)

The only drawbacks to SPI are that an MCU is required for efficient operational control and, in contrast to parallel input control, is slower at performing pulse width modulating (PWM) functions.

Figure 14. Multiple MCU SPI Control



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PIN FUNCTION DESCRIPTION

CSB Pin

The system MCU selects the MC33298 to be communicated with through the use of the CSB pin. Whenever the pin is in a logic low state, data can be transferred from the MCU to the MC33298 and vise versa. Clocked-in data from the MCU is transferred from the MC33298 shift register and latched into the power outputs on the rising edge of the CSB signal. On the falling edge of the CSB signal, drain status information is transferred from the power outputs and loaded into the device's shift register. The CSB pin also controls the output driver of the serial output pin. Whenever the CSB pin goes to a logic low state, the SO pin output driver is enabled allowing information to be transferred from the MC33298 to the MCU. To avoid any spurious data, it is essential that the high-to-low transition of the CSB signal occur only when SCLK is in a logic low state.

SCLK Pin

The system clock pin (SCLK) clocks the internal shift registers of the MC33298. The serial input pin (SI) accepts data into the input shift register on the falling edge of the SCLK signal while the serial output pin (SO) shifts data information out of the shift register on the rising edge of the SCLK signal. False clocking of the shift register must be avoided to guarantee validity of data. It is essential that the SCLK pin be in a logic low state whenever chip select bar pin (CSB) makes any transition. For this reason, it is recommended though not necessary, that the SCLK pin be kept in a low logic state as long as the device is not accessed (CSB in logic high state). When CSB is in a logic high state, any signal at the SCLK and SI pin is ignored and SO is tristated (high impedance). See the Data Transfer Timing diagram of Figure 16.

SI Pin

This pin is for the input of serial instruction data. SI information is read in on the falling edge of SCLK. A logic high state present on this pin when the SCLK signal rises will program a specific output OFF, and in turn, turns OFF the specific output on the rising edge of the CSB signal. Conversely, a logic low state present on the SI pin will program the output ON, and in turn, turns ON the specific output on the rising edge of the CSB signal. To program the eight outputs of the MC33298 ON or OFF, an eight bit serial stream of data is required to be entered into the SI pin starting with Output 7, followed by Output 6, Output 5, etc., to Output 0. For each rise of the SCLK signal, with CSB held in a logic low state, a databit instruction (ON or OFF) is loaded into the shift register per the databit SI state. The shift register is full after eight bits of information have been entered. To preserve data integrity, care should be taken to not transition SI as SCLK transitions from a low to high logic state.

SO Pin

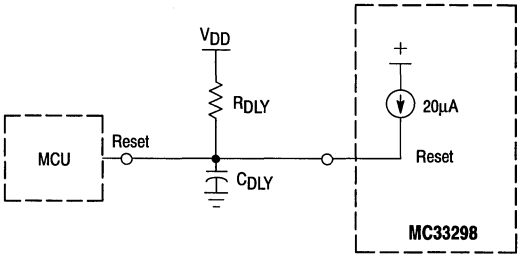
The serial output (SO) pin is the tri-stateable output from the shift register. The SO pin remains in a high impedance state until the CSB pin goes to a logic low state. The SO data reports the drain status, either high or low. The SO pin changes state on the rising edge of SCLK and reads out on the falling edge of SCLK. When an output is OFF and not faulted, the corresponding SO databit is a high state. When an output is ON, and there is no fault, the corresponding databit on the SO pin will be a low logic state. The SI/SO shifting of data follows a first-in-first-out protocol with both input and output words transferring the Most Significant Bit (MSB) first. The SO pin is not affected by the status of the Reset pin.

Reset Pin

The MC33298 Reset pin is active low and used to clear the SPI shift register and in doing so sets all output switches OFF. With the device in a system with an MCU; upon initial system power up, the MCU holds the Reset pin of the device in a logic low state ensuring all outputs to be OFF until both the V_{DD} and V_{PWR} pin voltages are adequate for predictable operation. After the MC33298 is reset, the MCU is ready to assert system control with all output switches initially OFF. If the V_{PWR} pin of the MC33298 experiences a low voltage, following normal operation, the MCU should pull the Reset pin low so as to shutdown the outputs and clear the input data register. The Reset pin is active low and has an internal pull-up incorporated to ensure operational predictability should the external pull-up of the MCU open circuit. The internal pull-up is only 20 µA to afford safe and easy interfacing to the MCU. The Reset pin of the MC33298 should be pulled to a logic low state for a duration of at least 250 ns to ensure reliable reset.

A simple power ON reset delay of the system can be programmed through the use of an RC network comprised of a shunt capacitor from the Reset pin to Ground and a resistor to V_{DD} (See Figure 15). Care should be exercised to ensure proper discharge of the capacitor so as to not adversely delay the reset nor damage the MCU should the MCU pull the Reset line low and yet accomplish initialization for turn ON delay. It may be easier to incorporate delay into the software program and use a parallel port pin of the MCU to control the MC33298 Reset pin.

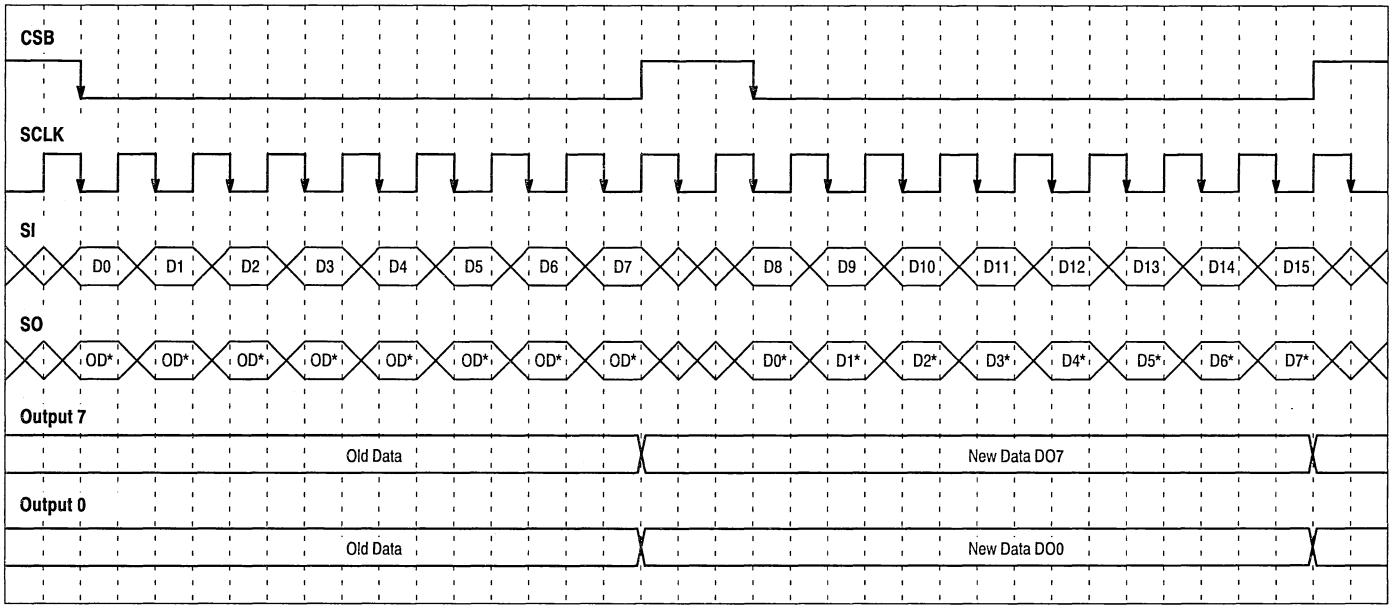
Figure 15. Power ON Reset



SFPD Pin

The Short Fault Protect Disable (SFPD) pin is used to disable the over current latch-OFF. This feature allows control of incandescent loads where in-rush currents exceed the device's analog current limits. Essentially the SFPD pin determines whether the MC33298 output(s) will instantly shut down upon sensing an output short or remain ON in a current limiting mode of operation until the output short is removed or thermal shutdown is reached. If the SFPD pin is tied to V_{DD} = 5.0 V the MC33298 output(s) will remain ON in a current limited mode of operation upon encountering a load short to supply. If the SFPD pin is grounded, a short circuit will immediately shut down only the output affected. Other outputs not having a fault condition will operate normally. The short circuit operation is addressed in more detail later.

Figure 16. Data Transfer Timing



NOTES:1. $\overline{\text{Reset}}$ pin is in a logic high state during the above operation.
2. D0, D1, D2, ..., and D15 relate to the ordered entry of program data into the MC33298 with D0/D8 bits (MSB) corresponding to Output 7 and D7/D15 corresponding to Output 0.
3. D0*, D1*, D2*, ..., and D7* relate to the ordered data out of the MC33298 with D0* bit (MSB) corresponding to Output 7.
4. OD* corresponds to Old Databits.
5. For brevity, only DO7 and DO0 are shown which respectively correspond to Output 7 and Output 0.

Data Transfer Timing (General)

CSB High-to-Low	SO pin is enabled. Output Status information transferred to Output Shift Register.
CSB Low-to-High	Data from the Shift Register is transferred to the Output Power Switches
SO	Will change state on the rising edge of the SCLK pin signal.
SI	Will accept data on the falling edge of the SCLK pin signal.

Power Consumption

The MC33298P has extremely low power consumption in both the operating and standby modes. In the standby or "sleep" mode, with $V_{DD} \leq 2.0$ V, the current consumed by the V_{PWR} pin is less than 50 μA. In the operating mode, the current drawn by the V_{DD} pin is less than 4.0 mA (1.0 mA typical) while the current drawn at the V_{PWR} pin is 2.0 mA maximum (1.0 mA typical). During normal operation, turning outputs ON increases I_{PWR} by only 20 μA per output. Each output experiencing a "soft short" (overcurrent conditions just under the current limit), adds 0.5 mA to the I_{PWR} current.

Paralleling of Outputs

Using MOSFETs as output switches allows the connection of any combination of outputs together. MOSFETs have an inherent positive temperature coefficient thermal feedback which modulates $r_{DS(ON)}$ providing balanced current sharing between outputs without destructive operation (bipolar outputs could not be paralleled in this fashion as thermal run-away would likely occur). The device can even be operated with all outputs tied together. This mode of operation may be desirable in the event the application requires lower power dissipation or the added capability of switching higher currents. Performance of parallel operation results in a corresponding decrease in $r_{DS(ON)}$ while the Output Off Open Load Detect Currents and the Output Current Limits increase correspondingly (by a factor of eight if all outputs are paralleled). Less than 56 mΩ $r_{DS(ON)}$ with current limiting of 24 to 48 A will result if all outputs are paralleled together. There will be no change in the Overvoltage detect or the OFF Output Threshold Voltage Range. The advantage of paralleling outputs within the same MC33298 affords the existence of minimal $r_{DS(ON)}$ and output clamp voltage variation between outputs. Typically, the variation of $r_{DS(ON)}$ between outputs of the same device is less than is 0.5%. The variation in clamp voltages (which could affect dynamic current sharing) is less than 5%. Paralleling outputs from two or more devices is possible but not recommended. This is because there is no guarantee that the $r_{DS(ON)}$ and clamp voltage of the two devices will match. System level thermal design analysis and verification should be conducted whenever paralleling outputs.

FAULT LOGIC OPERATION

General

The MCU can perform a parity check of the fault logic operation by comparing the command 8-bit word to the status 8-bit word. Assume that after system reset, the MCU first sends an 8-bit command word, Command Word 1, to the MC33298. Each output that is to be turned ON will have its corresponding databit low. Refer to the Data Transfer Timing diagram of Figure 16. As this word, Command Word 1, is being written into the shift register of the MC33298, a status word is being simultaneously written out and received by the MCU. However, the word being received by the MCU is the status of the previous write word to the MC33298, Status Word 0. If the command word of the MCU is written a second time (Command Word 2 = Command Word 1), the word received by the MCU, Status Word 2, is the status of Command Word 1. The timing diagram shown in Figure 16 depicts this operation. Status Word 2 is then compared with Command Word 1. The MCU will Exclusive *or* Status Word 2 with Command Word 1 to determine if the two words are identical. If the two words are identical, no faults exist. The timing between the two write words must be greater than 100 μs to receive proper drain status. The system databus integrity may be tested by writing two like words to the MC33298 within a few microseconds of each other.

Initial System Setup Timing

The MCU can monitor two kinds of faults:
(1) Communication errors on the data bus and
(2) Actual faults of the output loads.

After initial system start up or reset, the MCU will write one word to the MC33298. If the word is repeated within a few microseconds (say 5) of the first word, the word received by the MCU, at the end of the repeated word, serves as a confirmation of data bus integrity (1). At startup, the MC33298 will take 25 to 100 μs before a repeat of the first word can give the actual status of the outputs. Therefore, the first word should be repeated at least 100 μs later to verify the status of the outputs.

The SO of the MC33298 will indicate any one of four faults. The four possible faults are Over Temperature, Output Off Open Fault, Short Fault (overcurrent), and V_{PWR} Overvoltage Fault. All of these faults, with the exception of the Overvoltage Fault, are output specific. Over Temperature Detect, Output Off Open Detect, and Output Short Detect are dedicated to each output separately such that the outputs are independent in operation. A V_{PWR} Overvoltage Detect is of a "global" nature causing all outputs to be turned OFF.

Over Temperature Fault

Patent pending Over Temperature Detect and shutdown circuits are specifically incorporated for each individual output. The shutdown that follows an Over Temperature condition is independent of the system clock or any other logic signal. Each independent output shuts down at 155°C to 185°C. When an output shuts down due to an Over Temperature Fault, no other outputs are affected. The MCU recognizes the fault since the output was commanded to be ON and the status word indicates that it is OFF. A maximum hysteresis of 20°C ensures an adequate time delay between output turn OFF and recovery. This avoids a very rapid turn ON and turn OFF of the device around the Over Temperature threshold. When the temperature falls below the recovery level for the Over Temperature Fault, the device will turn ON only if the Command Word during the next write cycle indicates the output should be turned ON.

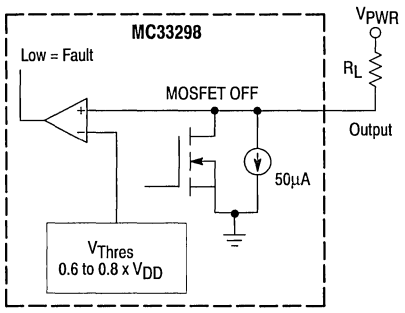
Overvoltage Fault

An Overvoltage condition on the V_{PWR} pin will cause the MC33298 to shut down all outputs until the overvoltage condition is removed and the device is re-programmed by the SPI. The overvoltage threshold on the V_{PWR} pin is specified as 28 V to 34 V with 1.0 V typical hysteresis. Following the overvoltage condition, the next write cycle sends the SO pin the hexadecimal word $FF (all ones) indicating all outputs are turned OFF. In this way, potentially dangerous timing problems are avoided and the MCU reset routine ensures an orderly startup of the loads. The MC33298 does not detect an overvoltage on the V_{DD} pin. Other external circuitry, such as the Motorola MC33161 Universal Voltage Monitor, is necessary to accomplish this function.

Output Off Open Load Fault

An Output Off Open Load Fault is the detection and reporting of an "open" load when the corresponding output is disabled (input in a logic high state). To understand the operation of the Open Load Fault detect circuit, see Figure 17. The Output Off Open Load Fault is detected by comparing the drain voltage of the specific MOSFET output to an internally generated reference. Each output has one dedicated comparator for this purpose.

Figure 17. Output OFF Open Load Detect



An Output Off Open Load Fault is indicated when the output voltage is less than the Output Threshold Voltage (V_{Thres}) of 0.6 to 0.8 x V_{DD}. Since the MC33298 outputs function as switches, during normal operation, each MOSFET output should either be completely turned ON or OFF. By design the threshold voltage was selected to be between the ON and OFF voltage of the MOSFET. During normal operation, the ON state V_{DS} voltage of the MOSFET is less than the threshold voltage and the OFF state V_{DS} voltage is greater than the threshold voltage. This design approach affords using the same threshold comparator for Output Open Load Detect in the OFF state and Short Circuit Detect in the ON state. See Figure 18 for an understanding of the Short Circuit Detect circuit. With V_{DD} = 5.0 V, an OFF state output voltage of less than 3.0 V will be detected as an Output Off Open Load Fault while voltages greater than 4.0 V will not be detected as a fault.

The MC33298 has an internal pull-down current source of 50 µA, as shown in Figure 17, between the MOSFET drain and ground. This prevents the output from floating up to V_{PWR} if there is an open load or internal wirebond failure. The internal comparator compares the drain voltage with a reference voltage, V_{Thres} (0.6 to 0.8 x V_{DD}). If the output voltage is less than this reference voltage, the MC33298 will declare the condition to be an open load fault.

During steady-state operation, the minimum load resistance (R_L) needed to prevent false fault reporting during normal operation can be found as follows:

$$V_{PWR} = 9.0\ V\ (min)$$
$$I_{LCO} = 50\ \mu A$$
$$V_{Thres}\ (max) = (0.8 \bullet 5.25)V = 4.2\ V$$

Therefore, the load resistance necessary to prevent false open load fault reporting is (using Ohm's Law) equal to 96 kΩ or less.

During output switching, especially with capacitive loads, a false Output Off Open Load Fault may be triggered. To prevent this false fault from being reported an internal fault filter of 25 to 100 µs is incorporated. The duration for which a false fault may be reported is a function of the load impedance (R_L, C_L, L_L), $r_{DS(ON)}$, and C_{out} of the MOSFET as well as the supply voltage, V_{PWR}. The rising edge of CSB triggers a built in fault delay timer which must time out (25 to 100 µs) before the fault comparator is enabled to detect a faulted threshold. The circuit automatically returns to normal operation once the condition causing the Open Load Fault is removed.

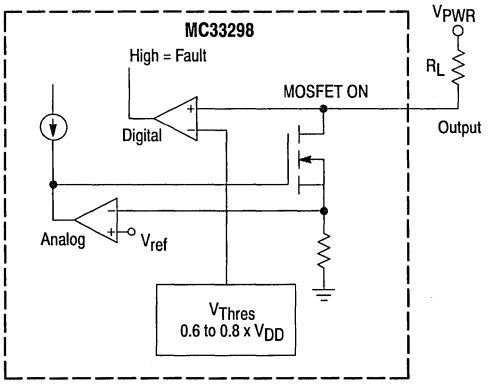
Shorted Load Fault

A shorted load (overcurrent) fault can be caused by any output being shorted directly to supply, or an output experiencing a current greater than the current limit.

There are three safety circuits progressively in operation during load short conditions which afford system protection: 1) The device's output current is monitored in an analog fashion using a SENSEFET™ approach and limited; 2) The device's output current limit threshold is sensed by monitoring the MOSFET drain voltage; and 3) The device's output thermal limit is sensed and when attained causes only the specific faulted output to be latched OFF, allowing remaining outputs to operate normally. All three protection mechanisms are incorporated in each output affording robust independent output operation.

The analog current limit circuit is always active and monitors the output drain current. An overcurrent condition causes the gate control circuitry to reduce the gate to source voltage imposed on the output MOSFET which re-establishes the load current in compliance with current limit (3.0 to 6.0 A) range. The time required for the current limit circuitry to act is less than 20 µs. Therefore, currents higher than 3.0 to 6.0 A will never be seen for more than 20 µs (a typical duration is 10 µs). If the current of an output attempts to exceed the predetermined limit of 3.0 to 6.0 A (4.0 A nominal), the V_{DS} voltage will exceed the V_{Thres} voltage and the overcurrent comparator will be tripped as shown in Figure 18.

Figure 18. Short Circuit Detect and Analog Current Limiting Circuit



The status of SFPD will determine whether the MC33298 will shut down or continue to operate in an analog current limited mode until either the short circuit is removed or thermal shutdown is reached.

Grounding the SFPD pin will enable the short fault protection shutdown circuitry. Consider a load short (output short to supply) occurring on an output before, during, and after output turn ON. When the CSB signal rises to the high logic state, the corresponding output is turned ON and a delay timer activated. The duration of the delay timer is 25 to 100 µs. If the short circuit takes place before the output is turned ON, the delay experienced is the entire 25 to 100 µs followed by shutdown. If the short occurs during the delay time, the shutdown still occurs after the delay time has elapsed. If the short circuit occurs after the delay time, shut- down is immediate (within 20 µs after sensing). The purpose of the delay timer is to prevent false faults from being reported when switching capacitive loads.

If the SFPD pin is at 5.0 V (or V_{DD}), an output will not be disabled when overcurrent is detected. The specific output will, within 5.0 to 10 µs of encountering the short circuit, go into an analog current limited mode. This feature is especially useful when switching incandescent lamp loads, where high in-rush currents experienced during startup last for 10 to 20 ms.

Each output of the MC33298 has its own overcurrent shutdown circuitry. Over temperature faults and the overvoltage faults are not affected by the SFPD pin.

Both load current sensing and output voltage sensing are incorporated for Short Fault detection with actual detection occurring slightly after the onset of current limit. The current limit circuitry incorporates a SENSEFET™ approach to measure the total drain current. This calls for the current through a small number of cells in the power MOSFET to be measured and the result multiplied by a constant to give the total current. Whereas output shutdown circuitry measures the drain to source voltage and shuts down if a threshold (V_{Thres}) is exceeded.

10

Short Fault detection is accomplished by sensing the output voltage and comparing it to V_{Thres}. The lowest V_{Thres} requires a voltage of 0.6 times 4.75 V (the minimum V_{DD} voltage) or 2.85 V to be sensed. For an enabled output, with V_{DD} = 5.0 ± 0.25 V, an output voltage in excess of 4.2 V will be detected as a "short" while voltages less than 2.85 V will not be detected as "shorts."

Over Current Recovery

If the SFPD pin is in a high logic state, the circuit returns to normal operation automatically after the short circuit is removed (unless thermal shutdown has occurred).

If the SFPD pin is grounded and overcurrent shutdown occurs; removal of the short circuit will result in the output remaining OFF until the next write cycle. If the short circuit is not removed, the output will turn ON for the delay time (25 to 100 µs) and then turn OFF for every write cycle commanding a turn ON.

SFPD Pin Voltage Selection

Since the voltage condition of the SFPD pin controls the activation of the short fault protection (i.e. shutdown) mode equally for all eight outputs, the load having the longest duration of in-rush current determines what voltage (state) the SFPD pin should be at. Usually if at least one load is, say an incandescent lamp, the in-rush current on that input will be milliseconds in duration. Therefore, setting SFPD at 5.0 V will prevent shutdown of the output due to the in-rush current. The system relies only on the Over Temperature Shutdown to protect the outputs and the loads. The MC33298 was designed to switch GE194 incandescent lamps with the SFPD pin in a grounded state. Considerably larger lamps can be switched with the SFPD pin held in a high logic state.

Sometimes both a delay period greater than 25 to 100 µs (current limiting of the output) followed by an immediate over current shutdown is necessary. This can be accomplished by programming the SFPD pin to 5.0 V for the extended delay period to afford the outputs to remain ON in a current limited mode and then grounding it to accomplish the immediate shutdown after some period of time. Additional external circuitry is required to implement this type of function. An MCU parallel output port can be devoted to controlling the SFPD voltage during and after the delay period, is often a much better method. In either case, care should be taken to execute the SFPD start-up routine every time start-up or reset occurs.

Undervoltage Shutdown

An undervoltage V_{DD} condition will result in the global shutdown of all outputs. The undervoltage threshold is between 2.5 V and 4.5 V. When V_{DD} goes below the threshold, all outputs are turned OFF and the SO register is reset to indicate the same.

An undervoltage condition at the V_{PWR} pin will not cause output shutdown and reset. When V_{PWR} is between 5.5 V and 9.0 V, the outputs will operate per the command word. However, the status as reported by the serial output (SO) pin may not be accurate. Proper operation at V_{PWR} voltages below 5.5 V cannot be guaranteed.

Deciphering Fault Type

The MC33298 SO pin can be used to understand what kind of system fault has occurred. With eight outputs having open load, over current and over temperature faults, a total of 25 different faults are possible. The SO status word received by the MCU will be compared with the word sent to the MC33298 during the previous write cycle. If the two words are not the same, then the MCU should be programmed to determine which output or outputs are indicating faults. If the command bit for any of the output switches indicating a fault is high, the fault is an open load.

The eight open load faults are therefore the ones most easily detected. Over current and over temperature faults are often related. Turning the affected output switches OFF and waiting for some time should make these faults go away. Over current and over temperature faults can not be differentiated in normal application usage.

One advantage of the synchronous serial output is that multiple faults can be detected with only one pin (SO) being used for fault status indication.

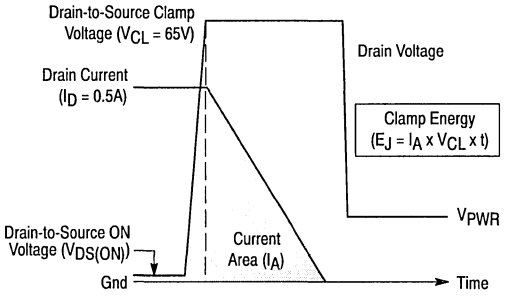
If V_{PWR} experiences an overvoltage condition, all outputs will immediately be turned OFF and remain latched OFF. A new command word is required to turn the outputs back ON following an overvoltage condition.

Output Voltage Clamping

Each output of the MC33298 incorporates an internal voltage clamp to provide fast turn-off and transient protection of the output. Each clamp independently limits the drain to source voltage to 65 V at drain currents of 0.5 A and keeps the output transistors from avalanching by causing the transient energy to be dissipated in the linear mode (see Figure 19). The total energy (E_J) can be calculated by multiplying the current area under the current curve (I_A) during the time the clamp is active and the clamp voltage (V_{CL}).

Characterization of the output clamps, using a single pulse repetitive method at 0.5 A, indicate the maximum energy to be 100 mJ at 25°C and 25 mJ at 125°C per output. Using a single pulse non-repetitive method at 0.5 A the clamps are capable of 2.0 Joules at 25°C and 0.5 Joules at 125°C.

Figure 19. Output Voltage Clamping



THERMAL CHARACTERIZATION

Thermal Model

Logic functions take up a very small area of the die and generate negligible power. In contrast, the output transistors take up most of the die area and are the primary contributors of power generation. The thermal model shown in Figure 20 was developed for the MC33298 mounted on a typical PC board. The model is accurate for both steady state and transient thermal conditions. The components R_{d0}, R_{d1}, R_{d2}, ..., and R_{d7} represent the steady state thermal resistance of the silicon die for transistor outputs 0, 1, 2, ..., and 7, while C_{d0}, C_{d1}, C_{d2}, ..., and C_{d7} represent the corresponding thermal capacitance of the silicon die transistor outputs and plastic. The device area and die thickness determine the values of these specific components.

The thermal impedance of the package from the internal mounting flag to the outside environment is represented by the terms R_{pkg} and C_{pkg}. The steady state thermal resistance of leads and the PC board make up the steady state package thermal resistance, R_{pkg}. The thermal capacitance of the package is made up of the combined capacitance of the flag and the PC board. The mold compound was not modeled as a specific component but is factored into the other overall component values.

The battery voltage in the thermal model represents the ambient temperature the device and PC board are subjected to. The I_{PWR} current source represents the total power dissipation and is calculated by adding up the power dissipation of each individual output transistor. This is easily done by knowing $r_{DS(ON)}$ and load current of the individual outputs.

Very satisfactory steady state and transient results have been experienced with this thermal model. Tests indicate the model accuracy to have less than 10% error. Output interaction with an adjacent output is thought to be the main contributor to the thermal inaccuracy. Tests indicate little or no detectable thermal affects caused by distant output transistors which are isolated by one or more other outputs. Tests were conducted with the device mounted on a typical PC board placed horizontally in a 33 cubic inch still air enclosure. The PC board was made of FR4 material measuring 2.5″ by 2.5″, having double-sided circuit traces of 1.0 oz. copper soldered to each device pin. The board temperature was measured with thermal couple soldered to the board surface one inch away from the center of the device. The ambient temperature of the enclosure was measured with a second thermal couple located over the center and one inch distant from device.

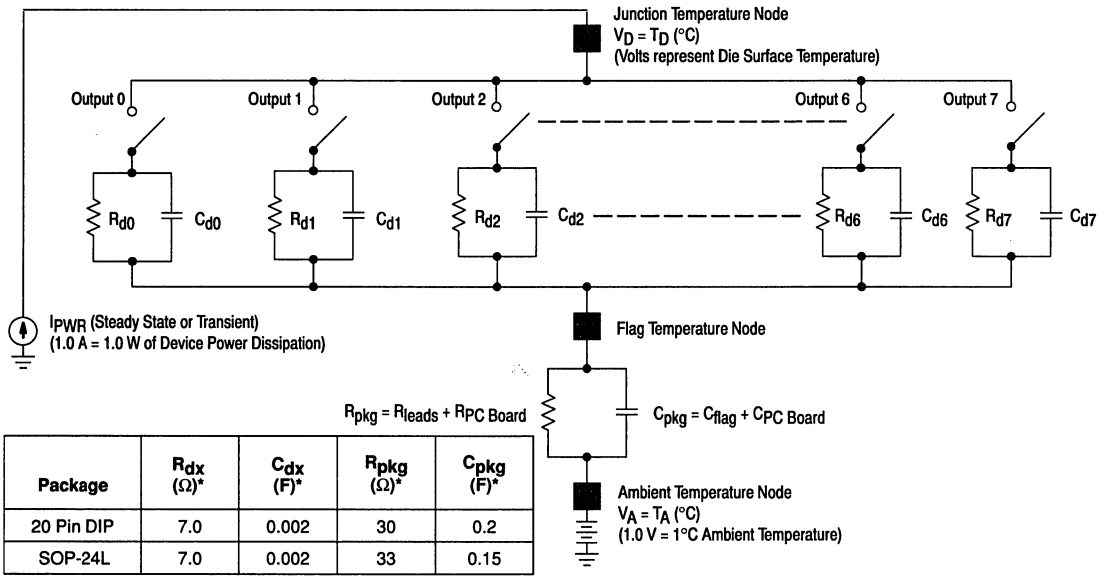
Thermal Performance

Figure 20 shows the worst case thermal component parameters values for the MC33298 in the 20 pin plastic power DIP and the SOP-24 wide body surface mount package. The power DIP package has Pins 5, 6, 15, and 16 connected directly to the lead frame flag. The parameter values indicated take into account adjacent output cell thermal pulling effects as well as different output combinations. The characterization was conducted over power dissipation levels of 0.7 to 17 W. The junction-to-ambient temperature thermal resistance was found to be 37°C/W with a single output active (31°C/W with all outputs dissipating equal power) and in conjunction with this, the thermal resistance from junction to PC board ($R_{junction\text{-}board}$) was found to be 27°C/W (board temperature, measured 1″ from device center). In addition, the thermal resistance from junction-to-heatsink lead was found to approximate 10°C/W. Devoting additional PC board metal around the heatsinking pins improved R_{pkg} from 30° to 28°C/W.

The SOP-24 package has Pins 5, 6, 7, 8, 17, 18, 19, and 20 of the package connected directly to the lead frame flag. Characterization was conducted in the same manner as for the DIP package. The junction-to-ambient temperature resistance was found to be 40°C/W with a single output active (34°C/W with all outputs dissipating equal power) and the thermal resistance from junction-to-PC board ($R_{junction\text{-}board}$) to be 30°C/W (board temperature, measured 1″ from device center). The junction-to-heatsink lead resistance was found again to approximate 10°C/W. Devoting additional PC board metal around the heatsinking pins for this package improved the R_{pkg} from 33° to 31°C/W.

The total power dissipation available is dependent on the number of outputs enabled at any one time. At 25°C the $r_{DS(ON)}$ is 450 mΩ with a coefficient of 6500 ppm/°C. For the junction temperature to remain below 150°C, the maximum available power dissipation must decrease as the ambient temperature increases. Figures 21 and 22 depict the per output limit of current at ambient temperatures necessary for the plastic DIP and SOP packages respectively when one, four, or eight outputs are enabled ON. Figure 23 depicts how the $r_{DS(ON)}$ output value is affected by junction temperature.

Figure 20. Thermal Model (Electrical Equivalent)



Package	R_{dx} (Ω)*	C_{dx} (F)*	R_{pkg} (Ω)*	C_{pkg} (F)*
20 Pin DIP	7.0	0.002	30	0.2
SOP-24L	7.0	0.002	33	0.15

* Ω = °C/W, F = W s/°C, I_{PWR} = W, and V_A = °C

Figure 21. Maximum DIP Package Steady State Output Current versus Ambient Temperature

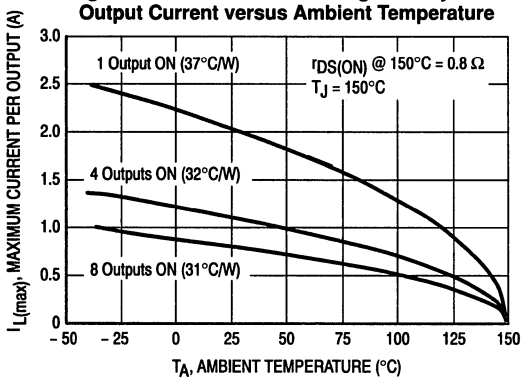


Figure 22. Maximum SOP Package Steady State Ouput Current versus Ambient Temperature

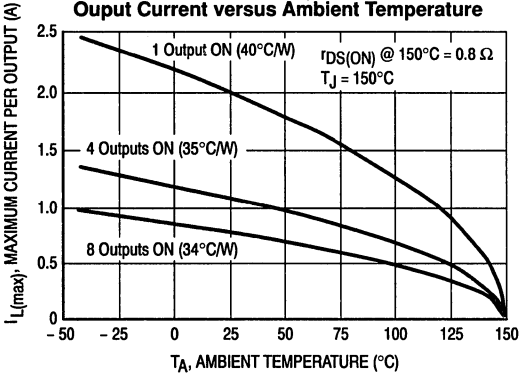
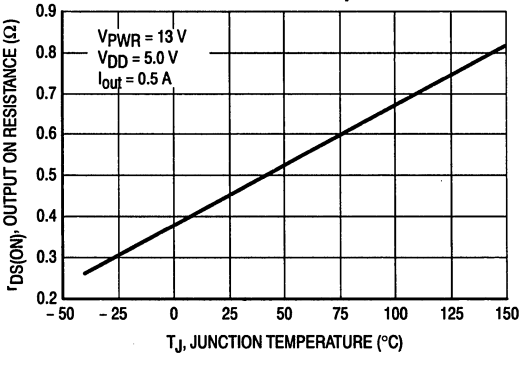


Figure 23. Maximum Output ON Resistance versus Junction Temperature



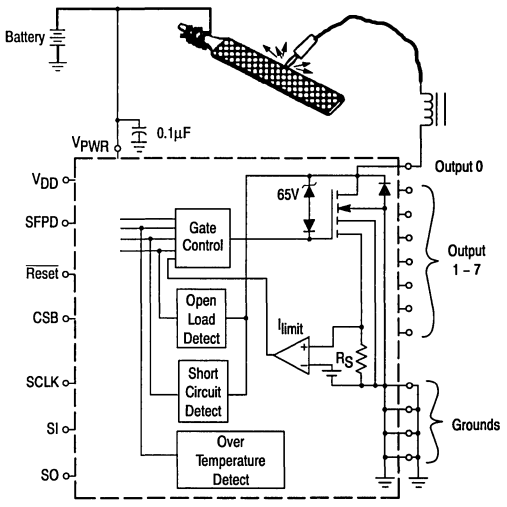
Latch-Up Immunity

Device latch-up caused by substrate injection has been characterized. Latch-up immunity has both a DC and a transient immunity component. DC latch-up immunity results indicate the device to be capable of withstanding in excess of four amps of reverse current out of any of the output transistors while the control logic continues to function normally. The logic control current (I_{DD}) was found to increase by only 0.6 mA with four amps of current being pulled out of an output. Additionally, the I_{PWR} current was found to increase by only 0.15 mA under the same condition. These increases are a result of minority carriers being injected into substrate and subsequently being collected.

The following procedure has been developed to test for transient latch-up immunity and has been applied to this automotive circuit design. Results of transient testing indicate the device to operate properly at output currents greater than 1.5 A. The procedure tests for the device's immunity to intermittent load to battery current connection with the device controlling an inductive load. Appropriately termed "the file test," the battery is connected to a shop file while the lead to the inductive load is dragged across the files surface causing intermittent load opens producing lots of arcs, sparks, and smoke, plus severe transients (see Figure 24). It is during these severe transients that latch-up most likely could occur. The battery voltage used for this test was 18 V and the inductive load was 2.0 mH. These values were found to produce severe transient stresses of the device outputs. All outputs must maintain operation and input control during transient generation to pass "the file test."

The device's input control currents were found to remain stable and were not affected by DC or transient latch-up immunity testing.

Figure 24. Transient Latch-Up Immunity File Test



APPLICATIONS INFORMATION

SIOP Communication

Two common communication protocols used in Motorola's microprocessors are the Serial Peripheral Interface (SPI) and Synchronous Input Output Port (SIOP). SIOP is a subset of the more flexible SPI and the simpler of the two protocols. SIOP is used on many of the MC68HC05 family of microcontrollers. Restrictions of the SIOP protocol include: 1) the SCLK frequency is fixed at one-fourth the internal clock rate and 2) the polarity of the SCLK signal is fixed.

By way of example, the MC68HC05P9 utilizes SIOP protocol and is not directly compatible with the serial input requirements of the MC33298. Specifically, the MC33298 accepts data on the falling edge of SCLK whereas its rising edge triggers data transfer in the SIOP protocol. SCLK is high during SIOP transmissions, which is the opposite of what the MC33298 requires.

Though designed specifically for SPI communication protocol, the MC33298 can easily be adapted to communicate with SIOP protocol through the use of software. The amount of code required to implement SPI in software is relatively small, so the only major drawback is a slower transfer of data. The software routine shown in Table 1 completes a transfer in about 100 µs.

Cost

The bottom line relates to cost. The MC33298 is a very cost effective octal output serial switch for applications typically encountered in the automotive and industrial market segments. To accomplish only the most basic serial switch function the MC33298 offers, using a discrete semiconductor approach, would require the use of at least eight logic level power MOSFETs for the outputs and two shift registers for the I/O plus other miscellaneous "glue" components. Additional circuitry would have to be incorporated to accomplish the protection features offered by the MC33298. Other noteworthy advantages the MC33298 offers are conservation of power and board space, requirement of fewer application components, and enhanced application reliability. The MC33298 is available at a fraction of the cost required for discrete component implementation and represents true value.

The MC33298 represents a cost effective device having advanced performance and features and worthy of consideration.

Table 1. Program to Exercise the MC33298 Using SPI (Having Only SIOP) Protocol

SET LABELS FOR OUTPUT REGISTERS

PORTA	EQU	$0000	;SPI Port ;DO (Data Out), SCLK, CS, RESET, X, FLTOUT, DI (Data In)
PORTB	EQU	$0001	;Normally the SIOP Port. SIOP will be disabled
PORTC	EQU	$0002	;A-D Converter Port
PORTD	EQU	$0003	;Timer Capture Port
DDRA	EQU	$0004	;Data Direction Register for SPI Port
DDRB	EQU	$0005	;Data Direction Register for SCLK, SDI, SDO, 11111
DDRC	EQU	$0006	;Data Direction Register for A-D Converter Port
DDRD	EQU	$0007	;Data Direction Register for PORTD, Timer Capture

DTOUT	EQU	$0080	;Register for the SPI output data. This register will be used for a Serial-to-Parallel transformation.
DATAIN	EQU	$0081	;Input Register for SPI. Also used for a Serial-to-Parallel transformation.
VALUE	EQU	$0082	;Register to store the SPI. Also used for a Serial-to-Parallel transformation.
DATA1	EQU	$0083	;Miscellaneous data register

SCR	EQU	$000A	;Label for SIOP control register, 0 SPE 0 MSTR 0 0 0 0.
SSR	EQU	$000B	;Label for SIOP status register, SPIF DCOL 0 0 0 0 0 0, Read Only Register.
SDR	EQU	$000C	;Label for SIOP data register.

	ORG	$0100	;Program starts at first byte of User ROM.
INIT	RSP		;Reset Stack Pointer to $FF.

INITIALIZE THE DATA REGISTERS AND THEIR DATA DIRECTION BIT REGISTERS

	LDA	#$FE	;Configuration PortA as the SPI Port.
	STA	DDRA	;All but Bit 0 will be outputs.

	LDA	#$FF	
	STA	DDRB	;Configure Register B as an output. SIOP is not used for the MC33298, but is available for another peripheral.
	STA	DDRC	;Configure Register C as an output
	STA	DDRD	;Configure Register D as an output

	LDA	#%00010000	;Initialize the SIOP Control Register.
	STA	SCR	;Disable SIOP by clearing Bit 6.

SELECT THE DESIRED OUTPUTS

TOP	LDA STA	#$55 VALUE	Select outputs of MC33298 to be turned ON. This instruction is left inside the loop to include changes while running the program. A set bit will cause the associated MC33298 output to be OFF. The value register is uncorrupted by the serial-to-parallel conversion.
	BSET	4,PORTA	;Reset the MC33298.
	BCLR	4,PORTA	;Also establishes a + or – trigger source
	BSET	4,PORTA	;The MC33298 is reset with a logic low.

	BCLR	5,PORTA	;Enable MC33298 by pulling CSB (chip select bar) low. Within the MC33298 the Fault Status is transferred to the MC33298 Serial Register at a falling edge of CSB.

	LDA	VALUE	;Select outputs to be turned ON.
	STA	DTOUT	;Save Output Word (Value) to check for fault.

SPI TRANSFER LOOP

	LDX	#$07	;Set the number of Read/Shift cycles.

LOOP	ASL	DATAIN	;Shift a Zero into LSB of DATAIN and ASL other bits.
	ASL	DTOUT	;Test value currently in MSB of DTOUT.
	BCS	DOONE	;
	BCLR	7,PORTA	;MSB was Zero, so clear DATA OUT bit.
	JMP	GOON	
DOONE	BSET	7,PORTA	;MSB was One, so set the DATA OUT bit.
GOON	BSET	6,PORTA	;Set the SCLK. Serial Output pin of the MC33298 changes state on the rising edge of the SCLK. Read the next bit coming from the MC33298.

	BRCLR	0,PORTA, WZZER0	;Read the bit and branch if Zero. LSB of DATAIN is already cleared due to the ASL above.
	BSET	0,DATAIN	;Bit was One. Set the next bit in DATAIN.

WZZER0	BCLR	6,PORTA	;Clear SCLK. Falling edge causes the MC33298 to read the next bit from the MCU.
	DECX		
	BPL	LOOP	;Continue to loop eight times until the SPI transfer is complete.

	BSET	5,PORTA	;Transfer control signal to output transistors.

ESTABLISH A BRIEF DELAY

	LDA	#16	
PAUSE	DECA		;3 Clock cycles
	BNE	PAUSE	;3 Clock cycles
	BCLR	5,PORTA	;Transfer output status to Serial Register.
	JSR	FLTCHK	;Jump to Fault Check subroutine.

	JSR	DLY	;Delay 1/T msec

	BSET	5,PORTA	;Deselect the MC33298.
	BRA	TOP	;Return to top of loop.

SUBROUTINE TO CHECK FOR FAULTS

FLTCHK	BCLR	1,PORTA	;CLR the Fault pin.
	LDA	DATAIN	
	CMP	VALUE	;Check for Faults.
	BEQ	NOFLT	;If there is no Fault, continue.
	BSET	1,PORTA	;Activate Fault LED.
NOFLT	RTS		

DELAY SUBROUTINE

DLY	STA	DATA1	;Save Accumulator in RAM.
	LDA	#$04	;Do outer loop 4 times, roughly 4.0 ms.
OUTLP	CLRX		;X used as Inner Loop Count
INNRLP	DECX		;0-FF, FF-FE, ... 1-0 256 loops.
	BNE	INNRLP	;6CYC* 256* 1.0 µs/CYC = 1.53 ms
	DECA		;4-3. 3-2, 2-1, 1-0
	BNE	OUTLP	;1545CYC* 4*1.0 µs/CYC = 6.18 ms
	LDA	DATA1	;Recover Accumulator value.
	RTS		;Return from subroutine.

	ORG	$1FF	
	FDB	INIT	

MCCF79076

Product Preview

Ignition Control Flip-Chip

The MCCF79076, in conjunction with an appropriate Motorola Power Darlington Transistor, provides an economical solution for automotive ignition applications. The MCCF79076 offers optimum performance by providing closed loop operation of the Power Darlington in controlling the ignition coil current.

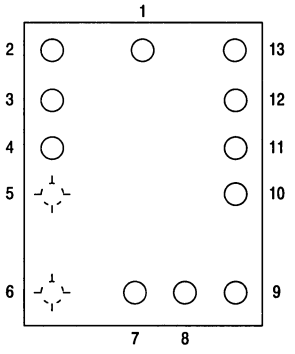
The MCCF79076 incorporates Flip-Chip Technology which involves the formation of solder bumps, rather than traditional wire bonds, to establish mechanical and electrical contact to the semiconductor chip. This process affords a unique device having improved reliability at elevated operating temperatures.

- Solder Bumped for Flip-Chip Assembly
- Ignition Coil Voltage Internally Limited to 375 V
- Coil Current Limiting to 7.5 A
- Output On-Time (Dwell) Control
- Dwell Feedback Control to Sense Coil Variation
- Hall Sensor Input
- $-30°C \le T_A \le +140°C$ Ambient Operating Temperature

IGNITION CONTROL FLIP-CHIP

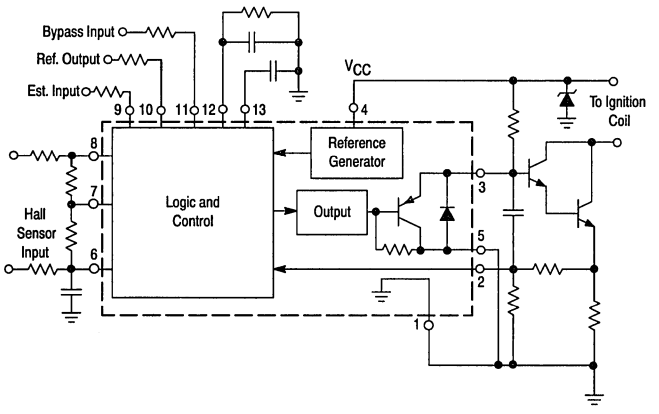
SILICON MONOLITHIC INTEGRATED CIRCUIT

FLIP-CHIP CONFIGURATION



Top View
(Bump Side)

Simplified Block Diagram and Application Circuit



BUMP CONNECTIONS

1. High Ground
2. Output Current Limit
3. Dwell Output
4. Supply
5. Low Ground
6. Reference Dwell Input
7. Advance Input
8. Bias Voltage
9. Est Input
10. Reference Output
11. Bypass Input
12. 900 RPM Detector
13. Dwell Control

ORDERING INFORMATION

Device	Temperature Range	Package
MCCF79076	– 30° to +125°C	Flip-Chip

10

TCF6000

Peripheral Clamping Array

The TCF6000 was designed to protect input/output lines of microprocessor systems against voltage transients.

- Optimized for HMOS System
- Minimal Component Count
- Low Board Space Requirement
- No P.C.B. Track Crossovers Required
- Applications Areas Include Automotive, Industrial, Telecommunications and Consumer Goods

PERIPHERAL CLAMPING ARRAY

SILICON MONOLITHIC INTEGERATED CIRCUIT

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO-8)

PIN CONNECTIONS

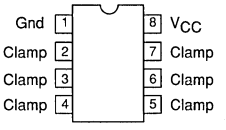
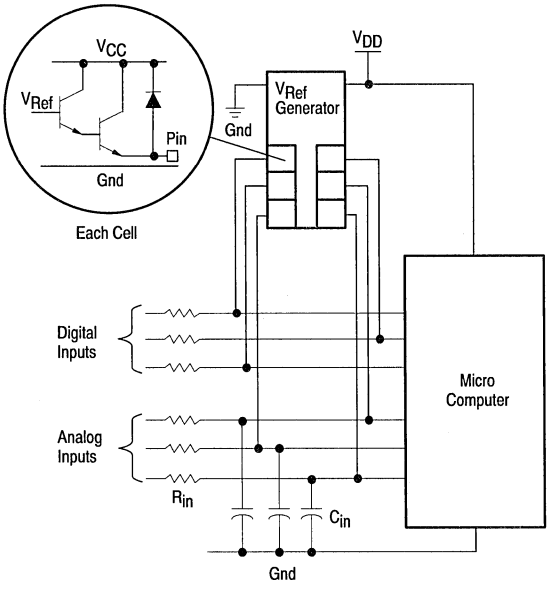


Figure 1. Block Diagram and Typical Aplication



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MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted, Note 1.)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	6.0	V
Supply Current	I_i	300	mA
Clamping Current	I_{IK}	±50	mA
Junction Temperature	T_J	150	°C
Power Dissipation (T_A = + 85°C)	P_D	400	m/W
Thermal Resistance (Junction-Ambient)	θ_{JA}	100	°C/W
Operating Ambient Temperature Range	T_A	–40 to +85	°C
Storage Temperature Range	T_{stg}	–55 to + 150	°C

Note 1. Values beyond which damage may occur.

ELECTRICAL CHARACTERICISTICS (T_A = 25°C, 4.5 ≤ V_{CC} ≤ 5.5 V; if not otherwise noted.)

Characteristics	Symbol	Min	Max	Unit
Positive Clamping Voltage (Note 2) (I_{IK} = 10 mA, –40°C ≤ T_A ≤ + 85°C)	$V_{(IK)}$	—	V_{CC} + 1.0	V
Positive Peak Clamping Current	$I_{IK(P)}$	—	20	mA
Negative Peak Clamping Voltage (I_{IK} = –10 mA, –40°C ≤ T_A ≤ + 85°C)	$V_{(IK)}$	–0.3	—	V
Negative Peak Clamping Current	$I_{IK(P)}$	–20	—	mA
Output Leakage Current (0 V ≤ V_{in} ≤ V_{CC}) (0 V ≤ V_{in} ≤ V_{CC}, –40°C ≤ T_A ≤ + 85°C)	I_L I_{LT}	— —	1.0 5.0	µA
Channel Crosstalk (A_{CT} = 20 log I_L/I_{IK})	A_{CT}	100	—	dB
Quiescent Current (Package)	I_B	—	2.0	mA

Note 2. The device might not give 100% protection in CMOS applications

CIRCUIT DESCRIPTION

To ensure the reliable operation of any integrated circuit based electronics system, care has been taken that voltage transients do not reach the device I/O pins. Most NMOS, HMOS and Bipolar integrated circuits are particularly sensitive to negative voltage peaks which can provoke latch-up or otherwise disturb the normal functioning of the circuit, and in extreme cases may destroy the device.

Generally the maximum rating for a negative voltage transients on integral circuits is –0.3 V over the whole temperature range. Classical protection units have consisted of diode/resistor networks as shown in Figures 2a and 2b.

The arrangement in Figure 2a does not, in general, meet the specification and is therefore inadequate.

The problem with the solution shown if Figure 2b lies mainly with the high current drain through the biassing devices R_1 and D_3. A second problem exists if the input line carries an analog signal. When V_{in} is close to the ground potential, currents arising from leakage and mismatch between D_3 and D_2 can be sourced into the input line, thus disturbing the reading.

Figure 2. Classical Protection Circuits

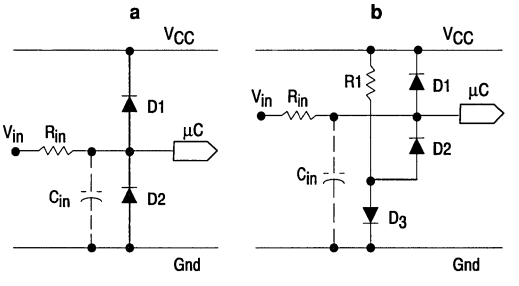
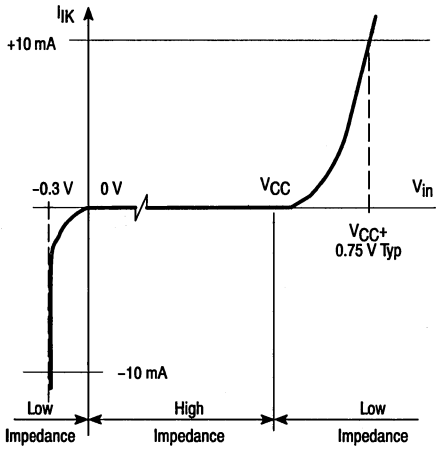


Figure 3 shows the clamping characteristics which are common to each of the six cells in the Peripheral Clamping Array.

As with the classical protection circuits, positive voltage transients are clamped by means of a fast diode to the V_{CC} supply line.

Figure 3. Clamping Characteristics



APPLICATIONS INFORMATION

Figure 4 depicts a typical application in a microcomputer based automotive ignition system.

The TCF6000 is being used not only to protect the system's normal inputs but also the (bidirectional) serial diagnostics port.

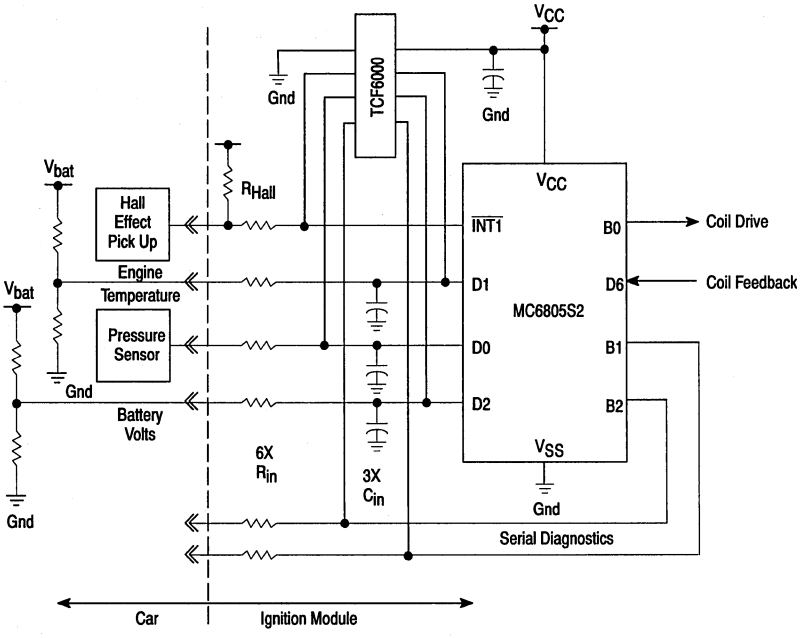
The value of the input resistors, R_{in}, is determined by the clamping current and the anticipated value of the spikes. Thus:

$$R_{in} = \frac{V}{I_{IK}}\ \Omega$$

where: V = Peak Volts (V)
I_{IK} = Clamping current (A)
So, taking, V = 300 V typically (SAE J1211)
I_{IK} = 10 mA (recommended)
gives, R_{in} = 30 k

Resistors of this value will not usually cause any problems in MOS systems, but their presence needs to be taken into account by the designer. Their effect will normally need to be compensated for Bipolar systems.

Figure 4. Typical Automotive Application



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The use of C_{in} is not mandatory, and is not recommended where the lines to be protected are used for output or for both input and output. For digital input lines, the use of a small capacitor in the range of 50 pF to 220 pF is recommended as this will reduce the rate of rise of voltage seen by the TCF6000 and hence the possibility of overshoot.

In the case of the analog inputs, such as that from the pressure sensor, the capacitor C_{in} is necessary for devices, such as the MC6805S2 shown, which present a low impedance during the sampling period. The maximum value for C_{in} is determined by the accuracy required, the time taken to sample the input and the input impedance during that time, while the maximum value is determined by the required frequency response and the value of R_{in}.

Thus for a resistive input A/D connector where:

T_S = Sample time (Seconds)

R_D = Device input resistance (Ω)

V_{in} = Input voltage (V)

k = Required accuracy (%)

Q_1 = Charge on capacitor before sampling

Q_2 = Charge on capacitor after sampling

I_D = Device input current (A)

Thus:

$$Q_1 - Q_2 = \frac{k.Q_1}{100}$$

but, $Q_1 = C_{in}\, V_{in}$

and, $Q_1 - Q_2 = I_D \bullet T_S$

so that, $$I_D\, T_S = \frac{k \bullet C_{in} - V_{in}}{100}$$

and, $$C_{in}\,(min) = \frac{I_D \bullet T_S}{V_{in} \bullet k} \text{ Farad}$$

so, $$C_{in}\,(min) = \frac{100 \bullet T_S}{k \bullet R_D} \text{ Farad}$$

The calculation for a sample and hold type converter is even simpler:

k = Required accuracy (%)

C_H = Hold capacitor (Farad)

$$C_{in}\,(min) = \frac{100 \bullet C_H}{k} \text{ Farad}$$

For the MC6805S2 this comes out at:

$$C_{in}\,(min) = \frac{100.25\ pF}{0.25} = 10\ nF \text{ for } 1/4\% \text{ accuracy}$$

10

UAA1041

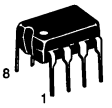
Automotive Direction Indicator

This device was designed for use in conjunction with a relay in automotive applications. It is also applicable for other warning lamps such as "handbrake ON," etc.

- Defective Lamp Detection
- Overvoltage Protection
- Short Circuit Detection and Relay Shutdown to Prevent Risk of Fire
- Reverse Battey Connection Protection
- Integrated Suppression Clamp Diode

AUTOMOTIVE DIRECTION INDICATOR

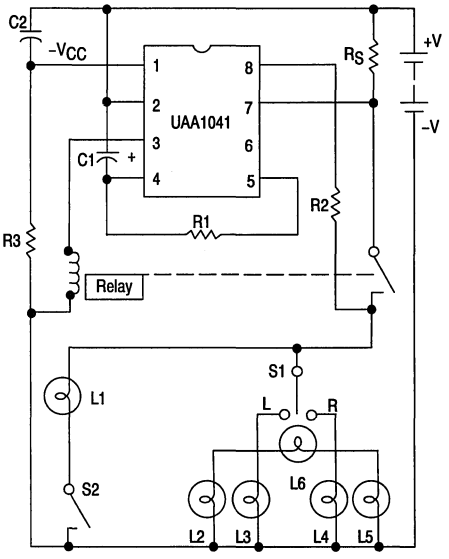
SILICON MONOLITHIC INTEGRATED CIRCUIT



P SUFFIX
PLASTIC PACKAGE
CASE 626

D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO-8)

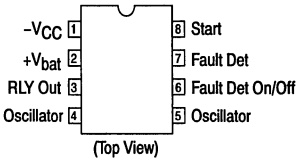
Figure 1. Typical Automotive System



L1: 1.2 W, warning light handbrake ON
L2, L3, L4, L5: 21 W, turn signals

R1 = 75 k
R2 = 3.3 k
R3 = 220 Ω
RS = 30 mΩ
C1 = 5.6 µF
C2 = 0.047 µF

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Ambient Temperature Range	Package
UAA1041D	–40° to + 100°C	SO–8
UAA1041P		Plastic DIP

10

MAXIMUM RATINGS

Rating	Pin	Value	Unit
Current: Continuous/Pulse*	1 2 3 8	+150/+500 –35/–500 +/–350/1900 +/–300/1400 +/–25/50	mA
Junction Temperature	T_J	150	°C
Operating Ambient Temperature Range	T_A	–40 to + 100	°C
Storage Temperature Range	T_{stg}	–65 to + 150	°C

* One pulse with an exponential decay and with a time constant of 500 ms.

ELECTRICAL CHARACTERICISTICS (T_1 = 25°C)

Characteristics		Symbol	Min	Typ	Max	Unit
Battery Voltage Range (normal operation)		V_B	8.0	—	18	V
Overvoltage Detector Threshold	(V_{Pin2}–V_{Pin1})	$D_{th(OV)}$	19	20.2	21.5	V
Clamping Voltage	(V_{Pin2}–V_{Pin1})	V_{IK}	29	31.5	34	V
Short Circuit Detector Threshold	(V_{Pin2}–V_{Pin7})	$D_{th(SC)}$	0.63	0.7	0.77	V
Output Voltage (I_{relay} = –250 mA)	(V_{Pin2}–V_{Pin3})	V_O	—	—	1.5	V
Starter Resistance $R_{st} = R_2 + R_{Lamp}$		R_{st}	—	—	3.6	kΩ†
Oscillator Constant (normal operation)		Kn	1.4	1.5	1.6	—
Temperature Coefficient of Kn		Kn	—	-1.5×10^{-3}	—	1/°C
Duty Cycle (normal operation)		—	45	50	55	%
Oscillator Constant — (1 lamp defect of 21 W)		K_F	0.63	0.68	0.73	—
Duty Cycle (1 lamp defect of 21 W)		—	35	40	45	%
Oscillator Constant		K1 K2 K3	0.167 0.25 0.126	0.18 0.27 0.13	0.193 0.29 0.14	—
Current Consumption (relay off) Pin 1; at $V_{Pin2} - V_{Pin1}$ = 8.0 V = 13.5 V = 18 V		I_{CC}	 — –2.5 —	 –0.9 –1.6 –2.2	 — –1.0 —	mA
Current Consumption (relay on) Pin 1; at $V_{Pin2} - V_{Pin1}$ = 8.0 V = 13.5 V = 18 V		—	 — — —	 –3.8 –5.6 –6.9	 — — —	mA
Defect Lamp Detector Threshold at V_{Pin2} to V_B = 8.0 V and R_3 = 220 Ω = 13.5 V = 18 V		V_{Pin2}–V_{Pin7} V_{Pin2}–V_{Pin7} V_{Pin2}–V_{Pin7}	— 79 —	68 85.3 100	— 91 —	mV

† See Note 1 of Application Information

10

CIRCUIT DESCRIPTION

The circuit is designed to drive the direction indicator flasher relay. Figure 2 shows the typical system configuration with the external components. It consists of a network (R1, C1) to determine the oscillator frequency, shunt resistor (R_S) to detect defective bulbs and short circuits in the system, and two current limiting resistors (R_2/R_3) to protect the IC against load dump transients. The circuit can be used either with or without short circuit detection, and features overvoltage, defective lamp and short circuit detection.

The lightbulbs L2, L3, L4, L5 are the turn signal indicators with the dashboard-light L6. When switch S1 is closed, after a time delay of t_1 (in our example t_1 = 75 ms), the relay will be actuated. The corresponding lightbulbs (L2, L3 or L4, L5) will flash at the oscillator frequency, independent of the battery voltage of 8.0 V to 18 V. The flashing cycle stops and the circuit is reset to the initial position when switch S1 is open.

Overvoltage Detection

Senses the battery voltage. When this voltage exceeds 20.2 V (this is the case when two batteries are connected in series), the relay will be turned off to protect the lightbulbs

Lightbulb Defect Detector

Senses the current through the shunt resistor R_S. When one of the lightbulbs is defective, the failure is indicated by doubling the flashing frequency.

Short Circuit Detector

Detects excessive current (I_{sh} > 25 A) flowing in the shunt resistor R_S. The detection takes place after a time delay of t_3 (t_3 = 55 ms). In this case, the relay will be turned off. The circuit is reset by switching S1 to the off position.

10

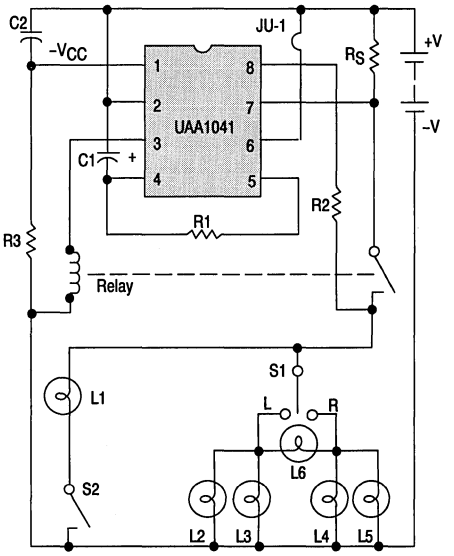
Operation with Short Circuit Detection

Pin 6 has to be left open and a capacitor C_2 has to be connected between Pin 1 and Pin 2.

Operation without Short Circuit Detection

Pin 6 has to be connected to Pin 2, and the use of capacitor C_2 is not necessary. The circuit can also be used for other warning flashers. In this example, when the handbrake is engaged, it is signaled by the light (L1).

Figure 2. Typical System Configuration



PARTS LIST

R1 = 75 kΩ	Relay-Coil Resistance
R2 = 3.3 kΩ	Range 60 Ω to 800 Ω
R3 = 220 Ω	
R_S = 30 mΩ	Note: Per text connect
Wire Resistor	jumper JU-1 bypass
C1 = 5.6 µF	short circuit detector
C2 = 0.047 µF	C2 may be deleted also.

APPLICATION INFORMATION

1. The flashing cycle is started by closing S1. The switch position is sensed across resistor R_2 and R_{Lamp} by Input 8.

   $$R_{st} = R_2 + R_{Lamp}.$$

   The condition for the start is: R_{st} < 3.6 kΩ.
   For correct operation, leakage resistance from Pin 8 to ground must be greater than 5.6 kΩ.

2. Flashing frequency: $f_n = \frac{1}{R_1 C_1 K_n}$

3. Flashing frequency in the case of one defective lightbulb of 21 W:

   $$f_F = \frac{1}{R_1 C_1 K_F} \quad K_n = 2{,}2K_F$$

4. t_1: delay at the moment when S1 is closed and first flash $t_1 = K_1 R_1 C$
5. t_2: defective lightbulb detection delay $t_2 = K_2 R_1 C_1$
6. t_3: short circuit detection delay $t_3 = K_1 R_1 C_1$
   In the case of short circuit — it is assumed that the voltage (V_{Pin2}–V_{Pin1}) ≥ 8.0 V. The relay will be turned off after delay t_3. The circuit is reset by switching S1 to the off position.
7. The capacitor C2 is not obligatory when the short circuit detector is not used. In this case Pin 6 has to be connected to Pin 2.
8. When overvoltage is sensed ($V_{Pin2} - V_{Pin1}$) the relay is turned off to protect the relay and the lightbulbs against excessive currents.

Other Linear Circuits

In Brief . . .

A variety of other analog circuits are provided for special applications with both bipolar and CMOS technologies. These circuits range from the industry standard analog timing circuits and multipliers to specialized CMOS smoke detectors. These products provide key functions in a wide range of applications, including data transmission, commercial smoke detectors, and various industrial controls.

Timing Circuits

These highly stable timers are capable of producing accurate time delays or oscillation. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For a stable operation as an oscillator, the free-running frequency and the duty cycle are both accurately controlled with two external resistors and one capacitor. The output structure can source or sink up to 200 mA or drive TTL circuits. Timing intervals from microseconds through hours can be obtained. Additional terminals are provided for triggering or resetting if desired.

Singles

MC1455P1,U,D T_A = 0° to +70°C, Case 626, 693, 751

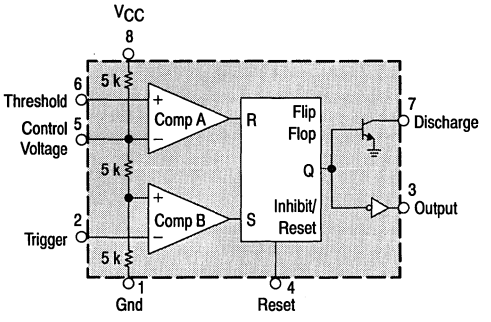
MC1455BP1 T_A = −40° to +85°C, Case 626

Duals

MC3456L,P T_A = 0° to +70°C, Case 632, 646

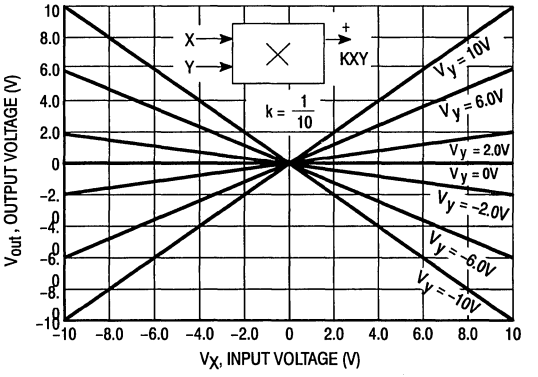
NE556A,N T_A = 0° to +70°C, Case 646

NE556D T_A = 0° to +70°C, Case 751



Multipliers

Multipliers are designed for use where the output voltage is a linear product of two input voltages. Typical applications include: multiply, divide, square, root-mean-square, phase detector, frequency doubler, balanced modulator/demodulator, electronic gain control.



Linear Four-Quadrant Multipliers

MC1594L T_A = −55° to +125°C, Case 620

MC1494L T_A = 0° to +70°C, Case 620

The MC1594/MC1494 is a variable transconductance multiplier with internal level-shift circuitry and voltage regulator. Scale factor, input offsets and output offset are completely adjustable with the use of four external potentiometers. Two complementary regulated voltages are provided to simplify offset adjustment and improve power supply rejection.

MC1595L T_A = −55° to +125° C, Case 632

MC1495L T_A = 0° to +70° C, Case 632

These devices are designed for uses where the output is a linear product of two input voltages. Maximum versatility is assured by allowing the user to select the level shift method. Typical applications include: multiply, divide(1), square root(1), mean square(1), phase detector, frequency doubler, balanced modulator/demodulator, and electronic gain control.

(1)When used with an operational amplifier.

11

Smoke Detectors (CMOS)

These smoke detector ICs require a minimum number of external components. When smoke is sensed, or a low battery voltage is detected, an alarm is sounded via an external piezoelectric transducer. All devices are designed to comply with UL specifications.

Smoke Detectors (CMOS)

Function	Recommended Power Source	Unique Feature	Low Battery Detector	Piezoelectric Horn Driver	Complies with UL217 and UL268	Device Number	Suffix/ Case
Ionization-Type Smoke Detector	Battery	High Input Impedance FET Comparator	✓	✓	✓	MC14467-1	P1/626
	Line		—	—	✓	MC14578	P/648
Ionization-Type Smoke Detector with Interconnect	Battery		✓	✓	✓	MC14468	
	Line		—	✓	✓	MC14470	
Photoelectric-Type Smoke Detector with Interconnect	Battery	Photo Amplifier	✓	✓	✓	MC145010	P/648 DW/751G
			✓	✓	✓		
	Line		(1)	✓	✓	MC145011	

(1)Low-supply detector

OTHER LINEAR CIRCUITS

Timing Circuits

Multipliers

RELATED APPLICATION NOTES

Application Note	Title	Related Device
AN489	Analysis and Basic Operation of the MC1595 (Out of Print)	**MC1595**
AN531	MC1596 Balanced Modulator	**MC1596**

MC1455

TIMING CIRCUIT

SILICON MONOLITHIC INTEGRATED CIRCUIT

P1 SUFFIX
PLASTIC PACKAGE
CASE 626

U SUFFIX
CERAMIC PACKAGE
CASE 693

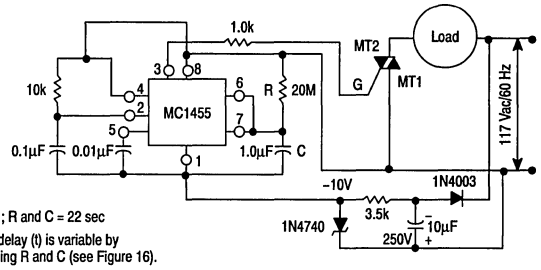
D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO-8)

Timing Circuit

The MC1455 monolithic timing circuit is a highly stable controller capable of producing accurate time delays or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode, time is precisely controlled by one external resistor and capacitor. For astable operation as an oscillator, the free-running frequency and the duty cycle are both accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output structure can source or sink up to 200 mA or drive MTTL circuits.

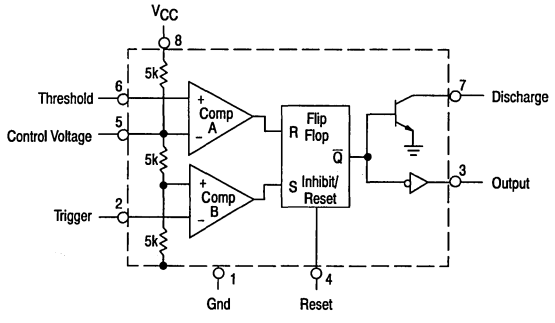
- Direct Replacement for NE555 Timers
- Timing from Microseconds through Hours
- Operates in Both Astable and Monostable Modes
- Adjustable Duty Cycle
- High Current Output Can Source or Sink 200 mA
- Output Can Drive MTTL
- Temperature Stability of 0.005% per °C
- Normally ON or Normally OFF Output

Figure 1. 22 Second Solid State Time Delay Relay Circuit



t = 1.1; R and C = 22 sec
Time delay (t) is variable by changing R and C (see Figure 16).

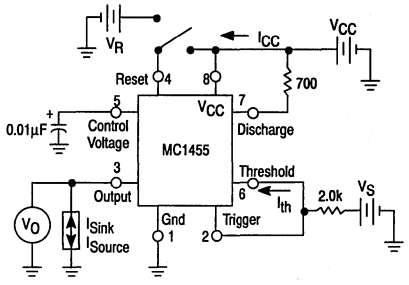
Figure 2. Block Diagram



ORDERING INFORMATION

Device	Temperature Range	Package
MC1455P1	0° to +70°C	Plastic DIP
MC1455D		SO-8
MC1455U		Ceramic DIP
MC1455BD	–40° to +85°C	SO-8
MC1455BP1		Plastic DIP

Figure 3. General Test Circuit



Test circuit for measuring DC parameters (to set output and measure parameters):
a) When $V_S \geq 2/3\ V_{CC}$, V_O is low.
b) When $V_S \leq 1/3\ V_{CC}$, V_O is high.
c) When V_O is low, Pin 7 sinks current. To test for Reset, set V_O, high, apply Reset voltage, and test for current flowing into Pin 7. When Reset is not in use, it should be tied to V_{CC}.

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MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+18	Vdc
Discharge Current (Pin 7)	I_7	200	mA
Power Dissipation (Package Limitation) U Suffix, Ceramic Package Derate above T_A = +25°C P1 Suffix, Plastic Package Derate above T_A = +25°C D Suffix, Plastic Package Derate above T_A = +25°C	 P_D P_D P_D 	 1000 6.6 625 5.0 625 160	 mW mW/°C mW mW/°C mW °C/W
Operating Temperature Range (Ambient) MC1455B MC1455	T_A	 –40 to +85 0 to +70	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = +25°C, V_{CC} = +5.0 V to +15 V, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Operating Supply Voltage Range	V_{CC}	4.5	—	16	V
Supply Current V_{CC} = 5.0 V, R_L = ∞ V_{CC} = 15 V, R_L = ∞, Low State (Note 1)	I_{CC}	 — —	 3.0 10	 6.0 15	mA
Timing Error (R = 1.0 kΩ to 100 kΩ) (Note 2) Initial Accuracy C = 0.1 µF Drift with Temperature Drift with Supply Voltage		 — — —	 1.0 50 0.1	 — — —	 % PPM/°C %/V
Threshold Voltage/Supply Voltage	V_{th}/V_{CC}	—	2/3	—	
Trigger Voltage V_{CC} = 15 V V_{CC} = 5.0 V	V_T	 — —	 5.0 1.67	 — —	V
Trigger Current	I_T	—	0.5	—	µA
Reset Voltage	V_R	0.4	0.7	1.0	V
Reset Current	I_R	—	0.1	—	mA
Threshold Current (Note 3)	I_{th}	—	0.1	0.25	µA
Discharge Leakage Current (Pin 7)	I_{dischg}	—	—	100	nA
Control Voltage Level V_{CC} = 15 V V_{CC} = 5.0 V	V_{CL}	 9.0 2.6	 10 3.33	 11 4.0	V
Output Voltage Low I_{Sink} = 10 mA (V_{CC} = 15 V) I_{Sink} = 50 mA (V_{CC} = 15 V) I_{Sink} = 100 mA (V_{CC} = 15 V) I_{Sink} = 200 mA (V_{CC} = 15 V) I_{Sink} = 8.0 mA (V_{CC} = 5.0 V) I_{Sink} = 5.0 mA (V_{CC} = 5.0 V)	V_{OL}	 — — — — — —	 0.1 0.4 2.0 2.5 — 0.25	 0.25 0.75 2.5 — — 0.35	V
Output Voltage High V_{CC} = 15 V (I_{Source} = 200 mA) V_{CC} = 15 V (I_{Source} = 100 mA) V_{CC} = 5.0 V (I_{Source} = 100 mA)	V_{OH}	 — 12.75 2.75	 12.5 13.3 3.3	 — — —	V
Rise Time Differential Output	t_r	—	100	—	ns
Fall Time Differential Output	t_f	—	100	—	ns

NOTES:
1. Supply current when output is high is typically 1.0 mA less.
2. Tested at V_{CC} = 5.0 V and V_{CC} = 15 V Monostable mode.
3. This will determine the maximum value of $R_A + R_B$ for 15 V operation. The maximum total R = 20 mΩ.

Figure 4. Trigger Pulse Width

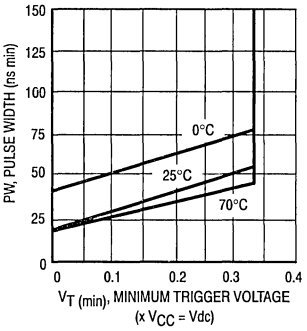

Figure 5. Supply Current

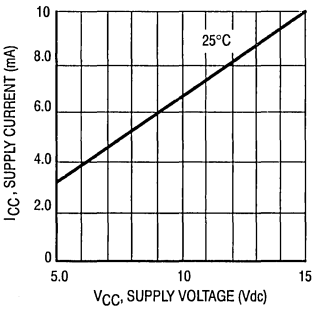

Figure 6. High Output Voltage

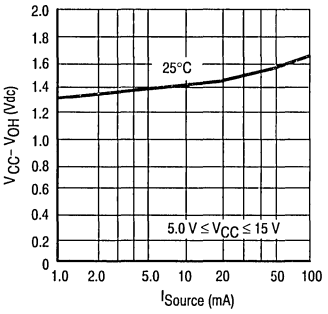

Figure 7. Low Output Voltage @ V_{CC} = 5.0 Vdc

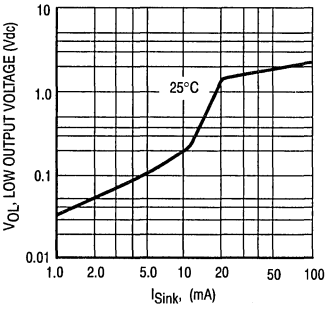

Figure 8. Low Output Voltage @ V_{CC} = 10 Vdc

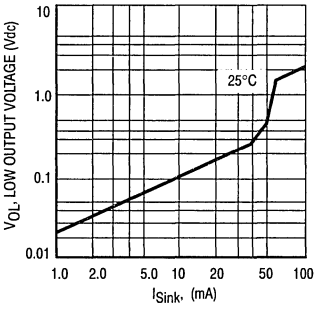

Figure 9. Low Output Voltage @ V_{CC} = 15 Vdc

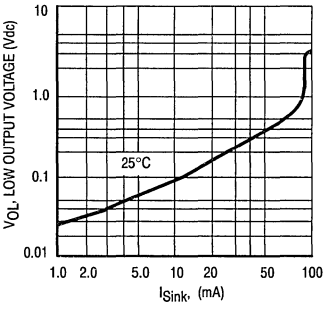

Figure 10. Delay Time versus Supply Voltage

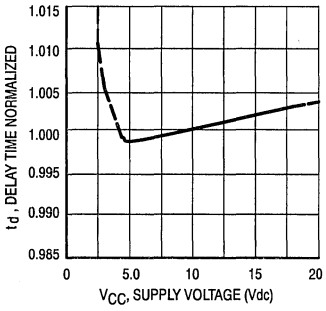

Figure 11. Delay Time versus Temperature

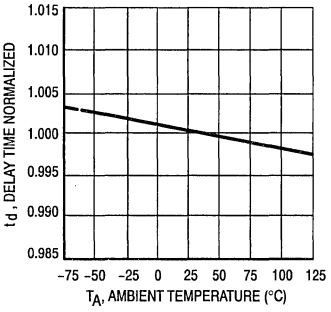

Figure 12. Propagation Delay versus Trigger Voltage

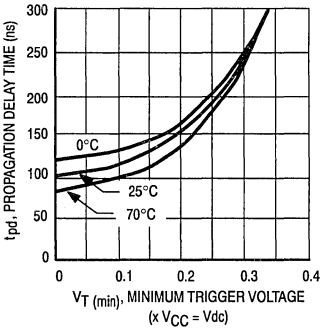

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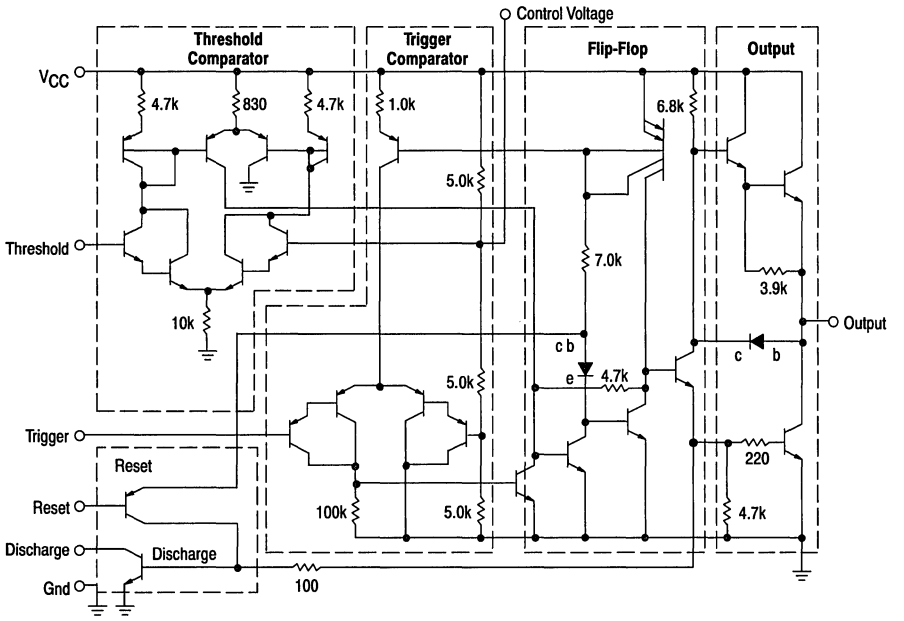
Figure 13. Representative Circuit Schematic



GENERAL OPERATION

The MC1455 is a monolithic timing circuit which uses as its timing elements an external resistor — capacitor network. It can be used in both the monostable (one-shot) and astable modes with frequency and duty cycle controlled by the capacitor and resistor values. While the timing is dependent upon the external passive components, the monolithic circuit provides the starting circuit, voltage comparison and other functions needed for a complete timing circuit. Internal to the integrated circuit are two comparators, one for the input signal and the other for capacitor voltage; also a flip-flop and digital output are included. The comparator reference voltages are always a fixed ratio of the supply voltage thus providing output timing independent of supply voltage.

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Monostable Mode

In the monostable mode, a capacitor and a single resistor are used for the timing network. Both the threshold terminal and the discharge transistor terminal are connected together in this mode, refer to circuit Figure 14. When the input voltage to the trigger comparator falls below 1/3 V_{CC} the comparator output triggers the flip-flop so that it's output sets low. This turns the capacitor discharge transistor "off" and drives the digital output to the high state. This condition allows the capacitor to charge at an exponential rate which is set by the RC time constant. When the capacitor voltage reaches 2/3 V_{CC} the threshold comparator resets the flip-flop. This action discharges the timing capacitor and returns the digital output to the low state. Once the flip-flop has been triggered by an input signal, it cannot be retriggered until the present timing period has been completed. The time that the output is high is given by the equation $t = 1.1\ R_A\ C$. Various combinations of R and C and their associated times are shown in Figure 16. The trigger pulse width must be less than the timing period.

A reset pin is provided to discharge the capacitor thus interrupting the timing cycle. As long as the reset pin is low, the capacitor discharge transistor is turned "on" and prevents the capacitor from charging. While the reset voltage is applied the digital output will remain the same. The reset pin should be tied to the supply voltage when not in use.

Figure 14. Monostable Circuit

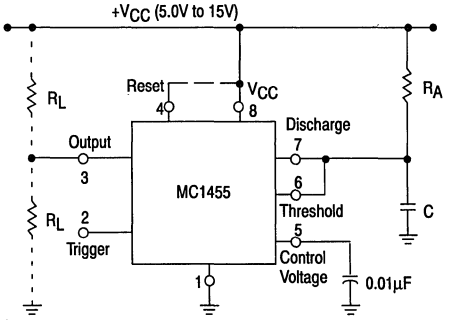
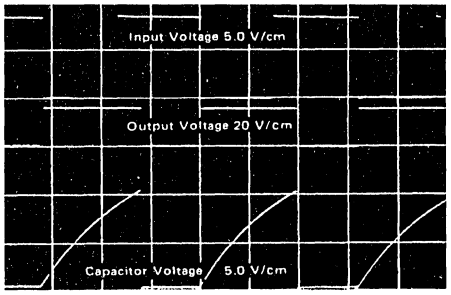


Figure 15. Monostable Waveforms



t = 50 µs/cm
(R_A = 10 kΩ, C = 0.01 µF, R_L = 1.0 kΩ, V_{CC} = 15 V)

Figure 16. Time Delay

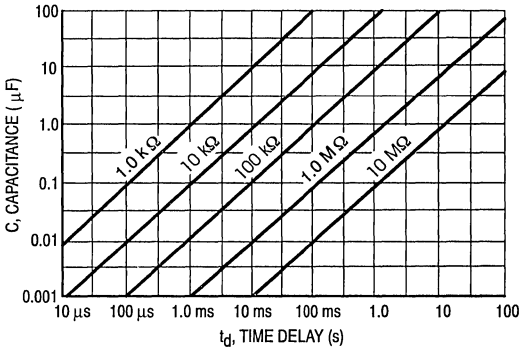


Figure 17. Astable Circuit

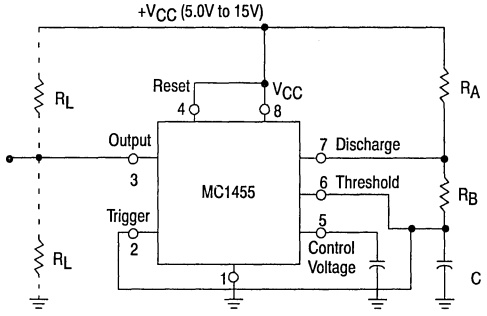
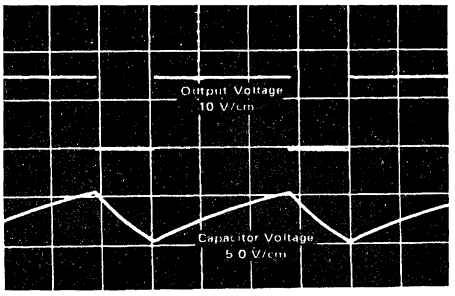


Figure 18. Astable Waveforms



t = 20 µs/cm
(R_A = 5.1 kΩ, C = 0.01 µF, R_L = 1.0 kΩ; R_B = 3.9 kΩ, V_{CC} = 15 V)

Astable Mode

In the astable mode the timer is connected so that it will retrigger itself and cause the capacitor voltage to oscillate between 1/3 V_{CC} and 2/3 V_{CC}. See Figure 17.

The external capacitor changes to 2/3 V_{CC} through R_A and R_B and discharges to 1/3 V_{CC} through R_B. By varying the ratio of these resistors the duty cycle can be varied. The charge and discharge times are independent of the supply voltage.

The charge time (output high) is given by:

$$t_1 = 0.695\ (R_A + R_B)\ C$$

The discharge time (output low) by:

$$t_2 = 0.695\ (R_B)\ C$$

Thus the total period is given by:

$$T = t_1 + t_2 = 0.695\ (R_A + 2R_B)\ C$$

The frequency of oscillation is then: $f = \frac{1}{T} = \frac{1.44}{(R_A + 2R_B)\ C}$

and may be easily found as shown in Figure 19.

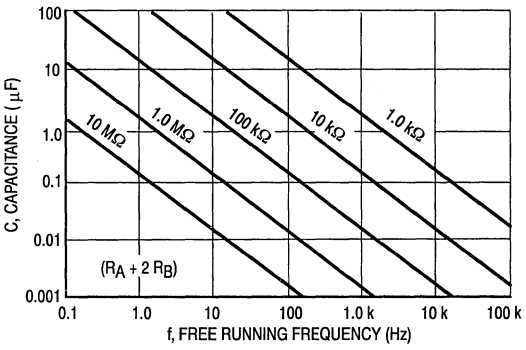
The duty cycle is given by: $DC = \frac{R_B}{R_A + 2R_B}$

To obtain the maximum duty cycle R_A must be as small as possible; but it must also be large enough to limit the discharge current (Pin 7 current) within the maximum rating of the discharge transistor (200 mA).

The minimum value of R_A is given by:

$$R_A \geq \frac{V_{CC}\ (Vdc)}{I_7\ (A)} \geq \frac{V_{CC}\ (Vdc)}{0.2}$$

Figure 19. Free Running Frequency



APPLICATIONS INFORMATION

Linear Voltage Ramp

In the monostable mode, the resistor can be replaced by a constant current source to provide a linear ramp voltage. The capacitor still charges from 0 V_{CC} to 2/3 V_{CC}. The linear ramp time is given by:

$$t = \frac{2}{3} \frac{V_{CC}}{1}, \text{ where } I = \frac{V_{CC} - V_B - V_{BE}}{R_E}$$

If V_B is much larger than V_{BE}, then t can be made independent of V_{CC}.

Missing Pulse Detector

The timer can be used to produce an output when an input pulse fails to occur within the delay of the timer. To accomplish this, set the time delay to be slightly longer than the time between successive input pulses. The timing cycle is then continuously reset by the input pulse train until a change in frequency or a missing pulse allows completion of the timing cycle, causing a change in the output level.

Figure 20. Linear Voltage Sweep Circuit

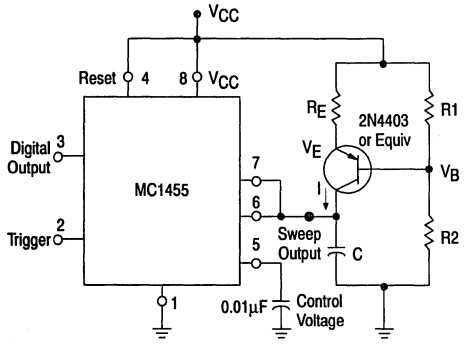
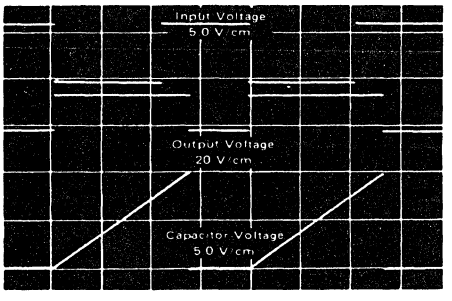


Figure 21. Linear Voltage Ramp Waveforms



t = 100 µs/cm

(R_E = 10 kΩ, R2 = 100 kΩ, R1 = 39 kΩ, C = 0.01 µF, V_{CC} = 15 V)

Figure 22. Missing Pulse Detector

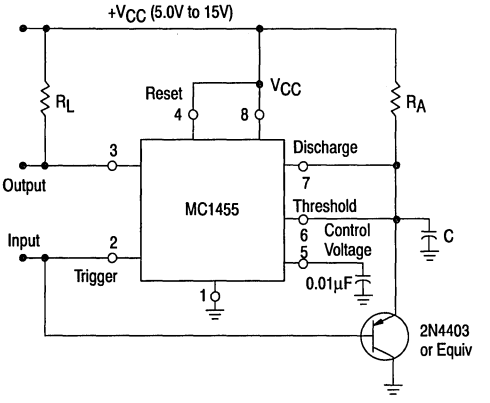
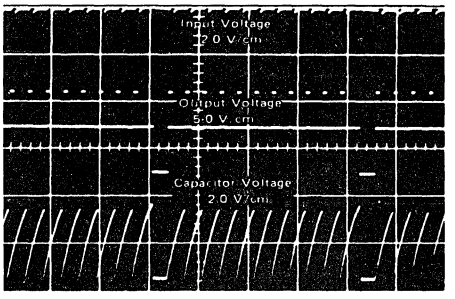


Figure 23. Missing Pulse Detector Waveforms



t = 500 µs/cm

(R_A = 2.0 kΩ, R_L = 1.0 kΩ, C = 0.01 µF, V_{CC} = 15 V)

Pulse Width Modulation

If the timer is triggered with a continuous pulse train in the monstable mode of operation, the charge time of the capacitor can be varied by changing the control voltage at Pin 5. In this manner, the output pulse width can be modulated by applying a modulating signal that controls the threshold voltage.

Figure 24. Pulse Width Modulator

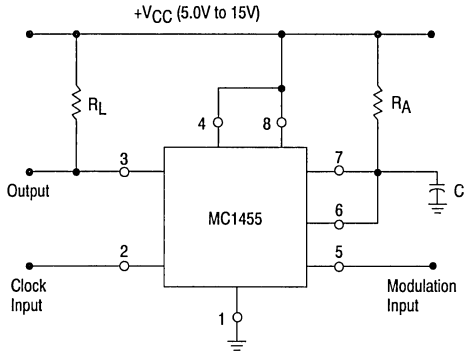
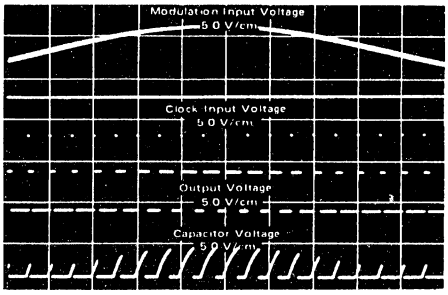


Figure 25. Pulse Width Modulation Waveforms



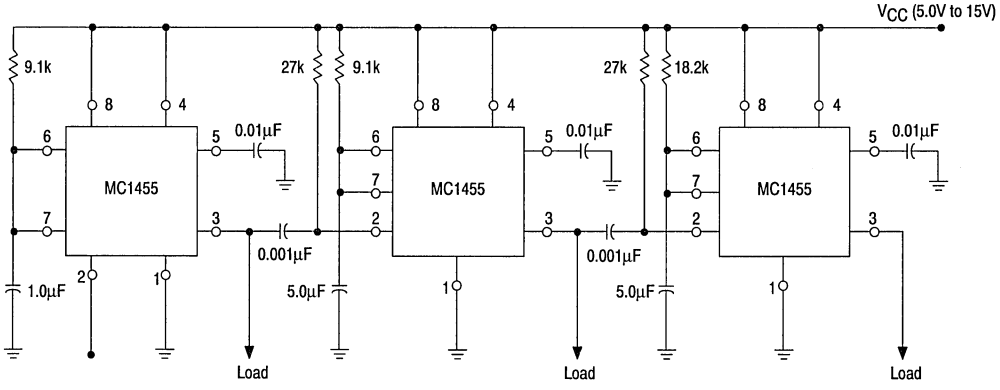
t = 0.5 ms/cm

(R_A = 10 kΩ, C = 0.02 µF, V_{CC} = 15 V)

Test Sequences

Several timers can be connected to drive each other for sequential timing. An example is shown in Figure 26 where the sequence is started by triggering the first timer which runs for 10 ms. The output then switches low momentarily and starts the second timer which runs for 50 ms and so forth.

Figure 26. Sequential Timer



11

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC1494
MC1594

Linear Four-Quadrant Multiplier

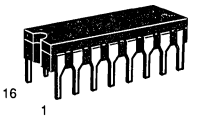
LINEAR FOUR-QUADRANT MULTIPLIER INTEGRATED CIRCUIT

SILICON MONOLITHIC EPITAXIAL PASSIVATED

The MC1494/1594 is designed for use where the output voltage is a linear product of two input voltages. Typical applications include: multiply, divide, square root, mean square, phase detector, frequency doubler, balanced modulator/ demodulator, electronic gain control.

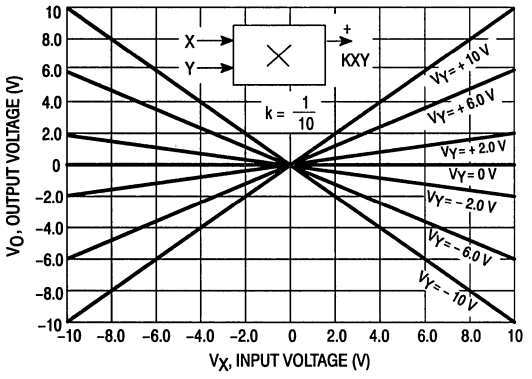
The MC1494/1594 is a variable transconductance multiplier with internal level-shift circuitry and voltage regulator. Scale factor, input offsets and output offset are completely adjustable with the use of four external potentiometers. Two complementary regulated voltages are provided to simplify offset adjustment and improve power supply rejection.

- Operates with ±15 V Supplies
- Excellent Linearity: Maximum Error (X or Y): ±0.5% (MC1594)
  ±1.0% (MC1494)
- Wide Input Voltage Range: ±10 V
- Adjustable Scale Factor, K (0.1 nominal)
- Single-Ended Output Referenced to Ground
- Simplified Offset Adjust Circuitry
- Frequency Response (3 dB Small-Signal): 1.0 MHz
- Power Supply Sensitivity: 30 mV/V typical

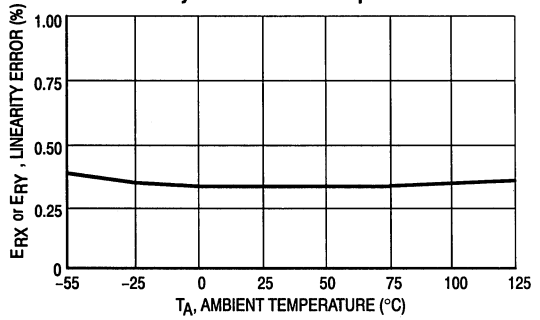


L SUFFIX
CERAMIC PACKAGE
CASE 620

Multiplier Transfer Characteristic



Linearity Error versus Temperature



ORDERING INFORMATION

Device	Ambient Temperature Range	Package
MC1494L	0° to +70°C	Ceramic DIP
MC1495L	−55° to +125°C	Ceramic DIP

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MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

Rating		Symbol	Value	Unit
Power Supply Voltages		± V	± 18	Vdc
Differential Input Signal		V_9–V_6 V_{10}–V_{13}	±|6 + I_1R_Y|<30 ±|6 + I_1R_X|<30	Vdc
Common Mode Input Voltage V_{CMY} = V_9 = V_6 V_{CMX} = V_{10} = V_{13}		 V_{CMY} V_{CMX}	 ±11.5 ±11.5	Vdc
Power Dissipation (Package Limitation) T_A = +25°C Derate above T_A = +25°C		 P_D $1/\theta_{JA}$	 750 5.0	 mW mW/°C
Operating Temperature Range	MC1494 MC1594	T_A	0 to +70 –55 to +125	°C
Storage Temperature Range		T_{stg}	–65 to +150	°C

ELECTRICAL CHARACTERISTICS (±V = ±15 V, T_A = +25°C, R1 = 16 kΩ, R_X = 30 kΩ, R_Y = 62 kΩ, R_L = 47 kΩ, unless otherwise noted.)

Characteristics	Fig.	Symbol	MC1594 Min	MC1594 Typ	MC1594 Max	MC1494 Min	MC1494 Typ	MC1494 Max	Unit
Linearity Output error in percent of full scale –10 V <V_X < +10 V (V_Y = ±10 V) –10 V <V_Y < +10 V (V_X = ±10 V) T_A = +25°C T_A = T_{high} or T_{low} (Note 1)	1	E_{RX} or E_{RY}	 — —	 ±0.3 —	 ±0.5 ±0.8	 — —	 ±0.5 —	 ±1.0 ±1.3	%
Input Voltage Range (V_X = V_Y = V_{in}) Resistance (X or Y Input) Offset Voltage (X Input) (Note 1) (Y Input) (Note 1) Bias Current (X or Y Input) Offset Current (X or Y Input)	2,3,4	 V_{in} R_{in} $\|V_{iox}\|$ $\|V_{ioy}\|$ I_b $\|I_{io}\|$	 ±10 — — — — —	 — 300 0.1 0.4 0.5 28	 — — 1.6 1.6 1.5 150	 ±10 — — — — —	 — 300 0.2 0.8 1.0 50	 — — 2.5 2.5 2.5 400	 V_{pk} MΩ V µA nA
Output Voltage Swing Capability Impedance Offset Voltage (Note 1) Offset Current (Note 1)	3,4	 V_O R_O $\|V_{OO}\|$ $\|I_{OO}\|$	 ±10 — — —	 — 850 0.8 17	 — — 1.6 34	 ±10 — — —	 — 850 1.2 25	 — — 2.5 52	 V_{pk} kΩ V µA
Temperature Stability (Drift) T_A = T_{high} to T_{low} Output Offset (X = 0, Y = 0) Voltage Current X Input Offset (Y = 0) Y Input Offset (X = 0) Scale Factor Total DC Accuracy Drift (X = 10, Y = 10)		 $\|TCV_{OO}\|$ $\|TCI_{OO}\|$ $\|TCV_{iox}\|$ $\|TCV_{ioy}\|$ $\|TCK\|$ $\|TCE\|$	 — — — — — —	 1.3 27 0.3 1.5 0.07 0.09	 — — — — — —	 — — — — — —	 1.3 27 0.3 1.5 0.07 0.09	 — — — — — —	 mV/°C nA/°C mV/°C %/°C
Dynamic Response Small Signal (3.0 dB) Power Bandwidth (47 k) 3° Relative Phase Shift 1% Absolute Error	5	 BW_{3dB} (X) BW_{3dB} (Y) P_{BW} fϕ fθ	 — — — — —	 0.8 1.0 440 240 30	 — — — — —	 — — — — —	 0.8 1.0 440 240 30	 — — — — —	 MHz kHz
Common Mode Input Swing (X or Y) Gain (X or Y)	6	 CMV A_{CM}	 ±10.5 —	 — –65	 — —	 ±10.5 —	 — –65	 — —	 V_{pk} dB
Power Supply Current Quiescent Power Dissipation Sensitivity	7	 I_{d+} I_{d-} P_D S+ S–	 — — — — —	 6.0 6.5 185 13 30	 9.0 9.0 260 50 100	 — — — — —	 6.0 6.5 185 13 30	 12 12 350 100 200	 mAdc mW mV/V
Regulated Offset Adjust Voltages Positive/Negative Temperature Coefficient (V_{R+} or V_{R-}) Power Supply Sensitivity (V_{R+} or V_{R-})	7	 V_{R+}, V_{R-} TCV_R S_{R+}, S_{R-}	 3.5 — —	 4.3 0.03 0.6	 5.0 — —	 3.5 — —	 4.3 0.03 0.6	 5.0 — —	 Vdc mV/°C mV/V

NOTES: 1. Offsets can be adjusted to zero with external potentiomers. T_{high} = +70°C for MC1494, +125°C for MC1594 T_{low} = 0°C for MC1494, –55°C for MC1594

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Figure 1. Linearity

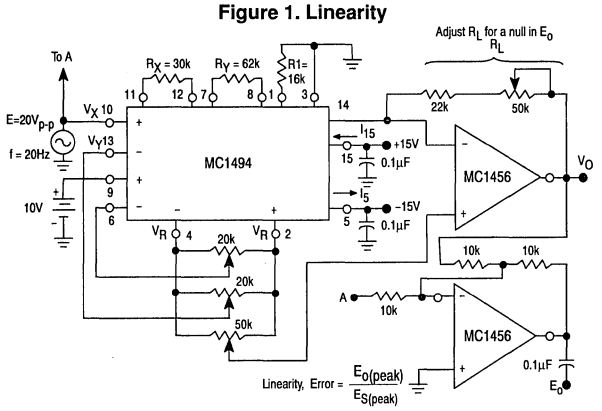


Figure 2. Input Resistance

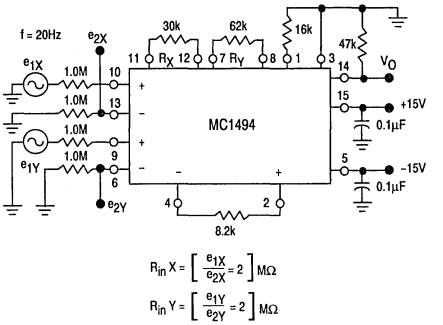


Figure 3. Offset Voltages, Gain

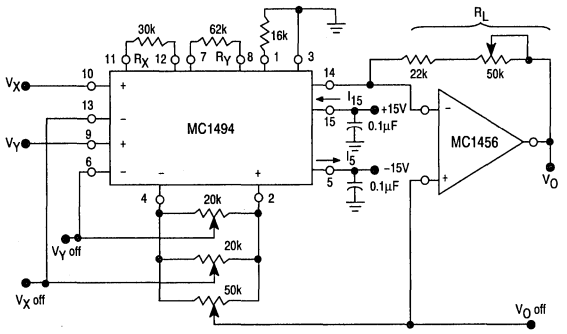


Figure 4. Input Bias Current/Input Offset Current, Output Resistance

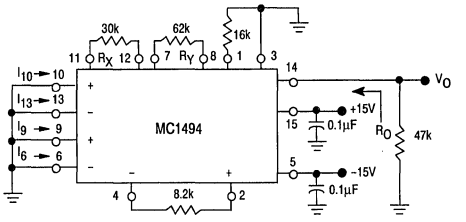


Figure 5. Frequency Response

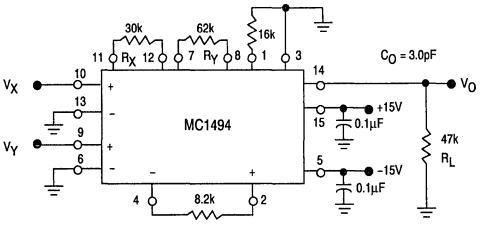


Figure 6. Common Mode

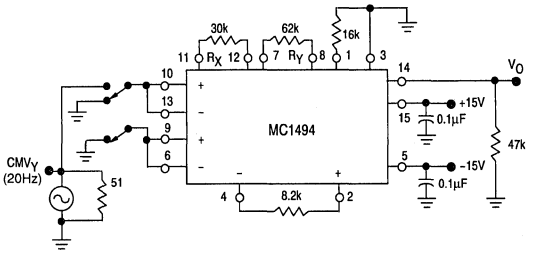


Figure 7. Power Supply Sensitivity

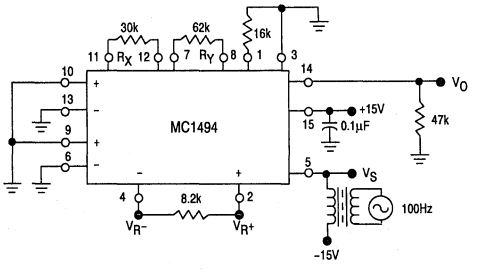


Figure 8. Burn-In

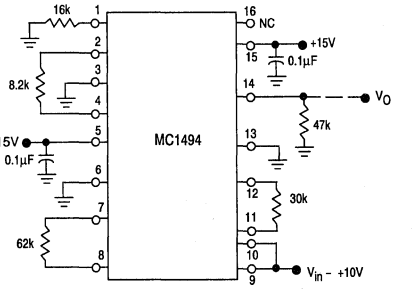


Figure 9. Frequency Response of Y Input versus Load Resistance

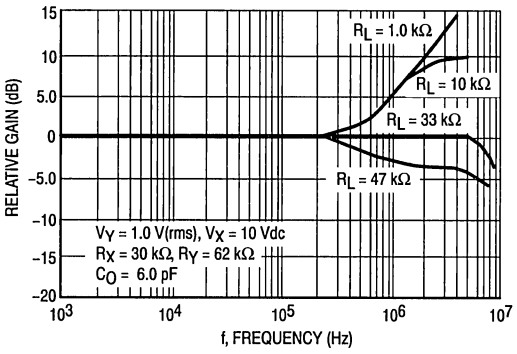


Figure 10. Frequency Response of X Input versus Load Resistance

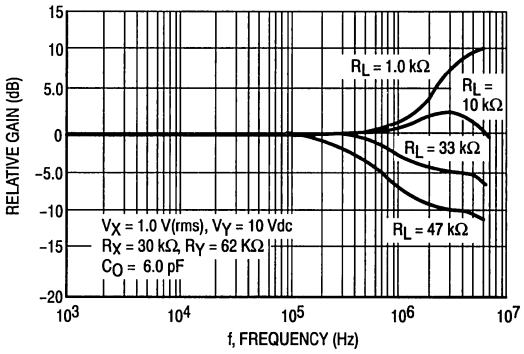


Figure 11. Linearity versus R_X or R_Y with K = 1

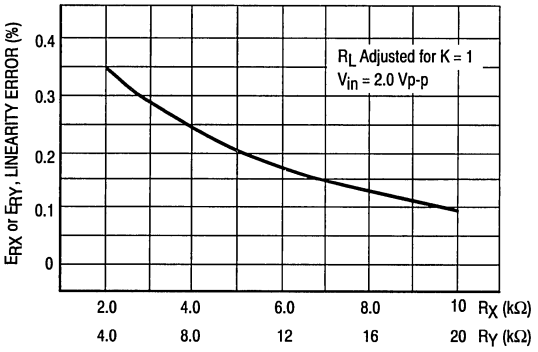


Figure 12. Linearity versus R_X or R_Y with K = 1/10

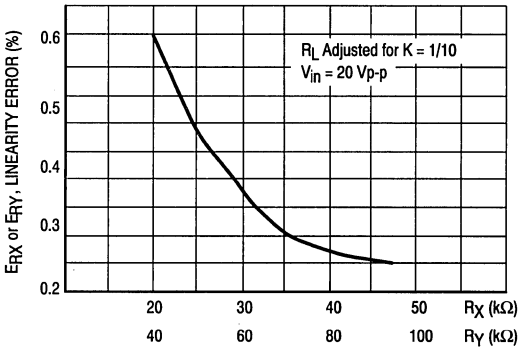


Figure 13. Large Signal Voltage versus Frequency

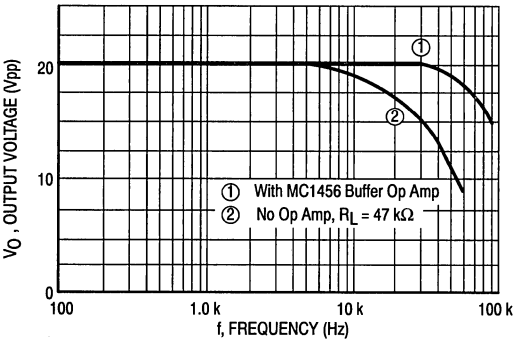
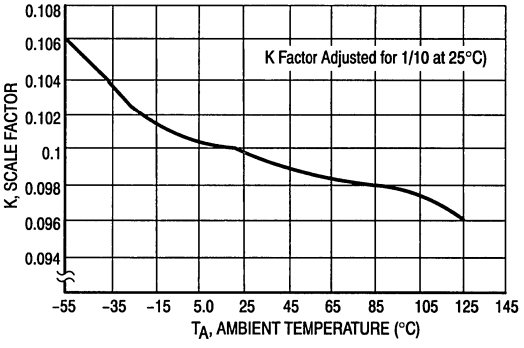


Figure 14. Scale Factor (K) versus Temperature



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CIRCUIT DESCRIPTION

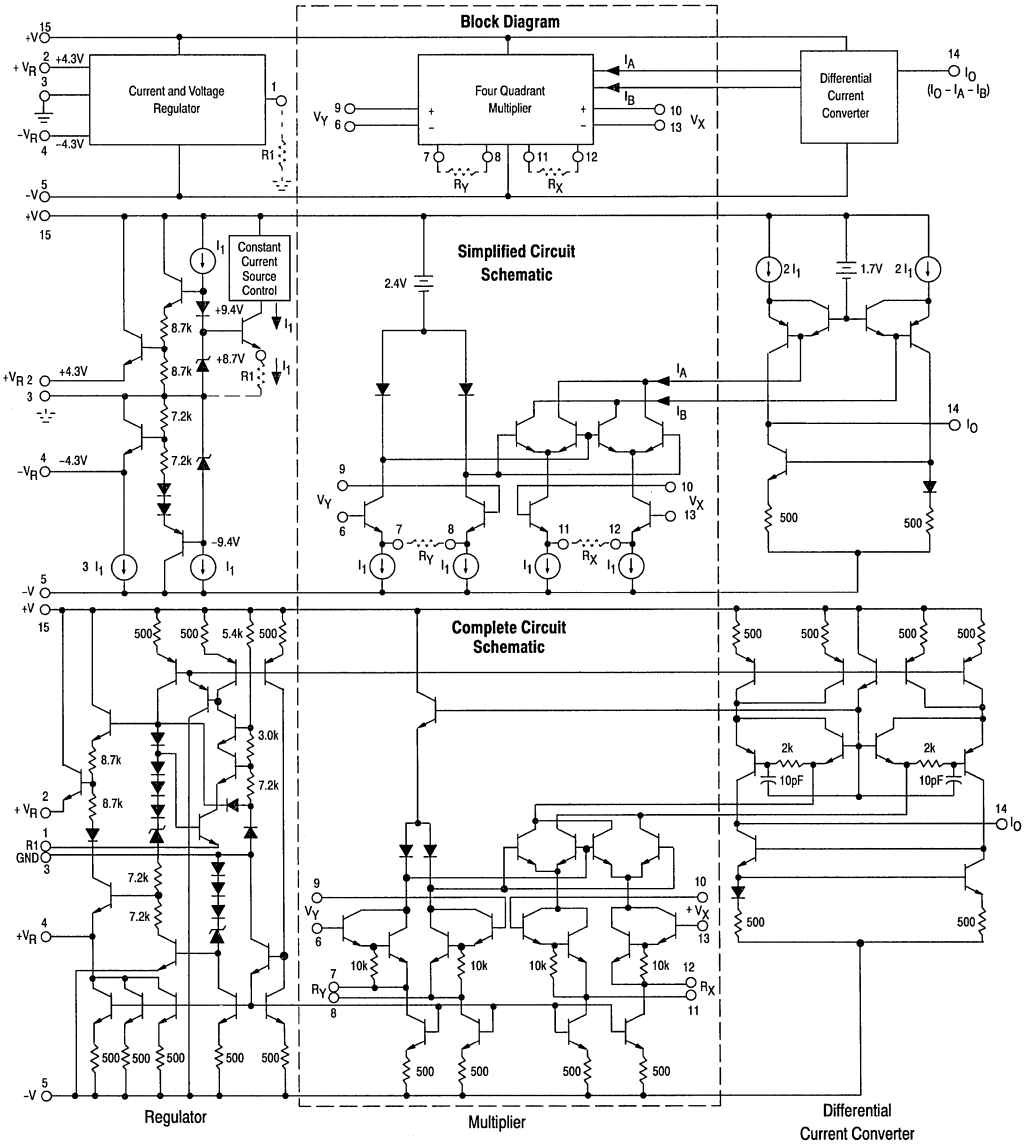
Introduction

The MC1494 is a monolithic, four-quadrant multiplier that operates on the principle of variable transconductance. It features a signal-ended current output referenced to ground and provides two complementary regulated voltages for use with the offset adjust circuits to virtually eliminate sensitivity of the offset voltage nulls to changes in supply voltages.

As shown in Figure 15, the MC1494 consists of a multiplier proper and associated peripheral circuitry to provide these features.

Figure 15

(Recommended External Circuitry is Depicted within Dotted Lines)



Regulator

The regulator biases the entire MC1494 circuit making it essentially independent of supply variation. It also provides two convenient regulated supply voltages which can be used in the offset adjust circuitry. The regulated output voltage at Pin 2 is approximately +4.3 V, while the regulated voltage at Pin 4 is approximately −4.3 V. For optimum temperature stability of these regulated voltages, it is recommended that $|I_2| = |I_4| = 1.0$ mA (equivalent load of 8.6 kΩ). As will be shown later, there will normally be two 20 kΩ potentiometers and one 50 kΩ potentiometer connected between Pins 2 and 4.

The regulator also establishes a constant current reference that controls all of the constant current sources in the MC1494. Note that all current sources are related to current I_1 which is determined by R1. For best temperatures performance, R1 should be 16 kΩ so that $I_1 \approx 0.5$ mA for all applications.

Multiplier

The multiplier section of the MC1494 (center section of Figure 15) is nearly identical to the MC1495 and is discussed in detail in Application Note AN489, *Analysis and Basic Operation of the MC1495*. The result of this analysis is that the differential output current of the multiplier is given by:

$$I_A - I_B = \Delta I \approx \frac{2V_X V_Y}{R_X R_Y I_1}$$

Therefore, the output is proportional to the product of the two input voltages.

Differential Current Converter

This portion of the circuitry converts the differential output current ($I_A - I_B$) of the multiplier to a single-ended output current (I_O); $I_O = I_A - I_B$

$$\text{or} \quad I_O = \frac{2V_X V_Y}{R_X R_Y I_1}$$

The output current can be easily converted to an output voltage by placing a load resistor R_L from the output (Pin 14) to ground (Figure 17) or by using an op amp as a current-to-voltage converter (Figure 16). The result in both circuits is that the output voltage is given by:

$$V_O = \frac{2R_L V_X V_Y}{R_X R_Y I_1} = KV_X V_Y$$

$$\text{where, K (scale factor)} = \frac{2R_L}{R_X R_Y I_1}$$

DC OPERATION

Selection of External Components

For low frequency operation the circuit of Figure 16 is recommended. For this circuit, R_X = 30 kΩ, R_Y = 62 kΩ, R1 = 16 kΩ and, hence, $I_1 \approx 0.5$ mA. Therefore, to set the scale factor (K) equal to 1/10, the value of R_L can be calculated to be:

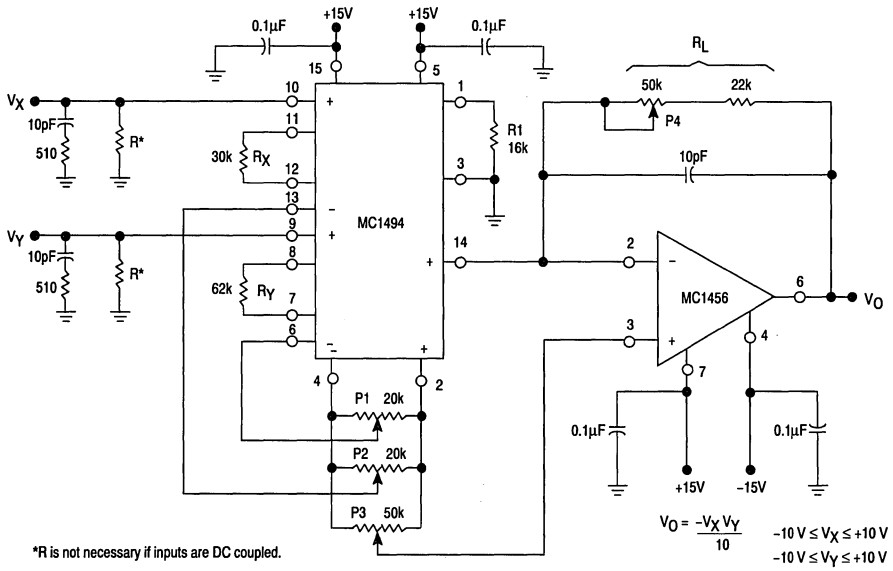
$$K = \frac{1}{10} = \frac{2R_L}{R_X R_Y I_1}$$

$$\text{or} \quad R_L = \frac{R_X R_Y I_1}{(2)\,(10)} = \frac{(30\text{ k})\,(62\text{ k})\,(0.5\text{ mA})}{20}$$

$$R_L = 46.5\text{ k}$$

Thus, a reasonable accuracy in scale factor can be achieved by making R_L a fixed 47 kΩ resistor. However, if it is desired that the scale factor be exact, R_L can be comprised of a fixed resistor and a potentiometer as shown in Figure 16.

Figure 16. Typical Multiplier Connection



It should be pointed out that there is nothing magic about setting the scale factor to 1/10. This is merely a convenient factor to use if the V_X and V_Y input voltages are expected to be large, say ±10 V. Obviously with $V_X = V_Y = 10$ V and a scale factor of unity, the device could not hope to provide a 100 V output, so the scale factor is set to 1/10 and provides an output scaled down by a factor of ten. For many applications it may be desirable to set K = 1/2 or K = 1 or even K = 100. This can be accomplished by adjusting R_X, R_Y and R_L appropriately.

The selection of R_L is arbitrary and can be chosen after resistors R_X and R_Y are found. Note in Figure 16 that R_Y is 62 kΩ while R_X is 30 kΩ. The reason for this is that the "Y" side of the multiplier exhibits a second order nonlinearity whereas the "X" side exhibits a simple nonlinearity. By making the R_Y resistor approximately twice the value of the R_X resistor, the linearity on both the "X" and "Y" sides are made equal. The selection of the R_X and R_Y resistor values is dependent upon the expected amplitude of V_X and V_Y inputs. To maintain a specified linearity, resistors R_X and R_Y should be selected according to the following equations:

$R_X \geq 3\ V_X$ (max) in kΩ when V_X is in Volts,

$R_Y \geq 6\ V_Y$ (max) in kΩ when V_Y is in Volts.

For example, if the maximum input on the "X" side is ±1.0 V, resistor R_X can be selected to be 3.0 kΩ. If the maximum input on the "Y" side is also ±1.0 V, then resistor R_Y can be selected to be 6.0 kΩ (6.2 kΩ nominal value). If a scale factor of K = 10 is desired, the load resistor is found to be 47 kΩ. In this example, the multiplier provides a gain of 20 dB.

Operational Amplifier Selection

The operational amplifier connection in Figure 16 is a simple but extremely accurate current-to-voltage converter. The output current of the multiplier flows through the feedback resistor R_L to provide a low impedance output voltage from the op amp. Since the offset current and bias currents of the op amp will cause errors in the output voltage, particularly with temperature, one with very low bias and offset currents is recommended. The MC1456 or MC1741 are excellent choices for this application.

Since the MC1494 is capable of operation at much higher frequencies than the op amp, the frequency characteristics of the circuit in Figure 16 will be primarily dependent upon the operational amplifier.

Stability

The current-to-voltage converter mode is a most demanding application for an operational amplifier. Loop gain is at its maximum and the feedback resistor in conjunction with stray or input capacitance at the multiplier output adds additional phase shift. It may therefore be necessary to add (particularly in the case of internally compensated op amps) a small feedback capacitor to reduce loop gain at the higher frequencies. A value of 10 pF in parallel with R_L should be adequate to insure stability over production and temperature variations, etc.

An externally compensated op amp might be employed using slightly heavier compensation than that recommended for unity-gain operation.

Offset Adjustment

The noninverting input of the op amp provides a convenient point to adjust the output offset voltage. By connecting this point to the wiper arm of a potentiometer (P3), the output offset voltage can be adjusted to zero (see Offset and Scale Factor Adjustment Procedure).

The input offset adjustment potentiometers, P1 and P2 will be necessary for most applications where it is desirable to take advantage of the multiplier's excellent linearity characteristics. Depending upon the particular application, some of the potentiometers can be omitted (see Figures 17, 19, 22, 24 and 25).

Offset and Scale Factor Adjustment Procedure

The adjustment procedure for the circuit of Figure 16 is:

A. X Input Offset
   1. Connect oscillator (1.0 kHz, 5.0 Vp-p sinewave) to the "Y" input (Pin 9).
   2. Connect "X" input (Pin 10) to ground.
   3. Adjust X-offset potentiometer, P2 for an AC null at the output.

B. Y Input Offset
   1. Connect oscillator (1.0 kHz, 5.0 Vp-p sinewave) to the "X" input (Pin 10).
   2. Connect "Y" input (Pin 9) to ground.
   3. Adjust Y-offset potentiometer, P1 for an AC null at the output.

C. Output Offset
   1. Connect both "X" and "Y" inputs to ground.
   2. Adjust output offset potentiometer, P3 until the output voltage V_O is 0 Vdc.

D. Scale Factor
   1. Apply +10 Vdc to both the "X" and "Y" inputs.
   2. Adjust P4 to achieve –10 V at the output.
   3. Apply –10 Vdc to both "X" and "Y" inputs and check for $V_O = -10$ V.

E. Repeat steps A through D as necessary.

The ability to accurately adjust the MC1494 is dependent on the offset adjust potentiometers. Potentiometers should be of the "infinite" resolution type rather than wirewound. Fine adjustments in balanced-modulator applications may require two potentiometers to provide "coarse" and "fine" adjustment. Potentiometers should have low temperature coefficients and be free from backlash.

Temperature Stability

While the MC1494 provides excellent performance in itself, overall performance depends to a large degree on the quality of the external components. Previous discussion shows the direct dependence on R_X, R_Y and R_L and indirect dependence on R1 (through I_1). *Any circuit subjected to temperature variations should be evaluated with these effects in mind.*

Bias Currents

The MC1494 multiplier, like most linear ICs, requires a DC bias current into its input terminals. The device cannot be capacitively coupled at the input without regard for this bias current. If inputs V_X and V_Y are able to supply the small bias current (≈0.5 μA) resistors R can be omitted (see Figure 16). If the MC1494 is used in an AC mode of operation and

capacitive coupling is used the value of resistor R can be any reasonable value up to 100 kΩ. For minimum noise and optimum temperature performance, the value of resistor R should be as low as practical.

Parasitic Oscillation

When long leads are used on the inputs, oscillation may occur. In this event, an RC parasitic suppression network similar to the ones shown in Figure 16 should be connected directly to each input using short leads. The purpose of the network is to reduce the "Q" of the source-tuned circuits which cause the oscillation.

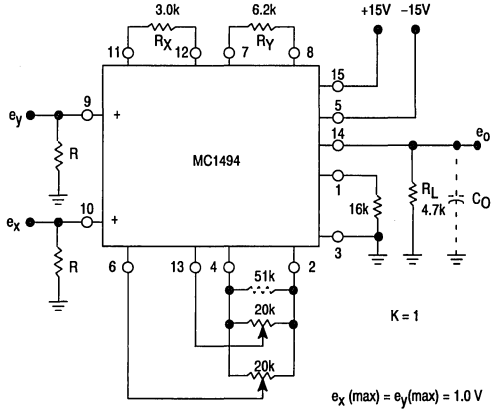
Inability to adjust the circuit to within the specified accuracy may be an indication of oscillation.

AC OPERATION

General

For AC operation, such as balanced modulation, frequency doubler, AGC, etc., the op amp will usually be omitted as well as the output offset adjust potentiometer. The output offset adjust potentiometer is omitted since the output will normally be AC coupled and the DC voltage at the output is of no concern providing it is close enough to zero volts that it will not cause clipping in the output waveform. Figure 17 shows a typical AC multiplier circuit with a scale factor K≈1. Again, resistor R_X and R_Y are chosen as outlined in the previous section, with R_L chosen to provide the required scale factor.

Figure 17. Wideband Multiplier



The offset voltage then existing at the output will be equal to the offset current times the load resistance. The output offset current of the MC1494 is typically 17 μA and 35 μA maximum. Thus, the maximum output offset would be about 160 mV.

Bandwidth

The bandwidth of the MC1494 is primarily determined by two factors. First, the dominant pole with be determined by the load resistor and the stray capacitance at the output terminal. For the circuit shown in Figure 17, assuming a total output capacitance (C_O) of 10 pF, the 3.0 dB bandwidth would be approximately 3.4 MHz. If the load resistor were 47 kΩ, the bandwidth would be approximately 340 kHz.

Secondly, a "zero" is present in the frequency response characteristic for both the "X" and "Y" inputs which causes the output signal to rise in amplitude at a 6 dB/octave slope at frequencies beyond the breakpoint of the "zero". The "zero" is caused by the parasitic and substrate capacitance which is related to resistors R_X and R_Y and the transistors associated with them. The effect of these transmission "zeros" is seen in Figures 9 and 10. The reason for this increase in gain is due to the bypassing of R_X and R_Y at high frequencies. Since the R_Y resistor is approximately twice the value of the R_X resistor, the zero associated with the "Y" input will occur at approximately one octave below the zero associated with "X" input. For R_X = 30 kΩ and R_Y = 62 kΩ, the zeros occur at 1.5 MHz for the "X" input and 700 kHz for the "Y" input. These two measured breakpoints correspond to a shunt capacitance of about 3.5 pF. Thus, for the circuit of Figure 17, the "X" input zero and "Y" input zero will be at approximately 15 MHz and 7.0 MHz respectively.

It should be noted that the MC1494 multiplies in the time domain, hence, its frequency response is found by means of complex convolution in the frequency (Laplace) domain. This means that if the "X" input does not involve a frequency, it is not necessary to consider the "X" side frequency response in the output product. Likewise, for the "Y" side. Thus, for applications such as a wideband linear AGC amplifier which has a DC voltage as one input, the multiplier frequency response has one zero and one pole. For applications which involve an AC voltage on both the "X" and "Y" side such as a balanced modulator, the product voltage response will have two zeros and one pole, hence, peaking may be present in the output.

From this brief discussion, it is evident that for AC applications; (1) the value of resistors R_X, R_Y and R_L should be kept as small as possible to achieve maximum frequency response, and (2) it is possible to select a load resistor R_L such that the dominant pole (R_L, C_O) cancels the input zero (R_X, 3.5 pF or R_Y, 3.5 pF) to give a flat amplitude characteristic with frequency. This is shown in Figures 9 and 10. Examination of the frequency characteristics of the "X" and "Y" inputs will demonstrate that for wideband amplifier applications, the best tradeoff with frequency response and gain is achieved by using the "Y" input for the AC signal.

For AC applications requiring bandwidths greater than those specified for the MC1494, two other devices are recommended. For modulator-demodulator applications, the MC1496 may be used up to 100 MHz. For wideband multiplier applications, the MC1495 (using small collector loads and AC coupling) can be used.

Slew-Rate

The MC1494 multiplier is not slew-rate limited in the ordinary sense that an op amp is. Since all the signals in the multiplier are currents and not voltages, there is no charging and discharging of stray capacitors and thus no limitations beyond the normal device limitataions. However, it should be noted that the quiescent current in the output transistors is

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0.5 mA and thus the maximum rate of change of the output voltage is limited by the output load capacitance by the simple equation:

$$\text{Slew Rate } \frac{\Delta V_O}{\Delta T} = \frac{I_O}{C}$$

Thus, if C_O is 10 pF, the maximum slew rate would be:

$$\frac{\Delta V_O}{\Delta T} = \frac{0.5 \times 10^{-3}}{10 \times 10^{-12}} = 50 \text{ V/}\mu\text{s}$$

This can be improved, if necessary, by the addition of an emitter-follower or other type of buffer.

Phase Vector Error

All multipliers are subject to an error which is known as the phase vector error. This error is a phase error only and does not contribute an amplitude error per se. The phase vector error is best explained by an example. If the "X" input is described in vector notation as;

$$X = A \angle 0°$$

and the "Y" input is described as;

$$Y = B \angle 0°$$

then the output product would be expected to be;

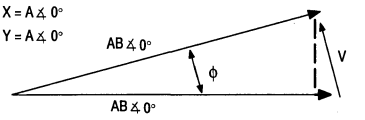
$$V_O = AB \angle 0° \text{ (see Figure 18)}$$

However, due to a relative phase shift between the "X" and "Y" channels, the output product will be given by:

$$V_O = AB \angle \phi$$

Notice that the magnitude is correct but the phase angle of the product is in error. The vector (V) associated with this error is the "phase vector error". The startling fact about the phase vector error is that it occurs and accumulates much more rapidly than the amplitude error associated with frequency response. In fact, a relative phase shift of only 0.57° will result in a 1% phase vector error. For most applications, this error is

Figure 18. Phase Vector Error



meaningless. If phase of the output product is not important, then neither is the phase vector error. If phase is important, such as in the case of double sideband modulation or demodulation, then a 1% phase vector error will represent a 1% amplitude error a the phase angle of interest.

Circuit Layout

If wideband operation is desired, careful circuit layout must be observed. Stray capacitance across R_X and R_Y should be avoided to minimize peaking (caused by a zero created by the parallel RC circuit).

DC APPLICATIONS

Squaring Circuit

If the two inputs are connected together, the resultant function is squaring:

$$V_O = KV^2$$

where K is the scale factor (see Figure 19).

However, a more careful look at the multiplier's defining equation will provide some useful information. The output voltage, without initial offset adjustments is given by:

$$V_O = K(V_X + V_{iox} - V_{X\,off})(V_Y + V_{ioy} - V_{Y\,off}) + V_{OO}$$

(Refer to "Definitions" section for an explanation of terms.)

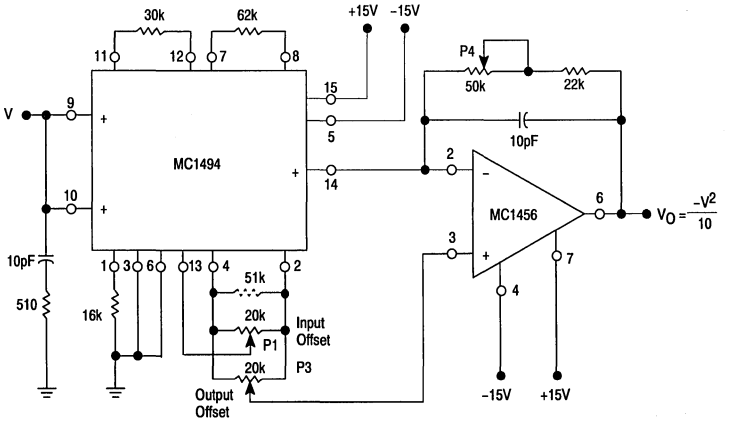
With $V_X = V_Y = V$ (squaring) and defining;

$$\epsilon_x = V_{iox} - V_{x\,(off)}$$
$$\epsilon_y = V_{ioy} - V_{y\,(off)}$$

The output voltage equation becomes:

$$V_O = KV_x^2 + KV_x(\epsilon_x + \epsilon_y) + K\epsilon_x\epsilon_y + V_{OO}$$

Figure 19. MC1594 Squaring Circuit



This shows that all error terms can be eliminated with only three adjustment potentiometers, eliminating one of the input offset adjustments. For instance, if the "X" input offset adjustment is eliminated, ϵ_X is determined by the internal offset (V_{IOX}) but ϵ_Y is adjustable to the extent that the ($\epsilon_X + \epsilon_Y$) term can be zeroed. Then the output offset adjustment is used to adjust the V_{OO} term and thus zero the remaining error terms. An AC procedure for nulling with three adjustments is:

A. AC Procedure:
   1. Connect oscillator (1.0 kHz, 15 Vp-p) to input.
   2. Monitor output at 2.0 kHz with tuned voltmeter and adjust P4 for desired gain (Be sure to peak response of voltmeter).
   3. Tune voltmeter to 1.0 kHz and adjust P1 for a minimum output voltage.
   4. Ground input and adjust P3 (output offset) for 0 Vdc out.
   5. Repeat steps 1 through 4 as necessary.

B. DC Procedure:
   1. Set $V_X = V_Y = 0$ V and adjust P3 (output offset potentiometer) such that $V_O = 0$ Vdc.
   2. Set $V_X = V_Y = 1.0$ V and adjust P1 (Y input offset potentiometer) such that the output voltage is –0.100 V.
   3. Set $V_X = V_Y = 10$ Vdc and adjust P4 (load resistor) such that the output voltage is –10 V.
   4. Set $V_X = V_Y = -10$ Vdc and check that $V_O = -10$ V.
   5. Repeat steps 1 through 4 as necessary.

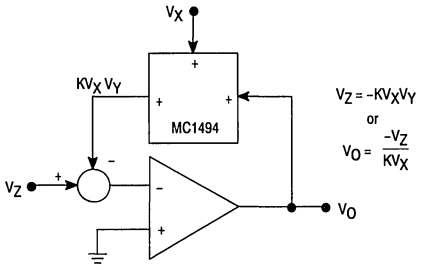
Divide

Divide circuits warrant a special discussion as a result of their special problems. Classic feedback theory teaches that if a multiplier is used as a feedback element in an operational amplifier circuit, the divide function results. Figure 20 illustrates the theoretical simplicity of such an approach and a practical realization is shown in Figure 21.

The characteristic "failure" mode of the divide circuit is latch-up. One way it can occur is if V_X is allowed to go negative, or in some cases, if V_X approaches zero.

Figure 20 illustrates why this is so. For $V_X > 0$ the transfer function through the multiplier is noninverting. Its output is fed to the inverting input of the op amp Thus, operation is in the negative feedback mode and the circuit is DC stable.

Figure 20. Basic Divide Circuit Using Multiplier

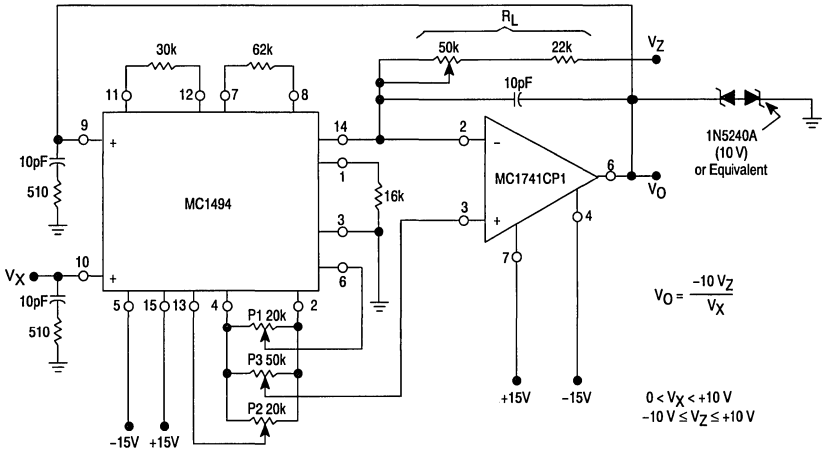


Should V_X change polarity, the transfer function through the multiplier becomes inverting, the amplifier has positive feedback and latch-up results. The problem resulting from V_X being near zero is a result of the transfer through the multiplier being near zero. The op amp is then operating with a very high closed-loop gain and error voltages can thus become effective in causing latch-up.

The other mode of latch-up results from the output voltage of the op amp exceeding the rated common mode input voltage of the multiplier. The input stage of the multiplier becomes saturated, phase reversal results, and the circuit is latched up. The circuit of Figure 21 protects against this happening by clamping the output swing of the op amp to approximately ± 10.7 V. Five percent tolerance, 10 V zeners are used to assure adequate output swing but still limit the output voltage of the op amp from exceeding the common mode input range of the MC1494.

Setting up the divide circuit for reasonably accurate operation is somewhat different from the procedure for the multiplier itself. One approach, however, is to break the feedback loop, null out the multiplier circuit, and then close the loop.

Figure 21. Practical Divide Circuit



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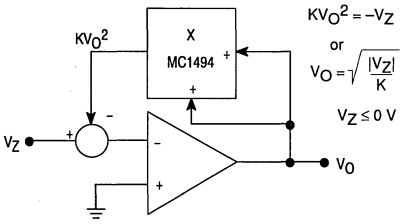
A simpler approach, since it does not involve breaking the loop (thus making it more practical on a production basis), is:

1. Set V_Z = 0 V and adjust the output offset potentiometer (P3) until the output voltage (V_O) remains at some (not necessarily zero) constant value as V_X is varied between +1.0 V and +10 V.
2. Maintain V_Z at 0 V, set V_X at +10 V and adjust the Y input offset potentiometer (P1) until V_O = 0 V.
3. With $V_X = V_Z$, adjust the X input offset potentiometer (P2) until the output voltage remains at some (not necessarily –10 V) constant value as $V_Z = V_X$ is varied between +1.0 V and +10 V.
4. Maintain $V_X = V_Z$ and adjust the scale factor potentiomeer (R_L) until the average value of V_O is –10 V as $V_Z = V_X$ is varied between +1.0 V and +10 V.
5. Repeat steps 1 through 4 as necessary to achieve optimum performance.

Users of the divide circuit should be aware that the accuracy to be expected decreases in direct proportion to the denominator voltage. As a result, if V_X is set to 10 V and 0.5% accuracy is available, then 5% accuracy can be expected when V_X is only 1.0 V.

In accordance with an earlier statement, V_X may have only one polarity (positive) while V_Z may be either polarity.

Figure 22. Basic Square Root Circuit



Square Root

A special case of the divide circuit in which the two inputs to the multiplier are connected together results in the square root function as indicated in Figure 22. This circuit too may suffer from latch-up problems similar to those of the divide circuit. Note that only one polarity of input is allowed and diode clamping (see Figure 23) protects against accidental latch-up. This circuit too, may be adjusted in the closed-loop mode:

1. Set V_Z = –0.01 Vdc and adjust P3 (output offset) for V_O = 0.316 Vdc.
2. Set V_Z to –0.9 Vdc and adjust P2 ("X" adjust) for V_O = +3.0 Vdc.
3. Set V_Z to –10 Vdc and adjust P4 (gain adjust) for V_O = +10 Vdc.
4. Steps 1 through 3 may be repeated as necessary to achieve desired accuracy.

Note: Operation near 0 V input may prove very inaccurate, hence, it may not be possible to adjust V_O to zero but rather only to within 100 mV to 400 mV of zero.

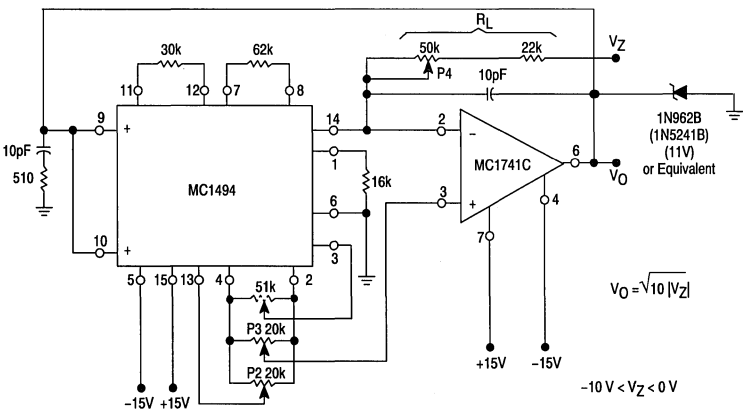
AC APPLICATIONS

Wideband Amplifier with Linear AGC

If one input to the MC1494 is a DC voltage and a signal voltage is applied to the other input, the amplitude of the output signal can be controlled in a linear fashion by varying the DC voltage. Hence, the multiplier can function as a DC coupled, wideband amplifier with linear AGC control.

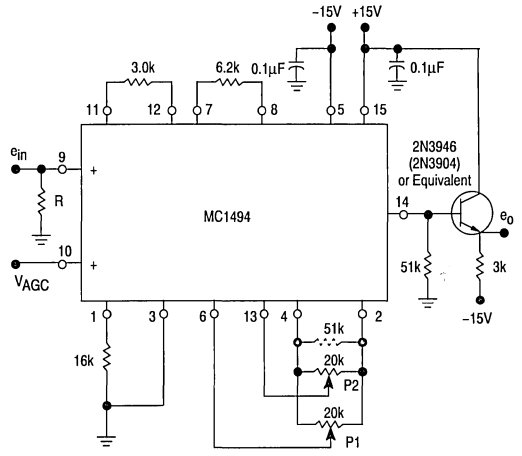
In addition to the advantage of linear AGC control, the multiplier has three other distinct advantages over most other types of AGC systems. First, the AGC dynamic range is theoretically infinite. This stems from the basic fact that with 0 Vdc applied to the AGC, the output will be zero regardless of the input. In practice, the dynamic range is limited by the ability to adjust the input offset adjust potentiometers. By using cermet multi-turn potentiometers, a dynamic range of 80 dB can be obtained. The second advantage of the multiplier is that variation of the AGC voltage has no effect on the signal handling capability of the signal port, nor does it alter the input impedance of the signal port. This feature is particularly important in AGC systems which are phase sensitive. A third advantage of the multiplier is that the output voltage swing capability and output impedance are unchanged with variations in AGC voltage.

Figure 23. Square Root Circuit



The circuit of Figure 24 demonstrates the linear AGC amplifier. The amplifier can handle 1.0 V (rms) and exhibits a gain of approximately 20 dB. It is AGC'd through a 60 dB dynamic range with the application of an AGC voltage from 0 Vdc to 1.0 Vdc. The bandwidth of the amplifier is determined by the load resistor and output stray capacitance. For this reason, an emitter-follower buffer has been added to extend the bandwidth in excess of 1.0 MHz.

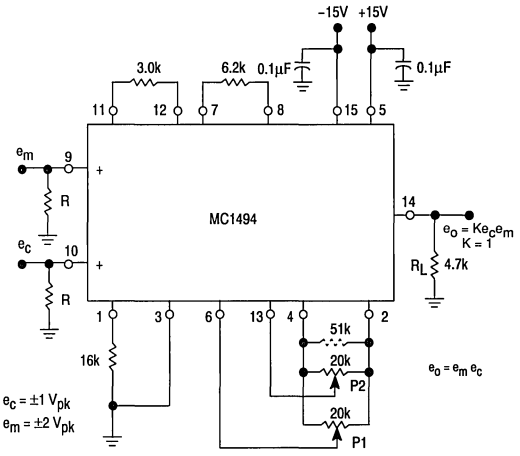
Figure 24. Wideband Amplifier with Linear AGC



The input reisstors (R) are used to supply bias current to the multiplier inputs as well as provide matching input impedance. The output frequency range of this configuration is determined by the 4.7 kΩ output impedance and capacitive loading. Assuming a 6.0 pF load, the small-signal bandwidth is 5.5 MHz.

The circuit of Figure 25 will provide at typical carrier rejection of ≥ 70 dB from 10 kHz to 1.5 MHz.

Figure 25. Balanced Modulator



Balanced Modulator

When two-time variant signals are used as inputs, the resulting output is suppressed-carrier double-sideband modulation. In terms of sinusoidal inputs, this can be seen in the following equation:

$$V_O = K(e_1 \cos\omega_m t)\,(e_2 \cos\omega_c t)$$

where ω_m is the modulation frequency and ω_c is the carrier frequency. This equation can be expanded to show the suppressed carrier or balanced modulation:

$$V_O = \frac{Ke_1e_2}{2}\,[\cos(\omega_c+\omega_m)\,t + \cos(\omega_c-\omega_m)t]$$

Unlike many modulation schemes, which are nonlinear in nature, the modulation which takes place when using the MC1494 is linear. This means that for two sinusoidal inputs, the output will contain only two frequencies, the sum and difference, as seen in the above equation. There will be no spectrum centered about the second harmonic of the carrier, or any multiple of the carrier. For this reason, the filter requirements of a modulation system are reduced to the minimum. Figure 25 shows the MC1494 configuration to perform this function.

Notice that the resistor values for R_X, R_Y and R_L have been modified. This has been done primarily to increase the bandwidth by lowering the output impedance of the MC1494 and then lowering R_X and R_Y to achieve a gain of 1. The e_c can be as large as 1.0 V peak and e_m as high as 2.0 V peak. No output offset adjust is employed since we are interested only in the AC output components.

The adjustment procedure for this circuit is quite simple.

1. Place the carrier signal at Pin 10. With no signal applied to Pin 9, adjust potentiometer P1 such that an AC null is obtained at the output.
2. Place a modulation signal at Pin 9. With no signal applied to Pin 10, adjust potentiometer P2 such that an AC null is obtained at the output.

Again, the ability to make careful adjustment of these offsets will be a function of the type of potentiometers used for P1 and P2. Multiple turn cermet type potentiometers are recommended.

Frequency Doubler

If for Figure 25 both inputs are identical:

$$e_m = e_c = E\cos\omega t$$

then the output is given by,

$$e_o = e_m e_c = E^2\cos^2\omega t$$

which reduces to,

$$e_o = \frac{E^2}{2}\,(1 + \cos 2\omega t)$$

This equation states that the output will consist of a DC term equal to one half the peak voltage squared and the second harmonic of the input frequency. Thus, the circuit acts as a frequency doubler. Two facts about this circuit are worthy of note. First, the second harmonic of the input frequency is the only frequency appearing at the output. The fundamental does not appear. Second, if the input is sinusoidal, the output will be sinusoidal and requires *no* filtering.

The circuit of Figure 25 can be used as a frequency doubler with input frequencies in excess of 2.0 MHz.

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Amplitude Modulator

The circuit of Figure 25 is also easily used as an amplitude modulator. This is accomplished by simply varying the input offset adjust potentiometer (P1) associated with the mudulation input. This procedure places a DC offset on the modulation input of the multiplier such that the carrier still passes through the multiplier when the modulating signal is zero. The result is amplitude modulation. This is easily seen by examining the basic mathematical expression for amplitude modulation given below. For the case under discussion, with K = 1,

$$e_o = (E + E_m \cos\omega_m t)(E_c \cos\omega_c t)$$

where E is the DC input offset adjust voltage. This expression can be written as:

$$e_o = E_o [1 + M \cos\omega_c t] \cos\omega_c t$$

where, $E_o = EE_c$

and, $M = \frac{E_m}{E}$ = modulation index.

This is the standard equation for amplitude modulation. From this, it is easy to see that 100% modulation can be achieved by adjusting the input offset adjust voltage to be exactly equal to the peak value of the modulation (E_m). This is done by observing the output waveform and adjusting the input offset potentiometer (P1) until the output exhibits the familiar amplitude modulation waveform.

Phase Detector

If the circuit of Figure 25 has as its inputs two signals of identical frequency, but having a relative phase shift, the output will be a DC signal which is directly proportional to the cosine of phase difference as well as the double frequency term.

$$e_c = E_c \cos\omega_c t$$
$$e_m = E_m \cos(\omega_c t + \phi)$$
$$e_o = e_c e_m = E_c E_m \cos\omega_c t \cos(\omega_c t + \phi)$$
$$\text{or, } e_o = \frac{E_c E_m}{2} [\cos\phi + \cos(2\omega_c t + \phi)]$$

The addition of a simple low pass filter to the output (which eliminates the second cosine term) and return of R_L to an offset adjustment potentiometer will result in a DC output voltage which is proportional to the cosine of the phase difference. Hence, the circuit functions as a synchronous detector.

DEFINITION OF SPECIFICATIONS

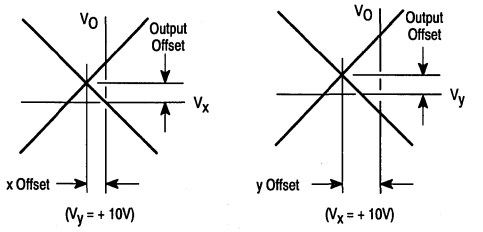
Because of the unique nature of a multiplier, i.e., two inputs and one output, operating specifications are difficult to define and interpret. Indeed the same specification may be defined in several completely different ways depending upon which manufacturer is doing the defining. In order to clear up some of the mystery, the following definitions and examples are presented.

MULTIPLIER TRANSFER FUNCTION — The output of the multiplier may be expressed by the following equation:

$$V_O = K[V_X \pm V_{iox} - V_{x(off)}][V_y \pm V_{ioy} - V_{y(off)}] \pm V_{OO} \quad (1)$$

where, K = scale factor
V_X = "x" input voltage
V_y = "y" input voltage
V_{iox} = "x" input offset voltage
V_{ioy} = "y" input offset voltage
$V_{x(off)}$ = "x" input offset adjust voltage
$V_{y(off)}$ = "y" input offset adjust voltage
V_{OO} = output offset voltage

The voltage transfer characteristic below indicates x, y and output offset voltages.



LINEARITY — Linearity is defined to be the maximum deviation of output voltage from a straight line transfer function. It is expressed as a percentage of full-scale output and is measured for V_X and V_y separately, either using an X-Y plotter (and checking the deviation from a straight line) or by using the method shown in Figure 1. The latter method nulls the output signal with the input signal, resulting in distortion components proportional to the linearity.

Example: 0.35% linearity means

$$V_O = \frac{V_X V_y}{10} \pm (0.0035)(10\ V)$$

INPUT OFFSET VOLTAGE — The input offset voltage is defined from Equation (1). It is measured for V_X and V_y separately and is defined to be that DC input offset adjust voltage (x or y) that will result in minimum AC output when AC (5.0 Vp-p, 1.0 kHz) is applied to the other input (y or x, respectively). From Equation (1) we have:

$$V_O(AC) = K[0 \pm V_{iox} - V_{x(off)}][\sin\omega t]$$

adjust $V_{x(off)}$ so that $[\pm V_{iox} - V_{x(off)}] = 0$.

OUTPUT OFFSET CURRENT AND VOLTAGE — Output offset current (I_{OO}) is the DC current flowing in the output lead when $V_X = V_y = 0$ and X and Y offset voltages are adjusted to zero.

Output offset voltage (V_{OO}) is:

$$V_{OO} = I_{OO} R_L$$

where R_L is the load resistance.

Note: Output offset voltage is defined by many manufacturers with all inputs at zero but without adjusting X and Y offset voltages to zero. Thus, it includes input offset terms, an output offset term and a scale factor term.

SCALE FACTOR — Scale factor is the K term in Equation (1). It determines the gain of the multiplier and is expressed approximately by the following equation.

$$K = \frac{2R_L}{R_X R_y I_1}, \text{ where } R_X \text{ and } R_y >> \frac{kT}{qI_1}$$

and I_1 is the current out of Pin 1.

TOTAL DC ACCURACY — The total DC accuracy of a multiplier is defined as error in multiplier output with DC (± 10 Vdc) applied to both inputs. It is expressed as a percent of full scale. Accuracy is not specified for the MC1494 because error terms can be nulled by the user.

TEMPERATURE STABILITY (DRIFT) — Each term defined above will have a finite drift with temperature. The temperature specifications are obtained by readjusting the multiplier offsets and scale factor at each new temperature (see previous definitions and the adjustment procedure) and noting the change.

Assume inputs are grounded and initial offset voltages have been adjusted to zero. Then output voltage drift is given by:

$$\Delta V_O = \pm [K \pm K\,(TCK)\,(\Delta T)]\,[(TCV_{iox})\,(\Delta T)]\,[(TCV_{ioy})\,(\Delta T)] \pm (TCV_{OO})\,(\Delta T)$$

TOTAL DC ACCURACY DRIFT — This is the temperature drift in output voltage with 10 V applied to each input. The output is adjusted to 10 V at $T_A = +25°C$. Assuming initial offset voltages have been adjusted to zero at $T_A = +25°C$, then:

$$V_O = [\,K \pm K\,(TCK)\,(\Delta T)]\,[10 \pm (TCV_{iox})\,(\Delta T)]\,[10 \pm (TCV_{ioy})\,(\Delta T)] \pm (TCV_{OO})\,(\Delta T)$$

POWER SUPPLY REJECTION — Variation in power supply voltages will cause undesired variation of the output voltage. It is measured by superimposing a 1.0 V, 100 Hz signal on each supply (±15 V) with each input grounded. The resulting change in the output is expressed in mV/V.

OUTPUT VOLTAGE SWING — Output voltage swing capability is the maximum output voltage swing (without clipping) into a resistive load. (Note, output offset is adjusted to zero).

If an op amp is used, the multiplier output becomes a virtual ground — the swing is then determined by the scale factor and the op amp selected.

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC1495
MC1595

Wideband Linear Four-Quadrant Multiplier

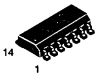
The MC1495/1595 is designed for use where the output is a linear product of two input voltages. Maximum versatility is assured by allowing the user to select the level shift method. Typical applications include: multiply, divide*, square root*, mean square*, phase detector, frequency doubler, balanced modulator/demodulator, and electronic gain control.

- Wide Bandwidth
- Excellent Linearity:
  2% max Error on X Input, 4% max Error on Y Input (MC1495)
  1% max Error on X Input, 2% max Error on Y Input (MC1595)
- Adjustable Scale Factor, K
- Excellent Temperature Stability
- Wide Input Voltage Range: ± 10 V
- ± 15 V Operation

*When used with an operational amplifier.

LINEAR FOUR-QUADRANT MULTIPLIER

SILICON MONOLITHIC INTEGRATED CIRCUIT



D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO-14)

L SUFFIX
CERAMIC PACKAGE
CASE 632

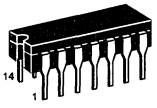


Figure 1. Multiplier Transfer Characteristic

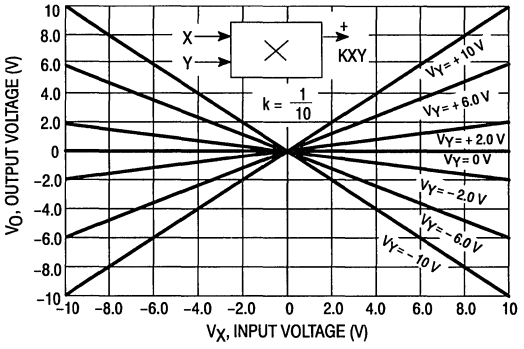


Figure 2. Transconductance Bandwidth

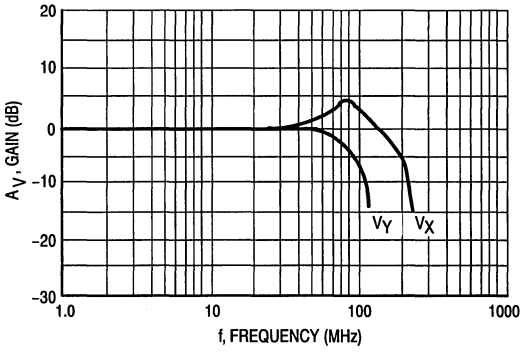
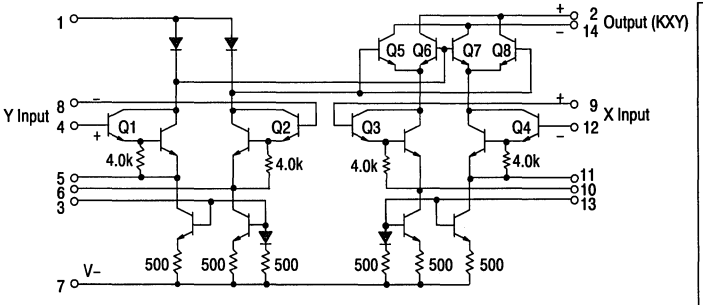


Figure 3. Circuit Schematic



ORDERING INFORMATION

Device	Ambient Temperature Range	Package
MC1495D	0° to +70°C	SO-14
MC1595D		
MC1495L	−55° to +125°C	Ceramic DIP
MC1595L		

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ELECTRICAL CHARACTERISTICS ($+V = +32$ V, $-V = -15$ V, $T_A = +25°C$, $I_3 = I_{13} = 1.0$ mA, $R_X = R_Y = 15$ kΩ, $R_L = 11$ kΩ, unless otherwise noted.)

Characteristics		Figure	Symbol	Min	Typ	Max	Unit
Linearity (Output Error in percent of full scale)		5					%
$T_A = +25°C$							
$-10 < V_X < +10$ ($V_Y = \pm 10$ V)	MC1495		E_{RX}	—	±1.0	±2.0	
	MC1595			—	±0.5	±1.0	
$-10 < V_Y < +10$ ($V_X = \pm 10$ V)	MC1495		E_{RY}	—	±2.0	±4.0	
	MC1595			—	+1.0	±2.0	
$T_A = 0°$ to $+70°C$							
$-10 < V_X < +10$ ($V_Y = \pm 10$ V)	MC1495		E_{RX}	—	±1.5	—	
$-10 < V_Y < +10$ ($V_X = \pm 10$ V)			E_{RY}	—	±3.0	—	
$T_A = -55°$ to $+125°C$	MC1595						
$-10 < V_X < +10$ ($V_Y = \pm 10$ V)			E_{RX}	—	±0.75	—	
$-10 < V_Y < +10$ ($V_X = \pm 10$ V)			E_{RY}	—	±1.5	—	
Square Mode Error (Accuracy in percent of full scale after Offset and Scale Factor adjustment)		5	E_{SQ}				%
$T_A = +25°C$	MC1495			—	±0.75	—	
	MC1595			—	±0.5	—	
$T_A = 0°$ to $+70°C$	MC1495			—	±1.0	—	
$T_A = -55°$ to $+125°C$	MC1595			—	±0.75	—	
Scale Factor (Adjustable) $\left(K = \frac{2R_L}{I_3 R_X R_Y}\right)$		—	K	—	0.1	—	
Input Resistance	MC1495	7	R_{inX}	—	30	—	MΩ
($f = 20$ Hz)	MC1595			—	35	—	
	MC1495		R_{inY}	—	20	—	
	MC1595			—	35	—	
Differential Output Resistance ($f = 20$ Hz)		8	R_O	—	300	—	kΩ
Input Bias Current		6					μA
$I_{bx} = \frac{(I_9 + I_{12})}{2}$, $I_{by} = \frac{(I_4 + I_8)}{2}$	MC1495		I_{bx}	—	2.0	12	
	MC1595			—	2.0	8.0	
	MC1495		I_{by}	—	2.0	12	
	MC1595			—	2.0	8.0	
Input Offset Current		6					μA
$\lvert I_9 - I_{12}\rvert$	MC1495		$\lvert I_{iox}\rvert$	—	0.4	2.0	
	MC1595			—	0.2	1.0	
$\lvert I_4 - I_8\rvert$	MC1495		$\lvert I_{ioy}\rvert$	—	0.4	2.0	
	MC1595			—	0.2	1.0	
Average Temperature Coefficient of Input Offset Current		6	$\lvert TC_{Iio}\rvert$				nA/°C
($T_A = 0°$ to $+70°C$)	MC1495			—	2.5	—	
($T_A = -55°$ to $+125°C$	MC1595			—	2.5		
Output Offset Current	MC1495	6	$\lvert I_{OO}\rvert$		20	100	μA
$\lvert I_{14} - I_2\rvert$	MC1595			—	10	50	
Average Temperature Coefficient of Output Offset Current		6	$\lvert TC_{IOO}\rvert$				nA/°C
($T_A = 0°$ to $+70°C$)	MC1495			—	20	—	
($T_A = -55°$ to $+125°C$)	MC1595			—	20	—	
Frequency Response		9,10					
3.0 dB Bandwidth, $R_L = 11$ kΩ			$BW_{(3dB)}$	—	3.0	—	MHz
3.0 dB Bandwidth, $R_L = 50$ Ω (Transconductance Bandwidth)			$T_{BW(3dB)}$	—	80	—	MHz
3° Relative Phase Shift Between V_X and V_Y			f_ϕ	—	750	—	kHz
1% Absolute Error Due to Input-Output Phase Shift			f_θ	—	30	—	kHz
Common Mode Input Swing	MC1495	11	CMV	±10.5	±12	—	Vdc
(Either Input)	MC1595			±11.5	±13	—	
Common Mode Gain	MC1495	11	A_{CM}	–40	–50	—	dB
(Either Input)	MC1595			–50	–60	—	
Common Mode Quiescent		12	V_{O1}	—	21	—	Vdc
Output Voltage			V_{O2}	—	21	—	
Differential Output Voltage Swing Capability		9	V_O	—	±14	—	V_{pk}
Power Supply Sensitivity		12	S^+	—	5.0	—	mV/V
			S^-	—	10	—	
Power Supply Current		12	I_7	—	6.0	7.0	mA
DC Power Dissipation		12	P_D	—	135	170	mW

MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Applied Voltage (V_2–V_1, V_{14}–V_1, V_1–V_9, V_1–V_{12}, V_1–V_4, V_1–V_8, V_{12}–V_7, V_9–V_7, V_8–V_7, V_4–V_7)	ΔV	30	Vdc
Differential Input Signal	V_{12}–V_9 V_4–V_8	±(6+I_{13} R_X) ±(6+I_3 R_Y)	Vdc
Maximum Bias Current	I_3 I_{13}	10 10	mA
Power Dissipation (Package Limitation) D Suffix, Plastic Package Derate above T_A = +25°C J Suffix, Ceramic Package Derate above T_A = +25°C	 P_D P_D 	 862 145 750 5.0	 mW mW/°C mW °C/W
Operating Temperature Range MC1495 MC1595	T_A	 0 to +70 –55 to +125	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

Figure 4. Linearity (Using Null Technique)

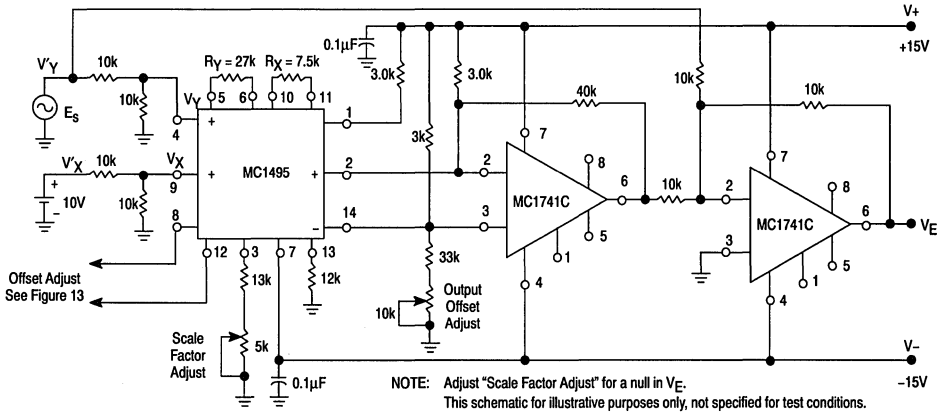

Figure 5. Linearity (Using X-Y Plotter Technique)

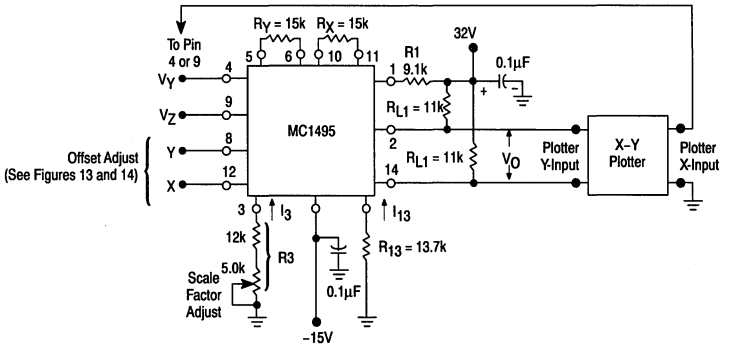

Figure 6. Input and Output Current

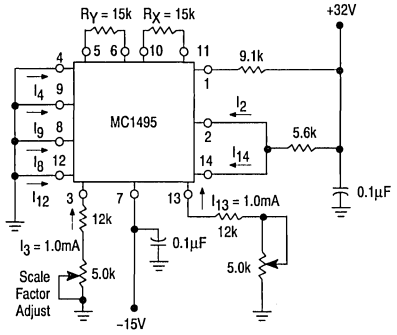

Figure 7. Input Resistance

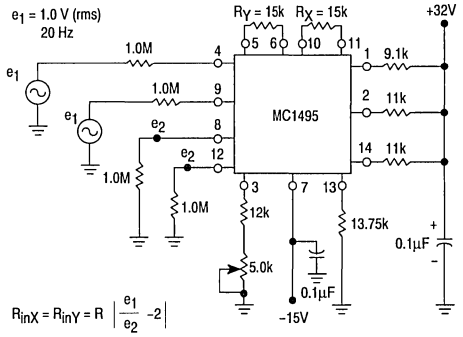

Figure 8. Output Resistance

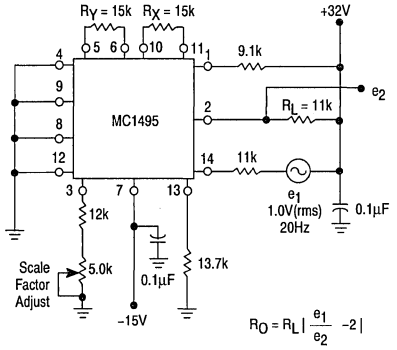

Figure 9. Bandwidth (R_L = 11kΩ)

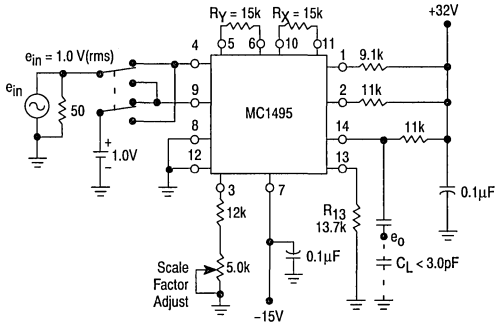

Figure 10. Bandwidth (R_L = 50 Ω)

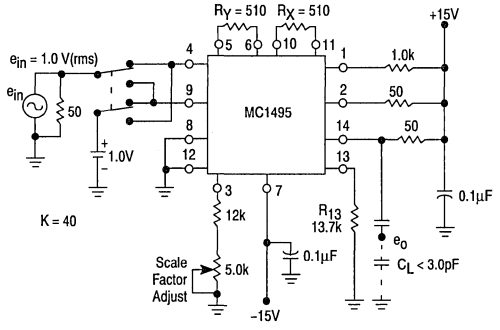

Figure 11. Common Mode Gain and Common Mode Input Swing

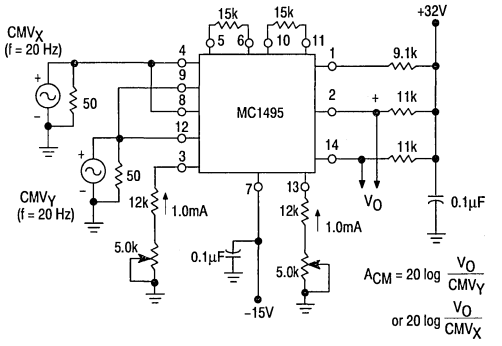

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Figure 12. Power Supply Sensitivity

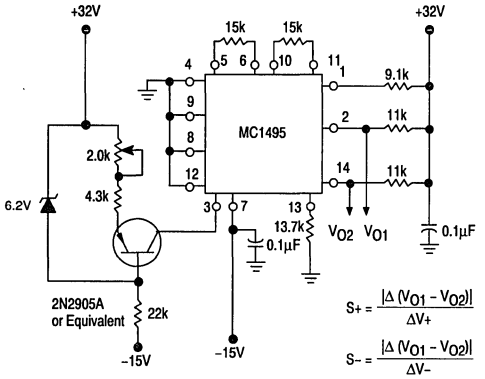
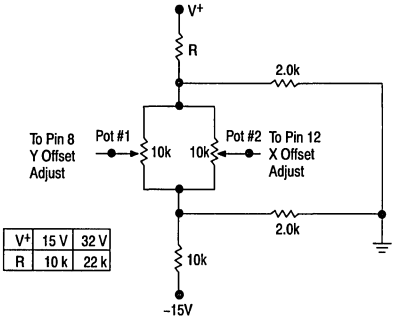
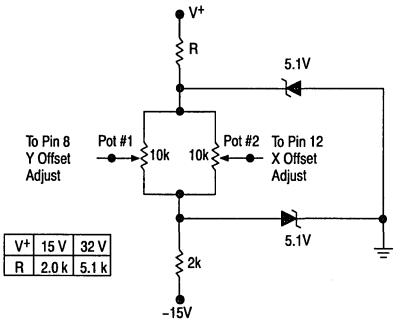


Figure 13. Offset Adjust Circuit



V+	15 V	32 V
R	10 k	22 k

Figure 14. Offset Adjust Circuit (Alternate)



V+	15 V	32 V
R	2.0 k	5.1 k

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Figure 15. Linearity versus Temperature

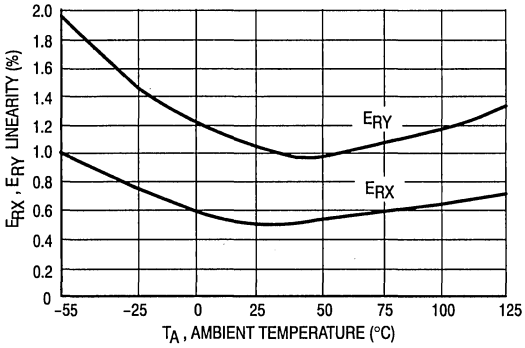


Figure 16. Scale Factor versus Temperature

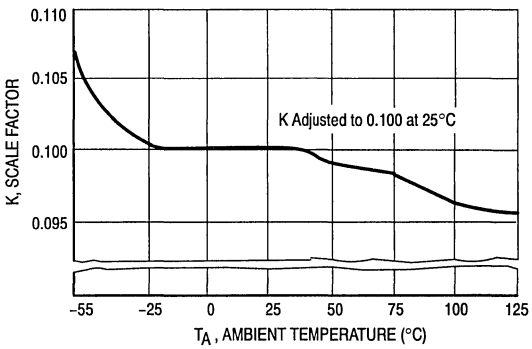


Figure 17. Error Contributed by Input Differential Amplifier

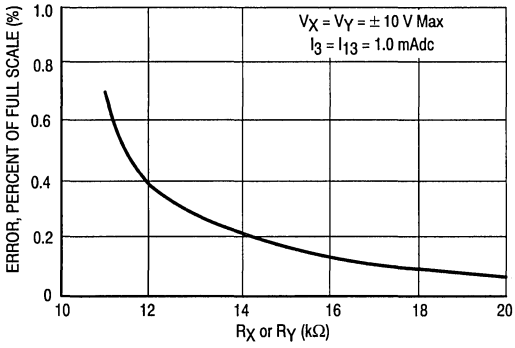


Figure 18. Error Contributed by Input Differential Amplifier

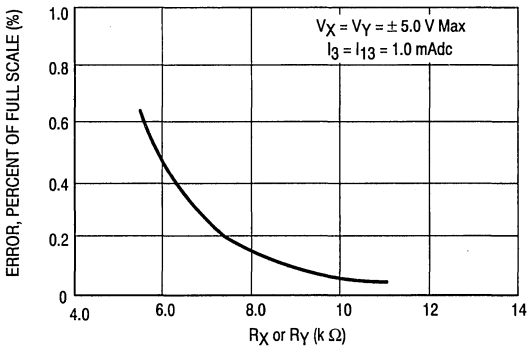
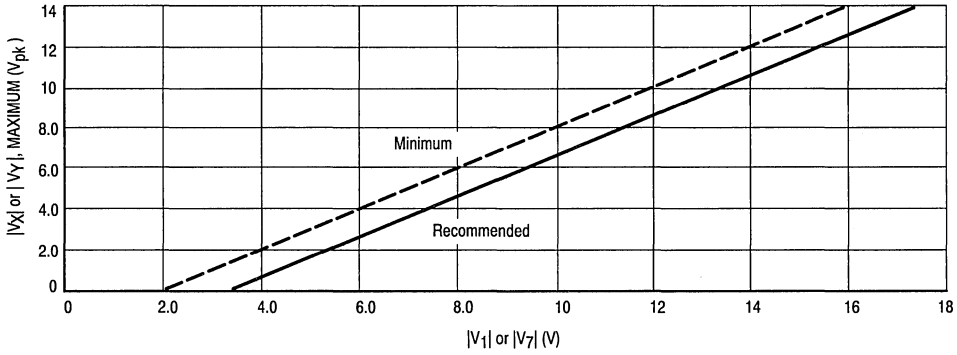


Figure 19. Maximum Allowable Input Voltage versus Voltage at Pin 1 or Pin 7



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OPERATION AND APPLICATIONS INFORMATION

THEORY OF OPERATION

The MC1495 is a monolithic, four-quadrant multiplier which operates on the principle of variable transconductance. A detailed theory of operation is covered in Application Note AN489, *Analysis and Basic Operation of the MC1595*. The result of this analysis is that the differential output current of the multiplier is given by:

$$I_A - I_B = \Delta I = \frac{2V_X V_Y}{R_X R_Y I_3}$$

where, I_A and I_B are the currents into Pins 14 and 2, respectively, and V_X and V_Y are the X and Y input voltages at the multiplier input terminals.

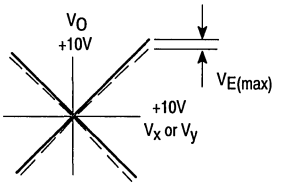
DESIGN CONSIDERATIONS

General

The MC1495 permits the designer to tailor the multiplier to a specific application by proper selection of external components. External components may be selected to optimize a given parameter (e.g. bandwidth) which may in turn restrict another parameter (e.g. maximum output voltage swing). Each important parameter is discussed in detail in the following paragraphs.

Linearity, Output Error, E_{RX} or E_{RY}

Linearity error is defined as the maximum deviation of output voltage from a straight line transfer function. It is expressed as error in percent of full scale (see figure below).



For example, if the maximum deviation, $V_{E(max)}$, is ±100 mV and the full scale output is 10 V, then the percentage error is:

$$E_R = \frac{V_{E(max)}}{V_{O(max)}} \bullet 100 = \frac{100 \bullet 10^{-3}}{10} \bullet 100 = \pm 1.0\%.$$

Linearity error may be measured by either of the following methods:

1. Using an X-Y plotter with the circuit shown in Figure 5, obtain plots for X and Y similar to the one shown above.
2. Use the circuit of Figure 4. This method nulls the level shifted output of the multiplier with the original input. The peak output of the null operational amplifier will be equal to the error voltage, $V_{E\ (max)}$.

One source of linearity error can arise from large signal nonlinearity in the X and Y input differential amplifiers. To avoid introducing error from this source, the emitter degeneration resistors R_X and R_Y must be chosen large enough so that nonlinear base-emitter voltage variation can be ignored. Figures 17 and 18 show the error expected from this source as a function of the values of R_X and R_Y with an operating current of 1.0 mA in each side of the differential amplifiers (i.e., $I_3 = I_{13}$ = 1.0 mA).

3 dB Bandwidth and Phase Shift

Bandwidth is primarily determined by the load resistors and the stray multiplier output capacitance and/or the operational amplifier used to level shift the output. If wideband operation is desired, low value load resistors and/or a wideband operational amplifier should be used. Stray output capacitance will depend to a large extent on circuit layout.

Phase shift in the multiplier circuit results from two sources: phase shift common to both X and Y channels (due to the load resistor-output capacitance pole mentioned above) and relative phase shift between X and Y channels (due to differences in transadmittance in the X and Y channels). If the input to output phase shift is only 0.6°, the output product of two sine waves will exhibit a vector error of 1%. A 3° relative phase shift between V_X and V_Y results in a vector error of 5%.

Maximum Input Voltage

$V_{X(max)}$, $V_{Y(max)}$ input voltages must be such that:

$$V_{X(max)} < I_{13} R_Y$$

$$V_{Y(max)} < I_3 R_Y$$

Exceeding this value will drive one side of the input amplifier to "cutoff" and cause nonlinear operation.

Current I_3 and I_{13} are chosen at a convenient value (observing power dissipation limitation) between 0.5 mA and 2.0 mA, approximately 1.0 mA. Then R_X and R_Y can be determined by considering the input signal handling requirements.

For $V_{X(max)} = V_{Y(max)} = 10$ V;

$$R_X = R_Y > \frac{10\ V}{1.0\ mA} = 10\ k\Omega.$$

The equation $I_A - I_B = \dfrac{2V_X V_Y}{R_X R_Y I_3}$

is derived from $I_A - I_B = \dfrac{2V_X V_Y}{(R_X + \frac{2kT}{qI_{13}})(R_Y + \frac{2kT}{qI_3}) I_3}$

with the assumption $R_X >> \dfrac{2kT}{qI_{13}}$ and $R_Y >> \dfrac{2kT}{qI_3}$.

At T_A = +25°C and $I_{13} = I_3$ = 1.0 mA,

$$\frac{2kT}{qI_{13}} = \frac{2kT}{qI_3} = 52\ \Omega.$$

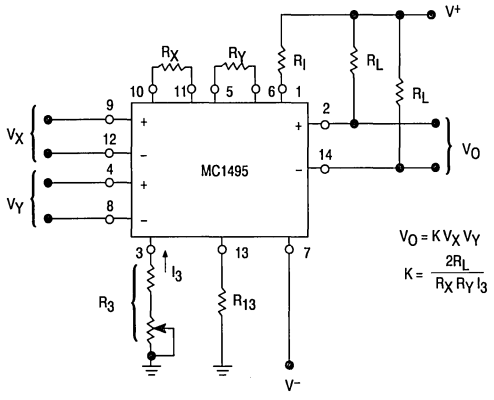
Therefore, with $R_X = R_Y$ = 10 kΩ the above assumption is valid. Reference to Figure 19 will indicate limitations of $V_{X(max)}$ or $V_{Y(max)}$ due to V_1 and V_7. Exceeding these limits will cause saturation or "cutoff" of the input transistors. See Step 4 of General Design Procedure for further details.

Maximum Output Voltage Swing

The maximum output voltage swing is dependent upon the factors mentioned below and upon the particular circuit being considered.

For Figure 20 the maximum output swing is dependent upon V+ for positive swing and upon the voltage at Pin 1 for negative swing. The potential at Pin 1 determines the quiescent level for transistors Q_5, Q_6, Q_7 and Q_8. This potential should be related so that negative swing at Pins 2 or 14 does not saturate those transistors. See General Design Procedure for further information regarding selection of these potentials.

Figure 20. Basic Multiplier



If an operational amplifier is used for level shift, as shown in Figure 21, the output swing (of the multiplier) is greatly reduced. See Section 3 for further details.

GENERAL DESIGN PROCEDURE

Selection of component values is best demonstrated by the following example. Assume resistive dividers are used at the X and Y-inputs to limit the maximum multiplier input to ± 5.0 V [$V_X = V_{Y(max)}$] for a ± 10 V input [$V_{X'} = V_{Y'(max)}$] (see Figure 21). If an overall scale factor of 1/10 is desired,

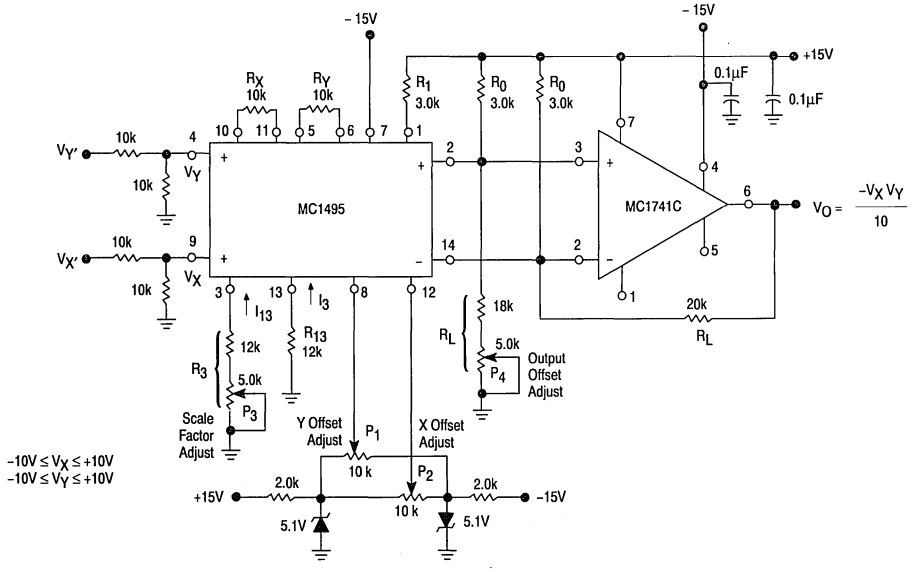
$$\text{then, } V_O = \frac{V_{X'} V_{Y'}}{10} = \frac{(2V_X)(2V_Y)}{10} = 4/10\ V_X V_Y$$

Therefore, K = 4/10 for the multiplier (excluding the divider network).

Step 1. The fist step is to select current I_3 and current I_{13}. There are no restrictions on the selection of either of these currents except the power dissipation of the device. I_3 and I_{13} will normally be 1.0 mA or 2.0 mA. Further, I_3 does not have to be equal to I_{13}, and there is normally no need to make them different. For this example, let

$$I_3 = I_{13} = 1.0\ \text{mA}.$$

Figure 21. Multiplier with Operational Amplifier Level Shift



To set currents I_3 and I_{13} to the desired value, it is only necessary to connect a resistor between Pin 13 and ground, and between Pin 3 and ground. From the schematic shown in Figure 3, it can be seen that the resistor values necessary are given by:

$$R_{13} + 500\ \Omega = \frac{|V-| - 0.7\ V}{I_{13}}$$

$$R_3 + 500\ \Omega = \frac{|V-| - 0.7\ V}{I_3}$$

Let V– = –15 V, then $R_{13} + 500 = \frac{14.3\ V}{1.0\ mA}$ or $R_{13} = 13.8\ k\Omega$

Let $R_{13} = 12\ k\Omega$. Similarly, $R_3 = 13.8\ k\Omega$, let $R_3 = 15\ k\Omega$

However, for applications which require an accurate scale factor, the adjustment of R_3 and consequently, I_3, offers a convenient method of making a final trim of the scale factor. For this reason, as shown in Figure 21, resistor R_3 is shown as a fixed resistor in series with a potentiometer.

For applications not requiring an exact scale factor (balanced modulator, frequency doubler, AGC amplifier, etc.) Pins 3 and 13 can be connected together and a single resistor from Pin 3 to ground can be used. In this case, the single resistor would have a value of 1/2 the above calculated value for R_{13}.

Step 2. The next step is to select R_X and R_Y. To insure that the input transistors will always be active, the following conditions should be met:

$$\frac{V_X}{R_X} < I_{13}, \qquad \frac{V_Y}{R_Y} < I_3$$

A good rule of thumb is to make $I_3R_Y \geq 1.5\ V_{Y(max)}$ and $I_{13}R_X \geq 1.5 V_{X(max)}$. The larger the I_3R_Y and $I_{13}R_X$ product in relation to V_Y and V_X respectively, the more accurate the multiplier will be (see Figures 17 and 18).

Let $R_X = R_Y = 10\ k\Omega$,

then $I_3R_Y = 10\ V$

$I_{13}R_X = 10\ V$

since $V_{X(max)} = V_{Y(max)} = 5.0\ V$, the value of R_X=R_Y=10 kΩ is sufficient.

Step 3. Now that R_X, R_Y and I_3 have been chosen, R_L can be determined:

$$K = \frac{2R_L}{R_X R_Y I_3} = \frac{4}{10}, \text{ or } \frac{(2)(R_L)}{(10\ k)(10\ k)(1.0\ mA)} = \frac{4}{10}$$

Thus $R_L = 20\ k\Omega$.

Step 4. To determine what power supply voltage is necessary for this application, attention must be given to the circuit schematic shown in Figure 3. From the circuit schematic it can be seen that in order to maintain transistors Q_1, Q_2, Q_3 and Q_4 in an active region when the maximum input voltages are applied ($V_{X'} = V_{Y'} = 10\ V$ or $V_X = 5.0\ V$, $V_Y = 5.0\ V$), their respective collector voltage should be at least a few tenths of a volt higher than the maximum input voltage. It should also be noticed that the collector voltage of transistors Q_3 and Q_4 is at a potential which is two diode-drops below the voltage at Pin 1. Thus, the voltage at Pin 1 should be about 2.0 V higher than the maximum input voltage. Therefore, to handle +5.0 V at the inputs, the voltage at Pin 1 must be at least +7.0 V. Let $V_1 = 9.0$ Vdc.

Since the current flowing into Pin 1 is always equal to $2I_3$, the voltage at Pin 1 can be set by placing a resistor (R_1) from Pin 1 to the positive supply:

$$R_1 = \frac{V+ - V_1}{2I_3}$$

Let V+ = 15 V, then $R_1 = \frac{15\ V - 9.0\ V}{(2)(1.0\ mA)}$

$$R_1 = 3.0\ k\Omega.$$

Note that the voltage at the base of transistors Q_5, Q_6, Q_7 and Q_8 is one diode-drop below the voltage at Pin 1. Thus, in order that these transistors stay active, the voltage at Pins 2 and 14 should be approximately halfway between the voltage at Pin 1 and the positive supply voltage. For this example, the voltage at Pins 2 and 14 should be approximately 11 V.

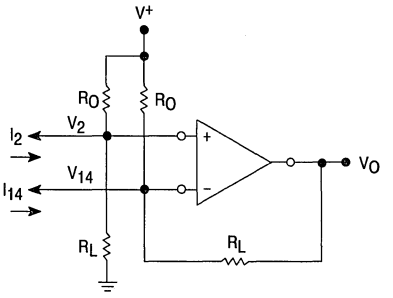
Step 5. For DC applications, such as the multiply, divide and square-root functions, it is usually desirable to convert the differential output to a single-ended output voltage referenced to ground. The circuit shown in Figure 22 performs this function. It can be shown that the output voltage of this circuit is given by:

$$V_O = (I_2 - I_{14})\ R_L$$

And since $I_A - I_B = I_2 - I_{14} = \frac{2I_X I_Y}{I_3} = \frac{2V_XV_Y}{I_3R_XR_Y}$

then $V_O = \frac{2R_L V_{X'} V_{Y'}}{4R_X R_X I_3}$ where, $V_{X'}$ $V_{Y'}$ is the voltage at the input to the voltage dividers.

Figure 22. Level Shift Circuit



The choice of an operational amplifier for this application should have low bias currents, low offset current, and a high common mode input voltage range as well as a high common mode rejection ratio. The MC1456, and MC1741C operational amplifiers meet these requirements.

Referring to Figure 21, the level shift components will be determined. When $V_X = V_Y = 0$, the currents I_2 and I_{14} will be equal to I_{13}. In Step 3, R_L was found to be 20 kΩ and in Step 4, V_2 and V_{14} were found to be approximately 11 V. From this information R_O can be found easily from the following equation (neglecting the operational amplifiers bias current):

$$\frac{V2}{R_L} + I_{13} = \frac{V^+ - V_2}{R_O}$$

And for this example, $\frac{11\ V}{20\ k\Omega} + 1.0\ mA = \frac{15\ V - 11\ V}{R_O}$

Solving for R_O: $R_O = 2.6\ k\Omega$, thus, select $R_O = 3.0\ k\Omega$

For $R_O = 3.0\ k\Omega$, the voltage at Pins 2 and 14 is calculated to be:

$$V_2 = V_{14} = 10.4\ V.$$

The linearity of this circuit (Figure 21) is likely to be as good or better than the circuit of Figure 5. Further improvements are possible as shown in Figure 23 where R_Y has been increased substantially to improve the Y linearity, and R_X decreased somewhat so as not to materially affect the X linearity. This avoids increasing R_L significantly in order to maintain a K of 0.1.

The versatility of the MC1495 allows the user to to optimize its performance for various input and output signal levels.

OFFSET AND SCALE FACTOR ADJUSTMENT

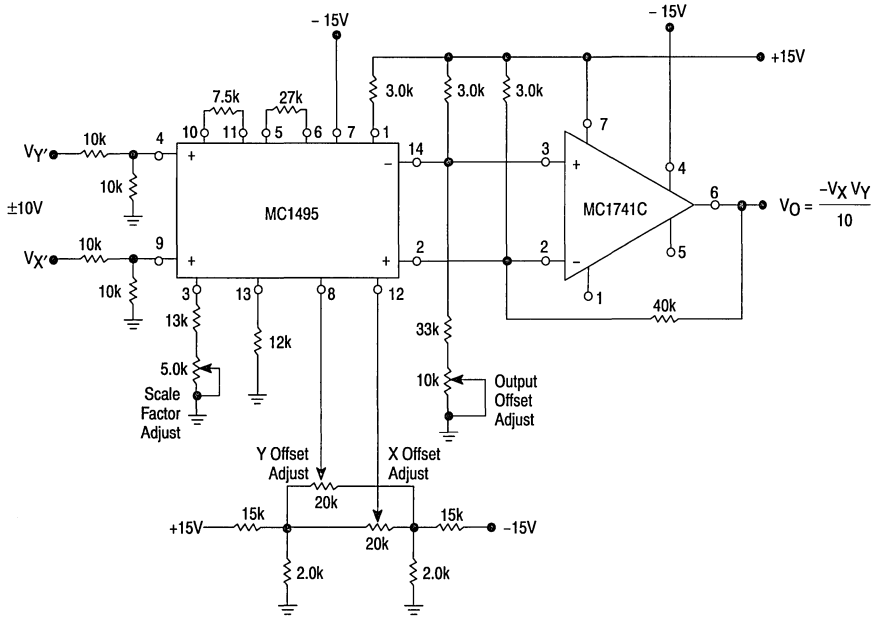
Offset Voltages

Within the monolithic multiplier (Figure 3) transistor base-emitter junctions are typically matched within 1.0 mV and resistors are typically matched within 2%. Even with this careful matching, an output error can occur. This output error is comprised of X-input offset voltage, Y-input offset voltage, and output offset voltage. These errors can be adjusted to zero with the techniques shown in Figure 21. Offset terms can be shown analytically by the transfer function:

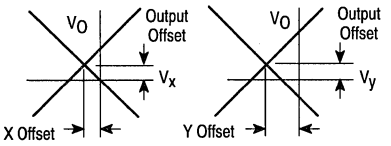
$$V_O = K[V_x \pm V_{iox} \pm V_{x(off)}]\,[V_y \pm V_{ioy} \pm V_{y(off)}] \pm V_{OO} \quad (1)$$

Where:
- K = scale factor
- V_x = "x" input voltage
- V_y = "y" input voltage
- V_{iox} = "x" input offset voltage
- V_{ioy} = "y" input offset voltage
- $V_{x(off)}$ = "x" input offset adjust voltage
- $V_{y(off)}$ = "y" input offset adjust voltage
- V_{OO} = output offset voltage.

Figure 23. Multiplier with Improved Linearity



X, Y and Output Offset Voltages



For most DC applications, all three offset adjust potentiometers (P_1, P_2, P_4) will be necessary. One or more offset adjust potentiometers can be eliminated for AC applications (see Figures 28, 29, 30, 31).

If well regulated supply voltages are available, the offset adjust circuit of Figure 13 is recommended. Otherwise, the circuit of Figure 14 will greatly reduce the sensitivity to power supply changes.

Scale Factor

The scale factor K is set by P_3 (Figure 21). P_3 varies I_3 which inversely controls the scale factor K. It should be noted that current I_3 is one-half the current through R_1. R_1 sets the bias level for Q_5, Q_6, Q_7, and Q_8 (see Figure 3). Therefore, to be sure that these devices remain active under all conditions of input and output swing, care should be exercised in adjusting P_3 over wide voltage ranges (see General Design Procedure).

Adjustment Procedures

The following adjustment procedure should be used to null the offsets and set the scale factor for the multiply mode of operation, (see Figure 21).

1. X-Input Offset
   (a) Connect oscillator (1.0 kHz, 5.0 V_{p-p} sinewave) to the Y-input (Pin 4).
   (b) Connect X-input (Pin 9) to ground.
   (c) Adjust X offset potentiometer (P_2) for an AC null at the output.
2. Y-Input Offset
   (a) Connect oscillator (1.0 kHz, 5.0 Vp-p sinewave) to the X-input (Pin 9).
   (b) Connect Y-input (Pin 4) to ground.
   (c) Adjust Y offset potentiometer (P_1) for an AC null at the output.
3. Output Offset
   (a) Connect both X and Y-inputs to ground.
   (b) Adjust output offset potentiometer (P_4) until the output voltage (V_O) is 0 Vdc.
4. Scale Factor
   (a) Apply +10 Vdc to both the X and Y-inputs.
   (b) Adjust P_3 to achieve + 10 V at the output.
5. Repeat steps 1 through 4 as necessary.

The ability to accurately adjust the MC1495 depends upon the characteristics of potentiometers P_1 through P_4. Multi-turn, infinite resolution potentiometers with low temperature coefficients are recommended.

DC APPLICATIONS

Multiply

The circuit shown in Figure 21 may be used to multiply signals from DC to 100 kHz. Input levels to the actual multiplier are 5.0 V (max). With resistive voltage dividers the maximum could be very large however, for this application two-to-one dividers have been used so that the maximum input level is 10 V. The maximum output level has also been designed for 10 V (max).

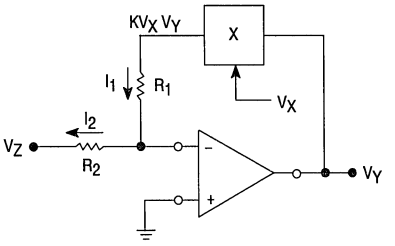
Squaring Circuit

If the two inputs are tied together, the resultant function is squaring; that is $V_O = KV^2$ where K is the scale factor. Note that all error terms can be eliminated with only three adjustment potentiometers, thus eliminating one of the input offset adjustments. Procedures for nulling with adjustments are given as follows:

A. AC Procedure:
   1. Connect oscillator (1.0 kHz, 15 Vp-p) to input.
   2. Monitor output at 2.0 kHz with tuned voltmeter and adjust P_3 for desired gain. (Be sure to peak response of the voltmeter.)
   3. Tune voltmeter to 1.0 kHz and adjust P_1 for a minimum output voltage.
   4. Ground input and adjust P_4 (output offset) for 0 Vdc output.
   5. Repeat steps 1 through 4 as necessary.

B. DC Procedure:
   1. Set $V_X = V_Y = 0$ V and adjust P_4 (output offset potentiometer) such that $V_O = 0$ Vdc
   2. Set $V_X = V_Y = 1.0$ V and adjust P_1 (Y-input offset potentiometer) such that the output voltage is + 0.100 V.
   3. Set $V_X = V_Y = 10$ Vdc and adjust P_3 such that the output voltage is + 10 V.
   4. Set $V_X = V_Y = -10$ Vdc. Repeat steps 1 through 3 as necessary.

Figure 24. Basic Divide Circuit



Divide Circuit

Consider the circuit shown in Figure 24 in which the multiplier is placed in the feedback path of an operational amplifier. For this configuration, the operational amplifier will maintain a "virtual ground" at the inverting (–) input. Assuming that the bias current of the operational amplifier is negligible, then $I_1 = I_2$ and,

$$\frac{KV_XV_Y}{R1} = \frac{-V_Z}{R2} \quad (1)$$

Solving for V_Y, $$V_Y = \frac{-R1}{R2\,K}\frac{V_Z}{V_X} \quad (2)$$

If R1=R2, $$V_Y = \frac{-V_Z}{KV_X} \quad (3)$$

If R1= KR2, $$V_Y = \frac{-V_Z}{V_X} \quad (4)$$

Hence, the output voltage is the ratio of V_Z to V_X and provides a divide function. This analysis is, of course, the ideal condition. If the multiplier error is taken into account, the output voltage is found to be:

$$V_Y = -\left[\frac{R1}{R2\,K}\right]\frac{V_Z}{V_X} + \frac{\Delta E}{KV_X} \quad (5)$$

where ΔE is the error voltage at the output of the multiplier. From this equation, it is seen that divide accuracy is strongly dependent upon the accuracy at which the multiplier can be set, particularly at small values of V_Y. For example, assume that R1 = R2, and K = 1/10. For these conditions the output of the divide circuit is given by:

$$V_Y = \frac{-10\,V_Z}{V_X} + \frac{10\,\Delta E}{V_X} \quad (6)$$

From Equation 6, it is seen that only when $V_X = 10$ V is the error voltage of the divide circuit as low as the error of the multiply circuit. For example, when V_X is small, (0.1 V) the error voltage of the divide circuit can be expected to be a hundred times the error of the basic multiplier circuit.

In terms of percentage error,

$$\text{percentage error} = \frac{\text{error}}{\text{actual}} \times 100\%$$

or from Equation (5),

$$PE_D = \frac{\frac{\Delta E}{KV_X}}{\left[\frac{R1}{R2\,K}\right]\frac{V_Z}{V_X}} = \left[\frac{R2}{R1}\right]\frac{\Delta E}{V_Z} \quad (7)$$

From Equation 7, the percentage error is inversely related to voltage V_Z (i.e., for increasing values of V_Z, the percentage error decreases).

A circuit that performs the divide function is shown in Figure 25.

Two things should be emphasized concerning Figure 25.

1. The input voltage ($V_{X'}$) must be greater than zero and must be positive. This insures that the current out of Pin 2 of the multiplier will always be in a direction compatible with the polarity of V_Z.
2. Pin 2 and 14 of the multiplier have been interchanged in respect to the operational amplifiers input terminals. In this instance, Figure 25 differs from the circuit connection shown in Figure 21; necessitated to insure negative feedback around the loop.

A suggested adjustment procedure for the divide circuit.

1. Set $V_Z = 0$ V and adjust the output offset potentiometer (P_4) until the output voltage (V_O) remains at some (not necessarily zero) constant value as $V_{X'}$ is varied between +1.0 V and +10 V.
2. Keep V_Z at 0 V, set $V_{X'}$ at +10 V and adjust the Y input offset potentiometer (P_1) until $V_O = 0$ V.
3. Let $V_{X'} = V_Z$ and adjust the X-input offset potentiometer (P_2) until the output voltage remains at some (not necessarily – 10 V) constant value as $V_Z = V_{X'}$ is varied between +1.0 and +10 V.
4. Keep $V_{X'} = V_Z$ and adjust the scale factor potentiometer (P_3) until the average value of V_O is –10 V as $V_Z = V_{X'}$ is varied between +1.0 V and +10 V.
5. Repeat steps 1 through 4 as necessary to achieve optimum performance.

Figure 25. Divide Circuit

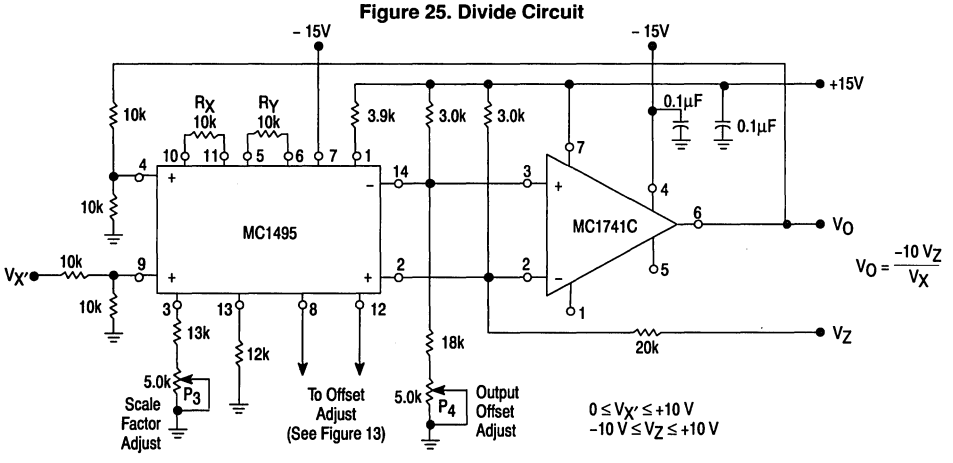
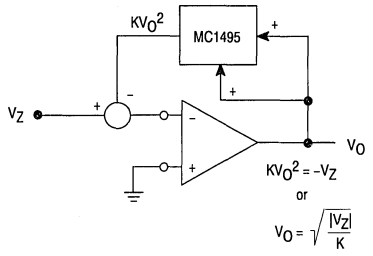


Figure 26. Basic Square Root Circuit



Square Root

A special case of the divide circuit in which the two inputs to the multiplier are connected together is the square root function as indicated in Figure 26. This circuit may suffer from latch-up problems similar to those of the divide circuit. Note that only one polarity of input is allowed and diode clamping (see Figure 27) protects against accidental latch-up.

This circuit also may be adjusted in the closed-loop mode as follows:

1. Set V_Z to –0.01 V and adjust P_4 (output offset) for V_O = +0.316 V, being careful to approach the output from the positive side to preclude the effect of the output diode clamping.
2. Set V_Z to –0.9 V and adjust P_2 (X adjust) for V_O = +3.0 V.
3. Set V_Z to –10 V and adjust P_3 (scale factor adjust) for V_O = +10 V.
4. Steps 1 through 3 may be repeated as necessary to achieve desired accuracy.

AC APPLICATIONS

The applications that follow demonstrate the versatility of the monolithic multiplier. If a potted multiplier is used for these cases, the results generally would not be as good because the potted units have circuits that, although they optimize DC multiplication operation, can hinder AC applications.

Frequency doubling often is done with a diode where the fundamental plus a series of harmonics are generated. However, extensive filtering is required to obtain the desired harmonic, and the second harmonic obtained under this technique usually is small in magnitude and requires amplification.

When a multiplier is used to double frequency the second harmonic is obtained directly, except for a DC term, which can be removed with AC coupling.

$$e_o = KE^2 \cos^2 \omega t$$

$$e_o = \frac{KE^2}{2} (1 + \cos 2\omega t).$$

A potted multiplier can be used to obtain the double frequency component, but frequency would be limited by its internal level-shift amplifiifer. In the monolithic units, the amplifier is omitted.

In a typical doubler circuit, conventional ± 15 V supplies are used. An input dynamic range of 5.0 V peak-to-peak is allowed. The circuit generates wave-forms that are double frequency; less than 1% distortion is encountered without filtering. The configuration has been successfully used in excess of 200 kHz; reducing the scale factor by decreasing the load resistors can further expand the bandwidth.

Figure 29 represents an application for the monolithic multiplier as a balanced modulator. Here, the audio input signal is 1.6 kHz and the carrier is 40 kHz.

Figure 27. Square Root Circuit

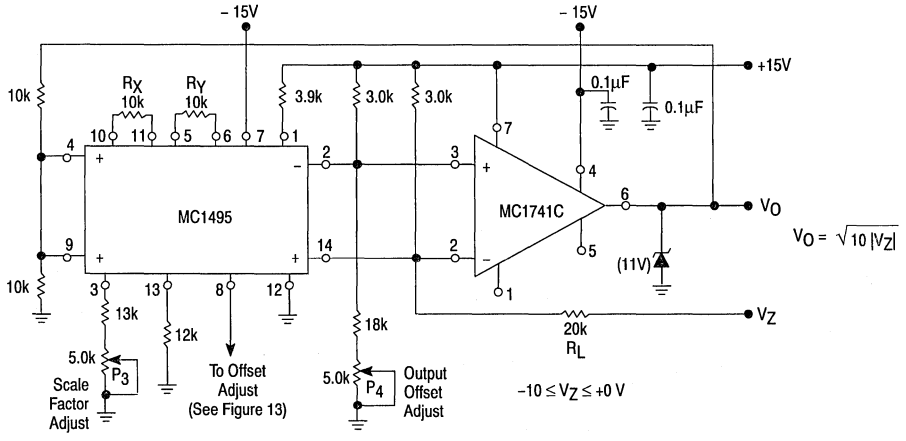
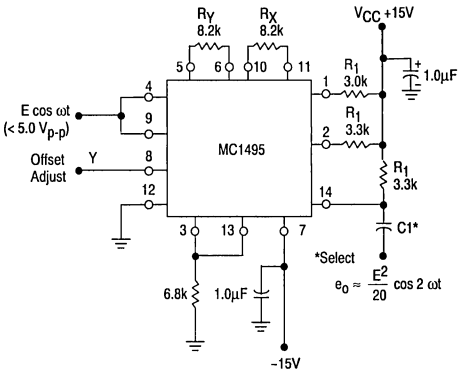


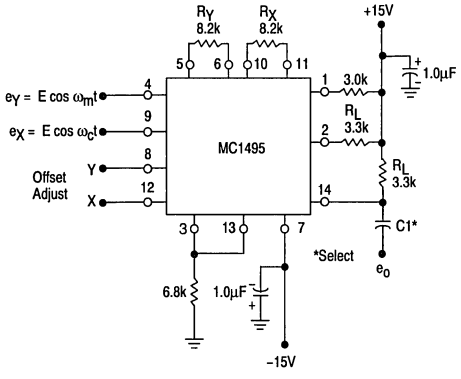
Figure 28. Frequency Doubler



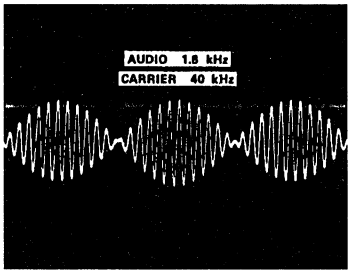
When two equal cosine waves are applied to X and Y, the result is a wave shape of twice the input frequency. For this example the input was a 10 kHz signal, output was 20 kHz.

Figure 29. Balanced Modulator

(A)



(B)



The defining equation for balanced modulation is

$$K(E_m \cos \omega_m t)(E_c \cos \omega_c t) =$$

$$\frac{KE_c E_m}{2}\left[\cos(\omega_c + \omega_m)t + \cos(\omega_c - \omega_m)t\right]$$

where ω_c is the carrier frequency, ω_m is the modulator frequency and K is the multiplier gain constant.

AC coupling at the output eliminates the need for level translation or an operational amplifier; a higher operating frequency results.

A problem common to communications is to extract the intelligence from single-sideband received signal. The ssb signal is of the form:

$$e_{ssb} = A \cos(\omega_c + \omega_m)t$$

and if multiplied by the appropriate carrier waveform, cos $\omega_c t$,

$$e_{ssb}e_{carrier} = \frac{AK}{2}\left[\cos(2\omega_c + \omega_m)t + \cos(\omega_c)t\right].$$

If the frequency of the band-limited carrier signal (ω_c) is ascertained in advance, the designer can insert a low pass filter and obtain the (AK/2) ($\cos\omega_c t$) term with ease. He/she also can use an operational amplifier for a combination level shift-active filter, as an external component. But in potted multipliers, even if the frequency range can be covered, the operational amplifier is inside and not accessible, so the user must accept the level shifting provided, and still add a low pass filter.

Amplitude Modulation

The multiplier performs amplitude modulation, similar to balanced modulating, when a DC term is added to the modulating signal with the Y-offset adjust potentiometer (see Figure 30).

Here, the identity is:

$$E_m(1 + m \cos \omega_m t)\, E_c \cos \omega_c t = KE_m E_c \cos \omega_c t +$$

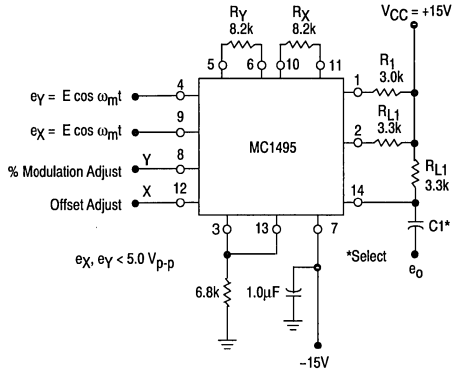
$$\frac{KE_m E_c m}{2}\left[\cos(\omega_c + \omega_m)t + \cos(\omega_c - \omega_m)t\right]$$

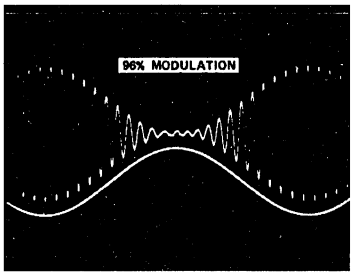
where m indicates the degrees of modulation. Since m is adjustable, via potentiometer P_1, 100% modulation is possible. Without extensive tweaking, 96% modulation may be obtained where ω_c and ω_m are the same as in the balanced modulator example.

Linear Gain Control

To obtain linear gain control, the designer can feed to one of the two MC1495 inputs a signal that will vary the unit's gain. The following example demonstrates the feasibility of this application. Suppose a 200 kHz sinewave, 1.0 V peak-to-peak, is the signal to which a gain control will be added. The dynamic range of the control voltage V_C is 0 V to +1.0 V. These must be ascertained and the proper values of R_X and R_Y can be selected for optimum performance. For the 200 kHz operating frequency, load resistors of 100 Ω were chosen to broaden the operating bandwidth of the multiplier, but gain was sacrificed. It may be made up with an amplifier operating at the appropriate frequency (see Figure 31).

Figure 30. Amplitude Modulation





The signal is applied to the unit's Y-input. Since the total input range is limited to 1.0 V_{p-p}, a 2.0 V swing, a current source of 2.0 mA and an R_Y value of 1.0 kΩ is chosen. This takes best advantage of the dynamic range and insures linear operation in the Y-channel.

Since the X-input varies between 0 and +1.0 V, the current source selected was 1.0 mA, and the R_X value chosen was 2.0 kΩ. This also insures linear operation over the X-input dynamic range. Choosing R_L = 100 assures wide bandwidth operation.

Hence, the scale factor for this configuration is:

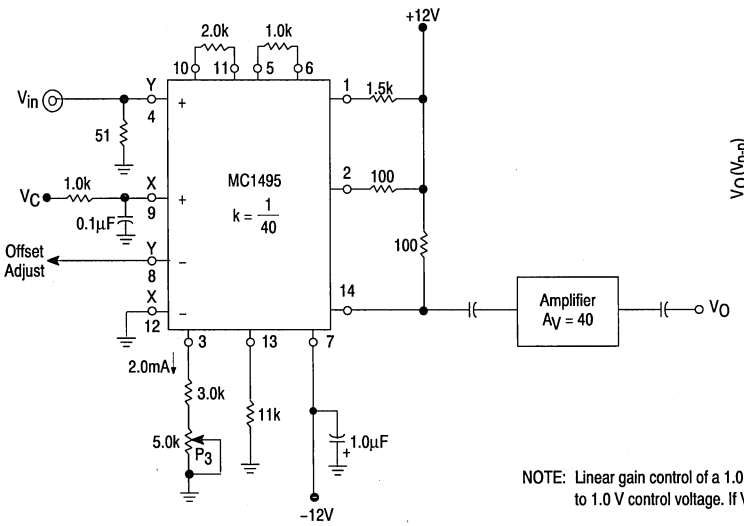
$$K = \frac{R_L}{R_X R_Y I_3}$$

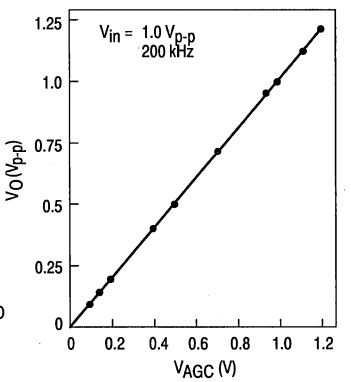
$$= \frac{100}{(2\text{ k})(1\text{ k})(2 \bullet 10^{+3})}\ V^{-1}$$

$$= \frac{1}{40}\ V^{-1}$$

The 2 in the numerator of the equation is missing in this scale factor expression because the output is single-ended and AC coupled.

Figure 31. Linear Gain Control





NOTE: Linear gain control of a 1.0 V_{p-p} signal is performed with a 0 V to 1.0 V control voltage. If V_C is 0.5 V the output will be 0.5 V_{p-p}.

MC3456

DUAL TIMING CIRCUIT

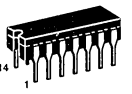
SILICON MONOLITHIC INTEGRATED CIRCUIT

Dual Timing Circuit

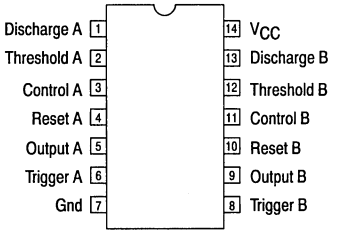
The MC3456 dual timing circuit is a highly stable controller capable of producing accurate time delays, or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor per timer. For astable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled with two external resistors and one capacitor per timer. The circuit may be triggered and reset on falling waveforms, and the output structure can source or sink up to 200 mA or drive MTTL circuits.

- Direct Replacement for NE556/SE556 Timers
- Timing From Microseconds Through Hours
- Operates in Both Astable and Monostable Modes
- Adjustable Duty Cycle
- High Current Output Can Source or Sink 200 mA
- Output Can Drive MTTL
- Temperature Stability of 0.005% per °C
- Normally "On" or Normally "Off" Output
- Dual Version of the Popular MC1455 Timer

L SUFFIX
CERAMIC PACKAGE
CASE 632

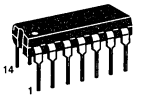


PIN CONNECTIONS



(Top View)

P SUFFIX
PLASTIC PACKAGE
CASE 646

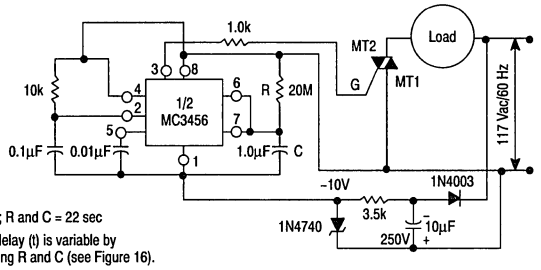


D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO-14)

ORDERING INFORMATION

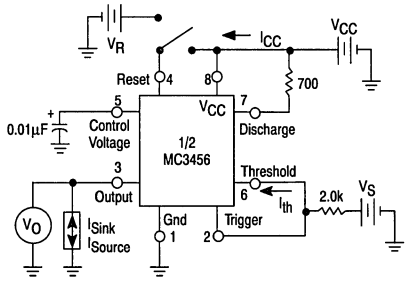
Device	Temperature Range	Package
MC3456L	0° to + 70°C	Ceramic DIP
MC3456P		Plastic DIP
NE556D		SO-14

Figure 1. 22 Second Solid State Time Delay Relay Circuit



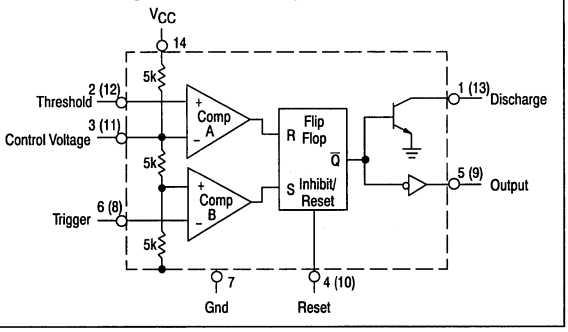
t = 1.1; R and C = 22 sec
Time delay (t) is variable by changing R and C (see Figure 16).

Figure 3. General Test Circuit



Test circuit for measuring DC parameters (to set output and measure parameters):
a) When $V_S \geq 2/3\ V_{CC}$, V_O is low.
b) When $V_S \leq 1/3\ V_{CC}$, V_O is high.
c) When V_O is low, Pin 7 sinks current. To test for Reset, set V_O high, apply Reset voltage, and test for current flowing into Pin 7. When Reset is not in use, it should be tied to V_{CC}.

Figure 2. Block Diagram (1/2 Shown)



MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+18	Vdc
Discharge Current	I_{dis}	200	mA
Power Dissipation (Package Limitation)	P_D		
J Suffix, Ceramic Package		1000	mW
Derate above T_A = +25°C		6.6	mW/°C
P Suffix, Plastic Package		625	mW
Derate above T_A = +25°C		5.0	mW/°C
D Suffix, Plastic SOIC Package		1.0	W
Derate above T_A = +25°C		8.0	mW/°C
Operating Ambient Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = +25°C, V_{CC} = +15 V, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	—	16	V
Supply Current	I_{CC}				mA
V_{CC} = 5.0 V, R_L = ∞		—	6.0	12	
V_{CC} = 15 V, R_L = ∞		—	20	30	
Low State, (Note 1)					
Timing Error (Note 2)					
Monostable Mode (R_A = 2.0 kΩ; C = 0.1 µF)					
Initial Accuracy		—	0.75	—	%
Drift with Temperature		—	50	—	PPM/°C
Drift with Supply Voltage		—	0.1	—	%/V
Astable Mode (R_A = R_B = 2.0 kΩ to 100 kΩ; C = 0.01 µF)					
Initial Accuracy		—	2.25	—	%
Drift with Temperature		—	150	—	PPM/°C
Drift with Supply Voltage		—	0.3	—	%/V
Threshold Voltage	V_{th}	—	2/3	—	xV_{CC}
Trigger Voltage	V_T				V
V_{CC} = 15 V		—	5.0	—	
V_{CC} = 5.0 V		—	1.67	—	
Trigger Current	I_T	—	0.5	—	µA
Reset Voltage	V_R	0.4	0.7	1.0	V
Reset Current	I_R	—	0.1	—	mA
Threshold Current (Note 3)	I_{th}	—	0.03	0.1	µA
Control Voltage Level	V_{CL}				V
V_{CC} = 15 V		9.0	10	11	
V_{CC} = 5.0 V		2.6	3.33	4.0	
Output Voltage Low	V_{OL}				
(V_{CC} = 15 V)					V
I_{Sink} = 10 mA		—	0.1	0.25	
I_{Sink} = 50 mA		—	0.4	0.75	
I_{Sink} = 100 mA		—	2.0	2.75	
I_{Sink} = 200 mA		—	2.5	—	
(V_{CC} = 5.0 V)					
I_{Sink} = 5.0 mA		—	0.25	0.35	
Output Voltage High	V_{OH}				V
(I_{Source} = 200 mA)					
V_{CC} = 15 V		—	12.5	—	
(I_{Source} = 100 mA)					
V_{CC} = 15 V		12.75	13.3	—	
V_{CC} = 5.0 V		2.75	3.3	—	
Toggle Rate (Figure 17, 19)					
R_A = 3.3 kΩ, R_B = 6.8 kΩ, C= 0.003 µF	—	—	100	—	kHz
Discharge Leakage Current	I_{dis}	—	20	100	nA
Rise Time of Output	t_{OLH}	—	100	—	ns
Fall Time of Output	t_{OHL}	—	100	—	ns
Matching Characteristics Between Sections					
Monostable Mode					
Initial Timing Accuracy		—	1.0	2.0	%
Timing Drift with Temperature		—	±10	—	ppm/°C
Drift with Supply Voltage		—	0.2	0.5	%/V

NOTES: 1. Supply current is typically 1.0 mA less for each output which is high.
2. Tested at V_{CC} = 5.0 V and V_{CC} = 15 V.
3. This will determine the maximum value of R_A + R_B for 15 V operation. The maximum total R = 20 mΩ.

Figure 4. Trigger Pulse Width

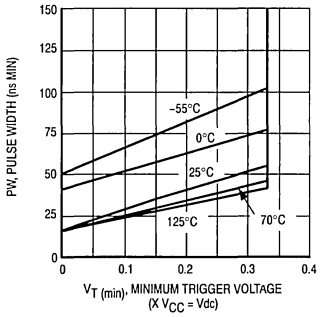


Figure 5. Supply Current

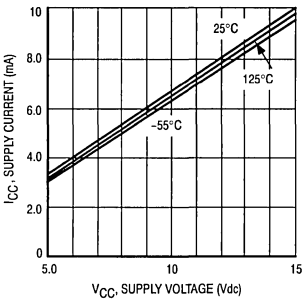


Figure 6. High Output Voltage

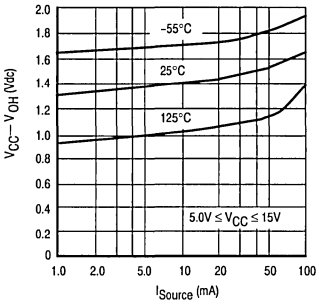


Figure 7. Low Output Voltage
(@ V_{CC} = 5.0 Vdc)

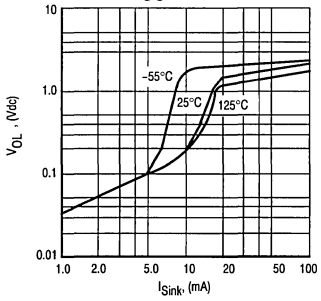


Figure 8. Low Output Voltage
(@ V_{CC} = 10 Vdc)

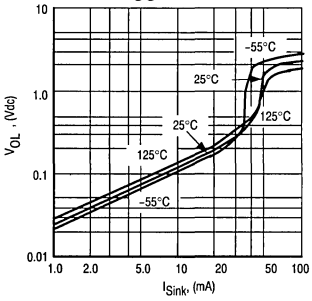


Figure 9. Low Output Voltage
(@ V_{CC} = 15 Vdc)

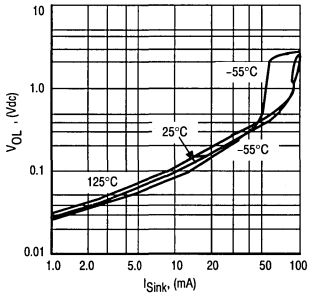


Figure 10. Delay Time versus Supply Voltage

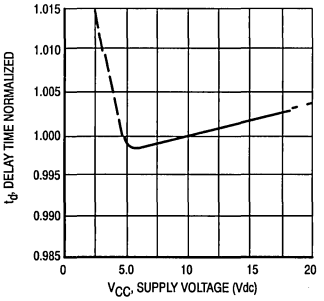


Figure 11. Delay Time versus Temperature

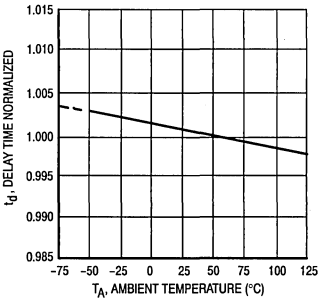
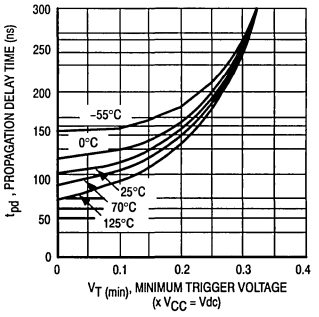
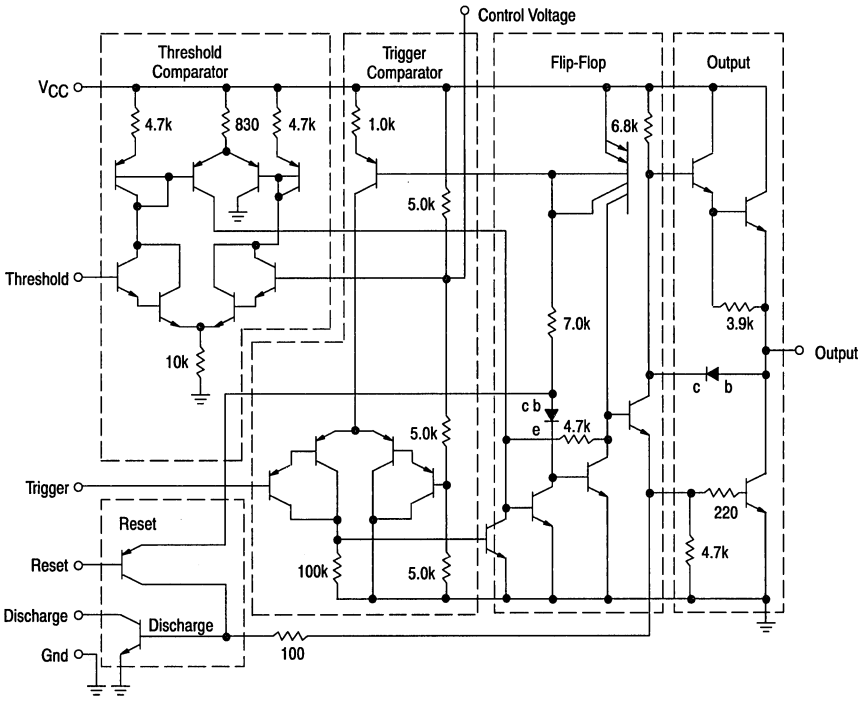


Figure 12. Propagation Delay versus Trigger Voltage



11

Figure 13. 1/2 Representative Circuit Schematic



GENERAL OPERATION

The MC3456 is a dual timing circuit which uses as its timing elements an external resistor/capacitor network. It can be used in both the monostable (one shot) and astable modes with frequency and duty cycle, controlled by the capacitor and resistor values. While the timing is dependent upon the external passive components, the monolithic circuit provides the starting circuit, voltage comparison and other functions needed for a complete timing circuit. Internal to the integrated circuit are two comparators, one for the input signal and the other for capacitor voltage; also a flip-flop and digital output are included. The comparator reference voltages are always a fixed ratio of the supply voltage thus providing output timing independent of supply voltage.

Monostable Mode

In the monostable mode, a capacitor and a single resistor are used for the timing network. Both the threshold terminal and the discharge transistor terminal are connected together in this mode, refer to circuit Figure 15. When the input voltage to the trigger comparator falls below 1/3 V_{CC} the comparator output triggers the flip-flop so that it's output sets low. This turns the capacitor discharge transistor "off" and drives the digital output to the high state. This condition allows the capacitor to charge at an exponential rate which is set by the RC time constant. When the capacitor voltage reaches 2/3 V_{CC} the threshold comparator resets the flip-flop. This action discharges the timing capacitor and returns the digital output to the low state. Once the flip-flop has been triggered by an input signal, it cannot be retriggered until the present timing period has been completed. The time that the output is high is given by the equation $t = 1.1\ R_A\ C$. Various combinations of R and C and their associated times are shown in Figure 14. The trigger pulse width must be less than the timing period.

A reset pin is provided to discharge the capacitor thus interrupting the timing cycle. As long as the reset pin is low, the capacitor discharge transistor is turned "on" and prevents the capacitor from charging. While the reset voltage is applied the digital output will remain the same. The reset pin should be tied to the supply voltage when not in use.

Figure 14. Time Delay

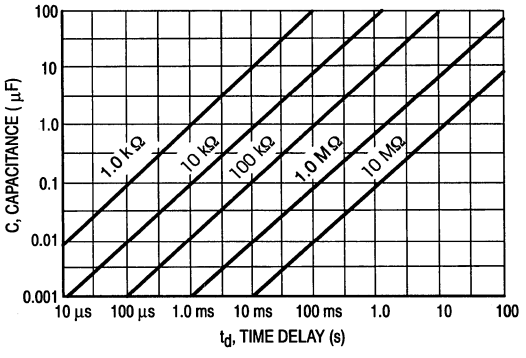
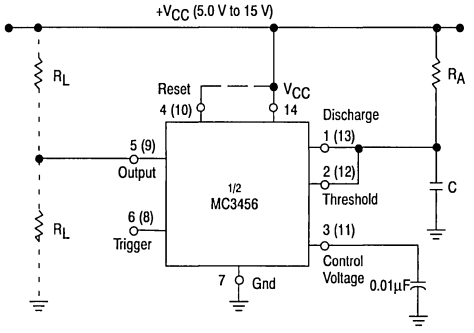
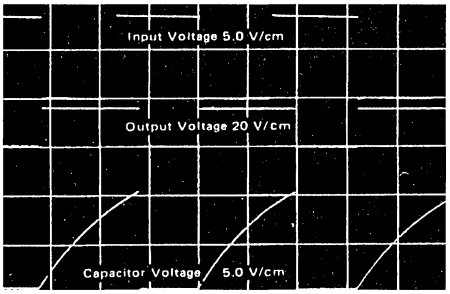


Figure 15. Monostable Circuit



Pin numbers in parenthesis ( ) indicate B-Channel

Figure 16. Monostable Waveforms



t = 50 µs/cm
(R_A = 10 kΩ, C = 0.01 µF, R_L = 1.0 kΩ, V_{CC} = 15 V)

Figure 17. Astable Circuit

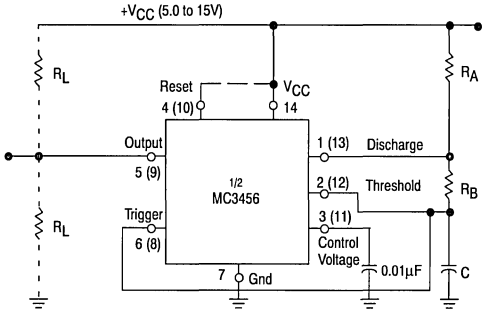
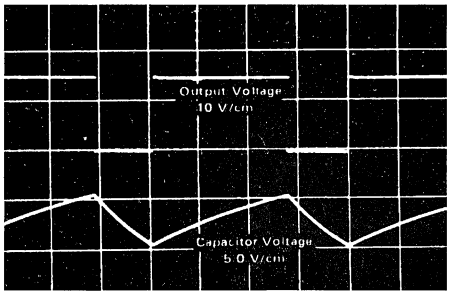


Figure 18. Astable Waveforms



t = 20 µs/cm
(R_A = 5.1 kΩ, C = 0.0 1 µF, R_L = 1.0 kΩ, R_B = 3.9 kΩ, V_{CC} = 15 V)

Astable Mode

In the astable mode the timer is connected so that it will retrigger itself and cause the capacitor voltage to oscillate between 1/3 V_{CC} and 2/3 V_{CC} (see Figure 17).

The external capacitor charges to 2/3 V_{CC} through R_A and R_B and discharges to 1/3 V_{CC} through R_B. By varying the ratio of these resistors the duty cycle can be varied. The charge and discharge times are independent of the supply voltage.

The charge time (output high) is given by:

$$t_1 = 0.695\ (R_A + R_B)\ C$$

The discharge time (output low) by:

$$t_2 = 0.695\ (R_B)\ C$$

Thus the total period is given by:

$$T = t_1 + t_2 = 0.695\ (R_A + 2R_B)\ C$$

The frequency of oscillation is then: $f = \frac{1}{T} = \frac{1.44}{(R_A + 2R_B)\ C}$

and may be easily found as shown in Figure 19.

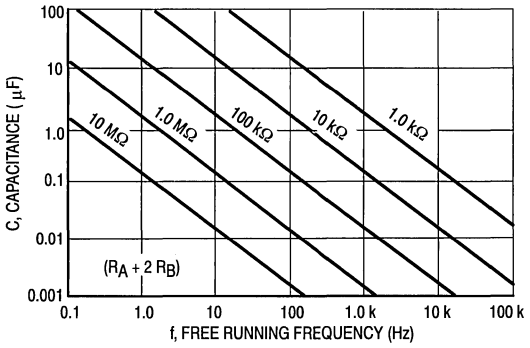
The duty cycle is given by: $DC = \frac{R_B}{R_A + 2R_B}$

To obtain the maximum duty cycle R_A must be as small as possible; but it must also be large enough to limit the discharge current (Pin 7 current) within the maximum rating of the discharge transistor (200 mA).

The minimum value of R_A is given by:

$$R_A \geq \frac{V_{CC}\ (Vdc)}{I_7\ (A)} \geq \frac{V_{CC}\ (Vdc)}{0.2}$$

Figure 19. Free Running Frequency



APPLICATIONS INFORMATION

Tone Burst Generator

For a tone burst generator the first timer is used as a monostable and determines the tone duration when triggered by a positive pulse at Pin 6. The second timer is enabled by the high output of the monostable. It is connected as an astable and determines the frequency of the tone.

Dual Astable Multivibrator

This dual astable multivibrator provides versatility not available with single timer circuits. The duty cycle can be adjusted from 5% to 95%. The two outputs provide two phase clock signals often required in digital systems. It can also be inhibited by use of either reset terminal.

Figure 20. Tone Burst Generator

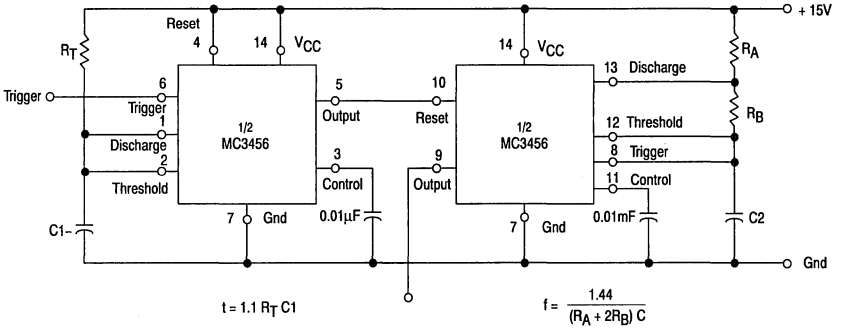
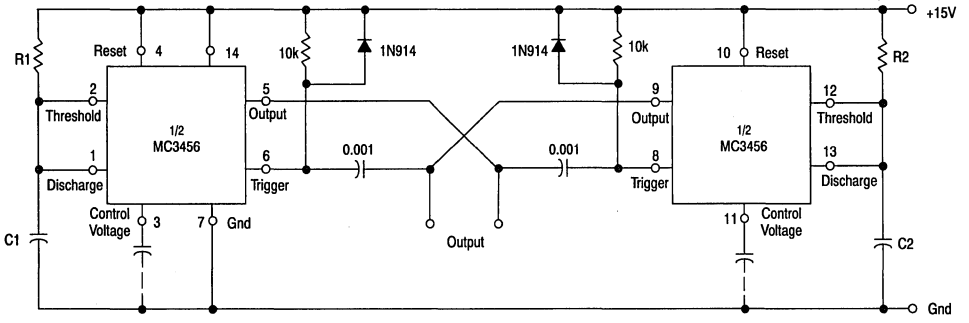


Figure 21. Dual Astable Multivibrator



Pulse Width Modulation

If the timer is triggered with a continuous pulse train in the monostable mode of operation, the charge time of the capacitor can be varied by changing the control voltage at Pin 3. In this manner, the output pulse width can be modulated by applying a modulating signal that controls the threshold voltage.

Test Sequences

Several timers can be connected to drive each other for sequential timing. An example is shown in Figure 24 where the sequence is started by triggering the first timer which runs for 10 ms. The output then switches low momentarily and starts the second timer which runs for 50 ms and so forth.

Figure 22. Pulse Width Modulation Circuit

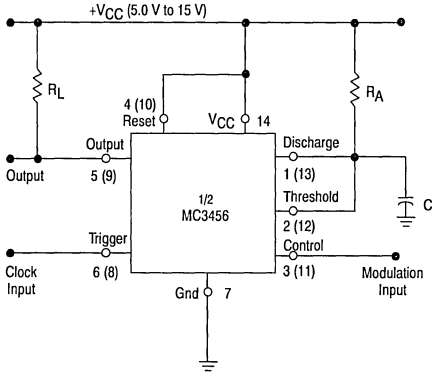
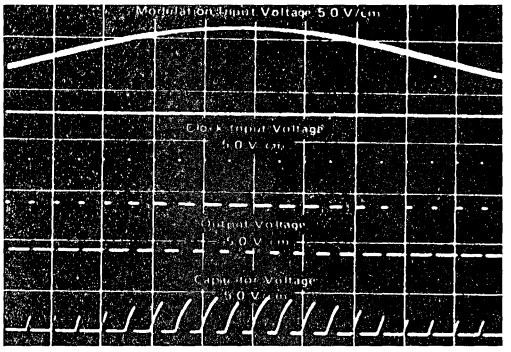
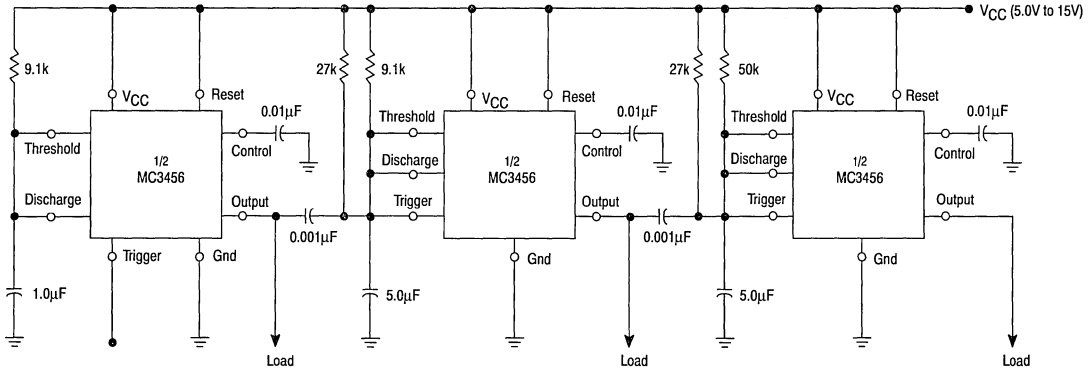


Figure 23. Pulse Width Modulation Waveforms



t = 0.5 ms/cm
(R_A = 10 kΩ, C = 0.02 μF, V_{CC} = 15 V)

Figure 24. Sequential Timing Circuit



Surface Mount Technology

In Brief . . .

Surface Mount Technology is now being utilized to offer answers to many problems that have been created in the use of Insertion Technology. Limitations have been reached with insertion packages and PC board technology. Surface Mount Technology offers the opportunity to continue to advance state-of-the-art designs that cannot be accomplished with Insertion Technology.

Surface Mount packages allow more optimum device performance with the smaller Surface Mount configuration. Internal lead lengths, parasitic capacitance and inductance that placed limitations on chip performance, have been reduced. The lower profile of Surface Mount packages allows more boards to be utilized in a given amount of space. They are stacked closer together and utilize less total volume than insertion populated PC boards.

Printed circuit costs are lowered with the reduction of the number of board layers required. The elimination or reduction of the number of plated-through-holes in the board, contribute significantly to lower PC board prices.

Surface Mount assembly does not require the preparation of components that are common on insertion technology lines. Surface Mount components are set directly to the assembly line, eliminating an intermediate step. Automatic placement equipment is available that can place Surface Mount components at the rate of a few thousand per hour to hundreds of thousands of components per hour.

Surface Mount Technology is cost effective, allowing the manufacturer the opportunity to produce smaller units and offer increased functions with the same size product.

Linear and Interface

Bipolar

All the major bipolar analog families are now represented in surface mount packaging. Standard SOIC and PLCC packages are augmented by SOP-8 and DPAK for Linear regulators. In addition, tape and reel shipping to the updated EIA-481A is now on line for the industry's largest array of operational amplifiers, regulators, interface, data conversion, consumer, telecom and automotive Linear ICs.

Device	Function	Package
CA3146D	Transistor Array	SO-14
DAC-08CD, ED	High-Speed 8-Bit Multiplying D-to-A Converter	SO-16
LF351D	Single JFET Operational Amplifier	SO-8
LF353D	Dual JFET Operational Amplifiers	SO-8
LF411CD	Single/Dual JFET Operational Amplifier	SO-8
LF412CD	Dual JFET Operational Amplifiers	SO-8
LF441CD	Single JFET Low Power Operational Amplifier	SO-8
LF442CD	Dual JFET Low Power Operational Amplifiers	SO-8
LF444CD	Quad JFET Low Power Operational Amplifiers	SO-14
LM201AD	General Purpose Adjustable Operational Amplifier	SO-8
LM211D	High Performance Voltage Comparator	SO-8
LM224D	Quad Low Power Operational Amplifiers	SO-14
LM239D,AD	Quad Single Supply Comparators	SO-14
LM258D	Dual Low Power Operational Amplifiers	SO-8
LM285D-1.2	Micropower Voltage Reference Diode	SO-8
LM285D-2.5	Micropower Voltage Reference Diode	SO-8
LM293D	Dual Comparators	SO-8
LM301AD	General Purpose Adjustable Operational Amplifier	SO-8
LM311D	High Performance Voltage Comparator	SO-8
LM317LD	Positive Adjustable 100 mA Voltage Regulator	SOP-8
LM317MDT	Positive Adjustable 500 mA Voltage Regulator	DPAK
LM324D,AD	Quad Low Power Operational Amplifiers	SO-14
LM339D,AD	Quad Single Supply Comparators	SO-14
LM348D	Quad MC1741 Operational Amplifiers	SO-14
LM358D	Dual Low Power Operational Amplifiers	SO-8
LM385D-1.2	Micropower Voltage Reference Diode	SO-8
LM385D-2.5	Micropower Voltage Reference Diode	SO-8
LM393D	Dual Comparators	SO-8
LM833D	Dual Audio Amplifiers	SO-8
LM2901D	Quad Single Supply Comparators	SO-14
LM2902D	Quad Low Power Operational Amplifiers	SO-14
LM2903D	Dual Comparators	SO-8
LM2904D	Dual Low Power Operational Amplifiers	SO-8
LM2931AD-5.0,D-5.0	Low Dropout Voltage Regulator	SOP-8
LM2931CD	Adjustable Low Dropout Voltage Regulator	SOP-8
LM3900D	Quad Single Supply Operational Amplifiers	SO-14
MC1350D	IF Amplifier	SO-8
MC1357D	FM IC with Quadrature Detector	SO-14
MC1377DW	Color Television RGB to PAL/NTSC Encoder	SO-20L
MC1378FN	Video Overlay Synchronizer	PLCC-44
MC1382DW	Multimode Monitor TTL To Analog Video	SO-24L
MC1403D	Precision Low Voltage Reference	SO-8
MC1413D	Peripheral Driver Array	SO-16
MC1436D,CD	High Voltage Operational Amplifier	SO-8
MC1455D	Timing Circuit	SO-8
MC1458D,CD	Dual Operational Amplifiers	SO-8
MC14C88BD	Quad EIA-232-D/EIA-562 Drivers	SO-14
MC1488D	Quad EIA-232-D Drivers	SO-14

Bipolar (continued)

Device	Function	Package
MC14C89ABD,BD	Quad EIA-232-D/EIA-562 Receivers	SO-14
MC1489D	Quad EIA-232-D Receivers	SO-14
MC1495D	Four-Quadrant Multiplier	SO-14
MC1496D	Balanced Modulator/Demodulator	SO-14
MC1723CD	Adjustable Positive or Negative Voltage Regulator	SO-14
MC1741CD	General Purpose Operational Amplifier	SO-8
MC1747CD	Dual MC1741 Operational Amplifiers	SO-14
MC1776CD	Programmable Operational Amplifier	SO-8
MC26LS31D	Quad EIA-422/23 Drivers	SO-16
MC26LS32D	Quad EIA-422 Receivers	SO-16
MC26S10D	Quad Bus Transceiver	SO-16
MC2831AD	FM Transmitter	SO-16
MC3303D	Quad Differential-Input Operational Amplifier	SO-14
MC3335DW	Basic Dual Conversion Receiver	SO-20L
MC3346D	General Purpose Transistor Array	SO-14
MC3356DW	FSK Receiver	SO-20L
MC3359DW	Low Power Narrowband FM IF Amplifier	SO-20L
MC3361AD	Low Voltage Narrowband FM IF Amplifier	SO-16
MC3362DW	Dual Conversion Receivers	SO-28L
MC3363DW	Dual Conversion Receivers	SO-28L
MC3367DW	Low Voltage VHF Receiver	SO-28L
MC3371D	Low Voltage FM Receiver with RSSI, LC Quadrature Detector	SO-16
MC3372D	Low Voltage FM Receiver with RSSI, Ceramic Quadrature Detector	SO-16
MC3391DW	Low Side Protected Switch	SOP-8+8L
MC3401D	Quad Operational Amplifiers	SO-14
MC3403D	Quad Differential-Input Operational Amplifier	SO-14
MC3418DW	CVSD	SO-16L
MC3423D	Overvoltage Sensing Circuit	SO-8
MC3448AD	Quad GPIB Transceivers	SO-16
MC3450D	Quad Line Receivers	SO-16
MC3452D	Quad Line Receivers	SO-16
MC3456D	Dual Timing Circuit	SO-14
MC3458D	Dual Low Power Operational Amplifiers	SO-8
MC3486D	Quad EIA-422/23 Receivers	SO-16
MC3487D	Quad EIA-422 Drivers	SO-16
MC4558CD	Dual High Frequency Operational Amplifiers	SO-8
MC4741CD	Quad MC1741 Operational Amplifiers	SO-14
MC78L05ACD	Positive Voltage Regulator, 5 V, 100 mA	SOP-8
MC78L08ACD	Positive Voltage Regulator, 8 V, 100 mA	SOP-8
MC78L12ACD	Positive Voltage Regulator, 12 V, 100 mA	SOP-8
MC78L15ACD	Positive Voltage Regulator, 15 V, 100 mA	SOP-8
MC78M05CDT	Positive Voltage Regulator, 5 V, 500 mA	DPAK
MC78M08CDT	Positive Voltage Regulator, 8 V, 500 mA	DPAK
MC78M12CDT	Positive Voltage Regulator, 12 V, 500 mA	DPAK
MC78M15CDT	Positive Voltage Regulator, 15 V, 500 mA	DPAK
MC79L05ACD	3-Terminal Negative Fixed Voltage Regulator, –5 V, 100 mA	SOP-8
MC79L12ACD	3-Terminal Negative Fixed Voltage Regulator, –12 V, 100 mA	SOP-8
MC79L15ACD	3-Terminal Negative Fixed Voltage Regulator, –15 V, 100 mA	SOP-8
MC79M05CDT	3-Terminal Negative Fixed Voltage Regulator, –5 V, 500 mA	DPAK
MC79M12CDT	3-Terminal Negative Fixed Voltage Regulator, –12 V, 500 mA	DPAK
MC79M15CDT	3-Terminal Negative Fixed Voltage Regulator, –15 V, 500 mA	DPAK
MC10319DW	8-Bit A/D Flash Converter	SO-24L
MC10321DW	7-Bit A/D Flash Converter	SO-20L
MC13022DW(1)	Medium Voltage AM Stereo C-QUAM® Decoder	SO-28L

(1)To be introduced.

Bipolar (continued)

Device	Function	Package
MC13024DW	Low Voltage C-QUAM® Receiver	SO-24L
MC13055D	VHF LAN Receiver — FSK	SO-16
MC13060D	1 Watt Audio Amplifier	SOP-8
MC33023DW,FN	High Speed (1.0 MHz) Single-Ended PWM Controller	SO-16L, PLCC-20
MC33025DW,FN	High Speed (1.0 MHz) Double-Ended PWM Controller	SO-16L, PLCC-20
MC33033DW	Brushless DC Motor Controller	SO-20L
MC33035DW	Brushless DC Motor Controller	SO-24L
MC33039D	Closed Loop Brushless Motor Adaptor (5 V ± 5% Supply)	SO-8
MC33060AD	Precision Switchmode Pulse Width Modulator	SO-14
MC33064D-5	Undervoltage Sensing Circuit	SO-8
MC33065DW	Dual Current Mode PWM Controller	SO-16L
MC33065DW-H	Dual Current Mode PWM Controller (Off-Line)	SO-16L
MC33065DW-L	Dual Current Mode PWM Controller (DC-to-DC Converters)	SO-16L
MC33066DW	Resonant Mode (ZCS) Controller	SO-16L
MC33067DW	Resonant Mode (ZVS) Controller	SO-16L
MC33071D,AD	Single, High Speed Single Supply Operational Amplifiers	SO-8
MC33072D,AD	Dual, High Speed Single Supply Operational Amplifiers	SO-8
MC33074D,AD	Quad, High Speed Single Supply Operational Amplifiers	SO-14
MC33076D	Dual High Output Current Operational Amplifiers	SO-8
MC33077D	Dual, Low Noise High Frequency Operational Amplifiers	SO-8
MC33078D	Dual Audio, Low Noise Operational Amplifiers	SO-8
MC33079D	Low Power, Single Supply Operational Amplifier	SO-14
MC33091D	High Side TMOS Driver	SO-8
MC33102D	Sleep-Mode™ 2-State, µProcessor Operational Amplifier	SO-8
MC33110D	Low Voltage Compander	SO-14
MC33120FN	SLIC II	PLCC-28
MC33121FN	Low Voltage Subscriber Loop Interface Circuit	PLCC-28
MC33129D	High Performance Current Mode Controller	SO-14
MC33151D	Dual Inverting MOSFET Drivers	SO-8
MC33152D	Dual Noninverting MOSFET Drivers	SO-8
MC33161D	Universal Voltage Monitor	SO-8
MC33164D-3	Micropower Undervoltage Sensing Circuit (3 V ± 5% Supply)	SO-8
MC33164D-5	Micropower Undervoltage Sensing Circuit (5 V ± 10% Supply)	SO-8
MC33171D	Single, Low Power, Single Supply Operational Amplifier	SO-8
MC33172D	Dual, Low Power, Single Supply Operational Amplifiers	SO-8
MC33174D	Quad, Low Power, Single Supply Operational Amplifiers	SO-14
MC33178D	Dual Precision Operational Amplifiers	SO-8
MC33179D	Quad Precision Operational Amplifiers	SO-14
MC33218DW	Voice-Switched Speakerphone with µProcessor Interface	SO-24L
MC33261D	Power Factor Controller	SO-8
MC33272D	Dual Precision Bipolar Operational Amplifiers	SO-8
MC33274D	Quad Precision Bipolar Operational Amplifiers	SO-14
MC33282D	Dual Precision Low Input JFET Operational Amplifiers (Trim-in-the-Package)	SO-8
MC33284D	Quad Precision JFET Operational Amplifiers (Trim-in-the-Package)	SO-14
MC34001D,BD	Single JFET Input Operational Amplifier	SO-8
MC34002D,BD	Dual JFET Input Operational Amplifiers	SO-8
MC34010FN	Electronic Telephone Circuit	PLCC-44
MC34012-1D	Telephone Tone Ringer	SO-8
MC34012-2D	Telephone Tone Ringer	SO-8
MC34012-3D	Telephone Tone Ringer	SO-8
MC34014DW	Telephone Speech Network with Dialer Interface	SO-20L
MC34017-1D	Telephone Tone Dialer	SO-8
MC34017-2D	Telephone Tone Dialer	SO-8
MC34017-3D	Telephone Tone Dialer	SO-8
MC34018DW	Voice Switched Speakerphone Circuit	SO-28L
MC34023DW,FN	High Speed (1.0 MHz) Single-Ended PWM Controller	SO-16L, PLCC-20

Bipolar (continued)

Device	Function	Package
MC34025DW,FN	High Speed (1.0 MHz) Double-Ended PWM Controller	SO-16L, PLCC-20
MC34050D	EIA-422/23 Transceivers	SO-16
MC34051D	EIA-422/23 Transceivers	SO-16
MC34060AD	Switchmode Pulse Width Modulation Control Circuit	SO-14
MC34063AD	Precision DC-to-DC Converter Control Circuit	SO-8
MC34064D-5	Undervoltage Sensing Circuit (5 V ± 5% Supply)	SO-8
MC34065DW	Dual Current Mode PWM Controller	SO-16L
MC34065DW-H	Dual Current Mode PWM Controller (Off-Line)	SO-16L
MC34065DW-L	Dual Current Mode PWM Controller (DC-to-DC Converter)	SO-16L
MC34066DW	Resonant Mode (ZCS) Controller	SO-16L
MC34067DW	Resonant Mode (ZVS) Controller	SO-16L
MC34071D,AD	Single, High Speed, Single Supply Operational Amplifier	SO-8
MC34072D,AD	Dual, High Speed, Single Supply Operational Amplifiers	SO-8
MC34074D,AD	Quad, High Performance, Single Supply Operational Amplifiers	SO-14
MC34080D	High Speed Decompensated ($A_{VCL} \geq 2$) JFET Input Operational Amplifier	SO-8
MC34081D	High Speed JFET Input Operational Amplifier	SO-8
MC34084DW,ADW	Quad High Speed, JFET Operational Amplifier	SO-16L
MC34085DW,ADW	Quad High Speed, JFET Operational Amplifier	SO-16L
MC34114DW	Speech Network II	SO-18L
MC34115DW	CVSD	SO-16L
MC34118DW	Speakerphone II	SO-28L
MC34119D	Telephone Speaker Amplifier	SO-8
MC34129D	Power Supply Controller	SO-14
MC34151D	Dual Inverting MOSFET Drivers	SO-8
MC34152D	Dual Noninverting MOSFET Drivers	SO-8
MC34161D	Universal Voltage Monitor	SO-8
MC34164D-3	Micropower Undervoltage Sensing Circuit (3 V ± 5% Supply)	SO-8
MC34164D-5	Micropower Undervoltage Sensing Circuit (5 V ± 10% Supply)	SO-8
MC34181D	Single, Low Power, High Speed JFET Operational Amplifier	SO-8
MC34182D	Dual, Low Power, High Speed JFET Operational Amplifiers	SO-8
MC34184D	Quad, Low Power, High Speed JFET Operational Amplifiers	SO-14
MC34217D	Adjustable Toner Ringer	SO-8
MC34261D	Power Factor Controller	SO-8
MC44301DW	High Performance Video IF	SO-28L
MC75172BDW	Quad EIA-485 Line Drivers w/3-State Outputs	SO-20L
MC75174BDW	Quad EIA-485 Line Drivers w/3-State Outputs	SO-20L
NE556D	Dual Timing Circuit	SO-14
TL064CD	Quad JFET Low Power Operational Amplifiers	SO-14
TL071CD,ACD	Single, Low Noise JFET Input Operational Amplifier	SO-8
TL072CD,ACD	Dual, Low Noise JFET Input Operational Amplifiers	SO-8
TL081CD,ACD	Single, JFET Input Operational Amplifier	SO-8
TL082CD,ACD	Dual, JFET Input Operational Amplifiers	SO-8
TL431ACD,AID,CD,ID	Programmable Precision Reference	SOP-8
UAA1041BD	Automotive Direction Indicator	SO-8
UC2842AD, BD, BD1	Off-Line Current Mode PWM Controller	SO-14, SO-8
UC2843AD, BD, BD1	Current Mode PWM Controller	SO-14, SO-8
UC2844D, BD, BD1	Off-Line Current Mode PWM Controller (DC ≤ 50%)	SO-14, SO-8
UC2845D, BD, BD1	Current Mode PWM Controller (DC ≤ 50%)	SO-14, SO-8
UC3842AD, BD, BD1	Off-Line Current Mode PWM Controller	SO-14, SO-8
UC3843AD, BD, BD1	Current Mode PWM Controller	SO-14, SO-8
UC3844D, BD, BD1	Off-Line Current Mode PWM Controller (DC ≤ 50%)	SO-14, SO-8
UC3845D, BD, BD1	Current Mode PWM Controller (DC ≤ 50%)	SO-14, SO-8

MOS Digital-Analog

Device	Function	Package
A/D and D/A Converters		
MC14433DW	3-1/2 Digit A/D Converter	SO-24L
MC14442FN	11-Channel 8-Bit A/D Converter with Parallel Interface	PLCC-28
MC14443DW	6-Channel A/D Converter Subsystem	SO-16L
MC14447DW	6-Channel A/D Converter Subsystem	SO-16L
MC44250FN	Triple 8-Bit Video A/D Converter	PLCC-44
MC144110DW	Hex D/A Converter with Serial Interface	SO-20L
MC144111DW	Quad D/A Converter with Serial Interface	SO-16L
MC145040FN1(2)	11-Channel, 8-Bit A/D Converter with Serial Interface	PLCC-20
MC145040FN2(2)	11-Channel, 8-Bit A/D Converter with Serial Interface	PLCC-20
MC145041FN1(2)	11-Channel, 8-Bit A/D Converter with Serial Interface	PLCC-20
MC145041FN2(2)	11-Channel, 8-Bit A/D Converter with Serial Interface	PLCC-20
MC145050DW	11-Channel, 10-Bit A/D Converter with Serial Interface	SO-20L
MC145051DW	11-Channel, 10-Bit A/D Converter with Serial Interface	SO-20L
MC145053D	11-Channel, 10-Bit A/D Converter with Serial Interface	SO-14
Display Drivers		
MC14489DW	Multi-Character LED Display/Lamp Driver	SO-20L
MC14495DW1(2)	Hex-to-7 Segment Latch/Decoder ROM/Driver	SO-16L
MC14499DW	7-Segment LED Display Decoder/Driver with Serial Interface	SO-20L
MC145000FN	48-Segment Multiplexed LCD Driver (Master)	PLCC-28
MC145001FN	44-Segment Multiplexed LCD Driver (Slave)	PLCC-28
MC145453FN	33-Segment LCD Driver with Serial Interface	PLCC-44
Operational Amplifiers/Comparators		
MC14573D	Quad Programmable Operational Amplifier	SO-16
MC14574D	Quad Programmable Comparator	SO-16
MC14575D	Dual Programmable Operational Amplifier and Dual Comparator	SO-16
MC14576BF	Dual Video Amplifier	SO-8 (EIAJ)
MC14577BF	Dual Video Amplifier	SO-8 (EIAJ)
MC14578D	Micro-Power Comparator Plus Voltage Follower	SO-16
Phase-Locked Loop Frequency Synthesizers		
MC145106FN	PLL Frequency Synthesizer	PLCC-20
MC145145DW1	4-Bit Data Bus Input PLL Frequency Synthesizer	SO-20L
MC145146DW1	4-Bit Data Bus Input PLL Frequency Synthesizer	SO-20L
MC145149DW	Serial Input Dual PLL Frequency Synthesizer	SO-20L
MC145151DW2	Parallel Input PLL Frequency Synthesizer	SO-28L
MC145151FN2	Parallel Input PLL Frequency Synthesizer	PLCC-28
MC145152DW2	Parallel Input PLL Frequency Synthesizer	SO-28L
MC145152FN2	Parallel Input PLL Frequency Synthesizer	PLCC-28
MC145155FN2	Serial Input PLL Frequency Synthesizer	PLCC-20
MC145155DW2	Serial Input PLL Frequency Synthesizer	SO-20L
MC145156FN2	Serial Input PLL Frequency Synthesizer	PLCC-20
MC145156DW2	Serial Input PLL Frequency Synthesizer	SO-20L
MC145157FN2	Serial Input PLL Frequency Synthesizer	PLCC-20
MC145157DW2	Serial Input PLL Frequency Synthesizer	SO-16L
MC145158FN2	Serial Input PLL Frequency Synthesizer	PLCC-20
MC145158DW2	Serial Input PLL Frequency Synthesizer	SO-16L
MC145159DW1	Serial Input PLL Frequency Synthesizer with Analog Phase Detector	SO-20L
MC145159FN(3)	Serial Input PLL Frequency Synthesizer with Analog Phase Detector	PLCC-20
MC145160DW	Dual PLL for Cordless Telephones	SO-20L
MC145161DW	Dual PLL for Cordless Telephones	SO-16L
MC145166DW	Dual PLL for Cordless Telephones	SO-16L
MC145167DW	Dual PLL for Cordless Telephones	SO-16L
MC145168DW	Dual PLL for Cordless Telephones	SO-16L
MC145170D	Serial Interface PLL Frequency Synthesizer	SO-16

(2)The digit 1 or 2 after the package designator is not a part of the package definition, but describes the electrical capability of the device.
(3)Electrical variations may require a numerical suffix after the package suffix. Contact your Motorola representative for details.
(4)Introduction of this device in surface mount packages is dependent on market demand.

MOS Digital-Analog (continued)

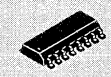
Device	Function	Package
Remote Control Functions		
MC14469FN	Addressable Asynchronous Receiver/Transmitter	PLCC-44
MC14497	PCM Remote Control Transmitter	(3)
MC145026D	Remote Control Encoder	SO-16
MC145027DW	Remote Control Decoder	SO-16L
MC145028DW	Remote Control Decoder	SO-16L
MC145030DW	Remote Control Encoder/Decoder	SO-20
MC145033DW	Remote Control Encoder/Decoder	SO-28L
MC145034DW	Remote Control Encoder	SO-28L
MC145035DW	Remote Control Decoder	SO-28L
Smoke Detectors		
MC14467	Low-Cost Smoke Detector	(3)
MC14468	Interconnectable Smoke Detector	(3)
MC145010DW	Photoelectric Smoke Detector with I/O	SO-16L
MC145011DW	Photoelectric Smoke Detector with I/O	SO-16L
Telecommunications Devices		
MC14410DW	2-of-8 Tone Encoder	SO-16L
MC14411DW	Bit Rate Generator	SO-24L
MC142100DW	Crosspoint Switch with Control Memory (4 × 4 × 1)	SO-16L
MC142103	Transcoder HDB31 AMI to NRZ	(3)
MC143403D	Quad Line Driver (Op Amp)	SO-14
MC145403DW	EIA-232/V.28 CMOS Driver/Receiver	SO-20L
MC145404DW	EIA-232/V.28 CMOS Driver/Receiver	SO-20L
MC145405DW	EIA-232/V.28 CMOS Driver/Receiver	SO-20L
MC145406DW	EIA-232/V.28 CMOS Driver/Receiver	SO-16L
MC145407DW	EIA-232/V.28 CMOS Driver/Receiver, 5.0 V Only	SO-20L
MC145408DW	EIA-232/V.28 CMOS Driver/Receiver	SO-20L
MC145412	Pulse/Tone Repertory Dialer (Nine 18-Digit Memory)	(3)
MC145416DW	Pulse/Tone Repertory Dialer (13 18-Digit Memory)	SO-20L
MC145421DW	UDLT II Master	SO-24L
MC145422DW	UDLT Master	SO-24L
MC145425DW	UDLT II Slave	SO-24L
MC145426DW	UDLT Slave	SO-24L
MC145428DW	Data Set Interface Circuit	SO-20L
MC145436DW	DTMF Decoder	SO-16L
MC145439	Transcoder B8ZS, B6ZS, HDB3 to NRZ	(3)
MC145442DW	300-Baud CCITT V.21 Single-Chip Modem	SO-20L
MC145443DW	300-Baud Bell 103 Single-Chip Modem	SO-20L
MC145447DW	Calling Line I.D. Receiver with Ring Detector	SO-16L
MC145472FE	ISDN U-Interface Transceiver	CQFP-68L
MC145472FU	ISDN U-Interface Transceiver	PQFP-68L
MC145475DW	ISDN S/T Transceiver	SO-28L
MC145480DW	+5.0 V PCM Codec/Filter	SO-20L
MC145488	Dual Data Link Controller	(3)
MC145502	PCM Codec/Filter	(3)
MC145503DW	PCM Codec/Filter	SO-16L
MC145505DW	PCM Codec/Filter	SO-16L
MC145532DW	ADPCM Transcoder	SO-16L
MC145540DW	ADPCM Codec	SO-28L
MC145554DW	PCM Codec/Filter (TP3054 Compatible)	SO-16L
MC145557DW	PCM Codec/Filter (TP3057 Compatible)	SO-16L
MC145564DW	PCM Codec/Filter (TP3064 Compatible)	SO-20L
MC145567DW	PCM Codec/Filter (TP3067 Compatible)	SO-20L
MC145705DW	EIA-232/V.28 CMOS Driver/Receiver, 5.0 V Only	SO-20L
MC145706DW	EIA-232/V.28 CMOS Driver/Receiver, 5.0 V Only	SO-20L
MC145707DW	EIA-232/V.28 CMOS Driver/Receiver, 5.0 V Only	SO-20L

Surface Mount Technology Package Overview

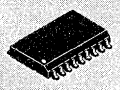
CASE 369A
PLASTIC
DPAK
DT SUFFIX

CASE 751
PLASTIC
SO-8, SOP-8
D, D1 SUFFIX

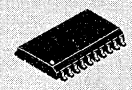
CASE 751A
PLASTIC
SO-14
D SUFFIX



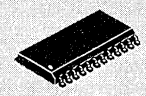
CASE 751B
PLASTIC
SO-16
D SUFFIX



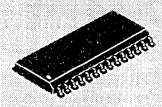
CASE 751C
PLASTIC
SO-18L
DW SUFFIX



CASE 751D
PLASTIC
SO-20L
DW SUFFIX



CASE 751E
PLASTIC
SO-24L
DW SUFFIX

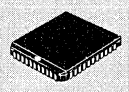


CASE 751F
PLASTIC
SO-28L
DW SUFFIX

CASE 751G
PLASTIC
SO-8+8L, SO-16L
DW SUFFIX

CASE 775
PLASTIC
PLCC-20
FN SUFFIX

CASE 776
PLASTIC
PLCC-28
FN SUFFIX



CASE 777
PLASTIC
PLCC-44
FN SUFFIX

12

Analog MPQ Table

Tape/Reel and Ammo Pack

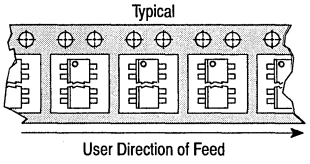
Package Type	Package Code	MPQ
PLCC		
Case 775	0802	1000/reel
Case 776	0804	500/reel
Case 777	0801	500/reel
Case 778	0805	450/reel
Case 779	0803	250/reel
Case 780	0806	250/reel
SOIC		
Case 751	0095	2500/reel
Case 751A	0096	2500/reel
Case 751B	0097	2500/reel
Case 751G	2003	1000/reel
Case 751C	2004	1000/reel
Case 751D	2005	1000/reel
Case 751E	2008	1000/reel
Case 751F	2009	1000/reel
TO-92		
Case 29	0031	2000/reel
Case 29	0031	2000/Ammo Pack

Tape and Reel
Logic and Analog Technologies, and MOS Integrated Circuits

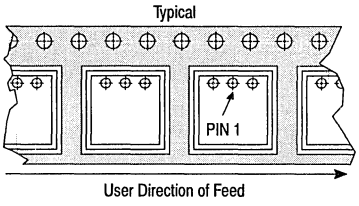
Motorola has now added the convenience of Tape and Reel packaging for our growing family of standard Integrated Circuit products. Three reel sizes are available, for all but the largest types, to support the requirements of both first and second generation pick-and-place equipment. The packaging fully conforms to the latest EIA-481A specification. The antistatic embossed tape provides a secure cavity, sealed with a peel-back cover tape.

Mechanical Polarization

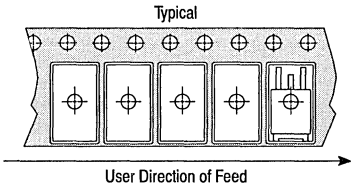
SOIC DEVICES



PLCC DEVICES



DPAK DEVICES

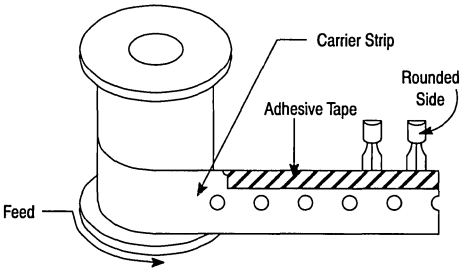


Package	Tape Width (mm)	Device(1) per Reel	Reel Size (inch)	Device Suffix
SO-8, SOP-8	12	2,500	13	R2
SO-14	16	2,500	13	R2
SO-16	16	2,500	13	R2
SO-16L, SO-8+8L WIDE	16	1,000	13	R2
SO-20L WIDE	24	1,000	13	R2
SO-24L WIDE	24	1,000	13	R2
SO-28L WIDE	24	1,000	13	R2
SO-28L WIDE	32	1,000	13	R3
PLCC-20	16	1,000	13	R2
PLCC-28	24	500	13	R2
PLCC-44	32	500	13	R2
PLCC-52	32	500	13	R2
PLCC-68	44	250	13	R2
PLCC-84	44	250	13	R2
TO-226AA (TO-92)(2)	18	2,000	13	RA, RB, RE, RM, or RP (Ammo Pack) only
DPAK	16	2,500	13	RK

(1)Minimum order quantity is 1 reel. Distributors/OEM customers may break lots or reels at their option, however broken reels may not be returned.
(2)Integrated circuits in TO-226AA packages are available in Styes A, B and E only, with optional "Ammo Pack" (Suffix RM or RP). For ordering information please contact your local Motorola Semiconductor Sales Office.

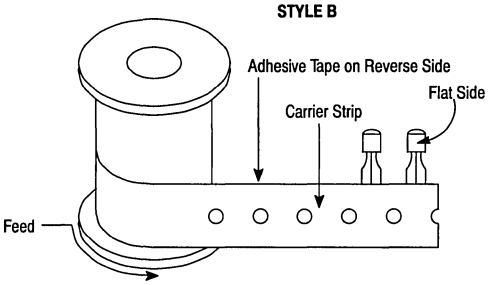
TO-92 Reel Styles

STYLE A



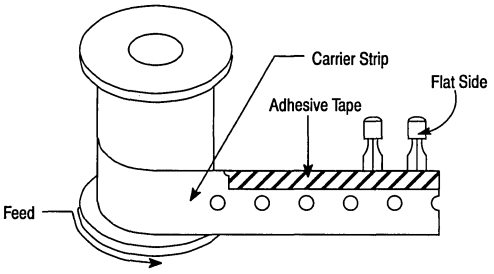
Rounded Side of Transistor and Adhesive Tape Visible.

STYLE B



Flat Side of Transistor and Carrier Strip Visible (Adhesive Tape on Reverse Side).

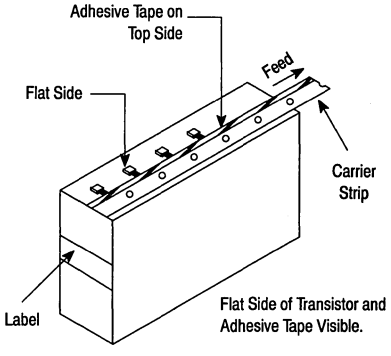
STYLE E



Flat Side of Transistor and Adhesive Tape Visible.

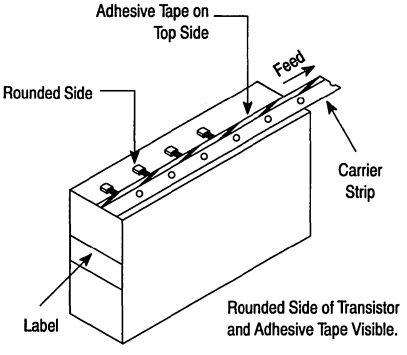
TO-92 Ammo Pack Styles

STYLE M



Style M Ammo Pack Is Equivalent to Style E of Reel Pack Dependent on Feed Orientation From Box.

STYLE P



Style P Ammo Pack Is Equivalent to Styles A and B of Reel Pack Dependent on Feed Orientation From Box.

12

Packaging Information

In Brief . . .

The packaging availability for each device type is indicated on the individual data sheets and the Selector Guide. All of the outline dimensions for the packages are given in this section.

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature can be found from the equation:

$$P_{D(TA)} = \frac{T_{J(max)} - T_A}{R_{\theta JA(Typ)}}$$

where:

$P_{D(TA)}$ = *Power Dissipation allowable at a given operating ambient temperature. This must be greater than the sum of the products of the supply voltages and supply currents at the worst case operating condition.*

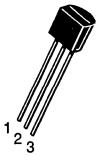
$T_{J(max)}$ = *Maximum operating Junction Temperature as listed in the Maximum Ratings Section. See individual data sheets for $T_{J(max)}$ information.*

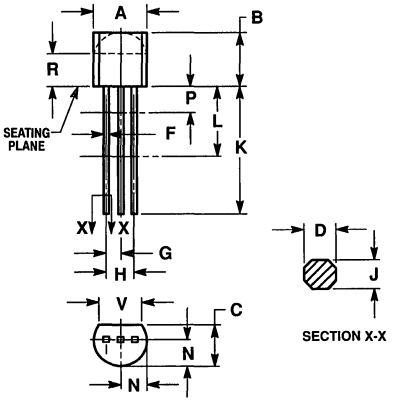
T_A = *Maximum desired operating Ambient Temperature*

$R_{\theta JA(Typ)}$ = *Typical Thermal Resistance Junction-to-Ambient*

Case Outline Dimensions

LP, P, Z SUFFIX
CASE 29-04
Plastic Package
$R_{\theta JA}$ = 200°C/W
(TO-226AA/TO-92)

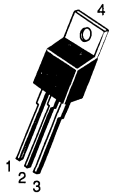


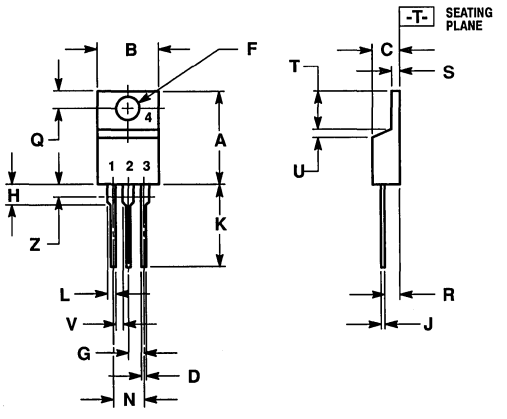


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CONTOUR OF PACKAGE BEYOND DIM R IS UNCONTROLLED.
4. DIM F APPLIES BETWEEN P AND L. DIM D AND J APPLIES BETWEEN L AND K MINIMUM. LEAD DIM IS UNCONTROLLED IN P AND BEYOND DIM K MINIMUM.
5. 029-01 AND -02 OBSOLETE, NEW STANDARD 029-04.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.45	5.20	0.175	0.205
B	4.32	5.33	0.170	0.210
C	3.18	4.19	0.125	0.165
D	0.41	0.55	—	0.022
F	0.41	0.48	0.016	0.019
G	1.15	1.39	0.045	0.055
H	2.42	2.66	0.095	0.105
J	0.39	0.50	0.015	0.020
K	12.70	—	0.500	—
L	6.35	—	0.250	—
N	2.04	2.66	0.080	0.105
P	—	2.54	—	0.100
R	2.93	—	0.115	—
V	3.43	—	0.135	—

KC, T SUFFIX
CASE 221A-06
Plastic Package
$R_{\theta JA}$ = 65°C/W (Typ)
(TO-220AB)



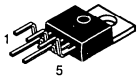


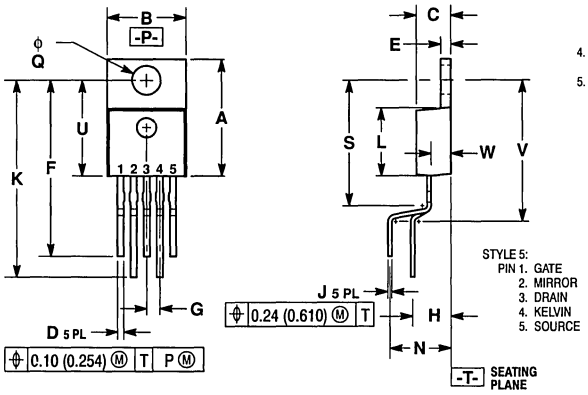
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.46	0.64	0.018	0.025
K	12.70	14.27	0.500	0.562
L	1.15	1.52	0.045	0.060
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

13

T, TV SUFFIX
CASE 314B-04
Plastic Package

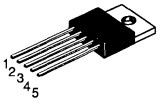


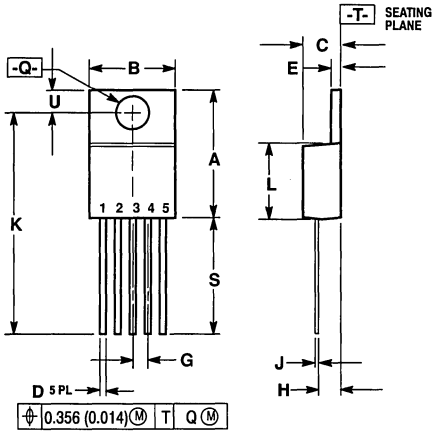


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION D DOES NOT INCLUDE INTERCONECT BAR (DAM BAR) PROTRUSION. DIMENSION D INCLUDING PROTRUSION SHALL NOT EXCEED 0.043 (1.092) MAXIMUM.
4. 314B-01, 314B-02 AND 314B-03 OBSOLETE, NEW STANDARD 314B-04.
5. STYLE 1 THRU 4: OBSOLETE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	14.529	15.570	0.572	0.613
B	9.906	10.541	0.390	0.415
C	4.318	4.572	0.170	0.180
D	0.635	0.965	0.025	0.038
E	1.219	1.397	0.048	0.055
F	21.590	23.749	0.850	0.935
G	1.702 BSC		0.067 BSC	
H	4.216 BSC		0.166 BSC	
J	0.381	0.635	0.015	0.025
K	22.860	27.940	0.900	1.100
L	8.128	9.271	0.320	0.365
N	8.128 BSC		0.320 BSC	
Q	3.556	3.886	0.140	0.153
S	—	15.748	—	0.620
U	11.888	12.827	0.468	0.505
V	—	18.669	—	0.735
W	2.286	2.794	0.090	0.110

T, T1 SUFFIX
CASE 314D-03
Plastic Package
$R_{\theta JA}$ = 65°C/W (Typ)

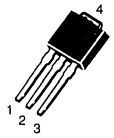


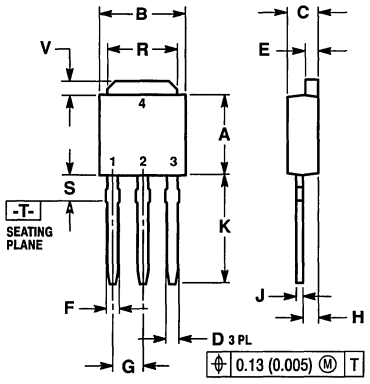


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	14.529	15.570	0.572	0.613
B	9.906	10.541	0.390	0.415
C	4.318	4.572	0.170	0.180
D	0.635	0.965	0.025	0.038
E	1.219	1.397	0.048	0.055
G	1.702 BSC		0.067 BSC	
H	2.210	2.845	0.087	0.112
J	0.381	0.635	0.015	0.025
K	25.908	27.051	1.020	1.065
L	8.128	9.271	0.320	0.365
Q	3.556	3.886	0.140	0.153
U	2.667	2.972	0.105	0.117
S	13.792	14.783	0.543	0.582

DT-1 SUFFIX
CASE 369-06
Plastic Package

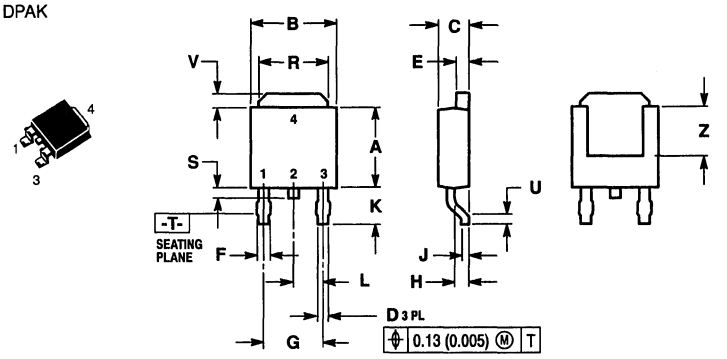




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 369-01 THRU -05 OBSOLETE, NEW STANDARD 369-06.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	5.97	6.22	0.235	0.245
B	6.35	6.73	0.250	0.265
C	2.19	2.38	0.086	0.094
D	0.69	0.88	0.027	0.035
E	0.84	1.01	0.033	0.040
F	0.94	1.19	0.037	0.047
G	2.29 BSC		0.090 BSC	
H	0.87	1.01	0.034	0.040
J	0.46	0.58	0.018	0.023
K	8.89	9.65	0.350	0.380
R	4.45	5.46	0.175	0.215
S	1.27	2.28	0.050	0.090
V	0.77	1.27	0.030	0.050

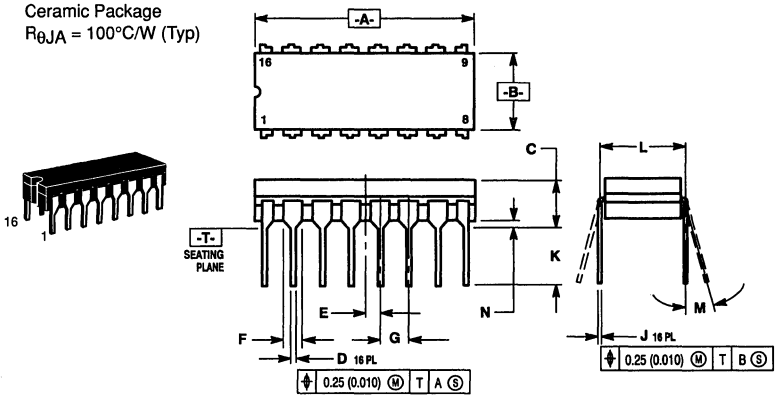
DT SUFFIX
CASE 369A-10
Plastic Package
DPAK



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 369A-01 THRU -03 OBSOLETE.
4. 369A-04 THRU -09 OBSOLETE, NEW STANDARD 369A-10.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	5.97	6.22	0.235	0.245
B	6.35	6.73	0.250	0.265
C	2.19	2.38	0.086	0.094
D	0.69	0.88	0.027	0.035
E	0.84	1.01	0.033	0.040
F	0.94	1.19	0.037	0.047
G	4.58 BSC		0.180 BSC	
H	0.87	1.01	0.034	0.040
J	0.46	0.58	0.018	0.023
K	2.60	2.89	0.102	0.114
L	2.29 BSC		0.090 BSC	
R	4.45	5.46	0.175	0.215
S	0.51	1.27	0.020	0.050
U	0.51	—	0.020	—
V	0.77	1.27	0.030	0.050
Z	3.51	—	0.138	—

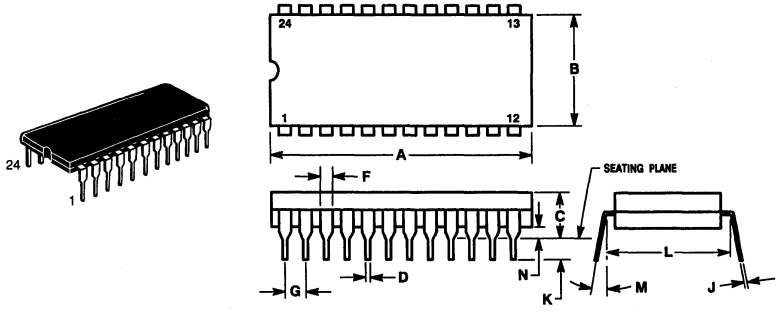
D, J, L, N SUFFIX
CASE 620-10
Ceramic Package
$R_{\theta JA}$ = 100°C/W (Typ)



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIM F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	19.05	19.93	0.750	0.785
B	6.10	7.49	0.240	0.295
C	—	5.08	—	0.200
D	0.39	0.50	0.015	0.020
E	1.27 BSC		0.050 BSC	
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
J	0.21	0.38	0.008	0.015
K	3.18	4.31	0.125	0.170
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.01	0.020	0.040

L SUFFIX
CASE 623-05
Ceramic Package
$R_{\theta JA}$ = 53°C/W (Typ)

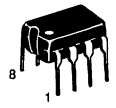


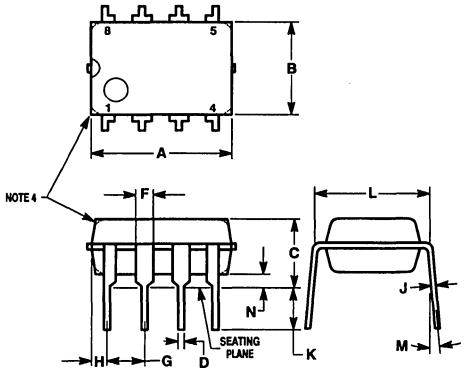
NOTES:
1. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
2. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION. (WHEN FORMED PARALLEL).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	31.24	32.77	1.230	1.290
B	12.70	15.49	0.500	0.610
C	4.06	5.59	0.160	0.220
D	0.41	0.51	0.016	0.020
F	1.27	1.52	0.050	0.060
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.27	0.020	0.050

13

DP1, N, P, P1 SUFFIX
CASE 626-05
Plastic Package
$R_{\theta JA}$ = 100°C/W (Typ)

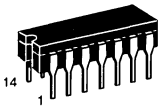


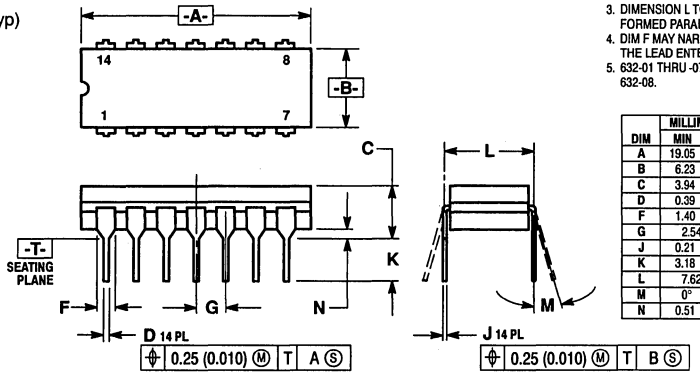


NOTES:
1. LEAD POSITIONAL TOLERANCE:
   ⌖ | ϕ 0.13 (0.005) Ⓜ | T | A Ⓜ | B Ⓜ
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
4. DIMENSIONS A AND B ARE DATUMS.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	—	10°	—	10°
N	0.76	1.01	0.030	0.040

J, F, L SUFFIX
CASE 632-08
Ceramic Package
$R_{\theta JA}$ = 100°C/W (Typ)
(TO-116)

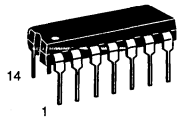


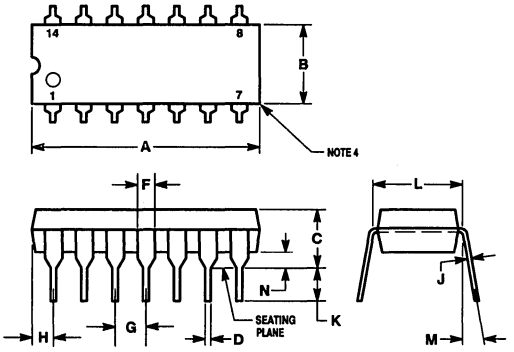


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIM F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.
5. 632-01 THRU -07 OBSOLETE, NEW STANDARD 632-08.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	19.05	19.94	0.750	0.785
B	6.23	7.11	0.245	0.280
C	3.94	5.08	0.155	0.200
D	0.39	0.50	0.015	0.020
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
J	0.21	0.38	0.008	0.015
K	3.18	4.31	0.125	0.170
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.01	0.020	0.040

N, P, N-14, P2 SUFFIX
CASE 646-06
Plastic Package
$R_{\theta JA}$ = 100°C/W (Typ)



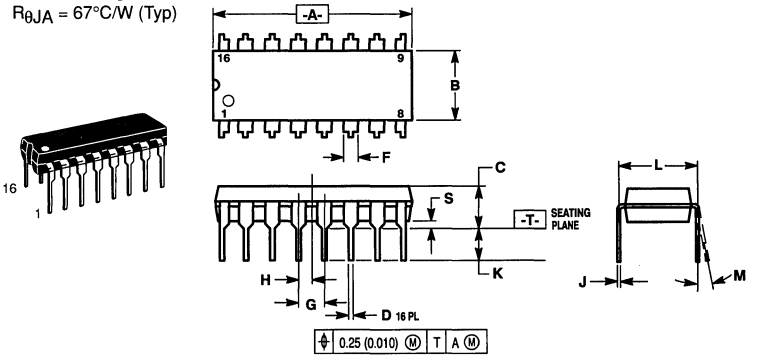


NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
4. ROUNDED CORNERS OPTIONAL.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	18.16	19.56	0.715	0.770
B	6.10	6.60	0.240	0.260
C	3.69	4.69	0.145	0.185
D	0.38	0.53	0.015	0.021
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	1.32	2.41	0.052	0.095
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	10°	0°	10°
N	0.39	1.01	0.015	0.039

13

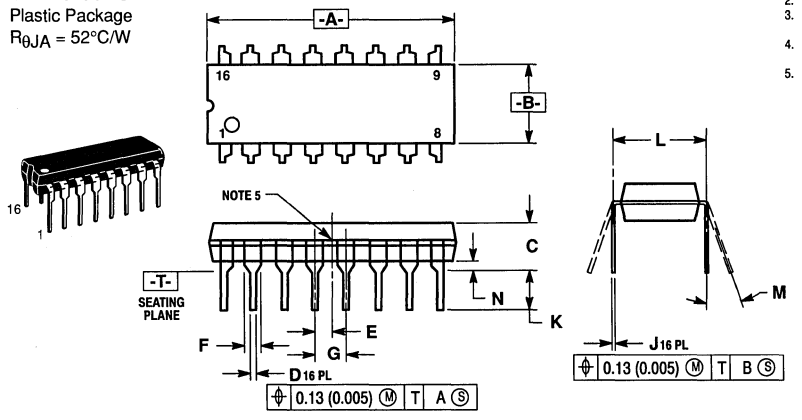
DP2, N, P, PC SUFFIX
CASE 648-08
Plastic Package
$R_{\theta JA}$ = 67°C/W (Typ)



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	18.80	19.55	0.740	0.770
B	6.35	6.85	0.250	0.270
C	3.69	4.44	0.145	0.175
D	0.39	0.53	0.015	0.021
F	1.02	1.77	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	1.27 BSC		0.050 BSC	
J	0.21	0.38	0.008	0.015
K	2.80	3.30	0.110	0.130
L	7.50	7.74	0.295	0.305
M	0°	10°	0°	10°
S	0.51	1.01	0.020	0.040

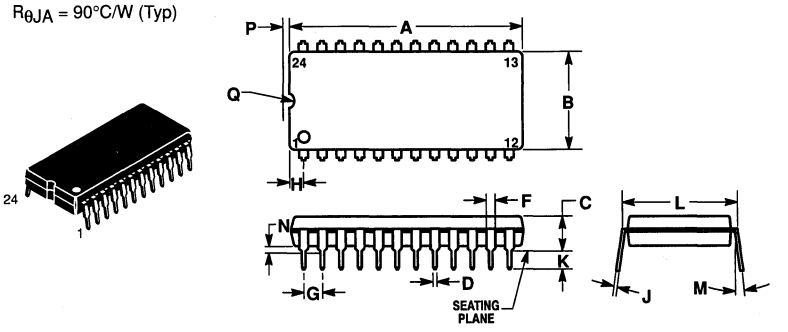
P, V SUFFIX
CASE 648C-03
Plastic Package
$R_{\theta JA}$ = 52°C/W



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. INTERNAL LEAD CONNECTION, BETWEEN 4 AND 5, 12 AND 13.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	18.80	21.34	0.740	0.840
B	6.10	6.60	0.240	0.260
C	3.69	4.69	0.145	0.185
D	0.38	0.53	0.015	0.021
E	1.27 BSC		0.050 BSC	
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	10°	0°	10°
N	0.39	1.01	0.015	0.040

P SUFFIX
CASE 649-03
Plastic Package
$R_{\theta JA}$ = 90°C/W (Typ)

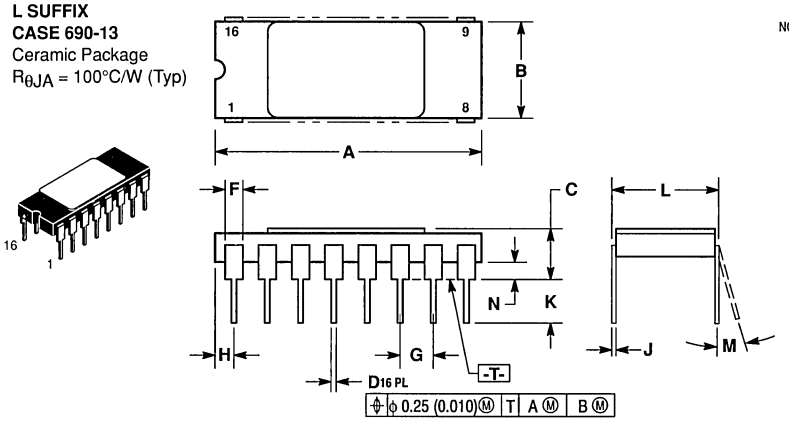


NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. 649-02 OBSOLETE, NEW STD 649-03 SEE ISSUE "C" FOR REFERENCE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	31.50	32.13	1.240	1.265
B	13.21	13.72	0.520	0.540
C	4.70	5.21	0.185	0.205
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	14.99	15.49	0.590	0.610
M	—	10°	—	10°
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

13

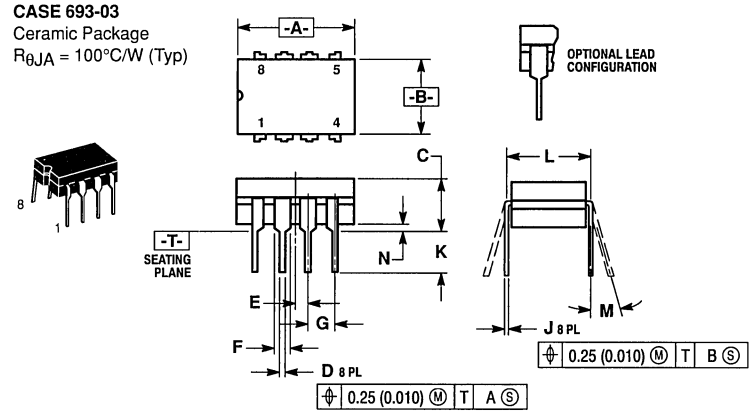
L SUFFIX
CASE 690-13
Ceramic Package
$R_{\theta JA}$ = 100°C/W (Typ)



NOTES:
1. -A- AND -B- ARE DATUMS.
2. -T- IS SEATING PLANE.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.
5. 690-11 AND 690-12 OBSOLETE. NEW STANDARD 690-13.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	20.07	20.57	0.790	0.810
B	7.11	7.74	0.280	0.305
C	2.67	4.19	0.105	0.165
D	0.38	0.53	0.015	0.021
F	0.76	1.52	0.030	0.060
G	2.54 BSC		0.100 BSC	
H	0.76	1.78	0.030	0.070
J	0.20	0.30	0.008	0.012
K	3.18	5.08	0.125	0.200
L	7.62 BSC		0.300 BSC	
M	—	10°	—	10°
N	0.38	1.52	0.015	0.060

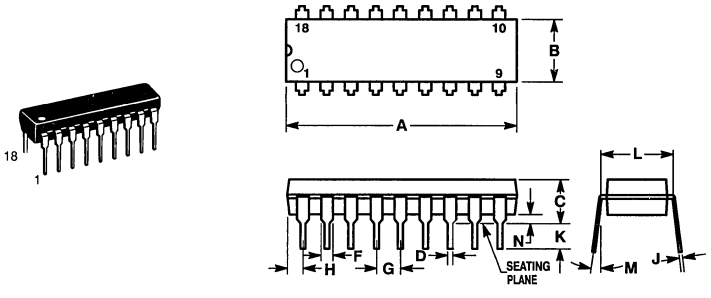
J-8, J, JG, U, Z SUFFIX
CASE 693-03
Ceramic Package
$R_{\theta JA}$ = 100°C/W (Typ)



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F FOR FULL LEADS. HALF LEADS AT LEAD POSITIONS 1, 4, 5, AND 8.
5. DIM F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.
6. 693-01 AND -02 OBSOLETE, NEW STANDARD 693-03.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.91	10.92	0.390	0.430
B	6.22	6.98	0.245	0.275
C	4.32	5.08	0.170	0.200
D	0.41	0.51	0.016	0.020
E	1.27 BSC		0.050 BSC	
F	1.27	1.65	0.050	0.065
G	2.54 BSC		0.100 BSC	
J	0.20	0.38	0.008	0.015
K	3.18	4.06	0.125	0.160
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

A, B, N, P SUFFIX
CASE 707-02
Plastic Package
$R_{\theta JA}$ = 100°C/W (Typ)

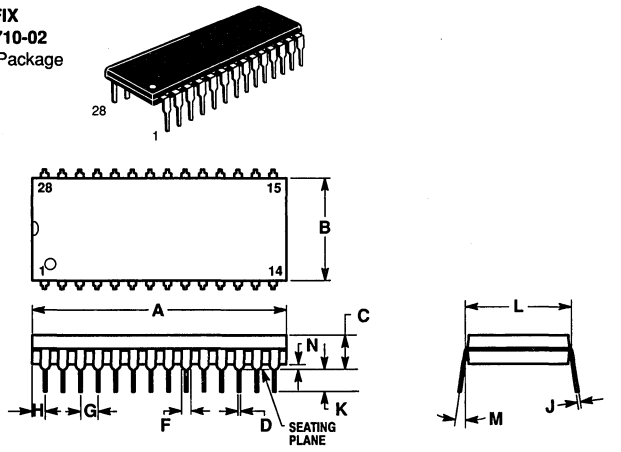


NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	22.22	23.24	0.875	0.915
B	6.10	6.60	0.240	0.260
C	3.56	4.57	0.140	0.180
D	0.36	0.56	0.014	0.022
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
H	1.02	1.52	0.040	0.060
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

13

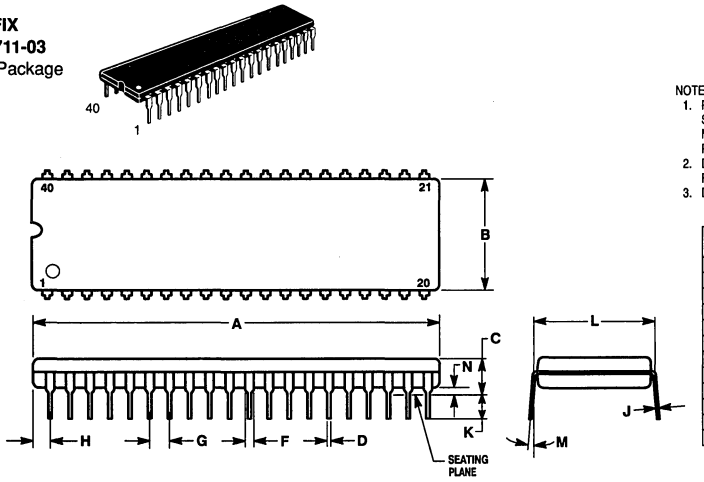
P SUFFIX
CASE 710-02
Plastic Package



NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
4. 710-01 OBSOLETE, NEW STANDARD 710-02.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	36.45	37.21	1.435	1.465
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

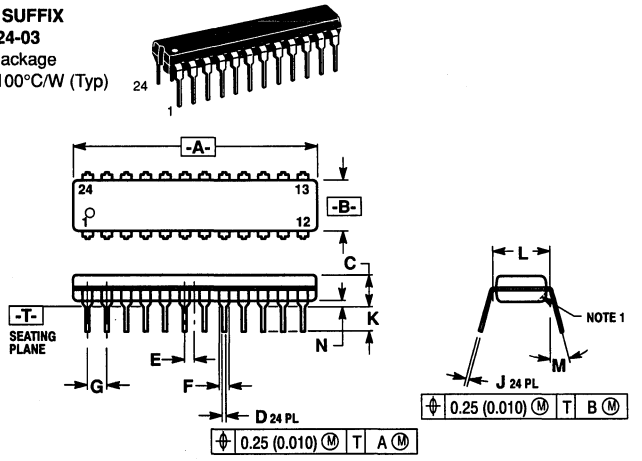
P SUFFIX
CASE 711-03
Plastic Package



NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	51.69	52.45	2.035	2.065
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0 °	15 °	0 °	15 °
N	0.51	1.02	0.020	0.040

F, P, P-3 SUFFIX
CASE 724-03
Plastic Package
$R_{\theta JA}$ = 100°C/W (Typ)

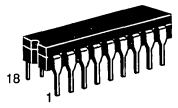


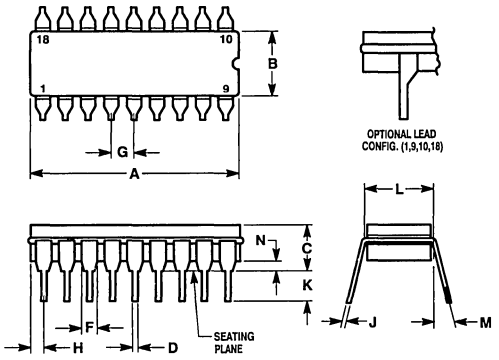
NOTES:
1. CHAMFERRED CONTOUR OPTIONAL.
2. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	31.25	32.13	1.230	1.265
B	6.35	6.85	0.250	0.270
C	3.69	4.44	0.145	0.175
D	0.38	0.51	0.015	0.020
E	1.27 BSC		0.050 BSC	
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
J	0.18	0.30	0.007	0.012
K	2.80	3.55	0.110	0.140
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.01	0.020	0.040

13

J, L SUFFIX
CASE 726-04
Ceramic Package
$R_{\theta JA}$ = 100°C/W (Typ)

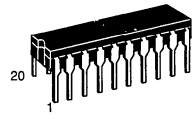


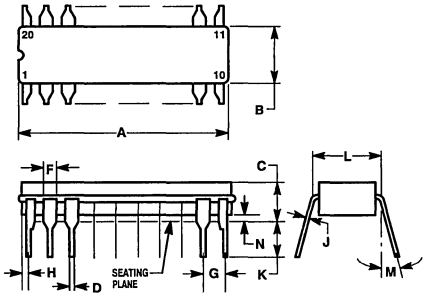


NOTES:
1. LEADS, TRUE POSITIONED WITHIN 0.25 mm (0.010) DIA. AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
2. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIM "A" & "B" INCLUDES MENISCUS.
4. "F" DIMENSION IS FOR FULL LEADS. "HALF" LEADS ARE OPTIONAL AT LEAD POSITIONS 1, 9, 10, AND 18.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	22.35	23.11	0.880	0.910
B	6.10	7.49	0.240	0.295
C	—	5.08	—	0.200
D	0.38	0.53	0.015	0.021
F	1.40	1.78	0.055	0.070
G	2.54 BSC		0.100 BSC	
H	0.51	1.14	0.020	0.045
J	0.20	0.30	0.008	0.012
K	3.18	4.32	0.125	0.170
L	7.62 BSC		0.300 BSC	
M	0 °	15 °	0 °	15 °
N	0.51	1.02	0.020	0.040

L SUFFIX
CASE 732-03
Ceramic Package
$R_{\theta JA}$ = 75°C/W (Typ)

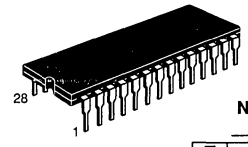


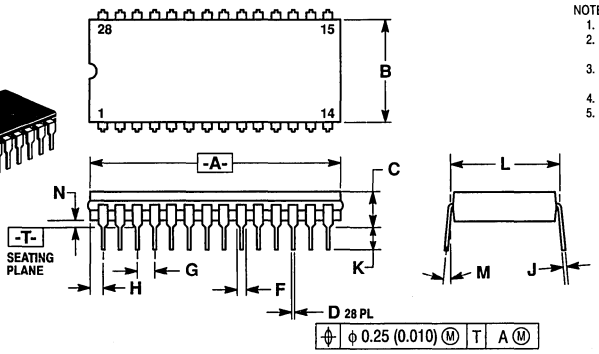


NOTES:
1. LEADS WITHIN 0.25 mm (0.010) DIA., TRUE POSITION AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
2. DIM L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIM A AND B INCLUDES MENISCUS.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	23.88	25.15	0.940	0.990
B	6.60	7.49	0.260	0.295
C	3.81	5.08	0.150	0.200
D	0.38	0.56	0.015	0.022
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	0.51	1.27	0.020	0.050
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.25	1.02	0.010	0.040

L SUFFIX
CASE 733-04
Ceramic Package

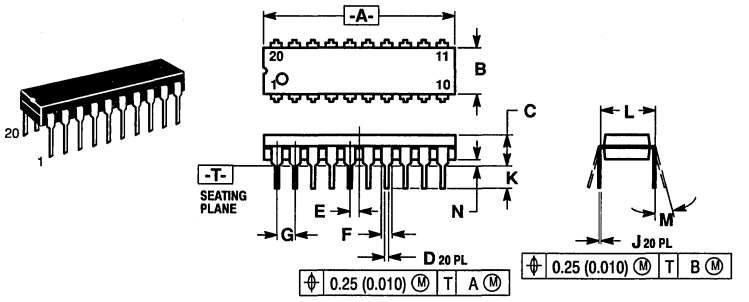




NOTES:
1. DIM A AND B INCLUDES MENISCUS.
2. DIM -L- TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1982.
4. CONTROLLING DIM: INCH.
5. 733-03 OBSOLETE, NEW STANDARD 733-04.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	36.45	37.84	1.435	1.490
B	12.70	15.36	0.500	0.605
C	4.06	5.84	0.160	0.230
D	0.38	0.55	0.015	0.022
F	1.27	1.65	0.050	0.065
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.27	0.020	0.050

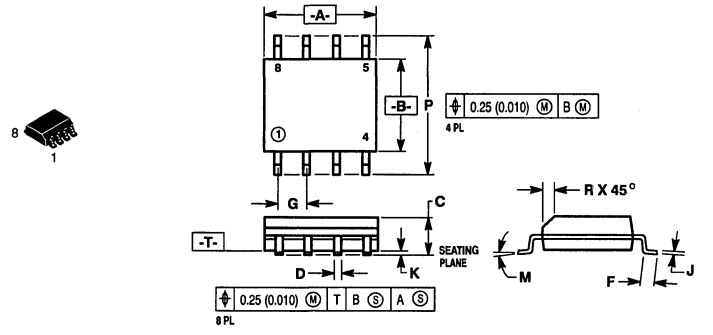
P SUFFIX
CASE 738-03
Plastic Package
$R_{\theta JA}$ = 75°C/W (Typ)



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION "L" TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
5. 738-02 OBSOLETE, NEW STANDARD 738-03.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	25.66	27.17	1.010	1.070
B	6.10	6.60	0.240	0.260
C	3.81	4.57	0.150	0.180
D	0.39	0.55	0.015	0.022
E	1.27 BSC		0.050 BSC	
F	1.27	1.77	0.050	0.070
G	2.54 BSC		0.100 BSC	
J	0.21	0.38	0.008	0.015
K	2.80	3.55	0.110	0.140
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.01	0.020	0.040

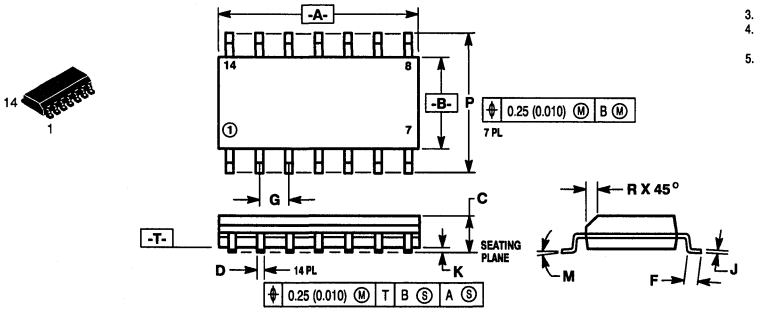
D SUFFIX
CASE 751-03
Plastic Package
(SO-8, SOP-8)



NOTES:
1. DIMENSIONS "A" AND "B" ARE DATUMS AND "T" IS A DATUM SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIM: MILLIMETER.
4. DIMENSION "A" AND "B" DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.196
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.18	0.25	0.007	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

D SUFFIX
CASE 751A-02
Plastic Package
(SO-14)

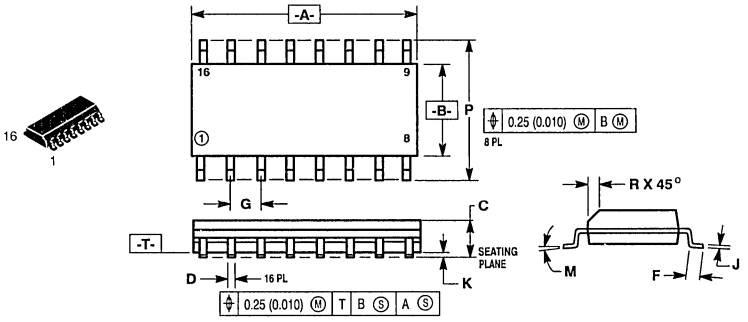


NOTES:
1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION: MILLIMETER.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

13

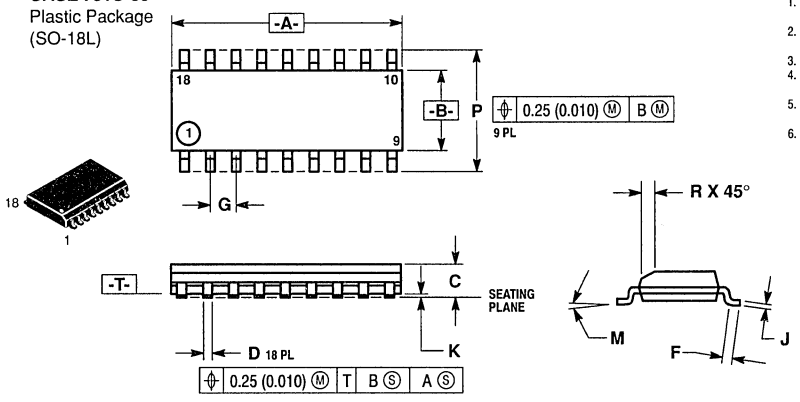
D SUFFIX
CASE 751B-03
Plastic Package
(SO-16)



NOTES:
1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION: MILLIMETER.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

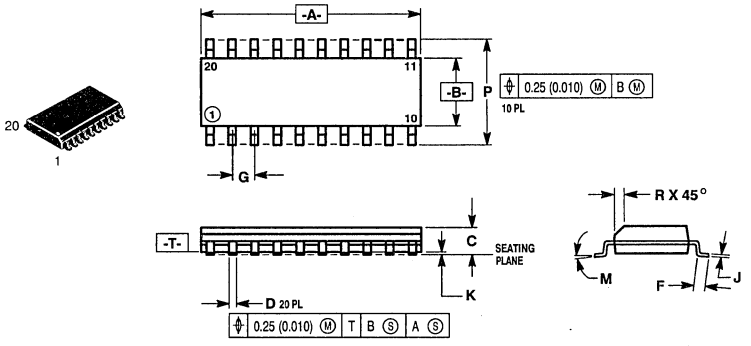
DW SUFFIX
CASE 751C-03
Plastic Package
(SO-18L)



NOTES:
1. DIMENSIONS "A" AND "B" ARE DATUMS AND "T" IS A DATUM SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIM: MILLIMETER.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
6. 751C-01, AND 02 OBSOLETE, NEW STANDARD 751C-03.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	11.40	11.70	0.449	0.460
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

DW SUFFIX
CASE 751D-03
Plastic Package
(SO-20L)

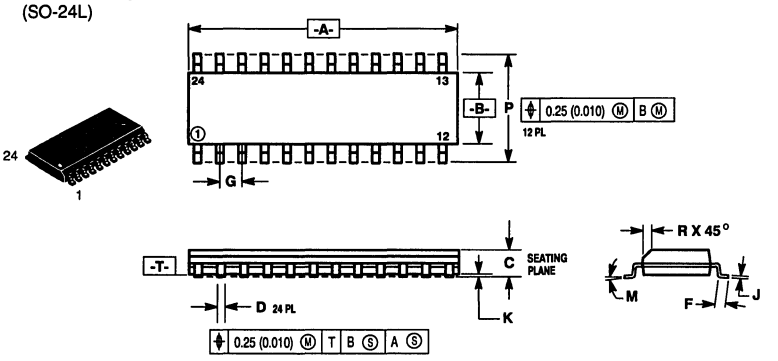


NOTES:
1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION: MILLIMETER.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	12.65	12.95	0.499	0.510
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

13

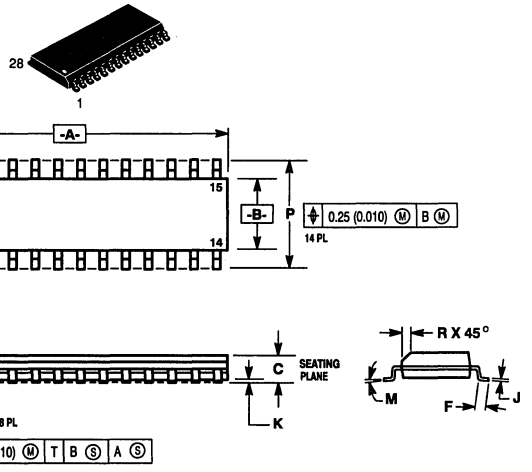
DW SUFFIX
CASE 751E-03
Plastic Package
(SO-24L)



NOTES:
1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION: MILLIMETER.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	15.25	15.54	0.601	0.612
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.41	0.90	0.016	0.035
G	1.27 BSC		0.050 BSC	
J	0.229	0.317	0.0090	0.0125
K	0.127	0.292	0.0050	0.0115
M	0°	8°	0°	8°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

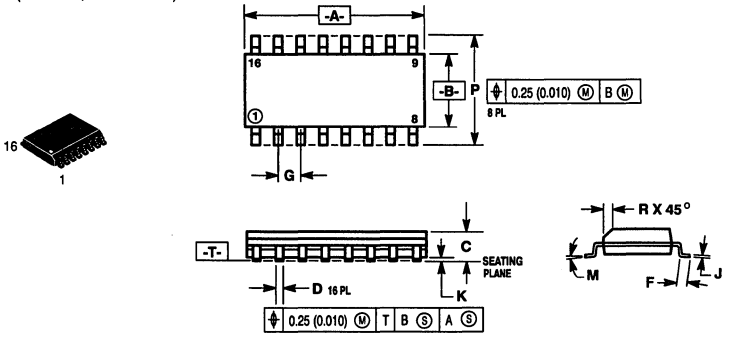
DW SUFFIX
CASE 751F-03
Plastic Package
(SO-28L)



NOTES:
1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION: MILLIMETER.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	17.80	18.05	0.701	0.711
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.41	0.90	0.016	0.035
G	1.27 BSC		0.050 BSC	
J	0.229	0.317	0.0090	0.0125
K	0.127	0.292	0.0050	0.0115
M	0°	8°	0°	8°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

DW SUFFIX
CASE 751G-01
Plastic Package
(SO-16L, SOP-8+8L)

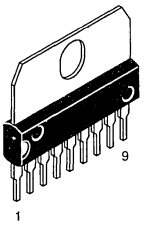


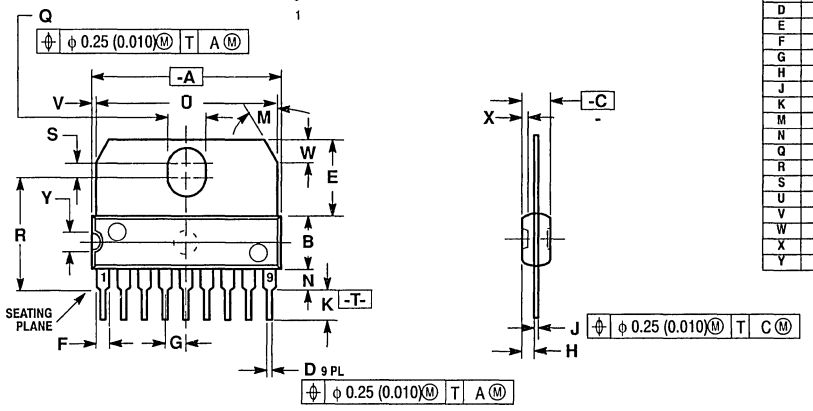
NOTES:
1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIMENSION: MILLIMETER.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	10.15	10.45	0.400	0.411
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

13

CASE 762-01
Plastic Medium Power Package
(SIP-9)
$R_{\theta JA}$ = 70°C/W(Typ)
$R_{\theta JC}$ = 15°C/W(Typ)

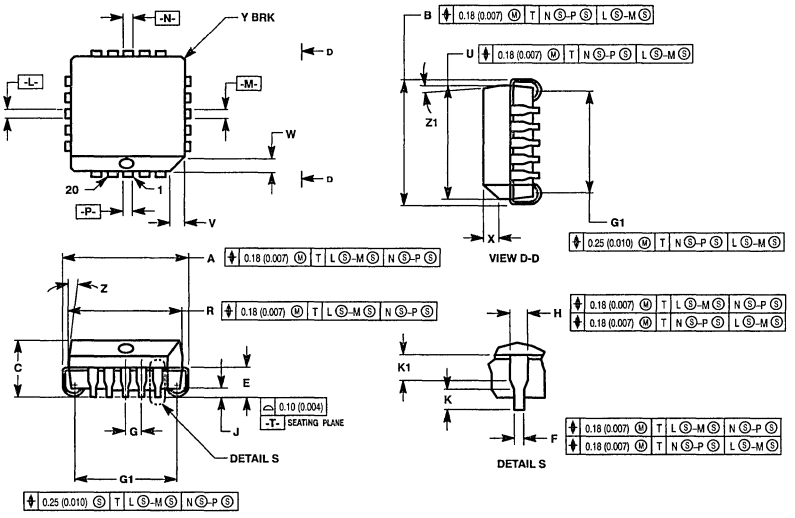




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1982.
2. CONTROLLING DIMENSION: MILLIMETER

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	22.40	23.00	0.873	0.897
B	6.40	6.60	0.252	0.260
C	3.45	3.65	0.135	0.143
D	0.40	0.55	0.015	0.021
E	9.35	9.60	0.368	0.377
F	1.40	1.60	0.055	0.062
G	2.54 BSC		0.100 BSC	
H	1.51	1.71	0.059	0.067
J	0.360	0.400	0.014	0.015
K	3.95	4.20	0.155	0.165
M	30° BAC		30° BAC	
N	2.50	2.70	0.099	0.106
Q	3.15	3.45	0.124	0.135
R	13.60	13.90	0.535	0.547
S	1.65	1.95	0.064	0.076
U	22.00	22.20	0.866	0.874
V	0.55	0.75	0.021	0.029
W	2.89 BSC		0.113 BSC	
X	0.65	0.75	0.025	0.029
Y	2.70	2.80	0.106	0.110

FN SUFFIX
CASE 775-02
Plastic Package
(PLCC-20)
$R_{\theta JA}$ = 72°C/W(Typ)
(5k SQML)

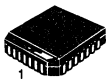


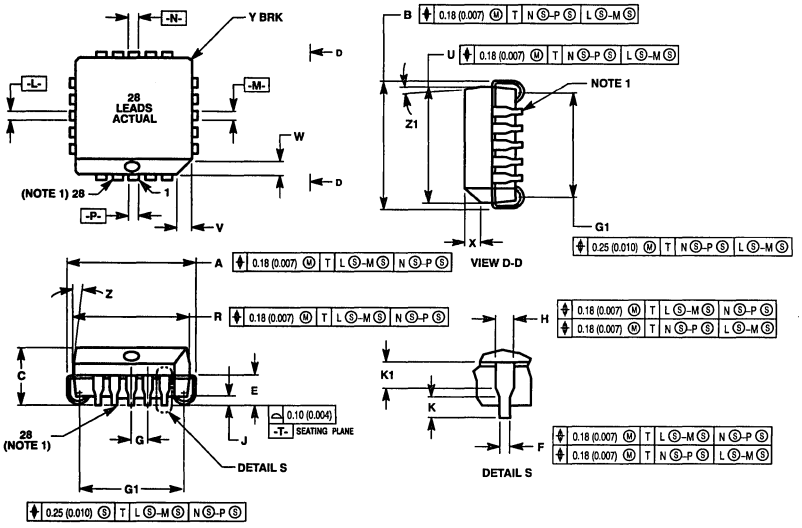
NOTES:
1. DATUMS -L-, -M-, -N-, AND -P- DETERMINED WHERE TOP OF LEAD SHOULDER EXIT PLASTIC BODY AT MOLD PARTING LINE.
2. DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
3. DIM R AND U DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.25 (0.010) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.78	10.03	0.385	0.395
B	9.78	10.03	0.385	0.395
C	4.20	4.57	0.165	0.180
E	2.29	2.79	0.090	0.110
F	0.33	0.48	0.013	0.019
G	1.27 BSC		0.050 BSC	
H	0.66	0.81	0.026	0.032
J	0.51	—	0.020	—
K	0.64	—	0.025	—
R	8.89	9.04	0.350	0.356
U	8.89	9.04	0.350	0.356
V	1.07	1.21	0.042	0.048
W	1.07	1.21	0.042	0.048
X	1.07	1.42	0.042	0.056
Y	—	0.50	—	0.020
Z	2°	10°	2°	10°
G1	7.88	8.38	0.310	0.330
K1	1.02	—	0.040	—
Z1	2°	10°	2°	10°

13

FN SUFFIX
CASE 776-02
Plastic Package
(PLCC–28)
$R_{\theta JA}$ = 66°C/W(Typ)
(5k SQML)

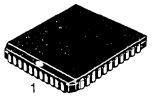


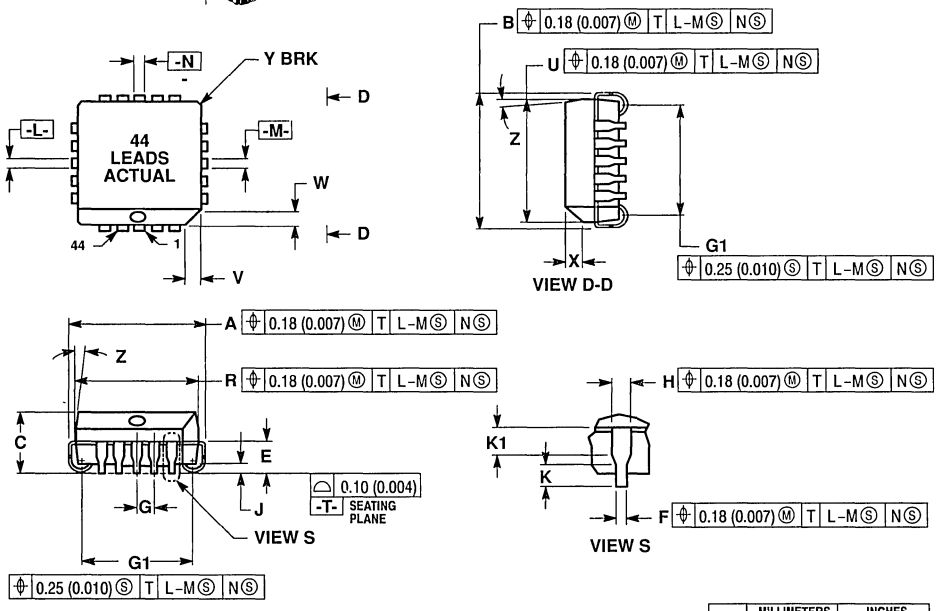


NOTES:
1. **DUE TO SPACE LIMITATION, CASE 776-02 SHALL BE REPRESENTED BY A GENERAL (SMALLER) CASE OUTLINE DRAWING RATHER THAN SHOWING ALL 28 LEADS.**
2. DATUMS -L-, -M-, -N-, AND -P- DETERMINED WHERE TOP OF LEAD SHOULDER EXIT PLASTIC BODY AT MOLD PARTING LINE.
3. DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
4. DIM R AND U DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.25 (0.010) PER SIDE.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
6. CONTROLLING DIMENSION: INCH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	12.32	12.57	0.485	0.495
B	12.32	12.57	0.485	0.495
C	4.20	4.57	0.165	0.180
E	2.29	2.79	0.090	0.110
F	0.33	0.48	0.013	0.019
G	1.27 BSC		0.050 BSC	
H	0.66	0.81	0.026	0.032
J	0.51	—	0.020	—
K	0.64	—	0.025	—
R	11.43	11.58	0.450	0.456
U	11.43	11.58	0.450	0.456
V	1.07	1.21	0.042	0.048
W	1.07	1.21	0.042	0.048
X	1.07	1.42	0.042	0.056
Y	—	0.50	—	0.020
Z	2°	10°	2°	10°
G1	10.42	10.92	0.410	0.430
K1	1.02	—	0.040	—
Z1	2°	10°	2°	10°

FN SUFFIX
CASE 777-02
Plastic Package

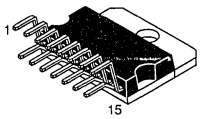


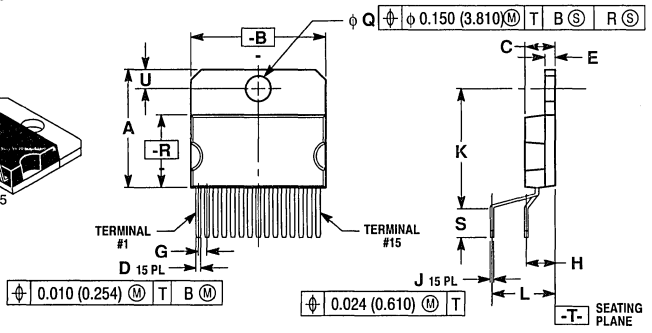


NOTES:
1. **DUE TO SPACE LIMITATION, CASE 777-02 SHALL BE REPRESENTED BY A GENERAL (SMALLER) CASE OUTLINE DRAWING RATHER THAN SHOWING ALL 44 LEADS.**
2. DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
3. DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
4. DIM R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.25 (0.010) PER SIDE.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
6. CONTROLLING DIMENSION: INCH.
7. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO .012 (.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
8. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN .037 (.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN .025 (.635).
9. 777-01 IS OBSOLETE, NEW STANDARD 777-02.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	17.40	17.65	0.685	0.695
B	17.40	17.65	0.685	0.695
C	4.20	4.57	0.165	0.180
E	2.29	2.79	0.090	0.110
F	0.33	0.48	0.013	0.019
G	1.27 BSC		0.050 BSC	
H	0.66	0.81	0.026	0.032
J	0.51	—	0.020	—
K	0.64	—	0.025	—
R	16.51	16.66	0.650	0.656
U	16.51	16.66	0.650	0.656
V	1.07	1.21	0.042	0.048
W	1.07	1.21	0.042	0.048
X	1.07	1.42	0.042	0.056
Y	—	0.50	—	0.020
Z	2°	10°	2°	10°
G1	15.50	16.00	0.610	0.630
K1	1.02	—	0.040	—

T SUFFIX
CASE 821C-02
Plastic Package
(15-Pin ZIP)

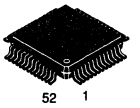


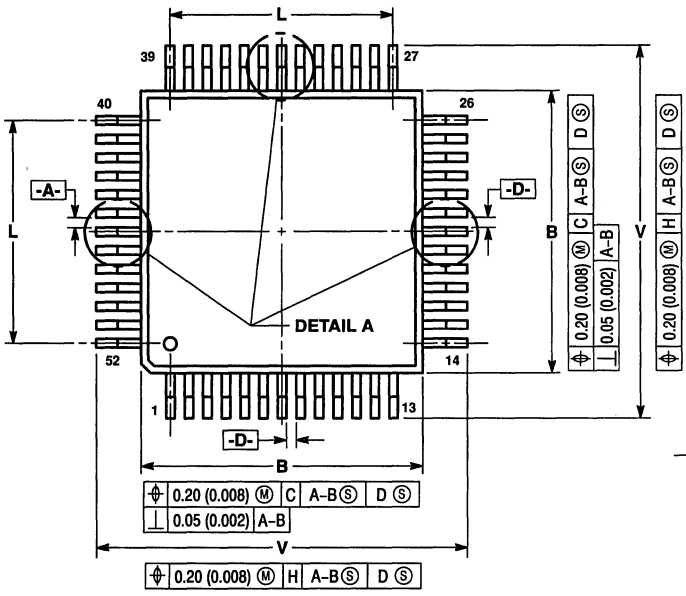


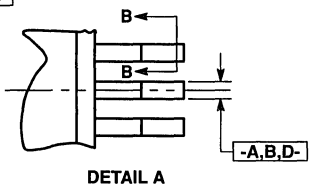
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION R DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
5. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 (0.250).
6. 821C-01 OBSOLETE, NEW STANDARD 821C-02.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	17.374	17.627	0.684	0.694
B	19.914	20.116	0.784	0.792
C	4.395	4.597	0.173	0.181
D	0.610	0.787	0.024	0.031
E	1.473	1.574	0.058	0.062
G	1.270 BSC		0.050 BSC	
H	4.293 BSC		0.169 BSC	
J	0.458	0.609	0.018	0.024
K	17.526	18.034	0.690	0.710
L	9.373 BSC		0.369 BSC	
Q	3.760	3.835	0.148	0.151
R	10.567	10.820	0.416	0.426
S	4.141	4.470	0.163	0.176
U	2.794 BSC		0.110 BSC	

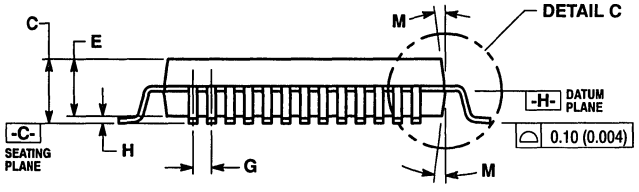
FU SUFFIX
CASE 848B-02
Plastic Package
(52 Pin Thin
Quad Flat Pack)

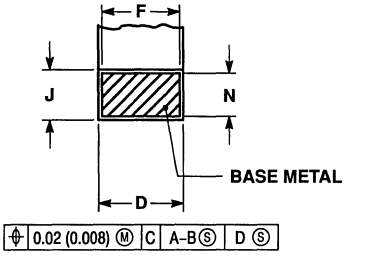




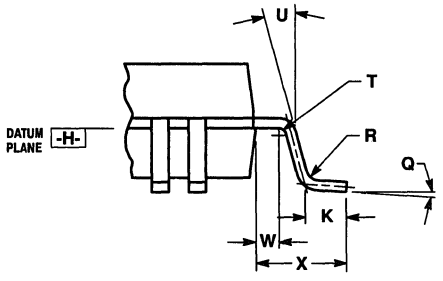


DETAIL A





SECTION B–B



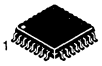
DETAIL C

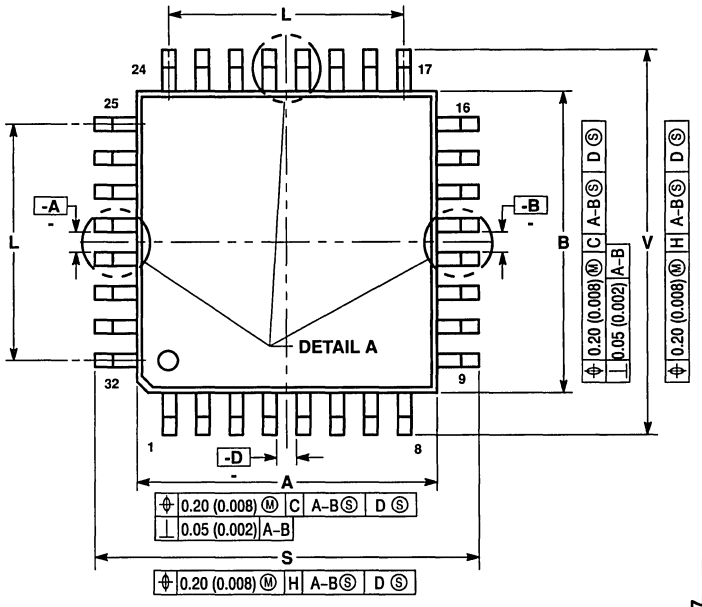
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -A-, -B- AND -D- TO BE DETERMINED AT SEATING PLANE -C-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -C-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

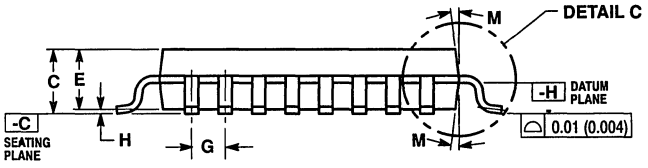
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.90	10.10	0.390	0.398
B	9.90	10.10	0.390	0.398
C	2.10	2.45	0.083	0.096
D	0.22	0. 38	0.009	0.015
E	2.00	2.10	0.079	0.083
F	0.22	0.33	0.009	0.013
G	0.65 BSC		0.026 BSC	
H	—	0.25	—	0.010
J	0.13	0.23	0.005	0.009
K	0.65	0.95	0.026	0.037
L	7.80 REF		0.307 REF	
M	5°	10°	5°	10°
N	0.13	0.17	0.005	0.007
Q	0°	7°	0°	7°
R	0.13	0.30	0.005	0.012
S	12.95	13.45	0.510	0.530
T	0.13	—	0.005	—
U	0°	—	0°	—
V	12.95	13.45	0.510	0.530
W	0.35	0.45	0.014	0.018
X	1.6 REF		0.063 REF	

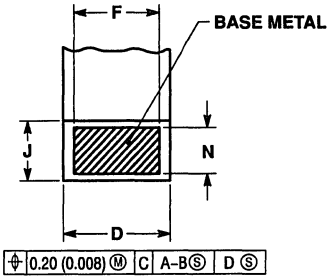
13

FU SUFFIX
CASE 873-01
Plastic Package
(32 Pin Flat Package)

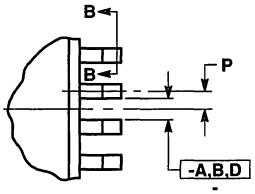




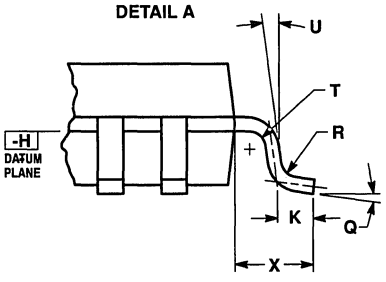




SECTION B



DETAIL A

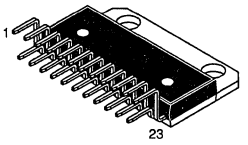


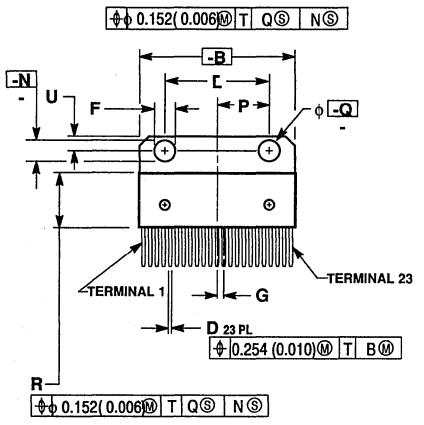
DETAIL C

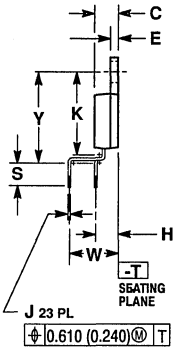
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -A-, -B- AND -D- TO BE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -C-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	6.95	7.10	0.274	0.280
B	6.95	7.10	0.274	0.280
C	1.40	1.60	0.055	0.063
D	0.273	0.373	0.010	0.015
E	1.30	1.50	0.051	0.059
F	0.273	—	0.010	—
G	0.80 BSC		0.031 BSC	
H	—	0.20	—	0.008
J	0.119	0.197	0.005	0.008
K	0.33	0.57	0.013	0.022
L	5.6 REF		0.220 REF	
M	6°	8°	6°	8°
N	0.119	0.135	0.005	0.005
P	0.40 BSC		0.016 BSC	
Q	5°	10°	5°	10°
R	0.15	0.25	0.006	0.010
S	8.85	9.15	0.348	0.360
T	0.15	0.25	0.006	0.010
U	5°	11°	5°	11°
V	8.85	9.15	0.348	0.360
X	1.0 REF		0.039 REF	

T SUFFIX
CASE 894-01
Plastic Package
(23-Pin ZIP)



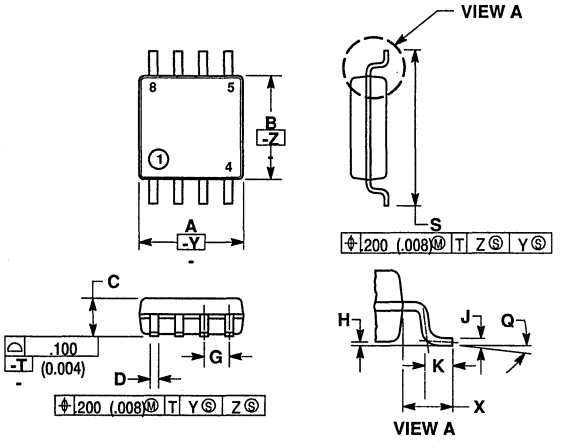




NOTES:
1. DIMENSIONING AND TOLERANCEING PER ANSI Y14.5M, 1982.
2. CONTROLING DIMENSION INCH.
3. DIMENSION R DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
5. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.250 (0.010).
6. OVERALL LEAD LENGTH DOES NOT INCLUDE LEAD FINISH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	17.374	17.627	0.684	0.694
B	30.048	30.302	1.183	1.193
C	4.445	4.547	0.175	0.179
D	0.660	0.787	0.026	0.031
E	1.473	1.574	0.058	0.062
F	4.191	4.445	0.165	0.175
G	1.270 BSC		0.050 BSC	
H	4.293 BSC		0.169 BSC	
J	0.356	0.508	0.014	0.020
K	15.875	16.231	0.625	0.639
L	19.558	20.066	0.770	0.790
M	4.039 BSC		0.159 BSC	
N	3.760	3.861	0.148	0.152
P	9.906 BSC		0.390 BSC	
Q	3.760	3.861	0.148	0.152
R	10.566	10.770	0.416	0.424
S	4.089	4.394	0.161	0.173
U	2.667	2.921	0.105	0.115
Y	17.577	17.932	0.692	0.706
W	9.373 BSC		0.369 BSC	

F SUFFIX
CASE 904-01
Plastic Package



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. MOLD PROTRUSION SHALL NOT EXCEED .150 (.006) PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	5.100	5.450	0.201	0.214
B	5.100	5.400	0.201	0.216
C	—	2.050	—	0.080
D	0.350	0.500	0.014	0.001
G	1.270 BASIC		0.050 BASIC	
H	0.050	0.200	0.002	0.007
J	0.180	0.270	0.008	0.010
K	0.500	0.850	0.020	0.033
Q	0°	10°	0°	10°
S	7.400	8.200	0.292	0.322
X	1.260 REF		0.0496 REF	

13

Quality and Reliability Assurance

In Brief . . .

The word quality has been used to describe many things, such as fitness for use, customer satisfaction, customer enthusiasm, what the customer says quality is, etc. These descriptions convey important truths, however, quality should be described in a way that precipitates immediate action. With that in mind, quality can be described as reduction of variability around a target, so that conformance to customer requirements and possibly expectations can be achieved in a cost effective way. This definition provides direction and potential for immediate action for a person desiring to improve quality.

The definition of quality as described above can be applied to a task, process or a whole company. If we are to reap the benefits of quality and obtain a competitive advantage, quality must be applied to the whole company.

Implementation of quality ideas company wide requires a quality plan showing: a philosophy (belief) of operation, measurable goals, training of individuals and methods of communicating this philosophy of operation to the whole organization.

Motorola, for example, believes that quality and reliability are the responsibility of every person. Participative Management is the process by which problem solving and quality improvement are facilitated at all levels of the organization through crossfunctional teams. Continuous improvement for the individual is facilitated by a broad educational program covering onsite, university and college courses. Motorola University provides leadership and administers this educational effort on a company wide basis.

Another key belief is that quality excellence is accomplished by people doing things right the first time and committed to never ending improvement. The Six Sigma (6σ) challenge is designed to convey and facilitate the idea of continuous improvement at all levels.

Page

Quality Concepts

Quality improvement for a task or a process can be quickly described in terms of the target, current status with respect to target (variability), reduction of variability (commitment to never ending improvement), customer requirements (who receives output, what are a person's requirements/ expectations) and economics (cost of nonconformance, loss function, etc.).

Application of quality to the whole company has come to be known by such names as **"Total Quality Control" (TQC); "Company Wide Quality Control" (CWQC); "Total Quality Excellence" or "Total Quality Engineering" (TQE); "Total Quality Involvement" (TQI).** These names attempt to convey the idea that quality is a process (a way of acting continuously) rather than a program (implying a beginning and an end). Nevertheless for this process to be successful it must be able to show measurable results.

"**Six Sigma** is the required capability level to approach the standard. The **standard** is **zero defects**. Our goal is to be Best-in-Class in product, sales and service." (For a more detailed explanation, contact your Motorola Representative for a pamphlet of the Six Sigma Challenge.)

Quick insight into six sigma is obtained if we realize that a six sigma process has variability which is one half of the variation allowed (tolerance, spread) by the customer requirements (i.e. natural variation is one half of the customer specification range for a given characteristic). When six sigma is achieved, virtually zero defects are observed in the output of a process/product even allowing for potential process shifts (Figure 1).

Policies, objectives and five year plans are the mechanisms for communicating the key beliefs and measurable goals to all personnel and continuously keeping them in focus. This is done at the corporate, sector, group, division, and department levels.

The Analog Division, for example, evaluates performance to the corporate goals of **10 fold improvement by 1989; 100 fold improvement by 1991** and achievement of **six sigma capability by 1992** by utilizing indices such as Outgoing Electrical and Visual Mechanical Quality **(AOQ)** in terms of PPM (parts per million or sometimes given in parts per billion); **% of devices with zero PPM ; product quality returns** (RMR); number of processes/products with specified **capability indices (cp, cpk); six sigma capability roadmaps; failure rates for various reliability tests** (operating life, temperature humidity bias, hast, temperature cycling, etc.); **on-time delivery; customer product evaluation and failure analysis turnaround; cost of nonconformance; productivity improvement and personnel development.**

Figure 2 shows the improvement in electrical outgoing quality for analog products over recent years in a normalized form. Figure 3 shows the number of parts with zero PPM over a period of time.

Documentation control is an important part of **statistical process control. Process mapping** (flow charting etc.) with documentation identified allows visualization and therefore optimization of the process. Figure 4 shows a portion of a flow chart for wafer fabrication. **Control plans** are an important part of Statistical Process Control, these plans identify in detail critical points where data for process control is taken, parameters measured, frequency of measurements, type of control device used, measuring equipment, responsibilities and reaction plans. Figure 5 shows a portion of a control plan for wafer fabrication. Six sigma progress is tracked by roadmaps based on the six sigma process, a portion of which is shown on Figure 6.

On-time delivery is of great importance, with the current emphasis on **just-in-time** systems. Tracking is done on an overall basis, and at the device levels.

Figure 1. A Six Sigma Process Has Virtually Zero Defects Allowing for 1.5σ Shift

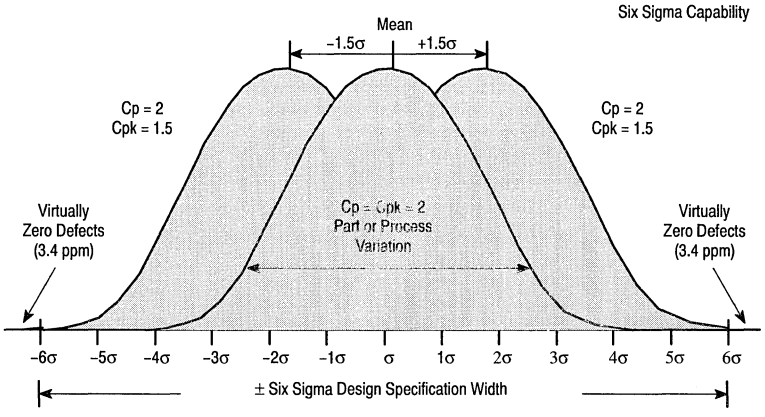


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Figure 2. Motorola Logic & Analog Technologies Group Electrical AOQ

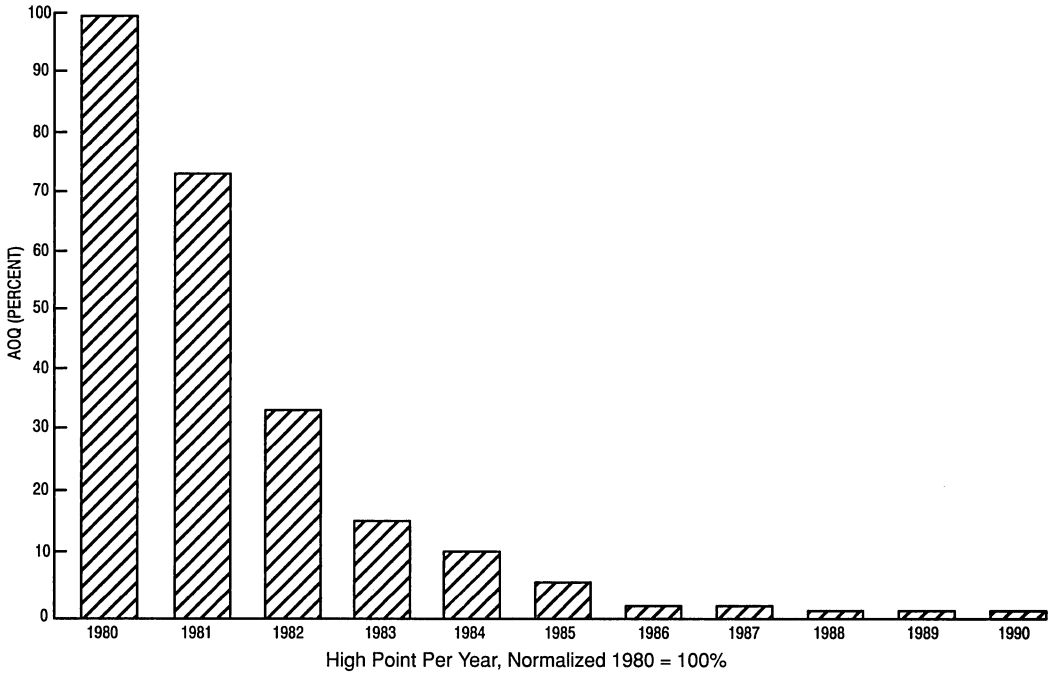

Figure 3. Percentage of Parts with Zero PPM AOQ

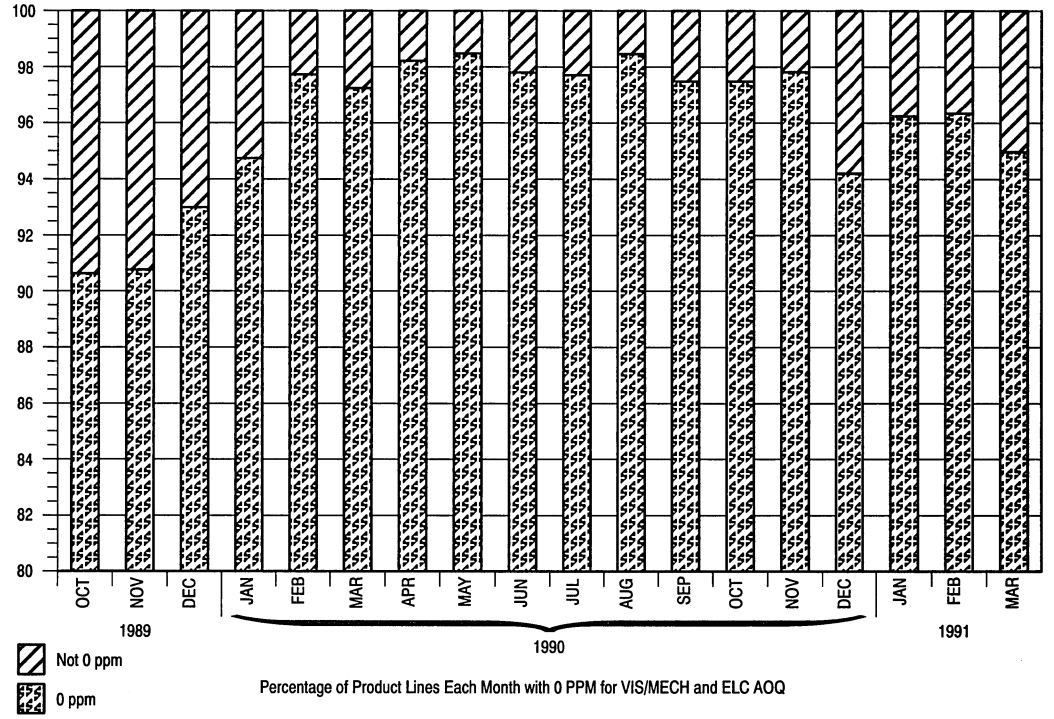

Figure 4. Portion of a Process Flow Chart From Wafer Fab, Showing Documentation Control and SPC

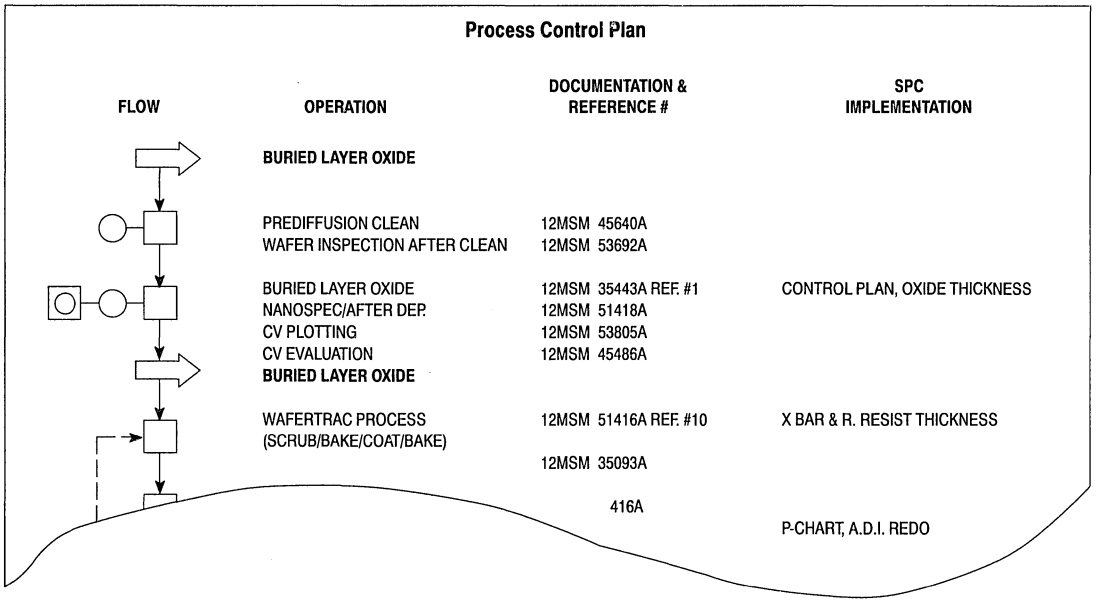

Figure 5. Part of a Wafer Fab Control Plan, Showing Statistical Process Control Details

Characteristics:	Code	Description	Code	Description
	A	VISUAL DEFECTS	E	FILM SHEET RESISTANCE
	B	VISUAL DEFECTS . . . MICROSCOPE	F	REFRACTIVE INDEX
	C	PARTICLE . . . MONITOR	G	CRITICAL DIMENSION
	D	FILM THICKNESS	H	CV PLOT

Process Location	Ref. No.	Characteristic Affected	Part/Process Detail	Measurements Method	Analysis Methods	Frequency Sample Size	Reaction Plan: Point out of Limit (3) (4)
B.L. OXIDE	1	D	OXIDE THICKNESS	NANOMETRIC	CONTROL GRAPH	EVERY RUN 3 WFR/RUN	IMPOUND LOT (1) ADJUST TIME TO CENTER PROCESS PER SPEC
EPI	2	D	THICKNESS	DIGILAB	$\bar{X}$ R CHART	EVERY RUN 5 SITES/WFR	IMPOUND LOT (1) NOTIFY ENGR.
QA		D	THICKNESS	DIGILAB	$\bar{X}$ R CHART	1WFR/SHIFT 5 SITES/WFR	IMPOUND LOT (2) NOTIFY ENGR.
		E	FILM RESISTIVITY	4PT PROBE	$\bar{X}$ R CHART	EVERY RUN 5 SITES/WFR	IMPOUND LOT (1) NOTIFY ENGR.
QA		E	FILM RESISTIVITY	4PT PROBE	$\bar{X}$ R CHART	1WFR/SHIFT 5 SITES/WFR	IMPOUND LOT (2) NOTIFY ENGR.
DEEP				4PT PROBE	MOVING R	EVERY LOT 1 CTRL WFR PER LOT	IMPOUND LOT NOTIFY ENGR.

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Figure 6. Portion of Six Sigma (6σ) Roadmap Showing Steps to Six Sigma Capability

STEP	±6σ Summary
1. Identify critical characteristics	• Product Description • Marketing • Industrial Design • R&D/Developmental Engineering • Actual or Potential Customers
2. Determine specified product elements contributing to critical characteristics	• Critical Characteristics Matrix • Cause-and-Effect and Ishikawa Diagrams • Success Tree/Fault Tree Analysis • Component Search or Other Forms of Planned Experimentation • FMECA (Failure Mode Effects and Critical Analysis)
3. For each product element, determine the process step or process choice that affects or controls required performance	• Planned Experiments • Computer-Aided Simulation • TOP/Process Engineering Studies • Multi-Vari Analysis • Comparative Experiments
4. Determine maximum (real) allowable tolerance for each and process	• Graphing Techniques • Engineering Handbooks • Planned Experiments • Optimization, Especially Response Surface Methodology

Reliability Concepts

Reliability is the probability that an analog integrated circuit will succesfully perform its specified function in a given environment for a specified period of time. This is the classical definition of reliability applied to analog integrated circuits.

Another way of thinking about reliability is in relationship to quality. While **quality** is a measure of variability (extending to potential nonconformances-rejects) in the population domain, **reliability** is a measure of variability (extending to potential nonconformances-failures) in the population, time and environmental conditions domain. In brief, **reliability** can be thought of as **quality over time** and **environmental conditions**.

Ultimately, **product reliability** is a function of proper **understanding** of **customer requirements** and **communicating** them throughout design, product/process development, manufacturing and final product use. **Quality Function Deployment (QFD)** is a technique which may be used to facilitate identification of customer quality and reliability requirements and communicating them throughout an organization.

The most frequently used reliability measure for integrated circuits is the **failure rate expressed** in percent per thousand device hours (%/1000 hrs.). If the time interval is small the failure rate is called **Instantaneous Failure Rate** [λ (t)] or "Hazard Rate." If the time interval is long (for example total operational time) the failure rate is called **Cumulative Failure Rate**.

The number of failures observed, taken over the number of device hours accumulated at the end of the observation period and expressed as a percent is called the point estimate failure rate. This however, is a number obtained from observations from a sample of all integrated circuits. If we are to use this number to estimate the failure rate of all integrated circuits (total population), we need to say something about the risk we are taking by using this estimate. A **risk** statement is provided by the **confidence level** expressed together with the failure rate. Mathematically, the failure rate at a given confidence level is obtained from the point estimate and the **CHI square** (X^2) distribution. (The X^2 is a statistical distribution used to relate the observed and expected frequencies of an event.) In practice, a reliability calculator rule is used which gives the failure rate at the confidence level desired for the number of failures and device hours under question.

As the number of device hours increases, our confidence in the estimate increases. In integrated circuits, it is preferred to make estimates on the basis of failures per 1,000,000,000 (10^9) device hours **(FITS)** or more. If such large numbers of device hours are not available for a particular device, then the point estimate is obtained by pooling the data from devices that are similar in process, voltage, construction, design, etc., and for which we expect to see the same failure modes in the field.

The environment is specified in terms of the temperature, electric field, relative humidity, etc., by an **Eyring** type equation of the form:

$$\lambda = Ae^{-\frac{\phi}{KT}} \ldots e^{-\frac{B}{RH}} \ldots e^{-\frac{C}{E}}$$

where A, B, C, ϕ & K are constants, T is temperature, RH is relative humidity, E is the electric field, etc.

The most familiar form of this equation deals with the first exponential which shows an **Arrhenius type** relationship of the **failure rate** versus the **junction temperature** of integrated circuits, while the causes of failure generally remain the same. Thus we can test devices near their maximum junction temperatures, analyze the failures to assure that they are the types that are accelerated by temperature and then applying known acceleration factors, estimate the failure rates for lower junction temperatures. The Eyring or Arrhenius relationships should be used for failure rate projections in conjunction with proper understanding of failure modes, mechanisms and patterns such as infant mortality, constant failure rate (useful region) and wearout. For example if by design and proper process control infant mortality and useful period failures have been brought to zero and wearout failures do not start until, let us say, 30,000 hours at 125°C then failure rate projections at lower temperatures must account for these facts and whether the observed wearout failures occur at lower temperatures.

Figure 7 shows an example of a curve which gives estimates of failure rates versus temperature for an integrated circuit case study.

Arrhenius type of equation: $\lambda = Ae^{-\frac{\phi}{KT}}$

where:
- λ = Failure Rate
- A = Constant
- e = 2.72
- ϕ = Activation Energy
- K = Botzman's Constant
- T = Temperature in Degrees Kelvin

$T_J = T_A + \theta_{JA} P_D$ or $T_J = T_C + \theta_{JC} P_D$

where:
- T_J = Junction Temperature
- T_A = Ambient Temperature
- T_C = Case Temperature
- θ_{JA} = Junction to Ambient Thermal Resistance
- θ_{JC} = Junction to Case Thermal Resistance
- P_D = Power Dissipation

Life patterns (failure rate curves) for equipment and devices can be represented by an idealized graph called the **Bathtub Curve** (Figure 8).

There are three important regions identified on this curve. In Region A, the failure rate decreases with time and it is generally called **infant mortality** or early life failure region. In Region B, the failure rate has reached a relatively constant level and it is called **constant failure rate** or useful life region. In the third region, the failure rate increases again and it is called **wearout region**. Modern integrated circuits generally do not reach the wearout portion of the curve when operating under normal use conditions.

Figure 7. Example of a Failure Rate versus Junction Temperature Curve

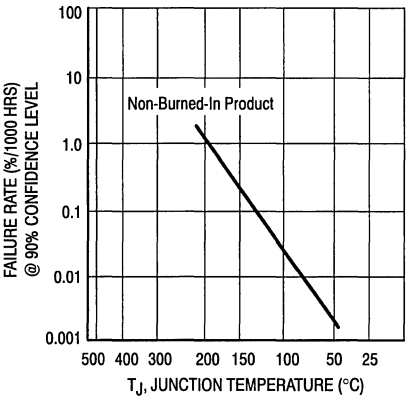
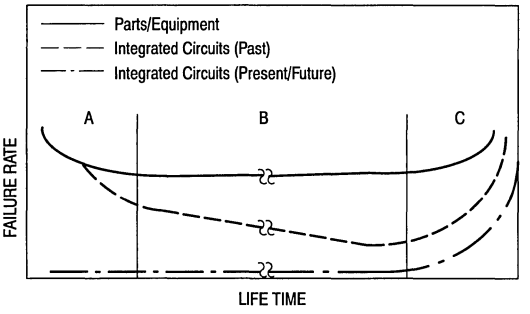


Figure 8. A Model for Failure Distribution in Time Domain Bathtub Curve Model



Decreasing Failure Rate	Constant Failure Rate	Increasing Failure Rate
Infant Mortality Burn-In	Useful Life	Wearout
Manufacturing Variations Workmanship Defects	Random (Chance) Defects (No Pattern; Occur Regularly)	Material, Design, Process Limitations
Weibull Log Normal Gamma Distribution	Weibull Exponential for Equipment Log Normal for ICs	Weibull Normal (Gaussian)

The wearout portion of the curve can usually be identified by using highly accelerated test conditions. For modern integrated circuits, even the useful life portion of the curve may be characterized by few or no failures. As a result the bathtub curve looks like continuously declining (few failures, Figure 8, Curve B) or zero infant and useful period failures (constant failure rate until wearout, Curve C).

The **infant mortality** portion of the curve is of most interest to equipment manufacturers because of its impact on customer perception and potential warranty costs. In recent years the infant mortality portion of the curve for integrated circuits, and even equipment, has been drastically reduced

(Figure 8, Curve C). The reduction was accomplished by improvements in technology, emphasis on statistical process control, reliability modeling in design and reliability in manufacturing (wafer level reliability, assembly level reliability, etc.). In this respect many integrated circuit families have zero or near zero failure patterns until wearout starts.

Does a user still need to consider burn-in? For this question to be answered properly the IC user must consider the **target failure rate** of the equipment, **apportioned** to the components used, application environment, maturity of equipment and components (new versus mature technology), the impact of a failure (i.e. safety versus casual loss of entertainment), maintenance costs, etc. Therefore, if the IC user is going through these considerations for the first time, the question of burn-in at the component level should be discussed during a user-vendor interface meeting.

A frequently asked question is about the reliability differences between **plastic** and **hermetic** packaged integrated circuits. In general, for all integrated circuits including analog, the field removal rates are the same for normal use environments, with many claims of plastic being better because of its "solid block" structure.

The tremendous decrease of failure rates of plastic packages has been accomplished by **continuous improvements** in piece parts, materials and processes. Nevertheless, differences can still be observed under highly accelerated environmental stress conditions. For example, if a bimetallic (gold wire and aluminum metallization) system is used in plastic packages and they are placed on a high temperature operating life test (125°C) then failures in the form of opens, at the gold to aluminum interface, may not be observed until 30,000 hours of continuous operating life. Packages, whether plastic or hermetic, with a monometallic system (aluminum wire to aluminum metallization) will have no opens because of the absence of the gold to aluminum interface. As a result, a difference in failure rates will be observable.

Differences in failure rates between plastics and hermetics may also be observed if devices from both packaging systems are placed in a moist environment such as 85°C, 85% RH with bias applied. At some point in time plastic encapsulated ICs should fail since they are considered pervious by moisture, (the failure mechanism being corrosion of the aluminum metallization) while hermetic packages should not fail since they are considered impervious by moisture. The reason the word "should" was used is because advances in plastic compounds, package piece parts, encapsulation processes and final chip passivation have made plastic integrated circuits capable of operating more than 5000 hours without failures in an 85°C, 85% RH environment. Differences in failure rates due to internal corrosion between plastic and hermetic packages may not be observable until well after 5000 operating hours.

The aforementioned two examples had environments substantially more accelerated than normal life so the two issues discussed are not even a factor under normal use conditions. In addition, mechanisms inherent in hermetic packages but absent in plastics were not even considered here. Improved reliability of plastic encapsulated ICs has decreased demand of hermetic packages to the point where many devices are offered only in plastic packages. The user then should feel comfortable in using the present plastic packaging systems.

A final question that is asked by the IC user is, how can one be assured that the reliability of standard product does not degrade over time? This is accomplished by our emphasis on **statistical process control, in-line reliability** assessment and **reliability auditing** by periodic and strategic sampling and accelerated testing of the various integrated circuit device packaging systems. A description of these audit programs follows.

Analog Reliability Audit Program

The reliability of a product is a function of proper understanding of the application and environmental conditions that the product will encounter during its life as well as design, manufacturing process and final use conditions. **Inherent reliability** is the reliability which a product would have if there were no imperfections in the materials, piece parts and manufacturing processes of the product. The presence of imperfections gives rise to reliability risks. **Failure Mode and Effects Analysis (FMEA)** is a technique for identifying, controlling and eliminating potential failures from the design and manufacture of the product.

Motorola uses **on-line** and **off-line** reliability monitoring in an attempt to prevent situations which could degrade reliability. **On-line** reliability monitoring is at the **wafer and assembly levels** while **off-line** reliability monitoring involves reliability assessment of the **finished product** through the use of **accelerated** environmental tests.

Continuous monitoring of the reliability of analog integrated circuits is accomplished by the **Analog Reliability Audit Program**, which is designed to compare the actual reliability to that specified. This objective is accomplished by periodic and strategic sampling of the various integrated circuit device packaging systems. The samples are tested by subjecting them to accelerated environmental conditions and the results are reviewed for unfavorable trends that would indicate a degradation of the reliability or quality of a particular packaging system. This provides the trigger mechanism for initiating an investigation for **root cause** and **corrective action**. Concurrently, in order to provide a minimum of interruption of product flow and assure that the product is fit for use, a lot by lot sampling or a non-destructive type 100% screen may be used to assure that a particular packaging system released for shipment does have the expected reliability. This rigorous surveillance is continued until there is sufficient proof (many consecutive lots) that the problem has been corrected.

The **Logic and Analog Technologies Group** has used reliability audits since the late sixties. Such programs have been identified by acronyms such as CRP (Consumer Reliability Program), EPIIC (Environmental Package Indicators for Integrated Circuits), LAPP (Linear Accelerated Punishment Program), and RAP (Reliability Audit Program).

Currently, the Analog Reliability Audit Program consists of a **Weekly Reliability Audit** and a **Quarterly Reliability Audit**. The Weekly Reliability Audit consists of rapid (short time) types of tests used to monitor the production lines on a real time basis. This type of testing is performed at the assembly/test sites worldwide. It provides data for use as an **early warning system** for identifying negative trends and triggering investigations for root cause and corrective actions.

The Quarterly Reliability Audit consists of long term types of tests and is performed at th U.S. Bipolar Analog Division Center. The data obtained from the Quarterly Reliability Audit is used to assure that the correlation between the short term weekly tests and long term quarterly tests has not changed and a new failure mechanism has not appeared.

A large data base is established by combining the results from the Weekly Reliability Audit with the results from the Quarterly Reliability Audit. Such a data base is necessary for estimating long term failure rates and evaluating potential process improvement changes. Also, after a process improvement change has been implemented, the Analog Reliability Audit Program provides a system for monitoring the change and the past history data base for evaluating the affect of the change.

Weekly Reliability Audit

The Weekly Reliability Audit is performed by each assembly/test site worldwide. The site must have capability for final electrical and quality assurance testing, reliability testing and first level of failure analysis. The results are reviewed on a continuous basis and corrective action is taken when appropriate. The results are accumulated on a monthly basis and published.

The Reliability Audit test plan is as follows:

Electrical Measurements: Performed initially and after each reliability test, consist of critical parameters and functional testing at 25°C on a go-no-go basis.

High Temperature Operating Life: Performed to detect failure mechanisms that are accelerated by a combination of temperature and electric fields. Procedure and conditions are per MIL-STD-883, Method 1015 with an ambient temperature of 145°C for 40 hours or equivalent based on a 1.0 eV activation energy and the Arrhenius equation.

Approximate Accelerated Factors

	125°C	50°C
145°C	4	4000
125°C	1	1000

Temperature Cycling/Thermal Shock: Performed to detect mechanisms related to thermal expansion and contraction of dissimilar materials, etc. Procedures and conditions are per MIL-STD-883, Methods 1010 or 1011, with ambient temperatures of –65° to +150°C or –40° to +125°C (JEDEC-STD-22-A104), for a minimum of 100 cycles.

Pressure Temperature Humidity (Autoclave): Performed to measure the moisture resistance of plastic encapsulated packages. It detects corrosion type failure mechanisms due to free ionic contaminants that may have entered the package during the manufacturing processes. Conditions are per JEDEC-STD-22, Method 102, a temperature of 121°C, steam environment and 15 psig. The duration of the test is 96 hours (minimum).

Analysis Procedure: Devices failing to meet the electrical criteria after being subjected to an accelerated environment type test are verified and characterized electrically, then submitted for failure analysis.

Quarterly Reliability Audit

The Quarterly Analog Reliability Audit Program is performed at the U.S. Bipolar Analog Division Center. This testing is designed to assure that the correlation between the short term weekly tests and the longer quarterly tests has not changed and that no new failure mechanisms have appeared. It also provides additional long term information for a data base for estimating failure rates and evaluation of potential process improvement changes.

Electrical Measurements: Performed initially and at interim readouts, consist of all standard DC and functional parameters at 25°C, measured on a go-no-go basis.

High Temperature Operating Life Test: Performed to detect failure mechanisms that are accelerated by a combination of temperature and electric fields. Procedure and conditions are per MIL-STD-883, Method 1015, with an ambient temperature of 145°C for 40 and 250 hours or equivalent, based on 1.0 eV activation energy and the Arrhenius equation.

Approximate Accelerated Factors

	125°C	50°C
145°C	4	4000
125°C	1	1000

Temperature Cycling/Thermal Shock: Performed to detect mechanisms related to thermal expansion and contraction, mismatch effects, etc. Procedure and conditions are per MIL-STD-883, Methods 1010 or 1011, with ambient temperatures of –65° to +150°C or –40° to +125°C (JEDEC-STD-22-A104) for 100, 500 and 1000 or more cycles, depending on the temperature range used. Temperature Cycling is used more frequently than Thermal Shock.

Pressure Temperature Humidity (Autoclave): Performed to measure the moisture resistance of plastic encapsulated packages. It detects corrosion type failure mechanisms due to free ionic contaminants that may have entered the package during the manufacturing processes. Conditions are per JEDEC-STD-22, Method 102, a temperature of 121°C, steam environment and 15 psig. The duration of the test is for 96 hours (minimum), with a 48 hour interim readout.

Pressure Temperature Humidity Bias (PTHB; Biased Autoclaved): This test measures the moisture resistance of plastic encapsulated packages. It detects corrosion type failure mechanisms due to free and bounded ionic contaminants that may have entered the package during the manufacturing processes, or they may be bound in the materials of the integrated circuit packaging system and activated by the moisture and the applied electrical fields. Conditions are per JEDEC-STD-22, Method 102, with bias applied, a temperature of 121°C, steam environment and 15 psig. This test detects the same type of failures as the Temperature Humidity Bias (85°C, 85% RH, with bias) test, only faster. The acceleration factor between PTHB and THB is between 20 and 40 times, depending on the type of corrosion mechanism, electrical field and packaging system.

Highly Accelerated Stress Test (HAST) is increasingly replacing the aforementioned **PTHB** test. The reason is that the **HAST** test allows control of pressure, temperature and

humidity independently of each other, thus we are able to set different combinations of temperature and relative humidity. The most frequently used combination is **130°C with 85% RH**. This has been related to THB (85°C, 85% RH) by an **acceleration factor of 20** (minimum). The ability to keep the relative humidity variable constant for different temperatures is the most appealing factor of the HAST test because it reduces the determination of the acceleration factor to a single Arrhenius type of relationship. Motorola has been phasing over to HAST testing since 1985.

Temperature, Humidity and Bias (THB): This test measures the moisture resistance of plastic encapsulated packages. It detects corrosion type failure mechanisms due to free and bounded ionic contaminants that may have entered the package during the manufacturing processes, or they may be bound in the materials of the integrated circuit packaging system and activated by moisture and the applied electrical fields. Conditions are per JEDEC-STD-22, Method 102 (85°C, 85% RH), with bias applied. The duration is for 1008 hours, with a 504 hour interim readout. The acceleration factor between THB (85°C, 85% RH with bias) and the 30°C, 90% RH is typically 40 to 50 times, depending on the type of corrosion mechanism, electrical field and packaging system.

Analysis Procedure: Devices failing to meet the electrical criteria after being subjected to an accelerated environment type test(s) are verified and characterized electrically, then they are submitted for root cause failure analysis and corrective action for continuous improvement.

Applications and Product Literature

In Brief . . .

Motorola's Applications Literature provides guidance to the effective use of its semiconductor families across a broad range of practical applications. Many different topics are discussed — in a way that is not possible in a device data sheet — from detailed circuit designs complete with PCB layouts, through matters to consider when embarking on a design, to complete overviews of product families and their design philosophies.

Information is presented in the form of Application Notes, Article Reprints and detailed Engineering Bulletins.

Abstracts of all the applications documents are provided as a guide to their content; each abstract also shows the number of pages in the document, plus the origin of the article in the case of Article Reprints. Documents new to this issue are highlighted throughout.

Applications and Product Literature

*Indicates New Document

The application literature listed in this section has been prepared to acquaint the circuits and systems engineer with Motorola Linear integrated circuits and their applications. To obtain copies of the notes, simply list the publications number or numbers and send your request on your company letterhead to: Literature Distribution Center, Motorola Semiconductor Products Inc., P.O. Box 20912, Phoenix, Arizona 85036.

Application Note Abstracts

AN004E ***Semiconductor Consideration for DC Power Supply Voltage Protector Circuits***

This paper addresses the requirements for the semiconductor sensing circuitry and SCR crowbar devices used in DC power supply over/under voltage protection schemes. (8pp)

AN428 ***Automotive Direction Indicator with Short Circuit Detection Using the UAA1041***

Cold lamps and faulty wiring can cause false operation when using the UAA1041 Automotive Direction Indicator IC. This note provides simple solutions. (3pp)

AN531 ***MC1596 Balanced Modulator***

The MC1596 Monolithic Balanced Modulator is a versatile HF communications building block. It functions as a broadband, double-sideband suppressed-carrier balanced modulator without the need for transformers or tuned circuits. This article describes device operation and biasing, and gives circuit details for typical modulator/demodulator applications in AM, SSB and suppressed-carrier AM. Additional uses as an SSB Product Detector, AM Modulator/Detector, Mixer, Frequency Doubler, Phase Detector and others are also illustrated. An appendix gives detailed AC and DC analysis. (13pp)

AN535 ***Phase-Locked-Loop Design Fundamentals***

The fundamental design concepts for phase-locked-loops implemented with integrated circuits are outlined. The necessary equations required to evaluate the basic loop performance are given in conjunction with a brief design example. (12pp)

AN545A ***Television Video IF Amplifier Using Integrated Circuits***

This applications note considers the requirements of the video IF amplifier section of a television receiver, and gives working circuit schematics using integrated circuits which have been specifically designed for consumer oriented products. The integrated circuits used are the MC1350, MC1352, and the MC1330. (12pp)

AN559 ***A Single Ramp Analog-to-Digital Converter***

A simple single ramp A/D converter which incorporates a calibration cycle to ensure an accuracy of 12 bits is discussed. The circuit uses standard ICs and requires only one precision part — the reference voltage used in the calibration. This converter is useful in a number of instrumentation and measurement applications (10pp)

AN569 ***Transient Thermal Resistance — General Data and its Use***

Data illustrating the thermal response of a number of semiconductor die and package combinations are given. Its use, employing the concepts of transient thermal resistance and superposition, permit the circuit designer to predict semiconductor junction temperature at any point in time during application of a complex power pulse train. (16pp)

AN587 ***Analysis and Design of the Op Amp Current Source***

Voltage-controlled current sources based on operational amplifiers are both versatile and accurate, yet the quality of op amps required is unimportant. This note develops general expressions for basic transfer function and output impedance, and shows that simplified equations give a very accurate description of actual circuit performance. Includes a section on analysis of the errors that result from changes in circuit parameters and temperature. (7pp)

AN703 ***Designing Digitally-Controlled Power Supplies***

This application note shows two design approaches; a basic low voltage supply using an inexpensive MC1723 voltage regulator and a high current, high voltage, supply using the MC1466 floating regulator with optoelectronic isolation. Various circuit options are shown to allow the designer maximum flexibility in an application. (9pp)

AN708A ***Line Driver and Receiver Considerations***

This report discusses many line driver and receiver design considerations such as system description, definition of terms, important parameter measurements, design procedures and application examples. An extensive line of devices is available from Motorola to provide the designer with the tools to implement the data transmission requirements necessary for almost every type of transmission system. (18pp)

AN719 ***A New Approach To Switching Regulators***

This article describes a 24 V, 3.0 A switching mode supply. It operates at 20 kHz from a 120 V AC line with an overall efficiency of 70%. New techniques are used to shape the load line. The control circuit uses a quad comparator and an opto-coupler and features short circuit protection. (12pp)

AN740 ***The Design of an N-Channel 16k x 16 Bit Memory System for the PDP-11***

This application note describes the design and construction of a mainframe memory system with MCM6605 N-channel MOS memories. Topics included are: the interface to the PDP-11, refresh control and bookkeeping, timing control logic for the memories, memory system considerations and organization. The memory also features new integrated circuits that reduce package count and enhance memory system performance. (16pp)

AN781A ***Revised Data Interface Standards***

Revised data interface standards allow higher data rates and longer cables. This note provides an overview and comparison of the electrical and performance characteristics of RS232-C, RS422, RS423, RS449 and RS485. Includes a list of appropriate Motorola drivers and receivers with performance summaries. (6pp)

AN829 ***Application of the MC1374 TV Modulator***

The MC1374 was designed for use in applications where separate audio and composite video signals are available, which need converting to a high quality VHF television signal. It's ideally suited as an output device for subscription TV decoders, video disk and video tape players. (12pp)

AN879 ***Monomax: Application of the MC13001 Monochrome Television Integrated Circuit***

This application note presents a complete 12″ black and white line-operated television receiver, including artwork for the printed circuit board. It is intended to provide a good starting point for the first-time user. Some of the most common pitfalls are overcome, and the significance of component selections and locations are discussed. (12pp)

AN917 ***Reading and Writing in Floppy Disk Systems Using Motorola Integrated Circuits***

The floppy disk system has become a widely used means for storing and retrieving both programs and data. A floppy disk drive requires precision controls to position and load the head as will as defined read/write signals in order to be a viable system. This application note describes the use of the MC3469 and MC3471 Write Control ICs and the MC3470 Read Amplifier which provide the necessary head and erase control, timing functions, and filtering. (16pp)

AN920 ***Theory and Applications of the MC34063 and μA78S40 Switching Regular Control Circuits***

This paper describes in detail the principle of operation of the MC34063 and μA78S40 switching regulator subsystems. Several converter design examples and numerous applications circuits with test data are included. (38pp)

AN921 ***Horizontal APC/AFC Loops***

The most popular method used in modern television receivers to synchronize the line frequency oscillator is the phase locked loop. The operating characteristics and parameters of the loops are discussed. (19pp)

AN932 ***Application of the MC1377 Color Encoder***

The MC1377 is an economical, high quality, RGB encoder for NTSC or PAL applications. It accepts RGB and composite sync inputs, and delivers a 1.0 Vp-p composite NTSC or PAL video output into a 75 Ω load. It can provide its own color oscillator and burst gating, or it can easily be driven from external sources. Performance virtually equal to high-cost studio equipment is possible with common color receiver components. (12pp)

AN957 ***Interfacing the Speakerphone to the MC34010/11/13 Speech Networks***

Interfacing the MC34018 speakerphone circuit to the MC34010 series of telephone circuits is described in this application note. The series includes the MC34010, MC34011, MC34013, and the new "A" version of each of those. The interface is applicable to existing designs, as well as to new designs. (12pp)

AN958 ***Transmit Gain Adjustments for the MC34014 Speech Network***

The MC34014 telephone speech network provides for direct connection to an electret microphone and to Tip and Ring. In between, the circuit provides gain, drive capability, and determination of the ac impedance for compatibility with the telephone lines. Since different microphones have different sensitivity levels, different gain levels are required from the microphone to the Tip and Ring lines. This application note will discuss how to change the gain level to suit a particular microphone while not affecting the other circuit parameters. (2pp)

AN959 ***A Speakerphone with Receive Idle Mode***

The MC34018 speakerphone system operates on the principle of comparing the transmit and receive signals to determine which is stronger, and then switching the circuit into that mode. (2pp)

AN960 ***Equalization of DTMF Signals Using the MC34014***

This application note will describe how to obtain equalization (line length compensation) of the DTMF dialing tones using the MC34014 speech network. (2pp)

AN968 ***A Digital Voice/Data Telephone Set***

This design provides standard analog telephone functions while simultaneously transmitting 9600 baud asynchronous data. It is based on Motorola's MC145422/26 UDLT family of voice/data ICs which provide 80 kbps full-duplex synchronous communication over distances up to 2 km. The circuit includes a Codec/filter, Data Set Interface and pulse/tone dialer. (7pp)

AN976 ***A New High Performance Current Mode Controller Teams Up with Current Sensing Power MOSFETs***

A new current mode control IC that interfaces directly with current sensing power MOSFETs is described. Its second generation architecture is shown to provide a variety of advantages in current mode power supplies. The most notable of these advantages is a "lossless" current sensing capability that is provided when used with current sensing MOSFETs. The discussion includes subtle factors to watch out for in practical designs, and an applications example. (8pp)

AN980 ***VHF Narrowband FM Receiver Design Using the MC3362 and the MC3363 Dual Conversion Receivers***

The MC3362 and MC3363 narrowband FM dual conversion receivers feature excellent VHF performance with low power drain, making them ideal for cordless telephones, narrowband voice and data receivers and RF security devices. This note provides a detailed description of the operation of the two devices, plus circuits and descriptions for four applications: a Single Channel VHF FM Narrowband Receiver; a Ten Channel Frequency Synthesized Cordless Telephone Receiver; a 256 Channel Frequency Synthesized Two-Meter Amateur Band Receiver; and a Single Chip Weather Band Receiver. (14pp)

AN983 ***A Simplified Power Supply Design Using the TL494 Control Circuit***

This application note describes the operation and characteristics of the TL494 Switchmode™ Voltage Regulator and shows its application of a 400 W offline power supply.

The TL494 is a fixed-frequency pulse width modulation control circuit, incorporating the primary building blocks required for the control of a switching power supply. (5pp)

AN1002 ***A Handsfree Featurephone Design Using the MC34114 Speech Network and the MC34018 Speakerphone ICs***

A comprehensive application note which develops a full featurephone circuit using the MC34114 Speech Network, the MC34018 Speakerphone IC and the MC145412 Dialer. Functions include 10 number memory pulse/tone dialer, tone ringer, mike mute and line length compensation for both handset and speakerphone operation. Options include line-powered circuit, line-powered circuit with booster for long lines, and external supply-powered. Includes glossary of telephone terms. (18pp)

AN1003 ***A Featurephone Design, with Tone Ringer and Dialer, Using the MC34118 Speakerphone IC***

This application note describes how to add a handset, dialer and tone ringer to the MC34118 speakerphone circuit. Although any one of several speech networks could be used as an interface between the MC34118 and the phone line this application note covers the case where simplicity and low cost are paramount. Two circuits are developed in this discussion: line-powered and supply-powered versions. (13pp)

AN1004 ***A Handsfree Featurephone Design Using the MC34114 Speech Network and the MC34118 Speakerphone ICs***

Complete designs for a featurephone providing 10 number memory, pulse or tone dialling, tone ringer, microphone muting, and line length compensation for both handset and speakerphone operation. Includes line-powered, line-powered plus long-line booster, and supply-powered versions. The MC34114 interfaces with tip and ring and provides 2-to-4 wire conversion. (18pp)

AN1006 ***Linearize the Volume Control of the MC34118 Speakerphone***

A single resistor added to the volume control potentiometer in an MC34118 speakerphone application will almost perfectly linearize the control law. (1pp)

AN1016 ***Infrared Sensing and Data Transmission Fundamentals***

Many applications need electrical isolation, remote control or position sensing. Infrared light provides an excellent solution due to its low cost, ease of use, availability of components, and freedom from the licensing and interference concerns of RF techniques. This note is a brief but informative reference on the design principles for IR systems, including a selection of receiver circuits. (6pp)

AN1019 ***NTSC Decoding Using the TDA3330, with Emphasis on Cable In/Cable Out Operation***

The TDA3330 is a Composite Video to RGB Color Decoder originally intended for PAL and NTSC color TV receivers and monitors — so its data sheet concentrates on picture tube drive. This practical application note supplements the data sheet by providing circuits for video cable drive as used in video processing, frame store and other specialized applications, and expands on TDA3330 functional details. Includes PCB artwork and layout of an evaluation board. (8pp)

AN1040 ***Mounting Considerations for Power Semiconductors***

The operating environment is a vital factor in setting current and power ratings of a semiconductor device. Reliability is increased considerably for relatively small reductions in junction temperature. Faulty mounting not only increases the thermal gradient between the device and its heatsink, but can also cause mechanical damage. This comprehensive note shows correct and incorrect methods of mounting all types of discrete packages, and discusses methods of thermal system evaluation. (20pp)

AN1044 ***The MC1378— A Monolithic Composite Video Synchronizer***

The MC1378 provides an interface between a remote composite color video source and local RGB. On-chip circuitry can lock a local computer to the remote source, switching between local and remote signals to generate composite video overlays. This detailed note describes local and remote operation; picture-in-picture applications and the design of test fixtures to help system development. Printed circuit artwork for an evaluation board is provided. The NTSC/PAL color encoder is similar to the MC1377, discussed in detail in AN932. (13pp)

AN1046 ***Three Piece Solution for Brushless Motor Control Design (Rev. 1)***

Until recently, the design of compact but comprehensive circuits taking full advantage of the unique attributes of brushless DC motors has been difficult, while available power transistors have not always performed as well as is necessary for the application. This high-performance three-chip solution couples the rugged MPM3003 three phase MOSFET bridge (in a 12-pin power package) with the MC33035 Brushless DC Motor Adapter. Design is simplified, board area reduced. Full circuit, parts list, and discussion of practical considerations. (10pp)

AN1077 ***Adding Digital Volume Control To Speakerphone Circuits***

Describes how to control speakerphone volume from UP and DOWN switches in place of the more usual potentiometer. Includes a fully annotated circuit using only three standard CMOS ICs and no critical components. (4pp)

AN1078 ***New Components Simplify Brush DC Motor Drives***

A variety of new components simplify the design of brush motor drives. One is a brushless motor control IC which is easily adapted to brush motors. Others include multiple Power MOSFETs in H-Bridge configuration, a new MOS turn-off device, and gain-stable opto level shifters. Several circuits illustrate how the new devices can be used in practical motor drives, in particular to control speed in both directions and operate from a single power supply. (6pp)

AN1080 ***External-Sync Power Supply with Universal Input Voltage Range for Monitors***

As the resolution of color monitors increases, the performance and features of their power supplies becomes more critical. EMI/RFI generated by switching power supplies can adversely affect resolution if switching frequency is not synchronized to horizontal scanning frequency. This 90 W flyback switching supply demonstrates the use of new high performance devices in a low cost design, and includes a new universal input voltage adapter. (20pp)

AN1081 ***Minimize the "pop" in the MC34119 Low Power Audio Amplifier***

Sometimes a "pop" is heard in the loudspeaker when the MC34119 audio amplifier is re-enabled. There are several possible causes, but this note offers a simple and low cost remedy to satisfy the most demanding user. (3pp)

AN1101 ***One-Horsepower Off-Line Brushless Permanent Magnet Motor Drive***

Brushless Permanent Magnet (BPM) motors (brushless DC motors) using MOSFET inverters are common in low voltage, variable speed applications such as disk drives. Higher voltage off-line applications can also use the same technology, but there have been problems in designing a reliable, low cost high side driver and understanding the more subtle effects of diode snap and PCB layout. This one-horsepower off-line BPM motor drive board uses opto-isolators and a special MOSFET turn-off IC for level translation. Includes PCB artwork and parts list, and a discussion of the theory. (10pp)

AN1108 ***Design Considerations for a Two Transistor, Current Mode Forward Converter***

This design for a 150 W, 150 kHz, two transistor, current mode forward converter illustrates solutions for noise control, feedback circuit analysis and magnetic component design — topics that often create the most problems for designers. Improved Schottky rectifiers, power MOSFETs and optocouplers — and their effects on switchmode power supply design — are also considered. Includes circuit, analysis, parts list and theoretical discussion. (11pp)

AN1122 ***Running the MC44802A PLL Circuit***

The MC44802A provides the Phase-Locked-Loop (PLL) portion of a tuning circuit intended for TV, FM radio and set-top converter applications up to 1.3 GHz; a complete tuning circuit is formed by adding a Voltage Controlled Oscillator (VCO) and mixer. The data sheet recommends use of an MCU for sending the control bytes that set the tuning frequency. This note describes a serial (I^2C) interface with an MC68HC11E9 in a tuner design — the information is sufficiently general to allow almost any MCU to be used. Includes M68HC11 program listing. (12pp)

AN1126** ***Evaluation Systems for Remote Control Devices on an Infrared Link

The availability at low cost of remote control devices and infrared communication links provides opportunities in many application areas. This note gives information for constructing the basic building blocks to evaluate both IR links and the most popular remote control devices. Schematics and single-side PCB layouts are presented that should enable the designer quickly to put together a basic control link and evaluate its suitability for a given application in terms of data rate, effective distance, error rate and cost. Sources for special parts are also given. (10pp)

AN1203 ***A Software Method for Decoding the Output from the MC14497/MC3373 Combination***

Infrared communication is now widely used as a simple and effective means of remote control over short distances. A variety of encoding methods is used, including the biphase scheme implemented by the MC14497, a complete building block for IR data transmission. The MC3373 is a companion receiver chip to the MC14497, providing front-end processing to interface a photo detector to a TTL level. This note describes the decoding of the data at the output of the MC3373, along with software listings for the MC68HC11 and the MC68HC05. (5pp)

AN1300 ***Interfacing Microcomputers to Fractional Horsepower Motors***

In fractional horsepower motion control systems, command signals are usually now generated by a microprocessor or digital signal processor, while power is applied with MOSFETs. The interface between the two can still present difficulties; for small motors it will be, typically, 5.0 V logic to complementary P-Channel/N-Channel MOSFET H-bridges. A number of factors need to be considered, including diode snap, group bounce, noise suppression and locking out invalid inputs. The design discussed here is embodied in evaluation board DEVB103. (8pp)

AN1301 ***Interfacing Analog Inputs to Fractional Horsepower Motors***

In many types of systems it is desirable to control motor speed with an analog signal. Even in digital systems, it is often cost effective to generate an analog signal from static speed control bits or a lower frequency PWM signal than to use a more expensive MCU capable of generating a 20 kHz+ PWM signal directly. Although recent developments have simplified analog input conversion and power MOSFET outputs, the interface between signal processing circuits and power outputs is still far from simple. This note discusses the issues using the DEVB118 evaluation board as an example design. (9pp)

AN1306 ***Thermal Distortion in Video Amplifiers***

Thermal distortion is a problem in many high resolution video amplifiers. It occurs when there are instantaneous power changes in the transistor stages, and if the problem remains uncompensated, this leads to the visual effect known as smearing. This note discusses what smearing is, what causes thermal distortion, how to measure it, and how to compensate for it. (5pp)

AN1307** ***A Simple Pressure Regulator Using Semiconductor Pressure Transducers

Semiconductor pressure transducers offer an economical means of achieving high reliability and performance in pressure sensing applications. The completely integrated MPX5100 (0 psi to 15 psi) series provides a temperature compensated, high level linear output suitable for interfacing directly with many linear control systems. This circuit illustrates how the MPX5100 can be used with a simple pressure feedback system based on the MC33033 Brushless Motor Controller to establish pressure regulation. Includes circuit diagram and PCB artwork. (7pp)

AN1510** ***A Mode Indicator for the MC34118 Speakerphone Circuit

Within the MC34118 are two comparators driven by the level detectors which are sensing the speech signals (see MC34118/D Data Sheet, Figure 24). The comparators' outputs drive the attenuator control block which sets the operating mode. (2pp)

ANE424 ***50 W Current Mode Controlled Offline Switch Mode Power Supply Working over 50% Duty Cycle using the UC3842A***

Switchmode power supplies based on flyback architecture and voltage-controlled PWM techniques are well established. This note describes a way of improving their dynamic characteristics using a Current Controlled PWM technique. A dedicated bipolar IC, the UC3842A Off-Line Current Mode PWM Controller, performs the current control, regulation and safety features. Full analysis of transformer and other components, plus discussion of the instability inherent in the current control mode. (27pp)

ANHK02 ***Low Power FM Transmitter System MC2831A***

This application note provides information concerning the MC2831A, a one-chip low-power FM transmitter system designed for FM communication equipment such as FM transceivers, cordless telephones, remote control and RF data link. (16pp)

Article Reprint Abstracts

AR301 ***Solid State Devices Ease Task of Designing Brushless DC Motors***

Brushless fractional-horsepower DC motors are gaining in popularity over brush type motors. Their characteristics are similar but they avoid the practical problems associated with brushes. In the past control complexity has made them less attractive, but dedicated control ICs like the MC33034, plus current-sensing power MOSFETs, mean that much of the control and protection electronics is available off the shelf. (*EDN*, 3 September 1987) (7pp)

AR323 ***Managing Heat Dissipation in DPAK Surface Mount Power Packages***

Physically smaller than a lead-formed TO-220, the DPAK was introduced to accommodate larger die than in previously available SM packages like the SOT-89. But larger die implies increased heat dissipation. New board materials and good circuit design ensure that DPAK Power MOSFETs can readily switch at their full pulse current ratings. (*Powertechnics*, December 1988) (4pp)

AR340 ***The Low Forward Voltage Schottky***

As feature sizes are scaled down in very high density circuits, it will be necessary for the standard power supply voltage to be reduced from 5.0 V to 3.3 V within the next few years to avoid degrading performance in the new devices. Also, greater power supply efficiency will be required if the power supply is not to occupy a disproportionate amount of the total system volume. Since the major power loss in switching power supplies is in the output rectification circuits, more efficient rectifiers are needed. Schottky rectifier technology shows the greatest potential. (*Powertechnics*, May 1990) (3pp)

Engineering Bulletin Abstracts

EB27A** ***Get 300 Watts EPE Linear Across 2 to 30 MHz from this Push-Pull Amplifier

Includes circuit, PCB artwork and layout for a 300 W push-pull linear amplifier based on two MRF422s, designed to operate over the 2.0 MHz to 30 MHz band. An MC1723 voltage regulator is used as a bias supply. (4pp)

EB85A ***Full-Bridge Switching Power Supplies***

A useful selection chart presenting preferred Bipolar, power MOSFET, Rectifier and Control devices for various areas of typical 500 W to 1000 W full-bridge switching power supplies. (1p)

EB112 ***The Application of a Telephone Tone Ringer as a Ring Detector***

Telephone ringers are driven by high voltage, low frequency AC signals which are superimposed on the 48 V DC Tip-Ring feed voltage. An electronic ring detector must sense the presence of an AC signal on the line and produce a dielectrically isolated logic level to the system processor. (2pp)

EB123 ***A Simple Brush Type DC Motor Controller***

A simple and cost effective way to drive brush type DC motors is to use power MOSFETs with a Brushless DC Motor Control IC. The low cost MC33033 controller and integrated 8.0 A/100 V MPM3002 H-bridge combine to give a minimum parts count brush motor drive. (2pp)

EB124 ***MOSFETs Compete with Bipolars in Flyback Power Supplies***

Power MOSFETs with 400 V to 500 V breakdown ratings are widely used in multiple-transistor off-line power supplies. Now they can be used in flyback supplies as well, as breakdown voltages are extended to 1000 V. A discussion of the advantages and disadvantages, illustrated with typical 100 W MOSFET and Bipolar designs. (2pp)

EB126 ***Ultra-Rapid Nickel-Cadmium Battery Charger***

Charging NiCad batteries is a particular problem when their voltage exceeds the voltage of the available charging source. The ultra-fast charger presented here is capable of charging eight to twelve 1.5 V batteries at 1.2 A to 1.8 A in 30 to 45 minutes from a 10 V to 14 V source — a feat made possible by the use of new sintered electrode technology by battery manufacturers. Includes PC artwork and layout. (3pp)

EB128 ***Simple, Low-Cost Motor Controller***

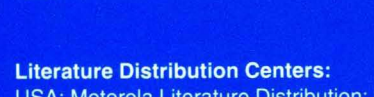
This low cost DC motor controller uses the cost effective MPM3002 SENSEFET-based H-Bridge, plus the MC34060 PWM IC. It is capable of driving a 1/3 HP, permanent magnet 90 V DC motor, and includes dynamic braking and Soft-Start. (2pp)

EB142 ***The MOSFET Turn-Off Device — A New Circuit Building Block***

Technical developments have lead to a variety of discrete devices using circuit integration to reduce system cost and board space, while offering some performance improvement over conventional solutions. The first of these new components — dubbed SMALLBLOCK™ — is a building block that simplifies and reduces the component cost of an active gate-turn-off network for current-source driven MOSFETs. It is available in TO-92, SOT-23 and SOT-223 packages. (8pp)

Product Literature

DL136/D	*Telecommunications Device Data*
HB206	*Linear & Switchmode Voltage Regulator Handbook* (See Back of Chapter 3) (Out of Print)
SG56/D	*TMOS Power MOSFET Selector Guide / Cross Reference*
SG73/D	*Master Selection Guide*
SG79/D	*SWITCHMODE — A Designer's Guide for Switching Power Supply Circuits and Components*
SG96/D	*Linear/Interface ICs Selector Guide Selector Guide and Cross Reference*
SG98/D	*Linear Telecom Cross Reference*
SG127/D	*Surface Mount Products Selector Guide*
SG368/D	*Video Capture Chip Sets Selector Guide* (See Front of Chapter 9)
SG410/D	*Applications & Product Literature Selector Guide / Cross Reference*



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