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Linear and Interface Circuits Applications

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Linear and Interface Circuits Applications

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PREFACE

The ever-increasing number of linear and interface integrated-circuit products has resulted in continuing, and steadily increasing, requirements for information regarding their performance in actual application situations. The objective of this book is to provide electronic system designers and technicians with basic theory related to the various types of linear and interface functions, practical application examples, and related performance results.

The applications discussed in this book have accrued from numerous laboratory tests and customer inquiries regarding the devices and their capabilities for performing desired functions. In many cases they are solutions to actual design requirements in users' systems. Because discussion of every possible design problem is obviously beyond the scope of a single volume, many guidelines and suggested design approaches are presented to provide ideas for design solutions not specifically discussed.

Design and application information has been provided by the Product Development and Applications departments of Texas Instruments in England and France, as well as the United States.

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1

Introduction

Jack Kilby of Texas Instruments ushered in the Integrated Circuit Age in 1958 when he fabricated two hand-built circuits. One of these, a phase-shift oscillator, was the first linear integrated circuit. From that beginning, rapidly emerging technologies have yielded the amazing diversity of sophisticated linear and digital integrated circuits available today.

For example, the Texas Instruments Data Book devoted exclusively to linear and interface products, which was published in 1973, contains more than 270 product listings in over 120 generic types.

Linear or Interface?

Linear devices such as operational amplifiers are those designed to operate primarily in a mode where the output is a continuous (linear) function of any input signal. Interface circuits, on the other hand, may contain both linear and logic circuitry, and are primarily used as information translators or to interface between different levels or types of components. These devices are often employed to shift standard logic levels (TTL) to power levels in applications such as interfacing logic to relays or lamps. They are also used as level detectors with a logic output, in logic to memory level translation, and to provide many other similar functions.

An operational amplifier or other device classified as a linear product often serves as an interface device, and an interface device may be biased to operate in a linear mode. In addition, devices have at times been classified according to the process technology used in their construction rather than by a strict definition of their primary function. An example is the SN72710 comparator, classified as a linear product, although its function is perhaps more nearly that of an interface circuit.

Product Categories

Each of the following chapters discusses integrated circuits designed for a specific category of applications, using a threefold approach. First, the basic theory relating to that area of application is discussed; second, the devices designed for that application, and their basic characteristics, are covered; third, practical application examples are presented. Product categories and basic definitions are:

Operational Amplifiers: Linear amplifiers designed to use external feedback for setting the gain and desired transfer function.

Comparators: Devices designed to provide standard TTL logic-level signals through comparison of two input voltage levels.

Video Amplifiers: Generally differential-input, differential-output linear devices having wide bandwidths (>10 MHz).

Voltage Regulators: Devices providing a fixed (or adjustable) output voltage that is stable with line or load variations.

Special Functions: Catalog devices for operation in special applications such as zero voltage switching, precision level detection, timing, modulation, mixing, multiplexing, and performance of logarithmic functions.

Peripheral Drivers: Universal interface circuits having TTL gates and medium-power transistors that may be connected to drive lamps, relays, memories, etc. from TTL level inputs or to provide TTL drive from other types of input signal levels. Because of their versatility, these circuits are also discussed in other chapters as they perform functions relative to those chapters.

MOS Interface Circuits: Products designed specifically for interfacing between digital logic (TTL/DTL/ECL) levels and MOS signal levels.

Core Memory Circuits: Drivers designed to deliver high-level, fast-switching currents required for core memories from standard digital logic (TTL/DTL/ECL) input signals. Sense amplifiers designed to provide digital logic output signals from low-level sense-line signals.

Line Transmission Circuits: Drivers for translating digital logic signals to voltage or current levels suitable for driving data transmission lines, and receivers for converting line transmission signals to digital logic levels.

Device Numbering System

The product identification number stamped on each integrated circuit is very descriptive of that device, and in fact is a code which defines its type, temperature

range, and package. An integrated-circuit identification number describes these features as follows:

EXAMPLE	SN	7	5	450B	N
	1	2	3	4	5

1. Prefix (two or three letters)
   - SN Standard IC Prefix
   - SNM IC tested to Mach IV Level 1
   - SNA IC tested to Mach IV Level 2
   - SNC IC tested to Mach IV Level 3
   - SNH IC tested to Mach IV Level 4

2. Temperature Range
   - 5 —55°C to +125°C Military Range
   - 6 —25°C to +85°C Reduced Military Range
   - 7 0°C to +70°C Industrial Range

3. General Category of IC
   - 2 Linear IC
   - 4 TTL Logic IC
   - 5 Interface IC
   - 6 Communication or Consumer IC

4. Function Identification
   This part of the identification will contain two or three numbers and may or may not include a letter. It is the primary identification of the device function.

5. Package Designation
   Must contain one or two letters which define the package type, as follows:

- N 14- or 16-pin dual-in-line plastic package
- J 14- or 16-pin dual-in-line ceramic base and ceramic cap
- P 8-pin dual-in-line plastic package
- L 8-pin (TO-99) or 10-pin (TO-100) welded metal-can package with glass sealant
- ND 8-pin and 2-tab frame dual-in-line package
- JA 14- or 16-pin alumina-filled glass header, metal lid, dual-in-line
- JB 14- or 16-pin metal-based header, metal lid, dual-in-line

JP 8-pin alumina-filled glass header, metal lid, dual-in-line
LA 3-pin welded metal-can package with glass sealant
FA 10-pin flat package, ceramic-based header, and metal lid
RA 24-pin flat package, ceramic header, and metal lid
SB 16- or 24-pin flat package, metal-based header, and metal lid

When selecting the package type, the particular device data sheet should be referred to for available package categories. For economical industrial and consumer applications in the 0 to 70°C operating range, N and P plastic packages are preferred. The various J and L, and the FA, RA, and SB packages are generally used in full military temperature (−55°C to +125°C) applications or high-reliability applications. In applications where some degree of shielding is required, metal-can or partially metal packages like the L, LA, FA, RA, and SB packages are preferable. The metal-can L and LA packages generally have slightly higher power-handling capability and may be preferred to eliminate a marginal condition. The ND package has heat-sink tabs and is particularly applicable in higher-power applications.

2

Operational Amplifiers

2.1 GENERAL

Operational amplifiers are high-gain linear devices designed to be used with external components to provide desired transfer functions. Frequency response, signal phase shift, gain, and transfer characteristics are normally determined by external-feedback and input-termination components. Feedback, although normally from the output to the inverting input (negative feedback), may in some applications be to the non-inverting input (positive feedback). It is possible to use both positive and negative feedback to produce controlled oscillation.

An ideal operational amplifier (Figure 2.1) would provide a linear output voltage proportional to the difference voltage between the two input terminals; the output voltage having the same polarity as the voltage at the non-inverting (+) input with respect to the voltage at the inverting (—) input.

An ideal amplifier would have the following characteristics:

Differential gain:	$\rightarrow \infty$	Output resistance:	0
Common-mode gain:	0	Bandwidth:	$\rightarrow \infty$
Input resistance:	$\rightarrow \infty$	Offset and drift:	0

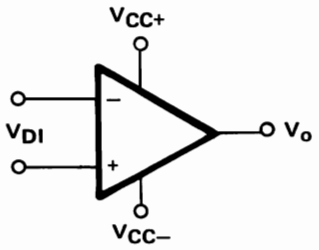


Figure 2.1. Ideal Operational Amplifier

The characteristics of an ideal amplifier cannot be realized in practice. Actual input and output parameters are finite and may be represented by an equivalent circuit as shown in Figure 2.2.

Input currents are represented by I_{IB1} and I_{IB2}
Differential input voltage V_{DI}
Input offset voltage V_{IO}
Input resistance r_i
The equivalent series output resistance is r_o.

The generator G represents the output voltage resulting from the product of gain and differential input voltage ($A_{VD}V_{DI}$).

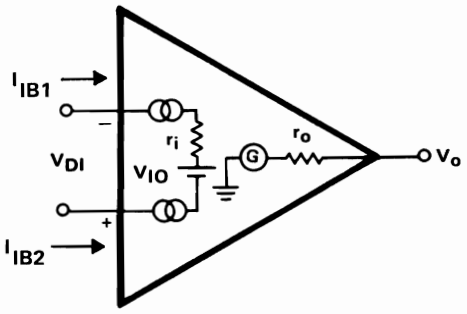


Figure 2.2. Equivalent Circuit for an Operational Amplifier

2.2 INFLUENCE OF INTERNAL PARAMETERS

The influence of internal parameters associated with operational amplifiers determines the actual values of the input-output transfer characteristics.

2.2.1 Influence of Open-Loop Gain A_{VD}

Assuming that other parameters are ideal the following relationships can be written for the inverting amplifier configuration shown in Figure 2.3:

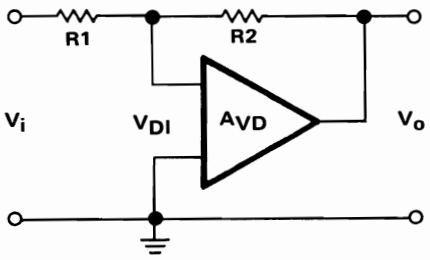


Figure 2.3. Influence of Open-Loop Gain

$$V_{DI} = \frac{V_o}{A_{VD}} \quad \text{and} \quad \frac{V_i - V_{DI}}{R1} = \frac{V_{DI} - V_o}{R2}$$

therefore

$$\frac{V_i}{V_o} = -\frac{1}{\frac{R2}{R1}} + \frac{1}{\frac{R2}{R1}A_{VD}} + \frac{1}{A_{VD}}$$

If R2/R1 is very small compared to A_{VD}, the A_{VD} has little effect on the ratio V_i/V_o. Simply, if $A_{VD} \gg R2/R1$, then $V_{DI} \ll Vi$ or V_o. The term $(V_i - V_{DI})/R1$ becomes $V_i/R1$, and $(V_{DI} - V_o)/R2$ becomes $-V_o/R2$. The result is that for practical applications the closed-loop gain, V_o/V_i, is equal to $-R2/R1$, the negative sign indicating that the circuit in Figure 2.3 is an inverting amplifier.

2.2.2 Influence of the Input Resistance

Applying Kirchhoff's law to Figure 2.4 gives $i_1 = i_2 + i_3$, from which can be written:

$$\frac{V_i - V_{DI}}{R1} = \frac{V_{DI} - V_o}{R2} + \frac{V_{DI}}{r_i}$$

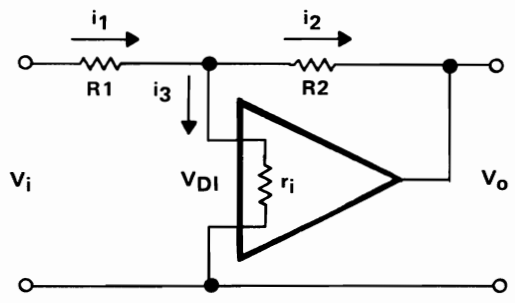


Figure 2.4. Influence of the Input Resistance

If the open-loop gain were infinite, V_{DI} would be zero, and the value of r_i would have no influence provided it were not zero. In reality $V_{DI} = V_o/A_{VD}$, and thus we may write:

$$\frac{V_i - \frac{V_o}{A_{VD}}}{R1} = \frac{\frac{V_o}{A_{VD}} - V_o}{R2} + \frac{\frac{V_o}{A_{VD}}}{r_i}$$

Therefore

$$\frac{V_i}{V_o} = \frac{1}{A_{VD}} + \frac{1}{\frac{R2}{R1} A_{VD}} + \frac{R1}{r_i A_{VD}} - \frac{1}{\frac{R2}{R1}}$$

or

$$\frac{V_i}{V_o} = -\frac{1}{\frac{R2}{R1}} + \frac{1}{\frac{R2}{R1} A_{VD}} + \frac{1}{A_{VD}} \left(1 + \frac{R1}{r_i} \right)$$

These equations make it clear that the input resistance (r_i) will have little or no effect on the ratio V_i/V_o unless r_i is a small value relative to R1. Therefore the closed-loop gain (V_o/V_i) is for practical applications independent of r_i.

2.2.3 Influence of Input Offset Voltage

The input offset voltage (V_{IO}) is internally generated and may be considered as a voltage provided by a generator inserted between the two inputs (Figure 2.5). It is a

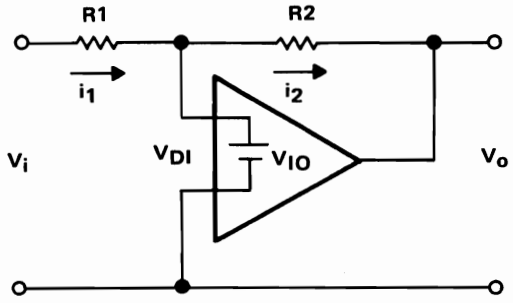


Figure 2.5. Influence of Input Offset Voltage

differential input voltage resulting from the mismatch of the operational amplifier's input stages. The currents i_1 and i_2 will be affected as follows:

$$\frac{V_i - V_{IO}}{R1} = \frac{V_{IO} - V_o}{R2}$$

If the input signal V_i is zero the equation becomes

$$\frac{-V_{IO}}{R1} = \frac{V_{IO} - V_o}{R2}$$

therefore

$$V_o = \left(\frac{R2}{R1} + 1\right) V_{IO}$$

Thus the input offset voltage is found at the output multiplied by the approximate gain. Methods of correcting for the offset voltage will be discussed later in the text.

2.2.4 Influence of Input Bias Current

The input bias current i_3 plus the normal operating currents flow through R1 and R2 (see Figure 2.6). It can be shown that a differential input voltage equal to $i_3(R1R2)/R1 + R2)$ is generated by this current. This voltage, which is not unlike V_{IO}, also appears at the output amplified by the system gain. Methods of correcting for effects of input bias current will be discussed later.

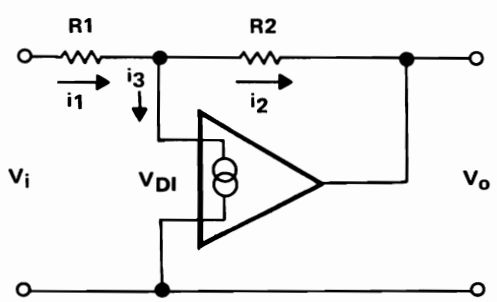


Figure 2.6. Influence of Input Bias Current

2.2.5 Influence of Voltage and Current Drift

Input offset voltage, input bias current, and differential offset currents may drift with temperature. Although it is relatively easy to compensate for the effects of these parameters, correcting for their drift due to temperature variations is difficult. It is therefore advisable to choose an amplifier having drift characteristics within the limits required by the application.

2.2.6 Influence of Output Resistance

From Figure 2.7 it is apparent that the output current may be expressed by:

$$I_o = i_2 + I_L, \text{ and } i_2 + I_L = \frac{V_o}{\frac{R2\,R_L}{R2 + R_L}}$$

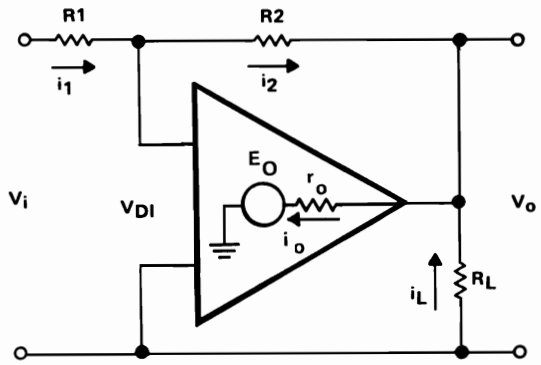


Figure 2.7. Influence of Output Resistance

If E_o is the output voltage of the equivalent ideal amplifier, and V_o the output voltage of the actual device, then V_o may be stated as:

$$V_o = E_o - r_o I_o = E_o - \frac{r_o V_o}{\frac{R2\,R_L}{R2 + R_L}}$$

For the ideal case $E_o = V_{DI}A_{VD}$; therefore

$$V_o = V_{DI}A_{VD} - r_o \frac{V_o}{\frac{R2\,R_L}{R2 + R_L}}$$

Dividing through by V_{DI} we get:

$$A'_{VD} = \frac{A_{VD}}{1 + \dfrac{r_o\,(R2 + R_L)}{R2\,R_L}}$$

where

$$A'_{VD} = \frac{V_o}{V_{DI}} \text{ and } A_{VD} = \text{the ideal open-loop gain}$$

The effect of the output resistance can be neglected for most of the second-generation operational amplifiers; however, this term should be considered in designs using devices such as the SN72702.

2.2.7 Influence of Device Bandwidth

The bandwidth of an ideal amplifier, by definition, approaches infinity, but circuit capacitances greatly limit actual device frequencies. As shown in Figure 2.8, the high open-loop gain begins to roll off at some relatively low frequency, limiting the available response. As an example, this typical general-purpose operational-amplifier response curve shows that a closed-loop gain of 40 dB will remain flat to about 10 kHz, where roll-off would begin. Finally the point of unity gain is reached (1 MHz in this example). This, referred to as the unity-gain bandwidth of the device, is expressed as B_1.

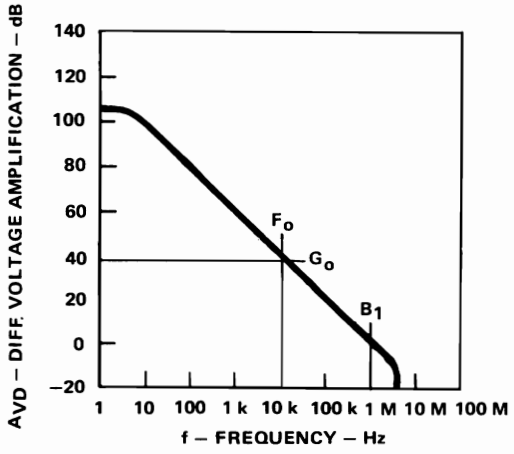


Figure 2.8. Influence of Device Bandwidth

2.2.8 Influence of Common-Mode Rejection Ratio (CMRR)

This characteristic, not considered in the single-ended inverting configurations previously discussed, has a definite effect on the balanced voltage follower and differential designs. The CMRR is expressed in dB, and is calculated as follows:

$$\text{CMRR} = 20 \log \frac{V_{ICM}}{V_{DI(equiv)}}$$

where V_{ICM} is the common-mode input voltage and $V_{DI(equiv)}$ is the equivalent differential input voltage necessary to provide the same output as that resulting from the V_{ICM}. The effect of a common-mode input signal is to generate an input offset voltage that appears at the output amplified by the closed-loop gain.

2.3 BASIC OPERATIONAL-AMPLIFIER DESCRIPTIONS

2.3.1 SN72702

Although preceded by several different operational-amplifier designs the SN72702 type devices (Figure 2.9) are considered the first widely used all-monolithic operational amplifiers. Operating from +12-volt and −6-volt supplies with proper external compensation, the SN52702A may be used for applications from dc to 30 MHz.

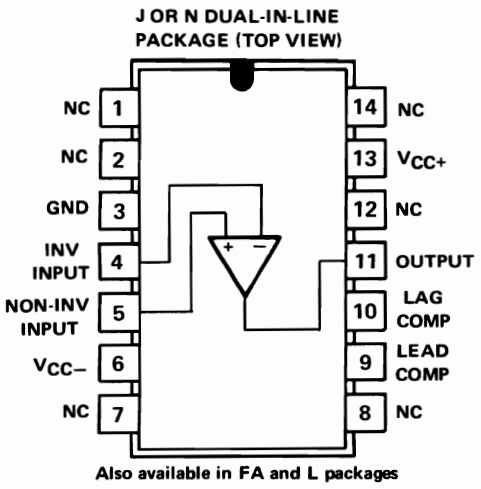


Figure 2.9. Package Diagram of the SN72702

2.3.2 SN72709

An improved device compared to the SN72702, the SN72709 (Figure 2.10) features increased gain and improved temperature stability. With selection of proper external compensation a gain of 60 dB is possible from dc to 300 kHz.

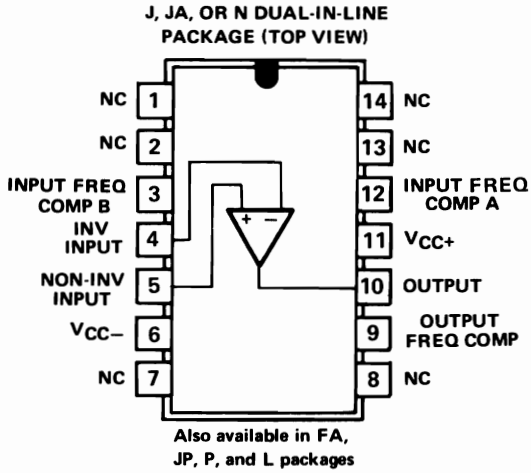


Figure 2.10. Package Diagram of the SN72709

2.3.3 SN72741 and SN72307

The SN72741 (Figure 2.11) is considered a second-generation device, having circuit improvements which make it presently the most popular general-purpose

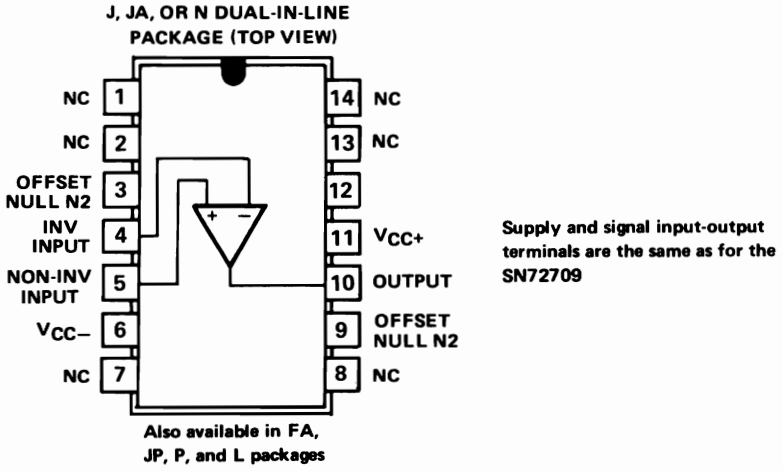


Figure 2.11. Package Diagram of the SN72741 and SN72307

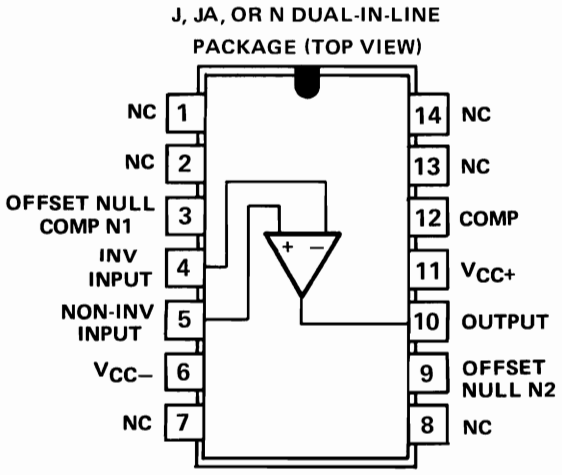
operational amplifier. It features output short-circuit protection, offset-voltage null capability, and improved common-mode capability. The SN72741 has no latch-up problems, and no external frequency-compensation components are required.

The SN72307 (Figure 2.11) is quite similar to the SN72741, but features lower input-bias current and input-offset current, improving its accuracy in high-impedance applications.

2.3.4 SN72748, SN72777, and SN72301A

The SN72748 (Figure 2.12) offers the same features as the SN72741 with the exception of internal frequency compensation. The external compensation of the SN72748 allows adjusting of the frequency response (where the closed-loop gain is greater than unity) for applications requiring wider bandwidth or higher slew rate.

The SN72777 (Figure 2.12) is a precision operational amplifier featuring very low offset and bias currents, allowing improved system accuracy in applications such as long-time integrators, sample-and-hold circuits, and high-source-impedance summing amplifiers. External frequency compensation allows control of bandwidth and slew rate.



Supply and signal input-output terminals are the same as for the SN72709

Also available in these packages:

	J	FA	JP	P	L
SN72748	X	X	X	X	X
SN72777		X	X	X	X
SN72301A	X	X	X	X	X

Figure 2.12. Package Diagram of the SN72748, SN72777, and SN72301A

The SN72301A (Figure 2.12) is a high-performance operational amplifier featuring very low input bias current and low input offset voltage and current. Normal external frequency compensation as well as feed-forward compensation may be used to adjust the frequency-response characteristics.

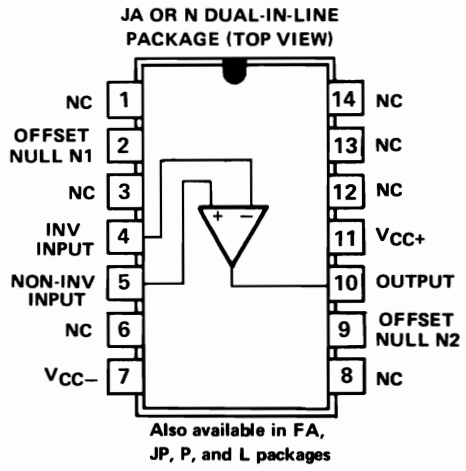
2.3.5 SN72770 and SN72771

The SN72770 and SN72771 (Figure 2.13) are high-performance, general-purpose, integrated-circuit operational amplifiers. The SN72771 is internally compensated, while the SN72770 is externally compensated to allow adjustments in frequency-response characteristics. These devices feature low input bias and offset current, characteristic of amplifiers using super-beta transistors. In addition these amplifiers have a high slew rate, making them ideal for fast-rise-time signals or large signals at high frequencies.

2.3.6 SN72660, SN72308, and SN72308A

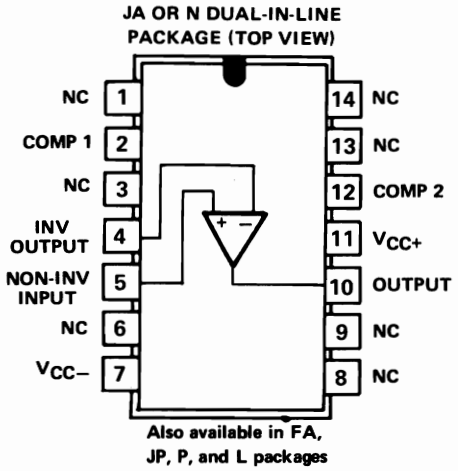
The SN72660 (Figure 2.14) was designed for applications requiring low input bias and offset currents and offset voltages. In addition the quiescent supply current is typically only 300 μA for low power consumption. The SN72660 performance characteristics make it useful in precision instrumentation applications as well as for other systems requiring accurate and stable performance.

The SN72308 and SN72308A amplifiers (Figure 2.14) feature very high gain super-beta circuitry providing extremely low input bias and offset currents and offset voltages. Designed specifically for high-performance applications, they also feature external frequency compensation for optimization of the frequency response for each application.



Pins 2 and 12 are used for external compensation of the SN72770 only

Figure 2.13. Package Diagram of the SN72770 and SN72771



Supply and signal input-output terminals are the same as for the SN72770 and SN72771

Figure 2.14. Package Diagram of the SN72660, SN72308, and SN72308A

2.3.7 SN72747

The SN72747 (Figure 2.15) is a dual-channel general-purpose operational amplifier featuring offset-voltage null capability for each amplifier. Each half is electrically similar to the SN72741.

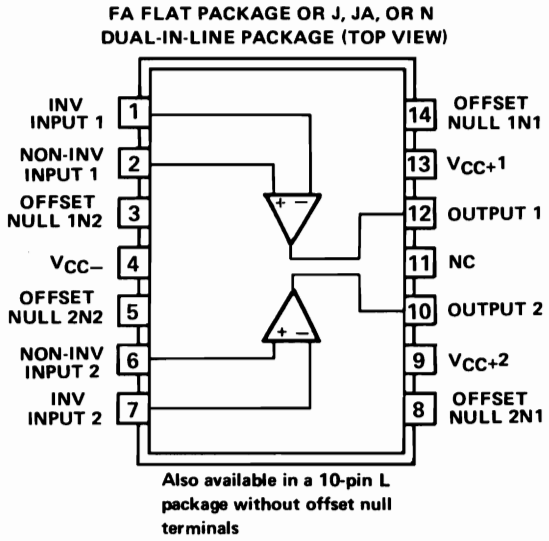


Figure 2.15. Package Diagram of the SN72747

2.3.8 SN72558 and SN72L022

The SN72558 (Figure 2.16) is a dual general-purpose operational amplifier, with each half electrically similar to the SN72741 except that offset null is not provided.

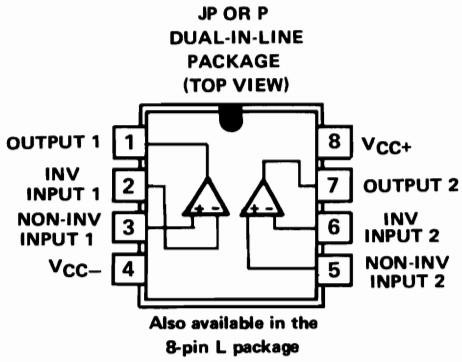


Figure 2.16. Package Diagram of the SN72558 and SN72L022

The SN72L022 (Figure 2.16) is a dual low-power operational amplifier designed for micropower applications. Internal compensation, absence of latch-up, and output short-circuit protection assure ease of use.

2.3.9 SN72L044

The SN72L044 (Figure 2.17) is a quad version of the SN72L022. It features the low-power characteristics of the SN72L022, and has separate positive power supplies for each section of two amplifiers.

2.3.10 SN72310

The SN72310 (Figure 2.18) is an internally connected unity-gain non-inverting amplifier (or voltage follower). It uses very high gain input transistors, resulting in low input bias currents. It also features high slew rate (30 V/μs typically) and a wide bandwidth of 20 MHz typically. It does not require external frequency compensation.

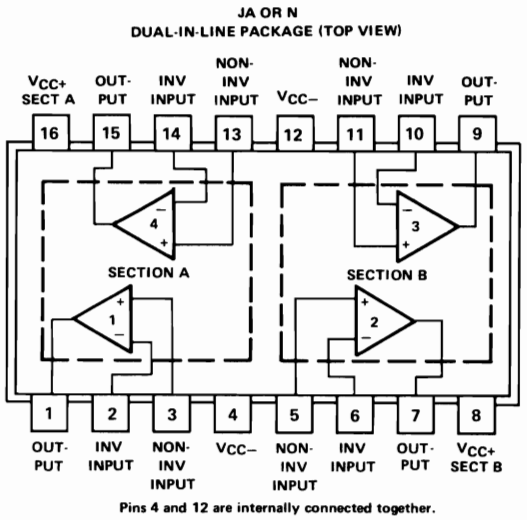


Figure 2.17. Package Diagram of the SN72L044

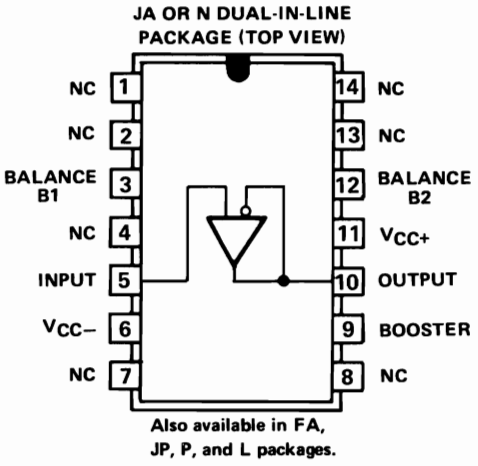


Figure 2.18. Package Diagram of the SN72310

2.3.11 SN72088

The SN72088 (Figure 2.19) is an extremely high-performance, chopper-stabilized operational amplifier. High input impedance, very low initial input offset voltage, low input offset voltage temperature coefficient, low input bias and offset currents, and high slew rate are achieved through the combination of state-of-the-art circuit techniques and advanced technologies.

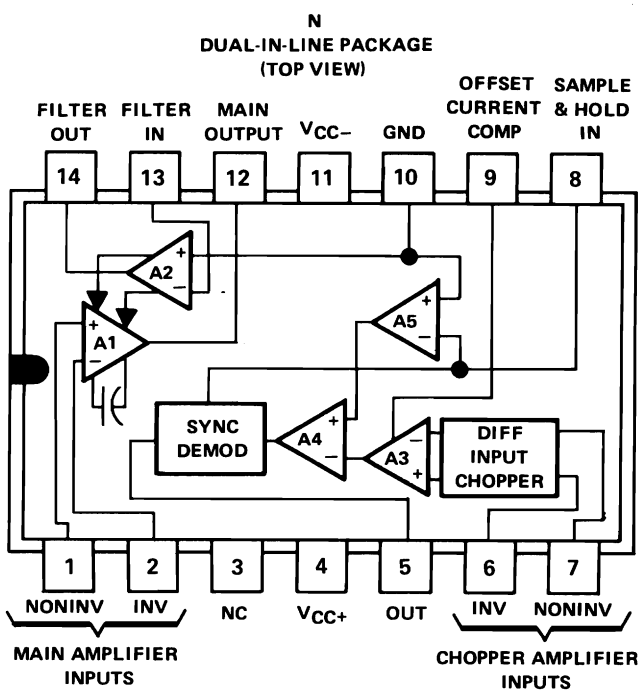


Figure 2.19. Package Diagram of the SN72088

2.4 COMPENSATION OF ERRORS DUE TO INTERNAL PARAMETERS

2.4.1 Compensation of Input Offset Voltage

Compensation of the SN72709 – This amplifier is compensated by modifying the collector current in one side of the input stage. This point is available at the input compensation terminal B (see Figure 2.20). Terminal B is connected, through a 150-kΩ resistor, to the arm of a 10-kΩ potentiometer terminated at V_{CC+} and ground to provide offset correction.

Compensation of the SN72741, SN72747, SN72307, or SN72771 – For these devices a 10-kΩ potentiometer is connected between the offset null terminals N1 and N2 (Figure 2.21), and the control arm is tied to V_{CC-}. Terminals N1 and N2 provide access to the emitters of the input-stage current sources, allowing easy control of input offset voltage.

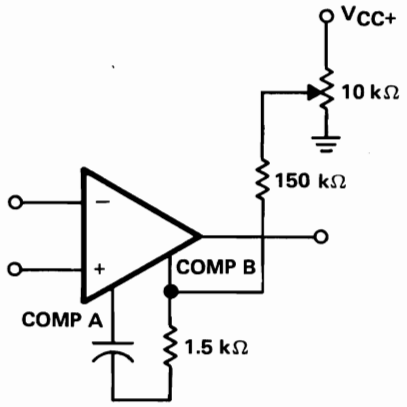


Figure 2.20. Offset-Voltage Compensation of the SN72709

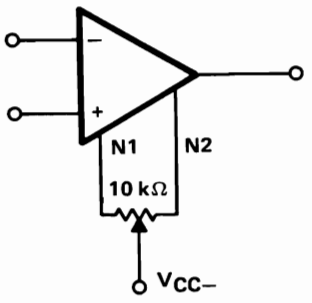


Figure 2.21. Offset-Voltage Compensation of the SN72741, SN72747, SN72307 or SN72771

Compensation of the SN72748, SN72770, SN72777, or SN72301A – In these amplifiers compensation is applied at the collector level of the input current sources. This allows one of these points to be used for frequency compensation as well as offset control. Because these points are at high impedance levels the control source must also be of high impedance to prevent excessive loading and gain loss (Figure 2.22). Thus offset correction is accomplished using a 5-megohm potentiometer across the null terminals with a 5.1-megohm resistor from its arm to ground.

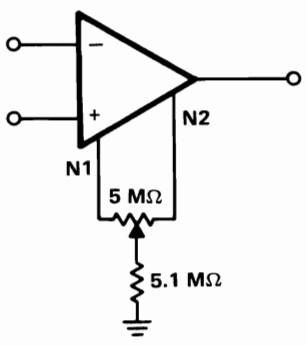


Figure 2.22. Offset-Voltage Compensation of the SN72748, SN72770, SN72777, or SN72301A

Compensation of the SN72308 — Offset correction for this device is similar to that of the SN72709 in that it is obtained by modification of first-stage currents. In the SN72308 it is accomplished by injecting a small current into the compensation-1 terminal. This point, corresponding to the base of the second stage, controls the collector voltage of an input stage. A 200-kΩ resistor (Figure 2.23) is connected from the compensation-1 terminal to the arm of a 10-kΩ potentiometer. The potentiometer is connected between V_{CC+} and ground, providing the injection current required.

2.4.2 Input-Current Compensation

Two basic methods are used to compensate for errors due to input currents. One is passive, using only resistors; the other is active, using external transistors.

Passive Compensation of an Inverting Amplifier — The input current i_1 (Figure 2.24) develops a voltage equal to $i_1(R1R2)/(R1 + R2)$ which appears at the inverting input terminal. The effects of this undesired voltage may be canceled by developing another voltage at the non-inverting input, with i_2 flowing through R3. To obtain complete cancellation, i_2R3 must equal $i_1(R1R2)/(R1 + R2)$. If i_1 and i_2, the input bias currents, are equal, it is sufficient to make $R3 = R1R2/(R1 + R2)$. When i_1 does not equal i_2, R3 could be made adjustable for an exact balance.

To help stabilize the dc level at the non-inverting input it may be desirable to provide a high-frequency bypass capacitor across R3. A ceramic capacitor in the 0.001-μF to 0.01-μF range would be sufficient in most cases.

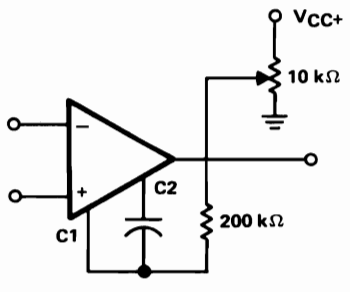


Figure 2.23. Offset-Voltage Compensation of the SN72308

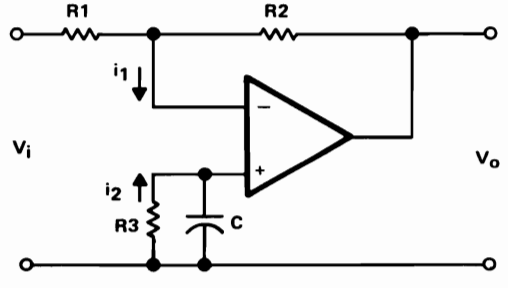


Figure 2.24. Passive Input-Current Compensation of an Inverting Amplifier

Passive Compensation of a Voltage-Follower Amplifier – The voltage follower (Figure 2.25) by definition must have a high input impedance. It is therefore not desirable that it be shunted by a low-value resistor. If the resistance (of the source) from the non-inverting input to ground is known and fixed, the voltage generated in it by input bias current can be calculated and compensated for by connecting a resistor R4 between the inverting input and the feedback network. The sum of R4 and R1R2/(R1 + R2) must equal the input source resistance.

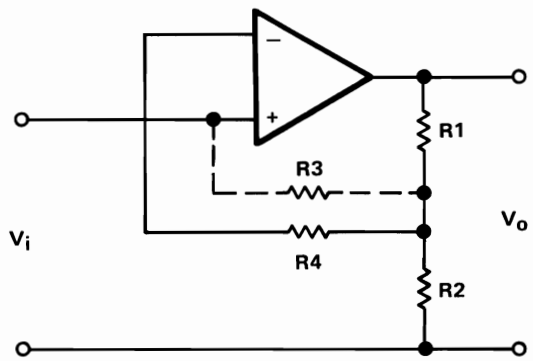


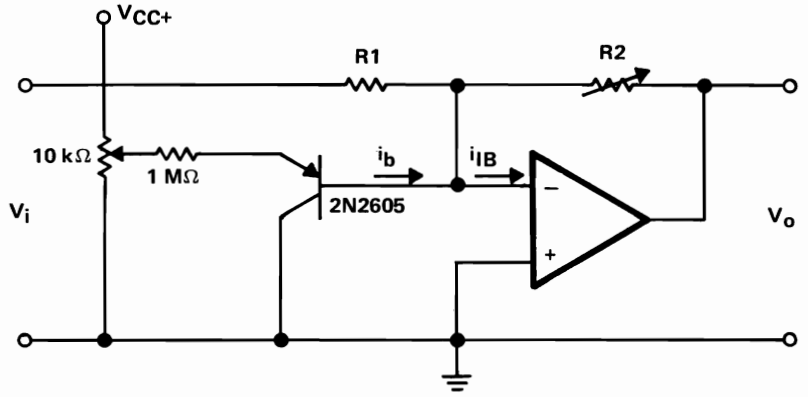
Figure 2.25. Passive Input-Current Compensation of a Voltage-Follower Amplifier

If the value of the input source resistance is unknown, bias to the non-inverting input may be provided by R3, connected between this input and the feedback network. If R3 and R4 are of equal value any large-value source impedance, connected at the input (V_i), would slightly lower the impedance seen at the non-inverting input, assuring more negative than positive feedback, thus maintaining stability. It should be noted that resistor tolerances might allow more feedback through R3 than R4, causing the amplifier to oscillate. If R4 is chosen to have a slightly lower nominal value than R3, negative feedback and stability are assured.

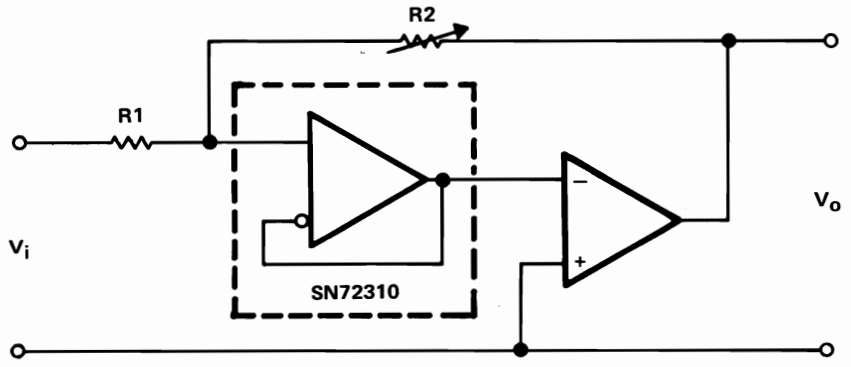
Active Compensation of an Inverting Amplifier – Passive compensation works only if the resistance of the feedback loop is fixed. If the feedback resistor R2 (Figure 2.24) varies, R3 must vary also to maintain compensation. This can be avoided with the circuit configuration shown in Figure 2.26a using a 2N2605, which automatically corrects the bias effects caused by varying R2. The 2N2605 is a PNP transistor with characteristics similar to those of the NPN input transistors of most IC operational amplifiers. A 2N2484 NPN transistor would be used if the IC has PNP input stages (i.e., SN72L022). Base current adjustment is provided by a 10-kΩ potentiometer (V_{CC+} to ground) through a 1-megohm resistor in series with the

2N2605's emitter. The potentiometer is adjusted to give a base current i_b equal to the required input bias current i_{IB}. Variations in input loading because of changes in R2 will affect input bias and base currents the same, thereby maintaining compensation.

Another method is to use a very low input bias current voltage-follower amplifier (SN72310) in the feedback loop, as seen in Figure 2.26b. In this example the SN72310 output furnishes the bias current required, while its input bias is only about 2 nanoamps.



a. USING A TRANSISTOR



b. USING A VOLTAGE-FOLLOWER AMPLIFIER

Figure 2.26. Active Input-Current Compensation of an Inverting Amplifier

Active Compensation of a Voltage-Follower Amplifier – The use of a single transistor is possible with the inverter because the non-inverting input is grounded. With a voltage follower the non-inverting input, which must be compensated, can be at any voltage with respect to ground. The external transistor's base and emitter currents must be constant even though the base (and non-inverting input) voltage is varying. For this reason a current generator (Figure 2.27) using the 2N3810 (to minimize temperature effects) injects the necessary current into the 2N2605's emitter. The result is a constant base current that can be set to compensate properly for the non-inverting input bias. The potentiometer R4 is adjusted to provide input bias compensation.

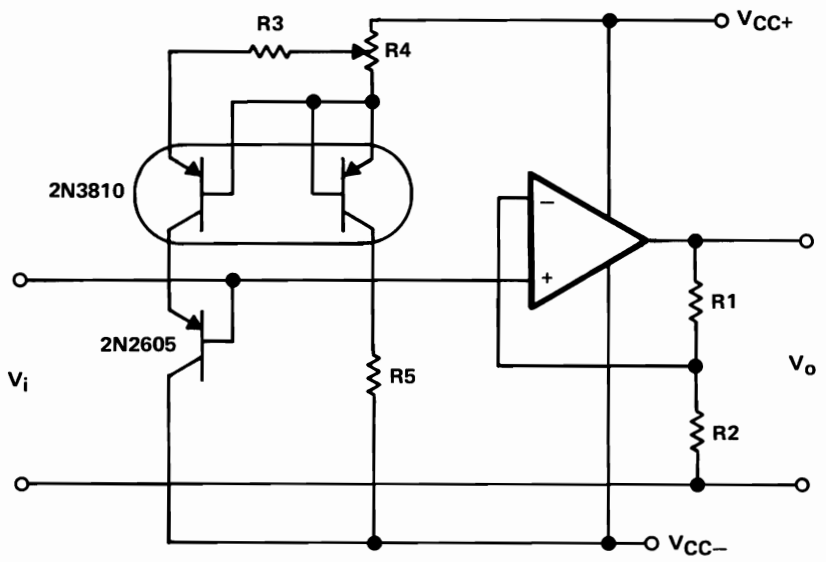


Figure 2.27. Active Input-Current Compensation of a Voltage-Follower Amplifier

Summary – Input-offset-voltage compensation should be set, using a sensitive meter, with the feedback resistance shorted and inputs grounded to minimize effects of bias currents. After offset voltage has been corrected, and with the circuit in operating order, input-bias-current compensation controls may be adjusted to obtain zero output voltage.

It should be noted that bias-current compensation techniques are normally required for general-purpose operational amplifiers; they are not applicable to devices such as the SN72308 super-beta amplifiers. The input bias currents of most super-beta devices are very low and do not generally cause significant offset voltages.

2.4.3 Compensation of Circuit Frequency Response and Closed-Loop Bandwidth

An operational amplifier may be considered as a voltage generator followed by an RC network which causes gain reduction and increased phase shift as the frequency increases, even though gain reduction and phase shifts occur in several stages of the amplifier. As frequency is increased it is important that gain be reduced to unity before the phase shift becomes 180°. If amplifier gain is ≥ 1 when the phase shift becomes 180°, oscillations will occur. Even with low-frequency input signals, oscillation will occur if the high-frequency phase shift and gain characteristics of the amplifier make it possible.

Frequency-compensation networks are defined for each type of amplifier. In many cases the minimum or unity-gain requirements for compensation are more severe than for other applications. Also, non-linear applications (limiting, integrating, etc.) require more compensation. Circuits which are internally compensated, or those which must operate in a number of different applications without adjustment of compensation, will need to be compensated for the unity-gain condition to assure stability.

Frequency Compensation for SN72702 Amplifiers — For closed-loop applications with gains of 250 (48 dB) or greater, external frequency compensation is unnecessary. Where gain is less than 48 dB, one or more of the available frequency-compensation networks must be utilized.

Output Phase-Lead Compensation — Used for gains greater than 38 dB, phase-lead compensation is accomplished by connecting a capacitor between the lead and lag terminals of the SN72702 (Figure 2.28). With this compensation, bandwidth is increased as the second breakpoint is moved out to about 30 MHz. The optimum value for this capacitor is in the 50- to 100-pF range.

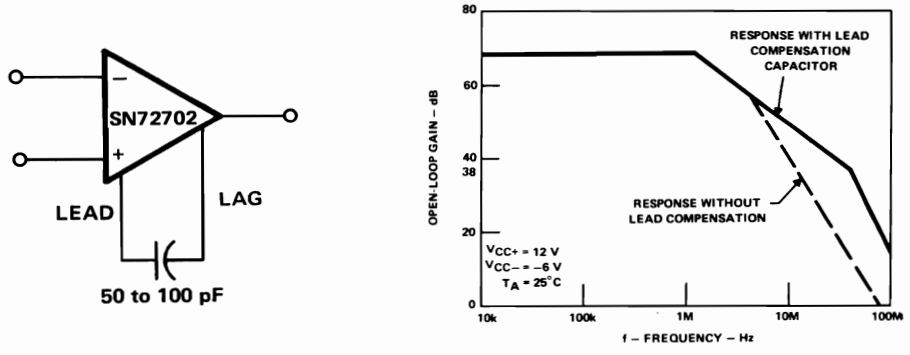
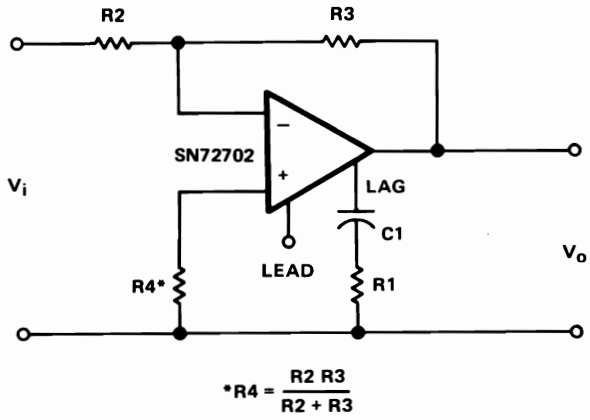


Figure 2.28. Output Phase-Lead Compensation of the SN72702



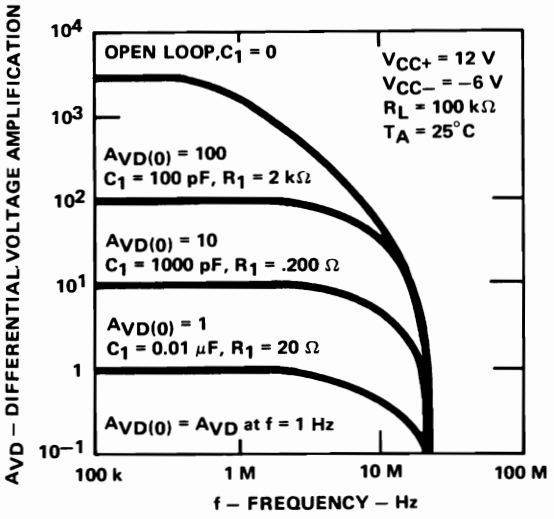


Figure 2.29. Output Phase-Lag Compensation of the SN72702

Output Phase-Lag Compensation – This compensation is used for applications which have gains between 48 dB and unity (Figure 2.29). Values of the compensating-network components are calculated as follows:

$$R1 = 20\left(1 + \frac{R3}{R2}\right) \text{ and } C1 = 10^{-2}\ \frac{R2}{R2 + R3}$$

where R is in ohms and C is in μF.

Input Phase-Lag Compensation — Output lag compensation limits the peak-to-peak voltage swing at high frequencies. With input phase-lag compensation this does not happen (Figures 2.30 and 2.31). Figure 2.30 shows a balanced differential input circuit with input compensation.

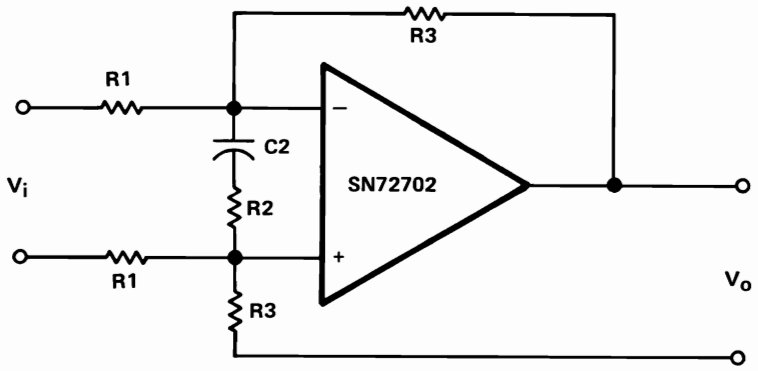


Figure 2.30. Input Phase-Lag Compensation of the SN72702

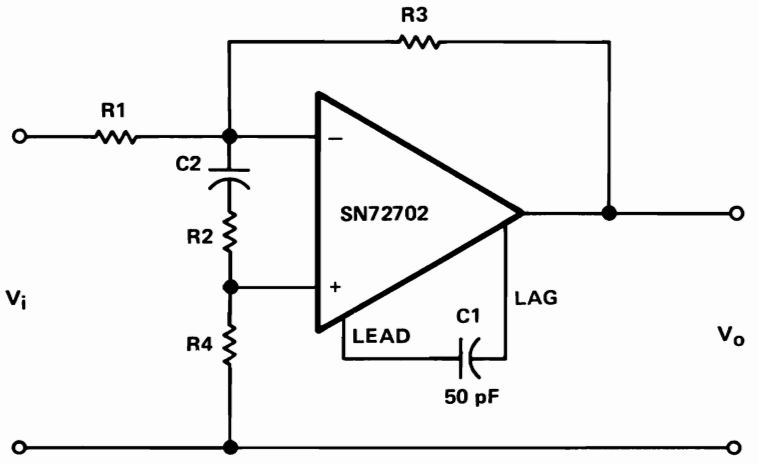


Figure 2.31. Mixed Lead-Lag Compensation of the SN72702

Mixed Lead-Lag Compensation — A combination of output lead compensation with input lag compensation (Figure 2.31) allows better control over the response characteristics without limiting output voltage swing. Calculation of compensation components is as follows:

$$C1 = 50 \text{ pF}$$

$$R2 = 20\ R3 \text{ and } C2 = \frac{0.01}{R3}$$

where R3 is in kilohms, R2 is in ohms, and C2 is in μF

For example:

$$\text{if } R3 = 10\ k\Omega,\ R2 = (20)(10) = 200\ \Omega, \text{ and } C2 = \frac{0.01}{10} = 0.001\ \mu F$$

Frequency Compensation for SN72709 Amplifier — The SN72709 has three gain stages and an open-loop gain in excess of 90 dB. Its high gain and phase shift allow it to oscillate even in the open-loop configuration. For proper operation two compensation networks are required: collector-to-base feedback around the second stage, and also around the output stage. Figure 2.32a shows these compensation networks, R1-C1 and C2, generally required for circuit stability. Most of the roll-off (60 dB) is provided by R1-C1, with the additional required compensation being supplied by C2.

Capacitive output loading may result in circuit instability, even with R1-C1 and C2 compensation. Therefore, in applications in which the load is somewhat capacitive, it is necessary to add some resistance (typically 50 ohms) in series with the output, isolating the output compensation from the load. As most loads will exhibit some capacitance, the 50-ohm series resistor is recommended for all applications to ensure stability.

The table in Figure 2.32a lists compensation components recommended for closed-loop operation of non-inverting amplifiers with gains of 0 to 60 dB. These values have been calculated for worst-case device parameters and should assure a phase margin of 45° or greater. Note that the value of R1 is 1.5 kΩ for gains up to 50 or 60 dB. The value of R1 may be larger than 1.5 kΩ in these examples, but never smaller. This resistor is necessary to prevent roll-off extension into the range where the Miller effect will produce an abnormal phase shift, causing oscillations. For inverting amplifiers (Figure 2.32b) the capacitor values C1 and C2 should be multiplied by the factor R3/(R3 + R2) to obtain equivalent bandwidths. Depending on the particular device being used, the —3-dB bandwidth will be from 0.4 to 1.8 MHz.

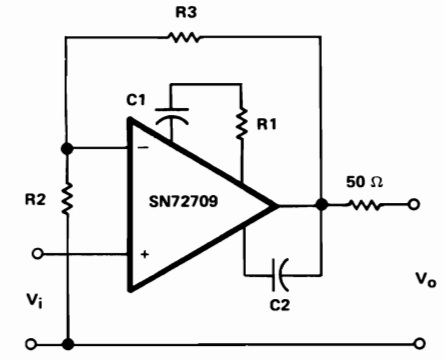
As with the SN72702, the output voltage swing of the SN72709 is limited at high frequencies. To improve the output capability it is possible to use the input compensating network shown in Figure 2.32c. It should be remembered that

although the output voltage swing is improved with this technique, the effective input noise is greater.

The compensation component values are calculated as follows:

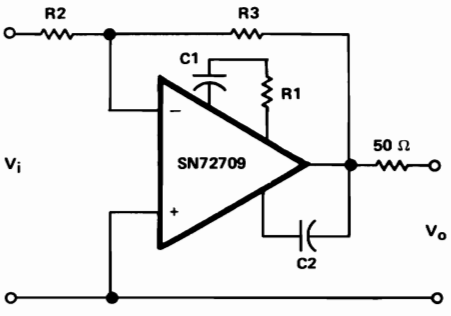
$$R4 = 20\ R3 \text{ and } C3 = \frac{9}{R3}$$

where R3 is in kΩ, R4 is in ohms, and C is in μF.

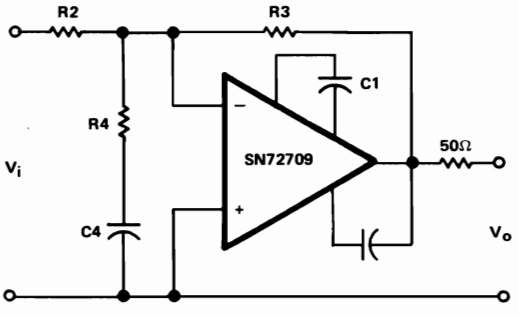


a. Non-inverting

GAIN dB	C1 pF	R1 kΩ	C2 pF
0	5000	1.5	200
20	500	1.5	20
40	100	1.5	3.0
60	10	0	3.0



b. Inverting



c. Inverting with Input Compensation

Figure 2.32. Frequency Compensation of the SN72709

Frequency Compensation of the SN72741, SN72747, SN72558, SN72307, and SN72771 — These operational amplifiers are internally compensated through use of a 30-pF MOS feedback capacitor across an intermediate stage. The frequency response, as seen in Figure 2.33, is rolled off at the rate of 6 dB per octave (20 dB per decade) to unity gain at a frequency of about 1 MHz. The amplifiers are therefore considered to be stable in any closed-loop gain configuration within the limits of circuit-layout and supply-stability criteria.

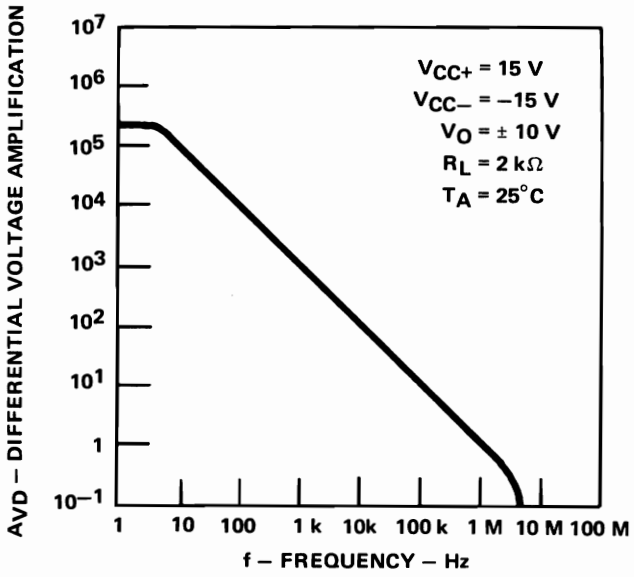


Figure 2.33. Frequency Response of the SN72741, SN72747, SN72558, SN72307, and SN72771

Frequency Compensation of the SN72748, SN72301A, SN72770, and SN72308A — These amplifiers have a terminal to provide external frequency compensation. If an external-compensation capacitor of 30 pF is used, the response would be similar to that of the SN72741 type amplifiers shown in Figure 2.33. External compensation has the distinct advantage that the capacitor value may be adjusted to provide better frequency response in higher gain applications. For gains higher than unity the compensation capacitance may be adjusted as follows: $C = 60/(1 + G)$ where G is the closed-loop gain. Therefore for unity gain $C = 60/(1 + 1) = 60/2 =$ 30 pF; but for a gain of 10 the capacitance could be reduced to a value of $60/(1 + 10)$, or about 5.6 pF. Regardless of the closed-loop gain, it is recommended that a minimum of 3.0 pF compensation be used to ensure stability. Figure 2.34 shows the relative response characteristics for different values of C using an SN72748. The result would be similar for the other device types in this group.

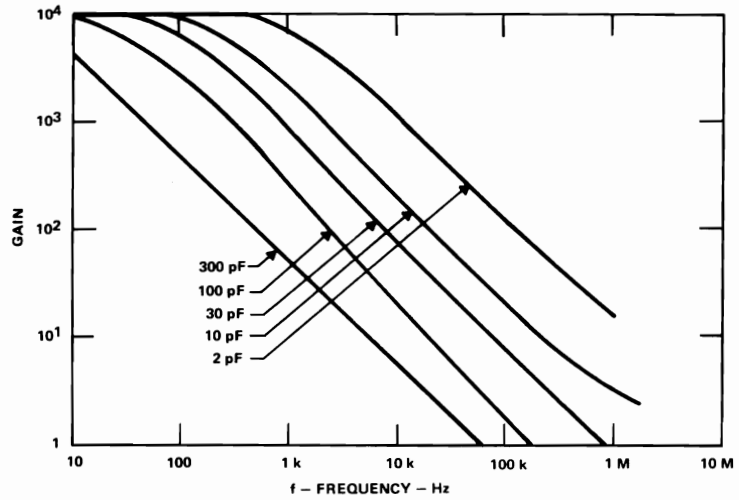


Figure 2.34. Measured Frequency Response of an SN72748

Additional SN72301A Compensation Characteristics — A different method of frequency compensation, available with the SN72301A type devices, allows a higher frequency response and greater output slew rate capability. The lateral PNP transistors, used to level-shift the signals from the input stage, have poor frequency response and introduce excessive phase shift. As a result the unity-gain bandwidth is limited to 1 MHz, and the slew rate is only about 0.5 volt per microsecond. Either of two techniques may be utilized to improve the circuit performance.

One technique is the use of phase-lag compensation as seen in Figure 2.35. Instead of connecting one capacitor across the compensation terminals, two capacitors are used. Capacitor C1 is connected between the second-stage base (terminal N1) and the load. Its value will be the same as before: 30 pF at unity gain or less. For higher gain applications another capacitor, C2, is connected in series with the output, as shown, providing only an ac path from the device output to the load and C1. The recommended value for C2 is 10 C1. A two-to-one improvement in frequency response and slew rate results from this technique.

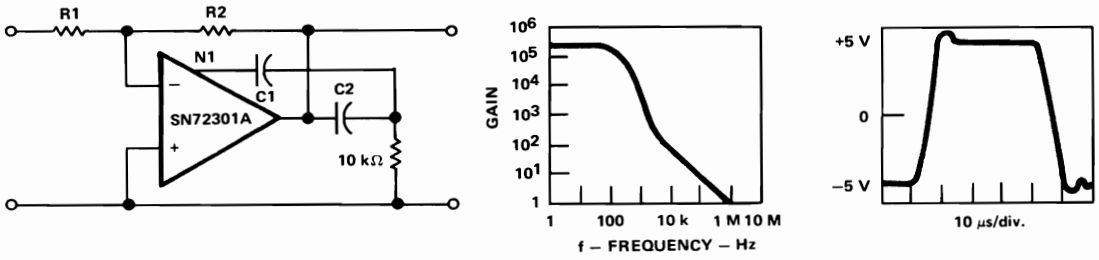


Figure 2.35. Phase-Lag Compensation of the SN72301A

Further improvement in the slew rate can be achieved by using phase-lead or feed-forward compensation as shown in Figure 2.36. Again two capacitors are used. The first capacitor is 150 pF, connected between the inverting input and the base of the second stage (terminal N1). This in effect bypasses the slow lateral PNP transistors at high frequencies and allows sufficient output drive for greater slew rates. Slew rates of up to 10 volts per microsecond are possible with this type of compensation.

An additional capacitor C1, connected across the feedback resistor, is used to shape the frequency response. C1 must provide the roll-off in response at the desired frequency. Its value therefore is determined by the value of the feedback resistor R2 and the desired roll-off frequency f_o (f_o must be less than 3.5 MHz). The value for C1 is calculated as follows: $C1 = 1/(2\pi f_o R2)$.

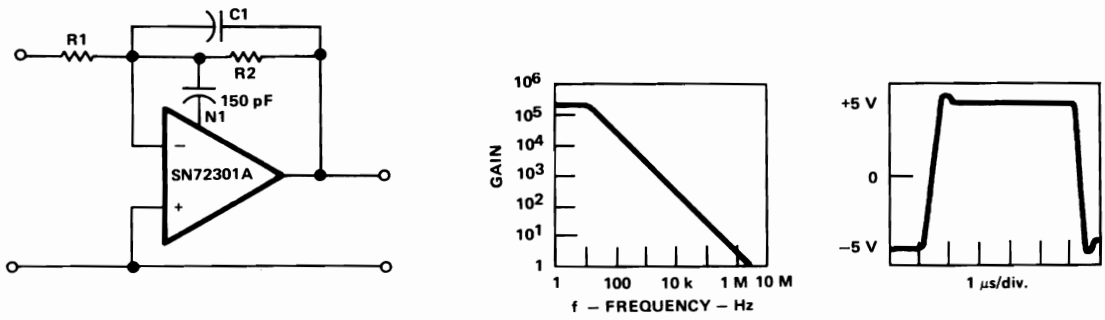


Figure 2.36. Feed-Forward Compensation of the SN72301A

Frequency Compensation of the SN72308 — A method of shunt compensation (Figure 2.37) may be used to improve the stability margin in low-frequency applications and increase supply ripple rejection. Supply rejection with 100-pF compensation is improved by a factor of 10 over the conventional compensation. The 100-pF capacitor is connected from the output of the second gain stage (compensation 2 terminal) to ground. The resulting excellent stability permits accurate sensing of voltages in such applications as an error amplifier for voltage regulators.

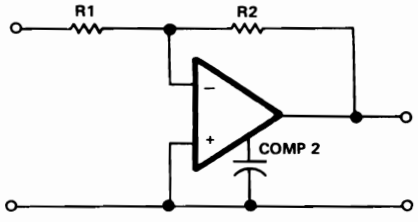


Figure 2.37. Shunt Compensation of the SN72308

2.5 SINGLE-ENDED AMPLIFICATION

2.5.1 Voltage-Follower Amplifiers

In single-ended applications one input is connected to ground or a fixed reference potential, and the signal is applied to the other. One example is the voltage follower (Figure 2.38).

This configuration has an output voltage which follows, or is in phase with, the input. If a feedback resistor R2 and termination resistor R1 are used as shown in Figure 2.38 the output voltage V_O will generate a current i through them. The resulting voltage drop across R1 is equal to V_i, the input voltage. As a result $i = V_i/R1$ and $V_O = i(R1 + R2)$. From these two equalities it is seen that $V_O = V_i(R1 + R2)/R1$, which is the voltage transfer function. A specific type of the voltage follower results when R2 is zero and R1 is infinite. The voltage transfer function reduces to $V_O/V_i = 1$, and the circuit is a unity-gain voltage follower with theoretically infinite input resistance and zero output resistance.

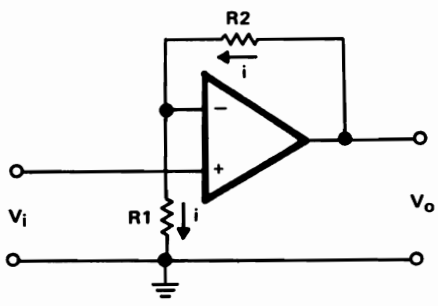


Figure 2.38. Basic Voltage-Follower Amplifier

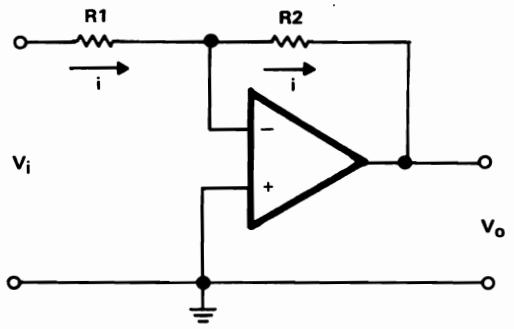


Figure 2.39. Basic Inverting Amplifier

2.5.2 Inverting Voltage Amplifiers

In the inverting-amplifier configuration (Figure 2.39) the output voltage is opposite in polarity to that of the input voltage. Again the current $i = V_i/R1$. With the inverting input appearing as a virtual ground (zero volts but drawing no current) the current i flows through R2, resulting in $V_O = -i\,R2$; therefore $V_O = -V_i(R2/R1)$. Again the theoretical output resistance is zero, but the input resistance is equal to $V_i/i = R1$. If a high input resistance is desired the inverter could be preceded by a voltage follower as shown in Figure 2.40.

If all of the resistor values are equal they cancel and $V_o = -(V_{i1} + V_{i2} + V_{i3})$.

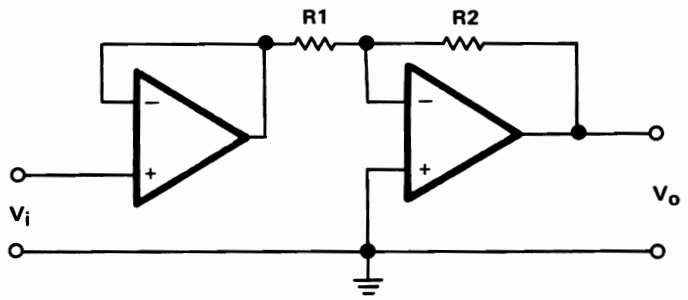


Figure 2.40. High-Input-Impedance Inverting Amplifier

2.5.3 Operational-Amplifier Voltage Adders

An inverting or non-inverting amplifier may be used for adding several input signals. An inverting adder circuit is shown in Figure 2.41. Applying Kirchhoff's laws, we see that $i_1, +i_2 + i_3 = i_4$. Also it follows that

$$\frac{V_{i1}}{R1} + \frac{V_{i2}}{R2} + \frac{V_{i3}}{R3} = -\frac{V_o}{R4}$$

therefore

$$V_o = -R4\left(\frac{V_{i1}}{R1} + \frac{V_{i2}}{R2} + \frac{V_{i3}}{R3}\right)$$

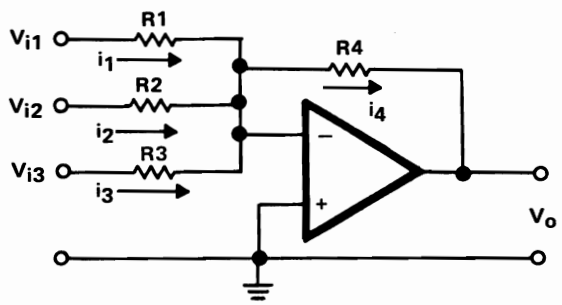


Figure 2.41. Inverting Adder

When a non-inverting amplifier is used (Figure 2.42) the currents are added in a real resistance R4 rather than in a virtual zero resistance, as was the case with an inverting amplifier. R4 will be very small relative to the input resistors. The voltage u generated across R4 is $u = R4(i_1 + i_2 + i_3)$. This voltage u also appears at the inverting input, as the two inputs have virtually the same potential. Therefore $i_5 = u/R5$ and $V_o = u(R5 + R6)/R5$. In most cases R4 and R5 are chosen to be equal, thus making i_4 and i_5 equal. It follows then that since

$$u = R4\left(\frac{V_{i1}}{R1} + \frac{V_{i2}}{R2} + \frac{V_{i3}}{R3}\right)$$

therefore

$$V_o = R4\left(\frac{V_{i1}}{R1} + \frac{V_{i2}}{R2} + \frac{V_{i3}}{R3}\right)\left(\frac{R5 + R6}{R5}\right)$$

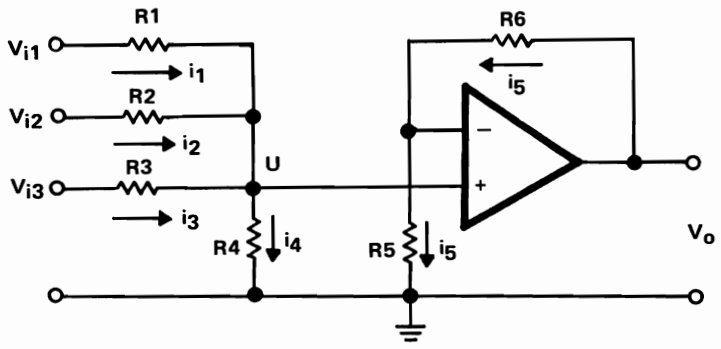


Figure 2.42. Non-Inverting Adder

2.6 SINGLE-ENDED AMPLIFIER APPLICATIONS

2.6.1 Low-Noise Preamplifier

Figure 2.43 shows an SN72709 connected as a low-noise audio preamplifier. It is wired to operate from a single +12-volt supply, with V_{CC+} tied to the supply and V_{CC-} connected to ground. The amplifier's quiescent point, or zero reference, is determined by the resistor divider network R3 and R4. It will be about 1/2 of the V_{CC+} level, or 6 volts, and is bypassed by C2 and C3 to provide good low- and high-frequency filtering. The input signal may be applied in one of two ways:

1) Between point A and ground, with dc isolation provided by C4. This capacitor will determine the low-frequency roll-off point.
2) Between points B and C, in which case C4 would not be necessary. In this case the input signal must be floating (not terminated to ground), as neither point B nor C can be connected to ground. The input signal could be transformer-coupled into points B and C to maintain a floating condition.

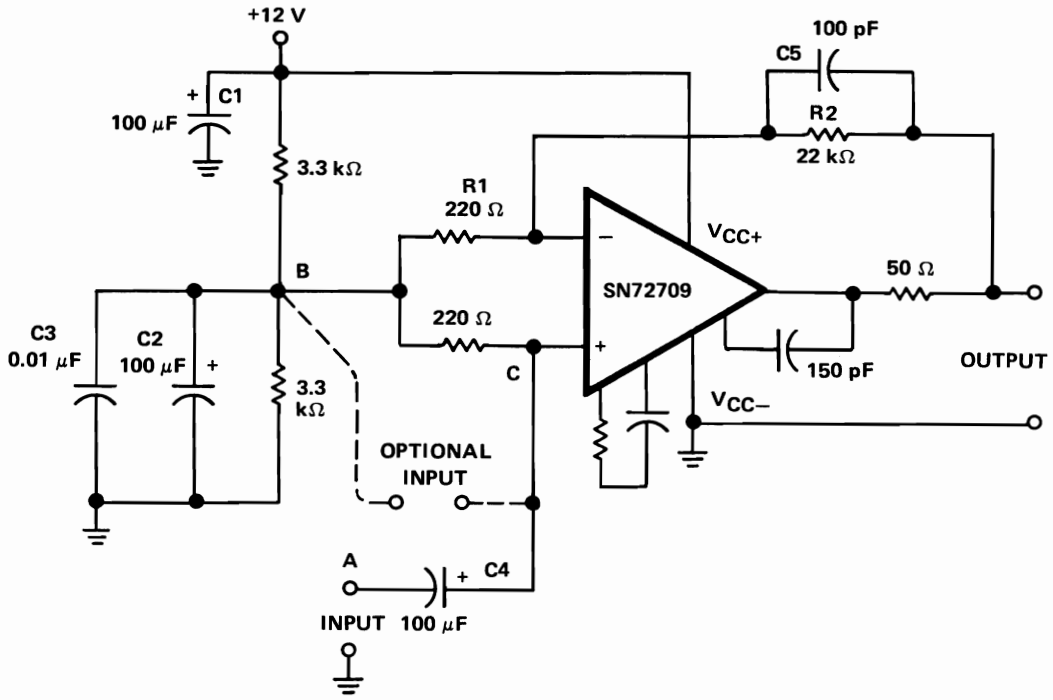


Figure 2.43. Low-Noise Preamplifier

The resulting SN72709 audio preamplifier characteristics are:

Equivalent input noise	$\leqslant 2\ \mu V$
Input impedance (determined by R_5)	220 Ω
Pass band (±1 dB)	20 Hz to 20 kHz
C4 controls the low-frequency roll-off	
C5 controls the high-frequency roll-off point.	
Amplifier gain (set by R1 and R2)	40 dB

These characteristics apply for V_{CC} values from +8 volts to +30 volts.

2.6.2 SN72558 as a Stereo Preamplifier

The SN72558, being a dual-channel internally compensated device, is easily used as a stereo preamplifier. The small L or P package allows it to be employed in compact, battery-operated systems. Figure 2.44 shows the basic connections required for a stereo preamplifier using a minimum of external components. The resulting performance characteristics are:

Equivalent input noise (over 10 kHz BW)	20 μV
Input impedance (set by R1)	200 ohms
—3 dB bandwidth	100 Hz to 20 kHz
(Low frequency limited by C1)	
Gain (determined by R2 and R3)	40 dB
Interchannel crosstalk rejection	>60 dB

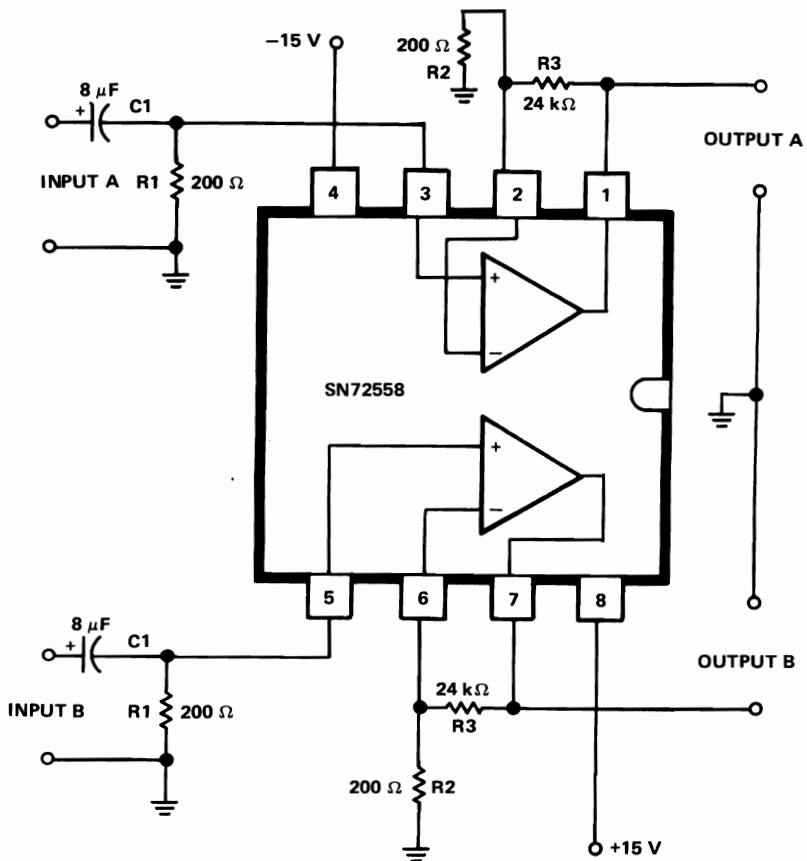


Figure 2.44. Stereo Preamplifier

2.6.3 Stereo Preamplifier for a Tape Recorder

The SN72301A has very low input offset and bias currents, making it a good selection for high-performance, low-noise audio applications. In this application, using two SN72301A devices as shown in Figure 2.45, feedback networks

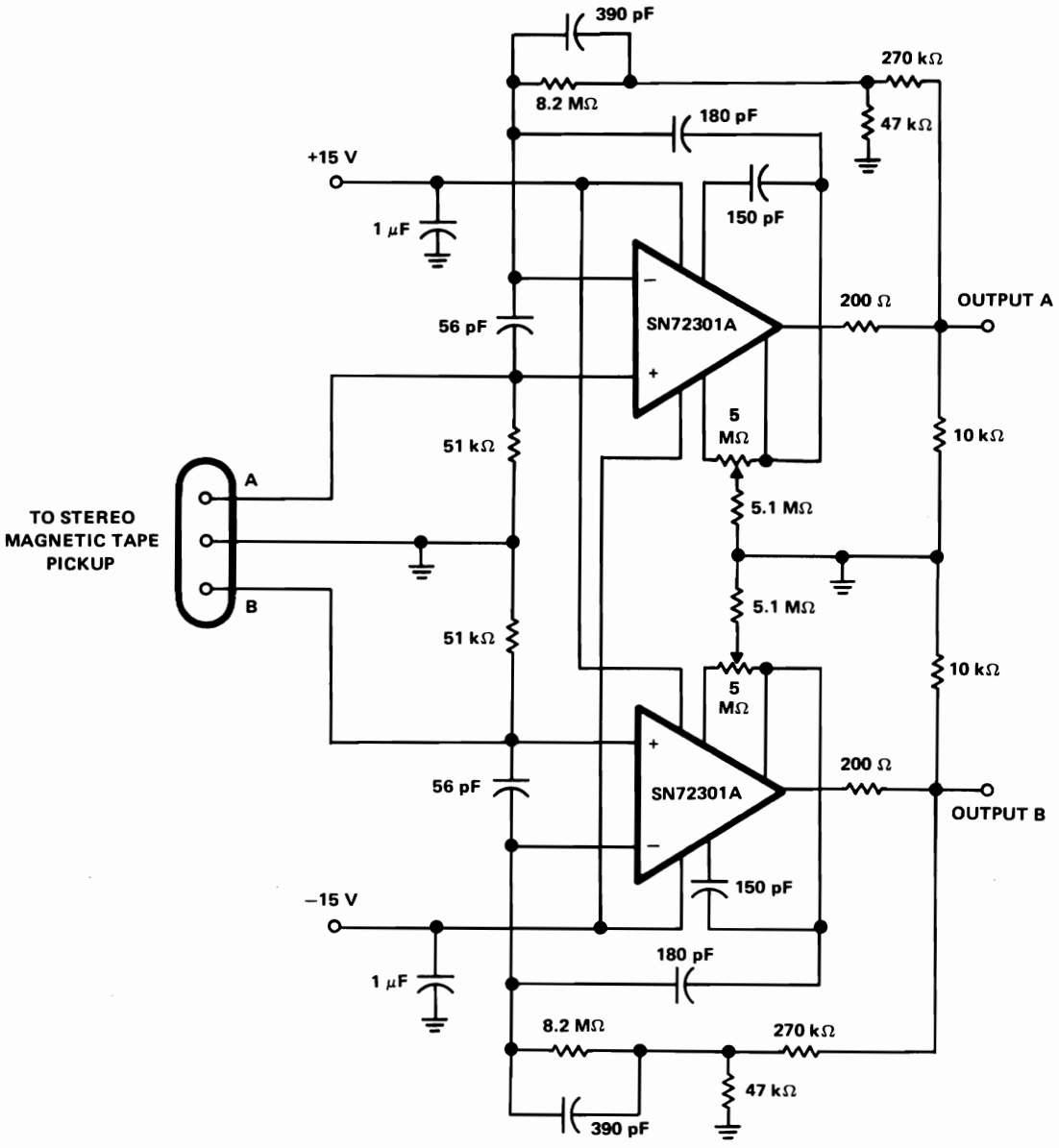


Figure 2.45. Stereo Preamplifier for Magnetic Tape Pickup

demonstrate a technique for providing uniform gain throughout the audio range. Figure 2.46 shows the resulting response curve with a relatively flat response up to 25 kHz. Symmetrically balanced output signals are provided by separate offset controls for each channel. Other general characteristics are:

Amplifier gain	15 dB
Output noise	—70 dB
Crosstalk rejection	>60 dB

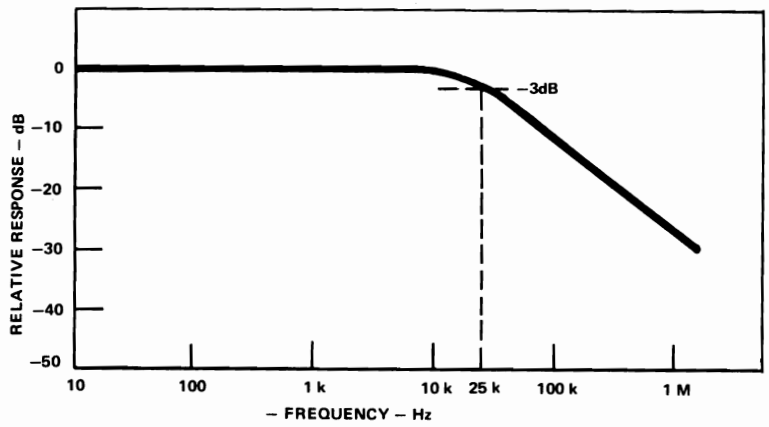


Figure 2.46. Frequency Response for Circuit in Figure 2.45

2.6.4 SN52702A as a 10-MHz Amplifier

Although the SN52702A is an operational amplifier and generally considered an audio amplifier, its broad bandwidth capability allows it to be used in the intermediate RF frequency ranges as well. The schematic diagram (Figure 2.47) illustrates the circuitry used for a broadband application of the SN52702A. The unity-gain bandwidth of this configuration is about 50 MHz typically.

A 10-kΩ feedback resistor and 330-Ω input termination set the low-frequency gain at 30 dB. The bandpass curve (Figure 2.48) is relatively flat from dc to about 20 MHz, with its —3 dB point falling at 30 MHz. Note that mixed input and intermediate stage lead-lag networks are used for frequency compensation. R1 and C1 at the input provide phase-delay compensation, and C2 supplies some phase-advance compensation. Simplicity of operational-amplifier gain-control techniques and the broad bandwidth capability of the SN52702A make it desirable for many medium-frequency applications.

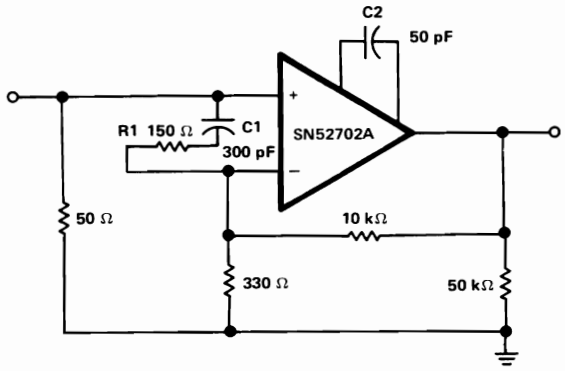


Figure 2.47. 30-dB, 10-MHz Amplifier

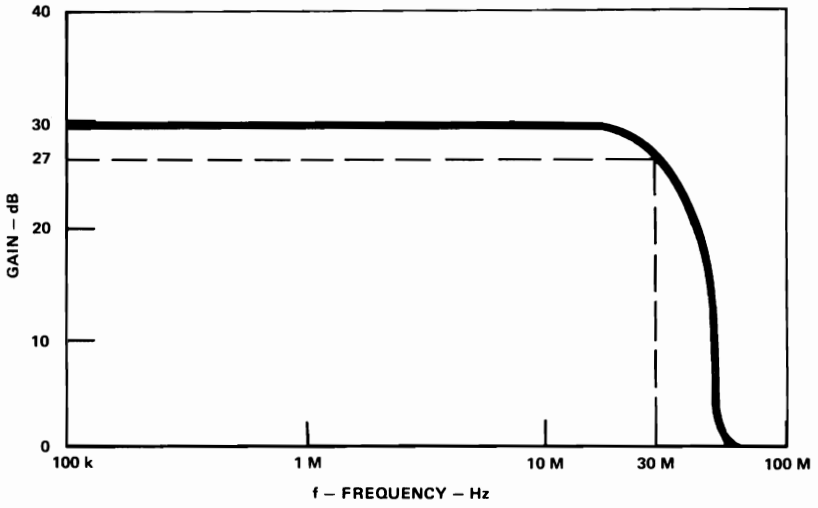


Figure 2.48. Frequency Response for Circuit of Figure 2.46

2.6.5 A 500-mW Audio Amplifier

An easily constructed low-power audio amplifier is illustrated in Figure 2.49. This circuit combines the internally compensated SN72741 type amplifier with the TIS92M and TIS93M matched complementary silicon transistors.

A 200-ohm resistor is used in series with the operational-amplifier output and its capacitive load to assure stability. For coupling between the operational amplifier and output transistors as well as between the output and load, 500-μF capacitors are used. These capacitors provide dc isolation, so that slight offset voltages of the operational amplifier or output stage do not appear at the output. A 1N914 diode

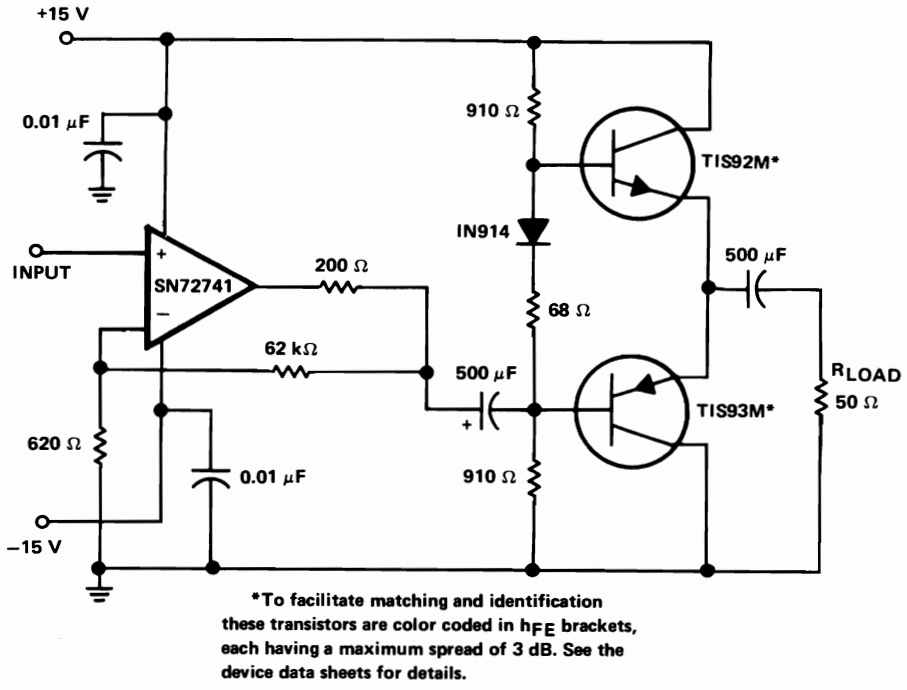


Figure 2. 49. 500-mW Audio Amplifier

and 68-ohm resistor provide proper compensation for transistor thresholds, preventing crossover distortion in the output stages. General performance characteristics are:

Output power (<2.0% distortion)	500 mW
Maximum power output (typical)	1.0 watt
Frequency response (−3 dB)	5 Hz to 20 kHz
Gain	40 dB

If operation at output power levels greater than 500 mW is required, heat sinks must be provided for the output transistors. In stereo applications, SN72747 or SN72558 dual-channel operational amplifiers would be used.

2.6.6 SN72709 as a Magnetic-Tape Preamplifier

The SN72709 was selected for this application because of its low input noise in the frequency range of operation. As is seen in Figure 2.50, the closed-loop gain is established by two different networks in the feedback loop. The first network in the feedback path, consisting of R4 and R5, determines the loop gain affecting all

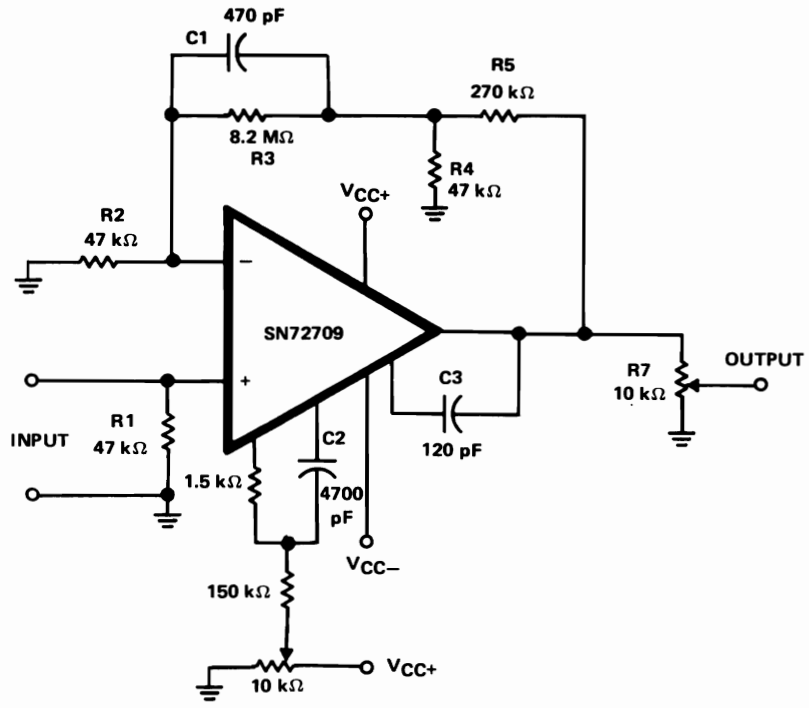


Figure 2.50. 60-dB Preamplifier for a Magnetic Tape Output

frequencies of operation. The second network, consisting of R3, C1, and R2, provides a gain segment that is frequency dependent. Capacitor C1 (470 pF), shunting the 8.2-megohm feedback resistor, reduces the gain at high frequencies. This compensation results in the bass boost desired in tape-recorder amplifiers.

C1 is effective at or above the frequency where the impedance Z (R3 in parallel with C1) is 0.707 R3. At this point the loop gain has been reduced by about 3 dB. Circuit calculations will show that the −3-dB breakpoint is at about 40 Hz. At very low frequencies (<20 Hz) the circuit gain is:

$$A = \left(\frac{R2 + R3}{R2}\right)\left(\frac{R4 + R5}{R4}\right)$$

or in this circuit

$$A = \left(\frac{47K + 8.2M}{47K}\right)\left(\frac{47K + 270K}{47K}\right) = (175.5)(6.74)$$

$$= 1182 \text{ or } 61.5 \text{ dB}$$

Due to circuit component errors and other factors, the system gain is taken as 60 dB at very low frequencies. At higher frequencies the gain is

$$A = \left(\frac{R2 + Z}{R2}\right)\left(\frac{R4 + R5}{R4}\right)$$

where Z is the resulting impedance of R3 in parallel with C1 at 20 kHz. For example, the product containing Z is reduced from 175.5 (the low-frequency value) to 1.36, and the resulting gain is therefore (1.36)(6.74), or about 19 dB. The roll-off in gain is shown in Figure 2.51.

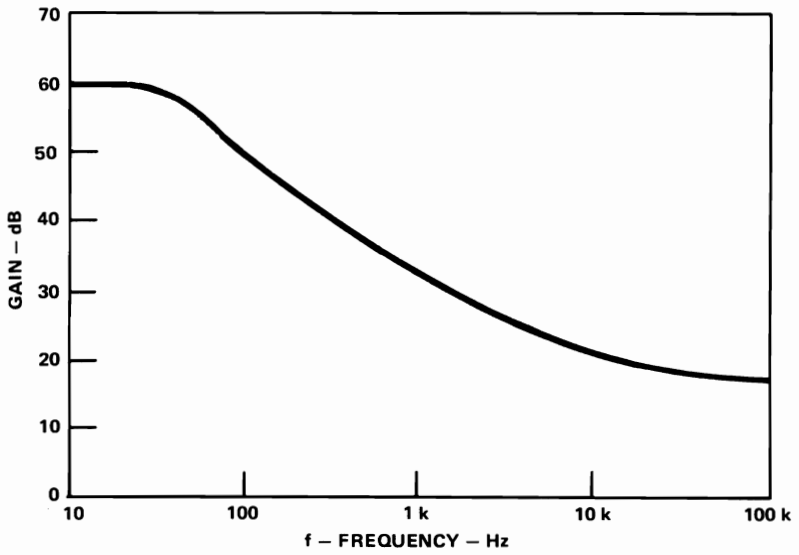


Figure 2.51. Frequency Response of Preamplifier in Figure 2.50

2.6.7 High-Input-Resistance Non-Inverting Amplifier

The basic non-inverting amplifier (Figure 2.52) can perform a valuable function provided the proper device is used. In this application a high input resistance (1 megohm) is required in matching a high-resistance source to a low-impedance load. Also it is important, with high-input termination resistances, that the input offset current be as low as possible to prevent a large dc output offset. Because of this the SN52107 was chosen for this application. With 1-megohm source resistance

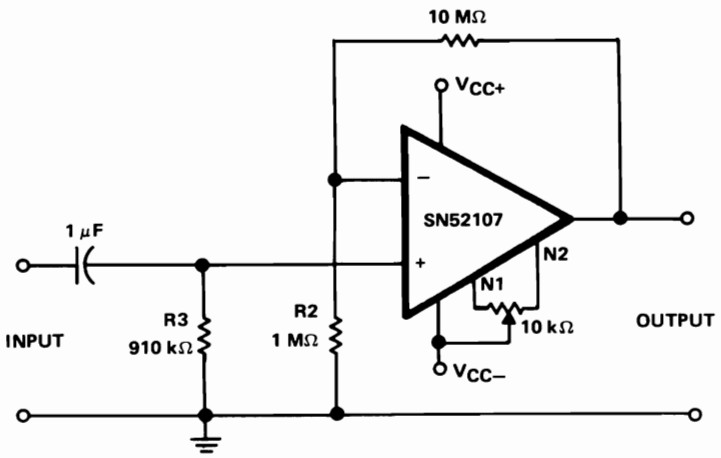


Figure 2.52. Non-Inverting Amplifier

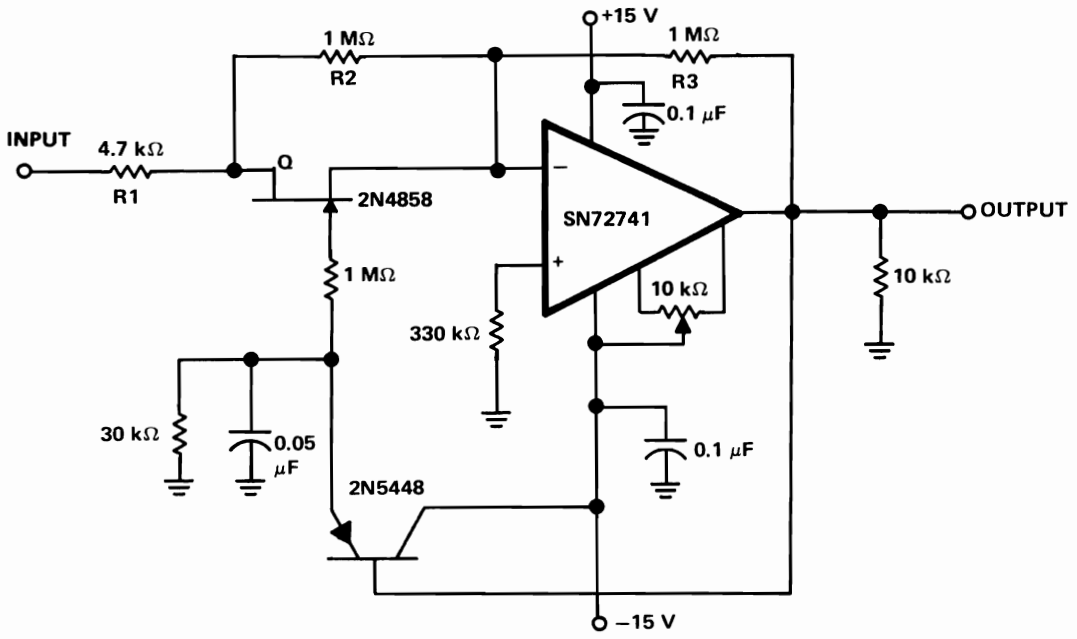
its 10-nA maximum input offset current (compared to 200 nA for the SN72741) will generate only 10 mV of input offset rather than the 0.2 volt associated with the SN72741. The SN52107 also has offset terminals to allow easy correction of normal input offset voltages.

2.6.8 Audio Amplifier with Automatic Gain Control

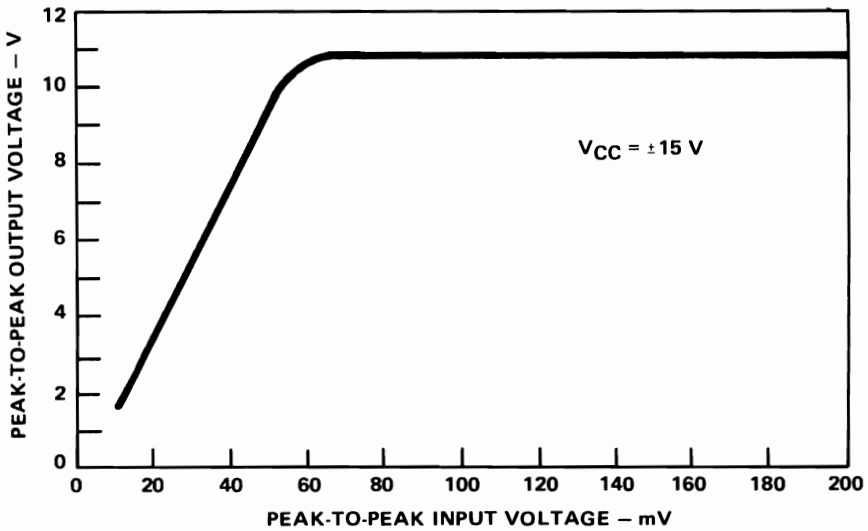
In the circuit of Figure 2.53a the amplifier gain is automatically controlled. This is accomplished by detection of the output signal with a 2N5448 silicon PNP transistor, and by feeding the filtered result to the gate of a 2N4858 silicon FET controlling the termination resistance of the inverting input. Any increase in output signal results in an increase in the negative dc voltage fed to the gate of the FET. This negative voltage results in less conduction through the FET, increasing the termination resistance and reducing the circuit gain.

With the FET turned off under large-input-signal conditions the circuit gain is R3/(R1 + R2), or 1M/1.005M $\approx$ 1. As the signal input decreases the FET will be turned on, increasing the gain to maintain the output level. At very low input levels the FET is fully on, with very low forward resistance. The circuit gain at this point is basically R3/R1 = 1M/4.7k, or 210. Thus the overall gain varies as much as 200:1. At intermediate signal levels the gain will be R3/(R1 + R2 $\|$ R_Q).

One of the primary advantages of AGC is that although there is high gain at low signal levels, 46 dB in this case, it is possible to handle large input signals without going into distortion. Figure 2.53b is a typical input versus output curve showing the AGC control, which is effective for input voltages ranging from 70 mV to 5 V, or 37 dB. This circuit will operate from supply voltages from ±7 V to ±15 V.



a. Schematic



b. AGC Characteristic

Figure 2.53. Audio Amplifier with AGC

2.6.9 Stereo-Headphone Amplifier

Many of the high-quality stereo headphones are low-impedance types requiring more drive power than is available from general-purpose operational amplifiers. The stereo amplifier in Figure 2.54 combines an economical general-purpose, dual-channel operational amplifier (SN72747) with equally economical *Silect*® transistors. This combination produces a stereo amplifier capable of driving the low-impedance (typically 300 ohms) stereo headphones with sufficient power for good fidelity. TIS92 and TIS93 complementary NPN-PNP transistors provide the desired impedance matching to the outputs of the SN72747.

This circuit was designed to provide 40-dB gain using source impedances of 4.7 kΩ (R1). The feedback resistances (R2) are therefore 470 kΩ. Different source impedances will result in different circuit gains unless the value of R2 is adjusted to maintain an R2/R1 ratio of 100. High-frequency roll-off is provided by 100-pF capacitors around the 470-kΩ feedback resistors. Offset voltage is adjusted by a separate control (P1) for each channel.

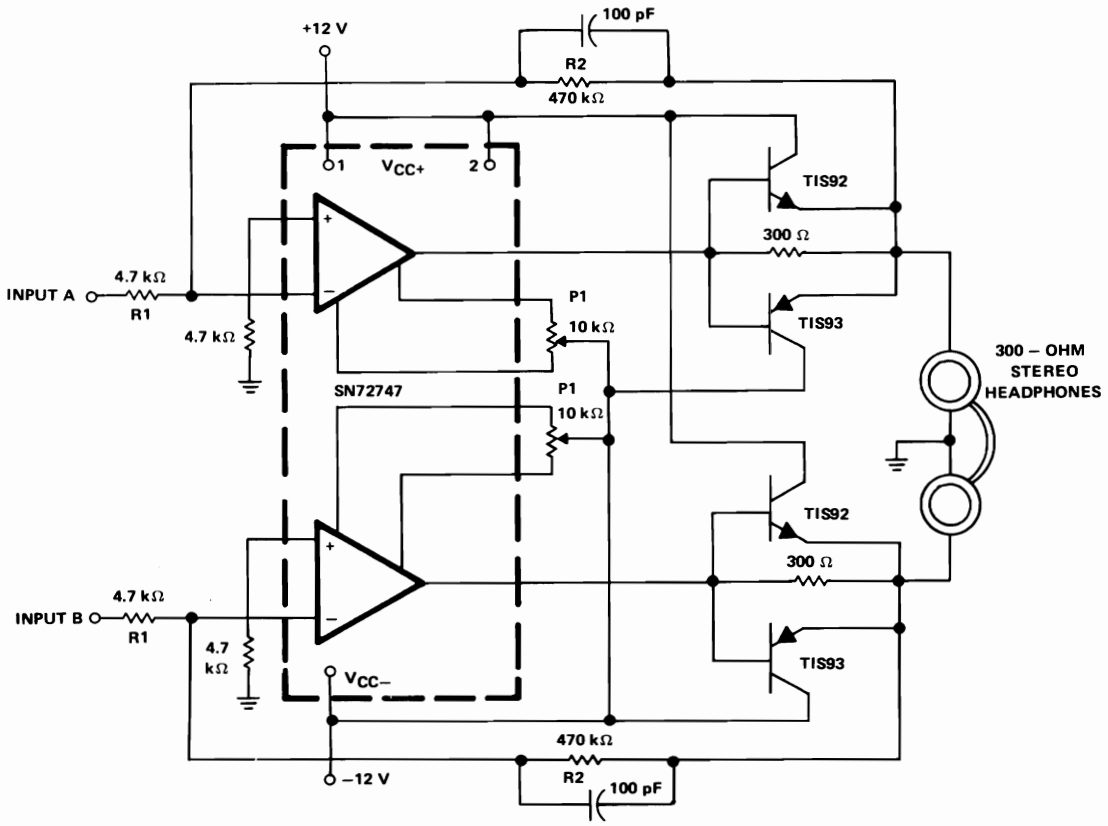


Figure 2.54. Stereo Headphone Amplifier

2.6.10 Bridge-Balance Indicator

In this application the 1N914 diodes in the feedback loop (Figure 2.55) result in high sensitivity and accuracy near the point of balance or equilibrium (R1/R2 = R3/R4). When the bridge is unbalanced (R1/R2 ≠ R3/R4) the amplifier's closed-loop gain is approximately R_F/r, where r is the parallel equivalent of R1 and R3. The resulting gain equation is $G = R_F(1/R1 + 1/R3)$. During an unbalanced condition the voltage at point A is different from that of point B. This difference voltage V_{AB}, amplified by the gain factor G, appears as a voltage V_O at the output. As the bridge approaches a balanced condition (R1/R2 = R3/R4), V_{AB} approaches zero. Under this condition the 1N914 diodes in the feedback loop lose their forward bias and their resistance increases. This results in an increase in the total feedback resistance, thus increasing the circuit gain and accuracy in detecting a balanced condition. Figure 2.56 indicates the effect of approaching balance on the circuit gain G.

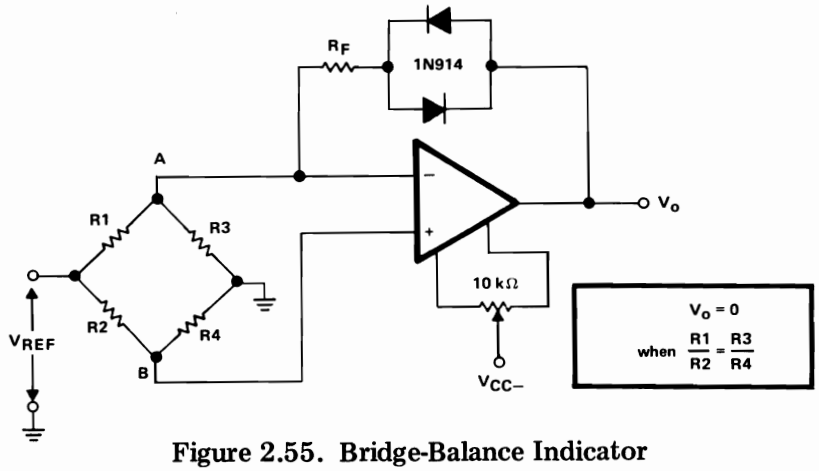


Figure 2.55. Bridge-Balance Indicator

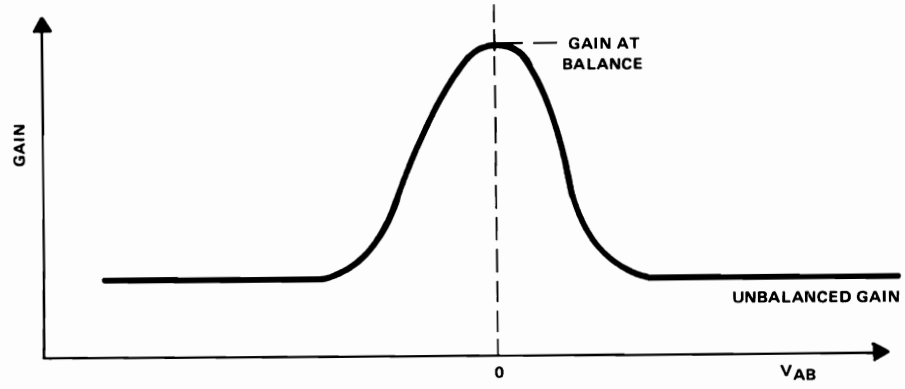


Figure 2.56. Gain as a Function of $V_{(A-B)}$

2.6.11 High-Input-Impedance Inverting Amplifier

If the source and input-termination impedances of an operational amplifier are high (>1 megohm), the offset voltages generated by input offset bias currents could be prohibitive. However, a super-beta type of amplifier such as the SN72770 has several advantages that assure adequate operating capability in applications of this type (Figure 2.57). The very low input offset current of 10 nA maximum at 25°C will generate only 50 mV of offset voltage. The device's high input resistance of 100 megohms allows operation from a 10-megohm source, as shown, with only slight loss in signal. In addition, external compensation allows adjustment of the compensation capacitor for optimum frequency response.

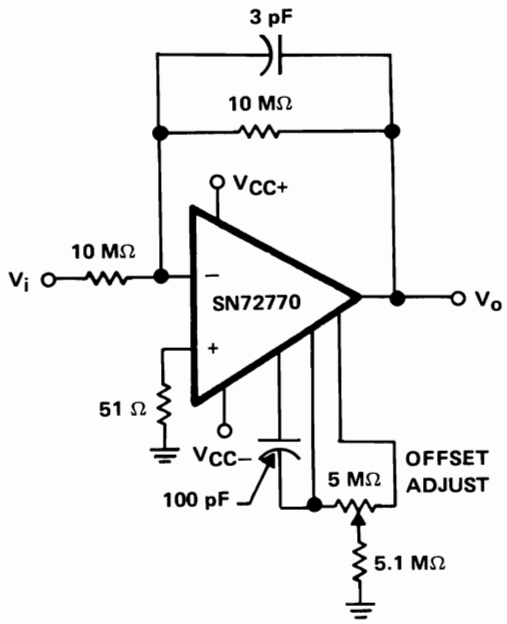


Figure 2.57. High-Input-Impedance Inverter

Further increase in input impedance is realized in the two-stage circuit shown in Figure 2.58. In this application the first stage is an SN72310 voltage follower with an input resistance of 10^{10} ohms or greater. The second stage is an SN72301A connected as a unity-gain inverter. Offset and frequency compensation are accomplished with the SN72301A, providing stable operation for the circuit.

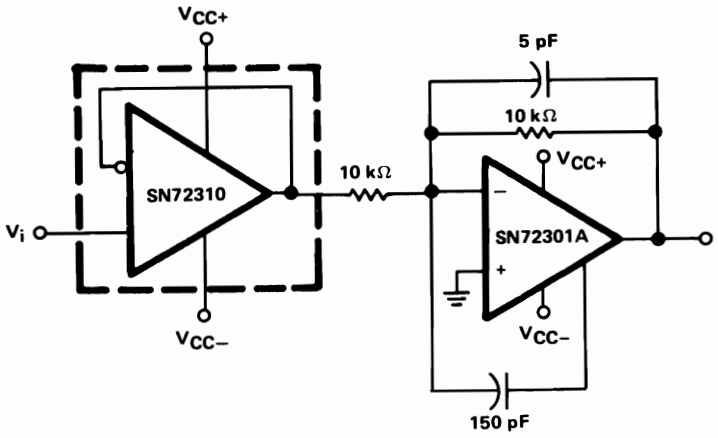


Figure 2.58. Very-High-Input-Impedance Inverter

2.6.12 Amplifier with Voltage-Controlled Gain

In this circuit (Figure 2.59) the gain is controlled by a negative control voltage (V_{GC}) applied to the base of Q3. Emitter currents for Q1 and Q2 are controlled by V_{GC}, the total current being equal to $V_{GC}/R6$. Controlling this current controls the circuit gain. The potentiometer P1 in the collector circuit of Q1 and Q2 is used to correct for offset voltages.

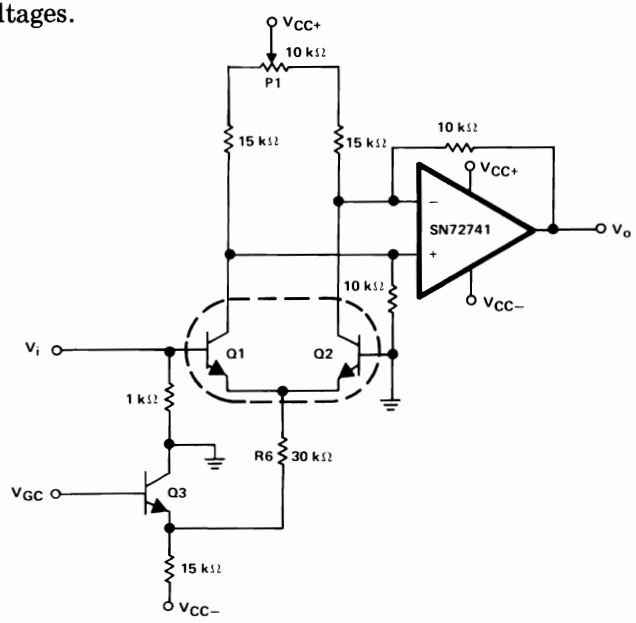


Figure 2.59. Amplifier with Voltage-Controlled Gain

The gain control voltage V_{GC} applied to the base of Q3 may be used to switch the amplifier on and off or to modulate the input signal. Figure 2.60 shows an input signal V_i, various V_{GC} modes, and the resulting output signal.

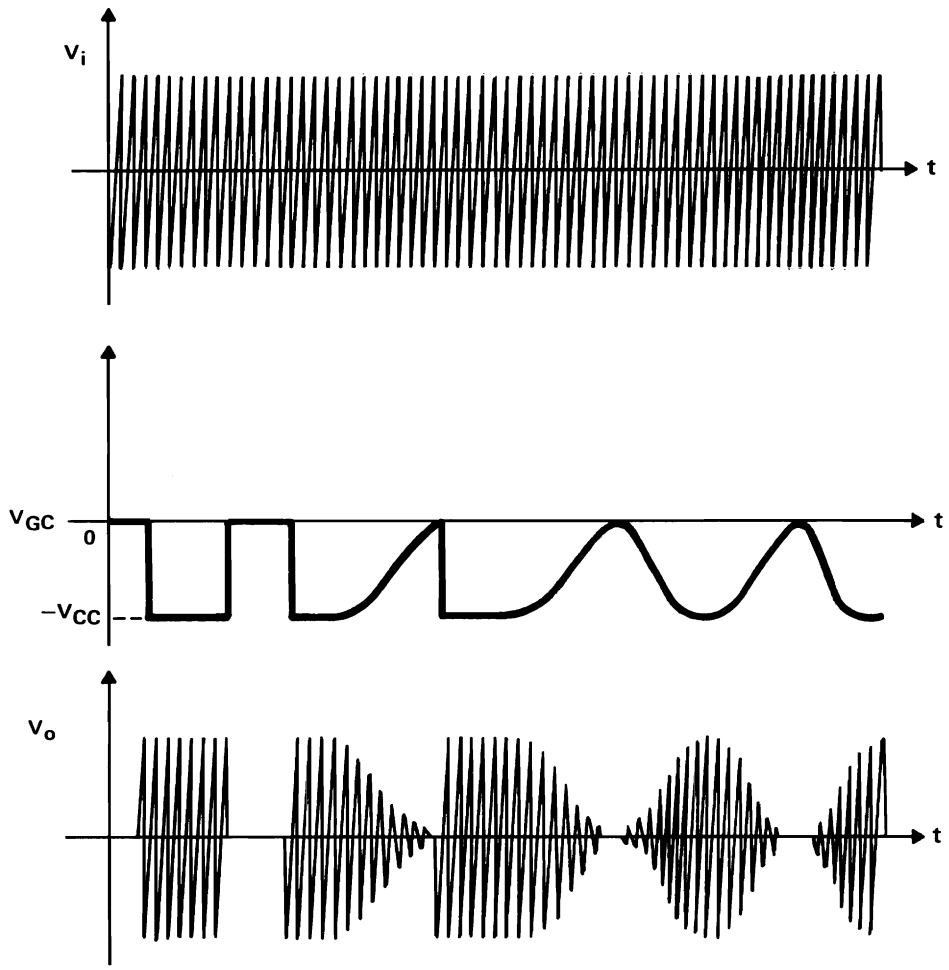


Figure 2.60. Input, Modulation, and Output Waveforms for Circuit of Figure 2.59

2.6.13 Multiple-Input, Logic-Controlled Analog Amplifier

In this application (Figure 2.61) the SN72748 operational amplifier has several inputs, all of which are switched on or off by TTL logic-control signals. Actual switching is accomplished with FETs which have relatively low on resistances

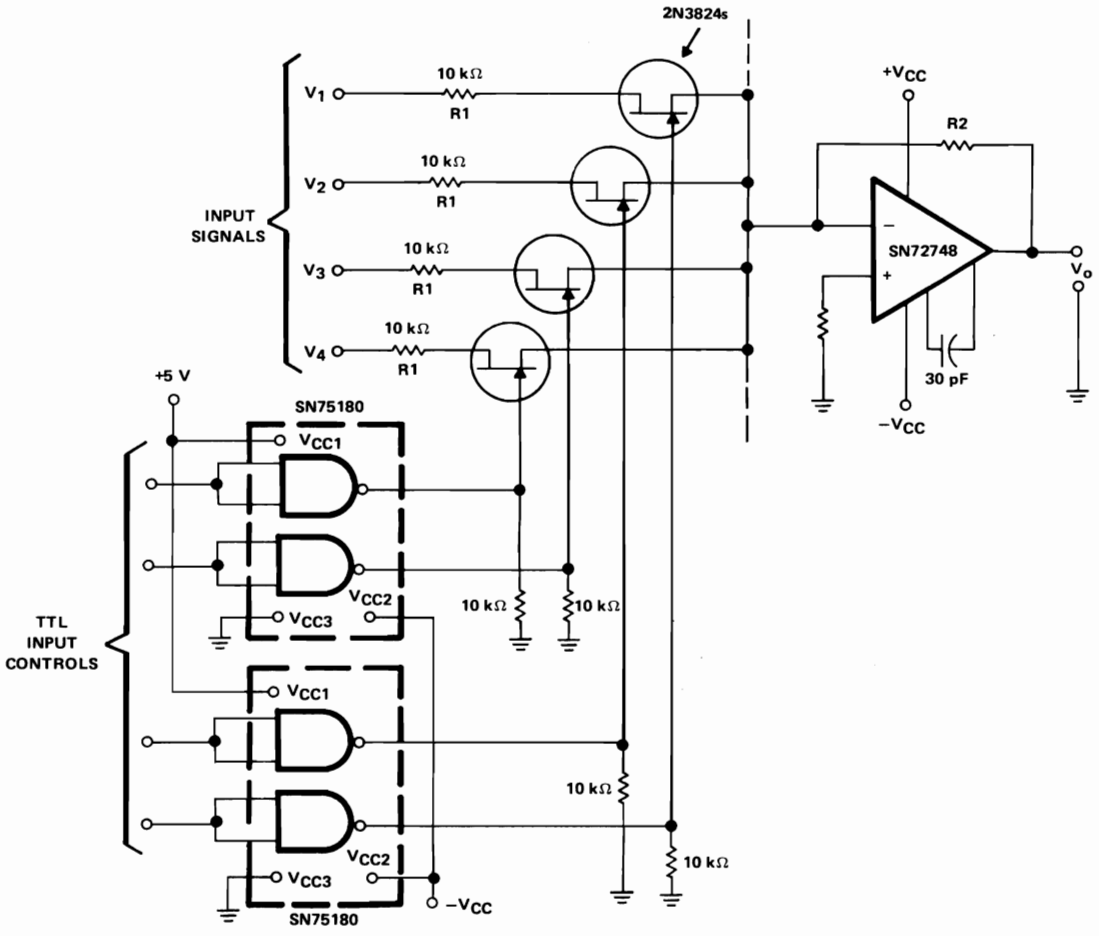


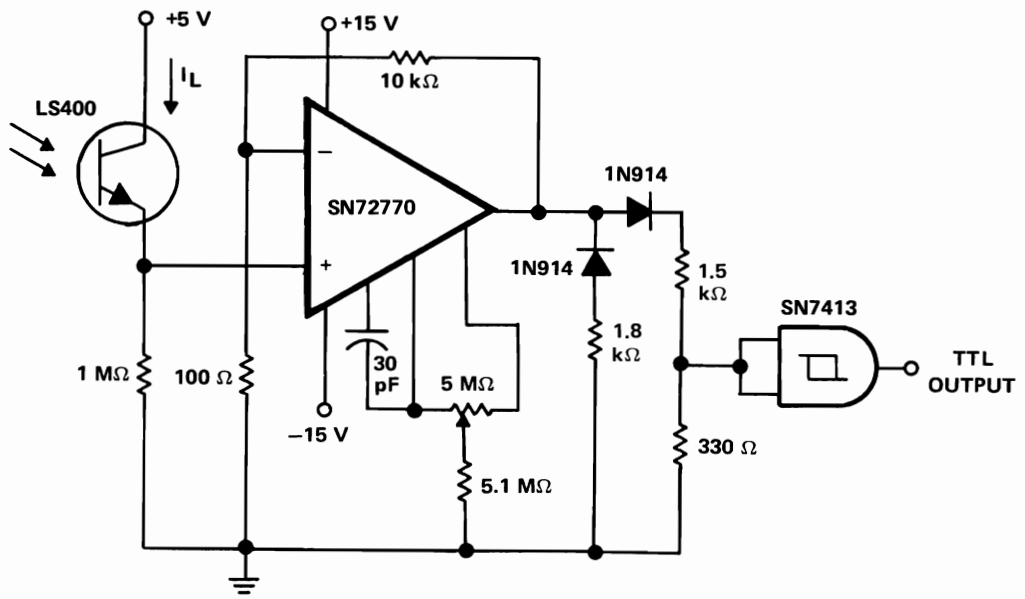
Figure 2.61. Multiple-Input, Logic-Controlled Amplifier

compared to signal-source and feedback resistances. For example, if 2N3824s having a R_{DS} on of $\leqslant 250\ \Omega$ are used, input currents will be limited primarily by the 10-kΩ source resistances. The SN75180 dual-channel TTL-to-MOS converter is used to interface from standard TTL control logic to the negative-level gate voltages required to switch the 2N3824 off. Resulting output signals or voltages will be the product of R2 (the feedback resistor) and the sum of all input currents from the on sources; namely, V_O = R2 (V1/R1 + V2/R2 + V3/R3 + . . . Vn/Rn). In this circuit, isolation between inputs is greater than 60 dB at 1 kHz. With input signals of 1 volt rms at 1 kHz, the signal distortion at the output is less than 2%.

2.6.14 Optical Sensor to TTL Interface

In low-light-level optoelectronic applications small signals from the detectors must be amplified. For example, in Figure 2.62 the on current from the LS400 is assumed to be 250 nA. It is necessary then to use an operational amplifier with very low input bias currents and high input resistance to successfully detect the on condition.

The SN72770 meets these requirements and provides a gain of 100. The 250-nA signal results in a +250-mV level at the non-inverting input of the SN72770. With a gain of 100 the output is in positive saturation. This output level is fed through a loading network to provide the basic TTL level. Due to the slow speed at which an optical circuit may operate, it might be desirable to follow the network with an SN7413 Schmitt trigger device to shape the TTL signal.



CONDITION	TIL400 CURRENT	OUTPUT LOGIC
LIGHT ON	⩾ 250 nA	0
LIGHT OFF	< 25 nA	1

Figure 2.62. Opto Sensor to TTL Interface

2.7 DIFFERENTIAL AMPLIFICATION

The basic differential amplifier (Figure 2.63) can be considered to be comprised of an inverting and a non-inverting amplifier. In the discussion of single-ended amplifiers it was noted that the basic gain equation for an inverting amplifier was $V_o = -(R2/R1)\ V_i$ where V_i was the input voltage to the circuit. For the circuit of Figure 2.63 this expression is

$$V_{o2} = -\frac{R2}{R1}\ V_{i2}$$

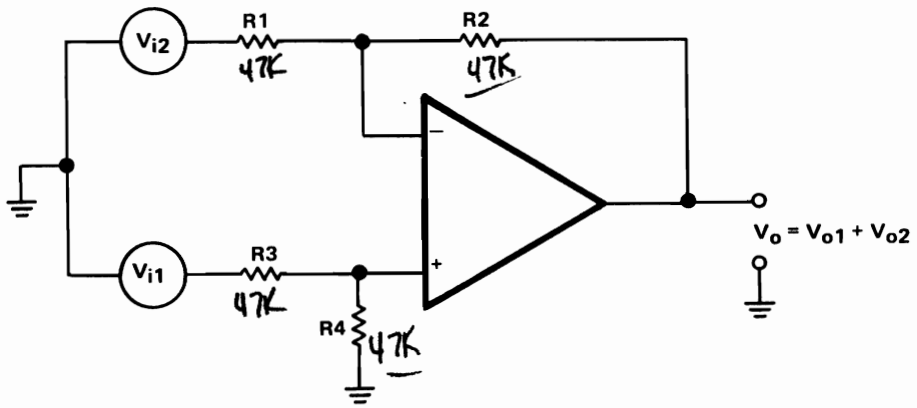


Figure 2.63. Basic Differential Amplifier

As also stated earlier, for the non-inverting amplifier the output voltage is a function of the voltage at the non-inverting input terminal of the device. In Figure 2.63 this input voltage is

$$\left(\frac{R4}{R3 + R4}\right) V_{i1}$$

The corresponding output voltage is

$$V_{o1} = \left(\frac{R1 + R2}{R1}\right)\left(\frac{R4}{R3 + R4}\right) V_{i1}$$

The total output voltage is simply

$$V_o = V_{o1} + V_{o2}$$

$$= \left(\frac{R1 + R2}{R1}\right)\left(\frac{R4}{R3 + R4}\right) V_{i1} - \frac{R2}{R1} V_{i2}$$

Usually R1 = R3 and R2 = R4 and this expression becomes

$$V_o = \left(\frac{R1 + R2}{R1}\right)\left(\frac{R2}{R1 + R2}\right) V_{i1} - \frac{R2}{R1} V_{i2}$$

$$= \frac{R2}{R1}\left(V_{i1} - V_{i2}\right)$$

In this balanced configuration only the input voltage difference appears in the gain equation; therefore normal common-mode input voltages have no effect on the output.

2.8 DIFFERENTIAL-AMPLIFIER APPLICATIONS

2.8.1 High-Input-Impedance Differential Amplifier

In the basic differential-amplifier circuit (Figure 2.63) input impedance is dependent on R1, R2, R3, and R4. High differential input impedance can be achieved by using the circuit of Figure 2.64, in which each input of amplifier A3 is

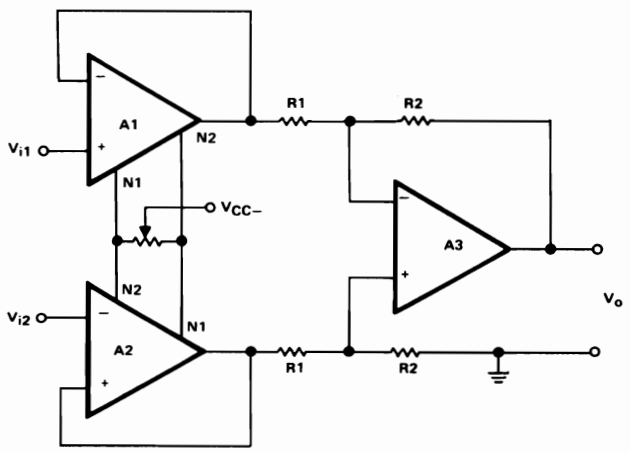


Figure 2.64. High-Input-Impedance Differential Amplifier

driven by a voltage follower (A1 and A2). If the input amplifiers A1 and A2 are SN72771 or SN72310 types, the input impedance at V_{i1} and V_{i2} will be very high (>100 megohms). The offset voltage is adjusted by a potentiometer common to the N1 and N2 terminals of both input amplifiers. Any common-mode output voltage is handled by the inputs of A3.

Improved performance can be achieved by allowing the input amplifiers to have some gain as shown in Figure 2.65. The input amplifiers have some differential gain, whereas any common-mode input voltages will experience only unity gain. These voltages will not appear as differential signals at the A3 input because they are effectively canceled when they appear at equal levels on both ends of R4. The difference between the two input signals, V_d, appears across R4 and is amplified by the factor (1 + 2R3/R4). The overall gain results in an output voltage V_o which may be expressed as

$$V_o = V_d \left(1 + \frac{2R3}{R4}\right)\left(\frac{R2}{R1}\right)$$

Substituting the resistor values given in Figure 2.65, the voltage gain is

$$A_V = \left[1 + \frac{2\,(45\ \text{k}\Omega)}{10\ \text{k}\Omega}\right] \frac{100\ \text{k}\Omega}{10\ \text{k}\Omega}$$

$$= 100, \text{ or } 40\ \text{dB}$$

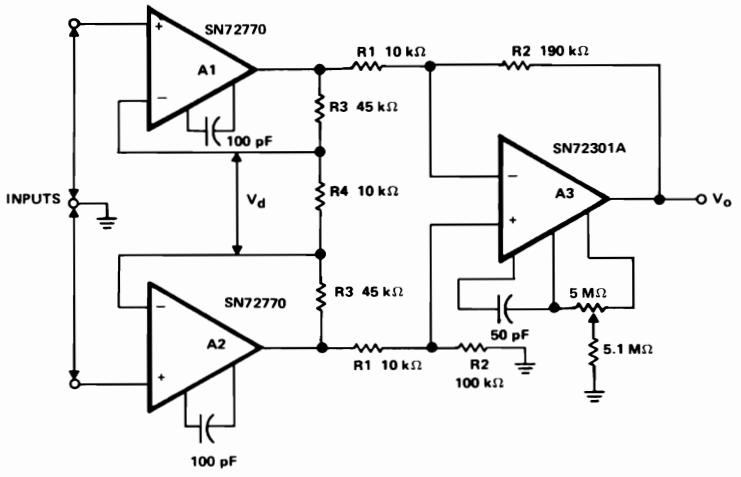


Figure 2.65. High-Input-Impedance Differential Amplifier with Improved Common-Mode Rejection

2.8.2 Bridge-Balance Detection

If a voltage is applied to a basic bridge circuit as in Figure 2.66a and R1/R2 = R3/R4, V_A will equal V_B. Any imbalance in the resistor ratios will result in a voltage difference between V_A and V_B. With the bridge resistors incorporated in a basic amplifier circuit as shown in Figure 2.66b, the voltage difference will be amplified, providing ease of measurement of the bridge condition. One of the resistors may be selected as the variable, and its value could be dependent on an external influence (pressure, temperature, radiation, etc.). In the circuit shown in Figure 2.66 the resulting output voltage would be:

$$V_o = V_i \left[\frac{R4}{R3 + R4} \left(1 + \frac{R2}{R1} \right) - \frac{R2}{R1} \right]$$

$$= V_i \left[\frac{R4 + R4 \dfrac{R2}{R1} - R3 \dfrac{R2}{R1} - R4 \dfrac{R2}{R1}}{R3 + R4} \right]$$

$$V_o = V_i \left[\frac{R4 - R3 \dfrac{R2}{R1}}{R3 + R4} \right]$$

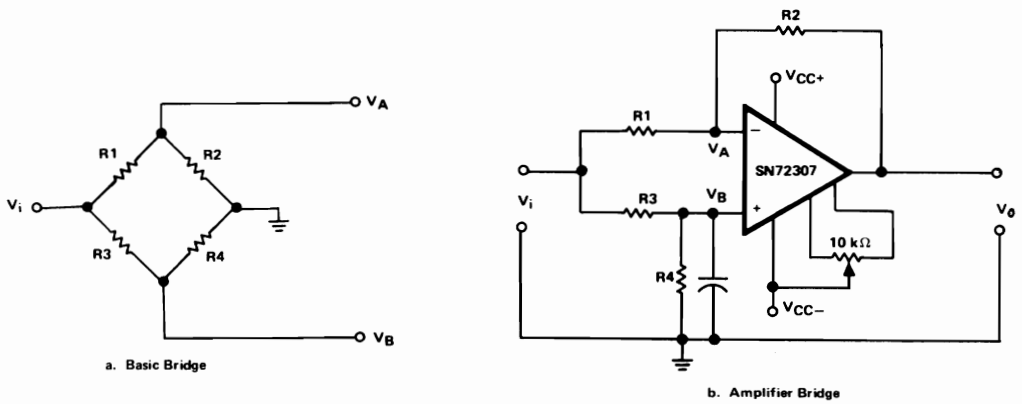


Figure 2.66. Differential-Amplifier Bridge Detector

When R4/R3 = R2/R1 the term in the numerator becomes zero, and therefore $V_o = 0$.

As an example of a practical application assume that R4 is the resistance in a strain gauge which has a value of 1.0 megohm when not under stress. R2 is fixed at 1.0 megohm, and R1 = R3 = 10 k ohms. When stress is applied to the sensor (R4) its resistance increases to 1.4 megohms. In the initial condition R1 = R3 and R2 = R4, permitting simplification of the equation to:

$$V_o = V_i\left(\frac{R4 - R2}{R3 + R4}\right)$$

If V_i is 10 volts, and the resistor values stated above are used, the output voltage is

$$V_o = V_i\left(\frac{1.4\ M\Omega - 1.0\ M\Omega}{10\ k\Omega + 1.4\ M\Omega}\right) = 10\ V\left(\frac{0.4\ M\Omega}{1.41\ M\Omega}\right)$$

$$V_o = 2.84 \text{ volts}$$

2.8.3 Amplifier with High Common-Mode Input Capability

In some instrumentation applications it is necessary to detect and amplify small variations in high-level voltages that exceed the normal common-mode input levels of operational amplifiers. The circuit in Figure 2.67 provides common-mode-input handling capability of ±100 volts. To minimize common-mode amplification effects it is important that the ratio R4/R1 be exactly equal to R5/R2. Precise resistor values and accurate adjustment of R4 establish an exact common-mode-level balance for optimum rejection. Circuit gain is determined by the ratio R3/R5. The SN72301A is selected for this application, allowing the use of feedforward compensation for extended frequency capability.

2.9 MISCELLANEOUS OPERATIONAL-AMPLIFIER APPLICATIONS

2.9.1 Reference Voltage Regulators

Basic Voltage Source — The basic voltage-follower configuration constitutes an accurate voltage source. In Figure 2.68 the operational amplifier provides a stable load to the zener diode and voltage divider network, while the load at V_o may vary. In addition the zener diode establishes a relatively stable input voltage to the

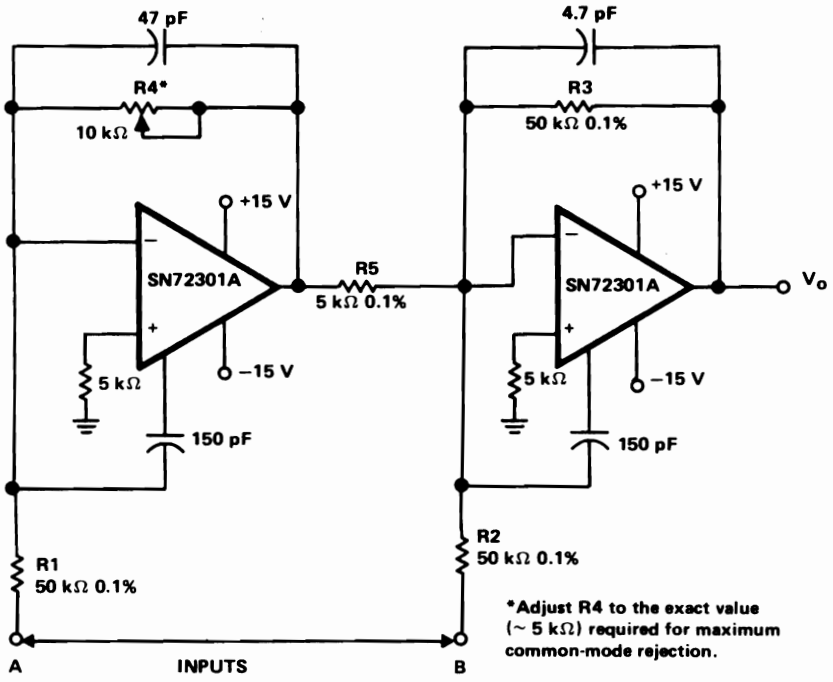


Figure 2.67. Differential-Amplifier with ±100-V Input-Common-Mode Range

amplifier even though V_{CC+} may fluctuate. The overall result is a voltage source that is relatively independent of load-current or supply-voltage variations. This circuit allows V_O to be any value between V_Z and zero, the actual value of the

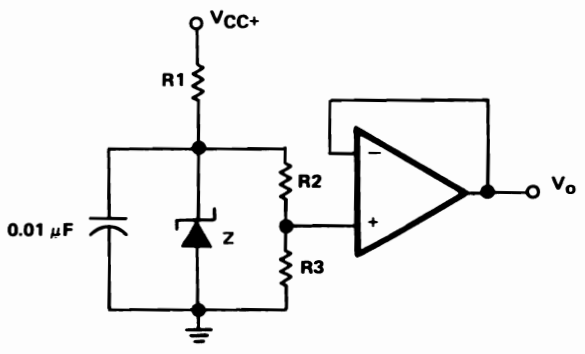


Figure 2.68. Stable Voltage Source ($V_O \leq V_Z$)

output voltage being determined by the relationship of R2 and R3 as follows: $V_O = V_Z$ R3/(R2 + R3). The voltage reference may be either positive or negative for a resultant positive or negative output-voltage source.

Source for Voltages Higher than V_{REF} – For voltage levels greater than V_Z the amplifier may be allowed to have some gain as shown in Figure 2.69. In addition this particular circuit exhibits considerable stability over temperature because of the characteristics of the mercury cell being used as a voltage reference of 1.35 volts. The output voltage of this circuit has ±0.2% stability over the 0°C to 70°C temperature range.

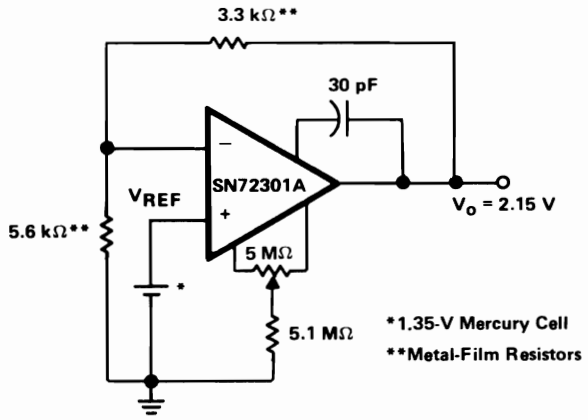


Figure 2.69. Stable Voltage Source ($V_O > V_{REF}$)

Reference-Inverting Voltage Source – The voltage source in Figure 2.70 supplies an output voltage that is opposite in polarity to the reference or zener value. A good feature of this circuit is that the output voltage may be adjusted (with R2) to provide voltages which are less than or greater than the reference voltage, V_Z. In this example $V_O = -V_Z$ (R2/R1).

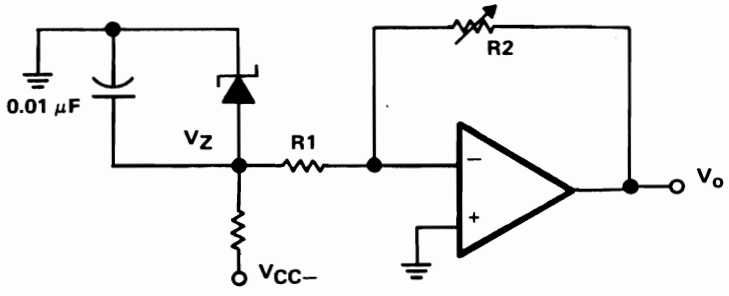


Figure 2.70. Reference-Inverting Voltage Source

Dual Tracking Voltage Regulator — In an extension of these principles, operational amplifiers may be used to compare a reference voltage with a supply output voltage, and to provide an error signal to the series pass transistor for maintaining a stable output voltage under varying load conditions. Such a system, using an SN72747, is seen in the dual tracking supply shown in Figure 2.71a. In this application, voltage from a resistor divider network (R1, R2, and R3) across the positive output is compared, in A1, with a stable 6.2-volt reference. Any difference voltage results in a correcting signal, which is fed to the 2N2219 pass transistor for adjusting the output voltage.

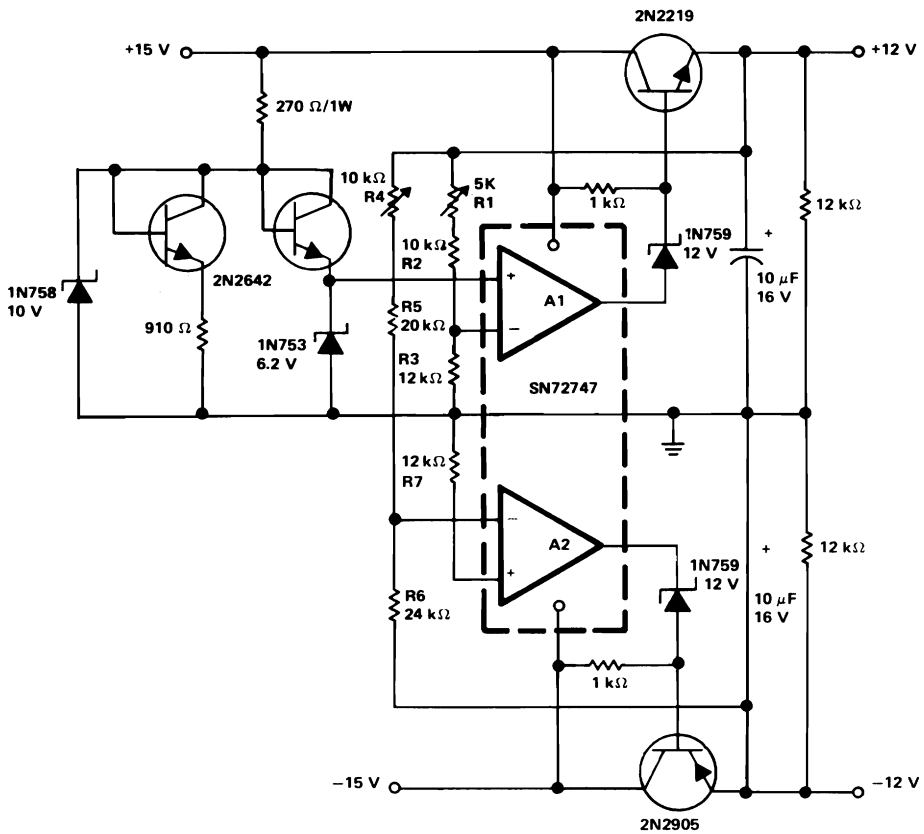


Figure 2.71a.Dual Tracking Regulator: Schematic

Resistors R4, R5, and R6 provide a balanced network between the positive output and the negative output. Its detected level, fed to amplifier A2 of the SN72747, is set to be zero when both outputs are equal. A ground reference is obtained by connecting the other A2 input to ground through R7. Any difference voltage, due to the negative output level being different from the positive output, will result in an error signal being sent to the 2N2905 pass transistor. Figure 2.71b shows the resulting output voltage levels versus load current. This circuit will provide regulation to within ±1% for load current from zero to 300 mA at each output.

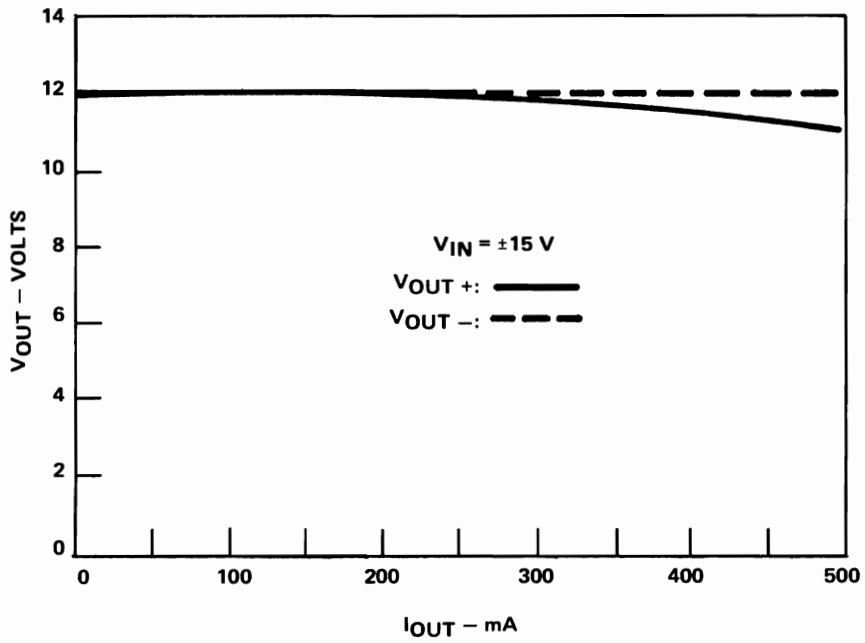


Figure 2.71b.Dual Tracking Regulator: Output Characteristics

V/2 Reference Supply – Another use of the operational amplifier as a voltage source is to provide a V/2 reference for dual-supply amplifiers when only a single power supply is available. Figure 2.72 shows an SN72301A furnishing the V/2 reference required. Input terminations for the dual-supply operational amplifier may then be connected to the V/2 source, allowing the full signal swing capability of the amplifier to be utilized. For typical operational amplifiers the single supply voltage may be 10 volts to 36 volts.

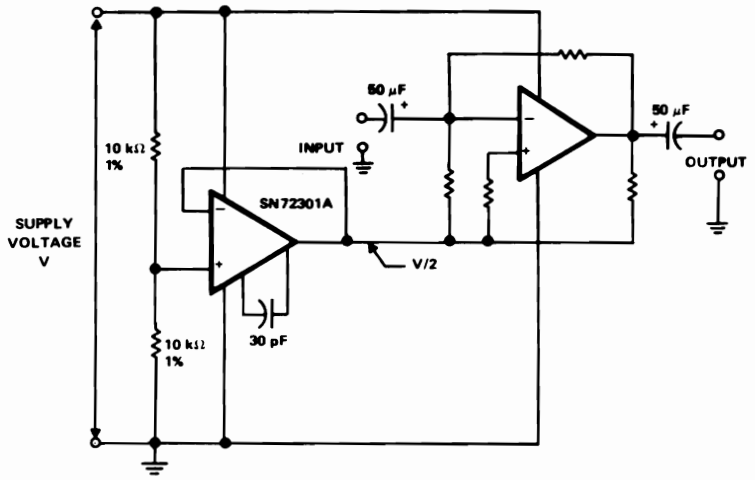


Figure 2.72. Operating an AC Coupled Operational Amplifier from a Single Supply Voltage

TTL-Controlled Positive or Negative Voltage Source — As indicated in Figure 2.73, logic selection of either a positive or a negative voltage source is possible. One of the SN72558 amplifiers furnishes the positive reference level, and

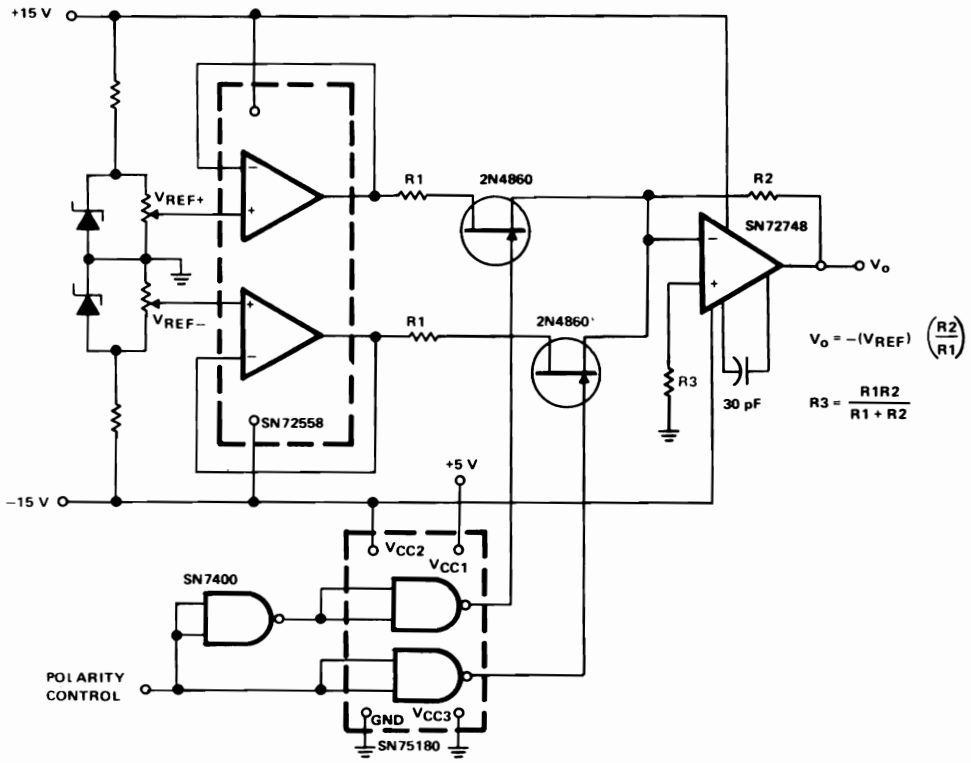


Figure 2.73. Calibrated Positive or Negative Voltage Source with TTL Input Control

the other the negative level. FET switches, controlled by TTL logic through an SN75180, select the desired reference polarity. The output amplifier provides the gain necessary to yield the desired output voltage level. The output V_O is equal to $-V_{REF}$ (R2/R1). For increased current capability a complementary (NPN-PNP) transistorized output circuit could be added.

2.9.2 Constant-Current Sources

Basic Current Source – The simplest voltage-to-current converters are obtained by connecting the load (R_L) in the feedback loop of an operational amplifier. Figures 2.74a and 2.74b show the use of inverting and non-inverting amplifier configurations. In both examples the loop current is determined by V_i/R. As the value of R_L changes, the output voltage V_O will change, maintaining a constant current through R_L.

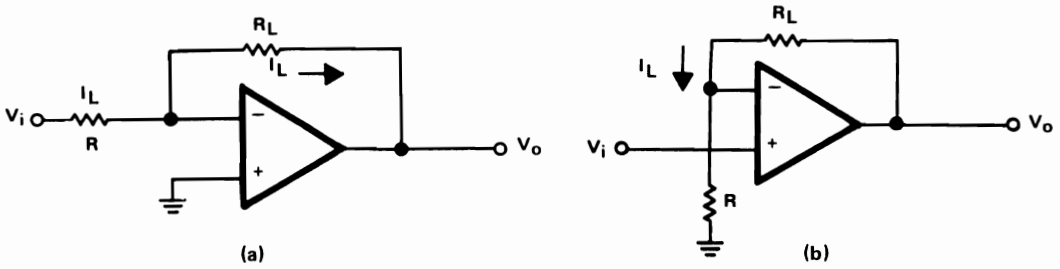


Figure 2.74. Simple Voltage-to-Current Converters

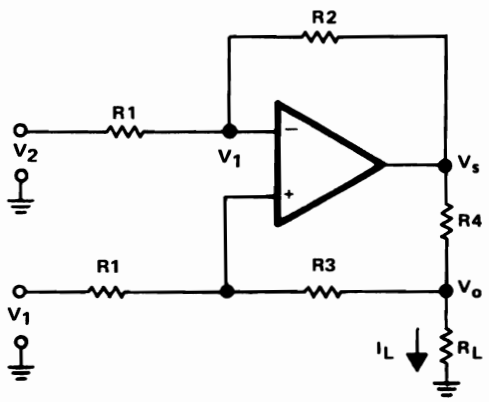


Figure 2.75a. Constant-Current Generators: General Circuit

Current Source with Differential Voltage Input – If the load is to be connected to ground, the circuit of Figure 2.75a may be used. The voltage V_s at the operational-amplifier output consists of V_{s1}, the component due to the non-inverting gain, and V_{s2}, due to the inverting gain.

$$V_s = V_{s1} + V_{s2}$$

where

$$V_{s1} = V_1'\left(\frac{R1 + R2}{R1}\right) \text{ and } V_{s2} = -V_2\left(\frac{R2}{R1}\right)$$

$$V_1' = V_1 - \frac{(V_i - V_o)\,R1}{R1 + R3} = \frac{V_1 R3 + V_o R1}{R1 + R3}$$

$$V_{s1} = \frac{V_i R3 + V_o R1}{R1 + R3}\left(\frac{R1 + R2}{R1}\right)$$

Therefore:

$$V_s = \frac{V_1 R3 + V_o R1}{R1 + R3}\left(\frac{R1 + R2}{R1}\right) - V_2\left(\frac{R2}{R1}\right)$$

V_s may also be expressed as

$$V_s = V_{R4} + V_o$$

where

$$V_{R4} = R4\,(I_{(R1 + R3)} + I_L) \text{ and } I_{(R1 + R3)} = \frac{V_o - V_1}{R1 + R3}$$

Therefore:

$$V_s = R4\left(\frac{V_o - V_1}{R1 + R3} + I_L\right) + V_o$$

From these equations, if R2 = R3 + R4 it can be shown that

$$I_L = \frac{R2}{R1R4}\,(V_1 - V_2)$$

Further simplification occurs if R3 = 0 and R2 = R4 (see Figure 2.75b). Substituting R2 for R4 in the equation for I_L, the load current becomes

$$I_L = \frac{V_1 - V_2}{R1}$$

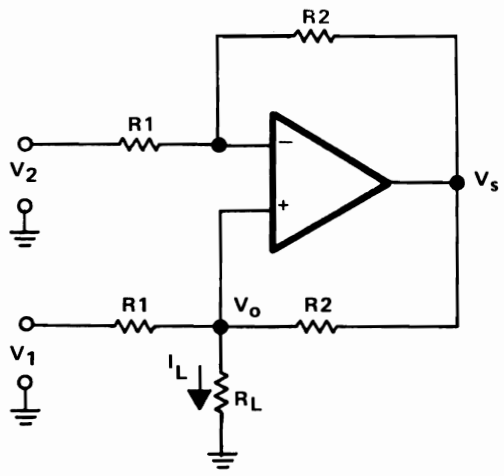


Figure 2.75b. Constant Current Generators: Simplified Circuit

High-Current Generator — Improved output current handling capability may be achieved by adding an FET or bipolar transistor to the output of the operational amplifier. As an example: The circuit in Figure 2.76 uses a Darlington transistor pair to achieve a high-level current source with only limited drive current required of the operational amplifier. The SN72741 will furnish the base drive required to maintain V_r at a desired level across r. V_r is the product of V_i and the circuit loop gain, and $V_r = V_i(R2/R1)$. The load current $I_L = V_r/r$, and therefore $I_l = V_i(R2/R1)(1/r)$.

A 200-ohm resistor is used in series with the operational-amplifier output to damp capacitive loading effects of the transistor inputs and prevent oscillations. Depending on the transistors used, this circuit could furnish constant-current levels of 1 amp or more.

2.9.3 Non-Sinusoidal Signal Generators

Basic Multivibrator — A basic multivibrator may easily be constructed with an operational amplifier and a few external components, as shown in Figure 2.77. When this circuit is turned on, the natural offset of the device serves as an automatic

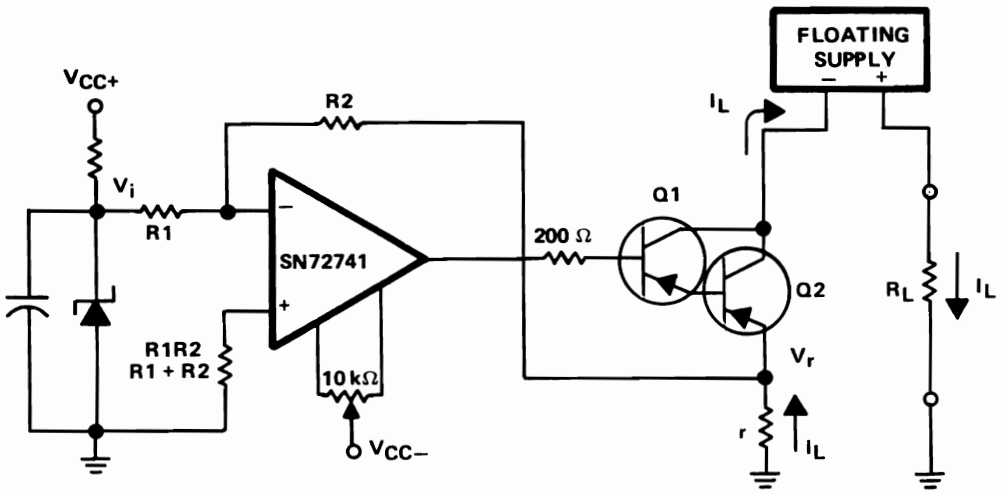


Figure 2.76. High-Level Current Source

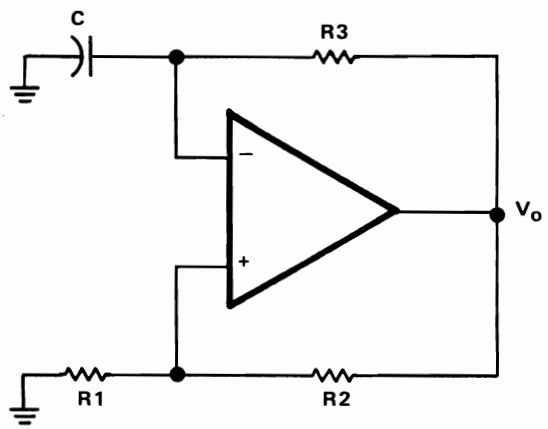


Figure 2.77. Basic Multivibrator

starting voltage. The output voltage V_O goes positive or negative, and the positive feedback through R2 and R1 forces the output to saturate. The high-voltage level at V_O then charges C through R3 until the inverting input voltage exceeds that of the non-inverting input. As the inverting input exceeds the non-inverting input level the output switches to the opposite polarity, and the capacitor is then discharged and recharged until it once again reaches the level at the non-inverting input, continuing the oscillation.

If the positive and negative output levels are at the same amplitude, oscillations of 50% duty cycle result. The total time period of one cycle will be $t_T = 2(R3)C \ln(1 + 2R1/R2)$.

Multivibrator with Variable Duty Cycle – If it is necessary to vary the duty cycle a slightly modified circuit, as seen in Figure 2.78, may be used. In this circuit the diodes provide separate charge and discharge paths. The resistive component of the two paths is controlled by R_C. Using this method the sum of the two RC time constants remains the same while the individual time constants are varied. R3 is one side of the potentiometer R_C; R4 is the other side. The total time period $t_T = (R3 + R4)(C) \ln(1 + 2R1/R2)$. Also, $t_T = t_1 + t_2$ where

$$t_1 = R3(C) \ln\left(1 + 2\,\frac{R1}{R2}\right)$$

$$t_2 = R4(C) \ln\left(1 + 2\,\frac{R1}{R2}\right)$$

Voltage-Controlled Multivibrator – The three-stage multivibrator with voltage-controlled frequency, shown in Figure 2.79, includes three operational amplifiers. The first stage, A1, is a differential amplifier similar to that described earlier in Figure 2.63. The input voltages V_{i1} and V_{i2} are replaced by one input V_{in}. R4 is replaced by the 2N4859 FET. If the FET is off, the value of R4 is effectively infinite and

$$\begin{aligned} V_{oA1} &= V_{in}\left(\frac{R1 + R2}{R1}\right) - V_{in}\left(\frac{R2}{R1}\right) \\ &= V_{in}\left(1 + \frac{R2}{R1} - \frac{R2}{R1}\right) \\ &= V_{in} \end{aligned}$$

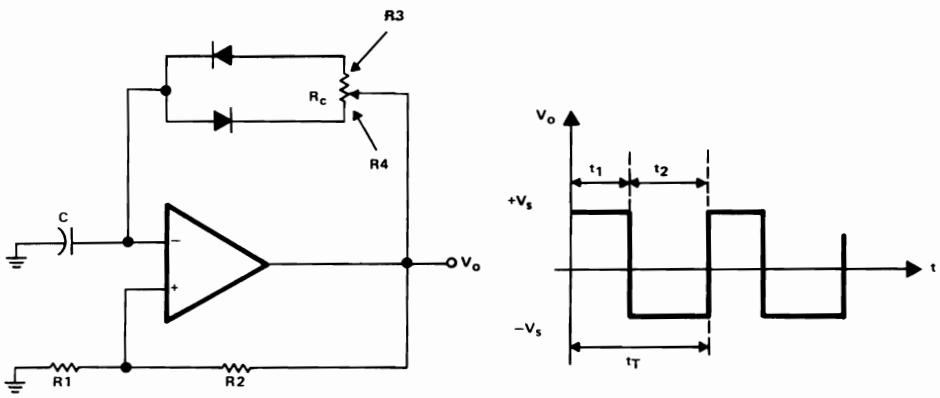


Figure 2.78. Multivibrator with Variable Duty Cycle

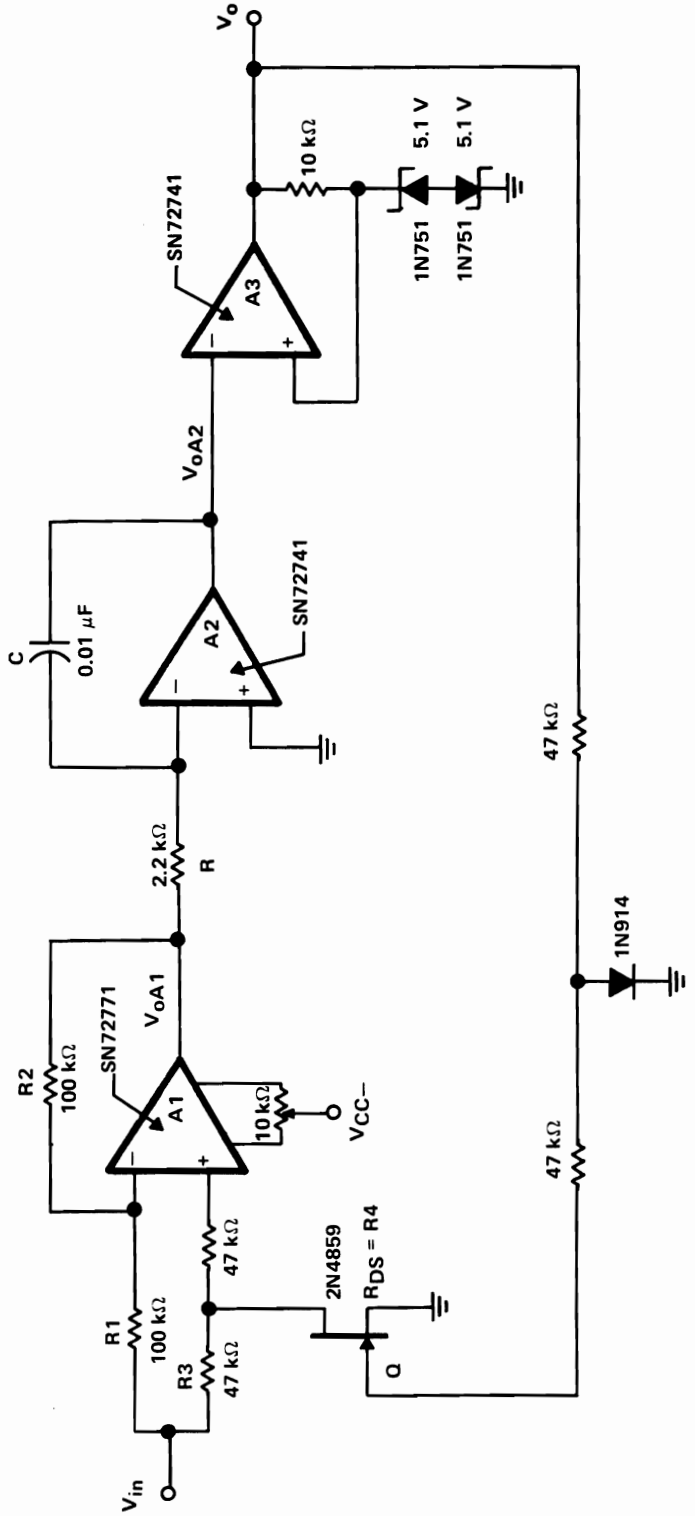


Figure 2.79. Multivibrator with Voltage-Controlled Frequency

If the FET is conducting, R4 is effectively zero ohms and

$$V_{oA1} = -V_{in}\left(\frac{R2}{R1}\right)$$

Therefore V_{oA1} will be either $+V_{in}$ or $-V_{in}$ in this application.

A2 is connected as a dual-slope generator, and its output V_{oA2} is a dual-slope signal that is compared at the input of A3 with a reference of $\pm(V_Z + V_D)$. The FET is conducting when the output V_o is positive, and off when V_o is negative. Thus the A1 output is alternately negative and positive, producing the slope change. The resulting frequency is proportional to the applied voltage as follows:

$$f = \frac{V_{in}}{4RC\,(V_Z + V_D)}$$

where V_{in} is the input control voltage, R is the A2 source impedance (2.2 k ohms in this example), C is the dual-slope detector feedback capacitor (0.01 μF in this example), and $V_Z + V_D$ are the zener voltage and forward voltage of the 1N751s. With these values the equation reduces to $f = V_{in}(0.5 \times 10^{-3})$, or 2 kHz/volt. With the operational amplifiers shown, a linear response may be obtained over an input range of 6 mV to 10 volts and with frequency of operation from 12 Hz to 20 kHz.

2.9.4 Sine-Wave Signal Generators

Wien-Bridge Oscillator — The basic Wien-bridge oscillator (Figure 2.80) is desirable for many oscillator applications because of the ability to set the operating level, with R4, to maintain operation in the linear region of the amplifier and provide low-distortion output signals. R2 and Q1 determine the inverting-input termination resistance. When the circuit is first turned on, C2 will clamp the FET gate to ground and Q1 will be on. The value of R2 is selected to assure that the oscillator will start at this point. After starting, the output would switch from one saturated level to the other except for feedback to the gate of Q1. The output signal is rectified by D1, and a filtered negative dc voltage is developed on the gate of Q1, biasing it in the off direction. This increases the inverting-input termination resistance, lowering the amplifier gain until equilibrium occurs. Proper adjustment of R4 will provide a sine-wave output with a frequency of

$$f = \frac{1}{2\pi RC}$$

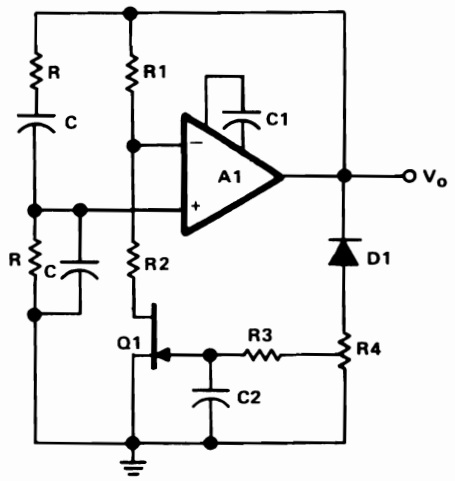


Figure 2.80. Wien-Bridge Oscillator

Sine-Cosine Generator – The oscillator in Figure 2.81, a sine-cosine generator, consists of two active filters in a closed-loop configuration having phase shift of 180° and loop gain of unity at the resonant frequency. Two zener diodes are used to limit output amplitudes, preventing amplifier saturation and signal distortion. The frequency of oscillation is

$$f = \frac{0.68}{2\pi RC}$$

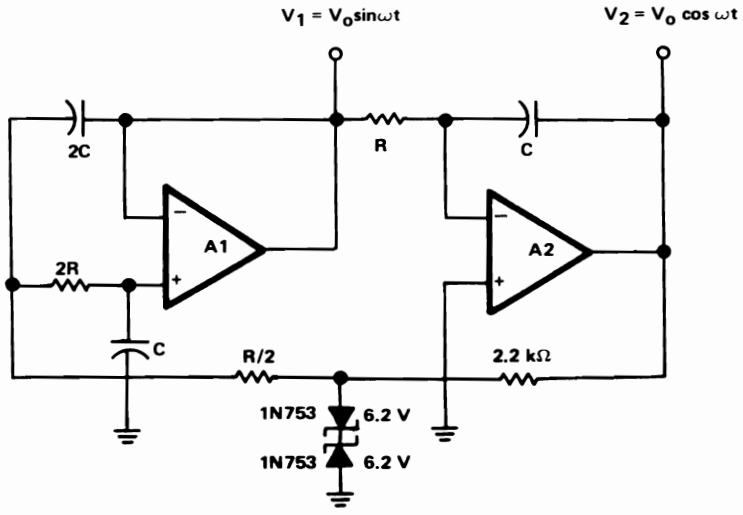


Figure 2.81. Sine-Cosine Generator (Quadrature Oscillator)

The outputs V_1 and V_2 from A1 and A2 are in quadrature with each other. If V_1 is expressed as $V_1 = V_o \sin \omega t$, then V_2, being 90° out of phase, is expressed as $V_2 = V_o \cos \omega t$.

Three-Phase Signal Generator — Using the same basic principle as the sine-cosine generator, a three-phase generator (Figure 2.82) employs three stages with individual phase shifts of 120° for three-phase generation. The first two stages, A1 and A2, are

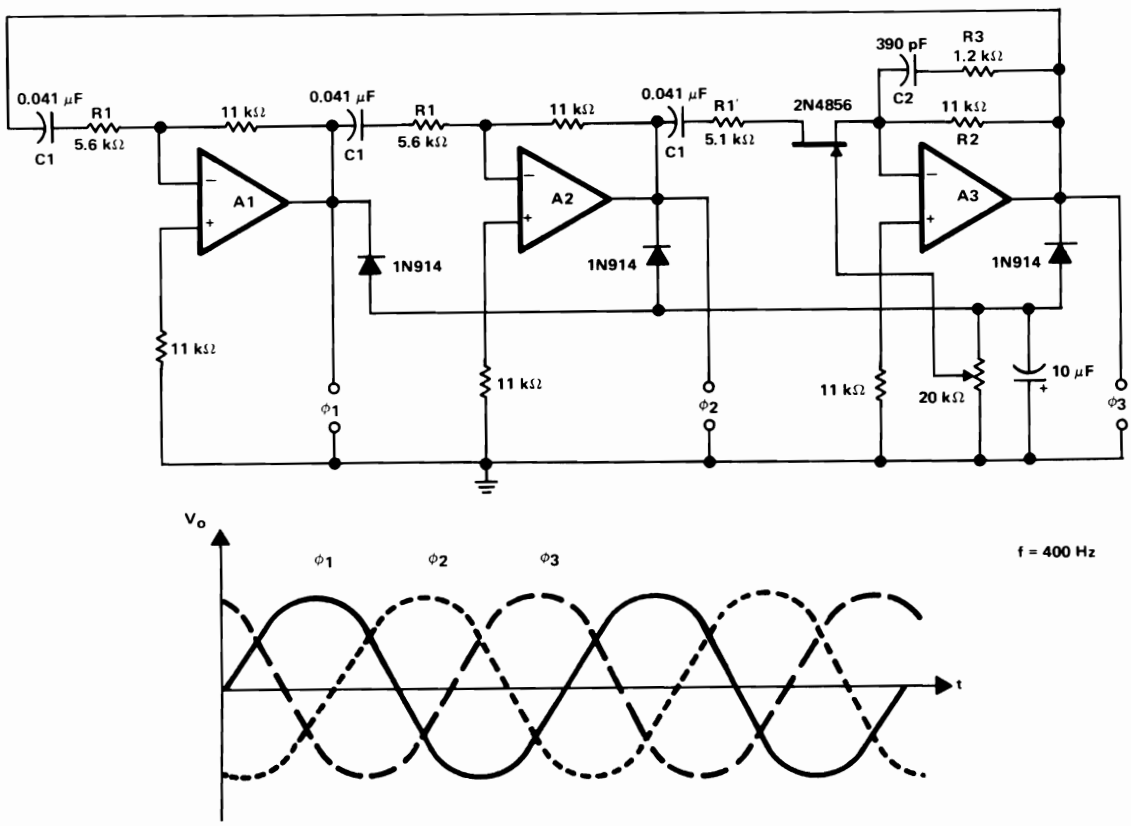


Figure 2.82. Three-Phase Signal Generator

basic active phase-shift networks which must have unity gain at a phase shift of 120°. Therefore the tangent of 120°, which is $\sqrt{3}$, must equal ($X_{C1}/R1$) at the frequency of operation. The unity-gain expression must also be true:

$$\text{Gain} = 1 = \frac{R2}{\sqrt{R1^2 + X_{C1}{}^2}}$$

Since $X_{C1}/R1 = \sqrt{3}$ then $X_{C1} = R1\sqrt{3}$

Solving the unity-gain equation for X_{C1}:

$$X_{C1} = \sqrt{R2^2 - R1^2}$$

Equating these terms:

$$\sqrt{R2^2 - R1^2} = R1\sqrt{3}$$

$$R2^2 - R1^2 = R1^2\,3$$

$$\frac{R2^2}{R1^2} - 1 = 3$$

$$\left(\frac{R2}{R1}\right)^2 = 4$$

Therefore $R2 = 2R1$

Output amplitude is adjusted by a control inserted in the third stage (amplifier A3). A 20 k-ohm potentiometer is used to set the operating level of an FET in the inverting input of this amplifier. The FET on resistance will be very low initially, giving amplifier A3 a gain in excess of unity to ensure that the oscillator starts. As soon as oscillations reach a desired level, AGC feedback from each amplifier, through 1N914 diodes, to the FET gate increases its on resistance until $R1' + R_{on} = R1$ and operational balance is achieved. Some high-frequency roll-off, preventing undesired oscillations and noise, is obtained by the use of C2 and R3.

The frequency of each stage (the system's operating frequency) is expressed as

$$f = \frac{1}{2\pi\sqrt{3}\ R1C1}$$

2.9.5 Operational Amplifiers in Signal Processing

Basic Schmitt Triggers – A voltage-follower Schmitt trigger can be realized by using positive feedback around an operational amplifier as shown in Figure 2.83. The feedback bias is to the non-inverting input, maintaining it at a voltage level proportional to the output, which is latched at either the V_{CC+} or V_{CC-} supply level. An input voltage V_{in} may be applied to overcome the feedback and force the output to the opposite polarity. The sum of the absolute values of the input voltages required to switch states is the hysteresis. With $V_{in} = 0$, the voltage at the non-inverting input terminal is $\pm V_{oMax}\ R1/(R1 + R2)$. An input voltage opposite in polarity and slightly greater in magnitude than $V_{oMax}\ R1/(R1 + R2)$ is required to switch states. The hysteresis is therefore $2\ V_{oMax}\ R1/(R1 + R2)$. The hysteresis curve in Figure 2.83 illustrates the transfer characteristics of a typical operational amplifier.

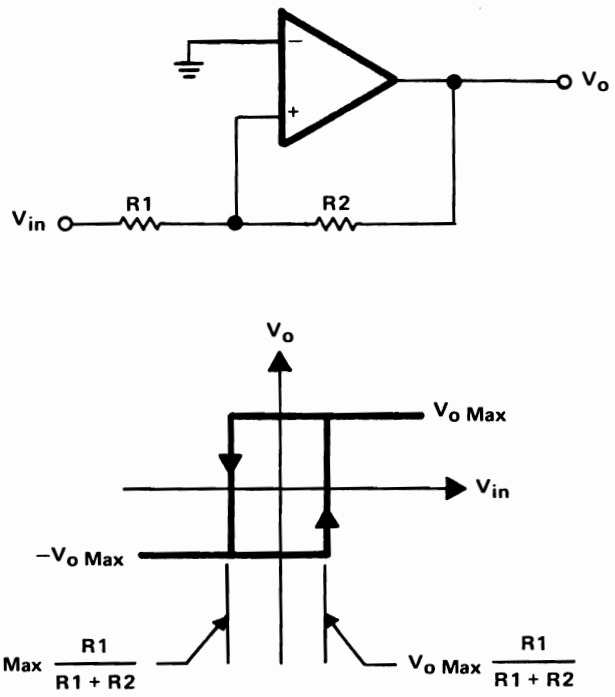


Figure 2.83. Voltage-Follower Schmitt Trigger

The inverting Schmitt trigger in Figure 2.84 has several advantages over the non-inverting example, the primary advantage being that the signal input current is independent of the output and feedback, as it flows only through R3. The input therefore may be from a current or voltage source, as it must generate only enough voltage across R3 to result in switching. The input thresholds are $\pm V_{oMax}$ R2/(R1 + R2). This circuit may be used to convert bipolar data to standard logic data. A positive voltage pulse of sufficient amplitude will switch the output negative, where it will remain until a negative input pulse is applied, which will switch the output back to the positive state. This is similar in operation to an RS type flip-flop. Operational amplifiers respond rather slowly for some switching applications. If additional speed is required, the use of externally compensated amplifiers is recommended. Very low value (1 to 2 pF) frequency-compensation capacitors will enhance switching speeds considerably, allowing data rates as high as 1 MHz. Devices recommended for this application are the SN72709, SN72301, SN72748, and SN72770.

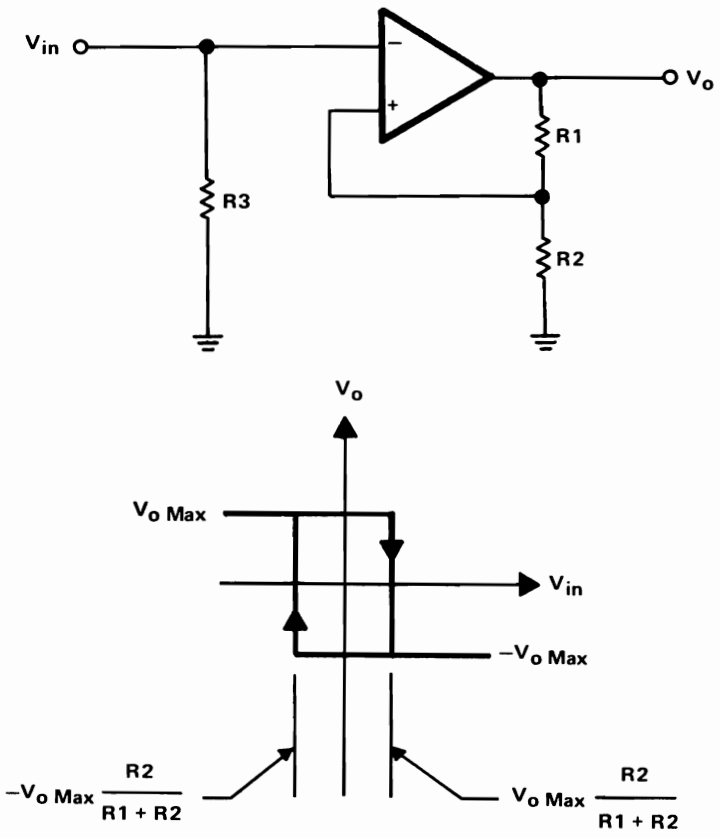


Figure 2.84. Inverting Schmitt Trigger

Schmitt Trigger with Voltage-Controlled Hysteresis – The circuit configuration of Figure 2.85 produces a Schmitt trigger with voltage-controlled hysteresis. Analyzing the negative-going and positive-going transitions separately will help in understanding the circuit operation.

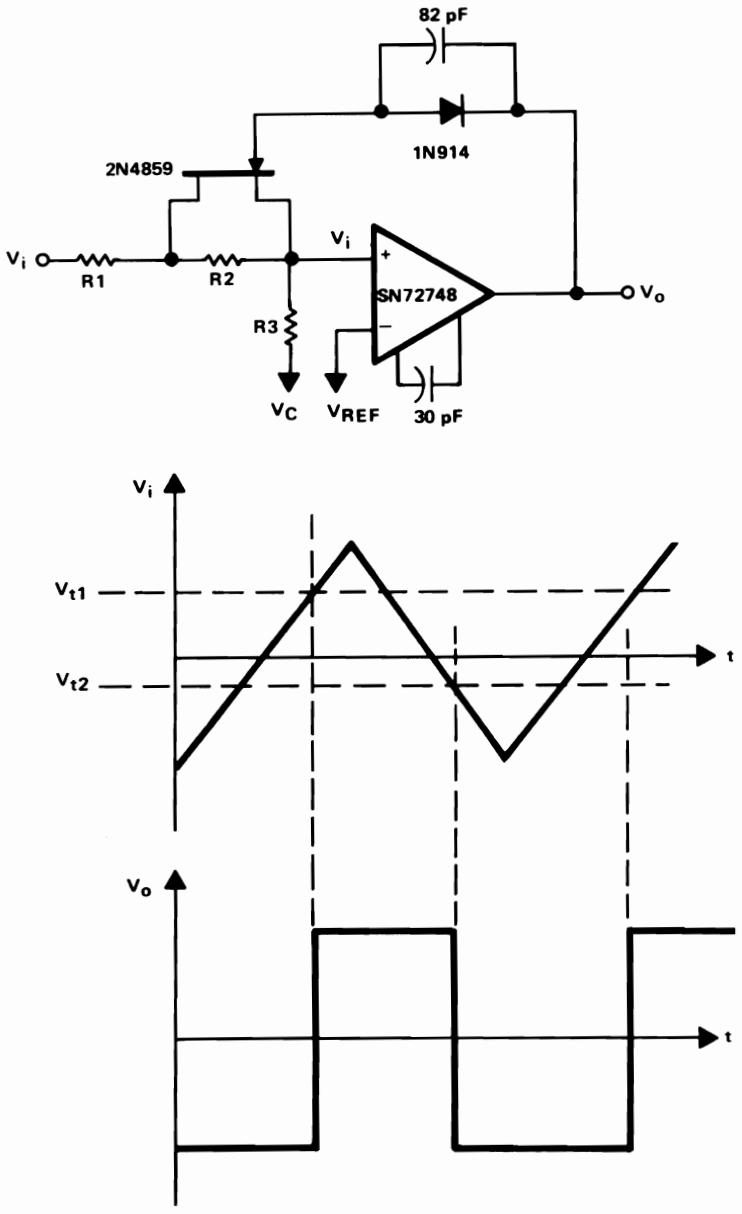


Figure 2.85. Schmitt Trigger with Voltage-Controlled Hysteresis

Beginning with the input V_i sufficiently negative with respect to the reference V_{REF}, the amplifier output will be negative as shown in the voltage waveforms. A negative output voltage will bias the FET off. The input voltage V_i' at the non-inverting input of the operational amplifier is determined by V_i (input voltage), V_C (hysteresis control voltage), and the resistors R1, R2, and R3. V_i' will be $(V_i - V_C)R3/(R1 + R2 + R3)$. The positive-going threshold level V_{t1} is calculated by equating V_i' to V_{REF}, as at the positive threshold point $V_i = V_{t1}$.

Therefore:

$$V_i' = V_{REF} = \frac{(V_{t1} - V_C)\,R3}{R1 + R2 + R3} + V_C$$

$$V_{t1} = \frac{(V_{REF} - V_C)\,(R1 + R2 + R3)}{R3} + V_C$$

$$= \frac{V_{REF}(R1 + R2)}{R3} + V_{REF} - \frac{V_C\,(R1 + R2)}{R3} - V_C + V_C$$

$$= (V_{REF} - V_C)\left(\frac{R1 + R2}{R3}\right) + V_{REF}$$

When the input voltage has exceeded the positive threshold (V_{t1}) the output (V_o) will be positive, and the FET will be on. The on impedance of the FET is very low relative to the resistor values used, and therefore R2 may be considered to be shorted out. Under this condition the threshold voltage becomes V_{t2}, which is calculated as follows:

$$V_i' = V_{REF} = \frac{(V_{t2} - V_C)\,R3}{R1 + R3} + V_C$$

$$V_{t2} = \frac{(V_{REF} - V_C)(R1 + R3)}{R3} + V_C$$

$$= (V_{REF} - V_C)\frac{R1}{R3} + V_{REF}$$

As may be observed from the equations for V_{t1} and V_{t2}, any change in V_C will affect the input threshold levels. The operating levels should be chosen progressively from V_{CC+}, beginning with the minimum values for threshold levels V_{t1} and V_{t2}, followed by V_{REF} and V_C.

AC Millivoltmeter — The millivoltmeter circuit in Figure 2.86 is an operational-amplifier application combining a high-input-impedance preamplifier (A1) and a voltage-to-current converter (A2). Amplifier A1 best serves as a high-input-impedance amplifier if it is a super-beta device; the SN72770 is recommended in this example. The preamplifier gain may be adjusted in steps, using R1 or R2, for various input-sensitivity levels if desired. A2 furnishes the drive for the diode-bridge detector circuit and meter movement. The output current is adjusted by R3 to the desired full-scale meter level.

When the A2 output is low the detector diodes are not forward biased, and A2 is in an open-loop configuration. C7, which is only 10 pF, provides proper compensation for this condition. When the signal increases in amplitude the diodes are forward biased, connecting C6 (180 pF) to provide the compensation required for the closed-loop condition. The circuit has a flat response over a maximum frequency range of ~1 Hz to 1 MHz. If R1 and R2 are selected to provide higher than unity gain, the upper frequency limit will be reduced. For example if G = 100, f_{max} = 10 kHz.

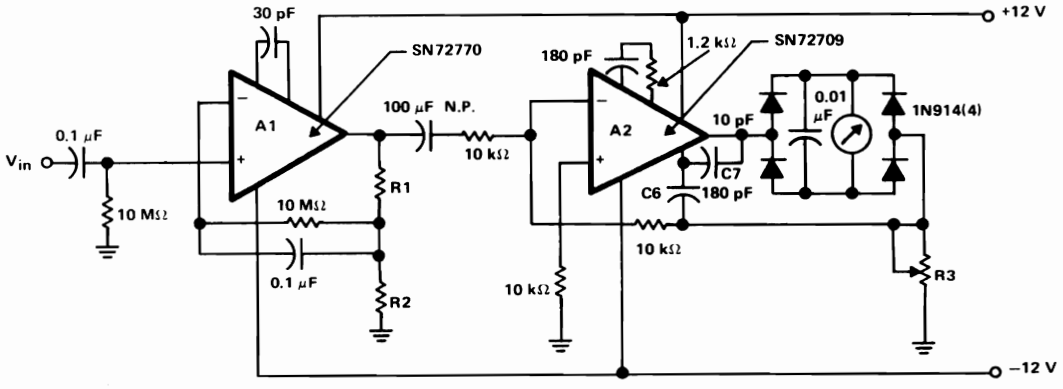


Figure 2.86. AC Millivoltmeter

2.9.6 Peak-Voltage Detection

Basic Peak Detector — The circuit in Figure 2.87 demonstrates the basic technique of peak-voltage detection. The SN72771 amplifier is utilized because of its low input bias current. This avoids premature discharge of capacitor C. The amplifier is wired as a voltage follower with a diode (D2) in its feedback loop. D2 compensates the output level for any loss through D1. Bias for D2 is provided through R1, which is connected to a negative voltage (—V). Positive input voltages (V_{in}) are applied to the capacitor C through D1. When the input voltage decreases from its peak value, D1 becomes reverse biased, leaving the peak value across C and at the amplifier output. The peak value is retained at the output until the capacitor is reset to zero by activating transistor Q. A negative-value peak detector may be implemented by reversing the diodes, changing the diode bias to a positive voltage and replacing the transistor Q with a PNP type.

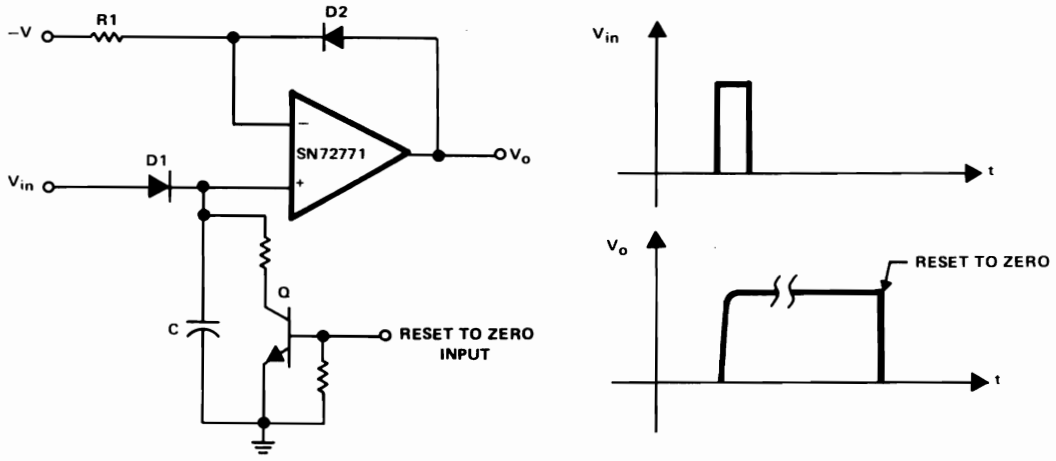


Figure 2.87. Basic Peak Detector

Peak-to-Peak Voltage Detector — Peak-to-peak voltage detection is accomplished by combining positive- and negative-level peak detectors in one circuit as shown in Figure 2.88. A1 accepts and holds positive input peaks while A2 accepts and holds negative input peaks. A3 serves as a summing amplifier for the signal peaks of opposite polarity, yielding a positive output level equal to $|V_{+peak}| + |V_{-peak}|$.

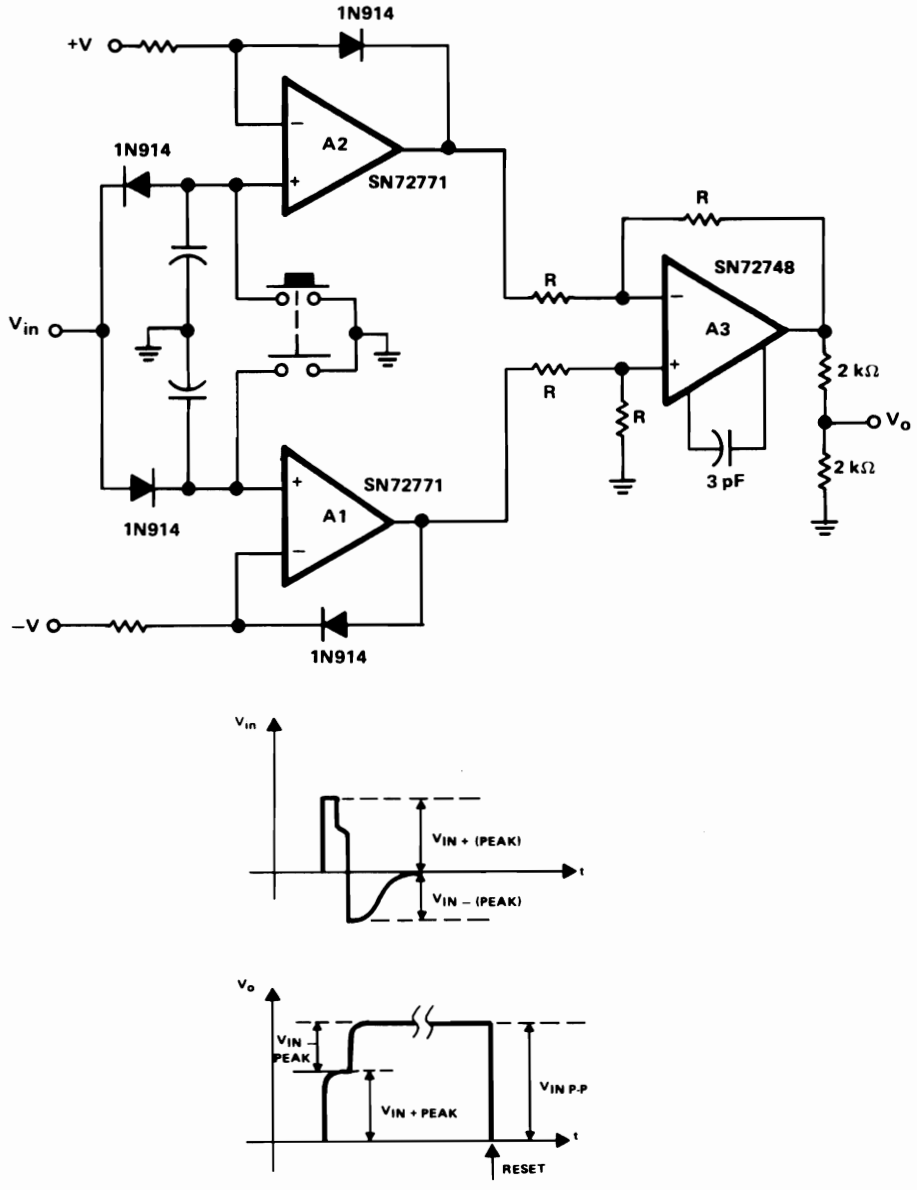


Figure 2.88. Peak-to-Peak Detector

Improved Peak Detector — Another method of holding a peak (or sampled) voltage is seen in Figure 2.89. In this circuit it is possible to use a lower-performance amplifier, with the high-impedance FETs preventing capacitor discharge until desired. The circuit gain is defined by R2/R1. When Q1 is switched off (in the sample mode) a positive input voltage V_{in} will charge C1 to a negative level that will maintain V_o at $-V_{in}$ R2/R1. If V_{in} decreases, V_o will remain at the sampled level, as neither Q1 nor Q2 provides a discharge path for C1. If Q1 is turned on, it will reset the output to zero.

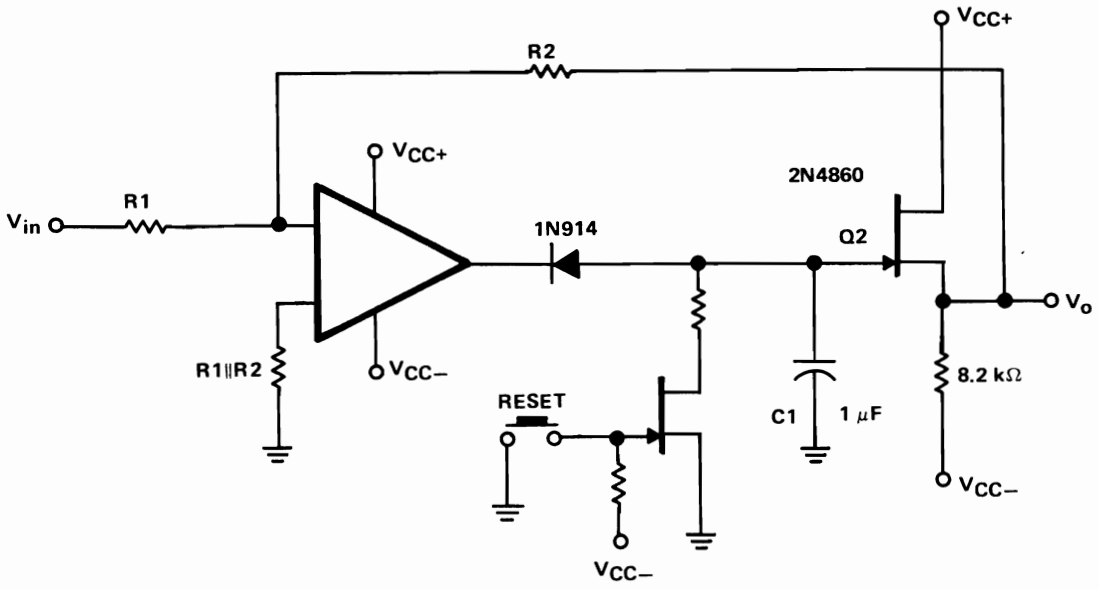


Figure 2.89. Improved Peak Detector

Sample-and-Hold Circuit — The basic sample-and-hold circuit shown in Figure 2.90 provides continuous sampling, with a hold at the moment desired. The amplifier A1 provides a high input impedance for the signal source and sufficient drive to quickly charge C1. A2 serves as a buffer to the output load. Q1 and Q2, controlled by the complementary interface drive shown, provide the two operating modes. The sample mode is obtained by a logic 1 control input (V_C). In this mode Q1 is off, Q2 is on, and C1 is charged to the V_{in} level. V_o will track changes in V_{in} unless a hold signal (logic 0) is applied to the control input. During the hold mode Q1 is on and Q2 is off, with C1 maintaining the level of the sampled voltage at the instant the hold is initiated. The curves in Figure 2.90 show a basic sample (or track) and hold sequence.

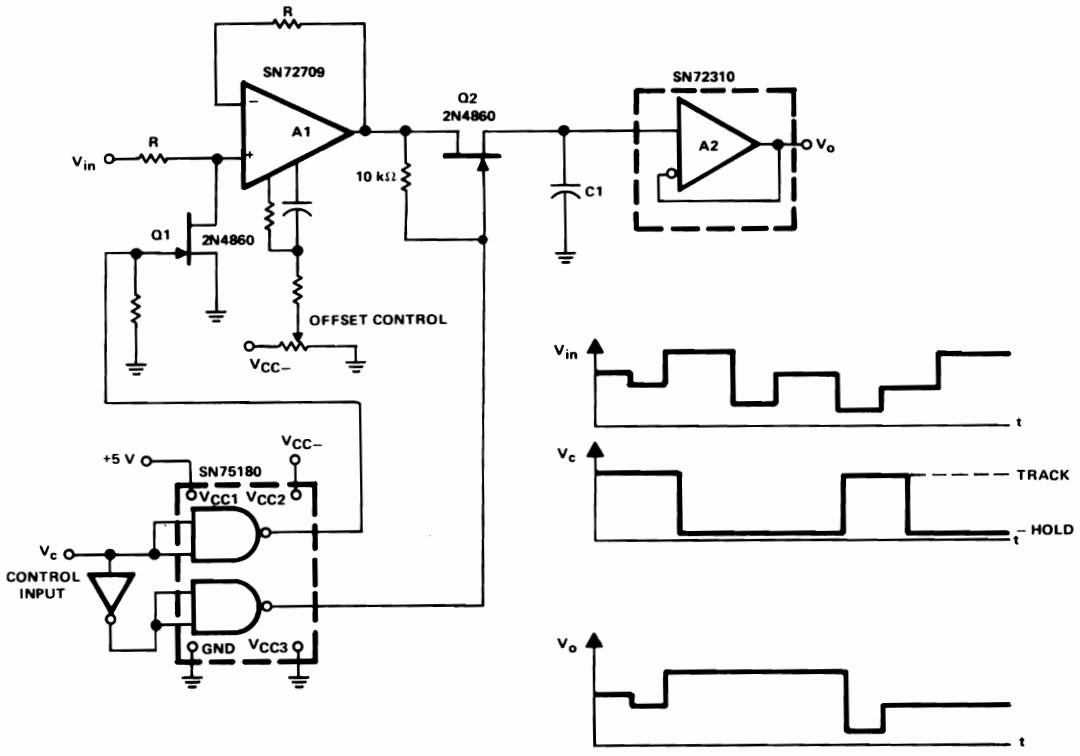


Figure 2.90. Sample (or Track) and Hold Circuit

2.9.7 Miscellaneous Circuits

Latch-Reset Circuit – Figure 2.91 illustrates another use of positive feedback. Positive feedback, through R4, is selected to be sufficient to latch the circuit in a fixed output state. In addition, bias to the inverting input through R1 and R2 ensures a negative steady-state output at turn-on. Arrival of a positive pulse at input V_1 will result in the output switching to a positive level and latching in that state. For the positive output latch condition the V_1 input pulse must have the following level:

$$V_1 \geq V_{CC}\left(\frac{R3}{R3+R4} + \frac{R1}{R1+R2}\right)$$

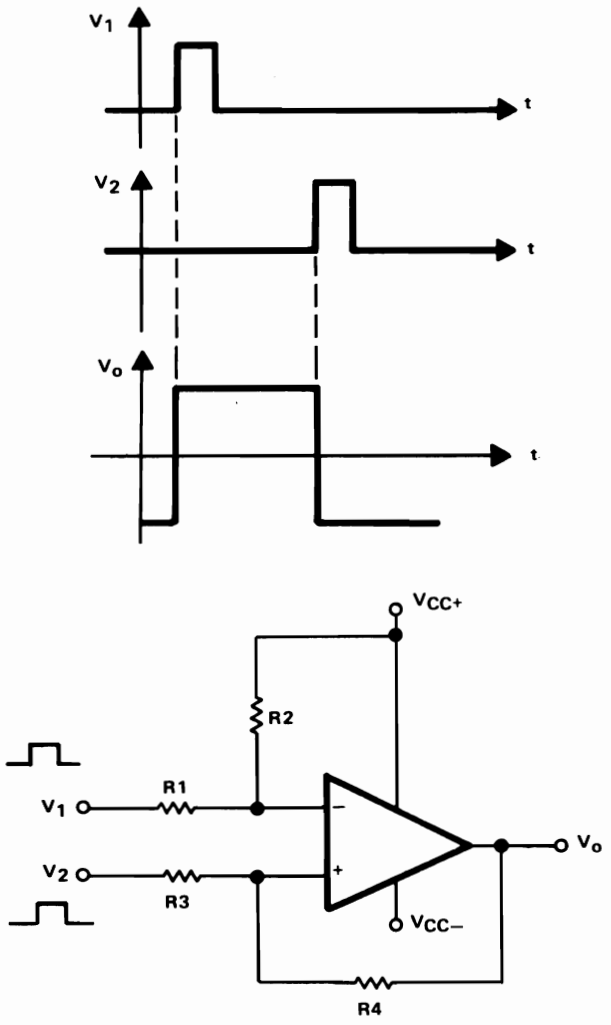


Figure 2.91. Latch-Reset Circuit

For a return to the negative output condition a positive pulse at V_2 is required. The amplitude of this pulse must be:

$$V_2 \geq V_{CC}\left(\frac{R3}{R3 + R4} - \frac{R1}{R1 + R2}\right)$$

The latching characteristic of this circuit makes it highly immune to system noise.

Square Wave to Triangle Wave Converter — Changing square-wave signals to triangular signals may be accomplished with an integrator circuit (Figure 2.92) sometimes called a dual-slope integrator. It is necessary to shunt the feedback capacitor C1 with the network consisting of R2, C2, and R2 to prevent the amplifier from being in the open-loop mode for dc signals. To keep the slope of the output signal linear, R2 and C2 must be so chosen that:

$$R2\,C2 \gg R1\,C1 \geqslant 2t$$

The output voltage level is

$$V_o = -V_{in\ Max}\ \frac{t}{2R1C1}$$

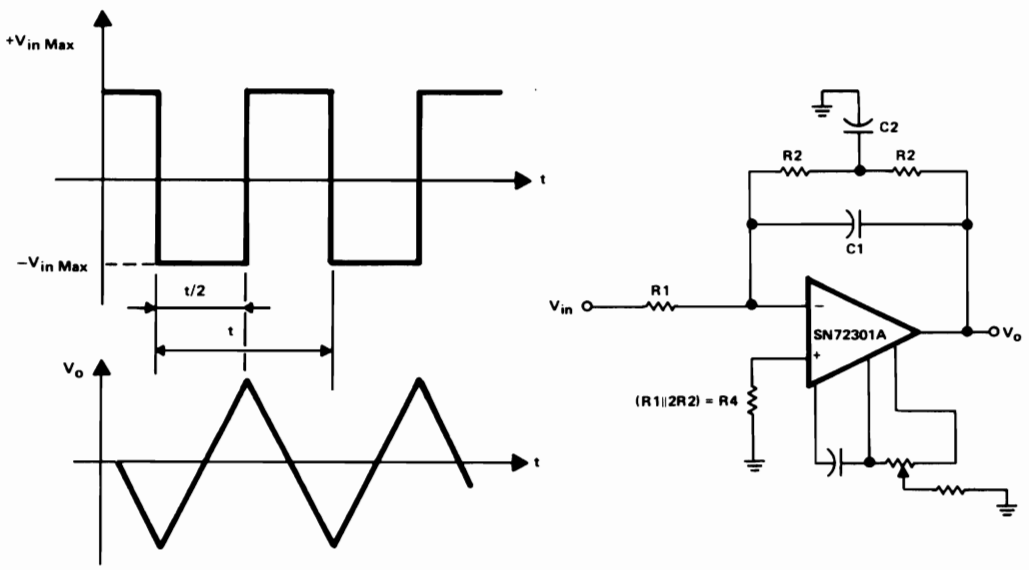


Figure 2.92. Square Wave to Triangle Wave Converter

Triangle Wave to Sine Wave Converter – Another type of signal converter, shown in Figure 2.93, uses a non-linear transfer characteristic to obtain a sine-wave output from a triangular input. To obtain the required transfer function the amplifier gain must decrease as the input voltage increases. A feedback loop consisting of three cells (Figure 2.93), using both NPN and PNP transistors, provides the required gain variations and will handle both positive and negative input signals.

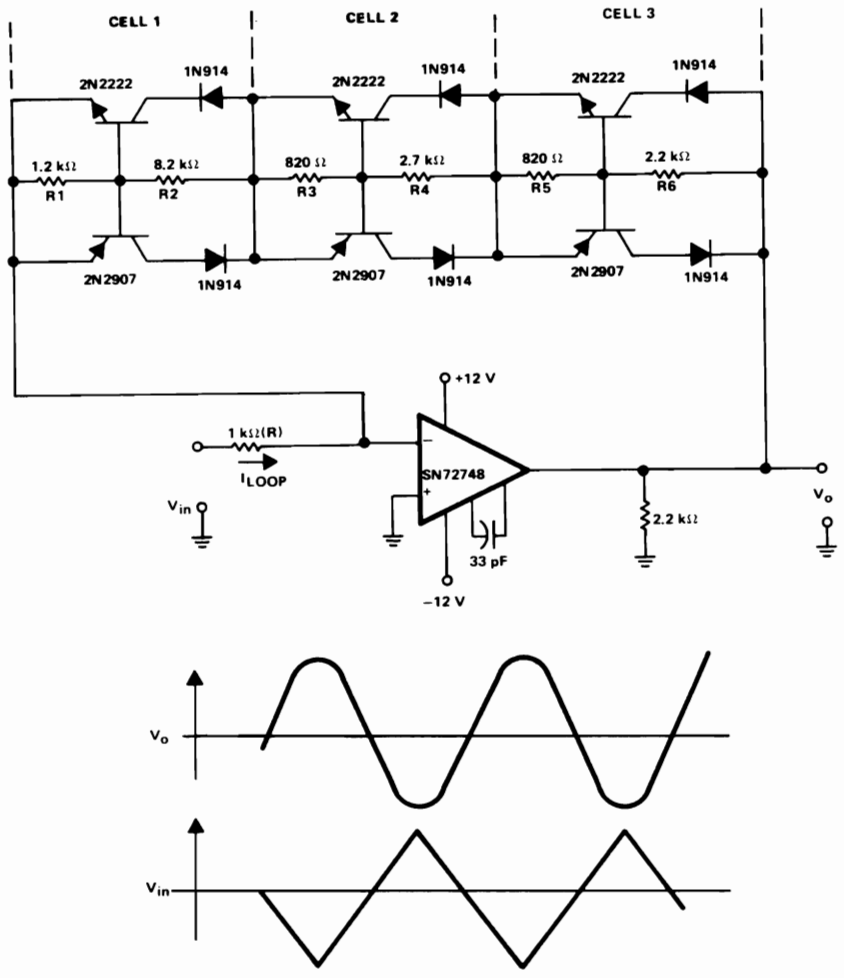


Figure 2.93. Triangle Wave to Sine Wave Converter

When the input voltage is near zero the loop current ($I_{Loop} = V_{in}/R$) will pass through resistors R1 to R6. All transistors in the loop will be off due to the low current level, and therefore the amplifier gain will be determined by (R1 + R2 + R3 + R4 + R5 + R6)/R. As V_{in} increases I_{Loop} increases until the voltage across R1 turns on a transistor in cell 1. Voltage across cell 1 follows the base-emitter junction characteristics, resulting in gain reduction. As the input voltage continues to increase, the same action will occur in cell 2 and then cell 3. The cumulative effect of these loop-gain variations is to smooth the response, yielding a close approximation to a sine wave. In the example shown in Figure 2.93 the input triangular wave was 1.8 volts peak to peak at a frequency of 1 kHz. The output is an 18-volt peak-to-peak sine wave with less than 3% total harmonic distortion. Low-distortion performance is possible from 5 Hz to 5 kHz with this circuit.

Light-Controlled Oscillator — Another circuit which combines several functions is the light-controlled oscillator seen in Figure 2.94a. In this application an LS400 phototransistor is used in the negative feedback loop of a basic multivibrator circuit. Capacitor C will be charged by a current from the LS400 acting as a current generator. Charging (or discharging) current is proportional to the light level applied. A diode bridge (using 1N914 diodes) assures correct flow of charging or discharging currents through the phototransistor. Positive feedback through R2 and R1 provides a Schmitt-trigger type of switching action, and a reference voltage V_{REF} at the non-inverting input which is equal to $(V_{oMax})R1/(R1 + R2)$. The frequency of operation is simply

$$f = \frac{i_{Light}}{4\,C\,V_{REF}}$$

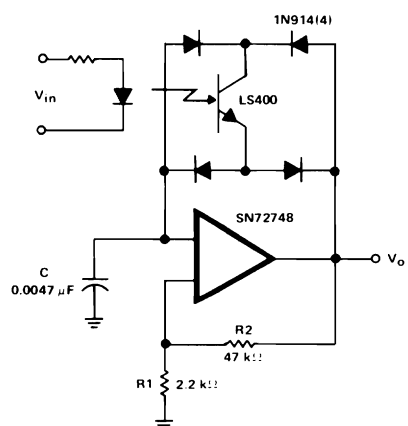


Figure 2.94a.Optically Controlled Multivibrator: Schematic

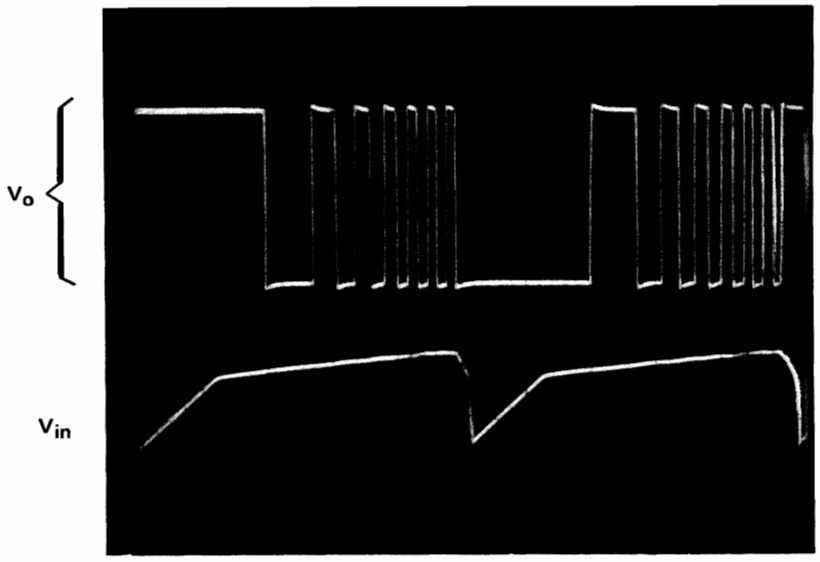


Figure 2.94b.Optically Controlled Multivibrator: Waveforms

In this application light levels from 0.02 mW/cm^2 to 20 mW/cm^2 will cause light currents (I_{Light}) of approximately 0.5 μA to 0.5 mA. Assuming a V_{oMax} of ± 12 volts, V_{REF} will be 0.5 volt. The resulting operating frequencies in this example will then be from 50 Hz to 50 kHz. Waveforms in Figure 2.94b illustrate the effect of a varying light level being applied with a light-emitting diode. Light levels, proportional to the input voltage V_{in}, cause the output V_o to vary over a wide frequency range.

Optically Coupled Audio Amplifier – In Figure 2.95 an optically coupled isolator (OCI-1) is driven by an SN72741 to provide audio modulation of a load that must be isolated. A positive input bias is applied to the inverting input through the bias control P1, for the purpose of biasing the amplifier output level to the linear operating region of the light-emitting diode. Gain is provided by the SN72741 while OCI-1 provides coupling of the audio signal and isolation from a load that may experience very high voltage levels. Isolation of dc voltages of 1000 volts or greater is possible. Frequencies from 50 Hz to 10 kHz may be handled with a relatively flat frequency response.

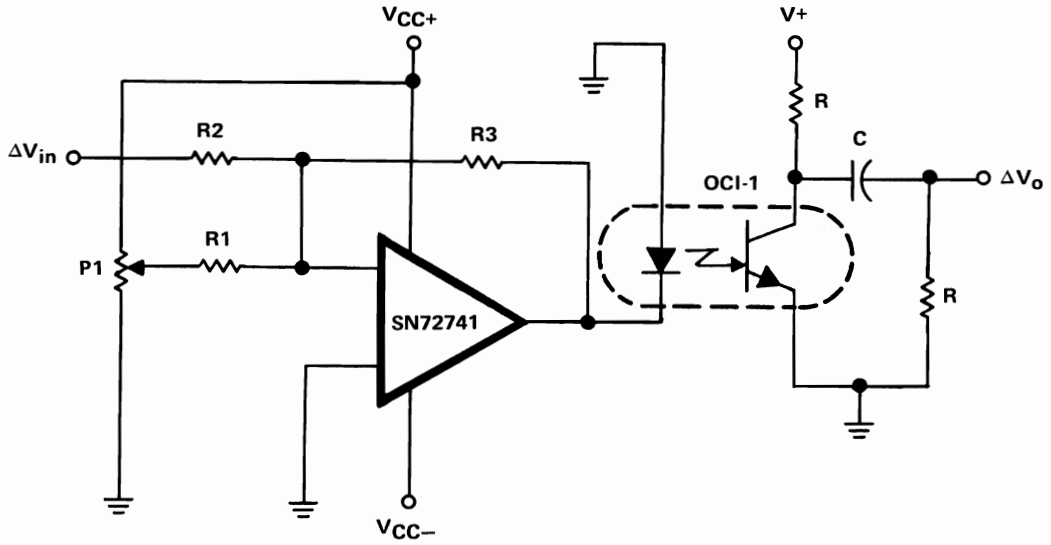


Figure 2.95. Optically Coupled Audio Amplifier

2.10 ACTIVE FILTERS

Filters are often thought of as networks consisting of resistors, capacitors, and inductors (passive components). Because the components are passive, the energy out of a passive filter is always less than the energy applied by the input signal. The attenuation or insertion losses limit the effectiveness of passive filters and make some applications impractical. However, resistors and capacitors can be combined with operational amplifiers to form active filters.

In an active filter the amplifier may add energy to the system, resulting in filtering and some power gain. Other advantages of active filters include low output impedance, cascaded stages without gain loss, and the capability of generating filtering functions having relatively high Q at low frequencies without use of inductors. In low-frequency applications, the required inductors are generally cumbersome, and difficult and costly to build. On the other hand, only a few convenient-to-use components are needed for active filters in these applications.

Depending on the circuit type, low-pass filters as well as high-pass, bandpass, or band-reject filters can be designed with a roll-off characteristic of 6 to 50 dB or greater per octave.

2.10.1 Unity-Gain Active Filters

This type of active filter, the simplest to develop, combines an operational amplifier connected in unity gain with RC filter networks. It can be either a low-pass filter (Figure 2.96a), or a high-pass filter (Figure 2.96b), depending on the resistor and capacitor positions. The −3 dB (cutoff) frequency is

$$f_o = \frac{1}{2\pi C\sqrt{R'R}} \quad \text{(low-frequency cutoff)}$$

$$f_o = \frac{1}{2\pi R\sqrt{C'C}} \quad \text{(high-frequency cutoff)}$$

for the low-pass and high-pass filters respectively. Q of the circuit can be stated as

$$Q = 1/2\sqrt{C'/C} \text{ for the low-pass filter}$$

$$Q = 1/2\sqrt{R'/R} \text{ for the high-pass filter}$$

These simple expressions are valid for Q greater than 10.

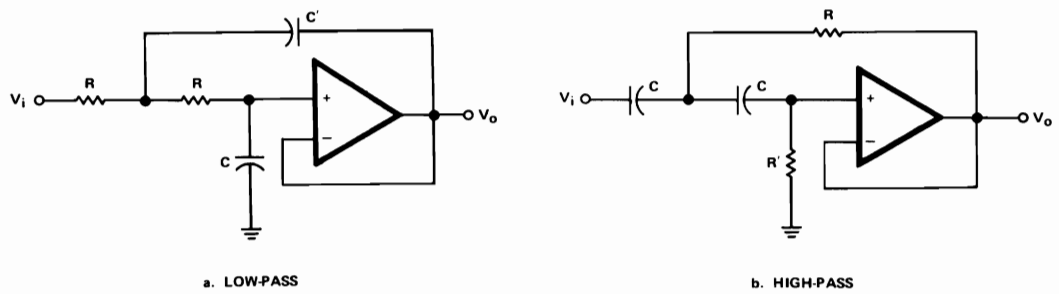


Figure 2.96. Unity-Gain Active Filters

2.10.2 Low-Pass Active Filters

Figure 2.97 shows a typical response curve of a low-pass active filter using a general-purpose operational amplifier. Outside the passband, attenuation is computed at 12 dB per octave. However, at high frequencies the attenuation of the filter is less than predicted. In simple theory the operational amplifier is considered to be perfect, and for a typical general-purpose operational amplifier this "perfection" proves to be acceptable up to 100 kHz. But beyond this frequency the output impedance and other characteristics of the amplifier can no longer be neglected. The combined effect of these factors is the loss of attenuation at high frequencies. As can be deduced from Figure 2.97, general-purpose amplifiers are most effective at audio frequencies. For higher frequency applications a broadband amplifier such as the SN7511 should be used.

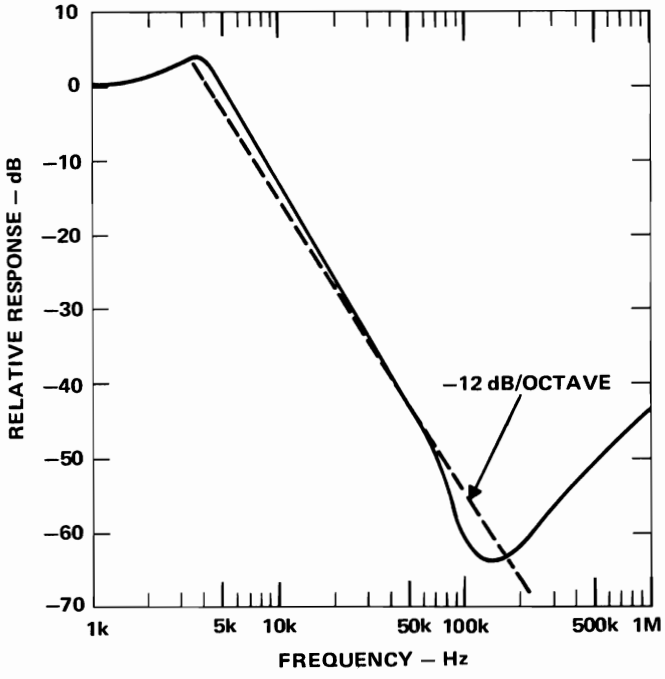


Figure 2.97. Response Curve of a Low-Pass Active Filter

When the frequency spectrum of the input signal is especially wide, the high-frequency rejection characteristic must be considered. This is the case when the filter is supplied by a rectangular signal. Figure 2.98 shows the response of a low-pass active filter to a 1-MHz square-wave signal.

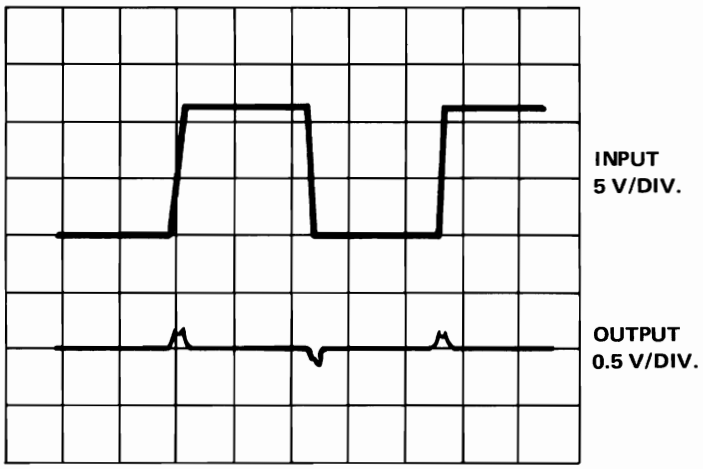


Figure 2.98. Response of a Low-Pass Active Filter to High-Frequency Signals

The high-frequency-cutoff problem is solved by using a simple RC filter, with better high-frequency-attenuation characteristics, ahead of the active filter having superior low-frequency performance. An impedance adapter should be inserted between the two filters as shown in Figure 2.99.

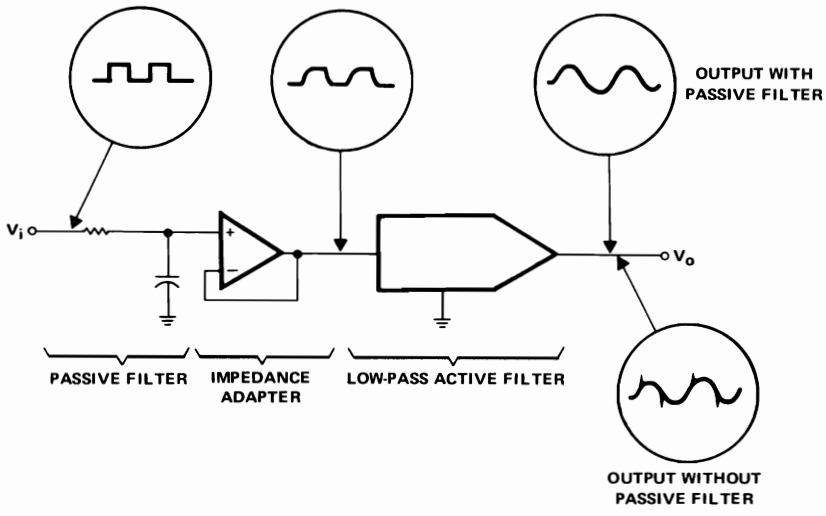


Figure 2.99. Use of a Passive Filter Preceding an Active Filter

2.10.3 Band-Reject Active Filter

In addition to the previously described functions, an active filter may be used to perform a band-reject function. A filter having a band-reject characteristic is frequently referred to as a notch filter. A circuit for this type of active filter, as shown in Figure 2.100, uses an SN72709 in a unity-gain configuration. This is a

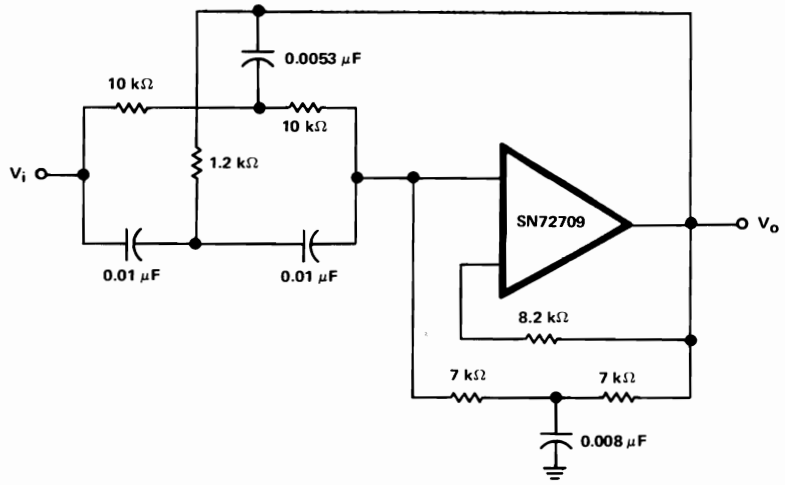


Figure 2.100. Band-Reject Active Filter

second-order band-reject filter with a notch frequency of 3 kHz as seen in Figure 2.101. The resulting Q of this filter is about 23, with a notch depth of 31 dB. Although three passive T networks are used in this application, it is obvious that the operational amplifier has permitted obtaining a sharply tuned low-frequency filter without the use of inductors or large-value capacitors.

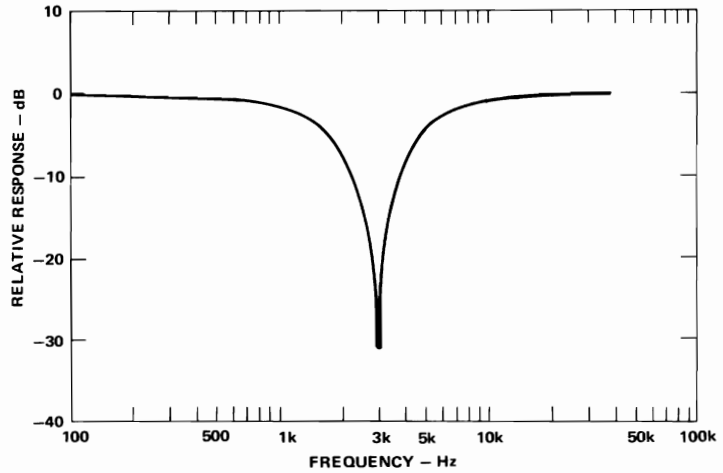


Figure 2.101. Response Curve of Band-Reject Active Filter

3

Comparators

3.1 GENERAL

The basic comparator is like a differential amplifier functioning in the open-loop mode. Because of high circuit gain the output is normally saturated in either the high state or the low state, depending on the polarity of the differential input voltage. In this manner the amplifier, or comparator, provides a logic output indicating the amplitude relationship between two analog signals.

An ideal comparator has the following characteristics:

Differential gain	$\rightarrow \infty$
Common-mode gain	0
Input impedance	$\rightarrow \infty$
Output impedance	$\rightarrow 0$
Bandwidth	$\rightarrow \infty$
Offset voltage and current	0

These characteristics are identical with those of an operational amplifier, and, initially, operational amplifiers were used in the open-loop mode to perform comparator functions. However, the desirability of devices designed specifically for this operation soon became evident. As a result, improvements were made in recovery time, switching time, and the output levels. The comparator is usually followed internally by a TTL logic circuit, thus producing output high and low levels matching the input levels required by one or more TTL loads.

Use of the comparator is basically as shown in the simplified diagram of Figure 3.1. In practice, however, several device parameters must be considered for proper design and application of comparator circuits. These are discussed in the following paragraphs.

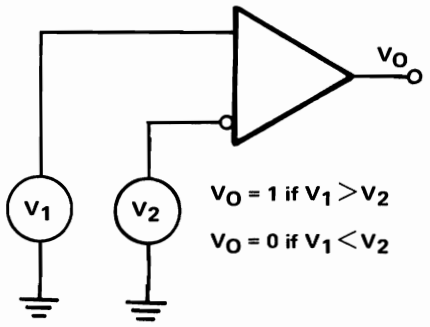


Figure 3.1. Basic Comparator Function

3.2 DEVICE PARAMETERS

3.2.1 Voltage Gain

The voltage gain A_{VD} determines the sensitivity and threshold accuracy of a comparator. For the ideal comparator the gain could be considered infinite, and an extremely small voltage applied between the two inputs would cause a change in the output state. In practice the gain is not infinite, and some minimum voltage variation at the input is required to obtain a change in the output state. The ratio of the variation of output voltage to that of input voltage is the voltage gain of the comparator. From the following relationship, the minimum sensitivity $\Delta V_{I(min)}$ which will cause a change in the output state can be determined.

$$\Delta V_{I(min)} = \frac{\Delta V_O}{A_{VD}}$$

The quantity ΔV_O, the difference between the high and low states of the output, is generally chosen to be 2.5 volts to ensure matching between the comparator and a TTL load.

3.2.2 Input Offset Voltage

The definition of this parameter is identical for a comparator and an operational amplifier. The offset voltage is the voltage that must be applied between the inputs to bring the output voltage to a specified value — a function of the ambient temperature. The guaranteed maximum offset voltage characteristic is verified by

measurements at the following temperatures and output voltage levels.

Ambient Temperature (°C)	Output Voltage (Volts)
−55	1.8
0	1.5
25	1.4
70	1.2
125	1.0

Note: 0, 25, and 70°C apply to the 72 series; −55, 25, and 125°C apply to 52 series devices.

These output levels were selected to match the switching threshold of TTL logic at these temperatures.

Figure 3.2 shows the input and output voltage waveforms for an SN72710 comparator, with the inverting input referenced to ground and the non-inverting input connected to a ramp. When the output voltage reaches the 1.4-volt level, the input voltage is equal to the offset voltage. From Figure 3.2 we can determine that the offset voltage is about −2 mV, the voltage gain is approximately 1150, and the sensitivity $\Delta V_{I(min)}$ is around 2.2 mV.

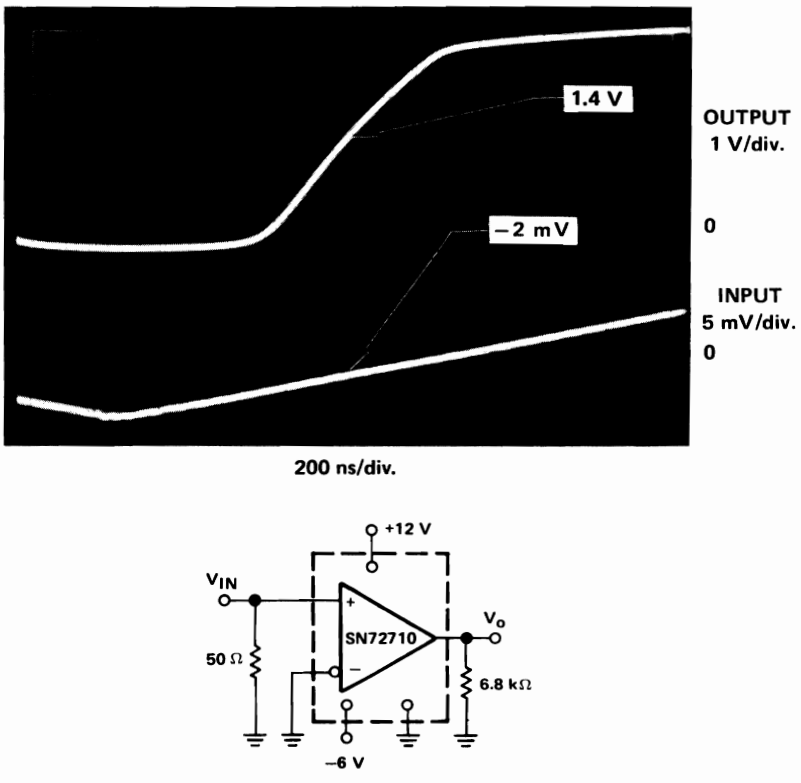


Figure 3.2. Measurement of Offset Voltage and Gain for an SN72710

Other product types, particularly data line receivers, are frequently used as comparators. Specifications for these devices normally do not include offset voltage and sensitivity. However, the manufacturer specifies the minimum switching voltage from one input to ground, with the other input grounded as a reference. This characteristic includes both offset voltage and sensitivity.

3.2.3 Output Characteristics

Although some comparators have a full TTL fan-out capability of 10 or greater, most have a fan-out limited to one TTL load. An evaluation of the output circuits will indicate the basic limiting factors and how maximum performance can be obtained.

In the active pull-down mode (Figure 3.3a) the output low-level sink current (I_{OL}) is limited. The emitter of Q2 is clamped at 1 V_{BE}, or −0.7 volt. With Q3 providing another V_{BE} drop, the resulting I_{OL} may be calculated from:

$$I_{OL} = \frac{V_{CC-} + 2\,V_{BE}}{1.77\ k\Omega} = \frac{-6\ V + 1.4\ V}{1.77\ k\Omega} = -2.6\ mA$$

This value is near the typical value for this device, with the minus sign indicating a sink current. The corresponding V_{OL} level is $V_{E(Q2)} + V_{CE(sat)(Q2)}$, or (−0.7 V + 0.2 V) = −0.5 volt, which is the data-sheet typical value.

In the logic 0 output state the SN72710 can handle only one standard TTL gate with its maximum I_{IL} requirement of −1.6 mA. Increased fan-out capability can be obtained by connecting an external resistor between the comparator output and the negative supply.

In the active pull-up mode the typical high-level output voltage, V_{OH}, is 3.2 volts for the SN72710. The voltage at the base of the pull-up transistor (Q1, Figure 3.3b) is defined by $V_{OH} + V_Z + V_{BE(Q1)}$, where V_Z is 6.2 volts and $V_{BE(Q1)}$ is 0.7 volt. The base voltage is therefore (3.2 + 6.2 + 0.7), 10.1 volts. The resulting base drive is

$$I_b = \frac{V_{CC+} - V_B}{R_b} = \frac{12\ V - 10.1\ V}{3.9\ k\Omega} = 0.488\ mA$$

Assuming a typical saturated h_{FE} of 12, the resulting pull-up drive capability is (0.488 mA)(12), or 5.8 mA. It should be noted that only part of the 5.8-mA drive is available to the external circuit. The remainder of the current will be shunted through the pull-down circuit, since the current sink is not turned off during the logic 1 output condition. For the SN72710, the resulting I_{OH} level available for

external drive will be the difference between the pull-up drive, 5.8 mA, and the pull-down sink, 2.6 mA, or 3.2 mA (Figure 3.3b). The 3.2 mA is quite adequate, as the logic 1 level (I_{OH}) required is only 40 μA per TTL load.

Similar calculations for the SN72711 comparator yield an I_{OL} level of 0.87 mA, and an I_{OH} level of 4.3 mA.

With the SN72710, and particularly the SN72711, increased fan-out capability may be required. For example, a fan-out capability of 2 requires an I_{OL} level of 3.2 mA. With the SN72711 (Figure 3.3c) a 2.7-kΩ resistor is connected from its output to the negative supply. The resulting I_{OL} is 3.2 mA at a 0.4-volt maximum V_{OL}. The resulting effective I_{OH} capability is reduced to 1.19 mA at a minimum V_{OH} of 2.4 volts.

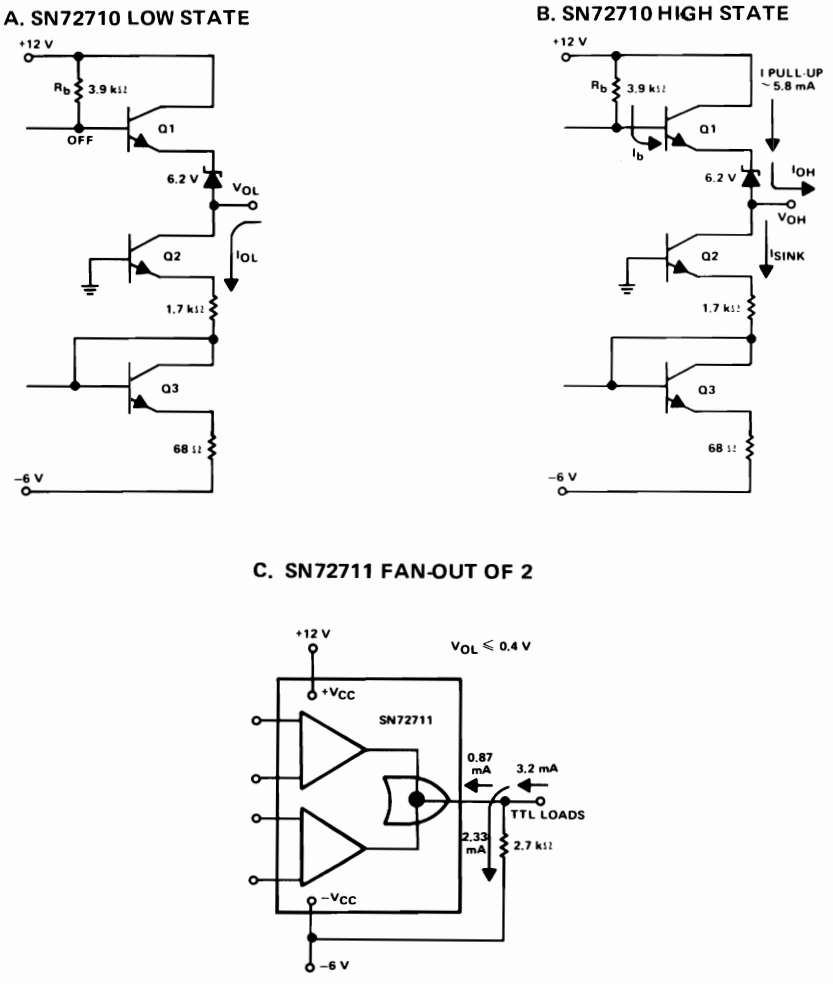


Figure 3.3. Comparator Output Configurations

3.2.4 Response Time

The response time of a comparator is a highly important characteristic to the user. Response time is affected by the amplitude and rate of change of the input signal. Since the influence of the rate of change can be determined from the voltage gain of the comparator, we will consider only the influence of a step function applied to the input. In the test setup one of the inputs is connected to a reference voltage high enough to drive the comparator output well into saturation in the quiescent state. A level of about 100 mV serves this purpose. The other input is driven by a 100-mV step with rise time negligible compared to the propagation time of the comparator. The response time of the comparator is by definition the interval between application of the input step and the time when the output voltage crosses the logic threshold voltage (1.4 volts for TTL at 25°C). The reference voltage is initially so adjusted that the 100-mV step input would drive the comparator output from saturation to the verge of switching to compensate for the offset voltage and eliminate this parameter from the speed measurement. That is, the amplitude of the reference voltage would be set to 100 mV minus the input offset voltage. However, under these conditions response time measurements would not be realistic. Therefore, for meaningful measurements the reference voltage is decreased an additional amount to enhance switching. This further variation corresponds to the differential overdrive voltage. A 5-mV overdrive level is generally used in characterizing typical propagation time. For example, the typical response time for an SN72811 is about 32 nanoseconds as shown in Figure 3.4.

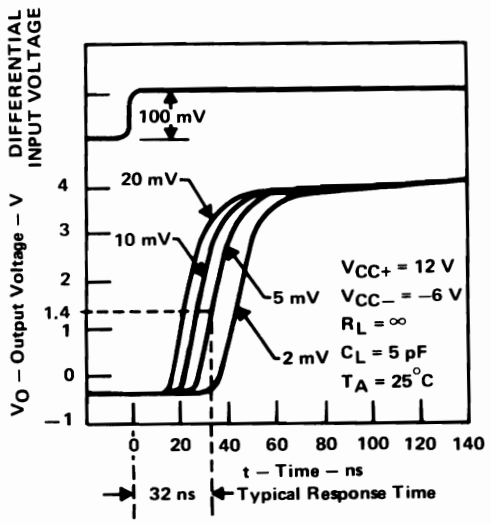


Figure 3.4. Output Response to Various Input Overdrives for the SN72811

3.2.5 Maximum Input Voltage

The input voltage limits for a comparator are of two types: absolute maximum and recommended ratings. First, the manufacturer defines the absolute maximum input voltages which can be applied to an integrated circuit without destroying it, but with no guarantee of proper operation. For example, the SN72710 would not be destroyed if the differential input voltage, V_{ID}, is no greater than ±5 volts, and if the input voltages with respect to ground, V_I, do not exceed ±7 volts.

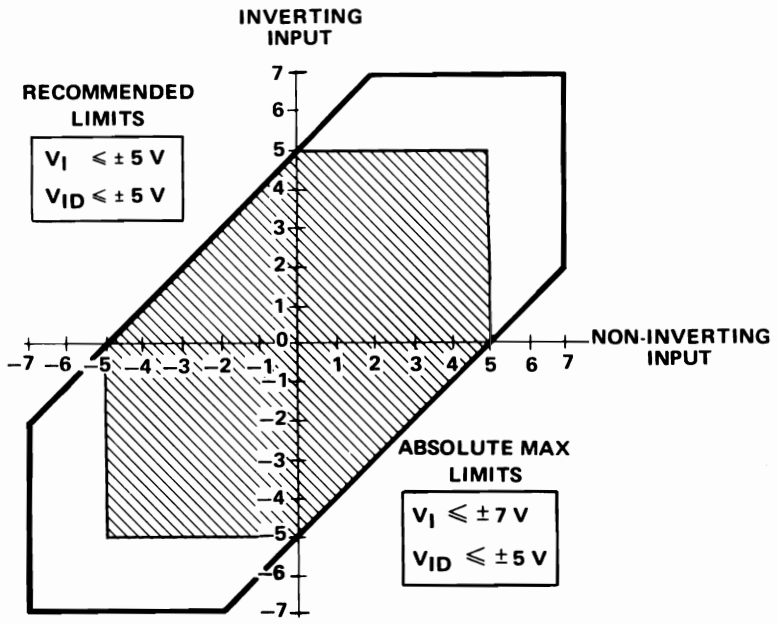


Figure 3.5. Input Voltage Ranges for the SN72710

It is possible to outline an area of non-destruction described by these absolute maximum ratings (Figure 3.5). Within this area is a region limited by the recommended input voltage levels, which for the SN72710 are $V_I \leq \pm 5$ volts and $V_{ID} \leq \pm 5$ volts, as indicated by the shaded portion of Figure 3.5. Operation within these limits is required to assure that the comparator will function according to specifications.

3.2.6 Other Parameters

The comparator is similar to the differential amplifier, and other parameters as defined in Chapter 2 are applicable. Such parameters are:

Bias current
Input differential current
Input offset voltage
Input offset current
Common-mode rejection ratio

3.3 DESCRIPTION OF COMPARATORS

3.3.1 First-Generation Designs

The scope of first-generation comparators is indicated by Table 3.1, a summary of these comparator designs. The circuits include basic single-channel devices, independent dual-channel units, and dual comparators with single output. Devices having inhibit strobes, as well as those without, are identified. Where an improved version of a comparator is listed, the original device is cited first.

Table 3.1 General-Purpose Comparators

	Basic Single-Channel Comparators	Independent Dual-Channel Comparators	Single-Output Dual-Channel Comparators
Without Inhibit Strobes	SN72710 SN72810	SN72720 SN72820	
With Inhibit Strobes	SN72510	SN72514	SN72711 SN72811

The comparators included in each vertical column employ identical functional diagrams and package pin-outs, except for the strobe terminals. For example, the SN72710, SN72810, and SN72510 are offered in the package types shown in Figure 3.6, and are also available in FA, JP, P, and L packages. The SN72720, SN72820, and SN72514 (Figure 3.7) and the SN72711 and SN72811 (Figure 3.8) likewise share the same configurations in the J and N packages. Package types FA and L are also available for the SN72711 and SN72811.

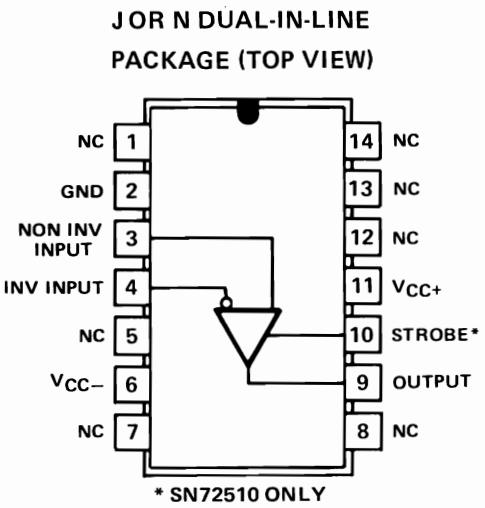


Figure 3.6. Functional Diagram and Pin-Out for the SN72710, SN72810, and SN72510

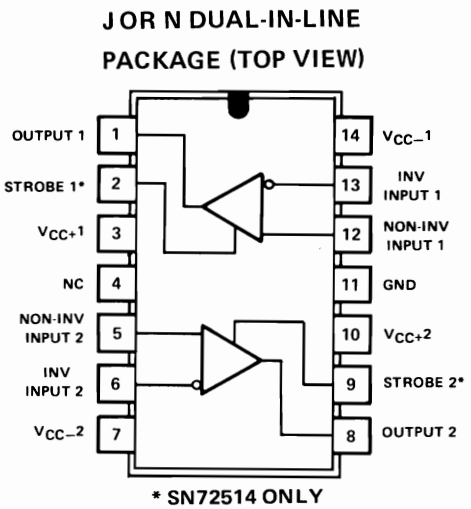


Figure 3.7. Functional Diagram and Pin-Out for the SN72720, SN72820, and SN72514

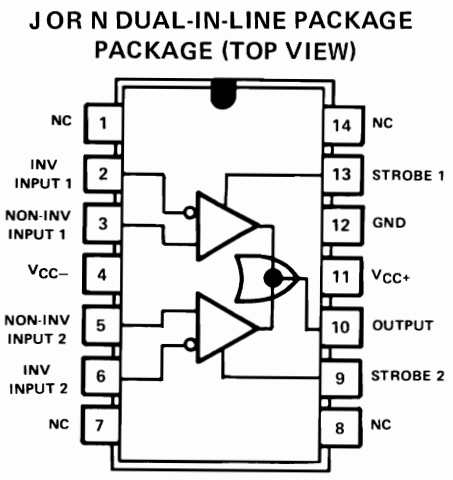


Figure 3.8. Functional Diagram and Pin-Out for the SN72711 and SN72811

SN72710 — This comparator (Figure 3.9) is one of the most basic types. It is easy to use, and in most systems it may be utilized to obtain TTL signals with few or no external components. Its low voltage gain (500 minimum) will result in a little less precision (refer to Figure 3.2) than is available with other comparators. Even under worst-case conditions the SN72710 provides a proper TTL level output with a differential input signal of only ±5 mV. The fact that the inherent stability may be better with a lower-gain (less sensitive) device should be considered when determining which device to use.

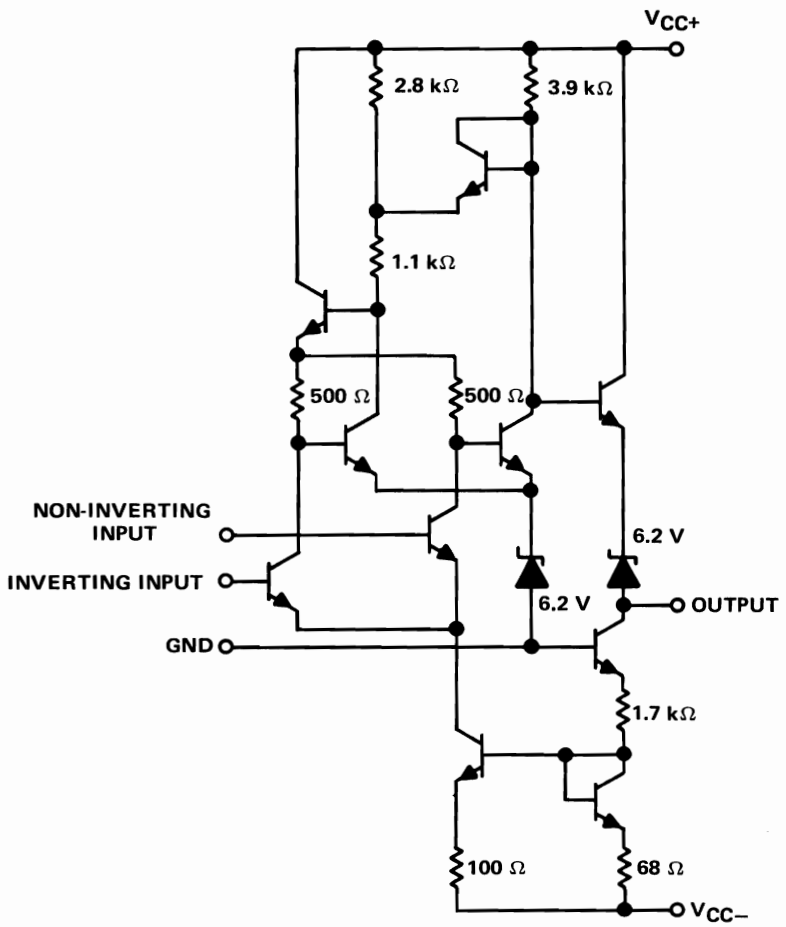


Figure 3.9. Schematic of the SN72710

SN72810 — This device (Figure 3.10), which is pin-to-pin compatible with the SN72710, is an improved version with regard to speed and gain. The voltage gain is 8,000 minimum, resulting in sensitivity to very small signals and greater threshold precision.

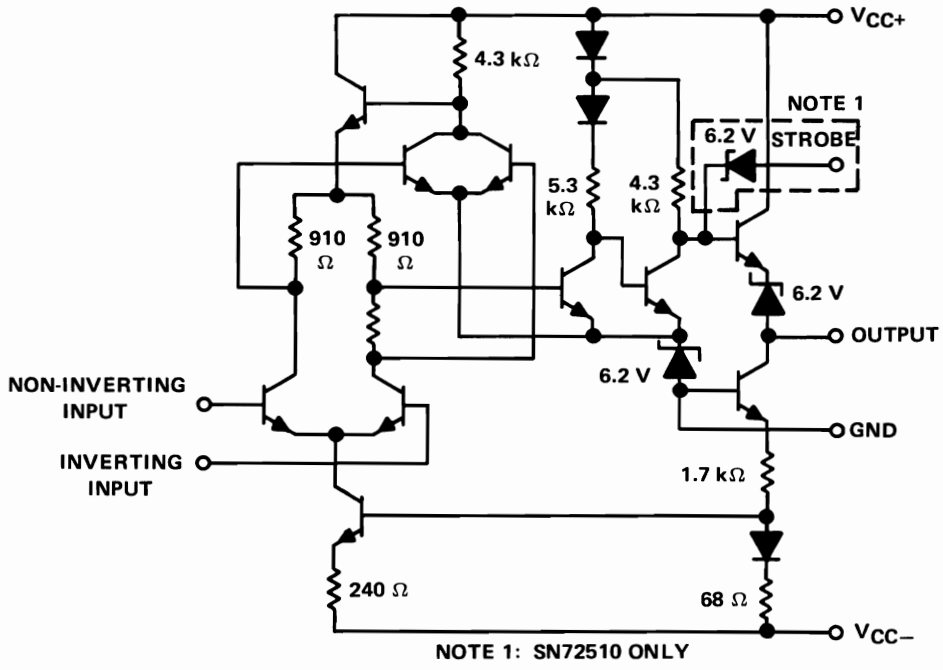


Figure 3.10. Schematic of the SN72810 and SN72510

SN72510 — It is sometimes useful to be able to hold the output of a comparator at its low state, regardless of the input conditions. The SN72510 (Figure 3.10), identical to the SN72810 in performance, has a strobe input which, when in the low state, imposes a low state on the output of the comparator.

SN72720 — The SN72720 (Figure 3.11) consists of two high-speed comparators in a single package, each electrically identical to the SN72710. A separate V_{CC} supply for each channel provides improved isolation between them, and permits reduced package power dissipation by placing one channel on standby (without power) when not in use.

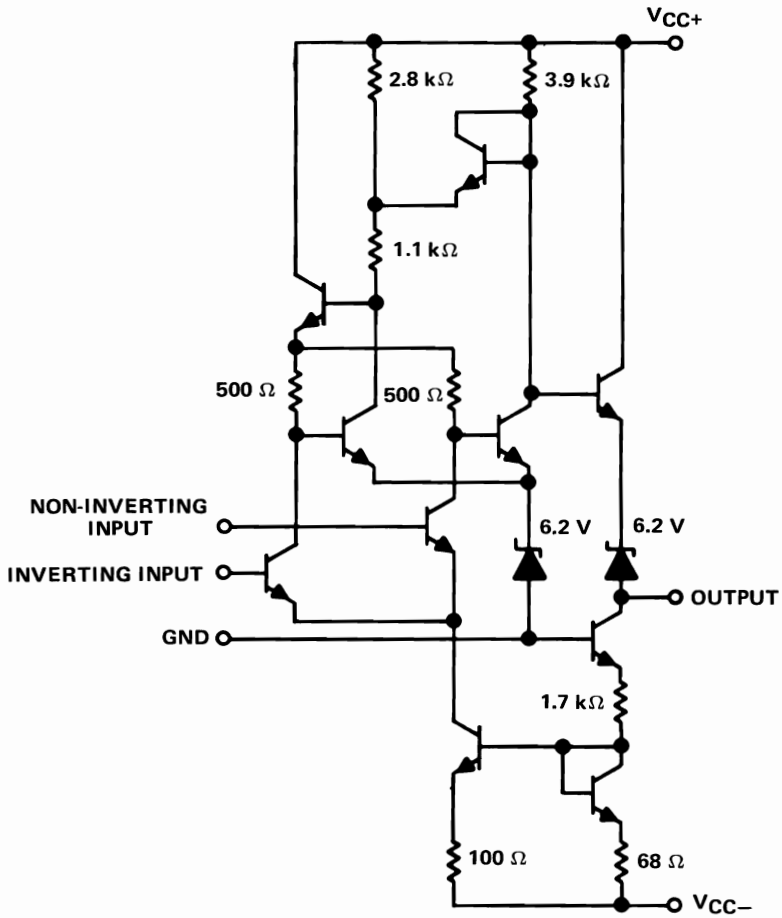


Figure 3.11. Schematic of the SN72720

SN72820 – This dual comparator (Figure 3.12) is an improved version of the SN72720. It is functionally a dual SN72810, and has the same pin-out as the SN72720. Its higher gain and input sensitivity make it desirable for many precision minimum-maximum limit detectors, or applications where two different levels must be detected accurately.

SN72514 – The SN72514 (Figure 3.12) has characteristics identical to those of the SN72820. However, the two independent strobe inputs allow each comparator to be inhibited individually. In many data sensing applications both precision level detection and channel selection are desirable. With the strobes on the SN72514 it is possible to inhibit or enable either or both channels with standard TTL logic levels, allowing the detection of desired incoming signals only during predetermined time intervals.

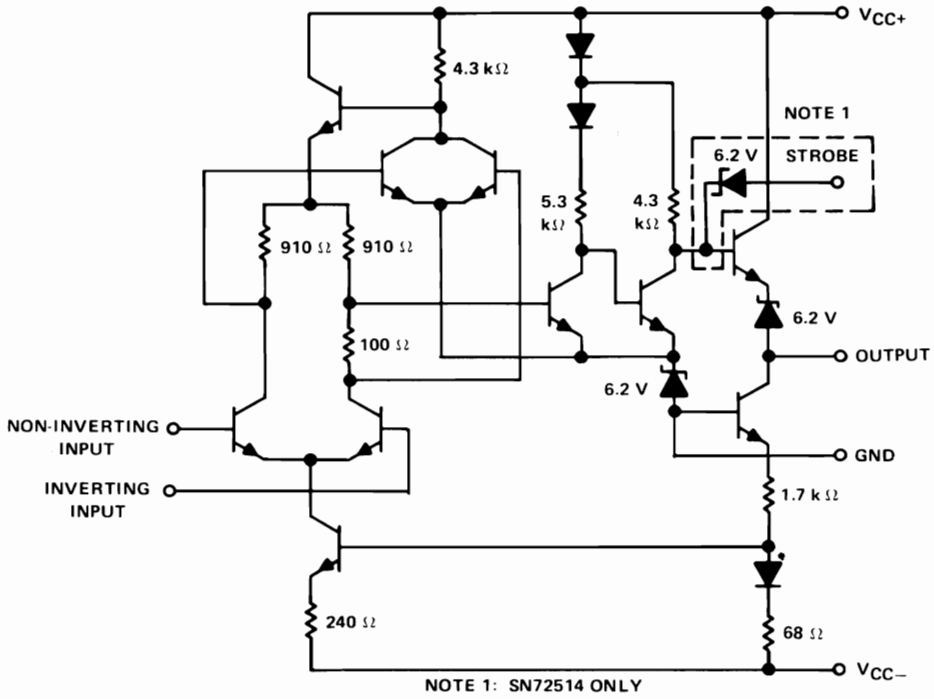


Figure 3.12. Schematic of the SN72820 and SN72514

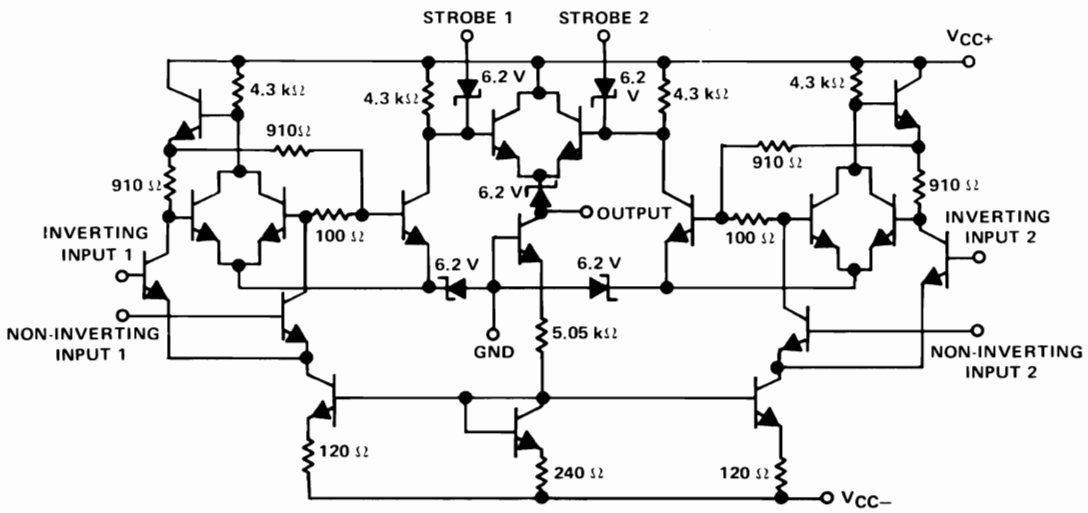


Figure 3.13. Schematic of the SN72711

SN72711 — This device (Figure 3.13) is a high-speed dual-channel comparator with differential inputs and a single low-impedance output. An independent strobe input is provided for each of the two channels; this, when taken low, inhibits the associated channel. If both strobes are taken low the output will be low, regardless of the conditions at the differential inputs.

SN72811 — This circuit (Figure 3.14) has the same pin-out as the SN72711, but it has higher gain for increased accuracy.

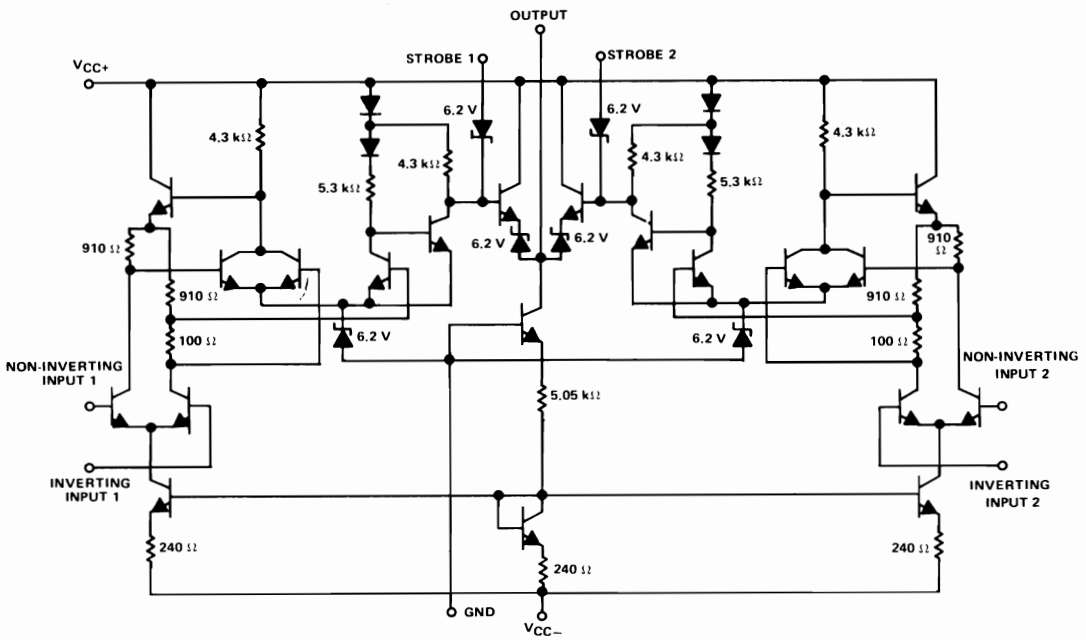


Figure 3.14. Schematic of the SN72811

3.3.2 Second-Generation Designs

SN52106/SN72306 — This comparator (Figure 3.15) features differential inputs, a low-impedance output with high sink-current capability (100 mA), and two strobe inputs. It is designed for directly driving digital logic or heavy loads such as lamps, relays, and VLED displays. Both short-circuit protection and surge-current limiting are provided. A low-level input to either strobe causes the output to be high, regardless of the input conditions. If both strobes are open or at a high logic level, the output voltage is controlled by the differential input voltage. This circuit will operate with a positive supply of 12 volts and any negative supply voltage between −3 volts and −12 volts with little difference in performance.

In addition to the package types shown in Figure 3.16, the SN52106/SN72306 is available in the FA, JP, P, and L packages.

SN72506 — This circuit (Figure 3.16) is a dual-channel version of the SN72306.

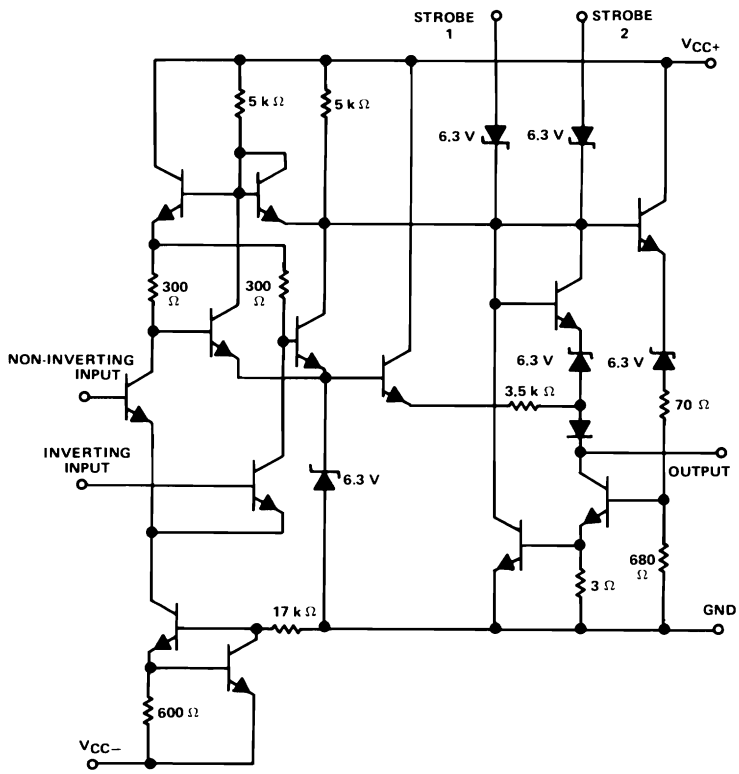


Figure 3.15. Schematic of the SN52106/SN72306

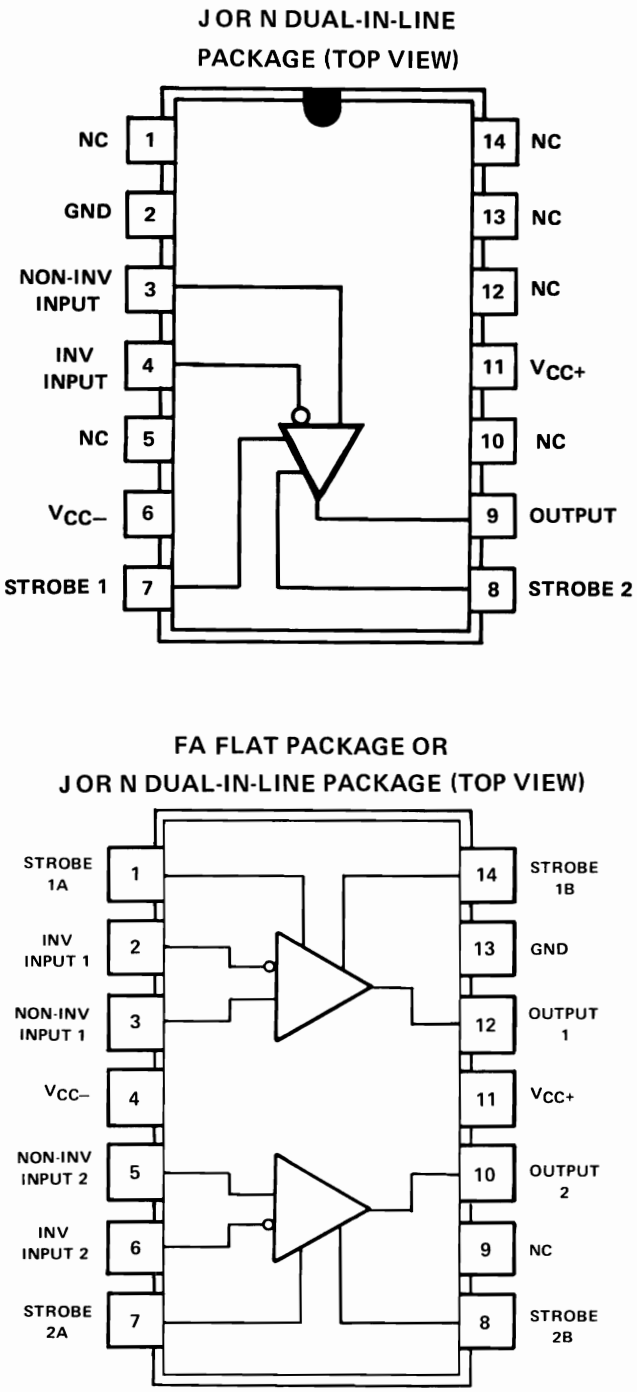


Figure 3.16. Functional Diagram and Pin-Out for the SN52106/SN72306 and SN72506

SN52111/SN72311 — This comparator (Figure 3.17) has very high gain, typically 200,000. It is designed to operate from a wide range of power supplies, including the ±15-volt supplies typical for operational amplifiers and the single 5-volt supply typical for logic systems. The circuit is relatively slow compared to most comparators, with a response time of 165 ns typically.

This circuit is capable of driving lamps or relays, and can switch voltages of up to 50 volts at current levels as high as 50 mA. Both collector and emitter outputs are available and can be isolated from system ground. Outputs may be referenced to ground, V_{CC+}, or V_{CC-}. Other features are strobe capability and offset control. Offset balance terminals allow extreme accuracy for critical signal detection. The outputs of several devices may be wire-OR connected. Although somewhat slower than other comparators, these devices are not as sensitive to spurious oscillations.

In addition to the package types shown in Figure 3.17, the SN52111/SN72311 is offered in the FA, JP, P, and L packages.

3.4 COMPARATOR APPLICATIONS

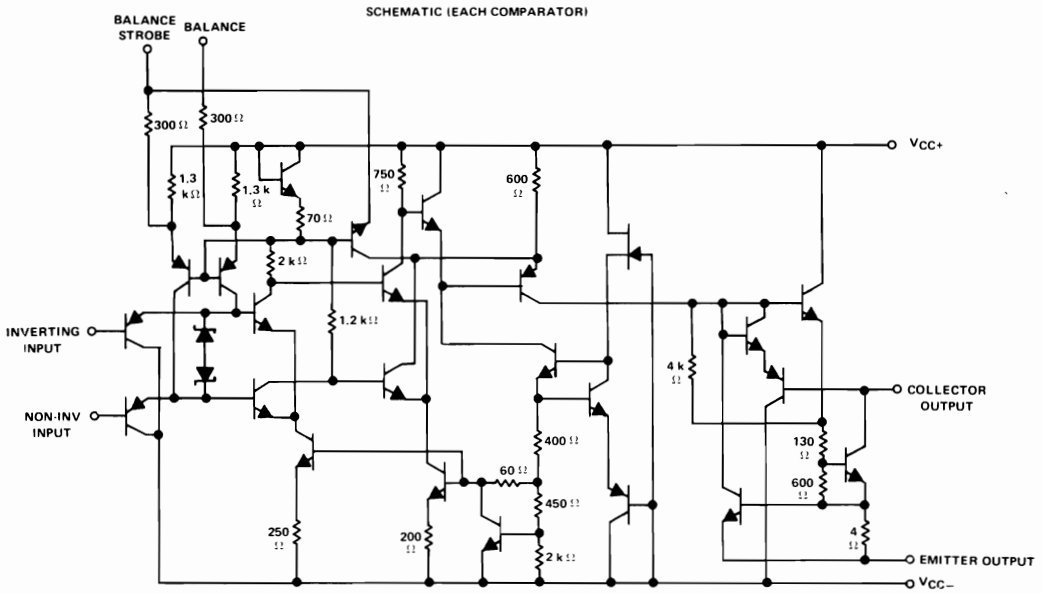
3.4.1 Application Precautions

In addition to the absolute ratings on input and output voltages and currents specified for each comparator, one should be aware of the problems which can arise when using the comparator.

Input Rise Time — The comparator is basically a differential amplifier with very high open-loop gain. The output of the comparator is specified to be compatible in voltage and current with the inputs of TTL circuits. However, this type of logic requires switching times of less than 150 nanoseconds to obtain correct functioning without oscillation. It is therefore necessary that the comparator input signal vary sufficiently rapidly to avoid this problem.

Figure 3.18a shows the output of an SN72710 being driven by a ramp which varies at about 0.1 millivolt per microsecond. The switching times of the output taken between 0.8 volt and 2 volts are about 10 microseconds for the fall and rise times. In this mode the output of the comparator is not compatible with TTL circuits.

Figure 3.18b shows an SN72810 working under the same conditions. The gain being higher, the switching speed is also higher, and the rise time appears to be compatible with TTL circuits. However, some oscillation is present during the periods of switching, because the input signal remains too long in the high-gain linear range of the comparator. A required input condition for obtaining a good output function from a comparator is one that forces the output signal to vary between 0.8 volt and 2 volts in 150 nanoseconds or less.



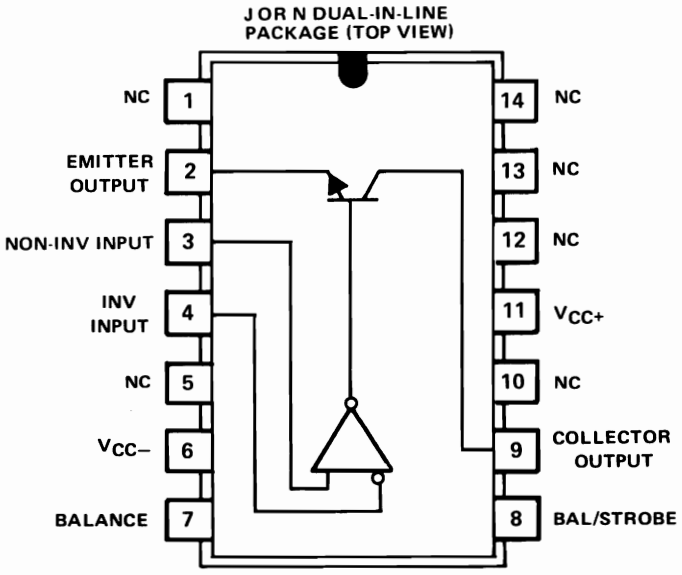
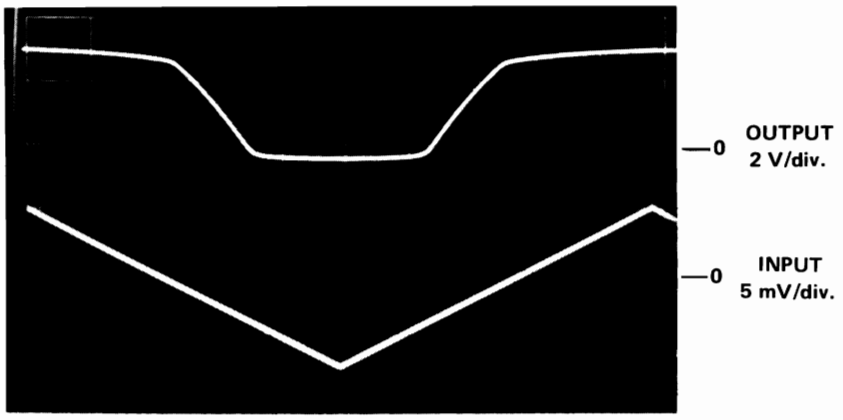
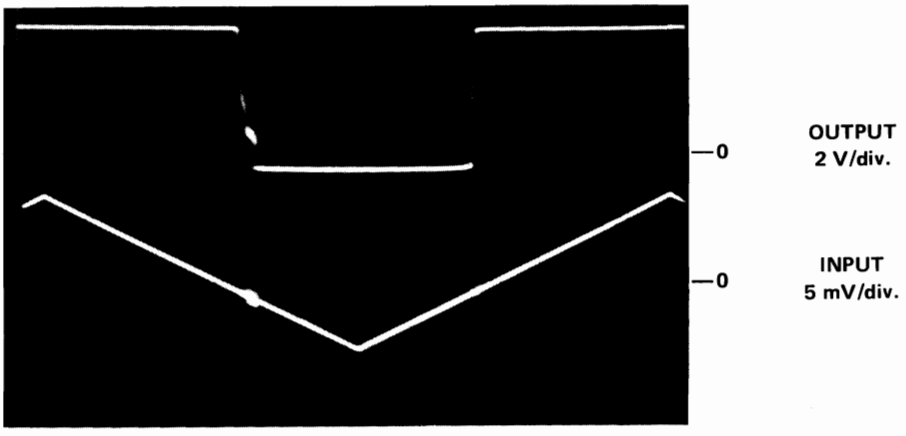


Figure 3.17. Schematic, Functional Diagram, and Pin-Out for the SN52111/SN72311



20 μs/div.

a. SN72710



20 μs/div.

b. SN72810

Figure 3.18. Response of an SN72710 and an SN72810 to a Ramp Input

With the minimum gain, A_{VD}, of the comparator known, the input signal must vary at a minimum rate determined by

$$\frac{2\text{ V} - 0.8\text{ V}}{150\text{ ns X } A_{VD}}$$

For the SN72710 this minimum rate is

$$\frac{2\text{ V} - 0.8\text{ V}}{150\text{ ns X } 500} = 16\text{ mV}/\mu\text{s}$$

and for the SN72810 the rate is

$$\frac{2\text{ V} - 0.8\text{ V}}{150\text{ ns X } 8{,}000} = 1.0\text{ mV}/\mu\text{s}$$

When these input conditions cannot be met, it is always possible to add some positive feedback or a Schmitt trigger configuration (Figure 3.19) to accelerate the speed of the input. The hysteresis thus generated makes the comparator somewhat less sensitive.

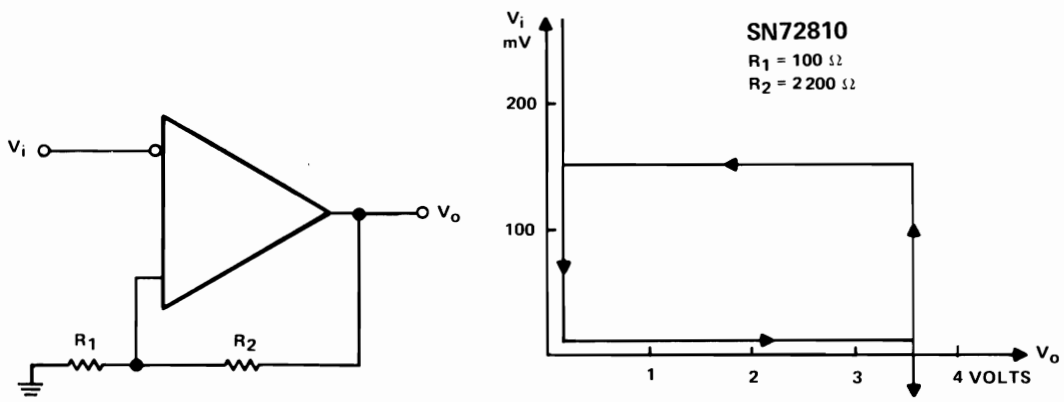
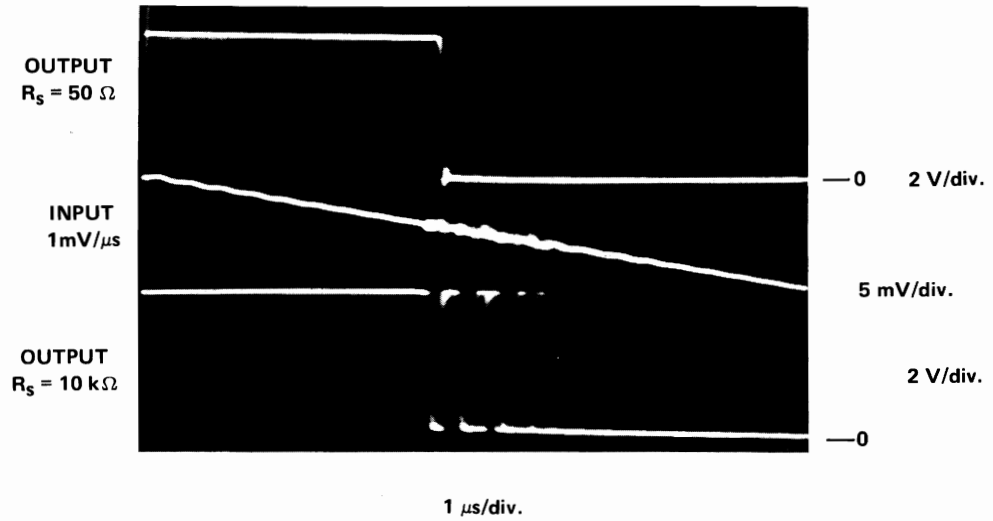


Figure 3.19. Use of Hysteresis to Prevent Oscillations

Source Impedance — The input bias current of a comparator is generally of the order of 10 microamps. When the differential input voltage makes the comparator switch, this input current is present at one of the inputs, and will be zero at the other. If the source impedances are not negligible, feedback will lower the gain of the comparator and create parasitic oscillations.

Figure 3.20 shows this phenomenon occurring with an SN72810. The comparator is driven by a ramp at the previously determined minimum rate of one millivolt per microsecond, as represented by the center curve. The upper curve shows the response of the comparator with a source impedance of 50 ohms. The lower curve represents the response of the same comparator with a source impedance of 10,000 ohms. The initial switching occurs sooner with the high source impedance as the bias current results in additional offset voltage. The subsequent oscillations make this circuit configuration unusable with low-slew-rate input signals.



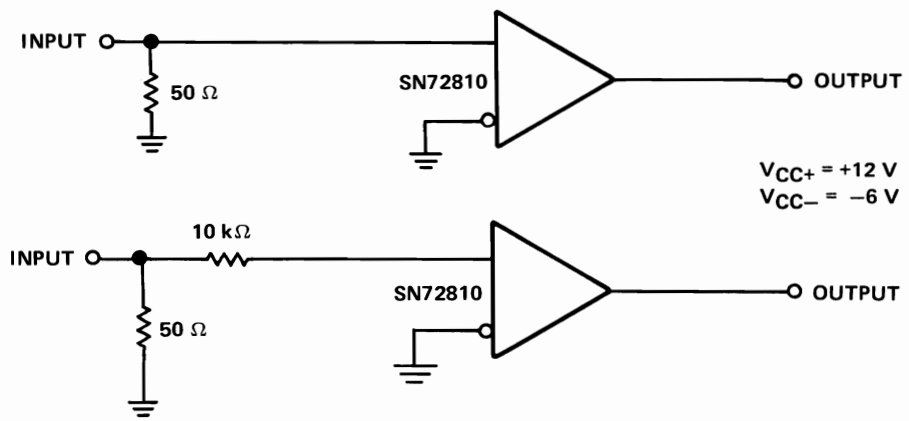


Figure 3.20. Influence of Source Impedance

3.4.2 Specific Applications

The field of applications for comparators is very wide. Comparators are used each time a decision is made regarding the amplitude of a voltage. The following comparator applications are a few examples of the many uses for these devices.

Rotation Detector Using Magnetic Sensing — An application in which the source impedance is not negligible is shown in Figure 3.21. A rotation detector using a magnetic sensor determines the source impedance. Voltage V_A, which is obtained when the cylinder is rotating, supplies, after integration by C, a relatively high-impedance signal B that varies rather slowly. It is therefore necessary to provide, by A1, an impedance transformation with or without gain, in order to establish the comparison using A2, whose output will indicate rotation or non-rotation of the cylinder. Note that some positive feedback is used around the comparator to provide stability.

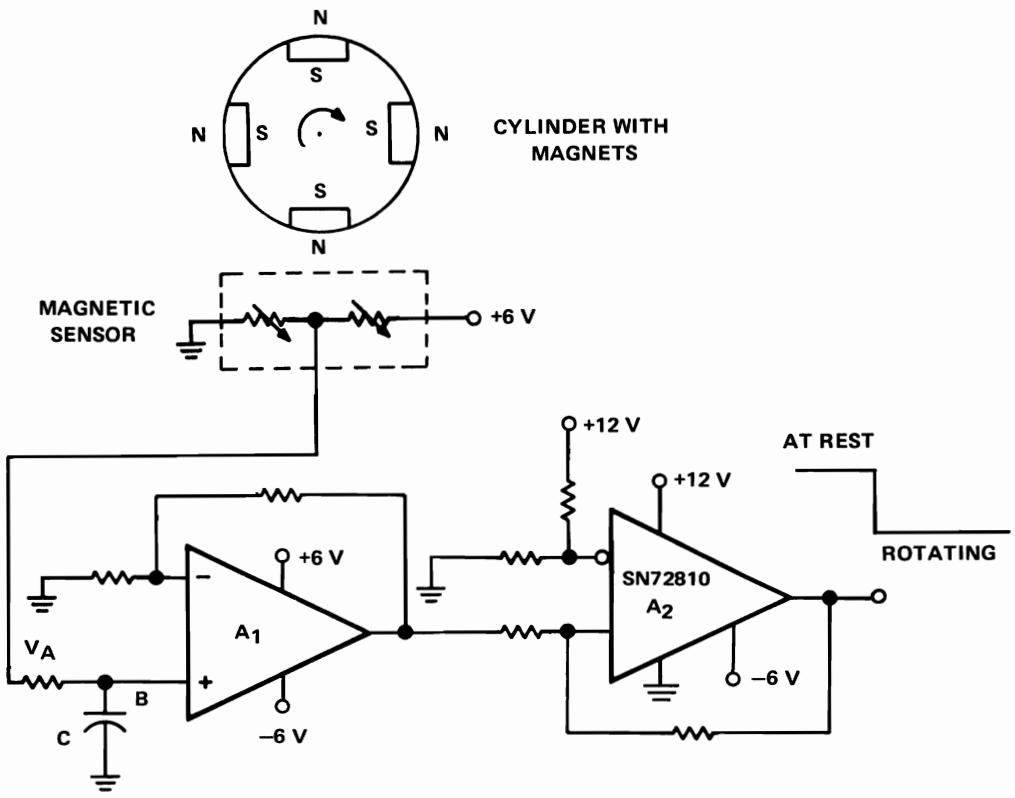


Figure 3.21. Rotation Detector Using a Magnetic Sensor

Crystal-Controlled Logic Generator — Figure 3.22 shows a crystal-controlled oscillator whose output levels are compatible with TTL logic. The negative-feedback RC circuit is selected to ensure that the crystal will oscillate only at its fundamental frequency. A small capacitor is used in series with the crystal, as shown, to trim the oscillator to the exact frequency required. The duty cycle is determined by the bias level at the non-inverting input. With the SN72810, the maximum operating frequency is approximately 5 MHz.

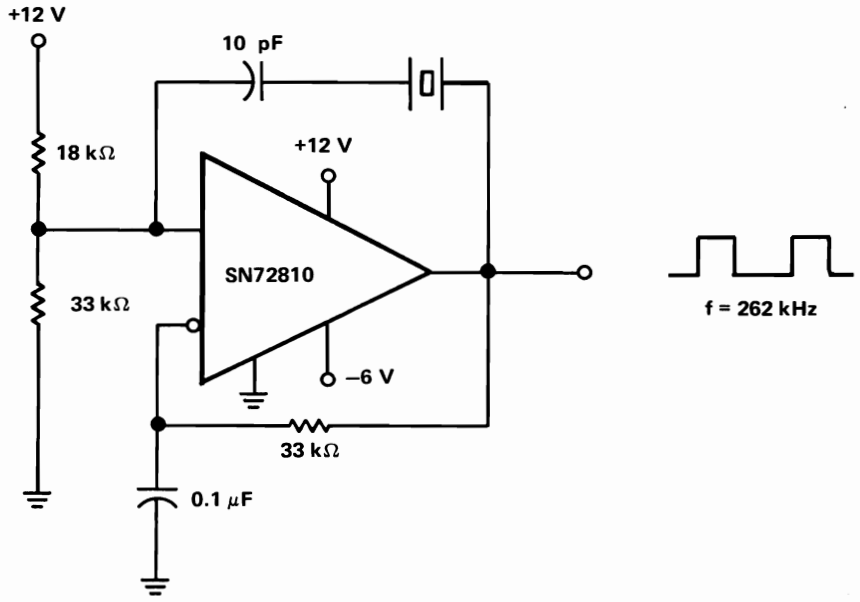


Figure 3.22. Crystal-Controlled Logic Generator

Voltage and Polarity Detector — This application (Figure 3.23) combines a dual comparator (SN72820) with a ramp generator, 1/3 of an SN7404 hex inverter, 1/4 of an SN7486 quad two-input exclusive-OR gate, and 1/2 of an SN7474 flip-flop, to form a voltage level and polarity detector. One channel of the SN72820 compares the input ramp with a ground reference, while the other compares it with the input voltage being tested.

As shown in Figure 3.23, the exclusive-OR gate's output will go to a high logic level when one comparator has switched, and return to a low logic level when the other comparator switches. The resulting pulse width is therefore directly related to the amplitude of the input voltage, and could be used to control a counter to acquire a digital read-out of the input voltage.

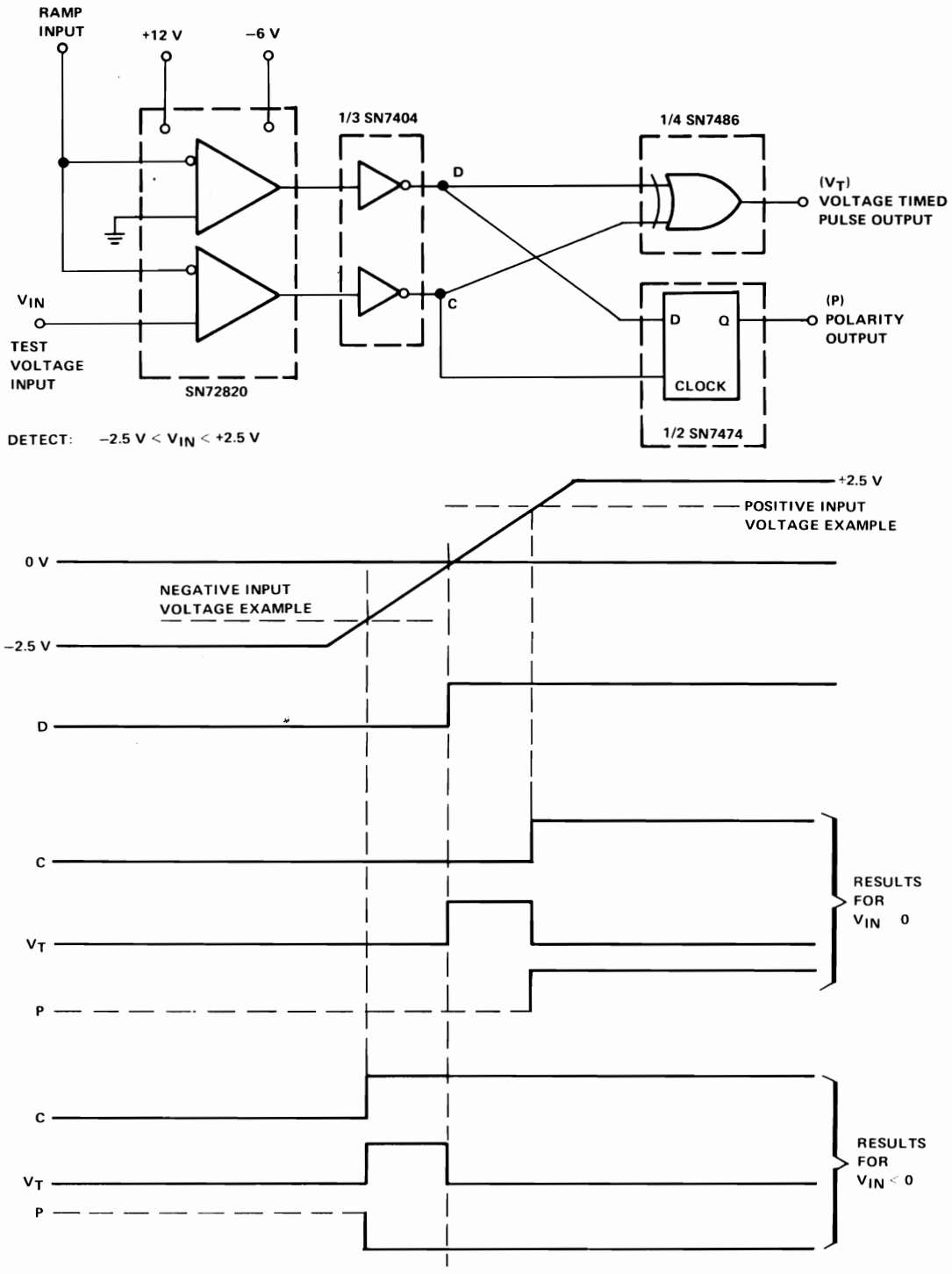
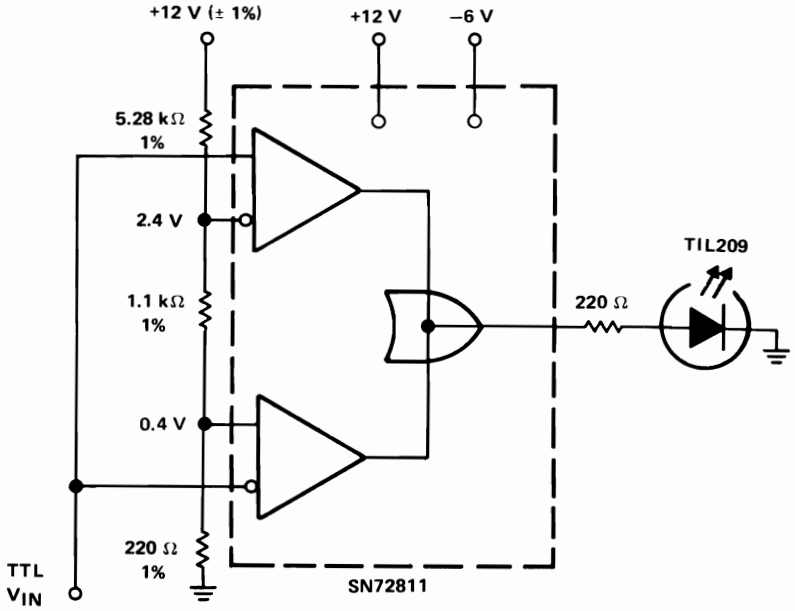


Figure 3.23. Voltage and Polarity Detector

The SN7474 D-type edge-triggered flip-flop will have a high-level logic output if the D input is high when the clock input is switched high, and a low-level logic output if the D input is low. Thus the SN7474 output (P) will be low for a negative-level input voltage and high for a positive-level input voltage. This information can be used to control the sign of the voltage in a digital read-out display.

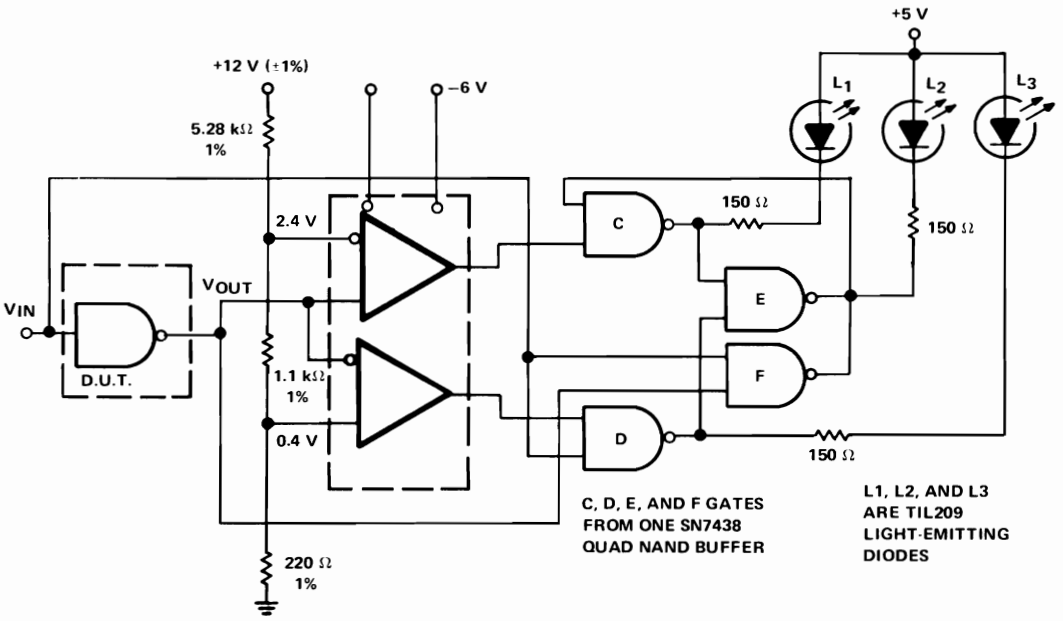
Basic Window Detector — In many testing applications it is desirable to detect parameter values below a specified minimum or above a specified maximum. Such a min-max limit detector is referred to as a window detector. A dual comparator with a single output such as the SN72811 can detect the presence or absence of a signal between two limits (Figure 3.24). In this application a proper TTL logic level (high or low) at the input will result in the TIL209 visible-light-emitting diode (VLED)



TTL VOLTAGE INPUT CONDITION	TIL209 VLED CONDITION
0 LOGIC $V_{IN} < +0.4$ V	ON
IMPROPER LEVEL $0.4_V < V_{IN} < 2.4$ V	OFF
1 LOGIC $V_{IN} > 2.4$ V	ON

Figure 3.24. Proper TTL Logic Level Detector

being turned on. An improper logic level, i.e., greater than 0.4 volt but less than 2.4 volts, will result in the TIL209 being off. If we wish to ensure that the gate output logic level is correct for its type of input, as well as to determine whether the logic amplitudes are correct, an SN72820 dual comparator may be used as shown in Figure 3.25. This circuit will indicate whether the NAND gate under test meets the data-sheet specifications for output logic levels. Light-emitting diode L1 will light for a good logic 1 output; L2 will light for a good logic 0 level output; and L3 will light for any logic-failure mode.



OUTPUT TEST CONDITION	V_{IN}	V_{OUT}	L_1	L_2	L_3
GOOD HIGH LEVEL	0.4 V	≥2.4 V	ON		
POOR OR LEAKY	0.4 V	>0.4 V <2.4 V			ON
SHORTED LOW	0.4 V	≤0.4 V			ON
GOOD LOW LEVEL	2.4 V	≤0.4 V		ON	
POOR OR LEAKY	2.4 V	>0.4 V <2.4 V			ON
SHORTED HIGH	2.4 V	>2.4 V			ON

Figure 3.25. Proper TTL Output versus Input Logic Level Indicator

4

Video Amplifiers

4.1 GENERAL

A video amplifier may be generally described as a differential amplifier with high open-loop bandwidth. Its ideal characteristics are identical with those of the ideal operational amplifier: "infinite" input resistance and gain, with "zero" output resistance and offset.

The primary differences between an operational amplifier and a video amplifier are the bandwidth and dc gain. The 3-dB bandwidth is around 100 kHz for a typical operational amplifier, but may be as much as 100 MHz for a video amplifier. Conversely, dc gain is around 100 dB for the operational amplifier and about 40 dB for the video amplifier. Most video amplifiers will function only in the open-loop mode because their internal phase shift does not permit the use of negative feedback to control gain. Video amplifiers, unlike operational amplifiers, have a rather limited output voltage swing which for high-frequency operation is limited to a few volts.

The input stage of most integrated-circuit video amplifiers consists of the basic emitter-coupled differential pair connected to a constant-current source transistor. In fact, all of the early video amplifiers were little more than these three transistors and a few integrated resistors and diodes, with all component terminals brought out for external interconnection. A typical configuration is shown in Figure 4.1. The bias input voltage can be adjusted to provide symmetrical output voltage swing with respect to ground.

4.2 PARAMETERS

Parameters of video amplifiers are similar to those of operational amplifiers and comparators. However, the following parameters are specifically applicable to video amplifiers.

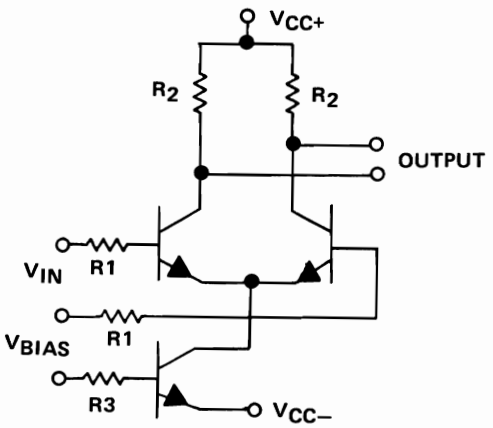


Figure 4.1. Basic Video-Amplifier Circuit

4.2.1 Voltage Gain

Video amplifiers have a differential input and output. The voltage gain is defined as the ratio of the change in differential output voltage to the change in differential input voltage (Figure 4.2).

4.2.2 Common-Mode Output Voltage

With the inputs grounded, the outputs of a video amplifier are at dc levels with respect to ground. The average of these two dc output voltages is the common-mode output voltage (Figure 4.3).

4.2.3 Output Offset Voltage

Under the same conditions (Figure 4.3), the difference between the dc levels at the two outputs is defined as the output offset voltage. This offset voltage can be referred to the input by dividing it by the differential voltage gain of the amplifier.

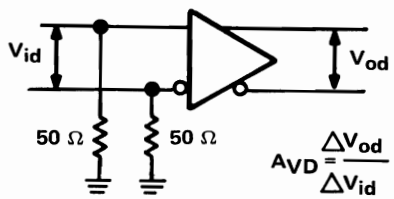


Figure 4.2. Differential Voltage Gain

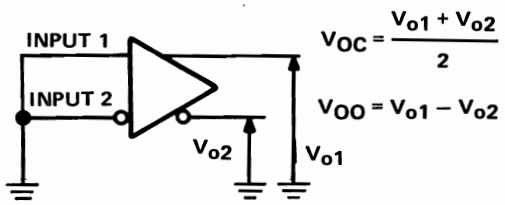


Figure 4.3. Common-Mode and Offset Voltages

4.3 DESCRIPTION OF VIDEO AMPLIFIERS

4.3.1 SN7510

With a 3-dB bandwidth of 40 MHz, this circuit (Figure 4.4), which is a basic video amplifier, has a minimum voltage gain of 60. Its input and output resistances are typically 6000 ohms and 35 ohms respectively; its operating frequency is from dc to greater than 100 MHz. In addition to the package shown, this device is also available in the FA and L packages.

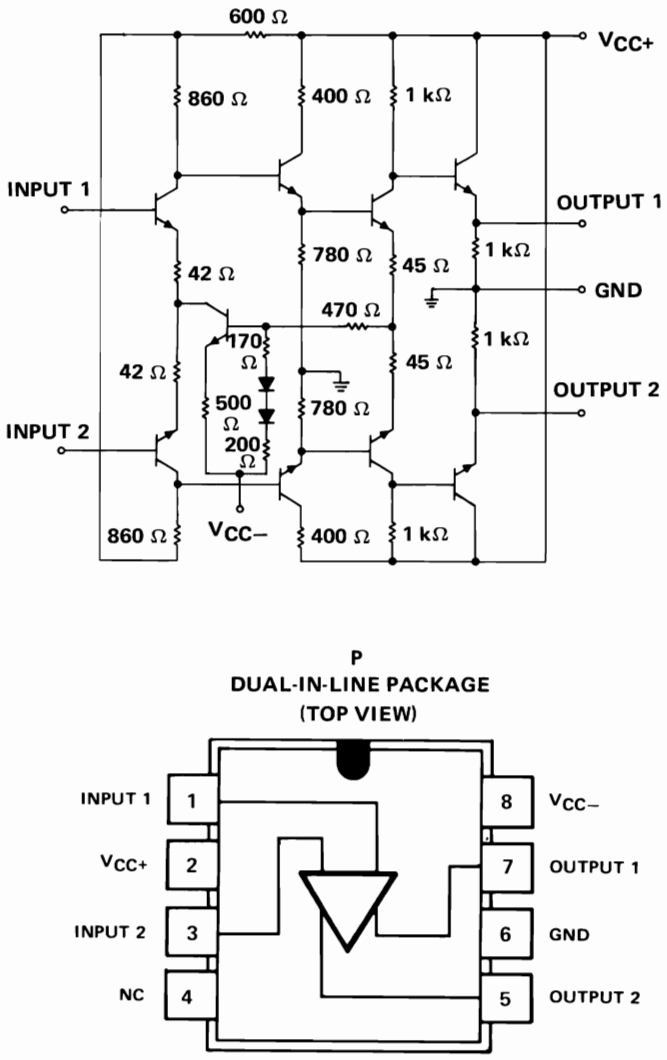


Figure 4.4. Schematic and Package Diagram of the SN7510

4.3.2 SN7512

This video amplifier offers improved performance in comparison with the SN7510; its 3-dB bandwidth is 80 MHz with a minimum gain of 200. Typical input and output resistances are 6000 ohms and 35 ohms respectively. Offset null terminals are provided to allow correction of the differential offset voltage by means of an external potentiometer. The SN7512 is also available in the type L plug-in package.

4.3.3 SN7514

Though basically the same as the SN7512 (see Figure 4.5), this circuit has no connections for nulling out the output offset voltage. Having fewer external

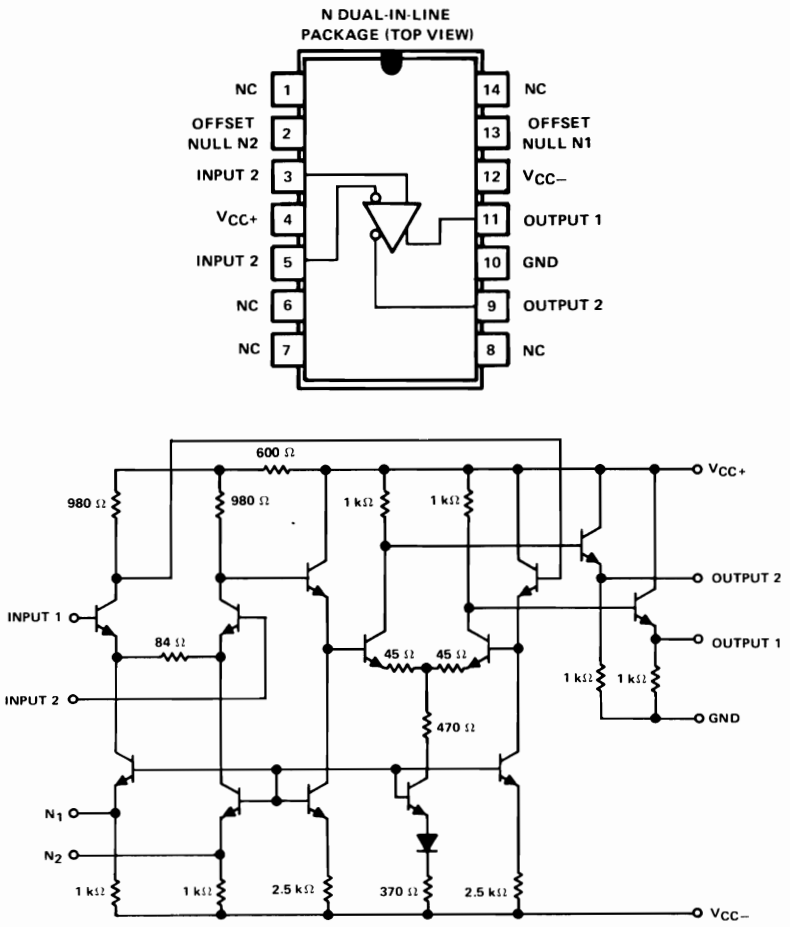


Figure 4.5. Schematic and Package Diagram of the SN7512

connections, the SN7514 is available in the eight-pin JP and P packages shown in Figure 4.6, and the type L plug-in package.

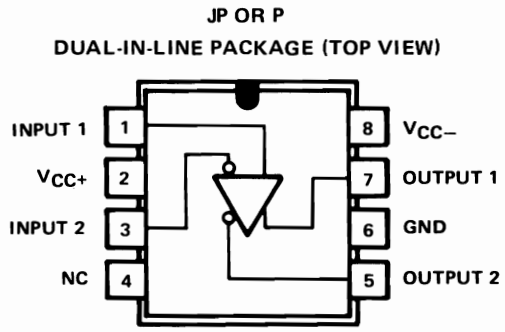


Figure 4.6. Package Diagram of the SN7514

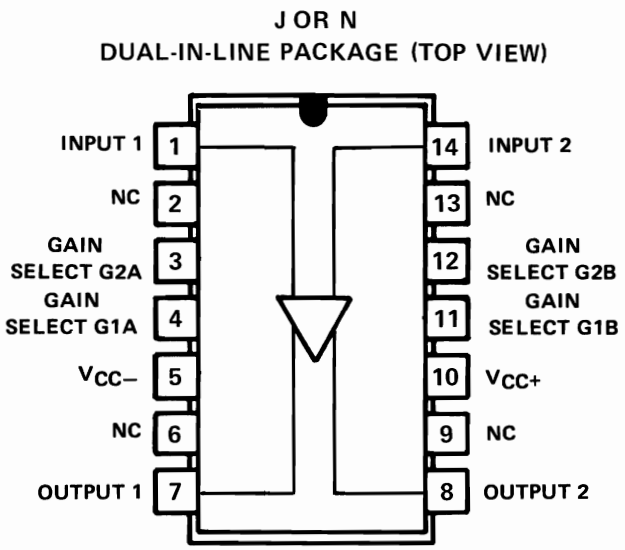
4.3.4 SN72733

The SN72733 (see Figure 4.7) is a high-performance video amplifier, having a 3-dB bandwidth of 200 MHz for a voltage gain of 10. The circuit has no provision for external feedback. However, connections to the emitters of the input transistors allow the choice, by external connections, of gain values of 10, 100, or 400. By means of a variable resistor or an FET all other intermediate gain levels are attainable.

4.3.5 SN7511

This video amplifier (Figure 4.8) is structurally similar to an operational amplifier and has many similar applications. Its frequency characteristics are such that a stable closed-loop configuration with 30-dB gain results in a 30-MHz bandwidth. Accessibility to the collectors of the input transistors permits frequency compensation and offset balancing. High gain, low offset, and low phase shift of the SN7511 allow use of feedback techniques to control its closed-loop gain. In addition to the N package this device is also available in the FA and L packages.

Another feature of the SN7511 is its regulator input (Figure 4.8) which allows operation from a single +12-volt supply. For single-supply operation the V_{CC-} terminal is connected to ground and the regulator input is connected to a +12-volt supply. With the device ground terminal left open, the internal zener will provide a 1/2 V_{CC} reference required by the current source for the input stages. Note that the input terminals are now referenced to about 1/2 V_{CC}, or +6 volts, rather than to ground; any dc input terminations should therefore be connected to a +6-volt reference level rather than to ground.



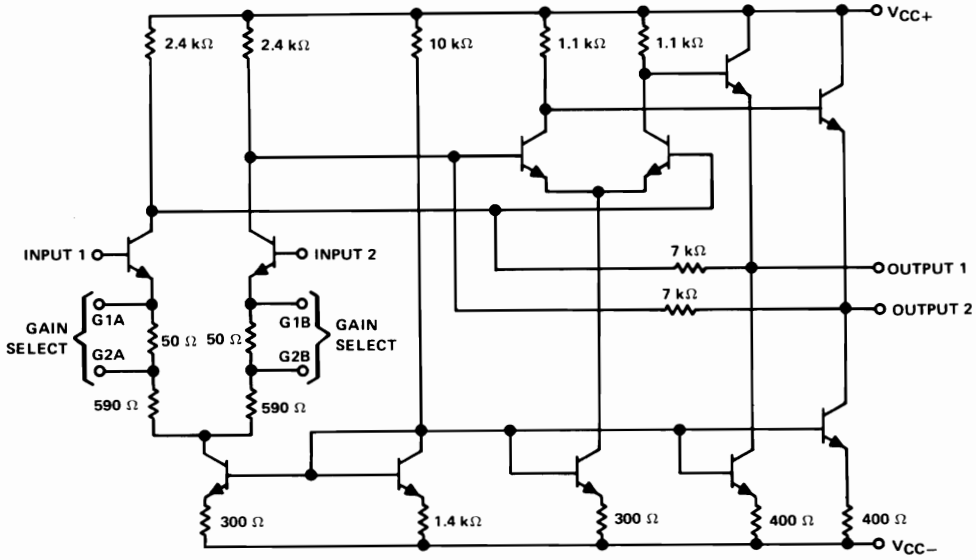
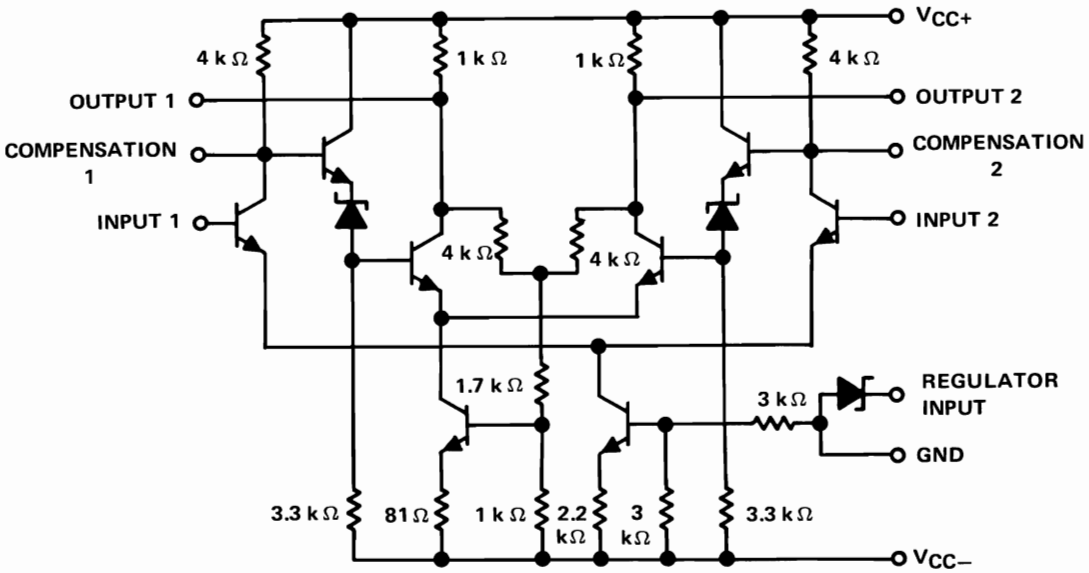


Figure 4.7. Schematic and Package Diagram of the SN72733



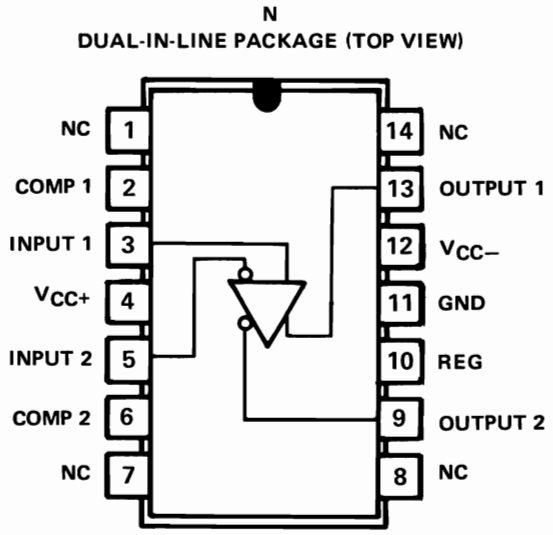


Figure 4.8. Schematic and Package Diagram of the SN7511

4.4 VIDEO AMPLIFIER APPLICATIONS

Video amplifiers have been designed to solve such problems as the amplification of wideband signals in video, RF, and radar data processing, but have applications in many other areas.

4.4.1 Wideband Amplifier

Used as an operational amplifier the SN7511 provides a stable gain which depends only on the value of resistors used. The compensation circuit, consisting of the series RC network, assures stability of the circuit. The SN7511 can be used as a wideband line amplifier providing various gains and bandwidths as shown in Figure 4.9.

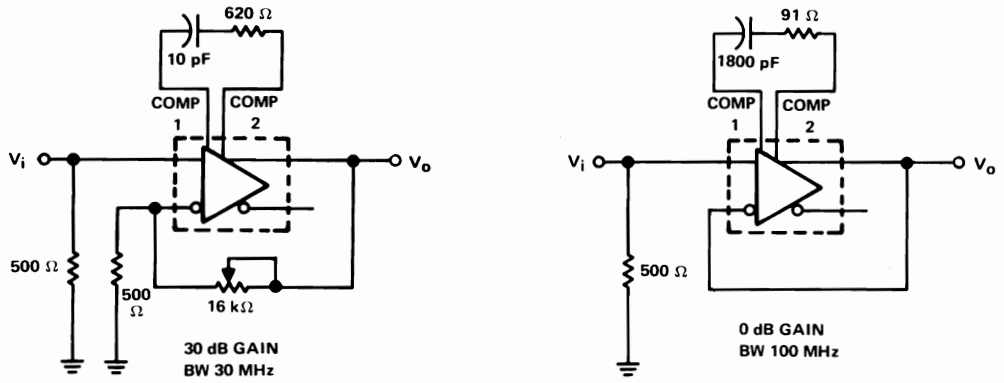


Figure 4.9. Adjusting Gain of the SN7511

4.4.2 Transformer Feedback Oscillator

Figure 4.10 shows an LC tuned oscillator circuit using an SN7511. With unity turns ratio and C and L at resonance, the feedback factor is unity, and the gain of the network is the voltage gain of the amplifier G, which is the resistance of the FET divided by 500 ohms. According to the Barkhausen criteria, if the gain and feedback-factor product is greater than 1 (in this case if $G > 1$) oscillations will occur at a frequency determined by the LC network, consisting primarily of n_1 and C_1. With proper choice of component values, the circuit can be used at frequencies as high as 50 MHz.

The use of an FET in the feedback loop provides a voltage-controlled method of reducing the amplifier gain to below that required to sustain oscillation. The gate input of the FET can therefore be used as a strobe control to switch the oscillator off and on.

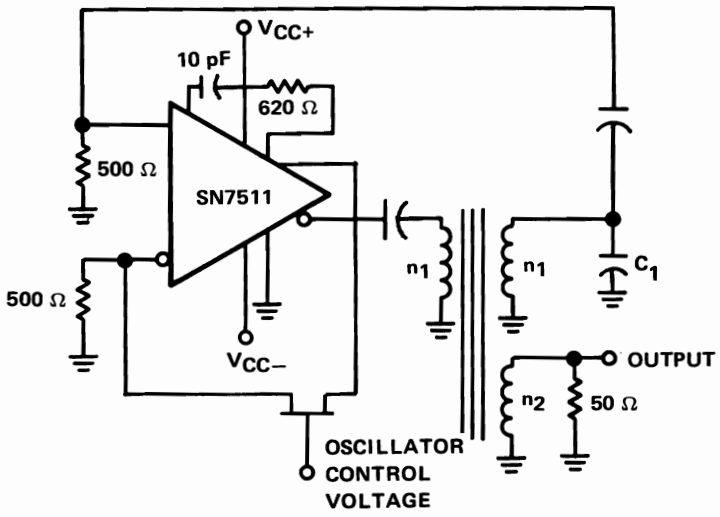


Figure 4.10. Basic Transformer-Feedback Oscillator

4.4.3 High-Input-Impedance Wideband Amplifier

The input resistance of most video amplifiers is relatively low (6000 ohms typically). However, the SN72733 with the gain set at 100 has a typical input resistance of 24,000 ohms. An FET such as the 2N3822, with high-frequency capability, can be used as shown in Figure 4.11 to increase the input resistance with

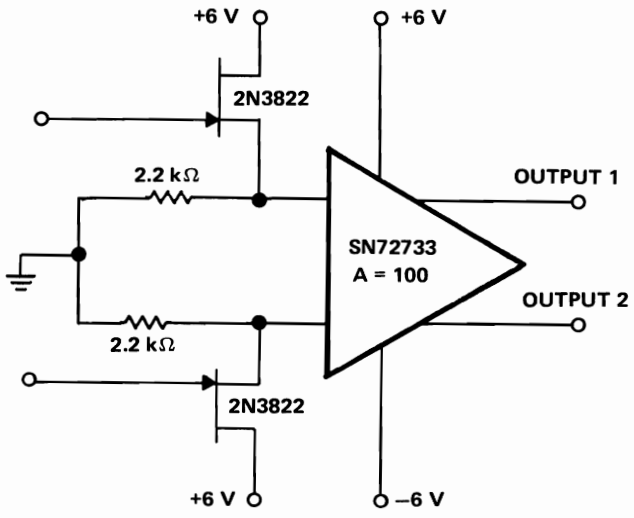
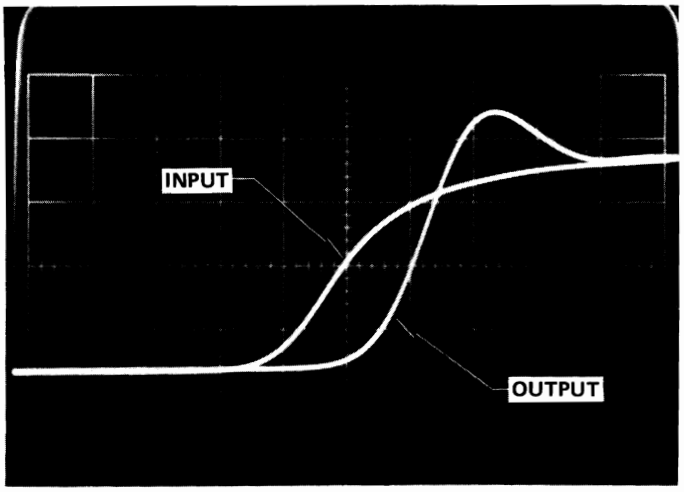
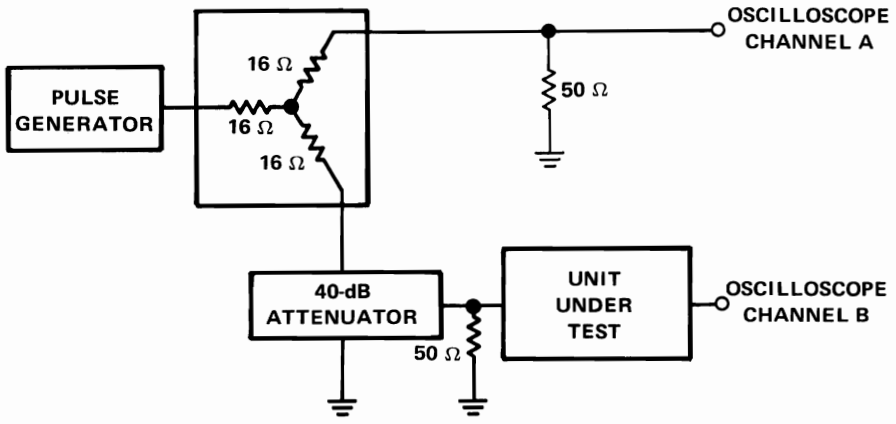


Figure 4.11. High-Input-Impedance Wideband Amplifier

little effect on the overall bandwidth. Figure 4.12 shows the test setup and measured pulse response of this circuit. A high-frequency sampling oscilloscope was used for observing the amplifier's propagation delay and transition times.



a) RESPONSE TIME



b) BLOCK DIAGRAM OF TEST SETUP

Figure 4.12. Test Setup and Pulse Response of the Circuit in Figure 4.11

4.4.4 Variable Phase Shifter

The circuit shown in Figure 4.13 permits a phase shift between 0 and 180°, depending on the values of R and C and the frequency of operation. Normally this

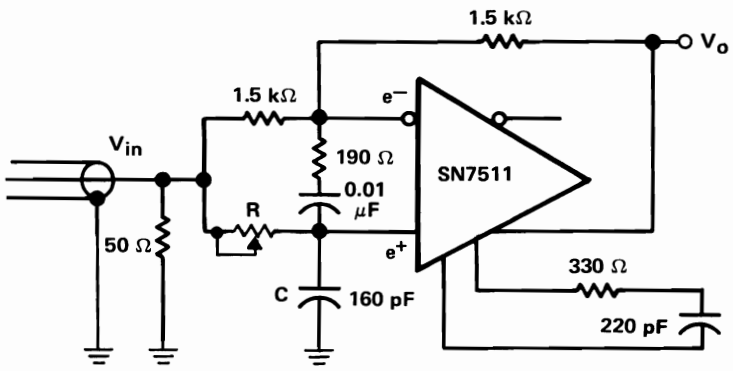


Figure 4.13. Variable-Phase-Shift Circuit

circuit is used to phase-shift a fixed frequency. Assuming an ideal amplifier, the relationship between the output voltage and the input voltage can be computed by equating the voltages at the inverting and non-inverting inputs:

$$e- = \frac{V_o + V_{in}}{2}$$

$$e+ = \frac{V_{in}}{1 + j\,\omega RC}$$

Equating these voltages yields

$$\frac{V_o}{V_{in}} = \frac{1 - j\,\omega RC}{1 + j\,\omega RC}$$

which is the transfer function of the circuit. The real part of the transfer function is equal to 1, regardless of the values of R and C. However, the phase angle ϕ varies from 0° (if R is zero) to −180° (if R is infinite) according to the following relationship

$$\tan \phi = \frac{-2\,\omega RC}{1 - \omega^2 R^2 C^2}$$

Figure 4.14 shows the resulting phase relationship of the output and input signals in the setup of Figure 4.13. The sampling oscilloscope employed in this experiment has negligible phase shift at 5 MHz. The $-90°$ phase shift was obtained by using a 160-pF capacitor and a 194-ohm resistor. The calculated resistance, determined from the condition that ωRC equals unity, is 200 ohms for a capacitance of 194 pF and a frequency of 5 MHz.

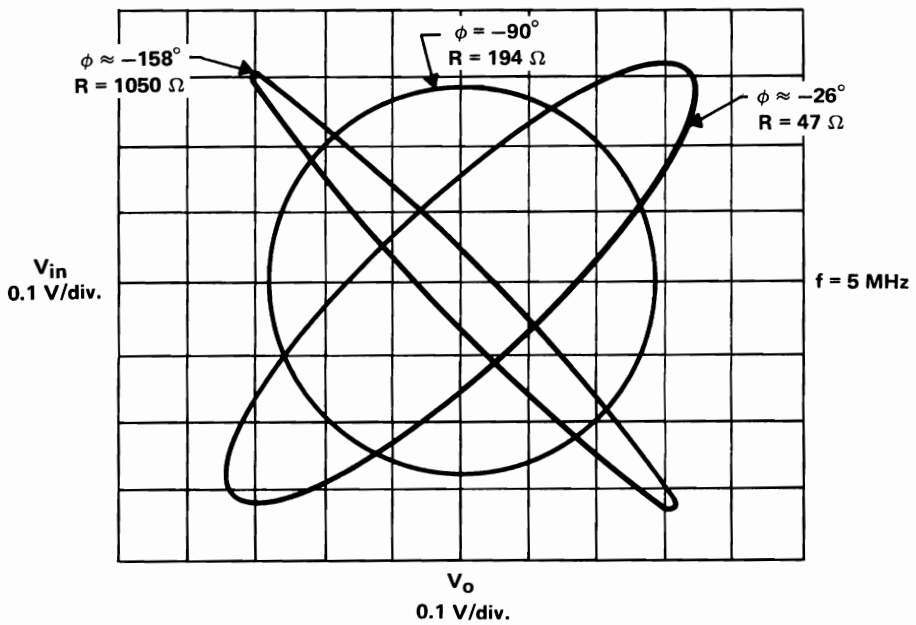


Figure 4.14. Input-Output Relationship of the Circuit in Figure 4.13

In examining the output amplitude as a function of the phase shift, note that it is not constant, contrary to the foregoing calculations, the reason being in part that the internal impedance of the signal generator was 50 ohms where it was considered to be zero. This circuit can be used to achieve phase modulation up to 50 MHz by replacing the resistor R with the drain and source of an FET which acts as a variable resistor, controlled by the voltage applied to its gate.

4.4.5 Fast Schmitt Trigger

Shaping of signals of various amplitudes and shapes to meet TTL levels can be achieved by integrated-circuit Schmitt triggers at frequencies up to 20 MHz. Beyond this frequency it is necessary to use fast triggers made from video amplifiers. Figure 4.15 shows an example of such a trigger, using an SN72733 and positive feedback realized from the resistor setup. The gain of the SN72733 was set at 100

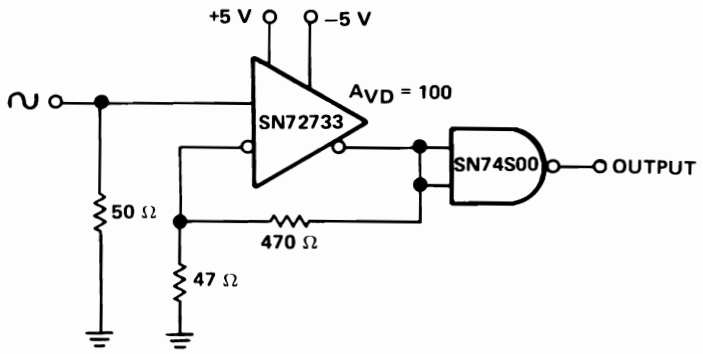


Figure 4.15. Fast Schmitt Trigger Using a Video Amplifier

for this experiment. The threshold voltage for the positive going input signal, 0.5 volt, is determined by the output voltage of the SN72733 divided by the feedback ratio. For a negative going signal, the threshold level is typically 0 volt. These thresholds can be seen in Figure 4.16 which shows the response of this circuit

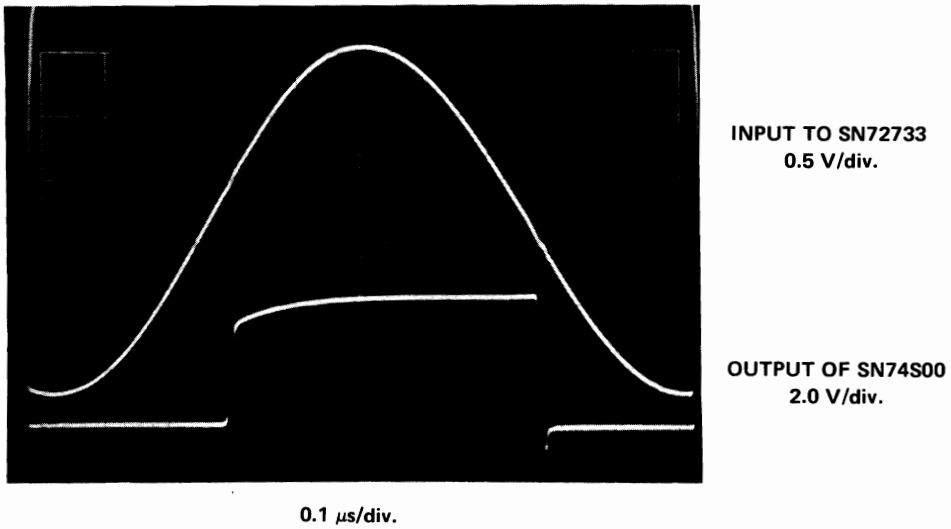


Figure 4.16. Signal Shaping at 1 MHz

to a 1-MHz sine-wave input signal. The upper curve in Figure 4.17 represents the output of the trigger circuit for an input signal of 20 MHz; the lower curve indicates the output for a signal of 50 MHz.

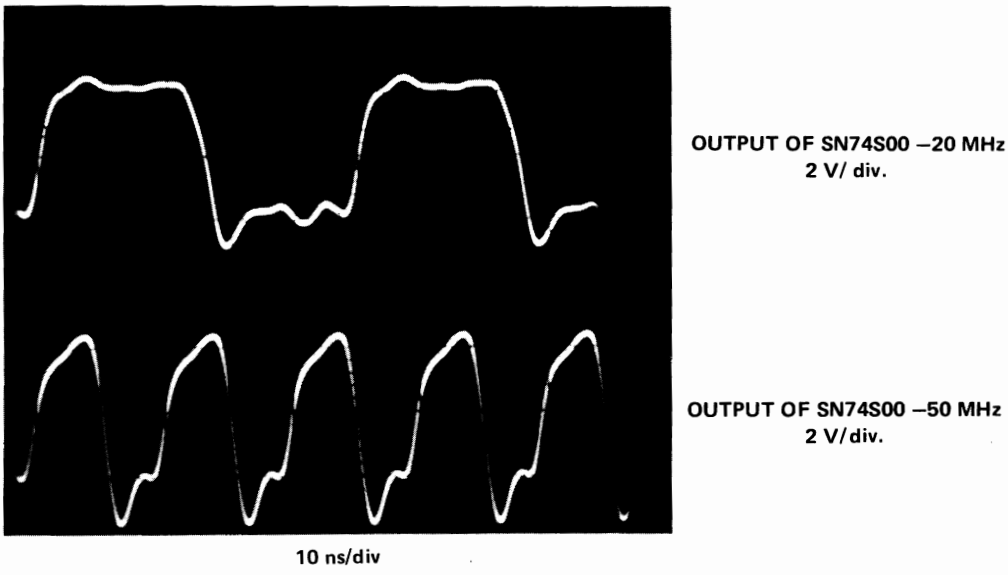


Figure 4.17. Signal Shaping at 20 and 50 MHz

4.4.6 Crystal Oscillator

Figure 4.18 shows an example of a crystal oscillator in which variable feedback is provided by a simple voltage-divider configuration of R1 and R2. The crystal precisely defines the operating frequency, since only at this frequency will significant feedback signal occur. The divider network can be used to adjust the feedback characteristic to provide an undistorted sinusoidal output. Since the SN7514 provides greater than 50-dB gain at frequencies up to 80 MHz, this network could be used to above 200 MHz in an oscillator circuit of this type.

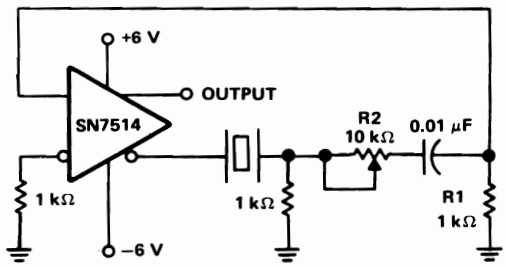


Figure 4.18. Crystal Oscillator with Variable Feedback

5

Voltage Regulators

5.1 GENERAL DESCRIPTION

A voltage regulator will generally consist of five main elements: (1) A reference element providing a known stable level. (2) A sampling element to sample the level of output voltage. (3) A comparator element for comparing the output sample with the reference and furnishing an error voltage, which is effectively $V_{REF} - V_O$. (4) An error amplifier used to amplify any error and furnish drive to the control element for correcting the error. And (5) a control element, which may be a shunt control (Figure 5.1a) or a series control (Figure 5.1b). The most popular type of

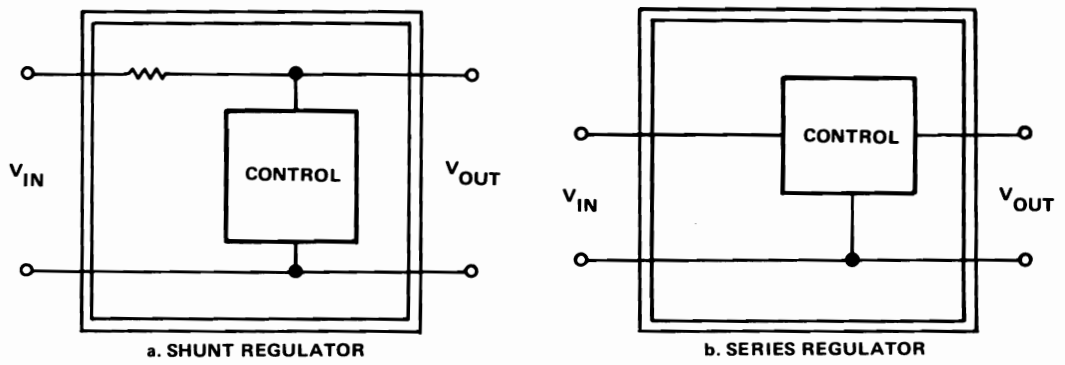


Figure 5.1. Basic Types of Voltage Regulators

integrated-circuit voltage regulator is the series regulator a block diagram of which is shown in Figure 5.2.

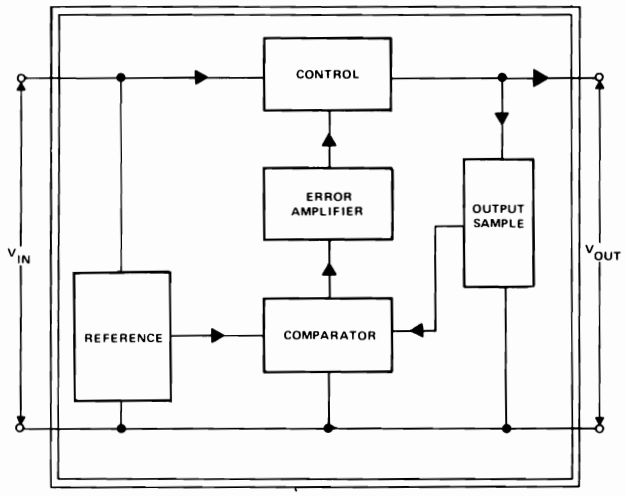


Figure 5.2. Block Diagram of Basic Series Voltage Regulator

The basic function of an integrated-circuit voltage regulator is to provide a fixed, stable dc voltage output despite changes in load current and input voltage.

Terms used to describe the performance of voltage regulators are defined as follows:

- *Input Regulation* — The percentage change in the output voltage for a change in input voltage from one level to another.

$$\text{Input Regulation} = \left[\frac{\Delta V_O}{V_O}\right] 100\%$$

where V_O is the output voltage at the ideal operating input voltage.

- *Ripple Rejection* — The ratio of the peak-to-peak input ripple voltage to the peak-to-peak output ripple voltage, expressed in dB.
- *Load Regulation* — The percentage change in the output voltage for a change in output current from one level to another.

$$\text{Load Regulation} = \left[\frac{V_O \text{ at } I_{O(2)} - V_O \text{ at } I_{O(1)}}{V_O \text{ at } I_{O(1)}}\right] 100\%$$

where $I_{O(1)}$ and $I_{O(2)}$ are the specified low and high currents respectively.

- *Average Temperature Coefficient of Output Voltage* (αV_O) — The ratio of the change in output voltage to the change in free-air temperature, expressed in percent per °C. This is an average value for the specified temperature range.

$$\alpha V_O = \left[\frac{V_O \text{ at } T_{A(2)} - V_O \text{ at } T_{A(1)}}{V_O \text{ at } 25°C} \right] \frac{100\%}{T_{A(2)} - T_{A(1)}}$$

Parameters and operating limits of popular device types are listed in Table 5.1.

Table 5.1. Voltage Regulator Selection Guide

PARAMETER	SN72304	SN72305	SN72305A	SN72309	SN72376	SN72723	UNIT
Input Voltage, Min	−8	8	8.5	7	9	9.5	V
Input Voltage, Max	−40	40	50	25	40	40	V
Output Voltage, Min	−0.035	4.5	4.5	5.0 Nom	5	2	V
Output Voltage, Max	−30	30	40		37	37	V
Input-to-Output Voltage Difference, Min	−0.5	3	3	2	3	3	V
Output Current, Max	20	12	45	500	25	150	mA
Input Regulation, Max	0.1%	0.06%/V	0.06%/V	50 mV	0.06%	0.3%	
Ripple Rejection, Min				85†		74†	dB
Ripple Sensitivity, Max	1 mV/V	0.01 %/V	0.003 %/V†				
Load Regulation, Max	5 mV	0.1%	0.4%	50 mV	0.5%	0.6%	
Standby Current, Max	5	2	2	10	2.5	4	mA

†Typical value at 25°C

5.2 FIXED POSITIVE-VOLTAGE REGULATORS

5.2.1 Basic 5-Volt Regulation with the SN72309

The SN72309 is a basic easy-to-use, three-terminal, 5-volt fixed-voltage regulator. The output-sampling, reference, comparator, error-amplifier, and control elements are internally connected, leaving only three external connections. The device is furnished in the LA metal-can package for convenient use in both plug-in and PC-board applications. Figure 5.3 shows the connections required for a fixed +5-volt regulator application.

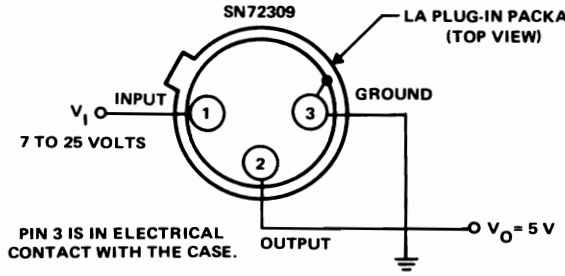


Figure 5.3. Basic 5-Volt Regulator

5.2.2 Regulation of Other Voltages with the SN72309

The output of the SN72309 is internally regulated at 5 volts above pin 3, the ground terminal. By referencing pin 3 to a level other than ground, regulation of voltages other than +5 volts can be accomplished. Figures 5.4a and 5.4b show examples of regulation of higher and lower voltages respectively. In Figure 5.4a the ratio of R1 and R2 was selected to yield a V_G of +7 volts for the desired output voltage of +12 volts. It is important to remember that the 5-mA bias current from pin 3 must be included in the calculations.

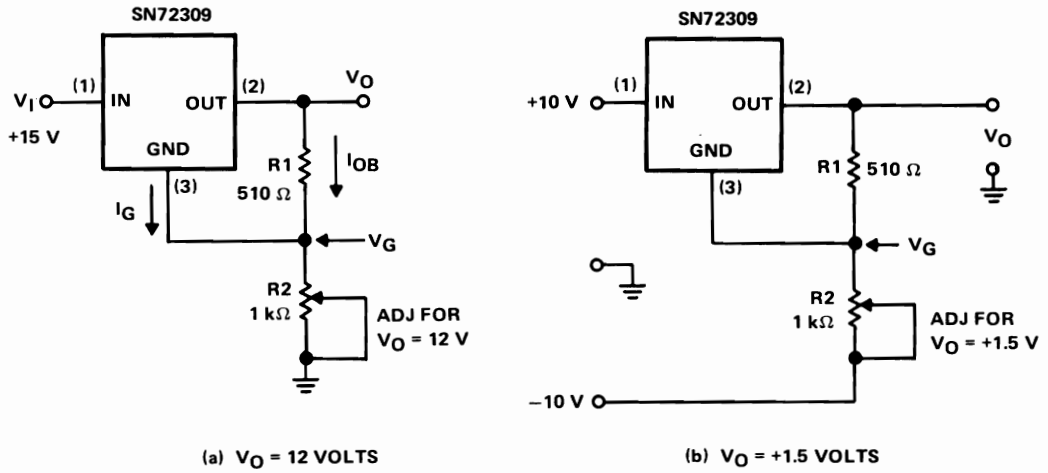


Figure 5.4. Regulation of Higher and Lower Voltages with the SN72309

The approximate value of R2 is $V_G/(I_G + I_{OB})$ where V_G must be $V_O - 5$ volts, or 7 volts. I_G, the device bias current, is 5 mA, and I_{OB} is the output bias current, selected in this case to be 10 mA. Therefore R2 = 7 V/15 mA $\approx$467 ohms. A 1000-ohm variable resistor may be used for adjusting V_O to exactly +12 volts. The voltage across R1 is regulated at +5 volts; therefore R1 = 5 V/10 mA = 500 ohms. A standard-value resistor of 510 ohms would be used.

If an accurate lower voltage supply is required the circuit of Figure 5.4b might be used. In this example a regulated output voltage of +1.5 volts is obtained from input voltages of plus and minus 10 volts. The output voltage is again determined by setting $V_G = V_O - 5$ volts, making $V_G = -3.5$ volts. Assuming the same bias-current conditions as before, R2 = 6.5 V/15 mA = 433 ohms. A 1000-ohm variable resistor could be used in this application also. R1 would be 510 ohms, as previously shown.

The load regulation of the SN72309 is within 50 mV for output loads of 5 mA to 50 mA. The loop gain of the feedback circuit can be increased as shown in Figure 5.5 to obtain even better load regulation, and also an adjustable output voltage. Regulation to within 10 mV for a 10-volt output, over an operating range of 5 mA to 50 mA, is possible.

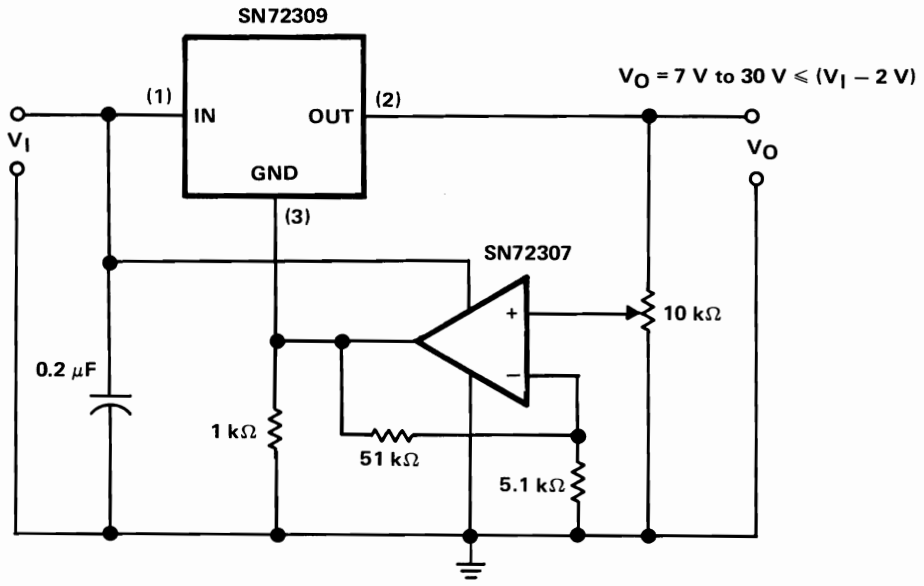


Figure 5.5. Highly Stable Adjustable-Output Voltage Regulator

5.3 NEGATIVE-VOLTAGE REGULATORS

5.3.1 Basic Negative-Voltage Regulator

The SN72304 is a negative-voltage regulator with an output voltage range of −40 volts to approximately 0 volts that can be programmed with a single external resistor. Access to the output-adjustment, reference, reference-supply, compensation, current-limit, and booster-output terminals (see Figure 5.6) makes the SN72304 type regulators very versatile. Although this type is designed primarily for application as a linear series regulator with 25-mA output capability, it can be used as a current regulator, switching regulator, or a control for high-current regulator applications. The SN72304 may also be used in constant-current and fold-back current-limiting applications.

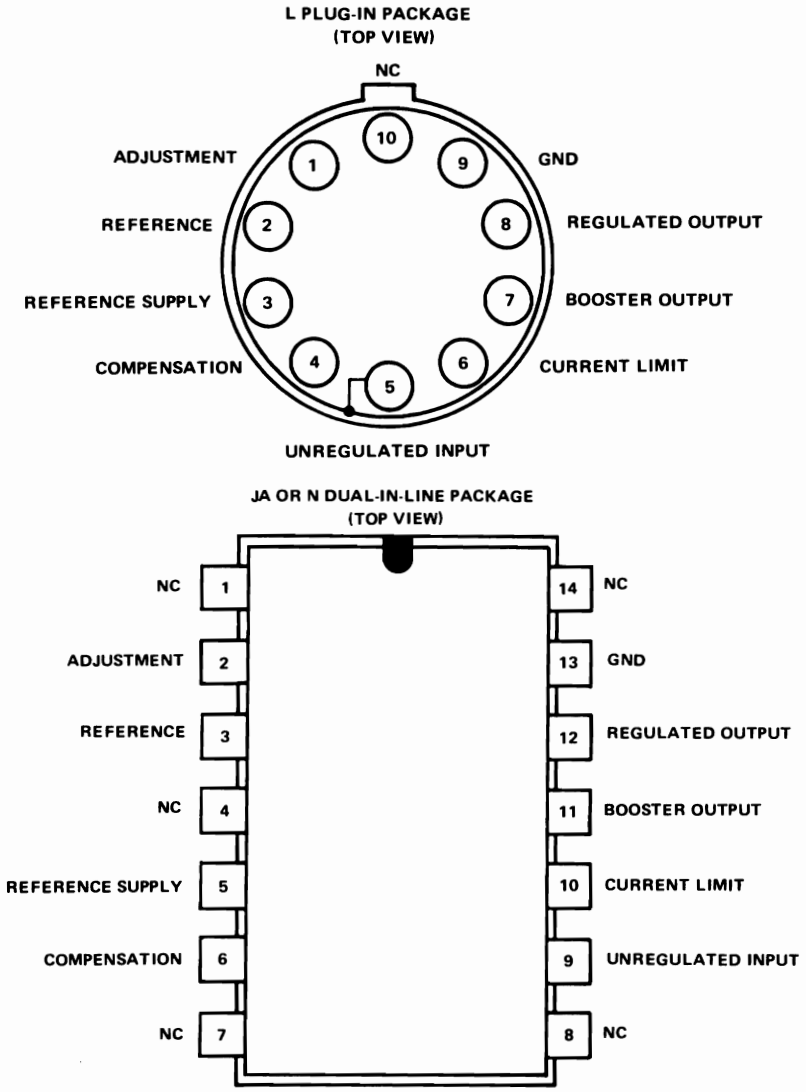


Figure 5.6. SN72304 Package Pin-Outs

The basic application in Figure 5.7 is a −30-volt regulator operating from a −40-volt source. The output voltage is proportional to R2, with the proportionality constant (scale factor) determined by R1. For R1 = 2.4 kΩ as shown, the output-voltage scale factor is 2 V/kΩ; that is, the output voltage will be 2 volts for each 1000 ohms of R2. In this example R2 = 15 kΩ and V_O is therefore 30 volts.

Short-circuit protection is set by resistor R_{CL} connected between the current-limit terminal and the unregulated input. Its value is selected to yield 300 mV at the desired current limit. In this example the desired cutoff is 15 mA; therefore the current-limit resistor R_{CL} = 300 mV/15 mA = 20 ohms.

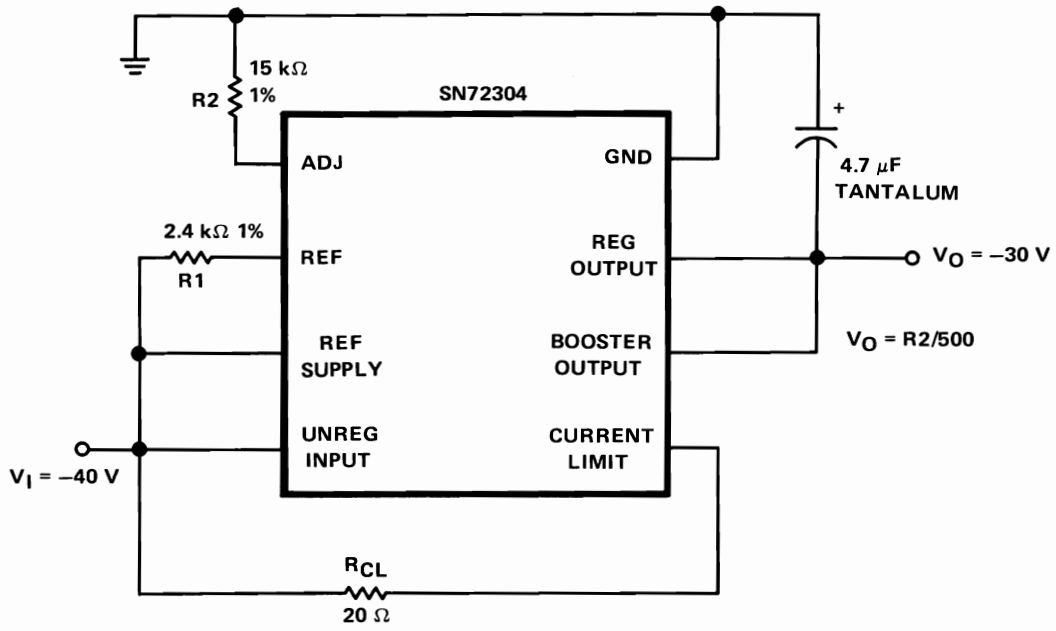


Figure 5.7. Basic −30-V Regulator

5.3.2 High-Current Regulator

For applications requiring currents greater than 25 mA, external boost transistors may be used with the SN72304 as seen in Figure 5.8. In addition to the current requirement power dissipation must also be considered when selecting boost transistors. For the application shown in Figure 5.8 the selected current limit is 2 amps, with $V_I = -20$ volts and $V_O = -15$ volts. The external pass transistor must dissipate power as high as $(V_I - V_O)I_O$, or 10 watts. To minimize the SN72304 output-current requirements and provide adequate output-current and power-handling capabilities, a TIP125 PNP Darlington-connected silicon power transistor is used as the booster. R_{ADJ} is set at 7.5 kΩ to achieve the −15 volt output level, and R_{CL} = 300 mV/2A = 0.15 ohm. A 10-μF tantalum capacitor connected to the output provides adequate stability and noise reduction.

5.4 POSITIVE-VOLTAGE REGULATORS

5.4.1 Basic Positive-Voltage Regulator

For positive-voltage applications, the SN72305A and SN72376 (Figure 5.9) provide performance and current capabilities equivalent to the SN72304. The SN72305 types also provide access to the booster-output, current-limit, compensation/shutdown, feedback, and reference-bypass terminals.

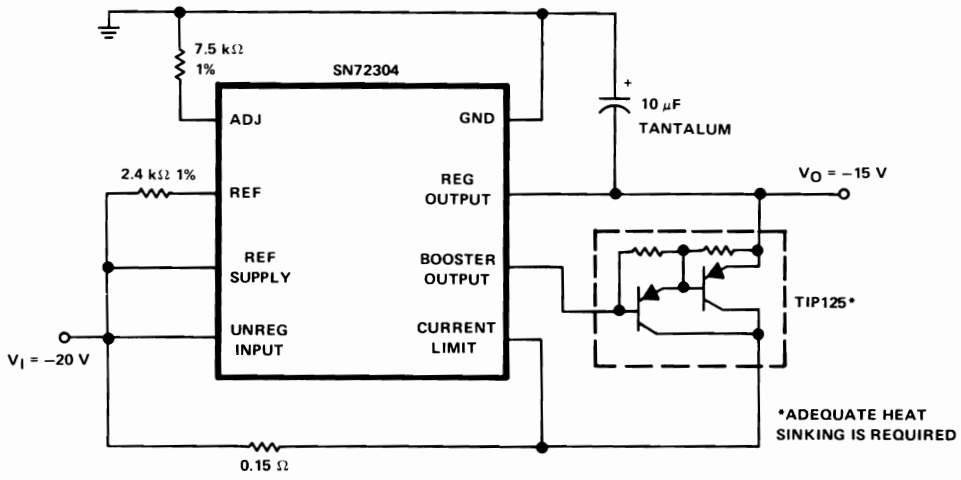


Figure 5.8. A 2-Amp −15-V Regulator

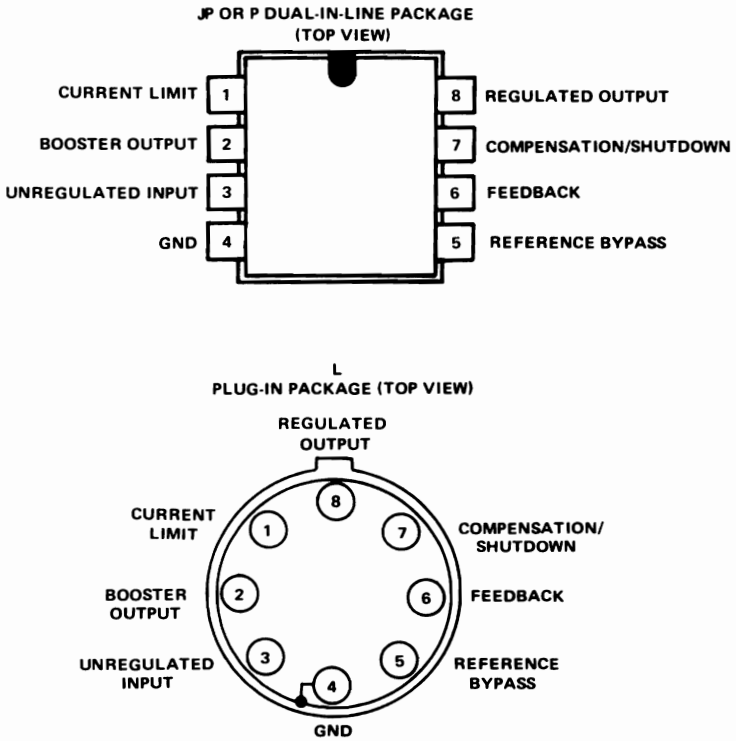


Figure 5.9. SN72305, SN72305A, and SN72376 Package Pin-Outs

A basic regulator circuit is shown in Figure 5.10. For this application the selected parameters were the input voltage (15 volts), output voltage (12 volts), and output current (10 mA max.). The feedback sense voltage, typically 1.7 volts, is an internally set level around which the feedback (output sample) signal must operate. The output voltage V_O is therefore controlled by the sampling network R1 and R2. The values of these resistors are related to the sample bias current I_{SB} by the following equations: R2 = 1.7 V/I_{SB} and R1 = (V_O − 1.7 V)/I_{SB}. If V_O is 12 volts, R1 = 10.3 V/I_{SB}. I_{SB} should be about 1 mA, making 10 kΩ an obvious choice for R1. Therefore I_{SB} is 1.03 mA and R2 is 1.65 kΩ. The 47-pF capacitor between the feedback terminal (pin 6) and the compensation/shutdown terminal (pin 7) provides high-frequency filtering to eliminate possible oscillations. The reference bypass, which is connected on the other side of the internal differential amplifier, also adds to the stability of the circuit and reduces any noise that might be generated by the internal reference supply. If the booster output is not being used, as in this basic application, it is connected directly to the unregulated input terminal (pin 3). The output short-circuit control (pin 1) has an input threshold of 325 mV. For current limiting (or short-circuit protection) the resistor R_{SC} is simply 325 mV/$I_{O(max)}$. In this example R_{SC} = 325 mV/10 mA = 32.5 ohms. A close standard value would be 33 ohms as shown.

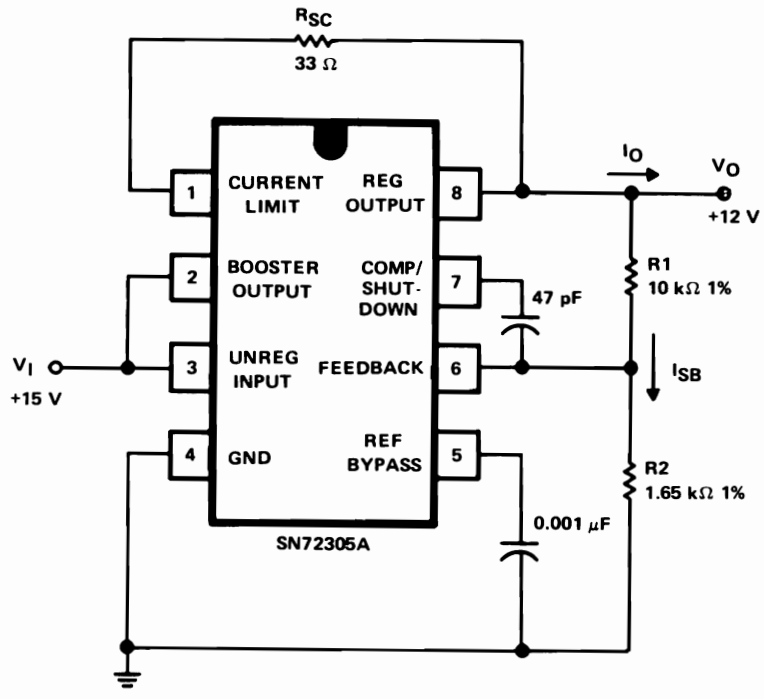


Figure 5.10. Basic Positive-Voltage Regulator with Short-Circuit Protection

5.4.2 Fold-Back Current Limiting

For high-current applications requiring an external boost transistor, it is important to check the power requirements under overload conditions. Even with the current-limit resistor in place a short or low-impedance load may result in very high power dissipation in the external series pass transistor as well as the regulator. Fold-back current limiting is a technique designed to reduce both the output voltage and the output current under overload conditions, thus greatly reducing the power dissipation.

A voltage regulator with high output current capability employing fold-back current limiting is shown in Figure 5.11. Operating from an unregulated +18-volt source this regulator must furnish up to 200 mA at V_O = +15 volts. R3 is the current-limit resistor; R1 and R2 form the output sampling network developing the feedback voltage as in the basic circuit. R4 and R5 have been added to produce the fold-back characteristic. R3 does not connect directly to pin 1 (current-limit input) but is connected through R4. The voltage across R4 opposes that across R3, requiring a higher voltage to be developed across R3 before limiting begins. As the output voltage during a short begins to decrease, the opposition from R4 decreases.

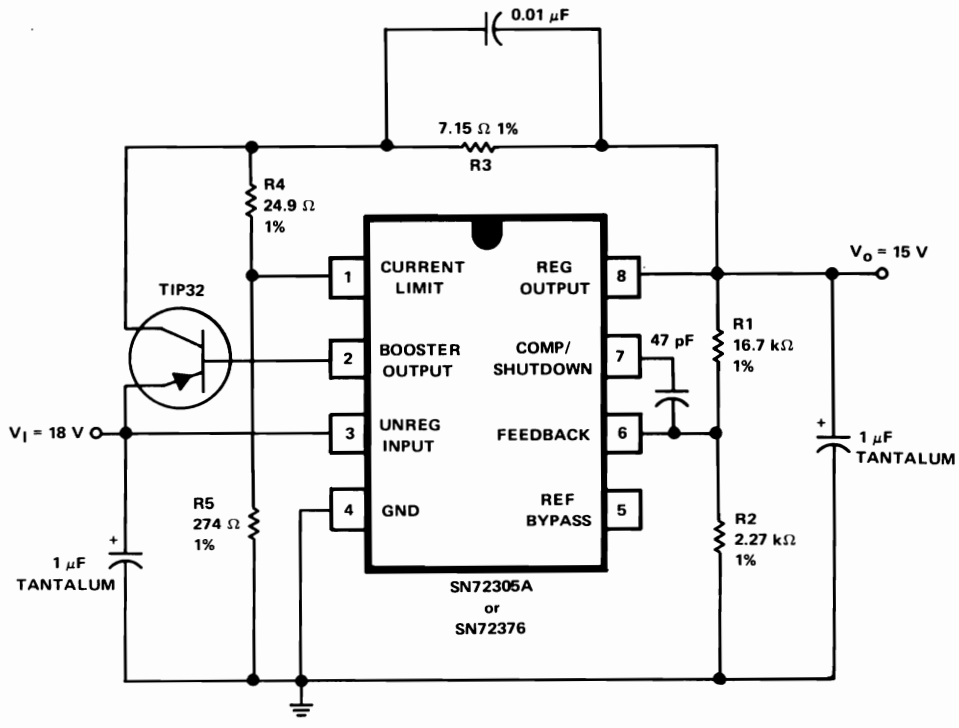


Figure 5.11. Linear Regulator with Fold-Back Current Limiting

In the *shorted condition* the output current is reduced to $I_{SC} = V_{SR3}/R3$ where V_{SR3} is the short-circuit current-limit sense voltage across R3. This voltage is the voltage drop across the current-limit resistor (R3) required to initiate current limiting. Figure 12 is a plot of V_{SR3}, with the output shorted, versus device junction temperature. For this application a maximum junction temperature of 70°C is chosen; therefore V_{SR3} is 0.36 volt. For most fold-back applications it is desirable that the short-circuit current I_{SC} be about 25% of $I_{O(max)}$. In this application $I_{O(max)}$ is 200 mA, and therefore I_{SC} would be about 50 mA. R3 is then equal to V_{SR3}/I_{SC} = 0.36 V/50 mA = 7.2 ohms.

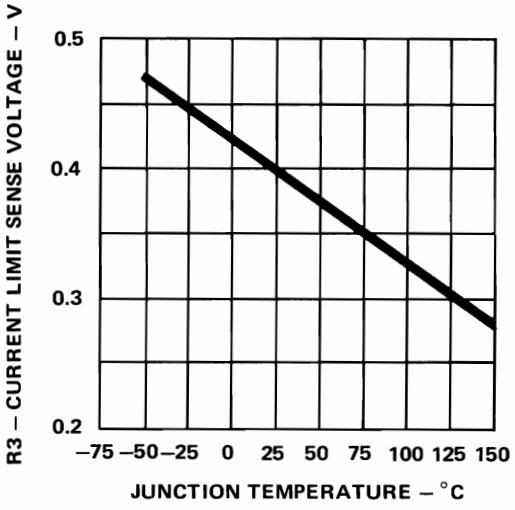


Figure 5.12. Voltage Drop Across Current-Limit Resistor V_{SR3} Required to Initiate Current Limiting

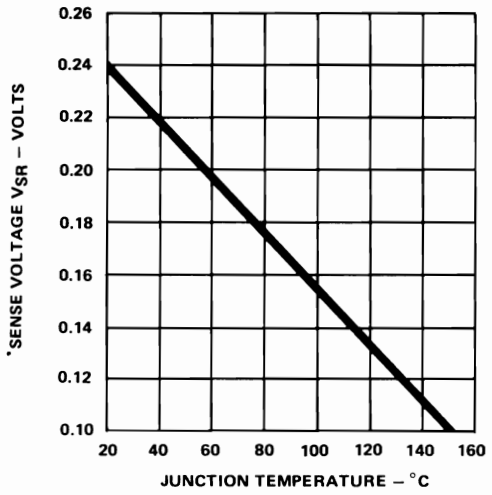


Figure 5.13. Maximum Sense Voltage at Full Load for 0.1% Worst-Case Load Regulation

The value for resistor R5 is determined as follows: $R5 = (V_O + V_{SR})/(I_B + I_D)$ where V_O is the regulated output voltage. V_{SR} is the sense voltage across R3 at full load for a worst-case output regulation of 0.1%, as taken from Figure 5.13. I_B is the bias current from the current-limit pin, and is equal to 2 mA plus the maximum base drive required for the external boost transistor. I_D is the current for the divider network (R4 and R5), and is equal to about 10 I_B.

In the example V_O = 15 volts; V_{SR} at the selected junction temperature of 70°C is 0.19 volt; $I_B = 2\text{ mA} + I_{O(max)}/h_{FE}$ where $I_{O(max)}$ is 200 mA and h_{FE} for the TIP32 may be as low as 70 at this current, and thus I_B = 2 mA + 200 mA/70 = 2 mA + 2.86 mA, or $I_B \approx 5$ mA. I_D is therefore 50 mA. It follows then that R5 = (15 V + 0.19 V)/(5 mA + 50 mA) = 0.276 kΩ. A close standard 1% value is 274 ohms.

R4 is expressed as $R4 = (I_{O(max)}\ R3 - V_{SR})/I_D$. Substituting the already determined values, R4 = [(200 mA)(7.15 Ω) − 0.19 V]/50 mA or R4 = 24.8 ohms, or 24.9 ohms for the nearest 1% value.

The addition of a 0.01-μF capacitor across the sense resistor will aid in preventing oscillations and undesirable effects from high-speed transients. With the use of fold-back current limiting, overall reliability is increased due to the reduction in power dissipation during output short-circuit conditions.

5.4.3 Dual Tracking Regulator

Although structured somewhat differently, the SN72305A and SN72304 may be combined to provide an accurate ±12-volt dual tracking regulator (Figure 5.14). Tracking is accomplished by connecting the feedback control point of the SN72305A to the adjust terminal of the SN72304 with resistor R2. R1 and R2 form a sampling network affecting both supplies.

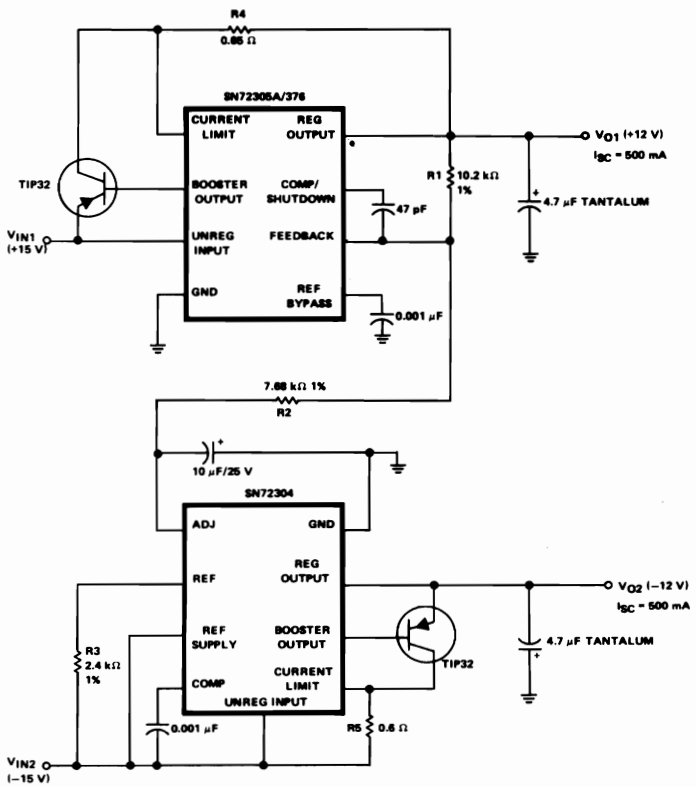


Figure 5.14. Dual Tracking Regulator

The feedback sense voltage V_{FS} of the SN72305A is 1.7 volts. A 1-mA interface current through R1 and R2 is established by the 2.4-kΩ reference-terminating resistor of the SN72304. The voltage at the SN72304 adjust terminal is $V_{O2}/2$, or −6 volts in this example. R2 = $(V_{FS} - V_{ADJ})/1$ mA or $[-1.7\text{ V} - (-6\text{ V})]/1$ mA. Therefore R2 = 7.7 kΩ, and a 7.68-kΩ standard 1% value is selected. R1 = $(V_{O1} - V_{FS})/1$ mA or $(12\text{ V} - 1.7\text{ V})/1$ mA. Therefore R1 = 10.3 kΩ and a standard 1% value of 10.2 kΩ is selected.

In this regulator a variation in either output voltage will result in a change in the other. Output voltage versus load current, and tracking results, are plotted in Figure 5.15. Short-circuit limits for the output current are set at 500 mA by R4 and R5.

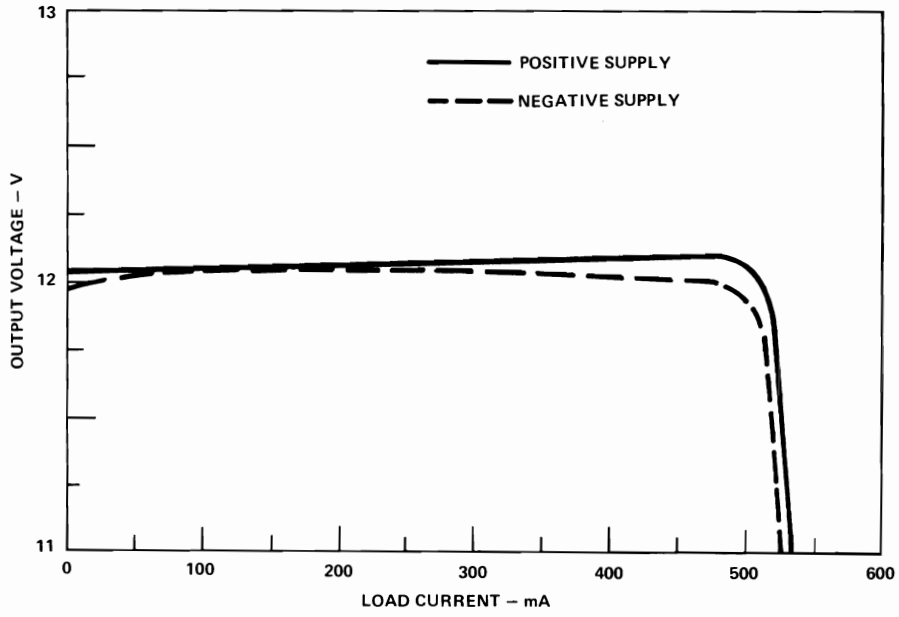


Figure 5.15. Output Characteristics of the Dual Tracking Regulator

5.5 SN72723 PRECISION VOLTAGE REGULATOR

5.5.1 Description

Its many features make the SN72723 a versatile and popular voltage regulator. These features include: high output current capability (150 mA); 0.01% typical input regulation; 74 dB typical ripple rejection; 0.03% typical load rejection; and a wide output range of 2 to 37 volts.

Figure 5.16 shows the package pin-outs and the functional block diagram of this device. The SN72723 was designed for use in positive and negative power supplies as a series or shunt regulator, and can also be utilized in switching and floating regulator applications.

The functional block diagram of Figure 5.16 indicates the variety of functions incorporated in this device. Internal functions include a temperature-compensated voltage source; an error amplifier with access to its inverting input, non-inverting input, and output terminals; a 150-mA series pass transistor; an adjustable current limiter; and a 6.2-volt zener for use in floating or negative voltage regulator applications.

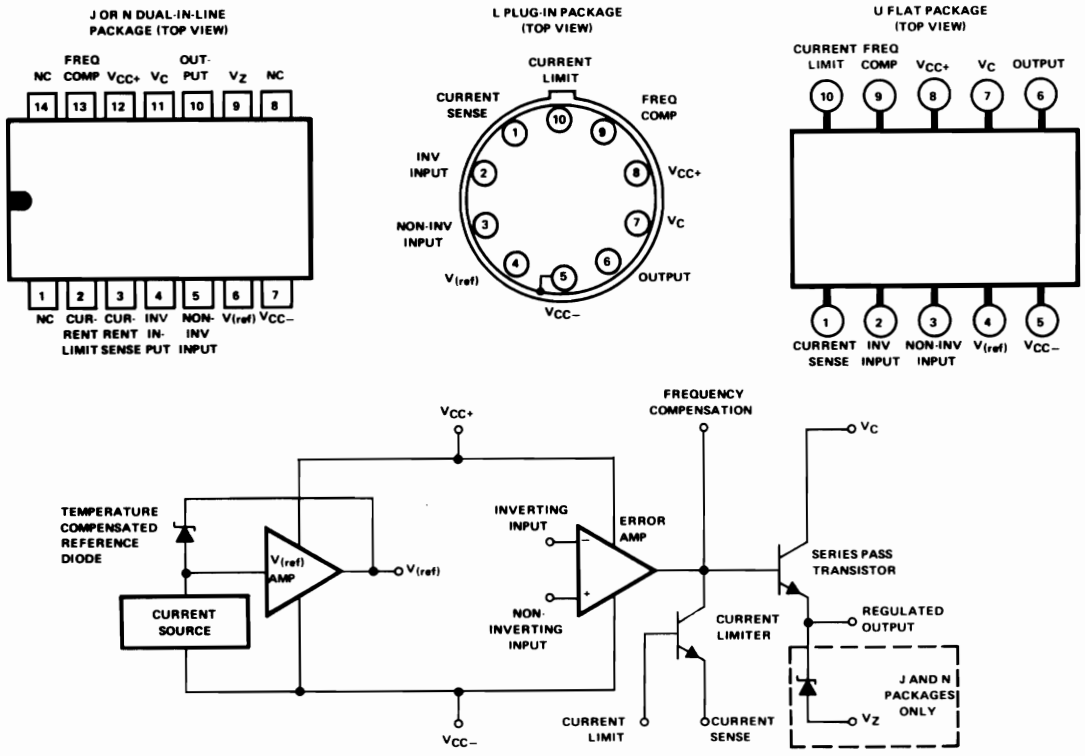


Figure 5.16. SN72723 Package Pin-Outs and Functional Block Diagram

5.5.2 Basic SN72723 Regulator Applications

Setting of the output voltage in the basic regulator application is accomplished with a simple voltage-divider network, the placement of which is determined by the desired voltage. Since there is an internal 7.1-volt reference supply, $V_{(ref)}$ is divided for output voltages of less than 7 volts. Figure 5.17 shows a 5-volt regulator, with R1 and R2 forming a divider network to yield a 5-volt reference voltage V_{NI}. $R2 = V_{NI}/I_B$ where I_B is the divider-network bias current. With the recommended I_B of 1 mA, R2 is a 4.99-kΩ, 1% resistor. $R1 = [V_{(ref)} - V_{NI}]/I_B$ or 2.1 kΩ, 1%.

In any normal current-limiting function the short-circuit protection resistor is equal to 0.65 volt divided by the desired short-circuit current limit I_{SC}. For the I_{SC} of 100 mA in this application R_{SC} is 6.5 ohms. R3 is used for balancing the impedances seen by the error-amplifier inputs, for improved stability and accuracy. Therefore R3 = R1R2/(R1 + R2); a 1.47-kΩ standard 1% value would be used.

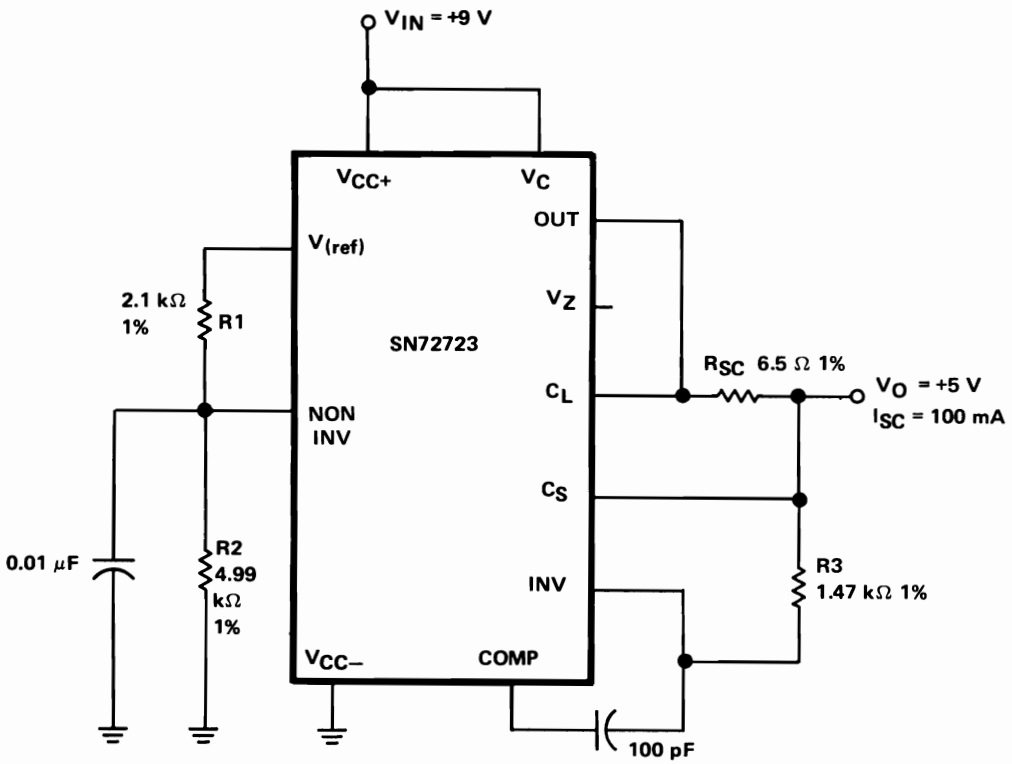


Figure 5.17. Basic SN72723 Regulator for Voltages Less Than 7 Volts

In the example in Figure 5.18 the desired output of 15 volts is greater than $V_{(ref)}$, and the divider network is connected between the output and ground to provide 7.1 volts at the inverting input of the error amplifier. The internal $V_{(ref)}$ of 7.1 volts is connected to the non-inverting input through R3. $R2 = V_{(ref)}/I_B$ = 7.1 V/1 mA or 7.1 kΩ; a standard 7.15-kΩ resistor is used. $R1 = [V_O - V_{(ref)}]/I_B$ = 7.9 kΩ, and a standard 1% value of 7.87 kΩ is used. As in the previous example, R_{SC} is 6.5 ohms for current limiting at 100 mA, and the impedance-balance resistor R3 is again the parallel equivalent of R1 and R2, 3.74 kΩ being the nearest 1% resistor value.

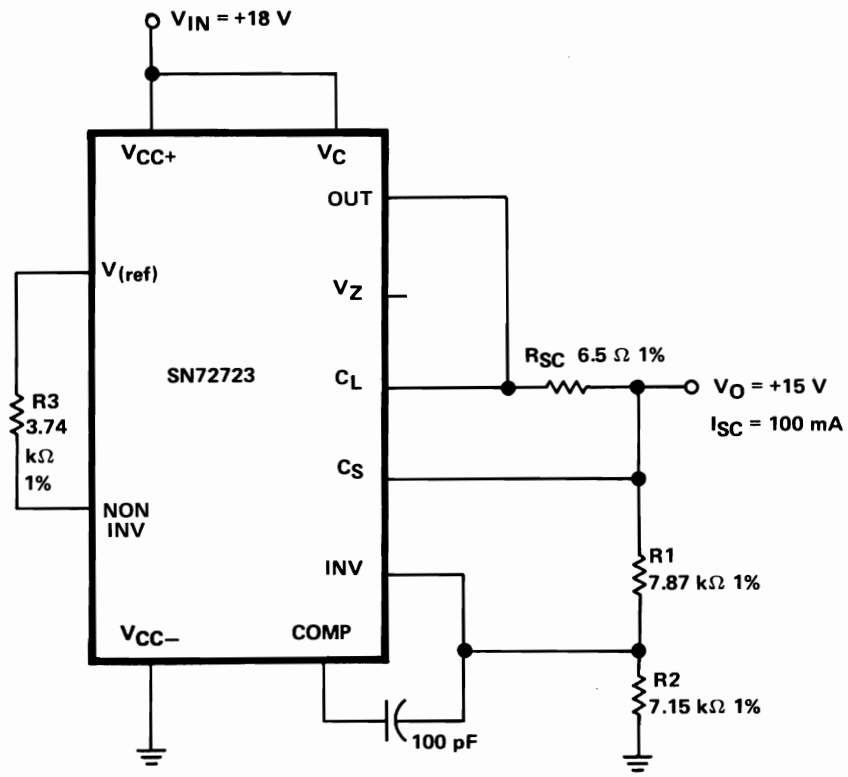


Figure 5.18. Basic SN72723 Regulator for Voltages Greater Than 7 Volts

5.5.3 Positive and Negative Regulators with Boost Outputs

Figures 5.19 and 5.20 show examples of positive and negative voltage regulation using external pass transistors. For positive voltages (Figure 5.19) the addition of an NPN pass transistor allows handling higher load current, with little change from the basic circuit of Figure 5.18.

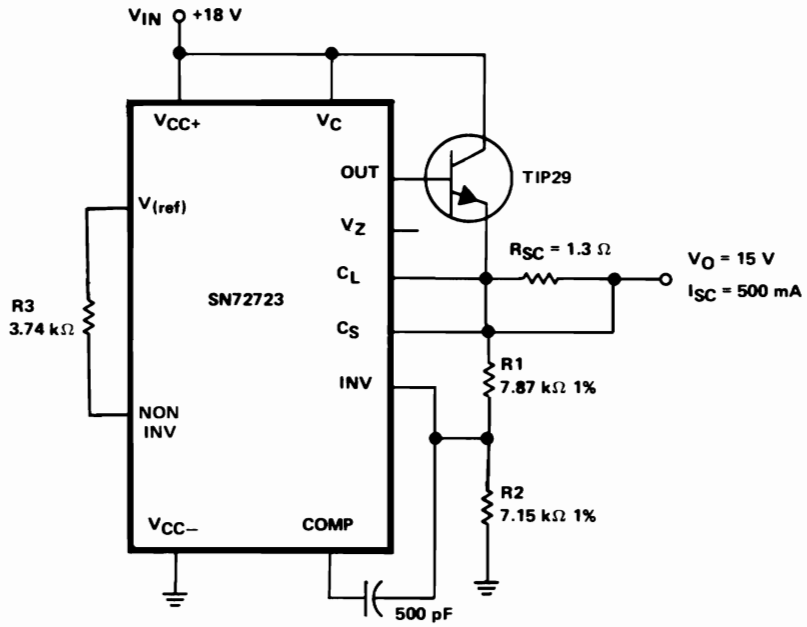


Figure 5.19. Basic Positive Regulator with Boost Output

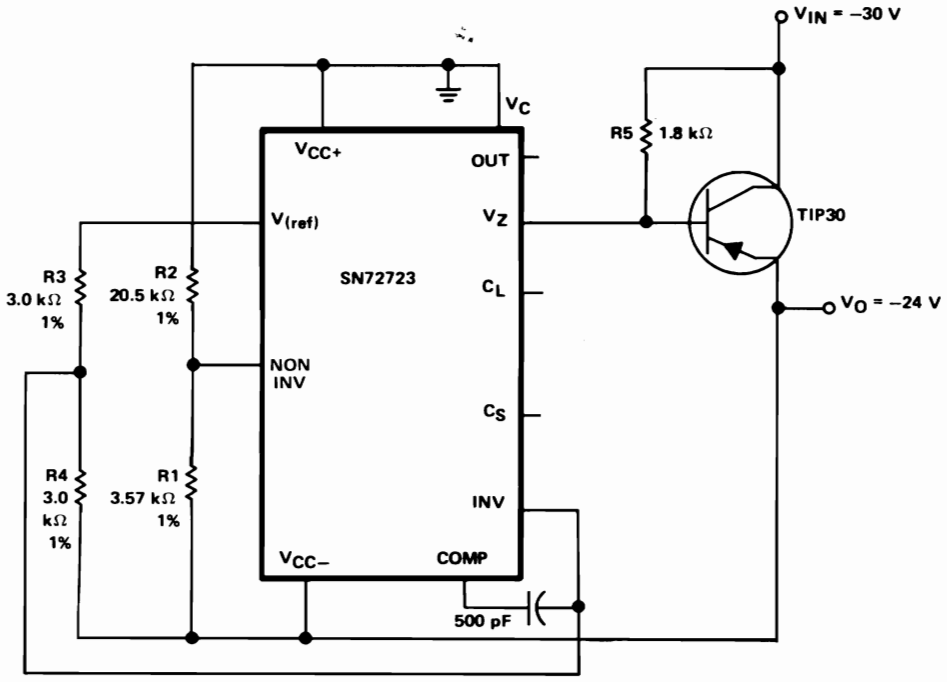


Figure 5.20. Basic Negative Regulator with Boost Output

A PNP pass transistor is utilized in Figure 5.20 for negative voltage regulation. Note that in this configuration the difference between the V_{CC+} and V_{CC-} terminals should not be less than 9 volts or greater than 40 volts.

Level shifting through the internal zener and using the V_Z output provide up to 25 mA drive for the pass transistor. In this example a −24-volt output with up to 250 mA capability is desired. The TIP30 will provide adequate output capability while operating from a −30-volt source. The internal reference voltage (7.1 volts) of the SN72723 is referenced to the V_{CC-} terminal, thus making it equal to $(V_O + 7.1)$, or −16.9 volts with respect to ground.

Due to the effects of using the zener output it is desirable to reduce by one-half the common-mode voltage at the error-amplifier input (relative to V_O). A divider network consisting of equal-value resistors R3 and R4 (3 kΩ, 1%) results in a $V_{(ref)}$ output current of slightly more than 1 mA. The voltage at the inverting input of the error amplifier is therefore $[V_O - V_{(ref)}]/2$, or −20.45 volts.

An output sampling network consisting of R1 and R2 is connected between V_O and ground to provide the same −20.45-volt level to the non-inverting input of the error amplifier. With a bias current of about 1 mA, this level is established using the values shown.

The TIP30 pass transistor has an h_{FE} of 40 or greater, making the base drive requirement for 250 mA output approximately 6 mA. For good balance about half of the base drive is furnished from the V_Z output with the remainder from the base pull-up resistor R5.

The internal current-limiting function of the SN72723 is not directly applicable to the negative-voltage regulator configuration. If current limiting is required, conventional clamping of the TIP30 can be provided.

5.5.4 High-Voltage Applications

The SN72723 can also regulate relatively high voltages. One popular high-level voltage where gas regulators have been used is 105 volts. Figures 5.21 and 5.22 illustrate both negative- and positive-voltage applications at this level. The basic consideration is to maintain a relatively low voltage across the SN72723 while regulating the required high voltage. To accomplish this the regulator is allowed to operate (or float) between the desired V_O level and another voltage within the 40-volt operating range of the device. Thus these types of applications are referred to as positive or negative floating regulators.

Figure 5.21 shows a positive floating regulator with an output-current capability of 50 mA at +105 volts. Short-circuit current is limited at 50 mA by the 13-ohm resistor R_{SC}. Because the boost transistor must be capable of dissipating 2.5 watts

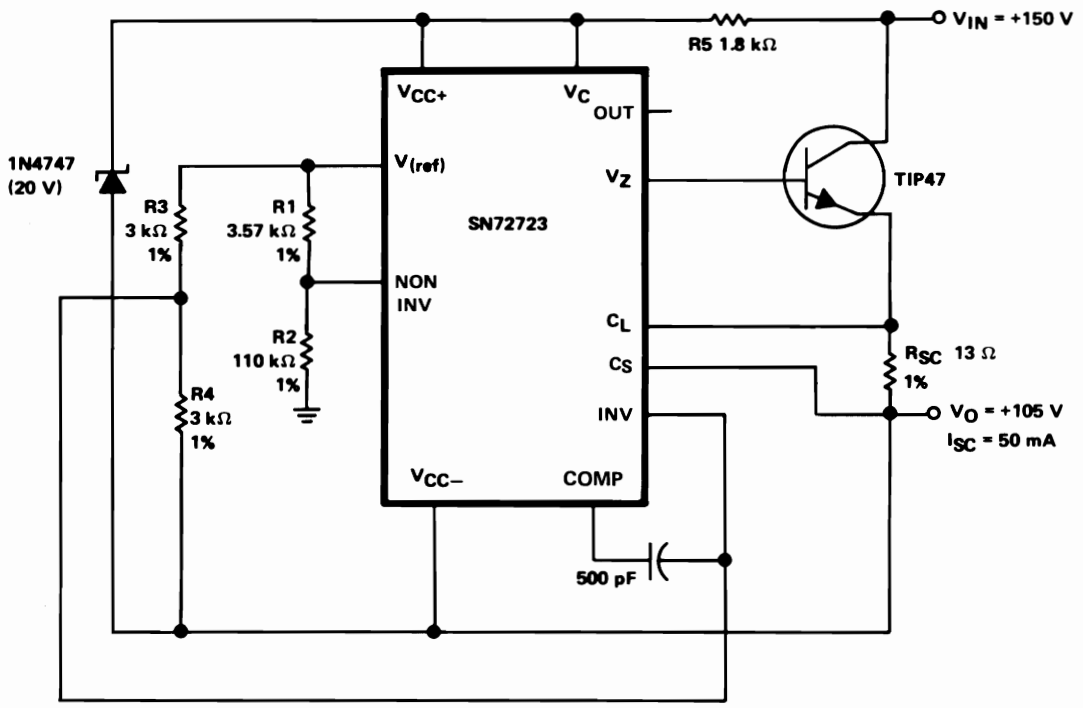


Figure 5.21. Positive 105-Volt Regulator

and operating from a 150-volt source, the TIP47, an economical plastic high-voltage power transistor, is selected for this application. R3 and R4 are used to reduce the reference voltage applied at the inverting input to $[V_O + V_{(ref)}]/2$, or 108.55 volts, with the 3-kΩ, 1% resistors resulting in a bias current of slightly over 1 mA.

The control input voltage at the non-inverting input is established with R1 and R2. Assuming the typical bias of 1 mA and a non-inverting input voltage V_{NI} of 108.55 volts (at balance), R2 ≈ 110 kΩ for the nearest 1% value. R1 = $[V_{(ref)}/2]/I_B$ or 3.57 kΩ for the nearest 1% value. With this bias arrangement any output change will result in a net change through the error amplifier that is in opposition to the output variation, thus correcting the output level. A 1N4747 20-volt zener is used to clamp the voltage between V_{CC+} and V_{CC-}, protecting the SN72723 from excessive voltage. R5 is selected to yield sufficient zener current and device bias currents. V_{CC+} is equal to V_O + 20 volts, or 125 volts. A total current level of about 14 mA is required; therefore R5 = (150 V − 125 V)/14 mA, or 1.8 kΩ.

Figure 5.22 shows a negative-voltage version of the 105-volt regulator. Calculation of the resistor values follows the same basic procedures used above. In this example a 1N759 12-volt zener is employed to clamp the voltage appearing across the floating regulator.

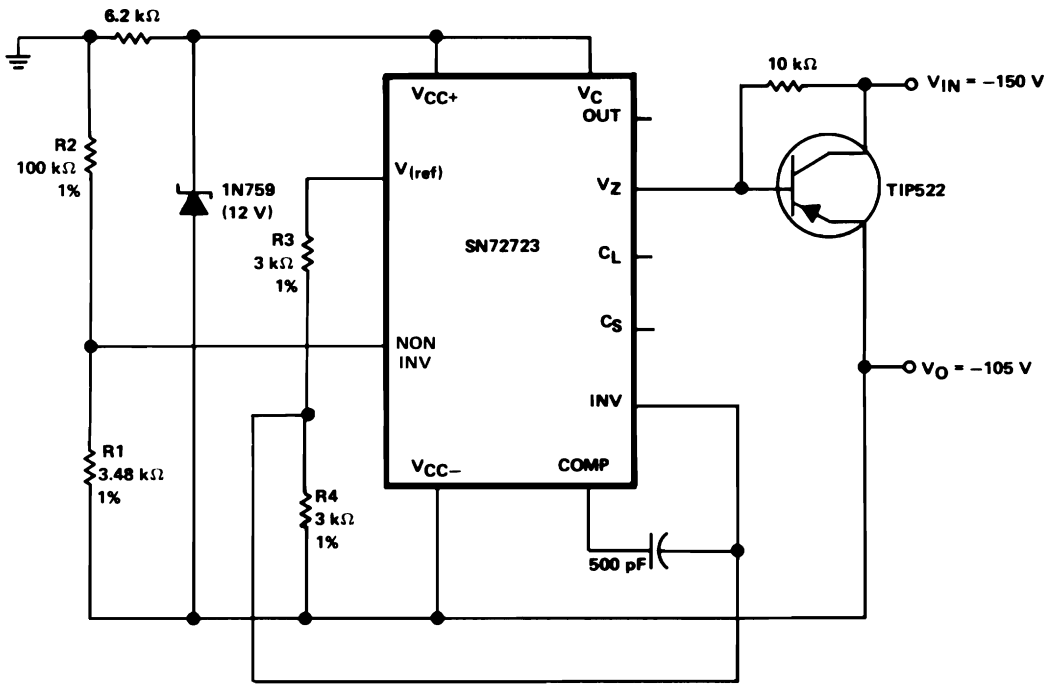


Figure 5.22. Negative 105-Volt Regulator

6

Special Functions

6.1 GENERAL

Numerous products were originally designed as custom circuits to fill specific applications. Many of these have evolved from this beginning into a full line or family of standard products, and most of the chapters in this book are concerned with particular family types. There are, however, several special functions that have become standard products but have not yet developed into large families of circuits. Discussion in this chapter is centered on these circuits and their applications: the SN72440 zero-voltage switch, SN72560 precision level detector, SN72555 precision timer, SN76502 logarithmic amplifier, and the SN76514 doubly balanced mixer.

6.2 SN72440 ZERO-VOLTAGE SWITCH

The SN72440 is a combination zero-voltage detector and pulse generator incorporating a comparator for threshold detection, a sawtooth generator, and an output driver. It is designed to provide gate drive to a triac or SCR in the form of pulses that occur only when the ac input signal crosses through zero volts. Thus the triac or SCR gate is fired while the line voltage is very low, minimizing undesirable turn-on transients and RFI. As a result the load receives complete half-wave or full-wave cycles of line voltage as opposed to partial cycles typical of phase-shift triac control circuits.

Figure 6.1 shows the functional block diagram of the SN72440. With its many built-in features, the SN72440 can be used either as an on-off control with or without hysteresis, or as a proportional control with the use of the internal sawtooth generator. Although the principal application of this device is in temperature control, it can be used for many power control applications such as photosensitive

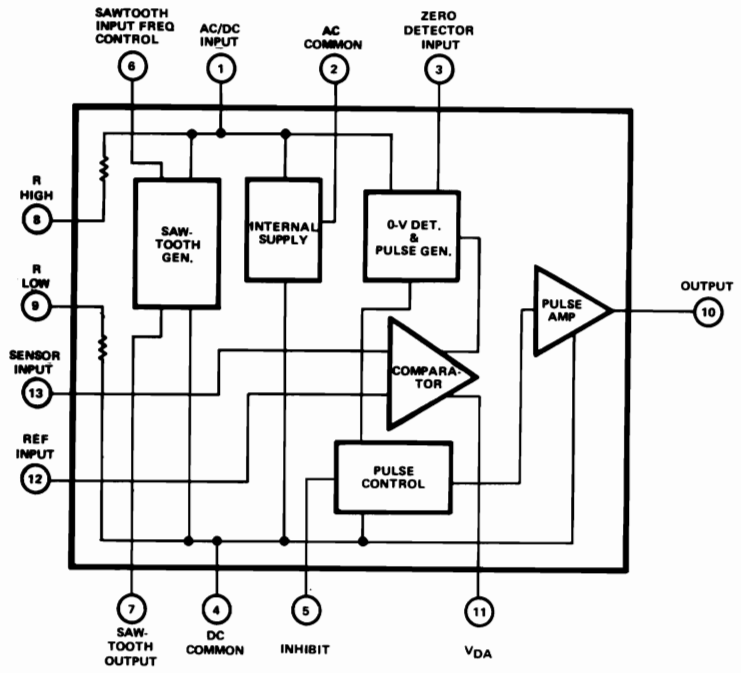


Figure 6.1. Block Diagram of the SN72440

controls, voltage level sensors, ac lamp flashers, small relay drivers, or miniature lamp drivers.

The inhibit function (pin 5) prevents output pulses from occurring when the applied voltage at the inhibit input is typically 1 volt or greater. Conversely, if the inhibit input is shorted to dc common (pin 4), an output pulse will be obtained for each zero-crossing of the ac power input waveform regardless of the sensor input conditions.

Internal resistors R_{high} and R_{low} are used to provide a V_{ref} of $V_{DC}/2$, or about 6 volts, for the comparator. The sensor input would then be biased to provide on-off control at the 6-volt level as bias is varied by an external sensor. The comparator output controls the zero-voltage detector and pulse generator. Resulting pulses are fed through the pulse-control and pulse-amplifier circuitry, providing triac or SCR gate drive at the output (pin 10).

For proportional control of the comparator and output pulses an internal sawtooth generator is provided. Internal bias establishes an input threshold level of about 67% of V_{DC} for the generator; therefore an RC network between pins 1 and 4 will drive pin 6 to provide a sawtooth with a frequency of about 1/RC.

A thermal probe (Figure 6.2) uses the SN72440 in a proportionally controlled power application, where the temperature of the probe, a 27-watt soldering iron, is maintained at a preset level. The probe temperature is sensed by a thermistor built into its tip. By adjusting the temperature to a desired level and applying the tip of the iron to a transistor, integrated circuit, resistor, or other component, individual reaction of the component to that temperature may be determined. With the temperature select control calibrated, it is possible to slowly raise the temperature of a component and easily determine the temperature at which it fails or changes characteristics.

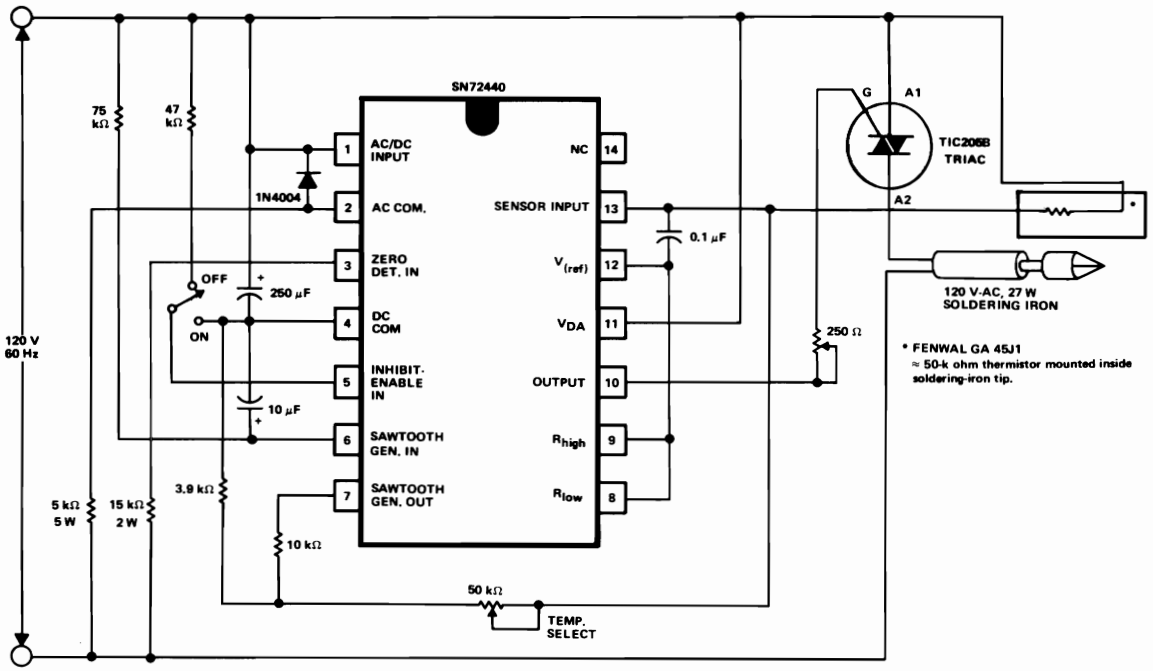


Figure 6.2. Thermal Probe Control Using the SN72440

6.3 SN72560 PRECISION LEVEL DETECTOR

6.3.1 Description

There are many types of level detectors and Schmitt-trigger circuits, but most have inputs similar to those of TTL circuitry. This precludes their use in high-impedance low-current applications such as timers and very low-frequency oscillators.

The SN72560 is a precision level detector intended for applications requiring a Schmitt-trigger function with high input impedance. The high input impedance of the SN72560 is characterized by its very low input bias requirement, typically 2 nA when below the positive-going threshold. This allows the use of large RC timing components to achieve long timing intervals. The device also features excellent voltage and temperature stability, and an externally adjustable internal reference for the threshold level. These characteristics make it an ideal interface between very low-frequency or high-impedance sources and logic systems.

The internal positive-going threshold is approximately 60% of the power-supply voltage over the supply voltage range of 2.5 to 7.0 volts. This is an interesting feature because the time required for charging to about 60% of the supply voltage is one RC time constant, making the time to the positive threshold very close to RC in seconds (with equal supply voltages for the timing circuit and the device). The low-level or negative-going threshold is about 0.6 volt, which results in the hysteresis characteristic seen in the basic transfer functions in Figure 6.3. The SN72560 was designed for dc or very low-frequency detection. For this reason the negative-going threshold and resulting hysteresis characteristic may be indeterminate in some switching applications.

The variation of threshold voltage with temperature for V_{CC} = 5 V is less than 4 mV/°C for V_{T+} and about 1.4 mV/°C for V_{T-} over the temperature range of 0 to 70°C.

The positive-going threshold is adjustable from approximately 0.6 volt to within about 0.6 volt of V_{CC}, using an external resistor connected from the reference terminal to ground or V_{CC}. The plot in Figure 6.4 shows a typical positive-going threshold versus different resistance values. Resistance from the reference terminal to ground should not be less than 200 ohms.

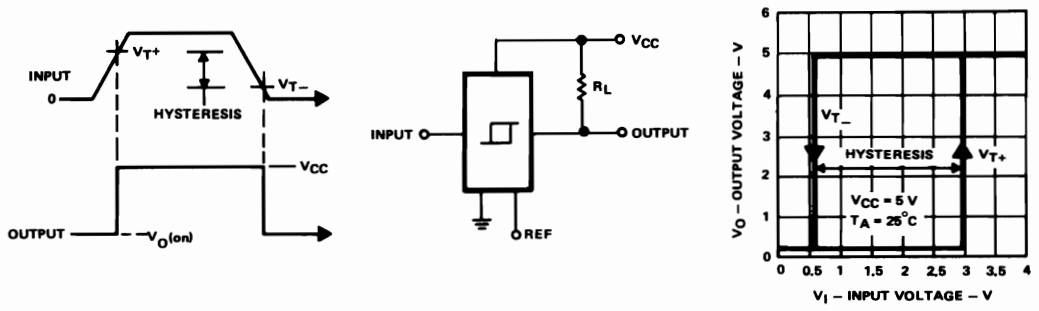


Figure 6.3. Transfer Function of the SN72560

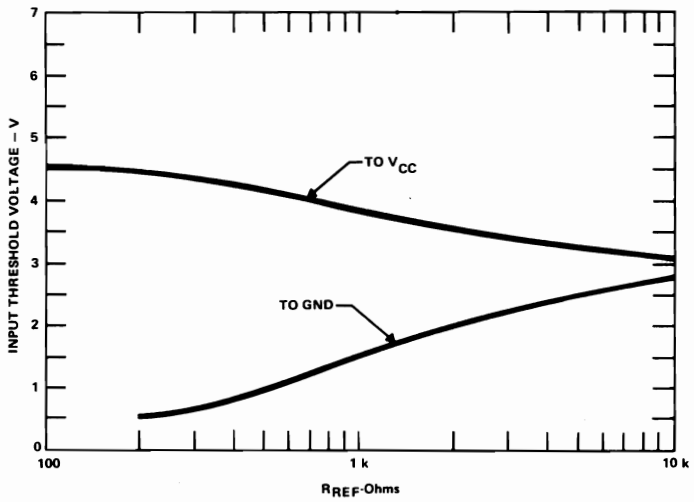


Figure 6.4. Input Threshold Versus V_{REF}

The output of the SN72560 is capable of sinking a maximum current of 160 mA and is guaranteed, at a TTL-compatible voltage of 0.4 V maximum, to sink a current of 48 mA. With the appropriate output pull-up resistor (R_L = 2.0 kΩ), a fan-out of 30 TTL loads can be accommodated.

The input source impedance should be limited, due to the fact that the input current I_{T+} is typically 2 nA and the holding current I_{T-} is 1.2 μA. The maximum recommended source resistance for stable operation is

$$R_{in}max = \frac{V_{CC} - V_{T-}}{I_{T-}}$$

but for safe operation it is better to add a 0.5-V noise margin above the negative-going threshold level. This makes

$$R_{in}max = \frac{V_{CC} - (V_{T-} + 0.5)}{I_{T-}}$$

For example: if V_{CC} = 5 V, I_{T-} = 1.2 μA, and V_{T-} = 0.6 V, $R_{in}max \approx 3$ MΩ.

6.3.2 SN72560 Applications

Bounceless Switch — An application that demonstrates the basic operating characteristic of the SN72560 is the bounceless switch, shown in the circuit of Figure 6.5. As soon as switch S_1 is opened, capacitor C will be charged through resistor R, and when V_{T+} is reached the output will go high. If, during the charge time, switch S_1 bounces and closes, capacitor C will discharge and nothing will be seen on the output until bouncing ceases. When the switch is closed, the output changes directly to zero. When a bounce occurs, nothing is seen on the output if C is not sufficiently charged. This is illustrated by the waveforms in Figure 6.5.

Long-Delay Timer — In this application (see Figure 6.6) resistor R can be much higher than 1 MΩ, because, if the output is low, diode D is reverse biased and the delay time is determined only by the values of C and R. As soon as the switch is opened and voltage V_{T+} is reached the output goes high, and diode D will be forward biased to deliver the extra input current necessary to keep the input high. The upper limitation for resistor R is influenced by:

1) The leakage resistance of capacitor C.

2) The reverse resistance of the diode and the resistance R_F.

Note: In this application

$$R_L \ll R_F, \text{ and } \frac{R\,(R_F + R_L)}{R + R_F + R_L} < 3\ \text{M}\Omega$$

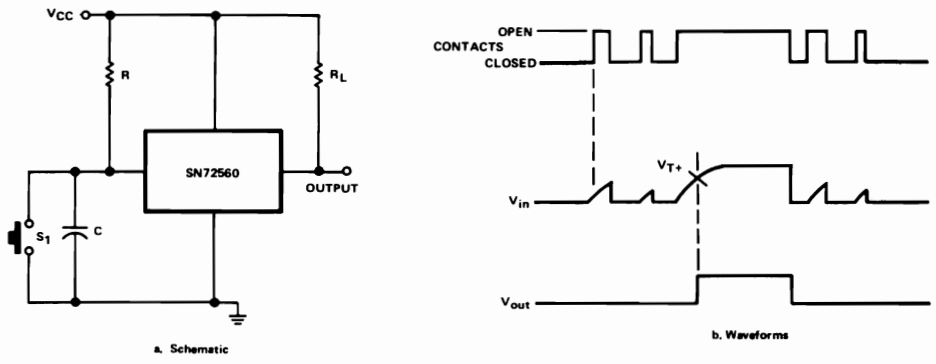


Figure 6.5. Bounceless Switch Interface

Another circuit for obtaining long delay periods is shown in Figure 6.7. When the switch is opened, capacitor C is charged by the base current of the transistor. This makes the charging time equal to $h_{FE}CR$. The timing period is h_{FE} dependent, but the circuit has the advantage of utilizing smaller resistor or capacitor values.

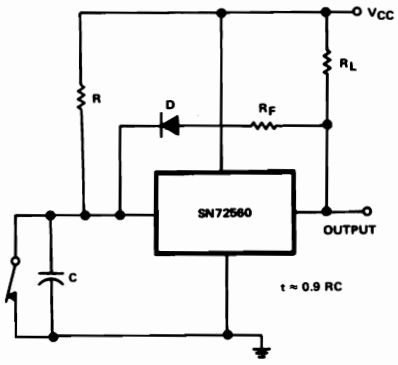


Figure 6.6. Basic Long-Delay Timer

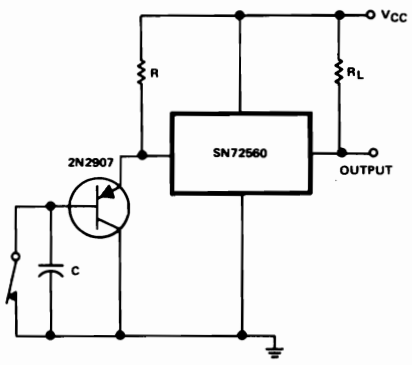


Figure 6.7. Alternate Long-Delay Timer

6.4 SN72555 PRECISION TIMER

6.4.1 Description

The SN72555 monolithic timing circuit is capable of producing accurate time delays or oscillation. The timed interval is controlled by a single resistor-capacitor network. When the device is used as an oscillator, the frequency and duty cycle are controlled with two external resistors and a single external capacitor.

An internal bias network, seen in Figure 6.8, establishes the positive-going input threshold at two-thirds V_{CC}, and the negative-going threshold at one-third V_{CC}. These levels may be changed by applying external bias to the control terminal (pin 5). Internal comparators sense input signal levels, setting the RS flip-flop when the input is below threshold, and thus switching the output high. If the input is above threshold, the flip-flop is reset and the output goes low. In addition, when the output is low transistor Q1 is turned on, providing a low impedance path to ground at pin 7. The SN72555 may be used at V_{CC} levels up to +16 volts, and is capable of sinking or sourcing currents up to 200 mA at its output.

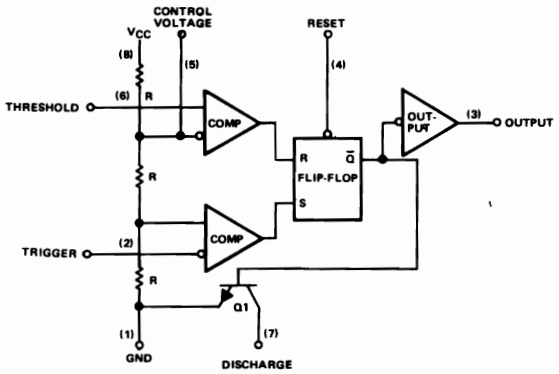


Figure 6.8. Block Diagram of the SN72555

6.4.2 SN72555 Applications

The SN72555 may easily be adapted to a simple one-shot type of monostable function by connecting it as shown in Figure 6.9. As illustrated by the waveforms, a negative-going input pulse at the trigger input sets the flip-flop, and the external capacitor begins charging. During the charge time the circuit output is held high. When the capacitor is charged to the threshold level the flip-flop is reset, energizing Q1, discharging C, and driving the output back to its low level.

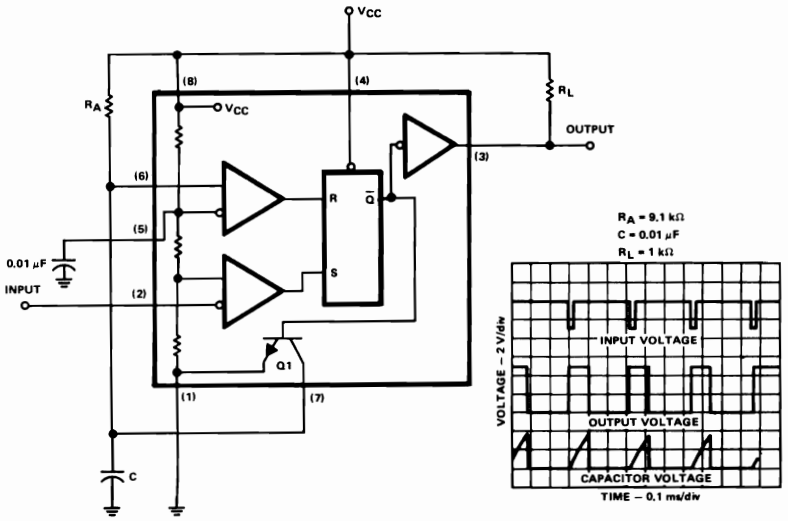


Figure 6.9. Monostable Operation of the SN72555

Once a trigger pulse has been applied, the circuit will continue to time out until the threshold level is reached, regardless of further triggering. The resulting pulse width is approximately 1.1 $R_A C$.

The variety of internal functions available in the SN72555 suggests a large number of applications. For example, the following applications are discussed in the data sheet for this device: monostable operation; pulse-width modulation; pulse-position modulation; astable multivibrator; missing-pulse detector; frequency divider; and sequential timer.

An additional practical application is power sequencing. It is simple to delay the turn-on of one supply or circuit by using the SN72555 output as the drive for a pass transistor furnishing power to a load (see Figure 6.10). The $R_A C$ time constant may be adjusted to provide the desired power-on delay time.

Delaying the turn-off of power to some part of a system requires slightly different circuitry, as shown in Figure 6.11. As long as the power switch is on, the output is maintained on due to output pass transistor drive from R1 and D1. When the switch S_1 is turned to the off position, a negative transient coupled into pin 2 starts the timing function. R2(680 kΩ) and C1(47 μF) will time out in slightly less than 30 seconds, at which point the output at pin 3 goes low, turning off the 2N5449 series pass transistor.

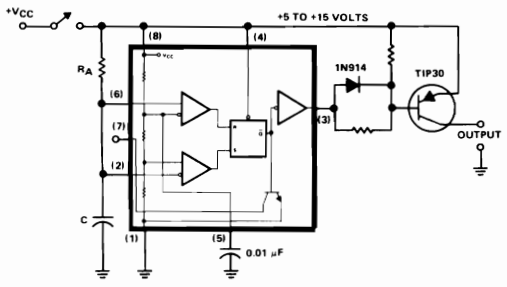


Figure 6.10. Delayed Turn-On Power Sequence

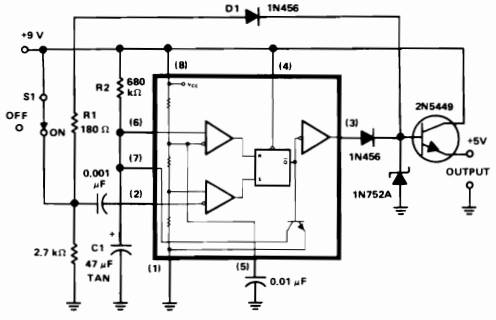


Figure 6.11. Delayed Turn-Off Power Sequence

6.5 SN76502 LOGARITHMIC AMPLIFIER

6.5.1 Description

The SN76502 logarithmic amplifier has been utilized in high-performance applications such as broadband radar, infrared reconnaissance, and weapons systems; however, it is useful for many general-purpose data-compression and analog applications.

For effective use of this device it is necessary to understand its advantages and limitations. The basic logarithmic response is derived from the exponential current-voltage relationship of collector current and base-emitter voltage. Differential amplifiers, used to allow dual-polarity inputs, provide self-compensation for variations in temperature and supply voltage, and common-mode noise rejection. A single differential section has a usable range of 15 dBV.

Figure 6.12 is the functional block diagram of the SN76502. There are eight log subsections each having a 15-dBV operating range. Each input to the device feeds two of these subsections, for a total range of 30 dBV per input section. The log currents from two sections (A1 and A2 or B1 and B2) are summed and coupled to a complementary output stage which provides a differential output signal that is the sum of the logs of the input signals. For example, $Y - \overline{Y} = \log A1 + \log A2$. The total operating range of one stage is 60 dBV.

Currents of the two output stages of the SN76502 can be summed by connecting Y to Z and $\overline{Y}$ to $\overline{Z}$ (Figure 6.12); the difference of the currents is obtained by connecting Y to $\overline{Z}$ and Z to $\overline{Y}$. When summing, the total theoretical operating range is 120 dBV.

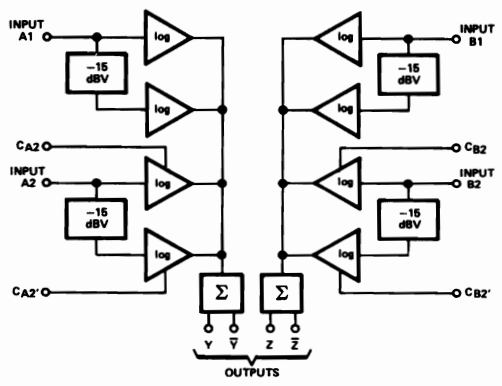


Figure 6.12. Functional Block Diagram of the SN76502

6.5.2 Input Considerations

To assure proper operation over a wide range of input voltages, certain operating limitations must be considered. The recommended input voltage range for any one section is 10 mV to 1.0 V. Signals below 10 mV are outside the normal log characteristic of the input stage, and levels exceeding 1.0 V may result in limiting as the input transistors go into saturation, allowing distortion of the output log characteristic. Excessive input signal ($> \pm 3$ V) will result in hard saturation and clamping of the log current summing, causing severe distortion of the output signal. To allow operation over a wide input range and maintain the input voltages to the different sections within limits, two signal modifications may be required.

1) There must be some form of signal-amplitude limiting at the input of each log section to prevent input overdrive. This may be accomplished by the use of diodes or by limiting within the interface amplifier.
2) The amplitude of each 30-dBV portion of the input signal must be adjusted to be at the proper operating level at the designated log-amp input.

Figure 6.13 shows an example of how a dynamic input signal might be modified as it is fed to the various logarithmic amplifier inputs. The input signal is to have a total range of 120 dBV (30 μV to 30 V). The signal from 30 μV to 1 mV is amplified 60 dB by G3, providing an ideal 30 mV to 1 V operating level into input B2. The 1 to 30 mV portion is amplified 30 dB by G2 to provide about 30 mV to 1 V drive for input B1. G1 provides unity gain to the 30 mV to 1 V portion, feeding input A2. The 1 to 30 V portion is attenuated by 30 dB as it is fed to input A1. All of the interface amplifiers must have some form of output limiting between 1 and 3 volts to prevent overdriving the SN76502 inputs during large input signal conditions. The circuit of Figure 6.14 will handle higher level input voltages, with the input circuitry providing lower gain.

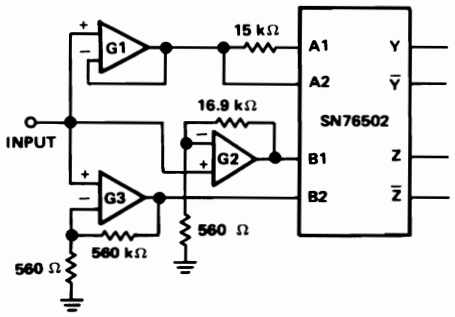


Figure 6.13. Configuration for Input Signals of 30 μV to 30 V

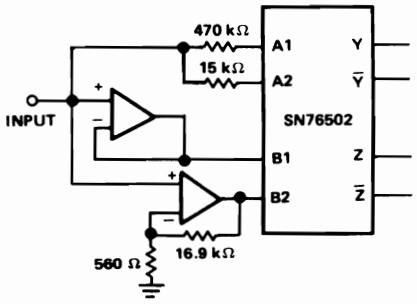


Figure 6.14. Configuration for Higher-Level Input Signals

Another input consideration is interface amplifier offset, particularly when using high-frequency amplifiers. For high-frequency (1 to 40 MHz) applications the amplifiers selected may have considerable output offset. This is characteristic of most video-frequency amplifiers, requiring capacitive coupling into the log amp for proper results.

6.5.3 Output Considerations

The output signals from the logarithmic amplifier are low level, generally less than 0.6 volt. The quiescent output level is about +5.6 volts. Note that this is near the V_{CC+} level of 6.0 volts and is in the form of a common-mode level for the Y-$\overline{Y}$ and Z-$\overline{Z}$ outputs. An external differential amplifier is normally used on the output to provide common-mode rejection and output slope and offset control. The output buffer amplifier must be capable of handling at least 6 volts common-mode input as well as the frequencies involved.

SN76502 differential output offset (normally only ±40 mV) may be adjusted by 10-k ohm potentiometers connected across the compensation terminals C_{A2} and C_{A2}', and C_{B2} and C_{B2}' with the control arms to V_{CC-}.

6.5.4 Performance Considerations

Device parameters best describing the performance characteristics of the SN76502 are the scale factor (ac or dc) and the dc error factor. The scale factor is a multiplier relating the actual output swing in mV of a log stage to its input swing in dBV. The resulting units are mV/dBV. The test points of 18-mV input and 560-mV input are chosen to be in the active and usable region of operation. They represent a 30-dBV swing in the input, from −5 dBV to −35 dBV. 1.0 volt is used as the reference level of 0 dBV.

With the unit of measurement being millivolts, 20 log 560 − 20 log 18 is equal to 55 − 25 or a 30 mV output swing. If this were true, the scale factor, relating the output swing of 30 mV to the input swing of 30 dBV, would be 1 mV/dBV. Internal gain will result in higher output levels. The following is a typical example.

Input Level	Output Level
18 mV	200 mV
560 mV	440 mV

Applying these values to the resulting equation for scale factor (SF) we have the following:

$$SF = \frac{V_{out} \text{ at } 560 \text{ mV} - V_{out} \text{ at } 18 \text{ mV}}{30 \text{ dBV}}$$

$$= \frac{440 \text{ mV} - 200 \text{ mV}}{30 \text{ dBV}} = \frac{240 \text{ mV}}{30 \text{ dBV}}$$

$$= 8 \text{ mV/dBV}$$

At low frequencies the scale factor for dc or ac conditions is essentially the same. At high frequencies (10 to 40 MHz) there may be some differences due to slight variations in gain at these levels.

The amount of droop (or bow) of the log-stage output response from its true value at the midpoint of its operating range is the dc error. This parameter is measured at an input level of 100 mV. This is the —20-dBV point and is chosen to be midway between the —5-dBV and —35-dBV test points.

The output level at the mid-range point should equal the average of the output levels at the end test points. If this were true, there would be no error. The absolute value of the difference between the actual midpoint output level and what it should be is the error in millivolts. To determine the actual error in dBV it is necessary to divide by the scale factor of this circuit.

The resulting equation for the error is

$$\text{Error} = \frac{\left|V_{out} \text{ at } 100 \text{ mV} - (.5)\,(V_{out} \text{ at } 560 \text{ mV} + V_{out} \text{ at } 18 \text{ mV})\right|}{\text{Scale Factor}}$$

In a typical application the output versus input levels are

Input Level	Output Level
18 mV (—35 dBV)	220 mV
100 mV (—20 dBV)	328 mV
560 mV (—5 dBV)	440 mV

$$\text{Error} = \frac{|328\text{ mV} - (.5)(440\text{ mV} + 200\text{ mV})|}{8\text{ mV/dBV}}$$

$$= \frac{|328\text{ mV} - 320\text{ mV}|}{8\text{ mV/dBV}} = \frac{8\text{mV}}{8\text{ mV/dBV}}$$

Typical Error = 1 dBV

6.5.5 SN76502 Applications

A good application of the logarithmic amplifier which demonstrates its functions and performance capability is the circuit shown in Figure 6.15 which solves for the hypotenuse of a right triangle when given the two sides. With SN76502 logarithmic amplifier sections it is possible to solve for Z (the hypotenuse), applying the values of X and Y into the input as shown. The output of the circuit is automatically the value for Z. An analysis of the various log functions required is as follows:

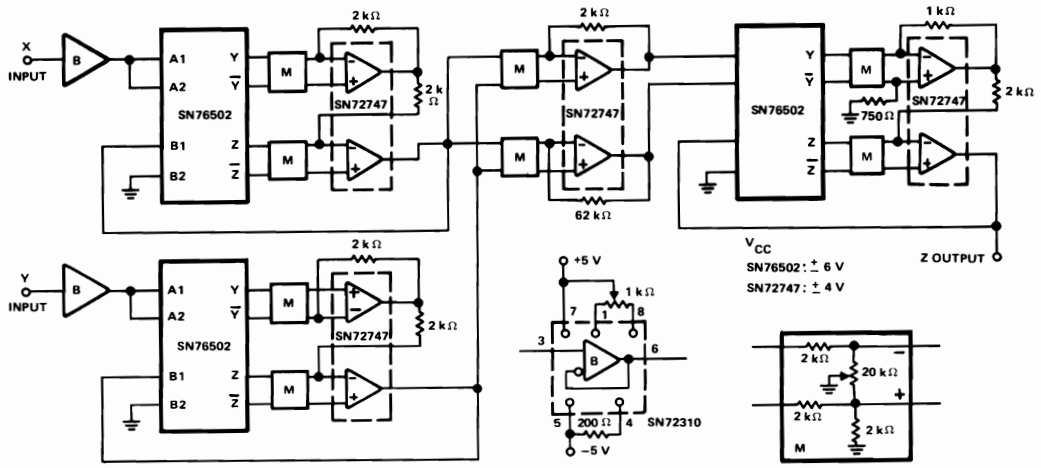


Figure 6.15. Circuit for Direct Solution of Right-Triangle Hypotenuse

$$Z^2 = X^2 + Y^2$$
$$= \text{antilog } 2 \log X + \text{antilog } 2 \log Y$$
$$Z = \text{antilog } 1/2 \log Z^2$$
$$= \text{antilog } 1/2 \log (\text{antilog } 2 \log X + \text{antilog } 2 \log Y)$$

6.6 SN76514 BALANCED MIXER

6.6.1 Description

The process of mixing two signals of two different frequencies to obtain a third signal is a widely used function in all types of communication systems.

With the increased use of the single-sideband suppressed-carrier type of transmission the demand for these circuits is increasing. In a single-sideband (SSB) system the frequency conversion process must be accomplished by a mixing or heterodyning action, rather than the frequency multiplying process which would result in a loss of the original modulating signal and in increased unwanted distortion products. In many respects the processes of modulation, mixing, and detection are basically the same; their requirements and circuit analysis are very similar. They operate on the basic principle in which two signals of different frequencies are applied to either one or two input ports. The output signal is a complex function best expressed by a power series such as:

$$E_{out} = A_0 + A_1 e_c + A_2 e_c^2 + A_3 e_c^3 + A_4 e_c^4$$

A mathematical expansion of this expression involving two input signals of frequency f_o and f_s will show the following products in the output:

f_o, f_s
$f_o \pm f_s$
$2f_o \pm f_s, f_o \pm 2f_s$
$3f_o \pm f_s, f_o \pm 3f_s$
$4f_o \pm f_s, f_o \pm 4f_s$ — — and so on

The order of the product $nf_o \pm mf_s$ is defined as the sum of n + m. Generally, the strongest components are the lower-order products. As such, only these are considered to be of importance. Since the desired output is either the sum or difference frequency $f_o \pm f_s$, all undesired components should be eliminated.

Attenuation of these undesired components is a major problem in the design of mixers and modulators. Often, mixer and modulator circuits are followed by filters or tuned circuits which attenuate those frequency components outside the desired passband range. This method of attenuation is adequate for attenuation of high-order products and other components outside the desired passband. However,

some of the odd-order intermodulation products fall inside or very close to the desired passband. Their attenuation is primarily a function of the mixer itself.

Balanced modulator/mixer circuits have the advantage of suppressing one of the input signals, usually the carrier, and also cancellation of harmonics of the same by applying two signals equal and opposite in phase to each other at the output. In the doubly balanced mixer, this is extended to include both input terminals. The degree of attenuation is dependent upon the balance of the two output signals. If both signals are equal and opposite in phase, maximum cancellation occurs. Balance can be achieved by matching components. Since this is impractical when using discrete components one or more adjustment controls, such as variable capacitors or resistors, can be used to offset the balance due to mismatch.

Although discrete component matching is impractical, component matching can be achieved by using integrated-circuit techniques. A balanced modulator/mixer circuit is ideally suited to integrated-circuit design since its power and voltage requirements are not high and no tuned circuits are necessary for obtaining the desired balance. The SN76514 monolithic integrated circuit has been developed to perform as a doubly balanced modulator or mixer with, in general, no controls required to achieve balance. This integrated circuit contains seven matched transistors and resistors in an L or N package (Figure 6.16). Since component matching is achieved with integrated-circuit techniques, a high degree of cancellation of undesired frequency components in the output signal is obtained. The SN76514 devices have three inputs and two separate outputs available. Other points in the circuit are brought out for proper ac bypassing and power supply connections. The circuit offers a definite size advantage over discrete component systems. No external adjustments are necessary to meet most of the required attenuation and isolation specifications.

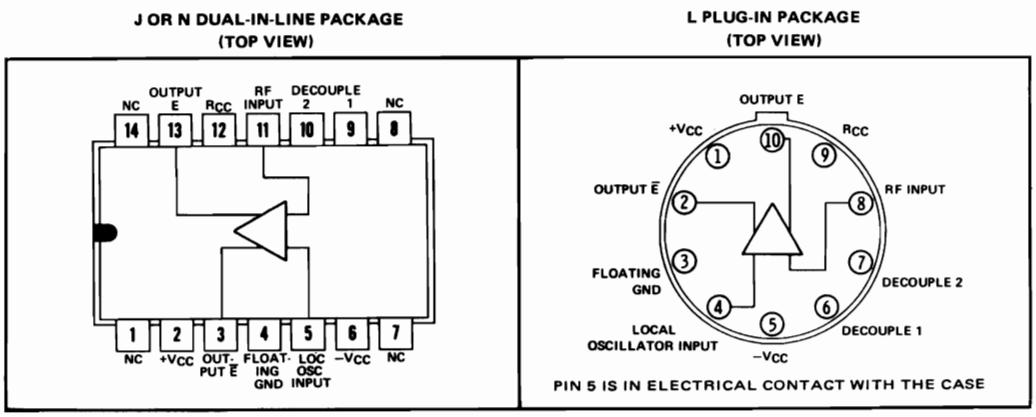


Figure 6.16. Package Pin-Outs of the SN76514

Figure 6.17 shows the SN76514 circuit diagram with pin assignments for the 10-pin metal-can L package. Throughout the discussion pin designations apply to the L package. In Figure 6.17 it can be seen that the device consists of two cross-coupled differential amplifiers, the emitters of which are driven by a third differential pair. Pins 7 and 8 form a differential pair for one input signal while pin 4 forms a single-ended input for the other signal. The device operates as a doubly balanced system in that both signal inputs are balanced out and appear greatly attenuated at the outputs. Pins 2 and 10 form the output connections where signals are available in push-pull or single-ended form.

The circuit is designed to operate from a single 12-volt supply or dual ±6-volt supplies. For operation from a single 12-volt supply, connect the positive terminal of the supply to $+V_{CC}$, the negative terminal to $-V_{CC}$, and the floating-ground terminal to R_{CC}. For operation from two 6-volt supplies, leave R_{CC} open and connect the positive terminal of one supply to $+V_{CC}$, the negative terminal of the other supply to $-V_{CC}$, and the remaining terminals of the two supplies to the floating-ground terminal.

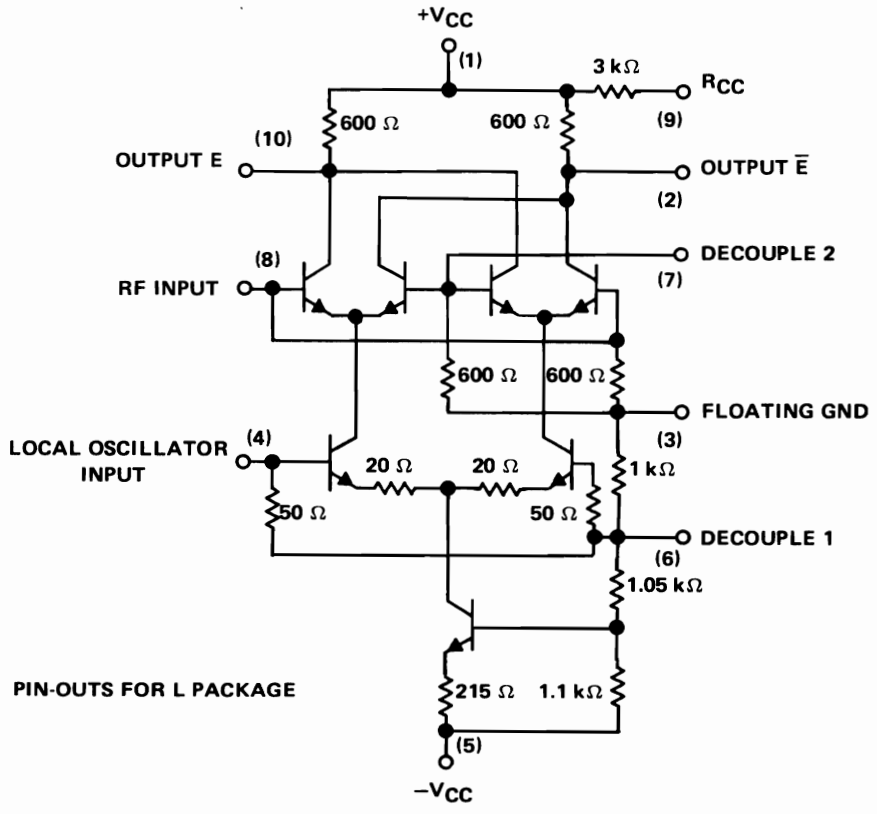


Figure 6.17. Schematic of the SN76514

The inputs and outputs should be ac coupled to prevent dc unbalance in the circuit. Particular care is required when operating a device at low frequencies because the coupling capacitors will usually be of the electrolytic type, and leakage in the input capacitors will degrade the balance in the circuit. This still applies if pins 7 and 8 operate around ground potential. Capacitive coupling is still required but leakage problems will be minimized.

The SN76514 was designed to present a low impedance at the inputs. This is nominally 50 ohms for pin 4 and 600 ohms for pins 7 and 8. Following is a list of single-ended input impedances versus frequency.

Frequency	Pin 4	Pin 7 or 8
5 MHz	63 Ω	530 Ω
10	62	450
50	68	360
100	80	290

The output impedance of either pair is dependent on the operating frequency and the collector load resistor, R_L. A 600-ohm resistor is supplied on the chip. This value can be reduced by externally connecting a resistor in parallel from V_{CC} to the collector.

The SN76514 has been operated satisfactorily up to 150 MHz. Depending on the required signal isolation and conversion gain it could be used at higher frequencies. Conversion gain is a function of the oscillator voltage level as related to the desired output signal.

A large oscillator voltage will provide good conversion gain but odd-order intermodulation products will be higher. A low oscillator voltage results in poor conversion gain, poor noise figure, and therefore relatively higher feedthrough ratio. The derivation of the transfer characteristic of the device shows the output voltage V_o to be: $V_o = -600\ (0.018)e_2 \tanh\ (38\ e_1/2)$ for the on-chip loads of 600 ohms, where e_1 is applied to pin 7 or 8, and e_2 is applied to pin 4.

6.6.2 SN76514 Applications

Mixer — One use of the SN76514 device is as a mixer, where a carrier f_o is mixed with a signal f_s. The desired output is $f_o \pm f_s$. As a result of the deficiencies in the mixing process other outputs are produced. Generally, the higher the order of the intermodulation product, the lower the amplitude.

Figures 6.18, 6.19, and 6.20 illustrate the performance of the SN76514 as a frequency converter using the input frequencies of 1 MHz and 10 MHz. These tests

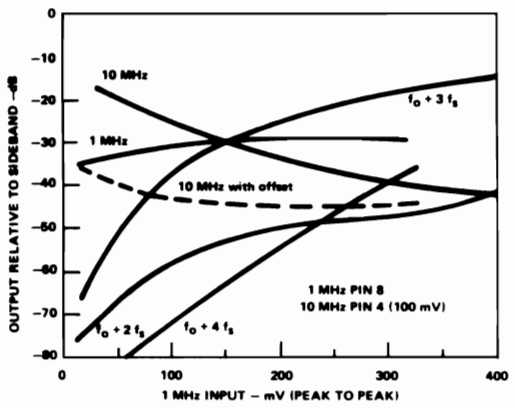


Figure 6.18. Input-Output Characteristics

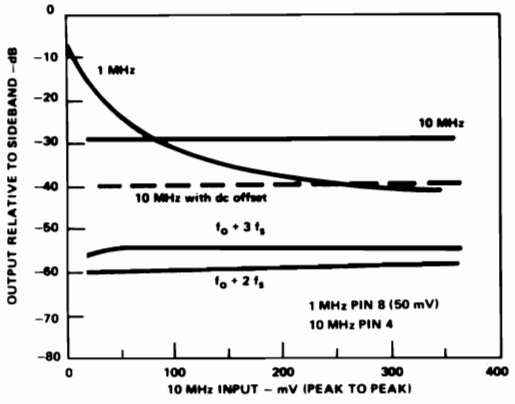


Figure 6.19. Input-Output Characteristics

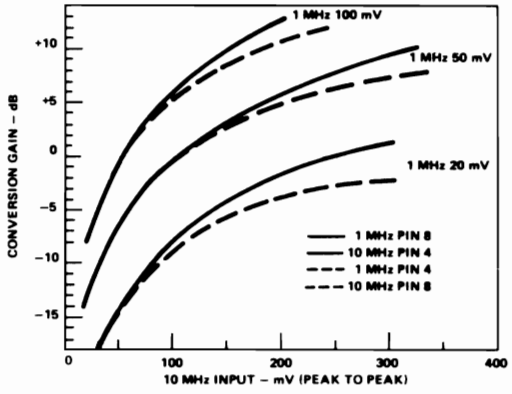


Figure 6.20. Conversion Gain

were made with a filter in the 1-MHz input. This improves the level of harmonic distortion present at the input to better than −90 dB. This was necessary to give accurate results for the intermodulation product measurements. Figures 6.18 and 6.19 are graphs plotted relative to mean sideband levels.

The large number of results are included because it is not easy to characterize a device such as a mixer which can be used over a wide range of input frequencies and levels. It can also be seen that the user must make the compromise between the levels of intermodulation products and feedthrough from the input signals that can be tolerated.

The SN76514 has a good performance as it stands with regard to intermodulation products and feedthrough of input signals, due to the inherent matching between the circuit elements produced by the monolithic integrated-circuit process. Good

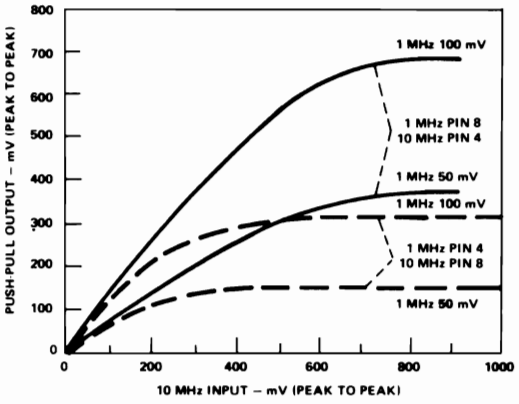


Figure 6.21. Mixer Performance Characteristics

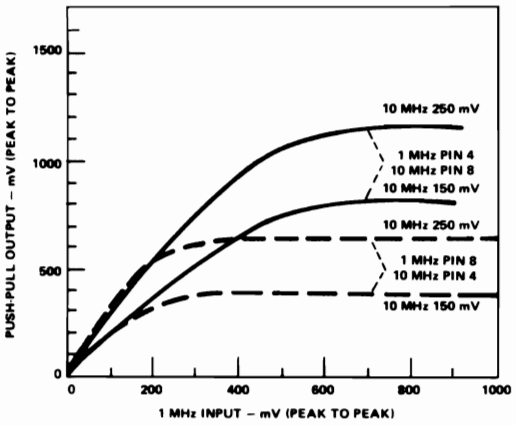


Figure 6.22. Mixer Performance Characteristics

thermal matching is also achieved because the elements result from the same diffusion processes and are in close physical proximity to one another. However, the performance can be improved by the introduction of a small dc differential offset current to the upper differential pairs (pins 7 and 8). The current required is small, being typically of the order of a microamp. The effect of this offset current can be seen in Figures 6.18, 6.19, and 6.20. It must be noted that pin 4 input is a signal affected by the balance method. This will dictate which of the two input signals should be applied to pin 4 and which to pin 7 or 8. Figures 6.21 and 6.22 show the input-output characteristics of a device when used as a mixer. Good linearity is preserved up to about 100 mV peak to peak.

Frequency Doubler — When the SN76514 is used as a frequency doubler the principle employed is that of a multiplier where the same frequency is applied to both input terminals. It is, of course, still single ended to pin 4 and single ended or differential to pins 7 and 8. The output can be taken single ended or push-pull from pins 2 and 10. No tuned circuits are employed, and Figure 6.23 shows the variation of harmonic content in the output waveform with input voltage level, relative to the level of the doubled frequency. The user must make the compromise between the tolerable level of 1-MHz component consistent with, in this case particularly, the 4-MHz component. Alternatively, while applying the same frequency, different levels can be applied to the input terminals (pins 4 and 8).

Figure 6.24 shows the input and output waveforms of 1 and 2 MHz respectively. Because the device is of monolithic integrated construction, there is no reason why the phase balance should not be good and therefore the phase relationship between

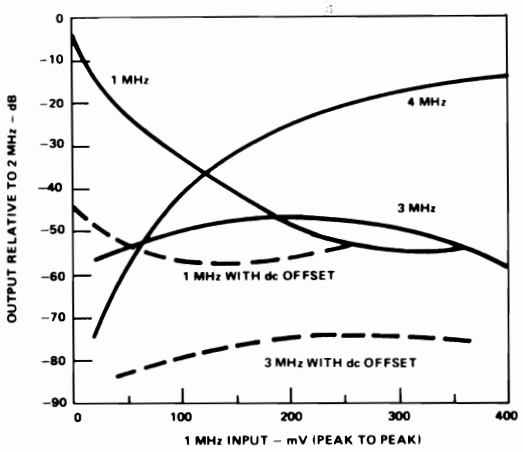


Figure 6.23. Input-Output Characteristics of Frequency Doubler

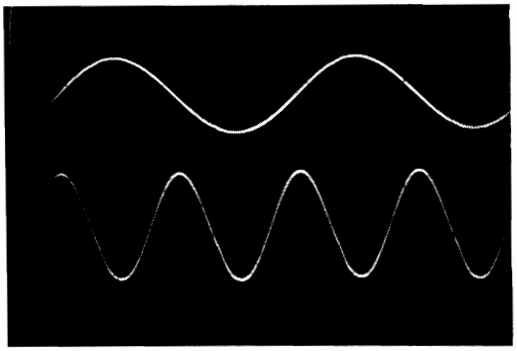


Figure 6.24. Input-Output Waveforms of Frequency Doubler

input and output waveforms be preserved over a wide frequency range. It should be noted that when using a device in a doubler application the use of the balance control to apply a small dc differential offset between pins 7 and 8 improves the performance considerably, particularly with regard to fundamental feedthrough. Differential dc current into pins 7 and 8 is typically in the microamp region.

Variable-Gain Amplifier — There is often a requirement in communication and radar systems for an amplifier, the gain of which can be controlled over a wide range by means of a control voltage. It is possible to use the SN76514 as a variable gain amplifier as shown in Figure 6.25.

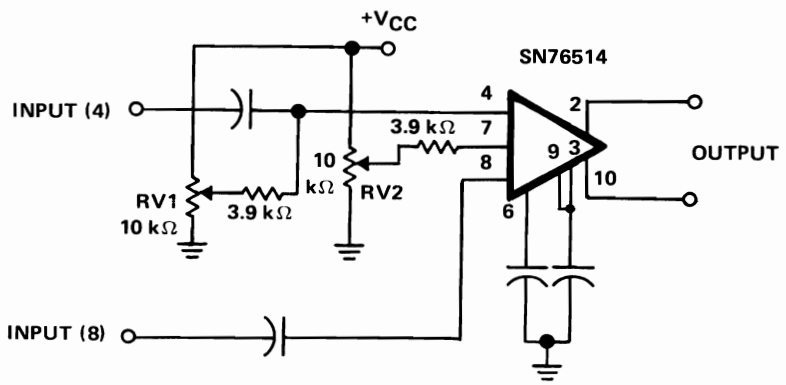
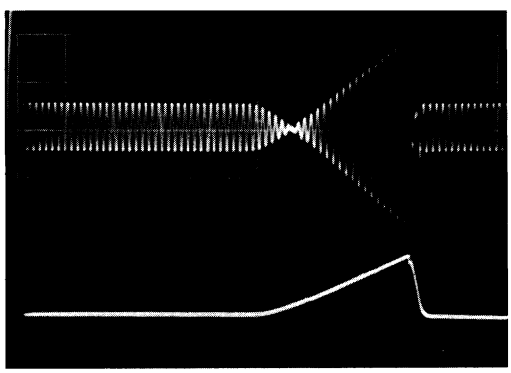


Figure 6.25. Variable-Gain Amplifier, Amplitude Modulator, or Chopper Circuit

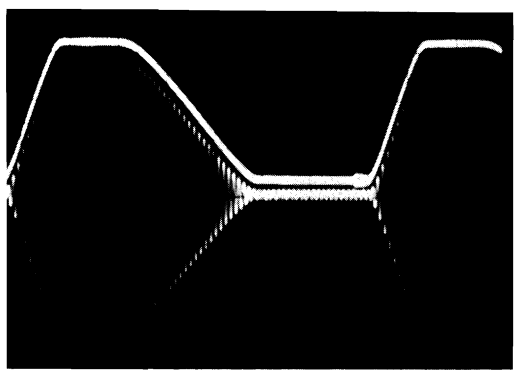
Potentiometer RV1 is used to set the mean level of the input voltage to pin 4. If there were no dc component present, the integrated circuit would give zero output at a point corresponding to balance. Either side of that point an output is produced but there will be a phase shift of π radians as balance is passed through. Figure 6.26 shows a 15-MHz carrier gain controlled by a ramp waveform but with no dc applied from RV1. The point of balance is readily seen as well as the π radians phase change as balance is passed through. Note that with no dc input the crossover point corresponds to the mean level of the input waveform.

Figure 6.27 shows the device used as a swept-gain amplifier operating at a signal frequency of 50 MHz. The input-controlling waveform is superimposed to give some idea of control linearity. Note that this waveform has been displaced on the oscilloscope to display it more clearly.



VERTICAL SCALE: 100 mV/div

Figure 6.26. Amplitude Variations with 15-MHz to Pin 8 and Modulating Ramp to Pin 4



VERTICAL SCALE: 50 mV/div

Figure 6.27. Swept-Gain 50-MHz Amplifier

Potentiometer RV2 in Figure 6.25 is purely a refinement serving as a trim control to set the positive and negative portions of the modulation envelope to equal amplitudes. In the majority of cases it is not required. The setting of potentiometer RV1 depends upon the amplitude of the controlling waveform, and, if it is capacitively coupled, its duty cycle. The object is to adjust the mixer to be balanced on one peak of the controlling waveform, corresponding to theoretically zero output. In practice, the null level will depend on the carrier frequency. Figure 6.27 shows the low level of feedthrough even at 50 MHz.

Care must be taken with the layout, keeping input and output separate. A shield may be required between them when operating at high frequencies.

If dc coupling to pin 4 at ground is required, pin 6 must be operated at ground (it could be connected to a low-impedance potentiometer of less than 100 Ω resistance

to act as a zero control). This implies that pin 5 is operated at −4 V and pin 1 at +8 V. Pin 3 is connected to pin 9. Output is taken from pins 2 and 10 in push-pull or single ended from either.

Amplitude Modulator — The SN76514 can be used as an amplitude modulator in communication systems. Here the modulation can be applied at low level, the output being increased in power level by succeeding linear power amplifiers. Operation is similar to the application as a variable gain amplifier.

Pins 7 and 8 are used as carrier inputs because it was found that there was less carrier feedthrough than when pin 4 was used. Potentiometer RV2 is not normally required but allows the amplitude of the positive and negative halves of the modulation envelope to be equalized. Conversely, if some asymmetry is required due perhaps to the characteristic of a later stage, this is readily achieved. Potentiometer RV1 is used to unbalance the device so that it just balances, giving theoretically zero output on the negative modulation peaks. If over-modulation is attempted, instead of the carrier cutting off, it passes through zero before the modulation peak is reached, reverses in phase and then increases again up to the peak of the modulating waveform.

Chopper — The SN76514 can be used as a chopper, a device required frequently in the instrumentation and control fields. Here, unlike the application as an amplitude modulator, the unbalanced dc signal is fed to the input with the high-frequency carrier. The carrier can be either sinusoidal or rectangular in form.

The majority of the dc offset is applied to pin 7 (pin 8 could be used). The setting required will depend on the level of carrier, both levels affecting the base line. If control is required over the symmetry of the positive and negative halves of the resultant envelope, the control RV1 is used to apply a small dc offset to pin 4.

Figure 6.28 shows a 2-MHz carrier chopping a 135-kHz sine wave. Figure 6.29 shows similar performance with a 10-MHz chopping signal and a 100-kHz sine wave.

If the signal to be chopped is dc about ground the following procedure should be adopted:

Pin 5 connected to a supply of −4 V
Pin 1 connected to a supply of +8 V
Potentiometer RV2 connected between the supply lines.

Balanced Modulator — The SN76514 is of great use in the generation of single-sideband suppressed-carrier signals. There are three basic methods for the production of such signals.

1) A filter method using a balanced modulator to mix audio and a frequency of several hundred kilohertz. The resultant double-sideband suppressed-carrier signal is passed through a fixed-frequency filter. The remaining single-sideband suppressed-carrier signal is mixed to the transmitter frequency and power level.
2) A phasing method using two audio signals from a coherent source but with 90° phase shift between them over the audio range. A similar carrier source is also arranged. By mixing all four signals in two doubly balanced modulators, the two resulting sidebands from each modulator can be added, canceling one, and reinforcing the other, due to their phase relationships.
3) A combination of 1) and 2) designed by D. K. Weaver. Here the majority of the circuitry is at audio frequency and the filters are easily derived and can have slack tolerances. The method makes use of the fact that when a lower sideband would theoretically be at a frequency less than zero, it appears at the frequency but changed in phase by 180°.

Many balanced modulators in use today are versions of a two- or four-diode design which offer no conversion gain. The SN76514 supplies some conversion gain, which is desirable when a filter is used to eliminate one sideband.

The availability of the various inputs, the doubly balanced circuitry, and frequency capability of the SN76514 allow its use in many types of RF circuitry. Some other applications are synchronous detectors, color TV chrominance demodulators, FM discriminators, product detectors, and phase modulators.

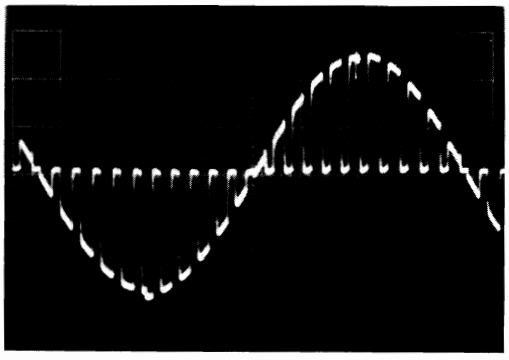


Figure 6.28. 135-kHz Sine Wave Chopped at 2 MHz

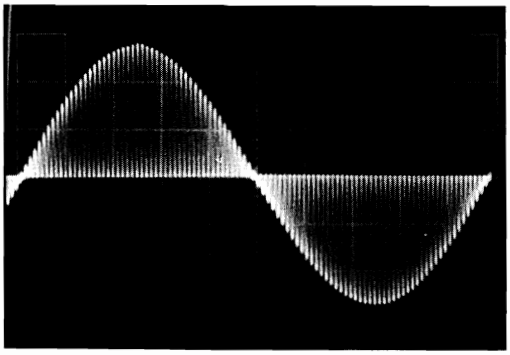


Figure 6.29. 100-kHz Sine Wave Chopped at 10 MHz

7

Peripheral Driver Circuits

7.1 DEVICE DESCRIPTIONS

Many circuit applications may be served using a combination of TTL gates and discrete transistors with good output drive capabilities. Circuits to interface between TTL circuitry and lamps, relays, MOS circuits, high-current devices, optoelectronic circuits, and SCR or triac gates may readily be constructed using such devices.

An integrated circuit containing gates and transistors is a universal type of device that can fill many application needs. Some basic requirements for a satisfactory general-purpose interface device are:

- High-speed capability $\geq$ 10 MHz
- Compatibility with popular voltages (5 to 24 V)
- Logic compatibility
- Output-current capability ($>$ 100 mA)
- Application versatility
- Medium power capability ($\geq$ 500 mW)
- Economical packaging.

The SN75450B, SN75460, SN75470, SN75401, and SN75411 series devices have been designed specifically to meet such application requirements. The versatility of these devices results from their power capability and pin arrangements. Power supply and ground terminals are located on corner pins, allowing easy board layouts. SN75450B, SN75460, and SN75470 NAND gate outputs and transistor bases are adjacent, since many applications require direct connection of these terminals. Also, the transistor emitters, gate ground, and chip substrate are located close to each other for easy interconnection. This arrangement can be seen in Figure 7.1.

A particular advantage of the SN75450B, SN75460, and SN75470 is the substrate terminal. The silicon substrate is not connected to ground, as is normal in TTL circuits. Thus the transistors can be operated at voltage levels more negative than system ground, if the substrate is connected to the most negative dc voltage used in the application. The basic internal schematic (Figure 7.2), with substrate diode

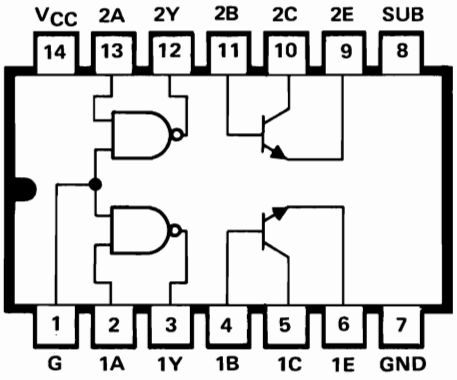


Figure 7.1. Functional Diagram and Pin-Out for SN75450B, SN75460, or SN75470

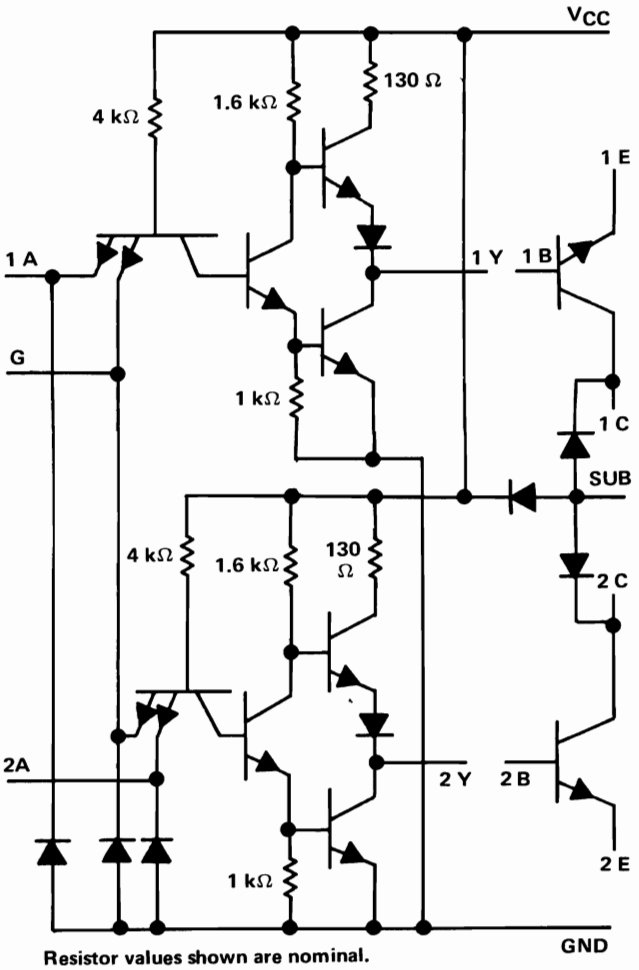


Figure 7.2. Basic Schematic for SN75450B, SN75460, or SN75470

junctions indicated, shows that making the substrate the most negative part of the circuit will keep the substrate diodes reverse biased, preventing any interaction between them and output transistors or gates.

The output-current capability of the SN75450B, SN75460, and SN75470 devices is 300 mA per transistor. The SN75450B has a 30-volt dc output capability with a 20-volt switching limit; the SN75460 has a 40-volt dc output capability and 30-volt switching limit; the SN75470 has a 50-volt dc output capability and 40-volt switching limit. The difference in their operating speeds is insignificant for most applications. For example, t_{PLH} is typically 20 ns for the SN75450B and 45 ns for the SN75460, and t_{PHL} is typically 20 ns for the SN75450B and 35 ns for the SN75460, these being combined gate and transistor speeds. The power-handling capability of the package is 800 mW. The low collector-to-emitter saturation of 0.5 volt typically at load currents of 300 mA makes the output transistors ideal for switching relay loads and for other similar power-control applications.

The many SN75450B series applications in which the gate output is connected directly to the transistor base resulted in the design of the SN75451B/461/471. Basically the same as the SN75450B/460/470 types in performance, these devices simplify circuit assembly in many applications (see Figure 7.3). In addition, the desire for different types of logic capability led to development of the SN75452B/462/472 NAND function, the SN75453B/463/473 OR function, and the SN75454B/464/474 NOR function devices.

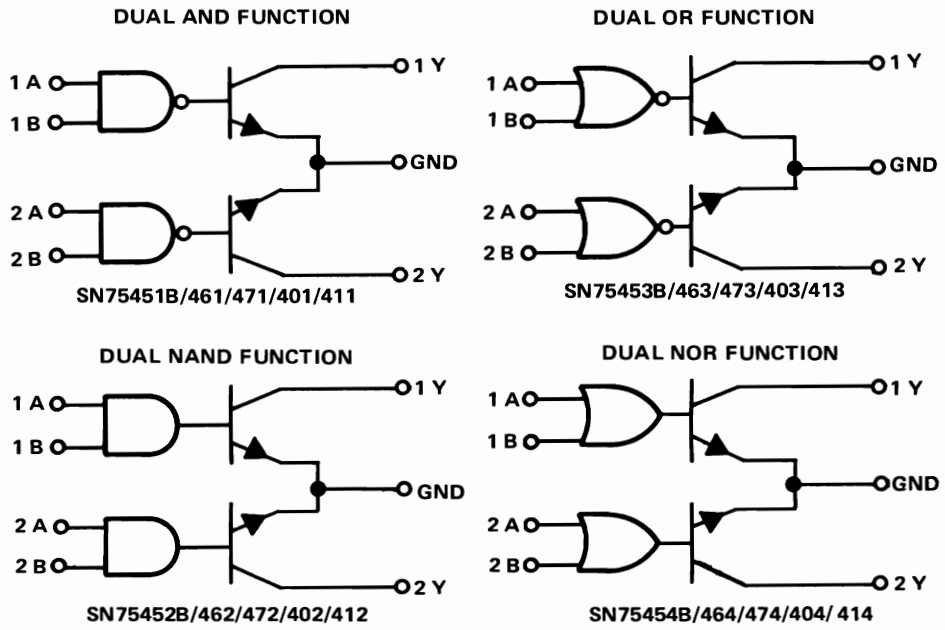


Figure 7.3. Functional Block Diagrams of Peripheral Drivers

Additional power-handling capability is required in some peripheral driver applications, and external power transistors are sometimes used. The SN75401 and SN75411 series devices were developed to allow operation in many applications requiring increased voltage or current capability without need of external transistors. Functional diagrams of the SN75401 and SN75411 series devices are shown in Figure 7.3.

With this series of peripheral drivers continuous current of 500 mA per output transistor is possible. For pulsed applications surge currents of 800 mA can be handled at duty cycles of 10%, if on-time intervals are less than 200 milliseconds. The SN75401 series devices have a 40-volt dc output capability and 30-volt switching limit; the SN75411 series has a 50-volt dc output capability and a 40-volt switching limit.

The SN75401 and SN75411 series devices employ the type ND package (Figure 7.4). The six central pins of the 14-pin DIP package are replaced by heat-sink fins, allowing the package to handle more power. This, combined with higher current output transistors, has increased the capability of monolithic drivers.

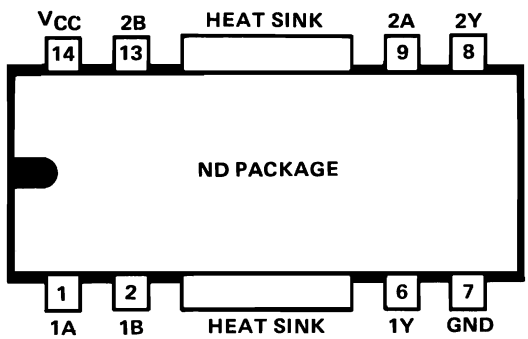


Figure 7.4. Pin-Out for SN75401and SN75411 Series Devices

Power-dissipation capability of the ND package must be considered in high-current applications. Following are some typical mounting configurations and the resulting power-handling capabilities. If no heat-sink material is used and the heat-sink tabs are not soldered to a printed circuit board but are exposed to free-air ambient temperature, resulting thermal resistance ($R_{\theta JA}$) is 75 °C per watt. Under this condition the maximum package power dissipation capability is 1.07 watts, at ambient temperatures up to 70°C. It may then be derated at 13.4 mW/°C to 333 mW at 125° C.†

†Only SN55 series devices should be operated at ambient temperatures above 70°C.

As another popular mounting, the device may be attached to a printed circuit board, with the heat-sink tabs soldered to the ground plane or isolated copper strips. A typical configuration (Figure 7.5) provides a heat-sink area of approximately one square inch. Using a 1/16-inch paper-epoxy board with a 1-oz copper laminate, the thermal resistance was 37.6°C per watt; 2.13 watts could be dissipated at ambient temperatures up to 70°C. The dissipation capability is derated linearly to 668 mW at 125°C.

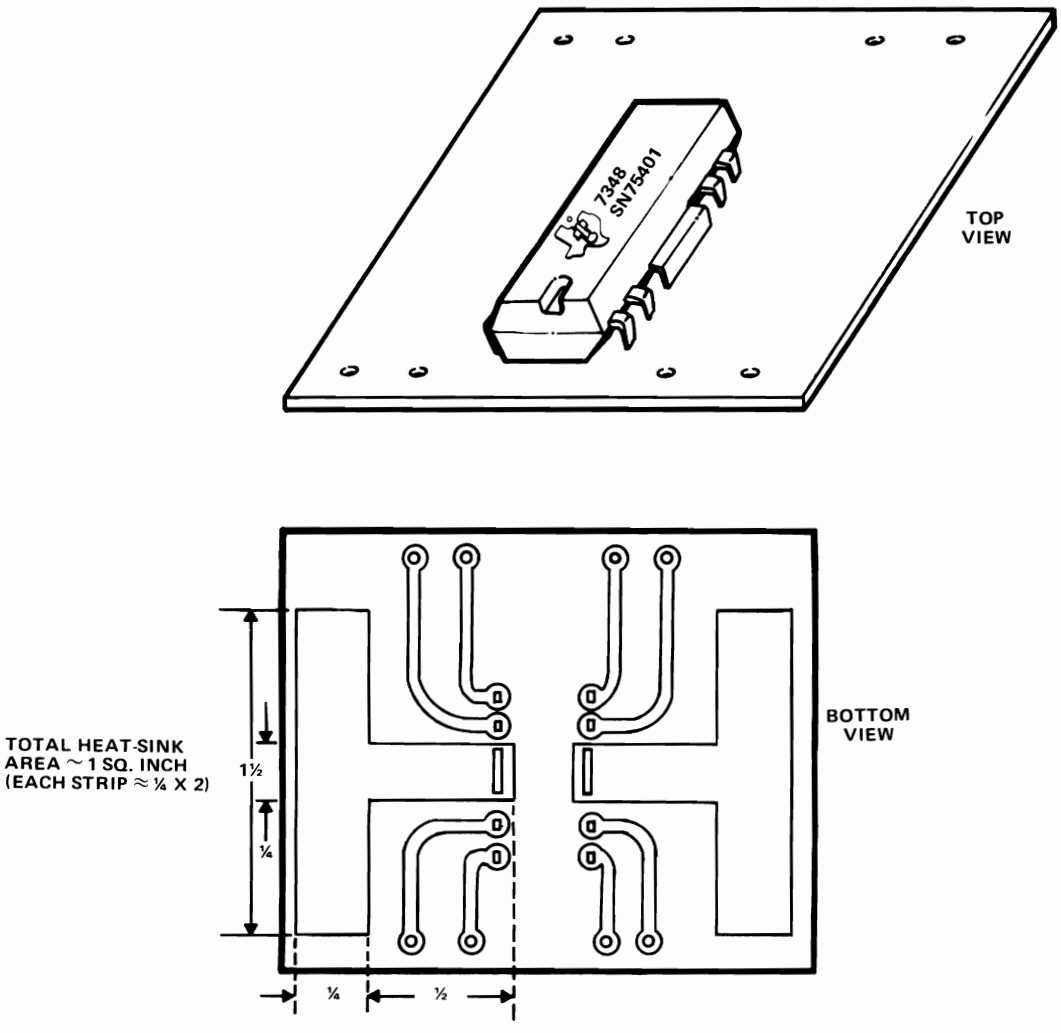


Figure 7.5. Typical PC Board Heat Sink for SN75401 and SN75411 Series Devices

With the heat sink depicted in Figure 7.6, the maximum power dissipation was increased to 2.29 watts, and is derated at 28.6 mW/°C from 70°C to 125°C ambient.

Although power dissipation is often a primary design consideration, care must be taken to assure that the current and voltage limits of the device are not exceeded.

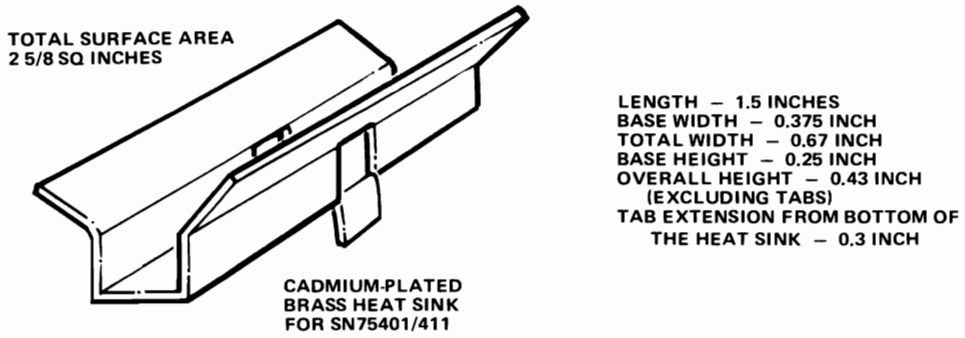


Figure 7.6. Typical Heat Sink for Type ND Package

7.2 APPLICATIONS

7.2.1 Relay Drivers

Probably the most popular use of peripheral drivers is as an interface between TTL circuits and relays for power-control applications. Figure 7.7 shows the basic circuit. Punch-card relays, power switching, and electromechanical controls are examples of this application.

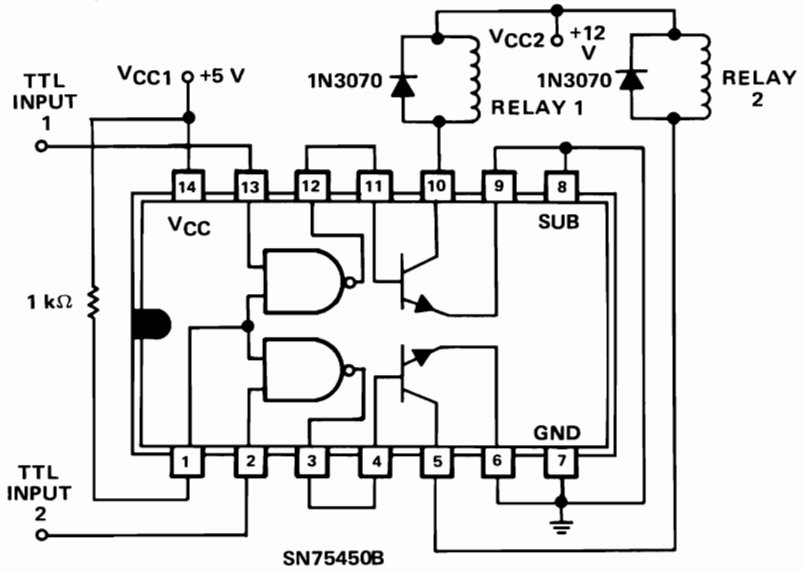


Figure 7.7. Dual-Channel TTL-to-Relay Interface

The 1N3070 diodes are used to clamp the collector voltages during turn-off, to prevent damage from the transient voltages that occur during this time. Even with the collectors clamped with 1N3070 diodes, the turn-off transient will cause the collector voltage to swing as much as V_{CC2} +1 volt. When using the SN75450B the maximum V_{CC2} allowable is the maximum collector switching voltage minus 1 volt, or 19 volts. For applications requiring the typical 24-volt V_{CC2} supply, the SN75460, with a transient capability of 30 volts, would be recommended.

In some systems power-supply failure or sequencing may result in the output V_{CC2} collector supply being on while the gate supply V_{CC1} is off. Under this condition the collector-to-emitter breakdown is generally lower because of the increase in base-terminating impedance resulting from the gate being off. Figure 7.8 shows a practical method of preventing complete loss of gate power while V_{CC2} is on; the zener diode yields a 4- to 5-volt supply level to the gate during V_{CC1} power failure.

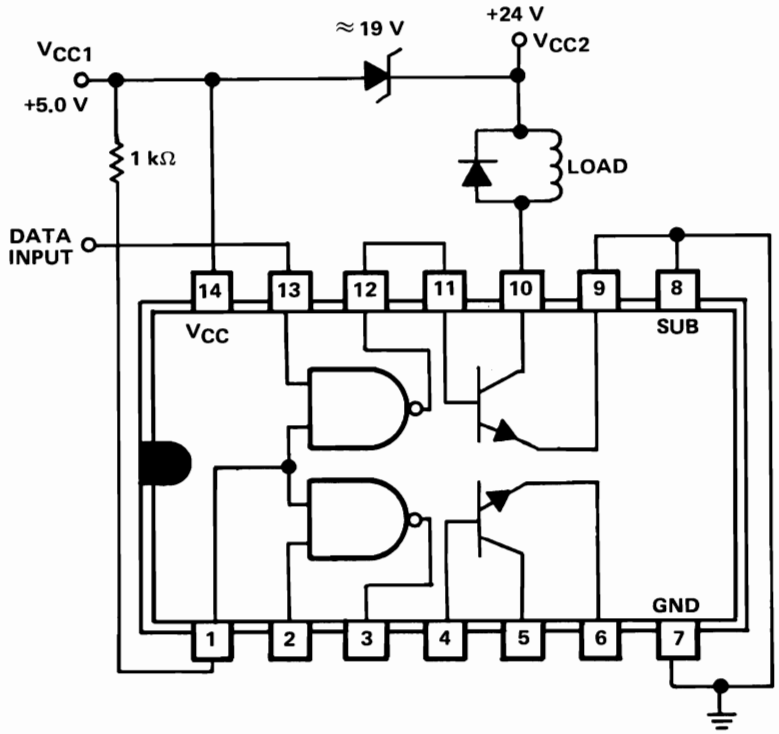


Figure 7.8. V_{CC1} Loss Protection

In some applications involving the switching of inductive loads, the fast rise time and high-voltage transient occurring during turn-off can force the output transistor into a secondary breakdown condition. In such cases the collector voltage reaches V_{CC2} levels within a few nanoseconds. To prevent undesired breakdown the

collector-voltage slew rate should be reduced to 1 volt per nanosecond or less. Thus the gate has sufficient time to provide a low base-to-ground impedance before the collector voltage is extremely high, and collector-to-emitter breakdown is prevented. To accomplish this a 500- to 1000-pF capacitor from the collector of the output transistor to ground is usually adequate (see Figure 7.9).

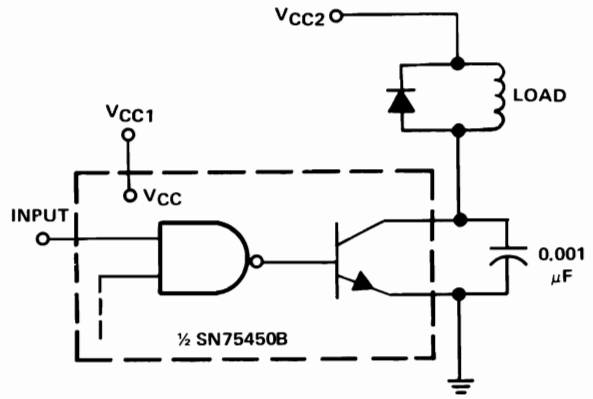


Figure 7.9. Capacitor Prevents Premature Collector-to-Emitter Breakdown

7.2.2 Lamp Drivers

Another popular general application of peripheral drivers is for driving lamps. Their 300- or 500-mA current capability is sufficiently high for most pilot lamps. Figure 7.10 shows a basic lamp-driver application.

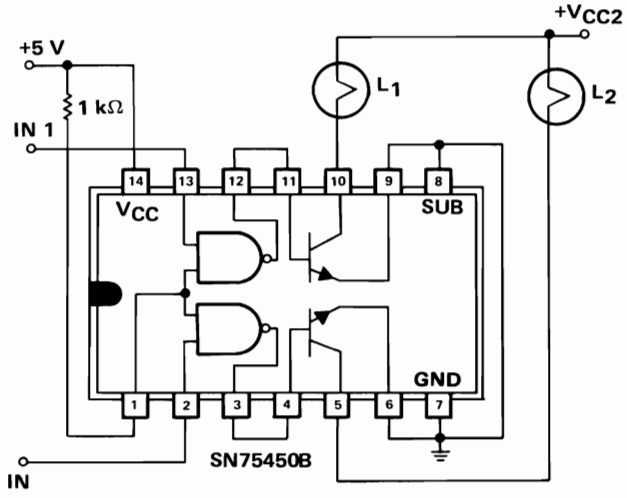


Figure 7.10. Dual-Channel Lamp Driver

Note that in any lamp-driver application the turn-on surge current of a cold lamp may be as much as 10 times the normal on current; a 100-mA lamp may have a 1-amp turn-on surge. Peripheral drivers can handle 100-mA operating currents, but a 1-amp surge is far more demanding. The normal, continuous collector-current maximum is 300 or 500 mA, although a 500- or 800-mA (maximum) surge current may be sustained for a 10% duty cycle not to exceed 200 milliseconds. Current peaks exceeding these maximums may cause device deterioration.

Several methods can be employed to limit surge currents when using peripheral drivers. These methods allow 200- to 300-mA lamps to be driven without exceeding the surge limits of the devices. With the basic SN75450B, SN75460, or SN75470, availability of gate output and base lead, as well as the emitter, allows use of several methods of current limiting. One method is to place a current-limiting resistor between the gate output and the transistor base, as shown in Figure 7.11. With an operating load current of 100 mA, a typical h_{FE} of 50 for the output transistor, and selecting 250 mA as the peak surge, the value of the base resistor can be determined from the following equation:

$$R = \frac{V_{OH(Gate)} - V_{BE}}{I_{BE(Limit)}}$$

where

$V_{OH}(Gate) = 3.3$ V (typical)

$V_{BE} = 0.85$ V (typical)

$$I_B\,(Limit) = \frac{I_C(Limit)}{h_{FE}} = \frac{250\text{ mA}}{50} = 5\text{ mA}$$

Therefore:

$$R = \frac{3.3 - 0.85}{0.005} = 490, \text{ or} \approx 500\ \Omega$$

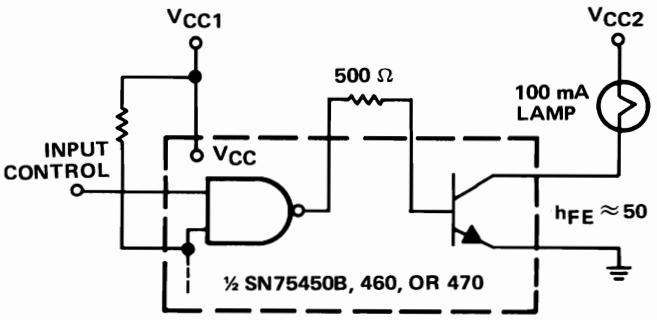


Figure 7.11. Base Resistor Surge Limiting

This method is not the best, because of lack of control over critical parameters. A worst-case condition of low V_{BE}, high h_{FE}, and high gate output would result in peak surges in excess of 500 mA.

Figure 7.12 shows a configuration that is less susceptible to variations in parameters. The emitter resistor is small enough to be of little significance at the steady-state on level, but will limit the peak levels. In this example a GE1815 lamp

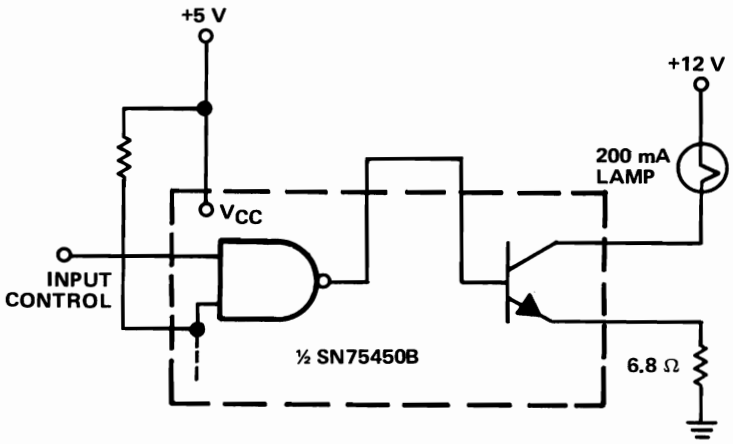


Figure 7.12. Emitter Resistor Surge Limiting

was used. The actual steady-state current was 191 mA. With a typical gate V_{OH} of 3.3 volts and a V_{BE} of 0.95 volt (at 200 mA) the transistor will saturate and limit when its emitter voltage reaches $V_{OH} - V_{BE}$, or 2.35 volts, this occurring at V_E/R_E, or about 345 mA. Figure 7.13 shows the output current waveform.

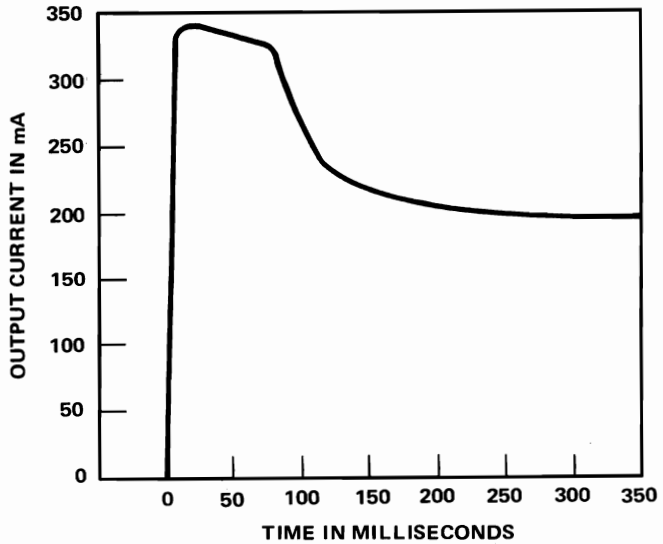


Figure 7.13. Output Current Waveform with Emitter Resistor Surge Protection

In this example the peak surge is sustained for about 150 milliseconds. As the lamp warms, its impedance rises and the load current drops rapidly to the steady-state level. Even with worst-case parameters the surge current would be under 500 mA. The efficient performance of this type of current limiting explains its popularity for lamp-driver applications.

Improved accuracy and consistent performance can be achieved by utilizing one of the output transistors as a current-sensing device to clamp the lamp driver, as shown in Figure 7.14. In this application the lamp current must flow through the 1.9-ohm resistor in the emitter of the lamp driver. The first advantage is that the resistor is smaller than that required in the previous circuit, and has even less effect on the steady-state operating level. The base-emitter junction of Q2 is connected across the 1.9-ohm resistor, with its collector tied to the base of Q1 in a typical current-limiting mode. A V_{BE} of only about 0.6 volt begins to turn Q2 on, clamping the base drive into Q1. Clamping occurs at an output current (I) equal to $V_{BE(clamp)}/1.9\ \Omega$, or $0.6\ V/1.9\ \Omega$; the output clamp level is then 316 mA. As in the previous application the surge current lasts for about 100 milliseconds before decreasing rapidly to the quiescent level of 190 to 200 mA.

Two important precautions should be kept in mind when using this type of surge protection: (1) Do not allow surge currents to exceed the driver surge rating under any conditions; and (2) be sure that current limiting does not take place during steady-state operation, as this would increase driver power dissipation and could cause failure.

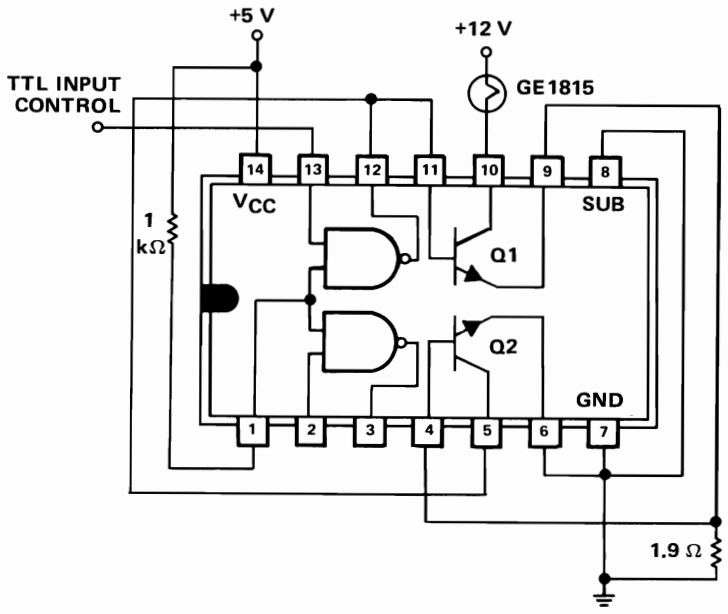


Figure 7.14. Surge-Limited Lamp Driver

Another method is basically to use two switches: one to turn on the lamp with current limiting and the second to turn on, after a delay, without current limiting. This eliminates the effects of parameter variation without reducing the quiescent operating level of the lamp. Such a circuit, using the SN75452, is shown in Figure 7.15. A logic 1 input turns on Q1 immediately, while Q2 is delayed by the input RC network, allowing about 200 milliseconds of limited-current warm-up before turning the lamp fully on. Figure 7.16 shows the current levels versus time, and the effect of the warm-up mode on resulting peak levels.

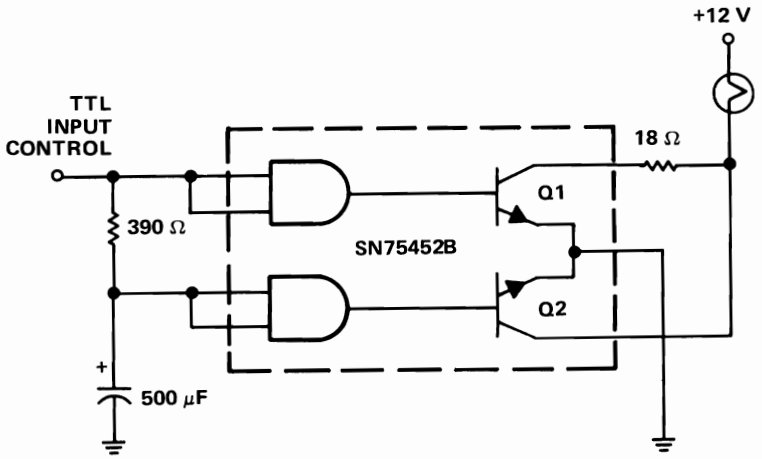


Figure 7.15. Lamp Driver with Warm-Up Circuit

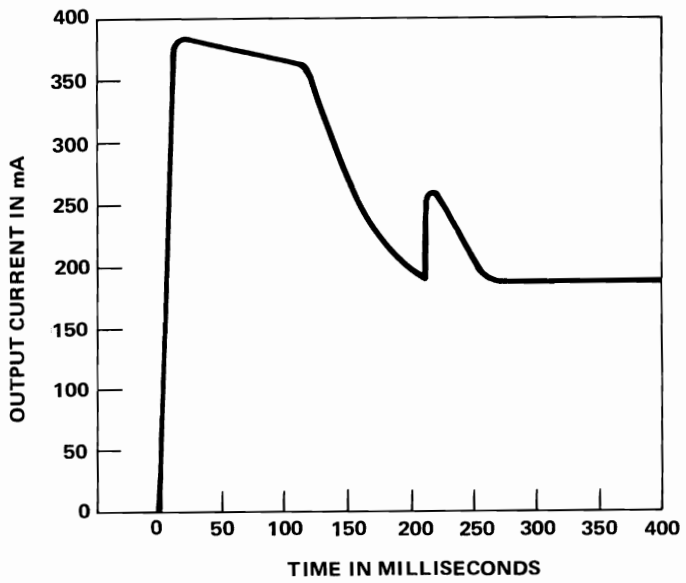


Figure 7.16. Output Current Waveform with Warm-Up Circuit

Another interesting lamp-driver application is depicted in Figure 7.17, showing the SN75450B as a panel-light intensity control. Controllable feedback around the gate allows its operation in the linear region, thus providing variable drive to the output transistor. An emitter resistor as shown may be used to limit initial turn-on surges. In this application a large amount of power will be dissipated in the output transistor at half-power operating levels.

Care must be taken not to exceed the 800-mW total power-dissipation capability of this package. In a typical application the gate output will be only about 2.2 volts, because of operation within the linear region. A control setting of about 280 ohms puts the gate in its linear region. A control setting of 100 to 150 ohms turns off the lamp, and a setting of 700 to 800 ohms will yield a full-on condition.

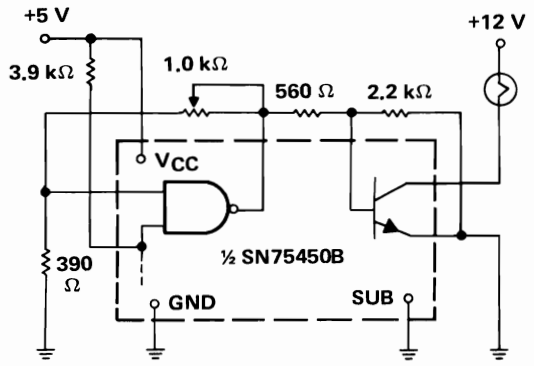


Figure 7.17. Light Intensity Control

7.2.3 Level Shifting

Level shifting between different voltages and polarities is another popular application of SN75450B series devices. Two popular logic levels are negative-level MOS and positive-level TTL. Interfacing between them may be accomplished with the circuits shown in Figures 7.18, 7.19, and 7.20. Figure 7.18 is a negative-level MOS-to-TTL interface that takes advantage of the substrate availability of SN75450B/460/470 devices. The resistor divider network on the input and base of the transistors will level-shift the negative MOS levels to positive levels. As the transistors are switched on and off their collectors swing TTL-compatible levels, providing the necessary gate drive.

A 39-pF capacitor is used across the series input resistor to speed up the leading edges of input pulses. Satisfactory operation is obtained at frequencies up to 10 MHz. Note that the substrate is connected to the MOS negative supply, providing the necessary bias to keep the substrate diodes reverse biased.

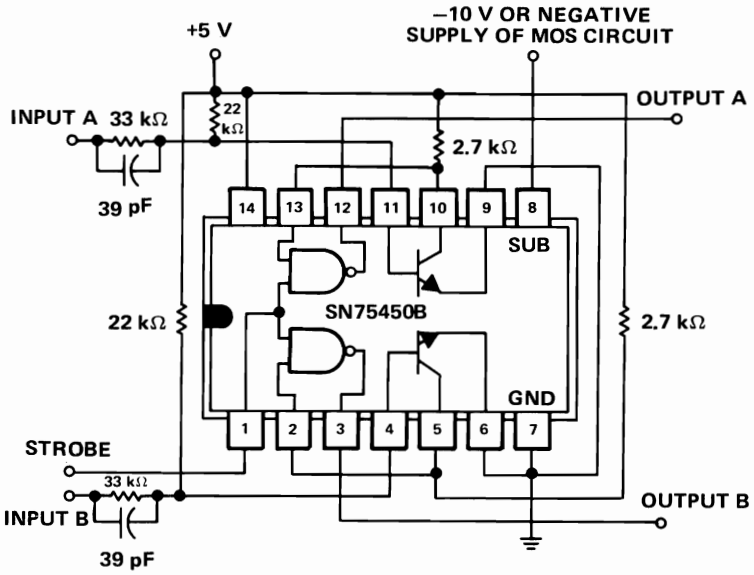


Figure 7.18. Dual MOS-to-TTL Driver

Figure 7.19 is an example of a dual TTL-to-MOS interface, with gate outputs level-shifted through zener diodes to proper drive levels for the output transistors. Transistor emitters, as well as the substrate, are connected to the negative MOS supply. In this example the collectors are terminated to the +5-volt supply, although they could be terminated to ground.

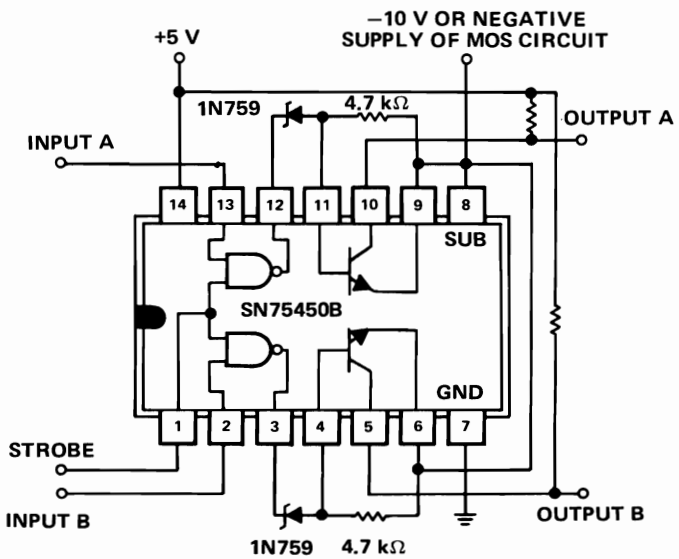
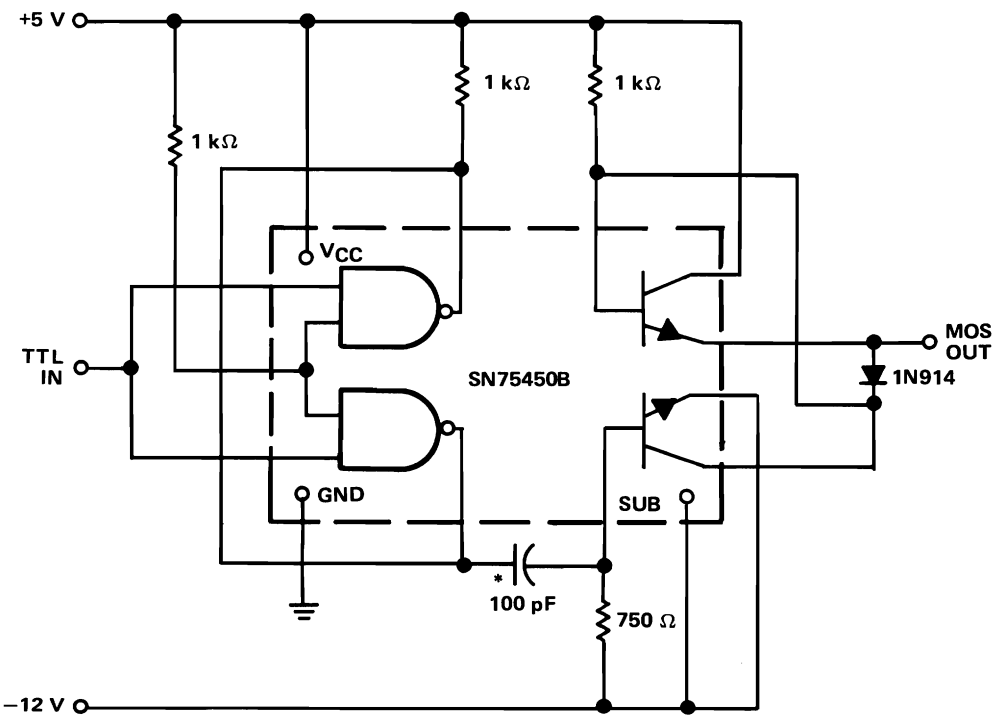


Figure 7.19. Dual TTL-to-MOS Driver

Output swing will be from near +5 V to near $-V_{CC}$, or −10 V in this example. The zener diodes selected must allow proper level shifting from TTL output levels to $(-V_{CC} + V_{BE})$. The major disadvantage of this circuit is its slower operating speeds caused by the zener diodes. Active pull-down provides fast switching to low negative levels, but the resistive pull-up results in an RC delay in charging any load capacitance to the high or positive level.

A faster TTL-to-MOS interface is shown in Figure 7.20. The ac coupling takes care of the level-shifting problem, and the active pull-up and active pull-down allow fast charging and discharging of capacitive loads. This circuit, operating into a 220-pF load, has output rise time and fall time of 22 and 26 nanoseconds respectively when tested at 5 MHz with a TTL input having a pulse width of 50 nanoseconds. Propagation delays are typically t_{PLH} = 36 ns, and t_{PHL} = 30 ns.



*THIS CAPACITOR VALUE MAY BE ADJUSTED FOR DIFFERENT FREQUENCIES OF OPERATION.

Figure 7.20. High-Speed TTL-to-MOS Interface

7.2.4 Signal Comparison

Another logic application is the comparing or detecting of in-phase logic signals. Figure 7.21 shows the SN75453B OR-function driver; however, several different peripheral drivers can be used to perform similar functions. Used as an in-phase detector, the SN75453B compares two incoming signals and provides a logic 0 output during simultaneous low inputs.

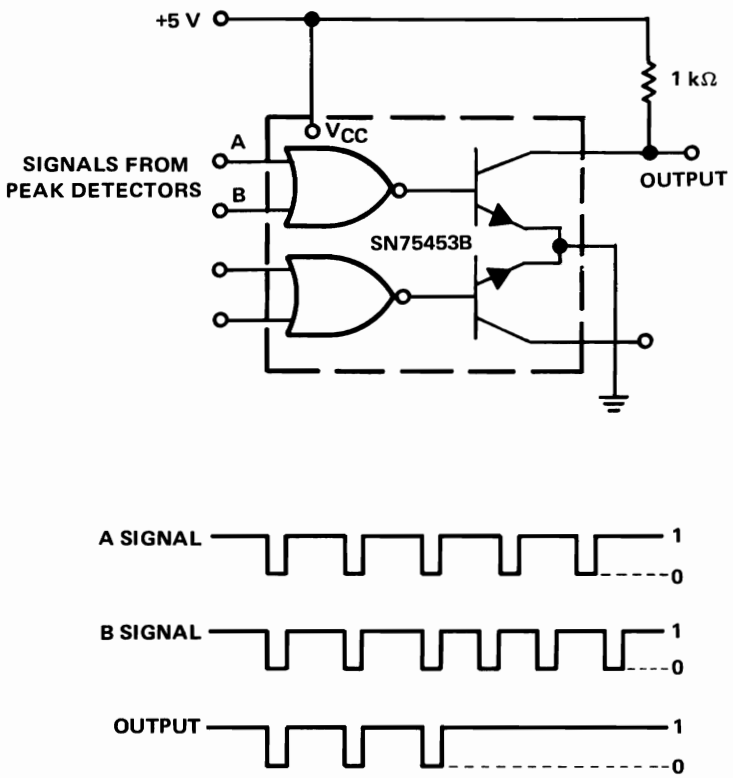


Figure 7.21. In-Phase Logic Detector

7.2.5 Signal Generation

Frequently, where a signal source such as a clock generator for shift registers is required, a simple square wave generator may be implemented using the SN75450B. Figure 7.22 shows that, with a few external resistors and capacitors, the SN75450B can provide a standard TTL-level output from the TTL gates. Both Q and $\overline{Q}$ outputs are available, and therefore two-phase TTL clock inputs can be driven directly from one package.

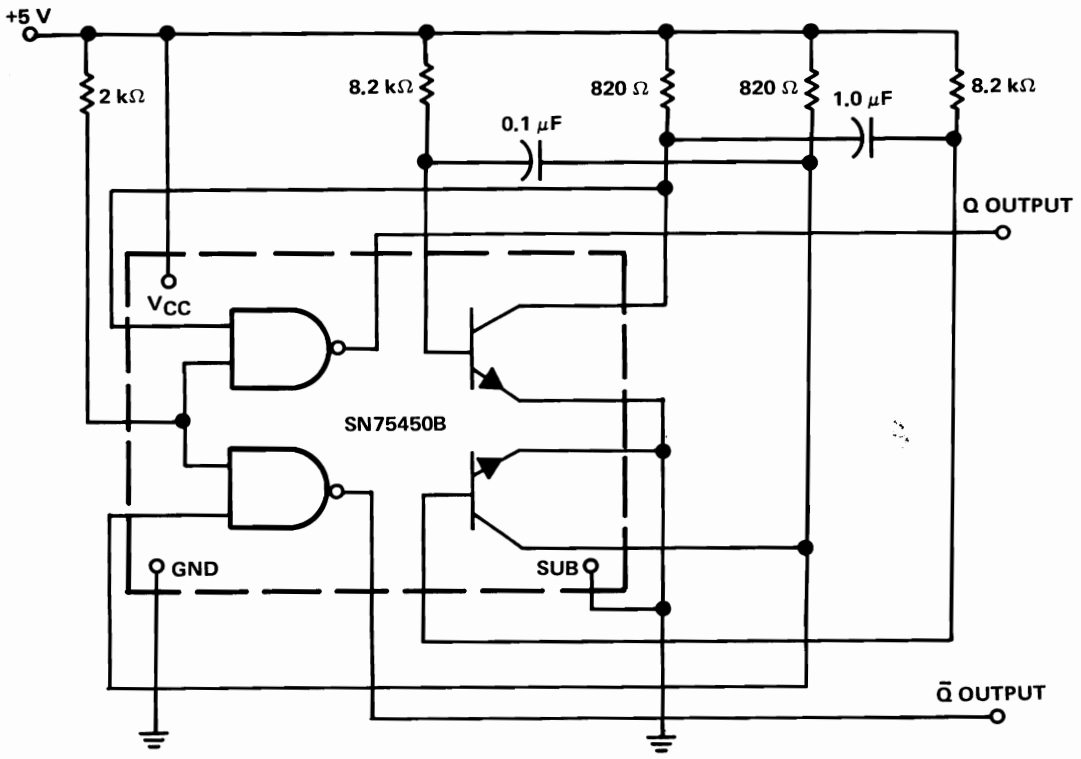


Figure 7.22. Square Wave Generator

7.2.6 Dual-Channel One Shot

The one shot, a function used in many different types of data processing, provides a pulse of fixed duration that occurs immediately following a positive or negative going voltage transition. Figure 7.23 shows an example of this type of function using an SN75450B.

Channel 1 is connected to provide a zero-level output pulse following a negative going input transition, while Channel 2 provides a one-level output pulse following a positive input transition. The uniform output pulses can be used in frequency or voltage conversion, counter circuitry, and other similar applications.

7.2.7 High Current Application

Increased current capability may be obtained by paralleling the output transistors as in Figure 7.24. In this application, using an SN75413, the input must be at a logic 0 level to turn on the output circuit.

$V_{(BR)CEO}$ for the SN75413 is 40 volts. The 1N3070 clamp diode prevents voltage swings above the rated $V_{(BR)CEO}$, and therefore the primary concern is

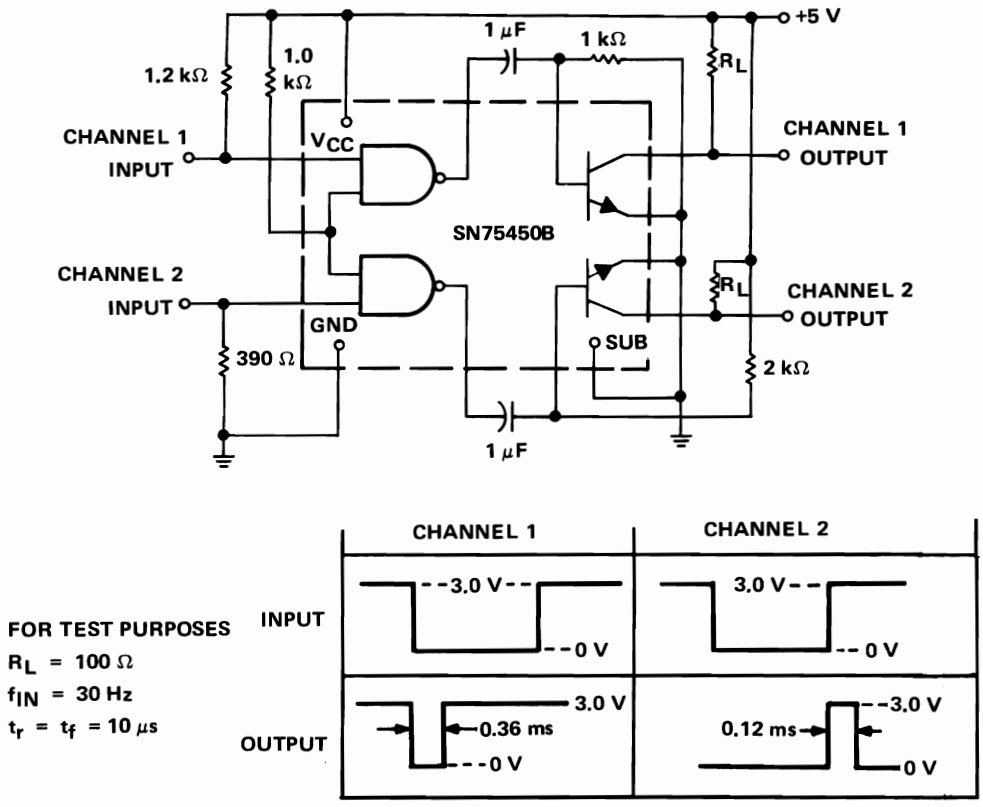


Figure 7.23. Dual-Channel One Shot

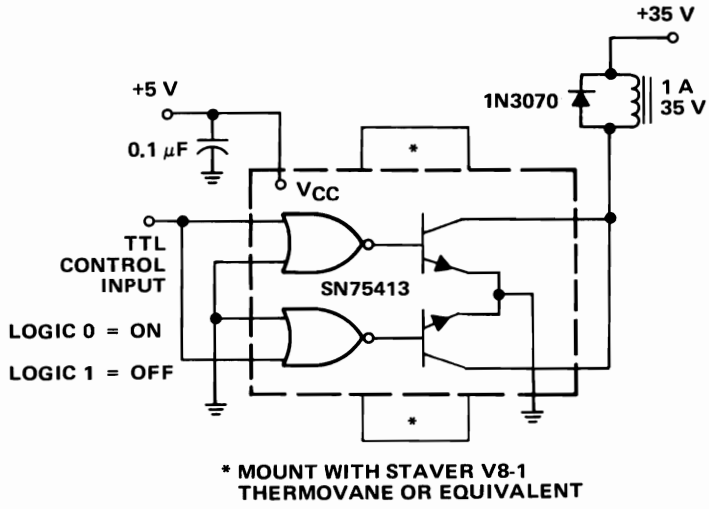


Figure 7.24. Power Solenoid Driver

total package power dissipation. $V_{CE(sat)}$ of the output transistors can be determined from Figure 7.25. With a total load current of 1 amp the individual outputs will be operating at 0.5 amp. Distribution of load current between the outputs will be particularly uniform because of the close matching of transistor characteristics inherent in monolithic processing. It can be seen in Figure 7.25 that $V_{CE(sat)}$ at 500 mA is about 0.55 volt typically. Collector-to-emitter power dissipation will be 0.5 A times 0.55 V, or 275 mW for each output. In addition, the +5-volt supply (V_{CC1}) must furnish about 55 mA for the gate circuitry and output base drives, resulting in an additional 275 mW dissipation. Total package power dissipation in this application is therefore 825 mW typically.

Under worst-case conditions of high $V_{CE(sat)}$ and I_{CC1} levels, the power dissipation could be as high as 1.1 watts. In determining whether these power levels are excessive it is necessary to evaluate the resulting junction temperature. As previously stated, the maximum power-handling capability of the ND package, without an additional heat sink, is only 1.07 watts at 70°C and 333 mW at 125°C. A heat sink would be required to operate at 70°C.

If the V8-1 Thermovane heat sink is used, the junction to ambient thermal resistance, $R_{\theta JA}$, is 35°C per watt. Using the worst-case analysis of 1.1 watts dissipation and a maximum ambient temperature of 70°C, the junction temperature, T_J, is calculated as follows:

$$T_J = T_A + P_d \cdot R_{\theta JA} \qquad \text{or}$$

$$T_J = 70°C + (1.1\ W)\ (35°C/W)$$

$$= 70°C + 38.5°C = 108.5°C$$

This is within the 150°C limit. If, however, we wished to operate over the full military temperature range (to +125°C) the resulting T_J would be 163.5°C. This exceeds the maximum junction temperature, and a more efficient heat sink would be required for operation in this range.

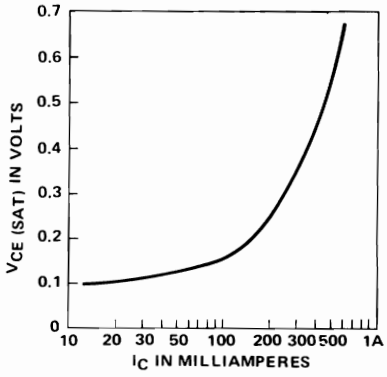


Figure 7.25. Typical $V_{CE(sat)}$ versus I_C for SN75401 and SN75411 Series Devices

8

MOS Interface Circuits

8.1 INTRODUCTION

Many types of high-performance MOS memories have input drive requirements and output levels not directly compatible with TTL or other popular logic levels. MOS shift registers used as circulating memories, MOS random access memories, and MOS calculator chips are typical of the circuits requiring special drive and sense circuits to interface with other logic levels. Interfacing with MOS levels may be accomplished with any of a variety of discrete or integrated-circuit level shifters. Frequently device types employed elsewhere in the system can perform the interfacing function adequately. However, the exact type of interface circuit required will depend on desired performance and input-output requirements of the system. Although the main emphasis in this chapter is on MOS/TTL interfacing, some discussion of MOS to ECL and CMOS levels is included. Circuits for interfacing directly between MOS and readout devices such as VLEDs and thermal print heads are also described.

Many of the MOS interface devices can be used to perform other functions. A number of these applications have been included in this chapter to indicate the versatility of these devices.

8.2 CONVERSION TO MOS LOGIC LEVELS

8.2.1 General Driver Requirements

MOS inputs are capacitive, and clock inputs generally have more capacitance than data inputs. Clock input capacitances may be 60 pF or greater for some devices. MOS drivers must be capable of operating into such loads and in some cases drive several inputs in parallel. For minimum switching times, t_r and t_f, it is desirable to

have both active pull-up and pull-down for the MOS driver output. Although some discrete devices have been used, power, speed, and economic factors have led to use of monolithic integrated-circuit drivers for TTL-to-MOS interfacing. Two basic types of drivers are required — one for negative-level and one for positive-level logic.

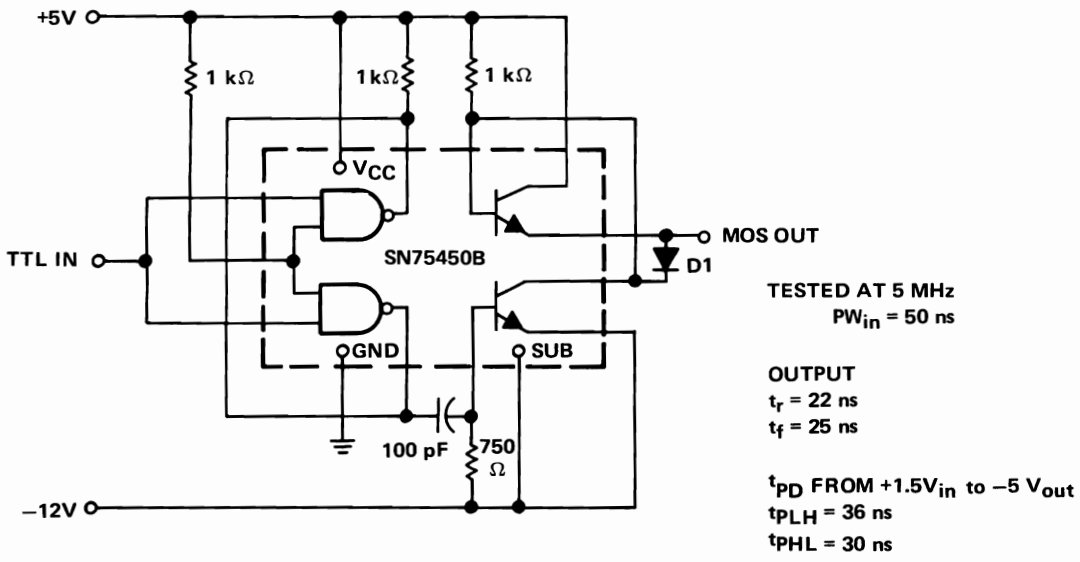


Figure 8.1. TTL-to-MOS Clock Driver Using the SN75450B

8.2.2 Driving Negative-Level MOS Logic

SN75450B Driver – The SN75450B peripheral driver (Figure 8.1) provides the high-speed negative drive required by many MOS shift registers. Level shifting from TTL logic levels to negative MOS logic levels is accomplished by ac (capacitive) coupling between the TTL gates and the output drive transistors of the SN75450B. Adjustment of the coupling capacitor to achieve an RC value approximately equal to twice the desired pulse width will yield proper output characteristics. For example, the 100-pF capacitor and 750-ohm base termination shown in Figure 8.1 have an RC time constant of 75 ns. The ideal frequency is $(2\,RC)^{-1}$ or about 6.67 MHz. However, good performance may be observed from 4 to 8 MHz.

In the configuration shown in Figure 8.1 the output swing will be from −10 volts to +4 volts. As the pull-down transistor is biased on, it goes into saturation, pulling the output toward the negative supply. The load capacitance becomes charged and serves as the source of bias during the next half of the cycle. When the pull-down transistor is turned off, any negative charge on the load capacitance will bias the pull-up transistor on, driving the output toward the positive supply. Charging of the load capacitance toward zero or the positive supply will occur quickly because the

saturation impedance of the pull-up transistor is low. When the pull-down transistor is forward-biased again, the forward voltage drop through D1 will provide reverse bias to the active pull-up transistor, holding it off.

SN75450B Two-Phase Driver – Figure 8.2 shows a pair of SN75450B devices being used in a two-phase clock driver system typical of many shift-register applications. In this configuration two 25% duty-cycle pulses are developed with 180° phase difference. The waveforms at various points in the circuit are shown in Figure 8.3. Pulse-width stability over the 0 to 70°C temperature range is characteristic of this circuit.

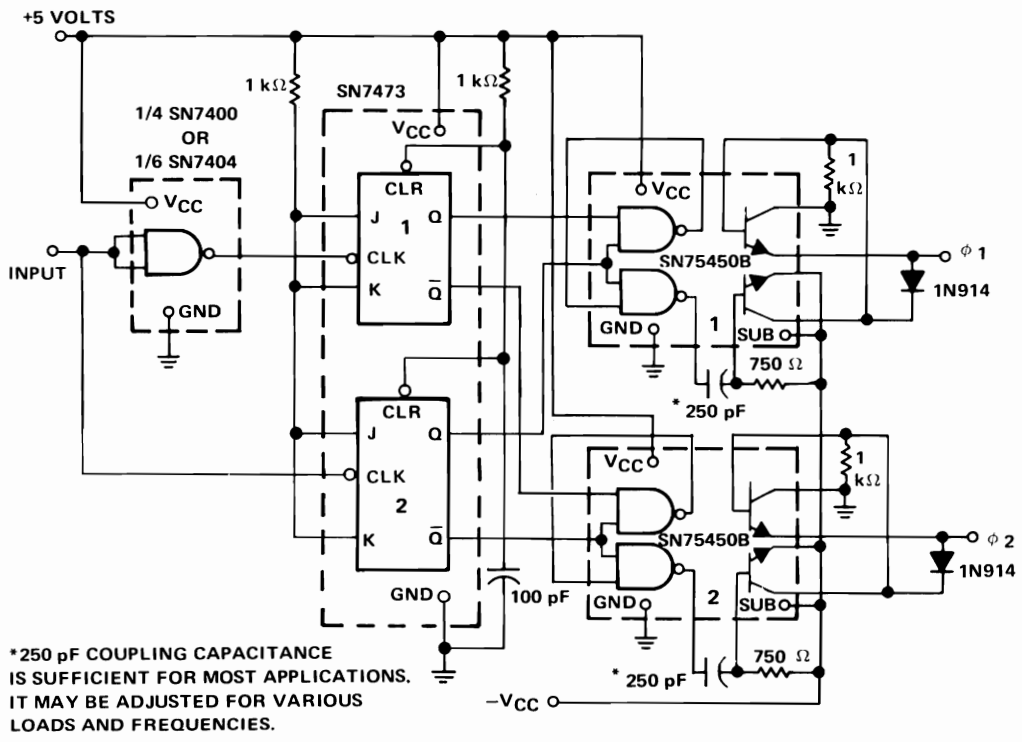


Figure 8.2. Two-Phase MOS Clock Driver

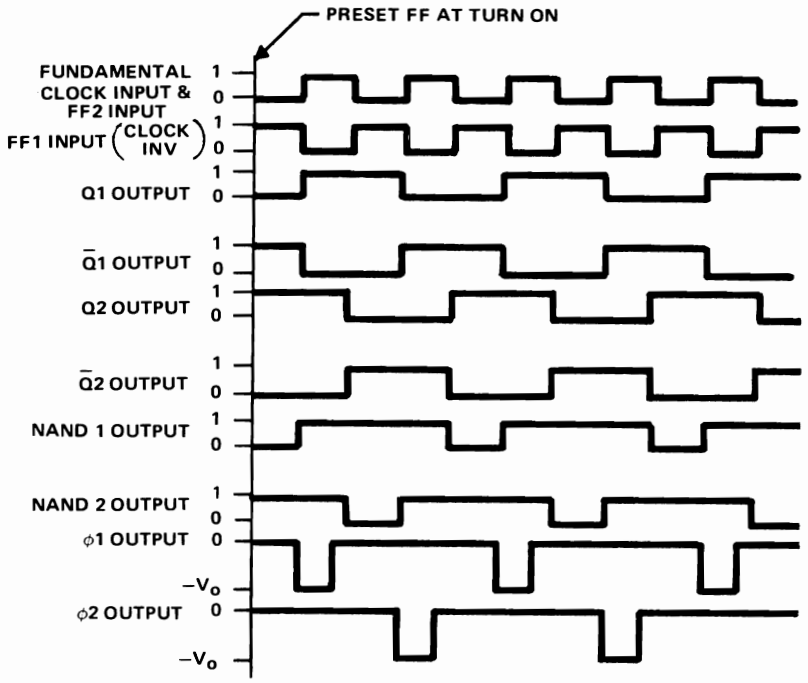


Figure 8.3. Waveforms in Circuit of Figure 8.2

8.2.3 Driving Positive-Level MOS Logic

SN75451B Driver – The circuit in Figure 8.4 combines the economical general-purpose SN75451B integrated circuit with the popular 2N5449 *Silect*® transistor to form a high-speed driver with short-circuit protection and the ability to drive a large number of clock inputs. Base pull-up resistor R_B may be adjusted to provide proper drive for various loads. The equation for determining R_B is

$$R_B = \frac{h_{FE}\left[V_{BB} - (V_D + V_{BE} + 22\Omega \cdot I_D)\right]}{I_D}$$

For example, let us assume the following:

V_{BB} = 22.5 V (base-supply voltage) I_D = 30 mA (output-drive current)
V_{SS} = 20.0 V (source-supply voltage) h_{FE} = 100 (2N5449)
V_D = 19.0 V (output-drive voltage) V_{BE} = 0.7 V (2N5449)

Therefore:
$$R_B = \frac{100\ (22.5\ V - 19.0\ V - 0.7\ V - 30\ mA \cdot 22\Omega}{30\ mA}$$
$$= 7.13\ k\Omega$$

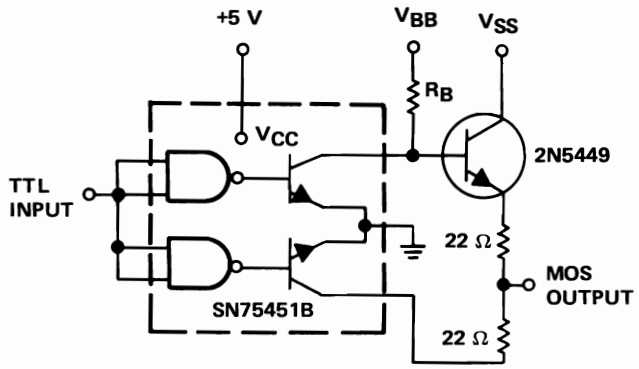


Figure 8.4. TTL-to-MOS Clock Driver Using an SN75451B and a 2N5449

SN75361A Driver – The ideal MOS driver circuit is totally monolithic, requiring no external components. The SN75361A (Figure 8.5) is such a device. It operates from standard +5 volts for V_{CC1} and will accept a TTL or DTL input. The V_{CC2} supply is connected to the required MOS level, typically +16 to +20 volts. The SN75361A output circuitry is active in both the pull-up and pull-down modes to provide high-speed operation into large capacitive loads. A typical connection is shown in Figure 8.6 where the SN75361A is driving a data input line of the 1103 dynamic RAM. The SN75361A (Figure 8.7) is available in the 8-lead plastic (P) and 14-lead plastic (N) packages. The pin-out has been arranged with the inputs on one side of the package and the outputs on the other for convenient board layout. Figure 8.8 shows the device power dissipation versus frequency and capacitive loading for a V_{CC2} of 20 volts. It should be noted that power dissipation is substantially affected by V_{CC2} levels. A 25% increase in V_{CC2} may result in a power-dissipation increase of 50% in some cases.

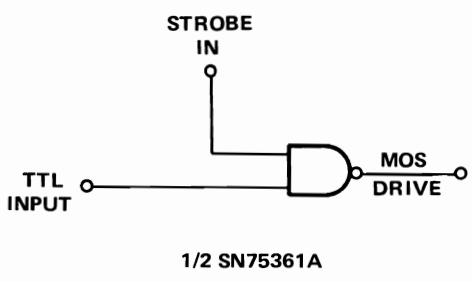


Figure 8.5. TTL-to-MOS Clock Driver Using the SN75361A

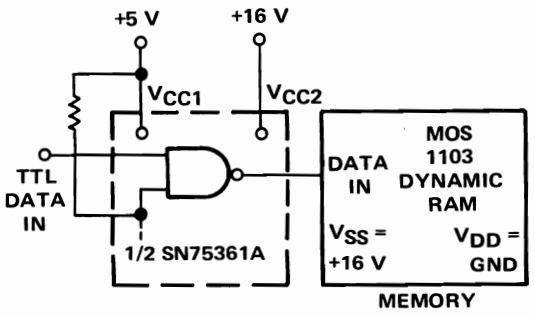


Figure 8.6. The SN75361A as an MOS Memory Driver

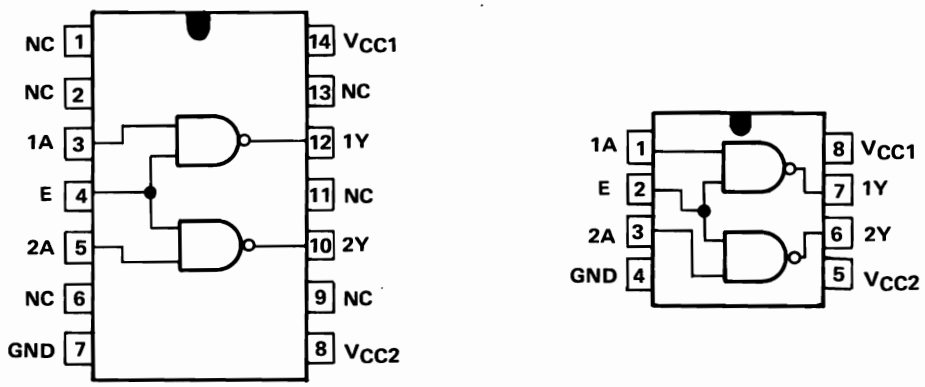


Figure 8.7. Functional Diagram and Pin Assignments: SN75361A

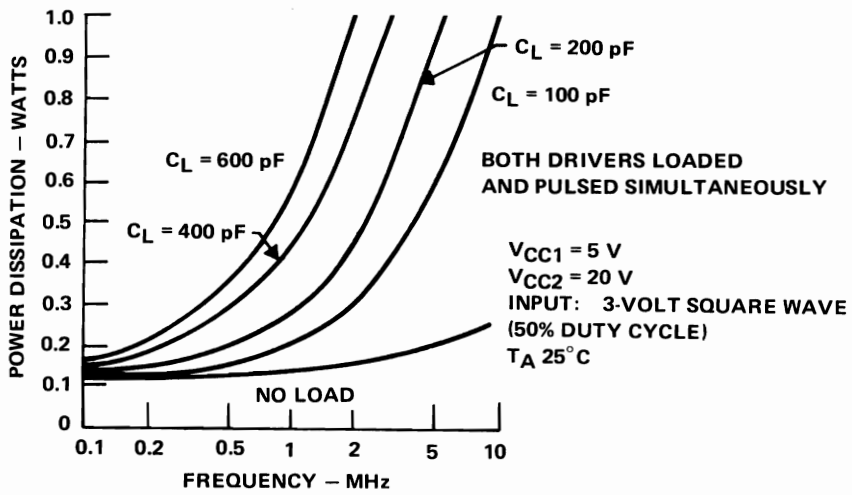


Figure 8.8. SN75361A Power Dissipation versus Frequency and Loading

SN75365 Driver – For additional reduction in package count, there is a quad version of the SN75361A, the SN75365 (Figure 8.9). Although basically the same as SN75361A, it has several advantages. The device has a V_{CC3} terminal as well as the high-level V_{CC2} and TTL-level V_{CC1} inputs. V_{CC3} may be tied to V_{SX} or similar supply, generally a few volts above V_{CC2}, to provide more base drive and higher output levels during sourcing. Typically V_{CC3} equals V_{CC2}+2.5 volts. The SN75365 has a low standby power of 20 milliwatts. Uniform propagation delay for the four stages is an added advantage. All input-to-output delays are typically within 3 nanoseconds of each other.

Figures 8.10 and 8.11 show power-dissipation curves versus loading and frequency for all channels operating simultaneously. As can be seen in these examples, increased supply voltages or additional base drive (V_{CC3}) will result in increased power dissipation. This increased power dissipation may be desirable in many applications to achieve the required speed and output accuracy.

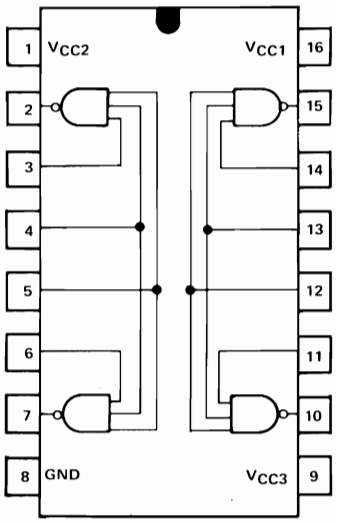


Figure 8.9. Functional Diagram and Pin Assignments: SN75365

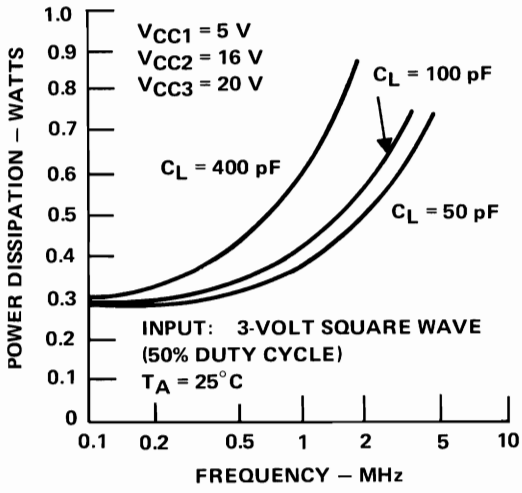


Figure 8.10. SN75365 Power Dissipation versus Frequency and Loading

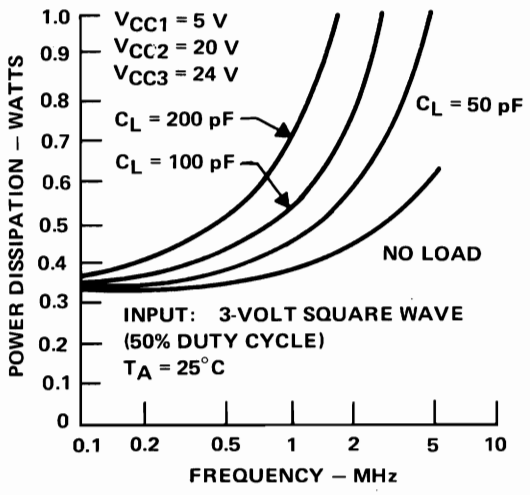


Figure 8.11. SN75365 Power Dissipation versus Frequency and Loading

Driver Selection – Specifications for the three TTL-to-MOS circuits just described are given in Table 8.1. Key features in selecting a driver are listed. For example, the 1103 data sheet indicates that the driver must be capable of driving from supply levels of up to +16 volts (V_{SS}), and operating at high switching speeds (rise and fall times of less than 100 ns typically). Circuits listed in Table 8.1 having +16-volt capability are the SN75361A and SN75451B. The SN75451B might be preferred if it were being employed elsewhere in the system. If speed, power dissipation, and minimum component count were primary factors the SN75361A would be chosen.

Table 8.1. Characteristics of TTL-to-MOS Converter Circuits

CIRCUITS	SN75451B				SN75361A				SN75450B			
Load "C" in pF	50	100	700	2K	50	100	700	2K	50	100	700	2K
Output t_r ns	29	30	55	114	9.5	11	26	53	75	75	150	330
Output t_f ns	8.2	11	37	79	7	10	25	66	22	26	200	330
t_{PLH} ns	29	31	47	79	15	16.5	26	51	25	25	30	50
t_{PHL} ns	21	23	33	50	7.0	8.6	19	40	30	30	50	200
Max. Freq. MHz	9.1	9.0	5.0	2.3	12.5	12	6.2	1.2	8.0	8.0	1.2	7.1
Storage Time ns	20	21	24	31	6.6	6.7	9.6	12	20	20	33	40
+ Supply Volts	5/19/16				5/16				5			
+ Supply mA*	28/10/38				11/9.3				30			
–Supply Volts	–				–				23			
–Supply mA*	–				–				21			
V_{OL} No Load	+0.1 V				+0.1 V				–21 V			
V_{OL} I_L = 3 mA	+0.1 V				+0.1 V				–20 V			
V_{OH} No Load	+15.9 V				+15.4 V				+4.6 V			
V_{OH} I_L = 3 mA	+15.9 V				+14.4 V				+4.0 V			

*At 50% duty cycle

SN75361A Series Devices – Several versions of the SN75361A are available, providing additional features required in different types of MOS systems. Proper selection of a particular driver is keyed to three or four basic features: number of channels per package; type of logic; V_{CC2} supply levels; and availability of a V_{CC3} pull-up for increased speed and output capability.

Table 8.2 lists key features of the SN75361A series device types. In many applications more than one type of driver could be used. Special device features, such as the availability of V_{CC3} pull-up to improve speed, or quad packages to reduce space or package count, may determine the optimum device for a particular application. The examples listed are typical of the many possible applications. When an SN75361A-type device is used its inherent high-speed characteristics in

Table 8.2. Dual and Quad Bipolar-to-MOS Memory Interface Circuits

Circuit	Package Type	No. of Functions	Interface Applications	V_{CC2} Max.	V_{CC3} Pull-Up	Typical Memory Applications
SN75361A	J, N, P	Dual	TTL-MOS	+24	No	1103, TMS4062, AMS6002
SN75362	J, N, P	Dual	TTL-MOS	+24	Yes	1103, TMS4062, TMS7001
SN75363	J, N, P	Dual	TTL-MOS	+15	No	TMS4030 C. E. Clock
SN57365	J, N	Quad	TTL-MOS	+24	Yes	1103
SN75367	J, N, SB	Quad	TTL-CMOS, 3 State	+15	No	CMOS Circuits
SN75368	J, N	Dual	ECL-MOS	+24	Yes	ECL 10K to 1103, TMS4062, TMS7001 ECL 10K to TTL
SN75369	J, N, P	Dual	Dual Current-to-MOS	+24	No	AMS6003 Clock Lines
SN75370	JB, N	Dual	TTL-MOS Read/Write	+24	No	TMS4062 I/O Lines

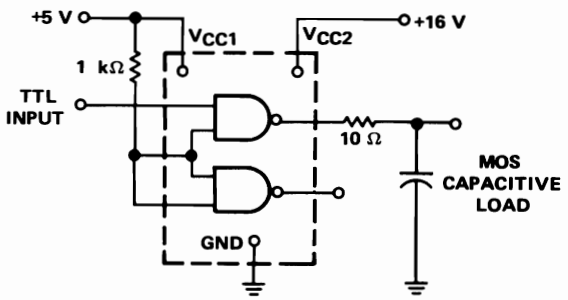


Figure 8.12. Basic SN75361A Application

conjunction with the load characteristics may result in an overshoot of the drive signal. If a damping resistor is used in series with the output, as shown in Figure 8.12, overshoot is reduced to an insignificant level. The resistance required is generally small, a good approximation of the value required being

where: $$R_D = 2\sqrt{L_L/C_L}$$

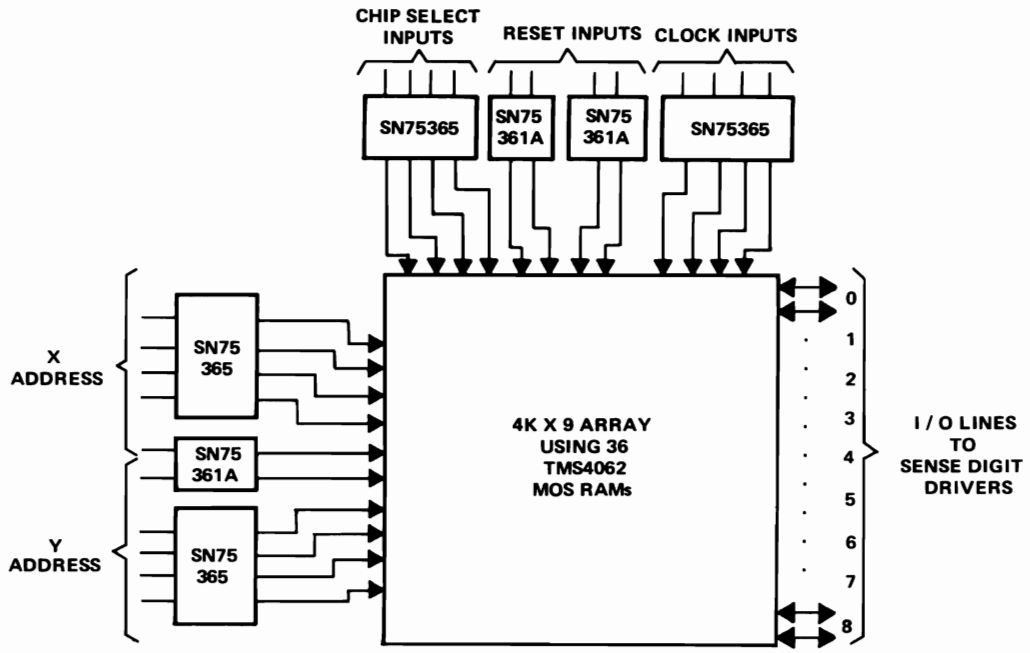
R_D = series damping resistance

L_L = inductance of the load or line being driven

C_L = capacitance of the load.

A typical value for most applications is 10 ohms.

Some comparisons may be made in package counts required when using the SN75361A dual or SN75365 quad drivers. In a typical 4K x 9 array of the 1103 MOS RAMs, a total of only 16 SN75361A driver packages is required to drive data inputs, address inputs, chip enable, precharge, and read/write inputs. In the same arrangement, but using SN75365s, only eight driver packages are required. However, this ratio does not always apply. As can be seen in the application of a 4K x 9 array of TMS4062 MOS RAMs (Figure 8.13), the higher input capacitance of reset inputs and a desired high-frequency operation may cause excessive power dissipation for the quad device and thus necessitate use of an SN75361A.



PACKAGE COUNT

TMS4062	36
SN75365	4
SN75361A	3

Figure 8.13. Typical Driver Application with TMS4062 RAMs

In a special case (Figures 8.14 and 8.15) where the 6003 RAM requires a three-phase clock input drive, only six SN75361A packages are required for a large 8K by 17 bit MOS memory. The block diagram (Figure 8.15) shows how easily the hookup is accomplished when taking advantage of the drive capability of the SN75361A.

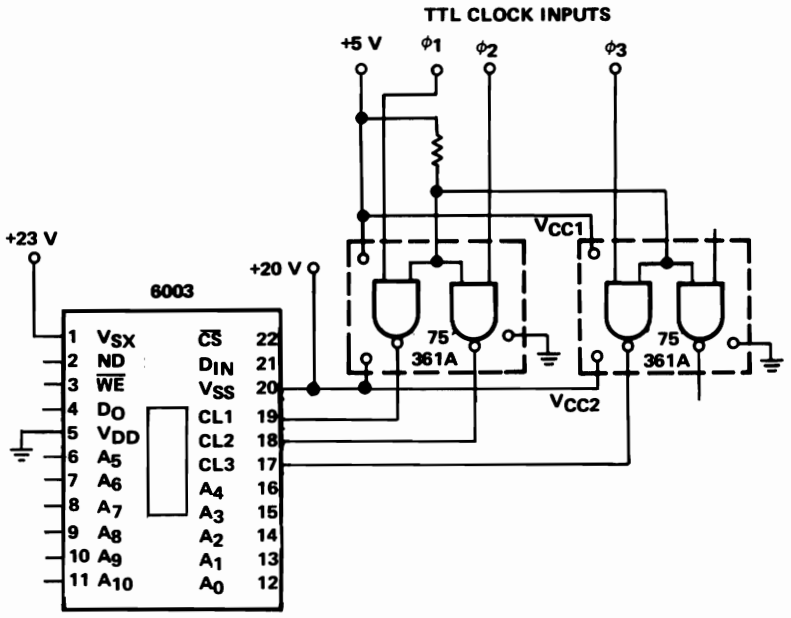


Figure 8.14. Three-Phase Clock Driver for the 6003 RAM

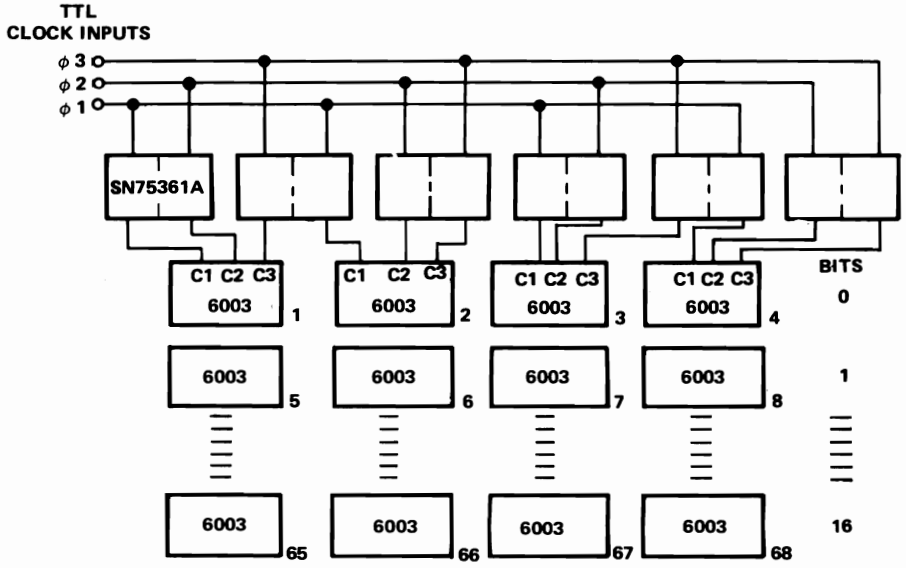


Figure 8.15. Three-Phase Clock Driver for an 8K x 17 Bit MOS Memory

The special features of each device type in the SN75361A series will provide the drive capability needed in a wide variety of applications. Following are some of the features to be considered for each device:

SN75362: Similar to the SN75361A but with V_{CC3} pull-up available. This permits the faster speeds generally handled by the SN75365, and greater load-handling capability, as there are only two channels and total power dissipation is less. Where larger MOS arrays are required the SN75362 has an advantage.

SN75363: Basically like the SN75361A except that it has been designed specifically for use as a chip-enable clock driver for the TMS4030 MOS RAM. It may be used as the address, control, or timing input driver for several other types of MOS RAMs. It features V_{CC1}, V_{CC2} and V_{CC3} supply terminals for compatibility with the TMS4030 power supplies.

SN75367: A quad TTL-to-CMOS driver and interface circuit with three-state outputs. It accepts standard TTL and DTL input signals and provides output levels compatible with CMOS devices. Each driver output may be disabled to the high-impedance state to allow connection of multiple drivers to the same bus line for selective-enable operation.

SN75368: A dual ECL-to-MOS driver which will accept standard SN10,000 series ECL input signals. Its outputs have high-current and high-voltage output levels suitable for driving MOS circuits. Specifically it may be used to drive address, control, and timing inputs for several types of MOS RAMs including the TMS4062, TMS7001, and AMS1103. The SN75368 is also used as an ECL-to-TTL converter. Single in-phase and dual out-of-phase inputs are available on each driver.

SN75369: A dual current-to-MOS driver designed to accept specified input currents and provide high-current, high-voltage output levels suitable for driving MOS circuits. Specifically it is used to drive the 6003 MOS RAM clock input as well as other MOS RAM inputs. The SN75369 output is capable of swinging negative and could therefore be used with many types of MOS shift registers in addition to MOS memory circuits. Input currents of less than 0.5 mA will guarantee the output to be high, near its V_{CC} level, typically 0 to +5 volts. Input currents of 6 mA or greater will ensure the output to be low, i.e., near its V_{EE} level of −15 volts typically. Supply voltages may be varied, provided the differential $V_{CC} - V_{EE}$ does not exceed 24 volts. High-speed TTL-to-MOS negative level shifting may be accomplished with an external PNP current source or a coupling capacitor as shown in Figures 8.16 and 8.17 respectively.

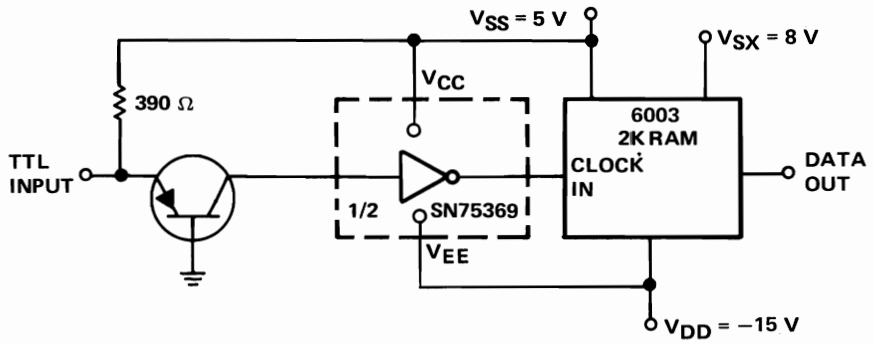


Figure 8.16. TTL-to-MOS Level Shifting with a PNP Transistor

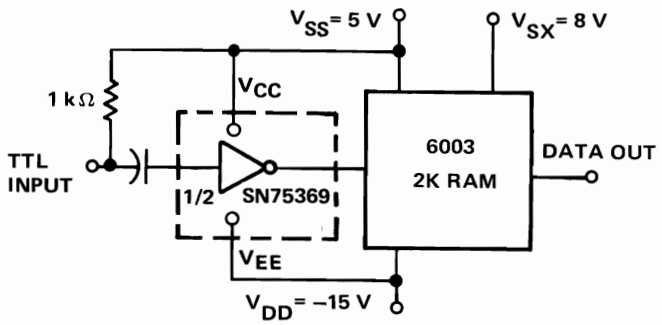


Figure 8.17. TTL-to-MOS Level Shifting with a Capacitor

SN75370: A dual-channel TTL/MOS read-write interface designed to connect directly to the input/output terminals of TMS4062 and AMS6002 MOS RAMs. Driver inputs and receiver outputs are TTL/DTL compatible. The write driver provides complementary high-voltage outputs to input/output terminals. The read amplifier responds to small differential input currents in input-output terminals. Further details of this device are presented in Section 8.4.

8.3 CONVERSION FROM MOS LOGIC LEVELS

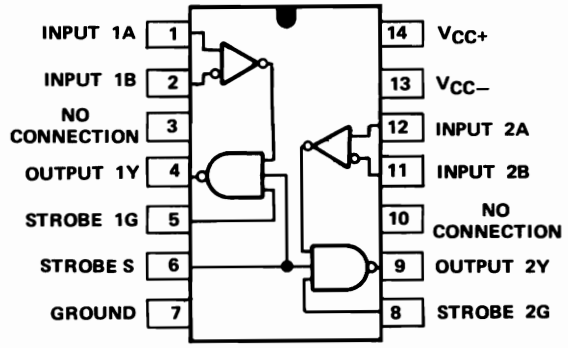
8.3.1 General Requirements

MOS output levels as well as input levels vary considerably between device types. Some outputs vary between ground and negative values from 10 to 20 volts. Other devices may have positive output levels, and in some cases very-low-level (+40 mV) signals may need to be detected. The following devices and circuits are designed to perform the various types of signal detecting and level translation required.

8.3.2 SN75107A/108A and SN75207/208 Sense Amplifiers

For sensing low-level MOS signals like those from an AMS1103 dynamic RAM the SN75107A/108A or SN75207/208 devices (Figure 8.18) are ideal. The 108A and 208 have open collector outputs while the 107A and 207 have standard TTL outputs. The input sensitivity of $\leqslant \pm 25$ mV of the 107A/108A is sufficient for many applications. For more accuracy the SN75207/208, with guaranteed input sensitivities of $\leqslant \pm 10$ mV, can be used. Identical pin-out arrangement for all of these devices simplifies substitution of device types to meet system requirements. In addition to high-speed capability these devices have several other advantages: two channels per package; individual and common strobes to provide both strobe and read-enable controls; differential inputs with high common-mode noise-handling ability; and standard TTL or open-collector outputs. Open-collector outputs allow connecting several outputs together.

Although the MOS output is single ended, a dummy line may be run with the sense line from the MOS output to the differential input of the sense amplifier (Figure 8.19). This will allow noise transients to be picked up as common-mode signals and rejected by the differential input of the sense amplifier. The combination of input sensitivity and common-mode noise rejection makes these devices excellent selections for MOS signal sensing.



DIFFERENTIAL INPUTS A-B	STROBES G	STROBES S	OUTPUT Y
$V_{ID} \geqslant 10$ mV (25 mV)	L OR H	L OR H	H
−10 mV < V_{ID} < 10 mV (−25 mV) (25 mV)	L OR H	L	H
	L	L OR H	H
	H	H	INDETERMINATE
$V_{ID} \leqslant -10$ mV (−25 mV)	L OR H	L	H
	L	L OR H	L
	H	H	L

NOTE: 10 mV LEVELS FOR 207/208
25 mV FOR 107A/108A

Figure 8.18. Functional Diagram and Truth Table: SN75107A/108A and SN75207/208

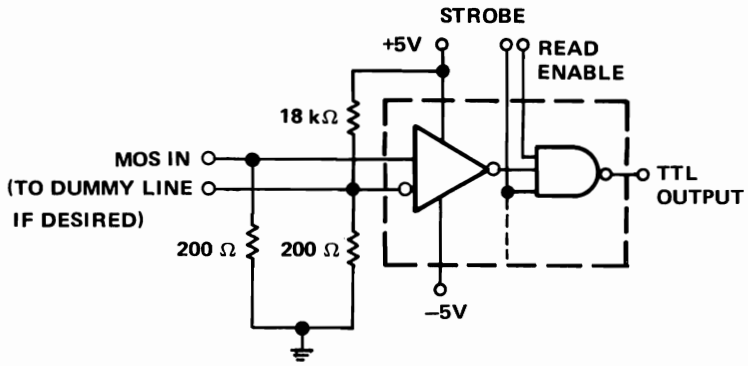


Figure 8.19. MOS-to-TTL Level-Shift Circuit Using an SN75107A or SN75207

8.3.3 SN75450B Level Shifter

The SN75450B peripheral driver may be used as a dual-channel interface between MOS and TTL. Use of one of its transistors to detect the MOS levels and drive one of its internal gates provides an easy method of interfacing. Positive or negative logic may be applied to the input, depending on input-bias arrangement.

Figure 8.20 shows the arrangement of half of an SN75450B for positive MOS input levels. MOS outputs of +3 volts or greater could be handled with this circuit.

Figure 8.21 shows an arrangement of the SN75450B for negative MOS levels that are typical of many shift registers. The 33,000-ohm series input resistor and 22,000-ohm pull-up resistor provide proper voltage levels at the transistor base. They may be adjusted to function with various negative-input levels. The series 100-pF capacitor is used to provide faster switching speed by shunting high-frequency components of the input pulse around the series resistor. The SN75450B could perform the level shifting for two channels.

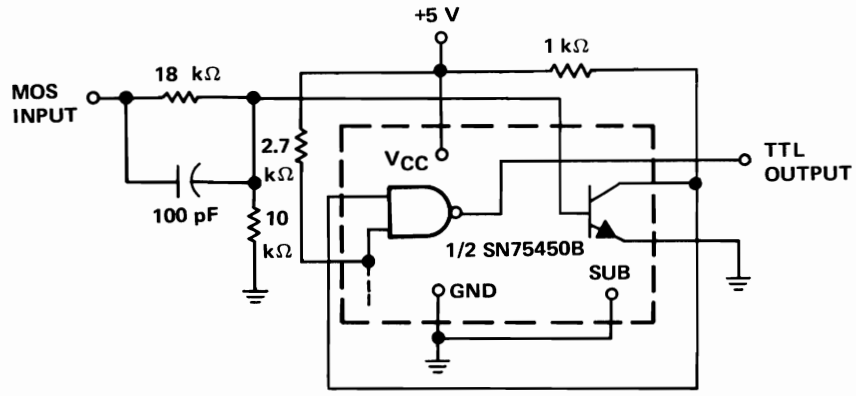


Figure 8.20. MOS-to-TTL Level-Shift Circuit for Positive MOS Levels Using an SN75450B

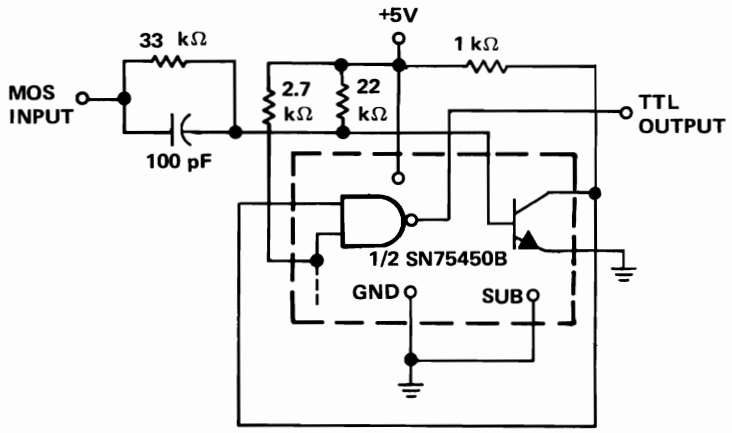


Figure 8.21. MOS-to-TTL Level-Shift Circuit for Negative MOS Levels Using an SN75450B

8.3.4 SN75270 Seven-Channel Interface

The SN75270 (Figure 8.22) is a special all-monolithic circuit with seven channels of MOS-to-TTL interface circuitry in one package. Total standby power for this seven-channel device is only 100 mW. This, combined with its high operating speed (t_{PLH} = 30 ns typical, t_{PHL} = 5 ns typical) and input sensitivity of 500 μA for a logic 1, makes the SN75270 desirable for many MOS-to-TTL applications. An input of 100 μA or less will guarantee a logic 0 output. Figure 8.23 shows the basic method of application as an MOS-to-TTL interface.

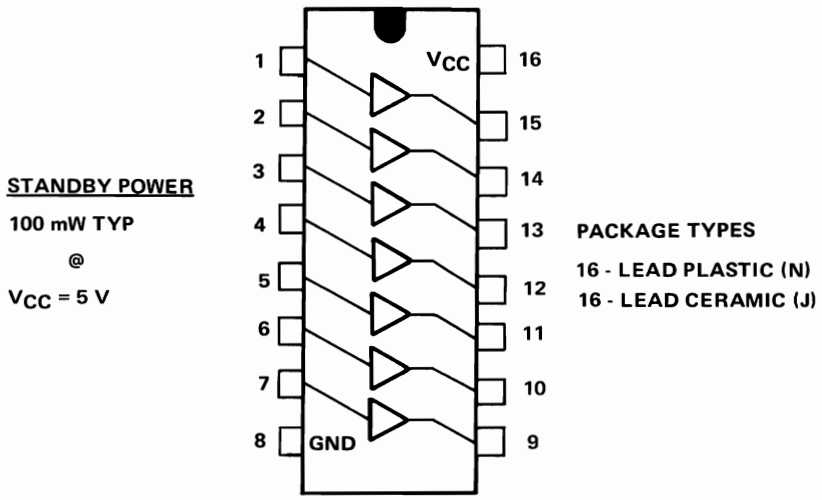


Figure 8.22. SN75270 Seven-Channel MOS-to-TTL Converter

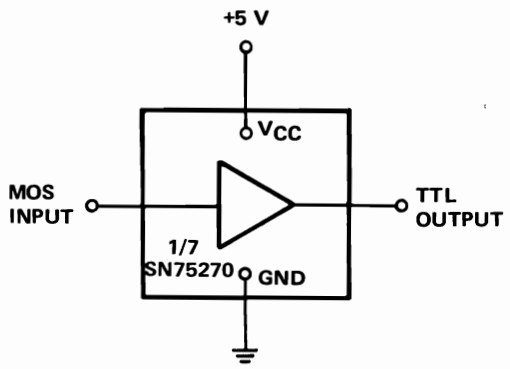


Figure 8.23. MOS-to-TTL Level Shifting with the SN75270

In Figure 8.24 the SN75270 is shown as the interface between an MOS calculator chip and a seven-segment thermal print head. Only a single +5-volt supply is required.

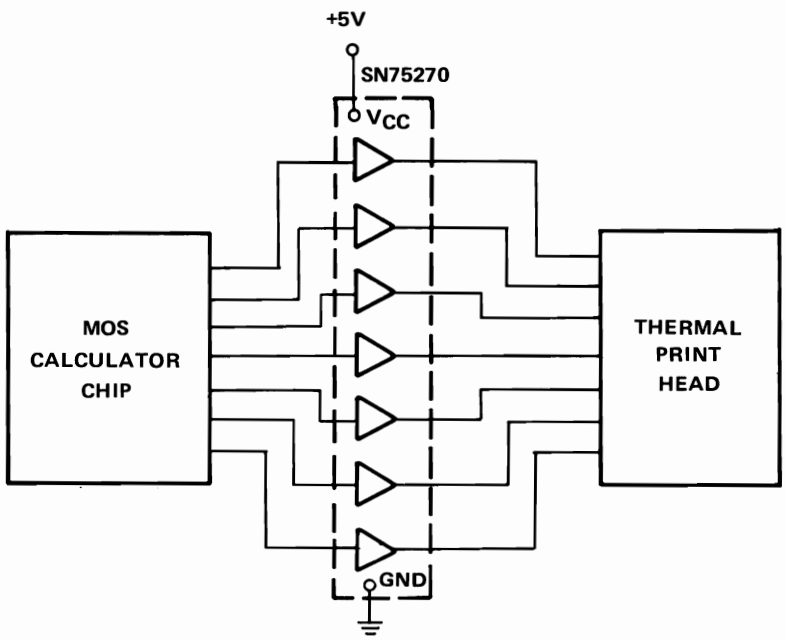


Figure 8.24. SN75270 as Seven-Channel MOS Sense Amp and Seven-Segment Thermal Print Head Driver

8.3.5 SN75260 MOS-to-ECL Interface

The SN75260 is a monolithic sense amplifier with SN10,000 series ECL-compatible logic outputs and differential MOS inputs (Figure 8.25). It is a dual-channel device with individual control strobes. Differential inputs may be connected directly to the D_O and $\overline{D_O}$ terminals of an MOS memory. Some additional features are:

Separate input-output grounds reduce interference possibilities
No external components required for interface
Only 200 μA input needed for a logic 1 level output
Less than 40 μA ensures a logic 0 level output
Uses MOS-compatible supplies
High speed with typical t_{PD} of 20 ns.

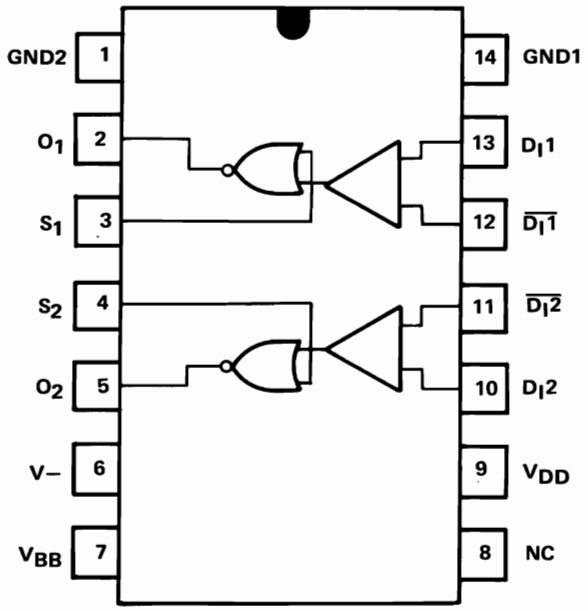


Figure 8.25. Functional Diagram and Pin Assignments: SN75260

Figure 8.26 shows a typical application example. The "Data In" and "$\overline{\text{Data In}}$" terminals connect directly to the "Data Out" and "$\overline{\text{Data Out}}$" terminals of the TMS7001. The output of the SN75260 sense amplifier will remain at a logic 0 level unless it receives a $\overline{D_O}$ output current of 20 μA at the time it is strobed, as shown in the typical waveforms of Figure 8.26.

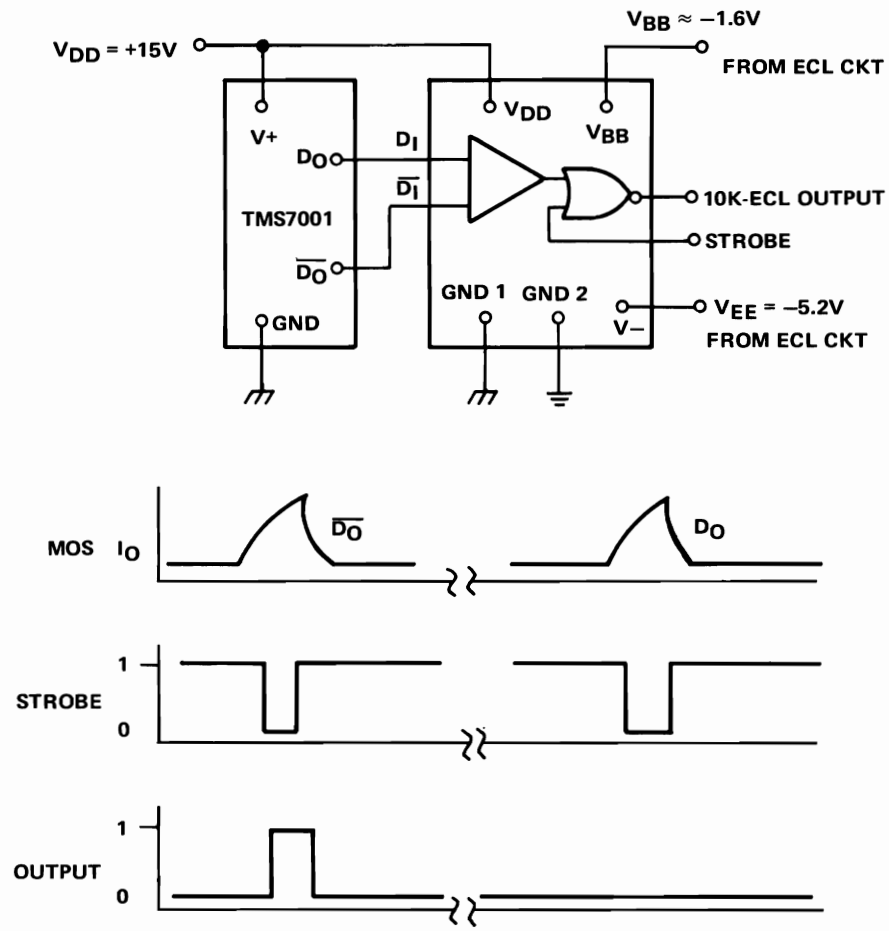


Figure 8.26. SN75260 Sense Amplifier for TMS7001

8.3.6 SN75261 MOS-to-TTL/DTL Interface

The SN75261, much like the SN75260, is a monolithic sense amplifier (Figure 8.27) with TTL/DTL-compatible logic outputs and differential MOS inputs. A typical application would be interfacing between a TMS7001 MOS RAM unit and TTL logic circuitry. General specifications and performance are the same as for the SN75260. In addition, its 20-mA output sink capability allows it to operate into a TTL bus with several loads.

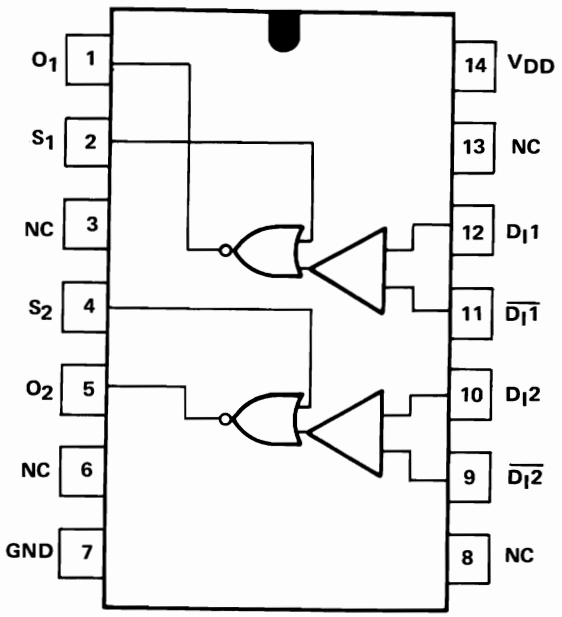


Figure 8.27. SN75261 MOS-to-TTL or DTL Sense Amplifier

8.4 COMBINATION MOS DRIVER AND SENSE AMPLIFIER

Circuits shown in Figures 8.28 and 8.29 are combination write (or drive) and read (or sense) circuits. Their compactness, speed of operation, and control features make them particularly suited for more complex systems incorporating MOS circuits like the TMS4062 1024-word by 1-bit dynamic RAM. Figure 8.28 shows a circuit using a combination of discrete and integrated-circuit devices, while Figure 8.29 provides a completely monolithic approach. The SN75370 is an entirely self-contained, dual-channel, sense-digit driver which significantly reduces component count. As a comparison it would require two SN75451B packages, one SN72711 package, four 2N4401 transistors, and 16 resistors to duplicate the function of one SN75370. Performance comparisons of these two circuits are shown in Table 8.3.

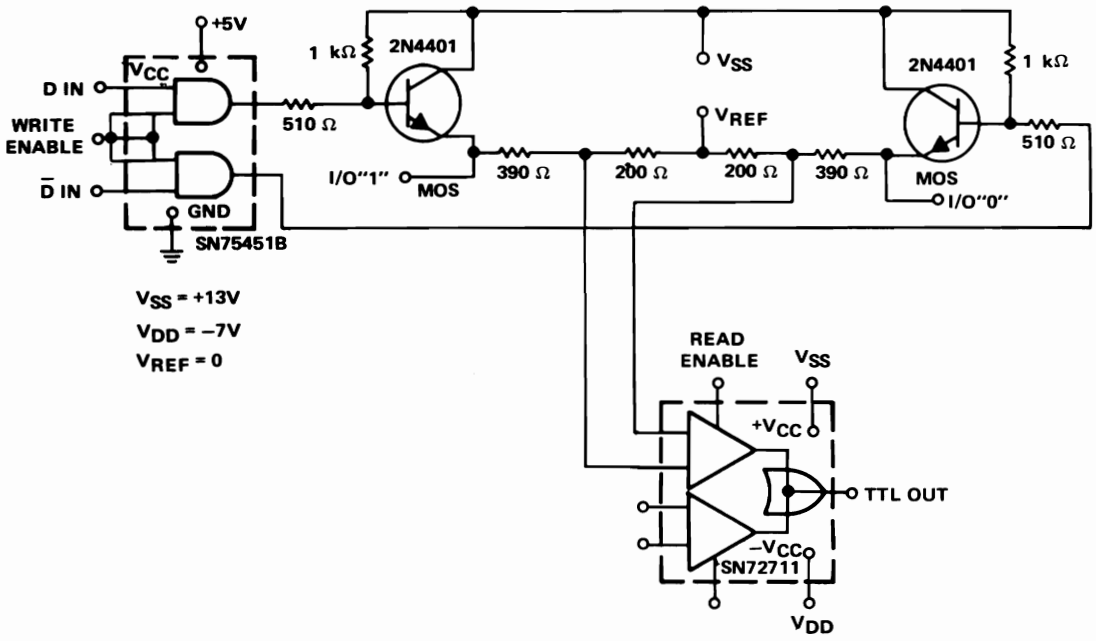


Figure 8.28. MOS-to-TTL Interface Using an SN75451B

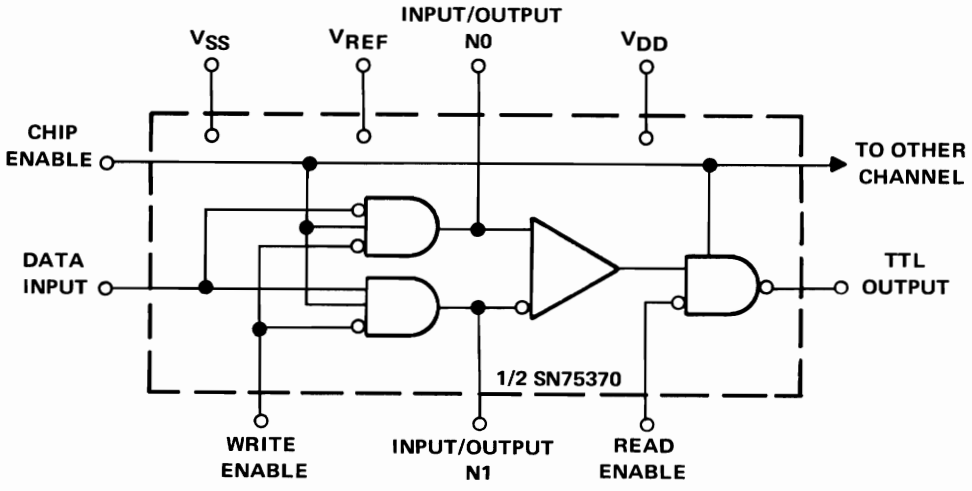


Figure 8.29. MOS-to-TTL Interface Using an SN75370

Table 8.3. Comparative Performance Data for Circuits Shown in Figures 8.28 and 8.29

	SN75370					Discrete				
	Write t_{PD} to I/O Line		Read t_{PD} to Output			Write t_{PD} to I/O Line		Read t_{PD} to Output		
MOS "C" Load (pF)	L-H (ns)	H-L (ns)	L-H (ns)	H-L (ns)	Max. Freq. (MHz)	L-H (ns)	H-L (ns)	L-H (ns)	H-L (ns)	Max. Freq. (MHz)
50	19.2	20.2	20.4	32.1	6.6	48.3	59.6	21	33	3.3
100	21.0	24.7			6.6	55	95			3.3
700	48.1	48.6			3.3	85	129			1.6
2000	113	105			1.3	168	320			0.67

8.4.1 SN75370 Sense-Digit Driver

The SN75370 was designed primarily as the sense-digit driver for the TMS4062 MOS RAM. Each of its two channels consists of a write driver and a read amplifier which are common at the input-output (I/O) terminals. These terminals are outputs for the write driver and inputs for the read amplifier. In a write mode the write-driver circuit is designed to write MOS-level binary information into the MOS RAM under control of TTL inputs. In the read mode the read amplifier is designed to read MOS-level binary information from the MOS RAM and convert it to TTL levels at data outputs. This function is also controlled by TTL inputs.

Data output is so constructed that it may be wire-AND connected to an external pull-up resistor if desired (see Figure 8.30 for package pin-out). The device has a chip enable (pin 9) common to both channels which can be used to disable the whole chip. Internal voltage regulators permit circuit operation over a wide range of supply voltages. Operational speeds are compatible with the 250-ns cycle times of the TMS4062.

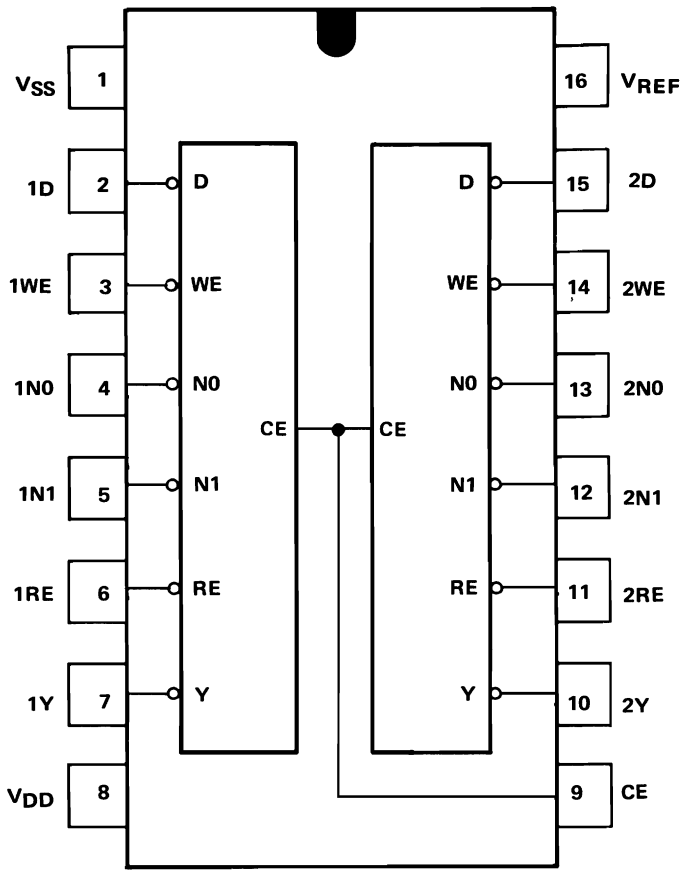


Figure 8.30. SN75370 MOS Sense Digit Driver

8.4.2 Typical SN75370 Application Examples

A typical configuration using one-half of an SN75370 to interface a TMS4062 RAM is shown in Figure 8.31. With V_{SS} =20 V and V_{REF} = 7 V the following typical characteristics can be expected:

Bit driver propagation delay ≈ 40 ns
Sense amplifier/converter propagation delay ≈ 25 ns
Power dissipation ≈ 600 mW (both channels in read mode)
Power dissipation ≈ 900 mW (both channels in write mode)
Standby power dissipation ≈ 400 mW (chip disabled)

When used with the TMS4062, the SN75370 will respond in ≈ 10 ns instead of the typical 25 ns listed above because the output current from the TMS4062 approximates the characteristics of a ramp function rather than a step function.

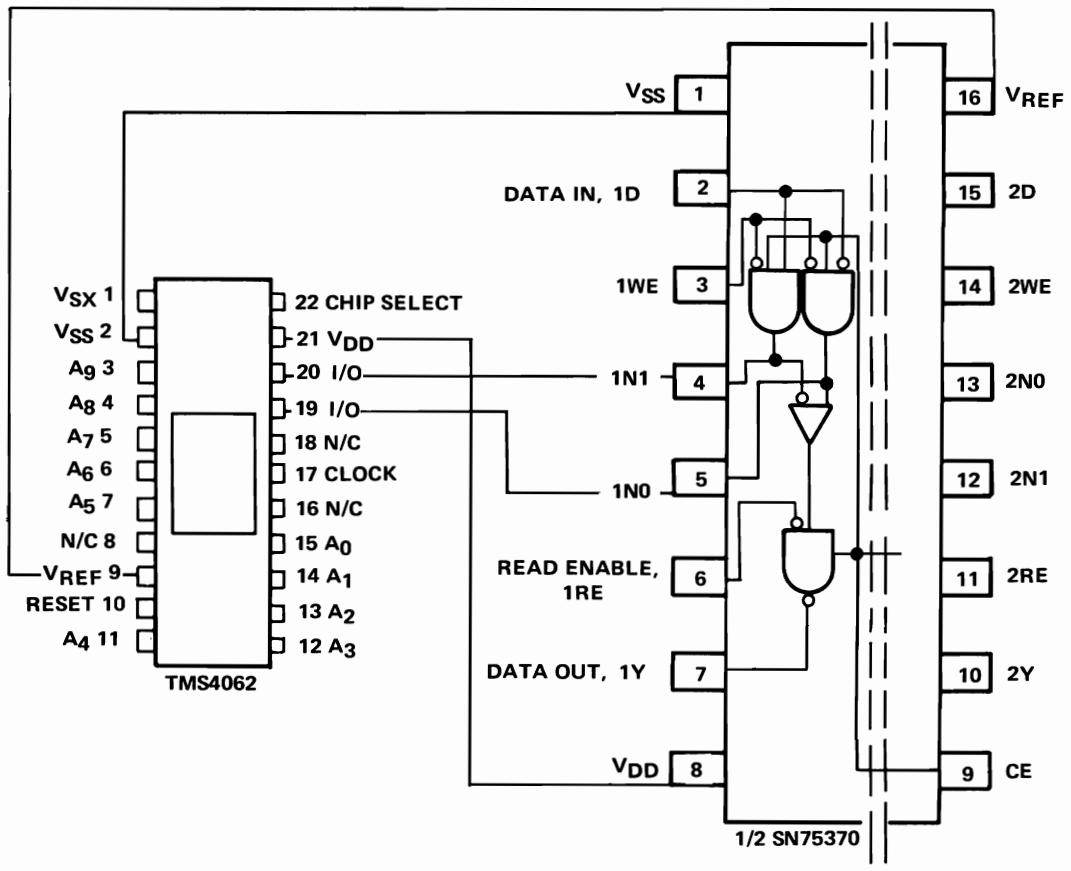


Figure 8.31. SN75370 as Interface to a TMS4062 RAM

Figure 8.32 is a block diagram of a 17 x 8 K memory organization employing the TMS4062. Dual-channel SN75361As are used to drive the clock, reset, and address inputs. Read/write inputs are driven and sensed by SN75370 dual-bit driver/sense amplifier/converters. Eight and one-half SN75370 packages and thirteen SN75361A packages are all that are required to interface to the 136 TMS4062 devices for this large memory.

The outputs of SN75370 devices may be used as independent outputs (Figure 8.33a), or connected to a single load resistor for wire-AND operation (Figure 8.33b).

Device power generated and the ability of the package to dissipate this power must be considered when using the SN75370. Power generated by the device depends on the mode of operation and the supply voltages used. Under some conditions the SN75370 may generate sufficient instantaneous power to exceed the recommended continuous (average) power-dissipation capability of the package.

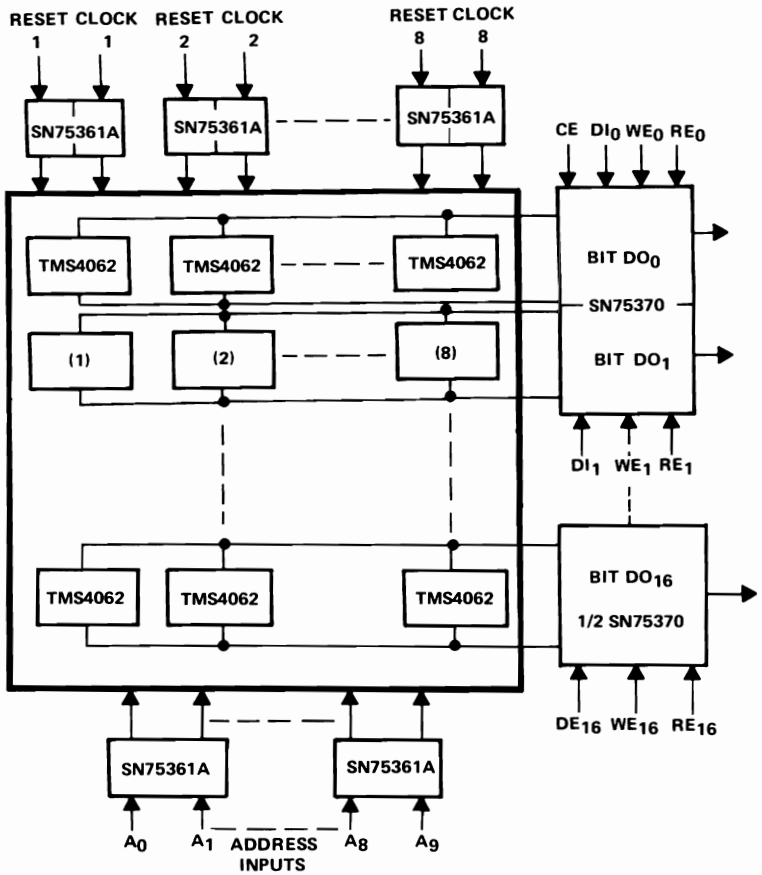


Figure 8.32. Block Diagram of an 8K x 17 Bit MOS Memory

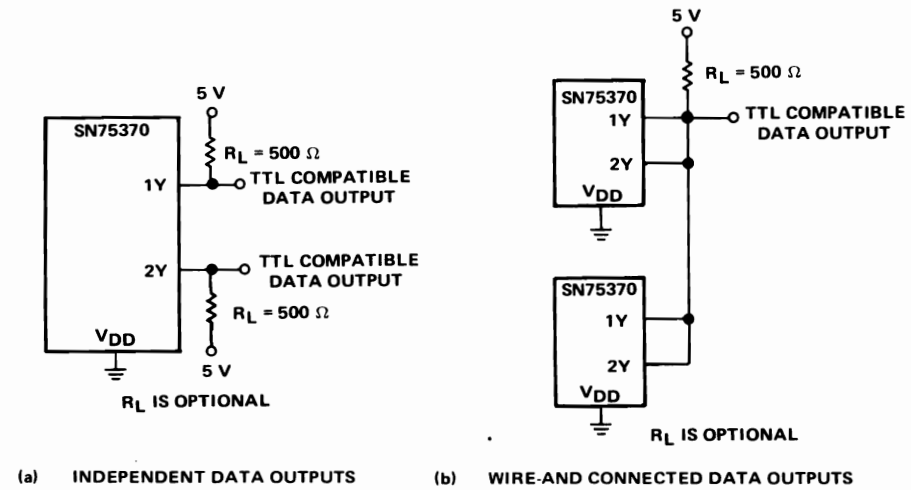


Figure 8.33. Methods of Using Data Outputs of the SN75370

Appropriate duty-cycling of high-power conditions must be used to keep average power generated by the SN75370 within the power-dissipation capability of the package.

Figure 8.34 shows typical methods to lower average power dissipation by pulsing CE, WE, and RE inputs. Highest power occurs when both channels are in write mode. Usually, write mode must be duty-cycled to reduce average power. Figure 8.34(d) and 8.35 demonstrate the use of a discrete PNP transistor to switch power to the V_{SS} terminal of the SN75370 to minimize average power. In addition, forced-air-cooling or heat-sinking techniques may be used to increase the power-dissipation capability of the SN75370 package.

The following example illustrates a method of calculating average dc supply power for the SN75370. Using Figure 8.34, the typical average power over period T can be calculated. Assume that both channels are operating identically, except in read mode, when one channel is reading a logic 1 and the other channel is reading a logic 0. Let V_{SS} = 20 V, V_{REF} = 7 V and T_A = 25°C.

$$P_{TYP} = (\%t_W)\,(P_W) + (\%t_R)\,(P_R) + (\%t_{SB})\,(P_{SB}) + (\%t_{CD})\,(P_{CD})$$

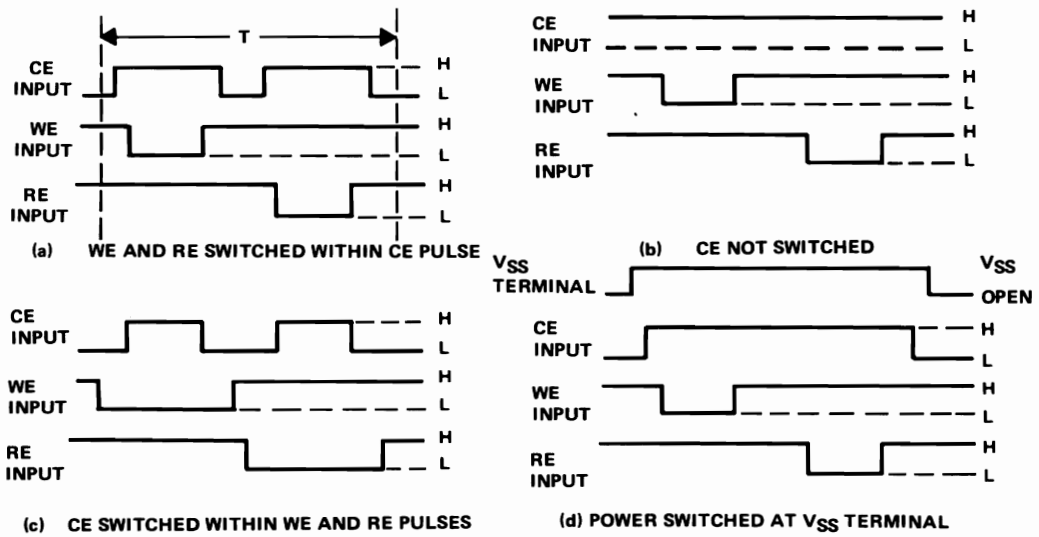


Figure 8.34. Typical Operating Input Waveforms for the SN75370

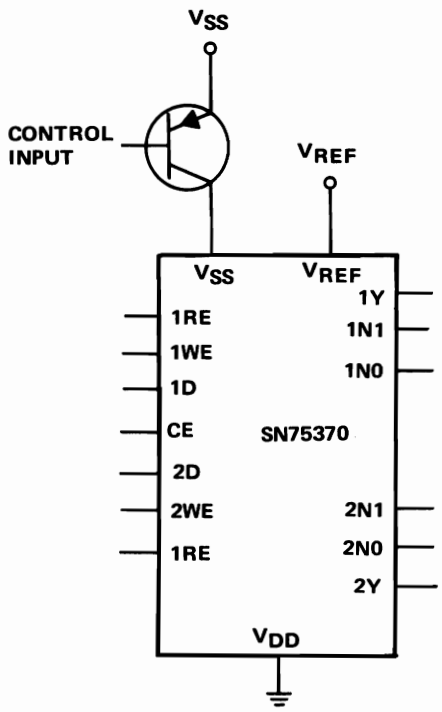


Figure 8.35. Controlling Power to V_{SS} Terminal of SN75370 Using a PNP Transistor

From the data sheet and Figure 8.34 the appropriate values are substituted to yield:

$$P_{TYP} = (0.25)\,(910) + (0.25)\left(\frac{560 + 640}{2}\right) + (0.2)\,(560) + (0.3)\,(410)$$

$$P_{TYP} = 613 \text{ mW}$$

Power dissipation is reduced by more than 80% when the V_{SS} supply is interrupted during the standby mode, greatly reducing the system power requirements, particularly in large systems.

8.5 JUNGLE CIRCUIT

8.5.1 SN72595 Description

The SN72595 (Figure 8.36) is a monolithic micro-processor drive system. It is a complex multifunction circuit sometimes referred to as a jungle circuit. Designed to

greatly reduce the package count and assembly cost of MOS memory systems and calculators, the SN72595 micro-processor drive system includes the following functions:

Clock Generator: a single-phase, self-starting generator with dual-frequency operation.

Clock Driver: a typical power-type driver capable of driving the capacitive MOS clock inputs.

V_{gg} Generator: a static V_{gg} supply and a pulsed V_{gg} supply are generated for the MOS circuitry.

Operating from a single V_{SS} supply of 7.2 volts (nominal), the SN72595 has a power dissipation of only 125 mW in the low-frequency mode and 250 mW in the high-frequency mode. Clock frequencies are 150 to 300 kHz for f_H and 20 to 40 kHz for f_L. Three inputs — K_1, K_2, and K_3 — may be used to key the oscillator to its f_H state.

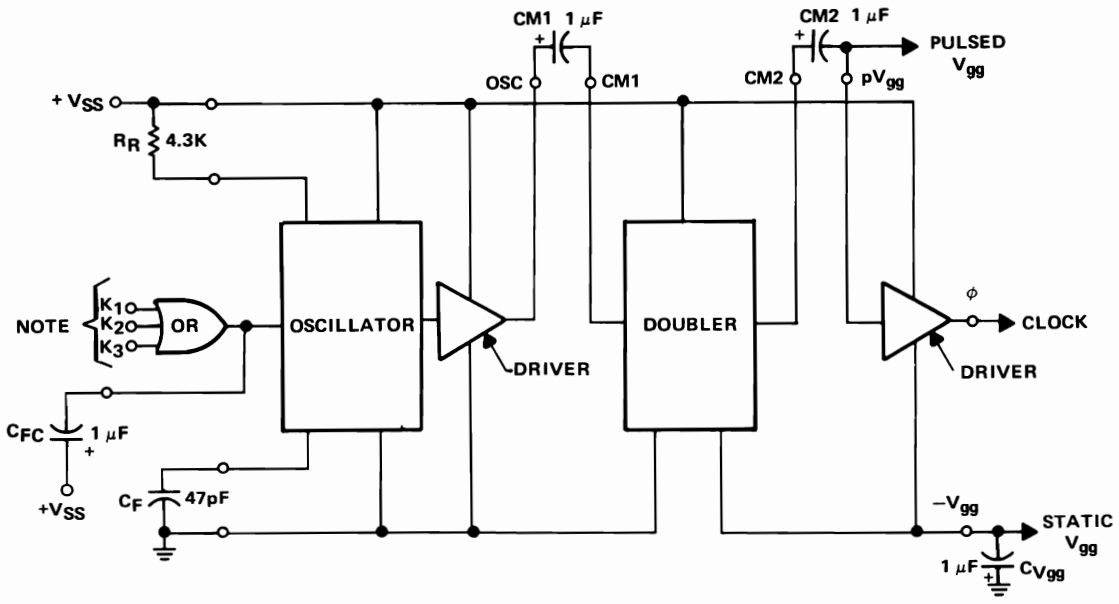


Figure 8.36. SN72595 Block Diagram

8.5.2 Typical SN72595 Application Examples

Figure 8.37 shows two basic applications for the SN72595. Figure 8.37a is a clock generator, clock driver, and V_{gg} supply for the TMS0117 decimal arithmetic processor, a popular application in digital systems. Note that the key inputs are tied to V_{SS}, fixing the clock generator in its high-frequency mode. A minimum number of external components is required. In Figure 8.37b the SN72595 is used with a typical one-chip calculator unit. Note in this application that the keyboard is used to control the frequency of the clock generator. A very versatile device — providing many of the functions required in digital processing and calculator circuits — the SN72595 also features fast rise and fall times on its clock pulses for accurate control of the driven circuitry. Clock pulse rise and fall times are typically 100 nanoseconds.

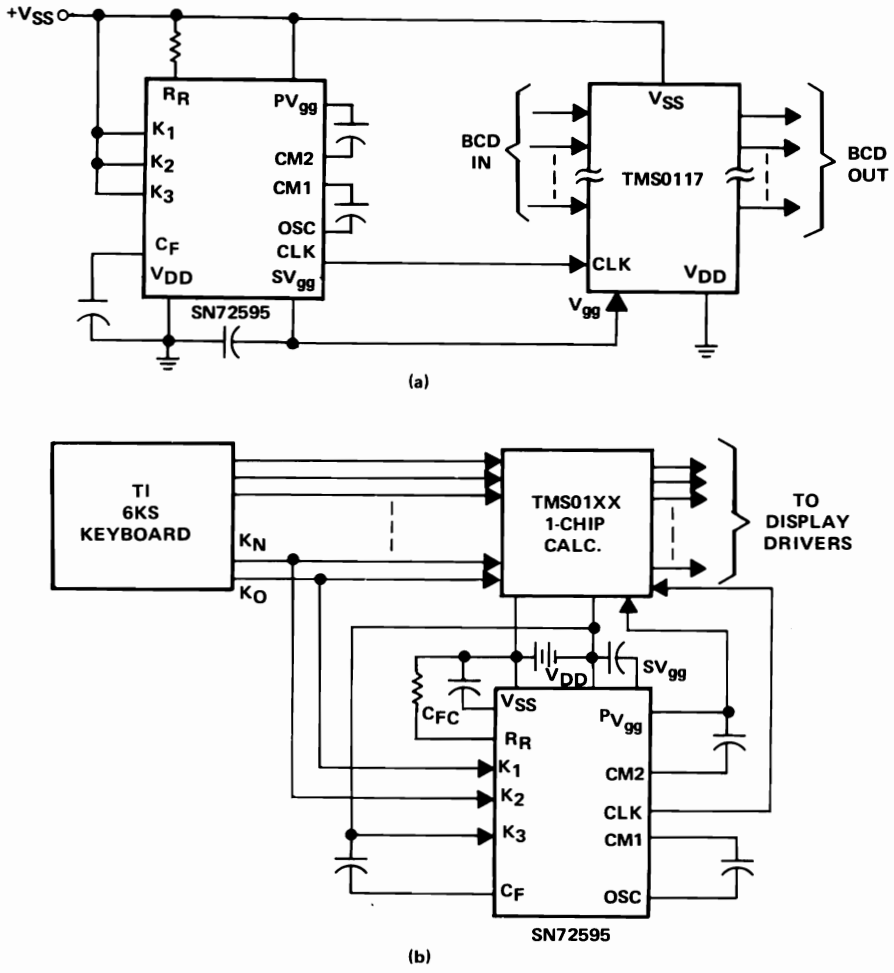


Figure 8.37. Typical SN72595 Applications

8.6 MOS-TO-VLED DRIVERS

Another popular type of MOS interface is that between the MOS device and a visible-light-emitting display. Visible-Light-Emitting Diode (VLED) displays are frequently employed because of their low power requirements and compact size.

8.6.1 SN75491 and SN75492

The SN75491 and SN75492 are designed for use with MOS integrated circuits and common-cathode VLEDs in serially addressed multidigit displays. This time-multiplexed system, using a segment-address and digit-scan method of VLED drive, minimizes the number of drivers required. Figures 8.38 and 8.39 show the package pin-out and functional diagram of the SN75491 and SN75492 respectively.

The SN75491 is a quad 50-mA source-or-sink device generally used as the segment driver. All inputs are compatible with low-current MOS output, and each circuit functions as a high-gain Darlington driver. The SN75492 is a hex 250-mA sink device which is generally used as the digit driver.

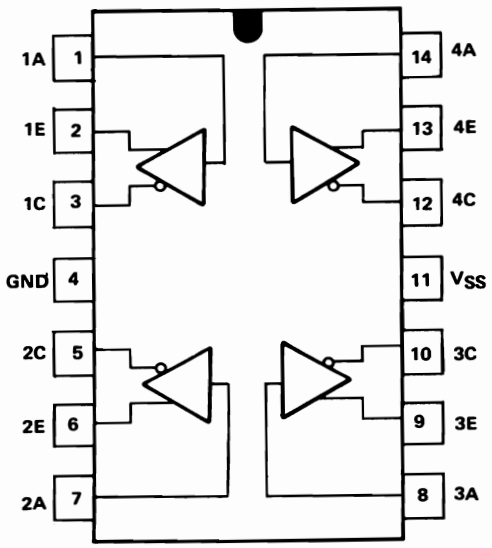


Figure 8.38. SN75491

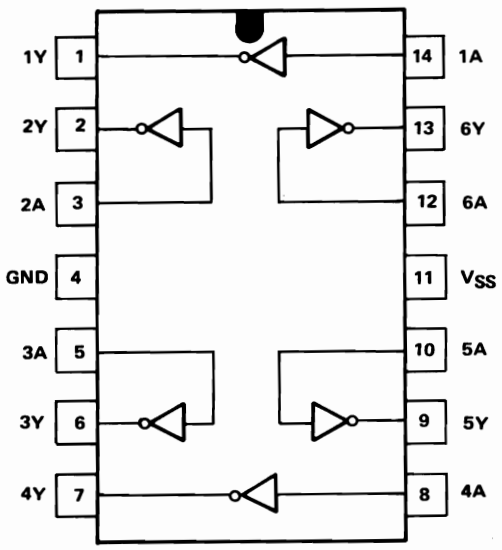


Figure 8.39. SN75492

8.6.2 SN75491 and SN75492 Applications

Figure 8.40 is an example of time-multiplexing the individual digits in a visible display to minimize the display circuitry required. As many as 12 digits, each using a seven-segment display plus a decimal point, may be driven using only two SN75491 and two SN75492 driver packages.

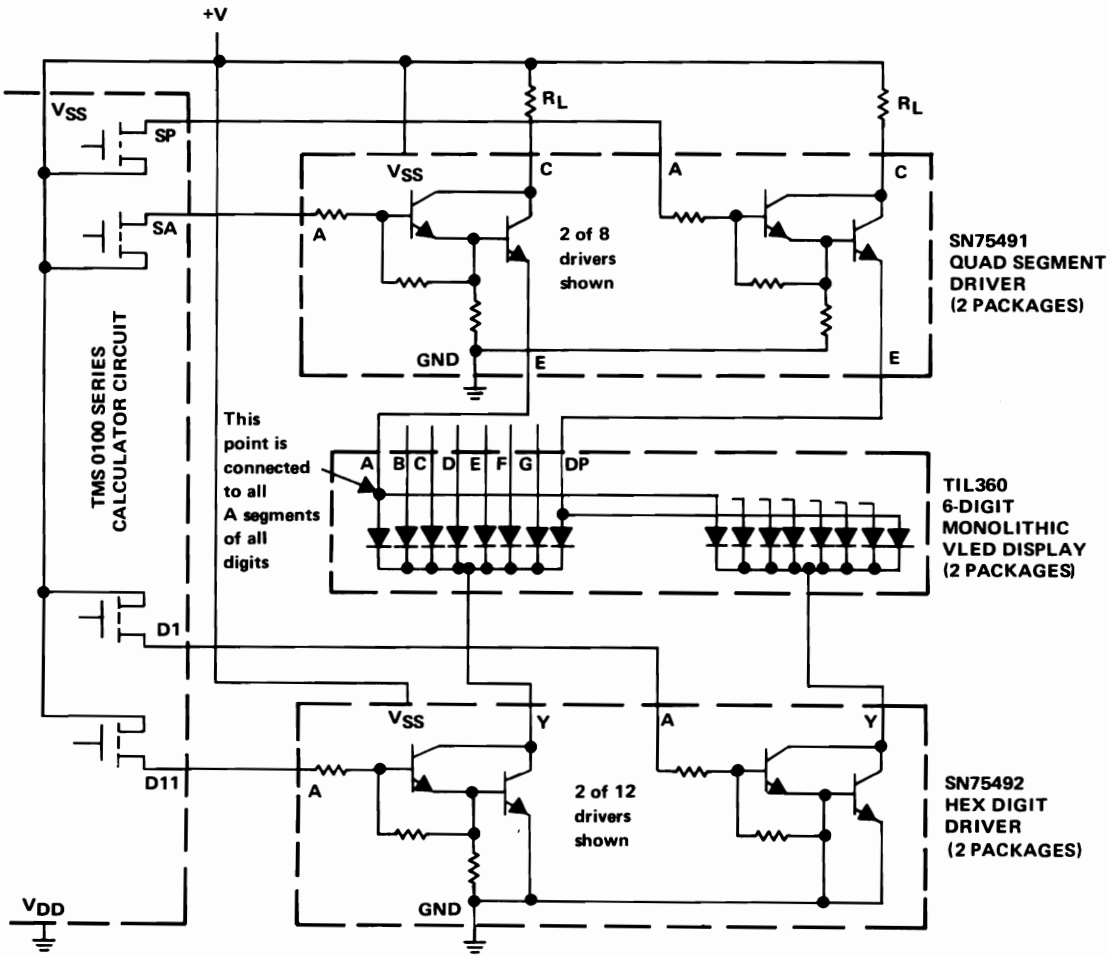


Figure 8.40. Interfacing Between MOS Calculator Circuit and Multi-Digit VLED Display

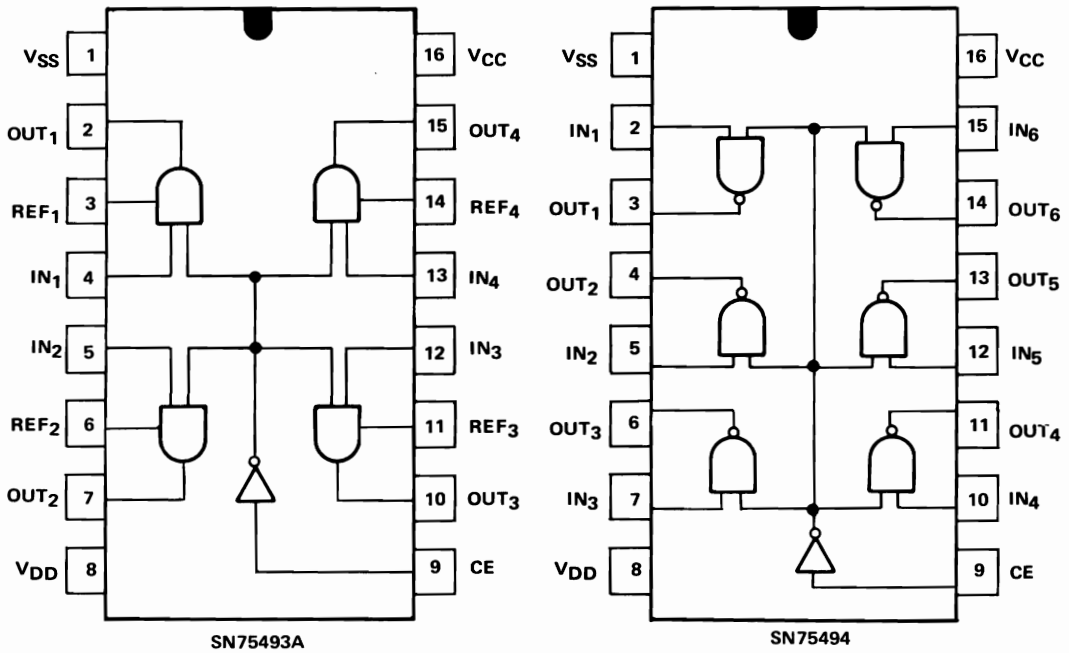


Figure 8.41. Functional Diagrams and Pin Assignments: SN75493A and SN75494

8.6.3 SN75493A and SN75494

The SN75493A and SN75494 (Figure 8.41) are similar to the SN75491 and SN75492, but have several advantages. Both the SN75493A and SN75494 can be operated from lower voltages, thereby reducing power consumption. The SN75493A is designed to deliver relatively constant current through an external resistor, independent of supply-voltage variations. Both the SN75493A and SN75494 have blanking inputs which permit low-standby-power operation.

8.7 ADDITIONAL APPLICATIONS FOR MOS INTERFACE CIRCUITS

8.7.1 SN75361A Series Applications

The SN75361A series devices may be used in many different types of applications as well as for memory drivers. Following are a few examples.

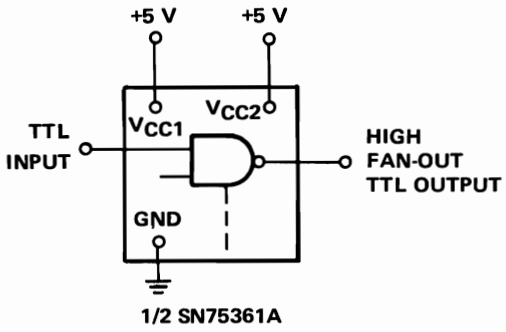
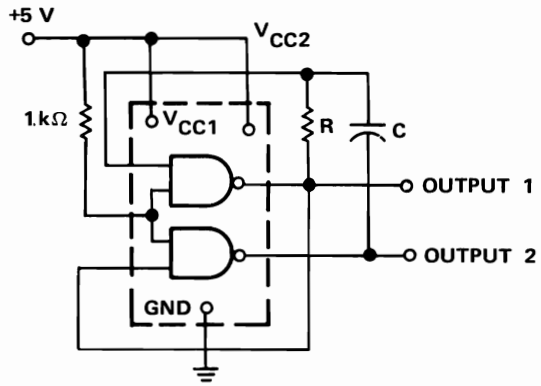


Figure 8.42. TTL Bus Driver

TTL Bus Driver – The SN75361A, 362, 363, 365, and 367 may be used as high fan-out or TTL bus drivers by connecting the V_{CC2} and V_{CC1} terminals to +5 volts as shown in Figure 8.42.

Oscillator – In this example, Figure 8.43, the SN75361A is used as an oscillator. Initial turn-on, due to the capacitor looking like a short circuit, will force Output 1 high and Output 2 low. The input to Channel 1 will rise as C is charged by Output 1 through R. When the TTL threshold is reached, positive feedback through Channel 2 will force the condition to reverse. The resulting frequency is approximately f = 0.4/RC.



TEST EXAMPLES

1. WHERE R = 1.0 kΩ AND C = 0.01 μF, FREQUENCY = 40 kHz
2. WHERE R = 1.0 kΩ AND C = 0.02 μF, FREQUENCY = 20.2 kHz

Figure 8.43. SN75361A Oscillator

Balanced-Line Transmission – The high-speed and output-drive capabilities of the SN75361A (Figure 8.44) allow it to drive relatively long, low-impedance transmission lines at very high frequencies. To take advantage of the common-mode rejection characteristics of the line receiver both drivers in the package are used to drive a balanced line. Input SN7404 and SN7408 buffer gates are used to drive the two SN75361A sections out of phase, providing a balanced drive to the line.

Output impedance of the SN75361A is low and, because of the need for proper line termination at high frequencies, series resistors are used. Referred to as reverse termination, these resistors minimize reflections and allow maximum-frequency operation.

In this application the line impedance Z_L is 100 ohms. Reverse-terminating resistors will be $Z_L/2$ or 50 ohms each, while termination across the line at the receiver is equal to Z_L (100 ohms). With a good layout, adequate supply bypassing, and a good uniform transmission line it is possible to operate with data rates up to 20 MHz over lines as long as 100 feet with this circuit.

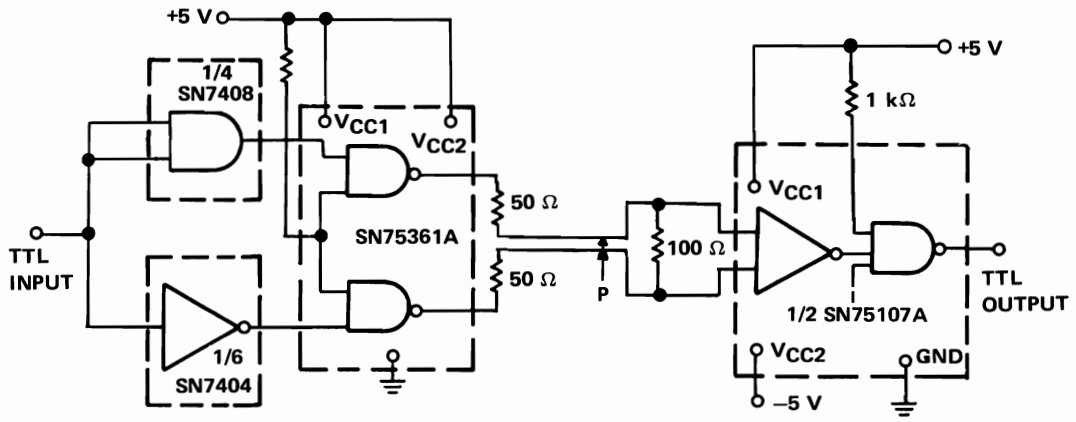
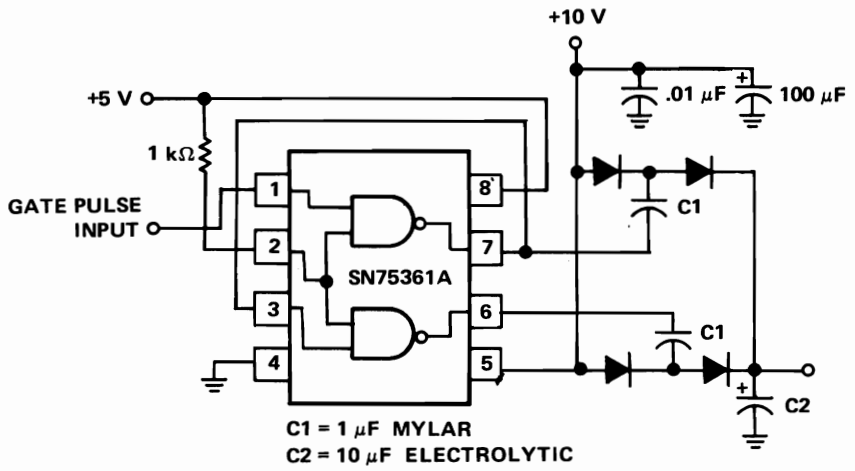


Figure 8.44. Balanced-Line Transmission Circuit

DC-to-DC Converter – In many applications it is desirable to limit the number of battery or other dc supply sources used. Therefore, it will sometimes be expedient to generate an additional supply level within the system, using a dc-to-dc converter (Figure 8.45). The SN75361A may be connected as a voltage doubler, and a gating pulse may be used to provide the switching. The result is a relatively clean supply voltage 60 to 80% greater than the source voltage for currents up to 20 mA.



OUTPUT CONDITION	OUTPUT VOLTAGE	OUTPUT RIPPLE %
NO LOAD	18.65	0.08
20 mA	16.24	0.123
50 mA	14.83	0.334
100 mA	13.33	0.936
200 mA	10.82	1.283

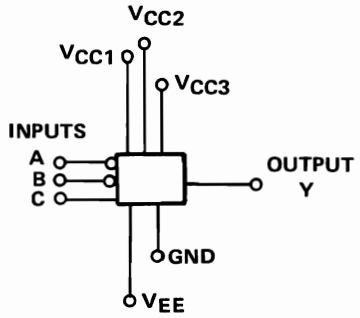
Figure 8.45. Low-Ripple Inverting DC-to-DC Converter

8.7.2 SN75368 Applications

In addition to use as an ECL-to-MOS driver and an ECL-to-TTL driver, the unique characteristics of the SN75368 permit it to be used as a NOR gate, a non-inverting gate, or a differential ECL line receiver. Truth tables for these functions are shown in Figure 8.46.

8.7.3 SN75270 as an Optical-to-TTL Interface

The sensitivity of the SN75270 recommends it for many other types of interfacing applications. A good example can be seen in the optical-to-TTL interface shown in Figure 8.47. Sensitivity to very low light levels is accomplished with the use of an LS400 phototransistor coupled to the sensitive input of the SN75270. Timing events, position indicators, card reading, and many other applications can easily be handled with this basic optical-to-TTL interface.



TRUTH TABLES

A	B	C	Y	FUNCTION
L	L	V_{BB}	H	
L	H	V_{BB}	L	NOR
H	L	V_{BB}	L	GATE
H	H	V_{BB}	L	
V_{BB}	V_{BB}	L	L	
V_{BB}	V_{BB}	H	H	
L	V_{BB}	L	L	NON-
L	V_{BB}	H	H	INVERTING
V_{BB}	L	L	L	GATE
V_{BB}	L	H	H	
H	H	L	L	
L	L	H	H	DIFF
L	H	L	L	LINE
L	L	H	H	RECEIVER
H	L	L	L	
L	L	H	H	

V_{BB} = Reference Supply Voltage for SN10000 Series ECL

Figure 8.46. SN75368 Functions

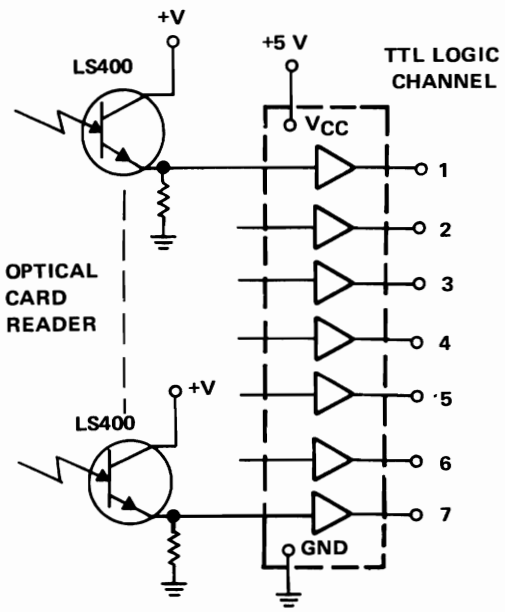


Figure 8.47. Optical-to-TTL Interface Using the SN75270

8.7.4 SN75491 Series Applications

With each VLED driver package containing several high-gain Darlington transistor combinations, these packages may be employed for numerous other applications. The following are typical examples:

Quad or Hex MOS-to-Relay Driver – Any one of the VLED drivers could be used to drive a relay. Utilized in a common-emitter configuration as a sink driver their collector supply terminals would be tied to the base of the relay. In this application (Figure 8.48) the combination of low MOS output currents and high-gain Darlington circuits provides adequate drive for many relay or hammer driver applications.

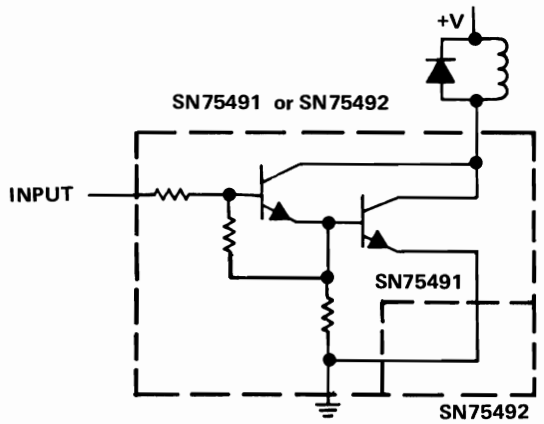


Figure 8.48. Quad or Hex Relay Driver

10-MHz RF Amplifier and Coax Driver – One basic problem with most wideband RF-type amplifiers is their inability to operate into low-impedance loads. In this application (Figure 8.49) the SN75491 is used to interface between a balanced high-impedance RF circuit and a single-ended, low-impedance load such as a coax cable.

First, one section is biased as current source for the amplifier-input sections. The 5000-ohm control is used to set the operating current at an optimum level for good gain and linearity. Two other sections are connected as differential input amplifiers. These will exhibit an input impedance matching well with the output from a typical video amplifier such as the SN7510. The output of the differential input pair drives the fourth section of the SN75491, which is connected as an emitter follower.

Some voltage gain, up to 26 dB, is achieved in this configuration, and the power-driving capability of the output section allows driving low-impedance loads. For example, a 50-ohm coax could easily be driven.

Very few external components are required. The result is a low-cost RF amplifier with capability of driving low-impedance transmission lines linearly.

Voltage Regulator – In this application (Figure 8.50) the basic amplifier configuration is again used. Section 1 of the SN75491 is connected as a current source for the comparator, consisting of Sections 2 and 3. A reference voltage is generated by the resistor divider network and zener diode, and fed to one input of the comparator (Section 2). The output voltage is sensed by Section 3. Any error voltage generated is fed to the input of Section 4, which acts as a series pass regulator controlling the output voltage. With the V_O adjust control set to yield 5 volts output this circuit maintains the output within ± 1% over a load range of 0 to 50 mA. At +15 volts output, regulation is still better than ± 2%. Most SN75491s will meet the voltage requirements of this application although they are outside the guaranteed limits.

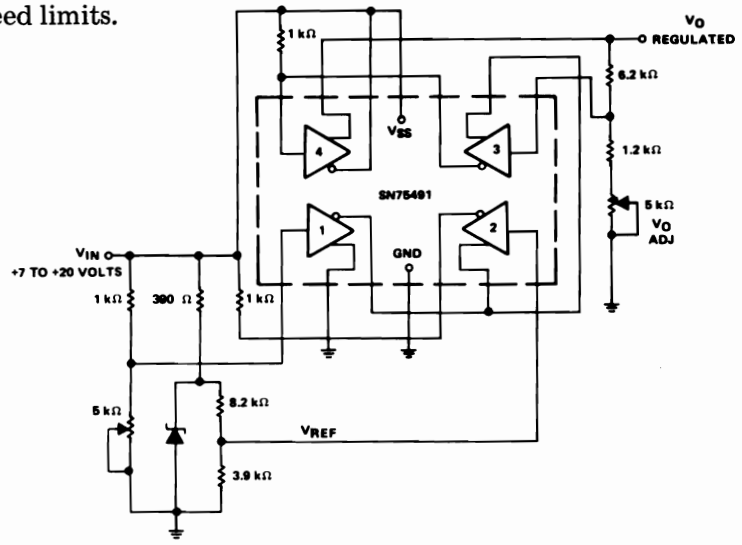


Figure 8.49. SN75491 as an Interface Between the Balanced 10 MHz Output of an RF Amplifier and a Coaxial Cable

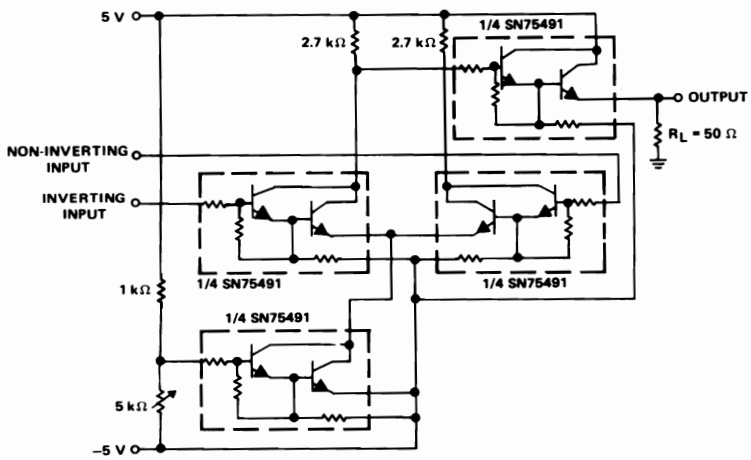


Figure 8.50. SN75491 as a Voltage Regulator

9

Core Memory Circuits

9.1 CHARACTERISTICS OF CORE MEMORIES

The need for high-speed, electronically alterable memories has resulted in the development of small ferrite toroids, or cores. These cores have made possible the construction of high-speed, low-cost memory systems ranging from the small 1000-bit scratchpad size to large bulk memories with 5-billion-bit storage capacity.

To readily understand the device parameters of core interface circuits we must first become familiar with the characteristics of the cores and with definitions of the current-pulse logic terms used. The following definitions and terms are employed in the discussions of core memory drivers and sense amplifiers:

- I_w Write current: A current pulse in the positive or negative sense, sufficient to fully switch a core.
- I_{pw} Partial write current: A current pulse of insufficient magnitude to cause flux switching; nominally $I_w/2$ in magnitude.
- I_r Read current: A pulse in the negative sense sufficient to fully switch a core from the 1 to the 0 state.
- I_{pr} Partial read current: A pulse in the negative sense, but of insufficient magnitude to cause flux switching; nominally $I_r/2$ in magnitude.
- I_i Inhibit current: A current pulse opposing the I_w current, sufficient to prevent flux switching; normally $I_w/2$ in magnitude.
- I_x X current: The current in an X-selected line — normally I_{pr} or I_{pw}.
- I_y Y current: The current in a Y-selected line — normally I_{pr} or I_{pw}.
- I_z Z current (bit current): The current pulse in the Z axis of a core plane. This line is also called the bit wire or inhibit wire. This pulse is normally I_i.

Since a core can store only a single bit of information, a typical memory system

utilizes a large number of cores, each core storing a single bit or binary digit — that is, part of a word. A typical memory then requires W x L cores, with W the number of words and L the number of bits per word. Most memories use a coincident current matrix (CCM) system for core selection.

Figure 9.1 depicts two core wiring configurations. In these examples an X current and a Y current flowing through the core in the same direction are sufficient to make up a full I_W level and address that particular core.

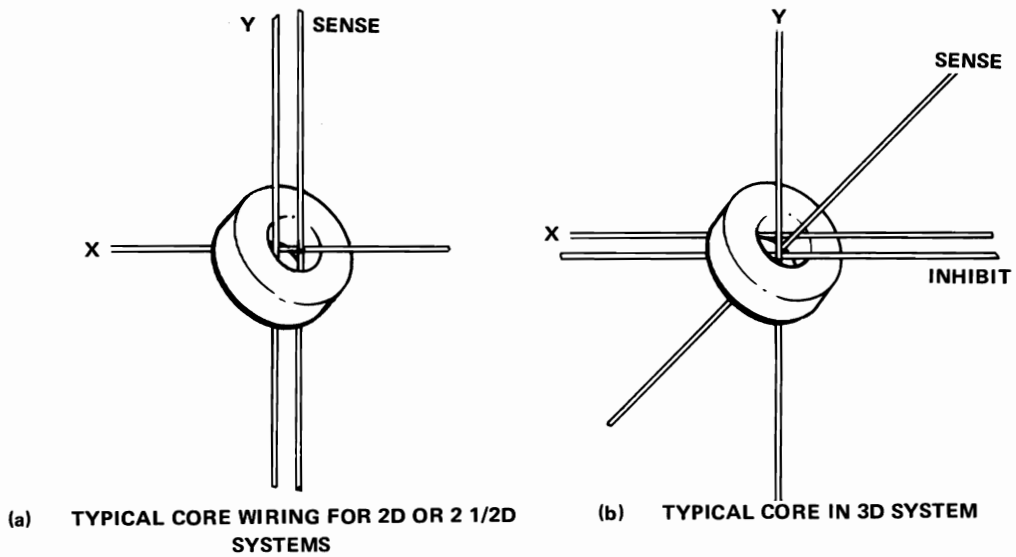


Figure 9.1. Core Wiring Configurations

The two stable states in the magnetization characteristics of the core are used for storage of the binary information (see Figure 9.2). Because of the very steep slopes in the B-H curve, a small incremental change in the magnetic flux intensity, H, causes a large change in the flux density, B. When a sufficient select current flows through the wire threading the core, the core is magnetized in a direction determined by the direction of this current.

Readout of the stored information, which is destructive, is performed by forcing the core to the 0 state; if the core is in the 1 state, flux reversal results. This flux change can be read out as a voltage pulse at the terminals of the sense line linking the core. If the core is already in the 0 state, flux reversal does not occur, and only a small amplitude voltage pulse appears on the sense line because of the slight slope of the hysteresis loop in the vicinity of the 0 state. The amplitude of a core switched from the 1 state will be larger than the 0 state output, but the ratio may be as low as 2:1 or 3:1.

As shown in Figure 9.2, a value of select (write or read) current, I_S, can be determined in such manner that I_S will always switch the core, while $I_S/2$ will never switch it. Two windings may therefore be used to supply select current to the core. Coincident half-select currents through a particular core will be sufficient for switching. However, the currents should be accurately controlled, and the hysteresis characteristics of the cores in the memory must be uniform.

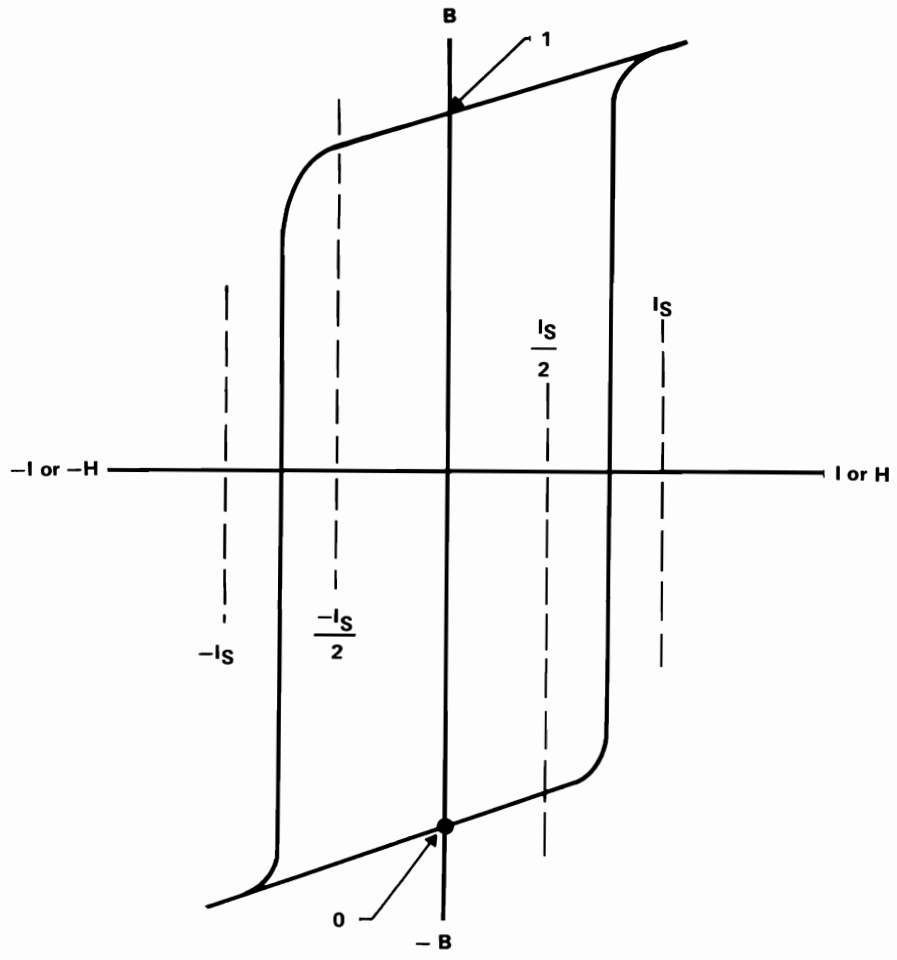


Figure 9.2. Characteristic Curve of a Magnetic Core

Application of a half-select current to a core causes traversing of minor hysteresis loops, thereby reducing the remanent flux density. This lessens the available output voltage when the core is switched, and lowers the ratio of the amplitudes of ones and zeros. For a practical core, the remanent flux density must converge at a fairly high value to be useful.

Cores are usually arranged in a matrix (see Figure 9.3). Half-select currents are supplied by the X and Y address lines. Any single core is selected by energizing its address lines with half-select currents. As other cores on the address lines will receive insufficient current for switching, the major flux change results from the switched core. Since only one core is selected at a time, a single sense line is sufficient for an entire core matrix or plane.

While Figure 9.3 shows only 25 cores in a 5 x 5 array, practical memories may utilize up to several thousand cores. A 64 x 64 array of 30-mil cores is a popular plane size. In an array of this size the minor flux changes from the half-selected cores, totaled, could cause an output pulse several times greater in amplitude than the 1 output from the switched core. Therefore the sense line is threaded through adjacent cores in opposite directions to cancel minor flux changes.

This causes an additional problem. Because of the sense-line arrangement, the output voltages from adjacent cores will be of opposite polarity. The sense amplifier must perform amplitude discrimination on 1 and 0 pulses of both positive and negative polarities.

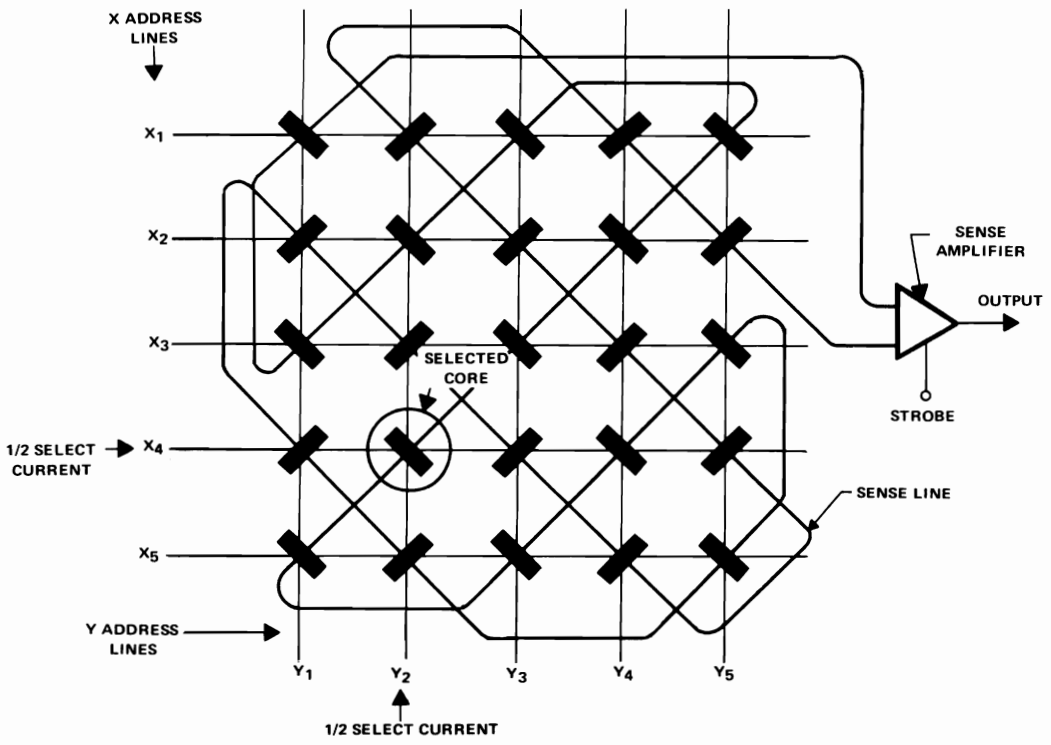


Figure 9.3. CCM Core Plane

The most severe design problem is noise originating in the high select current necessary for switching the cores. Noise appears on the sense line because of magnetic and capacitive coupling and the quantity and location of information being switched in the memory. While complete noise cancellation is never possible, a carefully designed sense line will present equal noise excursions at both sense-line terminals, thus conveying the noise to the sense amplifier as common-mode signals. An amplifier with high common-mode rejection can detect the small-amplitude differential signals from the switched core even in the presence of large common-mode signals.

The sense amplifier has a strobe input (see Figure 9.3). The strobe enables or disables the sense amplifier, allowing it to perform discrimination at signal time only. The maximum noise voltages usually occur at times other than when the signal is present.

Figure 9.4 shows the type of sense-line output signals for various X line and Y line input conditions. A sense amplifier tied to the sense line would be strobed off during a write sequence.

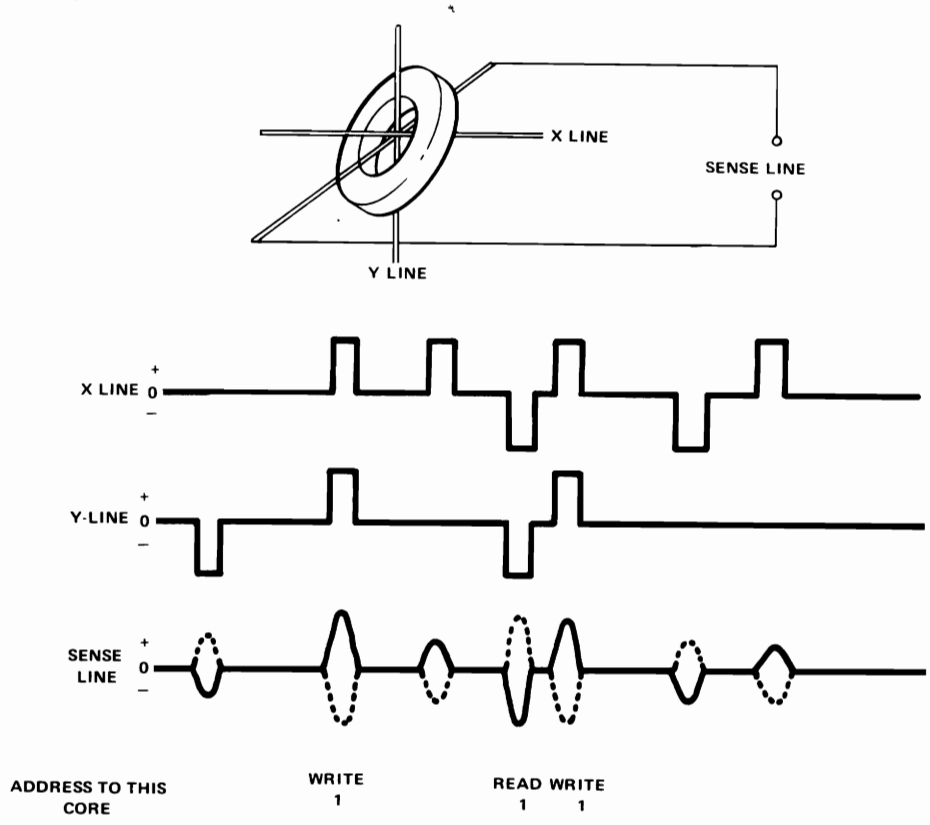


Figure 9.4. X Line, Y Line, and Sense Line Characteristics

Figure 9.5 shows typical sense-line output voltage waveforms resulting from $I_R/2$ and I_R level drive currents. Sense amplifiers have a reference level, or threshold, of some value plus or minus a possible variance or error. The total amount of possible error forms an error band about the sense threshold, as shown. It is evident from these curves that an adequate sense amplifier for this application would need a threshold of about 30 mV and a narrow error band.

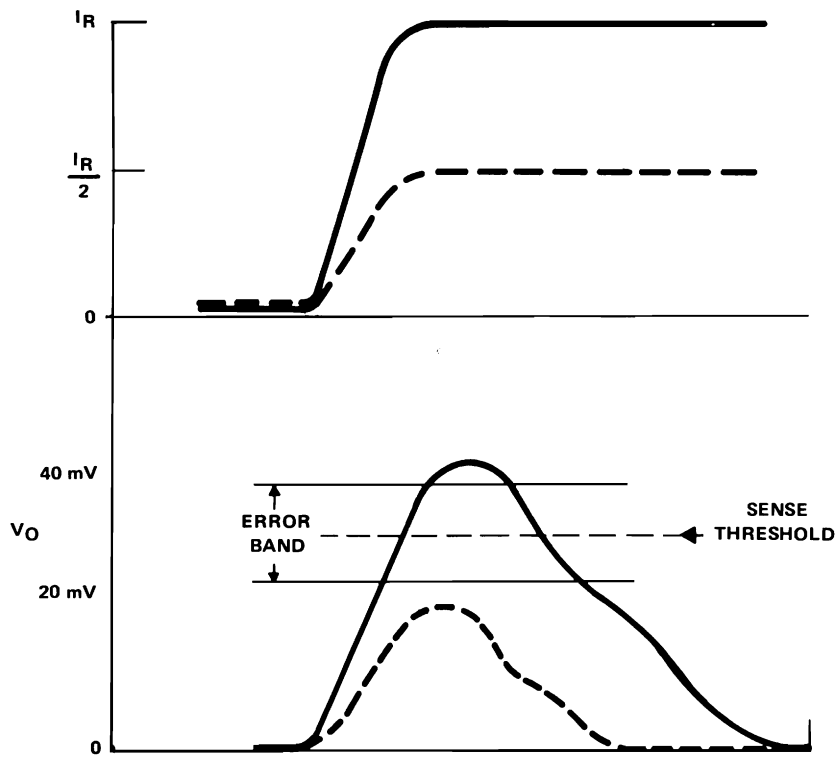


Figure 9.5. Typical Read and Sense Waveforms

Three basic types of memory systems are normally utilized: the two-dimensional (2D) system; the three-dimensional (3D) system; and the 2-1/2 dimensional (2-1/2D) system. The wiring configurations are shown in Figures 9.6, 9.7, and 9.8. The 2D system, although easy to wire, is used only in single-plane, scratchpad-type memories of no more than 1000-bit capacity. Each plane in a 3D system has a sense line and an inhibit line, as shown in Figure 9.7a. Inhibit lines are wired to oppose the Y lines. X lines and Y lines pass through all the planes, as shown in Figure 9.7b. The 2-1/2D system is a compromise between the complex 3D system and the simple 2D system. As shown in Figure 9.8, a single set of X lines is laced through all the memory planes, while each plane has its own set of Y lines. With this approach a single sense line may be used for several planes. An inhibit line or inhibit drive is not required.

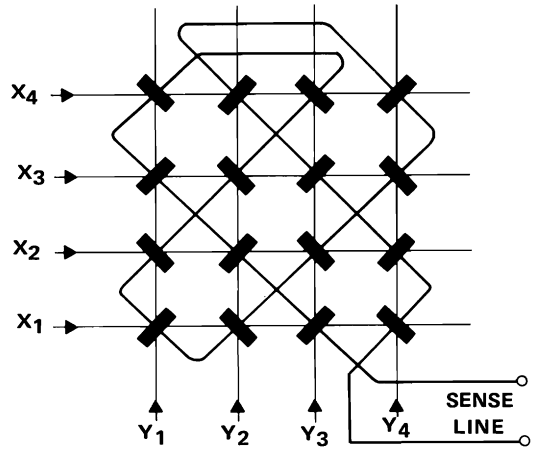


Figure 9.6. 2D Wiring Configuration

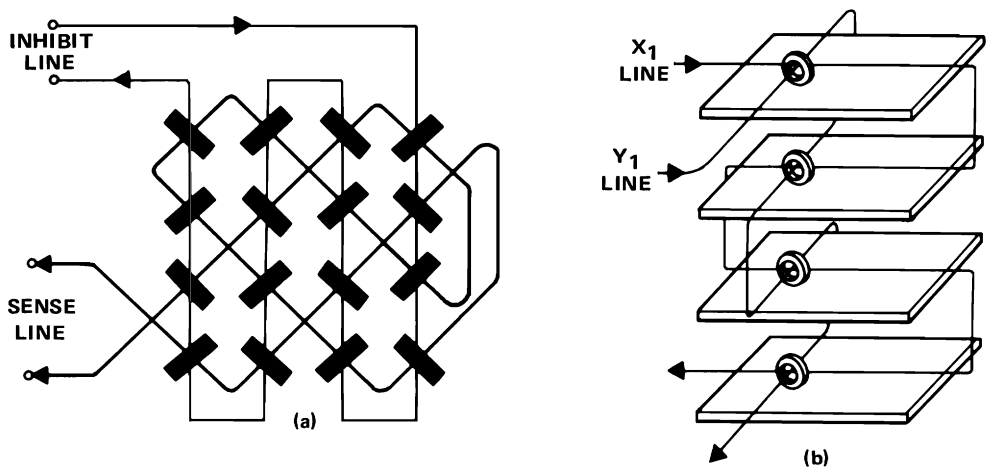


Figure 9.7. 3D Wiring Configuration

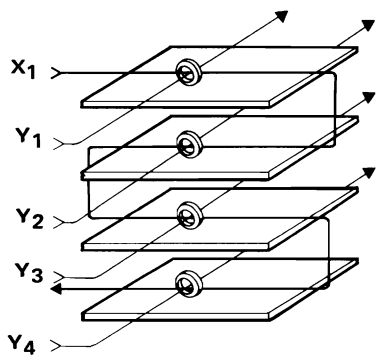


Figure 9.8. 2 1/2D Wiring Configuration

Figure 9.9 is a block diagram of a typical CCM system showing associated input, output, and control circuitry.

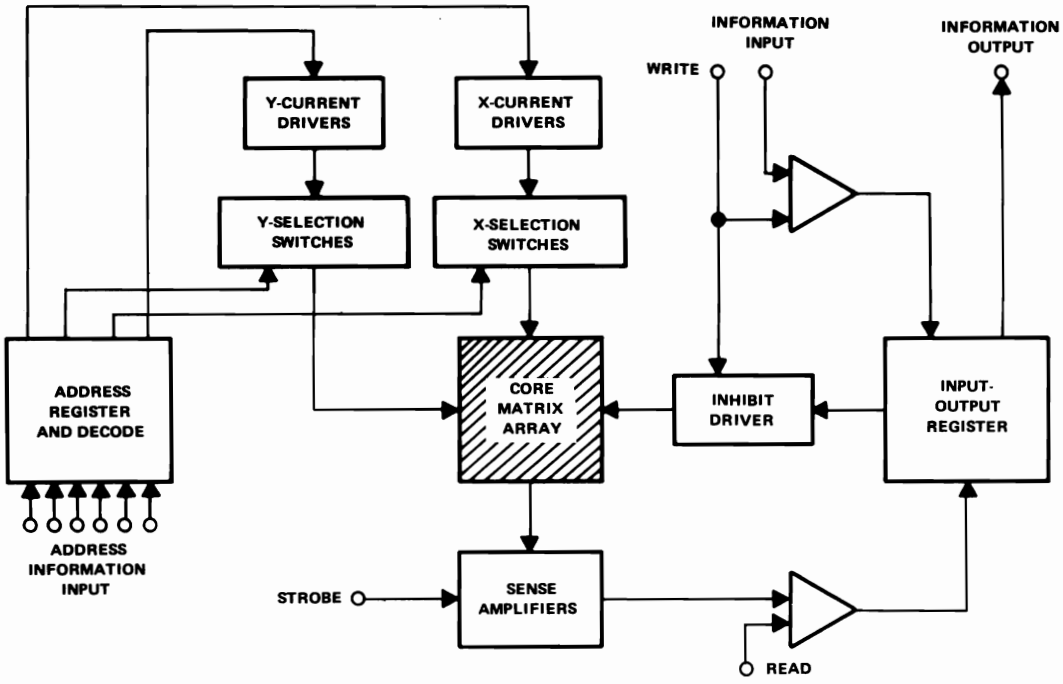


Figure 9.9. CCM System Block Diagram

9.2 CORE MEMORY DRIVERS

9.2.1 Driver Requirements

In CCM systems a selection matrix is necessary to so control the current in the cores that one core can be selected out of a large matrix. Discrete transistor-transformer combinations previously used in the driver section of line-selection schemes proved to be costly and space-consuming. Both of these problems were solved by integrated circuits that provide logic control with output capability for direct drive of diode matrixes and cores.

Core-drive requirements vary considerably depending on speed requirements and memory size. Total switching currents range from 200 mA for slow-speed, large-core stacks, to 1.2 A for small-core, high-speed memories. For coincident-current systems, half-current drive levels are 100 to 600 mA.

Core drivers must have low-saturation voltages. Driver outputs must have saturation levels of less than 1 volt at rated output to minimize package dissipation and guarantee adequate switching of power to the load.

When the driver is turned off the inductive kickback may be significant. Driver-output breakdown voltage or limiting must be adequate to prevent damage during turn-off. Since the address logic will generally be TTL it is desirable that the driver inputs be TTL compatible.

Although cores are usually the limiting factor in speed of operation, the drivers must be capable of operating in the 10-MHz range or higher, with minimum propagation delay.

9.2.2 Transistor Array Drivers

SN75303 Driver – High-speed, read-only memories (ROMs) in computers and calculators, plus the increasing use of thin-film, plated-wire, and core memories in the 2D or linear-select configuration, provide widespread applications for transistor arrays. Figure 9.9 depicts the configuration of the SN75303, a two-by-four transistor array designed for such systems.

Each SN75303 is a monolithic array of eight NPN transistors designed as a medium-current word-line driver. Selection is by base-emitter activation. This versatile type of control allows easy addressing and utilization of the device to drive many types of matrix systems.

Four base leads and two emitter leads, as shown in Figure 9.10, make up the inputs. Individual devices are activated by applying proper input levels to any one emitter and base. For example, by switching E1 to ground through an addressing device and applying a forward bias to B3, output C3·1 is enabled. Thus each of the eight outputs may be individually controlled.

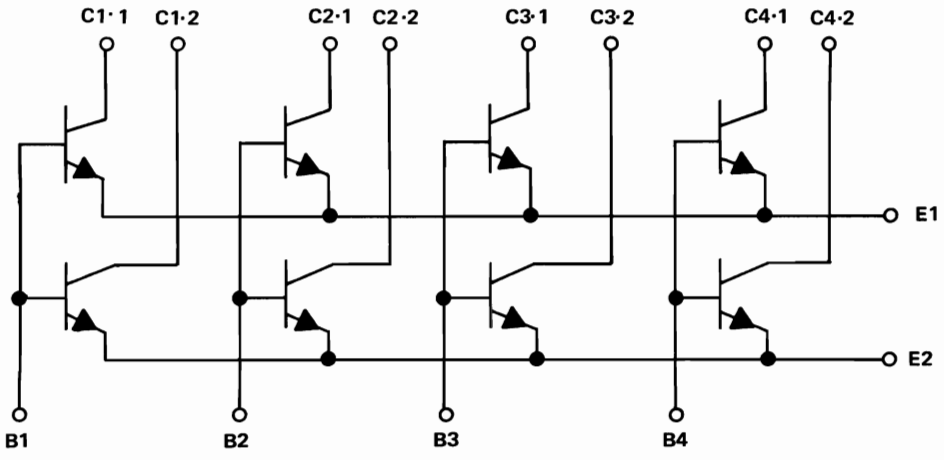


Figure 9.10. Transistor Configuration of the SN75303

Each collector of the array provides an output sink for a memory line. When enabled, it sinks one end of a word or bit line. Power to the line is furnished from the other end, as shown in Figure 9.11. Each output can handle 150 mA of current from a voltage source of up to 25 volts.

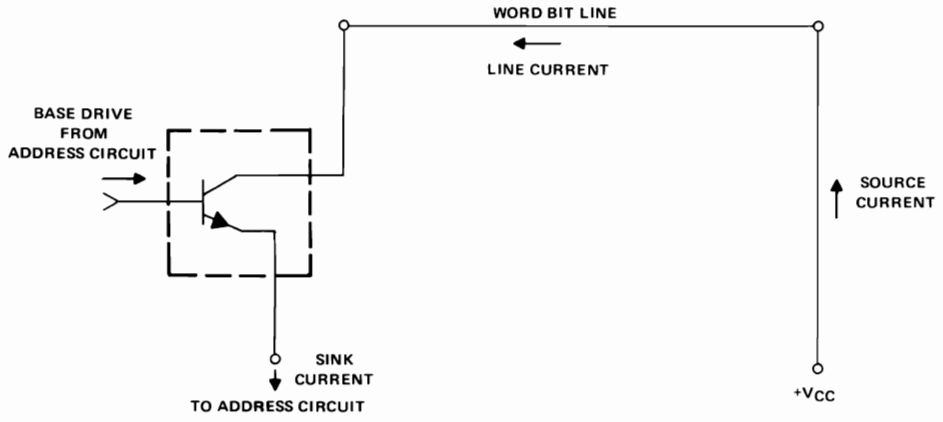


Figure 9.11. SN75303 as Line Selecting Sink

SN75308 Driver – Some plated-wire and thin-film memories and most core memories require line currents in the order of 500 mA. The SN75308, a two-by-four transistor array designed to handle these larger currents, is applicable to many control circuits as well as to memory circuitry. Figure 9.12 shows the transistor arrangement.

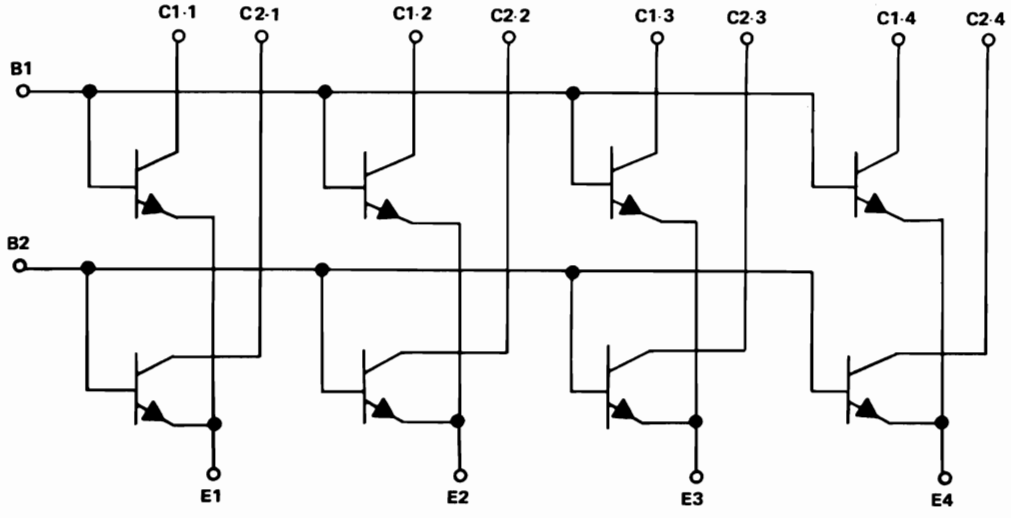


Figure 9.12. Transistor Configuration of the SN75308

Each SN75308 is a monolithic array of eight NPN transistors which can drive word lines without the aid of a transformer. Selection of any of the eight devices is by base-emitter activation, with four emitter control leads and two base leads forming the necessary matrix.

As with the SN75303, applying the proper dc levels to a single base lead and an emitter lead will select the output to be controlled. If E2 is taken to ground or a low positive level, and forward bias is applied to B2, the output C2.2 will be enabled. Control of the inputs is accomplished by the address circuitry.

Each collector of the array furnishes sinking for a memory drive line and may be the only switch controlling current in the line, as shown in Figure 9.13. This is an example of a read-only memory (ROM) for which the SN75308 is very useful.

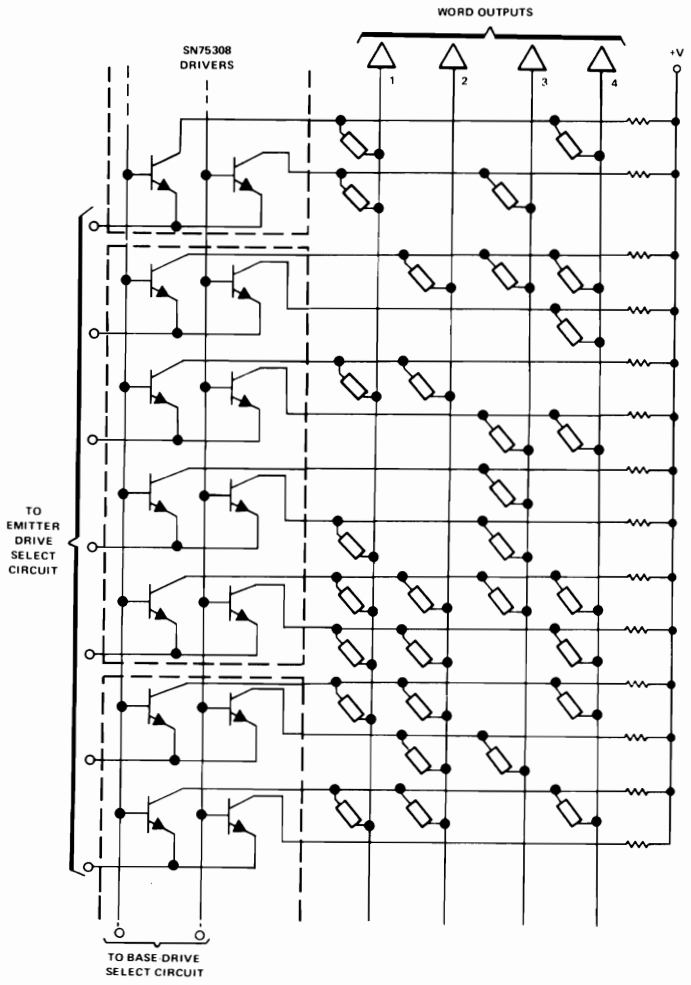


Figure 9.13. Read-Only Memory

Operation may be from as high as 25 volts. Figure 9.14 shows the device pin-out, available in 16-pin dual-in-line plastic or ceramic packages.

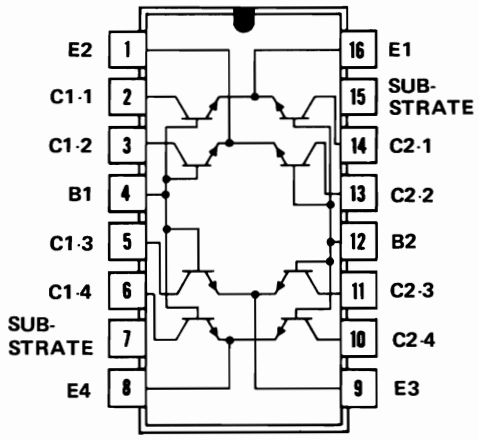


Figure 9.14. SN75308 Functional Diagram and Pin-Out

9.2.3 Integrated-Circuit Drivers

SN75324 Dual-Source Dual-Sink Driver with Decode Inputs – The SN75324 has been specifically designed to replace discrete transistor-transformer drivers used in magnetic memory circuits. This versatile, easy-to-use driver consists of four fast, high-current switches controlled by internal logic circuitry having inputs compatible with TTL and other standard logic systems. Figure 9.15, the SN75324's functional diagram, shows the pin-out of the 14-pin dual-in-line plastic package.

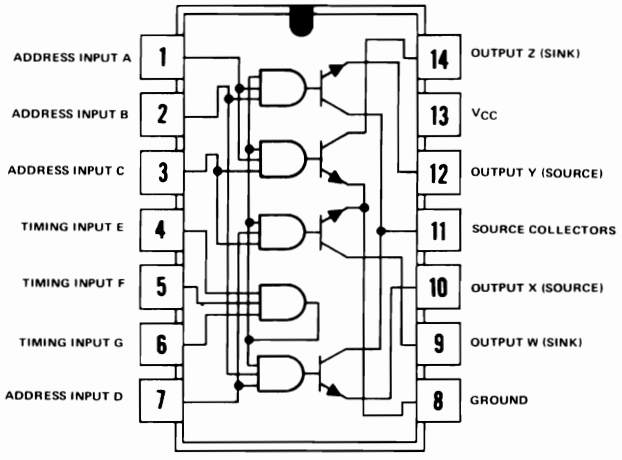


Figure 9.15. SN75324 Functional Diagram and Pin-Out

Because of the high-noise environment in which the SN75324 is intended to operate, the input logic levels have been purposely designed to be somewhat higher than standard 54/74 TTL logic levels, as compared below:

	54/74 TTL	SN75324
$V_{out(0)}$	0.4 V max.	— — —
$V_{out(1)}$	2.4 V min.	— — —
$V_{in(0)}$	0.8 V max.	1.0 V max.
$V_{in(1)}$	2.0 V min.	3.5 V min.
$V_{threshold}$	1.4 V typ.	2.3 V typ.

The higher logic 0 input level, $V_{in(0)}$, of the SN75324 guarantees a dc noise margin of 600 mV when driven from 54/74 TTL. However, the higher $V_{in(1)}$ of the SN75324 (3.5 V) leads to some minor difficulties when using 54/74 TTL. The minimum guaranteed logic 1 level of 2.4 V at a 54/74 TTL output falls short of the 3.5-V minimum level required at the SN75324 input. However, this problem can be readily solved by using a pull-up resistor at the gate output as shown in Figure 9.16.

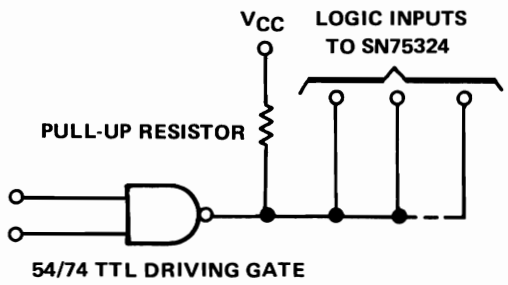


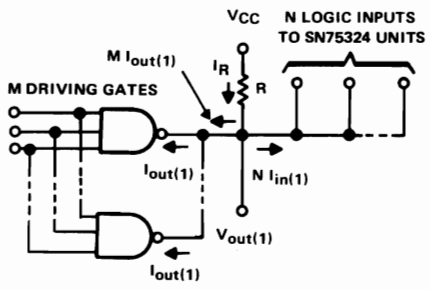
Figure 9.16. Input to SN75324 from 54/74 TTL Using Pull-Up Resistor

Because of the high logic 0 input current of the SN75324 (12 mA for the timing inputs, 6 mA for the address inputs), it may be desirable to drive the inputs with 54/74 TTL buffer gates (SN7440 or SN74H40) to assure adequate sink-current capability. Each SN7440 buffer gate output is specified at 0.4 V maximum $V_{out(0)}$ at a sink current of 48 mA. The $V_{out(0)}$ for the SN74H40 buffer gate is 0.4 V at a sink current of 60 mA. If additional sink current is required, the inputs and outputs of both gates in the SN7440 or SN74H40 package may be paralleled for 96 or 120 mA capability, respectively. (This parallel connection requires no significant sacrifice, if any, in switching characteristics, but the outputs of these gates should not be paralleled without also paralleling inputs. Otherwise one or both of the gates can be damaged because of the active pull-up or totem-pole output configuration.)

A large number of SN75324 inputs may also be driven from the output of any of several 54/74 TTL decode/drivers. For example, the output of the SN7445 BCD-to-Decimal Decoder/Driver can sink 80 mA at $V_{out(0)}$ of 0.9 V or sink 20 mA at $V_{out(0)}$ of 0.4 V. Since the maximum $V_{in(0)}$ of the SN75324 is 1.0 V, the SN7445 can drive the SN75324 with a pull-up resistor.

When a pull-up resistor is used at the driving gate output, its value must be selected to ensure proper logic levels. The worst-case resistor values may be readily calculated using available driving-gate data-sheet information.

The maximum resistor value is calculated to ensure that sufficient current is available when the driving gate output is high (off). This current must supply the SN75324 input as well as the driving gate output. For a logic 1 it is necessary to maintain 3.5 V minimum at the SN75324 input. A suggested method of calculating the maximum resistor value is shown in Figure 9.17. The minimum value of the resistor is calculated to ensure that its current plus that from the SN75324 inputs will not cause the output voltage $V_{out(0)}$ of the driving gate to exceed the maximum of 1.0 V. (See Figure 9.18.)



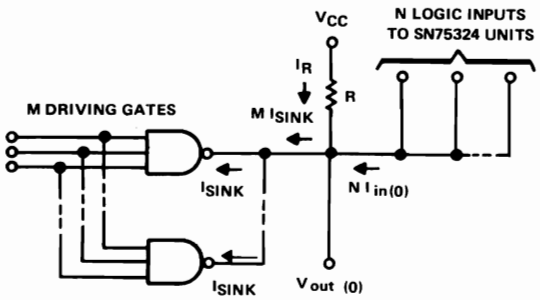
Voltage across R = $V_R = V_{CC}(min) - V_{out(1)}$

Current through R = $I_R = M\,I_{out(1)} + N\,I_{in(1)}$

Therefore $R_{(max)} = \dfrac{V_{CC(min)} - V_{out(1)}}{M\,I_{out(1)} + N\,I_{in(1)}}$

where $V_{out(1)}$ = 3.5 V minimum to drive SN75324 input
$I_{out(1)}$ = 250 μA maximum for 54/74 TTL gate output
$I_{in(1)}$ = 100 μA maximum for SN75324 timing inputs
= 200 μA maximum for SN75324 address inputs
M = number of parallel driving gates
N = number of parallel SN75324 inputs

Figure 9.17. Calculation of Maximum Value of Pull-Up Resistor in Figure 9.16



Current in resistor = $I_R = M\,I_{sink} - N\,I_{in(0)}$

Voltage across resistor = $V_R = V_{CC(max)} - V_{out(0)}$

$$R_{(min)} = \frac{V_{CC(max)} - V_{out(0)}}{M\,I_{sink} - N\,I_{in(0)}}$$

where $I_{in(0)}$ = 6 mA maximum for address inputs
$I_{in(0)}$ = 12 mA maximum for timing inputs
I_{sink} = maximum specified sink current of driving gate
$V_{out(0)}$ = maximum specified "0" level output voltage of the driving gate (≤ 1.0 V), which is 0.4 V for 54/74 TTL
M = number of parallel driving gates
N = number of parallel SN75324 inputs

Figure 9.18. Calculation of Minimum Value of Pull-Up Resistor in Figure 9.16

After determining the worst-case minimum and maximum pull-up resistor values, any value between the limits may be selected. (Obviously the calculated minimum value must be below the calculated maximum value to be practical.) Selecting a resistor value near the minimum limit will raise the logic 1 voltage and thereby improve the logic 1 noise margin.

An example of an SN74H40 buffer gate driving eight SN75324 address inputs is shown along with sample calculations in Figure 9.19. If, in this example, a value of 400 Ω is selected for the pull-up resistor, the guaranteed logic levels at the SN75324 inputs are 0.4 V maximum for $V_{in(0)}$ and 4.0 V minimum for $V_{in(1)}$. This resistor results in guaranteed dc noise margins of 600 mV at the logic 0 level and 500 mV at the logic 1 level under worst-case conditions.

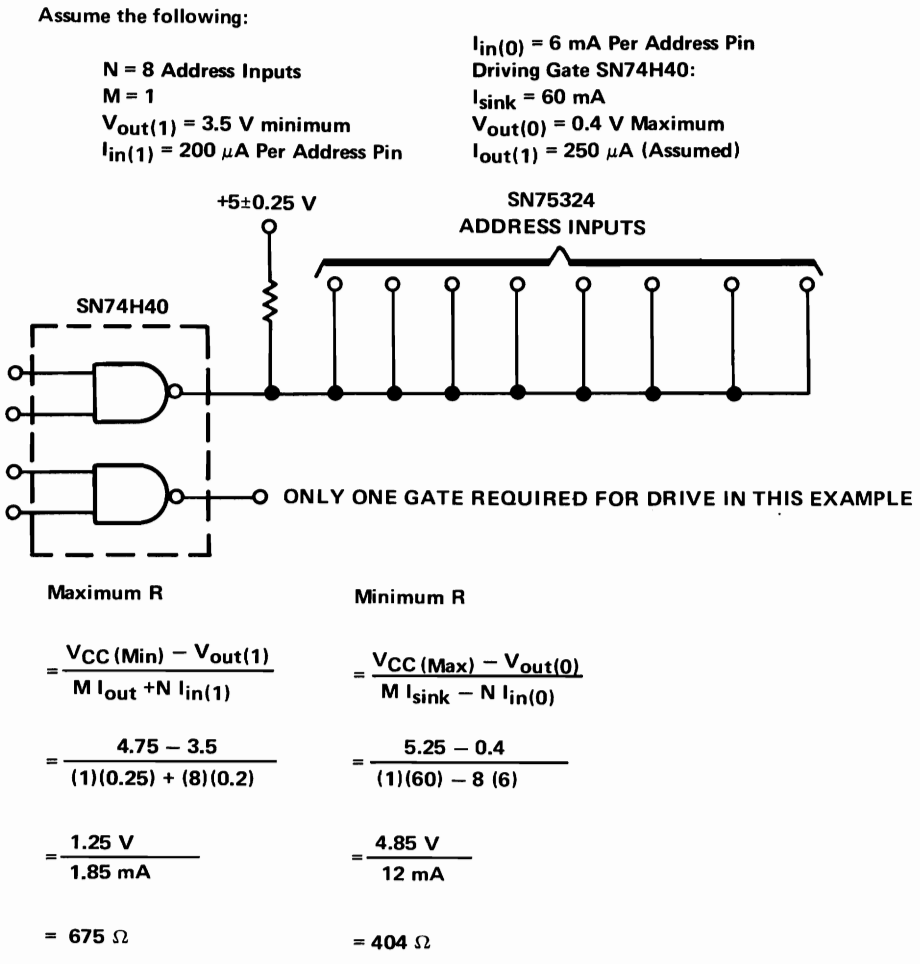


Figure 9.19. Sample Calculation of Pull-Up Resistor Value for SN74H40

In any memory-drive application, circuit-board mounting of the SN75324 should be judiciously considered to satisfy the problems of signal transmission, noise, and thermal management. If flat packs are used, they should be mounted flat on a wide copper lamina using a thermal compound, or mounted base up with high-velocity air flowing across them. A row of flat packs should run perpendicular to the cooling air stream rather than along it to avoid accumulated heating of air. If a copper lamina is used, it should be expanded to fill the empty area on the circuit board to enlarge the cooling surface. Furthermore, because memory-drive and logic currents share the same electrical ground in a direct-coupled system, it is necessary to take special care to minimize ground noise.

The three timing inputs E, F, and G are emitter inputs to a TTL multi-emitter input gate. As can be seen in Figure 9.20, the collector of the timing input gate is tied to one emitter of each address input gate. Thus, if any one of the three timing inputs is at a logic 0, all the address input gates will be disabled.

The timing inputs provide for individual device selection and control. The multiple input allows for special logic considerations.

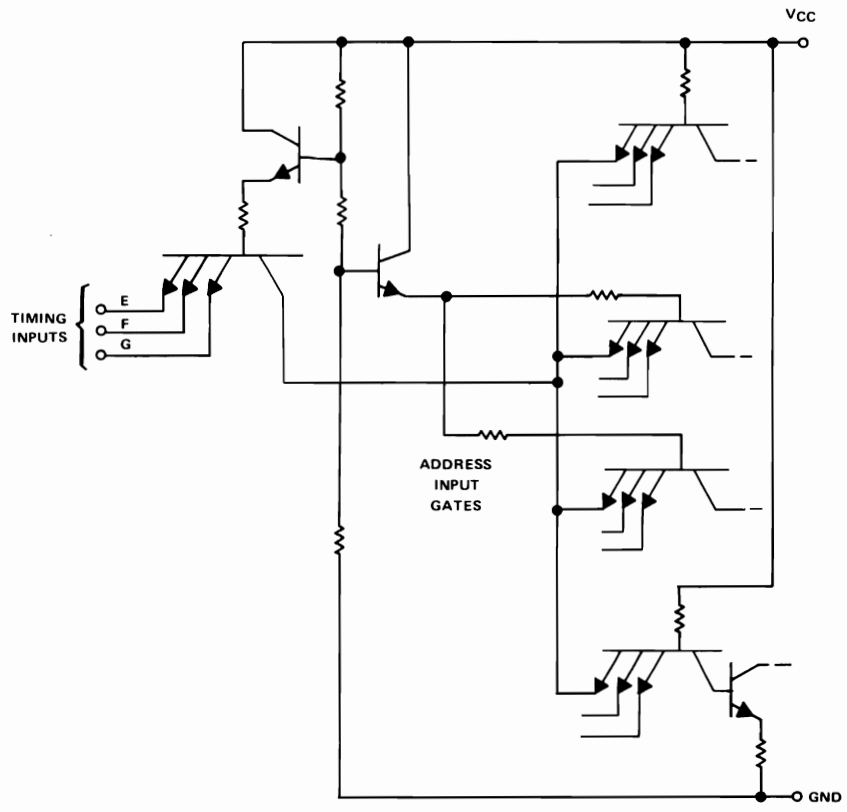


Figure 9.20. Timing Input Gate Configuration of the SN75324

Address inputs A, B, C, and D also have TTL-compatible input gates controlling the four output switches. The addressing circuitry driving these inputs needs to be controlled to assure that only one output switch comes on at a time. Table 9.1 shows the input combinations required for the various outputs. Note that with some input combinations it is possible to get more than one output on at a time. This is undesirable, as the unit may overheat unless a preventive method such as using inverters on the inputs is employed (see Figure 9.21). The inverter input conditions are also listed in Table 9.1.

Table 9.1. SN75324 Truth Table

INPUTS									OUTPUTS			
Inverter Address		Direct Address				Timing			Sink	Sources		Sink
1	2	A	B	C	D	E	F	G	W	X	Y	Z
0	0	0	0	1	1	1	1	1	ON	OFF	OFF	OFF
0	1	0	1	0	1	1	1	1	OFF	ON	OFF	OFF
1	1	1	1	0	0	1	1	1	OFF	OFF	ON	OFF
1	0	1	0	1	0	1	1	1	OFF	OFF	OFF	ON
X	X	X	X	X	X	0	X	X	OFF	OFF	OFF	OFF
X	X	X	X	X	X	X	0	X	OFF	OFF	OFF	OFF
X	X	X	X	X	X	X	X	0	OFF	OFF	OFF	OFF

X = Logic 1 or 0 (irrelevant)

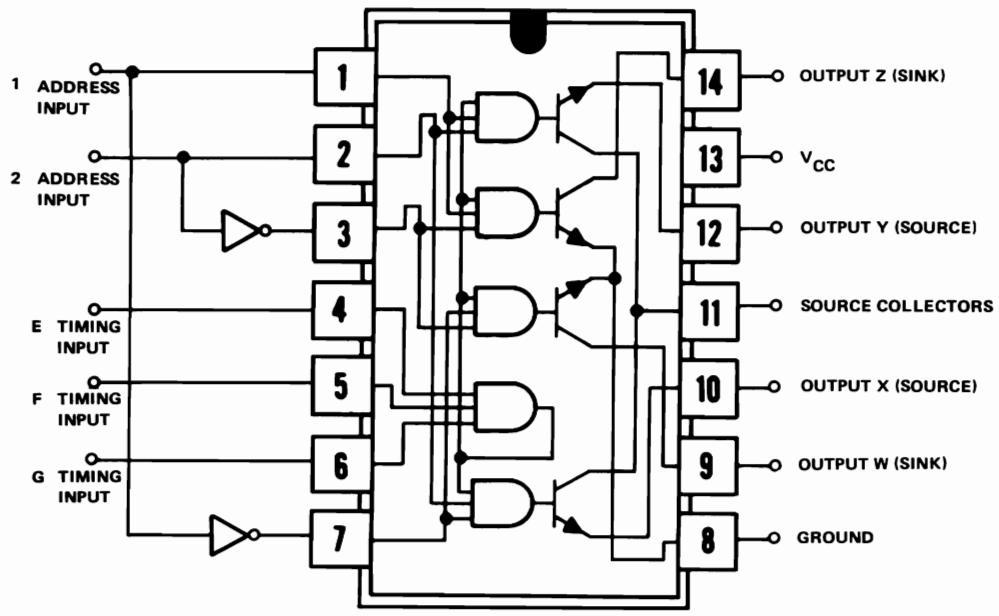


Figure 9.21. Interconnection of Address Inputs

As shown in Figure 9.21, each device contains two sinking outputs (Z and W), which may be used to sink the line current to ground when enabled. Figure 9.22 shows the sink output device and its primary control circuitry. If input drive from the timing input gate is high and the address inputs are high, the sink-circuit input gate is enabled, allowing current to flow through the base-collector junction to the sink drivers connected in a Darlington configuration for quick response to the input signal. The overdrive transistor during turn-on shunts the driver collector resistor, providing extra base drive and thus enhancing turn-on by charging the transition and Miller capacitances of the sink. During conduction the sink collector is pulled to ground, providing the output sinking and effectively disconnecting the stack discharge resistor from the overdrive. When the device is being turned off, the equivalent 14-V internal clamping diode allows inductive line energy to be conducted through it, limiting voltage excursions which might otherwise generate excessive system noise.

Each SN75324 package also contains two source outputs, used to furnish the read/write currents to the line (see Figure 9.23). The +3-volt reference voltage for

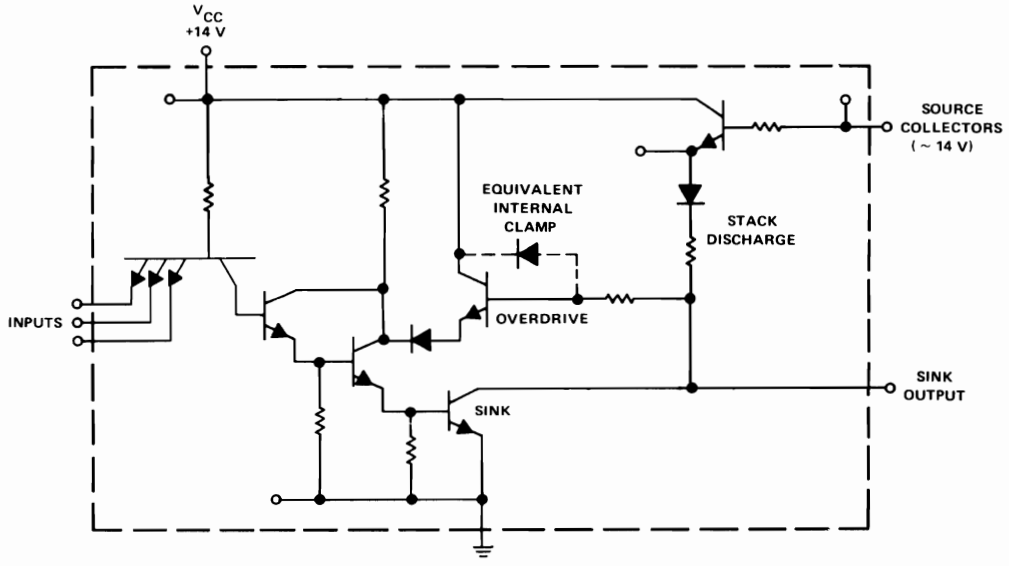


Figure 9.22. An Individual Sink Circuit of the SN75324

the base of the input gate is derived from the voltage-divider network and emitter follower as shown in Figure 9.24. This sets the threshold level of the inputs at about 2.3 volts. During the off state, one of the input emitters will be low because of the address circuitry or limiting circuitry. This condition keeps the drivers' input bases low, holding them and the source outputs off.

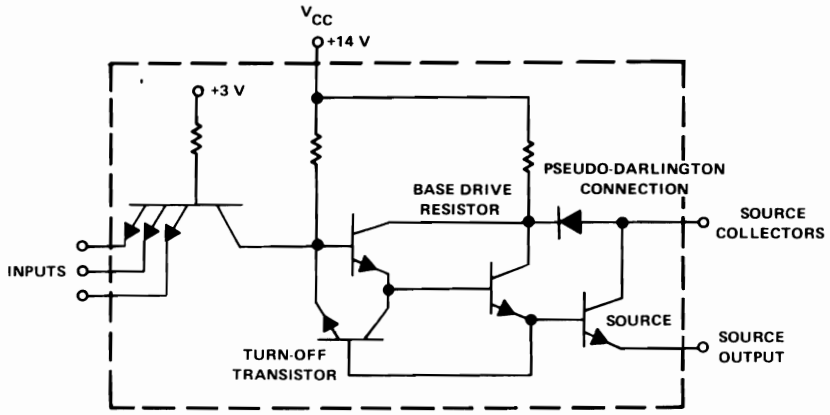


Figure 9.23. An Individual Source Circuit of the SN75324

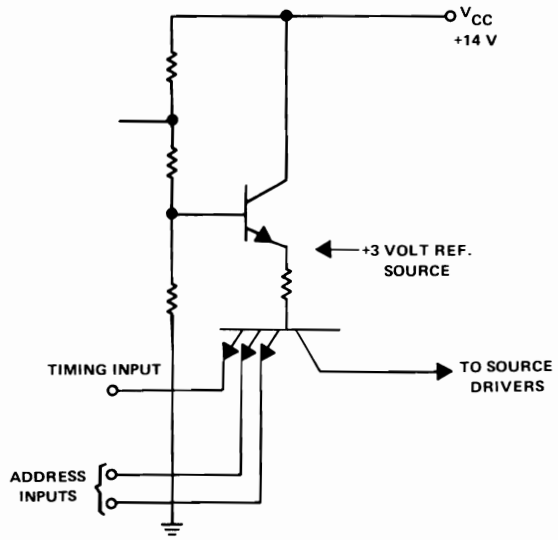


Figure 9.24. Internal Reference Voltage Source for Address Input Base Voltage, SN75324

During the turn-on transient the input emitters that were low are brought to a logic 1 level, allowing the input gate collector base junction to conduct, driving the input base of the drivers. Also, during this transitional period the diode in the pseudo-Darlington connection is forward biased, furnishing extra base current to the base of the source, enhancing the turn-on characteristics. Once the source becomes stable the source collector will have dropped to a low value, reverse-biasing the diode, and the base drive resistor will furnish all of the current needed to hold the source in saturation.

During the turn-off transient an emitter of the input gate is pulled low or back to a logic 0. As this happens the collector of the input gate is also pulled low, and, with it, the driver's input base and the emitter of the turn-off transistor. The turn-off transistor is now turned on, quickly removing the base charge from the pseudo-Darlington pair and holding the source base at an off potential.

Figure 9.25 shows a basic circuit utilizing the SN75324 to provide read/write drive to memory lines.

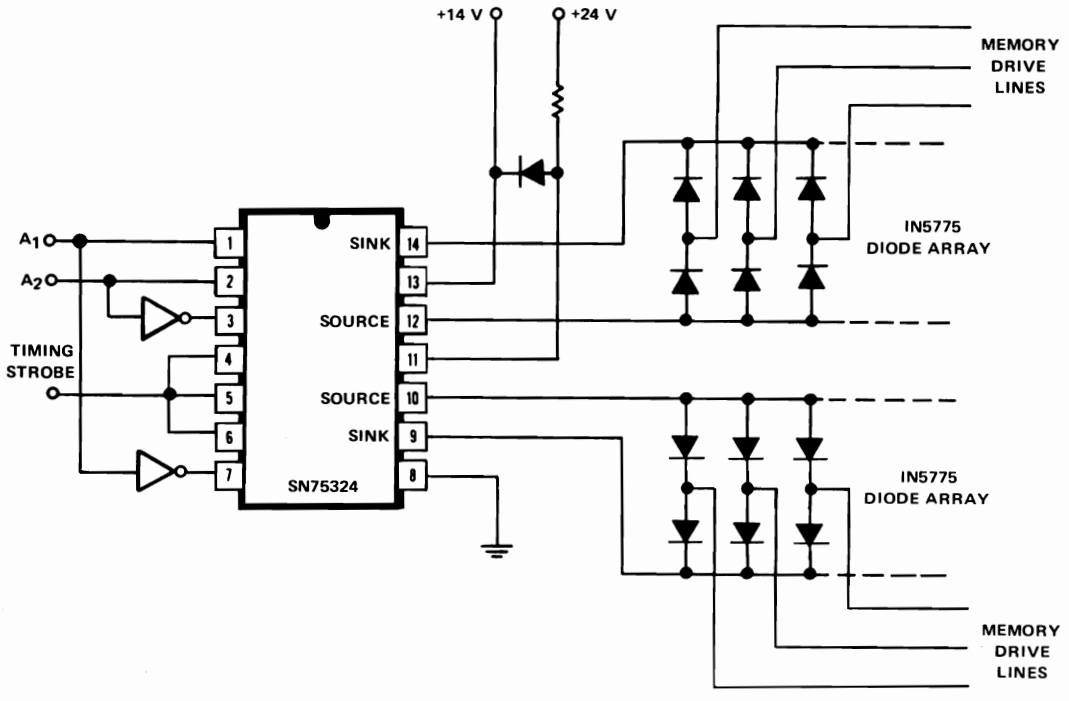


Figure 9.25. Basic Circuit Using the SN75324 to Provide Read/Write Drive

SN75325 High-Current Dual-Source Dual-Sink Core Driver — The SN75325 provides the necessary drive for large high-speed memories. Cores used in high-speed systems are generally smaller, requiring larger currents to switch them. The SN75325 has TTL-compatible inputs and an output drive capability of 600 mA from 25-volt supplies.

Figure 9.26 shows the basic diagram and pin-out for the SN75325, a dual sink and dual source in one package. Each output is controlled by its own address input and a strobe. There are two strobes, one for the sinks and one for the sources. The truth table (Table 9.2) shows input control requirements. Source drive level capability may be adjusted with a resistor between pins 13 and 16. Each sink-output collector has an internal pull-up resistor in parallel with a clamping diode connected to V_{CC2}.

Table 9.2. SN75325 Truth Table

Address Inputs				Strobe Inputs		Outputs			
Source		Sink		Source	Sink	Source		Sink	
A	B	C	D	S1	S2	W	X	Y	Z
0	1	X	X	0	1	ON	OFF	OFF	OFF
1	0	X	X	0	1	OFF	ON	OFF	OFF
X	X	0	1	1	0	OFF	OFF	ON	OFF
X	X	1	0	1	0	OFF	OFF	OFF	ON
X	X	X	X	1	1	OFF	OFF	OFF	OFF
1	1	1	1	X	X	OFF	OFF	OFF	OFF

X = LOGIC 1 OR 0 (IRRELEVANT)

NOTE: Not more than one output is to be on at any time.

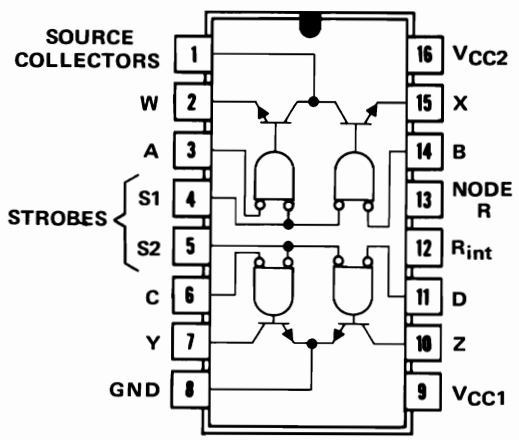


Figure 9.26. SN75325 Functional Diagram and Pin-Out

This arrangement provides protection from the voltage surges associated with switching of inductive loads.

Figure 9.27 shows the basic application configuration, with a source from one package driving a typical memory line, and a sink from another package to ground the other end of the line.

To improve on the wiring combinations available for large memories, a quad sink in one package and a quad source in one package are desirable. The SN75326 quad sink and SN75237 quad source provide this versatility.

SN75326 Quad Sink Driver — The SN75326 (Figure 9.28) is operated from a single 5-volt supply, and outputs and output clamps are rated at 24 volts. The amount of base drive available to the outputs may be increased by connecting an external resistor between pins 4 and 12.

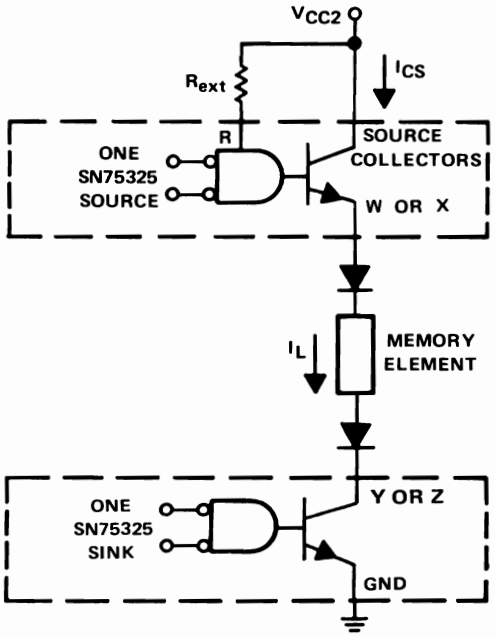


Figure 9.27. Basic Application of the SN75325

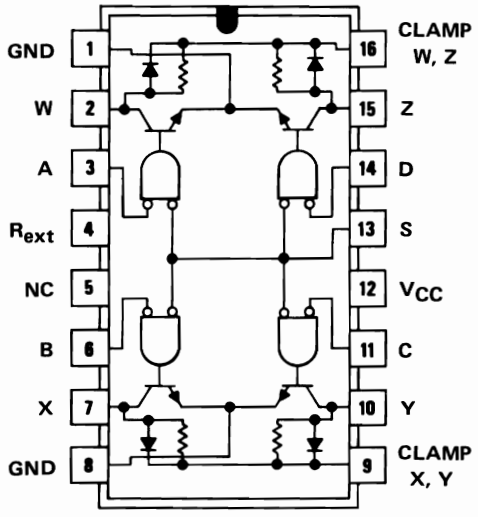


Figure 9.28. SN75326 Functional Diagram and Pin-Out

SN75327 Quad Source Driver — The SN75327 (Figure 9.29) is operated from two supplies: V_{CC1} = 5 V and V_{CC2} = 24 V maximum. The SN75327 outputs are rated at 24 volts.

Base drive to the outputs may be supplied either internally or externally. When pins 4 and 5 are connected, the amount of base drive available for any output is set internally by a 575-ohm resistor. This resistor value provides adequate base drive for source currents of up to 375 mA with a V_{CC2} of 15 volts, or 600 mA with a V_{CC2} of 24 volts. When source currents greater than 375 mA are required, a resistor of appropriate value should be connected between V_{CC2} and pin 4. When using an external resistor, pin 5 must be left open. Value of the external resistor may be determined by using the following equations:

$$R_{EXT} = \frac{16\left[V_{CC2(min)}\text{-}V_S\text{-}2.2\right]}{I_L\text{-}1.6\left[V_{CC2(min)}\text{-}V_S\text{-}2.9\right]}$$

where

R_{EXT} is in kΩ

V_S is source output voltage in volts with respect to ground

$V_{CC2(min)}$ is lowest expected value of V_{CC2} in volts

I_L is load current in mA

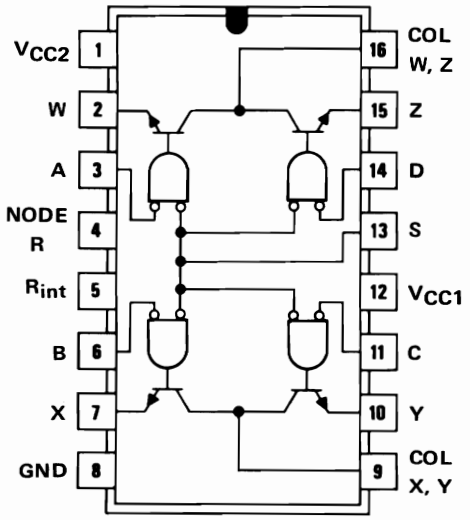
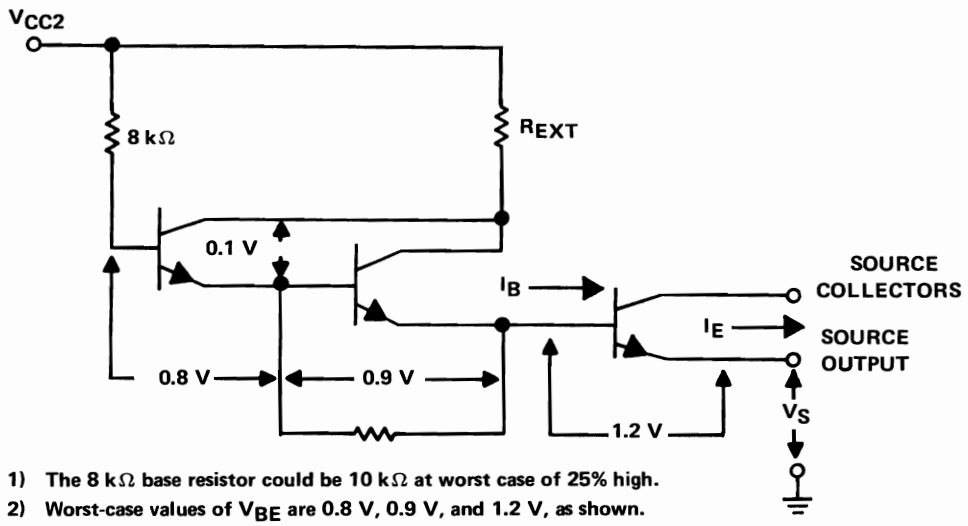


Figure 9.29. SN75327 Functional Diagram and Pin-Out

Derivation of the equation for R_{EXT} is given in Figure 9.30. The current into pin 4 should be limited to 60 mA.



1) The 8 kΩ base resistor could be 10 kΩ at worst case of 25% high.
2) Worst-case values of V_{BE} are 0.8 V, 0.9 V, and 1.2 V, as shown.
3) Total V_{BE} drops from the 8 kΩ resistor to the emitter output equal 2.9 V. Total from R_{EXT} is 2.2 V, including 0.1 V $V_{CE(sat)}$.

4) $$I_B = \frac{I_E}{h_{FE}+1} = \frac{V_{CC2}-V_S-2.9\text{ V}}{10\text{ k}\Omega} + \frac{V_{CC2}-V_S-2.2\text{ V}}{R_{EXT}}$$

For $h_{FE} = 15$, $h_{FE} + 1 = 16$ (min of output stage), the equation may be written as:

$$I_E = \frac{16\,(V_{CC2}-V_S-2.9\text{ V})}{10\text{ k}\Omega} + \frac{16\,(V_{CC2}-V_S-2.2\text{ V})}{R_{EXT}}$$

If I_E is in mA and R_{EXT} is in kΩ,

$$I_E R_{EXT} = R_{EXT}\,1.6\,(V_{CC2}-V_S-2.9) + 16\,(V_{CC2}-V_S-2.2)$$

Therefore: $$R_{EXT} = \frac{16\,(V_{CC2}-V_S-2.2)}{I_E - 1.6\,(V_{CC2}-V_S-2.9)}$$

Figure 9.30. Derivation of Equation for External Resistor for SN75327

Figure 9.31 is a basic diagram showing use of one source of an SN75327 to switch current from V_{CC2} to a memory drive line, and one sink of an SN75326 to switch the other end of the line to ground. The external diodes shown are steering diodes which are used when multiplexing.

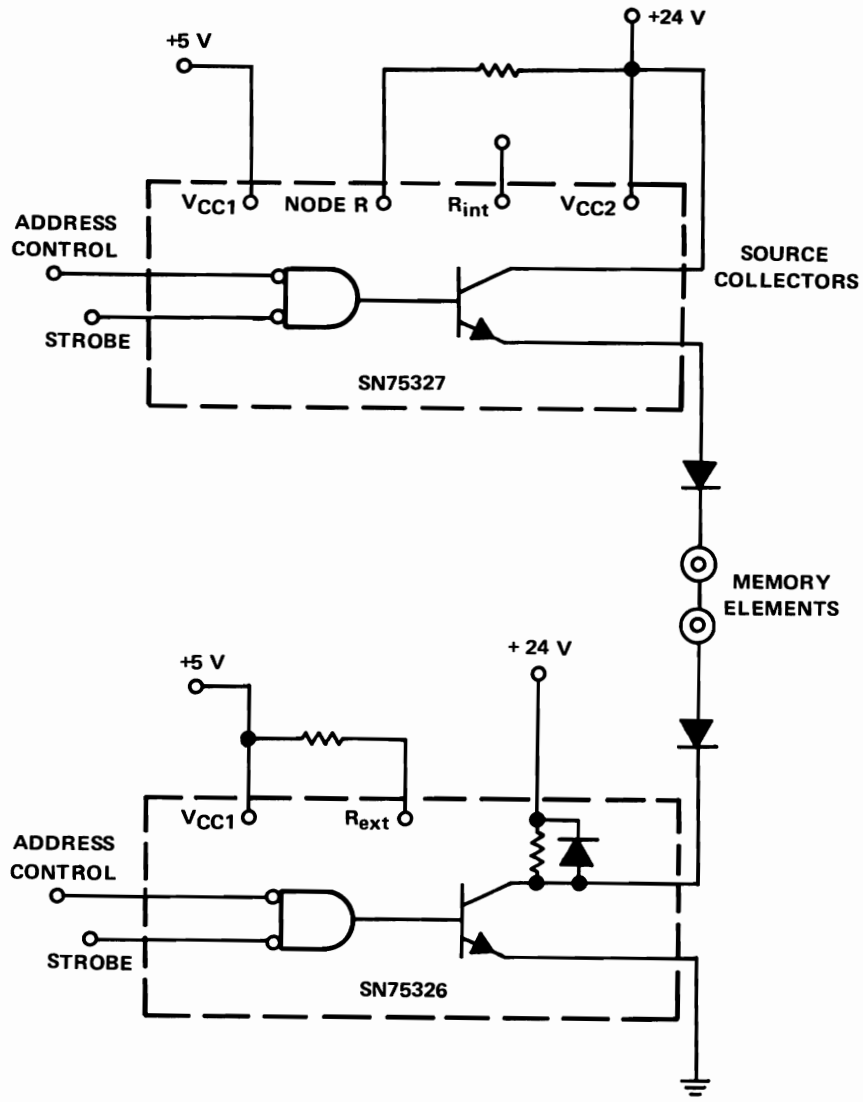


Figure 9.31. SN75326 and SN75327 Used as a Memory Driver

SN55329 Eight-Bit Memory Driver — Although the SN75324, SN75325, SN75326 and SN75327 provide the drive requirements, control characteristics, and versatility desired in most core memory systems, some additional features may be needed for high-reliability military-type equipment. The SN55329, an eight-bit core-memory driver, has been designed to fill these requirements. Some features of the SN55329 are:

MSI TTL 8-bit core driver
24-lead metallized-ceramic flat package
Full temperature operation, −55°C to +110°C
Decoded high-current outputs
Three-state selection and timing
Bipolar output currents to within ±5% by four shared external resistors
Output termination resistors
Fast switching times
Package standby power only 30 mW (typical)
Internal power control does not require power-supply sequencing

The device's functional diagram is shown in Figure 9.32. The integrated circuit contains eight identical bipolar, three-state, high-current drivers. A 3-line to 8-line

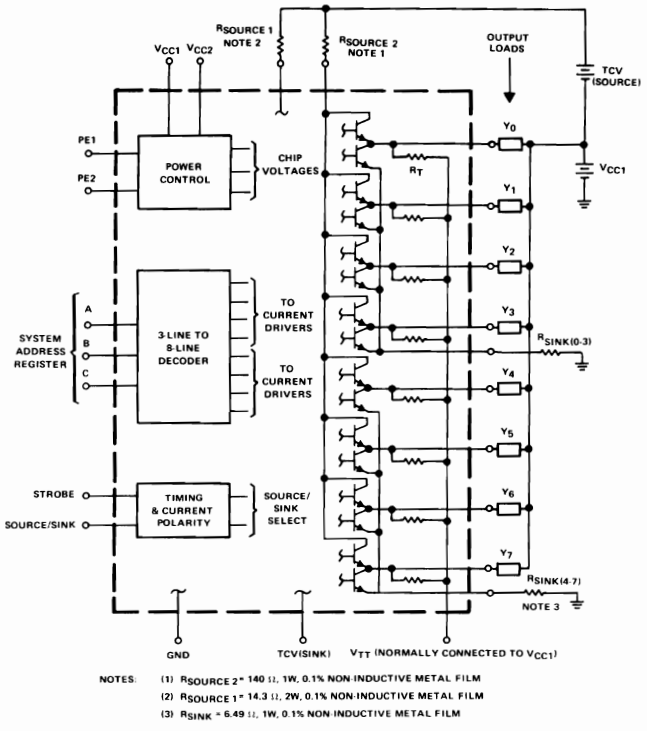


Figure 9.32. SN55329 Functional Diagram

decoder is provided for the system address register (SAR) inputs A, B and C. A package enable control (PE1) allows minimum device power dissipation during standby conditions. PE2 permits multiple chip control. Another input allows the selection of source or sink mode of operation.

Figure 9.33 shows a typical 1-μs memory driver cycle. At t = 0 the power-enable (PE1) input is switched low, followed by a PE2 input which selects the chip, resulting in V_{CC1} and V_{CC2} voltage activation. Decoder input SAR bits A, B, and C are set to select one of eight output current drivers, and the source/sink input level then selects the phase of the output driver. This selected driver remains off until the timing strobe input is pulsed low, controlling the width of the source or sink output current pulse through the core load. The output core lines return to V_{CC1} as shown in Figure 9.32. Amplitude of the source output is controlled by the precision external resistors $R_{source1}$ and $R_{source2}$ connected to the temperature-controlled voltage — TCV (source). Sink output amplitude is controlled by two precision non-inductive resistors R (sink) and control voltage TCV (sink). Completion of the memory cycle is accomplished within 1 μs as indicated in Figure 9.33.

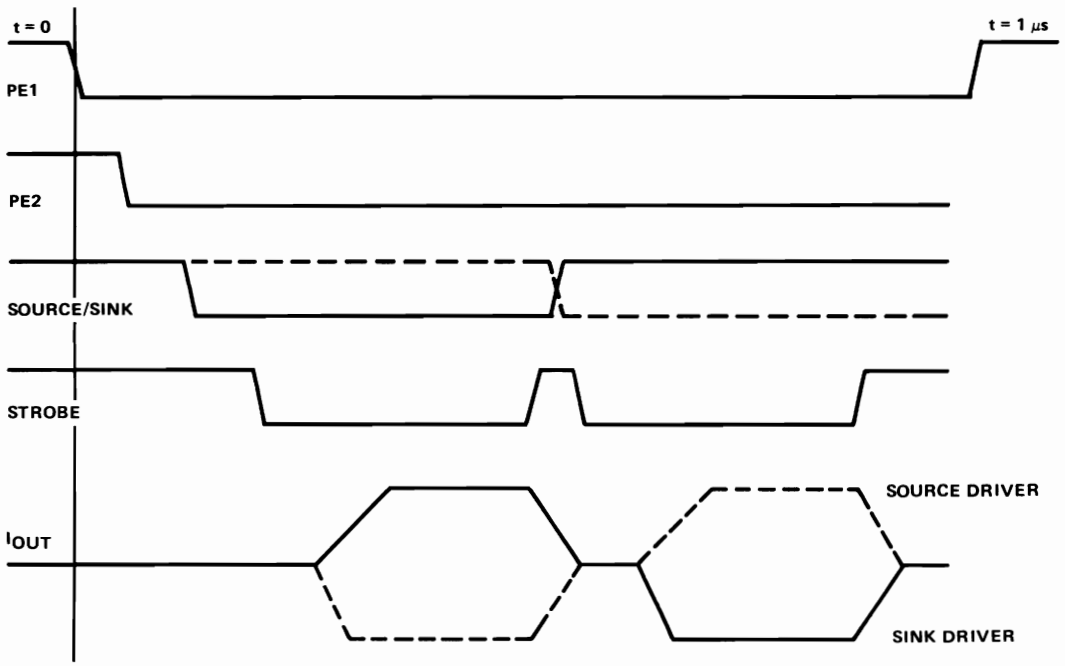


Figure 9.33. Typical One-Microsecond Memory Driver Cycle

9.2.4 Typical Memory-Driver Applications

Figure 9.34 shows a sample implementation of a read-only memory drive using an SN74154 decoder, SN7404 inverters, and a 2N5449 discrete transistor for addressing the SN75303 sections driving the required memory lines.

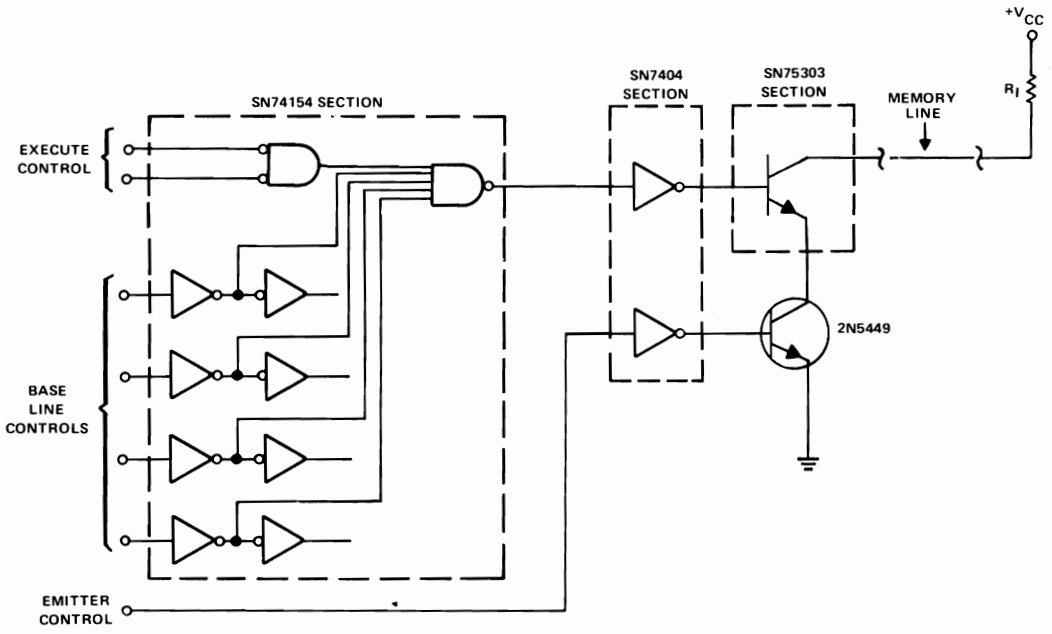


Figure 9.34. Read-Only Memory Drive Circuit

Figure 9.35 is a resistive read-only memory array using the SN75303 as the word-line drivers.

Figure 9.36 shows a combination of SN75308 and SN75325 drivers used in implementing a 2D memory drive. The word-line drivers must be bidirectional, with the read current greater than twice the I_{pw}. The bit current need only be in one direction and only of a magnitude I_{pw}. Therefore, SN75325 drivers are utilized for the word lines, and SN75308 transistor arrays are used for the bit drivers. The source and sink drivers are selected by the address decode, and S_1 and S_2 are used as strobes for timing the source and sink switches. Although generally used in small memory systems, 2D memories are widely applied in fast scratchpad-type applications.

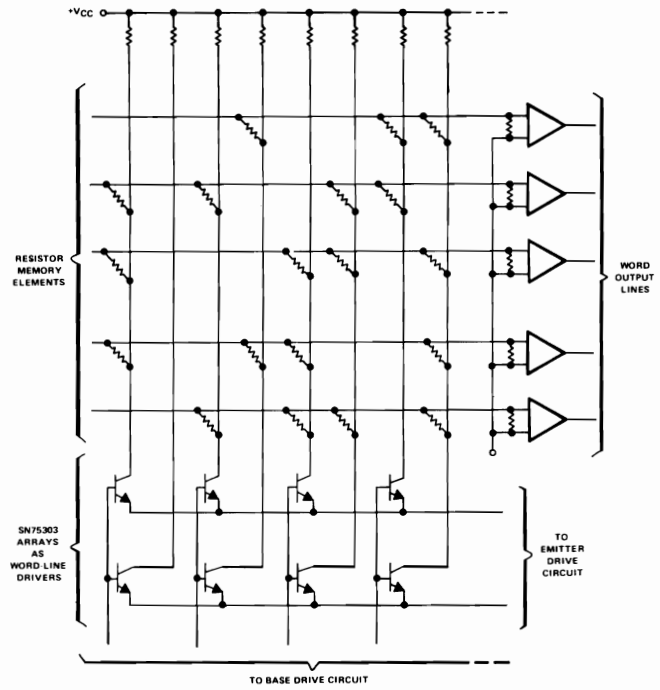


Figure 9.35. SN75303 as Word-Line Driver for Resistive Read-Only Memory

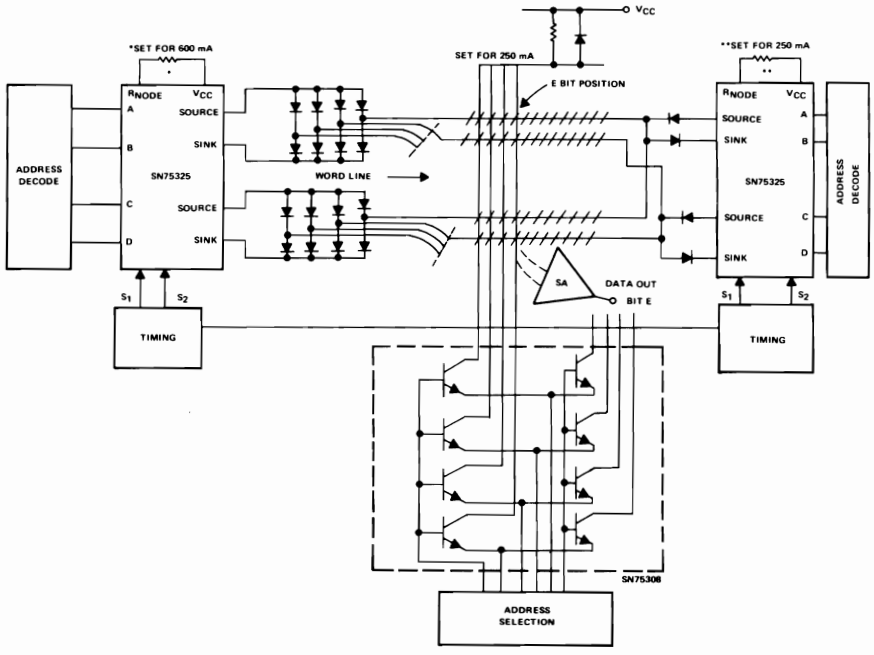


Figure 9.36. 2D Memory Application

In larger 2-1/2D and 3D memories the versatility of the SN75324 circuit allows simple addressing methods to be employed. In Figure 9.37 we see the combinations of input circuitry and output steering diodes used in addressing a matrix of X and Y lines. Hex buffers and hex inverter buffers with open collector outputs are utilized to provide adequate logic 1 levels to the SN75324 address inputs. SN7416 and SN7417 buffers are typical of those used in this application. For the X line and Y line inputs an SN75361A is used. It easily provides the 24-milliamp output capability required for supplying logic 0 levels to two SN75324 timing inputs. Figure 9.38 shows in more detail the typical output connections, and use of 1N5775 steering diodes. This example is a 256-bit system for a 2-1/2D memory application.

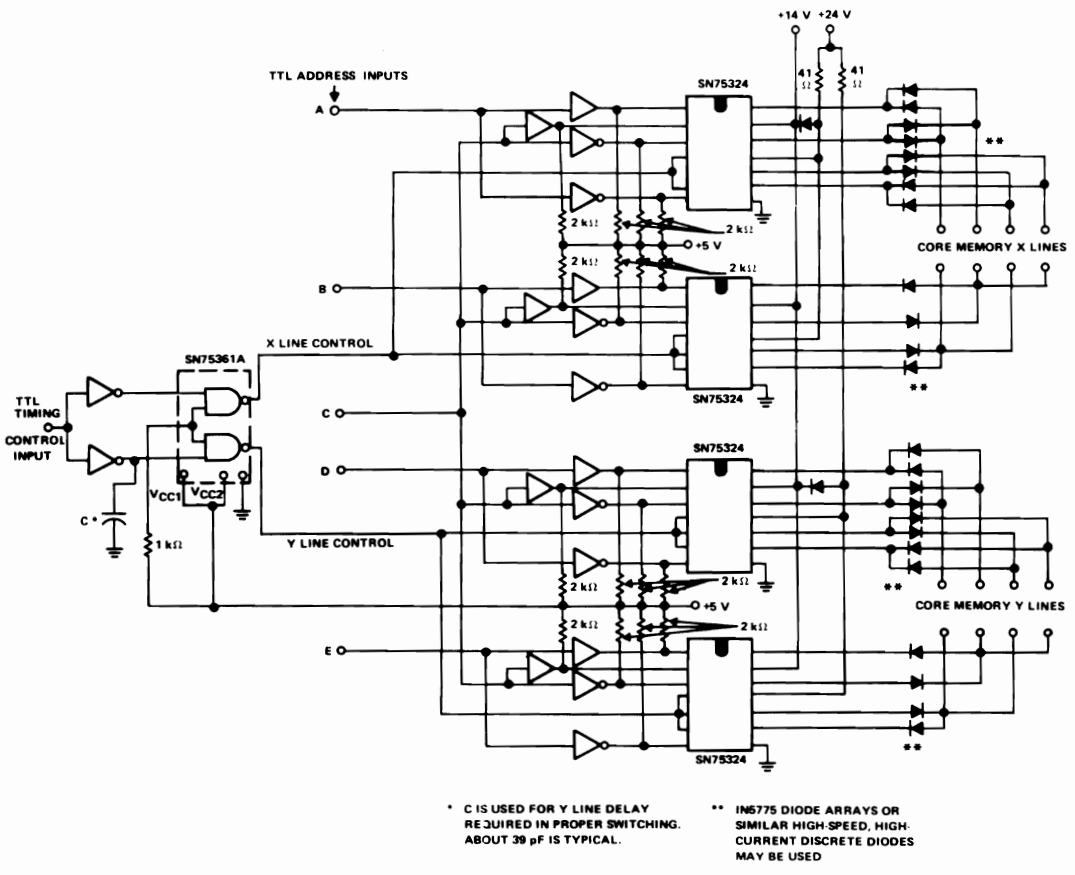


Figure 9.37. X and Y Line Drivers and Address Circuitry

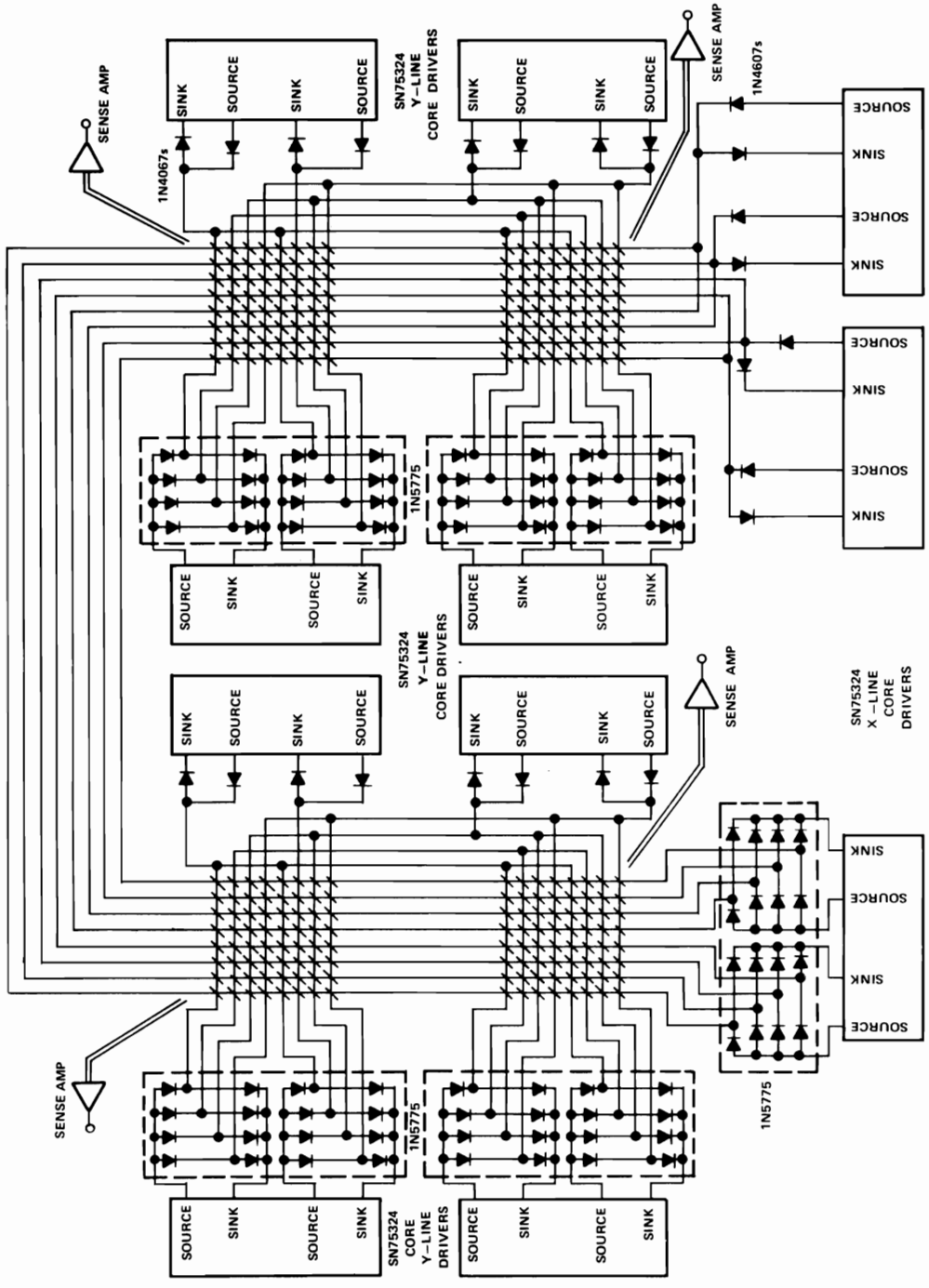


Figure 9.38. 256-Bit 2 1/2D Memory

The SN75325 is recommended for higher-speed systems requiring up to 600 mA of drive. Figure 9.39 shows a typical application that might be utilized with 2-1/2D or 3D systems. The 1N5775 steering diodes are employed because of their speed and current-handling ability. The SN74154 1 to 16 decoders used are capable of handling much larger matrixes and are recommended for simplifying large, complex systems. Mode selection and timing strobe circuits are implemented with high-speed SN74H00 gates, their speed and output capabilities making them well suited for this application.

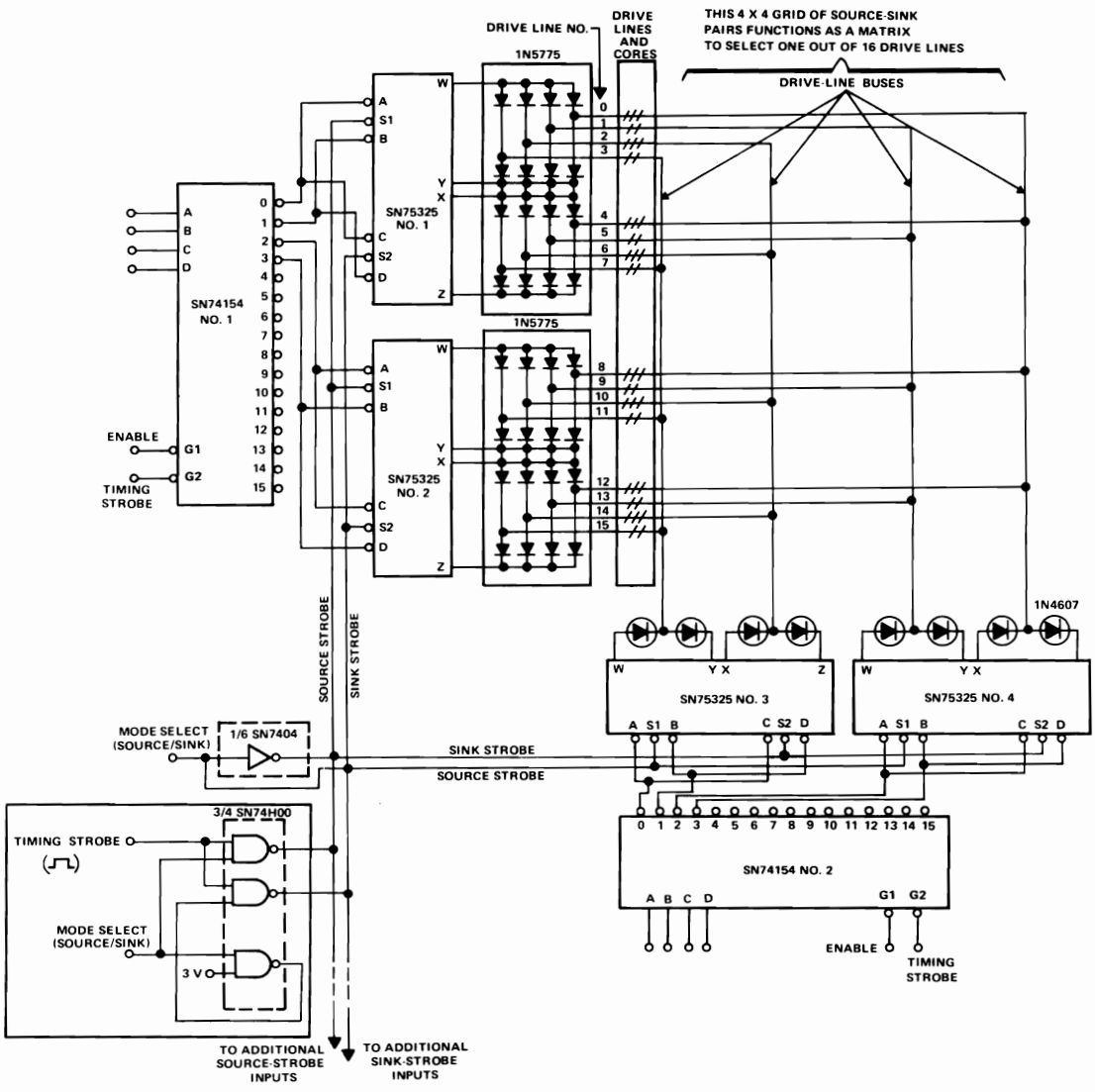


Figure 9.39. Typical Drive for 2 1/2D or 3D Memory

In some large system applications it is desirable to have four source drivers in one package and four sink drivers in another. This improves the PC board layout in some cases. Figure 9.40 shows a typical application using SN75326 quad sinks and SN75327 quad sources. This simple arrangement provides the addressing drive for a 256-bit matrix using four SN75326 units and four SN75327 units. The loads could be core memory, lamps, or relays, as the drive capability is sufficient for many situations.

There are special core memory applications where power dissipation, stability, and package size are major considerations. Military aircraft and space vehicles are two examples where this is true. As previously mentioned, the SN55329 was developed specifically for these types of applications. For this device V_{CC1} and V_{CC2} power supplies are nominally +5 volts and +12 volts respectively. $TCV_{(source)} = 4.7\ V_{dc} + V_{CC1}$ and $TCV_{(sink)} = 1.84\ V_{dc}$. With temperature-controlled voltages for the primary source and sink supplies, proper drive levels can be maintained over the full device-temperature range of −55°C to +110°C.

Because of the characteristics of ferrite cores they require higher read or write currents for switching at lower temperatures. The purpose of a temperature-controlled voltage source or sink is to provide the voltage that results in a correct current level for the operating temperature. At any particular temperature source and sink currents must be maintained accurately.

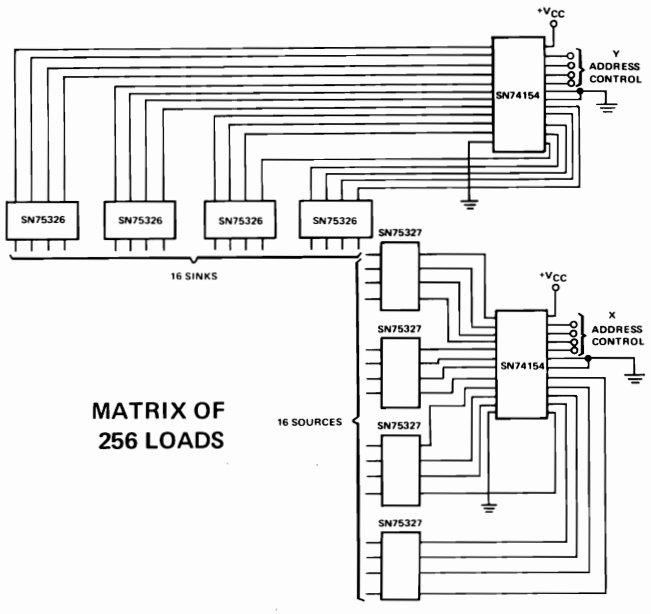


Figure 9.40. SN75326 and SN75327 Matrix Drivers

Tables 9.3 and 9.4 show typical current ranges versus temperature and their stability with variations in V_{CC1} or V_{CC2} supply levels. Current accuracy and stability over a wide range of operating conditions are vital for competent performance.

Table 9.3. Source Current Regulation (SN55329)

Case Temperature (°C)	TCV (Source)	Selected Output Voltage	V_{CC_1}	V_{CC_2}	$I_{(SOURCE)}$ mA_{dc}
+110	4.13	V_{CC_1} + 0.67 V_{dc}	4.75	12.36	−220±5%
			5.15	11.40	−220±5%
Room	4.70	V_{CC_1} + 0.62 V_{dc}	4.75	12.36	−270±5%
			5.15	11.40	−270±5%
−55	5.28	V_{CC_1} + 0.50 V_{dc}	4.75	12.36	−320±5%
			5.15	11.40	−320±5%

Note: All voltages V_{dc}

TCV (source) is referenced to V_{CC1} (pin 8)

V_{TT} (pin 24) is connected to pin 8

Table 9.4. Sink Current Regulation (SN55329)

Case Temperature (°C)	TCV(sink)	Selected Output Voltage	V_{CC_1}	V_{CC_2}	$I_{(sink)}$ mA_{dc}
+110	1.48	V_{CC_1} − 0.67 V_{dc}	5.15	12.36	+220±5%
			4.75	11.40	+220±5%
Room	1.84	V_{CC_1} − 0.62 V_{dc}	5.15	12.36	+270±5%
			4.75	11.40	+270±5%
−55	2.24	V_{CC_1} − 0.50 V_{dc}	5.15	12.36	+320±5%
			4.75	11.40	+320±5%

Note: All voltages V_{dc}

V_{TT} (pin 24) is connected to pin 8

Maximum supply currents at worst-case temperature conditions are given in Table 9.5. The advantage of low standby current and resulting low power dissipation is evident when standby and operating current levels are compared.

Although tested for 1-MHz operation (see Figure 9.33), typical application of the timing of circuit signals could be as follows: Referring to Table 9.6, at t = 0 the power enable is activated. In this typical application each succeeding function adds a delay so slight that a total cycle time of 503 nanoseconds may be possible.

Table 9.5. Power-Supply Currents Over Operating Case Temperature Range

PARAMETER	MAXIMUM	UNIT
$I_{V_{CC1}}$ Standby	1.0	mAdc
$I_{V_{CC2}}$ Standby	3.0	mAdc
I_{OUTPUT} Leakage	250	μAdc
$I_{V_{CC1}}$ Operate	50	mAdc
$I_{V_{CC2}}$ Operate	50	mAdc
$I_{TCV(Sink)}$ Operate	12	mAdc

Table 9.6. Timing of Circuit Signals: Typical Application

FUNCTION	INCREMENTAL TIME (ns)	TOTAL TIME (ns)
PE1 ON	0	0
PE2 ON	30	30
Strobe ON	40	70
Strobe Time	130	200
Source ON Included in Strobe Time	0	200
Source OFF	60	260
Source-Sink Strobe Cycle OFF-ON	60	320
Strobe Time	130	450
Sink ON Included in Strobe Time	0	450
Sink OFF	53	503

Figure 9.41 shows package outline and pin-out for the 24-lead hermetic metallized-ceramic flat package. Its very small size and convenient heat sinking ability make this type of package desirable in high-reliability military-type systems.

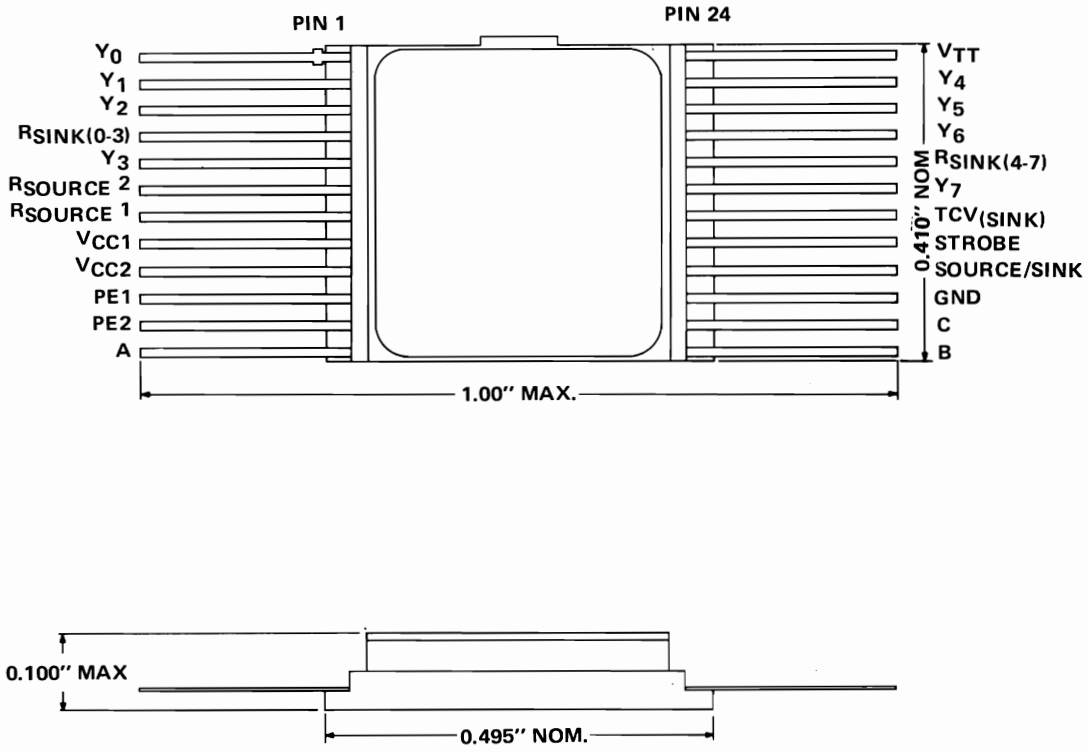


Figure 9.41. SN55329 Package Outline and Pin-Out

Because of compact packaging and complexity of the SN55329 it is possible to drive a 16 x 16 line matrix using only four packages, as shown in Figure 9.42. This 256-bit memory drive system requires only about 120 mW of standby power.

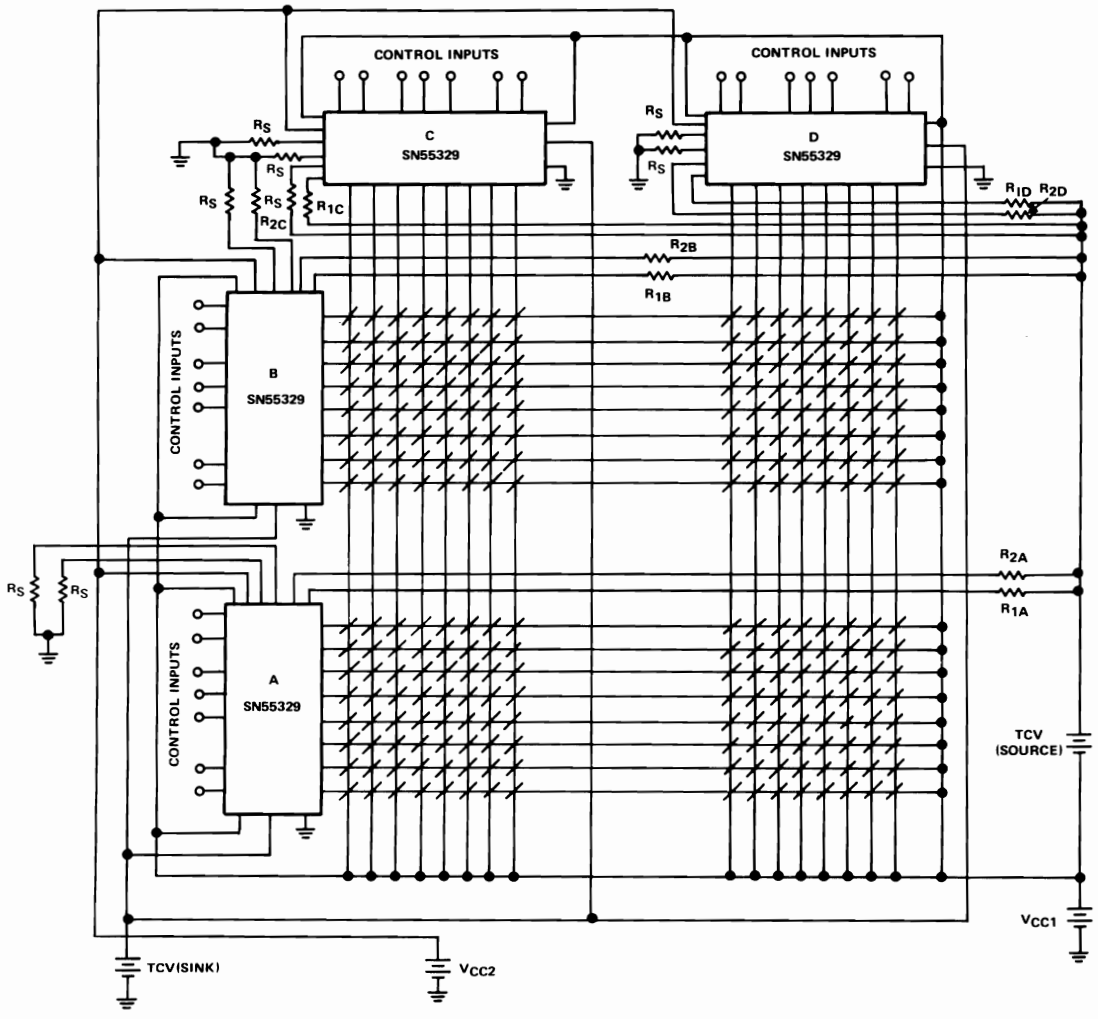


Figure 9.42. SN55329 Drive System for 256-Bit Memory

9.3 SENSE AMPLIFIERS

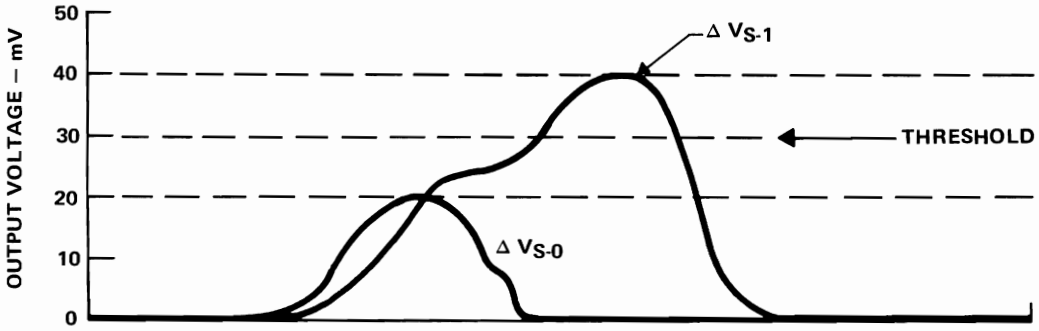
9.3.1 General Characteristics

Sense amplifiers form the other half of the core-memory interface. Core-memory sense amplifiers have particular requirements that make them uniquely different from most basic comparators.

As shown in Figure 9.5, the sense-line output signal may be a positive or negative pulse, and the logic level (1 or 0) is determined by the absolute value of its amplitude. Thus, the sense amplifier must respond to amplitude levels above a set threshold, regardless of polarity. Logic 1 levels range from 3 to 40 mV, depending on the core size and speed requirements.

Considering that the sensed logic 0 level may be 50% of the logic 1 level in the same system, the sense amplifier threshold and input sensitivity must be exceptional. For example (Figure 9.43), if the peak 1 level is 40 mV and the 0 level 20 mV, and a sense threshold level of 30 mV is set, even a threshold variation of ± 10 mV would be marginal. Under these conditions a threshold accuracy of ±7 mV would be desired. For lower-level signals more accuracy is required. Some very-high-speed memory systems may require ±3 mV maximum threshold variation.

The SN7520 series devices have been developed to meet the required input conditions and provide TTL logic outputs. Their threshold stability over temperature and power-supply variations makes them extremely useful to the design engineer working with memory systems.



NOTE 1. ΔV_{S-0} is the sense-line output voltage when a core in the logic 0 state is read.

2. ΔV_{S-1} is the sense-line output voltage when a core in the logic 1 state is read.

Figure 9.43. Typical Sense Line Output Voltage Waveforms

9.3.2 Basic Internal Characteristics and Operation

Series 7520 sense amplifiers are completely dc coupled. Previous designs had created circuits in which the threshold level could not be closely controlled because of extreme sensitivity to changes in dc levels throughout the amplifier, primarily caused by tolerances on the absolute value of resistors and resistor temperature coefficients. But the "matched-amplifier" design of Series 7520 circuits depends on resistor ratios rather than absolute values, and excellent stability of the threshold level can be maintained despite component variations and changes in bias levels. The capability of multiple-input amplifiers further increases the versatility of the design.

The basic circuit is used to implement several sense-amplifier designs. Additional logic circuitry added to the strobe-gate output provides versatile sensing functions. The outputs of two or more input amplifiers can be combined to implement multiple-input amplifiers, a function not previously available in integrated form. The dc-coupled design eliminates many of the problems associated with the overload recovery time and threshold shift with input repetition rate usually encountered in sense-amplifier designs that use reactive coupling components.

The basic Series 7520 threshold and strobe circuit (see Figure 9.44) uses a matched-amplifier concept, the theory being that identical amplifiers exhibit

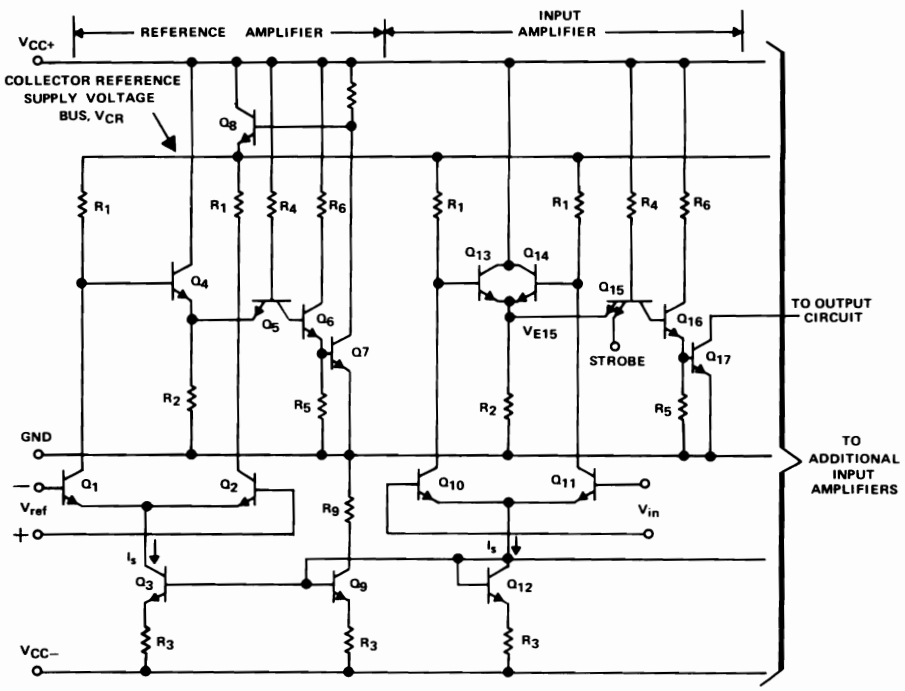


Figure 9.44. Basic Series 7520 Circuit

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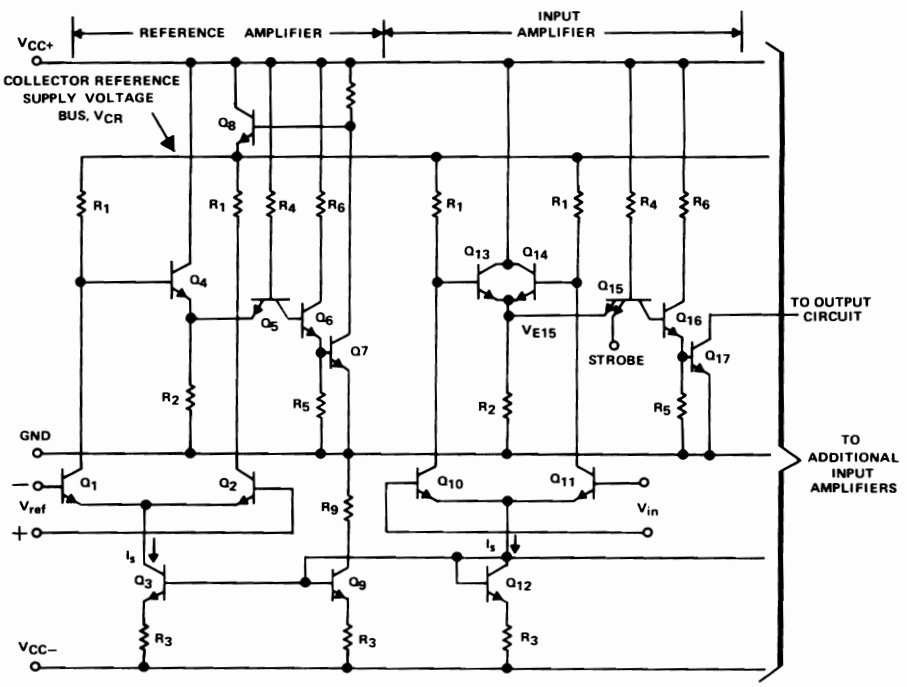


Figure 9.44. Basic Series 7520 Circuit

identical characteristics when operated under identical conditions. The concept is especially applicable to integrated-circuit fabrication techniques, since this process yields components with excellent thermal and electrical matching and tracking characteristics.

The circuit of Figure 9.44 includes a reference amplifier and an input amplifier, the reference amplifier being used to establish the input threshold voltage of the input amplifier. There is 1:1 correspondence between the applied reference voltage, V_{ref}, and the nominal differential-input threshold voltage level, V_T. Operation is as follows:

The collector reference voltage is controlled by the reference input voltage. The second stage of the reference amplifier, composed of Q_7, Q_6, and Q_5, has around it a feedback loop which keeps the second stage biased in the linear range for all reference input voltages of interest. The collector reference voltage and the reference input voltage may be related by:

$$V_{CR} = V_{BE7} + V_{BE6} - V_{offset\ 5} + I_s R_1 \left(\frac{1}{1 + e^{V_{ref}/26}} \right) + V_{BE4} \qquad (1)$$

The input amplifier is identical to the reference amplifier except that:

1) Its second stage does not have feedback
2) An additional emitter-follower transistor at the output of the first stage provides rectification of the input signal and therefore bipolar threshold action.

The second stage of the input amplifier (and the reference amplifier also) is a transistor-transistor logic (TTL) gate configuration with an input logic threshold voltage level of approximately 2 V_{BE}, as shown in Figure 9.45 by its voltage transfer plot. The gate has a high voltage gain as indicated by the steep transition region. The gate input threshold voltage level, V_{E15}, can be written as:

$$V_{E15} = V_{BE17} + V_{BE16} - V_{offset\ 15} \qquad (2)$$

The range of values of V_{E15} that keep the gate output in the transition region is very narrow because of the high voltage gain of the gate. The input-voltage amplitude (V_{in}) required to force the gate output to the logic threshold voltage level is, by definition, the differential-input threshold voltage level, V_T. For this condition the gate input must be at the logic threshold level as defined by Equation (2). For any value of V_{in} the voltage at V_{E15} may be defined by the following equation:

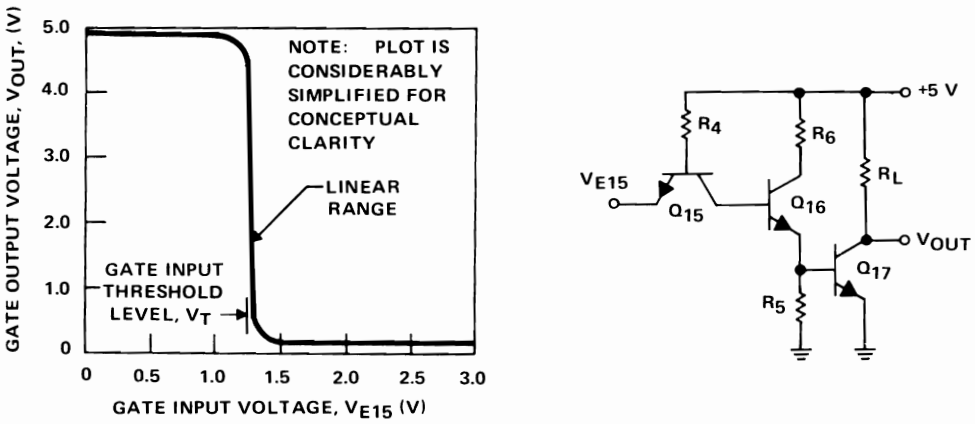


Figure 9.45. TTL Gate Voltage Transfer Plot

$$V_{E15} = V_{CR} - I_S R_1 \left(\frac{1}{1 + e^{V_{in}/26}} \right) - (V_{BE13} \text{ or } V_{BE14}) \tag{3}$$

When $V_{in} = V_T$, Equations (2) and (3) may be equated to determine V_{CR}. Substituting V_{CR} into Equation (1) results in:

$$V_{BE7} + V_{BE6} - V_{offset\ 5} + V_{BE4} + I_S R_1 \left(\frac{1}{1 + e^{V_{ref}/26}} \right)$$

$$= V_{BE17} + V_{BE16} - V_{offset\ 15} + (V_{BE13} \text{ or } V_{BE14})$$

$$+ I_S R_1 \left(\frac{1}{1 + e^{V_{in}/26}} \right) \tag{4}$$

For integrated circuits the parameters of similar transistors can be assumed to be matched, and therefore Equation (4) can be reduced to

$$V_{in} = V_{ref} \tag{5}$$

Since Equation (4) was assumed to define the condition at which the output of the TTL gate is at the logic threshold level, the value of V_{in} is equal to V_T, or $V_{in} = V_T = V_{ref}$. Therefore the threshold level is equal to the applied reference voltage, V_{ref}.

Because of the high overall gain of the input amplifier, only a small change in the input voltage amplitude is required to switch the gate output from one logic level to another. An inspection of Equation (3) for a given reference voltage shows that for the stated conditions the following results are obtained:

a) $V_{in} < V_{ref}$: gate output is in the cutoff region
b) $V_{in} = V_{ref}$: gate output is in the linear region
c) $V_{in} > V_{ref}$: gate output is in the saturated region

Note that power supplies do not enter into the equations. Changes in power-supply levels introduce similar changes in the reference and input amplifiers. If the similar components in the amplifiers are matched, these changes do not cause changes in the input threshold level. For instance, a change in the negative supply voltage, V_{CC-}, changes the magnitude of the current in the current source of the reference amplifier, causing a change in the amplitude of the collector reference voltage V_{CR}, as defined by Equation (1). However, a similar change is introduced in the current source of the input amplifier. Equation (4) shows that, so long as the currents are matched, they cancel and the threshold remains approximately equal to the reference voltage, V_{ref}.

Similarly, changes in the input amplifier characteristics due to temperature are compensated by similar changes in the reference amplifier. For instance, the TTL gate threshold voltage level, V_{E15}, is about twice as sensitive to temperature as V_{BE}, or -3.6 mV/°C. However, a similar stage in the reference amplifier has an identical variation due to temperature that compensates for this change.

For integrated circuits, excellent matching of components can be assumed. The foregoing analysis has assumed that resistors are matched, the transistor parameters are matched, and that transistor current gains are so high that base currents can be neglected. Also, the tracking of parameters with temperature and current level has been assumed to be ideal.

In practical application, some mismatch of components must necessarily be tolerated, even in integrated circuits. The major cause of error in the threshold (V_T) and reference (V_{ref}) levels is the product of normal differential-input offset voltage and gain of the input amplifiers. However, with proper design of the circuit and the bar layout, reasonable matching can be accomplished.

The reference amplifier can be used to supply the collector reference voltage simultaneously to more than one input amplifier. This allows simultaneous adjustment of the input threshold voltage level of several input amplifiers. Transistor Q_8 provides adequate output drive capability for the reference amplifier.

A strobe input is included in the input amplifier for adding a second input emitter to the input transistor (Q_{15}) of the TTL gate second stage. The amplified input

signal and the strobe input signal must be simultaneously above the TTL gate input threshold level ($2\ V_{BE}$) before the gate output will saturate. Implementing the strobe function at this point has several advantages:

1) The logic threshold level of the strobe is compatible with TTL or DTL (diode-transistor logic) levels.

2) The strobe input, when low, prevents normal overload signals at the sense input from saturating the threshold level detector (TTL gate) and causing excessive detector recovery time.

3) The delay times from the strobe input to the gate output and from the sense input to the gate output are very well defined, allowing precise strobe positioning.

4) The strobe input does not load the output of the sense input preamplifier (input stage).

The input (or sense) amplifier can therefore be strobed directly from standard saturated TTL or DTL gates. The second stage of the reference amplifier is not strobed. Transistor Q_5 is included to carry through the matched-amplifier concept. In a design with more than one input amplifier, each may be strobed independently or they may be strobed in parallel.

9.3.3 Device Descriptions

Table 9.7 is a listing of many of the sense-amplifier types available from Texas Instruments. The basic function, device number, temperature range, and package designations are listed. This list of device types reflects the variations in applications required by a large number of core-memory manufacturers. In addition to specific design characteristics, each device features:

Dual-channel capability
High speed (typically $>$ 20 MHz)
Fast recovery times (typically $<$ 20 ns)
Time and amplitude signal discrimination
Adjustable input threshold voltage levels
Narrow region of threshold uncertainty (typically $<$ 1 mV)
High dc noise margin (typically 1 volt)
TTL or DTL output-drive capability
Standard logic-supply voltages (± 5 volts)

Table 9.7. Series 7520 Sense Amplifiers

FUNCTION	OPERATING TEMPERATURE RANGE		PACKAGE TYPES
	−55°C to 125°C	0°C to 70°C	
Dual-Channel, Open-Collector Output	SN5522	SN7522	J, JA J, N
	SN5523	SN7523	J, JA J, N
Dual-Channel, Complementary Outputs	SN5520	SN7520	J, JA J, N
	SN5521	SN7521	J, JA J, N
Dual-Channel with Output Register		SN7526	J, N
		SN7527	J, N
Dual (Separate Outputs)	SN5524	SN7524	J, JA J, N
	SN5525	SN7525	J, JA J, N
	SN55234	SN75234	J, JA J, N
	SN55235	SN75235	J, JA J, N
Dual with Open-Collector Outputs	SN55232	SN75232	J, JA J, N
	SN55233	SN75233	J, JA J, N
Dual with Test Points	SN5528	SN7528	J, JA J, N
	SN5529	SN7529	J, JA J, N
	SN55238	SN75238	J, JA J, N
	SN55239	SN75239	J, JA J, N
Dual with Data Register and Buffer Outputs	SN55236	SN75236	SB SB
	SN55237	SN75237	SB SB

SN7520, SN7521 Sense Amplifiers — Figure 9.46 shows the functional block diagram of the SN7520 and SN7521 sense amplifiers, devices featuring dual sense-input preamplifiers with independent strobing of each sense channel. The outputs of the two sense channels are combined in a common output circuit composed of two cascaded TTL gates, providing complementary output logic levels compatible with standard TTL digital circuits. Each gate has an external gate input allowing additional output versatility. The output gates may be used as part of the logic circuitry, interconnected to form a latch function with an external clear input, or capacitively interconnected for output pulse stretching.

A single reference input voltage is used to adjust the input threshold voltage levels of the two sense input channels simultaneously, allowing the sense amplifier threshold to be tailored to the individual memory application for optimum performance.

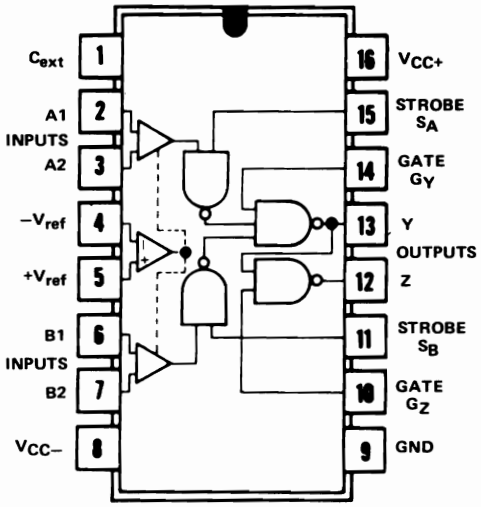


Figure 9.46. SN7520, SN7521 Functional Diagram and Pin-Out

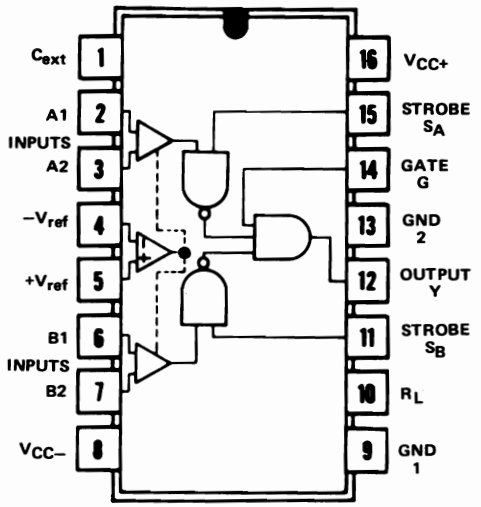


Figure 9.47. SN7522, SN7523 Functional Diagram and Pin-Out

The SN7520 and SN7521 are fabricated in the 16-pin plastic or ceramic dual-in-line packages, with pin breakout as shown in Figure 9.46. Electrical characteristics of the SN7520 and SN7521 and other products described here are included in the appropriate data sheets. A schematic of each circuit type is also shown in the data sheets.

SN7522, SN7523 Sense Amplifiers – The functional block diagram of the SN7522 and SN7523, which also feature dual sense-input preamplifiers with independent strobing of each sense channel, is shown in Figure 9.47. The outputs of the two sense channels are combined in a double-inverting, open-collector output gate. This output may be connected in the familiar wire-AND configuration with other SN7522/23s, SN7520/21s, or logic gates with the wire-AND capability, such as most diode-transistor logic (DTL) gates and the SN7401 TTL gate. This wire-AND capability permits implementation of a level of logic without additional gate delays. An internal load resistor is included in the SN7522 and SN7523 for use as a collector pull-up in applications where it is necessary; connection from the resistor to the output collector is made externally. A single reference input voltage simultaneously adjusts the threshold voltage levels of both sense input channels. These sense amplifiers may be used with the SN7520 and SN7521 for increased versatility.

The SN7522 and SN7523 are fabricated in the 16-pin plastic or ceramic dual-in-line packages with the pin breakout as seen in Figure 9.47.

SN7524, SN7525 Sense Amplifiers — The SN7524 and SN7525 functional block diagram is seen in Figure 9.48. Unlike the SN7520/21 and SN7522/23 sense amplifiers, the SN7524 and SN7525 consist of two separate single-preamplifier sense amplifiers. Because of its basic design and speed it is one of the more popular devices in use today.

Each sense input channel can be independently strobed. The output circuit of each channel features a simple TTL gate configuration with high fan-out capability. The SN7524 and SN7525 are designed primarily for small memory applications where performance and cost are important considerations.

A single reference input voltage simultaneously adjusts the threshold levels of the two sense-input channels. The SN7524 and SN7525 are fabricated in the 16-pin dual-in-line packages with pin breakout as shown in Figure 9.48.

SN7526, SN7527 Sense Amplifiers — The SN7526 and SN7527 functional block diagram is seen in Figure 9.49. This circuit is a dual-channel sense amplifier with the preamplifiers connected to a D-type flip-flop with external clear and preset inputs. A delay between the strobe input terminals and the clock input of the flip-flop ensures that data is set up at the D input of the flip-flop prior to clocking. Each channel may be independently strobed. The 16-pin dual-in-line package pin breakout for the SN7526 and SN7527 is shown in Figure 9.49.

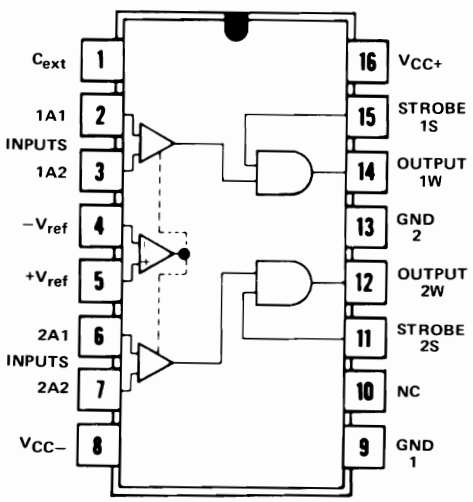


Figure 9.48. SN7524, SN7525 Functional Diagram and Pin-Out

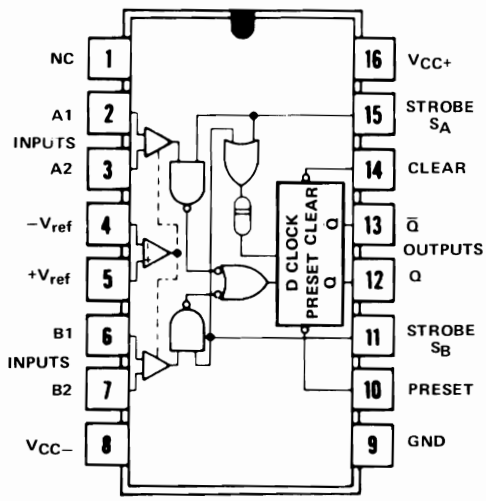


Figure 9.49. SN7526, SN7527 Functional Diagram and Pin-Out

SN7528, SN7529 Sense Amplifiers — The terminal designations and block diagram for these devices are depicted in Figure 9.50. This circuit features two separate single-preamplifier sense amplifiers in a single package. The output of each preamplifier is available as a test point which can be used to observe the amplified core signal to facilitate accurate strobe timing. When utilizing this device, care should be taken not to couple the strobe signal or other stray signals to the test point; also avoid excessive loading of the test point. Either coupling or loading would produce a change in the threshold voltage of the device. The output circuit of each channel features a simple TTL gate configuration which has high fan-out capability.

SN75232, SN75233 Sense Amplifiers – Figure 9.51 shows the block diagram and terminal designations of the SN75232 and SN75233 circuits, similar to the SN7524 and SN7525 but having several additional features. They are internally compensated, and output gates have open collector outputs, permitting two or more gate outputs to be connected in the wire-AND configuration.

The incorporation of inverting rather than non-inverting output gates in these devices eliminates the need for external inverters in most system applications. The SN75232 and SN75233 sense amplifiers are available in the 16-pin J and N dual-in-line packages.

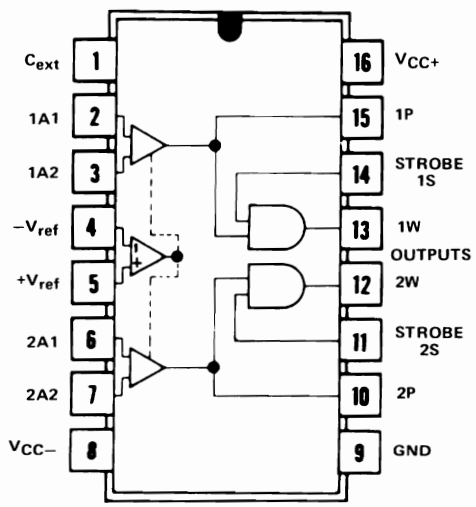


Figure 9.50. SN7528, SN7529 Functional Diagram and Pin-Out

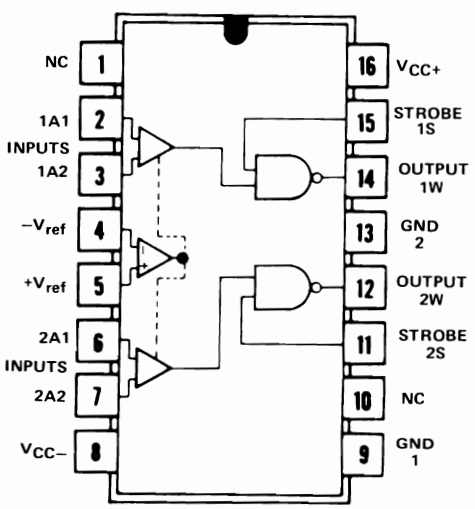


Figure 9.51. SN75232, SN75233 Functional Diagram and Pin-Out

SN75234, SN75235 Sense Amplifiers — Figure 9.52 shows the basic block diagram and terminal designations for these devices. The basic function is the same as that of the SN7524 and SN7525, with two important exceptions: (1) It does not require an external capacitor, being internally compensated; (2) the output gates are inverting (NAND) gates, eliminating need for an external inverter in most system applications.

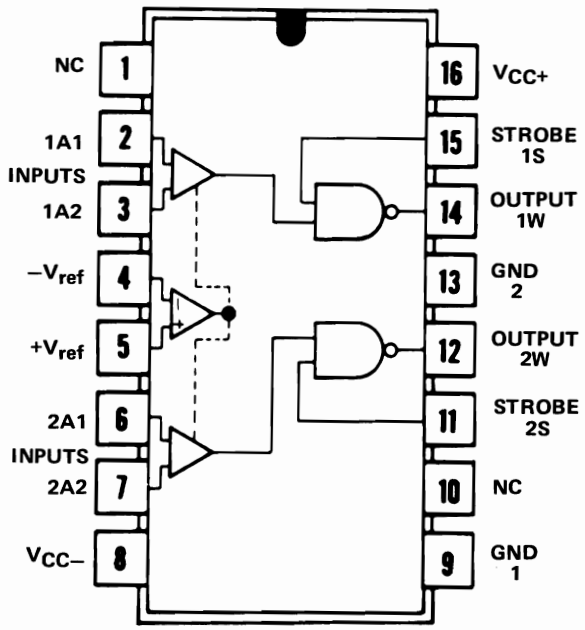


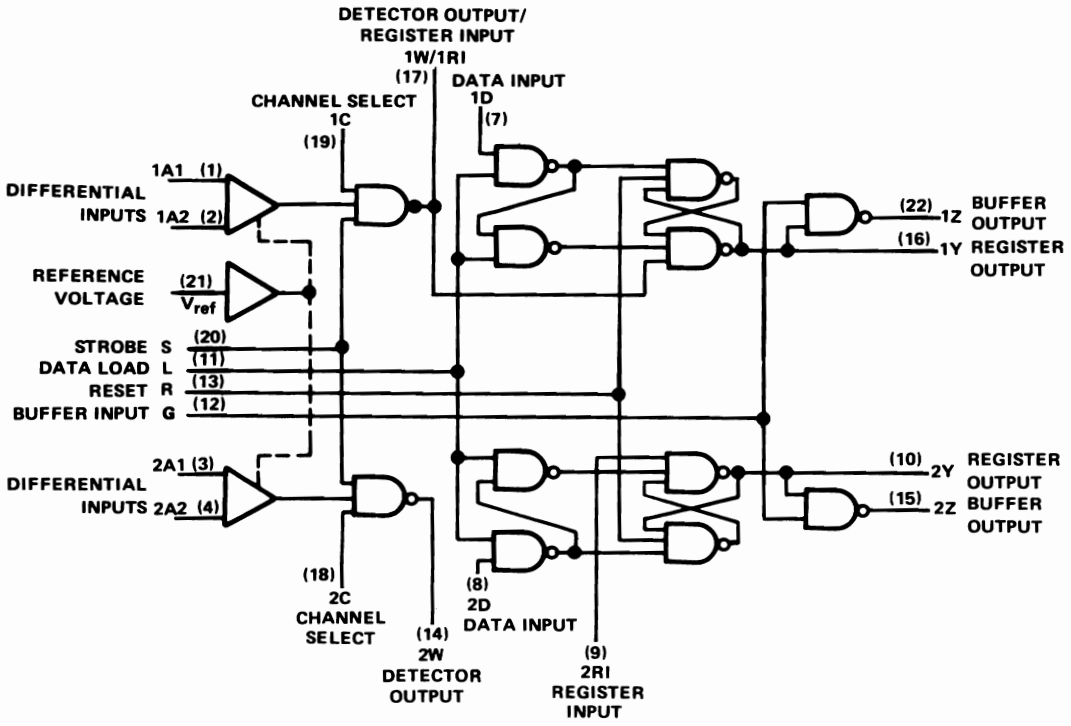
Figure 9.52. SN75234, SN75235 Functional Diagram and Pin-Out

SN75236, SN75237 Sense Amplifiers — Figure 9.53a depicts the block diagram for these devices. Originally designed as the SN55236 for military-type applications, it features a number of characteristics not found in most sense amplifiers. These are:

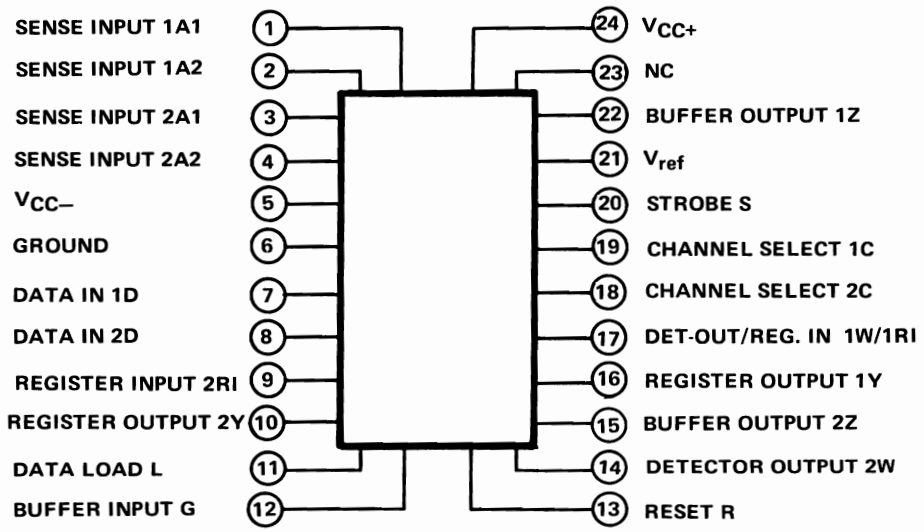
Typical ±2 mV threshold sensitivity	Internally compensated
Low power consumption	Dual data resistors
Internal reference attenuator	Ability to insert external data
TTL-compatible inputs and outputs	Buffer outputs available

These and other features make these devices desirable for complex but compact memory systems requiring low power and versatile output capability.

Figure 9.53b shows the 24-pin flat-package pin breakout.



(a)



(b)

Figure 9.53. SN75236, SN75237 Functional Diagram and Pin-Out

SN75238, SN75239 Sense Amplifiers — Block diagram of the SN75238 and SN75239 sense amplifiers is seen in Figure 9.54. The basic function of these devices is the same as that of the SN7528 and SN7529, but has the following additional features:

No external compensation is required.

It has inverting (NAND) output gates.

Figure 9.54 also shows the pin breakout and package configuration for these devices.

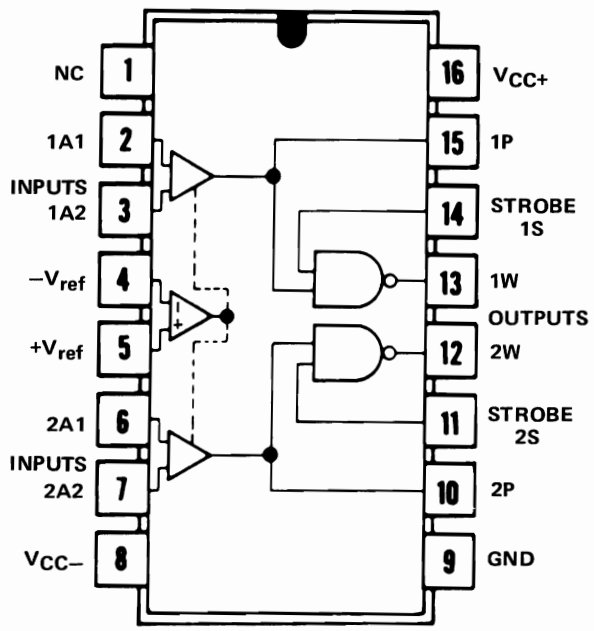


Figure 9.54. SN75238, SN75239 Functional Diagram and Pin-Out

9.3.4 Response and Stability Characteristics

Differential-Input Threshold Voltage Level Considerations — The differential-input threshold voltage level, V_T, of Series 7520 sense amplifiers is the voltage level required to force the logic output to the logic threshold level, for a given applied reference voltage. The nominal threshold voltage level is designed to be the same as the applied reference voltage as indicated in Figure 9.55. Typical voltage transfer plots (differential-input-to-logic-output) of these devices are shown in Figures 9.56 and 9.57.

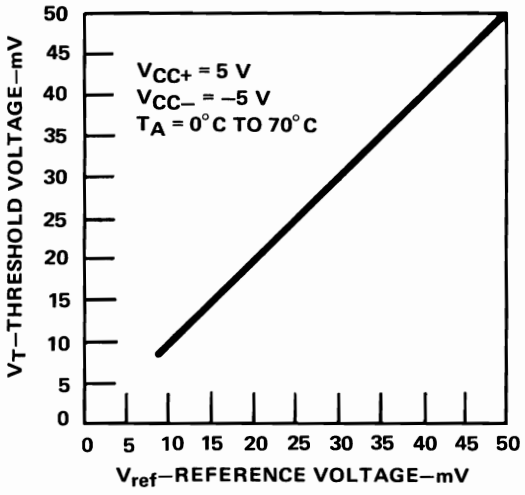


Figure 9.55. Threshold Voltage vs. Reference Voltage

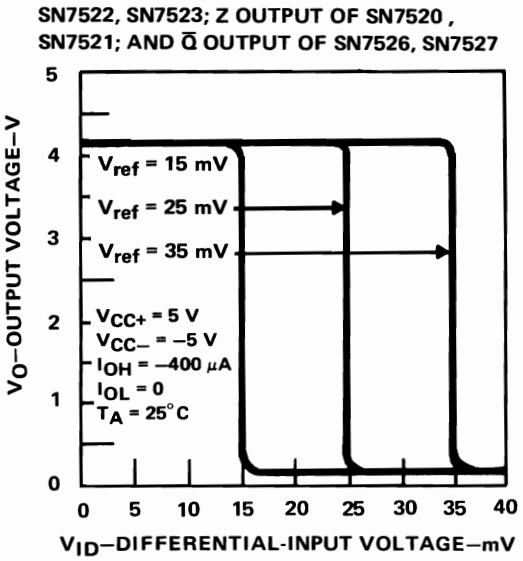


Figure 9.56. Typical Voltage Transfer Plot

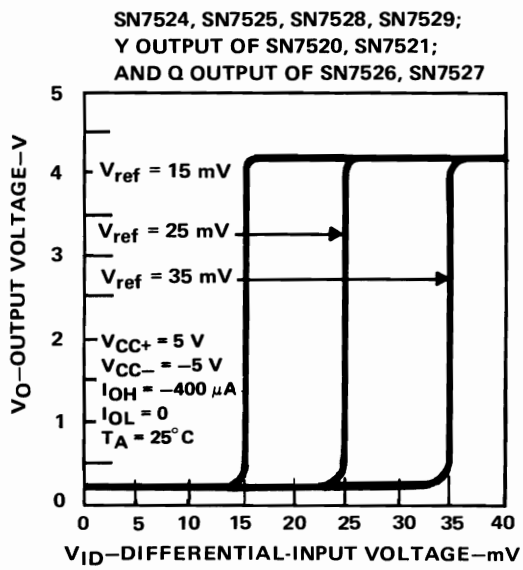


Figure 9.57. Typical Voltage Transfer Plot

Several factors influence the actual threshold voltage level for a given preamplifier, these factors including supply voltage, temperature, normal differential-input offset voltages, etc. Data-sheet specifications of threshold level for Series 7520 devices are designed to be useful over the normal range of memory output signals. Threshold level limits are imposed at reference voltage levels of 15 mV and 40 mV. Although limits are guaranteed only at reference voltages of 15 and 40 mV, the same reference/threshold correspondence can be assumed for reference voltage levels between approximately 10 and 60 mV for the majority of these devices. The slanted lines in Figures 9.58 and 9.59 indicate these assumed limits for the devices.

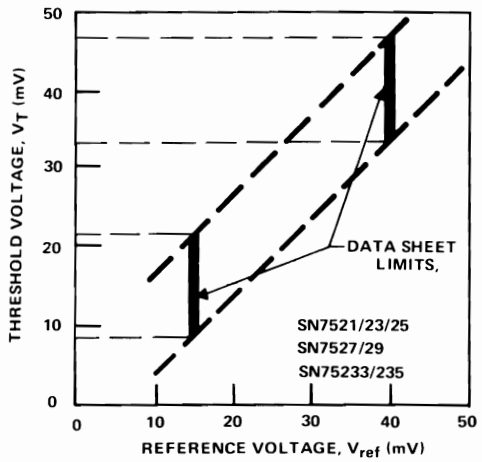


Figure 9.58. Threshold Voltage Limits vs. Reference Voltage

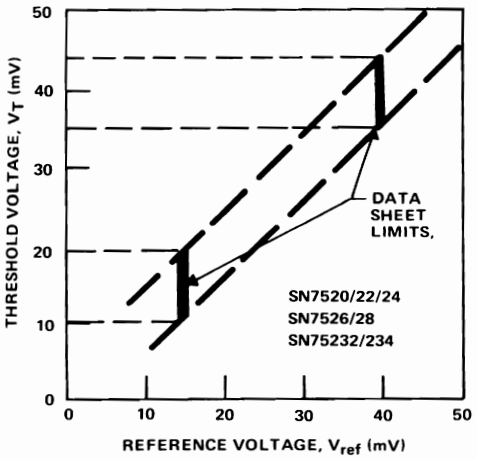


Figure 9.59. Threshold Voltage Limits vs. Reference Voltage

As indicated by these figures and data-sheet specifications, threshold/reference correspondence is $V_T = V_{ref} \pm 4$ mV for $V_{ref} = 15$ or 40 mV for the even-numbered devices; $V_T = V_{ref} \pm 7$ mV for $V_{ref} = 15$ or 40 mV for the devices which have odd numbers.

The tightest limits are imposed on the prime devices (even numbers), while loser limits have been applied to the remaining units. The two exceptions to these conditions are of course the SN75236/237, both of which are specified for higher performance.

The change in the threshold voltage level with variations in power supplies is an important consideration in sense-amplifier designs. The matched-amplifier Series 7520 design concept results in a circuit extremely tolerant of change in power-supply levels. Typical change in the threshold level for reference voltages of 15 and 40 mV and up to ±10% variations in power supplies is shown in Figure 9.60.

Although Series 7520 devices are specified for use with power-supply levels from ±4.75 to ±5.25 V for compatibility with Series 74 digital (TTL) circuits, they are usable over a wider range of supply levels.

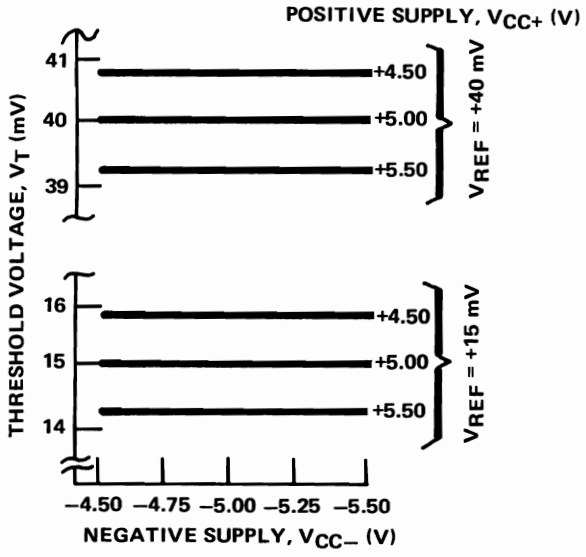


Figure 9.60. Threshold Voltage as a Function of Supply Voltages

Another important consideration is the drift in the threshold level with temperature. The typical Series 7520 device exhibits less than 15 μV variation in the threshold level for each Celsius degree change in ambient temperature, this being primarily because of normal differential-input offset voltage drifts in the reference and input preamplifiers. This low drift results in an almost flat threshold level over the specified temperature range of 0 to +70°C. Where a temperature coefficient is desirable in a particular memory design (perhaps for use with uncompensated cores) a simple reference voltage circuit can usually be designed to introduce the proper temperature coefficient.

Most sense-amplifier designs, either integrated or conventional, use reactive coupling to eliminate threshold-drift problems caused by bias level drift. However, reactive coupling is invariably accompanied by threshold level shift with frequency and excessive overload recovery time. Series 7520 devices use an all dc-coupled circuit approach in which the drift in bias levels is compensated by the matched reference and input amplifiers. The resultant circuit has excellent threshold frequency response, as shown in Figure 9.61.

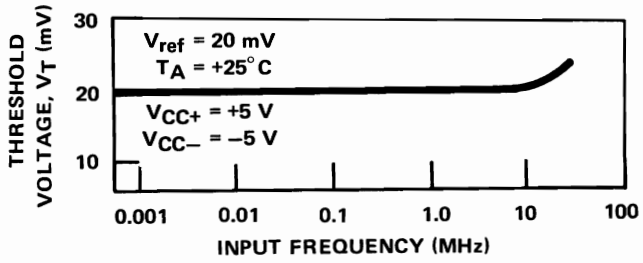


Figure 9.61. Threshold Frequency Response

This plot, made with a sine-wave input signal, indicates that the overall threshold frequency response is greater than 15 MHz. The upper frequency limit is determined primarily by propagation delay times. As most coincident current memories operate at input repetition rates of 3 MHz or less, Series 7520 devices are usable with virtually any core memory application.

The wide frequency response of the preamplifier results in minimal signal delay and good input waveform integrity at the output of the preamplifier. Since this output is applied directly to one of the inputs of the strobe gate (the other input being the strobe input), the strobe pulse position can be accurately positioned with respect to the input pulse — an important consideration in the determination of system timing.

Differential-Input Parameters — Several differential-input parameters influence the accuracy with which the threshold level of a sense amplifier can be set. The reference and input amplifiers of Series 7520 sense amplifiers have differential input circuit configurations. A dc path must be provided at the inputs for input bias currents. In sense-amplifier applications this dc path is normally provided by low-impedance (25 to 200 ohms) sense line termination resistors, R_T, from each sense input terminal. (See Figure 9.62.)

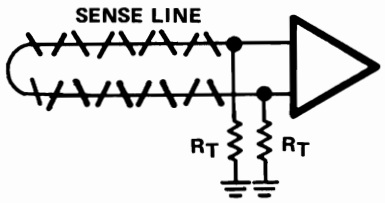


Figure 9.62. Termination Resistors Provide DC Bias

The reference amplifier must also have a dc bias path to ground for each input terminal. This, normally provided as part of the reference voltage source, is considered in a later section.

Typical input bias current for Series 7520 devices is in the 25- to 50-μA range, depending on the ambient temperature. The typical variation in input bias current as a function of temperature is indicated in the data sheets.

The data-sheet specification for input bias current for either the reference or sense-input terminals is 75 μA over the 0 to 70°C temperature range. When used in sense-amplifier applications with low termination resistor values, the effects of input bias currents in the specified range are relatively insignificant provided the bias currents to a given amplifier are reasonably matched. Input offset current, I_{DI}, or the difference in the input bias currents of a particular amplifier, varies as shown in the data sheets.

Because of the typically low input offset current of 0.5 μA, a maximum specification has not been included. A rigorous characterization indicates that approximately 98% of the amplifiers would comply with a 10-μA limit.

Another parameter purposely omitted from Series 7520 specifications is threshold offset voltage, V_{TO}, or the difference in the threshold levels for a given amplifier for opposite polarity input signals. Their threshold offset is typically 0.5 mV. Instead of including a threshold offset specification — a difficult measurement requiring calculation — the effects of offset voltage are absorbed in the threshold level

specification. Results of the threshold characterization indicate that offset voltage is relatively independent of the threshold level over the 15- to 40-mV specification range.

A factor of threshold offset to be considered is caused by mismatches in external termination resistors. This error is approximately equal to the product of the average input bias current and the resistor mismatch, or:

$$V_E \approx (R_{T1} - R_{T2})\, I_{in}$$

This error voltage is normally insignificant for reasonably matched (1%) termination resistors to ground in the 20- to 200-ohm range.

A more serious problem associated with termination-resistor mismatch is the reduction in common-mode rejection at the sense input. Series 7520 sense amplifiers normally reject in excess of 1 V of common-mode signal. Mismatch in terminal resistors can result in a differential-mode signal at the sense inputs which degrades the sense signal.

As an example of the importance of matched termination resistors, consider a high-level signal line (such as a strobe line) that passes near one of the sense preamplifiers, as illustrated in Figure 9.63. Assume that it has a signal with a rise time of 10 ns and 3 V amplitude, and capacitive coupling of 2 pF to each input (matched) terminal. Assume, however, that the 5% 100-Ω nominal termination resistors are mismatched by 10 Ω. As it can be shown that a differential signal of about 6 mV can be introduced, high-level signals should therefore be kept as isolated from the sense inputs as possible. Twisted pairs from the sense inputs to the memory will help reduce noise problems by assuring more nearly common-mode noise coupling.

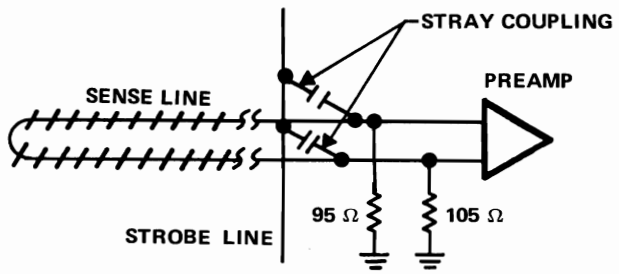


Figure 9.63. Unmatched Termination Resistors May Cause Noise Problems

Common-mode signals have little effect on the operation of Series 7520 devices until the common-mode signal approaches the common-mode dynamic range limits of the input. Tests indicate that at 25°C, dc common-mode signals up to +1.5 and −2.5 V cause changes in the threshold level of less than 0.5 mV — quite adequate for a properly designed memory.

One of the Series 7520 specifications is common-mode firing voltage, V_{CMF}, defined as the common-mode input voltage that exceeds the common-mode input range and causes false outputs. The data sheet shows the typical V_{CMF} of these devices as a function of temperature.

Overload recovery time is of prime importance in a sense-amplifier design. Series 7520 devices have excellent performance in this area. Since, normally, common-mode signals do not exceed the V_{CMF} of Series 7520 devices and therefore do not overload the devices, common-mode recovery time is not considered. However, differential overload recovery time may be shown as in Figure 9.64.

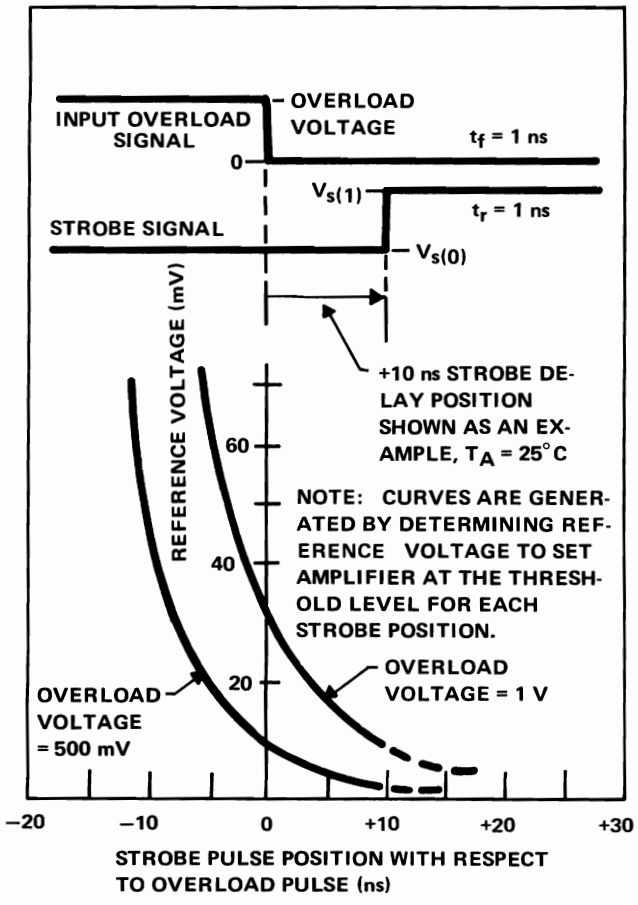


Figure 9.64. Differential Overload Recovery Time

Usually differential overload signals in a high-speed memory precede the sense signal by greater than 50 ns and are of 1000 mV amplitude or less. Devices in this series recover as shown in Figure 9.64. Within 20 ns after the overload signal has decreased to the sense-amplifier threshold level, the sense amplifier will have recovered to an extent that results in normal operation. Recovery time from amplitudes of less than 500 mV is less than the plot of 500 mV shown in the diagram. As Series 7520 devices have only a single gain stage and are strobed before the detector to prevent saturation of the detector, excellent recovery time is achieved.

Logic Interface Parameters — Series 7520 sense amplifiers are designed to be compatible with Series 74 TTL digital circuits. All logic inputs (i.e., strobe and gate inputs) and logic outputs are tested under the same test conditions as Series 74 to assure this compatibility.

Logic inputs are tested under worst-case conditions to make certain that no more than 1.6 mA flows from the input at a logic 0 voltage level. Similarly, each input is tested to assure that 40 μA or less flows into the terminal at a logic 1 voltage level. Currents into the input terminals are specified as positive values. The data sheets show typical logic input currents as a function of logic input voltage.

The plot in Figure 9.65 shows typical logic 0 input current for the strobe and gate inputs of these devices as a function of ambient temperature. The output gate of the SN7522 and SN7523 is a double-inverting configuration resulting in a higher voltage gain than other output gates and the strobe gates of the sense amplifiers, as evidenced by its steeper transition region (Figure 9.66).

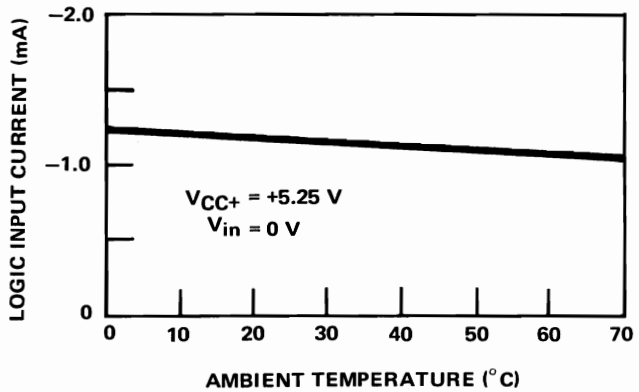


Figure 9.65. Logic Input Current as a Function of Temperature

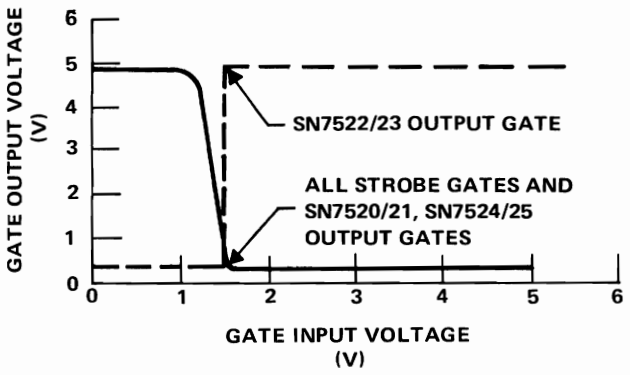


Figure 9.66. Logic Gate Voltage Transfer Plot

Each output is tested to ensure that the logic 1 output voltage will not fall below 2.4 V. This test is at full current load, lowest V_{CC+}, and 800 mV on the input (400 mV more than the guaranteed logic 0 maximum output level).

Each output is tested for maximum logic 0 output voltage of 400 mV at rated maximum sink current, lowest V_{CC+}, and 2.0 V on the input (400 mV less than the guaranteed logic 1 minimum level at rated maximum load current).

In actual system operation, the majority of the sense amplifiers do not experience worst-case conditions of current load or sink, supply voltage, temperature, and input voltage simultaneously. In addition the actual logic threshold voltage of Series 7520 devices is about 1.5 V, allowing extra margin beyond the guaranteed value.

The logic outputs of Series 7520 devices are specified in terms of sink and load current rather than in terms of fan-out, as with digital circuit families. This allows the user to quickly determine the fan-out to digital circuit configurations other than TTL, such as is used in Series 74. Fan-out to DTL, modified DTL, and even RTL can be determined.

Currents supplied by the logic outputs at the logic 1 level are load currents and are specified as negative values (out of the terminals). Currents into the output terminal (sink current) are positive.

9.3.5 General Application Considerations

Threshold Level Limitations — Under low-frequency conditions (operation from dc to 5 MHz) the recommended operating range of the reference supply is from 15 to 40 mV for the SN7520 series, except the SN75236 and SN75237 for which it is 4 to 25 mV. The device sensitivity and actual threshold level may vary ±4 mV for even-numbered and ±7 mV for odd-numbered devices. For the SN75236 it is ±3 mV; for the SN75237 it is ±6 mV.

Input pulse widths vary from 100 to 200 nanoseconds, according to the type of core system being used.

If the width of the incoming pulse is narrowed, its energy level is decreased. A larger input level is required to trigger the sense amplifier, even though the reference supply has not changed. This becomes particularly noticeable at input pulse widths of less than 50 nanoseconds. Figure 9.67 shows the effects of narrowing pulse widths on the threshold voltage. For example, a pulse width of only 20 nanoseconds will cause an increase in the threshold voltage of over 3 mV.

Bypass Considerations — The characteristics (particularly sensitivity) of this type of circuitry make it important that the reference supply be bypassed as close to the device terminals as possible. A 0.01-μF ceramic capacitor should be connected directly to the reference and ground terminals of the device. (See Figure 9.68.)

If a disc ceramic is used, it should be positioned to null out pickup and leave the reference line clean.

Some sense amplifiers, for example the SN7524, provide two ground terminals: ground 1 for small-signal (low-level) input stages, and ground 2 for large-signal (high-level) output stages. The reference input bypass must connect to ground 1.

Also, when using the basic SN7520 series, a 100-pF or greater capacitance should be connected from the C_{ext} terminal to ground, thus providing high-frequency roll-off for the reference amplifier and improving stability. The SN75200 series devices are internally compensated.

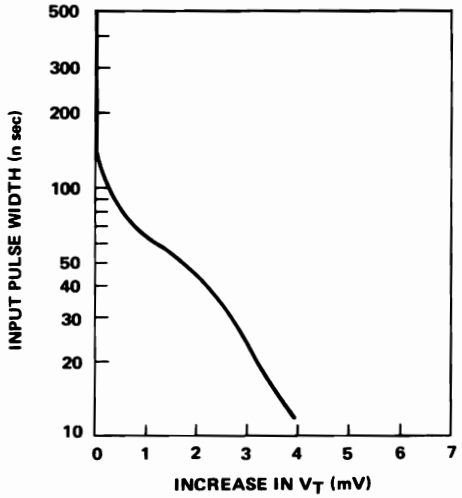


Figure 9.67. Typical ΔV_T vs. Pulse Width

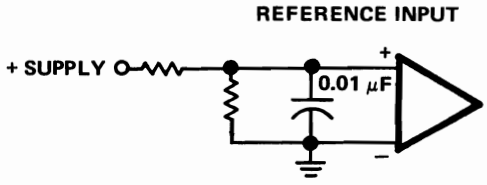


Figure 9.68. Bypass for Reference Input

Reference Voltage Source — As separation of the reference-supply voltage source from the other supplies usually is not practical, care in clamping and regulating the supply source is necessary to prevent supply ripple and transients from reaching the reference input. A divider network, as shown in Figure 9.69, is normally used to drop the voltage to a 15- to 40-mV level. It is desirable that the divider network be located as close to the device as possible, and long runs of reference-supply leads be avoided. If necessary to interconnect from one board to another, supply leads should be twisted to minimize inductive pickup.

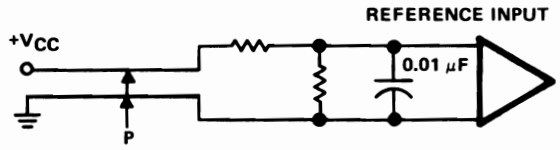


Figure 9.69. Twisted Supply Leads Minimize Inductive Pickup

Most systems employ a large number of sense amplifiers. For simplicity and economy a single reference voltage is distributed to all sense-amp reference terminals. Two factors can help reduce noise pickup and interference between amplifiers:

1) Use of a twisted-pair line and balanced termination (Figure 9.70) to take advantage of the common-mode rejection characteristics of the reference input. Transients induced into the twisted pair generate common-mode voltages which are rejected at the reference input.
2) A low-impedance voltage source to lower the level of induced transients on the reference line and reduce any cross-coupling between sense amps. An operational amplifier followed by an emitter-follower transistor (Figure 9.70) is a reliable low-impedance source.

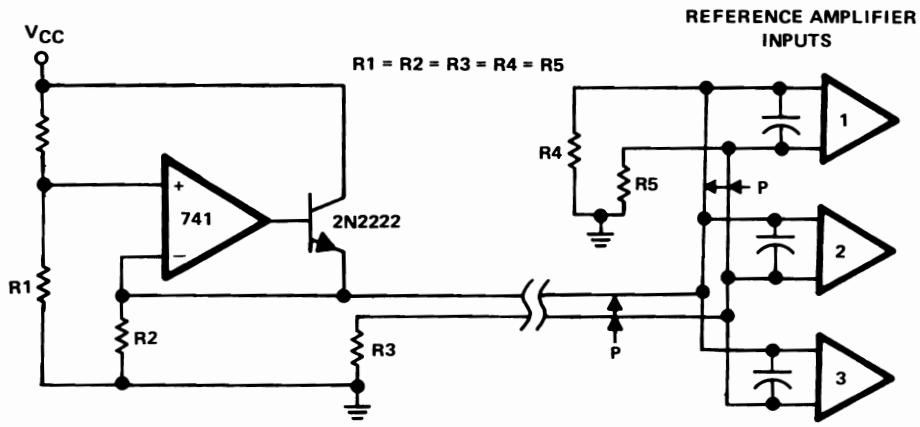


Figure 9.70. Balanced Termination of Low-Impedance Reference Voltage Source

Termination resistors for the reference supply should be located close to the reference input terminals and be bypassed at that point. Current-input requirements at the reference amplifier are small (approximately 100 μA) and therefore a bias current of about 1 milliamp in the divider network is adequate.

The layout of the reference-supply circuitry, as for any circuitry in a sensitive system such as this, can be critical. Care in keeping the reference-supply leads and ground paths separated from high-level current paths, such as those associated with the output and strobe circuitry, is imperative.

Power Supplies — Because of the unique design of the SN7520 series the power supplies do not need to be highly regulated. Supply voltages in the range of 5 volts (plus and minus) regulated to ±5% are satisfactory.

In preventing transients from interfering with the input and reference signal paths, it is important that the supplies be well bypassed. Decoupling procedures are similar to those used in high-frequency applications.

For optimum performance power-supply leads should be bypassed as close as possible to the sense amplifier package, using low-inductance disc-ceramic capacitors. Selection of a bypass capacitor should include serious consideration of environmental conditions and available space; also, the equivalent circuit of the point to be bypassed should be studied to assure that at frequency of operation the bypass capacitor will not exhibit inductive reactance because of long leads. Ceramic capacitors with copper ribbon leads may be used to reduce inductive characteristics. A value of 0.01 μF is typical.

Separate high-level and low-level supply lines should be provided where possible, to reduce coupling into low-level input circuitry. An analysis of the current requirements of various stages will prove helpful in supply-line layout.

Sense-Line Termination — The sense-line output from a memory should be terminated in its characteristic impedance, which is around 200 ohms for a typical sense line. Termination would consist of a 100-ohm resistor from each line to ground (see Figure 9.71). Sense amps and termination resistors should be placed

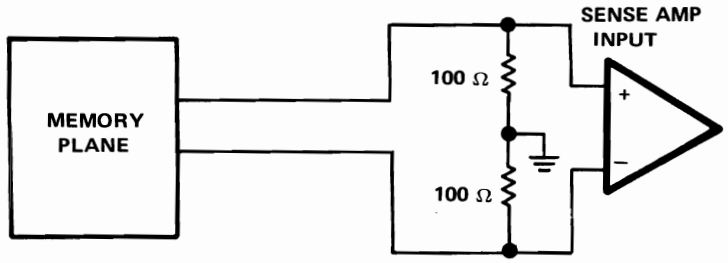


Figure 9.71. Typical Sense-Line Termination

close to the memory plane to avoid unnecessary pickup. As signal levels to be sensed are small, attenuation of long lines should be avoided.

Transition Time — The linear region, around the threshold point, of a typical Series 7520 sense amplifier is about 1 to 2 mV wide. Thus it is important that an adequate input level be used. Sufficient drive to swing through the linear region will help reduce any tendencies to oscillate.

Input voltage specifications of ±4 mV or ±7 mV assure getting a logic 1 output with an input signal that is at the threshold voltage plus these limits. If for example the threshold voltage is 20 mV, the output, under worst-case conditions, will switch by +24 or −24 mV when using a ±4-mV unit. The other possibility is that it will switch at an input level of +16 or −16 mV.

The normal slew rate of the input is from 0.1 to 1 volt per microsecond. If the slew rate is as low as 0.01 volt per microsecond or less, the sense amplifier may oscillate.

Strobe Inputs — If a channel is not in use its strobes should be grounded, thus disabling the channel and reducing noise pickup that might interfere with other channels.

Due to the slight propagation delay of the input amplifier and sense-line circuitry, it is necessary to delay the strobe input so that it occurs after the core stack is interrogated. The strobe must be timed to coincide with the incoming data pulse at the input to the strobed gate, as shown in Figure 9.72.

The SN7528 and SN7529 have a test point brought out from the gate input. Proper strobe positioning may be verified by observing its relationship to the incoming signal at that point, with an oscilloscope, taking care to avoid loading this point during these observations.

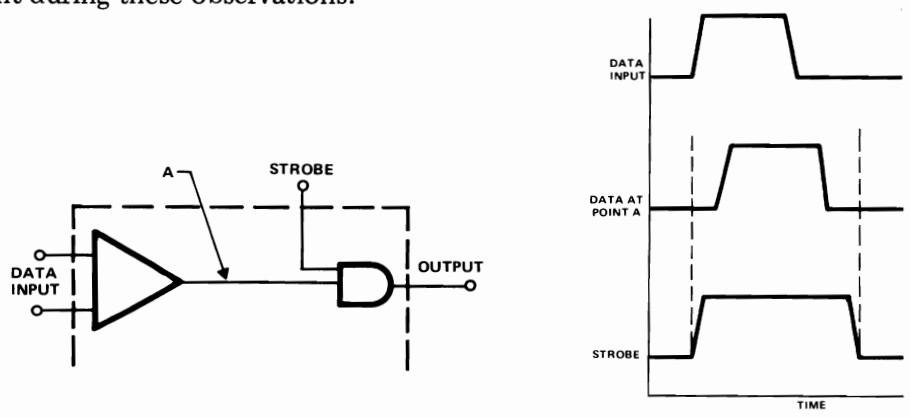


Figure 9.72. Strobe Timing

Output Considerations — Series 7520 sense amplifiers have standard TTL type gate outputs. Interfacing between them and other forms of logic (e.g., MOS) requires the same type of circuitry used with standard TTL. SN75450B type peripheral drivers and SN75361A type drivers may be used to interface between TTL and many other types of logic. Circuit details are given in the chapter on MOS drivers and the chapter on peripheral drivers.

Outputs from SN7520 type devices generally have active pull-up and pull-down transistors or standard totem poles. In most cases the strobe inputs to outputs are non-inverting.

Sometimes it is desirable to have open collector outputs for the purpose of wire-AND connecting several units together. It is then necessary that the output be inverting from the strobe, allowing all the outputs of units strobed off to be high and not interfere with an operating unit.

The addition of an SN74H01 gate or SN7406 gate as an inverter will also yield the desired open collector output, and will extend the total propagation delay no more than 8 nanoseconds. When used with the SN7524, for example, the total propagation delay is only 28 nanoseconds maximum.

The following device types have resistive pull-up circuits at their outputs:

SN7520	SN7521
SN7524	SN7525
SN7528	SN7529
SN75234	SN75235
SN75238	SN75239

It is sometimes desirable to wire-AND the outputs of these devices. They may be wire-AND connected within the limits of their individual output-handling ability. The following table gives recommended limits of AND-connected stages versus fan-out.

TTL Fan-Out	Max No. of Wire-AND Outputs
1	6
2	5
3 to 4	4
5	3
6 to 7	2

PC Board Layout — Memory sense amplifiers are sensitive, high-speed systems, and layout can be critical. An important consideration is the separation of high-level and low-level lines. Supply points for relatively high-level currents should be the same as, but bypassed separately from, those of low-current requirements. For example, the supply line feeding the reference circuit should not be associated directly with the one handling current from output stages of the sense amplifiers.

When multilayer boards are available, placing low-level and high-level signal paths on opposite sides of the board will prove helpful. Every precaution taken to prevent feedback from high-level output signals to sensitive inputs provides a more reliable and faster-operating system.

As in any system, care should be taken to prevent ground loops. A basic approach is to make certain there are not two paths from any point in the circuit back to the ground terminal. Such an error is often made where the ground completely encircles the PC board.

By breaking the ground lead circle we have two different ground leads. Low-level ground currents and sensitive input circuitry can be referenced to one ground path, and higher currents, like those related to output circuitry, can be referenced to the other.

With two-layer boards, low-level supply and grounds may be placed on one side and high-level signal paths on the other. An even better method is the use of a three-layer board with a ground plane between the high- and low-level signal paths. The ground plane will reduce coupling between the other board layers and further improve operating conditions.

As with any sensitive high-speed system, the key to error-free operation is a clean, well-ordered layout with good decoupling and isolation of sensitive input and higher level output signals.

Additional Device Characteristics — Table 9.8 illustrates the logic output and logic input specifications for Series 74 standard TTL, Series 74L low-power TTL, and

Table 9.8. Logic Specifications

Family	$V_{out(0)}$	$V_{out(1)}$	$I_{in(0)}$	$I_{in(1)}$
74 7520	0.4 V @ 16 mA	2.4 V @ –400 μA	–1.6 mA @ 0.4 V	40 μA @ 2.4 V
74L	0.4 V @ 3.6 mA	2.4 V @ –200 μA	–0.18 mA @ 0.3 V	10 μA @ 2.4 V
74H	0.4 V @ 20 mA	2.4 V @ –500 μA	–2.0 mA @ 0.4 V	50 μA @ 2.4 V

SERIES 7520 DRIVE CAPABILITY:

1) 8 Series 74H TTL digital circuits
2) 10 Series 74 TTL digital circuits
3) 40 Series 74L TTL digital circuits

Series 74H high-speed TTL circuits. Series 7520 devices are the same as Series 74 standard TTL. From these specifications it can be determined that Series 7520 devices exhibit the drive capability shown below the table.

In most applications less than the maximum fan-out capability is required. In these applications it may be desirable to use the extra output sink capability to drive a load resistor to improve capacitive load driving ability and decrease output rise time.

Many characteristics of Series 7520 devices are not specified over the full temperature range. Figures 9.73 through 9.84 indicate the typical performance of these devices over the 0 to 70°C temperature range under data-sheet test conditions. These curves should be helpful to the memory designer in using these devices.

ADDITIONAL TEMPERATURE CHARACTERISTICS

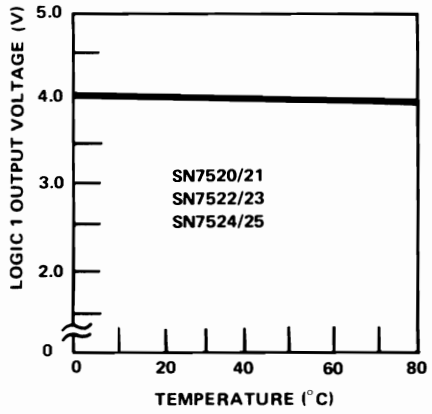


Figure 9.73

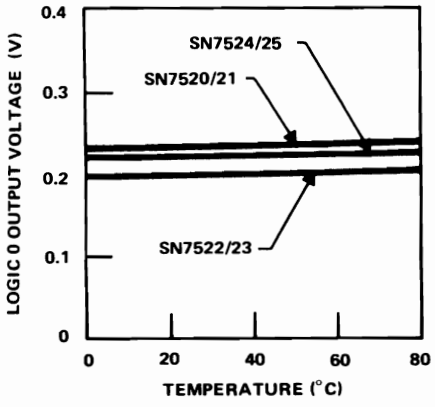


Figure 9.74

ADDITIONAL TEMPERATURE CHARACTERISTICS (CONT.)

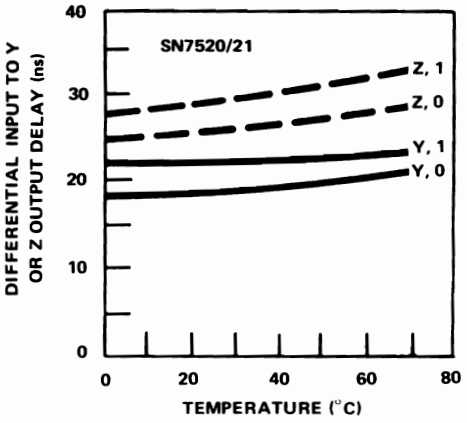


Figure 9.75

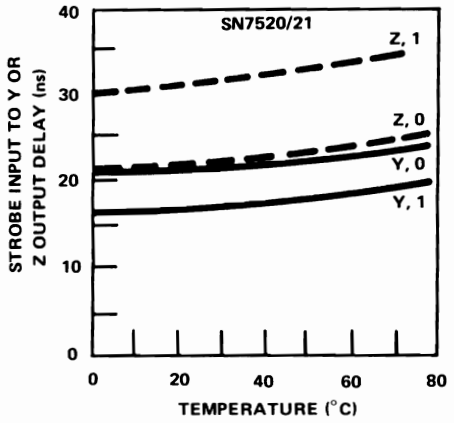


Figure 9.76

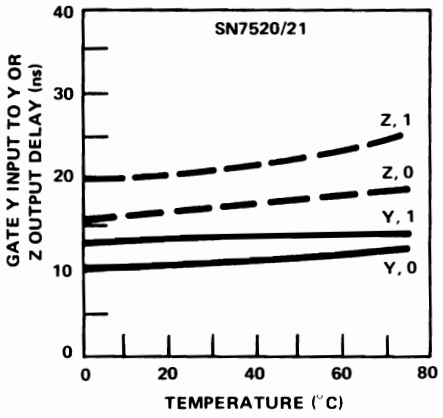


Figure 9.77

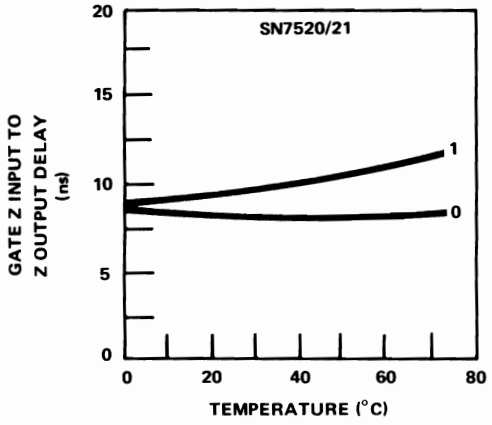


Figure 9.78

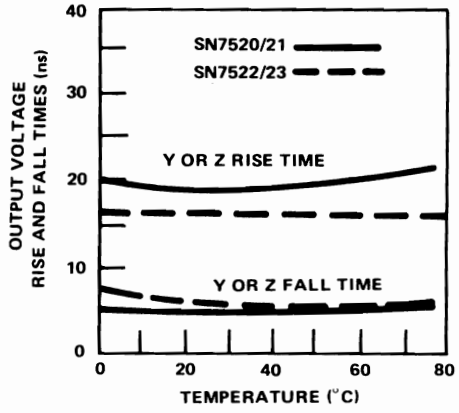


Figure 9.79

ADDITIONAL TEMPERATURE CHARACTERISTICS (CONT.)

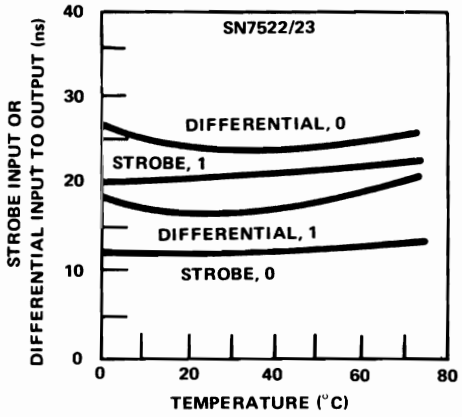


Figure 9.80

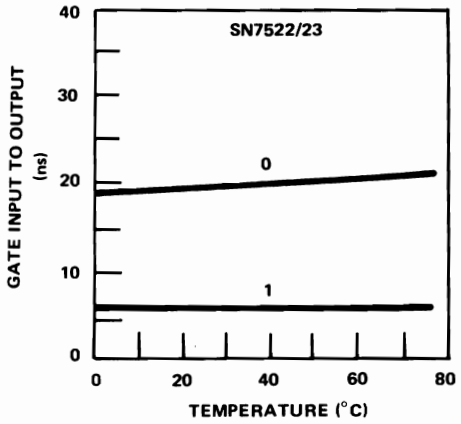


Figure 9.81

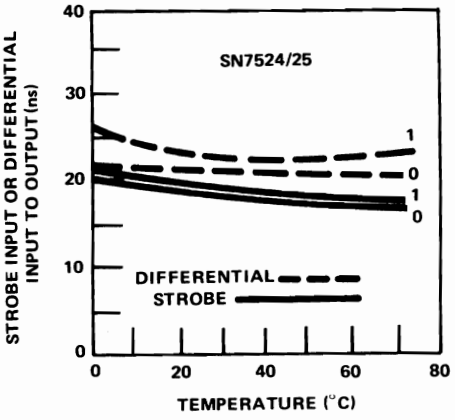


Figure 9.82

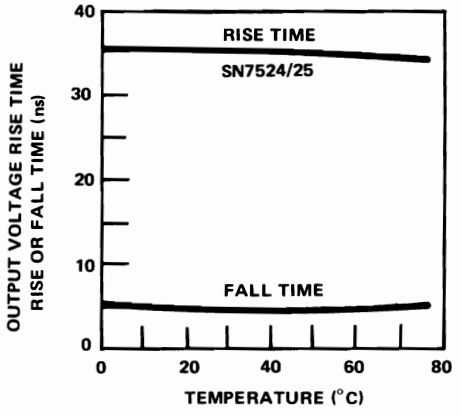


Figure 9.83

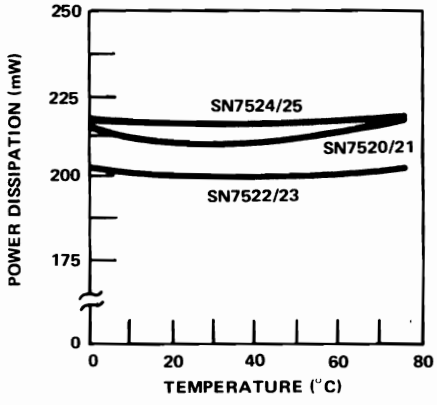


Figure 9.84

9.3.6 Specific Device Applications

Discrete sense-amplifier designs usually utilize reactive components such as inductors and capacitors to eliminate problems caused by dc bias level drift. Integrated sense amplifiers ordinarily have capacitive coupling for the same reason; or a dc comparator is used with a complicated input resistor network to obtain threshold action. These methods, however, introduce additional problems:

1) Reactive coupling usually results in threshold shift with increased repetition rates.
2) Reactive coupling results in excessive overload recovery time.
3) Input resistor networks degrade the common-mode rejection of the design and require expensive precision components.
4) Redundant circuitry results in excessive power.
5) High package or component count uses excessive board area and excessive interconnections, and reduces reliability.

Series 7520 devices incorporate the necessary circuitry to perform sensing for two sense lines without confronting these undesirable characteristics. This performance is achieved through the unique matched-amplifier circuit design which utilizes the inherent matching and tracking characteristics of integrated-circuit components. This design permits an all dc-coupled circuit without the associated dc drift problems. The result is close matching of all the sense channels for maximum system performance.

This results in a much higher signal-to-noise ratio than can be obtained with a larger number of cores on a sense line. Also, delays from various bit locations are more uniform, allowing more precise strobing.

In these memories it is common practice to limit the number of cores on each sense line to about 4000. Large core planes are sectored into smaller subplanes of approximately 4000 bits as shown in Figure 9.85, with separate sense lines for each subplane.

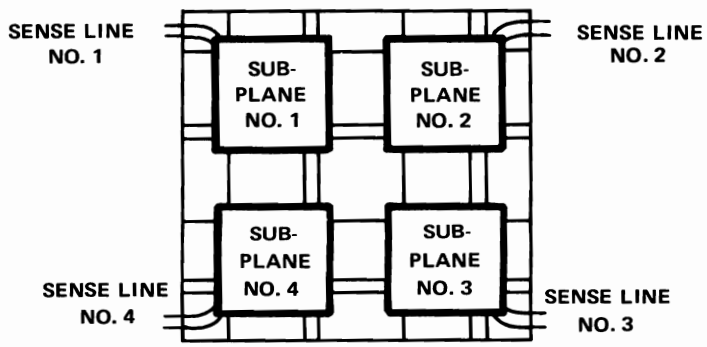


Figure 9.85. Sectored Core Plane

SN7520, SN7521 Applications — The SN7520 and SN7521 sense amplifiers are complete monolithic subsystems, incorporating all necessary threshold, strobing, and logic functions for sensing, gating, and storing information from up to 8000 cores in the memory. The output circuit of the SN7520 and SN7521 consists of two cascaded NAND gates. External inputs are available as logic inputs to each of the gates.

The gates may be connected in a cross-coupled gate latch configuration (Z output to Gate Y input) as shown in Figure 9.86. Thus the output circuit is able to function

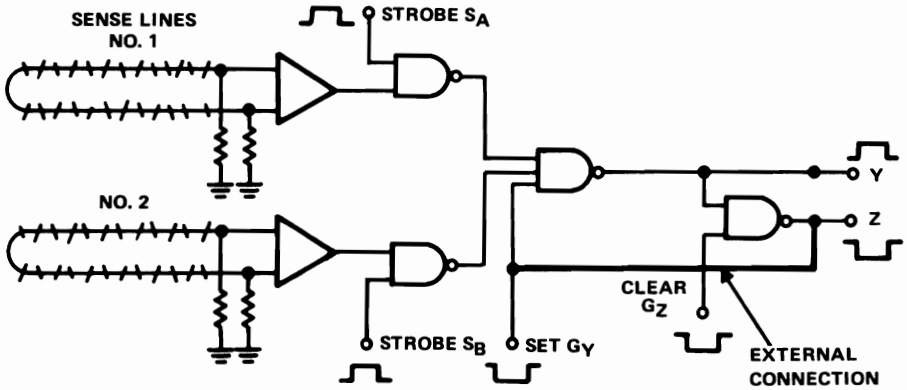


Figure 9.86. Cross-Coupled Gate Latch Configuration for SN7520 or SN7521

as part of the Memory Data Register (MDR). Information extracted from the sense lines during the strobe enable pulse can be retained as long as desirable for use with the computer logic section. A negative-going pulse applied to the Gate Y input clears the latch prior to the next strobe enable pulse.

In those applications where output pulse stretching is desirable, the gates in the output section of the SN7520 and SN7521 may be capacitively coupled, as shown in Figure 9.87. In some applications neither the latch configuration nor output pulse

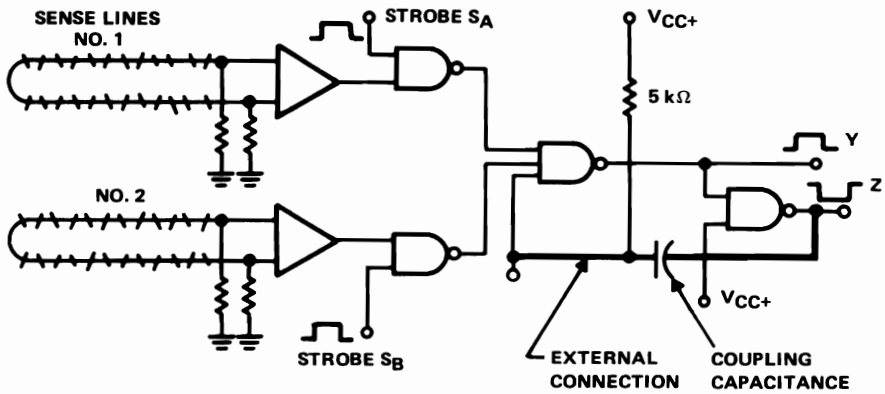


Figure 9.87. Output Pulse Stretching

stretching may be required. In these cases the gates in the output of the SN7520 or SN7521 may be used as a part of the logic unit, supplying complementary output logic levels with standard TTL fan-out capability.

In applications not utilizing the external gate inputs (Gate Y and Gate Z inputs) these terminals should be tied to the positive supply (V_{CC+}) to prevent capacitive coupling at these terminals from affecting delay times. Strobe inputs should be treated similarly.

In some memory applications more than 8000 words may require sensing. The dual sense input function of the SN7520 or SN7521 may be expanded to four sense inputs by addition of a dual-input SN7522 or SN7523 sense amplifier. The 4000 bits per sense line limit referred to in this book is a helpful rule of thumb which results in a favorable signal-to-noise ratio, thereby permitting good system performance. However, in especially clean (low-noise) memory designs it may be possible to have 8000 or more bits per sense line. Use of the SN7522 or SN7523 as an expander will be considered in detail in the next section.

SN7522, SN7523 Applications — The SN7522 and SN7523 have as an output circuit an open-collector gate that may be connected to perform the wire-AND logic function, thus permitting a logic level to be implemented without additional gate delays. Each SN7522 and SN7523 also has an internal load resistor of approximately 2000 ohms. One end of the resistor is internally connected to the positive supply (V_{CC+}); the other end is brought out through a separate pin. The resistor may be used as a collector pull-up resistor in applications where its value is acceptable. Load resistors from several SN7522 or SN7523 packages may be connected in parallel for lower impedance.

The output gate of the SN7522, SN7523 circuit is designed for high sink current capability. Although the specifications indicate a limit of 0.4 V maximum output logic 0 voltage level while sinking 16 mA, this limit is conservative, as indicated by the typical curve for this parameter.

The high output sink current capability increases the versatility of the SN7522, SN7523 circuit in a variety of applications. Several SN7522/23s may be wire-AND connected to provide the necessary number of sense inputs for large memory applications. Also, the output may be wire-AND connected with other sense amplifiers such as the SN7520/21. In this application, shown in Figure 9.88, the output of a single SN7520 or SN7521 is connected as a latch to function as part of the memory data register. As many SN7522 or SN7523 sense amps as necessary are connected to provide additional sense inputs to the MDR. The gate input terminal of each of the SN7522/23s in this application serves as an external set input for the MDR, allowing information to be entered into the MDR from the logic section. The Gate Z input of the SN7520 or SN7521 serves as the clear input for the latch in this application.

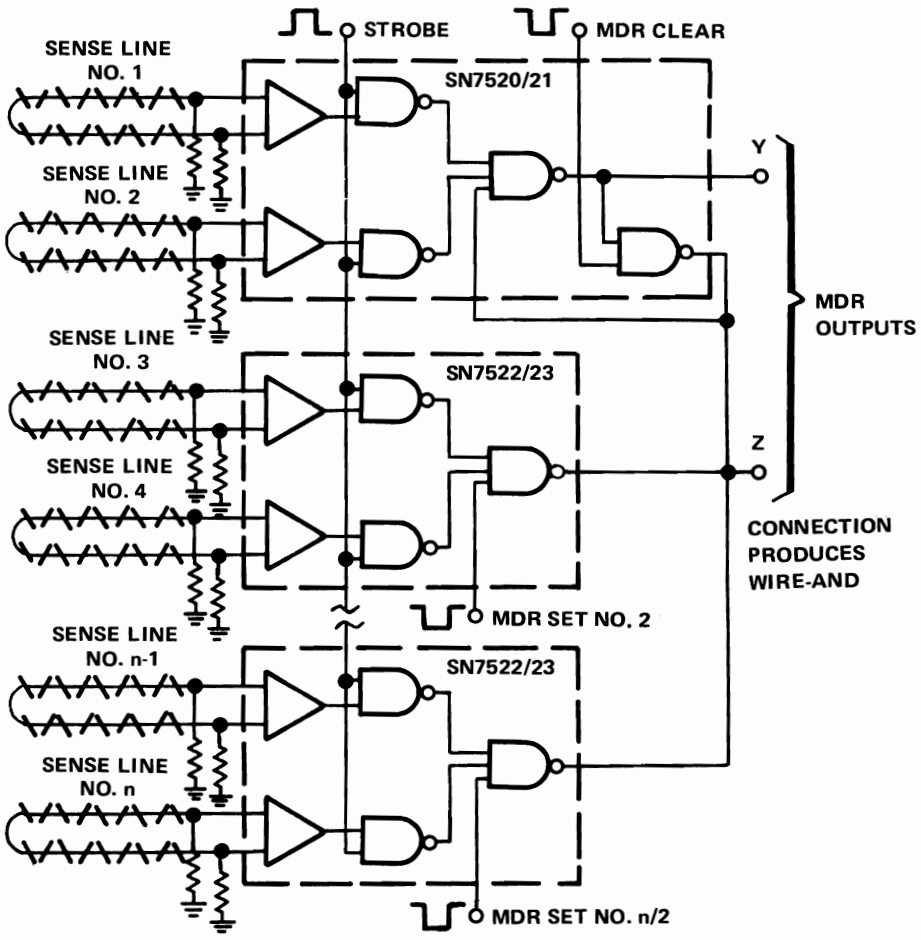


Figure 9.88. Use of SN7522/SN7523 as an Input Expander for the SN7520/SN7521

The output of the SN7522 or SN7523 may also be wire-AND connected with logic gates that feature this capability. This includes most diode-transistor logic (DTL) gates and the SN7401 quad two-input positive NAND gate.

In applications in which more than a simple latch is desirable for the MDR, several options may be considered. For example, the SN7474 dual D-type edge-triggered flip-flop is excellent for use with the SN7522 or SN7523. The SN7474 features direct clear and preset inputs and complementary outputs. Input at the D input is transferred to the Q output of the SN7474 on the positive edge of the clock pulse.

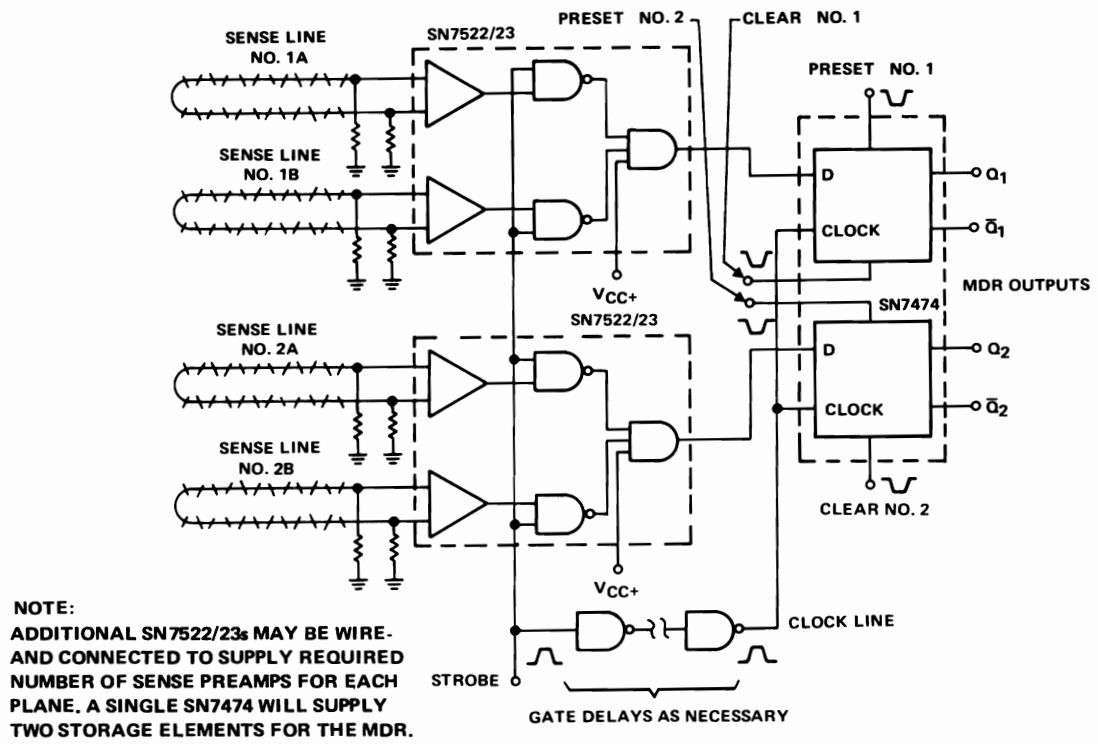


Figure 9.89. Use of SN7522/SN7523 with SN7474 as Memory Data Register

The outputs of one or more SN7522 or SN7523 circuits can be connected as shown in Figure 9.89 to provide inputs to the SN7474. A single SN7474 can provide two storage elements for the MDR. If a separate clock pulse is undesirable, the clocking function can be furnished by the strobe input. Proper delay must be provided to ensure that the D input is set up at clock time. In this application an inversion occurs from the sense inputs to the flip-flop output. Logic 1 sense inputs ($> V_T$) enter logic 0 levels into the Q output, because of the negative-going output from the SN7522/23.

SN7524, SN7525 Applications — The SN7524 and SN7525 sense amplifiers feature two separate sense amplifiers in a single package. Separate inputs, strobes, and outputs permit a single SN7524 or SN7525 package to service two separate bit planes in a memory. Since its outputs cannot be wire-AND connected because of the normally low output level, the SN7524 and SN7525 circuit finds widest application in small memories of up to about 4000 words. In such applications the SN7524/25 results in half the package count normally required. It also increases reliability and

reduces the memory size by means of fewer interconnections, less board area, and less power than other sensing schemes, as indicated in Figure 9.90.

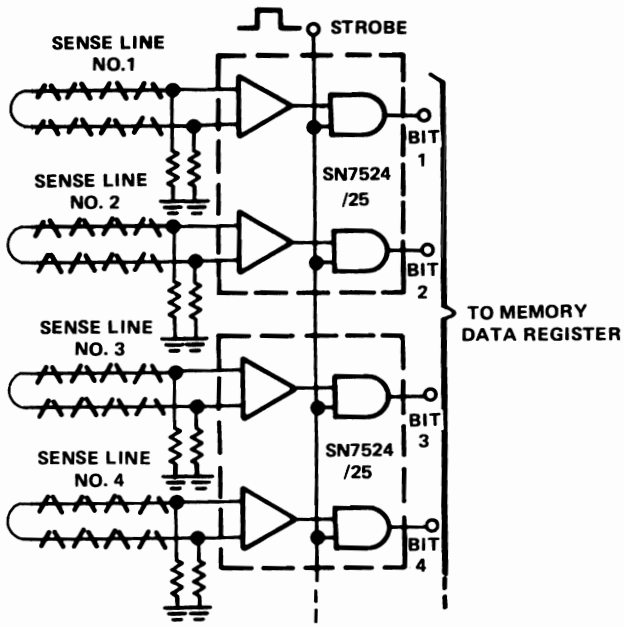


Figure 9.90. SN7524/SN7525 for Sensing Small Memory

Another useful application of this sense amplifier is in conjunction with the SN7475 quadruple bistable latch, as shown in Figure 9.91. In this application, the

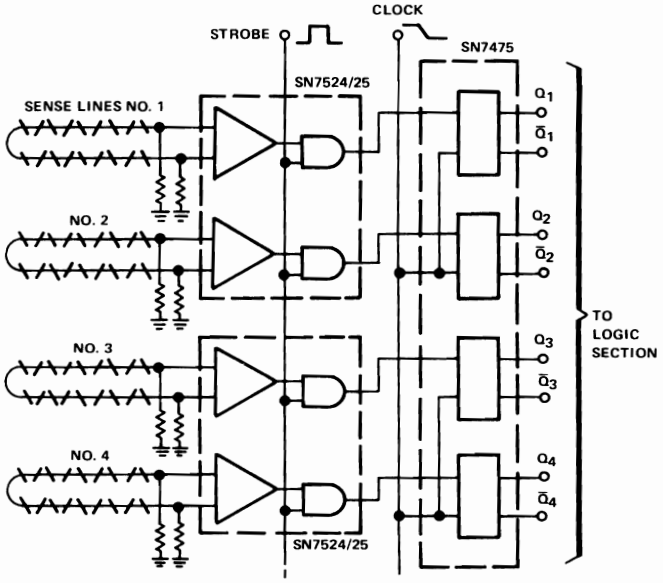


Figure 9.91. Use of SN7524/SN7525 with SN7475 as Memory Data Register

SN7475 is the memory data register (MDR) for two SN7524 or SN7525 packages. Four bits of the memory word are thus sensed and stored with only three integrated-circuit packages. Operation is as follows: While the clock input to the SN7475 is high the Q output follows the D input; when the clock input goes low, the information contained in the latch is retained until the clock input is permitted to return to the high state. When used with the SN7524 or SN7525 devices the SN7475 can retain information read from the memory for as long as desired. The negative edge of the clock must be timed to occur while the information is present at the output of the SN7524 or SN7525 sense amplifiers.

For a more exotic application, an SN7474 dual D-type flip-flop may be used with an SN7524 or SN7525, as shown in Figure 9.92.

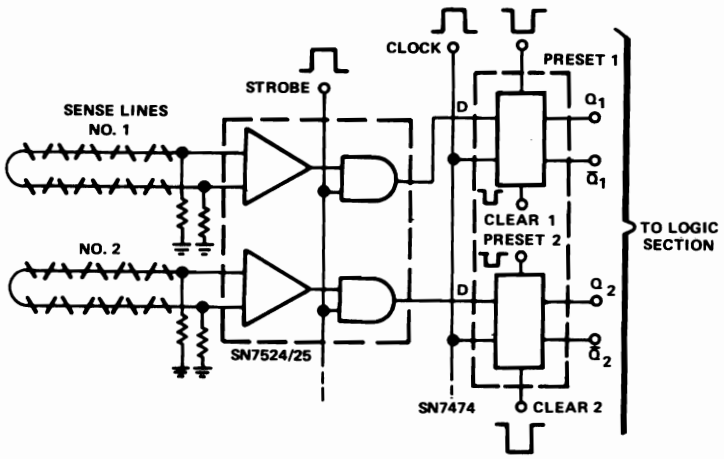


Figure 9.92. Use of SN7524/SN7525 with SN7474 as Memory Data Register

The SN7474 functions in a manner similar to that of the SN7475. Operation is as follows: The positive edge of the clock pulse shifts the information present at the D input to the Q output on the flip-flop; the Q output does not "follow" the D input except on the clock pulse command. The strobe input pulse may be used to supply the clock input pulse by adding the proper delays (Figure 9.93).

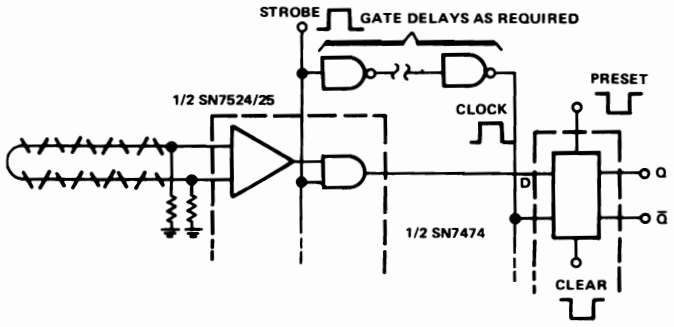


Figure 9.93. Delayed Strobe Pulse Drives Clock Input of SN7474

The positive edge of the strobe pulse should occur during the input pulse. The delays introduced from the strobe input to the clock input allow the sense information to propagate to the D input of the flip-flop, thereby ensuring that the clock pulse is properly timed with respect to the D input information. Since each SN7474 contains two D-type flip-flops, two planes can be serviced by a single SN7474 and a single SN7524 or SN7525. The SN7474 may have an advantage over the SN7475 since it includes external set and clear inputs, allowing entry into the two bits of the memory data register (formed by the SN7474) from an external source.

If it becomes desirable to OR the outputs of the SN7424 or SN7525, this process can readily be accomplished by the addition of a positive NOR gate, such as those comprising the SN7402 TTL device. This device is a quadruple 2-input positive NOR gate, and can be used to OR four pairs of SN7524 or SN7525 outputs, as shown in Figure 9.94. If more than two outputs are required in the OR connection, it is more desirable to utilize the wire-AND capability of the SN7522 or SN7523 for this application.

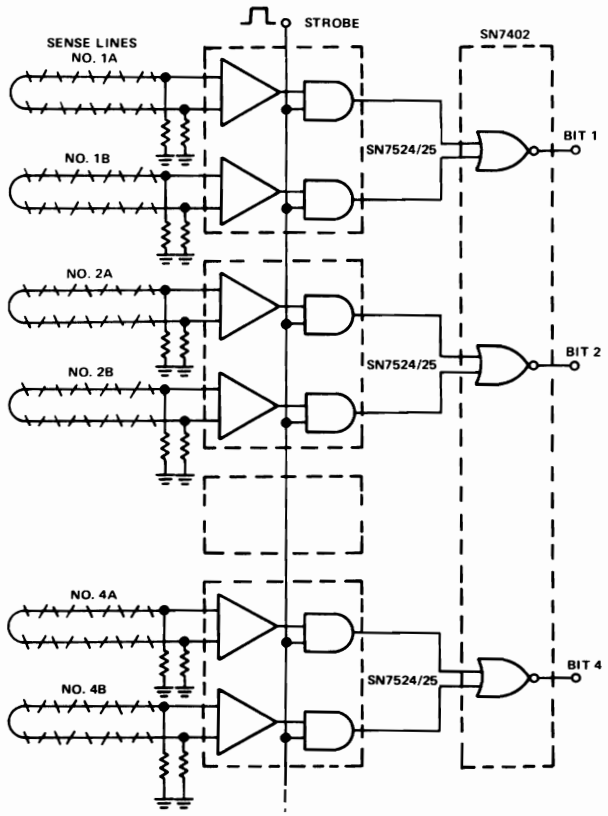


Figure 9.94. SN7402 Used to OR Four Pairs of SN7524/SN7525 Outputs

In either application the optimum threshold level can be determined for the memory by adjusting the threshold levels of the sense amplifiers. In extremely "tight" designs it may be desirable to adjust sense-amplifier threshold levels on an individual package basis. On less stringent applications, all threshold levels may be adjusted in parallel.

SN7526, SN7527 Applications — As noted with the SN7524 and SN7525, it is possible to use the SN7475 devices as a memory data register. With the SN7526 and SN7527 a memory data register is built into the device. Another advantage is that the two channels are OR connected internally prior to the MDR. As can be seen in Figure 9.95, the selection of core planes to be sensed in a matrix pattern simplifies strobing and external circuit requirements.

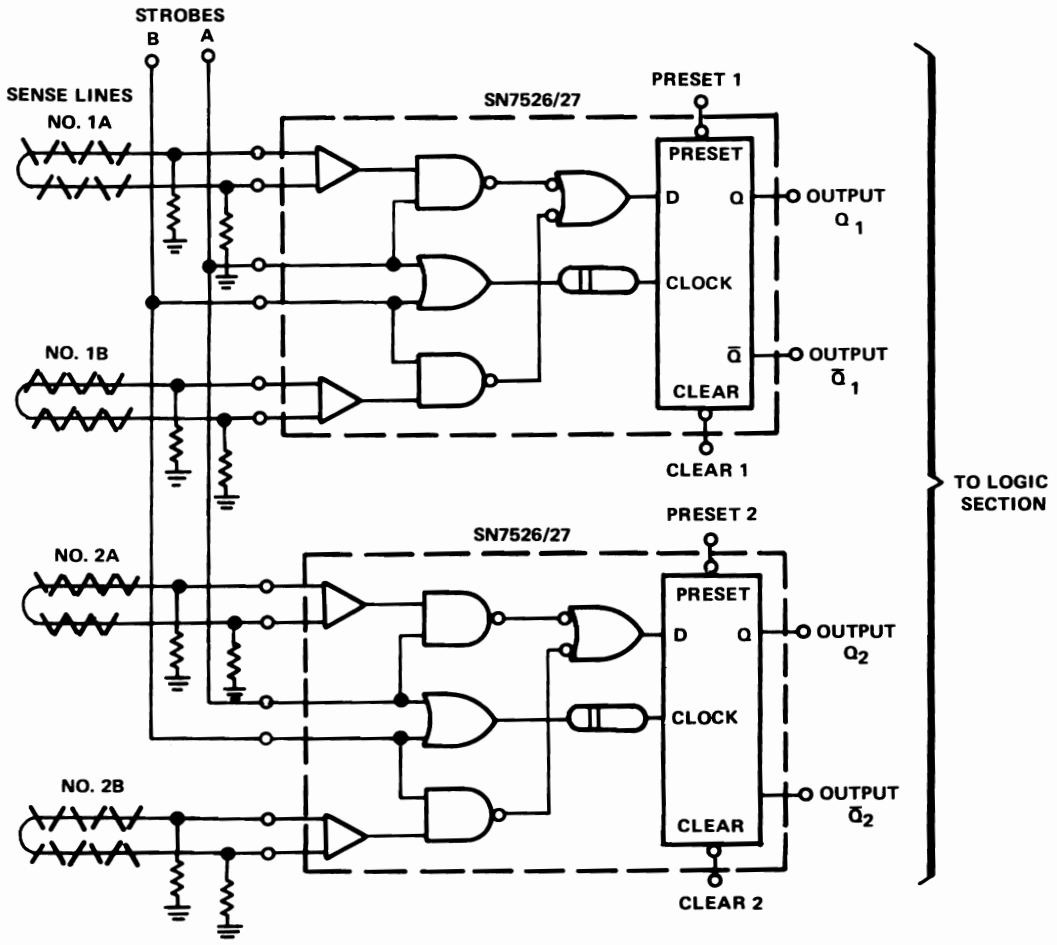


Figure 9.95. SN7526/SN7527 Provides Internal OR and MDR Functions

SN7528, SN7529 Applications — Application of an SN7528 or SN7529 is the same as that of the SN7524 and SN7525, except that a test point is available at each preamp output (or gate data input) to aid in the proper alignment of the strobe pulse with the data.

This application demonstrates an improved method of sensing data from relatively small memory systems. Two individual core planes, usually consisting of 4096 cores each, can be interfaced by each of the dual-channel SN7528 or SN7529 sense amplifiers; see Figure 9.96. Standard TTL or DTL integrated circuits, driven directly from the compatible sense-amplifier outputs, may be selected to serve as the memory data register (MDR).

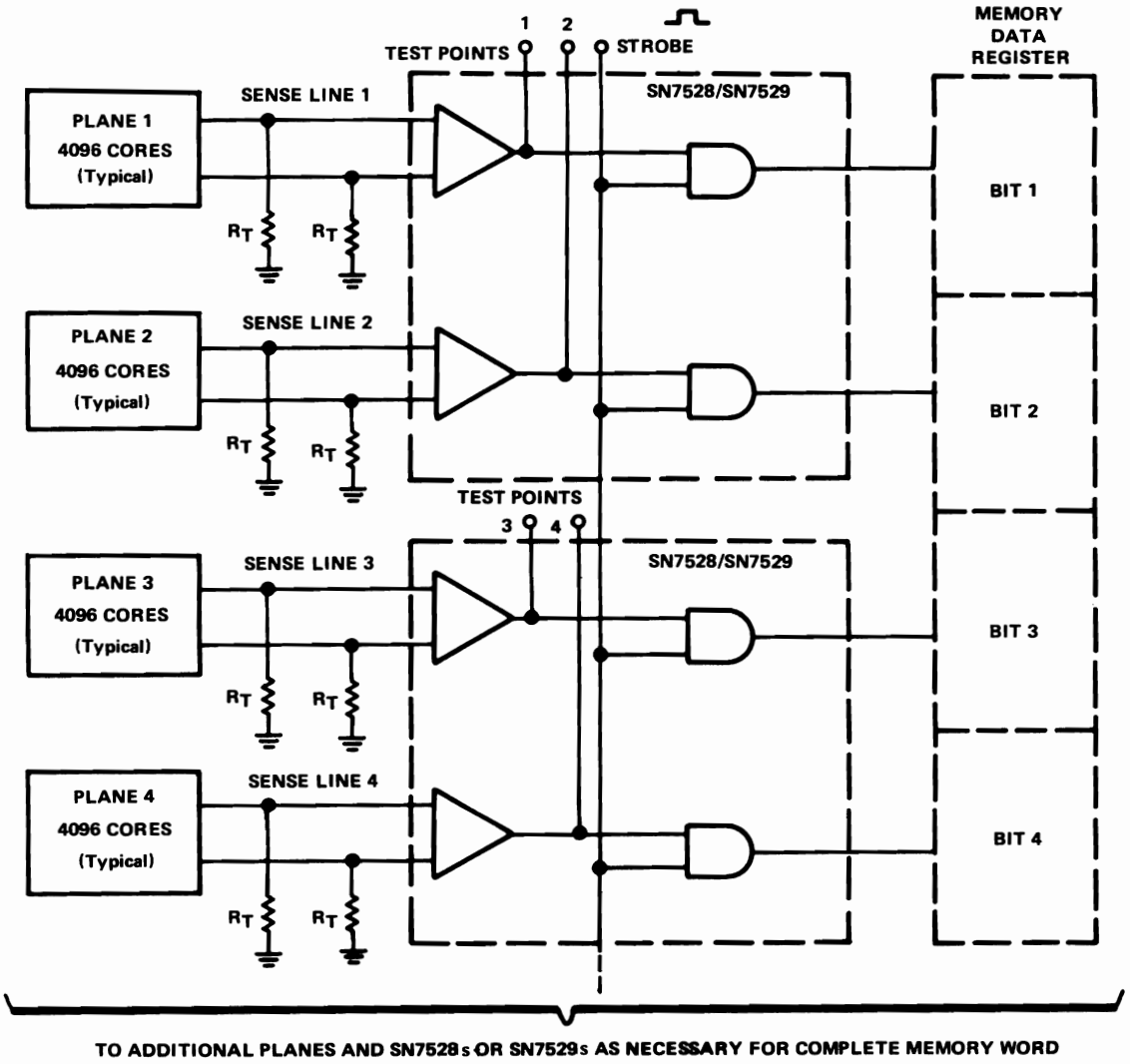


Figure 9.96. SN7528/SN7529 Sense Amplifier System

SN75232, SN75233 Applications — Three basic improvements in the SN7524 and SN7525 circuit allow, in most applications, a decrease in external components required. The output gate is a NAND rather than an AND function; the output is open collector; and it is internally compensated. As can be seen in Figure 9.97, the outputs may be connected directly, and the external circuitry, as seen in Figure 9.94, is not required.

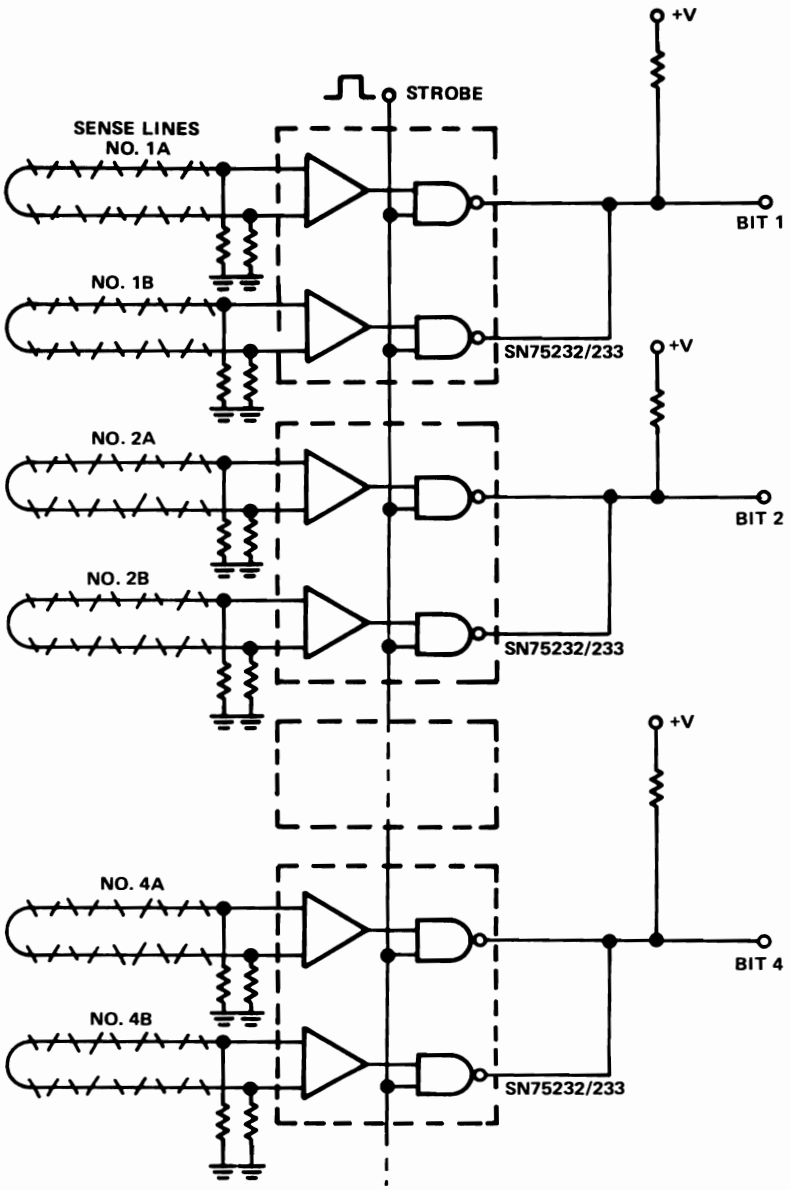


Figure 9.97. SN75232/SN75233 Produces Simpler Sense Amp System

SN75234, SN75235 Applications — Figure 9.98 shows the SN75234 or SN75235 used in sensing a series of 4K-bit memory planes. It is similar to the application of SN7524 or SN7525 devices, except that some memory data registers which would have required a preceding inverter do not need it for this application.

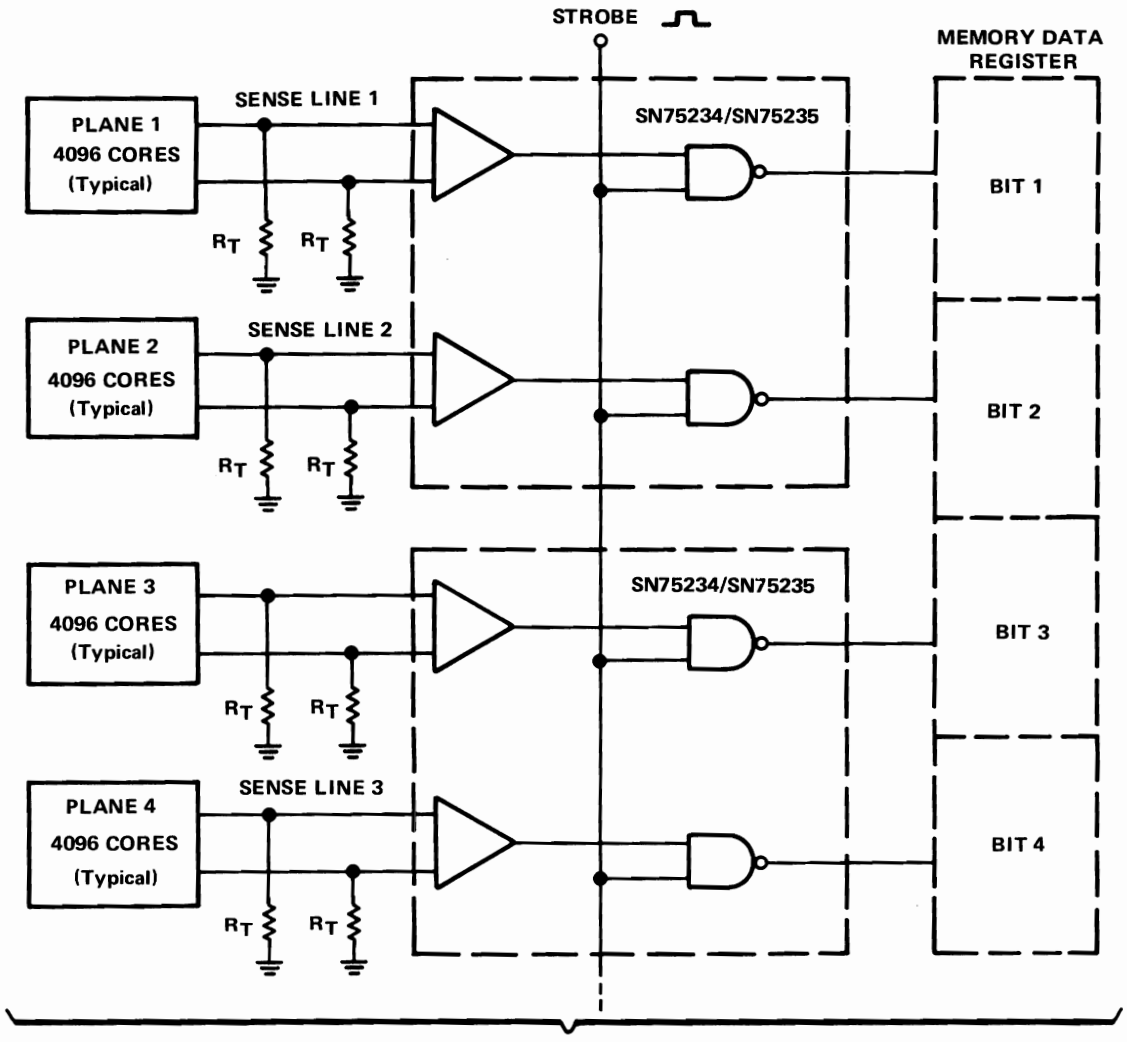


Figure 9.98. SN75234/SN75235 Sense Amplifier System

SN75236, SN75237 Applications — The SN75236 and SN75237 are special types of devices with highly improved performance capability and versatility as sense amplifiers. As may be seen from Figure 9.99 the input section (preamplifier and gates) is similar to that of the basic SN75234 or SN75235; in addition it has a common strobe and individual channel selects. The channel detector outputs feed directly to their respective built-in data registers. Where necessary the channel 2 detector output may be connected to the channel 1 register input for an AND-type function. Each register can have data entered from an external source, and this device may be used in the read/rewrite as well as the write function. To facilitate these functions, output buffers and normal register outputs are provided. The improved sensitivity of this device allows greater noise margins and permits operation in high-speed systems where the output signals are only 15 to 20 millivolts (Figure 9.100).

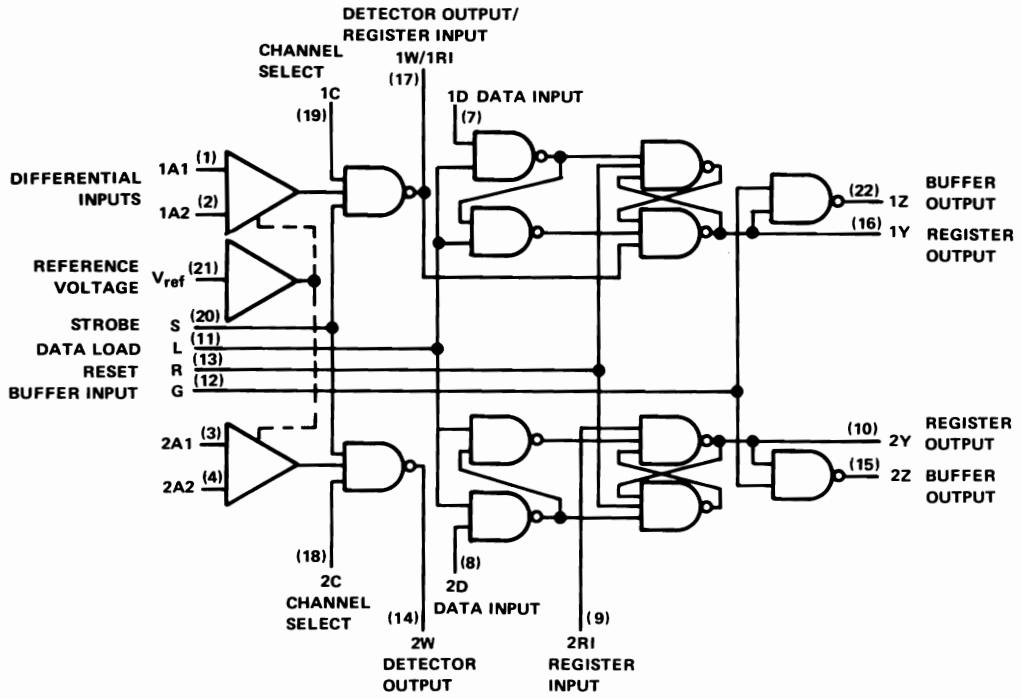


Figure 9.99. SN75236/SN75237 Functional Block Diagram

Figure 9.101 illustrates an application of the SN75236 with the two sense channels connected in an AND configuration. In this combination there is a direct output from the data register, and a buffered output furnishes the write drive input. The application also provides a spare register and buffer output for use elsewhere in the system.

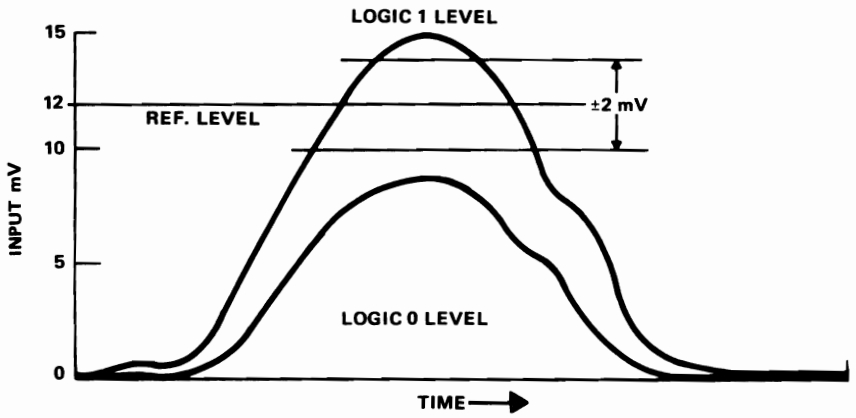


Figure 9.100. SN75236 Sensitivity Matches High-Speed Cores

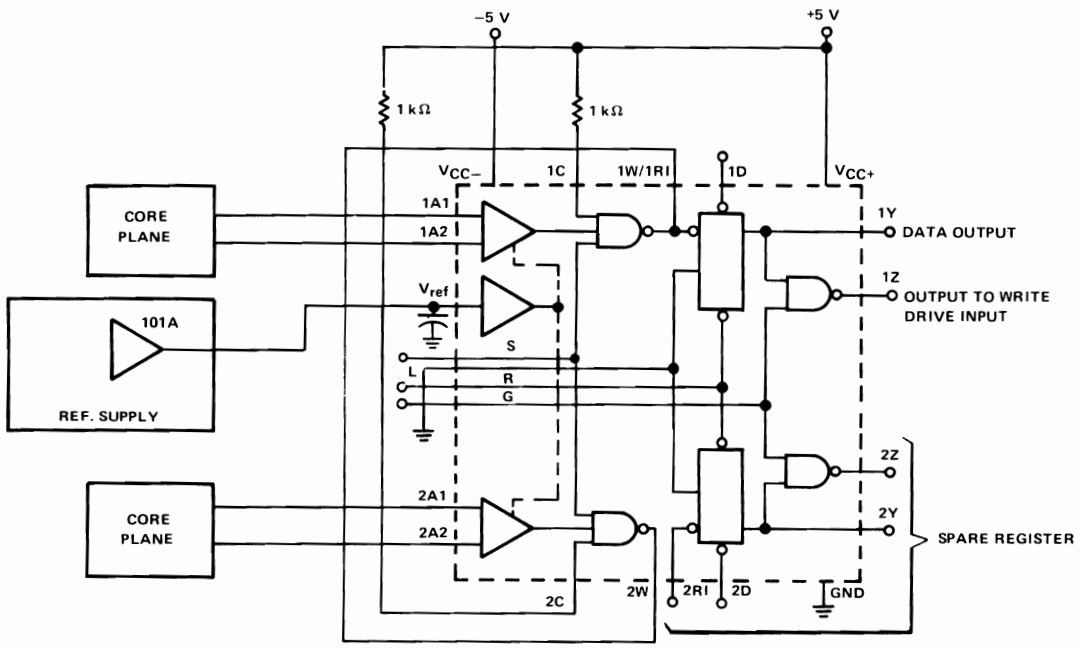


Figure 9.101. The Two Sense Channels of an SN75236 Connected in an AND Configuration

Figure 9.102 shows the basic two-channel application with both outputs driving their respective data registers. Individual channel select strobes are used, and external data changes may be fed into the system at the respective W/R terminals.

Use of an SN52101A in the reference-supply circuit furnishes stable threshold voltage over the full temperature range; a 1.35-volt mercury cell provides the input to the SN52101A amplifier. Because of the low input bias current required by the SN52101A, the reference cell should serve for its normal shelf life. An output of 2.1 volts from the reference supply yields a 7-mV threshold for the sense amplifiers.

For best performance of the SN75236 or SN75237 the reference input terminal should be bypassed as close to the package as possible to prevent feedback. Although originally designed as the SN55236, with full military temperature operating characteristics, the SN75236 and SN75237 devices are desirable for industrial applications where speed, power consumption, compactness, and reliability are important.

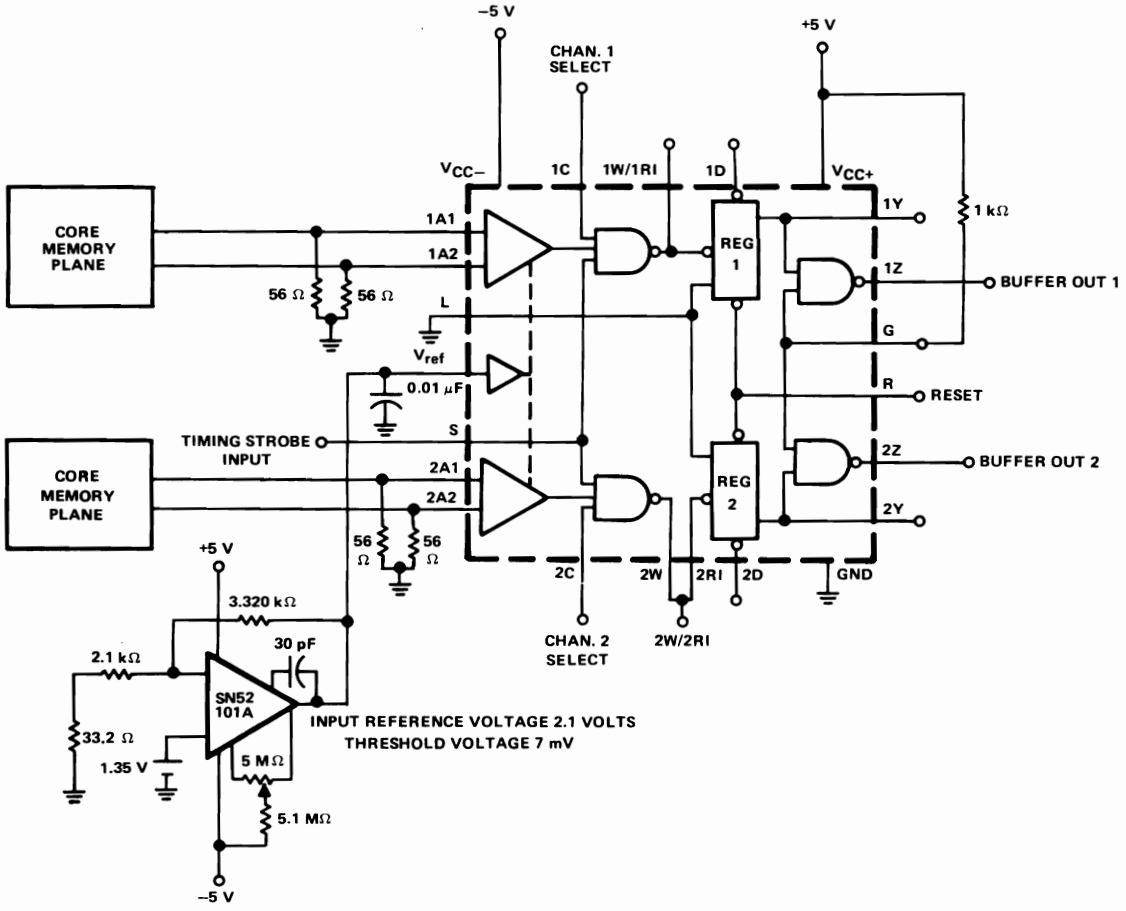


Figure 9.102. Basic Two-Channel Application of SN75236

Other Applications — The SN7520 series devices were designed specifically for sensing core memories. Their capability to detect signal amplitudes regardless of polarity makes impractical their use as basic comparators; but they are useful for a few applications other than memory sensing. One such example is their use (Figure 9.103) as zero voltage detectors. The SN75234 provides a logic 1 output except during the zero voltage crossing (or no input).

In this installation a resistor divider network between the positive 5-volt supply and ground provides a well-filtered 40-mV reference source setting the input threshold level.

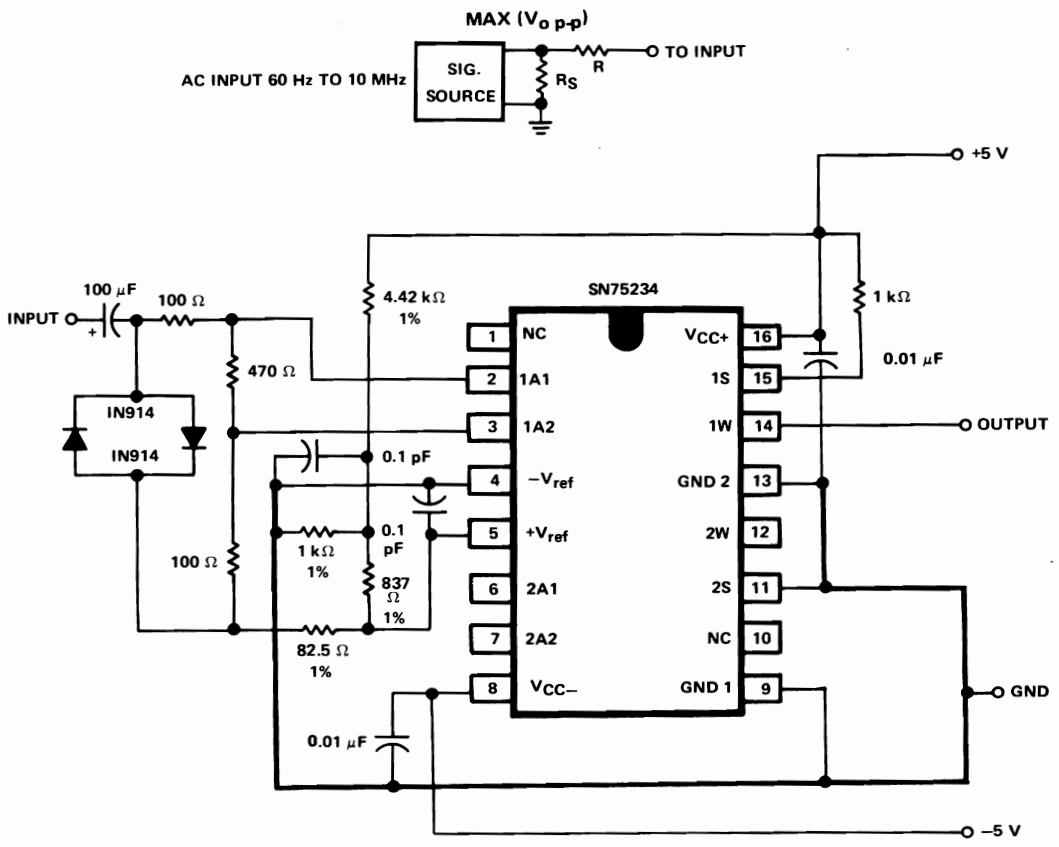


Figure 9.103. Zero Voltage Detector

To prevent excessive loading of the signal source and avoid excessive input voltage levels, a series dropping resistor is recommended. The value of R is easily calculated from the equation:

$$R = \frac{V_{o\ p\text{-}p} - 2 \text{ volts}}{3.5 \text{ mA}}$$

For input voltages greater than 0.8 volt p-p, the value of R should be limited to values equal to or greater than 56 ohms. This prevents overdriving the input clamp diodes and provides additional load impedance to the signal source.

10

Line Transmission Circuits

10.1 GENERAL REQUIREMENTS

As applications of memory systems and various types of logic equipment have increased, so has the need for communications between them. Data-transmission circuits, i.e., line drivers and line receivers, are used for communicating logic data between such equipment as main frame central computers and remote stations, printers, modems, optical displays, etc.

Some of the basic requirements for a good transmission system are:

- High-speed capability ($\geqslant$ 10 MHz† in most cases)
- Popular power supplies
- Logic compatibility
- Good receiver input sensitivity
- Stability over temperature and power-supply excursions
- Adequate noise rejection
- Drivers capable of driving low-impedance transmission lines
- Data-bus or party-line capability
- Economical packaging

Basic theory of data-transmission circuits, types of circuits available, and various applications of these circuits are discussed in the following sections.

10.2 SINGLE-ENDED TRANSMISSION SYSTEMS

10.2.1 Types of Lines

Single Wire and Ground Plane — A single-wire connection between a data driver and receiver is satisfactory where environment and circuit conditions are right. A

†May also be expressed in data frequency (bits per second), equal to two times the frequency in hertz.

typical application for a single-wire interconnect (Figure 10.1) is in logic systems where the output of one gate drives the input of another located on the same or an adjacent PC board. Distances between drivers and receivers must be short, with the system relatively free from switching transients or similar electrical noise, depending on the system speed. Distance limit for reliable communication is approximately three to six inches for most applications.

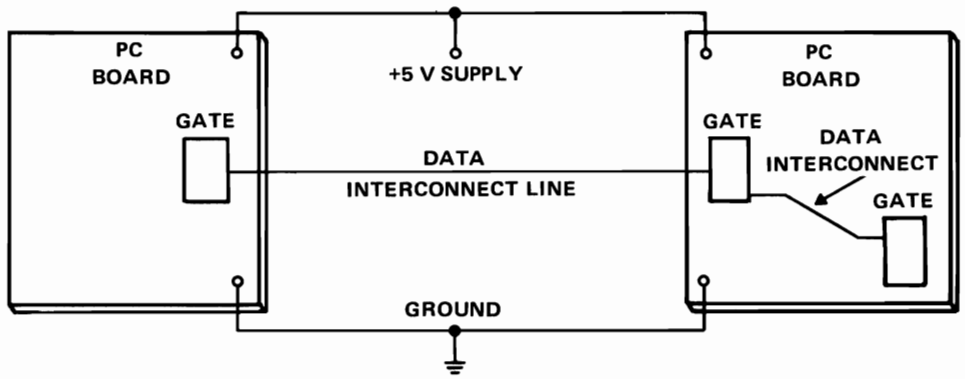


Figure 10.1. Single Wire and Ground Plane

Double Wire — Untwisted-dual-wire interconnects (see Figure 10.2) are seldom used. The second wire is generally a ground, and application limitations are similar to those for single wires.

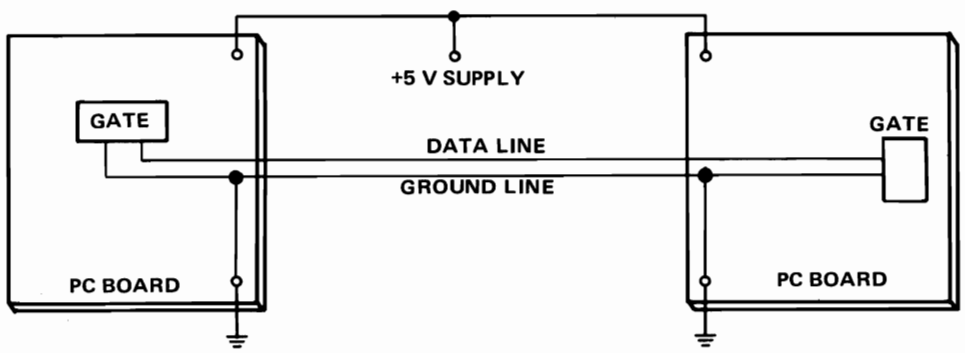


Figure 10.2. Double Wire

Twisted Pair — Two wires uniformly twisted (Figure 10.3) have a definite impedance characteristic, allowing proper termination of the line, and making possible both higher-speed and longer-line data transmission. System noise pickup is reduced through mutual coupling of the two wires.

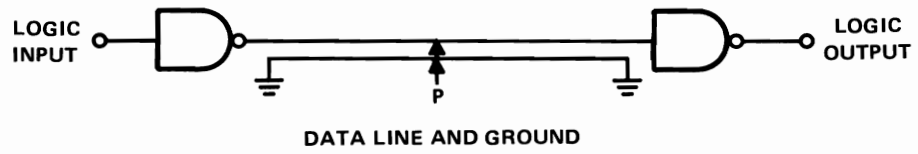


Figure 10.3. Twisted-Pair Line

Coaxial — Popular 50- to 200-ohm coaxial cables (Figure 10.4) offer the best transmission-line characteristics for single-ended transmission systems. They provide uniform characteristic impedances, relatively low loss, and good shielding against inductive interference.

Figure 10.4. Coaxial Line

10.2.2 Drivers

Logic Gates — For the author's convenience, TTL logic systems are used exclusively in the following discussions. However, other forms of logic should not be dismissed as inadaptable to the circuit configurations presented.

Probably the most common single-ended application is the transmission of data from one logic gate directly to another. Standard TTL gates can operate at frequencies up to 20 MHz. However, interconnects must be short (a few inches), and special care be taken to assure adequate noise margin and minimum line reflections. The higher speeds of ECL and Schottky TTL gates place even more emphasis on properly terminated, well-shielded lines.

The best type of transmission line for single-ended, high-speed applications, where line lengths exceed six inches, is coaxial. Coax lines provide uniformity and shielding against noise, but have high capacitive characteristics. Assuming a 2.4-volt minimum logic 1 level, 50-ohm coax requires 48-mA output drive capability, which can be supplied only by high-current TTL gates. However, typical TTL gates, with 16-mA sinking and driving capability at 2.4 volts, necessitate use of 150-ohm coax.

Another factor to consider in the use of gates is the environmental noise level. It can be seen in Figure 10.5 that negative-going noise peaks greater than 0.4 volt and positive-going noise peaks greater than 0.4 volt may result in false triggering. The guaranteed noise margin is therefore ±0.4 volt when using standard TTL gates.

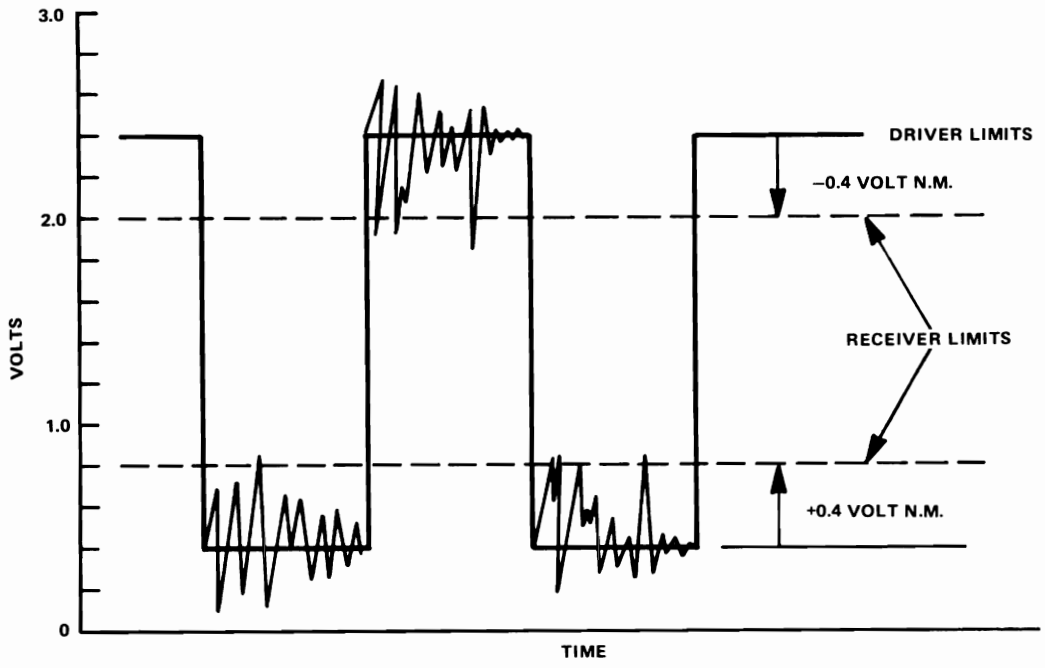


Figure 10.5. TTL Gate Noise Margins

Types of Line Drivers — Voltage-mode drivers are used in single-ended systems to provide the required levels for good noise immunity and signal reception. Voltage drivers are active switches used to transfer a voltage from a supply line to the load directly (Figure 10.6), or to switch the load from ground to allow it to receive the voltage through a low-value resistor (Figure 10.7). The drive current required is determined by the load impedance. It is desirable to drive a line with devices providing up to 100 mA drive at TTL voltage levels and TTL speeds. Single-ended drivers having this capability are of three basic types — active pull-up, active pull-down, and totem pole, as shown in Figures 10.6, 10.7, and 10.8.

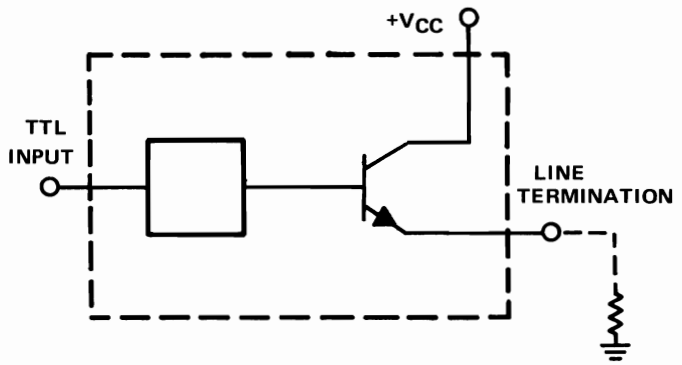


Figure 10.6. Active Pull-Up Configuration

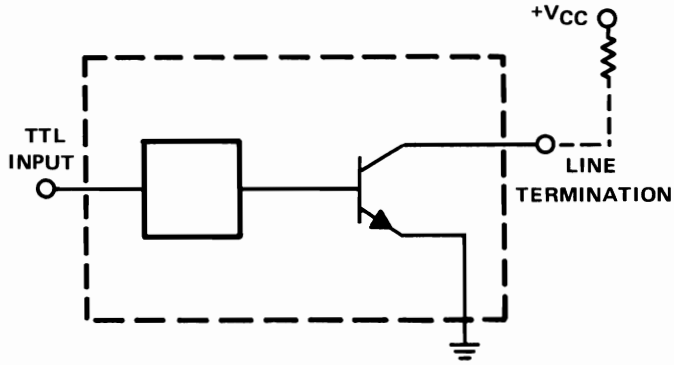


Figure 10.7. Active Pull-Down Configuration

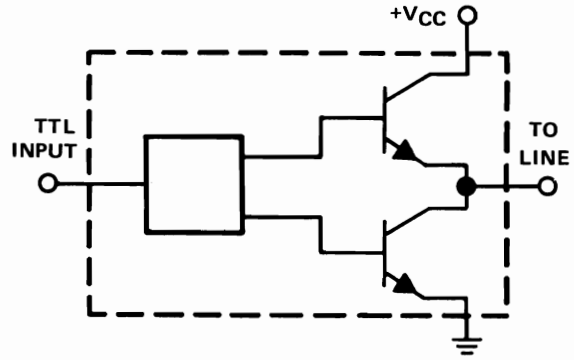


Figure 10.8. Totem-Pole Configuration

Active-Pull-Up Line Drivers — The SN75450B peripheral drivers may be used as dual-channel, active-pull-up line drivers. The following circuits show two typical applications.

The basic circuit approach for dual-channel line drivers is shown in Figure 10.9. Output voltages are about 2.5 volts typically. Since the gate output could be as low as 2.4 volts, a V_{BE} of about 0.8 volt gives an output to the line as low as 1.6 volts.

Line impedance (Z_O) as low as 50 ohms can be easily driven by the SN75450B, as its current-handling capacity is 300 mA per transistor. Propagation delays are less than 18 nanoseconds. Output pulse rise time is under 20 nanoseconds, but fall time is dependent on the RC characteristics resulting from line capacitance and termination impedances. For example, a 100-ohm terminated transmission line having 1000 pF capacitance would result in a fall time of about 0.2 μs.

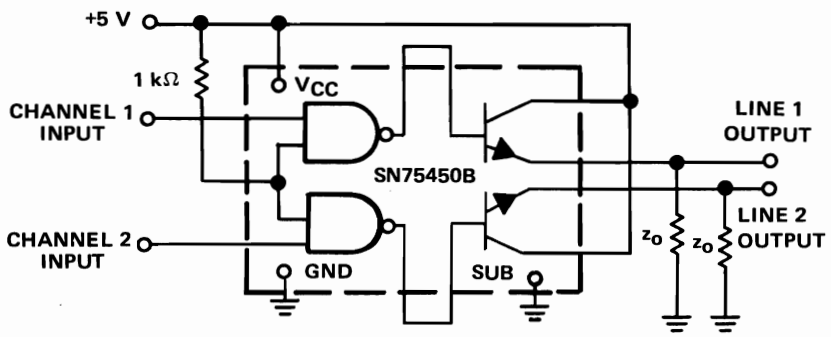


Figure 10.9. Basic Active-Pull-Up Line Driver

To aid the gate drive, and thereby achieve higher output drive voltages, the circuit shown in Figure 10.10 may be used. Low-value base pull-up resistors give more base drive and output voltage. During the time the gate output is a logic 0 the gate must sink current coming through this resistor, thus limiting its minimum value. As with a standard gate, a maximum sink capability of 16 mA is used in calculating the minimum resistor value. Assuming a worst-case supply voltage of 5.5 volts and a low gate output saturation of 0.2 volt (neglecting base-current leakage), the minimum resistance will be 5.3 V/16 mA, or about 331 ohms. A value of 390 ohms or greater is normally specified. When driving typical 100-ohm twisted-pair transmission lines, the results are as follows:

Logic 1 output voltage — 3.3 volts typical
Logic 0 output voltage — 0 volt typical

+5 volts, and may be as high as device output ratings will allow. For example, in this circuit V_{CC2} could be +12 volts. Care must be taken to assure that the driver selected is capable of driving a properly terminated line at the selected V_{CC2} level. If the line is 50-ohm coax, sink current will be a minimum of (V_{CC2}/Z_o), or 240 mA. Additional surge current will be drawn during turn-on to charge the line capacitance.

Although most TTL gates have relatively low output-current capability, proper selection of supply voltage and the line allows them to be used for driving relatively short lines. For example, the SN74H40, with 60-mA capability, could be used as shown in Figure 10.12.

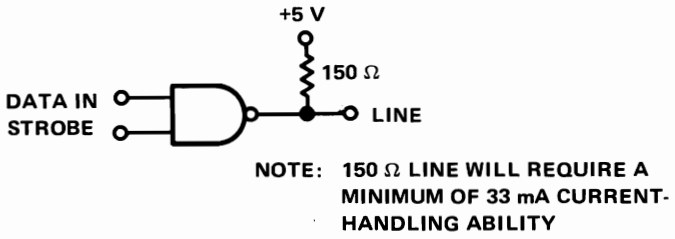


Figure 10.12. TTL Gate Line Driver

Totem-Pole Line Drivers — The totem pole offers the advantage of having both active pull-up and active pull-down, thus assuring higher switching speeds and a continuous low-impedance output. TTL gates have totem-pole outputs and are satisfactory in short-line applications, as previously mentioned. The low-output-drive problems associated with standard TTL gates are solved by use of the SN75450B wired as a totem-pole driver (see Figure 10.13). This basic circuit may be used to

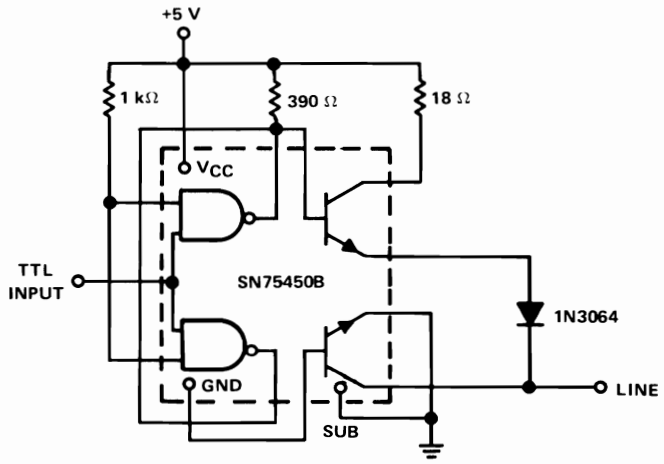


Figure 10.13. SN75450B Totem-Pole Line Driver

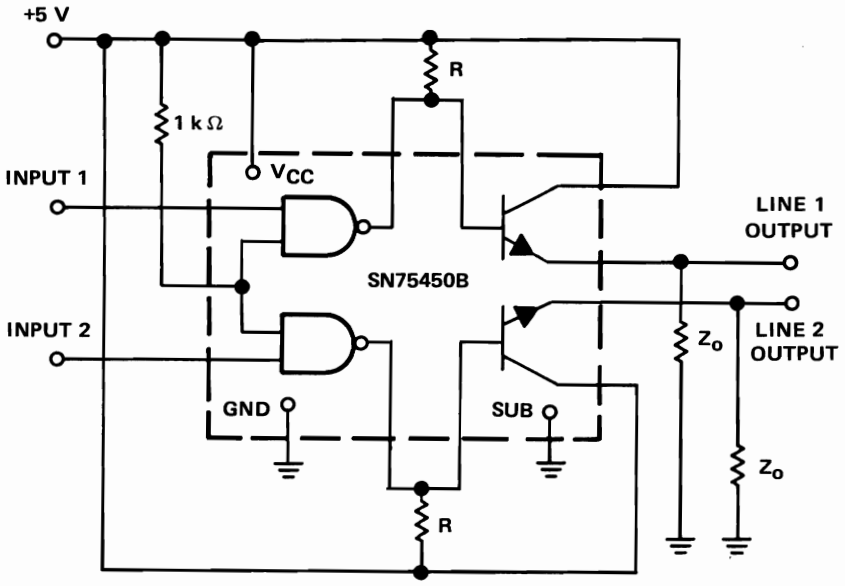


Figure 10.10. Base Pull-Up Resistors for Higher Output Voltage

Active-Pull-Down Line Drivers — Several types of ICs may be used as active-pull-down line drivers. A few examples are: open-collector gates, SN75451B series peripheral drivers, seven-segment readout drivers with open collectors, memory driver circuits, and the SN75138 quad transceiver.

The basic circuit, using an SN75451B peripheral driver as a dual-channel line driver, is shown in Figure 10.11. In this configuration V_{CC2} is not limited to

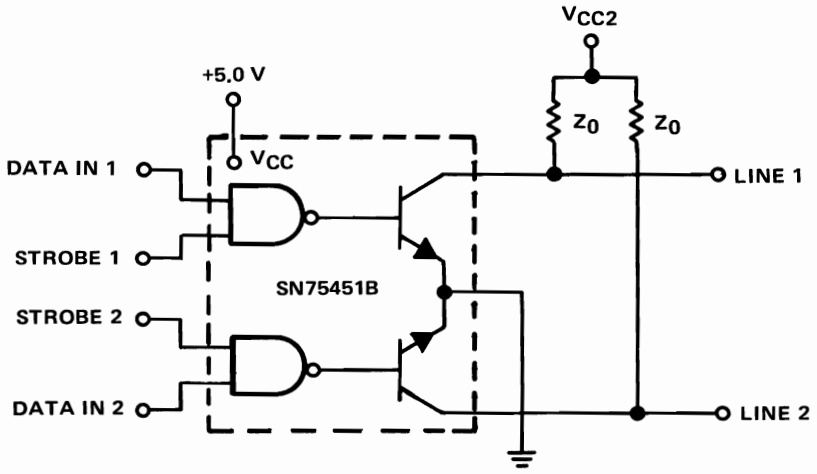


Figure 10.11. Basic Active-Pull-Down Line Driver

drive single-ended lines at frequencies up to 5 MHz at TTL levels, and to drive lines with impedances as low as 25 ohms.

Line drivers built to meet EIA RS-232C specifications have a type of totem-pole output allowing them to swing both positive and negative levels at their outputs. Some examples are:

Circuit Type	Manufacturer
SN75188	Texas Instruments
MC1488	Motorola
9616	Fairchild
8T15	Signetics
SN75150	Texas Instruments

Numerous circuits utilizing totem-pole output configurations have been designed specifically to drive transmission lines, many of these being basically TTL-type gates with 40- to 80-mA current-handling capability. Typical of these types are the following dual line drivers: SN75113, SN75114, and SN75183. Several variations of totem-pole output circuits are used, but all of these have basically the same voltage-type drive which is recommended for lines of medium lengths.

Another type of totem-pole driver is the SN75361A series MOS drivers. The SN75361A, SN75363, SN75365, SN75367, and SN75368 are all capable of driving relatively long single-ended lines. With this type of device the output-source voltage need not be limited to +5 volts. It may be increased as desired to as high as 24 volts, provided load impedances do not require excessive drive current (beyond the 160-mA output capability).

Advantages and Disadvantages of Single-Ended Drivers

Advantages

- Simplicity: Single-ended voltage-mode drivers are basic switching circuits, easy to understand and comparable to mechanically switching voltages on and off a line.
- Low Cost: Uncomplicated circuit design generally results in low product costs.
- Single Power Supply: Circuit construction allows easy operation from a single supply voltage, although EIA RS-232-C circuits require two supplies.
- TTL Compatible: Circuits may be TTL or DTL compatible at both inputs and outputs.

Disadvantages

- Poor Noise Immunity: A noisy environment presents a problem for single-ended transmission. Care must be taken to assure that induced noise or unwanted signals do not interfere with the desired signal. Use of shielded transmission lines or coaxial cable will help in this respect. The resulting noise margins will be related to driver output limits as well as receiver input limits, as previously shown.
- Expensive Coax: Under typical environmental conditions coaxial cable will be required to prevent noise interference.
- High Drive Power Required: This is particularly true when driving low-impedance coax lines. A typical 3-volt logic level output to a 50-ohm line will require 60-mA drive capability.
- High Line Losses: Due to the large IR drops, line lengths will be limited because of low noise margins. Some improvement may be obtained by using higher characteristic impedance transmission lines to lower the drive-current requirements.

10.2.3 Receivers

TTL Gates — Regular TTL gates may be used as receivers. Although this practice is not recommended for applications other than short lines (several inches), careful selection of devices and lines may allow transmission over several feet.

Schmitt Triggers — As shown in Figure 10.5 the noise margin of standard TTL gates is ±0.4 volt. However, this value may be improved to allow safer transmission

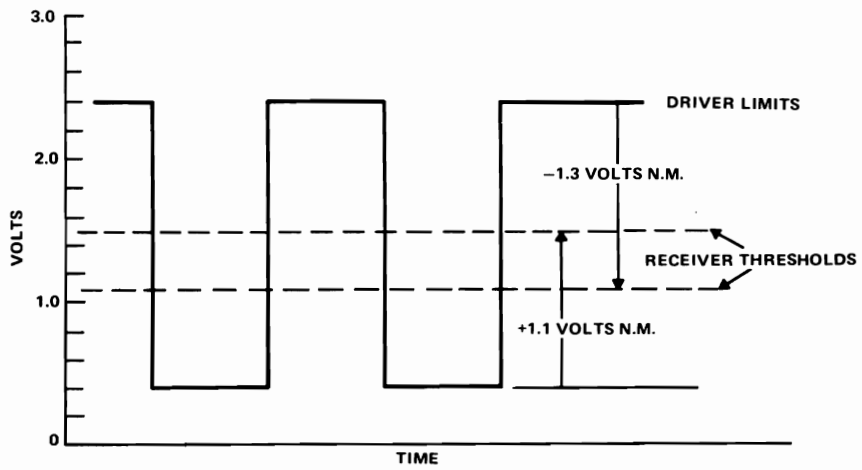


Figure 10.14. SN74H40 Driver to SN7413 Receiver Noise Margins

of data. An example is the use of an SN74H40 buffer as a driver and the SN7413 Schmitt trigger as a receiver. Input hysteresis characteristics of the SN7413 improve the noise margin, as may be seen in Figure 10.14. The noise margins of +1.1 volts and −1.3 volts under worst-case conditions are about three times better than those of standard TTL gates.

For connections between PC boards in a fairly large system this combination of driver and receiver will provide enough noise margin for satisfactory operation at frequencies up to 10 MHz. A good-quality 50-ohm coax cable could be used as the transmission line, for the SN74H40 has adequate drive capability.

Special Single-Ended Receivers with Hysteresis — Some receivers have been developed especially for receiving data transmitted in single-ended applications. Several device types are designed to meet the EIA RS-232 specification for receivers used with modem systems. Some examples of these units are:

Device No.	Description	Manufacturer
CM1162	Quad receiver (RS-232)	Cermetek
MC1489	Quad receiver (RS-232)	Motorola
DM8822	Dual receiver (RS-232)	National
SN75154	Quad receiver (RS-232)	Texas Instruments
SN75152	Dual receiver (RS-232)	Texas Instruments
SN75122	Triple receiver	Texas Instruments
SN75189/189A	Quad receiver (RS-232)	Texas Instruments
SN75124	Triple receiver	Texas Instruments

By using an SN75451B as the driver and an SN75154 as the receiver in the configuration shown in Figure 10.15, noise margins of ±1.8 volts may be realized (see Figure 10.16).

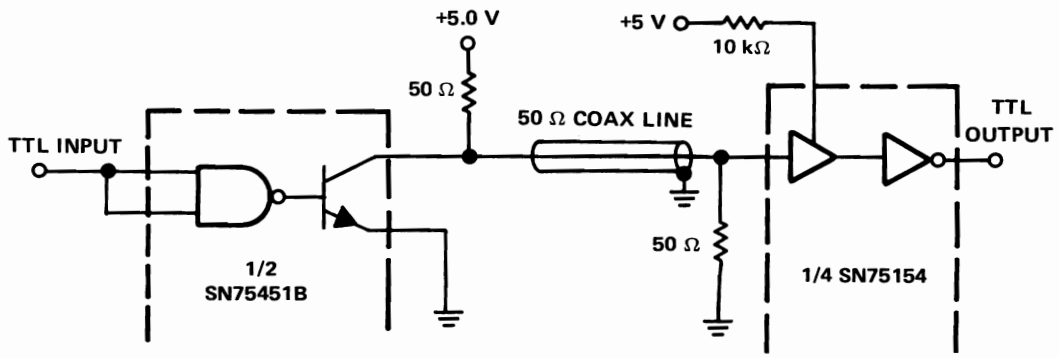


Figure 10.15. SN75451B Driver with SN75154 Receiver

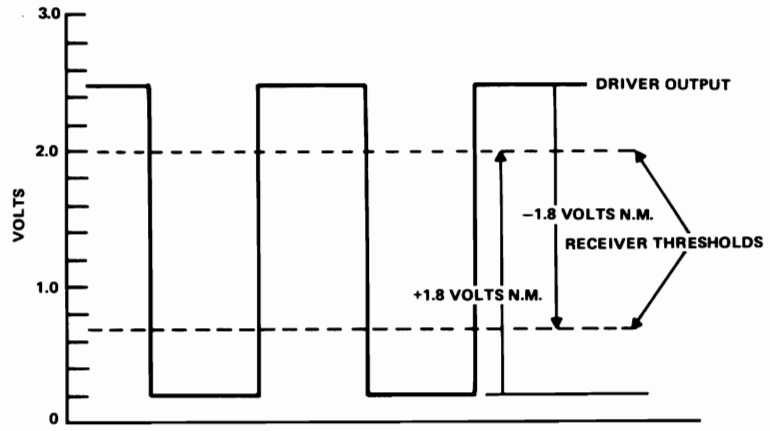


Figure 10.16. SN75451B Driver to SN75154 Receiver Noise Margins

SN75138 Quad Transceivers — The SN75138 quad bus transceiver was designed for two-way data communication over single-ended transmission lines. Each of the four identical channels consists of a driver with TTL inputs and a receiver with TTL output. The driver output, of the open-collector type, is designed to handle loads of up to 100 milliamperes (50 ohms to 5 volts). The receiver input is internally connected to the driver output, and has a high impedance to minimize loading of the transmission line. Because of the high driver output current and the high receiver input impedance, a large number (typically hundreds) of transceivers may be connected to a single data bus. Figure 10.17 shows such a system.

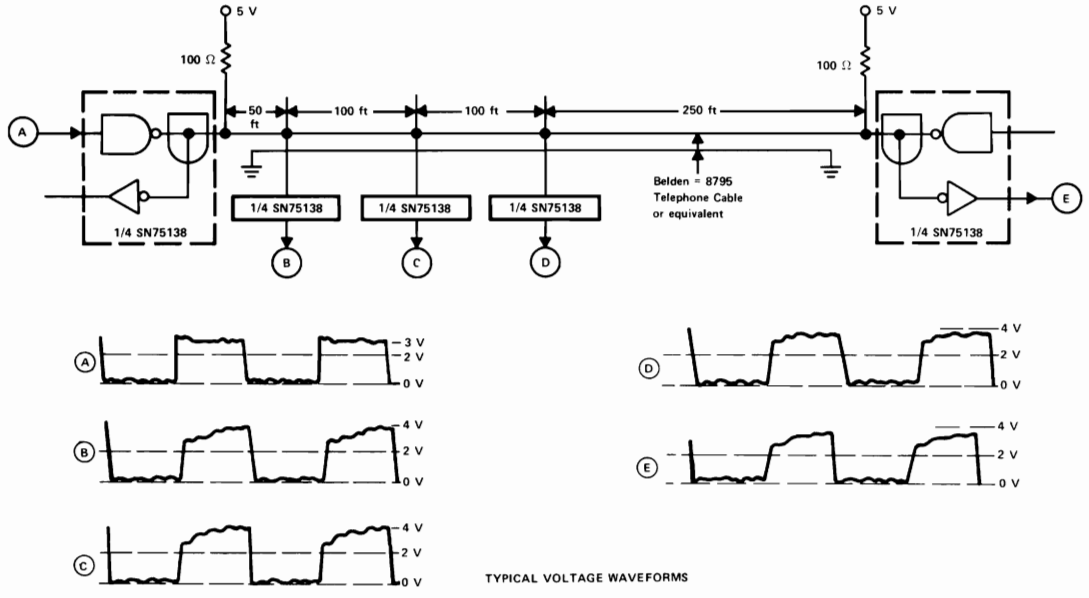


Figure 10.17. Party-line Communication on 500 Feet of Twisted Pair at 1 MHz

Another basic application for which the SN75138 is particularly suited is multichannel, bidirectional data transmission. Many memory applications require this type of parallel transmission of data between two locations. The circuit in Figure 10.18 shows how four channels of data may be transmitted or received using only one device package at each location. With typical 100-ohm transmission lines 100-ohm terminating resistors would be used, connected between the line and +5 volts as shown. Resulting signal levels on the lines are typically 0.3 volt for a logic 0 and 4.5 volts for a logic 1. In most applications of this type the receiver, with a typical threshold of 2.5 volts, will have noise margins of ± 2 volts or greater.

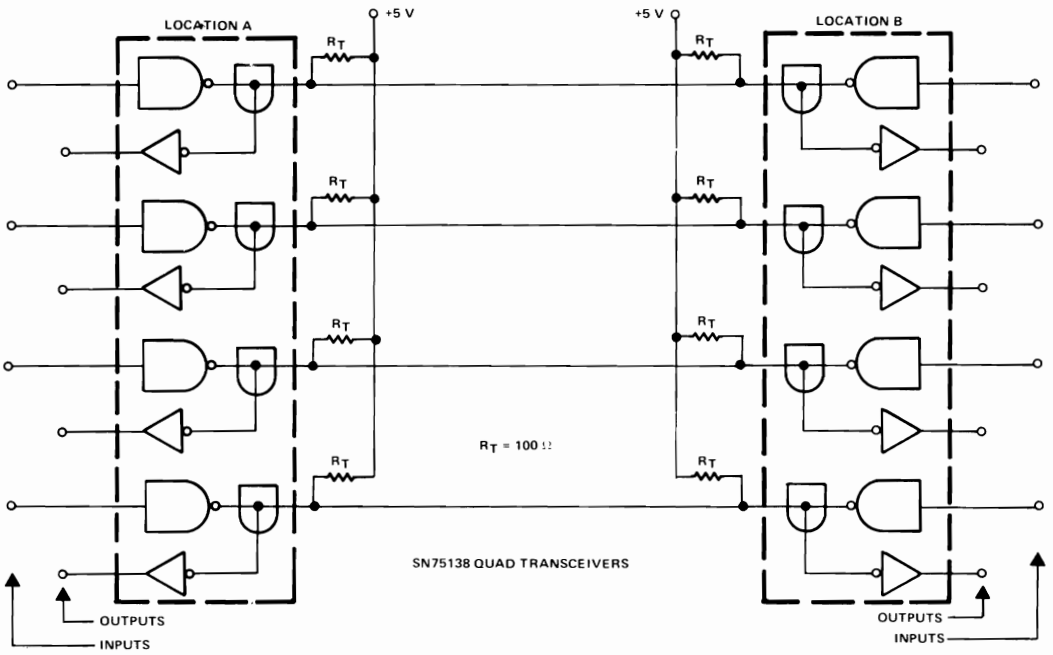


Figure 10.18. Multi-channel (Parallel) Data Transmission

10.3 BALANCED-LINE TRANSMISSION SYSTEMS

10.3.1 Types of Lines

Dual Coaxial Cable — Two-conductor coaxial cable, probably the best quality of wire used for balanced-line transmission, is selected primarily for applications

involving high environmental noise levels. Its advantages are noise immunity, extreme uniformity, and ability to handle relatively high frequency signals. Disadvantages are its cost, weight, and relatively high capacitance per foot, requiring more drive power at higher frequencies.

Dual Wire — Two loose wires may be used where frequencies are low and distances short (< 3 feet). This, the least expensive means of interconnection, could take the form of two conducting strips on a PC board. However, it is normally used in limited applications because of its nonuniform impedance characteristics.

Shielded Twisted-Pair Line — As mentioned previously, shielded twisted-pair lines, while offering some protection from noise pickup, do not generally have uniform impedance characteristics and are very capacitive. They are economical for short-line applications that involve severe noise conditions.

Twisted-Pair Line — There are two types of twisted-pair lines: hand-twisted or loosely twisted wire often used in audio applications, and the uniformly twisted pair with specified line-impedance characteristics. The latter is recommended for balanced-line transmission. Its uniformity, low impedance, low capacitance, and moderate cost make it the most popular high-speed data-transmission line for balanced systems, which depend on common-mode characteristics rather than shielding to eliminate noise.

10.3.2 Advantages of Balanced-Line Systems

Low Cost: In most applications inexpensive twisted-pair line can be used instead of coaxial line.

Low Impedance: Twisted-pair lines have impedances from about 50 to 200 ohms, depending on wire size, insulation, and twisting characteristics. This low impedance, when properly terminated, reduces noise pickup.

Uniform Impedance: Because of the construction of the line the impedance is uniform throughout its length, thus providing good high-frequency characteristics for long-line applications as well as for relatively short interconnections.

Common-Mode Characteristics: Noise, system transients, and unwanted signals picked up on the lines are common-mode signals (see Figure 10.19): the signal picked up on one line is equal in amplitude and phase to that picked up on the other. If the receiver has a differential input it will not accept or amplify the

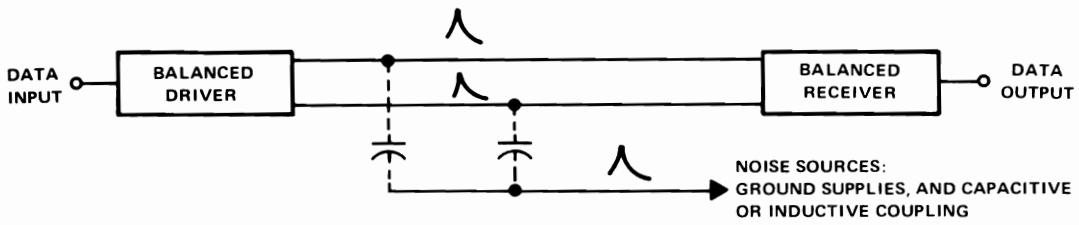


Figure 10.19. Noise in a Balanced-Line System

common-mode signals, and thus noise rejection becomes a characteristic of the common-mode rejection capability of the receiver. The induced voltages tend to cancel, and what is not canceled is common mode and is therefore rejected by the receiver. In an extremely high noise environment some differential noise may be generated. Shifting the threshold with hysteresis provides differential noise rejection at the expense of differential input sensitivity. Without hysteresis only the common-mode signals are rejected.

10.3.3 Balanced (Differential) Line Drivers

High-Current Gates as Voltage Drivers — As in single-ended drive applications, special high-current gates may be used as drivers. (For basic diagram see Figure 10.20.) This configuration may be built up from discrete gates like the SN74H40, or may be units that are designed specifically for this type of operation. The following drivers have this type of differential drive capability: SN75113, SN75114, SN75183.

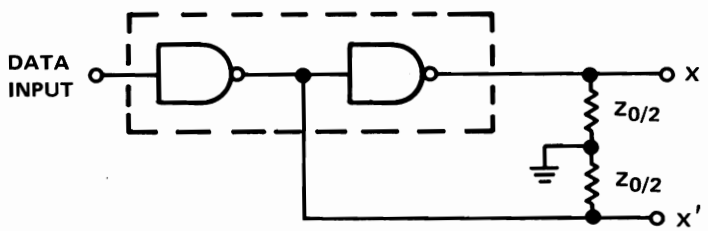


Figure 10.20. Basic Differential (Balanced) Line Driver

Peripheral Drivers as Voltage Drivers — Peripheral drivers are designed to interface between TTL and relays, lamps, transmission lines, etc. Generally of high-current-handling ability (300 to 500 mA), they may be connected to drive balanced as well as single-ended lines. Figure 10.21 is one example of a balanced-driver configuration using a peripheral driver.

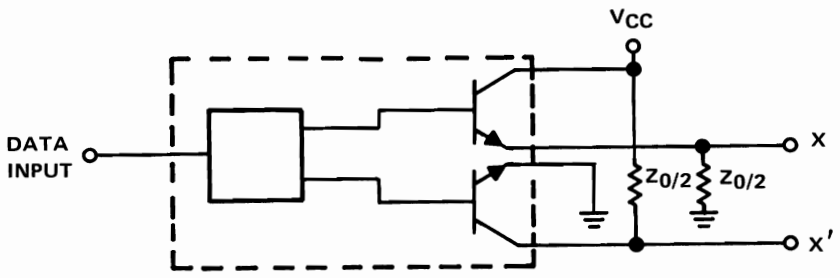


Figure 10.21. Peripheral Driver as a Balanced-Line Driver

Current Drivers — Balanced-line drivers with constant-current output capability are designed for driving low-impedance lines without the numerous disadvantages of voltage-mode transmission. The driver's basic function, as shown in Figure 10.22, is to control a differential output circuit that is fed by a constant-current generator. Output currents are in the range of 5 to 15 mA, and are constant. Line terminations may be to ground, as shown, to $+V_{CC}$, or to some point in between.

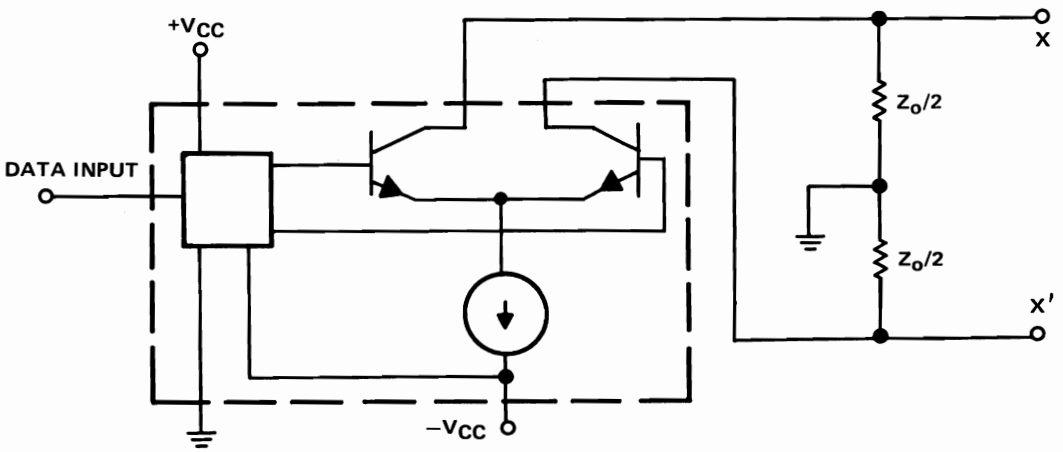


Figure 10.22. Constant-Current Balanced-Line Driver (e.g., SN75110)

10.3.4 Balanced (Differential) Line Receivers

Receivers must have differential inputs to benefit from the common-mode characteristics of balanced-line data transmission. The outputs of the receivers are generally compatible with TTL logic levels.

Single-Supply Differential Line Receivers — Line receivers designed to operate from one power supply work well but have limitations. Operation from a single supply results in the sacrifice of either common-mode range or sensitivity; in most cases sensitivity is reduced. Also, party-line or bus-line applications are not recommended, because of the resulting low input impedance.

Dual-Supply Differential Line Receivers — Basically this receiver is a high-input-impedance differential amplifier followed by a strobe-controlled gate amplifier with standard TTL output, as shown in Figure 10.23. Examples of differential line receivers are:

SN75107A	SN75208
SN75108A	SN75115
SN75207	SN75182

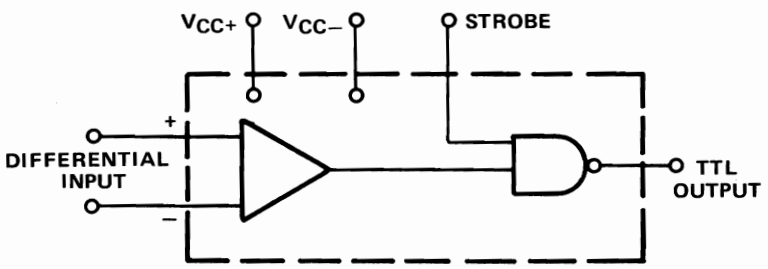


Figure 10.23. Dual-Supply Differential Line Receiver

10.4 APPLICATIONS OF LINE DRIVERS AND RECEIVERS

10.4.1 Comparison of Data-Transmission Systems

Before considering specific applications it is helpful to note the characteristics of the various types of line drivers and receivers.

Gate Single-Ended Drivers and Receivers
(SN74H40, SN7413, etc.)

Advantages	Disadvantages
Capable of high speeds (> 10 MHz)	Short lines only (< 3 feet)
TTL compatible	Poor noise immunity
Single power supply	No common-mode rejection
Popular supply voltage	Problems in driving low-Z lines
	Poor receiver sensitivity
	Little party-line capability

Other Single-Ended Voltage Drivers and Receivers
(SN75121, SN75123, SN75122, SN75124, SN75138, SN75154, SN75189, SN75450, SN75361A)

Advantages	Disadvantages
Capable of high speeds (> 10 MHz)	High power consumption
TTL compatible	No common-mode rejection
High drive-power capability	Subject to noise spikes
Single-supply voltage	Poor receiver sensitivity
Good noise immunity in some cases	Little or no party-line capability

Single-Supply Balanced-Line Drivers and Receivers
(SN75113, SN75114, SN75183, SN75115, SN75182, SN75116, SN75117)

Advantages	Disadvantages
Capable of speeds to 10 MHz	Driver slewing
TTL compatible	High power consumption
Good common-mode rejection	Frequency somewhat limited
Single power supply	High line losses
	Limited party-line capability
	Poor receiver sensitivity

Dual-Supply Balanced-Line Receivers and Current-Mode Drivers
(SN75107A, SN75108A, SN75109, SN75110, SN75207, SN75208)

Advantages	Disadvantages
Capable of high speeds (> 10 MHz)	Dual power supply
TTL compatible	Require balanced lines
Popular supply voltages	Moderate common-mode capability
Can drive low-Z lines easily	Stable over temperature

Advantages (Cont.)

High common-mode rejection	External strobe controls
Not susceptible to system noise	Good for party-line operation
Low driver power requirements	High driver output Z
Drive long lines (> 5K feet)	High receiver input Z
Good receiver sensitivity	Strobes TTL compatible

10.4.2 Line Characteristics

In determining the type of line to be used, some information on line characteristics is helpful. In particular, twisted-pair lines and coax lines will be considered.

Twisted-Pair Lines — Twisted-pair lines are available in an infinite number of configurations. Variations in wire size, insulation, and number of twists per foot affect the transmission characteristics.

Most wire manufacturers offer two basic types of machine-twisted wire: 1) Loosely twisted wire which usually does not have a specified impedance, and is often used as audio wire. 2) Twisted pairs built for use as telephone lines and data-transmission lines. The characteristic impedance of this wire is almost always specified.

Basic characteristics of twisted-pair lines commonly used for data tramsmission are listed in Table 10.1. The attenuation characteristic shown in Figure 10.24 is typical of this type of line.

Table 10.1. Characteristics of Twisted-Pair Lines

Description	Impedance (Ω)	Wire	Capacitance Per Foot (pF)	Manufacturer	Mfg. No.
Shielded Twisted Pair	100	#20 7 X 28	15	Belden	8227
Twisted Pair Vinyl Insulation	110	#22 Solid	12	Belden	8481
Twisted Pair Plastic Jacket	110	#22 Solid	25	Alpha	1793
Twisted Pair Plastic Insulation	100	#20 10 X 30	15	Alpha	1918
Twisted Pair Vinyl Insulation	100	#22 Solid	15	Belden	8795

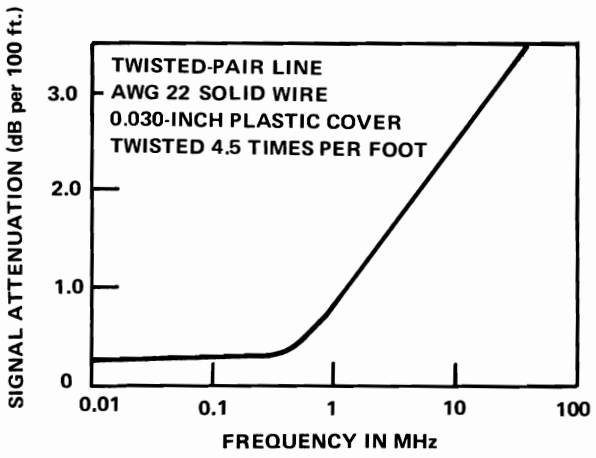


Figure 10.24. Attenuation of Typical Twisted-Pair Line

Coax Lines — Coax transmission lines provide good isolation from radiated noise and crosstalk. Although generally used for single-ended transmission, dual coax cables may be employed for balanced-line transmission. Impedance characteristics are uniform, and impedances in the range of 50 to 200 ohms are readily available.

Characteristics of typical RG/U transmission-line cables are listed in Table 10.2. Many wire manufacturers produce RG/U wire to MIL-C-17 specifications; thus it has uniform and standard characteristics. Signal attenuation in coax cables is frequency dependent, as shown in Figure 10.25.

Table 10.2. Characteristics of Typical Coaxial Lines

Type	Wire	Nominal Impedance (Ω)	Nominal Capacitance per Foot (pF)	Attenuation per 100 ft. f ≈ 10 MHz (dB)
RG-58A/U	#21 19 X 33	50	29.5	1.6
RG-59B/U	0.023 Solid Copper	75	20.5	1.1
RG-63B/U	0.025 Solid Copper	125	10	0.6
RG-22B/U (Dual)	Two 7 X 0.0152	95	16	1.6

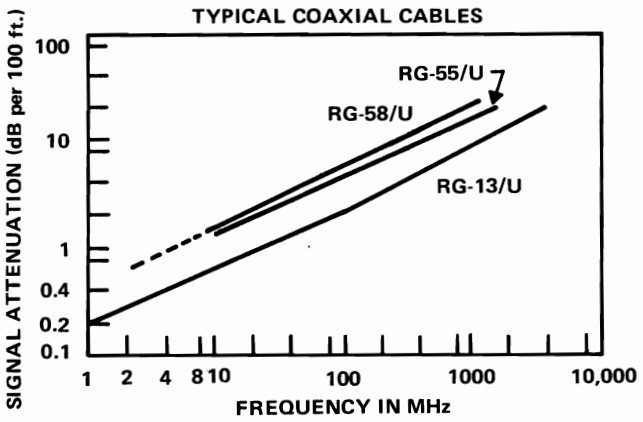


Figure 10.25. Attenuation of Typical Coaxial Cables

10.4.3 Single-Ended Systems

SN74H40 Driver with SN7400 Receiver — This circuit would be used in a cabinet or rack to transmit TTL data short distances ($\leqslant$ 3 feet) between PC boards where environmental conditions are not severe. The circuit is shown in Figure 10.26. The transmission line is adequately terminated at the driving end by the driver itself. The receiving end of the line should be terminated in 50 ohms to minimize line reflections. Frequencies up to 20 MHz can be handled with this system. Noise margins are at least ±0.4 volt. Total system propagation delay from the driver input to receiver output is typically 24 nanoseconds with a three-foot line. The driver accounts for 8.5 nanoseconds, the coax for 4.5 nanoseconds, and the receiver for 11.0 nanoseconds. Coax cables have typical propagation delays of 1.5 nanoseconds per foot.

Line: Due to the presence of other switching or logic circuitry the use of a good coax interconnect is suggested. RG-58A/U coax would be suitable for this application. Its characteristic impedance of 50 ohms is about the same as the output impedance of the SN74H40.

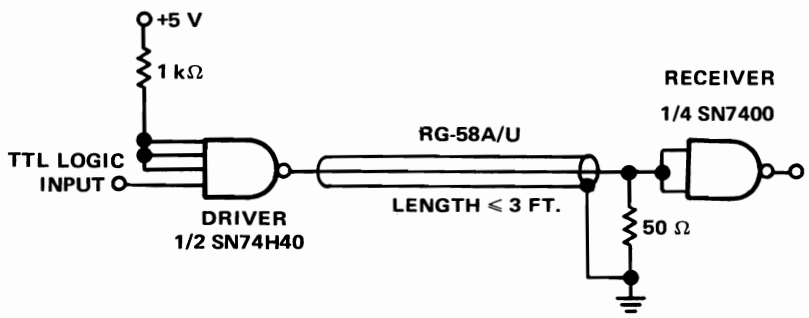


Figure 10.26. SN74H40 Driver with SN7400 Receiver

Driver: A high-current or H-series gate is necessary to adequately drive most coax lines. Such a device is the SN74H40 NAND buffer, providing a 2.5-volt logic 1 level into a 50-ohm transmission line.

Receiver: Any of the SN7400 series gates or other TTL logic gates could be used with comparable results.

SN7407 Hex Buffer as Both Driver and Receiver — A hex buffer with open-collector outputs and good current-handling ability finds many uses in a logic system. Since it is frequently used and each package has six gates, the SN7407 is an obvious candidate for use in line driving and receiving. Again the application would be for short runs of up to three feet, and coax line would be advisable. The circuit is shown in Figure 10.27. Frequencies up to 10 MHz may be transmitted using this system. Resulting noise margins are ±0.4 V, worst case. System propagation delays are around 45 nanoseconds. Although it is not as fast as the previous circuit, the use of a popular device makes this approach convenient for short-line applications.

Line: Due to the current limitations of the SN7407, higher-impedance coax is needed. RG-63B/U, with an impedance of 125 ohms, is a good choice for this application.

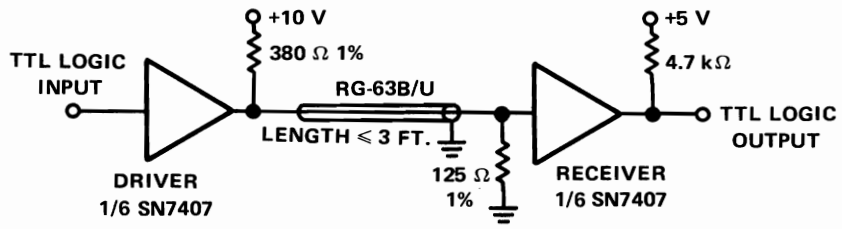


Figure 10.27. SN7407 Driver and Receiver

Pull-Up Resistor Calculations: The driver must have a pull-up resistor (Figure 10.28) large enough to limit the driver sink current to less than 30 mA, while still providing a good logic 1 level to the 125-ohm transmission line. If a logic 1 level of 2.5 volts is to be driven into the 125-ohm line, a minimum of 20 mA is required. Allowing for some supply variations, a maximum sink current of 25 mA

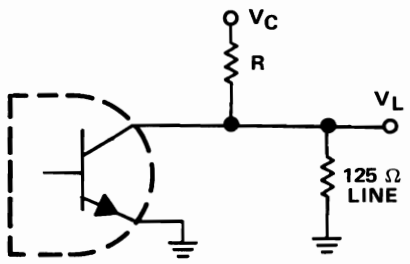


Figure 10.28. Pull-Up Resistor Determination

is chosen. The $V_{CE(sat)}$ at 25 mA is about 0.6 V. Calculations for V_C and R may be made simultaneously from the following equations:

$$R = \frac{V_C - V_{CE\,(sat)}}{I_{Sink(max)}} = \frac{V_C - 0.6\ V}{25\ mA}$$

and

$$R = \frac{V_C - V_L}{I_{Line(min)}} = \frac{V_C - 2.5\ V}{20\ mA}$$

Therefore V_C = 10.1 volts and R = 380 ohms.

Using these values and a power supply of 10 volts ±10%, worst-case conditions would be:

$$V_C = 11\ V \quad I_{sink} = \frac{11\ V - 0.6\ V}{380\ \Omega} + 1.6\ mA$$

$$= 27.4\ mA + 1.6\ mA$$

$$= 29\ mA\ (\text{within 30-mA limit})$$

$$V_C = 9\ V \qquad V_L = \frac{R_L}{R + R_L}\ V_C$$

$$= \frac{125\ \Omega}{505\ \Omega}\ (9\ V)$$

$$= 2.23\ \text{volts (over 2.0 V minimum)}$$

SN74H40 Driver with SN7413 Schmitt Trigger as Receiver — This system has the advantage of operating from a single 5-volt logic-supply voltage level. This circuit would also be used for short-line operation, and some improvement in noise immunity as compared with the SN7407 circuit will be noted. The dual-channel circuit is shown in Figure 10.29. The resulting receiver input voltage levels are about +4.8 volts for the logic 1 level and +0.4 volt for the logic 0 level. Typical input thresholds for the receiver are 0.9 volt negative going and 1.7 volts positive; resulting noise margins are −3.9 volts and +1.3 volts. Typical propagation delays are around 26 nanoseconds plus 1.5 nanoseconds per foot of line. This circuit may be operated at frequencies up to 10 MHz.

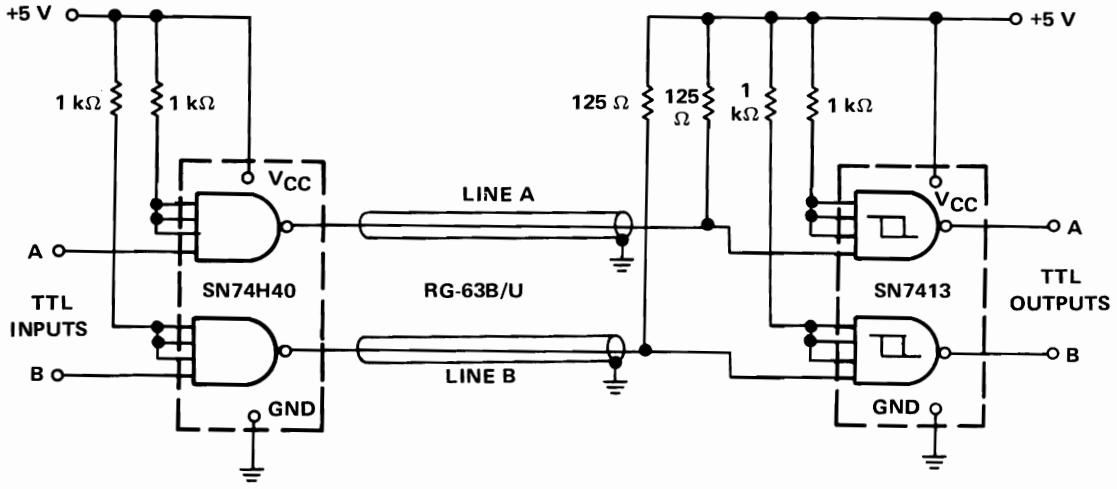


Figure 10.29. SN74H40 Driver with SN7413 Receiver

Line: A 125-ohm twisted-pair line or 125-ohm coax can be used. Since the circuit is a single-ended configuration, RG-63B/U coax is the best choice.

Driver: The SN74H40 quad-input positive-NAND buffer provides the current-handling ability required to switch this line. Two gates per package allow for dual-channel operation, and the multiple inputs provide for strobe control. The driver output is terminated to +5 volts at the receiving end of the line. With 125 ohms termination the driver needs to sink up to 40 mA and provide a good low logic 0 at the receiver.

Receiver: The SN7413 Schmitt trigger is chosen as a receiver. Its input characteristics cause it to switch quickly, and its hysteresis improves the noise margin.

Combining a Peripheral Driver with the SN7413 Schmitt Trigger — Circuits of this type can be used in short-line applications where better noise margin is required, and on longer lines (to 100 feet) where environmental conditions are not extreme. This method could be utilized for data transmission between adjacent racks or systems within one room. For this example the SN75453B is used as the driver. The circuit chosen (see Figure 10.30) requires termination at both ends of the transmission line to allow maximum operating frequencies with minimum ringing. The driving end is terminated to +5 volts; the receiving end is terminated to ground. Logic 1 levels at the receiver are +2.5 volts, and logic 0 levels are typically 0.3 volt. The worst-case input thresholds are 1.5 volts positive going and 1.1 volts negative going. Resulting worst-case noise margins are +1.2 volts and −1.4 volts. Typical noise margins are +1.4 volts and −1.6 volts. Propagation delays are about 35 nanoseconds for the driver, 18 nanoseconds for the receiver, and 150 nanoseconds for the 100-foot line. The system's t_{pD} will be about 203 nanoseconds. Transition times are fast enough to allow operation up to 20 MHz. When the driver is inhibited with a logic 1 level on the strobe, the receiver output will be at logic 0.

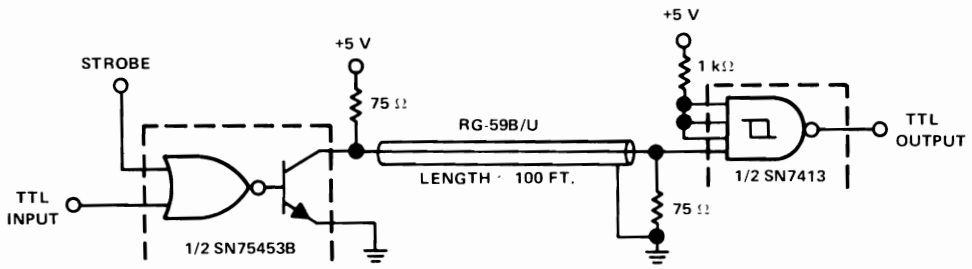


Figure 10.30. SN75453B Driver with SN7413 Receiver

Line: Because of single-ended transmission and possibly noisy environmental conditions, coax line is recommended. Several different types of coax lines can be employed, for the driver has high enough capability to drive low-impedance lines as well as moderate- or high-impedance lines. In this example 75-ohm RG-59B/U coax is used.

Driver: The SN75453B is chosen because of its logic characteristics. Its positive-OR function allows one input to be controlled by a strobe input which must be low to allow data transmission. The output drive capability permits use of low-impedance coax lines.

Receiver: The SN7413 Schmitt trigger provides additional noise margin. Use of this receiver with the SN75453B yields a noise margin about three times that of standard gates.

SN75451B Driver with SN75140 Receiver — In some single-ended applications where coax is driven and extremely long line lengths are used, two requirements prevail: (1) receiver sensitivity requirements are stringent, and (2) the driver must switch large signals at relatively high frequencies. The SN75451B, with 300-mA output current capability and low output saturation losses, can drive coax lines at high frequencies with signal levels close to the total V_{CC} voltage. The SN75140 receiver, while requiring only a single +5-volt supply, has a sensitivity of ±100 mV and an adjustable threshold for optimizing the noise margin.

Figure 10.31 shows a typical long-line application. The reference, or threshold, is set at one-half of the total pulse amplitude at the receiver. Lines of 10,000 feet or more may be driven in this configuration.

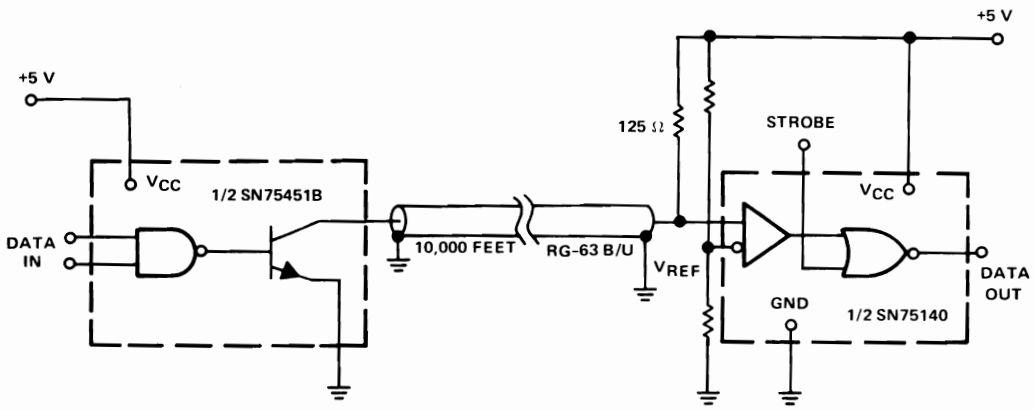


Figure 10.31. High-Speed Long-Line Transmission with Single-Ended Lines

SN75121 Driver with SN75122 Receiver — Designed primarily for single-ended applications, these devices are utilized with low-impedance coax lines. The combination is particularly desirable for aircraft or military applications requiring 50- or 75-ohm coax lines. Because of the driver's emitter-follower output and resulting high output impedance in the off condition, use in party-line or bus applications is possible.

Figure 10.32 depicts the SN75121 and SN75122 in a party-line application. With typical 0.5-V receiver threshold hysteresis, and assuming the typical negative going threshold of 1.3 V and a positive going threshold of 1.8 V, satisfactory noise margins result. The typical driver output levels are 3.7 V and 0 V. In this example the resulting noise margins are +1.8 volts and −2.4 volts.

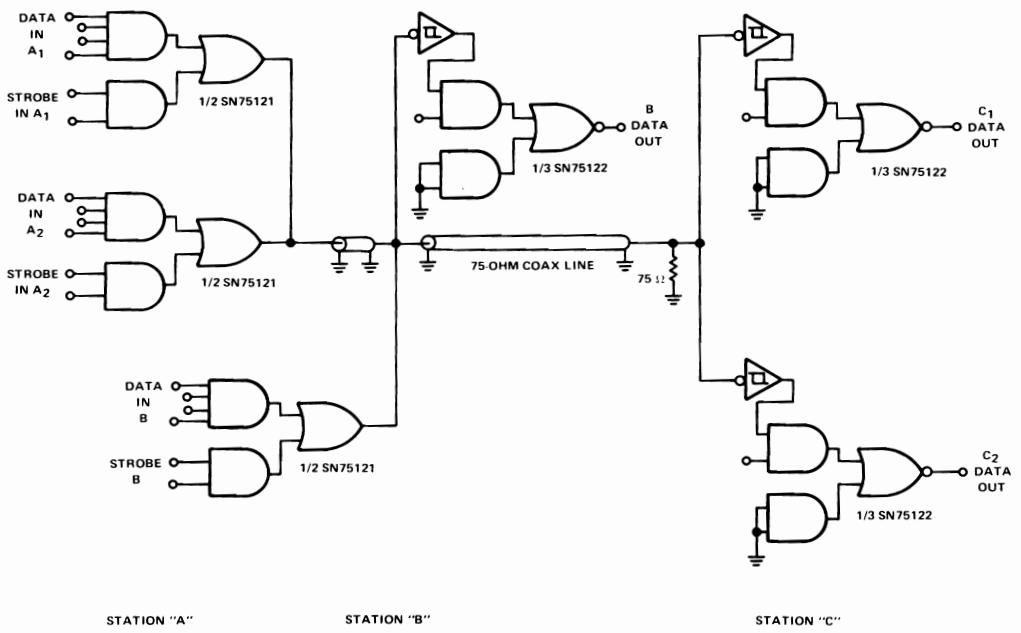


Figure 10.32. Single-Ended Party-Line Application

SN75365 Quad MOS Driver with SN75154 Quad Line Receiver — This combination provides a four-channel system (see Figure 10.33) with good operating characteristics. By connecting the driver V_{CC2} pin to the +5-volt supply the logic 1 and logic 0 levels at the receiver input will be about 4.5 volts and 0.5 volt respectively. With the receiver threshold controls connected through R_H to +5 volts, the negative going (logic 0 level) input threshold may be set as high as +1.5 volts. This yields a negative going noise margin of 3 volts and a positive going noise margin of 1.7 volts.

By allowing V_{CC2} of the driver to be 12 volts rather than 5 volts, it is possible to swing the receiver inputs from about 11.0 volts to 1.0 volt. With the hysteresis controls connected to +5 volts the noise margins will be −12 volts and +1.2 volts. Considerable improvement in positive noise margin could be obtained by using SN75152 receivers with hysteresis set symmetrically about a reference point midway in the input signal range. Noise margins of ±4.5 volts are possible.

Line: RG-63B/U 125-ohm coax line is recommended.

Driver: SN75365 quad driver with totem-pole outputs tied to a desired V_{CC2}. The input is TTL compatible, and output source and sink capabilities are 160 mA.

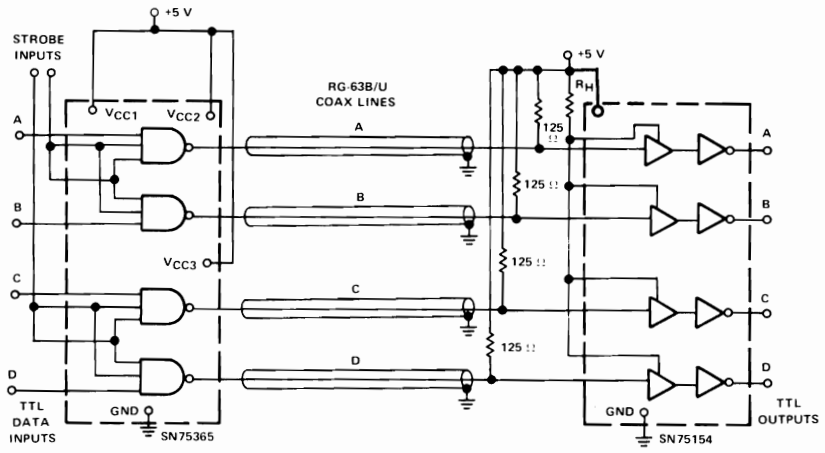


Figure 10.33. SN75365 Driver with SN75154 Receiver

Receiver: The SN75154, with high input voltage range capability (±25 V) and controllable hysteresis for optimum noise immunity, allows four lines to be driven and sensed by one driver and one receiver package.

SN75150 Driver and SN75154 Receiver — This circuit (Figure 10.34) utilizes device types designed for application in modem systems where the interfacing driver and receiver must meet EIA RS-232-C specifications. Although this particular application is data transmission over a line where the RS-232-C specifications are not applied, this series of device types provides excellent noise margins because of its design characteristics. This method would be used where single-ended transmission is required, line length is moderate (to 100 feet), frequency required is not high (under 100 kHz), and the environment is noisy.

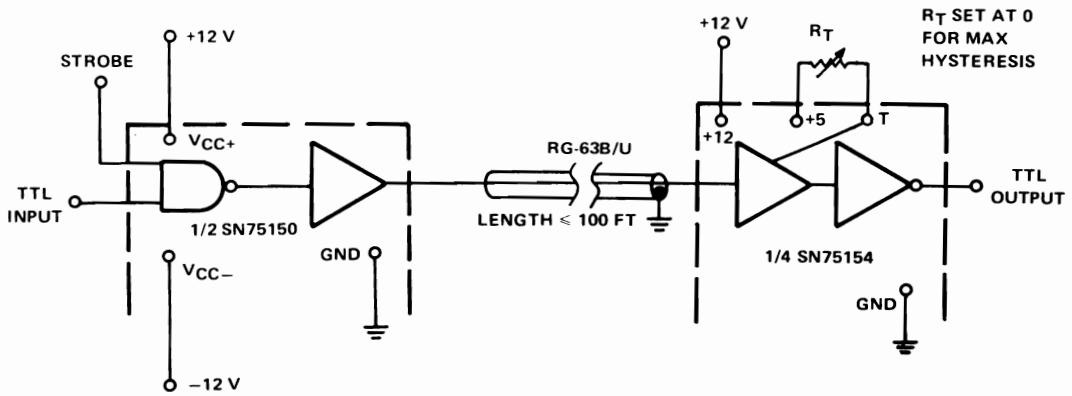


Figure 10.34. SN75150 Driver with SN75154 Receiver

The transmission line is unterminated, as shown in Figure 10.34. The receiver hysteresis is adjusted with R_T to achieve optimum results between noise margin and clean, sure switching. The driver strobe can be tied to a TTL logic 1 to leave it enabled. Logic 1 levels at the receiver input are +8 volts; logic 0 levels, —8 volts. With the receiver threshold terminal connected directly to +5 volts (pin 15), maximum hysteresis is achieved. The resulting noise margins are +10.2 volts and —9.1 volts (see Figure 10.35).

Propagation delays are about 60 nanoseconds for the driver and 22 nanoseconds for the receiver. Total system t_{PD} from driver input to receiver output is typically 230 nanoseconds for 100 feet.

Line: The line chosen for this application is RG-63B/U. To obtain a good drive level from the SN75150 a high-impedance load is required. The impedance of RG-63B/U is 125 ohms. The capacitance of this wire is only about 10 pF per foot, allowing the driver to operate at its highest frequency capability.

Driver: The SN75150 provides both positive and negative output voltage swings, allowing greater noise margins.

Receiver: The SN75154 is specifically suited to work with the SN75150 driver. Its wide and controllable hysteresis characteristics allow the circuit to have the best possible noise margin under these conditions. Noise margins nearly ten times those available from standard gates are possible.

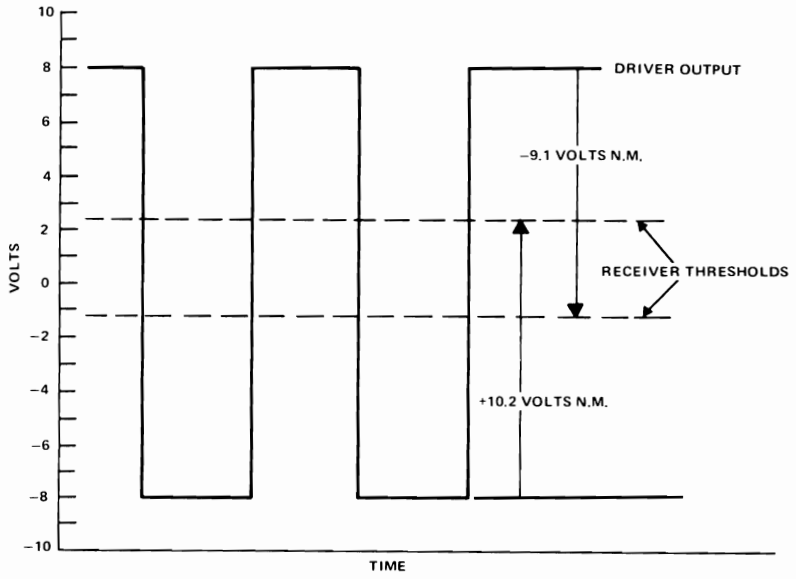


Figure 10.35. SN75150 Driver to SN75154 Receiver Noise Margins

SN75150 Driver and SN75154 Receiver in EIA RS-232-C Applications — This type of transmission system was designed to comply with EIA RS-232-C requirements for operation with modems (modulator-demodulator systems). They primarily serve as an interface between data terminals and the data modem (Figure 10.36). Basic terminology and device specifications applicable to such systems are presented below.

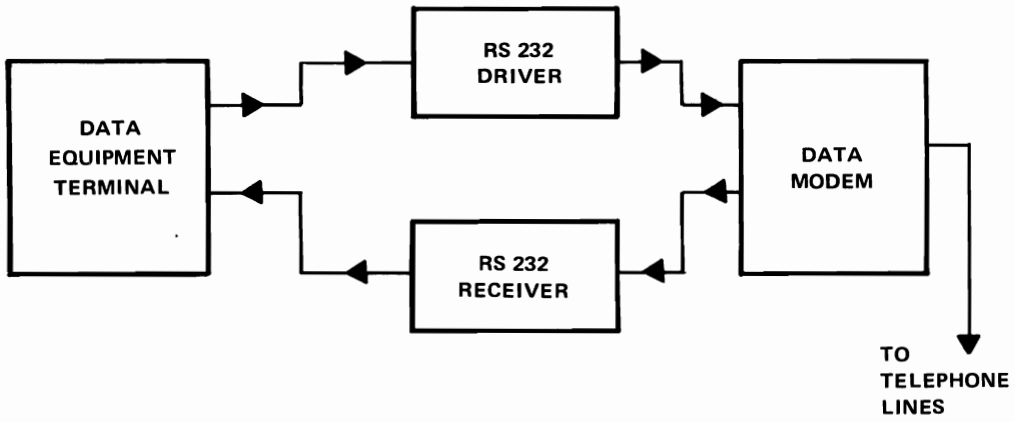


Figure 10.36. Data Terminal to Modem Interface

Definitions

Interchange Voltage: The voltage at the interface point between the modem and the interfacing driver or receiver.

Marking: The condition when an interchange voltage is more negative than −3 volts with respect to signal ground.

Transition Region: The region between plus and minus 3 volts. Table 10.3 shows the relationship between data and interchange voltage states.

Table 10.3. Relationship Between Data and Interchange Voltages

	Interchange Voltage		
Notation	Negative > −3 V	Positive > +3 V	−3 V to +3 V
Binary State	1	0	In Transition
Signal Condition	Marking	Spacing	In Transition
Function	Off	On	In Transition

Driver Requirements

Output must withstand an open circuit, or a short circuit to ground or either supply, or any other conductor in the interface cable.

Power-off output impedance must be ≥ 300 ohms.

Output drive must be equal to or less than ± 25 volts (open circuit condition).

Short-circuit output current must be less than 0.5 amp.

Absolute value of the output drive, into a 3000- to 7000-ohm load, must be ≥ 5 volts and ≤ 15 volts.

Output rise and fall times, within the transitional limits of plus and minus 3 volts, shall not exceed 1 millisecond.

Output slew rate shall not exceed 30 volts per microsecond. Must be capable of handling data rates of 20,000 bits/sec.

Receiver Requirements

Input impedance with an input voltage of ± 3 volts to ± 25 volts shall be ≥ 3000 ohms and ≤ 7000 ohms.

Load resulting from the receiver input and connecting cable shall not have an effective shunt capacitance in excess of 2500 pF. Its reactive component shall not be inductive.

Open-circuit input voltage of the receiver shall not exceed 2.0 volts.

Must be capable of handling data rates of up to 20,000 bits/sec.

Must withstand input voltages from −25 volts to +25 volts.

Output conditions — see Table 10.4.

Table 10.4. Input to Output Relationship

Input Level (Volts)	Output Logic
−3 to −25	1
+3 to +25	0
+3 to −3	Transition Region

SN75150 Dual Driver: The SN75150 dual driver is designed to be controlled by DTL or TTL logic and to drive a data modem within the conditional limits described in EIA Standard RS-232-C.

Supply Voltages:	V_{CC1} = +12 volts ±10% V_{CC2} = −12 volts ±10%
Operating Temperature Range:	0°C to +70°C
Packages:	Dual-in-line 8-pin plastic (P) Dual-in-line 14-pin plastic (N) Dual-in-line 14-pin ceramic (J) (See Figure 10.37)
Special Features:	Common input strobe. 1-microsecond transition time through ±3-V region with a full 2500-pF load. Meets all RS-232-C dynamic requirements Output short-circuit protected to ground or ±25 volts.

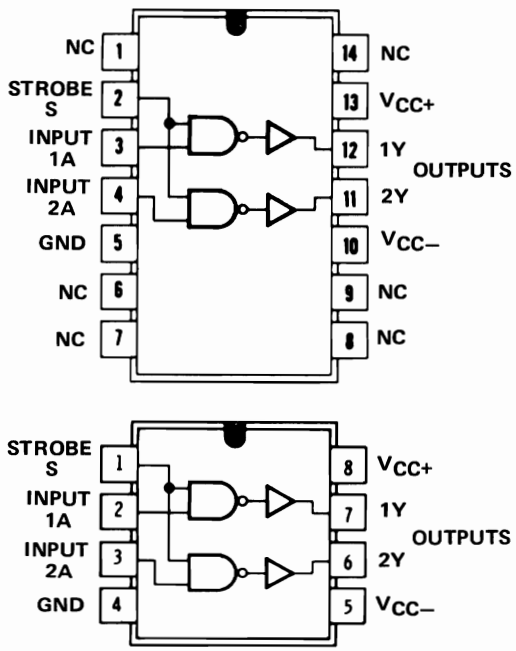


Figure 10.37. SN75150 Functional Diagram and Pin-Outs

SN75154 Quad Receiver for Modem Applications: Designed to interface directly from the data modem and TTL or DTL circuits as described in EIA Standard RS-232-C.

Supply Voltage:	+5 or optional +12 volts
Operating Temperature Range:	0°C to 70°C
Package:	Dual-in-line 16-pin N or J (See Figure 10.38)
Other Features:	Input Resistance — 3000 to 7000 ohms over the full RS-232-C voltage range. Internal threshold adjustable to meet "fail safe" requirements without external components. Built-in hysteresis for increased noise immunity. TTL output with active pull-up and pull-down for symmetrical switching speeds.

SN75152 Dual Receiver for Modem Applications: Designed to meet both MIL-STD-188C and EIA Standard RS-232-C.

Supply Voltages:	+12 volts and −12 volts
Operating Temperature Range:	0°C to 70°C
Package:	Dual-in-line 16-pin N or J (See Figure 10.39)

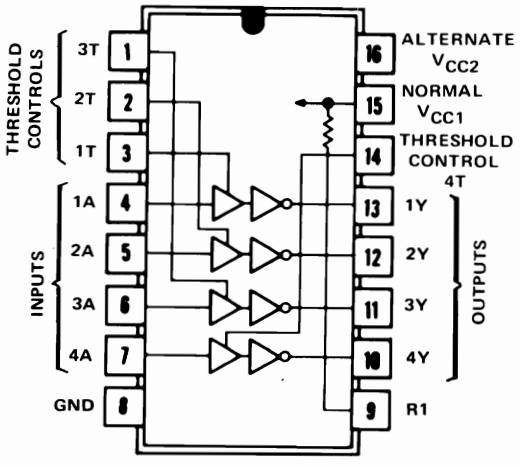


Figure 10.38. SN75154 Functional Diagram and Pin-Out

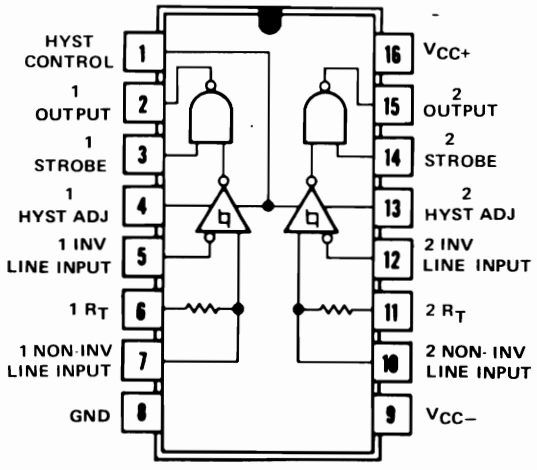


Figure 10.39. SN75152 Functional Diagram and Pin-Out

Other Features:

- Dual differential receivers with independent strobes.
- Common-mode input voltage range ±25 volts.
- Differential input capability, one input grounded, ±25 volts (Figure 10.40).
- Continuously adjustable hysteresis with external resistors from ±0.3 volt to ±5 volts typically (Figure 10.41).
- Input threshold stable with supply and temperature variations.

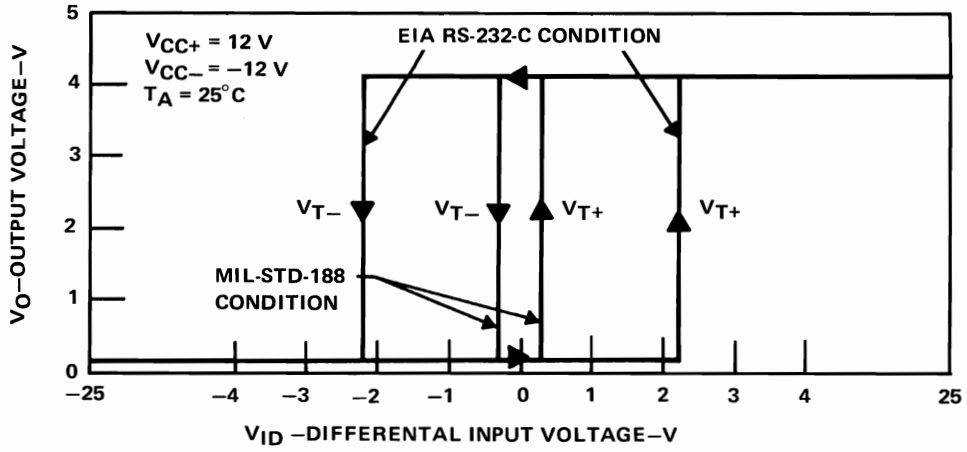


Figure 10.40. Threshold Hysteresis of SN75152

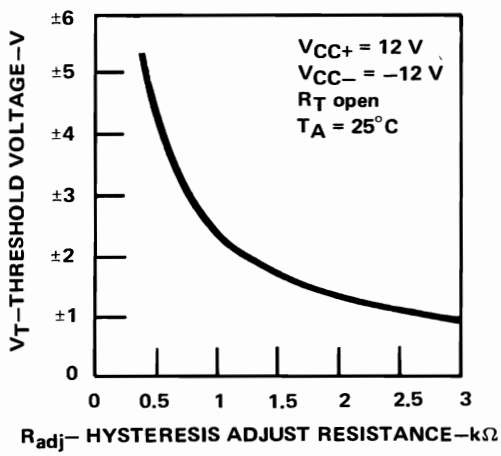


Figure 10.41. Threshold Voltage Characteristic of SN75152

SN75150 Driver and SN75152 Receiver in MIL-STD-188C Applications — Although the SN75150 was designed primarily for use in EIA RS-232-C interface systems it may also be employed in compliance with the military standard in modem applications. Driver requirements are slightly different, and a minor external modification is required to meet the 188C specification.

Transmitter Features	Receiver Features
V_{OUT} = ±6 V (±1 V) clamped by external zeners.	$R_{in} \geq$ 6,000 ohms
Z_{OUT} = 35 ohms typical	Differential inputs allow noninverted or inverted output
Standard ±12-volt supplies	Adjustable hysteresis
TTL/DTL-compatible inputs	Standard ±12-volt supplies
Dual channels	TTL/DTL-compatible outputs
	Dual channels

The circuit configuration for military standard 188C modem interface applications is shown in Figure 10.42.

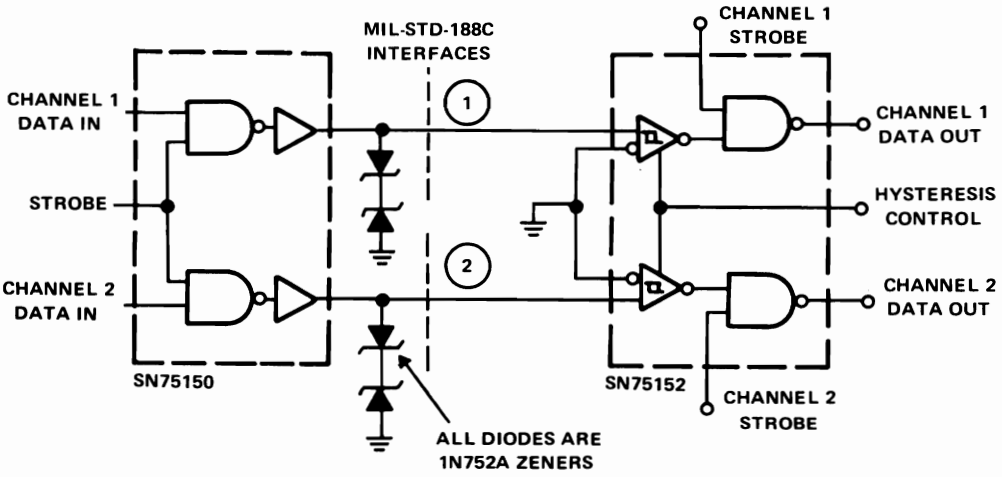


Figure 10.42. MIL-STD-188C Interface Circuit

10.4.4 Balanced Single-Supply Line Drivers and Receivers

Balanced-line transmission is favored in many applications because of common-mode characteristics of such a system. Using a form of balanced differential driver and a differential receiver allows reception of low-level data signals in the presence of rather high-level common-mode noise. The balanced line picks up noise signals (interference), but they are common to both lines and therefore rejected by the differential receiver.

SN75450B Driver with SN75115 Receiver — The SN75450B may be connected as a balanced-line driver operating from 5 volts. The SN75115 differential receiver also operates from a single 5-volt supply, in the circuit configuration shown in Figure 10.43. Driving the lines alternately to +5 volts yields an effective differential swing of 10 volts at the receiver. The balanced drive is accomplished by inverting the drive for one output and using it to drive the other output. Proper termination at the receiver helps maintain clean signal reception as well as providing the driver output supply voltage.

Common-mode limits of the receiver input are ±15 volts. Common-mode noise levels up to +4 volts and −15 volts do not interfere with the incoming signal. There is some delay between line 1 and line 2 drive signals, but the skew is typically under 10 nanoseconds. Frequencies of up to 10 MHz may be driven over relatively long lines (⩾ 500 feet). True party-line operation is not possible with this type of system, but up to five receivers can be connected to the line. Termination would be at the extreme end of the line. The 1N4444 blocking diodes, optional, provide additional driver common-mode capability.

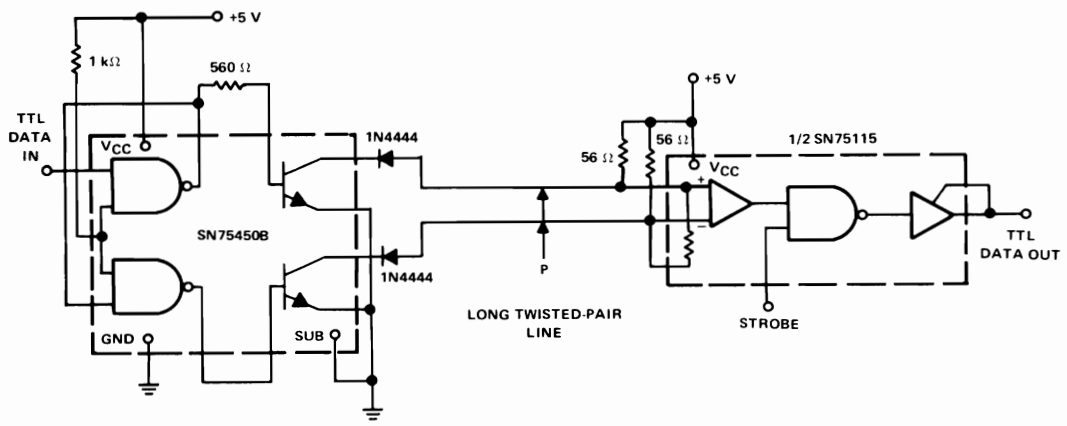


Figure 10.43. Balanced-Line Circuit Using a Peripheral Driver

Line: Twisted-pair line is used in most balanced-line applications. A 22-gauge twisted-pair line with characteristic impedance of 110 ohms would be a good choice for this application.

Driver: The ability of the SN75450B to quickly discharge the line and drive the low-impedance terminations makes it a good driver for this application.

Receiver: The SN75115 line receiver is designed to operate from balanced transmission lines at frequencies of up to 10 MHz. Although its sensitivity is not as great (±500 mV) as that of some differential input receivers, its advantages make it desirable in many moderate- to long-line balanced applications. This receiver works from a single 5-volt supply, and its input common-mode range of ±15 volts is desirable in long-line communications.

SN75113/SN75114 Driver with SN75115 Receiver — The SN75113/SN75114 and SN75115 devices have been designed specifically for driving balanced-transmission lines and operating from single 5-volt power supplies. This circuit combination may also be used to drive single-ended transmission lines. Both the driver and the receiver operate from popular +5-volt supplies. For a single driver circuit the SN75114 may be preferred. If more than one driver is to be on the line at a time, the SN75113 driver would be used because of its party-line or three-state output capability. (See Figure 10.44).

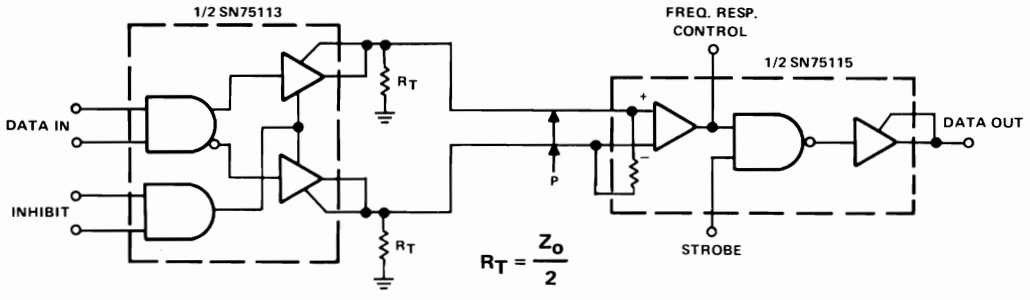


Figure 10.44. Single-Supply Transmission Circuit

Line: Typical 100-ohm twisted-pair line is recommended for balanced transmission, and 50-ohm coax for single-ended applications.

Driver: For frequencies of 5 MHz or less and line lengths of 500 feet or less, the SN75114 performs well. As it is a voltage-mode driver with limited power-handling ability, care must be taken in driving low-impedance lines.

Receiver: The SN75115 as previously described is well suited for this application.

SN75450B Driver with SN75152 Receiver — This circuit combination has the characteristics required to drive long low-impedance transmission lines in rather severe noise environments. Line lengths of up to a mile or more may be driven with satisfactory reception at frequencies of 1 MHz. High driver output levels and completely controllable hysteresis at the receiver combine to provide good noise-rejection characteristics.

The SN75450B is connected as a collector output balanced driver (see Figure 10.45). The 50-ohm terminators at the driver end of the lines provide short-circuit protection for the lines as well as proper termination. Voltage swing into the line is about 6 volts on each line for an effective differential swing of 12 volts. The high current-handling capability of the SN75450B allows it to easily drive the line. Driver sink current is about 240 mA, well within the pulse rating of the SN75450B output transistors.

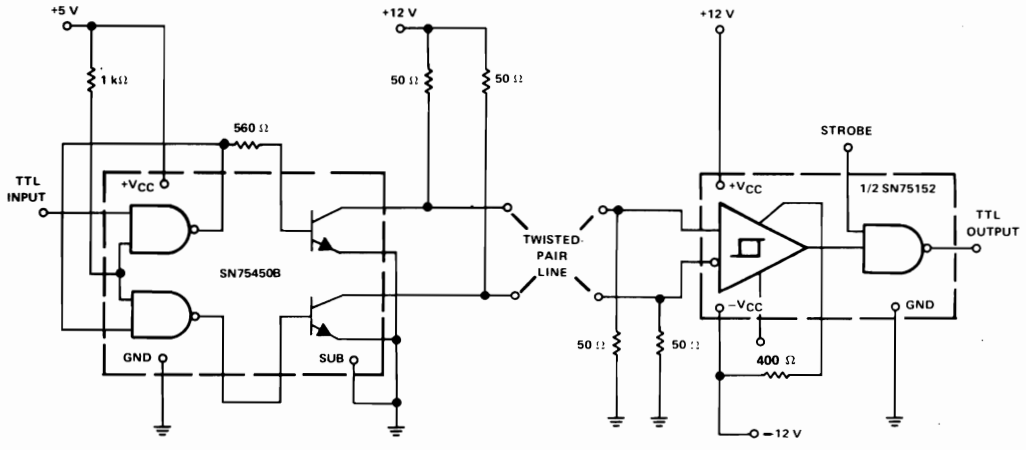


Figure 10.45. Balanced-Line Transmission with ±11 Volts Noise Margin

The receiver is connected to give ±5-volt switching levels, or a total hysteresis range of 10 volts. Figure 10.46 shows the resulting noise margin for this circuit to be ±11 volts. Even greater noise margins are possible, but, as drive voltages are increased, power dissipation and line currents become excessively large. It is possible, with some circuit modifications and higher collector supply voltages for the SN75450B, to obtain a noise margin as high as ±30 volts.

This circuit combination is probably one of the best available low-cost monolithic devices in respect to noise immunity. Both common-mode and single-ended noise margins are high. Because of the generally low impedance of the line terminations several watts of noise power could be coupled into the line before interference would occur.

Line: The transmission line could be coaxial or twisted pair. For this example a twisted-pair line is used to derive maximum benefit from the driver's capability. It is assumed that the impedance is a typical 100 ohms. Preferably 18-gauge wire should be used because of the high drive currents.

Driver: The SN75450B is chosen because of its ability to drive a balanced low-impedance line at high levels and at relatively high frequencies.

Receiver: The SN75152 is chosen because of its completely controllable hysteresis characteristics. The ability to adjust not only the hysteresis range but also the midpoint voltage assures maximum noise immunity.

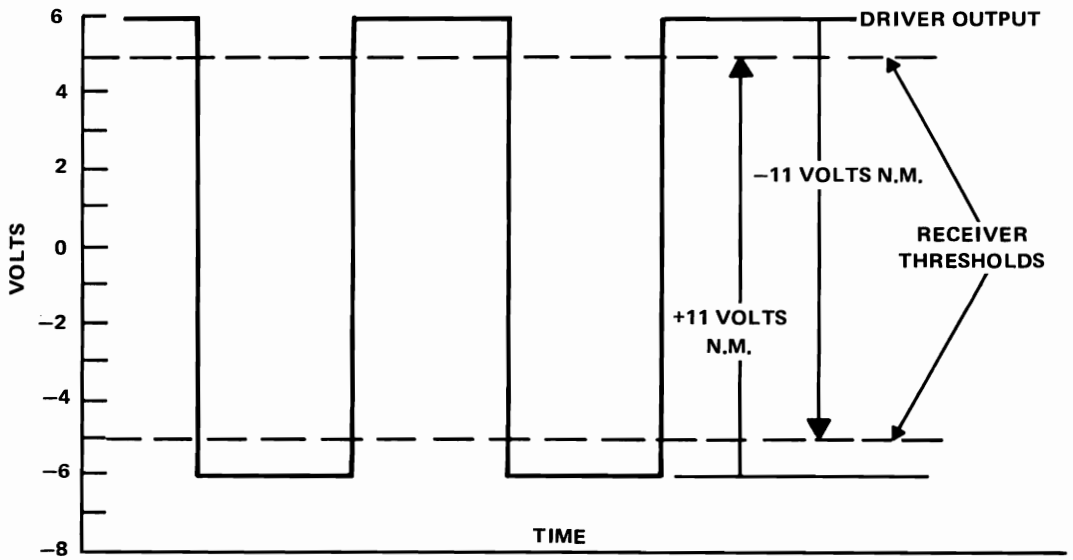


Figure 10.46. Noise Margins of Circuit in Figure 10.45

10.4.5 Current-Mode Drivers in Balanced Systems

The characteristics of voltage-mode line drivers make party-line applications difficult, and considerable power is required where low-impedance lines and high frequencies are needed. Using a dual power supply the SN75109 and SN75110 line drivers overcome these disadvantages by driving the lines from constant-current sources.

SN75109 Driver with SN75107A Receiver — This combination of driver and receiver has proved effective for short- or long-line applications. Its high impedance characteristics do not load the transmission line significantly, and therefore party-line operation, using several drivers and receivers, is possible. A basic balanced transmission system using the SN75107A series devices is shown in Figure 10.47. Operation over line lengths in excess of 1000 feet is possible, with excellent noise-rejection capability. The transmission line is terminated at the extreme ends only.

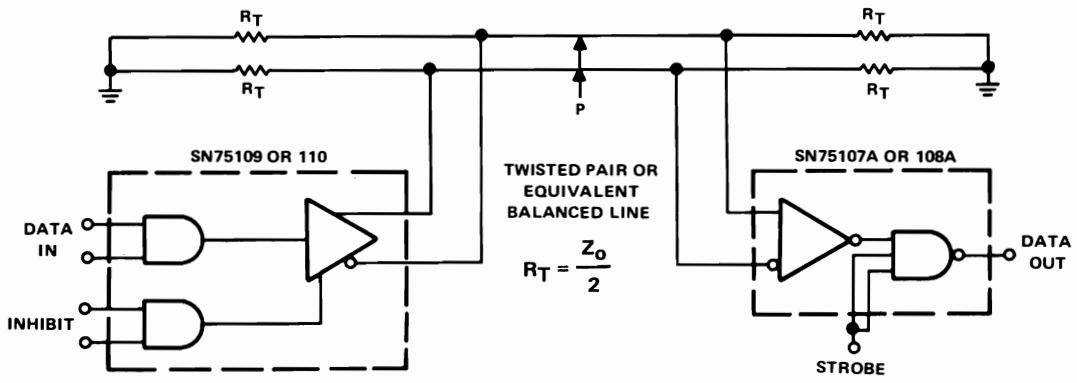


Figure 10.47. Basic Balanced System Using SN75107A Series Devices

Line: Almost any low-impedance balanced transmission line can be driven; in most applications an unshielded twisted pair is satisfactory. A typical 100-ohm shielded line is Belden 8227, built specifically for data line transmission. Belden 8795 is a typical unshielded line with about 100 ohms impedance.

Driver: The SN75109 driver has a differential output driven by a constant-current driver with 6 mA of drive. Controlled by a TTL input, the driver outputs are switched on and off alternately, providing a drive voltage from the product of the driver currents and line terminations. Strobes are available to enable or disable the

driver. When it is disabled the current generator is turned off, resulting in a high output impedance. It operates at frequencies up to 10 MHz. The SN75110 has a 12-mA output capability for driving longer lines than the SN75109.

Receiver: The SN75107A differential receiver, with input sensitivity of ±25 mV or better, has a common-mode input range of ±3 volts. This type of receiver works well in long-line applications where common-mode noise pickup is high and the transmitted signal has been attenuated considerably. With a differential input signal of only 25 mV and common-mode noise levels as high as 6 volts peak to peak, it faithfully reproduces the signal.

Oscilloscope traces show the two transmission lines with 4-volt peak-to-peak noise levels due to common-mode pickup. The test signal was a differential signal of only 50 mV peak to peak at 10 kHz. As noted in the receiver output trace, large common-mode noise signals were rejected and low-level data signals were faithfully reproduced at the receiver output.

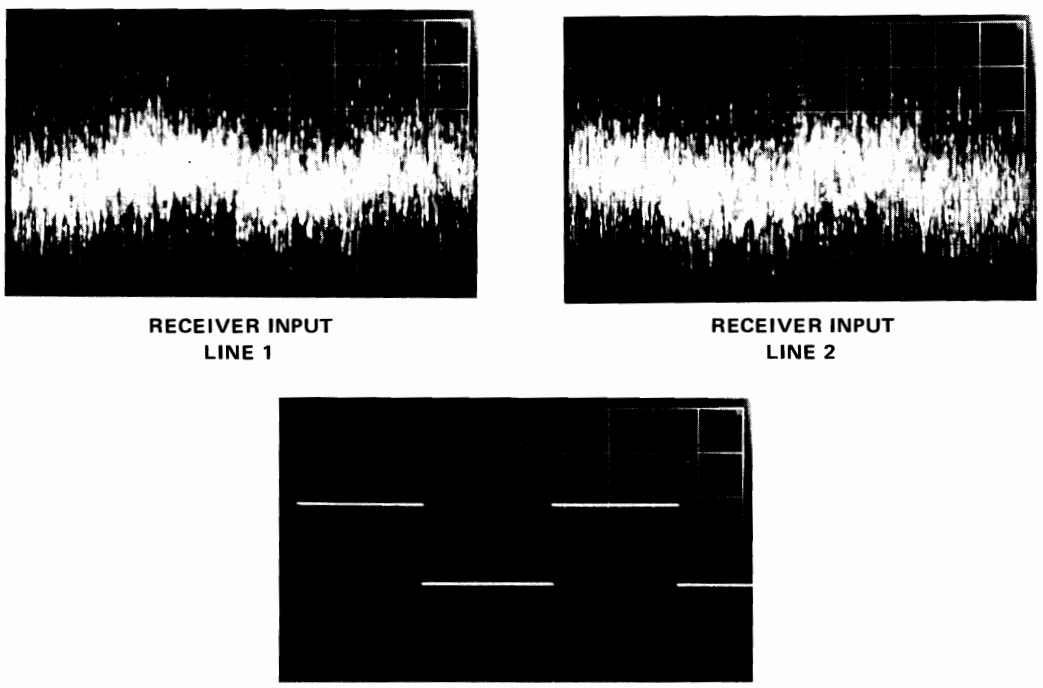


Figure 10.48. Common-Mode Rejection of the SN75108A Receiver

Party-Line Balanced Systems — The need to communicate between many receivers and line drivers using the scheme in Figure 10.47 could require large amounts of wire and consequently increase the installation costs. For example, in transmitting and receiving information from the cockpit of an airplane to some remote area in the tail of the plane, the wire required for a multi-channel system might well weigh more than all of the equipment involved. Thus a method allowing several drivers and receivers to share a single transmission line is desirable.

The strobe feature of the receivers and the inhibit feature of the drivers allow SN55107A series dual-line circuits to be used in party-line (also called data-bus) applications. Examples are shown in Figures 10.49, 10.50, and 10.51. In each of these systems an enabled driver transmits data to all enabled receivers on the line while other drivers and receivers are disabled. Data can therefore be time-multiplexed on the transmission line.

The SN55107A series specifications allow widely varying thermal and electrical environments at the various driver and receiver locations. The party-line system offers maximum performance at minimum cost for appropriate applications.

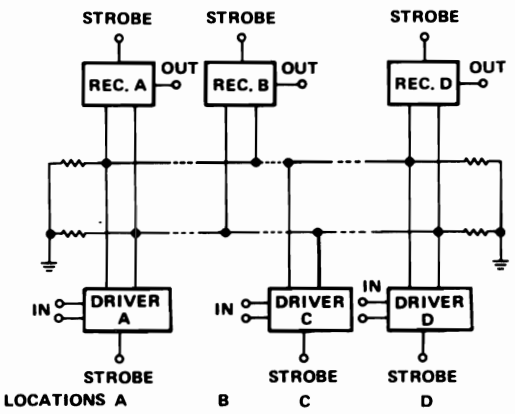


Figure 10.49. Basic Party-Line System

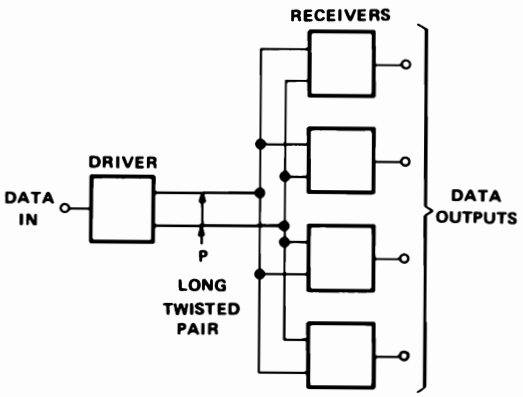


Figure 10.50. Party-Line System Using One Driver and Several Receivers

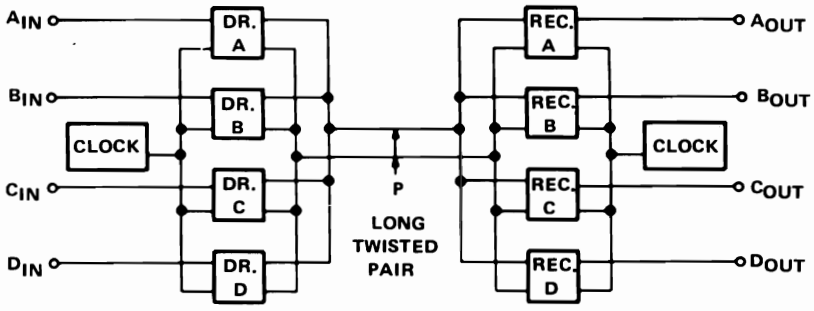


Figure 10.51. Four Transmission Channels Share a Single Line

Figure 10.52 shows an eight-channel party-line system similar to that in Figure 10.51, including clocking arrangements. This method uses two twisted-pair lines: one for data transmission and the other for clocking and control information. Details of this system appear in Figures 10.53 and 10.54. Careful matching of the line delay is necessary to insure synchronized clocking. Some compensation networks might be needed.

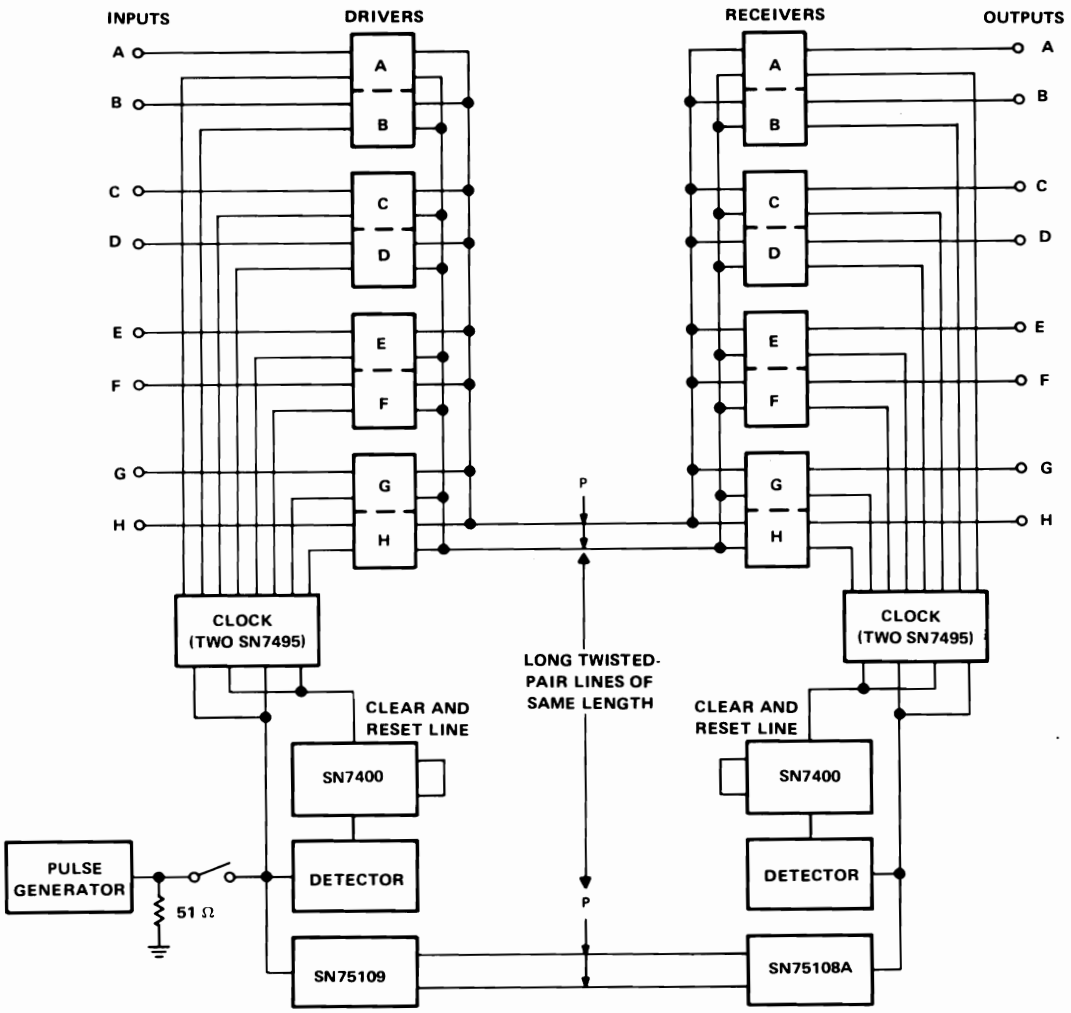


Figure 10.52. Multi-Channel System with Clocking Provisions

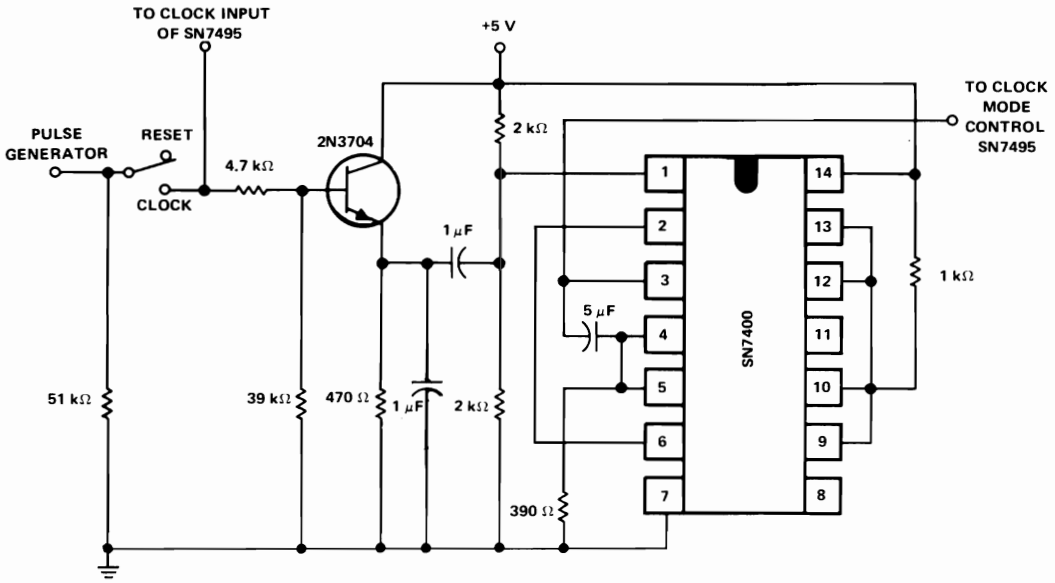


Figure 10.53. Detector Circuit for Clearing SN7495 Clock in Figure 10.52

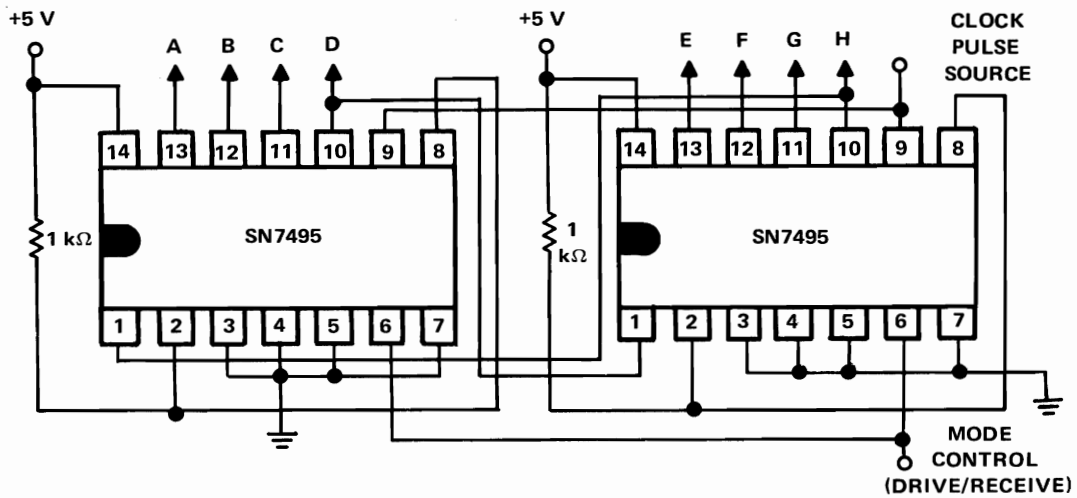


Figure 10.54. SN7495 Clock for Strobing Drivers and Receivers in Figure 10.52

Unbalanced or Single-Line Systems — SN55107A series dual-line circuits may also be used in unbalanced (single-line) systems. These systems do not offer the same performance as balanced systems for long lines, but are adequate for very short lines where environmental noise is not severe.

In such systems the receiver threshold level is established by applying a dc reference voltage to one receiver input terminal and supplying the transmission line signal to the remaining input. The reference voltage should be optimized so that signal swing is symmetrical with respect to it for maximum noise margin. The reference voltage should be in the range of −3 V to +3 V. It can be provided by either a separate voltage source or a voltage divider from one of the available supplies.

A single-ended output from a driver is used in single-wire systems as shown in Figure 10.55. A coaxial line is preferred, to minimize noise and crosstalk problems. For large signal swings, the SN75110 is recommended because it has the higher output current. Two drivers may be paralleled for even higher current. The unused driver output terminal should be tied to ground as shown in the figure. The voltage at the output of the driver is then $V_{out} = (V_p - R2\ I_{out})\ (R1)/(R1 + R2)$, where I_{out} is the given output sinking current. The values of R1 and R2 affect the amplitude of the pulse and its position with respect to ground.

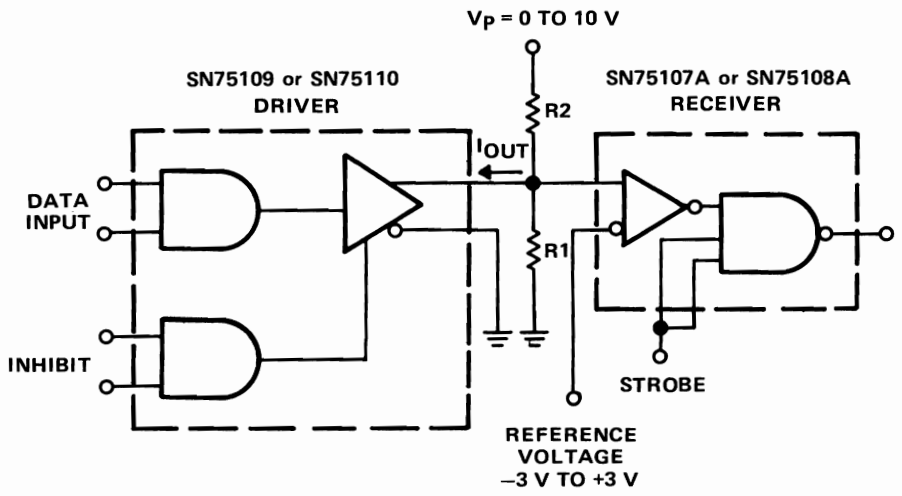


Figure 10.55. Typical Single-Line System Using SN75107A Series Devices

10.5 SELECTION OF LINE TRANSMISSION CIRCUITS

Since many line-driver and receiver circuits are available an analysis of system requirements is necessary before determining which device should be selected. Following is a list of basic considerations:

Line-circuit costs	Receiver sensitivity required
Availability	Drive mode and drive levels
Second-source availability	Number of channels required
Length of line to be driven	Voltage of power supplies
Maximum data rates	Party-line requirements
Environmental noise levels	Common-mode capability
Linve radiation restraints	Standard spec requirements

Tables 10.5 through 10.9 show the basic characteristics of line drivers, receivers, and transceivers. Typical combinations of drivers and receivers, with performance characteristics, are listed in Table 10.10. A review of system requirements and these line-circuit characteristics will substantially aid the designer in selecting line circuits for a particular application.

Table 10.5. Differential Line Receivers

FEATURES		SN55107A SN75107A	SN75207	SN55108A SN75108A	SN75208	SN55115 SN75115	SN75152†	SN55182 SN75182	UNIT
Receivers per Package		2	2	2	2	2	2	2	
Input Sensitivity		±25	±10	±25	±10	±1000	NA	±1000	mV
Input Common-Mode Range		±3	±3	±3	±3	±15	±25	±15	V
Hysteresis (Double Thresholds)		No	No	No	No	No	Yes	No	
Response Control		No	No	No	No	Yes	No	Yes	
Output Strobe		Yes	Yes	Yes	Yes	Yes	Yes	Yes	
TTL Output Configuration		Active Pull-Up	Active Pull-Up	Open-Collector	Open-Collector	Open-Collector with Active Pull-Up Option	Resistor Pull-Up	Active Pull-Up	
Power Supplies		±5	±5	±5	±5	+5	±12	+5	V
Package Types	Series 55	J		J		J, SB		J	
	Series 75	J, N	J, N	J, N	J, N	J, N, SB	J, N	J, N	

Table 10.6. Single-Ended Line Receivers

FEATURES		SN55122 SN75122	SN75124	SN75140	SN55142 SN75142	SN75154†	SN75189†	SN75189A†	UNIT
Receivers per Package		3	3	2	2	4	4	4	
Input Sensitivity		NA	NA	±100	±100	NA	NA	NA	mV
Hysteresis (Double Thresholds)		Yes	Yes	No	No	Yes	Yes	Yes	
Response Control		No	No	No	No	No	Yes	Yes	
Output Strobe		Yes	Yes	Yes	Yes	No	No	No	
TTL Output		Active	Active	Active	Active	Active	Resistor	Resistor	
Configuration		Pull-Up	Pull-Up	Pull-Up	Pull-Up	Pull-Up	Pull-Up	Pull-Up	
Power Supplies		+5	+5	+5	+5	+5 or +12	+5	+5	V
Package Types	Series 55	J			J				
	Series 75	J, N	J, N	P	J, N	J, N	J, N	J, N	

† Satisfies requirements of EIA RS-232-C

Table 10.7. Line Drivers, Differential or Single-Ended

FEATURES		SN55109 SN75109	SN55110 SN75110	SN55113 SN75113	SN55114 SN75114	SN55183 SN75183	SN55450B SN75450B
Drivers per Package		2	2	2	2	2	2
Party-Line (Data Bus) Operation		Yes	Yes	Yes	No	No	Yes
Type of Output		Current	Current	Voltage	Voltage	Voltage	Voltage
Output Strobe		Yes	Yes	Yes	No	No	No
Input Compatibility		TTL	TTL	TTL	TTL	TTL	TTL
Power Supplies		±5 V	±5 V	+5 V	+5 V	+5 V	+5 V
Package Types	Series 55	J	J	J, SB	J, SB	J	J, JB
	Series 75	J, N	J, N	J, N, SB	J, N, SB	J, N	J, N

Table 10.8. Line Drivers, Single-Ended Only

FEATURES		SN55121 SN75121	SN75123	SN75150†	SN75188†	SN75361A	SN55451B SN75451B
Drivers per Package		2	2	2	4	2	2
Party-Line (Data Bus) Operation		Yes	Yes	No	No	No	Yes
Type of Output		Voltage	Voltage	Voltage	Voltage	Voltage	Voltage
Output Strobe		Yes	Yes	No	No	No	Yes
Input Compatibility		TTL	TTL	TTL	TTL	TTL	TTL
Power Supplies		+5 V	+5 V	±12 V	±12 V	+5 V	+5 V
Package Types	Series 55	J					JP, L
	Series 75	J, N	J, N	J, N, P	J, N	J, N, P	L, P

Table 10.9. Line Transceivers

FEATURES		SN55138 SN75138	SN55116 SN75116	SN55117 SN75117	UNIT
Transceivers per Package		4	1	1	
Type of Operation		Single-Ended	Differential	Differential	
Party-Line (Data Bus) Operation		Yes	Yes	Yes	
Driver Output Type		Voltage (Open-collector)	Voltage (Open-collector with active pull-up option)	Voltage (Active pull-up)	
Driver Output Current Capability		150	40	40	mA
Driver Strobe		Yes	Yes	Yes	
Driver Input Compatibility		TTL	TTL	TTL	
Receiver Input Sensitivity		NA	±1000	±1000	mV
Receiver Strobe		No	Yes	Yes	
Receiver Response Control		No	Yes	No	
Receiver Hysteresis		No	No	No	
Receiver (TTL) Output Configuration		Active Pull-Up	Open-Collector with Active Pull-Up Option	Active Pull-Up	
Receiver Input Common-Mode Range (with Driver Off)		NA	±15	0 to 6	V
Package Types	Series 55	J	J	JP	
	Series 75	J, N	J, N	P	

† Satisfies requirements of EIA RS-232-C

Table 10.10(a). Characteristics of Typical Line-Transmission Circuit Combinations (Basic Device Characteristics)

Circuit Combinations	Driver Output Mode	Receiver Sensitivity	Channels per Package		Supplies Required	Party-Line Capability
			Driver	Rec.		
SN75109 SN75107A	Current 6 mA Differential	⩽ 25 mV	2	2	Dual ±5 V	Yes
SN75110 SN75108A	Current 12 mA Differential	⩽ 25 mV	2	2	Dual ±5 V	Yes
SN75113 SN75115	Voltage 3.2 V Differential	⩽ 500 mV	2	2	Single +5 V	Yes
SN75116 Transceiver	Voltage 3.2 V Differential	⩽ 500 mV	1	1	Single +5 V	Yes
SN75117 Transceiver	Voltage 3.2 V Differential	⩽ 500 mV	1	1	Single +5 V	Yes
SN75183 SN75182	Voltage 3.0 V Differential	⩽ 500 mV	2	2	Single +5 V	No
SN75150 SN75154	Voltage ± 8.0 V Single Ended	2.1 V pos. going 1.30 V neg. going	2	4	Driver ±12 V Rec. + 12 V OR + 5 V	No
SN75123 SN75124	Voltage 3.2 V Single Ended	1.7 V pos. going 0.7 V neg. going	2	3	Single +5 V	Yes
SN75138 Transceiver	Voltage 3.1 V Single Ended	2.3 V Threshold	4	4	Single +5 V	Yes
SN75361A SN75140	Voltage 3.5 V Single Ended	1.5 V Threshold 100 mV Sens.	2	2	Single +5 V	No
SN75451B SN75142	Voltage 5.0 V Single Ended	2.5 V Threshold 100 mV Sens.	2	2	Single +5 V	Yes

Table 10.10(b). Characteristics of Typical Line-Transmission Circuit Combinations (Performance Characteristics)

Circuit Combinations	Typ. Max. Freq. Over 100' TPL 50% DC	Typ. Max. Freq. Over 1K' TPL 50% DC	Additional Comments
SN75109 SN75107A	20 Mb/s	12 Mb/s	Low line radiation Std. TTL receiver output ±3 V common-mode range
SN75110 SN75108A	20 Mb/s	15 Mb/s	Same as 109/107A except receiver output open collector
SN75113 SN75115	25 Mb/s	7.5 Mb/s	Driver: Three-state, split totem-pole output. 40 mA drive receiver has freq. resp. cont.
SN75116 Transceiver	25 Mb/s	7.5 Mb/s	SN75113 type driver SN75115 type receiver ±15 V common-mode range
SN75117 Transceiver	25 Mb/s	7.5 Mb/s	Same as SN75116 except 8-pin package 0 to +6 V common-mode range
SN75183 SN75182	13 Mb/s	7.0 Mb/s	Driver: 4 inputs per channel Receiver: ± 15 V CMR
SN75150 SN75154	1.25 Mb/s	1.0 Mb/s	Meets all EIA RS-232-C req. ±25 V CMR controllable hysteresis
SN75123 SN75124	25 Mb/s	9.5 Mb/s	Designed to meet IBM 360 requirements. Receiver has built-in threshold hysteresis
SN75138 Transceiver	8.5 Mb/s	2.0 Mb/s	100 mA driver capability High receiver input Z and driver output Z allow >100 on a party line
SN75361A SN75140	11.0 Mb/s	6.0 Mb/s	Drivers and receivers come in 8-pin packages. High Z_{in} receiver allows many to be used
SN75451B SN75142	10.0 Mb/s	10.0 Mb/s	High driver output voltage and speed allow longer line operation at high frequencies