Technical Series IC-41

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RCA linear integrated circuits

- design fundamentals
- application information
- technical data

RCA linear integrated circuits

Radio Corporation of America
Electronic Components and Devices, Harrison, N. J. 07029

CONTENTS

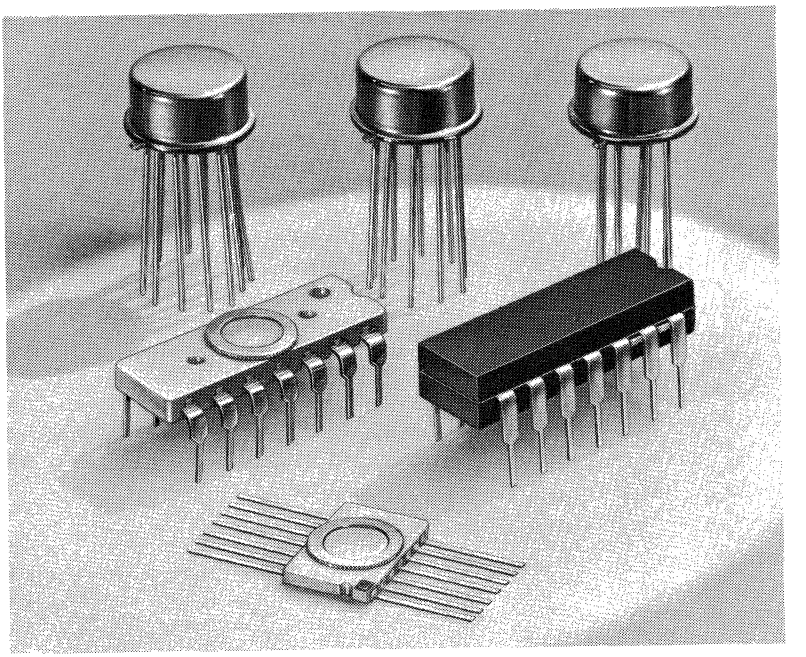
RCA linear integrated circuits

This Manual, like its preceding edition, has been prepared to provide an understanding of the basic principles involved in the design and application of linear integrated circuits. It may be used as a guide by circuit and systems designers in determining optimum design specifications with regard to integrated-circuit capabilities and system requirements. Effects of the silicon monolithic fabrication process on circuit design are explained, different types of integrated-circuit packages are discussed, and mounting and interconnection techniques are described. Design equations and performance criteria are derived for basic circuit configurations. Descriptive data and applications information are provided on a broad family of RCA linear integrated circuits.

This edition has been revised and expanded to cover the latest innovations in linear integrated circuit design, packaging, and application. Information has been added on many new types of circuits. Also featured are new **TECHNICAL DATA** and **OUTLINES** Sections that provide readily accessible information on ratings, characteristics, and package details for the complete line of RCA linear integrated circuits.

RADIO CORPORATION OF AMERICA
Electronic Components and Devices Harrison, New Jersey

RCA linear integrated circuits



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General Considerations

THE design of linear circuits involves the selection and interconnection of an optimum combination of active and passive components to accomplish a signal-processing function with maximum efficiency and minimum cost. This general rule is valid whether the components are conventional ones fabricated separately by a variety of processes or integrated components formed simultaneously by a single technology. The new design considerations introduced by the advent of integrated-circuit technology arise not from any differences in the fundamental electronic properties of the components individually, but from the technical and economic implications of simultaneous fabrication and interconnection. This section describes the technology used for the fabrication of integrated circuits, and discusses the aspects that introduce factors not present when discrete components are used and their implications with regard to the design of linear circuits.

INTEGRATED-CIRCUIT FABRICATION

The fundamental requirement of an integrated circuit is that components be processed simultaneously from common materials. A variety of technologies can be used to satisfy this requirement. If a circuit function can be represented solely by linear reciprocal networks consisting of resistive and capacitive elements, any one of several thin-film technologies using such materials as tantalum, nichrome, or tin oxide can be used effectively. The use of more sophisticated thin-film techniques makes it possible to form active as well as passive components. A cadmium sulfide technology developed by RCA is capable of fabricating both field-effect transistors and passive components on a common substrate.

The technology presently used for achieving circuit integration, however, is based not on thin-film approaches, but on the silicon planar technology developed for transistors. This technology has become dominant because of its ability to provide higher-quality active devices than any competing technology.

The basic steps of the silicon process are shown in Figs. 1 through 4. The starting material is a uniform single crystal of n-type or p-type silicon, as shown in Fig. 1. Diffusion processing techniques permit the introduction of impurities to desired depths and widths in the starting material. Vertical penetration of the impurities is controlled by the diffusion temperature and time, and lateral control of the diffusions is made possible by combination of the masking properties of silicon dioxide with photochemical techniques.

When localized n-type regions are diffused into p-type starting material, as shown in Fig. 2, isolated circuit nodes are achieved.

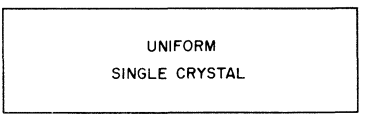


Fig. 1 — Silicon wafer used as starting material for an integrated circuit.

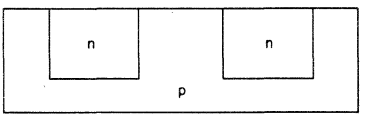


Fig. 2 — Diffusion of n-type areas to provide isolated circuit nodes.

The diodes formed by the p-type substrate and the n-type nodes accomplish electrical isolation between the nodes. Diffusion of additional p-type and n-type regions forms transistors, as shown in Fig. 3. The silicon wafer is then coated with an insulating oxide layer, and the oxide is opened selectively to permit metallization and interconnection, as shown in Fig. 4. When resistors are required, the n-type emitter diffusion is omitted and two ohmic

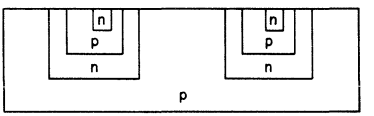


Fig. 3 — Diffusion of additional p-type and n-type regions to form transistors.

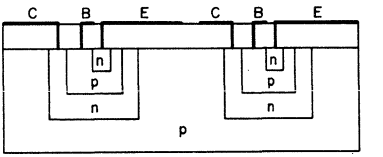


Fig. 4 — Addition of metallized contacts to transistor elements.

contacts are made to a p-type region formed simultaneously with the base diffusion, as shown in Fig. 5. When capacitors are required, the oxide itself is used as a dielectric, as shown in Fig. 6.

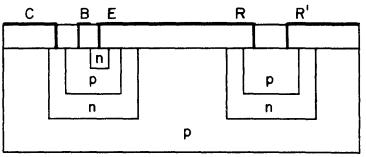


Fig. 5 — Connection of contacts to p-type region to form integrated resistor.

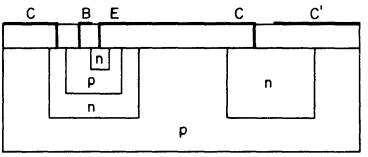


Fig. 6 — Use of oxide as a dielectric to form integrated capacitor.

Fig. 7 shows the combination of the three types of elements on a single wafer.

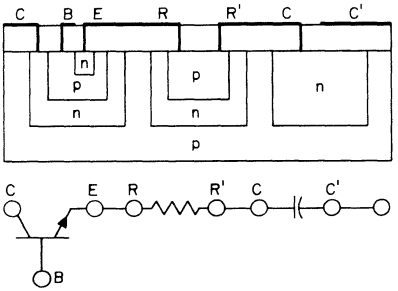


Fig. 7 — Completed silicon chip containing transistor, resistor, and capacitor.

COMPARISON OF DISCRETE AND INTEGRATED COMPONENTS

Because the basic fabrication process for integrated circuits is almost identical with that used to fabricate transistors, transistors formed by this technology are similar to discrete units. The major difference between discrete and integrated transistors is the extra capacitance associated with the substrate isolation diode.

Integrated resistors, however, are significantly different from discrete versions. Discrete resistors are normally made in standard form factors, and different values are obtained by variations in the resistivity of the material. In integrated circuits, the resistivity of the material cannot be varied to obtain different resistance values because it is determined by the optimum value required for the transistor base diffusion. The value of the resistor then depends primarily on its geometry. The resistor value R is determined by the product of its diffusion-determined sheet resistance R_s and the

ratio of its length l to its width w (i.e., $R = R_s \times l/w$). As a result, large resistors are long and narrow and small resistors are short and squat.

The value of an integrated capacitor C is equal to the product of its area A and the ratio of the dielectric constant E and the thickness d of the oxide layer (i.e., $C = A \times E/d$). Because d is kept constant, capacitor values vary directly with area.

COST FACTORS

Most of the cost of fabricating a monolithic silicon circuit is incurred in processing the silicon wafers through the various epitaxial, diffusion, and photochemistry operations. Because these costs are the same for any circuit wafer, the smaller the circuit, the more circuits that can be obtained per wafer and the lower the cost per circuit. Therefore, area minimization is an important consideration. The relative area requirements of different integrated components are as follows:

Component	*Relative Area*
Transistor	1
1000-ohm Resistor	2
10-pF Capacitor	3

These ratios are approximations that will be continually modified as technological advances are made. However, the basic relationships (that transistors use less area than resistors, which in turn are more compact than capacitors) will persist. Because area determines cost, these relationships indicate that economical integrated-circuit design requires minimization of the number of passive components. The requirement is exactly the reverse of the economic design rule for discrete-component circuits.

TEMPERATURE CONSIDERATIONS

One undesirable aspect of semiconductor resistors is their relatively large variation with temperature. This temperature dependence makes it difficult to achieve close tolerances on absolute values of resistors. However, the ratios of integrated-circuit resistors can be closely controlled by control of the geometry of photolithographic masks used in the fabrication process. As a result, it is desirable that integrated-circuit design be made dependent on ratios rather than absolute values of resistors.

Integrated transistors on the same circuit chip have a number of advantages over discrete units as a result of their proximity.

Adjacent transistors receive almost identical processing and thus are closely matched in characteristics. Because of the close spacing, minimum temperature differences occur between components and this close match is maintained over a wide operating range. In addition, integrated circuits can contain many more transistors per given area than discrete components. In a typical high-frequency silicon transistor, less than 10 per cent of the wafer area is used by the active device. The remaining area serves as a support for the bonding pads and as a "handle" for the transistor. Six integrated transistors in a circuit would use less silicon than the single discrete transistor shown in Fig. 8. Therefore, integrated-circuit

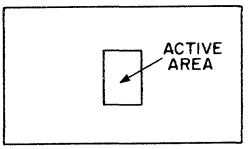


Fig. 8 — Discrete-transistor chip.

technology is most efficiently utilized when circuit designs are based on the use of a maximum number of matched active components.

BASIC DESIGN RULES

In summary, integrated-circuit technology offers the circuit designer a new approach to the synthesis of electronic functions. To use this approach most effectively, a designer should observe the following basic rules:

(a) maximize the number of active components,
(b) use resistor ratios rather than absolute values,
(c) take advantage of matched component parameters.

SELECTION OF CIRCUIT CONFIGURATIONS

Circuits intended for linear applications have a broad range of diverse design requirements and often must be essentially custom designed for the application in which they are used. In contrast, digital circuits are generally repetitive and concerned with only two levels of voltage or current and do not require accurate control of transitional-region characteristics (transconductance linearity for example). Digital circuits, therefore, can be standardized into a few basic designs and are readily adapted to integrated-circuit con-

struction techniques. Consequently, it is practical to produce such integrated circuits in large quantities, so that low-cost off-the-shelf devices are readily available to cover virtually the full range of circuit functions required for digital applications.

The variety of design requirements for linear circuits tends to prohibit standardization of circuit designs and, therefore, greatly complicates the selection of suitable configurations. The configurations chosen, in addition to being readily adapted to monolithic construction techniques, must offer widespread applicability to warrant the large-volume production required to achieve low cost per unit. Linear integrated circuits, therefore, must be either of two basic types. They can be exceptional versatile general-purpose devices that can be adapted to provide many different types of circuit functions in a variety of electronic-equipment applications. Alternatively, they may be special-purpose devices that simultaneously provide multiple circuit functions in specialized high-volume applications, such as those prevalent in the home-instrument consumer industry.

General-Purpose Circuits

The balanced differential amplifier is considered the optimum configuration for general-purpose linear integrated circuits. This circuit configuration is preferred over other possible types (a feedback pair for example) for the following reasons:

1. Advantage can be taken from the exceptional balance between the differential inputs that results from the inherent match in base-to-emitter voltage and short-circuit current gain of the two (differential-pair) transistors which are processed in exactly the same way and are located very close to each other on the same very small silicon chip.
2. The differential-amplifier circuit uses a minimum number of capacitors.
3. The use of large resistors can usually be avoided, and the gain of the differential-amplifier circuit is a function of resistance ratios rather than of actual resistance values.
4. The differential amplifier is much more versatile than other possible circuit configurations and can be readily adapted for use in a variety of equipment applications.

The differential amplifier is an ideal configuration for monolithic integrated-circuit processing, as indicated by the fact that the use of capacitors and large-value resistors can be held to a minimum. The prime reason for the selection of this circuit as the basic

configuration for RCA linear integrated circuits, however, is its exceptional versatility. The differential amplifier can provide linear amplifications from dc through the audio and video frequencies into the vhf region and may also be used for such functions as signal limiting, frequency multiplication, amplitude modulation, mixing, product detection, signal generation, gain control, squelch, and temperature compensation.

The differential-amplifier configuration inherently makes possible excellent output-to-input isolation, eliminates the need for neutralization, and simplifies feedback arrangements. The close match in temperature coefficients of components fabricated from the same material on a minute silicon chip assure stable electrical characteristics over a very broad temperature range.

For circuits intended primarily for narrow-band rf applications, the collectors of the differential pair of transistors are uncommitted, and external tuned circuits, input and output coupling networks, and feedback configurations determine, to a large extent, the operating characteristics and the type of circuit function (rf amplification, signal generation, mixing, product detection, or limiting) for which the device is to be used. For other circuits, resistors are diffused into the collector leads of the differential pair of transistors and emitter-follower or other types of transistor input and/or output stages are added to the basic differential amplifier on the same silicon chip to provide the desired input and output characteristics. Judicious use of external bias control and a few "outboarded" circuit elements permit these circuits to be adapted to perform numerous linear circuit functions. (These considerations and other factors related to the use of linear integrated circuits in practical electronic-equipment applications are discussed in subsequent chapters of this manual.)

Operational Amplifiers

An operational amplifier is basically a very-high-gain direct-coupled amplifier that uses external feedback for control of response characteristics. A common configuration for operational amplifiers is a direct-coupled cascade of two balanced differential-amplifier stages, with the second stage driven push-pull by the first stage, and an appropriate output stage. This circuit is readily adapted to integrated-circuit construction techniques.

By use of external feedback networks, the operational amplifier can be employed to synthesize a broad range of intricate transfer functions and, therefore, may be adapted for use in many widely different applications. Although this type of circuit was originally

designed to perform various mathematical functions, such as differentiation, integration, analog comparisons, and summation, it may also be used for numerous linear applications that have widely different transfer and response requirements. For example, the same operational amplifier, by modification of the feedback network, may be used to provide the broad, flat frequency-gain response required of video amplifiers or the peaked responses required of various types of shaping amplifiers. This capability makes the operational amplifier the most versatile configuration used for linear integrated circuits.

Arrays

Integrated-circuit arrays illustrate another approach to general-purpose configurations that offer widespread utility in many different types of circuit applications. Such arrays may consist of groups of unconnected active devices, of diode quads, of transistor Darlington pairs, or of individual circuit stages. The components of an array, which are fabricated simultaneously in the same way on a silicon chip, have nearly identical characteristics. The characteristics of the various components track each other with temperature variations because of the proximity of the components and the good thermal conductivity of silicon.

The integrated-circuit arrays are especially suited for applications in which closely matched device or circuit characteristics are required and in which a number of active devices must be interconnected with nonintegrable components such as tuned circuits, large-value or variable resistors, and large bypass or filter capacitors. Diode arrays, for example, are particularly useful in the design of bridge rectifiers, balanced mixers or modulators, gating circuits, and other configurations that require identical diodes. Transistor arrays make available closely matched devices that may be used in a variety of circuit applications (for example, push-pull amplifiers, differential amplifiers, multivibrators, and dual-channel circuits). The individual transistors in the array may also be employed in circuit stages that are located in different signal channels or in cascade or cascode circuits. Arrays of individual circuit stages are very useful in equipment that has two or more identical channels, such as stereo amplifiers, or they may be interconnected by use of external coupling elements to form cascade circuits.

Special-Purpose Circuits

Special-purpose linear integrated circuits are usually designed to replace several stages of discrete-component circuits in special-

ized high-volume applications. Such circuits may be intended to replace the if strips in AM or FM radio receivers, the sound circuits (if amplifier-limiters, discriminator, and audio voltage amplifiers) in intercarrier television receivers, the remote amplifier for remote-control television receivers, and similar types of specialized multi-stage circuits typical of the home-instrument consumer industry. The configurations chosen for special-purpose integrated circuits, therefore, should provide multiple circuit functions at performance levels equal to or greater than those of their discrete-component counterparts.

The high gain required of the amplifier sections of the special-purpose circuits can be provided by cascades of the balanced differential amplifier, the basic building block for most of the linear integrated circuits described in this manual. The differential amplifiers, however, must be augmented by other circuits such as voltage regulators or reference-voltage supplies, FM detectors, Darlington pairs, phase splitters, and buffer stages to provide the multiple circuit functions required in the specific application.

SUPPLY-VOLTAGE LIMITATIONS

Specifications for the maximum dc supply voltage that can be safely applied to an integrated circuit are given to ensure that voltage ratings will not be exceeded in any part of the circuit. The weak link is usually the collector-to-emitter breakdown voltage $V_{(BR)CEO}$ of the monolithic transistors. Although it is anticipated that the continuing efforts to develop improved processing techniques will result in higher breakdown levels in the future, the collector-to-emitter voltage breakdown rating for the conventional n-p-n transistors used in silicon monolithic circuits at present is typically in the range of 15 to 35 volts. This low rating substantially restricts the maximum value of dc voltage that may be safely applied to monolithic integrated circuits.

Supply voltages should be applied to monolithic integrated circuits in the usual polarity required for n-p-n transistor stages. If the polarity is reversed, the normally reversed-biased collector-to-substrate isolation junction will conduct very heavily and cause a portion of the metallization pattern to be destroyed. In battery-operated circuits, or other circuits in which supply leads could conceivably be reversed, the use of a protective diode in the dc supply line is recommended.

Any length of ribbon or wiring on a printed-circuit board has inductance that can develop significant voltages in response to high-frequency or fast-rise currents. Such voltages are added to the dc supply voltage of an integrated circuit mounted on the board. In addition, the supply-lead metallization of the integrated circuit may develop high-frequency signals as a result of stray internal feedback. Adequate compensation for both effects can be achieved by bypassing the supply leads of high-gain units with small external silvermica or high-Q-ceramic capacitors. The bypassing elements should be located as close to the integrated-circuit supply terminals as possible.

DC-LEVEL-SHIFTING REQUIREMENTS

In cascade direct-coupled amplifiers, the dc level rises through the successive stages toward the supply voltage. In linear integrated circuits, the dc voltage builds up through the n-p-n stages in the positive direction and must be shifted negatively if large output signal swings are to be obtained. In multistage high-gain integrated circuits, such as operational amplifiers and special-purpose multifunction circuits, which use external feedback to provide a wide range of gain-bandwidth and gain-stability tradeoffs, it is especially important to include provisions that compensate for the shift in dc level. Such amplifiers must have equal (preferably zero) input and output dc levels so that the dc coupling of the feedback connection does not shift any bias point.

The use of an output stage, such as that shown in Fig. 9, is a commonly used technique to prevent a shift in dc level between the output and input of an integrated circuit. Transistor Q_1 operates as an input buffer, and transistor Q_2 is essentially a current sink for Q_1. The shift in dc level is accomplished by the voltage drop across resistor R_1 produced by the collector current of transistor Q_2. The emitter of the output transistor Q_3 is connected in a bootstrap arrangement to the emitter of transistor Q_2. Feedback from this transistor through R_3 results in a decrease in the voltage drop across R_1 for negative-going output swings and an increase in this voltage drop for positive-going output swings.

If properly designed, the dc level shifting circuit shown in Fig. 9 can provide substantial voltage gain, high input impedance, low output impedance, and an output swing nearly equal to the supply voltages, in addition to the desired shift in dc level. Moreover, feedback may be coupled from this circuit to the differential-amplifier stages to compensate for dc common-mode effects that result from variations in the dc supply voltages.

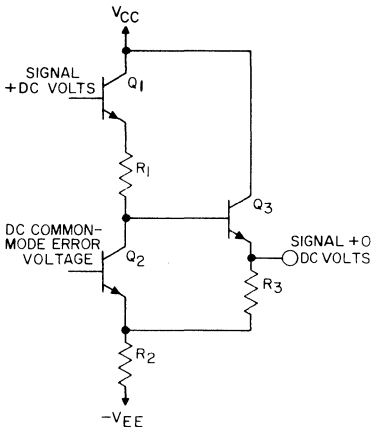


Fig. 9 — Output circuit used in linear integrated circuits to compensate for a shift in dc voltage level between output and input.

PACKAGE CONFIGURATIONS AND THERMAL CAPABILITIES

Integrated circuits are currently packaged in three distinct configurations: the TO-5-type glass-metal package, the ceramic flat pack, and the dual-in-line package. The dual-in-line package may be either ceramic or plastic. The TO-5-type package, which is an extension of the standard TO-5 transistor package, may be supplied with 8, 10, or 12 leads. The flat pack and the dual-in-line packages have 14 leads. Fig. 10 shows the different types of integrated-circuit packages.

Ceramic packages, whether flat-pack or dual-in-line types, offer the ultimate in hermeticity and package integrity, but their cost is high because of the complexity of their fabrication process. At present, dual-in-line plastic packages are achieving rapid popularity in the industry. Molded packages of this type are less costly than ceramic packages and can be readily designed to accommodate more than 14 leads.

The technique used by RCA for hermetically sealing TO-5-type packages, flat packs, and dual-in-line ceramic packages is to weld a cap onto the package in a dry-nitrogen atmosphere. Plastic packages are sealed by the plastic covering molded around the metal lead frame to which the chip is mounted. Metallization-pads-to-lead-frame connections are made with 1½-mil bonding wire. As the final steps in assembly, the circuits are subjected to a series of temperature-cycling tests and are checked for package hermeticity.

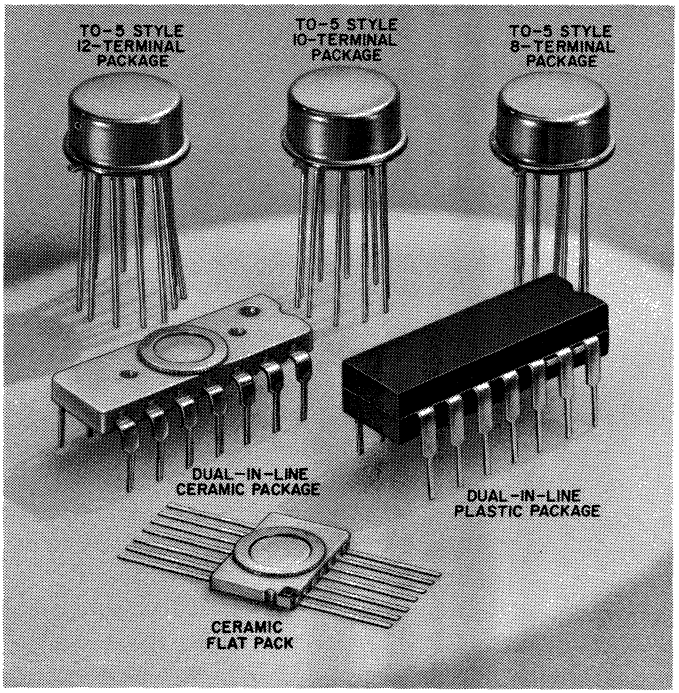


Fig. 10 — RCA integrated-circuit packages.

The basic thermal considerations for monolithic silicon integrated circuits do not differ significantly from those of discrete-components circuits. The heat dissipated by the circuit components must be transferred to the outside of the package without the temperature at any point on the circuit chip becoming excessive.

In an integrated circuit, all the heat is dissipated by active and passive components on top of the silicon chip. The heat sources, therefore, are highly localized, with the exact distribution determined by the circuit layout. Because the silicon chip mounted on a metal header is a good heat conductor, the heat rapidly diffuses throughout the chip, and the entire chip may be considered essentially isothermal. It is more meaningful, therefore, to examine the dissipation capability of the over-all chip than to determine the limits of each of the various localized regions. The dissipation capability of a monolithic silicon circuit chip is determined primarily by the encapsulation material, the chip mount, the terminating leads, and the volume and area of the integrated-circuit package.

The predominant mode of heat transfer in an integrated circuit is conduction through the silicon chip and through the case; the effects of internal free convection and radiation and lead conduc-

tion are small and may be neglected. The value of thermal resistance from pellet to case is dependent upon the pellet dimensions, the package configuration, and the location of the selected case reference point.

The maximum allowable power dissipation P_d in an integrated circuit is a function of the maximum storage temperature T_S, the maximum ambient temperature T_A, and the thermal resistance from pellet to case $\theta_{P\text{-}C}$ [i.e., $P_d = (T_S - T_A)/\theta_{P\text{-}C}$]. These parameters are usually specified in the manufacturer's published data on the integrated circuit.

For an RCA ceramic flat pack, the thermal resistance is typically 140°C per watt, the recommended maximum storage temperature is 175°C, and the recommended maximum ambient operating temperature is 125°C. For integrated circuits in TO-5-type packages, the thermal resistance is typically 140°C per watt, the recommended maximum storage temperature is 200°C, and the recommended maximum ambient temperature is 125°C. For dual-in-line packages, the thermal resistance is typically 70°C per watt for ceramic types and 150°C per watt for plastic types. The recommended maximum storage and ambient temperatures are, respectively, 85°C and 70°C for plastic packages, and 175°C and 125°C for ceramic packages.

MOUNTING AND CONNECTION TECHNIQUES

The selection of a particular method for mounting and connection of integrated circuits in equipment depends on the type of integrated-circuit package involved; on the equipment available for mounting and interconnection; on the connection method used (soldered, welded, crimped, etc.); on the size, shape, and weight of the equipment package; on the degree of reliability and maintainability (ease of replacement) required; and, of course, on cost consideration. The configuration, dimensions, and terminal arrangement for each type of RCA integrated-circuit package are shown in the *OUTLINES* section of this manual.

The sizes and shapes of the solder-pad terminations for 14-lead flat-pack integrated circuits will depend on whether "in-line" configurations or "staggered" terminal configurations are used. The sizes and shapes of pads for TO-5-type circuits will depend on the effective lead-circle diameter. In all cases the minimum permissible diameter for lead holes (after plating) is 20 mils; the maximum permissible diameter will depend on the sizes and shapes of the associated pads.

For applications in which speed and facility of installation and removal are major considerations (for example, in laboratory and testing applications), devices can be mounted in commercially available sockets. Table I lists and provides a brief description of some

Table I — *Integrated-Circuit Sockets*

Integrated-circuit Package Type	Manufacturer or Supplier	Mfr's or Supplier's Part No.	Description
14-Lead Flat Package	AMP Inc.	AMP-Crimpac▲ 583109 - 0 through 7 583110 - 0 through 7	Header (requires crimping machine) Receptacle
	Azimuth Electronics	5100-2	For use at temperatures up to 20°C
	Barnes Development Co.	MD-55	For use at temperatures up to 125°C
		MD-75	For use at temperatures up to 200°C
	Jettron Products, Inc.	71-062	Plug-in printed-circuit card
		71-005	
14-Lead Flat Package in RCA Carrier	Barnes Development Co.	029-001	For production batch testing
		029-090	For laboratory applications
14-Lead Dual In-Line (Plastic or Ceramic)	Augat, Inc.	314-AG10	For printed circuit boards
		314-AG3A	For chassis mounting
		114-AG1B	High-temperature Teflon, for chassis mounting
		114-AG1A	High-temperature Teflon*, for printed-circuit boards
	Barnes Development Co.	MGL-14	
8-Lead TO-5 Style	Augat, Inc.	8058-1G19	Miniature-type, Teflon, for chassis mounting
		8058-39G3	Miniature-type, Teflon, for printed-circuit boards
	Barnes Development Co.	MG-802	Miniature-type, Teflon
		MGR-81	Miniature-type, Teflon, for printed-circuit boards
		MF02-8	For chassis mounting
		MF03-8	For printed-circuit boards
10-Lead TO-5 Style	Augat, Inc.	8058-1G22	Miniature-type, Teflon, for chassis mounting
		8058-2HG1	Miniature-type, Teflon, for printed-circuit boards
	Barnes Development Co.	MG1002	Miniature-type, Teflon
		MGR102	Miniature-type, Teflon, for printed-circuit boards
		MF02-10	For chassis mounting
		MF03-10	For printed-circuit boards
	Sealectro Corp.	Series 60	Press-fit# type, Teflon
12-Lead TO-5 Style	Barnes Development Co.	MG1201	Miniature-type, Teflon
		MGR121	Miniature-type, Teflon, for printed-circuit boards
		MF02-12	For chassis mounting
		MF03-12	For printed-circuit boards
	Sealectro Corp.	Series 60	Press-fit type, Teflon

Registered Trade Mark, Sealectro Corporation. ▲ Registered Trade Mark, AMP Incorporated.
* Registered Trade Mark, E. I. DuPont De Nemours & Co.

commercially available sockets for integrated circuits by manufacturers' and/or suppliers' parts numbers. This list is based on manufacturers' and/or suppliers' published information and is not necessarily complete. Sockets having mechanical and electrical characteristics comparable with those of the devices listed may also be available from other manufacturers and/or suppliers of electronic components.

Ceramic Flat Packs

The RCA 14-lead ceramic flat-pack integrated circuits may be interconnected with other circuit elements by a variety of soldering or welding techniques in any one of three basic mounting arrangements. These various techniques are described and the relative merits of each type are discussed in the following paragraphs:

Soldering Techniques — Fig. 11 shows five methods for making soldered connections to RCA integrated circuits in 14-lead flat-packages. In the "straight-through" method, Fig. 11(a), the leads are bent downward at a 90° angle and inserted in 24-mil diameter holes in the printed-circuit board. Connections to all 14 leads may be made simultaneously in a dip-soldering or wave-soldering operation. To insure good solder-fillet formation around the lead ends, the leads should extend approximately 15 to 30 mils below the bottom of the circuit board. To insure that the holes will be filled with solder to form good electrical connections, the holes must be "plated-through." Replacement of the package can be accomplished by melting and removing the solder around each lead by means of a "solder gobbler."

A disadvantage of the straight-through method is that the integrated-circuit package must be held firmly in position during the soldering operation. Another disadvantage is that the clearance between the lead and the hole is critical. Optimum "wicking" in dip or wave soldering is achieved when the lead has a circular cross-section and a diameter 6 mils less than the lead hole.

The "clinched-lead full-pad" method shown in Fig. 11(b) requires an additional operation (clinching of the lead), but has the advantage that the integrated-circuit package does not have to be held in position during the soldering operation. This method also has these additional advantages over the straight-through method: (1) because the electrical connection is made on the pad, the hole-to-lead-diameter ratio is not critical, and the lead holes therefore can be larger — a feature which simplifies insertion of the leads; (2) the solder connections are more reliable (because of the larger wetted area, and better mechanical contact); (3) plating of the holes

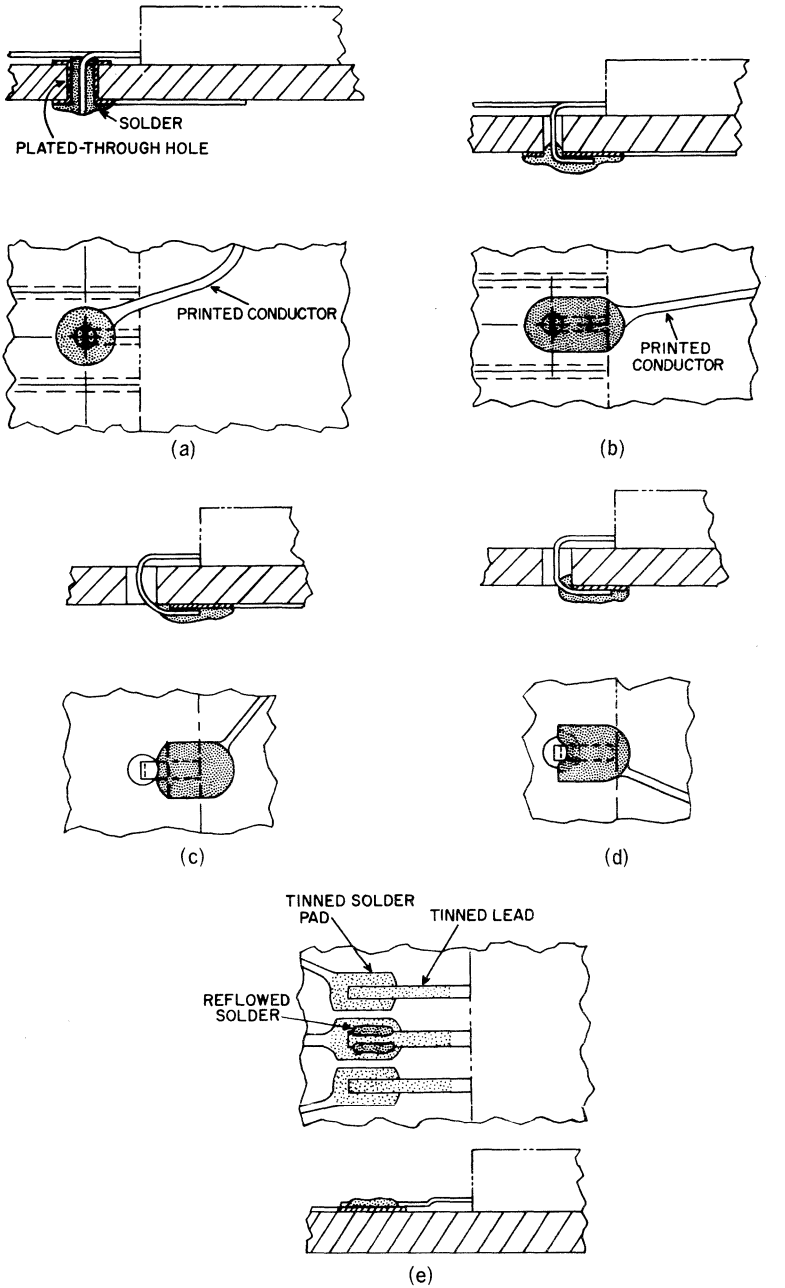


Fig. 11 — Interconnection methods for RCA 14-terminal ceramic flat packs: (a) straight-through method; (b) clinched-lead full-pad method; (c) clinched-lead offset-pad method; (d) clinched-lead half-pad method; (e) surface connection method (reflow soldering).

is neither necessary nor desirable (non-plated holes retain less solder and the integrated circuit may, therefore, be more easily removed if replacement is necessary).

The "clinched-lead offset-pad" method shown in Fig. 11(c) and the "clinched-lead half-pad" method shown in Fig. 11(d) are variations of the clinched-lead full-pad method that provide greater maintainability because the lead holes are free of solder and only partially filled with solder, respectively; the device therefore, can be more easily removed if replacement is necessary. The reliability of these connections probably is not as great as that of the clinched-lead full-pad type shown in Fig. 11(b).

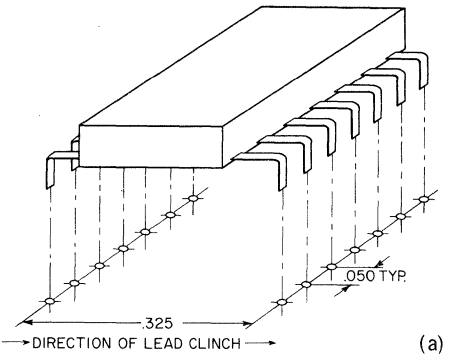
In the "surface-connection" method shown in Fig. 11(e), the connections are made on the package side of the printed-circuit board. This method has the following advantages: (1) drilling of the circuit board is not required; (2) bending or special forming of the integrated circuit leads is minimized; (3) higher component packing densities are practicable because components may be mounted on both surfaces of the printed-circuit board.

A disadvantage of the surface-connection method is that dip- or wave-soldering cannot be used. However, multi-lead "reflow soldering" systems are available in which all seven leads on one edge of a 14-lead flat package can be soldered simultaneously. Another disadvantage of the surface-connection method is that the integrated-circuit package must be held in position during the soldering operation.

Mounting Patterns — The mounting patterns shown in Fig. 12 employ "in-line" lead and pad arrangements. Although such in-line lead and pad arrangements simplify lead-forming requirements, they result in very close spacing between leads (approximately 32 mils), and require the use of high-precision manufacturing techniques, in both board manufacture and assembly, particularly when the leads must be inserted through holes in the printed-circuit board, as in Fig. 11(a) through 11(d). Another disadvantage of the in-line arrangement is the limited space available for routing circuit conductors between adjacent solder pads.

Some of these disadvantages can be overcome by the use of "staggered" lead arrangements, as shown in Fig. 13. In these staggered arrangements, the lead holes and terminal pads for adjacent leads on the same edge of a flat package are offset by some convenient distance from the in-line axis. Although a staggered lead arrangement requires somewhat more circuit-board area per device than the in-line arrangement, it provides several advantages: (1) tolerances are far less critical, (2) larger terminal

pads can be used, (3) even with larger pads more space is available for routing circuit conductors between adjacent terminal connections, and (4) larger lead holes can be used to simplify lead insertion.



SUGGESTED MINIMUM PAD SIZES (INCHES)	HOLE DIA. (INCHES) after plating	REMARKS
.0375 .042 .075	.020 min.	For use at points of clinched lead attachment
.050	.020 min.	For non-adjacent plated through hole terminal areas
.050 .042	.020 min.	For adjacent terminal areas on .050 centers when clinched lead attachment is not used (shaved .050 dia. pad)

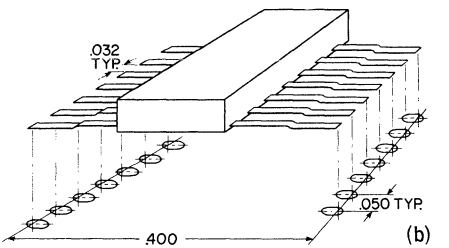
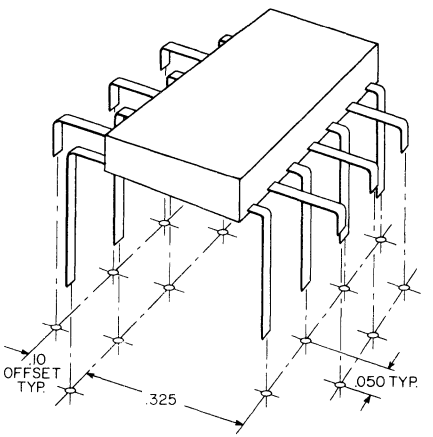


Fig. 12 — In-line lead and terminal arrangements for RCA 14-terminal flat packs: (a) through-the-board mounting method; (b) surface mounting method.

In a staggered lead arrangement a good compromise between loss of available circuit-board area and gain in the number of conductors that can be routed between adjacent circular terminal pads can be achieved by the use of a 100-mil offset between adjacent pads. With this combination standard manufacturing tolerances are applicable, and a 10-mil annular surface (a practicable minimum) is provided on each solder pad.

A staggered terminal arrangement can provide great flexibility in circuit wiring configurations. If offset lead holes 30 mils in diameter and circular solder pads 80 mils in diameter are used, at least one 8-mil-wide printed conductor can be routed between adjacent solder pads. If 60-mil diameter solder pads are used, up to two 8-mil-wide printed conductors can be routed between adjacent pads.



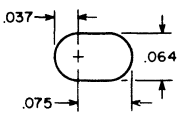
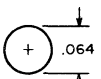
SUGGESTED MINIMUM PAD SIZES (INCHES)	HOLE DIA. (INCHES)	REMARKS
	.030 ± .003	For use at points of clinched lead attachment
	.030 ± .003	For terminal areas not used for clinched lead attachments

Fig. 13 — Staggered-lead mounting arrangement for RCA 14-terminal flat packs.

The maximum offset that can be achieved with RCA 14-lead flat-pack integrated circuits is 150 mils, based on a lead length of ¼ inch. When this maximum offset is used, only the straight-through type of connection shown in Fig. 11(a) is practicable.

Welded Connection Techniques — For some applications of integrated circuits, it may be necessary or desirable to use welded rather than soldered connections to the devices. Fig. 14 shows three methods which may be used for making such welded connections. In general, the mechanical space considerations described above for soldered connections (lead bending, tolerances, etc.) apply equally for welded connections.

Although for some applications welding may provide more reliable connections than soldering, it has the disadvantage that with conventional welding equipment only one connection can be made at a time.

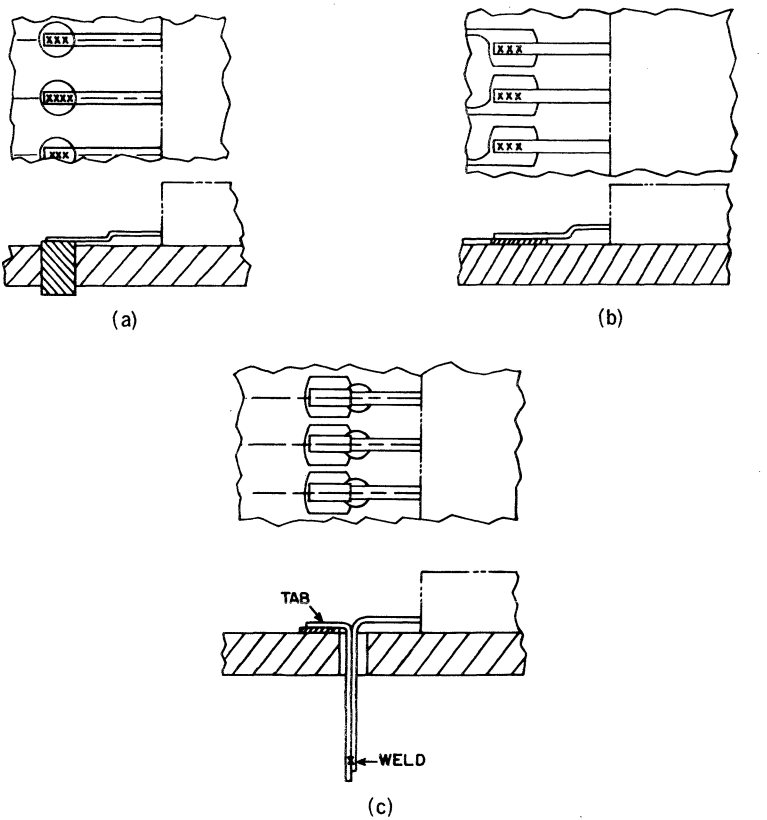


Fig. 14 — Welded connection methods for mounting RCA 14-terminal flat packs: (a) post method; (b) surface-pad method; (c) tab method.

The "Tab" method shown in Fig. 14(c) provides a high degree of maintainability, because the integrated circuit can be easily removed, if replacement becomes necessary. This method employs "cross-wire" resistance welding, in which the weld is made at the ends of the device lead and the terminal tab. The device can thus be removed simply by clipping the leads just above the weld points. This method, however, requires that terminal tabs and solder pads be provided on the printed-circuit board.

TO-5-Type Packages

The most direct method for mounting RCA integrated circuits in 8-lead, 10-lead, and 12-lead TO-5-type packages is shown in Fig. 15(a). In this method, the leads of the device are simply inserted in the proper plated-through holes in the printed-circuit board and connection is completed by dip- or wave-soldering.

Although this method of mounting requires minimum handling of the device (trimming of terminal leads to appropriate lengths may be necessary), it does require extremely precise drilling and "through-plating" of the lead holes and preparation of solder pads on a 230-mil diameter circle. It also has the disadvantages that automatic insertion of the device leads in such limited space can present problems, and that the device must be held in position during the soldering operation.

The method shown in Fig. 15(a) and the radially-offset method shown in Fig. 15(b) both make it possible to achieve effective "wicking" because they provide a nearly optimum relationship between lead diameter (18 mils) and lead-hole diameter (24 mils).

Fig. 15(c) shows variations of the method shown in Fig. 15(b), in which the holes are not plated through and the leads are clinched before the soldering operation is performed. Because the electrical connection depends on the solder on the pad and not on the solder in the hole, the lead-hole diameter can be made larger and therefore, permits easier lead insertion. Furthermore, the clinching of the leads helps to hold the device in position during soldering. Fig. 16 shows the lead hold arrangement for Straight-Through mounting of the 10-lead TO-5-type package. This arrangement, using 60-mil diameter pads, provides only 11 mils clearance between adjacent pads, the smallest clearance practicable without danger of shorting. This separation is insufficient to accommodate a printed conductor of conventional width. It is evident that with a 12-lead TO-5-type package, the spacing between adjacent pads on a 230-mil circle will be even smaller.

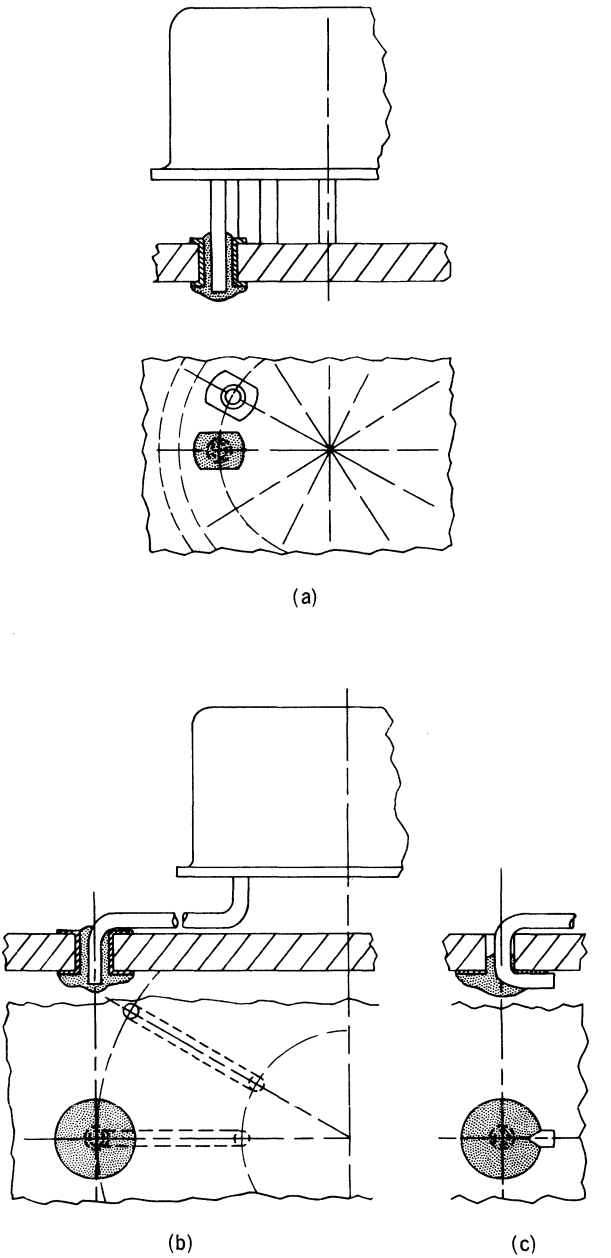


Fig. 15 — Mounting methods for RCA TO-5 style packages: (a) straight-through method; (b) straight-through method with leads radially offset; (c) radially offset leads with clinched-lead option.

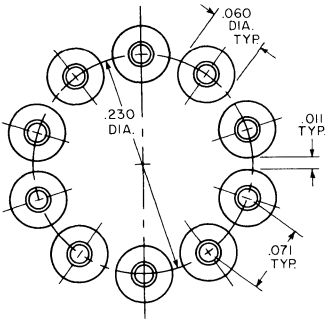


Fig. 16 — Lead-hole circle pattern for RCA 10-terminal TO-5 style package.

Fig. 17 shows a lead-circle pattern for a 12-lead TO-5-type package in which the leads are formed to increase the effective lead-circle diameter to 530 mils. This configuration permits the use of 80-mil diameter pads with sufficient spacing between pads to accommodate three eight-mil-width printed conductors. This radially offset lead-hold pattern also permits clinched-lead mounting, and represents a good compromise from the standpoints of mounting arrangement, reliability, maintainability, and cost.

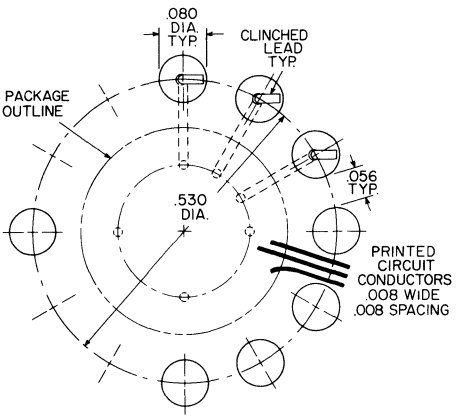


Fig. 17 — Radially offset mounting pattern for RCA 12-terminal package

Dual-In-Line Packages

Fig. 18 shows the mounting arrangement used for integrated-circuits in dual-in-line packages. Because the package configurations are very similar, the mounting arrangement and terminal-sorting techniques used for these circuits are much the same as those used,

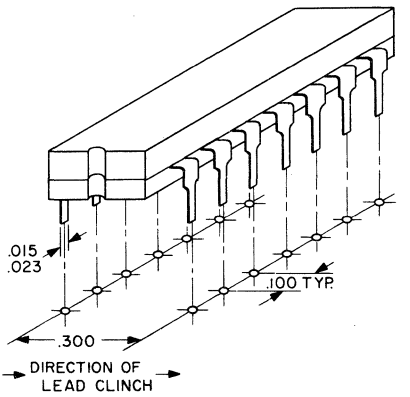


Fig. 18 — Mounting arrangement for RCA dual-in-line packages.

in the in-line method [shown in Fig. 12(a)], for the flat-pack circuits. The dual-in-line circuit is longer, however, and the soldering operation is made simpler because of the greater spacing provided between lead terminals.

The terminals of the dual-in-line package may be soldered to a printed board by use of any of the through-the-board techniques [shown in Figs. 11(a) through 11(d)] used for the in-line method of mounting the ceramic flat packs. The terminal leads of the dual-in-line package, however, are larger than those of flat pack. The diameter of the mounting holes drilled through the printed-circuit board must be increased to a minimum value (after plating) of 0.032 inch. The larger-size terminals are advantageous in that the increased rigidity that results enables them to be inserted more easily into the mounting holes in the printed-circuit board, or in integrated-circuit sockets.

Another significant feature of the terminals for the dual-in-line package is the sharp step increase in width near the package end. This step forms a shoulder upon which the package rests when mounted on the board; the package, therefore, is not mounted flush against the board. As a result, it is possible to run printed-circuit wiring directly under the package, convection cooling is increased, and the circuit can be more easily removed if a replacement is required.

Lead Bending and Forming Considerations

In any method of mounting integrated circuits which involves bending or forming of the device leads, it is extremely important that the leads be supported and clamped between the bend and the

seal, and that bending be done with extreme care to avoid damage to lead plating. In no case should the radius of the bend be less than the diameter of the lead, or in the case of rectangular leads such as those used in RCA 14-lead flat-packaged integrated circuits, less than the lead thickness. It is also extremely important that the ends of the bent leads be perfectly straight and parallel to assure proper insertion through the holes in the printed-circuit board.

Bending, forming, and clinching of integrated-circuit leads produce stresses in the leads and can cause stresses in the seals if precautions are not taken. In addition, wide variations in temperatures during normal use result in stresses in these devices. Tests of 14-lead flat-pack integrated circuits conducted under worst-case conditions, in which the packages were rigidly attached to posts extending from the printed-circuit board, showed that over a temperature swing of 180°C (from — 55°C to + 125°C) the stress developed in the leads, the tensile pull on the leads, the shear stress introduced in the seal, and the tensile stress developed in the seal were all well within the limits for these materials. The use of thermal stress-relief bends is, therefore, not necessary.

Lead bending and forming requirements for both flat-pack and TO-5-type packages are shown in Fig. 19.

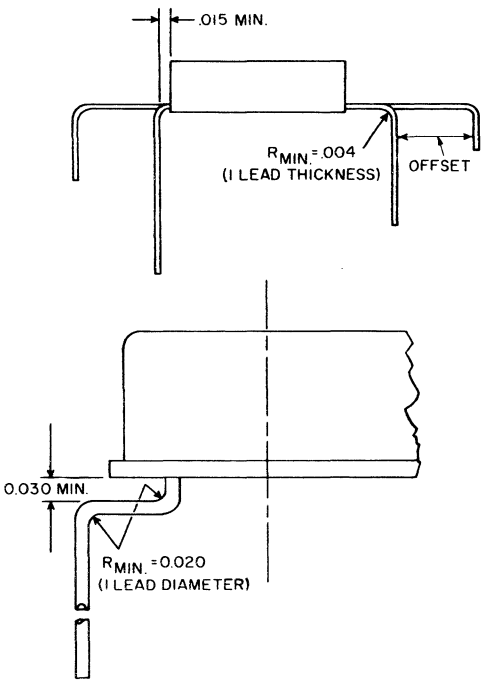


Fig. 19 — Lead-forming requirements for RCA integrated-circuit packages.

Basic Differential-Amplifier Configuration for Linear Integrated Circuits

The balanced differential amplifier shown in Fig.20 is the basic circuit configuration used for a broad line of all-monolithic-silicon integrated circuits designed for a wide variety of linear applications at frequencies from dc into the vhf region. The currents to the emitter-coupled pair of transistors are supplied from a controlled

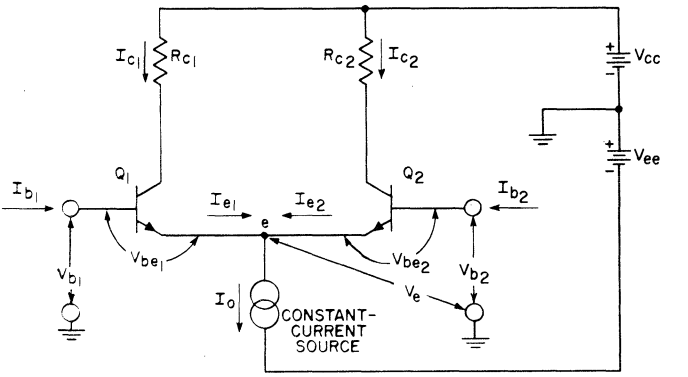


Fig. 20 — Schematic of the balanced differential amplifier used as the basic configuration for the linear integrated circuits.

source (i.e., a constant-current-sink transistor). Temperature-compensating networks can be readily incorporated as an integral part of the controlled-source circuit to assure that circuit gain, dc operating point, and other important characteristics vary as required over the operating temperature range (— 55°C to + 125°C).

CHARACTERISTICS OF THE BASIC INTEGRATED-CIRCUIT DIFFERENTIAL AMPLIFIER

As indicated in Fig.20, the integrated-circuit differential amplifier is usually operated from dual dc supply voltages, $+ V_{CC}$ and

$-V_{EE}$, applied in the normal polarities used for n-p-n transistors. Single-supply operation is also feasible, but requires an external voltage divider network and an additional bypass element. Single-ended outputs may be coupled from the collector of either transistor of the differential pair, or the amplifier may be used to provide double-ended outputs with the load circuit connected between the collectors of the two transistors.

The pair of integrated-circuit transistors (Q_1 and Q_2) behave in the same way as do a pair of discrete n-p-n transistors operated in a similar type of circuit configuration. A positive-going signal applied to the base of either transistor Q_1 or Q_2 tends to increase the current through the transistor. Because of the signal interaction that results from the emitter-coupled arrangement, however, the effective drive for the differential amplifier is the algebraic difference of the input voltages applied to the bases of the differential pair of transistors. When the base of transistor Q_1 is driven positive with respect to the base of transistor Q_2, the differential input voltage is considered to be positive. For this condition, the current through Q_1 increases, and the current through Q_2 decreases. Conversely, a reversal in the polarity of the differential input voltage results in a decrease in the current through Q_1 and an increase in the current through Q_2.

Differential Input Voltage

In the differential-amplifier circuit shown in Fig.20, the sum of the emitter currents of the differential pair of transistors Q_1 and Q_2 must be equal to the total amount of current (I_o) supplied to the constant-current sink, as shown by the application of Kirchoff's second law at node e:

$$I_{e1} + I_{e2} = I_o \tag{1}$$

The emitter-to-base voltages V_{be1} and V_{be2} of the emitter-coupled transistors Q_1 and Q_2 are expressed as follows:

$$V_{be1} = V_{b1} - V_e \tag{2}$$

$$V_{be2} = V_{b2} - V_e \tag{3}$$

where V_e is the voltage at the node e and V_{b1} and V_{b2} are defined as indicated in Fig. 20.

If the V_e term is eliminated in Eqs. (2) and (3), the following result is obtained:

$$V_{b1} - V_{b2} = V_{be1} - V_{be2} \tag{4}$$

This latter equation defines the differential input voltage for the differential amplifier.

Transfer Characteristics

The familiar equations for the current relationships in a transistor and for the voltage across the base-emitter diode are employed in the derivation of the transfer characteristics of the differential-amplifier circuit.

The basic transistor current relationships are expressed by the following equations which define the collector (I_c) and base (I_b) currents of transistors Q_1 and Q_2 in terms of their emitter current (I_e):

$$\begin{aligned} I_{c1} &= \alpha I_{e1} \\ I_{c2} &= \alpha I_{e2} \end{aligned} \tag{5}$$

$$\begin{aligned} I_{b1} &= (1 - \alpha)\, I_{e1} \\ I_{b2} &= (1 - \alpha)\, I_{e2} \end{aligned} \tag{6}$$

where alpha (α) is the fractional part of the emitter current that reaches the collector of the transistor. In this discussion, alpha is assumed to be the same for both transistors (Q_1 and Q_2) of the differential pair.

The base-emitter diode equation relates the base-to-emitter voltage (V_{be}) of a transistor to the emitter current (I_e) as follows:

$$I_e = I_s \left(\exp \frac{V_{be}}{h} - 1 \right) \tag{7}$$

where I_s is the saturation current of the transistor, and h is defined by the ratio KT/q where K is Boltzmann's constant, T is the temperature in degrees Kelvin, and q is the charge on an electron. At 300°K, a saturation current I_s in the order of 0.2×10^{-15} ampere is typical for some integrated-circuit transistors, and the factor h is approximately 26 millivolts.

For emitter currents of 1 nanoampere or more, the -1 term in the bracketed expression of Eq. (7) becomes insignificant, and the equation can be rewritten for the integrated-circuit transistors Q_1 and Q_2, respectively, as follows:

$$I_{e1} = I_{s1} \exp \frac{V_{be1}}{h} \tag{8}$$

$$I_{e2} = I_{s2} \exp \frac{V_{be2}}{h} \tag{9}$$

If the two transistors Q_1 and Q_2 are assumed to be identical, the following basic equalities can also be assumed:

$$\begin{aligned} I_{s1} &= I_{s2} = I_s \\ \alpha_1 &= \alpha_2 = \alpha \\ T_1 &= T_2 = T \end{aligned} \tag{10}$$

On the basis of the relationships expressed by Eqs. (4) through (10), Eq. (1) can be rewritten as follows:

$$\begin{aligned} I_o &= I_s \exp \frac{V_{be1}}{h} + I_s \exp \frac{V_{be2}}{h} \\ &= I_s \exp \frac{V_{be1}}{h} \left(1 + \exp \frac{V_{b2} - V_{b1}}{h}\right) \end{aligned} \tag{11}$$

Eqs. (8) and (9) can then be rewritten to express the emitter currents I_{e1} and I_{e2} in terms of the total source current I_o as follows:

$$I_{e1} = \frac{I_o}{1 + \exp \dfrac{V_{b2} - V_{b1}}{h}} \tag{12}$$

$$I_{e2} = \frac{I_o}{1 + \exp \dfrac{V_{b1} - V_{b2}}{h}} \tag{13}$$

The collector currents I_{c1} and I_{c2}, given by Eq. (5), may also be defined in terms of the current I_o, as follows:

$$I_{c1} = \frac{\alpha I_o}{1 + \exp \dfrac{V_{b2} - V_{b1}}{h}} \tag{14}$$

$$I_{c2} = \frac{\alpha I_o}{1 + \exp \dfrac{V_{b1} - V_{b2}}{h}} \tag{15}$$

The collector-current transfer curves defined by Eqs. (14) and (15) are shown in Fig. 21 In this figure, the abscissa represents the differential input voltage $V_{b1} - V_{b2}$ and is calibrated in units of the factor $h = KT/q$. The ordinate, which represents the collector current I_c, is calibrated in units of αI_o.

When V_{b1} is equal to V_{b2}, the two transistors Q_1 and Q_2 are balanced, and one-half the total current I_o flows through each transistor. This condition presents the usual operating point for an analog differential amplifier.

The transfer curves shown in Fig. 21 provide several important points of information about the differential amplifier:

1. The transfer characteristics are linear in a region about the operating point. For the curves shown (KT/q ≈ 26 millivolts), this linear region corresponds to an input-voltage swing of approximately 50 millivolts peak-to-peak.
2. The maximum slope of the curves, which occurs at the operating point, defines the effective transconductance of the differential amplifier.
3. The slope of the transfer curves (i.e., the transconductance) is dependent upon the value of the total current I_0 supplied to the constant-current sink. The slope of the

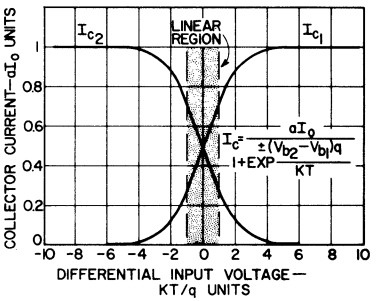


Fig. 21 — Transfer characteristics of the basic differential-amplifier circuit.

transfer curves can be changed, without changing the linear input region, by varying the value of I_0. This relationship implies that automatic gain control is inherent in the differential amplifier when the current I_0 is controlled.

4. The transfer characteristics and the slopes of these characteristics are a function of the alpha of the transistors and of the temperature, both of which are predictable, and of two physical constants.
5. The differential amplifier is a natural limiter; when input excursions exceed ±4KT/q (approximately ±100 millivolts for the curves shown), no further increase in the output is obtained.
6. The output current of an amplifier is the product of the input voltage and the transconductance. In the differential amplifier, the transconductance is proportional to the

controlled current I_o; this circuit, therefore, may be used for mixing, frequency multiplication, modulation, or product detection when the current I_o is made a multiplicand and the input waveform is the multiplier.

Transconductance Characteristics

As mentioned in the preceding paragraph, the slope of either of the transfer curves shown in Fig. 21 defines the transconductance of the differential amplifier. The transfer equation [Eq. (14) or Eq. (15)] can be differentiated, therefore, to obtain the general equation for the transconductance g_m as a function of the input voltage $V_{b1} - V_{b2}$. The following result is obtained:

$$\frac{di_c}{de_b} = g_m = \frac{\alpha \frac{I_o}{h} \exp \frac{e_b}{h}}{\left(1 + \exp \frac{e_b}{h}\right)^2} \tag{16}$$

where e_b represents $V_{b1} - V_{b2}$ and h is again equal to KT/q.

When the transconductance is evaluated at the operating point ($e_b = 0$), Eq. (16) reduces to

$$g_m = \frac{q\alpha I_o}{4KT} \tag{17}$$

Eq. (17) reveals that, for the same value of source current I_o, the effective transconductance of the differential amplifier is one-fourth that of a single transistor. This condition results from the fact that, at the operating point, exactly one-half of the total current I_o flows through each transistor of the differential pair and the input voltage must be divided equally between the two transistors.

When the differential amplifier is operated to provide double-ended outputs so that the output voltage is measured between the collectors of the differential pair of transistors, the output currents through the load impedance contribute equally to the output voltage from each transistor. As a result, the output voltage is twice that obtained for single-ended operation. This increase in output voltage results because the load impedance is doubled, not because of any doubling of the transconductance. However, if an impedance is connected between the two collectors and the shunt collector-feed resistors are large compared to this load impedance, the load current is twice as large as can be expected from a single-ended circuit. This condition indicates an

apparent effective transconductance, $g_{m\,(app)}$, for the double-ended circuit which is expressed by the following equation:

$$g_{m\,(app)} = \frac{q\alpha I_o}{2KT} \tag{18}$$

EFFECT OF EMITTER DEGENERATION ON DIFFERENTIAL-AMPLIFIER CHARACTERISTICS

Fig. 22 shows a curve of transconductance as a function of differential input voltage $V_{b_1} - V_{b_2}$ as obtained from Eq. (16). A study of this curve indicates that it may be desirable to increase

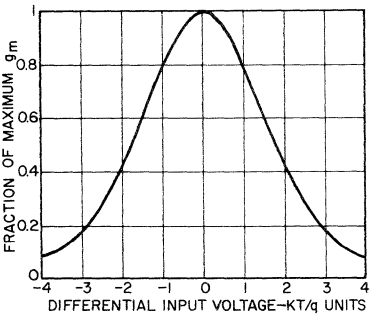


Fig. 22 — Transconductance of the basic differential amplifier as a function of the differential input voltage.

the range of linearity of the transconductance and, thus, suggests the use of emitter degeneration. Fig. 23 shows the basic differential amplifier with two identical emitter resistors (R_e) added. The degeneration introduced by the emitter resistors reduces the gain (transconductance) of the differential pair of transistors, but it also increases the linearity of both the transfer characteristics and the transconductance.

The combination of the nonlinear circuit characteristics and the linear emitter resistors does not lend itself immediately to a facile mathematical solution. A new transfer curve, which is a function of the actual level of the current I_o and the value of the emitter resistance R_e, can be constructed more easily by graphical techniques. The new transfer curve, shown in Fig. 24, is obtained from the addition, at a constant current, of the original differential-amplifier voltage drop and the voltage drop across the emitter resistor.

When the effects of two equal emitter resistors (used as

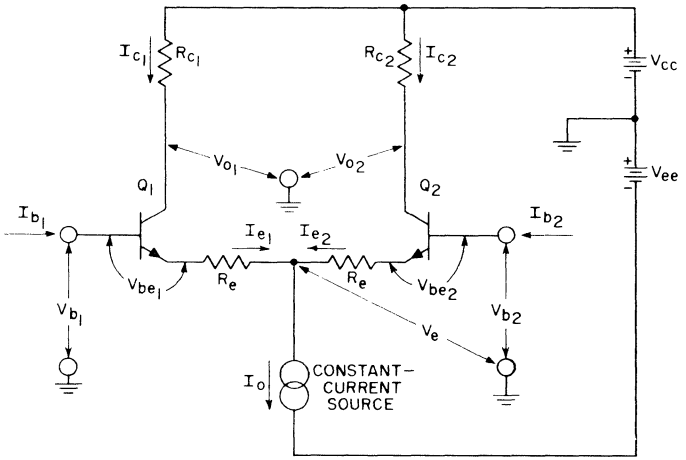


Fig. 23 — Schematic of the basic differential amplifier in which emitter degeneration is employed.

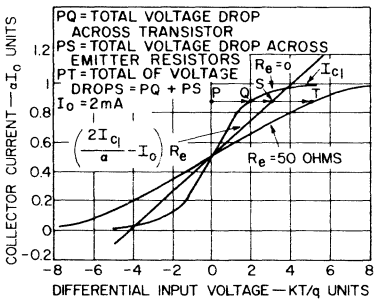


Fig. 24 — Effect of emitter degeneration on the transfer characteristics of the basic differential amplifier.

shown in Fig. 23) are considered, it is apparent that the differential input voltage must include the ohmic differential voltage drop across the two resistors. This ohmic voltage-drop component, $V_{Re_1} - V_{Re_2}$, can be expressed as follows:

$$V_{Re_1} - V_{Re_2} = I_{e_1} R_e - I_{e_2} R_e \tag{19}$$

If the relationship expressed by Eq. (1) is used, Eq. (19) becomes

$$V_{Re_1} - V_{Re_2} = (2I_{e_1} - I_o) R_e \tag{20}$$

or

$$V_{Re_1} - V_{Re_2} = (I_o - 2I_{e_2}) R_e \tag{21}$$

Eq. (20), which expresses the ohmic differential voltage drop in terms of the emitter current of transistor Q_1, may be rewritten to express this voltage drop in terms of the transistor collector current, as follows:

$$V_{Re1} - V_{Re2} = \left(\frac{2I_{c1}}{\alpha} - I_o\right) R_e \qquad (22)$$

where I_{c1} is defined as indicated in Eq. (5).

Eq. (22) is represented graphically by the straight line in Fig. 24, which gives the IR drop as a function of the differential input voltage for the circuit shown in Fig. 23 at a constant current I_o of 2 milliamperes.

When emitter resistors are used, therefore, the new transfer characteristics for a differential amplifier can be determined for any given value of the current I_o by addition of the voltage drops of the differential amplifier to those of the emitter resistors. Thus, at the current value P in Fig. 24, the voltage drop across the differential pair of transistors is PQ and that across the emitter resistors is PS. The point on the combined transfer curve that corresponds to these conditions is PQ + PS = PT.

This simple graphical addition of voltages at various current levels suggests a mathematical approach that may be used to determine the effects that the degeneration introduced by emitter resistors has on transconductance. In this approach, the transistor current relationship given by Eq. (13) or Eq. (14) is first solved for the differential input voltage $V_{b1} - V_{b2}$. In this inverted form, Eq. (14) becomes

$$V_{b1} - V_{b2} = -h \ln\left(\frac{\alpha I_o}{I_{c1}} - 1\right)$$

This expression for $V_{b1} - V_{b2}$, however, does not include the ohmic differential voltage drop across the emitter resistors. When this voltage $V_{Re1} - V_{Re2}$, as given by Eq. (22), is added, the equation for $V_{b1} - V_{b2}$ becomes

$$V_{b1} - V_{b2} = -h \ln\left(\frac{\alpha I_o}{I_{c1}} - 1\right) + \left(\frac{2I_{c1}}{\alpha} - I_o\right) R_e \qquad (23)$$

The derivative of Eq. (23) is then taken to obtain the following relationship:

$$\frac{d(V_{b1} - V_{b2})}{dI_{c1}} = h\left(\frac{\alpha I_o}{I_{c1}^2}\right)\left(\frac{I_{c1}}{\alpha I_o - I_{c1}}\right) + \frac{2R_e}{\alpha} \qquad (24)$$

At the operating point ($I_{c1} = \alpha I_o/2$), Eq. (24) reduces to

$$\frac{d(V_{b1} - V_{b2})}{dI_{c1}} = \frac{4h}{\alpha I_o} + \frac{2R_e}{\alpha} = \frac{4KT}{\alpha q I_o} + \frac{2\,R_e}{\alpha} \tag{25}$$

The reciprocal of this derivative is the effective transconductance, g_m', of the differential amplifier when emitter resistors are used, as given by

$$g_m' = \frac{1}{\frac{\alpha}{g_m} + \frac{2\,R_e}{\alpha}} = \frac{\alpha g_m}{\alpha^2 + 2R_e g_m} \tag{26}$$

where g_m is the transconductance of the basic differential amplifier at the operating point, as defined by Eq. (17).

Because α is approximately unity, Eq. (26) is usually simplified to the following form:

$$g_m' \approx \frac{g_m}{1 + 2R_e g_m} \tag{27}$$

For a differential amplifier having an original transconductance (g_m) of 20×10^3 micromhos, as would be expected for a current I_o of 2 milliamperes, the effective transconductance (g_m') becomes approximately one-third the original value when emitter resistors (R_e) of 50 ohms are used.

The transconductance curves for a differential amplifier which employs emitter degeneration may be constructed as follows: First, the reciprocal of Eq. (24) is taken to obtain the transconductance as a function of the current. The differential input voltage that corresponds to the current is then obtained from Eq. (23). Fig. 25 shows transconductance curves constructed

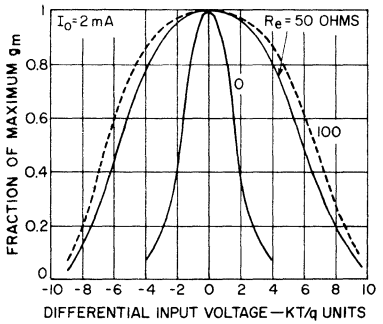


Fig. 25 — Effect of emitter degeneration on the transconductance of the basic differential amplifier.

in this manner for the differential amplifier shown in Fig. 23. These curves show the variation in transconductance as a function of the differential input voltage for emitter resistors (R_e) of 50 ohms and of 100 ohms. For comparison, the normalized transconductance of the circuit when no emitter resistors are used is also shown on the same scale.

The increased linearity of the transconductance characteristic that results from the degeneration introduced by the emitter resistors is evident from the curves shown in Fig. 25. This increased linearity, however, is accompanied by a reduction in the absolute value of the transconductance. As mentioned previously, the use of 50-ohm emitter resistors reduces the absolute value of transconductance to one-third the original value (for an I_o of 2 milliamperes). The use of 100-ohm emitter resistors further reduces the transconductance by approximately 40 per cent.

The preceding discussion has shown that the introduction of emitter degeneration decreases the slope of the transfer characteristics (results in a more linear transconductance) and reduces the sharpness of the cutoff "knee." As a result of these factors, a higher input voltage is required to produce distortion or limiting in the differential amplifiers when emitter resistors are used.

Experimental confirmation of the change in transfer characteristics that results from the use of emitter resistors is provided by the calculated and measured data shown in Fig. 26. The coordinate plane on the right shows one-half of the transfer curves obtained when no external emitter resistors are used. The co-

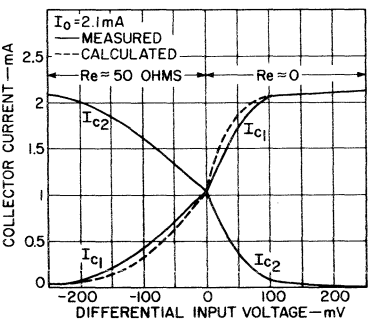


Fig. 26 — DC characteristics of the basic differential amplifier with and without emitter degeneration for a source current of I_o of 2.1 milliamperes.

ordinate plane on the left shows one-half the transfer curves obtained when emitter resistors having a nominal value of 50 ohms are included in the differential amplifier.

The theoretical (calculated) curves shown in Fig. 26 are graphical representations of Eqs. (14) and (23). The small differences between the measured and theoretical curves can be attributed to the few ohms of emitter-contact and bulk resistance inherent in the transistor. The exact amount of this emitter resistance can best be calculated from measured transconductance curves since measurements of slopes on curves such as those shown in Fig. 26 are not highly accurate.

The effect of the absolute value of the total current I_o on the transfer and transconductance characteristics, when a fixed-value emitter resistor is used, is also an important consideration in the differential-amplifier integrated circuit. This effect is illustrated in Fig. 27, which shows the dc transfer characteristics at a current I_o of 0.188 milliampere, rather than at an I_o of 2.1 milliamperes as shown in Fig. 26.

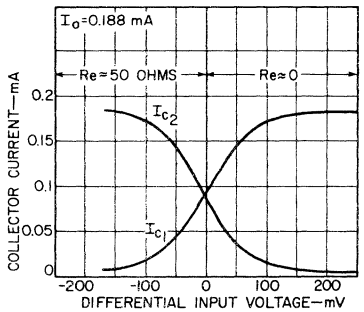


Fig. 27 — DC characteristics of the basic differential amplifier with and without emitter degeneration for a source current I_o of 0.188 milliampere.

At the lower current level, the transfer characteristics of the differential-amplifier transistors are not greatly altered by the use of the 50-ohm emitter resistors (R_e). At this current, the internal diffusion resistance (r_e) of each transistor is in the order of 260 ohms, and the 50-ohm emitter resistors (R_e) are relatively small in comparison. Eq. (23) shows that when the voltage drop across the differential pair of transistors (as represented by the first term of the equation) is equal to KT/q, the total input voltage drop across each resistor R_e (as given by the second term of the equation) is 0.28 KT/q for an I_o of 0.188 milliampere and 3.1 KT/q for an I_o of 2.1 milliamperes. This behavior suggests that, when gain control is provided by variations in the value of I_o, the signal-handling capability of the differential amplifier can be extended at maximum gain by the use of emitter resistors. As the current

I_o (and consequently the circuit gain) is reduced, however, the increase in signal-handling capability gradually disappears because the effect of the emitter resistors R_e becomes relatively insignificant compared to that of the internal diffusion resistance r_e of the transistors.

The family of curves shown in Fig. 28 illustrates the effect of emitter resistors on the transconductance at various current levels. Because of the inherent symmetry of the differential amplifier for positive and negative input signals, the same graph can be used to show the transconductance as a function of the input

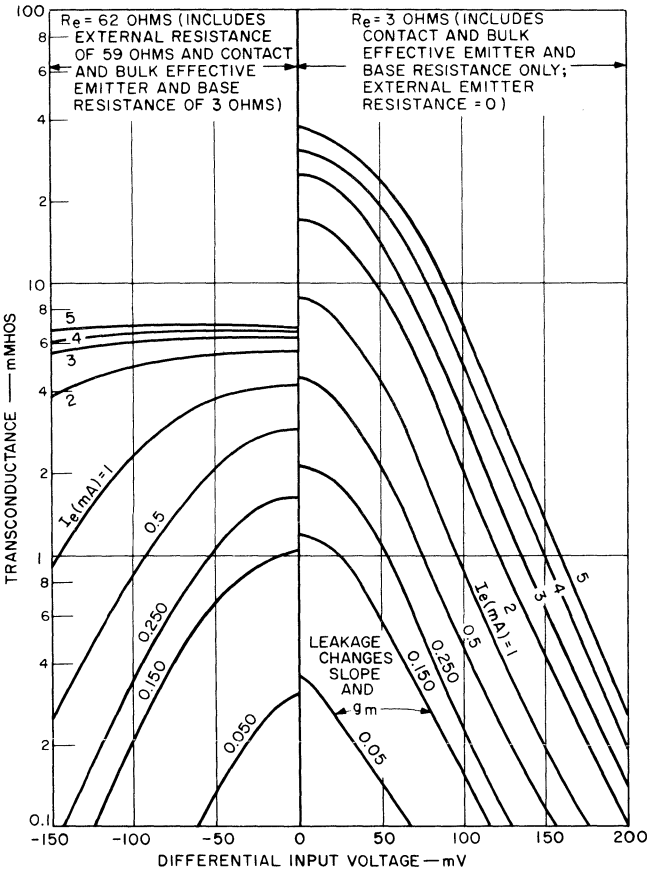


Fig. 28 — Transconductance of the basic differential amplifier as a function of differential input voltage for operation with and without emitter degeneration.

voltage for operation of the circuit at many different current values, with and without emitter resistors. The curves in Fig. 28 also show that the effects of a fixed-value emitter resistor become more pronounced, in relation to both the reduction in gain and the increase in linearity, as the current is increased. The experimental curves shown in Fig. 28 are in agreement with the theory presented thus far provided that the following postulations are used in the theoretical calculations:

1. The total of the effective emitter-contact and bulk resistance, r_e, inherent in each transistor of the differential pair is assumed to be 3 ohms.*
2. The actual value of each diffused emitter resistor R_e is 59 ohms, rather than the nominal value of 50 ohms used previously.
3. A leakage current of approximately 12 microamperes is assumed.**

When the inherent effective emitter resistance of the transistors is assumed to be 3 ohms, the measured transconductance curves shown on the right coordinate plane in Fig. 28 coincide (within the limits of experimental error) with theoretical curves calculated from Eqs. (17) and (27), except when the total αI_0 is equal to or less than 1 milliampere. At these low current levels, the theoretical curves must be corrected to compensate for leakage effects. The leakage current of 12 microamperes is subtracted from the nominal value of αI_0, and the theoretical transconductance values are thus decreased.

For the left coordinate plane, coincidence between theoretical and experimental curves requires that a value of 62 ohms be used in Eq. (27) for the emitter resistor R_e. When the effective internal emitter resistance of 3 ohms is subtracted from this value, the actual value of the external diffused emitter resistors is shown to be 59 ohms, as postulated above.

The excellent correlation of the theoretical assumptions with the actual measured data suggests that a more rigorous equation for the transconductance can be derived.

**The emitter resistance r_e is the sum of the emitter-contact and bulk resistance and the effective base resistance referred to the emitter, $(1 - \alpha)r_b'$. For the transistors in question, the resistance r_e consists of about 2 ohms of emitter resistance and 1 ohm of effective base resistance.*

*** This leakage-current value of 12 microamperes was based on experimental data obtained on early units. Tests on recent units indicate that processing improvements have substantially reduced the leakage in linear integrated circuits.*

As can be determined from Fig. 23, the total voltage drop from base to base of the differential pair of transistors Q_1 and Q_2 may be expressed as follows:

$$V_{b1} - V_{b2} = V_{be1} + I_{e1} R_e - I_{e2} R_e - V_{be2} \tag{28}$$

In a balanced circuit, the emitter-to-base voltages of transistors Q_1 and Q_2 are given by Eqs. (29) and (30), respectively:

$$V_{be1} = (1 - \alpha)\, I_{e1}\, r_b' + \frac{KT}{q} \ln \frac{I_{e1}}{I_s} + I_{e1}\, r_{ec} \tag{29}$$

$$V_{be2} = (1 - \alpha)\, I_{e2}\, r_b' + \frac{KT}{q} \ln \frac{I_{e2}}{I_s} + I_{e2}\, r_{ec} \tag{30}$$

where r_b' is the internal base resistance, r_{ec} is the internal emitter-contact resistance, and the following matching equalities are assumed:

$$\begin{aligned} I_s &= I_{s1} = I_{s2} \\ \alpha &= \alpha_1 = \alpha_2 \\ r_b' &= r_{b1}' = r_{b2}' \\ r_{ec} &= r_{ec1} = r_{ec2} \\ R_e &= R_{e1} = R_{e2} \end{aligned} \tag{31}$$

(The effects of the offsets that result from an unbalance in any of the matching parameters are analyzed in the next section.)

The relationships expressed by Eqs. (28), (29), and (30), together with those given by Eqs. (1), (5), and (6), are used to obtain equations for the transconductance in terms of the collector currents I_{c1} and I_{c2} of transistors Q_1 and Q_2, respectively, as follows:

$$V_{b1} - V_{b2} = [(1 - \alpha)\, r_b' + r_{ec} + R_e] \left(\frac{2I_{c1}}{\alpha} - I_o \right) + h \ln \frac{I_{c1}}{\alpha I_o - I_{c1}} \tag{32}$$

$$V_{b1} - V_{b2} = [(1 - \alpha)\, r_b' + r_{ec} + R_e] \left(I_o - \frac{2I_{c2}}{\alpha} \right) + h \ln \frac{\alpha I_o - I_{c2}}{I_{c2}} \tag{33}$$

Eqs. (32) and (33) are differentiated, and the results are evaluated at the operating point (at $I_{c1} = I_{c2} = \alpha I_o/2$) to obtain the following relationships:

$$\frac{d(V_{b1} - V_{b2})}{dI_{c1}} = \frac{2(1 - \alpha)\, r_b'}{\alpha} + \frac{(r_{ec} + R_e)\, 2}{\alpha} + \frac{4h}{\alpha I_o} \tag{34}$$

$$\frac{d(V_{b1} - V_{b2})}{dI_{c2}} = -\frac{2(1 - \alpha)\, r_b'}{\alpha} - \frac{(r_{ec} + R_e)\, 2}{\alpha} - \frac{4h}{\alpha I_o} \tag{35}$$

Eqs. (34) and (35) are inverted to obtain the required equations for the transconductance of transistors Q_1 and Q_2, respectively, as follows:

$$g_{m1} = \frac{dI_{c1}}{d(V_{b1} - V_{b2})} = \frac{\alpha}{2(1 - \alpha)\, r_b' + 2(r_{ec} + R_e) + 4h/I_o} \tag{36}$$

$$g_{m2} = \frac{dI_{c2}}{d(V_{b1} - V_{b2})} = \frac{-\alpha}{2(1 - \alpha)\, r_b' + 2(r_{ec} + R_e) + 4h/I_o} \tag{37}$$

The negative sign of Eq. 37 reflects the negative slope, shown in Fig. 21, of the transfer characteristic for I_{c2}.

OFFSETS IN THE DIFFERENTIAL-AMPLIFIER INTEGRATED CIRCUITS

In the preceding analyses, it has been assumed that the parameters of the pair of transistors in the differential-amplifier integrated circuits are perfectly matched. In general, this assumption is justified because, although finite differences in the parameters exist, they are usually negligible. Nevertheless, variations in the amount of the differences from unit to unit result in a statistical distribution, and practical production limits on the allowable deviations in corresponding parameters of the differential pair of transistors must be established. It is convenient to evaluate the effects of circuit and device unbalances in terms of a quantity, referred to as offset, which is a measure of the total accumulative unbalances.

Types of Offsets

The amount of offset in a differential amplifier can be determined by output-voltage offset measurements, by input-voltage offset measurements, or by input-current offset measurements. Each of these basic measurement techniques is straightforward and provides accurate results when employed at low frequencies. The measurements may also be used to determine the offset in cascaded differential amplifiers and in operational amplifiers.

Output-Voltage Offset — An offset in the differential-amplifier circuit is indicated by a difference in potential between the two outputs (V_{o1} and V_{o2}, as defined in Fig. 23) of the transistors when there is no signal applied to the input of either transistor. This type of offset is a measure of any unbalance caused by the flow of base currents from the differential pair of transistors Q_1 and Q_2 through the two external base resistors to ground. Under these conditions, the voltages V_{b1} and V_{b2} are both unequal to zero; an offset exists if these voltages are also unequal to each other (i.e., if $V_{b1} - V_{b2} \neq 0$).

A common method used to determine the offset at the output is to reduce the two base resistors to zero. This effect is achieved when the inputs of the transistors Q_1 and Q_2 are shorted to ground. The output offset determined in this manner is restricted in that unbalances caused by unequal base currents (betas) or by unequal external base resistors are excluded. All other unbalances, however, are included in the measurement.

Input-Voltage Offset — An offset voltage referred to the input is simply the differential output offset voltage divided by the double-ended voltage gain of the circuit. This definition indicates a convenient method that may be used to measure the offset. In this method, a voltage is applied to one input of the differential amplifier and is varied until the differential output voltage $V_{o1} - V_{o2}$ is reduced to zero. The value of the input voltage is then the offset voltage referred to the input.

Input-Current Offset — The offset in a differential amplifier can also be determined by the amount of current that must be introduced at one input to obtain a differential output voltage equal to zero. This type of measurement, together with the output offset measurement in which the inputs of the circuit are shorted to ground, tends to segregate unbalances in base currents (betas) and in the input base resistors.

Dependence of Offset on Base-to-Emitter Voltages

Offsets in the differential-amplifier integrated circuits can, in general, be attributed to three basic types of device or circuit unbalances:

1. Differences in the base-to-emitter voltage V_{be} and in the beta of the differential pair of transistors because of initial deviations in the geometry or the diffusion-concentration profiles of the transistors;

2. Differences in the V_{be}, the beta, or the internal resistances of the transistors that result from finite variations in thermal resistance or heat flow paths;
3. Differences in the values of resistors used in the collector, base, or emitter leads of the two transistors.

The voltage between the base and emitter leads of a transistor, V_{be}, includes the fundamental voltage drop across the emitter-base junction, as given by the diode equation [Eq. (7)], together with the voltage drops that are produced by the flow of base current through the intrinsic base resistance r_b' and by the flow of emitter current through the emitter-contact and bulk resistance r_{ec}. V_{be} can be expressed in terms of these voltage drops, as follows:

$$V_{be} = \left(\frac{KT}{q} \ln \frac{I_e}{I_s}\right) + I_e r_{ec} + I_e (1 - \alpha)\, r_b' \tag{38}$$

The emitter-contact and bulk resistance r_{ec} should not be confused with the diffusion resistance r_e, which is given by the familiar T-circuit representation as follows:

$$r_e = \frac{KT}{qI_e} \tag{39}$$

The voltage drop across the diffusion resistance r_e is included in the logarithmic term of Eq. (38).

The voltage V_{be} is obviously a nonlinear function of the transistor current and, therefore, cannot be represented properly by any lumped-constant linear equivalent circuit. Eq. (38), which contains no approximation, provides the best means for the calculation of this voltage.

The bulk saturation current I_s is best determined from a measured curve at an emitter current which is low enough so that the voltage drops across the internal resistances (r_b' and r_{ec}) of the transistor are negligible. Fig. 29 shows curves of V_{be} as a function of temperature at various emitter currents for a typical integrated-circuit transistor. This transistor has an intrinsic base resistance r_b' of 40 ohms, an emitter-contact and bulk resistance r_{ec} of approximately 3 ohms, and a beta of about 50. The V_{be} curve obtained at an emitter current of 100 microamperes can be used satisfactorily in the determination of the current I_s.

At an emitter current of 100 microamperes, the base current of the transistor is about 2 microamperes. The resultant voltage drop produced across the intrinsic base resistance r_b' then is about 0.08 millivolt. At this level of emitter current, the voltage

drop across the emitter-contact and bulk resistance r_{ec} is approximately 0.3 millivolt. Thus, at 100 microamperes of emitter current, the total voltage drop (approximately 0.38 millivolt) across the internal resistances of the transistor is negligible, and the measured value obtained for V_{be} can be attributed almost entirely to the logarithmic term in Eq. (38).

Fig. 29 shows that V_{be} is 0.7 volt for an emitter current of 100 microamperes and a temperature of 20°C. When the values of transistor parameters given by these conditions are substituted in Eq. (8), the following result can be obtained:

$$\frac{I_e}{I_s} = \exp \frac{700}{26} = 5 \times 10^{11}$$

$$I_s = 0.2 \times 10^{-15} \text{ ampere}$$

For each decade change in the emitter current, the logarithmic component of the base-to-emitter voltage V_{be} changes by an amount equal to KT/q ln 10, or 60 millivolts at 300°K. Fig. 29 shows, however, that the V_{be} curve for an emitter current of 1 milliampere is shifted 65 millivolts upward from the V_{be} curve obtained at 100 microamperes. The additional 5 millivolts of change is exactly equal to the voltage drop developed across the internal resistances of the transistor at the 1-milliampere level. For an emitter current of 5 milliamperes, the sum of the voltage drops across the internal resistances is in the order of 19 millivolts, and the logarithmic component of V_{be} is increased from the value obtained at 1 milliampere of emitter current by an amount equal to KT/q ln 5, or 42 millivolts at 300°K. These results show that the base-to-emitter voltage V_{be} is largely dependent upon the bulk saturation current I_s. At a given temperature, this current,

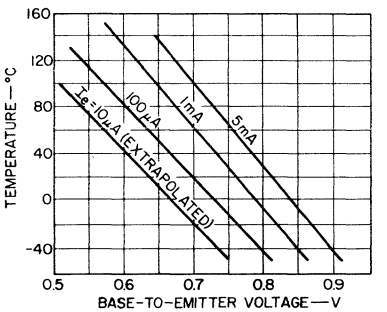


Fig. 29 — Effect of temperature and emitter current on the base-to-emitter voltage of an integrated-circuit transistor.

in turn, is a function of the geometry of the base-emitter junction and the diffusion-concentration profile.

The curves in Fig. 29 also show that the dependence of the base-to-emitter voltage on temperature is varied by a change in the level of emitter current. The variation in V_{be} with temperature changes from −1.6 millivolts per °C at low emitter currents (0.1 milliampere or less) to 1.3 millivolts per °C at 5 milliamperes of emitter current. This reduction in the negative temperature coefficient of V_{be} with an increase in emitter current is a result of the positive temperature coefficient of the transistor resistors.

Relative Effects of Various Circuit and Device Unbalances

The relative effects of unbalances in various transistor parameters and in emitter resistors on the offsets in the differential-amplifier integrated circuit can be evaluated on the basis of the preceding discussion of transistor base-to-emitter voltage. For this evaluation, an equation for offset voltage in terms of the various circuit and device parameters is derived for the differential-amplifier circuit shown in Fig. 23 so that the effects of an unbalance between corresponding parameters on the offset voltage can be readily determined.

In the offset-voltage derivation, the base currents I_{b_1} and I_{b_2} are assumed to enter the bases of the differential pair of transistors Q_1 and Q_2 through external base resistors R_{b_1} and R_{b_2}, respectively, from the ground reference. Kirchoff's first law then dictates that the sum of the voltage drops from the ground reference across R_{b_1}, the base-emitter junction of transistor Q_1, the two equal emitter resistors R_{e_1} and R_{e_2}, the base-emitter junction of transistor Q_2, R_{b_2}, and back to the ground reference must be zero. This summation may be expressed as follows:

$$I_{b_1} R_{b_1} + V_{be_1} + I_{e_1} R_{e_1} - I_{e_2} R_{e_2} - V_{be_2} - I_{b_2} R_{b_2} = 0 \quad (40)$$

Eq. (40) may be rewritten as follows:

$$(1-\alpha_1)I_{e_1}R_{b_1} + I_{e_1} R_{e_1} + V_{be_1} = (1-\alpha_2)\, I_{e_2} R_{b_2} + I_{e_2} R_{e_2} + V_{be_2} \quad (41)$$

This equation is then solved for I_{e_1} to obtain

$$I_{e_1} = \frac{I_{e_2}R_{b_2}\,(1-\alpha_2) + I_{e_2}R_{e_2}}{R_{b_1}\,(1-\alpha_1) + R_{e_1}} + \frac{V_{be_2} - V_{be_1}}{R_{b_1}\,(1-\alpha_1) + R_{e_1}} \quad (42)$$

In Eq. (42), the voltage drops across the intrinsic emitter and base resistances (r_{ec} and r_b') need not be explicitly expressed because these voltage drops are implied in the $V_{be_2} - V_{be_1}$ term.

Alternatively, if the $V_{be_2} - V_{be_1}$ term is used to represent the purely logarithmic component of the base-to-emitter voltage, the voltage drops across the intrinsic resistances, when they are significant, can be lumped with the external resistors.

The current-transfer relationships given by Eq. (5) are used to rewrite Eq. (42) in terms of the collector currents I_{c_1} and I_{c_2} of transistors Q_1 and Q_2, respectively, as follows:

$$\frac{I_{c_1}}{\alpha_1} = \frac{I_{c_2}}{\alpha_2}\left[\frac{R_{b_2}(1-\alpha_2)+R_{e_2}}{R_{b_1}(1-\alpha_1)+R_{e_1}}\right] + \frac{V_{be_2}-V_{be_1}}{R_{b_1}(1-\alpha_1)+R_{e_1}} \quad (43)$$

Eq. (41) may also be written in terms of the common-emitter current gain, i.e., the transistor beta (β), when the following relationships are employed:

$$\beta = \frac{\alpha}{1-\alpha} \quad (44)$$

$$\alpha = \frac{\beta}{\beta+1} \quad (45)$$

The resultant equation is given by

$$I_{c_1} = \frac{\beta_1}{\beta_2}\left[\frac{R_{b_2}+(\beta_2+1)R_{e_2}}{R_{b_1}+(\beta_1+1)R_{e_1}}\right] I_{c_2} + \frac{\beta_1(V_{be_2}-V_{be_1})}{R_{b_1}+(\beta_1+1)R_{e_1}} \quad (46)$$

As stated previously, an offset in a differential-amplifier circuit is indicated by a difference in the collector outputs of the differential pair of transistors. This offset-voltage difference is given by the following equation:

$$V_{o_1} - V_{o_2} = I_{c_2}R_{c_2} - I_{c_1}R_{c_1} \quad (47)$$

where V_{o_1} and V_{o_2} are the collector outputs of the differential-amplifier transistors Q_1 and Q_2, respectively, and R_{c_1} and R_{c_2} are the collector load resistors for these transistors.

The effects on the offset of differences in corresponding parameters of the differential pair of transistors Q_1 and Q_2 can be approximated by examination of Eqs. (43), (46), and (47) when such differences are introduced. In such examinations, differences in only one set of parameters are allowed at any given time, and the effects of these differences on the offset are noted.

In the evaluations, R_{e_1} and R_{e_2} are used to denote the total of the extrinsic and intrinsic emitter resistance, and R_{b_1} and R_{b_2} are used to denote the total of the extrinsic and intrinsic base resistance. The following initial assumptions are also made for a perfectly balanced differential amplifier:

$R_{e_1} = R_{e_2} =$ 50 ohms extrinsic + 3 ohms intrinsic
$R_{b_1} = R_{b_2} =$ 40 ohms intrinsic + 0, 1000, or 10,000 ohms extrinsic
$R_{c_1} = R_{c_2} =$ 1000 ohms
$I_{e_1} = I_{e_2} \approx$ 1 milliampere
$\beta_1 = \beta_2 \approx 60$

Figs. 30 to 36 show the effects on the offset of differences in corresponding pairs of the various parameters as calculated from Eqs. (46) and (47). Because these calculations all result in straight-line curves, the effects of the various unbalances can be readily compared by the graphic presentation. The effect of unbalanced conditions other than those shown, such as differences in collector resistors, may also be compared by the use of these simple graphic techniques.

Fig. 30 shows the effects on offset of unequal betas. Curves are shown for an external base resistance of zero and for transistor betas in the range of 20, 60, and 100. These curves represent the first term of Eq. (46).

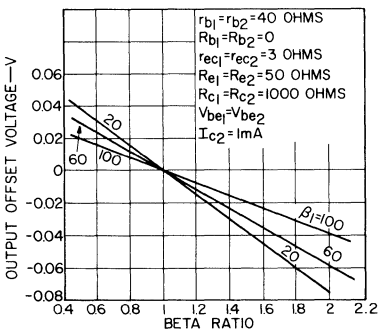


Fig. 30 — Effect of absolute values and ratios of the betas of the differential pair of transistors on the output offset voltage.

Fig. 31 shows the effect of different values of base resistances ($R_{b_1} = R_{b_2}$) on the offset when the betas of the differential-amplifier transistors are unequal. The curves in this figure show that a serious increase in the offset occurs when the external base resistances are significantly larger than the nominal value. Figs. 32 and 33, however, indicate that the use of larger external base resistances reduces the offset that is produced when the betas are the same and a difference exists between the emitter resistors or the base-to-emitter voltages.

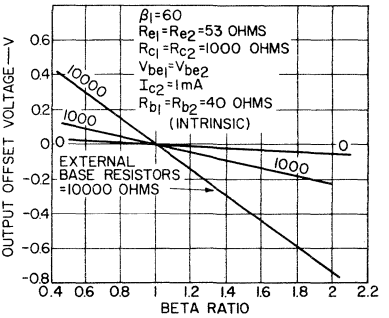


Fig. 31 — Output offset voltage as a function of the beta ratio of the differential pair of transistors for several values of external base resistors.

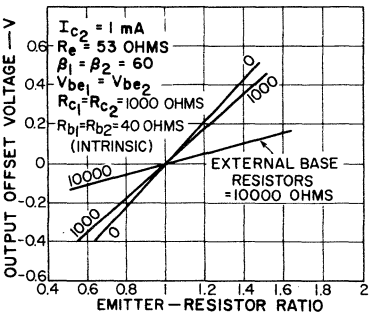


Fig. 32 — Output offset voltage as a function of the emitter-resistor ratio of the differential pair of transistors for several values of external base resistors.

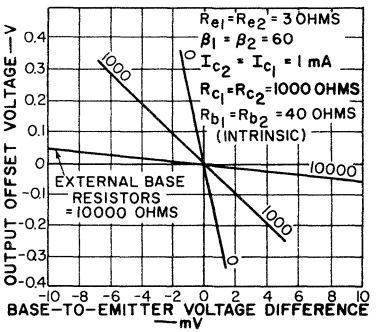


Fig. 33 — Output offset voltage as a function of the difference in the base-to-emitter voltage of the differential pair of transistors for several values of external base resistors.

Fig. 34 shows that the offset that results from differences in the emitter resistors is increased by the use of larger emitter resistors. Fig. 35 shows that the offset caused by differences in the V_{be} of the differential pair of transistors is reduced by the use of emitter resistors.

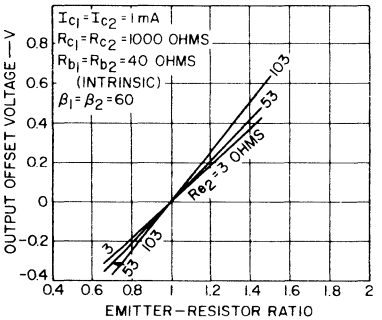


Fig. 34 — Effect of absolute values and ratios of the emitter resistors of the differential pair of transistors on the output offset voltage.

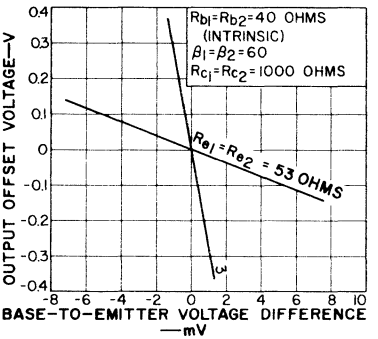


Fig. 35 — Output offset voltage as a function of the difference in the base-to-emitter voltages of the differential pair of transistors for several values of the total emitter resistance (internal + external) of each transistor.

Fig. 36 shows the offset as a function of differences in the base-to-emitter voltages of the transistors for transistor betas ($\beta_1 = \beta_2$) of 20, 60, and 100. The curves in this figure, which represent the second term in Eq. (46), indicate that the effects of the absolute values of the betas on this term are the opposite of those on the first term, as shown in Fig. 30.

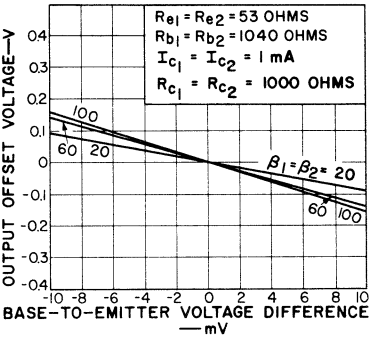


Fig. 36 — Output offset voltage as a function of the difference in the base-to-emitter voltages of the differential pair of transistors for several beta values.

Effects of Temperature on Circuit Offset Voltage

Each parameter in Eqs. (46) and (47) is dependent to some extent on temperature, even though this dependence cannot be readily expressed as a straightforward mathematical relationship. An analytical expression of the offset as a function of temperature is, therefore, of small practical value. It is more meaningful to relate the offset to temperature-caused differences in the values of the base-to-emitter voltages, betas, or resistances of the differential-amplifier transistors.

One of the main advantages of differential-amplifier integrated circuits is that each component for a given transistor is physically located very close to the corresponding component of the second transistor of the differential pair. As a result, the temperature environments for the pairs of components should be very similar. This feature is successfully exploited in the design of the integrated circuits, so that the effects of temperature on corresponding components is remarkably similar.

Experimental data on sample units have shown that the change in output offset varies from no measurable drift up to 10 millivolts for temperature variations over the 180-degree range from −55°C to +125°C. These limits correspond to an input offset of between 0 and 2.5 microvolts per °C. Statistical production controls usually allow for greater maximum drifts, e.g., 5 to 10 microvolts per °C.

CONSTANT-CURRENT SINK

The constant-current sink for the source current I_o, which is a significant factor in the transfer and transconductance characteristics of the differential amplifier, may be realized physically by a resistor and a dc power supply or by a transistor circuit and a dc power supply. The transistor-current-sink circuit has a higher ac-to-dc impedance ratio, which results in higher common-mode rejection. In addition, the gain characteristics and bias network of the transistor sink circuit make possible temperature compensation, gain control, squelch or switch action, and frequency multiplication in the differential amplifier. The transistor current sink, therefore, is clearly superior in versatility to the resistor current sink for use in the differential-amplifier integrated circuits. The characteristics of the transistor current sink are developed in detail below.

Analysis of Basic Current-Sink Circuit

Fig. 37 shows the general configuration of a transistor current-sink circuit in which diode temperature stabilization is employed. In this general circuit, all diodes are assumed to be forward-biased. D_1 represents the number (0, 1, 2, . . .) of forward-biased diodes in series with resistor R_1, and D_2 represents the number (0, 1, 2, . . .) of forward-biased diodes in series with resistor R_2.

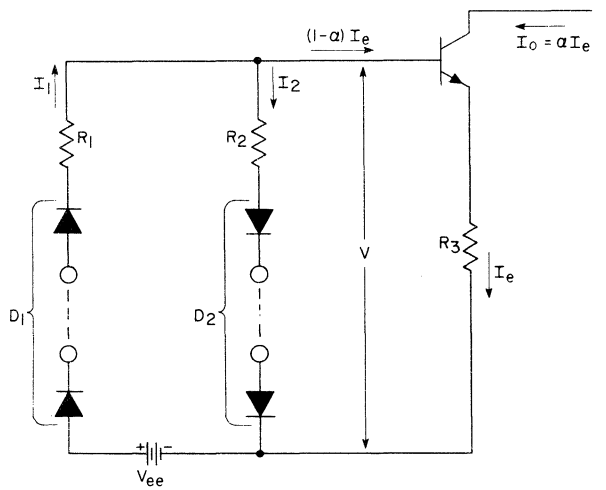


Fig. 37 — General configuration for a diode-stabilized transistor current-sink circuit.

The sink current I_o of the differential amplifier is the collector current of the current-sink transistor. This current is expressed in terms of the emitter current of the current-sink transistor by Eq. (5), which relates the collector and emitter currents of a single transistor, as $I_c = \alpha I_e$, where in this case the I_e is the emitter current of the current-sink transistor. Each diode used in the integrated circuits is actually a transistor connected to operate as a diode. The voltage drop V′ across each diode used in the current-sink circuit can be expressed as follows:

$$V' = \left(\frac{KT}{q} \ln \frac{I}{I_s}\right) + Ir \tag{48}$$

where r is the sum of all the internal resistance of the diode.

The resistance r is generally very small in comparison to the external resistors R_1 and R_2 in series with the diodes, and the voltage drop Ir can usually be neglected. For this condition, the voltage drop V′ is expressed by the first term of Eq. (48), and, as determined from Fig. 29, is about 0.765 volt for a current of 1 milliampere. The voltage drop Ir in Eq. (48) represents an additional 5 millivolts.

For a diode formed by the connection of the collector of a transistor to the base ($V_{CB} = 0$), the total currents and Ir drops are very similar to those of the transistor connection. For other possible connections of transistor terminals to form diodes, more of the diode current flows through r_b' and a higher forward voltage drop results. In Fig. 37, this additional voltage drop is lumped with the voltage drops across the external resistors R_1 and R_2.

For the transistor in the current-sink circuit, the voltage drop V′ is considered to be expressed by the logarithmic term in Eq. (38). The second and third terms of this equation represent voltage drops that, although identified separately, can be lumped with the resistive drops in the base and emitter paths for the circuit shown in Fig. 37.

For the general current-sink circuit shown in Fig. 37, the following equations are necessary and sufficient to define the operating requirements and characteristics:

$$I_1 = I_2 + (1 - \alpha)\, I_e \tag{49}$$

$$V_{ee} - (D_1 + D_2)\, V' = I_1 R_1 + I_2 R_2 \tag{50}$$

$$D_2 V' + I_2 R_2 = (1 - \alpha)\, r_b' I_e + V' + (r_{ec} + R_3)\, I_e \tag{51}$$

Solution of these three equations in terms of the emitter current I_e of the current-sink transistor yields the following relationship:

$$I_e = \frac{X\,[V_{ee} - (D_1 + D_2)\,V'] + (D_2 - 1)\,V'}{R_3 + r_{ec} + (1 - \alpha)\,(r_b' + R_1X)} \tag{52}$$

where

$$X = \frac{R_2}{R_1 + R_2} \tag{53}$$

Temperature Characteristics

In Eq. (52), the emitter resistor R_3 is usually the dominant term of the denominator; however, if the beta of the current-sink transistor is low, the contribution of the base resistance ($r_b + R_1X$) may also be significant. The effect of the base resistance can be particularly noticeable at the low extreme of the temperature range where the current gain [$\beta = \alpha/(1 - \alpha)$] is minimum. The temperature coefficient of the denominator of Eq. (52), therefore, results from the combination of the temperature coefficients of the resistors and the effects of temperature on the transistor beta and, hence, on $1 - \alpha$.

In the numerator of Eq. (52), V' is the main temperature-dependent parameter. The multipliers $(D_1 + D_2)$ and $(D_2 - 1)$, therefore, may be used to control the temperature characteristics in the numerator.

These statements indicate that the effects of temperature on the operation of the current-sink circuit can be controlled by the values selected for D_1, D_2, X, and V_{ee}. The effect of each of these parameters on the emitter current I_e, as given by Eq. (52), and hence on the output current of the current-sink circuit ($I_o = \alpha I_e$) is evaluated below.

In the use of Eq. (52) to evaluate the effects of temperature on the current-sink circuit, it is convenient to represent the numerator and denominator of the equation by more compact symbols, as follows:

$$I_e = \frac{E}{R_t} \tag{54}$$

where

$$E = X\,[V_{ee} - (D_1 + D_2)\,V'] + (D_2 - 1)\,V' \tag{55}$$

and

$$R_t = R_3 + r_{ec} + (1 - \alpha)\,(r_b' + R_1X) \tag{56}$$

In Eqs. (54) and (55), the term E represents the effective emitter voltage of the current-sink transistor.

Fig. 38 illustrates the effects of temperature on the resistance R_t. In this figure, curves B, C, and D show R_t as a function of

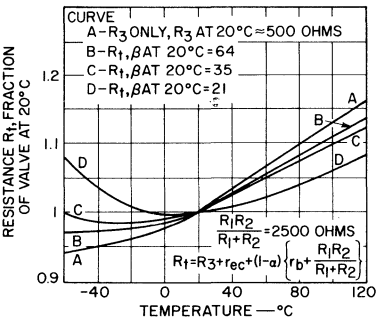


Fig. 38 — Resistance ratio R_t as a function of temperature for several values of the beta of the current-sink transistor.

temperature for three beta values when the nominal value of R_3 at 20°C is 500 ohms. Curve A shows variations in the value of resistor R_3 with temperature. The temperature coefficient of beta is considered linear. The slopes of this coefficient for the beta values of 64, 35, and 21 used in Fig. 38 are 0.26, 0.14, and 0.12 per °C, respectively.

These slopes are average values based on the measured performance of a number of transistors. The temperature coefficient of resistor R_3, as represented by curve A in Fig. 38, is also determined from measured values.

Fig. 39 indicates that the effect of beta variations with temperature on the composite resistance R_t is reduced as the

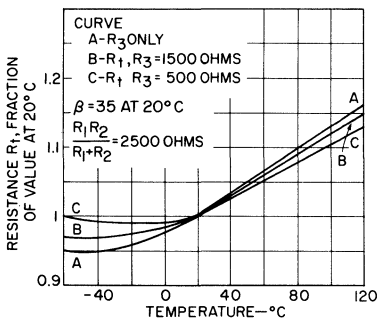


Fig. 39 — Resistance ratio R_t as a function of temperature for several values of the emitter resistor (R_3) of the current-sink transistor.

value of R_3 is increased. Figs. 38 and 39 illustrate the following main factors in this relationship:

1. As the temperature rises, the resistance R_t increases; the

emitter current I_e and, therefore, the source current I_o then decrease unless the voltage E is made to increase simultaneously. Eqs. (37) and (38) reveal that the transconductance also decreases as the temperature increases unless the source current I_o is made to increase with temperature.

2. If a collector load resistor tracks the composite resistance R_t over a large portion of the operating temperature range, the operating point is independent of temperature (to a first approximation) only if the factor E has a zero temperature coefficient.

It is desirable, therefore, to examine the factor E, given by Eq. (55), to determine (a) a zero temperature coefficient for E, and (b) a coefficient for E that is large enough to cause the current I_o to increase with increases in temperature.

It is convenient to define the voltage drop V′ as follows:

$$V' = V_o + C\triangle T \tag{57}$$

where V_o is the value of V′ at room temperature, C is the temperature coefficient of V′ (e.g., −1.43 millivolts per °C), and ΔT is the change in temperature from room temperature.

When the relationship expressed by Eq. (57) is used in Eq. (55), the value of E is given by

$$E = \frac{X}{M}(MV_{ee} - V_o - C\triangle T) \tag{58}$$

where

$$M = \frac{X}{(D_1 + D_2)\left(X - \dfrac{D_2 - 1}{D_1 + D_2}\right)} \tag{59}$$

The proportional change in E with temperature can be expressed as follows:

$$\frac{\triangle E}{E} = \frac{-C\triangle T}{MV_{ee} - V_o} \tag{60}$$

Because the temperature coefficient C is negative, the ratio $\Delta E/E$ can be positive only if M is positive and if MV_{ee} is greater than V_o. A zero temperature coefficient for E is approached when M approaches infinity; resistance ratio X is then given by

$$X = \frac{D_2 - 1}{D_1 + D_2} \tag{61}$$

When M is equal to or less than 1, the ratio $\Delta E/E$ is very

small and, for conventional dc power supplies ($V_{ee} >> V_o$), is positive. In the evaluation of M, it is important to remember that D_1 and D_2 are positive integers, and that X is a positive number between 0 and 1 (i.e., $0 < X < 1$). The value of X is restricted even further by practical circuit considerations. Eqs. (54), (55), and (56) show that the operating point of differential-amplifier integrated circuits is dependent upon the value of the resistance ratio X. This ratio, therefore, must be easy to maintain at the required value during production to assure a predictable operating point. The more closely the resistors R_1 and R_2 are matched in geometry, the more easily the value of the ratio X can be maintained at the required value.

Eq. (53) can be rewritten to obtain the following expression for X:

$$X = \frac{1}{\frac{R_1}{R_2} + 1}$$

If production tolerances restrict the ratio R_1/R_2 to a value between 0.5 and 2 (i.e., $0.5 \leq R_1/R_2 \leq 2$), X is then constrained to the region between 0.33 and 0.67 (i.e., $0.33 \leq X \leq 0.67$).

Practical considerations also dictate that the number of compensating diodes used in the current-sink circuit be limited to the minimum required to provide the necessary temperature compensation. The maximum value for D_1 or D_2 is limited to 3. A systematic exploration of all possible combinations is best accomplished by evaluation of Eqs. (59) and (60) as functions of X, D_1, and D_2, as D_1 and D_2 are assigned values of 0, 1, 2, and 3 in turn.

For $D_2 = 0$, Eq. (59) becomes

$$M = \frac{X}{D_1 X + 1} \tag{62}$$

M is positive for all values of X. Substitution of Eq. (62) into Eq. (60) shows that infinite points occur whenever $MV_{ee} = V_o$. When MV_{ee} is less than V_o, the ratio $\Delta E/E$ is negative; otherwise, this ratio is positive.

The change in $\Delta E/E$ that results from a 100°C rise in temperature is shown in Figs. 40 through 45, for various conditions. Fig. 40 shows this proportional change in E as a function of X for different values of D_1 when $D_2 = 0$ and $V_{ee} = 3.0$ volts. As X is varied from 0 to 1, the increase in temperature causes negative increases in E that rise to infinity. As X is increased further, the

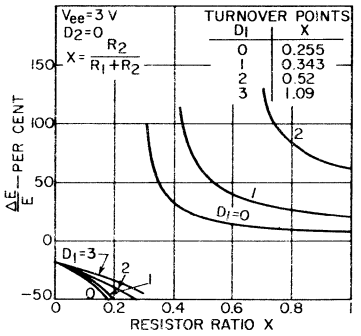


Fig. 40 — Effect of the number of diodes D_1 on the variation in the voltage E as a function of the ratio X for a temperature increase of 100°C and a supply voltage V_{ee} of 3 volts when no diodes D_2 are used.

proportional change in E becomes positive and becomes smaller and smaller as X approaches 1. The use of higher values of D_1 increases the value of X at which the turnover occurs and, in general, results in a higher positive value for $\Delta E/E$.

Fig. 41 shows $\Delta E/E$ as a function of X for the same conditions as those given in Fig. 40, except that V_{ee} is 6 volts. With V_{ee} doubled, the turnover point occurs closer to the origin, and the positive changes in E are smaller.

It is obvious that D_2 must equal 0 for a positive change in E to result from a temperature increase and for a negative change in E to result from a temperature decrease. The exact amount of change in E, together with the expected operating points, dictates the value of D_1 and of the ratio X.

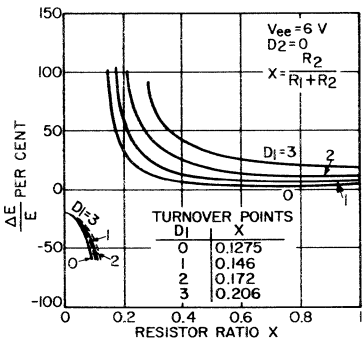


Fig. 41 — Effect of the number of diodes D_1 on the variation in the voltage E as a function of the ratio X for a temperature increase of 100°C and a supply voltage V_{ee} of 6 volts when no diodes D_2 are used.

For the condition $D_2 = 1$, Eq. (59) becomes

$$M = \frac{1}{1 + D_1} \tag{63}$$

This equation obviously is independent of the ratio X. The voltage E, therefore, is dependent upon only the power supply. This condition, however, does not permit the designer the option to introduce any quantitative change by the proper selection of X. For this reason, the condition $D_2 = 1$ is rejected and will not be considered further.

For the condition $D_2 = 2$, Eq. (59) is given as follows:

$$M = \frac{X}{(D_1 + 2)\left(X - \frac{1}{D_1 + 2}\right)} \tag{64}$$

For values of $X = 1/(2 + D_1)$, M is infinite, and Eq. (60) shows that $\Delta E/E$ becomes zero. When X is less than $1/(2 + D_1)$, M is negative, and negative values are obtained for $\Delta E/E$ as the temperature rises. When X is greater than $1/(2 + D_1)$, M is positive.

When the voltage V_{ee} is low enough, the ratio $\Delta E/E$ may again approach infinity and then become negative. As illustrated in Fig. 42, which shows variations in $\Delta E/E$ as a function of X for a V_{ee} of 3.0 volts and $D_1 = 3$, this condition can produce large positive coefficients. These coefficients are somewhat smaller when a higher V_{ee} is employed, as shown in Fig. 43 for $V_{ee} =$ 6.0 volts.

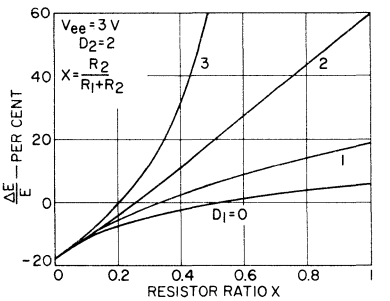


Fig. 42 — Effect of the number of diodes D_1 on the variation in the voltage E as a function of the ratio X for a temperature increase of 100°C and a supply voltage V_{ee} of 3 volts when two diodes D_2 are used.

When $D_2 = 3$, Eq. (59) can be written as follows:

$$M = \frac{X}{(3 + D_1)\left(X - \frac{2}{3 + D_1}\right)} \tag{65}$$

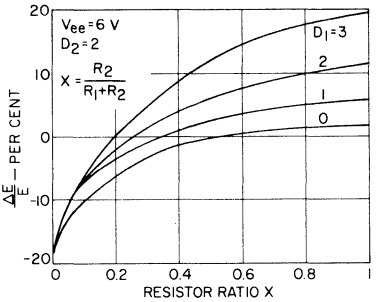


Fig. 43 — Effect of the number of diodes D_1 on the variations in the voltage E as a function of the ratio X for a temperature increase of 100°C and a supply voltage V_{ee} of 6 volts when two diodes D_2 are used.

The results for this condition are similar to those obtained for $D_2 = 2$, except that the points of the zero-temperature effect are shifted to higher values of X. The results for $D_2 = 3$ are illustrated in Figs. 44 and 45.

The simplest arrangement that results in a zero temperature coefficient is defined by the conditions $D_2 = 2$ and $D_1 = 0$. For these conditions, only two diodes are used, and the zero-

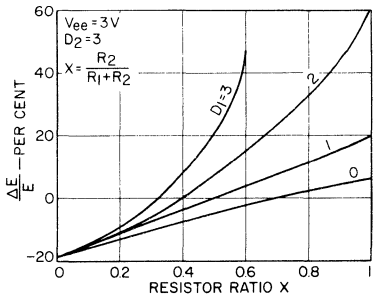


Fig. 44 — Effect of the number of diodes D_1 on the variations in the voltage E as a function of the ratio X for a temperature increase of 100°C and a supply voltage V_{ee} of 3 volts when three diodes D_2 are used.

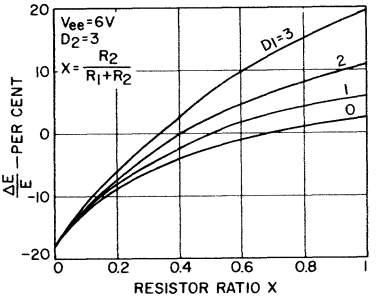


Fig. 45 — Effect of the number of diodes D_1 on the variations in the voltage E as a function of the ratio X for a temperature increase of 100°C and a supply voltage V_{ee} of 6 volts when three diodes D_2 are used.

temperature effect is obtained for X = 0.5. Little need then exists for the use of more diodes, particularly in view of the fact that the requirement for high positive coefficients is fulfilled by the condition $D_1 = D_2 = 0$, which does not require the use of any diodes.

Gain-Operating Point Relationships

More precise expressions than those thus far presented must be derived for the operating point and gain of a differential pair of transistors operated with a transistor current sink before an intelligent selection of the parameters for the sink circuit can be made.

Eqs. (5) and (54) are used to obtain the following definition for the collector currents of the differential pair of transistors at the operating point:

$$I_{c1} = I_{c2} = \frac{\alpha^2}{2}\left(\frac{E}{R_t}\right) \tag{66}$$

The voltage drop across the collector load resistor of each transistor is given by

$$I_cR_L = \left(\frac{\alpha^2}{2}\right)\left(\frac{ER_L}{R_t}\right) \tag{67}$$

If U is used to represent the ratio R_L/R_t, Eq. (67) may be rewritten as follows:

$$I_cR_L = \left(\frac{\alpha^2}{2}\right)EU \tag{68}$$

For a given positive collector supply voltage V_{cc}, the collector voltage V_{oc} of each transistor at the operating point is given by

$$V_{oc} = V_{cc} - \left(\frac{\alpha^2}{2}\right) UE \tag{69}$$

When an output emitter follower is used, the output voltage becomes

$$V_{oe} = V_{cc} - \left(\frac{\alpha^2}{2}\right) UE - V' \tag{70}$$

The gain G of each transistor at the operating point is equal to $|g_m R_L|$. On the basis of the relationships given by Eqs. (36), (54) and (67), this parameter can be defined as follows:

$$|G| = |g_m R_L| = \frac{\alpha U}{2\left[\frac{(1-\alpha) r_b' + (r_{ec} + R_e)}{R_t}\right] + \frac{4h}{\alpha E}} \tag{71}$$

Substitution of Eq. (58) into Eqs. (69) and (70) yields the following results:

$$V_{oc} = V_{cc} - \frac{\alpha^2}{2} UXV_{ee} + V_o\left(\frac{\alpha^2}{2}\frac{UX}{M}\right) + \frac{C\triangle T\alpha^2}{2}\left(\frac{UX}{M}\right) \tag{72}$$

$$V_{oe} = V_{cc} - \frac{\alpha^2 UXV_{ee}}{2} + V_o\left(\frac{\alpha^2 U}{2}\frac{X}{M} - 1\right) - C\triangle T\left(1 - \frac{\alpha^2 UX}{2M}\right) \tag{73}$$

For the conditions $D_1 = D_2 = 0$ and $X/M = 1$, Eqs. (72) and (73) may be rewritten as follows:

$$V_{oc} = V_{cc} - \frac{\alpha^2}{2} UXV_{ee} + \frac{V_o\alpha^2 U}{2} + C\triangle T\frac{\alpha^2 U}{2} \tag{74}$$

$$V_{oe} = V_{cc} - \frac{\alpha^2}{2} UXV_{ee} + V_o\left(\frac{\alpha^2 U}{2} - 1\right) - C\triangle T\left(1 - \frac{\alpha^2 U}{2}\right) \tag{75}$$

For the conditions $D_1 = 0$, $D_2 = 2$, and $X/M = 0$, the equations for V_{oc} and V_{oe} become

$$V_{oc} = V_{cc} - \frac{\alpha^2 U}{2} X V_{ee} \tag{76}$$

$$V_{oe} = V_{cc} - \frac{\alpha^2}{2} UXV_{ee} - V_o - C\triangle T \tag{77}$$

Eqs. (74) through (77) show that the operating point for the differential amplifier is dependent upon the resistor ratios U and X, upon the dc supply voltages V_{cc} and V_{ee}, and upon the α of the transistors.

Gain-Temperature Relationships

With the exception of α and U, which are expected to vary by small amounts with temperature, the only temperature-dependent terms in the expressions for the output voltage are those multiplied by $C\Delta T$. For the conditions under which Eq. (76) is applicable (i.e., $D_1 = 0$, $D_2 = 2$, and $X/M = 0$), the output-voltage equation contains no temperature-dependent terms except α and U. For the condition $D_1 = D_2 = 0$, Eq. (75) indicates the possibility of zero temperature coefficient for the output voltage of the differential amplifier when an output emitter follower is used and $\alpha^2 U/2$ approaches unity. For this condition ($D_1 = D_2 = 0$), the gain relationship, Eq. (71), becomes

$$|G| = \frac{\alpha U}{\frac{2R_{te}\,U}{R_e} + \frac{4KT\left(1 + \frac{\Delta T}{T_o}\right)}{q\,(V_{ee}X - V_o - C\Delta T)}} \tag{78}$$

where T_o represents the room temperature, ΔT is the amount of deviation in °C from the room temperature, and R_{te} is given by

$$R_{te} = (1 - \alpha)r_b' + (r_{ec} + R_e) \tag{79}$$

At room temperature (20°C), the gain is given by

$$|G|_{20°C} = \frac{\alpha\,U}{\frac{2\,R_{te}\,U}{R_L} + \frac{4K\,T_o}{\alpha q\,(V_{ee}\,X - V_o)}} \tag{80}$$

For the conditions used to obtain Eq. (76), i.e., $X/M = 0$, $D_1 = 0$ and $D_2 = 2$, the general gain equation is as follows:

$$|G| = \frac{\alpha U}{\frac{2R_{te}\,U}{R_L} + \frac{4KT_o\left(1 + \frac{\Delta T}{T_o}\right)}{\alpha q\,V_{ee}\,X}} \tag{81}$$

At room temperature, this equation reduces to

$$|G|_{20°C} = \frac{\alpha\,U}{\frac{2R_{te}\,U}{R_L} + \frac{4KT_o}{\alpha q\,V_{ee}\,X}} \tag{82}$$

The gain of the differential amplifier is thus found to depend upon the resistor ratios U, X, and R_{te}/R_L, upon α, and upon the dc supply voltage V_{ee}.

Relative Merits of Various Operating Modes

The variations in α and in α^2 with temperature are shown in Figs. 46 and 47, respectively. The effect of temperature on the resistance ratio U is shown in Fig. 48 for several values of resistor R_3 and a medium beta. The effect of different values of beta on the temperature dependence of the ratio U is shown in Fig. 49 for a resistor R_3 of 1000 ohms.

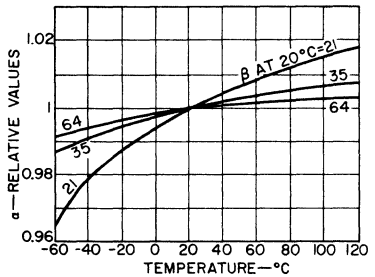


Fig. 46 — Relative values of the alpha for the current-sink transistor as a function of temperature for several beta values.

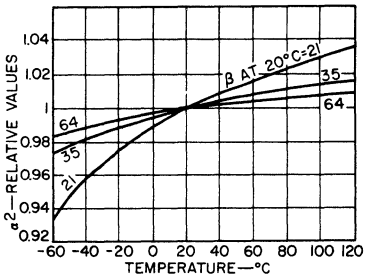


Fig. 47 — Relative values of the square of the alpha for the current-sink transistor as a function of temperature for several beta values.

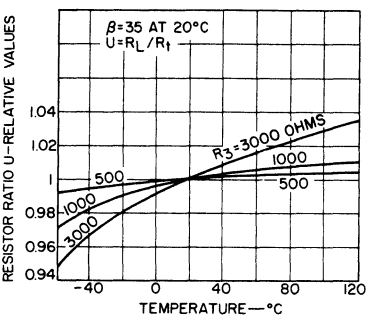


Fig. 48 — Resistor ratio U as a function of temperature for several values of the emitter resistor (R_3) of the current-sink transistor.

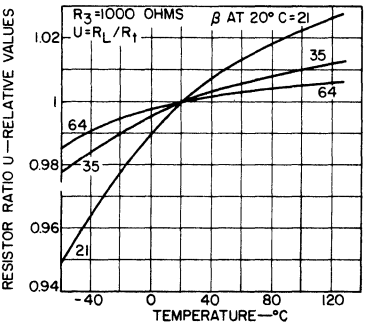


Fig. 49 — Resistor ratio U as a function of temperature for several values of the beta for the current-sink transistor.

The graphical data presented in Figs. 46 through 49, together with the relationships expressed by Eqs. (74) through (82), permit certain conclusions to be drawn about differential-amplifier integrated circuits. On the basis of the these conclusions, the relative merits of the various operating modes in the current-sink circuit can be evaluated with respect to the effects of temperature variations on the operating point and gain of differential-amplifier integrated circuits.

For the basic differential-amplifier circuit in which no output emitter follower is employed, Eq. (76) shows that when temperature-compensating diodes are used, the basic shift in the operating point with a change in temperature results entirely from a variation in α with temperature. Such α-caused shifts in the operating point result in small negative changes in the output voltage as the temperature increases.

When the compensating diodes are not used, Eq. (74) indicates that the decrease in output voltage will be more pronounced for the same increase in temperature. This condition is implied by the fact that the last term in Eq. (74) is negative for a rise in temperature. Although the amount of change in voltage can never become zero, it can be reduced by an increase in the value of resistor R_3.

When the emitter-follower output is used, the "diodes in" mode of operation can result in partial or complete cancellation of the negative-going decrease in voltage that occurs with rises in temperature. The degree of cancellation is dependent upon the values of U, X, and V_{ee}. For low values of V_{ee}, the trend may well be a rise in output voltage with temperature.

In the "diodes out" mode of operation, the change in output voltage with temperature is also largely dependent on the ratio U. If $\alpha^2U/2$ is greater than 1, the temperature coefficient of the output voltage may be negative. If $\alpha^2U/2$ is approximately equal to 1, the "diodes out" performance approaches the "diodes in" performance because the temperature-sensitive terms become very small and the variation of α with temperature is the only determining factor. If $\alpha^2U/2$ is substantially less than 1, the positive-temperature-coefficient terms should predominate, and an operating point that rises with increases in temperature will result.

Eq. (78) indicates that the basic decrease in g_m as the temperature rises (because of the KT/q term) can be cancelled or overcome if the value selected for the supply voltage V_{ee} or for the ratio X is low enough. This condition implies that, with the diodes out of the circuit, the gain can be made to decrease, re-

main constant, or increase with an increase in temperature.

With the diodes in the circuit, the decrease in gain with rises in temperature is not compensated and is about 2 dB per 100°C rise for very small values of the emitter resistors R_e. These emitter resistors tend to diminish the difference in the temperature characteristic for operation with the diodes in and with the diodes out. Thus, in circuits in which the external emitter resistors are not used, a greater difference will be observed for the two conditions in both gain and operating-point temperature dependence.

Even if there were no significant difference in the temperature characteristics of the two modes of operation, the inclusion of the diodes would be worthwhile because they allow a change in operating point without substantial change in the ratio X, as would be necessary if diodes were not used. Such variation in the ratio X could result in very undesirable temperature characteristics for some operating points as shown in Figs. 41 and 42.

Selection of Parameters for the Current-Sink Circuit

Equations have been derived to show the dependence of the gain and operating point of the differential-amplifier integrated circuits on temperature. These equations, which have been verified experimentally, provide accurate predictions of the characteristics of these important parameters with changes in temperature. Engineering judgment can then be used to specify all resistor ratios for any given combination of gain, operating point, and supply voltage.

Absolute values for the collector load resistor R_L and the resistor combination R_t are established by the bandwidth requirements of the circuit. The absolute value of the resistors R_1 and R_2, which determines the ratio X, is not controlled except as required by the following practical considerations:

1. The power dissipated in the bias circuit is inversely proportional to the absolute values of the resistors R_1 and R_2. Thus, the smaller the absolute values of the resistors, the higher the power dissipated in the bias circuit becomes.
2. The dependence of the ratio U on beta is reduced as the absolute values of the resistors R_1 and R_2 are decreased. Thus, the smaller the resistors are, the smaller the variations in U with changes in beta.

These conflicting considerations indicate that a compromise is required in the selection of the absolute values of R_1 and R_2.

Another factor that must be considered, before a final decision of the absolute value of R_1 is made, is the effect of the impedance in the base circuit on the output impedance of the current-sink transistor.

The output impedance of the current-sink transistor is both finite and frequency-dependent, rather than infinite and constant with frequency as implied in an ideal current source. Moreover, the output impedance is dependent upon the input impedance because of the non-unilateral characteristic of the current-sink transistor.

The output impedance must be high compared to the parallel emitter input impedances of the differential pair of transistors; otherwise, the current-source requirements are not met. Also, the common-mode gain is simply one-half the ratio of the differential-amplifier collector resistor to the equivalent impedance feeding the emitters. Because the common-mode gain in a differential amplifier should be as low as possible, the larger the impedance of the current source, the higher the common-mode rejection should be. (Common-mode rejection is the ratio of the differential gain to the common-mode gain.)

A quantitative evaluation of the output impedance and its dependence on the base resistor values may be made with the help of a transistor model. The model that best represents the integrated-circuit transistor used in the linear analog (differential-amplifier) integrated circuits is shown in Fig. 50. In this model, the substrate series resistance R_s is small enough so that its effect is negligible below frequencies of 100 MHz. The substrate-to-collector leakage

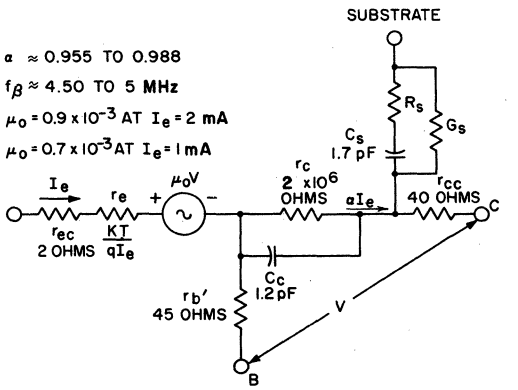


Fig. 50 — Equivalent-circuit model of an integrated-circuit transistor.

G_s is small, but not necessarily negligible, and therefore is represented.

From this model, the output admittance Y_{out} of a common-emitter single stage that has a base termination admittance of P times the common-emitter short-circuit input admittance is given by the following equation:

$$Y_{out} = G_s + j\omega C_s + \frac{\alpha\mu_o}{D}\frac{P}{1+P} + \frac{1}{DZ_c}\left[R_e + r_b' + \frac{\beta R_e}{1+P}\right] \quad (83)$$

where

$$D = R_e + (1-\alpha)r_b' \approx R_e \quad (84)$$

and R_e includes any external emitter resistor plus the internal emitter resistances r_{ec} and r_e. When Eq. (84) is substituted in Eq. (83), the expression for Y_{out} becomes

$$Y_{out} = G_s + j\omega C_s = \frac{\alpha\mu_o}{R_e}\frac{P}{1+P} - \frac{1}{Z_c}\left[1 + \frac{r_b'}{R_e} + \frac{\beta}{1+P}\right] \quad (85)$$

Fig. 51 shows the low-frequency output impedance of the current-sink transistor as a function of the base terminating resistance for various values of the emitter resistor. It is evident that the smaller the termination resistance in the base, the higher

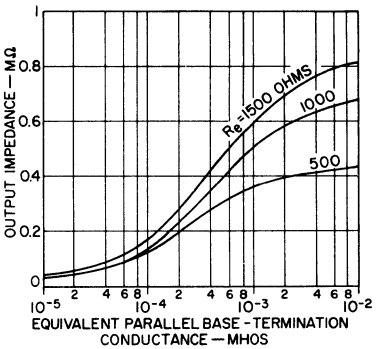


Fig. 51 — Low-frequency output impedance of the current-sink transistor as a function of the equivalent parallel base-termination conductance for several values of the emitter resistance.

the output impedance becomes. The selection of a very small resistor, however, is precluded by the high power dissipation that results in the base bias network.

Fig. 52 shows that the absolute value of output impedance varies inversely with frequency, primarily because of the collector capacitances. Even at frequencies as high as 100 MHz, the impedance is several hundred ohms for a base terminating conductance of 1 millimho (i.e., $G_b = 10^{-3}$ mho). This relatively high impedance, which is many times greater than the emitter impedances at the junctions of the differential pair of transistors, implies that, although the common-mode rejection will not be as high as desired at 100 MHz, the signal path will not be appreciably shunted by the constant current-sink transistor.

Fig. 53 shows the effects of the emitter resistor on the rate of the inverse change in output impedance with frequency. In effect, the larger the value selected for the emitter resistor, the higher the low-frequency output impedance becomes, and the

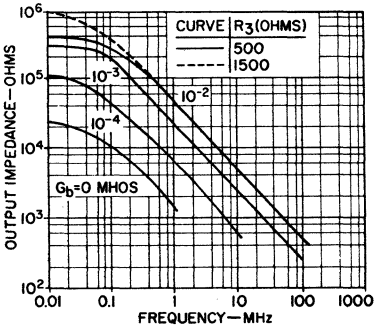


Fig. 52 — Absolute value of output impedance of the current-sink transistor as a function of frequency for several values of the base-termination conductance.

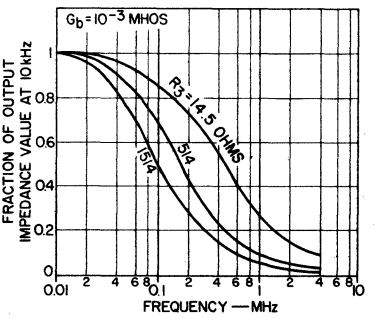


Fig. 53 — Effect of the emitter resistor (R_3) of the current-sink transistor on the change in output impedance with frequency.

lower the frequency at which the roll-off caused by the collector capacitances occurs.

Figs. 54 and 55 show that the phase angle of the output reaches 90 degrees (the condition which represents a pure capacitive output impedance) at a frequency of a few megahertz. The curves in these figures also show the relative effects of the emitter resistor and the base-termination resistance on the relationship between frequency and phase angle.

The variation in the power dissipated in the base bias network as a function of the sum of the base bias resistors, for a supply voltage V_{ee} of 6 volts, is shown in Fig. 56. The sum of

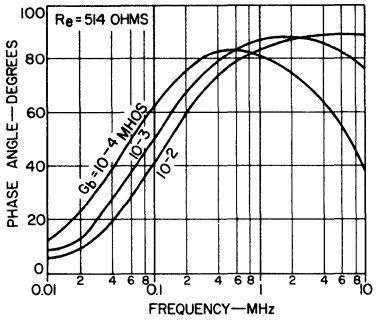


Fig. 54 — Output-impedance phase angle of the current-sink transistor as a function of frequency for several values of base-termination conductance.

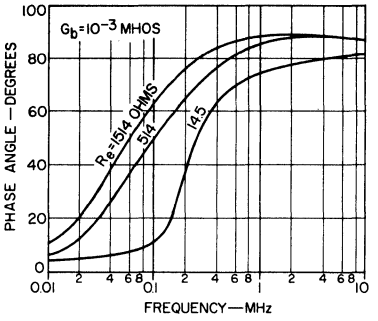


Fig. 55 — Output-impedance phase angle of the current-sink transistor as a function of frequency for several values of emitter resistance.

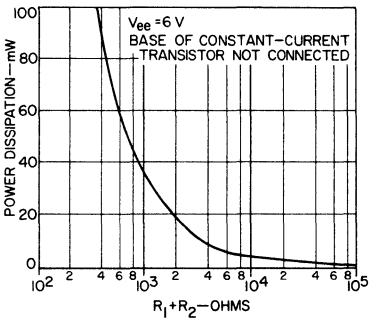


Fig. 56 — Power dissipation in the bias network of the current-sink transistors as a function of the sum of base-bias resistors R_1 and R_2.

the base-bias resistors, R_1 and R_2, should be greater than 7000 ohms to limit the dissipation to less than 5 milliwatts.

On the basis of these considerations, the final values for the parameters in the current-sink circuit can be selected. The value of the resistor R_1 is chosen as 5000 ohms. For the conditions $D_1 = 0$ and $D_2 = 2$ ("diodes in" mode of operaton), the ratio X is 0.5, and R_2 is also 5000 ohms. The sum $R_1 + R_2$ then is 10,000 ohms. The equivalent base termination resistance R_1X can be calculated as follows:

$$R_1X = R_1\left(\frac{R_2}{R_1 + R_2}\right) = 2500 \text{ ohms}$$

At a temperature of 20°C and for a transistor beta of 35, the quantity $(1 - \alpha)\ R_1X$ is about 70 ohms, which is more than 10 per cent of the value of a 500-ohm emitter resistor but only about 3 per cent of the value of a 3000-ohm emitter resistor.

For the "diodes out" mode of operation ($D_1 = D_2 = 0$), if the value of R_1 is again 5000 ohms and the ratio X is 0.36, R_1X is 1800 ohms. The quantity $(1 - \alpha)\ R_1X$ then represents a resistance of 50 ohms. The ratio R_1/R_2, as determined from Eq. (53), is 1.78, and the value of R_2 becomes 2800 ohms. The sum $R_1 + R_2$ is then 7800 ohms.

The circuit adopted as the final configuration for the transistor constant-current sink is shown in Fig. 57. This circuit

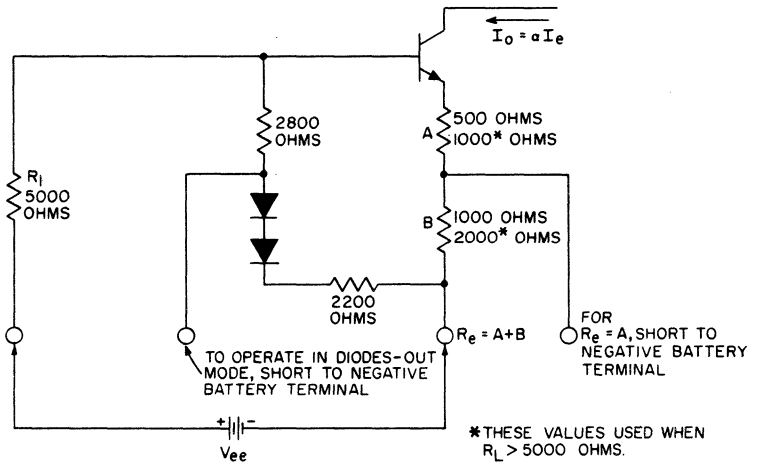


Fig. 57 — Current-sink configuration used in linear (differential-amplifier) integrated circuits.

which includes provisions for both modes of operation ("diodes in" and "diodes out") is used as the standard constant-current sink for RCA linear integrated circuits. Circuits that have a high value of collector load resistance (i.e., low-frequency, high-gain circuits) require larger values of emitter resistors than circuits that have low values of collector load resistance. The resistor values for each operating condition are indicated on the circuit schematic shown in Fig. 57.

Integrated-Circuit Operational-Amplifier Configuration

The term "operational amplifier" was originally intended to denote an amplifier circuit that performed various mathematical operations such as integration, differentiation, summation, and subtraction. The application of the operational amplifier, however, has been so vastly extended that, today, this term suggests a device that finds the widest use in such applications as signal amplification and wave shaping, servo and process controls, analog instrumentation and system design, impedance transformation, and many other routine functions. This versatile circuit may also be used in many nonlinear applications such as voltage comparators, analog-to-digital and digital-to-analog converters, logarithmic amplifiers, and nonlinear function generators.

The great versatility and many advantages of operational amplifiers stem from the use of negative feedback to control response characteristics. If the amplifier circuit provides sufficient gain, the closed-loop amplifier characteristics become a function of only the feedback components. The versatility in the application of the operational amplifier, therefore, is limited primarily by only the ingenuity of the circuit designer in the selection and arrangement of feedback components.

GENERAL CONSIDERATIONS

An ideal operational amplifier would have infinite open-loop gain and bandwidth and zero noise, offset, and drift. Although no amplifier has these ideal qualities, practical operational amplifiers are generally characterized by the following properties:

1. extremely high dc voltage gain, generally in the range from 10^3 to 10^6;
2. wide bandwidth that starts at dc and rolls off to unity gain at from 1 to 100 MHz with a slope of 6 dB per octave or at most 12 dB per octave;

3. positive and negative output voltage over a large dynamic range, usually from ± 10 to ± 100 volts;
4. very low input dc offset and drift with time and temperature;
5. high input impedance so that amplifier input current can be largely neglected.

The configuration most commonly used for operational amplifiers is a cascade of two differential-amplifier circuits, such as that described in the preceding section, together with an appropriate output stage. The cascaded differential-amplifier stages not only fulfill the operational-amplifier requirement for a high-gain direct-coupled amplifier circuit, but also provide significant advantages with respect to the application of the operational amplifier.

From an applications standpoint, the versatility of an operational amplifier that has a differential input is substantially greater than that of the single-input type of operational amplifier. The increased versatility of the differential-input operational amplifier results from the greater flexibility allowed in the selection of the feedback configuration. In the single-input operational amplifier, only the inverting type of feedback configuration can be employed. When differential inputs are employed, the operational amplifier may use either an inverting feedback configuration or a noninverting feedback configuration, which is dependent upon the common-mode rejection for its negative feedback. The characteristics of an operational amplifier may differ significantly depending upon the type of feedback used. The two types, therefore, tend to complement each other. Moreover, because the characteristics provided by each feedback configuration are required equally often, the differential-input operational amplifier is, from an applications standpoint, twice as versatile as the single-input operational amplifier.

The differential-input operational amplifier is readily adapted to integrated-circuit construction techniques. As pointed out in the preceding section, a differential-amplifier circuit is a stable dc-amplifier configuration that lends itself particularly well to the monolithic diffusion process used in the construction of the silicon integrated circuits. In addition, symmetrical differential-amplifier stages can be dc-cascaded readily, provided that each succeeding stage is driven push-pull by the preceding stage. The common-mode effects that result from this arrangement make possible stable, direct-coupled cascades.

The capabilities and limitations of operational amplifiers are

firmly defined by a few very simple equations and rules, which are based on a certain set of criteria that an operational amplifier must meet. Effective use of these simple relationships, however, requires knowledge of the conditions under which each is applicable so that errors that may result from various approximations are held to a minimum. This section explores the theory of the design and use of operational amplifiers, and develops each pertinent design equation in a general way. Evaluations are then made to determine the assumptions that must be made (or the criteria the operational amplifier must meet) to reduce these general equations to classical operational-amplifier design equations.

Frequency instabilities in the operational amplifier and the methods used to prevent them are also discussed. A thorough understanding of the principles of frequency stability is imperative to the successful application of operational amplifiers. The basic concepts and techniques involved in phase compensation (frequency stabilization) are explained in terms of (1) basic frequency-stability requirements, (2) the problems that may result from an uncontrolled frequency response, and (3) the techniques that may be used to correct these undesirable effects. (Specific applications of practical integrated-circuit operational amplifiers are described in a subsequent section.)

Finally, the basic criteria for an operational amplifier are given. This discussion is placed last because a basic insight to the theory of application is required before the effects of many of the operational-amplifier requirements can be fully appreciated.

BASIC THEORY OF OPERATIONAL AMPLIFIERS

In the development of the basic equations and concepts associated with the use of operational amplifiers, the precise formulations for the transfer functions, the input impedances, the output impedances, and the loop gains are presented for both the inverting and the noninverting feedback configurations, and classical design equations are then derived from these precise formulations. The effects of the load impedance and of common-mode gain (or common-mode rejection) on the inverting and noninverting feedback configurations are considered separately.

Inverting Feedback Configuration

An operational amplifier operated with an inverting feedback configuration is shown in Fig. 58. The load resistor R_L is assumed

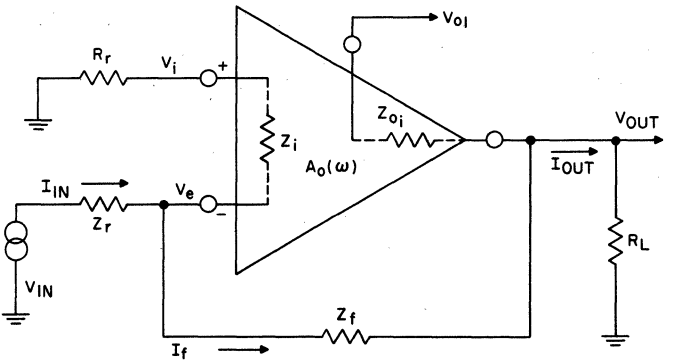


Fig. 58 — Inverting-feedback operational-amplifier configuration.

to be large enough so that its effect on the transfer characteristic is negligible, i.e., $I_{OUT} = 0$. (The effects of a finite R_L are investigated and evaluated subsequently in the discussion of the equivalent-circuit model of an operational amplifier.)

Certain differential-input operational amplifiers require a significant flow of bias current at each input. For this condition, the dc paths to ground for each input must be equal so that a minimum dc offset voltage (error) is developed at the output. Thus, for the terminology employed in Fig. 58, R_r must equal the parallel combination of $Z_r(\omega = 0)$ with the series combination of $Z_f(\omega = 0)$ and Z_{oi} $(\omega = 0)$.

In the circuit of Fig. 58, the drive-source impedance affects the feedback in the inverting configuration and, therefore, must be considered part of the Z_r term. For brevity, the symbol Z_r is defined to include the source impedance as well as certain feedback design elements. The impedances Z_i and Z_{oi} are the open-loop *intrinsic* input and output impedances of the operational amplifier. Ordinarily, these impedances are assumed in the amplifier symbol. In Fig. 58, however, they are identified to emphasize their importance in the ensuing equations. The term $A_o(\omega)$ is the open-loop differential voltage gain of the operational amplifier; this parameter is frequency-dependent. The terminals on the operational-amplifier symbol labeled minus (−) and plus (+) refer to the inverting and noninverting input, respectively.

Inverting-Configuration Transfer Function — The transfer function or closed-loop gain of an operational amplifier is generally considered to express the relationship between the input and output voltages. (It is relatively simple to convert the voltage transfer function to another desired transfer relationship.) In the

derivation of the transfer function for the schematic in Fig. 58, the following differential-amplifier relationship is used as the starting point:

$$V_{o1} = -A_o(\omega)\,(V_e - V_i) \tag{86}$$

where V_e and V_i are defined as follows:

$$V_e = \frac{V_{IN}\,(Z_f+Z_{oi})/\!/(Z_i+R_r)}{Z_r + (Z_f+Z_{oi})/\!/(Z_i+R_r)} + \frac{V_{o1}\,Z_r/\!/(Z_i+R_r)}{Z_f + Z_{oi} + Z_r/\!/(Z_i+R_r)} \tag{87}$$

and

$$V_i = V_e\,R_r/(Z_i + R_r) \tag{88}$$

(In these and subsequent equations, the load resistor R_L is assumed to approach infinity.)

If the expressions for V_e and V_i given by Eqs. (87) and (88) are substituted in Eq. (86), the resulting expression can be simplified as follows:

$$V_{o1} = \frac{-A_o(\omega)\,Z_i\,(Z_f+Z_{oi})\,V_{IN}}{(Z_f+Z_{oi})\,(Z_i+R_r)+Z_r\,(Z_f+Z_{oi}+Z_i+R_r)+A_o(\omega)Z_i\,Z_r} \tag{89}$$

The output voltage V_{OUT} is expressed in terms of V_{o1} and V_{IN} by the following equation:

$$V_{OUT} = \frac{V_{o1}\,[Z_f + Z_r/\!/(Z_i + R_r)]}{Z_{oi} + Z_f + Z_r/\!/(Z_i + R_r)} + \frac{V_{IN}\,Z_{oi}\,(Z_f + Z_{oi})/\!/(Z_i + R_r)}{(Z_f + Z_{oi})\,[Z_r + (Z_f + Z_{oi})/\!/(Z_i + R_r)]} \tag{90}$$

With V_{o1} defined as indicated by Eq. (89), the accurate equation for the transfer response (for $R_L \to \infty$) becomes

$$\frac{V_{OUT}}{V_{IN}} = \frac{Z_{oi}\,(Z_i+R_r) - A_o(\omega)\,Z_i\,Z_f}{(Z_f+Z_{oi})\,(Z_i+R_r)+Z_r\,(Z_f+Z_{oi}+Z_i+R_r)+A_o(\omega)Z_iZ_r} \tag{91}$$

If Z_i is assumed to be much greater than the combination of Z_r in parallel with $Z_f + Z_{oi}$, and if Z_{oi} is assumed to be much smaller than Z_f, then the closed-loop gain (or transfer function) may be expressed as follows:

$$\frac{V_{OUT}}{V_{IN}} \doteq \frac{-A_o(\omega)\,Z_f}{Z_f + Z_r + A_o(\omega)\,Z_r} \tag{92}$$

In addition, if the open-loop gain $A_o(\omega)$ is the dominant term in either Eq. (91) or (92), the transfer-function equation for the in-

verting configuration simplifies to the following familiar expression:

$$\frac{V_{OUT}}{V_{IN}} \underset{\text{=====}}{A_o(\omega) \rightarrow \infty} - \frac{Z_f}{Z_r} \tag{93}$$

Eq. (93) is considered to be the classical or ideal expression for the closed-loop gain (transfer function) for an operational amplifier that uses the inverting type of feedback configuration.

The difference between the open-loop gain and the closed-loop gain is in itself an important design parameter. This "gain throwaway", which is known as the loop gain L.G., is defined by the following equation:

$$\text{L. G.} = \frac{\text{open-loop gain, } A_o(\omega)}{\text{closed-loop gain, } \dfrac{V_{OUT}}{V_{IN}}} \tag{94}$$

When the transfer function is given by Eq. (92), the loop-gain equation may be written as follows:

$$\text{L. G.} = -\frac{Z_f + Z_r}{Z_f} - \frac{A_o(\omega)}{\dfrac{Z_f}{Z_r}} \tag{95}$$

Moreover, when the open-loop gain is very large, the inverting loop gain can be considered to be the open-loop gain divided by the *ideal* inverting closed-loop gain. The equation for L.G. then becomes

$$\text{L. G.} \doteq \frac{-A_o(\omega)}{\dfrac{Z_f}{Z_r}} \tag{96}$$

The loop-gain parameter can be used to predict the accuracy of the approximate operational-amplifier relationships. In general, the higher the loop gain, the more accurate the results provided by the approximate (or classical) relationships. This correlation is demonstrated in TableII, which compares values of V_{OUT}/V_{IN} obtained from the precise transfer expression, Eq. (91), with

Table II—*Comparison of Precise and Approximate Formulas for Closed-Loop Gain (Inverting Configuration)*

Conditions: $A_o(\omega) = 1000\ \underline{/0°}$, $Z_1 = 15{,}000\ \underline{/0°}$, $Z_{o_1} = 200\ \underline{/0°}$, $Z_r = 1000\ \underline{/0°}$.

$Z_f\ \underline{/0°}$ (ohms)	V_{OUT}/V_{IN} from Eq. (93) (dB)	V_{OUT}/V_{IN} from Eq. (91) (dB)	Error (dB)	L.G. (dB)
200,000	46.0	44.3	1.70	14.0
100,000	40.0	39.1	0.90	20.0
30,000	29.6	29.3	0.30	30.4
10,000	20.0	19.9	0.10	40.0
2,000	6.03	6.0	0.03	54.0

values obtained from the classical approximation, Eq. (93), for various gain settings. The tabular data show that the classical equation is accurate to within 1 dB provided the loop gain is at least 20 dB. Eq. (96) was used to calculate all of the loop-gain values given in the table.

Inverting-Configuration Input Impedance, Z_{IN} — The input impedance Z_{IN} for the inverting-feedback configuration of an operational amplifier, shown in Fig. 58, can be expressed as follows:

$$Z_{IN} = \frac{V_{IN}}{I_{IN}} \tag{97}$$

where

$$I_{IN} = \frac{V_{IN} - V_e}{Z_r} \tag{98}$$

Therefore,

$$Z_{IN} = \frac{Z_r}{1 - \dfrac{V_e}{V_{IN}}} \tag{99}$$

The ratio V_e/V_{IN} may be determined by substituting the expression for V_{o1} given by Eq. (89) into Eq. (87) and dividing through by V_{IN} (with $R_L \to \infty$.) The resultant equation is then simplified to obtain the following relationship:

$$\frac{V_e}{V_{IN}} = \frac{(Z_f + Z_{oi})(Z_i + R_r)}{Z_r(Z_f + Z_{oi} + Z_i + R_r) + (Z_f + Z_{oi})(Z_i + R_r) + A_o(\omega) Z_i Z_r} \tag{100}$$

If this expression for V_e/V_{IN} is substituted into Eq. (99), the result can be simplified to obtain the following precise expression for the closed-loop input impedance:

$$Z_{IN} = Z_r + \frac{(Z_f + Z_{oi})(Z_i + R_r)}{(Z_f + Z_{oi} + Z_i + R_r) + A_o(\omega) Z_i} \tag{101}$$

If $A_o(\omega)$ is dominant and Z_{oi} is small, Eq. (101) reduces to

$$Z_{IN} \doteq Z_r + \frac{Z_f (Z_i + R_r)}{A_o(\omega)\, Z_i} \tag{102}$$

A further simplification is possible when R_r is much smaller than Z_i, which is a common condition. In this case, the equation for the input impedance becomes

$$Z_{IN} \doteq Z_r + \frac{Z_f}{A_o(\omega)} \tag{103}$$

Eqs. (102) and (103), which are important in voltage-summing

or scaling-adder* applications, can be used to predict the degree of interaction among multiple inputs.

When $A_o(\omega)$ is large enough, Eqs. (102) and (103) may be rewritten as follows:

$$Z_{IN} \xrightarrow{A_o(\omega) \to \infty} Z_r \tag{104}$$

Eq. (104) is the "classical" equation for the input impedance of an operational amplifier when an inverting-feedback configuration is used. This equation, together with Eq. (101), implies the existence of a condition known as a virtual ground at the node-assigned voltage V_e (shown in Fig. 58). That is, the node is at ground potential even though there is no electrical connection between this point and ground. [This statement can be verified either intuitively by the use of Eq. (104) or directly if $A_o(\omega)$ is assumed to be infinite in Eq. (100)]. Moreover, no current flows into the negative terminal of the amplifier when the open-loop gain is infinite because the voltage V_e is zero while the impedance at the negative terminal (i.e., $Z_i + R_r$) is not zero. The concept of a virtual ground leads to an extremely simple three-step analysis procedure for an inverting operational-amplifier configuration.

1. Because of the virtual ground ($V_e = 0$), the input current I_{IN} and feedback current I_f can be defined as follows:

$$I_{IN} = \frac{V_{IN}}{Z_r} \tag{105}$$

$$I_f = \frac{-V_{OUT}}{Z_f} \tag{106}$$

2. Zero current flow into the inverting terminal ($V_e = 0$) indicates the following relationships:

$$I_{IN} = I_f \tag{107}$$

$$\frac{V_{IN}}{Z_r} = \frac{-V_{OUT}}{Z_f} \tag{108}$$

3. Eq. (108) can then be rewritten to obtain the classical gain equation, as follows:

$$\frac{V_{OUT}}{V_{IN}} = -\frac{Z_f}{Z_r} \tag{109}$$

**A scaling adder is an inverting operational-amplifier configuration which weights and sums multiple voltages.*

Although the foregoing analysis is certainly an idealized one, it is nevertheless practical because the required approximations are usually valid. Eq. (100) serves as a measure of the deviation from a true virtual ground.

Inverting-Configuration Output Impedance, Z_{OUT} — The closed-loop output impedance is the ratio of the unloaded output voltage V_{OUT} to the short-circuit output current I_{OUT} as follows:

$$Z_{OUT} = \frac{V_{OUT}\ (R_L \rightarrow \infty)}{I_{OUT}\ (R_L \rightarrow 0)} \tag{110}$$

It is apparent from Fig. 58 then that the output current I_{OUT} is given by

$$I_{OUT}\ (R_L \rightarrow 0) = \frac{-A_o(\omega)\ (V_e - V_i)}{Z_{oi}} \tag{111}$$

If the expression given by Eq. (88) is substituted for V_i, Eq. (111) can be rewritten as follows:

$$I_{OUT}\ (R_L \rightarrow 0) = \frac{-A_o(\omega)\ Z_i\ V_e}{Z_{oi}\ (Z_i + R_r)} \tag{112}$$

Under short-circuit conditions ($R_L = 0$), the voltage V_e in terms of V_{IN} is given by

$$V_e = \frac{V_{IN}\ Z_f /\!/ (Z_i + R_r)}{Z_r + Z_f /\!/ (Z_i + R_r)} = \frac{V_{IN}\ Z_f\ (Z_i + R_r)}{Z_r\ (Z_f + Z_i + R_r) + Z_f\ (Z_i + R_r)} \tag{113}$$

Therefore, I_{OUT} (at $R_L = 0$) can be expressed in terms of V_{IN} as follows:

$$I_{OUT} = \frac{-A_o(\omega)\ Z_i\ Z_f\ V_{IN}}{Z_{oi}\ [Z_r\ (Z_f + Z_i + R_r) + Z_f\ (Z_i + R_r)]} \tag{114}$$

If this expression for I_{OUT} is substituted in Eq. (110) and consideration is given to the intransience of V_{IN} in going from an unloaded to a fully loaded condition, the equation for Z_{OUT} becomes

$$Z_{OUT} = \frac{Z_{oi}\ [Z_r\ (Z_f + Z_i + R_r) + Z_f\ (Z_i + R_r)]}{-A_o\ (\omega)\ Z_i\ Z_f} \left(\frac{V_{OUT}}{V_{IN}}\right) \tag{115}$$

Finally, the desired equation for the closed-loop output impedance is obtained if the expression for V_{OUT}/V_{IN} given by Eq. (91) is substituted into Eq. (115), as follows:

$$Z_{OUT} = \frac{Z_{oi}[Z_r(Z_f + Z_i + R_r) + Z_f(Z_i + R_r)][A_o(\omega)Z_iZ_f - Z_{oi}(Z_i + R_r)]}{A_o(\omega)Z_iZ_f[Z_r(Z_f + Z_{oi} + Z_i + R_r) + (Z_f + Z_{oi})(Z_i + R_r) + A_o(\omega)Z_iZ_r]} \tag{116}$$

If the open-loop gain term $A_o(\omega)$ is dominant, Eq. (116) simplifies to

$$Z_{OUT} \doteq \frac{Z_{oi}\,[Z_r\,(Z_f + Z_i + R_r) + Z_f\,(Z_i + R_r)]}{A_o(\omega)\,Z_i\,Z_r} \qquad (117)$$

This expression for Z_{OUT} does not simplify to its "classical" equation unless Z_i is dominant also; in this case, Eq. (117) becomes

$$Z_{OUT} \doteq Z_{oi}\,\frac{1 + \frac{Z_f}{Z_r}}{A_o(\omega)} \qquad (118)$$

The assumption that Z_i is a dominant term is not always valid, especially if bipolar transistor inputs are employed. Eq. (117), therefore, may be considered to take precedence over Eq. (118).

Noninverting Feedback Configuration

Fig. 59 shows the general circuit for an operational amplifier operated with a noninverting feedback configuration. In this section, the equations for the transfer function and the closed-loop

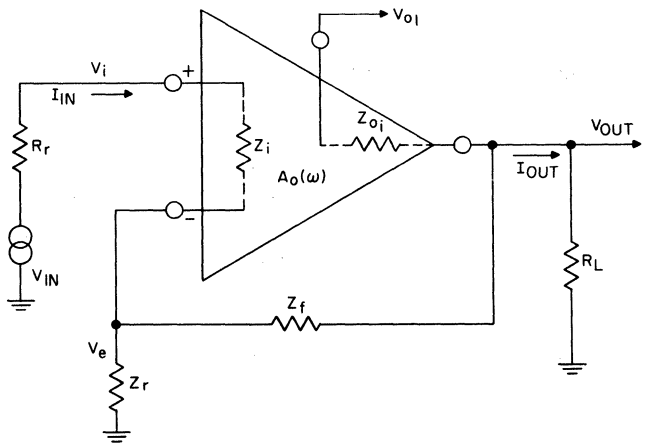


Fig. 59 — Noninverting-feedback operational-amplifier configuration.

input impedance for this type of operational-amplifier circuit are derived. These derivations, as did those for the inverting circuit, assume that the load resistor R_L is large enough so that its effect is negligible, i.e., $R_L \to \infty$ and $I_{OUT} = 0$. (The effects of a finite load resistance on the noninverting operational amplifier are evaluated in the discussion of the equivalent-circuit model of an operational amplifier.)

A noninverting operational amplifier, unlike the inverting type, requires a differential-input arrangement because it uses the common-mode effect in its feedback scheme. The following basic requirements and definitions that apply to the inverting circuit shown in Fig. 58 are also valid for the general noninverting circuit of Fig. 59:

1. The dc return paths to ground for the two inputs must be equal and finite for amplifiers that require a significant amount of input bias current.
2. The input and output impedances, Z_i and Z_{o_i}, are inherent in the basic amplifier unit and are shown on the diagram to emphasize their importance in the relationships to be derived.
3. The open-loop gain is frequency-dependent and is represented by the symbol $A_o(\omega)$.
4. The plus and minus labels on the input terminals designate the noninverting and inverting terminals, respectively.

In the noninverting circuit, however, the source impedance is included in the passive element R_r rather than the frequency-dependent parameter Z_r, as in the inverting circuit.

Noninverting-Configuration Transfer Function — As with the inverting circuit, the transfer function developed for the noninverting operational amplifier shows the relationship between the input and output voltages. It is relatively simple to convert this relationship to another type of transfer function.

When the load resistor R_L approaches infinity, the output voltage V_{OUT} for the general circuit shown in Fig. 59 can be expressed as follows:

$$V_{OUT} = \frac{V_{o1}\,[Z_f + Z_r /\!\!/ (Z_i + R_r)]}{Z_{o_i} + Z_f + Z_r /\!\!/ (Z_i + R_r)} + \frac{V_{IN}\,Z_{o_i}\,[Z_r /\!\!/ (Z_f + Z_{o_i})]}{(Z_f + Z_{o_i})\,[Z_i + R_r + Z_r /\!\!/ (Z_f + Z_{o_i})]} \tag{119}$$

Eq. (119) may be rewritten in the following form:

$$V_{OUT} = \frac{V_{o1}\,[Z_f\,(Z_r + Z_i + R_r) + Z_r\,(Z_i + R_r)] + Z_r\,Z_{o_i}\,V_{IN}}{(Z_i + R_r)\,(Z_r + Z_f + Z_{o_i}) + Z_r\,(Z_f + Z_{o_i})} \tag{120}$$

The voltage V_{o_1} is defined by the differential-gain expression, as follows:

$$V_{o1} = A_o(\omega)\,(V_i - V_e) \tag{121}$$

where V_i is the source voltage V_{IN} less the voltage drop across R_r, as given by

$$V_i = V_{IN} - I_{IN} R_r \tag{122}$$

where

$$I_{IN} = \frac{V_i - V_e}{Z_i} \tag{123}$$

The voltage V_i, given by Eq. (122), can now be expressed in terms of the voltages V_{IN} and V_e, as follows:

$$V_i = \frac{Z_i V_{IN} + R_r V_e}{Z_i + R_r} \tag{124}$$

It can be determined from Fig. 59 that, when R_L approaches infinity, the voltage V_e is given by the following equation:

$$V_e = \frac{V_{o1} Z_r /\!\!/ (Z_i + R_r)}{Z_{oi} + Z_f + Z_r /\!\!/ (Z_i + R_r)} + \frac{V_{IN} Z_r /\!\!/ (Z_f + Z_{oi})}{Z_i + R_r + Z_r /\!\!/ (Z_f + Z_{oi})} \tag{125}$$

If the relationships for V_{o1} and V_i given by Eqs. (121) and (124), respectively, are used, V_e can be expressed solely in terms of V_{IN}, as shown by the following equation:

$$V_e = \frac{(Z_r Z_f + Z_r Z_{oi} + A_o(\omega) Z_i Z_r) V_{IN}}{(Z_i + R_r)(Z_r + Z_f + Z_{oi}) + Z_r (Z_f + Z_{oi}) + A_o(\omega) Z_i Z_r} \tag{126}$$

Eqs. (121), (124), and (126) are now used to express V_{o1} in terms of V_{IN}, as follows:

$$V_{o1} = \frac{A_o(\omega) Z_i (Z_r + Z_f + Z_{oi}) V_{IN}}{(Z_i + R_r)(Z_r + Z_f + Z_{oi}) + Z_r (Z_f + Z_{oi}) + A_o(\omega) Z_i Z_r} \tag{127}$$

If this expression for V_{o1} is substituted into Eq. (120), the new equation that results can be simplified and divided through by V_{IN} to obtain the desired transfer function, as follows:

$$\frac{V_{OUT}}{V_{IN}} = \frac{Z_r Z_{oi} + A_o(\omega) Z_i (Z_r + Z_f)}{(Z_i + R_r)(Z_r + Z_f + Z_{oi}) + Z_r (Z_f + Z_{oi}) + A_o(\omega) Z_i Z_r} \tag{128}$$

The transfer function that is usually associated with the noninverting feedback configuration of an operational amplifier can be derived from Eq. (128) if the impedance Z_{oi} is assumed to be zero and the impedance Z_i is assumed to be very high. When these assumptions are made, Eq. (128) becomes

$$\frac{V_{OUT}}{V_{IN}} \doteq \frac{(Z_r + Z_f) A_o(\omega)}{(Z_r + Z_f) + Z_r A_o(\omega)} \tag{129}$$

Eq. (129) may be rewritten as follows:

$$\frac{V_{OUT}}{V_{IN}} \doteq \frac{A_o(\omega)}{1 + \dfrac{A_o(\omega)}{1 + Z_f/Z_r}} \tag{130}$$

If the term $A_o(\omega)$ is dominant in Eq. (130), the following "classical" expression for the noninverting transfer response results:

$$\frac{V_{OUT}}{V_{IN}} \xrightarrow{A_o(\omega) \to \infty} 1 + \frac{Z_f}{Z_r} \tag{131}$$

The term $1 + Z_f/Z_r$ represents the closed-loop gain for the *ideal* noninverting configuration. This term, which is referred to as the *ideal feedback characteristic,* is basic to operational-amplifier frequency-stabilization theory.

As might be expected, the loop gain of an operational amplifier is defined in the same way [by Eq. (94)] regardless of the type of feedback configuration. Under the conditions for which Eq. (130) is a valid expression for the transfer response, the loop gain for the noninverting configuration is given by

$$\text{L. G.} = 1 + \frac{A_o(\omega)}{1 + \dfrac{Z_f}{Z_r}} \tag{132}$$

If the second term of Eq. (132) is very large, this equation reduces to

$$\text{L. G.} \doteq \frac{A_o(\omega)}{1 + \dfrac{Z_f}{Z_r}} \tag{133}$$

Table III compares the values calculated from the precise and the approximate expressions [Eqs. (128) and (131), respectively] for the closed-loop gain of the noninverting operational-amplifier configuration. The approximate formula is accurate to within 1 dB provided the loop gain is 20 dB or more. A com-

Table III—*Comparison of Precise and Approximate Formulas for Closed-Loop Gain (Noninverting Configuration)*

Conditions: $A_o(\omega) = 1000 \angle 0°$, $Z_i = 15{,}000 \angle 0°$, $Z_{o_i} = 200 \angle 0°$, $Z_r = 1000 \angle 0°$.

$Z_f \angle 0°$ (ohms)	V_{OUT}/V_{IN} from Eq. (131) (dB)	V_{OUT}/V_{IN} from Eq. (128) (dB)	Error (dB)	L. G. from Eq. (133) (dB)
199,000	46.0	44.3	1.70	14.0
99,000	40.0	39.1	0.90	20.0
29,000	29.6	29.3	0.30	30.4
9,000	20.0	19.9	0.10	40.0
1,000	6.03	6.0	0.03	54.0

parison of Tables II and III shows that the error introduced by the use of the classical gain formula for the noninverting configuration [Eq. (131)] is identical to that introduced by the use of the classical gain formula for the inverting configuration [Eq. (93)].

Noninverting-Configuration Input Impedance, Z_{IN} — The following equation gives the basic definition of the input impedance Z_{IN}:

$$Z_{IN} = \frac{V_{IN}}{I_{IN}} \tag{134}$$

It can be readily determined from Fig. 59 that the input current I_{IN} is given by

$$I_{IN} = \frac{V_{IN} - V_e}{Z_i + R_r} \tag{135}$$

When this relationship is applied in Eq. (134), the expression for the noninverting input impedance becomes

$$Z_{IN} = \frac{Z_i + R_r}{1 - \frac{V_e}{V_{IN}}} \tag{136}$$

If the expression for the ratio of V_e/V_{IN}, given previously by Eq. (126), is substituted into Eq. (136), the result can be simplified to obtain the following precise expression for the input impedance (for $R_L \rightarrow \infty$):

$$Z_{IN} = Z_i + R_r + Z_r \frac{Z_f + Z_{oi} + A_o(\omega)\, Z_i}{Z_r + Z_f + Z_{oi}} \tag{137}$$

For the case where Z_i is dominant and Z_{oi} is small, Eq. (137) reduces to

$$Z_{IN} \doteq Z_i + \frac{A_o(\omega)\, Z_i}{1 + \frac{Z_f}{Z_r}} \tag{138}$$

The following expression for the input impedance results if $A_o(\omega)$ is also considered dominant:

$$Z_{IN} \doteq \frac{A_o(\omega)\, Z_i}{1 + \frac{Z_f}{Z_r}} \tag{139}$$

Eq. (139) states that the noninverting input impedance is equal to the intrinsic input impedance Z_i multiplied by the loop gain.

Noninverting-Configuration Output Impedance, Z_{OUT} — As in the inverting configuration, the closed-loop output impedance for the noninverting configuration is defined as the ratio of the

open-circuit output voltage, V_{OUT}, to the short-circuit output current, I_{OUT}, as follows:

$$Z_{OUT} = \frac{V_{OUT}\ (R_L \to \infty)}{I_{OUT}\ (R_L \to 0)} \tag{140}$$

where

$$I_{OUT}\ (R_L \to 0) = \frac{A_o(\omega)\ (V_i - V_e)}{Z_{o_i}} \tag{141}$$

For the general noninverting operational-amplifier configuration, the voltages V_i and V_e are given by the following equations for the conditions indicated:

$$V_i\ (R_L \to 0) = \frac{V_{IN}\ (Z_i + Z_r /\!\!/ Z_f)}{R_r + Z_i + Z_r /\!\!/ Z_f} \tag{142}$$

and

$$V_e\ (R_L \to 0) = \frac{V_{IN}\ Z_r /\!\!/ Z_f}{R_r + Z_i + Z_r /\!\!/ Z_f} \tag{143}$$

On the basis of the relationships expressed by Eqs. (142) and (143), Eq. (141) may be rewritten as follows:

$$I_{OUT}\ (R_L \to 0) = \frac{A_o(\omega)\ V_{IN}\ Z_i\ (Z_r + Z_f)}{Z_{o_i}\ [(Z_r + Z_f)\ (R_r + Z_i) + Z_r\ Z_f]} \tag{144}$$

The output impedance Z_{OUT} then becomes

$$Z_{OUT} = Z_{o_i}\left[\frac{Z_r\ Z_f + (Z_r + Z_f)\ (R_r + Z_i)}{A_o(\omega)\ Z_i\ (Z_r + Z_f)}\right]\left(\frac{V_{OUT}}{V_{IN}}\right) \tag{145}$$

Finally, the following precise equation for the output impedance Z_{OUT} is obtained when the ratio for V_{OUT}/V_{IN} is replaced by its impedance equivalent, as given by Eq. (128):

$$Z_{OUT} = \frac{Z_{o_i}\ [(Z_r+Z_f)\ (R_r+Z_i) + Z_r\ Z_f]\ [Z_r\ Z_{o_i} + A_o(\omega)Z_i\ (Z_r+Z_f)]}{[A_o(\omega)Z_i\ (Z_r+Z_f)]\ [(Z_i+R_r)\ (Z_r+Z_f+Z_{o_i}) + Z_r\ (Z_f+Z_{o_i}) + A_o(\omega)Z_i\ Z_r]} \tag{146}$$

If $A_o(\omega)$ is dominant, then Eq. (146) becomes

$$Z_{OUT} \doteq Z_{o_i}\left[\frac{Z_r\ Z_f + (Z_r + Z_f)\ (R_r + Z_i)}{A_o(\omega)\ Z_i\ Z_r}\right] \tag{147}$$

The expression for the closed-loop output impedance does not revert to its classical form unless both the intrinsic input impedance Z_i and the open-loop gain $A_o(\omega)$ are very large. Under such conditions, the equation for the output impedance reduces to

$$Z_{OUT} \doteq Z_{o_i} \frac{1 + \frac{Z_f}{Z_r}}{A_o(\omega)} \qquad (148)$$

This classical expression indicates that the output impedance of the noninverting configuration is equal to the intrinsic output impedance Z_{o_i} divided by the loop gain. It should be noted that the classical expressions for the closed-loop output impedances for the inverting and noninverting configurations [Eq. (118) and (148), respectively] are identical.

Effect of Finite Load Impedance on Operational-Amplifier Characteristics

Fig. 60 shows the equivalent circuit of a closed-loop operational amplifier. This equivalent circuit is valid for either the inverting or the noninverting configuration. In the inverting

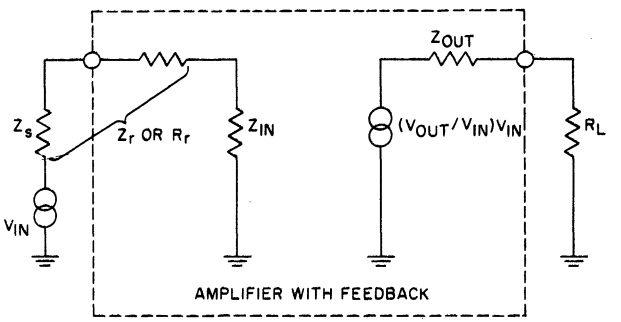


Fig. 60 — Equivalent-circuit model of a closed-loop operational amplifier.

configuration, Z_r is used to represent the impedance in series with the closed-loop input impedance Z_{IN}. In the noninverting configuration, term Z_r is replaced by R_r to show that the components thus represented are independent of frequency. The closed-loop input and output impedances (Z_{IN} and Z_{OUT}, respectively) and the transfer function V_{OUT}/V_{IN} were defined previously.

One of the important features of the equivalent-circuit model is that it accurately accounts for the effects of a finite load impedance, R_L. For example, if a 2000-ohm load impedance is used on the 46-dB (approximate) inverting amplifier for which data are given in TableII, the equation for the transfer response must be

modified as follows:

$$V_{OUT} = \frac{\left(\frac{V_{OUT}}{V_{IN}}\right) V_{IN} R_L}{R_L + Z_{OUT}} \tag{149}$$

If Eq. (91) is used to determine the value of V_{OUT}/V_{IN} and Eq. (115) is used to determine the value of Z_{OUT}, the transfer-function ratio for an R_L of 2000 ohms can be calculated from Eq. (149) as follows:

$$\frac{V_{OUT}}{V_{IN}} = 164 \left(\frac{2000 \text{ ohms}}{37.4 \text{ ohms} + 2000 \text{ ohms}}\right) = 162 \tag{150}$$

Thus, a ratio of 44.15 dB is obtained, as compared to 44.3 dB for an open-circuit load. Similarly, if a 2000-ohm load is used for the 6-dB amplifier, the gain becomes 5.98 dB, as compared to 6 dB indicated in Table I for an open-circuit load. The error in neglecting a 2000-ohm load, therefore, is 0.15 dB for the 46-dB amplifier and only 0.02 dB for the 6-dB amplifier (for the conditions given in TableII).

Effect of the Common Mode Gain (CMG) on Operational-Amplifier Characteristics

In the developments of the basic equations for the inverting and noninverting feedback configurations of the operational amplifier, it was tacitly assumed that the common-mode gain was essentially zero (infinite attenuation). The common-mode gain is defined as the ratio of the output voltage, V_{OUT}, to the input voltages, V_i and V_e, when V_i and V_e are identical in amplitude and phase. The validity of this assumption is considered separately in this section because the basic feedback equations become burdensome when common-mode effects are included. As a result, the salient features of these equations become obscured.

An examination of Figs. 58 and 59 shows that, in either the inverting or noninverting configuration, the differential gain acts on the difference between the voltages V_i and V_e. On the other hand, the common-mode gain acts on those portions of V_i and V_e that are in phase and identical in magnitude. That is, the common-mode gain acts on the smaller of the two in-phase signals (V_i or V_e). In the inverting configuration V_i is less than V_e, but in the noninverting configuration V_i is greater than V_e. These conditions are reflected by the output-voltage equations when the

effects of the common-mode gain (CMG) are considered, as follows:

1. For the inverting configuration,

$$V_{o_1} = A_o(\omega)(V_i - V_e) - (CMG)(V_i) \tag{151}$$

2. For the noninverting configuration,

$$V_{o_1} = A_o(\omega)(V_i - V_e) - (CMG)(V_e) \tag{152}$$

If these two equations are developed further, the following gain expressions are obtained for $Z_{o_i} = 0$ (i.e., $V_{o_i} = V_{OUT}$):

1. For the inverting configuration,

$$\frac{V_{OUT}}{V_{IN}} = \frac{-A_o(\omega)\,Z_i\,Z_f - (CMG)\,R_r\,Z_f}{Z_r(Z_f+Z_i+R_r)+Z_f(Z_i+R_r)+Z_i\,Z_r\,A_o(\omega)+R_r\,Z_r\,(CMG)} \tag{153}$$

2. For the noninverting configuration,

$$\frac{V_{OUT}}{V_{IN}} = \frac{A_o(\omega)\,Z_i\,(Z_r+Z_f) - (CMG)\,Z_r\,Z_f}{(Z_r+Z_f)(R_r+Z_i)+Z_r\,Z_f+A_o(\omega)\,Z_i\,Z_r+(CMG)\,Z_r\,(Z_i+R_r)} \tag{154}$$

In each case, the criteria for the common-mode gain, CMG, to be negligible compared to the open-loop gain, $A_o(\omega)$, are as follows:

1. For the inverting configuration,

$$CMG \ll \frac{A_o(\omega)\,Z_i}{R_r} \tag{155}$$

2. For the noninverting configuration,

$$CMG \ll \frac{A_o(\omega)\,Z_i}{Z_i + R_r} \tag{156}$$

Eq. (153) or inequality (155) shows that the gain of an inverting configuration is not affected by the common-mode gain when the input impedance V_i is assumed to be infinite. However, when this same assumption is made for a noninverting configuration, the gain is dependent upon the common-mode gain provided the open-loop gain is finite.

Inequalities (155) and (156) may be given in terms of the common-mode rejection, CMR, which is the open-loop gain, $A_o(\omega)$, divided by the common-mode gain, CMG. The following inequalities are then obtained:

1. For the inverting configuration,

$$\text{CMR} \gg \frac{R_r}{Z_i} \tag{157}$$

2. For the noninverting configuration,

$$\text{CMR} \gg \frac{Z_i + R_r}{Z_i} \tag{158}$$

Neither of these inequalities places a stringent restriction on common-mode rejection.

PHASE SHIFTS IN OPERATIONAL-AMPLIFIER FEEDBACK

In an operational amplifier, as in any other feedback amplifier, the phase of the feedback must be controlled to assure that the design is stable with frequency and that the desired gain-frequency response is obtained. Fig. 61 shows the gain and phase characteristics as functions of frequency for a typical 60-dB operational amplifier in which no phase-compensation techniques

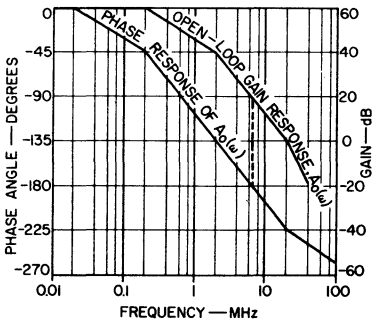


Fig. 61 — Gain and phase response of an open-loop operational amplifier operated without phase compensation.

are employed. Over the frequency range shown, the change in the phase of the feedback is substantially greater than 180 degrees. This phase response indicates that a low-frequency negative feedback can become positive and cause the amplifier to be unstable at high frequencies unless phase-compensation methods are employed to stabilize and control the response of the amplifier.

Effect of Excessive Phase Shift on Frequency Stability

The transfer equation for the inverting configuration, Eq. (92), can be rearranged so that it reflects the same classical

feedback form as that for the noninverting configuration, given by Eq. (130). These equations, which are based on the assumptions that Z_i approaches infinity and Z_{oi} is zero, are repeated below for convenience:

1. For the inverting configuration,

$$\frac{V_{OUT}}{V_{IN}} = \left(\frac{Z_f}{Z_f + R_r}\right)\left[\frac{-A_o(\omega)}{1 + \frac{A_o(\omega)}{1 + \frac{Z_f}{Z_r}}}\right]$$

2. For the noninverting configuration,

$$\frac{V_{OUT}}{V_{IN}} = \frac{A_o(\omega)}{1 + \frac{A_o(\omega)}{1 + \frac{Z_f}{Z_r}}}$$

If the phase angle of the feedback term, $A_o(\omega)/(1 + Z_f/Z_r)$, reaches 180 degrees (not asymptotically) while the magnitude of the term is still unity or greater, oscillations will occur. [If the term is greater than unity, the oscillations will build until limiting occurs. This limiting decreases $A_o(\omega)$, and thus the entire feedback term, until unity magnitude at a phase angle of 180 degrees is achieved.] These unstable conditions can be predicted readily. Fig. 62 shows a superposition of the gain-frequency curve shown

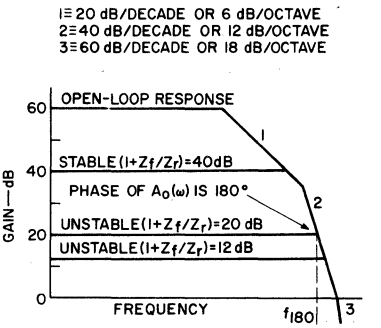


Fig. 62 — Open-loop response and stability characteristics of an operational amplifier.

in Fig. 61 on several sample plots of the ideal feedback characteristic, as given by $1 + Z_f/Z_r$ when Z_f and Z_r are purely resistive. Because the crucial frequency for a purely resistive feedback network is that at which $A_o(\omega)$ has a phase angle of 180 degrees, the

magnitude of $A_o(\omega)/(1 + Z_f/Z_r)$ at this frequency (f_{180}) determines whether the configuration is stable. If $A_o(f_{180})/(1 + Z_f/Z_r)$ is equal to or greater than unity, the configuration is *unstable*. On the other hand, if this term is less than unity, then the configuration is *stable*. This stability-determination technique is applied to the various values of $1 + Z_f/Z_r$ shown in Fig. 62; in each case, the gain of the amplifier at the frequency for which the phase angle is 180 degrees is assumed to be 10 [i.e., $A_o(f_{180})=10$].

When $1 + Z_f/Z_r = 100/\underline{0°}$, the stability ratio is calculated as follows:

$$\frac{A_o(f_{180})}{1 + \dfrac{Z_f}{Z_r}} = \frac{10/\underline{180°}}{100/\underline{0°}} = 0.10/\underline{180°}$$

Because the value of 0.10 obtained for the stability ratio is less than unity, the configuration is stable.

When $1 + Z_f/Z_r = 10.0/\underline{0°}$, the stability ratio becomes

$$\frac{A_o(f_{180})}{1 + \dfrac{Z_f}{Z_r}} = \frac{10/\underline{180°}}{10/\underline{0°}} = 1.0/\underline{180°}$$

For this case, the stability ratio is unity, and the configuration therefore, is unstable. As a check, an examination of the transfer expressions for both the inverting and the noninverting configuration [Eqs. (92) and (130)] reveals that for the condition specified, each contains the following term:

$$\frac{1}{1 + 1/\underline{180°}}$$

which is not finite and, therefore, indicates an oscillating condition.

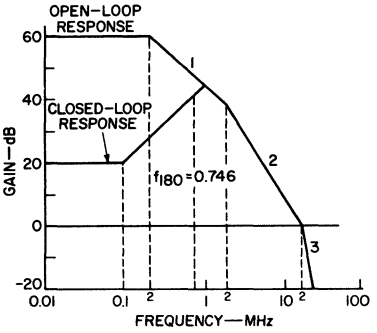
When $1 + Z_f/Z_r = 4.0/\underline{0°}$,

$$\frac{A_o(f_{180})}{1 + \dfrac{Z_f}{Z_r}} = \frac{10/\underline{180°}}{4/\underline{0°}} = 2.50/\underline{180°}$$

The value obtained is greater than unity, and the circuit, therefore, is unstable.

When Z_f and Z_r are not restricted to purely resistive values, a more general situation exists because the phase of $A_o(\omega)/(1 + Z_f/Z_r)$ is no longer dependent solely upon $A_o(\omega)$. Two examples which essentially cover the field are given below.

Example No. 1 — A characteristic of differentiating or peaking circuits is that the feedback term $1 + Z_f/Z_r$ is in the form $K(1 + jf/f_1)$, where K and f_1 are constants. Fig. 63 shows a curve



$$A_o(\omega) = \frac{1000}{\left(1 + j\frac{f}{0.2\,MHz}\right)\left(1 + j\frac{f}{2\,MHz}\right)\left(1 + j\frac{f}{20\,MHz}\right)}$$

$$1 + \frac{Z_f}{Z_r} = 10\left(1 + j\frac{f}{0.1\,MHz}\right)$$

Fig. 63 — Basic peaking response characteristics of an operational amplifier.

of this term as a function of frequency, for K = 10 and f_1 = 0.1 MHz, superimposed upon an operational-amplifier open-loop transfer curve. The equation for the open-loop characteristic can be derived from Fig. 62, as follows:

$$A_o(\omega) = \frac{1000}{\left(1 + j\frac{f}{0.2\,MHz}\right)\left(1 + j\frac{f}{2\,MHz}\right)\left(1 + j\frac{f}{20MHz}\right)} \quad (159)$$

The frequency at which the stability ratio $A_o(\omega)/1 + Z_f/Z_r$ has a phase angle of 180 degrees and the magnitude of the ratio for this frequency can then be calculated. The computation reveals that the phase angle is 180 degrees at a frequency (f_{180}) of 0.746 MHz, and the magnitude of the ratio is 3.22 at that frequency. The stability ratio is greater than one; therefore, the configuration is *unstable*. The point of instability (f_{180}) is marked in Fig. 63.

The stability of an operational amplifier may be determined more easily from an *estimate* of the phase angle of the ratio $A_o(\omega)/(1 + Z_f/Z_r)$ at the frequency of intersection (where the magnitude

of the ratio is unity). If the estimate shows that the phase angle is less than 180 degrees, the configuration is stable. On the other hand, if the estimate indicates a phase angle in excess of 180 degrees, the circuit is unstable. When the estimate shows that the phase angle is near 180 degrees, an accurate calculation is required to determine whether the operational amplifier is stable. This border-line type of configuration, however, is generally undesirable from the standpoint of frequency response, as discussed later.

In the application of the estimation technique to the problem presented in Fig. 63, the following conditions should be noted: The feedback characteristic $1 + Z_f/Z_r$ increases at the rate of 6 dB per octave (20 dB per decade) for a full decade before it intersects the open-loop response, $A_o(\omega)$. The intersection occurs near the second corner of the open-loop response, which decreases at the rate of 6 dB per octave for almost a full decade. The classical phase relationships associated with these observations are used to obtain the following phase estimates:

$$\text{Phase of } (1 + Z_f/Z_r) = +90°$$
$$-135° < \text{Phase of } A_o(\omega) < -90°$$

Therefore, the following phase estimate is obtained at the frequency of the intersection:

$$-225° < \text{Phase of } A_o(\omega)/(1 + Z_f/Z_r) < -180°$$

Thus, the configuration is *unstable.*

Example No. 2—An inherent characteristic of integrating or band-limiting configurations is that the feedback term $1 + Z_f/Z_r$ has the following form:

$$\frac{K}{1 + jf/f_1}$$

An example of this type of feedback characteristic is shown in Fig. 64 for $K = 10$ and $f_1 = 4$ MHz. The application of the phase-estimation technique to this problem results in the following estimates:

$$-45° > \text{Phase of } 1 + Z_f/Z_r > -90°$$
$$-135° > \text{Phase of } A_o(\omega) > -225°$$

At the frequency of intersection, therefore, the phase estimate is given by

$$-45° > \text{Phase of } A_o(\omega)/(1 + Z_f/Z_r) > -180°$$

Thus, the configuration is *stable.*

If the three basic types of feedback characteristics shown in Figs. 62, 63, and 64 are compared, it becomes evident that the

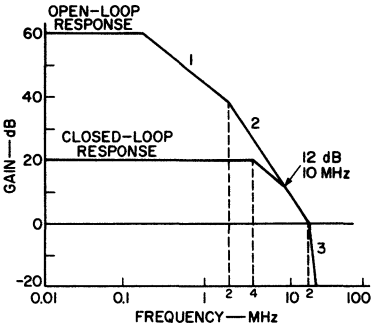


Fig. 64 — Basic integrating response characteristics of an operational amplifier.

differentiating or frequency-peaking configuration is the most unstable and that the integrating or low-pass configuration is the most stable. In fact, the techniques used to devise this latter configuration may be considered a form of phase compensation for certain situations, as discussed later.

Effects of Excessive Phase Shift on Frequency Response

The criterion evolved for frequency stability neither precludes uncontrolled frequency peaking nor provides for a 3-dB closed-loop bandwidth prediction. The conditions that are required to develop a stable, controlled-response feedback amplifier are evolved in this section.

Criteria for a Peaked Response — Frequency peaking results when the magnitude of the true closed-loop gain, as given by Eq. (92) for the inverting configuration and by Eq. (130) for the noninverting configuration, is greater than the magnitude of the ideal closed-loop gain (Z_f/Z_r for an inverting circuit and $1 + Z_f/Z_r$ for a noninverting circuit). The criteria for frequency peaking can be expressed for both configurations by the following expression:

$$\left| \frac{A_o(\omega)}{1 + \frac{A_o(\omega)}{1 + \frac{Z_f}{Z_r}}} \right| > \left| 1 + \frac{Z_f}{Z_r} \right| \qquad (160)$$

Inequality (160) may be used to develop a set of criteria that predict frequency peaking (or preclude the occurrence of frequency peaking).

The following substitution is first made in inequality (160):

$$\frac{A_o(\omega)}{1 + \frac{Z_f}{Z_r}} \equiv B\underline{/\theta} \tag{161}$$

If both sides of inequality (160) are then divided by the left-hand term, the following result is obtained:

$$1 > \left| 1 + \frac{1}{B}\underline{/-\theta} \right| \tag{162}$$

Inequality (162) may be rewritten in either of the following forms:

$$1 > \left[\left(1 + \frac{1}{B}\cos\theta\right)^2 + \left(-\frac{1}{B}\sin\theta\right)^2\right]^{\frac{1}{2}} \tag{163}$$

or

$$1 > \left[1 + \frac{2}{B}\cos\theta + \left(\frac{1}{B}\right)^2\right]^{\frac{1}{2}} \tag{164}$$

The real and imaginary parts of inequality (163) must also be less than unity, so that

$$1 > \left| 1 + \frac{1}{B}\cos\theta \right| \tag{165}$$

and

$$1 > \frac{1}{B}\left| -\sin\theta \right| \tag{166}$$

It is apparent from inequality (165) that

$$B > \frac{1}{2} \tag{167}$$

and from inequality (164) that

$$\cos\theta < -\frac{1}{2B} \tag{168}$$

The substitution indicated by the identity (161) is again made, and both sides of inequality (160) are then divided by the

right-hand term to obtain the following expressions:

$$\left| \frac{B\underline{/\theta}}{1 + B\underline{/\theta}} \right| > 1 \tag{169}$$

or

$$| B\underline{/\theta} | > | 1 + B\underline{/\theta} | \tag{170}$$

For peaking to occur, therefore, the following relationships must be in effect:

$$0.5 < | B\underline{/\theta} | < B$$

$$\cos\theta < -\frac{1}{2B}$$

3-dB Bandwidth Prediction — The 3-dB bandwidth of an operational amplifier is defined by the following condition:

$$\left| \frac{A_o(\omega)}{1 + \frac{A_o(\omega)}{1 + \frac{Z_f}{Z_r}}} \right| = \frac{\left| 1 + \frac{Z_f}{Z_r} \right|}{\sqrt{2}} \tag{171}$$

The terms of Eq. (171) are rearranged and the definition for $B\underline{/\theta}$ given by the identity (161) is used to obtain the following relationships:

$$\left| 1 + \frac{1}{B}\underline{/-\theta} \right| = \sqrt{2}$$

$$\left(1 + \frac{1}{B}\cos\theta\right)^2 + \left(-\frac{1}{B}\sin\theta\right)^2 = 2$$

$$1 + \frac{2}{B}\cos\theta + \left(\frac{1}{B}\right)^2 = 2 \tag{172}$$

Eq. (172) yields the following criteria for the 3-dB point:

$$1 \geq B > \frac{1}{1 + \sqrt{2}} = 0.414 \tag{173}$$

$$\cos\theta = \frac{B^2 - 1}{2B} \tag{174}$$

Inequality (173) predicts the possibility of a 3-dB bandwidth greater than that indicated by the intersection of $A_o(\omega)$ and $1 + Z_f/Z_r$ (B = 1 point). However, it should be realized that this "bandwidth extension" is actually caused by a slight peaking effect. Special care should be exercised in any attempt to use this effect to advantage.

Inequality (174) stipulates that the phase angle must be 90 degrees to obtain the 3-dB bandwidth where B = 1. This stipulation essentially coincides with a "rule of thumb" that has become a standard in the industry. This rule may be stated as follows: *For an unconditionally stable configuration, the ideal feedback characteristic, $1 + Z_f/Z_r$, must intersect the open-loop response, $A_o(\omega)$, at a slope less than 12 dB per octave.* An examination of this "rule of thumb" in terms of the phase relationship indicates that the phase angle asymptotically approaches 180 degrees when the change in amplifier response with frequency occurs at a rate of 12 dB per octave. Therefore, the amplifier is on the threshold of instability. Frequency dependence of less that 12 dB per octave indicates that the amplifier is stable; a dependence of greater than 12 dB per octave indicates that the amplifier is unstable.

PHASE-COMPENSATION TECHNIQUES

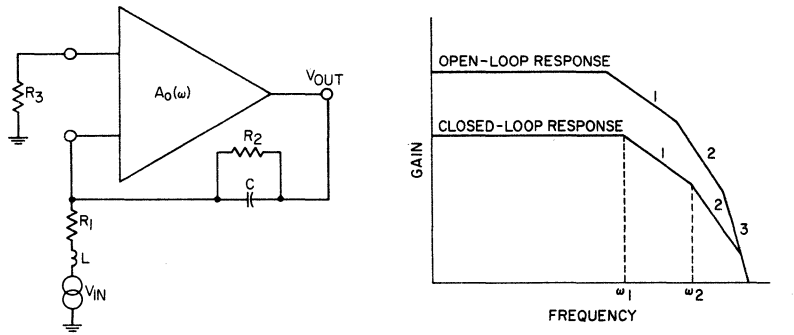
The design problems (i.e., ac instability and uncontrolled frequency response) created by excessive phase shift in the feedback can be solved by use of compensating techniques that alter the feedback response so that excessive phase shifts no longer occur. The frequency response can be controlled by limiting the slope of the intersection of the ideal feedback characteristic, $1 + Z_f/Z_r$, with the open-loop gain response, $A_o(\omega)$, to a safe value. Theoretically, this slope can have a maximum value of 12 dB per octave under certain conditions. In general, however, the maximum slope allowed for practical lumped-parameter systems is 6 dB per octave. In an operational amplifier, effective phase compensation can be accomplished only by a modification in one or more of the following parameters:

1. the ideal closed-loop gain (feedback characteristic), $1 + Z_f/Z_r$;
2. the open-loop input impedance, Z_i;
3. the open-loop gain, $A_o(\omega)$.

Closed-Loop Method

Phase compensation can be accomplished by modification of the closed-loop gain characteristic (i.e., the $1 + Z_f/Z_r$ term) for only those applications in which the intersection of the $1 + Z_f/Z_r$ characteristic with the open-loop response occurs in a region where the open-loop response rolls off at a slope of 12 dB per octave or 18 dB per octave. When the intersection occurs in a 12-dB-per-octave region of the $A_o(\omega)$ response, compensation techniques are used that cause the slope of the $1 + Z_f/Z_r$ response to roll off at 6 dB per octave near the intersection. As a result of these techniques, the slope of the intersection becomes 6 dB per octave. (An example of this method of phase compensation was discussed earlier, in the section on "Criteria for a Peaked Response", and the response curves for this example were shown in Fig. 64.)

For applications in which the use of an inductor is permissible, phase compensation in the 18-dB-per-octave region of the open-loop response can be accomplished by techniques that cause the $1 + Z_f/Z_r$ response to roll off at 12 dB per octave near the intersection. An example of this method of phase compensation, together with the appropriate response curves, is shown in Fig. 65.



$$R_3 = R_1 /\!\!/ R_2$$

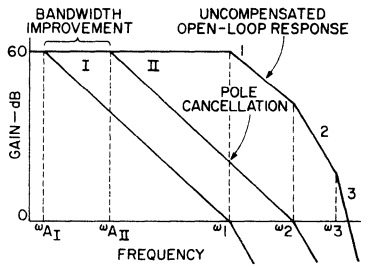
$$\frac{V_{OUT}}{V_{IN}} = \frac{-\dfrac{R_2}{1 + j\omega CR_2}}{R_1 + j\omega L} = -\frac{R_2}{R_1}\left[\frac{1}{\left(1 + j\dfrac{\omega L}{R_1}\right)(1 + j\omega CR_2)}\right]$$

Fig. 65 — Phase compensation of operational amplifier permissible in the "three-slope region."

In this example, the Z_f term is altered by a shunt capacitor and the Z_r term is altered by a series inductor so that the $1 + Z_f/Z_r$ response has the required 12-dB-per-octave roll-off. The location of these frequency-dependent components in the feedback configuration is unique for this type of phase compensation.

Open-Loop Methods

Phase-compensation techniques that alter either the open-loop input impedance or the open-loop gain permit the introduction of a zero, in addition to the low-frequency pole, into the open-loop gain characteristic. This zero can be designed to cancel one of the poles in the open-loop gain characteristic and thus to increase substantially the bandwidth of the operational amplifier. Alternatively, the operational-amplifier bandwidth can be increased by the introduction of a pole at a frequency low enough so that all the other corner points will occur at frequencies below that at which the open-loop response, $A_o(\omega)$, intersects the closed-loop response, $1 + Z_f/Z_r$. The two methods are compared in Fig. 66. It is apparent that the pole-cancellation method of phase compensation is superior to the method in which the other corner



I—Compensated open-loop response using simple depression of higher corner frequencies.

II—Compensated open-loop response using pole cancellation.

Fig. 66 — Phase compensation of operational amplifier by use of pole cancellation.

frequencies are depressed. In the phase-compensation techniques discussed below, therefore, the pole-cancellation method is employed.

Modification of the Open-Loop Input Impedance — The following analysis shows the limitations imposed on alterations in

the open-loop input impedance of an operational amplifier in order to provide phase compensation. In this phase-compensation technique, an appropriate network is connected between the input terminals so that it appears in parallel with the intrinsic input impedance, Z_i. Eqs. (92) and (130), which define the closed-loop inverting and noninverting responses, respectively, are used as the basis for establishing the conditions and the mechanisms involved in this kind of compensation.

If Z_i' is used to represent the modified open-loop input impedance and the open-loop output impedance, Z_{oi}, is assumed to be zero, the following equations for the closed-loop response are obtained:

1. For the inverting configuration,

$$\frac{V_{OUT}}{V_{IN}} = \frac{-A_o(\omega)\, Z_i'\, Z_f}{Z_f\,(Z_i' + R_r) + Z_r\,(Z_f + Z_i' + R_r) + A_o(\omega)\, Z_i'\, Z_r} \tag{175}$$

2. For the noninverting configuration,

$$\frac{V_{OUT}}{V_{IN}} = \frac{A_o(\omega)\, Z_i'\,(Z_r + Z_f)}{(Z_i' + R_r)\,(Z_r + Z_f) + Z_r\, Z_f + A_o(\omega)\, Z_i'\, Z_r} \tag{176}$$

A judicious rearrangement of terms in Eqs. (175) and (176) reveals the effect that the altered open-loop input impedance has on the open-loop response. With this rearrangement, the equation for the inverting configuration becomes

$$\frac{V_{OUT}}{V_{IN}} = \frac{-\left[\dfrac{A_o(\omega)\, Z_i'}{R_r + Z_r + Z_i'}\right] Z_f}{Z_f + \dfrac{Z_r\,(Z_i' + R_r)}{R_r + Z_r + Z_i'} + \left[\dfrac{A_o(\omega)\, Z_i'}{R_r + Z_r + Z_i'}\right] Z_r} \tag{177}$$

The equation for the noninverting configuration is then written as follows:

$$\frac{V_{OUT}}{V_{IN}} = \frac{\left[\dfrac{A_o(\omega)\, Z_i'}{R_r + Z_r + Z_i'}\right] (Z_r + Z_f)}{Z_f + \dfrac{Z_r\,(Z_i' + R_r)}{R_r + Z_r + Z_i'} + \left[\dfrac{A_o(\omega)\, Z_i'}{R_r + Z_r + Z_i'}\right] Z_r} \tag{178}$$

For each configuration, the modified open-loop response is defined as follows:

$$A_o'(\omega) \equiv \frac{A_o(\omega)\, Z_i'}{R_r + Z_r + Z_i'} \tag{179}$$

It is apparent from Eq. (179) that the alteration of the open-loop input impedance has no effect on the open-loop response unless

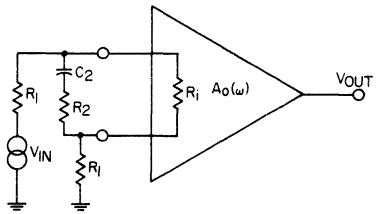
Z_i' is, at most, of the same order of magnitude as the $R_r + Z_r$ term. If Z_i' is made much less than $R_r + Z_r$, Eq. (179) becomes

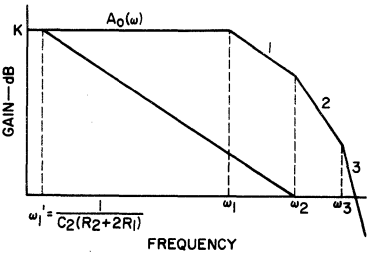
$$A_o'(\omega) \doteq \frac{A_o(\omega)\, Z_i'}{R_r + Z_r} \tag{180}$$

As predicted by Eqs. (179) and (180), three limitations are imposed in the use of the input-impedance modification technique to provide phase compensation: (1) the feedback impedance term Z_r is restricted in value and configuration by the phase-compensation requirements; (2) the effective open-loop input impedance must be smaller in magnitude than and different in configuration from the intrinsic input impedance, Z_i (thus the closed-loop input impedance, Z_{IN}, also is smaller and different); and (3) the dc open-loop gain is less for some input-impedance configurations.

Two examples of the input-impedance phase-compensation technique are shown in Figs. 67 and 68. In the method shown in Fig. 67, the required modification of the open-loop response is achieved by proper choice of the frequency characteristics for the network connected in shunt with the input terminals of the operational amplifier. Fig. 68 shows that the required modification of the response can be achieved by the appropriate choice of the frequency characteristics of R_r and Z_r. Both techniques employ pole-zero cancellation to extend the 6 dB-per-octave roll-off region depicted. The technique illustrated in Fig. 67 causes an early roll-off, while the one shown in Fig. 68 results in a reduction in the dc open-loop gain. Eqs. (179) and (180) indicate that phase-compensation can also be effected by an increase in the magnitude of $R_r + Z_r$, provided that the frequency characteristics of this parameter are controlled. However, this technique relies on the accuracy of the value of Z_i and therefore is unsatisfactory. (The intrinsic input impedance of an operational amplifier may vary significantly from unit to unit.)

Modification of Open-Loop Gain Characteristics — Phase compensation that is effected by internal modification of the open-loop gain response is the most widely accepted technique for integrated-circuit operational amplifiers. This method offers two distinct advantages over other types of phase compensation. First, the internal-modification technique affords complete isolation of the phase-compensation networks from the feedback parameters. This isolation is not possible with the compensation methods discussed previously. Second, the point at which the phase com-





$A_o(\omega)$ = uncompensated open-loop gain
$A_o'(\omega)$ = compensated open-loop gain
R = low-frequency intrinsic input impedance

$$A_o'(\omega) = \frac{\pm A_o(\omega) R_i \left(R_2 + \frac{1}{j\omega C_2}\right)}{\left(R_i + R_2 + \frac{1}{j\omega C_2}\right) 2R_1 + R_i \left(R_2 + \frac{1}{j\omega C_2}\right)}$$

$$A_o'(\omega) = \left[\frac{\pm A_o(\omega) R_i}{2R_1 + R_i}\right]\left[\frac{1 + j\omega R_2 C_2}{1 + j\omega C_2 \left(R_2 + \frac{2R_i R_1}{2R_1 + R_i}\right)}\right]$$

Because R_i is normally large, the equation for $A_o'(\omega)$ may be rewritten as follows:

$$A_o'(\omega) = \pm A_o(\omega) \frac{1 + j\omega R_2 C_2}{1 + j\omega C_2 (R_2 + 2R_1)}$$

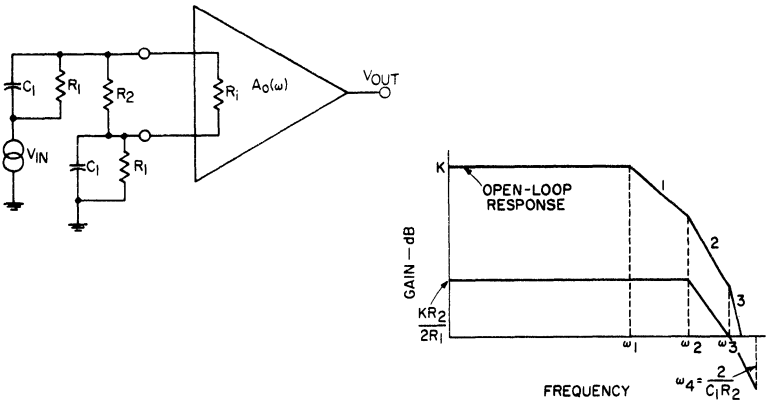
For $$A_o(\omega) = \frac{K}{\left(1 + j\frac{\omega}{\omega_1}\right)\left(1 + j\frac{\omega}{\omega_2}\right)\left(1 + j\frac{\omega}{\omega_3}\right)}$$

and if $$R_2 C_2 = \frac{1}{\omega_1}$$

the equation for $A_o'(\omega)$ becomes

$$A_o'(\omega) = \frac{\pm K}{[1 + j\omega C_2 (R_2 + 2R_1)]\left(1 + j\frac{\omega}{\omega_2}\right)\left(1 + \frac{\omega}{\omega_3}\right)}$$

Fig. 67 — Phase compensation of operational amplifier in which open-loop response is modified by connection of a compensating network that provides the required frequency characteristics in shunt with input terminals.



$A_o(\omega)$ = uncompensated open-loop gain
$A_o'(\omega)$ = compensated open-loop gain

$$A_o'(\omega) = \frac{\pm A_o(\omega)\, R_2\, R_i}{(R_2 + R_i)\left(\dfrac{2\,R_1}{1 + j\omega_1 R_1 C_1}\right) + R_2 R_i}$$

$$= \left[\frac{\pm A_o(\omega)\, R_2 R_i}{2R_1(R_2+R_i) + R_2 R_i}\right]\left[\frac{1 + j\omega\, R_1 C_1}{1 + j\omega \dfrac{R_1 R_2\, R_1 C_1}{2R_1(R_2+R_i) + R_2 R_i}}\right]$$

Because R_i is normally large, the equation for $A_o'(\omega)$ may be rewritten as follows:

$$A_o'(\omega) = \left(\frac{\pm A_o(\omega)\, R_2}{2R_1 + R_2}\right)\left(\frac{1 + j\omega\, R_1\, C_1}{1 + j\omega \dfrac{C_1 R_1\, R_2}{2R_1 + R_2}}\right)$$

If $R_2 << R_1$, the equation for $A_o'(\omega)$ becomes

$$A_o'(\omega) \doteq \left(\frac{\pm A_o(\omega)\, R_2}{2R_1}\right)\left(\frac{1 + j\omega R_1\, C_1}{1 + j\omega C_1 \dfrac{R_2}{2}}\right)$$

For $$A_o(\omega) = \frac{K}{\left(1 + j\dfrac{\omega}{\omega_1}\right)\left(1 + j\dfrac{\omega}{\omega_2}\right)\left(1 + j\dfrac{\omega}{\omega_3}\right)}$$

and $$R_1\, C_1 \equiv \frac{1}{\omega_1},$$

the compensated open-loop gain $A_o'(\omega)$ is given by

$$A_o'(\omega) = \frac{\pm K}{2\dfrac{R_1}{R_2}\left(1 + j\omega C_1 \dfrac{R_2}{2}\right)\left(1 + \dfrac{\omega}{\omega_2}\right)\left(1 + \dfrac{\omega}{\omega_3}\right)}$$

Fig. 68 — Phase compensation of operational amplifier in which open-loop response is modified by alteration of the $R_r + Z_r$ term to provide the required frequency characteristics.

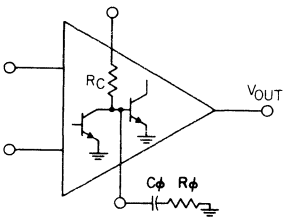
pensation is applied can be selected so that the open-loop response is altered in such a way that one of the existing 3-dB corner frequencies becomes the early roll-off corner in the compensated response. The advantage stems from the fact that no new corner frequencies are introduced, and an improved compensated response is thus obtained.

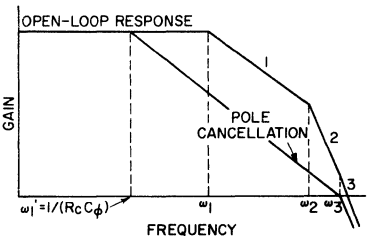
Internal phase compensation can be accomplished by either of two basic methods. In one method, referred to as the straight roll-off, an appropriate RC network is connected across a suitable internal resistor of the operational amplifier. With this method, the early roll-off starts at the corner frequency produced by the phase-compensating capacitor and the internal resistor. The other method is the Miller-effect roll-off. In this method, the phase-compensating network still appears electrically to be placed across an appropriate internal resistance of the amplifier, but is actually connected between the input and the output of an inverting-gain stage in the operational amplifier. The impedance of the compensating network then appears to be divided by the gain of that stage.

The Miller-effect roll-off technique requires a much smaller phase-compensating capacitor than that which must be used with the straight roll-off method. Moreover, the reduction in swing capability which is inherent in the straight roll-off is delayed significantly when the Miller-effect roll-off is used. Fig. 69 illustrates the solution to the problem of phase compensation of an operational amplifier in which a straight roll-off is used to cause the second 3-dB corner frequency to occur at unity gain. Fig. 70 illustrates the use of a Miller-effect roll-off to solve the same problem. For the same early corner frequency, the compensating capacitance required in the Miller-effect method is less than that required in the straight roll-off method by a factor of $1 + g_{m_{II}}R_{c_2}$ ($g_{m_{II}}$ and R_{c_2} are defined in Fig. 70).

DESIGN CRITERIA FOR OPERATIONAL AMPLIFIERS

It is apparent from the previous discussions that a completely universal design of an operational amplifier would have to satisfy an impossible set of criteria. As a result, the design of operational amplifiers is a somewhat specialized process in that a particular amplifier is usually designed for specific applications. For example, certain operational amplifiers are designed to provide high-frequency gain at the expense of other performance characteristics, while other operational amplifiers provide very high gain or high input impedance in low-frequency applications. Integrated-circuit operational amplifiers, which are fabricated by the diffusion





$A_o(\omega)$ = uncompensated open-loop gain
$A_o'(\omega)$ = compensated open-loop gain

$$A_o'(\omega) \doteq A_o(\omega)\left(1 + j\frac{\omega}{\omega_1}\right)\frac{1 + j\omega R_\phi C_\phi}{1 + j\omega R_c C_\phi}$$

The $1 + j\,\omega/\omega_1$ term in the equation above accounts for the modification of the ω_1 3-dB corner.

For
$$R_\phi C_\phi = \frac{1}{\omega_2}$$

and
$$A_o(\omega) = \frac{K}{\left(1 + j\frac{\omega}{\omega_1}\right)\left(1 + j\frac{\omega}{\omega_2}\right)\left(1 + j\frac{\omega}{\omega_3}\right)}$$

the equation for $A_o'(\omega)$ becomes

$$A_o'(\omega) \doteq \frac{\pm K}{(1 + j\omega R_c C_\phi)\left(1 + j\frac{\omega}{\omega_3}\right)}$$

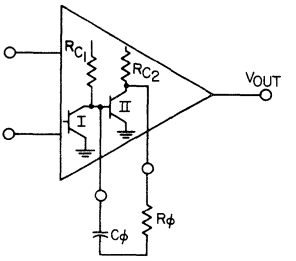
A third corner-frequency term, which occurs because of the time constant of R_ϕ and the input capacitance of the succeeding stage, should also be included in the equation above; the effects of this corner frequency, however, is appreciable only at very high frequencies (and usually at a gain less than unity). Because the corner frequency normally occurs well out of the active region, it is omitted in the expression for $A_o'(\omega)$.

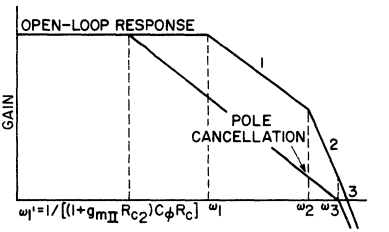
Fig. 69 — Phase compensation of operational amplifier by use of straight-rolloff method to modify open-loop response.

process, can be made suitable for comparator applications or can be processed to provide high gain at low dissipation levels. For these reasons, any discussion of the criteria for operational amplifiers must be of a general nature unless a specific application is being considered.

Input and Output DC Levels

In general, an operational amplifier should be designed so that the dc bias levels at the input and the output are equal. This





$A_o(\omega)$ = uncompensated open-loop gain
$A_o'(\omega)$ = compensated open-loop gain

$$A_o'(\omega) \doteq A_o(\omega)\left(1 + j\,\frac{\omega}{\omega_1}\right)\frac{1 + j\omega R_\phi\, C_\phi}{1 + j\omega R_c\,(1 + g_{mII}\,R_{c_2})\,C_\phi}$$

The $1 + j\,\omega/\omega_1$ term in the expression for $A_o'(\omega)$ accounts for the modification of the ω_1 3-dB corner.

For
$$R_\phi\, C_\phi = \frac{1}{\omega_2}$$

and
$$A_o(\omega) = \frac{K}{\left(1 + j\frac{\omega}{\omega_1}\right)\left(1 + j\frac{\omega}{\omega_2}\right)\left(1 + j\frac{\omega}{\omega_3}\right)}$$

The expression for $A_o'(\omega)$ becomes

$$A_o'(\omega) \doteq \frac{\pm K}{[1 + j\omega\,(1 + g_{mII}\,R_{c_2})\,C_\phi\,R_c]\left(1 + j\,\frac{\omega}{\omega_3}\right)}$$

A third corner frequency, which results from the time constant of R_ϕ and the feedback capacitance C_{bc}', is neglected in the expression for $A_o'(\omega)$, because this corner frequency occurs well out of the active region.

Fig. 70 — Phase compensation of operational amplifier by use of Miller effect to modify open-loop response.

condition is desirable to assure that the resistive feedback network can be connected between the input and the output without upsetting either the differential or the common-mode dc bias. Moreover, for applications in which two (positive and negative) power supplies are used, the operational amplifier should be designed so that it is possible to establish a set of standard supply values for which the equal input and output bias levels are at zero potential with respect to circuit ground. This latter condition is particularly important in direct-coupled cascade and comparator applications.

Output-Power Capability

As with any amplifier circuit, the output-power requirements for an operational amplifier depend almost entirely on the application. A few general conclusions can be drawn concerning the design of the output stage. First, this stage should provide a voltage swing essentially equal to the sum of the power-supply voltages. It should have sufficient gain so that it is the first stage to limit when the amplifier is overdriven. Finally, because of the design trade-off that is always required between output-power capability and dissipation, the output stage should be sufficiently versatile so that the output capability and dissipation can be tailored to the power needs of the particular application in which the operational amplifier is used.

Gain and Frequency-Response Characteristics

The numerical values of the open-loop gain and the 3-dB bandwidth of an operational amplifier are of relatively little importance in themselves. The important requirement is that the open-loop gain must be much greater than the closed-loop gain of the transfer response over the frequency range of interest if an accurate transfer function is to be maintained. (This requirement is explained in detail in the discussions of transfer functions for both the inverting and noninverting configurations.) For example, if a 40-dB amplifier and a 60-dB amplifier are used in a 20-dB gain configuration and the open-loop gain is decreased 50 per cent in each case, the closed-loop gain of the 40-dB amplifier varies only 9 per cent and that of the 60-dB amplifier varies only 1 per cent.

The frequency roll-off characteristics are the prime determinants of the frequency response of an operational amplifier. The greater the rate of roll-off prior to the intersection of the feedback-ratio frequency characteristic with the open-loop response (in the active region), the more difficult phase compensation of the operational amplifier becomes. An 18-dB-per-octave roll-off is generally considered the maximum slope that can occur in the active region before proper phase compensation becomes extremely difficult or impossible to achieve (as indicated in the discussion on the effects of feedback phase shifts). In addition, because operational amplifiers have useful applications down to and including unity gain, the active region of the amplifier may be considered as the entire portion of the frequency characteristic above its 0-dB bandwidth. Therefore, a well-designed amplifier should roll off at no greater than 18 dB per octave until well below unity gain.

Intrinsic Input and Output Impedances

The ideal values for the input and output impedances of an operational amplifier are infinity and zero, respectively (as mentioned in the discussions on input and output impedances for both inverting and noninverting configurations). The degree to which a practical amplifier approximates these values depends, for the most part, upon the application. A 5000-ohm open-loop input impedance may be quite sufficient for one application, while a 0.1-megohm intrinsic input impedance may not be sufficient for another. In most applications, however, the restrictions on the intrinsic input impedance are not severe. The closed-loop input impedance, which is equal to the product of the intrinsic input impedance and the gain "throwaway" or loop gain, is a more critical parameter. This parameter effectively increases the input impedance (decreases input capacitance) and is the reason that many operational amplifiers that have an input roll-off in the active region have no input roll-off in this region after negative feedback is applied.

Because the closed-loop output impedance is also affected by the loop gain (the proportionality is inverse), the same conclusions might be drawn about the importance of the intrinsic output impedance. Another factor, however, affects the restrictions placed upon the open-loop output impedance. A limiting situation in an inverting-configuration application affords an alternate path to the signal when the intrinsic output impedance is sufficiently high. The loop gain decreases to zero as the open-loop gain decreases when overdrive occurs. Therefore, the closed-loop output impedance increases until it equals the intrinsic value at full limiting. Thus, the intrinsic output must be much less than the lowest practical value of feedback impedance or an alternate signal path that effectively bypasses the limiting amplifier will exist through the feedback network.

Common-Mode Rejection

Under differential drive conditions, the common-mode rejection has no drastic effects on the performance of the operational amplifier unless the rejection ratio is extremely low (as discussed in respect to the effects of common-mode gain). However, in a common-mode drive situation, such as in a comparator type of application, high common-mode rejection can be imperative. For example, if a 60-dB differential amplifier having a 50-dB common-mode rejection is used to compare a 1-volt signal against a 1-volt reference, the output will be 3.2 volts when it should be zero.

Such results would be disastrous for many applications of this type. In general, the common-mode rejection should be a minimum of 20 dB greater than the differential gain.

Input Bias Current

Although an amplifier may have a high intrinsic input ac impedance, it can still require a significant amount of dc input bias current. This condition is undesirable in applications in which the drive source cannot accommodate a significant dc current. Examples of such applications are those that require very high impedance sources or sources of a magnetic nature that can be severely unbalanced by a flow of dc current. Unfortunately, the bipolar transistor remedies for this effect add so much capacitance that the frequency response of the amplifier is impaired. Therefore, either field-effect devices should be used in the differential input stage or a scheme should be available to assure that a very low bias current is obtained when it is absolutely necessary. The latter technique requires that sufficient leads be provided so that two external transistors can be added to form a Darlington or a modified Darlington input configuration.

Offset Voltage and Current

The offset voltage of an operational amplifier is the deviation of the output dc level from the arbitrary input-output level usually taken as ground reference when both inputs are shorted together. The offset current is the deviation when the inputs are driven by two identical dc input bias-current constant-current sources. These two offset parameters are usually referred to the input because their output values are dependent on feedback. Under normal operating conditions, the offset in the amplifier results from a combination of the two factors. For example, if an operational amplifier has a 1-millivolt input offset voltage and a 1-microampere input offset current with the inputs returned to ground through 1000-ohm resistors, the total input offset is either zero or 2 millivolts depending upon the phase relationship between the two offset parameters. The offset of an operational amplifier is a dc error and should be minimized for numerous reasons, including the following: (1) The use of an operational amplifier as a true dc amplifier is limited to signal levels much greater than the offset. (2) Comparator applications require that the output voltage be zero (within limits) when the two input signals are equal and in phase. (3) In a direct-coupled cascade, such as a video amplifier chain, the input offset of the first stage determines the offset characteristics of the entire system. Hence, the gain of the system must

be limited to a value that is insufficient to cause limiting at rated output voltage. This value is reduced when the offset is significant.

Power-Supply Stability

The power-supply stability is a measure of the sensitivity that the offset has to power-supply variations. Because the value of the offset at the output is dependent on feedback, this sensitivity is normally referred to the input and expressed in microvolts per volt. In a fixed-installation application that employs heavily regulated power supplies, this parameter is of little importance. In battery-operated applications of the operational amplifier, however, the sensitivity of the offset to power-supply variations is of the utmost importance. In a single-supply system, this sensitivity should be an absolute minimum. In a two-supply system, the difference in the sensitivities to each supply can be minimized because the supplies in many dual systems tend to track. This tracking results in a cancellation, or at least a partial cancellation, of the two sensitivities.

Temperature-Stability Requirements

Temperature stability of an operational amplifier requires stable thermal characteristics for most of the parameters discussed in this section. The stability demands imposed on the temperature characteristics of an operational amplifier are determined to a large extent by the application in which the circuit is used. In certain applications, stable temperature characteristics are of utmost importance; in other applications, the ability of the operational amplifier to perform the required functions is not appreciably affected by variations in circuit parameters with temperature.

In general, the dependence of the open-loop gain on temperature is of less importance than the thermal behavior of the amplifier frequency response. Variations in the intrinsic input and output impedances with temperature are of little consequence provided that the input impedance remains large enough and the output impedance remains small enough to satisfy the requirements of the application. If the value of the input bias current is important for the application in which the operational amplifier is used, stable temperature behavior is just as important. Variations in the offset voltage and current with temperature should always be small because they directly affect the internal biases, and thus the operation, of the operational amplifier.

Description and Applications of RCA Linear Integrated Circuits

The RCA line of linear integrated circuits encompasses a broad variety of devices designed to perform numerous types of circuit functions in many widely diverse applications. This group includes general-purpose and special-purpose circuits, as well as several device and circuit arrays. The balanced differential amplifier is used as the basic building block in both the general-purpose and the special-purpose circuits. These circuits, in general, exhibit excellent gain-frequency characteristics, high common-mode rejection, a wide operating temperature range, and good output-to-input isolation.

Table IV lists the type number and the descriptive name for each device in the RCA linear integrated-circuit family. Because of the exceptional versatility of the general-purpose circuits, however, a single name cannot completely categorize any one of them. The descriptive names assigned to these circuits, therefore, are merely generic designations provided for convenience of identification and are not indicative of the large variety of circuit functions for which they may be used.

DC AMPLIFIER

Fig. 71 shows the schematic diagram of the CA3000 integrated-circuit dc amplifier. This stabilized and compensated differential amplifier provides push-pull outputs, high-impedance (0.1-megohm) inputs, and gain of approximately 30 dB at frequencies up to 1 MHz. Its useful frequency response can be increased to several tens of megahertz by the use of external resistors or coils.

Table IV — *RCA Linear Integrated Circuits*

Descriptive Name	RCA Type No.
General-Purpose Types	
DC Amplifier	CA3000
AF Amplifier	CA3007
Video and Wide-Band Amplifiers	CA3001, CA3021, CA3022, and CA3023
IF Amplifier	CA3002
RF Amplifiers	CA3004, CA3005, CA3006, and CA3028A
Operational Amplifiers	CA3008, CA3008A, CA3010, CA3010A, CA3015, CA3015A, CA3016, CA3016A, CA3029, CA3029A, CA3030, CA3030A, CA3031/702A, CA3032/702C, CA3033, CA3033A, CA3037, CA3037A, CA3038, and CA3038A
Arrays	
Transistor Array	CA3018
Diode Array	CA3019
Wide-Band Amplifier Arrays	CA3035 and CA3035V1
Dual Darlington Array	CA3036
Special-Purpose Types	
Multipurpose Wide-Band Amplifier	CA3020
FM IF Amplifiers	CA3011 and CA3012
FM IF Amplifier/Discriminator/AF Amplifiers	CA3013 and CA3014
Wide-Band Amplifier/Phase Detectors	CA3034 and CA3034V1

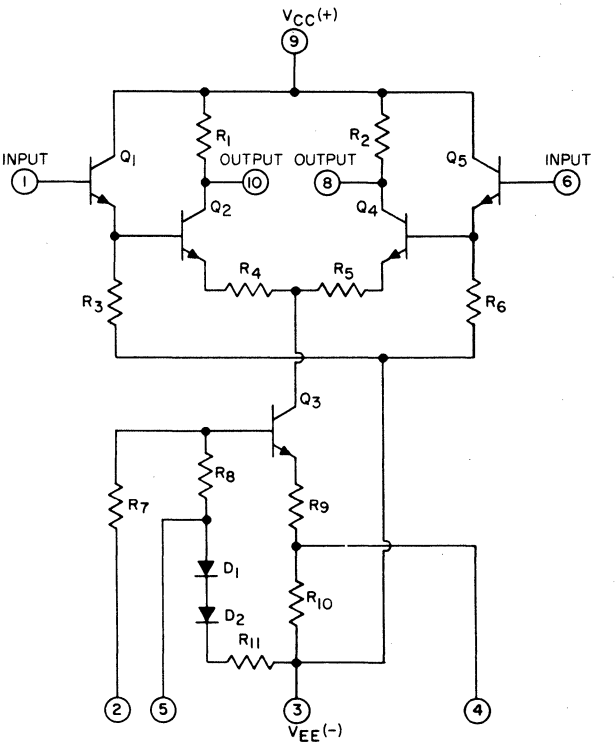


Fig. 71 — Schematic diagram of the CA3000 integrated-circuit dc amplifier.

The circuit, which is supplied in a 10-terminal TO-5 style package, is basically a single-stage differential amplifier (Q_2 and Q_4) with input emitter-followers (Q_1 and Q_5) and a constant-current sink (Q_3) in the emitter-coupled leg. Push-pull input and output capabilities are inherent in the differential configuration.

The use of degenerative resistors R_4 and R_5 in the emitter-coupled pair of transistors increases the linearity of the circuit. The low-frequency output impedance between each output (terminals 8 and 10) and ground is essentially the value of the collector resistors R_1 and R_2 in the differential stage.

Operating Requirements and Characteristics

The CA3000 is designed for operation from a wide range of supply voltages. Operation from either one or two power supplies is feasible, as illustrated by the typical biasing techniques shown in Fig. 72. However, operation from two supplies is recommended because fewer external bias networks are required and, therefore, less power is consumed.

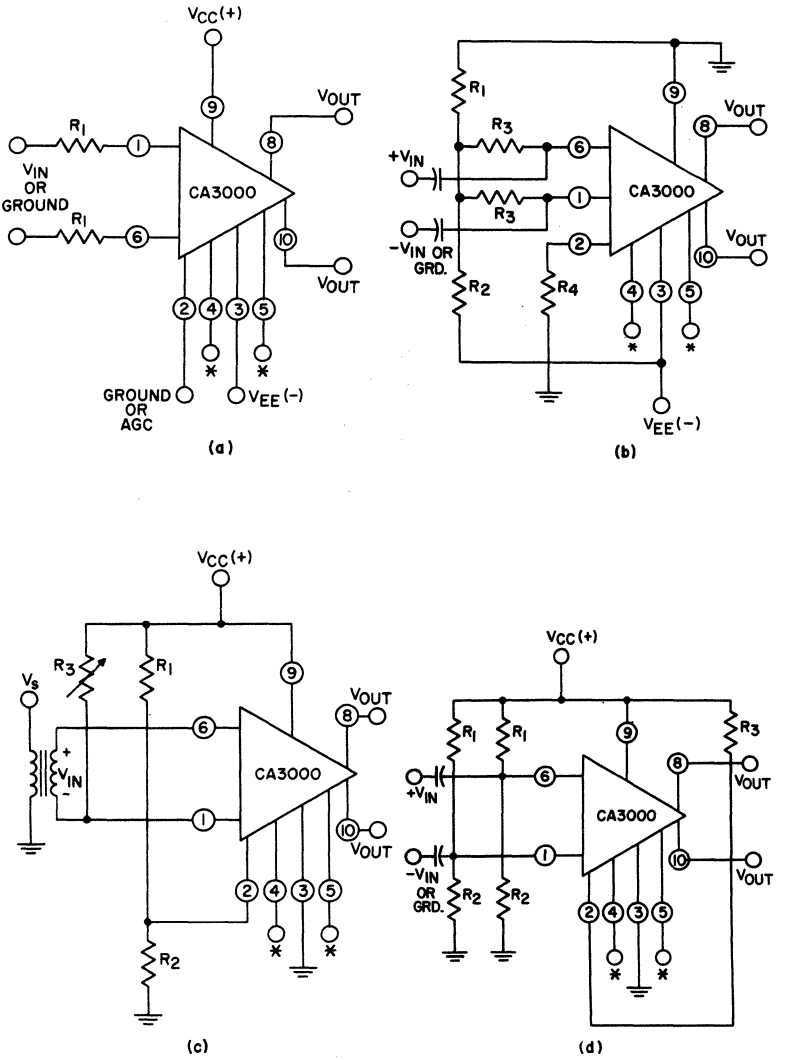
The maximum voltage that can be applied across the circuit (positive supply voltage V_{CC} plus negative supply voltage V_{EE}) is 16 volts. The maximum voltage capability (V_{CE}) of the differential pair is limited to 8 volts. Extra care must be used to ensure that these values are not exceeded when the circuit is used to drive inductive loads.

The operating-current conditions of the differential pair of transistors are determined by the base-bias circuit and emitter resistance of the emitter-coupled constant-current sink (Q_3), as well as by the voltage between terminals 2 and 3. Each possible current condition is manifested by (1) a distinct set of dc operating characteristics with differing temperature characteristics, (2) a particular value of gain having its own temperature dependence, and (3) a particular dynamic output-voltage capability. For each value of voltage between terminals 2 and 3 (V_{EE} when terminal 2 is grounded), there are four possible operating modes, as described in Table V.

Table V—*Operating Modes for CA3000 DC Amplifier*

Mode	Shorted Terminals	Condition of Diodes	Q_3 Emitter Resistor
A	none	in	$R_9 + R_{10}$
B	5-3	out	$R_9 + R_{10}$
C	4-3	in	R_9
D	5-4-3	out	R_9

The operating characteristics for these modes of operation are summarized in Table VI for various two-supply configurations with terminal 2 grounded and with V_{EE} values of −3 and −6 volts dc.



* Connection of terminals 4 and 5 depends upon mode of operation.

Fig. 72 — Typical biasing arrangements for the CA3000 for operation from (a) two separate voltage supplies, or (b), (c), and (d) a single voltage supply.

Table VI shows that the positive supply voltage can be adjusted for each mode of operation and for each value of negative supply so that the nominal dc output voltage is zero. (Although the V_{CC} value required for mode C for a V_{EE} of −6 volts dc is in excess of the maximum rating, operation within ratings can be achieved with slightly negative values of output voltage.) The use

Table VI—*Design Characteristics of CA3000 Operating Modes*

DC Supply Volts Positive V_{CC}	DC Supply Volts Negative $-V_{EE}$	Operating Mode	Single-ended Mid-Band Voltage Gain — dB G_{V_S}	DC Output Volts (Term. 8 or 10 to ground) $V_{o_{dc}}$	Positive Voltage Swing $V_{o_{max}}$*	Negative Voltage Swing $V_{o_{min}}$*	Total Power Dissipation — mW
6	−6	A	31.2	+2.3	+3.7	−3.8	40
6	−6	B	27.3	+4.3	+1.7	−5.7	36
6	−6	C	34.6	−1.5■	+7.5	0	61
6	−6	D	32.4	+1.0	+5.0	−2.4	47
3.7	−6	A	31.2	0	+3.7	−1.4	33
1.7	−6	B	27.3	0	+1.7	−1.4	25
10.6▲	−6	C	34.6	0	+10.6	−1.5	83
5.0	−6	D	32.4	0	+5.0	−1.5	43
3	−3	A	27.5	+1.2	+1.8	−2.6	8.8
3	−3	B	16.6	+2.6	+0.4	−4.1	7.4
3	−3	C	32.6	−1.5■	+4.5	0	14
3	−3	D	24.4	+1.9	+1.1	−3.3	8.5
1.8	−3	A	27.5	0	+1.8	−1.5	7.2
0.4	−3	B	16.6	0	+0.4	−1.5	8.4
5.3	−3	C	32.6	0	+5.3	−1.5	19
1.1	−3	D	24.4	0	+1.1	−2.6	6.2

* $V_{o_{max}}$ and $V_{o_{min}}$ are the ac swing extremities above and below V_{ode}.
▲ Over rating. ■ Saturated.

of these adjusted values of positive supply provides two advantages: (1) direct interstage coupling can be effected in a single-ended configuration, and (2) negative feedback can be introduced from a single output back to the appropriate input. For low-level applications in mode D with a negative supply voltage V_{EE} of −3 volts dc and a positive supply voltage V_{CC} of 1.1 volts dc, the CA3000 has a gain of 24.4 dB, a dissipation of 6.2 milliwatts, an output capability of 2.2 volts peak-to-peak, and a dc output-voltage reference level of zero.

The information in Table VI can be modified for single-supply designs by simple addition and/or subtraction of dc values. For example, the correct information for a single supply of 12 volts dc for operating mode A can be obtained from the conditions shown in the table for mode A for V_{CC} = 6 Vdc and V_{EE} = −6 Vdc by the addition of 6 volts to the values shown for V_{CC}, V_{EE}, Vo_{dc}, Vo_{max}, and Vo_{min}. (It should be noted that the required

voltage levels at the input terminals 1 and 6 and at terminal 2 are also 6 volts higher.)

As mentioned previously, the four operating modes exhibit different temperature characteristics. Fig 73 shows theoretical curves of dc output voltage as a function of temperature for each

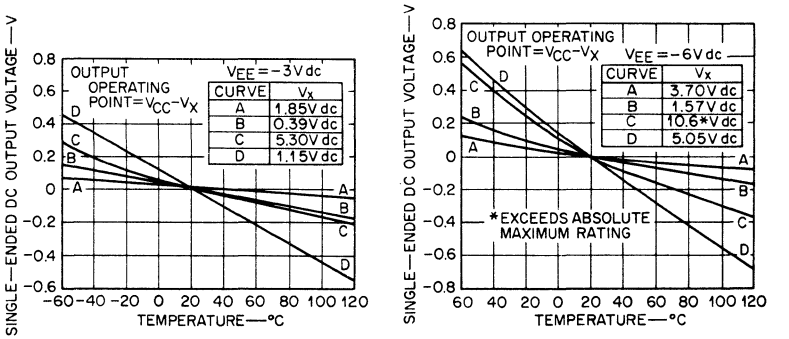


Fig. 73 — Theoretical curves of dc output voltage as a function of temperature for negative-supply voltages of −3 and −6 volts (calculated for β = 35 at 20°C).

operating mode for negative supply voltages V_{EE} of −3 and −6 volts dc. The experimental curves shown in Fig. 74 are in excellent agreement with the theoretical curves except in the case of mode C. In this mode, the differential-pair transistors Q_2 and Q_4 were driven into saturation as a result of the use of symmetrical sup-

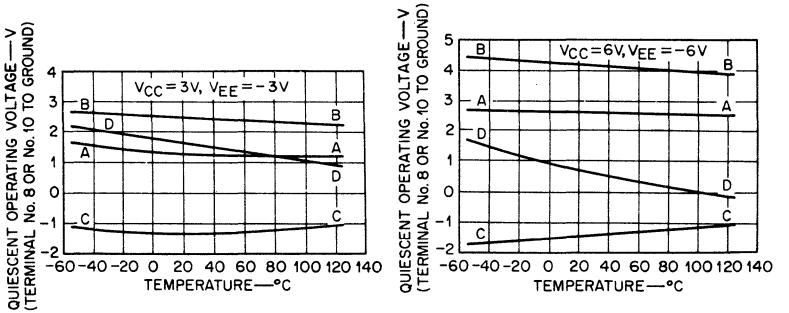


Fig. 74 — Measured curves of dc output voltage as a function of temperature for negative-supply voltages of −3 and −6 volts.

plies ($V_{CC} = V_{EE}$) for the experimental data. The discrepancy could be corrected by use of somewhat higher values of positive supply voltage.

Fig. 75 shows theoretical curves of gain as a function of temperature for the four operating modes with V_{EE} values of −3 and −6 volts dc. With the diodes in (modes A and C), the gain decreases for both values of V_{EE}. With the diodes out (modes B and D), on the other hand, the gain increases with temperature for a negative supply of −3 volts dc, but decreases with temperature

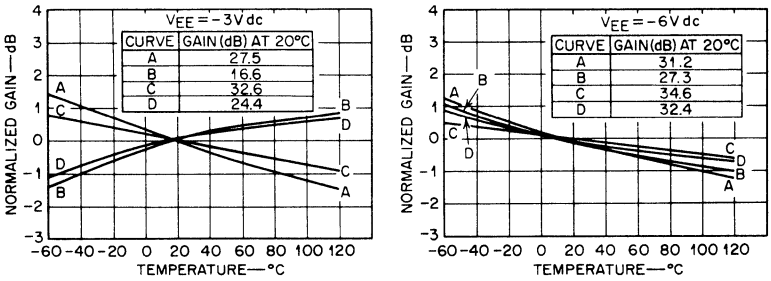


Fig. 75 — Theoretical curves of gain as a function of temperature for negative-supply voltages of −3 and −6 volts (calculated for $\beta = 35$ at 20°C).

for a negative supply of −6 volts dc. With the diodes out, there is a value of negative supply (approximately −4.5 volts dc) for which the gain is independent of temperature. Fig. 76 shows measured values of single-ended and push-pull gain for mode A with

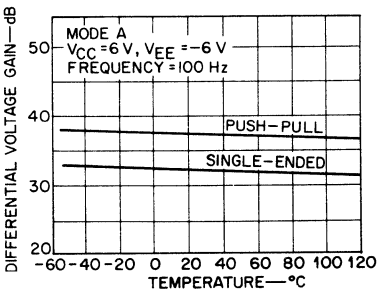


Fig. 76 — Measured values of single-ended and push-pull gain for mode A operation with symmetrical power supplies of ±6 volts.

symmetrical power supplies of ±6 volts dc. (This configuration is used in the remaining discussion because it provides the maximum sinusoidal output capability, as shown in Table VI, and because of the convenience of ±6-volt dc supplies.)

The typical single-ended voltage-gain/frequency-response curve of the CA3000 for dc supplies of ±6 volts in operating mode A is shown in Fig. 77, together with the test circuit used for voltage-gain measurements. The responses of the CA3000 are virtually independent of source impedance up to 10,000 ohms because of the emitter-follower inputs. The curves in Fig. 78 show that gain and bandwidth are virtually independent of temperature for operation in mode A with ±6-volt dc supplies.

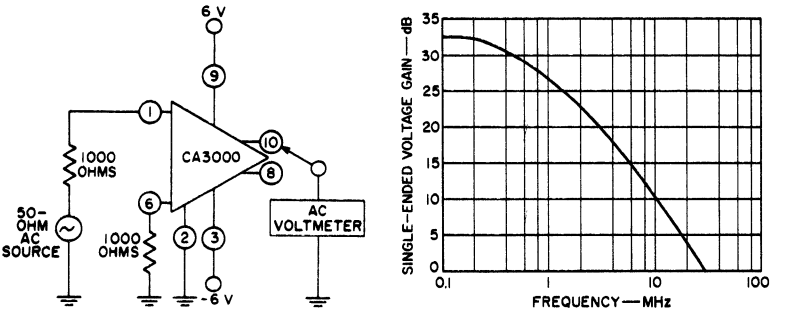


Fig. 77 — Single-ended voltage gain of the CA3000 as a function of frequency in test circuit shown.

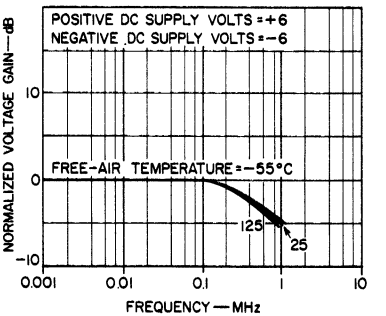


Fig. 78 — Normalized gain-frequency curves for the CA3000 at three different temperatures.

Fig. 79 shows agc characteristics for the CA3000 for an input frequency of 1 kHz, together with the agc voltage-gain test circuit. When the agc voltage at terminal 2 is varied from 0 to −6 volts, the amplifier gain can be varied over a range of 90 dB.

Fig. 80 shows the test circuit used to measure common-mode rejection, together with curves of common-mode rejection as a function of frequency and temperature. Typical rejection is 97 dB

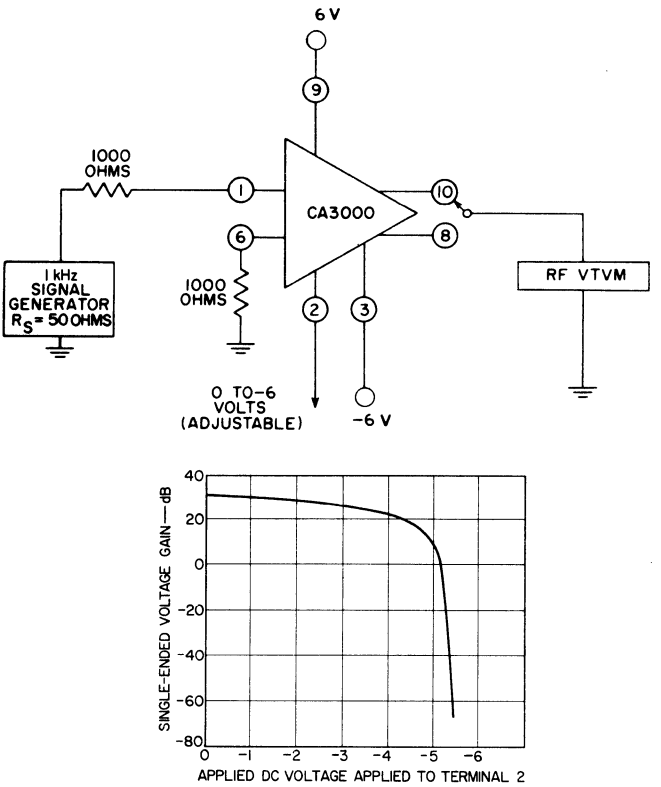
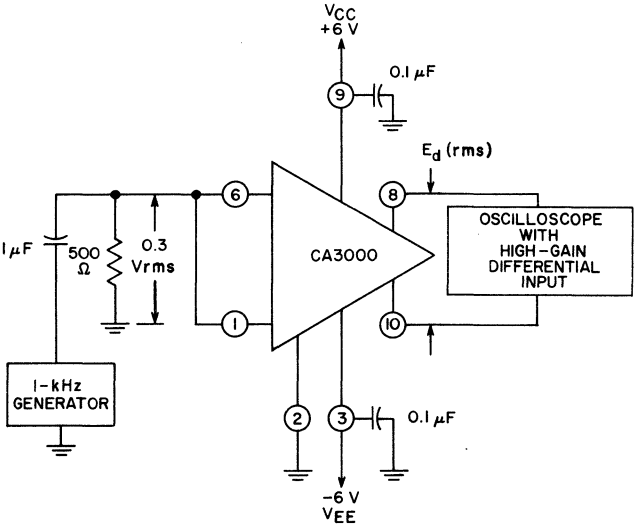


Fig. 79 — AGC characteristics of the CA3000 in test circuit shown at a frequency of 1 kHz.

at a frequency of 1 kHz. Fig. 81 shows the test circuit used to measure the dc unbalance of the amplifier (referred to the input), together with a curve of the input offset voltage as a function of temperature. Typical input offset voltage (with an assumed push-pull differential gain of 37 dB) is 1.5 millivolts. Fig. 82 shows curves of input bias current, input impedance, and dynamic output voltages as functions of temperature.

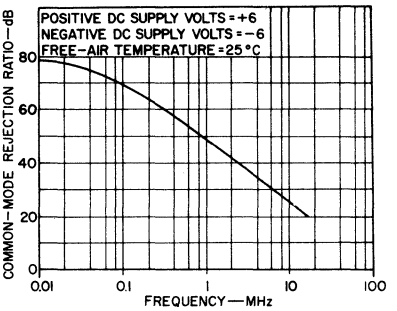
Applications of the DC Amplifier

The full gain-control capability inherent in the CA3000 makes possible the use of this circuit as a signal switch (with pedestal), a squelchable audio amplifier (with suppressed switching transient), a modulator, a mixer, or a product detector. When suitable external components are added, it can also be used as an



$$\text{COMMON-MODE REJECTION RATIO (CMR)} = 20 \log \frac{(A^*)(2)(0.3)}{E_d(\text{rms})}$$

*A = SINGLE-ENDED VOLTAGE GAIN AS MEASURED IN CIRCUIT SHOWN IN FIG. 77



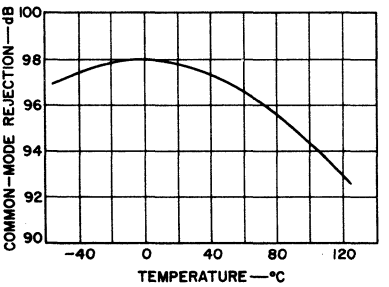


Fig. 80 — Common-mode rejection of CA3000 as a function of frequency and of temperature in test circuit shown.

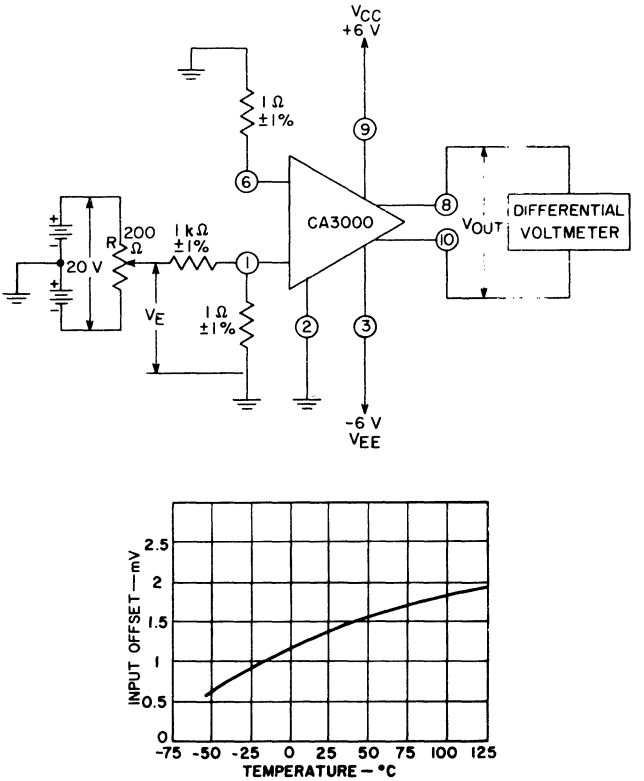


Fig. 81 — Input offset voltage of CA3000 as a function of temperature in test circuit shown.

oscillator, a one-shot multivibrator, or a trigger with controllable hysteresis. Within its specified frequency range, it is an excellent limiter, and can handle input signals up to about 80 millivolts rms before significant cross-modulation or intermodulation products are generated. Some of the applications of the CA3000 are discussed below.

Crystal Oscillator — The CA3000 can be used as a crystal oscillator at frequencies up to 1 MHz by connection of a crystal between terminals 8 and 1 and use of two external resistors, as shown in Fig. 83(a). The output is taken from the collector that is not connected to the crystal (in this case, terminal 10). If a variable-feedback ratio network is used, as shown in Fig. 83(b), the feedback may be adjusted to provide a sinusoidal oscillation. Output waveforms for both circuits are also shown. The frequency in each circuit is 455 kHz, as determined by the crystal. The range

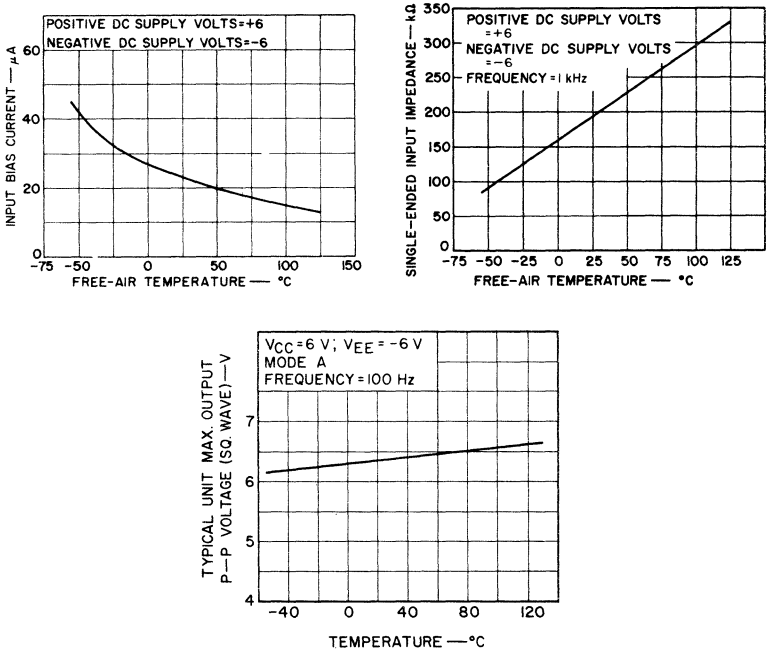


Fig. 82 — Input bias current, input impedance, and dynamic output voltage of CA3000 as functions of temperature.

of these crystal oscillators can be extended to frequencies of 10 MHz or more by use of collector tuning.

Modulated Oscillator — If a low-frequency signal is connected to terminal 2, as shown in Fig. 84, the CA3000 can function as an oscillator and produce an amplitude-modulating signal. The waveform in Fig. 84 shows the modulated signal output produced by the modulated oscillator circuit when a 1-kHz signal is introduced at terminal 2 and a high-pass filter is used at the output.

Low-Frequency Mixer — In a configuration similar to that used in modulated-oscillator applications, the CA3000 amplifier may be used as a mixer by connection of a carrier signal at the base input of either differential-pair transistor (terminal 1 or 6) and connection of a modulating signal to terminal 2 or 5.

Cascaded RC-Coupled Feedback Amplifier — The two-stage feedback cascade amplifier shown in Fig. 85 produces a typical open-loop mid-band gain of 63 dB. This circuit uses a 100-picofarad capacitor C_1 to shunt the differential outputs of the first stage. This capacitor staggers the high-frequency roll-offs of the amplifier and thus improves stability.

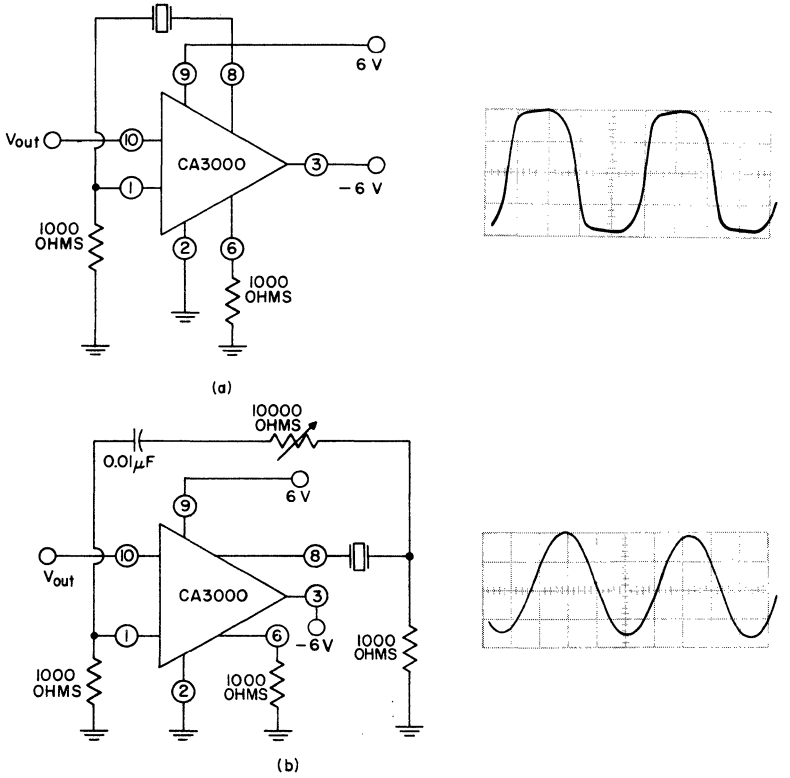


Fig. 83 — Schematic diagrams and output waveforms of (a) crystal oscillator and (b) crystal oscillator with variable feedback.

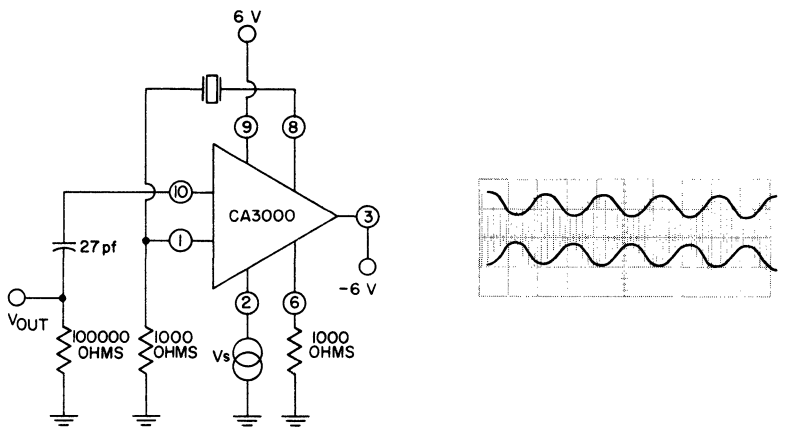
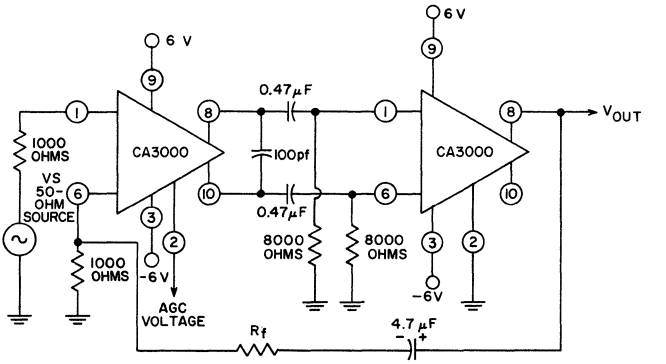


Fig. 84 — Schematic diagram and output waveform of CA3000 modulated oscillator.



R_f	G_V
∞	63 db (OPEN LOOP)
100000 OHMS	40 db
9000 OHMS	20 db

Fig. 85 — Cascaded RC-coupled feedback amplifier using two CA3000 circuits.

The gain-frequency characteristic of the feedback amplifier is shown in Fig. 86(a) for a feedback resistance R_f approaching infinity. The low-end roll-off of the amplifier is determined by the interstage coupling. Because agc may be applied to the first stage, the amplifier of Fig. 85 may be used in high-gain video-agc applications under open-loop conditions. If feedback is used to control the gain, agc may still be applied successfully.

Fig. 86(b) shows the agc characteristics for the two-stage amplifier under open-loop and two closed-loop conditions at a

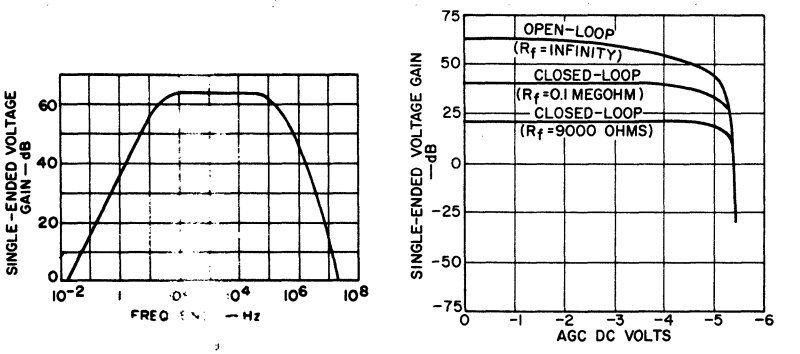


Fig. 86 — Ga… …uency (a) and agc (b) characteristics of feedback amplifier shown in Fig. 85.

frequency of 1 kHz. As shown in Fig. 86(a), the open-loop bandpass is 18 Hz to 135 kHz; under closed-loop conditions, the bandpass is 1.3 Hz to 2 MHz for 40-dB gain and 0.13 Hz to 6.6 MHz for 20-dB gain. The negative feedback thus improves low-frequency performance sufficiently so that the use of the small coupling capacitors C_2 and C_3 involves little sacrifice in low-frequency response. If three or more CA3000 amplifiers are cascaded, the low-frequency roll-offs must be staggered as well as those at the high end to prevent oscillation. A three-stage cascade has a midband gain of approximately 94 dB.

Narrow-Band Tuned Amplifier — Because of its high input and output impedances, the CA3000 is suitable for use in parallel tuned-input and tuned-output applications. There is comparative freedom in selection of circuit Q because the differential amplifier exhibits inherently low feedback qualities provided the following conditions are met: (1) the collector of the driven transistor is returned to ac ground and the output is taken from the non-driven side, and (2) the input is adequately shielded from the output by a ground plane.

The CA3000 has an output capacitance of approximately 9 picofarads at a frequency of 10 MHz. This capacitance will resonate a 28-microhenry coil at this frequency and give a minimum Q of 4.55 when the collector load resistor is the only significant load. With this low Q, stagger tuning may be unnecessary for many broad-band applications.

Fig. 87 shows the CA3000 in a narrow-band, tuned-input, tuned-output configuration for operation at 10 MHz with an input Q of 26 and an output Q of 25; the response curve of the amplifier is also shown. The 10-MHz voltage gain is 29.6 dB, and the total effective circuit Q is 37. There is very little feedback skew in the response curve. The CA3000 can be used in tuned-amplifier applications at frequencies up to the 30-MHz range.

Schmitt Trigger — The CA3000 can be operated as an accurate, predictable Schmitt trigger provided saturation of either side of the differential amplifier is prevented (hysteresis is less predictable if saturation occurs). Non-saturating operation is accomplished by operation in mode B (terminals 3 and 5 shorted together) in the configuration shown in Fig. 88. Large values are required for external resistors R_1 and R_2 because they receive the total collector current from terminal 10. Because of the high impedances, resistor R_2 is actually a parallel combination of the input impedance (approximately 0.1 megohm) of the CA3000 and the 0.25-megohm external resistor. The Schmitt-trigger design

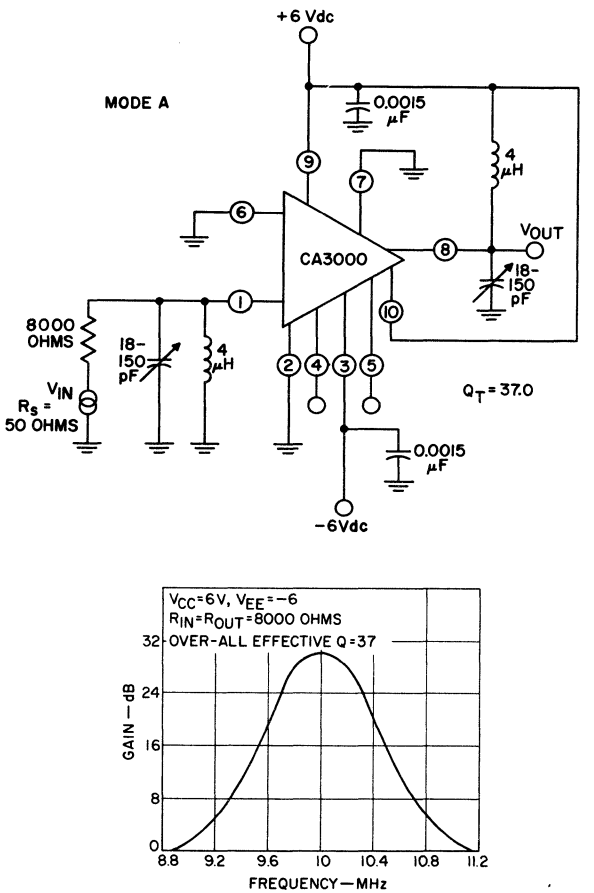


Fig. 87 — Schematic diagram and response curves for 10-MHz tuned-input, tuned-output narrow-band amplifier using CA3000.

equations (for $\alpha = 1$) are summarized below. In these equations, Q_2 and Q_4 are the differential-pair transistors, Q_1 and Q_5 are the emitter-follower transistors, and Q_3 is the constant-current sink.

State I: Q_2 off, Q_4 conducting (not saturated)

$$V_{6I} = \frac{V_{CC}\,(R_2) - V_{EE}\,(R_1 + 8000)}{R_1 + R_2 + 8000}$$

where 8000 ohms is the output impedance of Q_4 (obtained from the published data). For $R_1 = 27000$ ohms and $V_{CC} = V_{EE} = 6$ Vdc,

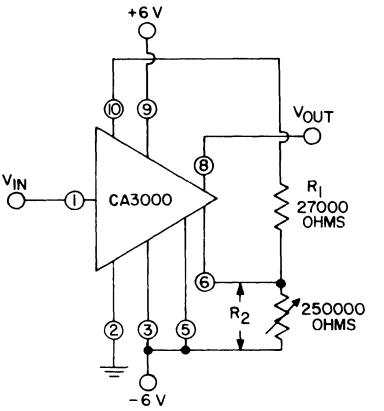


Fig. 88 — Schematic diagram of Schmitt trigger using CA3000.

$$V_{6I} = \frac{6V\ (R_2) - 6V\ (35000)}{R_2 + 35000} \qquad (A)$$

$$R_2 = (R_1 + 8000)\ \frac{V_{EE} + V_{6I}}{V_{CC} - V_{6I}}$$

$$R_2 = (35000)\ \frac{6V + V_{6I}}{6V - V_{6I}} \qquad (B)$$

$$V_{8I} = V_{CC} - I_E\ (8000)$$

where I_E = collector current of transistor Q_3 ($I_E \approx 0.48$ milliampere in operating mode B with $V_{EE} = -6$ volts dc.)

$$V_{8I} = 2.14\ V \qquad (C)$$

V_{FI} ≡ Firing voltage for transition from state I to state II

$$V_{FI} = V_{6I} - 0.053 - 100\ I_E \text{ at } 25°C$$

$$V_{FI} = V_{6I} - 0.101\ V \text{ at } 25°C \qquad (D)$$

State II: Q_2 conducting (not saturated), Q_4 off

$$V_{8II} = V_{CC}$$

$$V_{8II} = 6\ V \qquad (A)$$

$$V_{6II} = \frac{(V_{CC} - I_E\ 8000)\ R_2 - V_{EE}\ (R_1 + 8000)}{R_1 + R_2 + 8000}$$

$$V_{6II} = \frac{2.14\ V\ (R_2) - 6\ V\ (35000)}{R_2 + 35000} \qquad (B)$$

$V_{FII} \equiv$ Firing voltage for transition from state II back to state I

$V_{FII} = V_{6II} + 0.053 + 100\ I_E$ at 25°C

$V_{FII} = V_{6II} + 0.101$ V at 25°C (C)

Hysteresis Voltage

$$V_{HYS} = V_{FI} - V_{FII}$$

$$= \frac{3.86\ V\ (R_2)}{R_2 + 35000} = 0.202\ V \text{ at } 25°C$$

From the calculations for state I, it is evident that either V_{6I} or R_2 must be a known design value. Because R_2 is a composite value, V_{6I} is the more reasonable choice. The ability of these equations to predict the Schmitt-trigger performance is evidenced by the comparison of calculated and experimental data in Table VII.

Table VII—*Comparison of Calculated and Experimental Data for Schmitt Trigger*

Condition	Parameter	Calculated	Experimental
1) $V_{6I} = -2$ V	V_{FI}	−2.1 V	−2.2 V
	V_{FII}	−3.19 V	−3.2 V
	V_{HYS}	+1.09 V	+1.0 V
2) $V_{6I} = -1$ V	V_{FI}	−1.10 V	−1.0 V
	V_{FII}	−2.51 V	−2.45 V
	V_{HYS}	+1.41 V	+1.4 V
3) $V_{6I} = 0$	V_{FI}	−0.101 V	0
	V_{FII}	−1.83 V	−1.8 V
	V_{HYS}	+1.73 V	+1.8 V
4) $V_{6I} = +1$ V	V_{FI}	+0.9 V	+1.0 V
	V_{FII}	−1.15 V	−1.0 V
	V_{HYS}	+2.1 V	+2.0 V
5) $V_{6I} = +2$ V	V_{FI}	+1.9 V	+2.0 V
	V_{FII}	−0.472 V	−0.5 V
	V_{HYS}	+2.43 V	+2.4 V

AUDIO AMPLIFIER

The CA3007 integrated-circuit audio driver, shown in Fig. 89, is a balanced differential configuration with either a single-ended or a differential input and two push-pull emitter-follower outputs. The circuit, which is intended for use as a direct-coupled driver in a class B audio amplifier, exhibits both gain and operating-

point stability over the temperature range from −55 to 125°C. The CA3007 is an excellent controlled-gain audio driver for systems requiring audio squelching. The audio-driver circuit is available in a 12-terminal TO-5 style for low-silhouette package.

The input stage of the CA3007 consists of a differential pair of transistors (Q_1 and Q_2) operating as a phase splitter with gain.

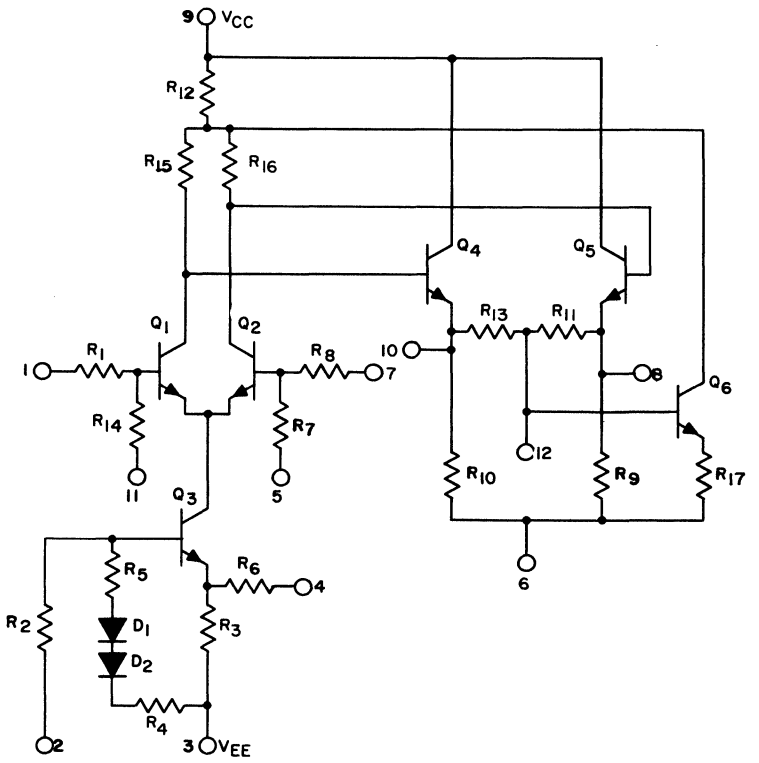


Fig. 89 — Schematic diagram of CA3007 integrated-circuit audio driver.

The two output signals from the phase splitter, which are 180 degrees out of phase, are direct-coupled through two emitter-followers (Q_4 and Q_5). The emitters of the differential pair of transistors are connected to the transistor constant-current sink Q_3.

The diodes in the bias circuit of the transistor constant-current sink make the emitter current of Q_3 essentially dependent on the temperature coefficient of the diffused emitter resistor R_3. Because the diffused collector resistors R_{15} and R_{16} should have

identical temperature coefficients, constant collector-voltage operating points should result at the collectors of transistors Q_1 and Q_2. However, the quiescent operating voltages at the output terminals 8 and 10 increase as temperature increases because the base-emitter voltage drops of transistors Q_4 and Q_5 decrease as temperature increases. This small variation in the output quiescent operating voltage is sufficient to cause a large variation in the standby current of a class B push-pull output stage when the audio driver and the output stage are direct-coupled. Resistors R_{11}, R_{12}, R_{13}, and R_{17} and transistor Q_6 form a dc feedback loop which stabilizes the quiescent operating voltage at output terminals 8 and 10 for both temperature and power-supply variations so that variations in the output operating points are negligible.

Resistors R_1, R_7, R_8, and R_{14} form the input circuit; a double-ended input is applied to terminals 1 and 5, and a single-ended input is applied to either terminal 1 or terminal 5, with the other terminal returned to ground. The CA3007 must be ac-coupled to the input source. In addition, any dc resistance between terminal 1 and ground should be added between terminal 5 and ground. Output power-gain stabilization for a direct-coupled driver and output stage is accomplished by means of an ac feedback loop that connects terminals 7 and 11 to the proper emitters of the push-pull output stage, as shown in Fig. 90.

Connection of voltage supplies to the CA3007 audio driver requires that the most positive voltage be connected to terminal 9 and the most negative voltage to terminal 3 (internally connected to the substrate and the case). The CA3007 may be operated from various supplies and at various levels. Operation from either a single supply (as shown in Fig. 91) or from dual power supplies (as shown in Fig. 90) is feasible. For dual-supply operation, symmetrical supplies must be used if the audio driver is to be direct-coupled to the audio output stage. For single-supply operation, the audio driver must be ac-coupled to the audio output stage, and the number of external components required increases.

For operation from either single or dual supplies, the operating current in transistor Q_3 is determined by the bias voltage between terminals 2 and 3. The more negative terminal of this bias voltage must be connected to terminal 3. For dual-supply systems, terminal 2 is either grounded or connected to a trigger circuit for audio-squelching purposes.

Fig. 90 shows the CA3007 used as a dual-supply audio driver in a direct-coupled audio amplifier. This amplifier provides a power output of 300 milliwatts for an audio input of 0.3 volt rms (V_{CC}

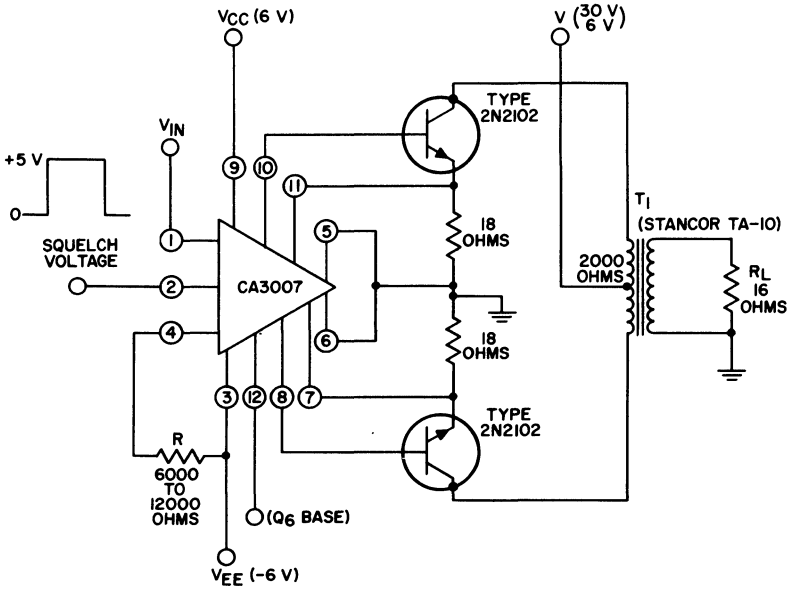


Fig. 90 — CA3007 used as an audio driver for a direct-coupled 300-milliwatt audio amplifier.

= 6 volts, V_{EE} = −6 volts, V = 30 volts). For a voltage V of 6 volts, the output power is 10 milliwatts without transformer optimization; the use of a lower-impedance transformer would permit power outputs in the order of 100 milliwatts.

The external resistor R connected between terminals 3 and 4 is used to set the class B output-stage standby current as required for a particular application. If the standby current is too low, crossover distortion will result; if it is too high, standby power drain will be excessive. Decreasing the value of resistor R reduces the standby current; for a standby current of 10 milliamperes, R is typically 10,000 ohms.

Terminal 2 must be grounded or, if an audio squelch is desired, must be connected to a positive voltage supply of 5 volts minimum. When terminal 2 is near ground, the audio amplifier functions normally. When terminal 2 is at 5 volts, the differential pair of the audio driver saturates, and the push-pull output stage is cut off. The squelch source must be capable of supplying a current of 1.5 milliamperes in the 5-volt condition, and 0.75 milliampere in the near-ground condition.

For a symmetrical audio driver, there is no ac signal present at the base of transistor Q_6. However, unbalances between the two

halves of the circuit may require that the base of Q_6 be bypassed for proper operation. The base of Q_6 may be bypassed by connection of an external capacitor (typically 50 microfarads, 6 volts) from terminal 12 to ground. Bypassing is usually not required unless high undistorted power outputs are required over the complete temperature range of −55 to 125°C.

Table VIII shows values of harmonic distortion and intermodulation distortion for the amplifier of Fig. 90.

Table VIII—*Distortion Measurements for Direct-Coupled Amplifier Shown in Fig. 90*

Harmonic Distortion

Power Output (mW)	Output-Signal Level (mV rms) with 2-KHz Input Signal						Harmonic Distortion (%)
	2 kHz	4 kHz	6 kHz	8 kHz	10 kHz	12 kHz	
62.5	1000	9	3.0	—	—	—	0.95
140	1500	18	4.0	2.0	1.4	1.0	1.24
250	2000	25	4.2	5.0	1.0	1.5	1.30
330	2300	27	6.0	9.0	3.0	2.0	1.27

Intermodulation Distortion

Output-Signal Level:	
at f_1 (2 kHz)	1000 mV rms
at f_2 (3 kHz)	1000 mV rms
at $2f_2$-f_1 (4 kHz)	0.7 mV rms
3rd-Order IMD	0.07 %

Fig. 91 shows the CA3007 used as a single-supply audio driver in a capacitor-coupled audio amplifier. This amplifier provides a power output of 30 milliwatts for an audio input of 6.5 millivolts rms (V_{CC} = 9 volts) with the transformer shown.

The connection shown in Fig. 91 still represents a differential-pair phase splitter fed from a constant-current transistor. The two output signals from the phase splitter are direct-coupled through two emitter-followers which are capacitor-coupled to the push-pull output stage. Because of the ac coupling, there is no longer a dc dependence between the driver and the output stage, and any desired audio output design or drive source may be used. As a single stage, the CA3007 audio driver provides a voltage gain of 24 dB for a dc power dissipation of 20 milliwatts with the harmonic distortion reaching 3 per cent for outputs of 0.6 volt rms at terminals 8 and 10 (without feedback).

Both dc and ac feedback loops are eliminated in the circuit of Fig. 91. Although the dc feedback loop is no longer required because of the ac coupling, removal of the ac feedback loop causes the output power gain to decrease about 1 dB for a 50°C rise in temperature.

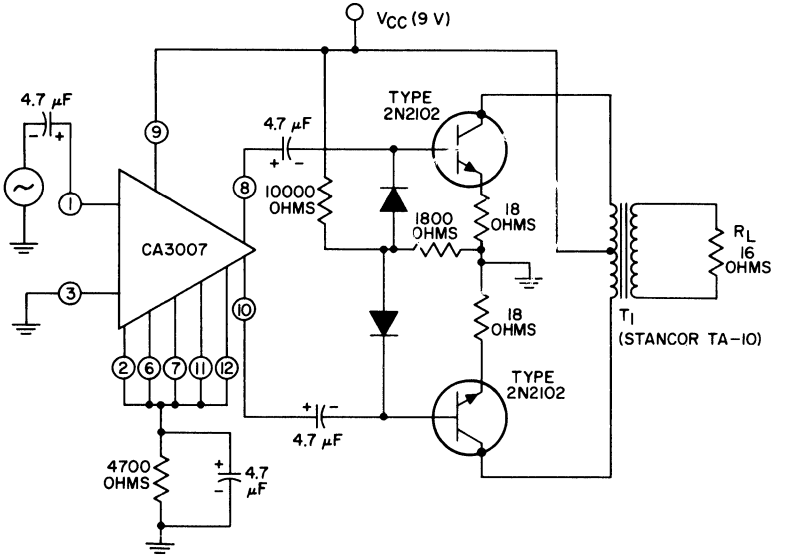


Fig. 91 — CA3007 used as an audio driver for a 30-milliwatt audio amplifier.

VIDEO AMPLIFIER

The CA3001 integrated circuit, shown in Fig. 92, is designed for use in intermediate-frequency or video amplifiers at frequencies up to 20 MHz and in Schmitt-trigger applications. This integrated circuit can be gated, and gain control can be applied. The CA3001 is available in a 12-terminal TO-5 style low-silhouette package.

The circuit consists of a differential pair of transistors, Q_3 and Q_4, the current of which is controlled by a constant-current transistor Q_7. Transistors Q_1, Q_2, Q_5, and Q_6 are operated in the common-collector configuration to provide a high-impedance input and low-impedance output. Thus, the CA3001 provides double-ended input and output, and can be iteratively connected with low-value coupling capacitors. The high-frequency response of the circuit is determined primarily by the resistance and capacitance in the collectors of the differential pair Q_3 and Q_4.

Biasing Requirements and Operating Modes

When voltage supplies are connected to the CA3001, the most positive voltage must be connected to terminal 9 and the most negative voltage to terminal 3 (internally connected to the substrate and the case). For typical operation, terminals 2 and 10 are returned to ground. If desired, however, automatic gain con-

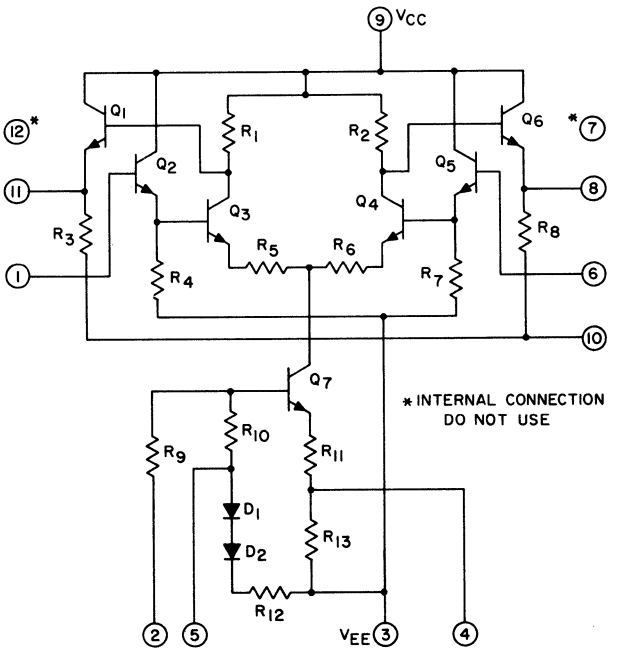


Fig. 92 — Schematic diagram of CA3001 integrated-circuit video amplifier.

trol can be applied to terminal 2, and terminal 10 can be connected to the negative supply to permit larger negative-going output swings in the output transistors.

The CA3001 may be operated with various supplies and at various levels. Operation from either a single supply or dual supplies is feasible, as shown in Fig. 93. When dual supplies are used, they may be either symmetrical or non-symmetrical. The use of separate positive and negative supplies minimizes the need for external components, as shown in Fig. 93(a). For single-supply applications, a resistor divider and a bypass capacitor must be added, as shown in Fig. 93(b).

When dual supplies are used, the inputs (terminals 1 and 6) are returned to ground through equal external resistors (the maximum recommended value of R is 3300 ohms for linear operation).

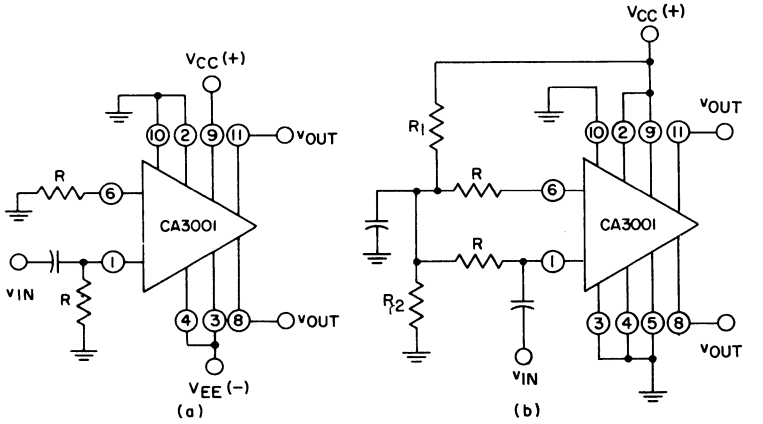


Fig. 93 — Circuit connections for the CA3001 for (a) separate positive and negative supplies and (b) a single supply.

The current through the resistor divider R_1 and R_2 should be greater than 1.5 milliamperes. For either single or dual supplies, the operating current in transistor Q_7 is determined by the operating mode. For any given bias voltage, four operating modes are possible, as described in Table IX. Each mode is characterized by a distinct operating current and a corresponding voltage gain, both of which have a particular temperature dependence.

Table IX—*Four Possible Operating Modes for CA3001 Amplifier*

Operating Mode	Shorted Terminals	Condition of Diodes	Q_7 Emitter Resistor
A	none	in	$R_{11} + R_{13}$
B	5-3	out	$R_{11} + R_{13}$
C	4-3	in	R_{11}
D	5-4-3	out	R_{11}

Table X shows typical design performance characteristics for the four operating modes of the CA3001 at room temperature. The output operating point and voltage gain of the circuit are reasonably independent of resistor value, but the current and power dissipation may vary with resistor values. Figs. 94 and 95 show theoretical curves of output operating point and voltage gain, respectively, as functions of temperature for nominal resistor values with supply voltage V_{EE} of −3 and −6 volts dc. The voltage between terminals 8 and 9 or terminals 11 and 9 is denoted by V_X. Because the variation of voltage gain and operating point with

temperature is small for all operating modes, the choice of mode depends on application requirements. With a supply voltage V_{EE} of −4.5 volts, voltage-gain variation is normally less than 0.5 dB for all operating modes over the temperature range of −55 to 125°C.

Table X—*Typical Design Performance Characteristics for the CA3001 Amplifier (terminals 2, 10, 6, and 1 referenced to ground) at 25°C*

Operating Mode	Supplies (±V)	Output Operating Volts (Term. 8 and 11 to ground)	Positive Supply Current (mA)	Negative Supply Current (mA)	Power Dissipation (mW)	Single-Ended Voltage Gain at 1 MHz (dB)
A	6	4.3	8.4	−4.7	79	15.5
B	6	4.8	7.8	−3.9	70	12.7
C	6	2.8	9.9	−7.9	106	17.8
D	6	4.1	8.7	−5.5	85	16.4
A	4.5	3.0	6.0	−3.4	43.6	14.6
B	4.5	3.4	5.6	−2.7	37.6	10.0
C	4.5	2.0	7.2	−5.8	58.4	17.7
D	4.5	2.9	6.0	−3.7	43.6	15.5
A	3	1.8	3.7	−3.9	22.6	13.0
B	3	2.1	3.3	−1.4	14.3	3.8
C	3	1.0	4.4	−3.7	25.5	16.4
D	3	2.0	2.4	−1.9	13.0	10.8

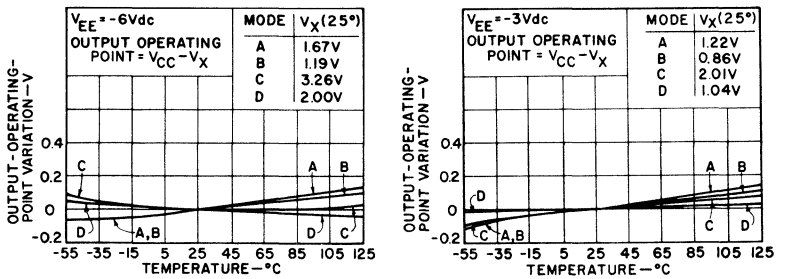


Fig. 94 — Output operating point of the CA3001 (normalized to the 25°C operating point) as a function of temperature for V_{EE} supplies of −3 and −6 volts.

Frequency Response

When the CA3001 video amplifier is used in cascade, its high-frequency response is determined primarily by the RC roll-off at the collectors of the differential pair Q_3 and Q_4. The generator source resistance may affect high-frequency bandwidth; for

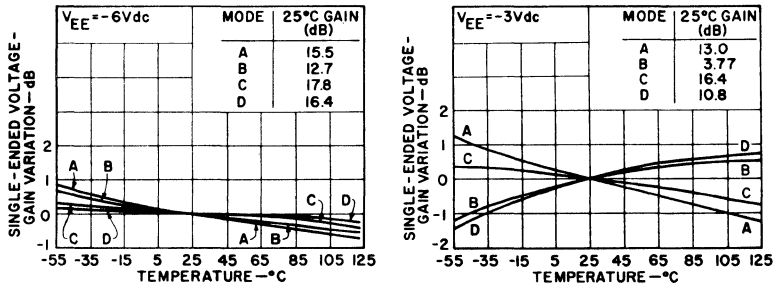


Fig. 95 — Voltage gain of the CA3001 (normalized to the 25°C gain) as a function of temperature for V_{EE} supplies of —3 and —6 volts.

full bandwidth capability, the parallel combination of source resistance and base-bias resistance should not exceed 800 ohms. The low-frequency response is determined by the coupling capacitor and the base-bias resistance value.

Fig. 96 shows the circuit used for evaluation of frequency response of the CA3001, together with the response characteristics obtained. The circuit is operated in mode C with supplies of ±6 volts. The 50-ohm generator simulates the frequency and gain behavior for iterative operation. The curves of Fig. 96 show the measured response characteristics.

The high-frequency roll-off of the CA3001 is a function of the values of resistors R_1 and R_2 in Fig. 92 and their variation with temperature. Fig. 97 shows the effect of temperature on high-fre-

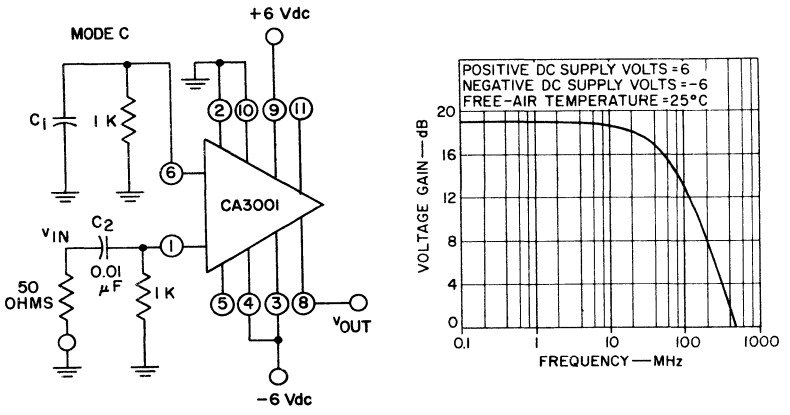


Fig. 96 — Frequency response of the CA3001 in the test circuit shown.

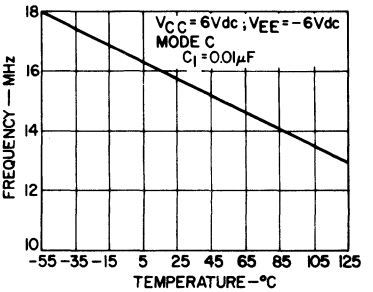


Fig. 97 — High-frequency 3-dB bandwidth of the CA3001 as a function of temperature.

quency response. The variation in response can be accounted for by the resistance variation with temperature; capacitance variations with temperature are a secondary effect.

Input and Output Impedances

Fig. 98 shows the parallel input resistance and capacitance of the CA3001 as a function of frequency. The input capacitance is constant until it begins to decrease at high frequencies. The input resistance decreases through the frequency range from 0.1 to 10

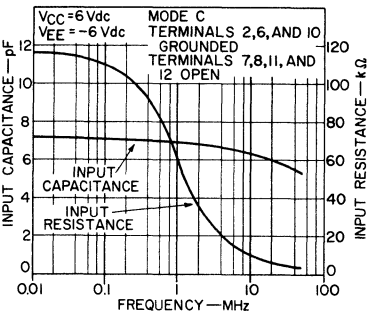


Fig. 98 — Parallel input resistance and capacitance of the CA3001 as functions of frequency.

MHz. Because the input resistance is high in comparison with the external base-bias resistors used (3300 ohms maximum), the high-frequency response characteristic of the input is determined by the driving-source resistance, the base-bias resistors, and the parallel input capacitance.

The parallel output resistance of the CA3001 is low (approximately 70 ohms), and the output reactance is sufficiently high to

provide little or no degradation of frequency response through the usable frequency range.

Noise Figure

Fig. 99(a) shows noise figure as a function of frequency for a 1000-ohm source. The 1/f noise corner occurs at approximately 30 kHz; above this frequency, the noise figure remains flat at approximately 5 dB to 6 MHz, and then begins to rise.

Fig. 99(b) shows noise figure as a function of source resistance for frequencies of 1.75 and 12 MHz. For stages in which noise performance is important, the source resistance should not be less than 500 ohms because of the rapid rise in noise figure at

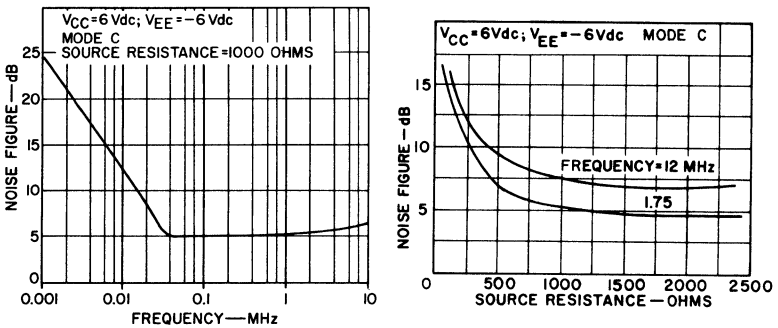


Fig. 99 — Noise figure of the CA3001 as a function of frequency and source resistance.

lower values. The noise figure of the CA3001 increases when non-driven base-bias resistors are unbypassed. For stages in which noise performance is important, the external resistor on an input base that is not receiving the signal must be bypassed if minimum noise figure is to be achieved.

Gain Control

AGC can be applied to the CA3001 at terminal 2 for any of the four operating modes. Fig. 100 shows representative agc characteristics for modes C and D at a frequency of 1 MHz. The threshold voltage is higher in mode C than in mode D because of the difference in the base-bias circuit for the constant-current sink transistor (Q_4).

The agc range is dependent on frequency at high frequencies because the feedthrough parameters are primarily capacitive;

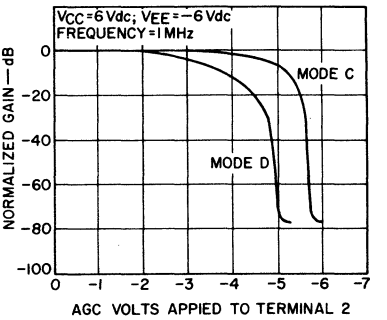


Fig. 100 — AGC characteristics of the CA3001 in modes C and D at 1 MHz.

therefore, it should eventually decrease at a rate of approximately 20 dB per decade. The average measured agc range at 10 MHz is 62 dB, and is 15 dB less than that at 1 MHz.

Common-Mode Rejection

Fig. 101(a) shows the common-mode rejection of the CA3001 as a function of temperature at a frequency of 1 kHz. The common-mode rejection increases with increasing temperature; a typical value at 25°C is 70 dB.

Because the CA3001 can be used in many applications with a single-ended output at high frequencies, both the single-ended differential gain and the single-ended common-mode gain are of considerable interest. Fig. 101(b) shows both single-ended common-mode and differential-mode gain as functions of frequency. The common-mode gain is a function of the impedance ratio between the constant-current transistor (Q_7) and the load resistor in one side of the differential pair (Q_3 or Q_4). The common-mode gain increases with increasing frequency.

The common-mode rejection is degraded if sufficient signal is applied to saturate the constant-current transistor (Q_7). The maximum peak-to-peak input voltage without degradation of common-mode rejection is a function of the voltage supplies and the operating mode of the constant-current transistor.

Harmonic Distortion and Swing Capability

When equal positive and negative supplies are used, operating mode C provides the largest swing capability because the output operating point is approximately centered. With voltage supplies of ±6 volts dc at a frequency of 1 MHz, the single-ended

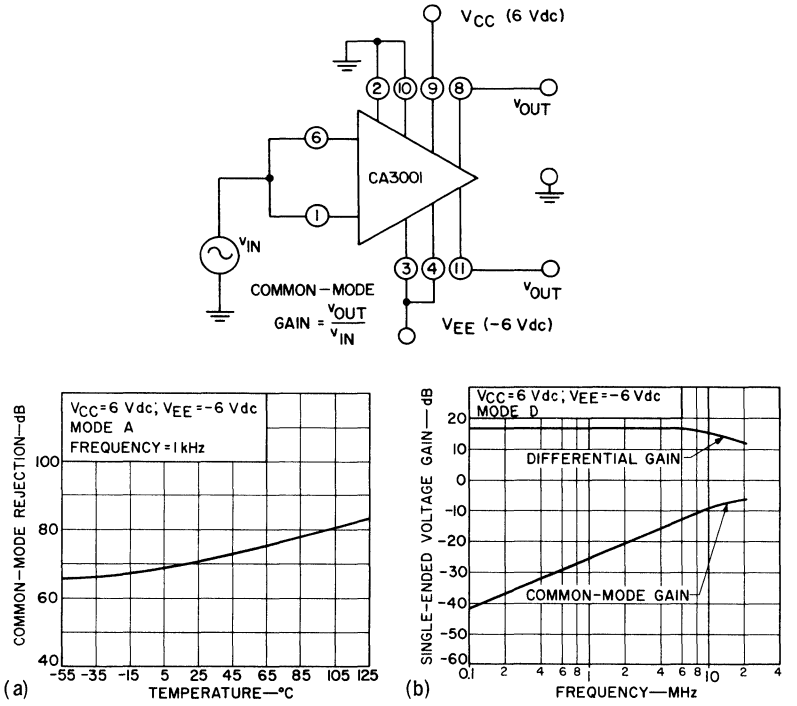


Fig. 101 — Common-mode rejection and voltage-gain characteristics of the CA3001 as a function of temperature and frequency.

output is 1.3 volts rms for 3-per-cent distortion in mode C and 0.665 volt rms in mode D.

The signal-swing capability was also evaluated as a function of temperature in mode C with voltage supplies of ±6 volts dc. For 3-per-cent distortion, an output swing of 1.2 volts rms can be obtained over the temperature range from 25 to 125°C.

For pulse-type signals, the total possible swing capability is important. The voltage at the collectors of the differential pair may rise to the positive supply voltage, V_{CC}, and fall to the saturation level. If the bases of the input emitter-followers are maintained at zero potential, the emitters of the differential pair are negative by twice the base-to-emitter voltage drop, V_{BE}, or approximately −1.4 volts. If the saturation voltage is assumed to be 0.2 volt, the collectors drop to about −1.2 volts before saturation. Therefore, the total swing available at the collectors is approximately V_{CC} + 1.2 volts; for a V_{CC} of 6 volts, the swing is 7.2 volts. The output voltage swing is lower than this value by V_{BE}, or from 5.3 to −2.0 volts. This total swing capability can be realized only when the

resistors R_3 and R_8 (terminal 10) are returned to the negative supply voltage (terminal 10 shorted to terminal 3). Selection of the operating point to obtain most of the available total swing in one direction involves proper choice of the operating mode and the negative supply voltage.

Cascade Operation

Over-all performance characteristics for three CA3001 stages operated in cascade are shown in Fig. 102. The need for supply decoupling is minimized by the symmetry of the circuit, which ensures equal and out-of-phase currents in the supply leads. Three circuits in close proximity can provide stable over-all gains of approximately 65 dB. A further advantage of the CA3001 in cascade is that a gain increase of 6 dB accrues each time a double-ended output is used.

Table XI and Fig. 102 show the performance of the CA3001 in the three-stage cascade circuit for various values of supplies and coupling capacitors. The only advantage of ±6-volt supplies as compared to ±4.5-volt supplies is a larger output-swing capability.

Table XI—*Performance of CA3001 Cascade Amplifier shown in Fig. 102*

Coupling Capacitor	0.02 μF		100 pF		
Voltage Supplies	±6	±4.5	±6	±4.5	Vdc
Power Dissipation	276	146	276	146	mW
Single-Ended-Output Mid-Band Gain	64.5	63	60.5	57.5	dB
3-dB Response: Upper	9	9	10.5	10.5	MHz
Lower	0.0125	0.0125	1.9	1.9	MHz
AGC Range	65	63	61	59	dB
Output Signal for 3-per-cent Distortion	1.3	1.15	1.15	0.7	Vrms
Input Signal for 3-dB Signal-to-Noise Ratio	26	14	20	18.5	μVrms

The use of ±4.5-volt supplies entails no sacrifice in bandwidth and little gain loss, and provides a saving in power dissipation of almost 2 to 1. Better signal-to-noise performance can be achieved with no change in bandwidth if a higher value of source resistor is used (e.g., 800 ohms, rather than the value of 50 ohms shown in Fig. 102). The agc range of the cascaded circuit is 10 dB less than that for an individual circuit because no interstage shielding is provided and double-ended output is not used.

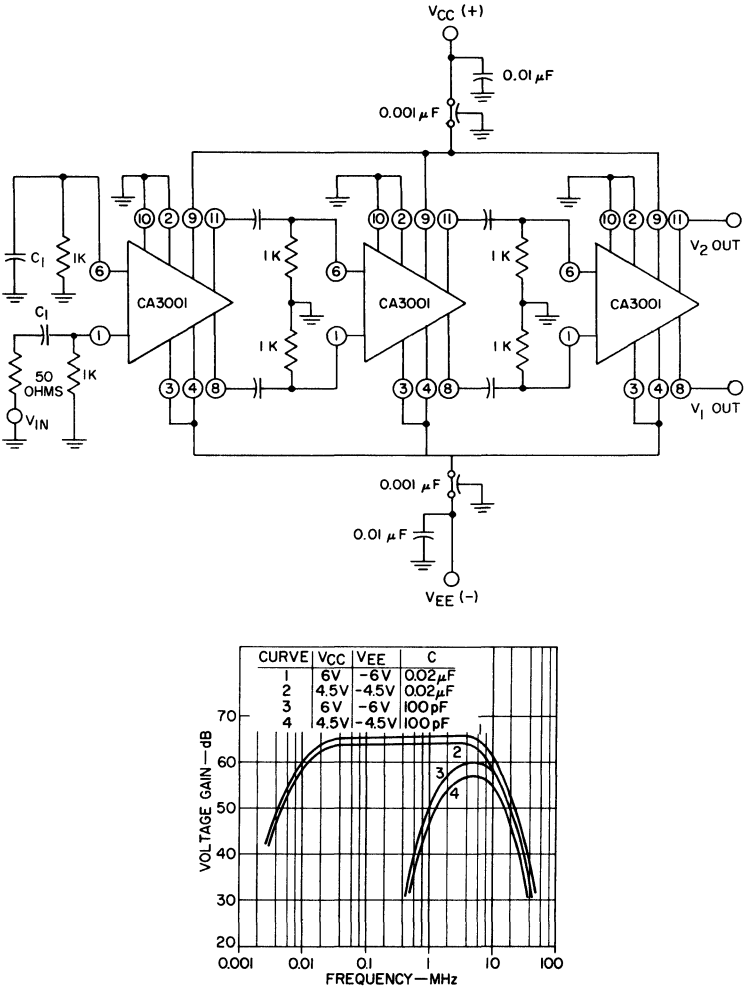


Fig. 102 — Three-stage CA3001 cascade amplifier and frequency-response characteristics.

Schmitt-Trigger Operation

The CA3001 has an advantage in Schmitt-trigger applications because the emitter-follower outputs isolate the impedances of the feedback loop from the differential stage. These outputs are also capable of driving low-impedance loads. When symmetrical power supplies of up to ±6 volts are used, the CA3001 operates without saturation of the basic differential pair (Q_3 and Q_4). For each

of the four operating modes, a complete offset at the input that causes all the sink-transistor current to pass through either Q_3 or Q_4 does not bring these transistors into saturation. As a result, uncertainties resulting in hysteresis prediction caused by storage time are eliminated.

When the CA3001 is connected as a Schmitt trigger, as shown in Fig. 103, the firing points can be changed by adjustment of the resistor R_2. This resistor value effectively sets the voltage at the input terminal 6 and requires that the input firing voltage at termi-

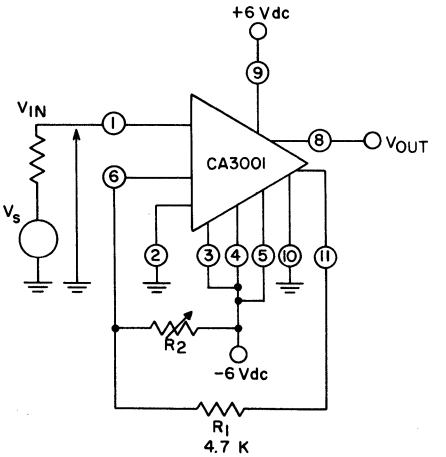


Fig. 103 — CA3001 Schmitt trigger.

nal 1 approach this value to obtain trigger action. The hysteresis voltages obtained for various trigger levels in the circuit of Fig. 103 are shown in Table XII.

Table XII—*Performance Data for CA3001 Used as a Schmitt Trigger*

Input Firing Volts			
Transition from State 1 to State 2	Transition from State 2 to State 1	Hysteresis Volts	R_2 Approximate Setting
3.0	1.5	1.5	max. resistance
1.1	0.1	1.0	decreasing R_2
−1.4	−1.9	0.5	
−3.2	−3.2	0	

IF AMPLIFIER

The CA3002 integrated-circuit if amplifier can be used with either a single-ended or a push-pull input. Its applications include RC-coupled if amplifiers, video amplifiers, envelope detectors, product detectors, and various trigger circuits. The if amplifier is supplied in a 10-terminal TO-5 style low-silhouette package.

Fig. 104 shows the circuit diagram for the CA3002 integrated circuit. The circuit is basically a single-stage balanced differential amplifier (Q_2 and Q_4) with input emitter-followers (Q_1 and Q_5),

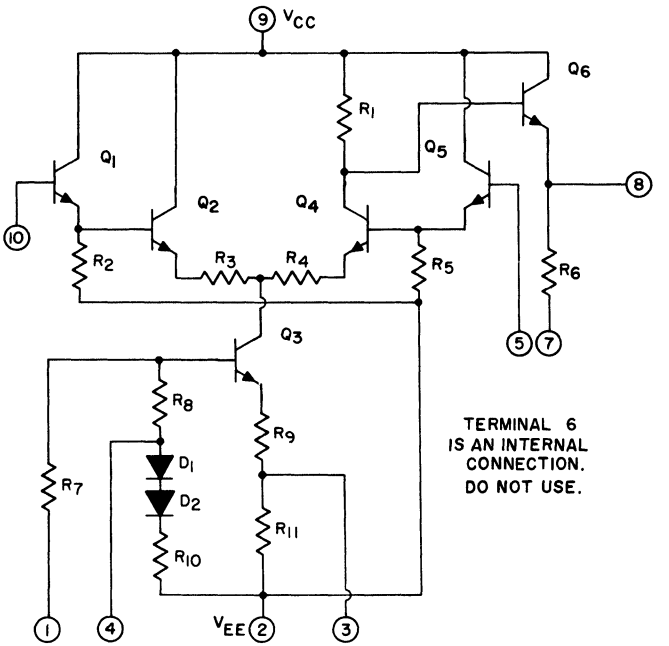


Fig. 104 — Schematic diagram of the CA3002 integrated-circuit if amplifier.

a constant-current sink (Q_3) in the emitter-coupled leg, and an output emitter-follower (Q_6). A single-ended input is connected to terminal 10 or a push-pull input to terminals 10 and 5. A single-ended output is direct-coupled at terminal 8 or capacitance-coupled at terminal 6. Terminals 5 and 10 must be provided with dc returns to ground through equal external base resistors. The emitters of the differential pair (Q_2 and Q_4) are connected through degenerative resistors (R_3 and R_4) to the transistor current source

(Q_3). The use of these resistors improves the linearity of the transfer characteristic and increases the signal-handling capability.

Transistor Q_1 provides a high input impedance for the if amplifier. Transistor Q_5 preserves the circuit symmetry, and also partially bypasses the base of Q_4. Additional bypassing can be obtained by connection of an external capacitor between terminal 5 and ground. The emitter-follower transistor Q_6 provides a direct-coupled output impedance of less than 100 ohms.

Circuit Characteristics

When voltage supplies are connected to the CA3002, the most positive voltage must be connected to terminal 9 and the most negative voltage to terminal 2 (internally connected to the substrate and case). The CA3002 may be operated from various supplies and at various levels. Operation from either single or dual power supplies is feasible. When two supplies are used, they may be either symmetrical or non-symmetrical. When both positive and negative voltage supplies are used, external components can be minimized, as shown in Fig. 105(a). For single-supply applications, a

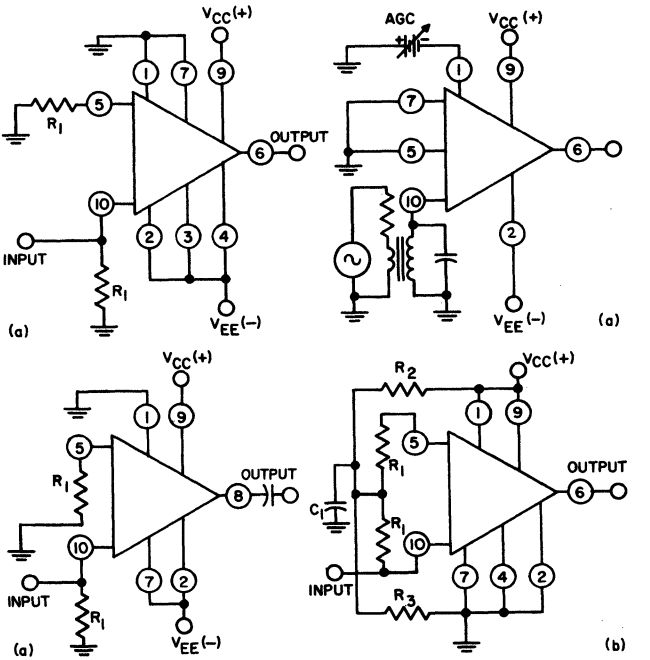


Fig. 105 — Circuit configurations for the CA3002 with (a) dual voltage supplies and (b) a single supply.

resistor divider and a bypass capacitor must be added externally, as shown in Fig. 105(b). The current through R_2 and R_3 should be greater than one milliampere. Except in applications that use inductive drive, equal external base resistors must be added at terminals 5 and 10 to provide base-current returns. Terminal 7 can be connected to ground, or to the negative supply if a larger negative-going voltage swing is desired at any operating point.

For either single or dual supplies, the operating current in transistor Q_3 is determined by the bias voltage between terminals 1 and 2. The more negative point of this bias voltage must be connected to terminal 2. For dual-supply systems, terminal 1 is usually referenced to ground.

Operating Modes — For any given bias voltage (V_{EE} when terminal 1 is grounded), four operating modes are possible, as described in Table XIII. In general, each mode is characterized by (1) a distinct dc operating point with a characteristic temperature dependence, and (2) a particular value of gain that has a distinct temperature dependence.

Table XIII—*Identification of CA3002 Operating Modes*

Operating Mode	Shorted Terminals	Condition of Diodes	Q_3 Emitter Resistor
A	none	in	$R_9 + R_{11}$
B	4-2	out	$R_9 + R_{11}$
C	3-2	in	R_9
D	4-3-2	out	R_9

When the diodes are utilized in the bias circuit (modes A and C), the current is essentially dependent on the temperature coefficient of the diffused emitter resistors R_9 and R_{11}, and has a tendency to decrease with increasing temperature at a rate independent of the negative supply voltage. The temperature coefficient of the diffused collector resistor R_1 is the same as that of the emitter resistor, and a constant collector-voltage operating point results at the collector of transistor Q_4. However, the operating point at output terminal 8 is modified by the base-emitter voltage drop of transistor Q_6 and its temperature dependence. Typical variation of the output operating point with temperature is shown in Fig. 106 for the four operating modes for V_{EE} supplies of −3 and −6 volts. The voltage between terminals 8 and 9 is denoted by V_X. In mode B (with the diodes out of the bias circuit), it should be noted that the output operating point is constant with temperature because the change in the collector operating point is cancelled by the change in the base-emitter voltage drop (V_{BE}).

When the diodes are out of the bias circuit, the current-temperature curves become dependent on the negative supply voltage.

Therefore, the value of V_{EE} can be adjusted so that the transconductance decreases, increases, or remains constant with temperature. As shown in Fig. 107, the gain increases with temperature for a −3-volt V_{EE} supply, but decreases with increasing temperature for a −6-volt V_{EE} supply. At some intermediate value of V_{EE} (approximately −4.5 volts), the gain should be constant as a function of temperature. In any case, however, a constant ac gain with temperature is accompanied by a change in the collector operating point of transistor Q_4.

Table XIV lists typical design performance characteristics for the four operating modes of the CA3002. By use of the data

Table XIV—*Typical Design Performance Characteristics for the Four Operating Modes of the CA3002 (Terminals 7 and 1 are grounded; temperature = 25°C)*

Mode	± Supply Volts	Output Operating Volts (Term. 8 to ground)	Voltage Gain (dB) at 1 MHz	+ Supply Current (mA)	− Supply Current (mA)	Power Dissipation (mW)
A	6	2.6	26.4	5.0	4.2	55.2
B	6	3.8	22.5	4.7	3.7	50.4
C	6	0	*	*	*	*
D	6	1.8	25.4	5.1	4.9	60
A	4.5	2.0	24.0	3.6	3.0	29.7
B	4.5	3.0	19.8	3.4	2.6	27.0
C	4.5	0	*	*	*	*
D	4.5	1.8	24.5	3.7	3.3	31.5
A	3	1.1	22	2.3	2.0	12.9
B	3	2.0	14.5	2.1	1.5	10.8
C	3	0	*	*	*	*
D	3	1.5	20	2.2	1.9	12.3

* Transistor Q_4 saturated, transistor Q_6 cut off.

in this table and in Figs. 106 and 107, it is possible to select the proper operating mode to provide the most transconductance per milliwatt of dissipation, the specified output-swing capability, and the desired temperature performance for a particular design requirement.

In operating mode C, a valid non-saturated operating point may be obtained by use of non-symmetrical voltage supplies. For example, when V_{EE} is −3 volts, the operating point will not be in saturation if a positive supply voltage of 4.5 volts or more is used (as indicated in Fig. 106). Resistor R_6 may then be returned to the negative supply instead of to ground to ensure the desired negative swings.

Input Offset Current — Fig. 108 shows a curve of input offset current of the CA3002 as a function of temperature. This offset current determines the maximum value of total effective external

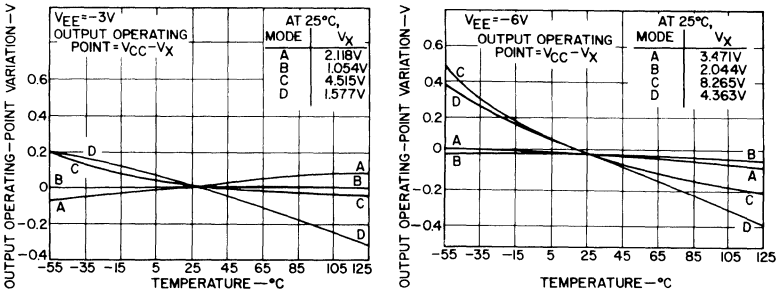


Fig. 106 — Output operating point of the CA3002 (normalized to the 25°C operating point) as a function of temperature with V_{EE} supply voltages of −3 and −6 volts.

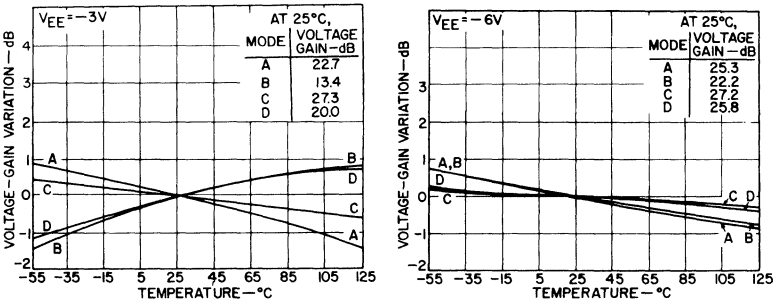


Fig. 107 — Voltage gain of the CA3002 (normalized to the 25°C voltage gain) as a function of temperature with V_{EE} supply voltages of −3 and −6 volts.

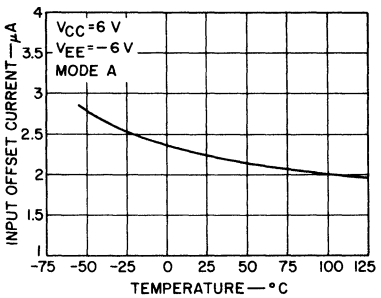


Fig. 108 — Input offset current of the CA3002 as a function of temperature.

resistance that may be used in each base circuit (resistors R_1 in Fig. 105). A maximum value of 10,000 ohms is recommended for each base circuit. However, larger resistances may be accommo-

dated if the resistors can be adjusted to maintain low input offset voltages, or if the operating points of Q_1 and Q_5 are not in the linear region (as in trigger circuits).

Input Impedance — The input impedance of the CA3002 is essentially a characteristic of the input emitter-followers, Q_1 and Q_5. Because these transistors are lightly loaded, they have parallel input impedances that are approximately 0.1 megohm at low frequencies and rise to infinity and become negative at a few megahertz. In most cases, these impedances are negligible in comparison with the impedances of external base resistors or inductors. The input capacitance is 3 to 5 picofarads.

The input impedance decreases with decreasing operating temperature. A typical low-frequency value of parallel input resistance is 55,000 ohms at −55°C. If a resonant line or tuned circuit that has appreciable impedance in the vhf range is connected to either input terminal, a series parasitic resistor of 50 to 100 ohms should be placed in series with the input lead to prevent vhf oscillation.

Output Impedance — The output impedance of the CA3002 is essentially that of the output emitter-follower Q_6, and is a function of the current in Q_6. The current, in turn, is determined by the operating mode, the supply voltages, and the connection of resistor R_6 to ground or to terminal 2. In operating mode D with R_6 returned to ground and ±6-volt supplies, the output resistance is approximately 80 ohms over most of the useful frequency range and rises to about 110 ohms (its highest value) at −55°C.

Frequency Response — The mid-frequency voltage gain of the CA3002 if amplifier is essentially independent of absolute resistor values, but depends on the resistor ratios. Fig. 109 shows a test circuit used to measure the response characteristics of an iterative-coupled amplifier that uses an input-coupling capacitor of 15 picofarads.

The response curves for an iterative-coupled amplifier that uses 0.01-microfarad input-coupling and output-coupling capacitors are shown in Fig. 110. If 1-microfarad coupling capacitors are used, the low-frequency response can be extended below 100 Hz. The addition of a 0.01-microfarad capacitor at terminal 5 improves the high-frequency performance.

Gain Control — The voltage gain of the CA3002 can be controlled over a wide range by adjustment of a negative dc voltage applied at terminal 1. Fig. 111 shows the voltage gain at 1.75 MHz (measured in the test circuit of Fig. 109) as a function of the dc voltage. When the gain is controlled in this manner, the

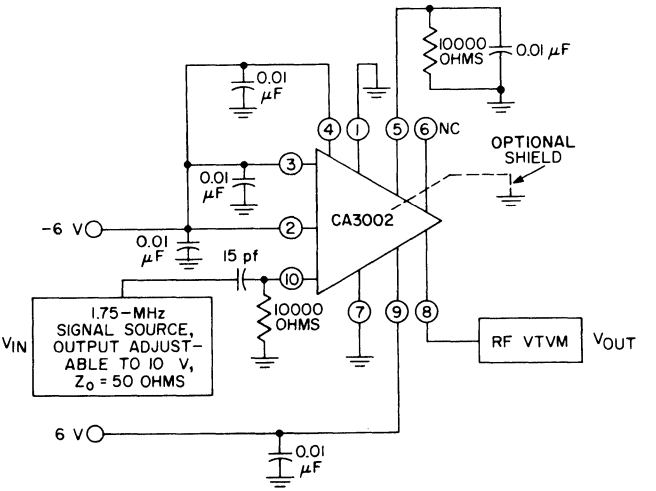


Fig. 109 — Voltage-gain test circuit.

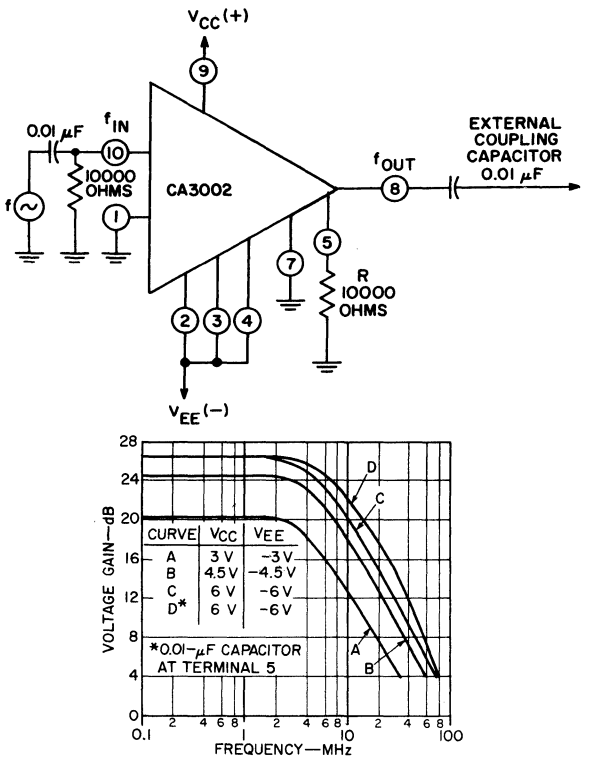


Fig. 110 — Effective single-state response characteristics for CA3002 if amplifier using 0.01-microfarad coupling capacitors. Curve D represents operation with 0.01-microfarad bypass capacitor connected at terminal 5 (not shown).

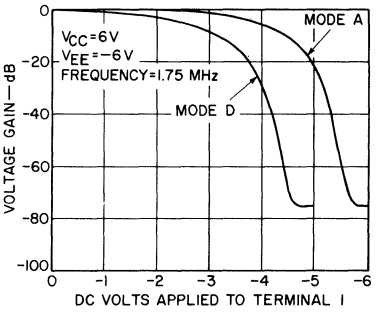


Fig. 111 — Voltage gain of the CA3002 as a function of negative dc supply voltage applied at terminal 1 (normalized to a gain of 26 dB).

CA3002 can be used as an if amplifier with a 75-dB agc range, or as a video gating, squelching, or blanking circuit with a similar range. The circuit function depends only on the manner in which the dc voltage applied to terminal 1 is controlled. The agc range is dependent on frequency, and decreases from 75 dB at 1 MHz to 60 dB at 25 MHz.

Third-Order Intermodulation Distortion — Fig. 112 shows the peak-to-peak input signal required to produce third-order intermodulation distortion of 3 per cent as a function of gain control for the CA3002 integrated circuit. The maximum tolerable signal

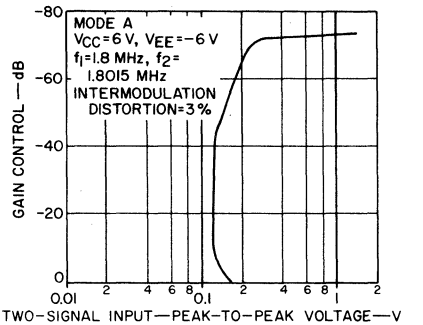


Fig. 112 — Third-order intermodulation characteristics of the CA3002 as a function of agc.

input for 3-per-cent intermodulation distortion is relatively constant over the entire agc range, but increases dramatically as cutoff is attained. When the CA3002 is operated in mode A with supplies of ±6 volts and an agc of −30 dB, a peak-to-peak input signal in excess of 100 millivolts is typically required for 3-per-cent distortion.

Noise Figure — Because noise figure is an important design parameter for both video and if-amplifier applications, it was evaluated for the CA3002 over the frequency range of 1 kHz to 10 MHz. Fig. 113 shows noise performance as a function of frequency when a 1000-ohm source is used. The noise figure is 4 dB over a large portion of the usable range. The 1/f noise corner occurs at approximately 15 kHz, and the high-frequency noise rise begins at approximately 4 MHz. Fig. 114 shows noise figure as a function of source resistance at 1.75 MHz. The typical noise figure is less than 4 dB. It is reasonably flat for source resistances from 500 to 2500 ohms, but rises rapidly at values below 500 ohms.

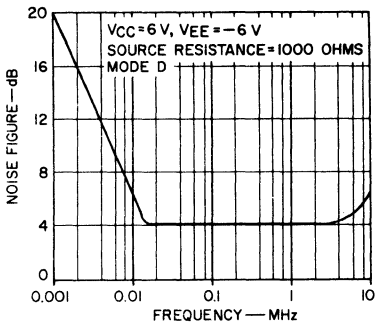


Fig. 113 — Noise figure of the CA3002 as a function of frequency.

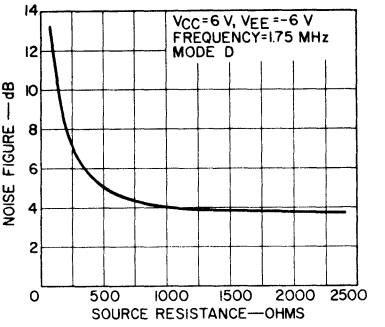


Fig. 114 — Noise figure of the CA3002 as a function of source resistance.

When external base-bias resistors are used, terminal 5 should be bypassed by an external capacitor for any stage in which low noise figure is required. If the base-bias resistors are not bypassed, the noise figure increases. In a practical receiver, bypassing may be avoided if the input at terminal 10 is transformer driven (from a filter) and terminal 5 is grounded. In the later if stages, noise figure can usually be ignored.

Applications of the IF Amplifier

The CA3002 integrated-circuit if amplifier is a versatile circuit that can be used for many diverse applications. The balanced differential amplifier fed from a constant-current source makes an excellent controlled-gain if amplifier. The gain-control function may be extended to include video gating, squelching, and

blanking applications. Envelope detection can be achieved by suitable biasing of the emitter-base diode of the output emitter-follower transistor. Product detection can be obtained by re-insertion of the carrier at the base of the constant-current-source transistor. Various trigger and waveform-generating circuits can also be achieved by the addition of suitable external components.

Envelope Detector — The CA3002 integrated circuit can be operated as an envelope detector in either of two ways, as shown in Fig. 115: (1) the emitter of the output transistor Q_6 can be operated at zero voltage by connection of an external resistor in the bias loop of the constant-current transistor Q_3, or (2) the current in transistor Q_6 can be reduced by connection of a large resistor (12,000 to 18,000 ohms) in series with its emitter resistor.

In the circuit for method 1, the current in the differential pair (Q_2 and Q_4 in Fig. 104) is increased to the point at which

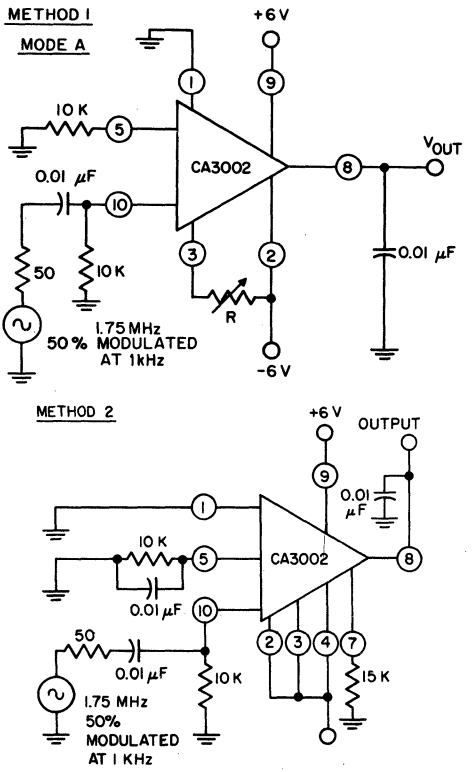


Fig. 115 — Envelope detectors using CA3002 integrated circuits.

the common-collector output transistor Q_6 is biased almost to cutoff. For this current increase, the constant-current transistor Q_3 is operated with terminal 4 open, and the emitter resistor R_9 is shunt loaded by the external resistor at terminal 3. Envelope detection can be accomplished only in mode A with method 1.

Although the output transistor is nearly cut off, all the other active devices are operating in their linear regions. For small ac signals, therefore, the circuit provides linear operation except for Q_6, which is turned on only by a positive signal. The maximum acceptable input signal depends on the linear range of the differential amplifier. An external filter capacitor is connected between terminal 8 and ground to remove the rf signal from the detected audio output.

In the circuit diagram for method 2 shown in Fig. 115, a fixed value of resistance (15,000 ohms) is used to reduce the emitter current in the output transistor (Q_6) to approximately 100 microamperes. This operating point provides the non-linearity for detection in transistor Q_6. Again, the remainder of the circuit produces gain because it is operating linearly. As in the case of method 1, an external filter capacitor is connected between terminal 8 and ground to remove the rf signal from the detected audio output.

Fig. 116 shows the input-output characteristics of the envelope-detector circuits shown in Fig. 115. The usable range of input signals for distortion below 3 per cent is 10 to 100 millivolts (20-dB range) for method 1 and 12 to 60 millivolts (14-dB range) for method 2. Automatic gain control of the if amplifier must maintain the input signals to the detector within this range.

Product Detector — A differential pair driven by a constant-current transistor can be used as a product detector if a suppressed-carrier signal is applied to the differential pair and the regenerated

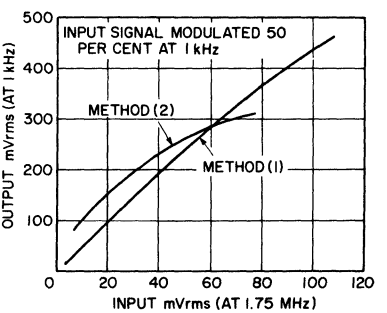


Fig. 116 — Input-output characteristics of the envelope detectors shown in Fig. 115.

carrier is applied to the constant-current transistor. There are two requirements for linearity: (1) the circuit must be operated in a linear region, and (2) the current from the constant-current transistor must be linear with respect to the reinserted carrier voltage.

The CA3002 satisfies these requirements and can be used as a product detector in the circuit shown in Fig. 117. A double-sideband suppressed-carrier signal is applied at terminal 10, and

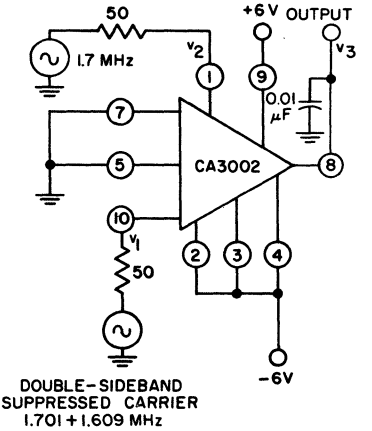


Fig. 117 — Product-detector circuit using the CA3002.

the 1.7-MHz carrier is applied to terminal 1. Because of the single-ended output, a high-frequency bypass capacitor (0.01 microfarad) is connected between terminal 8 and ground to provide filtering for the high-frequency components of the oscillator signal at the output.

When the amplitude of the suppressed-carrier signal and of the oscillator signal are varied, the gain and distortion characteristics shown in Table XV are obtained. The conversion voltage gain is constant at input signals up to 16 millivolts and would be 6 dB less for a single-sideband signal than for the double-sideband signal. The distortion increases with increasing input signal; for distortion of less than 1 per cent, the input drive level does not exceed 8 millivolts. The gain maximizes for oscillator voltages of 1 to 2 volts, and the distortion characteristic is also best in this region. Distortion increases both at low oscillator drive levels (0.25 volt) and at high levels (3 volts).

Table XV—*Performance Data for CA3002 as Product Detector*

V_1 Double-Sideband Voltage (mV)	V_2 Oscillator Voltage at Term. 1 (V)	V_3 Output at Term. 8 at 1 kHz (mV)	Conversion Voltage Gain (dB)	dB down from Fundamental of Harmonics * Harmonic 2nd	3rd
1	1.7	12.5	21.9	60	>65
4	1.7	50	21.9	51	61
8	1.7	100	21.9	46	56
16	1.7	200	21.9	37	46
32	1.7	310	19.8	32	30▲
4	0.25	22	15.6	15	42▪
4	0.5	42	20.3	32	52
4	1.0	60	23.5	45	60
4	1.3	60	23.5	49	61
4	1.7	50	21.9	51	61
4	2.0	48	21.6	52	62
4	2.5	31	17.8	49	60
4	3.0	15	11.4	42	60

* 4th and 5th harmonics greater than 65 dB down except as noted.
▲ 4th harmonic 51 dB down, 5th harmonic 64 dB down.
▪ 4th harmonic 44 dB down.

Schmitt Trigger — Fig. 118 shows the use of the CA3002 as a Schmitt trigger. In this application, the input is applied to terminal 5, and both the output and the feedback are taken from the output emitter-follower at terminal 8. The emitter-follower output isolates the feedback loop from the differential pair and makes it possible for the circuit to drive low-impedance loads. An additional advantage is that neither half of the differential pair saturates as the resistance of the feedback loop is varied. Fig. 118 also shows the output swing and associated hysteresis of the Schmitt trigger as a function of resistor R and the dc input voltage level at terminal 5.

WIDE-BAND AMPLIFIERS

The RCA-CA3021, CA3022, and CA3023 integrated circuits are multi-purpose high-gain amplifiers designed for use in video and AM or FM if stages in single-power-supply systems. These circuits are usable throughout the temperature range from —55°C to 125°C. They are supplied in a 12-terminal TO-5 style package.

The CA3021, CA3022, and CA3023 have the same circuit configuration and the same mid-band open-loop gain. However, different resistor values are used in the three circuits to provide different values of power dissipation and open-loop bandwidth.

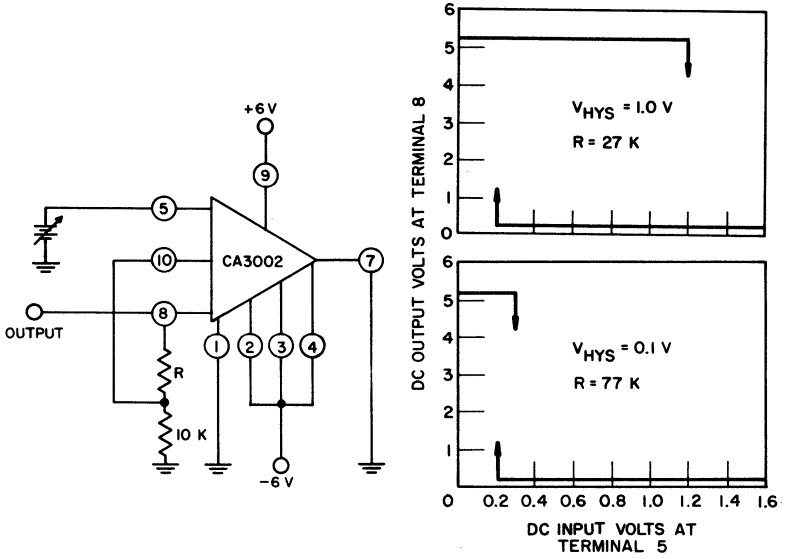


Fig. 118 — Schmitt trigger circuit using the CA3002 and the output swing and associated hysteresis for the circuit.

Typical power dissipation with a 6-volt supply is 3 milliwatts for the CA3021, 12 milliwatts for the CA3022, and 36 milliwatts for the CA3023. Wider bandwidths can be achieved with the CA3023, intermediate bandwidths with the CA3022, and narrower bandwidths with the CA3021.

The major features of these circuits is a flexibility that permits their use in the following applications: video amplifiers operating at frequencies through 30 MHz, AM and FM if amplifiers, and buffer amplifiers in which an isolation capability greater than 60 dB at 1 MHz is desired. The areas of circuit flexibility are as follows:

- Operation with dc supplies of 4.5 to 12 volts.
- Automatic-gain-control capability (60-dB agc range with large input-signal-handling capability).
- Limiting capability (by connection of diodes provided on the chip).
- Gain adjustment (by addition of external feedback resistor or network to obtain desired operating gain and bandwidth).

Circuit Description

The circuit diagram for the CA3021, CA3022, and CA3023 is shown in Fig. 119. Amplifier gain is obtained by use of transistors Q_1, Q_3, Q_4, and Q_6, which are connected as two dc-coupled common-emitter/common-collector amplifiers having a voltage gain of approximately 60 dB. The common-collector configuration provides the necessary impedance transformation (high-impedance input and low-impedance output) for wide bandwidth. The output transistor Q_6 provides the low output impedance desired for iterative operation. The circuit must be capacitively coupled, and should have a low-impedance source.

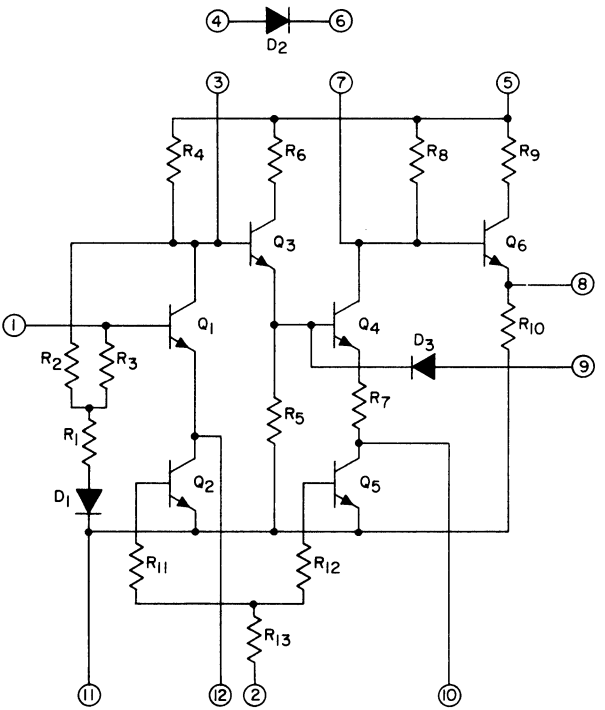


Fig. 119 — Schematic diagram for the CA3021, CA3022, and CA3023 integrated circuits.

Fig. 120 shows typical connections for the CA3021, CA3022, and CA3023 for wide-band and bandpass applications with and without agc, and for limiter applications. An external feedback resistor R_f or a tuned circuit can be added between terminals 3

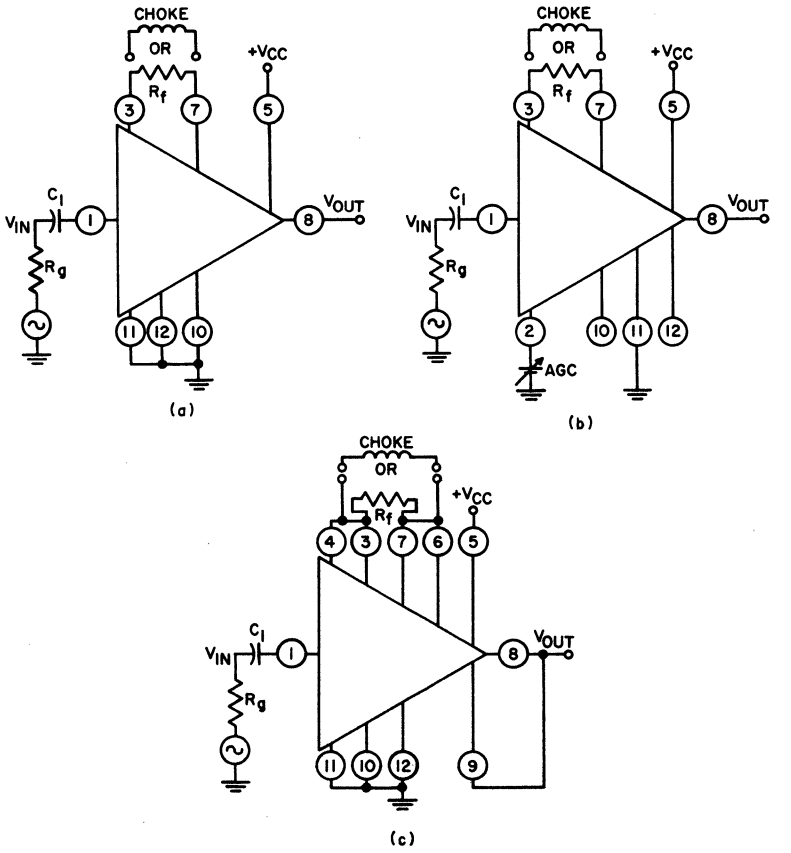


Fig. 120 — Typical connections for the CA3021, CA3022, and CA3023 for (a) wide-band and band-pass applications, (b) wide-band and band-pass applications that require agc, and (c) limiter applications.

and 7 for desired bandwidth and gain performance. Linear operating conditions are maintained by the bias applied between the collector and the base of Q_1 by the resistor-diode network R_2, R_3, R_1, and D_1. Because the collector of Q_1 is held at a fixed potential that is relatively independent of supply, device characteristics, and temperature, dc coupling to the remainder of the circuit can be used.

For applications in which gain control is desired, terminals 10 and 12 are left floating and agc is applied to terminal 2, as shown in Fig. 120(b). For maximum gain, terminal 2 is operated at a positive voltage not larger than the supply voltage applied to terminal 5. In the positive voltage condition, transistors Q_2 and

Q_5 are saturated and the impedance in the emitters of Q_1 and Q_4 is low. When the gain-control voltage becomes negative, Q_2 and Q_5 come out of saturation and provide high degenerative emitter resistance which reduces the gain. Because most of the increasing signals appear across the increasing degenerative resistance, the active gain transistors Q_1, Q_3, Q_4, and Q_6 handle only a small part of the large signal. As a result, signal-handling capability increases with increasing agc. Further increases of gain-control voltage reduce the current in Q_1 and Q_4 and thus provide the additional gain control needed to achieve maximum agc range.

In limiting applications, diodes D_2 and D_3 are connected in the feedback loops, as shown in Fig. 120(c) (terminals 4 to 3, 6 to 7, and 8 to 9). The diodes provide clamping for sufficient input-signal swing; limiting can be achieved with input-signal swings up to 2.5 volts rms.

Biasing Requirements

The most positive voltage to be applied to the CA3021, CA3022, and CA3023 integrated circuits is connected to terminal 5. The most negative voltage is connected to the substrate through terminal 11.

The circuits can be used with single power supplies of 4.5 to 12 volts. The bias technique used for transistor Q_1, and thus for the remainder of the circuit, makes the collector operating voltage of Q_1 and Q_4 relatively independent of the supply. Consequently, the current in the circuit increases almost linearly as a function of supply voltage. Fig. 121 shows typical power dissipation for the three circuits as a function of supply voltage. Because there is little change in the collector voltage of Q_4, there is little change in output operating point as a function of supply voltage.

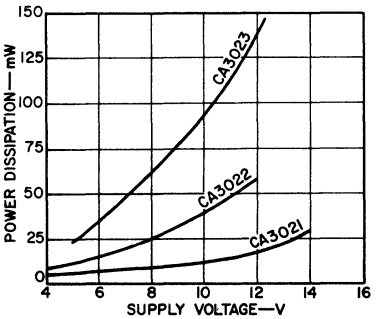


Fig. 121 — Power dissipation as a function of supply voltage for the CA3021, CA3022, and CA3023.

DC Stability with Temperature — The output operating points of the CA3021, CA3022, and CA3023 are shown in Fig. 122 as a function of temperature and feedback resistance. As a result of the resistor values used in each circuit, the output operating point is compensated in the temperature range between —20°C and 75°C

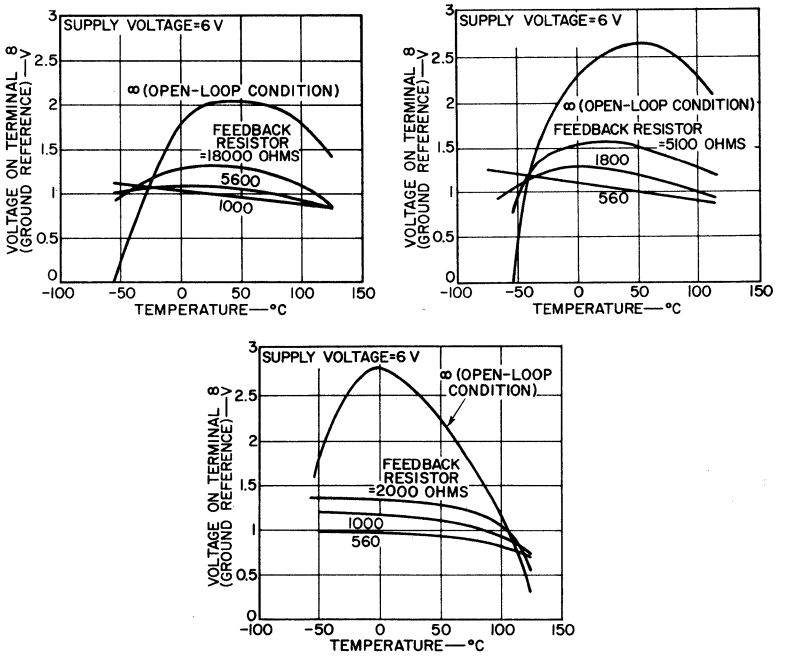


Fig. 122 — Output operating point of the CA3021, CA3022, and CA3023 as a function of temperature for various values of feedback resistance.

when the circuit is operated under open-loop conditions (terminals 3 and 7 floating). Insertion of a feedback resistor between terminals 3 and 7 is recommended to minimize degradation in performance at temperatures outside this range. The maximum value of the feedback resistor R_f recommended for optimum performance of each circuit is as follows:

Circuit	*Feedback Resistance, R_f — ohms*
CA3021	18000
CA3022	5100
CA3023	2000

Use of a feedback resistor of the maximum value provides equal ac and dc feedback, but reduces the usable gain of the circuit to

approximately 40 dB. When equal ac and dc feedback is not desired, as in the case of bandpass or tuned responses, a choke or tuned circuit can be included between the feedback terminals 3 and 7 to provide dc temperature stability and permit gains of 50 to 55 dB.

As a general rule, feedback should be included in all applications in which operation over an extended temperature range is required.

DC Considerations for Gain Control — When the agc transistors Q_2 and Q_5 are included in the circuit, the output operating point can be held constant only by addition of feedback. Variation of operating point is caused by the added collector-to-emitter voltage of Q_2 and Q_5 in saturation in the emitters of Q_1 and Q_4. The effect is more pronounced in the higher-current circuits CA3022 and CA3023. As discussed previously, full dc feedback can be used to stabilize the operating point; ac feedback can be removed by the use of tuned circuits. The maximum recommended values of R_f provide satisfactory stability when the circuit is connected for agc.

DC Considerations for Limiting — In limiter applications, diodes D_2 and D_3 are included in the feedback loops in the circuit [external connections are made as shown in Fig. 120(c)]. Under open-loop conditions, the dc operating point may be such that D_2 and D_3 (usually D_3) are turned on. The gain is then reduced and the amplifier will not operate linearly at low levels. The values of R_f recommended previously also assure correct operation for limiting amplifiers.

Gain-Frequency Characteristics

Open-loop frequency responses for the CA3021, CA3022, and CA3023 are given in Fig. 123. The curves also show the response characteristics to the 3-dB point for various values of feedback resistance. Values of feedback resistance larger than those recommended for operating-point temperature stability are included to indicate gain performance at resonance when tuned circuits or chokes are used in the feedback loop. For these measurements, the circuits were operated with a 50-ohm source and a high impedance load.

Fig. 124 shows the variation of gain with temperature for the three circuits. Each circuit was operated with sufficient feedback to provide a closed-loop gain of approximately 40 dB. The gain variation is practically independent of feedback, and is slightly greater for the CA3023 than for the other two circuits. Fig. 125

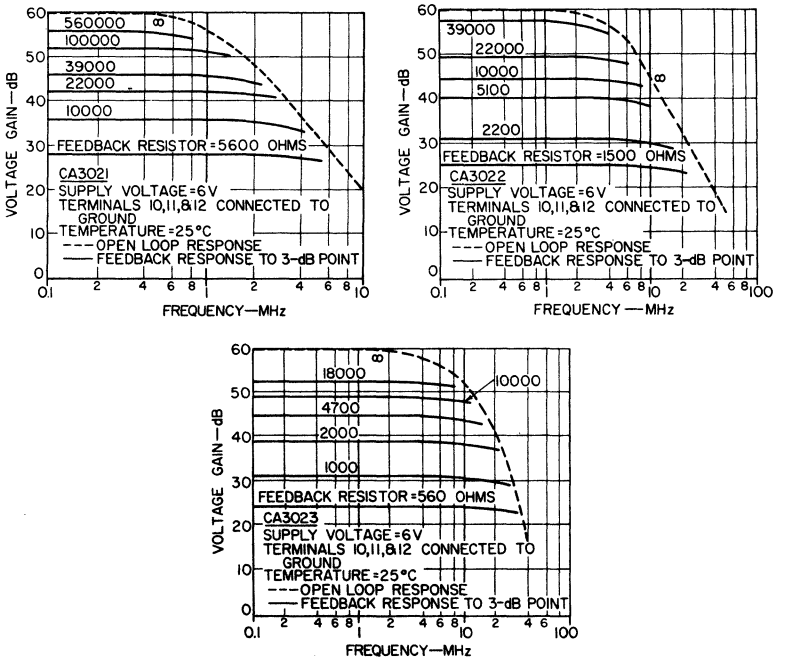


Fig. 123 — Frequency-response characteristics of the CA3021, CA3022, and CA3023.

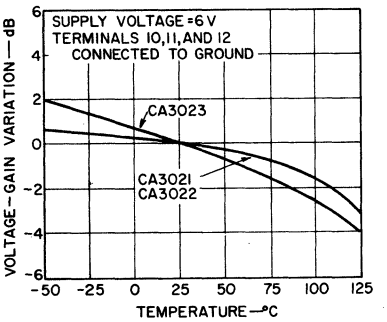


Fig. 124 — Voltage-gain variation with temperature for the CA3021, CA3022, and CA3023 (feedback adjusted to provide gain of approximately 40 dB at 25°C).

shows typical upper-3-dB frequency shifts with temperature for the three circuits for a gain of approximately 40 dB.

In buffer-amplifier applications, reverse feedback or isolation capability is required. Table XVI shows the isolation performance of the CA3021, CA3022, and CA3023 at three frequency levels with the input terminated in 50 ohms.

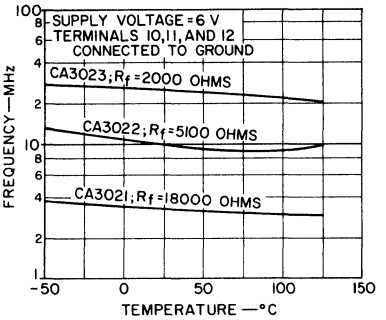


Fig. 125 — Upper 3-dB frequency shift with temperature for the CA3021, CA3022, and CA3023.

Table XVI—*Isolation Performance of the Wide-Band Amplifiers*

Circuit	Feedback Resistor R_f (ohms)	Voltage at Output (volts rms)	Resultant Feedthrough Input Voltage Below the Applied Output Voltage (dB) f = 1 MHz	f = 10 MHz	f = 50 MHz
CA3021	18000	2	66	66	54
CA3022	5000	2	66	66	54
CA3023	2000	2	66	66	52

Power-Output Capability

The maximum power-output capability of the common-collector output transistor Q_6 in Fig. 119 occurs for a load-resistance value higher than the output impedance. For determination of optimum load-resistor values, each circuit is operated from a 6-volt supply at a gain of approximately 40 dB with a variable resistor capacitively coupled to terminal 8. The variation of maximum linear signal output as a function of load resistance is shown in Fig. 126. Maximum power output is measured at a level at which output distortion is just discernible on an oscilloscope.

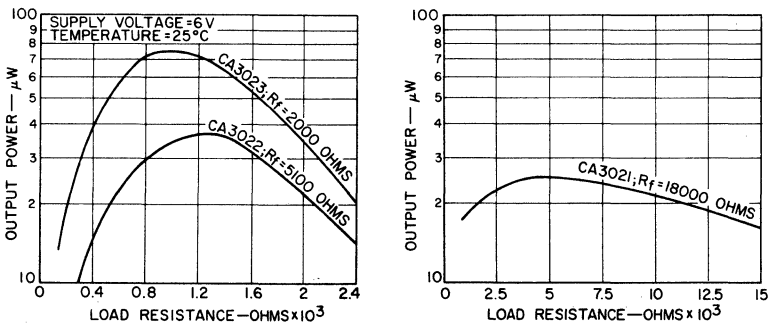


Fig. 126 — Maximum linear signal output of the CA3021, CA3022, and CA3023 as a function of load resistance.

Tuned Circuit in the Feedback Loop

When a parallel tuned circuit is included in the feedback path between terminals 3 and 7 of the CA3021, CA3022, or CA3023, the gain at resonance is a function of the equivalent resistance of the feedback loop. Gain characteristics of the three circuits as a function of feedback resistance are shown in Fig. 127. For each circuit, there is a value of feedback resistance R_f for which the gain approaches zero. This condition occurs when the small-signal transconductance g_m of the transistor Q_4 is equal to the conductance of the parallel tuned circuit; signal cancellation

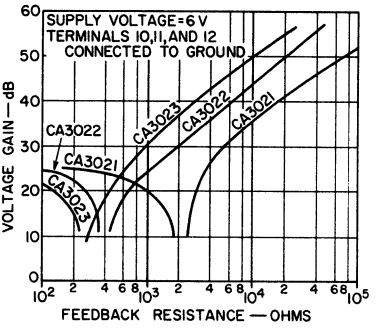


Fig. 127 — Voltage gain of the CA3021, CA3022, and CA3023 as a function of feedback resistance.

then results at terminal 7. In a tuned circuit designed with the correct feedback resistance R_f, therefore, zero gain can be obtained at the resonant frequency. The resistance valus required for signal cancellation are 2000 ohms for the CA3021, 400 ohms for the CA3022, and 230 ohms for the CA3023. When the tuned-circuit impedance is made equal to these cancellation resistance values at resonance, the gain increases at frequencies off resonance and a trapping effect results. For zero feedback resistance, the gain of each circuit is approximately 24 dB. For values of feedback resistance in excess of the cancellation resistance, the gain increases. When the tuned circuit has a resonant impedance higher than the cancellation resistance, the response is added to the video response characteristic, as shown in Fig. 128. Then, because no purely resistive value occurs that is equal to the cancellation resistance, no cancellation occurs.

The bandwidth of the response can be approximated by determining the total loading of R_p on the parallel tuned circuit in the feedback path, as follows:

$$R_p = \frac{R_T\ R_X\ (R_4 + R_8)}{(R_X + R_T)\ (R_4 + R_8) + R_X\ R_T} = \omega_0\ L_Q > R_{fc} \quad (181)$$

where R_T is the resistance at resonance of the unloaded Q, R_X is the resistance added to the tuned circuit for adjustment of gain, and $(R_4 + R_8)$ is the series combination of the two common-collector load resistors. The 3-dB bandwidth for the response is given by

$$\frac{f_0}{\Delta f} = \frac{R_P}{X_L} = \frac{R_P}{X_c} = Q_L \quad (182)$$

Typical values for $(R_4 + R_8)$ for the three circuits are 39000 ohms for the CA3021, 10900 ohms for the CA3022, and 4800 ohms for the CA3023.

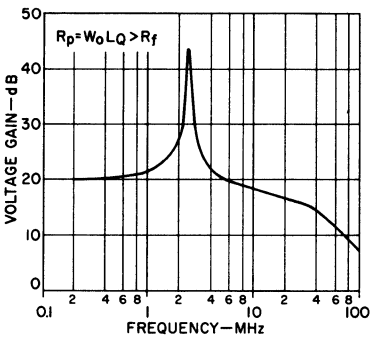


Fig. 128 — Voltage gain as a function of frequency in a band-pass amplifier when the tuned-circuit resonant impedance R_p is higher than the cancellation resistance R_{fc}.

Output Tuned Circuits

The curves of Fig. 126 indicate that capacitive coupling of the common-collector output transistor Q_6 to a matched load severely limits the transistor output-voltage-swing capability. If the required mismatch is achieved by ac coupling of a tuned circuit directly across the output, the tuned circuit will be loaded by the low output impedance of the common-collector transistor. However, comparable output power can be obtained by use of a resistor in series with the circuit output and the tuned circuit. This arrangement provides a load for the common-collector transistor for frequencies of resonance of the tuned circuit, and prevents the possibility of reactive loads causing emitter-follower transistor instability.

Gain Control

The CA3021, CA3022, and CA3023 are connected as shown in Fig. 120(b) when gain-control application is desired. Transistors Q_2 and Q_5 are then included in the emitter-signal path of transistors Q_1 and Q_4, respectively. For maximum gain, a positive voltage is applied to terminal 2 which saturates transistors Q_2 and Q_5. If a voltage of 6 volts is applied to terminal 2, the typical gain-control current is 0.8 milliampere. The gain-control action is provided by reduction of the voltage on terminal 2. The decreasing voltage causes transistors Q_2 and Q_5 to come out of saturation and present a high impedance in the emitter leads of transistors Q_1 and Q_4. It is important that good filtering and isolation be maintained at the agc terminal 2 because transistors Q_2 and Q_5 are in the linear active region for a portion of the agc range and can, therefore, provide gain for a signal on the agc terminal.

The minimum gain is determined by a combination of the gain of Q_1 and feed-through to the collector of Q_1 along a resistance path made up of R_3 and R_2. Because the signals are out of phase, there is a point at which cancellation of signal results. This cancellation occurs in all three circuits when terminal 2 is 0.5 volt more negative than terminal 11. It is accompanied by severe distortion of signal and AM modulation. Techniques for obtaining agc without reaching the cancellation point are discussed later.

When the maximum recommended feedback resistance for operating-point stability is used in the connection of Fig. 120(b), maximum gain is reduced because of the extra emitter resistance presented by the saturation resistance of transistors Q_2 and Q_5. Maximum voltage gain for each circuit is approximately 30 dB with the maximum recommended feedback resistance and a 6-volt supply. The typical agc range for each circuit is 55 dB with resistive feedback.

When a tuned circuit is used in the feedback loop, higher maximum gain can be obtained in the agc connection shown in Fig. 120(b). The maximum gain obtainable is approximately 50 dB when high feedback impedance is maintained. A self-resonant choke is a convenient element to add in the feedback loop to obtain high impedance because it provides wide bandwidth; resistance loading can be added to adjust the gain to the desired value. When a combination of self-resonant choke and added resistance is used, dc feedback is complete and the operating point is temperature-stable. Wide-bandwidth tuned circuits are suggested for all three circuits, but especially for the CA3022 and CA3023 because the

bandwidth shifts with gain control, as shown in Fig. 129. For a tuned frequency of 3 MHz at full gain, for example, the resonance point of the tuned response increases slightly (about 5 per cent) for gain control of —20 to —30 dB because of the combination of the low-frequency roll-off and the tuned response. In the region of gain control of —50 dB, the high-frequency roll-off affects the response and the resonant frequency decreases below 3 MHz

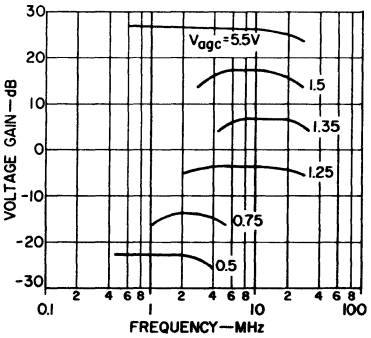


Fig. 129 — Effect of gain control on response characteristics of the CA3021, CA3022, and CA3023.

(by about 10 per cent). At full agc the tuned circuit becomes a trap in the feed-through path, minimum gain is achieved at the 3-MHz frequency, and the response is inverted, i.e., a notch occurs where a bandpass had existed. When tuned circuits are included in the feedback path of the gain-controlled amplifier, therefore, it is recommended that the bandwidth be chosen as wide as possible to minimize detuning effects. Desired bandwidth control should be obtained at the input, at the output, or in the feedback path of stages without gain control.

The use of emitter degeneration as a gain-control technique improves signal-handling capability. At full gain control, signals as high as 2 volts rms can be handled without the occurrence of serious overload distortion. Typical cross-modulation characteristics for the CA3021, CA3022, and CA3023 with only feedback resistance in the feedback loop are shown in Fig. 130. Maximum gain for each circuit is approximately 30 dB. When a tuned circuit is used in the feedback loop, more gain-control range is available as a result of the feedthrough reduction. Depending on the impedance of the tuned circuit, the gain-control range is between 60 and 80 dB. The cross-modulation characteristics when tuned circuits are used are similar to those obtained with resistive feedback except for modifications caused by different feedback characteristics of interfering signals outside the tuned-circuit passband.

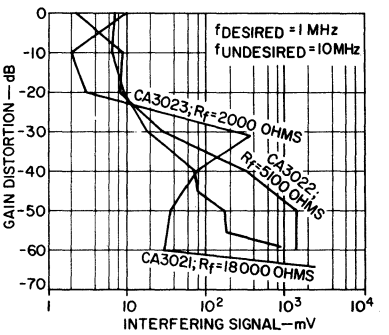


Fig. 130 — Cross-modulation distortion characteristics of the CA3021, CA3022, and CA3023.

Limiting

For applications in which signal limiting is required, the diodes of the CA3021, CA3022, and CA3023 are connected as shown in Fig. 120(c). At low signal levels, the diodes are cut off and the gain performance is similar to that described previously except for some bandwidth reduction caused by the inherent capacitance of the diodes. For large input-signal swings in the negative direction, the collector of transistor Q_1 becomes positive and the collector of transistor Q_4 becomes negative, and diode D_2 begins to conduct. This action clamps the collector of Q_1 to the collector of Q_4 and, because the diode is in the feedback path, reduces the gain. For positive swings at the input, the collector of transistor Q_1 becomes negative and the output at terminal 8 becomes positive. Two effects tend to limit input signals of positive polarity: transistor Q_4 going to cutoff, and diode D_3 going into conduction. When the circuits are connected as shown in Fig. 120(c), limiting is symmetrical at the onset. With increased signal, however, the symmetry is not perfectly preserved because of dc shift in the circuit. Typical output-signal characteristics as a function of input level are shown in Fig. 131. The lack of symmetry at high input levels causes a decrease in power output, as shown in the waveforms.

Limiting characteristics for the CA3021, CA3022, and CA3023 are measured in the circuit configuration shown in Fig. 132. The output tuned circuit is designed to provide filtering for the desired output frequency so that rms values of output voltage can be obtained. Limiting characteristics are measured for two types of feedback, resistive and tuned circuit; results are shown in Fig. 133. When a resonant circuit is used in the feedback loop, the gain of the circuits is higher and limiting occurs at a lower input level. The effects of multistage limiting are described later.

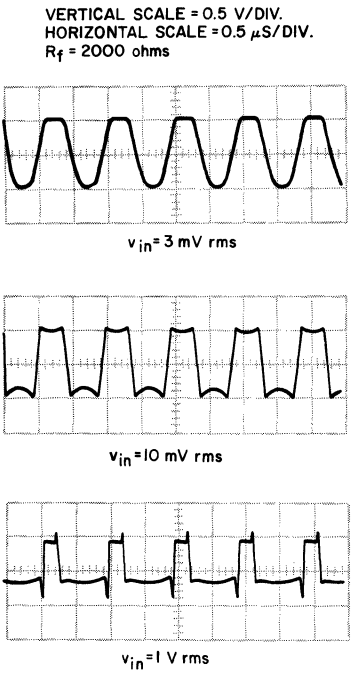


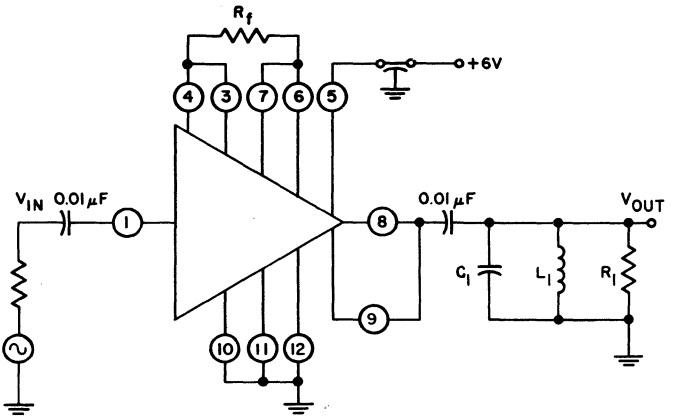
Fig. 131 — Output waveforms obtained in limiter applications using the CA3021, CA3022, and CA3023.

Noise Performance

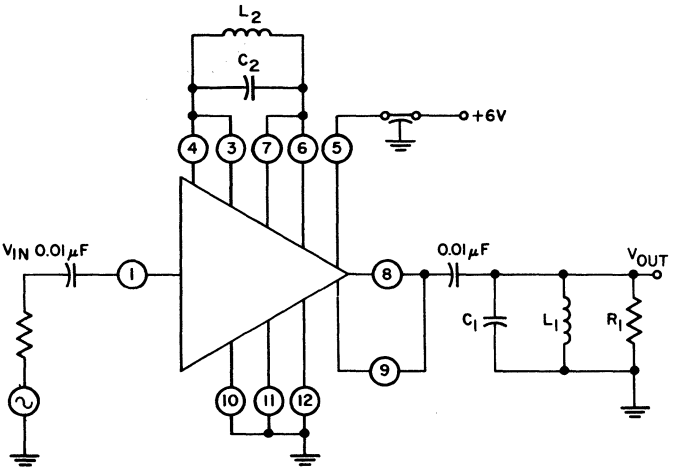
Table XVII shows typical noise figures for the CA3021, CA3022, and CA3023 circuits for a frequency of 1 MHz, a supply voltage of 6 volts, and a source resistance of 50 ohms. The data in the first column of noise figures were measured in the connection shown in Fig. 120(a); the second column shows data measured in the connection shown in Fig. 120(b).

Table XVII—*Typical Noise Figures for the Integrated-Circuit Wide-Band Amplifiers*

	Noise Figure — dB	
Circuit	Term. 10, 11, 12 connected to ground; gain = 40 dB	AGC operating, noise measured for maximum gain of 30 dB
CA3021	5.8	7.5
CA3022	7.1	8.7
CA3023	7.2	8.7



(a)



(b)

TYPE	FREQ. (MHz)	C_1 (pF)	L_1 (μH)	R_1 (kΩ)	CIRCUIT(a) R_F (kΩ)	CIRCUIT(b) L_2 (mH)	CIRCUIT(b) C_2 (pF)
CA3021	0.5	2000	36-64	8.2	18	10	-
CA3022	1	5000	3-5	1	5.1	1.2	4-45
CA3023	5	600	1.8	1	2	-	-

Fig. 132 — Test circuit used to evaluate limiting characteristics of the CA3021, CA3022, and CA3023.

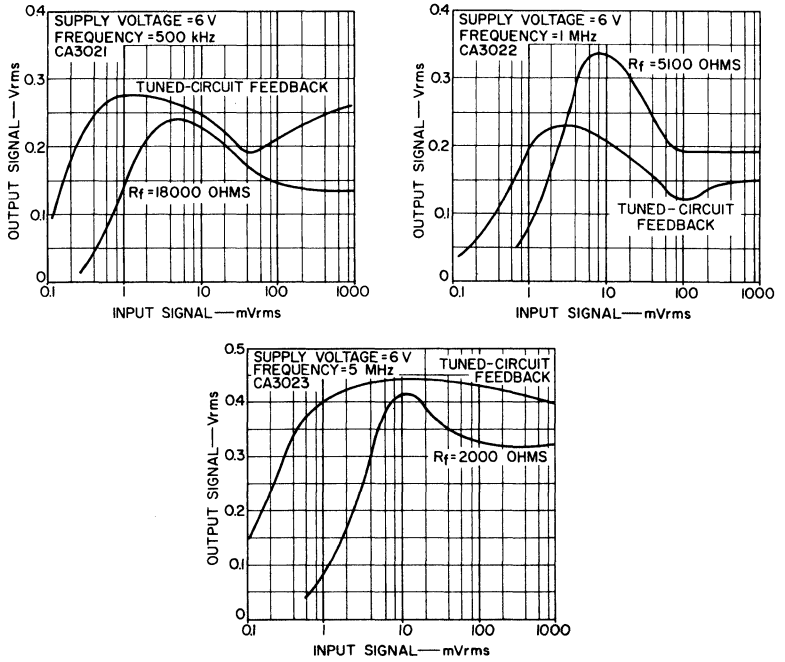


Fig. 133 — Limiting characteristics of the CA3021, CA3022, and CA3023.

Applications

The following paragraphs describes several typical applications of the integrated-circuit wide-band amplifiers.

Video Amplifiers — The use of single CA3021, CA3022, or CA3023 integrated circuits in video applications was discussed previously. For an evaluation of iterative video performance, two CA3022 circuits were operated in cascade. Each circuit employed 0.01-microfarad coupling capacitors and feedback resistors of 2000 ohms. Performance data can be summarized as follows:

Supply voltage	6	volts
Supply current	4.5	mA
Power dissipation	27	mW
Voltage gain	61	dB
Maximum undistorted output with 510-ohm load	0.25	Vrms
Signal level for a 3-dB signal-to-noise ratio	11	μV

Dynamic range (input-output linearity)	27	dB
Bandwith, 3-dB points:		
upper frequency	10.5	MHz
lower frequency	50	kHz

10-MHz IF Amplifier — Fig. 134 shows a 10-MHz amplifier employing two CA3023 circuits. The first stage is operated in a broadband mode with a 2000-ohm feedback resistor between terminals 3 and 7, in accordance with the design rules described previously. The second stage is a tuned if amplifier. Because the sinusoidal output capability of the CA3023 at 10-MHz is in the 200-millivolt range, it is necessary to step up the voltage to drive the envelope detector; therefore, a tuned transformer that has a 1-to-4 turns ratio is used at the second-stage output. The total effective circuit Q for this if configuration is 200, and the full rf voltage gain is 86 dB from the input of the first stage to the output of the step-up transformer.

A CA3018 integrated-circuit transistor array is used to provide detection, audio amplification, and dc amplification. (The CA3018 circuit is described in a later section.) Detection is provided by transistors Q_3 and Q_4 of the CA3018; the detected output is passed through a low-pass filter (C_1, C_2, and R_1) and applied to the agc amplifier transistor Q_2. Transistor Q_2 goes from cutoff to saturation with increasing signal. The voltage drop across a 100-ohm degenerative resistor R_2 prevents the gain-control voltage in terminal 2 of the first CA3023 amplifier from decreasing below 0.5 volt and causing signal cancellation. Transistor Q_1 of the CA3018 provides audio gain and is biased in a conventional manner. Fig. 134 also shows the output-signal and noise characteristics of the circuit as functions of rf input level for an input signal that is 30-per-cent modulated by a 1-kHz sine wave. The audio-output equivalent-noise bandwidth is 2.6 kHz.

455-kHz IF Amplifier — Fig. 135 shows a 455-kHz two-stage if amplifier using the CA3021. The tuned-circuit approach discussed previously is used in the first stage. The rf feedback choke is self-resonant at 455 kHz and has a Q of 3.2 in the circuit. The second stage is a video amplifier. Input filtering would normally be provided to obtain the desired if response. For the particular choice of stage gain and agc loop gain, an interstage pad network is used to maintain stability and achieve an acceptable signal-to-noise ratio with gain control. The CA3018 output configuration is essentially the same as that used in the circuit of Fig. 134. The signal and noise characteristics of the 455-kHz amplifier

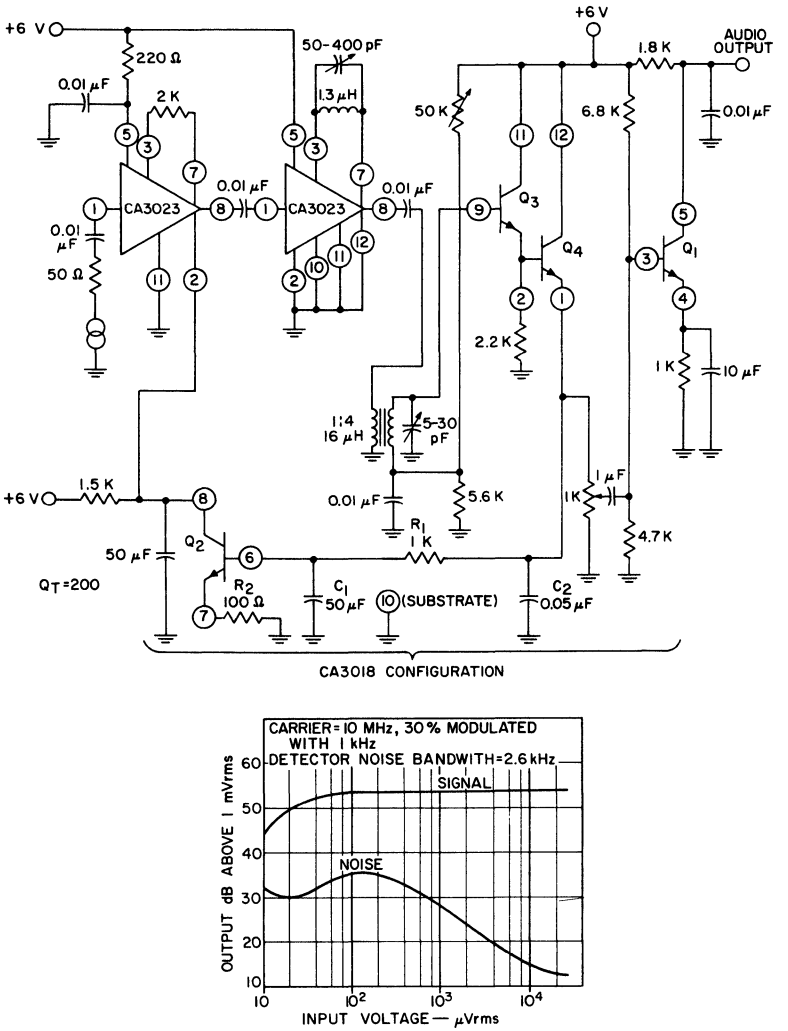


Fig. 134 — Schematic diagram and performance curves for 10-MHz if amplifier using two CA3023 circuits.

are also shown in Fig. 135 for the same conditions used for the 10-MHz amplifier.

28-MHz Two-Stage Limiter Amplifier — Fig. 136 shows the circuit diagram of a 28-MHz two-stage limiter amplifier using two CA3023 integrated circuits. Terminals 3 and 7 are connected to terminals 4 and 6, respectively; terminal 8 is connected to terminal 9 to provide limiting action. A self-resonant coil in parallel with

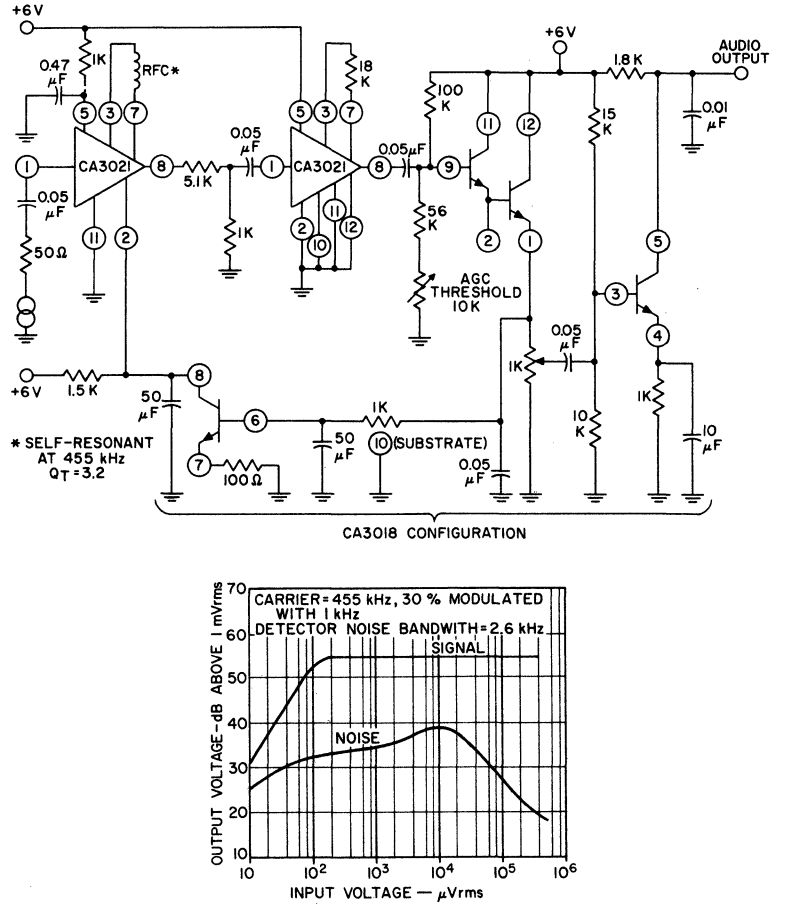
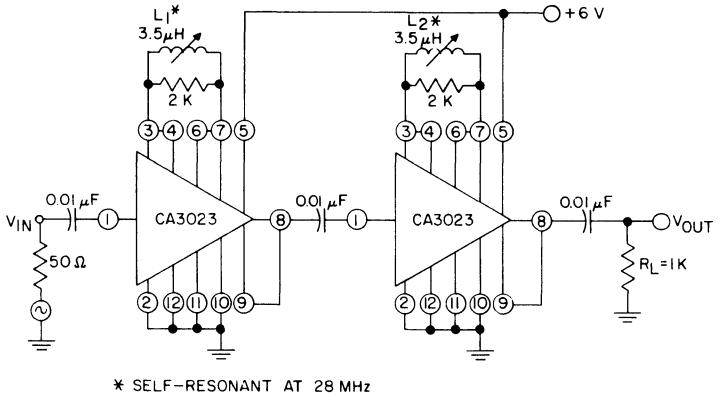


Fig. 135 — Schematic diagram and performance curves for 455-kHz if amplifier using two CA3021 circuits.

a 2000-ohm resistor is inserted in the feedback loop of each amplifier to provide gain and stability. The bandwidth of the system before limiting is 3.8 MHz, and the effective Q is 7.35. The total gain is 61 dB (30.5 dB per stage), and the power dissipation is 66 milliwatts. Fig. 136 also shows the limiting performance of the system. Full limiting occurs at an input of 300 microvolts.

500-kHz Limiting Amplifier — Fig. 137 shows the circuit diagram of a 500-kHz limiting amplifier using two CA3021 circuits. Two 500-kHz self-resonant chokes are used in the feedback path. A tuned circuit is included in the output to obtain a sine-wave output. The limiting characteristics of this amplifier are also



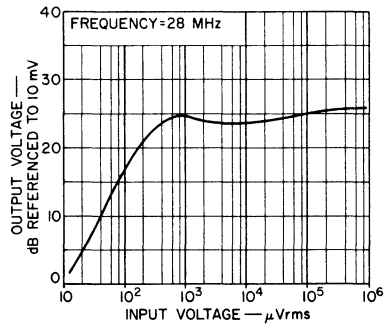


Fig. 136 — Schematic diagram and limiting performance of two-stage limiter-amplifier using the CA3023.

shown. Although limiting occurs for noise, a limited signal is apparent above the noise at an input signal of 1 microvolt. Because of the noise and early limiting, voltage gain can only be estimated; however, it is at least 100 dB. Good limiting performance is obtained for input signals up to 3 volts rms. Total power drain for the circuit with a 6-volt supply is approximately 6 milliwatts.

RF AMPLIFIERS

The CA3004, CA3005, CA3006, and CA3028A integrated-circuit rf amplifiers are supplied in TO-5 style packages. The CA3004, CA3005, and CA3006 are 12-terminal units designed to operate from low or medium dc supply voltages at frequencies from dc to 120 MHz. These circuits may be operated from single or dual dc power supplies. For dual-supply operation, either symmetrical or

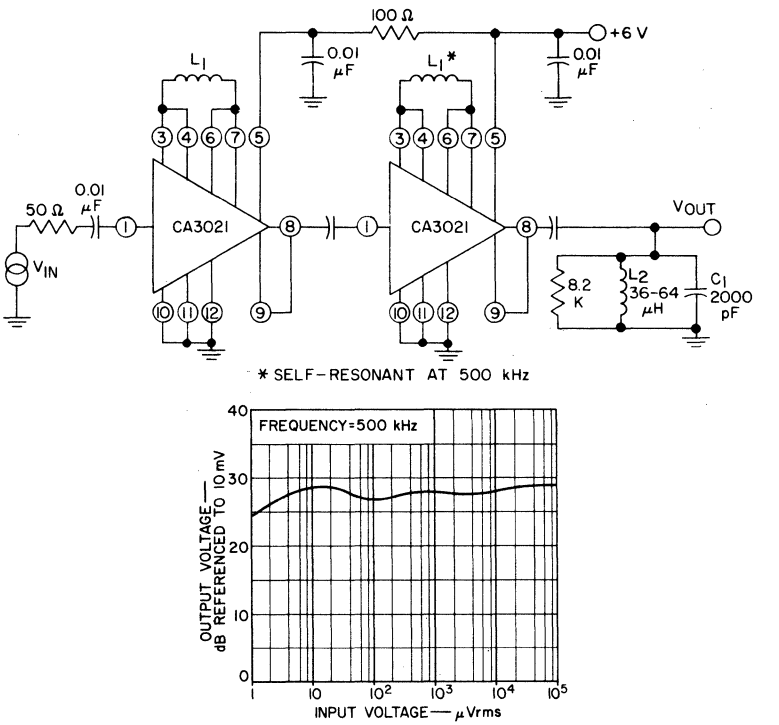


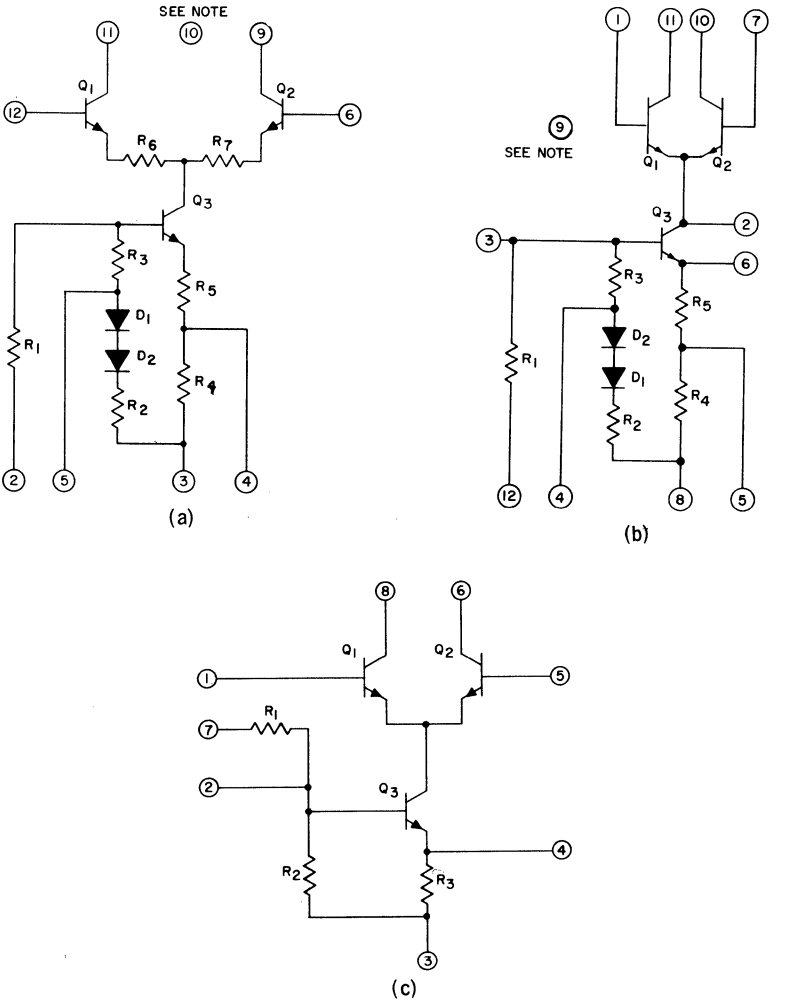
Fig. 137 — Schematic diagram and limiting performance of two-stage 500-kHz limiter-amplifier using the CA3021.

nonsymmetrical power supplies may be used. The CA3028A is an 8-terminal unit designed to operate from a single dc supply of 9 or 12 volts at frequencies from dc to 125 MHz. All the rf amplifiers have an inherent gain-control capability and provide stable operation over a range of ambient temperatures from — 55°C to + 125°C. These circuits are extremely versatile devices and may be used with external tuned-circuit, transformer, or resistive load impedances to provide the following types of functions:

1. Wide- or narrow-band amplification
2. Mixing
3. Limiting
4. Product detection
5. Frequency generation
6. Generation of pulse or digital waveforms

Operating Requirements and Characteristics

Fig. 138 shows the schematic diagrams for the CA3004, CA3005, CA3006 and CA3028A integrated-circuit rf amplifiers.



Note: Connect to most positive dc supply voltage.

Fig. 138 — Schematic diagrams of the integrated-circuit rf amplifiers: (a) CA3004, (b) CA3005 or CA3006, and (c) CA3028A.

Each circuit consists of a balanced differential amplifier that is driven from a controlled, constant-current source.

In the CA3004 circuit, resistors (R_6 and R_7) are included in the emitter leads of the differential pair of transistors, Q_1 and Q_2. The degeneration introduced by these unbypassed emitter resistors improves the linearity of the transfer characteristics and increases the single-handling capabilities of the circuit. Fig. 139

shows the dynamic transfer and limiting characteristics of the CA3004. The characteristics show that linear operation is possible over a wide range of differential input voltage and, thus, indicate that relatively large input signals can be handled by the circuit without limiting. These features indicate that the CA3004 is particularly useful for applications in which the ability to handle large input signals is an important consideration.

In the CA3005, CA3006 and CA3028A circuits, no emitter resistors are provided for the differential pair of transistors. As a result, these circuits have a smaller dynamic range and provide higher gain than the CA3004 circuit. The dynamic transfer and limiting characteristics of the CA3005 and CA3006, given in Fig. 140, show that these circuits are very good limiting amplifiers. A comparison of the curves in Fig. 140 with those given for the CA3004 in Fig. 139 emphasizes the excellent limiting characteristics of the CA3005 and CA3006.

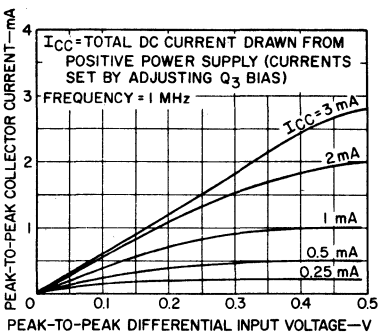


Fig. 139 — Dynamic transfer and limiting characteristics of the CA3004.

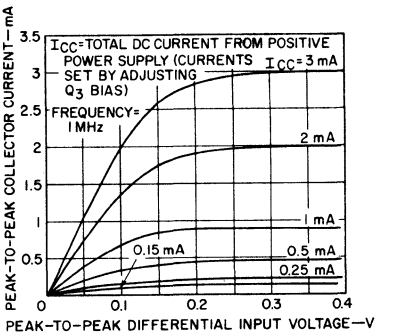


Fig. 140 — Dynamic transfer and limiting characteristics of the CA3005 or CA3006 operated in the differential-amplifier configuration.

Exceptional versatility in the operation of the CA3005, CA3006, and CA3028A is made possible by the availability of internal circuit points to which external circuit elements may be connected to alter the basic circuit configuration. As a result of such external modifications, it is possible to operate these circuits as push-pull amplifiers, as cascode amplifiers, or as single amplifiers in cascade or parallel channels.

The CA3005 and CA3006 rf amplifiers are identical except for their input offset voltages. The offset voltage for the CA3006 is typically less than 1 millivolt, while the offset voltage for the

CA3005 is normally in the order of 3 millivolts. The low level of input offset voltage makes the CA3006 well suited for balanced-modulator, mixer, or other push-pull applications that require a well-balanced circuit.

In the CA3028A rf amplifier, the temperature-compensating diodes (D_1 and D_2) used in the other rf amplifiers are omitted from the current-sink bias network, and only one value of emitter resistance is available for the current-sink transistor. As a result, this circuit does not provide the bias-circuit options that permit a choice of any one of four possible operating modes in the other rf amplifiers. (These operating modes are discussed in a subsequent paragraph.) The CA3028A circuit exhibits especially good performance characteristics when used in if amplifiers and in FM front ends as an rf amplifier, if amplifier, or converter.

Supply-Voltage Connections — Fig. 141 shows the supply-voltage connections for differential- and cascode-amplifier operation of the CA3005 or CA3006 from single and dual supplies. When two supplies, one for positive voltage and one for negative voltage, are used, as shown in Fig. 141(a) and 141(c), fewer external components are required. When only one supply is used, an external resistive voltage divider and bypass capacitor must be added to the circuit, as shown in Figs. 141(b) and 141(d). Tuned amplifiers that operate from dual supplies, such as that shown in Fig. 141(a), require the least number of external components.

For either single- or dual-supply operation, the operating current of transistor Q_3 is determined by the bias voltage, V_{EE}, applied between terminals 2 and 3 on the CA3004 or between terminals 8 and 12 on the CA3005 and CA3006 (refer to the circuit diagrams in Fig. 138). The more negative terminal of the bias-voltage source must be connected to terminal 3 on the CA3004 or to terminal 8 on the CA3005 and CA3006. In dual-supply systems, terminal 2 of the CA3004 and terminal 12 of the CA3005 and CA3006 are usually returned to dc ground.

Fig. 142 shows the supply-voltage connections for several operating arrangements of the CA3028A. Connections are shown for a differential amplifier that has agc capability; a cascode amplifier with a constant-impedance or conventional agc capability; a converter; a mixer; and an oscillator. Cascode operation of the CA3028A is preferred for applications that require high gain. The differential-amplifier configuration is preferred when good limiting is required.

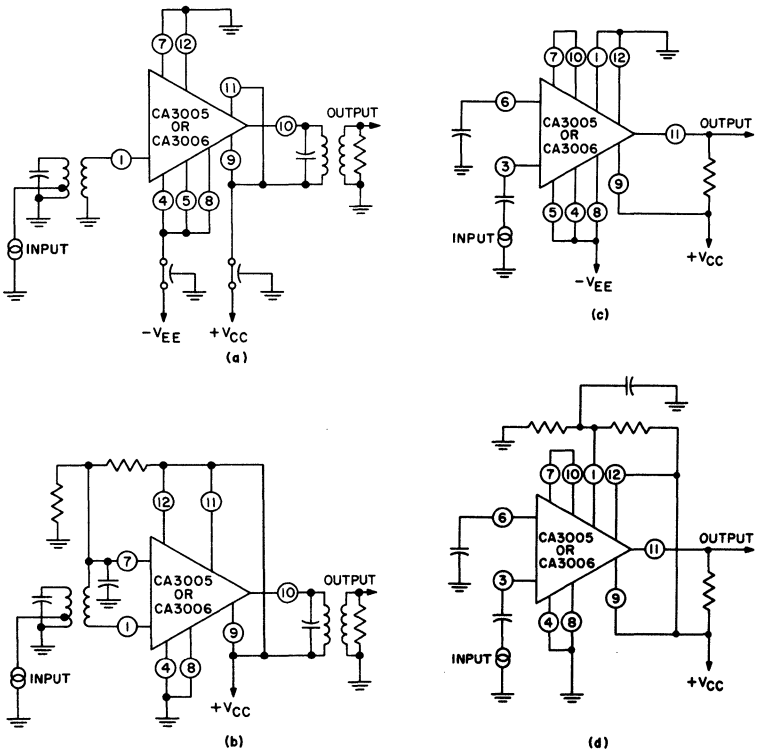


Fig. 141 — Supply-voltage connections for the CA3005 or CA3006 in (a) a differential-amplifier configuration operated from dual supplies, (b) a differential-amplifier configuration operated from a single supply, (c) a cascode configuration operated from dual supplies, and (d) a cascode configuration operation from a single supply.

Operating Modes — For any given bias voltage V_{EE}, there are four possible operating modes for the CA3004, CA3005, and CA3006 integrated-circuit rf amplifiers. In general, each mode is characterized by (1) a distinct level of operating current and corresponding transconductance, (2) the degree of dependence of the operating current on temperature, and (3) the way in which the transconductance is affected by temperature. The operating points for the various modes are established by:

1. The emitter resistance selected for the constant-current-source transistor, Q_3;
2. Whether the base-bias network includes the diodes shown in Fig. 138;
3. The magnitude of the bias voltage, V_{EE}, applied to the circuit.

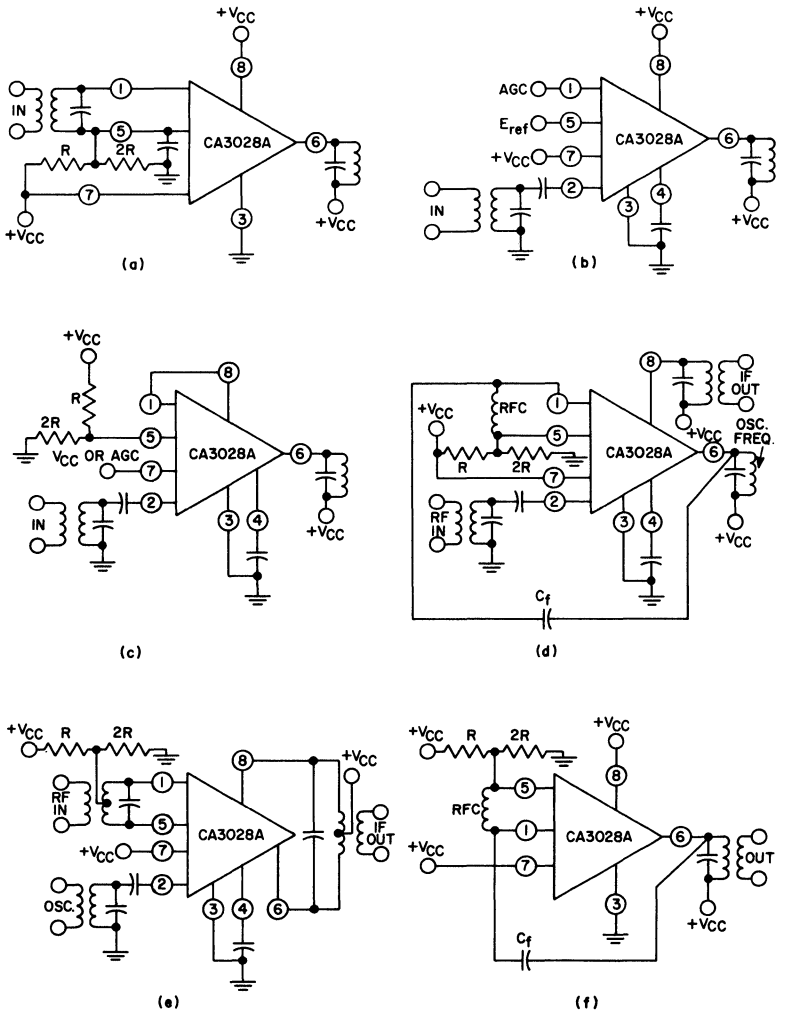


Fig. 142 — Connections for the CA3028A for use as (a) a balanced differential amplifier with a controlled constant-current-source drive and agc capability, (b) a cascode amplifier with a constant-impedance agc capability, (c) a cascode amplifier with conventional agc capability, (d) a converter, (e) a mixer, and (f) an oscillator.

As pointed out previously, the CA3028A is designed for only one mode of operation. This circuit, however, is very similar to the CA3005 operated in mode C. For operation at the same dc supply-voltage levels, the operating current, transconductance character-

istics, and temperature dependence of the CA3028A are essentially the same as those of the CA3005 in mode C.

Table XVIII lists the required conditions for the four operating modes of the CA3004, CA3005, and CA3006 integrated-circuit rf amplifiers. The following paragraphs describe the characteristics

Table XVIII—*Required Conditions for Each Operating Mode of the CA3004, CA3005, and CA3006 Integrated-Circuit RF Amplifiers*

Operating Mode*	CA3004 Terminals Shorted to Term. 3	CA3005 or CA3006 Terminals Shorted to Term. 8	Diodes In or Out of Bias Circuit	Q-3 Emitter Resistor(s)
A	—	—	In	$R_4 + R_5$
B	5	4	Out	$R_4 + R_5$
C	4	5	In	R_5
D	4,5	4,5	Out	R_5

* For all modes, terminals 2, 6, and 12 of the CA3004 and terminals 1, 7, and 12 of the CA3005 and CA3006 are grounded.

of the circuits in each operating mode. The data are given for operation of the circuits from symmetrical dual power supplies at three levels of dc supply voltage (±3 volts, ±4.5 volts, and ±6 volts).

Fig. 143 shows the operating current for the various modes as a function of temperature. The current-temperature data show that, in addition to the obvious shift in the level of operating current, the dependence of the operating current on temperature varies significantly with a change in the operating mode.

When the diodes are included in the base-bias circuit (modes A and C), the operating current, which is primarily dependent on the temperature coefficient of the diffused emitter resistor, tends to decrease with an increase in temperature at a rate that is relatively independent of the bias supply voltage V_{EE}. When the diodes are not used, however, the shape of the current-temperature curves is dependent on the magnitude of the supply voltage V_{EE}. The operating current then may remain constant or rise as the temperature is increased, depending upon the value of V_{EE}. The positive supply voltages, shown in Fig. 143, have no effect on the operating current, and the current-temperature curves are not changed by increases or decreases in this voltage. Some deviation in the current-temperature curves is to be expected because of normal variations in the absolute resistor values.

Fig. 144 shows the effects of different operating modes and variations in temperature on the single-ended transconductance* of

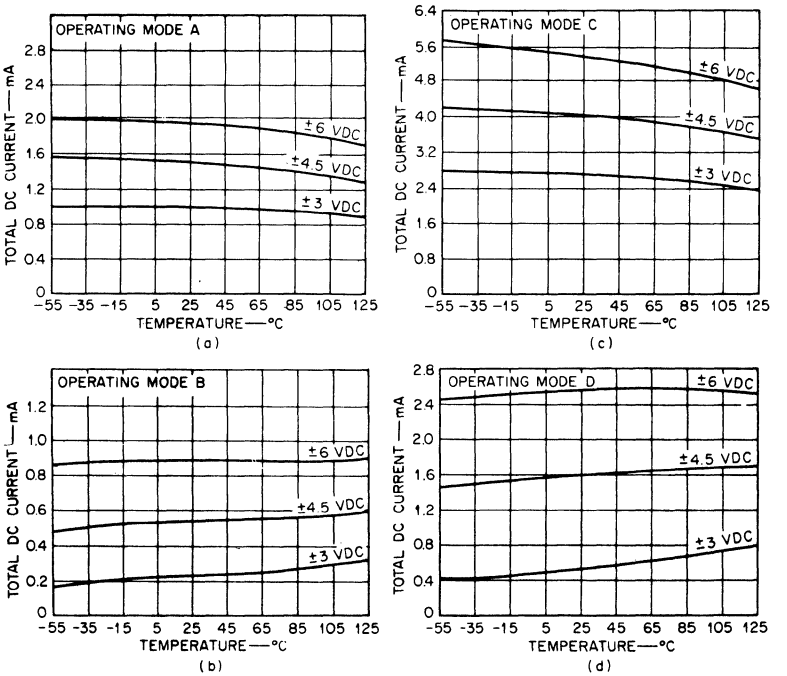


Fig. 143 — Operating current of the CA3004, CA3005, or CA3006 as a function of temperature for each operating mode.

the CA3004. In general, when diodes are used in the base-bias network, the transconductance decreases with increases in temperature. If the diodes are not used, the transconductance may decrease, increase, or remain constant as the temperature increases, depending on the value of the negative supply voltage V_{EE}. With the diodes out, however, the collector operating point tends to shift when resistive loads are used. In applications that require a stable collector dc operating point, therefore, operating mode A or C (diodes in) should be used.

Fig. 145 shows transconductance-temperature curves for each operating mode of the CA3005 or CA3006, operated in a differential-amplifier configuration. These transconductance curves differ from those for the CA3004 shown in Fig. 144 primarily because of the emitter resistors used in the CA3004. For each operating mode, the operating points for the differential-amplifier configura-

* The single-ended transconductance is the incremental output current for one collector of the differential pair of transistors divided by the incremental input voltage. The curves shown of this parameter are obtained at an operating frequency of 1 MHz.

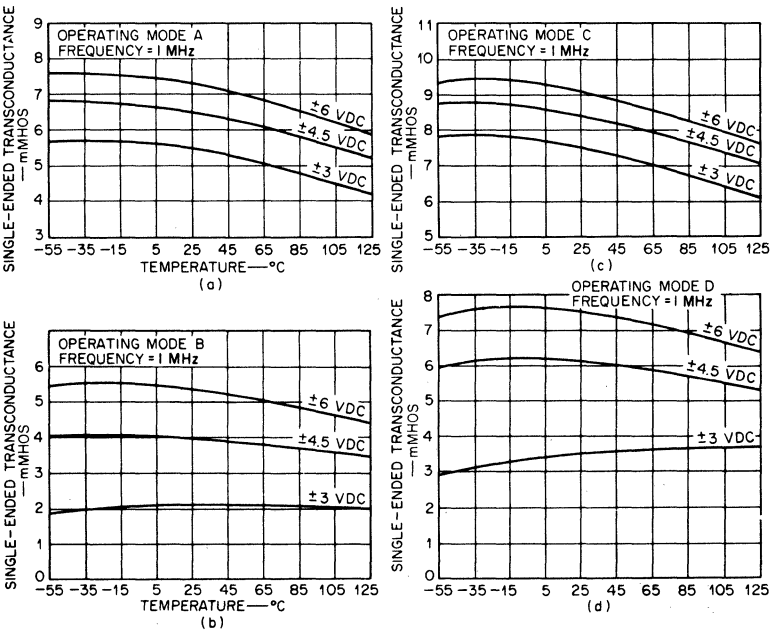


Fig. 144 — Single-ended transconductance of the CA3004 as a function of temperature for each operating mode.

tion of the CA3005 or CA3006, as well as for the CA3004, provide a current in each collector of the differential pair of transistors that is equal to one-half that shown in Fig. 143.

In a cascode configuration of the CA3005 or CA3006, the current through each part of the common emitter-common base cascode is equal to the total current shown in Fig. 143 in each mode. Fig. 146 shows the transconductance-temperature curves for each operating mode of the cascode circuit. These curves show that, in general, the transconductance is higher when the diodes are included in the base-bias network (modes A and C) than it is when the diodes are not used (modes B and D).

The power dissipation of the CA3004, CA3005, or CA3006 is highest when the circuit is operated in mode C. Table XIX shows power dissipation and the single-ended transconductance of the circuits for each operating mode. These data may be used to determine the operating point that provides the highest value of transconductance per milliwatt of circuit dissipation for given design conditions.

Admittance Parameters — In the design of rf and if circuits, the four-terminal blackbox short-circuit admittance parameters

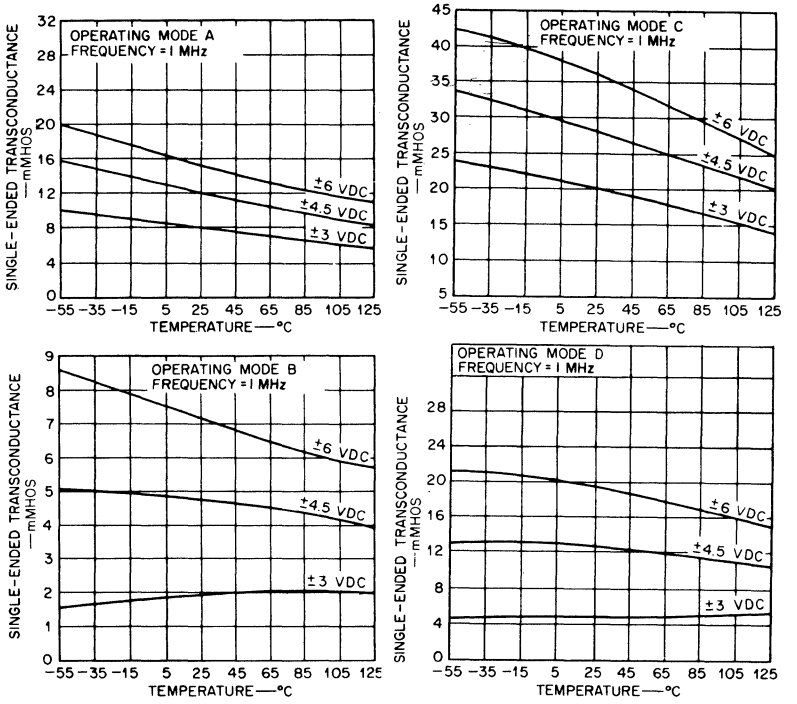


Fig. 145 — Single-ended transconductance of the CA3005 or CA3006 in a differential-amplifier configuration as a function of temperature for each operating mode.

have become a valuable tool. The determination of stability criteria, input and output impedances as a function of load and source admittance, power gain, and voltage gain in iterative connections are all facilitated by a knowledge of the "y" parameters.

The "y" parameter curves presented in this section have been calculated from a model and verified at several points by measurements. These curves are a valuable aid in the design of systems that use integrated circuits. For the CA3004, CA3005, and CA3006 circuits, the admittance curves are all generated for a quiescent operating current of 1.25 milliamperes in each of the transistors Q_1 and Q_2 in the differential-amplifier configurations and for a current of 2.5 milliamperes in transistor Q_3 in the cascode configuration. This operating current is obtained in operating mode D with supply voltages of ± 6 volts. For the CA3028A circuit, the admittance curves are generated for a quiescent current of 2.2 milliamperes in each differential-pair transistor in the differential-amplifier configuration and for a current of 4.5 milliamperes in transistor Q_3 in

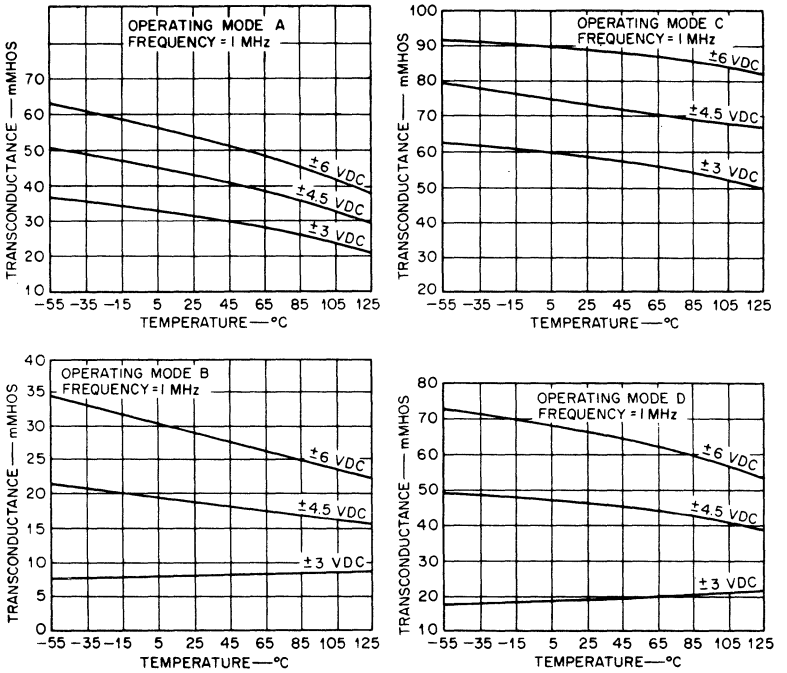


Fig. 146 — Transconductance of the CA3005 or CA3006 in a cascode configuration as a function of temperature for each operating mode.

the cascode configuration. The operating current in the CA3028A is obtained with a supply voltage of 9 volts.

The "y" parameters and their symbols are listed below:

1. Input admittance with the output voltage constant

$$y_i = g_i + jb_i \tag{183}$$

where y_i is the complex input admittance, g_i is the input conductance and b_i is the input susceptance.

2. Output admittance with the input voltage constant

$$y_o = g_o + jb_o \tag{184}$$

where y_o is the complex output admittance, g_o is the output conductance, and b_o is the output susceptance.

3. Forward-transfer admittance with the output voltage constant

$$y_f = g_f + jb_f \tag{185}$$

where y_f is the complex forward-transfer admittance, g_f is the

forward-transfer conductance, and b_f is the forward-transfer susceptance.

4. Reverse-transfer admittance with the input voltage constant

$$y_r = g_r + jb_r \tag{186}$$

Table XIX—*Relationship Between the Transconductance and the Power Dissipation of the Integrated-Circuit RF Amplifiers in Each Operating Mode**

Operating Mode	Type of Circuit	DC Supply Voltages (volts)	Single-Ended Transconductance (millimhos)†	Power Dissipation (milliwatts)†
A	CA3004	±3	5.5	6.5
	CA3005 or CA3006		8.5	6.6
	CA3004	±4.5	6.7	15.0
	CA3005 or CA3006		12.8	15.0
	CA3004	±6	7.3	25.0
	CA3005 or CA3006		15.0	25.0
B	CA3004	±3	1.6	2.3
	CA3005 or CA3006		1.9	2.3
	CA3004	±4.5	4.0	7.2
	CA3005 or CA3006		4.9	7.2
	CA3004	±6	5.3	15.0
	CA3005 or CA3006		7.2	15.0
C	CA3004	±3	7.5	17.5
	CA3005 or CA3006		22.0	17.5
	CA3004	±4.5	8.5	40.0
	CA3005 or CA3006		29.0	40.0
	CA3004	±6	9.1	62.8
	CA3005 or CA3006		37.0	62.8
D	CA3004	±3	3.3	4.2
	CA3005 or CA3006		5.0	4.2
	CA3004	±4.5	6.0	17.4
	CA3005 or CA3006		13.0	17.4
	CA3004	±6	7.2	35.9
	CA3005 or CA3006		20.0	35.9

* Circuits are operated in differential-amplifier configurations. The transconductances and power dissipations shown are calculated values for nominal units.

† For operation at the same supply-voltage levels, transconductance and dissipation of the CA3028A are the same as those of the CA3005 operated in mode C.

where y_r is the complex reverse-transfer admittance, g_r is the reverse-transfer conductance, and b_r is the reverse-transfer susceptance.

A comparison of the parameters of the various possible circuit configurations with those of the more familiar common-emitter parameters requires a second subscript to indicate the type of configuration being considered. Examples of the use of the second-subscript notation are given below:

The common-emitter reverse-transfer admittance is written as

$$y_{re} = g_{re} + jb_{re} \tag{187}$$

The differential-amplifier reverse-transfer admittance is expressed as

$$y_{rDA} = g_{rDA} + jb_{rDA} \tag{188}$$

The cascode-amplifier reverse-transfer admittance is given as

$$y_{rCAS} = g_{rCAS} + jb_{rCAS} \tag{189}$$

These cumbersome second subscripts will not be used when the type of circuit for which the parameter is given is clearly indicated by an illustration or a descriptive phrase in the text.

In general, it is valuable to understand the essential differences between the "y" parameters of a regular common-emitter stage and those of the compound stages, such as differential and cascode amplifiers.

The differential amplifier, when used at radio frequencies, consists essentially of a common-collector stage that drives a common-base stage. In comparison to the regular, common-emitter "y" parameters, the input admittance y_i, the output admittance y_o, and the forward transfer admittance y_f are decreased, almost exactly, by a factor of two when the differential-amplifier configuration is used.

The reverse-transfer admittance y_r is also less for the differential amplifier than for the single transistor in the common-emitter configuration. The ratio of the imaginary term in the differential-amplifier admittance to that of the single transistor is 1/140 at low frequencies and 1/10 at 100 MHz. Fig. 147 shows the ratios of imaginary parts b_{re}/b_{rDA} and real parts g_{re}/g_{rDA} of the reverse-transfer admittances as a function of frequency.

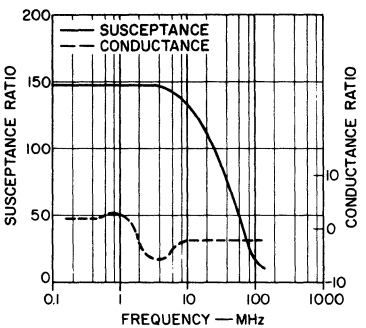


Fig. 147 — Ratio of real (conductance) and imaginary (susceptance) parts of the reverse-transfer admittance for a common-emitter stage to those for a differential-amplifier stage as a function of frequency.

In the cascode configuration of the rf amplifier circuits, a common-emitter stage drives a common-base stage. The input admittance y_i is, therefore, that of a common-emitter stage. The forward-transfer admittance y_f is that of a common-emitter stage times alpha. Because of the high-impedance drive source on the common-base stage, the output admittance y_o is very low (0.06×10^{-5} mho) at low frequencies and is both negative and low at high frequencies. Since the output admittance is low and may be negative, a conjugate match cannot be obtained at the output. Practical amplifiers are possible, however, provided that the sum $Y_{out} + Y_{load}$ is positive.

The reverse-transfer admittance y_r for the cascode circuit is less than that for the single-stage common-emitter circuit. The ratio of the imaginary terms of these admittances is 1/1200 at low frequencies and 1/35 at 100 MHz. The ratios of the real parts and of the imaginary parts as a function of frequency are shown in Fig. 148.

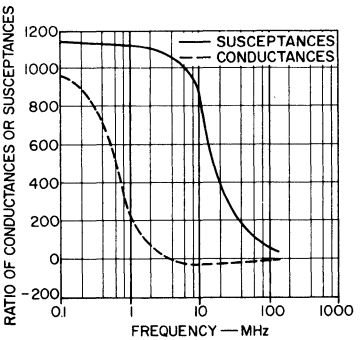


Fig. 148 — Ratio of real (conductance) and imaginary (susceptance) parts of the reverse-transfer admittance for a common-emitter stage to those for a cascode stage as a function of frequency.

Although the y_r is low for both the differential and cascode configurations, instability can occur in high-gain amplifiers. A further consideration in high-gain circuits is that the layout can contribute more feedback than the integrated circuit. Shielding and layout therefore are of prime importance if proper advantage is to be taken of the low feedback of these circuits.

The computed y parameters for the CA3004 differential amplifier are shown in Fig. 149. The admittance parameters for differential-amplifier operation of the CA3005 or CA3006 are given in

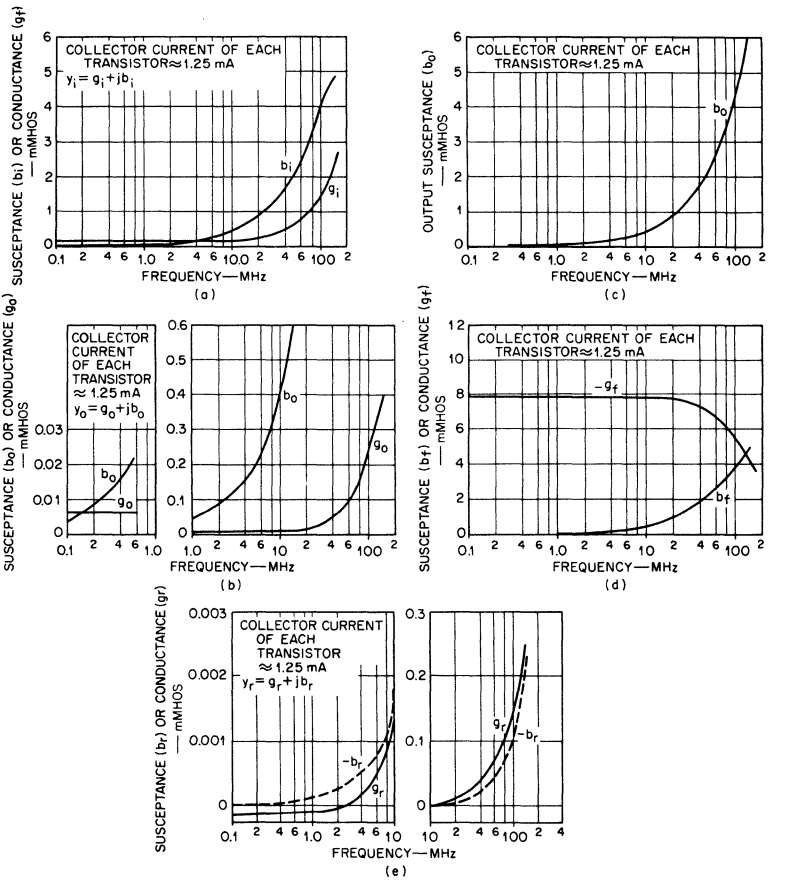


Fig. 149 — Admittance parameters of the CA3004 differential amplifier as a function of frequency.

Fig. 150 and those for cascode-amplifier operation of either circuit are given in Fig. 151. The y parameters for the CA3028A are shown in Figs. 152 and 153 for the differential-amplifier and cascode configurations, respectively.

Noise Figure — The noise figure of the CA3004, CA3005, and CA3006 integrated-circuit rf amplifiers is a function of the dc operating current and frequency, for both differential and cascode-amplifier configurations. The noise figure increases both with an increase in current and with an increase in frequency. For convenience, noise data are taken in a fixed configuration as the negative supply voltage is varied. On the data plots, the operating currents that correspond to the various supply voltages are in-

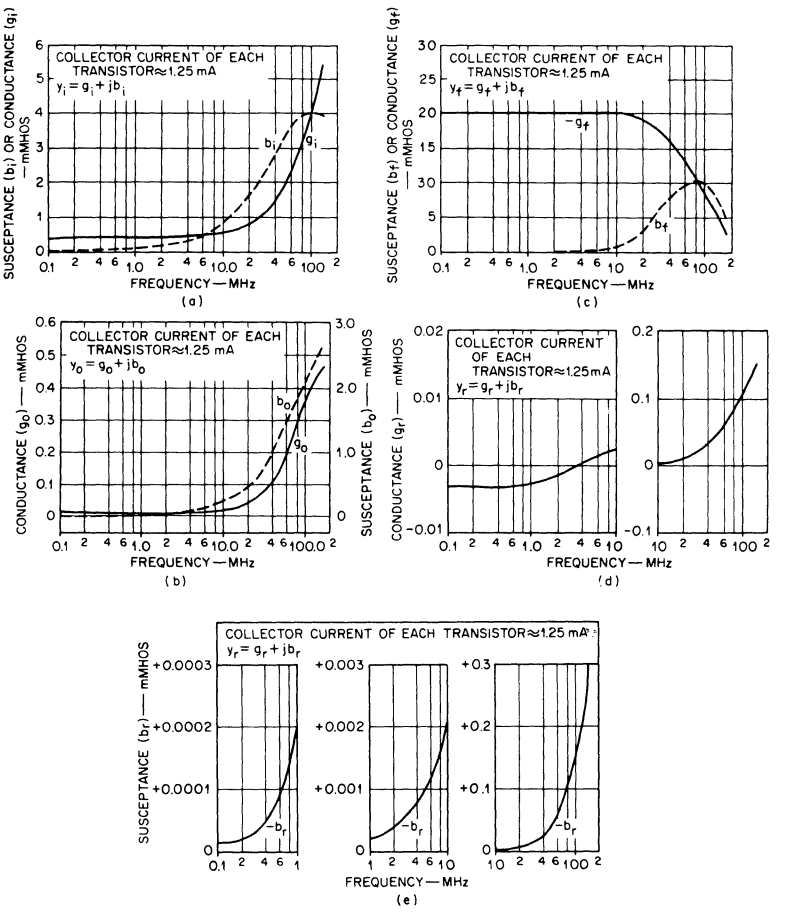


Fig. 150 — Admittance parameters of a CA3005 or CA3006 differential amplifier as a function of frequency.

cluded as a separate abscissa to show that the noise figure is a direct function of operating current. Figs. 154 and 155 show representative noise-figure data for tuned amplifiers in the differential and cascode configuration, respectively. In each case, the input and output are tuned, and the input is conjugately matched to a 50-ohm noise diode. Practically no change in noise figure occurs with variations of the positive supply voltage V_{CC}.

The curves in Figs. 154 and 155 show that, for optimum single-stage noise performance, the operating current should be low, which results in a low gain. Thus, in system applications of the tuned amplifiers, the operating current in each stage should

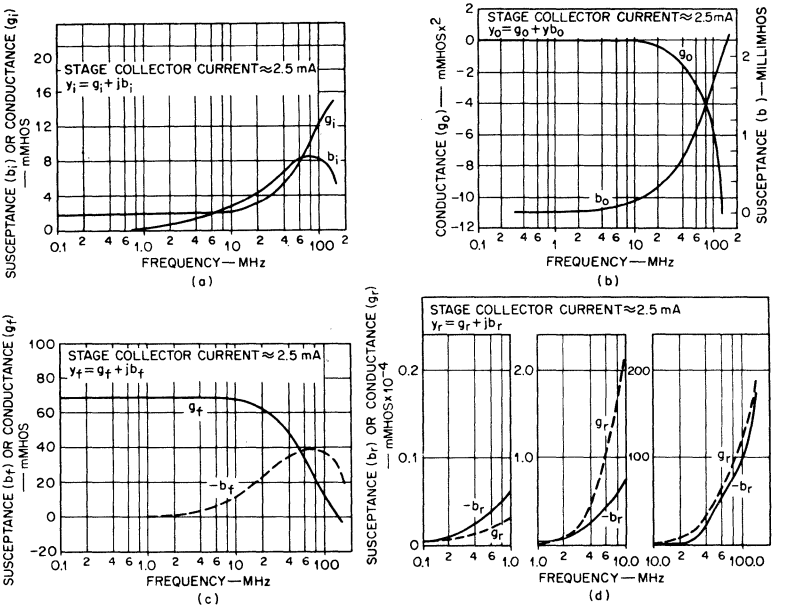


Fig. 151 — Admittance parameters of a CA3005 or CA3006 cascode amplifier as a function of frequency.

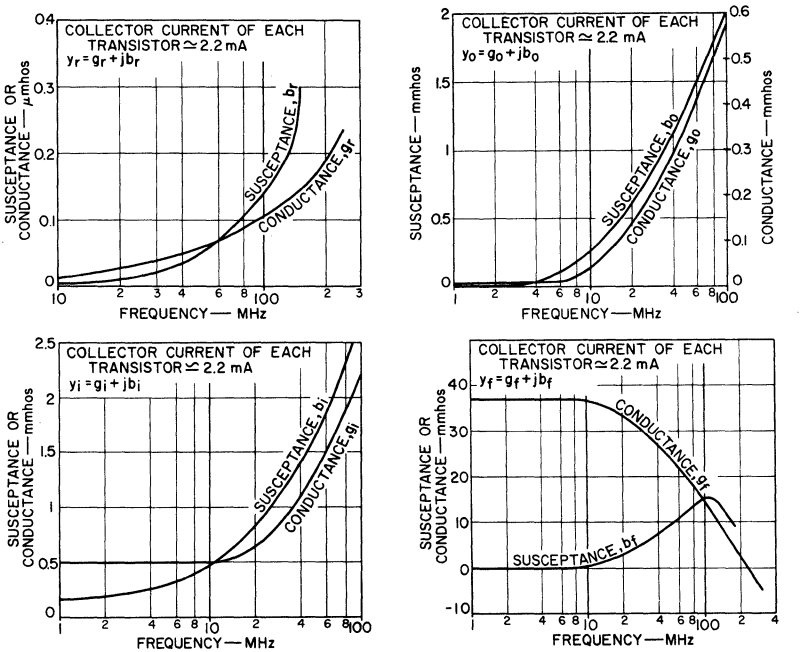


Fig. 152 — Admittance parameters of a CA3028A differential amplifier as a function of frequency.

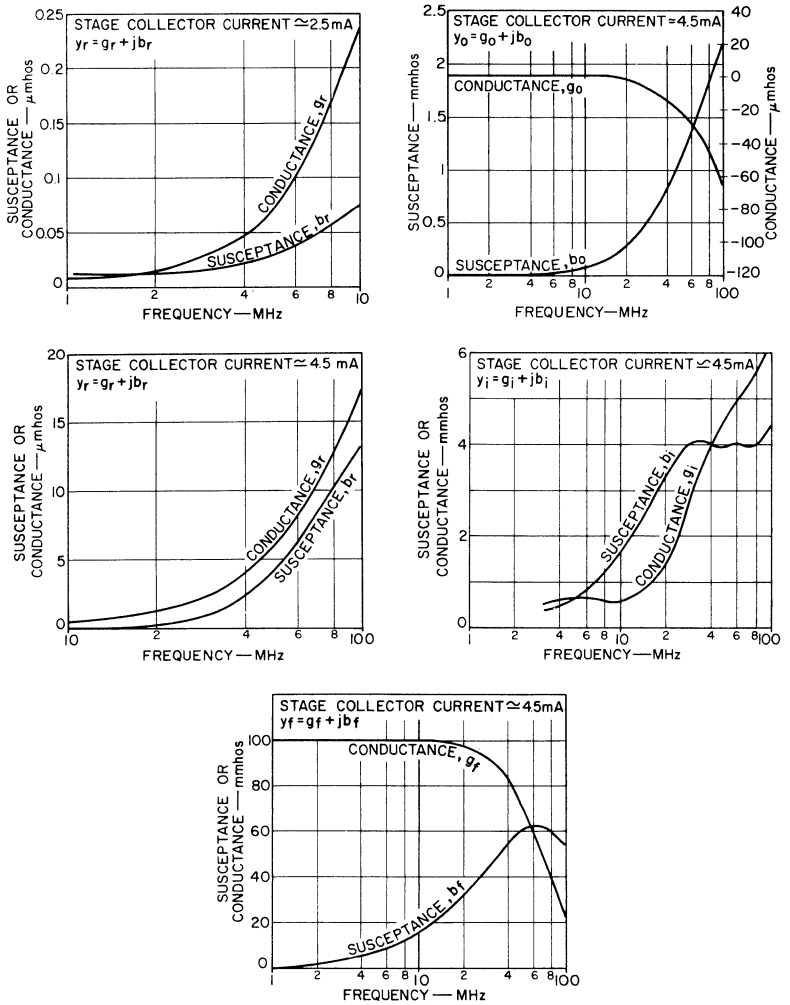


Fig. 153 — Admittance parameters of a CA3028A cascode amplifier as a function of frequency.

be adjusted to obtain the optimum over-all noise figure by considering the gain and noise figure of the first stage and the noise figure of the second stage. The operating-current adjustment can be accomplished by a change in the negative-supply voltage (V_{EE}) or by means of the bias connections that are available.

Fig. 156 shows the noise figure as a function of the source resistance for a CA3005 or CA3006 used as a differential amplifier at an operating frequency of 12 MHz. The equation given in

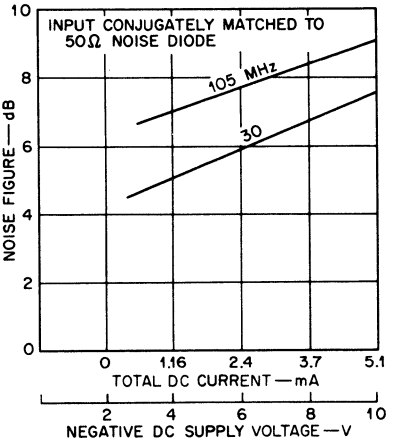


Fig. 154 — Representative noise performance of the CA3004, CA3005, or CA3006 operated in a differential-amplifier configuration (operating mode D).

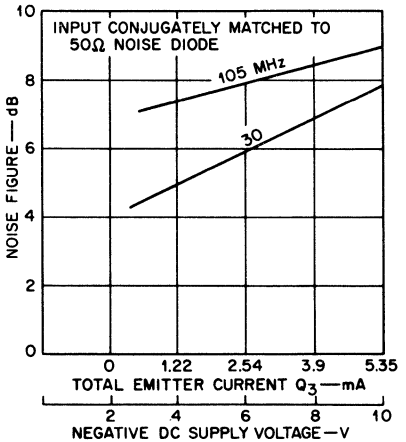


Fig. 155 — Representative noise performance of the CA3005 or CA3006 operated in a cascode configuration (operating mode D).

the figure can be used to predict noise performance as a function of source resistance for dc operating conditions. The load resistor R_L of the circuit is 2200 ohms and R_N = 800 ohms. (R_N is the equivalent noise resistance.)

Common-Mode Rejection Ratio — The common-mode rejection ratio (the ratio between the full differential gain and the common-mode gain) is a function of the ratio of the impedance

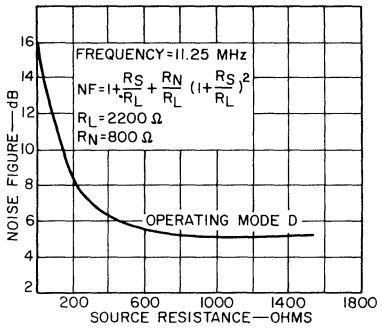


Fig. 156 — Noise figure of the CA3005 or CA3006 in a differential-amplifier configuration as a function of source resistance (operating mode D).

of the constant-current transistor Q_3 to the load resistor. The common-mode rejection decreases if the signal applied is large enough to saturate the constant-current transistor. The maximum peak-to-peak input voltage, therefore, is a function of the supply voltages and the bias connections of the constant-current transistor. The common-mode rejection ratio for a 1-kHz signal is shown in Table XX.

Fig. 157 shows the single-ended common-mode gain* for the integrated-circuit rf amplifiers as a function of frequency. (Fig.

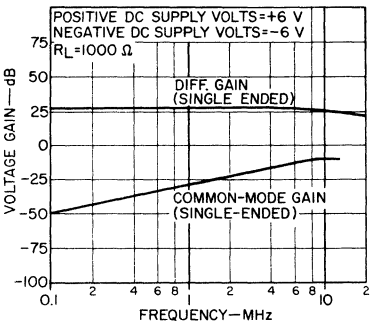


Fig. 157 — Single-ended common-mode and differential gains of the CA3004, CA3005, or CA3006 as a function of frequency.

* Single-ended common-mode gain: The ratio of the change in the single-ended output voltage, measured from either output terminal with respect to ground, to the change in the input voltage applied simultaneously to both inputs of the circuit, i.e., single-ended common-mode gain = $\triangle V_{in}/\triangle V_{out}$, as shown in Fig. 158.

158 shows the method used to determine the single-ended common-mode gain.) The common-mode rejection decreases with increasing frequency when the rf amplifiers are operated with a single-ended output.

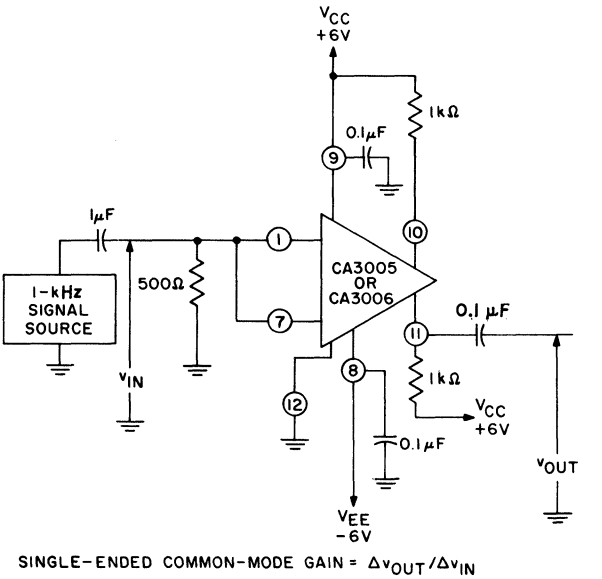


Fig. 158 — Test circuit used to determine single-ended common-mode gain.

Table XX—*Common-Mode Rejection Ratio for the CA3004, CA3005, and CA3006 Integrated-Circuit RF Amplifiers*

	At —55°C	At 25°C	At 125°C
CA3004	102 dB	98 dB	101 dB
CA3005 or CA3006	108 dB	101 dB	107 dB

Operating frequency = 1 kHz
Load resistance R_L = 1000 ohms in each collector.

Gain Control — The gain of the CA3004, CA3005, and CA3006 circuits may be controlled in either of two ways: (1) the negative voltage applied to the base-bias resistor R_1 can be adjusted to vary the current in transistor Q_3, or (2) a differential offset voltage can be applied to transistors Q_1 and Q_2. In both techniques, the gain-control voltage has a ground reference in a two-supply system, and maximum gain is obtained at zero volts. The first method provides greater gain-control range but also requires more control voltage than the second method. Figs. 159

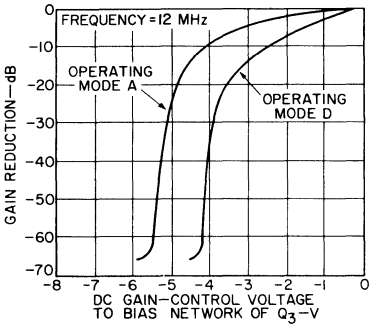


Fig. 159 — Gain-control characteristics of the CA3005 or CA3006 as a function of the dc gain-control voltage applied to the bias network of transistor Q_3.

and 160 show the typical gain control as a function of voltage for the CA3005 or CA3006 for the two methods. Fig. 159 gives the gain-control characteristic for the CA3005 or CA3006 when the gain-control voltage is applied to the base-bias network of transistor Q_3. Since the Q_3 bias networks are the same, the gain characteristics for the CA3004 are nearly the same as those for the CA3005 and CA3006. Fig. 160 shows that in the offset method of gain control the gain range is dependent on the polarity of drive.

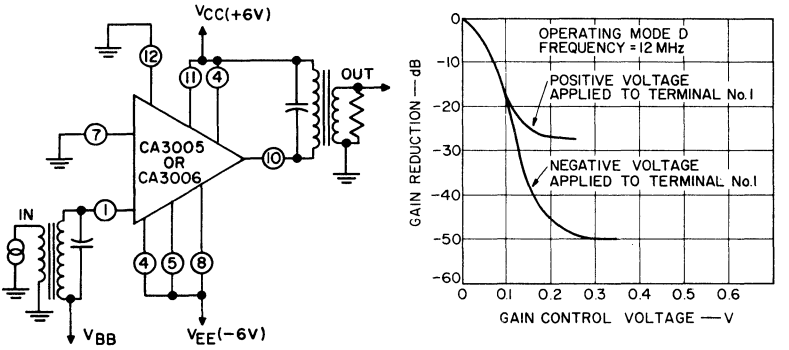


Fig. 160 — Gain control characteristics of the CA3005 or CA3006 as a function of the dc offset voltage V_{BB} applied to the differential pair of transistors Q_1 and Q_2.

For maximum gain-control range on a single-ended amplifier, the common-collector transistor should be cut off (negative voltage applied to its base). Because of the emitter resistors, R_6 and R_7, the CA3004 circuit will require more dc voltage for the same gain reduction as the CA3005 or CA3006, and the dc voltage required will be a function of the initial operating current.

The maximum gain-control range that can be provided by a reduction in the current of transistor Q_3 varies with frequency as shown in Fig. 161. The maximum gain-control range that can be obtained is dependent on the full gain used, the circuit loading, and the external-circuit layout.

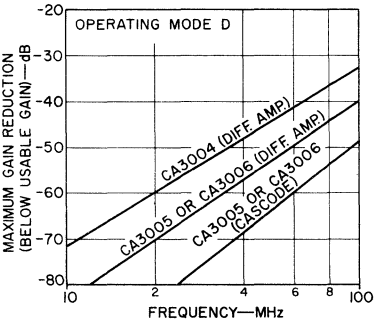


Fig 161 — Maximum gain control provided by variations in the current through transistor Q_3 as a function of frequency.

A large part of the variation in the maximum gain control for the different circuits results from differences in the initial gain of the various circuits. Capacitive feedthrough appears less for the cascode than for the differential-amplifier configuration.

In the CA3028A, gain control is achieved by application of a positive voltage to the base (terminal 7) of the constant-current-source transistor Q_3. A CA3028A operated in a differential-amplifier configuration, such as that shown in Fig. 142(a), can provide linear operation over a very wide input range with an agc voltage applied to terminal 7. As shown in Fig. 162(a), the CA3028A operated in a differential-amplifier circuit has a gain-control capability of — 60 dB at 10.7 MHz and of — 46 dB at 100 MHz. Fig. 162(b) shows the power gain and noise figure of the circuit as a function of agc voltage. The combination of an optimum noise figure of 5.5 dB and a power gain of 15 dB at 100 MHz makes this circuit suitable for use as an rf amplifier in the commercial FM band.

Cross-Modulation and Modulation Distortion — Cross-modulation and modulation distortion are important considerations in the selection of an amplifier for use in AM systems. Cross-modulation distortion refers to the transfer of modulation from an undesired carrier to the desired carrier by nonlinearities in the amplifier. Modulation distortion is a change in the modulation on the desired carrier caused by the same amplifier nonlinearities that

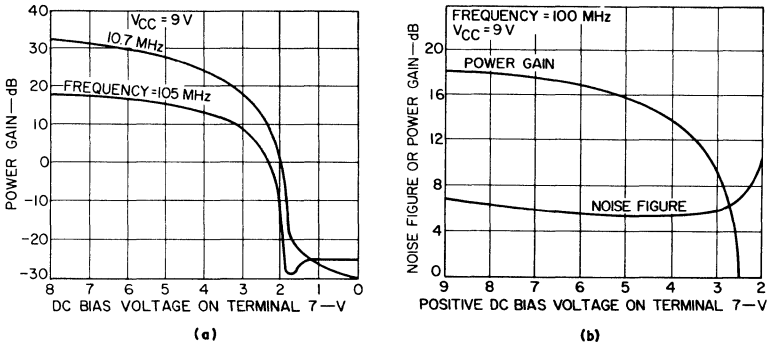


Fig. 162 — AGC characteristics of the CA3028A operated in a differential-amplifier configuration: (a) power gain as a function of agc voltage at 10.7 and 105 MHz; (b) power gain and noise figure as a function of agc voltage at 100 MHz.

produce cross-modulation. The two forms of distortion are related by the following equation:

$$\frac{D_2}{V_1^2} : \frac{K}{V_2^2} = \frac{3}{8} \text{ m} : 1 \qquad (190)$$

where D_2 is the per cent of distortion in the modulation on the desired carrier (i.e., the modulation distortion), K is the per cent of cross-modulation distortion, V_1 is the amplitude of the desired-carrier voltage at the input, V_2 is the amplitude of the undesired-carrier voltage at the input, and m is the per cent of modulation of the desired carrier.

When D_2 and K are equal and m is 100 per cent, the ratio of V_1 to V_2 is 1.64. In the following paragraphs, data are given for only the cross-modulation distortion. The modulation distortion can be predicted from these data, however, on the basis of the relationship of V_1 to V_2. For example, in Fig. 135, V_2 is given as 22 millivolts for a gain of 0 dB. The value of V_1, then, is 1.64×22, or 36 millivolts.

Figs. 163 through 167 show the cross-modulation distortion of the CA3004, CA3005, and CA3006 integrated circuits as a function of their gain-control characteristics in both differential-amplifier and cascode-amplifier configurations. (The cross-modulation characteristics of the CA3028A are essentially the same as those of the CA3005 and CA3006.) The amount of cross-modulation distortion is determined by the two-generator method with the input of the circuit under test driven from a 50-ohm source and with its output tuned to the frequency of the desired

carrier. The amplitude of the undesired-carrier input voltage is that necessary to produce 10 per cent cross-modulation distortion for each manually determined gain-control setting.

Differential-Amplifier Configurations — The availability of internal connection points makes possible several methods of gain control in differential-amplifier configurations of the CA3004, CA3005, and CA3006 circuits. Only two of these methods need be considered, however, to obtain an adequate evaluation of the cross-modulation characteristics. These include (1) the variation of the current in the constant-current transistor, Q_3, and (2) the use of an offset voltage to produce an unbalance in the differential pair of transistors, Q_1 and Q_2.

Fig. 163 shows the cross-modulation distortion characteristics of the CA3004, CA3005, and CA3006 with the differential pair of transistors balanced and with agc applied to the constant-current transistor. Because of the increased linearity that results

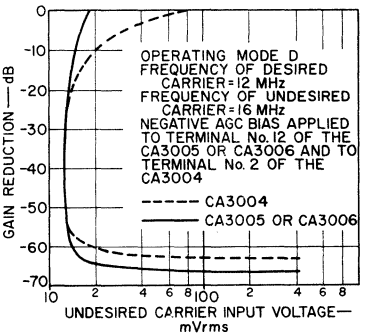


Fig. 163 — Gain control as a function of an undesired-carrier voltage that produces cross-modulation distortion of 10 per cent for balanced differential-amplifier operation of the CA3004, CA3005, and CA3006 when the gain-control voltage is applied to the bias network of the constant-current transistor Q_3.

from the emitter resistors R_6 and R_7, the CA3004 has improved cross-modulation characteristics at high current. The interfering signal voltage required to produce 10 per cent of cross-modulation distortion is practically a constant over the entire agc range for the CA3005 and CA3006. The value of the interfering-signal voltage (approximately 15 millivolts) for the CA3005 and CA3006 is twice that calculated from the logarithmic transconductance characteristic of a single transistor.

Fig. 164 shows the cross-modulation distortion characteristic of the CA3005 and CA3006 when an offset voltage is applied to

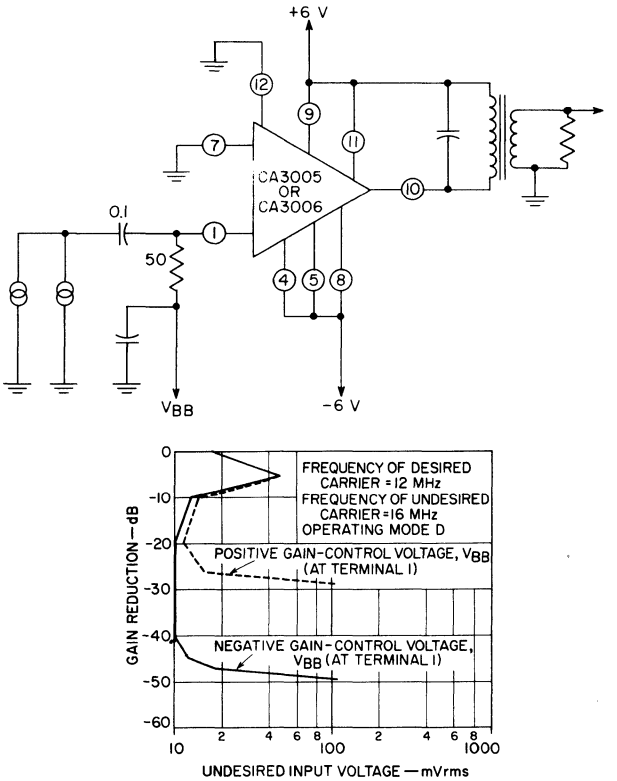


Fig. 164 — Gain control as a function of an undesired-carrier voltage that produces cross-modulation distortion of 10 per cent for balanced differential-amplifier operation of the CA3005 and CA3006 when gain control is provided by application of an offset voltage to the differential pair of transistors.

control the gain. The improved cross-modulation performance at −5 dB gain is coincident with an inflection point on the curve of transconductance as a function of input offset voltage. This point occurs at an offset voltage of approximately 50 millivolts.

The cross-modulation performance is improved by the offset of the differential pair of transistors. Fig. 165 shows the cross-modulation data when an initial offset of 50 millivolts is employed and agc is applied to the constant-current transistor. The introduction of the unbalance reduces the cross-modulation distortion to approximately 10 dB less than that of the balanced circuit. This reduction in cross-modulation distortion, however, is accompanied by a decrease in gain of approximately 5 dB.

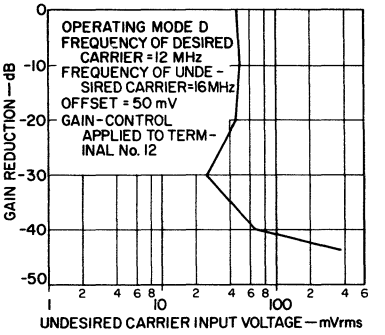


Fig. 165 — Gain control as a function of an undesired-carrier voltage that produces cross-modulation distortion of 10 per cent for a differential-amplifier configuration of the CA3005 or CA3006 having a 50-millivolt offset and with the gain-control voltage applied to the bias network of the constant-current transistor.

Cascode Configurations — Cross-modulation data for cascode configurations of the integrated-circuit rf amplifiers are given for only the CA3005 and CA3006 circuits, because the CA3004 circuit is not designed for this type of operation. When the CA3005 or CA3006 is operated in the cascode configuration, gain control may be provided by either of two methods: (1) a negative voltage may be applied to the base of transistor Q_3, or (2) a negative voltage may be applied to the base of transistor Q_1.

In the first method, the gain is reduced by the application of a negative-going voltage at terminal 12. As the amplitude of this voltage is increased to the value required to cut off transistor Q_3, the gain of the circuit is decreased. The cross-modulation distortion characteristics for this type of gain control are shown in Fig. 166. The cross-modulation characteristics are comparable to those of a single transistor having a bypassed emitter resistor.

The cross-modulation distortion characteristics obtained for the second method of gain control are shown in Fig. 167. No improvement in cross-modulation characteristics over those obtained for the first gain-control method are observed, although the agc range is greater.

Limiter Characteristics — The following paragraphs describe the limiter characteristics of the integrated-circuit rf amplifiers in both differential-amplifier and cascode configurations. (When the CA3028A is used for limiting, it should be operated in the differential-amplifier configuration.)

Differential-Amplifier Configurations — The differential-amplifier, driven by a constant-current transistor, is probably the

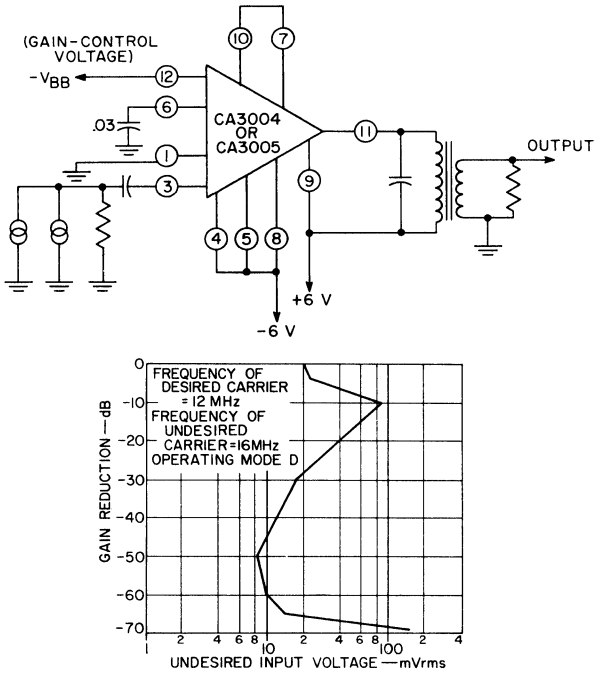


Fig. 166 — Gain control of the CA3005 or CA3006 in a cascode configuration as a function of an undesired-carrier voltage that produces cross-modulation distortion of 10 per cent when gain control is provided by a negative bias voltage applied to the base of transistor Q_3.

optimum circuit configuration for bipolar-transistor limiters. The advantage of such circuits in limiter applications is that collector saturation of either transistor Q_1 or Q_2 can be avoided because of the action of the constant-current transistor Q_3. Figs. 139 and 140 show typical limiting characteristics for the CA3004 and for the CA3005 and CA3006 respectively. Fig. 168 shows the limiting characteristics for the CA3028A. For the CA3005, CA3006, and CA3028A (no emitter degeneration), "hard" limiting is achieved for a peak-to-peak input of 300 millivolts for all values of total dc current (I_{CC}). For the CA3004, the input voltage required for "hard" limiting is a function of I_{CC} because of the linearizing effect of the degenerative emitter resistors, R_6 and R_7. As saturation must be prevented for good limiting, a maximum load resistor and low-level voltage gain exist for a given I_{CC} and positive supply voltage. Table XXI shows the maximum resistor values and voltage gains usable for $V_{CC} = 6$ volts, for the CA3004, CA3005, and CA3006. Table XXII shows the maximum permissible load resistance for nonsaturating operation of the CA3028A when single

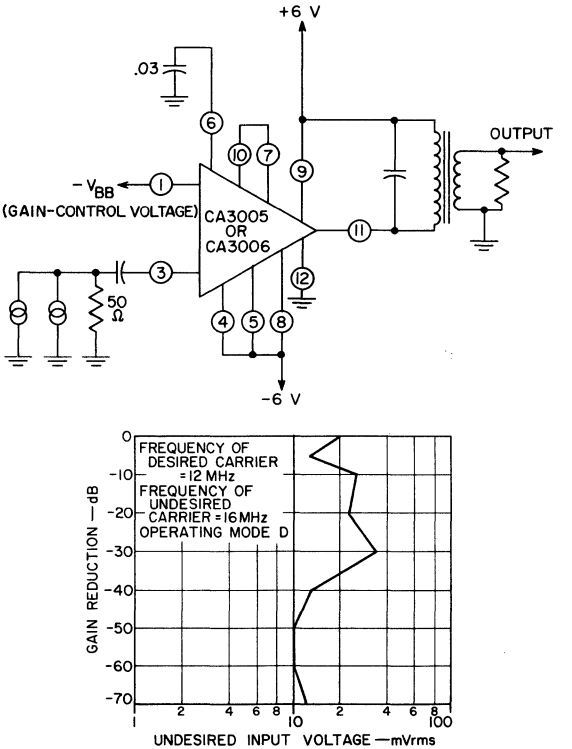


Fig. 167 — Gain control of the CA3005 or CA3006 in a cascode configuration as a function of an undesired-carrier voltage that produces cross-modulation distortion of 10 per cent when gain control is provided by a negative bias voltage applied to the base of transistor Q_1.

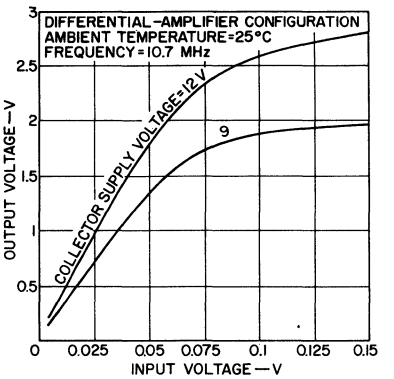


Fig. 168 — Limiting characteristics of the CA3028A operated in a differential-amplifier configuration.

supply voltages of 9 or 12 volts are used. The low-level transconductance can be obtained from the slope near the origin for the curves shown in Figs. 139 and 140. The maximum voltage gain is independent of I_{CC} in the CA3005 and CA3006 and is dependent on I_{CC} in the CA3004. Figs. 118 through 121 show the I_{CC} currents and transconductance for optional operating conditions.

Table XXI—*Limiter Performance of a Differential Amplifier*

Supply Volts	$I_{C_1}+I_{C_2}$ (mA)	Max. Resistive Load (ohms)	Max. Tuned Load (ohms)	Voltage Gain With Emitter Degeneration (dB)		Voltage Gain Without Emitter Degeneration (dB)	
				Resistive Load	Tuned Load	Resistive Load	Tuned Load
6	0.5	12000	24000	31	37	35	41
6	1.0	6000	12000	28	34	35	41
6	2.0	3000	6000	25	31	35	41
6	3.0	2000	4000	22	28	35	41

$R_L = \frac{V_{supply}}{I_{C_1}+I_{C_2}}$ Resistive Load; $R_L = \frac{2\,V_{supply}}{I_{C_1}+I_{C_2}}$ Tuned Load; $g_m R_L$ = voltage gain

Table XXII—*Maximum Load Resistance Permissible for Non-Saturating Operation with +9 and +12 Volt Single-Supply Voltages*

Supply Volts	$I_{C1}+I_{C2}$ (mA)	Maximum Tuned Load (ohms)	Maximum Resistive Load (ohms)
+9	5.0	3600	1800
+12	6.8	3500	1700

$R_L = V_{CC}/I_{C1} + I_{C2}$ Resistive Load
$R_L = 2\,V_{CC}/I_{C1} + I_{C2}$ Tuned Load

When the differential amplifier is used for limiting, the emitter-to-base breakdown voltage for transistors Q_1 and Q_2 cannot be exceeded without degradation in performance. For the CA3004, CA3005, and CA3006, this voltage including a safety margin should not exceed 2.5 volts rms. Either of two methods may be used to prevent this value being exceeded: (1) make sure the preceding stage limits before the input voltage reaches 2.5 volts (maximum voltage gain per stage approximately 20 dB), or (2) add one junction diode (D_1), as shown in Fig. 169 (this allows a maximum usable voltage gain consistent with good limiting and stability).

Cascode Amplifier — The limiting characteristics of the CA3005 or CA3006, when used as a cascode amplifier, are dependent on the current limiting in transistor Q_3 or the voltage limiting of transistor Q_1 (high-impedance output load). Limiting characteristics for both cases are shown in Figs. 170 and 171. The data in Fig. 170 are obtained with a collector load of 500 ohms.

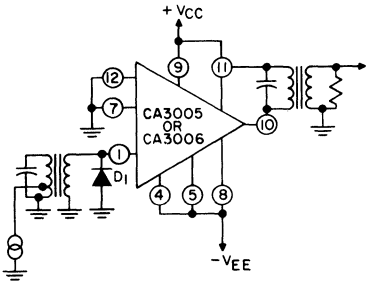


Fig. 169 — CA3005 or CA3006 differential-amplifier limiter that uses a diode to provide overload protection.

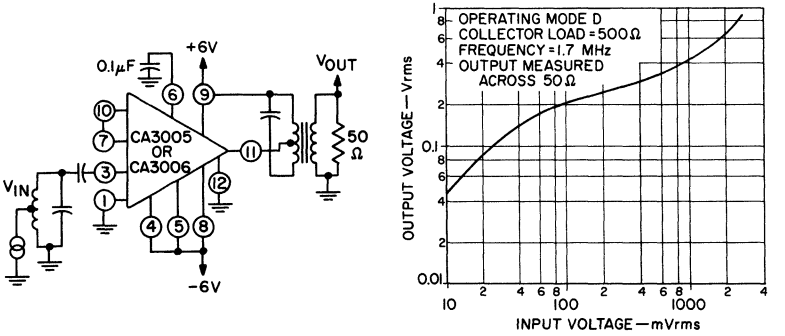


Fig. 170 — Limiting characteristics and circuit diagram of a CA3005 or CA3006 cascode limiter having a 500-ohm collector load impedance.

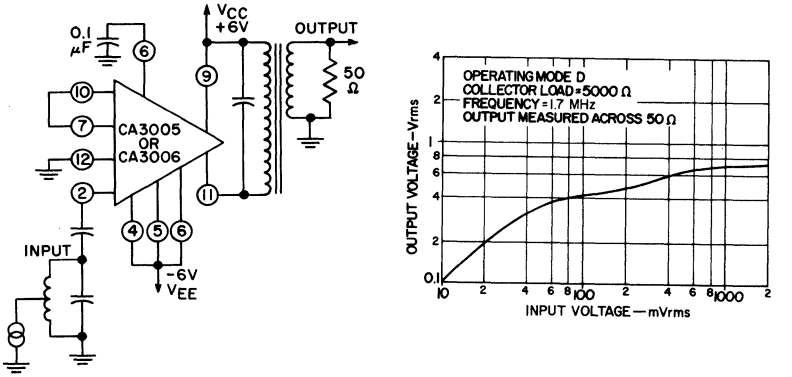


Fig. 171 — Limiting characteristics and circuit diagram of a CA3005 or CA3006 cascode limiter having a 5000-ohm collector load impedance.

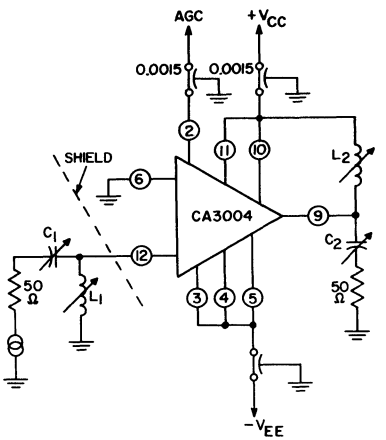
This limiting characteristic is "soft" and is acceptable over only a 20-dB range. The peak-to-peak voltage at the collector is never

large enough to cause saturation. The limiting characteristic shown in Fig. 171 is obtained with a collector load of 5000 ohms, and saturation of transistor Q_1 occurs. The limiting is harder and covers a broader range, but severe tuned-circuit loading occurs.

RF- and IF-Amplifier Capabilities

The typical applications described in the following paragraphs illustrate the use of the integrated-circuit rf amplifiers in both the differential and cascode modes.

RF and IF Amplifiers Using the CA3004, CA3005, and CA3006 — Figs 172, 173, and 174 illustrate the use of the CA3004, the CA3005 or CA3006 differential-amplifier configurations, and the CA3005 or CA3006 cascode configurations, respectively, as single-ended rf amplifiers. Adjustable matching networks,



Circuit Elements

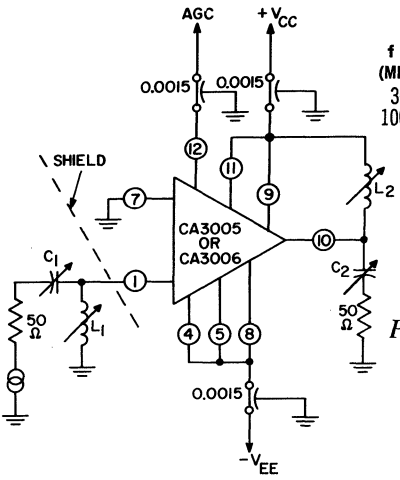
f (MHz)	L_1 (μH)	C_1 (pF)	L_2 (μH)	C_2 (pF)
30	1.8-2.7	2-10	1.8-2.7	2-10
.100	0.15-0.3	0.9-7	0.1-0.2	0.9-7

Power Gain Performance

DC SUPPLIES (volts)	POWER GAIN (dB) 30 MHz	100 MHz
±6	24	12

Fig. 172 — Test circuit used to evaluate rf-performance capabilities of CA3004.

derived from the y parameters, are included in each circuit. The values of the adjustable components, as well as typical power gains, are also shown in the figures. A conjugate match at the input is provided for all configurations. A conjugate match at the output is impossible for the cascode configuration (as pointed out in the



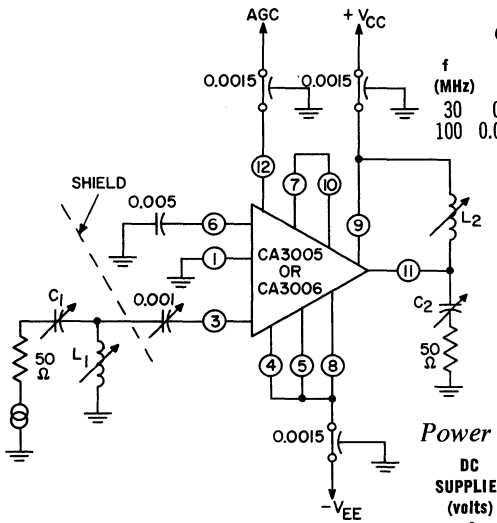
Circuit Elements

f (MHz)	L_1 (μH)	C_1 (pF)	L_2 (μH)	C_2 (pF)
30	1.2-2	5-40	1.2-2	1.5-20
100	0.4-0.7	1-12	0.25-0.5	1-12

Power Gain Performance

DC SUPPLIES (volts)	POWER GAIN (dB) 30 MHz	100 MHz
±6	29	18
±4.5	27.8	16
±3	23.0	11.5

Fig. 173 — Test circuit used to evaluate rf-performance capabilities of CA3005 or CA3006 in a differential-amplifier configuration.



Circuit Values

f (MHz)	L_1 (μH)	C_1 (pF)	L_2 (μH)	C_2 (pF)
30	0.3-0.6	14-150	0.8-1.4	5-40
100	0.07-0.12	5-40	0.15-.3	5-40

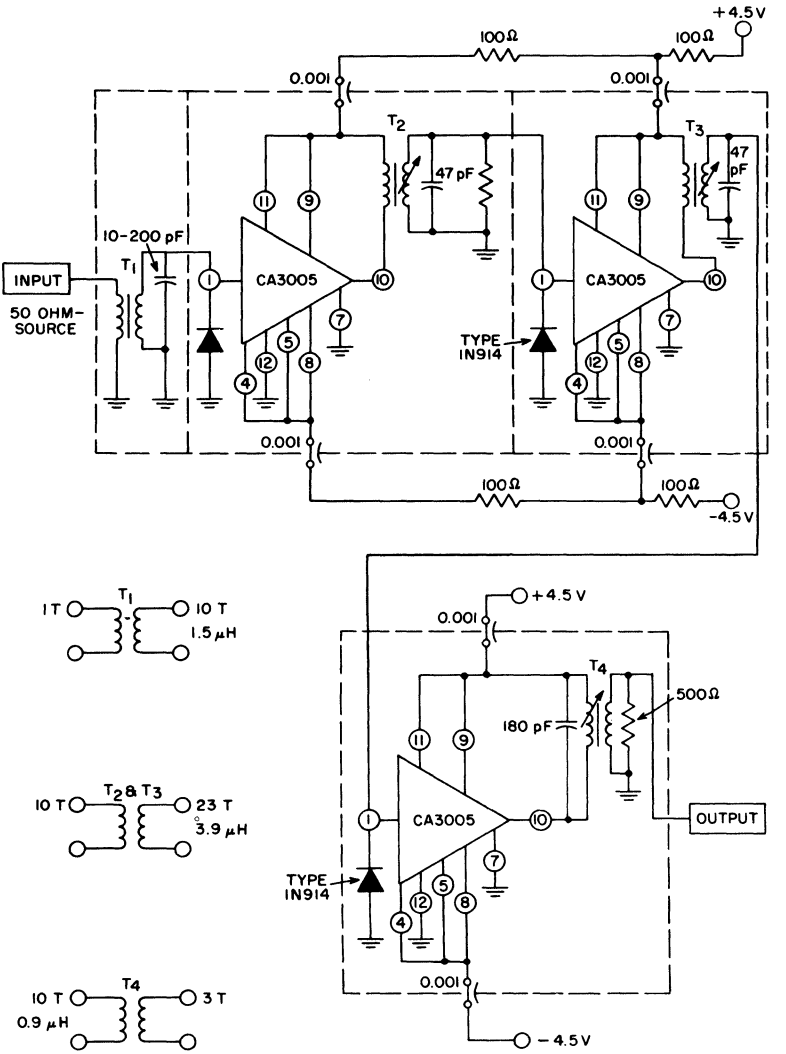
Power Gain Performance

DC SUPPLIES (volts)	POWER GAIN (dB) 30 MHz	100 MHz
±6	36	20
±4.5	33	18.5
±3	21.5	15.0

Fig. 174 — Test circuit used to evaluate rf-performance capabilities of a CA3005 or CA3006 in a cascode configuration.

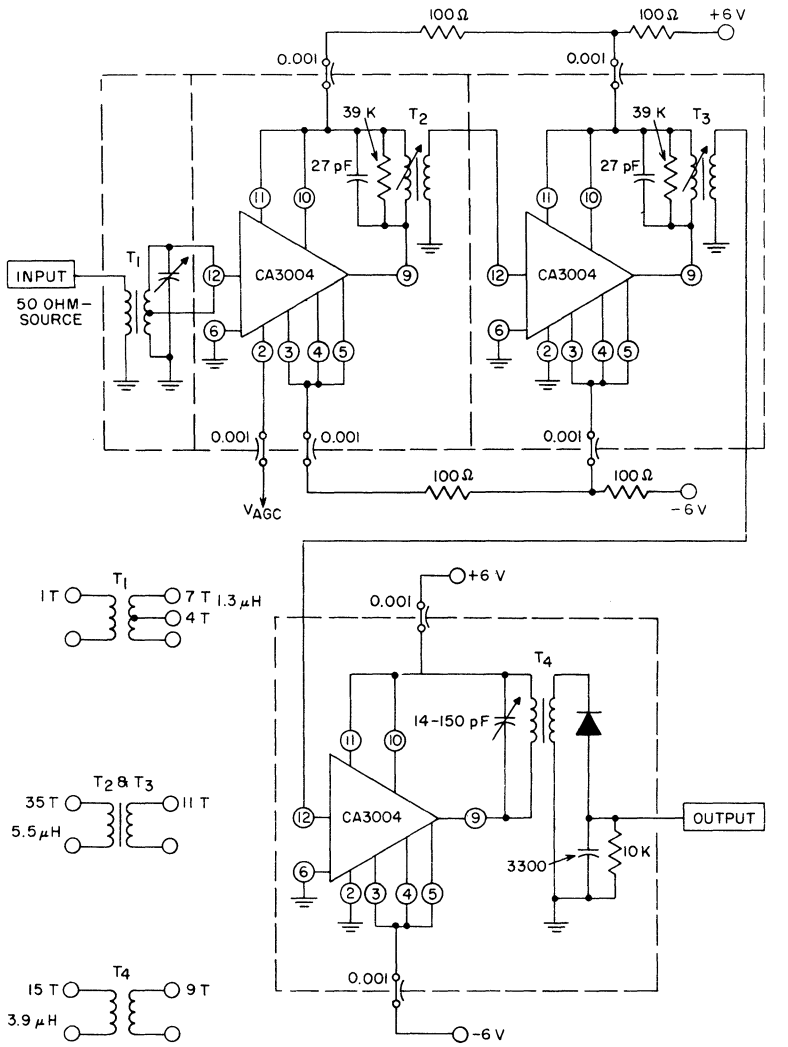
discussion of y parameters). At 30 MHz, the CA3005 differential amplifier output was mismatched. At high gains, the circuit feedback (y_r) is low, but the external-circuit layout adds feedback.

Two or more CA3004, CA3005, or CA3006 integrated circuits can be connected in cascade for use as a tuned if amplifier for either AM or FM applications. The schematic diagrams of two three-stage 12-MHz amplifiers are shown in Figs. 175 and 176,



Notes: 1. Transformer T_1 is a Ferramic Q-2 Type (unloaded Q = 200).
2. Transformers T_2, T_3, and T_4 are slug-tuned with carbonyl IT-75 material (unloaded Q = 75).

Fig. 175 — Three-stage, 12-MHz limiting if amplifier that uses CA3005 circuits in mode D.



Notes: 1. Transformers T_1 and T_4 are Ferramic Q-2 Toroid Types (unloaded Q = 200).
2. Transformers T_2 and T_3 are slug-tuned with carbonyl IT-71 material (unloaded Q = 70).

Fig. 176 — Three-stage, 12-MHz, gain-controlled AM amplifier that uses CA3004 circuits in operating mode D.

for FM and AM use, respectively. Both if amplifiers are housed in metal boxes, and adequate shielding and supply decoupling are provided.

The amplifier shown in Fig. 175 (limiting amplifier for FM use) is designed to provide a gain per stage of 26 dB. At this gain per stage, diodes are required at the input to prevent base-to-emitter breakdown. For operation as a low-level limiter, the circuit input is matched, and the required gain fixes the unloaded Q of the tuned circuit and the collector load. Good noise performance for the first stage is obtained by the use of a high-Q (200) toroid inductor for input transformer T_1. The other transformers are slug-tuned and have relatively low unloaded Q's (70 to 100) which contribute the necessary insertion loss for the required gain. A lower unloaded Q was required for transformer T_2, so 10,000 ohms of resistance was added in parallel with this transformer. Little or no skew is detectable in the response characteristic for this circuit, shown in Fig. 177. The limiting characteristic of the circuit is shown in Fg. 178. Other typical over-all performance characteristics are:

Total power drain = 48 milliwatts
Over-all power gain = 77 dB
3-dB bandwidth = 300 kHz
Input limiting level = 30 microvolts
Noise figure = 4 dB

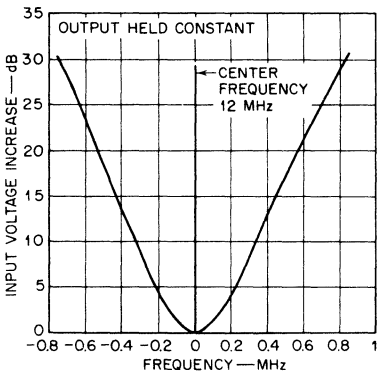


Fig. 177 — Frequency-response characteristics of the 12-MHz limiting amplifier shown in Fig. 175.

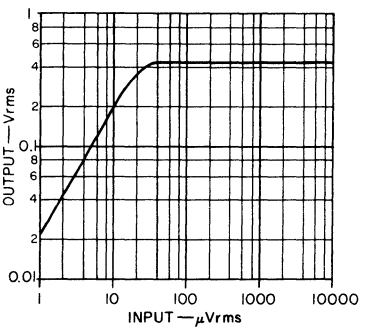


Fig. 178 — Limiting characteristics of the 12-MHz limiting amplifier shown in Fig. 175.

The AM circuit (Fig. 176) uses three CA3004 circuits and is designed to provide a stage gain of 25 dB. The source resistance to the input circuit was chosen as 800 ohms as a satisfactory compromise for gain, noise figure, and modulation-distortion perform-

ance. Input and output transformers, T_1 and T_4, have high unloaded Q's (200) to preserve good noise performance and to maximize the output power. The interstage transformers, T_2 and T_3, have low unloaded Q's (37) to achieve the required gain. The second detector has a 3-dB bandwidth of 5.0 kHz. The typical over-all performance characteristics are:

Power drain = 83 milliwatts
Power gain (to second-detector input) = 76 dB
AGC range (1st stage) = 60 dB
Noise figure = 4.5 dB
3-dB bandwidth = 160 kHz

The signal-to-noise ratio of the circuit as a function of the input is shown in Fig. 179, and the frequency-response characteristic is shown in Fig. 180.

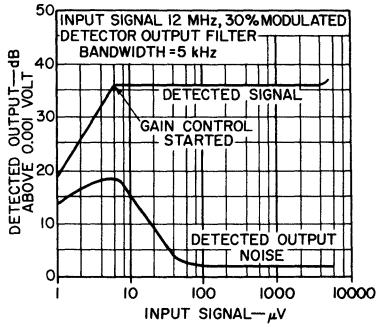


Fig. 179 — Output signal-to-noise ratio as a function of the input signal for the 12-MHz gain-controlled amplifier shown in Fig. 176 when gain control is used in only the first stage.

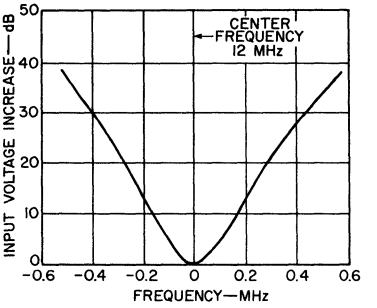
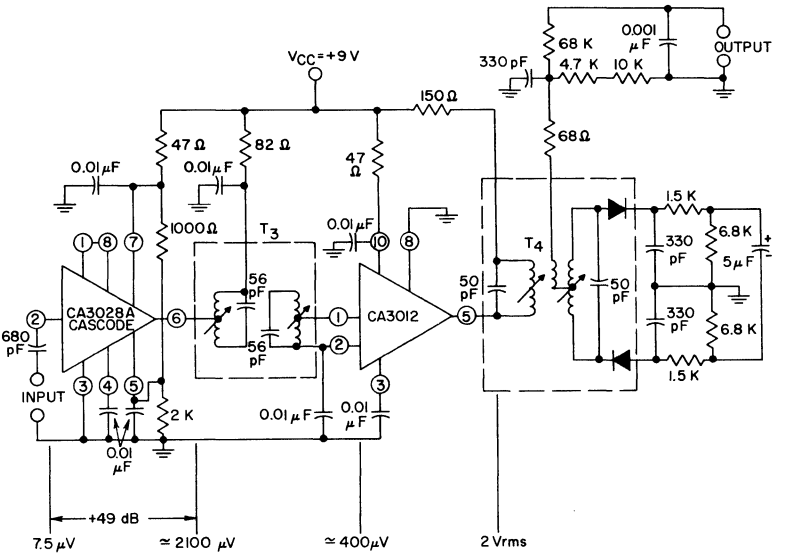


Fig. 180 — Frequency-response characteristics of the 12-MHz gain-controlled amplifier shown in Fig. 176.

10.7-MHz CA3028A Cascode IF Amplifier — Fig. 181 shows an FM if strip in which the CA3028A is used in a high-gain, high-performance cascode configuration in conjunction with a CA3012 integrated-circuit wide-band amplifier. (The CA3012 circuit is discussed in detail in a subsequent paragraph on FM IF AMPLIFIERS.) The CA3012 is used in the last stage because of the high gain of 74 dB input to the 4000-ohm-load ratio-detector transformer T_4. An input of approximately 400 microvolts is required at the base of the CA3012 for — 3 dB below full limiting. An impedance-transfer device and filter must be connected between the



T_3: Interstage transformer TRW #22486 or equiv.
T_4: Ratio detector TRW #22516 or equiv.
Audio Output: 155 mV rms for 7.5 μV ± 75 kHz input 3 dB below knee of transfer characteristic.

Fig. 181 — 10.7-MHz if amplifier using a CA3028A in a cascode configuration.

CA3012 base (terminal 1) and the output of the CA3028A (terminal 6). The insertion loss of this filter should be kept near 6 dB (1:2 ratio of loaded to unloaded Q) so that all possible gain can be realized up to the CA3012 base. In addition to this insertion loss, a voltage step-down loss of 5.8 dB in the interstage filter is unavoidable. Therefore, the total voltage loss is approximately 9 to 14 dB, and an output of 1500 to 2000 microvolts must be available from the CA3028A to provide the required 400-microvolt input to the CA3012.

The voltage gain of the CA3028A into a 3000-ohm load is determined as follows:

$$VG = \frac{-y_f}{y_o + y_L} = \frac{100 \times 10^{-3}}{0.33 \times 10^{-3}} = 300 = 49 \text{ dB} \quad (191)$$

This calculation indicates a sensitivity of 6.6 microvolts at the CA3028A base (terminal 2). This value cannot be realized, however, because the CA3012 limits on noise peaks so that the gain figure is reduced.

A sensitivity of 7.5 microvolts was realized in the design shown in Fig. 181. The filter approach with high-gain integrated-

circuit chips differ from that for single, cascaded transistor stages in that lumped selectivity is required rather than distributed selectivity.

Special care must be exercised when second-channel attenuation in the order of 45 dB is required. Selectivity is then proportioned as follows:

Interstage filter: double-tuned 220 kHz at — 3 dB; coefficient of critical coupling, 0.7; voltage loss, 8 dB

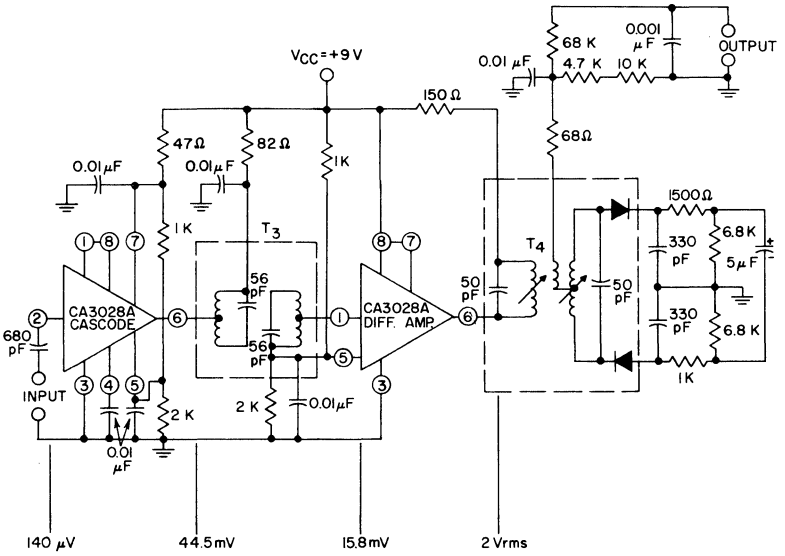
Converter filter: triple-tuned, 220 kHz at — 3 dB; coefficient of critical coupling, 0.8; voltage loss, about 28 dB

Because of input limiting in the CA3012, the interstage filter exhibits a somewhat wider bandwidth than the 220 kHz indicated. Therefore, a coefficient of critical coupling near 0.8 is realized, which is optimum for minimum deviation from constant time delay. The triple-tuned converter filter alone provides second-channel attenuation of 30 to 33 dB, while the interstage filter contributes 8 to 10 dB. The filters described meet requirements of both performance and economy.

The large collector swing that can be obtained in cascode operation of the CA3028A makes it desirable to take the agc voltage from the collector or "hot" end of the if transformer for front-end gain control. The cascode stage then operates primarily in its linear region, and excellent selectivity (40 dB) is maintained even for large signal inputs of approximately 0.4 volt. Front-end gain reduction is between 40 and 50 dB.

10.7-MHz IF Strip Using Two CA3028A Circuits — The 10.7-MHz if strip shown in Fig. 182 uses two CA3028A integrated circuits to provide less over-all gain than the circuit of Fig. 181. The first CA3028A is connected as a cascode amplifier and yields voltage gain of 50 dB; the second CA3028A is connected as a differential amplifier and yields voltage gain of 42 dB.

When a practical interstage transformer having a voltage insertion loss of 9 dB is used, over-all gain is 83 dB and the sensitivity at the base of the first CA3028A is 140 microvolts. A less sophisticated converter filter (double-tuned) could be employed at the expense of about 26 dB of second-channel attenuation. If the voltage insertion loss of the converter filter is assumed to be 18 dB and the front-end voltage gain (antenna to mixer collector) is 50 dB, this receiver would have an IHFM sensitivity* of approximately 8 microvolts.



T_3: Interstage transformer TRW #22486 or equiv.
T_4: Ratio detector TRW #22516 or equiv.
Audio Output: 155 mV rms for 140 μV $\pm$ 75 kHz input 3 dB below knee of transfer characteristic.

Fig. 182 — 10.7-MHz if strip using two CA3028A circuits.

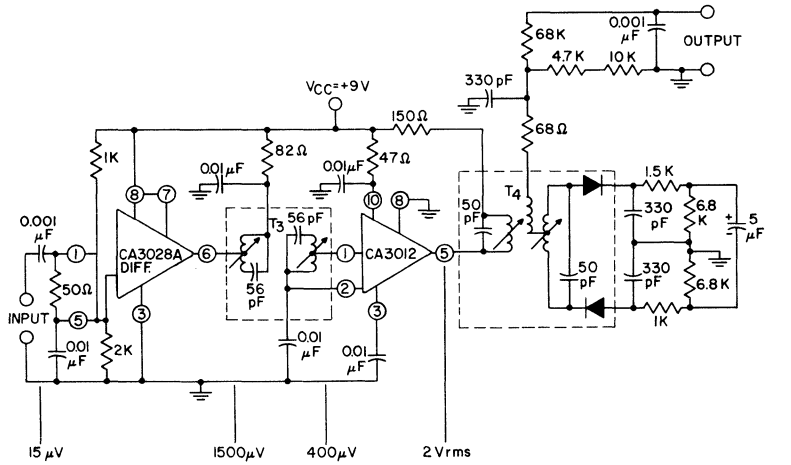
10.7-MHz CA3028A Differential-Amplifier IF Strip — Fig. 183 shows a 10.7-MHz medium-gain if strip consisting of a CA3028A connected as a differential amplifier and a CA3012 wide-band amplifier. As in the circuit shown in Fig. 181, an input of approximately 1500 microvolts is required to the interstage filter. The differential-mode voltage gain of the CA3028A into a 3000-ohm load is determined as follows:

$$VG = \frac{-y_f}{y_o + y_L} = \frac{35 \times 10^{-3}}{0.38 \times 10^{-3}} = 92.5 = 39.3 \text{ dB} \quad (192)$$

This voltage gain requires that an input of approximately 15 microvolts be available at the base of the CA3028A differential amplifier.

Even if a triple-tuned filter having a voltage insertion loss of 28 dB is used in a low-gain front end, a receiver having an IHFM sensitivity of 5 microvolts results. If 26 dB second-channel attenuation is permissible, a 3-microvolt-sensitivity IHFM receiver can be realized.

* Rating based on Institute of High Fidelity Manufacturer's standard No. IHF-A-201(1966).



T_3: Interstage transformer TRW #22486 or equiv.
T_4: Ratio detector TRW #22516 or equiv.
Audio Output: 155 mV rms for 15 μV $\pm$ 75 kHz input 3 dB below knee of transfer characteristic.

Fig. 183 — 10.7-MHz if strip using a CA3028A in a differential-amplifier configuration.

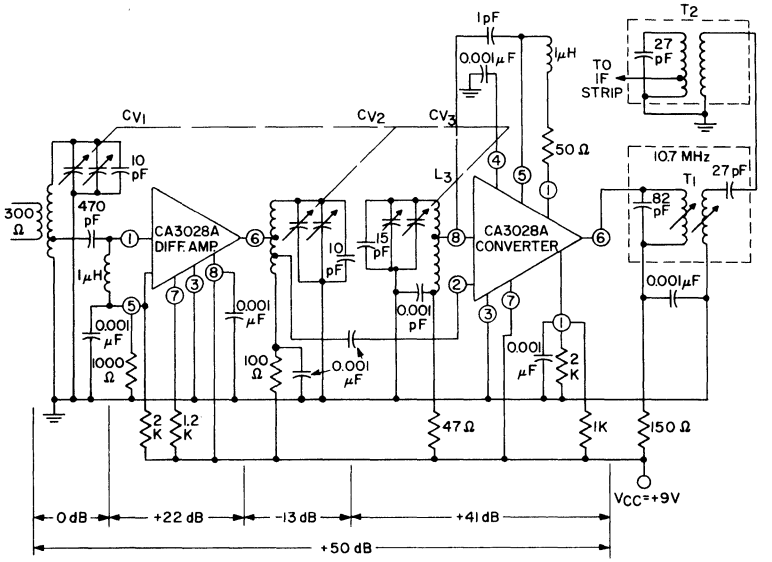
88-MHz-to-108-MHz FM Front End Using the CA3028A — Fig. 184 illustrates the use of the CA3028A as an rf amplifier and a converter in an 88-to-108-MHz FM front end. For best noise performance, the differential mode is used and the base of the constant-current source Q_3 is biased for a power gain of 15 dB. The rf amplifier input circuit is adjusted for an insertion loss of 2 dB to keep the noise figure of the front end low. Because the insertion loss of the input transformer adds directly to the integrated-circuit noise figure of 5.5 dB, the noise figure for the front end alone is 7.5 dB, as compared to noise figures of about 6 dB for commercial FM tuners.

Although a single-tuned circuit is shown between the collector of the rf-amplifier stage and the base of the converter stage, a double-tuned circuit is preferred to reduce spurious response of the converter. If the double-tuned circuit is critically coupled for the same 3-dB bandwidth as the single-tuned circuit, the insertion loss remains the same.

The collector of the rf stage is tapped down on the interstage coil at approximately 1500 ohms, and the base of the converter stage at 150 ohms. RF voltage gain is computed as follows:

Antenna to base	0 dB
Base to collector	22 dB

Voltage insertion loss of interstage coil ..... —13 dB
Net rf voltage gain ..... 9 dB



L_1: 3-3/4 T #18 tinned copper wire; winding length 5/16" on 9/32" form; tapped at 1-3/4 T; primary — 2 turns #30 SE.
L_2: 3-3/4 T #18 tinned copper wire; winding length 5/16" on 9/32" form; tapped at 6 2-1/4 T, A 3/4 T.
$Cv_{1\text{-}2}$: variable $\triangle$ C $\approx$ 15 pF.
T_1: Mixer transformer TRW #22484 or equiv.
T_2: Input transformer TRW #22485 or equiv.
L_3: 3-1/2 T #18 tinned copper wire; winding length 5/16" on 9/32" form.
$Cv_{1\text{-}3}$: variable, $\triangle$ C $\approx$ 15 pF.

Fig. 184 — 88-MHz-to-108-MHz front-end circuit for an FM receiver.

If an if converter transformer having an impedance of 10,000 ohms is used, the calculated voltage conversion gain is

$$VG_C = \frac{-y_f}{y_o + y_L} = 112 = 41.3 \text{ dB} \qquad (193)$$

Measured gain into the collector of the converter is 42 dB. The measured voltage gain of the rf amplifier and converter into a 10,000-ohm load is 52 dB; calculated gain is 50 dB. When the converter is tuned for the commercial FM band (88 to 108 MHz), the following parameters apply:

Input resistance R_{in}	170	ohms
Input capacitance C_{in}	6.3	pF
Output resistance R_{out}	80K	ohms
Output capacitance C_{out}	3.5	pF
Conversion transconductance	13	mmhos

The rf amplifier and converter shown in Fig. 184 were combined with the if amplifier shown in Fig. 181, and the following performance data were measured at 100 MHz:

30-dB (S + N)/N IHFM Sensitivity	3	μV
Image Rejection	46	dB

Receiver noise figure is the limiting factor that permits a sensitivity of only 3 microvolts to be realized.

Mixer Capabilities

The CA3004, CA3005, CA3006 and CA3028A integrated circuits may be used as mixers, modulators, and product detectors. The schematic diagrams in Figs. 185(a) and 185(b) illustrate the

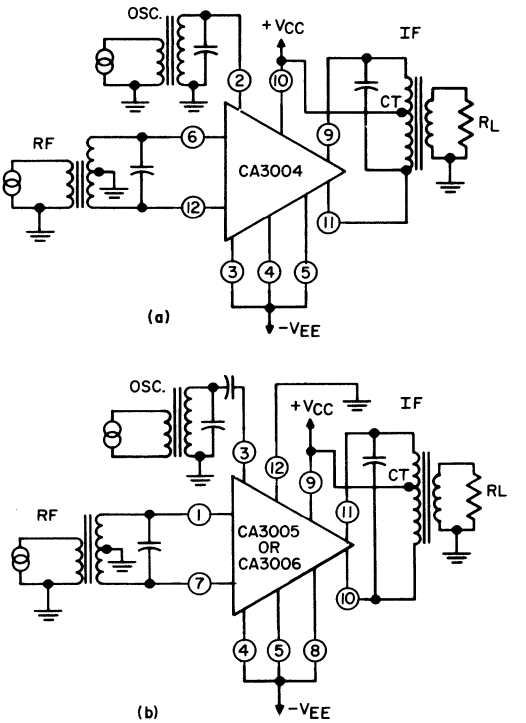


Fig. 185 — Circuit diagrams for use of (a) the CA3004 and (b) the CA3005 or CA3006 as mixers (operating mode D).

use of these circuits in mixer applications. The oscillator input is injected at the base of transistor Q_3 (because there is no direct-base connection available on the CA3004, a higher oscillator drive voltage is required for this circuit); the rf input is injected single- or double-ended to the bases of transistors Q_1 and Q_2. The use of a center-tapped inductor for the output tuned circuit (double-ended) allows the common-mode signal of the oscillator to be balanced out so that the oscillator will not overload subsequent stages, and provides carrier suppression for modulators.

The gain performance and generation of harmonics in the CA3004, CA3005, CA3006, and CA3028A mixer circuits are dependent on the amplitude of the oscillator drive signal and the dc bias. The expression for product detection or frequency multiplication in the CA3005 or CA3006 (consult Fig. 186) is determined as follows:

$$e_o = e_1 g_m Z_L \tag{194}$$

where e_o is the output voltage, e_1 is the differential input voltage, g_m is the transconductance of the differential pair of transistors (Q_1 and Q_2), and Z_L is the load impedance (total between collectors). For a balanced circuit, the transconductance is given by

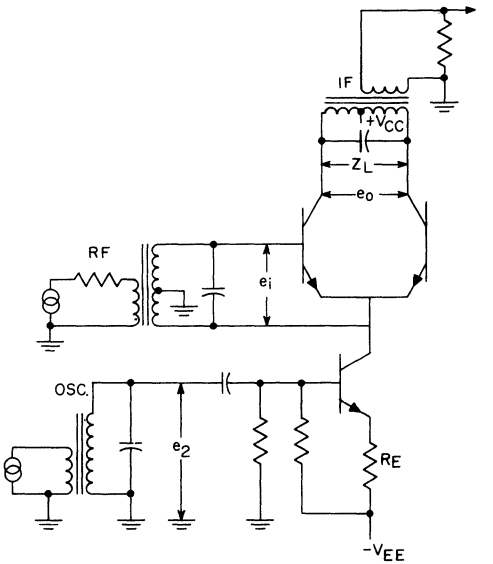


Fig. 186 — Circuit diagram of a CA3005 or CA3006 balanced mixer (operating mode D). The equations for product detection or multiplication are based on this circuit.

$$g_m = \frac{\alpha q}{2KT} I_o \tag{195}$$

The term I_o represents the collector current of transistor Q_3 and may be expressed as

$$I_o = g_{m_2} e_2 \tag{196}$$

where g_{m2} is the transconductance of transistor Q_3 and e_2 is the input voltage applied to transistor Q_3. The output voltage, e_o, therefore, is given by the following equation:

$$e_o = \frac{\alpha q}{2KT} e_1 e_2 g_{m_2} Z_L \tag{197}$$

Eq. (197) is a general expression for the output voltage of the mixer having input signals e_1 and e_2. With emitter degeneration in the constant-current transistor (Q_3), g_{m2} is essentially constant for a sufficiently large emitter current (greater than 1 milliampere); the current I_o, therefore, follows the applied voltage e_2.

When e_1 and e_2 are sinusoidal and g_m is constant, the input signal voltages are given as follows:

$$e_1 = E_1 e^{j\omega_1 t} + \overset{*}{E}_1 e^{-j\omega_1 t} \tag{198}$$

$$e_2 = E_2 e^{j\omega_2 t} + \overset{*}{E}_2 e^{-j\omega_2 t} \tag{199}$$

($\overset{*}{E}_1$ is the conjugate of E_1, and $\overset{*}{E}_2$ is the conjugate of E_2)

With the substitution of these relationships, the equation for the output voltage for he CA3005 or CA3006 then becomes

$$e_0 = \frac{\alpha q}{2KT} g m_2 Z_L [E_1 E_2 e^{j(\omega_1 + \omega_2)t} + \overset{*}{E}_1 \overset{*}{E}_2 e^{-j(\omega_1 + \omega_2)t}]$$

$$+ \frac{\alpha q}{2KT} g m_2 Z_L [\overset{*}{E}_1 \overset{*}{E}_2 e^{j(\omega_1 - \omega_2)t} + \overset{*}{E}_1 E_2 e^{-j(\omega_1 - \omega_2)t}] \tag{200}$$

Eq. (200) gives the output voltage for a CA3005 or CA3006 used as a product detector or multiplier. (Note that only the two sideband frequencies are included in the output.) The requirements for product detectors or multipliers are that the circuit should be biased in a linear region with a small signal voltage applied. Because $\alpha q g_{m2}/2KT$ is essentially constant, the gain of the mixer is determined from Z_L and the $e_1 e_2$ product. The linearity of the CA3006 is illustrated by the curve of the conversion trans-

conductance as a function of the oscillator voltage, shown in Fig. 187. (Although the curve is plotted on logarithmic paper because of the wide range, the relationship is linear.) The gain reaches a

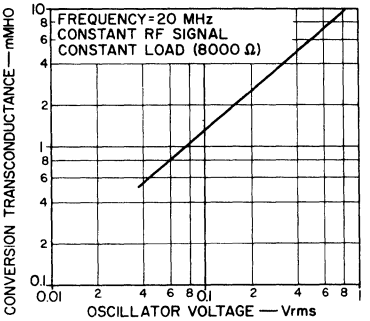


Fig. 187 — Conversion gain of a CA3005 or CA3006 mixer circuit as a function of oscillator voltage.

maximum value at approximately 2.5 volts rms. Because measurement inaccuracies prevent the use of this curve to determine harmonic generation, spurious-signal measurements were taken on CA3005 and CA3006 mixer circuits. For these measurements, the rf input was untuned and the oscillator and if frequencies were held constant. For a fixed amplitude of oscillator injection on terminal 3, the rf was varied in frequency, and the amplitude of the responses was recorded. The results are shown in Table XXIII. The spurious signals generated are a function of oscillator drive. A low oscillator drive (0.1 volt rms) produced only three spurious signals for which the rejection was less than 70 dB down.

Table XXIII—*Response of a CA3005 or CA3006 Mixer to Spurious Harmonics*

Frequency	Signal Frequency f_x (MHz)	Difference-Frequency Output (dB relative to $f_o - f_x$) for V_{osc} at Term. 3 (Vrms) of 1	0.7	0.3	0.1
$f_o - f_x$	1.0	0	0	0	0
f_{if}	0.659	7.5	10	18	27
$2f_x - f_o$	1.159	—53.1	—53.1	—54.9	—52.3
$2f_o - 2f_x$	1.329	—76.1	—	—	—
$2f_x - 2f_o$	1.988	—75.5	—	—	—
$f_x - f_o$	2.318	0	0	0	0
$2f_o - f_x$	2.659	—31.7	—35	—39.7	—47.8
$2f_x - 3f_o$	2.813	—79.6	—	—	—
$f_x - 2f_o$	3.977	—31.7	—35	—39.7	—47.8
$3f_o - f_x$	4.309	—35.8	—59.3	—74.7	—
$f_x - 3f_o$	5.627	—38.5	—57	—74	—
$4f_o - f_x$	5.977	—38.9	—63	—	—

f_o = 1.659 MHz; V_{osc} = oscillator injection voltage.

All blank spaces indicate difference-frequency output more than 70 dB below the $f_o - f_x$ output.

These measurable spurious responses were third-order products that involved the second harmonic of either the oscillator or rf signal. The relative if gain increases with decreasing oscillator drive because of lower mixer gain.

The common-mode cancellation of the oscillator signal at the collector outputs is indicative of the carrier suppression that can be provided in modulators. The carrier suppression is a function of output tuned-circuit balance and the transistor offset voltage. The contribution of the offset is illustrated in Figs. 188 and 189 which show the output signal as a function of the offset voltage for the CA3004 and for the CA3005 or CA3006, respectively. These data were obtained on circuits operated with a balanced output tuned to the oscillator frequency.

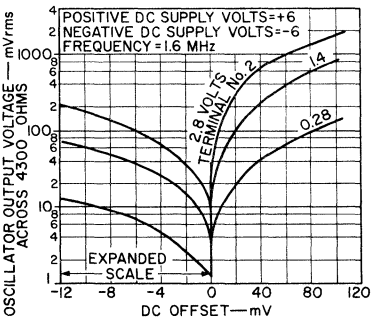


Fig. 188 — Cancellation of the oscillator signal at the output of a CA3004 mixer as a function of dc offset voltage.

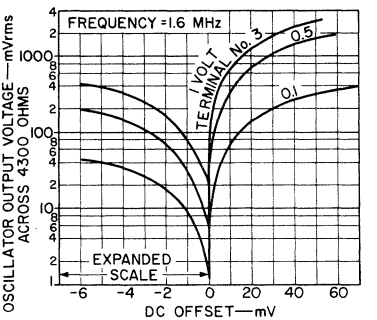


Fig. 189 — Cancellation of the oscillator signal at the output of a CA3005 or CA3006 mixer as a function of dc offset voltage.

Mixers — The use of the CA3004 and the CA3005 or CA3006 as balanced mixers to convert 20 MHz to 1.75 MHz is shown in Fig. 190. Because the input impedances of the two cir-

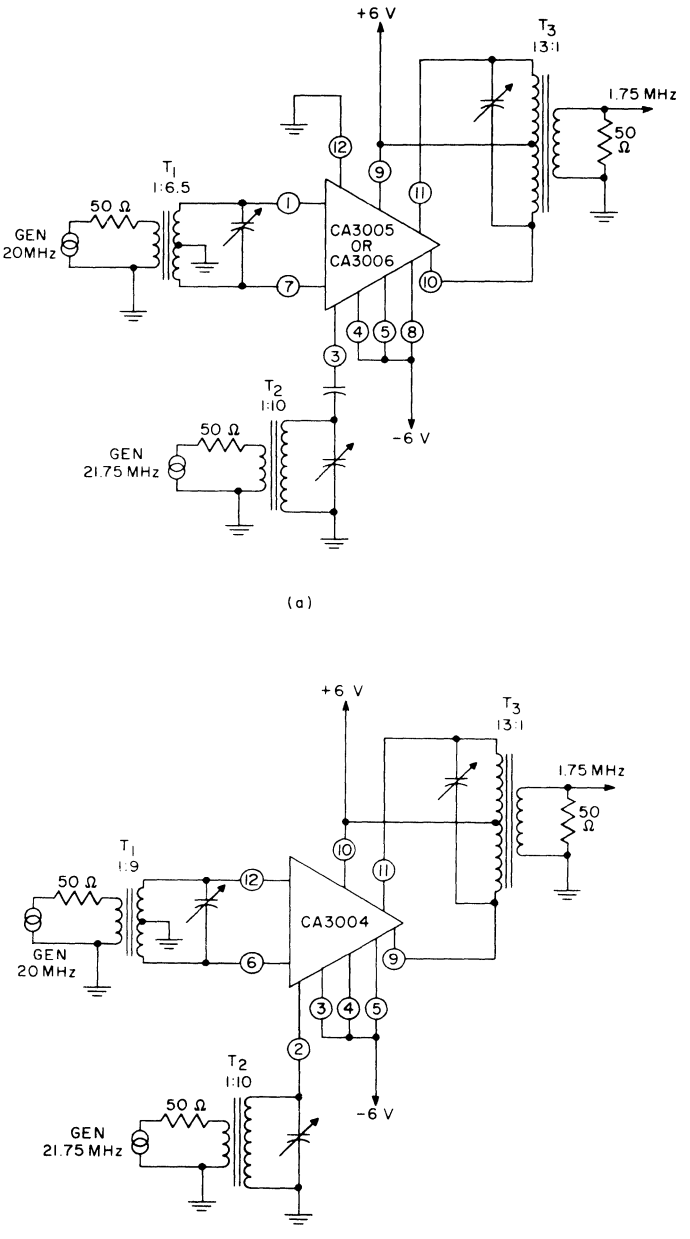


Fig. 190 — CA3004 and CA3005 or CA3006 balanced mixers used to convert an input frequency of 20 MHz to an output frequency of 1.75 MHz.

cuits differ by a factor of approximately 2:1, typically 4000 ohms for the CA3004 and 2200 ohms for the CA3005 or CA3006, different input transformers (T_1) are required; the other tuned circuits, however, are the same. The output load impedance between collectors is approximately 8000 ohms. The conversion power gain and noise figure as a function of the oscillator drive are shown in Figs. 191 and 192. Power gain increases and noise figure decreases with increases in oscillator drive.

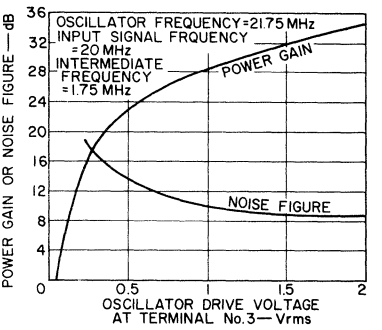


Fig. 191 — Power gain and noise figure as a function of oscillator drive voltage for the CA3005 or CA3006 balanced mixer.

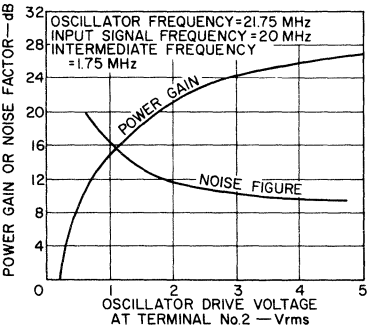


Fig. 192 — Power gain and noise figure as a function of oscillator drive voltage for the CA3004 balanced mixer.

Suppressed-Carrier Modulator and Product Detector — The CA3005 and CA3006 can be used in a suppressed-carrier double-sideband modulator and product detector. The double-sideband modulator is a convenient vehicle to evaluate carrier suppression and product detection. With the two circuits coupled together, the relation between modulation distortion and drive levels is readily established.

Feedback may cause oscillation or unbalance; care must, therefore, be taken in the external-circuit layout design. Shielding must also be provided for both the double-sideband modulator and product detector.

The circuit diagram of the double-sideband modulator is shown in Fig. 193. The modulating signal is applied single-ended to the differential pair of transistors, Q_1 and Q_2, and the oscillator signal is applied to the base of transistor Q_3. The output is taken double-ended from the balanced transformer, T_2. The carrier suppression is a function of bilateral symmetry (offset, output-transformer balance and modulation drive circuits) and the modulation-to-carrier drive ratio. With the external-circuit bilateral

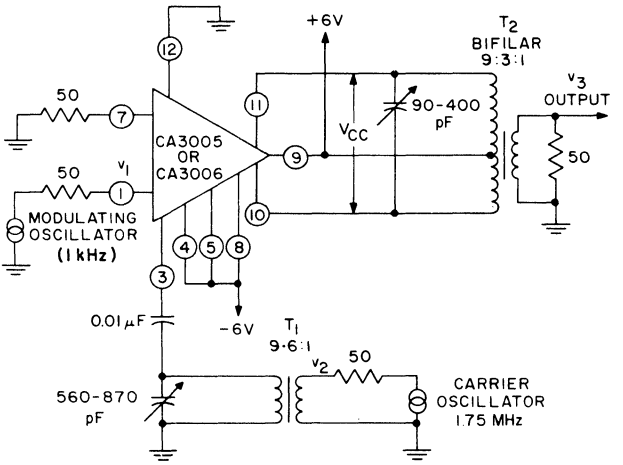


Fig. 193 — Double-sideband, suppressed-carrier modulator using the CA3005 or CA3006.

symmetry carefully preserved, the carrier output is approximately 25 dB below the double-sideband output for CA3006 units (offset $\leqq$ 1 millivolt) operated with a drive v_1 = 10 millivolts rms and v_2 = 31.5 millivolts rms. Although the signal-to-carrier ratio of 25 dB represents an inadequate rejection for most systems (40 to 60 dB is usually required), this value relaxes the filter requirements from those necessary on more commonly used single-sideband modulators. An improvement over the 25-dB ratio is obtained if the modulation drive v_1 is increased and the carrier drive v_2 is decreased, because the output is a function of the product of v_1 and v_2.

The circuit diagram for a product detector is shown in Fig. 194. The product detector, which provides the advantage of a double-ended out-of-phase output, is driven through a 50-ohm adjustable feed by the double-sideband signal from the modulator. The levels of v_1, v_2, v_4, and v_5 are altered to establish the relationship between the harmonic distortion and drive levels as well as gain values for typical operation. The results are shown in Table XXIV. Overdrive by the modulation (v_1) or the modulated signal (v_4) results in third-harmonic distortion of the detected signal. It should be noted that gain is a function of either the product of v_1 and v_2, or the product of v_4 and v_5.

Video-Amplifier Capabilities

The CA3004, CA3005, and CA3006 integrated circuits may be used as video amplifiers, as shown in Figs. 195(a) and 195(b).

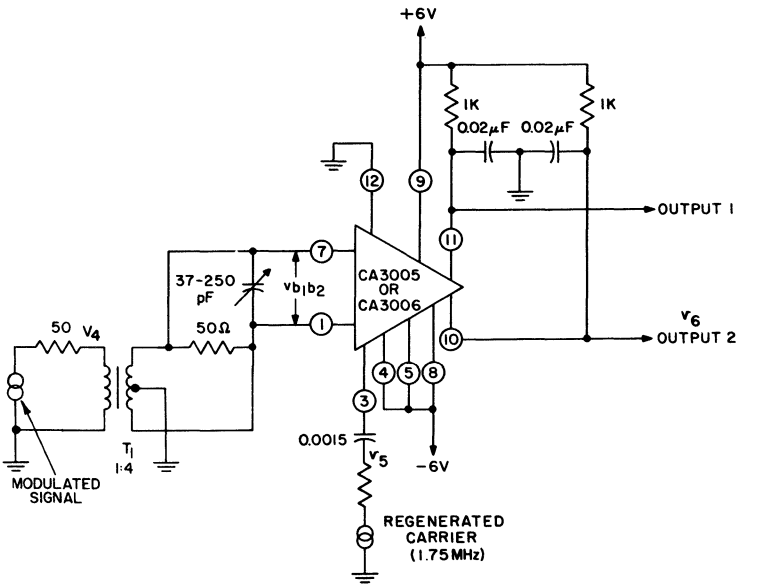


Fig. 194 — Product detector using the CA3005 or CA3006.

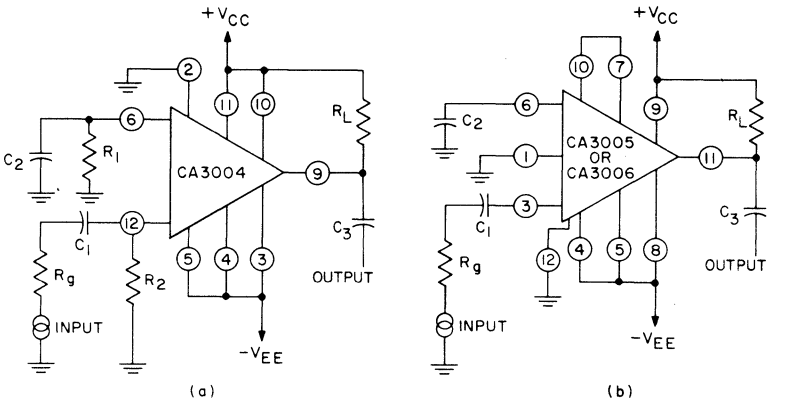


Fig. 195 — Video amplifiers using (a) the CA3004 in a differential-amplifier configuration and (b) the CA3005 or CA3006 in a cascode configuration.

A relatively large number of external components is required, and the availability of internal-circuit connections for these external components provides a large degree of flexibility to the user with respect to such factors as bandwidth, gain, power dissipation, and peaking. In the circuit shown in Fig. 195(a), R_1 should be equal

to R_2 to preserve the circuit balance, and C_2 should be an adequate bypass so that the noise factor and gain are not degraded. For the cascode configuration shown in Fig. 195(b), C_2 is an emitter bypass, and its reactance should be less than 1.5 ohms at the lowest video frequency to be handled.

In either cascode or single-ended differential-amplifier configurations, the feedback is low. Each configuration provides good isolation from output to input; the high-frequency performance therefore can be approximated from the input and output parallel R and C for a single stage or from the total shunt R and C between stages for an iterative connection. The mid-frequency voltage gain can be computed from the familiar $g_m R_L$ product. As an aid to such calculations, Table XXV gives the input and output parallel R and C and the absolute values of g_m for the various circuits and configurations for operation at 1, 10, and 40 MHz. For more precise, but more elaborate calculations, the y parameters may be used for video-amplifier design.

Table XXIV—*Gain and Distortion as a Function of Different Drive Levels for a Double-Sideband Modulator and Product Detector Using the CA3006*

Variable	Voltages ▲ (mV rms) Term. 3	V_{CC}	V_3	$V_{b_1b_2}$	V_6	3rd Harmonic Distortion (dB below fundamental) *
V_1 varied, $V_2 = 31.5$ mV, $V_4 = 1$ mV, $V_5 = 0.5$ mV						
5	296	46	4.95	4	36	54
10	296	80	8.9	4	36	54
30	296	250	26.6	4	36	37.5
V_2 varied, $V_1 = 10$ mV, $V_4 = 1$ mV, $V_5 = 0.5$ mV						
31.5	296	83	8.9	4	36	54
100	960	262	28	4	36	51
315	2960	830	8.9	4	36	50
V_4 varied, $V_1 = 10$ mV, $V_2 = 31.5$ mV, $V_5 = 0.5$ mV						
0.5	296	83	8.9	2	17.5	54
1	296	83	8.9	4	36	52
3	296	83	8.9	12	110	47.5
5	296	83	8.9	20	188	37▪
V_5 varied, $V_1 = 10$ mV, $V_2 = 31.5$ mV, $V_4 = 1$ mV						
0.315	296	83	8.9	4	23	54‡
0.5	296	83	8.9	4	36	54
1.0	296	83	8.9	4	86	50

▲ See Figs. 193 and 194 for explanation of voltage designations.
* 2nd, 4th, and 5th harmonics more than 60 dB down except as noted.
▪ 2nd harmonic 51 dB down, 5th harmonic 59 dB down.
‡ 2nd harmonic 56 db down.

Table XXV—*Input and Output Parallel RC Network, Transconductance, and Video Performance Data for CA3004, CA3005, and CA3006 RF Amplifiers**

Frequency (MHz)	Input Parallel RC R_{in} (ohms)	Input Parallel RC C_{in} (pF)	Output Parallel RC R_{out} (ohms)	Output Parallel RC C_{out} (pF)	Transconductance g_m (mmhos)
CA3005 or CA3006 Cascode Operation					
1	500	42	-1.67×10^6	3	78
10	500	42	-1.67×10^6	3	77
40	180	22	-6×10^5	3	58
CA3005 or CA3006 Differential-Amplifier Operation					
1	2500	16	10^5	4	20
10	1800	13	4×10^4	4	20
40	670	10.5	2800	7.6	18.6
CA3004 Differential-Amplifier Operation					
1	6650	8	1.7×10^5	6.5	7.8
10	6650	6.2	10^5	6.1	7.8
40	2000	5	2×10^4	6.8	7.6

Video Performance (Simulated Iterative Connection)

Type	Operation	Interstage R_L (ohms)	High-Frequency 3-dB Point (MHz) Meas.	High-Frequency 3-dB Point (MHz) Calc.	Mid-Band Voltage Gain (dB) Meas.	Mid-Band Voltage Gain (dB) Calc.
CA3005 or CA3006	Cascode Differ. Ampl.	150	23	20	19.3	20.6
CA3005 or CA3006	Differ. Ampl.	500	18	16	19.5	20.0
CA3004		1000	18.4	15	17.2	18.0

* Data obtained for circuits operated from ±6-volt dc supplies in operating mode D.

OPERATIONAL AMPLIFIERS

The RCA family of linear integrated circuits includes a broad line of highly versatile operational amplifiers that may be adapted to perform a large variety of circuit functions in telemetry, data-processing, instrumentation, and communications equipment. Typical applications include narrow-band or wide-band amplifiers, oscillators, multivibrators, comparators, scaling adders, integrators, and differentiators. These amplifiers are primarily designed to operate with externally applied negative feedback. Table XXVI lists the operational amplifiers and points out the maximum dc supply voltage, package configuration, and operating-temperature range for each type.

The integrated-circuit operational amplifiers are designed to operate from symmetrical positive and negative dc power supplies at various levels of supply voltage. On the basis of the dc supply

Table XXVI—*RCA Integrated-Circuit Operational Amplifiers*

Type No.*	Type of Package	Maximum DC supply Voltage (volts)	Operating-Temperature Range (°C)
CA3008 CA3008A	14-terminal ceramic flat pack	±6	−55 to +125
CA3010 CA3010A	12-terminal TO-5 style package	±6	−55 to +125
CA3015 CA3015A	12-terminal TO-5 style package	±12	−55 to +125
CA3016 CA3016A	14-terminal ceramic flat pack	±12	−55 to +125
CA3029 CA3029A	14-terminal dual-in-line plastic package	±6	0 to 70
CA3030 CA3030A	14-terminal dual-in-line plastic package	±12	0 to 70
CA3033 CA3033A	14-terminal dual-in-line plastic package	±12 ±18	−55 to +125
CA3037 CA3037A	14-terminal dual-in-line ceramic package	±6	−55 to +125
CA3038 CA3038A	14-terminal dual-in-line ceramic package	±12	−55 to +125

* The RCA line of integrated-circuit operational amplifiers also includes the CA3031/702A and CA3032/702C types. These amplifiers are designed to operate from asymmetrical dual dc supply voltage up to +12 and −6 volts, are supplied in 8-terminal TO-5 style packages, and have an operating temperature range of −55°C to +125°C. Ratings and characteristics for the CA3031/702A and CA3032/702C are given in the TECHNICAL DATA section of this manual and in the technical bulletin on these types.

voltage rating, the amplifiers may be classified as ±6-volt types, ±12-volt types, and ±18-volt types. The types indicated by the "A" suffix (refer to Table XXVI) have lower noise figures and improved static characteristics (i.e., input offset voltage and current, input bias current, and input impedance) in comparison to the corresponding types without the "A" suffix. As shown in Table XXVI, the CA3033A also has a higher supply-voltage rating than the CA3033. For applications in which low noise and dc balance are important considerations, the "A"-version types are recommended. Fig. 196 shows the noise figure of the "A"-version operational amplifiers as a function of frequency for operation from ±6-volt and ±12-volt dc supply voltages.

±6-Volt Types

The **CA3008** and **CA3008A,** the **CA3010** and **CA3010A,** the **CA3029** and **CA3029A,** and the **CA3037** and **CA3037A** integrated-circuit operational amplifiers are designed to operate from

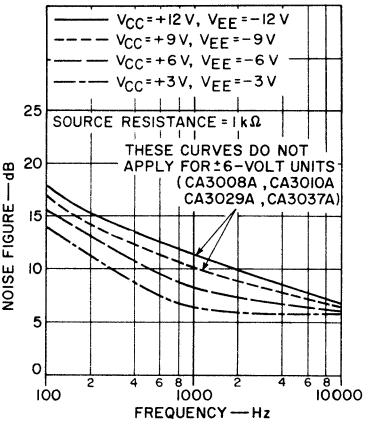


Fig. 196 — Noise figure for the "A"-version integrated-circuit operational amplifiers for operation from ±6-volt and ±12-volt supply voltages.

dual positive and negative 6-volt dc supplies. All the amplifiers have the same circuit configuration and, except for the improved noise and static characteristics of the "A"-version types, their electrical characteristics are also the same.

Fig. 197 shows the schematic diagram and terminal numbers for the ±6-volt integrated-circuit operational amplifiers. Two sets of terminal numbers are shown because the numbering system for the CA3010 and CA3010A, which are supplied in 10-terminal TO-5 style packages, differs from that of the other circuits, which are supplied in 14-terminal (flat-pack or dual-in-line) packages. The numerals enclosed in squares are the terminal designations for the CA3010 and CA3010A packages.

In the following discussion, terminal numbers referred to in the text or shown on diagrams are those for the 14-terminal circuits; corresponding terminals for the CA3010 and CA3010A can be determined from the schematic diagram in Fig. 197. Moreover, for convenience of notation, specific reference is made to only the CA3008 and CA3008A circuits. All information given for the CA3008 is equally applicable to the CA3010, CA3029, and CA3037; all information given for the CA3008A can also be directly applied to the other "A"-version types.

Circuit Description — Each operational amplifier consists basically of two differential amplifiers and a single-ended output circuit in cascade. The pair of cascaded differential amplifiers are responsible for virtually all the gain provided by the operational-amplifier circuit. The inputs to the operational amplifier are applied to the bases of the pair of emitter-coupled transistors, Q_1 and Q_2,

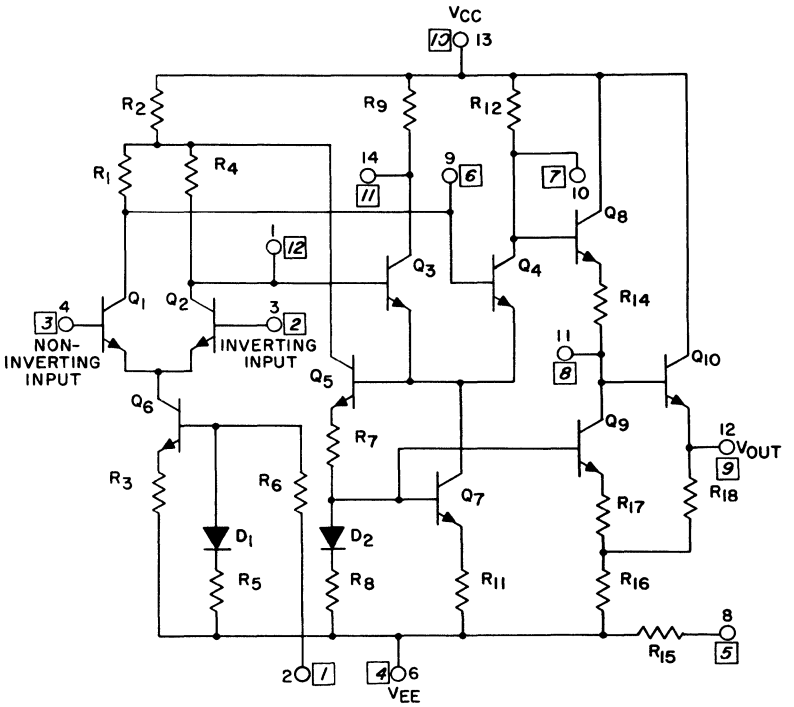


Fig. 197 — Schematic diagram for the ±6-volt integrated-circuit operational amplifiers (CA3008, CA3008A, CA3010, CA3010A, CA3029, CA3029A, CA3037, and CA3037A).

in the first differential amplifier. The inverting input (at terminal 3) is applied to the base of transistor Q_2, and the noninverting input (at terminal 4) is applied to the base of transistor Q_1. These transistors develop the driving signals for the second differential amplifier. A dc constant-current-sink transistor, Q_6, is also included in the first stage to provide bias stabilization for transistors Q_1 and Q_2. Diode D_1 provides thermal compensation for the first differential stage.

The emitter-coupled transistors, Q_3 and Q_4, in the second differential amplifier are driven push-pull by the outputs from the first differential amplifier. Bias stabilization for the second differential amplifier is provided by current-sink transistor Q_7. Compensating diode D_2 provides the thermal stabilization for the second differential amplifier and also for the current-sink transistor, Q_9, in the output stage.

Transistor Q_5 develops the negative feedback to reduce common-mode error signals that are developed when the same input

is applied to both input terminals of the operational amplifier. Transistor Q_5 samples the signal that is developed at the emitters of transistors Q_3 and Q_4. Because the second differential stage is driven push-pull, the signal at this point will be zero when the first differential stage and the base-emitter circuits of the second stage are matched and there is no common-mode input. A portion of any common-mode, or error, signal that appears at the emitters of transistors Q_3 and Q_4 is developed by transistor Q_5 across resistor R_2 (the common collector resistor for transistors Q_1, Q_2, and Q_5) in the proper phase to reduce the error. The emitter circuit of transistor Q_5 also reflects a portion of the same error signal into current-sink transistor Q_7 in the second differential stage so that the activating error signal is further reduced.

Transistor Q_5 also develops feedback signals to compensate for dc common-mode effects produced by variations in the supply voltages. For example, a decrease in the dc voltage from the positive supply results in a decrease in the voltage at the emitters of transistors Q_3 and Q_4. This negative-going change in voltage is reflected by the emitter circuit of transistor Q_5 to the bases of current-sink transistors Q_7 and Q_9. Less current then flows through these transistors. The decrease in the collector current of transistor Q_7 results in a reduction of the current through transistors Q_3 and Q_4, and the collector voltages of these transistors tend to increase. This tendency to increase on the part of the collector voltages partially cancels the decrease that occurs with the reduction in the positive supply voltage. The partially cancelled decrease in the collector voltage of transistor Q_4 is coupled directly to the base of transistor Q_8 and is transmitted by the emitter circuit of this transistor to the base of output transistor Q_{10}. At this point, the decrease in voltage is further cancelled by the increase in the collector voltage of current-sink transistor Q_9 that results from the decrease in current mentioned above.

In a similar manner, transistor Q_5 develops the compensating feedback to cancel the effects of an increase in the positive supply voltage or of variations in the negative supply voltage. Because of the feedback stabilization provided by transistor Q_5, the CA3008 and CA3010 operational amplifiers provide high common-mode rejection, have excellent open-loop stability, and have a low sensitivity to power-supply variations.

In addition to their function in the cancellation of supply-voltage variations, transistors Q_8, Q_9, and Q_{10} are used in an emitter-follower type of single-ended output circuit. The output

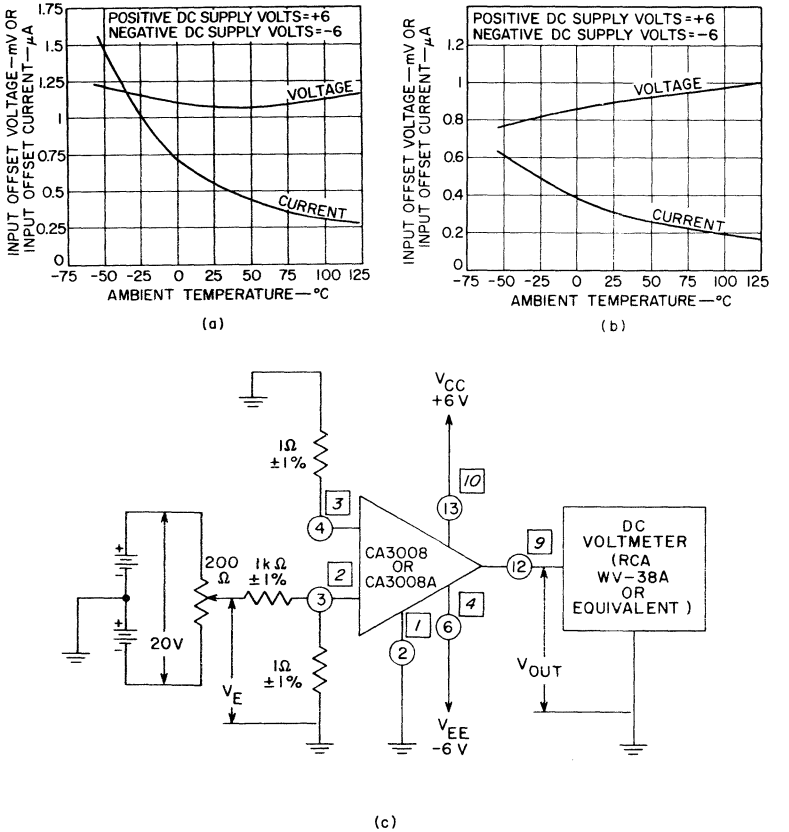
of the second differential amplifier is directly coupled to the base of transistor Q_8, and the emitter circuit of transistor Q_8 supplies the base-drive input for output transistor Q_{10}. A small amount of signal gain in the output circuit is made possible by the bootstrap connection from the emitter of output transistor Q_{10} to the emitter circuit of transistor Q_9. If this bootstrap connection were neglected, transistor Q_9 could be considered as merely a dc constant-current sink for drive transistor Q_8. Because of the bootstrap arrangement, however, the output circuit can provide a signal gain of 1.5 from the collector of differential-amplifier transistor Q_4 to the output (terminal 12). Although this small amount of gain may seem insignificant, it does increase the output-swing capabilities of the operational amplifiers.

The output from the operational-amplifier circuit is taken from the emitter of output transistor Q_{10} so that the dc level of the output signal is substantially lower than that of the differential-amplifier output at the collector of transistor Q_4. In this way, the output circuit shifts the dc level at the output so that it is effectively the same as that at the input when no signal is applied.

Resistor R_{15} in series with terminal 8 (refer to Fig. 197) increases the ac short-circuit load capability of the operational amplifier, when this terminal is shorted to terminal 12 so that the resistor is connected between the output and the negative supply.

DC Characteristics — The operational amplifiers are designed to operate from two symmetrical dc power supplies at supply voltages in the range from ±3 volts to ±6 volts. For operation with ±3-volt supplies, the power dissipation in the amplifiers is less than 7.0 milliwatts with terminal 8 open or 23 milliwatts with terminal 8 shorted to terminal 12. When ±6-volt supplies are used, the dissipation level increases to either 30 or 92 milliwatts, depending upon whether terminal 8 is open or shorted to terminal 12.

The input offset voltage for the operational amplifiers is typically 1.1 millivolts for the CA3008 and 0.9 millivolt for the CA3008A for all symmetrical supply voltages. This parameter is relatively insensitive to variations in the supply voltages. When ±6-volt supplies are used, the variation in the input offset voltage with fluctuations in supply voltage is typically less than 300 microvolts per volt for either supply. For ±3-volt supplies, the variation is typically 700 microvolts per volt. The offset voltage varies slightly with temperature as shown in Fig. 198. (Fig. 198(c) shows the schematic diagram of the special test circuit used for the offset-voltage measurements.)



Note: Pins 8 and 12 should be shorted for the pertinent power-dissipation measurement only.

Fig. 198 — Input offset voltage and input offset current as a function of temperature: (a) for CA3008; (b) for CA3008A; (c) test circuit used for offset-voltage measurements.

The input bias current and the input offset current of the amplifiers are typically 5.3 microamperes and 0.54 microampere, respectively, for the CA3008 and 2.6 microamperes and 0.31 microampere for the CA3008A when ±6-volt supplies are used. Figs. 198 and 199 show the variations in these parameters with temperature.

Gain-Frequency Response — The operational amplifiers provide a gain of 60 dB at low frequencies and have a unity-gain bandwidth of 18 MHz when operated from ±6-volt supplies. The

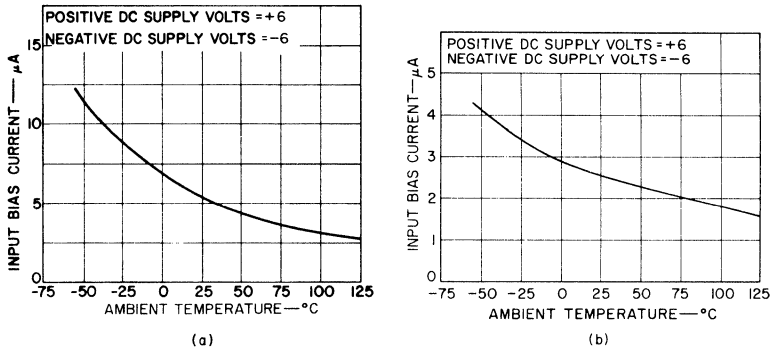


Fig. 199 — Input bias current as a function of temperature: (a) for CA3008; (b) for CA3008A.

typical gain-frequency response is shown in Fig. 200 for operation of the amplifier at −55°C, at 25°C, and at 125°C. The response of the amplifier exhibits little change over the temperature range. A typical gain-frequency characteristic for amplifiers operated from ±3-volt supplies at 25°C is shown in Fig. 201.

Transfer Characteristic — The transfer characteristic of the operational amplifiers is shown in Fig. 202. This characteristic shows that the amplifiers do not exhibit any hysteresis effect.

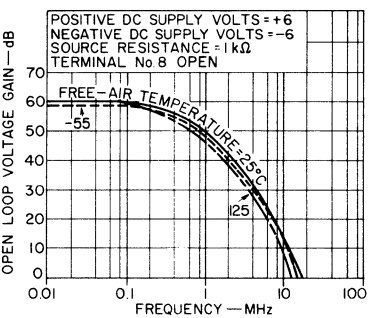


Fig. 200 — Open-loop gain as a function of frequency.

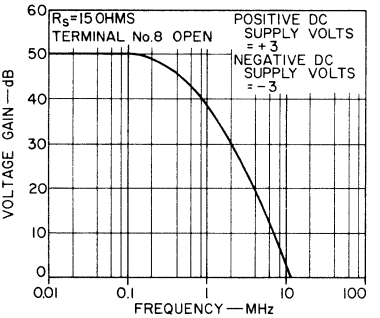


Fig. 201 — Voltage gain as a function of frequency.

Common-Mode Rejection — The common-mode rejection provided by the operational amplifiers is typically 94 dB for operation with ±6-volt supplies. Fig. 203 shows the differential-gain and common-mode gain frequency plots for the amplifiers. Fig. 204 shows the common-mode rejection as a function of frequency.

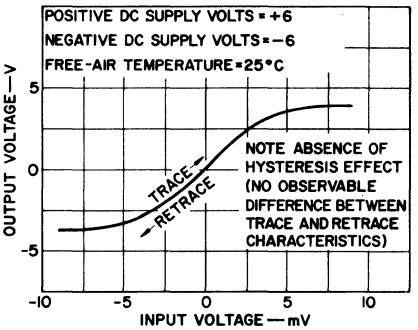


Fig. 202 — Output voltage as a function of input voltage for an open-loop operational amplifier.

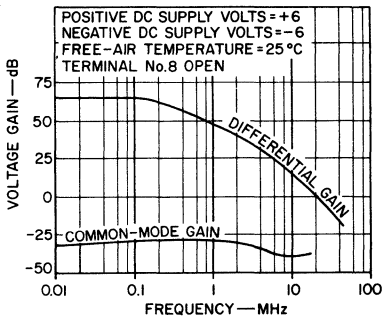


Fig. 203 — Differential and common-mode gain as a function of frequency.

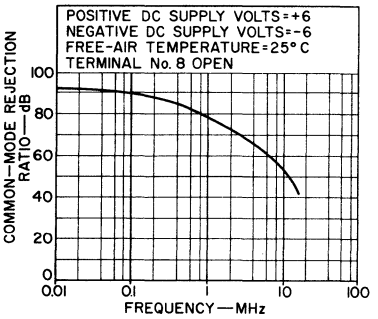


Fig. 204 — Common-mode rejection as a function of frequency.

Output Swing — The operational amplifiers exhibit a maximum dynamic-swing capability of ±3.5 volts with terminal 8 open and of ±3.0 volts with terminal 8 shorted to terminal 12. The output-swing capability varies only slightly with temperature, as shown in Fig. 205. Fig. 206 shows the variation in the output-swing capability with frequency.

Input and Output Impedances — When the CA3008 operational amplifier is operated from ±6-volt supplies, it has an input impedance of 14,000 ohms at 1 KHz and an output impedance of 200 ohms (terminal 8 open) or 75 ohms (terminal 8 shorted to terminal 12). For the same operating conditions, the CA3008A has an input impedance typically of 20,000 ohms and an output impedance of 160 ohms (terminal 8 open) or 85 ohms (terminal 8 shorted to terminal 12). The input impedance and output impedance of the amplifiers are affected by temperature as shown in Figs. 207 and 208 respectively.

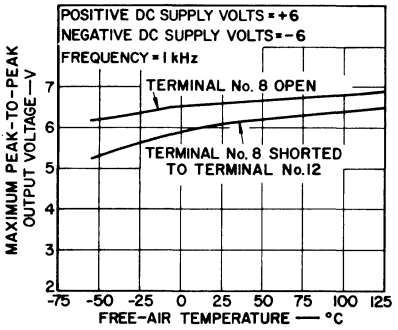


Fig. 205 — Output-swing capabilities as a function of temperature.

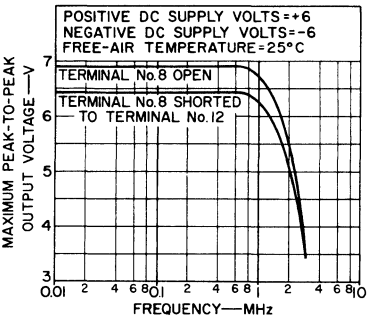


Fig. 206 — Output-swing capabilities as a function of frequency.

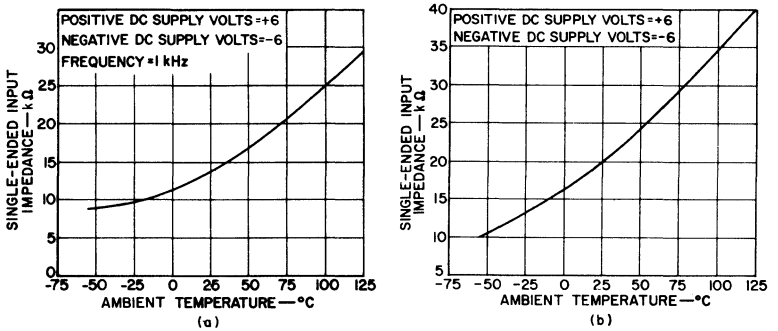


Fig. 207 — Input impedance as a function of temperature: (a) for CA3008; (b) for CA3008A.

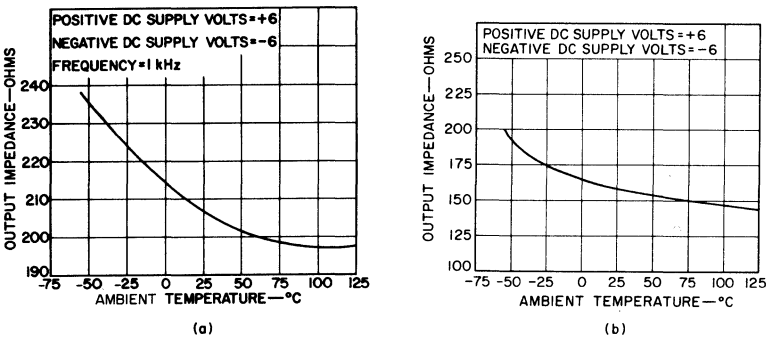


Fig. 208 — Output impedance as a function of temperature: (a) for CA3008; (b) for CA3008A.

Output-Power Capability — A choice of two output-power capabilities is provided in the operational amplifiers. The output can be tailored to the specific load requirements by leaving terminal 8 open and placing an appropriate resistor between terminals 6 and 12. The minimum safe value of load resistance (including the aforementioned resistor) is 200 ohms when ±6-volt supplies are used. In determining the output capability, it should be kept in mind that the feedback network can contribute to the output loading especially in the lower-gain configurations.

The output-power capability of the operational amplifiers can be increased by the addition of an external emitter-follower output stage or a class B push-pull output stage. The emitter-follower approach is highly inefficient from a dissipation standpoint. A class B push-pull output stage, added as shown in Fig. 209, works well in a closed-loop circuit, but is subject to thermal runaway under open-loop conditions. The thermal-runaway effect may be controlled by the introduction of a small amount of emitter degeneration in each of the push-pull transistors. The load requirements,

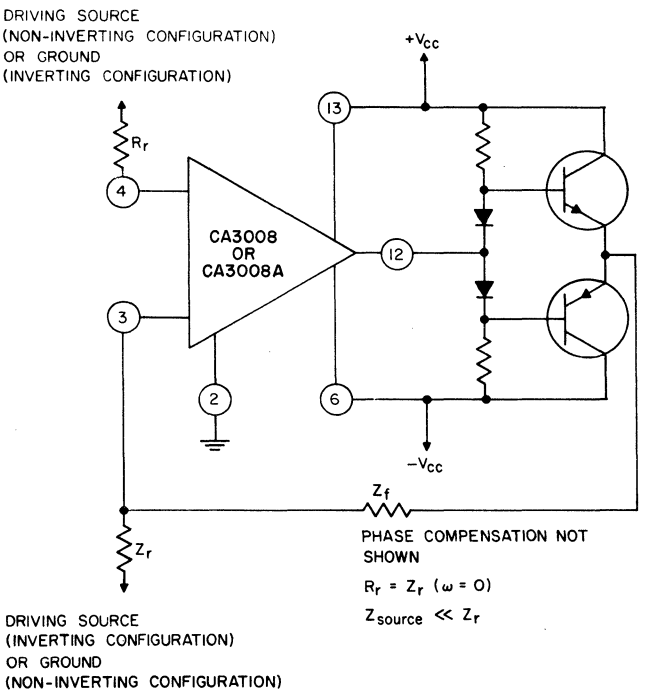
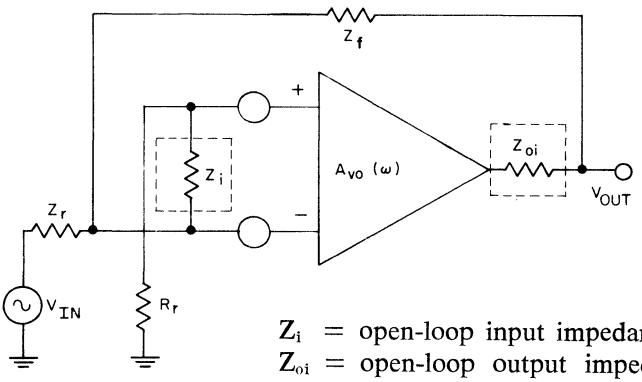


Fig. 209 — Schematic diagram showing addition of an external push-pull output stage to increase the output capability of an operational amplifier.

however, are sometimes severe enough to preclude the use of emitter degeneration. Moreover, depending on the choice of complementary transistors, the addition of the push-pull amplifier may limit the over-all bandwidth.

Phase Compensation — The response characteristics of an operational amplifier can be controlled by an external feedback circuit. Because of this feedback control, the amplifier can be used to synthesize a wide variety of transfer functions and is, therefore, useful in many diverse applications. Figs. 210 and 211 show the basic schematic diagrams for the use of the CA3008 or CA3008A operational amplifier in the inverting and noninverting feedback configurations, respectively. For convenience, the "classical" design equations for each type of configuration are repeated below the schematic diagram. In each configuration, the two inputs are returned to ground through dc paths that are effectively identical, as required to assure a minimum offset voltage.



Z_i = open-loop input impedance
Z_{oi} = open-loop output impedance
$A_o(\omega)$ = open-loop gain

$$R_r = Z_r\ (\omega = 0) /\!/ Z_f\ (\omega = 0)$$

$$\frac{V_{OUT}}{V_{IN}} = \frac{-Z_f}{Z_r + (Z_f + Z_r)/A_o(\omega)} = -\frac{Z_f}{Z_r}$$

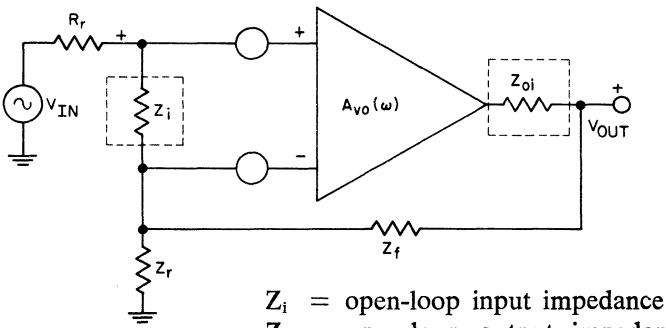
$$Z_{IN} = Z_r + \left(\frac{Z_f}{A_o(\omega)} /\!/ Z_i\right) \doteq Z_r$$

$$Z_o = Z_{oi}\,\frac{1 + \dfrac{V_{OUT}}{V_{IN}}}{A_o(\omega)} \doteq 0$$

Fig. 210 — Inverting-feedback configuration for an operational amplifier.

The open-loop input capacitance of the CA3008 and CA3008A integrated-circuit operational amplifiers is less than 10 picofarads; the frequency response of these amplifiers, therefore, is virtually independent of the drive source impedance. The input-impedance equations given in Figs. 210 and 211 indicate that this lack of dependence is even more pronounced when the amplifiers are operated with negative feedback.

In any given application of the operational amplifiers, small values of capacitance properly added to the circuit will provide the required phase compensation. When ±6-volt supplies are used, two phase-compensating networks, each of which consists of a 27-picofarad capacitor in series with a 2000-ohm resistor, connected between terminals 1 and 14 and between terminals 9 and 10, cause



Z_i = open-loop input impedance
Z_{oi} = open-loop output impedance
$A_o(\omega)$ = open-loop gain

$$R_r = Z_r\ (\omega = 0) /\!/ Z_f\ (\omega = 0)$$

$$\frac{V_{OUT}}{V_{IN}} = \frac{A_o(\omega)\ (Z_r + Z_f)}{Z_r + Z_f + Z_o\ Z_r} \doteq 1 + \frac{Z_f}{Z_r}$$

$$Z_{IN} = Z_i \left(1 + \frac{A_o(\omega)}{\frac{V_{OUT}}{V_{IN}}} \right)$$

$$Z_o = Z_{oi} \left(\frac{\frac{V_{OUT}}{V_{IN}}}{A_o(\omega)} \right)$$

Fig. 211 — Noninverting-feedback configuration for an operational amplifier.

the closed-loop response of the integrated-circuit operational amplifier to roll off at a slope of one (6 dB per octave) all the way to unity gain (where it then breaks into a slope of two). This

value of compensation is sufficient to stabilize the amplifier for all resistive-feedback applications including unity gain. The response for this value of phase compensation is compared to the original open-loop response in Fig. 212. Although the two compensating networks are sufficient to ac-stabilize the amplifier, they are not sufficient to produce a flat response (within ±1 dB) for closed-loop gains below 15 dB. Fig. 213 shows a plot of the capacitance required to produce a flat (±1-dB) gain response as a function of closed-loop gain. The capacitors must have a resistor in series with them so that $1/(2\pi RC) = 3$ MHz.

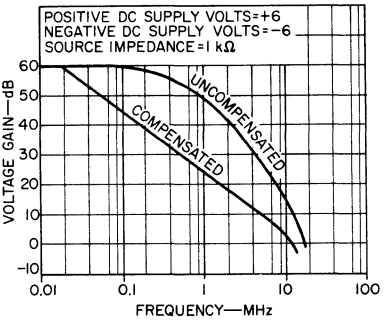


Fig. 212 — Open-loop gain as a function of frequency for both phase-compensated and uncompensated operational amplifiers.

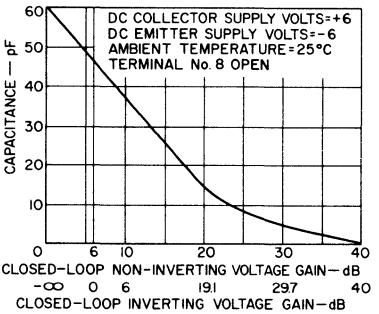


Fig. 213 — Amount of phase-compensating capacitance required to obtain a flat (±1-dB) gain-frequency response.

Phase compensation may also be effected conventionally by adding a capacitor in series with a resistor between terminal 11 and ground. A 0.02-microfarad capacitor in series with a 22-ohm resistor is sufficient to ac-stabilize the integrated-circuit operational amplifier at resistive closed-loop gains down to unity.

The required phase compensation depends upon the feedback configuration and not upon the location of the drive source. Hence, phase-compensating networks that provide sufficient compensation for a 10-dB noninverting configuration also provide sufficient compensation for a 6-dB inverting configuration because the two feedback configurations are identical.

Video Amplifiers — When the feedback is applied through a purely resistive network and suitable phase compensation is employed, flat gains are attainable from the operational amplifiers. Fig. 214 shows a 30-dB noninverting configuration of a video amplifier, together with the closed-loop response of the circuit. The phase compensation is provided by a 5-picofarad capacitor in series

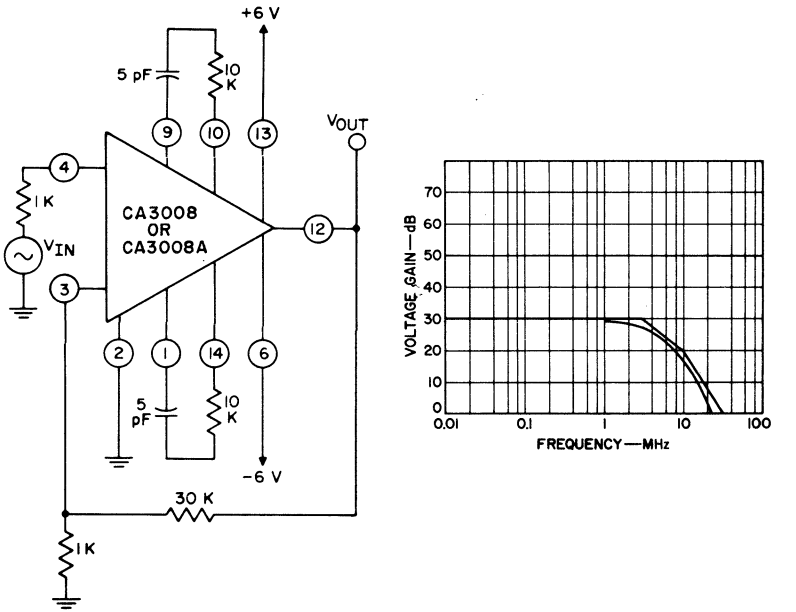


Fig. 214 — Circuit diagram and closed-loop response of a noninverting type of operational amplifier used as a 30-dB video amplifier.

with a 10,000-ohm resistor. This arrangement provides the required amount of compensation, as predicted in Fig. 213. (For purposes of comparison, the uncompensated response of the 30-dB configuration is shown in Fig. 215. Observe the 13-dB peaking effect at 4.5 MHz.) An alternate method of phase compensation may be used when the intersection of the closed-loop characteristic and the open-loop response occurs in a two-slope region. The technique is to cause the feedback ratio (Z_f/Z_r) to roll off at a slope of one. Fig. 216 illustrates this alternate technique for the 30-dB gain circuit.

The low-frequency input impedance of the 30-dB noninverting configuration is 480,000 ohms, as calculated from the appropriate equation in Fig. 178 (Z_i = 14,000 ohms).

Fig. 217 shows the configuration and the response of a 6-dB inverting type of video amplifier. The intersection of the closed-loop characteristic with the compensated open-loop response predicts the 3-dB bandwidth of the video amplifier provided the transfer phase shift of the open-loop amplifier is approximately −90 degrees. This relationship suggests a way to extend the bandwidth without peaking. In the 6-dB video amplifier shown in Fig.

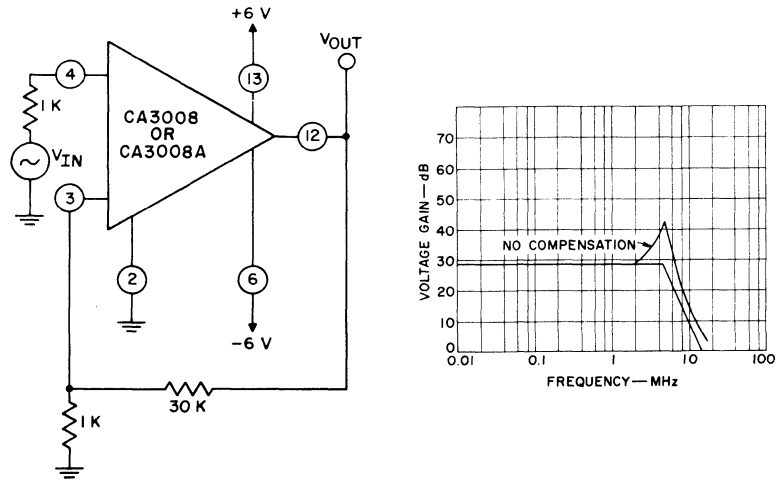


Fig. 215 — Circuit diagram and gain-frequency response of the 30-dB noninverting video amplifier operated without phase compensation.

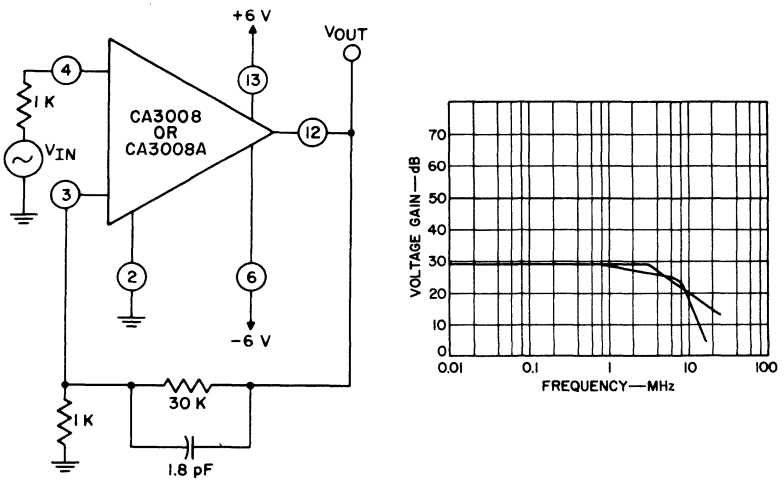


Fig. 216 — Circuit diagram and gain-frequency response of the 30-dB video amplifier when phase compensation is accomplished by addition of a capacitor in parallel with the feedback resistor.

218, the 3-dB bandwidth has been increased from 5.6 to 11 MHz by a decrease in the value of the phase-compensating capacitors from 56 to 33 picofarads.

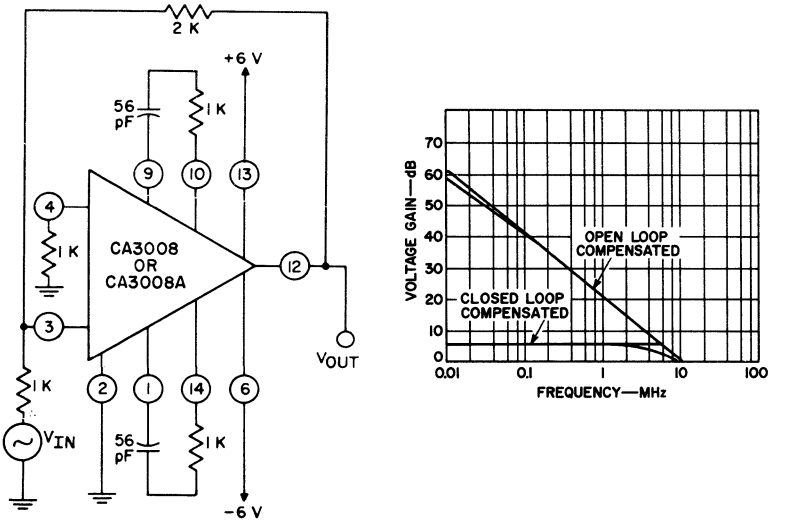


Fig. 217 — Circuit diagram and closed-loop response of an inverting type of operational amplifier used as a 6-dB video amplifier.

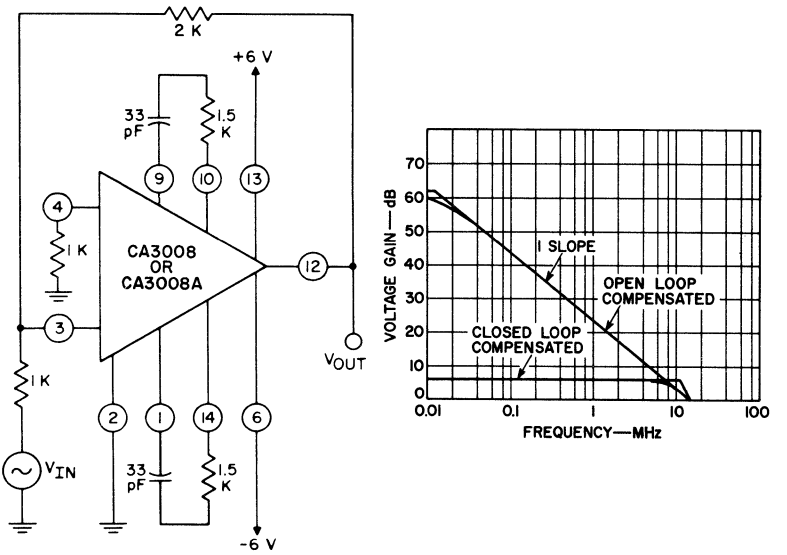
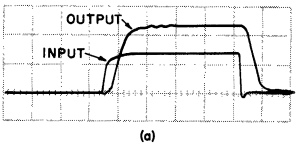


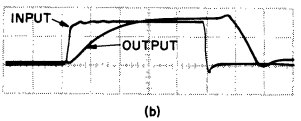
Fig. 218 — Effect of a decrease in phase-compensating capacitance from 56 picofarads to 33 picofarads on the response of the 6-dB video amplifier.

Because a broad-band amplifier should be capable of handling digital signals, data were taken to determine this capability. Figs. 219(a) and 219(b) illustrate the pulse-handling capabilities of the 30-dB noninverting circuit shown in Fig. 214. Fig. 219(a) shows the low-level (non-saturating) pulse response. The input is a 38-millivolt, 960-nanosecond pulse; the output is a 1.1-volt pulse having a 40-nanosecond delay time, a zero storage time, and 125-nanosecond rise and fall times. Fig. 219(b) shows the response of the amplifier for a 960-nanosecond input pulse under 20-dB overdrive conditions. The output pulse has an amplitude of 3.2 volts, a delay time of 32 nanoseconds, a storage time of 160 nanoseconds, a rise time of 500 nanoseconds, and a fall time of 160 nanoseconds.



Low-Level Pulse

$V_{IN} = 38$ mV
$V_{OUT} = 1.1$ V
$t_d = 40$ ns
$t_s = 0$ ns
$t_r = t_f = 120$ ns



Overdriven Pulse

$V_{IN} = 1.27$ V
$V_{OUT} = 3.2$ V
$t_d = 32$ ns
$t_s = 160$ ns
$t_r = 500$ ns
$t_f = 160$ ns

Note:

t_d = DELAY TIME
t_s = STORAGE TIME
t_r = RISE TIME
t_f = FALL TIME

Fig. 219 — Pulse-handling characteristics of the noninverting 30-dB video amplifier: (a) low-level pulse response; (b) pulse response under overdrive conditions.

Frequency-Shaping Amplifiers — The operational amplifiers may be used to create simple frequency-shaped characteristics, such as those associated with band-pass, notched-response, and single-tuned narrow-band amplifiers.

Fig. 220 shows a noninverting amplifier that may be used to synthesize the following peaked-response transfer function:

$$\frac{V_{OUT}}{V_{IN}} = +10\,\frac{\left(1+j\frac{f}{f_1}\right)\left(1+j\,\frac{f}{f_4}\right)}{\left(1+j\,\frac{f}{f_2}\right)\left(1+j\frac{f}{f_3}\right)} \qquad (201)$$

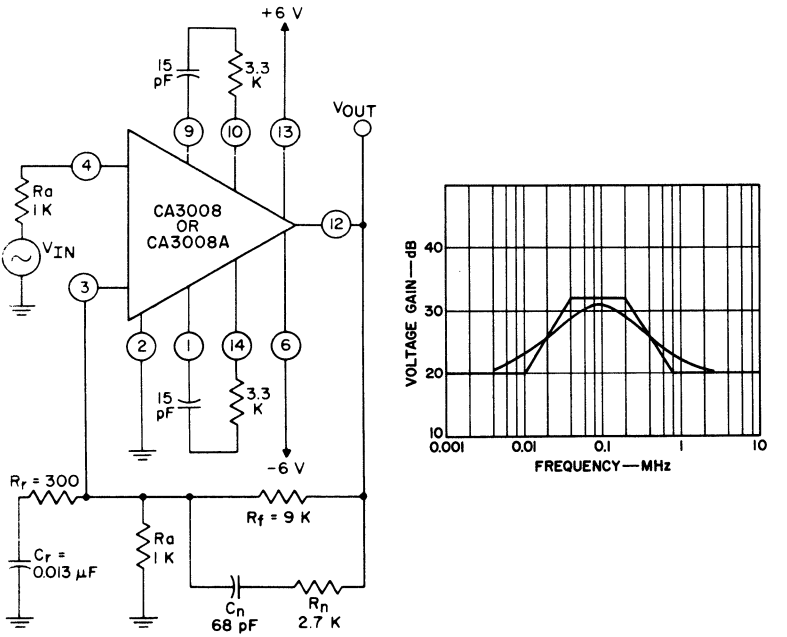


Fig. 220 — Circuit diagram and response of a noninverting type of operational amplifier used to synthesize peaked-response transfer functions.

In terms of the notations employed in Fig. 220, the break-frequency equations for the amplifier may be expressed as follows:

$$f_1 = \frac{10}{2\pi C_r(R_f + 10R_r)} = 10 \text{ kHz} \qquad (202)$$

$$f_2 = \frac{1}{2\pi C_r R_r} = 40 \text{ kHz} \qquad (203)$$

$$f_3 = \frac{1}{2\pi C_n(R_n + R_f)} = 200 \text{ kHz} \qquad (204)$$

$$f_4 = \frac{40}{2\pi C_n(40R_n + R_f)} = 800 \text{ kHz} \qquad (205)$$

These break-frequency equations are the precise equations derived from the gain equation in Fig. 211. The amount of phase compensation required is that shown in Fig. 213 for a noninverting gain of 20 dB.

Fig. 221 shows the circuit configuration and the frequency response of a narrow-band, 100-KHz tuned amplifier. The circuit Q is 33.3. A true single-tuned response can be obtained from only

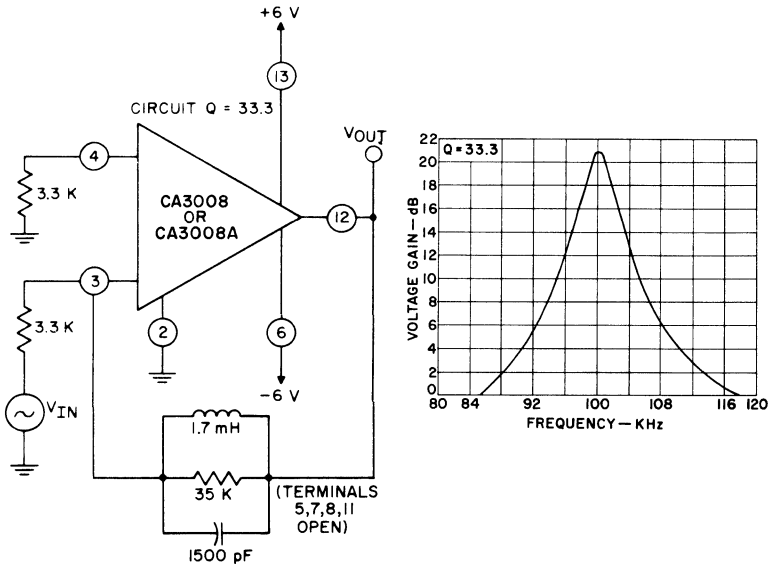


Fig. 221 — Circuit diagram and response of an inverting type of operational amplifier used as a narrow-band 100-kHz tuned amplifier.

an inverting circuit configuration, as shown by the gain equation for the two types of configurations given in Figs. 210 and 211 and repeated below:

1. For the inverting configuration, the gain equation is given as:

$$\frac{V_{OUT}}{V_{IN}} = -Z_r/Z_r$$

2. For the noninverting configuration, the following gain equation is used:

$$\frac{V_{OUT}}{V_{IN}} = 1 + Z_r/Z_r$$

The "1+" term in the gain expression for the noninverting configuration indicates that the gain of this type of circuit will never decrease to zero as required for a true single-tuned response. The amount of phase compensation required for the narrow-band 100-kHz amplifier is the value given in Fig. 213 for an inverting gain of 0.0 (infinite attenuation).

Comparators — The CA3008 and CA3008A operational amplifiers have excellent transfer characteristics for comparator appli-

cations. As shown in Fig. 202, the amplifiers have no observable hysteresis effect; the trace (minus to plus) and retrace (plus to minus) excursions coincide.

Integrators — The important design consideration when an operational amplifier is to be used as an integrator is that dc feedback be provided. This feedback is necessary so that an offset (error) voltage cannot continuously charge the feedback capacitor until the amplifier limits. The required dc feedback is normally provided by shunting the integrating capacitor with a resistor so that the resulting time constant is substantially longer than the periods for the frequencies of interest. Fig. 222 shows the circuit configuration for the use of the CA3008 or CA3008A operational amplifier as an integrator and the responses of the circuit for 1-kHz square-wave inputs. The dc gain of the circuit is limited to 20 dB by the 390,000-ohm feedback resistor. The effect of this resistor on the gain, however, becomes negligible for ac signals at frequencies above 13 Hz because of the 0.03-microfarad capacitor in parallel with it. The weighting factor of integration for the circuit is about 1 millisecond (R = 39,000 ohms; C = 0.03 microfarad).

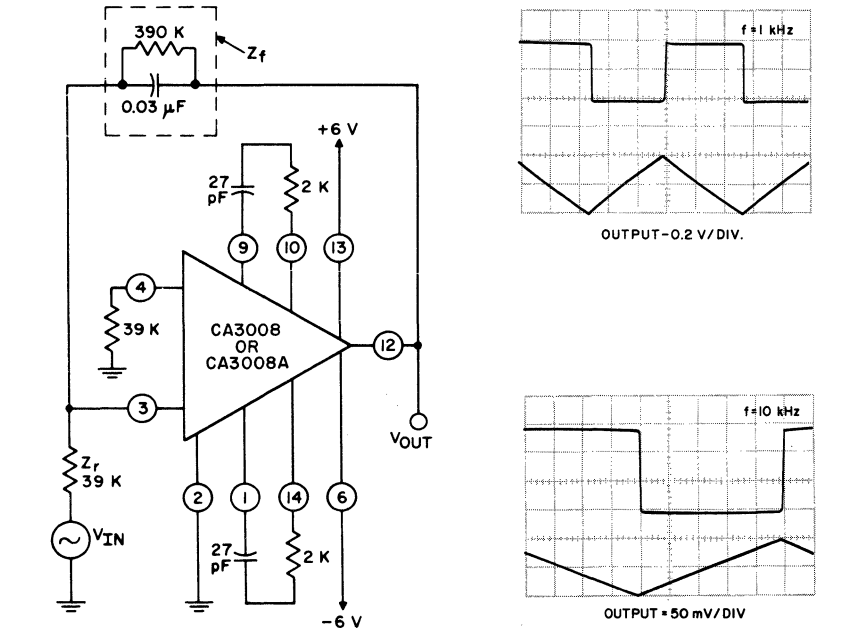


Fig. 222 — Circuit diagram and the input and output waveforms for an operational amplifier used as an integrator.

Phase compensation must also be provided in an integrating amplifier circuit to assure ac stability. In general, the amount of compensation required is the maximum value given by Fig. 213, because the closed-loop characteristic of the integrator has rolled off completely at the frequency where the intersection of the open-loop response and the closed-loop characteristic occurs.

Differentiators — The main problem in the design of differentiating amplifiers is that the gain of such amplifiers increases with frequency; hence, they are susceptible to high-frequency noise. The classical remedy for this effect is to connect a small resistor in series with the input capacitor so that the high-frequency gain is decreased. Actually, the addition of the resistor results in a more realistic model of a differentiator because a resistance is always added in series with the input capacitor by the source impedance. The schematic diagram of a CA3008 or CA3008A operational amplifier used as a differentiating circuit and the response of the circuit for 1-kHz square waves are shown in Fig. 223. A value of 51 ohms is selected for the gain-limiting resistor to illustrate that the effect of the source impedance is not necessarily negligible in differentiator applications. This 51-ohm resistor limits the high-frequency numerical gain factor of the amplifier to 433.

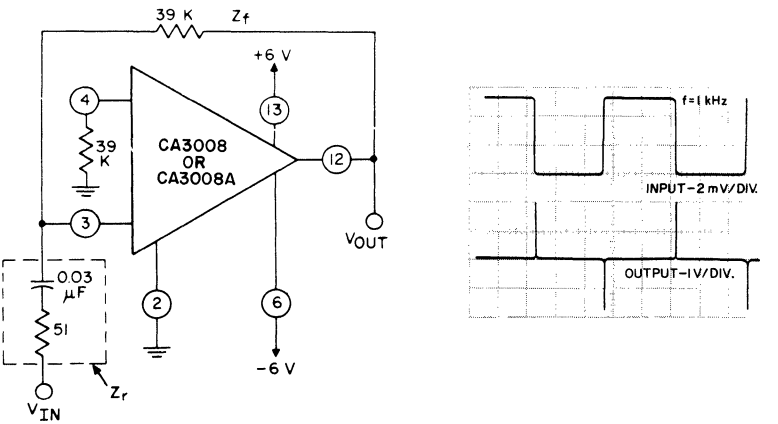


Fig. 223 — Circuit diagram and the input and output waveforms for an operational amplifier used as a differentiator.

If the closed-loop gain of a differentiator rises to the open-loop value before the open-loop response has started to roll off, no phase compensation of the circuit is required. In order to assure that the intersection of the closed-loop characteristic with the

open-loop response occurs at a slope less than two, the RC time constant of the phase-compensating network must be adjusted so that open-loop response does not roll off in the region of the intersection.

Scaling Adders — The inverting feedback configuration of the operational amplifiers lends itself not only to summing several different signals, but also to weighting each signal to be summed. The weighting operation is possible because the virtual ground that exists at the junction of the feedback resistor and the inverting input (terminal 3) isolates each signal channel from the others. The weighting operation requires that each input signal enter the virtual-ground node through an impedance of such value that its ratio to the feedback impedance is equal to the desired weighting factor.

Fig. 224 illustrates the use of the CA3008 or CA3008A operational amplifier as a scaling adder (weighting amplifier). This figure also shows the output waveform. The minimum phase compensation needed for this circuit is that required for the gain obtained when a single signal drives all the input channels in parallel.

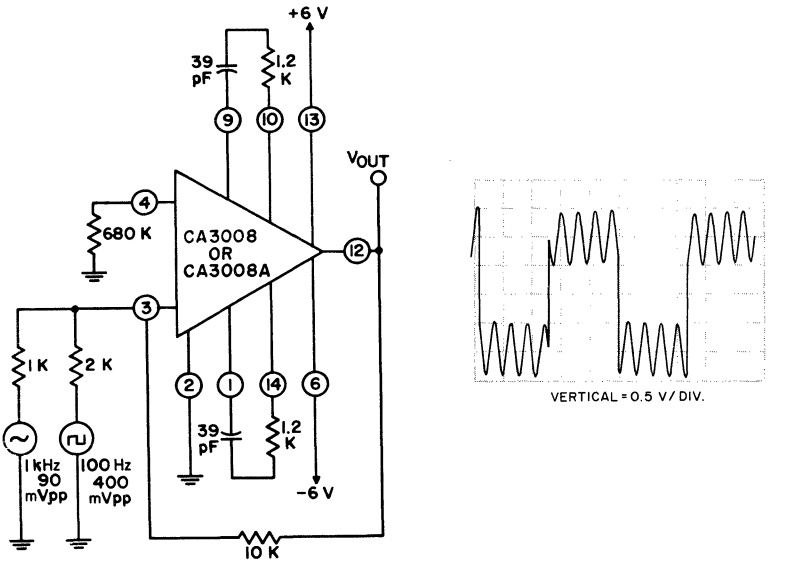


Fig. 224 — Circuit diagram and output waveform for an operational amplifier used as a scaling adder.

±12-Volt Types

The **CA3015** and **CA3015A,** the **CA3016** and **CA3016A,** the **CA3030** and **CA3030A,** and the **CA3038** and **CA3038A** opera-

tional amplifiers are identical in circuit configuration to the ±6-volt types discussed previously, but have improved device breakdown voltage that permits operation from 12-volt supplies. Operation of these types from power supplies of ±6 volts or ±3 volts is the same as for the lower-voltage types. This section describes the operating characteristics of the operational amplifiers at ±12 volts and discusses applications that take advantage of the higher gain-bandwidth product and increased output signal swing obtained at the higher voltages. (The circuit configuration of the CA3033 differs from that of the other ±12-volt types, and this circuit is discussed together with the CA3033A in a later section.)

Fig. 225 shows the schematic diagram and terminal numbers for the ±12-volt operational amplifiers. The numerals enclosed in squares are the terminal designations for the 12-terminal CA3015 and CA3015A circuits. As in the case of the ±6-volt types, each operational amplifier consists basically of two differential amplifiers and a single-ended output stage in cascade. Throughout the following discussion, terminal numbers referred to in the text or shown on illustrations are those for the 12-terminal CA3015 or CA3015A circuit; the corresponding terminals for the 14-terminal circuits can be determined from the schematic in Fig. 225.

DC Characteristics — When operated from ±12-volt power supplies, the operational amplifiers have a typical dissipation of 175 milliwatts with terminal 5 open. If terminals 5 and 9 are shorted, higher output-current capability can be achieved, but the dissipation increases to a typical value of 500 milliwatts. The input offset voltage for the CA3015, CA3016, CA3030, and CA3038 is typically 1.4 millivolts, and the variation in input offset voltage is typically less than 200 microvolts per volt for fluctuations in either supply voltage. At 25°C, the input bias current and the input offset current for these types are typically 9.6 and 1 microamperes, respectively. For the "A"-version types, the input offset voltage is typically 1 millivolt, and the variation in this voltage is typically less than 200 microvolts per volt for fluctuations in either supply voltage. At 25°C, the input bias current and input offset current for the "A"-version types are typically 4.7 and 0.5 microamperes, respectively. (Curves of input offset voltage, input bias current, and input offset current for the ±12-volt operational amplifiers are given in the technical bulletin on these types.)

When the ±12-volt operational amplifiers are operated from ±12-volt supplies with terminals 5 and 9 shorted for greater output capability, the power dissipation is high enough so that tem-

perature derating is necessary. The maximum junction-temperature rating is 150°C, and the thermal resistance is 100°C per watt. The maximum power-dissipation rating is 600 milliwatts at 25°C (with terminals shorted as described above). In this higher-output mode. the circuits can operate safely at ambient temperatures up to 90°C.

AC Characteristics — The open-loop transfer characteristic for the ±12-volt operational amplifiers is shown in Fig. 226. As in the case of the ±6-volt operational amplifiers, there is no hysteresis effect. The technical bulletins on the ±12-volt operational amplifiers include curves of maximum peak-to-peak voltages as functions of load resistance with terminal 5 open and with terminals 5 and 9 shorted. The operational amplifiers can drive a low-resistance load when these terminals are shorted.

The open-loop low-frequency gain of the operational amplifiers with ±12-volt supplies is typically 70 dB with a 3-dB bandwith of 320 kHz. The unity-gain crossover occurs at a frequency of 58 MHz.

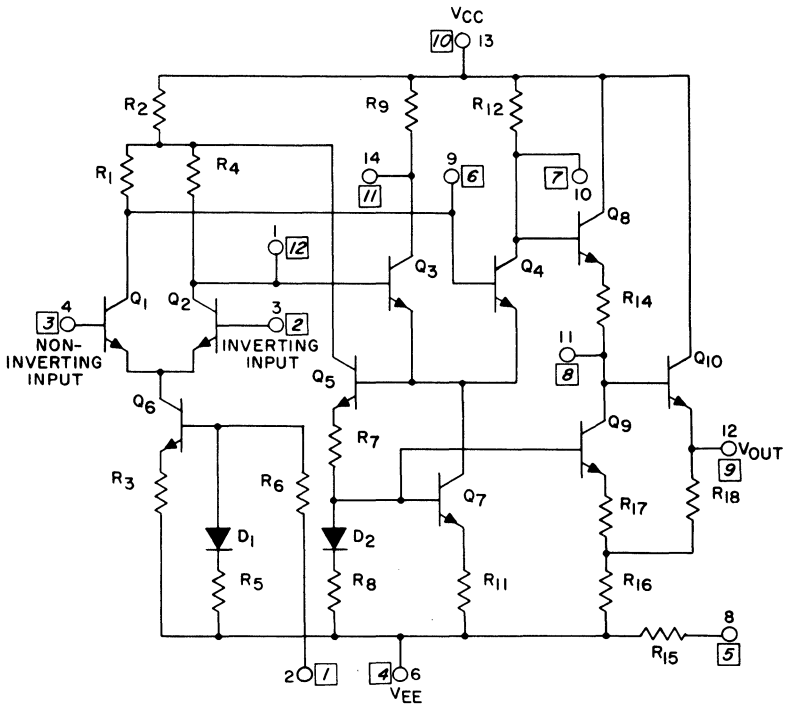


Fig. 225 — Schematic diagram for the ±12-volt operational amplifiers (CA3015, CA3015A, CA3016, CA3016A, CA3030, CA3030A, CA3038, and CA3038A).

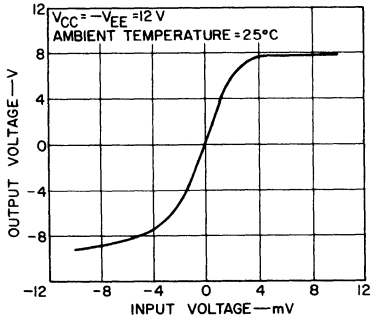


Fig. 226 — Open-loop transfer characteristics.

The common-mode rejection ratio of the operational amplifiers is typically 104 dB for operation with ±12-volt supplies. A curve of common-mode rejection ratio as a function of frequency is included in the technical bulletin.

The technical bulletins for the ±12-volt operational amplifiers include curves of input and output impedances as functions of temperature. At 25°C, the typical input impedance is 7800 ohms for the CA3015 and 10,000 ohms for the CA3015A. The typical output impedance of the CA3015 is 92 ohms with terminal 5 open, and 76 ohms with this terminal connected to the output. The output impedance of the CA3015A is typically 85 ohms with terminal 5 open and 78 ohms with this terminal connected to the output.

Phase Compensation — When the operational amplifiers are operated from ±6-volt supplies, the phase-compensation techniques described previously for the ±6-volt types are applicable. Fig. 227 shows the various phase-compensation techniques for the CA3015 or CA3015A. When the CA3015 or CA3015A is operated from ±12-volt supplies, corrections must be made in the phase-lag compensation to allow for the shift in frequency at which the second break in the open-loop response occurs. At ±12 volts, this second break occurs at a frequency of 10 MHz. For Miller-effect and conventional phase-lag compensation, the series RC combinations must be adjusted so that $1/(2\pi RC) = 10$ MHz to correct for the shift in frequency. In addition, the Miller technique requires a larger value of phase-lag capacitance for a non-peaking (±1 dB) response to allow for the higher gain.

Fig. 228 shows a curve of the required phase-lag capacitance as a function of gain, together with the corresponding response curves. (The required capacitance values shown in this figure are

applicable not only for ±12-volt power supplies, but also for all lower-voltage symmetrical supplies; however, smaller capacitors could be used at lower voltages.)

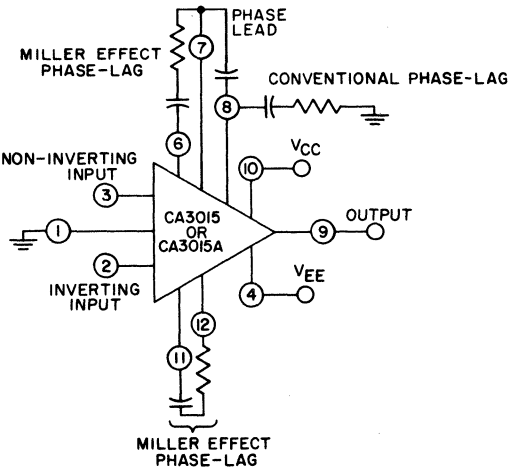


Fig. 227 — Terminal connections for phase-lag and phase-lead compensation of the CA3015 or CA3015A.

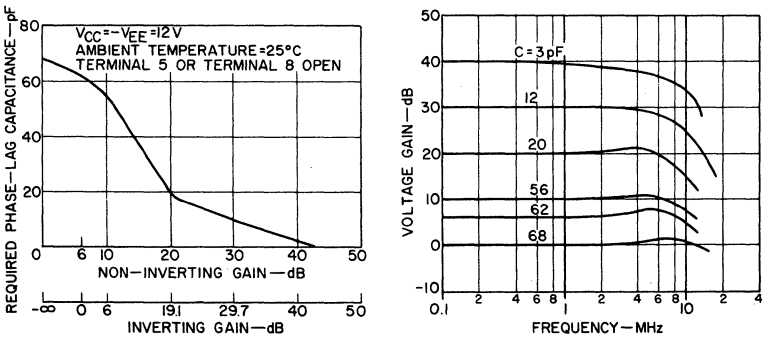


Fig. 228 — Amount of phase-lag capacitance required to obtain a flat (±1-dB) response and typical response characteristics.

Fig. 229 shows curves of open-loop compensated and uncompensated frequency response with ±12-volt supplies. Although the phase-lag compensation capacitance of 18 picofarads shown in curve (B) of this figure is sufficient to provide stability in resistive-feedback amplifiers down to unity gain, it is not sufficient to provide flat closed-loop response (±1 dB) below 20 dB.

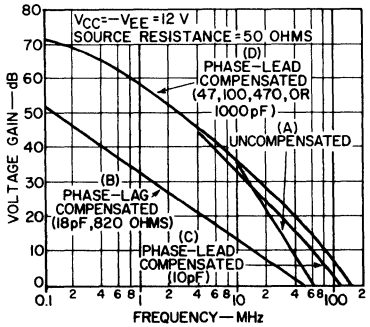


Fig. 229 — Open-loop gain as a function of frequency for compensated and uncompensated operational amplifiers.

In addition to the standard phase-lag compensation discussed above, the ±12-volt operational amplifiers have a phase-lead compensation capability. For this phase-lead compensation, a capacitor is connected between terminals 7 and 8 of the CA3015 or CA3015A, as shown in Fig. 227. The effect of this capacitor is to eliminate the break at 10 MHz in the open-loop response and thus extend the 6-dB-per-octave roll-off. The second break in the response then occurs at approximately 35 MHz, and the unity-gain crossover occurs at 150 MHz. The phase-lead compensated open-loop response is shown in curves (C) and (D) of Fig. 229 for various values of capacitance. For optimum performance, a minimum phase-lead capacitance of 47 picofarads is recommended.

For flat (±1 dB) responses at closed-loop gains below 30 dB, a small amount of phase-lag compensation is required in addition to the phase-lead compensation. The required phase-lag capacitance for flat (±1 dB) responses and the corresponding response curves are shown in Fig. 230. When phase-lead compensa-

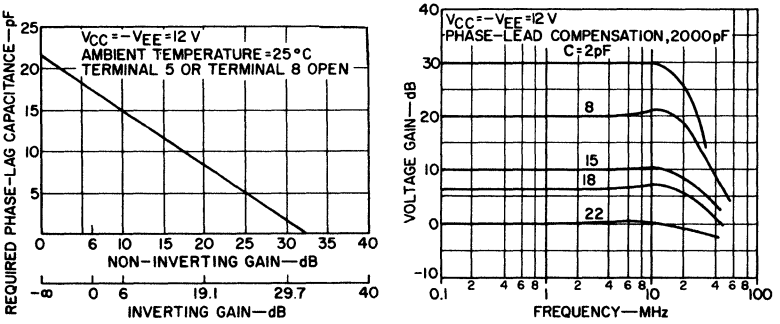


Fig. 230 — Amount of phase-lag capacitance required to obtain a flat (±1-dB) response when phase-lead compensation is used, and typical response characteristics.

tion is used, the series RC combinations should be adjusted so that $1/(2\pi RC) = 35$ MHz.

The phase-lead compensation is also applicable when ±6-volt power supplies are used, and provides a unity-gain crossover improvement of about one octave as compared to the uncompensated connection. As mentioned earlier, the phase-lag capacitance requirement for ±12-volt supplies shown in Fig. 228 is satisfactory for ±6-volt supplies, although smaller capacitors could be used with the lower voltages.

50-db Amplifier — Fig. 231 shows the circuit configuration and frequency response for a non-inverting, 50-dB amplifier em-

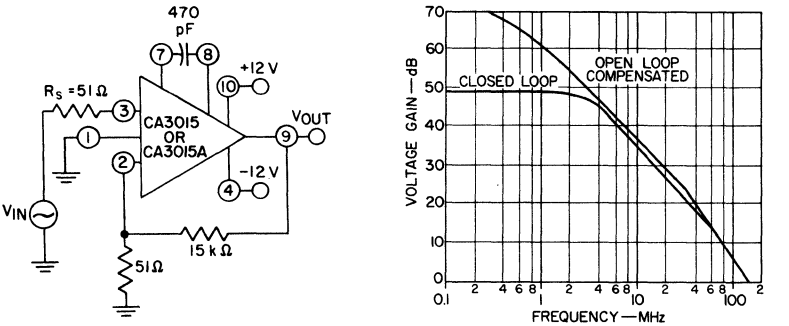


Fig. 231 — Circuit diagram and response for a 50-dB noninverting operational amplifier with phase-lead compensation.

ploying phase-lead compensation. This amplifier has a 3-dB bandwidth of 3.5 MHz, and a unity-gain crossover at 150 MHz.

10-dB, 42-MHz Amplifier — Fig. 232 shows the circuit diagram and frequency response for a 10-dB, non-inverting amplifier employing both phase-lead and phase-lag compensation. Slight peaking (2 dB) occurs for the phase compensation shown. Flat response with bandwidth reduction to 25 MHz may be obtained by use of a phase-lag capacitance of 15 picofarads.

Twin-T Bandpass Amplifier — Fig. 233 shows the circuit diagram and frequency response of a bandpass amplifier using a twin-T network in the feedback loop. The difference in resonant frequency between the bandpass-amplifier response and the twin-T network response is caused by device capacitances and loading effects. The unloaded Q (Q_O) of the twin-T network is 14.4; the Q_O of the bandpass amplifier is 12.8.

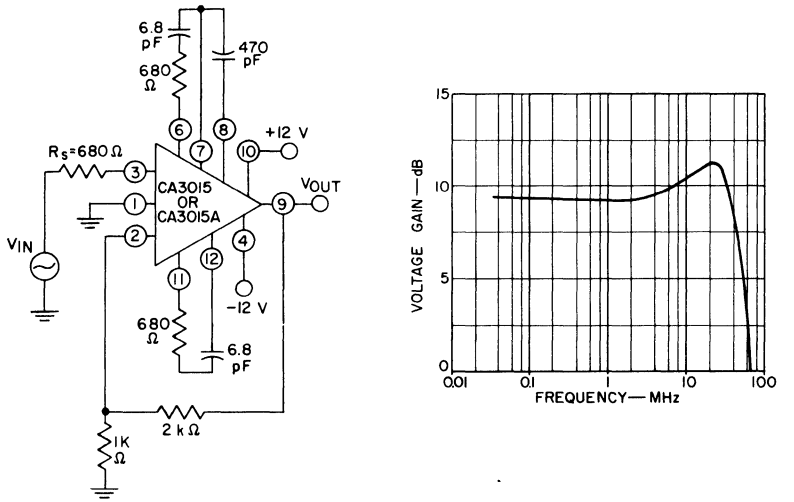


Fig. 232 — Circuit diagram and response for a 10-dB noninverting operational amplifier with phase-lead and phase-lag compensation.

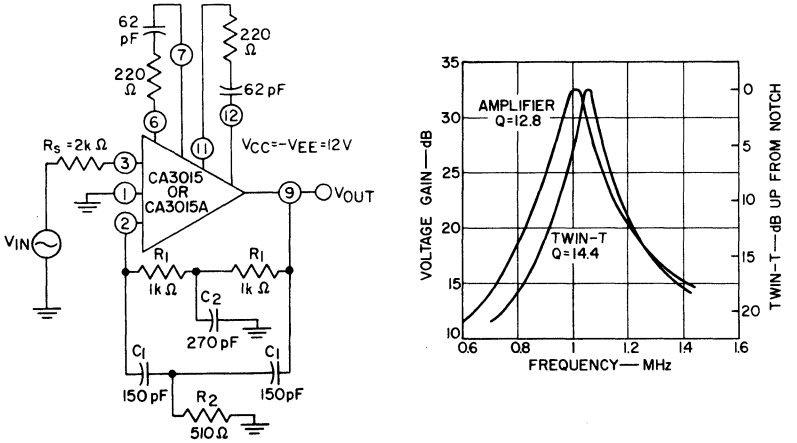


Fig. 233 — Circuit diagram and response for a band-pass amplifier using a twin-T network.

The symmetrical twin-T network can be designed by use of the following equations:

$$R_1 = 2\ R_2 \tag{206}$$

$$C_1 = \tfrac{1}{2}\ C_2 \tag{207}$$

$$f_0 = 1/(2\pi R_1 C_1) \tag{208}$$

It is important in the design of this type of bandpass amplifier that the two inputs be returned to ground through equal resistances; in this case a value of 2000 ohms is used.

20-dB, 10-MHz Bandpass Amplifier — Fig. 234 shows the circuit diagram and frequency response of an RLC bandpass amplifier. This amplifier is designed to have a Q_O of about 10 ($R_p = X_c\ Q_O = 2200$ ohms) and a gain of about 20 dB at resonance (2200/200 = 11, or 20.9 dB). In this application, the inputs are effectively grounded.

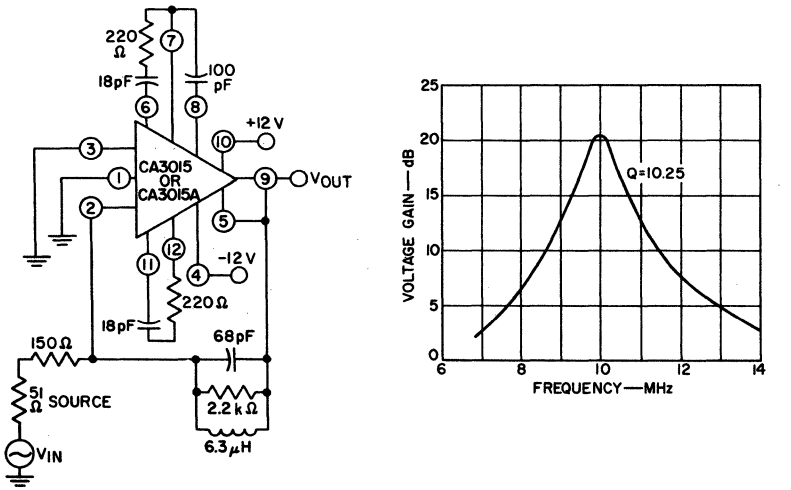


Fig. 234 — Circuit diagram and response for a 10-MHz band-pass amplifier.

Voltage Follower — A voltage follower is a non-inverting, unity-gain amplifier used primarily to transform from a high impedance to a low impedance. Because low voltages are usually associated with high-impedance sources, the voltage follower need not have a great voltage capability.

Fig. 235 shows the circuit diagram for a voltage follower using the CA3015 or CA3015A together with a curve of maximum undistorted output voltage as a function of load resistance. When terminals 5 and 9 are shorted, the voltage follower is capable of transforming a 3.4-volt peak-to-peak voltage from a 100,000-ohm source to a 470-ohm load.

If higher voltage-swing capability is desired, the positive supply voltage (V_{CC}) may be increased. Temperature derating may be necessary, depending on the magnitude of V_{CC} and whether the high- or low-current mode is used.

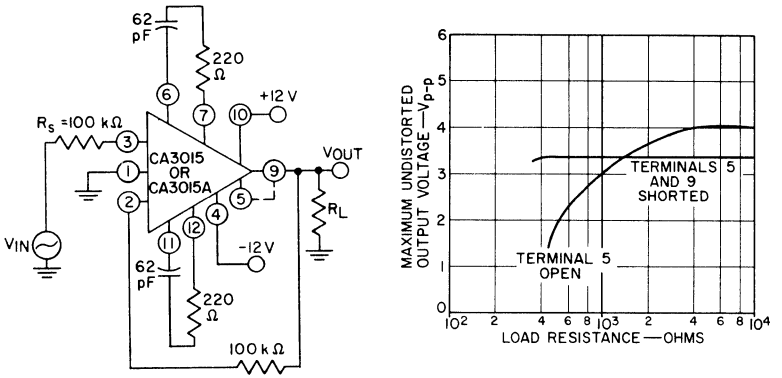


Fig. 235 — Circuit diagram for a voltage follower driven from a 100,000-ohm source, and curve showing maximum undistorted output voltage as a function of load resistance.

CA3033 and CA3033A Types

The **CA3033** and **CA3033A** integrated-circuit operational amplifiers have improved device breakdown voltages that permit operation from dual 12- and 18-volt dc power supplies, respectively. Fig. 236 shows the schematic diagram for these circuits.

The modified-Darlington inputs provide isolation and improve frequency response. The isolation is afforded by the very high ac input impedance and the very low base bias current of these units. Frequency response is improved because the effective source impedance of the preceding circuitry is divided by the h_{fe} of the input transistor (Q_1, Q_2, Q_{19} or Q_{20}).

By deriving the base bias for transistor Q_8 from the emitter circuitry of feedback transistor Q_5, an additional common-mode negative-feed back path is obtained. A common-mode signal appearing at the collectors of the first stage (Q_3 and Q_4) is reflected to the coupled emitter of the second stage (Q_6 and Q_7), where it is sampled by Q_5 and applied through its emitter circuitry to the base of the constant-current-sink transistor Q_8 of the first stage. Transistor Q_8 then causes a common-mode change in the bias current of the first stage so that the actuating common-mode signal is attenuated. The results are improved common-mode rejection and power-supply stability.

The third (output) stage of the CA3033 or CA3033A provides signal gain, an efficient high-power-output drive, and a shift in the dc level reference from the quiescent voltage of the second stage to zero or ground reference.

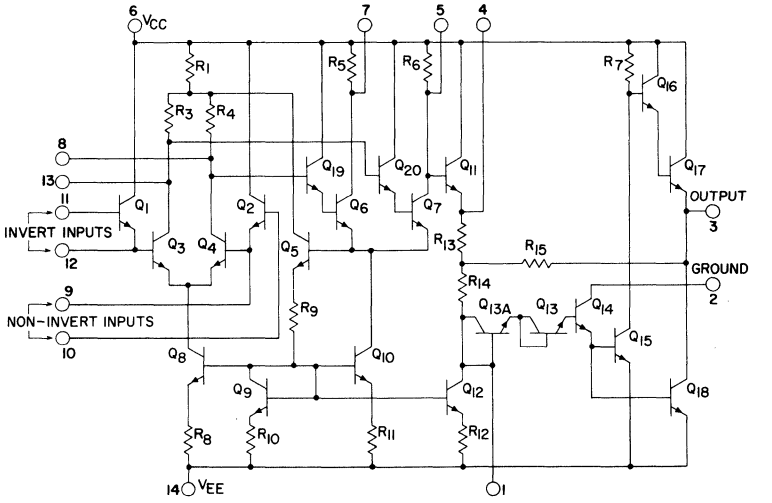


Fig. 236 — Schematic diagram of the CA3033 or CA3033A integrated-circuit operational amplifier.

If the feedback supplied by resistor R_{15} is neglected, the signal from the second stage is injected into the base of common-collector transistor Q_{11}. Constant-current-sink transistor Q_{12} and the emitter circuitry of Q_{11} shift the dc reference (with very little attenuation) to a dc level that is appropriate for driving the succeeding circuitry. Signal attenuation is minimized by the high input impedance of the succeeding circuitry and by the high output impedance of Q_{12}.

The signal appears at the base of modified-Darlington transistor Q_{14} through the forward-biased diode-connected transistors Q_{13} and Q_{13A}. Transistor Q_{14} drives inverting transistor Q_{15} and output transistor Q_{18} in parallel. Transistor Q_{14} provides impedance transformation, multiplying the parallel combination of the input impedances of Q_{15} and Q_{18} by $1 + h_{fe}$. Its prime function, therefore, is to provide the high input impedance required by the level-shift circuitry for minimum ac attenuation. It also increases the frequency response somewhat by offering a low-impedance source to transistors Q_{15} and Q_{18}.

Transistor Q_{18} is the output transistor for the negative signal excursions. Its gain is equal to its transconductance (g_m) multiplied by the load impedance applied. Transistor Q_{15} provides inversion and gain for the positive signal channel. It also presents the negative portion of the signal to the input of the positive output transistors in order to insure that they are in cutoff while the negative channel is conducting.

The most significant function of transistor Q_{15} is to provide idle current bias for output transistors Q_{17} and Q_{18}. It accomplishes this by virtue of its V_{BE} voltage drop shunting that of transistor Q_{18}. If transistors Q_{15} and Q_{18} are ideally matched, their collector currents will be equal. Hence, the collector current of transistor Q_{15} determines the idle current of the output transistors. Furthermore, the collector current of Q_{15} is limited by the power supply voltage levels and the size of resistor R_7. The maximum value of the collector current has been designed so that thermal runaway of output transistors Q_{17} and Q_{18} does not occur with power supply values up to ± 24 Vdc.

Modified-Darlington transistor Q_{16} provides impedance transformation of resistor R_7 so that it does not limit the positive output swing under high-load-current conditions. The impedance that effectively appears in series with the load is divided by the $1 + h_{fe}$ of two transistors, Q_{16} and Q_{17}, instead of just the $1 + h_{fe}$ of output transistor Q_{17}.

Transistor Q_{17}, the positive channel output transistor, has a common-collector configuration and, therefore, has no voltage gain.

Thermal stabilization of the output stage is accomplished by a proper choice of resistor values to offset the thermal variations in the input bias voltages, appearing at the bases of transistors Q_{11} and Q_{12}, as well as the inherent variations in the output stage.

The use of a negative feedback resistor in the output stage aids in thermal stabilization, sets the voltage gain, and enables the use of a wide range of power supply values. Feedback resistor R_{15} is placed between the output and the virtual ground in the level-shift circuitry (junction of R_{13} and R_{14}). The voltage gain with R_{15} in place is essentially R_{15}/R_{13}, regardless of which channel is conducting, provided the positive-negative channel gains without R_{15} are much greater.

The output stage will work properly over a wide range of power supply values because the collector voltage of Q_{12} is essentially clamped to the negative supply through the diode action of Q_{13}, Q_{13A}, Q_{14} and Q_{15}, and Q_{18}. Only a few millivolts are required at the collector of Q_{12} to cover the entire range of Q_{15} and Q_{18}, from cutoff to saturation. The feedback can affect this change of a few millivolts, forcing a balance between output transistors Q_{17} and Q_{18}.

Detailed ratings and characteristics for the CA3033 and CA3033A are given in the technical bulletins on these circuits. Ratings and typical operating characteristics at an ambient tem-

perature of 25°C are given in the TECHNICAL DATA section of this manual.

MULTIPURPOSE WIDE-BAND AMPLIFIER

The RCA-CA3020 monolithic integrated circuit is a multipurpose, multi-function power amplifier designed for use in portable and fixed communication equipment and servo control systems. This circuit is a stabilized direct-coupled amplifier, and performs pre-amplifier, phase inverter, driver, and power-output functions without transformers. The circuit is designed to operate from a single power supply between +3 to +9 volts; the ac power-output capability and the idling current are direct functions of the supply voltage used. At a supply voltage of +3 volts, the CA3020 delivers a typical power output of 65 milliwatts with an idling current of 7 milliamperes; at +9 volts, it delivers 550 milliwatts with a current of 22 milliamperes. The circuit includes a temperature-tracking voltage regulator which permits stable operation over a wide temperature range (−55°C to +125°C). Principal features of the CA3020 are as follows:

- Specially designed power transistors which deliver high power efficiently.
- Single-power-supply operation from +3 to +9 volts.
- Built-in temperature compensation to assure stable power gain and circuit operating points over the temperature range from −55° to +125°C.
- Low idling-current capability depending on supply voltage and circuit connections used.
- Easy application of squelch to the amplifier.
- Low-distortion operation obtainable.
- Optional buffer stage for increased input impedance.
- High power gain to permit coupling to most detectors without additional amplification.
- Wideband operation (typical 3-dB bandwidth of 6 MHz).
- Availability of restricted frequency capability.
- 12-lead TO-5 package to permit use with economical heat sinks at higher power levels.

Circuit Description

The schematic diagram of the CA3020 amplifier is shown in Fig. 237. The functional block diagram in Fig. 238 shows that the circuit performs five functions: voltage regulator, buffer or optional amplifier, differential amplifier and phase splitter, driver, and power-output amplifier.

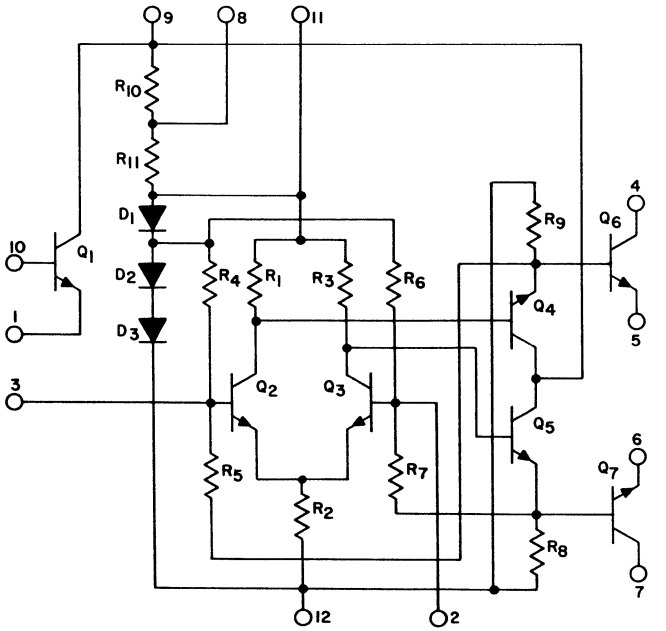


Fig. 237 — Schematic diagram of the CA3020 integrated-circuit multipurpose wide-band amplifier.

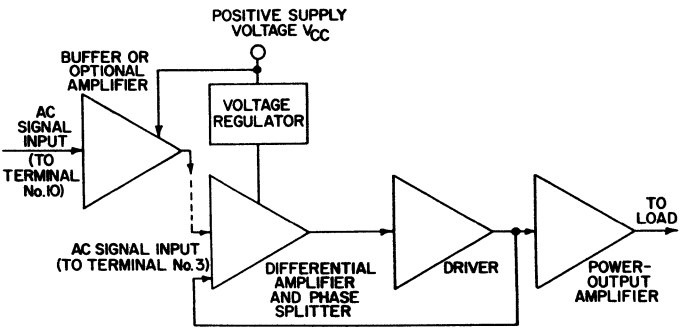


Fig. 238 — Functional block diagram of the CA3020.

The voltage regulator consists of diodes D_1, D_2, and D_3 and resistors R_{10} and R_{11}. The diodes are constructed from transistor emitter-base junctions to permit temperature tracking over the range from −55°C to +125°C. The regulator supplies two voltages to the differential amplifier, a base supply voltage equal to 2 V_{BE} (about 1.4 volts) and a collector supply voltage equal to 3 V_{BE} (about 2.1 volts).

The differential-amplifier-and-phase-splitter circuit consists of transistors Q_2 and Q_3, collector resistors R_1 and R_3, and biasing resistors R_4, R_5, R_6, and R_7. The ac signal voltage may be capacitor-coupled directly into terminal 3 or applied to terminal 10 (buffer amplifier Q_1) and then coupled into terminal 3. Whichever technique is used, the signal is amplified and the 180-degree phase shift necessary for push-pull operation is obtained between the collectors of transistors Q_2 and Q_3.

The ac signal is then applied to the emitter-follower transistors Q_4 and Q_5 which form the driver stage. Feedback resistors R_5 and R_7 provide dc and ac stability in the differential amplifier. If these resistors were not used, slight variations in V_{BE}, beta and/or resistor ratios could cause the dc voltage between the collectors of Q_2 and Q_3 to vary from zero. However, application of the emitter-follower voltages from Q_4 and Q_5 to the differential amplifier through R_5 and R_7 compensates for any imbalance.

The power transistors Q_6 and Q_7 accept the ac signal from the emitters of Q_4 and Q_5 and deliver power to the load in a class B push-pull mode of operation.

Operating Requirements and Characteristics

The following paragraphs describe circuit operating requirements and characteristics for the CA3020.

Supply Voltages and Derating — The CA3020 operates with any supply voltage between +3 and +9 volts. Fig. 239 shows

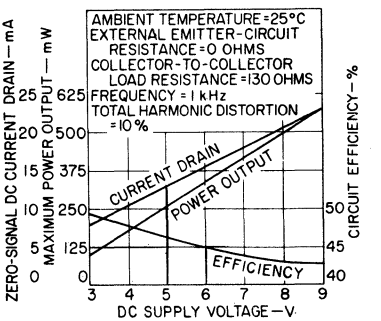


Fig. 239 — Performance characteristics of the CA3020 as a function of supply voltage.

performance characteristics at an ambient temperature of 25°C for various supply voltages, and Fig. 240 shows the temperature derating curve. At supply voltages from +6 volts to +9 volts, a heat sink should be used for maximum power-output capability.

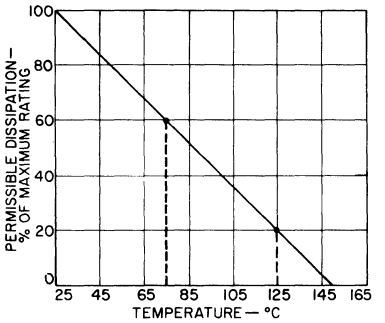


Fig. 240 — Temperature derating curve for the CA3020.

Input-Resistance Options — The input signal may be applied to the CA3020 in either of two ways, as shown in Fig. 241. Typical input resistance is 700 ohms for the configuration in Fig. 241(a), and 50,000 ohms for the configuration shown in Fig. 241(b).

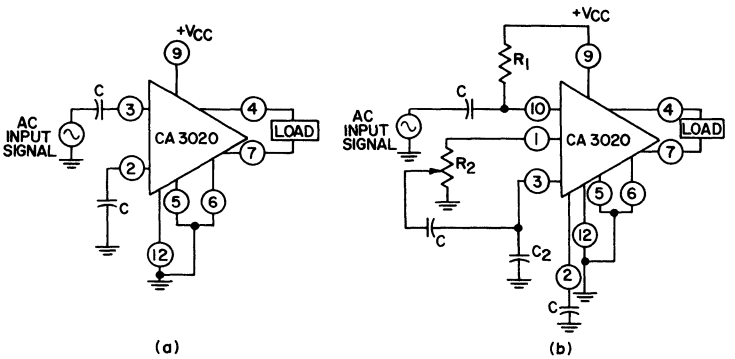


Fig. 241 — Input-impedance options for the CA3020.

DC Idling Current, Power Output, and Distortion — The CA3020 idling current, power output, and distortion are controlled primarily by the connections of terminals 8, 9, and 11. Lowest idling current is obtained when terminals 8 and 11 are open. When terminal 8 is connected to terminal 9 or 11, the idling current and power output increase and total harmonic distortion is reduced.

For applications in which low distortion is a premium requirement, a resistor may be connected between terminals 8 and 11, as shown in Fig. 242. The optimum value of this resistor for various supply voltages is shown in Table XXVII.

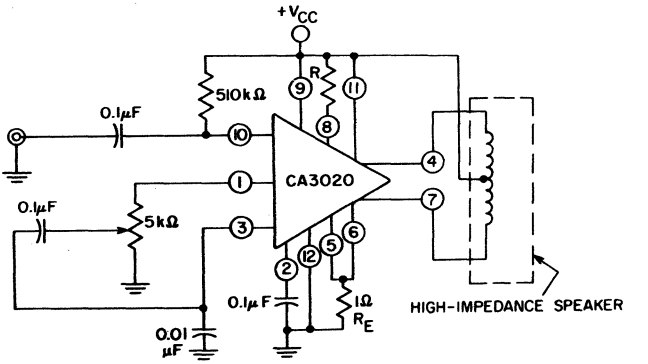


Fig. 242 — CA3020 connection optimized for low distortion.

Table XXVII — *Optimum Value of Resistor Connected Between Terminals 8 and 11*

Supply Voltage V_{CC} (V)	Idling Current I_{do} (mA)	Resistor between Terminals 8 and 11 (ohms)	Power Output P_{out} (mW)	Total Harmonic Distortion (%)
3	10	220	50	2.0
6	21	1000	200	2.0
9	24	∞	400	2.5

Although the CA3020 is thermally stable at all rated temperatures because of the built-in temperature-tracking voltage regulator, a small resistor (1 ohm) may be inserted from terminals 5 and 6 to ground for added stability. This introduction of negative feedback in the output stage also reduces distortion and idling current.

Power-Output Connections — The collectors of the power transistors Q_6 and Q_7 may be used for direct drive of center-tapped speakers or center-tapped output transformers when low-impedance loads are used. A curve of output power as a function of loading is shown in Fig. 243.

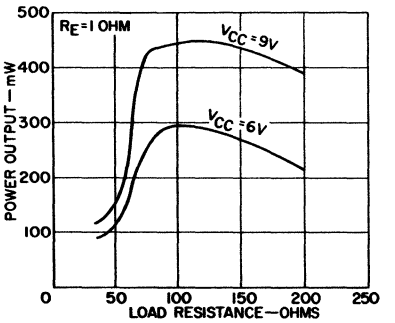


Fig. 243 — Output power as a function of load resistance.

Squelch — The CA3020 has an extremely flexible squelch capability. Two methods of squelch application are shown in Fig. 244. In method A, when the squelch voltage E_s is at zero, transistor Q_s is off. When E_s switches to a value of 1 volt or more (threshold is at a V_{BE} of about 0.7 volt), Q_s turns on, terminal 11 is clamped to 0.3 volt, and the differential amplifier is turned off. Method B operates in the same manner as method A except that the center-tap of R_{10} and R_{11} (terminal 8) is connected to the collector of Q_s. The resistor R_2 is not necessary for squelching, but can be used to set the desired operating mode (idling current).

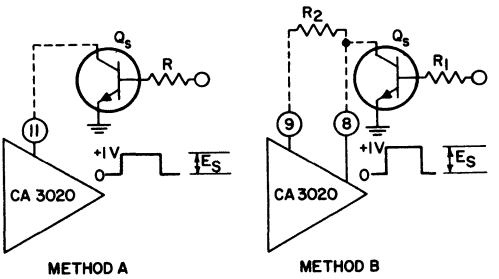


Fig. 244 — Methods of applying squelch to the CA3020.

Frequency Shaping

In communication systems it is often necessary to restrict the bandwidth of the audio amplifier to minimize the effects of noise (particularly low-frequency noise) and other interfering signals outside the passband. The CA3020 is a wideband amplifier that has a relatively flat frequency response to approximately 6 MHz. Various methods can be used to roll off the high- and low-frequency response by means of the coupling capacitors and bypass capacitors shown in the feedback loop in Fig. 245.

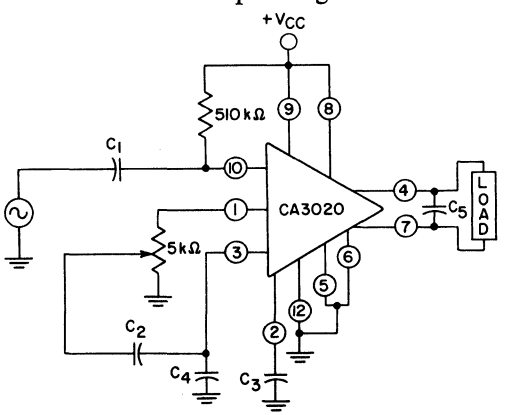


Fig. 245 — Methods of restricting the bandwidth of the CA3020.

Capacitors C_1, C_2, and C_3 may be used for rolling off the low-frequency response. The low-frequency cutoff is determined by the time constants C_1R_{10} and C_2R_3, where R_{10} is the input resistance at terminal 10 (about 50,000 ohms) and R_3 is the input resistance at terminal 3 (about 700 ohms).

Capacitors C_4 and C_5 are used for establishing the upper-frequency cutoff. The high-frequency roll-off is determined by the time constants C_4R_3 and C_5R_L, where R_L is the load resistance.

For a restricted bandwidth of 300 Hz to 3 kHz, the following capacitance values are recommended:

C_1	0.02 μF
C_2	1 μF
C_3	2 μF
C_4	0.1 μF
C_5	0.2 μF

Applications

The CA3020 may be used to drive a high-impedance speaker directly, without transformers, or it may be used with power transformers to deliver power to a low-impedance speaker or to one or more power transistors to develop power output up to 7 watts.

310-Milliwatt Transformerless Audio Amplifier — Fig. 246 shows a circuit configuration for a 310-milliwatt audio amplifier that uses no driver or output transformers. This circuit can be used with most AM and FM detectors because full power is developed

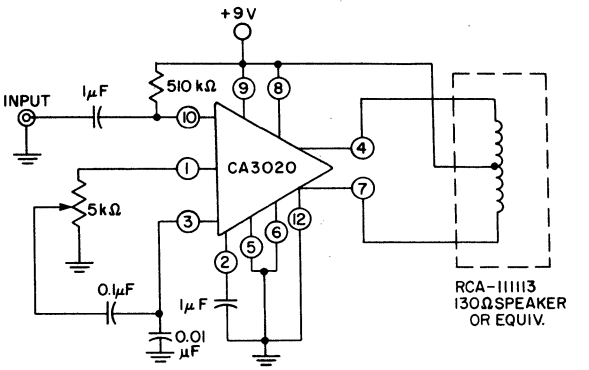


Fig. 246 — 310-milliwatt audio amplifier without transformers.

with a typical input voltage of 45 millivolts rms. Pertinent circuit characteristics are summarized below:

Input voltage for full power output	45 mV
Maximum power output	310 mW

Idling current	24 mA
Input resistance	50,000 ohms
Total harmonic distortion at P_{out} = 135 mW	1%
Signal-to-noise ratio (input voltage reference of 20 mV)	77 dB

545-Milliwatt Amplifier Driving a Low-Impedance Speaker — Fig. 247 shows a circuit configuration that has the required characteristics for driving a conventional low-impedance speaker. The circuit shown uses a transformer capable of driving a 3.2-ohm

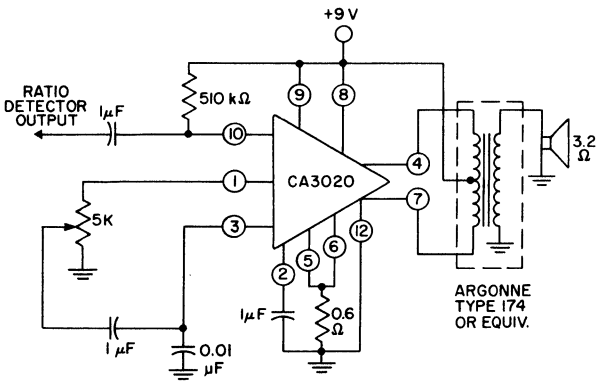


Fig. 247 — 545-milliwatt amplifier driving a low-impedance speaker.

speaker; other transformers may be used to drive 8-ohm and 16-ohm speakers. This circuit has the following characteristics:

Input voltage for full power output	45 mV
Maximum power output	545 mW
Idling current	22 mA
Input resistance	50,000 ohms
Total harmonic distortion at P_{out} = 135 mW	3.3%
Signal-to-noise ratio (input voltage reference of 20 mV)	77 dB

4-Watt Class A Audio Amplifier — Fig. 248 shows a class A audio amplifier in which the CA3020 is used with a driver transformer, a 2N2148 power transistor, and an output transformer. This circuit can deliver a power output of 4 watts to an 8-ohm speaker for an input voltage of 18 millivolts, or 0.45 watt for an input of 5.5 millivolts.

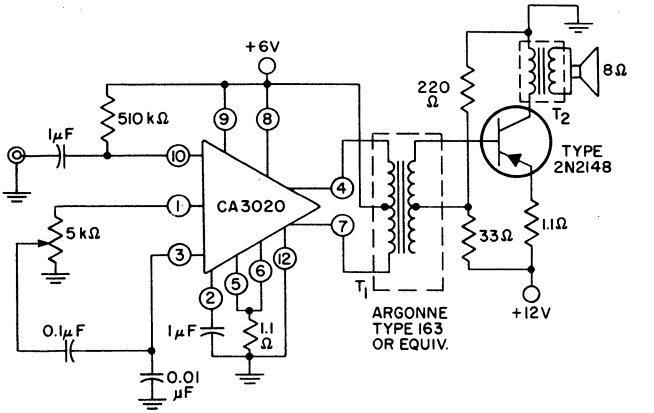


Fig. 248 — 4-watt audio amplifier.

7-Watt Single-Ended Class B Audio Amplifier — Fig. 249 shows a class B audio amplifier in which the CA3020 is used with a driver transformer and two 2N2869 power transistors in a single-ended output stage. With an input voltage of 14.2 millivolts, this circuit has an idling current of 350 milliamperes and can deliver an output of 7 watts to the 2.5-ohm speaker.

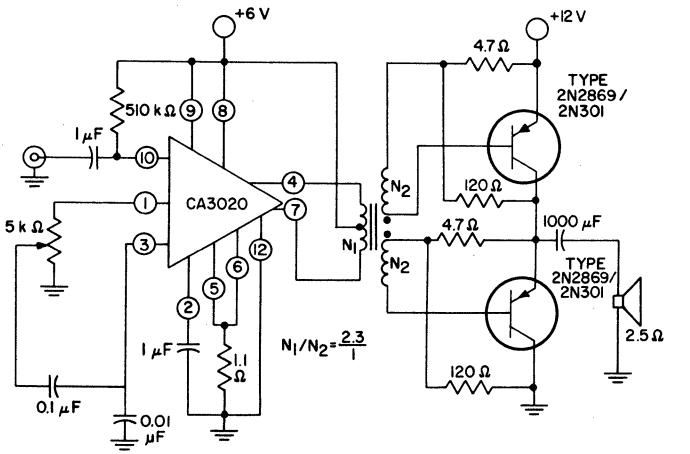


Fig. 249 — 7-watt class B single-ended audio amplifier.

AC Amplifiers — The CA3020 may be used in control systems as a highly efficient power amplifier. Fig. 250 shows a typical configuration in which the CA3020 is connected for wideband operation with a resistive load. At a frequency of 1 kHz, the voltage gain V.G. of this circuit is given by

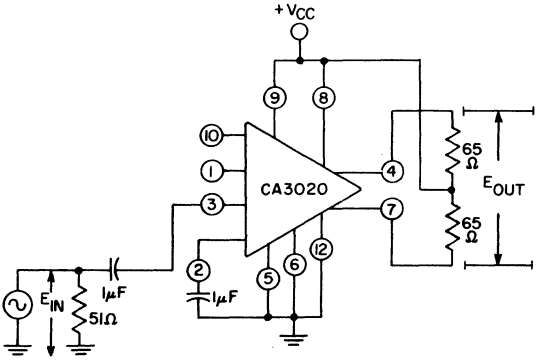
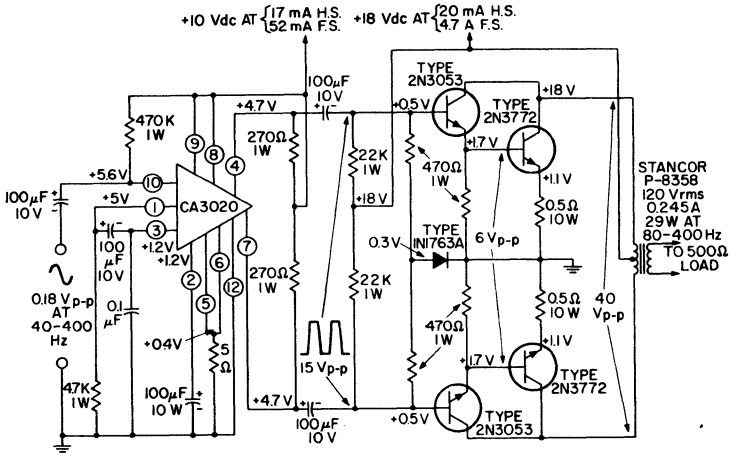


Fig. 250 — CA3020 as a wide-band amplifier.

$$\text{V.G.} = 20 \log_{10} (E_{out}/E_{in}) = 44 \text{ dB}.$$

Motor Controller and Servo Amplifier — The CA3020 may be used as a 40-to-400-Hz motor controller and servo amplifier, as shown in Fig. 251.



$$\text{Efficiency of power stage at 80-400 Hz} = \frac{29 \times 100}{85} = 34\%$$

$$\text{Efficiency of power stage at 40 Hz} = \frac{21 \times 100}{85} = 25\%$$

Fig. 251 — 40-to-400-Hz motor controller and servo amplifier using the CA3020.

Class A Wide-Band Amplifier — Fig. 252 shows the use of the CA3020 in a class A wide-band amplifier that operates over

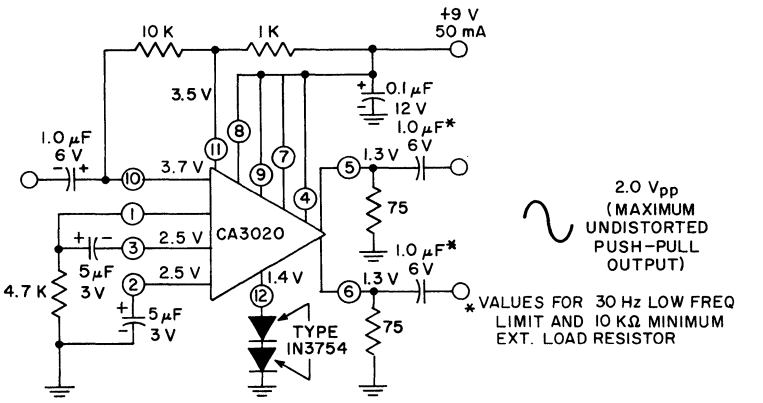


Fig. 252 — CA3020 as a wide-band class A amplifier.

the frequency range from 30 Hz to 8 MHz. For a peak-to-peak input of 0.12 volt at 1 MHz, the amplifier provides an undistorted peak-to-peak output of 2 volts. The input impedance of the amplifier at 1 MHz is 7800 ohms, and the output impedance at this frequency is 3 ohms.

FM IF AMPLIFIERS

The CA3011 and CA3012 wide-band amplifiers and the CA3013 and CA3014 amplifier-discriminators are designed for use in black-and-white or color television receivers or in FM broadcast or communications receivers. The CA3011 and CA3012 are basically if amplifier-limiters intended for use with external FM detectors. The CA3013 and CA3014, however, can provide if amplification, noise limiting, FM detection, and low-level audio amplification in the sound-if section of intercarrier television receivers or in FM receivers without the use of external components other than tuned coupling networks and bypass elements.

Circuit Descriptions

The circuit configurations of the CA3011 and CA3012 are identical; the circuits differ, however, in that the CA3012 is capable of operation at higher levels of dc voltage and current. Similarly, the CA3013 and CA3014 are identical, except that the CA3014 has higher dc voltage and current ratings.

Fig. 253 shows the schematic diagram of the CA3011 or CA3012 wide-band amplifier. The amplifier consists of three direct-coupled cascaded differential-amplifier stages and a built-in regulated power supply. Each of the first two stages consists of

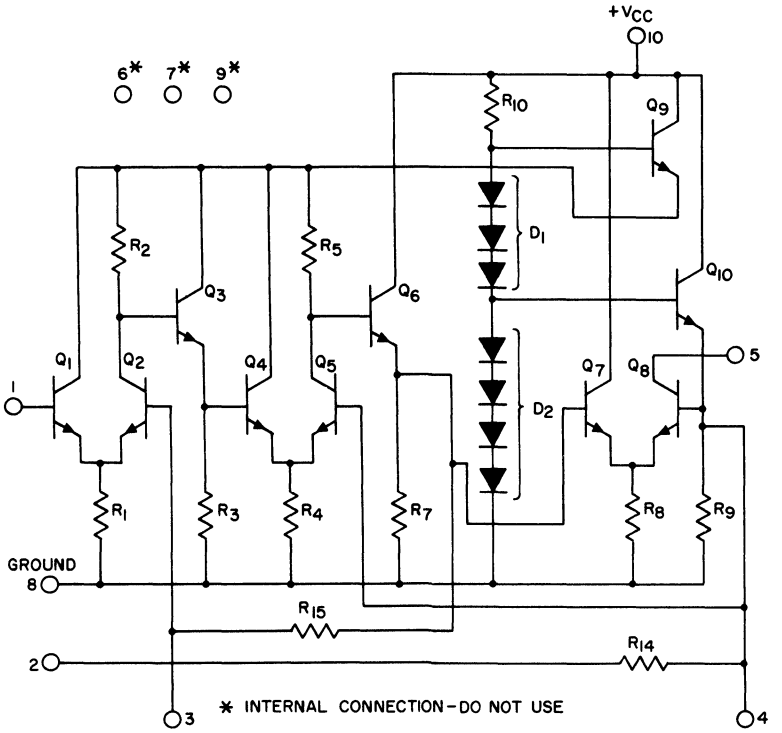


Fig. 253 — Schematic diagram of the CA3011 or CA3012 integrated-circuit wide-band amplifier.

an emitter-coupled amplifier and an emitter follower. The operating conditions are selected so that the dc voltage at the output of each stage is identical to that at the input to the stage. This condition is achieved by operation of the bases of the emitter-coupled differential pair of transistors at one-half the supply voltage and selection of the value of the common-emitter load resistor to be one-half that of the collector load resistor. As a result, the voltage drops across the emitter and collector load resistors are equal, and the collector of the emitter-coupled stage operates at a voltage equal to V_{BE} plus the common-base potential. The potential at the output of the emitter follower, therefore, is the same as the common-base potential.

Fig. 254 shows the schematic for the CA3013 or CA3014 amplifier-discriminator. Each amplifier-discriminator includes a three-stage, direct-coupled, amplifier-limiter cascade and regulated power supply identical to those in the CA3011 and CA3012 wide-band amplifiers, together with an FM detector and a Darlington

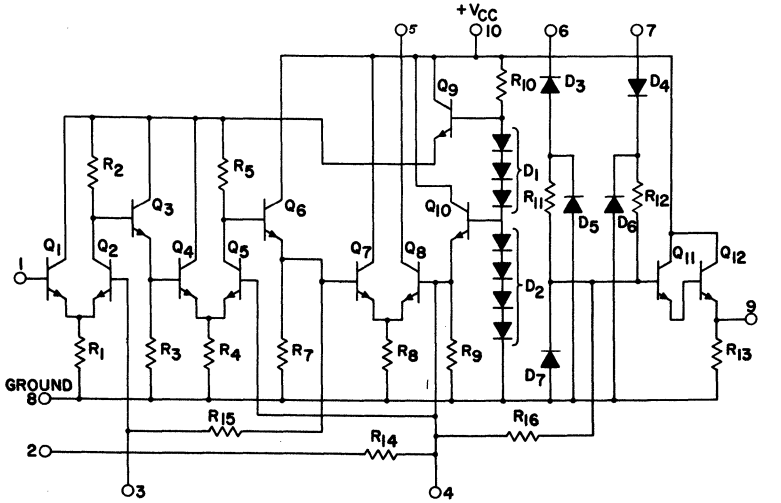


Fig. 254 — Schematic diagram of the CA3013 or CA3014 integrated-circuit amplifier-discriminator.

pair low-level audio output stage, on the same silicon chip. The operation of the amplifier-limiter stages and the regulated power supply is identical to that of the wide-band amplifiers.

The FM detector includes all the components required for FM demodulation except the tuned phase-shift transformer. In the design of the integrated detector, the large nonintegrable diode load capacitors conventionally used to obtain peak rectification in balanced phase-shift discriminators and in ratio detectors are eliminated, and average detection is employed with a substantially resistive load. Filtering of the signal frequency and its harmonics is provided by the distributed capacitance of the load resistors; additional filtering is provided by the capacitance of the small reverse-biased diode junctions D_5, D_6, and D_7. The parallel input resistance at the discriminator terminals 6 and 7 is typically 12,000 ohms; the parallel input capacitance at these terminals is typically 7 picofarads.

Operating Characteristics

The CA3011 and CA3013 are designed to operate at various levels of dc supply voltage up to 7.5 volts. The CA3012 and CA3014, which have higher supply-voltage and dissipation ratings, may be operated at dc supply voltages up to 10 volts. For each circuit, the external dc voltage is applied to terminals 10 and 5; dc voltages required at other terminals are derived from the in-

ternal power supply. When the circuits are operated at the same dc levels, the characteristics of their amplifier-limiter stages are identical. For operation at 7.5 volts with an ac resistive load impedance of 3000 ohms from terminal 5 to ground, the output voltage at terminal 5 with respect to ground is typically 3 volts peak-to-peak. Figs. 255 through 260 show the significant characteristics of the FM-if amplifier integrated circuits.

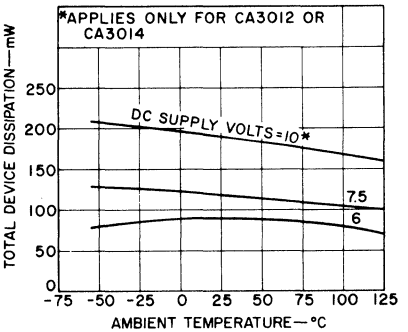


Fig. 255 — Total dissipation as a function of temperature.

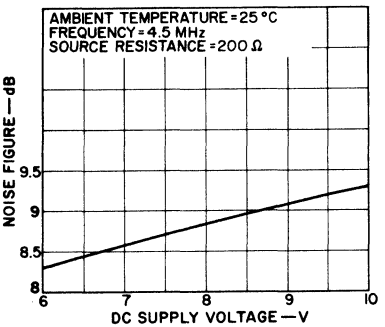


Fig. 256 — Noise figure as a function of dc supply voltage.

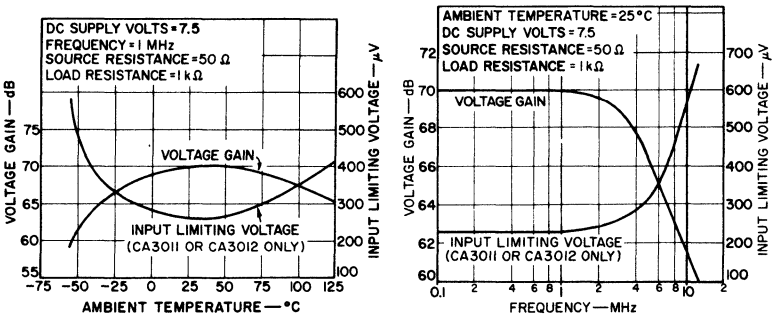


Fig. 257 — Voltage gain and input limiting voltage as a function of temperature and of frequency.

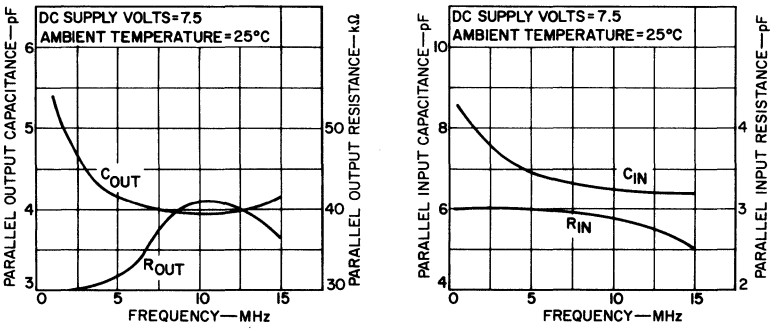


Fig. 258 — Input and output impedance as a function of frequency.

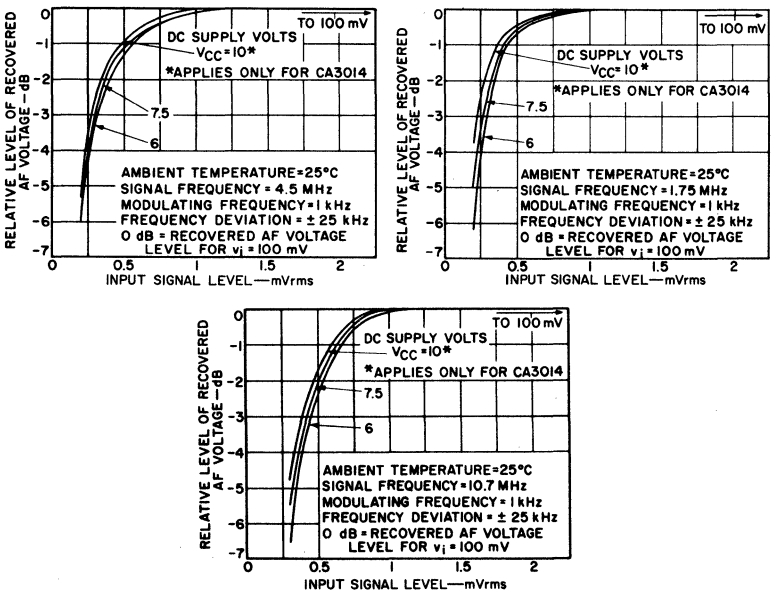


Fig. 259 — Input limiting voltage (knee) and recovered audio-frequency voltage for operation of amplifier-discriminator at 1.75, 4.5, and 10.7 MHz.

Applications

The performance of the integrated circuits in the FM sound channel of intercarrier television receivers and in the if amplifier-limiter-detector channel of FM radio receivers is at least equal to that of conventional circuits in every characteristic, and is superior in many of them. In particular, the AM rejection ratio (more than 50 dB) of the integrated circuits is so large that it cannot be measured with commercial FM-AM signal generators because of incidental phase modulation of the generators. The block diagram

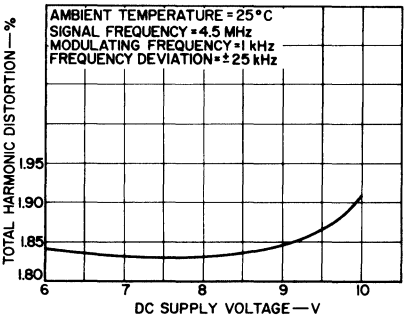


Fig. 260 — Total harmonic distortion as a function of dc supply voltage.

in Fig. 261 shows the use of the CA3013 or CA3014 amplifier-discriminator in the sound channel of an intercarrier television receiver. (Details of discriminator transformer shown in Fig. 261 are given in Fig. 262.) Fig. 263 shows the use of the CA3011 or CA3012 wide-band amplifier in the 10.7-MHz if-amplifier channel of an FM broadcast receiver.

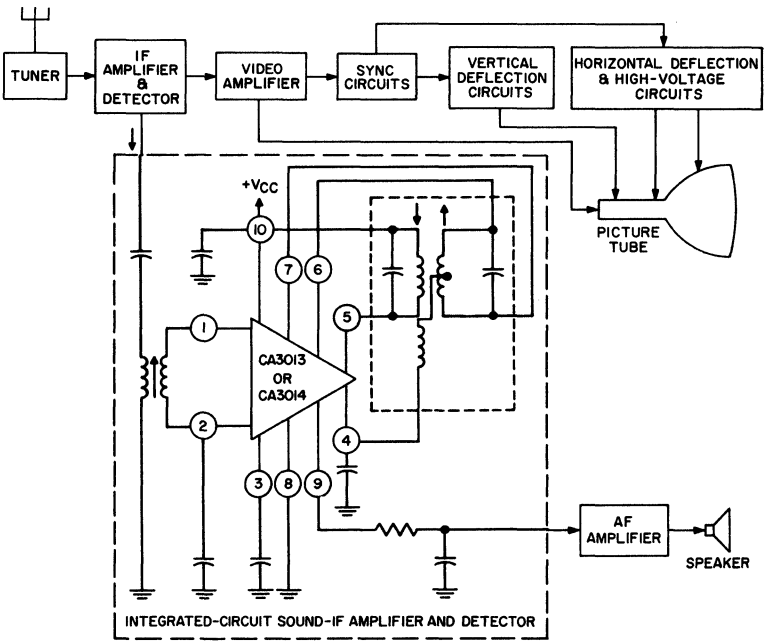
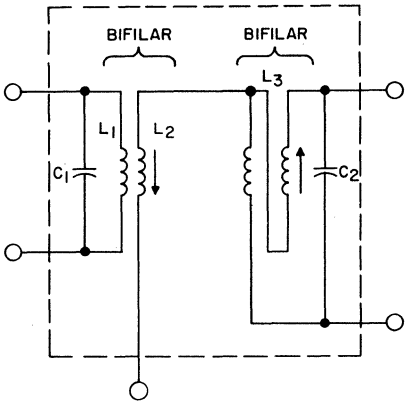


Fig. 261 — Block diagram of typical television receiver using CA3013 or CA3014 integrated-circuit sound if amplifier and detector section.



Discriminator-Transformer Construction Details

Coil-form outside diameter = 7/32 inch.
Slugs: Radio Industries, Inc., Type "E" material, or equiv.
Wire Type: GRIPEZE,* or equiv.

f MHz	Size AWG#	L_1▲	Turns L_2▲	L_3▼	C_1 pF	C_2 pF
1.75	36	44	20	44 total	820	820
4.5▪	40	18	7	22 total	560	330
10.7•	36	18	18	18 total	100	100

* Registered Trade Mark, Phelps-Dodge Copper Products
▲ Wound bifilar
▼ Two sections bifilar wound; bifilar turns = ½ total turns
▪ At this frequency, TRW Type No. 21685, or equiv., may be used for discriminator transformer
• At this frequency, TRW Type No. 21590-R1, or equiv., may be used for discriminator transformer.

Fig. 262 — Details of discriminator transformer shown in Fig. 261.

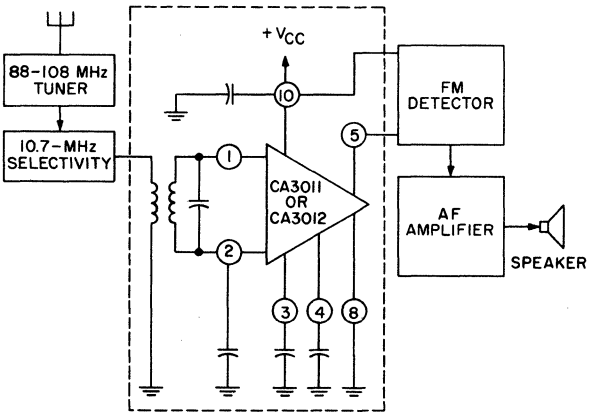


Fig. 263 — Block diagram of typical FM receiver using CA3011 or CA3012 integrated-circuit wide-band amplifier.

CA3012 FM IF Strip — Fig. 264 shows the use of two CA3012 units in a 10.7-MHz if-amplifier strip. At an operating point 3 dB down from the knee of the transfer curve, the CA3012 requires an input between 400 and 600 microvolts, depending on the ratio-detector design. A double-tuned filter that has a voltage insertion loss of 8 dB is located between the two CA3012 units to

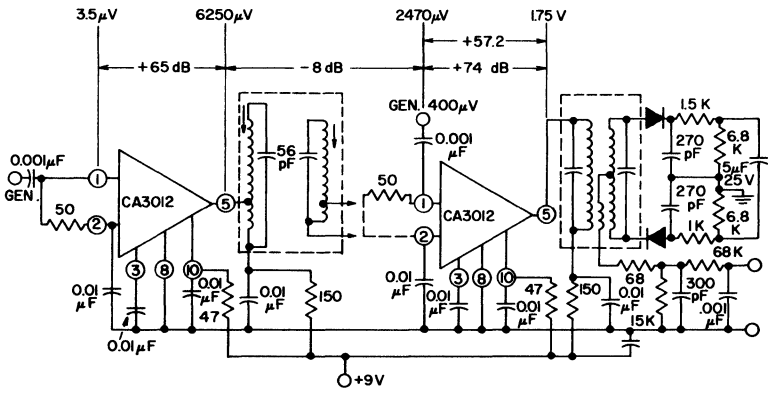


Fig. 264 — 10.7-MHz if-amplifier strip using CA3012 integrated circuit.

provide a filter input of approximately 1000 microvolts (at terminal 5 of the first CA3012). For an if-strip sensitivity of 4 microvolts, a gain of 48 dB is required. However, if the CA3012 used has a load impedance of 1200 ohms, the available gain is 65 dB, or approximately 17 dB more than required. The extra gain is not wasted, but drives the second CA3012 harder, causing it to limit so that its gain is reduced by approximately 17 dB.

Fig. 265 shows the selectivity of the double-tuned interstage filter. The 3-dB bandwidth is 200 kHz at an input of 10 microvolts and 240 kHz at inputs from 500 microvolts to 0.5 volt. The coefficient of critical coupling is approximately 0.5 at 10 microvolts and increases to 1.0 but still maintains good phase response. The double-tuned filter should be coupled capacitance-aiding to

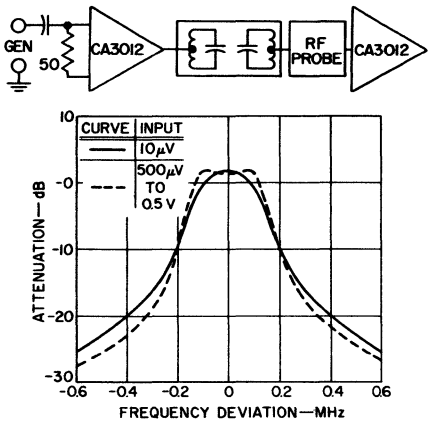


Fig. 265 — Selectivity curve for double-tuned interstage filter used in the if-amplifier strip of Fig. 264.

avoid a nearly in-phase over-all relationship. Otherwise, bypassing of terminal 10 and the ratio-detector primary becomes critical, and over-all stability is impaired.

The connection of the FM front end to the integrated-circuit if strip must provide good selectivity and good phase response. A double-tuned filter is not suitable from the standpoint of selectivity. An actual IHFM receiver selectivity between 35 and 40 dB is practical and does not impose too much burden on alignment. Because IHFM selectivity includes other factors than passband, a combined filter design that provides second-channel attenuation between 52 and 60 dB becomes imperative.

Investigation of various types of inductance-capacitance filters indicates the use of a triple-tuned type to form the major lumped selectivity of the FM receiver. Fig. 266 shows the response curve and two configurations for such a filter. Economy and ease of alignment are the major features in this approach.

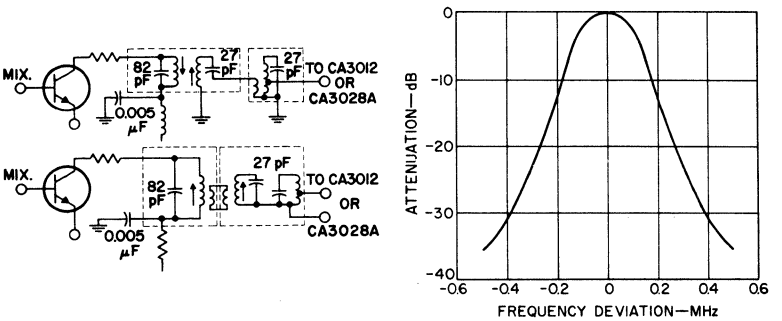


Fig. 266 — Configurations and response curve for triple-tuned interstage filter.

The triple-tuned filter, which is located between the mixer and the first integrated circuit, may have a voltage insertion loss of 33 dB, depending on the desired gain distribution. The power insertion loss of the filter, which is between 12 and 17 dB, is the loss that contributes to if noise. If the primary impedance is reduced to provide a lower voltage insertion loss, the front-end gain is decreased by a corresponding amount. Stability criteria must be the deciding factor in impedance and gain distribution.

Most FM front ends come equipped with a double-tuned 10.7-MHz if transformer in which a secondary high-impedance winding is brought out capacitively unterminated and non-polarized with respect to ground. This configuration does not lend itself readily to optimum skirt selectivity (form factor) when connected

with an additional single-tuned transformer to form a triple-tuned filter. Most effective use of the existing front-end filter is accomplished by the addition of another double-tuned filter, such as those shown in Fig. 267. Either bottom inductance or capacitance coupling can be used. Voltage insertion losses from 18 dB to 26 dB can be expected. Fig. 268 shows the response curve obtained with a quadruple-tuned interstage filter. The per-cent coupling between filters and the coupling mode must be determined on the basis of over-all stability and performance.

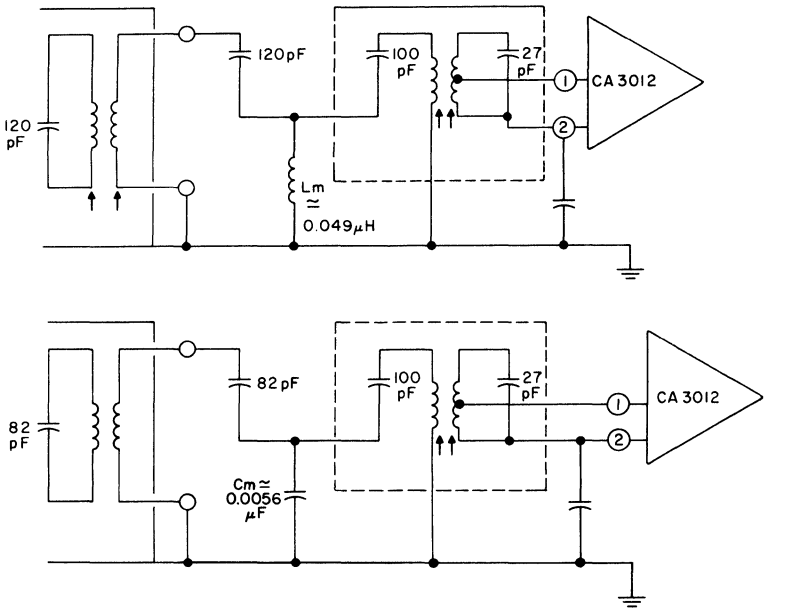


Fig. 267 — Configurations of two quadruple-tuned interstage filters.

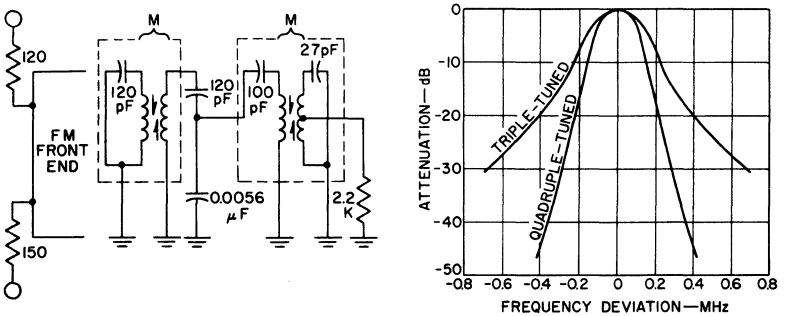


Fig. 268 — Response curve obtained with quadruple-tuned filter.

It may be appropriate to consider briefly the noise associated with high-insertion-loss filters. Over-all receiver noise F is calculated as follows:

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} \tag{209}$$

where F_1, F_2, and F_3 are the noise figures of the first (rf), second (mixer), and third (if) stages, respectively; and G_1 and G_2 are the power gains of the first and second stages. If a value of 27 dB is assumed for the if noise figure F_3 (filter plus integrated circuit), 10 dB for the mixer noise figure, and 30 dB for mixer power gain, the effect of if noise on mixer noise is determined as follows:

$$F_2' = F_2 + \frac{F_3 - 1}{G_2} = 10 + \frac{27 - 1}{1000} = 10.026 \text{ dB} \tag{210}$$

If the rf stage is assumed to have a power gain of 15 dB and a noise figure of 5 dB, total received noise is then determined as follows:

$$F = F_1 + \frac{F_2' - 1}{G_1} = 5 + \frac{10.87 - 1}{31.7} = 5.285 \text{ dB} \tag{211}$$

These calculations show that the power gain of the rf-amplifier stage overrides both if noise and mixer noise. A minimum power gain of 10 dB is advisable.

The use of a tuning capacitance of 82 picofarads in the collector circuit of the mixer stage provides a loaded primary impedance of approximately 10,000 ohms and eliminates the need for a tap. The 27-picofarad tuning capacitances that comprise the other poles of this filter could be reduced to obtain more favorable loaded-to-unloaded-Q ratios without use of additional resistor loading. The choice of 27 picofarads is based primarily on circuit stability considerations.

Fig. 269 shows one type of complete integrated-circuit if strip, and Fig. 270 shows the accompanying voltage gains and impedances. Values are given for two levels of mixer output impedance. All other impedance levels shown have exhibited good stability. Over-all performance of the circuit is illustrated in Fig. 271.

Capture ratio, which was measured at various levels, varies from 5 dB at 2 microvolts to 1.2 dB above 500 microvolts. With careful adjustment, values as low as 0.8 dB can be obtained. The selectivity curve for the integrated-circuit if strip is shown in Fig. 272. Over-all selectivity for a given ratio detector and the if strip is shown in Fig. 273. Some distributed-selectivity receivers have

very little second-channel selectivity at an antenna input of 2000 microvolts. The points marked in Fig. 273 show such selectivity for several antenna input levels.

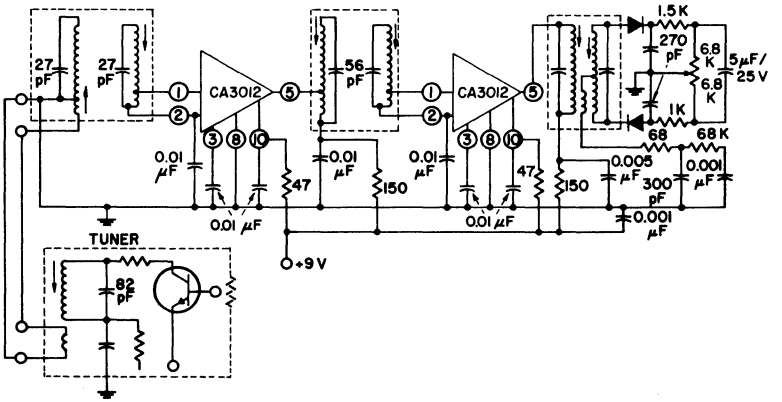


Fig. 269 — Complete 10.7 MHz if-amplifier strip using two CA3012 integrated circuits.

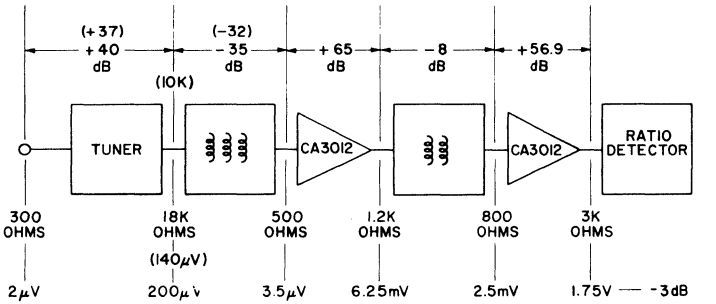


Fig. 270 — Voltage gain and impedance values for if-amplifier strip of Fig. 269.

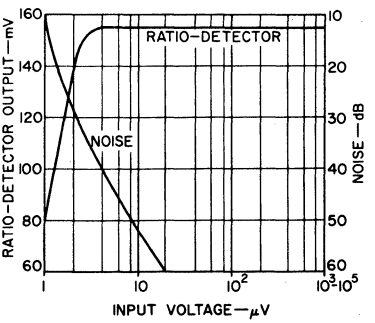


Fig. 271 — Performance curves for if-amplifier strip of Fig. 269.

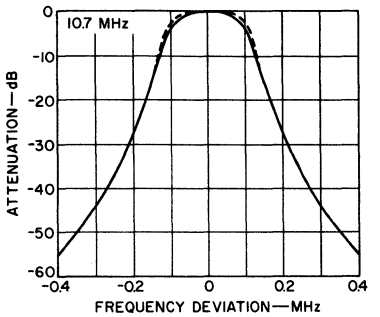


Fig. 272 — Selectivity curve for if-amplifier strip of Fig. 269.

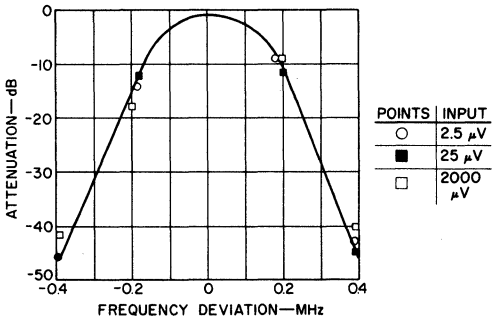


Fig. 273 — Measured over-all selectivity curve for if-amplifier strip of Fig. 269 and a given ratio detector.

Fig. 274 shows an if strip that combines high gain per package and the single-stage-per-package approach. CA3012 and CA3028 integrated circuits are used in a differential-mode connection. An if sensitivity of 15 microvolts can be obtained with this if strip.

If discrete circuits are directly replaced by single differential integrated-circuit amplifiers, a minimum of if transformer and printed-circuit-board redesign is required. Values of voltage gain and impedance are indicated on the block diagram in Fig. 275. All three double-tuned transformers are made symmetrical with respect to primary and secondary windings and taps.

Because the single- or double-tuned circuit used between the mixer and the if strip has inherently less insertion loss than a triple-tuned input filter, the input required is 20 instead of 3.5 microvolts. All three double-tuned if transformers have an insertion loss of 6 dB and a 3-dB bandwidth of 280 to 300 kHz. The ratio-detector primary impedance dictates the stage gain of 36 dB for the last integrated circuit. Each of the remaining three stages

has a gain of 21.5 dB, for the total required gain of 100 dB. The impedance required for the desired stage gain was calculated to be 660 ohms for both the primary and secondary windings of the if transformers.

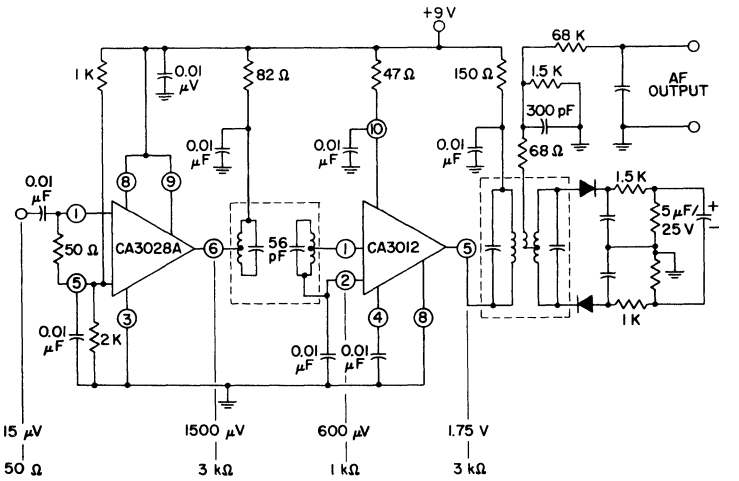


Fig. 274 — IF-amplifier strip using CA3028A and CA3012 integrated circuits.

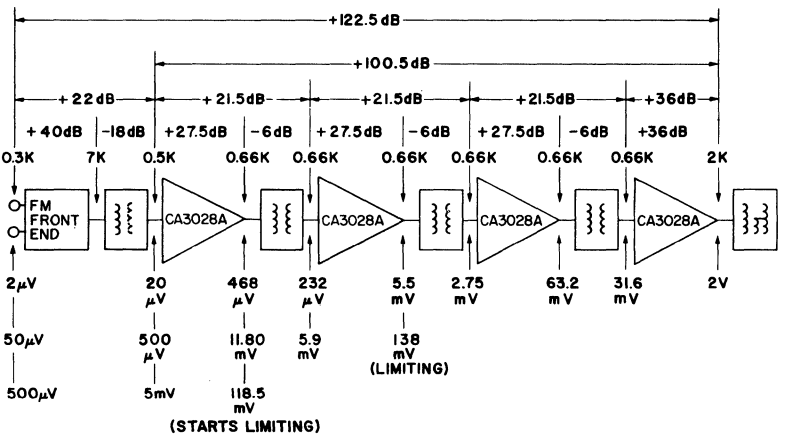


Fig. 275 — Voltage gain and impedance values for if-amplifier strip of Fig. 274.

With inputs from 20 to 200 microvolts, second-channel selectivity as high as 52 to 59 dB can be attained for three double-tuned and four double-tuned filters, respectively, for a 3-dB bandwidth of 196 kHz. For higher inputs, the same deterioration of

selectivity occurs as that experienced with discrete circuits, as shown in Fig. 276.

Several receivers incorporating the if strips shown have been field-tested in areas of 200-kHz station separation, where a weak station was sandwiched between two strong stations. The weak station was received without interference, as compared to the performance of other high-quality FM receivers fabricated with discrete-component if circuits, where lack of selectivity marred reception.

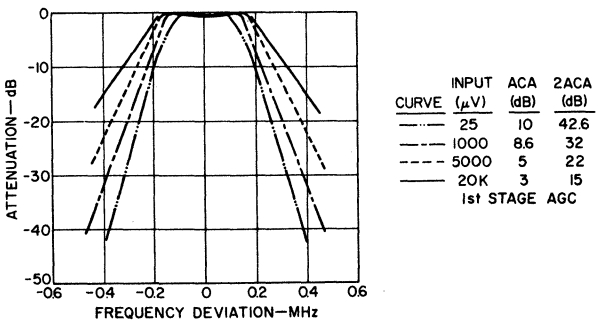


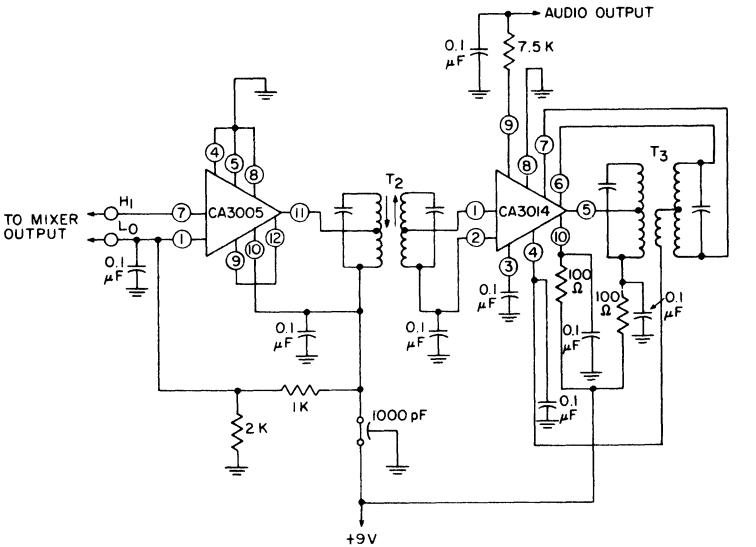
Fig. 276 — Selectivity curves for discrete-component if-amplifier strip using six double-tuned filters.

FM IF Amplifier, Limiter, and Detector — Fig. 277 shows a 10.7-MHz FM if strip and detector that uses a CA3005 and a CA3014 to provide 95 dB of gain. The input limiting knee for the if strip is 30 microvolts. The recovered audio obtained from terminal 9 of the CA3014 is 220 millivolts rms. The if selectivity curve and the detector "S" curve are also shown in Fig. 277. The AM rejection referenced to a 30-percent modulated (FM and AM) signal with the AM signal at 30 millivolts is 50 dB.

The 10.7-MHz FM signal from the mixer in the FM receiver is applied to terminal 7 of the CA3005. The gain from this point to the input of the CA3014 is 25 dB. The interstage transformer T_2 is designed so that the collector output of the CA3005 at terminal 1 does not saturate. As a result, bandpass spreading is kept to a minimum over large swings in input voltage. The 10.7-MHz FM signal receives additional gain of 70 dB and limiting from terminal 1 to terminal 5 in the CA3014. The FM output at terminal 5 is applied to the primary winding of the phase-shift (discriminator) transformer T_3. The secondary winding, which is connected to terminals 6 and 7, is in quadrature with the primary voltage at the center frequency, 10.7 MHz. As the FM signal

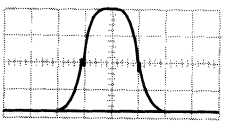
varies, the phase shift of the secondary voltage follows the modulation. The detected output at the base of Q_{11} in the CA3014 (terminals 6 and 7) is thus amplified and buffered. The recovered audio is taken from the low-impedance terminal 9.

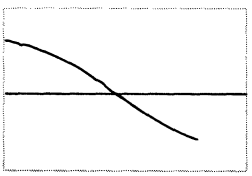
If more selectivity in the if strip is desired, an additional double-tuned transformer can be added to the circuit.



T_2 = TRW No. 21969 or equiv.
T_3 = TRW No. 21590 or equiv.

10.7-MHz IF SELECTIVITY CURVE
(Markers are 100 kHz apart with center at 10.7 MHz)





DETECTOR "S" CURVE

Fig. 277 — 10.7-MHz if amplifier, limiter, and discriminator using CA3005, CA3014, and interstage transformer, together with the selectivity curve and the detector "S" curve.

WIDE-BAND AMPLIFIER/PHASE DETECTORS

The CA3034 and CA3034V1 integrated-circuit wide-band amplifier/phase detectors are multiple-function circuits designed primarily for use in automatic-frequency-control (afc) applications at frequencies from dc to 100 MHz. These circuits are identical except that the CA3034 is supplied in a 10-terminal TO-5 style package with straight leads and the CA3034V1 is supplied in a TO-5 style package with formed leads. The circuits are designed to operate from a single dc power supply, at various voltage levels up to 15 volts, over a range of ambient temperatures from −55°C to +125°C.

Fig. 278 shows the schematic diagram for the CA3034 and CA3034V1 integrated circuits. These circuits perform the functions of amplifier limiter, dual phase detector, difference amplifier, and

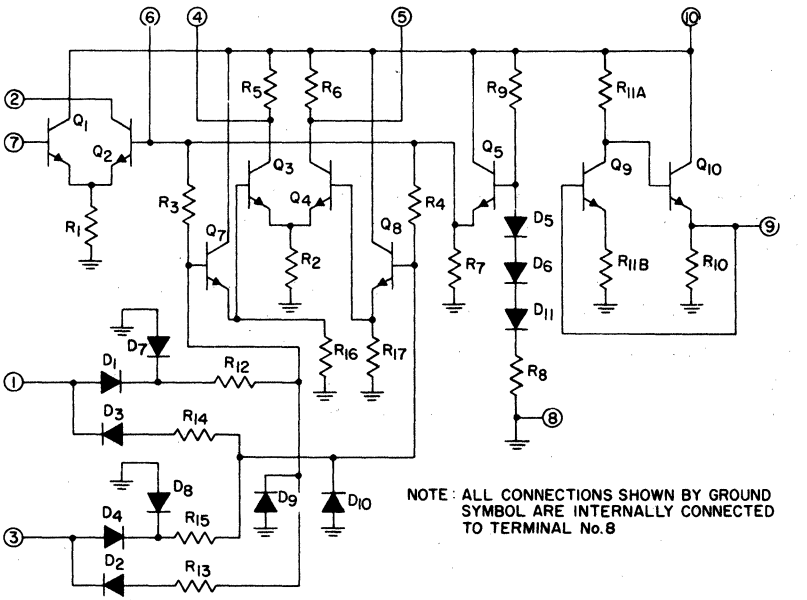


Fig. 278 — Schematic diagram of the CA3034 or CA3034V1 integrated-circuit wide-band amplifier/phase detector.

reference voltage regulator. Fig. 279 shows a block diagram that illustrates the use of the CA3034 or CA3034V1 to perform the afc function in a color television receiver. The integrated circuit samples the video if signal, detects any frequency deviation of the picture carrier from the center frequency that may result because of mistuning or drift of the tuner local oscillator, and converts

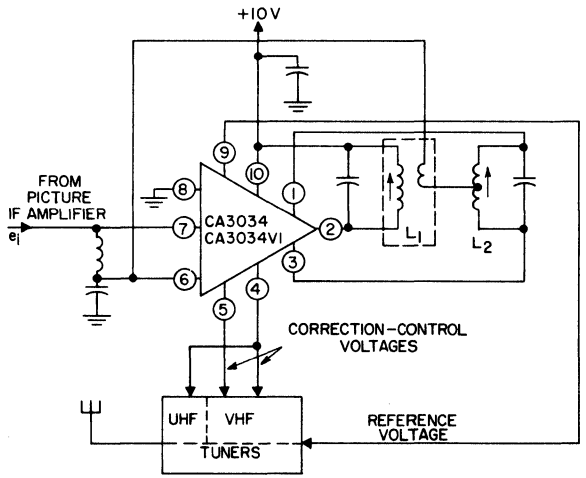


Fig. 279 — Block diagram of a typical afc application of the CA3034 or CA3034V1 in a color television receiver.

these deviations into dc correction voltages. These correction voltages, together with a reference voltage, are supplied to voltage-variable diodes in the VHF and UHF tuners to compensate for the local-oscillator drift.

The input voltage e_1 is the 45.75-MHz picture carrier, which is usually obtained from the output of the third picture if stage. This signal is amplified, limited, and applied to the primary of a phase-shift transformer. The secondary voltage of the transformer is normally in quadrature with the primary voltage. At the center frequency (47.75 MHz), the potential at the junctions of R_{12} and R_{13} and of R_{14} and R_{15} is approximately to 2.25 volts (bias voltage). The differential amplifier (Q_3, Q_4, Q_7, and Q_8) is balanced for this condition; the voltage difference between terminals 4 and 5 is then equal to 0 ± 1.5 volts.

On either side of the center frequency, the voltage swings positively and negatively about the bias voltage at the detector resistor junctions. As the junction of R_{12} and R_{13} become positive, the junction of R_{14} and R_{15} becomes negative. These junction voltages control the biasing of the differential amplifier, which in turn, determines the correction voltages at terminals 4 and 5. The color-receiver designer can use either the differential correction voltages from terminals 4 and 5, or single-ended correction voltages in conjunction with the regulator correction voltage.

WIDE-BAND AMPLIFIER ARRAYS

The CA3035 and CA3035V1 integrated-circuit arrays are ultra-high-gain, low-noise, wide-band devices intended primarily for use as remote-control amplifiers in receiver applications. The circuits are supplied in 10-terminal TO-5 style packages. With the exception that the CA3035 package has straight leads and the CA3035V1 has formed leads, the circuits are identical. The circuits operate from a single dc power supply at various voltage levels up to 15 volts over an ambient temperature range from −55°C to +125°C.

Each circuit consists of three general-purpose high-gain amplifier stages that may be operated independently or in cascade. Each stage can provide a voltage gain in excess of 40 dB and when operated in cascade provide an over-all voltage gain of 129 dB at 40 kHz.

Fig. 280 shows the schematic diagram for the wide-band integrated arrays. The first stage features a low-noise common-emitter amplifier combined with emitter followers at both the input

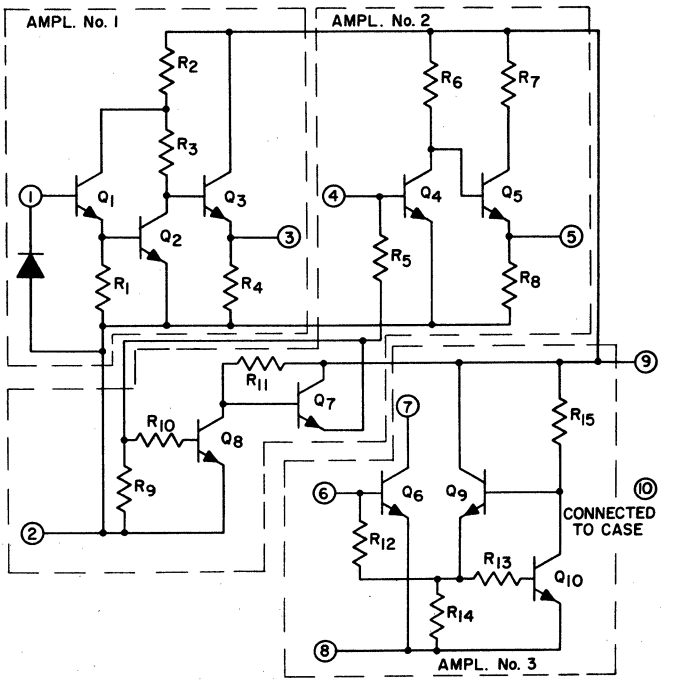


Fig. 280 — Schematic diagram of the CA3035 or CA3035V1 integrated-circuit wide-band amplifier array.

and the output. The second stage consists of a common-emitter input, an emitter-follower output, and a dc voltage regulator. The third stage consists of a common-emitter amplifier with uncommitted collector and a voltage regulator. The uncommitted collector permits the use of tuned or resistive loads and an increased collector supply voltage for larger output swings. Fig. 281 shows the gain-frequency response for each amplifier stage.

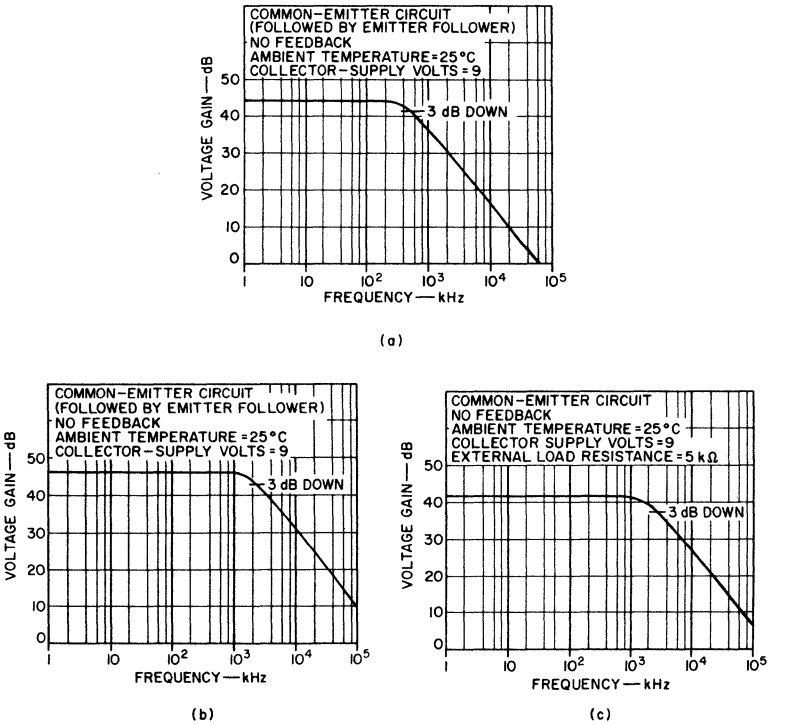


Fig. 281 — Typical gain-frequency response of the three amplifier stages in the CA3035 or CA3035V1 array: (a) first stage; (b) second stage; (c) third stage.

Fig. 282 shows the CA3035 used in a remote-control system. An input signal of about 40 kHz is delivered to terminal 1 from the microphone pickup. The remote-control system requires a typical input voltage of 100 μV to pull in the relay driver.

The ease of accessibility to the 3 separate stages of the circuit makes it possible to vary the gain and bandwidth of each stage by adjustment of external feedback resistors. As a result, the amplifier

array can be used in many applications that require different gain-bandwidth specifications.

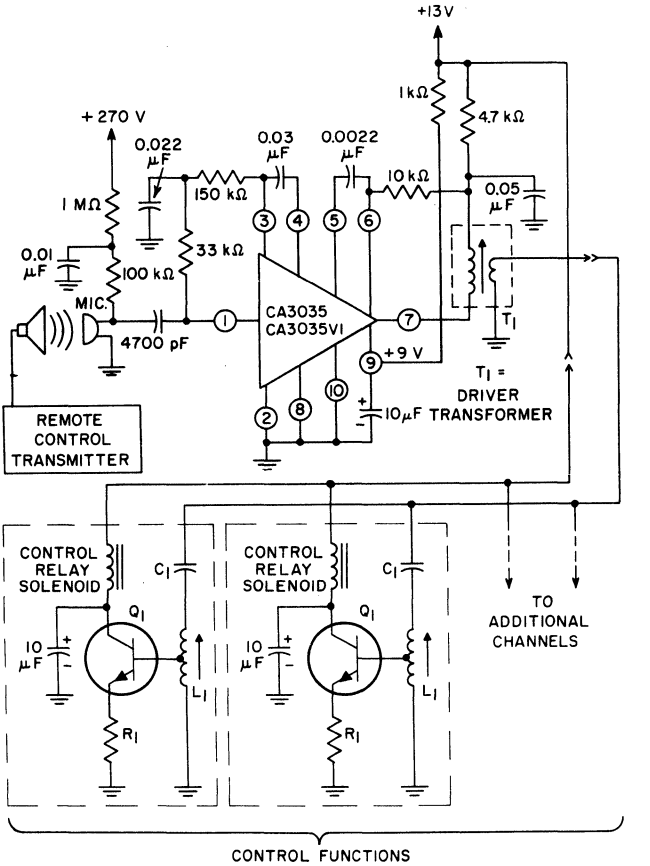


Fig. 282 — Block diagram of a typical remote control system using the CA3035 or CA3035V1.

DIODE ARRAY

The RCA-CA3019 integrated-circuit diode array provides four diodes internally connected in a diode-quad arrangement plus two individual diodes. Its applications include gating, mixing, modulating, and detecting circuits.

The CA3019 is designed for operation at ambient temperatures from −55°C to 125°C and is supplied in a 10-terminal TO-5 low silhouette package.

Because all the diodes are fabricated simultaneously on a single silicon chip, they have nearly identical characteristics, and their parameters track each other with temperature variations as a result of their close proximity and the good thermal conductivity of silicon. Consequently, the CA3019 is particularly useful in circuit configurations which require either a balanced diode bridge or identical diodes.

Circuit Configuration and Operating Characteristics

Fig. 283 shows the circuit diagram and terminal connections for the CA3019. Diodes D_1 through D_4 are internally interconnected to form a diode quad, while diodes D_5 and D_6 are available as independent diodes. Each diode is formed from a transistor by connection of the collector and the base to form the diode anode and use of the emitter for the diode cathode (this technique is one of five methods by which the transistor structure can be utilized as a diode). This diode configuration, in which the collector-base junction is shorted, is the most useful connection for a high-speed diode because it has the lowest storage time. The only charge stored is that in the base. This configuration also exhibits the lowest forward voltage drop, and is the only one which has no p-n-p transistor action to the substrate. The diode has the emitter-to-base reverse breakdown voltage characteristic (typically 6 volts).

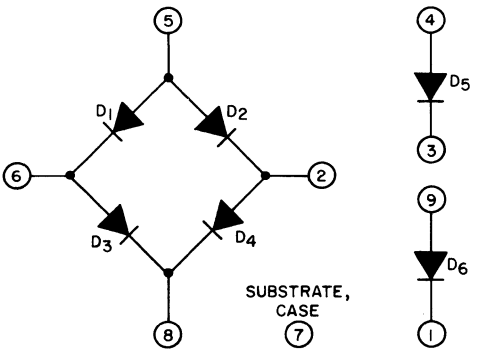


Fig. 283 — Schematic diagram of the CA3019 integrated-circuit diode array.

The monolithic process produces a substrate diode between the collector of a transistor and its supporting substrate, as shown in Fig. 284. Connected at each diode anode, therefore, is the cathode of a substrate diode for which the anode is the substrate

(Terminal 7). In many applications, the substrate can be left floating because a forward bias on any substrate diode creates a self reverse-bias on the other substrate diodes. However, the uncertainty of this bias and the capacitive feedthrough paths provided by the substrate must be considered.

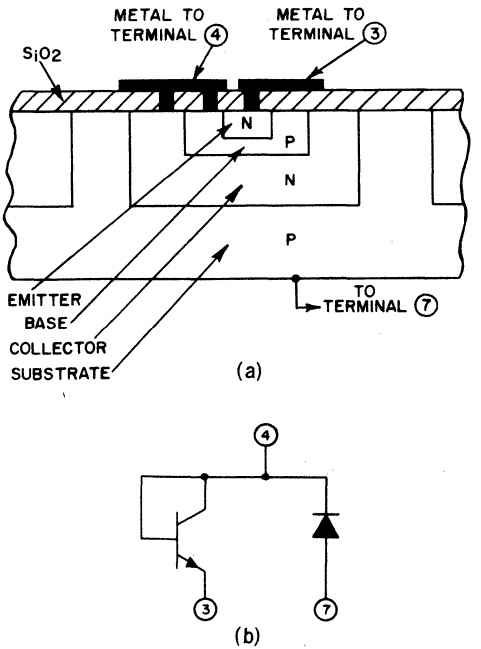


Fig. 284 — Diagram and equivalent circuit of the monolithic array.

The capacitive feedthrough paths can be eliminated if the substrate is either ac grounded or returned to a dc voltage (or ground when possible). This dc voltage must be more negative than any anticipated ac or dc operating voltage present on any diode anode to assure that every substrate diode will always be reverse-biased. When a choice exists, the substrate diodes should be reverse-biased.

The operating characteristics of the CA3019 integrated diode array are determined primarily by the individual diode characteristics, which are given in the technical bulletin.

Applications

There are many possible applications for the CA3019. Besides the obvious uses as separate diodes and possible quad combinations, some of which are covered in the following discussion, it should be

noted that shorting of terminals 2 and 6 in the quad effectively provides two diodes in series. This diode connection can be used as the elements of special balanced mixers, as ring modulators, and as compensating networks that provide two diode drops. Fig. 285 shows an example of a typical synthesizer mixer circuit. Shorting of terminals 5 and 8 provides two independent sets of back-to-back diodes useful for limiting and clipping, as shown in Fig. 286.

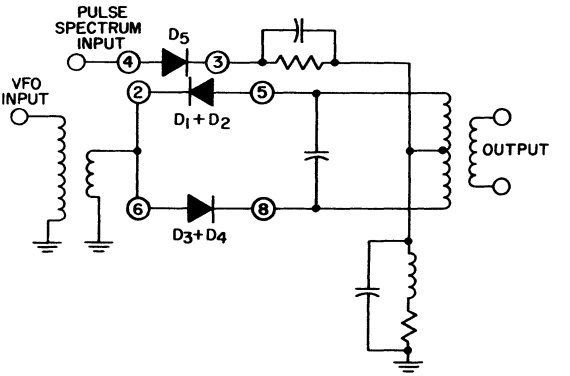


Fig. 285 — Typical synthesizer mixer circuit using the CA3019.

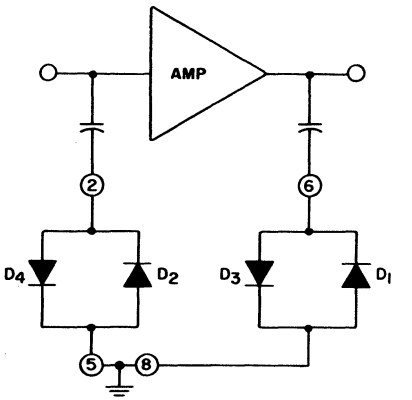
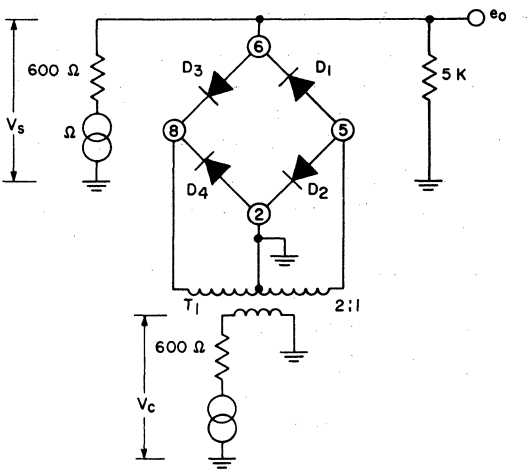


Fig. 286 — Limiters using the CA3019.

Balanced Modulator — Fig. 287 shows the use of the CA3019 as a balanced modulator which minimizes the carrier frequency from the output by means of a symmetrical bridge network. A carrier of one polarity causes all the diodes to conduct, and thus effectively short-circuits the signal source. A carrier of the opposite polarity cuts off all the diodes and allows signal current to flow to



T_1—TECHNITROL No. 85II66 OR EQUIV.

Fig. 287 — Balanced modulator using the CA3019.

the load. If the four diodes are identical, the bridge is perfectly balanced and no carrier current flows in the output load. The circuit operates properly with the substrate (terminal 7) either floating or returned to a negative voltage. Table XXVIII lists the characteristics of the balanced modulator.

High-Speed Gates — In high-speed gates, the gating signal often appears at the output and causes the output signal to ride a "pedestal." A diode-quad bridge circuit can be used to balance out the undesired gating signal at the output and reduce the pedestal to the extent that the bridge is balanced.

A diode-quad gate functions as a variable impedance between a source and a load, and can be connected either in series or in shunt with the load. The circuit configuration used depends on the input and output impedances of the circuits to be gated. A series gate is used if the source and load impedances are low compared to the diode back resistance, and a shunt gate is used if the source and load impedances are high compared to the diode forward resistance.

Fig. 288 shows the use of the CA3019 as a series gate in which the diode bridge, in series with the load resistance, balances out the gating signal to provide a pedestal-free output. With a proper gating voltage (1 to 3 volts rms, 1 to 500 kHz), diodes D_5 and D_6 conduct during one half of each gating cycle and do not conduct during the other half of the cycle. When diodes D_5 and D_6

Table XXVIII — *Characteristics of Balanced Modulator of Fig. 287*

Carrier Voltage VRMS at 30 KHz	0.75	0.75	0.75	0.50	1.0
Signal Voltage mVRMS at 2 KHz	77	245	770	245	245

Output Frequency KHz	Output Voltage mV rms	db Below Vs	Output Voltage mV rms	db Below Vs	Output Voltage mV rms	db Below Vs	Output Voltage mV rms	db Below Vs	Output Voltage mV rms	db Below Vs
28 and 32*	34	6.5	115	7	440	5	51	14	170	3
30	0.7	41	0.82	49	2.6	50	0.1	68	3.6	37
26 and 34	0.02	72	0.05	72+	0.48	64	0.04	72+	0.07	71
24 and 36	0.03	69	0.49	54	60	22	0.58	52.5	0.6	53
22 and 38	0.001	72+	0.01	72+	1.4	55	.015	72+	0.02	72+

* Double-Sideband, Suppressed-Carrier Output.
All other outputs are spurious signals.

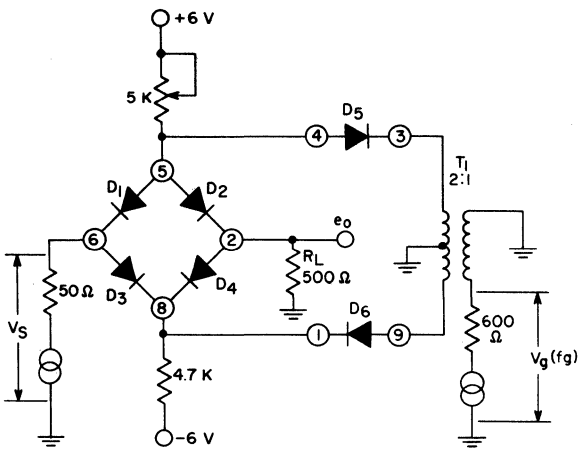


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Fig. 288 — Series gate using the CA3019.

are conducting, the diode bridge (D_1 through D_4) is not conducting and the high diode back resistance prevents the input signal V_s from appearing across the load resistance R_L; when diodes D_5 and D_6 are not conducting, the diode bridge conducts and the low diode forward resistance allows the input signal to appear across the load resistance. Resistor R_1 may be adjusted to minimize the gating voltage present at the output. The substrate (terminal 7) is connected to the —6 volt supply. The on-to-off ratio as a function of frequency for the series gate is shown in Fig. 289.

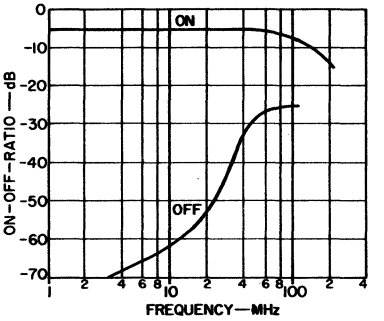
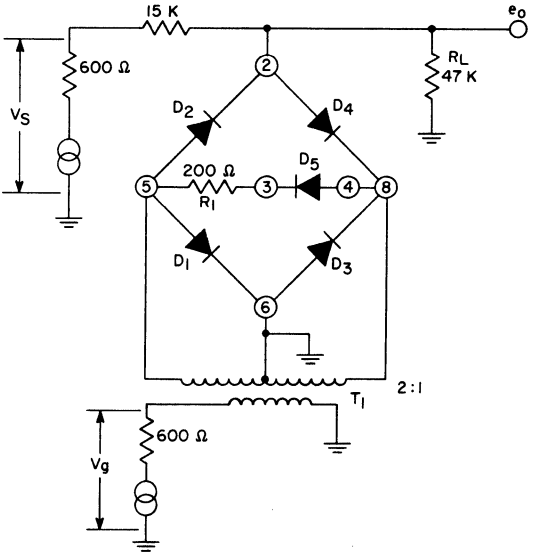


Fig. 289 — On-to-off ratio of the series gate of Fig. 288 as a function of frequency.

Fig. 290 shows the use of the CA3019 as a shunt gate in which the diode bridge, in shunt with the load resistance, balances out the gating signal to provide a pedestal-free output. When the gating voltage V_g is of sufficient amplitude, the diode bridge (D_1 through D_4) conducts during one half of each gating cycle and does not conduct during the other half of the cycle. When the diode bridge is conducting, its low diode forward resistance shunts the load resistance R_L and prevents the input signal V_s from appearing at the output; when the diode bridge is not conducting, its high diode back resistance allows the input signal to appear at the output. Diode D_5 and resistor R_1 keep the transformer load nearly constant during both halves of the gating cycle. The substrate (terminal 7) can either be left floating or returned to a negative voltage, but it cannot be returned to ground. The characteristics of the shunt gate are as follows:

Gating frequency (f_g) — 1 to 100 kHz
Gating voltage (V_g) — 0.8 to 1.2 Vrms
Signal frequency (f_s) — dc to 500 kHz (2 dB down)
Signal voltage (V_g) — 0 to 1 Vrms

The amount of gating voltage V_g present at the output as a function of the amplitude and frequency of V_g is shown in Table XXIX.



T_1—TECHNITROL No. 85I166 OR EQUIV.

Fig. 290 — Shunt gate using the CA3019.

Table XXIX — *Gating Characteristics of Shunt Gate Shown in Fig. 290*

Frequency of V_g kHz	Amplitude of V_g volts	Amount of V_g Present at the Output mV
1	0.8	0.2
1	1.0	0.5
1	1.2	1.3
10	0.8	2.0
10	1.0	4.7
10	1.2	8.7
50	0.8	11.0
50	1.0	24.0
50	1.2	40.0

A series-shunt gate which utilizes all six diodes of the CA3019 is shown in Fig. 291. This configuration combines the good on-to-off impedance ratio of the shunt gate with the low-output pedestal of the series gate.

On the gating half-cycle during which the voltage at A is positive with respect to the voltage at B, there is no output because the shunt diodes are forward-biased and the series diodes are reverse-biased. Any signal passing through the input diodes (D_4 and D_2) encounters a low shunt impedance to ground (D_5 and D_6) and a

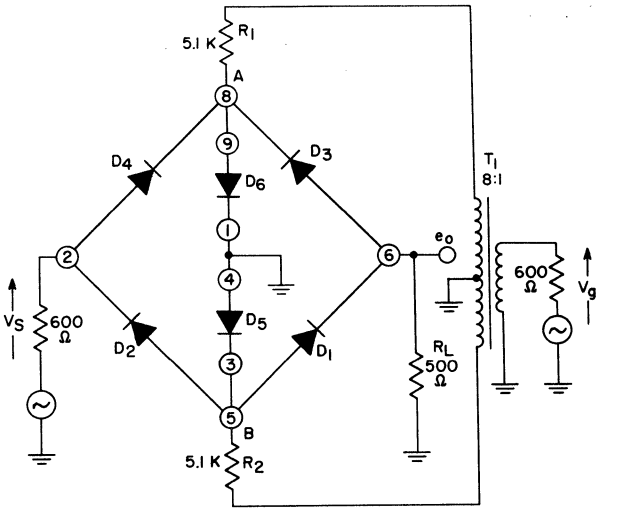


Fig. 291 — Series-shunt gate using the CA3019.

high impedance in series with the signal path to the load (D_3 and D_1). This arrangement assures a good on-to-off impedance ratio. When the voltages at A and B reverse, the conduction states of the shunt and series diodes reverse, and the signal passes through the gate to the load resistor R_L. Any pedestal at the output is a function of the resistor, transformer, and diode balance.

The gate continues to operate successfully with resistors R_1 and R_2 shorted if the transformer center tap is removed from ground. In either case, no dc supply is required to bias the gate diodes.

Balanced Mixer — Fig. 292 illustrates the use of the CA3019 as a conventional balanced mixer. The load resistor across the output tuned circuit is selected to provide maximum power output. The conversion gain of the mixer for a 45-MHz input signal and a 55-MHz oscillator signal is shown in Fig. 293. The input impedance at point A is approximately 600-ohms for a 0.6-volt-rms oscillator drive.

The CA3019 mixer shown in Fig. 294 is essentially a balanced mixer with two additional diodes (D_3 and D_4) added to form a half-wave carrier switch. The additional diodes permit both legs of the circuit (D_1 — D_2 and D_3 — D_4) to function throughout the ac cycle. As compared with a conventional balanced mixer, shown in Fig. 292, this circuit effectively doubles the desired output voltage and reduces the output voltage at the oscillator frequency by half.

However, the capacitances associated with the integrated diodes prevent this circuit configuration from realizing the improvement in conversion gain at frequencies above 20 MHz.

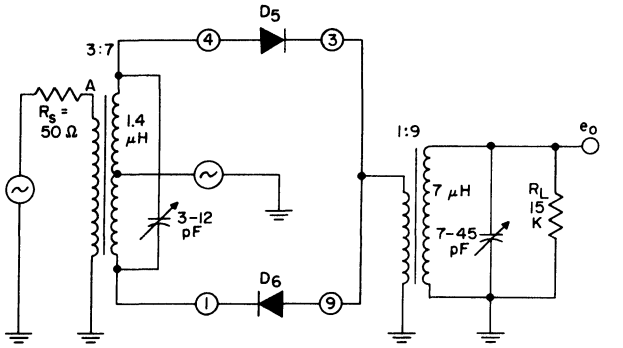


Fig. 292 — Balanced mixer using the CA3019.

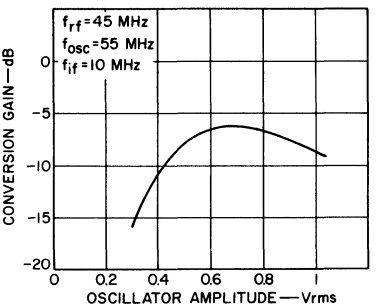


Fig. 293 — Conversion gain as a function of oscillator voltage for the balanced mixer of Fig. 292.

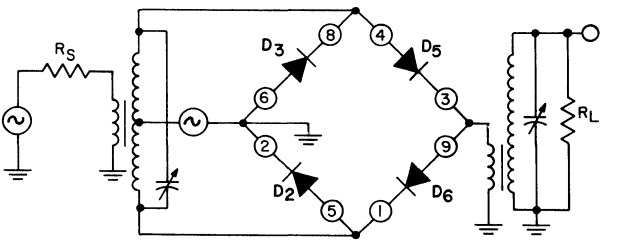


Fig. 294 — Balanced mixer with half-wave carrier switch using the CA3019.

Ring Modulator — The use of the CA3019 as a ring modulator is shown in Fig. 295. If a perfectly balanced arrangement were used, carrier current of equal magnitude and opposite direc-

tion would flow in each half of the center-tapped transformer T_2. Thus, the effect of the carrier current in transformer T_2 would be cancelled, and the carrier frequency would not appear in the output. However, the ring modulator of Fig. 295 is not exactly balanced because diodes $(D_1 + D_2)$ and $(D_3 + D_4)$ are actually two diodes in parallel, while diodes (D_5) and (D_6) are individual diodes. Nevertheless, this circuit attenuates the carrier in the output as well as an arrangement that uses both individual diodes in two CA3019 circuits.

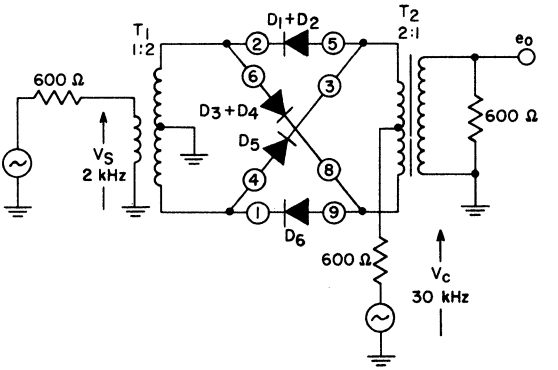


Fig. 295 — Ring modulator using the CA3019.

As the carrier passes through half of its cycle, diodes $(D_1 + D_2)$ and (D_6) conduct, and diodes $(D_3 + D_4)$ and (D_5) do not conduct. When the carrier passes through the other half of its cycle, the previously nonconducting diodes conduct, and vice versa. As a result, the output amplitude is alternately switched from plus to minus at the carrier frequency. The signal-frequency component of the output waveform is thus symmetrical about the zero axis and is not present in the output. Therefore, the ring modulator suppresses both the carrier frequency and the signal frequency so that the output theoretically contains only the upper and lower sidebands. For single-sideband transmission, one of these sidebands can be eliminated by selective filtering. The performance of the CA3019 as a ring modulator is shown in Table XXX.

TRANSISTOR ARRAY

The CA3018 integrated circuit consists of four silicon epitaxial transistors on a single chip mounted in a 12-lead TO-5 style package. The four active devices, two isolated transistors plus two transistors with an emitter-base common connection, are especially

Table XXX — *Performance Characteristics of Ring Modulator*

Output Freq. kHz		For a given $V_S + V_g$, e_o in millivolts			
	V_s mvs	300	350	450	500
	V_c mvs	600	500	350	300
28 or 32	Upper or Lower Sidebands	86	97	83	91
2	Sig. Freq.	0.042	0.02	0.015	0.020
30	Carrier Freq.	1.3 (—37dB)*	0.88 (—41dB)*	0.67 (—42dB)*	0.62 (—43dB)*
26 or 34	Higher Order Sidebands	0.018	0.016	0.036	0.043
24 or 36		0.021	0.054	0.047	5.0

* dB below the desired upper and lower sidebands

suitable for applications in which closely matched device characteristics are required, or in which a number of active devices must be interconnected with nonintegrable components such as tuned circuits, large-value resistors, variable resistors, and microfarad bypass capacitors. Such areas of application include if, rf (through 100 MHz), video, agc, audio, and dc amplifiers. Because the CA3018 has the feature of device balance, it is useful in special applications of the differential amplifier, and can be used to advantage in circuits which require temperature compensation of base-to-emitter voltage.

Circuit Configuration and Operating Characteristics

The circuit configuration for the CA3018 is shown in Fig. 296. In a 12-lead TO-5 package, because it is necessary to provide a terminal for connection to the substrate, two transistor terminals must be connected to a common lead. The particular configuration chosen is useful in emitter-follower and Darlington circuit connections. In addition, the four transistors can be used almost independently if terminal 2 is grounded or ac grounded so that Q3 can

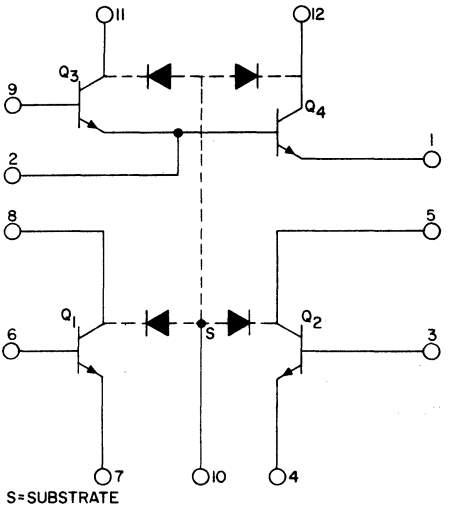


Fig. 296 — Schematic diagram for the CA3018 integrated-circuit transistor array.

be used as a common-emitter amplifier and Q4 as a common-base amplifier. In pulse video amplifiers and line-driver circuits, Q4 can be used as a forward-biased diode in series with the emitter of Q3. Q3 may be used as a diode connected to the base of Q4; in a reverse-biased connection, Q3 can serve as a protective diode in rf circuits connected to operational antennas. The presence of Q3 does not inhibit the use of Q4 in a large number of circuits.

In transistors Q1, Q2, and Q4, the emitter lead is interposed between the base and collector leads to minimize package and lead capacitances. In Q3, the substrate lead serves as the shield between base and collector. This lead arrangement reduces feedback capacitance in common-emitter amplifiers, and thus extends video bandwidth and increases tuned-circuit amplifier gain stability.

Operating characteristics for the CA3018 are given in the technical bulletin.

Circuit Applications

The applications for the CA3018 are many and varied. The typical applications discussed in the following paragraphs have been selected to demonstrate the advantages of four matched devices available on a single chip. These few examples should stimulate the generation of a great many more applications.

Video Amplifiers — A common approach to video-amplifier design is to use two transistors in a configuration designed to reduce the feedback capacitance (appearing as a Miller capacitance) inherent in a single triode device. These configurations which utilize two devices are (1) the cascode cricuit, (2) the single-ended differential-amplifier, and (3) the common-collector, common-emitter circuit. In all three circuits, the output-to-input feedback capacitance is minimized by isolation inherent in the configuration. The availability of four identical transistors in a common package provides a convenient vehicle for these circuit configurations for video-amplifier design. Two of the many possible circuit variations are discussed below.

A broadband video-amplifier design using the CA3018 is shown in Fig. 297. This amplifier may be considered as two dc-coupled stages, each consisting of a common-emitter, common-collector configuration. The common-collector transistor provides a low-impedance source to the input of the common-emitter transistor and a high-impedance, low-capacitance load at the common-emitter output. Iterative operation of the video amplifier can be achieved by capacitive coupling of stages.

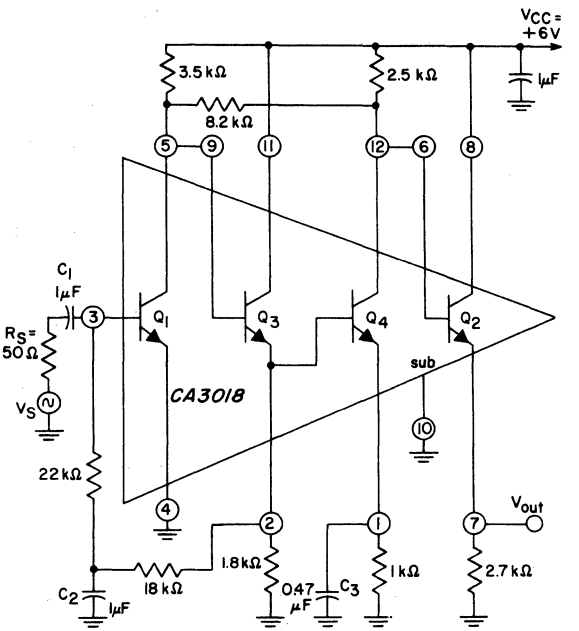


Fig. 297 — Schematic diagram for a CA3018 broadband video amplifier.

Two feedback loops provide dc stability of the broadband video amplifier and exchange gain for bandwidth. The feedback loop from the emitter of Q_3 to the base of Q_1 provides dc and low-frequency feedback; the loop from the collector of Q_4 to the collector of Q_1 provides both dc feedback and ac feedback at all frequencies.

The frequency response of the broadband video amplifier is shown in Fig. 298. The upper 3-dB break occurs at a frequency of 32 MHz. The low-frequency 3-dB characteristics are determined primarily by the values of capacitors C_1, C_2, and C_3. The low-frequency 3-dB break occurs at 800 Hz. The mid-frequency gain of 49 dB is constant to within 1 dB over the temperature range from −55° to +125°C. The upper 3-dB break is constant at 32 MHz from −55°C to +25°C, and drops to 21 MHz at +125°C.

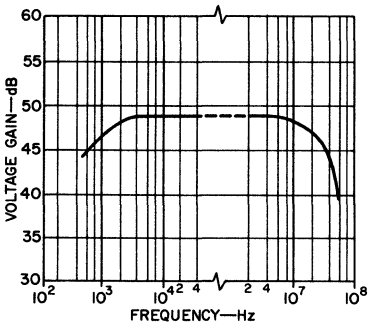


Fig. 298 — Voltage gain as a function of frequency for the broadband video amplifier of Fig. 297.

The total power dissipation over the entire temperature range is 22.8 milliwatts. The dc output voltage varies from 2.33 volts at −55°C to 3 volts at +125°C. The tangential sensitivity occurs at 20 microvolts peak-to-peak. The dynamic range is from 20 microvolts peak-to-peak to 4 millivolts rms at the input.

The circuit of Fig. 297 demonstrates a typical approach that can be altered, especially with regard to gain and bandwidth, to meet specific performance requirements.

The cascode configuration offers the advantages of common-emitter gain with reduced feedback capacitance and thus greater bandwidth. Fig. 299 shows a typical circuit diagram of a cascode video amplifier using the CA3018. Transistors Q_2 and Q_1 comprise the common-emitter and common-base portions of the cascode, respectively. The common-base unit is followed by cascaded emitter followers (Q_3 and Q_4) which provide a low output impedance to maintain bandwidth for iterative operation.

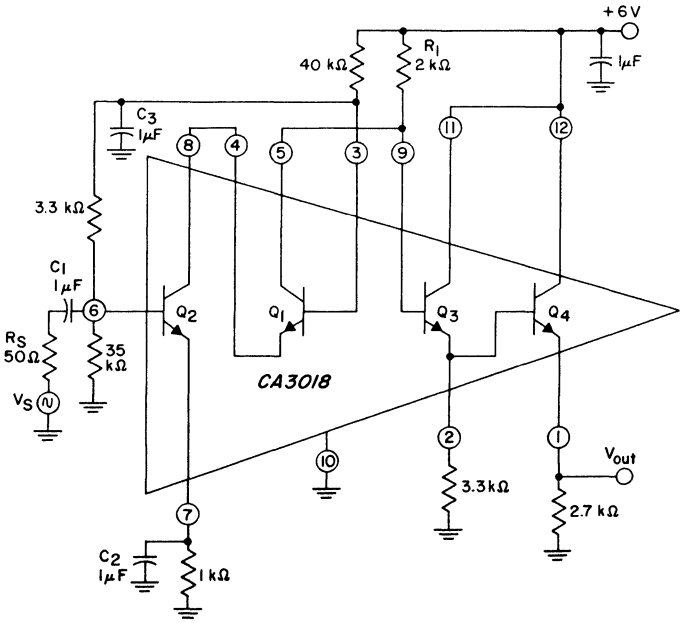


Fig. 299 — Schematic diagram for a CA3018 cascode video amplifier.

The frequency response of the cascode video amplifier is shown in Fig. 300. The lower and upper 3-dB points occur at frequencies of 6 kHz and 11 MHz, respectively. The lower 3-dB point is primarily a function of capacitors C_1, C_2, and C_3. The upper 3-dB point is a function of the devices and of the load resistor R_1, and is 10.5 MHz at −55°C and 5 MHz at +125°C.

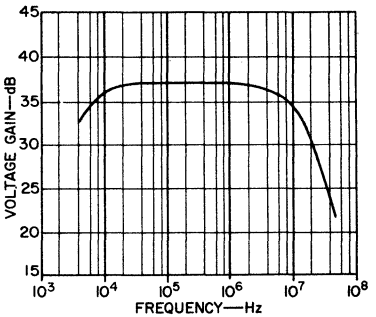
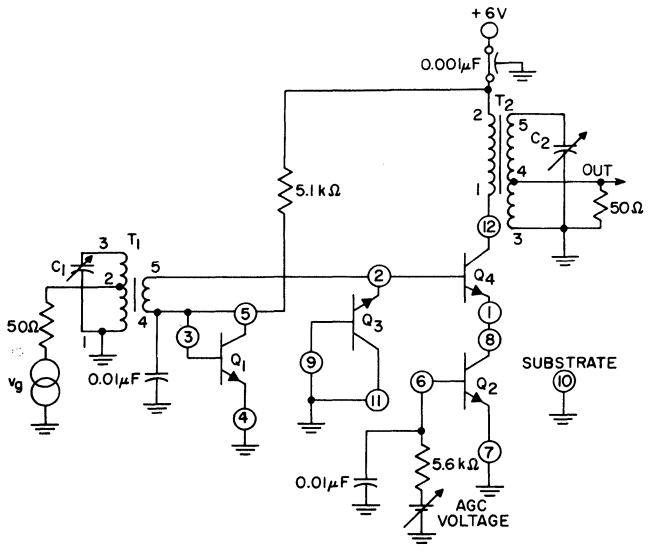
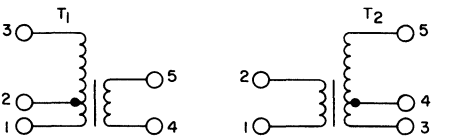


Fig. 300 — Voltage gain as a function of frequency for the cascode amplifier of Fig. 299.

The mid-frequency voltage gain of the amplifier is 37 dB ± 1 dB over the temperature range from −55°C to +125°C. The power dissipation varies from 16.8 milliwatts at −55°C to 17.6 milliwatts at +125°C. The amplifier has a tangential sensitivity of 40 microvolts peak-to-peak and a useful dynamic input range from 40 microvolts to 16.6 millivolts peak-to-peak.

15-MHz RF Amplifier — Fig. 301 shows a typical design approach for a tuned amplifier for use in the frequency range of 2 to 30 MHz in military receivers. This circuit was designed for a mid-band frequency of 15 MHz to demonstrate its capability. Gain is obtained in a common-emitter stage (Q_4). Transistor Q_2 is used





$L = 0.8\ \mu H$
$Q_o = 200$
$T_{1-3} = 6T$
$T_{1-2} = 1T$
$T_{4-5} = 2T$

$L = 0.8\ \mu H$
$Q_o = 200$
$T_{3-5} = 6T$
$T_{1-2} = 4T$
$T_{3-4} = 1T$

#22 wire on Q-2 material, CF107 Toroid from Indiana General.
C_1, C_2 = Arco 425 or equiv.

Fig. 301 — Schematic diagram for a CA3018 15-MHz rf amplifier.

as a variable resistor in the emitter of Q_4 to provide improved signal-handling capability with agc. Transistor Q_1 is used as a bias diode to stabilize Q_4 with temperature, and the reverse breakdown of Q_3 as a diode is used to protect the common-emitter stage from signal overdrive of adjacent transmitters.

The tuned-circuit design of Fig. 301 utilizes mismatching to obtain stability. Although the usable stable gain for a common-emitter amplifier using this type of transistor is 26 dB at 15 MHz, the tuned rf amplifier was designed for a total gain of 20 dB to obtain greater stability and more uniform performance with device variations. The general performance characteristics of the circuit are as follows:

Power Gain	20 dB
Power-Gain Variation from −55 to ±125°C	±1 dB
Bandwidth	315 kHz
Noise Figure at Full Gain	7.4 dB
AGC Range	45 dB
Power Dissipation	1.8 mW

Fig. 302 shows the cross-modulation characteristics of the circuit for in-band signals. For out-of-band undesired signals, the cross-modulation performance is improved by the amount of attenuation provided by the input tuned circuit. Cross-modulation performance also improves (i.e. more interfering signal voltage is required for cross-modulation distortion of 10 per cent) with increased agc as a result of the degeneration in the emitter of Q_4.

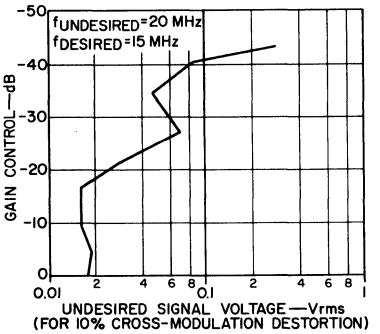


Fig. 302 — In-band cross-modulation characteristic of the 15-MHz amplifier of Fig. 301 (data taken with untuned input).

Final IF Amplifier Stage and Second Detector — Fig. 303 illustrates the use of the CA3018 as a last if amplifier and second detector (0.1 volt emitter voltage on terminal 1). The bias on transistor Q_4 is maintained at approximately cutoff to permit the cascaded emitter-follower configuration (Q_3 and Q_4) to be used as a second detector. Because this stage is driven by a common collector configuration, the input impedance to the detector can be kept high. A low output load impedance can be used as a result of the output current capability of the cascaded emitter-follower configuration. The input impedance (terminal 9) of approximately 9000 ohms is largely determined by the bias network. A minimum if input power of 0.4 microwatt must be delivered to terminal 9 for linear operation. The audio output power for 60 per cent modulation for this drive condition is 0.8 microwatt. Linear detection is obtained through an input range of 20 dB for 60 per cent modulation. This detector arrangement requires less power-output capability from the last if amplifier than a conventional diode detector yet allows a low dc load resistor to achieve a good ac-to-dc ratio for the first audio amplifier.

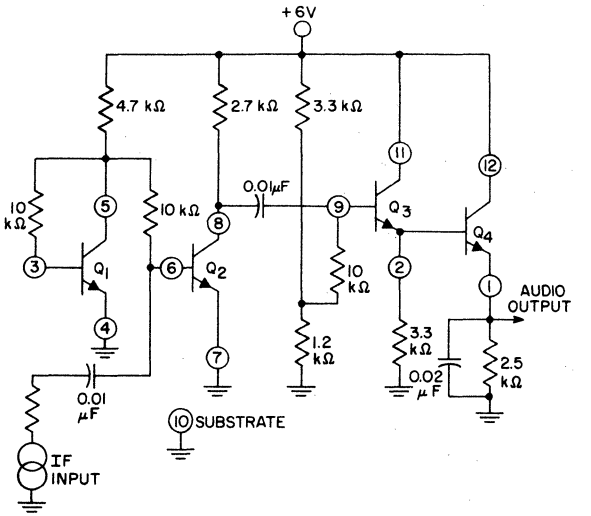
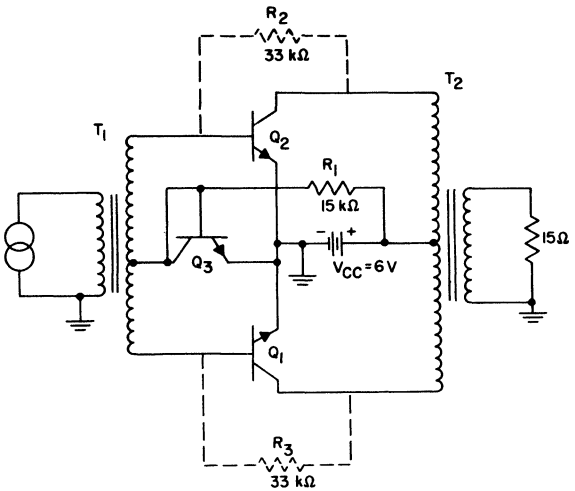


Fig. 303 — Schematic diagram for a CA3018 final if amplifier and second detector.

The if amplifier of Fig. 303 has a voltage gain of 30 dB at 1 MHz. Transistor Q_1 is used in the base-bias loop of the common-emitter amplifier Q_2 to stabilize the output operating point against temperature variations. This arrangement also eliminates

the need for an emitter resistor and bypass capacitor, and thus provides a larger voltage-swing capability for Q_2. If Q_2 is biased conventionally with base-bias resistors, Q_1 can be made available for the first audio or agc amplifier.

Class B Amplifier — Characteristics were obtained on a low-level class B amplifier to establish the idling-current performance of nearly identical devices on a single chip with respect to temperature variations. The transistors in the CA3018 can be used only for low-power class B operation (maximum output of 40 milliwatts) because of the h_{FE} roll-off and moderately high saturation resistance at high currents. A typical circuit is shown in Fig. 304. Idling-current bias is provided to Q_1 and Q_2 by use of transistor Q_3 as a diode (with collector and base shorted) and connection of a series resistor to the supply. The idling current for each transistor in the class B output is equal to the current established in



T_1 — ADC Products No. 5SX1322 or equiv.
T_2 — Chicago Standard Trans. Corp. No. TA-10 or equiv.
Note: R_1 is removed when R_2 and R_3 are added.

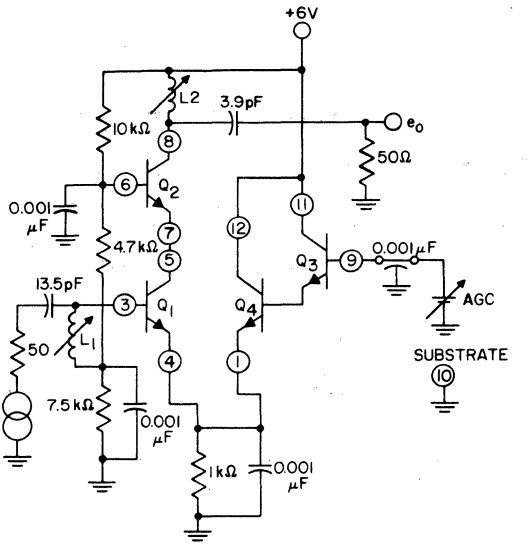
Fig. 304 — Schematic diagram for a CA3018 class B amplifier.

the resistance-diode loop. Because the resistor R_1 is the predominant factor in controlling the current in the bias loop, the bias current is relatively independent of temperature. In addition, because the devices have nearly equal characteristics and are at the same temperature, the idling current is nearly independent through the

full military temperature range. The total idling current for transistors Q_1 and Q_2 in Fig. 304 varies from 0.5 to 0.6 milliampere from −55 to +125°C. Excellent balance between output devices is achieved throughout the range.

AC feedback as well as dc feedback can be obtained by substitution of two resistors R_2 and R_3 in place of R_1, as shown by the dotted lines in Fig. 304. These two resistors, which have a parallel combination equal to R_1, are connected between collector and base of transistors Q_2 and Q_1. The added feedback reduces the power gain by approximately 6 dB (30 to 24 dB), but improves the linearity of the circuit. Although the output-power capability for the circuit shown in Fig. 304 is approximately 18 milliwatts, output levels up to 40 milliwatts can be obtained in similar configurations with optimized components.

100-MHz Tuned RF Amplifier — Fig. 305 illustrates the use of the CA3018 in a 100-MHz cascode circuit with an agc amplifier. Transistors Q_1 and Q_2 are used in a cascode configuration, and transistors Q_3 and Q_4 are used to provide an agc capability and amplification. With a positive-going agc signal, current in the cascode amplifier is transferred to the Darlington configuration by differential-amplifier action. This agc amplifier has the advantage



$L_1 = 0.11$ to 0.17 μH
$L_2 = 0.5$ to 0.8 μH

Fig. 305 — Schematic diagram for a CA3018 100-MHz cascode amplifier.

of low-power drive (high input impedance). In addition, the emitter of Q_1 can be back-biased with respect to the base to provide larger input-signal-handling capability under full agc conditions.

The operating characteristics of the amplifier shown in Fig. 305 are as follows:

Power Gain	— 26 dB
Agc Range	— 70 dB
3-dB Bandwidth	— 4.5 MHz
Noise Figure	— 6.8 dB
Power Dissipation	— 7.7 mW

The response characteristic is shown in Fig. 306.

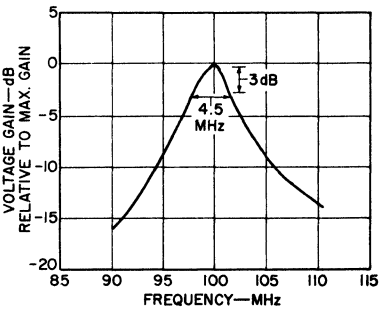


Fig. 306 — Response characteristics of 100-MHz amplifier of Fig. 305.

DUAL DARLINGTON ARRAY

The CA3036 integrated-circuit array may be used to provide two independent low-noise wide-band amplifier channels. These arrays are designed to operate over a range of ambient temperatures from —55°C to +125°C and are supplied in 10-terminal TO-5 style metal packages. They are particularly useful for preamplifier and low-level amplifier applications in single-channel or stereo systems.

Fig. 307 shows the schematic diagram of the CA3036 array. The array consists of four transistors connected to form two independent Darlington pairs. Fig. 308 shows a block diagram that illustrates the use of the array in a typical stereo phonograph. The CA3036 can be mounted directly on a stereo cartridge. Because of the low noise, high input impedance, and low output impedance or the array, only minimal shielding is required from the pickup to the amplifier. The buffering action of the CA3036 also substantially reduces losses and decreases hum pickup.

The CA3036 array features matched transistors with emitter-follower outputs, low-noise performance, and a gain-bandwidth product typically of 200 MHz. Typical applications of the array include stereo phonograph amplifiers, low-level stereo and single-channel stages, low-noise emitter-follower differential amplifiers, and operational-amplifier drivers.

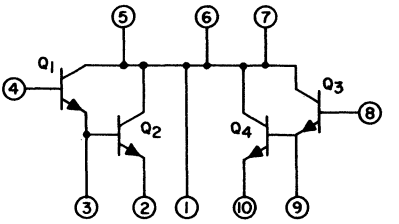


Fig. 307 — Schematic diagram of the CA3036 integrated-circuit dual Darlington array.

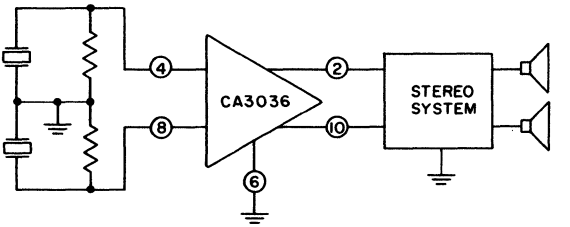


Fig. 308—Block Diagram of Stereo System using CA3036 as Phono Preamplifier.

Technical Data

This section lists ratings and typical operating characteristics for all current RCA linear integrated circuits. These data provide a convenient, readily accessible source of information that is useful in the selection of the optimum circuit type for a particular application. For complete descriptive data on specific circuits being considered, as well as information on test setups and methods used to determine circuit operating characteristics, the prospective user should consult the technical bulletins for individual types. Because the technical bulletins are frequently updated to include the latest available circuit information, reference to the appropriate bulletin is an important step in any proposed application of RCA linear integrated circuits.

DC AMPLIFIER — CA3000

General-purpose amplifier used in Schmitt-trigger, RC-coupled feedback-amplifier, mixer, comparator, crystal-oscillator, sense-amplifier, and modulator applications. 10-lead "TO-5" package; Outline No. 1. For schematic diagram and characteristics curves, see Fig. 71 and Figs. 73 through 82.

MAXIMUM RATINGS

Positive DC Supply Voltage	V_{CC}	+10	V
Negative DC Supply Voltage	V_{EE}	−10	V
Input Signal Voltage:			
Single-ended		±2	V
Common-mode		±2	V
Total Device Dissipation		300	mW
Temperature Range:			
Operating		−55 to +125	°C
Storage		−65 to +200	°C

TYPICAL CHARACTERISTICS (At ambient temperature = 25°C, V_{CC} = + 6V, V_{EE} = −6V)

Input Offset Voltage	V_{IO}	1.4	mV
Input Offset Current	I_{IO}	1.2	μA
Input Bias Current	I_I	23	μA

TYPICAL CHARACTERISTICS (continued)

Quiescent Operating Voltage:			
Terminals 4 and 5 not connected	V_8 or V_{10}	2.6	V
Terminal 4 not connected, terminal 5 connected to V_{EE}	V_8 or V_{10}	4.2	V
Terminal 4 connected to V_{EE}, terminal 5 not connected	V_8 or V_{10}	−1.5	V
Terminals 4 and 5 connected to V_{EE}	V_8 or V_{10}	0.6	V
Device Dissipation	P_T	30	mW
Differential Voltage Gain (Single-Ended Input, f = 1 kHz):			
Single-ended output	A_{DIFF}	32	dB
Double-ended output	A_{DIFF}	37	dB
-3-dB Bandwidth	BW	650	kHz
Maximum Output-Voltage Swing (f = 1 kHz)	V_{out}(P-P)	6.4	V_{p-p}
Common-Mode Rejection Ratio (f = 1 kHz)	CMR	98	dB
Single-Ended Input Impedance (f = 1 kHz)	Z_{in}	195	kΩ
Single-Ended Output Impedance (f = 1 kHz)	Z_{out}	8	kΩ
Total Harmonic Distortion (f = 1 kHz)	THD	0.2	%
Useful Frequency Range		dc to 30	MHz
AGC Range (Maximum voltage gain to complete cutoff, f = 1 kHz)	AGC	90	dB

CA3001

VIDEO AND WIDE-BAND AMPLIFIER

General-purpose amplifier used in dc, if, and video amplifier, Schmitt-trigger, mixer, and modulator applications. 12-lead "TO-5" package; Outline No. 2. For schematic diagram and characteristics curves, see Fig. 92 and Figs. 94 through 101.

MAXIMUM RATINGS

Positive DC Supply Voltage	V_{CC}	+10	V
Negative DC Supply Voltage	V_{EE}	−10	V
Input Signal Voltage			
Single-ended		±2.5	V
Common-mode		±2.5	V
Total Device Dissipation		300	mW
Temperature Range:			
Operating		−55 to 125	°C
Storage		−65 to 200	°C

TYPICAL CHARACTERISTICS (At ambient temperature = 25°C, V_{CC} = +6V, V_{EE} = −6V)

Input Offset Voltage	V_{IO}	1.5	mV
Input Offset Current	I_{IO}	3.4	μA
Input Bias Current	I_I	10	μA
Output Offset Voltage	V_{OO}	52	mV
Quiescent Operating Voltage:			
Terminals 4 and 5 not connected	V_8 or V_{11}	4.4	V
Terminal 4 not connected, terminal 5 connected to V_{EE}	V_8 or V_{11}	4.8	V

TYPICAL CHARACTERISTICS (continued)

Terminal 4 connected to V_{EE}, terminal 5 not connected	V_8 or V_{11}	2.9	V
Terminals 4 and 5 connected to V_{EE}	V_8 or V_{11}	3.9	V
Device Dissipation	P_T	80	mW
Differential Voltage Gain (Single-ended input and output):			
f = 1.75 MHz	A_{DIFF}	19	dB
f = 20 MHz	A_{DIFF}	14	dB
-3-dB Bandwidth	BW	16	MHz
Maximum Output Voltage Swing (f = 1.75 MHz)	V_{out}(P-P)	5	V_{p-p}
Noise Figure:			
R_S = 1 kΩ, f = 1.75 MHz	NF	5	dB
R_S = 1 kΩ, f = 11.7 MHz	NF	7.7	dB
Common-Mode Rejection Ratio (f = 1 kHz)	CMR	70	dB
Parallel Input Resistance (f = 1.75 MHz)	R_{in}	50	kΩ
Parallel Input Capacitance (f = 1.75 MHz)	C_{in}	7	pF
Output Resistance (f = 1.75 MHz)	R_{out}	70	Ω
Useful Frequency Range		dc to 20	MHz
AGC Range (Maximum voltage gain to complete cutoff, f = 1.75 MHz)	AGC	60	dB

IF AMPLIFIER — CA3002

General-purpose amplifier used in video amplifier, product and AM detector applications. 10-lead "TO-5" package; Outline No. 1. For schematic diagram and characteristics curves, see Fig. 104 and Figs. 106 through 114.

MAXIMUM RATINGS

Positive DC Supply Voltage	V_{CC}	+10	V
Negative DC Supply Voltage	V_{EE}	−10	V
Input Signal Voltage (Single-ended)		±3.5	V
Total Device Dissipation		300	mW
Temperature Range:			
Operating		−55 to 125	°C
Storage		−65 to 200	°C

TYPICAL CHARACTERISTICS (At ambient temperature = 25°C, V_{CC} = +6V, V_{EE} = −6V)

Input Unbalance Voltage	V_{IU}	2.2	mV
Input Unbalance Current	I_{IU}	2.2	μA
Input Bias Current	I_I	20	μA
Quiescent Operating Voltage:			
Terminal 2 connected to V_{EE}, terminal 4 not connected		2.8	V
Terminals 2 and 4 connected to V_{EE}		3.9	V
Device Dissipation	P_T	55	mW
Differential Voltage Gain (Single-Ended Input and Output, f = 1.75 MHz)	A_{DIFF}	24	dB
-3-dB Bandwidth	BW	11	MHz

TYPICAL CHARACTERISTICS (continued)

Maximum Output Voltage Swing	V_{out}(P-P)	5.5	V_{p-p}
Noise Figure (R_S = 1 kΩ, f = 1.75 MHz)	NF	4	dB
Parallel Input Resistance (f = 1.75 MHz)	R_{in}	100	kΩ
Parallel Input Capacitance (f = 1.75 MHz)	C_{in}	4	pF
Output Resistance (f = 1.75 MHz)	R_{out}	70	Ω
3rd Harmonic Intermodulation Distortion	IMD	—40	dB
Useful Frequency Range		dc to 15	MHz
AGC Range (Maximum Voltage Gain to Complete Cutoff, f = 1.75 MHz)	AGC	80	dB

CA3004 RF AMPLIFIER

General-purpose amplifier used in push-pull input and output, wide- and narrow-band amplifier, agc, detector, mixer, limiter, and modulator applications. 12-lead "TO-5" package; Outline No. 2. For schematic diagram and characteristics curves, see Figs. 138, 139, 143, 144, 149, 154, 157, and 163.

MAXIMUM RATINGS

Positive DC Supply Voltage	V_{CC}	+12 V
Negative DC Supply Voltage	V_{EE}	—12 V
Input Signal Voltage:		
Single-ended		±3.5 V
Common-mode		+3.5 to —2.5 V
Total Device Dissipation		300 mW
Temperature Range:		
Operating		—55 to 125 °C
Storage		—65 to 200 °C

TYPICAL CHARACTERISTICS (At ambient temperature = 25°C, V_{CC} = +6V, V_{EE} = —6V)

Input Offset Voltage	V_{IO}	1.7	mV
Input Offset Current	I_{IO}	0.125	μA
Input Bias Current	I_I	21	μA
Quiescent Operating Current:			
Terminals 4 and 5 not connected	I_9 or I_{11}	1	mA
Terminal 4 connected to V_{EE}, terminal 5 not connected	I_9 or I_{11}	2.7	mA
Terminal 4 not connected, terminal 5 connected to V_{EE}	I_9 or I_{11}	0.45	mA
Terminals 4 and 5 connected to V_{EE}	I_9 or I_{11}	1.25	mA
Quiescent Operating Current Ratio	I_9/I_{11}	1.1	
Device Dissipation	P_T	26	mW
Power Gain (f = 100 MHz)	G_P	12	dB
Noise Figure (f = 100 MHz)	NF	6.3	dB
Common-Mode Rejection Ratio (f = 1 kHz)	CMR	98	dB
Useful Frequency Range		dc to 120	MHz
AGC Range (Maximum Voltage Gain to Complete Cutoff, f = 1.75 MHz)	AGC	—60 min	dB

RF AMPLIFIER CA3005

General-purpose amplifier used in push-pull input and output, wide- and narrow-band amplifier, agc, detector, mixer, limiter, modulator, and cascode amplifier applications. 12-lead "TO-5" package; Outline No. 2. For schematic diagram and characteristics curves, see Figs. 138, 140, 143, 145, 146, 150, 151, 154 through 161, and 163 through 166.

MAXIMUM RATINGS

Positive DC Supply Voltage	V_{CC}	+12 V
Negative DC Supply Voltage	V_{EE}	−12 V
Input Signal Voltage:		
Single-ended		±3.5 V
Common-mode		+3.5 to −2.5 V
Total Device Dissipation		300 mW
Temperature Range:		
Operating		−55 to 125 °C
Storage		−65 to 200 °C

TYPICAL CHARACTERISTICS (At ambient temperature = 25°C, V_{CC} = +6V, V_{EE} = −6V)

Input Offset Voltage	V_{IO}	2.6	mV
Input Offset Current	I_O	1.4	μA
Input Bias Current	I_I	19	μA
Quiescent Operating Current:			
Terminals 4 and 5 not connected	I_{10} or I_{11}	1	mA
Terminal 4 not connected, terminal 5 connected to V_{EE}	I_{10} or I_{11}	2.7	mA
Terminal 4 connected to V_{EE}, terminal 5 not connected	I_{10} or I_{11}	0.45	mA
Terminals 4 and 5 connected to V_{EE}	I_{10} or I_{11}	1.25	mA
Quiescent Operating Current Ratio	I_{10}/I_{11}	1.05	
Device Dissipation	P_T	26	mW
Power Gain (f = 100 MHz):			
Cascode circuit	G_P	20	dB
Differential-amplifier circuit	G_P	16	dB
Noise Figure (f = 100 MHz):			
Cascode circuit	NF	7.8	dB
Differential-amplifier circuit	NF	7.8	dB
Common-Mode Rejection Ratio (f = 1 kHz)	CMR	101	dB
Useful Frequency Range		dc to 120	MHz
AGC Range (Maximum Voltage Gain to Complete Cutoff, f = 1.75 MHz)	AGC	−60 min	dB

RF AMPLIFIER CA3006

General-purpose amplifier used in push-pull input and output, wide- and narrow-band amplifier, agc, detector, mixer, limiter, modulator, and cascode amplifier applications. 12-lead "TO-5" package; Out-

line No. 2. For schematic diagram and characteristics curves, see Figs. 138, 140, 143, 145, 146, 150, 151, 154 through 161, and 163 through 166. This type is identical to type CA3005 except for the following item:

TYPICAL CHARACTERISTICS (At ambient temperature = 25°C, $V_{CC} = +6V$, $V_{EE} = -6V$)

Input Offset Voltage	V_{IO}	0.8	mV

CA3007 AF AMPLIFIER

Special-purpose audio amplifier used in audio driver applications, sound systems, and communications equipment. 12-lead "TO-5" package; Outline No. 2. For schematic diagram, see Fig. 89.

MAXIMUM RATINGS

Positive DC Supply Voltage	V_{CC}	+10	V
Negative DC Supply Voltage	V_{EE}	−10	V
Input Signal Voltage:			
Single-ended		±2.5	V
Common-mode		±2.5	V
Total Device Dissipation		300	mW
Temperature Range:			
Operating		−55 to 125	°C
Storage		−65 to 200	°C

TYPICAL CHARACTERISTICS (At ambient temperature = 25°C, $V_{CC} = +6V$, $V_{EE} = -6V$)

Input Unbalance Voltage	V_{IU}	0.57	mV
Input Unbalance Current	I_{IU}	0.57	μA
Input Bias Current	I_I	11	μA
Quiescent Operating Voltage	V_8 or V_{10}	0.87	V
Device Dissipation	P_T	30	mW
Power Gain (f = 1 kHz)	G_P	22	dB
Total Harmonic Distortion (f = 1 kHz)	THD	0.28	%
Useful Frequency Range		dc to 20	kHz
Common-Mode Rejection Ratio (f = 1 kHz)	CMR	77	dB
Input Impedance (f = 1 kHz)	Z_{in}	4	kΩ
Output Impedance (f = 1 kHz)	Z_{out}	60	Ω

CA3008 OPERATIONAL AMPLIFIER

General-purpose amplifier used in narrow-band and bandpass amplifier, feedback amplifier, dc and video amplifier, multivibrator, oscillator, comparator, and servo driver applications. 14-lead ceramic-and-metal flat package; Outline No. 3. For schematic diagram and characteristics curves, see Figs. 197 through 208.

MAXIMUM RATINGS

Positive DC Supply Voltage	V_{CC} +10	V
Negative DC Supply Voltage	V_{EE} −10	V
Input Signal Voltage (Single-ended)	+1, −4	V
Total Device Dissipation	300	mW
Temperature Range:		
Operating	−55 to 125	°C
Storage	−65 to 200	°C

TYPICAL CHARACTERISTICS (At ambient temperature = 25°C, V_{CC} = +6V, V_{EE} = −6V)

Input Offset Voltage	V_{IO}	1.08	mV
Input Offset Current	I_{IO}	0.54	μA
Input Bias Current	I_I	5.3	μA
Input Offset Voltage Sensitivity:			
Positive	$\triangle V_{IO}/\triangle V_{CC}$	0.103	mV/V
Negative	$\triangle V_{IO}/\triangle V_{EE}$	0.260	mV/V
Device Dissipation:			
Terminal 8 not connected	P_T	30	mW
Terminal 8 shorted to terminal 12	P_T	102	mW
Open-Loop Differential Voltage Gain (f = 1 kHz)	A_{OL}	60	dB
Open-Loop —3-dB Bandwidth	BW_{OL}	300	kHz
Common-Mode Rejection Ratio (f = 1 kHz)	CMR	94	dB
Maximum Output-Voltage Swing (f = 1 kHz)	V_O(P-P)	6.75	V_{p-p}
Input Impedance (f = 1 kHz)	Z_{in}	14	kΩ
Output Impedance (f = 1 kHz)	Z_{out}	200	Ω
Useful Frequency Range		dc to 15	MHz
Common-Mode Input-Voltage Range (f = 1 kHz)	V_{CMR}	+0.5, −4	V

OPERATIONAL AMPLIFIER CA3008A

General-purpose amplifier used in narrow-band and bandpass amplifier, feedback, dc and video amplifier, multivibrator, oscillator, comparator, and servo driver applications. 14-lead ceramic-and-metal flat package; Outline No. 3. For schematic diagram and characteristics curves, see Figs. 196 through 208. This type is identical to type CA3008 except for the following items:

TYPICAL CHARACTERISTICS (At ambient temperature = 25°C, V_{CC} = +6V, V_{EE} = −6V)

Input Offset Voltage	V_{IO}	0.9	mV
Input Offset Current	I_{IO}	0.3	μA
Input Bias Current	I_I	2.5	μA
Input Impedance	Z_{in}	20	kΩ
Output Impedance	Z_{out}	160	Ω
Noise Figure	NF	8.3	dB

CA3010 OPERATIONAL AMPLIFIER

General-purpose amplifier used in narrow-band and bandpass amplifier, feedback amplifier, dc and video amplifier, multivibrator, oscillator, comparator, and servo driver applications. 12-lead "TO-5" package; Outline No. 2. For schematic diagram and characteristics curves, see Figs. 197 through 208. This type is electrically identical to type CA3008.

CA3010A OPERATIONAL AMPLIFIER

General-purpose amplifier used in narrow-band and bandpass amplifier, feedback, dc and video amplifier, multivibrator, oscillator, comparator, and servo driver applications. 12-lead "TO-5" package; Outline No. 2. For schematic diagram and characteristics curves, see Figs. 196 through 208. This type is identical to type CA3010 except for the following items:

TYPICAL CHARACTERISTICS (At ambient temperature = 25°C, V_{CC} = +6V, V_{EE} = −6V)

Input Offset Voltage	V_{IO}	0.9	mV
Input Offset Current	I_{IO}	0.3	μA
Input Bias Current	I_I	2.5	μA
Input Impedance	Z_{in}	20	kΩ
Output Impedance	Z_{out}	160	Ω
Noise Figure	NF	8.3	dB

CA3011 FM IF AMPLIFIER

Special-purpose amplifier used in if amplifiers for FM broadcast and TV sound applications. 10-lead "TO-5" package; Outline No. 1. For schematic diagram and characteristics curves, see Figs. 253, 255 through 258, and 260.

MAXIMUM RATINGS

Positive DC Supply Voltage	V_{CC}	+10	V
Recommended Minimum DC Supply Voltage (V_{CC})		5.5	V
Input Signal Voltage (Single-ended)		±3	V
Total Device Dissipation		300	mW
Temperature Range:			
Operating		−55 to 125	°C
Storage		−65 to 200	°C

TYPICAL CHARACTERISTICS (At ambient temperature = 25°C, V_{CC} = +7.5V)

Device Dissipation	P_T	120	mW

TYPICAL CHARACTERISTICS (continued)

Voltage Gain:			
f = 1 MHz	A	70	dB
f = 4.5 MHz	A	67	dB
f = 10.7 MHz	A	61	dB
Parallel Input Resistance (f = 4.5 MHz)	R_{in}	3	kΩ
Parallel Input Capacitance (f = 4.5 MHz)	C_{in}	7	pF
Parallel Output Resistance (f = 4.5 MHz)	R_{out}	31.5	kΩ
Parallel Output Capacitance (f = 4.5 MHz)	C_{out}	4.2	pF
Noise Figure (f = 4.5 MHz)	NF	8.7	dB
Useful Frequency Range	100 kHz to > 20 MHz		
Input Limiting Voltage, Knee (f = 4.5 MHz)	V_i(lim)	300	μV

FM IF AMPLIFIER — CA3012

Special-purpose amplifier used in if amplifiers for FM broadcast and TV sound applications. 10-lead "TO-5" package; Outline No. 1. For schematic diagram and characteristics curves, see Figs. 253, 255 through 258, and 260. This type is electrically identical to type CA3011 except for the following item:

MAXIMUM RATINGS

Positive DC Supply Voltage	V_{CC}	+13	V

FM IF AMPLIFIER/ DISCRIMINATOR/AF AMPLIFIER — CA3013

Special-purpose amplifier used in if amplifier, AM and noise limiter, FM detector, and af preamplifier applications. 10-lead "TO-5" package; Outline No. 1. For schematic diagram and characteristics curves, see Figs. 254 through 260.

MAXIMUM RATINGS

Positive DC Supply Voltage	V_{CC}	+10	V
Recommended Minimum DC Supply Voltage (V_{CC})		5.5	V
Input Signal Voltage (Between terminals 1 and 2)		±3	V
Total Device Dissipation		300	mW
Temperature Range:			
Operating		−55 to 125	°C
Storage		−65 to 200	°C

TYPICAL CHARACTERISTICS (At ambient temperature = 25°C, V_{CC} = +7.5V)

Device Dissipation	P_T	120	mW
Voltage Gain:			
f = 1 MHz	A	70	dB
f = 4.5 MHz	A	67	dB

TYPICAL CHARACTERISTICS (continued)

f = 10.7 MHz	A	60	dB
Parallel Input Resistance (f = 4.5 MHz)	R_{in}	3	kΩ
Parallel Input Capacitance (f = 4.5 MHz)	C_{in}	7	pF
Parallel Output Resistance (f = 4.5 MHz)	R_{out}	31.5	kΩ
Parallel Output Capacitance (f = 4.5 MHz)	C_{out}	4.2	pF
Noise Figure (f = 4.5 MHz)	NF	8.7	dB
Input Limiting Voltage, Knee (f = 4.5 MHz)	V_i(lim)	300	μV
Recovered AF Voltage (f = 4.5 MHz)	V_o(af)	188	mV
Amplitude Modulation Rejection (f = 4.5 MHz)	AMF	50	dB
Discriminator Output Resistance (f = 4.5 MHz)	R_o(disc)	60	Ω
Useful Frequency Range	100 kHz to > 20 MHz		
Total Harmonic Distortion (f = 4.5 MHz)	THD	1.8	%

CA3014 FM IF AMPLIFIER/ DISCRIMINATOR/AF AMPLIFIER

Special-purpose amplifier used in if amplifier, AM and noise limiter, FM detector, and af preamplifier applications. 10-lead "TO-5" package; Outline No. 1. For schematic diagram and characteristics curves, see Figs. 254 through 260. This type is identical to type CA3013 except for the following item:

MAXIMUM RATINGS

Positive DC Supply Voltage	V_{CC}	+13	V

CA3015 OPERATIONAL AMPLIFIER

General-purpose amplifier used in narrow-band and bandpass amplifier, feedback amplifier, dc and video amplifier, multivibrator, oscillator, comparator, and servo driver applications. 12-lead "TO-5" package; Outline No. 2. For schematic diagram and characteristics curves, see Figs. 225 and 226.

MAXIMUM RATINGS

Positive DC Supply Voltage	V_{CC}	+20	V
Negative DC Supply Voltage	V_{EE}	−20	V
Input Signal Voltage (Single-ended)		+1, −8	V
Total Device Dissipation		600	mW
Temperature Range:			
Operating		−55 to 125	°C
Storage		−65 to 200	°C

TYPICAL CHARACTERISTICS (At ambient temperature = 25°C, V_{CC} = +12V, V_{EE} = −12V)

Input Offset Voltage	V_{IO}	1.37	mV
Input Offset Current	I_{IO}	1.07	μA
Input Bias Current	I_I	9.6	μA

TYPICAL CHARACTERISTICS (continued)

Input Offset Voltage Sensitivity:			
Positive	$\Delta V_{IO}/\Delta V_{CC}$	0.096	mV/V
Negative	$\Delta V_{IO}/\Delta V_{EE}$	0.156	mV/V
Device Dissipation:			
Terminal 5 not connected	P_T	175	mW
Terminal 5 shorted to terminal 9	P_T	500	mW
Open-Loop Differential Voltage Gain (f = 1 kHz)	A_{OL}	70.2	dB
Open-Loop —3-dB Bandwidth	BW_{OL}	320	kHz
Common-Mode Rejection Ratio (f = 1 kHz)	CMR	103.5	dB
Maximum Output-Voltage Swing (f = 1 kHz)	V_O(P-P)	14	V_{p-p}
Input Impedance (f = 1 kHz)	Z_{in}	7.8	kΩ
Ouput Impedance (f = 1 kHz)	Z_{out}	92	Ω
Useful Frequency Range		dc to 50	MHz
Common-Mode Input-Voltage Range (f = 1 kHz)	V_{CMR}	+0.65, —8	V

OPERATIONAL AMPLIFIER CA3015A

General-purpose amplifier used in narrow-band and bandpass amplifier, feedback amplifier, dc and video amplifier, multivibrator, oscillator, comparator, and servo driver applications. 12-lead "TO-5" package; Outline No. 2. For schematic diagram and characteristics curves, see Figs. 196, 225, and 226. This type is identical to type CA3015 except for the following items:

TYPICAL CHARACTERISTICS (At ambient temperature = 25°C, V_{CC} = +12V, V_{EE} = —12V)

Input Offset Voltage	V_{IO}	1	mV
Input Offset Current	I_{IO}	0.5	μA
Input Bias Current	I_I	4.7	μA
Input Impedance	Z_{in}	10	kΩ
Output Impedance	Z_{out}	85	Ω
Noise Figure	NF	11	dB

OPERATIONAL AMPLIFIER CA3016

General-purpose amplifier used in narrow-band and bandpass amplifier, feedback amplifier, dc and video amplifier, multivibrator, oscillator, comparator, and servo driver applications. 14-lead ceramic-to-metal flat package; Outline No. 3. For schematic diagram and characteristics curves, see Figs. 225 and 226. This type is electrically identical to type CA3015.

CA3016A OPERATIONAL AMPLIFIER

General-purpose amplifier used in narrow-band and bandpass amplifier, feedback, dc and video amplifier, multivibrator, oscillator, comparator, and servo driver applications. 14-lead ceramic-and-metal flat package; Outline No. 3. For schematic diagram and characteristics curves, see Figs. 196, 225, and 226. This type is identical to type CA3016 except for the following items:

TYPICAL CHARACTERISTICS (At ambient temperature = 25°C, V_{CC} = +12V, V_{EE} = −12V)

Input Offset Voltage	V_{IO}	1	mV
Input Offset Current	I_{IO}	0.5	μA
Input Bias Current	I_I	4.7	μA
Input Impedance	Z_{in}	10	kΩ
Output Impedance	Z_{out}	85	Ω
Noise Figure	NF	11	dB

CA3018 TRANSISTOR ARRAY

General-purpose array consisting of two isolated transistors and two transistors with a common base-emitter terminal used in 100-MHz cascode amplifier, final if amplifier and 2nd detector, 15-MHz tuned rf amplifier, video amplifier, class B amplifier, and cascode video amplifier applications. 12-lead "TO-5" package; Outline No. 2. For schematic diagram, see Fig. 297.

MAXIMUM RATINGS

Each Transistor:			
Collector-to-Emitter Voltage	V_{CEO}	15	V
Collector-to-Base Voltage	V_{CBO}	20	V
Emitter-to-Base Voltage	V_{EBO}	4	V
Collector Current	I_C	50	mA
Device Dissipation:			
Any one transistor	P_S	300	mW
Total package	P_T	300	mW
Ambient Temperature:			
Operating		−55 to 125	°C
Storage		−65 to 200	°C

TYPICAL CHARACTERISTICS (At ambient temperature = 25°C)

Each Transistor:			
Collector-to-Substrate Breakdown Voltage (I_C = 10μA, I_{C1} = 0)	$V_{(BR)CIO}$	20 min	V
Emitter-to-Base Breakdown Voltage (I_E = 10μA, I_C = 0)	$V_{(BR)EBO}$	4 min	V
Collector-to-Emitter Breakdown Voltage (I_C = 1mA, I_B = 0)	$V_{(BR)CEO}$	15 min	V

TYPICAL CHARACTERISTICS (continued)

Collector-to-Base Breakdown Voltage ($I_C = 10\mu A$, $I_E = 0$)	$V_{(BR)CBO}$	20 min	V
Collector-Cutoff Current:			
$V_{CB} = 5V$, $I_E = 0$	I_{CBO}	0.1 max	μA
$V_{CE} = 15V$, $I_B = 0$	I_{CEO}	10 max	μA
Static Forward-Current Transfer Ratio:			
Static Beta, $V_{CE} = 3V$, $I_C = 1mA$	h_{FE}	67	
Transistors with common base-emitter terminal Q_3 and Q_4, $V_{CE} = 3V$, $I_C = 1mA$	h_{FEC}	3500	
Magnitude of Static Beta Ratio, Isolated transistors Q_1 and Q_2 ($V_{CE} = 3V$, $I_{C1} = I_{C2} = 1mA$)	$\frac{h_{FE1}}{h_{FE2}}$	1	
Magnitude of Input-Offset Voltage, Isolated transistors Q_1 and Q_2 ($V_{CC} = +6V$, $V_{EE} = -6V$, $I_{C1} = I_{C2} = 1mA$)	$\lvert V_{BE1}-V_{BE2}\rvert$	1	mV
Temperature Coefficient, Magnitude of Input-Offset Voltage ($V_{CC} = +6V$, $V_{EE} = -6V$, $I_{C1} = I_{C2} = 1mA$)	$\frac{V_{BE1}-V_{BE2}}{\Delta T}$	10	$\mu V/°C$
Small-Signal Forward-Current Transfer Ratio ($V_{CE} = 3V$, $I_C = 1mA$, $f = 1kHz$)	h_{fe}	70	
Small-Signal Input Impedance ($V_{CE} = 3V$, $I_C = 1mA$, $f = 1kHz$)	h_{ie}	2800	Ω
Small-Signal Output Impedance ($V_{CE} = 3V$, $I_C = 1mA$, $f = 1kHz$)	h_{oe}	35	μmho
Small-Signal Reverse Voltage-Transfer Ratio ($V_{CE} = 3V$, $I_C = 1mA$, $f = 1kHz$)	h_{re}	6.5×10^{-4}	
Forward Transfer Admittance ($V_{CE} = 3V$, $I_C = 1mA$, $f = 1MHz$)	Y_{fe}	$31 - j\,1.5$	mmho
Input Admittance ($V_{CE} = 3V$, $I_C = 1mA$, $f = 1MHz$)	Y_{ie}	$0.3 + j\,0.05$	mmho
Output Admittance ($V_{CE} = 3V$, $I_C = 1mA$, $f = 1MHz$)	Y_{oe}	$0.02 + j\,0.05$	mmho
Gain-Bandwidth Product (Substrate (terminal 10) connected to ground)	f_T	400	MHz
Output Capacitance ($V_{CB} = 3V$, $I_E = 0$)	C_{cbo}	1.9	pF
Input Capacitance ($V_{BE} = 3V$, $I_C = 0$)	C_{ibo}	1.8	pF
Collector-to-Substrate Capacitance ($V_{C1} = 3V$, $I_C = 0$)	C_{c1o}	3.5	pF

DIODE ARRAY CA3019

One diode "quad" and two isolated diodes on a common substrate used for modulator, mixer, balanced modulator, analog switch, and diode gate for chopper-modulator applications. 10-lead "TO-5"

package; Outline No. 1. For schematic diagrams, see Figs. 283 and 284.

MAXIMUM RATINGS

Device Dissipation:		
Any one diode unit	20	mW
Total for device	120	mW
Diode Voltage Limits	−3 to +12	V
Temperature Range:		
Operating	−55 to 125	°C
Storage	−65 to 200	°C

TYPICAL CHARACTERISTICS (At ambient temperature = 25°C)

DC Forward Voltage Drop (I_F = 1mA)	V_F	0.73	V
DC Reverse Breakdown Voltage (I_R = −10μA):			
Any diode	$V_{(BR)R}$	6	V
Any diode and substrate	$V_{(BR)R}$	80	V
DC Reverse Leakage Current (V_R = −4V):			
Any diode	I_R	0.0055	μA
Any diode and substrate	I_R	0.010	μA
Magnitude of Diode Offset (Difference in DC Forward Voltage Drops of any Two Units) (I_F = 1mA)	$\lvert V_{F1} - V_{F2} \rvert$	1	mV
Single Diode Capacitance (V_R = −2V, f = 1MHz)	C_D	1.8	pF
Diode Quad-to-Substrate Capacitance (V_R between terminals 2, 5, 6, or 8 of diode quad and terminal 7 (substrate) = −2V):			
Terminal 2 or 6 to terminal 7	C_{DQ-1}	4.4	pF
Terminal 5 or 8 to terminal 7	C_{DQ-1}	2.7	pF
Series Gate Switching Pedestal Voltage	V_S	10	mV

CA3020 MULTIPURPOSE WIDE-BAND POWER AMPLIFIER

Special-purpose amplifier used in audio applications; combines functions of preamplifier, phase-inverter, driver, and power-output stages. 12-lead "TO-5" package; Outline No. 2. For schematic diagrams and characteristics curves, see Figs. 237 through 244.

MAXIMUM RATINGS

Positive DC Supply Voltage:			
Differential Amplifier	V_{CC}	+12	V
Push-Pull Amplifier	V_{CC}	+20	V
Input Signal Voltage (Single-ended)		±3	V
Total Device Dissipation:			
At ambient temperatures up to 25°C		600	mW
At ambient temperatures above 25°C	Derate at 4.8 mW/°C		

MAXIMUM RATINGS (continued)

Temperature Range:	
Operating	—55 to 125 °C
Storage	—65 to 200 °C

TYPICAL CHARACTERISTICS (At ambient temperature = 25°C,

Positive Supply Voltage	V_{CC}	3	6	9	V
Zero-Signal Current Drain	I_{min}	7	14	22	mA
Maximum-Signal Current Drain	I_{max}	47	105	145	mA
Maximum Power Output	P_{out}	65	300	550	mW
Transducer Power Gain	G_p	—	58	—	dB
—3-dB Bandwidth	BW	—	6	—	MHz
Signal-to-Noise Ratio	S/N	—	70	—	dB
Total Harmonic Distortion	THD	—	1	—	%
Sensitivity	e_{in}	—	35	—	mV
Useful Frequency Range			dc to 8		MHz
Circuit Efficiency	η	—	45	—	%
Input Resistance (f = 1 kHz):					
Terminal 3 to ground	R_{in3}	—	600	—	Ω
Terminal 10 to ground	R_{in10}	—	40	—	kΩ

VIDEO AND WIDE-BAND AMPLIFIER

CA3021

General-purpose amplifier used in gain-controlled linear amplifier, AM/FM if amplifier, video amplifier, and limiter applications. 12-lead "TO-5" package; Outline No. 2. For schematic diagrams and characteristics curves, see Figs. 119 through 133.

MAXIMUM RATINGS

Positive DC Supply Voltage	V_{CC}	+18	V
Negative DC Supply Voltage	V_{EE}	−6	V
Input Signal Voltage (Single-ended)		±3	V
Total Device Dissipation		120	mW
Temperature Range:			
Operating		—55 to 125	°C
Storage		—65 to 200	°C

TYPICAL CHARACTERISTICS (At ambient temperature = 25°C, V_{CC} = +6V, V_{EE} = 0)

Device Dissipation	P_T	4	mW
Quiescent Output Voltage	V_o	2.2	V
AGC Source Current (V_{AGC} = 6V)	I_{AGC}	0.8	mA
Voltage Gain (f = 0.5 MHz)	A	56	dB
—3-dB Bandwidth	BW	2.4	MHz
Input Resistance (f = 1 MHz)	R_{in}	4	kΩ
Input Capacitance (f = 1 MHz)	C_{in}	11	pF
Output Resistance (f = 1 MHz)	R_{out}	300	Ω
Noise Figure (f = 1 MHz)	NF	4.2	dB
AGC Range (f = 1 MHz)	AGC	33	dB
Useful Frequency Range		dc to 6	MHz
Maximum Output Voltage (f = 1 MHz)	v_{out}	0.6	V_{rms}

CA3022

VIDEO AND WIDE-BAND AMPLIFIER

General-purpose amplifier used in gain-controlled linear amplifier, AM/FM if amplifier, video amplifier, and limiter applications. 12-lead "TO-5" package; Outline No. 2. For schematic diagrams and characteristics curves, see Figs. 119 through 133. For maximum ratings, refer to type CA3021.

TYPICAL CHARACTERISTICS (At ambient temperature = 25°C, V_{CC} = +6V, V_{EE} = 0)

Device Dissipation	P_T	12.5	mW
Quiescent Output Voltage	V_O	1.9	V
AGC Source Current (V_{AGC} = 6V)	I_{AGC}	0.8	mA
Voltage Gain (f = 2.5 MHz)	A	57	dB
−3-dB Bandwidth	BW	7.5	MHz
Input Resistance (f = 5 MHz)	R_{in}	1300	Ω
Input Capacitance (f = 5 MHz)	C_{in}	18	pF
Output Resistance (f = 5 MHz)	R_{out}	120	Ω
Noise Figure (f = 1 MHz)	NF	4.4	dB
AGC Range (f = 5 MHz)	AGC	33	dB
Useful Frequency Range		dc to 20	MHz
Maximum Output Voltage (f = 5 MHz)	v_{out}	0.7	V_{rms}

CA3023

VIDEO AND WIDE-BAND AMPLIFIER

General-purpose amplifier used in gain-controlled linear amplifier, AM/FM if amplifier, video amplifier, and limiter applications. 12-lead "TO-5" package; Outline No. 2. For schematic diagrams and characteristics curves, see Figs. 119 through 133. For maximum ratings, refer to type CA3021.

TYPICAL CHARACTERISTICS (At ambient temperature = 25°C, V_{CC} = +6V, V_{EE} = 0)

Device Dissipation	P_T	35	mW
Quiescent Output Voltage	V_O	1.3	V
AGC Source Current (V_{AGC} = 6V)	I_{AGC}	0.8	mA
Voltage Gain (f = 5 MHz)	A	53	dB
−3-db Bandwidth	BW	16	MHz
Input Resistance (f = 10 MHz)	R_{in}	300	Ω
Input Capacitance (f = 10 MHz)	C_{in}	13	pF
Output Resistance (f = 10 MHz)	R_{out}	100	Ω
Noise Figure (f = 1 MHz)	NF	6.5	dB
AGC Range (f = 10 MHz)	AGC	33	dB
Useful Frequency Range		dc to 40	MHz
Maximum Output Voltage (f = 10 MHz)	v_{out}	0.5	V_{rms}

DIFFERENTIAL/ CASCODE AMPLIFIER

CA3028A

General-purpose amplifier used in differential or cascode if amplifier, converter for FM broadcast band, limiter, mixer, oscillator, and audio, sense, and dc amplifier applications. 8-lead "TO-5" package; Outline No. 4. For schematic diagram and characteristics curves, see Figs. 138, 152, 153, 162, and 168.

MAXIMUM RATINGS

Positive DC Supply Voltage	V_{CC}	+18	V
Negative DC Supply Voltage	V_{EE}	−6	V
Input Signal Voltage (Single-ended)		6	V_{p-p}
Total Device Dissipation		300	mW
Temperature Range:			
Operating		−55 to 125	°C
Storage		−65 to 200	°C

TYPICAL CHARACTERISTICS (At ambient temperature = 25°C)

		Differential Amplifier	*Cascode Amplifier*	
Quiescent Operating Current:				
V_{CC} = +9V	I_6 or I_8	2.5	—	mA
V_{CC} = +12V	I_6 or I_8	3.4	—	mA
Input Bias Current:				
V_{CC} = +9V	I_I	29	—	μA
V_{CC} = +12V	I_I	44	—	μA
AGC Bias Current (Into Constant-Current Source Terminal No. 7):				
V_{AGC} = +9V	I_{AGC}	1.28		mA
V_{AGC} = +12V	I_{AGC}	1.65		mA
Device Dissipation:				
V_{CC} = +9V	P_T	56		mW
V_{CC} = +12V	P_T	113		mW
Power Gain:				
V_{CC} = +9V, f = 100 MHz	G_P	17	20	dB
V_{CC} = +9V, f = 10.7 MHz	G_P	32	39	dB
Noise Figure:				
(V_{CC} = +9V, f = 100 MHz)	NF	6.7	7.2	dB
Input Admittance				
(V_{CC} = +9V, f = 10.7 MHz)	Y_{11}	0.5 + j0.5	0.6 + j1.6	mmho
Reverse Transfer Admittance				
(V_{CC} = +9V, f = 10.7 MHz)	Y_{12}	0.01 − j0.0002	0.0003 − j0	mmho
Forward Transfer Admittance				
(V_{CC} = +9V, f = 10.7 MHz)	Y_{21}	−37 + j0.5	99 − j18	mmho
Output Admittance				
(V_{CC} = +9V, f = 10.7 MHz)	Y_{22}	0.04 + j0.23	0 + j0.08	mmho
Power Output (Untuned)				
(V_{CC} = +9V, f = 10.7 MHz)	P_O	5.7	—	μW
Voltage Gain				
(V_{CC} = +9V, R_L = 1 kΩ, f = 10.7 MHz)	A	32	98	dB
Useful Frequency Range		dc to 120		MHz
AGC Range, Maximum Power Gain to Full Cutoff:				
(V_{CC} = +9V, f = 10.7 MHz)	AGC	62	—	dB

CA3029 OPERATIONAL AMPLIFIER

General-purpose amplifier used in narrow-band and bandpass amplifier, feedback amplifier, dc and video amplifier, multivibrator, oscillator, comparator, servo driver, scaling adder, and balanced modulator-driver applications. 14-lead dual in-line plastic package; Outline No. 6. For schematic diagram and characteristics curves, see Figs. 197 through 208.

MAXIMUM RATINGS

Positive DC Supply Voltage	V_{CC}	+10 V
Negative DC Supply Voltage	V_{EE}	−10 V
Input Signal Voltage		+1, −4 V
Total Device Dissipation		300 mW
Temperature Range:		
Operating		0 to 70 °C
Storage		−25 to 85 °C

TYPICAL CHARACTERISTICS (At ambient temperature = 25°C, V_{CC} = +6V, V_{EE} = −6V)

Input Offset Voltage	V_{IO}	1.08	mV
Input Offset Current	I_{IO}	0.54	μA
Input Bias Current	I_I	5.3	μA
Input Offset Voltage Sensitivity:			
Positive	$\triangle V_{IO}/\triangle V_{CC}$	0.103	mV/V
Negative	$\triangle V_{IO}/\triangle V_{EE}$	0.260	mV/V
Device Dissipation:			
Terminal 8 not connected	P_T	30	mW
Terminal 8 shorted to 12	P_T	102	mW
Open-Loop Differential Voltage Gain (f = 1 kHz)	A_{OL}	60	dB
Open-Loop —3-dB Bandwidth	BW_{OL}	300	kHz
Common-Mode Rejection Ratio (f = 1 kHz)	CMR	94	dB
Maximum Output-Voltage Swing (f = 1 kHz)	V_O(P-P)	6.75	V_{p-p}
Input Impedance (f = 1 kHz)	Z_{in}	14	kΩ
Output Impedance (f = 1 kHz)	Z_{out}	200	Ω
Useful Frequency Range		dc to 15	MHz
Common-Mode Input-Voltage Range (f = 1 kHz)	V_{CMR}	+0.5, −4	V

CA3029A OPERATIONAL AMPLIFIER

General-purpose amplifier used in narrow-band and bandpass amplifier, dc and video amplifier, multivibrator, oscillator, comparator, and servo driver applications. 14-lead TO-116 dual-in-line plastic package; Outline No. 6. For schematic diagram and characteristics curves, see Figs. 196 through 208. This type is identical to type CA3029 except for the following items:

TYPICAL CHARACTERISTICS (At ambient temperature = 25°C, V_{CC} = +6V, V_{EE} = −6V)

Input Offset Voltage	V_{IO}	0.9	mV
Input Offset Current	I_{IO}	0.3	μA
Input Bias Current	I_I	2.5	μA
Input Impedance	Z_{in}	20	kΩ
Output Impedance	Z_{out}	160	Ω
Noise Figure	NF	8.3	dB

OPERATIONAL AMPLIFIER CA3030

General-purpose amplifier used in narrow-band and bandpass amplifier, feedback amplifier, dc and video amplifier, multivibrator, oscillator, comparator, servo driver, scaling adder, and balanced modulator-driver applications. 14-lead dual in-line plastic package; Outline No. 6. For schematic diagram and characteristics curves, ses Figs. 225 and 226.

MAXIMUM RATINGS

Positive DC Supply Voltage	V_{CC}	+20	V
Negative DC Supply Voltage	V_{EE}	−20	V
Total Device Dissipation		600	mW
Temperature Range:			
Operating		0 to 70	°C
Storage		−25 to 85	°C

TYPICAL CHARACTERISTICS (At ambient temperature = 25°C, V_{CC} = +12V, V_{EE} = −12V)

Input Offset Voltage	V_{IO}	1.37	mV
Input Offset Current	I_{IO}	1.07	μA
Input Bias Current	I_I	9.6	μA
Input Offset Voltage Sensitivity:			
Positive	$\triangle V_{IO}/\triangle V_{CC}$	0.096	mV/V
Negative	$\triangle V_{IO}/\triangle V_{EE}$	0.156	mV/V
Device Dissipation:			
Terminal 8 not connected	P_T	175	mW
Terminal 8 shorted to 12	P_T	500	mW
Open-Loop Differential Voltage Gain (f = 1 kHz)	A_{OL}	70.2	dB
Open-Loop —3-dB Bandwidth	BW_{OL}	320	kHz
Common-Mode Rejection Ratio (f = 1 kHz)	CMR	103.5	dB
Maximum Output-Voltage Swing (f = 1 kHz)	V_O(P-P)	14	V_{p-p}
Input Impedance (f = 1 kHz)	Z_{in}	7.8	kΩ
Output Impedance (f = 1 kHz)	Z_{out}	92	Ω
Useful Frequency Range		dc to 50	MHz
Common-Mode Input-Voltage Range (f = 1 kHz)	V_{CMR}	+0.65, −8	V

CA3030A OPERATIONAL AMPLIFIER

General-purpose amplifier used in narrow-band and bandpass amplifier, feedback, dc and video amplifier, multivibrator, oscillator, comparator, and servo driver applications. 14-lead TO-116 plastic dual-in-line package; Outline No. 6. For schematic diagram and characteristics curves, see Figs. 196, 225, and 226. This type is identical to type CA3030 except for the following items:

TYPICAL CHARACTERISTICS (At ambient temperature = 25°C, $V_{CC} = +12V$, $V_{EE} = -12V$)

Input Offset Voltage	V_{IO}	1	mV
Input Offset Current	I_{IO}	0.5	μA
Input Bias Current	I_I	4.7	μA
Input Impedance	Z_{in}	10	kΩ
Output Impedance	Z_{out}	85	Ω
Noise Figure	NF	11	dB

CA3031/702A OPERATIONAL AMPLIFIER

General-purpose amplifier used in narrow-band and bandpass amplifier, feedback amplifier, dc and video amplifier, multivibrator, oscillator, comparator, servo driver, and scaling adder applications. 8-lead "TO-5" package; Outline No. 4.

MAXIMUM RATINGS

Positive DC Supply Voltage	V_{CC} +18	V
Negative DC Supply Voltage	V_{EE} −12	V
Input Signal Voltage (Single-ended)	+1.5, −8	V
Total Device Dissipation	300	mW
Temperature Range:		
Operating	−55 to 125	°C
Storage	−65 to 200	°C

TYPICAL CHARACTERISTICS (At ambient temperature = 25°C, $V_{CC} = +12V$, $V_{EE} = -6V$)

Input Offset Voltage	V_{IO}	2	mV
Input Offset Current	I_{IO}	0.5	μA
Input Bias Current	I_I	3	μA
Input Offset Voltage Sensitivity:			
Positive	$\Delta V_{IO}/\Delta V_{CC}$	0.05	mV/V
Negative	$\Delta V_{IO}/\Delta V_{EE}$	0.065	mV/V
Device Dissipation	P_T	85	mW
Open-Loop Differential Voltage Gain (f = 1 kHz)	A_{OL}	70	dB
Open-Loop −3-dB Bandwidth	BW_{OL}	700	kHz
Common-Mode Rejection Ratio (f = 1 kHz)	CMR	85	dB

TYPICAL CHARACTERISTICS (continued)

Maximum Output-Voltage Swing (R_L = 100 kΩ, f = 1 kHz)	V_O(P-P)	10 min	V_{p-p}
Input Resistance (f = 1 kHz)	R_{in}	25	kΩ
Output Resistance (f = 1 kHz)	R_{out}	130	Ω
Useful Frequency Range		dc to 40	MHz
Common-Mode Input-Voltage Range (f = 1 kHz)	V_{CMR}	+0.5, −4	V

OPERATIONAL AMPLIFIER CA3032/702C

General-purpose amplifier used in narrow-band and bandpass amplifier, feedback amplifier, dc and video amplifier, multivibrator, oscillator, comparator, servo driver, and scaling adder applications. 8-lead "TO-5" package; Outline No. 4. The maximum ratings for this type are identical to type CA3031/702A, except for the temperature ranges mentioned below.

MAXIMUM RATINGS

Temperature Range:	
Operating	0 to 70 °C
Storage	−65 to 150 °C

TYPICAL CHARACTERISTICS (At ambient temperature = 25°) V_{CC} = +12V, V_{EE} = −6V)

Input Offset Voltage	V_{IO}	5	mV
Input Offset Current	I_{IO}	1.5	μA
Input Bias Current	I_I	5	μA
Device Dissipation	P_T	90	mW
Open-Loop Differential Voltage Gain (f = 1 kHz)	A_{OL}	70	dB
Open-Loop −3-dB Bandwidth	BW_{OL}	700	kHz
Common-Mode Rejection Ratio (f = 1 kHz)	CMR	80	dB
Maximum Output-Voltage Swing (R_L = 100 kΩ, f = 1 kHz)	V_O(P-P)	10 min	V_{p-p}
Input Resistance (f = 1 kHz)	R_{in}	20	kΩ
Output Resistance (f = 1 kHz)	R_{out}	200	Ω
Useful Frequency Range		dc to 40	MHz
Common-Mode Input-Voltage Range (f = 1 kHz)	V_{CMR}	+0.5, −4	V

OPERATIONAL AMPLIFIER CA3033

General-purpose amplifier used in narrow-band and bandpass amplifier, feedback amplifier, dc and video amplifier, multivibrator, oscillator, comparator, and servo driver applications. 14-lead TO-116 dual-in-line ceramic package; Outline No. 7.

MAXIMUM RATINGS

Input Signal Voltage	±10	V
Device Dissipation	600	mW
Temperature Range:		
Operating	—55 to 125	°C
Storage	—65 to 200	°C

TYPICAL CHARACTERISTICS (At ambient temperature = 25°C, V_{CC} = +12V, V_{EE} = −12V)

Input Offset Voltage	V_{IO}	2.6	mV
Input Offset Current	I_{IO}	5	nA
Input Bias Current	I_I	83	nA
Input Offset Voltage Sensitivity:			
Positive	$\Delta V_{IO}/\Delta V_{CC}$	0.3	mV/V
Negative	$\Delta V_{IO}/\Delta V_{EE}$	0.3	mV/V
Device Dissipation	P_T	120	mW
Open-Loop Differential Voltage Gain (f = 1 kHz)	A_{OL}	84	dB
Open-Loop −3-dB Bandwidth	BW_{OL}	100	kHz
Common-Mode Rejection Ratio	CMR	94	dB
Common-Mode Input-Voltage Range (f = 1 kHz)	V_{CMR}	+5, −9	V
Input Impedance (f = 1 kHz)	Z_{in}	1.5	MΩ
Output Current (R_L = 500Ω, f = 1 kHz)	I_O	44	mA_{p-p}
Maximum Output-Voltage Swing (f = 1 kHz)	V_O(P-P)	21	V_{p-p}
Slew Rate	SR	6	V/μs
Power Output (R_L = 500Ω, f = 1 kHz)	P_O	122	mW

CA3033A OPERATIONAL AMPLIFIER

General-purpose amplifier used in narrow-band and bandpass amplifier, feedback amplifier, dc and video amplifier, multivibrator, oscillator, comparator, and servo driver applications. 14-lead TO-116 dual-in-line ceramic package; Outline No. 7.

MAXIMUM RATINGS

Input Signal Voltage	±10	V
Device Dissipation	600	mW
Temperature Range:		
Operating	—55 to 125	°C
Storage	—65 to 200	°C

TYPICAL CHARACTERISTICS (At ambient temperature = 25°C, V_{CC} = +18V, V_{EE} = −18V)

Input Offset Voltage	V_{IO}	2.86	mV
Input Offset Current	I_{IO}	9	nA
Input Bias Current	I_I	103	nA
Input Offset Voltage Sensitivity:			
Positive	$\Delta V_{IO}/\Delta V_{CC}$	0.2	mV/V
Negative	$\Delta V_{IO}/\Delta V_{EE}$	0.2	mV/V
Device Dissipation	P_T	290	mW
Open-Loop Differential Voltage Gain (f = 1 kHz)	A_{OL}	91	dB

TYPICAL CHARACTERISTICS (continued)

Open-Loop —3-dB Bandwidth	BW_{OL}	110	kHz
Common-Mode Rejection Ratio (f = 1 kHz)	CMR	103	dB
Common-Mode Input-Voltage Range (f = 1 kHz)	V_{CMR}	+7, —12	V
Input Impedance (f = 1 kHz)	Z_{in}	1	MΩ
Output Current (R_L = 500Ω, f = 1 kHz)	I_O	64	mA_{p-p}
Maximum Output-Voltage Swing (f = 1 kHz)	V_O(P-P)	32	V_{p-p}
Slew Rate	SR	10	V/μs
Power Output (R_L = 500Ω, f = 1 kHz)	P_O	255	mW

HIGH-FREQUENCY WIDE-BAND AMPLIFIER/ PHASE DETECTOR — CA3034

Special-purpose amplifier used in differential input amplifier, dual phase detector with differential output amplifier, and afc applications. 10-lead "TO-5" package; Outline No. 1. For schematic diagrams, see Figs. 278 and 279.

MAXIMUM RATINGS

Input Signal Voltage (Single-ended)	12	V_{p-p}
Supply Voltage	15	V
Total Device Dissipation	300	mW
Temperature Range:		
Operating	—55 to 125	°C
Storage	—65 to 200	°C

TYPICAL CHARACTERISTICS (At ambient temperature = 25°C, V_{CC} = 10V)

Total Current Drain	I_d	9	mA
Quiescent Operating Current into Terminal 2	I_2	1.9	mA
Reference Voltage at Terminal 9	V_9	5.5	V
Quiescent Operating Voltage at Terminal 4	V_4	5.5	V
Quiescent Operating Voltage at Terminal 5	V_5	5.5	V
Output Offset Voltage between Terminals 4 and 5	V_{4-5}	0	V
Input Impedance (Terminal 7)	Z_{in}	2	kΩ

HIGH-FREQUENCY WIDE-BAND AMPLIFIER/ PHASE DETECTOR — CA3034V1

Special-purpose amplifier used in differential input amplifier, dual phase detector with differential output amplifier, and afc applications. 10-formed-lead "TO-5" package; Outline No. 5. For sche-

matic diagrams, see Figs. 278 and 279. This type is electrically identical to type CA3034.

CA3035 ULTRA-HIGH-GAIN WIDE-BAND AMPLIFIER ARRAY

General-purpose amplifier with three individual amplifiers used in remote-control amplifier applications, such as TV receivers. 10-lead "TO-5" package; Outline No. 1. For schematic diagrams and characteristics curves, see Figs. 280 through 282.

MAXIMUM RATINGS

Input Signal Voltage (Single-ended)	1	V_{p-p}
Supply Voltage	15	V
Total Device Dissipation	300	mW
Temperature Range:		
Operating	—55 to 125	°C
Storage	—65 to 200	°C

TYPICAL CHARACTERISTICS (At ambient temperature = 25°C, V_{CC} = +9V)

Quiescent Operating Voltage	V_3	2	V
Quiescent Operating Voltage	V_5	1.9	V
Quiescent Operating Voltage	V_7	4.9	V
Total Current Drain (R_{L3} = 5 kΩ)	I_d	5	mA
Voltage Gain (f = 40 kHz):			
Amplifier 1	A_1	44	dB
Amplifier 2	A_2	46	dB
Amplifier 3	A_3	42	dB
Cascade		132	dB
Output Voltage Swing:			
Amplifier 1, R_{L1} = 10 kΩ	V_1 out	2	V_{p-p}
Amplifier 2, R_{L2} = 10 kΩ	V_2 out	2.6	V_{p-p}
Amplifier 3, R_{L3} = 5 kΩ	V_3 out	8	V_{p-p}
Input Resistance (f = 40 kHz):			
Amplifier 1	R_1 in	50	kΩ
Amplifier 2	R_2 in	2	kΩ
Amplifier 3	R_3 in	670	Ω
Output Resistance (f = 40 kHz):			
Amplifier 1	R_1 out	270	Ω
Amplifier 2	R_2 out	170	Ω
Amplifier 3	R_3 out	100	kΩ
—3-dB Bandwidth			
Amplifier 1	BW_1	500	kHz
Amplifier 2	BW_2	2.5	MHz
Amplifier 3	BW_3	2.5	MHz
Noise Figure (Amplifier 1) (R_S = 1 kΩ, f = 1 kHz)	NF_1	6	dB
Sensitivity (V_{CC} = +13V, Relay Current = 7.5 mA)		100	μV

ULTRA-HIGH-GAIN WIDE-BAND AMPLIFIER ARRAY — CA3035V1

General-purpose amplifier with three individual amplifiers used in remote-control amplifier applications, such as TV receivers. 10-formed-lead "TO-5" package; Outline No. 5. For schematic diagrams and characteristics curves, see Figs. 280 through 282. This type is electrically identical to type CA3035.

DUAL DARLINGTON ARRAY — CA3036

General-purpose amplifier with two independent low-noise wide-band amplifier channels used in stereo phonograph preamplifier, low-level stereo and single-channel amplifier stages, low-noise emitter-follower differential amplifier, and operational-amplifier driver applications. 10-lead "TO-5" package; Outline No. 1. For schematic diagram, see Fig. 307.

MAXIMUM RATINGS

Device Dissipation (Any one transistor or total for device)	300	mW
For Each Transistor In The Array:		
Collector-to-Emitter Voltage	15	V
Collector-to-Base Voltage	30	V
Emitter-to-Base Voltage	5	V
Collector Current	50	mA
Temperature Range:		
Operating	—55 to 125	°C
Storage	—65 to 200	°C

TYPICAL CHARACTERISTICS (At ambient temperature = 25°C)

For Each Transistor (Q_1, Q_2, Q_3, Q_4):			
Collector-to-Emitter Breakdown Voltage (I_C = 1 mA, I_B = 0)	$V_{(BR)CEO}$	20	V
Collector-to-Base Breakdown Voltage (I_C = 10 μA, I_E = 0)	$V_{(BR)CBO}$	44	V
Emitter-to-Base Breakdown Voltage (I_E = 10 μA, I_C = 0)	$V_{(BR)EBO}$	6	V
Collector-Cutoff Current:			
V_{CB} = 5V, I_E = 0	I_{CBO}	0.5 max	μA
V_{CE} = 15V, I_B = 0	I_{CEO}	5 max	μA
For Either Input Transistor (Q_1 or Q_3):			
Static Forward Current-Transfer Ratio (I_{C1} or I_{C3} = 1 mA)	h_{FE}	82	
Forward Transfer Admittance (I_{C1} or I_{C3} = 2 mA, f = 50 MHz)	y_{fe}	0.68 + j7.9	mmhos

TYPICAL CHARACTERISTICS (continued)

Input Admittance (Output Short-Circuited) (I_{C1} or I_{C3} = 2 mA, f = 50 MHz)	y_{ie}	4.14 + j5.95	mmhos
Output Admittance (Input Short-Circuited) (I_{C1} or I_{C3} = 2 mA, f = 50 MHz)	y_{oe}	1.94 + j2.64	mmhos
Reverse Transfer Admittance (Input Short-Circuited) (I_{C1} or I_{C3} = 2 mA, f = 50 MHz)	y_{re}	Negligible	mmhos
For Either Darlington Pair (Q_1, Q_2 or Q_3, Q_4):			
Emitter-to-Base Breakdown Voltage (I_{E2} or I_{E4} = 10 μA)	$V_{(BR)EBO(D)}$	12.6	V
Static Forward Current-Transfer Ratio (I_{C1} + I_{C2} or I_{C3} + I_{C4} = 1 mA)	$h_{FE(D)}$	4540	
Small-Signal Forward-Current Transfer Ratio (I_{C1} + I_{C2} or I_{C3} + I_{C4} = 1 mA, f = 1 kHz)	$h_{fe(D)}$	1300	
Small-Signal Input Impedance (I_{C1} + I_{C2} or I_{C3} + I_{C4} = 1 mA, f = 1 kHz)	$h_{ie(D)}$	82	kΩ
Small-Signal Output Admittance (I_{C1} + I_{C2} or I_{C3} + I_{C4} = 1 mA, f = 1 kHz)	$h_{oe(D)}$	108	μmhos
Small-Signal Reverse-Voltage Transfer Ratio (I_{C1} + I_{C2} or I_{C3} + I_{C4} = 1 mA, f = 1 kHz)	$h_{re(D)}$	2.7×10^{-4}	
Voltage Gain (I_{C1} + I_{C2} or I_{C3} + I_{C4} = 1 mA, f = 1 kHz)	$A_{(D)}$	26	dB
Power Gain (I_{C1} + I_{C2} or I_{C3} + I_{C4} = 1 mA, f = 1 kHz)	$G_{p(D)}$	47	dB
Noise Voltage (f = 1 kHz)	E_N	$0.05\frac{\mu V_{rms}}{\sqrt{f(Hz)}}$	
Input Admittance (I_{C1} + I_{C2} or I_{C3} + I_{C4} = 2 mA, f = 50 MHz)	$y_{ie(D)}$	1.71 + j2.8	mmhos
Output Admittance (I_{C1} + I_{C2} or I_{C3} + I_{C4} = 2 mA, f = 50 MHz)	$y_{oe(D)}$	3.96 + j2.6	mmhos
Gain-Bandwidth Product (I_{C1} + I_{C2} or I_{C3} + I_{C4} = 2 mA)	$f_{T(D)}$	200	MHz
For Each Input Transistor Q_1 or Q_3 (I_{C1} or I_{C3} = 1 mA, f = 1 kHz):			
Small-Signal Forward Current-Transfer Ratio	h_{fe}	82	
Small-Signal Input Impedance	h_{ie}	2.6	kΩ
Small-Signal Output Admittance	h_{oe}	7	μmhos
Small-Signal Reverse Voltage-Transfer Ratio	h_{re}	9.8×10^{-5}	

OPERATIONAL AMPLIFIER CA3037

General-purpose amplifier used in narrow-band and bandpass amplifier, feedback amplifier, dc and video amplifier, multivibrator, oscillator, comparator, and servo driver applications. 14-lead TO-116 dual-in-line ceramic package; Outline No. 7. For schematic diagram and characteristics curves, see Figs. 197 through 208. This type is electrically identical to type CA3008.

OPERATIONAL AMPLIFIER CA3037A

General-purpose amplifier used in narrow-band and bandpass amplifier, feedback amplifier, dc and video amplifier, multivibrator, oscillator, comparator, and servo driver applications. 14-lead TO-116 dual-in-line ceramic package; Outline No. 7. For schematic diagram and characteristics curves, see Figs. 196 through 208. This type is identical to type CA3037 except for the following items:

TYPICAL CHARACTERISTICS (At ambient temperature = 25°C, V_{CC} = +6V, V_{EE} = −6V)

Input Offset Voltage	V_{IO}	0.9	mV
Input Offset Current	I_{IO}	0.3	μA
Input Bias Current	I_I	2.5	μA
Input Impedance	Z_{in}	20	kΩ
Output Impedance	Z_{out}	160	Ω
Noise Figure	NF	8.3	dB

OPERATIONAL AMPLIFIER CA3038

General-purpose amplifier used in narrow-band and bandpass amplifier, feedback amplifier, dc and video amplifier, multivibrator, oscillator, comparator, and servo driver applications. 14-lead TO-116 dual-in-line ceramic package; Outline No. 7. For schematic diagram and characteristics curves, see Figs. 225 and 226. This type is electrically identical to type CA3016.

OPERATIONAL AMPLIFIER CA3038A

General-purpose amplifier used in narrow-band and bandpass amplifier, feedback, dc and video amplifier, multivibrator, oscillator, comparator, and servo driver applications. 14-lead TO-116 ceramic dual-in-line package; Outline No. 7. For schematic diagram and

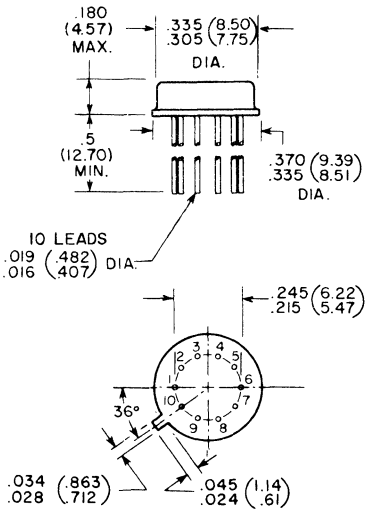
characteristics curves, see Figs. 196, 225, and 226. This type is identical to type CA3038 except for the following items:

TYPICAL CHARACTERISTICS (At ambient temperature = 25°C, V_{CC} = +12V, V_{EE} = −12V)

Input Offset Voltage	V_{IO}	1	mV
Input Offset Current	I_{IO}	0.5	μA
Input Bias Current	I_I	4.7	μA
Input Impedance	Z_{in}	10	kΩ
Output Impedance	Z_{out}	85	Ω
Noise Figure	NF	11	dB

Outlines

Dimensions shown in parentheses are in millimeters and are derived from the basic inch dimensions as indicated.



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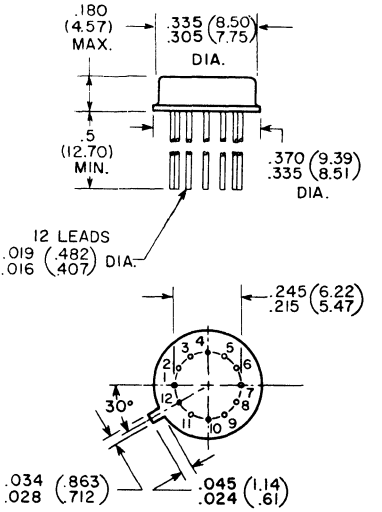

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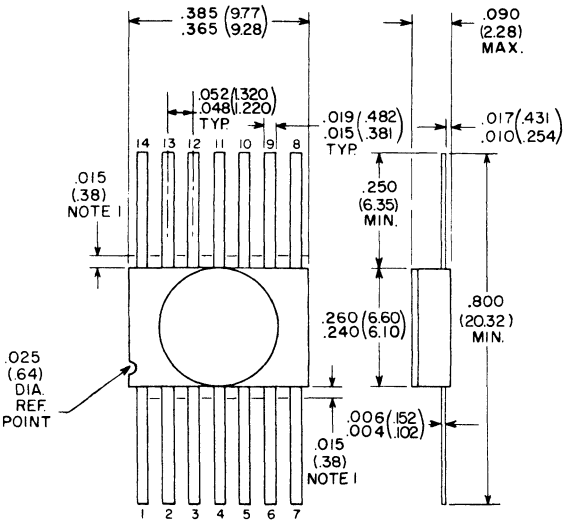

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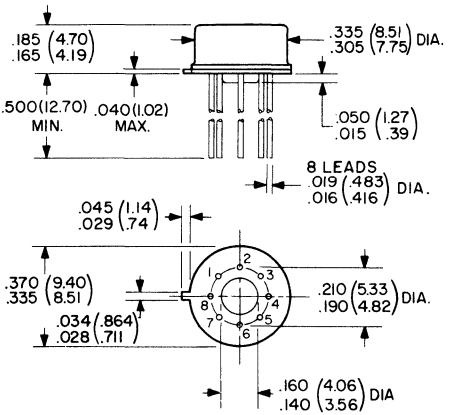
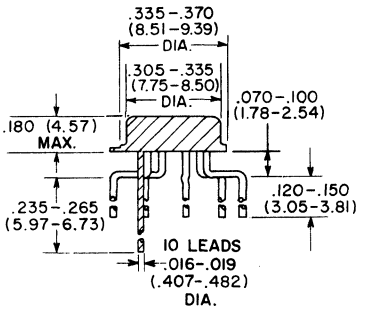
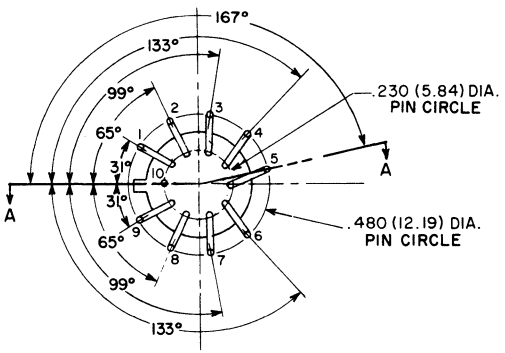

.185 (4.70)
.165 (4.19)
.335 (8.51)
.305 (7.75) DIA.
.500(12.70) MIN.
.040(1.02) MAX.
.050 (1.27)
.015 (.39)
8 LEADS
.019 (.483)
.016 (.416) DIA.
.045 (1.14)
.029 (.74)
.370 (9.40)
.335 (8.51)
.210 (5.33)
.190 (4.82) DIA.
.034(.864)
.028(.711)
.160 (4.06)
.140 (3.56) DIA

4


.335-.370
(8.51-9.39)
DIA.
.305-.335
(7.75-8.50)
DIA.
.070-.100
(1.78-2.54)
.180 (4.57)
MAX.
.120-.150
(3.05-3.81)
.235-.265
(5.97-6.73)
10 LEADS
.016-.019
(.407-.482)
DIA.


167°
133°
99°
65°
31°
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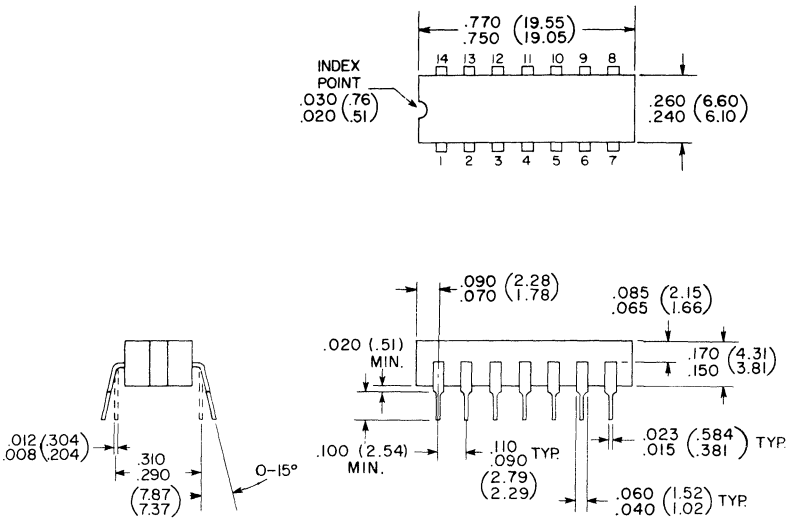
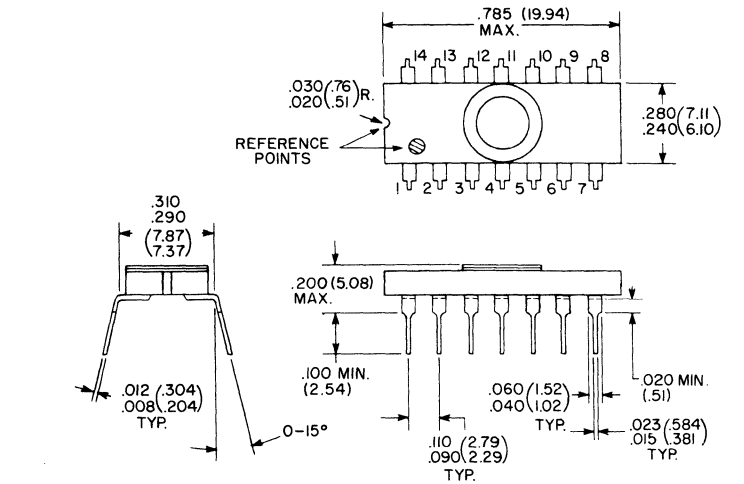
PIN CIRCLE
A
A
.480 (12.19) DIA.
PIN CIRCLE

5


.770 (19.55)
.750 (19.05)
14 13 12 11 10 9 8
INDEX POINT
.030 (.76)
.020 (.51)
.260 (6.60)
.240 (6.10)
1 2 3 4 5 6 7
.090 (2.28)
.070 (1.78)
.085 (2.15)
.065 (1.66)
.020 (.51) MIN.
.170 (4.31)
.150 (3.81)
.012 (.304)
.008 (.204)
.310
.290
(7.87)
(7.37)
0-15°
.100 (2.54) MIN.
.110
.090 TYP.
(2.79)
(2.29)
.023 (.584)
.015 (.381) TYP.
.060 (1.52)
.040 (1.02) TYP.

6


.785 (19.94)
MAX.
14 13 12 11 10 9 8
.030 (.76) R.
.020 (.51)
REFERENCE POINTS
.280 (7.11)
.240 (6.10)
1 2 3 4 5 6 7
.310
.290
(7.87)
(7.37)
.200 (5.08)
MAX.
.100 MIN.
(2.54)
.012 (.304)
.008 (.204)
TYP.
0-15°
.060 (1.52)
.040 (1.02)
TYP.
.020 MIN.
(.51)
.110 (2.79)
.090 (2.29)
TYP.
.023 (.584)
.015 (.381)
TYP.

7

Index