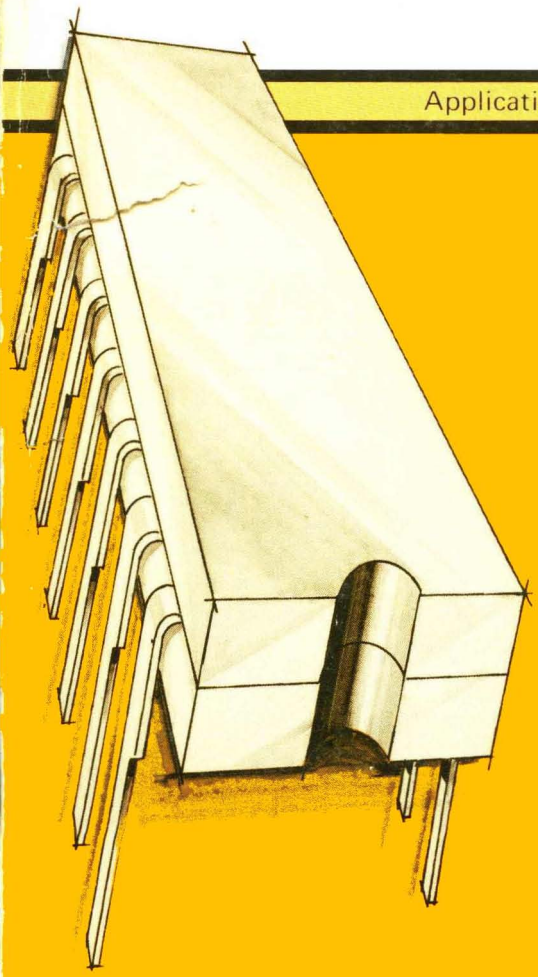
RCA

# LINEAR Integrated Circuits

Application Notes



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For ease of reference, the application notes in this book are arranged in numerical sequence. The index on pages 6-8 groups the notes in the same categories used in the SSD-201C selection charts: (a) operational amplifiers; (b) arrays; (c) differential and broadband (video) amplifiers; (d) power-control, computer-interface, and analog-multiplier circuits; (e) consumer circuits; (f) DMOS devices.

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RCA Solid State | Box 3200 | Somerville, N.J., U.S.A. 08876
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# Operating Considerations for RCA Solid State Devices

Solid state devices are being designed into an increasing variety of electronic equipment because of their high standards of reliability and performance. However, it is essential that equipment designers be mindful of good engineering practices in the use of these devices to achieve the desired performance.

This Note summarizes important operating recommendations and precautions which should be followed in the interest of maintaining the high standards of performance of solid state devices.

The ratings included in RCA Solid State Devices data bulletins are based on the Absolute Maximum Rating System, which is defined by the following Industry Standard (JEDEC) statement:

Absolute-Maximum Ratings are limiting values of operating and environmental conditions applicable to any electron device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

The device manufacturer chooses these values to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in device characteristics.

The equipment manufacturer should design so that initially and throughout life no absolute-maximum value for the intended service is exceeded with any device under the worst probable operating conditions with respect to supply-voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in device characteristics.

It is recommended that equipment manufacturers consult RCA whenever device applications involve unusual electrical, mechanical or environmental operating conditions.

## GENERAL CONSIDERATIONS

The design flexibility provided by these devices makes possible their use in a broad range of applications and under many different operating conditions. When incorporating these devices in equipment, therefore, designers should anticipate the rare possibility of device failure and make certain that no safety hazard would result from such an occurrence.

The small size of most solid state products provides obvious advantages to the designers of electronic equipment. However, it should be recognized that these compact devices usually provide only relatively small insulation area between adjacent leads and the metal envelope. When these devices are used in moist or contaminated atmospheres, therefore, supplemental protection must be provided to prevent the development of electrical conductive paths across the relatively small insulating surfaces. For specific information on voltage creepage, the user should consult references such as the JEDEC Standard No. 7 "Suggested Standard on Thyristors," and JEDEC Standard RS282 "Standards for Silicon Rectifier Diodes and Stacks".

The metal shells of some solid state devices operate at the collector voltage and for some rectifiers and thyristors at the anode voltage. Therefore, consideration should be given to the possibility of shock hazard if the shells are to operate at voltages appreciably above or below ground potential. In general, in any application in which devices are operated at voltages which may be dangerous to personnel, suitable precautionary measures should be taken to prevent direct contact with these devices.

Devices should not be connected into or disconnected from circuits with the power on because high transient voltages may cause permanent damage to the devices.

## TESTING PRECAUTIONS

In common with many electronic components, solid-state devices should be operated and tested in circuits which have reasonable values of current limiting resistance, or other forms of effective current overload protection. Failure to observe these precautions can cause excessive internal heating of the device resulting in destruction and/or possible shattering of the enclosure.

### TRANSISTORS AND THYRISTORS WITH FLEXIBLE LEADS

Flexible leads are usually soldered to the circuit elements. It is desirable in all soldering operatings to provide some slack or an expansion elbow in each lead to prevent excessive tension on the leads. It is important during the soldering operation to avoid excessive heat in order to prevent possible damage to the devices. Some of the heat can be absorbed if the flexible lead of the device is grasped between the case and the soldering point with a pair of pliers.

### TRANSISTORS AND THYRISTORS WITH MOUNTING FLANGES

The mounting flanges of JEDEC-type packages such as the TO-3 or TO-66 often serve as the collector or anode terminal. In such cases, it is essential that the mounting flange be securely fastened to the heat sink, which may be the equipment chassis. Under no circumstances, however, should the mounting flange of a transistor be soldered directly to the heat sink or chassis because the heat of the soldering operation could permanently damage the device. Soldering is the preferred method for mounting thyristors; see "Rectifiers and Thyristors," below. Devices which cannot be soldered can be installed in commercially available sockets. Electrical connections may also be made by soldering directly to the terminal pins. Such connections may be soldered to the pins close to the pin seals provided care is taken to conduct excessive heat away from the seals; otherwise the heat of the soldering operation could crack the pin seals and damage the device.

During operation, the mounting-flange temperature is higher than the ambient temperature by an amount which depends on the heat sink used. The heat sink must have sufficient thermal capacity to assure that the heat dissipated in the heat sink itself does not raise the device mounting-flange temperature above the rated value. The heat sink or chassis may be connected to either the positive or negative supply.

In many applications the chassis is connected to the voltage-supply terminal. If the recommended mounting hardware shown in the data bulletin for the specific solid-state device is not available, it is necessary to use either an anodized aluminum insulator having high thermal conductivity or a mica insulator between the mounting-flange and the chassis. If an insulating aluminum washer is required, it should be drilled or punched to provide the two mounting holes for the terminal pins. The burrs should then be removed from the washer and the washer anodized. To insure that the anodized insulating layer is not destroyed during mounting, it is necessary to remove the burrs from the holes in the chassis.

It is also important that an insulating bushing, such as glass-filled nylon, be used between each mounting bolt and the chassis to prevent a short circuit. However, the insulating bushing should not exhibit shrinkage or softening under the operating temperatures encountered. Otherwise the thermal resistance at the interface between device and heat sink may increase as a result of decreasing pressure.

### PLASTIC POWER TRANSISTORS AND THYRISTORS

RCA power transistors and thyristors (SCR's and triacs) in molded-silicone-plastic packages are available in a wide range of power-dissipation ratings and a variety of package configurations. The following paragraphs provide guidelines for handling and mounting of these plastic-package devices, recommend forming of leads to meet specific mounting requirements, and describe various mounting arrangements, thermal considerations, and cleaning methods. This information is intended to augment the data on electrical characteristics, safe operating area, and performance capabilities in the technical bulletin for each type of plastic-package transistor or thyristor.

#### Lead-Forming Techniques

The leads of the RCA VERSAWATT in-line plastic packages can be formed to a custom shape, provided they are not indiscriminately twisted or bent. Although these leads can be formed, they are not flexible in the general sense, nor are they sufficiently rigid for unrestrained wire wrapping

Before an attempt is made to form the leads of an in-line package to meet the requirements of a specific application, the desired lead configuration should be determined, and a lead-bending fixture should be designed and constructed. The use of a properly designed fixture for this operation eliminates the need for repeated lead bending. When the use of a special bending fixture is not practical, a pair of long-nosed pliers may be used. The pliers should hold the lead firmly between the bending point and the case, but should not touch the case.

When the leads of an in-line plastic package are to be formed, whether by use of long-nosed pliers or a special bending fixture, the following precautions must be observed to avoid internal damage to the device:

1. Restrain the lead between the bending point and the plastic case to prevent relative movement between the lead and the case.
2. When the bend is made in the plane of the lead (spreading), bend only the narrow part of the lead.
3. When the bend is made in the plane perpendicular to that of the leads, make the bend at least 1/8 inch from the plastic case.
4. Do not use a lead-bend radius of less than 1/16 inch.
5. Avoid repeated bending of leads.

The leads of the TO-220AB VERSAWATT in-line package are not designed to withstand excessive axial pull. Force in this direction greater than 4 pounds may result in permanent damage to the device. If the mounting arrangement tends to impose axial stress on the leads, some method of strain relief should be devised.

Wire wrapping of the leads is permissible, provided that the lead is restrained between the plastic case and the point of the wrapping. Soldering to the leads is also allowed. The maximum soldering temperature, however, must not exceed 275°C and must be applied for not more than 5 seconds at a distance not less than 1/8 inch from the plastic case. When

wires are used for connections, care should be exercised to assure that movement of the wire does not cause movement of the lead at the lead-to-plastic junctions.

The leads of RCA molded-plastic high-power packages are not designed to be reshaped. However, simple bending of the leads is permitted to change them from a standard vertical to a standard horizontal configuration, or conversely. Bending of the leads in this manner is restricted to three 90-degree bends; repeated bendings should be avoided.

**Mounting**

Recommended mounting arrangements and suggested hardward for the VERSAWATT package are given in the data bulletins for specific devices and in RCA Application Note AN-4142. When the package is fastened to a heat sink, a rectangular washer (RCA Part No. NR231A) is recommended to minimize distortion of the mounting flange. Excessive distortion of the flange could cause damage to the package. The washer is particularly important when the size of the mounting hole exceeds 0.140 inch (6-32 clearance). Larger holes are needed to accommodate insulating bushings; however, the holes should not be larger than necessary to provide hardware clearance and, in any case, should not exceed a diameter of 0.250 inch.

Flange distortion is also possible if excessive torque is used during mounting. A maximum torque of 8 inch-pounds is specified. Care should be exercised to assure that the tool used to drive the mounting screw never comes in contact with the plastic body during the driving operation. Such contact can result in damage to the plastic body and internal device connections. An excellent method of avoiding this problem is to use a spacer or combination spacer-isolating bushing which raises the screw head or nut above the top surface of the plastic body. The material used for such a spacer or spacer-isolating bushing should, of course, be carefully selected to avoid "cold flow" and consequent reduction in mounting force. Suggested materials for these bushings are diallphtalate, fiberglass-filled nylon, or fiberglass-filled polycarbonate. Unfilled nylon should be avoided.

Modification of the flange can also result in flange distortion and should not be attempted. The package should not be soldered to the heat sink by use of lead-tin solder because the heat required with this type of solder will cause the junction temperature of the device to become excessively high.

The TO-220AA plastic package can be mounted in commercially available TO-66 sockets, such as UID Electronics Corp. Socket· No. PTS-4 or equivalent. For testing purposes, the TO-220AB in-line package can be mounted in a Jetron Socket No. DC74-104 or equivalent. Regardless of the mounting method, the following precautions should be taken:

1. Use appropriate hardware.
2. Always fasten the package to the heat sink before the leads are soldered to fixed terminals.
3. Never allow the mounting tool to come in contact with the plastic case.
4. Never exceed a torque of 8 inch-pounds.
5. Avoid oversize mounting holes.
6. Provide strain relief if there is any probability that axial stress will be applied to the leads.
7. Use insulating bushings to prevent hot-creep problems. Such bushings should be made of diallphthalate, fiberglass-filled nylon, or fiberglass-filled polycarbonate.

The maximum allowable power dissipation in a solid state device is limited by the junction temperature. An important factor in assuring that the junction temperature remains below the specified maximum value is the ability of the associated thermal circuit to conduct heat away from the device.

When a solid state device is operated in free air, without a heat sink, the steady-state thermal circuit is defined by the junction-to-free-air thermal resistance given in the published data for the device. Thermal considerations require that a free flow of air around the device is always present and that the power dissipation be maintained below the level which would cause the junction temperature to rise above the maximum rating. However, when the device is mounted on a heat sink, care must be taken to assure that all portions of the thermal circuit are considered.

To assure efficient heat transfer from case to heat sink when mounting RCA molded-plastic solid state power devices, the following special precautions should be observed:

1. Mounting torque should be between 4 and 8 inch-pounds.
2. The mounting holes should be kept as small as possible.
3. Holes should be drilled or punched clean with no burrs or ridges, and chamfered to a maximum radius of 0.010 inch.
4. The mounting surface should be flat within 0.002 inch/inch.
5. Thermal grease (Dow Corning 340 or equivalent) should always be used on both sides of the insulating washer if one is employed.
6. Thin insulating washers should be used. (Thickness of factory-supplied mica washers range from 2 to 4 mils).
7. A lock washer or torque washer, made of material having sufficient creep strength, should be used to prevent degradation of heat sink efficiency during life.

A wide variety of solvents is available for degreasing and flux removal. The usual practice is to submerge components in a solvent bath for a specified time. However, from a reliability stand point it is extremely important that the solvent, together with other chemicals in the solder-cleaning system (such as flux and solder covers), do not adversely affect the life of the component. This consideration applies to all non-hermetic and molded-plastic components.

It is, of course, impractical to evaluate the effect on long-term device life of all cleaning solvents, which are marketed with numerous additives under a variety of brand names. These solvents can, however, be classified with

respect to their component parts as either acceptable or unacceptable. Chlorinated solvents tend to dissolve the outer package and, therefore, make operation in a humid atmosphere unreliable. Gasoline and other hydrocarbons cause the inner encapsulant to swell and damage the transistor. Alcohol is an acceptable solvent. Examples of specific, acceptable alchols are isopropanol, methanol, and special denatured alcohols, such as SDA1, SDA30, SDA34, and SDA44.

Care must also be used in the selection of fluxes for lead soldering. Rosin or activated rosin fluxes are recommended, while organic or acid fluxes are not. Examples of acceptable fluxes are:

1. Alpha Reliaros No. 320-33
2. Alpha Reliaros No. 346
3. Alpha Reliaros No. 711
4. Alpha Reliafoam No. 807
5. Alpha Reliafoam No. 809
6. Alpha Reliafoam No. 811-13
7. Alpha Reliafoam No. 815-35
8. Kester No. 44

If the completed assembly is to be encapsulated, the effect on the molded-plastic transistor must be studied from both a chemical and a physical standpoint.

## RECTIFIERS AND THYRISTORS

A surge-limiting impedance should always be used in series with silicon rectifiers and thyristors. The impedance value must be sufficient to limit the surge current to the value specified under the maximum ratings. This impedance may be provided by the power transformer winding, or by an external resistor or choke.

A very efficient method for mounting thyristors utilizing the "modified TO-5" package is to provide intimate contact between the heat sink and at least one half of the base of the device opposite the leads. This package can be mounted to the heat sink mechanically with glue or an expoxy adhesive, or by soldering, the most efficient method.

The use of a "self-jigging" arrangement and a solder preform is recommended. If each unit is soldered individually, the heat source should be held on the heat sink and the solder on the unit. Heat should be applied only long enough to permit solder to flow freely. For more detailed thyristor mounting considerations, refer to Application Note AN3822, "Thermal Considerations in Mounting of RCA Thyristors".

## MOS FIELD-EFFECT TRANSISTORS

Insulated-Gate Metal Oxide-Semiconductor Field-Effect Transistors (MOS FETs), like bipolar high-frequency transistors, are susceptible to gate insulation damage by the electrostatic discharge of energy through the devices. Electrostatic discharges can occur in an MOS FET if a type with an unprotected gate is picked up and the static charge, built in the handler's body capacitance, is discharged through the device. With proper handling and applications procedures, however, MOS transistors are currently being extensively used in production by numerous equipment manufacturers in military, industrial, and consumer applications, with virtually no problems of damage due to electrostatic discharge.

In some MOS FETs, diodes are electrically connected between each insulated gate and the transistor's source. These diodes offer protection against static discharge and in-circuit transients without the need for external shorting mechanisms. MOS FETs which do not include gate-protection diodes can be handled safely if the following basic precautions are taken:

1. Prior to assembly into a circuit, all leads should be kept shorted together either by the use of metal shorting springs attached to the device by the vendor, or by the insertion into conductive material such as "ECCOSORB* LD26" or equivalent.
   (NOTE: Polystyrene *insulating* "SNOW" is not sufficiently conductive and should not be used.)
2. When devices are removed by hand from their carriers, the hand being used should be grounded by any suitable means, for example, with a metallic wristband.
3. Tips of soldering irons should be grounded.
4. Devices should never be inserted into or removed from circuits with power on.

## RF POWER TRANSISTORS

### Mounting and Handling

Stripline rf devices should be mounted so that the leads are not bent or pulled away from the stud (heat sink) side of the device. When leads are formed, they should be supported to avoid transmitting the bending or cutting stress to the ceramic portion of the device. Excessive stresses may destroy the hermeticity of the package without displaying visible damage.

Devices employing silver leads are susceptible to tarnishing; these parts should not be removed from the original tarnish-preventive containers and wrappings until ready for use. Lead solderability is retarded by the presence of silver tarnish; the tarnish can be removed with a silver cleaning solution, such as thiourea.

The ceramic bodies of many rf devices contain beryllium oxide as a major ingredient. These portions of the transistors should not be crushed, ground, or abraded in any way because the dust created could be hazardous if inhaled.

### Operating

**Forward-Biased Operation.** For Class A or AB operation, the allowable quiescent bias point is determined by reference to the infrared safe-area curve in the appropriate data bulletin. This curve depicts the safe current/voltage combinations for extended continuous operation.

**Load VSWR.** Excessive collector load or tuning mismatch can cause device destruction by over-dissipation or secondary breakdown. Mismatch capability is generally included on the data bulletins for the more recent rf transistors.

See RCA RF Power Transitor Manual, Technical Series RMF-430, pp 39-41, for additional information concerning the handling and mounting of rf power transistors.

*Trade Mark: Emerson and Cumming, Inc.

## INTEGRATED CIRCUITS

### Handing

All COS/MOS gate inputs have a resistor/diode gate protection network. All transmission gate inputs and all outputs have diode protection provided by inherent p-n junction diodes. These diode networks at input and output interfaces protect COS/MOS devices from gate-oxide failure in handling environments where static discharge is not excessive. In low-temperature, low-humidity environments, improper handling may result in device damage. See ICAN-6000, "Handling and Operating Considerations for MOS Integrated Circuits", for proper handling procedures.

### Mounting

Integrated circuits are normally supplied with lead-tin plated leads to facilitate soldering into circuit boards. In those relatively few applications requiring welding of the device leads, rather than soldering, the devices may be obtained with gold or nickel plated Kovar leads.* It should be recognized that this type of plating will not provide complete protection against lead corrosion in the presence of high humidity and mechanical stress. The aluminum-foil-lined cardboard "sandwich pack" employed for static protection of the flat-pack also provides some additional protection against lead corrosion, and it is recommended that the devices be stored in this package until used.

When integrated circuits are welded onto printed circuit boards or equipment, the presence of moisture between the closely spaced terminals can result in conductive paths that may impair device performance in high-impedance applications. It is therefore recommended that conformal coatings or potting be provided as an added measure of protection against moisture penetration.

In any method of mounting integrated circuits which involves bending or forming of the device leads, it is extremely important that the lead be supported and clamped between the bend and the package seal, and that bending be done with care to avoid damage to lead plating. In no case should the radius of the bend be less than the diameter of the lead, or in the case of rectangular leads, such as those used in RCA 14-lead and 16-lead flat-packages, less than the lead thickness. It is also extremely important that the ends of the bent leads be straight to assure proper insertion through the holes in the printed-circuit board.

### Operating

#### Unused Inputs

All unused input leads must be connected to either $V_{SS}$ or $V_{DD}$, whichever is appropriate for the logic circuit involved. A floating input on a high-current type, such as the CD4049 or CD4050, not only can result in faulty logic operation, but can cause the maximum power dissipation of 200 milliwatts to be exceeded and may result in damage to the device. Inputs to these types, which are mounted on printed-circuit boards that may temporarily become unterminated, should have a pull-up resistor to $V_{SS}$ or $V_{DD}$. A useful range of values for such resistors is from 10 kilohms to 1 megohm.

#### Input Signals

Signals shall not be applied to the inputs while the device power supply is off unless the input current is limited to a steady state value of less than 10 milliamperes. Input currents of less than 10 milliamperes prevent device damage; however, proper operation may be impaired as a result of current flow through structural diode junctions.

#### Output Short Circuits

Shorting of outputs to $V_{SS}$ or $V_{DD}$ can damage many of the higher-output-current COS/MOS types, such as the CD4007, CD4041, CD4049, and CD4050. In general, these types can all be safely shorted for supplies up to 5 volts, but will be damaged (depending on type) at higher power-supply voltages. For cases in which a short-circuit load, such as the base of a p-n-p or an n-p-n bipolar transistor, is directly driven, the device output characteristics given in the published data should be consulted to determine the requirements for a safe operation below 200 milliwatts.

For detailed COS/MOS IC operating and handling considerations, refer to Application Note ICAN-6000 "Handling and Operating Considerations for MOS Integrated Circuits".

## SOLID STATE CHIPS

Solid state chips, unlike packaged devices, are non-hermetic devices, normally fragile and small in physical size, and therefore, require special handling considerations as follows:

1. Chips must be stored under proper conditions to insure that they are not subjected to a moist and/or contaminated atmosphere that could alter their electrical, physical, or mechanical characteristics. After the shipping container is opened, the chip must be stored under the following conditions:
   A. Storage temperature, 40°C max.
   B. Relative humidity, 50% max.
   C. Clean, dust-free environment.
2. The user must exercise proper care when handling chips to prevent even the slightest physical damage to the chip.
3. During mounting and lead bonding of chips the user must use proper assembly techniques to obtain proper electrical, thermal, and mechanical performance.
4. After the chip has been mounted and bonded, any necessary procedure must be followed by the user to insure that these non-hermetic chips are not subjected to moist or contaminated atmosphere which might cause the development of electrical conductive paths across the relatively small insulating surfaces. In addition, proper consideration must be given to the protection of these devices from other harmful environments which could conceivably adversely affect their proper performance.

*Mil-M-38510A, paragraph 3.5.6.1 (a), lead material.

# Application Considerations for the RCA 3N128 VHF MOS Field-Effect Transistor

by

F. M. Carlson

Early MOS field-effect transistors were intended primarily for low-frequency applications in which their extremely high input impedance is advantageous, and were not designed to be useful in the vhf range (30 to 300 MHz). Recently, however, RCA has developed high-frequency MOS transistors that exhibit high gain and low noise at vhf, together with very low feedback capacitance and cross-modulation distortion that approaches the low levels of electron tubes. The low level of cross-modulation distortion is a particularly important characteristic in view of the increasing congestion of the communications frequency bands.

This note describes applications and vhf circuit considerations for a new high-frequency n-channel MOS field-effect transistor, the RCA 3N128. Biasing requirements and basic circuit configurations are discussed, and selection of the optimum operating point and methods of automatic gain control are explained. The cross-modulation and intermodulation distortion characteristics of the 3N128 MOS transistor are compared to those of bipolar transistors, and procedures are given for the design of a practical vhf amplifier that uses the 3N128.

### Biasing Requirements and Circuit Configurations

The biasing requirements and operating characteristics of an n-channel MOS transistor such as the 3N128 are similar to those of an electron tube. For example, the 3N128 uses positive drain voltages and usually negative gate voltages which are analogous to the plate and grid voltages, respectively, of electron tubes. In addition, the current-voltage characteristics of the 3N128, shown in Fig. 1, are similar to those of a pentode tube. An electron-tube analogy, therefore, can be useful in the analysis of the n-channel 3N128 MOS transistor.[†]

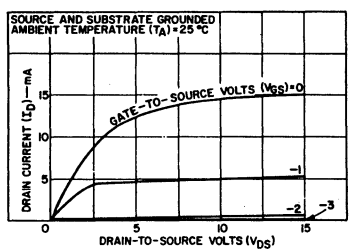



*Fig. 1 - Transfer characteristics for the RCA 3N128 vhf MOS transistor.*

Although their characteristics are similar, MOS transistors have several important advantages over electron tubes. They can be operated at the low voltages typical of bipolar transistors. The dc gate current of MOS transistors is substantially less than the

[†] The electron-tube analogy does not apply to p-channel MOS transistors or to enhancement types.

grid current of most electron tubes. In addition, the MOS transistor requires no heat-generating filament.

MOS transistors are most often used in the common-source type of circuit configuration. Fig.2 shows three basic methods of dc-biasing an MOS transistor in a common-source circuit. MOS transistors may also be used in common-gate or common-drain (source-follower) configurations.[2] These circuits are not widely used in vhf applications, however, because their gain is low at high frequencies.

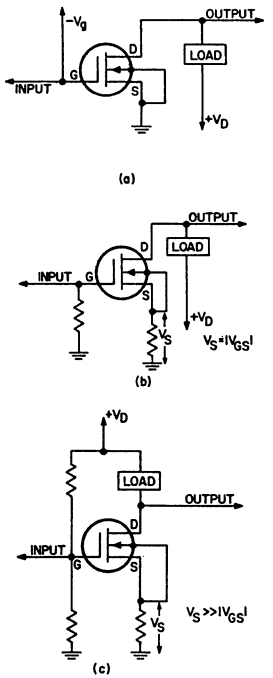
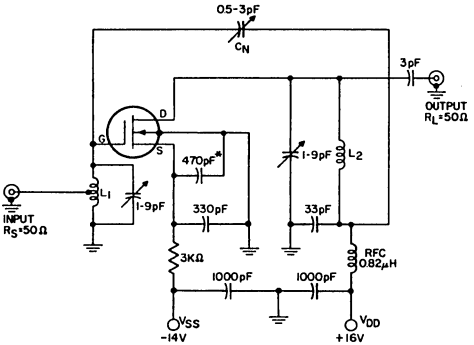



*Fig.2 - Bias methods for common-source MOS transistor stages: (a) fixed bias; (b) source-resistor bias; (c) constant-current bias.*

Fig.3 shows a 200-MHz common-source amplifier used to measure the rf power gain of the MOS transistor. This amplifier uses a modified form of the constant-current biasing arrangement shown in Fig.2(c). With this modified biasing arrangement, both the insulated gate and the case of the MOS transistor are operated at dc ground potential. The insulated gate should always have a dc path to ground even if the path is through a multimegohm resistor. If the gate is allowed to float, the resultant dc bias conditions may be unpredictable and possibly harmful.




L1 = 4-1/2 turns of No.20 wire, 3/16 inch in dia., 1/2 inch long, tapped at 1 turn

L2 = 3-1/2 turns of No.20 wire, 3/8 inch in dia., 1/2 inch long

* Leadless disc capacitor

*Fig.3 - 200-MHz common-source amplifier.*

Fig.4 illustrates the effect of the leakage resistances $R_{L1}$ and $R_{L2}$ when the insulated gate is floating. When these resistances ($\approx 10^{14}$ ohms) are approximately equal, they form a voltage divider which biases the insulated gate at $+V_{DD}/2$. This value of bias voltage may exceed the maximum rating for positive gate voltage and, in addition, may cause an excessive flow of drain current.

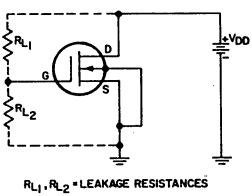



*Fig.4 - Bias conditions for an MOS transistor when the insulated gate is floating.*

The cascode configuration represents a useful variation of common-source circuit. In this configuration, a common-source-connected MOS transistor is used in the lower section of the cascode, and a common-gate-connected MOS transistor is used in the upper section. Fig.5 shows the use of MOS transistors in a 200-MHz cascode amplifier. This circuit normally requires a negative voltage on the gate of $Q_1$, a positive voltage on the gate of $Q_2$, and approximately equal drain-to-source voltages for each transistor. Although the gate of $Q_2$ may require a positive voltage of 5 to 10 volts, the net gate-to-source voltage for this transistor should be approximately 0 to -1 volt.

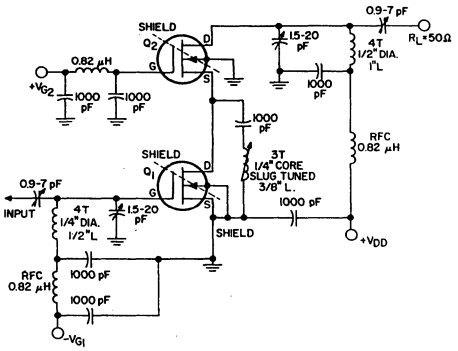



*Fig.5 - 200-MHz cascode amplifier.*

**Selection of Operating Point**

The operating point selected determines the power gain, noise figure, power dissipation, and, where applicable, battery life. In many applications, a compromise between gain and available supply voltages or battery lifetime is necessary. Knowledge of the variation in gain and noise figure as functions of voltage and current is essential, therefore, before an operating point can be selected.

The 3N128 provides maximum rf power gain at a drain-to-source voltage $V_{DS}$ of approximately 20 volts and a drain current $I_D$ of about 5 milliamperes. The transistor also exhibits a minimum noise figure at a $V_{DS}$ of 20 volts for a drain current of about 2 milliamperes. The difference in the noise figures obtained at 2 milliamperes and at 5 milliamperes, however, is very small (usually between 0 and 0.2 dB) and generally is not a significant factor in the selection of the operating point. Although a $V_{DS}$ of 20 volts represents the optimum value for the 3N128 in terms of both rf power gain and noise figure, this value is also the maximum $V_{DS}$ rating for the transistor. Greater long-term reliability is achieved, therefore, by operation of the 3N128 at a $V_{DS}$ of 12 to 15 volts rather than at 20 volts.

For a $V_{DS}$ of 15 volts and an $I_D$ of 5 milliamperes, the 3N128 typically provides a power gain of 18 dB and a noise figure of 4 dB at 200 MHz. Operation of the 3N128 at considerably lower drain currents, such as those normally employed in battery-powered equipment, does not seriously affect system performance. For example, when the transistor is operated at a $V_{DS}$ of 15 volts and an $I_D$ of only 1 milliampere, the power gain and noise figure at 200 MHz are typically 15.5 dB and 4.5 dB, respectively. Because the MOS transistor is a voltage-controlled device, its performance for a given power dissipation can often be improved by operation at high voltage and low current levels. At a power dissipation of 30 milliwatts, for example, the 3N128 typically provides a power gain of 17.3 dB and a noise figure of 3.9 dB when operated at 15 volts and 2 milliamperes. At the same dissipation level, however, the power gain is reduced to 14.6 dB and the noise figure is increased to 4.7 dB when the 3N128 is operated at 6 volts and 5 milliamperes. Fig.6 shows the variations in power gain and noise figure of the 3N128 as functions of the drain current and voltage.

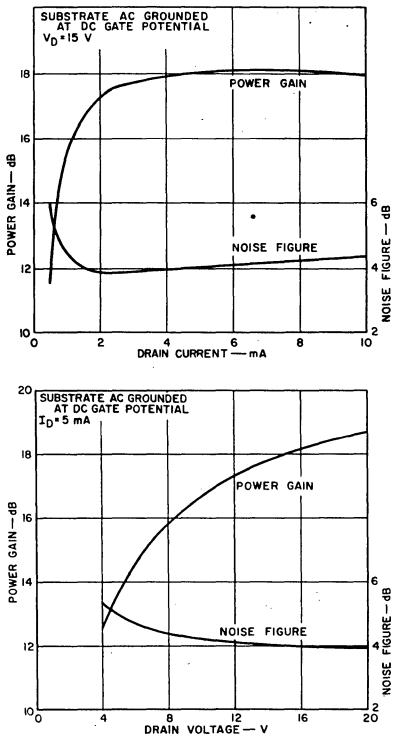



*Fig.6 - Power gain and noise figure of the RCA 3N128 at 200 MHz as functions of drain current and voltage.*

A gate voltage $V_G$ of between -0.5 and -2 volts is normally required to bias a 3N128 for operation at a drain voltage $V_D$ of 15 volts and a drain current $I_D$ of 5 milliamperes. If a fixed-bias circuit, as shown in Fig.2(a), is used, the value of the gate voltage must be adjustable to compensate for variations among individual transistors. For the source-resistance bias circuit shown in Fig.2(b) the value of the biasing resistor should be 200 ohms (5 mA x 200 ohms = 1 volt). The source-resistance circuit will limit the variations in current among the different transistors to approximately

50 per cent. With the constant-current bias circuit shown in Fig.2(c), variations in current from one transistor to another can easily be limited to less than 10 per cent. Regardless of the bias circuit or the bias point selected, there is no danger of thermal runaway with the 3N128 because this transistor has a negative temperature coefficient at the zero-gate-bias point. In the selection of the bias circuit for an MOS transistor stage in which automatic gain control is employed, consideration should be given to the following principle: The more restrictive the tolerance imposed on quiescent operating-point current, the more difficult automatic gain control of the stage becomes because the self-compensating action of the constant-current bias circuit also resists current changes that result from the agc action.

### AGC Methods

When it is necessary to employ agc in an MOS transistor stage, either of two methods may be used to reduce transistor gain. In one method, referred to as reverse agc, the reduction in gain is accomplished by an increase in negative gate bias. In the other method, the gain is decreased by reduction of the drain-to-source voltage.

In the reverse agc method, the application of higher negative voltage to the gate reduces the drain current and the transconductance of the transistor. The low feedthrough capacitance of the 3N128 (typically about 0.13 picofarad) usually permits more than 30 dB of gain reduction at frequencies up to 200 MHz. Substantially greater gain reduction can be achieved at lower frequencies or in neutralized amplifier circuits.

Gain reduction achieved by the decrease of drain-to-source voltage is usually controlled by a variable impedance in series, or in shunt, with the MOS transistor. The variable impedance may be another MOS transistor or a bipolar transistor. A major disadvantage of this method is that the MOS feedback capacitance rises by a factor of 4 or 6 times as $V_D$ approaches zero. This increase in capacitance reduces the agc range obtainable and decreases the effectiveness of a fixed neutralization network. In addition, the output impedance of the 3N128 decreases with a reduction in the drain voltage.

In the cascode circuit, agc is accomplished most effectively by application of a negative voltage to the gate of the upper (common-gate) section. A wide agc range can be obtained in this circuit. Gain reductions greater than 45 dB at 200 MHz or 65 dB at 60 MHz are realizable in an unneutralized cascode circuit.

### RF Considerations

One of the prime advantages of the 3N128 MOS transistor over bipolar transistors is its superior cross-modulation, intermodulation, and modulation distortion performance. The 3N128 has considerably lower feedback capacitance than junction-gate field-effect transistors. In addition, the 3N128 maintains a high input resistance at frequencies well into the vhf range (the real part of the input admittance, $Re(y_{11}) = 0.15$ mmho at 100 MHz).

At maximum gain, the cross-modulation distortion of the 3N128 is approximately one-tenth that of most bipolar transistors, or roughly comparable to the cross-modulation performance of vacuum tubes (at 200 MHz, an interfering signal of approximately 80 millivolts is required to produce cross-modulation distortion of 1 per cent). However, cross-modulation susceptibility changes as the gain of the stage is changed. For a single 3N128, the cross-modulation distortion increases when reverse agc is applied; the distortion is also increased, but to a lesser extent, if agc action is achieved by reduction of the drain-to-source voltage. A deterioration in cross-modulation performance at high attenuation results from the fact that the MOS triode is a sharp-cutoff device; as a result, large non-linearities occur near "pinch-off." Beyond "pinch-off," the transadmittance depends primarily upon the capacitive feedthrough, which does not have large third-order non-linearities. Cross-modulation performance at the extreme limits of attenuation, therefore, is very good.[1] In cascode stages, the effect of reverse agc on cross-modulation distortion is reduced when the agc is applied to the gate of the common-gate stage; application of reverse bias to the gate of the common-source stage results in cross-modulation performance similar to that of a single triode-connected stage. Figs.7 and 8 show the variation in cross-modulation susceptibility as a function of agc. The test circuits used to measure cross-modulation distortion of MOS transistors are shown in Fig.9.

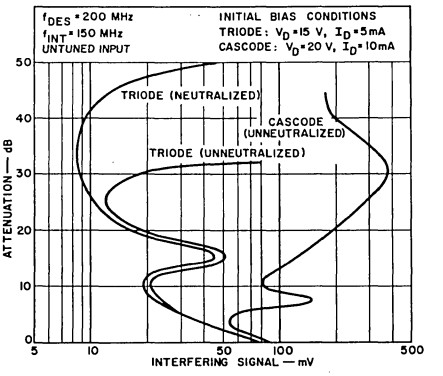



*Fig.7 - Cross-modulation distortion as a function of the attenuation produced by reverse agc.*

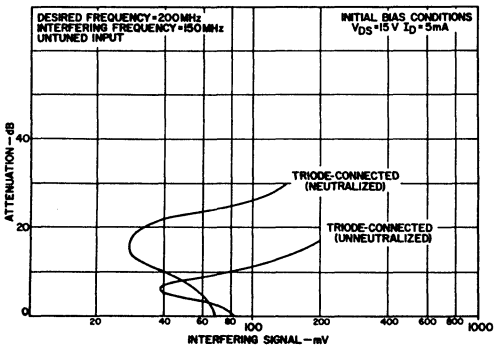



*Fig.8 - Cross-modulation distortion as a function of the attenuation produced when agc is accomplished by a reduction of drain-to-source voltage.*

The test circuit shown in Fig.10 is used to measure the intermodulation distortion of MOS transistors. In such measurements, the receiver is tuned to 150 MHz. The MOS is then inserted, and bias voltages are applied. When no signals are applied (i.e., the amplitudes of the signals $f_1$ and $f_2$ are both 0 volts), the rf indicator of the receiver indicates an equivalent input noise level of approximately 2.4 microvolts. The signals $f_1$ and $f_2$ are gradually increased in amplitude until the reading on the rf indicator is 1 microvolt above the noise level (3.4 microvolts total). This reading indicates that 2.4 microvolts of 150-MHz signal is being produced by the interaction of $f_1$ and $f_2$ (i.e., $2f_1 - f_2 = 150$ MHz). Table I lists the dc bias levels used for the 3N128 MOS transistor and the amplitude of the $f_1$ and $f_2$ signals required to produce an output, at 150 MHz, of 2.4 microvolts, which corresponds to 1 microvolt above the input noise level. The amplitudes of $f_1$ and $f_2$ were measured by an rf vacuum-tube voltmeter; the $f_1$ generator was turned down for measurement of $f_2$, and vice versa.

**Table I**

**INTERMODULATION DISTORTION DATA FOR THE 3N128 MOS TRANSISTOR**

| | | Interfering Voltages Required to Produce 2.4 microvolts at 150 MHz | |
|---|---|---|---|
| $V_D$ volts | $I_D$ mA | $f_1$ (175 MHz) mV | $f_2$ (200 MHz) mV |
| 16.5 | 10 | 18 | 18 |
| 16.5 | 10 | 7 | 150 |
| 16.5 | 5 | 15 | 15 |
| 16.5 | 5 | 3.5 | 150 |
| 16.5 | 5 | 30 | 3.5 |
| 16.5 | 2.5 | 19 | 21 |

When the same test methods were used to measure the intermodulation distortion of bipolar transistors, distortion levels were found to be two to five times greater than those of the 3N128 MOS transistor.

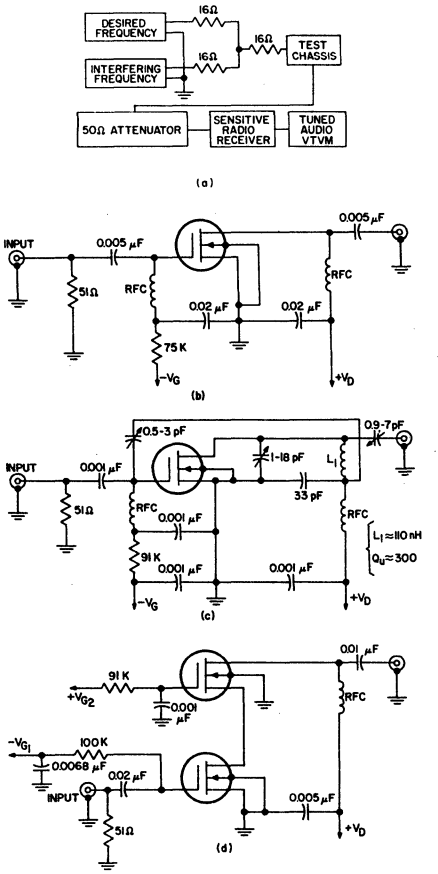



*Fig.9 - Test circuits used to measure cross-modulation distortion in MOS transistors: (a) block diagram; (b) unneutralized-stage test circuit; (c) neutralized-stage test circuit; (d) cascode-stage test circuit.*

### Designing VHF MOS Amplifier Circuits

A complete set of graphs of typical y parameters, both as a function of frequency at constant bias and as as a function of bias at constant frequency, are given in the published data for the 3N128 MOS transistor. The application of these y parameters in the design of the 200-MHz amplifier shown in Fig.3 is discussed in following paragraphs.

For operation at a frequency of 200 MHz, an $I_D$ of

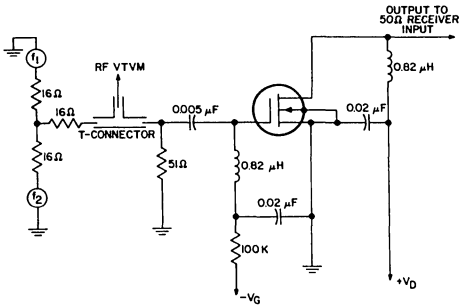



*Fig. 10 - Test circuit used to measure intermodulation distortion in MOS transistors.*

5 milliamperes, and a $V_D$ of 15 volts, the y parameters of the 3N128 are typically as follows:

$y_{11}$ (input admittance with output short-circuited) = 0.45 + j7.2 mmhos

$y_{22}$ (output admittance with input short-circuited) = 0.28 + j1.75 mmhos

$y_{21}$ (forward transfer admittance with output short-circuited) = 7.0 - j1.9 mmhos

$y_{12}$ (reverse transfer admittance with input short-circuited) = 0 - j0.16 mmhos

If $y_{12}$ is assumed to be zero, the maximum available power gain (MAG) under conjugately matched conditions,* may be computed. MAG serves as a useful figure of merit for comparison of the vhf power gain of various MOS transistors. The MAG for the 3N128 is determined as follows:

$$MAG = \frac{|y_{21}|^2}{4Re(y_{11})Re(y_{22})} = \frac{|7.0-j1.9|^2}{4(0.45)(0.28)} = 104 = 20.2\,dB \quad (1)$$

where Re means "the real part of."

All MOS transistors have a small, but measurable, feedback component ($y_{12}$); it is possible, therefore, that some of them will oscillate under certain circuit conditions. This possibility may be checked by use of methods given by Linvill[2,4] and by Stern.[3,4] If the transistor is unconditionally stable for any combination of passive source and load admittances, then Linvill's critical stability factor C, as determined from the following equation, is less than |1|:

$$C = \frac{|y_{21}y_{12}|}{2Re(y_{11})Re(y_{22}) - Re(y_{21}y_{12})} \quad (2)$$

The critical stability factor for the 3N128 is calculated as follows:

$$C = \frac{|(7.0-j1.9)(0-j0.16)|}{2(0.45)(0.28) - Re(7.0-j1.9)(-j0.16)} = 2.08$$

Stern has derived a similar expression for stability $C_S$ that includes the effect of the generator and load conductances, $y_g$ and $y_L$, respectively, as follows:

$$C_S = \frac{|y_{21}y_{12}|}{2\,Re(y_{11}+y_g)Re(y_{22}+y_L) - Re(y_{21}y_{12})} < |1| \quad (3)$$

If a conjugate match is assumed at both the input and the output, then $Re(y_g) = Re(y_{11})$, and $Re(y_L) = Re(y_{22})$. For this condition, the stability factor is calculated as follows:

$$C_S = \frac{|(7.0-j1.9)(-j0.16)|}{2(0.45+0.45)(0.28+0.28) - Re(7.0-j1.9)(-j0.16)} = \frac{1.16}{1.31} = 0.885$$

These calculations show that the transistor itself is not unconditionally stable, but that it is stable when placed in a conjugately matched circuit. Therefore, neutralization is not required, although it may be used if a more symmetrical pass-band characteristic is desired. All unneutralized amplifiers have a certain amount of skew in the selectivity characteristic; if this skewness becomes objectionable for the required application, then neutralization (or mis-matching) is necessary.

When neutralization is desired, there are two common methods of obtaining the required feedback. The first, and more common method, is the capacitance-bridge technique shown in Fig. 11(a). The capacitance bridge becomes more apparent when the circuit is redrawn as shown in Fig. 11(b). The condition for neutral-

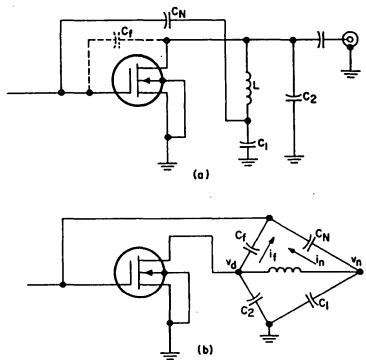



*Fig. 11 - Capacitance-bridge neutralization circuit: (a) actual circuit configuration; (b) circuit redrawn to emphasize capacitance-bridge network.*

* Conjugate match means that the transistor input and the generator and the transistor output and load are matched resistively and that all reactance is tuned out.

ization is that $i_f = i_n$. This condition implies the following relationship:

$$\frac{v_d}{jX_f} = \frac{-v_n}{jX_n}, \text{ or } C_f v_d = -C_n v_n \quad (4)$$

The voltage $v_n$ is defined by the following equation:

$$v_n = \left(\frac{v_d}{jX_L + jX_1}\right) jX_1 = \left(\frac{v_d}{\frac{-\omega^2 LC_1 + 1}{j\omega C_1}}\right) \frac{1}{j\omega C_1} = \frac{v_d}{-\omega^2 LC_1 + 1} \quad (5)$$

If this relationship for $v_n$ is substituted in Eq.(4), the following result is obtained:

$$C_f v_d = -C_n \left(\frac{v_d}{-\omega^2 LC_1 + 1}\right), \text{ or } C_n = -C_f(-\omega^2 LC_1 + 1) \quad (6)$$

At resonance, the equation for the neutralization capacitance $C_n$ may be rewritten as follows:

$$C_n = -C_f\left[\left(\frac{-1}{\omega C_2}\right)\omega C_1 + 1\right] = C_f\left(\frac{C_1}{C_2} - 1\right) \quad (7)$$

If $C_1 >> C_2$, Eq.(7) may be rewritten as follows:

$$C_n \approx C_f\left(\frac{C_1}{C_2}\right) \quad (8)$$

The other common method of neutralization is the transformer-coupled method shown in Fig.12. Again, the condition for neutralization is that $i_f = i_n$. The requirements for this condition are expressed by the following equation:

$$\frac{v_d}{X_f} = \frac{-v_n}{X_n}, \text{ or } C_f v_d = -C_n v_n \quad (9)$$

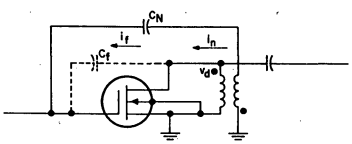



*Fig.12 - Transformer-coupled neutralization circuit.*

Eq.(9) may be rewritten in the following form:

$$\left|\frac{v_d}{v_n}\right| = \frac{C_n}{C_f} \quad (10)$$

The required turns ratio for the coupling transformer can be determined from Eq.(10).

The generator and load impedances must be matched to the transistor input and output impedances, respectively, to obtain maximum gain. For the 200-MHz amplifier shown in Fig.3, the generator resistance at the input is 50 ohms. For a conjugately matched input, the generator admittance $y_g$ and the real part of the transistor input admittance must appear to be equal. Because the generator admittance $y_g$ is 20 mmhos and the real part of the input admittance $Re(y_{11})$ is 0.45 mmho, the coupling transformer must provide a transformation ratio of 44 to obtain the desired impedance match. The turns ratio required is determined as follows:

$$\frac{N_2}{N_1} = \sqrt{44} = 6.6$$

Experimentally, a turns ratio of 4 was found to be approximately the optimum value. This difference results, in part, from the fact that the parallel resistance of the tank coil was not considered in the calculation. At the output of the 200-MHz amplifier, the load is also 50 ohms. Because the dc drain voltage must be blocked from the load, a series matching capacitor was selected which performs both dc blocking and resistive matching simultaneously.

In the actual load-circuit network shown in Fig.13(a), the value of capacitor $C_S$ must be chosen so that the load admittance, $y_L$ = 20 millimhos, is apparently equal to the real part of the transistor output admittance, $Re(y_{22})$ = 0.28 millimhos. Fig.13(b) shows the equivalent circuit of the load-circuit network for this condition.

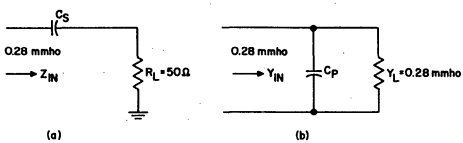



*Fig.13 - Output network in which series coupling capacitance is used for dc-voltage blocking and resistive matching: (a) actual network; (b) electrical equivalent.*

The following equation gives the input impedance $Z_{IN}$ for the network shown in Fig.13:

$$Z_{IN} = R_S + \frac{1}{j\omega C_S} \quad (11)$$

The input admittance $y_{IN}$, therefore, may be expressed as follows:

$$y_{IN} = \frac{1}{R_p} + j\omega C_p = \frac{1}{Z_{IN}} = \frac{1}{R_S + \frac{1}{j\omega C_S}} \quad (12)$$

The terms in Eq.(12) are rearranged to obtain the following result:

$$\frac{R_S}{R_p} + j\omega C_p R_S + \frac{1}{j\omega C_S R_p} + \frac{j\omega C_p}{j\omega C_S} = 1 \quad (13)$$

The real and imaginary terms in Eq.(13) are equated to obtain the following relationships:

$$\frac{R_S}{R_p} + \frac{C_p}{C_S} = 1 \qquad (14)$$

$$\omega C_p R_S - \frac{1}{\omega C_S R_p} = 0 \qquad (15)$$

$$C_p = \frac{1}{(\omega C_S R_p)(\omega R_S)} \qquad (16)$$

Eq.(16) is substituted into Eq.(14) to obtain the following equation for the matching capacitance $C_S$:

$$C_S = \frac{1}{\omega}\sqrt{\frac{1}{(R_p - R_S)R_S}} \qquad (17)$$

Substitution of numerical values for the parameters in Eq.(17) yields the following value for $C_S$:

$$C_S = \frac{1}{2\pi(2 \times 10^8)}\sqrt{\frac{1}{(3600-50)50}} = 1.9 \text{ pF}$$

Experimentally, a 3-picofarad capacitor was found to perform very satisfactorily in the amplifier. If $R_p >> R_S$, then $C_p \approx C_S$. Therefore, a 3-picofarad capacitance appears in parallel with the 1.4-picofarad capacitance of the MOS transistor. A small 1-to-9-picofarad variable air capacitor was selected for the tank tuning capacitor to compensate for variations among transistors. For a nominal value of 2 picofarads for the air capacitor, the total output capacitance is 6.4 picofarads. The inductance required to resonate with 6.4 picofarads at 200 MHz is 0.1 microhenry. When the total output capacitance is known, the required neutralization capacitor can be calculated. If $C_1$ is arbitrarily selected as 33 picofarads, the neutralization is determined from Eq.(8), as follows:

$$C_n \approx C_f\left(\frac{C_1}{C_2}\right) = 0.2\left(\frac{33}{6.4}\right) = 1.0 \text{ pF}$$

The optimum value for the neutralization capacitor was determined experimentally by use of a small (0.5-to-3-picofarad) variable capacitor. This capacitor was adjusted to the optimum value for a typical unit ($C_{rss}$ = 0.13 pF) and then fixed. The required input inductance was found to be 0.06 microhenry. The completed amplifier is shown schematically in Fig.3. The bandwidth of the amplifier is typically 8 MHz and shows negligible skew.

The y parameters may also be used to design a cascode vhf amplifier such as the one shown in Fig.5. This circuit had typical power gain and noise figure of 17 dB and 4.2 dB, respectively. The amplifier has a bandwidth of 10 MHz with negligible skew. The capacitance of the $source_2$-$drain_1$ interconnection must be tuned out to achieve a good vhf noise figure. The noise figure of the cascode amplifier is 2 to 3 dB higher if this capacitance is not tuned out.

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# VHF Mixer Design Using the RCA-3N128 MOS Transistor

by

F. M. Carlson

The 3N128 is a vhf MOS field-effect transistor suitable for use throughout the vhf band (30 to 300 MHz) as an amplifier, mixer, or oscillator. This Note discusses some of the design criteria pertinent to the construction of MOS mixers, and presents an example of a complete vhf MOS converter.

### Mixer Design Considerations

The conversion gain obtained from a mixer is the ratio of intermediate-frequency (if) power output divided by the radio-frequency (rf) power input. This conversion gain CG is usually expressed in dB, as follows:

$$CG = 10 \log \frac{\text{if } P_{out}}{\text{rf } P_{in}}$$

The value of CG approximates the gain of the active device operated as an amplifier (unneutralized) at the intermediate frequency, minus the rf losses at the input of the device. Practical mixers normally have a conversion gain of 3 to 5 dB less than their if-amplifier gain.

The 3N128 transistor has good gain and noise figure throughout the vhf band. Because it also has a nonlinear region of operation, it may be used as a vhf mixer to provide good conversion gain. The transfer function of the 3N128, shown in Fig.1, indicates that the maximum nonlinearities occur at a drain current of about 1.5 milliampere. At drain currents above approximately 5 milliamperes, the transfer function starts to become linear. No mixing action can occur if the transfer function is perfectly linear. Because the amplifier gain of the 3N128 is higher at 5 milliamperes than at 1.5 milliamperes, the best bias point for an MOS mixer is a compromise between the region where best mixing occurs and the region where optimum if power gain occurs. For the 3N128, this point is empirically determined to be between 3.5 and 4.5 milliamperes.

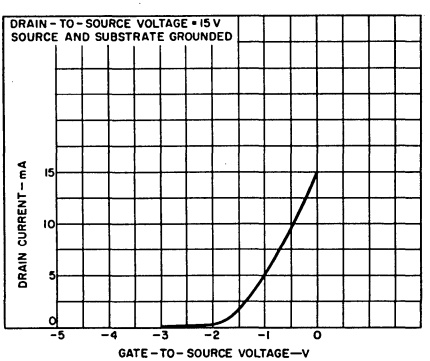


*Fig.1 - Drain current as a function of gate-to-source voltage for the 3N128 vhf MOS transistor.*

The local-oscillator signal may be introduced into a 3N128 mixer at the insulated gate, the source, or the junction gate (substrate). Application of the oscillator signal to the junction gate can be very effective, but is not recommended because the junction gate of the

3N128 is tied to the case; placing the transistor case at local-oscillator signal potential can pose possible radiation problems.

Injection of the oscillator signal at the source is not desirable because the source should always be at rf/if ground for optimum gain, but could not be at ground at the oscillator frequency. Designing a network to meet these criteria is difficult and adds to the cost of the mixer.

Injection of the oscillator signal at the insulated gate is the least troublesome of the three methods. The local oscillator may be coupled to the insulated gate by means of an inductive loop or a small coupling capacitor.

The input circuit is normally designed for a conjugate match with the input impedance of the MOS transistor at the radio frequency. The output circuit is normally designed for a conjugate match with the output impedance of the 3N128 at the intermediate frequency, unless electrical instabilities (oscillations) occur, in which case the output circuit must be mismatched. Oscillations are not normally a problem in a 3N128 mixer, provided the if and rf signals are relatively far apart in frequency. Under these conditions, the output circuit presents a low impedance to the rf signal, and the input circuit presents a low impedance to the if signal; consequently, oscillations at either frequency are unlikely to occur.

Neutralization is not generally used in mixers because of the different frequencies at the output and the input.

**Design Example**

A vhf receiver "front end" has been designed and built to demonstrate the preceding design considerations and to illustrate the use of the 3N128 vhf MOS transistor in all four stages: rf, mixer, if, and local oscillator. The complete converter, shown in Fig.2, uses an rf input frequency of 200 MHz and an if output frequency of 30 MHz.

The input stage is a straight-through 200-MHz amplifier* employing a source resistor for gate bias. This configuration permits the gate to be at dc ground, and greatly reduces the possibility of damage to the MOS gate from input transients. The 240-ohm resistor allows a current of approximately 5 milliamperes to flow through the device so that maximum vhf power gain is obtained. A variable inductor resonates with the output capacitance of the 3N128 to provide a bandwidth of approximately 12 MHz for the rf stage alone. (Narrower bandwidth could have been obtained by use of more capacitance in the tuned circuits and different loading on the output circuit; however, no particular effort was made to achieve very narrow bandwidth because a wide bandwidth is desirable in some applications.) Capacitive bridge neutralization is used to achieve the maximum allowable stage gain of 20 dB for the particular 3N128 used.

The input coil of the mixer stage is designed to permit a conjugate match with the transistor input admittance. The input admittance $y_{11}$ of the 3N128 at 200 MHz is approximately 0.45 + j 7.2 millimhos. Therefore, an admittance of $y_{11}$* (=0.45 - j 7.2 milli-

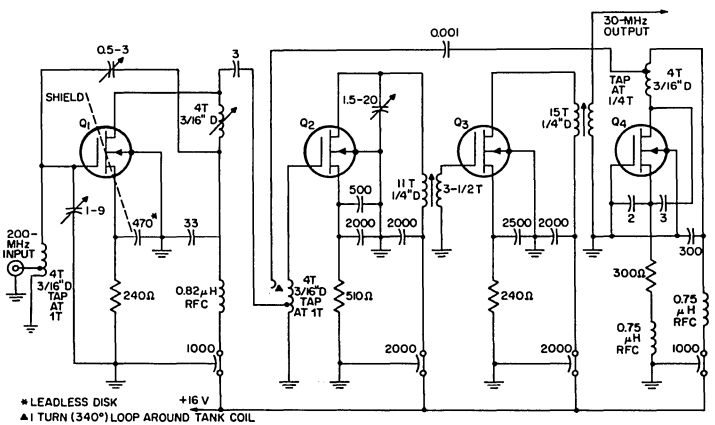


*Fig.2 - VHF receiver "front end" using the 3N128 in all stages.*

* Design information for vhf MOS amplifiers is given in RCA Application Note AN-3193: "Application Considerations for the RCA-3N128 VHF MOS Field-Effect Transistor," by F.M. Carlson, August 1966.

mhos) should be presented to the mixer input. A conjugate match is not used at the output because it is desirable to load the input of the following (if) stage for stability. Therefore, a step-down transformer is used. (A conjugate match would require use of a step-up transformer because $g_{11} > g_{22}$ at 30 MHz.)

The local oscillator is coupled into the insulated gate of the mixer by means of an ungrounded 340-degree loop placed around the input tank coil at its high-impedance end. A small coupling capacitor could also be used for this purpose. Local-oscillator amplitude is approximately 1.4 volts rms into the coupling loop. Power gain of the mixer stage is 16 dB. Fig.3 shows the conversion gain of the mixer as a function of local-oscillator amplitude. A lower oscillator level than 1.1 volts would probably be desirable if spurious output frequencies were found to be troublesome.

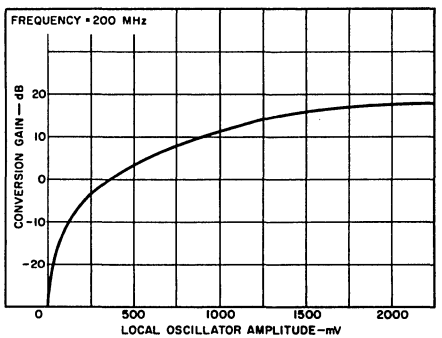


*Fig.3 - Conversion gain of the mixer stage in Fig.2 as a function of local-oscillator amplitude.*

A 510-ohm source resistor is used in the mixer stage to provide a drain current of 4 milliamperes. (This value is larger than would normally be expected for a drain current of this level because the gate is subjected to large signal excursions by the local oscillator.)

The maximum available gain (MAG) of the 3N128 at 30 MHz in a conjugately matched circuit (with $y_{12}$ assumed to be approximately zero) may be computed from the y-parameters for the device, as follows:

$$MAG = \frac{|y21|^2}{4\, g_{11}\, g_{22}} = \frac{|7.2|^2}{4(0.03)(0.12)} = 3610 = 35.6 \text{ dB}$$

The maximum usable gain (MUG) of the 3N128 in an unneutralized 30-MHz amplifier is computed as follows:

$$MUG = \frac{0.4\, g_m}{\omega C_{rss}} = \frac{(0.4)(7.2)(10^{-3})}{(2\pi)(30)\,10^6\,(0.13)\,10^{-12}} = 118 = 20.7 \text{ dB}$$

If the 30-MHz stage is operated at a gain significantly above the MUG value, the possibility of circuit oscillation exists. Therefore, the input of the if stage is mismatched to reduce the stage gain from the MAG level to about 20 dB. (In some cases, it may be easier to mismatch at the output than at the input.) The output of the if stage is transformer-coupled to a 50-ohm load.

The local-oscillator stage is a Colpitts circuit in which frequency is adjusted by means of a slug-tuned inductor.

The complete converter has a power gain of 56 dB, a noise figure of 3 dB, and a bandwidth of 1.5 MHz. Spurious responses (referred to a level of 0 dB at the 200-MHz input frequency) are -51 dB at 100 MHz, -36 dB at 215 MHz, and -35 dB at 260 MHz. These spurious responses could be greatly improved by use of a narrower bandwidth in the rf stage; the present bandwidth is 12 MHz at the 3-dB points.

Table I shows measurements of cross-modulation of the converter as a function of frequency.

| Interfering Frequency (MHz) | Interfering Signal Voltage Necessary for 1% Cross-Modulation (mV) |
|---|---|
| 50 | 160 |
| 90 | 115 |
| 100 | 87 |
| 110 | 98 |
| 120 | 97 |
| 130 | 87 |
| 140 | 78 |
| 150 | 77 |
| 160 | 65 |
| 170 | 52 |
| 180 | 39 |
| 190 | 9 |

*Table I - Cross-modulation of MOS mixer.*

# Chopper Circuits Using RCA MOS Field-Effect Transistors

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Although electromechanical relays have long been used to convert low-level dc signals into ac signals or for multiplex purposes, relays are seriously limited with respect to life, speed, and size. Conventional (bipolar) transistors overcome the inherent limitations of relays, but introduce new problems of offset voltage and leakage currents. This Note describes the use of MOS field-effect transistors in solid-state chopper and multiplex designs that have the long life, fast speed, and small size of bipolar-transistor choppers, but eliminate their inherent offset-voltage and leakage-current problems.

### Basic Chopper Circuits

Chopper circuits are basically of either the shunt type or the series type, as shown in Fig.1, or a combination of the two.

The shunt chopper circuit, shown in Fig.1(a), operates as follows: When the switch S is opened, a voltage that is directly proportional to the input signal appears across the load. When the switch is closed, all of the input signal is shorted to ground. Therefore, if the switch is opened and closed periodically, the voltage across the load appears as a square wave that has an amplitude directly porportional to the input signal. This square wave may be highly amplified by a relatively drift-free, stable-gain ac amplifier. This procedure is generally used in low-level dc amplifiers, i.e., a small dc input is chopped, the resulting ac signal is amplified, and the output of the ac amplifier is rectified to produce a dc output directly proportional to the input.

The series chopper circuit, shown in Fig.1(b), can also be used to chop dc signals. This type of circuit is particularly useful in telemetry or other systems in which a signal source such as a transducer is to be connected periodically to a load such as a transmitter.

An ideal chopper is simply an on-off switch that has certain desirable characteristics. Table I lists

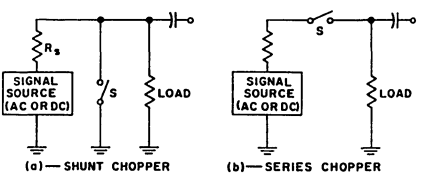


*Fig.1 - Basic chopper circuits.*

| Ideal Chopper Characteristics | Available Chopper Devices Compared to Ideal | | |
|---|---|---|---|
| | MOS | Bipolar | Electromechanical Relay |
| Infinite Life | Good | Good | Poor |
| Infinite Frequency Response | Good | Good | Poor |
| Infinite OFF Resistance | Good | Fair | Good |
| Zero ON Resistance | Poor | Fair | Good |
| Zero Driving-Power Consumption | Good | Fair | Fair |
| Zero Offset Voltage | Good | Poor | Good |
| Zero Feedthrough between the driving signal and signal being chopped | Fair | Fair | Good |
| Small Size | Good | Good | Poor |

*Table I - Comparison of available chopper devices with an ideal.*

some of these characteristics, and shows the relative merits of relays, bipolar transistors, and MOS transistors in each area.

### Use of MOS Transistors as Choppers

Fig.2 shows voltage-current characteristics of an n-channel depletion-type MOS field-effect transistor such as the RCA-40460. Fig.3 shows an expanded view of the curves in Fig.2(a) in the region about the origin.

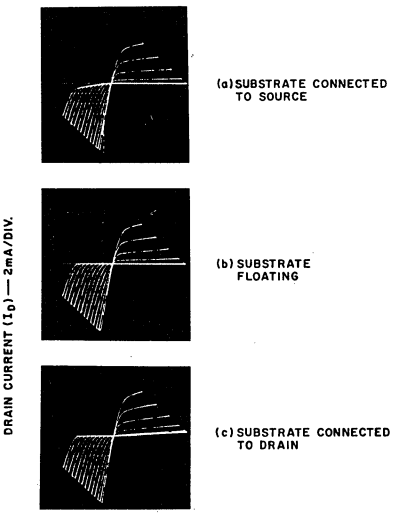


*Fig.2 - Voltage-current characteristics of an n-channel depletion-type MOS transistor: (a) with substrate connected to source; (b) with substrate floating; (c) with substrate connected to drain.*

Because each curve passes through the origin, the MOS transistor is said to have zero offset voltage. In an MOS shunt chopper circuit, therefore, the output is zero when the input voltage is zero. This result is not obtained with bipolar transistors. Even for zero input voltage, a bipolar transistor has an offset voltage equivalent to the collector-to-emitter saturation voltage $V_{CE}(sat)$ between its collector and emitter terminals. MOS transistors have no parameter comparable to $V_{CE}(sat)$.

When the gate-to-source voltage $V_{GS}$ is zero, an MOS transistor such as the 40460 has an effective resistance of 200 to 300 ohms between its drain and source terminals. If the gate-to-source voltage is made positive, this resistance decreases to about 100 ohms (typically to 90 ohms for the 40460). No significant increase in gate current occurs when $V_{GS}$ is made positive because the gate of an MOS transistor is insulated from the source-to-drain channel by an oxide layer. (In a junction-gate field-effect transistor, the gate and the channel form a p-n junction, and low gate current can be obtained only when this junction is reverse-biased.) When the resistance between the drain and source terminals is low (100 to 300 ohms), an MOS transistor is said to be ON; the drain-to-source channel resistance is then designated as $r_{ds}(ON)$. This ON condition corresponds to the closed-switch condition in the circuits of Fig.1.

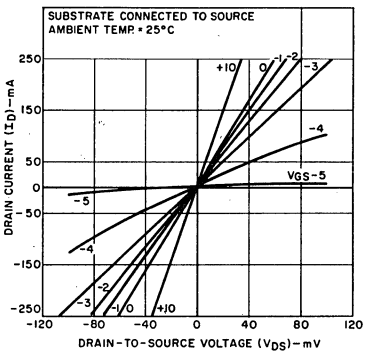


*Fig.3 - Low-level drain current as a function of drain-to-source voltage in an n-channel depletion-type MOS transistor with substrate connected to source.*

When a negative voltage of about -6 volts or more is applied between the gate and the source of the MOS transistor, the channel resistance between drain and source becomes extremely high (typically thousands of megohms). In this condition, which is known as "cut-off" or "pinchoff", it is impractical to measure the channel resistance directly; instead, the leakage current that flows from drain to source at cutoff is normally specified. This current $I_D(OFF)$, is typically 0.1 nanoampere for the 40460. Because $I_D(OFF)$ is measured at a drain-to-source voltage of 1 volt, the equivalent channel resistance is 10,000 megohms. This OFF condition corresponds to the open-switch condition in the circuits of Fig.1.

Fig.4 shows three basic chopper circuits using the MOS field-effect transistor. The gating signal for the 40460 should swing from zero to at least -6 volts, and may cover a range as large as ±10 volts. The substrate (and thus the case) of the 40460 transistor is usually connected to the source. However, if the incoming

signal to be chopped exceeds -0.3 volt, the substrate must be "floated", connected to the drain, or biased negatively so that the source-to-substrate and drain-to-substrate voltages never exceed -0.3 volt. If this value is exceeded, the substrate, which forms two p-n junctions with the drain and the source, becomes forward-biased and the resulting flow of diode current shunts the incoming signal to ground.

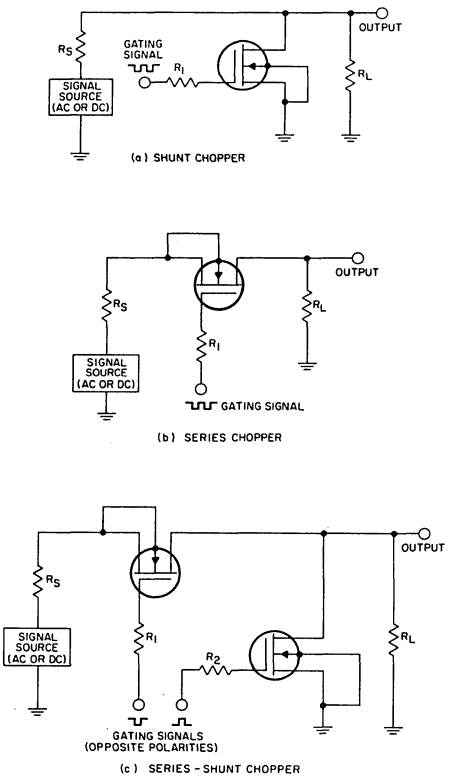


*Fig.4 - Basic MOS chopper circuits.*

### Steady-State Conditions

Ideally, when an MOS transistor in a shunt chopper circuit is ON, the output voltage of the circuit should be zero. Because the drain-to-source resistance $r_{ds}$ is some finite value, however, the output cannot reach true zero. Fig.5 shows an equivalent circuit for steady-state conditions in an MOS shunt chopper. For the ON condition, the output voltage $E_O$ is given by

$$E_O = E_S \left[ \frac{\dfrac{r_{ds}\, R_L}{r_{ds} + R_L}}{R_S + \dfrac{r_{ds}\, R_L}{r_{ds} + R_L}} \right] \quad (1)$$

In Eq.(1), it is assumed that the gate leakage resistance $R_G$ is much larger than the drain-to-source resistance $r_{ds}$. If the load resistance $R_L$ is also much larger than $r_{ds}$; Eq.(1) can be simplified as follows:

$$E_O = E_S \left[ \frac{r_{ds}}{R_S + r_{ds}} \right] \quad (2)$$

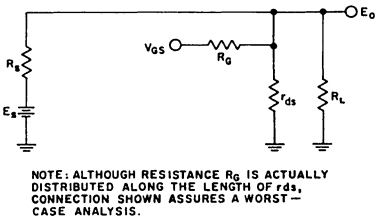


*Fig.5 - Steady-state equivalent circuit of MOS shunt chopper.*

For $E_O$ to approach zero, it is necessary that the source resistance $R_S$ be much greater than $r_{ds}$. The value of $E_O$ is then given by

$$E_O = E_S\,(r_{ds}/R_S) \quad (3)$$

A typical value for $R_S$ and $R_L$ in an MOS shunt chopper is 0.1 megohm. A typical value of $r_{ds}$(ON) for the 40460 transistor is 90 ohms. If these values are substituted in Eq.(3) and the signal voltage $E_S$ is assumed to be 1 millivolt, $E_O$ is calculated as follows:

$$E_O = 10^{-3}\,(90/10^5) = 0.9 \text{ microvolt}$$

In the ON condition, therefore, the dc error voltage is less than 0.1 per cent for the values used, and is directly proportional to the input signal.

For the OFF condition, the steady-state output voltage $E_O$ is given by

$$E_O = E_S \left[ \frac{\dfrac{r_{ds}\, R_L}{r_{ds} + R_L}}{R_S + \dfrac{r_{ds}\, R_L}{r_{ds} + R_L}} \right] + V_{GS} \left[ \frac{\dfrac{r_{ds}\, R_L}{r_{ds} + R_L}}{R_G + \dfrac{r_{ds}\, R_L}{r_{ds} + R_L}} \right] \quad (4)$$

In most MOS transistors, both $r_{ds}(OFF)$ and $R_G$ are much greater than $R_L$. Therefore, Eq.(4) may be simplified as follows:

$$E_O = E_S \frac{R_L}{R_S + R_L} + V_{GS} \frac{R_L}{R_G} \qquad (5)$$

If $R_S$, $R_L$, and $E_S$ are assumed to have the values used previously, the gate-to-source voltage $V_{GS}$ is assumed to be -10 volts, and the gate resistance $R_G$ is assumed to be $10^{12}$ ohms (minimum permissible gate resistance for the 40460), the value of $E_O$ is calculated as follows:

$$E_O = 10^{-3}\left[\frac{10^5}{2 \times 10^5}\right] - 10 \left[\frac{10^5}{10^{12}}\right]$$

$$= \frac{10^{-3}}{2} - 10^{-6} \approx 0.5 \text{ millivolt}$$

The second term in Eq.(5) is the error term for the OFF condition; it is not proportional to the input signal $E_S$. For the numbers used, the output error in the OFF condition is only 0.2 per cent. If a typical value of $10^{14}$ ohms is used for the 40460 gate resistance instead of the minimum value of $10^{12}$ ohms, the error voltage is reduced to only 0.002 per cent. The output error remains small for any value of signal voltage $E_S$ that does not approach the error voltage in magnitude.

Because the error voltage is inversely proportional to the gate leakage resistance $R_G$, most junction gate field-effect transistors produce larger error voltages than MOS transistors (the minimum $R_G$ of most junction-gate devices is only 1 to 10 per cent that of MOS transistors).

A similar procedure may be used for analysis of series chopper and series-shunt chopper circuits.

The operation of all MOS chopper circuits is greatly affected by the magnitude of the source and load resistances. Table II lists the output voltages of the three basic chopper circuits for various combinations of source and load resistances. It is assumed that the input voltage $E_S$ is 1 millivolt, and that the drain-to-source resistance $r_{ds}$ is 100 ohms in the ON condition and 1000 megohms in the OFF position. The gate leakage resistance $R_G$ ($10^{12}$ ohms or more) is neglected. The following conclusions can be drawn from the data shown:

1. Only the series or the series-shunt circuit should be used when $R_S < r_{ds}(ON)$.
2. In general, $R_L$ should be high. ($R_L >> r_{ds}(ON)$)
3. The load resistance should be higher than the source resistance. ($R_L \geq R_S$)
4. The performance of the series-shunt circuit is equal to or better than that of either the series or the shunt chopper alone for any combination of $R_S$ and $R_L$.

| Source Resistance $R_S$ (ohms) | Load Resistance $R_L$ (ohms) | Approximate Output Voltage $E_o$ - $\mu$V (Max. Output = 1 mV) Shunt Chopper (ON) | Shunt Chopper (OFF) | Series Chopper (ON) | Series Chopper (OFF) | Series-Shunt Chopper (ON) | Series-Shunt Chopper (OFF) |
|---|---|---|---|---|---|---|---|
| 1 M | 1 M | 0.1 | 500 | 500 | 1 | 500 | 0.0001 |
| 100 K | 1 M | 1 | 900 | 900 | 1 | 900 | 0.0001 |
| 100 | 1 M | 500 | 1000 | 1000 | 1 | 1000 | 0.0001 |
| 0 | 1 M | 1000 | 1000 | 1000 | 1 | 1000 | 0.0001 |
| 1 M | 100 K | 0.1 | 90 | 90 | 0.1 | 90 | 0.0001 |
| 1 M | 100 | 0.05 | 0.1 | 0.1 | 0.0001 | 0.1 | 0.00005 |
| 100 K | 100 K | 1 | 500 | 500 | 0.1 | 500 | 0.0001 |
| 100 | 100 | 333 | 500 | 333 | 0.0001 | 333 | 0.00005 |

*Table II - Steady-state chopper output voltage for various source and load resistances.*

### Transient Conditions

Fig.6 shows the ac equivalent circuit of an MOS shunt chopper. The interelectrode capacitances of the MOS transistor affect operation of the circuit at high frequencies. The input capacitance $C_{gs}$ increases the rise time of the gate driving signal and thus increases the switching time of the chopper. This effect is not usually a serious limitation, however, because the

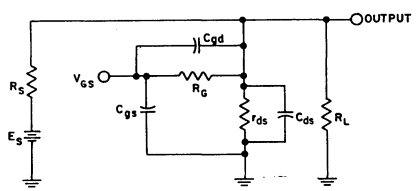


*Fig.6 - AC equivalent circuit of MOS shunt chopper.*

switching time of the MOS transistor depends primarily on the input and output time constants. Switching times as short as 10 nanoseconds can be achieved when an MOS transistor is driven from a low-impedance generator and the load resistance is less than about 2000 ohms.

The output capacitance $C_{ds}$ also tends to limit the maximum frequency that can be chopped. When the reactance of this capacitance becomes much lower than the load resistance $R_L$, the chopper becomes ineffective because $X_{C_{ds}}$ is essentially in parallel with $R_L$ and $r_{ds}(OFF)$.

The feedthrough capacitance $C_{gd}$ is the most important of the three interelectrode capacitances because it couples a portion of the gate drive signal into the load circuit and causes a voltage spike to appear across $R_L$ each time the gate drive signal changes state. $C_{gd}$ and $R_L$ form a differentiating network which allows the leading edge of the gate drive signal to pass through. The output capacitance $C_{ds}$ is beneficial to the extent that it helps reduce the amplitude of the feedthrough spike.

The effect of the feedthrough spikes can be reduced by several methods. Typical approaches include the following:

(a) use of a clipping network on the output when the input signal to be chopped is fixed in amplitude,

(b) use of a low chopping frequency,

(c) use of an MOS transistor that has a low feedthrough capacitance $C_{gd}$ (some RCA MOS transistors have typical $C_{gd}$ values as low as 0.13 picofarad),

(d) use of a gate drive signal that has poor rise and fall times,

(e) use of a source and load resistance as low as feasible,

(f) use of a shield between the gate and drain leads,

(g) use of a series-shunt chopper circuit.

### Temperature Variations

The variation of MOS transistor parameters with temperature can affect the operation of a chopper circuit unless allowance is made for such variations in the circuit design. It is important, therefore, to determine the approximate degree to which each parameter can be expected to change with temperature. Fig.7 shows curves of channel resistance $r_{ds}$, gate leakage current

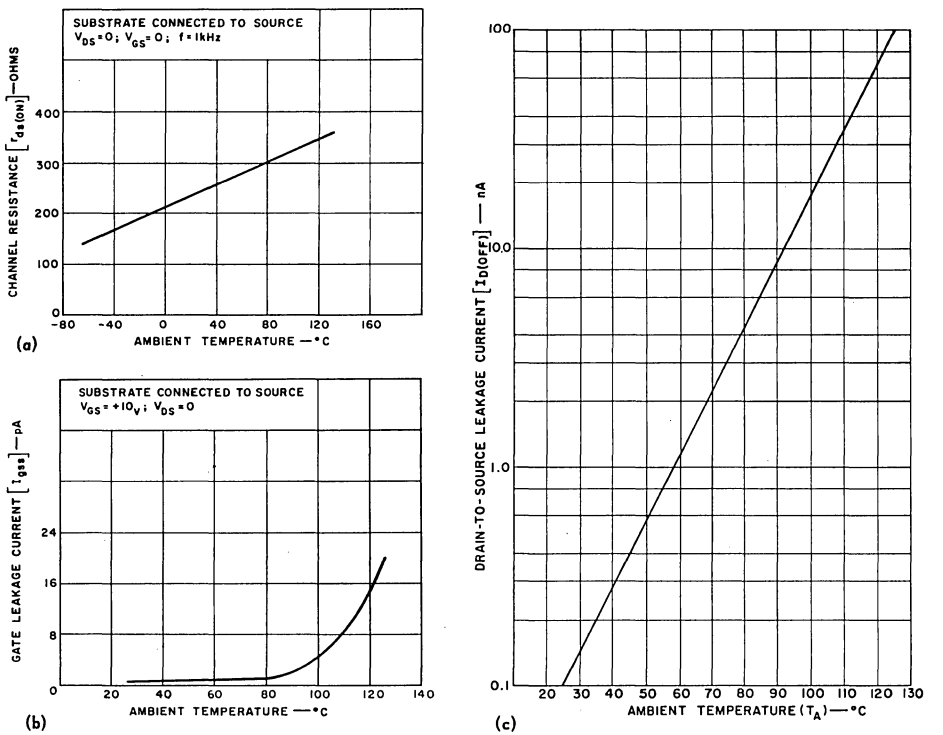


*Fig.7 - Variation of 40460 parameters with ambient temperature: (a) channel resistance $r_{ds}$; (b) gate leakage current $I_{gss}$; (c) drain-to-source leakage current $I_{D(OFF)}$.*

$I_{GSS}$, and drain-to-source leakage current $I_{D(OFF)}$ as a function of temperature for the 40460. $I_{GSS}$ and $I_{D(OFF)}$ were not measured at temperatures below 25° C because condensation and frost that form on the test chassis result in erroneous and/or erratic readings of pico-ampere currents. Test circuits used to measure these parameters are shown in the Appendix.

### Typical Circuits

Fig.8 shows three chopper circuits that were constructed for demonstration purposes: (a) a shunt chopper, (b) a series chopper, and (c) an ac chopper. The 0.005-microfarad capacitor across the gate drive generator in

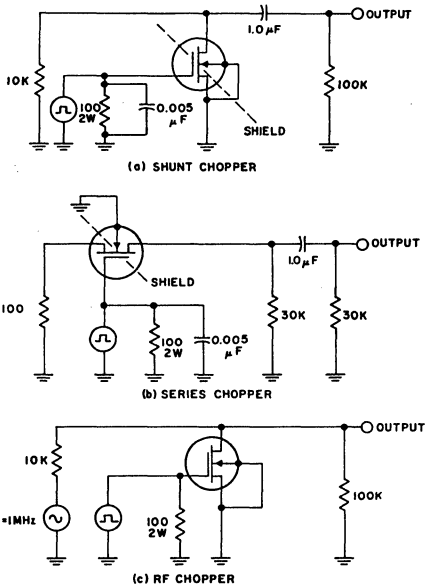


*Fig.8 - Typical MOS chopper circuits: (a) shunt chopper; (b) series chopper; (c) rf chopper.*

circuits (a) and (b) increases the rise time of the gate drive signal. A resistor is used in each circuit to simulate the impedance of the signal source. The actual input voltage was set at zero so that spike feedthrough and offset voltages could be measured. The dc offset voltage, which is caused primarily by the average value of the spikes over the whole cycle, was too small to be measured on the equipment available. Fig.9 shows the actual spike feedthrough for the 40460 and 3N128 MOS transistors in the shunt and series circuits of Figs.8(a) and 8(b); the rise time of the gate drive signal was 1 microsecond.

It is recommended that MOS choppers be driven from a square-wave source. Fig.10 shows the feed-through that results when the circuits of Figs.8(a) and 8(b) are driven from a sine-wave generator instead of a square wave.

Fig.11 shows how the circuit of Fig.8(c) can be used to chop an rf signal at either a slow or a fast chopping frequency. The 40460 transistor can be used to chop rf signals extending up to the low vhf region. The frequency of the gate drive signal can be as high as several hundred kilohertz before excessive degradation of the square wave occurs. The rise time of the

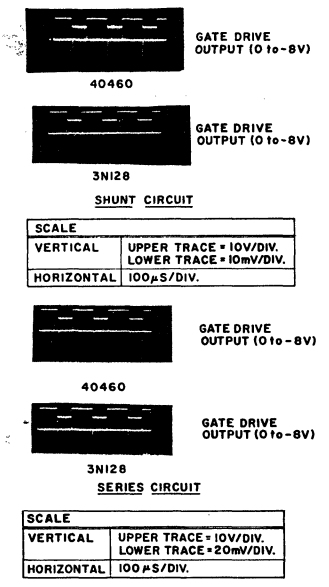


*Fig.9 - Actual spike feedthrough in shunt and series chopper circuits employing the 40460 and 3N128 MOS transistors.*

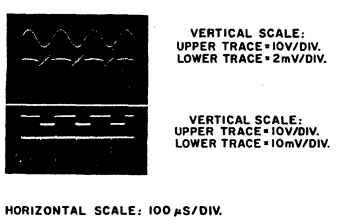


*Fig.10 - Comparison of sine- and square-wave gate drive for an MOS shunt chopper employing the 40460.*

gate drive signal for the circuit of Fig. 8(c) was 15 nanoseconds.

In field-effect-transistor choppers using a version of the series-shunt circuit shown in Fig.8(c), noise and offset voltages as low as 10 microvolts or less have been obtained.[1] Balanced MOS chopper circuits using special compensating networks have also been developed to chop 0.1-microvolt signals at impedance levels up to 40,000 ohms and chopping frequencies up to 250 Hz.[2]


*Fig.11 - Results of using MOS rf chopper at a fast and a slow chopping frequency.*

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2. J.J. Hitt and G. Mosley, "FET Chopper Circuits for Low-Level Signals", 1967 IEEE CONVENTION DIGEST, page 488.

## APPENDIX

### Test Circuits

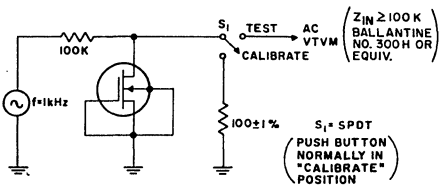



*Fig.A-1 - Channel resistance ($r_{ds}(ON)$) measurement circuit.*

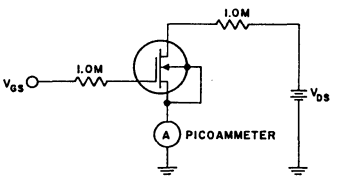



*Fig.A-2 - Cutoff current ($I_D(OFF)$) measurement circuit.*

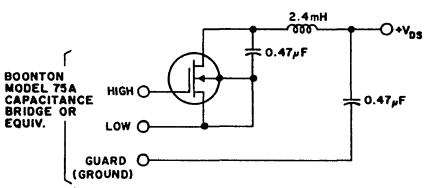



*Fig.A-3 - Input capacitance ($C_{iss}$) measurement circuit.*

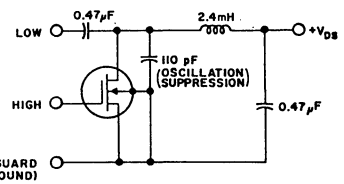



*Fig.A-4 - Reverse transfer (Feedback) capacitance ($C_{rss}$) measurement circuit.*

# An FM Tuner Using an RCA-40468 MOS-Transistor RF Amplifier

by

H. M. Kleinman and C. H. Lee

Previous work with field-effect transistors in general, and MOS field-effect transistors in particular, has demonstrated the superior signal-handling capability of this type of device.[1-3] This Note describes an FM tuner that incorporates an MOS field-effect transistor as the rf amplifier, and shows how the MOS transistor is instrumental in minimizing the spurious responses normally found in FM receivers.

Spurious responses result when harmonics of an unwanted incoming signal mix with harmonics of the local-oscillator signal to produce a difference frequency which falls within the if passband of the receiver.* When these harmonics of unwanted signals are created in the rf amplifier, they may be removed by improved filtering between the rf amplifier and the mixer. When used as an rf amplifier, the MOS transistor produces an output signal that contains low levels of the harmonics of unwanted signals. As a result, the need for a double-tuned rf interstage transformer is reduced and acceptable performance can generally be achieved with single-tuned circuits in both the antenna and rf interstage sections.

The FM tuner described in this Note utilizes an RCA-40468 MOS rf amplifier, an RCA-40478 bipolar mixer, and an RCA-40244 bipolar oscillator. The rf-stage gain of 12.7 dB and mixer gain of 21.8 dB yield a total tuner gain of 34.5 dB. A three-stage if-amplifier strip that uses RCA-40482 bipolar transistors and exhibits 94 dB of gain completes the FM tuner.

Table I summarizes the performance of the system. The figure shown for if rejection was achieved when the tuner section was tested with a fully shielded, remotely located if-amplifier strip. When the final tuner was assembled, only partial shielding was used around the if amplifier. This partial shielding, coupled with the close proximity of tuner and if amplifier, reduced the if rejection to 77 dB.

| | | |
|---|---|---|
| Carrier Frequency | 100 | MHz |
| Modulation | 400 Hz, 22.5 kHz deviation | |
| Sensitivity:* | | |
| For 20-dB signal-to-noise ratio | 1.4 | μV |
| For 30-dB signal-to-noise ratio | 2.2 | μV |
| For -3-dB limiting point (with 94-dB if strip) | 1.6 | μV |
| Image Rejection◆ | 72 | dB |
| IF Rejection◆ | 91 | dB |
| Half-IF Rejection◆ | 96 | dB |
| Rejection of Other Spurious Responses◆ (with 0.2 volt at antenna terminals) | >100 | dB |

* Measured at antenna terminals (300-ohm nominal impedance).

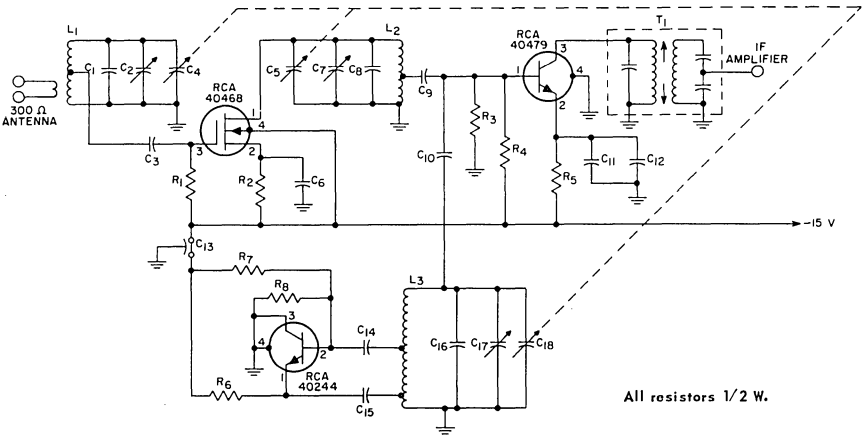
◆ Relative to 2 μV.

*Table I - Over-all Tuner Performance*

### Circuit Considerations

The rf section of the tuner is shown in Fig.1, and the if strip in Fig.2. The if strip, which is described more fully elsewhere,[4] utilizes three 40482 bipolar transistors that operate at collector currents of 3.5

* In a receiver tuned to 100 MHz, the local oscillator is tuned to 110.7 MHz. The second harmonic of the local oscillator occurs at 221.4 MHz. A signal at a frequency of 210.7 MHz can beat with the 221.4-MHz signal to form the 10.7-MHz intermediate frequency. This 210.7-MHz frequency is the second harmonic of 105.35 MHz, which is above the desired channel by half the intermediate frequency.




| | | | |
|---|---|---|---|
| $R_1$ | = 100 KΩ | $C_1, C_8, C_{16}$ | = 16 pF |
| $R_2$ | = 220 KΩ | $C_2, C_7$ | = 2-12 pF, Trimmer |
| $R_3, R_4$ | = 47 KΩ | $C_3, C_6$ | = 0.002 μF |
| $R_5$ | = 4.7 KΩ | $C_4, C_5, C_{18}$ | = 5.5-22.5 pF, ganged tuning capacitor |
| $R_6$ | = 8.2 KΩ | $C_9$ | = 5000 pF |
| $R_7$ | = 120 KΩ | $C_{10}$ | = 2.7 pF |
| $R_8$ | = 22 KΩ | $C_{11}$ | = 0.01 μF |
| | | $C_{12}, C_{14}, C_{15}$ | = 1000 pF |
| | | $C_{13}$ | = 1000 pF feedthrough type |
| | | $C_{17}$ | = 2-10 pF, Trimmer |

$L_1$ = #18 bare copper wire, 4 turns, 1/4" I.D., 7/16" winding length, $Q_o$ at 100 MHz = 130.
Tunes with 34 pF capacitance at 100 MHz.
Antenna Link approximately 1 turn from ground end.
Gate Tap approximately 1-1/2 turns from ground end.

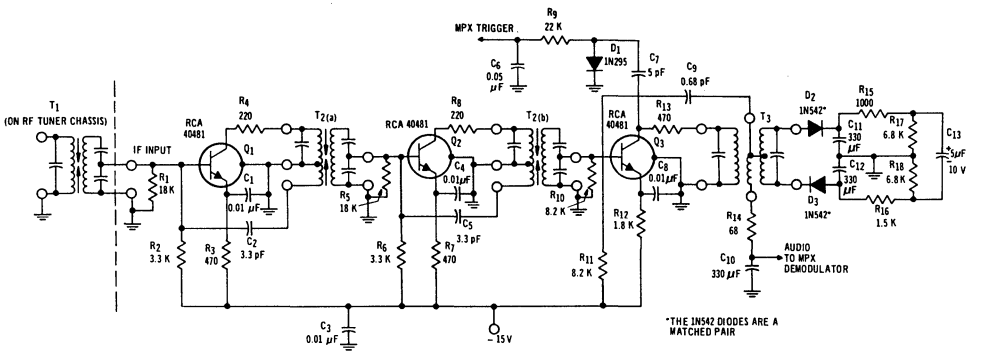
$L_2$ = #18 bare copper wire, 4 turns, 1/4" I.D., 7/16" winding length, $Q_o$ at 100 MHz = 120.
Tunes with 34 pF capacitance at 100 MHz.
Base Tap approximately 3/4-turn.

$L_3$ = #18 bare copper wire, 4 turns, 7/32" I.D., 7/16" winding length, $Q_o$ at 100 MHz =120.
Tunes with 34 pF capacitance at 100 MHz.
Emitter Tap approximately 1-1/2 turns from ground end.
Base Tap approximately 2 turns from ground end.

***Fig.1 - Typical FM receiver front end using RCA-40468 MOS field-effect transistor.***

milliamperes in neutralized configurations and provide an over-all if gain of 94 dB.

The rf section provides a total gain of 34.5 dB, which includes 12.7 dB in the rf stage and 21.8 dB in the mixer. The mixer and oscillator were designed according to principles established previously,[5,6] and details of their design are not discussed. The common-collector oscillator provides an extremely clean oscillator waveform. In addition, the low injection level at the mixer base, 25 to 30 millivolts, coupled with the design of the preceding circuits, limits the maximum possible signal at the mixer base and minimizes the generation of spurious responses in that stage.




| | |
|---|---|
| $T_1$ | TRW-EO-21124-RA |
| $T_{2(a)}$, $T_{2(b)}$ | TRW-EO-21125-R1 |
| $T_3$ | TRW-EO-23023 |

All resistors 1/4 watt
0.01- and 0.05-μF capacitors, 50-V ceramic disks
330-pF capacitors, 1-kV disks

*Fig.2 - Typical if-amplifier strip.*

### RF-Stage Design

The 40468 rf stage is designed to achieve the published maximum usable stable gain of 14 dB at a nominal operating point of 5 milliamperes. Additional losses of 1.3 dB reduce the actual gain in the tuner to 12.7 dB. Details of the rf-stage design are given in the Appendix.

Selection of the appropriate source and load impedances for the rf stage is based on the fact that a low spurious response requires the gate of the 40468 to be tapped as far down on the antenna coil as gain and noise considerations permit. This arrangement applies the smallest possible voltage swing to the gate and makes optimum use of the available dynamic range. (In a bipolar tuner designed to optimize the rejection of spurious responses, the tap point on the antenna coil was approximately 25 ohms.)

For low spurious response, therefore, the entire rf coil is used as the load for the 40468. The interstage coil presents a load impedance to the rf stage of 3800 ohms, which nearly matches the 4200-ohm output impedance of the 40468. Although this arrangement loads the interstage coil and causes a degradation of selectivity of the front end, it is an acceptable compromise in this case because the antenna coil is not loaded by the gate of the MOS transistor.

As indicated by the calculations in the Appendix, this approach yields a source impedance of approximately 200 ohms for the 4500-ohm input impedance of the gate of the 40468.

### Tuner Performance

Performance of the tuner with respect to sensitivity limiting, if rejection, and image rejection compares favorably with that of tuners using high-performance bipolar transistors. Figs.3, 4, and 5 show typical performance characteristics of the receiver. Receiver performance, particularly as regards spurious-response-rejection figures, is highly dependent on such factors as physical layout, power-supply decoupling, and care in construction. The use of a negative supply voltage facilitates the grounding of tuned circuits and the decoupling of the supply.

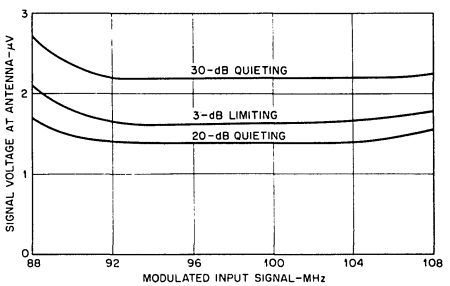



*Fig.3 - Sensitivity curves for FM receiver using circuits of Figs.1 and 2.*

The elimination of spurious response was the primary goal in this design. Generally, a circuit that has a low spurious response is difficult to reproduce. In some systems, the performance of such a circuit depends on the exact operating points of the transistors used; when the rf-amplifier transistor in Fig.1 was repeatedly changed, performance of the tuner remained essentially the same. The best correlation was found with the operating current of the transistor in the circuit. Fig.6 shows the change in the rejection of the "half-if" spurious response as a function of drain current for a

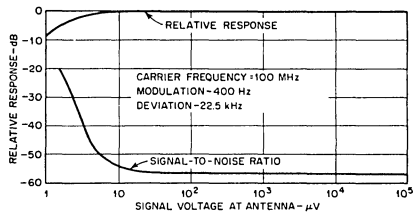



*Fig.4 - Relative response as a function of signal voltage measured at antenna terminals.*

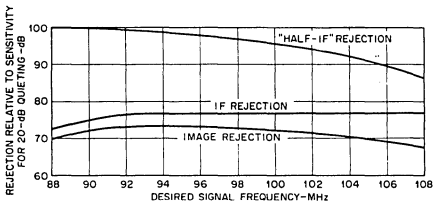



*Fig.5 - Spurious-response rejection as a function of frequency.*

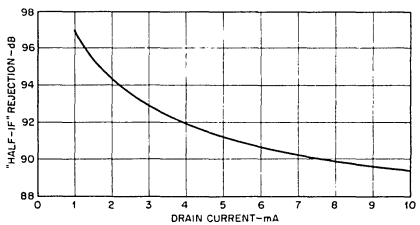



*Fig.6 - Half-if rejection as a function of operating point.*

typical 40468. For the normal spread of operating current in this circuit of 3.5 to 7 milliamperes, the variation in rejection is shown to be about ± 1 dB.

Fig.7 shows the variation of 20-dB quieting sensitivity as a function of drain current, and indicates why the 5-milliampere nominal operating point was chosen. Below 3 milliamperes, the sensitivity of the receiver degrades very rapidly. However, at 5 milliamperes the actual spread of 3.5 to 7 milliamperes causes a negligible change in performance.

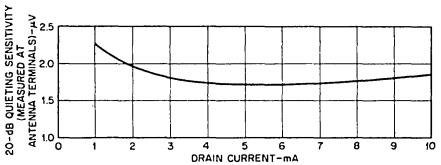



*Fig.7 - 20-dB quieting sensitivity as a function of operating point.*

## Conclusions

The 40468 MOS field-effect transistor has been incorporated into an FM tuner in which all other stages are high-performance, low-capacitance bipolar types. The wider dynamic range of the MOS transistor provides significant improvements in the rejection of spurious responses over results previously achieved with bipolar rf amplifiers.

Most significantly, the performance with respect to spurious-response rejection has been repeated when devices with wide parameter variations have been used. Furthermore, the system has been duplicated with comparable results. These two factors strongly indicate that the performance advantages are real and are attributable to the characteristics of the MOS rf amplifier used rather than the result of cancellation or peculiar trapping in a single tuner.

**Appendix - Design of 40468 RF-Amplifier Stage**

The following parameters are important in the design of the rf-amplifier stage:

40468 parameters (at $V_{DD}$ = 15 V, $I_D$ = 5 mA):

| | | |
|---|---|---|
| input resistance $R_{in}$ | 4500 | ohms |
| output resistance $R_{out}$ | 4200 | ohms |
| forward transmittance $y_{fs}$ | 7500 | $\mu$mhos |
| feedback capacitance $C_{rss}$ (max). | 0.2 | pF |

mixer-stage parameters:

| | | |
|---|---|---|
| input resistance $R_{in}$(mix) | 550 | ohms |
| input stability IS(mix) (from previous design) | 4 | |

coil data:

| | | |
|---|---|---|
| mounted unloaded Q | 120 | |
| tuning capacitance $C_T$ at 100 MHz | 34 | pF |
| antenna impedance | 300 | ohms |

Fig.8 shows the ac equivalent circuit for the rf stage. At resonance, this circuit reduces to the form

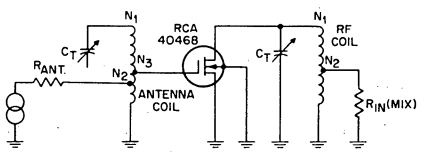



*Fig.8 - AC equivalent circuit of the 40468 rf stage.*

shown in Fig.9, where all impedances are referred to the gate and drain terminals of the 40468. The maximum available gain (MAG) is the gain in a conjugately matched, unilateralized circuit and is defined as follows:

$$MAG = \frac{|y_{fs}|^2 R_{in} R_{out}}{4} \quad (1)$$

For the values given above, MAG = 266 = 24.2 dB.

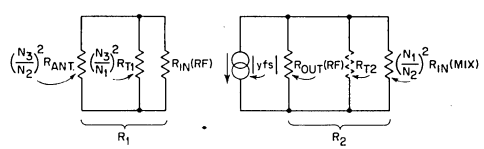



*Fig.9 - Equivalent input ($R_1$) and output ($R_2$) circuit of the rf stage during resonance.*

The maximum usable gain MUG is the stable gain which may be realized in a practical neutralized or unneutralized circuit. It is defined by the relationship for the unneutralized case as follows:

$$MUG = \frac{2|y_{fs}|}{\omega C_{rss}} \times \frac{a}{b} \quad (2)$$

where a is a skew factor smaller than unity which is used to maintain bandwidth, and b is a number equal to or greater than unity related to the number of stages (inserted to maintain bandwidth in multistage amplifiers). A skew factor of 0.2 is generally used. Because only one stage of 100-MHz gain is used in the amplifier shown in Fig.1, b = 1. For the values given, therefore, MUG is given by

$$MUG = \frac{0.4\, y_{fs}}{\omega C_{rss}} = 23.5 = 13.7 \text{ dB} \quad (3)$$

The total mismatch loss is called the stability factor S, and is equal to the difference (in dB) between MAG and MUG, as follows:

$$S = MAG - MUG = 10.5 \text{ dB, or } 11.3 \text{ times} \quad (4)$$

This value is arbitrarily divided between the input and output circuits by use of an input stability IS and an output stability OS, as follows:

$$IS = R_{in}/2R_1 \quad (5)$$

$$OS = R_{out}/2R_2 \quad (6)$$

where $R_1$ and $R_2$ are the total parallel impedances at the input terminal (gate) and the output terminal (drain), respectively. These stability terms are related to the stability factor S as follows:

$$S = IS \times OS \quad (7)$$

The division between IS and OS is made by means of some arbitrary choices. As mentioned previously, it was decided to maximize IS so that the signal level at the gate would be minimized. This choice necessitates matching or nearly matching $R_{out}$ to its load. Therefore, the entire rf coil is used as the output load.

As indicated in Eq.(6), the value of $R_2$ must be determined to define OS; the value of IS can then be determined and the input circuit defined. $R_2$ consists of the parallel combination of $R_{out}$, $R_{T2}$, and $(N_1/N_2)^2 \times R_{in}$(mix), where $R_{T2}$ is the tuned impedance of the rf coil and is given by

$$R_{T2} = Q_o/\omega_o C_t \quad (8)$$

The value of $R_{out}$ is given above as 4200 ohms. The value of $R_{T2}$ as calculated from Eq.(8) is 5600 ohms. The value of the input impedance of the mixer $R_{in}$(mix), obtained from the published data for the 40479, is 550 ohms. The only remaining component of $R_2$ to be determined is the turns ratio $N_1/N_2$.

In Fig.8, the rf coil $L_2$ represents both the input circuit of the mixer and the output circuit of the rf stage. Therefore, the stability of the mixer stage must also be considered. Because stability factors are equal to resistance ratios, the input stability of the

mixer can be considered at the top of the rf coil, as follows:

$$IS(mix) = \frac{(N_1/N_2)^2 R_{in(mix)}}{2R_2} \quad (9)$$

The value of IS(mix) was specified above as 4 (from a previous design). Because $R_2$ is a linear function of $(N_1/N_2)^2 R_{in(mix)}$, manipulation of the data through several steps provides a value of 5.5 for $(N_1/N_2)$ and a reflected value of 16,800 ohms for $R_{in(mix)}$.

The output stability of the rf stage can then be determined. $R_2$ is computed as the parallel combination of $R_{out}$, $R_{T2}$, and $(N_1/N_2)^2 R_{in(mix)}$, and is found to be 2100 ohms. The output stability OS is determined from Eq.(6), as follows:

$$OS = R_{out}/2R_2 = 4200/(2 \times 2100) = 1$$

The value of unity indicates an impedance match between $R_{out}$ and the load.

The input stability of the rf amplifier can then be determined from Eq.(7), as follows:

$$IS = S/OS = 11.3$$

By use of this stability term, the input-circuit constants can be calculated. $R_1$ is determined from Eq.(5), as follows:

$$R_1 = R_{in}/2IS = 191 \text{ ohms}$$

This value is so much lower than $R_{in}$ that it is apparent the MOS transistor does not load the antenna coil at all.

Because it is desired to match the antenna with the input circuit, the value of $R_1$ should be one-half the reflected antenna impedance. Therefore, the value of $(N_3/N_2)^2 R_{ANT}$ is 382 ohms, which is a very slight step up. Because two of the three component terms of $R_1$ are then known, the remaining term $(N_3/N_1)^2 R_{T1}$ can be determined as 456 ohms. The turns ratios are then given by

$$N_1/N_2 = 4.3$$
$$N_1/N_3 = 3.7$$

The values of circuit components obtained by means of this design method are given in the parts list for Fig.1.

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# An FM Tuner Using Single-Gate MOS Field-Effect Transistors as RF Amplifier and Mixer

by
C.H. Lee and S. Reich

Selection of the transistors for use in FM-tuner stages involves consideration of such device characteristics as spurious response[1], dynamic range, noise immunity, gain, and feedthrough capacitance. MOS field-effect transistors are especially suitable for use in FM rf-amplifier and mixer stages because of their inherent superiority for spurious-response rejection and signal-handling capability. This Note describes an FM tuner that uses an RCA-40468 MOS transistor as the rf amplifier and an RCA-40559 MOS transistor as the mixer. A conversion gain of 17.5 dB was obtained, to provide an over-all tuner gain of approximately 30 dB. RF and mixer circuit considerations pertinent to the design are discussed.

## Performance Features of MOS Transistors

Spurious response in an FM tuner is caused by the mixture of unwanted signals with the desired carrier in either the rf stage or the mixer. This effect can be expressed mathematically by use of the Taylor series expansion of the simple transfer function of output current as a function of input voltage at the operating point, as follows:

$$i_o = I_o + \alpha e_s + \beta e_s^2 + \theta e_s^3 + \ldots \qquad (1)$$

where $i_o$ is the instantaneous value of output current of the device; $I_o$ is the dc component of output current; $e_s$ is the rf signal voltage present at the input terminal of the transistor; and $\alpha$, $\beta$, and $\theta$ are the coefficients of a Taylor series expansion. These coefficients are related to the first-, second-, and third-order derivatives of the transfer characteristic as determined by the bias point. It can be shown[2,3] that mixing action within the device is attributable to the second-order term ($\beta e_s^2$), and that cross-modulation and intermodulation result from third- and higher-order terms. Therefore, when a device has an inherent square-law transfer characteristic, i.e., the drain current varies as the square of the applied gate-to source voltage, third- and higher-order terms are zero and spurious response is eliminated. The transfer characteristic of MOS field-effect transistors more nearly approaches this ideal square-law relationship than the very steep exponential transfer characteristic of bipolar transistors.

The dynamic-range capability of MOS field-effect transistors is about 25 times greater than that of bipolar transistors. In an actual tuner circuit, this large intrinsic dynamic range is reduced by a factor proportional to the square of the circuit source impedances.[4] The net result is a practical dynamic range for MOS tuner circuits about five times that for bipolar types.

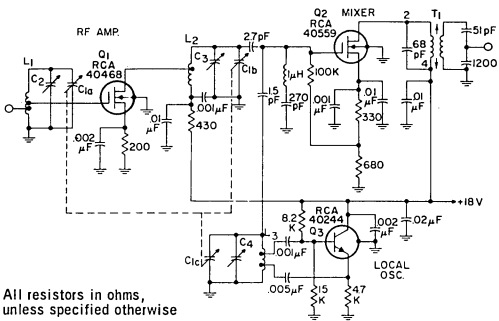
With MOS field-effect transistors, as contrasted with either bipolar transistors or junction-gate field-effect transistors, there is no loading of the input signal, nor drastic change of input capacitance even under extreme overdrive conditions.

In junction-gate field-effect transistors, a large incoming signal can have sufficiently high positive swing to drive the gate into conduction by a momentary forward bias; power is then drawn from the input signal in the same way as if a resistance were placed across the input circuit. In bipolar transistors, there is a gradual change of both input impedance and input capacitance as a function of large signal excursions. These changes are undesirable because they can result in detuning of tuned circuits and widening of the input selectivity curve.

### FM Tuner Design

The FM tuner shown in Fig.1 uses single-gate MOS field-effect transistors in the rf-amplifier and mixer stages and a bipolar transistor as the local oscillator. The rf-amplifier transistor RCA-40468 operates in the common-source configuration with a stage gain of 12.7 dB. The mixer transistor RCA-40559 also operates in the common-source configuration, with both the rf and local-oscillator signals applied to the gate terminal. The bipolar oscillator transistor RCA-40244 operates in the common-collector mode. The conversion power gain from the mixer stage is 17.5 dB; the total gain of the tuner is 30.2 dB.

Performance of the FM tuner was evaluated by use of the bipolar-transistor if amplifier shown in Fig.2. The 10.7-MHz if output from the tuner is coupled to the first if-amplifier stage by means of a double-tuned transformer $T_1$. The if amplifier employs two 40245 and one 40246 bipolar transistors, each operating in a neutralized common-emitter configuration at a collector current of 3.5 milliamperes. The over-all gain of the if amplifier is 88 dB. A detailed analysis of a similar if amplifier is covered in an earlier publication.[5]




$C_{1a}, C_{1b}, C_{1c}$ - 3-gang tuning capacitor, TRW 5-plate Model V2133 with trimmers stripped off.

$C_2, C_3, C_4$ - Arco 402 trimmer, maximum value 10 pF

$L_1$ - No.18 bare copper wire, 5 turns on 19/64" form, coil length 1/2", with IRN .250" x .250" Arnold slug. $Q_0$ = 164. Antenna tap at 0.8 of a turn, output tap at 1.4 turns.

$L_2$ - No.18 bare copper wire, 5 turns on 15/64" form, coil length 3/8", with 0.181" x 0.375" Arnold slug. $Q_0$ = 104.

$L_3$ - No.18 bare copper wire, 5 turns, air core with 3/8" O.D., coil length 1/2". Emitter tap on 1-1/2 turns. Feedback tap on 2 turns. Q = 164.

$T_1$ - Double tuned, 90 per cent of critical coupling. Primary unloaded uncoupled Q = 137 with 68-pF tuning capacitance, secondary unloaded uncoupled Q = 76 with 47-pF tuning capacitance. Secondary has a turns ratio of 26.2 to 1.0. Primary, No.32 enamel wire, 15 turns, space wound at 60 TPI, 0.250" x 0.500" TH slug. Secondary, No.36 enamel wire, 18 turns, close wound, 0.250" x 0.250" TH slug. Both coils on 9/32" form without shield.

*Fig.1 - Circuit diagram of FM tuner using MOS transistors for the rf amplifier and mixer stages.*

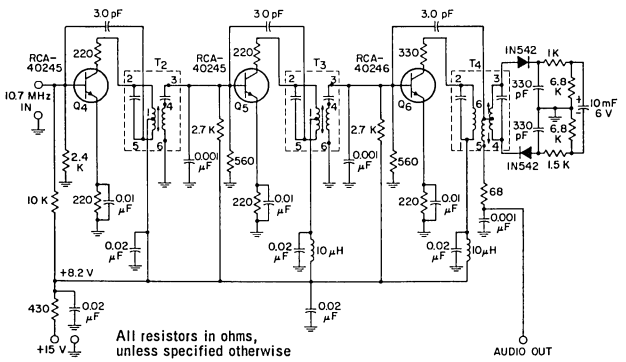



*Fig.2 - Three-stage if amplifier using bipolar transistors.*

Table I summarizes the performance of the MOS tuner. Spurious response was evaluated with a generator output of 350 millivolts.

**OVER-ALL TUNER PERFORMANCE**

| | | |
|---|---|---|
| Carrier Frequency | 100 | MHz |
| Modulation Frequency | 400 | Hz |
| Deviation (except IHFM) | 22.5 | kHz |
| Sensitivity: | | |
| IHFM | 1.75 | $\mu$V |
| 20-dB Quieting | 1.5 | $\mu$V |
| 30-dB Quieting | 1.75 | $\mu$V |
| 3-dB Limiting | 2.5 | $\mu$V |
| Image Rejection | 62 | dB |
| IF Rejection | 96 | dB |
| Half-IF Rejection | 92 | dB |
| Spurious Response across VHF band with $e_{gen.}$ = 0.35 volt | NONE | |

*Table I - Over-all performance characteristics of FM tuner.*

### RF-Circuit Considerations

The RCA-40468 MOS transistor used in the rf amplifier stage has a maximum available gain of 24 dB. Because the design criteria required a total mismatch plus insertion loss of 11.3 dB, the net gain for the stage is 12.7 dB. Although the design procedure used for these calculations has been discussed previously,[1,6] some of the considerations for optimizing performance warrant additional comment.

In the design of an rf stage for FM performance, the stage gain should be a compromise between optimum receiver sensitivity and spurious response rejection. In other words, the rf gain capability should be large to minimize the effects of noise from the mixer, and yet be limited to prevent a very large undesired incoming signal located on the skirt of the selectivity curve from driving the mixer beyond its dynamic range. Good FM tuner performance is achieved by selection of the proper rf-stage gain and step-down to the mixer input.

The rf input coil $L_1$ is tapped down to provide the smallest practical input swing to the gate of the rf-amplifier transistor for increased dynamic range. This tap-down is a compromise between optimizing for dynamic range and noise. When the degree of mismatch has been established, the drain-circuit load $L_2$ is determined from stage-gain and bandwidth requirements. Table II shows the device parameters used for the design of the rf stage.

The 40468 MOS transistor has a typical feedback capacitance of 0.12 picofarad, with a maximum value of 0.2 picofarad. This small value of $C_{rss}$ minimizes oscillator radiation feedback through the device, and also makes it unnecessary to add neutralization components to the rf stage to achieve adequate gain.

### Mixer-Circuit Considerations

The mixer circuit shown in Fig.1 is designed for operation into an 8000-ohm-load. A load up to 12,000 ohms is permissible and provides a gain increase of about 1 dB from the mixer. The input circuit is tapped down by a 2.7-picofarad capacitor in series with the device input capacitance to improve dynamic range. These mismatch losses result in a stage gain of 17.5 dB, as compared to the maximum available gain of 21.5 dB shown in the published data for the 40559 transistor.

The trap consisting of a 1-microhenry inductor and 270-picofarad capacitor is designed to bypass any 10.7-MHz component that may appear at the input to the mixer. A 1.5-picofarad capacitor couples the oscillator signal to the mixer gate. Because the capacitor is small, interaction with the oscillator tuned circuit is minimized and good oscillator stability is maintained. The injection level at the gate of the mixer is 700 millivolts rms.

The biasing arrangement for the mixer stage is particularly important: substrate bias is used to provide the optimum combination of mixing and spurious-response rejection. Fig.3 shows the shift of the transfer characteristic as a function of negative substrate bias $E_{bs}$ for the RCA-40559 mixer transistor.

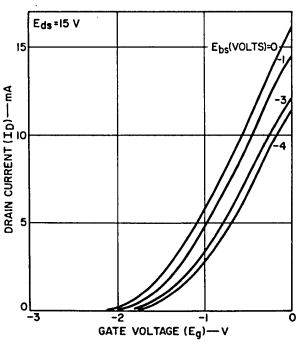



*Fig.3 - Transfer characteristics of the RCA-40559 MOS field-effect transistor for several values of substrate bias.*

The transconductance, which is the first derivative of the transfer characteristic, also varies as a function of substrate bias, as shown in Fig.4. As stated previously, mixing is accomplished by means of the quadratic term of Eq.(1); higher-order terms contribute only to undesired responses. For ideal mixing, therefore, the

transconductance curve should approach a straight line. As the transconductance curve becomes linear, higher-order derivatives (i.e., above the second) reduce to zero and the conversion transconductance increases. Fig.4 shows that the transconductance curve is most linear at

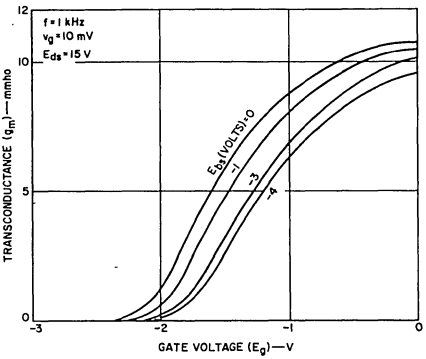



*Fig.4 - Transconductance of the RCA-40559 as a function of gate bias with the substrate voltage as the parameter.*

a substrate bias of -3 volts. Fig.5 shows the relative conversion gain of the RCA-40559 mixer stage as a function of the oscillator injection level at substrate bias of zero and -3 volts. It can be seen that the conversion transconductance also increases with the oscillator injection level.

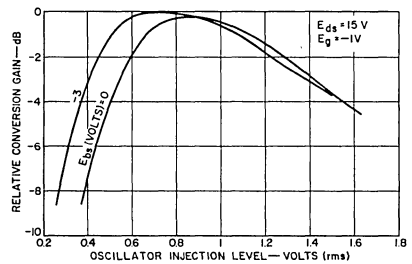



*Fig.5 - Conversion transconductance as a function of oscillator injection level.*

Table II shows the MOS device characteristics measured under circuit conditions. Reasonable verification of the measured conversion transconductance was obtained by calculation of the conversion transconductance for gate voltages ranging from zero to -2.1 volts. Details of these measurements are given in the Appendix.

| Parameter | Units | RF Amplifier RCA-40468 | Mixer RCA-40559 |
|---|---|---|---|
| $C_{rss}$ | pF | 0.12 | 0.12 |
| $R_{in}$ | KΩ | 4.5 | 6 (100 MHz) |
| $C_{in}$ | pF | 5.5 | 5.0 |
| $R_o$ | KΩ | 4.2 | 12 (10.7 MHz) |
| $C_o$ | pF | 1.4 | 1.5 |
| $y_{21}$ | mmho | 7.5 | 2.8 |
| MAG | dB | 24.2 | 21.5 |
| MUG (unneutralized) | dB | 14 | - |
| $G_p$ (in tuner) | dB | 12.7 | 17.5 |

*Table II - Device parameters for RCA-40468 and 40559 MOS field-effect transistors.*

On the basis of these results, the optimum operating conditions for the mixer circuit were empirically established at an effective gate bias of -1 volt and an effective substrate bias of -3 volts to provide a typical drain current of 3 milliamperes.

### Oscillator-Circuit Considerations

The common-collector oscillator circuit shown in Fig.1 generates an extremely clean output waveform. The absence of harmonics in the oscillator signal is an important factor in good tuner design. The oscillator signal is coupled to the mixer gate by means of a 1.5-picofarad capacitor which isolates the tuned circuit of the oscillator from the input circuit of the mixer and thus minimizes the possibility of oscillator instabilities as a result of "pulling".

### Over-all Tuner Performance

The performance of the single-gate MOS tuner with respect to sensitivity, limiting, and particularly spurious response exceeds that obtained with the best bipolar transistors. In general, spurious-response performance can be degraded by inadequate circuit layout and wiring practices. For this reason, care should be exercised in arranging the physical layout of the tuner, and power-supply decoupling should be used.

Figs.6 and 7 show the measured sensitivity of the tuner of Fig.1. The quieting sensitivity, shown in Fig.6, is practically flat across the entire FM band. IHFM sensitivity and 3-dB limiting, shown in Fig.7, show the same excellent performance. The IHFM sensitivity test input voltage, as defined by the Institute of High Fidelity Manufacturers, is the minimum 100-per-cent-modulated signal input which, when applied to a receiver through the standard 300-ohm dummy antenna and an audio voltmeter connected through a 400-Hz filter, re-

duces a total internal receiver noise and distortion to the point where the output rises 30 dB when the 400-Hz null filter is removed from the audio voltmeter circuit. This value is expressed in microvolts.

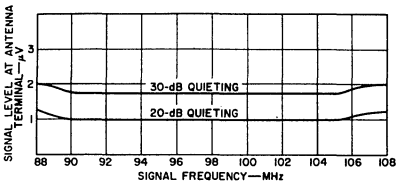



*Fig.6 - Signal level for 20- and 30-dB quieting as a function of signal frequency.*

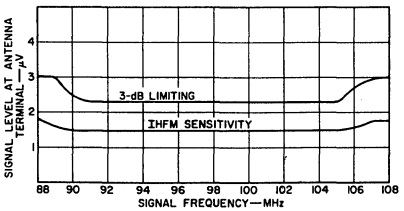



*Fig.7 - Signal level for 3-dB limiting and IHFM sensitivity as a function of signal frequency.*

Figs.8 and 9 provide additional performance characteristics. Fig.8 shows the gain and noise characteristics; Fig.9 shows the image and half-if rejection of the tuner. The spurious responses shown in Fig.9 were measured with a generator drive capability of 350-millivolts from 10.7 to 216 MHz.

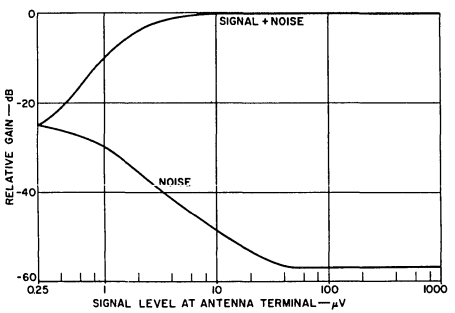



*Fig.8 - Relative gain of signal and noise as a function of the signal voltage level.*

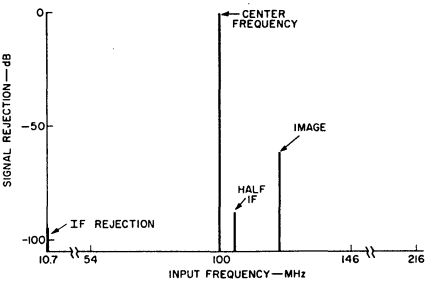



*Fig.9 - Signal rejection as a function of input frequency, measured with a generator voltage of 350 millivolts.*

MOS transistors covering a wide range of drain current were tested in the rf-amplifier and mixer sockets. Performance variations for image rejection and half-if rejection were within ± 1 dB of the values shown in Table I. Variations in sensitivity were less than 0.25 microvolt.

## Conclusions

The RCA-40468 and 40559 MOS field-effect transistors were designed into an FM tuner. Evaluation of this tuner was made in conjunction with an FM-if amplifier that used 40245 and 40246 bipolar transistors. Over-all performance of the combination showed that the capability of MOS devices for dynamic range, sensitivity, and spurious response rejection exceeds that obtained with similar FM tuners that used bipolar transistors. Experimental work indicated that performance variations as a function of product distribution were insignificant.

## APPENDIX

### Calculation of Conversion Transconductance from the Operating Characteristic

The following procedure is used to calculate the conversion transconductance of the mixer stage based on the degree of linearity of the transconductance curves of Fig.4 and the magnitude of the oscillator injection voltage. The results show that the conversion transconductance is greatest for the curve that is most linear. For the mixer circuit described in this Note, this condition occurs at a substrate bias of -3 volts.

For the curves of Fig.4, the transconductance $g_m$ is given by the following general relation:

$$g_m = f(E_g) \qquad (2)$$

where $E_g$ is the gate bias. For a substrate bias of -3 volts, and a gate bias between zero and -2.1 volts,

the corresponding curve of transconductance is expressed as follows:

$$g_m = 12.5 - 2.14\epsilon^{-0.937E_g} \quad (3)$$

For optimum mixer performance with a minimum of spurious responses, a gate voltage of -1 volt was selected as the quiescent operating point. The Taylor series expansion for Eq.(3) for a center-point operating bias $E_g$ of -1 volt is given by

$$g_m = 10.3 + 2.584\, e_g - 0.148\, e_g^2 + 0.75\, e_g^3 + \ldots \quad (4)$$

where $e_g$ is the instantaneous voltage on the gate. This instantaneous gate voltage $e_g$ can be expressed in terms of the peak oscillator signal voltage $e_o$, as follows:

$$e_g = -1 + e_o \sin \omega_o t \quad (5)$$

Substitution of Eq.(5) into Eq.(4) yields the following expression for transconductance:

$$g_m = 6.82 + 5.13\, e_o \sin \omega_o t - 2.39\, e_o^2 \sin^2 \omega_o t + 0.75\, e_o^3 \sin^3 \omega_o t \quad (6)$$

An expression for instantaneous drain current $i_d$ in terms of Eq.(6) and the incoming signal $e_s$ can then be written, as follows:

$$i_d = g_m e_s \sin \omega_s t \quad (7)$$

Expansion of Eq.(7) in terms of $e_o \sin \omega_o t$ and $e_s \sin \omega_s t$ and selection of those components which are effective at 10.7 MHz [i.e., sin $(\omega_o - \omega_s)t$ components] provides the following expression for drain current at the intermediate frequency:

$$i_{IF} = (2.57\, e_o + 0.28\, e_o) e_s \quad (8)$$

By definition, the conversion transconductance $g_c$ is equal to the if current divided by the signal voltage, as follows:

$$g_c = i_{IF}/e_s \quad (9)$$

Therefore, $g_c$ can be expressed in terms of the oscillator injection voltage $e_o$ as follows:

$$g_c = (2.57 + 0.28)e_o \quad (10)$$

Because the magnitude of oscillator injection voltage $e_o$ for the MOS FM tuner was selected to be 1 volt peak, the conversion transconductance is calculated to be

$$g_c = (2.57) + (0.28) = 2.85 \text{ mmhos}$$

By use of the same procedure, the conversion transconductance at a substrate bias of zero volts is calculated to be 2.29 millimhos. It is apparent that the application of a substrate bias provides an increase in conversion transconductance of more than 25 per cent.

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# Design of Gate-Protected MOS Field-Effect Transistors

by L.A. Jacobus and S. Reich

MOS (metal-oxide-semiconductor) field-effect transistors are in demand for rf-amplifier applications because their transfer characteristics make possible significantly better performance than that experienced with other solid-state devices. [1,2] Unless equipped with gate protection, however, MOS transistors require careful handling to prevent static discharges from rupturing the dielectric material that separates the gate from the channel. This Note describes the design of dual-gate MOS field-effect transistors that use a built-in signal-limiting diode structure to provide an effective short circuit to static discharge and limit high potential build-up across the gate insulation.

### Breakdown Mechanism

Before the techniques of gate protection can be applied, the breakdown mechanism associated with gate destruction must be understood. For the sake of simplicity in exploring the breakdown mechanism, a single-gate structure is used. Fig. 1 shows this single-gate structure (a), its electrical symbol (b), and a much simplified equivalent circuit (c) that explains the possible static discharge paths within the device. The substrate diode is formed by the p-n junction integrated over the entire junction area, i.e., the source and drain diffusions connected by the inversion layer or n-type channel. Fig. 1 (c) lumps the diffuse diode into one equivalent diode terminating at the center of the channel.

$C_{IN}$ in Fig. 1(c) represents the gate-to-channel capacitance, and $R_1$ and $R_2$ represent the channel resistance. $R_3$ is the leakage resistance associated with the substrate-to-channel equivalent diode $D_1$. Leakage resistance across $C_{IN}$ was intentionally deleted because it is more than a thousand orders of magnitude higher than $R_3$. In a typical RCA MOS field-effect transistor (e.g., 3N128), $C_{IN}$ is less than 5 picofarads. The channel resistance $R_1 + R_2$, which is a function of the applied bias, can range from $10^2$ to $10^{10}$ ohms. $R_3$ is also subject to variations determined by operating conditions, but can be assumed to be in the order of $10^9$ ohms. Thus, the application of a dc potential between the gate and any other element results in practically all of this potential being applied across $C_{IN}$.

In a dual-gate MOS field-effect transistor, the oxide thickness of the $C_{IN}$ dielectric is about 600 angstroms. The dielectric material is $SiO_2$, which has a breakdown constant of $5 \times 10^6$ volts per centimeter. The gate voltage-handling capability is therefore 30 volts. A cross-

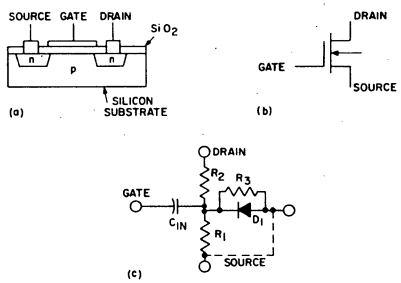



*Fig. 1 - Single-gate MOS field-effect transistor: (a) structure; (b) electrical symbol; (c) simplified equivalent circuit.*

section of a typical RCA dual-gate device is shown in Fig. 2 (a), and its schematic symbol in Fig. 2(b). The substrate in this structure is internally tied to the source; this connection is also shown schematically by the dotted line in Fig. 1(c).

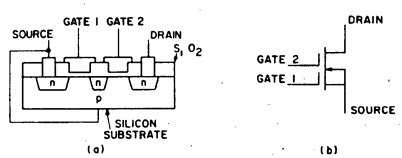



*Fig. 2 - Dual-gate MOS field-effect transistor: (a) structure; (b) electrical symbol.*

### Static Discharge

If the potential applied to an MOS transistor were entirely within the control of the circuit designer, there would be no need for gate protection. Unfortunately, designers do not have complete control of the MOS field-effect transistor environment and static potentials do accumulate. These high potentials can inadvertently be discharged through the device when it is handled

during the equipment manufacturing cycle or by a receiving antenna associated with the end product in which the transistor is used. The more severe of these conditions, in terms of percentage of units that suffer damage, is probably the initial handling phase.

Fig. 3 shows a simple equivalent circuit of a static discharge generator as it appears at the input of an MOS transistor. $E_S$ represents the static potential stored in the static generator capacitor $C_D$. This voltage must be discharged through internal generator resistance $R_S$. Laboratory experiments have determined that a human body acts as a static (storage) generator with a capacitance $C_D$ ranging from 100 to 200 picofarads and a resistance $R_S$ greater than 1000 ohms. Although there is

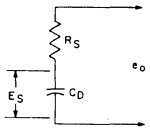



*Fig. 3 - Equivalent circuit of a static discharge generator.*

virtually no upper limit to the amount of static voltage that can be accumulated, repeated measurements suggest that the amount of potential stored is usually less than 1000 volts. Experience has also indicated that the potential from a static discharge is more severe during transistor handling than when the device is installed in a typical application. In an rf application, for example, a static potential picked up by the antenna would traverse an input circuit that normally provides a large degree of attenuation to the static surge before it appears at the input of the rf amplifier. For this reason, the development of gate-protected MOS transistors concentrated on the requirement that the devices be capable of withstanding the static discharges likely to occur during handling operations.

### Gate-Protection Methods

It has been established above that in terms of a static discharge potential it is reasonable to represent the MOS transistor as a capacitor, such as $C_{IN}$ in Fig. 4. The ideal situation in gate protection is to provide a signal-limiting configuration that allows for a signal such as that shown in Fig. 4(a) to be handled without clipping or distortion. The signal-limiting devices should limit all transient responses that exceed the gate breakdown voltage, as shown in Fig. 4(b). One possible means of securing proper limiting is to place a diode in parallel with $C_{IN}$, as shown in Fig. 4(c). Unfortunately, this arrangement causes several undesirable consequences. In terms of signal handling, the single diode clips the positive peaks of a sine wave such as that in Fig. 3(a) when the transistor is operated in the vicinity of zero bias. The 3N140 dual-gate MOS transistor, for example, is frequently operated with the rf signal superimposed on a slightly positive "bias" potential on gate No. 1. Furthermore, gate No. 2 of the 3N140 is designed to handle large positive and negative dc voltage swings from the agc loop. A single-diode arrangement would render this device useless for this type of circuit. It is important, therefore, that the limiting device be an effective open circuit to any incoming signals through the amplitude range of such signals. The best available method for accomplishing this effective open circuit is the back-to-back diode arrangement pioneered by RCA and shown in Fig. 3(d).

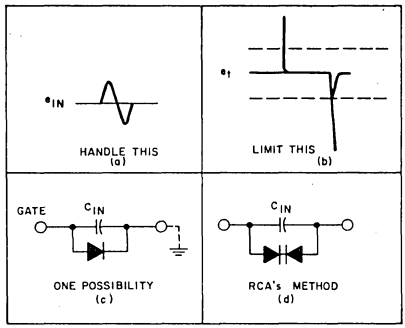



*Fig. 4 - Gate-protection requirements and two solutions.*

Ideally, the transfer characteristic of the protective signal-limiting diodes has an infinite slope at limiting, as shown in Fig. 5(a). Under these conditions, the static potential generator in Fig. 5(b) discharges through its internal impedance $R_S$ into the load represented by the signal-limiting diodes. The ideal signal-limiting diodes, with an infinite transfer slope ($R_S = 0$), would then limit the voltage presented to the gates to its knee value, $e_d$. The difference voltage $E - e_d = e_S$ (where E is the static potential in the static generator, $e_d$ is the diode voltage drop, and $e_S$ is the voltage drop across the generator internal resistance) appears as an IR drop across $R_S$, the internal impedance of the generator. The instantaneous value of the diode current is then equal to $e_S/R_S$. During handling, the practical range of this discharge varies from several milliamperes to several hundred milliamperes.

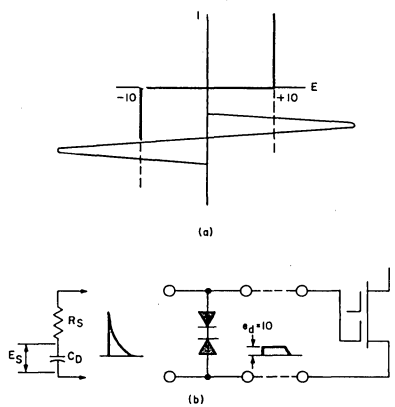



*Fig. 5 - Transfer characteristic of protective diodes (a), and resulting waveforms in equivalent circuit (b).*

### Electrical Requirements

The previous discussion points out that optimum protection is afforded to the gate with a signal-limiting diode that exhibits zero resistance (i.e., an infinite transfer slope and fast turn-on time) to all high-level transients. In addition, the diode ideally adds no capacitance or loading to the rf input circuit.

The first phase in the development of gate-protected MOS field-effect transistors was, quite naturally, their construction in hybrid form. This form was used for initial measurements because it effectively enabled the physical separation of the diodes from the MOS pellet. This separation made it possible to measure the performance of the active device apart from the combined structure and thus obtain a more precise assessment of the loading effect of the diodes. The hybrid phase has now been followed by the development of monolithic gate-protected MOS field-effect transistors such as the RCA-40673. In this transistor, the diodes are an integral part of the MOS device and are internally connected as shown in Fig. 6.

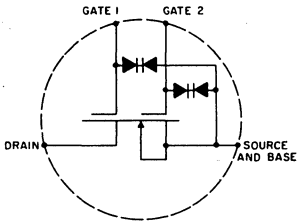



*Fig. 6 - Connection of integral protective diodes in dual-gate MOS transistor.*

### Monolithic Gate-Protected MOS Transistors

In the design of a monolithic diode-protected MOS transistor, several factors must be taken into account. (1) The high-frequency performance of the device must be comparable to that of available unprotected units. (2) The device must be designed so that no additional assembly cost is incurred. (3) The silicon area must be used efficiently to provide the maximum number of devices per semiconductor wafer. (4) The diodes must provide adequate protection against the transients experienced primarily in handling but also when the transistor is finally installed in some piece of equipment.

One approach to integrating protective diodes into an MOS transistor structure on one chip is shown in Fig. 7. In this approach, the silicon substrate required for an n-channel depletion-type MOS device is the starting material. The n-type wells are diffused into the silicon to provide pockets for the protective devices. The surface concentration and depth of these wells are carefully controlled because both of these factors are important in determining diode characteristics.

The $p^+$-type regions are diffused into the n-type wells to form the diodes and around the periphery to isolate the diode structure from the surface of the MOS device and to provide a region into which the channels may be terminated. The size of the diodes is determined by the desired current-handling capability and the amount of capacitance that can be tolerated across the gate of the MOS transistor. The spacing of the diodes is determined by the area available and the desired amount of control of transistor action from diode to diode. After the diode structures are formed, they are covered by a protective oxide. The MOS device is then fabricated by conventional means.

Fig. 8 shows a photograph of a completed monolithic diode-protected dual-gate MOS transistor. In this structure,

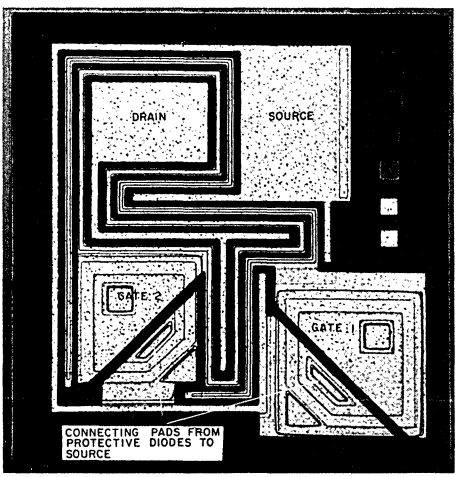



*Fig. 8 - Completed monolithic diode-protected dual-gate MOS transistor.*

one of the diodes of each pair has been located under the gate bonding pads. The small triangular metal pads

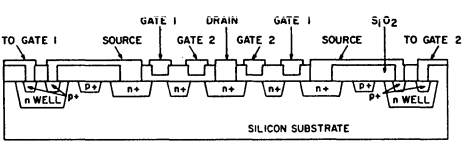



*Fig. 7 - Structure of MOS transistor chip including protective diodes.*

make contact with the second diode of each pair and connect it to the source metalization. In assembly, the source is shorted to the substrate so that a low-resistance path to ground is provided for the diodes. To ground the diodes under the second gate properly, it is necessary to break the metal of the first gate and terminate the first channel on the $p^+$-type guard band surrounding the diode structure of the second gate. This technique prevents spurious source-to-drain current which could result from the open nature of the structure.

### Current-Handling Capability

Fig. 9 shows a typical diode transfer characteristic measured with a one-microsecond pulse width at a 4 x $10^{-3}$ duty cycle. The purpose of the protective diode is to limit the amplitude of the transient to a value that is below the gate breakdown voltage. Typically, a dual-gate transistor has a gate-to-source breakdown voltage rating of 20 volts. The curves in Fig. 9 show that the transfer characteristic of the signal-limiting diodes will constrain a transient impulse to potential values well below this 20-volt limit even when the input surge is capable of delivering hundreds of milliamperes.

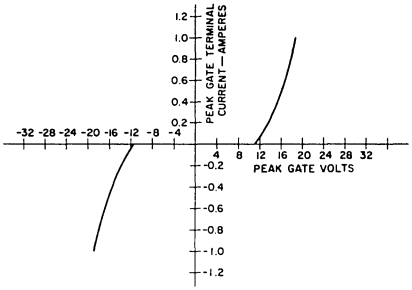



*Fig. 9 - Typical diode transfer characteristic measured with 1-microsecond pulse width at 4 x $10^{-3}$ duty cycle.*

The protection offered by the MOS signal-limiting diodes is more dramatically demonstrated when a gate-protected MOS transistor is compared to a high-frequency bipolar device. A laboratory experiment in which a static charge was accumulated in a capacitor and discharged through a circuit configuration like the one shown in Fig. 3 demonstrated that the special signal-limiting diodes made the protected-gate MOS field-effect transistor less vulnerable to static discharge damage than the bipolar transistor by a factor greater than two.

### Input Capacitance and Resistance

The curves of input capacitance and input resistance as a function of drain current in Fig. 10 represent average readings taken from ten hybrid devices with diodes first connected and then disconnected (the readings for all ten devices were remarkably close to the averages). The curves indicate that the diodes increase input capacitance by about 2.5 picofarads and decrease input resistance by about 200 ohms.

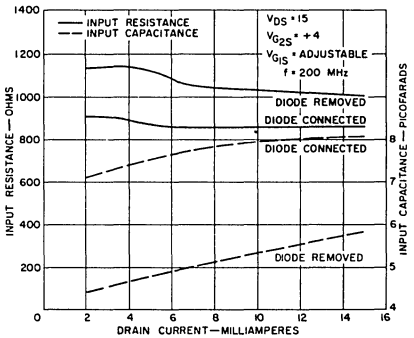


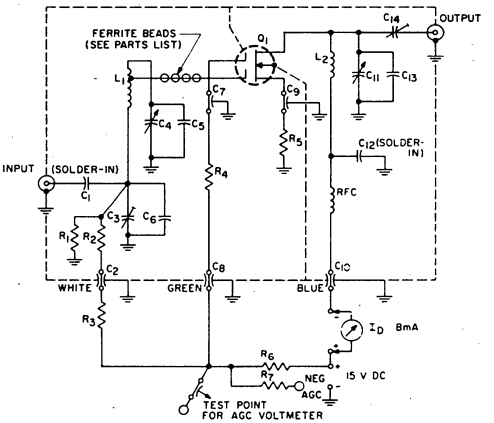

*Fig. 10 - Input resistance and capacitances as a function of drain current for hybrid structures with and without diodes.*

### Power Gain and Noise Factor

In the final analysis, the question that must be answered is how the addition of the protective signal-limiting diodes affects circuit power gain and noise factor. Performance data taken on the ten units described above in the typical rf test circuit shown in Fig. 11 are given in Table 1. Noise-factor values show an average degradation of 0.25 dB when the diodes are connected. The power-gain values show that the change in this characteristic is insignificant.

Table 1 - Power Gain and Noise Factor at 200 MHz.

| HYBRID UNIT | POWER GAIN (dB) | | NOISE FACTOR (dB) | |
|---|---|---|---|---|
| | DIODES IN | DIODES REMOVED | DIODES IN | DIODES REMOVED |
| 1 | 16.3 | 16.4 | 3.7 | 3.4 |
| 2 | 18.8 | 18.5 | 2.4 | 2.2 |
| 3 | 16.5 | 16.2 | 3.3 | 3.0 |
| 4 | 16.3 | 15.7 | 3.9 | 3.4 |
| 5 | 17.7 | 17.8 | 2.6 | 2.4 |
| 6 | 17.2 | 17.5 | 2.8 | 2.5 |
| 7 | 17.1 | 17.0 | 3.3 | 3.2 |
| 8 | 17.9 | 18.0 | 2.9 | 2.6 |
| 9 | 18.5 | 18.5 | 2.4 | 2.3 |
| 10 | 17.3 | 17.3 | 3.2 | 3.0 |




$C_1$: 100 picofarads, ceramic disc
$C_2$ $C_7$ $C_8$ $C_9$ $C_{10}$: 1000 picofarads, feed-through type
$C_3$: 1 to 10 picofarads, variable air (piston); JFD VAM-010, Johnson Co. No. 4335, or equivalent
$C_4$: 1.8 to 8.7 picofarads, variable air; Johnson Co. No. 160-104 or equivalent
$C_5$: 3 picofarads, tubular ceramic
$C_6$: 22 picofarads, ceramic disc
$C_{11}$: 1.5 to 5 picofarads, variable air; Johnson Co. No. 160-102 or equivalent
$C_{12}$: 100 picofarads, ceramic disc
$C_{13}$: 1.5 picofarads, tubular ceramic
$C_{14}$: 0.8 to 4.5 picofarads, variable air (piston); Erie 560-013 or equivalent
Ferrite beads: 4 beads on No. 24 wire between $L_1$ and socket; beads are Pyroferrio Co. "Carbonyl J" or equivalent: 0.093-inch OD, 0.03-inch ID, 0.063 inch thick
$L_1$: 4 turns 0.020-inch copper ribbon, silver-plated, 0.075 to 0.085 inch wide, 0.25-inch inside diameter, coil approximately 0.80 inch long
$L_2$: 4.5 turns 0.020-inch copper ribbon, silver-plated, 0.085 to 0.095 inch wide, 0.3125-inch inside diameter, coil approximately 0.90 inch long
$Q_1$: MOS transistor under test
RFC: Ohmite part No. Z235 or equivalent
$R_1$: 27,000 ohms
$R_2$: 47,000 ohms
$R_3$: 36,000 ohms
$R_4$: 1800 ohms
$R_5$: 275 ohms, ½ watt, 1%
$R_6$: 120,000 ohms
$R_7$: 1000 ohms

*Fig. 11 - RF test circuit for dual-gate MOS transistors.*

## Conclusions

Gate-protected dual-gate MOS field-effect transistors such as the RCA-40673 make available to the circuit designer a device capable of good rf performance without the hazards previously associated with the handling and installation of MOS devices. Moreover, the gate protection is provided by signal-limiting diodes that do not significantly compromise dynamic range, noise factor, or power gain.

## Acknowledgment

The authors thank L. Baar for collecting data and providing general support for the work described, and C. Tollin for fabricating the devices tested.

## References

1. H.M. Kleinman, "Application of Dual-Gate MOS Field-Effect Transistors in Practical Radio Receivers", IEEE TRANSACTIONS ON BROADCAST AND TV RECEIVERS, July 1967.

# Applications of the RCA CA3048 Integrated-Circuit Amplifier Array

by
L. Kaplan

The RCA CA3048 integrated circuit is an array of four identical amplifiers, each with independent inputs and outputs, all on a single monolithic silicon chip. The circuit is housed in a 16-lead dual-in-line plastic package. It has an operating and storage temperature range of -25°C to +85°C. Each amplifier in the array has a typical open-loop gain of 58 dB and input impedance of 90,000 ohms. The noise in the CA3048 is inherently very low and is tightly controlled in rigorous factory and quality-control testing.

The combination of low noise, high gain, and high input impedance make, the CA3048 a very versatile unit. and numerous applications suggest themselves for its use.

## CIRCUIT DESCRIPTION

Fig. 1 shows the complete schematic of the CA3048 integrated-circuit amplifier array. Each amplifier ($A_1$ through $A_4$) provides two stages of voltage gain.

The input stage is basically a differential amplifier with a Darlington transistor added on the one side. The output stage consists of a combination of three transistors and associated resistors connected in an inverting configuration. For example, in amplifier $A_3$, $Q_{19}$ is the Darlington input transistor, and $Q_{20}$ and $Q_{21}$ are the differential-pair transistors. The load resistor $R_{29}$ for the differential input stage is located in the collector lead of transistor $Q_{20}$. Transistors $Q_{13}$, $Q_{14}$, and $Q_{17}$ are used in the output stage. Transistor $Q_{17}$ is the actual output transistor; transistors $Q_{13}$ and $Q_{14}$ raise the input impedance of the output stage so that the loading of the 30,000-ohm source resistance $R_{29}$ (i.e., load resistor for the differential-amplifier input stage) is small. The ratio of total collector resistance to emitter resistance $[(R_{31} + R_{38})/R_{50}]$ in the output stage is 1000/200, or 5. In view of the small source loading, the stage gain, therefore, is essentially equal to 5.

A feedback network ($R_{41}$, $R_{42}$, $R_{46}$, and $D_7$) is connected between the output terminal and the base of transistor $Q_{21}$. The resistor values are chosen so that the output transistor is biased at approximately 5 milliamperes for maximum dynamic range. Diode $D_7$ compensates for variations in the base-to-emitter voltage of $Q_{21}$ with changes in temperature. Because the other transistor ($Q_{20}$) of the differential amplifier has two emitter-base junctions in series, two diodes, $D_3$ and $D_4$, are required for temperature compensation. Diodes $D_3$ and $D_4$ also provide temperature compensation for the differential-pair transistor $Q_1$ in amplifier $A_2$ (similarly diodes $D_5$ and $D_6$ are shared by amplifiers $A_1$ and $A_4$).

Diodes $D_3$ and $D_4$ and diodes $D_5$ and $D_6$ are connected to their respective inputs through a relatively stiff voltage divider (for amplifier $A_3$, the divider consists of $R_{27}$ and $R_{28}$). The input to amplifier $A_3$ is normally applied to the base of the Darlington transistor $Q_{19}$. The 100-kilohm resistor $R_{37}$ supplies bias current to this transistor. The voltage drop across resistor $R_{37}$ is small because of the very small base current of transistor $Q_{19}$.

Each amplifier of the CA3048 may be viewed as an ac operational amplifier in which a fixed resistance is permanently connected between the output and the inverting input. The built-in feedback resistor delimits the characteristics of the CA3048 amplifiers in the following ways:

1. The impedance as viewed from the noninverting input terminal consists mainly of the 100 kilohm input-bias resistance ($R_{13}$, $R_{15}$, $R_{37}$, or $R_{39}$). This resistance is shunted by the input capacitance of approximately 10 picofarads and the additional resistive loading presented by the input impedance of the Darlington input pairs. When the amplifier is operated under open-loop conditions (inverting input at ac ground), the total input impedance consists of 90 kilohms in shunt with the input capacitance. When the built-in feedback loop is allowed to function (by insertion of an unbypassed resistance in the noninverting input lead), then the loading caused by the Darlington input pairs is reduced, and the input resistance rises asymptotically towards 100 kilohms.
2. The impedance as viewed from the inverting input terminal is small (in the order of 40 to 50 ohms.)
3. When the CA3048 is used in its normal mode of operation, each amplifier in the array may be represented by the equivalent circuit shown in Fig. 2. (The capacitances shown are the sum of the device capacitances, socket capacitances, and stray capacitances.) The transconductance $G_m$, which is equal to the product of the voltage gain and the output conductance ($10^{-3}$mho), is typically 0.8 mho at midband.

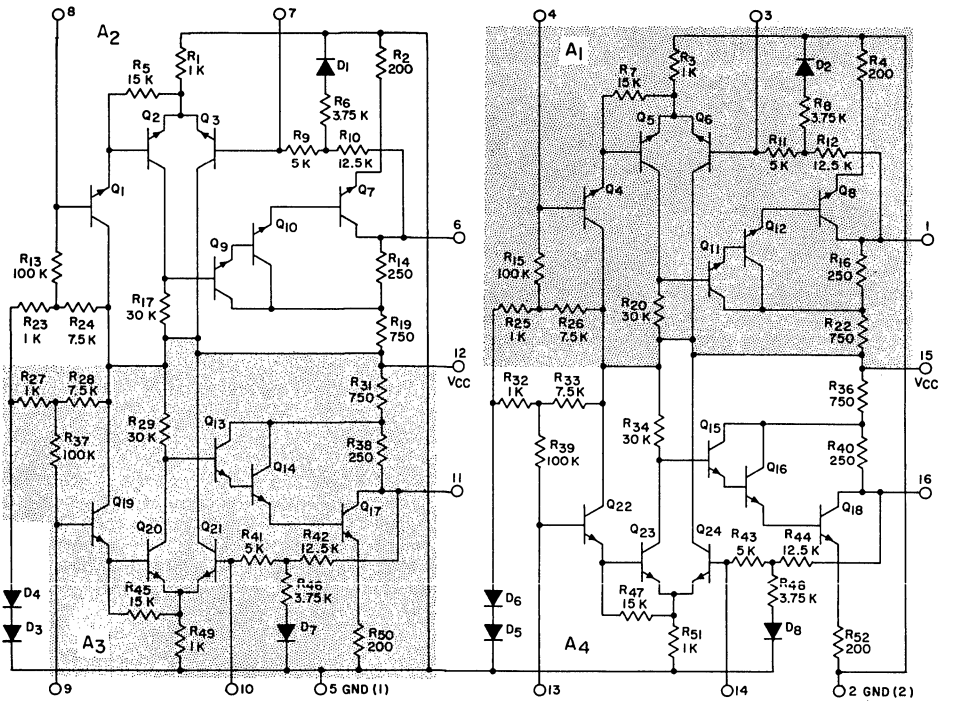



*Fig. 1 - Schematic of the CA3048 integrated-circuit amplifier array.*

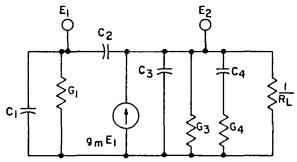



*Fig. 2 - Equivalent circuit of a CA3048 amplifier.*

## GAIN-FREQUENCY RESPONSE

Curves of the transconductance of any amplifier in the CA3048 array as a function of frequency up to 30 MHz show two break points. At frequencies above the first break point, which occurs at 300 kHz, the transconductance rolls off at a rate of 6 dB per octave to 12 MHz. At frequencies above 12 MHz, the rate of roll-off increases to 12 dB per octave. At frequencies up to 12 MHz, therefore, the transconductance of any amplifier in the CA3048 array is expressed by the following equation:

$$g_m = \frac{\omega_o g_{mo}}{\omega_o + S} \qquad (1)$$

where S is the complex frequency, $g_{mo}$ is the mid-band transconductance, and $\omega_o = 2\pi \times 300 \times 10^3$.

Fig. 3 shows the open-loop transconductance for an amplifier in the CA3048 array as a function of frequency. This response indicates potential uses of the CA3048 integrated circuit at frequencies that extend into the video range.

## STABILITY

The equivalent circuit shown in Fig. 2 can be used to determine the stability of the amplifiers in the CA3048 array under various conditions of loading when undesirable external capacitance is present in the wiring and socket. With no external generator connected to the circuit, the input conductance $G_1$ is equal to 1/100000 mho, and the output conductance $G_3$ is equal to 1/1000 mho (for amplifiers $A_1$, $A_2$, $A_3$, or $A_4$, respectively, $G_1$ is equal to $1/R_{15}$, $1/R_{13}$, $1/R_{37}$, or $1/R_{29}$, and $G_3$ is equal to $1/(R_{16} + R_{22})$, $1/(R_{14} + R_{19})$, $1/(R_{31} + R_{38})$, or $1/(R_{36} + R_{40})$. The capacitance $C_4$ and the conductance $G_4$ shown in Fig. 2 represent an external damping network which can be varied or deleted as demanded by stability or gain-bandwidth requirements.

A necessary and sufficient condition for a system to be stable is that the roots of the characteristic equation of the system have no positive real parts. The characteristic equation for the circuit of Fig. 2 is obtained by expansion of the circuit determinant and collection of the coefficients of the complex frequency S. The equation assumes the following form:

$$A_1 + A_2S + A_3S^2 + A_4S^3 + A_5S^4 = 0 \qquad (2)$$

After much tedious algebra, the coefficients are determined as follows:

$$A_1 = \omega_o G_1 G_3 G_4$$

$$A_2 = \omega_o G_4 [G_3(C_1 + C_2) + G_1(C_2 + C_3) - g_{m_o} G_2] + G_1 G_3 (C_3 \omega_o + G_4)$$

$$A_3 = \omega_o \{C_2 C_3 (G_1 + G_3 + G_4 - g_{m_o}) + C_1 [C_3(G_3 + G_4) + C_2 G_4]\} + G_4 [G_3(C_1 + C_2) + G_1(C_2 + C_3)] + G_1 G_3 C_3$$

$$A_4 = G_4 [C_1(C_2 + C_3) + C_2 C_3] + C_3 [C_1(\omega_o C_2 + G_3) + C_2(G_1 + G_3)]$$

$$A_5 = C_1 C_2 C_3 \qquad (3)$$

With the aid of a computer, it is possible to check very quickly many combinations of circuit values for stability by solving for the roots of Eq. (2) with different circuit values assigned to the various components.

Although there are many variables involved, it is possible to state in a general sense the results of several solutions of Eq. 2.

The system cannot oscillate without capacitor $C_2$ to introduce positive feedback. The analysis is reduced, therefore, to the determination of the maximum value of $C_2$ before oscillation occurs. With careful printed-circuit-board layout, the feedback capacitance $C_2$ is small, and the system is usually stable. If a socket is used the feedback capacitance is greatly increased, and

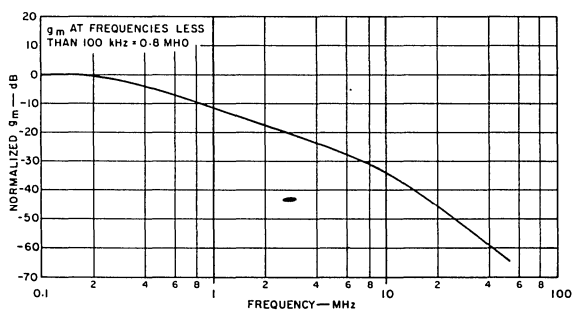


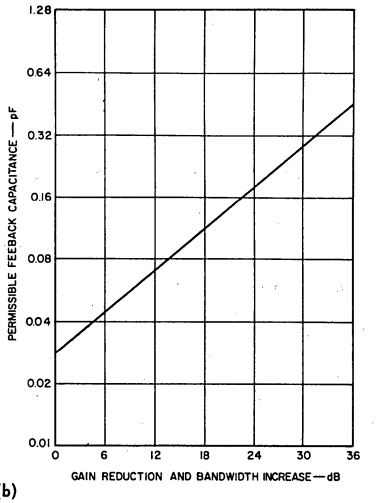

*Fig. 3 - Typical gain-frequency response for a CA3048 amplifier.*

stabilization of the circuit is generally required.

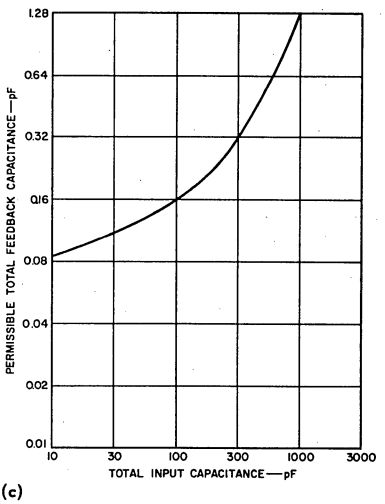
As with any two-port network, any increase in source or load conductance aids stability. In addition, analyses of Eq. (2) show that addition of shunt capacitance at the input is a very effective stability technique when the source impedance is high. Introduction of negative feedback into the circuit [which is simulated in Eq. (2) by a decrease in the value assigned to the transconductance $g_m$ and an increase in the cutoff frequency] also improves circuit stability.

Another stability method, which is effective for any source impedance or gain value, is the addition of a damping network such as that formed by capacitance $C_4$ and conductance $G_4$ in Fig. 2. In this method, the value of $C_4$ is chosen so that its reactance is equal to the parallel combination of $R_3$ and $R_L$ at the highest frequency of desired amplification. The value of $R_4$ is made small so that the gain is reduced at high frequencies and is typically 1/10 or 1/20 the value of the parallel combination of $R_3$ and $R_L$.

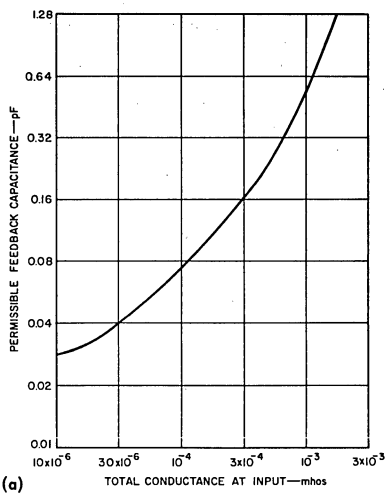
The series of curves in Fig. 4 show the results of the computation for the roots of $E_q$. (2). It should be noted that the maximum value shown for capacitance $C_2$ is that obtained just before oscillation occurs. Severe peaking of the response (or ringing) may result before the listed value of $C_2$ is reached. It is advisable, therefore, to maintain the capacitance of $C_2$ well below the indicated value.




(b)




(c)




(a)

*Fig. 4 - Stability curves for a CA3048 amplifier: (a) permissible feedback capacitance as a function of the total conductance at the input; (b) permissible feedback capacitance as a function of gain reduction and of bandwidth increase; (c) permissible feedback capacitance as a function of the total input capacitance.*

## OUTPUT SWING VS. SUPPLY VOLTAGE

Fig. 5 shows the output voltage for any one of the CA3048 amplifiers as a function of supply voltage. The solid lines represent the performance obtained with the full open-loop gain. The dotted line shows the improvement obtained when 12 dB of negative feedback is added by inclusion of a 150-ohm unbypassed resistor in the inverting-input lead. The values obtained for this curve are those which prevail when the output is loaded only by the measuring equipment. It should be realized that any substantial loading will tend to reduce the magnitude of the available output voltage for equivalent distortion figures. For example, an additional 1000-ohm load exactly balances the internal load resistor, and would reduce the available output voltage by 50 per cent.

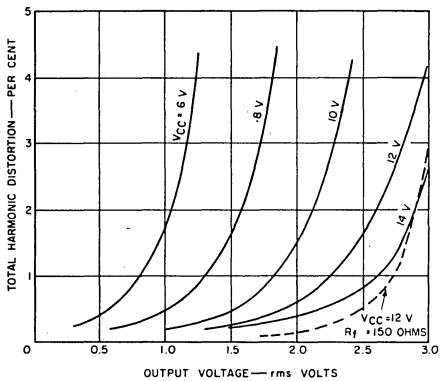



*Fig. 5 - Total harmonic distortion of a CA3048 amplifier as a function of output voltage for different value of dc supply voltage.*

## NOISE

Fig. 6 shows output noise obtained when a single amplifier of the CA3048 is operated at 40 dB gain into a "C" filter. Table I shows typical values of noise voltage ($E_{noise}$) and current ($I_{noise}$) for the CA3048 at spot frequencies of 10, 100, 1000, 10000, and 100000 Hz. From these values, the equivalent input noise voltage for any value of source resistance may be computed by use of the following equation:

$$E_{equiv} = \sqrt{(E_{noise})^2 + (I_{noise}\, R_{source})^2} \qquad (4)$$

Laboratory measurements have shown that the noise performance of the CA3048 is not significantly affected by variation of the supply voltage. The values shown in Fig. 6, therefore, may be used with supply voltages down to about 2 volts if it is remembered that the open-loop gain decreases to about 35 dB at a supply voltage of 2.5 volts.

**TABLE I**
**TYPICAL NOISE VOLTAGE AND CURRENT FOR AN AMPLIFIER IN THE CA3048 ARRAY**

| Frequency (Hz) | $E_{noise}$ (volts) | $I_{noise}$ (amperes) |
|---|---|---|
| 10 | $30.5 \times 10^{-9}$ | $7.5 \times 10^{-12}$ |
| 100 | $17 \times 10^{-9}$ | $4.3 \times 10^{-12}$ |
| 1000 | $8 \times 10^{-9}$ | $1.2 \times 10^{-12}$ |
| 10000 | $6 \times 10^{-9}$ | $0.5 \times 10^{-12}$ |
| 100000 | $4 \times 10^{-9}$ | $0.3 \times 10^{-12}$ |

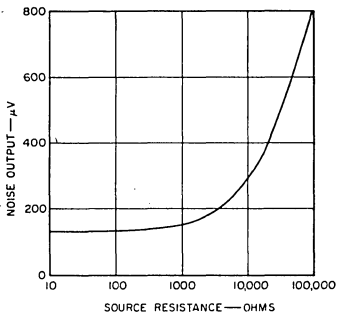



*Fig. 6 - Noise output as a function of source resistance for a CA3048 amplifier.*

## CIRCUIT APPLICATIONS

In all the foregoing discussions, a single amplifier has been described as though it existed alone. The CA3048, however, consists of four separate amplifiers, which may be used independently or in combination. A glance at the complete schematic of the CA3048 reveals other aspects worthy of consideration.

Two supply-voltage terminals and two ground terminals are indicated. Terminal No. 12 supplies the $V_{CC}$ voltage to amplifiers $A_2$ and $A_3$, and terminal No. 15 supplies the $V_{CC}$ voltage to amplifiers $A_1$ and $A_4$. The ground return for amplifiers $A_1$ and $A_4$ is provided by terminal No. 2; all other ground returns are provided by terminal No. 5.

When two units are cascaded, it is preferred to let amplifiers $A_2$ and $A_3$ be the input units, and amplifiers $A_1$ and $A_4$ be the output units. This arrangement permits separation of both the $V_{CC}$ and ground lines for low- and high-level signals.

If resistive decoupling is used, amplifiers $A_2$ and $A_3$ can be operated at lower $V_{CC}$ voltages to effect a savings in current consumption.

### Hartley Oscillator

The Hartley oscillator is easily designed and constructed using the CA3048 amplifier. No feedback capacitor is required, and it is possible to extract "square", sawtooth, or sinusoidal waveshapes.

In the circuit shown in Fig. 7, the tap on the coil is located at one-fourth the total turns, capacitors $C_1$ and $C_2$ provide dc blocking, and capacitor $C_3$ tunes with inductor $L_1$ ($\omega_o = 1/\sqrt{L_1C_3}$). When the circuit is operated from a 12-volt supply, the output voltage is a clipped sine wave that has a peak-to-peak value of about 7 volts. The voltage at the inverting input is a sawtooth that has a peak-to-peak value of about 0.300 volt. If an unclipped sine wave is desired, it is available across the coil $L_1$. A sine wave can be obtained in the single-ended connection if the value of $C_2$ is made large with respect to $C_3$ so that it effectively bypasses the sawtooth to ground; the voltage across $L_1$ is then sinusoidal with respect to ground.

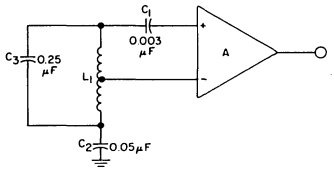



*Fig. 7 - Hartley oscillator.*

### Colpitts Oscillator

A tunable Colpitts oscillator is readily designed using one of the amplifiers of the CA3048 array. Fig. 8 shows an example of the CA3048 used in this way. Capacitors $C_1$ and $C_2$ are dc blocking capacitors; the series combination of capacitors $C_3$ and $C_4$ resonates with coil L. The ratio of $C_3$ to $C_4$ determines the relative amounts of signal fed back to the two inputs, and may be chosen on the basis of stability or strength of oscillation.

For the component values shown in Fig. 8, the frequency of oscillation is 33.536 kHz with a 12-volt supply and increases to 33.546 kHz when the supply voltage is reduced 25 per cent to 9 volts.

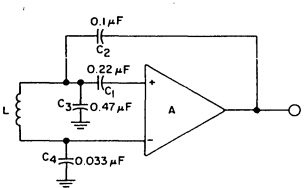



*Fig. 8 - Colpitts oscillator.*

Three waveshapes are available from the Colpitts oscillator. A sawtooth waveform is obtained at the output, a sinusoidal waveform is obtained at the inverting input, and a clipped sinusoidal waveform appears at the noninverting input.

### Astable Multivibrator

The CA3048 may be connected as an astable multivibrator with the addition of only two external components. An example of this type of operation is shown in Fig. 9.

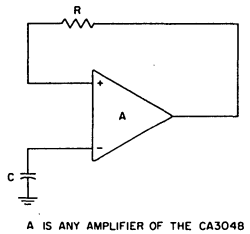



*Fig. 9 - Astable multivibrator.*

The resistor R introduces positive feedback into the circuit, and the capacitor C sets the period of the waveform. The operation of the circuit can be explained more easily if it is assumed that transistor $Q_{17}$ (of amplifier $A_3$) has just turned OFF so that the voltage at terminal No. 11 becomes very positive. This positive voltage is fed through R to the base of $Q_{19}$ to maintain the conduction of this transistor and to hold transistors $Q_{21}$, $Q_{13}$, $Q_{14}$, and $Q_{17}$ cut off. Meanwhile, capacitor C charges through the internal bias resistors $R_{41}$ and $R_{42}$. When the voltage on capacitor C reaches the level at which transistor $Q_{21}$ begins to become forward-biased, some current is diverted from $Q_{20}$ to $Q_{21}$ and $Q_{13}$, $Q_{14}$, and $Q_{17}$ begin to turn ON. The action is regenerative because the negative-going voltage from the collector of $Q_{17}$ feeds a negative-going signal back to the base of $Q_{19}$ to enhance the switching action. When C discharges to the point at which $Q_{21}$ turns OFF, $Q_{20}$ begins to turn ON and the process repeats itself.

Two waveforms are available from the astable multivibrator circuit, both at low impedance. A rectangular waveform that has a peak-to-peak amplitude of 7 volts or greater is obtained from the output terminal. The waveform available at the inverting input is an isosceles triange that has a peak-to-peak amplitude of approximately 0.220 volt.

With the circuit as shown, reliable oscillation is obtained for values of the resistor R in the order of 2.2 megohms, with supply voltages as low as six volts.

### 4-Channel Linear Mixer

Fig. 10 illustrates the use of the CA3048 as a linear mixer. Each input is connected to its own CA3048

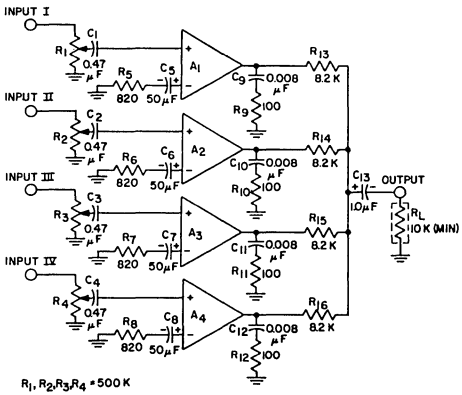



*Fig. 10 - Linear mixer.*

amplifier through the gain-control potentiometers $R_1$, $R_2$, $R_3$, and $R_4$. Capacitors $C_1$, $C_2$, $C_3$, and $C_4$ block the dc voltage at the inputs.

The gain of any input to the corresponding output is 20 dB for the circuit values shown and a load impedance of 10000 ohms or greater. Resistors $R_5$, $R_6$, $R_7$, and $R_8$ program the gain of the system, and may be varied to provide more or less gain, depending on the requirements of the application. The curve in Fig. 11 illustrates the effect of variation in the resistance in the feedback circuit of the CA3048. The difference in the 20 dB gain indicated for the mixer circuit and the approximately 34 dB shown in Fig. 12 results from the loss in the combining circuit that consists of $R_{13}$, $R_{14}$, $R_{15}$, $R_6$, and $R_L$.

A resistor-capacitor combination ($R_9$, $C_9$, $R_{10}$, $C_{10}$, $R_{11}$, $C_{11}$, $R_{12}$, $C_{12}$) connected to the output of each amplifier stabilizes the amplifiers when source and load conductances are too small to provide adequate damping.

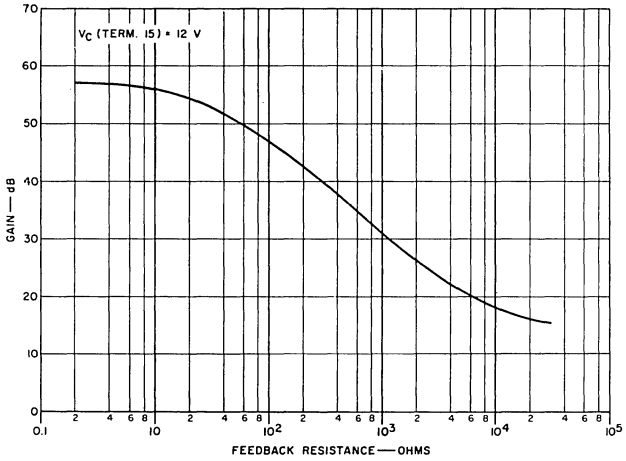



*Fig. 11 - Gain of a CA3048 amplifier as a function of feedback resistance.*

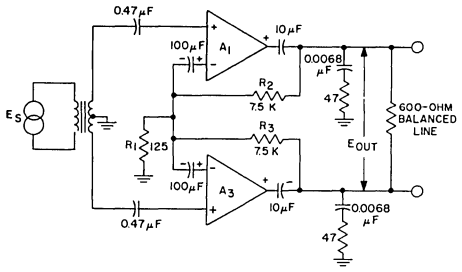



*Fig. 12 - Balanced-line driver.*

The input impedance of each amplifier of the CA-3048 is nominally 90 kilohms. In the linear mixer, however, the input potentiometers $R_1$ through $R_4$ are 500 kilohms. The effective impedance presented to the device, therefore, is quite high except when the circuit is adjusted for maximum gain. At this time, the impedance decreases to about 75 kilohms.

### Driver for 600-ohm Balanced Line

Two amplifiers of the CA3048 may be connected to drive a 600-ohm balanced line at levels up to 1 volt rms with a gain of 40 dB. When the circuit is connected as shown in Fig. 12, the distortion is less than 1 per cent at an output level of 1 volt and a gain of 40 dB.

The output of the circuit is limited to a value slightly greater than 1 volt rms, primarily because of drive-current limitations to the output transistors. In this respect, it is self-protecting. Should a short circuit develop across the line, the circuit will not destroy itself.

Resistor $R_1$ in Fig. 12 is common to the output and input circuits of both amplifiers $A_1$ and $A_3$. Should a gain unbalance exist, or should the input signals be of unequal amplitude, then the outputs would tend to become unbalanced with respect to ground. For example, if amplifier $A_1$ had the larger output, a signal in phase with the output at $A_1$ would be developed across resistor $R_1$. In this event, the voltage developed at $R_1$ would tend to reduce the output of amplifier $A_1$ because this voltage is applied to the inverting input. At the same time, the voltage at $R_1$ is applied to the inverting input of amplifier $A_3$ and tends to increase the effective input voltage of that amplifier and, in this way, help to restore balance. The balancing effect takes place regardless of the cause of the initial unbalance.

### Gain-Controlled Amplifier

Any amplifier of the CA3048 may be used as a gain-controlled amplifier in order to accommodate a wide range of input signal amplitude. Fig. 13 shows one amplifier of the CA3048 used in this type of configuration. By variation of the dc potential at the gate No. 1 of the MOS transistor $Q_1$, the gain of the amplifier may be varied from 14 dB to 49 dB. In this circuit, the MOS transistor $Q_1$ acts as a variable impedance in the feedback loop of the CA3048.

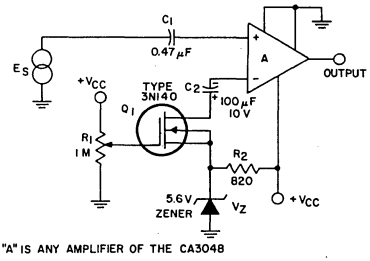



*Fig. 13 - Gain-controlled amplifier.*

In a circuit such as that shown in Fig. 13, the voltage gain may be expressed as follows:

$$\frac{E_o}{E_s} = \frac{A\,(R_a + R_f)}{R_f + R_a(A + 1)} \qquad (5)$$

where $R_a$ is the equivalent resistance of the MOS transistor and $R_f$ is the feedback resistance, which includes the internal feedback resistance of the integrated circuit together with any paralleled external feedback resistance.

As the value of resistor $R_a$ approaches zero, the gain of the circuit approaches the open-loop gain of the amplifier (A). For very large values of resistor $R_a$ the gain of the circuit approaches A/(A + 1), or approximately unity. The maximum theoretical agc range then is A.

The practical agc range of this circuit is limited on the high end by the "ON" resistance of the MOS transistor, and on the low end by the finite input impedance of the CA3048. In the circuit shown in Fig. 13, the range of control is 35 dB.

There is no necessity for direct current to flow in the MOS transistor, and if a low impedance source of about five volts is available, this voltage may be substituted for the Zener diode-resistor combination so that the power requirements of the circuit are further reduced.

Distortion, which is inherently low, ranges from 0.65 per cent at minimum gain (output of 2 volts rms) to 0.4 per cent at maximum gain.

RCA
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# MOS Field-Effect Transistors

## Application Note AN-4125

# MOS/FET Biasing Techniques

by S. Reich

A wide variety of applications exist for field-effect transistors today including rf amplifiers and mixers, i-f and audio amplifiers, electrometer and memory circuits, attenuators, and switching circuits.

Several different FET structures have also evolved. The dual-gate metal-oxide-semiconductor FET, for example, appears particularly advantageous in rf stages because of low feedback capacitance, high transconductance and superior cross modulation with automatic-gain-control capability.

The rules for biasing FETs vary slightly depending upon the type of FET being applied. But we'll attempt to cover most of the possibilities by looking at several typical examples.

As you know, all FETs including junction devices, can be classified as depletion or enhancement types, depending upon the conductivity state of the channel at zero gate-to-source voltage or bias. In a depletion type, charge carriers are present and the channel is conductive when no bias is applied to the gate. Reverse bias depletes this charge and reduces channel conductivity; forward bias draws more charge carriers into the channel and increases conductivity. In an enhancement type, no useful channel conductivity exists at either zero or reverse gate bias; the gate must be forward-biased to produce active carriers and permit conduction through the channel.

Test circuits which can be used to measure the zero-bias drain current $I_{DSS}$ of junction-gate and insulated-gate field-effect transistors are shown in Fig. 1. The junction-gate device, shown in Fig. 1(a), is always a depletion type and thus exhibits a reading for $I_{DSS}$. Insulated-gate or MOS devices may be either depletion or enhancement types; depletion types exhibit reasonable $I_{DSS}$ readings in the circuit of Fig. 1(b), while enhancement types are cut off. The transistor symbol shown in Fig. 1(b) uses a solid channel line to indicate the "normally ON" channel of a depletion type. An enhancement type is represented by an interrupted channel line, that indicates the "normally OFF" channel.

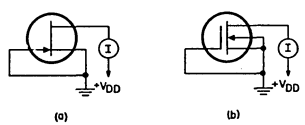



Fig. 1. $I_{DSS}$ test circuits for (a) junction-gate and (b) insulated-gate field-effect transistors.

Although enhancement types are always operated (activated) in the enhancement mode (because application of reverse bias would simply cut the device off), depletion types can operate in either mode. Junction-gate devices can operate in the enhancement mode only within a very limited range because gate voltages exceeding 0.3 V also forward-bias the gate-to-source input diode and load the signal source. However, MOS depletion devices can operate in either the enhancement or the depletion mode without the constraints associated with input-diode loading.

The field-effect transistors shown in Fig. 1 are single-channel, single-gate, or triode-type devices. Although it is possible that the substrate of either the junction-gate or insulated-gate transistor may be used as a separate control element, in most circuits it is adequate as a control element and is extrinsically connected to the source or operated at a fixed potential.

When two separate control elements are required in a circuit, a dual-gate MOS transistor such as that shown in Fig. 2 is usually used. In this type of device, two independent gate electrodes that control individual channels are serially interconnected. In newer dual-gate MOS transistors, gate protection is provided by intrinsic back-to-back diodes, as shown in Fig. 2(b). The substrate in this type of device is in-

ternally connected to the source.

***Biasing a single-gate MOS transistor***

The bias circuit for a single-gate MOS transistor may take three forms, as shown in Fig. 3: (a) self-bias, (b) an external supply, or (c) a combination of the two. The design of a self-bias circuit is fairly straightforward. For example, if it is desired to operate a 3N128 MOS transistor (an n-channel, depletion device) with a drain-to-source $V_{DS}$ voltage of 15 V and a

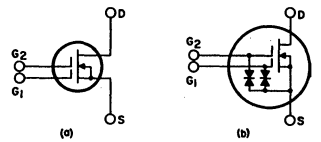



Fig. 2. Dual-gate MOS transistors. (a) conventional symbol, (b) modified symbol to show gate-protected device.

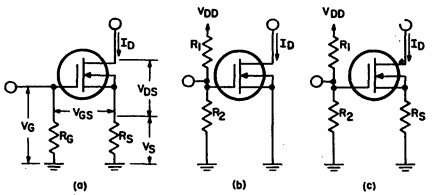



Fig. 3. Biasing circuits for single-gate transistors: (a) self-biasing; (b) external biasing; (c) a combination of self-biasing and external biasing.

small-signal transconductance $g_{fs}$ of 7.4 mmhos, the drain current $I_D$ required for the desired transconductance is first obtained from published transfer-characteristics curves such as those shown in Fig. 4(a). A published curve such as the one shown in Fig. 4(b) is then used to determine the gate-to-source voltage $V_{GS}$ required for the desired value of $I_D$. The circuit parameters can then be calculated using $V_{DS} =$ 15 V, $I_D = 5$ mA, $V_{GS} = -1.1$ V and $V_G = 0$.

$$V_S = V_G - V_{GS} = 1.1 \text{ V} \quad (1)$$

$$R_S = V_S/I_D = 1.1/5 = 220\ \Omega \quad (2)$$

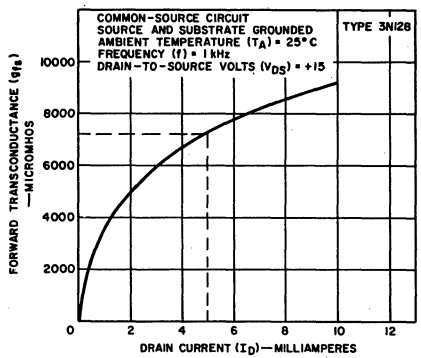
$$V_{DD} = V_{DS} + V_S = 15 + 1.1 = 16.1 \text{ V} \quad (3)$$

In a circuit designed for applied bias only, the problem becomes more complicated. For example, the voltage divider consisting of $R_1$ and $R_2$ in Fig. 3(b) may be required to apply a $V_{GS}$ of $-1.1$ V. In addition to the fact that a negative supply is required, a more serious problem exists. The bias-voltage computations shown above were based on the solid-line curve shown in Fig. 4(b) for a typical device.

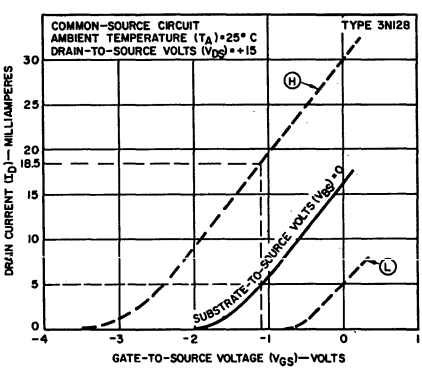
However, the drain currents for individual devices may cover a wide range of values, as indicated by the dashed curves H and L representing high- and low-limit devices, respectively. With a fixed-bias supply of $-1.1$ V, therefore, drain current could range from cutoff to 18.5 mA. Some form of dc feedback is obviously desirable to maintain the drain current constant over the normal range of product variation.

The combination bias method shown in Fig. 3(c) makes use of a larger value of $R_S$ to narrow the range of drain current to plus or minus a few milliamperes. Figure 5 shows curves of $I_{DSS}$ as a function of $I_D$ for various values of $R_S$. The normal range of $I_{DSS}$ for the 3N128 is from 5 to 25 mA, or a spread of 20 mA. The use of the 220-Ω source resistor $R_S$ calculated in the previous example reduces this spread to about 5 mA, for a 4-to-1 improvement. Higher values of $R_S$ achieve tighter control of the spread of drain-current values.

As an example, the circuit of Fig. 3(c) may




(a)




(b)

Fig. 4. (a) Transfer and (b) operating characteristics of the 3N128 single-gate MOS transistor.

be required to maintain drain current constant within ±1 mA for the same conditions given in the previous example. Figure 5 shows that a value of $R_S$ equal to or greater than 1000 Ω will satisfy the required drain-current tolerance. However, a quiescent current of 5 mA through a source resistor of 1000 Ω produces a $V_{GS}$ value of −5 V, which is incompatible with a drain current of 5 mA. Therefore, an applied bias must be used in conjunction with the self-bias. The circuit parameters for Fig. 3(c) are then calculated using $V_{DS} = 15$ V, $I_D = 5$ mA, $V_{GS} = -1.1$ V, and $R_S = 1000$ Ω.

$$V_S = I_D R_S = (0.005)\ (1000) = 5 \text{ V} \quad (4)$$

$$V_G = V_{GS} + V_S = -1.1 + 5 = 3.9 \text{ V} \quad (5)$$

$$V_{DD} = V_{DS} + V_S = 15 + 5 = 20 \text{ V} \quad (6)$$

$$\frac{V_{DD}}{V_G} = \frac{R_1 + R_2}{R_2} = \frac{20}{3.9} = 5.12 \quad (7)$$

The lower limits of $R_1$ and $R_2$ are established by determining the maximum permissible loading of the input circuit and setting this value equal to the parallel combination of the two resistors. For example, if the total shunting of the input circuit is to be no less than 50,000 Ω, $R_1$ and $R_2$ are calculated as follows:

$$\frac{R_1 R_2}{R_1 + R_2} = 50{,}000 \quad (8)$$

$$\frac{R_1 + R_2}{R_2} = 5.12 \quad (9)$$

$R_1 = 256{,}000$ Ω, and $R_2 = 62{,}000$ Ω.

In practice, the effects of input-circuit loading can frequently be eliminated by the use of the circuit arrangement shown in Fig. 5.

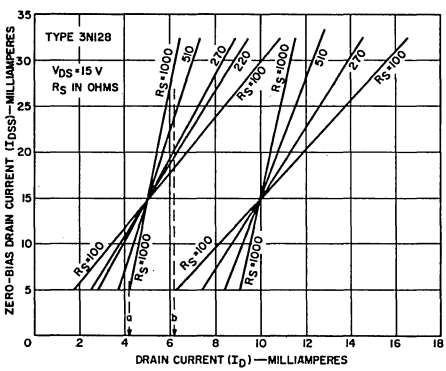



Fig. 5. Zero-bias drain current $I_{DSS}$ as a function of drain current $I_D$ for various values of source resistance $R_S$ in a 3N128 single-gate MOS transistor.

The upper limits of $R_1$ and $R_2$ are usually determined by practical consideration of the resistor component values because the absolute values of gate-leakage current $I_{GSS}$ are extremely small. In unique applications where $I_{GSS}$ is a significant factor, a maximum value for the parallel combination of $R_1$ and $R_2$ can be determined by dividing the total permissible change in voltage $V_G$ across the combination by the maximum allowable value of $I_{GSS}$ at the expected operating temperature, as determined from the published data for the transistor used.

Because $I_{GSS}$ consists of leakage currents from both drain and source, and these currents are usually measured with a maximum-rated voltage stress on the gate with respect to all other elements, the published value of $I_{GSS}$ is generally much higher than that which could be expected under typical circuit conditions. As a result, the values of $R_1$ and $R_2$ determined in this manner are conservative.

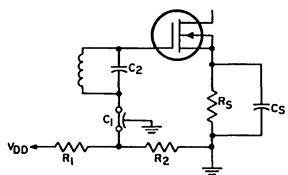



Fig. 6. Circuit used to eliminate input-circuit loading.

***Substrate biasing***

As mentioned previously, many single-gate FETs incorporate provisions for separate connection to the substrate because it is sometimes desirable to apply a separate bias to the substrate and use it as an additional control element. A simple arrangement for achieving this bias is shown in Fig. 7(a). In this circuit, the substrate bias $V_{US}$ is equal to $I_D\ (R_1 + R_2)$ and the gate bias $V_{GS}$ is equal to $I_D R_1$.

One application in which substrate bias is mandatory is the attenuator circuit shown in Fig. 7(b). An MOS transistor is extremely useful as an attenuation device because it acts as a fairly linear resistance whose intrinsic conductivity can be drastically changed by means of a dc voltage applied to the gate. In the circuit of Fig. 7(b), for example, a signal applied

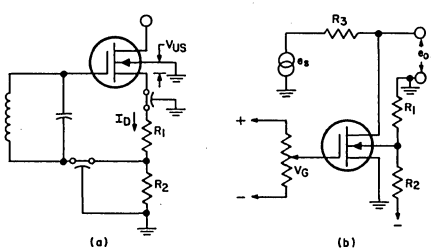



Fig. 7. Substrate biasing circuits.

to the drain can be attenuated by application of a positive voltage to the MOS transistor gate. The attenuation $A_V$ obtained is given by

$$A_V = \frac{R_D}{R_D + R_s} \quad (10)$$

where $R_D$, the device channel resistance, is a function of bias voltage and can be varied from approximately 100 Ω to $10^5$ MΩ. Because of the construction of the MOS transistor, however, the drain must always be positive with respect to the substrate so that the drain-to-source diode (diffusion) will not be biased into conduction. Therefore, the substrate must be back-biased to at least the peak value of the negative-going signal that might be applied to the drain. Figure 7(b) shows how this back-bias is obtained.

#### Biasing a junction-gate transistor

The biasing techniques that have been described for single-gate MOS transistors are directly applicable to junction-gate devices with one exception. Because the input gate of a junction-gate field-effect transistor consists of a back-biased diode, the device must always be biased so that the input-gate diode is not in conduction. Effectively, therefore, a junction-gate device will almost always be operated in the depletion mode.

Although the biasing considerations covered thus far are applicable to all types of single-gate transistors, it should be remembered that enhancement-type devices must be turned on before they can be used as amplifiers. Therefore, applied bias such as shown in Fig. 3(b) and 3(c) must always be used with these devices. In addition, it is desirable to narrow the range of drain current by means of a source resistor, such as that shown in Fig. 3(c), that produces self-bias after the transistor is turned on.

As an example of this type of biasing, it may be assumed that a 2N4065 p-channel enchancement-type MOS transistor is to be operated at room temperature with a supply voltage of 19 V, a source resistance of 1000 Ω, and a drain current of 1 mA, as shown in Fig. 8. To complete the bias circuit, it is necessary to determine the values of $R_1$ and $R_2$ to satisfy a total input-loading requirement of 10,000 Ω.

The 2N4065 transistor has a typical threshold voltage of −5.3 V and requires a gate voltage of approximately −9.2 V for a drain current of 1 mA. (The threshold voltage $V_{TH}$ for an enhancement-type device is comparable to the cut-off voltage $V_{GS}$ (OFF) for a depletion-type device, and is the value of gate voltage required to initiate drain current. It is usually specified for a drain-current value between 10 and 100 mA). Circuit parameters for the network of Fig. 8 are then calculated as follows:

$$V_S = I_S R_S \doteq (-0.001)(1000) = -1 \text{ V} \quad (11)$$

$$V_{DS} = V_{DD} - V_S = -19 + 1 = -18 \text{ V} \quad (12)$$

$$V_G = V_{GS} + V_S = -9.2 - 1 = -10.2 \text{ V} \quad (13)$$

$$\frac{R_1 + R_2}{R_2} = \frac{V_{DD}}{V_G} = \frac{19}{10.2} = 1.86 \quad (14)$$

$$\frac{R_1 R_2}{R_1 + R_2} = 10{,}000\ \Omega \quad (15)$$

$$R_1 = 18{,}600\ \Omega \quad (16)$$

$$R_2 = 21{,}500\ \Omega \quad (17)$$

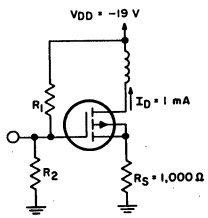



Fig. 8. Biasing circuit for an enhancement-type MOS transistor.

#### Biasing the dual-gate MOS transistor

A dual-gate MOS transistor such as that shown in Fig. 9(a) is actually a combination of two single-gate MOS transistors arranged in a cascode configuration, as depicted in Fig. 9 (b). The element voltages associated with each of the individual transistors can be analyzed as follows:

$$V_{DS} = V_{DS1} + V_{DS2} \quad (18)$$

$$V_{GS2} = V_{DS1} + V_{GS2} \quad (19)$$

$$V_{G1S} = V_{GS1} \quad (20)$$

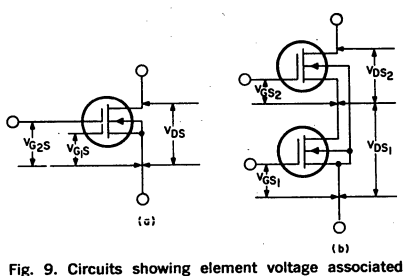



Fig. 9. Circuits showing element voltage associated with MOS dual-gate transistors.

Curves of the voltage distributions for the 3N140 dual-gate MOS transistor are shown in Fig. 10. It can be seen for an applied gate-No. 1-to-source voltage $V_{G1S}$ of zero, a supply voltage $V_{DD}$ of +15 V and a gate-No. 2-to-source volt-

age $V_{G2S}$ of + 3 V ,the actual drain voltage across the grounded-source unit is approximately +2.75 V and gate No. 2 is 0.25 V positive with respect to its own source. These curves explain the logic behind the apparently high positive gate-No. 2 voltages (in the order of +4 V) recommended for typical operation of dual-gate MOS transistors.

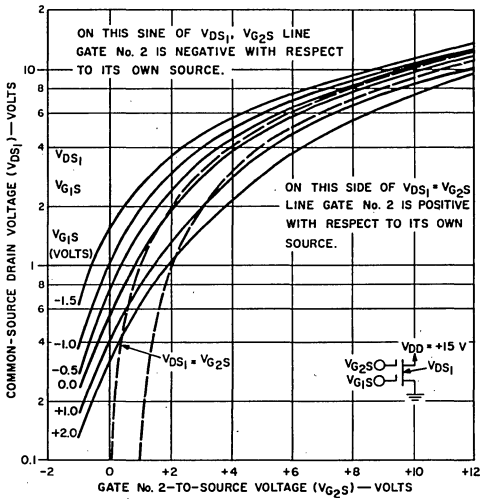



Fig. 10. Voltage distributions for the 3N140 dual-gate MOS transistor.

Operating curves for the 3N140 are shown in Fig. 11. These curves can be used to establish a quiescent operating condition for the transistor. For example, a typical application may require the 3N140 to be operated at a drain-to-source voltage $V_{DS}$ of 15 V and a transconductance $g_{fs}$ of 10.5 mmhos. As shown in Fig. 11(a), the desired value of $g_{fs}$ can be obtained with a gate-No. 2-to-source voltage $V_{G2S}$ of +4 V and a gate-No. 1-to-source voltage $V_{G1S}$ of −0.45 V. From Fig. 11(b), the drain current compatible with these gate voltages is 10 mA.

Two biasing arrangements which can be used to provide these operating conditions for the 3N140 are shown in Fig. 12. For the application mentioned above, it may be assumed that shunt resistance for gate No. 1 should be 25,000 Ω and the dc potential on gate No. 2 should be fixed and at rf ground. The remaining parameters for the biasing circuits can then be obtained from the curves showing $I_D$ as a function of $R_S$ in Fig. 13, with $R_S = 270$ Ω:

$$V_S = I_D R_S = +2.7 \text{ V} \quad (21)$$
$$V_{G1} = V_{G1S} + V_S = +2.25 \text{ V} \quad (22)$$
$$V_{G2} = V_{G2S} + V_S = +6.7 \text{ V} \quad (23)$$
$$V_{DD} = V_{DS} + V_S = +17.7 \text{ V} \quad (24)$$

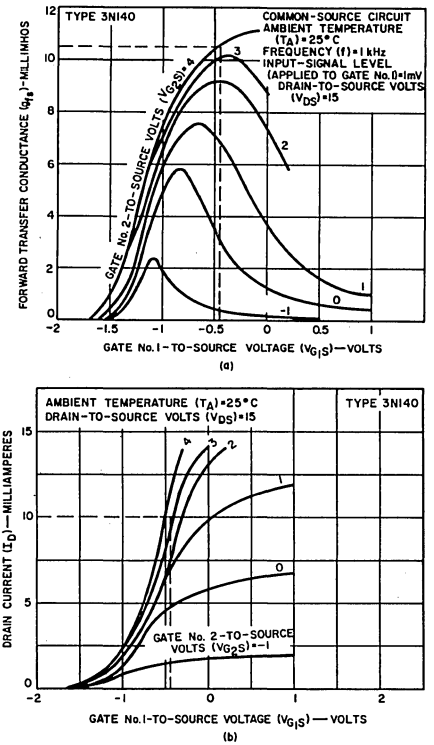



Fig. 11. Characteristics curves for the 3N140.

The values of the resistance voltage dividers required to provide the appropriate gate voltages are determined in the same manner as shown previously for single-gate transistors. For the circuit of Fig. 12(a), $R_2$ is 197,000 Ω, $R_4$ is 28,600 Ω, and $R_1$ $R_2 = 11/6.7$.

The circuit of Fig. 12(a) is normally used in rf-mixer applications and in rf-amplifier circuits which do not use agc. The circuit of Fig. 12(b) is recommended for the application of agc volt-

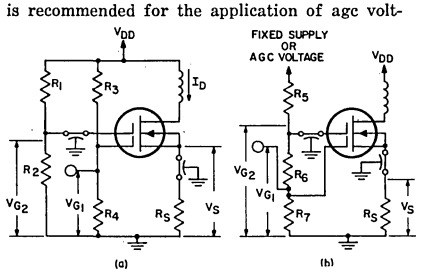



Fig. 12. Typical biasing circuits for the 3N140.

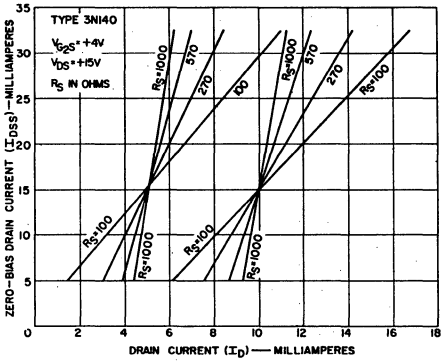



Fig. 13. Drain-current curves for various values of $R_S$ for the 3N140.

age to rf-amplifier stages. In this circuit, the rf signal is applied to gate No. 1, and the agc voltage to gate No. 2.

The dual-gate MOS transistor is useful in agc-supplied rf amplifiers because almost no agc power is required by the device as a result of the high dc input resistance indigenous to the MOS transistor. Another advantage provided by the MOS transistor is revealed by the ease with which it obtains delayed agc action and good cross-modulation characteristics as a function of agc. The application of agc bias to gate No. 2 while the bias on gate No, 1 is changed improves the cross-modulation characteristics of the transistor as a function of agc applied.

***Biasing to compensate for temperature variations***

Unlike bipolar transistors, MOS transistors exhibit a negative temperature coefficient for typical values of drain current. That is, drain current and dissipation decrease as temperature increases, and there is no possibility of $I_D$ runaway with elevated temperature. Unfortunately, transconductance and rf power gain also decrease as temperature increases. Figure 14 shows curves of drain current and transconductance as a function of temperature. These curves also show the compensating effects produced by the use of source resistance $R_S$; variations in drain current are reduced significantly by use of an $R_S$ value of 1000 Ω.

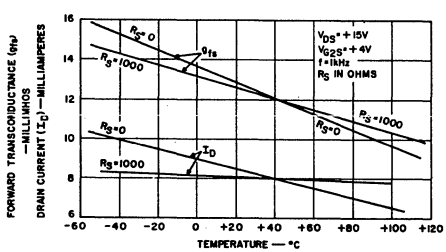



Fig. 14. Drain current and transconductance as a function of temperature for the 3N140.

Variations in transconductance can be virtually eliminated by application of a gain-control voltage from a temperature-dependent voltage-divider network to gate No. 2. For example, the values of the resistance voltage dividers in the circuit of Fig. 12(a) were determined to provide a transconductance of 9.5 mmhos at ambient temperature, and the device temperature was then varied through the range of −45 to +100°C. The values of gate-No. 2-to-source voltage $V_{GSS}$ required to maintain a constant transconductance over the entire temperature range, for $R_S$ values of zero and 1000 Ω are shown in Fig. 15.

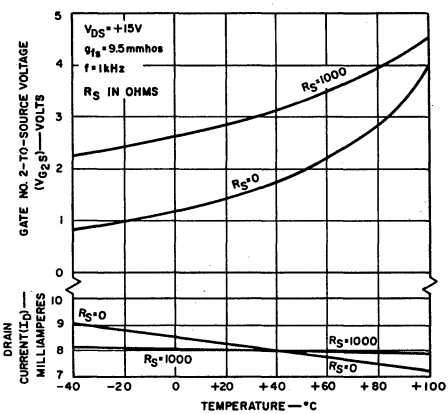



Fig. 15. Drain current and gate-No. 2-to-source voltage for constant $I_D$ as a function of temperature for the circuit of Fig. 14 (b).

In a practical circuit, the required voltages can be applied to gate No. 2 if $R_1$, or the combination of $R_1$ and $R_2$, is a temperature-sensitive resistor that is thermally linked to the MOS transistor package. This thermistor network can be designed to provide a desired voltage characteristic at gate No. 2 either to keep the transconductance constant or to permit some variation with temperature to compensate for changes in other stages. The effects of temperature given in percentages on these other stages may be summarized as follows: $R_{in}$—one percent; $C_{in}$—one percent; $C_{feedback}$—one percent; $R_{out}$—plus 45 percent; $C_{out}$—one percent.

The data was measured on a 3N140 MOS transistor in the circuit of Fig. 12(a). Drain current was 8 mA, frequency was 200 MHz, and the temperature varied from 0 to 100°C.

***Summary***

All field-effect transistors may be biased similarly. Uniform quiescent operating points can be easily achieved in MOS field-effect transistors by employing circuit designs that incorporate a source resistance. For a given $I_{DSS}$ range, the value of the source resistance inversely affects the in-circuit $I_D$ spread. An increase in the value of the source resistance minimizes variations in $I_D$ as a function of temperature. The dual-gate MOS field-effect transistor is ideally suited for use in gain-controlled stages; dual-gate transistor biasing can provide various types of agc action including temperature compensation to assure constant output.

***Acknowledgements***

The author thanks L.A. Jacobus and W.A. Harris for the computations and computer run-off for the curves shown in Fig. 10, and R. Miller for collecting much of the data shown.

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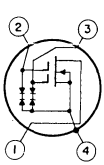
# RF Applications of the Dual-Gate MOS/FET up to 500 MHz

by L. S. Baar

The RCA dual-gate protected, metal-oxide silicon, field-effect transistor (MOS FET) is especially useful for high-frequency applications in RF amplifier circuits. The dual-gate feature permits the design of simple AGC circuitry requiring very low power. The integrated diodes protect the gates against damage due to static discharge that may develop during handling and usage. This Note describes the use of the RCA-3N200 dual-gate MOS FET in RF applications. The 3N200 has good power gain and a low noise factor at frequencies up to 500 MHz, offers especially good cross-modulation performance, and has a wide dynamic range; its low-feedback capacitance provides stable performance without neutralization.

### Gate-Protection Diodes

Fig. 1 shows the terminal diagram for the 3N200. Gate No. 1 is the input signal electrode and Gate No. 2 is normally used to obtain gain control. The back-to-back diodes are connected from each of the gates to the source terminal, lead No. 4. If short duration pulses greater than ±10 volts, generated for example by static discharge, are inadvertently applied to either gate, the protective diodes limit these voltages and shunt the current to the source terminal. Thus the gates, under normal operating conditions, are protected against the effects of overload voltages.[1]




LEAD 1 - DRAIN
LEAD 2 - GATE NO. 2
LEAD 3 - GATE NO. 1
LEAD 4 - SOURCE, SUBSTRATE, AND CASE

*Fig. 1 – Terminal diagram for the 3N200.*

### Operating Conditions

Typical two-port characteristics at 400 MHz including both "y" and "s" parameters, are given for the 3N200 in the RCA technical bulletin, File No. 437. This note makes use of the "y" parameters; however, designers who prefer the alternate method can, by parallel analysis, make use of the "s" parameters.

A recommended operating drain current ($I_D$) for the 3N200 is approximately 10 milliamperes with Gate No. 2 sufficiently forward biased such that a change in the bias voltage does not greatly affect the drain current. An adequate Gate No. 2-to-source voltage ($V_{G2S}$) is approximately +4 volts. The forward transadmittance ($y_{fs}$) increases with drain current, but saturates at higher current levels. The increase in RF performance at drain currents above 10 milliamperes is achieved only with less efficient use of input power.

To establish the optimum operating conditions for a type, consideration must be given to the range of variations in characteristics values encountered in production quantities of the type.[2] One important measure of type variation is the range of zero bias drain current ($I_{DS}$). The current range given in the 3N200 technical bulletin for $I_{DS}$ is from 0.5 mA to 12 mA. A fixed bias condition intended to center the range of drain current at the desired level, still will produce an operating drain current range of 11.5 milliamperes with a resultant wide range of forward transconductance ($g_{fs}$). The drain current can be regulated by applying dc feedback with a bypassed source resistor ($R_S$). A good approximation of $R_S$ (where $I_{DQ} \geq I_{DS}/2$) can be calculated by the use of the following formula*, assuming that $V_{G1S}$ vs. $I_{DS}$ is linear over the current range under consideration:

$$R_S \approx \left(\frac{1}{g_{fs}(\text{min.})}\right)\left(\frac{\Delta I_{DS}}{\Delta I_{DQ}} - 1\right) \qquad \text{Eq. 1}$$

*See Appendix

where:

$\Delta I_{DS}$ is the current range given in the 3N200 technical bulletin

$\Delta I_{DQ}$ is the desired range of operating current

$g_{fs}$(min.) is the minimum forward transconductance at 1000 Hz

With the value of $R_S$ established, then the Gate-No. 1 Voltage ($V_{G1}$) can be calculated from the equation

$$V_{G1} = V_{G1S} + I_{DQ} R_S \qquad \text{Eq. 2}$$

where $V_{G1S}$ is estimated by:

$$V_{G1S} \approx \frac{I_{DQ} - I_{DS}}{g_{fs}(\text{avg.})} \qquad \text{Eq. 3}$$

where:

$g_{fs}$(avg.) is the average forward transconductance

To establish the Gate-No. 2 Voltage ($V_{G2}$), follow the same procedure described for calculating the Gate-No. 1 Voltage, except that a fixed $V_{G2S}$ of approximately 4 volts is adequate.

If gain control is desired, apply a negative-going voltage to Gate No. 2. Because Gate No. 2 has little control in the voltage range of +2 to +5 volts, this characteristic may be used to effect AGC delay of the device in order to maintain the low noise figure until the RF signal is out of the noise-level range.

### Stability Considerations

Typical "y" parameter data as a function of frequency are given in Table 1. Maximum available gain (MAG) calculated from these data are also included to indicate ideal gain performance (i.e., $y_{rs} = 0$). The ability of the MOS FET to approach these gain levels depends on the device maintaining stable performance at the required operating frequency.

There are several methods which may be used to test for gain vs. stability. One of these methods, the Linvill Criteria (C), is defined by the equation:

$$C = \frac{y_{rs}\, y_{fs}}{2g_{is}\, g_{os} - R_e\,(y_{rs}\, y_{fs})} \qquad \text{Eq. 4}$$

A value for C which is less than 1 indicates unconditional stability. Applying the 400-MHz values taken from Table 1 to the Linvill Criteria yields a value of C = 0.615; substantially less than the value indicating unconditional stability.

| CHARACTERISTICS | SYMBOL | FREQUENCY (MHz) 100 | 200 | 300 | 400 | 500 | UNITS |
|---|---|---|---|---|---|---|---|
| y Parameters | | | | | | | |
| Input Conductance | $g_{is}$ | 0.25 | 0.8 | 2.0 | 3.6 | 6.2 | mmho |
| Input Susceptance | $b_{is}$ | 3.4 | 5.8 | 8.5 | 11.2 | 15.5 | mmho |
| Magnitude of Forward Transadmittance | $\lvert y_{fs} \rvert$ | 15.3 | 15.3 | 15.4 | 15.5 | 16.3 | mmho |
| Angle of Forward Transadmittance | $\angle y_{fs}$ | -15.0 | -25.0 | -35.0 | -47.0 | -60.0 | degrees |
| Output Conductance | $g_{os}$ | 0.15 | 0.3 | 0.5 | 0.8 | 1.1 | mmho |
| Output Susceptance | $b_{os}$ | 1.5 | 2.7 | 3.6 | 4.25 | 5.4 | mmho |
| Magnitude of Reverse Transadmittance | $\lvert y_{rs} \rvert$ | 0.012 | 0.025 | 0.06 | 0.14 | 0.26 | mmho |
| Angle of Reverse Transadmittance | $\angle y_{rs}$ | -60.0 | -25.0 | 0 | 14.0 | 20.0 | degrees |
| Maximum Available Gain | MAG | 32.0 | 24.0 | 17.5 | 13 | 10.0 | dB |

**Table 1 – "y" Parameters from 100 to 500 MHz**

The following equation for Maximum Usable Gain $(MUG)^3$ is:

$$MUG = \frac{2K \left| y_{fs} \right|}{\left| y_{rs} \right| (1 + \cos \theta)} \qquad \text{Eq. 5}$$

where:

$\theta = \angle y_{fs} + \angle y_{rs}$

K = skew factor

$\angle y_{rs}$ = angle of reverse transadmittance

$\angle y_{fs}$ = angle of forward transadmittance

The skew factor, introduced in this equation, is a safety measure that establishes an arbitrary degree of skewing in the frequency response which may be introduced by regeneration. A value of 0.2 for K has been established on the basis of past experience. The value of MUG calculated at 400 MHz is 13.8 dB. This value of MUG is greater than the value of MAG, again indicating unconditional stability, since MAG, ignoring inherent feedback, is the conjugately matched gain. Therefore, neutralization or circuit loading is not required to insure stable performance, and the gain can approach MAG, limited only by circuit losses.

Reverse transadmittance ($y_{rs}$) is composed of several components, but the major ones are feedback capacitance ($C_{rss}$) and source-lead inductance ($L_S$). Therefore, care must be exercised in the application of the $y_{rs}$ values, shown in Table 1, at the upper end of the usable frequency range. The 3N200 utilizes a JEDEC TO-72 package that has 4 leads. The data in Table 1 was compiled with the use of a socket which contacts the leads of the 3N200 as close as possible to the bottom of the package as specified by the JEDEC Standard Proposal SP-1028 "Measurement of VHF-UHF "y" Parameters". The leads are shielded from each other to eliminate stray capacitance between the leads, but some lead inductance is inevitable. If the device is soldered directly to the circuit components using commercial production techniques rather than by precise laboratory methods, then additional source lead inductance can be expected. Also, some additional capacitive coupling may result if the input and output circuits are not completely isolated from each other.

Because the published $y_{rs}$ value for the 3N200 is very small, the circuit $y_{rs}$ values may differ significantly from the $y_{rs}$ values shown in Table 1 and hence, may result in an unstable operating condition. It is impossible to provide data for all possible mounting combinations, therefore, a recommended mounting arrangement is shown in Fig. 2. The source and substrate in the TO-72 package of the 3N200 are internally connected to lead No. 4 and the case. The source-lead inductance can be reduced, if the case is used as the source connection. Fig. 2 illustrates a partial component layout in which the case is held by a clamp or other fingered device. The clamp is soldered to a feedthrough capacitor to provide an effective, very-low inductance bypass to RF signals. This mounting arrangement still permits the use of a source resistor for DC stability, and enables the case to provide isolation between the input and output circuit in addition to the isolation afforded by the shield.

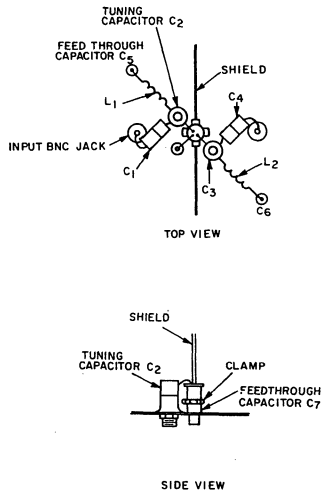



*Fig. 2 – Partial component layout of 400-MHz amplifier circuit*

The reduction of source-lead inductance provides in addition to greater stability, a lower input and output conductance. Table 2 shows the differences in "y" parameter values at 400 MHz when measured with the source connection made to lead No. 4 (in accordance with the published data for the 3N200) and when measured with the case connected directly to the ground plane of the test jig. The magnitude of reverse transadmittance is halved with a significant change in its phase angle. The input conductance is reduced by 30%, and the output conductance is reduced by 13%. A recalculation of the expressions for MAG, MUG, and Linvill Criteria (C) shows a significant improvement in gain and circuit stability.

While it is difficult to provide accurate information on the effects of shielding between the input and output circuits, its effect can be demonstrated when all other feedback components have been reduced to negligible values. The circuit, shown in Fig. 3 (for component layout see Fig. 2), was measured both with and without a shield. The maximum gain, without the shield, averaged 0.8 dB lower than with the use of the shield.

When receiver sensitivity is an important consideration in the design of an RF amplifier, a compromise must be made in the circuit power gain to achieve a lower noise

| CHARACTERISTICS | SYMBOL | FREQUENCY (f) = 400 MHz | | UNITS |
|---|---|---|---|---|
| | | Normal Connection | Case Grounded | |
| Maximum Available Power Gain | MAG | 13.0 | 15.7 | dB |
| Maximum Usable Power Gain (unneutralized) | MUG | 13.8 | 19.4 | dB |
| Linvill Stability Factor, C | C | 0.615 | 0.335 | mmho |
| "y" Parameters | | | | |
| Input Conductance | $g_{is}$ | 3.6 | 2.5 | mmho |
| Input Susceptance | $b_{is}$ | 11.2 | 11.7 | mmho |
| Magnitude of Forward Transadmittance | $\lvert y_{fs} \rvert$ | 15.5 | 15.5 | mmho |
| Angle of Forward Transadmittance | $\angle y_{fs}$ | -47.0 | -40.0 | degrees |
| Output Conductance | $g_{os}$ | 0.8 | 0.65 | mmho |
| Output Susceptance | $b_{os}$ | 4.25 | 4.25 | mmho |
| Magnitude of Reverse Transadmittance | $\lvert y_{rs} \rvert$ | 0.14 | 0.07 | mmho |
| Angle of Reverse Transadmittance | $\angle y_{rs}$ | 14.0 | 49.0 | degrees |

**Table 2 – "y" Parameters at 400 MHz with source connection to lead No. 4 and with case connected to ground plane of test jig**

factor. A contour plot of noise figure as a function of generator source admittance is shown in Fig. 4. Each contour is a plot of noise figure as a function of the generator source conductance and susceptance. Data for the noise figure were obtained from a test amplifier designed with very low feedback. Even though the area of very low-noise figure in the curves in Fig. 4 cover a broad range of source admittance, impedance-matching for maximum power gain could result in a relatively poor noise figure. As shown in Table 2, the input conductance ($g_{is}$) with the case grounded is 2.5 mmho. With the reactive portion tuned out, the noise factor at power matched conditions is almost 1 dB higher than the optimum noise figure. However, matching to 5.0 mmho results in a near optimum noise factor with a loss of only 0.5 dB in gain. In addition, impedance matching to high conductance

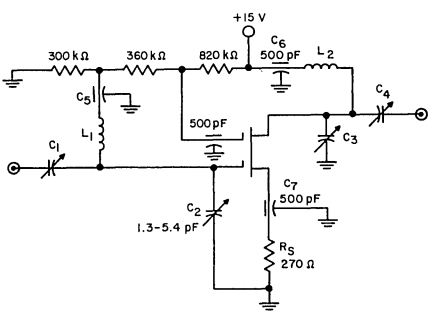



*Fig. 3 – 400-MHz amplifier circuit*

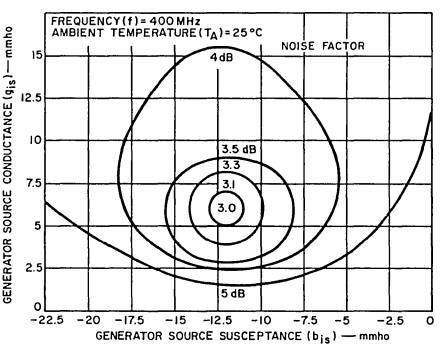



*Fig. 4 – Noise factor vs. generator source (input) admittance (Yis)*

also benefits crossmodulation performance, as will be discussed in a later section.

### Gate Protection Diodes

The diodes incorporated into RCA dual-gate MOS FETs, for gate protection, have been designed to minimize RF loading on the input circuits. The small amount of RF loading results in only a fraction of a dB loss in power gain and a negligible increase in the noise figure. The advantages of diode protection, greatly outweigh the slight loss in power gain, especially in an RF amplifier intended for the input stage of a receiver.

In addition to the protection afforded in normal handling, the diodes also provide in-circuit protection against events such as: static discharge due to contact with the antenna, delay in transmit-receive switching, or connection of an antenna with an accumulated charge to the receiver.

### Crossmodulation

Crossmodulation is an important consideration because it is an inherent device characteristic where circuit considerations are secondary. Crossmodulation is the transfer of modulation from an undesired signal on a desired signal caused by the non-linear characteristics of a device.

Crossmodulation is proportional to the third-order term of the expansion of the $I_D$ - $V_{GS}$ curve. It is normally specified as the undesired signal voltage required to produce a crossmodulation factor of 0.01. The crossmodulation factor is defined as the percent modulation on a desired carrier by the modulated undesired signal divided by the percent modulation of the undesired signal.[4]

Inspection of the $I_D$ - $V_{G1S}$ curve of Fig. 5 offers an insight to the possible crossmodulation as a function of gain-reduction performance. When both channels of the 3N200 are fully conducting current, as shown by the $V_{G2S}$ = 4-volt curve, the device approximately follows a square-law characteristic. If the $I_D$ - $V_{G1S}$ curve was ideal, the third-order term would be zero; but in practical cases, the third-order term and crossmodulation have some low values. When the gain is reduced, by the application of bias to Gate No. 2, the square-law characteristic changes to a curve with a knee. Sharp curvatures usually result in larger high-order terms and poorer crossmodulation performance can be expected at lower gain conditions. If in Fig. 6, Circuit A, we assume a fixed bias ($V_{G1S}$) of approximately +0.4 volt, then the expected variation in crossmodulation is determined at the points where the ordinate at $V_{G1S}$ = +0.4 volt crosses the curves. Crossmodulation performance at values of $V_{G2S}$ = +4 volts to cutoff is as follows: good (low crossmodulation) at +4 volts, poorer at +2 volts, poorest at +1 volt, and again improves from zero volts to cutoff.

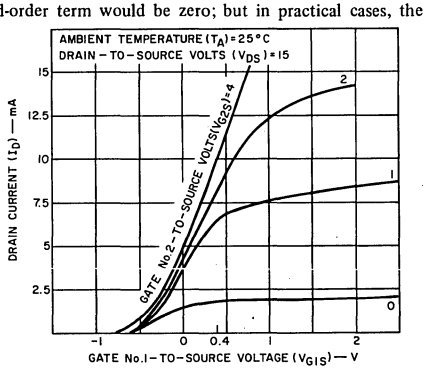



*Fig. 5 – Drain current ($I_D$) vs. gate No. 1-to-source voltage ($V_{G1S}$)*

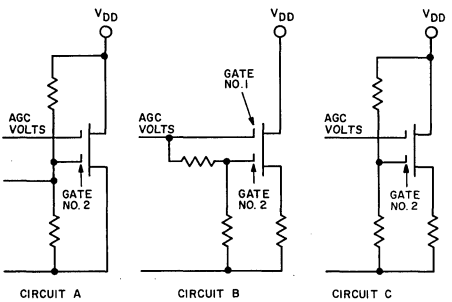



*Fig. 6 – Biasing circuits using the 3N200*

Curve A, Fig. 7 shows a curve of the undesired signal with a crossmodulation factor of 0.01 as a function of gain reduction. The curve indicates performance is poorest when gain reduction is in the 3- to 15-dB region; this region represents a Gate No. 2-voltage range of approximately 0.5 volt to 2 volts. The exception to the poor crossmodulation perform-

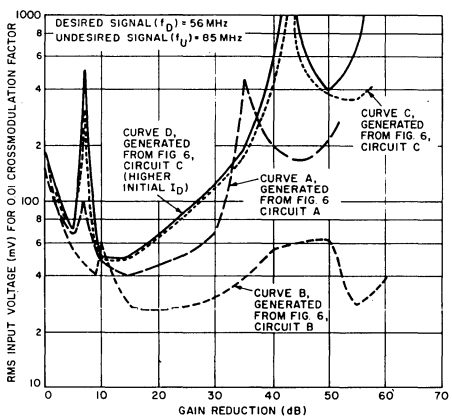



*Fig. 7 – Crossmodulation vs. gain reduction using biasing circuits shown in Fig. 6*

ance in this range is the sharp peak which occurs at the 5-dB level and is due to a curve inversion that takes place just prior to the knee. Beyond the 15-dB level, crossmodulation generally shows an improvement.

If Gate No. 1 is also reverse biased in conjunction with Gate No. 2 in the manner shown in Fig. 6, Circuit B, then the overall performance is poorer because the Gate No. 1 voltage will tend to follow the knee of each curve. This occurrence is evident in Fig. 7, Curve B. If Gate No. 1 is biased as shown in Fig. 6, Circuit C, the Gate No. 1-to-Source voltage intercepts the Gate No. 2 curves where the curvature is less severe, indicating as shown by Fig. 7, Curve C an improvement in crossmodulation performance. A further slight improvement is possible by the use of a higher initial operating drain current, which effectively moves the intercepts to the right on each curve. This improvement is indicated in Fig. 7, Curve D.

The curves in Fig. 7 establish that the biasing arrangement which provides optimum crossmodulation performance is the one in which Gate No. 1 forward bias increases as Gate No. 2 controls the gain. This biasing arrangement is easily accomplished by the use of a fixed Gate No. 1 voltage and a source resistor. As the Gate No. 2 bias voltage reduces the drain current, there is also a decrease in source voltage and an increase in the Gate No. 1-to-Source voltage. The gate-to-source voltage ratings must not be exceeded under any circumstances.

### Summary

An RF amplifier, ideally, should provide high gain, a low-noise figure, and low crossmodulation. The 3N200 offers a good compromise in providing these three features. As indicated in the section on "Stability Considerations" a mismatch at the circuit input to a higher conductance level, provides an improved noise figure. The same mismatch condition also improves crossmodulation performance. The input signal at the gate of the device, when mismatched as indicated above, is lower than if it is power matched. The same ratio applies to any undesired signal and, thus, reduces the possibility of crossmodulation interference.

### Appendix

The drain current of a device is established by the relationship

$$I_D = g_{fs} V_{G1S} + I_{DS}$$

where:

$I_{DS}$ = drain current

at:

$V_{G1S} = 0$, $V_{G2S} = +4$ volts.

If a source resistor is used, as shown in Fig. A1, the gate No. 1-to-source voltage is

$$V_{G1S} = V_{G1} - I_D R_S$$

then

$$I_D = g_{fs} (V_{G1} - I_D R_S) + I_{DS} \quad \text{or}$$

$$I_D = \frac{g_{fs} V_{G1}}{1 + g_{fs} R_S} + \frac{I_{DS}}{1 + g_{fs} R_S}$$

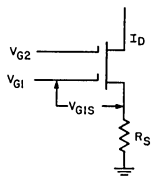



*Fig. A1 – Bias circuit using the 3N200*

The typical curves in Fig. A2 show drain current vs. Gate No. 1-to-Source Voltage as a function of $I_{DS}$ level. These curves are almost linear when the typical operating drain current is in the 10-milliampere region. For the remainder of the analysis a linear relationship will be assumed for the required range of quiescent current. The assumption of linearity dictates that $g_{fs}$ is a constant.

The required range of drain current is $I_{D2} - I_{D1}$

where:

$$I_{D2} = \frac{g_{fs} V_{G1}}{1 + g_{fs} R_S} + \frac{I_{DS}\,(max.)}{1 + g_{fs} R_S}$$

$$I_{D1} = \frac{g_{fs} V_{G1}}{1 + g_{fs} R_S} + \frac{I_{DS}\,(min.)}{1 + g_{fs} R_S}$$

$$\Delta I_D = I_{D2} - I_{D1} = \frac{I_{DS}\,(max.) - I_{DS}\,(min.)}{1 + g_{fs} R_S} = \frac{\Delta I_{DS}}{1 + g_{fs} R_S}$$

Solving the above equation for $R_S$ gives

$$R_S = \frac{(\Delta I_{DS}/\Delta I_D) - 1}{g_{fs}}$$

where:

$g_{fs}$ is equal to the expected minimum value at the required $I_D$

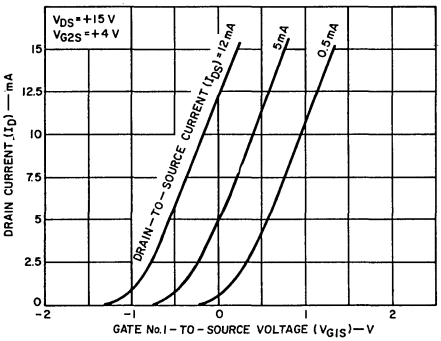



*Fig. A2 — Drain current vs. gate No. 1-to-source voltage*

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1. L. A. Jacobus and S. Reich, "Design of Gate-Protected MOS Field-Effect Transistors", RCA Application Note AN-4018
2. S. Reich, "Field-Effect Transistor Biasing Techniques", EEE, Sept. 1970
3. R. A. Santilli, "RF and IF Amplifier Design Considerations", IEEE Transactions on Broadcast and TV Receivers, Nov. 1967
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# Using MOS FET Integrated Circuits in Linear Circuit Applications

by S. Reich

Although the discrete metal-oxide-semiconductor (MOS) field-effect transistor (FET) has been available for many years,[1] its usage has been comparatively limited. Designers have been reluctant to employ MOS FET devices in their circuits because the gate oxide in a discrete device is vulnerable to damage by static electricity discharges encountered during handling and/or electrical transients found in circuit applications. RCA engineers have now successfully combined MOS FET and integrated-circuit (IC) fabrication techniques to produce a simple monolithic MOS FET IC in which back-to-back diodes are connected in shunt with the gate oxide to restrict the gate potential appearing across the gate oxide. The simple gate-protected IC's are of major significance because their immunity to damage by static electricity or by in-circuit transients is on a par of excellence with that of other solid-state devices intended for similar types of applications. Consequently, circuit designers can now practically utilize the many unique MOS FET characteristics, viz., high input impedance, square-law transfer characteristic, wide dynamic range, dual-gate configuration, etc. For example, the square-law transfer characteristic is especially desirable in the maintenance of low cross-modulation characteristics in rf amplifiers.[2,3] This paper contains a brief review of the device theory, followed by a survey of some linear circuit applications for the MOS FET IC.

## REVIEW OF DEVICE THEORY

The operating voltage applied to the MOS FET determines whether the device will function as a resistor, an amplifier, or a diode. This section will provide a review of these various MOS FET operational modes. Subsequently, the useful operational modes will be employed in typical applications.

Fig. 1 is a sketch, for zero gate-to-source voltage, of $I_D$ as a function of $V_{DS}$ for an n-channel depletion-type MOS FET. Changes in the conductivity pattern are shown in the simplified conductivity profile for each region of operation.

Ohmic – Region 'A' depicts an $I_D$-$V_{DS}$ curve that is characteristic of a resistance. The shape of this curve is a function of $V_{DS}$ (drain-to-source voltage). Its slope is governed by $V_{GS}$ (gate-to-source voltage). The $V_{DS}/I_D$

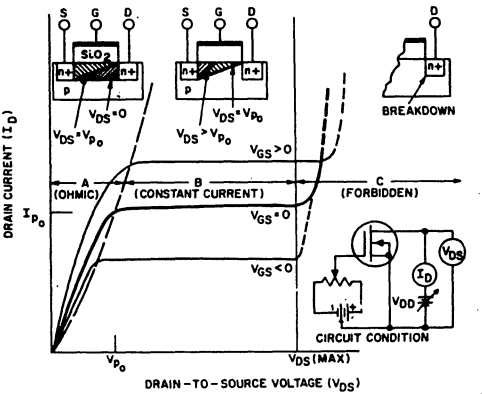



*Fig. 1—Regions of operation – n-channel depletion MOS FET.*

characteristic i.e., its resistance value, is controlled by the gate voltage.

As $V_{DS}$ is increased, it produces an electrostatic stress in the channel that modifies the channel conductivity as shown. The channel is completely pinched off beyond $V_{Po}$ (pinch-off voltage). Increasing $V_{DS}$ serves only to maintain $I_D$ at a constant level.

Amplifier[4] – For a fixed gate-voltage, $I_D$ is at a constant level in region 'B'. A change in $V_{GS}$ produces a change in $I_D$; thus in region 'B' the device exhibits the transconductance characteristic that is essential in amplifier operation (i.e., $G_m = dI_D/dV_{GS}$).

"Forbidden" Region – Increase of $V_{DS}$ beyond its rated maximum could produce avalanching in the drain-to-substrate diffusion (diode). Therefore MOS FET devices should not be operated in this region.

The dual-gate device is a serial arrangement of two single-gate devices. This arrangement improves the MOS FET performance by reducing capacitance from output to input (drain to gate 1), and provides an added control element that adds to the versatility of the MOS FET.

**Gate Protection**

A gate-protection system, which can be incorporated as an integral part of the transistor structure, has been developed for dual-gate MOS transistors. In devices that include this protection system, a set of back-to-back diodes is fabricated on the semiconductor pellet and connected between each insulated gate and the source. (The low junction-capacitance of the small diodes represents a relatively insignificant addition to the total capacitance that shunts the gate.) Fig. 2 is a profile drawing and schematic symbol for an n-channel dual-gate-protected depletion-type MOS field-effect transistor. The MOS FET IC metallization pattern, including the connections to the drain, gate 1, gate 2, source, and protective devices, all on a single monolithic structure, is shown in Figure 3.

The back-to-back diodes do not conduct unless the gate-to-source voltage exceeds typically ±10 volts. The transistor, therefore, can handle a very wide dynamic signal swing without significant conductive shunting effects by the diodes (leakage through the "nonconductive" diodes is very low, typically 1 na). If the potential on either gate exceeds typically +10 volts, the upper diode (shown in Fig. 2) of the pair associated with that particular gate becomes conductive in the forward direction and the lower diode breaks down in the backward (Zener) direction. In this way, the back-to-back diode pair provides a path to shunt excessive positive charge from the gate to the source. Similarly, if the potential on either gate exceeds typically -10 volts, the lower diode becomes conductive in the forward direction and the upper diode breaks down in the reverse direction to provide a shunt path for excessive negative charge from the gate to the source. The diode gate-protection technique is described in more detail in the following section on integrated gate protection.

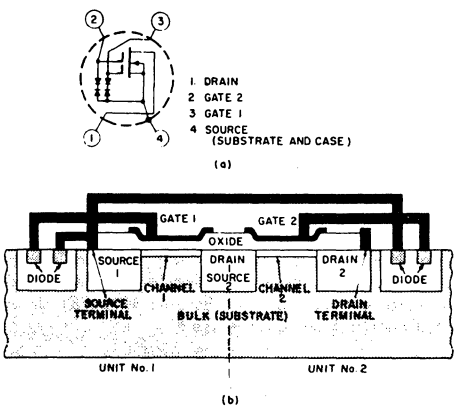



*Fig. 2–Protected dual-gate MOS FET IC: (a) schematic diagram; (b) profile sketch.*

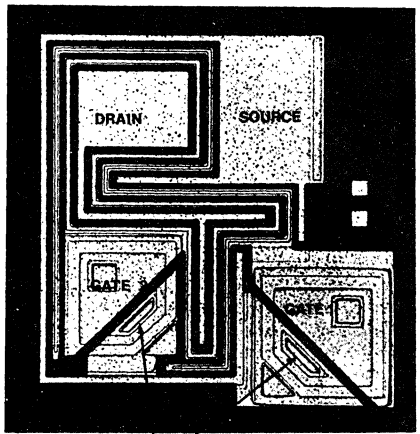



*Fig. 3–Monolithic protected dual-gate MOS FET IC.*

**Integrated Gate Protection**

The advent of an integrated system of gate-protection in MOS field-effect transistors has resulted in a class of solid-state devices that exhibits ruggedness on a par with other solid-state rf devices. The gate-protection system mentioned in the preceding section offers protection against static discharge during handling operations without the need for external shorting mechanisms. This system also guards against potential damage from in-circuit transients. Because the integral gate-protection system has provided a major impact on the acceptability of MOS field-effect transistors for a broad spectrum of applications, it is pertinent to examine the rudiments of this system.

Fig. 4 shows a simple equivalent circuit for a source of static electricity that can deliver a potential $e_O$ to the gate input of an MOS transistor. The static potential $E_S$ stored in

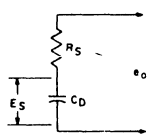



*Fig. 4–Equivalent circuit for source of static electricity.*

an "equivalent" capacitor $C_D$ must be discharged through an internal generator resistance $R_S$. Laboratory experiments indicate that the human body acts as a static (storage) source with a capacitance $C_D$ ranging from 100 to 200 picofarads and a resistance $R_S$ greater than 1000 ohms. Although the upper limits of accumulated static voltage can be very high, measurements suggest that the potential stored by the human body is usually less than 1000 volts. Experience has also indicated that the likelihood of damage to an MOS transistor as a result of static discharge is greater during handling than when the device is installed in a typical circuit. In an rf application, for example, static potential discharged into the antenna must traverse an input circuit that normally provides a large degree of attenuation to the static surge before it appears at the gate terminal of the MOS transistor. The ideal gate-protection signal-limiting circuit is a configuration that allows for a signal, such as that shown in Fig. 5(a), to be handled without clipping or distortion, but limits the amplitude of all transients that exceed a safe operating level, as shown in Fig. 5(b). An arrangement of back-to-back diodes, shown in Fig. 5(c), meets these requirements for protecting the gate insulation in MOS transistors.

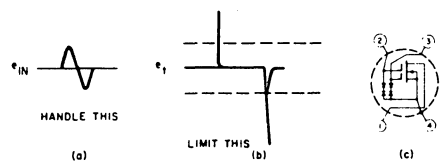



*Fig. 5—Gate-protection requirements and solution.*

Ideally, the transfer characteristic of the protective signal-limiting diodes should have an infinite slope at limiting, as shown in Fig. 6(a). Under these conditions, the static potential across $C_D$ in Fig. 6(b) discharges through its internal impedance $R_S$ into the load represented by the signal-limiting diodes. The ideal signal-limiting diodes, which have an infinite transfer slope, would then limit the voltage present at the gate terminal to its knee value, $e_d$. The difference voltage $e_s$ appears as an IR drop across the internal impedance of the source $R_S$, i.e., $e_s = E_s - e_d$ where $E_s$ is the potential in the source of static electricity and $e_d$ is the diode voltage drop. The instantaneous value of the diode current is then equal to $e_s/R_S$. During physical handling, practical peak values of currents produced by static-electricity discharges range from several milliamperes to several hundred milliamperes.

Fig. 7 shows a typical transfer characteristic curve measured on a typical set of back-to-back diodes used to protect the gate insulation in an MOS field-effect transistor that is nominally rated for a gate-to-source breakdown

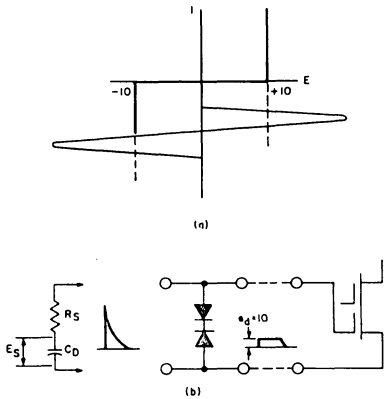



*Fig. 6—Ideal transfer characteristic of protective diodes (a), and resulting waveforms in equivalent circuit (b).*

voltage of 20 volts. The transfer-characteristic curves show that the diodes will constrain a transient impulse to potential values well below the ±20 volt limit, even when the source of the transient surge is capable of delivering several hundred milliamperes of current. (These data were measured with 1-microsecond pulses applied to the protected gate at a duty factor of $4 \times 10^{-3}$).

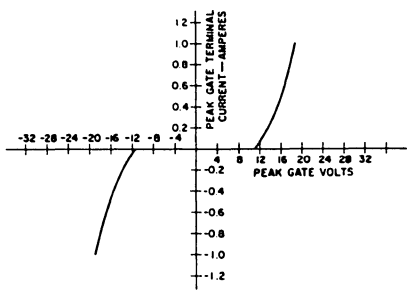



*Fig. 7—Typical diode transfer characteristic.*

### Electrical Requirements

The previous discussion points out that optimum protection is afforded to the gate with a signal-limiting diode that exhibits zero resistance (i.e., an infinite transfer slope and fast turn-on time) to all high-level transients. In addition, the ideal diode adds no capacitance or loading to the rf input circuit. This ideal diode in practice simply does not exist, but integrated circuit techniques made possible the development of a gate-protected MOS FET IC that is close to the ideal. For example, Fig. 8 shows typical 200-MHz input characteristic changes brought about by the addition of the integrated circuit diodes. Their effect on power gain and noise factor is shown by the data given in Table I. These data indicate that there are no discernible reductions in power gain and a trivial noise factor increase of about 0.25 dB.

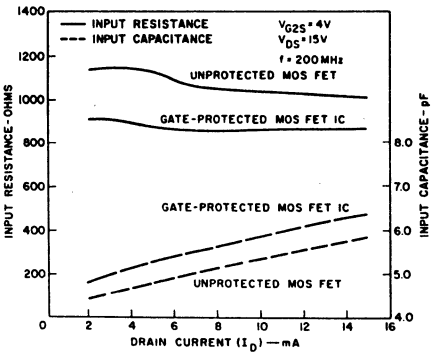



*Fig. 8–Input resistance and capacitance as functions of drain current for the MOS FET with and without diodes.*

**Table I - Power Gain and Noise Factor at 200 MHz**

| UNIT | POWER GAIN (dB) | | NOISE FACTOR (dB) | |
|---|---|---|---|---|
| | DIODES IN | DIODES REMOVED | DIODES IN | DIODES REMOVED |
| 1 | 16.3 | 16.4 | 3.7 | 3.4 |
| 2 | 18.8 | 18.5 | 2.4 | 2.2 |
| 3 | 16.5 | 16.2 | 3.3 | 3.0 |
| 4 | 16.3 | 15.7 | 3.9 | 3.4 |
| 5 | 17.7 | 17.8 | 2.6 | 2.4 |
| 6 | 17.2 | 17.5 | 2.8 | 2.5 |
| 7 | 17.1 | 17.0 | 3.3 | 3.2 |
| 8 | 17.9 | 18.0 | 2.9 | 2.6 |
| 9 | 18.5 | 18.5 | 2.4 | 2.3 |
| 10 | 17.3 | 17.3 | 3.2 | 3.0 |

### The Triode-Connected Protected Dual-Gate IC

The dual-gate MOS FET can be connected so that it functions as a single-gate device, as shown in Fig. 9. The triode-connected configuration has curve tracer (drain family) characteristics that look like the 'real' triode. The curves in Fig. 10 show that characteristics for the triode MOS FET (3N128) and the triode-connected dual-gate MOS FET (3N187) are essentially similar.

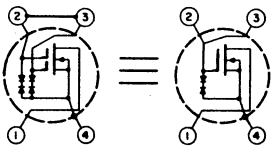



*Fig. 9–Dual-gate MOS FET IC in a single-gate configuration.*

### Triode-Connected-Device Characteristics

Some useful triode-connected-device characteristics are provided in Table II in the form of comparisons with dual-gate and single-gate devices. It should be noted that the difference in $I_{DS}$ level between the 3N187 and the 3N200 carries over to their triode-connected versions. A curve showing $I_{DSS}$ for triode connection versus $I_{DS}$ for the dual-gate configuration (i.e., $V_{G2S}$ = 4 volts) is shown in Fig. 11.

A plot of the triode-connected dual-gate transfer characteristics ($I_D$ vs. $V_{GS}$) is shown in Fig. 12; similarly, $g_{fs}$ curves are given in Fig. 13 as functions of $I_D$. Curves for typical dual-gate operation are available in commercial data sheets.[5,6]

Dual gates connected as tetrodes and triodes were evaluated for $R_{D(ON)}$ where 'on' resistance compares favorably with single-gate devices. Typical variations in $R_{D(ON)}$ as a function of gate voltage are shown in Fig. 14.

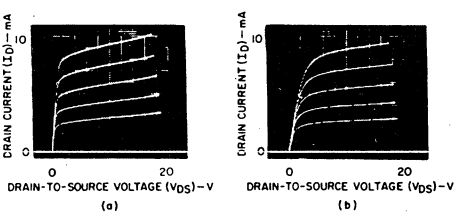



*Fig. 10–Drain families: (a) for triode-connected protected dual-gate device; (b) for triode.*

**Table II – Comparison of Typical Electrical Characteristics for Triode-Connected Dual-Gate, Dual-Gate, and Triode MOS FET Devices**

| CHARACTERISTIC | CONDITIONS | TRIODE–CONNECTED 3N187 | TRIODE–CONNECTED 3N200 | DUAL–GATE CIRCUIT* 3N187 | DUAL–GATE CIRCUIT* 3N200 | SINGLE GATE 3N128 | UNITS |
|---|---|---|---|---|---|---|---|
| $I_{DS}$ | $V_{DS}$ = 15 v | 6.0 | 2.0 | 15 | 5 | 15 | mA |
| $g_{fs}$ | $V_{DS}$ = 15 v, $I_D$ = 10 mA, f = 1 kHz | 7.0 | 8.5 | 12 | 15 | 9 | mmho |
| $V_{G1S(OFF)}$ | $V_{DS}$ = 15 v, $I_D$ = 50 μA | -2.0 | -1.0 | -2.0 | -1.0 | -1.5 | V |
| $I_{G1SS}$ | $V_{GS}$ = ±6 v | 2.0 | 2.0 | 1.0 | 1.0 | $10^{-4}$ | nA |
| $C_{iss}$ | $V_{DS}$ = 15 v, $I_D$ = 10 mA, f = 1 kHz | 10.0 | 10.0 | 6.0 | 6.0 | 5.5 | pF |
| $C_{rss}$ | $V_{DS}$ = 15 v, $I_D$ = 10 mA, f = 1 kHz | 0.5 | 0.5 | 0.02 | 0.02 | 0.2 | pF |
| $C_{oss}$ | $V_{DS}$ = 15 v, $I_D$ = 10 mA, f = 1 kHz | 2.0 | 2.0 | 2.0 | 2.0 | 1.4 | pF |
| $R_{DS(ON)}$ | $V_{DS}$ = 1 v, $V_{GS}$ = 0 | 160 | 250 | 100 | 150 | 300 | ohm |

*$V_{G2S}$ = 4 v except for $I_{GSS}$ measurement, where $V_{G2S}$ = 0.

It should not be inferred from these comments that all single-gate applications can be handled by the protected dual-gate device. The advent of MOS FET opened application areas in which circuit requirements imposed leakage-current limits in the picoampere range. For these applications the present generation of protective gate devices do not suffice and it is necessary to employ a "classical" MOS FET type (e.g., 3N128) and exercise precautions against gate-insulation puncture.

## SURVEY OF LINEAR APPLICATIONS

This section shows typical circuit arrangements. Some are documented, and others are design ideas for use of dual-gate MOS FET's with integrated diodes in applications using tetrode and triode-connected configurations.

### Choppers

The circuits shown in Fig. 15 use the dual-gate MOS FET IC in chopper or gating circuits. In the shunt-circuit configurations shown in Figs. 15(a) and 15(b), the MOS device is normally conductive, i.e., $e_o$ is low. A negative gating-pulse turns off the MOS device so that approximately 50 percent of $e_g$ appears at the output terminals. Circuit (a) features the use of an additional control potential ($V_{G2}$). A dc potential may be applied as shown to the second gate, thereby establishing the value of desired channel 'on' resistance ($R_{DS}$). Alternatively, circuitry can be arranged so that the second gate can function as a "coincidence-gate", i.e., to reduce $e_o$ to a low value, a positive-going pulse must be applied to gate 2 simultaneously with a positive-pulse to gate 1.

All circuits in Fig. 15 make reference to Note (A). The circuit diagrams show a "jumper" connected between two terminals in the drain-to-ground-return circuits. The circuits as drawn assume a peak generator level ($e_g$) of less than 0.2 volts. Should the signal exceed this value, it is possible that the "n-p" parasitic diode between the drain and semi-

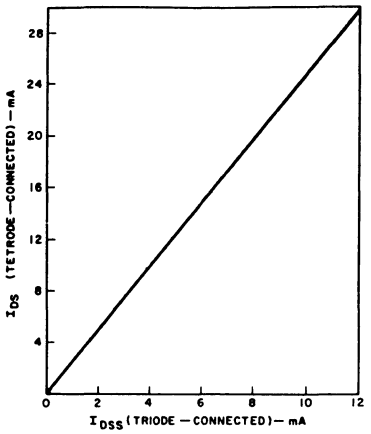



*Fig. 11—Correlation of zero-bias drain current for the protected dual-gate device in tetrode ($I_{DS}$) and triode ($I_{DSS}$) configurations.*

conductor substrate will be driven into conduction and load the signal. This contingency may be obviated (with a simultaneous improvement in attenuator linearity) by connecting a suitable dc potential in lieu of the "jumper", so that a positive potential is applied to the drain. The magnitude of this voltage should equal or exceed the peak value of the rms signal from $e_g$.

Circuits shown in Figs. 15(c) and 15(d) function in a manner opposite to those described above, i.e., output voltage appears at $e_o$ in the absence of a gating signal. Consequently, a negative gating signal reduces the level of $e_o$. The dual-gate configuration can be made into an 'or' circuit, i.e., a negative signal applied to gate 2 of sufficient magnitude to override $V_{G2}$ will also reduce the level at $e_o$.

**Attenuators**

Fig. 16 shows the dual-gate device in an attenuator circuit. In Fig. 16(a) both gates are used as control elements. This type of circuitry is particularly attractive when control of the attenuator must be located at some remote location. A dc potential on gate 1 has greater control on the channel resistance than is the case for gate 2. Thus an arrangement can be used whereby gate 2 provides a "fine" attenuator adjustment and gate 1 controls "course" adjustment. The circuit in Fig. 16(b) shows the dual-gate device in a triode-connected attenuator circuit. Curves showing typical variations in resistance as a function of gate-voltage were given in Fig. 14.

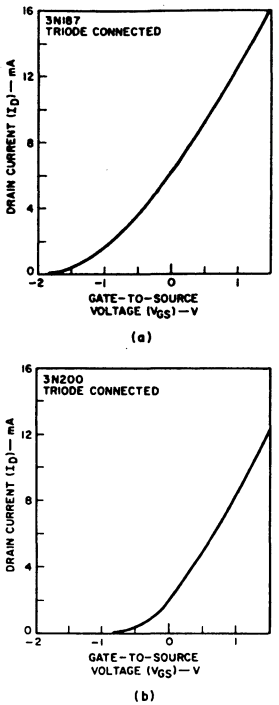



*Fig. 12—Triode-connected protected dual-gate MOS FET IC transfer characteristics.*

**Constant-Current Sources**

The characteristics of the MOS FET IC in the region beyond pinch-off make the device suitable for constant-current supplies, as illustrated in Fig. 17 (using a "triode-connected" dual-gate device).

The dual-gate device may be used to obtain higher values of current-regulation with the circuit depicted in Fig. 18. A supply circuit with a maximum output voltage capability of about 4.0 to 5.0 volts is required for $V_{G2}$. Values greater than this will have negligible effect on output current control.

The circuits in Fig. 19 use the MOS FET constant-current characteristic to make a regulated constant-voltage reference source by feeding $I_{DS}$ through a fixed-value resistor.

In any typical amplifier application using the MOS FET device, e.g., in Fig. 20, the voltage developed across a bypassed source resistance provides a well-regulated fixed reference voltage (if the amplifier stage is not subjected to

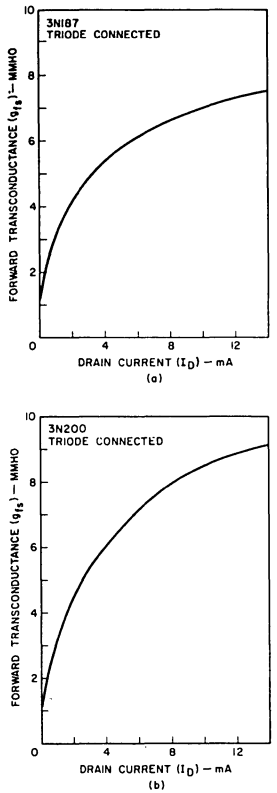



*Fig. 13–Triode-connected protected dual-gate MOS FET IC transconductance characteristics.*

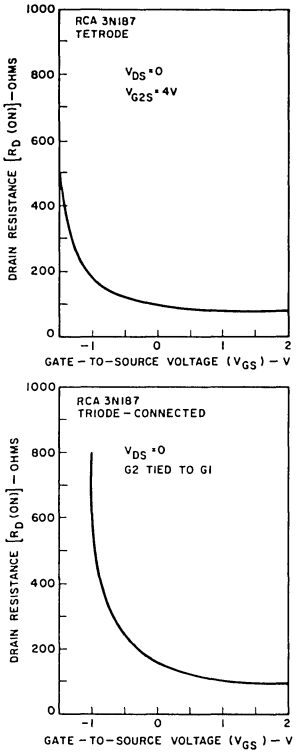



*Fig. 14–"ON" resistance as a function of gate voltage for tetrode- and triode-connected protected dual-gate MOS FET IC's.*

varying bias conditions, such as those encountered in connection with AGC). When a reference voltage is obtained in this manner, it is advisable to feed it to other circuitry through an adequate decoupling network.

**General-Purpose Amplifier Circuits**

Fig. 21 shows three basic single-stage amplifier configurations that utilize dual-gate-protected MOS FET IC's as triodes and as tetrodes in common source, common-drain, and common-gate circuits. Each configuration has its own particular advantages for specific applications. The dual-gate device has an added advantage in any of these configurations in that gate 2 provides (a) reduced gate-to-drain capacity by an order of magnitude, and (b) a convenient means for controlling the gain of the stage by adjusting the dc potential applied to gate 2.

A dual-gate device is shown in Fig. 22 as a shunt-type attenuator to control the input level to a source-follower. The source-follower uses the dual-gate MOS FET with gate 2 available as a control for adjusting the gain of the source-follower. The jumper in the ground return path of the generator can be used to insert a positive voltage on the drain for the reasons explained above.

Fig. 23 shows a circuit using the "triode-connected" dual-gate device in a simple 20-dB preamplifier for extending the sensitivity range of an oscilloscope or ac voltmeter. It can also be used in audio circuits as a phono preamplifier or microphone preamplifier. It is shown as self-contained, i.e.,

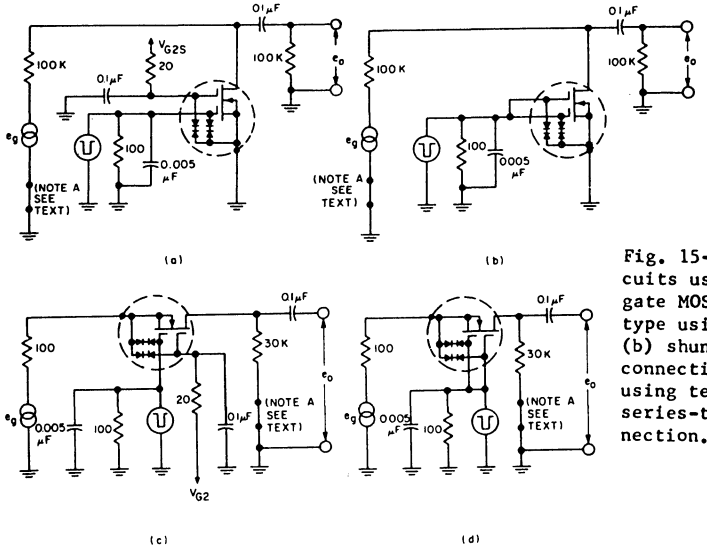



Fig. 15--Typical chopper circuits using protected dual-gate MOS FET IC's. (a) shunt-type using tetrode connection; (b) shunt-type using triode connection; (c) series-type using tetrode connection; (d) series-type using triode connection.

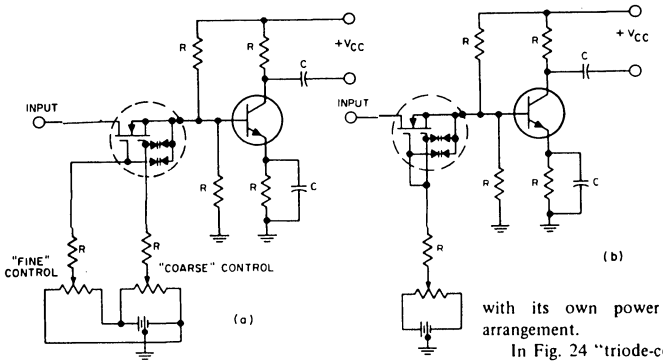



*Fig. 16—Attenuator circuits using the protected dual-gate MOS FET IC: (a) variable series-type attenuator with coarse and fine controls; (b) variable series-type attenuator using triode-connected configuration.*

with its own power supply and a by-pass switching arrangement.

In Fig. 24 "triode-connected" MOS FET devices are used in a simple differential amplifier configuration in which the "triode-connected" gates of the two devices are biased from a single source (the junction of R1 and R2). This arrangement is possible because the 3N187 has a typical gate current ($I_{GSS}$) in the triode configuration of 2 nanoamperes. Therefore, the bias can be supplied through R3 with a negligible voltage offset. Resistor R5 is used to null out the effects of slight differences in device characteristics so that the offset-voltage at $e_O$ can be set to zero.

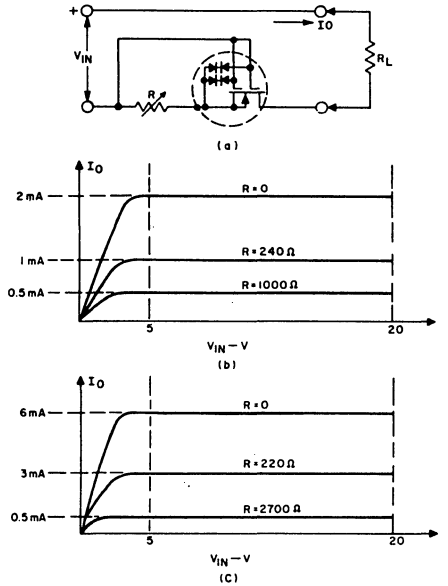



*Fig. 17—Constant-current supply using protected dual-gate MOS FET IC in triode configuration: (a) basic circuit; (b) typical $I_o$ vs. $V_{in}$ for RCA-3N200 in the basic circuit; (c) typical $I_o$ vs. $V_{in}$ for RCA-3N187 in the basic circuit.*

The circuit in Fig. 25 shows another differential amplifier configuration, in which the offset voltage at $e_o$ can be set to zero by means of appropriate potentials supplied to the No. 2 gates, adjustment being provided by R6.

The circuit shown in Fig. 26 is a frequency-selective amplifier intended for operation within the audio frequency range of 10 Hz to 20 kHz. Frequency-selective circuits are used for selective coding, i.e., in garage-door openers, narrowing the bandwidth response in CW receivers to eliminate unwanted side bands, and in systems requiring some form of keying impulse (e.g., synchronizing the narration in a tape recorder with slides).

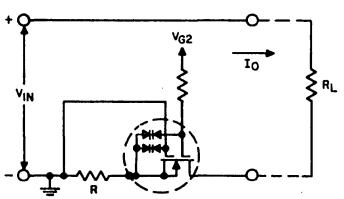



*Fig. 18—Protected dual-gate device as a constant-current source.*

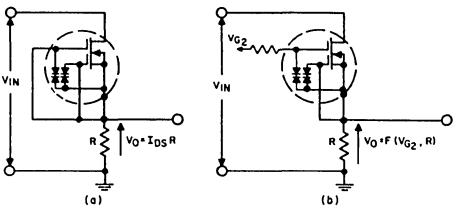



*Fig. 19—Voltage-reference circuits using protected dual-gate MOS FET IC: (a) as triode; (b) as tetrode.*

The frequency-selective circuit shown is an audio amplifier with a twin-"T" RC filter circuit in its output. This network provides regenerative feedback to the input circuit at an audio frequency predetermined by the selection of capacitors C5, C6, and C7. The peaking control R7 fine-tunes the twin-"T" for the desired frequency of operation, and potentiometer R8 adjusts the level of feedback for desired performance. The circuit as shown in Fig. 26 is selective at an audio frequency of 1200 Hz. Table III below lists values of the bridge capacitors for operation at other frequencies.

**RF Amplifiers, Oscillators, and Mixers**

The circuit in Fig. 27 is a converter used to convert 10-MHz WWV broadcasts to 1.5 MHz for reception on a standard broadcast-band receiver. The MOS FET IC is used in the dual-gate configuration as a mixer and is triode-

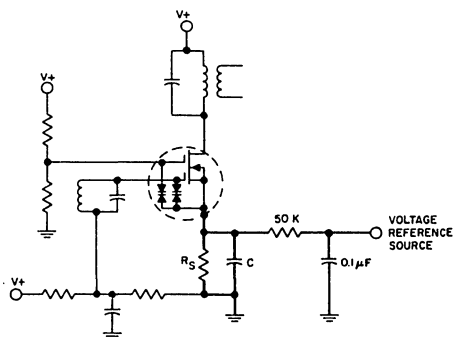



*Fig. 20—Typical amplifier using bypassed source resistor as a voltage source.*

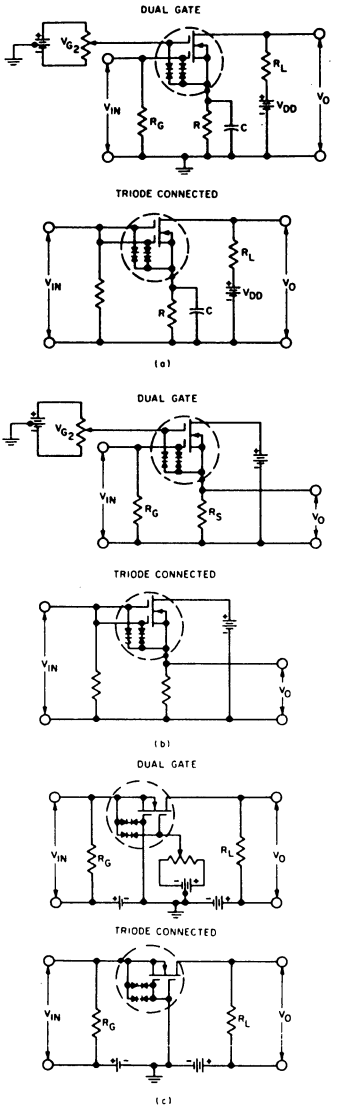



*Fig. 21—Three basic single-stage amplifier configurations that use protected dual-gate MOS FET IC's as triodes and tetrodes: (a) common source; (b) common drain; (c) common gate.*

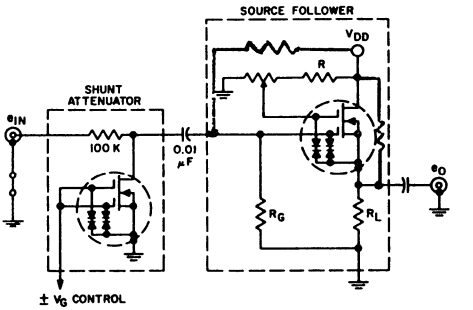



*Fig. 22—Shunt-type attenuator controlling input level to source-follower.*

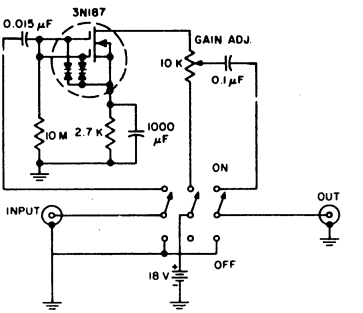



*Fig. 23—Protected dual-gate MOS FET IC preamplifier.*

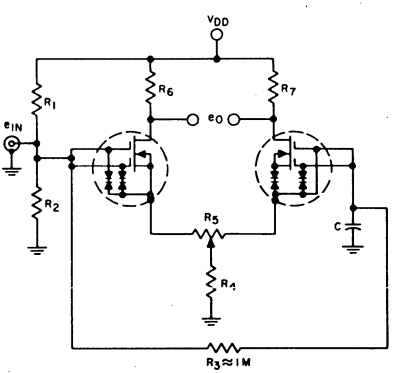


*Fig. 24—Triode-connected MOS FET IC's in a simple differential amplifier circuit.*

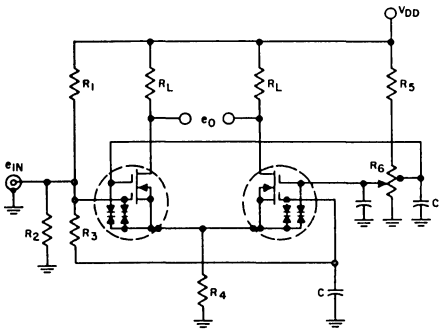



*Fig. 25—Protected dual-gate MOS FET IC's in typical differential amplifier circuit using gate 2 for balance control.*

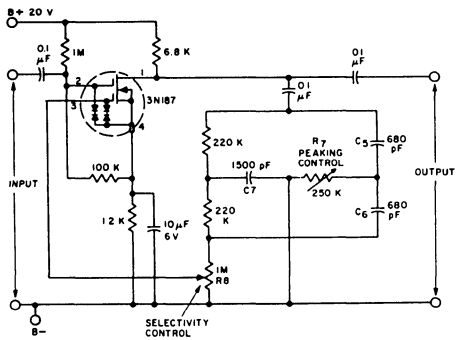



*Fig. 26—Selective audio-frequency amplifier.*

**Table III — Capacitor values for Fig. 26**

| FREQUENCY (Hz) | C5, C6 (pF) | C7 (pF) |
|---|---|---|
| 150 | 5,600 | 12,000 |
| 300 | 2,700 | 6,200 |
| 600 | 1,300 | 3,000 |
| 2400 | 330 | 750 |
| 4800 | 160 | 360 |
| 9600 | 82 | 180 |

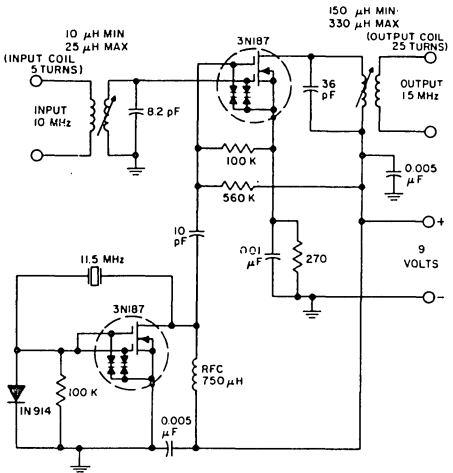



*Fig. 27—10 MHz-to-1.5 MHz converter for WWV reception.*

connected in a crystal oscillator circuit. MOS FET characteristics are very attractive for use in highly stable oscillator circuits because the inherent reactive components, $C_{iss}$ and $C_{oss}$, are relatively invariant over a very wide temperature range. Additional types of oscillator circuits in a number of different arrangements are shown in Fig. 28.

It is also feasible to use the MOS FET IC as a keyed oscillator, by utilizing a circuit arrangement shown in Fig. 29. A negative voltage at gate 2 will key the oscillator. Additionally, the level of the oscillator output can be controlled by variation of $R_L$. It should be understood that any of the oscillator configurations shown above are adaptable to the circuit arrangement in Fig. 29.

A dual-gate-protected MOS FET IC is used in Fig. 30 as a regenerative amplifier/detector. The circuit is basically an amplifier with controlled feedback adjusted to the verge of oscillation, as shown in Fig. 30. Gate 2 provides a convenient means to adjust the amplifier gain to the requisite level. Detection is accomplished in the gate 1 input circuit by the interaction of the diode in parallel with the 100-kilohm resistor and the 270-picofarad capacitor.

A typical circuit that utilizes the MOS FET IC in the pix IF section of a TV receiver is shown in Fig. 31. This circuit utilizes gate 2 for AGC. The reverse AGC bias[7] applied to gate 2 in the circuit of Fig. 31 has the secondary effect of making gate 1 move in a positive direction. Evaluations of the relationship between AGC and crossmodulation show that it is desirable to allow the voltage between gate 1 and the source to move in a positive direction when gate 2 is reverse-biased. Various circuit arrangements have been used

to achieve this action. Reference to a more comprehensive review on crossmodulation as a function of bias is given in the bibliography.[2,3]

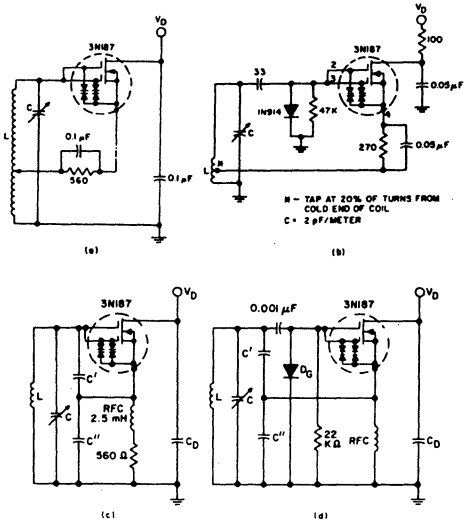



*Fig. 28–Oscillator circuits using MOS FET IC's: (a) and (b) Hartley oscillators; (c) and (d) Colpitts oscillators.*

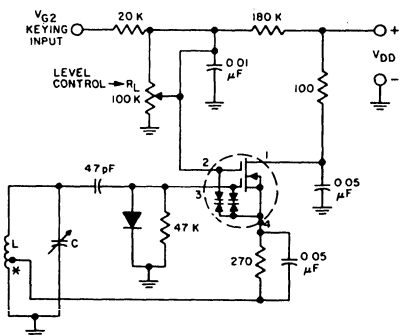



*Fig. 29–Gate-keyed oscillator using MOS FET IC.*

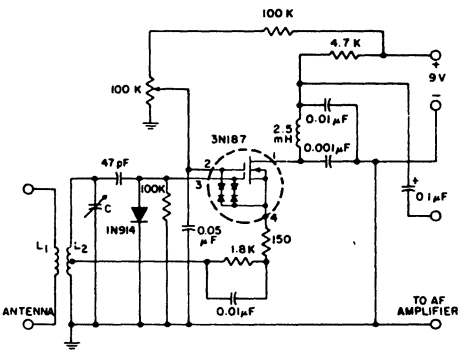



*Fig. 30–Protected dual-gate MOS FET IC regenerative receiver.*

A typical circuit for an FM tuner is shown in Fig. 32. The biasing arrangement for the rf stage incorporates provisions for AGC. The circuit in Fig. 33 is an rf amplifier designed for 200-MHz operation. The typical power gain for a 3N187 in this circuit is 18 db, with a noise factor of 3.5 dB.

Typical circuits for a TV tuner are shown in Figs. 34(a)-(d). Fig. 34(a) is the rf stage operating at a current level of approximately 10 milliamperes. Gate 1 is about 2 volts above ground potential. When AGC applied to gate 2 is advanced the drain current decreases, with a consequent reduction in voltage drop across the 270-ohm source resistances.[7]

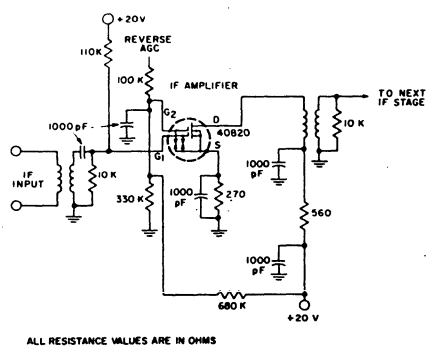
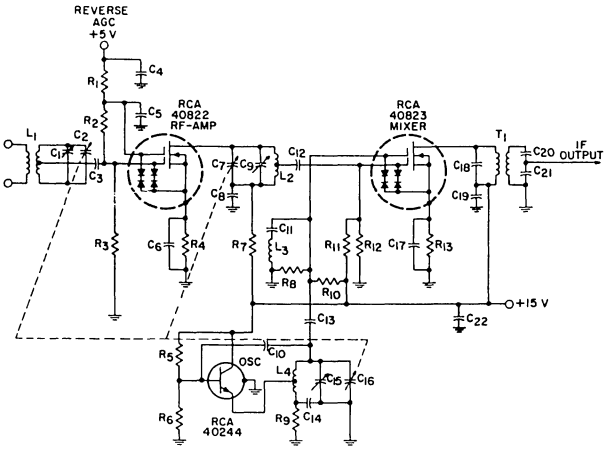
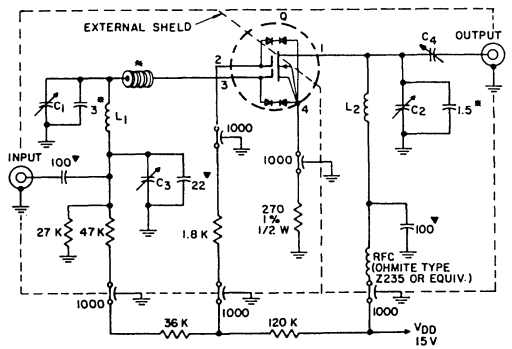



*Fig. 31–TV IF amplifier stage utilizing RCA-40820 MOS FET IC.*




C1, C9, C15 = Trimmer capacitor, 2 to 14 pF
C2, C7, C16 = Ganged tuning capacitors, each section = 6 to 19.5 pF
C3, C6, C14, C17, C22 = 2000 pF, ceramic
C4, C5 = 1000 pF, ceramic disc
C8, C19 = 0.01 μF, ceramic disc
C10 = 3.3 pF, NPO ceramic
C11 = 270 pF
C12 = 500 pF, ceramic disc
C13 = 3 pF, NPO ceramic
C18 = 68 pF, ceramic
C20 = 50 pF, ceramic
C21 = 1200 pF, ceramic
L1 = antenna coil; 4 turns of No. 18 bare copper wire; inner diameter, 9/32 inch; winding length, 3/8 inch; nominal inductance, 0.86 μH; unloaded Q, 120; tapped approximately 1 1/4 turns from ground end; antenna link approximately 1 turn from ground end
L2 = rf interstage coil; same as L1 antenna link
L3 = rf choke, 1 μH
L4 = oscillator coil; 3 1/4 turns of No. 18 bare copper wire; inner diameter, 9/32 inch; winding length, 5/16 inch; nominal inductance, 0.062 μH, unloaded Q, 120; tapped approximately 1 turn from low end
R1, R10 = 0.56 megohm, 0.5 watt
R2 = 0.75 megohm, 0.5 watt
R3 = 0.27 megohm, 0.5 watt
R4, R13 = 270 ohms, 0.5 watt
R5 = 22000 ohms, 0.5 watt
R6 = 56000 ohms, 0.5 watt
R7 = 330 ohms, 0.5 watt
R8, R12 = 0.1 megohm, 0.5 watt
R9 = 4700 ohms, 0.5 watt
R11 = 1.6 megohms, 0.5 watt
T1 = first if (10.7 MHz) transformer; double-tuned with 90 per cent of critical coupling; primary: 15 turns of No. 32 enamel wire, space wound at 60 turns per inch on 0.25-by-0.5-inch slug; secondary: 18 turns of No. 36 enamel wire, close wound on 0.25-by-0.25 inch slug; both coils wound on 9/32-inch coil form.

*Fig. 32—FM tuner using RCA-40822 and RCA-40823 MOS FET IC's for the rf amplifier and mixer stages.*




#Ferrite bead (4); Pyroterric Co. "Carbonl J" Q = 3N187 0.09 in. OD; 0.03 in. ID; 0.063 in. thickness.
▼ Disc ceramic
* Tubular ceramic
All resistors in ohms
All capacitors in pF
C1 = 1.8-8.7 pF variable air capacitor: E.F. Johnson Type 160-104, or equivalent.
C2 = 1.5-5 pF variable air capacitor: E.F. Johnson Type 160-102, or equivalent.
C3 = 1-10 pF piston-type variable air capacitor: JFD Type VAM-010; Johanson Type 4335, or equivalent
C4 = 0.8-4.5 pF piston type variable air capacitor: Erie 560-013 or equivalent.
L1 = 4 turns silver-plated 0.02-in. thick, 0.075-0.085-in. wide, copper ribbon, internal diameter of winding = 0.25 in., winding length approx. 0.08 in.
L2 = 4½ turns silver-plated 0.02-in. thick, 0.085-0.095-in. wide, 5/16 in. ID. Coil = .90 in. long.

*Fig. 33—200-MHz amplifier using the RCA-3N187 MOS FET IC.*

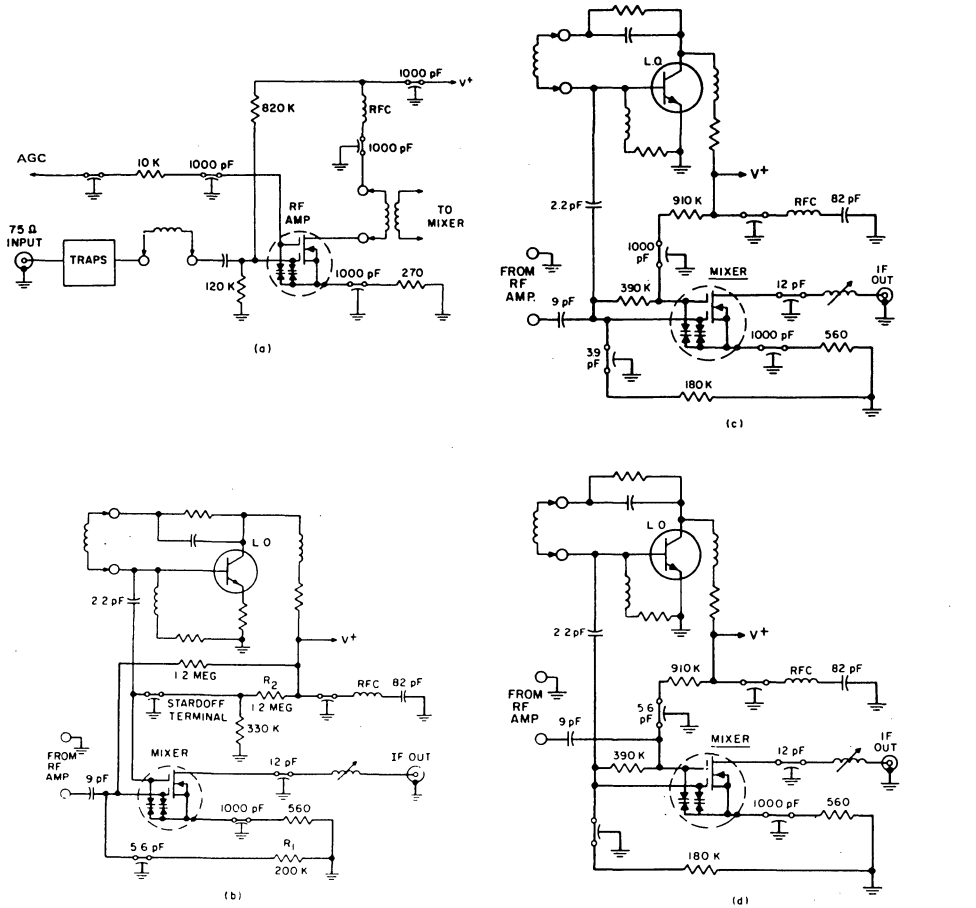



*Fig. 34–Typical circuits using protected dual-gate MOS FET IC's in a TV tuner for (a) rf stage, (b) mixer with rf on gate 1, oscillator on gate 2; (c) mixer with both rf and oscillator on gates 1 and 2; (d) mixer with rf on gate 2 and oscillator on gate 1.*

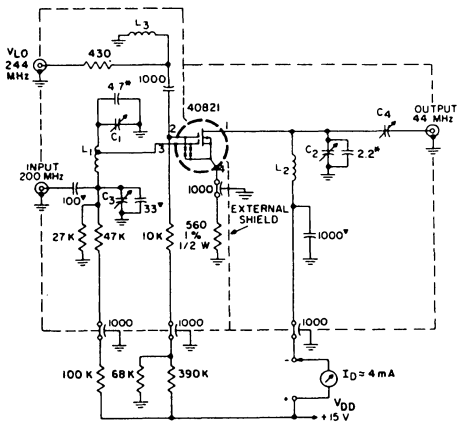
Because the voltage on gate 1 is fixed, the effect of applying AGC is to make the gate-to-source voltage drift in a positive direction as a negative gate 2 (AGC) voltage is applied. In these cases, as in the earlier IF system shown in Fig. 31, this circuit arrangement optimizes tuner performance for crossmodulation.[2]

The rf stage in Fig. 34(a) can work into any of the mixer circuits shown in Figs. 34(b), (c), and (d).

Fig. 34(b) is a mixer circuit arrangement with oscillator injection into gate 2 and the rf signal applied to gate 1. Fig. 34(c) utilizes gate 1 and gate 2 as the input elements for both rf signal and oscillator. Fig. 34(d) shows the rf signal applied to gate 2 and oscillator injection on gate 1.

Each of the above circuit arrangements has its own desirable characteristics, and the subject of mixer performance deserves a much more detailed discussion than can be accommodated here. In this context it is intended to demonstrate feasibility in terms of circuit arrangements.

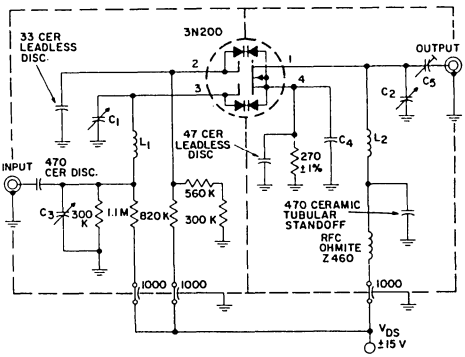
A mixer circuit with component values used in the laboratory for measuring conversion power gain from 200 to 44 MHz is shown in Fig. 35.[8]




▼ Disc. ceramic.
* Tubular ceramic.
All resistors in ohms
All capacitors in pF
C1, C2 = 1.5-5 pF variable air capacitor: E.F. Johnson Type 160-102 or equivalent.
C3 = 1-10 pF piston-type variable air capacitor: JFD Type VAM-010, Johanson Type 4335, or equivalent.
C4 = 0.9-7 pF compression-type capacitor: ARCO 400 or equivalent
L1 = 5 turns silver-plated 0.02" thick, 0.07"-0.08" wide copper ribbon. Internal diameter of winding = 0.25"; winding length approx. 0.65". Tapped at 1-1/2 turns from C1 end of winding.
L2 = Ohmite Z-235 RF choke or equivalent.
L3 = J.W. Miller Co. #4580 0.1 μH RF choke or equivalent.
NOTE: If 50Ω meter is used in place of sweep detector, a low pass filter must be provided to eliminate local oscillator voltage from load.

*Fig. 35—Mixer circuit for 200 MHz-to-44 MHz conversion, using the RCA-40821 MOS FET IC.*

Protected dual-gate MOS FET's have been used in applications operating at frequencies up to 500 MHz. They are useful in such uhf applications as rf amplifiers and mixer circuits. For example, the RCA-3N200 has the capability to provide a typical rf power gain of 12.5 dB with 4.5-dB noise factor at 400 MHz in a common-source configuration without the need for neutralization. A circuit with this capability is shown in Fig. 36.




All resistances in ohms
All capacitances in pF
C1, C2 = 1.3-5.4 pF variable air capacitor: Hammerland Mac 5 type or equivalent
C3 = 1.9-13.8 pF variable air capacitor: Hammerland Mac 15 type or equivalent
C4 = Approx. 300 pF - capacitance formed between socket cover & chassis
C5 = 0.8-4.5 pF piston type variable air capacitor: Erie 560-013 or equivalent
L1, L2 = inductance to tune circuit

*Fig. 36—Using the RCA-3N200 MOS FET IC in a 400-MHz amplifier.*

## CONCLUSIONS

The preceding discussions outlined numerous practical applications that utilized the unique technical features of the RCA protected dual-gate MOS FET IC. A summary of these technical features includes:

1. Wide dynamic range – MOS FET IC's will handle both positive and negative signal excursions.
2. Crossmodulation and spurious response performance is inherently better than with other active devices such as bipolars and single-gate FET's.
3. The very low gate-leakage permits AGC circuitry with virtually no power requirements.

4. Two input control elements make the device adaptable for mixers, remote-control gain circuits, coincidence gate circuits, etc. The device can also function as a triode-equivalent when the two gates are connected to a single terminal.
5. An exceptionally high transconductance.
6. Negative temperature coefficient for drain current, so that thermal runaway is virtually impossible.
7. Extremely low feedback capacity, typically 0.02 picofarad; this means very low oscillator feedthrough from the mixer stage back to the antenna.
8. The low feedback capacity enables the dual-gate MOS FET IC to provide good rf power gain in common-source amplifiers without the need for neutralization.
9. In addition to the above features, the new MOS FET IC provides protection against static electricity discharges encountered during handling and/or in circuit applications. This protection was achieved with insignificant compromises in overall device performance.

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# Application of the RCA CA3008 and CA3010 Integrated-Circuit Operational Amplifiers

BY
A. J. LEIDICH

The RCA CA3008 and CA3010 Operational Amplifiers are silicon monolithic integrated circuits designed to operate from two symmetrical low- or medium-level dc power supplies (at supply voltages in the range from ±3 volts to ±6 volts). The power dissipation in the amplifiers ranges from 7.0 milliwatts to 92 milliwatts depending upon the supply-voltage level and the desired output-power level. The amplifiers are primarily intended to operate with externally applied negative feedback; however, they may also be operated successfully under open-loop conditions. The main features of the CA3008 and CA3010 Operational Amplifiers are listed below:

- All-monolithic construction designed to operate at ambient temperatures from −55°C to +125°C.
- Built-in temperature compensation which assures that the gain and dc operating point are stable over the temperature range of −55°C to +125°C.
- Capability of operating at extremely low dissipation and supply-voltage levels, as well as at medium levels.
- Balanced differential-amplifier input configuration and a single-ended output configuration.
- No shift in the dc level between the differential inputs and the output.
- Little effect on the input offset voltage from variations in the power-supply voltages.

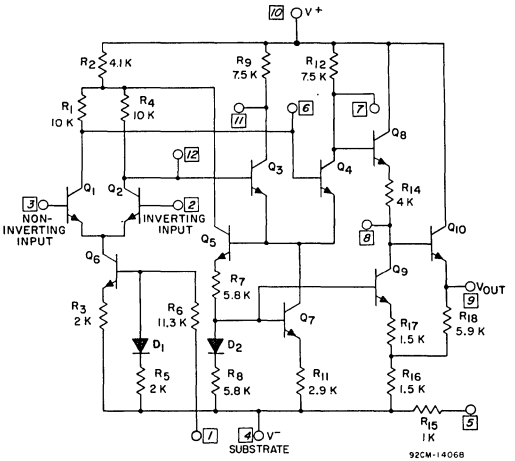
The CA3008 Operational Amplifier is supplied in a 14-terminal flat-pack; the CA3010 Operational Amplifier is supplied in a conventional 12-terminal TO-5 package. With the exception of the differences in their package construction, the two operational amplifiers are identical. This note describes the circuit arrangement, lists the performance characteristics, explains the major design considerations, and discusses typical applications of the operational amplifiers.

## CIRCUIT DESCRIPTION

Fig. 1 shows the schematic diagram of the CA3008 or the CA3010 Operational Amplifier. The numerals shown alongside the circuit terminals indicate the terminal designations for the CA3008 14-terminal flat-pack and CA3010 12-terminal TO-5 package. The numerals enclosed in squares are the designations for the CA3010 package. The diagram in the upper right corner of the figure shows the orientation of the terminals on the CA3008 flat-pack; the diagram at the lower right corner shows the orientation on the CA3010 TO-5 package. (The number designations used to refer to specific terminals in the following discussion, or elsewhere in this note, are those for the CA3008 14-terminal flat-pack. The corresponding terminals on the

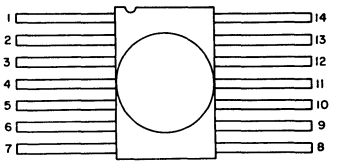
CA3010 12-terminal TO-5 package can be determined from the schematic in Fig. 1.)

As shown in the schematic diagram, each operational amplifier consists basically of two differential amplifiers

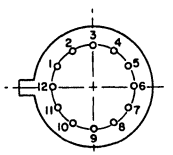



Note: $R_{10}$ and $R_{13}$ not used.

the second differential amplifier is provided by current-sink transistor $Q_7$. Compensating diode $D_2$ provides the thermal stabilization for the second differential amplifier and also for the current-sink transistor, $Q_7$, in the output stage.




CA3008
14-TERMINAL FLAT-PACK




CA3010
12-TERMINAL TO-5 PACKAGE

*Fig. 1—Schematic diagram of the CA3008 or CA3010 Integrated-Circuit Operational Amplifier.*

and a single-ended output circuit in cascade. Circuit elements are also included to provide thermal stabilization and to compensate for shifts in the dc operating point. In addition, negative feedback loops are employed to cancel common-mode signals (i.e., error signals developed when the two inputs to the operational amplifier are in phase and of equal amplitude).

## CASCADED GAIN STAGES

The pair of cascaded differential amplifiers are responsible for virtually all the gain provided by the operational-amplifier circuit. The inputs to the operational amplifier are applied to the bases of the pair of emitter-coupled transistors, $Q_1$ and $Q_2$, in the first differential amplifier. The inverting input (at terminal 3) is applied to the base of transistor $Q_2$, and the noninverting input (at terminal 4) is applied to the base of transistor $Q_1$. These transistors develop the driving signals for the second differential amplier. A dc constant-current-sink transistor, $Q_6$, is also included in the first stage to provide bias stabilization for transistors $Q_1$ and $Q_2$. Diode $D_1$ provides thermal compensation for the first differential stage.

The emitter-coupled transistors, $Q_3$ and $Q_4$, in the second differential amplifier are driven push-pull by the outputs from the first differential amplifier. Bias stabilization for

## COMMON-MODE-REJECTION FEEDBACK LOOPS

Transistor $Q_5$ develops the negative feedback to reduce common-mode error signals that are developed when the same input is applied to both input terminals of the operational amplifier. Transistor $Q_5$ samples the signal that is developed at the emitters of transistors $Q_3$ and $Q_4$. Because the second differential stage is driven push-pull, the signal at this point will be zero when the first differential stage and the base-emitter circuits of the second stage are matched and there is no common-mode input. A portion of any common-mode, or error, signal that appears at the emitters of transistors $Q_3$ and $Q_4$ is developed by transistor $Q_5$ across resistor $R_2$ (the common collector resistor for transistors $Q_1$, $Q_2$, and $Q_6$) in the proper phase to reduce the error. The emitter circuit of transistor $Q_5$ also reflects a portion of the same error signal into current-sink transistor $Q_7$ in the second differential stage so that the activating error signal is further reduced.

Transistor $Q_5$ also develops feedback signals to compensate for dc common-mode effects produced by variations in the supply voltages. For example, a decrease in the dc voltage from the positive supply results in a decrease in the voltage at the emitters of transistors $Q_3$ and $Q_4$. This negative-going change in voltage is reflected by the emitter circuit of transistor $Q_5$ to the bases of current-sink transistors $Q_7$ and $Q_6$. Less current then flows through these transistors. The decrease in the collector current of transistor $Q_7$ results in a reduction of the current through transistors $Q_3$

and $Q_1$, and the collector voltages of these transistors tend to increase. This tendency to increase on the part of the collector voltages partially cancels the decrease that occurs with the reduction in the positive supply voltage. The partially cancelled decrease in the collector voltage of transistor $Q_4$ is coupled directly to the base of transistor $Q_8$ and is transmitted by the emitter circuit of this transistor to the base of output transistor $Q_{10}$. At this point, the decrease in voltage is further cancelled by the increase in the collector voltage of current-sink transistor $Q_9$ that results from the decrease in current mentioned above.

In a similar manner, transistor $Q_5$ develops the compensating feedback to cancel the effects of an increase in the positive supply voltage or of variations in the negative supply voltage. Because of the feedback stabilization provided by transistor $Q_5$, the CA3008 and CA3010 Operational Amplifiers provide high common-mode rejection, have excellent open-loop stability, and have a low sensitivity to power-supply variations.

## OUTPUT STAGES

In addition to their function in the cancellation of supply-voltage variations, transistors $Q_8$, $Q_9$, and $Q_{10}$ are used in an emitter-follower type of single-ended output circuit. The output of the second differential amplifier is directly coupled to the base of transistor $Q_8$, and the emitter circuit of transistor $Q_8$ supplies the base-drive input for output transistor $Q_{10}$. A small amount of signal gain in the output circuit is made possible by the bootstrap connection from the emitter of output transistor $Q_{10}$ to the emitter circuit of transistor $Q_9$. If this bootstrap connection were neglected, transistor $Q_9$ could be considered as merely a dc constant-current sink for drive transistor $Q_8$. Because of the bootstrap arrangement, however, the output circuit can provide a signal gain of 1.5 from the collector of differential-amplifier transistor $Q_4$ to the output (terminal 12). Although this small amount of gain may seem insignificant, it does increase the output-swing capabilities of the operational amplifiers.

The output from the operational-amplifier circuit is taken from the emitter of output transistor $Q_{10}$ so that the dc level of the output signal is substantially lower than that of the differential-amplifier output at the collector of transistor $Q_4$. In this way, the output circuit shifts the dc level at the output so that it is effectively the same as that at the input when no signal is applied.

Resistor $R_{15}$ in series with terminal 8 (refer to Fig. 1) increases the ac short-circuit load capability of the operational amplifier when this terminal is shorted to terminal 12 so that the resistor is connected between the output and the negative supply.

## OPERATING CHARACTERISTICS

The operating characteristics of the CA3008 and CA3010 Integrated-Circuit Operational Amplifiers are identical. The characteristics data given in the following paragraphs, therefore, apply equally to each type. A proper evaluation of the capabilities of the operational amplifiers requires a thorough understanding of the parameters in terms of which the operating characteristics are expressed. For this reason, the special parameters for which additional clarification may be necessary are defined in an appendix at the end of this note.

## DC CHARACTERISTICS

The operational amplifiers are designed to operate from two symmetrical dc power supplies at supply voltages in the range from ±3 volts to ±6 volts. For operation with ±3-volt supplies, the power dissipation in the amplifiers is less than 7.0 milliwatts with terminal 8 open or 23 milliwatts with terminal 8 shorted to terminal 12. When ±6-volt supplies are used, the dissipation level increases to either 30 milliwatts or 92 milliwatts, depending upon whether terminal 8 is open or shorted to terminal 12.

The input offset voltage for the operational amplifiers is typically 1.1 millivolts for all symmetrical supply voltages. This parameter is relatively insensitive to variations in the supply voltages. When ±6-volt supplies are used, the variation in the input offset voltage with fluctuations in supply voltage is typically less than 300 microvolts per volt for either supply. For ±3-volt supplies, the variation is typically 700 microvolts per volt. The offset voltage varies slightly with temperature as shown in Fig. 2. (Fig. 3

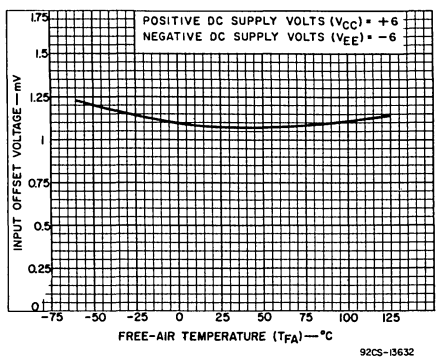
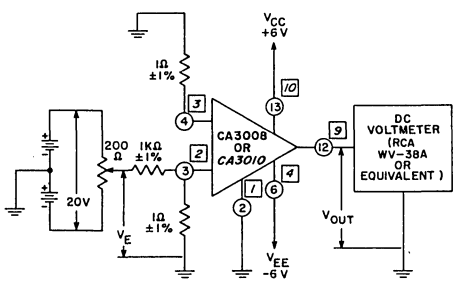



*Fig. 2—Input offset voltage as a function of temperature.*




NOTE: Pins 8 and 12 should be shorted for the pertinent power dissipation measurement ONLY!

*Fig. 3—Test circuit used to measure the input offset voltage.*

shows the schematic diagram of the special test circuit used for the offset-voltage measurements.)

The input bias current and the input offset current of the amplifiers are typically 5.3 microamperes and 0.54 microampere, respectively, when ±6-volt supplies are used. Figs. 4 and 5 show the variations in these parameters with temperature.

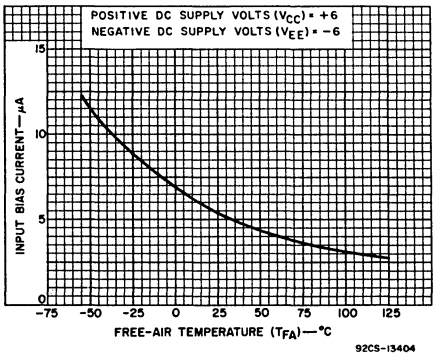



*Fig. 4—Input bias current as a function of temperature.*

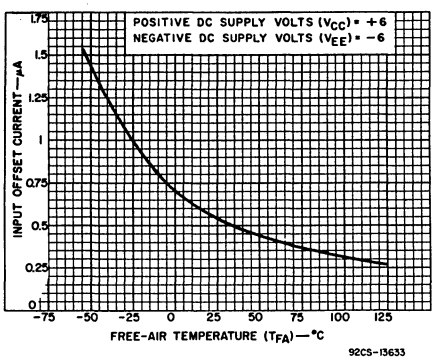



*Fig. 5—Input offset current as a function of temperature.*

## AC CHARACTERISTICS

**Gain-Frequency Response:** The operational amplifiers provide a gain of 60 dB at low frequencies and have a unity-gain bandwidth of 18 MHz when operated from ±6-volt supplies. The typical gain-frequency response is shown in Fig. 6 for operation of the amplifier at −55°C, at +25°C, and at +125°C. The response of the amplifier exhibits little change over the temperature range. A typical gain-frequency characteristic for amplifiers operated from ±3-volt supplies at 25°C is shown in Fig. 7.

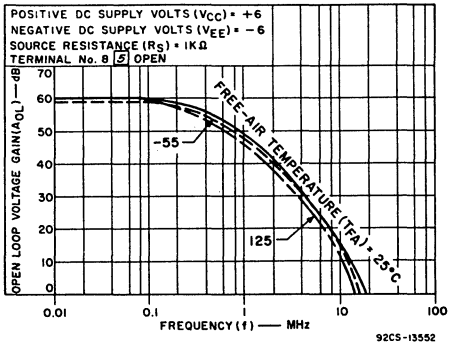



*Fig. 6—Open-Loop gain as a function of frequency.*

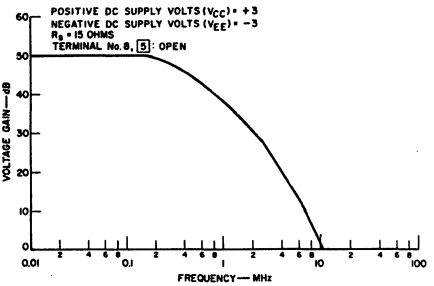



*Fig. 7—Voltage gain as a function of frequency.*

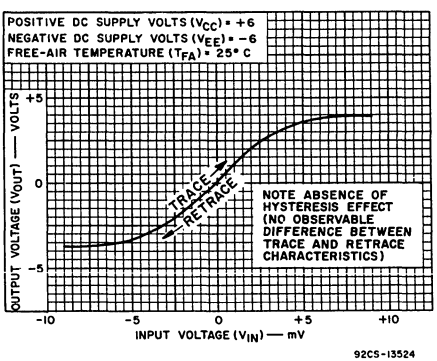



*Fig. 8—Output voltage as a function of input voltage for an open-loop operational amplifier.*

**Transfer Characteristic:** The transfer characteristic of the operational amplifiers is shown in Fig. 8. This characteristic shows that the amplifiers do not exhibit any hysteresis effect.

**Common-Mode Rejection:** The common-mode rejection provided by the operational amplifiers is typically 94 dB for operation with ±6-volt supplies. Fig. 9 shows the differential-gain and common-mode-gain frequency plots for the amplifiers. Fig. 10 shows the common-mode rejection as a function of frequency.

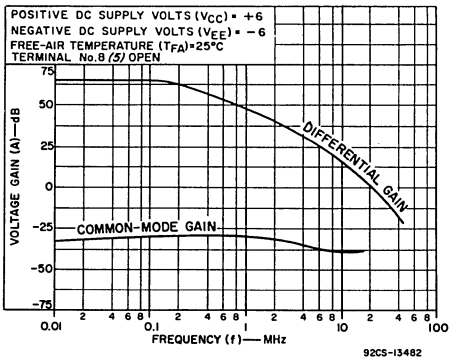



*Fig. 9—Differential and common-mode gain as a function of frequency at different temperatures.*

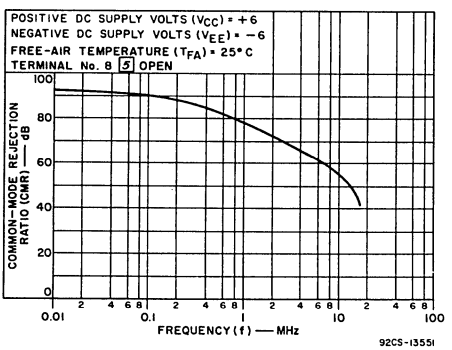



*Fig. 10—Common-mode rejection as a function of frequency.*

**Output Swing:** The operational amplifiers exhibit a maximum dynamic-swing capability of ±3.5 volts with terminal 8 open and of ±3.0 volts with terminal 8 shorted to terminal 12. The output-swing capability varies only slightly with temperature, as shown in Fig. 11. Fig. 12 shows the variation in the output-swing capability with frequency.

**Input and Output Impedances:** When the CA3008 or CA3010 Operational Amplifier is operated from ±6-volt supplies, it has an input impedance of 14,000 ohms at 1

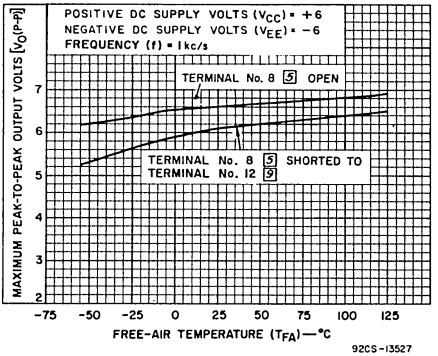



*Fig. 11—Output-swing capabilities as a function of temperature.*

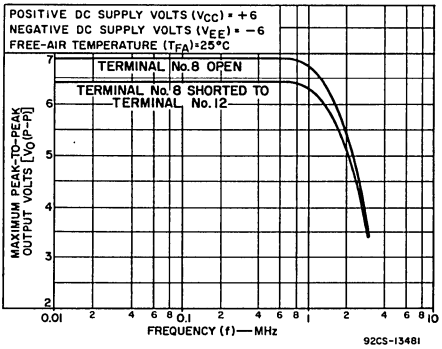



*Fig. 12—Output-swing capabilities as a function of frequency.*

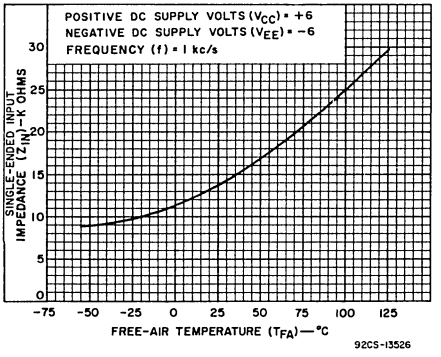



*Fig. 13—Input impedance as a function of temperature.*

kHz and an output impedance of 200 ohms (terminal 8 open) or 75 ohms (terminal 8 shorted to terminal 12). The input impedance and output impedance of the amplifier are affected by temperature as shown in Figs. 13 and 14, respectively.

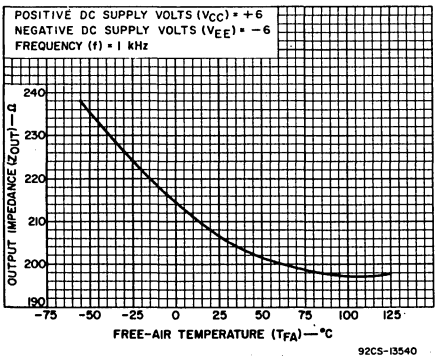
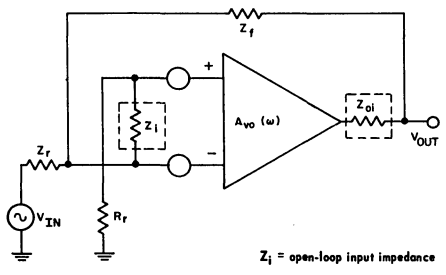



*Fig. 14—Output impedance as a function of temperature.*

## CIRCUIT DESIGN CONSIDERATIONS

The basic design equations for the CA3008 or CA3010 Operational Amplifier in closed-loop circuits are summarized in Figs. 15 and 16. Fig. 15 shows the basic schematic diagram and gives the design equations for the generalized inverting feedback configuration, and Fig. 16 provides the diagram and the equations for the noninverting configuration. In both configurations, the inputs are returned to ground through dc paths that are effectively identical. This condition is necessary for minimum offset voltage (dc error).

Because the open-loop input capacitance of the operational amplifier is less than 10 picofarads, the frequency response is virtually independent of the drive source impedance. The input-impedance equations given in Figs. 15 and 16 indicate that this lack of dependence is even more pronounced when the amplifiers are operated with negative feedback.

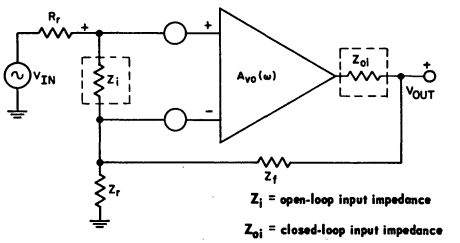



$$V_{out}/V_{in} = \frac{-Z_f}{Z_r + (Z_f + Z_r)/A_{V_o}(\omega)} \doteq -Z_f/Z_r$$

$$Z_{in} = Z_r + (Z_f/A_{V_o}(\omega)) // Z_i \doteq Z_r$$

$$Z_o = Z_{oi}\frac{(1 + V_{out}/V_{in})}{A_{V_o}(\omega)} \doteq 0$$

*Fig. 15—Inverting-feedback configuration for an operational amplifier.*




$$V_{out}/V_{in} = \frac{A_{V_o}(\omega)(Z_r + Z_f)}{Z_r + Z_f + Z_{vo}Z_r} \doteq 1 + Z_f/Z_r$$

$$Z_{in} = Z_i\left(1 + \frac{A_{V_o}(\omega)}{V_{out}/V_{in}}\right)$$

$$Z_o = Z_{oi}\left(\frac{V_{out}/V_{in}}{A_{V_o}(\omega)}\right)$$

*Fig. 16—Noninverting-feedback configuration for an operational amplifier.*

## PHASE COMPENSATION

Basically, phase compensation is used to alter the response of an amplifier so that a phase shift of 180 degrees cannot occur at a frequency for which the loop gain is unity or greater. A rule of thumb that will guarantee an ac-stable amplifier is that at the intersection of the closed-loop response with the open-loop response, the respective slopes must have a difference less than 12 dB per octave.

With few exceptions (some of which will be covered in the section on applications), phase compensation must be accomplished by altering the open-loop response of the operational amplifier itself. One of the advantageous features of the CA3008 and CA3010 Operational Amplifiers is that small values of capacitance properly added to the amplifier circuit will provide the required phase compensation. When ±6-volt supplies are used, two phase-compensating networks, each of which consists of a 27-picofarad capacitor in series with a 2000-ohm resistor,

connected between terminals 1 and 14 and between terminals 9 and 10, cause the amplifier to roll-off at a slope of one (6 dB per octave) all the way to unity gain (where it then breaks into a slope of two). This value of compensation is sufficient to stabilize the amplifier for all resistive-feedback applications including unity gain. The response for this value of phase compensation is compared to the original open-loop response in Fig. 17. Although the two compensating networks are sufficient to ac stabilize the amplifier, they are not sufficient to produce a flat response (within ±1 dB) for closed-loop gains below 15 dB. Fig. 18 shows a plot of the capacitance required to produce

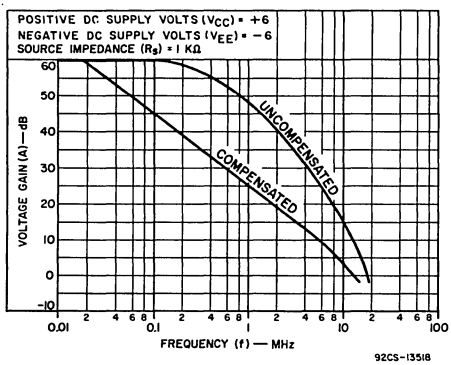



*Fig. 17—Open-loop gain as a function of frequency for both phase-compensated and uncompensated operational amplifiers.*

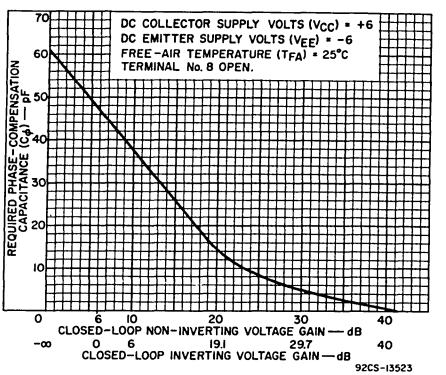



*Fig. 18—Amount of phase-compensating capacitance required to obtain a flat (± 1-dB) gain response as a function of frequency.*

a flat (±1-dB) gain response as a function of closed-loop gain. The capacitors must have a resistor in series with them so that $\frac{1}{2\pi RC} = 3$ MHz.

Phase compensation may also be effected conventionally by adding a capacitor in series with a resistor between terminal 11 and ground. A 0.02-microfarad capacitor in series with a 22-ohm resistor is sufficient to ac stabilize the CA3008 or CA3010 Operational Amplifier at resistive closed-loop gains down to unity.

The required phase compensation depends upon the feedback configuration and not upon the location of the drive source. Hence, phase-compensating networks that provide sufficient compensation for a 10-dB noninverting configuration also provide sufficient compensation for a 6-dB inverting configuration because the two feedback configurations are identical.

### OUTPUT-POWER MODIFICATIONS

A choice of two output-power capabilities is provided in the CA3008 and CA3010 Operational Amplifiers. The output can be tailored to the specific load requirements by leaving terminal 8 open and placing an appropriate resistor between terminals 6 and 12. The minimum safe value of load resistance (including the aforementioned resistor) is 200 ohms when ±6-volt supplies are used. In determining the output capability, it should be kept in mind that the feedback network can contribute to the output loading especially in the lower-gain configurations.

## APPLICATIONS OF THE OPERATIONAL AMPLIFIERS

The CA3008 and CA3010 Integrated-Circuit Operational Amplifiers can be adapted for use in a variety of diverse applications. For example, the amplifiers may be operated to provide the broad, flat gain-frequency response required for video amplifiers or the peaked responses required for various types of shaping amplifiers. Other applications of these amplifiers include comparators, integrators, differentiators, and summing amplifiers. The following paragraphs describe the circuit arrangements and the performance characteristics of the operational amplifiers in such applications:

### VIDEO AMPLIFIERS

When the feedback is applied through a purely resistive network and suitable phase compensation is employed, flat gains are attainable from the operational amplifiers. Fig. 19 shows a 30-dB noninverting configuration of a video amplifier, together with the closed-loop response of the circuit. The phase compensation is provided by a 5-picofarad capacitor in series with a 10,000-ohm resistor. This arrangement provides the required amount of compensation, as predicted in Fig. 18. (For purposes of comparison, the uncompensated response of the 30-dB configuration is shown in Fig. 20. Observe the 13-dB peaking effect at 4.5 MHz.) An alternate method of phase compensation may be used when the intersection of the closed-loop characteristic and the open-loop response occurs in a two-slope region. The technique is to cause the feedback ratio

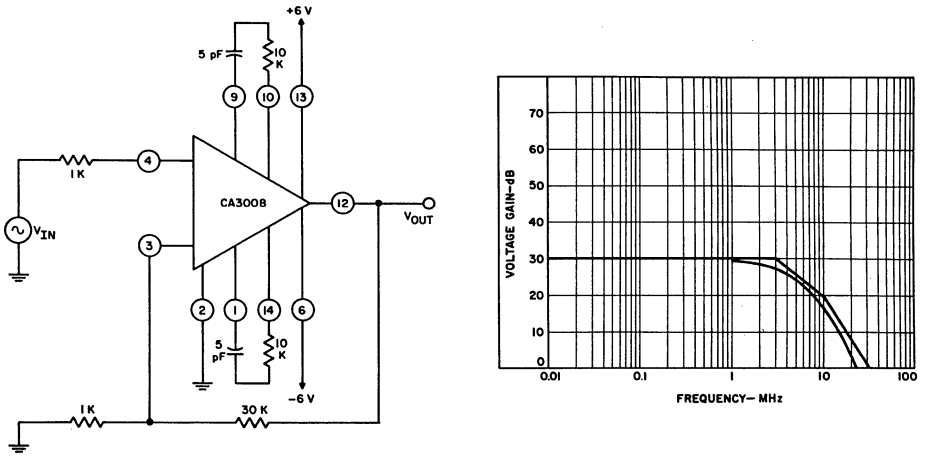



*Fig. 19—Noninverting configuration and closed-loop response of an operational-amplifier type of video amplifier that provides a gain of 30-dB.*

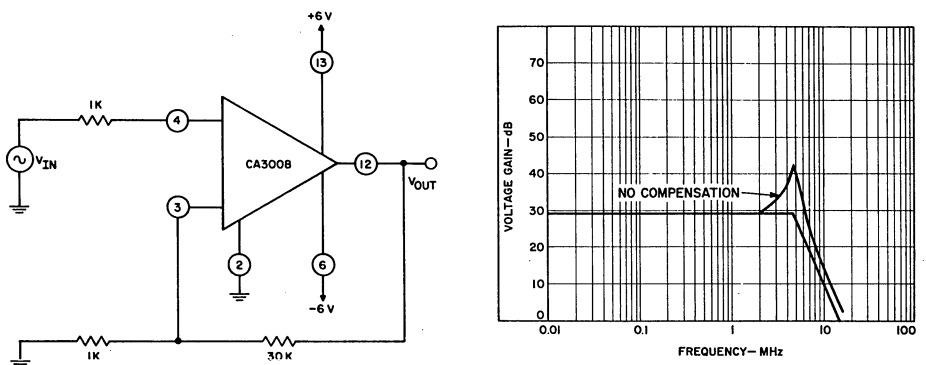



*Fig. 20—Circuit diagram and gain-frequency response of the 30-dB noninverting video amplifier operated without phase compensation.*

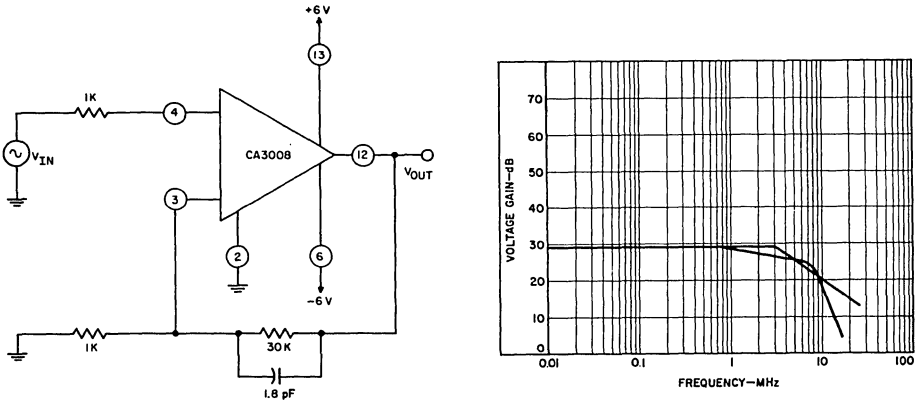



*Fig. 21—Circuit diagram and gain-frequency response of the 30-dB video amplifier when the phase compensation is accomplished by the addition of a capacitor in parallel with the feedback resistor.*

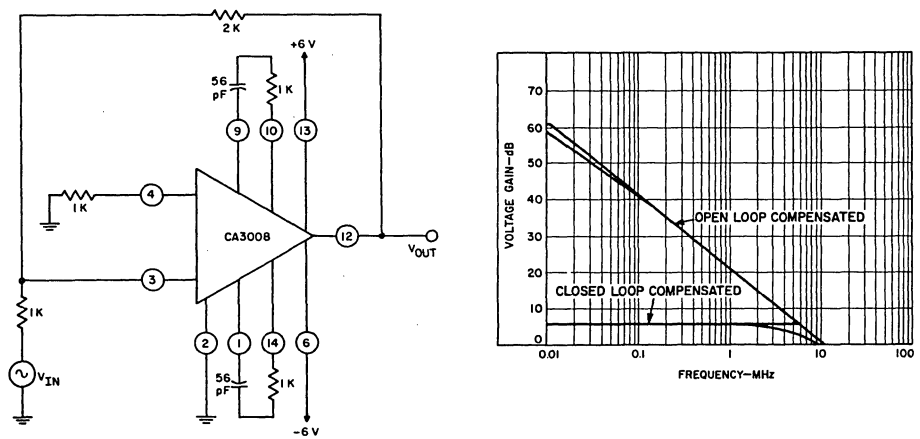



*Fig. 22—Circuit diagram and response of an inverting type of operational amplifier used as a 6-dB video amplifier.*

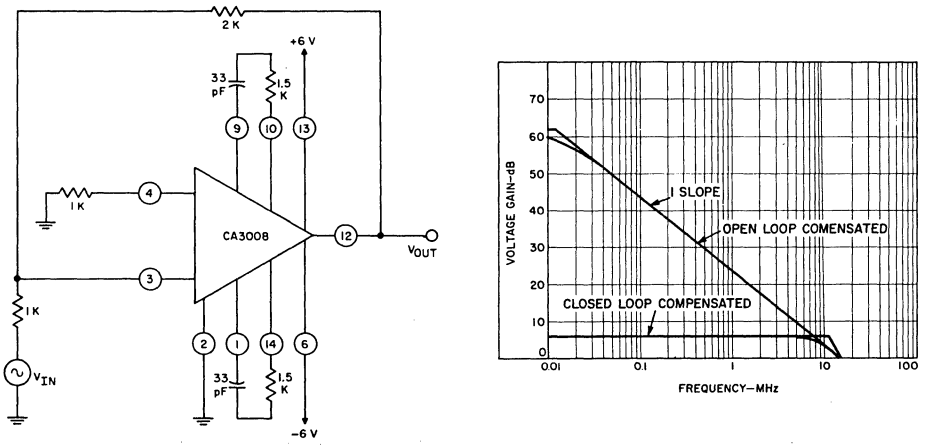



*Fig. 23—Effect of a decrease in the phase-compensating capacitance from 56 picofarads to 33 picofarads on the response of the 6-dB video amplifier.*

($Z_f/Z_i$) to roll off at a one slope. Fig. 21 illustrates this alternate technique for the 30-dB gain circuit.

The low-frequency input impedance of the 30-dB noninverting configuration is 480.000 ohms, as calculated from the appropriate equation in Fig. 16 ($Z_i$ = 14.000 ohms).

Fig. 22 shows the configuration and the response of a 6-dB inverting type of video amplifier. The intersection of the closed-loop characteristic with the compensated open-loop response predicts the 3-dB bandwidth of the video amplifier provided the transfer phase shift of the open-loop amplifier is approximately −90 degrees. This relationship suggests a way to extend the bandwidth without peaking. In the 6-dB video amplifier shown in Fig. 23, the 3-dB bandwidth has been increased from 5.6 MHz to 11 MHz by a decrease in the value of the phase-compensating capacitors from 56 picofarads to 33 picofarads.

Because a broadband amplifier should be capable of handling digital signals, data were taken to determine this capability. Figs. 24(a) and 24(b) illustrate the pulse-handling capabilities of the 30-dB noninverting circuit shown in Fig. 19. Fig. 24(a) shows the low-level (nonsaturating) pulse response. The input is a 38-millivolt, 960-nanosecond pulse; the output is a 1.1-volt pulse having a 40-nanosecond delay time, a zero storage time, and 125-nanosecond rise and fall times. Fig. 24(b) shows the response of the amplifier for a 960-nanosecond input pulse under 20-dB overdrive conditions. The output pulse has an amplitude of 3.2 volts, a delay time of 32 nanoseconds, a storage time of 160 nanoseconds, a rise time of 500 nanoseconds, and a fall time of 160 nanoseconds.

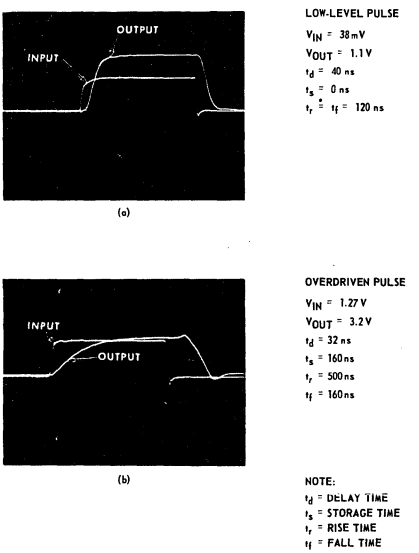



*Fig. 24—Pulse-handling characteristics of the noninverting 30-dB video amplifier: (a) Low-level pulse response; (b) Pulse response under overdrive conditions.*

## FREQUENCY-SHAPING AMPLIFIERS

The operational amplifiers may be used to create simple frequency-shaped characteristics, such as those associated with band-pass, notched-response, and single-tuned narrow-band amplifiers.

Fig. 25 shows a noninverting amplifier that may be used to synthesize the following peaked-response transfer function:

$$\frac{V_{out}}{V_{in}} = +10\,\frac{\left(1+j\frac{f}{f_1}\right)\left(1+j\frac{f}{f_4}\right)}{\left(1+j\frac{f}{f_2}\right)\left(1+j\frac{f}{f_3}\right)}$$

where $f_1 = 10$ kc/s, $f_2 = 40$ kc/s, $f_3 = 200$ kc/s, and $f_4 = 800$ kc/s.

In terms of the notations employed in Fig. 25, the break-frequency equations for the amplifier may be expressed as follows:

$$\frac{10}{2\pi C_r(R_f + 10R_r)} = 10\,\text{kHz}$$

$$\frac{1}{2\pi C_r R_r} = 40\,\text{kHz}$$

$$\frac{1}{2\pi C_n(R_n + R_f)} = 200\ \text{kHz}$$

$$\frac{40}{2\pi C_n(40R_n + R_f)} = 800\ \text{kHz}$$

These break-frequency equations are the precise equations derived from the gain equation in Fig. 16. The amount of phase compensation required is that shown in Fig. 18 for a noninverting gain of 20 dB.

Fig. 26 shows the circuit configuration and the frequency response of a narrow-band, 100-kHz tuned amplifier. The circuit Q is 33.3. A true single-tuned response can be obtained from only an inverting circuit configuration, as shown by the gain equation for the two types of configurations given in Figs. 15 and 16 and repeated below:

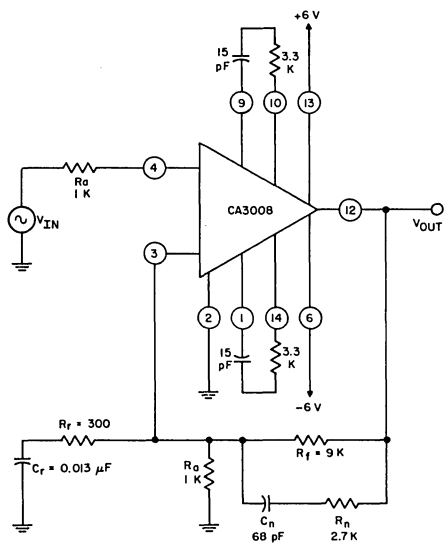
1. For the inverting configuration, the gain equation is given as:

$$\frac{V_{out}}{V_{in}} = -Z_f/Z_r$$

2. For the noninverting configuration, the following gain equation is used:

$$\frac{V_{out}}{V_{in}} = 1 + Z_f/Z_r$$

The "1+" term in the gain expression for the noninverting configuration indicates that the gain of this type of circuit will never decrease to zero as required for a true single-tuned response. The amount of phase compensation required for the narrow-band 100-kHz amplifier is the value given in Fig. 18 for an inverting gain of 0.0 (infinite attenuation).



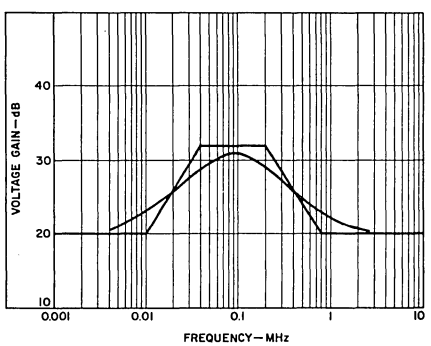
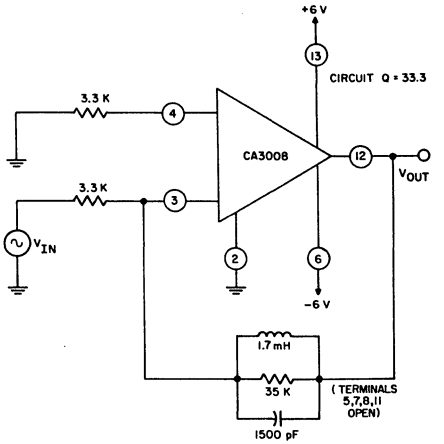
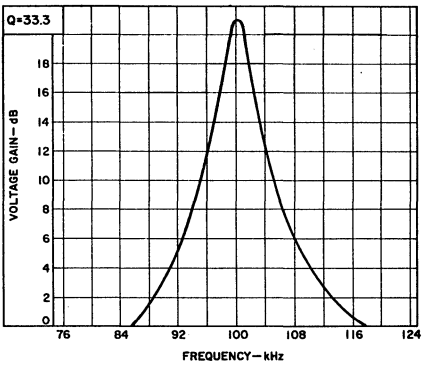




*Fig. 25—Circuit diagram and response of a noninverting type of operational amplifier used to synthesize peaked-response transfer functions.*




Phase Compensation not shown. It is 62 pF in series with 820 Ω between terminals 1 and 14 and between terminals 9 and 10.

*Fig. 26—Circuit diagram and response of an inverting type operational amplifier used as a narrow-band 100-kc/s tuned amplifier.*

## COMPARATOR CIRCUITS

The CA3008 and CA3010 Operational Amplifiers have excellent transfer characteristics for comparator applications. As shown in Fig. 8, the amplifiers have no observable hysteresis effect; the trace (minus to plus) and retrace (plus to minus) excursions coincide.

## INTEGRATORS

The important design consideration when an operational amplifier is to be used as an integrator is that dc feedback be provided. This feedback is necessary so that an offset (error) voltage cannot continuously charge the feedback capacitor until the amplifier limits. The required dc feedback is normally provided by shunting the integrating capacitor with a resistor so that the resulting time constant is considerably longer than the periods for the frequencies of interest. Fig. 27 shows the circuit configuration for the use of the CA3008 or CA3010 Operational Amplifier as an integrator and the responses of the circuit for 1-kHz square-wave inputs. The dc gain of the circuit is limited to 20 dB by the 39,000-ohm feedback resistor. The effect of this resistor on the gain, however, becomes negligible for ac signals at frequencies above 13 Hz because of the 0.03-microfarad capacitor in parallel with it. The weighting factor of integration for the circuit is about 1 millisecond (R = 39,000 ohms; C = 0.03 microfarad).

Phase compensation must also be provided in an integrating amplifier circuit to assure ac stability. In general, the amount of compensation required is the maximum value given by Fig. 18, because the closed-loop characteristic of the integrator has rolled off completely at the frequency where the intersection of the open-loop response and the closed-loop characteristic occurs.

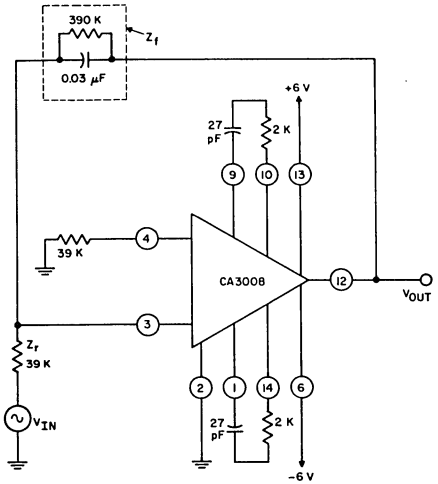
## DIFFERENTIATORS

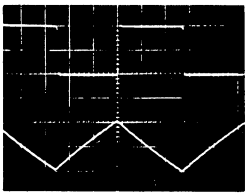
The main problem in the design of differentiating amplifiers is that the gain of such amplifiers increases with frequency; hence, they are susceptible to high-frequency noise. The classical remedy for this effect is to connect a small resistor in series with the input capacitor so that the high-frequency gain is decreased. Actually, the addition of the resistor results in a more realistic model of a differentiator because a resistance is always added in series with the input capacitor by the source impedance. The schematic diagram of a CA3008 or CA3010 Operational Amplifier used as a differentiating circuit and the response of the circuit for 1-kHz square waves are shown in Fig. 28. A value of 51 ohms is selected for the gain-limiting resistor to illustrate that the effect of the source impedance is not necessarily negligible in differentiator applications. This 51-ohm resistor limits the high-frequency numerical gain factor of the amplifier to 433.

If the closed-loop gain of a differentiator rises to the open-loop value before the open-loop response has started to roll off, no phase compensation of the circuit is required. In order to assure that the intersection of the closed-loop characteristic with the open-loop response occurs at a slope less than two, the RC time constant of the phase-compensating network must be adjusted so that the open-loop response does not roll off in the region of the intersection.

## SCALING ADDERS

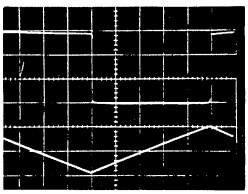
The inverting feedback configuration of the CA3008 and CA3010 Operational Amplifiers lends itself not only to summing several different signals, but also to weighting



f = 1Kc/s

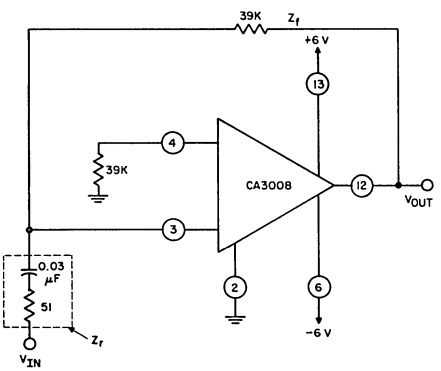
OUTPUT-0.2V/DIV.

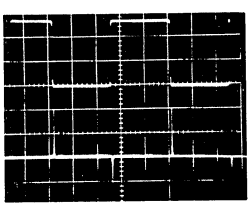


f = 10Kc/s

OUTPUT = 50mV/DIV.

*Fig. 27—Circuit diagram and the input and output waveforms for an operational amplifier used as an integrator.*



f = 1Kc/s

INPUT-2mV/DIV.

OUTPUT-1V/DIV.

*Fig. 28—Circuit diagram and the input and output waveforms for an operational amplifier used as a differentiator.*

each signal to be summed. The weighting operation is possible because the virtual ground that exists at the junction of the feedback resistor and the inverting input (terminal 3) isolates each signal channel from the others. The weighting operation requires that each input signal enters the virtual-ground node through an impedance of such value that its ratio to the feedback impedance is equal to the desired weighting factor.

Fig. 29 illustrates the use of the CA3008 or CA3010 Operational Amplifier as a scaling adder (weighting amplifier). This figure also shows a photograph of the output waveform. The minimum phase compensation needed for this circuit is that required for the gain obtained when a single signal drives all the input channels in parallel.

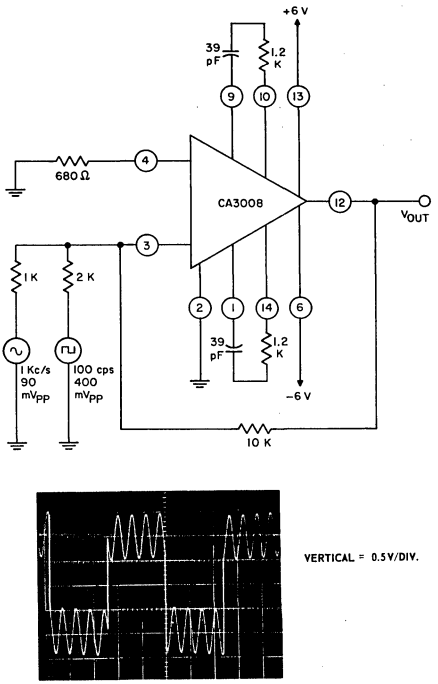



*Fig. 29—Circuit diagram and output waveform obtained when an operational amplifier is used as a scaling adder.*

## EXTERNAL MODIFICATIONS OF THE OPERATIONAL AMPLIFIERS

Although the CA3008 and CA3010 units meet all the requirements of an operational amplifier, there are special applications for which certain modifications are desirable. The two most common examples are applications in which the operational amplifier is required to supply high levels of output power and those for which the amplifier is operated with low dc input bias current.

### ADDITION OF A POWER-OUTPUT STAGE

The output-power capability of the operational amplifiers can be increased by the addition of an external emitter-follower output stage or a class B push-pull output stage. The emitter-follower approach is highly inefficient from a dissipation standpoint. A class B push-pull output stage, added as shown in Fig. 30, works well in a closed-loop circuit, but is subject to thermal runaway under open-loop conditions. The thermal-runaway effect may be controlled by the introduction of a small amount of emitter degeneration in each of the push-pull transistors. The load requirements, however, are sometimes severe enough to preclude the use of emitter degeneration. Moreover, depending on the choice of complementary transistors, the addition of the push-pull amplifier may limit the over-all bandwidth.

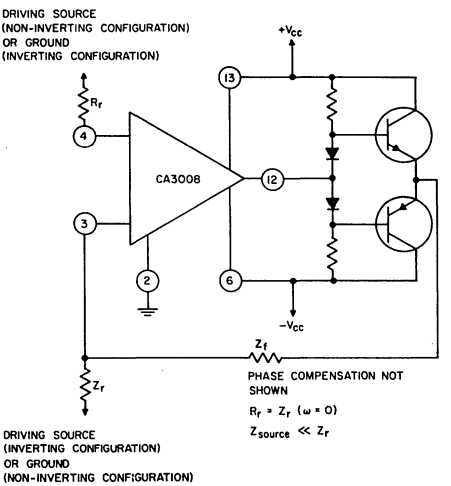



*Fig. 30—Schematic diagram showing the addition of an external push-pull output stage to increase the output capability of an operational amplifier.*

## ADDITION OF INPUT EMITTER FOLLOWERS

The dc input bias current of the operational amplifiers is required to be low when the amplifiers are driven either from a high-impedance source, such as a vidicon tube, or from a drive source that cannot accommodate high levels of dc current. The input bias current required is substantially decreased when emitter followers are added to the input terminals of the operational amplifiers. An emitter-follower modification to the operational amplifiers is illustrated in Fig. 31. The use of the emitter followers reduces the input-bias-current requirements from 5 microamperes per input to 0.14 microampere per input. This modification, however, also results in a decrease in the bandwidth, as indicated by the response curve for the modified circuit (see Fig. 31). The bandwidth is decreased because the emitter followers operate at very low levels of collector current and are driven from a high-impedance source (1 megohm for the circuit shown in Fig. 31).

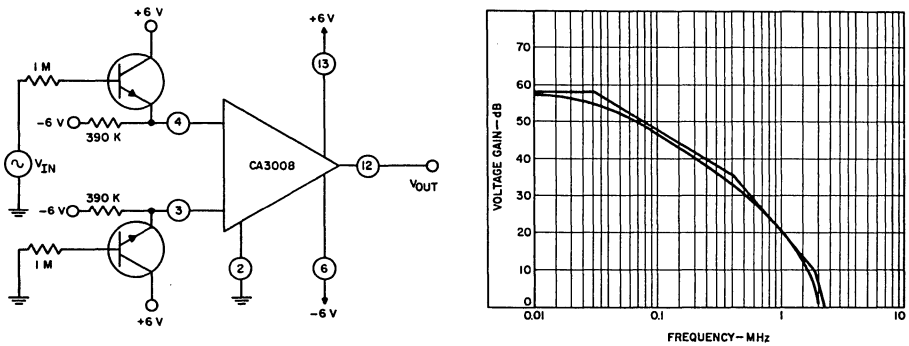



*Fig. 31—Schematic diagram showing the addition of input emitter followers to reduce the input-bias-current requirements of an operational amplifier.*

# Application of the RCA CA3004, CA3005, and CA3006 Integrated-Circuit RF Amplifiers

BY

M. E. MALCHOW AND G. E. THERIAULT

The RCA CA3004, CA3005, and CA3006 rf amplifiers are silicon-epitaxial monolithic integrated circuits, supplied in 12-terminal TO-5 packages. These circuits are designed to operate from low or medium levels of dc supply voltage, over a range of ambient temperatures from −55°C to +125°C, at frequencies from dc to 100 MHz. They may be used with external tuned-circuit, transformer, or resistive load impedances to provide the following types of functions:

1. Wide- or narrow-band amplification
2. Mixing
3. Limiting
4. Product detection
5. Frequency generation
6. Generation of pulse or digital waveforms

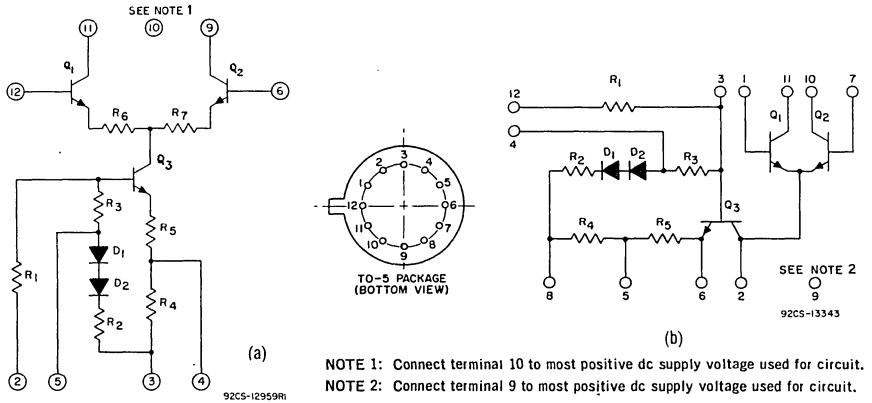
The CA3004 has linear transfer characteristics, excellent circuit stability, and a wide dynamic range. These features indicate that the CA3004 is particularly useful for applications in which the ability to handle large input signals is an important consideration.

The CA3005 and CA3006 feature high gain, sharp limiting characteristics, and exceptional versatility. The versatility in the operation of the CA3005 and CA3006 is made possible by the availability of internal circuit points to which external circuit elements may be connected to alter the basic circuit configuration. As a result of such external modifications, it is possible to operate these circuits as push-pull amplifiers, as cascode amplifiers, or as single amplifiers in cascade or parallel channels.

The CA3005 and CA3006 rf amplifiers are identical except for their input offset voltages. The offset voltage for the CA3006 is typically less than 1 millivolt, while the offset voltage for the CA3005 is normally in the order of 3 millivolts. The low level of input offset voltage makes the CA3006 well suited for balanced-modulator, mixer, or other push-pull applications that require a well-balanced circuit.

## CIRCUIT DESCRIPTIONS AND OPERATING MODES

Fig. 1 shows the schematic diagrams, together with the terminal arrangement on the TO-5 packages, for the CA3004, CA3005, and CA3006 integrated-circuit rf amplifiers. Each circuit consists of a balanced differential amplifier that is driven from a controlled, constant-current source.




NOTE 1: Connect terminal 10 to most positive dc supply voltage used for circuit.
NOTE 2: Connect terminal 9 to most positive dc supply voltage used for circuit.

*Fig. 1—Schematic diagrams of the integrated-circuit rf amplifiers: (a) CA3004; (b) CA3005 or CA3006. The terminal arrangement on the TO-5 package, which is the same for each type, is also shown.*

In the CA3004 circuit, resistors ($R_6$ and $R_7$) are included in the emitter leads of the differential pair of transistors, $Q_1$ and $Q_2$. The degeneration introduced by these unbypassed emitter resistors improves the linearity of the transfer characteristics and increases the signal-handling capabilities of the circuit. Fig. 2 shows the dynamic transfer and limiting

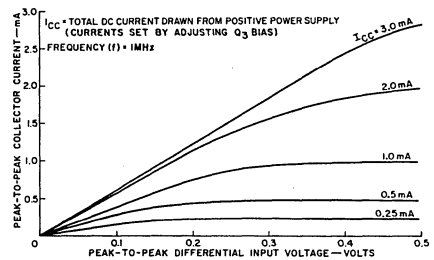



*Fig. 2—Dynamic transfer and limiting characteristics of the CA3004 integrated-circuit rf amplifier.*

characteristics of the CA3004. The characteristics show that linear operation is possible over a wide range of differential input voltage and, thus, indicate that relatively large input signals can be handled by the circuit without limiting.

In the CA3005 and CA3006 circuits, no emitter resistors are provided for the differential pair of transistors. As a result, these circuits have a smaller dynamic range and provide higher gain than the CA3004 circuit. The dynamic transfer and limiting characteristics of the CA3005 and CA3006, given in Fig. 3, show that these circuits are very good limiting amplifiers. A comparison of the curves in Fig. 3 with those given for the CA3004 in Fig. 2 emphasizes the excellent limiting characteristics of the CA3005 and CA3006.

## SUPPLY-VOLTAGE CONNECTIONS

The CA3004, CA3005, and CA3006 circuits may be operated, at various levels of supply voltage, from single or dual dc power supplies. For dual-supply operation, either symmetrical or nonsymmetrical power supplies may be used.

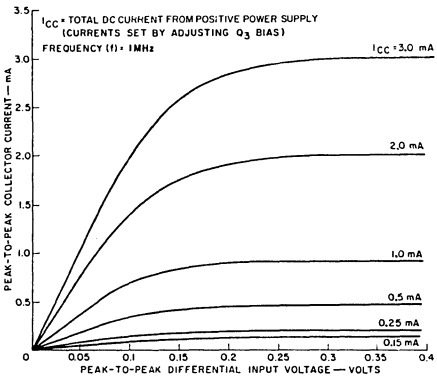



*Fig. 3—Dynamic transfer and limiting characteristics of the CA3005 or CA3006 integrated-circuit rf amplifier operated in the differential-amplifier configuration.*

Fig. 4 shows the supply-voltage connections for differential- and cascode-amplifier operation of the CA3005 or CA3006 from single and dual supplies. When two supplies, one for positive voltage and one for negative voltage, are used, as shown in Figs. 4(a) and 4(c), fewer external components are required. When only one supply is used, an external resistive voltage divider and bypass capacitor must

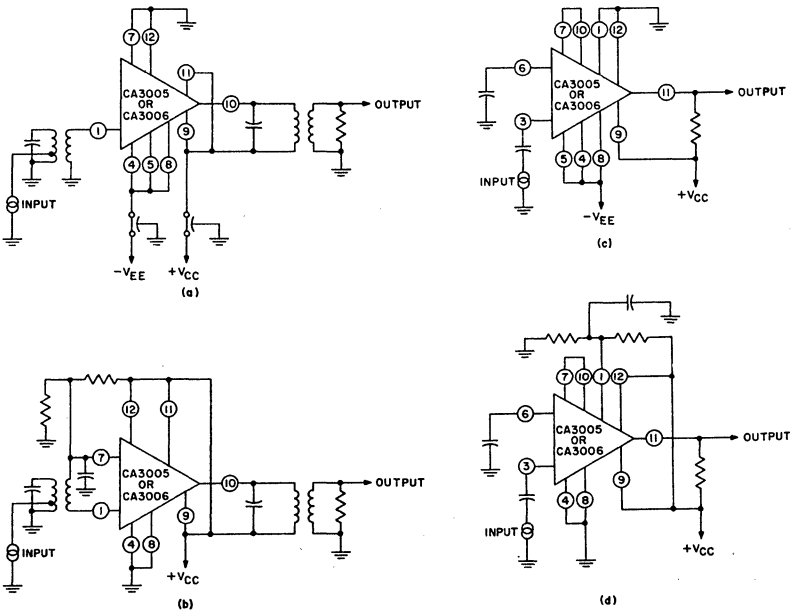



*Fig. 4—Schematic diagrams showing supply-voltage connections to the CA3005 or CA3006 for operation from either single or dual power supplies: (a) Differential-amplifier configuration operated from dual supplies; (b) Differential-amplifier configuration operated from a single supply; (c) Cascode configuration operated from dual supplies; (d) Cascode configuration operated from a single supply.*

be added to the circuit, as shown in Figs. 4(b) and 4(d). Tuned amplifiers that operate from dual supplies, such as that shown in Fig. 4(a), require the least number of external components.

For either single- or dual-supply operation, the operating current of transistor $Q_3$ is determined by the bias voltage, $V_{EE}$, applied between terminals 2 and 3 on the CA3004 or between terminals 8 and 12 on the CA3005 and CA3006 (refer to the circuit diagrams in Fig. 1). The more negative terminal of the bias-voltage source must be connected to terminal 3 on the CA3004 or to terminal 8 on the CA3005 and CA3006. In dual-supply systems, terminal 2 of the CA3004 and terminal 12 of the CA3005 and CA3006 are usually returned to dc ground.

## OPERATING MODES

For any given bias voltage $V_{EE}$, there are four possible operating modes for the integrated-circuit rf amplifiers. In general, each mode is characterized by (1) a distinct level of operating current and corresponding transconductance, (2) the degree of dependence of the operating current on temperature, and (3) the way in which the transconductance is affected by temperature. The operating points for the various modes are established by:

1. The emitter resistance selected for the constant-current-source transistor, $Q_3$;
2. Whether the base-bias network includes the diodes shown in Fig. 1.
3. The magnitude of the bias voltage, $V_{EE}$, applied to the circuit.

Table I lists the required conditions for the four operating modes, designated A, B, C, and D. The following paragraphs describe the characteristics of the circuits in each operating mode. The data are given for operation of the circuits from symmetrical dual power supplies at three levels of dc supply voltage (±3 volts, ±4.5 volts, and ±6 volts).

Fig. 5 shows the operating current for the various modes as a function of temperature. The current-temperature data show that, in addition to the obvious shift in the level of operating current, the dependence of the operating current on temperature varies significantly with a change in the operating mode.

When the diodes are included in the base-bias circuit

TABLE I

Required Conditions for Each Operating Mode of the CA3004, CA3005, and CA3006 Integrated-Circuit RF Amplifiers

| *Operating Mode** | *CA3004 Terminals Shorted To Terminal 3* | *CA3005 or CA3006 Terminals Shorted To Terminal 8* | *Diodes In or Out of Bias Circuit* | *Q-3 Emitter Resistor(s)* |
|---|---|---|---|---|
| A | — | — | In | $R_4 + R_5$ |
| B | 5 | 4 | Out | $R_4 + R_5$ |
| C | 4 | 5 | In | $R_5$ |
| D | 4, 5 | 4, 5 | Out | $R_5$ |

*For all modes, terminals 2, 6, and 12 of the CA3004 and terminals, 1, 7, and 12 of CA3005 and CA3006 are grounded.

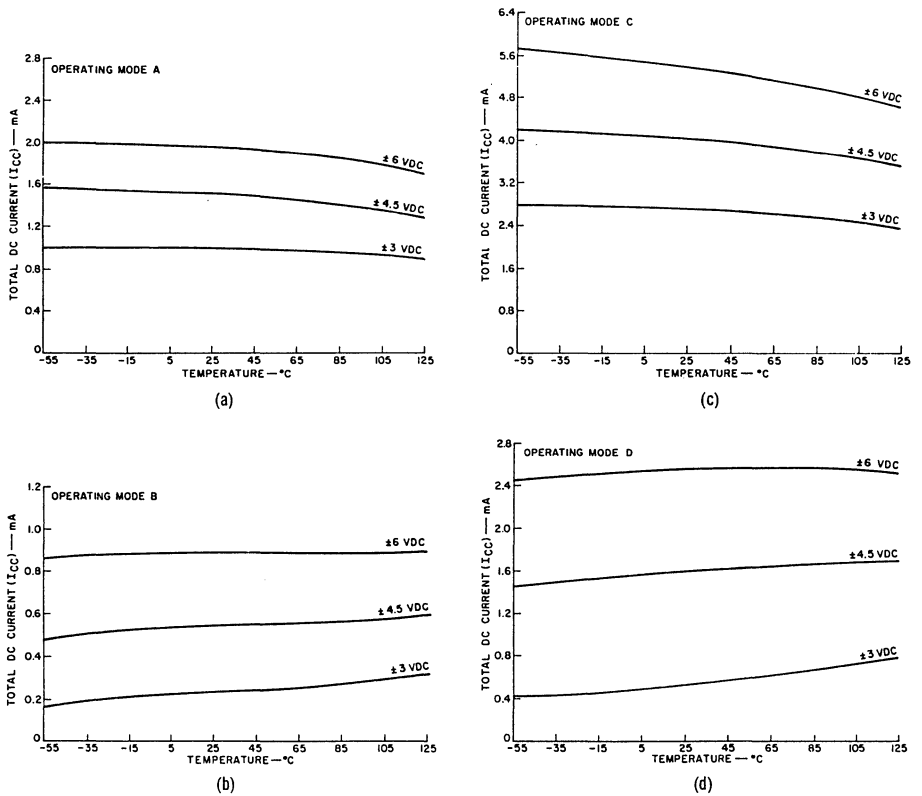



*Fig. 5—Variation in the operating currents of the CA3004, CA3005, or CA3006 as a function of temperature for each mode of operation.*

(modes A and C), the operating current, which is primarily dependent on the temperature coefficient of the diffused emitter resistor, tends to decrease with an increase in temperature at a rate that is relatively independent of the bias supply voltage $V_{EE}$. When the diodes are not used, however, the shape of the current-temperature curves is dependent on the magnitude of the supply voltage $V_{EE}$. The operating current then may remain constant or rise as the temperature is increased, depending upon the value of $V_{EE}$. The positive supply voltages, shown in Fig. 5, have no effect on the operating current, and the current-temperature curves are not changed by increases or decreases in this voltage. Some deviation in the current-temperature curves is to be expected because of normal variations in the absolute resistor values.

Fig. 6 shows the effects of different operating modes and variations in temperature on the single-ended transconductance* of the CA3004. In general, when diodes are used in the base-bias network, the transconductance decreases with increases in temperature. If the diodes are not used, the transconductance may decrease, increase, or remain constant as the temperature increases, depending on the value of the negative supply voltage $V_{EE}$. With the diodes out, however, the collector operating point tends to shift when resistive loads are used. In applications that require a stable collector dc operating point, therefore, operating mode A or C (diodes in) should be used.

Fig. 7 shows transconductance-temperature curves for each operating mode of the CA3005 or CA3006, operated in a differential-amplifier configuration. These transconductance curves differ from those for the CA3004 shown in Fig. 6 primarily because of the emitter resistors used in the CA3004. For each operating mode, the operating points for the differential-amplifier configuration of the CA3005 or CA3006, as well as for the CA3004, provide a current in each collector of the differential pair of transistors that is equal to one-half that shown in Fig. 5.

In a cascode configuration of the CA3005 or CA3006, the current through each part of the common emitter-common

*The single-ended transconductance is the incremental output current for one collector of the differential pair of transistors divided by the incremental input voltage. The curves shown of this parameter are obtained at an operating frequency of 1 MHz.

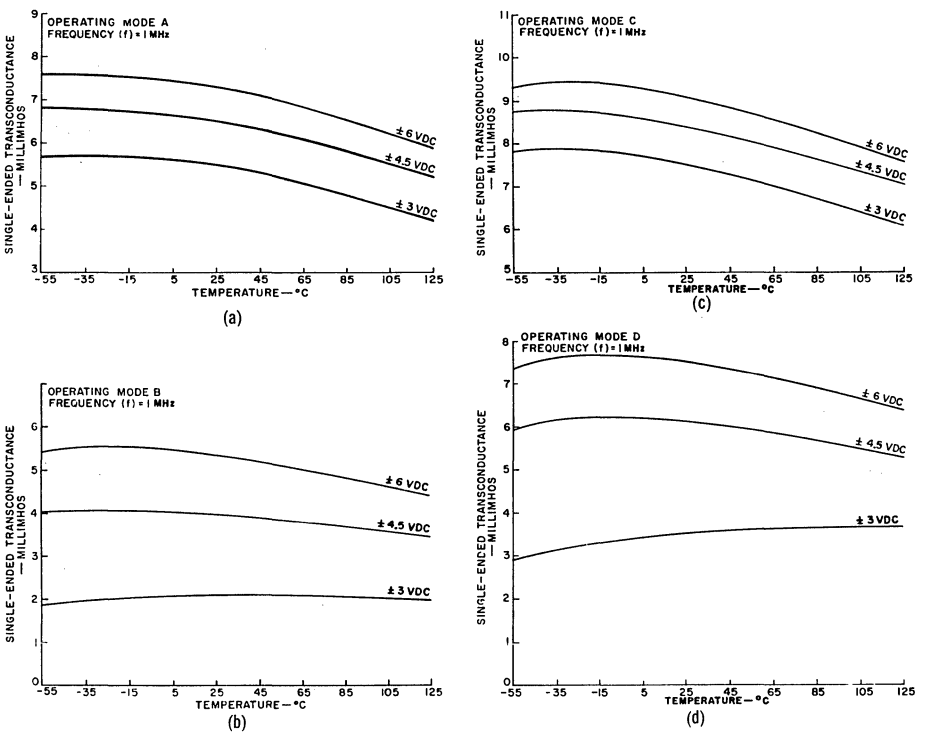



*Fig. 6—Variation in the single-ended transconductance of the CA3004 as a function of temperature for each operating mode.*

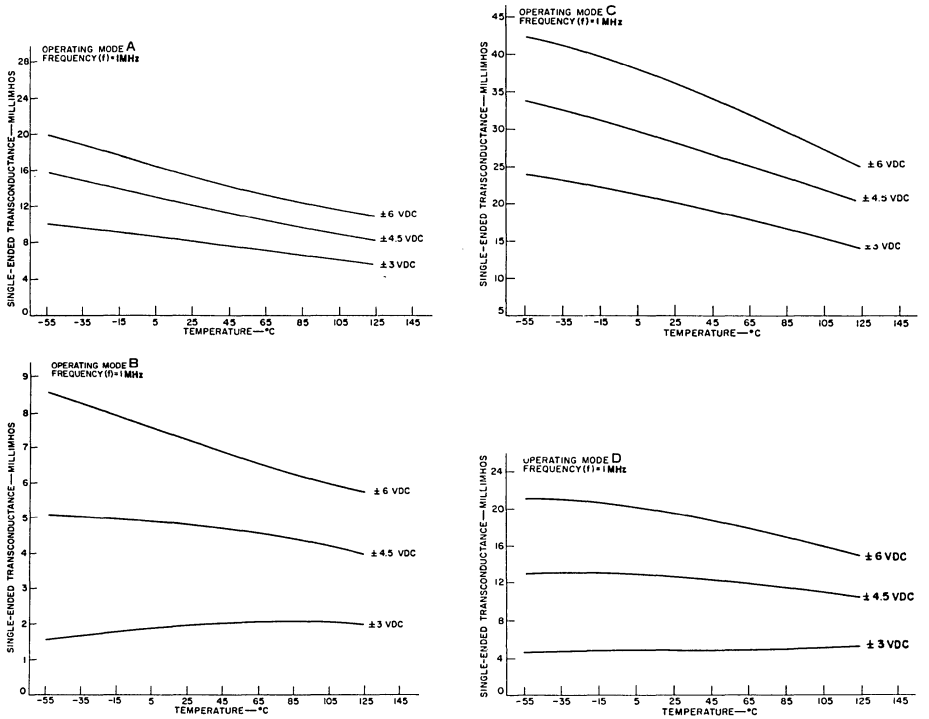



*Fig. 7—Variation in the single-ended transconductance of the CA3005 or CA3006 in a differential-amplifier configuration as a function of temperature for each operating mode.*

base cascode is equal to the total current shown in Fig. 5 in each mode. Fig. 8 shows the transconductance-temperature curves for each operating mode of the cascode circuit. These curves show that, in general, the transconductance is higher when the diodes are included in the base-bias network (modes A and C) than it is when the diodes are not used (modes B and D).

The power dissipation of the CA3004, CA3005, or CA3006 is highest when the circuit is operated in mode C. Table II shows power dissipation and the single-ended transconductance of the circuits for each operating mode. These data may be used to determine the operating point that provides the highest value of transconductance per milliwatt of circuit dissipation for given design conditions.

## CHARACTERISTICS OF THE RF AMPLIFIER CIRCUITS

### Y PARAMETERS

In the design of rf and if circuits, the four-terminal black-box short-circuit admittance parameters have become a valuable tool. The determination of stability criteria, input and output impedances as a function of load and source admittance, power gain, and voltage gain in iterative connections are all facilitated by a knowledge of the "y" parameters.

The "y" parameter curves presented in this section have been calculated from a model and verified at several points by measurements. These curves are a valuable aid in the design of systems that use integrated circuits. The admittance curves are all generated for a quiescent operating current of 1.25 milliamperes in each of the transistors $Q_1$ and $Q_2$ in the differential-amplifier configurations and for a current of 2.5 milliamperes in transistor $Q_3$ in the cascode configuration. This operating current is obtained in the operating mode D, as defined in the preceding section, with supply voltages of ±6 volts.

The "y" parameters and their symbols are listed below:

1. Input admittance with the output voltage constant

$$y_i = g_i + jb_i$$

where $y_i$ is the complex input admittance, $g_i$ is the input conductance and $b_i$ is the input susceptance.

TABLE II

Relationship Between the Transconductance and the Power Dissipation of the Integrated-Circuit RF Amplifiers in Each Operating Mode*

| *Operating Mode* | *Type of Circuit* | *DC Supply Voltages (volts)* | *Single-Ended Transconductance (millimhos)* | *Power Dissipation (milliwatts)* |
|---|---|---|---|---|
| A | CA3004 | ±3 | 5.5 | 6.6 |
| | CA3005 or CA3006 | | 8.5 | 6.6 |
| | CA3004 | ±4.5 | 6.7 | 15.0 |
| | CA3005 or CA3006 | | 12.8 | 15.0 |
| | CA3004 | ±6 | 7.3 | 25.0 |
| | CA3005 or CA3006 | | 15.0 | 25.0 |
| B | CA3004 | ±3 | 1.6 | 2.3 |
| | CA3005 or CA3006 | | 1.9 | 2.3 |
| | CA3004 | ±4.5 | 4.0 | 7.2 |
| | CA3005 or CA3006 | | 4.9 | 7.2 |
| | CA3004 | ±6 | 5.3 | 15.0 |
| | CA3005 or CA3006 | | 7.2 | 15.0 |
| C | CA3004 | ±3 | 7.5 | 17.5 |
| | CA3005 or CA3006 | | 22.0 | 17.5 |
| | CA3004 | ±4.5 | 8.5 | 40.0 |
| | CA3005 or CA3006 | | 29.0 | 40.0 |
| | CA3004 | ±6 | 9.1 | 62.8 |
| | CA3005 or CA3006 | | 37.0 | 62.8 |
| D | CA3004 | ±3 | 3.3 | 4.2 |
| | CA3005 or CA3006 | | 5.0 | 4.2 |
| | CA3004 | ±4.5 | 6.0 | 17.4 |
| | CA3005 or CA3006 | | 13.0 | 17.4 |
| | CA3004 | ±6 | 7.2 | 35.9 |
| | CA3005 or CA3006 | | 20.0 | 35.9 |

*Circuits are operated in differential-amplifier configurations. The transconductances and power dissipations shown are calculated values for nominal units.

2. Output admittance with the input voltage constant

$$y_o = g_o + jb_o$$

where $y_o$ is the complex output admittance, $g_o$ is the output conductance, and $b_o$ is the output susceptance.

3. Forward-transfer admittance with the output voltage constant

$$y_f = g_f + jb_f$$

where $y_f$ is the complex forward-transfer admittance, $g_f$ is the forward-transfer conductance, and $b_f$ is the forward-transfer susceptance.

4. Reverse-transfer admittance with the input voltage constant

$$y_r = g_r + jb_r$$

where $y_r$ is the complex reverse-transfer admittance, $g_r$ is the reverse-transfer conductance, and $b_r$ is the reverse-transfer susceptance.

A comparison of the parameters of the various possible circuit configurations with those of the more familiar common-emitter parameters requires a second subscript to indicate the type of configuration being considered. Examples of the use of the second-subscript notation are given below:

The common-emitter reverse-transfer admittance is written as

$$y_{re} = g_{re} + jb_{re}$$

The differential-amplifier reverse-transfer admittance is expressed as

$$y_{rDA} = g_{rDA} + jb_{rDA}$$

The cascode-amplifier reverse-transfer admittance is given as

$$y_{rCAS} = g_{rCAS} + jb_{rCAS}$$

These cumbersome second subscripts will not be used when the type of circuit for which the parameter is given is clearly indicated by an illustration or a descriptive phrase in the text.

In general it is valuable to understand the essential differences between the "y" parameters of a regular common-emitter stage and those of the compound stages, such as differential and cascode amplifiers.

The differential amplifier, when used at radio frequencies, consists essentially of a common-collector stage that drives a common-base stage. In comparison to the regular, common-emitter "y" parameters, the input admittance $y_i$ the output admittance $y_o$, and the forward transfer admittance $y_f$, are decreased, almost exactly, by a factor of two when the differential-amplifier configuration is used.

The reverse-transfer admittance $y_r$ is also less for the differential amplifier than for the single transistor in the common-emitter configuration. The ratio of the imaginary term in the differential-amplifier admittance to that of the single transistor is 1/140 at low frequencies and 1/10 at 100 MHz. Fig. 9 shows the ratios of imaginary parts

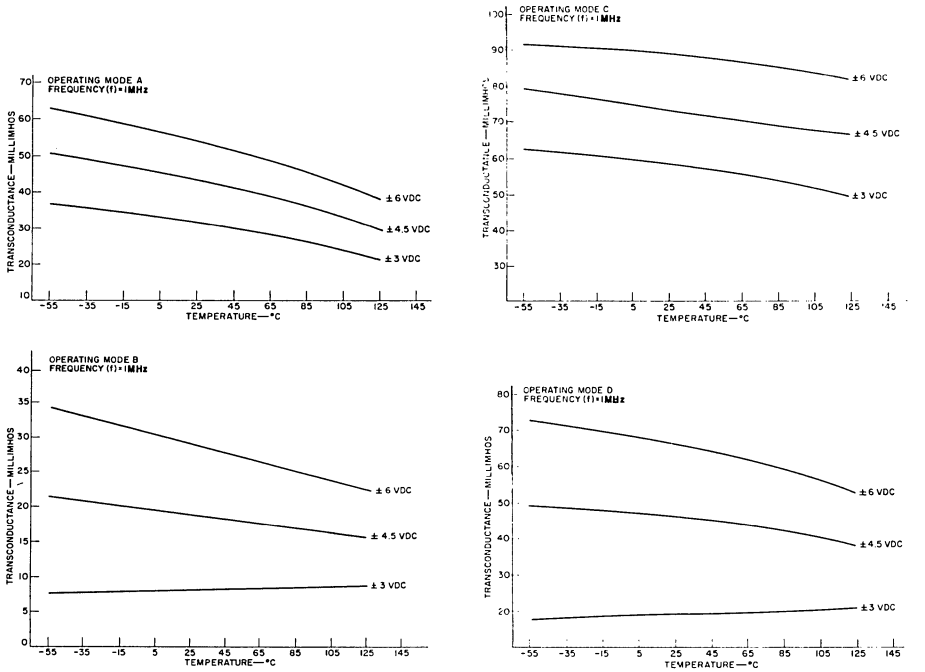



*Fig. 8—Variation in the transconductance of the CA3005 or CA3006 in a cascode configuration as a function of temperature for each operating mode.*

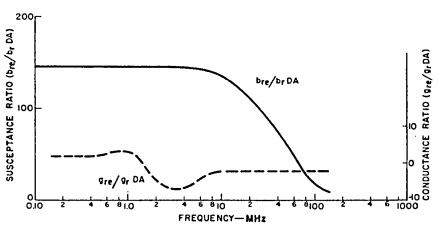



*Fig. 9—Ratio of the real (conductance) and the imaginary (susceptance) parts of the reverse-transfer admittance for a common-emitter stage to those for a differential-amplifier stage as a function of frequency.*

$b_{re}/b_{rDA}$ and real parts $g_{re}/g_{rDA}$ of the reverse-transfer admittances as a function of frequency.

In the cascode configuration of the rf amplifier circuits, a common-emitter stage drives a common-base stage. The input admittance $y_i$ is, therefore, that of a common-emitter stage. The forward-transfer admittance $y_f$ is that of a common-emitter stage times alpha. Because of the high-impedance drive source on the common-base stage, the output admittance $y_o$ is very low (0.06 x $10^{-5}$ mhos) at low frequencies and is both negative and low at high frequencies. Since the output admittance is low and may be negative, a conjugate match cannot be obtained at the output. Practical amplifiers are possible however, provided that the sum $Y_{out} + Y_{load}$ is positive.

The reverse-transfer admittance $y_r$ for the cascode circuit is less than that for the single-stage common-emitter

circuit. The ratio of the imaginary terms of these admittances is 1/1200 at low frequencies and 1/35 at 100 MHz. The ratios of the real parts and of the imaginary parts as a function of frequency are shown in Fig. 10.

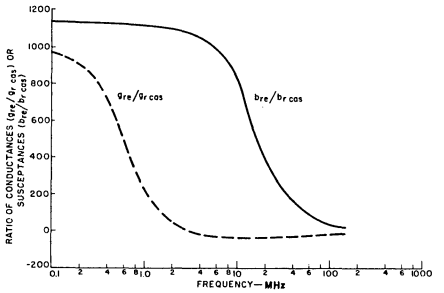



*Fig. 10—Ratio of the real (conductance) and the imaginary (susceptance) parts of the reverse-transfer admittance for a common-emitter stage to those for a cascode stage as a function of frequency.*

Although the $y_r$ is low for both the differential and cascode configurations, instability can occur in high-gain amplifiers. A further consideration in high-gain circuits is that the layout can contribute more feedback than the integrated circuit. Shielding and layout therefore are of prime importance if proper advantage is to be taken of the low feedback of these circuits.

The computed y parameters for the CA3004 differential amplifier are shown in Fig. 11. The admittance parameters for differential-amplifier operation of the CA3005 or CA3006 are given in Fig. 12 and those for cascode-amplifier operation of either circuit are given in Fig. 13.

## VIDEO-AMPLIFIER CAPABILITIES

The CA3004, CA3005, and CA3006 integrated circuits may be used as video amplifiers, as shown in Figs. 14(a) and 14(b). A relatively large number of external components is required, and the availability of internal-circuit connections for these external components provides a large degree of flexibility to the user with respect to such factors as bandwidth, gain, power dissipation and peaking. In the circuit shown in Fig. 14(a), $R_1$ should be equal to $R_2$ to preserve the circuit balance, and $C_2$ should be an adequate bypass so that the noise factor and gain are not degraded. For the cascode configuration shown in Fig. 14(b), $C_2$ is an emitter bypass, and its reactance should be less than 1.5 ohms at the lowest video frequency to be handled.

In either cascode or single-ended differential-amplifier configurations, the feedback is low. Each configuration provides good isolation from output to input; the high frequency performance therefore can be approximated from the input and output parallel R and C for a single stage or from the total shunt R and C between stages for an iterative connection. The mid-frequency voltage gain can be computed from the familiar $g_m R_L$ product. As an aid to such calculations, Table III gives the input and output parallel R and C and the absolute values of $g_m$ for the various circuits and configurations for operation at 1, 10, and 40 MHz. For more precise, but more elaborate calculations, the $y$ parameters may be used for video-amplifier design.

## NOISE PERFORMANCE

The noise figure of the CA3004, CA3005 and CA3006 integrated-circuit rf amplifiers is a function of the dc operating current and frequency, for both differential and cascode-amplifier configurations. The noise figure increases both with an increase in current and with an increase in fre-

TABLE III

Input and Output Parallel RC Network, Transconductance, and Performance Data for the CA3004, CA3005, and CA3006 Integrated-Circuit RF Amplifiers

| | | | | | | *VIDEO PERFORMANCE (Simulated Iterative Connection)* | | | |
|---|---|---|---|---|---|---|---|---|---|
| *Freq. (MHz)* | *Input Parallel RC* $R_{in}$ *(ohms)* | $C_{in}$ *(pF)* | *Output Parallel RC* $R_{out}$ *(ohms)* | $C_{out}$ *(pF)* | *Transconductance,* $g_m$ *(millimhos)* | *Interstage* $R_L$ *(ohms)* | *High-Freq. 3-dB Point (MHz)* | *Mid-Band Voltage Gain (dB)* | |
| CASCODE OPERATION (CA3005 OR CA3006) | | | | | | | | | |
| 1 | 500 | 42 | —1.67 X $10^6$ | 3.0 | 78 | | 23 | 19.3 | Measured |
| 10 | 500 | 42 | —1.67 X $10^6$ | 3.0 | 77 | 150 | | | |
| 40 | 180 | 22 | —6 X $10^5$ | 3.0 | 58 | | 20 | 20.6 | Calculated |
| DIFFERENTIAL-AMPLIFIER OPERATION (CA3005 OR CA3006) | | | | | | | | | |
| 1 | 2500 | 16 | $10^5$ | 4.0 | 20 | | 18 | 19.5 | Measured |
| 10 | 1800 | 13 | 4 X $10^4$ | 4.0 | 20 | 500 | | | |
| 40 | 670 | 10.5 | 2800 | 7.6 | 18.6 | | 16 | 20.0 | Calculated |
| DIFFERENTIAL-AMPLIFIER OPERATION (CA3004) | | | | | | | | | |
| 1 | 6650 | 8 | 1.7 X $10^5$ | 6.5 | 7.8 | | 18.4 | 17.2 | Measured |
| 10 | 6650 | 6.2 | $10^5$ | 6.1 | 7.8 | 1000 | | | |
| 40 | 2000 | 5.0 | 2 X $10^4$ | 6.8 | 7.6 | | 15 | 18.0 | Calculated |

Data obtained for circuits operated from ±6-volt dc supplies in operating mode D.

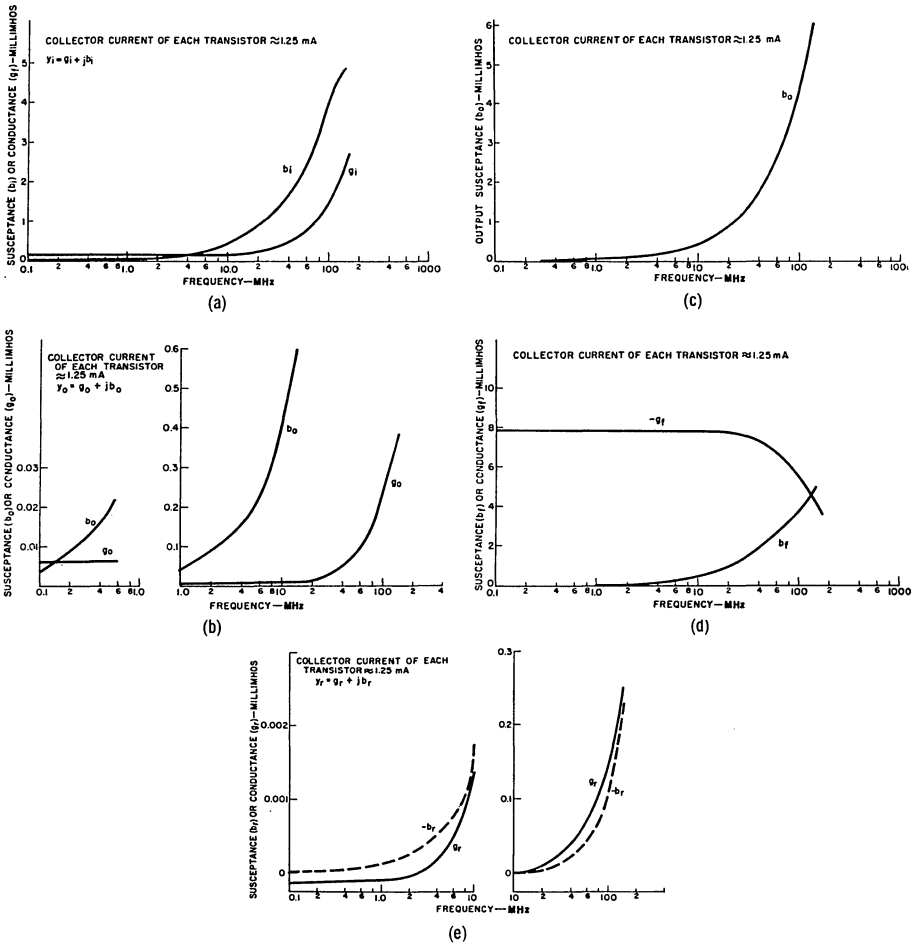



*Fig. 11—Admittance characteristics of a CA3004 differential amplifier as a function of frequency: (a) Input admittance, $y_i$; (b) Output admittance, $y_o$; (c) Output susceptance, $b_o$, above 10 MHz; (d) Forward-transfer admittance, $y_f$; (e) Reverse transfer admittance, $y_r$.*

quency. For convenience, noise data were taken in a fixed configuration as the negative supply voltage was varied. On the data plots, the operating currents that correspond to the various supply voltages are included as a separate abscissa to show that the noise figure is a direct function of operating current. Figs. 15 and 16 show representative noise-figure data for tuned amplifiers in the differential and cascode configuration, respectively. In each case, the input and output are tuned and the input is conjugately matched to a 50-ohm noise diode. Practically no change in noise figure occurs with variations of the positive supply voltage $V_{CC}$.

The curves in Figs. 15 and 16 show that, for optimum single-stage noise performance, the operating current should be low, which results in a low gain. Thus, in system applications of the tuned amplifiers, the operating current in each stage should be adjusted to obtain the optimum overall noise

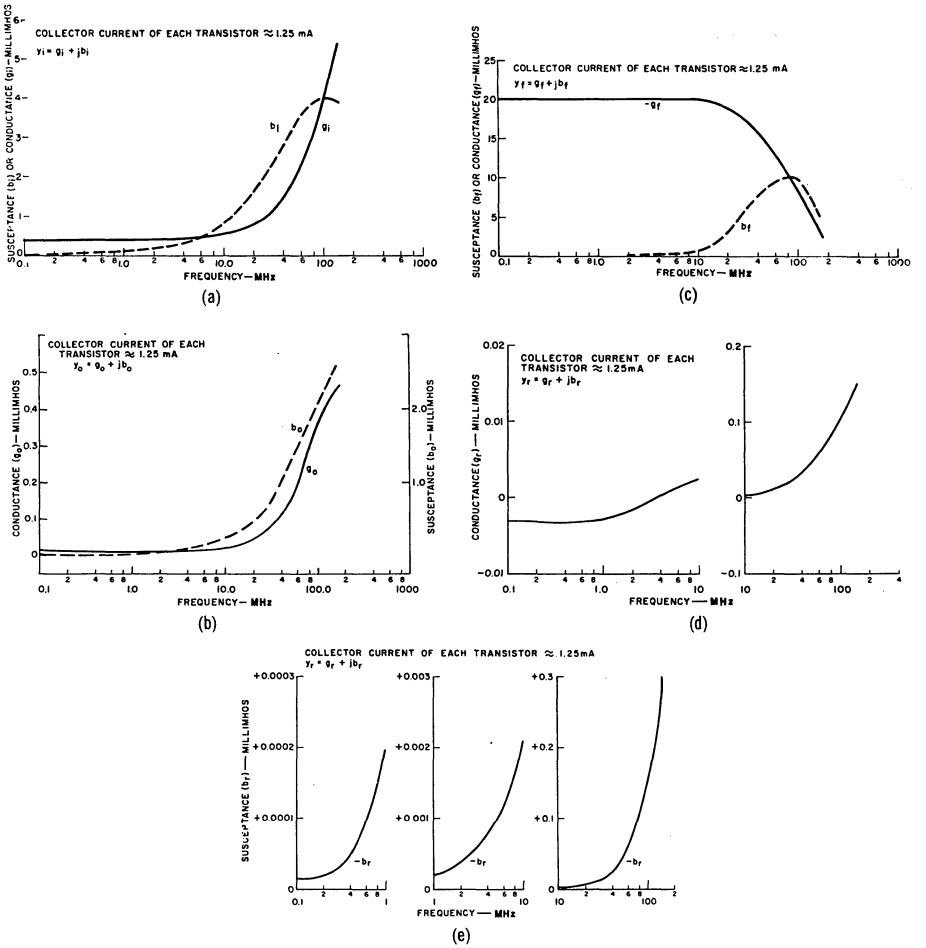



*Fig. 12—Admittance characteristics of a CA3005 or CA3006 differential amplifier as a function of frequency: (a) Input admittance, $y_i$; (b) Output admittance, $y_o$; (c) Forward transfer admittance, $y_f$; (d) Reverse transfer conductance, $g_r$; (e) Reverse transfer susceptance, $b_r$.*

figure by considering the gain and noise figure of the first stage and the noise figure of the second stage. The operating-current adjustment can be accomplished by a change in the negative-supply voltage ($V_{EE}$) or by means of the bias connections that are available.

Fig. 17 shows the noise figure as a function of the source resistance for a CA3005 or CA3006 used as a differential amplifier at an operating frequency of 12 MHz. The equation given in the figure can be used to predict noise performance as a function of source resistance for dc operating conditions. The load resistor $R_L$ of the circuit is 2200 ohms and $R_N$ = 800 ohms. ($R_N$ is the equivalent noise resistance).

## COMMON-MODE REJECTION RATIO

The common-mode rejection ratio of a differential amplifier, defined as the ratio between the full differential gain

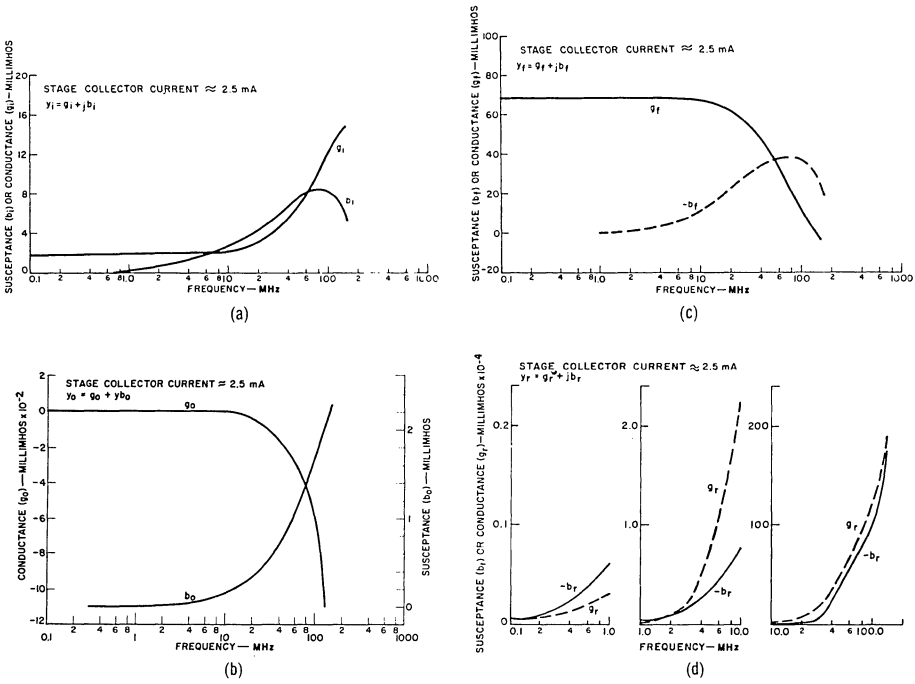



*Fig. 13—Admittance characteristics of a CA3005 or CA3006 cascode amplifier as a function of frequency: (a) Input admittance, $y_i$; (b) Output admittance, $y_o$; (c) Forward transfer admittance, $y_f$ (d) Reverse transfer admittance, $y_r$.*

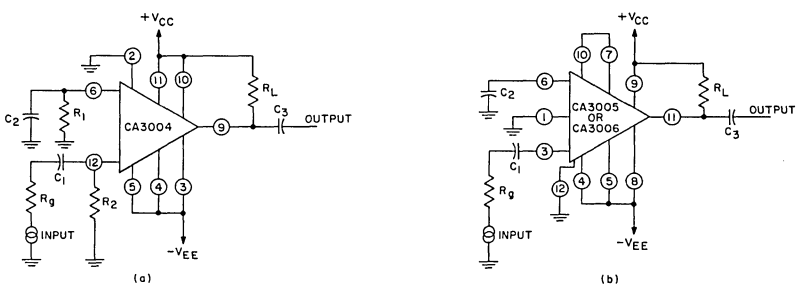



*Fig. 14—Schematic diagrams showing the use of the integrated-circuit rf amplifiers as video amplifiers: (a) CA3004 in a differential-amplifier configuration; (b) CA3005 or CA3006 in a cascode-amplifier configuration.*

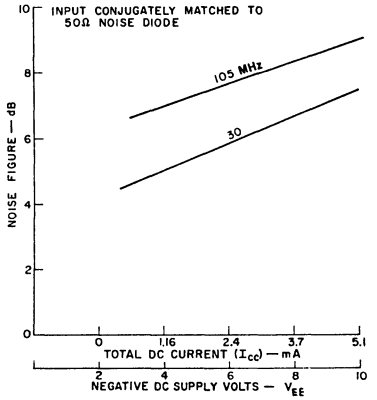



*Fig. 15—Representative noise performance of the CA3004, CA3005, or CA3006 operated in a differential-amplifier configuration (operating mode D).*

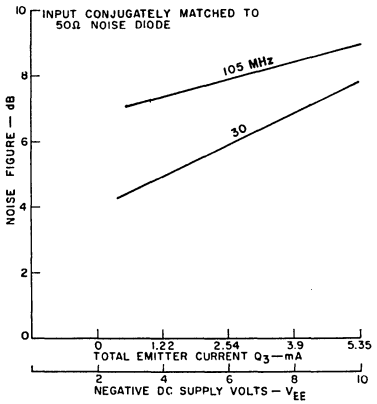



*Fig. 16—Representative noise performance of the CA3005 or CA3006 operated in a cascode-amplifier configuration (operating mode D).*

and the common-mode gain, is a useful performance characteristic. The common-mode rejection is a function of the ratio of the impedance of the constant-current transistor $Q_3$ to the load resistor. The common-mode rejection decreases if the signal applied is large enough to saturate the constant-current transistor. The maximum peak-to-peak input voltage, therefore, is a function of the supply voltages and the bias connections of the constant-current transistor. The common-mode rejection for a 1-kHz signal is shown in Table IV.

TABLE IV

Common-mode Rejection Ratio for the CA3004, CA3005, and CA3006 Integrated-Circuit RF Amplifiers

| | *At −55°C* | *At 25°C* | *At 125°C* |
|---|---|---|---|
| CA3004 | 102 dB | 98 dB | 101 dB |
| CA3005 or CA3006 | 108 dB | 101 dB | 107 dB |

Operating frequency = 1 kc/s.
Load resistance, $R_L$ = 1000 ohms in each collector.

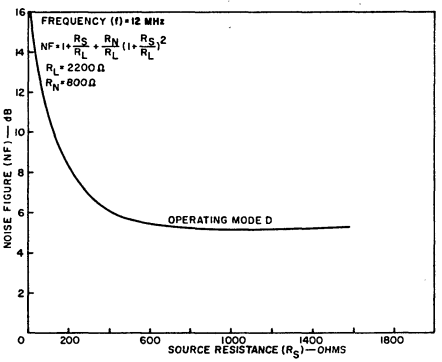



*Fig. 17—Noise figure of the CA3005 or CA3006 in a differential-amplifier configuration as a function of the source resistance (operating mode D).*

Fig. 18 shows the single-ended common-mode gain* for the CA3004, CA3005, and CA3006 as a function of frequency. (Fig. 19 shows the method used to determine the single-ended common-mode gain.) The common-mode rejection decreases with increasing frequency when the CA3004, CA3005, and CA3006 are operated with a single-ended output.

## GAIN CONTROL

The gain of the CA3004, CA3005, and CA3006 circuits may be controlled in either of two ways: (1) The negative voltage applied to the base-bias resistor $R_1$ can be adjusted to vary the current in transistor $Q_3$ or (2) A differential offset voltage can be applied to transistors $Q_1$ and $Q_2$. In both techniques, the gain-control voltage has a ground reference in a two-supply system, and maximum gain is obtained at 0 volts. The first method provides greater gain-control range but also requires more control voltage than the second method. Figs. 20 and 21 show the typical gain control as a

*Single-ended common-mode gain: The ratio of the change in the single-ended output voltage, measured from either output terminal with respect to ground, to the change in the input voltage applied simultaneously to both inputs of the circuit, i.e., single-ended common-mode gain $= \Delta V_{in}/\Delta V_{out}$, as shown in Fig. 19.

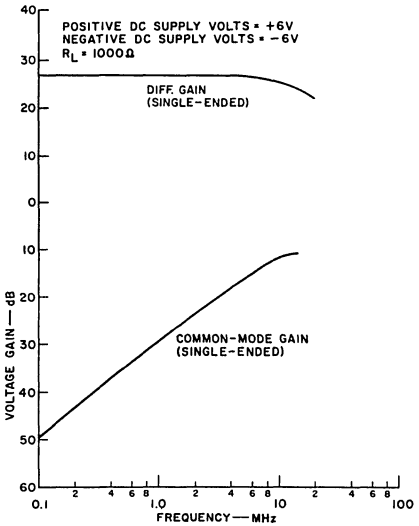



*Fig. 18—Single-ended common-mode and differential-mode gains of the CA3004, CA3005, or CA3006 as a function of frequency.*

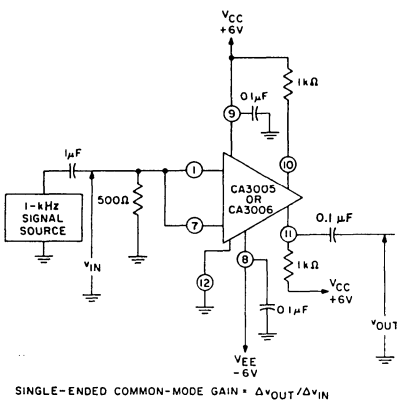



*Fig. 19—Schematic of the circuit used to determine the single-ended common-mode gain.*

function of voltage for the CA3005 or CA3006 for the two methods. Fig. 20 gives the gain-control characteristic for the CA3005 or CA3006 when the gain-control voltage is applied to the base-bias network of transistor $Q_3$. Since the

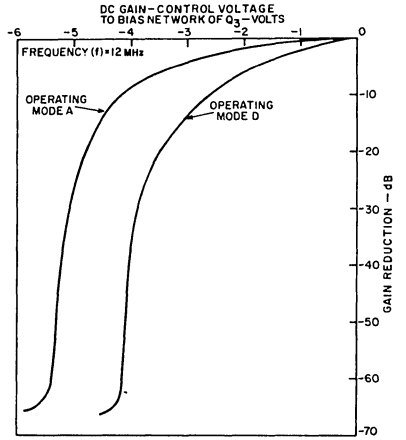



*Fig. 20—Gain-control characteristics of the CA3005 or CA3006 as a function of the dc gain-control voltage applied to the bias network of transistor $Q_3$.*

$Q_3$ bias networks are the same, the gain characteristics for the CA3004 are nearly the same as those for the CA3005 and CA3006. Fig. 21 shows that in the offset method of gain control the gain range is dependent on the polarity of drive. For maximum gain-control range on a single-ended amplifier, the common-collector transistor should be cut off (negative voltage applied to its base). Because of the emitter resistors, $R_6$ and $R_7$, the CA3004 circuit will require more dc voltage for the same gain reduction as the CA3005 or CA3006, and the dc voltage required will be a function of the initial operating current.

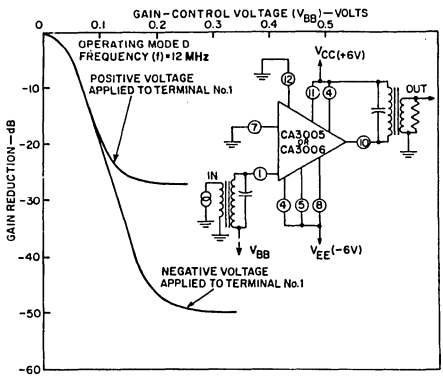



*Fig. 21—Gain-control characteristics of the CA3005 or CA3006 as a function of the dc offset voltage, $V_{BB}$, applied to the differential pair of transistors $Q_1$ and $Q_2$.*

The maximum gain-control range that can be provided by a reduction in the current of transistor $Q_3$ varies with frequency as shown in Fig. 22. The maximum gain-control range that can be obtained is dependent on the full gain used, the circuit loading, and the external-circuit layout.

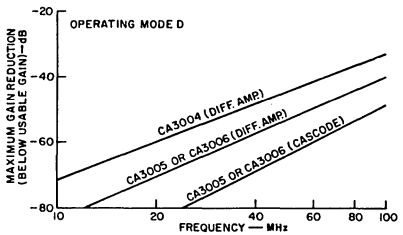



*Fig. 22—Maximum gain control provided by variations in the current through $Q_3$ as a function of frequency.*

A large part of the variation in the maximum gain control for the different circuits results from differences in the initial gain of the various circuits. Capacitive feed through appears less for the cascode than for the differential-amplifier configuration.

The following discussion of cross modulation describes variations of the two gain-control techniques.

## CROSS-MODULATION AND MODULATION DISTORTION

Cross-modulation and modulation distortion are important considerations in the selection of an amplifier for use in AM systems. Cross-modulation distortion refers to the transfer of modulation from an undesired carrier to the desired carrier by nonlinearities in the amplifier. Modulation distortion is a change in the modulation on the desired carried caused by the same amplifier nonlinearities that produce cross modulation. The two forms of distortion are related by the following equation:

$$\frac{D_2}{V_1^2} : \frac{K}{V_2^2} = \frac{3}{8} m : 1$$

where $D_2$ is the per cent of distortion in the modulation on the desired carrier (i.e., the modulation distortion), K is the per cent of cross-modulation distortion, $V_1$ is the amplitude of the desired-carrier voltage at the input, $V_2$ is the amplitude of the undesired-carrier voltage at the input, and m is the per cent of modulation of the desired carrier.

When $D_2$ and K are equal and m is 100 per cent, the ratio of $V_1$ to $V_2$ is 1.64. In the following paragraphs, data are given for only the cross-modulation distortion. The modulation distortion can be predicted from these data, however, on the basis of the relationship of $V_1$ to $V_2$. For example, in Fig. 23, $V_2$ is given as 22 millivolts for a gain of 0 dB. The value of $V_1$, then, is 1.64 x 22, or 36 millivolts.

Figs. 23 through 27 show the cross-modulation distortion of the CA3004, CA3005, and CA3006 integrated circuits as a function of their gain-control characteristics in both differential-amplifier and cascode-amplifier configurations. The amount of cross-modulation distortion is determined by the two-generator method with the input of the circuit under test driven from a 50-ohm source and with its output tuned to the frequency of the desired carrier. The amplitude of the undesired-carrier input voltage is that necessary to produce 10 per cent cross-modulation distortion for each manually determined gain-control setting.

**Differential-Amplifier Configurations** — The availability of internal connection points make possible several methods of gain control in differential-amplifier configurations of the CA3004, CA3005, and CA3006 circuits. Only two of these methods need be considered, however, to obtain an adequate evaluation of the cross-modulation characteristics. These include (1) the variation of the current in the constant-current transistor, $Q_3$, and (2) the use of an offset voltage to produce an unbalance in the differential pair of transistors, $Q_1$ and $Q_2$.

Fig. 23 shows the cross-modulation distortion characteristics of the CA3004, CA3005, and CA3006 with the differential pair of transistors balanced and with agc applied to the constant-current transistor. Because of the increased linearity that results from the emitter resistors $R_6$ and $R_7$, the CA3004 has improved cross-modulation characteristics at high current. The interfering signal voltage required to produce 10 per cent of cross modulation distortion is practically a constant over the entire agc range for the CA3005 and CA3006. The value of the interfering signal voltage (approximately 15 mv) for the CA3005 and CA3006 is twice that calculated from the logarithmic transconductance characteristic of a single transistor.

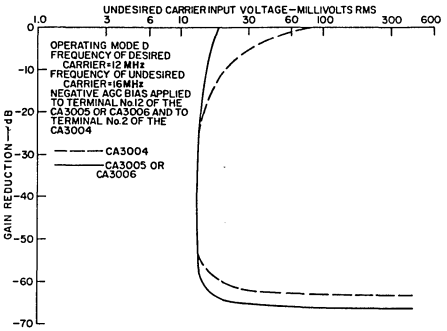



*Fig. 23—Gain control as a function of the input voltage from an undesired carrier that will produce cross-modulation distortion of 10 per cent for balanced differential-amplifier operation of the CA3004, CA3005 and CA3006. The gain-control voltage is applied to bias network of the constant-current transistor.*

Fig. 24 shows the cross-modulation distortion characteristic of the CA3005 and CA3006 when an offset voltage is applied to control the gain. The improved cross modulation performance at −5 dB gain is coincident with an inflection point on the curve of tranconductance as a function of input offset voltage. This point occurs at an offset voltage of approximately 50 millivolts.

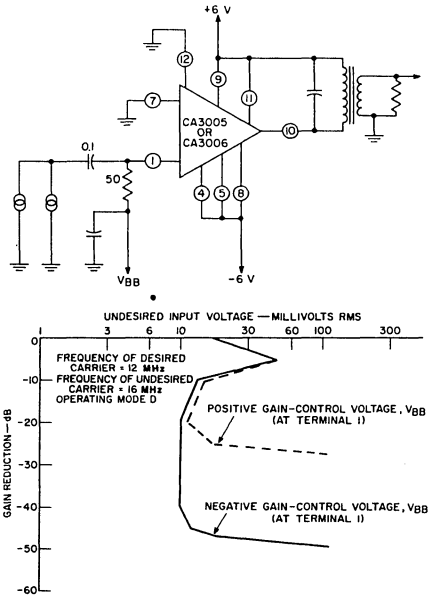



*Fig. 24—Gain control as a function of the undesired-carrier voltage that will produce 10 percent cross-modulation distortion for differential-amplifier operation of the CA3005 or CA3006 when gain control is provided by the application of an offset voltage to the differential pair of transistors.*

The cross-modulation performance is improved by the offset of the differential pair of transistors. Fig. 25 shows the cross-modulation data when an initial offset of 50 millivolts is employed and agc is applied to the constant-current transistor. The introduction of the unbalance reduces the cross-modulation distortion to approximately 10 dB less than that of the balanced circuit. This reduction in cross-modulation distortion, however, is accompanied by a decrease in gain of approximately 5 dB.

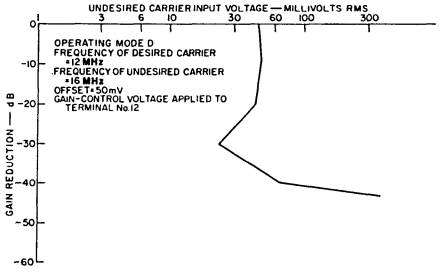



*Fig. 25—Gain control as a function of the input voltage from an undesired carrier that will produce cross modulation distortion of 10 per cent, for a differential-amplifier configuration of the CA3005 or CA3006 having a 50-millivolt offset and with the gain control voltage applied to the bias network of the constant-current transistor.*

**Cascode Configurations** — Cross-modulation data for cascode configurations of the integrated-circuit rf amplifiers are given for only the CA3005 and CA3006 circuits, because the CA3004 circuit is not designed for this type of operation. When the CA3005 or CA3006 is operated in the cascode configuration, gain control may be provided by either of two methods: (1) A negative voltage may be applied to the base of transistor $Q_3$ or (2) A negative voltage may be applied to the base of transistor $Q_1$.

In the first method, the gain is reduced by the application of a negative-going voltage at terminal 12. As the amplitude of this voltage is increased to the value required to cut off transistor $Q_3$, the gain of the circuit is decreased. The cross-modulation distortion characteristics for this type of gain control are shown in Fig. 26. The cross-modulation characteristics are comparable to those of a single transistor having a bypassed emitter resistor.

The cross-modulation distortion characteristics obtained for the second method of gain control are shown in Fig. 27. No improvement in cross-modulation characteristics over those obtained for the first gain-control method are observed, although the agc range is greater.

## MIXER CAPABILITIES

The CA3004, CA3005, and CA3006 integrated circuits may be used as mixers, modulators, and product detectors. The schematic diagrams in Figs. 28(a) and 28(b) illustrate the use of these circuits in mixer applications. The oscillator input is injected at the base of transistor $Q_3$ (because there is no direct-base connection available on the CA3004, a higher oscillator drive voltage is required for this circuit); the rf input is injected single- or double-ended to the bases of transistors $Q_1$ and $Q_2$. The use of a center-tapped inductor for the output tuned circuit (double-ended) allows the common-mode signal of the oscillator to be balanced out so that the oscillator will not overload subsequent stages, and provides carrier suppression for modulators.

The gain performance and generation of harmonics in the CA3004, CA3005, and CA3006 mixer circuits are dependent on the amplitude of the oscillator drive signal and the dc bias. The expression for product detection or frequency multiplication in the CA3005 or CA3006 (consult Fig. 29) are determined as follows:

$$e_o = e_1 g_m Z_L \qquad (1)$$

where $e_o$ is the output voltage, $e_1$ is the differential input voltage, $g_m$ is the transconductance of the differential pair of transistors ($Q_1$ and $Q_2$), and $Z_L$ is the load impedance (total between collectors). For a balanced circuit, the transconductance is given by

$$g_m = \frac{\alpha q}{2KT} I_o \qquad (2)$$

The term $I_o$, is used to represent the collector current of

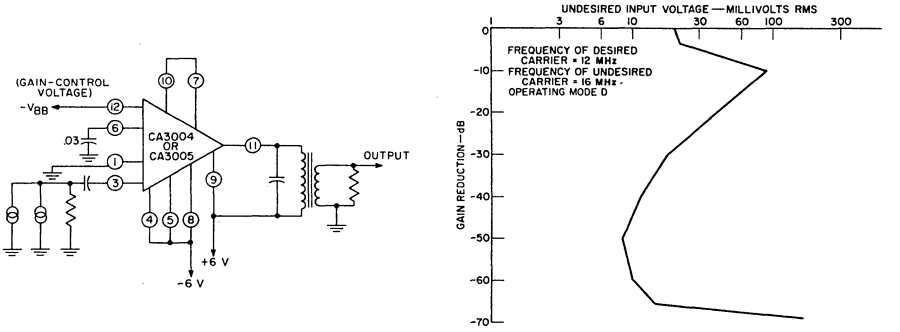



*Fig. 26—Gain control of the CA3005 or CA3006, in a cascode configuration, as a function of the undesired-carrier voltage that will produce 10 per cent cross-modulation distortion when the gain is controlled by a negative bias voltage applied to the base of transistor $Q_1$. The schematic diagram illustrates the circuit configuration.*

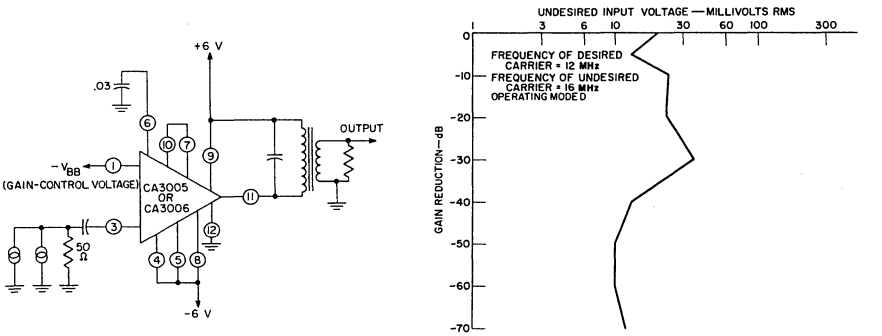



*Fig. 27—Gain control of the CA3005 or CA3006, in a cascode configuration, as a function of the undesired-carrier voltage that will produce 10 per cent cross-modulation distortion when the gain is controlled by a negative bias voltage applied to the base of transistor $Q_1$. The schematic diagram illustrates the circuit configuration.*

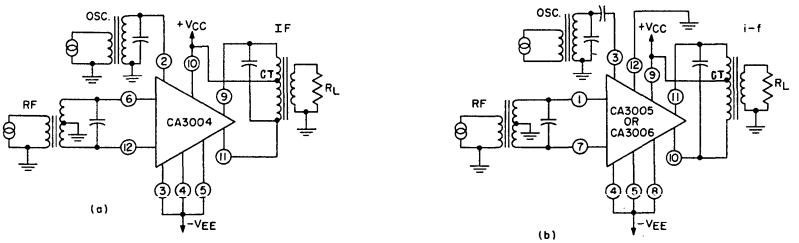



*Fig. 28—Circuit diagrams for the use of the integrated-circuit rf amplifiers as mixers (operating mode D): (a) CA3004; (b) CA3005 or CA3006.*

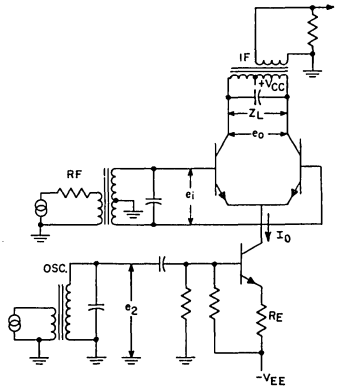



*Fig 29—Circuit diagram of a CA3005 or CA3006 balanced mixer (operating mode D). The equation derived for product detection or multiplication are based on this circuit.*

transistor $Q_3$ and may be expressed as

$$I_o = g_{m_2} e_2 \quad (3)$$

where $g_{m_2}$ is the transconductance of transistor $Q_3$ and $e_2$ is input voltage applied to transistor $Q_3$. The output voltage, $e_o$, therefore is given by the following equation:

$$e_o = \frac{\alpha q}{2KT} e_1 e_2 g_{m_2} Z_L \quad (4)$$

Eq. (4) is a general expression for the output voltage of the mixer having input signals $e_1$ and $e_2$. With emitter degeneration in the constant-current transistor ($Q_3$), $g_{m_2}$ is essentially constant for a sufficiently large emitter current (> 1 ma); the current $I_o$, therefore, follows the applied voltage $e_2$.

When $e_1$ and $e_2$ are sinusoidal and $g_m$ is a constant, the input signal voltages are given as follows:

$$e_1 = E_1 e^{j\omega_1 t} + \overset{*}{E}_1 e^{-j\omega_1 t} \quad (5)$$

$$e_2 = E_2 e^{j\omega_2 t} + \overset{*}{E}_2 e^{-j\omega_2 t} \quad (6)$$

($\overset{*}{E}_1$ is the conjugate of $E_1$, and $\overset{*}{E}_2$ is the congugate of $E_2$)

With the substitution of these relationships, the equation for the output voltage the CA3005 or CA3006 now becomes

$$e_o = \frac{\alpha q}{2KT} g_{m_2} Z_L [E_1 E_2 e^{j(\omega_1+\omega_2)t} + \overset{*}{E}_1 \overset{*}{E}_2 e^{-j(\omega_1+\omega_2)t}]$$

$$+ \frac{\alpha q}{2KT} g_{m_2} Z_L [E_1 \overset{*}{E}_2 e^{j(\omega_1-\omega_2)t} + \overset{*}{E}_1 E_2 e^{-j(\omega_1-\omega_2)t}] \quad (7)$$

Eq. 7 gives the output voltage for a CA3005 or CA3006 used as a product detector or multiplier. (Note that only the two sideband frequencies are included in the output). The requirements for product detectors or multipliers are that the circuit should be biased in a linear region with a small signal voltage applied. Because $\alpha q\ g_{m_2}/2KT$ is essentially constant, the gain of the mixer is determined from $Z_L$ and the $e_1 e_2$ product. The linearity of the CA3006 is illustrated by the curve of the conversion transconductance as a function of the oscillator voltage, shown in Fig. 30. (Although the curve is plotted on logarithmic paper because of the wide range, the relationship is linear.) The gain reaches a maximum value at approximately 2.5 volts rms. Because measurement inaccuracies prevent the use of this curve to determine harmonic generation, spurious-signal measurements were taken on CA3005 and CA3006 mixer circuits. For these measurements, the rf input was untuned and the oscillator and if frequencies were held constant. For a fixed amplitude of oscillator injection on terminal 3, the rf was varied in frequency, and the amplitude of the responses was recorded. The results are shown in Table V. The spurious signals generated are a function of oscillator drive. A low oscillator drive (0.1 volt rms) produced only three spurious signals for which the rejection was less than 70 dB down. These measurable spurious responses were third-order products that involved the second harmonic of either the oscillator or rf signal. The relative if gain increases with decreasing oscillator drive because of lower mixer gain.

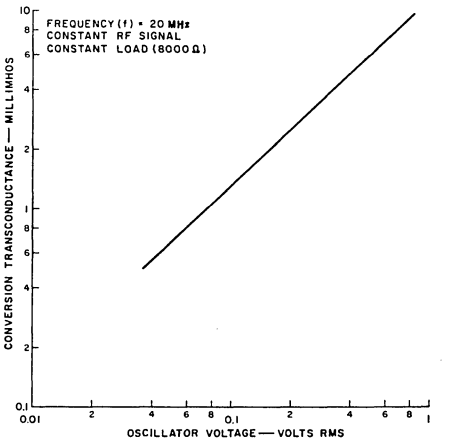



*Fig. 30—Conversion gain of a CA3005 or CA3006 mixer circuit as a function of the oscillator voltage.*

The common-mode cancellation of the oscillator signal at the collector outputs is indicative of the carrier suppression that can be provided in modulators. The carrier suppression is a function of output tuned-circuit balance and the transistor offset voltage. The contribution of the offset is illustrated in Figs. 31 and 32 which show the output signal as a function of the offset voltage for the CA3004 and for CA3005 and CA3006 respectively. These data were obtained on circuits operated with a balanced output tuned to the oscillator frequency.

TABLE V

Response of a CA3005 or CA3006 Mixer to Spurious Harmonics

| Frequency | Signal Freq., $f_s$ (MHz) | $V_{osc}$ at term. 3 (rms volts) | Diff.-Freq. Output (dB relative to $f_o - f_x$) | $V_{osc}$ at term. 3 (rms volts) | Diff.-Freq. Output (dB relative to $f_o - f_x$) | $V_{osc}$ at term. 3 (rms volts) | Diff.-Freq. Output (dB relative to $f_o - f_x$) | $V_{osc}$ at term. 3 (rms volts) | Diff.-Freq. Output (dB relative to $f_o - f_x$) |
|---|---|---|---|---|---|---|---|---|---|
| $f_o - f_x$ | 1.0 | 1 | 0 | 0.7 | 0 | 0.3 | 0 | 0.1 | 0 |
| $f_{if}$ | 0.659 | 1 | 7.5 | 0.7 | 10 | 0.3 | 18 | 0.1 | 27 |
| $2f_x - f_o$ | 1.159 | 1 | −53.1 | 0.7 | −53.1 | 0.3 | −54.9 | 0.1 | −52.3 |
| $2f_o - 2f_x$ | 1.329 | 1 | −76.1 | 0.7 | — | 0.3 | — | 0.1 | — |
| $2f_x - 2f_o$ | 1.988 | 1 | −75.5 | 0.7 | — | 0.3 | — | 0.1 | — |
| $f_x - f_o$ | 2.318 | 1 | 0 | 0.7 | 0 | 0.3 | 0 | 0.1 | 0 |
| $2f_o - f_x$ | 2.659 | 1 | −31.7 | 0.7 | −35 | 0.3 | −39.7 | 0.1 | −47.8 |
| $2f_x - 3f_o$ | 2.813 | 1 | −79.6 | 0.7 | — | 0.3 | — | 0.1 | — |
| $f_x - 2f_o$ | 3.977 | 1 | −31.7 | 0.7 | − 35 | 0.3 | −39.7 | 0.1 | −47.8 |
| $3f_o - f_x$ | 4.309 | 1 | −35.8 | 0.7 | −59.3 | 0.3 | −74.7 | 0.1 | — |
| $f_x - 3f_o$ | 5.627 | 1 | −38.5 | 0.7 | −57 | 0.3 | −74 | 0.1 | — |
| $4f_o - f_x$ | 5.977 | 1 | −38.9 | 0.7 | −63 | 0.3 | — | 0.1 | — |

$f_o$ = 1.659 Mc/s; $V_{osc}$ = oscillator injection voltage.

All blank spaces indicate difference-frequency output more than 70 dB below the $f_o - f_x$ output.

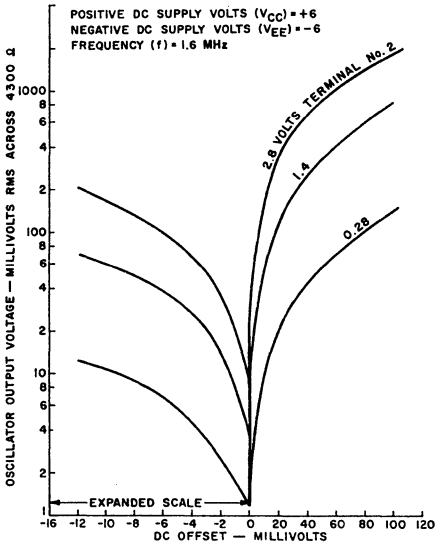



*Fig. 31—Cancellation of the oscillator signal at the output of a CA3004 mixer as a function of the dc offset voltage.*

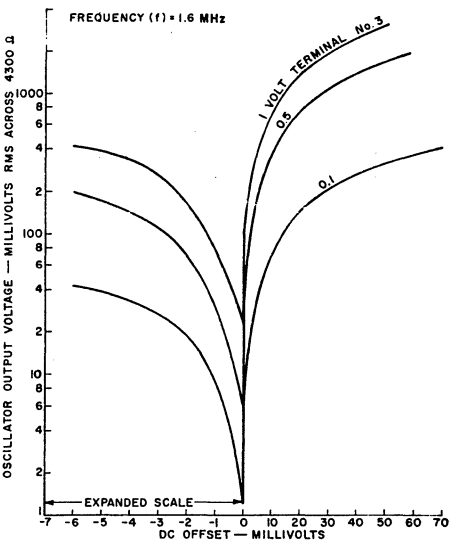



*Fig. 32—Cancellation of the oscillator signal at the output of a CA3005 or CA3006 mixer as a function of the dc offset voltage.*

## LIMITER CHARACTERISTICS

**Differential-Amplifier Configuration** — The differential-amplifier, driven by a constant-current transistor, is probably the optimum circuit configuration for bipolar transistor limiters. The advantage of such circuits in limiter applications is that collector saturation of either transistor $Q_1$ or $Q_2$ can be avoided because of the action of the constant-current transistor $Q_3$. Figs. 2 and 3 show typical limiting characteristics for the CA3004 and for the CA3005 and CA3006 respectively. For the CA3005 and CA3006 (no emitter degeneration), "hard" limiting is achieved for a peak-to-peak input of 300 millivolts for all values of total dc current ($I_{CC}$). For the CA3004, the input voltage required for "hard" limiting is a function of $I_{CC}$ because of the linearizing effect of the degenerative emitter resistors, $R_6$ and $R_7$. As saturation

TABLE VI
Limiter Performance of a Differential Amplifier

| *V Supply (volts)* | $I_{C_1} + I_{C_2}$ *(mA)* | *Maximum Resistive Load (ohms)* | *Maximum Tuned Load (ohms)* | *Voltage Gain With Emitter Degeneration (dB)* | | *Voltage Gain Without Emitter Degeneration (dB)* | |
|---|---|---|---|---|---|---|---|
| | | | | *Resistive Load* | *Tuned Load* | *Resistive Load* | *Tuned Load* |
| 6 | 0.5 | 12000 | 24000 | 31 | 37 | 35 | 41 |
| 6 | 1.0 | 6000 | 12000 | 28 | 34 | 35 | 41 |
| 6 | 2.0 | 3000 | 6000 | 25 | 31 | 35 | 41 |
| 6 | 3.0 | 2000 | 4000 | 22 | 28 | 35 | 41 |

$$R_L = \frac{V_{supply}}{I_{C1} + I_{C2}} \quad \text{Resistive Load}$$

$$R_L = \frac{2\,V_{supply}}{I_{C1} + I_{C2}} \quad \text{Tuned Load}$$

$g_m R_L$ = voltage gain

must be prevented for good limiting, a maximum load resistor and low-level voltage gain exists for a given $I_{CC}$ and positive supply voltage. Table VI shows the maximum resistor values and voltage gains usable for $V_{CC}$ = 6 volts, for the three circuit types. The low-level transconductance can be obtained from the slope near the origin for the curves shown in Figs. 2 and 3. The maximum voltage gain is independent of $I_{CC}$ in the CA3005 and CA3006 and is dependent on $I_{CC}$ in the CA3004. Figs 5 through 8 show the $I_{CC}$ currents and transconductance for optional operating conditions.

When the differential amplifier is used for limiting, the emitter-to-base breakdown voltage for transistors $Q_1$ and $Q_2$ cannot be exceeded without degradation in performance. For the CA3004, CA3005, and CA3006, this voltage including a safety margin should not exceed 2.5 volts rms. Either of two methods may be used to prevent this value being exceeded: (1) Make sure the preceding stage limits before the input voltage reaches 2.5 volts (maximum voltage gain per stage approximately 20 dB), or (2) add one junction diode ($D_1$), as shown in Fig. 33 (this allows a maximum usable voltage gain consistent with good limiting and stability).

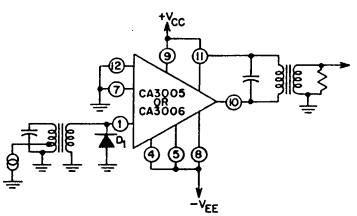



*Fig. 33—Circuit diagram of a CA3005 or CA3006 differential-amplifier limiter that uses a diode to provide input overload protection.*

**Cascode Amplifier** — The limiting characteristics of the CA3005 or CA3006, when used as a cascode amplifier are dependent on the current limiting in transistor $Q_3$ or the voltage limiting of transistor $Q_1$ (high-impedance output load). Limiting characteristics for both cases are shown in Figs. 34 and 35. The data in Fig. 34 are obtained with a collector load of 500 ohms. This limiting characteristic is "soft" and is acceptable over only a 20-dB range. The peak-to-peak voltage at the collector is never large enough to cause saturation. The limiting characteristic shown in Fig. 35 is obtained with a collector load of 5000 ohms, and saturation of transistor $Q_1$ occurs. The limiting is harder and covers a broader range, but severe tuned-circuit loading occurs.

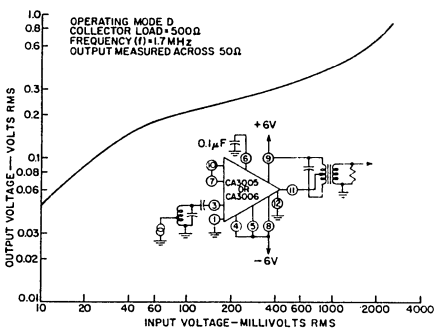



*Fig. 34—Limiting characteristics and circuit diagram of a CA3005 or CA3006 cascode limiter having a 500-ohm collector load impedance.*

## APPLICATIONS OF THE RF AMPLIFIER CIRCUITS

### RF AMPLIFIER

Figs. 36, 37, and 38 illustrate the use of the CA3004, the CA3005 or CA3006 differential-amplifier configurations, and the CA3005 or CA3006 cascode configurations, respectively, as single-ended rf amplifiers. Adjustable matching networks, derived from the y parameters, are included in each circuit. The values of the adjustable components as

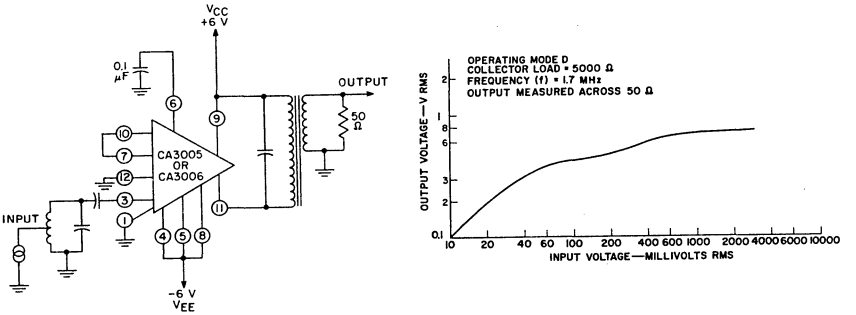
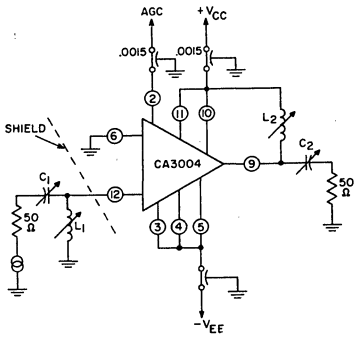



*Fig. 35—Limiting characteristics and circuit diagram of a CA3005 or CA3006 cascode limiter having a 5000-ohm collector load impedance.*



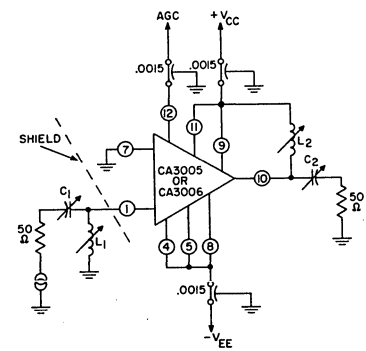

**CIRCUIT ELEMENTS**

| *FREQUENCY (MHz)* | $L_1$ *(μH)* | $C_1$ *(pF)* | $L_2$ *(μH)* | $C_2$ *(pF)* |
|---|---|---|---|---|
| 30 | 1.8-2.7 | 2-10 | 1.8-2.7 | 2-10 |
| 100 | 0.15-0.3 | 0.9-7 | 0.1-0.2 | 0.9-7 |

**POWER GAIN PERFORMANCE**

| *DC SUPPLIES (volts)* | *POWER GAIN (dB) 30 MHz* | *100 MHz* |
|---|---|---|
| ±6 | 24 | 12 |

*Fig. 36—Circuit used to determine the rf performance capabilities of a CA3004 integrated-circuit rf amplifier.*



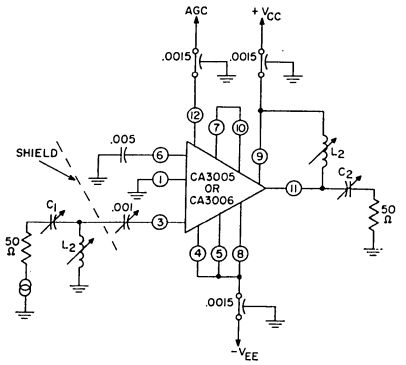

**CIRCUIT ELEMENTS**

| *FREQUENCY (MHz)* | $L_1$ *(μH)* | $C_1$ *(pF)* | $L_2$ *(μH)* | $C_1$ *(pF)* |
|---|---|---|---|---|
| 30 | 1.2-2 | 5-40 | 1.2-2 | 1.5-20 |
| 100 | 0.4-0.7 | 1-12 | 0.25-0.5 | 1-12 |

**POWER GAIN PERFORMANCE**

| *DC SUPPLIES (volts)* | *POWER GAIN (dB) 30 MHz* | *100 MHz* |
|---|---|---|
| ±6 | 29 | 18 |
| ±4.5 | 27.8 | 16 |
| ±3 | 23.0 | 11.5 |

*Fig. 37—Circuit used to determine the rf performance capabilities of a CA3005 or CA3006 integrated-circuit rf amplifier in a differential-amplifier configuration.*




**CIRCUIT VALUES**

| *FREQUENCY (MHz)* | $L_1$ *(μH)* | $C_1$ *(pF)* | $L_2$ *(μH)* | $C_2$ *(pF)* |
|---|---|---|---|---|
| 30 | 0.3-0.6 | 14-150 | 0.8-1.4 | 5-40 |
| 100 | 0.07-0.12 | 5-40 | 0.15-.3 | 5-40 |

**POWER GAIN PERFORMANCE**

| *DC SUPPLIES (volts)* | *POWER GAIN (dB)* 30 MHz | 100 MHz |
|---|---|---|
| ±6 | 36 | 20 |
| ±4.5 | 33 | 18.5 |
| ±3 | 21.5 | 15.0 |

*Fig. 38—Circuit used to determine the rf performance capabilities of a CA3005 or CA3006 integrated-circuit rf amplifier in a cascode configuration.*

well as typical power gains are also shown in the figures. A conjugate match at the input is provided for all configurations. A conjugate match at the output is impossible for the cascode configuration (as pointed out in the discussion of y parameters). At 30 MHz, the CA3005 differential amplifier output was mismatched. At high gains, the circuit feedback ($y_r$) is low, but the external-circuit layout adds feedback.

**Tuned IF Amplifier** — Two or more CA3004, CA3005 or CA3006 integrated circuits can be connected in cascade for use as a tuned if amplifier for either AM or FM applications. The schematic diagrams of two three-stage 12-MHz amplifiers are shown in Figs. 39 and 40, for FM and AM use, respectively. Both if amplifiers are housed in metal boxes, and adequate shielding and supply decoupling are provided.

The amplifier shown in Fig. 39 (limiting amplifier for FM use), is designed to provide a gain per stage of 26 dB. At this gain per stage, diodes are required at the input to prevent base-to-emitter breakdown. For operation as a low-level limiter, the circuit input is matched, and the required gain fixes the unloaded Q of the tuned circuit and the collector load. Good noise performance for the first stage is obtained by the use of a high Q (200) toroid inductor for input transformer $T_1$. The other transformers are slug-tuned and have relatively low unloaded Q's (70 to 100) which contribute the necessary insertion loss for the required gain. A lower unloaded Q was required for transformer $T_2$, so 10,000 ohms of resistance was added in parallel with this transformer. Little or no skew is detectable in the response characteristic for this circuit, shown in Fig. 41. The limiting characteristic of the circuit is shown in Fig. 42. Other typical over-all performance characteristics are:

Total power drain = 48 milliwatts
Overall power gain = 77 dB
3-dB bandwidth = 300 kHz
Input limiting level = 30 microvolts
Noise figure = 4 dB

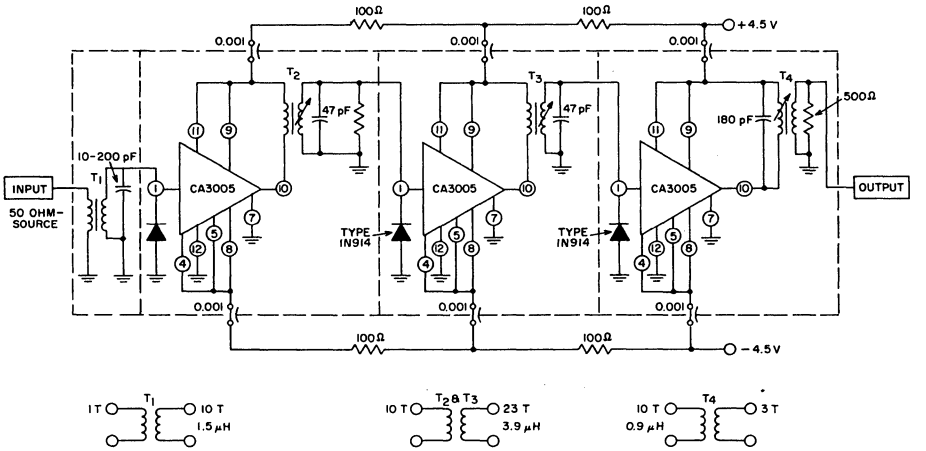
The AM circuit (Fig. 40) uses three CA3004 circuits and is designed to provide a stage gain of 25 dB. The source resistance to the input circuit was chosen as 800 ohms as a satisfactory compromise for gain, noise figure, and modulation-distortion performance. Input and output transformers, $T_1$ and $T_4$, have high unloaded Q's (200) to preserve good noise performance and to maximize the output power. The interstage transformers, $T_2$ and $T_3$, have low unloaded Q's (37) to achieve the required gain. The second detector has a 3-dB bandwidth of 5.0 kHz, the typical over-all performance characteristics are:

Power drain = 83 milliwatts
Power gain (to second-detector input) = 76 dB
AGC range (1st stage) = 60 dB
Noise figure = 4.5 dB
3-dB bandwidth = 160 kHz

The signal-to-noise ratio of the circuit as a function of the input is shown in Fig. 43, and the frequency-response characteristic is shown in Fig. 44.

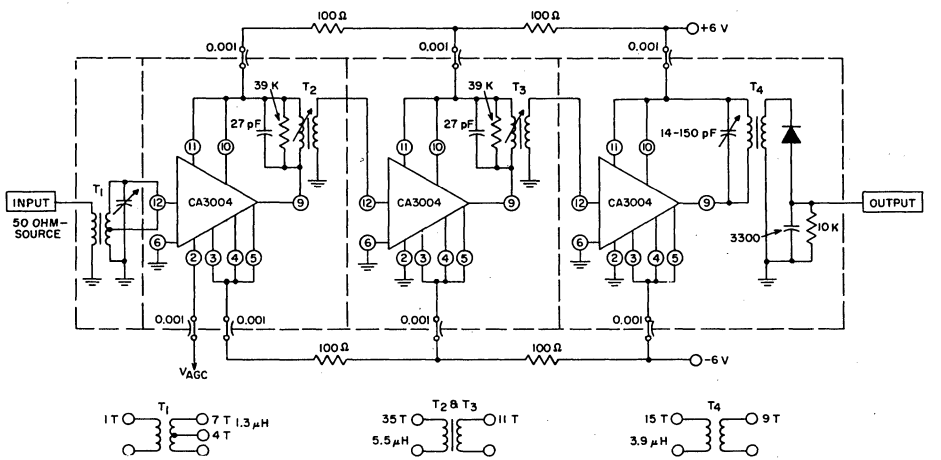
**Mixers** — The use of the CA3004 and the CA3005 or CA3006 as balanced mixers to convert 20 MHz to 1.75 MHz., is shown in Fig. 45. Because the input impedance of the two circuits differ by a factor of approximately 2:1, typically 4000 ohms for the CA3004 and 2200 ohms for the CA3005 or CA3006, different input transformers ($T_1$) are required; the other tuned circuits, however, are the same. The output load impedance between collectors is approximately 8000 ohms. The conversion power gain and noise figure as a function of the oscillator drive are shown in Fig. 46 and 47. Power gain increases and noise figure decreases with increases in the oscillator drive.

**Suppressed-Carrier Modulator and Product Detector**— The CA3005 and CA3006 were used in a suppressed-carrier double-sideband modulator and product detector. The double-sideband modulator is a convenient vehicle to evaluate carrier suppression and product detection. With the two circuits coupled together, the relation between modulation




**NOTES:** 1. Transformer $T_1$ is a Ferramic Q-2 Toroid Type (unloaded Q = 200).
2. Transformers $T_2$, $T_3$, and $T_4$ are slug-tuned with Carbonyl IT-75 material (unloaded Q = 75).

*Fig. 39—Schematic diagram of a three-stage, 12-MHz limiting if amplifier that uses CA3005 circuits in operating mode D.*




**NOTES:** 1. Transformers $T_1$ and $T_4$ are Ferramic Q-2 Toroid Types (unloaded Q =200).
2. Transformers $T_2$ and $T_3$ are slug-tuned with Carbonyl IT-71 material (unloaded Q = 70).

*Fig. 40—Schematic diagram of a three-stage, 12-MHz gain-controlled AM amplifier that uses CA3004 circuits in operating mode D.*

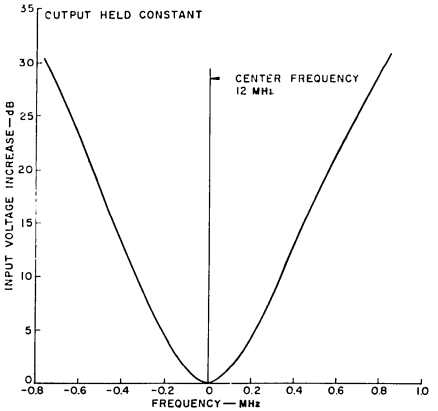



*Fig. 41—Frequency-response characteristics of the 12-MHz limiting amplifier shown in Fig. 39.*

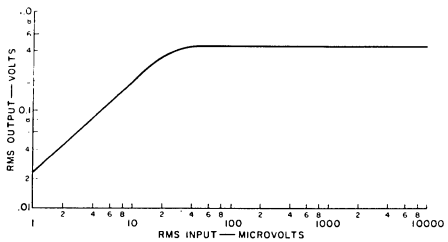



*Fig. 42—Limiting characteristics of the 12-MHz limiting amplifier shown in Fig. 39.*

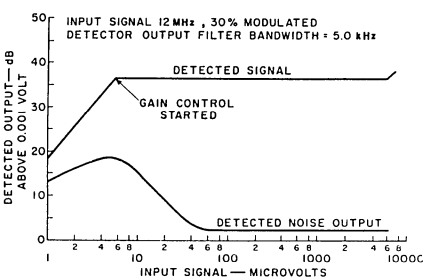



*Fig. 43—Output signal-to-noise ratio as a function of the input signal for the 12-MHz gain-controlled amplifier shown in Fig.40 when gain control is used in only the first stage.*

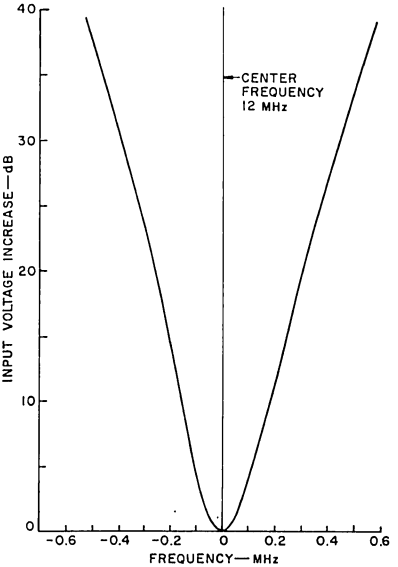



*Fig. 44—Frequency-response characteristics of the 12-MHz gain-controlled amplifier shown in Fig. 40.*

distortion and drive levels is readily established.

Feedback may cause oscillation or unbalance; care must, therefore, be taken in the external-circuit layout design. Shielding must also be provided for both the double-sideband modulator and product detector.

The circuit diagram of the double-sideband modulator is shown in Fig. 48. The modulating signal is applied single-ended to the differential pair of transistors, $Q_1$ and $Q_2$, and the oscillator signal is applied to the base of transistor $Q_3$. The output is taken double-ended from the balanced transformer, $T_2$. The carrier suppression is a function of bilateral symmetry (offset, output-transformer balance, and modulation drive circuits) and the modulation-to-carrier drive ratio. With the external-circuit bilateral symmetry carefully preserved, the carrier output is approximately 25 dB below the double-sideband output for CA3006 units (offset $\leqq$ 1 millivolt) operated with a drive $v_1$ = 10 millivolts rms and $v_2$ = 31.5 millivolts rms. Although the signal-to-carrier ratio of 25 dB represents an inadequate rejection for most systems (40 to 60 dB is usually required), this value relaxes the filter requirements from those necessary on more commonly used single-sideband modulators. An improvement over the 25-dB ratio is obtained if the modulation drive $v_1$ is increased and the carrier drive $v_2$ is decreased, because the output is a function of the product of $v_1$ and $v_2$.

The circuit diagram for a product detector is shown in Fig. 49. The product detector which provides the advantage

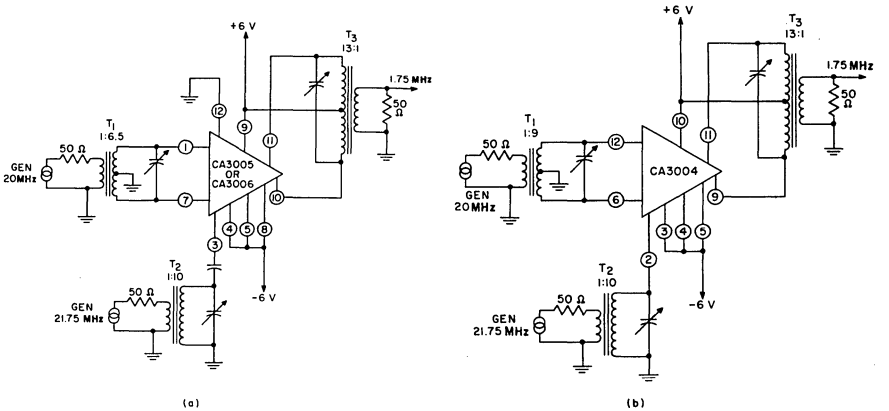



*Fig. 45—Circuit diagrams for the use of CA3004, CA3005, and CA3006 integrated circuits as balanced mixers to convert an input frequency of 20 MHz to an output frequency of 1.75 MHz.*

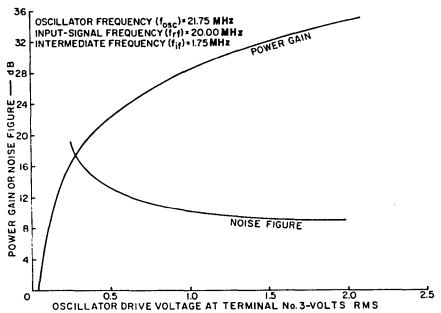



*Fig. 46—Power gain and noise figure as a function of the oscillator drive voltage for the CA3005 or CA3006 balanced mixer.*

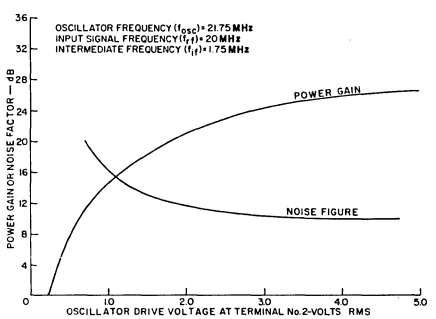



*Fig. 47—Power gain and noise figure as a function of the oscillator drive voltage for the CA3004 balanced mixer.*

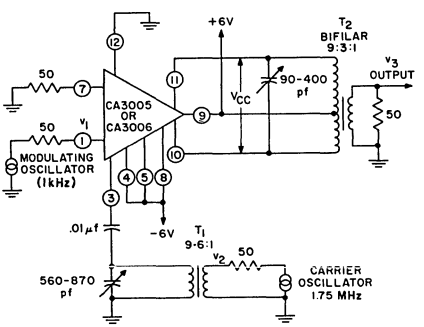



*Fig. 48—Circuit diagram for the use of the CA3005 or CA3006 as a double-sideband, suppressed-carrier modulator.*

of a double-ended out-of-phase output, is driven through a 50-ohm adjustable feed by the double-sideband signal from the modulator. The levels of $v_1$, $v_2$, $v_4$, and $v_5$ are altered to establish the relationship between the harmonic distortion and drive levels as well as gain values for typical operation. The results are shown in Table VII. Overdrive by the modulation ($v_1$) or the modulated signal ($v_4$) results in third-harmonic distortion of the detected signal. Note that gain is a function of either the product of $v_1$ and $v_2$, or the product of $v_4$ and $v_5$.

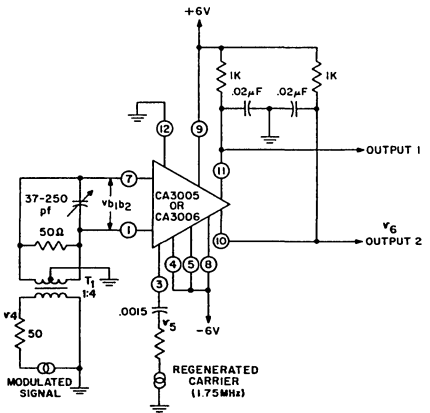



*Fig. 49—Circuit diagram for the use of a CA3005 or CA3006 as a product detector.*

TABLE VII

Gain and Distortion as a Function of Different Drive Levels for a Double-Sideband Modulator and Product Detector Using the CA3006

| Condition | $v_1$ (mv rms) | $v_2$ (mv rms) | Terminal 3 Voltage (Volts rms) | $v_{ce}$ (volts rms) | $v_3$ (mv rms) | $v_4$ (mv rms) | $v_{b1b2}$ (mv rms) | $v_5$ (mv rms) | $v_6$ (mv rms) | Harmonic Distortion (dB below fundamental) 2nd | 3rd | 4th | 5th |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $v_1$ Varied | 5 | 31.5 | 0.296 | 0.046 | 4.95 | 1 | 4 | 0.5 | 36 | | 54 | | |
| | 10 | 31.5 | 0.296 | 0.080 | 8.9 | 1 | 4 | 0.5 | 36 | | 54 | | |
| | 30 | 31.5 | 0.296 | 0.25 | 26.6 | 1 | 4 | 0.5 | 36 | | 37.5 | | |
| $v_2$ Varied | 10 | 31.5 | 0.296 | 0.083 | 8.9 | 1 | 4 | 0.5 | 36 | | 54 | | |
| | 10 | 100 | 0.96 | 0.262 | 28 | 1 | 4 | 0.5 | 36 | | 51 | | |
| | 10 | 315 | 2.96 | 0.83 | 89 | 1 | 4 | 0.5 | 36 | | 50 | | |
| $v_4$ Varied | 10 | 31.5 | 0.296 | 0.083 | 8.9 | 0.5 | 2 | 0.5 | 17.5 | | 54 | | |
| | 10 | 31.5 | 0.296 | 0.083 | 8.9 | 1 | 4 | 0.5 | 36 | | 52 | | |
| | 10 | 31.5 | 0.296 | 0.083 | 8.9 | 3 | 12 | 0.5 | 110 | | 47.5 | | |
| | 10 | 31.5 | 0.296 | 0.083 | 8.9 | 5 | 20 | 0.5 | 188 | 51 | 37 | | 59 |
| $v_5$ Varied | 10 | 31.5 | 0.296 | 0.083 | 8.9 | 1 | 4 | 0.315 | 23 | 56 | 54 | | |
| | 10 | 31.5 | 0.296 | 0.083 | 8.9 | 1 | 4 | 0.5 | 36 | | 54 | | |
| | 10 | 31.5 | 0.296 | 0.083 | 8.9 | 1 | 4 | 1.0 | 86 | | 50 | | |

Notes: 1. Consult Figs. 48 and 49 for explanation of voltage designations.
2. Blank spaces indicate harmonic distortion is more than 60 dB below the fundamental.

# Application of the RCA-CA3000 Integrated-Circuit DC Amplifier

BY
A. J. LEIDICH and M. E. MALCHOW

The RCA-CA3000 dc amplifier is a monolithic silicon integrated circuit supplied in a 10-terminal TO-5 package. This stabilized and compensated differential amplifier has push-pull outputs, high-impedance (0.1-megohm) inputs, and gain of approximately 30 dB at frequencies up to one MHz. Its useful frequency response can be increased to several tens of megahertz by the use of external resistors or coils.

Because full gain-control capability is inherent in the CA3000, it can be used as a signal switch (with pedestal), a squelchable audio amplifier (with suppressed switching transient), a modulator, a mixer, or a product detector. When suitable external components are added, it can also be used as an oscillator, a one-shot multivibrator, or a trigger with controllable hysteresis. Within its specified frequency range, it is an excellent limiter, and can handle input signals up to about 80 millivolts rms before significant cross-modulation or intermodulation products are generated.

## CIRCUIT DESCRIPTION

The circuit diagram and terminal connections for the CA3000 dc amplifier are shown in Fig. 1. The circuit is basically a single-stage differential amplifier ($Q_2$ and $Q_4$) with input emitter-followers ($Q_1$ and $Q_5$) and a constant-current sink ($Q_3$) in the emitter-coupled leg. Push-pull input and output capabilities are inherent in the differential configuration.

The use of degenerative resistors $R_4$ and $R_5$ in the emitter-coupled pair increases the linearity of the circuit and decreases its gain. The low-frequency output impedance between each output (terminals 8 and 10) and ground is essentially the value of the collector resistors $R_1$ and $R_2$ in the differential stage.

## OPERATION OF THE CIRCUIT

The CA3000 is designed for operation from a wide range of supply voltages. Operation from either one or two power supplies is feasible, as illustrated by the typical biasing techniques shown in Fig. 2. However, operation from two supplies is recommended because fewer external bias networks are required and, therefore, less power is consumed.

The maximum voltage that can be applied across the circuit (positive supply voltage $V_{CC}$ plus negative supply voltage $V_{EE}$) is 16 volts. The maximum voltage capability ($V_{CE}$) of the differential pair is limited to 8 volts. Extra care must be used to ensure that these values are not exceeded when the circuit is used to drive inductive loads.

The operating-current conditions of the differential pair are determined by the base-bias circuit and emitter resistance of the emitter-coupled constant-current sink ($Q_3$), as well as by the voltage between terminals 2 and 3. Each possible current condition is manifested by (1) a distinct set of dc operating characteristics with differing temperature characteristics, (2) a particular value of gain having its own temperature dependence, and (3) a particular dynamic

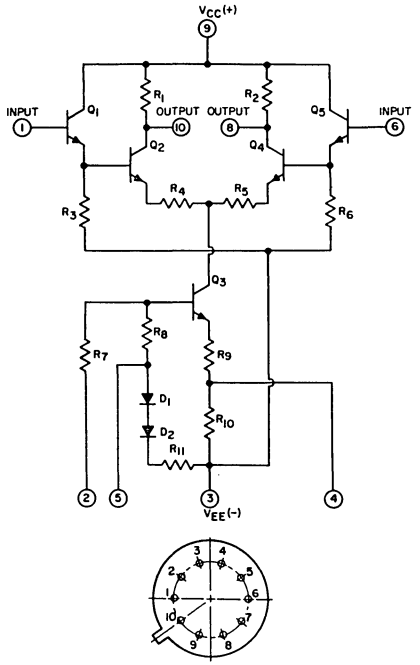



*Fig. 1 - Schematic diagram and terminal connections for the CA3000 integrated-circuit dc amplifier.*

output-voltage capability. For each value of voltage between terminals 2 and 3 ($V_{EE}$ when terminal 2 is grounded), there are four possible operating modes, as described in Table I.

Table I—Operating Modes for CA3000 DC Amplifier

| *Mode* | *Shorted Terminals* | *Condition of Diodes* | *$Q_3$ Emitter Resistor* |
|---|---|---|---|
| A | none | in | $R_9 + R_{10}$ |
| B | 5-3 | out | $R_9 + R_{10}$ |
| C | 4-3 | in | $R_9$ |
| D | 5-4-3 | out | $R_9$ |

The operating characteristics for these modes of operation are summarized in Table II for various two-supply configurations with terminal 2 grounded and with $V_{EE}$ values of −3 and −6 volts dc.

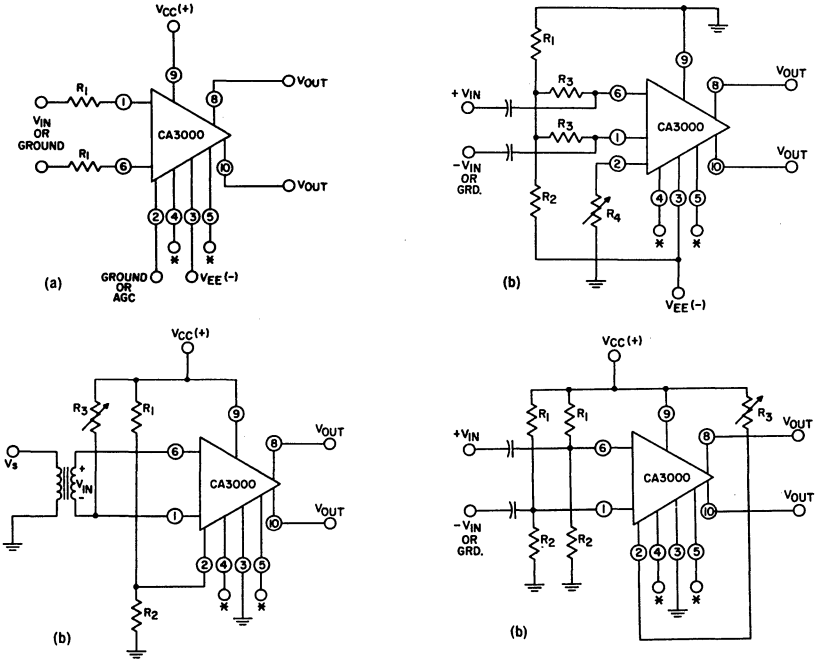
Table II shows that the positive supply voltage can be adjusted for each mode of operation and for each value of negative supply so that the nominal dc output voltage is zero. (Although the $V_{CC}$ value required for mode C for a $V_{EE}$ of −6 volts dc is in excess of the maximum rating, operation within ratings can be achieved with slightly negative values of output voltage.) The use of these adjusted values of positive supply provides two advantages: (1) direct interstage coupling can be effected in a single-ended configuration, and (2) negative feedback can be introduced from a single output back to the appropriate input. For low-level applications in mode D with a negative supply voltage $V_{EE}$ of −3 volts dc and a positive supply voltage $V_{CC}$ of 1.1 volts dc, the CA3000 has a gain of 24.4 dB, a dissipation of 6.2 milliwatts, an output capability of 2.2 volts peak-to-peak, and a dc output-voltage reference level of zero.

The information in Table II can be modified for single-supply designs by simple addition and/or subtraction of dc values. For example, the correct information for a single

Table II—Design Characteristics of CA3000 Operating Modes

| *DC Supply Volts Positive* $V_{cc}$ | *Negative* $-V_{EE}$ | *Operating mode* | *Single-ended midband voltage gain — dB* $G_{VS}$ | *DC output volts (Terminal 8 or 10 to ground)* $V_{odc}$ | *Positive voltage swing* $V_{omax}$* | *Negative voltage swing* $V_{omin}$* | *Total power dissipation — mW* |
|---|---|---|---|---|---|---|---|
| 6 | −6 | A | 31.2 | +2.3 | +3.7 | −3.8 | 40 |
| 6 | −6 | B | 27.3 | +4.3 | +1.7 | −5.7 | 36 |
| 6 | −6 | C | 34.6 | −1.5 (saturated) | +7.5 | 0 | 61 |
| 6 | −6 | D | 32.4 | +1.0 | +5.0 | −2.4 | 47 |
| 3.7 | −6 | A | 31.2 | 0 | +3.7 | −1.4 | 33 |
| 1.7 | −6 | B | 27.3 | 0 | +1.7 | −1.4 | 25 |
| 10.6 (over rating) | −6 | C | 34.6 | 0 | +10.6 | −1.5 | 83 |
| 5.0 | −6 | D | 32.4 | 0 | +5.0 | −1.5 | 43 |
| 3 | −3 | A | 27.5 | +1.2 | +1.8 | −2.6 | 8.8 |
| 3 | −3 | B | 16.6 | +2.6 | +0.4 | −4.1 | 7.4 |
| 3 | −3 | C | 32.6 | −1.5 (saturated) | +4.5 | 0 | 14 |
| 3 | −3 | D | 24.4 | +1.9 | +1.1 | −3.3 | 8.5 |
| 1.8 | −3 | A | 27.5 | 0 | +1.8 | −1.5 | 7.2 |
| 0.4 | −3 | B | 16.6 | 0 | +0.4 | −1.5 | 8.4 |
| 5.3 | −3 | C | 32.6 | 0 | +5.3 | −1.5 | 19 |
| 1.1 | −3 | D | 24.4 | 0 | +1.1 | −2.6 | 6.2 |

* $V_{omax}$ and $V_{omin}$ are the ac swing extremities above and below $V_{odc}$.




* Connection of terminals 4 and 5 depends on mode of operation.

***Fig.2 - Typical biasing arrangements for the CA3000 for operation from (a) two separate voltage supplies, or (b) a single voltage supply.***

supply of 12 volts dc for operating mode A can be obtained from the conditions shown in the table for mode A for $V_{CC} = 6$ Vdc and $V_{EE} = -6$ Vdc by the addition of 6 volts to the values shown for $V_{CC}$, $V_{EE}$, $Vo_{dc}$, $Vo_{max}$, and $Vo_{min}$. (It should be noted that the required voltage levels at the input terminals 1 and 6 and at terminal 2 are also 6 volts higher.

As mentioned previously, the four operating modes exhibit different temperature characteristics. Fig. 3 shows theoretical curves of dc output voltage as a function of

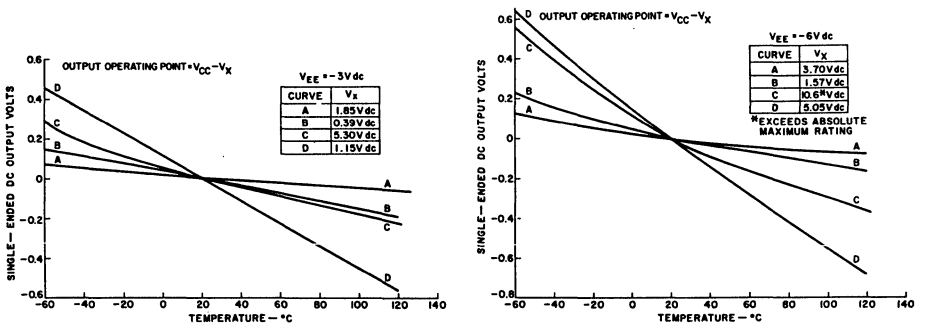



***Fig.3 - Theoretical curves of dc output voltage as a function of temperature for negative-supply voltages of -3 and -6 volts dc (calculated for β = 35 at 20°C).***

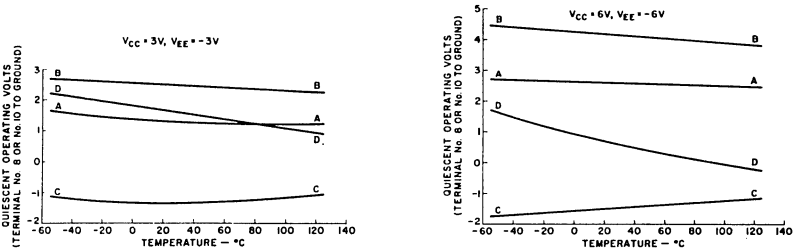



*Fig.4 - Measured curves of dc output voltage as a function of temperature for negative-supply voltages of -3 and -6 volts dc.*

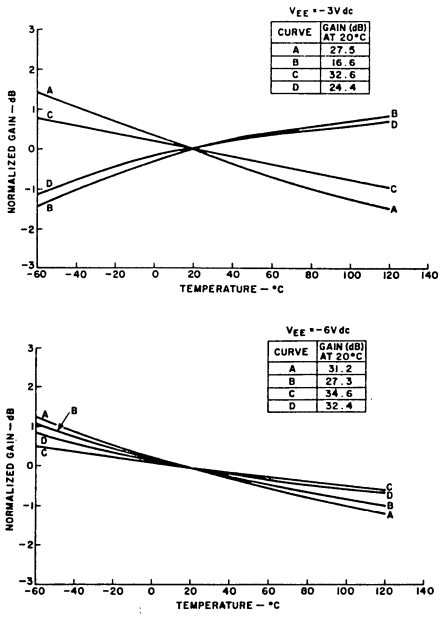



*Fig.5 - Theoretical curves of gain as a function of temperature for negative-supply voltages of -3 and -6 volts dc (calculated for β = 35 at 20°C).*

temperature for each operating mode for negative supply voltages $V_{EE}$ of −3 and −6 volts dc. The experimental curves shown in Fig. 4 are in excellent agreement with the theoretical curves except in the case of mode C. In this mode, the differential-pair transistors $Q_2$ and $Q_4$ were driven into saturation as a result of the use of symmetrical supplies ($V_{CC} = V_{EE}$) for the experimental data. The discrepancy could be corrected by use of somewhat higher values of positive supply voltage.

Fig. 5 shows theoretical curves of gain as a function of temperature for the four operating modes with $V_{EE}$ values of −3 and −6 volts dc. With the diodes in (modes A and C), the gain decreases for both values of $V_{EE}$. With the diodes out (modes B and D), on the other hand, the gain increases with temperature for a negative supply of −3 volts dc, but decreases with temperature for a negative supply of −6 volts dc. With the diodes out, there is a value of negative supply (approximately −4.5 volts dc) for which the gain is independent of temperature. Fig. 6 shows measured values of single-ended and push-pull gain for mode A with symmetrical power supplies of ±6 volts dc. (This configuration is used in the remaining discussion because it provides the maximum sinusoidal output capability, as shown in Table II, and because of the convenience of ±6-volt dc supplies.)

The typical single-ended voltage-gain/frequency-response curve of the CA3000 for dc supplies of ±6 volts in operating mode A is shown in Fig. 7, together with the test circuit used for voltage-gain measurements. The Bode responses of the CA3000 are virtually independent of source impedance up to 10,000 ohms because of the emitter-follower inputs. The curves in Fig. 8 show that gain and bandwidth are virtually independent of temperature for operation in mode A with ±6-volt dc supplies.

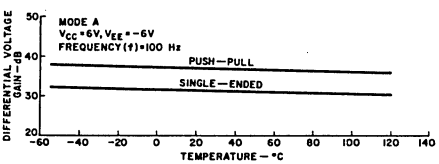



*Fig.6 - Measured values of single-ended and push-pull gain for mode A operation with symmetrical power supplies of ±6 volts dc.*

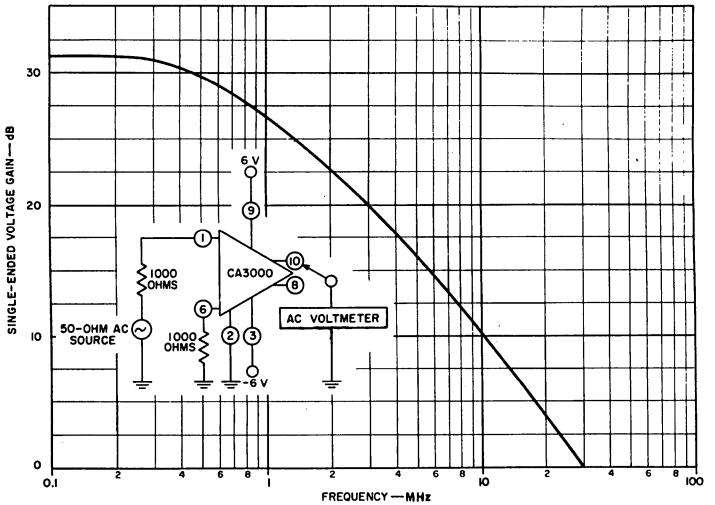



*Fig.7 - Single-ended voltage gain of CA3000 as a function of frequency in test circuit shown.*

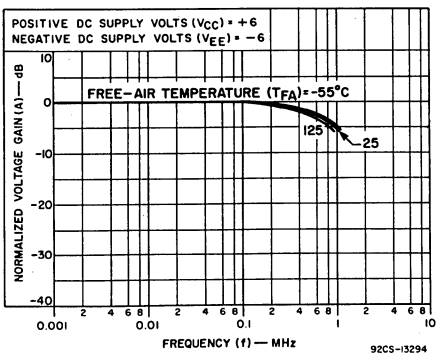
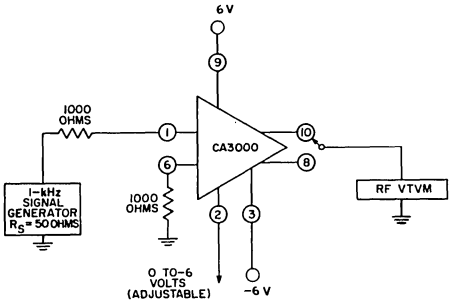



*Fig.8 - Normalized gain-frequency curves for CA3000 at three different temperatures.*

Fig. 9 shows agc characteristics for the CA3000 for an input frequency of 1 kHz, together with the agc voltage-gain test circuit. When the agc voltage at terminal 2 is varied from 0 to −6 volts, the amplifier gain can be varied over a range of 90 dB.

Fig. 10 shows the test circuit used to measure common-mode rejection, together with curves of common-mode rejection as a function of frequency and temperature. Typical rejection is 97 dB at a frequency of 1 kHz. Fig. 11 shows the test circuit used to measure the dc unbalance of the amplifier (referred to the input), together with a curve of the input offset voltage as a function of temperature. Typical input offset voltage (with an assumed push-pull differential gain of 37 dB) is 1.5 millivolts. Fig. 12 shows curves of input bias current, input impedance, and dynamic output voltage as functions of temperature.



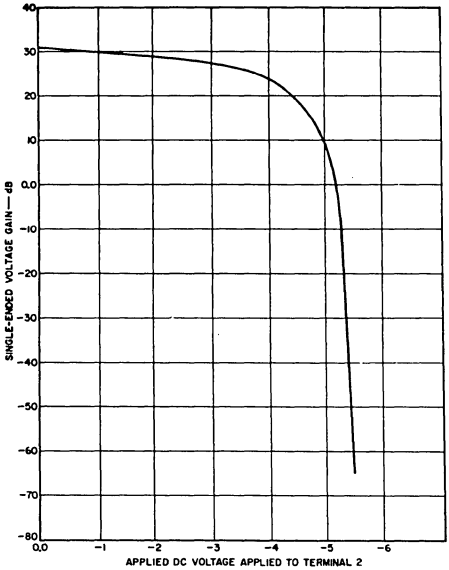
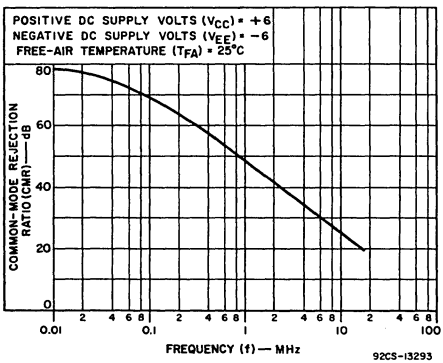
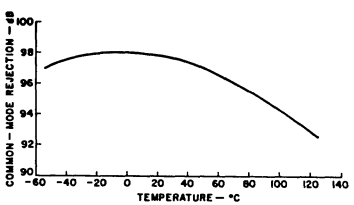




*Fig.9 - AGC characteristics of CA3000 in test circuit shown at frequency of 1 kHz.*



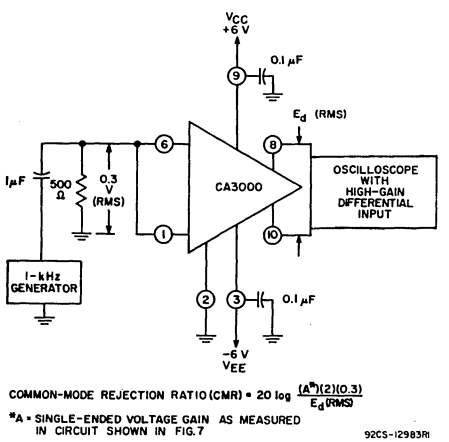




*Fig.10 - Common-mode rejection of CA3000 as a function of frequency and of temperature in test circuit shown.*

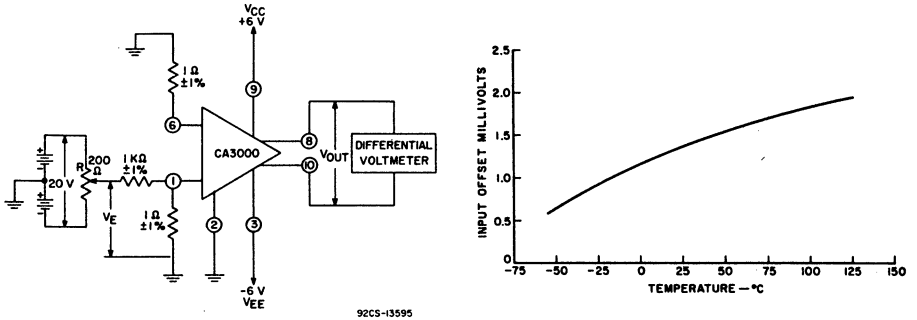



*Fig.11 - Input offset voltage of CA3000 as a function of temperature in test circuit shown.*

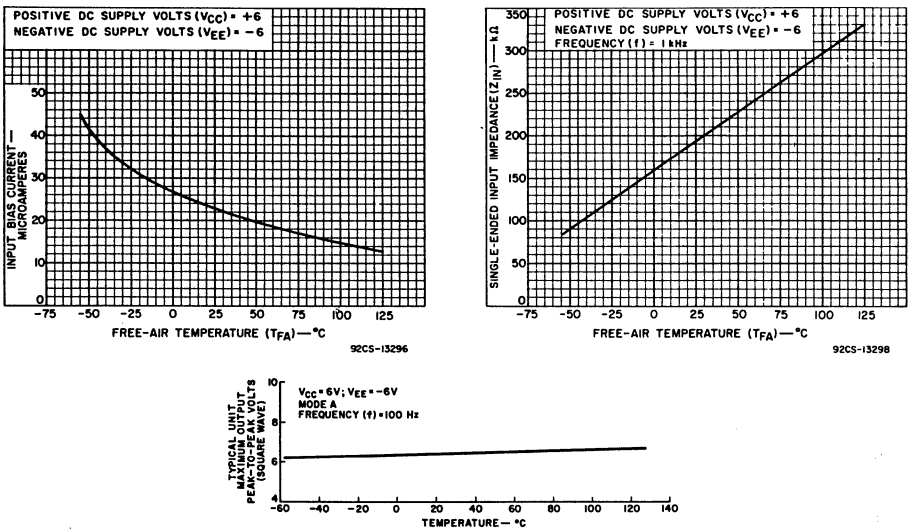



*Fig.12 - Input bias current, input impedance, and dynamic output voltage of CA3000 as functions of temperature.*

## APPLICATIONS

**Crystal Oscillator**—The CA3000 can be used as a crystal oscillator at frequencies up to 1 MHz by connection of a crystal between terminals 8 and 1 and use of two external resistors, as shown in Fig. 13(a). The output is taken from the collector that is not connected to the crystal (in this case, terminal 10). If a variable-feedback ratio network is used, as shown in Fig. 13(b), the feedback may be adjusted to provide a sinusoidal oscillation. Output waveforms for both circuits are also shown. The frequency in each circuit is 455 kHz, as determined by the crystal. The range of these crystal oscillators can be extended to frequencies of 10 MHz or more by use of collector tuning.

**Modulated Oscillator**—If a low-frequency signal is connected to terminal 2, as shown in Fig. 14, the CA3000 can function as an oscillator and produce an amplitude-modulating signal. The waveform in Fig. 14 shows the modulated signal output produced by the modulated oscillator circuit when a 1-kHz signal is introduced at terminal 2 and a high-pass filter is used as the output.

**Low-Frequency Mixer**—In a configuration similar to that used in modulated-oscillator applications, the CA3000 amplifier may be used as a mixer by connection of a carrier signal at the base input of either differential-pair transistor (terminal 1 or 6) and connection of a modulating signal to terminal 2 or 5.

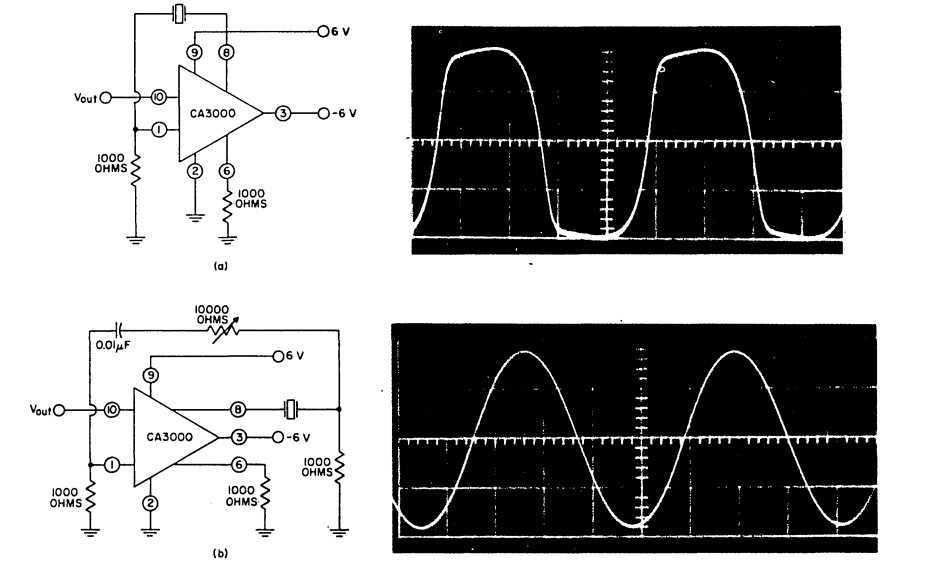



*Fig. 13 - Schematic diagrams and output waveforms of (a) crystal oscillator and (b) crystal oscillator with variable feedback.*

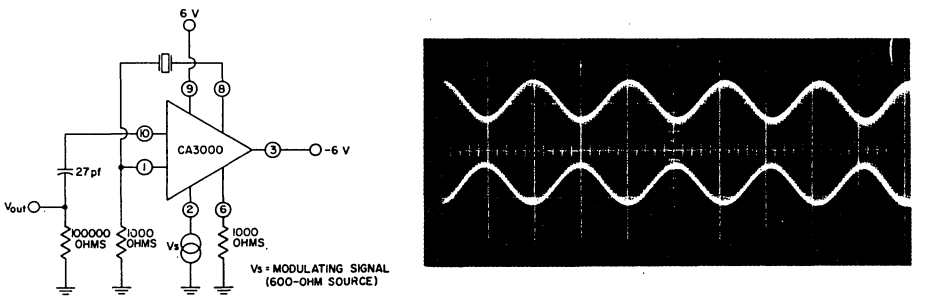



*Fig. 14 - Schematic diagram and output waveform of CA3000 modulated oscillator.*

**Cascaded RC-Coupled Feedback Amplifier**—The two-stage feedback cascade amplifier shown in Fig. 15 produces a typical open-loop midband gain of 63 dB. This circuit uses a 100-picofarad capacitor $C_1$ to shunt the differential outputs of the first stage. This capacitor staggers the high-frequency roll-offs of the amplifier and thus improves stability.

The gain-frequency characteristic of the feedback amplifier is shown in Fig. 16(a) for a feedback resistance $R_f$ approaching infinity. The low-end roll-off of the amplifier is determined by the interstage coupling. Because agc may be applied to the first stage, the amplifier of Fig. 15 may be used in high-gain video-agc applications under open-loop conditions. If feedback is used to control the gain, agc may still be applied successfully.

Fig. 16(b) shows the agc characteristics for the two-stage amplifier under open-loop and two closed-loop conditions at a frequency of 1 kHz. As shown in Fig. 16(a), the open-loop bandpass is 18 Hz to 135 kHz; under closed-loop conditions, the bandpass is 1.3 Hz to 2 MHz for 40-dB gain and 0.13 Hz to 6.6 MHz for 20-dB gain. The negative feedback thus improves low-frequency performance suffi-

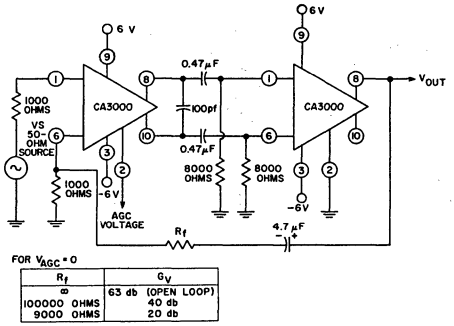
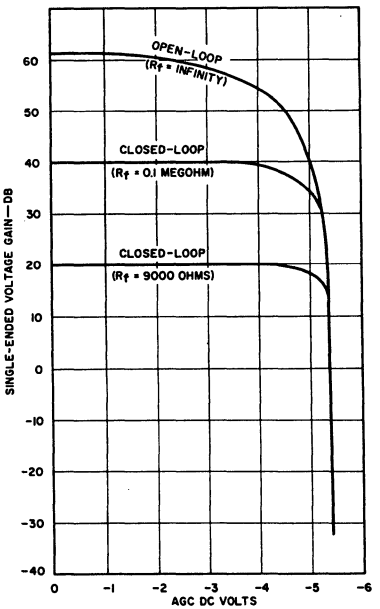



*Fig.15 - Cascaded RC-coupled feedback amplifier using two CA3000 circuits.*

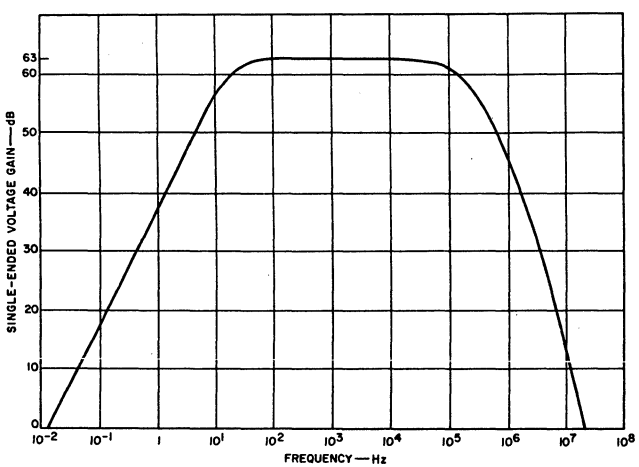
ciently so that the use of small coupling capacitors $C_2$ and $C_3$ involves little sacrifice in low-frequency response. If three or more CA3000 amplifiers are cascaded, the low-frequency roll-offs must be staggered as well as those at the high end to prevent oscillation. A three-stage cascade has a midband gain of approximately 94 dB.

**Narrow-Band Tuned Amplifier**—Because of its high input and output impedances, the CA3000 is suitable for use in parallel tuned-input and tuned-output applications. There is comparative freedom in selection of circuit Q because the differential amplifier exhibits inherently low feedback qualities provided the following conditions are met: (1) the collector of the driven transistor is returned to ac ground and the output is taken from the non-driven side, and (2) the input is adequately shielded from the output by a ground plane.

The CA3000 has an output capacitance of approximately 9 picofarads at a frequency of 10 MHz. This capacitance




(b)




(a)

*Fig.16 - (a) Gain-frequency and (b) agc characteristics of feedback amplifier shown in Fig.15.*

will resonate a 28 microhenry coil at this frequency and give a minimum Q of 4.55 when the collector load resistor is the only significant load. With this low Q, stagger tuning may be unnecessary for many broad-band applications.

Fig. 17 shows the CA3000 in a narrow-band, tuned-input, tuned-output configuration for operation at 10 MHz with an input Q of 26 and an output Q of 25; the response curve of the amplifier is also shown. The 10-MHz voltage gain is 29.6 dB, and the total effective circuit Q is 37. There is very little feedback skew in the response curve. The CA3000 can be used in tuned-amplifier applications at frequencies up to the 30-MHz range.

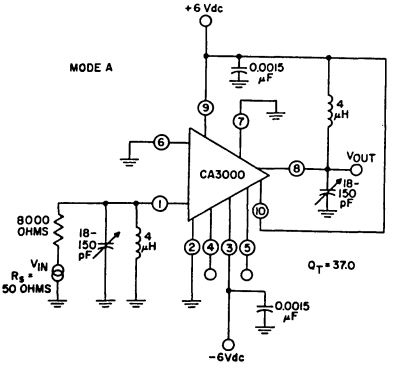



*Fig. 17 - Schematic diagram and response curve for 10-MHz tuned-input, tuned-output, narrow-band amplifier using CA3000.*

**Schmitt Trigger**—The CA3000 can be operated as an accurate, predictable Schmitt trigger provided saturation of either side of the differential amplifier is prevented (hysteresis is less predictable if saturation occurs). Non-saturating operation is accomplished by operation in mode B

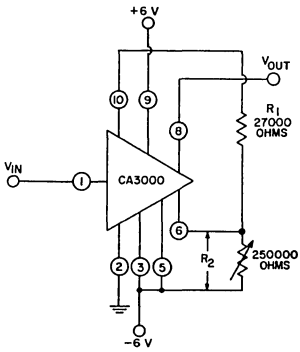



*Fig. 18 - Schematic diagram for Schmitt trigger using CA3000.*

(terminals 3 and 5 shorted together) in the configuration shown in Fig. 18. Large values are required for external resistors $R_1$ and $R_2$ because they receive the total collector current from terminal 10. Because of the high impedances, resistor $R_2$ is actually a parallel combination of the input impedance (approximately 0.1 megohm) of the CA3000 and the 0.25-megohm external resistor. The Schmitt-trigger design equations (for $\alpha = 1$) are summarized below. In these equations, $Q_2$ and $Q_4$ are the differential-pair transistors, $Q_1$ and $Q_5$ are the emitter-follower transistors, and $Q_3$ is the constant-current sink.

**STATE I:** $Q_2$ off, $Q_4$ conducting (not saturated)

$$V_{e_1} = \frac{V_{CC}(R_2) - V_{EE}(R_1 + 8000)}{R_1 + R_2 + 8000}$$

where 8000 ohms is the output impedance of $Q_1$ (obtained from the published data). For $R_1 = 27000$ ohms and $V_{CC} = V_{EE} = 6$ Vdc,

$$V_{e_1} = \frac{6V(R_2) - 6V(35000)}{R_2 + 35000} \quad (A)$$

$$R_2 = (R_1 + 8000)\frac{V_{EE} + V_{e_I}}{V_{CC} - V_{e_I}}$$

$$R_2 = (35000)\frac{6V + V_{e_I}}{6V - V_{e_I}} \quad (B)$$

$$V_{e_I} = V_{CC} - I_E(8000)$$

where $I_E$ = collector current of transistor $Q_3$ ≈0.48 milliampere in operating mode B with $V_{EE} = -6$ volts dc.

$$V_{e_I} = 2.14\ V \quad (C)$$

$V_{P_I}$ ≡ Firing voltage for transition from state I to state II

$$V_{P_I} = V_{e_I} - 0.053 - 100\,I_E \text{ at } 25°C$$

$$V_{P_I} = V_{e_I} - 0.101\ V \text{ at } 25°C \quad (D)$$

**STATE II:** $Q_4$ conducting (not saturated), $Q_2$ off

$$V_{e_{II}} = V_{CC}$$

$$V_{e_{II}} = 6\ V \quad (A)$$

$$V_{e_{II}} = \frac{(V_{CC} - I_E\,8000)R_2 - V_{EE}(R_1 + 8000)}{R_1 + R_2 + 8000}$$

$$V_{e_{II}} = \frac{2.14\ V\ (R_3) - 6\ V\ (35000)}{R_3 + 35000} \quad (B)$$

$V_{T_{II}}$ ≡ Firing voltage for transition from state II back to state I

$V_{T_{II}} = V_{e_{II}} + 0.053 + 100\ I_R$ at 25°C

$V_{T_{II}} = V_{e_{II}} + 0.101$ V at 25°C (C)

## HYSTERESIS VOLTAGE

$V_{HYS} = V_{T_I} - V_{T_{II}}$

$$= \frac{3.86\ V\ (R_3)}{R_3 + 35000} - 0.202\ V \text{ at } 25°C$$

From the calculations for state I, it is evident that either $V_{e_I}$ or $R_3$ must be a known design value. Because $R_R$ is a composite value, $V_{e_I}$ is the more reasonable choice. The ability of these equations to predict the Schmitt-trigger performance is evidenced by the comparison of calculated and experimental data in Table III.

Table III — Comparison of Calculated and Experimental Data for Schmitt Trigger

| *Condition* | *Parameter* | *Calculated* | *Experimental* |
|---|---|---|---|
| 1) $V_{e_I} = -2V$ | $V_{T_I}$ | −2.1V | −2.2V |
| | $V_{T_{II}}$ | −3.19V | −3.2V |
| | $V_{HYS}$ | +1.09V | +1.0V |
| 2) $V_{e_I} = -1V$ | $V_{T_I}$ | −1.10V | −1.0V |
| | $V_{T_{II}}$ | −2.51V | −2.45V |
| | $V_{HYS}$ | +1.41V | +1.4V |
| 3) $V_{e_I} = 0$ | $V_{T_I}$ | −0.101V | 0 |
| | $V_{T_{II}}$ | −1.83V | −1.8V |
| | $V_{HYS}$ | +1.73V | +1.8V |
| 4) $V_{e_I} = +1V$ | $V_{T_I}$ | +0.9V | +1.0V |
| | $V_{T_{II}}$ | −1.15V | −1.0V |
| | $V_{HYS}$ | +2.1V | +2.0V |
| 5) $V_{e_I} = +2V$ | $V_{T_I}$ | +1.9V | +2.0V |
| | $V_{T_{II}}$ | −0.472V | −0.5V |
| | $V_{HYS}$ | +2.43V | +2.4V |

# Application of the RCA-CA3002 Integrated-Circuit IF Amplifier

BY
G. E. THERIAULT AND R. G. TIPPING

The RCA-CA3002 integrated-circuit if amplifier is a balanced differential amplifier that can be used with either a single-ended or a push-pull input and can provide either a direct-coupled or a capacitance-coupled single-ended output. Its applications include RC-coupled if amplifiers that use the internal silicon output-coupling capacitor, video amplifiers that use an external coupling capacitor, envelope detectors, product detectors, and various trigger circuits.

The CA3002 features all-monolithic silicon epitaxial construction designed for operation at ambient temperatures from −55 to 125°C, and contains a built-in temperature-compensating network for stabilization of gain and dc operating point over this operating-temperature range. It is supplied in a 10-terminal TO-5 low-silhouette package.

Because the CA3002 is a balanced differential amplifier fed from a constant-current source, it makes an excellent controlled-gain amplifier. The gain-control function may be extended to include video gating, squelching, and blanking applications. Envelope detection can be achieved by suitable biasing of the emitter-base diode of the output emitter-follower transistor. Product detection can be obtained by re-insertion of the carrier at the base of the constant-current-source transistor. Various trigger and waveform-generating circuits can also be achieved by the addition of suitable external components.

## CIRCUIT DESCRIPTION AND OPERATING MODES

Fig. 1 shows the circuit diagram and terminal connections for the CA3002 integrated circuit. The circuit is basically a single-stage differential amplifier ($Q_2$ and $Q_4$) with input emitter-followers ($Q_1$ and $Q_7$), a constant-current sink ($Q_3$) in the emitter-coupled leg, and an output emitter-follower ($Q_6$). A single-ended input is connected to terminal 10 or a push-pull input to terminals 10 and 5. A single-ended output is direct-coupled at terminal 8 or capacitance-coupled at terminal 6. Terminals 5 and 10 must be provided with dc returns to ground through equal external base resistors. The emitters of the differential pair ($Q_2$ and $Q_4$) are connected through degenerative resistors ($R_3$ and $R_4$) to the transistor current source ($Q_3$). The use of these resistors improves the linearity of the transfer characteristic and increases the signal-handling capability.

Transistor $Q_1$ provides a high input impedance for the if amplifier. Transistor $Q_5$ preserves the circuit symmetry, and also partially bypasses the base of $Q_4$. Additional bypassing can be obtained by connection of an external capacitor between terminal 5 and ground. The emitter-follower transistor $Q_6$ provides a direct-coupled output impedance of less than 100 ohms.

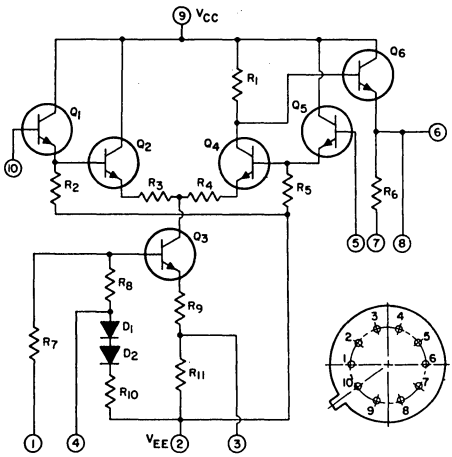



*Fig. 1—Schematic diagram and terminal connections for the CA3002 integrated-circuit if amplifier.*

When voltage supplies are connected to the CA3002, the most positive voltage must be connected to terminal 9 and the most negative voltage to terminal 2 (internally connected to the substrate and case). The CA3002 may be operated from various supplies and at various levels. Operation from either single or dual power supplies is feasible. When two supplies are used, they may be either symmetrical or non-symmetrical. When both positive and negative voltage supplies are used, external components can be minimized, as shown in Fig. 2(a). For single-supply applications, a resistor divider and a bypass capacitor must be added externally, as shown in Fig. 2(b). The current through $R_2$ and $R_3$ should be greater than one milliampere. Except in applications that use inductive drive, equal external base resistors must be added at terminals 5 and 10 to provide base-current returns. Terminal 7 can be connected to ground, or to the negative supply if a larger negative-going voltage swing is desired at any operating point.

For either single or dual supplies, the operating current in transistor $Q_3$ is determined by the bias voltage between terminals 1 and 2. The more negative point of this bias voltage must be connected to terminal 2. For dual-supply systems, terminal 1 is usually referenced to ground.

For any given bias voltage ($V_{EE}$ when terminal 1 is grounded), four operating modes are possible, as described in Table I. In general, each mode is characterized by (1) a distinct dc operating point with a characteristic temperature dependence, and (2) a particular value of gain that has a distinct temperature dependence.

When the diodes are utilized in the bias circuit (modes A and C), the current is essentially dependent on the temperature coefficient of the diffused emitter resistors $R_9$ and $R_{11}$, and has a tendency to decrease with increasing temperature at a rate independent of the negative supply voltage. The

Table I—Identification of CA3002 Operating Modes

| *Operating Mode* | *Shorted Terminals* | *Condition of Diodes* | *$Q_3$ Emitter Resistor* |
|---|---|---|---|
| A | none | in | $R_9 + R_{11}$ |
| B | 4-2 | out | $R_9 + R_{11}$ |
| C | 3-2 | in | $R_9$ |
| D | 4-3-2 | out | $R_9$ |

temperature coefficient of the diffused collector resistor $R_1$ is the same as that of the emitter resistor, and a constant collector-voltage operating point results at the collector of transistor $Q_1$. However, the operating point at output terminal 8 is modified by the base-emitter voltage drop of transistor $Q_6$ and its temperature dependence. Typical variation of the output operating point with temperature is shown in Fig. 3 for the four operating modes for $V_{EE}$ supplies of −3 and −6 volts. The voltage between terminals 8 and 9 is denoted by $V_N$. In mode B (with the diodes out of the bias circuit), it should be noted that the output operating point is constant with temperature because the change in the collector operating point is cancelled by the change in the base-emitter voltage drop ($V_{BE}$).

When the diodes are out of the bias circuit, the current-temperature curves become dependent on the negative supply voltage. Therefore, the value of $V_{EE}$ can be adjusted so that the transconductance decreases, increases, or remains constant with temperature. As shown in Fig. 4, the gain increases with temperature for a −3-volt $V_{EE}$ supply, but decreases with increasing temperature for a −6-volt $V_{EE}$ supply. At some intermediate value of $V_{EE}$ (approximately −4.5 volts), the gain should be constant as a function of temperature. In any case, however, a constant ac gain with temperature is accompanied by a change in the collector operating point of transistor $Q_1$.

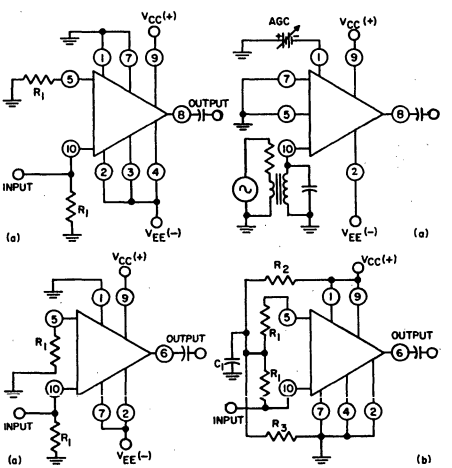



*Fig. 2—Circuit configurations for the CA3002 with (a) dual voltage supplies, and (b) a single supply.*

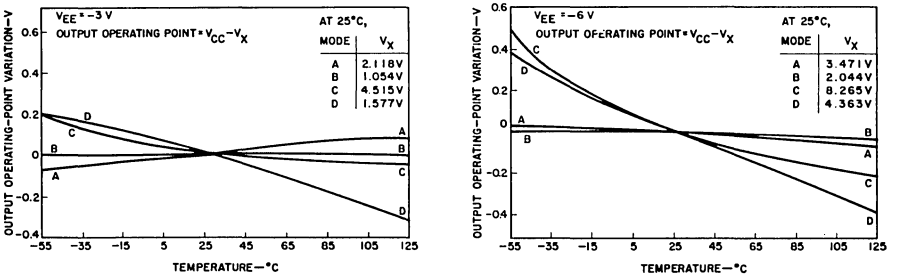



*Fig. 3—Output operating-point variation of the CA3002 (normalized to the 25°C operating point) as a function of temperature with $V_{EE}$ supply voltages of −3 and −6 volts.*

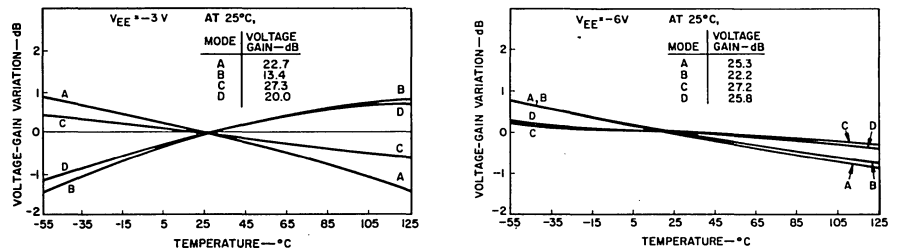



*Fig. 4—Voltage-gain variation of the CA3002 (normalized to the 25°C voltage gain) as a function of temperature with $V_{EE}$ supply voltages of −3 and −6 volts.*

Table II lists typical design performance characteristics for the four operating modes of the CA3002. By use of the data in this table and in Figs. 3 and 4, it is possible to select the proper operating mode to provide the most transconductance per milliwatt of dissipation, the specified output-swing capability, and the desired temperature performance for a particular design requirement.

In operating mode C, a valid non-saturated operating point may be obtained by use of non-symmetrical voltage supplies. For example, when $V_{EE}$ is −3 volts, the operating point will not be in saturation if a positive supply voltage of 4.5 volts or more is used (as indicated by Fig. 3). Resistor $R_6$ may then be returned to the negative supply instead of to ground to ensure the desired negative swings.

Table II—Typical Design Performance Characteristics for the Four Operating Modes of the CA3002 (Terminals 7 and 1 are grounded; temperature = 25°C)

| *Mode* | *± Supply Volts* | *Output Operating Point (Volts) at Terminal 8 to Ground* | *Voltage Gain (dB) at 1 MHz* | *+ Supply Current (mA)* | *− Supply Current (mA)* | *Power Dissipation (mW)* |
|---|---|---|---|---|---|---|
| A | 6 | 2.6 | 26.4 | 5.0 | 4.2 | 55.2 |
| B | 6 | 3.8 | 22.5 | 4.7 | 3.7 | 50.4 |
| C | 6 | 0 | | (transistor $Q_4$ saturated, transistor $Q_6$ cutoff) | | |
| D | 6 | 1.8 | 25.4 | 5.1 | 4.9 | 60 |
| A | 4.5 | 2.0 | 24.0 | 3.6 | 3.0 | 29.7 |
| B | 4.5 | 3.0 | 19.8 | 3.4 | 2.6 | 27.0 |
| C | 4.5 | 0 | | ($Q_4$ saturated, $Q_6$ cutoff) | | |
| D | 4.5 | 1.8 | 24.5 | 3.7 | 3.3 | 31.5 |
| A | 3 | 1.1 | 22 | 2.3 | 2.0 | 12.9 |
| B | 3 | 2.0 | 14.5 | 2.1 | 1.5 | 10.8 |
| C | 3 | 0 | | ($Q_4$ saturated, $Q_6$ cutoff) | | |
| D | 3 | 1.5 | 20 | 2.2 | 1.9 | 12.3 |

## CHARACTERISTICS

**Input Unbalance Current.** The input unbalance current of the CA3002 is defined as the difference between the currents flowing into the base input terminals 10 and 5. Fig. 5 shows a curve of input unbalance current as a function of temperature. This unbalance current determines the maximum value of total effective external resistance that may be used in each base circuit (resistors $R_1$ in Fig. 2). A maximum value of 10,000 ohms is recommended for each base circuit. However, larger resistances may be accommodated if the resistors can be adjusted to maintain low input offset voltages, or if the operating points of $Q_1$ and $Q_5$ are not in the linear region (as in trigger circuits).

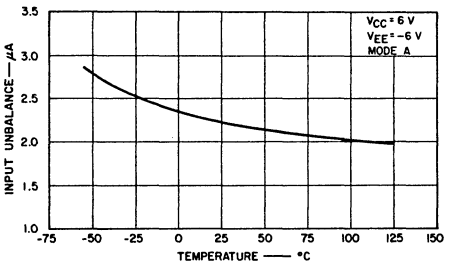



*Fig. 5—Input unbalance current of the CA3002 as a function of temperature.*

**Input Impedance.** The input impedance is essentially a characteristic of the input emitter-followers, $Q_1$ and $Q_2$. Because these transistors are lightly loaded, they have parallel input impedances that are approximately 0.1 megohm at low frequencies and rise to infinity and become negative at a few megahertz. In most cases, these impedances are negligible in comparison with the impedances of external base resistors or inductors. The input capacitance is 3 to 5 picofarads.

The input impedance decreases with decreasing operating temperature. A typical low-frequency value of parallel input resistance is 55,000 ohms at −55°C. If a resonant line or tuned circuit that has appreciable impedance in the vhf range is connected to either input terminal, a series parasitic resistor of 50 to 100 ohms should be placed in series with the input lead to prevent vhf oscillation.

**Output Impedance.** The output impedance is essentially that of the output emitter-follower $Q_6$, and is a function of the current in $Q_6$. The current, in turn, is determined by the operating mode, the supply voltages, and the connection of resistor $R_6$ to ground or to terminal 2. In operating mode D with $R_6$ returned to ground and ±6-volt supplies, the output resistance is approximately 80 ohms over most of the useful frequency range and rises to about 110 ohms (its highest value) at −55°C.

**Frequency Response.** The mid-frequency voltage gain of the CA3002 if amplifier is essentially independent of absolute resistor values, but depends on the resistor ratios. Fig. 6

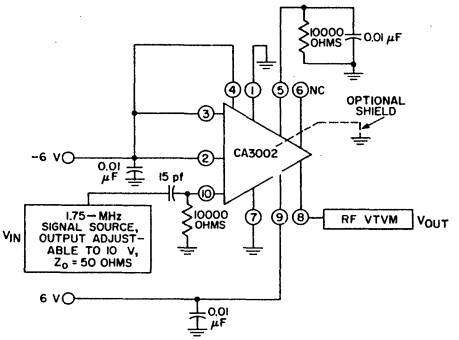
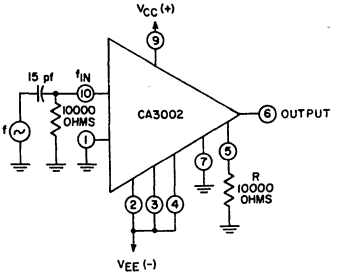



*Fig. 6—Voltage-gain test circuit.*

shows a test circuit used to measure the response characteristics of an iterative-coupled amplifier that uses an input-coupling capacitor of 15 picofarads.

The response curves for several values of positive and negative supply voltage are shown in Fig. 7. The gain of the



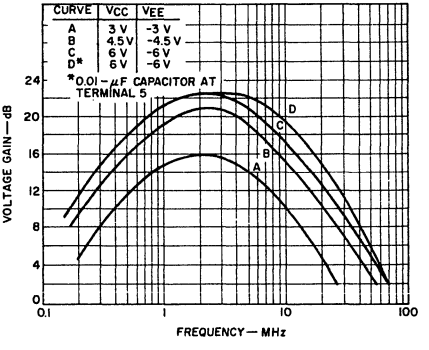
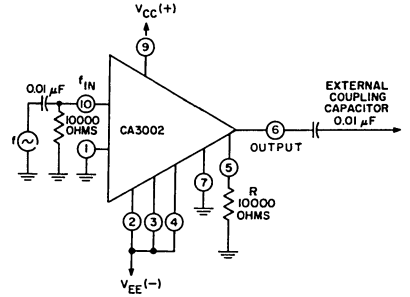




*Fig. 7—Effective single-stage response characteristics of iterative-coupled if amplifier. Curve D represents operation with 0.01-microfarad capacitor connected at terminal 5 (not shown).*

amplifier is reduced at low frequencies by the 15-picofarad input-coupling capacitor and at high frequencies by the RC roll-off within the circuit. The addition of a 0.01-microfarad bypass capacitor at terminal 5 improves both the high-frequency response and the mid-frequency gain by eliminating ac feedback from terminal 8 to terminal 5.

If a wideband video response is desired, the 15-picofarad internal silicon output-coupling capacitor of the CA3002 must be replaced with a larger external coupling capacitor connected to terminal 6. The response curves for an iterative-coupled amplifier that uses 0.01-microfarad input-coupling and output-coupling capacitors are shown in Fig. 8.



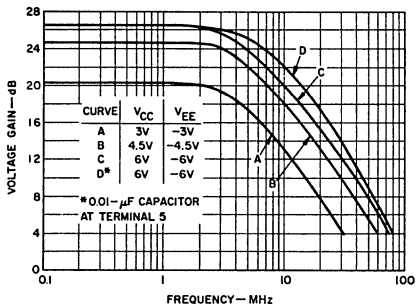




*Fig. 8—Effective single-stage response characteristics for if amplifier using 0.01-microfarad coupling capacitors. Curve D represents operation with 0.01-microfarad capacitor connected at terminal 5 (not shown).*

The response of the amplifier is substantially extended at the low frequencies. If 1-microfarad coupling capacitors are used, the low-frequency response can be extended below 100 Hz. Again, the addition of a 0.01-microfarad capacitor at terminal 5 improves the high-frequency performance. A shield separating the external leads at terminals 5 and 6 also reduces the feedback and extends the response.

**AGC.** The voltage gain of the CA3002 can be controlled over a wide range by adjustment of a negative dc voltage applied at terminal 1. Fig. 9 shows the voltage gain at 1.75 MHz (measured in the test circuit of Fig. 6) as a function

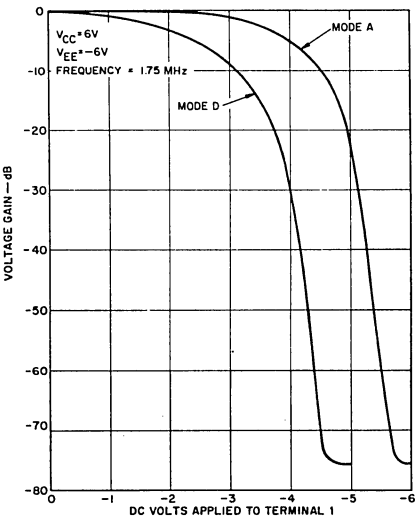



*Fig. 9—Voltage gain of the CA3002 as a function of negative dc supply voltage applied at terminal 1 (normalized to a gain of 26 dB).*

of the dc voltage. When the gain is controlled in this manner, the CA3002 can be used as an if amplifier with a 75-dB agc range, or as a video gating, squelching, or blanking circuit with a similar range. The circuit function depends only on the manner in which the dc voltage applied to terminal 1 is controlled. The agc range is dependent on frequency, and decreases from 75 dB at 1 MHz to 60 dB at 25 MHz.

**Third-Order Intermodulation Distortion.** Fig. 10 shows the peak-to-peak input signal required to produce third-order intermodulation distortion of 3 per cent as a function of gain control for the CA3002 integrated circuit. The maximum tolerable signal input for 3-per-cent intermodulation dis-

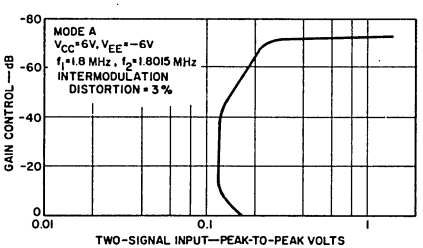



*Fig. 10—Third-order intermodulation-distortion characteristic as a function of agc.*

tortion is relatively constant over the entire agc range, but increases dramatically as cutoff is attained. When the CA3002 is operated in mode A with supplies of ±6 volts and an agc of −30 dB, a peak-to-peak input signal in excess of 100 millivolts is typically required for 3-per-cent distortion.

**Noise Figure.** Because noise figure is an important design parameter for both video and if-amplifier applications, it was evaluated for the CA3002 over the frequency range of 1 kHz to 10 MHz. Fig. 11 shows noise performance as a function of frequency when a 1000-ohm source is used. The noise figure is 4 dB over a large portion of the usable

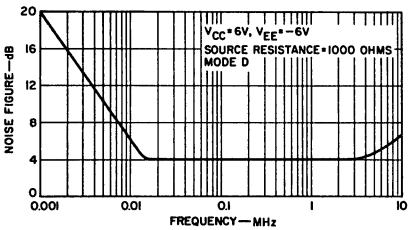



*Fig. 11—Noise figure of the CA3002 as a function of frequency.*

range. The 1/f noise corner occurs at approximately 15 kHz, and the high-frequency noise rise begins at approximately 4 MHz. Fig. 12 shows noise figure as a function of source resistance at 1.75 MHz. The typical noise figure is less than 4 dB. It is reasonably flat for source resistances from 500 to 2500 ohms, but rises rapidly at values below 500 ohms.

When external base-bias resistors are used, terminal 5 should be bypassed by an external capacitor for any stage which low noise figure is required. If the base-bias resistors are not bypassed, the noise figure increases. In a practical receiver, bypassing may be avoided if the input at terminal 10 is transformer driven (from a filter) and terminal 5 is grounded. In the later if stages, noise figure can usually be ignored.

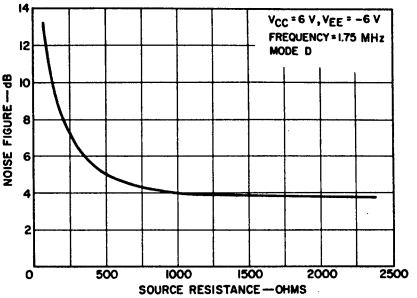



*Fig. 12—Noise figure of the CA3002 as a function of source resistance.*

## APPLICATIONS

**Four-Stage 1.75 MHz IF Amplifier.** Effective if design for AM circuits requires consideration of both the signal level at the input stage (as a function of agc range) and the acceptable signal-to-noise ratio at the output. The agc action must be initiated at the first stage at the proper voltage level to prevent excessive modulation distortion throughout the entire agc range. This input-signal voltage level is calculated to be approximately 25 millivolts rms for 100-per-cent modulation at an allowable distortion of 10 per cent. Before the applied signal reaches 25 millivolts, the first stage must be gain controlled and completely cut off before gain control is applied to subsequent stages.

Fig. 13 shows a four-stage 1.75-MHz amplifier used to evaluate the performance of the CA3002 amplifier for AM

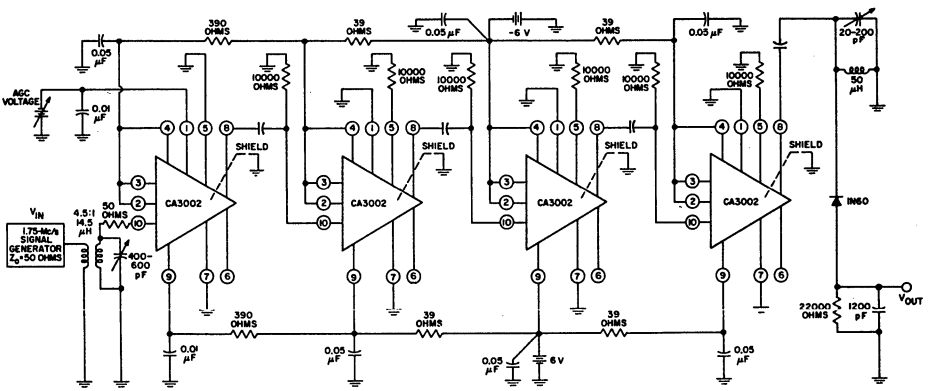



*Fig.13—Four-stage 1.75-MHz if amplifier.*

applications. A tuned circuit and a diode detector are connected to terminal 8 of the output stage to evaluate detected output and signal-to-noise ratio. The audio bandwidth of the detector output filter is 3 dB down at 4.2 kHz. The tuned circuit at the input is driven by a 50-ohm generator and provides a 1000-ohm source to the circuit. The first stage is operated at reduced supply voltages (about ±3 volts) to reduce the required agc control voltage. This lower supply-voltage level ensures that a sufficient control voltage can be developed by a separate CA3002 unit used as an agc amplifier without introducing a separate supply voltage. An additional advantage of lower-voltage operation in the first stage is a reduction in noise figure.

If desired, the first-stage tuned circuit in Fig. 13 can be replaced by a crystal filter and a transformer. Because the CA3002 input impedance is high and does not vary appreciably with agc, no impedance variations are presented to the crystal filter.

The voltage gain realized from terminal 10 of the first stage to terminal 8 of the fourth stage is 85 dB, or approximately 21 dB per stage. From the 50-ohm input, the typical voltage gain is 98 dB. Because the maximum signal-handling capability of the output stage is slightly greater than 0.7 volt rms, gain control should begin when this value is measured at terminal 8. The modulation distortion is acceptable over the entire 60-dB agc range. For input signals greater than 8 millivolts, modulation distortion begins to increase because of fourth-stage overload. Overloading can be prevented by application of a delayed gain control to the second stage. The signal-to-noise performance as a function of input signal is shown in Fig. 14.

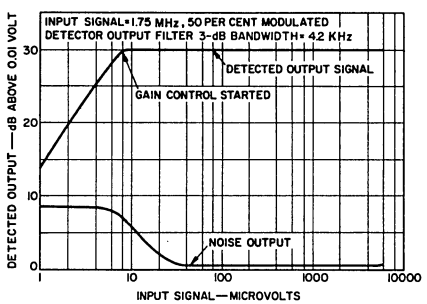



*Fig. 14—Output signal and noise of the amplifier shown in Fig. 13.*

**Envelope Detector.** The CA3002 integrated circuit can be operated as an envelope detector in either of two ways, as shown in Fig. 15: (1) the emitter of the output transistor $Q_6$ can be operated at zero voltage by connection of an external resistor in the bias loop of the constant-current transistor $Q_3$, or (2) the current in transistor $Q_6$ can be reduced by connection of a large resistor (12,000 to 18,000 ohms) in series with its emitter resistor.

In the circuit for method 1, the current in the differential pair ($Q_2$ and $Q_4$ in Fig. 1) is increased to the point at which the common-collector output transistor $Q_6$ is biased almost to cutoff. For this current increase, the constant-current transistor $Q_3$ is operated with terminal 4 open, and the emitter resistor $R_6$ is shunt loaded by the external resistor at terminal 3. Envelope detection can be accomplished only in mode A with method 1.

Although the output transistor is nearly cut off, all the other active devices are operating in their linear regions.

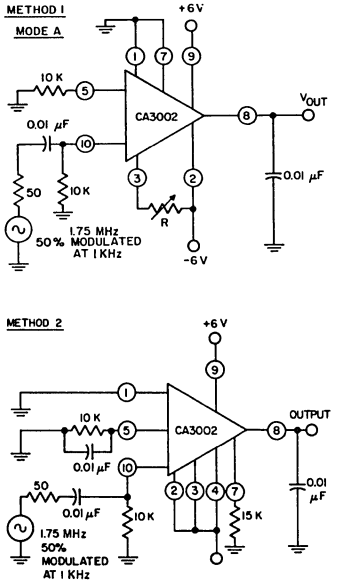



*Fig. 15—Envelope detectors using CA3002 integrated circuits.*

For small ac signals, therefore, the circuit provides linear operation except for $Q_6$, which is turned on only by a positive signal. The maximum acceptable input signal depends on the linear range of the differential amplifier. An external filter capacitor is connected between terminal 8 and ground to remove the rf signal from the detected audio output.

In the circuit diagram for method 2 shown in Fig. 15, a fixed value of resistance (15,000 ohms) is used to reduce the emitter current in the output transistor ($Q_6$) to approximately 100 microamperes. This operating point provides the nonlinearity for detection in transistor $Q_6$. Again, the remainder of the circuit produces gain because it is operating linearly. As in the case of method 1, an external filter capacitor is connected between terminal 8 and ground to remove the rf signal from the detected audio output.

Fig. 16 shows the input-output characteristics of the envelope-detector circuits shown in Fig. 15. The usable range of input signals for distortion below 3 per cent is 10 to 100 millivolts (20-dB range) for method 1 and 12 to 60 millivolts (14-dB range) for method 2. Automatic gain control of the if amplifier must maintain the input signals to the detector within this range.

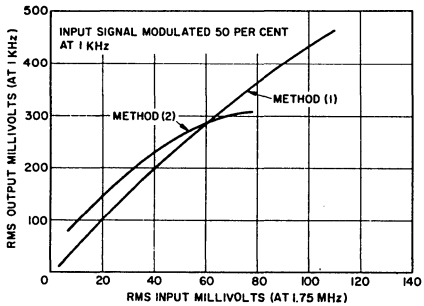



*Fig. 16—Input-output characteristics of the envelope detectors shown in Fig. 15.*

**Product Detector.** A differential pair driven by a constant-current transistor can be used as a product detector if a suppressed-carrier signal is applied to the differential pair and the regenerated carrier is applied to the constant-current transistor. There are two requirements for linearity: (1) the circuit must be operated in a linear region, and (2) the current from the constant-current transistor must be linear with respect to the reinserted carrier voltage.

The CA3002 satisfies these requirements and can be used as a product detector in the circuit shown in Fig. 17. A double-sideband suppressed-carrier signal is applied at terminal 10, and the 1.7-MHz carrier is applied to terminal 1.

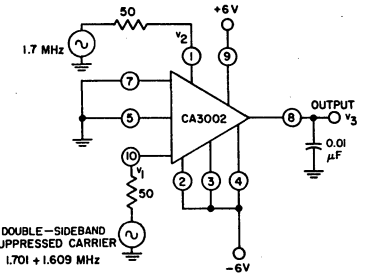



*Fig. 17—Product detector circuit.*

Because of the single-ended output, a high-frequency bypass capacitor (0.01 microfarad) is connected between terminal 8 and ground to provide filtering for the high-frequency components of the oscillator signal at the output.

When the amplitude of the suppressed-carrier signal and of the oscillator signal are varied, the gain and distortion characteristics shown in Table III are obtained. The conversion voltage gain is constant at input signals up to 16 millivolts and would be 6 dB less for a single-sideband signal than for the double-sideband signal. The distortion increases with increasing input signal; for distortion of less than 1 per cent, the input drive level does not exceed 8 millivolts. The gain maximizes for oscillator voltages of 1 to 2 volts, and the distortion characteristic is also best in this region. Distortion increases both at low oscillator drive levels (0.25 volt) and at high levels (3 volts).

**Schmitt Trigger.** Fig. 18 shows the use of the CA3002 as a Schmitt trigger. In this application, the input is applied to terminal 5 and both the output and the feedback are taken from the output emitter-follower at terminal 8. The emitter-follower output isolates the feedback loop from the differ-

Table III—Performance Data for CA3002 as Product Detector

| $v_1$ Double-Sideband Voltage (mV) | $v_t$ Oscillator Voltage at Terminal 1 (V) | $v_3$ Output at Terminal 8 at 1 kc/s (mV) | Conversion Voltage Gain (dB) | dB down from Fundamental of Harmonics * | | | |
|---|---|---|---|---|---|---|---|
| | | | | Harmonic | | | |
| | | | | 2nd | 3rd | 4th | 5th |
| 1 | 1.7 | 12.5 | 21.9 | 60 | | | |
| 4 | 1.7 | 50 | 21.9 | 51 | 61 | | |
| 8 | 1.7 | 100 | 21.9 | 46 | 56 | | |
| 16 | 1.7 | 200 | 21.9 | 37 | 46 | | |
| 32 | 1.7 | 310 | 19.8 | 32 | 30 | 51 | 64 |
| 4 | 0.25 | 22 | 15.6 | 15 | 42 | 44 | |
| 4 | 0.5 | 42 | 20.3 | 32 | 52 | | |
| 4 | 1.0 | 60 | 23.5 | 45 | 60 | | |
| 4 | 1.3 | 60 | 23.5 | 49 | 61 | | |
| 4 | 1.7 | 50 | 21.9 | 51 | 61 | | |
| 4 | 2.0 | 48 | 21.6 | 52 | 62 | | |
| 4 | 2.5 | 31 | 17.8 | 49 | 60 | | |
| 4 | 3.0 | 15 | 11.4 | 42 | 60 | | |

*Harmonic Distortion Greater than 65 dB Down If Omitted

ential pair and makes it possible for the circuit to drive low-impedance loads. An additional advantage is that neither half of the differential pair saturates as the resistance of the feedback loop is varied. Fig. 18 also shows the output swing and associated hysteresis of the Schmitt trigger as a function of resistor R and the dc input voltage level at terminal 5.

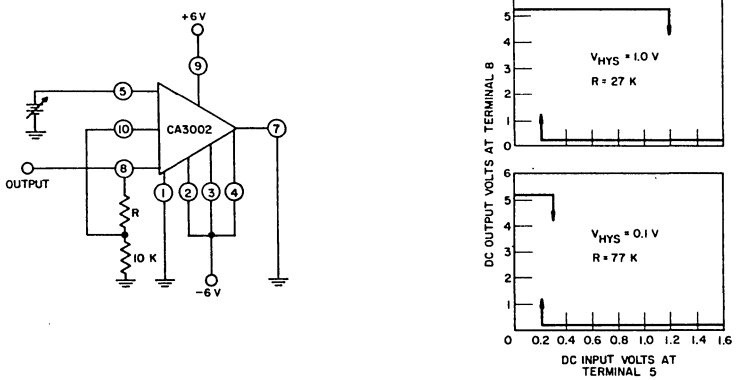



*Fig. 18—Schmitt trigger circuit and output swing and associated hysteresis.*

# Application of the RCA-CA3007 Integrated-Circuit Audio Amplifier

by
R.G. TIPPING

The RCA-CA3007 audio driver is a balanced differential configuration with either a single-ended or a differential input and two push-pull emitter-follower outputs. The circuit features all-monolithic silicon epitaxial construction, and is intended for use as a direct-coupled driver in a class B audio amplifier which exhibits both gain and operating-point stability over the temperature range from -55 to 125°C. Because of its circuit configuration (a balanced differential pair fed by a constant-current transistor), the CA3007 is an excellent controlled-gain audio driver for systems requiring audio squelching. This circuit is also usable as a servo driver. The audio driver circuit is available in a 12-terminal TO-5 low-silhouette package.

## CIRCUIT DESCRIPTION

Fig.1 shows the schematic diagram and terminal connections for the CA3007 circuit. The input stage consists of a differential pair ($Q_1$ and $Q_2$) operating as a phase splitter with gain. The two output signals from the phase splitter, which are 180 degrees out of phase, are direct-coupled through two emitter-followers ($Q_4$ and $Q_5$). The emitters of the differential pair are connected to the transistor constant-current sink $Q_3$.

The diodes in the bias circuit of the transistor constant-current sink make the emitter current of $Q_3$ essentially dependent on the temperature coefficient of the diffused emitter resistor $R_3$. Because the diffused collector resistors $R_{15}$ and $R_{16}$ should have identical temperature coefficients, constant collector-voltage operating points should result at the collectors of transistors $Q_1$ and $Q_2$. However, the quiescent operating voltages at the output terminals 8 and 10 increase as temperature increases because the base-emitter voltage drops of transistors $Q_4$ and $Q_5$ decrease as temperature increases. This small variation in the output quiescent operating voltage is sufficient to cause a large variation in the standby current of a class B push-pull output stage when the audio driver and the output stage are direct-coupled. Resistors $R_{11}$, $R_{12}$, $R_{13}$, and $R_{17}$ and transistor $Q_6$ form a dc feedback loop which stabilizes the quiescent operating voltage at output terminals 8

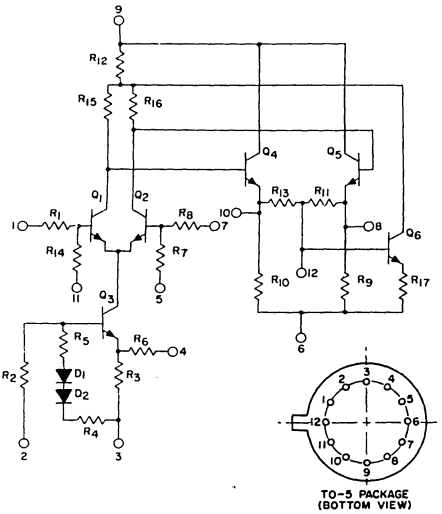



*Fig.1 - Schematic diagram and terminal connections for the CA3007 audio driver.*

and 10 for both temperature and power-supply variations so that variations in the output operating points are negligible.

Resistors $R_1$, $R_7$, $R_8$, and $R_{14}$ form the input circuit; a double-ended input is applied to terminals 1 and 5, and a single-ended input is applied to either terminal 1 or terminal 5, with the other terminal returned to ground. The CA3007 must be ac-coupled to the input source. In addition, any dc resistance between terminal 1 and ground should be added between terminal 5 and ground. Output power-gain stabilization for a direct-coupled driver and output stage is accomplished by means of an ac feedback loop that connects terminals 7 and 11 to the proper emitters of the push-pull output stage, as shown in Fig.2.

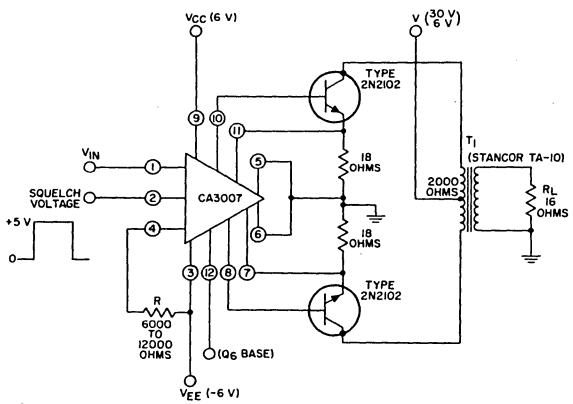



*Fig.2 - CA3007 used as an audio driver for a direct-coupled 300-milliwatt audio amplifier.*

Connection of voltage supplies to the CA3007 audio driver requires that the most positive voltage be connected to terminal 9 and the most negative voltage to terminal 3 (internally connected to the substrate and the case). The CA3007 may be operated from various supplies and at various levels. Operation from either a single supply (as shown in Fig.3) or from dual power supplies (as shown in Fig.2) is feasible. For dual-supply operation, symmetrical supplies must be used if the audio driver is to be direct-coupled to the audio output stage. For single-supply operation, the audio driver must be ac-coupled to the audio output stage, and the number of external components required increases.

The external resistor R connected between terminals 3 and 4 is used to set the class B output-stage standby current as required for a particular application. If the standby current is too low, crossover distortion will result; if it is too high, standby power drain will be excessive. Decreasing the value of resistor R reduces the standby current; for a standby current of 10 milliamperes, R is typically 10,000 ohms.

Terminal 2 must be grounded or, if an audio squelch is desired, must be connected to a positive voltage supply of 5 volts minimum. When terminal 2 is near ground, the audio amplifier functions normally. When

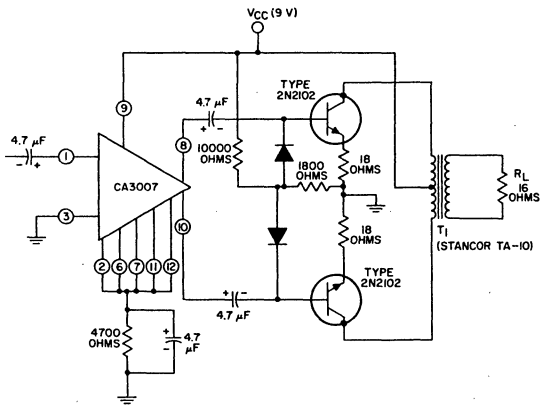



*Fig.3 - CA3007 used as an audio driver for a 30-milliwatt audio amplifier.*

For operation from either single or dual supplies, the operating current is transistor $Q_3$ is determined by the bias voltage between terminals 2 and 3. The more negative terminal of this bias voltage must be connected to terminal 3. For dual-supply systems, terminal 2 is either grounded or connected to a trigger circuit for audio-squelching purposes.

## APPLICATIONS

**Dual-Supply Audio Driver in a Direct-Coupled Audio Amplifier.** Fig.2 shows the CA3007 used as a dual-supply audio driver in a direct-coupled audio amplifier. This amplifier provides a power output of 300 milliwatts for an audio input of 0.3 volt rms ($V_{CC}$ = 6 volts, $V_{EE}$ = -6 volts, V = 30 volts). For a voltage V of 6 volts, the output power is 10 milliwatts without transformer optimization; the use of a lower-impedance transformer would permit power outputs in the order of 100 milliwatts.

terminal 2 is at 5 volts, the differential pair of the audio driver saturates, and the push-pull output stage is cut off. The squelch source must be capable of supplying a current of 1.5 milliamperes in the 5-volt condition, and 0.75 milliampere in the near-ground condition.

For a symmetrical audio driver, there is no ac signal present at the base of transistor $Q_6$. However, unbalances between the two halves of the circuit may require that the base of $Q_6$ be bypassed for proper operation. The base of $Q_6$ may be bypassed by connection of an external capacitor (typically 50 microfarads, 6 volts) from terminal 12 to ground. Bypassing is usually not required unless high undistorted power outputs are required over the complete temperature range of -55 to 125°C.

Table I shows values of harmonic distortion and intermodulation distortion for the amplifier of Fig.2.

Table I - Distortion Measurements for Direct-Coupled Amplifier Shown in Fig.2

**HARMONIC DISTORTION**

| *Power Output (mW)* | *Output-Signal Level (mVrms) with 2-kHz Input Signal* | | | | | | *Harmonic Distortion (%)* |
|---|---|---|---|---|---|---|---|
| | *2 kHz* | *4 kHz* | *6 kHz* | *8 kHz* | *10 kHz* | *12 kHz* | |
| 62.5 | 1000 | 9 | 3.0 | — | — | — | 0.95 |
| 140 | 1500 | 18 | 4.0 | 2.0 | 1.4 | 1.0 | 1.24 |
| 250 | 2000 | 25 | 4.2 | 5.0 | 1.0 | 1.5 | 1.30 |
| 330 | 2300 | 27 | 6.0 | 9.0 | 3.0 | 2.0 | 1.27 |

**INTERMODULATION DISTORTION**

Output-Signal Level:

| | |
|---|---|
| at $f_1$ (2 kHz) | 1000 mV rms |
| at $f_2$ (3 kHz) | 1000 mV rms |
| at $2f_2$-$f_1$ (4 kHz) | 0.7 mV rms |
| 3rd-Order IMD | 0.07 % |

**Single-Supply Audio Driver in a Capacitor-Coupled Audio Amplifier.** Fig.3 shows the CA3007 used as a single-supply audio driver in a capacitor-coupled audio amplifier. This amplifier provides a power output of 30 milliwatts for an audio input of 6.5 millivolts rms ($V_{CC}$ = 9 volts) with the transformer shown.

The connection shown in Fig.3 still represents a differential-pair phase splitter fed from a constant-current transistor. The two output signals from the phase splitter are direct-coupled through two emitter-followers which are capacitor-coupled to the push-pull output stage. Because of the ac coupling, there is no longer a dc dependence between the driver and the output stage, and any desired audio output design or drive source may be used. As a single stage, the CA3007 audio driver provides a voltage gain of 24 dB for a dc power dissipation of 20 milliwatts with the harmonic distortion reaching 3 per cent for outputs of 0.6 volt rms at terminals 8 and 10 (without feedback).

Both dc and ac feedback loops are eliminated in the circuit of Fig.3. Although the dc feedback loop is no longer required bacause of the ac coupling, removal of the ac feedback loop causes the output power gain to decrease about 1 dB for a 50°C rise in temperature.

# Application of the RCA-CA3001 Integrated-Circuit Video Amplifier

BY
G. E. THERIAULT

The CA3001 silicon monolithic integrated circuit is designed for use in intermediate-frequency or video amplifiers at frequencies up to 20MHz and in Schmitt-trigger applications. This integrated circuit can be gated, and gain control can be applied. The CA3001 incorporates the following primary features: (a) all-monolithic silicon epitaxial construction designed for operation at ambient temperatures from —55 to 125°C; (b) balanced differential-amplifier configuration with low-impedance double-ended input; (c) built-in temperature-compensating network for gain or dc operating-point stability over the temperature range from —55 to 125°C. This integrated-circuit amplifier is available in a 12-pin TO-5 low-silhouette package.

## CIRCUIT DESCRIPTION

Fig. 1 shows the schematic diagram and terminal connections for the CA3001 amplifier. The circuit consists of a differential pair $Q_3$ and $Q_5$, the current of which is controlled by a constant-current transistor $Q_4$. Transistors $Q_1$, $Q_2$, $Q_6$, and $Q_7$ are operated in the common-collector configuration to provide a high-impedance input and low-impedance output. Thus, the CA3001 provides double-ended input and output, and can be iteratively connected with low-value coupling capacitors. The high-frequency response of the circuit is determined primarily by the resistance and capacitance in the collectors of the differential pair $Q_3$ and $Q_5$.

## BIASING

When voltage supplies are connected to the CA3001, the most positive voltage must be connected to terminal 9 and the most negative voltage to terminal 3 (internally connected to the substrate and the case). For typical operation, terminals 2 and 10 are returned to ground. If desired, however, automatic gain control can be applied to terminal 2, and terminal 10 can be connected to the negative supply to permit larger negative-going output swings in the output transistors.

The CA3001 may be operated with various supplies and at various levels. Operation from either a single supply or dual supplies is feasible, as shown in Fig. 2. When dual supplies are used, they may be either symmetrical or nonsymmetrical. The use of separate positive and negative supplies minimizes the need for external components, as shown in Fig. 2(a). For single-supply applications, a resistor divider and a bypass capacitor must be added, as shown in Fig. 2(b).

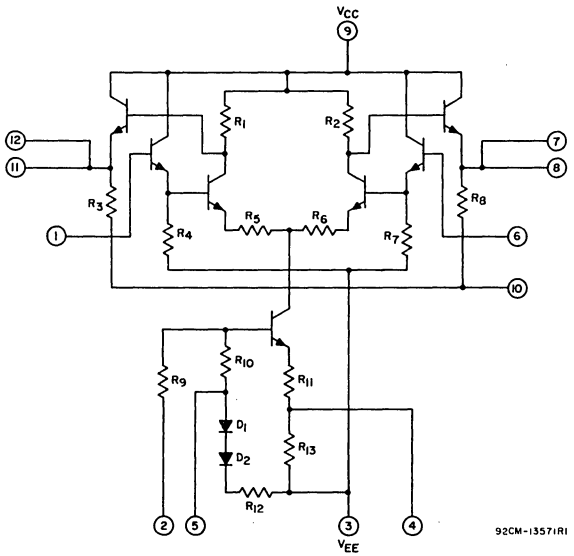



*Fig.1 - Schematic diagram and terminal connections for the CA3001 video amplifier.*

When dual supplies are used, the inputs (terminals 1 and 6) are referenced to ground through equal external resistors (the maximum recommended value of R is 3300 ohms for linear operation). The current through the resistor divider $R_1$ and $R_2$ should be greater than 1.5 milliamperes. For either single or dual supplies, the operating current in transistor $Q_4$ is determined by the operating mode. For any given bias voltage, four operating modes are possible, as described in Table I. Each mode is characterized by a distinct operating current and a corresponding voltage gain, both of which have a particular temperature dependence.

Table I—Four Possible Operating Modes for CA3001 Amplifier

| *Operating Mode* | *Shorted Terminals* | *Condition of Diodes* | *$Q_4$ Emitter Resistor* |
|---|---|---|---|
| A | none | in | $R_{11} + R_{13}$ |
| B | 5-3 | out | $R_{11} + R_{13}$ |
| C | 4-3 | in | $R_{11}$ |
| D | 5-4-3 | out | $R_{11}$ |

Table II shows typical design performance characteristics for the four operating modes of the CA3001 at room temperature. The output operating point and voltage gain of the circuit are reasonably independent of resistor value, but the

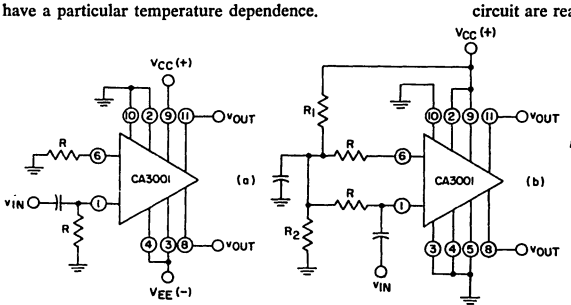



*Fig.2 - Circuit connections for the CA3001 for (a) separate positive and negative voltage supplies, and (b) a single supply.*

Table II—Typical Design Performance Characteristics for the CA3001 Amplifier (terminals 2, 10, 6, and 1 referenced to ground) at 25°C

| Operating Mode | Supplies (±V) | Output Operating Volts (Terminals 8 and 11 To Ground) | Positive Supply Current (mA) | Negative Supply Current (mA) | Power Dissipation (mW) | Single-Ended Voltage Gain at 1 MHz (dB) |
|---|---|---|---|---|---|---|
| A | 6 | 4.3 | 8.4 | −4.7 | 79 | 15.5 |
| B | 6 | 4.8 | 7.8 | −3.9 | 70 | 12.7 |
| C | 6 | 2.8 | 9.9 | −7.9 | 106 | 17.8 |
| D | 6 | 4.1 | 8.7 | −5.5 | 85 | 16.4 |
| A | 4.5 | 3.0 | 6.0 | −3.4 | 43.6 | 14.6 |
| B | 4.5 | 3.4 | 5.6 | −2.7 | 37.6 | 10.0 |
| C | 4.5 | 2.0 | 7.2 | −5.8 | 58.4 | 17.7 |
| D | 4.5 | 2.9 | 6.0 | −3.7 | 43.6 | 15.5 |
| A | 3 | 1.8 | 3.7 | −3.9 | 22.6 | 13.0 |
| B | 3 | 2.1 | 3.3 | −1.4 | 14.3 | 3.8 |
| C | 3 | 1.0 | 4.4 | −3.7 | 25.5 | 16.4 |
| D | 3 | 2.0 | 2.4 | −1.9 | 13.0 | 10.8 |

current and power dissipation may vary with resistor values. Figs. 3 and 4 show theoretical curves of output operating point and power gain, respectively, as functions of temperature for nominal resistor values with supply voltage $V_{EE}$ of −3 and −6 volts dc. The voltage between terminals 8 and 9 or terminals 11 and 9 is denoted by $V_X$. Because the variation of voltage gain and operating point with temperature is small for all operating modes, the choice of mode depends on application requirements. With a supply voltage $V_{EE}$ of −4.5 volts, voltage-gain variation is normally less than 0.5 dB for all operating modes over the temperature range of −55 to 125°C.

## CHARACTERISTICS

**Frequency Response.** When the CA3001 video amplifier is used in cascade, its high-frequency response is determined primarily by the RC roll-off at the collectors of the differential pair $Q_3$ and $Q_5$. The generator source resistance may affect high-frequency bandwidth; for full bandwidth capability, the parallel combination of source resistance and base-bias resistance should not exceed 800 ohms. The low-frequency response is determined by the coupling capacitor and the base-bias resistance value.

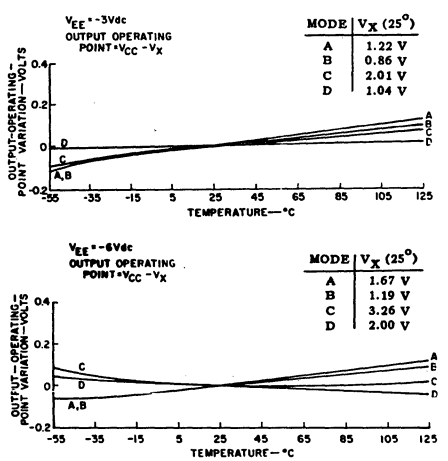



*Fig.3 - Output operating point of the CA3001 (normalized to the 25°C operating point) as a function of temperature for $V_{EE}$ supplies of -3 and -6 volts dc.*

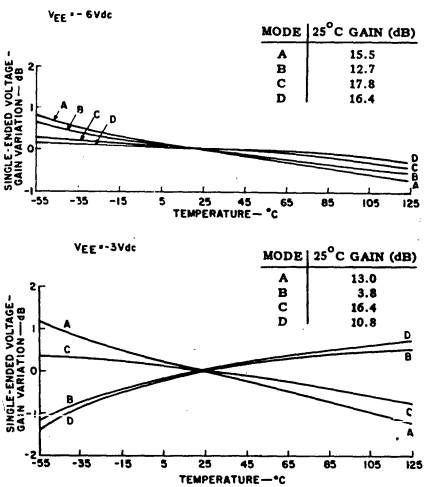



*Fig.4 - Voltage gain of the CA3001 (normalized to the 25°C gain) as a function of temperature for $V_{EE}$ supplies of -3 and -6 volts dc.*

Fig. 5 shows the circuit used for evaluation of frequency response of the CA3001, together with the response characteristics obtained. The circuit is operated in mode C with supplies of ±6 volts. The 50-ohm generator simulates the frequency and gain behavior for iterative operation. The curves of Fig. 5 show the measured response characteristics with terminal 6 bypassed and unbypassed. When terminal 6 is bypassed, the voltage gain is down 3 dB at 16 MHz,

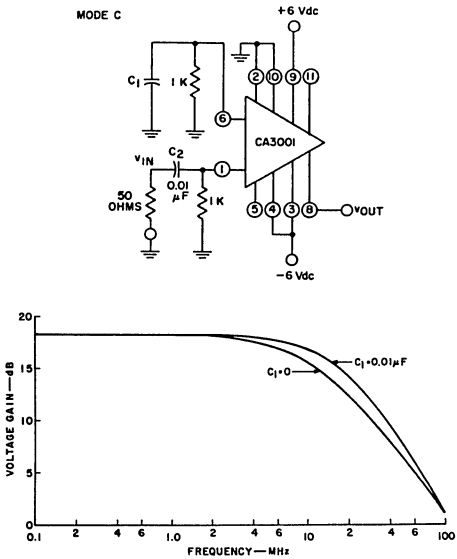



*Fig.5 - Frequency response of the CA3001 as a function of capacitor $C_1$ in the test circuit shown with terminal 6 bypassed and unbypassed.*

and is greater than 10 dB through 30 MHz. When the non-driven input (terminal 6 in the circuit shown) is not bypassed, the gain decreases more rapidly as a result of the feedback capacitance between terminals 7 and 6. This feedback can be minimized by use of short leads and inter-terminal shielding. A shielding method is to ground terminal 7.

The high-frequency roll-off of the CA3001 is a function of the values of resistors $R_1$ and $R_2$ in Fig. 1 and their variation with temperature. Fig. 6 shows the effect of temperature on high-frequency response. The variation in response can be accounted for by the resistance variation with temperature; capacitance variations with temperature are a secondary effect.

The internal capacitors provided at the outputs of the CA3001 ($C_1$ and $C_2$ in Fig. 1) can be used for coupling circuits in cascade for narrow-band applications. Because

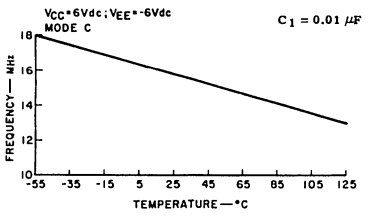



*Fig.6 - High-frequency 3-dB bandwidth of the CA3001 as a function of temperature.*

the value of these capacitors is small, the external base-bias resistors shown in Fig. 5 should be increased from 1000 to 3300 ohms to improve low-frequency response. Fig. 7 shows the response characteristics for a single stage in which the input is applied to terminal 1 from a 50-ohm generator through a capacitor (equal in value to $C_2$ in Fig. 1), and the voltage gain is measured from the generator to output terminal 8. Because this arrangement simulates single-ended operation, the results can be applied directly to iterative operation.

The voltage division between the input capacitance and the coupling capacitor causes a reduction in voltage gain at all frequencies. The feedback capacitance from output to input also affects the gain performance, as shown in Fig. 7.

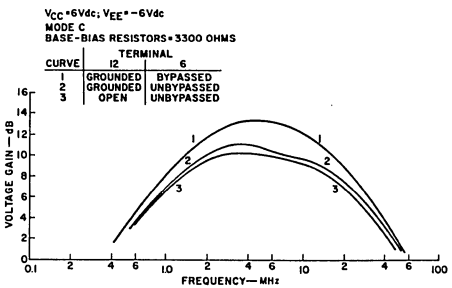



*Fig.7 - Response characteristics of a CA3001 amplifier with capacitor-coupled input.*

**Input and Output Impedance.** Fig. 8 shows the parallel input resistance and capacitance of the CA3001 as a function of frequency. The input capacitance is constant until it begins to decrease at high frequencies. The input resistance decreases through the frequency range from 0.1 to 10 MHz. Because the input resistance is high in comparison with the external base-bias resistors used (3300 ohms maximum), the high-frequency response characteristic of the input is determined by the driving-source resistance, the base-bias resistors, and the parallel input capacitance.

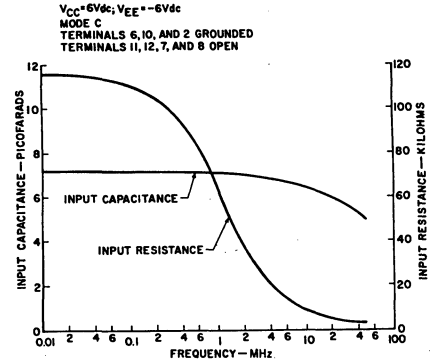



*Fig.8 - Parallel input resistance and capacitance of the CA3001 as functions of frequency.*

The parallel output resistance of the CA3001 is low (approximately 70 ohms), and the output reactance is sufficiently high to provide little or no degradation of frequency response through the usable frequency range.

**Noise Figure.** Fig. 9(a) shows noise figure as a function of frequency for a 1000-ohm source. The 1/f noise corner occurs at approximately 30 kHz; above this frequency, the noise figure remains flat at approximately 5 dB to 6 MHz, and then begins to rise.

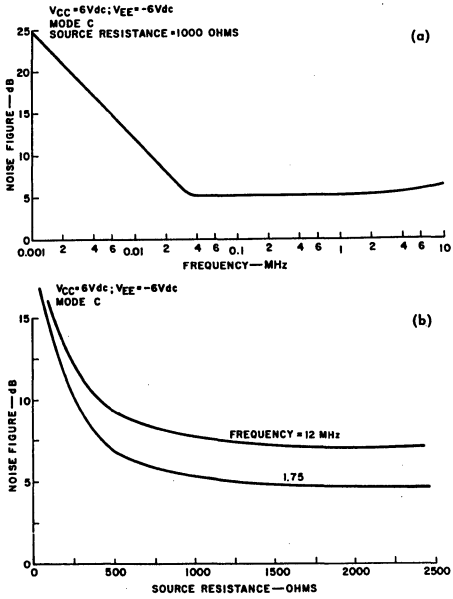



*Fig.9 - Noise figure of the CA3001 as a function of frequency and source resistance.*

Fig. 9(b) shows noise figure as a function of source resistance for frequencies of 1.75 and 12 MHz. For stages in which noise performance is important, the source resistance should not be less than 500 ohms because of the rapid rise in noise figure at lower values. The noise figure of the CA3001 increases when non-driven base-bias resistors are unbypassed. For stages in which noise performance is important, the external resistor on an input base that is not receiving a signal must be bypassed if minimum noise figure is to be achieved.

**Gain Control.** AGC can be applied to the CA3001 at terminal 2 for any of the four operating modes. Fig. 10 shows representative agc characteristics for modes C and D at a frequency of 1 MHz. The threshold voltage is higher in mode C than in mode D because of the difference in the base-bias circuit for the constant-current sink transistor ($Q_4$).

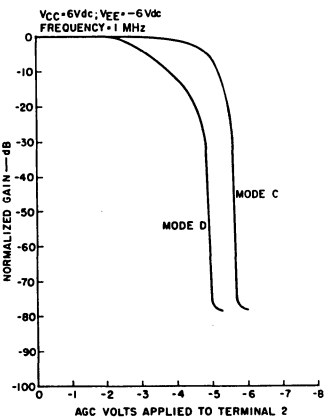


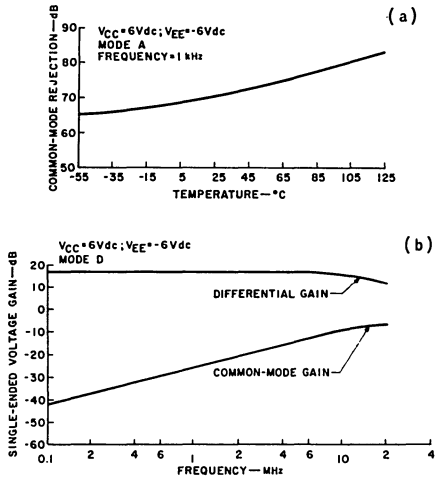

*Fig.10 - AGC characteristics of the CA3001 in modes C and D at 1 megahertz.*

The agc range is dependent on frequency. At high frequencies, because the feedthrough parameters are primarily capacitive, it should eventually decrease at a rate of approximately 20 dB per decade. The average measured agc range at 10 MHz is 62 dB, and is 15 dB less than that at 1 MHz.

**Common-Mode Rejection.** The common-mode rejection of a differential amplifier is defined as the ratio between the full differential gain and the common-mode gain. It is a useful performance characteristic, particularly at low

frequencies. Fig. 11(a) shows the common-mode rejection of the CA3001 as a function of temperature at a frequency of 1 kHz. The common-mode rejection increases with increasing temperature; a typical value at 25°C is 70 dB.

Because the CA3001 can be used in many applications with a single-ended output at high frequencies, both the single-ended differential gain and the single-ended common-mode gain are of considerable interest. Fig. 11(b) shows




both single-ended common-mode and differential-mode gain as functions of frequency. The common-mode gain is a function of the impedance ratio between the constant-current transistor ($Q_4$) and the load resistor in one side of the differential pair ($Q_3$ or $Q_5$). The common-mode gain increases with increasing frequency.

The common-mode rejection is degraded if sufficient signal is applied to saturate the constant-current transistor ($Q_4$). The maximum peak-to-peak input voltage without degradation of common-mode rejection is a function of the voltage supplies and the operating mode of the constant-current transistor.

**Harmonic Distortion and Swing Capability.** When equal positive and negative supplies are used, operating mode C provides the largest swing capability because the output operating point is approximately centered. With voltage supplies of ±6 volts dc at a frequency of 1 MHz, the single-ended output is 1.3 volts rms for 3-per-cent distortion in mode C and 0.665 volt rms in mode D.

The signal-swing capability was also evaluated as a function of temperature in mode C with voltage supplies of ±6 volts dc. For 3-per-cent distortion, an output swing of 1.2 volts rms can be obtained over the complete temperature range from 25 to 125°C.

For pulse-type signals, the total possible swing capability is important. The voltage at the collectors of the differential pair may rise to the positive supply voltage, $V_{CC}$, and fall to the saturation level. If the bases of the input emitter-followers are maintained at zero potential, the emitters of the differential pair are negative by twice the base-to-emitter

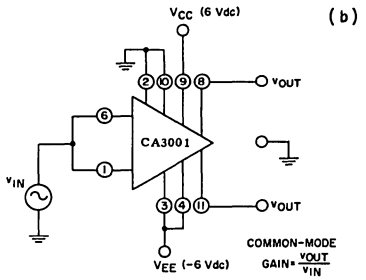
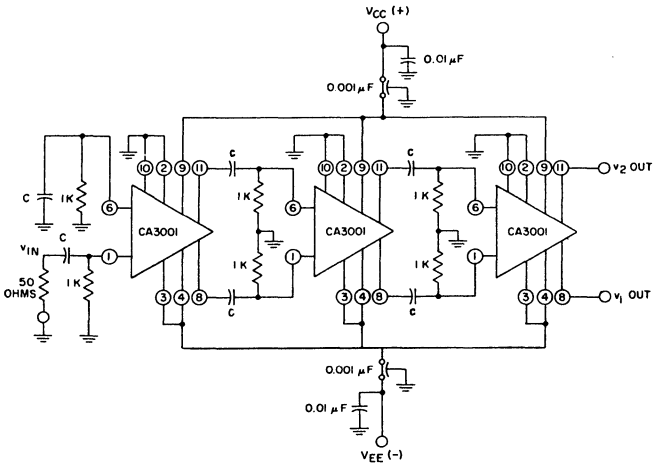


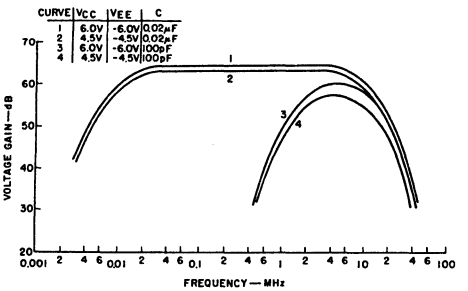

*Fig. 11 - Common-mode rejection and voltage-gain characteristics of the CA3001 as a function of temperature and frequency.*

voltage drop, $V_{BE}$, or approximately −1.4 volts. If the saturation voltage is assumed to be 0.2 volt, the collectors drop to about −1.2 volts before saturation. Therefore, the total swing available at the collectors is approximately $V_{CC}$ + 1.2 volts; for a $V_{CC}$ of 6 volts, the swing is 7.2 volts. The output voltage swing is lower than this value by $V_{BE}$, or from 5.3 to −2.0 volts. This total swing capability can be realized only when the resistors $R_3$ and $R_8$ (terminal 10) are returned to the negative supply voltage (terminal 10 shorted to terminal 3). Selection of the operating point to obtain most of the available total swing in one direction involves proper choice of the operating mode and the negative supply voltage.

## APPLICATIONS

**Cascaded Stages.** Over-all performance characteristics for three CA3001 stages operated in cascade are shown in Fig. 12. The need for supply decoupling is minimized by the symmetry of the circuit, which ensures equal and out-of-phase currents in the supply leads. Three circuits in close proximity can provide stable over-all gains of approximately 65 dB. A further advantage of the CA3001 in cascade is




$$\text{Voltage Gain} = 20 \log \frac{V_{1\,OUT}}{V_{IN}}$$

***Fig. 12 - Three-stage CA3001 cascade amplifier and frequency-response characteristics.***

that a gain increase of 6 dB accrues each time a double-ended output is used.

Table III and Fig. 12 show the performance of the CA3001 in the three-stage cascade circuit for various values of supplies and coupling capacitors. The only advantage of ±6-volt supplies as compared to ±4.5-volt supplies is a larger output-swing capability. The use of ±4.5-volt supplies entails no sacrifice in bandwidth and little gain loss, and provides a saving in power dissipation of almost 2 to 1. Better signal-to-noise performance can be achieved

Table III—Performance of CA3001 Cascade Amplifier shown in Fig. 12

| *Coupling Capacitor* | | *0.02 μF* | | *100 pF* | | |
|---|---|---|---|---|---|---|
| *Voltage Supplies* | | *±6* | *±4.5* | *±6* | *±4.5* | *Vdc* |
| Power Dissipation | | 276 | 146 | 276 | 146 | mW |
| Single-Ended-Output Midband Gain | | 64.5 | 63 | 60.5 | 57.5 | dB |
| 3-dB Response | Upper | 9 | 9 | 10.5 | 10.5 | MHz |
| | Lower | 0.0125 | 0.0125 | 1.9 | 1.9 | MHz |
| AGC Range | | 65 | 63 | 61 | 59 | dB |
| Output Signal for 3-per-cent Distortion | | 1.3 | 1.15 | 1.15 | 0.7 | Vrms |
| Input Signal for 3-dB Signal-to-Noise Ratio | | 26 | 14 | 20 | 18.5 | μVrms |

with no change in bandwidth if a higher value of source resistor is used (e.g., 800 ohms, rather than the value of 50 ohms shown in Fig. 12). The agc range of the cascaded circuits was 10 dB less than that for an individual circuit because no interstage shielding was provided and double-ended output was not used.

**Schmitt Trigger.** The CA3001 has an advantage in Schmitt-trigger applications because the emitter-follower outputs isolate the impedances of the feedback loop from the differential stage. These outputs are also capable of driving low-impedance loads. When symmetrical power supplies of up to ±6 volts are used, the CA3001 operates without saturation of the basic differential pair ($Q_3$ and $Q_5$). For each of the four operating modes, a complete offset at the input that causes all the sink-transistor current to pass through either $Q_3$ or $Q_5$ does not bring these transistors into saturation. As a result, uncertainties resulting in hysteresis prediction caused by storage time are eliminated.

When the CA3001 is connected as a Schmitt trigger, as shown in Fig. 13, the firing points can be changed by adjustment of the resistor $R_2$. This resistor value effectively sets the voltage at the input terminal 6 and requires that the input firing voltage at terminal 1 approach this value to obtain trigger action. The hysteresis voltages obtained for various trigger levels in the circuit of Fig. 13 are shown in Table IV

Table IV—Performance Data for CA3001 Used as a Schmitt Trigger

| *Input Firing Volts* | | | |
|---|---|---|---|
| *Transition from State 1 to State 2* | *Transition from State 2 to State 1* | *Hysteresis Volts* | $R_1$ *Approximate Setting* |
| 3.0 | 1.5 | 1.5 | max. resistance |
| 1.1 | 0.1 | 1.0 | decreasing $R_2$ |
| −1.4 | −1.9 | 0.5 | |
| −3.2 | −3.2 | 0 | |

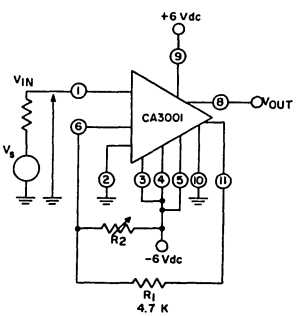



**Fig.13 – CA3001 Schmitt trigger.**

# Application of the RCA CA3015 and CA3016 Integrated-Circuit Operational Amplifiers

BY

T. C. CAMPBELL

The RCA integrated-circuit operational amplifiers CA3015 and CA3016 are identical in circuit configuration to the previously announced types CA3008 and CA3010, but have an improved device breakdown voltage that permits operation from ±12-volt supplies. Operation of the CA3015 and CA3016 from power supplies of ±6 volts or ±3 volts is the same as for the earlier types.[1] This Note describes the operating characteristics of the CA3015 and CA3016 at ±12 volts, and discusses applications that take advantage of the higher gain-bandwidth product and increased output signal swing obtained at the higher voltages.

## OPERATING CHARACTERISTICS

Fig. 1 shows the schematic diagrams and terminal numbers for the CA3015 and CA3016. As in the case of the CA3008 and CA3010, each operational amplifier consists basically of two differential amplifiers and a single-ended output circuit in cascade. The CA3015 is supplied in a 12-lead TO-5 package, and the CA3016 in a 14-lead flat package. Throughout this Note, terminal numbers for the CA3015 are shown in the illustrations; however, the discussion applies to both packages.

### DC Characteristics

When operated from ±12-volt power supplies, these operational amplifiers have a typical dissipation of 175 milliwatts with terminal 5 of the CA3015 or terminal 8 of the CA3016 open. If terminals 5 and 9 of the CA3015 or terminals 8 and 12 of the CA3016 are shorted, higher output-current capability can be achieved, but the dissipation increases to a typical value of 500 milliwatts. The input offset voltage is typically 1.4 millivolts, and the variation in input offset voltage is typically less than 200 microvolts per volt for fluctuations of either supply voltage. At 25°C, the input bias current and input offset current are typically 9.6 and 1 microamperes, respectively. (Curves of input offset voltage, input bias current, and input offset current as functions of temperature are given in the technical bulletin for the CA3015 and CA3016.)

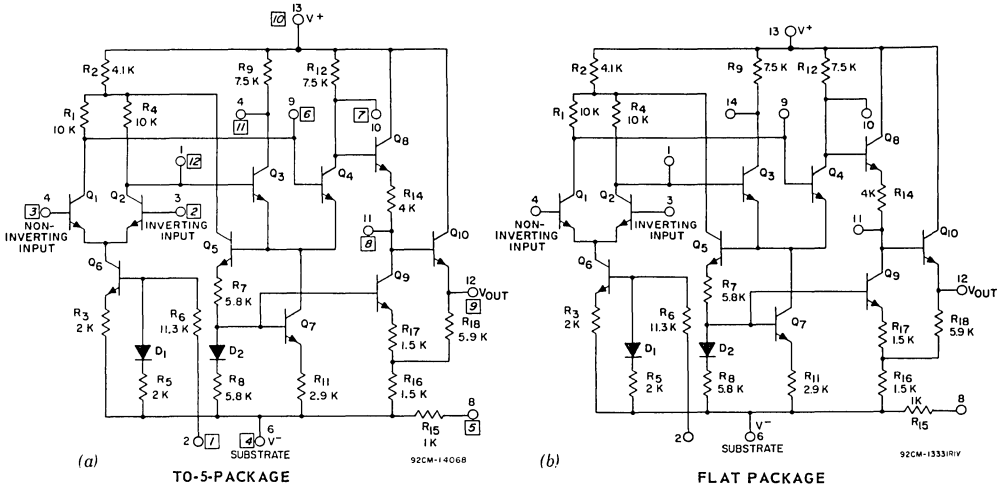



*Fig.1 - Schematic diagrams and terminal connections for the (a) CA3015 and (b) CA3016 integrated-circuit operational amplifiers.*

**Derating.** When these operational amplifiers are operated from ± 12-volt supplies with terminals 5 and 9 of the CA3015 or terminals 8 and 12 of the CA3016 shorted for greater output capability, the power dissipation is high enough so that temperature derating is necessary. The maximum junction-temperature rating is 150°C, and the thermal resistance is 100°C per watt. The maximum power-dissipation rating is 600 milliwatts at 25°C (with terminals shorted as described above). In this higher-output mode, the circuits can operate safely at ambient temperatures up to 90°C.

## AC Characteristics

**Transfer Characteristic.** The open-loop transfer characteristic is shown in Fig.2. As in the case of the CA3008 and CA3010, there is no hysteresis effect. The CA3015 and CA3016 technical bulletin includes curves of maximum peak-to-peak voltages as functions of load resistance with terminal 5 of the CA3015 or terminal 8 of the CA3016 open and with terminals 5 and 9 of the CA3015 or terminals 8 and 12 of the CA3016 shorted. The CA3015 and CA3016 can drive a lower-resistance load when these terminals are shorted.

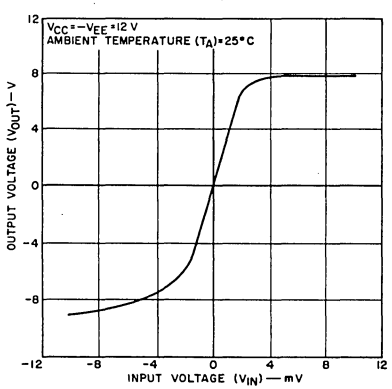



*Fig.2 - Open-loop transfer characteristic.*

**Gain vs Frequency Response.** The open-loop low-frequency gain of the CA3015 and CA3016 with ±12-volt supplies is typically 70 dB with a 3-dB bandwidth of 320 kHz. The unity-gain crossover occurs at a frequency of 58 MHz.

**Common-Mode Rejection.** The common-mode rejection ratio of the CA3015 and CA3016 is typically 104 dB for operation with ±12-volt supplies. A curve of common-mode rejection ratio as a function of frequency is included in the bulletin.

**Input and Output Impedances.** The technical bulletin for the CA3015 and CA3016 includes curves of input and output impedances as functions of temperature. At 25°C, the typical input impedance is 7800 ohms. The typical output impedance is 92 ohms with terminal 5 of the CA3015 or terminal 8 of the CA3016 open, and 76 ohms with these terminals connected to the output.

## PHASE COMPENSATION

The following section describes phase-lag and phase-lead compensation techniques for these operational amplifiers. Fig.3 shows the various phase-compensation connections for the CA3015.

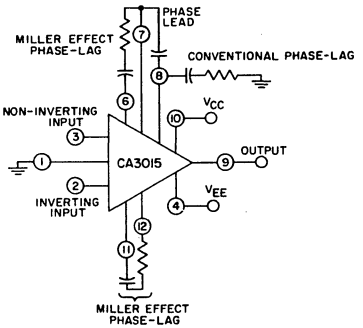



*Fig.3 - Terminal connections for phase-lag and phase-lead compensation of the CA3015.*

### Phase-Lag Compensation

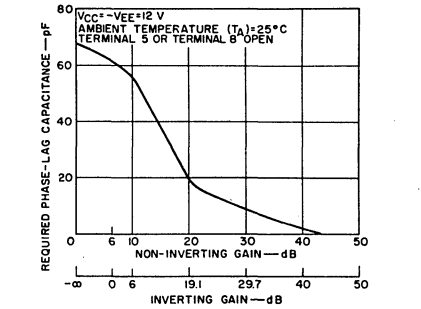
When the CA3015 and CA3016 are operated from ±6-volt supplies, the phase-compensation techniques described previously for the CA3008 and CA3010 are applicable.[1] When the CA3015 and CA3016 are operated from ±12-volt supplies, corrections must be made in the phase-lag compensation to allow for the shift in frequency at which the second break in the open-loop Bode plot occurs. At ±12 volts, this second break occurs at a frequency of 10 MHz. For Miller-effect and conventional phase-lag compensation, the series RC combinations must be adjusted so that $1/(2\pi RC) = 10$ MHz to correct for the shift in frequency. In addition, the Miller technique requires a larger value of phase-lag capacitance for a non-peaking (±1 dB) response to allow for the higher gain.

Fig.4 shows a curve of the required phase-lag capacitance as a function of gain, together with the corresponding response curves. (The required capacitance values shown in this figure are applicable not only for ±12-volt power supplies, but also for all lower-voltage symmetrical supplies; however, smaller capacitors could be used at lower voltages.)

Fig.5 shows curves of open-loop compensated and uncompensated frequency response with ±12-volt supplies. Although the phase-lag compensation capacitance of 18 picofarads shown in curve (B) of this figure is sufficient to provide stability in resistive-feedback amplifiers down to unity gain, it is not sufficient to provide flat closed-loop response (±1 dB) below 20 dB.

### Phase-Lead Compensation

In addition to the standard phase-lag compensation discussed above, the CA3015 and CA3016 have a



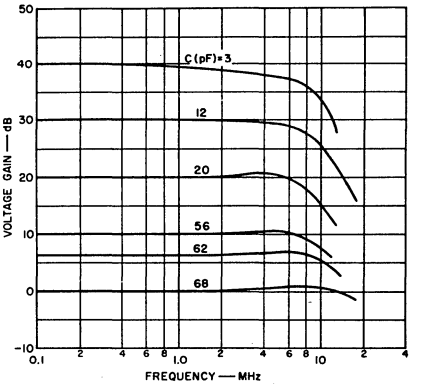




*Fig.4 - Amount of phase-lag capacitance required to obtain a flat (±1 dB) response, and typical response characteristics.*

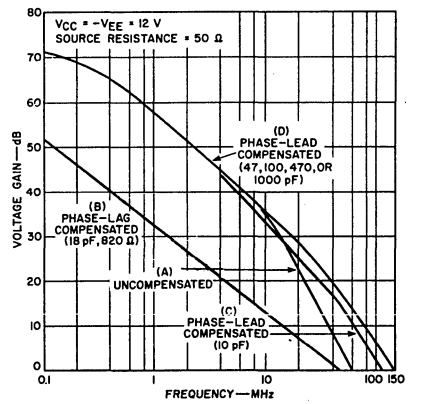



*Fig.5 - Open-loop gain as a function of frequency for compensated and uncompensated amplifiers.*

phase-lead compensation capability. For this phase-lead compensation, a capacitor is connected between terminals 7 and 8 of the CA3015, as shown in Fig.3, or between terminals 10 and 11 of the CA3016. The effect of this capacitor is to eliminate the break at 10 MHz in the Bode plot and thus extend the 6-dB-per-octave roll-off. The second break in the Bode plot then occurs at approximately 35 MHz, and the unity-gain crossover occurs at 150 MHz. The phase-lead compensated open-loop response is shown in curves (C) and (D) of Fig.5 for various values of capacitance. For optimum performance, a minimum phase-lead capacitance of 47 picofarads is recommended.

For flat (±1 dB) responses at closed-loop gains below 30 dB, a small amount of phase-lag compensation is required in addition to the phase-lead compensation. The required phase-lag capacitance for flat (±1 dB) responses and the corresponding response curves are shown in Fig.6. When phase-lead compensation is used, the series RC combinations should be adjusted so that $1/(2\pi RC) = 35$ MHz.

The phase-lead compensation is also applicable when ±6-volt power supplies are used, and provides a unity-gain crossover improvement of about one octave as compared to the uncompensated connection. As mentioned earlier, the phase-lag capacitance requirement for ±12-volt supplies shown in Fig.4 is satisfactory for ±6-volt supplies, although smaller capacitors could be used with the lower voltages.

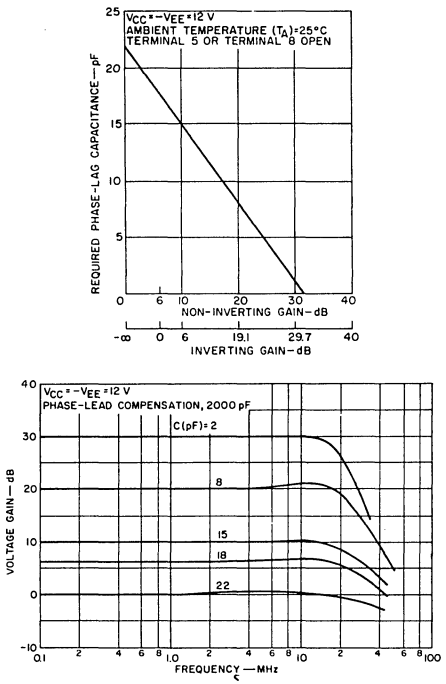



*Fig.6 - Amount of phase-lag capacitance required to obtain a flat (±1 dB) response when phase-lead compensation is used, and typical response characteristics.*

## APPLICATIONS

For all applications, ac and dc balance at the input must be preserved, i.e., the two inputs must be returned to ground through equal impedances.

### 50-dB Amplifier

Fig.7 shows the circuit configuration and frequency response for a non-inverting, 50-dB amplifier employing phase-lead compensation. This amplifier

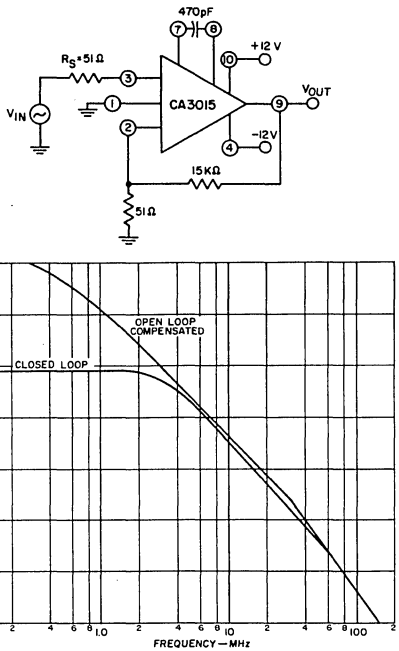
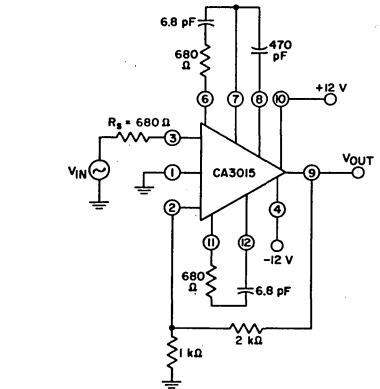



*Fig.7 - Circuit diagram and response curve for a 50-dB, non-inverting amplifier with phase-lead compensation.*

has a 3-dB bandwidth of 3.5 MHz, and a unity-gain crossover at 150 MHz.

### 10-dB, 42-MHz Amplifier

Fig.8 shows the circuit diagram and frequency response for a 10-dB, non-inverting amplifier employing both phase-lead and phase-lag compensation. Slight peaking (2 dB) occurs for the phase compensation shown. Flat response with bandwidth reduction to 25 MHz may be obtained by use of a phase-lag capacitance of 15 picofarads.



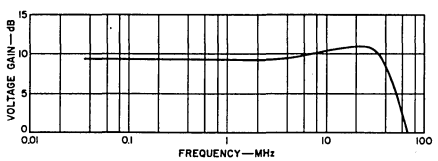
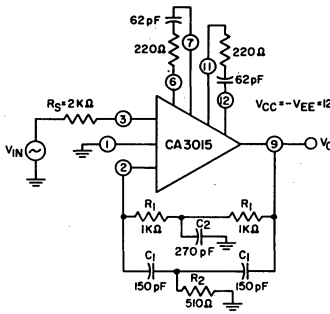




*Fig.8 - Circuit diagram and response curve for a 10-dB, non-inverting amplifier with phase-lead and phase-lag compensation.*

### Twin-T Bandpass Amplifier

Fig.9 shows the circuit diagram and frequency response of a bandpass amplifier using a twin-T network in the feedback loop. The difference in resonant frequency between the bandpass-amplifier response and the twin-T network response is caused by device capacitances and loading effects. The unloaded Q ($Q_0$) of the twin-T network is 14.4; the $Q_0$ of the bandpass amplifier is 12.8.



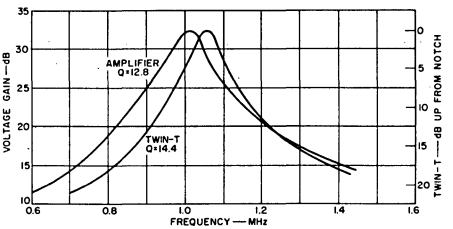




*Fig.9 - Circuit diagram and response curves for a bandpass amplifier using a twin-T network.*

The symmetrical twin-T network can be designed by use of the following equations:

$$R_1 = 2\,R_2$$

$$C_1 = \tfrac{1}{2}\,C_2$$

$$f_0 = 1/(2\pi R_1 C_1)$$

It is important in the design of this type of bandpass amplifier that the two inputs be returned to ground through equal resistances; in this case a value of 2000 ohms is used.

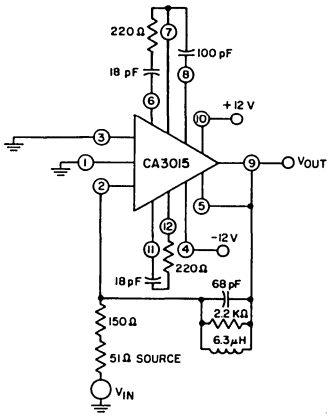
### 20-dB, 10-MHz Bandpass Amplifier

Fig.10 shows the circuit diagram and frequency response of an RLC bandpass amplifier. This amplifier is designed to have a $Q_0$ of about 10 ($R_p = X_C Q_0$ = 2200 ohms) and a gain of about 20 dB at resonance (2200/200 = 11, or 20.9 dB). In this application, the inputs are effectively grounded.

### Voltage Follower

A voltage follower is a non-inverting, unity-gain amplifier used primarily to transform from a high impedance to a low impedance. Because low voltages

are usually associated with high-impedance sources, the voltage follower need not have a great voltage capability.



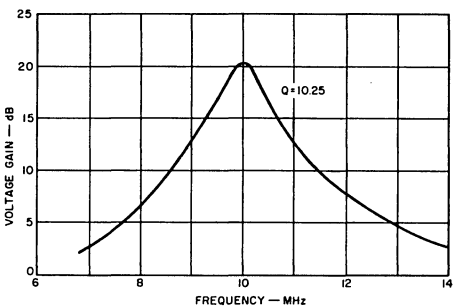




*Fig.10 - Circuit diagram and response curve for a 10-MHz RLC bandpass amplifier.*

Fig.11 shows the circuit diagram for a voltage follower using the CA3015, together with a curve of maximum undistorted output voltage as a function of load resistance. When terminals 5 and 9 are shorted (or terminals 8 and 12 of the CA3016), the voltage follower is capable of transforming a 3.4-volt peak-to-peak voltage from a 100,000-ohm source to a 470-ohm load.

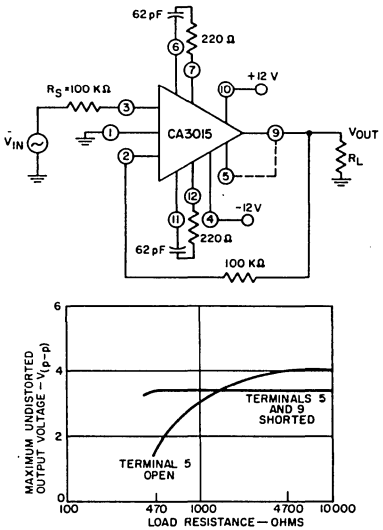



*Fig.11 - Circuit diagram for a voltage follower driven from a 100,000-ohm source, and curve showing maximum undistorted output voltage as a function of load resistance.*

If higher voltage-swing capability is desired, the positive supply voltage ($V_{CC}$) may be increased. Temperature derating may be necessary, depending on the magnitude of $V_{CC}$ and whether the high- or low-current mode is used.

## REFERENCE

1. "Application of the RCA CA3008 and CA3010 Integrated-Circuit Operational Amplifiers", RCA Integrated Circuits Application Note ICAN-5015, November 1965.

# Integrated Circuits For FM Broadcast Receivers

by

R.L. Sanquini

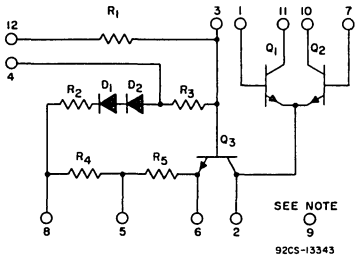
Silicon monolithic integrated circuits have certain design features which make them more attractive than discrete-component circuits for consumer electronic applications. These features include small size, light weight, high reliability, and more potential circuit functions per dollar of cost. Until recently, the major limitation to the extensive use of integrated circuits in commercial FM (88-to-108-MHz) broadcast receivers has been the relatively high cost of such circuits when they were designed to perform the same functions as their discrete-circuit counterparts. This limitation has now been removed by the introduction of high-reliability, low-cost, multifunction integrated circuits such as the RCA CA3005, CA3011, CA3012, CA3013, and CA3014. With these circuits, high-performance inexpensive FM receivers can be designed to meet the rigorous standards set by high-quality commercial FM receivers using vacuum tubes and transistors.

This note describes several approaches to FM receiver design using silicon monolithic integrated circuits. The tuner section is described first, and then the if-amplifier and detector sections. Performance characteristics are described where applicable. The FM receivers discussed are designed for use from a +9-volt supply. The key to design simplicity is the use of the RCA multifunction integrated circuits

CA3005, CA3012, and CA3014. The CA3005 may be used as a cascode rf amplifier, a differential rf amplifier, a mixer-oscillator, and an if amplifier; the CA3012 and CA3014 perform if amplification, limiting, detection, and preamplification.

### FM Tuner

The CA3005 is the basic building block for the three front-end approaches discussed below. A schematic diagram of the CA3005 is shown in Fig. 1. Fig. 2

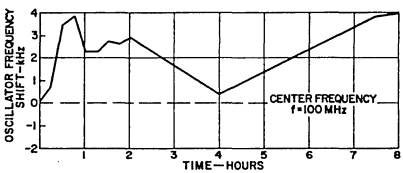


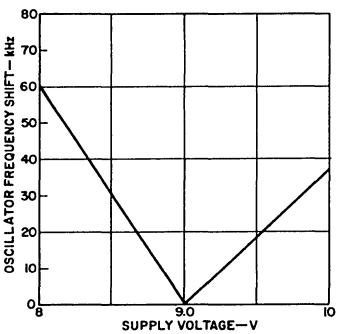

**Note:** Connect terminal 9 to most positive dc supply voltage.

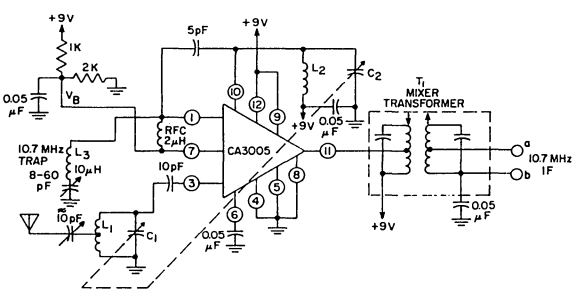
***Fig. 1 - Schematic diagram of RCA CA3005 integrated-circuit rf amplifier.***

shows a single-chip front end that uses one CA3005 and a two-gang capacitor tuning system. The CA3005 performs the functions of rf amplifier, oscillator, and mixer in a unique manner.

The circuit operation may best be explained by reference to Figs. 1 and 2. The first function of the current-sink transistor $Q_3$ in Fig. 1 is to supply the emitter currents for the differential-amplifier transistors $Q_1$ and $Q_2$. Positive feedback from the collector of $Q_2$ (terminal 10) to the base of $Q_1$ (terminal 1) through the 5-picofarad capacitor shown in Fig. 2 establishes the oscillator function; the frequency of oscillation is determined by the tuned circuit $L_2$ and $C_2$. Because the output impedance at the collector of $Q_3$ is high compared to the input impedance at the emitter of $Q_1$ and $Q_2$, $Q_3$ is isolated from $Q_1$ and $Q_2$ and receives very little oscillator signal. The rf input signal




$L_1$ – 4 turns of No. 22 wire, center-tapped; 1/4" O.D. coil form, "E" mat'l slug

$L_2$ – 6 turns No. 32 wire on toroid core; Radio Industries Inc., 1/4" O.D., No. 8 mat'l

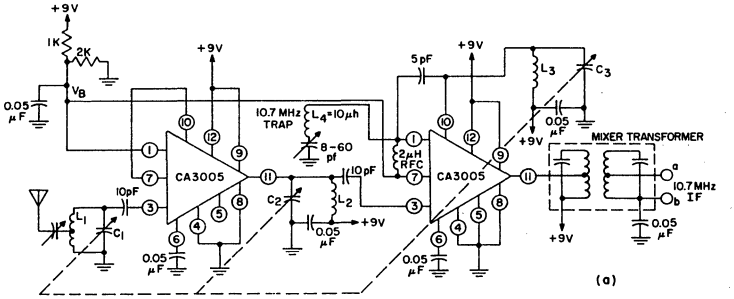
$T_1$ – TRW No. 21629, or equiv.

***Fig. 2 - Single-chip front end using the CA3005. Curves show oscillator stability with time and supply voltage.***

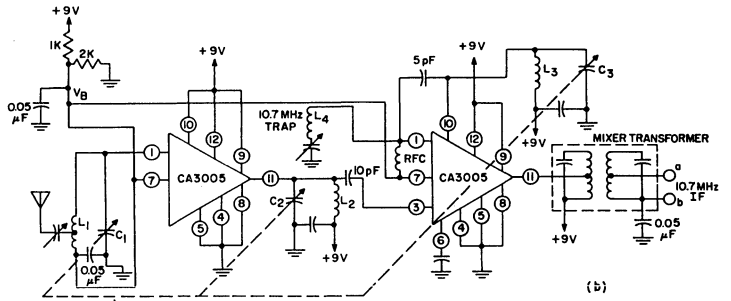
is applied to the base of $Q_3$ (terminal 3), amplified, and injected into the emitter of $Q_1$ and $Q_2$ to mix with the oscillator signal. The 10.7-MHz intermediate frequency is obtained from the collector of $Q_1$ (terminal 11).

The CA3005 draws a total current of 4.5 milliamperes from the +9-volt supply. The front end shown in Fig. 2 has a power gain of 15 dB and a sensitivity of 10 microvolts for 30 dB of quieting; it can handle a maximum input signal of 7 millivolts. Automatic frequency control can be applied to the oscillator in a conventional manner by connection of a voltage-dependent capacitor (diode) to the oscillator tuned circuit $L_2$ and $C_2$. Curves of oscillator stability as a function of time and supply voltage are also shown in Fig. 2.

The approach to the front end shown in Fig. 2, although economical, results in only adequate performance. Improved performance can be obtained by addition of an rf amplifier to the mixer-oscillator circuit, as shown in Fig. 3. In this figure, a CA3005 used as an rf amplifier and a three-gang capacitor tuning system are added to the basic single-chip circuit to provide higher power gain, lower noise figure, and improved selectivity. The CA3005 is connected as a cascode amplifier in Fig. 3(a) and in an emitter-coupled configuration in Fig. 3(b). Both configurations require no neutralization.



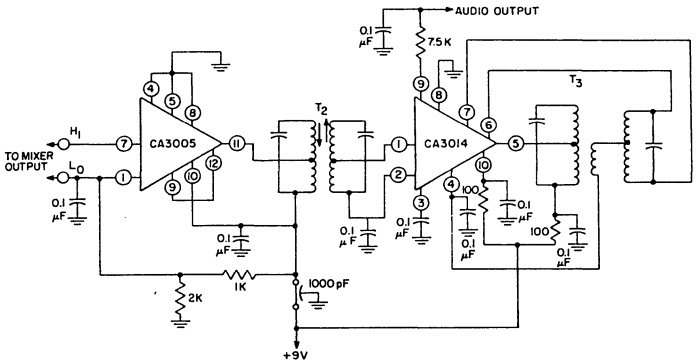

$L_1$ – 4 turns No. 22 wire; center- tapped; 1/4-inch outer-diameter coil form; "E" material slug
$L_2$ – Same as $L_1$ without center tap
$L_3$ – 6 turns No. 32 wire on toroid core; Radio Industries, Inc.; 1/4-inch outer diameter; No. 8 material
Mixer Transformer – TRW No. 21629, or equiv.




$L_1$ – 4 turns of No. 22 wire; center-tapped; 1/4-inch outer-diameter coil form: "E" material slug
$L_2$ – Same as $L_1$ without center tap
$L_3$ – 6 turns of No. 22 wire on toroid core; Radio Industries, Inc.; 1/4-inch outer diameter; No. 8 material
Mixer Transformer – TRW No. 21629, or equiv.

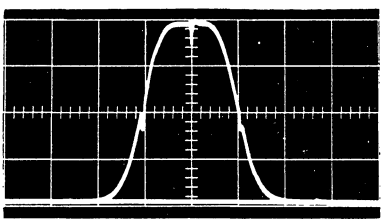
***Fig. 3 - Two-chip front ends using CA3005 rf amplifier connected (a) in cascode, and (b) in emitter-coupled configuration.***

The cascode front end has a higher power gain (28 dB, as compared to 24 dB for the emitter-coupled configuration), but the emitter-coupled front end has better cross-modulation characteristics. The emitter-coupled amplifier can handle interfering signals up to about 15 millivolts with 10 per cent cross-modulation at maximum gain, while the capability of the cascode amplifier is limited to that of a single transistor.[1] The cascode front end has a sensitivity of 2 microvolts for 30 dB of quieting, while the emitter-coupled front end has a sensitivity of 3 microvolts. Reverse agc can be applied to both configurations by variations of the voltage at terminal 12 from 9 volts (maximum gain) to 3 volts (full cutoff) from a 0.5-milliampere agc source. Both amplifiers have a dynamic agc range of 60 dB.

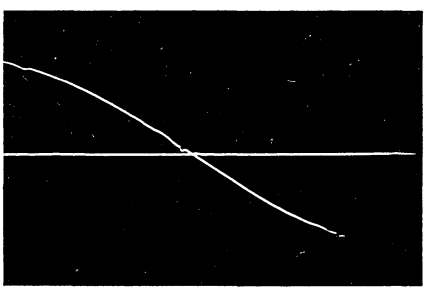



$T_2$ = TRW No. 22468 or equiv.

$T_3$ = TRW No. 21590 or equiv.



10.7-MHz IF SELECTIVITY CURVE
(Markers are 100 kHz apart with center at 10.7 MHz)



DETECTOR "S" CURVE
(Markers are 100 kHz apart with center at 10.7 MHz)

*Fig.4 - Two-chip 10.7-MHz if amplifier, limiter, and discriminator using CA3005, CA3014, and Interstage transformer. Photographs show selectivity curve, detector "S" curve.*

### FM IF Amplifier, Limiter, and Detector

Fig. 4 shows a 10.7-MHz FM if strip and detector that uses a CA3005 and a CA3014 to provide 95 dB of gain. The schematic diagram of the CA3005 was shown in Fig. 1; the CA3014 schematic is shown in Fig. 5. The heart of both these integrated circuits is the differential amplifier, which is probably the best simple configuration on the market today for symmetrical limiting over a wide input-voltage range. The differential-amplifier configuration is also ideal for integration because the parameters that are most important in integrated-circuit design (matched $V_{BE}$, matched beta, and resistor ratios) are the easiest to control on a single silicon chip. In the FM if strip, therefore, three advantages are obtained: high performance, low cost, and fewer individual components.

The input limiting knee for the if strip shown in Fig. 4 is 30 microvolts. The recovered audio obtained from terminal 9 of the CA3014 is 220 millivolts rms. The if selectivity curve and the detector "S" curve are also shown in Fig. 4. The AM rejection referenced to a 30-percent modulated (FM and AM) signal with the AM signal at 30 millivolts is 50 dB.

The 10.7-MHz if-amplifier circuit of Fig. 4 operates as follows: The 10.7-MHz FM signal from the mixer is applied to terminal 7 of the CA3005. The gain from this point to the input of the CA3014 is 25 dB. The interstage transformer $T_2$ is designed so that the collector output of the CA3005 at terminal 1 does not saturate. As a result, bandpass spreading is kept to a minimum over large swings in input voltage. The 10.7-MHz FM signal receives additional gain of 70 dB and limiting from terminal 1 to terminal 5 in the CA3014. The FM output at terminal 5 is applied to the primary winding of the phase-shift (discriminator) transformer $T_3$. The secondary winding, which is connected to terminals 6 and 7, is in quadrature with the primary voltage at the center frequency, 10.7 MHz. As the FM signal varies, the phase shift of the secondary voltage follows the modulation. The detected output at the base of $Q_{11}$ in the CA3014 (terminals 6 and 7) is thus amplified and buffered. The recovered audio is taken from the low-impedance terminal 9.

If more selectivity in the if strip is desired, an additional double-tuned transformer can be added to the circuit.

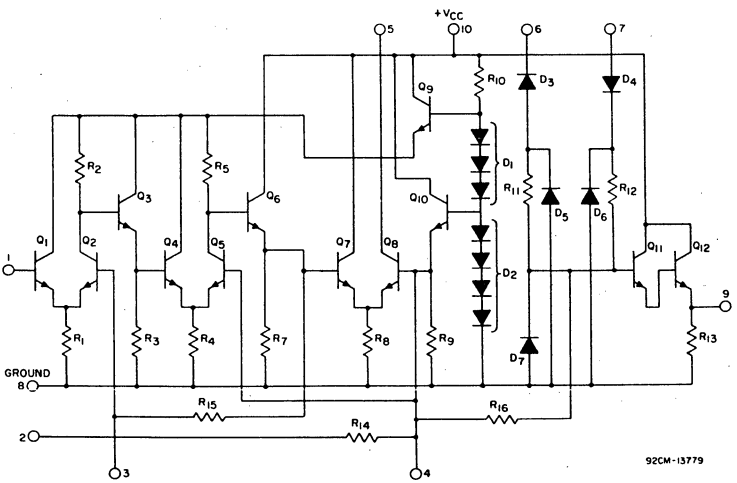
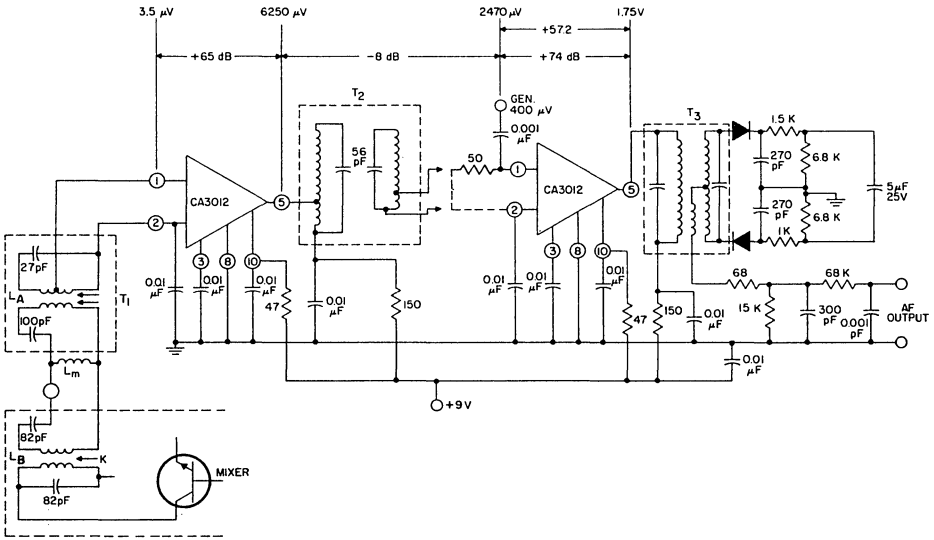



*Fig.5 - Schematic diagram of RCA CA3014 wide-band amplifier-discriminator.*

Fig.6 shows an approach in which the two transformers areplaced immediately after the mixer stage. Fig.7 shows the details of the input filter and Fig.8 shows the schematic of the CA3012 used in the if stages of this circuit. When the transformers (10.7-MHz filter) are placed immediately after the mixer, better adjacent-channel rejection is obtained.

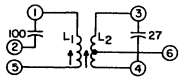
## References

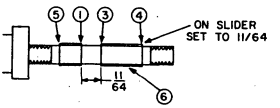

1. "Application of RF Amplifier-Mixer Integrated Circuits CA3004, CA3005, and CA3006," RCA APPLICATION NOTE ICAN-5022, November 1965
2. Mischa Schwartz, INFORMATION TRANSMISSION MODULATION AND NOISE, McGraw-Hill Book Company, 1959
3. J. Avins, "It's a television first. . . .receivers with integrated circuits," ELECTRONICS, March 21, 1966
4. RCA Technical Bulletins: CA3005, CA3011-3012, CA3013-3014
5. R. L. Sanquini, "Multipurpose Chips Cut Costs of FM Receiver," ELECTRONICS, May 16, 1966


$T_1$ - for details see Fig.7
$T_2$ - TRW No.22960-R2 or equiv.
$T_3$ - TRW 23148 or equiv.

*Fig.6 - 10-MHz if amplifier and detector.*




Winding 1-5 - 17 turns #36SE or equiv., $Q_\mu \approx 70$
Winding 3-4 - 40 turns #36SE or equiv., $Q_\mu \approx 75$
Winding 4-6 - 5 turns max; RX-Meter-900 ohms (no load)
Tuning slug: Winding 1-5 - Carbonyl TH or equiv., 1/4" long
Winding 3-4 - Carbonyl TH or equiv., 5/16"long
Front End: $KQ \leq 1$, $Lm = K\sqrt{LA\ LB} = 0.049\ \mu H$

TEST CIRCUIT:

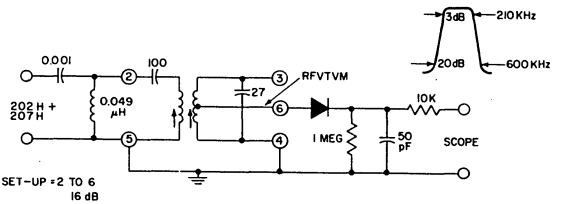
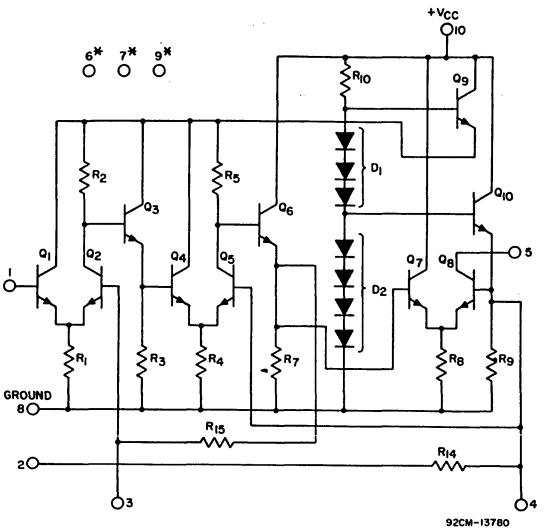



*Fig.7 - Details of 10.7-MHz input filter, $T_1$.*




* Internal Connection - Do Not Use
**Note:** $R_6$ Deleted

*Fig.8 - Schematic diagram of RCA CA3012 wide-band amplifier.*

# Integrated-Circuit Operational Amplifiers

An operational amplifier is basically a very-high-gain direct-coupled amplifier which uses feedback for control of response characteristics. This circuit can be used to synthesize a broad variety of intricate transfer functions and thus can be adapted for use in many widely diverse applications. The operational amplifier is principally used to perform various mathematical functions, such as differentiation, integration, analog comparisons, and summation. This versatile circuit, however, may also be used for numerous other applications that have significantly different transfer and response requirements. For example, the same operational amplifier may be adapted to provide either the broad, flat frequency-gain response required of video amplifiers or the peaked responses required of various types of shaping amplifiers.

## GENERAL CONSIDERATIONS

The configuration most commonly used for operational amplifiers is a cascade of two differential-amplifier circuits together with an appropriate output stage. The cascaded differential-amplifier stages not only fulfill the operational-amplifier requirement for a high-gain direct-coupled amplifier circuit, but also provide significant advantages with respect to application.

From an applications standpoint, an operational amplifier that has a differential input is much more versatile than a single-input type. This increased versatility results from greater flexibility in selection of the feedback configuration. With a single-input operational amplifier, only an inverting feedback configuration can be employed. When differential inputs are used, the feedback configuration may be either an inverting type or a noninverting type, which depends on the common-mode rejection for its negative feedback. The type of feedback affects the characteristics of an operational amplifier, and the two types tend to complement each other. Because the characteristics of each type are required equally often, the differential-input operational amplifier is twice as versatile as the single-input type.

The differential-input operational amplifier is readily adapted to integrated-circuit construction techniques because the stable dc-amplifier configuration lends itself well to the monolithic diffusion process used in the fabrication of silicon integrated circuits. In addition, symmetrical differential-amplifier stages can be dc-cascaded readily, provided that each stage is driven push-pull by the preceding stage. The common-mode effects that result from this arrangement make possible stable, direct-coupled cascaded.

The capabilities and limitations of operational amplifiers are firmly defined by a few very simple equations and rules, which are based on a certain set of criteria that an operational amplifier must meet. Effective use of these simple relationships, however, requires knowledge of the conditions under which each is applicable so that errors that may result from various approximations are held to a minimum. This Note explores the theory of the design and use of operational amplifiers, and develops each pertinent design equation in a general way. Evaluations are then made to determine the assumptions that must be made (or the criteria the operational amplifier must meet) to reduce these general equations to classical operational-amplifier design equations.

Frequency instabilities in the operational amplifier and the methods used to prevent them are also discussed. A thorough understanding of the principles of frequency stability is imperative to the successful application of operational amplifiers. The basic concepts and techniques involved in phase compensation (frequency stabilization) are explained in terms of (1) basic frequency-stability requirements, (2) the problems that may result from an uncontrolled frequency response, and (3) the techniques that may be used to correct these undesirable effects.

Finally, the basic criteria for an operational amplifier are given. This discussion is placed last because a basic insight to the theory of application is required before the effects of many of the operational-amplifier requirements can be fully appreciated.

## BASIC THEORY OF OPERATIONAL AMPLIFIERS

In the development of the basic equations and concepts associated with the use of operational amplifiers, the precise formulations for the transfer functions, the input impedances, the output impedances, and the loop gains are presented for both the inverting and the noninverting feedback configurations, and classical design equations are then derived from these precise formulations. The effects of the load impedance and of common-mode gain (or common-mode rejection) on the inverting and noninverting feedback configurations are considered separately.

### Inverting Feedback Configuration

An operational amplifier operated with an inverting feedback configuration is shown in Fig.1. The load resistor $R_L$ is assumed to be large enough so that its effect on the transfer characteristic is negligible, i.e., $I_{OUT} = 0$. (The effects of a finite $R_L$ are investigated and evaluated subsequently in the discussion of the equivalent-circuit model of an operational amplifier.)

Certain differential-input operational amplifiers require a significant flow of bias current at each input. For this condition, the dc paths to ground for each input must be equal so that a minimum dc offset voltage (error) is developed at the output. Thus, for the terminology employed in Fig.1, $R_r$ must equal the parallel combination of $Z_f(\omega = 0)$ with the series combination of $Z_f(\omega = 0)$ and $Z_{oi}(\omega = 0)$.

In the circuit of Fig.1, the drive-source impedance affects the feedback in the inverting configuration and, therefore, must be considered part of the $Z_r$ term. For

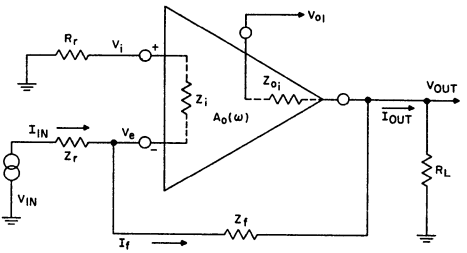



*Fig.1 - Inverting-feedback operational-amplifier configuration.*

brevity, the symbol $Z_r$ is defined to include the source impedance as well as certain feedback design elements. The impedances $Z_i$ and $Z_{oi}$ are the open-loop *intrinsic* input and output impedances of the operational amplifier. Ordinarily, these impedances are assumed in the amplifier symbol. In Fig.1, however, they are identified to emphasize their importance in the ensuing equations. The term $A_o(\omega)$ is the open-loop differential voltage gain of the operational amplifier; this parameter is frequency-dependent. The terminals on the operational-amplifier symbol labled minus (–) and plus (+) refer to the inverting and noninverting input, respectively.

***Inverting-Configuration Transfer Function*** – The transfer function or closed-loop gain of an operational amplifier is generally considered to express the relationship between the input and output voltages. (It is relatively simple to convert the voltage transfer function to another desired transfer relationship.) In the derivation of the transfer function for the schematic in Fig.1, the following differential-amplifier relationship is used as the starting point:

$$V_{o_1} = -A_o(\omega)\,(V_e - V_i) \qquad (1)$$

where $V_e$ and $V_i$ are defined as follows:

$$V_e = \frac{V_{IN}\,(Z_f + Z_{oi}) /\!/ (Z_i + R_r)}{Z_r + (Z_f + Z_{oi}) /\!/ (Z_i + R_r)} + \frac{V_{o_1}\,Z_r /\!/ (Z_i + R_r)}{Z_f + Z_{oi} + Z_r /\!/ (Z_i + R_r)} \qquad (2)$$

and

$$V_i = V_e\,R_r/(Z_i + R_r) \qquad (3)$$

(In these and subsequent equations, the load resistor $R_L$ is assumed to approach infinity.)

If the expressions for $V_e$ and $V_i$ given by Eqs. (2) and (3) are substituted in Eq. (1), the resulting expression can be simplified as follows:

$$V_{o_1} = \frac{-A_o(\omega)\, Z_i\, (Z_f+Z_{o_i})\, V_{IN}}{(Z_f+Z_{o_i})\,(Z_i+R_r)+Z_r\,(Z_f+Z_{o_i}+Z_i+R_r)+A_o(\omega)Z_i\,Z_r} \quad (4)$$

The output voltage $V_{OUT}$ is expressed in terms of $V_{o_1}$ and $V_{IN}$ by the following equation:

$$V_{OUT} = \frac{V_{o_1}\,[Z_f + Z_r /\!/ (Z_i + R_r)]}{Z_{o_i} + Z_f + Z_r /\!/ (Z_i + R_r)} + \frac{V_{IN}\, Z_{o_i}\, (Z_f + Z_{o_i}) /\!/ (Z_i + R_r)}{(Z_f + Z_{o_i})\,[Z_r + (Z_f + Z_{o_i}) /\!/ (Z_i + R_r)]} \quad (5)$$

With $V_{o_1}$ defined as indicated by Eq. (4), the accurate equation for the transfer response (for $R_L \to \infty$) becomes

$$\frac{V_{OUT}}{V_{IN}} = \frac{Z_{o_i}\,(Z_i+R_r) - A_o(\omega)\, Z_i\, Z_f}{(Z_f+Z_{o_i})\,(Z_i+R_r)+Z_r\,(Z_f+Z_{o_i}+Z_i+R_r)+A_o(\omega)Z_iZ_r} \quad (6)$$

If $Z_i$ is assumed to be much greater than the combination of $Z_r$ in parallel with $Z_f + Z_{oi}$, and if $Z_{oi}$ is assumed to be much smaller than $Z_f$, then the closed-loop gain (or transfer function) may be expressed as follows:

$$\frac{V_{OUT}}{V_{IN}} \doteq \frac{-A_o(\omega)\, Z_f}{Z_f + Z_r + A_o(\omega)\, Z_r} \quad (7)$$

In addition, if the open-loop gain $A_o(\omega)$ is the dominant term in either Eq. (6) or (7), the transfer-function equation for the inverting configuration simplifies to the following familiar expression:

$$\frac{V_{OUT}}{V_{IN}} \xrightarrow{A_o(\omega) \to \infty} -\frac{Z_f}{Z_r} \quad (8)$$

Eq. (8) is considered to be the classical or ideal expression for the closed-loop gain (transfer function) for an operational amplifier that uses the inverting type of feedback configuration.

The difference between the open-loop gain and the closed-loop gain is in itself an important design parameter. This "gain throwaway", which is known as the loop gain L.G., is defined by the following equation:

$$\text{L. G.} = \frac{\text{open-loop gain, } A_o(\omega)}{\text{closed-loop gain, } \dfrac{V_{OUT}}{V_{IN}}} \quad (9)$$

When the transfer function is given by Eq. (7), the loop-gain equation may be written as follows:

$$\text{L. G.} = -\frac{Z_f + Z_r}{Z_f} - \frac{A_o(\omega)}{\dfrac{Z_f}{Z_r}} \quad (10)$$

Moreover, when the open-loop gain is very large, the inverting loop gain can be considered to be the open-loop gain divided by the *ideal* inverting closed-loop gain. The equation for L.G. then becomes

$$\text{L. G.} \doteq \frac{-A_o(\omega)}{\dfrac{Z_f}{Z_r}} \quad (11)$$

The loop-gain parameter can be used to predict the accuracy of the approximate operational-amplifier relationships. In general, the higher the loop gain, the more accurate the results provided by the approximate (or classical) relationships. This correlation is demonstrated in Table I, which compares values of $V_{OUT}/V_{IN}$ obtained from the precise transfer expression, Eq. (6),

*Table I – Comparison of Precise and Approximate Formulas for Closed-Loop Gain (Inverting Configuration)*

**Conditions:** $A_o(\omega) = 1000\ \underline{/0°}$, $Z_i = 15{,}000\ \underline{/0°}$, $Z_{o_i} = 200\ \underline{/0°}$, $Z_r = 1000\ \underline{/0°}$.

| $Z_f$ /0° (ohms) | $V_{OUT}/V_{IN}$ (dB) | $V_{OUT}/V_{IN}$ from Eq. (6) (dB) | Error (dB) | L.G. (dB) |
|---|---|---|---|---|
| 200,000 | 46.0 | 44.3 | 1.70 | 14.0 |
| 100,000 | 40.0 | 39.1 | 0.90 | 20.0 |
| 30,000 | 29.6 | 29.3 | 0.30 | 30.4 |
| 10,000 | 20.0 | 19.9 | 0.10 | 40.0 |
| 2,000 | 6.03 | 6.0 | 0.03 | 54.0 |

with values obtained from the classical approximation, Eq.(8), for various gain settings. The tabular data show that the classical equation is accurate to within 1 dB provided the loop gain is at least 20 dB. Eq. (11) was used to calculate all of the loop-gain values given in the table.

***Inverting-Configuration Input Impedance, $Z_{IN}$*** – The input impedance $Z_{IN}$ for the inverting-feedback configuration of an operational amplifier, shown in Fig.1, can be expressed as follows:

$$Z_{IN} = \frac{V_{IN}}{I_{IN}} \quad (12)$$

where

$$I_{IN} = \frac{V_{IN} - V_e}{Z_r} \quad (13)$$

Therefore,

$$Z_{IN} = \frac{Z_r}{1 - \dfrac{V_e}{V_{IN}}} \quad (14)$$

The ratio $V_e/V_{IN}$ may be determined by substituting the expression for $V_{o_1}$ given by Eq. (4) into Eq. (2) and dividing through by $V_{IN}$ (with $R_L \rightarrow \infty$.) The resultant equation is then simplified to obtain the following relationship:

$$\frac{V_e}{V_{IN}} = \frac{(Z_f+Z_{o_i})\,(Z_i+R_r)}{Z_r\,(Z_f+Z_{o_i}+Z_i+R_r)+(Z_f+Z_{o_i})\,(Z_i+R_r)+A_o(\omega)Z_i\,Z_r} \quad (15)$$

If this expression for $V_e/V_{IN}$ is substituted into Eq.(14), the result can be simplified to obtain the following precise expression for the closed-loop input impedance:

$$Z_{IN} = Z_r + \frac{Z_r\,(Z_{o_i}\,Z_i + Z_{o_i}R_r + Z_fR_r + Z_f\,Z_i)}{Z_r\,(Z_f+Z_{o_i}+Z_i)+R_r\,(Z_r+Z_{o_i})+A_o(\omega)Z_i\,Z_r} \quad (16)$$

If $A_o(\omega)$ is dominant and $Z_{o_i}$ is small, Eq. (16) reduces to

$$Z_{IN} \doteq Z_r + \frac{Z_f\,(Z_i+R_r)}{A_o(\omega)\,Z_i} \quad (17)$$

A further simplification is possible when $R_r$ is much smaller than $Z_i$, which is a common condition. In this case, the equation for the input impedance becomes

$$Z_{IN} \doteq Z_r + \frac{Z_f}{A_o(\omega)} \quad (18)$$

Eqs. (17) and (18), which are important in voltage-summing or scaling-adder* applications, can be used to predict the degree of interaction among multiple inputs.

When $A_o(\omega)$ is large enough, Eqs. (17) and (18) may be rewritten as follows:

$$Z_{IN} \xrightarrow{A_o(\omega)\rightarrow\infty} Z_r \quad (19)$$

Eq. (19) is the "classical" equation for the input impedance of an operational amplifier when an inverting-feedback configuration is used. This equation, together with Eq. (16), implies the existence of a condition known as a virtual ground at the node-assigned voltage $V_e$ (shown in Fig.1). That is, the node is at ground potential even though there is no electrical connection between this point and ground. [This statement can be verified either intuitively by the use of Eq. (19) or directly if $A_o(\omega)$ is assumed to be infinite in Eq.(15).] Moreover, no current flows into the negative terminal of the amplifier when the open-loop gain is infinite because the voltage $V_e$ is zero while the impedance at the negative terminal (i.e., $Z_i + R_r$) is not zero. The concept of a virtual ground leads to an extremely simple three-step analysis procedure for an inverting operational-amplifier configuration.

1. Because of the virtual ground ($V_e = 0$), the input current $I_{IN}$ and feedback current $I_f$ can be defined as follows:

$$I_{IN} = \frac{V_{IN}}{Z_r} \quad (20)$$

$$I_f = \frac{-V_{OUT}}{Z_f} \quad (21)$$

2. Zero current flow into the inverting terminal ($V_e = 0$) indicates the following relationships:

$$I_{IN} = I_f \quad (22)$$

$$\frac{V_{IN}}{Z_r} = \frac{-V_{OUT}}{Z_f} \quad (23)$$

3. Eq. (23) can then be rewritten to obtain the classical gain equation, as follows:

$$\frac{V_{OUT}}{V_{IN}} = -\frac{Z_f}{Z_r} \quad (24)$$

Although the foregoing analysis is certainly an idealized one, it is nevertheless practical because the required approximations are usually valid. Eq. (15) serves as a measure of the deviation from a true virtual ground.

***Inverting-Configuration Output Impedance, $Z_{OUT}$ –*** The closed-loop output impedance is the ratio of the unloaded output voltage $V_{OUT}$ to the short-circuit output current $I_{OUT}$ as follows:

$$Z_{OUT} = \frac{V_{OUT}\,(R_L \rightarrow \infty)}{I_{OUT}\,(R_L \rightarrow 0)} \quad (25)$$

It is apparent from Fig.1 then that the output current $I_{OUT}$ is given by

$$I_{OUT}\,(R_L \rightarrow 0) = \frac{-A_o(\omega)\,(V_e - V_i)}{Z_{o_i}} \quad (26)$$

If the expression given by Eq. (3) is substituted for $V_i$, Eq. (26) can be rewritten as follows:

$$I_{OUT}\,(R_L \rightarrow 0) = \frac{-A_o(\omega)\,Z_i\,V_e}{Z_{o_i}\,(Z_i+R_r)} \quad (27)$$

Under short-circuit conditions ($R_L = 0$), the voltage $V_e$ in terms of $V_{IN}$ is given by

$$V_e = \frac{V_{IN}\,Z_f /\!\!/ (Z_i+R_r)}{Z_r + Z_f /\!\!/ (Z_i+R_r)} = \frac{V_{IN}\,Z_f\,(Z_i+R_r)}{Z_r\,(Z_f+Z_i+R_r)+Z_f\,(Z_i+R_r)} \quad (28)$$

*A scaling adder is an inverting operational-amplifier configuration which weights and sums multiple voltages.

Therefore, $I_{OUT}$ (at $R_L = 0$) can be expressed in terms of $V_{IN}$ as follows:

$$I_{OUT} = \frac{-A_o(\omega)\, Z_i\, Z_f\, V_{IN}}{Z_{o_i}\,[Z_r\,(Z_f+Z_i+R_r) + Z_f\,(Z_i+R_r)]} \quad (29)$$

If this expression for $I_{OUT}$ is substituted in Eq. (25) and consideration is given to the intransience of $V_{IN}$ in going from an unloaded to a fully loaded condition, the equation for $Z_{OUT}$ becomes

$$Z_{OUT} = \frac{Z_{o_i}\,[Z_r\,(Z_f+Z_i+R_r) + Z_f\,(Z_i+R_r)]}{-A_o\,(\omega)\, Z_i\, Z_f} \left(\frac{V_{OUT}}{V_{IN}}\right) \quad (30)$$

Finally, the desired equation for the closed-loop output impedance is obtained if the expression for $V_{OUT}/V_{IN}$ given by Eq. (6) is substituted into Eq. (30), as follows:

$$Z_{OUT} = \frac{Z_{o_i}[Z_r(Z_f+Z_i+R_r)+Z_f(Z_i+R_r)]\,[A_o(\omega)Z_iZ_f - Z_{o_i}(Z_i+R_r)]}{A_o(\omega)Z_iZ_f[Z_r(Z_f+Z_{o_i}+Z_i+R_r)+(Z_f+Z_{o_i})(Z_i+R_r)+A_o(\omega)Z_iZ_r]} \quad (31)$$

If the open-loop gain term $A_o(\omega)$ is dominant, Eq. (31) simplifies to

$$Z_{OUT} \doteq \frac{Z_{o_i}\,[Z_r\,(Z_f + Z_i + R_r) + Z_f\,(Z_i + R_r)]}{A_o(\omega)\, Z_i\, Z_r} \quad (32)$$

This expression for $Z_{OUT}$ does not simplify to its "classical" equation unless $Z_i$ is dominant also; in this case, Eq. (32) becomes

$$Z_{OUT} \doteq Z_{o_i}\,\frac{1 + \frac{Z_f}{Z_r}}{A_o(\omega)} \quad (33)$$

The assumption that $Z_i$ is a dominant term is not always valid, especially if bipolar transistor inputs are employed. Eq. (32), therefore, may be considered to take precedence over Eq. (33).

### Noninverting Feedback Configuration

Fig.2 shows the general circuit for an operational amplifier operated with a noninverting feedback configuration. In this section, the equations for the transfer function and the closed-loop input impedance for this type of operational-amplifier circuit are derived. These derivations, as did those for the inverting circuit, assume that the load resistor $R_L$ is large enough so that its effect is negligible, i.e., $R_L \to \infty$ and $I_{OUT} = 0$. (The effects of a finite load resistance on the noninverting operational amplifier are evaluated in the discussion of the equivalent-circuit model of an operational amplifier.)

A noninverting operational amplifier, unlike the inverting type, requires a differential-input arrangement because it uses the common-mode effect in its feedback

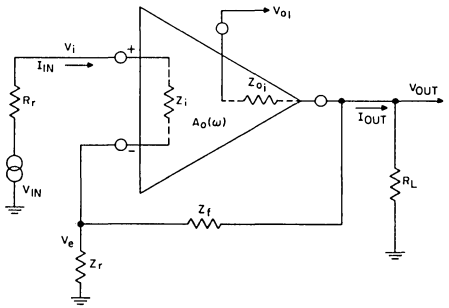



*Fig.2 - Noninverting-feedback operational-amplifier configuration.*

scheme. The following basic requirements and definitions that apply to the inverting circuit shown in Fig.1 are also valid for the general noninverting circuit of Fig.2:

1. The dc return paths to ground for the two inputs must be equal and finite for amplifiers that require a significant amount of input bias current.
2. The input and output impedances, $Z_i$ and $Z_{o_i}$, are inherent in the basic amplifier unit and are shown on the diagram to emphasize their importance in the relationships to be derived.
3. The open-loop gain is frequency-dependent and is represented by the symbol $A_o(\omega)$.
4. The plus and minus labels on the input terminals designate the noninverting and inverting terminals, respectively.

In the noninverting circuit, however, the source impedance is included in the passive element $R_r$ rather than the frequency-dependent parameter $Z_r$, as in the inverting circuit.

***Noninverting-Configuration Transfer Function*** – As with the inverting circuit, the transfer function developed for the noninverting operational amplifier shows the relationship between the input and output voltages. It is relatively simple to convert this relationship to another type of transfer function.

When the load resistor $R_L$ approaches infinity, the

output voltage $V_{OUT}$ for the general circuit shown in Fig.2 can be expressed as follows:

$$V_{OUT} = \frac{V_{o1}\,[Z_f + Z_r /\!/ (Z_i + R_r)]}{Z_{o_i} + Z_f + Z_r /\!/ (Z_i + R_r)} + \frac{V_{IN}\,Z_{o_i}\,[Z_r /\!/ (Z_f + Z_{o_i})]}{(Z_f + Z_{o_i})\,[Z_i + R_r + Z_r /\!/ (Z_f + Z_{o_i})]} \quad (34)$$

Eq. (34) may be rewritten in the following form:

$$V_{OUT} = \frac{V_{o1}\,[Z_f\,(Z_r + Z_i + R_r) + Z_r\,(Z_i + R_r)] + Z_r\,Z_{o_i}\,V_{IN}}{(Z_i + R_r)\,(Z_r + Z_f + Z_{o_i}) + Z_r\,(Z_f + Z_{o_i})} \quad (35)$$

The voltage $V_{o1}$ is defined by the differential-gain expression, as follows:

$$V_{o1} = A_o(\omega)\,(V_i - V_e) \quad (36)$$

where $V_i$ is the source voltage $V_{IN}$ less the voltage drop across $R_r$, as given by

$$V_i = V_{IN} - I_{IN}\,R_r \quad (37)$$

where

$$I_{IN} = \frac{V_i - V_e}{Z_i} \quad (38)$$

The voltage $V_i$, given by Eq. (37), can now be expressed in terms of the voltages $V_{IN}$ and $V_e$, as follows:

$$V_i = \frac{Z_i\,V_{IN} + R_r\,V_e}{Z_i + R_r} \quad (39)$$

It can be determined from Fig.2 that, when $R_L$ approaches infinity, the voltage $V_e$ is given by the following equation:

$$V_e = \frac{V_{o1}\,Z_r /\!/ (Z_i + R_r)}{Z_{o_i} + Z_f + Z_r /\!/ (Z_i + R_r)} + \frac{V_{IN}\,Z_r /\!/ (Z_f + Z_{o_i})}{Z_i + R_r + Z_r /\!/ (Z_f + Z_{o_i})} \quad (40)$$

If the relationships for $V_{o1}$ and $V_i$ given by Eqs. (36) and (39), respectively, are used, $V_e$ can be expressed solely in terms of $V_{IN}$, as shown by the following equation:

$$V_e = \frac{(Z_r\,Z_f + Z_r\,Z_{o_i} + A_o(\omega)\,Z_i\,Z_r)\,V_{IN}}{(Z_i + R_r)\,(Z_r + Z_f + Z_{o_i}) + Z_r\,(Z_f + Z_{o_i}) + A_o(\omega)\,Z_i\,Z_r} \quad (41)$$

Eqs. (36), (39), and (41) are now used to express $V_{o1}$ in terms of $V_{IN}$, as follows:

$$V_{o1} = \frac{A_o(\omega)\,Z_i\,(Z_r + Z_f + Z_{o_i})\,V_{IN}}{(Z_i + R_r)\,(Z_r + Z_f + Z_{o_i}) + Z_r\,(Z_f + Z_{o_i}) + A_o(\omega)\,Z_i\,Z_r} \quad (42)$$

If this expression for $V_{o1}$ is substituted into Eq. (35), the new equation that results can be simplified and divided through by $V_{IN}$ to obtain the desired transfer function, as follows:

$$\frac{V_{OUT}}{V_{IN}} = \frac{Z_r\,Z_{o_i} + A_o(\omega)\,Z_i\,(Z_r + Z_f)}{(Z_i + R_r)\,(Z_r + Z_f + Z_{o_i}) + Z_r\,(Z_f + Z_{o_i}) + A_o(\omega)\,Z_i\,Z_r} \quad (43)$$

The transfer function that is usually associated with the noninverting feedback configuration of an operational amplifier can be derived from Eq. (43) if the impedance $Z_{o_i}$ is assumed to be zero and the impedance $Z_i$ is assumed to be very high. When these assumptions are made, Eq. (43) becomes

$$\frac{V_{OUT}}{V_{IN}} \doteq \frac{(Z_r + Z_f)\,A_o(\omega)}{(Z_r + Z_f) + Z_r\,A_o(\omega)} \quad (44)$$

Eq. (44) may be rewritten as follows:

$$\frac{V_{OUT}}{V_{IN}} \doteq \frac{A_o(\omega)}{1 + \dfrac{A_o(\omega)}{1 + Z_f/Z_r}} \quad (45)$$

If the term $A_o(\omega)$ is dominant in Eq. (45), the following "classical" expression for the noninverting transfer response results:

$$\frac{V_{OUT}}{V_{IN}} \xrightarrow{A_o(\omega) \to \infty} 1 + \frac{Z_f}{Z_r} \quad (46)$$

The term $1 + Z_f/Z_r$ represents the closed-loop gain for the *ideal* noninverting configuration. This term, which is referred to as the *ideal feedback characteristic,* is basic to operational-amplifier frequency-stabilization theory.

As might be expected, the loop gain of an operational amplifier is defined in the same way [by Eq. (9)] regardless of the type of feedback configuration. Under the conditions for which Eq. (45) is a valid expression for the transfer response, the loop gain for the noninverting configuration is given by

$$\text{L. G.} = 1 + \frac{A_o(\omega)}{1 + \dfrac{Z_f}{Z_r}} \quad (47)$$

If the second term of Eq. (47) is very large, this equation reduces to

$$\text{L. G.} \doteq \frac{A_o(\omega)}{1 + \frac{Z_f}{Z_r}} \tag{48}$$

Table II compares the values calculated from the precise and the approximate expressions [Eqs. (43) and (46), respectively] for the closed-loop gain of the noninverting operational-amplifier configuration. The approximate formula is accurate to within 1 dB provided

*Table II – Comparison of Precise and Approximate Formulas for Closed-Loop Gain (Noninverting Configuration)*

**Conditions:** $A_o(\omega) = 1000 \angle 0°$, $Z_i = 15{,}000 \angle 0°$, $Z_{o_i} = 200 \angle 0°$, $Z_r = 1000 \angle 0°$

| $Z_f \angle 0°$ (ohms) | $V_{OUT}/V_{IN}$ from Eq. (46) (dB) | $V_{OUT}/V_{IN}$ from Eq. (43) (dB) | Error (dB) | L. G. from Eq. (48) (dB) |
|---|---|---|---|---|
| 199,000 | 46.0 | 44.3 | 1.70 | 14.0 |
| 99,000 | 40.0 | 39.1 | 0.90 | 20.0 |
| 29,000 | 29.6 | 29.3 | 0.30 | 30.4 |
| 9,000 | 20.0 | 19.9 | 0.10 | 40.0 |
| 1,000 | 6.03 | 6.0 | 0.03 | 54.0 |

the loop gain is 20 dB or more. A comparison of Tables I and II shows that the error introduced by the use of the classical gain formula for the noninverting configuration [Eq. (46)] is identical to that introduced by the use of the classical gain formula for the inverting configuration [Eq. (8)].

***Noninverting-Configuration Input Impedance, $Z_{IN}$ –*** The following equation gives the basic definition of the input impedance $Z_{IN}$:

$$Z_{IN} = \frac{V_{IN}}{I_{IN}} \tag{49}$$

It can be readily determined from Fig.2 that the input current $I_{IN}$ is given by

$$I_{IN} = \frac{V_{IN} - V_e}{Z_i + R_r} \tag{50}$$

When this relationship is applied in Eq. (49), the expression for the noninverting input impedance becomes

$$Z_{IN} = \frac{Z_i + R_r}{1 - \frac{V_e}{V_{IN}}} \tag{51}$$

If the expression for the ratio of $V_e/V_{IN}$, given previously by Eq. (41), is substituted into Eq. (51), the result can be simplified to obtain the following precise expression for the input impedance (for $R_L \to \infty$):

$$Z_{IN} = Z_i + R_r + Z_r \frac{Z_f + Z_{o_i} + A_o(\omega)\, Z_i}{Z_r + Z_f + Z_{o_i}} \tag{52}$$

For the case where $Z_i$ is dominant and $Z_{oi}$ is small, Eq. (52) reduces to

$$Z_{IN} \doteq Z_i + \frac{A_o(\omega)\, Z_i}{1 + \frac{Z_f}{Z_r}} \tag{53}$$

The following expression for the input impedance results if $A_o(\omega)$ is also considered dominant:

$$Z_{IN} \doteq \frac{A_o(\omega)\, Z_i}{1 + \frac{Z_f}{Z_r}} \tag{54}$$

Eq. (54) states that the noninverting input impedance is equal to the intrinsic input impedance $Z_i$ multiplied by the loop gain.

***Noninverting-Configuration Output Impedance, $Z_{OUT}$-*** As in the inverting configuration, the closed-loop output impedance for the noninverting configuration is defined as the ratio of the open-circuit output voltage, $V_{OUT}$, to the short-circuit output current, $I_{OUT}$, as follows:

$$Z_{OUT} = \frac{V_{OUT}\,(R_L \to \infty)}{I_{OUT}\,(R_L \to 0)} \tag{55}$$

where

$$I_{OUT}\,(R_L \to 0) = \frac{A_o(\omega)\,(V_i - V_e)}{Z_{o_i}} \tag{56}$$

For the general noninverting operational-amplifier configuration, the voltages $V_i$ and $V_e$ are given by the following equations for the conditions indicated:

$$V_i\,(R_L \to 0) = \frac{V_{IN}\,(Z_i + Z_r /\!\!/ Z_f)}{R_r + Z_i + Z_r /\!\!/ Z_f} \tag{57}$$

and

$$V_e\,(R_L \to 0) = \frac{V_{IN}\, Z_r /\!\!/ Z_f}{R_r + Z_i + Z_r /\!\!/ Z_f} \tag{58}$$

On the basis of the relationships expressed by Eqs. (57) and (58), Eq. (56) may be rewritten as follows:

$$I_{OUT}\,(R_L \to 0) = \frac{A_o(\omega)\, V_{IN}\, Z_i\,(Z_r + Z_f)}{Z_{o_i}\,[(Z_r + Z_f)(R_r + Z_i) + Z_r Z_f]} \tag{59}$$

The output impedance $Z_{OUT}$ then becomes

$$Z_{OUT} = Z_{o_i}\left[\frac{Z_r Z_f + (Z_r + Z_f)(R_r + Z_i)}{A_o(\omega)\, Z_i\,(Z_r + Z_f)}\right]\left(\frac{V_{OUT}}{V_{IN}}\right) \tag{60}$$

Finally, the following precise equation for the output impedance $Z_{OUT}$ is obtained when the ratio for $V_{OUT}/V_{IN}$ is replaced by its impedance equivalent, as given by Eq. (43):

$$Z_{OUT} = \frac{Z_{oi}[(Z_r+Z_f)(R_r+Z_i) + Z_rZ_f]}{A_o(\omega)\, Z_i(Z_r + Z_f)} \times \frac{Z_r\, Z_{oi} + A_o(\omega)Z_i\,(Z_r+Z_f)}{(Z_i+R_r)(Z_r+Z_f+Z_{oi})+Z_r\,(Z_f+Z_{oi})+A_o(\omega)\, Z_i\, Z_r} \quad (61)$$

If $A_o(\omega)$ is dominant, then Eq. (61) becomes

$$Z_{OUT} \doteq Z_{oi}\left[\frac{Z_r\, Z_f + (Z_r + Z_f)\,(R_r + Z_i)}{A_o(\omega)\, Z_i\, Z_r}\right] \quad (62)$$

The expression for the closed-loop output impedance does not revert to its classical form unless both the intrinsic input impedance $Z_i$ and the open-loop gain $A_O(\omega)$ are very large. Under such conditions, the equation for the output impedance reduces to

$$Z_{OUT} \doteq Z_{oi}\frac{1+\frac{Z_f}{Z_r}}{A_o(\omega)} \quad (63)$$

This classical expression indicates that the output impedance of the noninverting configuration is equal to the intrinsic output impedance $Z_{oi}$ divided by the loop gain. It should be noted that the classical expressions for the closed-loop output impedances for the inverting and noninverting configurations [Eq. (33) and (63), respectively] are identical.

### Equivalent-Circuit Model of a Closed-Loop Operational Amplifier

Fig.3 shows the equivalent circuit of a closed-loop operational amplifier. This equivalent circuit is valid for either the inverting or the noninverting configuration. In the inverting configuration, $Z_r$ is used to represent

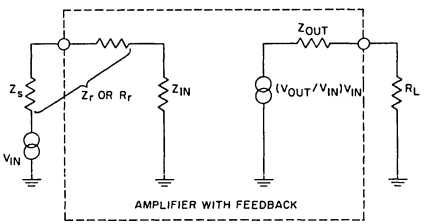



*Fig.3 - Equivalent-circuit model of a closed-loop operational amplifier.*

the impedance in series with the closed-loop input impedance $Z_{IN}$. In the noninverting configuration, term $Z_r$ is replaced by $R_r$ to show that the components thus represented are independent of frequency. The closed-loop input and output impedances ($Z_{IN}$ and $Z_{OUT}$, respectively) and the transfer function $V_{OUT}/V_{IN}$ were defined previously.

***Effect of a Finite Load Impedance on Operational-Amplifier Characteristics*** — One of the important features of the equivalent-circuit model is that it accurately accounts for the effects of a finite load impedance, $R_L$. For example, if a 2000-ohm load impedance is used on the 46-dB (approximate) inverting amplifier for which data are given in Table I, the equation for the transfer response must be modified as follows:

$$V_{OUT} = \frac{\left(\frac{V_{OUT}}{V_{IN}}\right) V_{IN}\, R_L}{R_L + Z_{OUT}} \quad (64)$$

If Eq. (6) is used to determine the value of $V_{OUT}/V_{IN}$ and Eq. (30) is used to determine the value of $Z_{OUT}$, the transfer-function ratio for an $R_L$ of 2000 ohms can be calculated from Eq. (64) as follows:

$$\frac{V_{OUT}}{V_{IN}} = 164\left(\frac{2000\text{ ohms}}{37.4\text{ ohms} + 2000\text{ ohms}}\right) = 162 \quad (65)$$

Thus, a ratio of 44.15 dB is obtained, as compared to 44.3 dB for an open-circuit load. Similarly, if a 2000-ohm load is used for the 6-dB amplifier, the gain becomes 5.98 dB, as compared to 6 dB indicated in Table I for an open-circuit load. The error in neglecting a 2000-ohm load, therefore, is 0.15 dB for the 46-dB amplifier and only 0.02 dB for the 6-dB amplifier (for the conditions given in Table I).

***Effect of the Common Mode Gain (CMG) on Operational-Amplifier Characteristics*** — In the developments of the basic equations for the inverting and noninverting feedback configurations of the operational amplifier, it was tacitly assumed that the common-mode gain was essentially zero (infinite attenuation). The common-mode gain is defined as the ratio of the output voltage, $V_{OUT}$, to the input voltages, $V_i$ and $V_e$, when $V_i$ and $V_e$ are identical in amplitude and phase. The validity of this assumption is considered separately in this section because the basic feedback equations become burdensome when common-mode effects are included. As a result, the salient features of these equations become obscured.

An examination of Figs. 1 and 2 shows that, in either the inverting or noninverting configuration, the differential gain acts on the difference between the voltages $V_i$ and $V_e$. On the other hand, the common-mode gain acts on those portions of $V_i$ and $V_e$ that are in phase and identical in magnitude. That is, the com-

mon-mode gain acts on the smaller of the two in-phase signals ($V_i$ or $V_e$). In the inverting configuration $V_i$ is less than $V_e$, but in the noninverting configuration $V_i$ is greater than $V_e$. These conditions are reflected by the output-voltage equations when the effects of the common-mode gain (CMG) are considered, as follows:

1. For the inverting configuration,

$$V_{o_1} = A_o(\omega)(V_i - V_e) - (CMG)(V_i) \quad (66)$$

2. For the noninverting configuration,

$$V_{o_1} = A_o(\omega)(V_i - V_e) - (CMG)(V_e) \quad (67)$$

If these two equations are developed further, the following gain expressions are obtained for $Z_{o_i} = 0$ (i.e., $V_{o_i} = V_{OUT}$):

1. For the inverting configuration,

$$\frac{V_{OUT}}{V_{IN}} = \frac{-A_o(\omega)\,Z_i\,Z_f - (CMG)\,R_r\,Z_f}{Z_r(Z_f+Z_i+R_r)+Z_f(Z_i+R_r)+Z_i\,Z_r\,A_o(\omega)+R_r\,Z_r\,(CMG)} \quad (68)$$

2. For the noninverting configuration,

$$\frac{V_{OUT}}{V_{IN}} = \frac{A_o(\omega)\,Z_i\,(Z_r+Z_f) - (CMG)\,Z_r\,Z_f}{(Z_r+Z_f)(R_r+Z_i)+Z_r\,Z_f+A_o(\omega)\,Z_i\,Z_r+(CMG)\,Z_r\,(Z_i+R_r)} \quad (69)$$

In each case, the criteria for the common-mode gain, CMG, to be negligible compared to the open-loop gain, $A_o(\omega)$, are as follows:

1. For the inverting configuration,

$$CMG \ll \frac{A_o(\omega)\,Z_i}{R_r} \quad (70)$$

2. For the noninverting configuration,

$$CMG \ll \frac{A_o(\omega)\,Z_i}{Z_i + R_r} \quad (71)$$

Eq. (68) or inequality (70) shows that the gain of an inverting configuration is not affected by the common-mode gain when the input impedance $V_i$ is assumed to be infinite. However, when this same assumption is made for a noninverting configuration, the gain is dependent upon the common-mode gain provided the open-loop gain is finite.

Inequalities (70) and (71) may be given in terms of the common-mode rejection, CMR, which is the open-loop gain, $A_o(\omega)$, divided by the common-mode gain, CMG. The following inequalities are then obtained:

1. For the inverting configuration,

$$CMR \gg \frac{R_r}{Z_i} \quad (72)$$

2. For the noninverting configuration,

$$CMR \gg \frac{Z_i + R_r}{Z_i} \quad (73)$$

Neither of these inequalities places a stringent restriction on common-mode rejection.

## FEEDBACK PHASE SHIFTS IN OPERATIONAL AMPLIFIERS

In an operational amplifier, as in any other feedback amplifier, the phase of the feedback must be controlled to assure that the design is stable with frequency and that the desired gain-frequency response is obtained. Fig.4 shows the gain and phase characteristics as functions of frequency for a typical 60-dB operational amplifier in which no phase-compensation techniques are employed. Over the frequency range shown, the change in the phase of the feedback is substantially greater than 180 degrees. This phase response indicates that a low-frequency negative feedback can become positive and cause the amplifier to be unstable at high frequencies unless phase-compensation methods are employed to stabilize and control the response of the amplifier.

### Effect of Excessive Phase Shift on Frequency Stability

The transfer equation for the inverting configuration, Eq. (7), can be rearranged so that it reflects the same classical feedback form as that for the noninverting configuration, given by Eq. (45). These equations, which are based on the assumptions that $Z_i$ approaches infinity and $Z_{oi}$ is zero, are repeated below for convenience:

1. For the inverting configuration,

$$\frac{V_{OUT}}{V_{IN}} = \left(\frac{Z_f}{Z_f + R_r}\right)\left[\frac{-A_o(\omega)}{1 + \frac{A_o(\omega)}{1 + \frac{Z_f}{Z_r}}}\right]$$

2. For the noninverting configuration,

$$\frac{V_{OUT}}{V_{IN}} = \frac{A_o(\omega)}{1 + \frac{A_o(\omega)}{1 + \frac{Z_f}{Z_r}}}$$

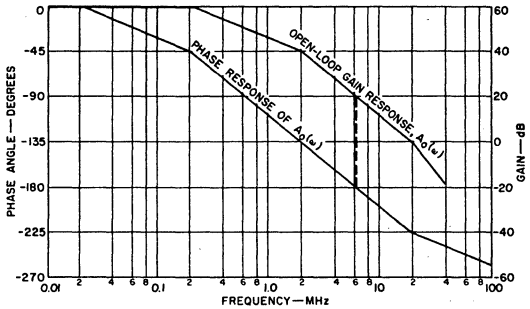



*Fig.4 - Gain and phase response of an open-loop operational amplifier operated without phase compensation.*

If the phase angle of the feedback term, $A_o(\omega)/(1 + Z_f/Z_r)$, reaches 180 degrees (not asymptotically) while the magnitude of the term is still unity or greater, oscillations will occur. [If the term is greater than unity, the oscillations will build until limiting occurs. This limiting decreases $A_o(\omega)$, and thus the entire feedback term, until unity magnitude at a phase angle of 180 degrees is achieved.] These unstable conditions can be predicted readily. Fig.5 shows a superposition of the gain-frequency curve shown in Fig.4 on several

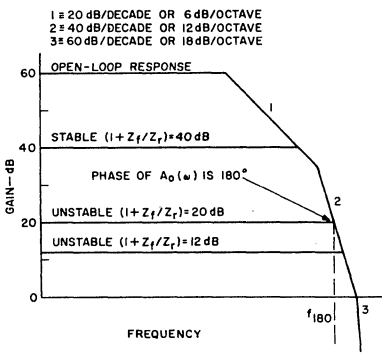



*Fig.5 - Open-loop response and stability characteristics of an operational amplifier.*

sample plots of the ideal feedback characteristic, as given by $1 + Z_f/Z_r$ when $Z_f$ and $Z_r$ are purely resistive. Because the crucial frequency for a purely resistive feedback network is that at which $A_o(\omega)$ has a phase angle of 180 degrees, the magnitude of $A_o(\omega)/(1 + Z_f/Z_r)$ at this frequency ($f_{180}$) determines whether the configuration is stable. If $A_o(f_{180})/(1 + Z_f/Z_r)$ is equal to or greater than unity, the configuration is *unstable*. On the other hand, if this term is less than unity, then the configuration is *stable*. This stability-determination technique is applied to the various values of $1 + Z_f/Z_r$ shown in Fig.5; in each case, the gain of the amplifier at the frequency for which the phase angle is 180 degrees is assumed to be 10 [i.e., $A_o(f_{180}) = 10$].

When $1 + Z_f/Z_r = 100/\underline{0^\circ}$, the stability ratio is calculated as follows:

$$\frac{A_o(f_{180})}{1 + \frac{Z_f}{Z_r}} = \frac{10/\underline{180^\circ}}{100/\underline{0^\circ}} = 0.10/\underline{180^\circ}$$

Because the value of 0.10 obtained for the stability ratio is less than unity, the configuration is stable.

When $1 + Z_f/Z_r = 10.0/\underline{0^\circ}$, the stability ratio becomes

$$\frac{A_o(f_{180})}{1 + \frac{Z_f}{Z_r}} = \frac{10/\underline{180^\circ}}{10/\underline{0^\circ}} = 1.0/\underline{180^\circ}$$

For this case, the stability ratio is unity, and the configuration therefore, is unstable. As a check, an examination of the transfer expressions for both the inverting and the noninverting configuration [Eqs. (7) and (45)] reveals that for the condition specified, each contains the following term:

$$\frac{1}{1 + 1/\underline{180^\circ}}$$

which is not finite and, therefore, indicates an oscillating condition.

When $1 + Z_f/Z_r = 4.0/\underline{0^\circ}$,

$$\frac{A_o(f_{180})}{1 + \frac{Z_f}{Z_r}} = \frac{10/\underline{180^\circ}}{4/\underline{0^\circ}} = 2.50/\underline{180^\circ}$$

The value obtained is greater than unity, and the circuit, therefore, is unstable.

When $Z_f$ and $Z_r$ are not restricted to purely resistive values, a more general situation exists because the phase of $A_o(\omega)/(1 + Z_f/Z_r)$ is no longer dependent solely upon $A_o(\omega)$. Two examples which essentially cover the field are given below.

***Example No.1*** – A characteristic of differentiating or peaking circuits is that the feedback term $1 + Z_f/Z_r$ is in the form $K(1 + jf/f_1)$, where K and $f_1$ are constants. Fig.6 shows a curve of this term as a function of frequency, for K = 10 and $f_1$ = 0.1 MHz, superimposed upon an operational-amplifier open-loop transfer curve. The equation for the open-loop characteristic can be derived from Fig.5, as follows:

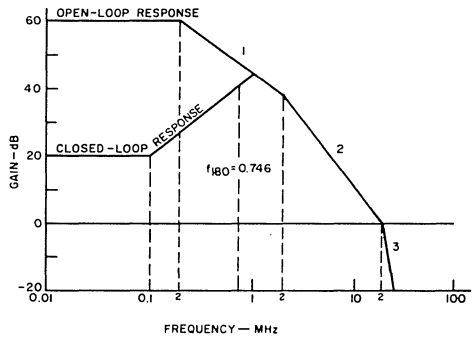



*Fig.6 - Basic peaking response characteristics of an operational amplifier.*

$$A_o(\omega) = \frac{1000}{\left(1 + j\frac{f}{0.2\ MHz}\right)\left(1 + j\frac{f}{2\ MHz}\right)\left(1 + j\frac{f}{20\ MHz}\right)}$$

$$1 + \frac{Z_f}{Z_r} = 10\left(1 + j\frac{f}{0.1\ MHz}\right)$$

$$A_o(\omega) = \frac{1000}{\left(1 + j\frac{f}{0.2\ MHz}\right)\left(1 + j\frac{f}{2\ MHz}\right)\left(1 + j\frac{f}{20MHz}\right)} \quad (74)$$

The frequency at which the stability ratio $A_o(\omega)/1 + Z_f/Z_r$ has a phase angle of 180 degrees and the magnitude of the ratio for this frequency can then be calculated. The computation reveals that the phase angle is 180 degrees at a frequency ($f_{180}$) of 0.746 MHz, and the magnitude of the ratio is 3.22 at that frequency. The stability ratio is greater than one; therefore, the configuration is *unstable*. The point of instability ($f_{180}$) is marked in Fig.6.

The stability of an operational amplifier may be determined more easily from an *estimate* of the phase angle of the ratio $A_o(\omega)/(1 + Z_f/Z_r)$ at the frequency of intersection (where the magnitude of the ratio is unity). If the estimate shows that the phase angle is less than 180 degrees, the configuration is stable. On the other hand, if the estimate indicates a phase angle in excess of 180 degrees, the circuit is unstable. When the estimate shows that the phase angle is near 180 degrees, an accurate calculation is required to determine whether the operational amplifier is stable. This border-line type of configuration, however, is generally undesirable from the standpoint of frequency response, as discussed later.

In the application of the estimation technique to the problem presented in Fig.6, the following conditions should be noted: The feedback characteristic $1 + Z_f/Z_r$ increases at the rate of 6 dB per octave (20 dB per decade) for a full decade before it intersects the open-loop response, $A_o(\omega)$. The intersection occurs near the second corner of the open-loop response, which decreases at the rate of 6 dB per octave for almost a full decade. The classical phase relationships associated with these observations are used to obtain the following phase estimates:

$$\text{Phase of } (1 + Z_f/Z_r) = +90°$$
$$-135° < \text{Phase of } A_o(\omega) < -90°$$

Therefore, the following phase estimate is obtained at the frequency of the intersection:

$$-225° < \text{Phase of } A_o(\omega)/(1 + Z_f/Z_r) < -180°$$

Thus, the configuration is *unstable.*

***Example No.2*** – An inherent characteristic of integrating or band-limiting configurations is that the feedback term $1 + Z_f/Z_r$ has the following form:

$$\frac{K}{1 + jf/f_1}$$

An example of this type of feedback characteristic is shown in Fig.7 for K = 10 and $f_1$ = 4 MHz. The application of the phase-estimation technique to this problem results in the following estimates:

$$-45° > \text{Phase of } 1 + Z_f/Z_r > -90°$$
$$-135° > \text{Phase of } A_o(\omega) > -225°$$

At the frequency of intersection, therefore, the phase estimate is given by

$$-45° > \text{Phase of } A_o(\omega)/(1 + Z_f/Z_r) > -180°$$

Thus, the configuration is *stable.*

If the three basic types of feedback characteristics shown in Figs.5, 6, and 7 are compared, it becomes evident that the differentiating or frequency-peaking

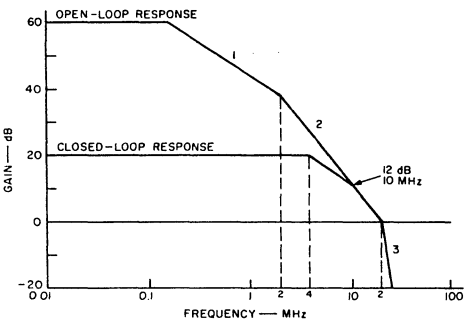



*Fig.7 - Basic integrating response characteristics of an operational amplifier.*

configuration is the most unstable and that the integrating or low-pass configuration is the most stable. In fact, the techniques used to devise this latter configuration may be considered a form of phase compensation for certain situations, as discussed later.

### Effects of Excessive Phase-Shift on Frequency Response

The criterion evolved for frequency stability neither precludes uncontrolled frequency peaking nor provides for a 3-dB closed-loop bandwidth prediction. The conditions that are required to develop a stable, controlled-response feedback amplifier are evolved in this section.

***Criteria for a Peaked Response*** – Frequently peaking results when the magnitude of the true closed-loop gain, as given by Eq. (7) for the inverting configuration and by Eq. (45) for the noninverting configuration, is greater than the magnitude of the ideal closed-loop gain ($Z_f/Z_r$ for an inverting circuit and $1 + Z_f/Z_r$ for a noninverting circuit). The criteria for frequency peaking can be expressed for both configurations by the following expressions:

$$\left| \frac{A_o(\omega)}{1 + \frac{A_o(\omega)}{1 + \frac{Z_f}{Z_r}}} \right| > \left| 1 + \frac{Z_f}{Z_r} \right| \tag{75}$$

Inequality (75) may be used to develop a set of criteria that predict frequency peaking (or preclude the occurrence of frequency peaking).

The following substitution is first made in inequality (75):

$$\frac{A_o(\omega)}{1 + \frac{Z_f}{Z_r}} \equiv B\underline{/\theta} \tag{76}$$

If both sides of inequality (75) are then divided by the left-hand term, the following result is obtained:

$$1 > \left| 1 + \frac{1}{B}\underline{/-\theta} \right| \tag{77}$$

Inequality (77) may be rewritten in either of the following forms:

$$1 > \left[ \left( 1 + \frac{1}{B}\cos\theta \right)^2 + \left( -\frac{1}{B}\sin\theta \right)^2 \right]^{\frac{1}{2}} \tag{78}$$

or

$$1 > \left[ 1 + \frac{2}{B}\cos\theta + \left( \frac{1}{B} \right)^2 \right]^{\frac{1}{2}} \tag{79}$$

The real and imaginary parts of inequality (78) must also be less than unity, so that

$$1 > \left| 1 + \frac{1}{B}\cos\theta \right| \tag{80}$$

and

$$1 > \frac{1}{B}\left| -\sin\theta \right| \tag{81}$$

It is apparent from inequality (80) that

$$B > \frac{1}{2} \tag{82}$$

and from inequality (79) that

$$\cos\theta < -\frac{1}{2B} \tag{83}$$

The substitution indicated by the identity (76) is again made, and both sides of inequality (75) are then divided by the right-hand term to obtain the following expressions:

$$\left| \frac{B\underline{/\theta}}{1 + B\underline{/\theta}} \right| > 1 \tag{84}$$

or

$$B\underline{/\theta} \; | > | \; 1 + B\underline{/\theta} \; | \tag{85}$$

*For peaking to occur,* the following relationships must be in effect:

$$0.5 < \left| B\angle\theta \right| < 2.62$$

$$\cos\theta < -\frac{1}{2B}$$

***3-dB Bandwidth Prediction*** – The 3-dB bandwidth of an operational amplifier is defined by the following condition:

$$\left| \frac{A_o(\omega)}{1 + \frac{A_o(\omega)}{1 + \frac{Z_f}{Z_r}}} \right| = \frac{\left| 1 + \frac{Z_f}{Z_r} \right|}{\sqrt{2}} \tag{86}$$

The terms of Eq. (86) are rearranged and the definition for $B\angle\theta$ given by the identity (76) is used to obtain the following relationships:

$$\left| 1 + \frac{1}{B}\angle -\theta \right| = \sqrt{2}$$

$$\left(1 + \frac{1}{B}\cos\theta\right)^2 + \left(-\frac{1}{B}\sin\theta\right)^2 = 2$$

$$1 + \frac{2}{B}\cos\theta + \left(\frac{1}{B}\right)^2 = 2 \tag{87}$$

Eq. (87) yields the following criteria for the 3-dB point:

$$1 \geq B > \frac{1}{1 + \sqrt{2}} = 0.414 \tag{88}$$

$$\cos\theta = \frac{B^2 - 1}{2B} \tag{89}$$

Inequality (88) predicts the possibility of a 3-dB bandwidth greater than that indicated by the intersection of $A_o(\omega)$ and $1 + Z_f/Z_r$ ($B = 1$ point). However, it should be realized that this "bandwidth extension" is actually caused by a slight peaking effect. Special care should be exercised in any attempt to use this effect to advantage.

Inequality (89) stipulates that the phase angle must be 90 degrees to obtain the 3-dB bandwidth where $B = 1$. This stipulation essentially coincides with a "rule of thumb" that has become a standard in the industry. This rule may be stated as follows: *For an unconditionally stable configuration, the ideal feedback characteristic, $1 + Z_f/Z_r$, must intersect the open-loop response, $A_o(\omega)$, at a slope less than 12 dB per octave.* An examination of this "rule of thumb" in terms of the phase relationship indicates that the phase angle asymptotically approaches 180 degrees when the change in amplifier response with frequency occurs at a rate of 12 dB per octave. Therefore, the amplifier is on the threshold of instability. Frequency dependence of less than 12 dB per octave indicates that the amplifier is stable; a dependence of greater than 12 dB per octave indicates that the amplifier is unstable.

## PHASE-COMPENSATION TECHNIQUES FOR OPERATIONAL AMPLIFIERS

The design problems (i.e., ac instability and uncontrolled frequency response) created by excessive phase shift in the feedback can be solved by use of compensating techniques that alter the feedback response so that excessive phase shifts no longer occur. The frequency response can be controlled by limiting the slope of the intersection of the ideal feedback characteristic, $1 + Z_f/Z_r$, with the open-loop gain response, $A_o(\omega)$, to a safe value. Theoretically, this slope can have a maximum value of 12 dB per octave under certain conditions. In general, however, the maximum slope allowed for practical lumped-parameter systems is 6 dB per octave. In an operational amplifier, effective phase compensation can be accomplished only by a modification in one or more of the following parameters:

1. the ideal closed-loop gain (feedback characteristic), $1 + Z_f/Z_r$;
2. the open-loop input impedance, $Z_i$;
3. the open-loop gain, $A_o(\omega)$.

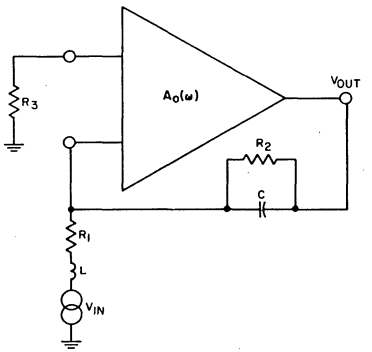
### Closed-Loop Compensation Method

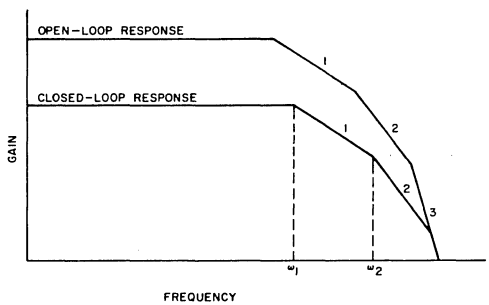
Phase compensation can be accomplished by modification of the closed-loop gain characteristic (i.e., the $1 + Z_f/Z_r$ term) for only those applications in which the intersection of the $1 + Z_f/Z_r$ characteristic with the open-loop response occurs in a region where the open-loop response rolls off at a slope of 12 dB per octave or 18 dB per octave. When the intersection occurs in a 12-dB-per-octave region of the $A_o(\omega)$ response, compensation techniques are used that cause the slope of the $1 + Z_f/Z_r$ response to roll off at 6 dB per octave near the intersection. As a result of these techniques, the slope of the intersection becomes 6 dB per octave. (An example of this method of phase compensation was discussed earlier, in the section on "Criteria for a Peaked Response", and the response curves for this example were shown in Fig.7.)

For applications in which the use of an inductor is permissible, phase compensation in the 18-dB-per-

octave region of the open-loop response can be accomplished by techniques that cause the $1 + Z_f/Z_r$ response to roll off at 12 dB per octave near the intersection. An example of this method of phase compensation, together with the appropriate response curves, is shown in Fig.8.

In this example, the $Z_f$ term is altered by a shunt capacitor and the $Z_r$ term is altered by a series inductor so that the $1 + Z_f/Z_r$ response has the required 12-dB-per-octave roll-off. The location of these frequency-dependent components in the feedback configuration is unique for this type of phase compensation.




$$R_3 = R_1 /\!/ R_2$$

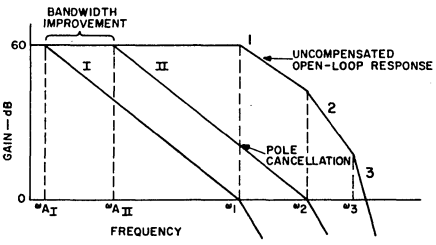
$$\frac{V_{OUT}}{V_{IN}} = \frac{-\dfrac{R_2}{1 + j\omega CR_2}}{R_1 + j\omega L}$$

$$= -\frac{R_2}{R_1}\left[\frac{1}{\left(1 + j\dfrac{\omega L}{R_1}\right)(1 + j\omega CR_2)}\right]$$

*Fig.8 - Phase compensation of operational amplifier permissible in the "three-slope region".*

**Open-Loop Compensation Methods**

Phase-compensation techniques that alter either the open-loop input impedance or the open-loop gain permit the introduction of a zero, in addition to the low-frequency pole, into the open-loop gain characteristic. This zero can be designed to cancel one of the poles in the open-loop gain characteristic and thus to increase substantially the bandwidth of the operational amplifier. Alternatively, the operational-amplifier bandwidth can be increased by the introduction of a pole at a frequency low enough so that all the other corner points will occur at frequencies below that at which the open-loop response, $A_o(\omega)$, intersects the closed-loop response, $1 + Z_f/Z_r$. The two methods are compared in Fig.9. It is apparent that the pole-cancellation method of phase compensation is superior to the method in




I—Compensated open-loop response using simple depression of higher corner frequencies.

II—Compensated open-loop response using pole cancellation.

*Fig.9 - Phase compensation of operational amplifier by use of pole cancellation.*

which the other corner frequencies are depressed. In the phase-compensation techniques discussed below, therefore, the pole-cancellation method is employed.

***Modification of the Open-Loop Input Impedance*** — The following analysis shows the limitations imposed on alterations in the open-loop input impedance of an operational amplifier in order to provide phase compensation. In this phase-compensation technique, an appropriate network is connected between the input terminals so that it appears in parallel with the intrinsic input impedance, $Z_i$. Eqs. (7) and (45), which define the closed-loop inverting and noninverting responses, respectively, are used as the basis for establishing the conditions and the mechanisms involved in this kind of compensation.

If $Z_i'$ is used to represent the modified open-loop input impedance and the open-loop output impedance,

$Z_{oi}$, is assumed to be zero, the following equations for the closed-loop response are obtained:

1. For the inverting configuration,

$$\frac{V_{OUT}}{V_{IN}} = \frac{-A_o(\omega)\, Z_i'\, Z_f}{Z_f\,(Z_i' + R_r) + Z_r\,(Z_f + Z_i' + R_r) + A_o(\omega)\, Z_i'\, Z_r} \quad (90)$$

2. For the noninverting configuration,

$$\frac{V_{OUT}}{V_{IN}} = \frac{A_o(\omega)\, Z_i'\,(Z_r + Z_f)}{(Z_i' + R_r)\,(Z_r + Z_f) + Z_r\, Z_f + A_o(\omega)\, Z_i'\, Z_r} \quad (91)$$

A judicious rearrangement of terms in Eqs. (90) and (91) reveals the effect that the altered open-loop input impedance has on the open-loop response. With this rearrangement, the equation for the inverting configuration becomes

$$\frac{V_{OUT}}{V_{IN}} = \frac{-\left[\frac{A_o(\omega)\, Z_i'}{R_r + Z_r + Z_i'}\right] Z_f}{Z_f + \frac{Z_r\,(Z_i' + R_r)}{R_r + Z_r + Z_i'} + \left[\frac{A_o(\omega)\, Z_i'}{R_r + Z_r + Z_i'}\right] Z_r} \quad (92)$$

The equation for the noninverting configuration is then written as follows:

$$\frac{V_{OUT}}{V_{IN}} = \frac{\left[\frac{A_o(\omega)\, Z_i'}{R_r + Z_r + Z_i'}\right] (Z_r + Z_f)}{Z_f + \frac{Z_r\,(Z_i' + R_r)}{R_r + Z_r + Z_i'} + \left[\frac{A_o(\omega)\, Z_i'}{R_r + Z_r + Z_i'}\right] Z_r} \quad (93)$$

For each configuration, the modified open-loop response is defined as follows:

$$A_o'(\omega) \equiv \frac{A_o(\omega)\, Z_i'}{R_r + Z_r + Z_i'} \quad (94)$$

It is apparent from Eq. (94) that the alteration of the open-loop input impedance has no effect on the open-loop response unless $Z_i'$, is at most, of the same order of magnitude as the $R_r + Z_r$ term. If $Z_i'$ is made much less than $R_r + Z_r$, Eq. (94) becomes

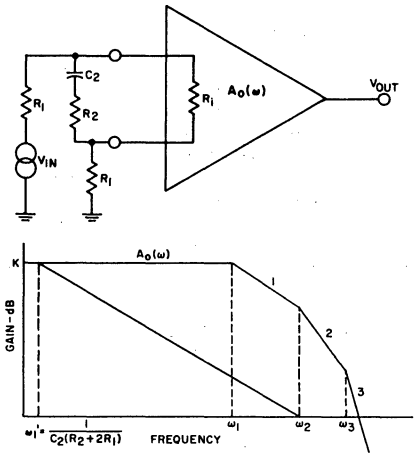
$$A_o'(\omega) \doteq \frac{A_o(\omega)\, Z_i'}{R_r + Z_r} \quad (95)$$

As predicted by Eqs. (94) and (95), three limitations are imposed in the use of the input-impedance modification technique to provide phase compensation: (1) the feedback impedance term $Z_r$ is restricted in value and configuration by the phase-compensation requirements; (2) the effective open-loop input impedance must be smaller in magnitude than and different in configuration from the intrinsic input impedance, $Z_i$ (thus the closed-loop input impedance, $Z_{IN}$, also is smaller and different); and (3) the dc open-loop gain is less for some input-impedance configurations.

Two examples of the input-impedance phase-compensation technique are shown in Figs. 10 and 11. In the method shown in Fig.10, the required modification of the open-loop response is achieved by proper choice of the frequency characteristics for the network connected in shunt with the input terminals of the operational amplifier. Fig.11 shows that the required modification of the response can be achieved by the appropriate choice of the frequency characteristics of $R_r$ and $Z_r$. Both techniques employ pole-zero cancellation to extend the 6 dB-per-octave roll-off region depicted. The technique illustrated in Fig.10 causes an early roll-off, while the one shown in Fig.11 results in a reduction in the dc open-loop gain. Eqs. (94) and (95) indicate that phase-compensation can also be effected by an increase in the magnitude of $R_r + Z_r$, provided that the frequency characteristics of this parameter are controlled. However, this technique relies on the accuracy of the value of $Z_i$ and therefore is unsatisfactory. (The intrinsic input impedance of an operational amplifier may vary significantly from unit to unit.)

***Modification of Open-Loop Gain Characteristics*** – Phase compensation that is effected by internal modification of the open-loop gain response is the most widely accepted technique for integrated-circuit operational amplifiers. This method offers two distinct advantages over other types of phase compensation. First, the internal-modification technique affords complete isolation of the phase-compensation networks from the feedback parameters. This isolation is not possible with the compensation methods discussed previously. Second, the point at which the phase compensation is applied can be selected so that the open-loop response is altered in such a way that one of the existing 3-dB corner frequencies becomes the early roll-off corner in the compensated response. The advantage stems from the fact that no new corner frequencies are introduced, and an improved compensated response is thus obtained.

Internal phase compensation can be accomplished by either of two basic methods. In one method, referred to as the straight roll-off, an appropriate RC network is connected across a suitable internal resistor of the operational amplifier. With this method, the early roll-off starts at the corner frequency produced by the phase-compensating capacitor and the internal resistor. The other method is the Miller-effect roll-off. In this method, the phase-compensating network still appears electrically to be placed across an appropriate internal resistance of the amplifier, but is actually connected between the input and the output of an inverting-gain stage in the operational amplifier. The impedance of the compen-




$A_o(\omega)$ = uncompensated open-loop gain
$A_o'(\omega)$ = compensated open-loop gain
$R_i$ = low-frequency intrinsic input impedance

$$A_o'(\omega) = \frac{\pm A_o(\omega) R_i \left(R_2 + \frac{1}{j\omega C_2}\right)}{\left(R_i + R_2 + \frac{1}{j\omega C_2}\right) 2R_1 + R_i \left(R_2 + \frac{1}{j\omega C_2}\right)}$$

$$A_o'(\omega) = \left[\frac{\pm A_o(\omega) R_i}{2R_1 + R_i}\right]\left[\frac{1 + j\omega R_2 C_2}{1 + j\omega C_2 \left(R_2 + \frac{2R_i R_1}{2R_1 + R_i}\right)}\right]$$

Because $R_i$ is normally large, the equation for $A_o'(\omega)$ may be rewritten as follows:

$$A_o'(\omega) = \pm A_o(\omega) \frac{1 + j\omega R_2 C_2}{1 + j\omega C_2 (R_2 + 2R_1)}$$

For $$A_o(\omega) = \frac{K}{\left(1 + j\frac{\omega}{\omega_1}\right)\left(1 + j\frac{\omega}{\omega_2}\right)\left(1 + j\frac{\omega}{\omega_3}\right)}$$

and if $$R_2 C_2 = \frac{1}{\omega_1}$$

the equation for $A_o'(\omega)$ becomes

$$A_o'(\omega) = \frac{K}{[1 + j\omega C_2 (R_2 + 2R_1)]\left(1 + j\frac{\omega}{\omega_2}\right)\left(1 + \frac{\omega}{\omega_3}\right)}$$

*Fig.10 - Phase compensation of operational amplifier in which open-loop response is modified by connection of a compensating network that provides the required frequency characteristics in shunt with input terminals.*

sating network then appears to be divided by the gain of that stage.

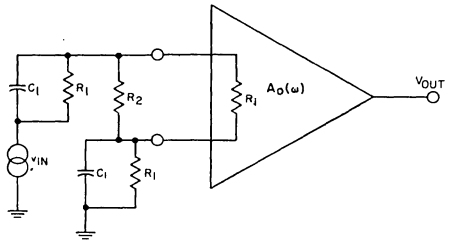
The Miller-effect roll-off technique requires a much smaller phase-compensating capacitor than that which must be used with the straight roll-off method. Moreover, the reduction in swing capability which is inherent in the straight roll-off is delayed significantly when the Miller-effect roll-off is used. Fig.12 illustrates the solution to the problem of phase compensation of an operational amplifier in which a straight roll-off is used to cause the second 3-dB corner frequency to occur at unity gain. Fig.13 illustrates the use of a Miller-effect roll-off to solve the same problem. For the same early corner frequency, the compensating capacitance required in the Miller-effect method is less than that required in the straight roll-off method by a factor of $1 + g_{mII}R_{c2}$ ($g_{mII}$ and $R_{c2}$ are defined in Fig.13).

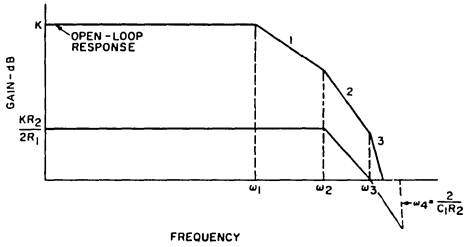
## DESIGN CRITERIA FOR OPERATIONAL AMPLIFIERS

It is apparent from the previous discussions that a completely universal design of an operational amplifier would have to satisfy an impossible set of criteria. As a result, the design of operational amplifiers is a somewhat specialized process in that a particular amplifier is usually designed for specific applications. For example, certain operational amplifiers are designed to provide high-frequency gain at the expense of other performance characteristics, while other operational amplifiers provide very high gain or high input impedance in low-frequency applications. Integrated-circuit operational amplifiers, which are fabricated by the diffusion process, can be made suitable for comparator applications or can be processed to provide high gain at low dissipation levels. For these reasons, any discussion of the criteria for operational amplifiers must be of a general nature unless a specific application is being considered.

### Input and Output DC Levels

In general, an operational amplifier should be designed so that the dc bias levels at the input and the output are equal. This condition is desirable to assure that the resistive feedback network can be connected between the input and the output without upsetting either the differential or the common-mode dc bias. Moreover, for applications in which two (positive and negative) power supplies are used, the operational amplifier should be designed so that it is possible to establish a set of standard supply values for which the equal input and output bias levels are at zero potential with respect to circuit ground. This latter condition is particularly important in direct-coupled cascade and comparator applications.




$A_o(\omega)$ = uncompensated open-loop gain
$A_o'(\omega)$ = compensated open-loop gain

$$A_o'(\omega) = \frac{\pm A_o(\omega)\, R_2\, R_i}{(R_2 + R_i)\left(\frac{2R_1}{1 + j\omega_1 R_1 C_1}\right) + R_2 R_i}$$

$$= \left[\frac{\pm A_o(\omega)\, R_2\, R_i}{2R_1(R_2+R_i) + R_2 R_i}\right] \left[\frac{1 + j\omega R_1 C_1}{1 + j\omega \frac{R_1 R_2 R_i C_1}{2R_1(R_2+R_i) + R_2 R_i}}\right]$$

Because $R_i$ is normally large, the equation for $A_o'(\omega)$ may be rewritten as follows:

$$A_o'(\omega) = \left(\frac{\pm A_o(\omega)\, R_2}{2R_1 + R_2}\right)\left(\frac{1 + j\omega R_1 C_1}{1 + j\omega \frac{C_1 R_1 R_2}{2R_1 + R_2}}\right)$$

If $R_2 << R_1$, the equation for $A_o'(\omega)$ becomes

$$A_o'(\omega) \doteq \left(\frac{\pm A_o(\omega)\, R_2}{2R_1}\right)\left(\frac{1 + j\omega R_1 C_1}{1 + j\omega C_1 \frac{R_2}{2}}\right)$$

For $$A_o(\omega) = \frac{K}{\left(1 + j\frac{\omega}{\omega_1}\right)\left(1 + j\frac{\omega}{\omega_2}\right)\left(1 + j\frac{\omega}{\omega_3}\right)}$$

and $$R_1 C_1 \equiv \frac{1}{\omega_1},$$

the compensated open-loop gain $A_o'(\omega)$ is given by

$$A_o'(\omega) = \frac{\pm K}{2\frac{R_1}{R_2}\left(1 + j\omega C_1 \frac{R_2}{2}\right)\left(1 + \frac{\omega}{\omega_2}\right)\left(1 + \frac{\omega}{\omega_3}\right)}$$

*Fig.11 - Phase compensation of operational-amplifier in which open-loop response is modified by alteration of the $R_f + Z_f$ term to provide the required frequency characteristics.*

### Output-Power Capability

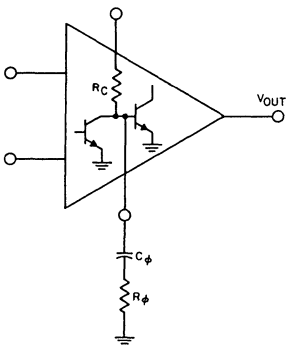
As with any amplifier circuit, the output-power requirements for an operational amplifier depend almost entirely on the application. A few general conclusions can be drawn concerning the design of the output stage. First, this stage should provide a voltage swing essentially equal to the sum of the power-supply voltages. It should have sufficient gain so that it is the first stage to limit when the amplifier is overdriven. Finally, because of the design trade-off that is always required between output-power capability and dissipation, the output stage should be sufficiently versatile so that the output capability and dissipation can be tailored to the power needs of the particular application in which the operational amplifier is used.

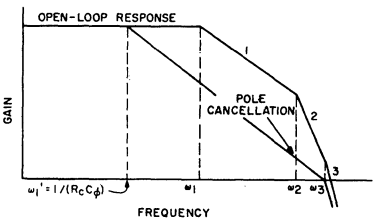
### Gain and Frequency-Response Characteristics

The numerical values of the open-loop gain and the 3-dB bandwidth of an operational amplifier are of relatively little importance in themselves. The important requirement is that the open-loop gain must be much greater than the closed-loop gain of the transfer response over the frequency range of interest if an accurate transfer function is to be maintained. (This requirement is explained in detail in the discussions of transfer functions for both the inverting and noninverting configurations.) For example, if a 40-dB amplifier and a 60-dB amplifier are used in a 20-dB gain configuration and the open-loop gain is decreased 50 per cent in each case, the closed-loop gain of the 40-dB amplifier varies only 9 per cent and that of the 60-dB amplifier varies only 1 per cent.

The frequency roll-off characteristics are the prime determinants of the frequency response of an operational amplifier. The greater the rate of roll-off prior to the intersection of the feedback-ratio frequency characteristic with the open-loop response (in the active region), the more difficult phase compensation of the operational amplifier becomes. An 18-dB-per-octave roll-off is generally considered the maximum slope that can occur in the active region before proper phase compensation becomes extremely difficult or impossible to achieve

(as indicated in the discussion on the effects of feedback phase shifts). In addition, because operational amplifiers have useful applications down to and including unity gain, the active region of the amplifier may be considered as the entire portion of the frequency characteristic above its 0-dB bandwidth. Therefore, a well-designed amplifier should roll off at no greater than 18 dB per octave until well below unity gain.




$A_o(\omega)$ = uncompensated open-loop gain
$A_o'(\omega)$ = compensated open-loop gain

$$A_o'(\omega) = A_o(\omega)\left(1 + j\frac{\omega}{\omega_1}\right)\frac{1 + j\omega R_\phi C_\phi}{1 + j\omega R_c C_\phi}$$

The $1 + j\,\omega/\omega_1$ term in the equation above accounts for the modification of the $\omega_1$ 3-dB corner.

For $$R_\phi C_\phi = \frac{1}{\omega_2}$$

and $$A_o(\omega) = \frac{K}{\left(1 + j\frac{\omega}{\omega_1}\right)\left(1 + j\frac{\omega}{\omega_2}\right)\left(1 + j\frac{\omega}{\omega_3}\right)}$$

the equation for $A_o'(\omega)$ becomes

$$A_o'(\omega) \doteq \frac{K}{(1 + j\omega R_c C_\phi)\left(1 + j\frac{\omega}{\omega_3}\right)}$$

A third corner-frequency term, which occurs because of the time constant of $R_\phi$ and the input capacitance of the succeeding stage, should also be included in the equation above; the effects of this corner frequency, however, is appreciable only at very high frequencies (and usually at a gain less than unity). Because the corner frequency normally occurs well out of the active region, it is omitted in the expression for $A_o'(\omega)$.

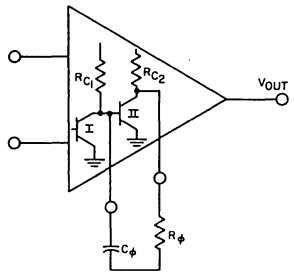
*Fig.12 - Phase compensation of operational amplifier by use of straight-rolloff method to modify open-loop response.*

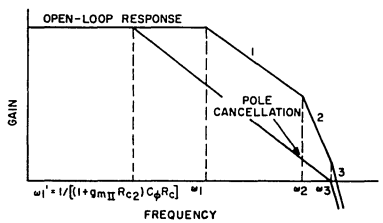
### Intrinsic Input and Output Impedances

The ideal values for the input and output impedances of an operational amplifier are infinity and zero, respectively (as mentioned in the discussions on input and output impedances for both inverting and noninverting configurations). The degree to which a practical amplifier approximates these values depends, for the most part, upon the application. A 5000-ohm open-loop input impedance may be quite sufficient for one application, while a 0.1-megohm intrinsic input impedance may not be sufficient for another. In most applications, however, the restrictions on the intrinsic input impedance are not severe. The closed-loop input impedance, which is equal to the product of the intrinsic input impedance and the gain "throwaway" or loop gain, is a more critical parameter. This parameter effectively increases the input impedance (decreases input capacitance) and is the reason that many operational amplifiers that have an input roll-off in the active region have no input roll-off in this region after negative feedback is applied.

Because the closed-loop output impedance is also affected by the loop gain (the proportionality is inverse), the same conclusions might be drawn about the importance of the intrinsic output impedance. Another factor, however, affects the restrictions placed upon the open-loop output impedance. A limiting situation in an inverting-configuration application affords an alternate path to the signal when the intrinsic output impedance is sufficiently high. The loop gain decreases to zero as the open-loop gain decreases when overdrive occurs. Therefore, the closed-loop output impedance increases until it equals the intrinsic value at full limiting. Thus, the intrinsic output must be much less than the lowest

practical value of feedback impedance or an alternate signal path that effectively bypasses the limiting amplifier will exist through the feedback network.




$A_o(\omega)$ = uncompensated open-loop gain
$A_o'(\omega)$ = compensated open-loop gain

$$A_o'(\omega) = A_o(\omega)\left(1 + j\frac{\omega}{\omega_1}\right)\frac{1 + j\omega R_\phi C_\phi}{1 + j\omega R_c (1 + g_{mII} R_{c2}) C_\phi}$$

The $1 + j\,\omega/\omega_1$ term in the expression for $A_o'(\omega)$ accounts for the modification of the $\omega_1$ 3-dB corner.

For $$R_\phi C_\phi = \frac{1}{\omega_2}$$

and $$A_o(\omega) = \frac{K}{\left(1 + j\frac{\omega}{\omega_1}\right)\left(1 + j\frac{\omega}{\omega_2}\right)\left(1 + j\frac{\omega}{\omega_3}\right)}$$

The expression for $A_o'(\omega)$ becomes

$$A_o'(\omega) \doteq \frac{K}{[1 + j\omega (1 + g_{mII} R_{c2}) C_\phi R_c]\left(1 + j\frac{\omega}{\omega_3}\right)}$$

A third corner frequency, which results from the time constant of $R_\phi$ and the feedback capacitance $C_{bc'}$, is neglected in the expression for $A_o'(\omega)$, because this corner frequency occurs well out of the active region.

*Fig.13 - Phase compensation of operational amplifier by use of Miller effect to modify open-loop response.*

### Common-Mode Rejection

Under differential drive conditions, the common-mode rejection has no drastic effects on the performance of the operational amplifier unless the rejection ratio is extremely low (as discussed in respect to the effects of common-mode gain). However, in a common-mode drive situation, such as in a comparator type of application, high common-mode rejection is imperative. For example, if a 60-dB differential amplifier having a 50-dB common-mode rejection is used to compare a 1-volt signal against a 1-volt reference, the output will be 3.2 volts when it should be zero. Such results would be disastrous for almost any application of this type. In general, the common-mode rejection should be a minimum of 20 dB greater than the differential gain.

### Input Bias Current

Although an amplifier may have a high intrinsic input ac impedance, it can still require a significant amount of dc input bias current. This condition is undesirable in applications in which the drive source cannot accommodate a significant dc current. Examples of such applications are those that require very high impedance sources or sources of a magnetic nature that can be severely unbalanced by a flow of dc current. Unfortunately, the bipolar transistor remedies for this effect add so much capacitance that the frequency response of the amplifier is impaired. Therefore, either field-effect devices should be used in the differential input stage or a scheme should be available to assure that a very low bias current is obtained when it is absolutely necessary. The latter technique requires that sufficient leads be provided so that two external transistors can be added to form a Darlington or a modified Darlington input configuration.

### Offset Voltage and Current

The offset voltage of an operational amplifier is the deviation of the output dc level from the arbitrary input-output level usually taken as ground reference when both inputs are shorted together. The offset current is the deviation when the inputs are driven by two identical dc input bias-current constant-current sources. These two offset parameters are usually referred to the input because their output values are dependent on feedback. Under normal operating conditions, the offset in the amplifier results from a combination of the two factors. For example, if an operational amplifier has a 1-millivolt input offset voltage and a 1-microampere input offset current with the inputs returned to ground through 1000-ohm resistors, the total input offset is either zero or 2 millivolts depending upon the phase relationship between the two offset parameters. The offset of an operational amplifier is a dc error and should be minimized for numerous reasons, including the following:

(1) The use of an operational amplifier as a true dc amplifier is limited to signal levels much greater than the offset. (2) Comparator applications require that the output voltage be zero (within limits) when the two input signals are equal and in phase. (3) In a direct-coupled cascade, such as a video amplifier chain, the input offset of the first stage determines the offset characteristics of the entire system. Hence, the gain of the system must be limited to a value that is insufficient to cause limiting at rated output voltage. This value is reduced when the offset is significant.

### Power-Supply Stability

The power-supply stability is a measure of the sensitivity that the offset has to power-supply variations. Because the value of the offset at the output is dependent on feedback, this sensitivity is normally referred to the input and expressed in microvolts per volt. In a fixed-installation application that employs heavily regulated power supplies, this parameter is of little importance. In battery-operated applications of the operational amplifier, however, the sensitivity of the offset to power-supply variations is of the utmost importance. In a single-supply system, this sensitivity should be an absolute minimum. In a two-supply system, the difference in the sensitivities to each supply can be minimized because the supplies in many dual systems tend to track. This tracking results in a cancellation, or at least a partial cancellation, of the two sensitivities.

### Temperature-Stability Requirements

Temperature stability of an operational amplifier requires stable thermal characteristics for most of the parameters discussed in this Note. The stability demands imposed on the temperature characteristics of an operational amplifier are determined to a large extent by the application in which the circuit is used. In certain applications, stable temperature characteristics are of utmost importance; in other applications, the ability of the operational amplifier to perform the required functions is not appreciably affected by variations in circuit parameters with temperature.

In general, the dependence of the open-loop gain on temperature is of less importance than the thermal behavior of the amplifier frequency response. Variations in the intrinsic input and output impedances with temperature are of little consequence provided that the input impedance remains large enough and the output impedance remains small enough to satisfy the requirements of the application. If the value of the input bias current is important for the application in which the operational amplifier is used, stable temperature behavior is just as important. Variations in the offset voltage and current with temperature should always be small because they directly affect the internal biases, and thus the operation, of the operational amplifier.

# APPLICATION OF THE RCA-CA3018 INTEGRATED-CIRCUIT TRANSISTOR ARRAY

BY

G.E. THERIAULT, A.J. LEIDICH, AND T.H. CAMPBELL

The CA3018 integrated circuit consists of four silicon epitaxial transistors produced by a monolithic process on a single chip mounted in a 12-lead TO-5 package. The four active devices, two isolated transistors plus two transistors with an emitter-base common connection, are especially suitable for applications in which closely matched device characteristics are required, or in which a number of active devices must be interconnected with non-integrable components such as tuned circuits, large-value resistors, variable resistors, and microfarad bypass capacitors. Such areas of application include if, rf (through 100 MHz), video, agc, audio, and dc amplifiers. Because the CA3018 has the feature of device balance, it is useful in special applications of the differential amplifier, and can be used to advantage in circuits which require temperature compensation of base-to-emitter voltage.

## CIRCUIT DESCRIPTION AND OPERATING CHARACTERISTICS

The circuit configuration for the CA3018 is shown in Fig. 1. In a 12-lead TO-5 package, because it is necessary to provide a terminal for connection to the substrate, two transistor terminals must be connected to a common lead. The particular configuration chosen is useful in emitter-follower and Darlington circuit connections. In addition, the four transistors can be used almost independently if terminal 2 is grounded or ac grounded so that Q3 can be used as a common-emitter amplifier and Q4 as a common-base amplifier. In pulse video amplifiers and line-driver circuits, Q4 can be used as a forward-biased diode in series with the emitter of Q3. Q3 may be

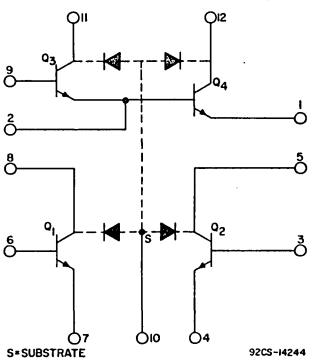



*Fig. 1—Schematic diagram and TO-5 terminal connections for the CA3018 integrated-circuit transistor array.*

used as a diode connected to the base of Q4; in a reverse-biased connection, Q3 can serve as a protective diode in rf circuits connected to operational antennas. The presence of Q3 does not inhibit the use of Q4 in a large number of circuits.

In transistors Q1, Q2, and Q4, the emitter lead is interposed between the base and collector leads to minimize package and lead capacitances. In Q3, the substrate lead serves as the shield between base and collector. This lead arrangement reduces feedback capacitance in common-emitter amplifiers, and thus extends video bandwidth and increases tuned-circuit amplifier gain stability.

Operating characteristics for the CA3018 are given in the technical bulletin.

## CIRCUIT APPLICATIONS

The applications for the CA3018 are many and varied. The typical applications discussed in this Note have been selected to demonstrate the advantages of four matched devices available on a single chip. These few examples should stimulate the generation of a great many more applications.

### Video Amplifiers

A common approach to video-amplifier design is to use two transistors in a configuration designed to reduce the feedback capacitance (appearing as a Miller capacitance) inherent in a single triode device. Three configurations which utilize two devices are (1) the cascode circuit, (2) the single-ended differential-amplifier, and (3) the common-collector, common-emitter circuit. In all three circuits, the output-to-input feedback capacitance is minimized by isolation inherent in the configuration. The availability of four identical transistors in a common package provides a convenient vehicle for these circuit configurations for video-amplifier design. Two of the many possible circuit variations are discussed below.

**Broadband Video Amplifier.** A broadband video-amplifier design using the CA3018 is shown in Fig. 2. This amplifier may be considered as two dc-coupled stages, each consisting of a common-emitter, common-collector configuration. The common-collector transistor provides a low-impedance source to the input of the common-emitter transistor and a high-impedance, low-capacitance load at the common-emitter output. Iterative operation of the video amplifier can be achieved by capacitive coupling of stages.

Two feedback loops provide dc stability of the broadband video amplifier and exchange gain for bandwidth. The feedback loop from the emitter of $Q_3$ to the base of $Q_1$ provides dc and low-frequency feedback; the loop from the collector of $Q_4$ to the collector of $Q_1$ provides both dc feedback and ac feedback at all frequencies.

The frequency response of the broadband video amplifier is shown in Fig. 3. The upper 3-dB break occurs at a frequency of 32 MHz. The low-frequency 3-dB characteristics are determined primarily by the values of capacitors $C_1$, $C_2$, and $C_3$. The low-frequency 3-dB break

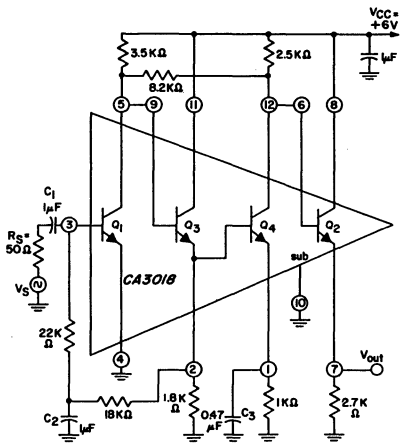



*Fig. 2—Schematic diagram for a CA3018 broadband video amplifier.*

occurs at 800 Hz. The mid-frequency gain of 49 dB is constant to within 1 dB over the temperature range from −55° to +125°C. The upper 3-dB break is constant at 32 MHz from −55°C to +25°C, and drops to 21 MHz at +125°C.

The total power dissipation over the entire temperature range is 22.8 milliwatts. The dc output voltage varies from 2.33 volts at −55°C to 3 volts at +125°C. The tangential sensitivity occurs at 20 microvolts peak-to-peak. The dynamic range is from 20 microvolts peak-to-peak to 4 millivolts rms at the input.

The circuit of Fig. 2 demonstrates a typical approach that can be altered, especially with regard to gain and bandwidth, to meet specific performance requirements.

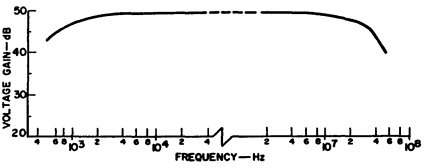



*Fig. 3—Voltage gain as a function of frequency for the broadband video amplifier of Fig. 2.*

**Cascode Video Amplifier.** The cascode configuration offers the advantages of common-emitter gain with reduced feedback capacitance and thus greater bandwidth. Fig. 4 shows a typical circuit diagram of a cascode video amplifier using the CA3018. Transistors $Q_2$ and $Q_1$ comprise the common-emitter and common-base portions of

the cascode, respectively. The common-base unit is followed by cascaded emitter followers ($Q_3$ and $Q_4$) which provide a low output impedance to maintain bandwidth for iterative operation.

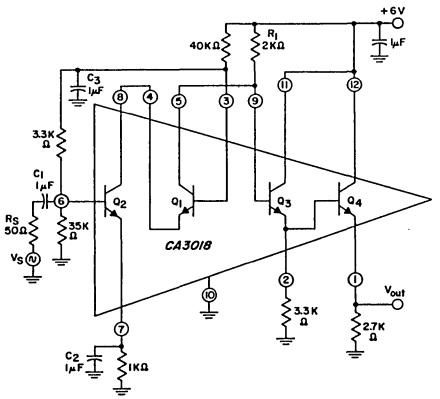



*Fig. 4—Schematic diagram for a CA3018 cascode video amplifier.*

The frequency response of the cascode video amplifier is shown in Fig. 5. The lower and upper 3-dB points occur at frequencies of 6 KHz and 11 MHz, respectively. The lower 3-dB point is primarily a function of capacitors C1, C2, and C3. The upper 3-dB point is a function of the devices and of the load resistor $R_1$, and is 10.5 MHz at −55°C and 5 MHz at +125°C.

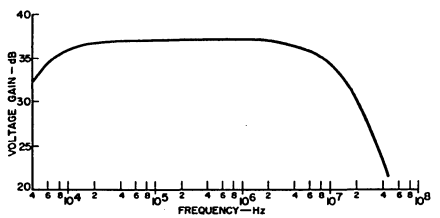
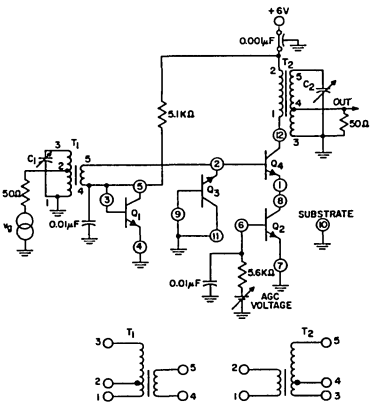



*Fig. 5—Voltage gain as a function of frequency for the cascode amplifier of Fig. 4.*

The mid-frequency voltage gain of the amplifier is 37 dB ± 1 dB over the temperature range from −55°C to +125°C. The power dissipation varies from 16.8 milliwatts at −55°C to 17.6 milliwatts at +125°C. The amplifier has a tangential sensitivity of 40 microvolts peak-to-peak and a useful dynamic input range from 40 microvolts to 16.6 millivolts peak-to-peak.

## 15-MHz RF Amplifier

Fig. 6 shows a typical design approach for a tuned amplifier for use in the frequency range of 2 to 30 MHz in military receivers. This circuit was designed for a mid-band frequency of 15 MHz to demonstrate its capability. Gain is obtained in a common-emitter stage ($Q_4$). Transistor $Q_2$ is used as a variable resistor in the emitter of $Q_4$ to provide improved signal-handling capability with agc. Transistor $Q_1$ is used as a bias diode to stabilize $Q_4$ with temperature, and the reverse breakdown of $Q_3$ as a diode is used to protect the common-emitter stage from signal overdrive of adjacent transmitters.




| | |
|---|---|
| L = 0.8 μH | L = 0.8 μH |
| $Q_0$ = 200 | $Q_0$ = 200 |
| $T_{1\text{-}3}$ = 6T | $T_{3\text{-}5}$ = 6T |
| $T_{1\text{-}2}$ = 1T | $T_{1\text{-}2}$ = 4T |
| $T_{4\text{-}5}$ = 2T | $T_{3\text{-}4}$ = 1T |

#22 wire on Q-2 material, CF107 Torroid from Indiana General.

$C_1$, $C_2$ = Arco 425 or equiv.

*Fig. 6—Schematic diagram for a CA3018 15-MHz rf amplifier.*

The tuned-circuit design of Fig. 6 utilizes mismatching to obtain stability. Although the usable stable gain for a common-emitter amplifier using this type of transistor is 26 dB at 15 mHz, the tuned rf amplifier was designed for a total gain of 20 dB to obtain greater stability and more uniform performance with device variations. The general performance characteristics of the circuit are as follows:

| | |
|---|---|
| Power Gain | 20 dB |
| Power-Gain Variation from −55 to +125°C | ±1 dB |

| | |
|---|---|
| Bandwidth | 315 kHz |
| Noise Figure at Full Gain | 7.4 dB |
| AGC Range | 45 dB |
| Power Dissipation | 1.8 mW |

Fig. 7 shows the cross-modulation characteristics of the circuit for in-band signals. For out-of-band undesired signals, the cross-modulation performance is improved by the amount of attenuation provided by the input tuned circuit. Cross-modulation performance also improves (i.e. more interfering signal voltage is required for cross-modulation distortion of 10 per cent) with increased agc as a result of the degeneration in the emitter of $Q_4$.

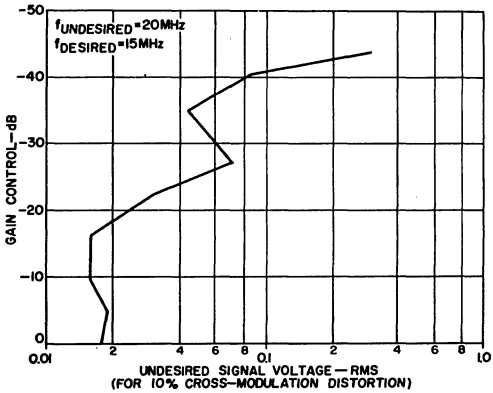



*Fig. 7—In-band cross-modulation characteristic of 15-MHz amplifier of Fig. 6 (data taken with untuned input).*

### Final If Amplifier Stage and Second Detector

Fig. 8 illustrates the use of the CA3018 as a last if amplifier and second detector (0.1 volt emitter voltage on terminal 1). The bias on transistor $Q_4$ is maintained at approximately cutoff to permit the cascaded emitter-follower configuration ($Q_3$ and $Q_4$) to be used as a second detector. Because this stage is driven by a common collector configuration, the input impedance to the detector can be kept high. A low output load impedance can be used as a result of the output current capability of the cascaded emitter-follower configuration. The input impedance (terminal 9) of approximately 9000 ohms is largely determined by the bias network. A minimum if input power of 0.4 microwatt must be delivered to terminal 9 for linear operation. The audio output power for 60 per cent modulation for this drive condition is 0.8 microwatt. Linear detection is obtained through an input range of 20 dB for 60 per cent modulation. This detector arrangement requires less power-output capability from the last if amplifier than a conventional diode detector yet allows a low dc load resistor to achieve a good ac-to-dc ratio for the first audio amplifier.

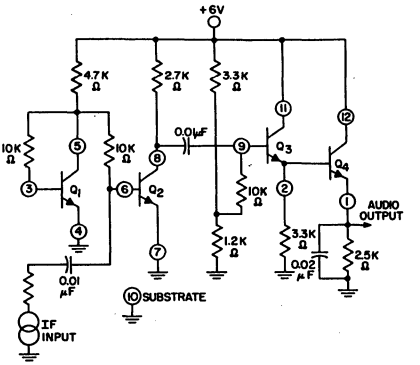



*Fig. 8—Schematic diagram for a CA3018 final if amplifier and second detector.*

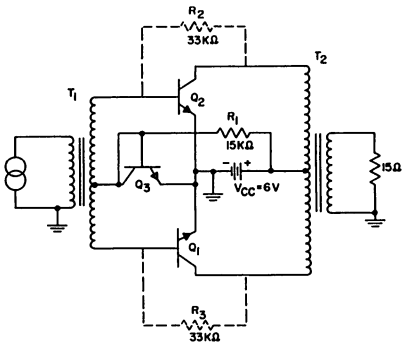
The if amplifier of Fig. 8 has a voltage gain of 30 dB at 1 MHz. Transistor $Q_1$ is used in the base-bias loop of the common-emitter amplifier $Q_2$ to stabilize the output operating point against temperature variations. This arrangement also eliminates the need for an emitter resistor and bypass capacitor, and thus provides a larger voltage-swing capability for $Q_2$. If $Q_2$ is biased conventionally with base-bias resistors, $Q_1$ can be made available for the first audio or agc amplifier.

### Class B Amplifier

Characteristics were obtained on a low-level class B amplifier to establish the idling-current performance of nearly identical devices on a single chip with respect to temperature variations. The transistors in the CA3018 can be used only for low-power class B operation (maximum output of 40 milliwatts) because of the $h_{FE}$ roll-off and moderately high saturation resistance at high currents. A typical circuit is shown in Fig. 9. Idling-current bias is provided to $Q_1$ and $Q_2$ by use of transistor $Q_3$ as a diode (with collector and base shorted) and connection of a series resistor to the supply. The idling current for each transistor in the class B output is equal to the current established in the resistance-diode loop. Because the resistor $R_1$ is the predominant factor in controlling the current in the bias loop, the bias current is relatively independent of temperature. In addition, because the devices have nearly equal characteristics and are at the same temperature, the idling current is nearly independent through the full military temperature range. The total idling current for transistors $Q_1$ and $Q_2$ in Fig. 9 varies from 0.5 to 0.6 miliiampere from $-55$ to $+125$°C. Excellent balance between output devices is achieved throughout the range.

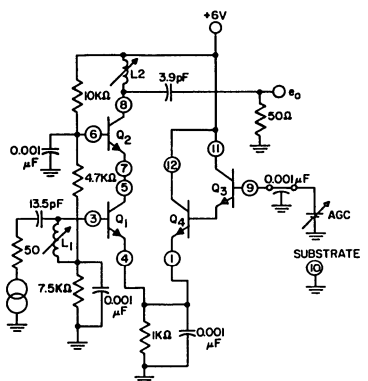
AC feedback as well as dc feedback can be obtained by substitution of two resistors $R_2$ and $R_3$ in place of $R_1$,

as shown by the dotted lines in Fig. 9. These two resistors, which have a parallel combination equal to $R_1$, are connected between collector and base of transistors $Q_2$ and $Q_1$. The added feedback reduces the power gain by approximately 6 dB (30 to 24 dB), but improves the linearity of the circuit. Although the output-power capability for the circuit shown in Fig. 9 is approximately 18 milliwatts, output levels up to 40 milliwatts can be obtained in similar configurations with optimized components.




$T_1$ — ADC Products No. 5SX1322 or equiv.
$T_2$ — Chicago Standard Trans. Corp. No. TA-10 or equiv.
Note: $R_1$ is removed when $R_2$ and $R_3$ are added.

*Fig. 9—Schematic diagram for a CA3018 class B amplifier.*




$L_1$ = 0.11 to 0.17 μH
$L_2$ = 0.5 to 0.8 μH

*Fig. 10—Schematic diagram for a CA3018 100-MHz cascode amplifier.*

## 100-MHz Tuned RF Amplifier

Fig. 10 illustrates the use of the CA3018 in a 100-MHz cascode circuit with an agc amplifier. Transistors $Q_1$ and $Q_2$ are used in a cascode configuration, and transistors $Q_3$ and $Q_4$ are used to provide an agc capability and amplification. With a positive-going agc signal, current in the cascode amplifier is transferred to the Darlington configuration by differential-amplifier action. This agc amplifier has the advantage of low-power drive (high input impedance). In addition, the emitter of $Q_1$ can be backbiased with respect to the base to provide larger input-signal-handling capability under full agc conditions.

The operating characteristics of the amplifier shown in Fig. 10 are as follows:

| | |
|---|---|
| Power Gain | — 26 dB |
| Agc Range | — 70 dB |
| 3-dB Bandwidth | — 4.5 MHz |
| Noise Figure | — 6.8 dB |
| Power Dissipation | — 7.7 mW |

The response characteristic is shown in Fig. 11

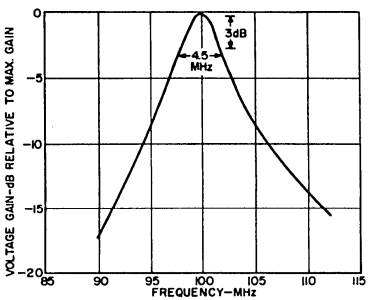



*Fig. 11—Response characteristic of 100-MHz amplifier of Fig. 10.*

# APPLICATION OF THE RCA-CA3019 INTEGRATED-CIRCUIT DIODE ARRAY

BY
G. E. THERIAULT AND R. G. TIPPING

The RCA-CA3019 integrated circuit diode array provides four diodes internally connected in a diode-quad arrangement plus two individual diodes. Its applications include gating, mixing, modulating, and detecting circuits.

The CA3019 features all-monolithic-silicon epitaxial construction designed for operation at ambient temperatures from −55°C to 125°C. It is supplied in a 10-terminal TO-5 low silhouette package.

Because all the diodes are fabricated simultaneously on a single silicon chip, they have nearly identical characteristics, and their parameters track each other with temperature variations as a result of their close proximity and the good thermal conductivity of silicon. Consequently, the CA3019 is particularly useful in circuit configurations which require either a balanced diode bridge or identical diodes.

## CIRCUIT CONFIGURATION AND OPERATING CHARACTERISTICS

Fig. 1 shows the circuit diagram and terminal connections for the CA3019. Diodes $D_1$ through $D_4$ are internally interconnected to form a diode quad, while diodes $D_5$ and $D_6$ are available as independent diodes. Each diode is formed from a transistor by connection of the collector and the base to form the diode anode and use

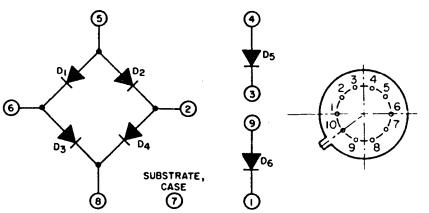
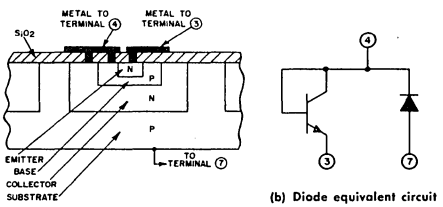



*Fig. 1—Schematic diagram and terminal connections for the CA3019 integrated-circuit diode array.*

of the emitter for the diode cathode (this technique is one of five methods by which the transistor structure can be utilized as a diode). This diode configuration, in which the collector-base junction is shorted, is the most useful connection for a high-speed diode because it has the lowest storage time. The only charge stored is that in the base. This configuration also exhibits the lowest forward voltage drop, and is the only one which has no p-n-p transistor action to the substrate. The diode has the emitter-to-base reverse breakdown voltage characteristic (typically 6 volts).

The monolithic process produces a substrate diode between the collector of a transistor and its supporting substrate, as shown in Fig. 2. Connected at each diode anode,

therefore, is the cathode of a substrate diode for which the anode is the substrate (terminal 7). In some applications, the substrate can be left floating because a forward bias on any substrate diode creates a self reverse-bias on the other substrate diodes. However, the uncertainty of this bias and the capacitive feedthrough paths provided by the substrate make it advisable to apply a reverse bias to all substrate diodes by returning the substrate through terminal 7 to a dc voltage which is more negative than the most negative voltage on a diode anode. Such reverse bias is most important when ac circuit balance is essential because the capacitance of the substrate diodes is a nonlinear function of the voltage across them. In such circuits, the changing capacitance of these parasitic elements can make good balance over a wide dynamic range impossible.




(a) Cross section of monolithic diode structure

(b) Diode equivalent circuit

*Fig. 2—Diagram and equivalent circuit of the monolithic array.*

Reverse bias of the substrate diodes is always indicated, therefore, and should be omitted only if the inclusion of such bias is not possible or practical. Terminal 7 may be returned to a negative power supply as long as the combined value of that supply voltage and the maximum positive voltage on any diode anode does not exceed the maximum rating of 25 volts. In systems that use single power supplies, the active circuit may be raised above ground potential and the signals coupled into the diodes by capacitive or inductive means.

The operating characteristics of the CA3019 integrated diode array are determined primarily by the individual diode characteristics, which are given in the technical bulletin.

## APPLICATIONS

Although there are many possible applications for the CA3019, this note describes a few practical circuits to stimulate the thinking of the potential user. Besides the obvious uses as separate diodes and possible quad combinations, some of which are covered in the following discusssion, it should be noted that shorting of terminals 2 and 6 in the quad effectively provides two diodes in series. This diode connection can be used as the elements of special balanced mixers, as ring modulators, and as compensating networks that provide two diode drops. Fig. 3 shows an example of a typical synthesizer mixer circuit.

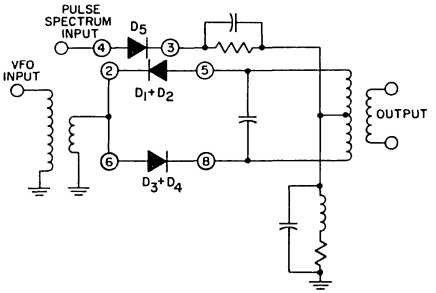



*Fig. 3—Typical synthesizer mixer circuit.*

Shorting of terminals 5 and 8 provides two independent sets of back-to-back diodes useful for limiting and clipping, as shown in Fig. 4.

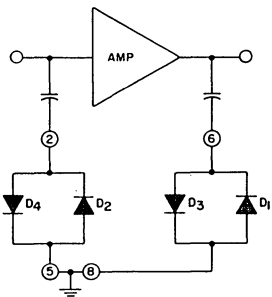



*Fig. 4—Limiters using the CA3019.*

### Balanced Modulator

Fig. 5 shows the use of the CA3019 as a balanced modulator which minimizes the carrier frequency from the output by means of a symmetrical bridge network. A carrier of one polarity causes all the diodes to conduct, and thus effectively short-circuits the signal source. A carrier of the opposite polarity cuts off all the diodes and allows signal current to flow to the load. If the four diodes are identical, the bridge is perfectly balanced and no carrier current flows in the output load. Table I lists the characteristics of the balanced modulator.

### High-Speed Gates

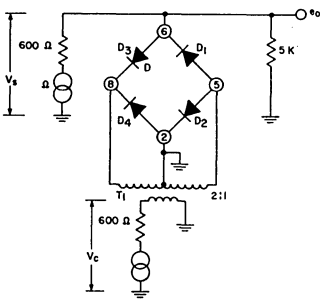
In high-speed gates, the gating signal often appears at the output and causes the output signal to ride a "pedestal." A diode-quad bridge circuit can be used to balance out the undesired gating signal at the output and reduce the pedestal to the extent that the bridge is balanced.

## TABLE I. CHARACTERISTICS OF BALANCED MODULATOR OF FIG.5

| | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Carrier Voltage VRMS at 30 KHz | 0.75 | | 0.75 | | 0.75 | | 0.50 | | 1.0 | |
| Signal Voltage mVRMS at 2 KHz | 77 | | 245 | | 770 | | 245 | | 245 | |
| *Output Frequency KHz* | *Output Voltage mV rms* | *db Below Vs* | *Output Voltage mV rms* | *db Below Vs* | *Output Voltage mV rms* | *db Below Vs* | *Output Voltage mV rms* | *db Below Vs* | *Output Voltage mV rms* | *db Below Vs* |
| 28 and 32* | 34 | 6.5 | 115 | 7 | 440 | 5 | 51 | 14 | 170 | 3 |
| 30 | 0.7 | 41 | 0.82 | 49 | 2.6 | 50 | 0.1 | 68 | 3.6 | 37 |
| 26 and 34 | 0.02 | 72 | 0.05 | 72+ | 0.48 | 64 | 0.04 | 72+ | 0.07 | 71 |
| 24 and 36 | 0.03 | 69 | 0.49 | 54 | 60 | 22 | 0.58 | 52.5 | 0.6 | 53 |
| 22 and 38 | 0.001 | 72+ | 0.01 | 72+ | 1.4 | 55 | .015 | 72+ | 0.02 | 72+ |

* Double-Sideband, Suppressed-Carrier Output.

All other outputs are spurious signals.

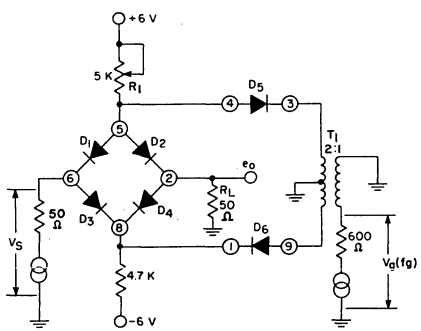



T1 — Technitrol No. 8511660 or equiv.

*Fig. 5—Balanced modulator using the CA3019.*

A diode-quad gate functions as a variable impedance between a source and a load, and can be connected either in series or in shunt with the load. The circuit configuration used depends on the input and output impedances of the circuits to be gated. A series gate is used if the source and load impedances are low compared to the diode back resistance, and a shunt gate is used if the source and load impedances are high compared to the diode forward resistance.

**Series Gate.** Fig. 6 shows the use of the CA3019 as a series gate in which the diode bridge, in series with the load resistance, balances out the gating signal to provide a pedestal-free output. With a proper gating voltage (1 to 3 volts rms, 1 to 500 kHz), diodes $D_5$ and $D_6$ conduct during one half of each gating cycle and do not conduct during the other half of the cycle. When diodes $D_5$ and $D_6$ are conducting, the diode bridge ($D_1$ through $D_4$) is not conducting and the high diode back resistance prevents the input signal $V_s$ from appearing across the load resistance $R_L$; when diodes $D_5$ and $D_6$ are not conducting, the diode bridge conducts and the low diode forward resistance allows the input signal to appear across the load resistance. Resistor $R_1$ may be adjusted to minimize the




T1 — Technitrol No. 8511666 or equiv.

*Fig. 6—Series gate using the CA3019.*

gating voltage present at the output. The substrate (terminal 7) is connected to the −6-volt supply. Fig. 7 shows the on-to-off ratio of the series gate as a function of frequency.

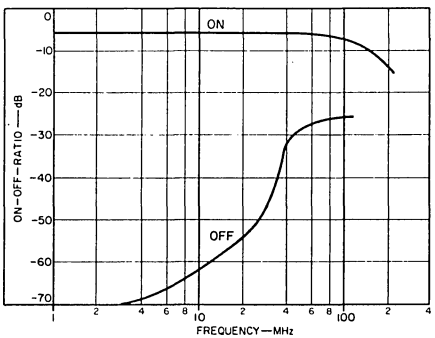
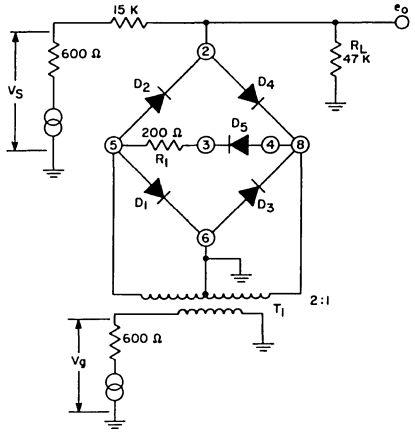



*Fig.7—On-to-off ratio for the series gate of Fig.6 as a function of frequency.*

**Shunt Gate.** Fig. 8 shows the use of the CA3019 as a shunt gate in which the diode bridge, in shunt with the load resistance, balances out the gating signal to provide a pedestal-free output. When the gating voltage $V_g$ is of sufficient amplitude, the diode bridge ($D_1$ through $D_4$) conducts during one half of each gating cycle and does not conduct during the other half of the cycle. When the diode bridge is conducting, its low diode forward resistance shunts the load resistance $R_L$ and prevents the input signal $V_s$ from appearing at the output; when the diode bridge is not conducting, its high diode back resistance allows the input signal to appear at the output. Diode $D_5$ and resistor $R_1$ keep the transformer load nearly constant during both halves of the gating cycle. The substrate (terminal 7) can either be left floating or returned to a negative voltage, but it cannot be returned to ground. The characteristics of the shunt gate are as follows:

Gating frequency ($f_g$) — 1 to 100 kHz
Gating voltage ($V_g$) — 0.8 to 1.2 Vrms
Signal frequency ($f_s$) — dc to 500 kHz (2 dB down)
Signal voltage ($V_g$) — 0 to 1 Vrms

The frequency range of this circuit can be extended by application of a reverse bias to the substrate. The amount of gating voltage $V_g$ present at the output as a function of the amplitude and frequency of $V_g$ is shown in Table II.




$T_1$ — Technitrol No. 8511666 or equiv.

*Fig.8 —Shunt gate using the CA3019.*

**TABLE II. GATING CHARACTERISTICS OF SHUNT GATE SHOWN IN FIG.8**

| *Frequency of $V_g$ kHz* | *Amplitude of $V_g$ volts* | *Present at the Amount of $V_g$ Output mvs* |
|---|---|---|
| 1 | 0.8 | 0.2 |
| 1 | 1.0 | 0.5 |
| 1 | 1.2 | 1.3 |
| 10 | 0.8 | 2.0 |
| 10 | 1.0 | 4.7 |
| 10 | 1.2 | 8.7 |
| 50 | 0.8 | 11.0 |
| 50 | 1.0 | 24.0 |
| 50 | 1.2 | 40.0 |

**Series-Shunt Gate.**

A series-shunt gate which utilizes all six diodes of the CA3019 is shown in Fig. 9 This configuration combines the good on-to-off impedance ratio of the shunt gate with the low-output pedestal of the series gate.

On the gating half-cycle during which the voltage at A is positive with respect to the voltage at B, there is no output because the shunt diodes are forward-biased and

the series diodes are reverse-biased. Any signal passing through the input diodes ($D_4$ and $D_2$) encounters a low shunt impedance to ground ($D_5$ and $D_6$) and a high impedance in series with the signal path to the load ($D_3$ and $D_1$). This arrangement assures a good on-to-off impedance ratio. When the voltages at A and B reverse, the conduction states of the shunt and series diodes reverse, and the signal passes through the gate to the load resistor $R_L$. Any pedestal at the output is a function of the resistor, transformer, and diode balance.

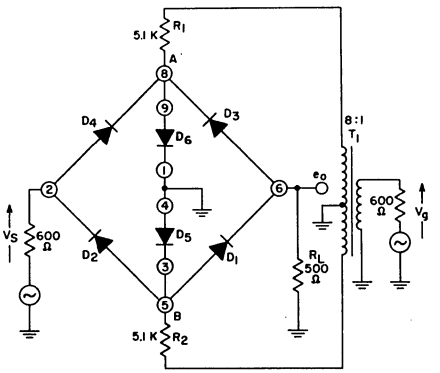



*Fig.9 —Series-shunt gate using the CA3019.*

The gate continues to operate successfully with resistors $R_1$ and $R_2$ shorted if the transformer center tap is removed from ground. In either case, no dc supply is required to bias the gate diodes.

## Balanced Mixer

Fig. 10 illustrates the use of the CA3019 as a conventional balanced mixer. The load resistor across the output tuned circuit is selected to provide maximum power output. The conversion gain of the mixer for a 45-MHz input signal and a 55-MHz oscillator signal is shown in Fig. 11. The input impedance at point A is approximately 600-ohms for a 0.6-volt-rms oscillator drive.

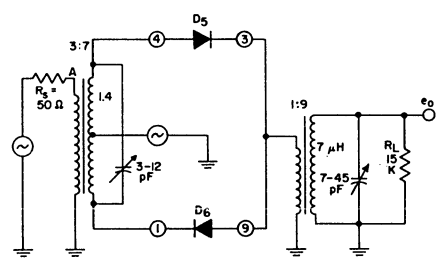



*Fig.10 —Balanced mixer using the CA3019.*

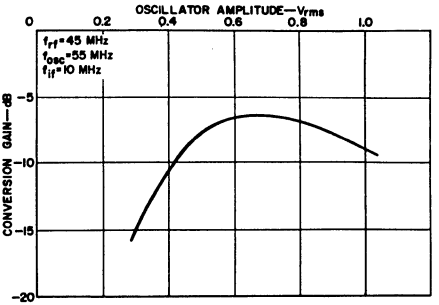



*Fig.11 —Conversion gain as a function of oscillator amplitude for the balanced mixer of Fig.10.*

The CA3019 mixer shown in Fig. 12 is essentially a balanced mixer with two additional diodes ($D_3$ and $D_4$) added to form a half-wave carrier switch. The additional diodes permit both legs of the circuit ($D_1 - D_2$ and $D_3 - D_4$) to function throughout the ac cycle. As compared with a conventional balanced mixer, shown in Fig.10, this circuit effectively doubles the desired output voltage

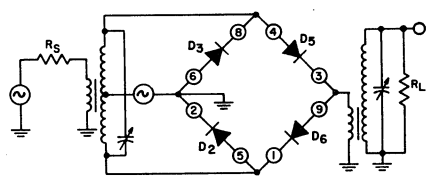



*Fig.12—Balanced mixer with half-wave carrier switch using the CA3019.*

and reduces the output voltage at the oscillator frequency by half. However, the capacitances associated with the integrated diodes prevent this circuit configuration from realizing the improvement in conversion gain at frequencies above 20 MHz.

## Ring Modulator

The use of the CA3019 as a ring modulator is shown in Fig. 13. If a perfectly balanced arrangement were used, carrier current of equal magnitude and opposite direction would flow in each half of the center-tapped transformer $T_2$. Thus, the effect of the carrier current in transformer $T_2$ would be cancelled, and the carrier frequency would not appear in the output. However, the ring modulator of Fig. 13 is not exactly balanced because diodes ($D_1 + D_2$) and ($D_3 + D_4$) are actually two diodes in

parallel, while diodes ($D_5$) and ($D_6$) are individual diodes. Nevertheless, this circuit attenuates the carrier in the output as well as an arrangement that uses both individual diodes in two CA3019 circuits.

As the carrier passes through half of its cycle, diodes ($D_1 + D_2$) and ($D_6$) conduct, and diodes ($D_3 + D_4$) and (D5) do not conduct. When the carrier passes through the other half of its cycle, the previously nonconducting diodes conduct, and vice versa. As a result, the output amplitude, is alternately switched from plus to minus at the carrier frequency. The signal-frequency component of the output waveform is thus symmetrical about the zero axis and is not present in the output. Therefore, the ring modulator suppresses both the carrier frequency and the signal frequency so that the output theoretically contains only the upper and lower sidebands. For single-sideband transmission, one of these sidebands can be eliminated by selective filtering. The performance of the CA3019 as a ring modulator is shown in Table III.

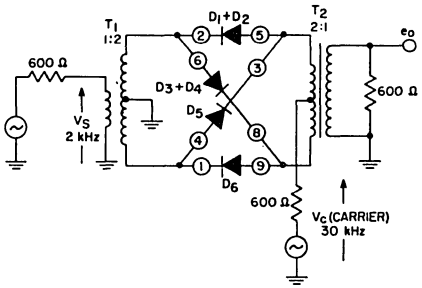



*Fig.13 —Ring modulator using the CA3019.*

## TABLE III. PERFORMANCE CHARACTERISTICS OF RING MODULATION OF FIG.13

| | | For a given $V_S + V_g$, $e_o$ in millivolts | | | |
|---|---|---|---|---|---|
| Output Freq. KHz | $V_s$ mvs | 300 | 350 | 450 | 500 |
| | $V_c$ mvs | 600 | 500 | 350 | 300 |
| 28 or 32 | Upper or Lower Sidebands | 86 | 97 | 83 | 91 |
| 2 | Sig. Freq. | 0.042 | 0.02 | 0.015 | 0.020 |
| 30 | Carrier Freq. | * 1.3 (−37db) | * 0.88 (−41db) | * 0.67 (−42db) | * 0.62 (−43db) |
| 26 or 34 | Higher Order Sidebands | 0.018 | 0.016 | 0.036 | 0.043 |
| 24 or 36 | | 0.021 | 0.054 | 0.047 | 5.0 |

* db below the desired upper and lower sidebands

# Application of the RCA-CA3028A and CA3028B Integrated-Circuit RF Amplifiers in the HF and VHF Ranges

by

H. C. KIEHN

The CA3028A and CA3028B monolithic-silicon integrated circuits are single-stage differential amplifiers. Each circuit also contains a constant-current transistor and suitable biasing resistors. The circuits are primarily intended for service in communications systems operating at frequencies up to 100 MHz with single power supplies. This Note provides technical data and recommended circuits for use of the CA3028A and CA3028B in the following applications:

- RF Amplifier
- Autodyne Converter
- IF Amplifier
- Limiter

In addition to the applications listed above, the CA3028A and CA3028B are suitable for use in a wide range of applications in dc, audio, and pulse amplifier service; they have been used as sense amplifiers, preamplifiers for low-level transducers, and dc differential amplifiers. The CA3028B, which features tight control of operating current, input offset voltage, and input bias and offset current, is recommended for those applications in which balance and operating conditions are important.

Useful information concerning operation of the CA3028A and CA3028B in mixers, oscillators, balanced modulators, and similar circuits may be found in ICAN-5022, "Application of the RCA CA3004, CA3005, and CA3006 Integrated-Circuit RF Amplifiers." Biasing considerations for the CA3028A and CA3028B differ from the types discussed in ICAN-5022; however, dynamic performance is quite similar to that of the CA3005 and CA3006. ICAN-5022 contains circuits that illustrate operation from dual supplies which, when available, can simplify the biasing of the CA3028A or CA3028B.

Both the CA3028A and CA3028B are supplied in an 8-terminal TO-5 package which assures minimum interlead capacitance and consequently excellent stability in high-frequency circuits. The spacing of the leads on the hermetically sealed package permits installation of the integrated circuits on printed circuit boards by wave-soldering techniques.

### Circuit Description

The circuit diagram and terminal connections for the CA3028A and CA3028B are shown in Fig.1. The circuit is basically a single-stage differential amplifier composed of transistors $Q_1$ and $Q_2$ driven from a constant-current source $Q_3$. A single-ended input may be connected to terminal 1 or terminal 5, or push-pull inputs to terminals 1 and 5. Each of these terminals must be provided with a biasing network. Care must be taken to insure that the bias voltages on terminals 1 and 5 are nearly equal when balanced operation is desired. This can only be achieved in practice by using a single voltage divider as shown in Fig.2(a). Bias is first established on the base of one transistor, in this case $Q_1$, through terminal 1. The base of the second transistor, $Q_2$ in Fig.2(a), is then connected to the first through a low-valued dc impedance. In Fig.2(a), the inductive winding of the input transformer provides the

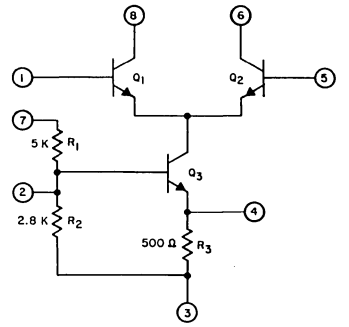
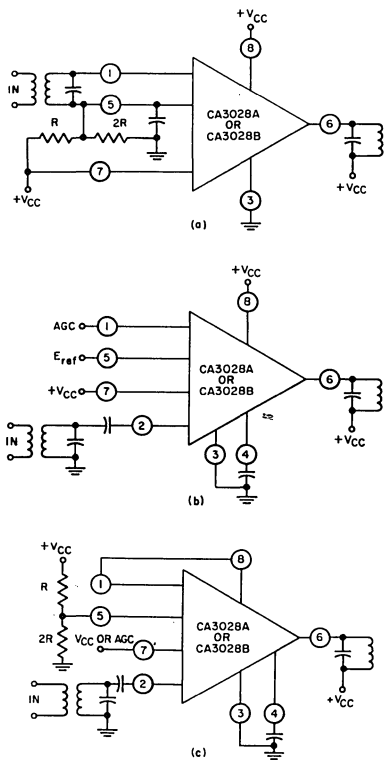



*Fig.1 - Schematic diagram and terminal connections for the CA3028A and CA3028B integrated circuits.*



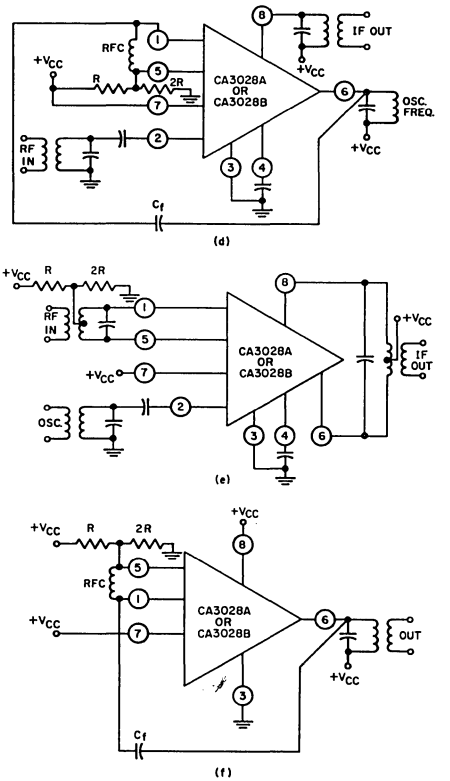




*Fig.2 - Connections for the CA3028A and CA3028B for use as (a) a balanced differential amplifier with a controlled constant-current-source drive and agc capability; (b) a cascode amplifier with a constant-impedance agc capability; (c) a cascode amplifier with conventional agc capability; (d) a converter; (e) a mixer; (f) an oscillator.*

low-resistance path. An rf choke or low-valued resistor may be used in place of transformer coupling, but caution must be exercised because even as little as 100 ohms may cause serious unbalance in some applications. A single-ended output may be taken from terminal 6 or terminal 8, or push-pull outputs from terminals 6 and 8. In systems with a single power supply of up to 12 volts, terminal 7 is connected to the highest positive potential for maximum gain. Other operating points can be selected by application of a varying bias voltage (agc) to $Q_3$.

The circuit diagrams in Fig.2 illustrate the flexibility of the CA3028A and CA3028B. Terminal connections are shown for a differential amplifier driven from a controlled constant-current source that has agc capability; a cascode amplifier with constant-impedance or conventional agc capability; a converter; a mixer; and an oscillator. The cascode mode of operation is recommended for applications that require higher gain. The differential mode is preferred when good limiting is required.

### Operating Modes

The CA3028A and CA3028B integrated-circuit rf amplifiers can be operated in either the differential mode or the cascode mode. Applications using the differential mode are distinguished by high input impedance, good gain-control characteristics, large input-signal-handling capability, and good limiting.

For ease of design of systems using the CA3028A and CA3028B, admittance or "y" parameters are shown in Fig.3 for the differential mode and in Fig.4 for the cascode mode. It should be noted that the y parameters of the more complex differential and cascode amplifier stages differ from those of simple common-emitter transistor stages.

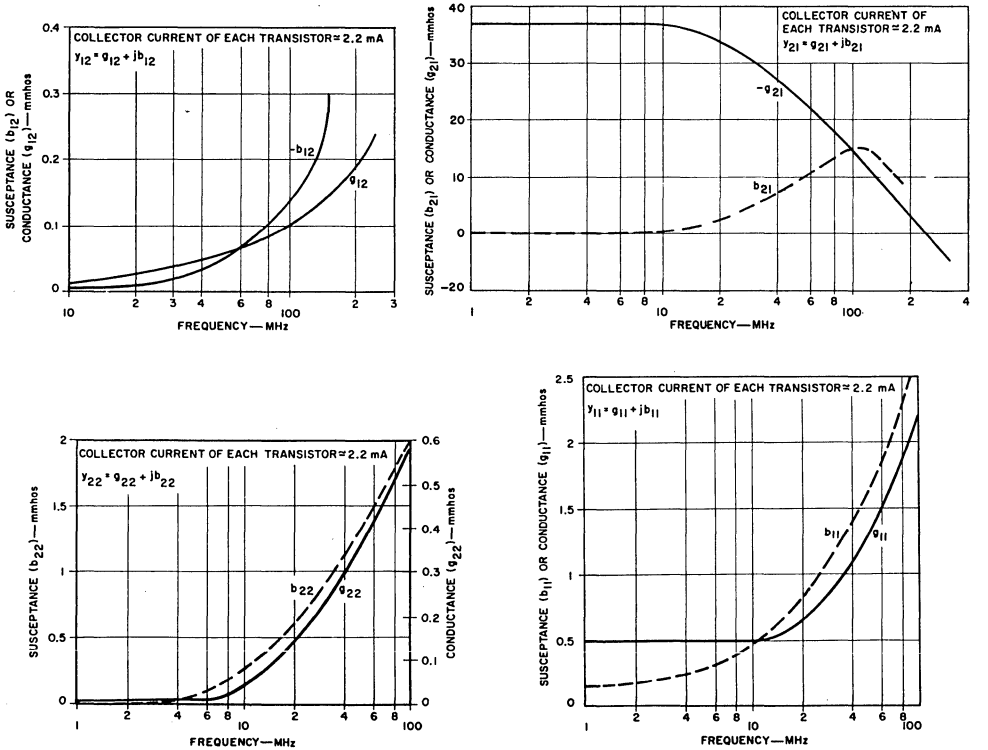
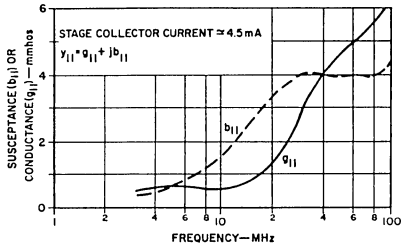
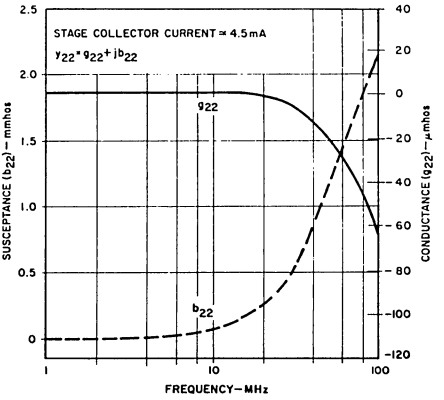
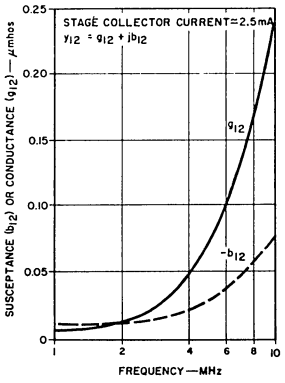
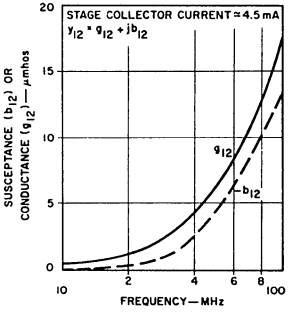



*Fig.3 - Y parameters of the CA3028A and CA3028B in the differential-amplifier connection.*



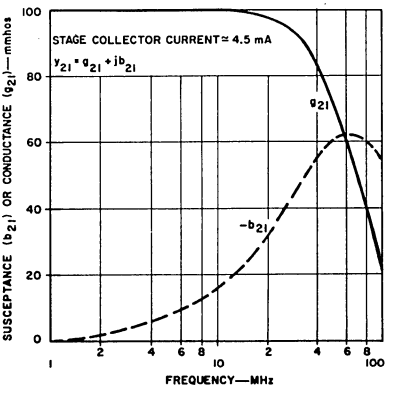




*Fig.4 - Y parameters of the CA3028A and CA3028B in the cascode connection.*

For quick reference, values for input and output parallel RC networks and transconductance values are listed in Table I for the differential amplifier and in Table II for the cascode amplifier.

Although the reverse transfer admittance $y_{12}$ of the CA3028A or CA3028B is low for either cascode or differential operation, circuit-layout-induced instability can occur in high-gain amplifiers. Circuit layout is of paramount importance in both modes because undesirable coupling admittances can be much greater than the CA3028A or CA3028B admittances. Attention to layout and shielding is imperative if proper advantage is to be taken of the low feedback of the CA3028A and CA3028B.

Table I Input and Output Parallel RC Network Component Values, Transconductance Values, and Performance Data for the CA3028A and CA3028B Integrated Circuits in the Differential Amplifier.

| Frequency | Input Parallel RC Network | | Output Parallel RC Network | | Transconductance |
|---|---|---|---|---|---|
| (MHz) | $R_{in}$ (ohms) | $C_{in}$ (pF) | $R_{out}$ (ohms) | $C_{out}$ (pF) | $g_m$ (millimhos) |
| 10.7 | 1800 | 8 | $2.2 \times 10^4$ | 4 | 35 |
| 100 | 500 | 4.5 | $1.8 \times 10^3$ | 4 | 15 |

Table II Input and Output Parallel RC Network Component Values, Transconductance Values, and Performance Data for the CA3028A and CA3028B Integrated Circuit Cascode Amplifier.

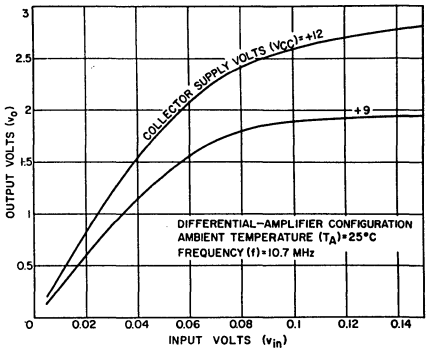
| Frequency | Input Parallel RC Network | | Output Parallel RC Network | | Transconductance |
|---|---|---|---|---|---|
| (MHz) | $R_{in}$ (ohms) | $C_{in}$ (pF) | $R_{out}$ (ohms) | $C_{out}$ (pF) | $g_m$ (millimhos) |
| 10.7 | 900 | 22 | $-1.67 \times 10^6$ | 3.1 | 100 |
| 100 | 170 | 6.3 | $-5 \times 10^5$ | 3.5 | 14 |

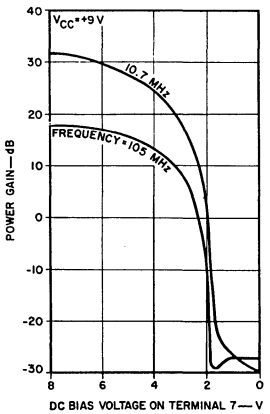
**Differential Amplifier**

The differential amplifier shown in Fig.2(a) is designed for operation at 10.7 MHz and 100 MHz. Because the amplifier consists essentially of a common-collector stage driving a common-base stage, the input admittance $y_{11}$, the output admittance $y_{22}$, and the forward transfer admittance $y_{21}$ are decreased by a factor of two. The reverse transfer admittance $y_{12}$ is typically 140 times lower than that of a single common-emitter transistor at 10.7 MHz, and 10 times lower at 100 MHz. As a result, the CA3028A and CA3028B can be aligned easily in if strips without need for neutralization.

The transfer characteristic in Fig.5(a) shows the excellent limiting capabilities of the CA3028A and CA3028B differential amplifiers. This limiting performance is achieved because the constant-current transistor $Q_3$ limits the circuit operating current so that the collectors of the differential-pair transistors $Q_1$ and $Q_2$ do not saturate. Table III shows the maximum permissible load resistances for non-saturating operation when single supply voltages of 9 and 12 volts are used.

When linear operation over a wide input-voltage range is imperative, agc voltage may be applied to the constant-current source $Q_3$ at terminal 7. Gain-control



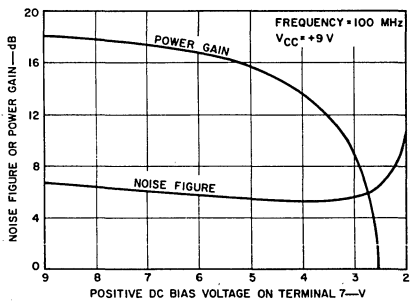




*Fig.5 - Characteristics of the CA3028A and CA3028B in the differential-amplifier connection: (a) 10.7-MHz transfer characteristics; (b) agc capabilities; (c) power gain as a function of noise figure.*

Table III Maximum Load Resistance Permissible for Non-Saturating Operation with +9 and +12 volt Single-Supply Voltages

| $V_{CC}$ (volts) | $I_{C1} + I_{C2}$ (milliamperes) | Maximum Tuned Load (ohms) | Maximum Resistive Load (ohms) |
|---|---|---|---|
| +9 | 5.0 | 3.6 K | 1.8 K |
| +12 | 6.8 | 3.5 K | 1.7 K |

$R_L = V_{CC}/I_{C1} + I_{C2}$ Resistive Load

$R_L = 2\ V_{CC}/I_{C1} + I_{C2}$ Tuned Load

capabilities are -60 dB at 10.7 MHz and -46 dB at 100 MHz, as shown in Fig.5(b). Fig.5(c) shows curves of power gain and noise figure as a function of agc voltage. The combination of an optimum noise figure of 5.5 dB and a power gain of 15 dB at 100 MHz makes this circuit suitable for use as an rf amplifier in the commercial FM band.

### Cascode Amplifier

When the CA3028A or CA3028B is used in the cascode configuration for rf-amplifier circuits, a common-emitter stage drives a common-base stage. The input admittance $y_{11}$ is essentially that of a common-emitter stage, and the forward transfer admittance $y_{21}$ is that of a common-emitter stage times the common-base alpha. Because of the high-impedance drive source for the common-base stage, the output admittance $y_{22}$ is quite low at low frequencies (0.6 $\mu$mho). The reverse transfer admittance $y_{12}$ for the cascode circuit is 900 times less than that for a single-stage common-emitter at 10.7 MHz, and 35 times less at 100 MHz. As in the differential amplifier, ease in tuning is obtained without need for neutralization.

The transfer characteristic in Fig.6 shows the suitability of the cascode configuration for agc take-off for FM front-end controls.

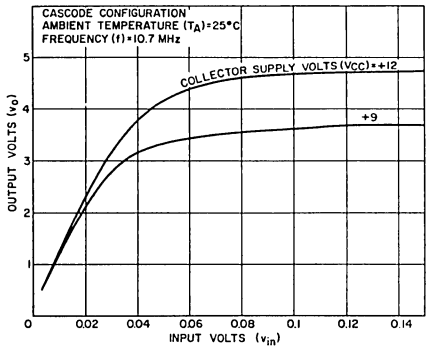



*Fig.6 - 10.7-MHz transfer characteristics of the CA3028A and CA3028B in the cascode connection.*

### Applications

The typical applications described below illustrate the use of the CA3028A and CA3028B integrated-circuit rf amplifiers in both the differential and the cascode modes.

**10.7-MHz Cascode IF Amplifier.** Fig.7 shows an FM if strip in which the CA3028A or CA3028B is used in a high-gain, high-performance cascode configuration in conjunction with a CA3012 integrated-circuit wide-band amplifier. The CA3012 is used in the last stage because of the high gain of 74 dB input to the 4000-ohm-load ratio-detector transformer $T_4$. An input of approximately 400 microvolts is required at the base of the CA3012 for -3 dB below full limiting. An impedance-transfer device and filter must be connected between the CA3012 base (terminal 1) and the output of the CA3028A or CA3028B (terminal 6). The insertion loss of this filter should be kept near 6 dB (1:2 ratio of loaded to unloaded Q) so that all possible gain can be realized up to the CA3012 base. In addition to this insertion loss, a voltage step-down loss of 5.8 dB in the interstage filter is unavoidable. Therefore, the total voltage loss is approximately 9 to 14 dB, and an output of 1500 to 2000 microvolts must be available from the CA3028A or CA3028B to provide the required 400-microvolt input to the CA3012.

The voltage gain of the CA3028A or CA3028B into a 3000-ohm load is determined as follows:

$$VG = \frac{-y_{21}}{y_{22} + y_L} = \frac{100 \times 10^{-3}}{0.33 \times 10^{-3}} = 300 = 49\ dB$$

This calculation indicated a sensitivity of 6.6 microvolts at the CA3028A or CA3028B base (terminal 2). This value cannot be realized, however, because the CA3012 limits on noise peaks so that the gain figure is reduced.

A sensitivity of 7.5 microvolts was realized in the design shown in Fig.7. The filter approach with high-gain integrated-circuit chips differs from that for single, cascaded transistor stages in that lumped selectivity is required rather than distributed selectivity.

Special care must be exercised when second-channel attenuation in the order of 45 dB is required. Selectivity is then proportioned as follows:

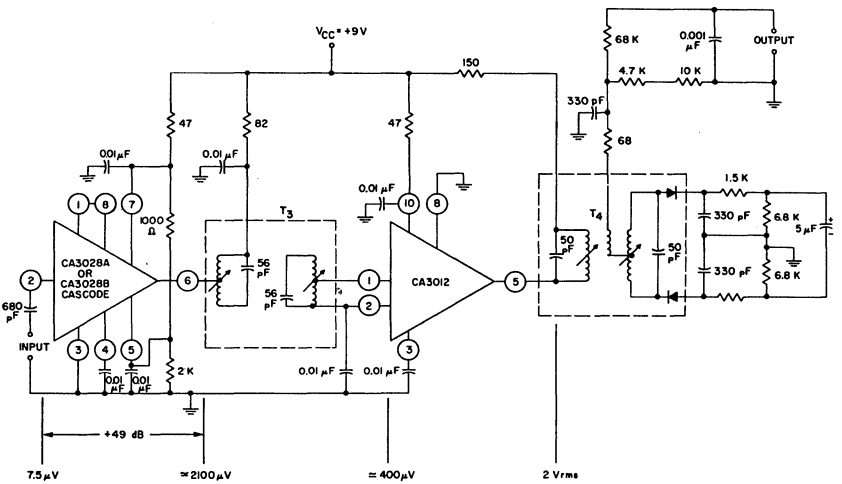
Interstage filter: double-tuned 220 kHz at -3 dB; coefficient of critical coupling, 0.7; voltage loss, 8 dB

Converter filter: triple-tuned, 220 kHz at -3 dB; coefficient of critical coupling, 0.8; voltage loss, about 28 dB

Because of input limiting in the CA3012, the interstage filter exhibits a somewhat wider bandwidth than the 220 kHz indicated. Therefore, a coefficient of critical coupling near 0.8 is realized, which is optimum for minimum deviation from constant time delay. The triple-tuned converter filter alone provides second-channel attenuation of 30 to 33 dB, while the interstage

**10.7-MHz IF Strip Using Two CA3028A or CA3028B Circuits.** The 10.7-MHz if strip shown in Fig.8 uses two CA3028A or CA3028B integrated circuits to provide less over-all gain than the circuit of Fig.7. The first integrated circuit is connected as a cascode amplifier and yields voltage gain of 50 dB; the second integrated circuit is connected as a differential amplifier and yields voltage gain of 42 dB.

When a practical interstage transformer having a voltage insertion loss of 9 dB is used, over-all gain is




$T_3$: Interstage transformer TRW #22486 or equiv.

$T_4$: Ratio detector TRW #22516 or equiv.

Audio Output: 155 mV rms for 7.5 μV ± 75 kHz input 3 dB below knee of transfer characteristic.

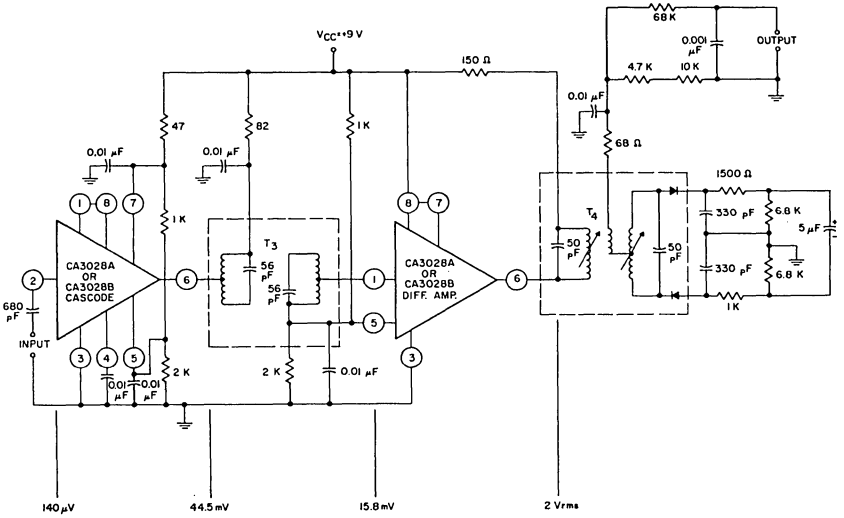
***Fig.7 - 10.7-MHz if amplifier using a CA3028A or CA3028B in the cascode mode.***

filter contributes 8 to 10 dB. The filters described meet requirements of both performance and economy.

The large collector swing that can be obtained in cascode operation of the CA3028A or CA3028B makes it desirable to take the agc voltage from the collector or "hot" end of the if transformer for front-end gain control. The cascode stage then operates primarily in its linear region, and excellent selectivity (40 dB) is maintained even for large signal inputs of approximately 0.4 volt. Front-end gain reduction is between 40 and 50 dB.

83 dB and the sensitivity at the base of the first integrated circuit is 140 microvolts. A less sophisticated converter filter (double-tuned) could be employed at the expense of about 26 dB of second-channel attenuation. If the voltage insertion loss of the converter filter is assumed to be 18 dB and the front-end voltage gain (antenna to mixer collector) is 50 dB, this receiver would have an IHFM* sensitivity of approximately 8 microvolts.

* Institute of High-Fidelity Manufacturers.




$T_3$: Interstage transformer TRW #22486 or equiv.

$T_4$: Ratio detector TRW #22516 or equiv.

Audio Output: 155 mV rms for 140 μV ± 75 kHz input 3 dB below knee of transfer characteristic.

*Fig.8 - 10.7-MHz if strip using two CA3028A or CA3028B integrated circuits.*

**10.7-MHz Differential-Amplifier IF Strip.** Fig.9 shows a 10.7-MHz medium-gain if strip consisting of a CA3028A or CA3028B connected as a differential amplifier and a CA3012 wide-band amplifier. As in the circuit shown in Fig.7, an input of approximately 1500 microvolts is required to the interstage filter. The differential-mode voltage gain of the CA3028A or CA3028B into a 3000-ohm load is determined as follows:

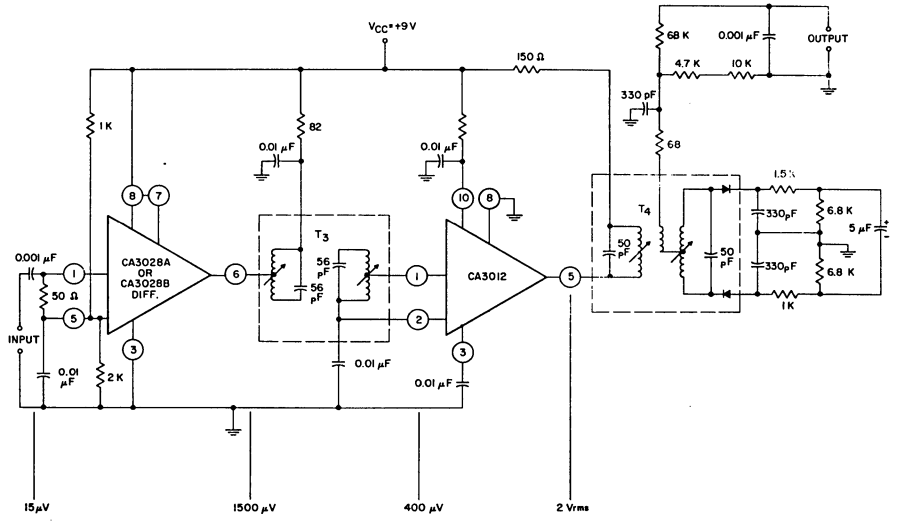
$$VG = \frac{-y_{21}}{y_{22} + y_L} = \frac{35 \times 10^{-3}}{0.38 \times 10^{-3}} = 92.5 = 39.3 \text{ dB}$$

This voltage gain requires that an input of approximately 15 microvolts be available at the base of the CA3028A or CA3028B differential amplifier.

Even if a triple-tuned filter having a voltage insertion loss of 28 dB is used in a low-gain front end, a receiver having an IHFM sensitivity of 5 microvolts results. If 26 dB second-channel attenuation is permissible, a 3-microvolt-sensitivity IHFM receiver can be realized.

**88-MHz-to-108-MHz FM Front End.** Fig.10 illustrates the use of the CA3028A or CA3028B as an rf amplifier and a converter in an 88-to-108-MHz FM front end. For best noise performance, the differential mode is used and the base of the constant-current source $Q_3$ is biased for a power gain of 15 dB. The rf amplifier input circuit is adjusted for an insertion loss of 2 dB to keep the noise figure of the front end low. Because the insertion loss of the input transformer adds directly to the integrated-circuit noise figure of 5.5 dB, the noise figure for the front end alone is 7.5 dB, as compared to noise figures of about 6 dB for commercial FM tuners.

Although a single-tuned circuit is shown between the collector of the rf-amplifier stage and the base of the converter stage, a double-tuned circuit is preferred to reduce spurious response of the converter. If the double-tuned circuit is critically coupled for the same 3-dB bandwidth as the single-tuned circuit, the insertion loss remains the same.




$T_3$: Interstage transformer TRW #22486 or equiv.

$T_4$: Ratio detector TRW #22516 or equiv.

Audio output: 155 mV rms for 15 μV ± 75 kHz input 3 dB below knee of transfer characteristic.

*Fig.9 - 10.7-MHz if strip using a CA3028A or CA3028B in the differential mode.*

The collector of the rf stage is tapped down on the interstage coil at approximately 1500 ohms, and the base of the converter stage at 150 ohms. RF voltage gain is computed as follows:

| | |
|---|---|
| Antenna to base | 0 dB |
| Base to collector | 22 dB |
| Voltage insertion loss of interstage coil | -13 dB |
| Net rf voltage gain | 9 dB |

If an if converter transformer having an impedance of 10,000 ohms is used, the calculated voltage conversion gain is

$$VG_c = \frac{-y21}{y22 + y_L} = 112 = 41.3 \text{ dB}$$

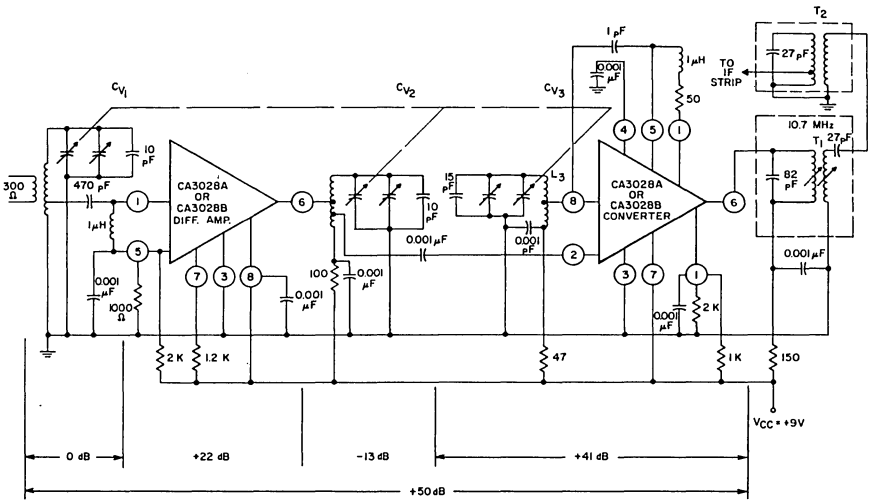
Measured gain into the collector of the converter is 42 dB. The measured voltage gain of the rf amplifier and converter into a 10,000-ohm load is 52 dB; calculated gain is 50 dB. When the converter is tuned for the commercial FM band (88 to 108 MHz), the following parameters apply:

| | | |
|---|---|---|
| Input resistance $R_{in}$ | 170 | ohms |
| Input capacitance $C_{in}$ | 6.3 | pF |
| Output resistance $R_{out}$ | 80K | ohms |
| Output capacitance $C_{out}$ | 3.5 | pF |
| Conversion transconductance | 13 | mmhos |

The rf amplifier and converter shown in Fig.10 were combined with the if amplifier shown in Fig.7, and the following performance data were measured at 100 MHz:

| | |
|---|---|
| 30-dB (S + N)/N IHFM Sensitivity | 3 μV |
| Image Rejection | 46 dB |

Receiver noise figure is the limiting factor that permits a sensitivity of only 3 microvolts to be realized.




$L_1$: 3-3/4 T #18 tinned copper wire; winding length 5/16" on 9/32" form; tapped at 1-3/4 T; primary — 2 turns #30 SE.

$L_2$: 3-3/4 T #18 tinned copper wire; winding length 5/16" on 9/32" form; tapped at 6 2-1/4 T, A 3/4 T.

$C_{V_{1-2}}$: variable $\Delta C \approx 15$ pF

$T_1$: Mixer transformer TRW #22484 or equiv.

$T_2$: Input transformer TRW #22485 or equiv.

$L_3$: 3-1/2 T #18 tinned copper wire; winding length 5/16" on 9/32" form.

$C_{V_{1-3}}$: variable, $\Delta C \approx 15$ pF.

*Fig. 10 - 88-MHz-to-108-MHz FM front end.*

# Application of the RCA CA3021, CA3022, and CA3023 Integrated-Circuit Wideband Amplifiers

BY

G.E. THERIAULT, T. H. CAMPBELL, AND A. J. LEIDICH

The RCA-CA3021, CA3022, and CA3023 integrated circuits are multi-purpose high-gain amplifiers designed for use in video and AM or FM if stages in single-power-supply systems. These circuits feature monolithic-silicon construction, and are usable throughout the temperature range from -55°C to 125°C. They are supplied in a 12-terminal TO-5 package.

The CA3021, CA3022, and CA3023 have the same circuit configuration and the same mid-band open-loop gain. However, different resistor values are used in the three circuits to provide different values of power dissipation and open-loop bandwidth. Typical power dissipation with a 6-volt supply is 3 milliwatts for the CA3021, 12 milliwatts for the CA3022, and 36 milliwatts for the CA3023. Wider bandwidths can be achieved with the CA3023, intermediate bandwidths with the CA3022, and narrower bandwidths with the CA3021.

The major feature of these circuits is a flexibility that permits their use in the following applications: video amplifiers operating at frequencies through 30 MHz, AM and FM if amplifiers, and buffer amplifiers in which an isolation capability greater than 60 dB at 1 MHz is desired. The areas of circuit flexibility are as follows:

- Operation with dc supplies of 4.5 to 12 volts.
- Automatic-gain-control capability (60-dB agc range with large input-signal-handling capability).
- Limiting capability (by connection of diodes provided on the chip).
- Gain adjustment (by addition of external feedback resistor or network to obtain desired operating gain and bandwidth).

## Circuit Description

The circuit diagram for the CA3021, CA3022, and CA3023 is shown in Fig. 1. Amplifier gain is obtained by use of transistors $Q_1$, $Q_3$, $Q_4$, and $Q_6$, which are connected as two dc-coupled common-emitter/common-collector amplifiers having a voltage gain of approximately 60 dB. The

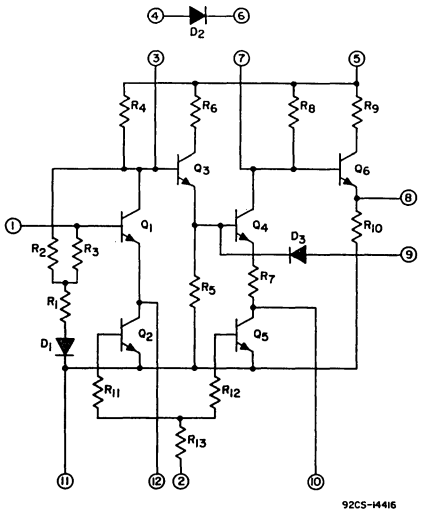



*Fig. 1 - Circuit diagram and TO-5 terminal connections for the CA3021, CA3022, and CA3023 integrated circuits.*

common-collector configuration provides the necessary impedance transformation (high-impedance input and low-impedance output) for wide bandwidth. The output transistor $Q_6$ provides the low output impedance desired for iterative operation. The circuit must be capacitively coupled, and should have a low-impedance source. A source resistance of 50 ohms was used for the circuit measurements given in this Note.

Fig. 2 shows typical connections for the CA3021, CA3022, and CA3023 for wideband and bandpass applications with and without agc, and for limiter applications. An external feedback resistor $R_f$ or a tuned circuit can be added between terminals 3 and 7 for desired bandwidth and gain performance. Linear operating conditions are maintained by the bias applied between the collector and the base of $Q_1$ by the resistor-diode network $R_2$, $R_3$, $R_1$, $D_1$. Because the collector of $Q_1$ is held at a fixed potential that is relatively independent of supply, device characteristics, and temperature, dc coupling to the remainder of the circuit can be used.

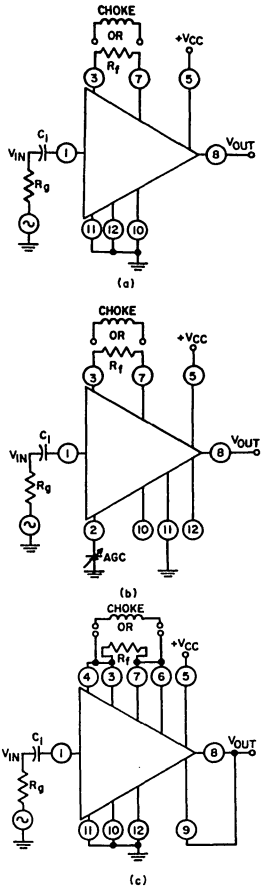



*Fig. 2 - Typical connections for the CA3021, CA3022, and CA3023 for (a) wideband and bandpass applications, (b) wideband and bandpass applications requiring agc, and (c) limiter applications.*

For applications in which gain control is desired, terminals 10 and 12 are left floating and agc is applied to terminal 2, as shown in Fig. 2b. For maximum gain, terminal 2 is operated at a positive voltage not larger than the supply voltage applied to terminal 5. In the positive voltage condition, transistors $Q_2$ and $Q_5$ are saturated and the impedance in the emitters of $Q_1$ and $Q_4$ is low. When the gain-control voltage becomes negative, $Q_2$ and $Q_5$ come out of saturation and provide high degenerative emitter resistance which reduces the gain. Because most of the increasing signals appear across the increasing degenerative resistance, the active gain transistors $Q_1$, $Q_3$, $Q_4$, and $Q_6$ handle only a small part of the large signal. As a result, signal-handling capability increases with increasing agc. Further increases of gain-control voltage reduce the current in $Q_1$ and $Q_4$ and thus provide the additional gain control needed to achieve maximum agc range.

In limiting applications, diodes $D_2$ and $D_3$ are connected in the feedback loops, as shown in Fig. 2c (terminals 4 to 3, 6 to 7, and 8 to 9). The diodes provide clamping for sufficient input-signal swing; limiting can be achieved with input-signal swings up to 2.5 volts rms.

## Operating Characteristics

**DC Supply Considerations.** The most positive voltage to be applied to the CA3021, CA3022, and CA3023 integrated circuits is connected to terminal 5. The most negative voltage is connected to the substrate through terminal 11.

The circuits can be used with single power supplies of 4.5 to 12 volts. The bias technique used for transistor $Q_1$, and thus for the remainder of the circuit, makes the collector operating voltage of $Q_1$ and $Q_4$ relatively independent of the supply. Consequently, the current in the circuit increases almost linearly as a function of supply voltage. Fig. 3 shows typical power dissipation for the three circuits as a function of supply voltage. Because there is little change in the collector voltage of $Q_4$, there is little change in output operating point as a function of supply voltage.

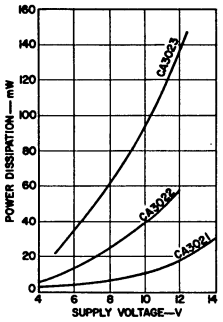



*Fig. 3 - Power dissipation as a function of supply voltage.*

**DC Stability with Temperature.** The output operating points of the CA3021, CA3022, and CA3023 are shown in Fig. 4 as a function of temperature and feedback resistance. As a result of the resistor values used in each circuit, the output operating point is compensated in the temperature range between -20°C and 75°C when the circuit is operated under open-loop conditions (terminals 3 and 7 floating). Insertion of a feedback resistor between terminals 3 and 7 is recommended to minimize degradation in performance at temperatures outside this range. The maximum value of the feedback resistor $R_f$ recommended for optimum performance of each circuit is shown in the following table:

| Circuit | $R_f$ - ohms |
|---|---|
| CA3021 | 18000 |
| CA3022 | 5100 |
| CA3023 | 2000 |

Use of a feedback resistor of the maximum value provides equal ac and dc feedback, but reduces the usable gain of the circuit to approximately 40 dB. When equal ac and dc feedback is not desired, as in the case of bandpass or tuned responses, a choke or tuned circuit can be included between the feedback terminals 3 and 7 to provide dc temperature stability and permit gains of 50 to 55 dB.

As a general rule, feedback should be included in all applications in which operation over an extended temperature range is required.

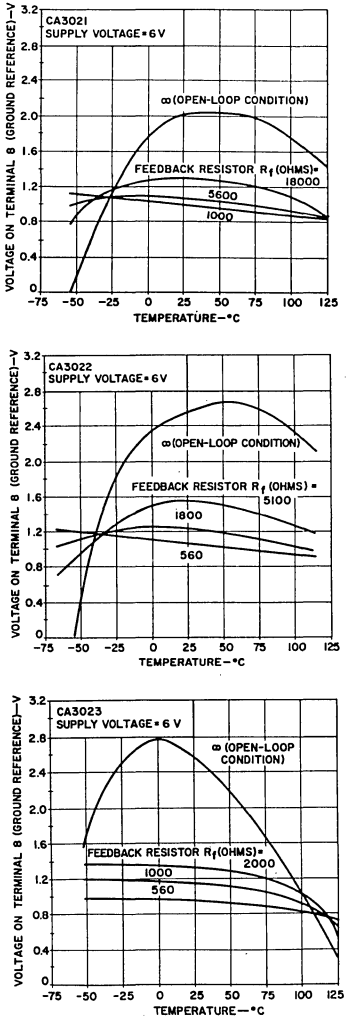


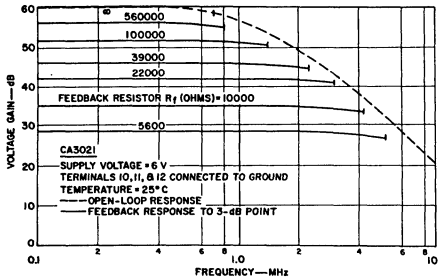

*Fig. 4 - Output operating point as a function of temperature for various values of feedback resistance.*

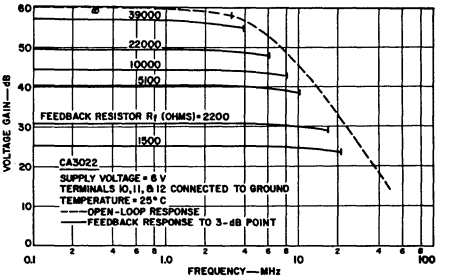
**DC Considerations for Gain Control.** When the agc transistors $Q_2$ and $Q_5$ are included in the circuit, the output operating point can be held constant only by addition of feedback. Variation of operating point is caused by the added collector-to-emitter voltage of $Q_2$ and $Q_5$ in saturation in the emitters of $Q_1$ and $Q_4$. The effect is more pronounced in the higher-current circuits, CA3022 and CA3023. As discussed previously, full dc feedback can be used to stabilize the operating point; ac feedback can be removed by the use of tuned circuits. The maximum recommended values of $R_f$ provide satisfactory stability when the circuit is connected for agc.

**DC Considerations for Limiting.** In limiter applications, diodes $D_2$ and $D_3$ are included in the feedback loops in the circuit (external connections are made as shown in Fig. 2c). Under open-loop conditions, the dc operating point may be such that $D_2$ and $D_3$ (usually $D_3$) are turned on. The gain is then reduced and the amplifier will not operate linearly at low levels. The values of $R_f$ recommended previously also assure correct operation for limiting amplifiers.

**AC Frequency Response and Gain Performance.** Open-loop frequency responses for the CA3021, CA3022, and CA3023 are given in Fig. 5. The curves also show the response characteristics to the 3-dB point for various values of feedback resistance. Values of feedback resistance larger than those recommended for operating-point temperature stability are included to indicate gain performance at resonance when tuned circuits or chokes are used in the feedback loop. For these measurements, the circuits were operated with a 50-ohm source and a high impedance load.

Fig. 6 shows the variation of gain with temperature for the three circuits. Each circuit was operated with sufficient feedback to provide a closed-loop gain of approximately 40 dB. The gain variation is practically independent of feedback, and is slightly greater for the CA3023 than for the other two circuits. Fig. 7 shows typical upper-3-dB frequency shifts with temperature for the three circuits for a gain of approximately 40 dB.



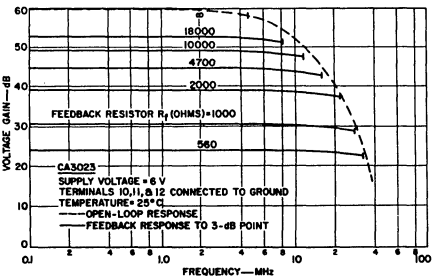




*Fig. 5 - Frequency-response characteristics.*

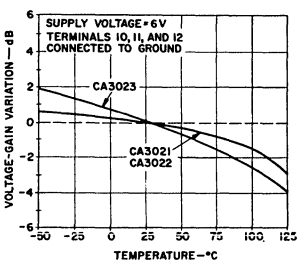



*Fig. 6 - Voltage-gain variation with temperature (feedback adjusted to provide gain of approximately 40 dB at 25°C).*

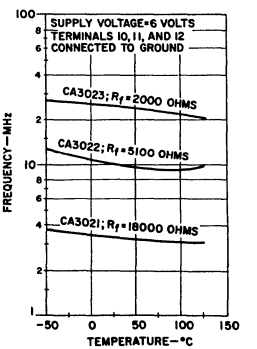



*Fig. 7 - Upper-3-dB frequency shift with temperature.*

In buffer-amplifier applications, reverse feedback or isolation capability is required. The following table shows the isolation performance of the CA3021, CA3022, and CA3023 at three frequency levels with the input terminated in 50 ohms.

| Circuit | Feedback Resistor $R_f$ (ohms) | Voltage Injected at Output (volts rms) | Resultant Feedthrough Input Voltage Below the Applied Output Voltage (dB) | | |
|---|---|---|---|---|---|
| | | | f = 1 MHz | f = 10 MHz | f = 50 MHz |
| CA3021 | 18000 | 2 | 66 | 66 | 54 |
| CA3022 | 5000 | 2 | 66 | 66 | 54 |
| CA3023 | 2000 | 2 | 66 | 66 | 52 |

**AC Signal Power Output.** The maximum power-output capability of the common-collector output transistor $Q_6$ in Fig.1 occurs for a load-resistance value higher than the output impedance. For determination of optimum load-resistor values, each circuit was operated from a 6-volt supply at a gain of approximately 40 dB with a variable resistor capacitively coupled to terminal 8. The variation of maximum linear signal output as a function of load resistance is shown in Fig.8.

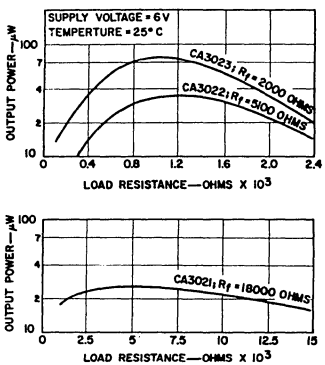



*Fig.8 - Maximum linear signal output as a function of load resistance.*

Maximum power output was measured at a level at which output distortion was just discernible on an oscilloscope.

**Tuned Circuit in the Feedback Loop.** When a parallel tuned circuit is included in the feedback path between terminals 3 and 7 of the CA3021, CA3022, or CA3023, the gain at resonance is a function of the equivalent resistance of the feedback loop. Gain characteristics of the three circuits as a function of feedback resistance are shown in Fig.9. For each circuit, there is a value of feedback

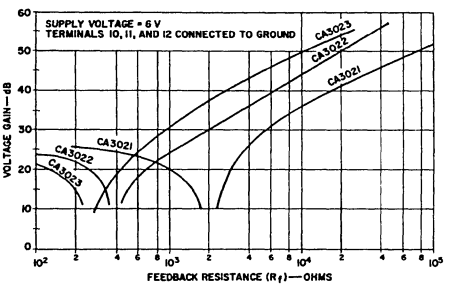



*Fig.9 - Voltage gain as a function of feedback resistance.*

resistance $R_f$ for which the gain approaches zero. This condition occurs when the small-signal transconductance $g_m$ of the transistor $Q_4$ is equal to the conductance of the parallel tuned circuit; signal cancellation then results at terminal 7. In a tuned circuit designed with the correct feedback resistance $R_f$, therefore, zero gain can be obtained at the resonant frequency. The resistance values required for signal cancellation are 2000 ohms for the CA3021, 400 ohms for the CA3022, and 230 ohms for the CA3023. When the tuned-circuit impedance is made equal to these cancellation resistance values at resonance, the gain increases

at frequencies off resonance and a trapping effect results. For zero feedback resistance, the gain of each circuit is approximately 24 dB. For values of feedback resistance in excess of the cancellation resistance, the gain increases. When the tuned circuit has a resonant impedance higher than the cancellation resistance, the response is added to the video response characteristic, as shown in Fig. 10. Then, because no

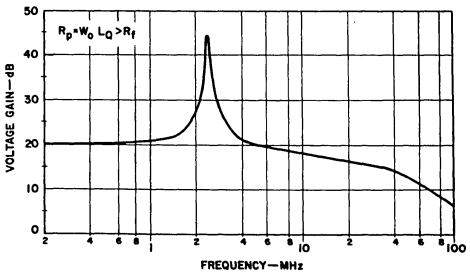



*Fig. 10 - Voltage gain as a function of frequency in a bandpass amplifier when the tuned-circuit resonant impedance $R_p$ is higher than the cancellation resistance $R_{fc}$.*

purely resistive value occurs that is equal to the cancellation resistance, no cancellation occurs.

The bandwidth of the response can be approximated by determining the total loading of $R_p$ on the parallel tuned circuit in the feedback path, as follows:

$$R_p = \frac{R_T R_X (R_4+R_8)}{(R_X+R_T)(R_4+R_8)+R_X R_T}$$

where $R_T$ is the resistance at resonance of the unloaded Q, $R_X$ is the resistance added to the tuned circuit for adjustment of gain, and $(R_4 + R_8)$ is the series combination of the two common-collector load resistors. The 3-dB bandwidth for the response is given by

$$\frac{f_o}{\Delta f} = \frac{R_P}{X_L} = \frac{R_P}{X_C} = Q_L$$

Typical values for $(R_4 + R_8)$ for the three circuits are 39000 ohms for the CA3021, 10900 ohms for the CA3022, and 4800 ohms for the CA3023.

**Output Tuned Circuits.** The curves of Fig. 8 indicate that capacitive coupling of the common-collector output transistor $Q_6$ to a matched load severely limits the transistor output-voltage-swing capability. If the required mismatch is achieved by ac coupling of a tuned circuit directly across the output, the tuned circuit will be loaded by the low output impedance of the common-collector transistor. However, comparable output power can be obtained by use of a resistor in series with the circuit output and the tuned circuit. This arrangement provides a load for the common-collector transistor for frequencies off resonance of the tuned circuit, and prevents the possibility of reactive loads causing emitter-follower transistor instability.

**Gain Control.** The CA3021, CA3022, and CA3023 are connected as shown in Fig. 2b when gain-control application is desired. Transistors $Q_2$ and $Q_5$ are then included in the emitter-signal path of transistors $Q_1$ and $Q_4$, respectively. For maximum gain, a positive voltage is applied to terminal 2 which saturates transistors $Q_2$ and $Q_5$. If a voltage of 6 volts is applied to terminal 2, the typical gain-control current is 0.8 milliampere. The gain-control action is provided by reduction of the voltage on terminal 2. The decreasing voltage causes transistors $Q_2$ and $Q_5$ to come out of saturation and present a high impedance in the emitter leads of transistors $Q_1$ and $Q_4$. It is important that good filtering and isolation be maintained at the agc terminal 2 because transistors $Q_2$ and $Q_5$ are in the linear active region for a portion of the agc range and can, therefore, provide gain for a signal on the agc terminal.

The minimum gain is determined by a combination of the gain of $Q_1$ and feedthrough to the collector of $Q_1$ along a resistance path made up of $R_3$ and $R_2$. Because the signals are out of phase, there is a point at which cancellation of signal results. This cancellation occurs in all three circuits when terminal 2 is 0.5 volt more negative than terminal 11.

It is accompanied by severe distortion of signal and AM modulation. Techniques for obtaining agc without reaching the cancellation point are discussed later.

When the maximum recommended feedback resistance for operating-point stability is used in the connection of Fig. 2b, maximum gain is reduced because of the extra emitter resistance presented by the saturation resistance of transistors $Q_2$ and $Q_5$. Maximum voltage gain for each circuit is approximately 30 dB with the maximum recommended feedback resistance and a 6-volt supply. The typical agc range for each circuit is 55 dB with resistive feedback.

When a tuned circuit is used in the feedback loop, higher maximum gain can be obtained in the agc connection shown in Fig. 2b. The maximum gain obtainable is approximately 50 dB when high feedback impedance is maintained. A self-resonant choke is a convenient element to add in the feedback loop to obtain high impedance because it provides wide bandwidth; resistance loading can be added to adjust the gain to the desired value. When a combination of self-resonant choke and added resistance is used, dc feedback is complete and the operating point is temperature-stable. Wide-bandwidth tuned circuits are suggested for all three circuits, but especially for the CA3022 and CA3023 because the bandwidth shifts with gain control, as shown in Fig. 11. For a tuned frequency of 3 MHz at full gain,

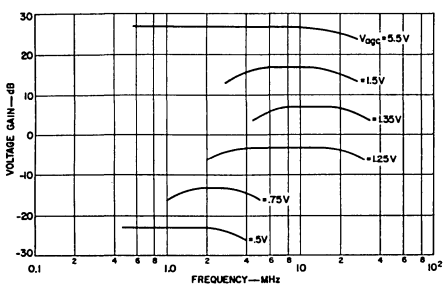



*Fig. 11 - Effect of gain control on response characteristics.*

for example, the resonance point of the tuned response increases slightly (about 5 per cent) for gain control of -20 to -30 dB because of the combination of the low-frequency roll-off and the tuned response. In the region of gain control of -50 dB, the high-frequency roll-off affects the response and the resonant frequency decreases below 3 MHz (by about 10 per cent). At full agc the tuned circuit becomes a trap in the feedthrough path, minimum gain is achieved at the 3-MHz frequency, and the response is inverted, i.e., a notch occurs where a bandpass had existed. When tuned circuits are included in the feedback path of the gain-controlled amplifier, therefore, it is recommended that the bandwidth be chosen as wide as possible to minimize detuning effects. Desired bandwidth control should be obtained at the input, at the output, or in the feedback path of stages without gain control.

The use of emitter degeneration as a gain-control technique improves signal-handling capability. At full gain control, signals as high as 2 volts rms can be handled without the occurrence of serious overload distortion. Typical cross-modulation characteristics for the CA3021, CA3022, and CA3023 with only feedback resistance in the feedback loop are shown in Fig. 12. Maximum gain for each circuit

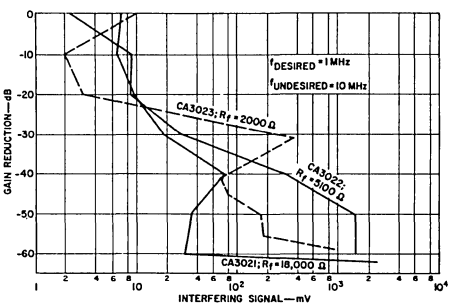



*Fig. 12 - Cross-modulation distortion characteristics.*

was approximately 30 dB. When a tuned circuit is used in the feedback loop, more gain-control range is available as a result of the feedthrough reduction. Depending on the impedance of the tuned circuit, the gain-control range is between 60 and 80 dB. The cross-modulation characteristics when tuned circuits are

used are similar to those obtained with resistive feedback except for modifications caused by different feedback characteristics of interfering signals outside the tuned-circuit passband.

**Limiting.** For applications in which signal limiting is required, the diodes of the CA3021, CA3022, and CA3023 are connected as shown in Fig.2c. At low signal levels, the diodes are cut off and the gain performance is similar to that described previously except for some bandwidth reduction caused by the inherent capacitance of the diodes. For large input-signal swings in the negative direction, the collector of transistor $Q_1$ becomes positive and the collector of transistor $Q_4$ becomes negative, and diode $D_2$ begins to conduct. This action clamps the collector of $Q_1$ to the collector of $Q_4$ and, because the diode is in the feedback path, reduces the gain. For positive swings at the input, the collector of transistor $Q_1$ becomes negative and the output at terminal 8 becomes positive. Two effects tend to limit input signals of positive polarity: transistor $Q_4$ going to cutoff, and diode $D_3$ going into conduction. When the circuits are connected as shown in Fig.2c, limiting is symmetrical at the onset. With increased signal, however, the symmetry is not perfectly preserved because of dc shift in the circuit. Typical output-signal characteristics as a function of input level are shown in Fig.13. The lack of symmetry at high input levels causes a decrease in power output, as shown in the waveforms.

Limiting characteristics for the CA3021, CA3022, and CA3023 were measured in the circuit configurations shown in Fig.14. The output tuned circuit was designed to provide filtering for the desired output frequency so that rms values of output voltage could be obtained. Limiting characteristics were measured for two types of feedback, resistive and tuned circuit; results are shown in Fig.15. When a resonant circuit is used in the feedback loop, the gain of the circuits is higher and limiting occurs at a lower input level. The effects of multistage limiting are described later.

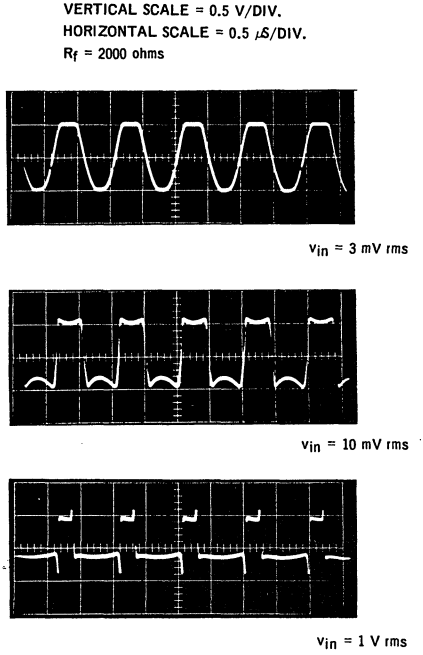
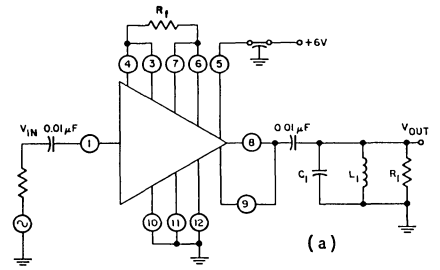
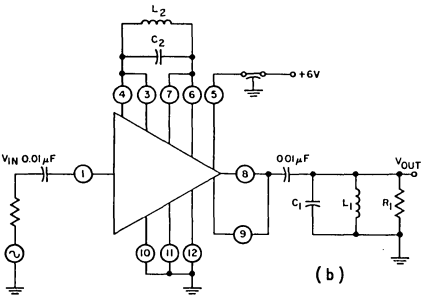



*Fig.13 - Output waveforms obtained in a limiter application.*

**Noise Performance.** The table below shows typical noise figures for the CA3021, CA3022, and CA3023 circuits for a frequency of 1 MHz, a supply voltage of 6 volts, and a source resistance of 50 ohms. The data in the first column of noise figures were measured in the connection shown in Fig.2a; the second column shows data measured in the connection shown in Fig.2b.

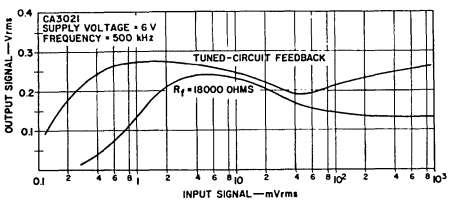
| | Noise Figure — dB | |
|---|---|---|
| Circuit | Term.10,11,12 connected to ground; gain = 40 dB | AGC operating, noise measured for maximum gain of 30 dB |
| CA3021 | 5.8 | 7.5 |
| CA3022 | 7.1 | 8.7 |
| CA3023 | 7.2 | 8.7 |

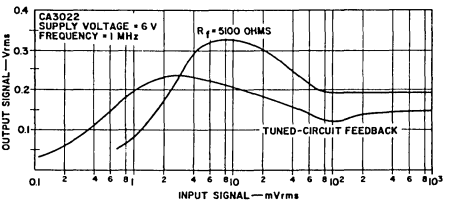



| TYPE | FREQ. (MHz) | $C_1$ (pF) | $L_1$ (μH) | $R_1$ (kΩ) | CIRCUIT(a) $R_F$ (kΩ) | CIRCUIT(b) $L_2$ (mH) | CIRCUIT(b) $C_2$ (pF) |
|---|---|---|---|---|---|---|---|
| CA3021 | 0.5 | 2000 | 36-64 | 8.2 | 18 | 10 | - |
| CA3022 | 1 | 5000 | 3-5 | 1 | 5.1 | 1.2 | 4-45 |
| CA3023 | 5 | 600 | 1.8 | 1 | 2 | - | - |

*Fig. 14 - Circuits used for evaluation of limiting characteristics.*



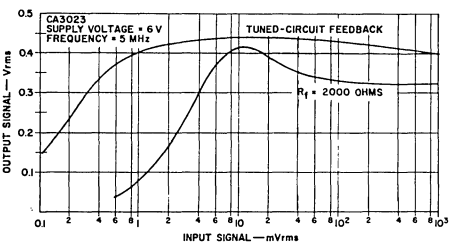




*Fig. 15 - Limiting characteristics.*

## Applications

**Video Amplifiers.** The use of single CA3021, CA3022, or CA3023 integrated circuits in video applications was discussed previously. For an evaluation of iterative video performance, two CA3022 circuits were operated in cascade. Each circuit employed 0.01-microfarad coupling capacitors and feedback resistors of 2000 ohms. Performance data can be summarized as follows:

| | | |
|---|---|---|
| Supply voltage | 6 | volts |
| Supply current | 4.5 | mA |
| Power dissipation | 27 | mW |
| Voltage gain | 61 | dB |
| Maximum undistorted output with 510-ohm load | 0.25 | Vrms |
| Signal level for 3-dB signal-to noise ratio | 11 | μV |
| Dynamic range (input-output linearity) | 27 | dB |
| Bandwidth, 3-dB points: | | |
| upper frequency | 10.5 | MHz |
| lower frequency | 50 | kHz |

10-MHz IF Amplifier. Fig.16 shows a 10-MHz amplifier employing two CA3023 circuits. The first stage is operated in a broadband mode with a 2000-ohm feedback resistor between terminals 3 and 7, in accordance with the design rules described previously. The second stage is a tuned if amplifier. Because the sinusoidal output capability of the CA3023 at 10-MHz is in the 200-millivolt range, it is necessary to step up the voltage to drive the envelope detector; therefore, a tuned transformer that has a 1-to-4 turns ratio is used at the second-stage output. The total effective circuit Q for this if configuration is 200, and the full rf voltage gain is 86 dB from the input of the first stage to the output of the step-up transformer.

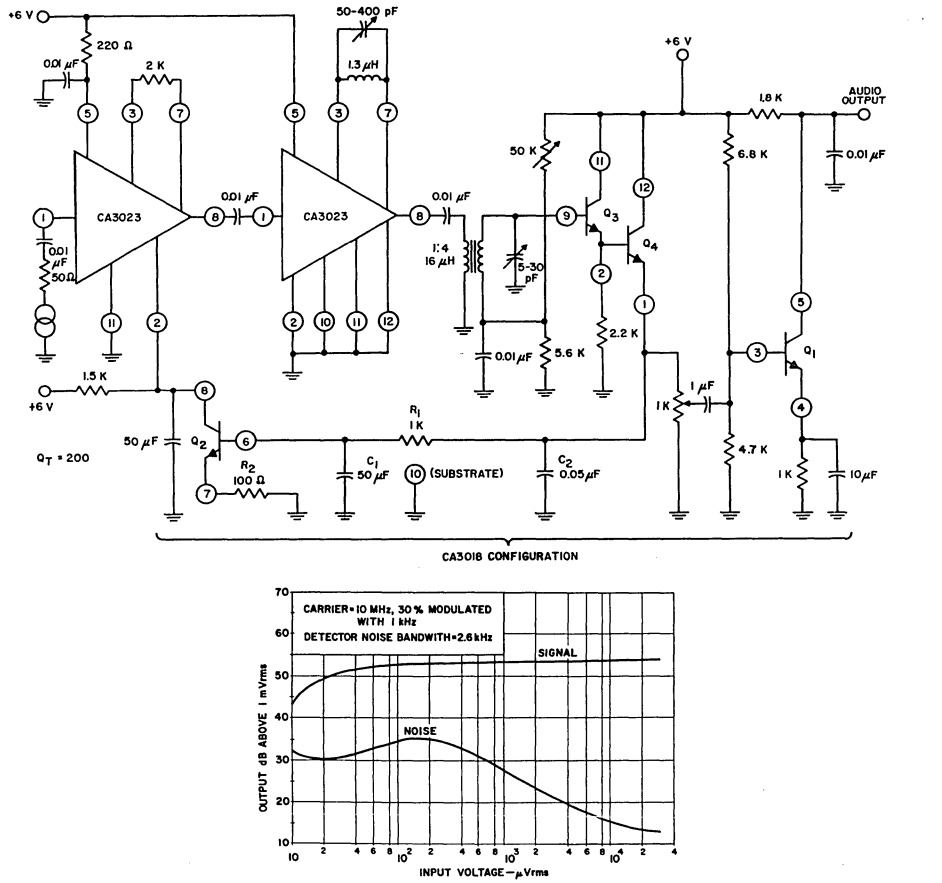



*Fig.16 - Schematic diagram and performance curves for 10-MHz if amplifier using two CA3023 circuits.*

A CA3018 integrated-circuit transistor array is used to provide detection, audio amplification, and dc amplification. Detection is provided by transistors $Q_3$ and $Q_4$ of the CA3018; the detected output is passed through a low-pass filter ($C_1$, $C_2$, and $R_1$) and applied to the agc amplifier transistor $Q_2$. Transistor $Q_2$ goes from cutoff to saturation with increasing signal. The voltage drop across a 100-ohm degenerative resistor $R_2$ prevents the gain-control voltage in terminal 2 of the first CA3023 amplifier from decreasing below 0.5 volt and causing signal cancellation. Transistor $Q_1$ of the CA3018 provides audio gain and is biased in a conventional manner. Fig. 16 also shows the output-signal and noise characteristics of the circuit as functions of rf input level for an input signal that is 30-percent modulated by a 1-kHz sine wave. The audio-output equivalent-noise bandwidth is 2.6 kHz.

**455-kHz IF Amplifier.** Fig. 17 shows a 455-kHz two-stage if amplifier using

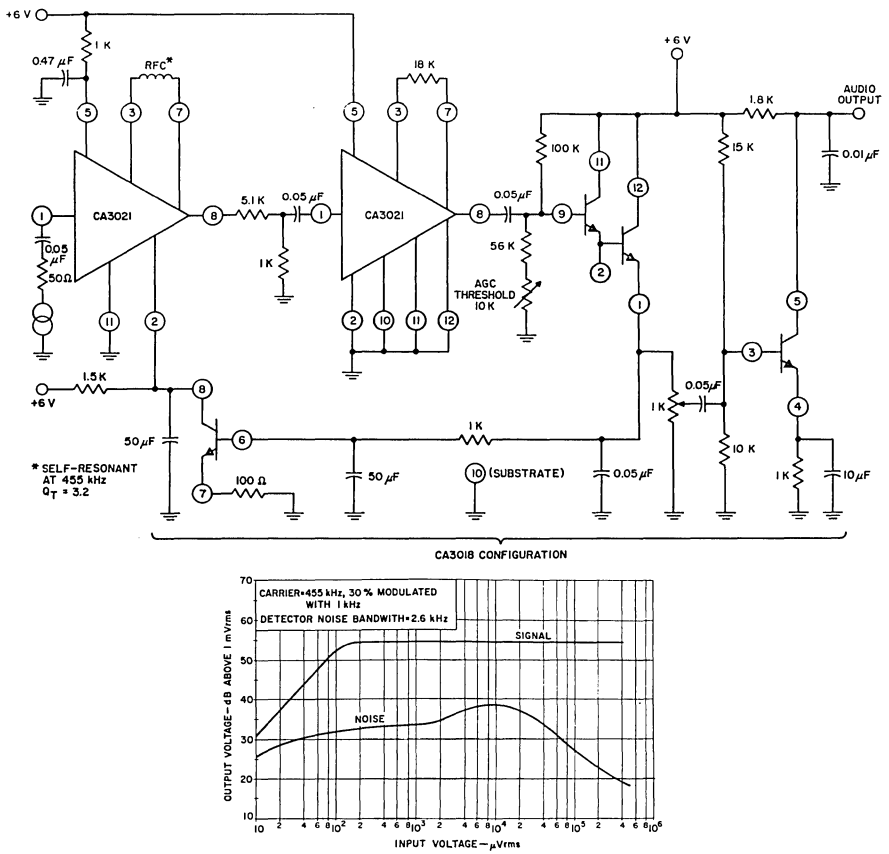






*Fig. 17 - Schematic diagram and performance curves for 455-kHz if amplifier using two CA3021 circuits.*

the CA3021. The tuned-circuit approach discussed previously is used in the first stage. The rf feedback choke is self-resonant at 455 kHz and has a Q of 3.2 in the circuit. The second stage is a video amplifier. Input filtering would normally be provided to obtain the desired if response. For the particular choice of stage gain and agc loop gain, an inter-stage pad network is used to maintain stability and achieve an acceptable signal-to-noise ratio with gain control. The CA3018 output configuration is essentially the same as that used in the circuit of Fig.16. The signal and noise characteristics of the 455-kHz amplifier are also shown in Fig.17 for the same conditions used for the 10-MHz amplifier.

**28-MHz Two-Stage Limiter Amplifier.** Fig.18 shows the circuit diagram of a 28-MHz two-stage limiter amplifier using two CA3023 integrated circuits. Terminals 3 and 7 are connected to terminals 4 and 6, respectively; terminal 8 is connected to terminal 9 to provide limiting action. A self-resonant coil in parallel with a 2000-ohm resistor is inserted in the feedback loop of each amplifier to provide gain and stability. The bandwidth of the system before limiting is 3.8 MHz, and the effective Q is 7.35. The total gain is 61 dB (30.5 dB per stage), and the power dissipation is 66 milliwatts. Fig.18 also shows the limiting performance of the system. Full limiting occurs at an input of 300 microvolts.

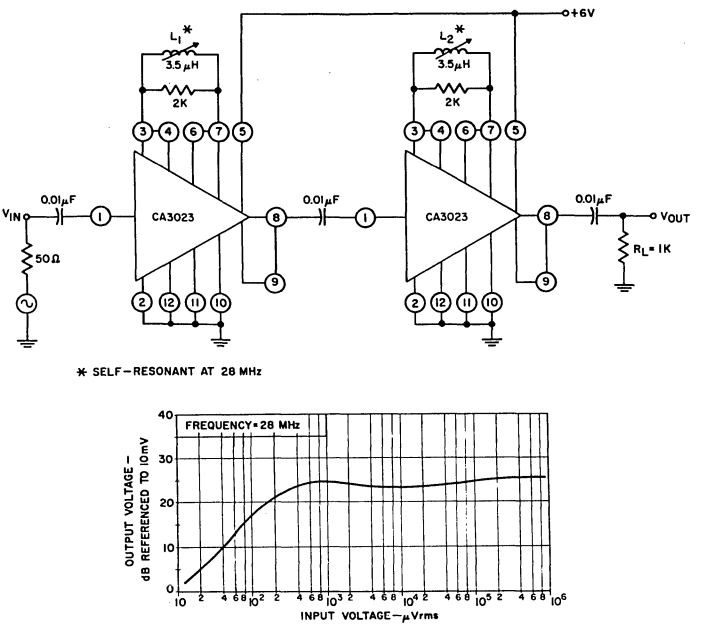



*Fig.18 - Schematic diagram and limiting performance of two-stage 28-MHz limiter amplifier using the CA3023.*

**500-kHz Limiting Amplifier.** Fig.19 shows the circuit diagram of a 500-kHz limiting amplifier using two CA3021 circuits. Two 500-kHz self-resonant chokes are used in the feedback path. A tuned circuit is included in the output to obtain a sine-wave output. The limiting characteristics of this amplifier are also shown. Although limiting occurs for noise, a limited signal is apparent above the noise at an input signal of 1 microvolt. Because of the noise and early limiting, voltage gain can only be estimated; however, it is at least 100 dB. Good limiting performance was obtained for input signals up to 3 volts rms. Total power drain for the circuit with a 6-volt supply was approximately 6 milliwatts.

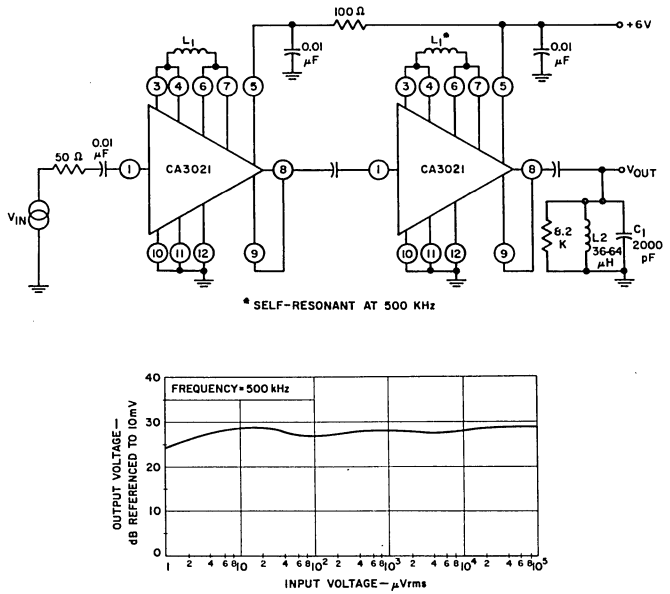



*Fig. 19 - Schematic diagram and limiting performance of two-stage 500-kHz limiter amplifier using the CA3021.*

# Integrated-Circuit Frequency-Modulation IF Amplifiers

by

H.C. Kiehn and R.L. Sanquini

Silicon monolithic integrated circuits that use a differential-amplifier configuration have certain design features which make them more attractive than discrete-component circuits for FM if-amplifier applications. These features include better performance, small size, light weight, and more potential circuit functions per dollar of cost.

### The Differential Amplifier

The heart of integrated-circuit FM if amplifiers is the differential amplifier, which is probably the best simple configuration available today for symmetrical limiting over a wide input-voltage range. Each half of the differential amplifier is alternately cut off on positive and negative half-cycles of the input signal.

As shown in Fig.1, the total current through the circuit $I_T$ is relatively constant. A current equal to $I_T/2$ flows through each transistor at balance (quiescent condition). When the base voltage $V_{B1}$ is made

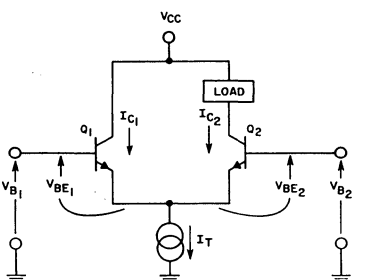



*Fig.1 - Basic differential-amplifier configuration.*

This material was presented at the IEEE Second Annual Semiconductor-Device Clinic on Linear Integrated Circuits in New York City, March 24, 1967.

more positive than $V_{B2}$, however, the collector current $I_{C1}$ increases and $I_{C2}$ decreases. The value of $I_{C1}$ becomes equal to the total current $I_T$ when the following condition exists:

$$V_{B1} - V_{B2} - V_{BE1} \geq V_{BE2} \text{ (threshold)}$$

The transistor $Q_1$ is then full on, and $Q_2$ is then cut off. Similarly, when $V_{B1}$ is made more negative than $V_{B2}$, the value of $I_{C2}$ becomes equal to $I_T$; $Q_1$ is then cut off and $Q_2$ is full on. When the worst-case value of $I_T$ is known, the maximum load impedance for symmetrical limiting is selected so that collector saturation does not occur, as follows:

$$\text{Resistive Load: } R_L = V_{CC}/I_T$$

$$\text{Tuned Load: } R_L = 2\,V_{CC}/I_T$$

Under these conditions, symmetrical limiting is obtained without spurious phase modulation.

The transfer characteristics for a typical differential amplifier shown in Fig.2 illustrate the excellent

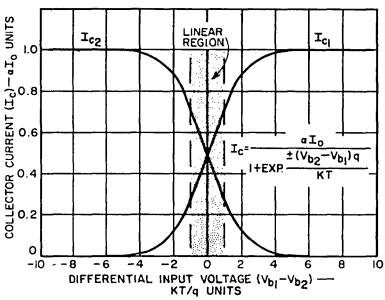



*Fig.2 - Transfer characteristics of basic differential-amplifier circuit.*

limiting characteristics. Further increases in input voltage ($V_{B1} - V_{B2}$) produce no change in collector current above 4KT/q units of input signal.

There are two basic approaches to the design of integrated-circuit FM if-amplifier stages using differential amplifiers: (1) lumped-filter FM if amplifiers using high-gain multi-stage integrated-circuit packages, or (2) individually tuned FM if amplifiers using single-stage integrated-circuit packages. This paper discusses the performance obtained with these approaches and outlines their merits and limitations.

### Evolution of High-Gain Selective Building Blocks

The tuned rf amplifiers used in early broadcast receivers soon exhibited a point of diminishing returns with regard to gain and selectivity improvements. With the advent of the superheterodyne principle, the intermediate-frequency amplifier became the first building block that had fixed-frequency tuning, relatively high gain, and good selectivity as a result of its operation at a frequency lower than the signal frequency.

Because of its demands for high gain, phase linear amplification, and good symmetrical amplitude limiting, and because of the numerous FCC station allocations, FM broadcasting is now facing the dilemma of providing selectivity with good phase response. That is, receiver selectivity must be maintained for large signal inputs without deterioration of phase response. (A discussion of the practical solution of this problem is beyond the scope of this paper.) Successive limiting from the last stage back to the first stage can no longer be tolerated.

### High-Gain-Per-Package Differential Integrated-Circuit IF Strips

Fig.3 shows the schematic diagram of a high-gain integrated circuit, the CA3012, which can be used in an if-amplifier strip to drive a ratio detector. The CA3012 wideband amplifier, designed for use in FM broadcast or communications receivers, is basically an if amplifier-limiter intended for use with external FM detectors. It consists of three direct-coupled cascaded differential-amplifier stages and a built-in regulated power supply. Each of the first two stages consists of an emitter-coupled amplifier and an emitter-follower. The operating conditions are selected so that the dc voltage at the

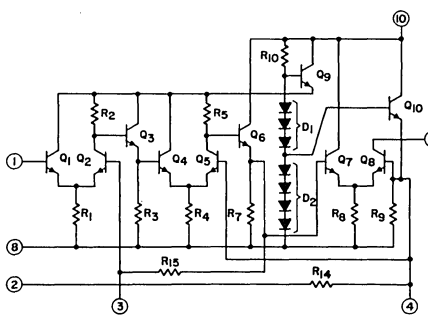



*Fig.3 - Schematic diagram of CA3012 integrated-circuit wideband amplifier.*

output of each stage is identical to that at the input of the stage. This condition is achieved by operation of the bases of the emitter-coupled differential pair of transistors at one-half the supply voltage and selection of the value of the common-emitter load resistor to be one-half that of the collector load resistor. As a result,

the voltage drops across the emitter and collector load resistors are equal, and the collector of the emitter-coupled stage operates at a voltage equal to the base-to-emitter voltage $V_{BE}$ plus the common base potential. The potential at the output of the emitter-follower, therefore, is the same as the common base potential.

At an operating point 3 dB down from the knee of the transfer curve, therefore, the CA3012 requires an input between 400 and 600 microvolts, depending on the ratio-detector design. Fig.4 shows the use of two CA3012 units in a 10.7-MHz if-amplifier strip. A double-tuned filter that has a voltage insertion loss of 8 dB is located between the two CA3012 units to provide a filter input of approximately 1000 microvolts (at terminal 5 of the first CA3012). For an if-strip sensitivity of 4 microvolts, a gain of 48 dB is required. However, if the CA3012 used has a load impedance of 1200 ohms, the available gain is 65 dB, or approximately 17 dB more than required. The extra gain is not wasted, but drives the second CA3012 harder, causing it to limit so that its gain is reduced by approximately 17 dB.

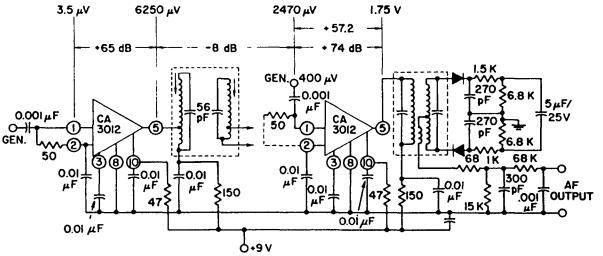



*Fig.4 - 10.7-MHz if-amplifier strip using CA3012 integrated circuit.*

Fig.5 shows the selectivity of the double-tuned interstage filter. The 3-dB bandwidth is 200 kHz at an input of 10 microvolts and 240 kHz at inputs from 500 microvolts to 0.5 volt. The coefficient of critical coupling is approximately 0.5 at 10 microvolts and increases to 1.0 but still maintains good phase response. The double-tuned filter should be coupled capacitance-aiding to avoid a nearly in-phase over-all relationship. Otherwise, bypassing of terminal 10 and the ratio-detector primary becomes critical and over-all stability is impaired.

The connection of the FM front end to the integrated-circuit if strip must provide good selectivity and good phase response. A double-tuned filter is not suitable from the standpoint of selectivity. An actual IHFM* receiver selectivity between 35 and 40 dB is practical and does not impose too much burden on alignment. Because IHFM selectivity includes other factors than passband, a combined filter design that provides second-channel attenuation between 52 and 60 dB becomes imperative.

Investigation of various types of inductance-capacitance filters indicates the use of a triple-tuned type to form the major lumped selectivity of the FM receiver. Fig.6 shows the response curve and two configurations for such a filter. Economy and ease of alignment are the major features in this approach.

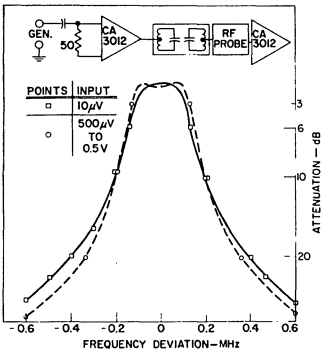



*Fig.5 - Selectivity curve for double-tuned interstage filter.*

The triple-tuned filter, which is located between the mixer and the first integrated circuit, may have a voltage insertion loss of 33 dB, depending on the desired gain distribution. The power insertion loss of the filter, which is between 12 and 17 dB, is the loss that contributes to if noise. If the primary impedance is reduced to provide a lower voltage insertion loss, the front-end gain is decreased by a corresponding amount. Stability criteria must be the deciding factor in impedance and gain distribution.

* Institute of High-Fidelity Manufacturers.

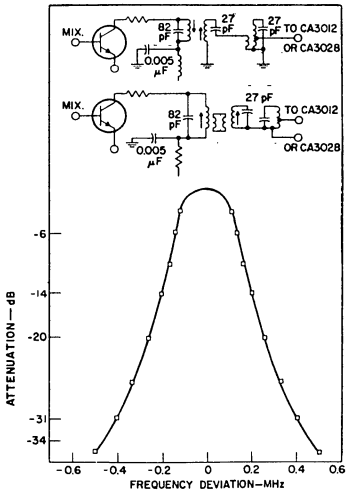



*Fig.6 - Configurations and response curve for triple-tuned interstage filter.*

Most FM front ends come equipped with a double-tuned 10.7-MHz if transformer in which a secondary high-impedance winding is brought out capacitively unterminated and non-polarized with respect to ground. This configuration does not lend itself readily to optimum skirt selectivity (form factor) when connected with an additional single-tuned transformer to form a triple-tuned filter. Most effective use of the existing front-end filter is accomplished by the addition of another double-tuned filter, such as those shown in Fig.7. Either

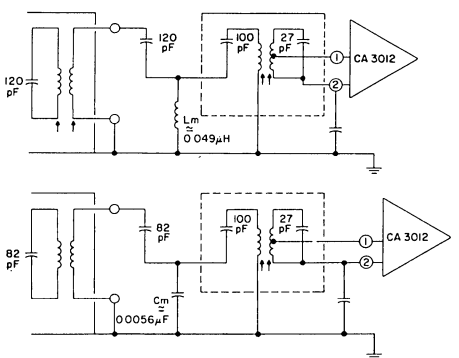



*Fig.7 - Configurations of two quadruple-tuned interstage filters.*

bottom inductance or capacitance coupling can be used. Voltage insertion losses from 18 dB to 26 dB can be expected. Fig.8 shows the response curve obtained

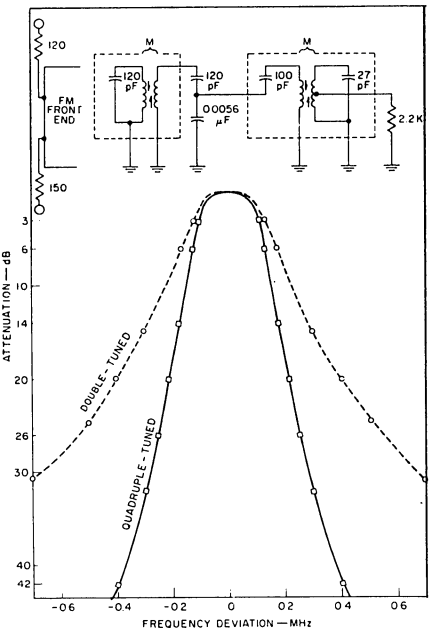



*Fig.8 - Response curve obtained with quadruple-tuned filter.*

with a quadruple-tuned interstage filter. The per-cent coupling between filters and the coupling mode must be determined on the basis of over-all stability and performance.

It may be appropriate to consider briefly the noise associated with high-insertion-loss filters. Over-all receiver noise F is calculated as follows:

$$F = F_1 + \frac{F_2-1}{G_1} + \frac{F_3-1}{G_1G_2}$$

where $F_1$, $F_2$, and $F_3$ are the noise figures of the first (rf), second (mixer), and third (if) stages, respectively; and $G_1$ and $G_2$ are the power gains of the first and second stages. If a value of 27 dB is assumed for the if noise figure $F_3$ (filter plus integrated circuit), 10 dB for the mixer noise figure, and 30 dB for mixer power gain, the effect of if noise on mixer noise is determined as follows:

$$F_2' = F_2 + \frac{F_3-1}{G_2} = 10 + \frac{27-1}{30} = 10.87 \text{ dB}$$

If the rf stage is assumed to have a power gain of 15 dB and a noise figure of 5 dB, total receiver noise is then determined as follows:

$$F = F_1 + \frac{F_2 - 1}{G_1} = 5 + \frac{10.87 - 1}{15} = 5.66 \text{ dB}$$

These calculations show that the power gain of the rf-amplifier stage overrides both if noise and mixer noise. A minimum power gain of 10 dB is advisable.

The use of a tuning capacitance of 82 picofarads in the collector circuit of the mixer stage provides a loaded primary impedance of approximately 10,000 ohms and eliminates the need for a tap. The 27-picofarad tuning capacitances that comprise the other poles of this filter could be reduced to obtain more favorable loaded-to-unloaded-Q ratios without use of additional resistor loading. The choice of 27 picofarads was based primarily on circuit stability considerations.

Fig.9 shows one type of complete integrated-circuit if strip, and Fig.10 shows the accompanying voltage gains and impedances. Values are given for two levels of mixer output impedance. All other impedance levels shown have exhibited good stability. Over-all performance of the circuit is illustrated in Fig.11.

Capture ratio, which was measured at various levels, varies from 5 dB at 2 microvolts to 1.2 dB above 500 microvolts. With careful adjustment, values as low as 0.8 dB can be obtained. The selectivity curve for the integrated circuit if strip is shown in Fig.12. Over-all selectivity for a given ratio detector and the if strip is shown in Fig.13. Some distributed-selectivity receivers have very little second-channel selectivity at an antenna input of 2000 microvolts. The points marked in Fig.13 show such selectivity for several antenna input levels.

Fig.14 shows an if strip that combines high gain per package and the single-stage-per-package approach. CA3012 and CA3028 integrated circuits are used in a differential-mode connection. An if sensitivity of 15 microvolts can be obtained with this if strip.

If discrete circuits are directly replaced by single differential integrated-circuit amplifiers, a minimum of if transformer and printed-circuit-board redesign is required. Values of voltage gain and impedance are indicated on the block diagram in Fig.15. All three double-tuned transformers are made symmetrical with respect to primary and secondary windings and taps.

Because the single- or double-tuned circuit used between the mixer and the if strip has inherently less

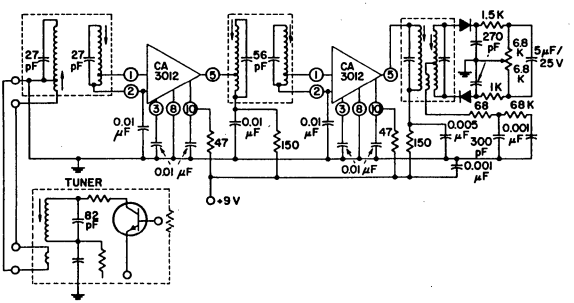



*Fig.9 - Complete 10.7-MHz if-amplifier strip using two CA3012 integrated circuits.*

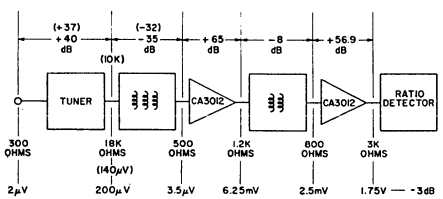



*Fig.10 - Voltage gain and impedance values for if-amplifier strip of Fig.7.*

insertion loss than a triple-tuned input filter, the input required is 20 instead of 3.5 microvolts. All three double-tuned if transformers have an insertion loss of 6 dB and a 3-dB bandwidth of 280 to 300 kHz. The ratio-detector primary impedance dictates the stage gain of 36 dB for the last integrated circuit. Each of the remaining three stages has a gain of 21.5 dB, for the total required gain of 100 dB. The impedance required for the desired stage gain was calculated to be 660 ohms for both the primary and secondary windings of the if transformers.

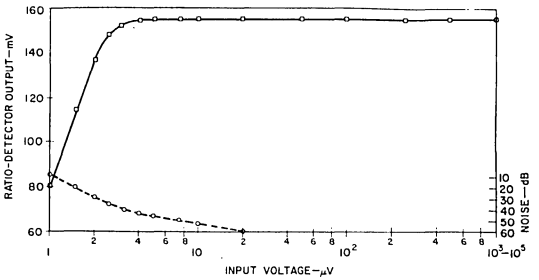



*Fig.11 - Performance curves for if-amplifier strip of Fig.7.*

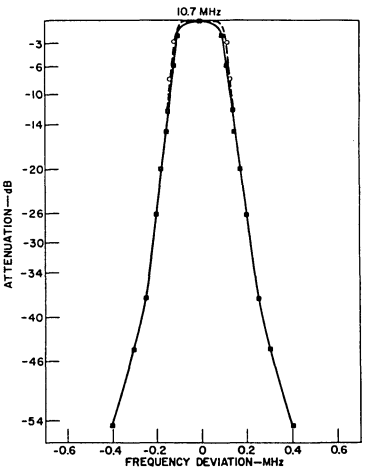



*Fig.12 - Selectivity curve for if-amplifier strip of Fig.7.*

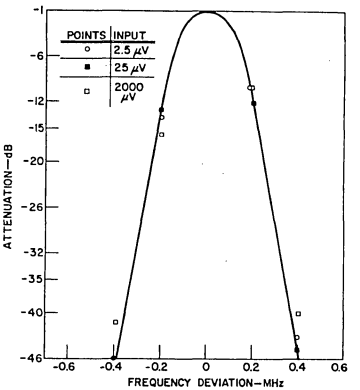



*Fig.13 - Measured over-all selectivity curve for if-amplifier strip of Fig.7 and a given ratio detector.*

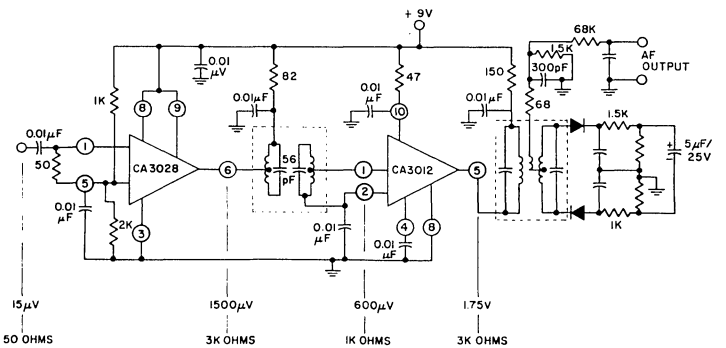



*Fig.14 - IF-amplifier strip using CA3028 and CA3012 integrated circuits.*

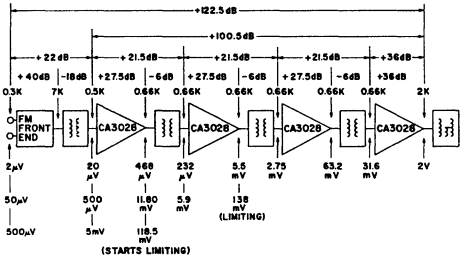



*Fig.15 - Voltage gain and impedance values for if-amplifier strip of Fig.12.*

With inputs from 20 to 200 microvolts, second-channel selectivity as high as 52 to 59 dB can be attained for three double-tuned and four double-tuned filters, respectively, for a 3-dB bandwidth of 196 kHz. For higher inputs, the same deterioration of selectivity occurs as that experienced with discrete circuits, as shown in Fig.16.

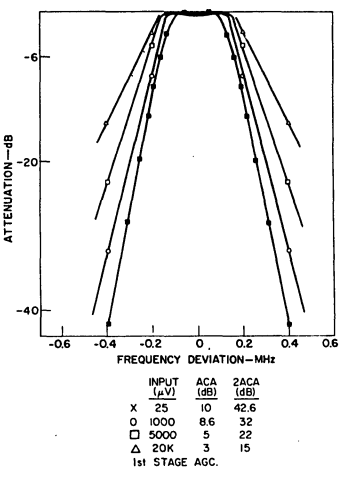



*Fig.16 - Selectivity curves for discrete-component if strip using six double-tuned filters.*

Several receivers incorporating the if strips shown have been field-tested in areas of 200-kHz station separation, where a weak station was sandwiched between two strong stations. The weak station was received without interference, as compared to the performance of other high-quality FM receivers fabricated with discrete-component if circuits, where lack of selectivity marred reception.

## Conclusions

The preceding discussion has shown that the simplest approach to the use of integrated circuits in FM if-amplifier strips is to replace each stage in present discrete-transistor if strips with a differential amplifier. This integrated-circuit approach requires a minimum of re-engineering because a cascade of individually tuned if stages is used. From a performance point of view, this approach results in better AM rejection than that obtained with discrete circuits because of the inherent limiting achieved with the differential-amplifier configuration.

This approach, however, is not the best for cost performance in the long run. The single stage of gain is most difficult to justify economically when a single transistor stage is replaced with a single integrated-circuit package. The boundary condition for such an approach is that ultimately the cost of fabricating a package containing three transistors and three resistors (a typical complement for a differential-amplifier stage) must be the same as that of the one transistor the stage replaces.

Approaches to FM if stages which use the high-gain-per-package concept achieve the excellent AM rejection of differential amplifiers, as well as superior adjacent-channel attenuation, because more gain is inserted between the selectivity elements. From a performance point of view, this approach is superior to both discrete-stage and individually tuned integrated-circuit if strips.

From the point of view of cost, this approach has better possibilities because two packages are equivalent to four single stages of gain (four integrated-circuit packages). This approach results in maximum utilization of present-day monolithic integrated-circuit technology, and is closer to the optimum FM if amplifier shown in Fig.17.

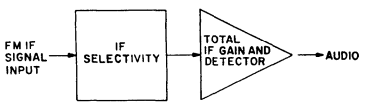



*Fig.17 - Optimum FM if-amplifier configuration.*

# Application of RCA CA3033 and CA3033A High-Performance Integrated-Circuit Operational Amplifiers

by

H. A. Wittlinger

The new RCA CA3033 and CA3033A high-performance operational amplifiers represent a significant step forward in monolithic integrated circuits in many respects. They are capable of delivering power outputs in excess of 250 milliwatts into a 500-ohm load resistance with harmonic distortion of less than 0.2 per cent, and have a typical input impedance of one megohm with voltage gain of at least 90 dB. Offset voltage is less than 5 millivolts, and offset current is typically 9 nanoamperes. Input bias current is typically 100 nanoamperes. These features make these amplifiers especially suitable for systems in which an operational amplifier and power amplifier or driver were formerly required.

## Circuit Description

The RCA CA3033 and CA3033A consist of two differential-amplifier stages followed by a class B output stage, as shown in the schematic diagram of Fig.1. (The two circuits are designed to permit operation from dual 12- and 18-volt dc power supplies, respectively.) Emitter-follower inputs provide the exceptionally high input impedance and low bias current. An additional advantage of the emitter-follower inputs is that the Miller capacitance of the differential amplifier is substantially reduced and the input capacitance of the amplifier is lower than if a similar single-transistor configuration were used.

The output of the first differential-amplifier stage ($Q_3$ and $Q_4$) is buffered from the input of the next differential-amplifier stage ($Q_6$ and $Q_7$) by emitter followers $Q_{19}$ and $Q_{20}$. This arrangement reduces the input-loading effects on the first stage and therefore maintains the first-stage gain.

A circuit is incorporated in this design to sense any change in the operating point of the first differential amplifier caused by variations in either the positive or the negative supply voltage. Any changes in the supply voltages are reflected to the base of transistor $Q_5$, which detects changes in the collector voltage of the first differential amplifier and compensates for them. For example, a rise in the voltage at the emitters of $Q_6$ and $Q_7$ increases the bias voltage to $Q_5$ and thus increases the collector current, countering the apparent rise in the collector voltage of either $Q_3$ or $Q_4$. At the same time, the emitter current of $Q_5$ also increases, and increases the voltage drop across the diode-connected

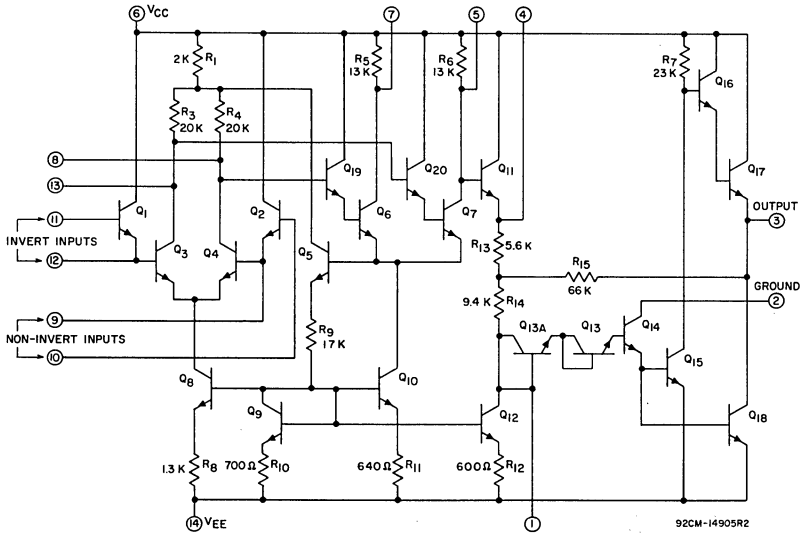



*Fig.1 - Schematic diagram of a CA3033 or CA3033A operational amplifier.*

transistor Q9 and resistor R10 to increase the collector current of Q8. Thus, any apparent increase in the collector voltage of the first differential stage causes a correction both at the constant-current source Q8 and at the collector supply voltage through $R_1$, the common load resistor for $Q_3$, $Q_4$, and $Q_5$.

An emitter-follower $Q_{11}$ buffers the output of the second differential-amplifier stage and drives the divider and summing network to the output stage. Resistor R13 may be considered the input resistance of an amplifier to the summing point, the junction of $R_{13}$, $R_{14}$, and $R_{15}$. Resistor $R_{14}$ shifts to the operating point of the output stage with little attenuation of the signal as a result of the high collector impedance of the constant-current source $Q_{12}$.

Diode-connected transistors $Q_{13A}$ and $Q_{13}$ provide further dc shifting of the signal to the base of emitter-follower $Q_{14}$. This emitter-follower provides further level shifting and a low driving impedance to transistors $Q_{15}$ and $Q_{18}$.

The excellent matching of the base-to-emitter voltage of the integrated-circuit transistors makes it possible to establish the idling current of the output stage accurately. Because the collector-current characteristics of $Q_{15}$ and $Q_{18}$ as a function of base-to-emitter voltage are matched, the collector current in $Q_{15}$ determines the idling current in $Q_{18}$. For example, if the operating current of $Q_{15}$ is set at 1 milliampere for a given base-to-emitter voltage, the operating current of $Q_{18}$ is also 1 milliampere because the base-to-emitter voltages of both transistors are the same. This type of design results from the excellent transistor matching that is possible with monolithic processing.

### Noise Figure

Fig.2 shows noise figure as a function of source resistance for the CA3033A. The curve shows that the optimum noise match occurs for input impedances between 100,000 ohms and 1 megohm. An improvement in noise figure of approximately 14 dB at a frequency of 1 kHz and an input impedance of 1000 ohms may be obtained by addition of two 0.3-megohm resistors from the emitters to the $V_{EE}$ supply to increase the operating current of the input transistors.

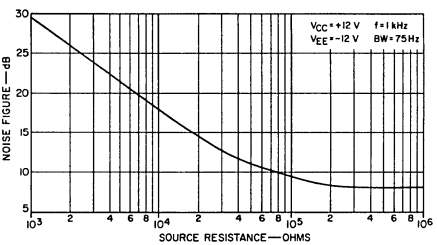



*Fig.2 - Noise-figure curve for CA3033A.*

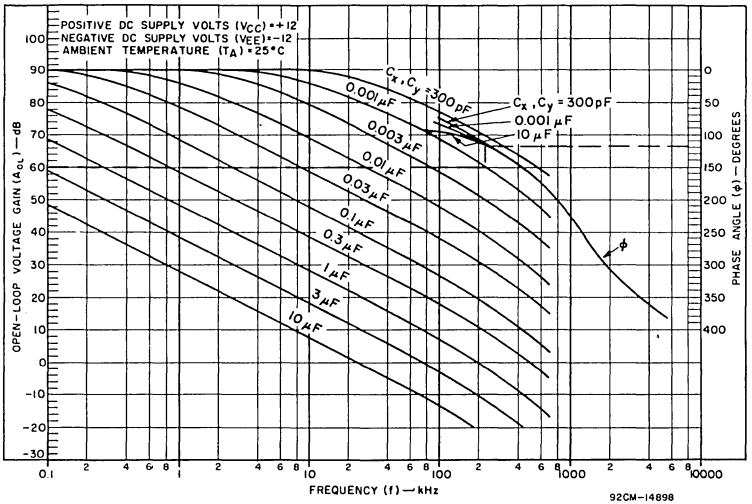



*Fig.3 - Phase-compensation characteristics for CA3033 or CA3033A.*

### Compensation

Basic phase compensation of the CA3033 and CA3033A amplifiers is quite simple. Fig.3 shows typical phase-compensation characteristics for the CA3033; data for the CA3033A are similar. The two compensating capacitors $C_x$ and $C_y$ are connected from the collectors of the first differential amplifier (terminals 8 and 13) to ground. When capacitance values greater than 0.1 microfarad are used, however, a lower-voltage capacitor that has a value equal to half that given on the curves may be connected between terminals 8 and 13, and a 0.001-microfarad capacitor connected from either terminal 8 or 13 to ground. This arrangement provides the same gain-phase roll-off shown on the curves and permits the use of lower-voltage ceramic disc capacitors now available. For linear operation, the maximum expected difference voltage between the two collectors is less than 1 volt.

The dashed lines in Fig.3 illustrate the use of the curves for design of a 60-dB amplifier. First, the intersection of the various gain-frequency curves is followed out to the curve for a capacitor value of 0.001 microfarad. At this point, the expected 3-dB amplifier response is approximately 230 kHz and the phase angle $\phi$ is 118 degrees; the phase margin ($180^\circ - \phi$) is thus 62 degrees. For a capacitance value of 300 picofarads, the expected 3-dB response is 580 kHz, but the phase angle is 175 degrees; the resulting phase margin of only 5 degrees is a most undesirable situation. In the other direction, the use of 0.003-microfarad compensating capacitors provides a 3-dB response of 90 kHz and a phase angle of approximately 90 degrees, with a phase margin of 90 degrees.

### Slewing Rate

One of the most important considerations in using a high-power operational amplifier such as the CA3033 or CA3033A is the maximum full power output swing in terms of frequency that can be expected from the unit. This characteristic is important both in low-frequency applications and in pulse applications in which the rise times of a given design must be known. Fig.4 shows the maximum rate of change, or slewing rate, of a sine wave in volts per microsecond for various peak-to-peak output voltages.[1] For example, a 30-volt peak-to-peak sine wave at a frequency of 10 kHz has a maximum rate of change of 1 volt per microsecond. Besides being able to swing the value of 30 volts peak to peak at dc, therefore, an amplifier must also be able to swing this amplitude at a minimum rate of 1 volt per microsecond.

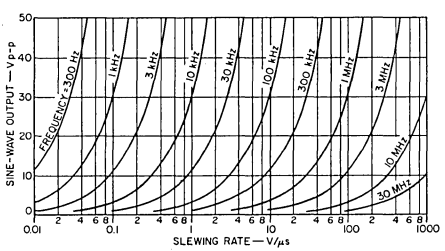



*Fig.4 - Slewing-rate curve.*

Slewing rate is a function of the phase-compensation circuit, the operational-amplifier design in terms of the gain after phase compensation, and the output-stage design. The phase-compensation circuit is usually placed around the input stages of an operational amplifier. This approach offers two advantages. First, it reduces the amplitude of any higher-frequency components that may overload the following stages. (For example, the residual rf carrier remaining on the output of a video detector with a single RC roll-off could cause serious overload and a distorted output if it were allowed to continue through the amplifier.) Second, because of the relatively high gain that follows the compensating circuit in the input stage, the compensating capacitors charge and discharge on a smaller and faster portion of the RC time constant associated with the collector load resistors and compensation capacitors.

Another consideration that influences the slewing rate is the signal-handling capability of the output stage. It is evident that, regardless of how fast the first portion of an amplifier responds to a step input, the output stage can limit the rate of rise and fall.

Fig.5 shows a curve of the maximum full-power-output frequency of the CA3033 and CA3033A as a function of the phase-compensation capacitance. This curve may be used with the curve of Fig.4 to determine the amplifier slewing rate. In the case of the 60-dB amplifier shown in Fig.6, for example, two 0.002-microfarad capacitors are used for phase compensation. The curves of Fig.3 indicate that the 3-dB bandwidth is 120 kHz.

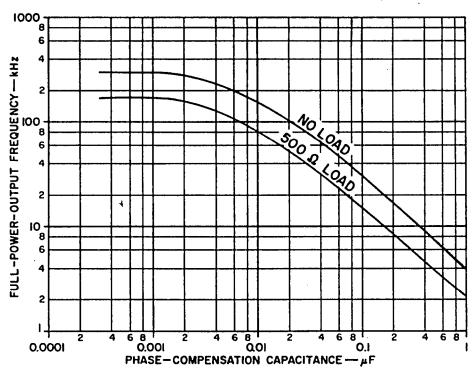



*Fig.5 - Frequency for full power output as a function of phase-compensating capacitance.*

Fig.5 shows that full output swing with no load may be expected up to a frequency of 280 kHz. Therefore, the design is capable of full power output up to the 3-dB point.

A similar approach may be used for a pulse amplifier. Two 0.01-microfarad phase-compensating capacitors are used to yield a 3-dB response of 30 kHz. The expected rise time in microseconds is equal to 0.35 divided by the 3-dB frequency in MHz, or 11.7 microseconds.[2] The power-output curve of Fig.5 shows that the maximum frequency for full power output is 155 kHz; thus the slewing rate is 10.6 volts per microsecond. For the 20-volt input-signal swing specified for the CA3033, the rise time based on this slewing rate would be (1 microsecond/10.6 volts) x 20 volts, or 1.9 microseconds. Because this value is greater than the rise time estimated from the 3-dB point, the design is not slewing-rate limited, and the 3-dB rise time will be met. Thus, for maximum high-frequency output, the lowest value of phase-compensation capacitors must be used; therefore, high closed-loop gains are implicit.

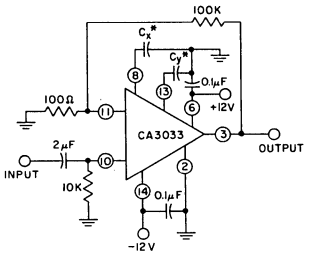



*Fig.6 - 60-dB test amplifier for CA3033.*

Waveforms for the 60-dB amplifier are shown in Fig.7.

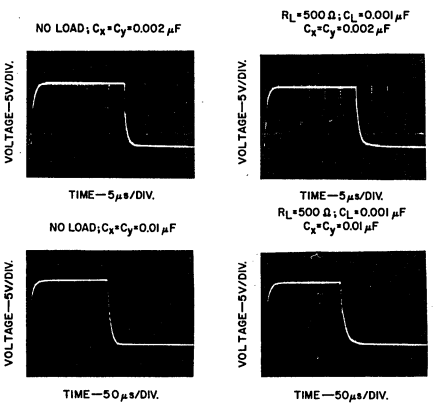



*Fig.7 - Waveforms for the 60-dB amplifier shown in Fig.6.*

## Applications

Fig.8 illustrates the use of the CA3033A in a 20-dB, 255-milliwatt power amplifier operating from a single

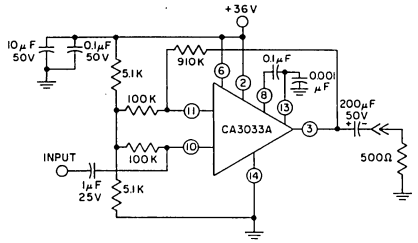



*Fig.8 - 20-dB, 255-milliwatt power amplifier using a CA3033A operating from a 36-volt supply.*

36-volt supply. Fig.9 shows the pulse response of this amplifier under no-load conditions and with a resistive load of 500 ohms; also shown are curves of distortion as a function of frequency. The waveforms show that the pulse response of the amplifier is limited by slewing rate rather than frequency response. Some crossover distortion is evident in the response for the 500-ohm load.

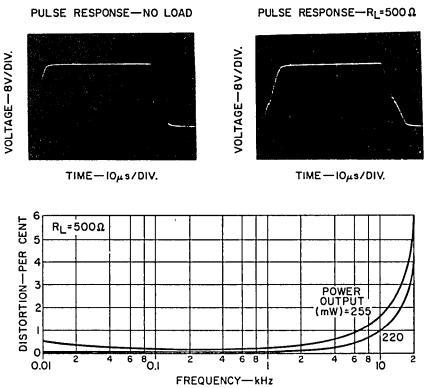



*Fig.9 - Pulse-response waveforms and distortion curves for the amplifier shown in Fig.8.*

The impedance of the feedback network can have a significant effect on the pulse response of a given amplifier design, particularly when higher-frequency performance is required. The response is influenced by the stray capacitance of the associated wiring, the shunt capacitance of the feedback resistors, and the input impedance of the operational amplifier. Because the CA3033 and CA3033A have higher input impedance as a result of the emitter-follower inputs, the input capacitive loading is reduced considerably and higher-impedance feedback networks can be used.

A simple system was fabricated to demonstrate the ease with which the CA3033 and CA3033A operational amplifiers may be applied. The basis of the system was the rudiments of a digital voltmeter, using the linear staircase approach, without the associated totalizing circuitry.

Fig.10 shows a block diagram of the system, together with the waveforms of all interfaces. A squelchable integrated-circuit multivibrator is used as the clock. As described later, the clock frequency is independent of supply voltage. Although this independence is not a necessary condition for circuit operation, it is inherent in this type of operational-amplifier multivibrator circuit and may be considered an integrated-circuit bonus.

The output from the clock drives a linear staircase generator. Input voltage to this circuit is applied directly from the multivibrator to minimize the effects of diode temperature coefficients. The output from the staircase generator is applied to a comparator that compares the staircase with the voltage to be measured.

The comparator output fires a monostable multivibrator that controls the display time, which is variable from about 100 milliseconds to one second. An inverter following the multivibrator supplies drive of the correct polarity to the integrator capacitor-discharge switch and the multivibrator squelch circuit.

Circuit operation begins with the staircase generator ramp running down until its voltage is equal to the unknown voltage on the input of the comparator. When the two voltages are equal, the monostable multivibrator is triggered by the output from the comparator. The output of the monostable multivibrator squelches the astable multivibrator and discharges the integrating capacitor through the bistable multivibrator. The wait, or display time, set by the monostable multivibrator allows sufficient time for full discharge of the integration capacitor and appears as a steady reading on the display device.

**Astable Multivibrator** - A schematic diagram of a squelchable multivibrator is shown in Fig.11. The only requirement that must be met by the squelch circuit is that the amplitude of the output pulse not change as a result of the squelch operation; otherwise, the amplitude of the final steps would be different from that of the initial steps and staircase linearity would suffer.

Freedom of the circuit from supply-voltage variations results from the excellent saturation characteristics of the integrated circuit at both positive and negative output swings. The positive and negative thresholds of the circuit are given by

$$\text{Positive threshold} = (V_{CC} - V_{CE+sat}) \frac{R1}{R1+R2}$$

$$\text{Negative threshold} = (V_{EE} + V_{CE-sat}) \frac{R1}{R1+R2}$$

where $V_{CC}$ and $V_{EE}$ are the positive and negative supply voltages and $V_{CE+sat}$ and $V_{CE-sat}$ are the positive and negative saturation voltages of the amplifier. Be-

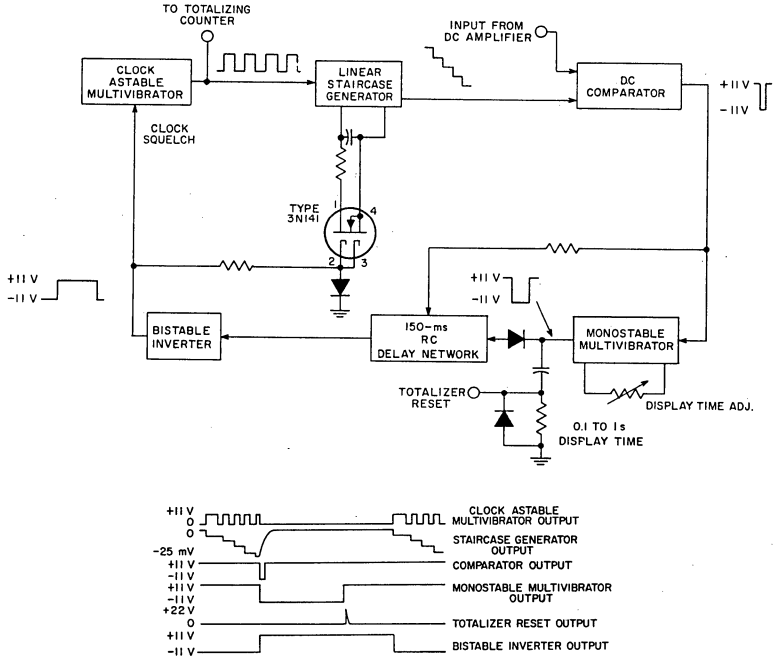



*Fig.10 - Block diagram and waveforms of digital voltmeter system using five CA3033 integrated circuits.*

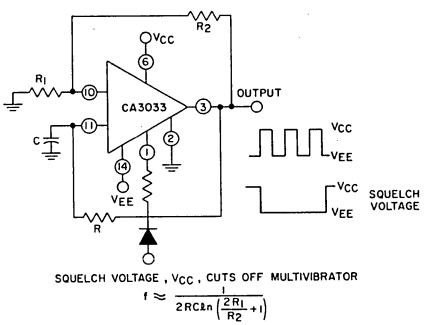



*Fig.11 - CA3033 squelchable astable multivibrator.*

cause these saturation voltages are low and have temperature coefficients less than 5 millivolts per degree C, they can be neglected for ease of computation. If the charging current is considerably greater than the base current, the frequency f may be expressed as follows:[3]

$$f \approx \frac{1}{2\,RC\,\ln\left(\frac{2R_1}{R_2}+1\right)}$$

**Linear Staircase Generator** - The design of a linear staircase generator is nearly identical to that of a linear ramp or sawtooth generator. Fig.12(a) shows a linear ramp generator in which the non-inverting input of an operational amplifier is grounded and a switch $S_1$ returns the output to the inverting input. When $S_1$ is closed, the amplifier is in the unity-gain configuration and the output is at ground less the input offset voltage. When $S_1$ is opened, the output moves in the positive direction when the reference voltage $V_{ref}$ is negative, or in the negative direction when $V_{ref}$ is positive. Because the output under closed-loop conditions tries to maintain the input terminal at zero voltage, the charging current to the capacitor is constant at a rate of dV/dt = i/C,

where i = $V_{ref}/R$. It is apparent that this analysis is valid as long as the input current to the first stage is considerably less than the charging current.

Fig.12(b) shows the circuit for a linear staircase generator. In this circuit, a pulse of amplitude e couples a charge Q to the amplifier input. The charge Q is equal to $C_1$ (e - $2V_{ak}$), where $2V_{ak}$ is the forward voltage drop across the two diodes. Again, if the amplifier input current is small compared to the effective charging current, capacitor $C_2$ is incrementally charged in steps of (e - $2V_{ak}$) $C_1/C_2$. If the pulse height is made sufficiently large compared to the expected temperature variations of the diodes, a reasonable degree of temperature independence results.

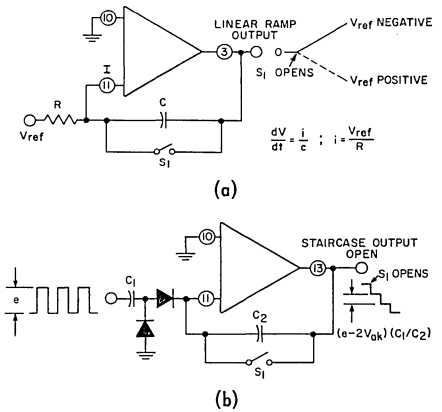



*Fig.12 - Diagrams of (a) linear ramp generator and (b) linear staircase generator.*

**Comparator** - Regeneration is added around the comparator circuit in this system to accelerate the transition time when the two input voltages are equal. Fig.13 shows a complete schematic diagram of the entire system. Waveforms at critical points are shown in Fig.14. The 470-picofarad capacitor and 1000-ohm resistor between terminals 3 and 10 of the CA3033 in the comparator circuit provide the regeneration. Two 0.001-microfarad capacitors on each input filter any externally generated noise.

**Monostable Multivibrator** - The monostable multivibrator circuit shown in Fig.13 makes use of the extremely low input bias currents of the CA3033 by using small timing capacitors and large timing resistors to obtain the long (one-second) display time. The small timing capacitor in conjunction with the diode $D_3$ permits the fast recycling time necessary for the one-step case. Triggering of the circuit is accomplished by the 470-picofarad capacitor to the non-inverting input (terminal 10).

An RC timing network is incorporated at the output of the monostable multivibrator to add an additional 150-millisecond delay that performs two functions. First, the added delay allows more time to complete the timing-capacitor recycling mentioned above. The second and more important function of this network is the generation of a reset pulse at the trailing edge of the monostable multivibrator. Diode $D_4$ couples the negative output of the multivibrator to the next stage and rapidly charges the 0.22-microfarad network timing capacitor through the 470-ohm resistor. After the monostable multivibrator completes the cycle, diode $D_4$ disconnects, and the 0.22-microfarad capacitor charges to the 1.1-volt switching threshold of the next stage through the two one-megohm resistors. This cycle is approximately 150 milliseconds.

**Bistable Multivibrator** - The output from the monostable multivibrator is coupled to the next stage, a bistable multivibrator or inverter. The switching thresholds are determined by the 100,000- and 10,000-ohm resistors in the positive feedback loop. The primary function of this stage is to invert the signals from both the comparator and the monostable multivibrator to drive the clock-astable-multivibrator squelch circuit and the staircase capacitor-discharge switch, an RCA-3N141 dual-gate MOS field-effect transistor. Diode $D_6$ protects the gates of the MOS transistor; the 47-picofarad capacitor reduces the rise time of the negative-going output of the bistable multivibrator and prevents it from coupling into the beginning of staircase and obscuring the first few steps by this negative transition.

**Acknowledgment**

The author thanks A. J. Leidich for his work on the design of the CA3033 and CA3033A and for supplying the noise-figure curve, and J. Klinger for breadboarding and evaluating the many circuits used in the paper.

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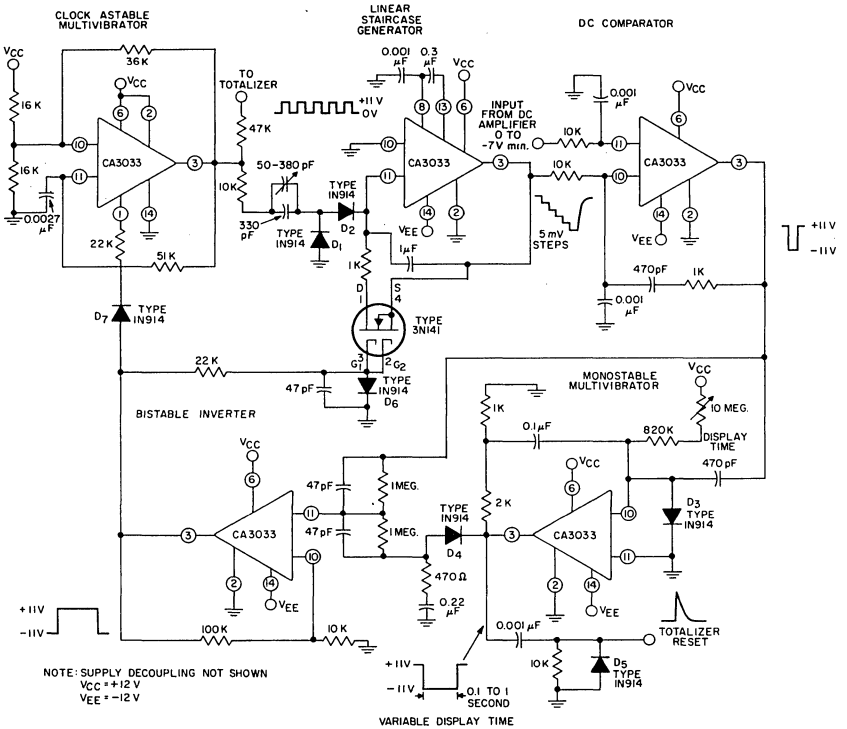



*Fig.13 - Schematic diagram of a digital voltmeter using CA3033 integrated circuits.*

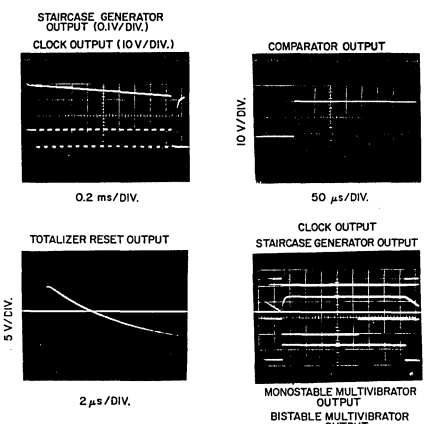



*Fig.14 - Waveforms for the digital voltmeter shown in Fig.13.*

# APPLICATION OF THE RCA CA3020 AND CA3020A INTEGRATED-CIRCUIT MULTI-PURPOSE WIDE-BAND POWER AMPLIFIERS

by

W. M. AUSTIN AND H. M. KLEINMAN

The discussions in this Note are applicable to both integrated-circuit types. The CA3020A can operate in all circuits shown for the CA3020. The CA3020, on the other hand, has a lower voltage rating and must not be used in applications which require voltages on the output transistors greater than 18 volts. The integrated circuit protects the output transistor by limiting the drive to the output stages. The drive-limited current capability of the CA3020 is less than that of the CA3020A, but peak currents in excess of 150 milliamperes are an assured characteristic of the CA3020.

The RCA CA3020 and CA3020A integrated circuits are multi-purpose, multi-function power amplifiers designed for use as power-output amplifiers and driver stages in portable and fixed communications equipment and in ac servo control systems. The flexibility of these circuits and the high-frequency capabilities of the circuit components make these types suitable for a wide variety of applications such as broadband amplifiers, video amplifiers, and video line drivers. Voltage gains of 60 dB or more are available with a 3-dB bandwidth of 8 MHz.

The discussions in this Note are applicable to both integrated-circuit types. The CA3020A can operate in all circuits shown for the CA3020. The CA3020, on the other hand, has more limited voltage- and current-handling capability and must not be used in applications which require voltage swings on the output transistors greater than 18 volts or peak currents in excess of 150 milliamperes.

The CA3020 and CA3020A are designed to operate from a single supply voltage which may be as low as +3 volts. The maximum supply voltage is dictated by the type of circuit operation. For transformer-loaded class B amplifier service, the maximum supply voltages are +9 and +12 volts for the CA3020 and the CA3020A, respectively. When operated as a class B amplifier, either circuit can deliver a typical output of 150 milliwatts from a +3-volt supply or 400 milliwatts from a +6-volt supply. At +9 volts, the idling dissipation can be as low as 190 milliwatts, and either circuit can deliver an output of 550 milliwatts. An output of slightly more than 1 watt is available from the CA3020A when a +12-volt supply is used.

## CIRCUIT DESCRIPTION AND OPERATION

Fig. 1 shows the schematic diagram of the CA3020 and CA3020A, and indicates the five functional blocks into

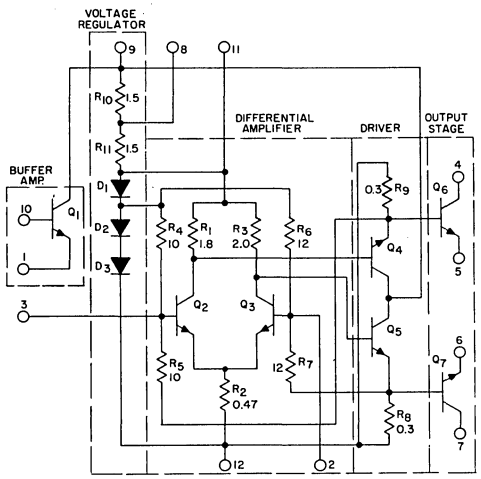



*Fig. 1—Schematic diagram of CA3020 and CA3020A integrated-circuit amplifiers.*

which the circuit can be divided for understanding of its operation. Fig. 2 shows the relationship of these blocks in block-diagram form.

A key to the operation of the circuit is the voltage regulator consisting of diodes $D_1$, $D_2$, and $D_3$ and resistors $R_{10}$ and $R_{11}$. The three diodes are designed to provide accurately controlled voltages to the differential amplifier so that the proper idling current for class B operation is established in the output stage. The characteristics of these monolithic diodes closely match those of the driver and output stages so that proper bias voltages are applied over the entire military temperature range of −55 to +125°C. The close thermal coupling of the circuit assures against thermal runaway within the prescribed temperature and dissipation ratings of the devices.

The differential amplifier operates in a class A mode to supply the power gain and phase inversion required for the push-pull class B driver and output stages. In normal operation, an ac signal is capacitively coupled to terminal

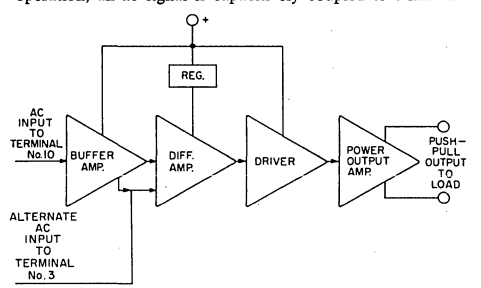



*Fig. 2—Functional block diagram of the CA3020 and CA3020A.*

3, and terminal 2 is grounded through a suitable capacitor. When the signal becomes positive, transistor $Q_2$ is turned on and its collector voltage changes in a negative direction. The same current flows out of the emitter of $Q_2$ and tends to flow to ground through resistor $R_2$. However, the impedance of $R_2$ is high compared to the input impedance of the emitter of $Q_3$, and an alternate path is available to ground through the emitter-to-base junction of transistor $Q_3$ and then through the bypass capacitor from terminal 2 to ground. Because this path has a much lower impedance than $R_2$, most of the current takes this alternate route. The signal current flowing into the emitter of $Q_3$ reduces the magnitude of that current and, because the collector current is nearly equal to the emitter current, the collector current in $Q_3$ drops and the collector voltage rises. Thus, a positive signal on terminal 3 causes a negative ac voltage on the collector of transistor $Q_2$ and a positive ac voltage on transistor $Q_3$, and provides the out-of-phase signals required to drive the succeeding stages. It should be noted that the differential amplifier is not balanced; resistor $R_3$ is ten per cent greater than $R_1$. This unbalance is deliberately introduced to compensate for the fact that all of the current in the emitter of $Q_2$ does not flow into $Q_3$. Use of a larger load resistor for transistor $Q_3$ compensates for the lower current so that the voltage swings on the two collectors have nearly the same magnitude.

The driver stages (transistors $Q_4$ and $Q_5$) are emitter-follower amplifiers which shift the voltage level between the collectors of the differential-amplifier transistors and the bases of the output transistors and provide the drive current required by the output transistors.

The power transistors ($Q_6$ and $Q_7$) are large, high-current devices capable of delivering peak currents greater than 0.25 ampere. The emitters are made available to facilitate various modes of operation or to permit the inclusion of emitter resistors for more complete stabilization of the idling current of the amplifier. Inclusion of such resistors also reduces distortion by introducing negative feedback, but reduces the power-output capability by limiting the available drive.

Inclusion of emitter resistors between terminals 5 and 6 and ground also enhances the effectiveness of the internal dc feedback supplied to the bases of transistors $Q_2$ and $Q_3$ through resistors $R_5$ and $R_7$. Any increase in the idling current in either output transistor is reflected as an increased voltage at its base. This change is coupled to the input through the appropriate resistor to correct for the increased current.

A later section of this Note describes how stable class A operation of the output stages may be obtained.

## OPERATING CHARACTERISTICS

**Supply Voltages and Derating.** The CA3020 operates with any supply voltage between +3 and +9 volts. The CA3020A can also be operated with supply voltages up to +12 volts with inductive loads or +25 volts with resistive loads. Fig. 3 shows the permissible dissipation rating of the CA3020 and CA3020A as a function of case

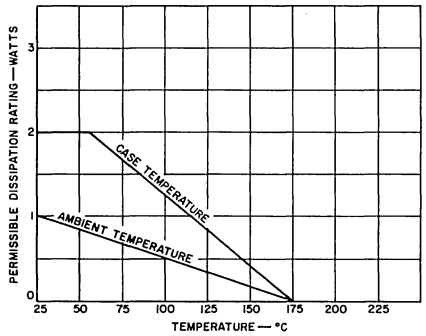


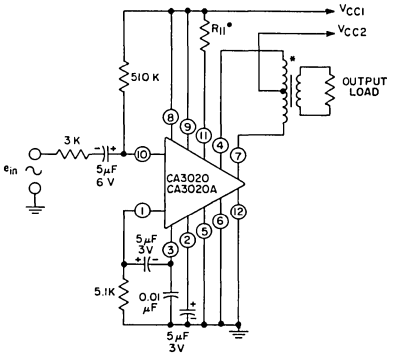

*Fig. 3—Dissipation rating of the CA3020 and CA3020A as a function of case and ambient temperatures.*

and ambient temperatures. At supply voltages from +6 to +12 volts, a heat sink may be required for maximum power-output capability. The worst-case dissipation $P_{d_{max}}$ as a function of power output can be calculated as follows:

$$P_{d_{max}} = (V_{CC_1} I_{CC_1} + V_{CC_2} I_{CC_2}) + (V_{CC_2}{}^2/(R_{CC})$$

where $V_{CC_1}$ and $V_{CC_2}$ are the supply voltages to the differential-amplifier and output-amplifier stages, respectively; $I_{CC_1}$ and $I_{CC_2}$ are the corresponding idling currents; and $R_{CC}$ is the collector-to-collector load resistance of the output transformer. This equation is preferred to the conventional formula for the dissipation of a class B output transistor (i.e., 0.84 times the maximum power output) because the $P_{d_{max}}$ equation accounts for the device standby power and device variability.

**Basic Class B Amplifier.** Fig. 4 shows a typical audio-amplifier circuit in which the CA3020 or CA3020A can provide a power output of 0.5 or 1 watt, respectively. Table 1 shows performance data for both types in this amplifier. The circuit can be used at all voltage and power-output levels applicable to the CA3020 and CA3020A.




* Better Coil and Transformer DF108A, Thordarson TR-192, or equivalent.
• see text and tables.

*Fig. 4—Basic class B audio amplifier circuit using the CA3020 or CA3020A.*

The emitter-follower stage at the input of the amplifier in Fig. 4 is used as a buffer amplifier to provide a high input impedance. Although many variations of biasing may

**Table 1 — Typical Performance of CA3020 and CA3020A in Circuit of Fig. 4***

| Characteristic | CA3020 | CA3020A | |
|---|---|---|---|
| Power Supply — $V_{CC_1}$ | 9 | 9 | V |
| $V_{CC_2}$ | 9 | 12 | V |
| Zero-Signal Idling Current — $I_{CC_1}$ | 15 | 15 | mA |
| $I_{CC_2}$ | 24 | 24 | mA |
| Maximum-Signal Current — $I_{CC_1}$ | 16 | 16.6 | mA |
| $I_{CC_2}$ | 125 | 140 | mA |
| Maximum Power Output at 10% THD | 550 | 1000 | mW |
| Sensitivity | 35 | 45 | mV |
| Power Gain | 75 | 75 | dB |
| Input Resistance | 55 | 55 | kΩ |
| Efficiency | 45 | 55 | % |
| Signal-to-Noise Ratio | 70 | 66 | dB |
| % Total Harmonic Distortion at 150 mW | 3.1 | 3.3 | % |
| Test Signal | 1000 Hz/600Ω generator | | |
| Equivalent Collector-to-Collector Load | 130 | 200 | Ω |
| Idling-Current Adjust Resistor ($R_{11}$) | 1000 | 1000 | Ω |

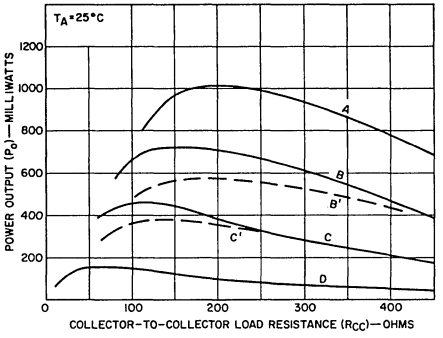
* Integrated circuit mounted on a heat sink, Wakefield 209 Alum. or equiv.

be applied to this stage, the method shown is efficient and economical. The output of the buffer stage is applied to terminal 3 of the differential amplifier for proper balance of the push-pull drive to the output stages. Terminals 2 and 3 must be bypassed for approximately 1000 ohms at the desired low-frequency roll-off point.

At low power levels, the cross-over distortion of the class B amplifier can be high if the idling current is low. For low cross-over distortion, the idling current should be approximately 12 to 24 milliamperes, depending on the efficiency, idling dissipation, and distortion requirements of the particular application. The idling current may be increased by connection of a jumper between terminals 8 and 9. If higher levels of operating idling current are desired, a resistor ($R_{11}$) may be used to increase the regulated voltage at terminal 11 by a slight amount with additional current injection from the power supply $V_{CC_1}$.

In some applications, it may be desirable to use the input transistor $Q_1$ of the CA3020 or CA3020A for other purposes than the basic buffer amplifier shown in Fig. 4. In such cases, the input ac signal can be applied directly to terminal 3.

The extended frequency range of the CA3020 and CA3020A requires that a high-frequency ac bypass capacitor be used at the input terminal 3. Otherwise, oscillation could occur at the stray resonant frequencies of the external components, particularly those of the transformers. Lead inductance may be sufficient to cause oscillation if long power-supply leads are not properly ac bypassed at the CA3020 or CA3020A common ground point. Even the bypassing shown may be insufficient unless good high-frequency construction practices are followed.

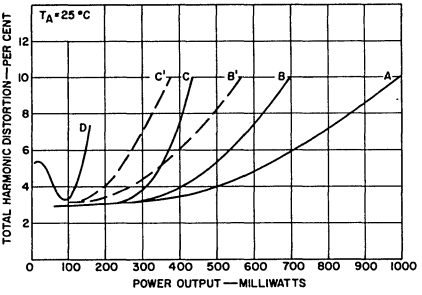



| CURVE CA3020 | CURVE CA3020A | IDLING CURRENT (mA) $I_{CC1}$ | IDLING CURRENT (mA) $I_{CC2}$ | POWER-SUPPLY VOLTAGE (V) $V_{CC1}$ | POWER-SUPPLY VOLTAGE (V) $V_{CC2}$ | $R_{11}$ (OHMS) |
|---|---|---|---|---|---|---|
| - | A | 9 | 10 | 9 | 12 | ∞ |
| B' | B | 9 | 10 | 9 | 9 | ∞ |
| C' | C | 7 | 6 | 6 | 6 | ∞ |
| - | D | 8 | 8 | 3 | 3 | 220 |

*Fig. 5—Power output of the CA3020 and CA3020A as a function of collector-to-collector load resistance $R_{CC}$.*

Fig. 5 shows typical power output of the CA3020A at supply voltages of +3, +6, +9, and +12 volts, and of the CA3020 at +6 and +9 volts, as measured in the basic class B amplifier circuit of Fig. 4. The CA3020A has higher power output for all voltage-supply conditions because of its higher peak-output-current capability.

Fig. 6 shows total harmonic distortion (THD) as a function of power output for each of the voltage conditions shown in Fig. 5. The values of the collector-to-collector load resistance ($R_{CC}$) and the idling-current adjust resistor ($R_{11}$) shown in the figure are given merely as a fixed reference; they are not necessarily optimum values. Higher idling-current drain may be desired for low cross-over distortion, or a higher value of $R_{CC}$ may be used for better sensitivity with less power-output capability. Because the maximum power output occurs at the same conditions of peak-current limitations, the sensitivities at maximum power output for the curves of Figs. 5 and 6 are approximately the same. Increasing the idling-current drain by reducing the value of the resistor $R_{11}$ also improves the sensitivity.




| CURVE CA3020 | CURVE CA3020A | IDLING CURRENT (mA) | | POWER-SUPPLY VOLTAGE (V) | | $R_{CC}$ (OHMS) | $R_{11}$ (OHMS) |
|---|---|---|---|---|---|---|---|
| - | A | 15 | 24 | 9 | 12 | 200 | 1000 |
| B' | B | 15 | 24 | 9 | 9 | 150 | 1000 |
| C | C | 12 | 14 | 6 | 6 | 100 | 1000 |
| - | D | 9 | 9 | 3 | 3 | 50 | 220 |

*Fig. 6—Total harmonic distortion of the CA3020 or CA3020A as a function of power output.*

Fig. 7 illustrates the improvement in cross-over distortion at low power levels. Distortion at 100 milliwatts is shown as a function of idling current $I_{CC_2}$ (output stages only). There is a small improvement in total harmonic distortion for a large increase in idling current as the current level exceeds 15 milliamperes.

## APPLICATIONS

**Audio Amplifiers.** The circuit shown in Fig. 4 may be used as a highly efficient class B audio power-output circuit in such applications as communications systems, AM or FM radios, tape recorders, phonographs, intercom sets, and linear mixers. Fig. 8 shows a modification of this

circuit which may be used as a transformerless audio amplifier in any of these applications or in other portable instruments. The features of this circuit are a power-output capability of 310 milliwatts for an input of 45 millivolts, and a high input impedance of 50,000 ohms. The idling-current drain of the circuit is 24 milliamperes. The curves of Fig. 5 may be used to determine the value of the center-tapped resistive load required for a specified power-output level (the indicated load resistance is divided by two).

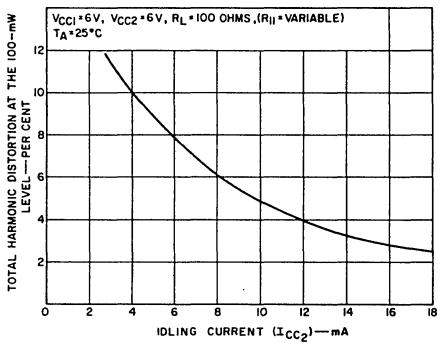



*Fig. 7—Total harmonic distortion as a function of idling current for a supply voltage of 6 volts and an output of 100 milliwatts.*

The CA3020 or CA3020A provides several advantages when used as a sound output stage or as a preamplifier-driver in communications equipment because each type is a compact and low-power-drain circuit. The squelching requirement in such applications is simple and economical.

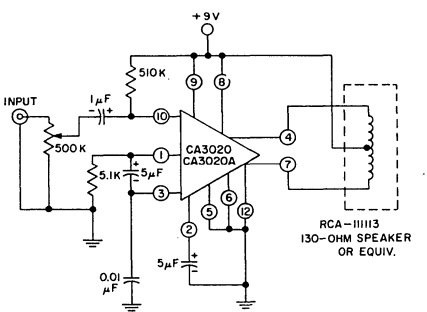



*Fig. 8—310-milliwatt audio amplifier without transformers.*

Fig. 9 shows a practical method of providing squelch to the CA3020 or CA3020A. When the squelch switching transistor $Q_s$ is in the "on" state, the CA3020 or CA3020A

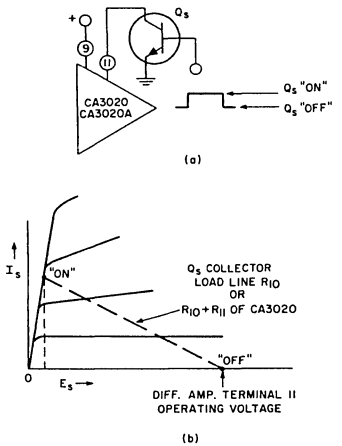


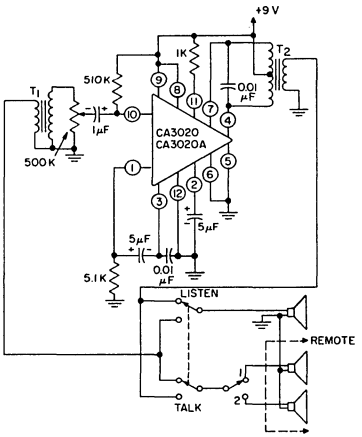

*Fig. 9—Method of applying squelch to the CA3020 or CA3020A to save idling dissipation.*

is "off" and draws only fractional idling dissipation. The only current that flows is that of the buffer-amplifier transistor $Q_1$ in the integrated circuit and the saturating current drain of $Q_s$. For a circuit similar to that of Fig. 8, the squelched condition requires an idling current of approximately 7 milliamperes, as compared to a normal idling-current drain of 24 milliamperes.

In applications requiring high gain and impedance matching, the CA3020 or CA3020A can be adapted for use without complex circuit modifications. Detectors having low signal outputs or high impedances can be easily matched to the input of the CA3020 or CA3020A buffer amplifier. The typical integrated-circuit input impedance of 55,000 ohms may be too low for crystal output devices such as phonograph pickups, but the sensitivity may be sacrificed to impedance-match at the input while still providing adequate drive to the CA3020 or CA3020A. Both types may be used in tape recorders as high-gain amplifiers, bias oscillators, or record and playback amplifiers. The availability of two input terminals permits the use of the CA3020 or CA3020A as a linear mixer, and thus adds to its flexibility in systems that require adaptation to multiple functions, such as communications equipment and tape recorders.

Fig. 10 illustrates the use of the audio amplifier shown in Fig. 4 in an intercom in which a listen-talk position switch controls two or more remote positions. Only the speakers, the switch, and the input transformer are added to the basic audio amplifier circuit. A suitable power supply for the intercom could be a 9-volt battery used intermittently rather than continuously.

**Wide-Band Amplifiers.** A major general-purpose application of the CA3020 and CA3020A is to provide high gain and wide-band amplification. The CA3020 and CA3020A




$T_1$: Primary 4 ohms, Secondary 25,000 ohms; Stancor A4744 or equiv.

$T_2$: Better Coil and Transformer DF1084, Thordarson TR-192, or equiv.

Speakers: 4 ohms

*Fig. 10—Intercom using CA3020 or CA3020A.*

have typically flat gain-bandwidth response to 8 MHz. Although the circuits are normally biased for class B operation, only the output stages operate in this mode. If proper dc bias conditions are applied, the output stages may be operated as linear class A amplifiers.

Fig. 11 shows the recommended method for achieving an economical and stable class A bias. The differential-amplifier portion of the CA3020A is placed at a potential

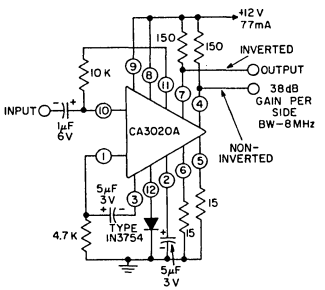



*Fig. 11—Wide-band video amplifier illustrating economical and stable class A bias of CA3020A.*

above ground equal to the base-to-emitter voltage $V_{be}$ of the integrated-circuit transistors (0.5 to 0.7 volt). In this condition, the output stages have an emitter-current bias approximately equal to the base-to-emitter voltage divided by the emitter-to-ground resistance. The circuit in Fig. 11 is a wide-band video amplifier that provides a gain of 38 dB at each of the push-pull outputs, or 44 dB in a balanced-output connection. The 3-dB bandwidth of the circuit is 30 Hz to 8 MHz. Higher gain-bandwidth performance can be achieved if the diode-to-ground voltage drop at terminal 12 is reduced. The lower voltage drop permits the use of a higher ratio of output-stage collector-to-emitter resistors without departure from the desired portion of the class A load line. It is important to note that the temperature coefficient of the terminal-12-to-ground reference element should be sufficiently low to prevent a large change in the current of the output stages.

The same method for achieving class A bias is used in the large-signal-swing output amplifier shown in Fig. 12.

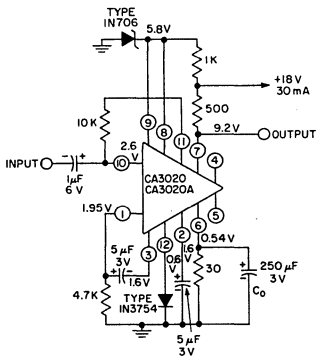



*Fig. 12—Large-signal-swing output amplifier using CA3020 or CA3020A.*

Either the CA3020 or the CA3020A may be used in this circuit with power supplies below +18 volts; the CA3020A can also be used with B+ voltages up to 25 volts with non-inductive loads. The circuit of Fig. 12 provides a gain of 60 dB and a bandwidth of 3.2 MHz if the output transistor $Q_7$ has a bypassed emitter resistor. With an unbypassed output emitter resistor, the gain is 40 dB and the bandwidth is 8 MHz. The output stage can deliver a 5-volt-rms signal when a supply of +18 volts is used. For better performance in this type of circuit, the input signal is coupled from the buffer amplifier $Q_1$ to the input terminal 3 of the differential amplifier. This arrangement provides higher gain because the collector resistor of the differential-amplifier transistor $Q_3$ is larger than that of $Q_2$. (This difference results from a requirement of differential drive balance that is not used in this circuit.) In addition, the terminals of the unused output transistor $Q_6$ help to form an isolating shield between the input at terminal 3 and the output at terminal 7. This cascade of amplifiers has a single phase inversion at the output for much better stability than could be achieved if terminal 4 were used as the output and terminal 3 as the input.

Fig. 13 illustrates the use of the CA3020 or CA3020A as a class A linear amplifier. This circuit features a very

low output impedance and may be used as a line-driver amplifier for wide-band applications up to 8 MHz. The circuit requires a 0.12-volt peak-to-peak input for a single-ended output of 1 volt or a balanced peak-to-peak output of 2 volts from a 3-ohm output impedance at each emitter. The input impedance is specified as 7800 ohms, but is primarily a function of the external 10,000-ohm resistor that provides bias to $Q_1$ from the regulating terminal 11.

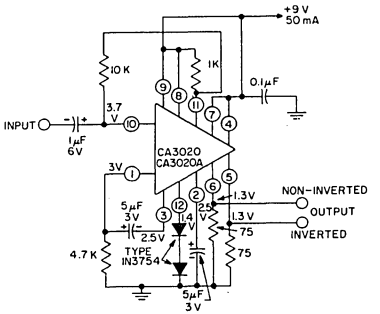



*Fig. 13—Class A linear amplier using CA3020 or CA3020A.*

Fig. 14 illustrates the practical use of the CA3020 or CA3020A as a tuned amplifier. This circuit uses dc biasing similar to that shown previously, and has a gain of 70 dB at a frequency of 160 kHz. The CA3020 or CA3020A can be used as a tuned rf amplifier or oscillator at frequencies well beyond the 8-MHz bandwidth of the basic circuit.

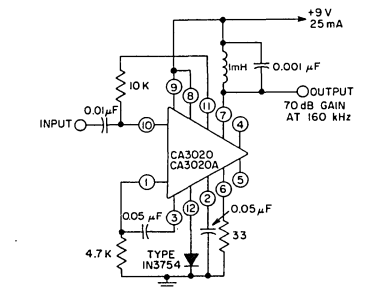
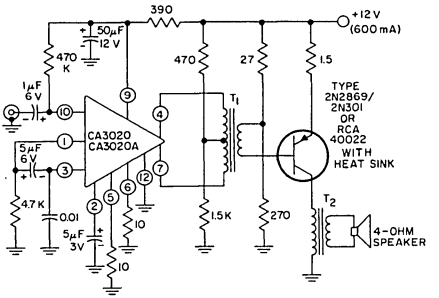



*Fig. 14—160-kHz tuned amplifier using the CA3020 or CA3020A.*

**Driver Amplifiers.** The high power-gain and power-output capabilities of the CA3020 and CA3020A make these integrated circuits highly suitable for use as drivers for higher-power stages. In most applications, the full power-output capability of the circuit is not required, and large emitter resistors may be used in the output stage to reduce distortion. The CA3020 and CA3020A can drive any transformer-coupled load within their respective ratings. Several examples of typical applications are given below.

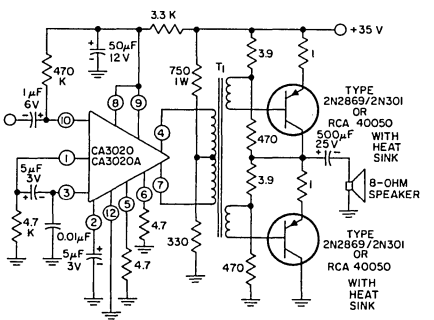
Fig. 15 illustrates the use of the CA3020 or CA3020A to drive a germanium power-output transistor to a 2.5-watt level. Because the integrated circuit is required to deliver a maximum power output of less than 50 milliwatts, an unbypassed emitter resistor can be used in the output stage to reduce distortion. Sensitivity for an output of 2.5 watts is 3 millivolts; this figure can be improved at a slight increase in distortion by reduction of the 4.7-ohm resistors between terminals 5 and 6 and ground.




$T_1$: primary impedance, 10,000 ohms; center-tapped at 160 ohms; primary direct current, 2 milliamperes; Thordarson TR-207 (entire secondary), or equiv.

$T_2$: primary impedance, 20 ohms; primary direct current, 0.6 ampere; secondary, 4 ohms; Thordarson TR-304, Stancor TP62, or equiv.

*Fig. 15—2.5-watt class A audio amplifier using the CA3020 or CA3020A as a driver amplifier.*




$T_1$: primary impedance, 4,000 ohms; center-tapped; secondary impedance, 600 ohms; center-tapped, split; Thordarson TR-454 or equivalent.

*Fig. 16—10-watt single-ended class B audio amplifier using the CA3020 or CA3020A as a driver amplifier.*

Because so little of the power-output capability of the CA3020 or CA3020A is used, higher-power class B stages can easily be accommodated by selection of suitable output transistors and appropriate transformers.

Fig. 16 shows a medium-power class B audio amplifier in which the CA3020 or CA3020A is used as a driver. The output stage uses a pair of TO-3-type germanium output transistors which must be mounted on a heat sink for reliable operation. Idling current for the entire system is 70 milliamperes from the 35-volt supply. Sensitivity is 10 millivolts for an output of 10 watts.

**Motor Controller and Servo Amplifier.** The CA3020 or CA3020A may be used as a 40-to-400-Hz motor controller and servo amplifier, as shown in Fig. 17.

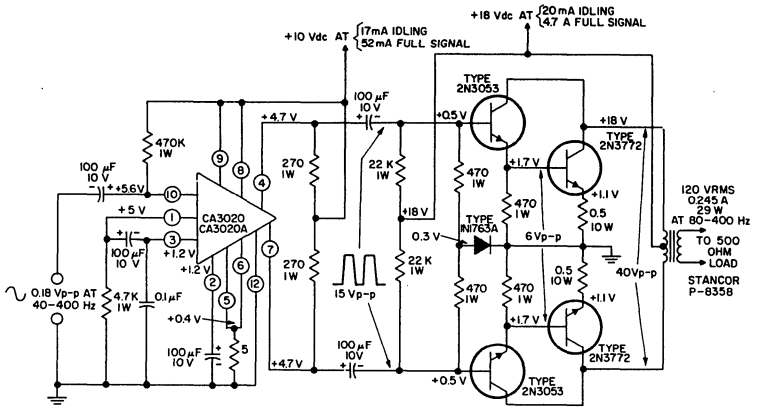



*Fig. 17—Motor controller and servo amplifier using CA3020 or CA3020A.*

# Application of the RCA-CA3044 and CA3044V1 Integrated Circuits in Automatic-Fine-Tuning Systems

by

W. M. Austin, H. M. Kleinman, and J. Sundburg

This Note describes the use of the RCA-CA3044 and CA3044V1 integrated circuits as automatic-fine-tuning (AFT) system components and discusses the advantages of integrated circuits in this application. The CA3044V1 is electrically identical to the CA3044, but is supplied with formed leads for easier printed-circuit-board mounting; throughout this Note a reference to the CA3044 implies a similar reference to the CA3044V1.

The RCA-CA3044 is a special-function subsystem integrated circuit that represents a second generation of the AFT integrated circuit, the CA3034, that was designed specifically for frequency-control applications. The CA3044, unlike the CA3034, has an internal zener-regulated power supply that improves performance and reduces system cost. It is designed to replace the CA3034 in similar applications with only minor changes in the system circuit.

## Circuit Description and Operation

The schematic diagram of the CA3044 is shown in Fig. 1; the use of the circuit in a typical automatic-fine-tuning (AFT) system for a color television receiver is shown in Fig. 2. In such a system, the CA3044 provides all of the signal-processing components needed (with the exception of the tuned phase-detector transformer) to derive the AFT correction signals from the output of the video-if amplifier. The other components of the system provide signal coupling and power-supply decoupling as required for proper signal processing in the video intermediate-frequency range.

The CA3044 integrated circuit can be considered as the combination of four functional blocks: a limiter-amplifier, a balanced detector, a differential amplifier, and a regulator. The 45-MHz limiter-amplifier composed of $Q_1$ and $Q_2$ is a differential amplifier that supplies a

peak-to-peak output current of approximately 4 milliamperes for input levels above the limiting threshold. The use of a load impedance which does not exceed 2000 ohms guarantees an excellent limiting characteristic and eliminates detuning effects caused by saturation of the amplifier under worst-case conditions. In the system shown in Fig.2, the load impedance at the center frequency is about 1800 ohms.

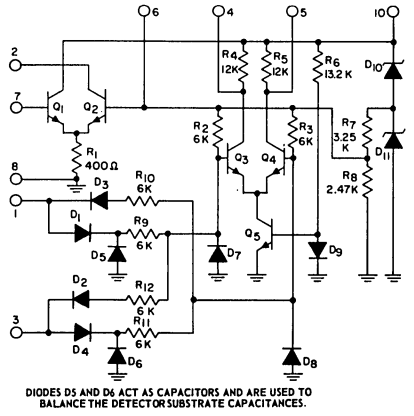



*Fig.1 - Schematic diagram of the CA3044 and CA3044VI.*

The diode matrix composed of $D_1$, $D_2$, $D_3$, and $D_4$ constitutes a balanced detector that converts the output of the phase transformer to a filtered dc signal. Diodes $D_1$ through $D_4$ perform the detection function. Diodes $D_7$ and $D_8$ are always reverse-biased and serve as capacitors; they filter the output of the detector in conjunction with $R_9$ through $R_{12}$. Diodes $D_5$ and $D_6$ are included to balance the parasitic diodes that exist between the cathodes of $D_2$ and $D_3$ and the substrate.

Transistors $Q_3$, $Q_4$, and $Q_5$ form a constant-current driven differential amplifier that is directly coupled to the output of the detector. The amplifier contributes greatly to the high sensitivity of the system and, in addition, provides sufficient power to allow the use of a low-cost tuning element. The output impedance at either output of the amplifier is approximately 12,000 ohms.

The zener-diode regulator comprising $D_{10}$ and $D_{11}$ provides the regulation necessary for a differential post-detection amplifier output that is both stable and independent of temperature and power-supply variations. The junction of $D_{10}$ and $D_{11}$ is connected to a bias divider network that assures correct base bias on both differential-amplifier pairs.

During normal operation, the proper dc bias for terminals 1,3, and 7 of the CA3044 is supplied through terminal 6 and external rf coils, as shown in Fig.2. RF bypassing is required both for terminal 6 and for terminal 10, which is connected through the primary winding of the detector transformer to terminal 2.

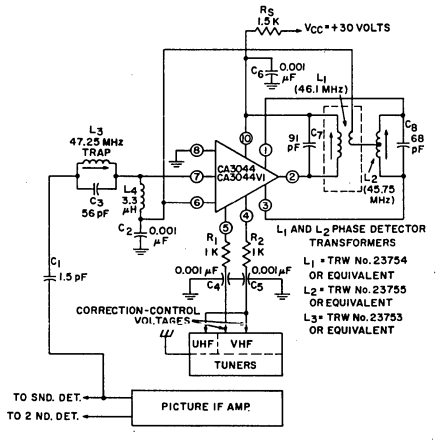



*Fig.2 - System diagram of a typical automatic-fine-tuning (AFT) application showing the CA3044 or CA3044VI in use in a color-TV receiver.*

## Operating Characteristics

The CA3044 is designed to operate from supply voltages greater than the zener regulating voltage; because the zener-diode voltage varies from 10.5 to 11.9 volts at the 14-milliampere current-drain level, the supply voltage should be greater than 15 volts for proper regulation and circuit operation. The effect of all component and power-supply tolerances on zener regulating current must be taken into account in calculation of the value of the series regulating resistor $R_s$ shown at the top of Fig. 2. In the typical circuit shown in Fig. 2, power is supplied to terminal 10 of the CA3044 from a +30-volt supply through a 1500-ohm series dropping resistor. The recommended value of $R_s$ can be determined for other supply conditions by use of the curves in Fig.3, which show current at terminal 10 as a function of supply voltage. An $R_s$ load line may be drawn through the safe operating area to show extremes of voltage and current for normal variations in product. Safe operation with proper regulation is achieved on any load line that avoids the lower cross-hatched area and does not exceed the allowable maximum dissipation as determined for a given ambient temperature. The cross-hatched area represents voltage-regulation dropout resulting from an insufficient amount of zener-diode current.

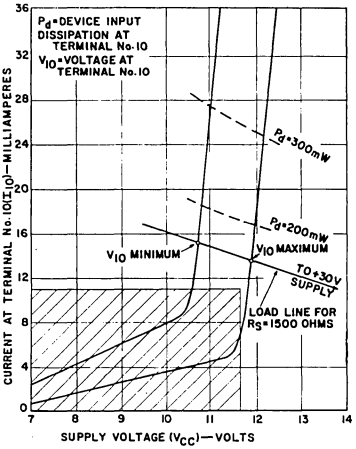



*Fig.3 - Curves for determining the zener-diode regulating voltage at terminal 10.*

The maximum value of $R_S$ is determined by construction of a load line from the minimum supply voltage ($V_{CC}$) to the upper right corner of the cross-hatched area. The largest standard resistor having a maximum value (including tolerance) smaller than the slope of this line is selected. Dissipation under the worst-case conditions of minimum $R_S$ and maximum $V_{CC}$ must then be checked to assure compliance with the maximum device ratings.

The dissipation rating of the CA3044 is 830 milliwatts at an ambient temperature of 25°C. At ambient temperatures above 25°C, this maximum value must be derated by a factor of 5.6 milliwatts per degree. Fig.4 shows the permissible dissipation of the CA3044 as a function of ambient temperature. The worst-case dissipation may occur at either a voltage or a current maximum. The equation for total dissipation $P_d$ in the CA3044 is

$$P_d = \frac{(V_{CC} - V_{10})}{R_S} \quad V_{10}$$

where $V_{10}$ is the voltage at terminal 10 and $V_{CC}$ is the power-supply voltage supplied through the series dropping resistor $R_S$ to terminal 10. The permissible ambient-temperature operating range for the CA3044 is - 55°C to +125°C.

### Dynamic Performance

The system diagram of Fig.2 shows the CA3044 in its function as rf amplifier, frequency discriminator, and post-detection differential dc amplifier. The circuit shown is a portion of a color television receiver in which critical tuning is essential because of the presence of the color subcarrier and its sidebands. The

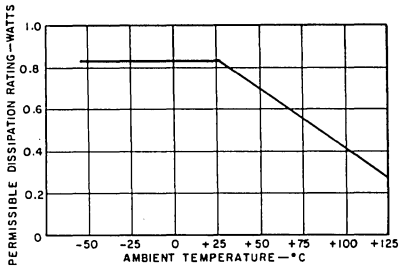



*Fig.4 - Dissipation rating of the CA3044 and CA3044VI as a function of ambient temperature.*

CA3044 AFT system provides a uniform and accurate tuning reference. When the correction voltage developed at terminals 4 and 5 of the CA3044 is sufficient, the system locks on the picture-carrier intermediate frequency and holds the tuner oscillator within ±25 kHz of the picture carrier so that a high-quality picture is produced at all times. Operation within such a narrow band of oscillator frequencies represents a color-reference deviation of less than 5 per cent from the ±500-kHz color-subcarrier sidebands; this deviation is in general far smaller than the amplitude and phase-change errors that are introduced by other receiver and transmitter functions.

The system shown in Fig.2 can be used in a typical color receiver. The sampling connection from the picture-if amplifier to the AFT circuit is made from the output of the last if stage directly to the input of the CA3044 rf amplifier. The loading effect of the AFT-system coupling circuit on the picture-if amplifier is negligible and does not distort the if response. Unless provision has been made to trap out the adjacent-channel sound carrier elsewhere in the circuit, such action must be taken at the input to the CA3044. Trapping of the adjacent-channel sound carrier is essential because it may have sufficient amplitude to cause limiting at the rf amplifier/limiter stage of the CA3044. The trapping circuit, composed of $L_3$ and $C_3$ in Fig.2, also helps to peak the picture carrier at 45.75 MHz while trapping the adjacent-channel sound carrier at 47.25 MHz. To compensate for an if response that places the picture carrier at the 50-per-cent point on the if slope, the input trap should be adjusted to peak the response above 45.75 MHz at the input to the CA3044.

Proper dc biasing of the amplifier/limiter stage composed of $Q_1$ and $Q_2$ requires that a small choke, $L_4$, be used to couple terminal 6 to terminal 7. The common bias connection at terminal 6 is bypassed with a 0.001-microfarad disc capacitor. No form of external dc connection should be made to either terminal 6 or terminal 7.

The output load on the differential amplifier consists of the impedance of the phase-shift transformer

comprising $L_1$ and $L_2$. The differential-amplifier stage assures symmetrical limiting above 100 millivolts at the input of terminal 7. The primary of the phase-shift transformer is typically tuned to 46.1 MHz as an additional error-correction device to help peak the picture carrier at 45.75 MHz. The secondary is tuned to 45.75 MHz and symmetrically drives the double-balanced detector comprising diodes $D_1$, $D_2$, $D_3$, and $D_4$. The detector diodes $D_1$ through $D_4$ minimize frequency shifting by symmetrically loading the discriminator transformer. Symmetrical loading is assured by diodes $D_5$ and $D_6$, which are used as capacitors to balance the inherent substrate capacitances associated with $D_2$ and $D_3$.

The error signal detected by the double-balanced detector is filtered by the 6000-ohm resistors $R_9$, $R_{10}$, $R_{11}$, and $R_{12}$ and diodes $D_7$ and $D_8$ at the inputs to the differential output amplifier composed of $Q_3$ and $Q_4$. The differential output amplifier is compensated for all temperature-change effects including those of the zener-diode regulator. In the absence of an error signal, output terminals 4 and 5 are at a dc level of 6.5 volts; in mistuning or frequency correction, the output level varies from 33 to 85 per cent of the zener-regulated voltage over the ±25-kHz limits. Fig.5 shows the typical narrow-band response of the system shown in Fig.2; Fig.6 shows the wide-band response. The curves shown are characteristic of the Fig.2 circuit for an input rf signal level of 200 millivolts rms at terminal 7. Both narrow- and wide-band response characteristics are a function of the CA3044 limiting level. The narrow-band crossover slope decreases and the wide-band response becomes narrow as the signal level decreases.

The reference levels(A, B, C, and D) indicated on the curves of Fig.5 and 6 refer to the narrow- and wide-band control points expressed as a percentage of the zener reference voltage at terminal 10. References A and B are narrow-band (±25-kHz) control points at 85

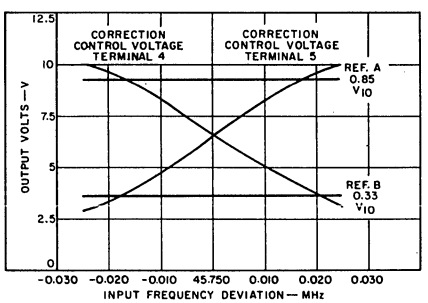



*Fig.5 - Typical narrow-band dynamic control voltage characteristics.*

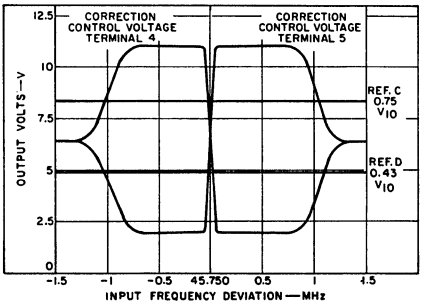



*Fig.6 - Typical wide-band dynamic control voltage characteristics.*

and 33 per cent of the terminal 10 reference voltage, while references C and D are the wide-band (±0.9-MHz) control points at 75 and 43 per cent of the same voltage. The dynamically controlled test circuit for measuring performance in the recommended application circuit is similar to that circuit and is shown in Fig.7. The correction voltages from terminals 4 and 5 are applied to

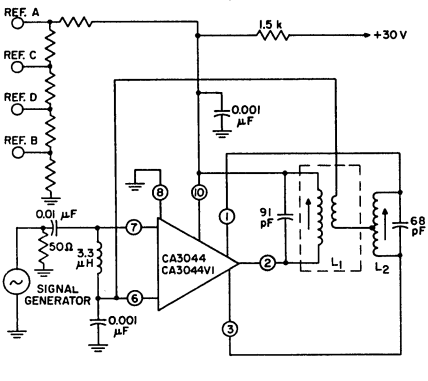



*Fig.7 - Correction voltage test circuit for the CA3044 and CA3044VI.*

the tuning elements of the voltage-controlled oscillator portion of the uhf and vhf tuners. These voltages may be used single-ended and of either phase-polarity for uhf oscillator control. The vhf oscillator may be controlled with a push-pull output to assure attainment of maximum tuning range. The channel-tuning defeat-switch function is normally accomplished by shorting the control-voltage terminals 4 and 5 together. For fil-

tering purposes and to protect the integrated circuit, it is best to include a shunt capacitor and series resistor between the tuning elements and terminals 4 and 5; in Fig.2, 1000-ohm resistors and 0.001-microfarad feed-through capacitors are used.

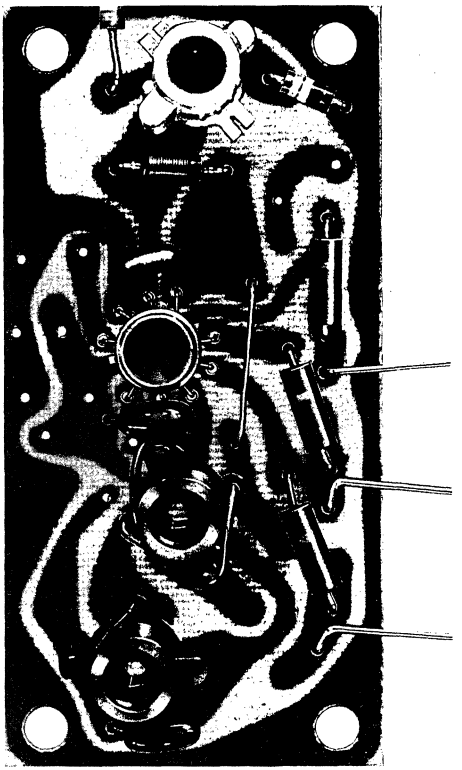


*Fig.8 - Printed circuit board containing the circuit of Fig.2.*

**Construction**

Fig.8 shows a circuit board containing the circuit of Fig.2; Fig.9 is an unobstructed view of the printed-circuit board used. The location and orientation of the discriminator transformer coils affect the over-all response of the circuit; therefore, their placement should be given the greatest attention. Because the metal pattern must be taken into account in component placement, some experimentation may be necessary to achieve the best results. It is recommended that the circuit be shielded to prevent radiation of the 45.75-MHz signal.

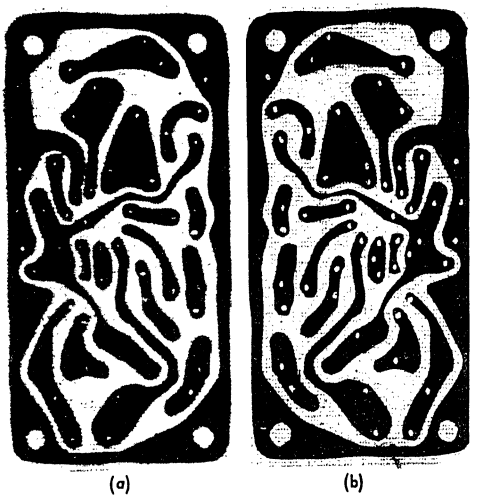



*Fig.9 - An unobstructed view of the top (a) and bottom (b) of the printed circuit board used in Fig.8.*

The circuit described in this Note has been duplicated many times with both hand-made and commercial coils. Alignment has always been rapid and positive and the performance extremely uniform.

# Feedback-Type Volume-Control Circuits for RCA-CA3041 and CA3042 Integrated Circuits

by

L. Kaplan

This Note describes feedback-type volume controls for use with RCA-CA3041 and CA3042 integrated circuits in television receivers. In television sets using these integrated circuits, the volume control is often located remote from the amplifier. The long leads required in such a configuration sometimes pick up undesirable signals that, in turn, cause the system to exhibit hum and noise at low volume levels. The proposed feedback-type volume control reduces hum and noise pick-up by reducing the gain of the system rather than the signal level, and thus eliminates the cost of shielding the leads.

### Types of Volume Controls

Fig.1 shows a conventional or "losser" type of volume control that is susceptible to hum and noise. When the input impedance of the amplifier is high, the input voltage $E_i$ and the output voltage $E_o$ depend on the voltage division between resistances $R_1$ and $R_2$. The gain of the amplifier is constant, but the input signal is increased or decreased according to the potentiometer rotation.

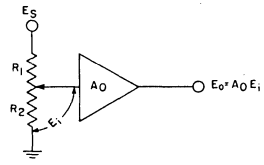



*Fig.1 - Conventional volume-control circuit.*

Fig.2 shows the basic variable-feedback volume control. When the wiper arm of the potentiometer is close to the input terminal, which has a signal input $E_S$, the gain of the system is essentially the open-loop gain $A_O$. As the wiper arm approaches the output terminal, the gain is reduced to a closed-loop value $A_C$ according to the following formula:

$$A_C = \frac{A_O}{1 + \beta A_O}$$

where $\beta$ is the feedback factor.

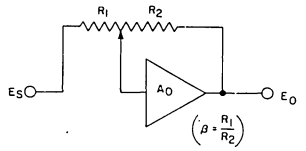



*Fig.2 - A variable-feedback volume-control circuit.*

### Feedback Control

Fig.3 shows the equivalent circuit of a feedback control. Gain control in this circuit is provided by the potentiometer, which varies according to the resistance ratio of $R_S$ and $R_f$. The system gain $E_O/E_S$ for this circuit can be described by the following equation:

$$\frac{E_o}{E_S} = \frac{G_S\left(1-\frac{g_m}{G_f}\right)}{\left(G_S + G_i\right)\left(1+\frac{G_L}{G_f}\right) + g_m + G_L} \qquad (1)$$

where $E_O$ and $E_S$ are the output and input signal levels, respectively; $g_m$ is the transconductance of the amplifier device; and $G_S$, $G_f$, $G_i$, and $G_L$ are the conductances of the source, feedback, input, and load resistances, respectively.

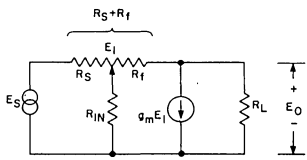



*Fig.3 - Equivalent circuit of a feedback volume control.*

When the control is set for maximum gain ($R_S = 0$; $G_S = \infty$), the system reduces to the following expression:

$$\frac{E_o}{E_S} = \frac{G_f - g_m}{G_f + G_L} = \frac{R_L - g_m R_f R_L}{R_L + R_f} \qquad (2)$$

At the minimum-gain setting, the gain of the system is given by

$$\frac{E_o}{E_S} = \frac{1}{1+\frac{1}{G_S}\left(G_i+G_L+g_m\right)} = \frac{1}{1+R_S\left(\frac{1}{R_i}+\frac{1}{R_L}+g_m\right)} \qquad (3)$$

The resistance $R_f$ of Eq.(2) and the resistance $R_S$ of Eq.(3) are the same because they represent the total resistance of the volume-control potentiometer. If the value of $R_f$ in Eq.(2) is made large with respect to the load resistance $R_L$, the gain and maximum volume reduce to the familiar expression $g_m R_L$.

Eq.(3) shows that the gain of the system is not zero at the minimum volume setting. For both the RCA-CA3041 and CA3042 integrated circuits, typical values encountered indicate that the expression is dominated by the transconductance $g_m$. Substitution of typical values in Eq.(3) shows that the minimum-voltage gain of a 0.25-megohm volume control is of the order of 98 dB and 136 dB below the maximum gain for the RCA-CA3041 and CA3042 circuits, respectively, which is well below the normally acceptable residual levels.

### Loudness Contouring

A desirable feature of audio systems in which low-frequency overload may be encountered is bass roll-off at high volume levels. The low-frequency overload may result because of limited amplifier power output or an inadequate loudspeaker. In either case, an unpleasant "honking" can be avoided by use of variable low-frequency cut-off. This cut-off is achieved by use of the characteristics of the circuit shown in Fig.3. The input impedance $Z_i$ of the system, as shown in Fig.3, is as follows:

$$Z_i = R_S + \frac{1 + G_L R_f}{G_i + G_L + g_m + G_i G_L R_f} \qquad (4)$$

If the total resistance of the volume-control potentiometer is denoted by $R_V$, the input impedance at minimum volume $Z_i$ (min) is given by

$$Z_i(\text{min}) = R_V + \frac{1}{G_i + G_L + g_m} \approx R_V \qquad (5)$$

At maximum volume, the input impedance $Z_i$ (max) changes to the following expression:

$$Z_i(\text{max}) = \frac{1 + G_L R_V}{G_i + G_L + g_m + G_i G_L R_L} \qquad (6)$$

Thus, the input coupling capacitor can be selected to roll off at the desired frequency at maximum volume with assurance that at lower volumes the lower frequencies will be enhanced. With typical device parameter values of the CA3041 or CA3042, the input impedance reduces to approximately 10,000 ohms at maximum volume. When the CA3041 and CA3042 are used in the circuits shown in Figs.4 through 8, the input impedance at minimum volume is essentially the resistance of the volume control used.

Fig.4 shows a diagram of a feedback-type volume-control circuit for the CA3041. This circuit offers enhanced power output and gain as compared to a conventional "losser" type of volume-control-circuit such as that shown in Fig.5. At a carrier frequency of 4.5 MHz, the circuit provides one watt of power output at ±8.5-kHz deviation. In this circuit, the coupling capacitor and the resistor to the grid of the output tube are eliminated. This arrangement offers cost savings because it uses fewer parts and is easier to assemble.

Fig.6 shows a circuit in which the CA3042 is used in a feedback control. The circuit shown in Fig.6 can provide 2 watts of audio power output at ±7-kHz maximum

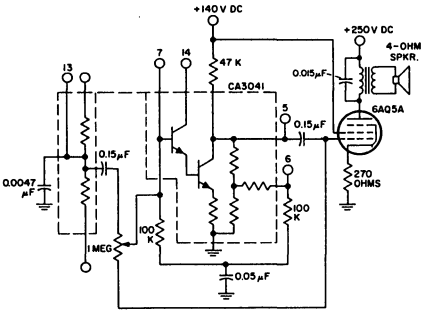



*Fig.4 - A feedback volume-control circuit for the RCA-CA3041.*

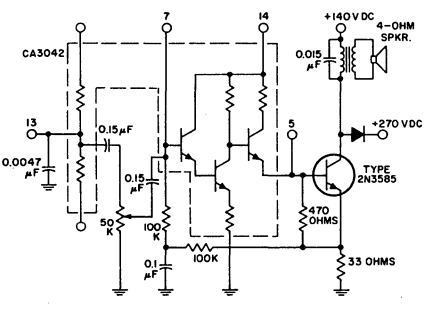



*Fig.7 - A conventional volume-control circuit for the RCA-CA3042.*

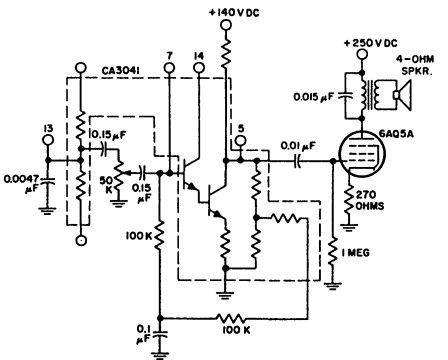



*Fig.5 - A conventional volume-control circuit for the RCA-CA3041.*

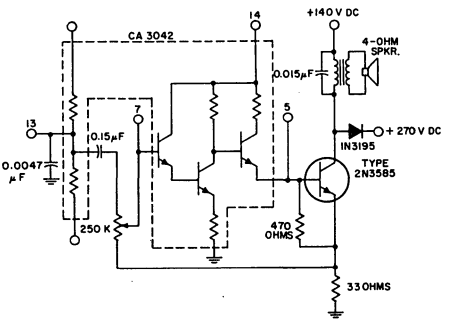



*Fig.8 - A low-cost feedback volume-control circuit for the RCA-CA3042.*

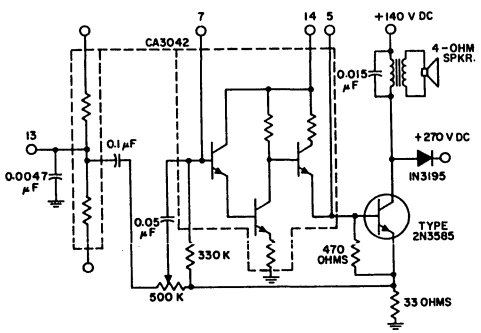



*Fig.6 - A feedback volume-control circuit for the RCA-CA3042.*

frequency deviation from the 4.5-MHz carrier. This circuit costs less than a conventional circuit such as that shown in Fig.7 because it uses smaller coupling capacitors.

Fig.8 shows a very-low-cost circuit that provides essentially the same performance as the circuit shown in Fig.6. An additional capacitor and resistor are eliminated in this circuit. Although a steady-state current flows through the volume control, it is limited to about 1.5 microamperes under worst-case conditions. Because of the small but finite current flowing through $R_1$, the current shifts in the output transistor as the control is rotated from minimum to maximum. The current deviation is ±6 milliamperes maximum about the nominal value, and the flow is in a direction that reduces current at low volume and increases it at high volume.

### Tapers

Because the gain of the system, rather than the input signal, is varied, the volume taper of a feedback

control is characteristically different from that of a conventional "losser" type of control. Therefore, Eq.(1) can be rewritten as follows:

$$\frac{E_o}{E_s} = \frac{1 - a g_m R_v}{1 + (1-a) G_i R_v (1 + a R_v G_L) + R_v G_L + g_m (1-a)} \quad (7)$$

where the term $R_f$ of Eq.(1) is replaced by $(a R_v)$ and $R_s$ is replaced by $(1-a)R_v$. The gain then becomes a function of the term a, which expresses the taper of the control. Curves of this equation for various tapers are shown in Fig.9.

The exponential functions of the taper factor, a, actually define the familiar logarithmic tapers; however, they are arranged counterclockwise so that, as the control is rotated clockwise, the resistance increases very rapidly at first and then more slowly toward maximum resistance. A linear taper (bottom curve of Fig.9) exhibits almost a step-function response, while the parabolic taper is slightly smoother. Clockwise log tapers fall below the linear-taper curve, and are thus totally unacceptable. The controls which are probably most satisfactory are those which correspond to very-low-percentage counterclockwise log tapers.*

* The percentage taper is calculated as follows:

$$\frac{R_{\text{(measured from start of control to wiper arm)}}}{\text{Total resistance}} \times 100,$$

The measurement is taken at 50-per-cent rotation of the control.

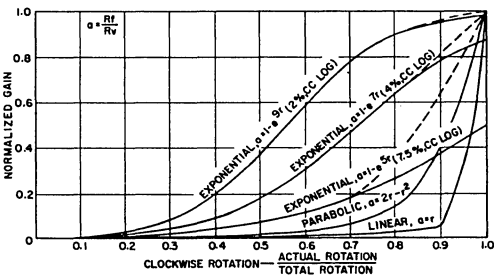



*Fig.9 - Gain as a function of rotation for various types of potentiometers.*

# Principal Features and Applications of the RCA-CA3040 Integrated-Circuit Wideband Amplifier

by
W. M. Austin

The RCA-CA3040 is a monolithic integrated circuit designed for use in wideband video and intermediate-frequency amplifier applications to frequencies as high as 100 MHz. The device, offered in a 12-pin TO-5 package, features a balanced differential voltage gain of 37 dB with less than 1 dB of imbalance and provides a typical 3-dB bandwidth of 55 MHz. Useful voltage gain is well beyond the 3-dB frequency roll-off point which, in some applications, extends to frequencies up to 200 MHz. Additional features of the CA3040 include temperature compensation for gain and voltage over the -55 to 125°C temperature range, a choice of zero or 180-degree phase shift from input to output terminals, and high input and low output impedance characteristics over a broad bandwidth. This Note describes the operation of the CA3040, its electrical characteristics and ratings, and its primary application as a wideband amplifier.

## CIRCUIT DESCRIPTION

Fig. 1 shows the schematic diagram for the CA3040 circuit. The heart of this circuit consists of two differentially connected cascode amplifiers that form a so-called "differential cascode" amplifier. The transistors $Q_3$ and $Q_4$ are common-emitter amplifiers which are connected at the emitters to form the differential transfer junction. The common-base transistors $Q_5$ and $Q_6$ are emitter-driven from the common-emitter transistors $Q_3$ and $Q_4$, respectively, to form two differential-cascode amplifier pairs.

Each common-emitter amplifier is buffer-isolated from the input terminals by an emitter-follower stage for high input impedance and minimum co-channel phase pulling. Each common-base amplifier of the cascode is coupled to the output terminals by use of an emitter-follower stage for low impedance at the output terminals.

When the signal flow through the device is from terminal 4 to terminal 12 and from terminal 6 to terminal 10, there is a 180-degree internal phase shift; when signal flow is from terminal 4 to terminal 10 and from terminal 6 to terminal 12, the phase shift is zero. Fig. 2 shows a signal-flow diagram for the former case. The dc feedback loop shown is a bias-selection and temperature-tracking network. The bias network consists of reference diodes $D_1$ and $D_2$, transistor $Q_9$, and resistors $R_3$,

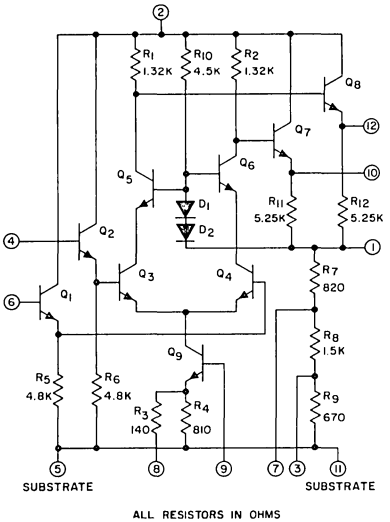



*Fig. 1 – Schematic diagram of the CA3040 wideband amplifier.*

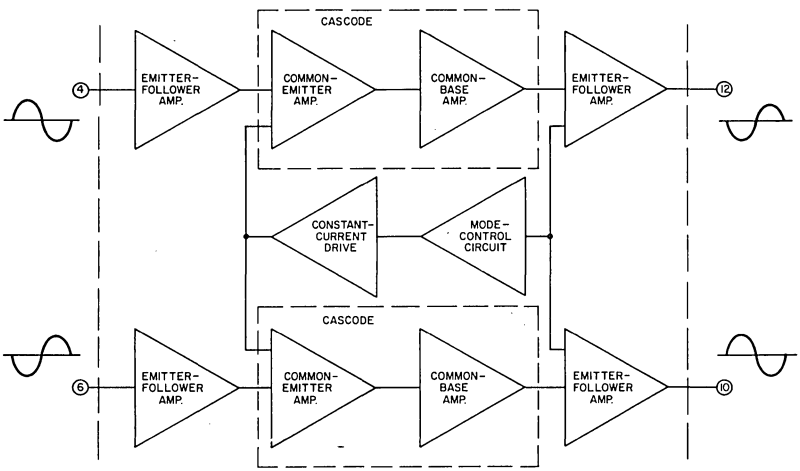



*Fig. 2 – Signal-flow diagram of the CA3040.*

$R_4$, $R_7$, $R_8$, $R_9$, and $R_{10}$. The bias network selected by proper connection of terminals 3, 7, 8, and 9 determines the "mode" of desired temperature tracking.

## BIAS MODES

The dc bias-point stability or ac gain stability of the CA3040 is maintained over the temperature range of -55 to 125°C by the choice of two bias modes. These bias modes are selected by proper connection of the transistor $Q_9$ biasing network. Fig. 3 shows the bias modes for (a) constant voltage and (b) constant gain.

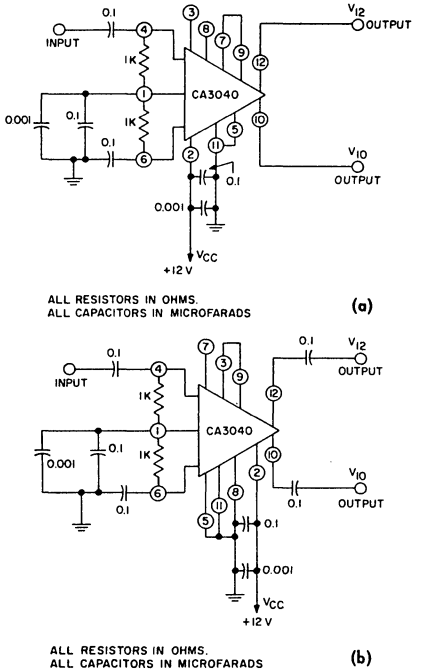



***Fig. 3 – Bias configurations for the CA3040 using a single 12-volt power supply: (a) constant-voltage bias; (b) constant-gain bias.***

In the constant-voltage bias arrangement, terminals 3 and 8 are open, and terminals 7 and 9 are externally connected. This circuit yields a constant-voltage output for applications that use dc coupling to succeeding stages or that require maximum dynamic range over the specified temperature. DC voltage variation in this mode is less than 0.1 volt over the entire temperature range; ac gain variation is ± 2.0 dB.

In the constant-gain bias arrangement, terminals 3 and 9 are externally connected, terminal 7 is open, and terminal 8 is externally connected to the substrate terminals 5 and 11. In this mode, the ac gain is extremely stable (typical variation is 0 dB); the dc variation at the output terminals is ± 0.8 volt.

For most applications, the constant-voltage bias mode is preferred. This mode provides typical ac-gain variation of less than 0.5 dB over the range from room temperature (25°C) to 85°C ambient. The dynamic range in this mode remains high, and the circuit exhibits less distortion and greater common-mode range for large-signal output swings. Finally, this mode requires one less terminal connection and provides a less complex layout design than that required for the constant-gain circuit.

Both modes have identical power-supply requirements, as illustrated in Figs. 3 and 4. Fig. 3 shows the use of a single 12-volt power supply, and Fig. 4

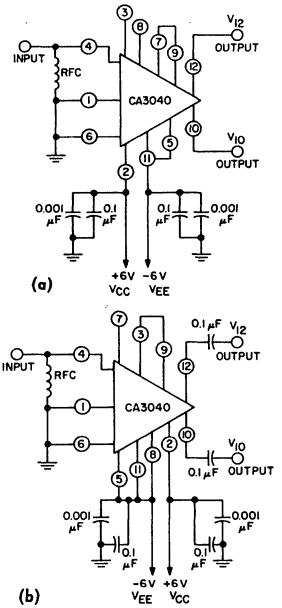



***Fig. 4 – Bias configurations for the CA3040 using balanced dual (±6-volt) power supplies; (a) constant-voltage bias; (b) constant-gain bias.***

shows balanced dual positive and negative 6-volt power supplies. In Fig. 3(a) and 3(b), the inputs are bias-coupled to terminal 1, which is a reference to the center point of the power supply. Although this connection is most commonly used to maintain the common-mode range, any dc supply or "stiff" bleeder (at one-half the power-supply voltage) may be used. It should be noted that terminal 1 should not be direct-coupled to any external

circuit except as a bias source; otherwise, the input transistors or the temperature-compensation characteristic will not remain within the limits.

## CHARACTERISTICS AND RATINGS

The high-frequency capability of the CA3040 is a characteristic of the advanced design that has been developed in the second generation of monolithic integrated-circuit devices. The following are typical performance characteristics of the CA3040.

Fig. 5(a) shows gain as a function of frequency for the CA3040. The test circuit used to obtain this curve is shown in Fig. 5(b). The 3-dB bandwidth is typically 55 MHz and the minimum is 40 MHz at either differential output when terminal 4 is driven from a single-ended 50-ohm source. At 1 MHz, using a 63-millivolt output level, imbalance is not greater than ± 1 dB. In contrast

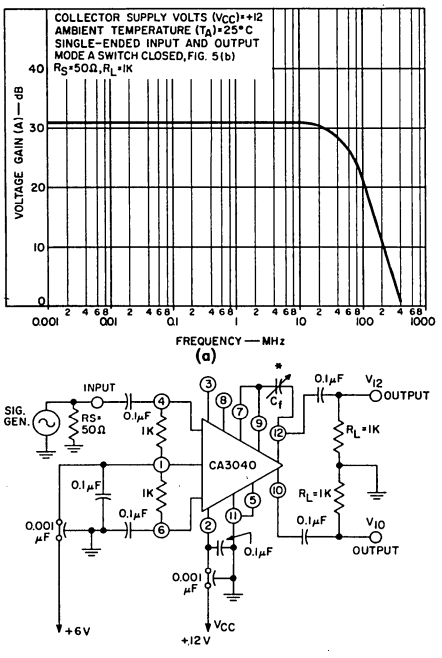



*Fig. 5 – (a) Voltage gain as a function of frequency and (b) test circuit of CA3040.*

to the more common specification of minimum gain at high frequency, the performance of the CA3040 is given in terms of flat bandwidth relative to the 1-MHz-gain test point.

Fig. 6(a) shows the input resistance and capacitance characteristics of the CA3040. (The input resistance $R_{IN}$ is plotted as conductance $G_{IN}$ because the resistance magnitude approaches infinity at approximately 22 MHz.) The test circuit used to obtain these data is shown in Fig. 6(b). These curves were obtained

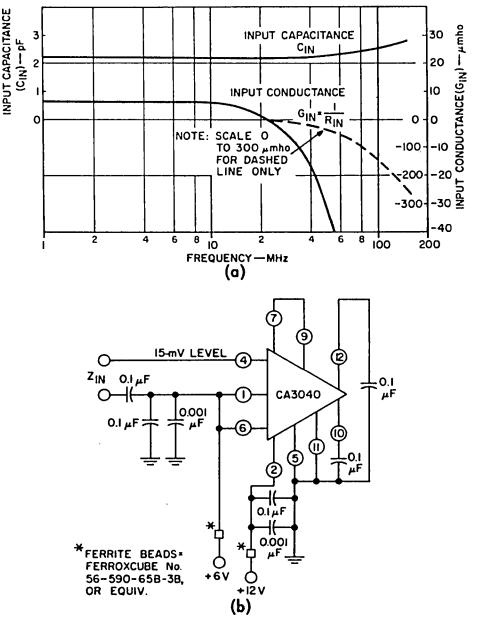


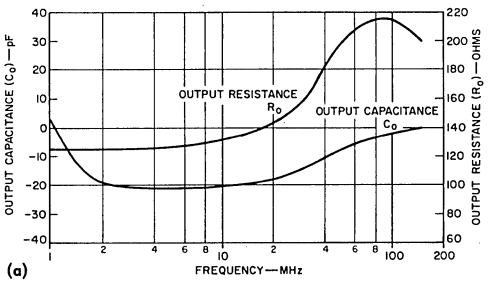

*Fig. 6 – (a) Input impedance characteristics and (b) test circuit of CA3040.*

with the output terminals shorted and by use of the constant-voltage bias configuration. Although this form of bias has a second-order effect on the input and output capacitance, the input and output capacitance and conductance values for the circuits of Figs. 3 and 4 do not change appreciably from those shown in Fig. 6(a). The negative value of input resistance remains high over the high-gain region and has sufficient magnitude (several thousand ohms) at 150 MHz so that the amplifier remains stable for practical values of the input matching impedance. From 1 to 10 MHz, this resistance remains approximately 150 kilohms. The input capacitance $C_{IN}$ of the CA3040 is approximately 2.2 picofarads and remains relatively constant over the useful frequency range.

Fig. 7(a) shows the output resistance and output capacitance of the CA3040 amplifier as a function of frequency. The test circuit used for these measurements is shown in Fig. 7(b). The output resistance of the cir-

ciut is approximately 125 ohms at low frequencies and gradually rises to 215 ohms at 100 MHz, but decreases again to 200 ohms at 150 MHz. Although a lower output impedance (50 ohms or less) is more desirable, the higher output impedance results in greater temperature-stable gain. When necessary, however, the output impedance can be reduced by addition of another emitter-follower stage. Even when this stage is directly coupled to the output, it has little effect on the dc stability for bias-current drains less than 0.1 milliampere.

Fig. 8(a) shows the 30-MHz noise figure as a function of source resistance in the test circuit presented in Fig. 8(b). This amplifier is similar to the constant-voltage bias circuit shown in Fig. 4(a). The gain and frequency response of the amplifiers are equivalent. The 1-kilohm resistors at the input stage of the circuit of Fig. 5(a), however, produce a 2-dB increase in the noise figure when the CA3040 is matched for maximum power transfer. For low-noise applications, therefore, these shunt-biasing resistors should be replaced by low-loss input matching circuits which can include rf chokes, a transformer, or inductive-capacitive input circuits. It is important that the dc resistances of the two stages remain equal. An unequal dc voltage drop across the bias network produces a large dc offset at the output.



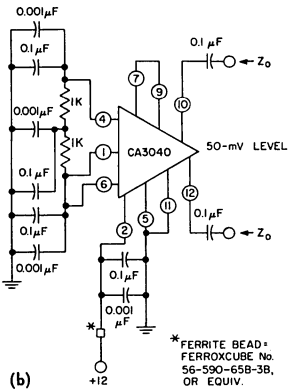
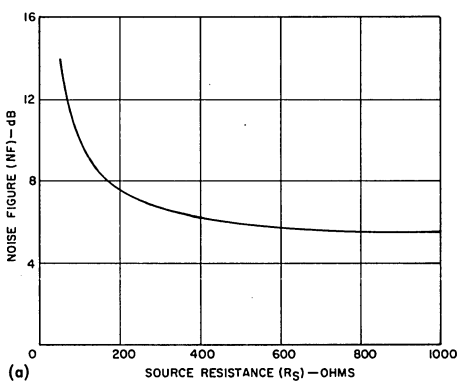




*Fig. 7 – (a) Output impedance characteristics and (b) test circuit of CA3040.*



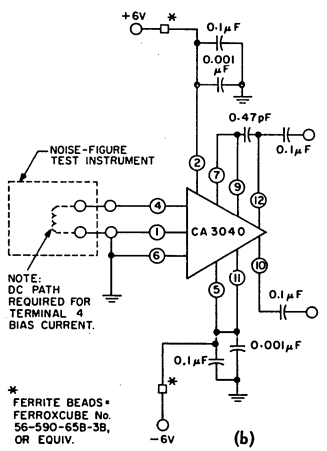
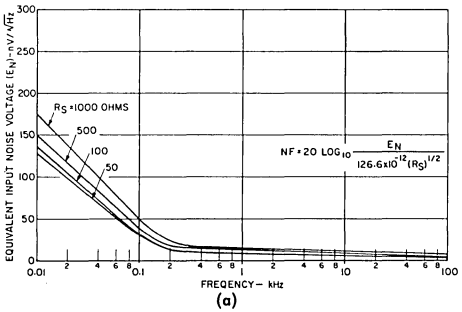




*Fig. 8. – (a) Typical 30-MHz noise figure and (b) test circuit of CA3040.*

Fig. 9(a) shows the 1/f noise characteristics of the CA3040 in the test-amplifier circuit of Fig. 9(b). The curves represent different values of source resistance. The bandwidth of the test amplifier circuit is restricted to adapt the circuit to a Quan-Tech noise analyzer. The equivalent input 1/f noise is expressed in nanovolts per



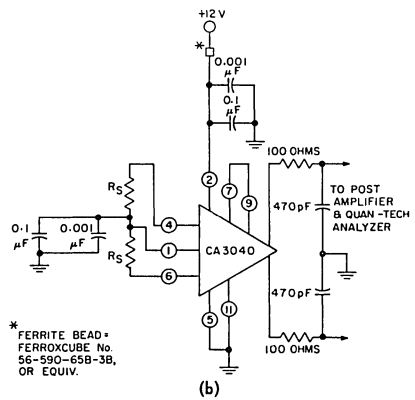




*Fig. 9 – (a) Equivalent input noise voltage as a function of frequency and (b) test circuit of CA3040.*

square root of the frequency. The limiting low-frequency 1/f noise approaches 125 nanovolts per $\sqrt{Hz}$ at 10 Hz and drops to approximately 25 nanovolts per $\sqrt{Hz}$ at 100 Hz. Above 200 Hz, the noise component is primarily shot noise.

The noise figure NF is related to the noise voltage $E_N$ as follows:

$$NF = 20 \log_{10} \frac{E_N}{(4KTR_S)^{1/2}} = 20 \log_{10} \frac{E_N}{126.6 \times 10\text{-}12\ (R_S)^{1/2}},$$

where $E_N$ is the noise voltage in volts per $\sqrt{Hz}$, K is Boltzmann's constant ($1.38 \times 10^{-23}$ joule/°K), T is the temperature in degrees Kelvin, and $R_S$ is the external source resistance in ohms.

The CA3040 has a linear phase-shift characteristic. Fig. 10 shows the amplifier phase shift from input terminal 6 to output terminal 10 and the differential phase between outputs over the frequency range from 1 to 60 MHz. The test amplifier of Fig. 5(b) was used to obtain the data for these curves. The resistive portion of the output-impedance load in Fig. 5(b) consists primarily of the 1-kilohm resistors. The capacitive load consists of all essential circuitry as well as BNC connectors and phase-meter input probes that represent approximately 8.5 picofarads. Any imbalance from 180 degrees of differential phase at the output terminals remains small in comparison to the reference input-to-output phase shift and is typically less than 1 degree at frequencies up to 50 MHz. Fig. 10 shows the differential output phase

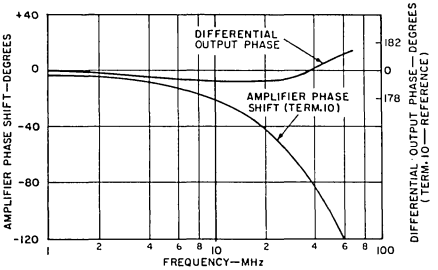



*Fig. 10 – Amplifier phase shift and differential output phase as a function of frequency for the CA3040 test circuit of Fig. 5(b).*

with terminal 10 given as the reference phase. The imbalance exists because the feedthrough capacitance from terminal 10 to terminal 9 is greater than that from terminal 12 to terminal 9. The constant-current transistor ($Q_9$ of Fig. 1) amplifies this unbalanced stray capacitance coupling. A fundamental correction for phase can be made by adjustment of the output-capacitance load. In Fig. 5(b), a variable capacitance $C_f$ is used between terminals 9 and 12 for this purpose. The addition of $C_f$ makes possible adjustment of the output signals for phase and gain balance at the high-frequency roll-off point.

Fig. 11(a) shows the frequency response of the CA3040 for various values of load resistance. The test circuit used for these measurements is shown in Fig. 11(b). This amplifier is biased from a balanced dual power supply, but is otherwise similar to the circuit of Fig. 5(b). The curves are valid for either method of biasing.

The low-frequency portion of the curves of Fig. 11(a) shows the decrease in gain with decreased load resistance which is characteristic of the 125-ohm output resistance. The higher-frequency range shows the reduction in bandwidth as the load resistance is decreased.

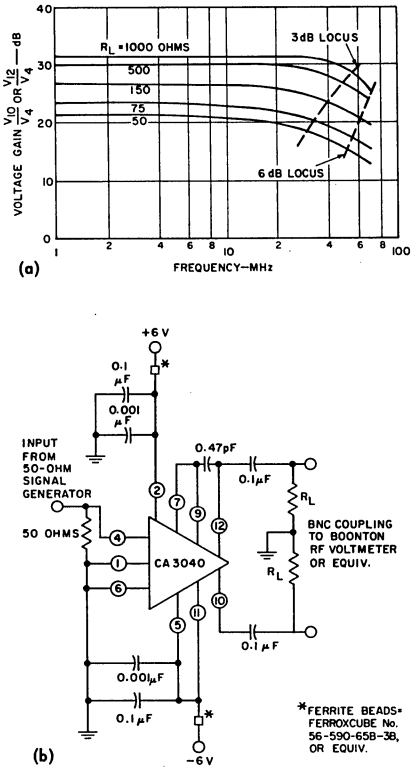



*Fig. 11 – (a) Frequency response curves and (b) test circuit for CA3040.*

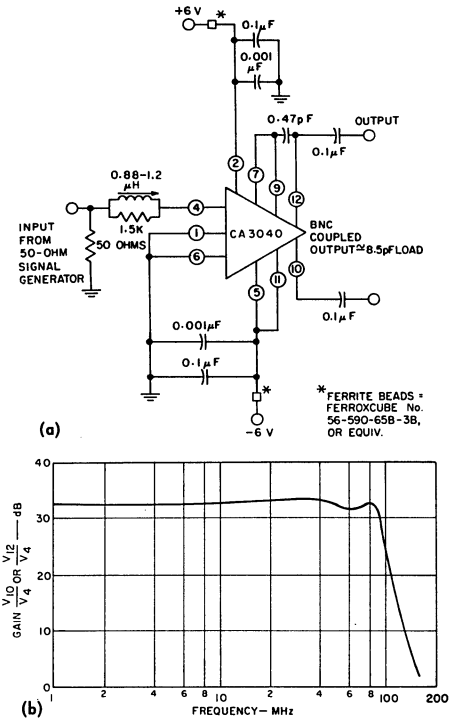



*Fig. 12 – (a) Typical CA3040 wideband-amplifier circuit with series input peaking and (b) frequency response characteristic.*

This output characteristic is typical of emitter-follower circuits and is caused by a reduction in transistor beta at higher frequencies.

## WIDEBAND AMPLIFIERS

In the basic amplifier circuit of Figs. 5(b) and 11(b), the bandwidth of the CA3040 may be increased by use of conventional RL and RC peaking, as well as feedback correction, at the input and output stages. Fig. 12(a) shows a typical wideband amplifier configuration using the CA3040; Fig. 12(b) shows its frequency response. The circuit has a wide-band series-peaked bandwidth greater than 90 MHz at the 3-dB point and greater than 85 MHz to within ±1 dB of gain variation. In the circuit of Fig. 12(a), care is taken to avoid "over-peaking" of the input at higher signal levels so that limiting and distortion effects are minimized.

The frequency-response curves shown in Fig. 12(b), as well as in Figs. 5(a) and 11(a), were obtained with conventional output circuits that contain BNC connectors coupled to the rf voltmeters and produce a total capacitive load of approximately 8 to 9 picofarads. The curve of Fig. 5(a) shows a roll-off characteristic of approximately 12 dB per octave in the 100-to-200-MHz range which is the result of capacitive loading of the cascode and emitter-follower output stages. These output stages may be peaked for partial compensation of the bandwidth loss that results from emitter-follower output loading. The remaining loss in bandwidth, however, results from internal circuit effects and is less easily corrected.

Fig. 13 (a) shows a wideband-amplifier circuit that produces 50 dB ± 1 dB of gain up to 53MHz, as shown by the curve of Fig. 13 (b). The curve shown is for an input-drive signal of 1.0 millivolt rms although the post amplifier can provide an output of 1.0 volt rms before limiting. The post amplifier has a broadband

capability of approximately 85 MHz and uses adjustable rf coils, Miller Type 20A__RBI, or equivalent. The adjustable capacitor at the emitter or the cascode serves to "over peak" the post amplifier and compensate for the RC roll-off of the CA3040 amplifier. With this type of peaking compensation, a flat response that deviates less than 0.2 dB up to 50 MHz is obtained. Wideband capability of the post amplifier is also achieved through the use of high-performance silicon n-p-n transistors. The RCA-40235 has a high gain-bandwidth product $f_T$ and a low collector-to-base feedback capacitance $C_{cb}$ suitable for television rf applications. The 2N5187 is a high-speed switching transistor that has all the basic requirements for economical line-driver applications. The peaking circuit is of the series-shunt type at the collector of the RCA-40235 cascode. Because high idle current is needed in the amplifier output stage, the output level before limiting is set for the minimum requirement necessary for the desired level of peak-to-peak output signal. In this case, a peak-to-peak signal of 2 volts is easily obtained to drive a 50-ohm line that is matched at both ends.

The CA3040 amplifier in Fig. 13(a) is the same as the amplifier of Fig. 5(a), although the basic circuit can use any bias mode or power-supply configuration shown previously. In this particular case, the simple 12-volt power supply (at approximately 60 milliamperes of current drain) satisfies the requirement for a low-cost, wideband circuit. However, when several supply voltages are available, the circuit of Fig. 13(a) can be a direct-coupled combination of the balanced dual ±6-volt CA3040 circuit and the post amplifier. This post amplifier which uses RCA-40235 transistors in a cascode configuration, is designed for dc base voltages of 3 and 6 volts.

## STABILITY

In the classical analysis, stability is evaluated as a function of the transfer impedance parameter. The number of possible operating modes and bias options, each of which is evaluated over the useful frequency range, limits the practicality of this type of analysis for the CA3040. Such an analysis would be further comp-

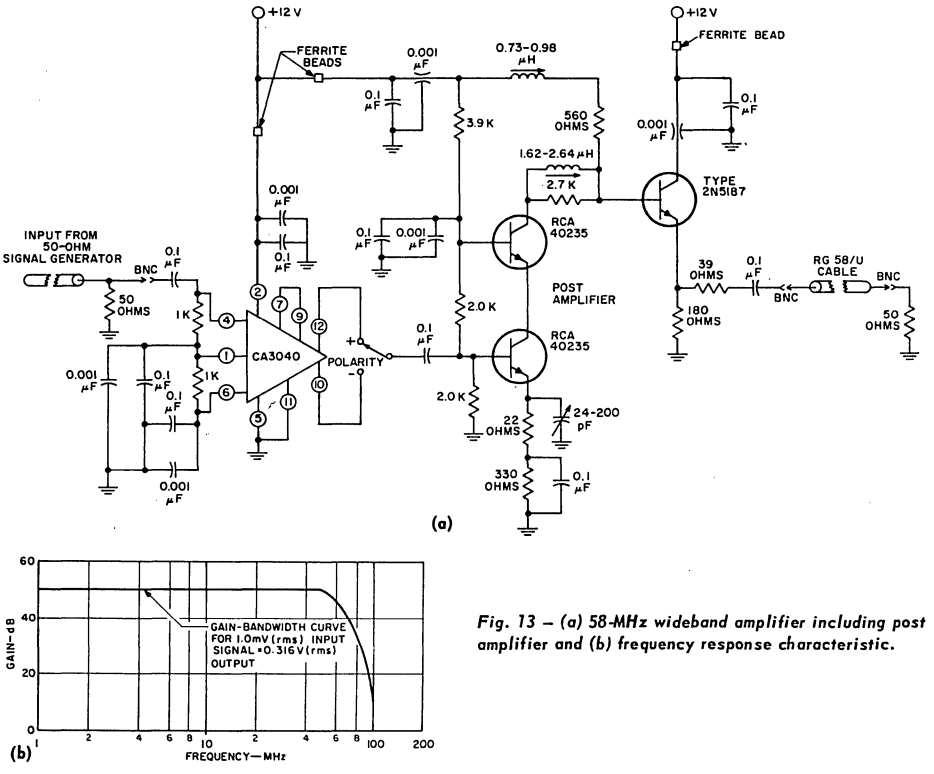



*Fig. 13 – (a) 58-MHz wideband amplifier including post amplifier and (b) frequency response characteristic.*

licated by the fact that y-parameter data are applicable only at the discrete frequency at which they are taken. In view of these factors, the characteristics of the CA-3040 are guaranteed to have a reasonable stability margin through evaluations in test circuits and by integrity of design. Poor circuit design or improper layout, however, can reduce the stability margin so that oscillations can possibly result.

The differential-amplifier configuration of the CA-3040 offers the advantage in wideband amplifier applications of neutralizing its own feedback. For this reason the circuit layout and printed-board pattern should be designed with a high degree of symmetry.

For stability purposes, terminal 9 of the CA3040 should not be bypassed because common-base oscillations may result in the constant-current transistor $Q_9$. This effect, however, may be used to advantage in oscillator and mixing applications.

For some applications, such as wideband if amplifiers, it is desirable to limit the high-frequency characteristics of the CA3040. In this case, series resistors in the base input leads of transistors $Q_1$ and $Q_2$ are recommended. Resistances of 10 to 100 ohms in series with terminals 4 and 6 not only limit the bandwidth but also act as parasitic suppressors.

## CONSTRUCTION

The basic construction of the CA3040 generally follows the usual recommendations for high-frequency wideband amplifiers. Figs. 14 and 15 illustrate the

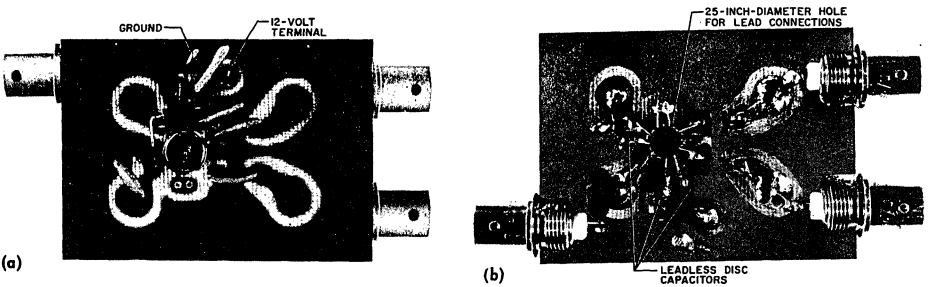



*Fig. 14 – Printed-circuit board for the CA3040 wideband amplifier circuit of Fig. 5(b) using constant-voltage bias configuration and a single 12-volt power supply: (a) top view; (b) bottom view.*

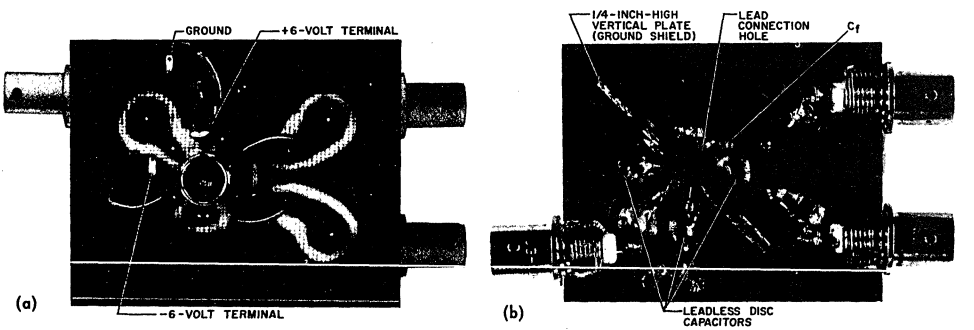
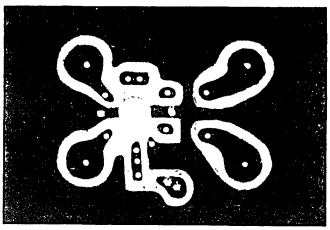
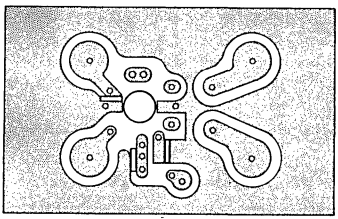



*Fig. 15 – Printed-circuit board for the CA3040 wideband amplifier circuit of Fig. 8(b) using constant-gain bias configuration and balanced dual (±6-volt) power supplies; (a) top view; (b) bottom view.*

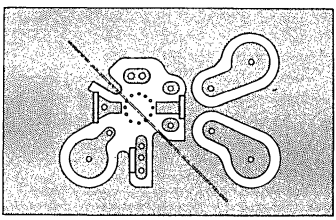
printed-board layout used for wideband applications of the CA3040. Fig. 16(a) is an exact-scale photograph of the printed board used in the circuits of Figs. 14 and 15. Figs. 16(b) and 16(c) show modifications in this board made to accommodate the different connections for the single 12-volt and balanced dual 6-volt power supplies. Fig. 16(c) shows an alternate mounting arrangement for the CA3040 in which lead connections are made through individual holes in the printed board. The printed board layout is intended for use with the constant-voltage bias connection in which terminal 7 is connected to terminal 9. Before the CA3040 is mounted, the pins for terminals 3 and 8 are cut off because they are not used in these circuits.



(a)



(b)



(c)

*Fig. 16 – Printed-circuit board used for the construction of wideband amplifier circuits shown in this Note: (a) exact-scale photograph; (b) modifications required to accommodate connections for the single 12-volt dc supply; (c) modifications required to accommodate connections for balanced dual 6-volt supplies.*

The balanced dual-power-supply circuit of Fig. 15 requires greater attention to layout because of the additional difficulty in bypassing the negative supply. The emitter circuits, as well as the substrate and case, of the CA3040 are common to the negative supply terminals 5 and 11. This arrangement permits the negative power-supply source impedance to become a common element for feedback. For wideband applications, however, this arrangement presents a problem for bypassing these circuit elements. The series lead inductance L in microhenries is given by

$$L = 0.005\ell\left[2.3\log_{10}\left(\frac{4\ell}{d}-0.75\right)\right]$$

where $\ell$ is the lead length and d is the lead diameter, both in inches.

Because this inductance is appreciable for some values of bypass capacitance, the circuit may resonate within the bandwidth of the amplifier. This resonance always exists and, therefore, requires extensive bypassing. As a result, the use of two and sometimes three capacitors at a bypass point is necessary for adequate bypassing of all frequencies in the pass band. In addition, the use of ferrite beads, chokes, and resistors may be necessary for suppression of "ripples" or "suck-out" in the pass band. Because of these problems a knowledge of the high-frequency self-resonant characteristics of passive circuit components up to frequencies near the unity-gain point of the amplifier device is essential. For the CA3040, this frequency may reach 800 MHz.

As an added precaution in minimizing inductance, the leads of the CA3040 should be trimmed to the minimum practical length. Lead trimming, forming, and soldering, however, should be performed at least 1/32 inch from the case to avoid damage to the package. Each lead of the CA3040 is inserted through a hole which has a sufficiently large diameter so that the lead just passes through without forcing. The leads are then folded out and soldered to their respective connections. Leadless disc capacitors are used with the circuit board slotted at the closest bypass point. The capacitors are soldered directly in vertical position to the printed board.

Fig. 17 shows the constructed wideband post amplifier in which most parts are easily identifiable. Because the case and collector lead of each 2N5187 transistor are connected together, direct bypassing to the case was used in this particular layout to reduce lead inductance in the collector circuit of the 2N5187. Leadless disc capacitors are used at critical bypass points. The terminal tie-points are teflon-insulated stand-offs. Input and output are shown as BNC connectors coupled by 0.1-microfarad disc capacitors. The output cable and 50-ohm load of Fig. 13(a) are not shown.

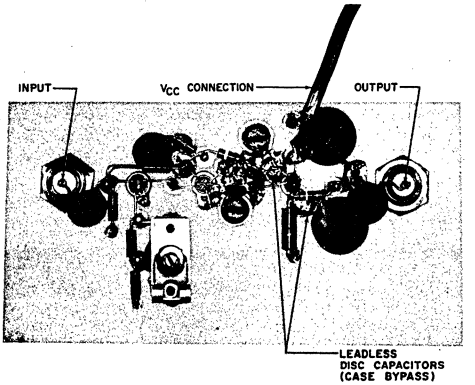



*Fig. 17 – Photograph of constructed post amplifier of Fig. 13(a).*

# An IC for AM Radio Applications

by
L. Baar
RCA Solid State Division
Somerville, N. J.

An integrated circuit intended to be used in AM radio applications can assume many forms depending on the class of service in which it is to be used. The RCA-CA3088E is designed for use in high-quality AM superheterodyne receivers. It provides the basic functions of signal conversion, if amplification, detection, and audio preamplification sufficient to drive a separate power amplifier. Auxiliary functions supplied are: a supply-voltage regulator, internal agc for the first if amplifier, agc voltage for an optional external rf stage, and an amplified signal to drive a tuning-meter output. This device is housed in a 16-lead dual-in-line plastic package.

While the circuit design is intended for use in commercial AM broadcast receivers, it is equally suited for use in most AM receiver applications up to a frequency of 30 MHz. In addition, since most functions are externally accessible this device is also a general-purpose amplifier array. The possible number and variety of uses of the CA3088E are largely a function of the needs and imagination of the designer.

## INTEGRATED CIRCUIT DESCRIPTION

The schematic diagram of the RCA-CA3088E is shown in Fig. 1. The correspondence of terminals to functional section within the device is shown in Table I. The various stages are designated in terms of AM-radio functions because the primary functions of the device are so intended; the AM-radio terminology is continued throughout the paper for the sake of continuity.

The heart of this integrated circuit is the second if amplifier-detector combination. The if amplifier consists of Q7, Q9 and Q10 with their associated components. Q7 and Q10 are emitter followers which isolate the gain stage, Q9. The supply voltage to the collectors is regulated by the zener diode, Z1. The quiescent operating point is stabilized by connecting the emitter of Q10 to the base of Q7 through R14. The connection is made by externally tying pin 7 to pin 8 through a suitable impedance. For dc stabilization, pin 7 should be at ac ground

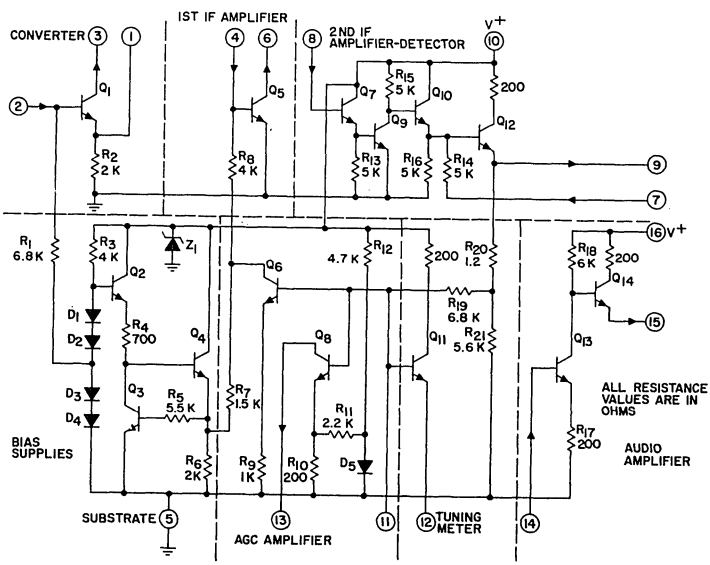



*Fig. 1 — Schematic diagram of the RCA CA3088E.*

TABLE I. CORRESPONDENCE OF TERMINALS TO FUNCTION

| Function | Terminal |
|---|---|
| Converter | 1, 2, 3 |
| First IF Amplifier | 4, 6 |
| Second IF Amplifier-Detector | 7, 8, 9, 10 |
| AGC Amplifier | 11, 13 |
| Tuning-Meter Amplifier | 12 |
| Audio Preamplifier | 14, 15, 16 |

potential, otherwise signal feedback will modify the basic characteristic of the stage. The output of Q10 is fed directly to Q12, an emitter follower operating at a quiescent current of approximately 100 microamperes. This stage becomes a detector by connecting the proper filter circuit to the emitter; the emitter is brought out on pin 9. The rectified emitter current develops a voltage at the junction of R20 and R21; the junction is connected to the bases of the agc and meter amplifiers.

Q11 is an emitter follower normally used to drive a tuning meter at pin 12. Q11 is biased off with no signal and will deliver approximately 150 microamperes with a maximum signal as indicated in the curve of Fig. 2.

Q8 is an agc amplifier intended to control an optional external rf amplifier. Collector voltage, applied through a load resistor to pin 13, provides a decreasing voltage at pin 13 with increasing signal. The voltage drop across diode D5 must be overcome by the drive voltage to the base of Q8, thus introducing a delay in the application of gain control to the rf stage. The agc curve of a typical circuit is shown in Fig. 2.

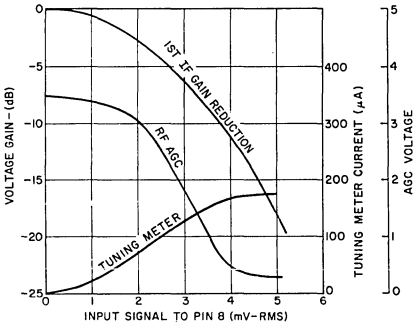



*Fig. 2 — Typical performance curves for the CA3088E.*

Q5 is the first if amplifier and is biased to draw one milliampere of current under zero signal conditions. This condition is set by the biasing circuit of Q2, Q3, Q4 and diodes D1 through D4. A nominal current of one milliampere is established in Q3, which is a mirror of Q5, thus determining the current in Q5. The supply voltage to the biasing circuit is also regulated by Z1. With no signal, Q6 is cut off and has no affect on the operating point of Q5. As signal strength increases and the base drive voltage increases, Q6 conducts some of the base current being applied to Q5 and reduces the collector current and, thus, the gain, as shown in Fig. 2.

Q1 is normally used as a converter stage. It is biased to a nominal current of 0.35 milliampere by diodes D3 and D4 in combination with the source resistor, R2. The emitter is brought out on pin 1; this terminal may be bypassed or may be used to apply a local-oscillator signal to the emitter.

Q13 and Q14 form the audio driver stage, a grounded emitter stage coupled directly to an emitter follower. The emitter follower provides a low-impedance drive for an external audio amplifier. This stage must be externally biased; a convenient method is to feed a portion of the dc potential on the emitter of Q14 to the base of Q13 with the proper network connected between pins 14 and 15. A nominal voltage gain from pin 14 to pin 15 of 30 times is determined by the ratio of resistor R18 to R17.

In addition to the voltage regulation provided by the zener diode, Z1, the circuit is temperature compensated by the bias circuit described previously. Transistors Q1, Q5, and Q13 are large-geometry devices which provide low-noise performance in the CA3088E. All emitter follower stages which have the emitters brought out to external terminals are protected against inadvertently shorted terminals. The size of the chip is 52 mils by 52 mils.

## APPLICATIONS

### AM Broadcast Receivers

When would a designer use the CA3088E as the basic subsystem of an AM radio? The typical low-cost table model or portable radio ordinarily has neither an rf amplifier stage nor a tuning meter; therefore, two features of the CA3088E have no use in simple AM radios. Furthermore, economic considerations make it difficult for integrated devices to compete with discrete devices in these minimal-performance receivers. On the other hand, the high-performance console receiver is an application in which all of the features of the CA3088E are useable. The CA3088E, in which the biasing of most stages is accomplished internally, provides savings in the number of components to be specified, purchased, handled, and connected.

Fig. 3 shows the circuit for a typical AM receiver using the CA3088E. Double-tuned, transformer-coupled circuits are shown here, but any of the other forms of band-pass filters may be used that best suit the needs of the designer. The rf stage may take on any of several forms and so is shown only as a gain block. The intention here is not to present an optimum receiver design, but to show how a specific device, the CA3088E, may be used. Fig 4 shows performance curves obtained in a receiver using the CA3088E in conjunction with an external rf stage.

In addition to commercial broadcast-receiver, a multitude of receiver applications exist in communications equipment of all forms. The CA3088E will suit many of these applications with the extra features available in the circuit. The CA3088E may be used as a straight if amplifier for use with a separate tuner, or it could serve as a subsystem in a double-conversion receiver.

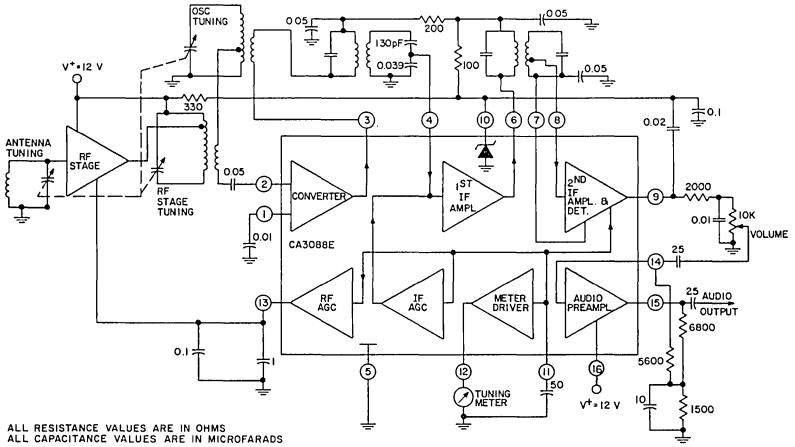



*Fig. 3 — Typical AM broadcast receiver using the CA3088E.*

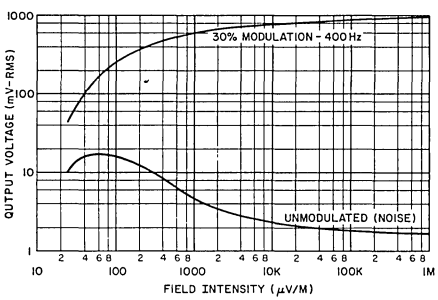



*Fig. 4 — Performance curves for an AM receiver with an rf stage using the CA3088E.*

Amateur radio receivers are a natural for the circuit. Narrow-band or fixed-tuned systems, such as remote control systems, and hand-carried receivers, systems in which the space saving features of an integrated circuit could be important, could make good use of the CA3088E.

### High-Frequency Applications

Many receivers use if amplifiers at the higher frequencies; therefore, the high-frequency characteristics of the CA3088E are important. Table II shows some of the four pole characteristics of the individual signal stages of the CA3088E at 1 MHz and 30 MHz. The forward transconductance is not significantly affected in the frequency range considered.

The high-frequency performance of the second-if-amplifier/detector stage is determined within the chip. Fig. 5 is a plot of the voltage gain of the stage as a function of frequency. The gain is down about 6 decibels at 10 MHz and about 16 decibels

**TABLE II. INPUT AND OUTPUT IMPEDANCE DATA**

| | $C_{IN}$ Picofarads | $C_{OUT}$ Picofarads | $C_{fb}$ Picofarads | 1 MHz $R_i$ Ohms | 30 MHz $R_i$ Ohms | 1 MHz $R_o$ Ohms | 30 MHz $R_o$ Ohms |
|---|---|---|---|---|---|---|---|
| $Q_1$ | 12 | 5 | 1.5 | 3500 | 2000 | 100 K | 9 K |
| $Q_5$ | 17 | 5 | 1.5 | 2000 | 1000 | 100 K | 9 K |
| $Q_7$ | 3.5 | – | – | 75 K | 45 K | – | – |

at 30 MHz. The nominal gain of this stage is 40 decibels; therefore, this stage has considerable gain at these frequencies.

The converter and first-if stages will operate at higher frequencies, but stability considerations will control the practical gain. Calculations of maximum useable gain (MUG) and maximum available gain (MAG), using the data in Table I for the unneutralized single-stage amplifier, show that about 10 decibels of power gain must be sacrificed to maintain good stability at 30 MHz. More gain can be obtained by neutralizing, but at the expense of circuit simplicity.

The audio-preamplifier stage may also be used as another if stage provided that the low-output impedance of the emitter follower is not detrimental to performance. The stage may be used to drive a crystal or ceramic filter in which the typical matching impedances are quite low. The frequency response of this stage is very similar to that of the second-if stage with about 6 decibels drop in gain at 10 MHz. This stage may also be controlled by the output from pin 13 as is the case with the external rf stage.

Fig. 6 shows the circuit of a 10.7 MHz if amplifier using two ceramic filters. This circuit shows how the use of the CA3088E with low-impedance filters can simplify a design. Stability is maintained by the low-impedance terminations used with the filters. The first two stages are coupled together with a single-tuned circuit which provides impedance matching. A

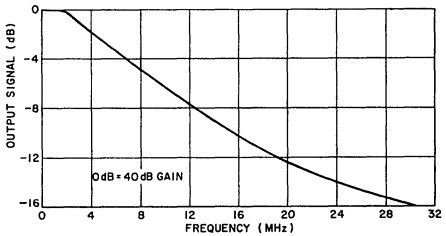



*Fig. 5 – Plot of voltage gain as a function of frequency for the second-if-amplifier/detector stage of a CA3088E.*

50-microvolt input signal with 30-percent modulation produces a detected audio signal of 22 millivolts at the detector output. The audio stage may be used as an audio driver or as an additional if stage to drive the input ceramic filter.

### General-Purpose Amplifier Array

The CA3088E is versatile enough to be used as a general-purpose amplifier array. Q1 and Q5 are internally biased and require only a collector load to produce an amplifier. These devices may be operated to a maximum collector voltage of 16 volts. With the addition of external biasing, the operating points of these stages may be varied from the internally established quiescent point. The second-if-amplifier/ detector combination is biased externally as discussed previously. Q12, which is normally connected as an envelope detector may be connected as another emitter follower by loading resistors R20 and R21 with an external resistor.

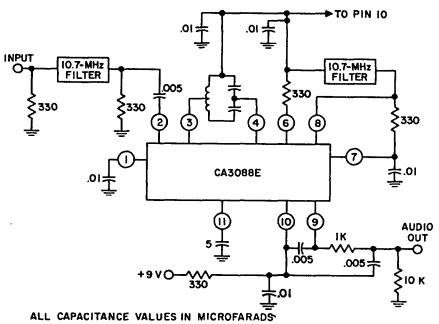



*Fig. 6 – A 10.7-MHz if amplifier using the CA3088E and two ceramic filters.*

The audio preamplifier is independent and biased externally. The gain-control circuits may be used as in the AM-radio applications. If Q12 is not used as a detector, the gain-control voltage can be applied on pin 11. Q11 provides a positive-going voltage with increasing signal and Q8 provides a negative-going voltage.

### Acknowledgements

The author thanks Messrs. Leo Harwood and Max Malchow for their aid and suggestions in discussions concerning this project, and Mr. Frank Curley for his aid in circuit construction and collection of data.

# Some Applications of A Programmable Power Switch/Amplifier

by L. R. Campbell and H. A. Wittlinger

The RCA-CA3094 unique monolithic programmable power switch/amplifier IC consists of a high-gain preamplifier driving a power-output amplifier stage. It can deliver average power of 3 watts or peak power of 10 watts to an external load, and can be operated from either a single or dual power supply. This Note briefly describes the characteristics of the CA3094, and illustrates its use in the following circuit applications:

Class A instrumentations and power amplifiers

Class A driver-amplifier for complementary power transistors

Wide-frequency-range power multivibrators

Current- or voltage-controlled oscillators

Comparators (threshold detectors)

Voltage regulators

Analog timers (long time delays)

Alarm systems

Motor-speed controllers

Thyristor-firing circuits

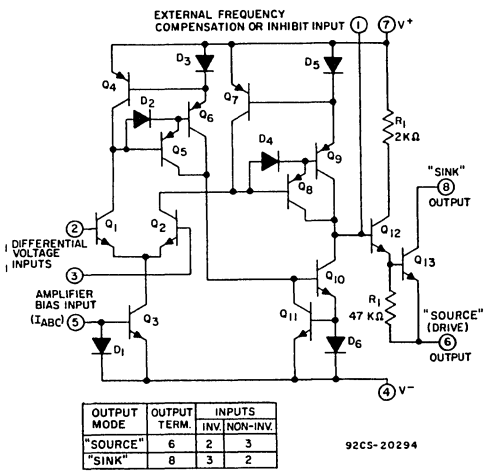
Battery-charger regulator circuits

Ground-fault-interrupter circuits

**Circuit Description**

The CA3094 series of devices offers a unique combination of circuit flexibility and power-handling capability. Although these monolithic IC's dissipate only a few microwatts when quiescent, they have a high current-output capability (100 milliamperes average, 300 milliamperes peak) in the active state, and the premium-grade devices can operate at supply voltages up to 44 volts.

Fig. 1 shows a schematic diagram of the CA3094. The portion of the circuit preceding transistors $Q_{12}$ and $Q_{13}$ is the preamplifier section and is generically similar to that of the RCA-CA3080 Operational Transconductance Amplifier (OTA).[1,2] The CA3094 circuits can be gain-programmed by either digital and/or analog signals applied to a separate Amplifier-Bias-Current ($I_{ABC}$) terminal (No. 5 in Fig. 1) to control circuit sensitivity. Response of the amplifier is essentially linear as a function of the current at terminal 5. This additional signal input "port" provides added flexibility in many applications. Thus, the output of the amplifier is a function of input signals applied differentially at terminals 2 and 3 and/or in a single-ended configuration at terminal 5. The output portion of the monolithic circuit in the CA3094 consists of a Darlington-connected transistor pair with access provided to both the collector and emitter terminals to provide capability to "sink" and/or "source" current.




| OUTPUT MODE | OUTPUT TERM. | INPUTS | |
|---|---|---|---|
| | | INV. | NON-INV. |
| "SOURCE" | 6 | 2 | 3 |
| "SINK" | 8 | 3 | 2 |

*Fig. 1—CA3094 circuit schematic diagram.*

The CA3094 series of circuits consists of six types that differ only in voltage-handling capability and package options, as

shown below; other electrical characteristics are identical.

| Package Options | Maximum Voltage Rating |
|---|---|
| CA3094S; CA3094T | 24 V |
| CA3094AS; CA3094AT | 36 V |
| CA3094BS; CA3094BT | 44 V |

The suffix "S" indicates circuits packaged in TO-5 enclosures with leads formed to an 8-lead dual-in-line configuration (0.1" pin spacing). The suffix "T" indicates circuits packaged in 8-lead TO-5 enclosures with straight leads. The generic CA3094 type designation is used throughout this Note.

### Class A Instrumentation Amplifiers

One of the more difficult instrumentation problems frequently encountered is the conversion of a differential input signal to a single-ended output signal. Although this conversion can be accomplished in a straightforward design through the use of classical op-amps, the stringent matching requirements of resistor ratios in feedback networks make the conversion particularly difficult from a practical standpoint. Because the gain of the preamplifier section in the CA3094 can be defined as the product of the transconductance and the load resistance ($g_m R_L$), feedback is not needed to obtain predictable open-loop gain performance. Fig. 2 shows the CA3094 in this basic type of circuit.

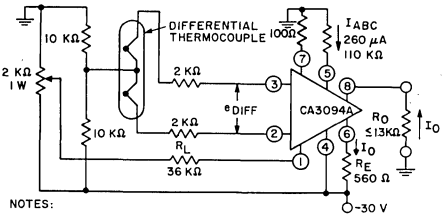



*Fig.2—Open-loop instrumentation amplifier with differential input and single-ended output.*

The gain of the preamplifier section (to terminal No. 1) is $g_m R_L = (5 \times 10^{-3})(36 \times 10^3) = 180$. The transconductance $g_m$ is a function of the current into terminal No. 5, $I_{ABC}$, the amplifier-bias-current. In this circuit an $I_{ABC}$ of 260 microamperes results in a $g_m$ of 5 millimhos. The operating point of the output stage is controlled by the 2-kilohm potentiometer. With no differential input signal ($e_{diff} = 0$), this potentiometer is adjusted to obtain a quiescent output current $I_O$ of 12 milliamperes. This output current is established by the 560-ohm emitter resistor, $R_E$, as follows:

$$I_O \approx \frac{(g_m R_L)(e_{diff})}{R_E}$$

Under the conditions described, an input swing $e_{diff}$ of ±26 millivolts produces a variation in the output current $I_O$ of ±8.35 milliamperes. The nominal quiescent output voltage is 12 milliamperes times 560 ohms or 6.7 volts. This output level drifts approximately −4 millivolts, or −0.0595 per cent, for each °C change in temperature. Output drift is caused by temperature-induced variations in the base-emitter voltage of the two output transistors, $Q_{12}$ and $Q_{13}$.

Fig. 3 shows the CA3094 used in conjunction with a resistive-bridge input network; and Fig. 4 shows a single-supply

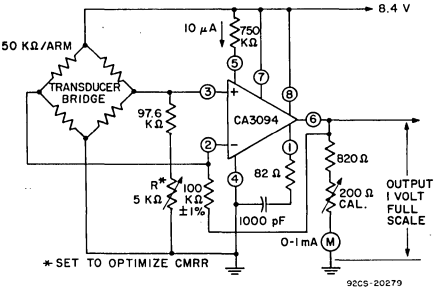



*Fig.3—Single-supply differential-bridge amplifier.*

amplifier for thermocouple signals. The RC networks* connected between terminals 1 and 4 in Figs. 3 and 4 provide compensation to assure stable operation.

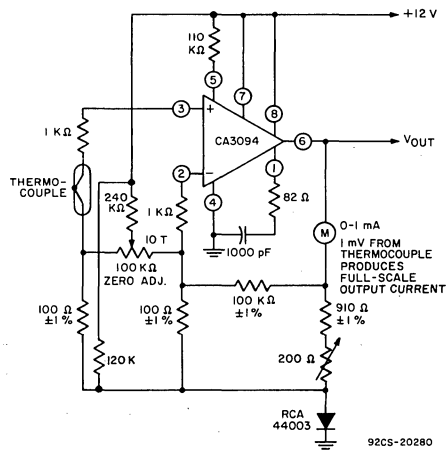



*Fig.4—Single-supply amplifier for thermocouple signals.*

### Class A Power Amplifiers

The CA3094 is attractive for power-amplifier service because the output transistor can control current up to 100 milliamperes (300 milliamperes peak), the premium devices

*The components of the RC network are chosen so that

$$\frac{1}{2\pi RC} \approx 2 \text{ MHz}.$$

(CA3094B) can operate at supply voltages up to 44 volts, and the TO-5 package can dissipate power up to 1.6 watts when equipped with a suitable heat sink that limits the case temperature to 55°C.

Fig. 5 shows a Class A amplifier circuit using the CA3094A that is capable of delivering 280 milliwatts to a 350-ohm resistive load. This circuit has a voltage gain of 60 dB and a

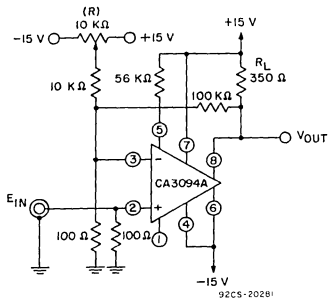



*Fig.5—Class-A amplifier — 280-mW capability into a resistive load.*

3-dB bandwidth of about 50 kHz. Operation is stable without the use of a phase-compensation network. Potentiometer R is used to establish the quiescent operating point for class A operation.

The circuit of Fig. 6 illustrates the use of the CA3094 in a class A power-amplifier circuit driving a transformer-coupled load. With dual power supplies of +7.5 volts and −7.5 volts, a

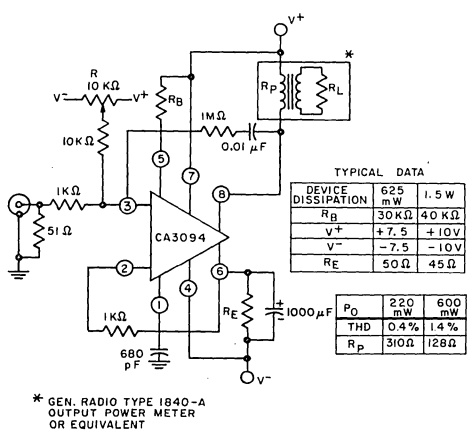



*Fig.6—Class-A amplifier with transformer-coupled load.*

base resistor $R_B$ of 30 kilohms, and an emitter resistor $R_E$ of 50 ohms, CA3094 dissipation is typically 625 milliwatts. With supplies of +10 volts and −10 volts, $R_B$ of 40 kilohms, and $R_E$ of 45 ohms, the dissipation is 1.5 watts. Total harmonic distortion is 0.4 per cent at a power-output level of 220 milliwatts with a reflected load resistance $R_P$ of 310 ohms, and is 1.4 per cent for an output of 600 milliwatts with an $R_P$ of 128 ohms. The setting of potentiometer R establishes the quiescent operating point for class A operation. The 1-kilohm resistor connected between terminals 6 and 2 provides dc feedback to stabilize the collector current of the output transistor. The ac gain is established by the ratio of the 1-megohm resistor connected between terminals 8 and 3 and the 1-kilohm resistor connected to terminal 3. Phase compensation is provided by the 680-picofarad capacitor connected to terminal 1.

### Class A Driver-Amplifier for Complementary Power Transistors

The CA3094 configuration and characteristics are ideal for driving complementary power-output transistors;[3] a typical circuit is shown in Fig. 7. This circuit can provide 12 watts of audio power output into an 8-ohm load with intermodulation distortion (IMD) of 0.2 per cent when 60-Hz and 2-kHz signals are mixed in a 4:1 ratio. Intermodulation distortion is shown as a function of power output in Fig. 8.

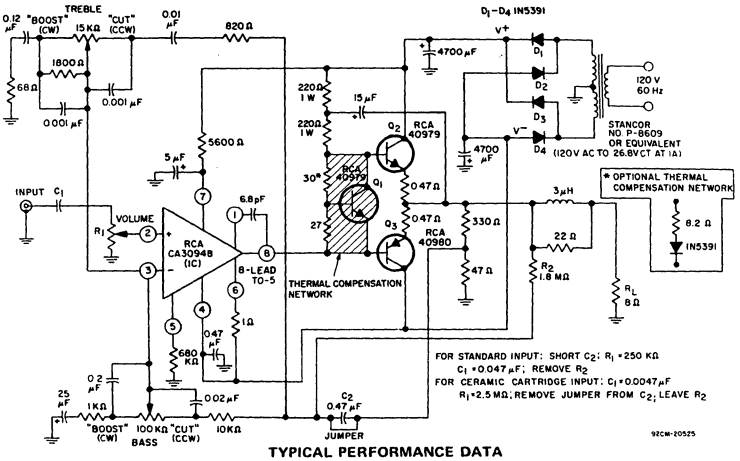
The large amount of loop gain and the flexibility of feedback arrangements with the CA3094 make it possible to incorporate the tone controls into a feedback network that is closed around the entire amplifier system. The tone controls in the circuit of Fig. 7 are part of the feedback network connected from the amplifier output (junction of the 330- and 47-ohm resistors driven by the emitters of $Q_2$ and $Q_3$) to terminal 3 of the CA3094. Fig. 9 shows voltage gain as a function of frequency with tone controls adjusted for "flat" response and for responses at the extremes of tone-control rotation. The use of tone controls incorporated in the feedback network results in excellent signal-to-noise ratio. Hum and noise are typically 700 microvolts (83 dB down) at the output.

In addition to the savings resulting from reduced parts count and circuit size, the use of the CA3094 leads to further savings in the power-supply system. Typical values of power-supply rejection and common-mode rejection are 90 dB and 100 dB, respectively. An amplifier with 40-dB gain and 90-dB power-supply rejection would require a 31-millivolt power-supply ripple to produce one millivolt of hum at the output. Therefore, no filtering is required other than that provided by the energy-storage capacitors at the output of the rectifier system shown in Fig. 7.

For applications in which the operating temperature range is limited (e.g., consumer service) the thermal compensation network (shaded area) can be replaced by a more economical configuration consisting of a resistor-diode combination (8.2 ohms and 1N5391) as shown in Fig. 7.

### Power Multivibrators (Astable and Monostable)

The CA3094 is suitable for use in power multivibrators because its high-current output transistor can drive low-impedance circuits while the input circuitry and the frequency-determining elements are operating at micropower levels. A typical example of an astable multivibrator using the CA3094 with a




## TYPICAL PERFORMANCE DATA

**For 12-W Audio Amplifier Circuit**

| | | |
|---|---|---|
| Power Output (8Ω load, Tone Control set at "Flat") | | |
| Music (at 5% THD, regulated supply) | 15 | W |
| Continuous (at 0.2% IMD, 60 Hz & 2 kHz mixed in a 4:1 ratio, unregulated supply) See Fig. 8 | 12 | W |
| Total Harmonic Distoration | | |
| At 1 W, unregulated supply | 0.05 | % |
| At 12 W, unregulated supply | 0.57 | % |
| Voltage Gain | 40 | dB |
| Hum and Noise (Below continuous Power Output) | 83 | dB |
| Input Resistance | 250 | kΩ |
| Tone Control Range | See Fig. 9 | |

*Fig.7—12-watt amplifier circuit featuring true complementary-symmetry output stage with CA3094 in driver stage.*

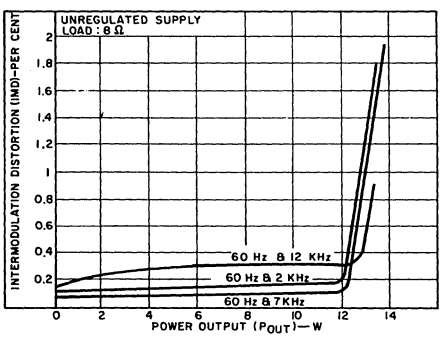



*Fig.8—Intermodulation distortion vs. power output.*

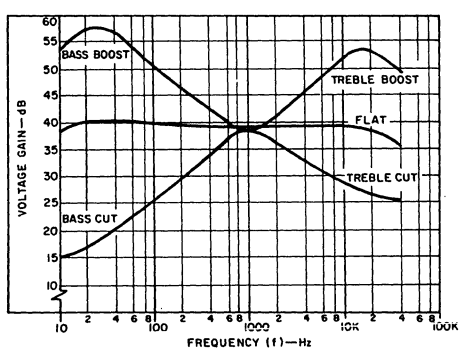



*Fig.9—Voltage gain vs. frequency.*

dual power supply is shown in Fig. 10. The output frequency $f_{OUT}$ is determined as follows:

$$f_{OUT} = \frac{1}{2RC\ln[(2R1/R2) + 1]}$$

If R2 is equal to 3.08 R1, then $f_{OUT}$ is simply the reciprocal of RC.

Fig. 11 is a single-supply astable multivibrator circuit which illustrates the use of the CA3094 for flashing an incandescent lamp. With the component values shown, this circuit produces one flash per second with a 25-per-cent "on"-time while delivering output current in excess of 100 milliamperes. During

the 75-per-cent "off"-time it idles with micropower consumption. The flashing rate can be maintained within ±2 per cent of the nominal value over a battery voltage range from 6 to 15 volts and a temperature excursion from 0 to 70°C. The CA3094 series of circuits can supply peak-power output in excess of 10 watts when used in this type of circuit. The frequency of oscillation $f_{OSC}$ is determined by the resistor ratios, as follows:

$$f_{OSC} = \frac{1}{2RC\ln[(2R_1/R_2)+1]}$$

where

$$R1 = \frac{R_A R_B}{R_A + R_B}$$

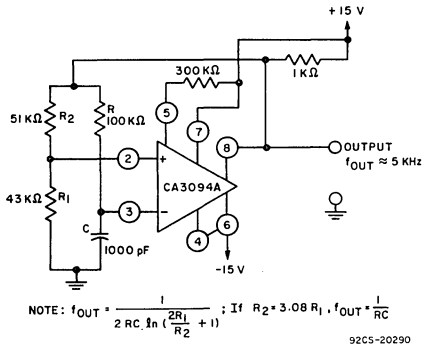



*Fig. 10—Astable multivibrator using dual supply.*

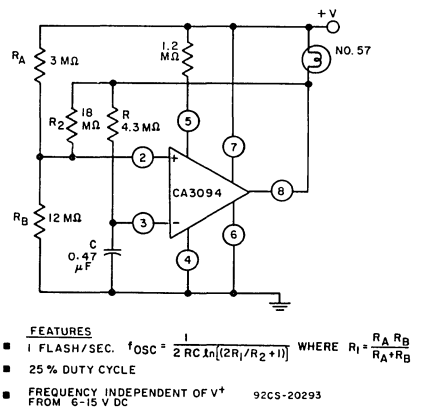



*Fig. 11—Astable multivibrator using single supply.*

Provisions can easily be made in the circuit of Fig. 11 to vary the multivibrator pulse length while maintaining an essentially constant pulse repetition rate. The circuit shown in Fig. 12 incorporates a potentiometer Rp for varying the width of pulses generated by the astable multivibrator to drive a light-emitting diode (LED).

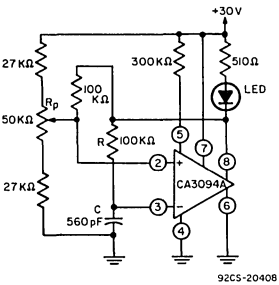



*Fig. 12—Astable power multivibrator with provisions for varying duty cycle.*

Fig. 13 shows a circuit incorporating independent controls ($R_{ON}$ and $R_{OFF}$) to establish the "on" and "off" periods of the current supplied to the LED. The network between points "A" and "B" is analogous in function to that of the 100-kilohm resistor R in Fig. 12.

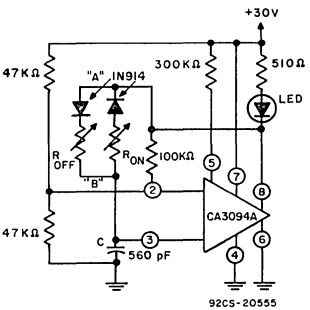



*Fig. 13—Astable power multivibrator with provisions for independent control of LED "on-off" periods.*

The CA3094 is also suitable for use in monostable multivibrators, as shown in Fig. 14. In essence, this circuit is a pulse counter in which the duration of the output pulses is independent of trigger-pulse duration. The meter reading is a function of the pulse repetition rate which can be monitored with the speaker.

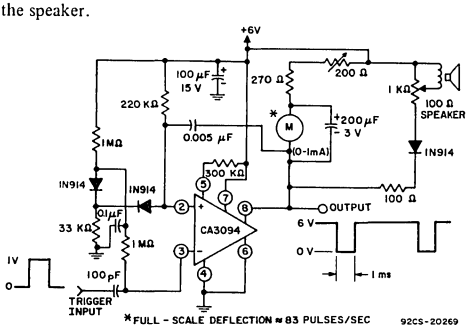



*Fig. 14—Power monostable multivibrator.*

### Current- or Voltage-Controlled Oscillators

Because the transconductance of the CA3094 varies linearly as a function of the amplifier bias current ($I_{ABC}$) supplied to terminal 5, the design of a current- or voltage-controlled oscillator is straightforward, as shown in Fig. 15. Fig. 16 and 17 show oscillator frequency as a function of $I_{ABC}$ for a current-controlled oscillator for two different values of capacitor C in Fig. 15. The addition of an appropri-

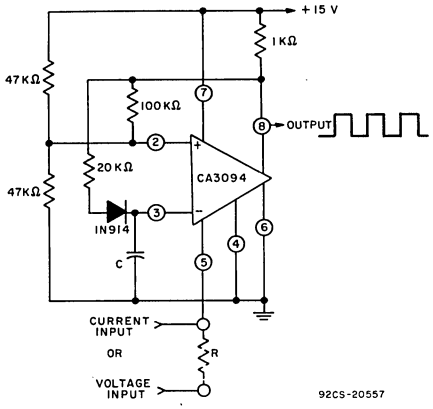



*Fig.15—Current- or voltage-controlled oscillator.*

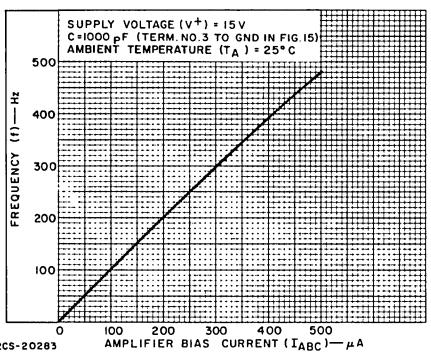



*Fig.16—Frequency as a function of $I_{ABC}$ for C=1000 pF for circuit in Fig. 15.*

ate resistor (R) in series with terminal 5 in Fig. 15 converts the circuit into a voltage-controlled oscillator. Linearity with respect to either current or voltage control is within 1 per cent over the middle half of the characteristics. However, variation in the symmetry of the output pulses as a function of frequency is an inherent characteristic of the circuit in Fig. 15, and leads to distortion when this circuit is used to drive the phase detector in phase-locked-loop applications. This type of distortion can be eliminated by interposing an appropriate flip-flop between the output of the oscillator and the phase-locked discriminator circuits.

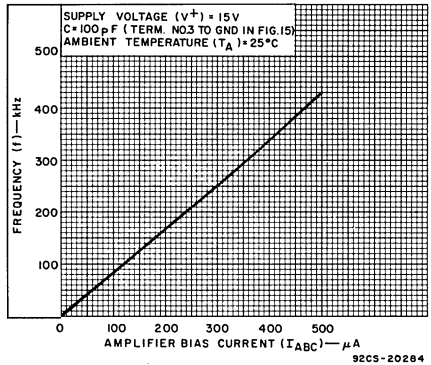



*Fig.17—Frequency as a function of $I_{ABC}$ for C=100 pF for circuit in Fig. 15.*

### Comparators (Threshold Detectors)

Comparator circuits are easily implemented with the CA3094, as shown by the circuits in Fig. 18. The circuit of Fig. 18(a) is arranged for dual-supply operation; the input voltage exceeds the positive threshold, the output voltage swings essentially to the negative supply-voltage rail (it is assumed that there is negligible resistive loading on the output ter-

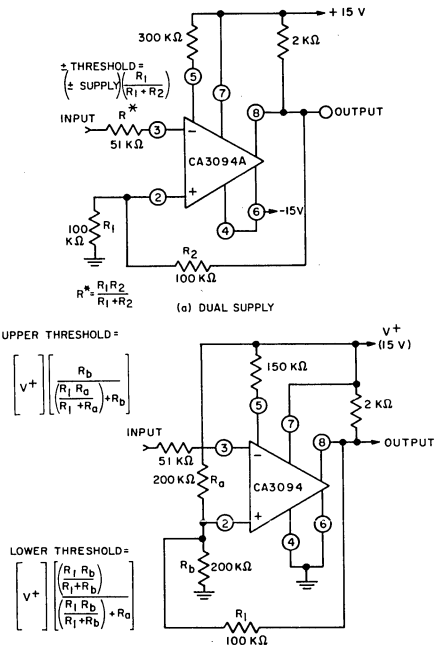



*Fig.18—Comparators (threshold detectors) — dual- and single-supply types.*

minal). An input voltage that exceeds the negative threshold value results in a positive voltage output essentially equal to the positive supply voltage. The circuit in Fig. 18(b), connected for single-supply operation, functions similarly.

Fig. 19 shows a dual-limit threshold detector circuit in which the high-level limit is established by potentiometer R1

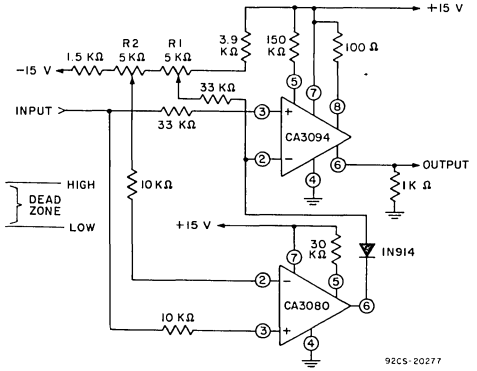



*Fig.19—Dual-limit threshold detector.*

and the low-level limit is set by potentiometer R2 to actuate the CA3080 low-limit detector.[1,2] A positive output signal is delivered by the CA3094 whenever the input signal exceeds either the high-limit or the low-limit values established by the appropriate potentiometer settings. This output voltage is approximately 12 volts with the circuit shown.

The high current-handling capability of the CA3094 makes it useful in Schmitt power-trigger circuits such as that shown in Fig. 20. In this circuit, a relay coil is switched whenever the

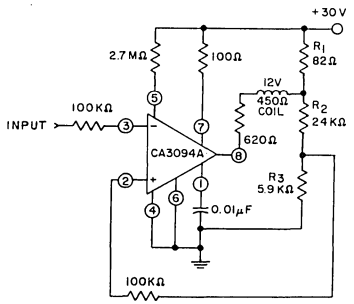



*Fig.20—Precision Schmitt power-trigger circuit.*

input signal traverses a prescribed upper or lower trip point, as defined by the following expressions:

$$\text{Upper Trip Point} = 30\left(\frac{R3}{R1 + R2 + R3}\right)$$

$$\text{Lower Trip Point} \cong (30 - 0.026R1)\frac{R3}{R2 + R3}$$

The circuit is applicable, for example, to automatic ranging. With the values shown in Fig. 20, the relay coil is energized when the input exceeds approximately 5.9 volts and remains energized until the input signal drops below approximately 5.5 volts.

### Power-Supply Regulators

The CA3094 is an ideal companion device to the CA3085 series regulator circuits[4] in dual-voltage tracking regulators that handle currents up to 100 milliamperes. In the circuit of Fig. 21, the magnitude of the regulated positive voltage provided by the CA3085A is adjusted by potentiometer R. A sample of this positive regulated voltage supplies the power for the CA3094A negative regulator and also supplies a refer-

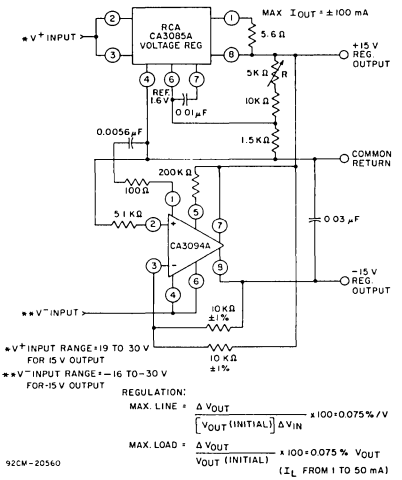



*Fig.21—Dual-voltage tracking regulator.*

ence voltage to its terminal 3 to provide tracking. This circuit provides a maximum line regulation equal to 0.075 per cent per volt of input voltage change and a maximum load regulation of 0.075 per cent of the output voltage.

Fig. 22 shows a regulated high-voltage supply similar to the type used to supply power for Geiger-Mueller tubes. The CA3094, used as an oscillator, drives a step-up transformer which develops suitable high voltages for rectification in the RCA-44007 diode network. A sample of the regulated output voltage is fed to the CA3080A operational transconductance amplifier through the 198-megohm and 910-kilohm divider to control the pulse repetition rate of the CA3094. Adjustment of potentiometer R determines the magnitude of the regulated output voltage. Regulation of the desired output voltage is maintained within one per cent despite load-current variations of 5 to 26 microamperes. The dc-to-dc conversion efficiency is about 48 per cent.

### Timers

The programmability feature inherent in the CA3094 (and operational transconductance amplifiers in general) simplifies the design of presettable timers such as the one shown in

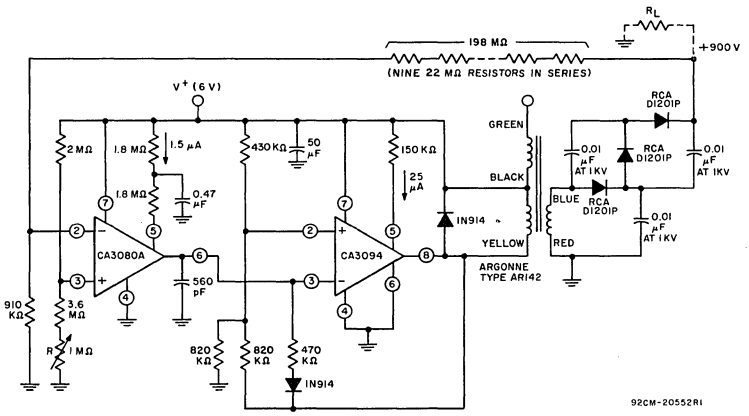



*Fig.22—Regulated high-voltage supply.*

Fig. 23. Long timing intervals (e.g., up to 4 hours) are achieved by discharging a timing capacitor $C_1$ into the signal-input terminal (e.g., No. 3) of the CA3094. This discharge current is controlled precisely by the magnitude of the amplifier bias current $I_{ABC}$ programmed into terminal 5 through a resistor selected by switch S2. Operation of the circuit is initiated by charging capacitor $C_1$ through the momentary closing of switch $S_1$. Capacitor $C_1$ starts discharging and continues discharging until voltage $E_1$ is less than voltage $E_2$. The differential input transistors in the CA3094 then change state, and terminal 2 draws sufficient current to reverse the polarity of the output voltage (terminal 6). Thus, the CA3094 not only has provision for readily presetting the time delay, but also provides significant output current to drive control devices such as thyristors. Resistor $R_5$ limits the initial charging current for $C_1$. Resistor $R_7$ establishes a minimum voltage of at least 1 volt at terminal 2 to insure operation within the common-mode-input range of the device. The diode limits the maximum differential input voltage to 5 volts. Gross changes in time-range selection are made with switch S2, and vernier trimming adjustments are made with potentiometer $R_6$.

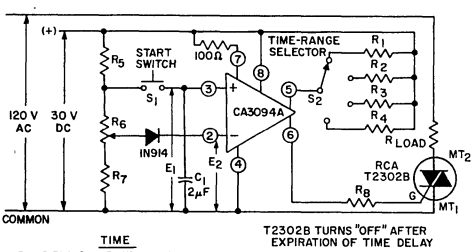



*Fig.23—Presettable analog timer.*

In some timer applications, such as that shown in Fig. 24, a meter readout of the elapsed time is desirable. This circuit uses the CA3094 and the CA3083 transistor array[5] to control the meter and a load-switching triac. The timing cycle starts with the momentary closing of the start switch to charge capacitor $C_1$ to an initial voltage determined by the 50-kilohm vernier timing adjustment. During the timing cycle, capacitor $C_1$ is discharged by the input bias current at terminal 3, which is a function of the resistor value $R_1$ chosen by the time-range selection switch. During the timing cycle the output of the CA3094, which is also the collector voltage of $Q_1$, is "high". The base drive for $Q_1$ is supplied from the positive supply through a 91-kilohm resistor. The emitter of $Q_1$, through the 75-ohm resistor, supplies gate-trigger current to the triac. Diode-connected transistors $Q_4$ and $Q_5$ are connected so that transistor $Q_1$ acts as a constant-current source to drive the triac. As capacitor $C_1$ discharges, the CA3094 output voltage at terminal 6 decreases until it becomes less than the $V_{CEsat}$ of $Q_1$. At this point the flow of drive current to the triac ceases and the timing cycle is ended. The 20-kilohm resistor between terminals 2 and 6 of the CA3094 is a feedback resistor. Diode-connected transistors $Q_2$ and $Q_3$ and their associated networks serve to compensate for nonlinearities in the discharge-circuit network by bleeding corrective current into the 20-kilohm feedback resistor. Thus, current flow in the meter is essentially linear with respect to the timing period. The time periods as a function of $R_1$ are indicated on the Time-Range Selection Switch in Fig. 24.

### Alarm Circuit

Fig. 25 shows an alarm circuit utilizing two "sensor" lines. In the "no-alarm" state, the potential at terminal 2 is lower than the potential at terminal 3, and terminal 5 ($I_{ABC}$) is driven with sufficient current through resistor $R_5$ to keep the output voltage "high". If either "sensor" line is opened, shorted to ground, or shorted to the other sensor line, the output goes "low" and activates some type of alarm system.

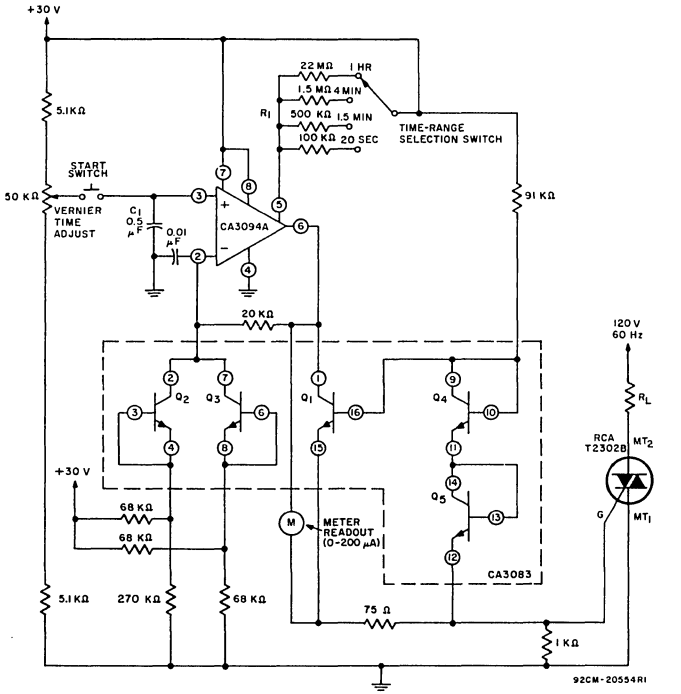



*Fig.24—Presettable timer with linear readout.*

The back-to-back diodes connected between terminals 2 and 3 protect the CA3094 input terminals against excessive differential voltages.

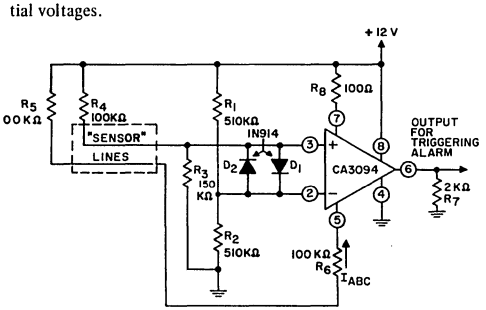



*Fig.25—Alarm system.*

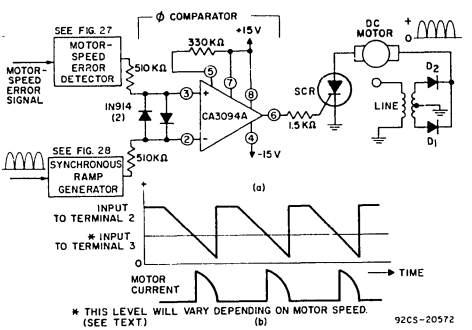



*Fig.26—Motor-speed controller system.*

### Motor-Speed Controller System

Fig. 26 illustrates the use of the CA3094 in a motor-speed controller system. Circuitry associated with rectifiers $D_1$ and $D_2$ comprises a full-wave rectifier which develops a train of half-sinusoid voltage pulses to power the dc motor. The motor speed depends on the peak value of the half-sinusoids and the period of time (during each half-cycle) the SCR is conductive. The SCR conduction, in turn, is controlled by the time duration of the positive signal supplied to the SCR by the phase comparator. The magnitude of the positive dc voltage supplied to terminal 3 of the phase comparator depends on motor-speed error as detected by a circuit such as that shown in Fig. 27. This dc voltage is compared to that of a fixed-amplitude ramp wave generated synchronously with the ac-line-voltage frequency. The comparator output at terminal 6 is "high" (to trigger the SCR into conduction) during the period

when the ramp potential is less than that of the error voltage on terminal 3. The motor-current conduction period is increased as the error voltage at terminal 3 is increased in the positive direction. Motor-speed accuracy of ±1 per cent is easily obtained with this system.

**Motor-Speed Error Detector.** Fig. 27(a) shows a motor-speed error detector suitable for use with the circuit of Fig. 26. A CA3080 operational transconductance amplifier is used as a voltage comparator. The reference for the comparator is established by setting the potentiometer R so that the voltage at terminal 3 is more positive than that at terminal 2 when the motor speed is too low. An error voltage $E_1$ is derived from a tachometer driven by the motor. When the motor speed is too low, the voltage at terminal 2 of the voltage comparator is less positive than that at terminal 3, and the output voltage at terminal 6 goes "high". When the motor speed is too high, the opposite input conditions exist, and the output voltage at terminal 6 goes "low". Fig. 27(b) also shows these conditions graphically, with a linear transition region between the "high" and "low" output levels. This linear transition region is known as "proportional bandwidth". The slope of this region is determined by the proportional bandwidth control to establish the error-correction response time.

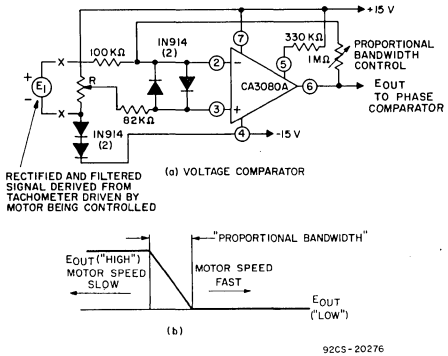



*Fig. 27—Motor speed error detector.*

**Synchronous Ramp Generator.** Fig. 28 shows a schematic diagram and signal waveforms for a synchronous ramp generator suitable for use with the motor-controller circuit of Fig. 26. Terminal 3 is biased at approximately +2.7 volts (above the negative supply voltage). The input signal $E_{IN}$ at terminal 2 is a sample of the half-sinusoids (at line frequency) used to power the motor in Fig. 26. A synchronous ramp signal is produced by using the CA3094 to charge and discharge capacitor $C_1$ in response to the synchronous toggling of $E_{IN}$. The charging current for $C_1$ is supplied by terminal 6. When terminal 2 swings more positive than terminal 3, transistors $Q_{12}$ and $Q_{13}$ in the CA3094 (Fig. 1) lose their base drive and become non-conductive. Under these conditions, $C_1$ discharges linearly through the external diode $D_3$ and the $Q_{10}$, $D_6$ path in the CA3094 to produce the ramp wave. The $E_{out}$ signal is supplied to the phase comparator in Fig. 26.

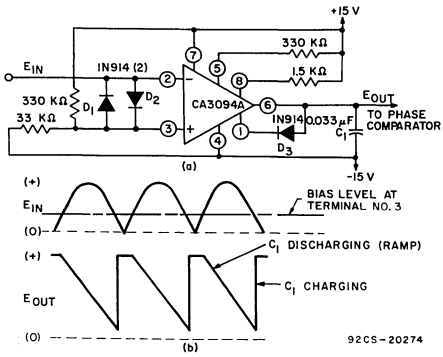



*Fig.28—Synchronous ramp generator with input and output waveforms.*

## Thyristor Firing Circuits

**Temperature Controller.** In the temperature control system shown in Fig. 29, the differential input of the CA3094 is connected across a bridge circuit comprised of a PTC (positive-temperature-coefficient) temperature sensor, two 75-kilohm resistors, and an arm containing the temperature set control. When the temperature is "low", the resistance of the PTC-type sensor is also low; therefore, terminal 3 is more positive than terminal 2 and an output current from terminal 6 of the CA3094 drives the triac into conduction. When the temperature is "high", the input conditions are reversed and the triac is cut off. Feedback from terminal 8 provides hysteresis to the control point to prevent rapid cycling of the system. The 1.5-kilohm resistor between terminal 8 and the positive supply limits the triac gate current and develops the voltage for the hysteresis feedback. The excellent power-supply-rejection and common-mode-rejection ratios of the CA3094 permit accurate repeatability of control despite appreciable power-supply ripple. The circuit of Fig. 29 is equally suitable for use with NTC (negative-temperature-coefficient) sensors provided the positions of the sensor and the associated resistor R are interchanged in the circuit. The diodes connected back-to-back across the input terminals of the CA3094 protect the device against excessive differential input signals.

**Thyristor Control from AC-Bridge Sensor.** Fig. 30 shows a line-operated thyristor-firing circuit controlled by a CA3094 that operates from an ac-bridge sensor. This circuit is particularly suited to certain classes of sensors that cannot be operated from dc. The CA3094 is inoperative when the high side of the ac line is negative because there is no $I_{ABC}$ supply to terminal 5. When the sensor bridge is unbalanced so that terminal 2 is more positive than terminal 3, the output stage of the CA3094 is cut off when the ac line swings positive, and the output level at terminal 8 of the CA3094 goes "high". Current from the line flows through the 1N3193 diode to charge the 100-microfarad reservoir capacitor, and also provides current to drive the triac into conduction. During the succeeding negative swing of the ac line, there is sufficient remanent energy in the reservoir capacitor to maintain conduction in the triac.

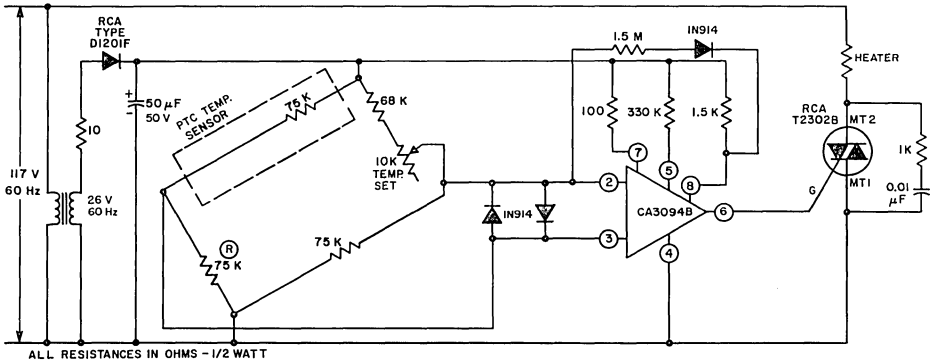



*Fig.29—Temperature controller.*

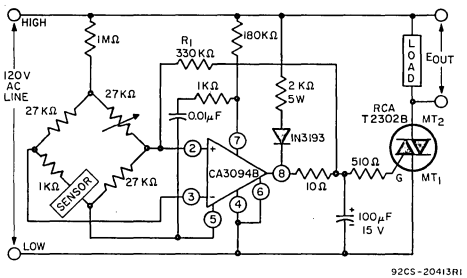



*Fig.30—Line-operated thyristor-firing circuit controlled by ac-bridge sensor.*

When the bridge is unbalanced in the opposite direction so that terminal 3 is more positive than terminal 2, the output of the CA3094 at terminal 8 is driven sufficiently "low" to "sink" the current supplied through the 1N3193 diode so that the triac gate cannot be triggered. Resistor $R_1$ supplies the hysteresis feedback to prevent rapid cycling between turn-on and turn-off.

### Battery-Charger Regulator Circuit

The circuit for a battery-charger regulator circuit using the CA3094 is shown in Fig. 31. This circuit accurately limits the peak output voltage to 14 volts, as established by the zener diode connected across terminals 3 and 4. When the output voltage rises slightly above 14 volts, signal feedback through a 100-kilohm resistor to terminal 2 reduces the current drive supplied to the 2N3054 pass transistor from terminal 6 of the CA3094. An incandescent lamp serves as the indicator of charging-current flow. Adequate limiting provisions protect the circuit against damage under load-short conditions. The advantage of this circuit over certain other types of regulator circuits is that the reference voltage supply doesn't drain the battery when the power supply is disconnected. This feature is important in portable service applications, such as in a trailer where a battery is kept "on-charge" when the trailer is parked and power is provided from an ac line.

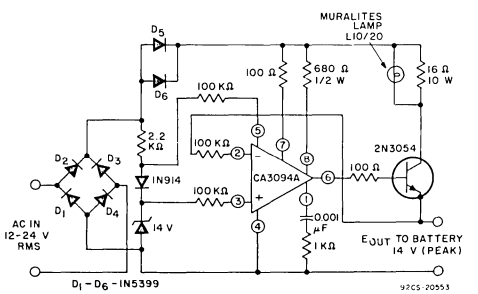
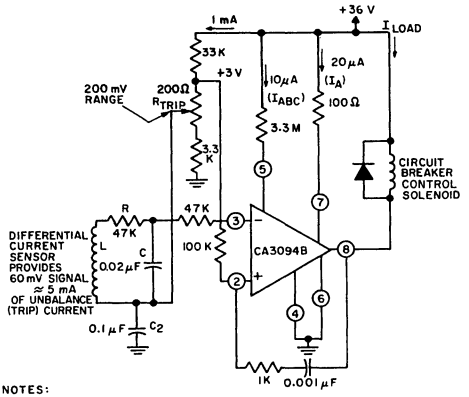



*Fig.31—Battery-charger regulator circuit.*

### Ground-Fault Interrupters (GFI)

Ground-fault-interrupter systems are used to continuously monitor the balance of current between the high and neutral lines of power-distribution networks. Power is interrupted whenever the unbalance exceeds a preset value (e.g., 5 milliamperes). An unbalance of current can occur when, for example, defective insulation in the high side of the line permits leakage of current to an earth ground. GFI systems can be used to reduce the danger of electrocution from accidental contact with a "high" line because the unbalance caused by the leakage of current from the "high" line through a human body to ground results in an interruption of current flow.

The CA3094 is ideally suited for GFI applications because it can be operated from a single supply, has adequate sensitivity, and can drive a relay or thyristor directly to effect power interruption. Fig. 32 shows a typical GFI circuit. Vernier adjustment of the trip point is made by the $R_{TRIP}$ potentiometer. When the differential current sensor supplies a signal that exceeds the selected trip-point voltage level (e.g., 60 millivolts), the CA3094 is toggled "on" and terminal 8 goes "low" to energize the circuit-breaker trip coil. Under quiescent conditions, the entire circuit consumes approximately 1 milliampere. The resistor R, connected to one leg of the current sensor, provides current limiting to protect the CA3094 against voltage spikes as large as 100 volts. Fig. 32 also shows the pertinent waveform for the GFI circuit.




NOTES:

1. ALL RESISTORS IN OHMS, 1/2 WATT, ±10%
2. RC SELECTED FOR 3db POINT AT 200 Hz
3. $C_2$=AC BY-PASS
4. OFFSET ADJ. INCLUDED IN $R_{TRIP}$
5. INPUT IMPEDANCE FROM 2 TO 3 EQUALS 800 K.
6. WITH NO INPUT SIGNAL TERMINAL 8 (OUTPUT) AT +36 VOLTS

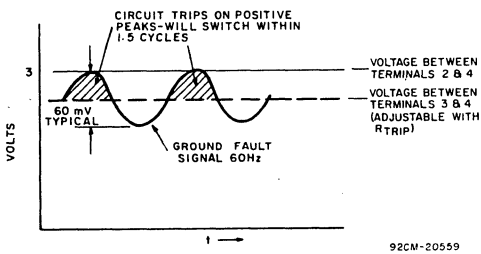



*Fig.32—Ground fault interrupter (GFI) and waveform pertinent to ground fault detector.*

Because hazards of severe electrical shock are a potential danger to the individual user in the event of malfunctions in GFI apparatus, it is mandatory that the highest standards of good engineering practice be employed in designing equipment for this service. Every consideration in design and application must be given to the potentially serious consequences of component malfunction in such equipment. Use of "reliability-through-redundancy" concepts and so-called "fail-safe" features is encouraged.

**Acknowledgments**

The authors thank A. Sheng and R. Baird for their assistance in designing some of the circuits described in this Note.

**References**

1. RCA Published Data for CA3080 and CA3080A, File No. 475.
2. Applications of the CA3080 and CA3080A High Performance Operational Transconductance Amplifiers, RCA Application Note ICAN-6668.
3. L. Kaplan and H. A. Wittlinger, "An IC Operational-Transconductance-Amplifier (OTA) with Power Capability". Paper originally presented at the IEEE Chicago Spring Conference on Broadcast and TV Receivers, June 1972. Reprinted by the RCA Solid State Division as Publication No. ST-6077.
4. RCA Published Data for CA3085, File No. 491.
5. RCA Published Data for CA3083, File No. 481.

# Digital-to-Analog Conversion Using the RCA-CD4007A COS/MOS IC

By O. H. Schade, Jr.

RCA COS/MOS integrated circuits have demonstrated outstanding performance in a wide variety of DIGITAL applications. Simplified circuitry, design flexibility, low power consumption, moderate speed, and high noise immunity of these devices can complement the high transconductance of bipolar IC's in an extension to LINEAR signal processing applications. This Note demonstrates the use of The RCA-CD4007A♦ COS/MOS Dual Complementary Pair Plus Inverter as the Digital-to-Analog (D/A) switch; the op-amp output stage for a Digital-to-Analog Converter (DAC) uses COS/MOS and bipolar transistor-array IC's.

### General Considerations

In combination with a p-channel input pair (two p-channels of the CD4007A), a buffer-follower COS/MOS-bipolar op-amp has been designed with the capability to attain essentially the negative supply voltage at both the input and output terminals. Therefore, to consider inexpensive single-supply operation becomes possible without the sacrifice of speed and bandwidth that results with many monolithic bipolar IC op-amps. An additional advantage is the use of an MOS input stage to provide exceptionally high input resistance and low input current.

A 9-bit DAC is described in this Note to illustrate this design approach. This system combines the concepts of multiple-switch COS/MOS IC's, a low-cost ladder network of discrete metal-oxide film resistors, a COS/MOS-bipolar op-amp follower, and an inexpensive monolithic regulator in a simple single-supply system. An additional feature which complements the ever-increasing use of COS/MOS IC's for digital signal processing is the readily interfaced COS/MOS-DAC input logic.

Although the accuracy of a DAC system depends on many factors, it is the ladder network which must initiate properly-proportioned current or voltage outputs. Recognition of various ladder types and an appreciation of the design flexibility and constraints are paramount to a well executed DAC development.

### Resistance Networks for DAC's

Ladder networks for DAC's can take many forms, although three types are most generally encountered. Among the best-known variations is the current ladder shown in Fig. 1. This network is frequently used in combination with bipolar current switches which utilize a reference potential at the transistor base terminals to establish emitter currents having binary proportions. Because current summing is accomplished at the collectors of these transistors, the extent of $V_{BE}$- and beta-matching of these transistors depends on the degree of accuracy and temperature-range requirements. The use of a 10/20/40/80 $-k\Omega$ network in conjunction with a "quad" switch, a follower amplifier, and dual power supplies is common.

♦For data, see bulletin File No. 479.

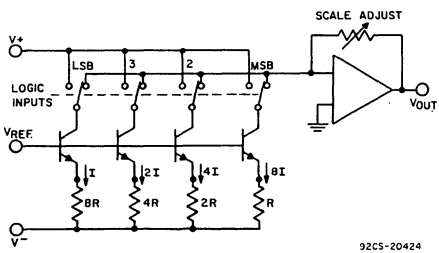



*Fig. 1— Current ladder-network for bipolar DAC.*

Fig. 2 shows an R/2R current ladder commonly employed in monolithic DAC's. Similar resistance values can simplify the problem of meeting ratio-match accuracy requirements. This ladder must be terminated in a single potential (or at least invariable values) to maintain proper current proportions. Although the *absolute* resistance values of the circuit in Fig. 1 must temperature track the summing resistor (or additional compensation must be employed), the R/2R current ladder must maintain only a resistance *ratio;* it is the current sink which must remain stable under external influences.

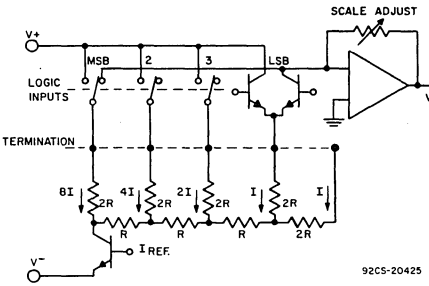



*Fig. 2– R/2R current ladder-network for monolithic DAC.*

Fig. 3 shows a less common *voltage* ladder suitable for DAC's using COS/MOS switches. Output potentials are obtained directly by terminating the ladder arms at either the positive or the negative power supply. Each COS/MOS inverter output pair functions as a double-throw switch. If the switch (channel) resistance is kept small compared to the ladder-arm resistance value, accuracy becomes a function of ladder supply voltage and resistance ratios alone. Operation of this ladder is *dynamic;* the current in an arm reverses as the logic state changes. Therefore, stray capacitances (or the inductance of a wirewound resistor) can limit speed as a result of typical settling times of several microseconds. However, the proper selection of parallel connection of switches for the most significant bit (MSB) to minimize channel resistance can result in COS/MOS-DAC speeds which approach those of the best bipolar systems, particularly when consideration is given to follower-amplifier speed limitations.

In the illustrative 9-bit application, a modified voltage-ladder design is employed. The use of 1%-tolerance metal-oxide film resistors can result in inexpensive networks suitable to about the 10-bit level. Such networks are readily constructed for system evaluations and may also prove to be suitable for production. Practical tolerance considerations call for variations from the "pure" R/2R configuration, as discussed later.

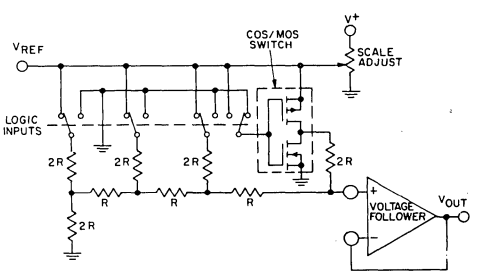



*Fig. 3– R/2R voltage ladder-network for COS/MOS DAC.*

### The COS/MOS Switch

A typical COS/MOS switch (CD4007A) is shown in Fig. 4. A change in input logic level causes the output to swing to either the positive or the negative supply voltage. Power consumption is low, typically a few microwatts to a few milliwatts, depending on the ladder resistance and voltage choice. Large DAC ladder resistance values can be used to minimize the effects of switch resistance. Fig. 5 shows the minimum ladder resistance value for a given saturation resistance to produce an accuracy of 1/2 LSB (Least Significant Bit), with bit number as a parameter. For example, the CD4007A which has a channel resistance of approximately 250-ohms ($V_{DD}$ = 10 V), requires a minimum ladder resistance of 100 kΩ to maintain a 9-bit accuracy level. Reference to the dashed "settling time" line and the rightside ordinate shows that the approximate settling time of such a network having a 10-pF node capacitance is 6 μs. This settling time has been based on six time constants for settling to 1/2 LSB, an *average* value for the bit range illustrated. If a faster settling time is required, circuits employing the RCA-CD4041A can be used.

The CD4041A[o] can drive (in a theoretical example) a 4–kΩ, 6-bit ladder network which has a settling time of approximately 250 ns. This is as fast as the *best* presently available monolithic bipolar switches. High-slew-rate voltage-follower amplifiers are needed to maintain these speed levels; when a COS/MOS bipolar op-amp is used, the slew rate is approximately 30 V/μs and the settling time is several hundred nanoseconds for a 10-V full-scale signal. This performance approaches the state-of-the-art for monolithic op-amps, especially in low-cost systems. In fact, high-speed op-amps capable of swinging to the negative supply have not generally been available.

### A Voltage-Follower Amplifier for Single-Supply Operation

It is practical to utilize commercially available COS/MOS and bipolar transistor-array IC's to provide a composite op-amp suitable for single-supply DAC systems. Fig. 6 shows a unity-gain follower amplifier having a COS/MOS p-channel input, an n-p-n second gain stage, and a COS/MOS inverter output. The IC building blocks are two CA3600E's[Δ] (COS/MOS Transistor Pairs) and a CA3046[□] n-p-n transistor array. A zener-regulated leg provides bias for a 400-μA p-channel current source feeding the input stage, which is terminated in an n-p-n current mirror. Amplifier voltage-offset is nulled with the 10-kΩ balance potentiometer. The second-stage current level is established by the 20-kΩ load, and is selected to approximate the first-stage current level, to assure similar positive and negative slew rates. The COS/MOS inverter portion forms the final output stage and is terminated in a 2-kΩ load, a typical value used with monolithic op-amps. Voltage gain is affected by the choice of load resistance value. The output stage of this amplifier is easily driven to within 1 mV of the negative supply voltage.

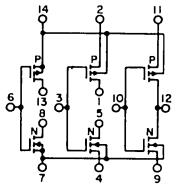



*Fig. 4– CD4007A schematic diagram.*

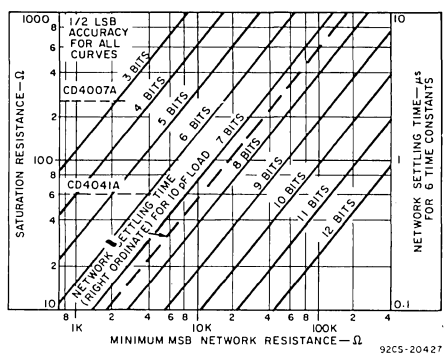



*Fig. 5– COS/MOS-DAC voltage-network requirements.*

[o] COS/MOS Quad True/Complement Buffer

[Δ] For data, see bulletin File No. 619.

[□] For data, see bulletin File No. 341.

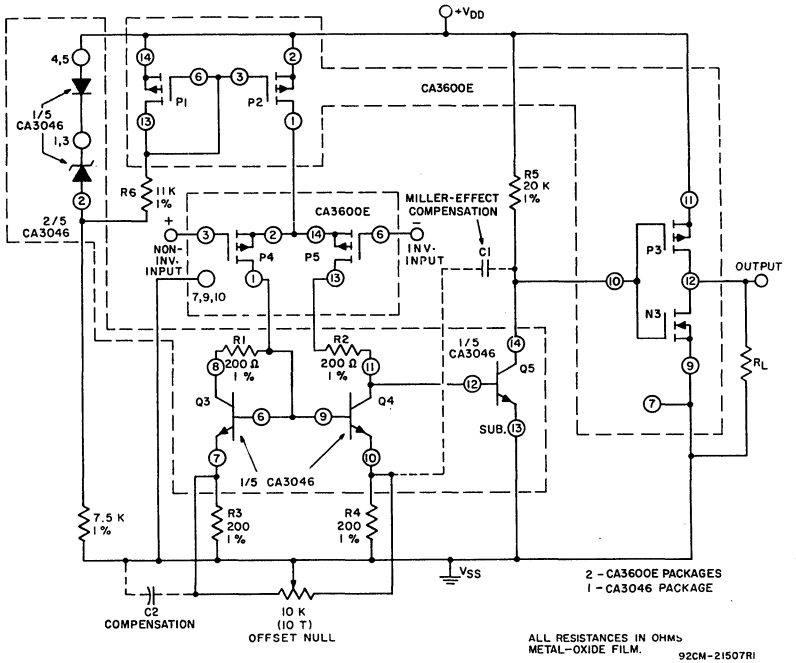



*Fig. 6— Voltage-follower amplifier for single-supply operation.*

Compensation for the unity-gain non-inverting mode is provided by Miller feedback of 39 pF and a 300-pF by-pass capacitor shunting one-half the driving current (1-2 MHz). Unity-gain bandwidth is just under 10 MHz and the open-loop gain is 75 dB. Fig. 7 shows the gain-bandwidth characteristics for this circuit. A potential latch situation at the bipolar mirror is avoided by use of resistor-capacitor network (R = 1 k Ω, C = 150 pF), which limits the dc feedback through the p-channel gate-protective diode.

The amplifier response to 4-V input pulses is shown in Fig. 8. Although the slew rate is approximately 30 V/μs, the settling time is significantly prolonged (approximately 2 μs) as a result of the method of second-stage biasing when the output swings near the negative supply. For many applications, this speed loss is not significant. If a faster amplifier is desired, the load resistor can be replaced with a p-channel CA3600E current source similar to that used for the first stage. In fact, it may be desirable to change the current and resistance values to optimize the gain/speed trade-off for a particular application. For example, if higher gain is desired for less follower offset, the 20-kΩ resistance value can be increased. The choice of output load resistance also affects the gain/speed compromise.

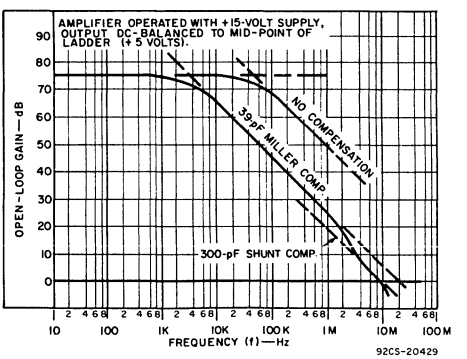



*Fig. 7— Voltage-follower open-loop gain characteristics.*

### A 9-Bit COS/MOS DAC

An example of a 9-bit DAC is shown in Fig. 9. Three CD4007A IC packages perform the switch function using a 10-V logic level. A single 15-V supply provides a positive bus for the follower amplifier and feeds the CA3085▲ voltage regulator. The "scale-adjust" function is provided by the regulator output control which is set to a nominal 10 V in this system. The line-voltage regulation (approximately 0.2%) permits 9-bit accuracy to be maintained with a variation of several volts in the supply. System power consumption ranges between 70 and 200 mW; a major portion is dissipated in the load resistor and op-amp. The regulated supply provides a maximum current of 440 μA of which 370 μA flows through the scale-adjust leg.

The resistor ladder is composed of 1-per-cent tolerance metal-oxide film resistors available from several manufacturers at modest cost. The five arms requiring the highest accuracy are built of series and parallel combinations of 806-kΩ resistors from the same manufacturing lot. The *ratio match* between resistance values is in the order of 0.2%, usually without need for special selection. The construction of a "standard" with eight parallel resistors assures a high probability that ratio matching will be satisfactory. If the usual assumption that tolerances can be improved with the square-root of the sample number is adopted, the loss of tolerance is slower than the increase of resistance value toward the LSB. Once the most critical match has been attained, therefore, subsequent ratio matches should be more than adequate. An impedance-matching resistor is used between the fifth and sixth bits to permit ladder completion with individual resistors of the most desirable values where a 1% tolerance is adequate. This resistor value is chosen as R5-1/2R6, to terminate the first five bits in a fifth-bit value (the impedance is 1/2R6 looking left into that node).

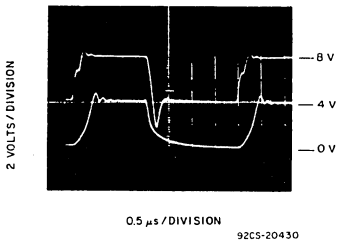



*Fig. 8— Amplifier response to 4—V input pulses.*

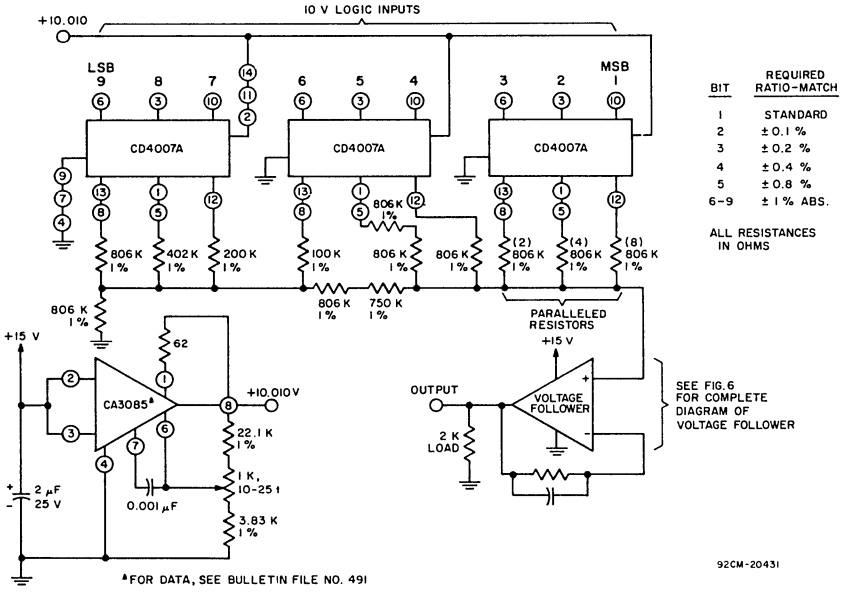



*Fig. 9— 9-bit DAC using COS/MOS CD4007A.*

The follower amplifier has the offset adjustment nulled at approximately a 1-volt output level. System operating potentials are shown in Table I, where each bit is set "low" individually to observe the progression of output values. The positive ladder-supply voltage was adjusted to 10.010 V to provide a small compensation for the MSB switch resistance. A high-impedance 5-digit multimeter, such as the DANA 5330 or equivalent, is needed for direct measurement of the ladder output, and is invaluable during system development and evaluation. Table I shows ideal potential values, system output, and ladder output and illustrates the sources of system inaccuracy. The system output maintains proportional accuracy within ± 5.6 mV, or ± 1/4 LSB.

Fig. 10 shows the system output response to a 4-V logic pulse. The ringing is caused by the voltage follower, and the more gradual transients are caused by voltage-follower and ladder time constants. Settling time to 1/2 LSB is 5 μs.

This 9-bit COS/MOS-DAC demonstrates accuracy and simplicity with economical components and modest power-supply requirements. In addition, the design flexibility afforded by the COS/MOS building blocks simplifies the generation of DAC systems tailored to individual needs. COS/MOS switches used in conjunction with COS/MOS counters also find application in Analog-to-Digital Conversion Systems. The low-power and high noise-immunity features of these devices make them attractive A/D system components.

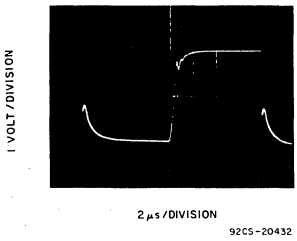
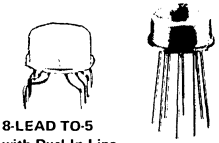



*Fig. 10– System response to most-significant-bit logic pulse.*



**Table I. Set Of Values For 10.010-V Regulated Supply Voltage**

| BINARY WORD | IDEAL POTENTIAL (V) | SYSTEM OUTPUT (V) | LADDER OUTPUT (V) | SYSTEM ERROR (mV) | VOLTAGE FOLLOWER OFFSET (mV) | LADDER & SWITCH ERROR (mV) | POSITIVE SWITCH DROP (mV) |
|---|---|---|---|---|---|---|---|
| 000000000 | 9.9802 | 9.9856 | 9.9915 | + 5.4 | - 5.9 | + 11.3 | – |
| 011111111 | 5.0000 | 4.9959 | 4.9997 | - 4.1 | - 3.8 | - 0.3 | 14.8 |
| 101111111 | 2.5000 | 2.4996 | 2.5023 | - 0.4 | - 2.6 | + 2.3 | 11.0 |
| 110111111 | 1.2500 | 1.2554 | 1.2565 | + 5.4 | - 1.0 | + 6.5 | 6.5 |
| 111011111 | 0.6250 | 0.6233 | 0.6226 | - 2.7 | + 0.7 | - 2.4 | 3.2 |
| 111101111 | 0.3125 | 0.3133 | 0.3113 | + 0.8 | + 2.1 | - 1.2 | 1.7 |
| 111110111 | 0.1568 | 0.1603 | 0.1571 | + 3.5 | + 3.2 | + 0.3 | 14.0 |
| 111111011 | 0.0784 | 0.0826 | 0.0786 | + 4.2 | + 4.0 | + 0.2 | 11.8 |
| 111111101 | 0.0397 | 0.0439 | 0.0393 | + 4.2 | + 4.6 | - 0.4 | 6.8 |
| 111111110 | 0.0198 | 0.0245 | 0.0195 | + 4.7 | + 5.0 | - 0.3 | 3.6 |
| 111111111 | 0.0000 | 0.0056 | 0.0000 | + 5.6 | + 5.6 | 0.0 | – |



8-LEAD TO-5
with Dual-In-Line
Formed Leads

8-LEAD
TO-5

# Applications of the CA3085-Series Monolithic IC Voltage Regulators

by A. C. N. Sheng and L. R. Avery

The RCA-CA3085, CA3085A, and CA3085B monolithic IC's are positive-voltage regulators capable of providing output currents up to 100 milliamperes over the temperature range from $-55^{o}$ to $+125^{o}$C. They are supplied in 8-lead TO-5 type packages; their characteristics and ratings are given in RCA Data File No. 491. The following tabulation shows some key characteristics and salient differences between devices in the CA3085 Series.

| Type | $V_{IN}(V_I)$ Range V | $V_{OUT}(V_O)$ Range V | Max. $I_{OUT}(I_O)$ mA | Max. Load Regulation % $V_O$ |
|---|---|---|---|---|
| CA3085 | 7.5–30 | 1.8–26 | 12* | 0.1 |
| CA3085A | 7.5–40 | 1.7–36 | 100 | 0.15 |
| CA3085B | 7.5–50 | 1.7–46 | 100 | 0.15 |

* This value may be extended to 100 mA; however, regulation is not specified beyond 12 mA.

In addition to these differences, the range of some specified performance parameters is more tightly controlled in the CA3085B than in the CA3085A, and more in the CA3085A than in the CA3085.

This Note describes the basic circuit of the CA3085-series devices and some typical applications that include a high-current regulator, constant-current regulators, a switching regulator, a negative-voltage regulator, a dual-tracking regulator, high-voltage regulators, and various methods of providing current limiting. A circuit in which the CA3085 is used as a general-purpose amplifier is also shown.

### Circuit Description

The block diagram of the CA3085-series circuits is shown in Fig. 1. Fundamentally, the circuit consists of a frequency-compensated error-amplifier which compares an internally generated reference voltage with a sample of the output voltage and controls a series-pass amplifier to regulate the output. The starting circuit assures stable latch-in of the voltage-reference circuitry. The current-limiting portion of the circuit is an optional feature that protects the IC in the event of overload.

Terminal 5 provides a source of stable reference voltage for auxiliary use; a current of about 250 microamperes can be supplied to an external circuit without significantly disturbing reference-voltage stability. If necessary, filtering of the inherent noise of the reference-voltage circuit can be accomplished by connecting a suitable bypass capacitor between terminals 5 and 4.

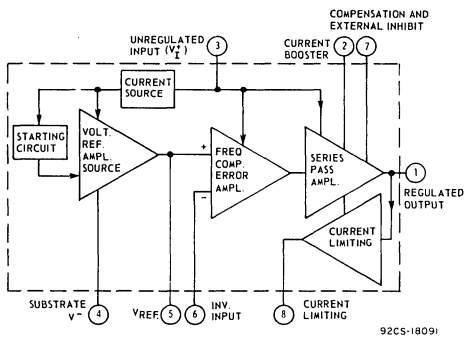



*Fig. 1– Block diagram of CA3085 series.*

Terminal 6 (the "inverting input" in accordance with operational-amplifier terminology) is the input through which a sample of the regulated output voltage is applied.

The collector of the series-pass output transistor is brought out separately at terminal 2 ("current booster") to provide base drive for an external p-n-p transistor; this approach is one method of regulating currents greater than 100 milliamperes.

Because the voltage regulator is essentially an operational amplifier having considerable feedback, frequency compensation is necessary in some circuits to prevent oscillations. Terminal 7 is provided for external frequency compensation; it can also be used to "inhibit" (strobe, squelch, pulse, key) the operation of the series-pass amplifier.

### Brief Description of CA3085 Schematic Diagram

The schematic diagram of the CA3085-series circuits is shown in Fig. 2. The left-hand section includes the starting circuit, the voltage-reference circuit, and the constant-current circuit. The center section is basically an elementary opera-

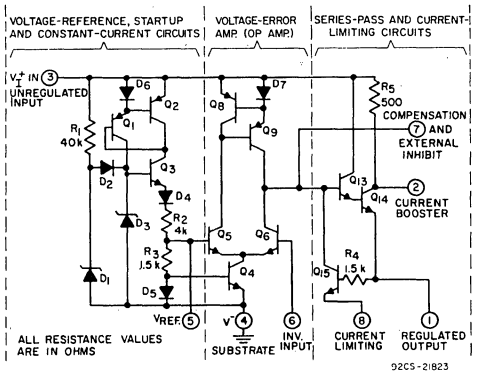



*Fig. 2– Schematic diagram of CA3085 series.*

tional amplifier which serves as the voltage-error amplifier. It controls the series-pass Darlington pair (Q13, Q14) shown in the right-hand section. When controlled by an appropriate external sensing network, transistor Q15 serves to provide protective current-limiting characteristics by diverting base drive from the series-pass circuit. For operation at the highest current levels, terminals 2 and 3 are tied together to eliminate the voltage drop which would otherwise be developed across resistor R5.

### Voltage-Reference Circuits

The basic voltage-reference element used in the CA3085 is zener diode D3. It provides a nominal reference voltage of 5.5 volts and exhibits a positive temperature coefficient of approximately 2.5 millivolts/°C. If this reference voltage were used directly in conjunction with the error-amplifier (Q5, Q6, etc.), the IC would exhibit two major undesirable characteristics: (1) its performance with temperature variations would be poor, and (2) its use as a regulator would be restricted to circuits in which the minimum regulated output voltages are in excess of 5.5 volts. Consequently, it is necessary to provide means of compensating for the positive temperature coefficient of D3 and at the same time provide for obtaining a stable source of lower reference voltage. Both temperature compensation and the reduction of the reference voltage are accomplished by means of the series divider network consisting of the base-emitter junction of Q3, diode D4, resistors R2 and R3, and diode 5.

The voltage developed across D3 drives the divider network and a voltage of approximately 4 volts is developed between the cathode of D4 and the cathode of D5 (terminal 4). The current through this divider network is held nearly constant with temperature because of the combined temperature coefficients of the zener diode (D3), Q3 base-emitter junction, D4 D5, and the resistors R2 and R3. This constant current through the diode D5 and the resistor R3 produces a voltage drop between terminals 4 and 5 that results in the reference voltage (≈ 1.6 volts) having an effective temperature coefficient of about 0.0035 per cent/°C.

The reference diode D3 receives a current of approximately 620 microamperes from a constant-current circuit consisting of Q3 and the current-mirror* D6, Q1, and Q2. Current to startup the constant-current source initially is provided by auxiliary zener diode D1 and R1. Diode D2 blocks current from the R1-D1 source after latch-in of the constant-current source establishes a stable reference potential, and thereby prevents modulation of the reference voltage by ripple voltage on the unregulated input voltage.

### Voltage-Error Amplifier

Transistors Q5 and Q6 comprise the basic differential amplifier that is used as a voltage-error amplifier to compare the stable reference voltage applied at the base of Q5 with a sample of the regulator output voltage applied at terminal 6. The D5-Q4 combination is a current-mirror which maintains essentially constant-current flow to Q5 and Q6 despite variations in the unregulated input voltage. The Q8, Q9, and D7 network provides a "mirrored" active collector load for Q5 and Q6 and also provides a variable single-ended drive to the Q13 and Q14 series-pass transistors in accordance with the difference signal developed between the bases of Q5 and Q6. The open-loop gain of the error-amplifier is greater than 1000.

### Series-Pass and Current-Limiting Circuits

In the normal mode of operation, or in the current-boost mode when terminals 2 and 3 are tied together, the Darlington pair Q13-Q14 performs the basic series-pass regulating function between the unregulated input voltage and the regulated output voltage at terminal 1. In the current-limiting mode transistor Q15 provides current-limiting to protect the CA3085 and/or limit the load current. To provide current-limiting protection, a resistor (e.g., 5 ohms) is connected between terminals 1 and 8; terminal 8 becomes the source of regulated output voltage. As the voltage drop across this resistor increases, base drive is supplied to transistor Q15 so that it becomes increasingly conductive and diverts base drive from the Q13-Q14 pass transistor to reduce output current accordingly. Resistor R4 is provided to protect Q15 against overdrive by limiting its base current under transient and load-short conditions.

Because the CA3085 regulator is essentially an op-amp having considerable feedback, frequency compensation may be required to prevent oscillations. Stability must also be maintained despite line and load transients, even during operation into reactive loads (e.g., filter capacitors). Provisions are included in the CA3085 so that a small-value capacitor may be connected between terminals 6 and 7 to compensate the regulator, when necessary, by "rolling-off" the amplifier frequency-response. Terminal 7 is also used to externally "inhibit" operation of the CA3085 by diverting base current supplied to Q13-Q14, thereby permitting the use of keying, strobing, programming, and/or auxiliary overload-protection circuits.

* The fundamentals of current-mirror theory are reviewed in the Appendix of Application Note ICAN-6668.

## APPLICATIONS

### A Simple Voltage Regulator

Fig. 3 shows the schematic diagram of a simple regulated power supply using the CA3085. The ac supply voltage is stepped down by T1, full-wave rectified by the diode bridge circuit, and smoothed by the large electrolytic capacitor C1 to provide unregulated dc to the CA3085 regulator circuit. Frequency compensation of the error-amplifier is provided by capacitor C2. Capacitor C3 bypasses residual noise in the reference-voltage source, and thus decreases the incremental noise-voltage in the regulator circuit output.

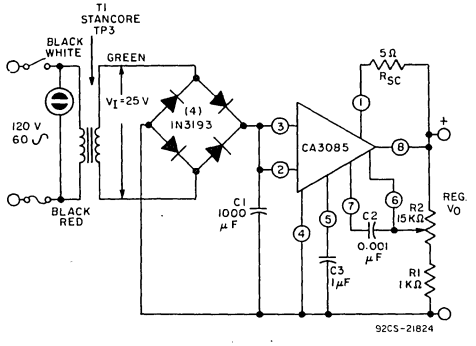



*Fig. 3– Basic power supply.*

Because the open-loop gain of the error-amplifier is very high (greater than 1000), the output voltage may be directly calculated from the following expression:

$$V_O = \frac{(R2 + R1)}{R1} V_{ref} \qquad (1)$$

In the circuit shown in Fig. 3, the output voltage can be adjusted from 1.8 volts to 20 volts by varying R2. The maximum output current is determined by $R_{SC}$; load-regulation characteristics for various values of $R_{SC}$ are shown in Fig. 4.

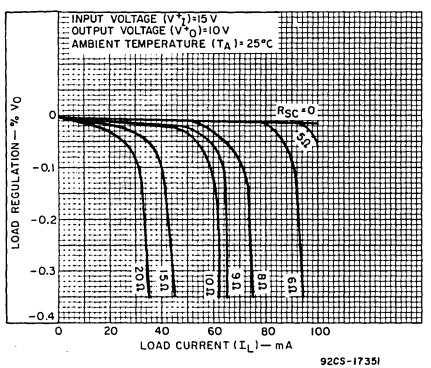



*Fig. 4– Load regulation characteristics for circuit of Fig. 3.*

When this circuit is used to provide high output currents at low output voltages, care must be exercised to avoid excessive IC dissipation. In the circuit of Fig. 3, this dissipation control can be accomplished by increasing the primary-to-secondary transformer ratio (a reduction in $V_I$) or by using a dropping resistor between the rectifier and the CA3085 regulator. Fig. 5 gives data on dissipation limitation ($V_I$-$V_O$ vs. $I_O$) for CA3085-series circuits.

The short-circuit current is determined as follows:

$$I_{SC} = \frac{V_{BE}}{R_{SC}} \approx \frac{0.7}{R_{SC}} \text{ amperes} \qquad (2)$$

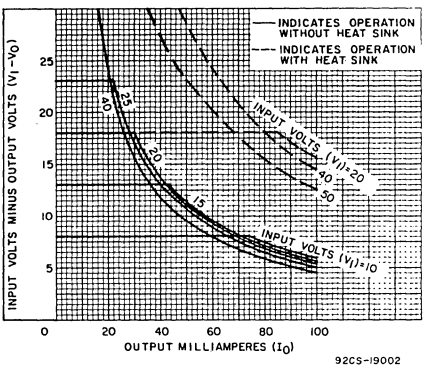


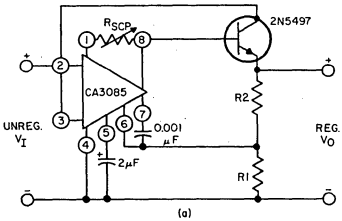

*Fig. 5– Dissipation limitation ($V_I - V_O$ vs. $I_O$) for CA3085 series circuits.*

The line- and load-regulation characteristics for the circuit shown in Fig. 3 are approximately 0.05 per cent of the output voltage.

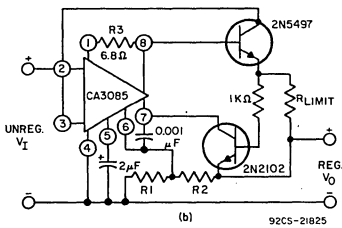
### High-Current Voltage Regulator

When regulated voltages at currents greater than 100 milliamperes are required, the CA3085 can be used in conjunction with an external n-p-n pass-transistor as shown in the circuits of Fig. 6. In these circuits the output current available from the regulator is increased in accordance with the $h_{FE}$ of the external n-p-n pass-transistor. Output currents up to 8 amperes can be regulated with these circuits. A Darlington power transistor can be substituted for the 2N5497 transistor when currents greater than 8 amperes are to be regulated.

A simplified method of short-circuit protection is used in connection with the circuit of Fig. 6(a). The variable resistor $R_{SCP}$ serves two purposes: (1) it can be adjusted to optimize the base drive requirements ($h_{FE}$) of the particular 2N5497 transistor being used, and (2) in the event of a short-circuit in the regulated output voltage the base drive current in the 2N5497 will increase, thereby increasing the voltage drop




*(a) with simplified short-circuit protection*




*(b) with auxiliary short-circuit protection*

*Fig. 6– High-current voltage regulator using n-p-n pass transistor.*

across $R_{SCP}$. As this voltage-drop increases the short-circuit protection system within the CA3085 correspondingly reduces the output current available at terminal 8, as described previously. It should be noted that the degree of short-circuit protection depends on the value of $R_{SCP}$, i.e., design compromise is required in choosing the value of $R_{SCP}$ to provide the desired base drive for the 2N5497 while maintaining the desired short-circuit protection. Fig. 6(b) shows an alternate circuit in which an additional transistor (2N2102) and two resistors have been added as an auxiliary short-circuit protection feature. Resistor R3 is used to establish the desired base drive for the 2N5497, as described above. Resistor $R_{limit}$ now controls the short-circuit output current because, in the event of a short-circuit, the voltage drop developed across its terminals increases sufficiently to increase the base drive to the 2N2102 transistor. This increase in base drive results in reduced output from the CA3085 because collector current flow in the 2N2102 diverts base drive from the Darlington output stage of the CA3085 (see Fig. 2) through terminal 7. The load regulation of this circuit is typically 0.025 per cent with 0 to 3-ampere load-current variation; line regulation is typically 0.025 per cent/volt change in input voltage.

### Voltage Regulator with Low $V_I$-$V_O$ Difference

In the voltage regulators described in the previous section, it is necessary to maintain a minimum difference of about 4 volts between the input and output voltages. In some applications this requirement is prohibitive. The circuit shown in Fig. 7 can deliver an output current in the order of 2 amperes with a $V_I$-$V_O$ difference of only one volt.

It employs a single external p-n-p transistor having its base and emitter connected to terminals 2 and 3, respectively, of the CA3085. In this circuit, the emitter of the output transistor (Q14 in Fig. 2) in the CA3085 is returned to the negative supply rail through an external resistor ($R_{SCP}$) and two series-connected diodes (D1, D2). These forward-biased diodes maintain Q6 in the CA3085 within linear-mode operation. The

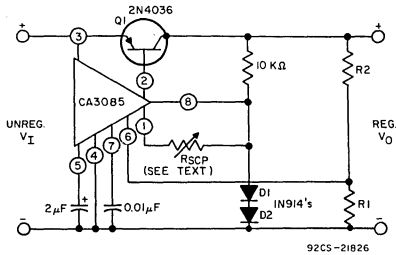



*Fig. 7– Voltage regulator for low $V_I - V_O$ difference.*

choice of resistors R1 and R2 is made in accordance with Eq. (1). Adequate frequency compensation for this circuit is provided by the 0.01-microfarad capacitor connected between terminal 7 of the CA3085 and the negative supply rail.

Fig. 8, which shows the output impedance of the circuit of Fig. 7 as a function of frequency, illustrates the excellent ripple-rejection characteristics of this circuit at frequencies below 1 kHz. Lower output impedances at the higher frequencies can be provided by connecting an appropriate capacitor across the output voltage terminals. The addition of a capacitor will, however, degrade the ability of the system to react to transient-load conditions.

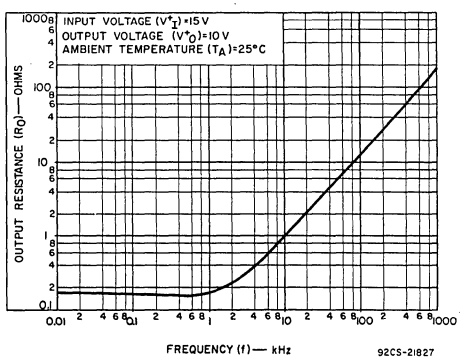



*Fig. 8– Output resistance vs. frequency for circuit of Fig. 7.*

### High-Voltage Regulator

Fig. 9 shows a circuit that uses the CA3085 as a voltage-reference and regulator control device for high-voltage power supplies in which the voltages to be regulated are well above the input-voltage ratings of the CA3085-series circuits. The external transistors Q1 and Q2 require voltage ratings in excess of the maximum input voltage to be regulated. Series-pass transistor Q2 is controlled by the collector current of Q1, which in turn is controlled by the normally regulated current output supplied by the CA3085. The input voltage for the CA3085

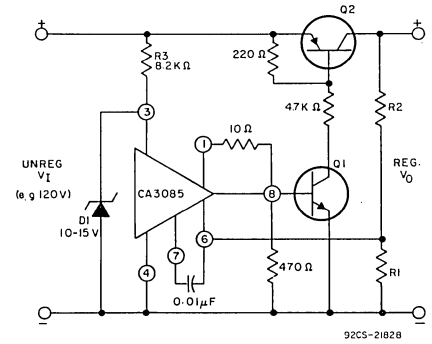



*Fig. 9— High-voltage regulator.*

regulator at terminal 3 is supplied through dropping resistor R3 and the clamping zener diode D1. The values for resistor R1 and R2 are determined in accordance with Eq. (1).

### Negative-Voltage Regulator

The CA3085 is used as a negative-supply voltage regulator in the circuit shown in Fig. 10. Transistor Q3 is the series-pass transistor. It should be noted that the CA3085 is effectively connected across the load-side of the regulated system. Diode D1 is used initially in a "circuit-starter" function; transistor Q2 "latches" D1 out of its starter-circuit function so that the CA3085 can assume its role in controlling the pass-transistor Q3 by means of Q1.

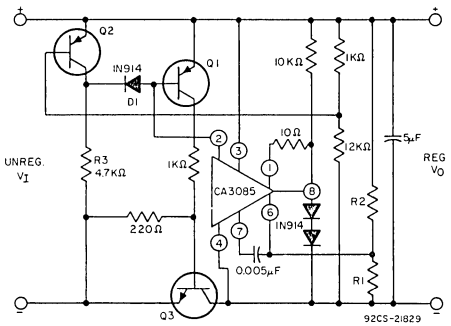



*Fig. 10— Negative-voltage regulator.*

Operation of the circuit is as follows: current through R3 and D1 provides base drive for Q1, which in turn provides base drive for the pass-transistor Q3. By this means operating potential for the CA3085 is developed between the collector of Q3 (terminal 4 of the CA3085) and the positive supply-rail (terminal 3 of the CA3085). When the output voltage has risen sufficiently to maintain operation of the CA3085 (approx. 7.5 volts), transistor Q2 is driven into conduction by the base drive supplied from the 1 kilohm-12 kilohm voltage divider. As Q2 becomes conductive, it diverts the base drive being supplied to Q1 through the R3-D1 path, and diode D1 ceases to conduct. Under these conditions, base-current drive to Q1 through terminal 2 of the CA3085 regulates the base drive to Q3. Values of R1 and R2 are determined in accordance with Eq. (1).

The circuit shown in Fig. 11 is similar to that of Fig. 10, except for the addition of a constant-current limiting circuit

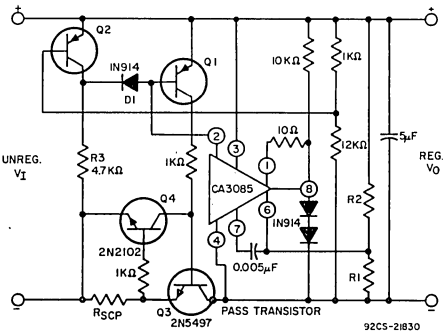



*Fig. 11— Negative-voltage regulator with constant-current limiting circuit.*

consisting of transistor Q4, a 1-kilohm resistor, and resistor $R_{SCP}$. When the load current increases above a particular design value, the corresponding increase in the voltage drop across resistor $R_{SCP}$ provides additional base drive to transistor Q4. Thus, as transistor Q4 becomes increasingly conductive, its collector current diverts sufficient base drive from Q3 to limit the current in the pass transistor feeding the regulated load. With the types of transistors shown in Figs. 10 and 11, maximum currents in the order of 5 amperes can be regulated.

### High-Output-Current Voltage Regulator With "Foldback" Current-Limiting (Also known as "Switch-Back" Current-Limiting)

In high-current voltage regulators employing constant-current limiting (e.g., Figs. 6 and 7), it is possible to develop excessive dissipation in the series-pass transistor when a short-circuit develops across the output terminals. This situation can be avoided by the use of the "foldback" current-limiting circuitry as shown in Fig. 12. In this circuit, terminal 8 of the

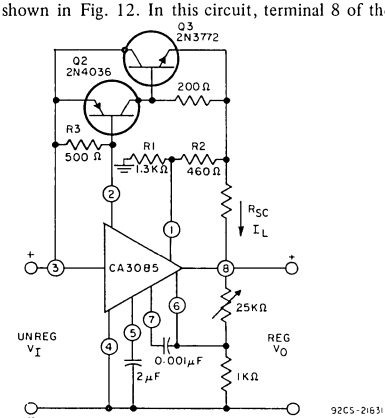



*Fig. 12— High-output-current voltage regulator with "foldback" current limiting.*

CA3085 senses the output voltage, and terminal 1 is tied to a tap on a voltage-divider network connected between the emitter of the pass-transistor (Q3) and ground. The current-foldback trip-point is established by the value of resistor $R_{SC}$.

The protective tripping action is accomplished by forward-biasing Q15 in the CA3085 (see Fig. 2). Conditions for tripping-circuit operation are defined by the following expressions:

$$V_{BE(Q15)} = (\text{voltage at terminal 1}) - (\text{output voltage})$$

$$= \left[(V_O + I_L R_{SC})\frac{R1}{R1 + R2}\right] - V_O \qquad (3)$$

$$\text{If } \frac{R1}{R1 + R2} = K, \text{ then}$$

$$V_{BE(Q15)} = (V_O + I_L R_{SC})\,K - V_O = KV_O + KI_L R_{SC} - V_O$$

and therefore

$$R_{SC} = \frac{V_O + V_{BE(Q15)} - KV_O}{KI_L} \qquad (4)$$

Under load short-circuit conditions, terminal 8 is forced to ground potential and current flows from the emitter of Q14 in the CA3085, establishing terminal 1 at one $V_{BE}$-drop [≅ 0.7 V] above ground and Q15 in a partially conducting state. The current through Q14 necessary to establish this one-$V_{BE}$ condition is the sum of currents flowing to ground through R1 and [R2 + $R_{SC}$]. Normally $R_{SC}$ is much smaller than R2 and can be ignored; therefore, the equivalent resistance $R_{eq}$ to ground is the parallel combination of R1 and R2. The Q14 current is then given by:

$$I_{Q14} = \frac{V_{BE(Q15)}}{R_{eq}} = \frac{V_{BE(Q15)}}{\frac{R1R2}{R1 + R2}} = \frac{0.7\ [\,1.3 + 0.46\,]}{1.3 \times 0.46} = 2.06 \text{ milliamperes}$$

This current provides a voltage between terminals 2 and 3 as follows:

$$V_{2-3} = I_{Q14} \times 250 \text{ ohms} = 2.06 \times 10^{-3} \times 250 = 0.515 \text{ volt}$$

The effective resistance between terminals 2 and 3 is 250 ohms because the external 500-ohm resistor R3 is in parallel with the internal 500-ohm resistor R5. It should be understood that the $V_{2-3}$ potential of 0.515 volt is insufficient to maintain the external p-n-p transistor Q2 in conduction, and, therefore, Q3 has no base drive. Thus the output current is reduced to zero by the protective circuitry. Fig. 13 shows the foldback characteristic typical of the circuit of Fig. 12.

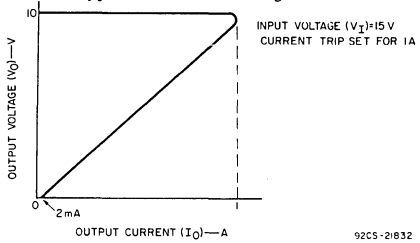



*Fig. 13– Typical "foldback" current-limiting characteristic for circuit of Fig. 12.*

An alternative method of providing "foldback" current-limiting is shown in Fig. 14. The operation of this circuit is similar to that of Fig. 12 except that the foldback-control transistor Q2 is external to the CA3085 to permit added flexibility in protection-circuit design.

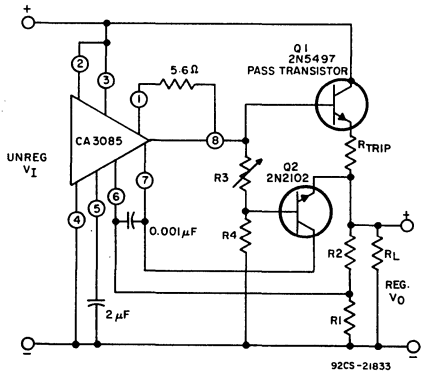



*Fig. 14– High-output-current voltage regulator using auxiliary transistor to provide "foldback" current limiting.*

Under low load conditions Q2 is effectively reverse-biased by a small amount, depending upon the values of R3 and R4. As the load current increases the voltage drop across $R_{trip}$ increases, thereby raising the voltage at the base of Q1, and Q2 starts to conduct. As Q2 becomes increasingly conductive it diverts base current from transistors Q13 and Q14 in the CA3085, and thus reduces base drive to the external pass-transistor Q1 with a consequent reduction in the output voltage. The point at which current-limiting occurs, $I_{trip}$, is calculated as follows:

$V_{BE(Q1)}$ = voltage at terminal 8 − $V_O$ (assuming a low value for $R_{trip}$)

$$V_{BE(Q2)} = \text{voltage at terminal 8}\left(\frac{R4}{R3 + R4}\right) - V_O$$

$$= \left[V_O + I_L R_{trip} + V_{BE(Q1)}\right]\left[\frac{R4}{R3 + R4}\right] - V_O$$

if $K = \frac{R4}{R3 + R4}$, then the trip current is given by:

$$I_{trip} = \frac{V_{BE(Q2)} - K\left[V_O + V_{BE(Q1)}\right] + V_O}{KR_{trip}} \qquad (7)$$

In the circuit in Fig. 12 the load current goes to zero when a short circuit occurs. In the circuit of Fig. 14 the load current is significantly reduced but does not go to zero. The value for $I_{SC}$ is computed as follows:

$$V_{BE(Q2)} + \left[\frac{V_{BE(Q2)}}{R2} + I_{B(Q2)}\right] R1 = V_{BE(Q1)} + I_{SC}R_{trip}$$

$$I_{SC} = \frac{V_{BE(Q2)} + \left[\frac{V_{BE(Q2)}}{R2} + I_{B(Q2)}\right] R1 - V_{BE(Q1)}}{R_{trip}} \qquad (8)$$

Fig. 15 shows that the transfer characteristic of the load current is essentially linear between the "trip-point" and the "short-circuit" point.

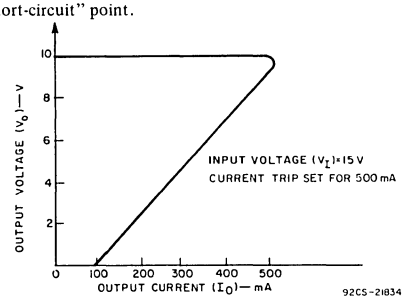



*Fig. 15— Typical foldback current-limiting characteristic for circuit of Fig. 14.*

### High-Voltage Regulator Employing Current "Snap-Back" Protection

In high-voltage regulators (e.g., see Fig. 9), "foldback" current-limiting cannot be used safely because the high voltage across the pass transistor can cause second breakdown despite the reduction in current flow. To adequately protect the pass transistor in this type of high-voltage regulator, the so-called "snap-back" method of current limiting can be employed to reduce the current to zero in a few microseconds, and thus prevent second-breakdown destruction of the device.

The circuit diagram of a high-voltage regulator employing current "snap-back" protection is shown in Fig. 16. The basic regulator circuit is similar to that shown in Fig. 9. The additional circuitry in the circuit of Fig. 16 quickly interrupts base drive to the pass transistor in event of load fault. The point of current-trip is established as follows:

$$I_{trip} = \frac{V_{BE(Q1)}}{R_{SC}} \qquad (9)$$

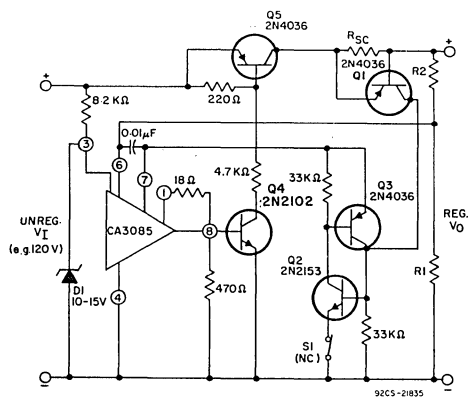



*Fig. 16— High-voltage regulator incorporating current "snap-back" protection.*

Thus, when a sufficient voltage drop is developed across $R_{SC}$, transistor Q1 becomes conductive and current flows into the base of Q2 so that it also becomes conductive. Transistor Q3, in turn, is driven into conduction, thereby latching the Q2-Q3 combination (basic SCR action) so that it diverts (through terminal 7) base drive from the output stage (Q13, Q14) in the CA3085. By this means, base drive is diverted from Q4 and the pass transistor Q5. To restore regulator operation, normally closed switch S1 is momentarily opened and unlatches Q2-Q3.

### Switching Regulator

When large input-to-output voltage differences are necessary, the regulators described above are inefficient because they dissipate significant power in the series-pass transistor. Under these conditions, high-efficiency operation can be achieved by using a switching-type regulator of the generic type shown in Fig. 17(a). Transistor Q1 acts as a keyed switch and operates in

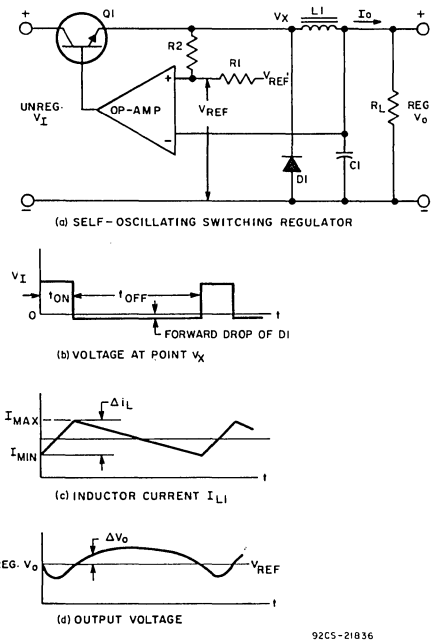



*Fig. 17— Switching regulator and associated waveforms.*

either a saturated or cut-off condition to minimize dissipation. When transistor Q1 is conductive, diode D1 is reverse-biased and current in the inductance L1 increases in accordance with the following relationship:

$$i_L = \frac{1}{L}\int_{t_o}^{t_1} V dt \qquad (10)$$

where V is the voltage across the inductance L1. The current through the inductance charges the capacitor C1 and supplies current to the load. The output voltage rises until it slightly exceeds the reference voltage $V_{ref}$. At this point the op-amp removes base drive to Q1 and the unregulated input voltage $V_I$ is "switched off". The energy stored in the inductor L1 now causes the voltage at $V_X$ to swing in the negative direction and current flows through diode D1, while continuing to supply current into the load $R_L$. As the current in the inductor falls below the load current, the capacitor C1 begins to discharge and $V_O$ decreases. When $V_O$ falls slightly below the value of $V_{ref}$, the op-amp turns on Q1 and the cycle is repeated. It should be apparent that the output voltage oscillates about $V_{ref}$ with an amplitude determined by R1 and R2. Actually, the value of $V_{ref}$ varies from being slightly more positive than $V_{ref}'$ when Q1 is conducting, to being slightly more negative than $V_{ref}'$ when D1 is conducting. The voltage and current waveforms are shown in Fig. 17(b), (c), and (d).

**Design Example:** The following specifications are used in decomputations for a switching regulator:

$V_I = 30$ V, $V_O = 5$ V, $I_O = 500$ mA,
switching frequency = 20 kHz,
output ripple = 100 mV.

If it is assumed that transistor Q1 is in steady-state saturated operation with a low voltage-drop, the current in the inductor is given by Eq. 10, as follows:

$$i_L = \frac{1}{L}\int_{t_o}^{t_1} V dt = \left(\frac{V_I - V_O}{L1}\right) t_{on} \qquad (11)$$

When transistor Q1 is off, the current in the inductor is given by:

$$i_L \cong \frac{(V_O + V_{D1})\, t_{off}}{L1} \qquad (12)$$

From Eq. 11,

$$L_1 = \frac{(V_I - V_O)}{i_L} \cdot \frac{1}{f} \cdot \frac{V_O}{V_I} \qquad (13)$$

If $i_{max}$ is 1.3 $I_L$, then during $t_{on}$ the current in the inductor ($i_L$) will be 0.5 A x 1.3 = 0.65 A; therefore, $\Delta i_L$ = 0.15 A

Substitution in Eq. 13 yields

$$L_1 = \frac{(30 - 5)}{0.15} \cdot \frac{1}{(20 \times 10^3)} \cdot \frac{5}{30} = 1.4 \text{ mH} \qquad (14)$$

Current discharge from the capacitor C1 is given by:

$$i_c = C\frac{dv}{dt} \qquad (15)$$

Thus, $\Delta i_c = C\frac{\Delta v}{\Delta t}$, or $C = \frac{\Delta i_c\ \Delta t}{\Delta v}$

Since $i_c = i_L$ and $\Delta t = t_{off}$, then

$$C = \frac{\Delta i_L\ t_{off}}{\Delta v}$$

Substitution for the value of $i_L$ from Eq. 13 yields

$$C = \frac{\left(\frac{V_I - V_O}{L1}\right) \cdot \frac{1}{f} \cdot \left(\frac{V_O}{V_I}\right) \cdot t_{off}}{\Delta v} \qquad (16)$$

The total period $T = t_{off} + t_{on}$, and $T = \frac{1}{f}$. Therefore,

$$t_{off} = \frac{1}{f} - t_{on} \qquad (17)$$

For optimum efficiency $t_{on}$ should be

$$\cong \left(\frac{V_O}{V_I}\right) T \cong \left(\frac{V_O}{V_I}\right) \frac{1}{f} \qquad (18)$$

Substitution for $t_{on}$ in Eq. 18 yields

$$t_{off} = \frac{1}{f} - \left(\frac{V_O}{V_I}\right)\frac{1}{f} = \frac{1}{f}\left(1 - \frac{V_O}{V_I}\right) \qquad (19)$$

Substitution for $t_{off}$ in Eq. 16 yields

$$C = \frac{\frac{(V_I - V_O)}{L_1} \cdot \frac{1}{f} \cdot \frac{V_O}{V_I} \cdot \frac{1}{f} \cdot \left(1 - \frac{V_O}{V_I}\right)}{\Delta v}$$

Substitution of numerical values in Eq. 20 produces the following value for C:

$$C = \frac{\frac{30 - 5}{1.4 \times 10^{-3}} \cdot \frac{1}{20 \times 10^3} \cdot \frac{5}{30} \cdot \frac{1}{20 \times 10^3} \cdot \left(1 - \frac{5}{30}\right)}{10^{-1}} = 63\ \mu F$$

A switching-regulator circuit using the CA3085 is shown in Fig. 18. The values of L and C (1.5 millihenries and 50 microfarads, respectively) are commercially available components having values approximately equal to the computed values in the previous design example.

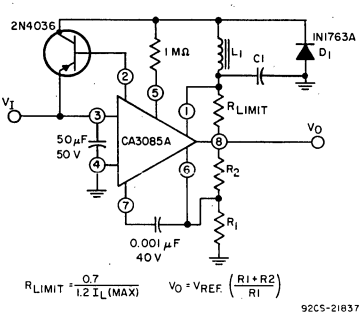
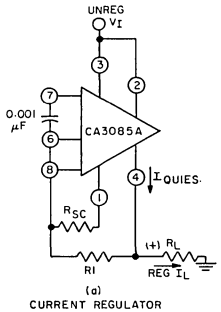



*Fig. 18– Typical switching regulator circuit.*

### Current Regulators

The CA3085 series of voltage regulators can be used to provide a constant source or sink current. A regulated-current supply capable of delivering up to 100 milliamperes is shown in Fig. 19(a). The regulated load current is controlled by R1 because the current flowing through this resistor must establish a voltage difference between terminals 6 and 4 that is equal to the internal reference voltage developed between terminals 5 and 4. The actual regulated current, reg $I_L$, is the sum of the quiescent regulator current and the current through R1, i.e.,

$$\text{reg } I_L = I_{quiescent} + I_{R1}$$



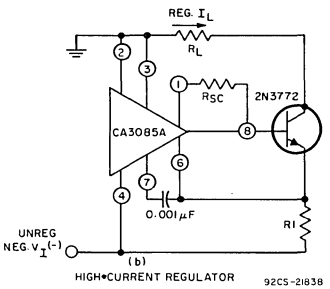




*Fig. 19– Constant current regulators.*

Fig. 19(b) shows a high-current regulator using the CA3085 in conjunction with an external n-p-n transistor to regulate currents up to 3 amperes. In this circuit the quiescent regulator current does not flow through the load and the output current can be directly programmed by R1, i.e.,

$$\text{Reg } I_L = \frac{V_{ref}}{R1}$$

With this regulator currents between 1 milliampere and 3 amperes can be programmed directly. At currents below 1 milliampere inaccuracies may occur as a result of leakage in the external transistor.

### A Dual-Tracking Voltage Regulator

A dual-tracking voltage regulator using a CA3085 and a CA3094A* is shown in Fig. 20. The CA3094A is basically an op-amp capable of supplying 100 milliamperes of output current.

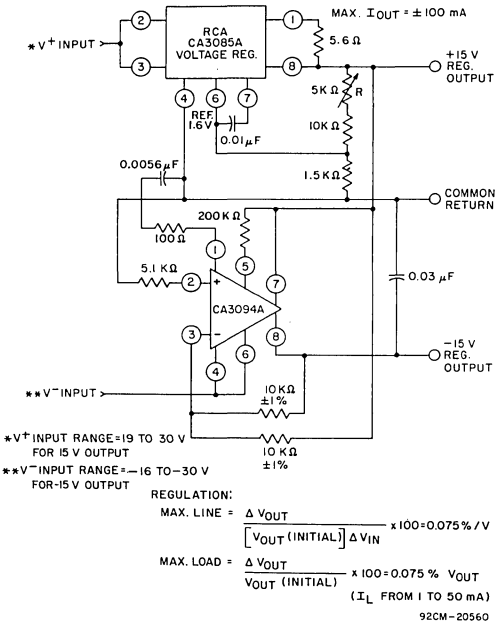



*Fig. 20– Dual-voltage tracking regulator.*

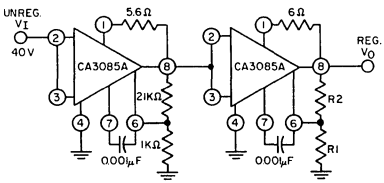
The positive output voltage is regulated by a CA3085 operating in a configuration essentially similar to that described in connection with Fig. 3. Resistor R is used as a vernier adjustment of output voltage. The negative output voltage is regulated by the CA3094A, which is "slaved" to the regulated positive voltage supplied by the CA3085. It should be noted that the non-inverting input of the CA3094A and the negative supply terminal of the CA3085 are connected to a common ground reference. The "slaving" potential for the CA3094A is derived from an accurate 1:1 voltage-divider network comprised of two 10-kilohm resistors connected between the +15-volt and −15-volt output terminals. The junction of these two resistors is connected to the inverting input of the CA3094A. The voltage at this junction is compared with the voltage at the non-inverting input, and the CA3094A then automatically adjusts the output current at the negative terminal to maintain a negative regulated output voltage essentially equal to the regulated positive output voltage. Typical performance data for this circuit are shown in Fig. 20.

* Specifications for the CA3094A appear in RCA Data File No. 598 and application information is presented in ICAN-6048.

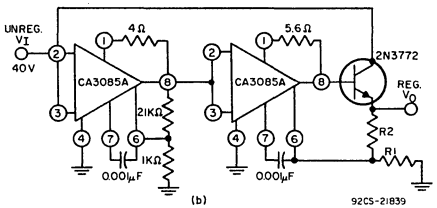
The basic circuit of Fig. 20 can be modified to regulate dissimilar positive and negative voltages (e.g., +15 V, −5 V) by appropriate selection of resistor ratios in the voltage-divider network discussed previously. As an example, to provide tracking of the +15 V and −5 V regulated voltages with the circuit of Fig. 20, it is only necessary to replace the 10-kilohm resistor connected between terminals 3 and 8 of the CA3094A with a 3.3-kilohm resistor.

### Regulators With High Ripple Rejection

When the reference-voltage source in the CA3085 is adequately filtered, the typical ripple rejection provided by the circuit is 56 dB. It is possible to achieve higher ripple-rejection performance by cascading two stages of the CA3085, as shown in Fig. 21. The voltage-regulator circuit in Fig. 21(a) provides 90 dB of ripple rejection. The output voltage is adjustable over the range from 1.8 to 30 volts by appropriate adjustment of resistors R1 and R2. Higher regulated output currents up to 1 ampere can be obtained with this circuit by adding an external n-p-n transistor as shown in Fig. 21(b).




*(a) voltage regulator with high ripple rejection*




*(b) high-current voltage regulator with high ripple rejection*

*Fig. 21– Regulators with high ripple rejection.*

### The CA3085 As A Power Source For Sensors

Certain types of sensor applications require a regulated power source. Additionally, low-impedance sensors can consume significant power. An example of a circuit with these requirements, in which a CA3085 provides regulated power for a low-impedance sensor and the CA3059* zero-voltage switch, is shown in Fig. 22. Terminal 12 on the CA3059 provides the ac trigger-signal which actuates the zero-voltage switch synchronously with the power line to control the load-switching triac.

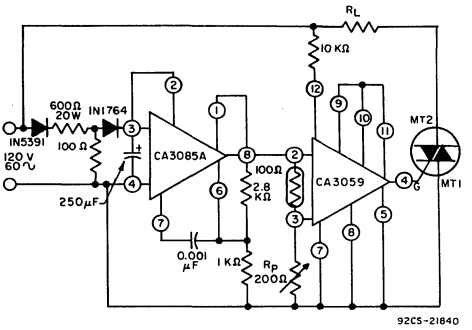



*Fig. 22– Voltage regulator for sensor and zero-voltage switch.*

### The CA3085 As A General-Purpose Amplifier

As described above, the CA3085 series regulators contain a high-gain linear amplifier having a current-output capability up to 100 milliamperes. The premium type (CA3085B) can operate at supply voltages up to 50 volts. When equipped with an appropriate radiator or heat-sink, the TO-5 package of these devices can dissipate up to 1.6 watts at 55°C. A very stable internal voltage-reference source is used to bias the high-gain amplifier and/or provide an external voltage-reference despite extreme temperature or supply-voltage variations. These factors, plus economics, prompt consideration of this circuit for general-purpose uses, such as amplifiers, relay controls, signal-lamp controls, and thyristor firing.

As an example, Fig. 23 shows the application of the CA3085 in a general-purpose amplifier. Under the conditions shown,

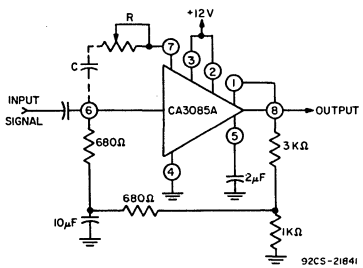



*Fig. 23– General purpose amplifier using CA3085A.*

the circuit has a typical gain of 70 dB with a flat response to at least 100 kHz without the RC network connected between terminals 6 and 7. The RC network is useful as a tone control or to "roll-off" the amplifier response for other reasons. Current limiting is not used in this circuit. The network connected between terminals 8 and 6 provides both dc and ac feedback. This circuit is also applicable for directly driving an external discrete n-p-n power transistor.

* Technical specifications for RCA integrated-circuit zero-voltage switches CA3058, CA3059, and CA3079 appear in File No. 490; related application information is given in ICAN-6182.

# Features and Applications of RCA Integrated-Circuit Zero-Voltage Switches (CA3058, CA3059, and CA3079)

by A. C. N. Sheng, G. J. Granieri, and J. Yellin

RCA-CA3058, CA3059 and CA3079 zero-voltage switches are monolithic integrated circuits designed primarily for use as trigger circuits for thyristors in many highly diverse ac power-control and power-switching applications. These integrated-circuit switches operate from an ac input voltage of 24, 120, 208 to 230, or 277 volts at 50, 60, or 400 Hz.

The CA3059 and CA3079 are supplied in a 14-terminal dual-in-line plastic package. The CA3058 is supplied in a 14-terminal dual-in-line ceramic package. The electrical and physical characteristics of each type are detailed in RCA Data Bulletin File No. 490.

RCA zero-voltage switches (ZVS) are particularly well suited for use as thyristor trigger circuits. These switches trigger the thyristors at zero-voltage points in the supply-voltage cycle. Consequently, transient load-current surges and radio-frequency interference (RFI) are substantially reduced. In addition, use of the zero-voltage switches also reduces the rate of change of on-state current (di/dt) in the thyristor being triggered, an important consideration in the operation of thyristors. These switches can be adapted for use in a variety of control functions by use of an internal differential comparator to detect the difference between two externally developed voltages. In addition, the availability of numerous terminal connections to internal circuit points greatly increases circuit flexibility and further expands the types of ac power-control applications to which these integrated circuits may be adapted. The excellent versatility of the zero-voltage switches is demonstrated by the fact that these circuits have been used to provide transient-free temperature control in self-cleaning ovens, to control gun-muzzle temperature in low-temperature environments, to provide sequential switching of heating elements in warm-air furnaces, to switch traffic signal lights at street intersections, and to effect other widely different ac power-control functions.

## FUNCTIONAL DESCRIPTION

RCA zero-voltage switches are multistage circuits that employ a diode limiter, a zero-crossing (threshold) detector, an on-off sensing amplifier (differential comparator), and a Darlington output driver (thyristor gating circuit) to provide the basic switching action. The dc operating voltages for these stages is provided by an internal power supply that has sufficient current capability to drive external circuit elements, such as transistors and other integrated circuits. An important feature of the zero-voltage switches is that the output trigger pulses can be applied directly to the gate of a triac or a silicon controlled rectifier (SCR). The CA3058 and CA3059 also feature an interlock (protection) circuit that inhibits the application of these pulses to the thyristor in the event that the external sensor should be inadvertently opened or shorted. An external inhibit connection (terminal No. 1) is also available so that an external signal can be used to inhibit the output drive. This feature is not included in the CA3079; otherwise, the three integrated-circuit zero-voltage switches are electrically identical.

### Over-all Circuit Operation

Fig. 1 shows the functional interrelation of the zero-voltage switch, the external sensor, the thyristor being triggered, and the load elements in an on-off type of ac power-control system. As shown, each of the zero-voltage switches incorporates four functional blocks as follows:

(1) Limiter-Power Supply – Permits operation directly from an ac line.

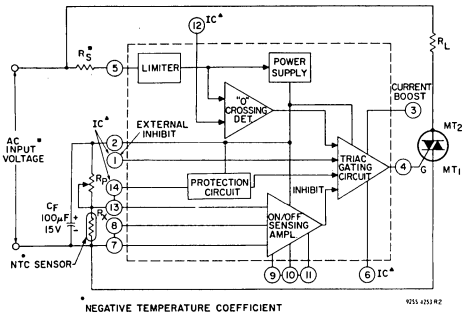
(2) Differential On/Off Sensing Amplifier – Tests the condition of external sensors or command signals. Hysteresis or proportional-control capability may easily be implemented in this section.

(3) Zero-Crossing Detector – Synchronizes the output pulses of the circuit at the time when the ac cycle is at a zero-voltage point and thereby eliminates radio-frequency inteference (RFI) when used with resistive loads.

(4) Triac Gating Circuit – Provides high-current pulses to the gate of the power-controlling thyristor.

In addition, the CA3058 and CA3059 provide the following important auxiliary functions (shown in Fig. 1):

(1) A built-in protection circuit that may be actuated to remove drive from the triac if the sensor opens or shorts.




| AC Input Voltage (50/60 or 400 Hz) V AC | Input Series Resistor ($R_S$) k Ω | Dissipation Rating for $R_S$ W |
|---|---|---|
| 24 | 2 | 0.5 |
| 120 | 10 | 2 |
| 208/230 | 20 | 4 |
| 277 | 25 | 5 |

*Fig. 1 – Functional block diagrams of the zero-voltage switches CA3058, CA3059, and CA3079.*

(2) Thyristor firing may be inhibited through the action of an internal diode gate connected to terminal 1.

(3) High-power dc-comparator operation is provided by overriding the action of the zero-crossing detector. This override is accomplished by connecting terminal 12 to terminal 7. Gate current to the thyristor is continuous when terminal 13 is positive with respect to terminal 9.

Fig. 2 shows the detailed circuit diagram for the integrated-circuit zero-voltage switches. (The diagrams shown in Figs. 1 and 2 are representative of all three RCA zero-voltage switches, i.e., the CA3058, CA3059, and CA3079; the shaded areas indicate the circuitry that is not included in the CA3079.)

The limiter stage of the zero-voltage switch clips the incoming ac line voltage to approximately ±8 volts. This signal is then applied to the zero-voltage-crossing detector, which generates an output pulse each time the line voltage passes through zero. The limiter output is also applied to a rectifying diode and an external capacitor, $C_F$, that comprise the dc power supply. The power supply provides approximately 6 volts as the $V_{CC}$ supply to the other stages of the zero-voltage switch. The on-off sensing amplifier is basically a differential comparator. The thyristor gating circuit contains a driver for direct triac triggering. The gating circuit is enabled when all the inputs are at a "high" voltage, i.e., the line voltage must be approximately zero volts, the sensing-amplifier output must be "high," the external voltage to terminal 1 must be a logical "0", and, for the CA3058 and CA3059, the output of the fail-safe circuit must be "high." Under these conditions, the thyristor (triac or SCR) is triggered when the line voltage is essentially zero volts.

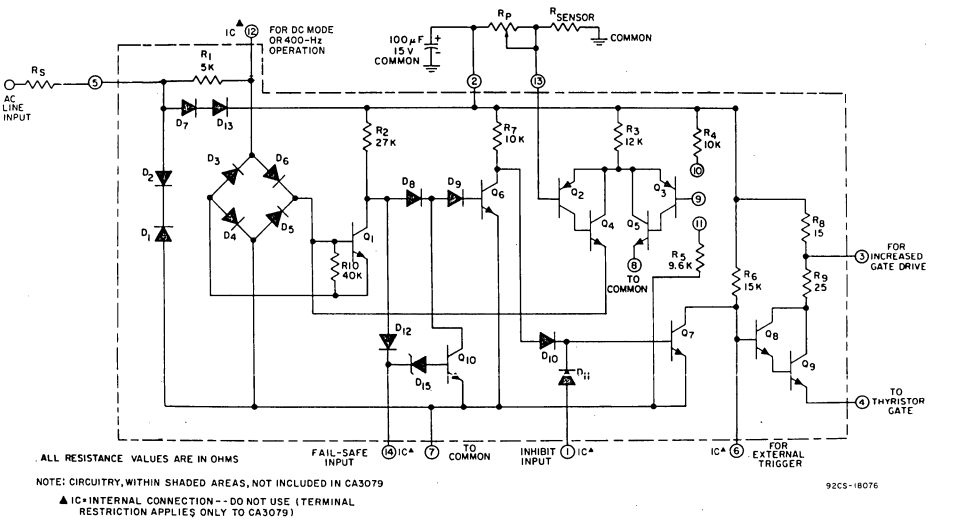



*Fig. 2 – Schematic diagram of zero-voltage switches CA3058, CA3059, and CA3079.*

### Thyristor Triggering Circuits

The diodes $D_1$ and $D_2$ in Fig. 2 form a symmetrical clamp that limits the voltages on the chip to ±8 volts; the diodes $D_7$ and $D_{13}$ form a half-wave rectifier that develops a positive voltage on the external storage capacitor, $C_F$.

The output pulses used to trigger the power-switching thyristor are actually developed by the zero-crossing detector and the thyristor gating circuit. The zero-crossing detector consists of diodes $D_3$ through $D_6$, transistor $Q_1$, and the associated resistors shown in Fig. 2. Transistors $Q_1$ and $Q_6$ through $Q_9$ and the associated resistors comprise the thyristor gating circuit and output driver. These circuits generate the output pulses when the ac input is at a zero-voltage point so that RFI is virtually eliminated when the zero-voltage switch and thyristor are used with resistive loads.

The operation of the zero-crossing detector and thyristor gating circuit can be explained more easily if the on state (i.e., the operating state in which current is being delivered to the thyristor gate through terminal 4) is considered as the operating condition of the gating circuit. Other circuit elements in the zero-voltage switch inhibit the gating circuit unless certain conditions are met, as explained later.

In the on state of the thyristor gating circuit, transistors $Q_8$ and $Q_9$ are conducting, transistor $Q_7$ is off, and transistor $Q_6$ is on. Any action that turns on transistor $Q_7$ removes the drive from transistor $Q_8$ and thereby turns off the thyristor. Transistor $Q_7$ may be turned on directly by application of a minimum of +1.2 volts at 10 microamperes to the external-inhibit input, terminal 1. (If a voltage of more than 1.5 volts is available, an external resistance must be added in series with terminal 1 to limit the current to 1 milliampere.) Diode $D_{10}$ isolates the base of transistor $Q_7$ from other signals when an external-inhibit signal is applied so that this signal is the highest priority command for normal operation. (Although grounding of terminal 6 creates a higher-priority inhibit function, this level is not compatible with normal DTL or TTL logic levels.) Transistor $Q_7$ may also be activated by turning off transistor $Q_6$ to allow current flow from the power supply through resistor $R_7$ and diode $D_{10}$ into the base of $Q_7$. Transistor $Q_6$ is normally maintained in conduction by current that flows into its base through resistor $R_2$ and diodes $D_8$ and $D_9$ when transistor $Q_1$ is off.

Transistor $Q_1$ is a portion of the zero-crossing detector. When the voltage at terminal 5 is greater than +3 volts, current can flow through resistor $R_1$, diode $D_6$, the base-to-emitter junction of transistor $Q_1$, and diode $D_4$ to terminal 7 to turn on $Q_1$. This action inhibits the delivery of a gate-drive output signal at terminal 4. For negative voltages at terminal 5 that have magnitudes greater than 3 volts, the current flows through diode $D_5$, the emitter-to-base junction of transistor $Q_1$, diode $D_3$, and resistor $R_1$, and again turns on transistor $Q_1$. Transistor $Q_1$ is off only when the voltage at terminal 5 is less than the threshold voltage of approximately ±2 volts. When the integrated-circuit zero-voltage switch is connected as shown in Fig. 1, therefore, the output is a narrow pulse which is approximately centered about the zero-voltage time in the cycle, as shown in Fig. 3. In some applications, however,

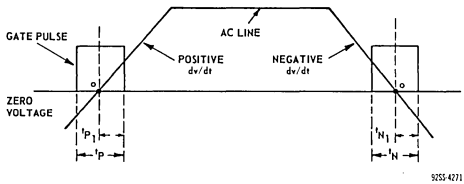



*Fig. 3 – Waveform showing output-pulse duration of the zero-voltage switch.*

particularly those that use either slightly inductive or low-power loads, the thyristor load current does not reach the latching-current value* by the end of this pulse. An external capacitor $C_X$ connected between terminal 5 and 7, as shown in Fig. 4, can be used to delay the pulse to accommodate such loads. The amount of pulse stretching and delay is shown in Figs. 5(a) and 5(b).

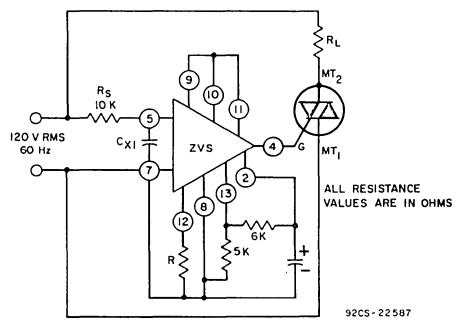



*Fig. 4 – Use of a capacitor between terminals 5 and 7 to delay the output pulse of the zero-voltage switch.*

Continuous gate current can be obtained if terminal 12 is connected to terminal 7 to disable the zero-crossing detector. In this mode, transistor $Q_1$ is always off. This mode of operation is useful when comparator operation is desired or when inductive loads must be switched. (If the capacitance in the load circuit is low, most RFI is eliminated.) Care must be taken to avoid overloading of the internal power supply in this mode. A sensitive-gate thyristor should be used, and a resistor should be placed between terminal 4 and the gate of the thyristor to limit the current, as pointed out later under **Special Application Considerations.**

Fig. 6 indicates the timing relationship between the line voltage and the zero-voltage- switch output pulses. At 60 Hz, the pulse is typically 100 microseconds wide; at 400 Hz, the pulse width is typically 12 microseconds. In the basic circuit shown, when the dc logic signal is "high", the output is disabled; when it is "low", the gate pulses are enabled.

* The latching current is the minimum current required to sustain conduction immediately after the thyristor is switched from the off to the on state and the gate signal is removed.

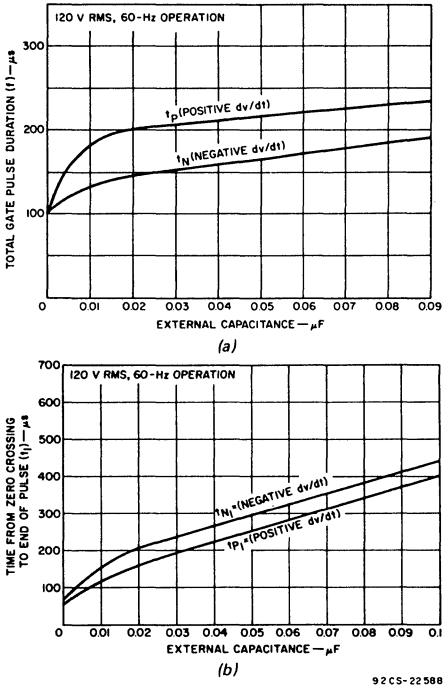



*Fig. 5 – Curves showing effect of external capacitance on (a) the total output-pulse duration, and (b) the time from zero crossing to the end of the pulse.*

### On-Off Sensing Amplifier

The discussion thus far has considered only cases in which pulses are present all the time or not at all. The differential sense amplifier consisting of transistors $Q_2$, $Q_3$, $Q_4$, and $Q_5$ (shown in Fig. 2) makes the zero-voltage switch a flexible power-control circuit. The transistor pairs $Q_2$-$Q_4$ and $Q_3$-$Q_5$ form a high-beta composite p-n-p transistors in which the emitters of transistors $Q_4$ and $Q_5$ act as the collectors of the composite devices. These two composite transistors are connected as a differential amplifier with resistor $R_3$ acting as a constant-current source. The relative current flow in the two "collectors" is a function of the difference in voltage between the bases of transistors $Q_2$ and $Q_3$. Therefore, when terminal 13 is more positive than terminal 9, little or no current flows in the "collector" of the transistor pair $Q_2$-$Q_4$. When terminal 13 is negative with respect to terminal 9, most of the current flows through that path, and none in terminal 8. When current flows in the transistor pair $Q_2$-$Q_4$, the path is from the supply through $R_3$, through the transistor pair $Q_2$-$Q_4$, through the base-emitter junction of transistor $Q_1$, and finally through the diode $D_4$ to terminal 7. Therefore, when $V_{13}$ is equal to or more negative than $V_9$, transistor $Q_1$ is on, and the output is inhibited.

In the circuit shown in Fig. 1, the voltage at terminal 9 is derived from the supply by connection of terminals 10 and 11 to form a precision voltage divider. This divider forms one side of a transducer bridge, and the potentiometer $R_p$ and the negative-temperature-coefficient (NTC) sensor form the other side. At low temperatures, the high resistance of the sensor causes terminal 13 to be positive with respect to terminal 9 so that the thyristor fires on every half-cycle, and power is applied to the load. As the temperature increases, the sensor resistance decreases until a balance is reached, and $V_{13}$ approaches $V_9$. At this point, the transistor pair $Q_2$-$Q_4$ turns on and inhibits any further pulses. The controlled temperature is adjusted by variation of the value of the potentiometer $R_p$. For cooling service, either the positions of $R_p$ and the sensor may be reversed or terminals 9 and 13 may be interchanged.

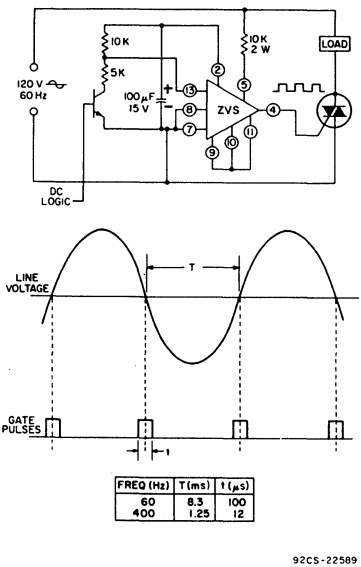



*Fig. 6 – Timing relationship between the output pulses of the RCA zero-voltage switch and the ac line voltage.*

The low bias current of the sensing amplifier permits operation with sensor impedances of up to 0.1 megohm at balance without introduction of substantial error (i.e., greater than 5 per cent). The error may be reduced if the internal bridge elements, resistors $R_4$ and $R_5$, are not used, but are replaced with resistances which equal the sensor impedance. The minimum value of sensor impedance is restricted by the current drain on the internal power supply. Operation of the zero-voltage switch with low-impedance sensors is discussed later under **Special Application Considerations**. The voltage applied to terminal 13 must be greater than 1.8 volts at all times to assure proper operation.

### Protection Circuit

A special feature of the CA3058 and CA3059 zero-voltage switches is the inclusion of an interlock type of circuit. This circuit removes power from the load by interrupting the thyristor gate drive if the sensor either shorts or opens. However, use of this circuit places certain constraints upon the user. Specifically, effective protection-circuit operation is dependent upon the following conditions:

(1) The circuit configuration of Fig. 1 is used, with an internal supply, no external load on the supply, and terminal 14 connected to terminal 13.

(2) The value of potentiometer $R_p$ and of the sensor resistance must be between 2000 ohms and 0.1 megohm.

(3) The ratio of sensor resistance and $R_p$ must be greater than 0.33 and less than 3.0 for all normal conditions. (If either of these ratios is not met with an unmodified sensor, a series resistor or a shunt resistor must be added to avoid undesired activation of the circuit.)

The protective feature may be applied to other systems when operation of the circuit is understood. The protection circuit consists of diodes $D_{12}$ and $D_{15}$ and transistor $Q_{10}$. Diode $D_{12}$ activates the protection circuit if the sensor shown in Fig. 1 shorts or its resistance drops too low in value, as follows: Transistor $Q_6$ is on during an output pulse so that the junction of diodes $D_8$ and $D_{12}$ is 3 diode drops (approximately 2 volts) above terminal 7. As long as $V_{14}$ is more positive or only 0.15 volt negative with respect to that point, diode $D_{12}$ does not conduct, and the circuit operates normally. If the voltage at terminal 14 drops to 1 volt, the anode of diode $D_8$ can have a potential of only 1.6 to 1.7 volts, and current does not flow through diodes $D_8$ and $D_9$ and transistor $Q_6$. The thyristor then turns off.

The actual threshold is approximately 1.2 volts at room temperature, but decreases 4 millivolts per degree C at higher temperatures. As the sensor resistance increases, the voltage at terminal 14 rises toward the supply voltage. At a voltage of approximately 6 volts, the zener diode $D_{15}$ breaks down and turns on transistor $Q_{10}$, which then turns off transistor $Q_6$ and the thyristor. If the supply voltage is not at least 0.2 volt more positive than the breakdown voltage of diode $D_{15}$, activation of the protection circuit is not possible. For this reason, loading the internal supply may cause this circuit to malfunction, as may selection of the wrong external supply voltage. Fig. 7 shows a guide for the proper operation of the protection circuit when an external supply is used with a typical integrated-circuit zero-voltage switch.

## SPECIAL APPLICATION CONSIDERATIONS

As pointed out previously, the RCA integrated-circuit zero-voltage switches (CA3058, CA3059, and CA3079) are exceptionally versatile units that can be adapted for use in a wide-variety of power-control applications. Full advantage of this versatility can be realized, however, only if the user has a basic understanding of several fundamental considerations that apply to certain types of applications of the zero-voltage switches.

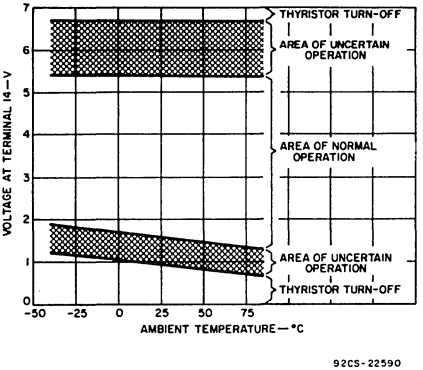



*Fig. 7 – Operating regions for built-in protection circuits of a typical zero-voltage switch.*

### Operating-Power Options

Power to the zero-voltage switch may be derived directly from the ac line, as shown in Fig. 1, or from an external dc power supply connected between terminals 2 and 7, as shown in Fig. 8. When the zero-voltage switch is operated directly from the ac line, a dropping resistor $R_S$ of 5,000 to 10,000 ohms must be connected in series with terminal 5 to limit the current in the switch circuit. The optimum value for this resistor is a function of the average current drawn from the internal dc power supply, either by external circuit elements or by the thyristor trigger circuits, as shown in Fig. 9. The chart shown in Fig. 1 indicates the value and dissipation rating of the resistor $R_S$ for ac line voltages of 24, 120, 208 to 230, and 277 volts.

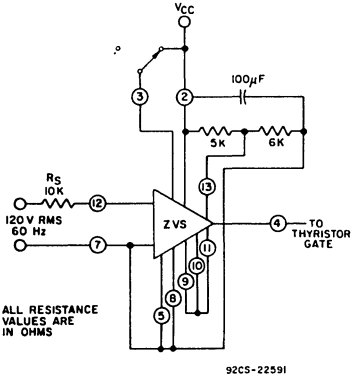



*Fig. 8 – Operation of the zero-voltage switch from an external dc power supply connected between terminals 2 and 7.*

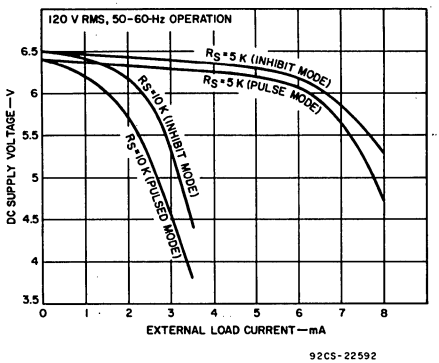



*Fig. 9 – DC supply voltage as a function of external load current for several values of dropping resistance $R_S$.*

### Half-Cycling Effect

The method by which the zero-voltage switch senses the zero crossing of the ac power results in a half-cycling phenomenon at the control point. Fig. 10 illustrates this phenomenon. The zero-voltage switch senses the zero-voltage crossing every half-cycle, and an output, for example pulse No. 4, is produced to indicate the zero crossing. During the remaining 8.3 milliseconds, however, the differential amplifier in the zero-voltage switch may change state and inhibit any further output pulses. The uncertainity region of the differential amplifier, therefore, prevents pulse No. 5 from triggering the triac during the negative excursion of the ac line voltage.

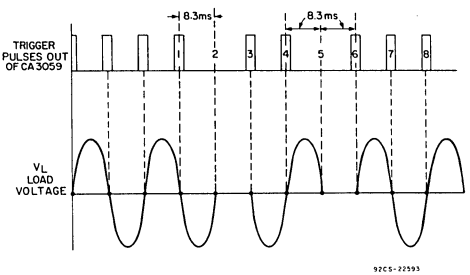



*Fig. 10 – Half-cycling phenomenon in the zero-voltage switch.*

When a sensor with low sensitivity is used in the circuit, the zero-voltage switch is very likely to operate in the linear mode. In this mode, the output trigger current may be sufficient to trigger the triac on the positive-going cycle, but insufficient to trigger the device on the negative-going cycle of the triac supply voltage. This effect introduces a half-cycling phenomenon, i.e., the triac is turned on during the positive half-cycle and turned off during the negative half-cycle.

Several techniques may be used to cope with the half-cycling phenomenon. If the user can tolerate some hystersis in the control, then positive feedback can be added around the differential amplifier. Fig. 11 illustrates this technique. The tabular data in the figure lists the recommended values of resistors $R_1$ and $R_2$ for different sensor impedances at the control point.

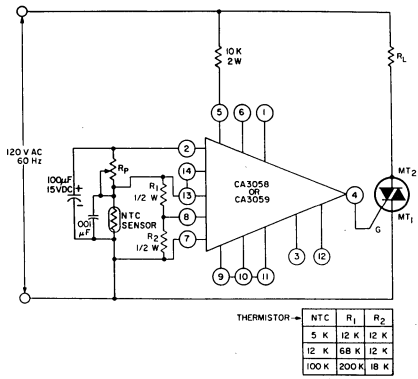



*Fig. 11 – CA3058 or CA3059 on-off controller with hysteresis.*

If a significant amount (greater than ±10%) of controlled hysteresis is required, then the circuit shown in Fig. 12 may be employed. In this configuration, external transistor $Q_1$ can be used to provide an auxiliary timed-delay function.

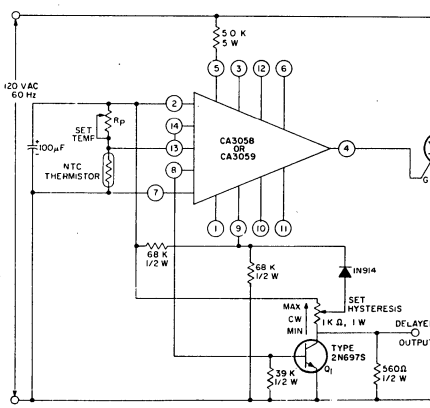



*Fig. 12 – CA3058 or CA3059 on-off controller with controlled hysteresis.*

For applications that require complete elimination of half-cycling without the addition of hysteresis, the circuit shown in Fig. 13 may be employed. This circuit uses a

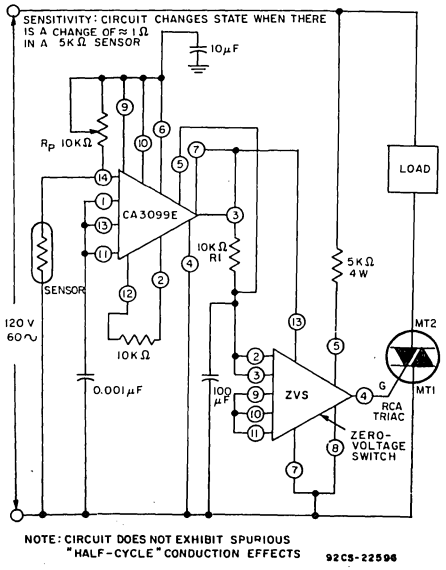



*Fig. 13 – Sensitive temperature control.*

CA3099E integrated-circuit programmable comparator with a zero-voltage switch. A block diagram of CA3099E is shown in Fig. 14. Because the CA3099E contains an integral flip-flop, its output will be in either a "0" or "1" state. Consequently the zero-voltage switch cannot operate in the linear mode, and spurious half-cycling operation is prevented. When the signal-input voltage at terminal 14 of the CA3099E is equal to or less than the "low" reference voltage (LR), current flows from the power supply through resistor $R_1$, and a logic "0" is applied to terminal 13 of the zero-voltage switch. This condition turns off the triac. The triac remains off until the signal-input voltage rises to or exceeds the "high" reference voltage (HR), thereby effecting a change in the state of the flip-flop so that a logic "1" is applied to terminal 13 of the zero-voltage switch, and triggers the triac on.

### "Proporational Control" Systems

The on-off nature of the control shown in Fig. 1 causes some overshoot that leads to a definite steady-state error. The addition of hysteresis adds further to this error factor. However, the connections shown in Fig. 15(a) can be used to add proportional control to the system. In this circuit, the sense amplifier is connected as a free-running multivibrator. At balance, the voltage at terminal 13 is much less than the voltage at terminal 9. The output will be inhibited at all times until the voltage at terminal 13 rises to the design differential voltage between terminals 13 and 9; then proportional control resumes. The voltage at terminal 13 is as shown in Fig. 15(b). When this voltage is more positive than the threshold, power is

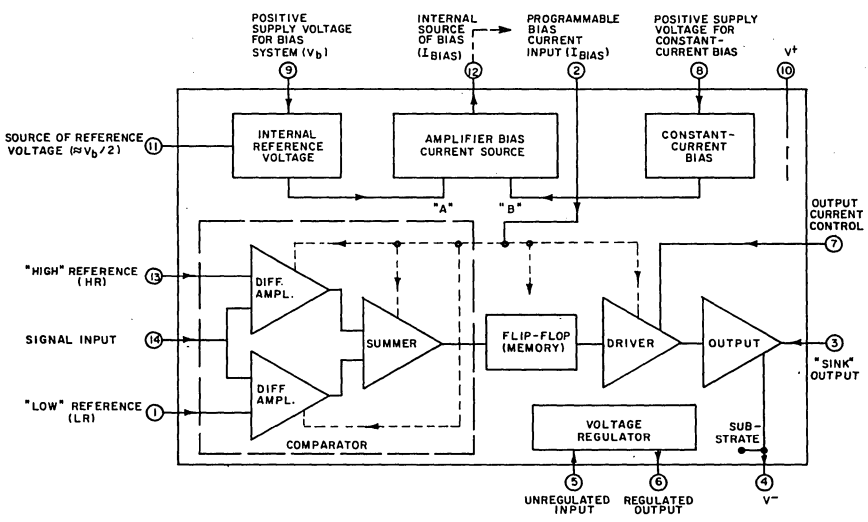



*Fig. 14 – Block diagram of CA3099E integrated-circuit programmable comparator.*

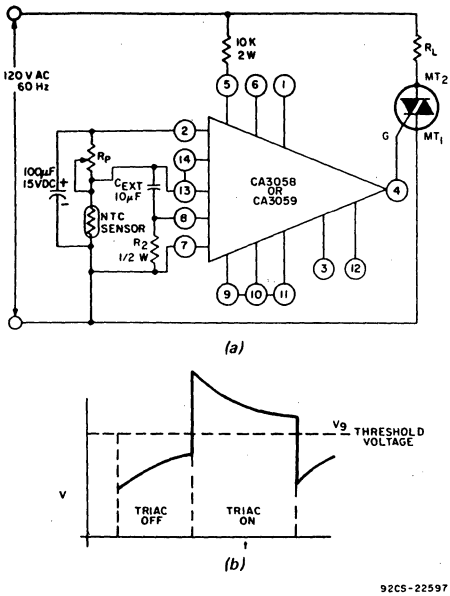



*Fig. 15 – Use of the CA3058 or CA3059 in a typical heating control with proportional control: (a) schematic diagram, and (b) waveform of voltage at terminal 13.*

applied to the load so that the duty cycle is approximately 50 per cent. With a 0.1 megohm sensor and values of $R_p$ = 0.1 megohm, $R_2$ = 10,000 ohms, and $C_{EXT}$ = 10 microfarads, a period greater than 3 seconds is achieved. This period should be much shorter than the thermal time constant of the system. A change in the value of any of these elements changes the period, as shown in Fig. 16. As the resistance of the sensor changes, the voltage on terminal 13 moves relative to $V_9$. A cooling sensor moves $V_{13}$ in a positive direction. The triac is on for a larger portion of the pulse cycle and increases the average power to the load.

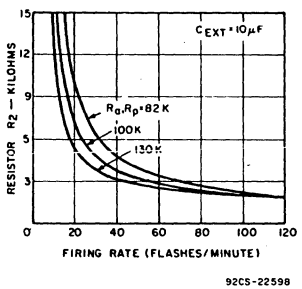



*Fig. 16 – Effect of variations in time-constant elements on period.*

As in the case of the hysteresis circuitry described earlier, some special applications may require more sophisticated systems to achieve either very precise regions of control or very long periods.

Zero-voltage switching control can be extended to applications in which it is desirable to have constant control of the temperature and a minimization of system hysteresis. A closed-loop top-burner control in which the temperature of the cooking utensil is sensed and maintained at a particular value is a good example of such an application; the circuit for this control is shown in Fig. 17. In this circuit, a unijunction

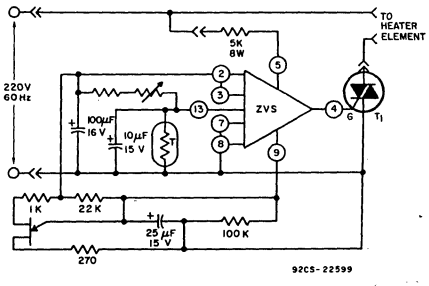



*Fig. 17 – Schematic diagram of proportional zero-voltage-switching control.*

oscillator is outboarded from the basic control by means of the internal power supply of the zero-voltage switch. The output of this ramp generator is applied to terminal 9 of the zero-voltage switch and establishes a varied reference to the differential amplifier. Therefore, gate pulses are applied to the triac whenever the voltage at terminal 13 is greater than the voltage at terminal 9. A varying duty cycle is established in which the load is predominantly on with a cold sensor and predominantly off with a hot sensor. For precise temperature regulation, the time base of the ramp should be shorter than the thermal time constant of the system but longer than the period of the 60-Hz line. Fig. 18, which contains various waveforms for the system of Fig. 17, indicates that a typical variance of ±0.5°C might be expected at the sensor contact to the utensil. Overshoot of the set temperature is minimized with this approach, and scorching of any type is minimized.

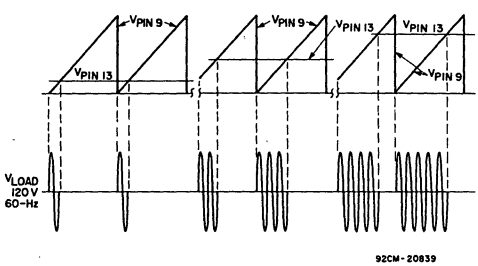



*Fig. 18 – Waveforms for the circuit of Fig. 17.*

**Effect of Thyristor Load Characteristics**

The zero-voltage switch is designed primarily to gate a thyristor that switches a resistive load. Because the output pulse supplied by the switch is of short duration, the latching current of the triac becomes a significant factor in determining whether other types of loads can be switched. (The latching-current value determines whether the triac will remain in conduction after the gate pulse is removed.) Provisions are included in the zero-voltage switch to accommodate inductive loads and low-power loads. For example, for loads that are less than approximately 4 amperes rms or that are slightly inductive, it is possible to retard the output pulse with respect to the zero-voltage crossing by insertion of the capacitor $C_X$ from terminal 5 to terminal 7. The insertion of capacitor $C_X$ permits switching of triac loads that have a slight inductive component and that are greater than approximately 200 watts (for operation from an ac line voltage of 120 volts rms). However, for loads less than 200 watts (for example, 70 watts), it is recommended that the user employ the T2300B* sensitive-gate triac with the zero-voltage switch because of the low latching-current requirement of this triac.

For loads that have a low power factor, such as a solenoid valve, the user may operate the zero-voltage switch in the dc mode. In this mode, terminal 12 is connected to terminal 7, and the zero-crossing detector is inhibited. Whether a "high" or "low" voltage is produced at terminal 4 is then dependent only upon the state of the differential comparator within the integrated-circuit zero-voltage switch, and not upon the zero crossing of the incoming line voltage. Of course, in this mode of operation, the zero-voltage switch no longer operates as a zero-voltage switch. However, for many applications that involve the switching of low-current inductive loads, the amount of RFI generated can frequently be tolerated.

For switching of high-current inductive loads, which must be turned on at zero line current, the triggering technique employed in the dual-output over-under temperature controller and the transient-free switch controller described subsequently in this Note is recommended.

**Switching of Inductive Loads**

For proper driving of a thyristor in full-cycle operation, gate drive must be applied soon after the voltage across the device reverses. When resistive loads are used, this reversal occurs as the line voltage reverses. With loads of other power factors, however, it occurs as the current through the load becomes zero and reverses.

There are several methods for switching an inductive load at the proper time. If the power factor of the load is high (i.e., if the load is only slightly inductive), the pulse may be delayed by addition of a suitable capacitor between terminals 5 and 7, as described previously. For highly inductive loads, however, this method is not suitable, and different techniques must be used.

If gate current is continuous, the triac automatically commutates because drive is always present when the voltage reverses. This mode is established by connection of terminals 7 and 12. The zero-crossing detector is then disabled so that current is supplied to the triac gate whenever called for by the sensing amplifier. Although the RFI-eliminating function of the zero-voltage switch is inhibited when the zero-crossing detector is disabled, there is no problem if the load is highly inductive because the current in the load cannot change abruptly.

Circuits that use a sensitive-gate triac to shift the firing point of the power triac by approximately 90 degrees have been designed. If the primary load is inductive, this phase shift corresponds to firing at zero current in the load. However, changes in the power factor of the load or tolerances of components will cause errors in this firing time.

The circuit shown in Fig. 19 uses a CA3086 integrated-circuit transistor array to detect the absence of load current by sensing the voltage across the triac. The internal zero-crossing detector is disabled by connection of terminal 12 to terminal 7, and control of the output is made through the external inhibit input, terminal 1. The circuit permits an output only when the voltage at point A exceeds two $V_{BE}$ drops, or 1.3 volts. When A is positive, transistors $Q_3$ and $Q_4$ conduct and reduce the voltage at terminal 1 below the inhibit state. When A is negative, transistors $Q_1$ and $Q_2$ conduct. When the voltage at point A is less than ±1.3 volts, neither of the transistor pairs conducts; terminal 1 is then pulled positive by the current in resistor $R_3$, and the output in inhibited.

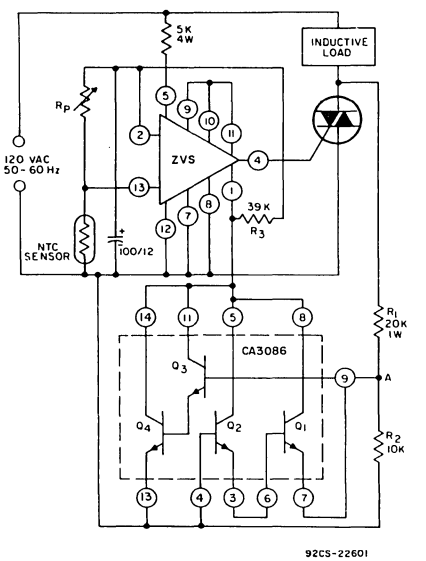



*Fig. 19 – Use of the CA3058 or CA3059 together with CA3086 for switching inductive loads.*

The circuit shown in Fig. 19 forms a pulse of gate current and can supply high peak drive to power traics with low average current drain on the internal supply. The gate pulse will always last just long enough to latch the thyristor so that

* Formerly RCA 40526

there is no problem with delaying the pulse to an optimum time. As in other circuits of this type, RFI results if the load is not suitably inductive because the zero-crossing detector is disabled and initial turn-on occurs at random.

The gate pulse forms because the voltage at point A when the thyristor is on is less than 1.3 volts: therefore, the output of the zero-voltage switch is inhibited, as described above. The resistor divider $R_1$ and $R_2$ should be selected to assure this condition. When the triac is on, the voltage at point A is approximately one-third of the instantaneous on-state voltage ($v_T$) of the thyristor. For most RCA thyristors, $v_T$ (max) is less than 2 volts, and the divider shown is a conservative one. When the load current passes through zero, the triac commutates and turns off. Because the circuit is still being driven by the line voltage, the current in the load attempts to reverse, and voltage increases rapidly across the "turned-off" triac. When this voltage exceeds 4 volts, one portion of the CA3086 conducts and removes the inhibit signal to permit application of gate drive. Turning the triac on causes the voltage across it to drop and thus ends the gate pulse. If the latching current has not been attained, another gate pulse forms, but no discontinuity in the load current occurs.

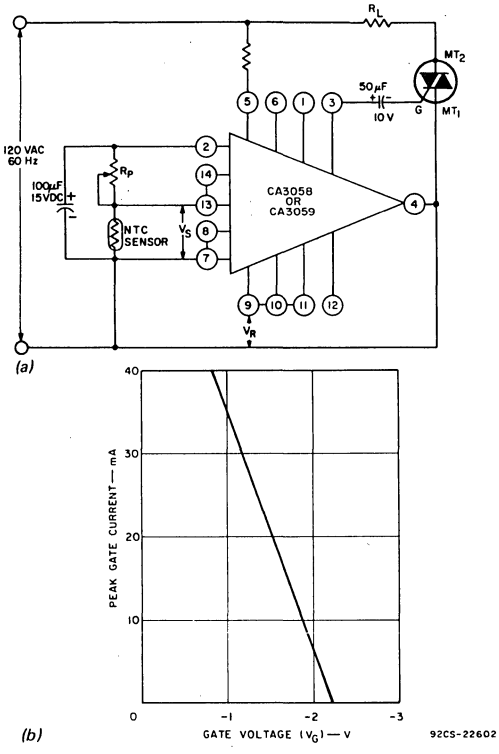



*Fig. 20 – Use of the CA3058 or CA3059 to provide negative gate pulses: (a) schematic diagram; (b) peak gate current (at terminal 3) as a function of gate voltage.*

### Provision of Negative Gate Current

Triacs trigger with optimum sensitivity when the polarity of the gate voltage and the voltage at the main terminal 2 are similar ($I^+$ and $II^-$ modes). Sensitivity is degraded when the polarities are opposite ($I^-$ and $III^+$ modes). Although RCA triacs are designed and specified to have the same sensitivity in both $I^-$ and $III^+$ modes, some other types have very poor sensitivity in the $III^+$ condition. Because the zero-voltage switch supplies positive gate pulses, it may not directly drive some higher-current triacs of these other types.

The circuit shown in Fig. 20(a) uses the negative-going voltage at terminal 3 of the zero-voltage switch to supply a negative gate pulse through a capacitor. The curve in Fig. 20(b) shows the approximate peak gate current as a function of gate voltage $V_G$. Pulse width is approximately 80 microseconds.

### Operation with Low-Impedance Sensors

Although the zero-voltage switch can operate satisfactorily with a wide range of sensors, sensitivity is reduced when sensors with impedances greater than 20,000 ohms are used. Typical sensitivity is one per cent for a 5000-ohm sensor and increases to three per cent for a 0.1-megohm sensor.

Low-impedance sensors present a different problem. The sensor bridge is connected across the internal power supply and causes a current drain. A 5000-ohm sensor with its associated 5000-ohm series resistor draws less than 1 milliampere. On the other hand, a 300-ohm sensor draws a current of 8 to 10 milliampers from the power supply.

Fig. 21 shows the 600-ohm load line of a 300-ohm sensor on a redrawn power-supply regulation curve for the zero-voltage switch. When a 10,000-ohm series resistor is used, the voltage across the circuit is less than 3 volts and both sensitivity and output current are significantly reduced. When a 5000-ohm series resistor is used, the supply voltage is nearly 5 volts, and operation is approximately normal. For more consistent operation, however, a 4000-ohm series resistor is recommended.

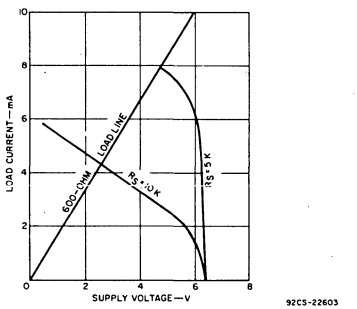



*Fig. 21 – Power-supply regulation of the CA3058 or CA3059 with a 300-ohm sensor (600-ohm load) for two values of series resistor.*

Although positive-temperature-coefficient (PTC) sensors rated at 5 kilohms are available, the existing sensors in ovens are usually of a much lower value. The circuit shown in Fig. 22 is offered to accommodate these inexpensive metal-wound

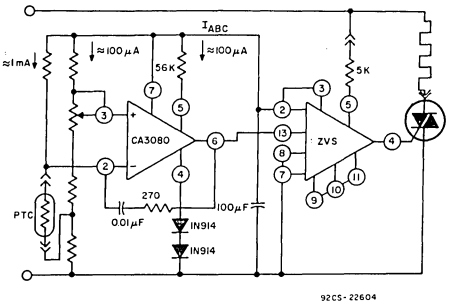



*Fig. 22 – Schematic diagram of circuit for use with low-resistance sensor.*

sensors. A schematic diagram of the RCA CA3080 integrated-circuit operational transconductance amplifier used in Fig. 22, is shown in Fig. 23. With an amplifier bias current, $I_{ABC}$, of 100 microamperes, a forward transconductance of 2 milliohms is achieved in this configuration. The CA3080 switches when the voltage at terminal 2 exceeds the voltage at terminal 3. This action allows the sink current, $I_S$, to flow from terminal 13 of the zero-voltage switch (the input impedance to terminal 13 of the zero-voltage switch is approximately 50 kilohms); gate pulses are no longer applied to the triac because $Q_2$ of the zero-voltage switch is on. Hence, if the PTC sensor is cold, i.e., in the low resistance state, the load is energized. When the temperature of the PTC sensor increases to the desired temperature, the sensor enters the high resistance state, the voltage on terminal 2 becomes greater than that on terminal 3, and the triac switches the load off.

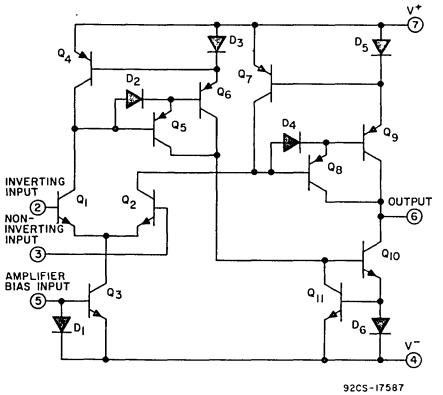



*Fig. 23 – Schematic diagram of the CA3080.*

Further cycling depends on the voltage across the sensor. Hence, very low values of sensor and potentiometer resistance can be used in conjunction with the zero-voltage switch power supply without causing adverse loading effects and impairing system performance.

### Interfacing Techniques

Fig. 24 shows a system diagram that illustrates the role of the zero-voltage switch and thyristor as an interface between the logic circuitry and the load. There are several basic

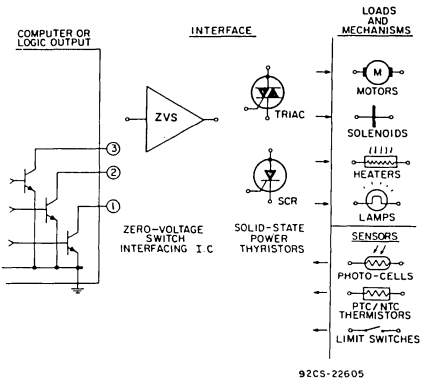



*Fig. 24 – The zero-voltage switch and thyristor as an interface.*

interfacing techniques. Fig. 25(a) shows the **direct input** technique. When the logic output transistor is switched from the on state (saturated) to the off state, the load will be turned on at the next zero-voltage crossing by means of the interfacing zero-voltage switch and the triac. When the logic output transistor is switched back to the on state, zero-crossing pulses from the zero-voltage switch to the triac

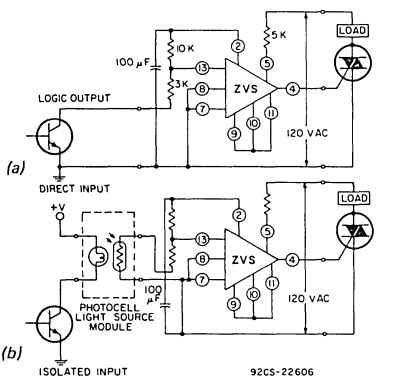



*Fig. 25 – Basic interfacing techniques: (a) direct input; (b) isolated input.*

gate will immediately cease. Therefore, the load will be turned off when the triac commutates off as the sine-wave load current goes through zero. In this manner, both the turn-on and turn-off conditions for the load are controlled.

When electrical isolation between the logic circuit and the load is necessary, the **isolated-input** technique shown in Fig. 25(b) is used. In the technique shown, optical coupling is used to achieve the necessary isolation. The logic output transistor switches the light-source portion of the isolator. The light-sensor portion changes from a high impedance to a low impedance when the logic output transistor is switched from off to on. The light sensor is connected to the differential amplifier input of the zero-voltage switch, which senses the change of impedance at a threshold level and switches the load on as in Fig. 25(a).

### Sensor Isolation

In many applications, electrical isolation of the sensor from the ac input line is desirable. Two common isolation techniques are shown in Fig. 26.

**Transformer Isolation** – In Fig. 26(a), a pulse transformer is used to provide electrical isolation of the sensor from incoming ac power lines. The pulse transformer $T_1$ isolates the

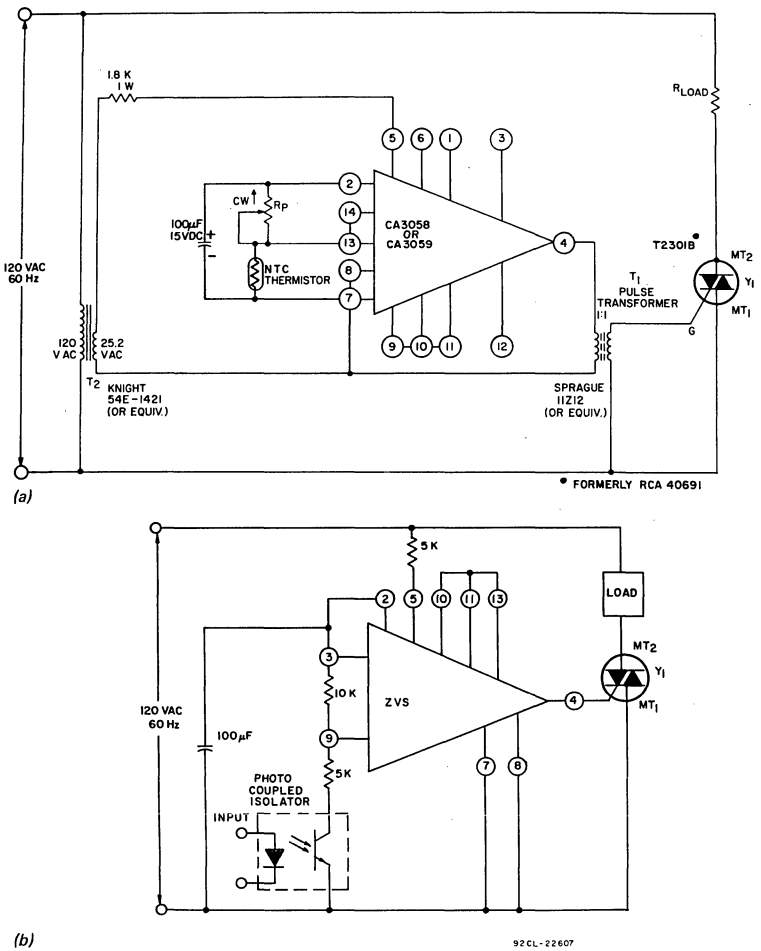



*Fig. 26 – Zero-voltage switch (a) on-off controller with an isolated sensor, (b) on-off controller with photocoupler.*

sensor from terminal No. 1 of the triac $Y_1$, and transformer $T_2$ isolates the CA3058 or CA3059 from the power lines. Capacitor $C_1$ shifts the phase of the output pulse at terminal No. 4 in order to retard the gate pulse delivered to triac $Y_1$ to compensate for the small phase-shift introduced by transformer $T_1$.

**Photocoupler Isolation** – In Fig. 26(b), a photocoupler provides electrical isolation of the sensor logic from the incoming ac power lines. When a logic "1" is applied at the input of the photocoupler, the triac controlling the load will be turned on whenever the line voltage passes through zero. When a logic "0" is applied to the photocoupler, the triac will turn off and remain off until a logic "1" appears at the input of the photocoupler.

## TEMPERATURE CONTROLLERS

Fig. 27 shows a triac used in an on-off temperature-controller configuration. The triac is turned on at zero voltage whenever the voltage $V_s$ exceeds the reference

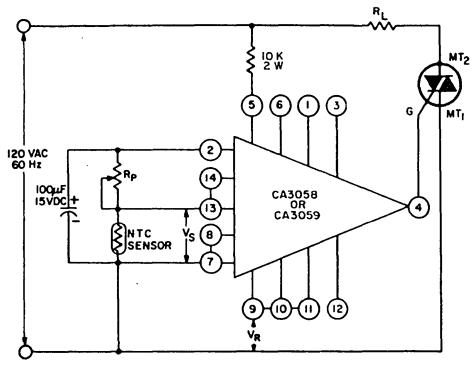



*Fig. 27 – CA3058 or CA3059 on-off temperature controller.*

voltage $V_r$. The transfer characteristic of this system, shown in Fig. 28(a), indicates significant thermal overshoots and undershoots, a well-known characteristic of such a system. The differential or hysteresis of this system, however, can be further increased, if desired, by the addition of positive feedback.

For precise temperature-control applications, the proportional-control technique with synchronous switching is employed. The transfer curve for this type of controller is shown in Fig. 28(b). In this case, the duty cycle of the power supplied to the load is varied with the demand for heat required and the thermal time constant (inertia) of the system. For example, when the temperature setting is increased in an on-off type of controller, full power (100 per cent duty cycle) is supplied to the system. This effect results in significant temperature excursions because there is no anticipatory circuit to reduce the power gradually before the actual set temperature is achieved. However, in a proportional control technique, less power is supplied to the load (reduced duty cycle) as the error signal is reduced (sensed temperature approaches the set temperature).

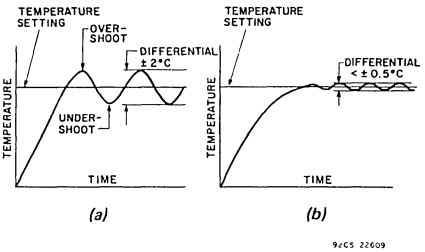



*Fig. 28 – Transfer characteristics of (a) on-off and (b) proportional control systems.*

Before such a system is implemented, a time base is chosen so that the on-time of the triac is varied within this time base. The ratio of the on-to-off time of the triac within this time interval depends on the thermal time constant of the system and the selected temperature setting. Fig. 29 illustrates the principle of proportional control. For this operation, power is supplied to the load until the ramp voltage reaches a value greater than the dc control signal supplied to the opposite side of the differential amplifier. The triac then remains off for the remainder of the time-base period. As a result, power is "proportioned" to the load in a direct relation to the heat demanded by the system.

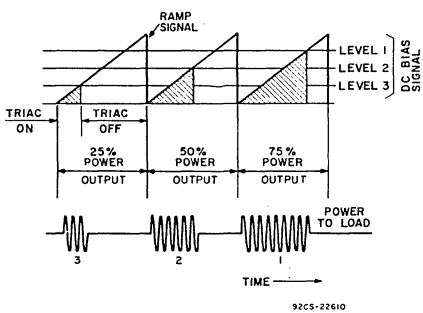



*Fig. 29 – Principles of proportional control.*

For this application, a simple ramp generator can be realized with a minimum number of active and passive components. A ramp having good linearity is not required for proportional operation because of the nonlinearity of the thermal system and the closed-loop type of control. In the circuit shown in Fig. 30, the ramp voltage is generated when the capacitor $C_1$ charges through resistors $R_0$ and $R_1$. The time base of the ramp is determined by resistors $R_2$ and $R_3$, capacitor $C_2$, and the breakover voltage of the D3202U* diac.

* Formerly RCA 45412

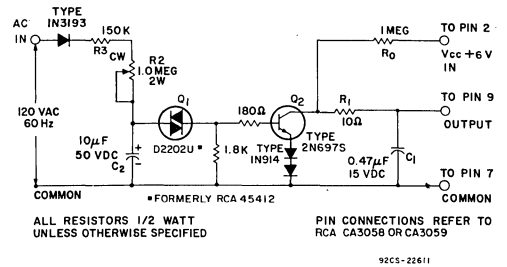



*Fig. 30 – Ramp generator.*

When the voltage across $C_2$ reaches approximately 32 volts, the diac switches and turns on the 2N697S transistor and 1N914 diodes. The capacitor $C_1$ then discharges through the collector-to-emitter junction of the transistor. This discharge time is the retrace or flyback time of the ramp. The circuit shown can generate ramp times ranging from 0.3 to 2.0 seconds through adjustment of $R_2$. For precise temperature regulation, the time base of the ramp should be shorter than the thermal time constant of the system, but long with respect to the period of the 60-Hz line voltage. Fig. 31 shows a triac connected for the proportional mode.

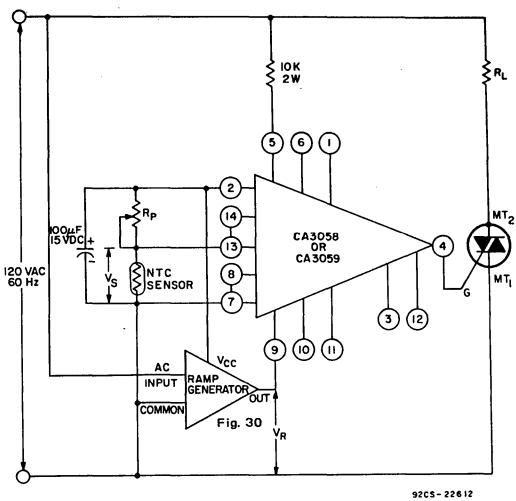



*Fig. 31 – CA3058 or CA3059 proportional temperature controller.*

Fig. 32(a) shows a dual-output temperature controller that drives two triacs. When the voltage $V_S$ developed across the temperature-sensing network exceeds the reference voltage $V_{R1}$, motor No. 1 turns on. When the voltage across the network drops below the reference voltage $V_{R2}$, motor No. 2 turns on. Because the motors are inductive, the currents $I_{M1}$ lag the incoming line voltage. The motors, however, are switched by the triacs at zero current, as shown in Fig. 32(b).

The problem of driving inductive loads such as these motors by the narrow pulses generated by the zero-voltage switch is solved by use of the sensitive-gate RCA-40526 triac. The high sensitivity of this device (3 milliamperes maximum) and low latching current (approximately 9 milliamperes) permit synchronous operation of the temperature-controller circuit. In Fig. 32(a), it is apparent that, though the gate pulse $V_g$ of triac $Y_1$ has elapsed, triac $Y_2$ is switched on by the current through $R_{L1}$. The low latching current of the RCA-40526 triac results in dissipation of only 2 watts in $R_{L1}$, as opposed to 10 to 20 watts when devices that have high latching currents are used.

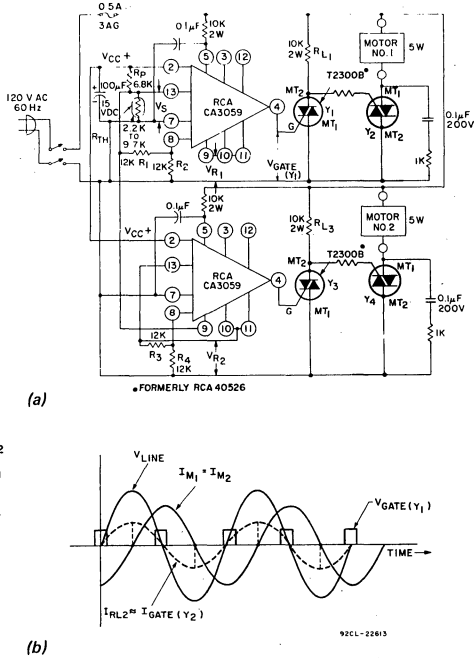



*Fig. 32 – Dual output, over-under temperature controller (a) circuit, (b) voltage and current waveforms.*

### Electric-Heat Application

For electric-heating applications, the RCA-2N5444 40-ampere triac and the zero-voltage switch constitute an optimum pair. Such a combination provides synchronous switching and effectively replaces the heavy-duty contactors which easily degrade as a result of pitting and wearout from the switching transients. The salient features of the 2N5444 40-ampere triac are as follows:

(1) 300-ampere single-surge capability (for operation at 60-Hz),

(2) a typical gate sensitivity of 20 milliamperes in the $I(^+)$ and $III(^+)$ modes,

(3) low on-state voltage of 1.5 volts maximum at 40 amperes, and

(4) available $V_{DROM}$ equal to 600 volts.

Fig. 33 shows the circuit diagram of a synchronous-switching heat-staging controller that is used for electric heating systems. Loads as heavy as 5 kilowatts are switched sequentially at zero voltage to eliminate RFI and prevent a dip in line voltage that would occur if the full 25 kilowatts were to be switched simultaneously.

$Q_1$ and $Q_4$ are used as a constant-current source to charge capacitor C in a linear manner. Transistor $Q_2$ acts as a buffer stage. When the thermostat is closed, a ramp voltage is provided at output $E_o$. At approximately 3-second intervals, each 5-kilowatt heating element is switched onto the power system by its respective triac. When there is no further demand for heat, the thermostat opens, and capacitor C discharges through $R_1$ and $R_2$ to cause each triac to turn off in the reverse heating sequence. It should be noted that some half-cycling occurs before the heating element is switched fully on. This condition can be attributed to the inherent dissymmetry of the triac and is further aggravated by the slow-rising ramp voltage applied to one of the inputs. The timing diagram in Fig. 34 shows the turn-on and turn-off sequence of the heating system being controlled.

Seemingly, the basic method shown in Fig. 33 could be modified to provide proportional control in which the number of heating elements switched into the system, under any given

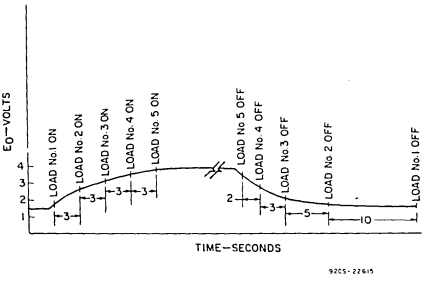



*Fig. 34 – Ramp-voltage waveform for the heat-staging controller.*

thermal load, would be a function of the BTU's required by the system or the temperature differential between an indoor and outdoor sensor within the total system environment. That is, the closing of the thermostat would not switch in all the heating elements within a short time interval, which inevitably results in undesired temperature excursions, but would switch in only the number of heating elements required to satisfy the actual heat load.

### Oven/Broiler Control

Zero-voltage switching is demonstrated in the oven control circuit shown in Fig. 35. In this circuit, a sensor element is included in the oven to provide a closed-loop system for accurate control of the oven temperature.

As shown in Fig. 35, the temperature of the oven can be adjusted by means of potentiometer $R_1$, which acts, together with the sensor, as a voltage divider at terminal 13. The voltage

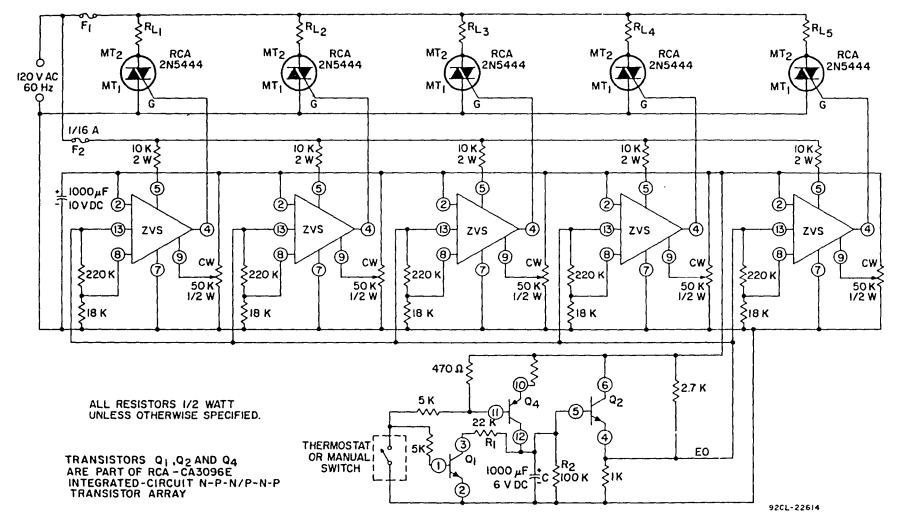



*Fig. 33 – Synchronous-switching heat-staging controller using a series of zero-voltage switches.*

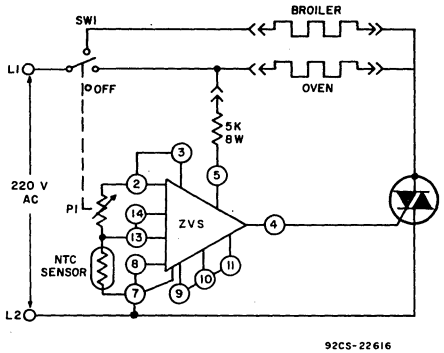



*Fig. 35 – Schematic diagram of basic oven control.*

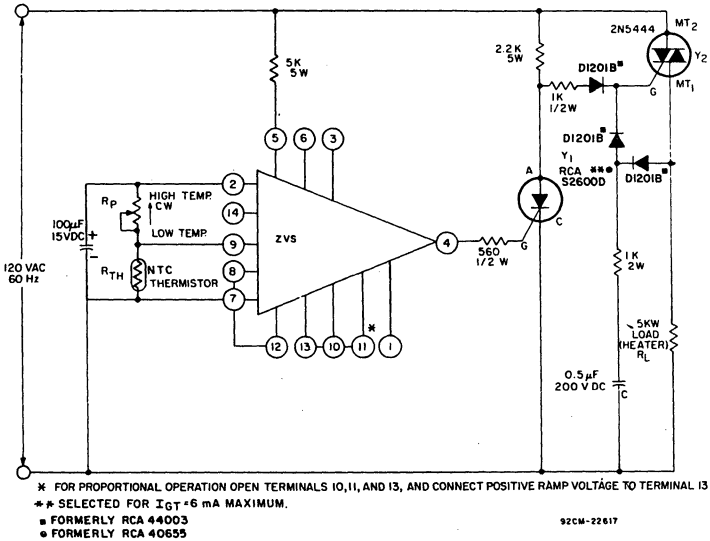
at terminal 13 is compared to the fixed bias at terminal 9 which is set by internal resistors $R_4$ and $R_5$. When the oven is cold and the resistance of the sensor is high, transistors $Q_2$ and $Q_4$ are off, a pulse of gate current is applied to the triac, and heat is applied to the oven. Conversely, as the desired temperature is reached, the bias at terminal 13 turns the triac off. The closed-loop feature then cycles the oven element on and off to maintain the desired temperature to approximately ±2°C of the set value. Also, as has been noted, external resistors between terminals 13 and 8, and 7 and 8, can be used to vary this temperature and provide hysteresis. In Fig. 11, a circuit that provides approximately 10-per-cent hysteresis is demonstrated.

In addition to allowing the selection of a hysteresis value, the flexibility of the control circuit permits incorporation of other features. A PTC sensor is readily used by interchanging terminals 9 and 13 of the circuit shown in Fig. 35 and substituting the PTC for the NTC sensor. In both cases, the sensor element is directly returned to the system ground or common, as is often desired. Terminal 9 can be connected by external resistors to provide for a variety of biasing, e.g., to match a lower-resistance sensor for which the switching-point voltage has been reduced to maintain the same sensor current.

To accommodate the self-cleaning feature, external switching, which enables both broiler and oven units to be paralleled, can easily be incorporated in the design. Of course, the potentiometer must be capable of a setting such that the sensor, which must be characterized for the high, self-clean temperature, can monitor and establish control of the high-temperature, self-clean mode. The ease with which this self-clean mode can be added makes the over-all solid-state systems cost-competitive with electromechanical systems of comparable capability. In addition, the system incorporates solid-state reliability while being neater, more easily calibrated, and containing less-costly system wiring.

**Integral-Cycle Temperature Controller (No half-cycling)**

If a temperature controller which is completely devoid of half-cycling and hysteresis is required, then the circuit shown in Fig. 36 may be used. This type of circuit is essential for applications in which half-cycling and the resultant dc component could cause overheating of a power transformer on the utility lines.




* FOR PROPORTIONAL OPERATION OPEN TERMINALS 10, 11, AND 13, AND CONNECT POSITIVE RAMP VOLTAGE TO TERMINAL 13
** SELECTED FOR $I_{GT}$ ≤6 mA MAXIMUM.
■ FORMERLY RCA 44003
● FORMERLY RCA 40655

*Fig. 36 – Integral-cycle temperature controller in which half-cycling effect is eliminated.*

In the integral-cycle controller, when the temperature being controlled is low, the resistance of the thermistor is high, and an output signal at terminal 4 of zero volts is obtained. The SCR ($Y_1$), therefore, is turned off. The triac ($Y_2$) is then triggered directly from the line on positive cycles of the ac voltage. When $Y_2$ is triggered and supplies power to the load $R_L$, capacitor C is charged to the peak of the input voltage. When the ac line swings negative, capacitor C discharges through the triac gate to trigger the triac on the negative half-cycle. The diode-resistor-capacitor "slaving network" triggers the triac on negative half-cycle to provide only **integral cycles** of ac power to the load.

When the temperature being controlled reaches the desired value, as determined by the thermistor, then a positive voltage level appears at terminal 4 of the zero-voltage switch. The SCR then starts to conduct at the beginning of the positive input cycle to shunt the trigger current away from the gate of the triac. The triac is then turned off. The cycle repeats when the SCR is again turned OFF by the zero-voltage switch.

The circuit shown in Fig. 37 is similar to the configuration in Fig. 36 except that the protection circuit incorporated in the zero-voltage switch can be used. In this new circuit, the NTC sensor is connected between terminals 7 and 13, and transistor $Q_o$ inverts the signal output at terminal 4 to nullify the phase reversal introduced by the SCR ($Y_1$). The internal power supply of the zero-voltage switch supplies bias current to transistor $Q_o$.

Of course, the circuit shown in Fig. 37 can readily be converted to a **true proportional integral-cycle temperature controller** simply by connection of a positive-going ramp voltage to terminal 9 (with terminals 10 and 11 open), as previously discussed in this Note.

### Thermocouple Temperature Control

Fig. 38 shows the CA3080A operating as a pre-amplifier for the zero-voltage switch to form a zero-voltage switching circuit for use with thermocouple sensors.

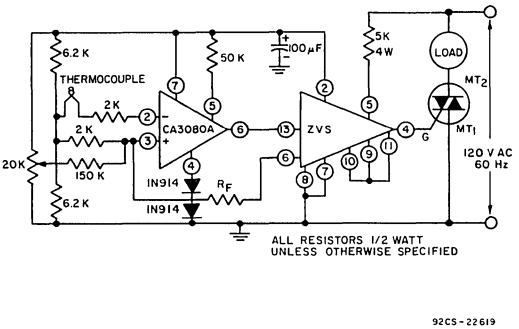
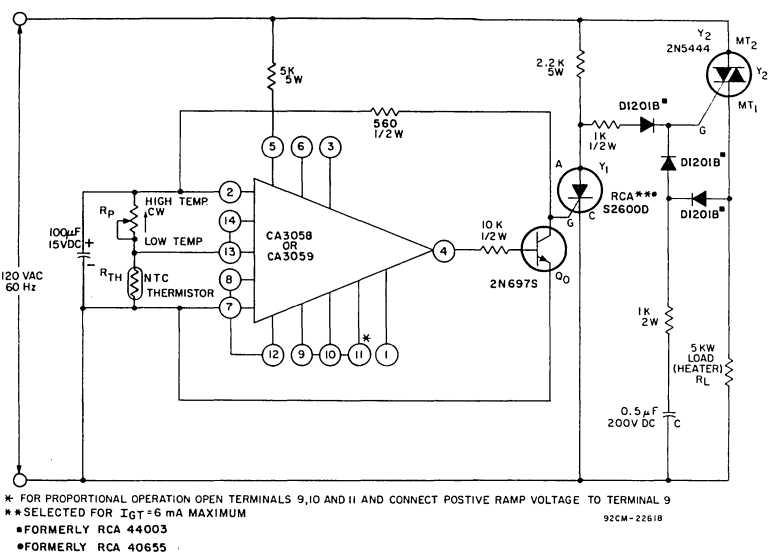



*Fig. 38 – Thermocouple temperature control with zero-voltage switching.*




* FOR PROPORTIONAL OPERATION OPEN TERMINALS 9,10 AND 11 AND CONNECT POSTIVE RAMP VOLTAGE TO TERMINAL 9
** SELECTED FOR $I_{GT}$ = 6 mA MAXIMUM
• FORMERLY RCA 44003
• FORMERLY RCA 40655

*Fig. 37 – CA3058 or CA3059 integral-cycle temperature controller that features a protection circuit and no half-cycling effect.*

## MACHINE CONTROL AND AUTOMATION

The earlier section on interfacing techniques indicated several techniques of controlling ac loads through a logic system. Many types of automatic equipment are not complex enough or large enough to justify the cost of a flexible logic system. A special circuit, designed only to meet the control requirements of a particular machine, may prove more economical. For example, consider the simple machine shown in Fig. 39; for each revolution of the motor, the belt is advanced a prescribed distance, and the strip is then punched. The machine also has variable speed capability.

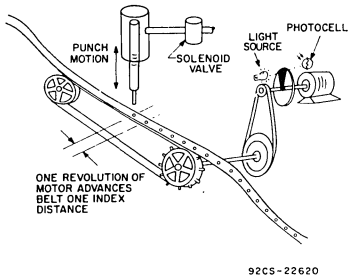



*Fig. 39 – Step-and-punch machine.*

The typical electromechanical control circuit for such a machine might consist of a mechanical cambank driven by a separate variable speed motor, a time delay relay, and a few logic and power relays. Assuming use of industrial-grade controls, the control system could get quite costly and large. Of greater importance is the necessity to eliminate transients generated each time a relay or switch energizes and deenergizes the solenoid and motor. Fig. 40 shows such transients, which might not affect the operation of this machine, but could affect the more sensitive solid-state equipment operating in the area.

A more desirable system would use triacs and zero-voltage switching to incorporate the following advantages:

a. Increased reliability and long life inherent in solid-state devices as opposed to moving parts and contacts associated with relays.

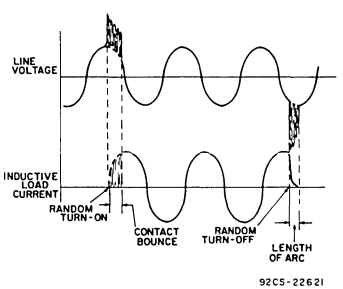



*Fig. 40 – Transients generated by relay-contact bounce and non-zero turn-off of inductive load.*

b. Minimized generation of EMI/RFI using zero-voltage switching techniques in conjunction with thyristors.
c. Elimination of high-voltage transients generated by relay-contact bounce and contacts breaking inductive loads, as shown in Fig. 39.
d. Compactness of the control system.

The entire control system could be on one printed-circuit board, and an over-all cost advantage would be achieved. Fig. 41 is a timing diagram for the proposed solid-state

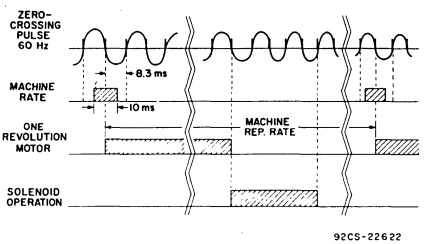



*Fig. 41 – Timing diagram for proposed solid-state machine control.*

machine control, and Fig. 42 is the corresponding control schematic. A variable-speed machine repetition rate pulse is set up using either a unijunction oscillator or a transistor astable multivibrator in conjunction with a 10-millisecond one-shot multivibrator. The first zero-voltage switch in Fig. 42 is used to synchronize the entire system to zero-voltage crossing. Its output is inverted to simplify adaptation to the rest of the circuit. The center zero-voltage switch is used as an interface for the photo-cell, to control one revolution of the motor. The gate drive to the motor triac is continuous dc, starting at zero voltage crossing. The motor is initiated when both the machine rate pulse and the zero-voltage sync are at low voltage. The bottom zero-voltage switch acts as a time-delay for pulsing the solenoid. The inhibit input, terminal 1, is used to assure that the solenoid will not be operated while the motor is running. The time delay can be adjusted by varying the reference level (50K potentiometer) at terminal 13 relative to the capacitor charging to that level on terminal 9. The capacitor is reset by the SCR during the motor operation. The gate drive to the solenoid triac is direct current. Direct current is used to trigger both the motor and solenoid triacs because it is the most desirable means of switching a triac into an inductive load. The output of the zero-voltage switch will be continuous dc by connecting terminal 12 to common. The output under dc operation should be limited to 20 milliamperes. The motor triac is synchronized to zero crossing because it is a high-crurent inductive load and there is a chance of generating RFI. The solenoid is a very low current inductive load, so there would be little chance of generating RFI: therefore, the initial triac turn-on can be random, which simplifies the circuitry.

This example shows the versatility and advantages of the RCA zero-voltage switch used in conjunction with triacs as interfacing and control elements for machine control.

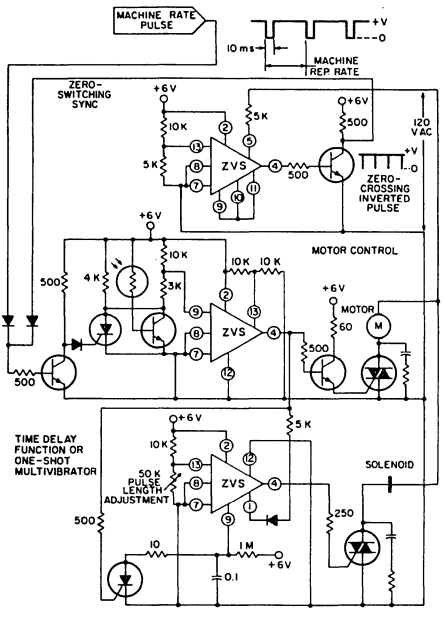



*Fig. 42 – Schematic of proposed solid-state machine control.*

## 400-Hz TRIAC APPLICATIONS

The increased complexity of aircraft control systems, and the need for greater reliability than electromechanical switching can offer, has led to the use of solid-state power switching in aircraft. Because 400-Hz power is used almost universally in aircraft systems, RCA offers a complete line of triacs rated for 400-Hz applications. Use of the RCA zero-voltage switch in conjunction with these 400-Hz triacs results in a minimum of RFI, which is especially important in aircraft.

Areas of application for 400-Hz triacs in aircraft include:

a. Heater controls for food-warming ovens and for windshield defrosters.
b. Lighting controls for instrument panels and cabin illumination
c. Motor controls
d. Solenoid controls
e. Power-supply switches

Lamp dimming is a simple triac application that demonstrates an advantage of 400-Hz power over 60-Hz power. Fig. 43 shows the adjustment of lamp intensity by phase control of the 60-Hz line voltage. RFI is generated by the step functions of power each half cycle, requiring extensive filtering. Fig. 44 shows a means of controlling power to the lamp by the zero-voltage-switching technique. Use of 400-Hz power makes possible the elimination of complete or half cycles within a period (typically 17.5 milliseconds)

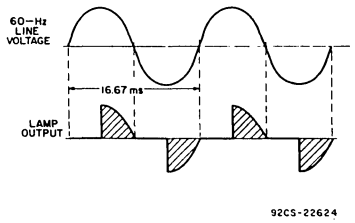



*Fig. 43 – Waveforms for 60-Hz phase-controlled lamp dimmer.*

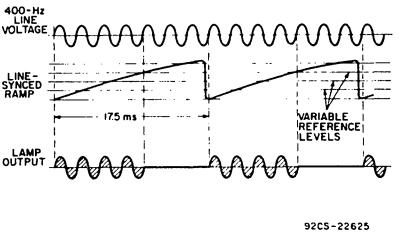



*Fig. 44 – Waveforms for 400-Hz zero-voltage-switched lamp dimmer.*

without noticeable flicker. Fourteen different levels of lamp intensity can be obtained in this manner. A line-synced ramp is set up with the desired period and applied to terminal No. 9 of the differential amplifier within the zero-voltage switch, as shown in Fig. 45. The other side of the differential amplifier (terminal No. 13) uses a variable reference level, set by the 50K potentiometer. A change of the potentiometer setting changes the lamp intensity.

In 400-Hz applications it may be necessary to widen and shift the zero-voltage switch output pulse (which is typically 12 microseconds wide and centered on zero voltage crossing), to assure that sufficient latching current is available. The 4K resistor (terminal No. 12 to common) and the 0.015-microfarad capacitor (terminal No. 5 to common) are used for this adjustment.

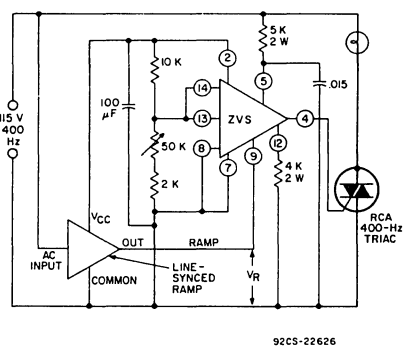



*Fig. 45 – Circuit diagram for 400-Hz zero-voltage-switched lamp dimmer.*

## SOLID-STATE TRAFFIC FLASHER

Another application which illustrates the versatility of the zero-voltage switch, when used with RCA thyristors, involves switching traffic-control lamps. In this type of application, it is essential that a triac withstand a current surge of the lamp load on a continuous basis. This surge results from the difference between the cold and hot resistance of the tungsten filament. If it is assumed that triac turn-on is at 90 degrees from the zero-voltage crossing, the first current-surge peak is approximately ten times the peak steady-state value or fifteen times the steady-state rms value. The second current-surge peak is approximately four times the steady-state rms value.

Transistors $Q_1$ and $Q_2$ inhibit these pulses to the gates of the triacs until the triacs turn on by the logical "1" ($V_{CC}$ high) state of the flip-flop.

The arrangement described can also be used for a synchronous, sequential traffic-controller system by addition of one triac, one gating transistor, a "divide-by-three" logic circuit, and modification in the design of the diac pulse generator. Such a system can control the familiar red, amber, and green traffic signals that are found at many intersections.

## SYNCHRONOUS LIGHT FLASHER

Fig. 47 shows a simplified version of the synchronous-switching traffic light flasher shown in Fig. 46.

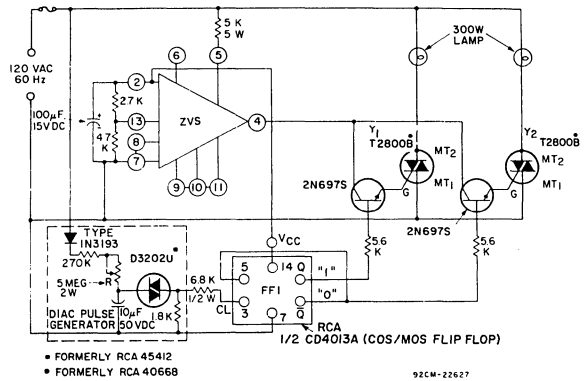



*Fig. 46 – Synchronous-switching traffic flasher.*

When the triac randomly switches the lamp, the rate of current rise di/dt is limited only by the source inductance. The triac di/dt rating may be exceeded in some power systems. In many cases, exceeding the rating results in excessive current concentrations in a small area of the device which may produce a hot spot and lead to device failure. Critical applications of this nature require adequate drive to the triac gate for fast turn-on. In this case, some inductance may be required in the load circuit to reduce the initial magnitude of the load current when the triac is passing through the active region. Another method may be used which involves the switching of the triac at zero line voltage. This method involves the supply of pulses to the triac gate only during the presence of zero voltage on the ac line.

Fig. 46 shows a circuit in which the lamp loads are switched at zero line voltage. This approach reduces the initial di/dt, decreases the required triac surge-current ratings, increases the operating lamp life, and eliminates RFI problems. This circuit consists of two triacs, a flip-flop (FF-1), the zero-voltage switch, and a diac pulse generator. The flashing rate in this circuit is controlled by potentiometer R, which provides between 10 and 120 flashes per minute. The state of FF-1 determines the triggering of triacs $Y_1$ or $Y_2$ by the output pulses at terminal 4 generated by the zero-crossing circuit. Flash rate is set by use of the curve shown in Fig. 16. If a more precise flash rate is required, the ramp generator described previously may be used. In this circuit, $ZVS_1$ is the master control unit and $ZVS_2$ is slaved to the output of $ZVS_1$ through its inhibit terminal (terminal 1). When power is applied to lamp No. 1, the voltage of terminal 6 on $ZVS_1$ is high and $ZVS_2$ is inhibited by the current in $R_x$. When lamp

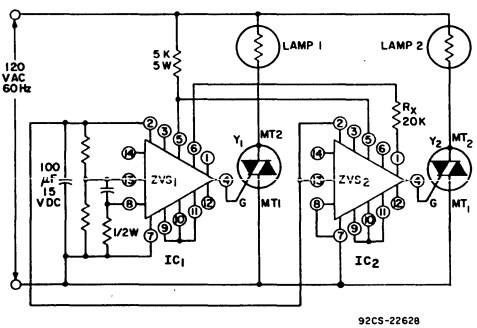



*Fig. 47 – Synchronous light flasher.*

No. 1 is off, $ZVS_2$ is not inhibited, and triac $Y_2$ can fire. The power supplies operate in parallel. The on-off sensing amplifier in $ZVS_2$ is not used.

## TRANSIENT-FREE SWITCH CONTROLLERS

The zero-voltage switch can be used as a simple solid-state switching device that permits ac currents to be turned on or off with a minimum of electrical transients and circuit noise.

The circuit shown in Fig. 48 is connected so that, after the control terminal 14 is opened, the electronic logic waits until the power-line voltage reaches a zero crossing before power is applied to the load $Z_L$. Conversely, when the control terminals are shorted, the load current continues until it reaches a zero crossing. This circuit can switch a load at zero current whether it is resistive or inductive.

The circuit shown in Fig. 49 is connected to provide the opposite control logic to that of the circuit shown in Fig. 48. That is, when the switch is closed, power is supplied to the load, and when the switch is opened, power is removed from the load.

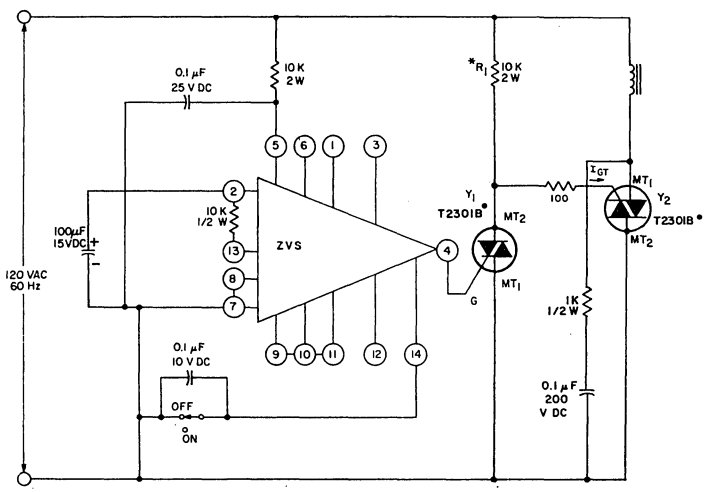
In both configurations, the maximum rms load current that can be switched depends on the rating of triac $Y_2$. If $Y_2$ is an RCA-2N5444 triac, an rms current of 40 amperes can be switched.

## DIFFERENTIAL COMPARATOR FOR INDUSTRIAL USE

Differential comparators have found widespread use as limit detectors which compare two analog input signals and provide a go/no-go, logic 'one" or logic "zero" output, depending upon the relative magnitudes of these signals. Because the signals are often at very low voltage levels and very accurate discrimination is normally required between them, differential comparators in many cases employ differential amplifiers as a basic building block. However, in many industrial control applications, a high-performance differential comparator is not required. That is, high resolution, fast switching speed, and similar features are not essential. The zero-voltage switch is ideally suited for use in such applications. Connection of terminal 12 to terminal 7 inhibits the zero-voltage threshold detector of the zero-voltage switch, and the circuit becomes a differential comparator.

Fig. 50 shows the circuit arrangement for use of the zero-voltage switch as a differential comparator. In this application, no external dc supply is required, as is the case with most commercially available integrated-circuit comparators; of course, the output-current capability of the zero-voltage switch is reduced because the circuit is operating in the dc mode. The 1000-ohm resistor $R_G$, connected between terminal 4 and the gate of the triac, limits the output current to approximately 3 milliamperes.

When the zero-voltage switch is connected in the dc mode, the drive current for terminal 4 can be determined from a curve of the external load current as a function of dc voltage from terminals 2 and 7. This curve is shown in the technical bulletin for RCA integrated-circuit zero-voltage switches, File No. 490. Of course, if additional output current is required, an external dc supply may be connected between terminals 2




*IF $Y_2$, FOR EXAMPLE, IS A 40-AMPERE TRIAC, THEN $R_1$ MUST BE DECREASED TO SUPPLY SUFFICIENT $I_{GT}$ FOR $Y_2$.

•FORMERLY RCA 40691

92CM-22629

*Fig. 48 – Zero-voltage switch transient-free switch controller in which power is supplied to the load when the switch is open.*

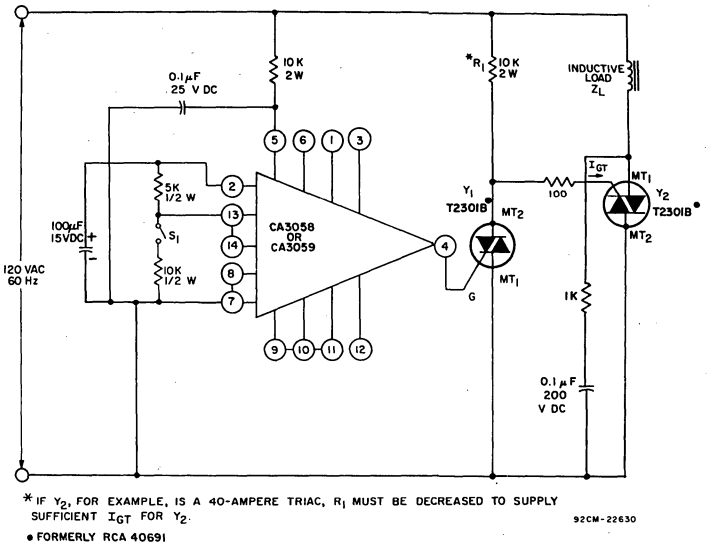



*Fig. 49 – Zero-voltage switch transient-free switch controller in which power is applied to the load when the switch is closed.*

and 7, and resistor $R_X$ (shown in Fig. 50) may be removed.

The chart below compares some of the operating characteristics of the zero-voltage switch, when used as a comparator, with a typical high-performance commercially available integrated-circuit differential comparator.

| Parameters | Zero-Voltage Switch (Typical Values) | Typical Integrated-Circuit Comparator (710) |
|---|---|---|
| Sensitivity | 30 mV | 2 mV |
| Switching speed (rise time) | > 20 μs | 90 ns |
| Output drive capability | *4.5 V at ⩽ 4 mA | 3.2 V at ⩽ 5.0 mA |

* Refer to Fig. 20; $R_X$ equals 5000 ohms.

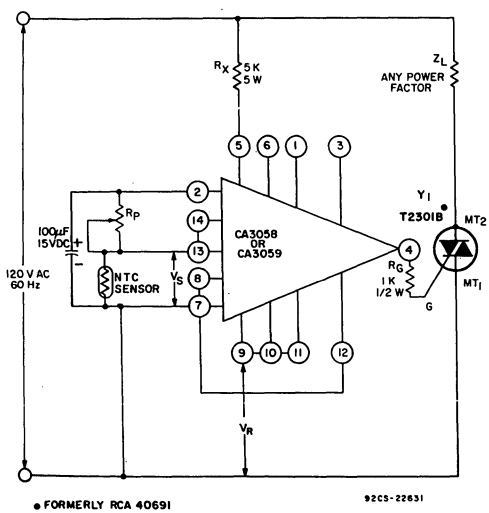



*Fig. 50 – Differential comparator using the CA3058 or CA3059 integrated-circuit zero-voltage switch.*

## POWER ONE-SHOT CONTROL

Fig. 51 shows a circuit which triggers a triac for one complete half-cycle of either the positive or negative alternation of the ac line voltage. In this circuit, triggering is initiated by the push button PB-1, which produces triggering of the triac near zero voltage even though the button is randomly depressed during the ac cycle. The triac does not trigger again until the button is released and again depressed. This type of logic is required for the solenoid drive of electrically operated stapling

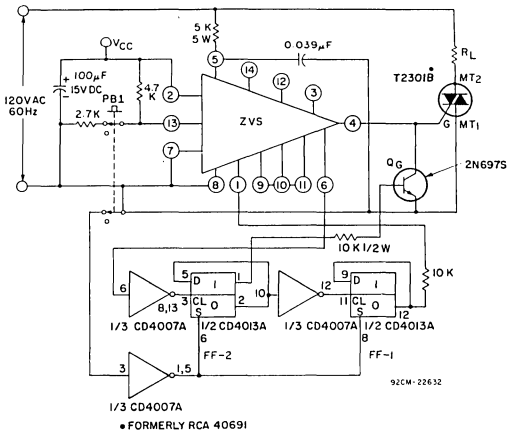



*Fig. 51 – Block diagram of a power one-shot control using a zero-voltage switch.*

guns, impulse hammers, and the like, where load-current flow is required for only one complete half-cycle. Such logic can also be adapted to keyboard consoles in which contact bounce produces transmission of erroneous information.

In the circuit of Fig. 51, before the button is depressed, both flip-flop outputs are in the "zero" state. Transistor $Q_G$ is biased on by the output of flip-flop FF-1. The differential comparator which is part of the zero-voltage switch is initially biased to inhibit output pulses. When the push button is depressed, pulses are generated, but the state of $Q_G$ determines the requirement for their supply to the triac gate. The first pulse generated serves as a "framing pulse" and does not trigger the triac but toggles FF-1. Transistor $Q_G$ is then turned off. The second pulse triggers the triac and FF-1 which, in turn, toggles the second flip-flop FF-2. The output of FF-2 turns on transistor $Q_7$, as shown in Fig. 52, which inhibits all further output pulses. When the pushbutton is released, the circuit resets itself until the process is repeated with the button. Fig. 53 shows the timing diagram for the described operating sequence.

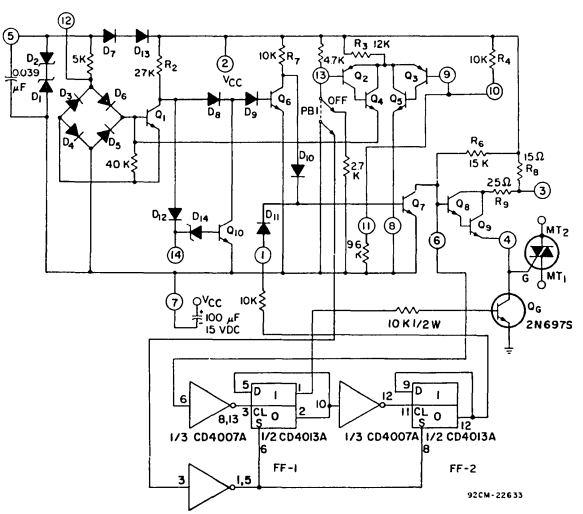



*Fig. 52 – Circuit diagram for the power one-shot control.*

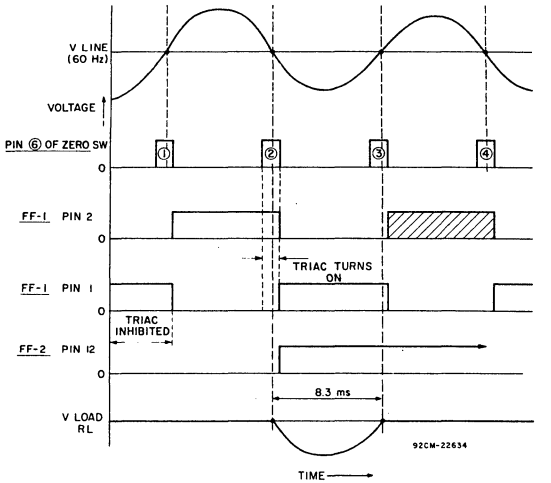



*Fig. 53 – Timing diagram for the power one-shot control.*

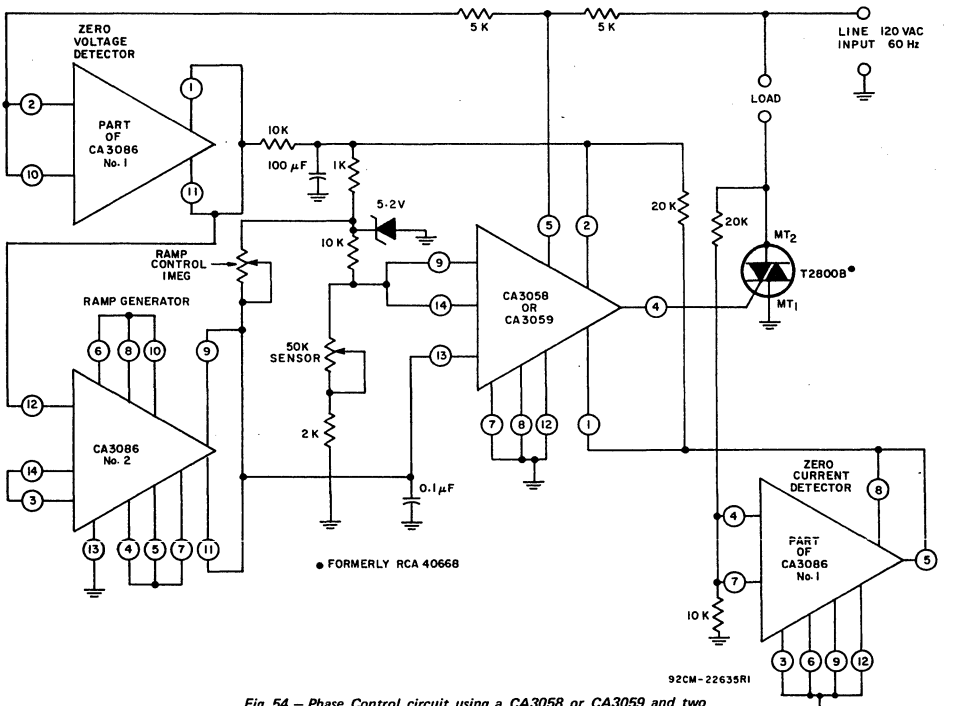



*Fig. 54 – Phase Control circuit using a CA3058 or CA3059 and two CA3086 integrated-circuits.*

### PHASE CONTROL CIRCUIT

Fig. 54 shows a circuit using a CA3058 or CA3059 zero-voltage switch together with two CA3086 integrated-circuit transistor arrays to form a phase-control circuit. This circuit is specifically designed for speed control of ac induction motors, but may also be used as a light dimmer. The circuit, which can be operated from a line frequency of 50-Hz to 400-Hz, consists of a zero-voltage detector, a line-synchronized ramp generator, a zero-current detector, and a line-derived control circuit (i.e., the zero-voltage switch). The zero-voltage detector (part of CA3086 No. 1) and the ramp generator (CA3086 No. 2) provide a line-synchronized ramp-voltage output to terminal 13 of the zero-voltage switch. The ramp voltage, which has a starting voltage of 1.8 volts, starts to rise after the line voltage passes the zero point. The ramp generator has an oscillation frequency of twice the incoming line frequency. The slope of the ramp voltage can be adjusted by variation of the resistance of the 1-megohm ramp-control potentiometer. The output phase can be controlled easily to provide 180° firing of the triac by programming the voltage at terminal 9 of the zero-voltage switch. The basic operation of the zero-voltage switch driving a thyristor with an inductive load was explained previously in the discussion on switching of inductive loads.

## TRIAC POWER CONTROLS FOR THREE-PHASE SYSTEMS

This section describes recommended configurations for power-control circuits intended for use with both inductive and resistive balanced three-phase loads. The specific design requirements for each type of loading condition are discussed.

In the power-control circuits described, the integrated-circuit zero-voltage switch is used as the trigger circuit for the power triacs. The following conditions are also imposed in the design of the triac control circuits:

1. The load should be connected in a three-wire configuration with the triacs placed external to the load; eiter delta or wye arrangements may be used. Four-wire loads in wye configurations can be handled as three independent single-phase systems. Delta configurations in which a triac is connected within each phase rather than in the incoming lines can also be handled as three independent single-phase systems.
2. Only one logic command signal is available for the control circuits. This signal must be electrically isolated from the three-phase power system.
3. Three separate triac gating signals are required.
4. For operation with resistive loads, the zero-voltage switching technique should be used to minimize any radio-frequency interference (RFI) that may be generated.

### Isolation of DC Logic Circuitry

As explained earlier under **Special Application Considerations**, isolation of the dc logic circuitry* from the ac line, the triac, and the load circuit is often desirable even in many single-phase power-control applications. In control circuits for polyphase power systems, however, this type of isolation is essential, because the common point of the dc logic circuitry cannot be referenced to a common line in all phases.

In the three-phase circuits described in this section, photo-optic techniques (i.e., photo-coupled isolators) are used to provide the electrical isolation of the dc logic command signal from the ac circuits and the load. The photo-coupled isolators consist of an infrared light-emitting diode aimed at a silicon photo transistor, coupled in a common package. The light-emitting diode is the input section, and the photo transistor is the output section. The two components provide a voltage isolation typically of 1500 volts. Other isolation techniques, such as pulse transformers, magnetoresistors, or reed relays, can also be used with some circuit modifications.

### Resistive Loads

Fig. 55 illustrates the basic phase relationships of a balanced three-phase resistive load, such as may be used in heater applications, in which the application of load power is

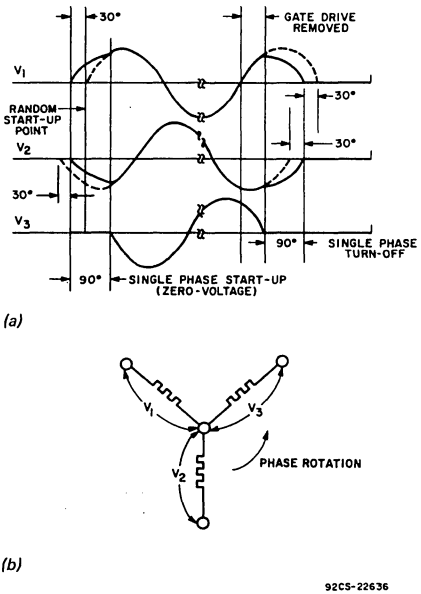



*Fig. 55 – Voltage phase relationship for a three-phase resistive load when the application of load power is controlled by zero-voltage switching: (a) voltage waveforms, (b) load-circuit orientation of voltages. (The dashed lines indicate the normal relationship of the phases under steady-state conditions. The deviation at start-up and turn-off should be noted.)*

* The dc logic circuitry provides the low-level electrical signal that dictates the state of the load. For temperature controls, the dc logic circuitry includes a temperature sensor for feedback. The RCA integrated-circuit zero-voltage switch, when operated in the dc mode with some additional circuitry, can replace the dc logic circuitry for temperature controls.

controlled by zero-voltage switching. The following conditions are inherent in this type of application:

1. The phases are 120 degrees apart; consequently, all three phases cannot be switched on simultaneously at zero voltage.
2. A single phase of a wye configuration type of three-wire system cannot be turned on.
3. Two phases must be turned on for initial starting of the system. These two phases form a single-phase circuit which is out of phase with both of its component phases. The single-phase circuit leads one phase by 30 degrees and lags the other phase by 30 degrees.

These conditions indicate that in order to maintain a system in which no appreciable RFI is generated by the switching action from initial starting through the steady-state operating condition, the system must first be turned on, by zero-voltage switching, as a single-phase circuit and then must revert to synchronous three-phase operation.

Fig. 56 shows a simplified circuit configuration of a three-phase heater control that employs zero-voltage synchronous switching in the steady-state operating condition, with random starting. In this system, the logic command to turn on the system is given when heat is required, and the command to turn off the system is given when heat is not required. Time proportioning heat control is also possible through the use of logic commands.

The three photo-coupled inputs to the three zero-voltage switches change state simultaneously in response to a "logic command". The zero-voltage switches then provide a positive pulse, approximately 100 microseconds in duration, only at a zero-voltage crossing relative to their particular phase. A balanced three-phase sensing circuit is set up with the three zero-voltage switches each connected to a particular phase on their common side (terminal 7) and referenced at their high side (terminal 5), through the current-limiting resistors R4, R5, and R6, to an established artificial neutral point. This artificial neutral point is electrically equivalent to the inaccessible neutral point of the wye type of three-wire load and, therefore, is used to establish the desired phase relationships. The same artificial neutral point is also used to establish the proper phase relationships for a delta type of three-wire load. Because only one triac is pulsed on at a time, the diodes (D1, D2, and D3) are necessary to trigger the opposite-polarity triac, and, in this way, to assure initial latching-on of the system. The three resistors (R1, R2, and R3) are used for current limiting of the gate drive when the opposite-polarity triac is triggered on by the line voltage.

In critical applications that require suppression of all generated RFI, the circuit shown in Fig. 57 may be used. In addition to synchronous steady-state operating conditions, this circuit also incorporates a zero-voltage starting circuit. The start-up condition is zero-voltage synchronized to a

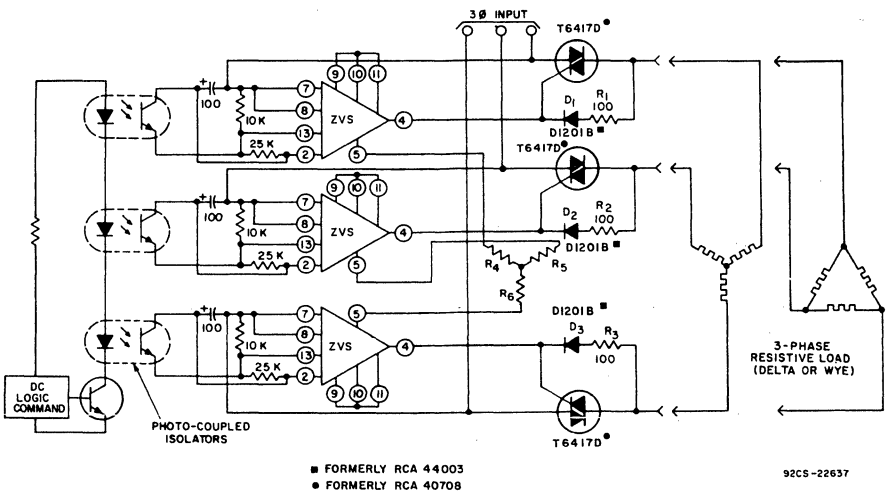



*Fig. 56 – Simplified diagram of a three-phase heater control that employs zero-voltage synchronous switching in the steady-state operating conditions.*

single-phase, 2-wire, line-to-line circuit, comprised of phases A and B. The logic command engages the single-phase start-up zero-voltage switch and three-phase photo-coupled isolators OC13, OC14, OC15 through the photo-coupled isolators OC11 and OC12. The single-phase zero-voltage switch, which is synchronized to phases A and B, starts the system at zero voltage. As soon as start-up is accomplished, the three photo-coupled isolators OC13, OC14, and OC15 take control, and three-phase synchronization begins. When the "logic command" is turned off, all control is ended, and the triacs automatically turn off when the sine-wave current decreases to zero. Once the first phase turns off, the other two will turn off simultaneously, 90° later, as a single-phase line-to-line circuit, as is apparent from Fig. 55.

**Inductive Loads**

For inductive loads, zero-voltage turn-on is not generally required because the inductive current cannot increase instantaneously; therefore, the amount of RFI generated is usually negligible. Also, because of the lagging nature of the inductive current, the triacs cannot be pulse-fired at zero voltage. There are several ways in which the zero-voltage switch may be interfaced to a triac for inductive-load applications. The most direct approach is to use the zero-voltage switch in the dc mode, i.e., to provide a continuous dc output instead of pulses at points of zero-voltage crossing. This mode of operation is accomplished by connection of terminal 12 to terminal 7, as shown in Fig. 58. The output of the zero-voltage switch should also be

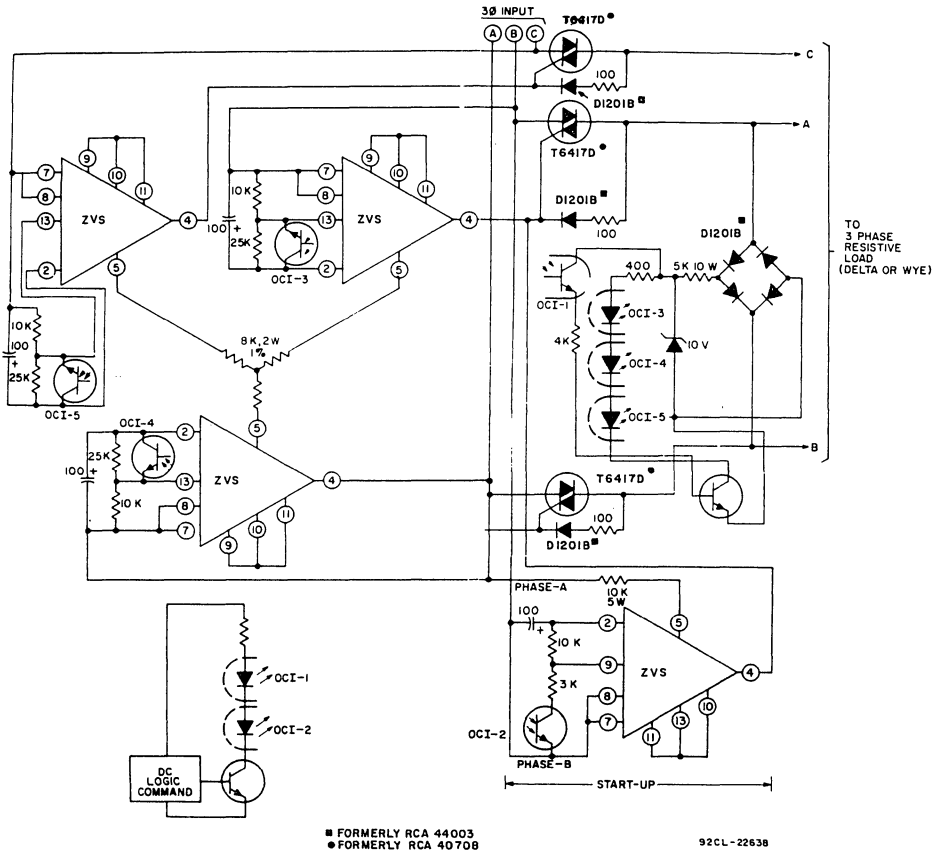



*Fig. 57 – Three-phase power control that employs zero-voltage synchronous switching both for steady-state operation and for starting.*

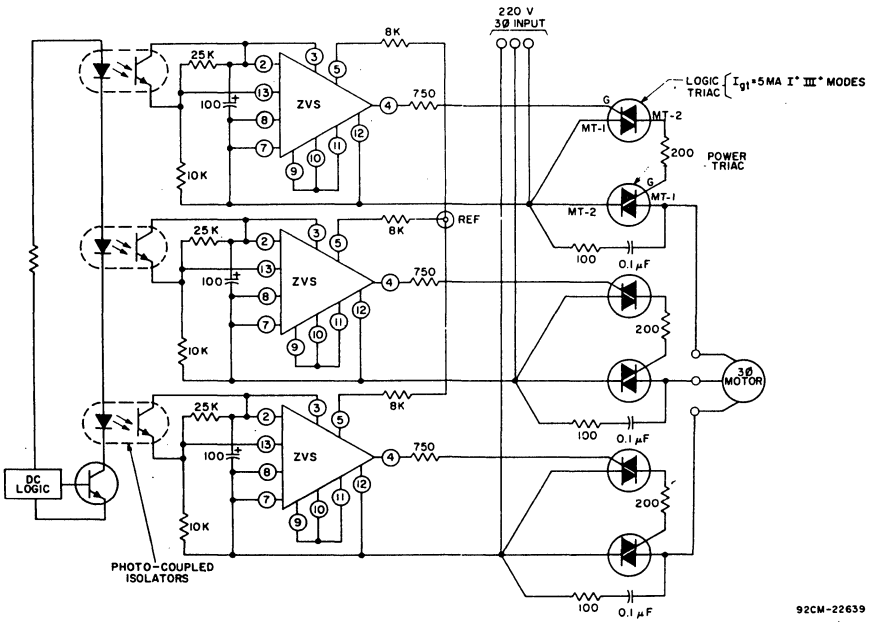



*Fig. 58 – Triac three-phase control circuit for an inductive load, i.e., three-phase motor.*

limited to approximately 5 milliamperes in the dc mode by the 750-ohm series resistor. Use of a triac such as the T2301D* is recommended for this application. Terminal 3 is connected to terminal 2 to limit the steady-state power dissipation within the zero-voltage switch. For most three-phase inductive load applications, the current-handling capability of the 40692 triac (2.5 amperes) is not sufficient. Therefore, the 40692 is used as a trigger triac to turn on any other currently available power triac that may be used. The trigger triac is used only to provide trigger pulses to the gate of the power triac (one pulse per half cycle); the power dissipation in this device, therefore, will be minimal.

Simplified circuits using pulse transformers and reed relays will also work quite satisfactorily in this type of application. The RC networks across the three power triacs are used for suppression of the commutating dv/dt when the circuit operates into inductive loads.

* Formerly RCA 40692

The specific integrated-circuits, triacs, SCR's, and rectifiers included in circuit diagrams shown in this Application Note are listed below. Additional information on these devices can be obtained by requesting the applicable RCA data-bulletin file number.

| Type No. | File No. | Type No. | File No. |
|---|---|---|---|
| CA3058, CA3059, and CA3079 | 490 | T2300B (40526) | 470 |
| CA3099E | 620 | T2301B (40691), T2301D (40692) | 431 |
| CA3086 | 483 | T64170 (40708) | 406 |
| CA3080 | 475 | S2600D (40655) | 496 |
| CD4007A, CD4013A | 479 | D1201B (44003) | 495 |
| 2N5444 | 456 | D3202U (45412) | 577 |
| T2800B (40668) | 364 | | |

Note: Numbers in parenthesis (e.g. 40668) are former RCA type numbers.

# DESIGNING WITH AN IC TRANSISTOR ARRAY CONTAINING MATCHED SUPER-BETA TRANSISTORS

by T. J. Robe

Many small-signal, low-frequency, and video-frequency applications require an amplifying device with a very high input impedance, low input-bias current, and low-noise characteristics that can maintain low dc offset voltage and drift. Examples of such applications include:

Small-signal instrumentation - chart recorders, meters, etc.
Pre-amps for op-amps.
Magnetic tape-head and photo-cartridge amplifiers.
Opto-electric amplifiers.
Medical electronics.

Devices suitable for such applications are also generally applicable in circuits having long time constants, such as timers, integrators, monostable oscillators, comparators, and low-frequency oscillators. Matched super-beta transistors are well suited for use in these applications.

Super-beta transistors are similar to conventional bipolar transistors except that they have betas in the range of 1000 to 5000; the beta range of a conventional bipolar transistor is from 50 to 400. Since super-beta transistors are commonly used in high-source-impedance applications that require high input impedance and low-noise characteristics, it is equally important that they exhibit super-beta performance at operating currents of a few microamperes. On the other hand, to achieve broadband characteristics in video-amplifier applications, super-beta performance must be maintained with collector currents of 1 milliampere or more. This Note describes the RCA-CA3095 super-beta transistor array and discusses its operation in some typical applications.

## A TRANSISTOR-ARRAY IC CONTAINING SUPER-BETA TRANSISTORS

Fig.1 shows the schematic diagram of the RCA-CA3095E, a monolithic IC[1] containing an array of n-p-n transistors of which $Q_1$ and $Q_2$ have super-beta characteristics. $Q_1$ and $Q_2$ are connected, in conjunction with transistors $Q_3$ and $Q_4$, in a differential-cascode-amplifier configuration. Since the super-beta transistors in this IC have a collector-emitter breakdown voltage $V_{(BR)CEO}$ of about 2 volts, it is necessary to limit the collector-emitter voltage accordingly. Limiting is accomplished

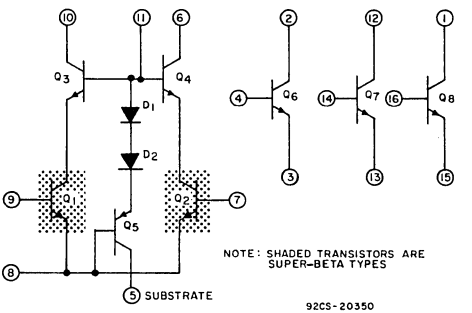



*Fig. 1 – Schematic diagram of the CA3095E.*

by means of the voltage-limiting network composed of $D_1$, $D_2$ and $Q_5$; these components are included on the CA3095E chip. With this arrangement, the voltage applied to the bases of $Q_1$ and $Q_2$ can be varied over a wide common-mode voltage range while the collector-emitter voltages are restrained within a maximum range of about 1.5 volts. The collectors of transistors $Q_3$ and $Q_4$ have a minimum collector-to-emitter breakdown voltage of 35 volts. The salient characteristics of the differential-cascode amplifier ($Q_1$ through $Q_4$) is the "super-high" ratio between the collector currents (at terminals 10 and 6) and the base currents (into terminals 9 and 7, respectively). The beta of the circuit is typically in the range of 1000 to 5000 at collector currents ranging from less than 1 microampere to more than 1 milliampere. As a consequence, amplifier circuits can be designed to operate with extremely small input base-bias currents. Implicit in this performance are high input impedance, low noise, and low dc offset-error effects.

Transistors $Q_5$, $Q_6$, and $Q_7$ are conventional n-p-n types with betas in the range of 150 to 400 at collector currents in the range of 1 microampere to 10 milliamperes. These transistors also have a minimum collector-emitter breakdown voltage $V_{(BR)CEO}$ of 35 volts.

### Operating the Super-Beta, Differential-Cascode Amplifier

Application of the differential-cascode amplifier in the CA3095E is similar to that of the classical differential-cascode amplifier; differential input signals are applied at terminals 7 and 9 with balanced collector loads connected from terminals 6 and 10 to the positive supply voltage. The common emitter connection, terminal 8, may be made directly or through a "current source" (e.g., a transistor or resistor) to the negative supply voltage. The circuit in Fig. 2 illustrates the use of "mirrored" transistors ($Q_7$, $Q_8$) as a constant-current source to provide high emitter impedance for the differential-cascode amplifier. As an alternative, a resistor may be used as a "current source" (as illustrated by the circuit in Figs. 8, 9, and 11). The IC substrate (terminal 5) is usually connected directly to the negative supply terminal, as shown in Fig. 2, because it must be maintained at the most negative potential of all elements on the CA3095E chip.

The only additional requirement for CA3095E operation is for bias current into terminal 11 to forward-bias the network composed of $D_1$, $D_2$ and Q5, and to supply base-bias current for transistors $Q_3$ and $Q_4$. This base-bias current can be provided by connecting a dropping resistor between terminal 11 and the positive supply voltage; this arrangement is illustrated by the use of resistor $R_{BIAS}$ in Fig. 2. As an alternative, this current can be supplied from the positive supply to terminal 11 through a p-n-p constant-current-source transistor to maximize common-mode and power-supply rejection characteristics. In most applications, however, such a constant-current-source arrangement is not necessary because transistor $Q_5$ conducts most of the $D_1$, $D_2$ signal current to the IC substrate connected to terminal 5. As a general rule, the current supplied to terminal 11 should be approximately 4 to 10 per cent of the current drawn from terminal 8. The input signals to the super-beta transistors (terminals 7 and 9) should not be permitted to swing more than 6 volts below the voltage at terminal 11 to avoid exceeding the $V_{CBO}$ rating of super-beta transistors $Q_1$ and $Q_2$. This factor is normally a design consideration only when one or both of the input-stage transistors is to be biased off.

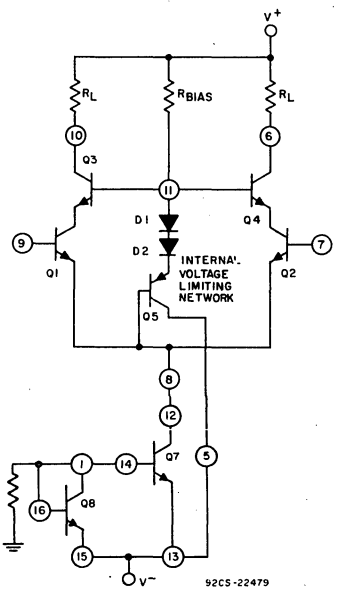



*Fig. 2 – Bias arrangement for operation of the super-beta differential-cascode amplifier.*

### Low-Frequency Operation

When an amplifier is to operate at very low frequencies, or as a dc amplifier, the signal source must be directly coupled to the amplifier input. This coupling requires the use of an amplifying device with a very low input dc offset error and low offset-error drift with temperature variations. A matched differential-cascode amplifier, like the one used in the CA3095E, is particularly well suited to this requirement, not only because of its low input offset voltage ($V_{IO}$ = 1 mV, typical), but also because of its low input offset current ($I_O$ = 4 nA, typical, at $I_C$ = 100 μA). When the input signal is provided from a high-impedance source ($R_S$), both of these characteristics assume importance because the total effective input-offset-voltage error is the sum of their effects:

$$\text{Total Offset Error} = V_{IO} + I_{IO}R_S$$

The differential input impedance in megohms ($Z_{id}$ in Fig. 3) of an amplifier operating at low frequencies is given by:

$$Z_{id} = \frac{26\text{ mV X the number of p-n junctions in the input stage}}{I_{IB}\text{ (in nA)}}\ M\Omega$$

where $I_{IB}$ is the input-stage base-bias current. Consequently, the input bias current ($I_{IB}$) must be quite low if a high input impedance is to be established. The characteristics of the super-beta transistors in the CA3095E are well suited for use

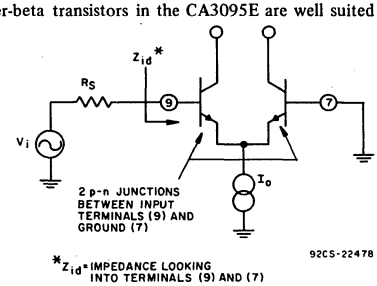



*Fig. 3 – Input circuit for the differential amplifier.*

in dc amplifiers requiring high input impedance. For example, with the super-beta transistors operating at input-stage emitter currents of 1 microampere and an $H_{FE}$ of 2000, the base-bias current is only 0.5 nanoampere. Under these conditions,

$$Z_{id} = \frac{26\text{ mV X }2}{0.5\text{ nA}} = 104\text{ megohms}$$

Impedance levels of this order can also be realized by using negative feedback in connection with devices having higher

input bias currents, as illustrated by the circuit shown in Fig. 4. In this arrangement, the use of the feedback network effectively multiplies the differential input impedance. Unfortunately, this arrangement does not avoid the input-offset-voltage effect resulting from the flow of unequal currents through the signal-source resistance ($R_S$) and the equivalent resistance of the feedback network; i.e., $R_i//R_f$. Consequently, the advantage to be gained by using super-beta transistors is apparent.

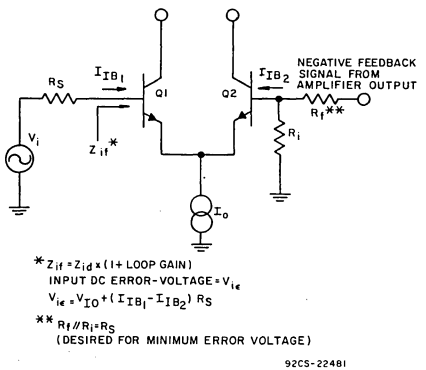



*Fig. 4 — Differential input with provisions for feedback.*

### Considerations in Low-Noise Performance

Fig.5 shows the schematic diagram of a noise model useful in a review of the considerations pertinent to optimizing low-noise performance in amplifier operation.

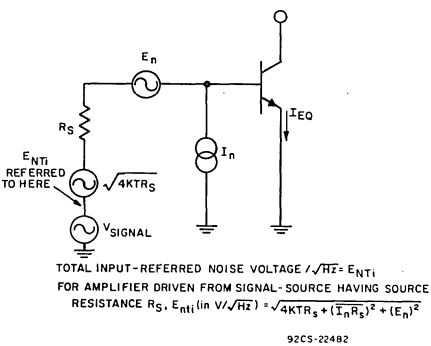



*Fig. 5 — Sources of noise in the transistor-amplifier stage.*

This model illustrates that consideration must be given to three major sources of noise:

1. Noise contributed by the "thermal-noise" voltage developed across the signal-source resistance, $R_S$. The magnitude of this voltage in $V/\sqrt{Hz}$ is approximately equal to $\sqrt{4KTR_S}$ for a 1-cycle bandwidth, where k is Boltzmann's constant ($1.38 \times 10^{-23}$ joule/°K), T is the temperature in degrees Kelvin, and $R_S$ is the source resistance in ohms.
2. The noise voltage, $E_n$, resulting from the combined effects of shot noise due to emitter current flow and thermal noise due to transistor base resistance. These effects add in rms fashion to give a total $E_n$ equal to $(E_{shot}^2 + 4KTrb'b)^{1/2}$. The shot-noise component, $E_{shot}$, is inversely proportional to the square root of $I_{EQ}$, and has a value

$$E_{shot} = \frac{14.2 \times 10^{-12}}{\sqrt{I_{EQ}}} (V/Hz.)$$

   In super-beta transistors, the base resistance component of $E_n$ tends to dominate, particularly at currents greater than 10 microamperes. In addition, this component of $E_n$ has been experimentally found to be inversely related to operating current. Therefore, the total value of $E_n$ is inversely related to operating current $I_{EQ}$. For example, the CA3095E has a total 1-kHz $E_n$ of approximately 15 $nV/\sqrt{Hz}$ at a collector current of 5 microamperes and approximately 8 $nV/\sqrt{Hz}$ at 50 microamperes.
3. The noise current, $I_n$, resulting from the combined "shot noise" generated by the flow of base current and the 1/f noise generated in the transistor. The magnitude of $I_n$ is approximately proportional to $\sqrt{I_{IB}}$, where $I_{IB}$ is the base current. The value of $I_n$ is typically 0.12 $pA/\sqrt{Hz}$ at f = 10 Hz when the super-beta differential-cascode amplifier in the CA3095E is operating at $I_{EQ} = 5\ \mu A$. $I_n$ decreases to approximately 0.03 $pA\sqrt{Hz}$ at f = 1 kHz.

When each input terminal in a differential amplifier is driven from a source resistance ($R_S$), the total noise voltage (referred to the input, see Fig. 5) per unit bandwidth is given by:

$$E_{nti}\ (\text{in } V/\sqrt{Hz}) = \sqrt{2KTR_S + 2(\overline{I_nR_S})^2 + (E_n)^2}$$

When amplifiers are driven from low source impedances, $E_n$ is the predominant factor in noise contributions, whereas the effect of $I_n$ predominates when input signals are supplied from high source impedances. Consequently, since the CA3095E operates with very high beta at very low operating currents, it has exceptionally low values of $I_n$, and is an excellent choice to amplify signals from high source resistances when low amplifier noise contribution is desired. Additionally, the incidence of "popcorn" (burst) noise[2] is low in the CA3095E, a characteristic which further enhances its suitability for use in amplifying signals supplied from high-impedance sources. Figs. 6 and 7 show typical data on $I_n$ and $E_n$ characteristics, respectively, as a function of frequency, for the super-beta transistors in the CA3095E.

Because the operating current of the super-beta transistors in the CA3095E is adjustable over a wide range, the circuit designer can optimize the operating current for maximum

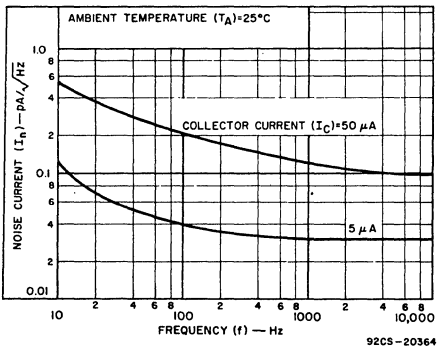



*Fig. 6 — Noise current $I_n$ as a function of frequency f for each super-beta cascode-amplifier transistor pair ($Q_1$ - $Q_3$ and $Q_2$ - $Q_4$).*

signal-to-noise ratio at a particular frequency and source resistance. This adjustment is accomplished by selecting an operating point for which $E_n$ is approximately equal to $\sqrt{2}\, I_n\, R_s$. For example, the optimum operating collector currents in the differential-cascode amplifier are about 5 microamperes when the amplifier is to be driven from two 300-kilohm source resistors. For operation from higher source resistances, the currents should be proportionately lower, and vice versa. Operating currents in the range from 0.1 to 1.0 milliampere are recommended when the amplifier is to be operated as a low-noise video amplifier. At these current levels, the gain-bandwidth product ($f_T$) is increased significantly with respect to low collector current operation.

## ILLUSTRATIVE CIRCUIT APPLICATIONS

Like other RCA transistor-array IC's, the CA3095E offers the circuit designer a class of solid-state devices featuring matched electrical and thermal characteristics, compactness, ease of physical handling, economy, and versatility of use. The CA3095E is an electronic "building block" which permits the designer to optimize performance of a particular circuit for gain, noise, power consumption, bandwidth, and/or other specific considerations. Some typical circuit applications of the CA3095E are described below.

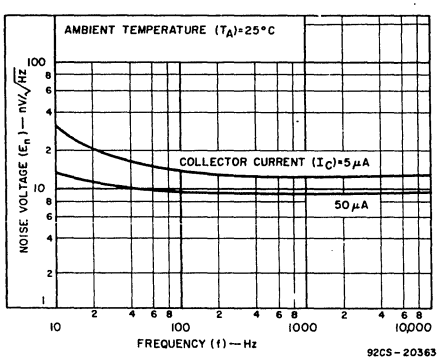



*Fig.7 — Noise voltage $E_n$ as a function of frequency f for each super-beta cascode-amplifier transistor pair ($Q_1$–$Q_3$ and $Q_2$–$Q_4$).*

### High-Input-Resistance Low-Noise Amplifier

The CA3095E contains all the transistors necessary for the construction of a low-noise, feedback amplifier having a high input resistance ($R_{IN} \cong 20$ MΩ) and a 3-dB bandwidth of about 50 kHz. In the circuit shown in Fig. 8, voltage gain is provided by a cascade of two stages, the differential-cascode

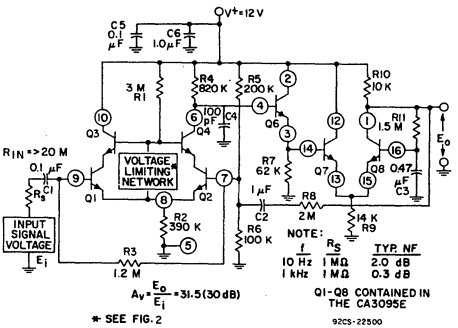



*Fig. 8 — High-input-resistance, low-noise amplifier circuit.*

stage ($Q_1, Q_3$ - $Q_2, Q_4$) and the differential stage ($Q_7, Q_8$). Transistor $Q_6$ is an interstage emitter-follower. The voltage gain of the amplifier (approximately 30 dB with the circuit values shown) is essentially established by the ratio of $R_8$ to the parallel combination of $R_5$ and $R_6$. The $R_8, C_2$ network couples feedback around the entire amplifier. Capacitor $C_4$ provides stabilizing compensation. The output-voltage swing ($E_o$) is typically 3 volts, peak-to-peak. Typical noise-figure data are shown in Fig. 8. Power consumption of the amplifier is typically about 750 microamperes at a supply voltage of 12 volts, although the current in transistors $Q_1$ and $Q_2$ is less than 5 microamperes.

### Low-Noise Video Amplifier

The circuit shown in Fig. 9 illustrates the use of super-beta transistors in the input stage of a video amplifier. The circuit is capable of delivering 4 volts, peak-to-peak, of output signal with a typical gain of 33 dB across a bandwidth from dc to 10 MHz (3-dB point). In this application, each super-beta transistor is biased for operation at about 400 microamperes to achieve wideband operation. The super-beta transistor characteristics minimize the contributions to noise generated by noise current ($I_n$) in the input stage. The equivalent input-noise-voltage-vs-frequency characteristics for the entire amplifier circuit are shown in Fig.10. Transistors $Q_1$ through $Q_4$ are connected as an emitter-coupled pair of cascode amplifiers with a single-ended load resistor, $R_3$, to drive a discrete transistor Q-PNP. This

combination provides sufficient current gain to drive $Q_6$, the voltage-gain-stage transistor, with load resistor $R_8$. Resistor $R_7$ provides a path for dc and ac feedback around this stage. Transistor $Q_8$ is an emitter-follower output stage. The typical current drain of the amplifier is approximately 8 milliamperes at a total supply voltage of 10 volts.

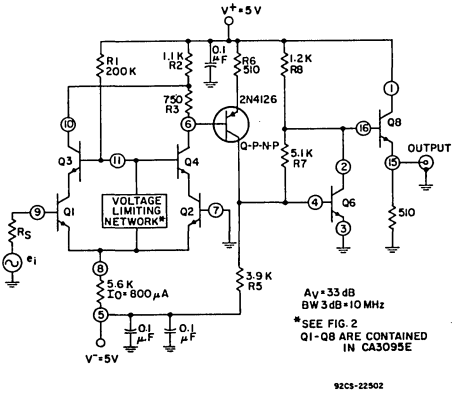



*Fig. 9 – Video amplifier.*

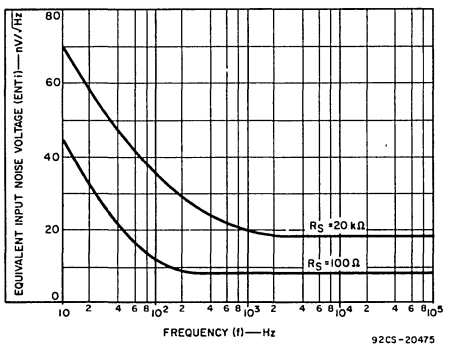



*Fig. 10 – Equivalent input noise voltage vs frequency for the circuit of Fig. 9.*

### Long-Delay Monostable Multivibrator

Super-beta transistors are useful in the design of long-delay, monostable multivibrator circuits, as illustrated in the circuit of Fig. 11. Basically, the circuit is a differential-cascode amplifier biased so that, in the quiescent state, the current path through transistors $Q_1$ and $Q_3$ is cut off, and the path through transistors $Q_2$ and $Q_4$ is conductive. This arrangement is accomplished by biasing the base of transistor $Q_2$ so that it

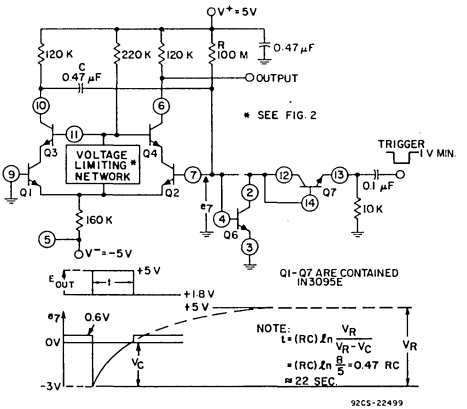



*Fig. 11 – Long-delay monostable-multivibrator circuit.*

is one step of $V_{be}$ (potential $e_7 \cong 0.6$ V) above the base of transistor $Q_1$, a condition established by the diode-connected transistor $Q_6$ in shunt with the base of $Q_2$. The timing cycle is initiated by the application of a negative-going trigger pulse at terminal 13, which is coupled to the base of $Q_2$ through diode-connected transistor $Q_7$. $Q_2$ is cut off and the output voltage rises to essentially V+. Since $Q_1$ and $Q_2$ are emitter-coupled, $Q_1$ is turned on by the trigger pulse, and the potential at terminal 10 drops rapidly; this drop pulls the left-side electrode of capacitor C toward ground. The right-side electrode of capacitor C is connected to the positive 5-volt supply terminal through resistor R; this connection permits the capacitor to be charged in the exponential characteristic of an RC network and, primarily, determines the delay time. Eventually, voltage $e_7$ rises sufficiently to again switch $Q_2$ on (and Q1 off) so that the output voltage drops to its quiescent level (approximately +1.8 V) to signify the end of the timing period. The trigger-voltage pulse should be at least -1 volt in amplitude to assure positive switching.

### Low-Input-Bias Current Comparator

The circuit shown in Fig. 12 employs the super-beta and conventional transistors in the CA3095E in a comparator circuit that requires an input signal of only 1.5 nanoamperes at threshold to produce toggling. The output of the circuit can interface directly with COS/MOS logic circuits. Transistor pairs $Q_1 - Q_3$ and $Q_2 - Q_4$ are connected in the differential-cascode arrangement described above. Transistor $Q_6$ is a programmable constant-current source (i.e., capable of being keyed, gated, clocked, etc.) for the differential-cascode pair. Transistors $Q_7$ and $Q_8$ are a differential pair used to provide sufficient gain for the control of the external discrete transistor Q-PNP. The reference voltage for the comparator is applied at terminal 7; voltages in the range from 1.5 to 6.0 volts are suitable for satisfactory circuit operation.

### Analog Timer for Long Delays

The very low input-bias-current characteristic of the super-beta transistors in the CA3095E is very desirable in the design of an analog timer for long time delays; the circuit shown in Fig. 13 is illustrative, and functions in a manner quite similar to that of the circuit of Fig. 12. Time delay can be varied in accordance with the expression shown in Fig. 13.

The timing cycle is initiated by momentarily closing the push-button switch to discharge timing capacitor C. At this instant, transistors $Q_1$ and $Q_3$ are non-conductive and $Q_2$ and $Q_4$ are conductive; this arrangement prevents conduction in transistors $Q_8$ and Q-PNP. Consequently, the output is essentially zero volts. Timing capacitor C is charged exponentially through resistor R until the voltage across the capacitor is sufficiently large to toggle transistor $Q_1$ and $Q_3$ into conduction (and $Q_2$ and $Q_4$ into non-conduction). Tran-

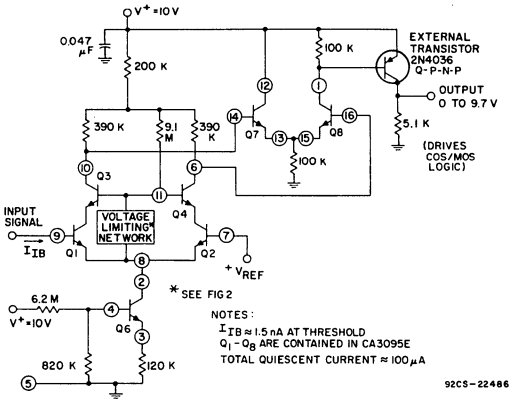



*Fig. 12 — Low-input-bias-current comparator circuit.*

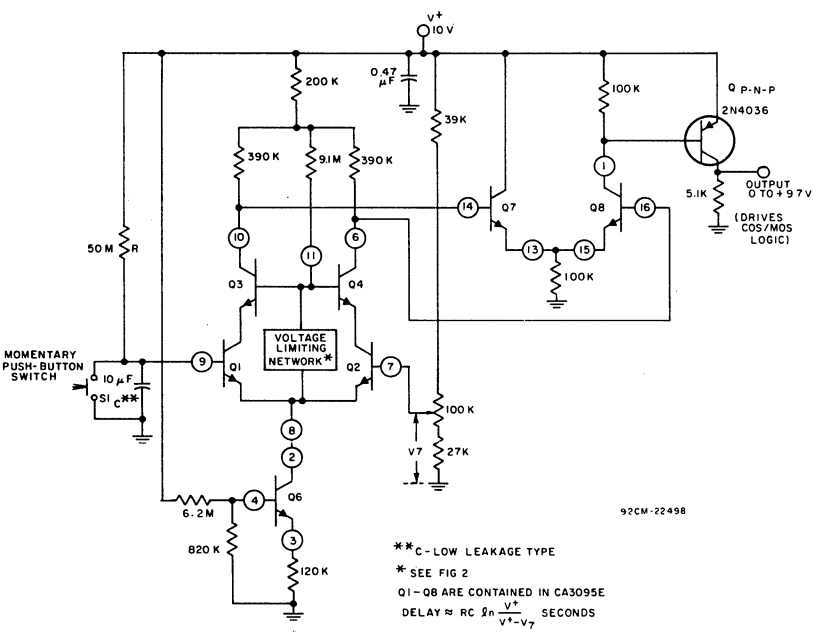



*Fig. 13 — Analog timer for long delays.*

sistors $Q_7$ and $Q_8$ are also switched so as to drive Q-PNP into conduction and produce a "high" output signal (approximately 9.7 volts). With the values shown, the time delay can be varied over the range from about 90 to 725 seconds, depending on the setting of the 100-kilohm potentiometer. The leakage-current loading on timing capacitor C due to transistor $Q_1$ is quite small, and is only of second-order importance in determining timing accuracy.

### Super-Beta Transistors in Preamplifier Applications

The wide operating-current range and circuit-connection flexibility available in the super-beta transistors contained in the CA3095E offer numerous advantages for applications in preamplifiers. For example, these transistors can be simply connected as a preamplifier for many of the common, economy-type op-amps (e.g., CA741, CA748)[3] The combination of the CA3095E and one of these op-amps provides an op-amp with the superior input characteristics offered by some of the high-priced op-amps that use super-beta transistors in their input stages. The CA3095E in conjunction with "commodity-class" op-amps can provide an over-all circuit exhibiting orders-of-magnitude improvement over the op-amp itself in terms of input impedance, noise, and the effects of error currents. Several circuit combinations of this type are described below.

Mention has already been made of the low-noise performance which can be achieved with the super-beta transistors in the CA3095E. This attribute is a requisite for preamplifiers operating with low-level signal outputs from sources such as tape heads and magnetic phonograph cartridges. The circuits described below illustrate the simplicity with which super-beta transistor circuits using the CA3095E can be equalized to meet the requirements for NAB playback and RIAA phonograph-record reproduction.

**Unity-Gain Preamplifier.** The circuit in Fig. 14 illustrates a unity-gain preamplifier using the transistors in the CA3095E to drive a CA741 op-amp. This circuit boosts the input impedance, $Z_{id}$, of the op-amp to the order of 20 megohms, typical. Transistors $Q_1$ - $Q_3$ and $Q_2$ - $Q_4$ operate as a differential-cascode amplifier with transistor $Q_8$ as their constant-current source. Transistors $Q_6$ and $Q_7$ are diode-connected to establish dc levels which are appropriate for direct connection to the CA741 input terminals. No additional external compensation is required with this circuit because the unity voltage gain provided by the preamplifier precedes the internally compensated CA741 op-amp. The resultant offset voltage of the combination circuit is the algebraic sum of the offsets due to $Q_1$, $Q_7$ vs $Q_2$, $Q_6$, and the offset due to the CA741. The resultant offset can be nulled at the normal nulling terminals on the CA741. This circuit is ideal for amplification of signals emanating from sources with very high impedances.

**High-Gain Preamplifier** The circuit in Fig. 15 shows a high-gain preamplifier using the transistors in the CA3095E to drive a CA748 op-amp. Transistors $Q_1$ - $Q_3$, and $Q_2$ - $Q_4$ operate as a differential-cascode amplifier with transistor $Q_8$ as their constant-current source. Transistor $Q_7$ is diode-connected to drop the dc common-mode voltage at the input of the CA741 to within its linear operating range.

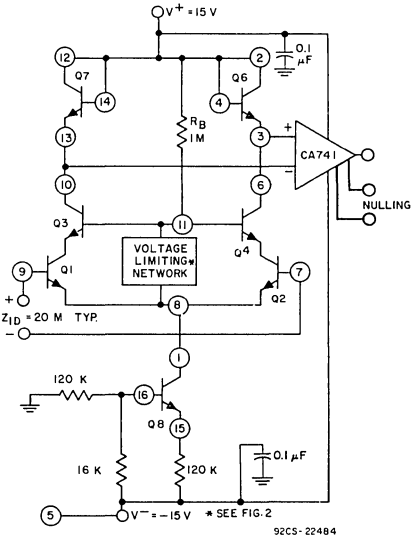



*Fig. 14 – Op-amp with unity gain preamplifier.*

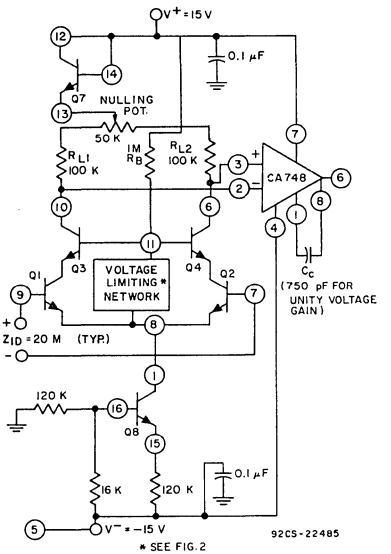



*Fig. 15 – Op-amp with high-gain preamplifier.*

This circuit boosts the input impedance, $Z_{id}$, of the op-amp to the order of 20 megohms, typical. It also can capitalize on the low-noise operational capability of the CA3095E, and reduces the noise (and offset-voltage) contributions of the CA748 by an increment equal to the gain of the preamplifier, typically about 28 dB with the circuit constants shown. In this case, external compensation of the CA748 may be necessary when the over-all op-amp is connected with feedback.

The approximate value of the compensation capacitor required can be computed by use of the following relationship:

$$C_c \text{ (in pF)} = \frac{30 \text{ X the voltage gain of the preamp}}{\text{closed-loop voltage gain of the composite op-amp}}$$

The circuits in Fig. 16 illustrate applications utilizing the superior input characteristics of super-beta op-amps. A circuit such as the one shown in Fig. 16(a) is useful in applications where input impedances in the order of 150 megohms are required at frequencies up to 5 kHz. Since input bias currents are required to flow through 10-megohm resistors in this circuit, it is mandatory that the input stage exhibit both low bias current and very low input offset current. (The capacitive reactance of the coupling capacitor C must be much lower than 5 megohms to achieve the high-input-impedance characteristic described above.) The low-drift, long-time-constant integrator circuit shown in Fig. 16(b) is another excellent application for the CA3095E super-beta transistor array. Because exceedingly low input bias currents permit the use of a high-value integrating resistor, R, without introducing substantial error, long-time-constant integration can be accomplished. The low input-offset-voltage drift characteristic of the super-beta transistors also contributes to low-error performance. Further reductions in error effects, particularly with temperature variation, can be achieved by using a temperature compensated bias-current source (e.g., $R_1$–$R_3$, $D_1$). In the circuit of Fig.15, such an arrangement could be implemented by using $Q_6$ in a diode connected fashion to serve as $D_1$. With such an arrangement, temperature-compensated bias current is applied to the inverting input terminal.

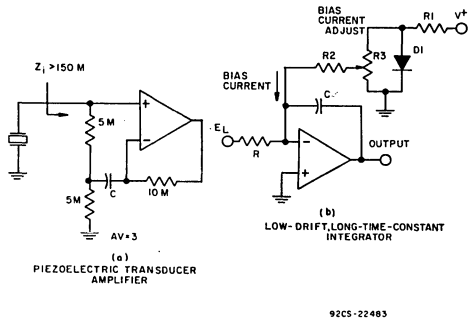



*Fig. 16 – Typical super-beta op-amp applications: (a) piezoelectric transducer amplifier (b) low-drift, long-time-constant integrator.*

### High-Input-Impedance DC-Voltmeter Circuit

The combination of a preamplifier circuit using the CA3095E in conjunction with a CA748 op-amp as described above is adaptable to dc-voltmeter circuits requiring high input impedance, as illustrated by the circuit of Fig. 17. An appropriate resistor-divider network is provided to develop a dc input signal at terminal 9 of the CA3095E with transistors $Q_1$ - $Q_3$ and $Q_2$ - $Q_4$ connected in the differential-cascode arrangement. Biasing and dc feedback are applied at terminal 7 of the CA3095E through a 10-megohm resistor. The CA748 op-amp drives a 200-microampere meter calibrated in terms of the voltages to be measured. A full-scale reading occurs when the voltage applied to pin 9 is 500 millivolts dc. The entire circuit is nulled with the 500-kilohm zero-adjustment potentiometer. The total power-supply requirement is only 6 volts with a supply current of only 300 microamperes; this requirement can be met with batteries. The input impedance of this simple circuit is approximately 40 megohms on all scales.

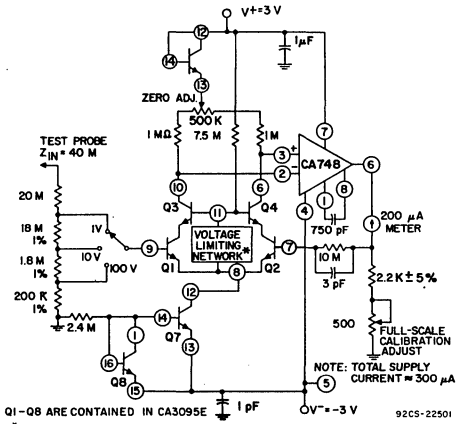



*Fig. 17 – Typical high-input-impedance dc-voltmeter circuit.*

### Preamplifier for Tape-Head Signals

The exceptional low-noise characteristics of the CA3095E make it suitable for preamplifier service in professional-grade tape-playback systems. A typical circuit with equalization for NAB standards (7.5 in/s) is shown in Fig. 18. Transistors $Q_1$ and $Q_3$ are cascode-connected as the input stage, and transistor $Q_6$ is connected as a common-emitter post-amplifier. Transistors $Q_2$ and $Q_4$ are non-conductive because the emitter-base junction in $Q_2$ and the base-collector junction in $Q_4$ are shunted by external wiring. Equalization for the NAB tape-playback, frequency-response characteristics is provided by the $R_1$, $C_1$, $C_2$ network connected in the ac feedback path; DC feedback stabilization is provided by the path through resistor

$R_2$. The amplifier has an over-all gain of about 37 db at 1 kHz, and can deliver output voltages in the order of 25 volts, peak-to-peak. The circuit configuration of Fig.18 is preferred to the differential-amplifier configuration because it limits the input-noise contribution to that of a single transistor (e.g., $Q_1$).

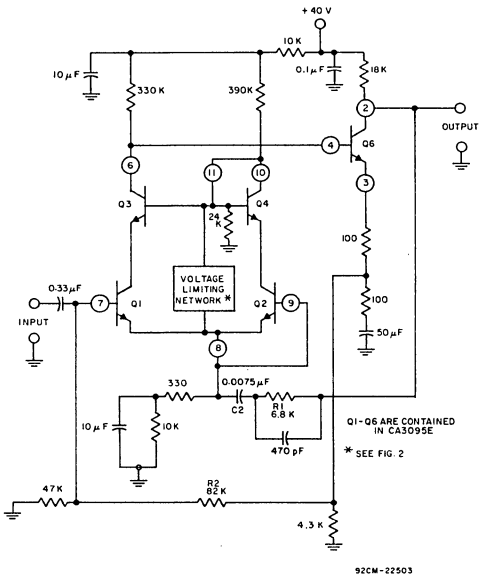



*Fig. 18 – Tape play-back preamplifier equalized for NAB standards (7.5 in/s).*

**Preamplifier for Signals from Magnetic-Phonograph Cartridges**

The exceptional low-noise characteristics of the CA3095E are also of great use in preamplifier service in equipment used to reproduce signals from magnetic phonograph cartridges. A typical circuit for this application with equalization for RIAA playback standards is shown in Fig. 19. Transistors $Q_1$ and $Q_3$ are cascode-connected as the input stage, and transistor $Q_6$ is connected as a common-emitter post-amplifier. Transistor $Q_2$ and $Q_4$ are non-conductive because the emitter-base junction in $Q_2$ and the base-collector junction in $Q_4$ are shunted by external wiring. Equalization for the RIAA phonograph-frequency-response characteristics is provided by the $R_1$, $C_1$ network connected in the ac feedback path. DC feedback stabilization is provided by the path through resistor $R_2$. The amplifier has an over-all gain of about 40 dB at 1 Hz, and can deliver output voltages in the order of 25 volts, peak-to-peak. The dynamic range of these circuits is typically about 95 dB with the gains indicated.

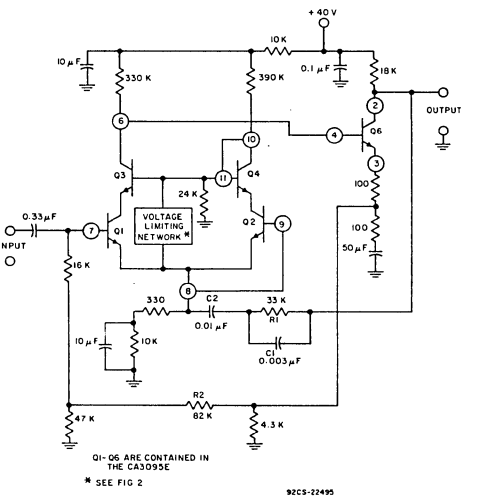



*Fig. 19 – Preamplifier equalized for RIAA standards applicable to magnetic phonograph catridges.*

**ACKNOWLEDGMENT**

The circuits of Figs. 18 and 19 were designed by L.A. Kaplan.

**REFERENCES**

1. "Super-Beta Transistor Array," CA3095E, RCA Data File No. 591.
2. "Measurement of Burst ("Popcorn") Noise in Linear Integrated Circuits," T. J. Robe, RCA Application Note ICAN-6732.
3. "Operational Amplifiers," RCA Data File No. 531.

RCA
Solid State
Division

# Application Note

# ICAN-6247

# Application of the CA3126Q Chroma-Processing IC Using Sample-and-Hold Circuit Techniques

This Note* describes the CA3126Q monolithic integrated circuit intended for use in processing the chrominance signal in a color television receiver. In performing the functions of color subcarrier regeneration and chroma control, emphasis has been placed on utilizing all the information available in the signal so as to approach ultimate system performance capability, while at the same time substantially reducing the number of external components and adjustments.

As contrasted with prior state-of-the-art IC designs, sample-and-hold techniques are used in the phase detectors for the AFPC and the ACC-killer loops of the CA3126Q. The improved signal-to-dc unbalance attained thereby makes it possible to eliminate the adjustments conventionally used in those circuits. The only set-up adjustment is a trimmer capacitor to tune the crystal filter.

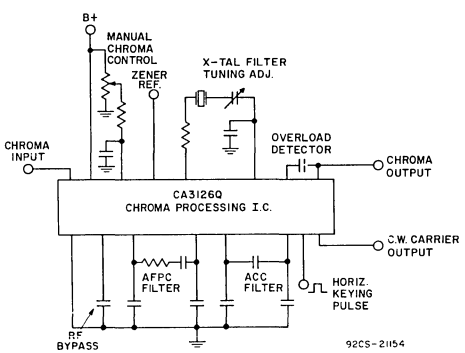



*Fig. 1– Components external to the CA3126Q.*

Two controls serve to adjust the chroma level: One control is automatic and functions as a supplementary ACC loop to prevent oversaturation under condition of improper transmitted burst-to-chrominance ratio, and under noisy-signal conditions. The second chroma level control is for manual adjustment of the saturation by the viewer. This control has a linear characteristic over the range of the chroma gain control.

The CA3126Q integrated circuit which performs these functions is housed in a 16-terminal package. The external components, shown in Fig. 1, are relatively few and consist of integration capacitors for the servo loops and the filter network in the VCO. Table I summarizes the performance of the circuit.

**Table I – Performance Data Typical Values**

| Function | Nom. Supply $V_{CC}$ = 11.2 V | Supply Var. $V_{CC}$ ±2 V | Temp. Var. ΔT = 50°C |
|---|---|---|---|
| **Oscillator Characteristic** | | | |
| C. W. Carrier Ampl. | 1 $V_{pp}$ | ±5% | + 10% |
| Frequency | Nom. Sub Carrier | ∓ 70 Hz | −70 Hz |
| **AFPC Characteristic** | | | |
| DC Loop Gain | 40 Hz/deg. | | |
| Pull-in Range | ±500 Hz | | |
| Phase Error | | ∓2° | −2° |
| Noise Bandwidth $f_{NN}$ | 100 Hz | | |
| **ACC and Killer Characteristic** | | | |
| 100% Input Level (Red Field) | 0.25 $V_{pp}$ | | |
| Nominal Output with Overload Detector | 0.5 $V_{pp}$ | ±2.5% | −5% |
| Nominal Output without Overload Detector | 2.7 $V_{pp}$ | ±10% | −5% |
| ACC–3 dB Point | 20% $E_{IN}$ | | |
| Killer Threshold | 5% $E_{IN}$ | | |
| Diff. Phase Error Over Entire ACC Range | 1° | | |
| **Manual Control Characteristic** | | | |
| Chroma Output Linearly Proportional to Control Bias | | | |
| Diff. Phase Shift with Bias Var. | 2° | | |

* This Note, revised by Wayne Austin (RCA Solid State Division) was originally prepared by L. A. Harwood (Consumer Electronics Division) for publication in the IEEE TRANSACTIONS ON BROADCAST AND TV RECEIVERS, May 1973, Vol. BTR-19, No. 2.

## MAJOR FUNCTIONS

The signal flow and organization of the CA3126Q are shown in block form in Fig. 2. The composite chroma signal is applied to the first chroma amplifier. The output from this stage proceeds along three paths. The first path leads to the doubly-balanced wide-band AFPC detector. Here the burst signal is compared with the reference carrier to produce the required error signal for synchronization. Two sample-and-hold circuits serve to achieve high detection efficiency and bias stability. One sample-and-hold circuit samples the detected signal during the horizontal keying interval and stores the peak error signal in a filter capacitor. A second similar circuit provides an accurate reference potential as described later. The bias stability of this system is sufficient to eliminate the need for the adjustments required in conventional circuit design.

The detected and filtered burst signal controls the frequency and phase of a voltage-controlled oscillator (VCO) by operating on an electronic phase-shifter. The VCO consists of an amplifier-limiter followed by the electronic phase-shifter. A crystal filter located between the output of the phase-shifter and the input of the amplifier-limiter closes the loop of the VCO. The filtered oscillator signal is amplified to produce the required reference carriers for the AFPC and ACC synchronous detectors. The required quadrature relationship is obtained by $+\pi/4$ and $-\pi/4$ radian integrated phase-shift networks.

The ACC-killer detector is similar in structure to the AFPC detector, and is also driven from the first chroma amplifier stage. It detects synchronously the in-phase component of the burst signal and produces a pulse signal proportional in amplitude to the level of the burst signal. The resulting control signal passes through a sampling circuit, as described above, and is applied to the killer and ACC amplifiers. The action of both amplifiers is delayed so that the unkill action takes place prior to ACC and the latter is fully activated upon reaching the predetermined burst level. The ACC amplifier controls the gain of the first chroma amplifier so as to maintain the burst signal constant while the killer amplifier enables the output stage in the presence of the burst signal.

The signal level to the second chroma amplifier is reduced to one fourth of the available signal level to allow for the extremes of the chroma signal excursions. A horizontal rate keyer operating on this stage removes the burst signal so that the output stage is activated only during the horizontal scanning interval. A saturation control, available for front panel control, allows a continuous gain adjustment of this amplifier. A desirable feature of this control is the linear correspondence between the control bias and the chroma output signal. The chroma maximum level corresponds to the maximum bias potential without a dead spot at the extreme of the control range. A threshold type overload detector monitors the output signal and maintains the output from the second chroma amplifier below an arbitrarily set level. This prevents the overload of the picture tube usually experienced on noisy or excessively large chroma signals. The required keying signals for the various functions are generated by two cascaded keyer stages where either polarity pulses are generated.

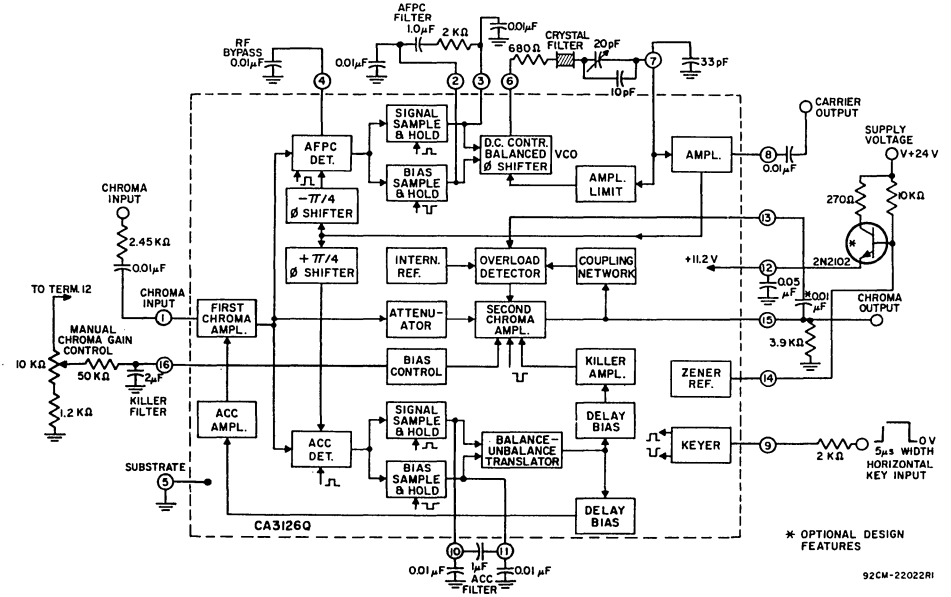



*Fig. 2— Signal flow and organization of the CA3126Q.*

## REGENERATION OF THE SUBCARRIER

The regeneration of the subcarrier is performed in the circuit shown in Fig. 3. This section consists of a synchronous phase detector, the sample-and-hold circuits, and a voltage-controlled oscillator. Several keying circuits serve to maintain the operation in proper time sequence.

### The Phase Detector

The phase detector is formed by transistors $Q_{51}$, $Q_{52}$ and $Q_5$ to $Q_{10}$. The composite chroma signal amplified by the first chroma amplifier is applied to transistors $Q_7$ and $Q_8$ and the reference carrier is applied to transistors $Q_9$ and $Q_{52}$. The product of the two signals is developed across the load resistor $R_{13}$. Transistors $Q_5$ and $Q_6$, triggered by a horizontal rate keyer circuit, operate on the phase detector so as to allow detection of the burst signal only. The current compensation of transistors $Q_7$ and $Q_8$ by the gating transistors $Q_5$ and $Q_6$ and the absence of filtering at the output of the detector results in transient-free switching of the phase detector. In the absence of chrominance, the potential across the load resistor $R_{13}$ remains constant regardless of the keying. In the presence of the chrominance signal, the phase detector produces two time-spaced outputs: one during the horizontal scanning interval corresponding to the quiescent potential, the second during the horizontal keying interval representing the detected burst. Thus, the detected burst can be measured relative to the quiescent potential rather than to an arbitrary reference. This results in excellent stability for temperature and supply variations.

### Sample-and-Hold Circuits

As previously stated, the sample-and-hold circuits shown in Fig. 3 allow efficient utilization of the detected error signal and provide a reliable reference potential. During the sampling interval, the detected pulse signal available at the detector load resistor $R_{13}$ is translated to the AFPC filter capacitor of terminal 2 via transistors $Q_{53}$ and $Q_{54}$. $Q_{53}$ serves to isolate the detector from the switching pulses generated in the sampling circuits. The sample-and-hold action is accomplished by controlling the conduction current in transistor $Q_{54}$ thus alternating the charge path during those intervals. During the sampling interval, transistor $Q_{54}$ conducts and its emitter exhibits a relatively low impedance in comparison with the value of the integrated charging resistor $R_{20}$. The detected or sampled signal is stored in the AFPC filter capacitor which, with $R_{20}$, determines the time constant during this time interval. During the hold period, transistor $Q_{54}$ is off and the filter time constant is several orders of magnitude larger than previously. The discharge of the filter capacitor is reduced to very small base bias currents only and little of the stored information is lost.

The "on" and "off" condition of the transistor $Q_{54}$ is determined by the state of the transistor-pair $Q_{11}$ and $Q_{12}$. During the "on" (sampling) interval, a signal from the horizontal rate keyer disables transistor $Q_{11}$ and the collector current of the transistor $Q_{12}$ maintains the transistor $Q_{54}$ in the "on" condition. During the "off" (hold) period, transistors $Q_{11}$ and $Q_{12}$ change their states and the transistor $Q_{54}$ is "off".

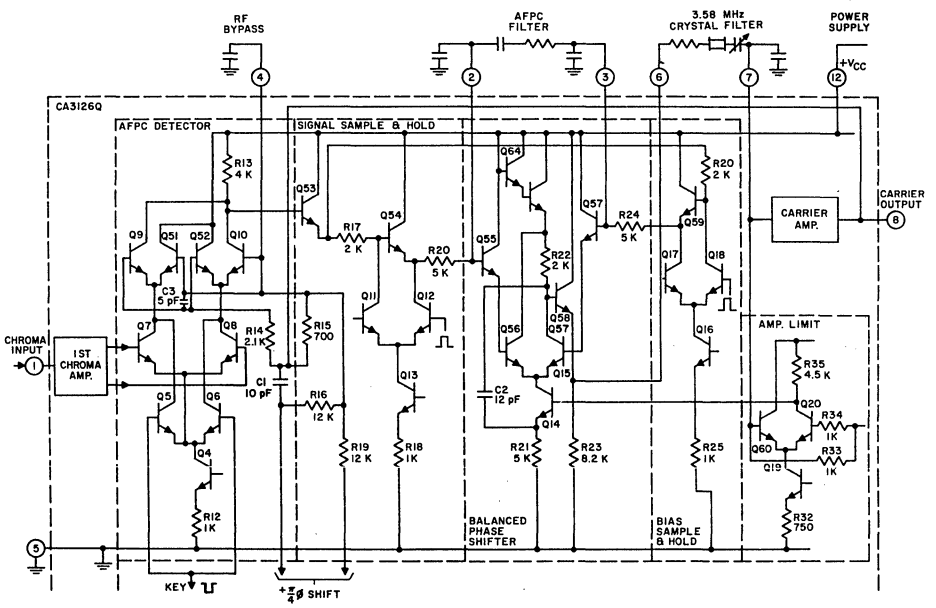



*Fig. 3– Subcarrier regeneration circuit.*

The bias sample-and-hold circuit, similar in structure to the above-described circuit, consists of the sampling switch $Q_{59}$ and the transistor-pair $Q_{17}$ and $Q_{18}$. This circuit, also activated by a signal from a horizontal rate keyer, samples the quiescent potential of the phase detector. The two signals, the error and the bias, processed by the sampling circuits, are stored in filter capacitors, and are applied to opposite terminals of a differential phase control. The phase control circuit synchronizes the reference carrier produced by the VCO.

Depending on the free-running frequency of the VCO, the detected signal is in the form of positive or negative going pulse trains which are then stored in a filter capacitor. The sampling switch has equal drive capabilities for both polarities of the signal; a requirement of particular importance in the presence of noise signals. Non-linear operation of the detector and sampling circuit would produce a rectified dc component causing an erroneous detuning of the VCO.

### The VCO Loop

The amplification and amplitude limiting of the oscillator signal takes place in the amplifier-limiter formed by the transistor-pair $Q_{60}$ and $Q_{20}$. The output from $Q_{20}$ is fed to the dc controlled phase-shifter and returns to the amplifier through a crystal filter. The amplifier operates in a non-inverting mode, hence, the total phase shift through the phase-shifter plus crystal filter must be a multiple of $2\pi$ radians. The crystal filter is tuned to the subcarrier frequency and the filter band-width is determined by a resistor in series with the crystal. The DC controlled phase-shifter has a phase range of approximately $\pm \frac{\pi}{4}$ radians, and a phase change activated by a control signal results in a corresponding oscillator frequency change.

In the phase-shifter, the oscillator signal available at the collector of $Q_{20}$ is applied to the base of $Q_{14}$ from which it proceeds along two paths. An integrated capacitor $C_2$ couples this signal from the emitter of $Q_{14}$ to the collector load of $Q_{15}$ and, at this point, the signal is phase-shifted by approximately $\pi/4$ radians. In the second path, the signal arriving at the collector of $Q_{15}$ passes through a current splitter formed by the transistor-pair $Q_{56}$, $Q_{15}$. This signal is reduced to a level determined by the control voltage at the bases of transistors $Q_{56}$ and $Q_{15}$. At one extreme, transistor $Q_{15}$ is OFF and the signal at the collector of $Q_{15}$ arrives through the capacitor $C_2$ only. Conversely, with transistor $Q_{15}$ ON, and $Q_{56}$ OFF, the signal arriving through the transistor $Q_{15}$ is phase-oriented so that the resultant signal has a phase of $+3/4\ \pi$ radians. The phase-control is linear throughout most of the control range.

A buffer amplifier is used to supply the CW carrier required for the demodulators, and the carrier is available at terminal 8. Internally, the buffer amplifier supplies the two synchronous detectors. Two R-C phase-shifters fed from the buffer amplifier provide the required phase orientation. A low-pass $R_{14}$-$C_3$ filter shifts the carrier to the AFPC detector by $-\pi/4$ while a high-pass filter provides a $+\pi/4$ oriented carrier for the ACC-killer detector.

## AMPLITUDE CONTROL OF THE CHROMINANCE SIGNAL

Two cascaded amplifier stages serve to process the chroma signal and several signals are developed to control the gain of each stage.

### First Chroma Amplifier and ACC Servo Loop

The first chroma amplifier, shown in Fig. 4, is controlled by the burst responsive ACC-killer detector only. The amplifier formed by the transistor-pair $Q_1$, $Q_2$ is driven single-ended by the applied composite chroma signal. The amplified output from this stage drives differentially the synchronous ACC-killer detector. The gain of the first amplifier is a function of the dc emitter current supplied by the constant current source $Q_3$. This current source is biased to provide a nominal current and, hence, a nominal gain in the first amplifier stage. The bias of the current source is reduced in response to a detected burst signal and the gain of the first stage diminishes correspondingly.

The ACC-killer detector is similar in structure to the AFPC detector. However, the CW carrier applied to the detector is in phase with the burst signal. The detected burst signal is processed by a sampling circuit in the same manner as previously described in connection with the AFPC circuit. The signal sampling consists of the transistor follower $Q_{73}$ and the keyed transistor-pair $Q_{40}$, $Q_{41}$. Resistor $R_{63}$ serves to produce an intentional dc offset across the inputs of the differential pair $Q_{43}$, $Q_{76}$. The detected ACC signal is unipolar with respect to the reference potential; thus, the dc offset extends the linear operating range of the amplifier $Q_{43}$, $Q_{76}$. The bias sampling circuit consisting of transistors $Q_{79}$, $Q_{44}$, $Q_{45}$ applies the quiescent bias to the base of transistor $Q_{76}$. In the absence of a burst signal, the dc offset maintains transistor $Q_{43}$ in the OFF condition and the following p-n-p transistor, $Q_{29}$, is also disabled. Thus, the ACC amplifier $Q_{28}$ is non-conducting and the current source $Q_3$ provides the maximum current to the input stage.

The OFF state of transistor $Q_{29}$ renders the killer amplifier (transistor $Q_{27}$) inoperative, a condition required to disable the second chroma stage.

Upon amplification of the burst signal in the first chroma amplifier, the detected burst signal increases proportionately to the amplitude of the input signal and combines differentially with the previously described bias signal in the collector load of transistor $Q_{43}$. Prior to it, the detected and bias signals are smoothed by the ACC filter capacitors. The linear operation of the chroma amplifier, the detector, and the amplifier which follows the sampling circuits is maintained to a signal level sufficient to enable the transistor $Q_{28}$. This potential, approximately 0.7 V, establishes the delay of the ACC charac-

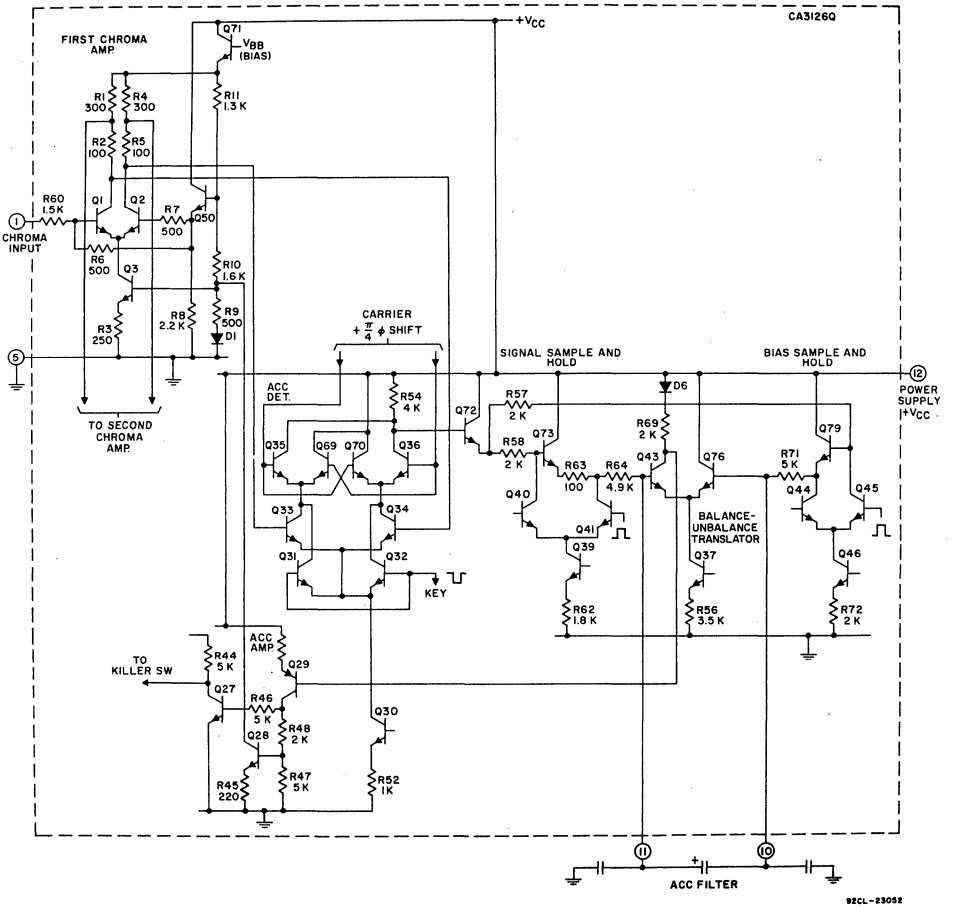



*Fig. 4— The first chroma amplifier and the ACC servo loop.*

teristic as shown in Fig. 5. The chroma (burst) signal at the output of the first stage remains essentially constant with further increase of the input signal. The increasing dc potential at the collector of $Q_{29}$ also activates the killer-amplifier $Q_{27}$. In order to maintain a predictable killer threshold, this action is referenced to the delay point of the ACC. As previously stated, the ACC begins to function at a signal level at which the dc potential across resistor $R_{47}$ reaches 0.7 V. The killer threshold is lower than that of the ACC action and is determined by the voltage drop across resistors $R_{48}$ and $R_{47}$. Thus, the two threshold signals are predictably established by the ratio $R_{47}/(R_{47} + R_{48})$.

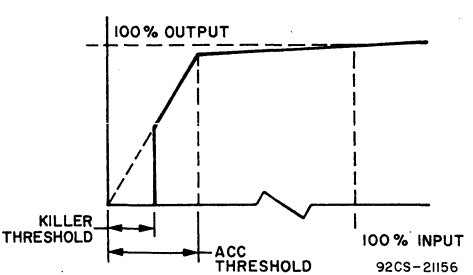



*Fig. 5— Normalized ACC characteristic.*

### The Second Chroma Amplifier

The operation of the second chroma amplifier is controlled simultaneously by several signals. As described previously, they are: a customer-operated chroma gain (saturation) control, the killer detector signal, the overload detector, and the keyer.

The amplifier circuit shown in Fig. 6 is formed by the transistor-pair $Q_{65}$, $Q_{24}$ and is driven differentially by the first chroma amplifier. The signal level to this stage is reduced by means of a resistive voltage divider. The amplifier $Q_{65}$,$Q_{24}$ is interrupted during the horizontal keying interval by the transistor-pair $Q_{66}$, $Q_{23}$ to remove the burst information from the composite signal. The gating transistors $Q_{66}$ and $Q_{23}$ are connected so that their emitters and collectors are in parallel with the respective emitters and collectors of transistors $Q_{65}$ and $Q_{24}$. The resulting collector current compensation maintains the quiescent output potential regardless of the keying operation.

The gain of the second chroma amplifier is adjusted by varying the current in the transistor $Q_{25}$. A resistive divider $R_{41}$,$R_{42}$ fed from a follower stage $Q_{67}$ provides the bias potential to the base of the transistor $Q_{25}$ and the voltage drop across resistor $R_{40}$ determines the current flowing from the collector of $Q_{25}$ to the emitters of $Q_{65}$ and $Q_{24}$. The diode $D_3$ compensates the base to emitter potential of the transistor $Q_{25}$.

Since the bias resistors $R_{40}$, $R_{41}$, and $R_{47}$, and also the amplifier load resistor $R_{43}$, are located on the same IC chip, the resistance ratio of these components is accurately controlled. Thus, the gain of the second chroma amplifier determined by these components is very predictable, and is a function of the bias potential applied to the base of transistor $Q_{67}$ only.

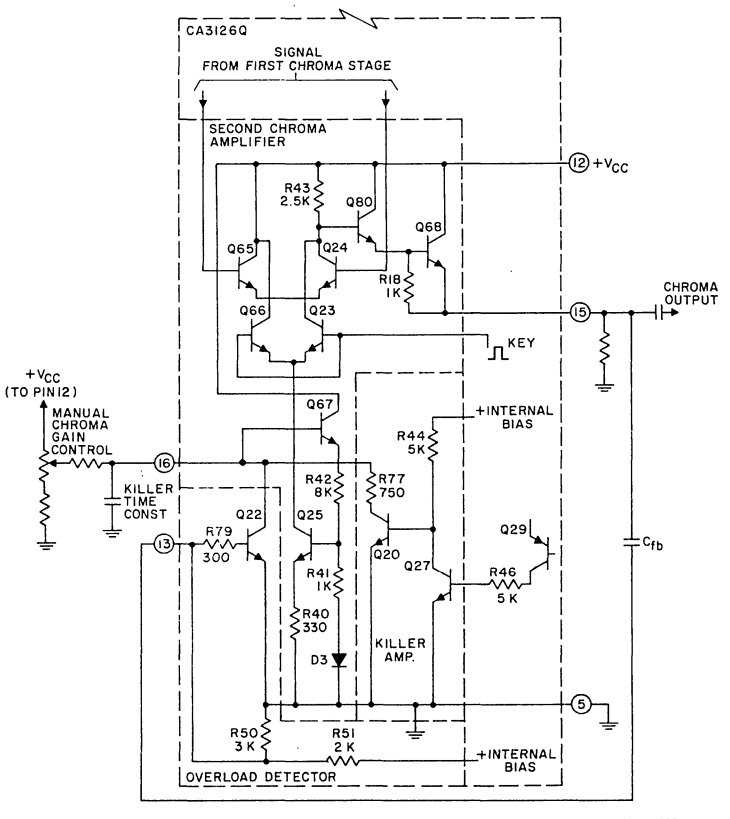



*Fig. 6— Chroma output stage.*

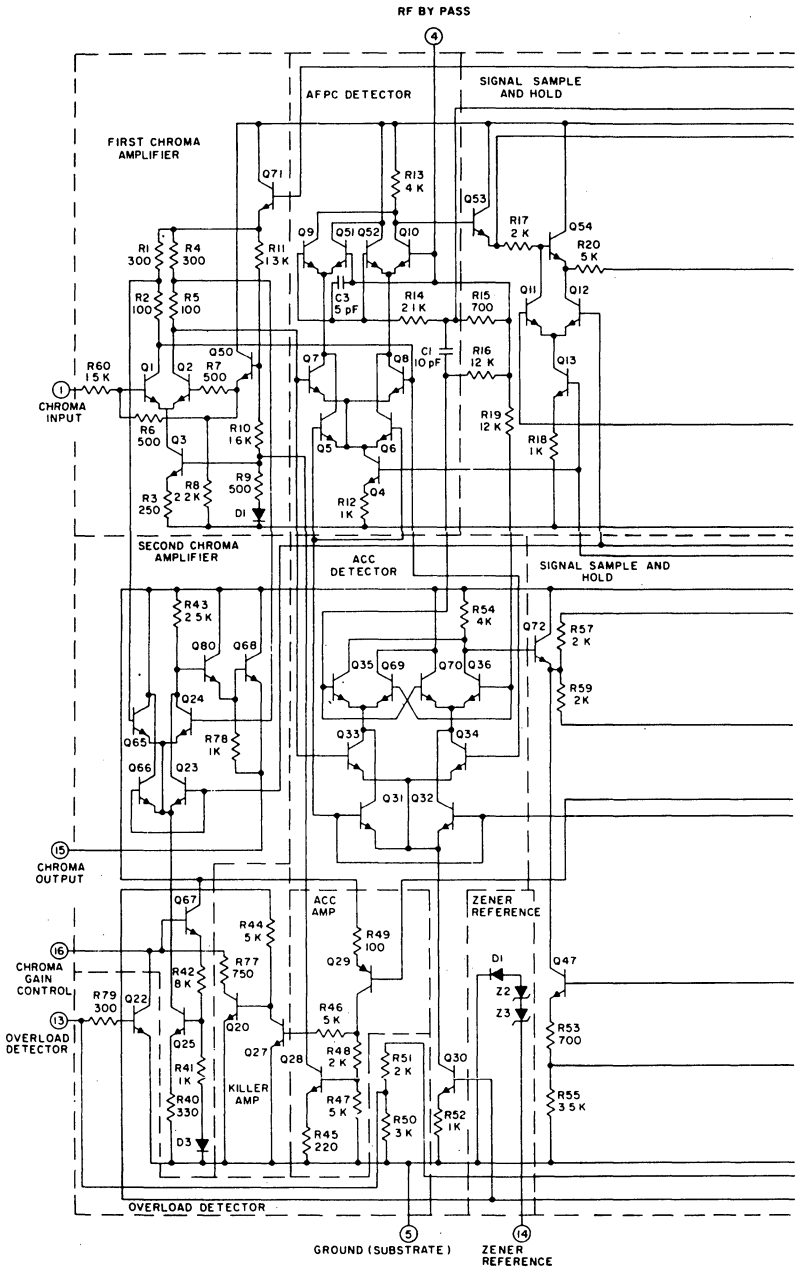



*Fig. 7—Complete circuit diagram showing details of the deying circuit and internal bias circuits.*

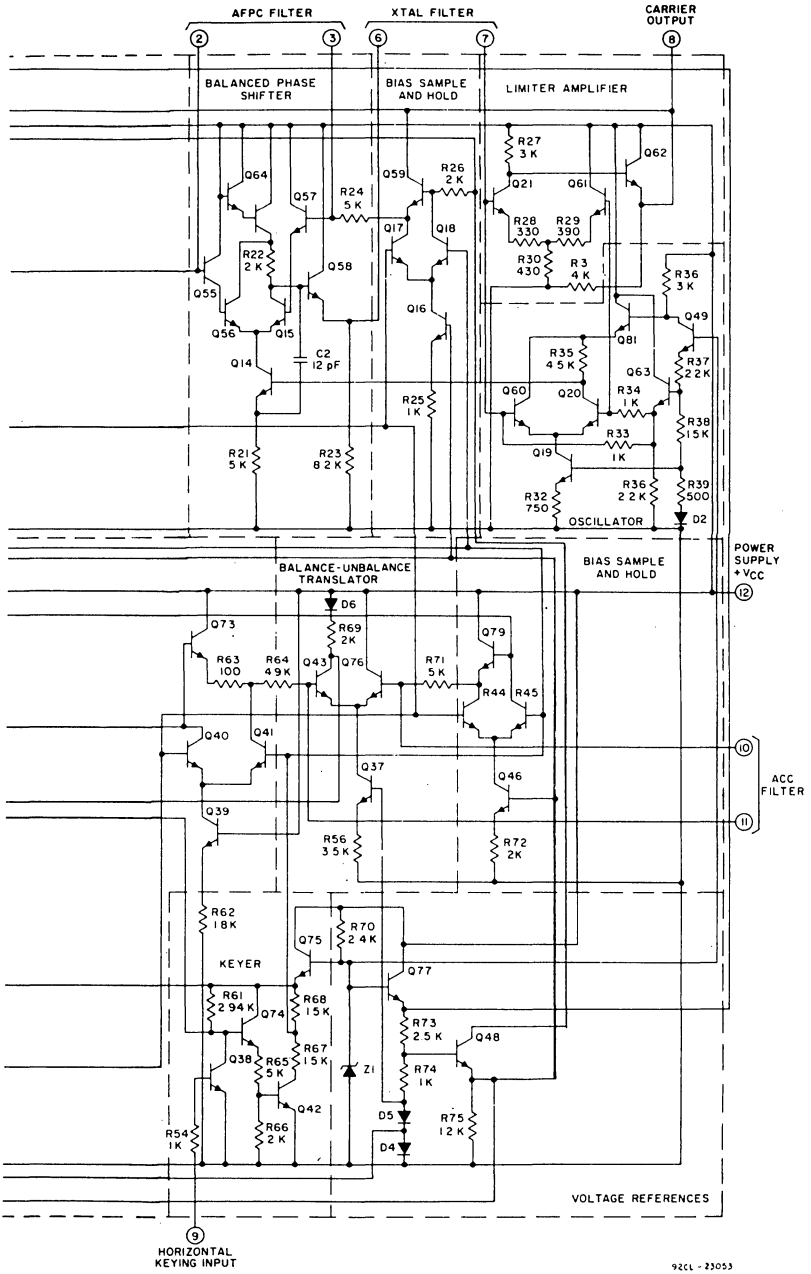



*Fig. 7—Complete circuit diagram showing details of the keying circuit and internal bias circuits.*

The interfacing of IC's with external control circuits usually presents problems due to the large tolerances associated with both components. The circuit used here overcomes these difficulties. The transistor follower $Q_{67}$ exhibits negligible loading on the bias set by the manual chroma control. Thus, the gain of the second chroma amplifier is uniquely determined by the rotation of the gain control potentiometer and is relatively independent of its resistance value.

The killer operation is also performed on the second chroma amplifier. The amplified output from the ACC-killer detector is applied to the killer switch $Q_{20}$. In the presence of a burst signal, transistor $Q_{20}$ is off and the chroma amplifier remains undisturbed. In the absence of a burst signal, the collector current in $Q_{20}$ reduces the potential on the base of the transistor $Q_{67}$ so as to cut off the second chroma amplifier.

### The Overload Detector

The ACC and the manually operated saturation control provide the essential means to maintain the proper chrominance level to the picture tube. Under certain conditions, however, the presence of the ACC is detrimental. As previously stated, the ACC servo loop maintains a constant output level of the burst signal regardless of the chroma information. Transmitter variations in burst-to-chroma ratios are improperly corrected by the ACC action and, on signals with low burst-to-chroma ratios, the excessively amplified chroma can exceed the dynamic range of the picture tube.

Similar overload problems are experienced when receiving weak signals. The Synchronous ACC detector produces a control signal proportional to the average value of the burst interval signal, and noise does not contribute to the output. Although this type of noise-immune detection is necessary for reliable operation of the killer circuits, it is less desirable for the ACC action because the noise-peaks plus signal tend to produce undesirable over-saturation effects.

The overload detector operating on the second chroma stage eliminates both these overload problems. The chroma signal from the output terminal of the second chroma amplifier is coupled, by means of the coupling capacitor $C_{fb}$ to overload detector $Q_{22}$. Transistor $Q_{22}$ is biased by means of an internal bias supply to 0.5 V, and remains off until its base potential is raised to approximately 0.7 V. Thus, detection takes place whenever the chroma signal plus dc bias is equal to or exceeds 0.7 V. The detected and filtered signal lowers the bias potential on the base of transistor $Q_{67}$ and reduces the gain of the output stage.

## KEYING CIRCUITS

Details of the keying circuit and of the internal bias circuits are shown in the complete diagram of the CA3126Q in Fig. 7. A positive horizontal rate keying pulse applied to terminal 9 activates the keying circuit. This circuit maintains the AFPC and ACC detectors, with the corresponding sample-and-hold circuit, in the ON position during the keying interval, and disables the chroma output stage at the same time.

## CONCLUSION

The new chroma processing circuit improves the performance of a color television receiver. The use of synchronous detection and sampling results in excellent signal stability and fewer external components and adjustments. An overload detector prevents over-saturation of the picture tube, and the improved manual control simplifies the adjustment of the chroma level.

# Application of the CA3089E FM-IF Subsystem

by L. S. Baar

The RCA-CA3089E, shown in Fig. 1, is an FM-IF subsystem intended for use in FM receiver applications. In addition to the amplifier-limiter and quadrature detector sections, the CA3089E provides such auxiliary functions as mute, AFC output, tuning-meter output, and delayed rf-AGC.[1] This Note briefly describes each circuit section and discusses practical aspects of designing with this device.

### Circuit Description

The three-stage direct-coupled amplifier-limiter uses a cascode input stage to reduce input noise and provide better stability. The peak-to-peak swing of approximately 300 millivolts is developed across the 390-ohm resistor, R31, at pin 8. The operating-point stability is provided by dc feedback to the input stage. The input voltage for an output 3 dB below limiting is typically 12 microvolts rms.

The detector is a doubly balanced circuit driven symmetrically by the output of the if amplifier. The voltage at pin 8 is coupled through a reactance to the tuned circuit at pin 9. The detector output is taken from both sides and combined differentially to produce an audio output and automatic-frequency-control voltage. The audio output may be attenuated by a current driving pin 5. The current is normally provided by the mute drive, which reduces the level by more than 50 dB. Fig. 2 shows the detector and audio-AFC translator circuits redrawn to illustrate the balanced circuitry. The audio output is developed across a 5,000-ohm resistor, R49, Fig. 1. The AFC output can be used either as a current or voltage source.

The meter output and rf-AGC circuits are driven by three level detectors which detect the output levels of each of the if amplifier stages. The tuning-meter circuit sums these levels and provides a voltage which is a function of the input signal. The rf-AGC circuit is driven by the level detector connected to the output of the first amplifier stage, which provides the delay. The mute logic output is developed from the output of the third limiter. With a large signal, the if envelope is detected, and drives the mute logic voltage low. As the signal-to-noise ratio deteriorates, "holes" are created in the envelope; these "holes" are detected, and provide the voltage to drive pin 5.

The bias supply maintains the device current drain virtually constant from a supply voltage of 16 volts to approximately 8 volts over a temperature range of −40°C to +100°C while maintaining the performance of the device virtually unchanged. The typical curves in Figs. 3 through 7 illustrate these characteristics. A reference voltage brought out to pin 10 may be used in conjunction with the AFC, if desired.

### Stability Considerations

Because the CA3089E is a very high gain device, the external circuit must be laid out carefully to eliminate or reduce any feedback path.[2] Fig. 8 shows a 10.7-MHz printed-circuit-board layout of the circuit in Fig. 9(a). The ground-plane layout was devised to prevent large rf currents at the output terminals from returning to the input grounds. Bypass-capacitor grounds also were selected to achieve the same purpose. It is recommended that bypass capacitors be placed on terminals of the auxiliary functions since most of them are connected to rectifier circuits which are not completely filtered within the device. Capacitors of the disc ceramic type with a 0.01- to 0.02-microfarad value are usually good bypass capacitors at 10.7 MHz. Larger values may exhibit a self-resonance below 10.7 MHz, and actually exhibit inductive reactance at their terminals. The nominal input impedance of the CA3089E is approximately 9,000 ohms, and it is not recommended that an impedance match be attempted. Most commercial receivers use ceramic-filter frequency-selective elements that normally have source impedances of 500 ohms or less. When these filters are properly terminated with loading resistors, the typical source impedance is further decreased to 250 ohms or less. Higher levels of source impedance are possible with very careful circuit layout; however, the maintenance of stability could be difficult.

The CA3089E has a frequency response that is typically flat to 20 MHz; consequently, the device can provide useful gain well above that frequency. If the device is used at lower frequencies, the larger-value bypass capacitors required may not be adequate to bypass the higher frequencies. Double bypassing with lower-value capacitors can overcome such a problem. Another means of alleviating the problem is to externally reduce the frequency response by using a small capacitance across the output load of the device.

### Quadrature-Detector Circuits

The quadrature-detector tuned circuit is connected between pins 9 and 10. The signal voltage at pin 8 is

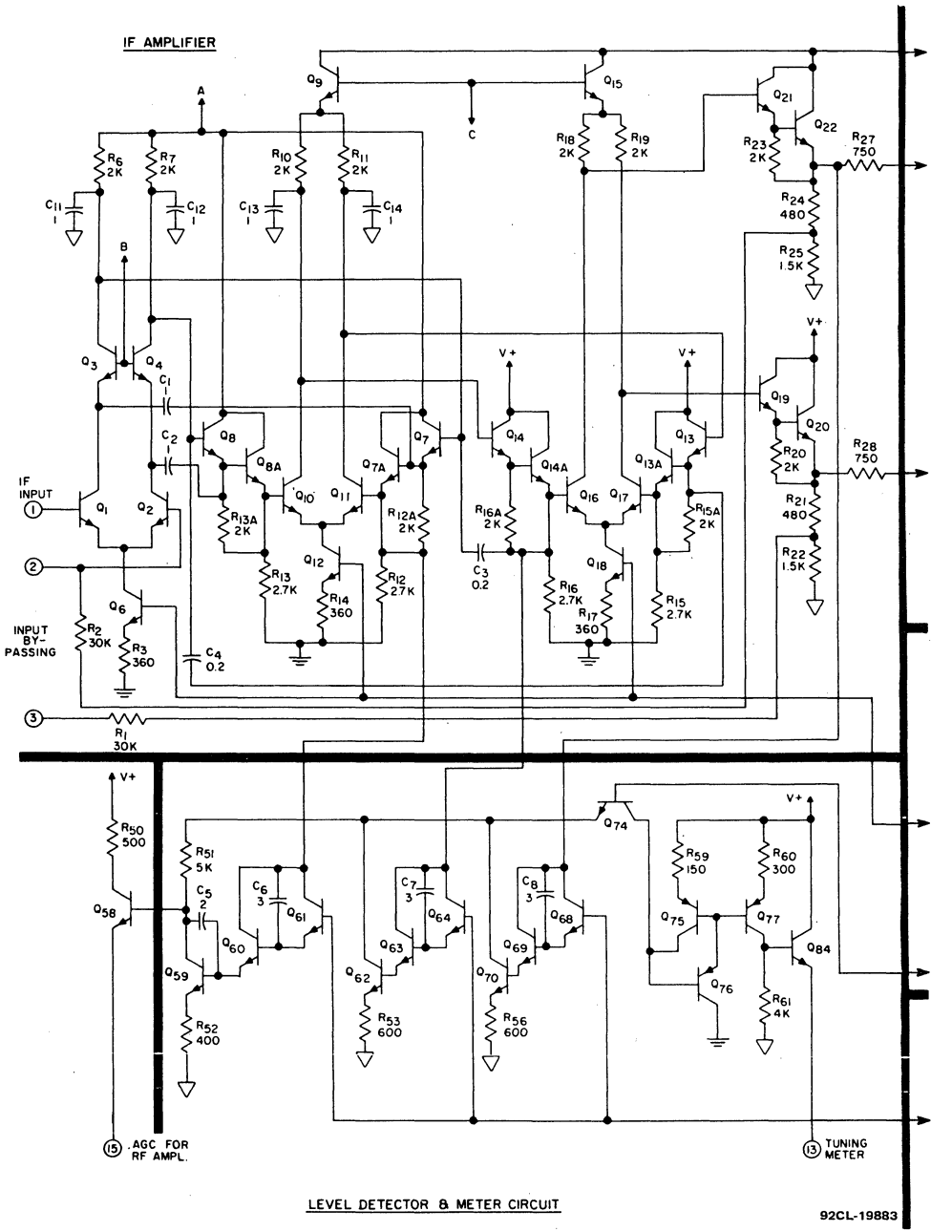



*Fig.1 – Schematic diagram of the CA3089E.*

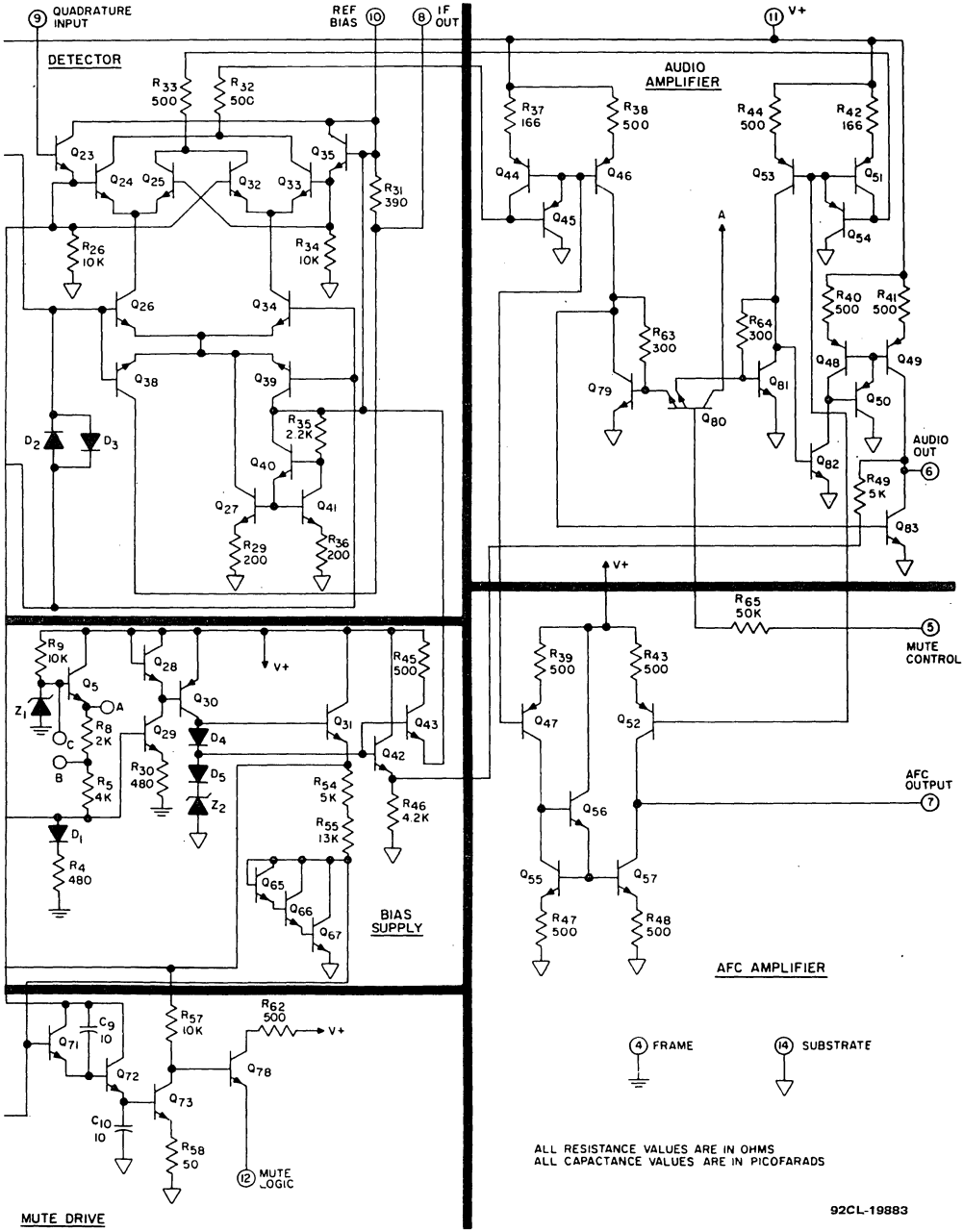



*Fig.1 – Schematic diagram of the CA3089E.*

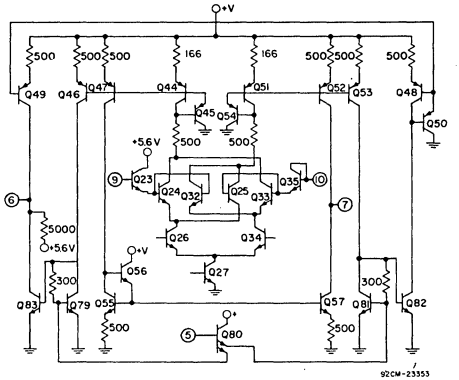



*Fig. 2— Detector, audio, and AFC circuits.*

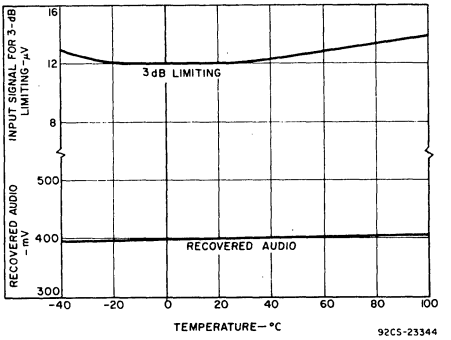



*Fig. 5— Input limiting and recovered audio as a function of temperature.*

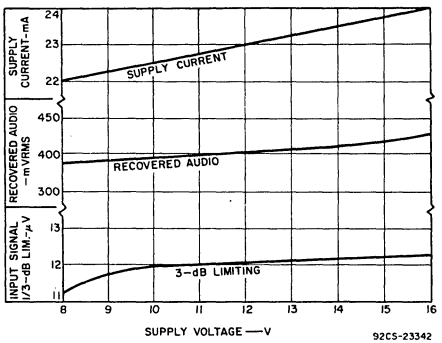



*Fig. 3— Supply current, recovered audio, and input limiting as a function of supply voltage.*

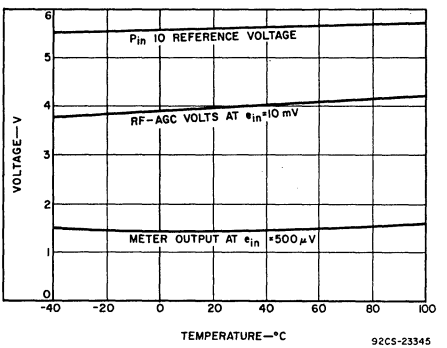



*Fig. 6— Reference voltage, rf-AGC, and meter output as a function of temperature.*

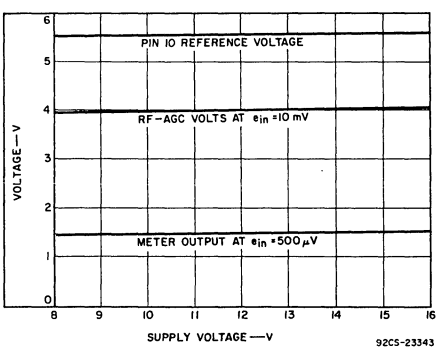



*Fig. 4— Reference voltage, rf-AGC, and meter output as a function of supply voltage.*

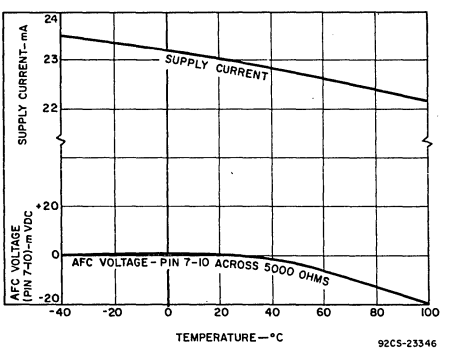
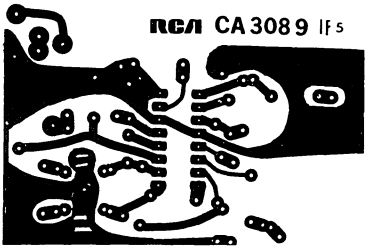
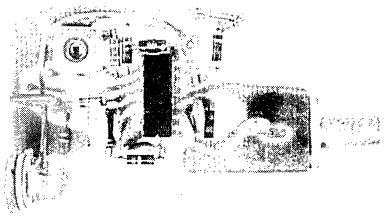



*Fig. 7— Supply current and AFC voltage as a function of temperature.*



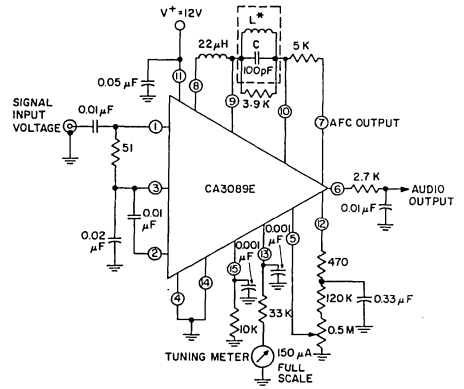

*a) Bottom view of printed-circuit board.*



*b) Component side – top view.*

*Fig. 8.—Actual-size photographs of the CA3089E and outboard components mounted on a printed circuit board.*

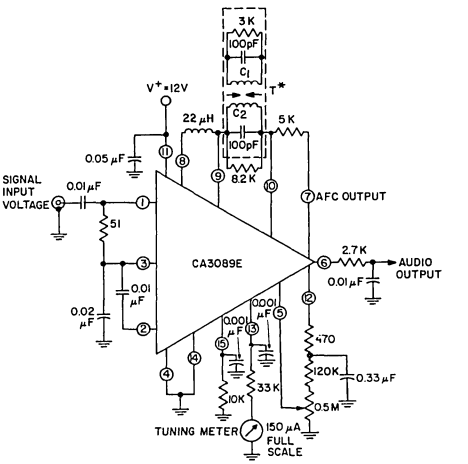
normally coupled to pin 9 through a choke. The circuit values for the detector network are determined by several factors, the primary one being distortion at a particular level of recovered audio. Distortion is determined by the phase linearity of the quadrature network and is not influenced by the device unless excessive, recovered audio overdrives the audio circuit. With a single tuned network, the phase linearity improves as the bandwidth increases; however, recovered audio decreases. A satisfactory compromise for most FM-receiver applications is reflected in the circuit of Fig. 9(a). This circuit typically provides 400 millivolts rms of recovered audio with less than 0.5-percent distortion. Because a double-tuned circuit has better phase linearity over a wider bandwidth, distortion figures of less than 0.1-percent are attainable with the network used in the circuit of Fig. 9(b). Proper alignment and coupling adjustment of the double-tuned circuit are most easily accomplished while viewing the resulting S curve. Initial adjustment of the primary tuning slug to the proper crossover is made with the secondary slug removed. The secondary tuning slug is then adjusted until a slight "ripple" is observed moving along the S curve. If the ripple is excessive (enough to distort the S curve) the coupling is too tight. If no ripple is observed, the coupling is too loose. As the ripple moves through the crossover point, it will be observed that the S curve becomes more linear near the center frequency. Slight readjustment of both slugs may be necessary for final alignment. The best performance can then be achieved by slight adjustment while measuring distortion. The coupling may be varied by either moving the coils or by changing the value of the secondary load resistor.




ALL RESISTANCE VALUES ARE IN OHMS
*L TUNES WITH 100 pF (C) AT 10.7 MHz
$Q_0$(UNLOADED)≅75 (G.I. AUTOMATIC MFG. DIV. EX22741 OR EQUIVALENT)

92CM-19040RI

(a)




ALL RESISTANCE VALUES ARE IN OHMS
*T: PRI.–$Q_0$(UNLOADED)≅75 (TUNES WITH 100 pF (C1) 20t OF 34e ON 7/32" DIA. FORM
SEC.–$Q_0$(UNLOADED)≅75 (TUNES WITH 100 pF (C2) 20t OF 34e ON 7/32" DIA. FORM
kQ (PER CENT OF CRITICAL COUPLING)≅70%
(ADJUSTED FOR COIL VOLTAGE $V_C$)=150 mV
ABOVE VALUES PERMIT PROPER OPERATION OF MUTE (SQUELCH) CIRCUIT
"E" TYPE SLUGS, SPACING 4 mm

92CM-19041RI

(b)

*Fig. 9– (a) Test circuit for the CA3089E using a single-tuned detector coil, (b) test circuit for the CA3089E using a double-tuned detector coil.*

Various circuit values can be used to obtain the same recovered audio, but the basic conditions of circuit bandwidth and phase linearity must be maintained. The detector circuit also sets up conditions which are required for proper operation of the mute circuit. The rf voltage on pin 9 must be held at approximately 175 millivolts rms, ±25 millivolts. The reason for this requirement is discussed subsequently in connection with the mute logic circuit. The approximate voltage at pin 9 is determined from the equivalent circuit shown in Fig. 10.

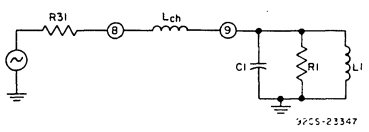



*Fig. 10—Equivalent circuit used to determine approximate voltage on pin 9 of the CA3089E in Fig. 9.*

The peak-to-peak voltage on pin 9 is:

$$|V_9| \cong |V_8| \frac{R1}{\omega L_{ch}}$$

where R1 is the total parallel resistance and V8 is approximately 300 millivolts, peak-to-peak.

The Q of the tuned circuit between pins 9 and 10 may be affected by the effective Q of the choke between pins 8 and 9 and the series resistor R31 in the CA3089E. All of the above factors should be considered in selecting circuit values. Table I lists some typical combinations of component values under various conditions.

A choke is normally selected to equalize delays in the signal path and in the limiter–quadrature path. It also reduces the if harmonic content across the quadrature circuit. In some cases, such as in narrow-band applications, it may become necessary to use a capacitor as the coupling component where large values of inductance with high Q's are difficult to obtain. If a capacitor is used, the phase of the recovered audio and AFC voltage will be reversed, some asymmetry of the S curve may result, and the distortion may be adversely affected to a small degree.

As indicated above, the inductance between pins 8 and 9 tends to equalize delays in the detector signal paths. The matching of elements of the IC in the balanced detector circuit results in an AFC output with a very small offset when referred to the voltage at pin 10. For most applications, the inherent offset variation is well within tolerances, and does not affect circuit performance. In some narrow-band applications, however, the offset becomes more critical because of the very narrow bandwidth. In such situations, the combination of normal production variations of the device and the external circuit components results in receiver detuning when the AFC loop is closed. This detuning results in an increased distortion of the recovered audio. This distortion can be corrected with the addition of a variable capacitor from pin 8 to ground to provide phase compensation. The capacitor can be adjusted to provide zero AFC offset with minimum distortion. Generally, the offset is in one direction for a given set of conditions. The addition of a fixed capacitor will minimize variations sufficiently to satisfy many applications. A value of 5 picofarads is an effective value for the circuit of Fig. 9(a) with the recommended PC-board layout. Conversely, the offset created by using a capacitor between pins 8 and 9, as mentioned earlier, may be compensated by placing an inductance between pins 8 and 10.

### Audio and AFC Circuits

The audio and AFC circuits are very similar, and both develop the same audio signal at their respective output terminals. The audio output voltage on pin 6 is developed across an internal, nominal, 5,000-ohm resistor (R49) connected to the 5.6-volt reference. In addition, the audio signal level can be attenuated by providing a direct current into pin 5 without any shift in its dc level. The audio output, as shown in Fig. 11, is uniform to a frequency of more than 1 MHz when measured in the circuit shown.

The AFC output at pin 7 is a current source and, if terminated with 5,000 ohms, will provide an audio output identical to that at pin 6. The AFC output may be referenced to a wide range of voltages, from near ground potential to near supply voltage. However, because of the balanced circuit configuration, the best AFC sensitivity and offset will occur at, or near, the 5.6-volt internal reference. An AFC voltage developed across a load tied back to pin 10 is recommended. As a consequence of this connection, variations in the AFC voltage as a function of operating voltage and temperature are minimized because the voltage on pin 7 tends to follow changes in the reference voltage.

### Mute Circuit

The signal to the mute logic circuit is taken from the emitter follower connected to pin 9. This signal drives a peak

**TABLE I – FIG. 10 COMPONENT VALUES AND CHARACTERISTICS AS A FUNCTION OF FREQUENCY**

| Freq. (Hz) | $L_1$ (H) | $QL_1$ | $C_1$ (pF) | R1 (ohms) | X (pin 8 to pin 9) | Deviation (kHz) | Recovered Audio (mV) |
|---|---|---|---|---|---|---|---|
| 10.7M | 2.2μ | 75 | 100 | 3900 | 22μH | ±75 | 400 |
| 10.7M | 2.2μ | 120 | 100 | | 120μH | ±5 | 280 |
| 10.7M | 2.2μ | 120 | 100 | | 1.3pF | ±5 | 290 |
| 455k | 0.1m | 65 | 100 | 68k | 1 mH | ±5 | 400 |

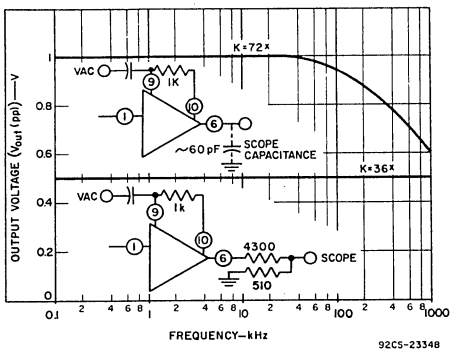



*Fig. 11—Audio response at pin 6.*

detector followed by an inverter such that the mute logic developed is zero volts with an input signal level sufficient to develop a fully limited output signal. As the input signal level is reduced below limiting, noise becomes significant, and creates "holes" in the if envelope. The detected drive voltage decreases and causes the mute logic voltage at pin 12 to increase. This voltage, in turn, is fed to pin 5 to provide the current to attenuate the audio. If the if level at pin 9 is too high, the "holes" created by the noise are insufficient to drive the mute logic voltage high enough to attenuate the audio. If the pin 9 voltage is too low, the mute drive voltage never reaches zero, and the external mute-threshold control behaves like a volume control. It is for this reason that the mute logic circuit requirements influence the selection of detector circuit values.

Another condition affecting proper mute performance is excessive gain in the tuner or preceding if stages. High gain ahead of the CA3089E under a condition of low signal-to-noise ratio results in the noise being clipped by the limiting amplifiers. The clipping has the effect of reducing the number of "holes" in the if envelope, and limits the mute drive voltage at pin 12 to values insufficient to attenuate the audio. If high gain is a system requirement, an externally derived mute logic voltage is necessary to drive pin 5.

The external circuit on pin 12 in Fig. 9(a) serves to filter the output, and provides a variable potential for mute-threshold adjustment. The 470-ohm resistor in series with pin 12 reduces the effective Q of the filter capacitor and prevents the circuit from setting up on noise current transients as the mute circuit begins to function. The voltage divider, composed of the 500 kilohm potentiometer and 120 kilohm resistor, controls the threshold point. These values are suggested ones, and may be altered to suit the user. Curve A in Fig. 12 shows the change in audio output level as a function of input signal with the mute-threshold control circuit (also shown in Fig. 12) at its maximum-voltage setting. Because of the more shallow slope and the larger circuit time constant involved, a "soft" mute action results. Curves B and C illustrate the change in the curves resulting from adjustment of the values of the threshold control circuit. These latter circuits provide a faster acting mute. The fixed resistor, R1, in addition to controlling the slope of the mute characteristic, limits the voltage appearing at pin 5. The use of this resistor is recommended to prevent a latch-up at the attenuating circuit, which, if it occurs, maintains the circuit in muted condition until the supply voltage is removed.

The curves in Fig. 12 show that the muting action cannot be initiated under any condition until some noise is present in the output signal. In this respect, the mute performance of the CA3089E differs from that of some other systems which are activated by signal level. Such systems can be adjusted to allow noise-free signals to be processed further. When the CA3089E circuit operates under small-signal conditions, noise may be audible before muting action occurs. The threshold-level adjustment only permits more or less noise to appear at the output; a listener can use the control to adjust the interstation hiss to the level of his preference.

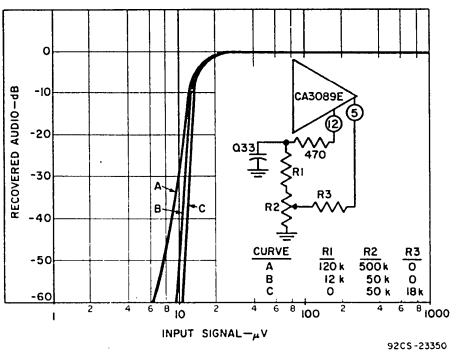



*Fig. 12—Mute curves.*

### Tuning Meter and RF-AGC Circuit

The tuning-meter circuit sums the output of three peak detectors connected to successive stages of the if amplifier-limiter. These circuits detect not only the carrier, but also harmonics developed when successive stages go into limiting and eventually form a square wave. The result is a logarithmic dc output as a function of input signal, as shown by the curve in Fig. 13. The circuit developing the delayed rf-AGC voltage is driven by the level detector connected to the first if stage. As a result, no output is detected until the input signal is large enough to drive the peak detector; the result is a delayed AGC action. The curve of rf-AGC voltage as a function of input signal is also shown in Fig. 13.

### IF Amplifier/Detector System and Stereo Decoder

Fig. 14 shows the circuit diagram of a complete FM-if detector system driving a stereo decoder. Using the selectivity of two ceramic filters, the CA3089E in conjunction with the CA3090AQ stereo decoder provides the basic signal processing between the tuner output and the

audio amplifiers. The gain of the silicon n-p-n bipolar-transistor stage is adjusted to make up the losses of the two filters. In addition to driving a tuning meter, the voltage at pin 13 of the CA3089E may be used to drive a "stereo defeat" circuit in the CA3090AQ, thereby holding the decoder in a monaural condition to improve the signal-to-noise ratio under weak signal conditions. A suggested PC-board pattern and parts layout are shown in Fig. 15.

### Operation at Frequencies Other Than 10.7 MHz

Because the CA3089E was designed for use in FM broadcast receivers, its circuits are optimized for use at 10.7 MHz. Nevertheless, the device performs equally well over a wide range of frequencies both above and below 10.7 MHz. The if amplifier response is essentially flat from dc to more than 20 MHz. The operation of the detector circuit is dependent only on the external components. The operation of the auxiliary sections–rf-AGC, meter output, and mute logic – depend on internal peak detectors, and, as a consequence, their performance at lower frequencies is limited. The internal capacitors were optimized for 10.7 MHz operation, and are too small to operate effectively at lower frequencies. The detector efficiencies begin to deteriorate at about 2 MHz, and the detectors are essentially unusable at 455 kHz without the use of external circuitry. The rf-AGC and mute logic circuits do not develop sufficient dc voltage to perform their functions, and the meter output signal loses its logarithmic characteristic and exhibits peaks and valleys as input signal is increased. Operation of the rf-AGC and mute logic circuits may be enhanced by the addition of a dc

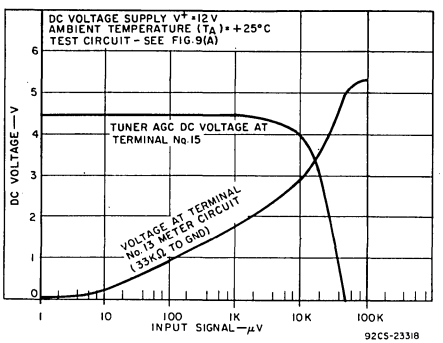



*Fig. 13–Tuner AGC and tuning-meter output as a function of input signal voltage.*

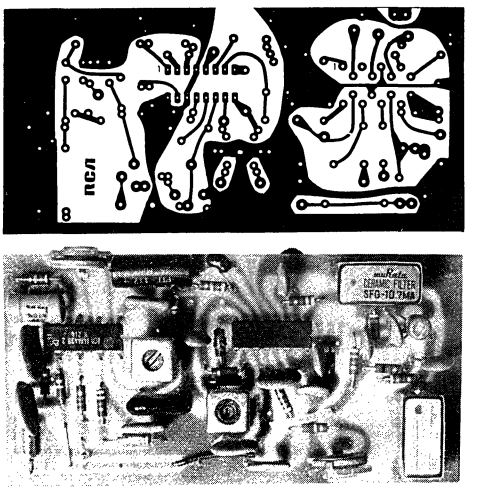


*Fig. 15–Suggested PC-board pattern and parts layout for the circuit of Fig. 14.*

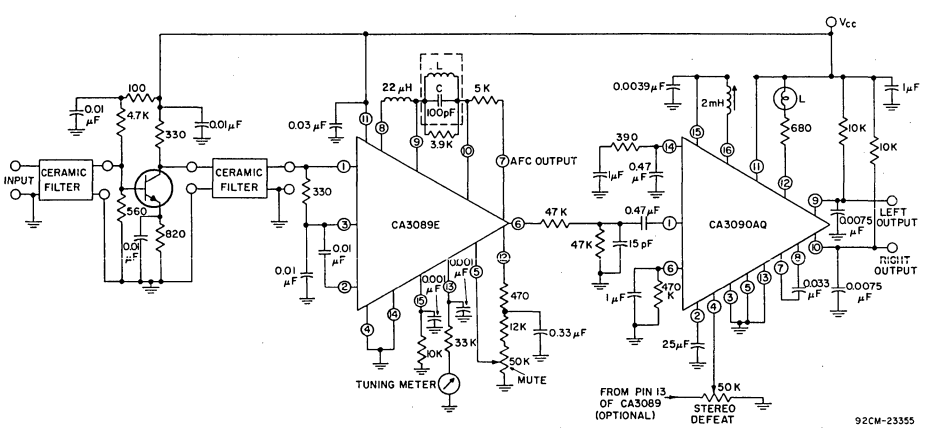



*Fig. 14–IF amplifier/detector system and stereo decoder.*

amplifier and inverter to each circuit. A simple example using a CA3096E IC transistor array is shown in Fig. 16.[3]

The CA3089E may be used effectively in narrow-band communication receivers. In double-conversion receivers, some of the functions of the CA3089E are negated at a 455-kHz intermediate frequency. However, if a 10.7-MHz intermediate frequency is used, all of the auxiliary features

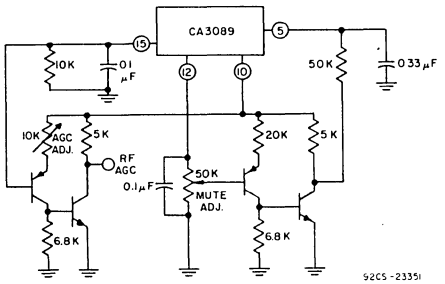



*Fig. 16—External mute and rf-AGC drive circuits for the CA3089E operating at 455 kHz. External transistors are parts of the CA3096E n-p-n/p-n-p transistor array.*

may be used, but another set of problems is encountered. The small deviation signals encountered in narrow-band systems require the use of high-Q circuits in the quadrature detector, as indicated in Table I. However, variations in external-component parameters with temperature changes may cause the tuned frequency of the detector to drift out of the if pass band. Normally temperature-compensated components are necessary. The CA3089E, operating in conjunction with an inexpensive operational transconductance amplifier,[4,5] provides means of locking the tuned circuit to the incoming frequency. Fig. 17 shows the block diagram of such a system. The AFC output voltage developed across the resistor between pins 7 and 10 is

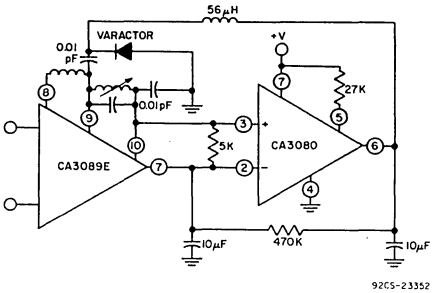



*Fig. 17—Detector frequency-stabilization circuit.*

amplified by the op-amp and drives a varactor to maintain the tuned frequency on the incoming-signal frequency.

The CA3089E may also be used as the core of an ultra-linear FM generator; Fig. 18 shows the circuit. The carrier is generated by the CA3089E with the introduction of feedback from the output terminal, pin 8. The carrier is modulated by the varactor connected across the tuned circuit at the input of the CA3089E. The varactor is driven by the output of the differential amplifier, A1, using a CA3028 IC.[6,7] This differential-amplifier stage is driven at one of its input terminals by the audio modulating signal. Negative feedback of the audio signal is provided by driving the other differential-amplifier input from the recovered audio output of the CA3089E at pin 6. The detector circuit uses a double-tuned transformer to produce audio with very little distortion at pin 6. This feedback technique results in a very low distortion modulation. The rf output of the CA3089E at pin 8 is essentially a square wave, and is fed to a tuned-amplifier stage to buffer the signal and restore the sine-wave-shaped rf output signal.

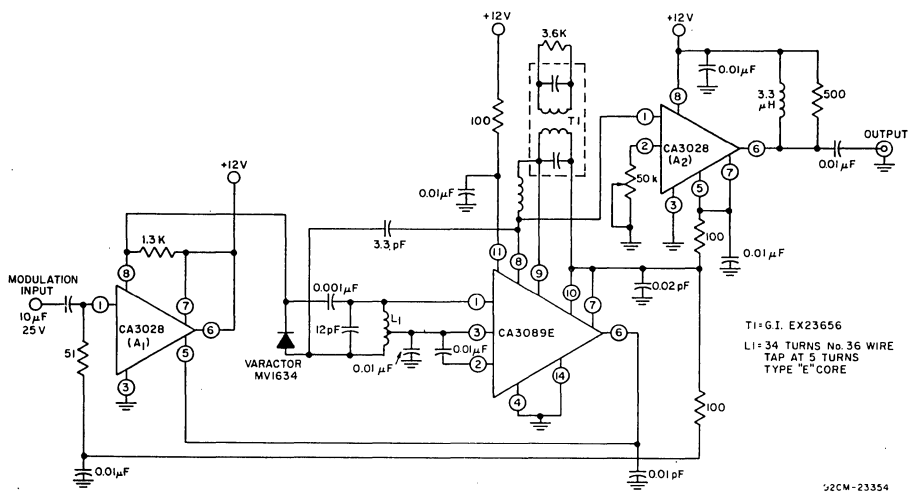



*Fig. 18 — FM generator circuit.*

# Integrated-Circuit Stereo Decoder Using the CA3090AQ Stereo Multiplex Demodulator

by

L.A. Kaplan, and A.L. Limberg
RCA Solid State Division
Somerville, New Jersey, 08876

The demodulation of FM stereo broadcast information may be accomplished very simply by use of no more than three transistors, four to six diodes, and two small transformers as major system components. All of these components may be very inexpensive with minimal specifications. However, accurate demodulation of FM stereo broadcast information, particularly when the signal to noise ratio of the incoming signal is poor and when the performance must be achieved over a wide ambient temperature range such as, for example, in the automobile radio, is an entirely different matter.

The system shown in Fig. 1 was built by RCA's Transistor Applications Laboratory to demonstrate a high-performance demodulator system. Some of the design considerations will be discussed later, but the complexity of the filtering included and the bulk of the system is evident.

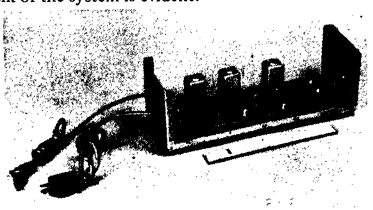


*Fig. 1 – Multiplex stereo decoder using discrete components.*

By contrast, the integrated-circuit system described in this Note*, Fig. 2, performs all the functions of its predecessor, and does them better. Performance of the IC system is summarized in Table 1.

* This Note supersedes RCA Technical Publication ST-4700, "Integrated-Circuit Stereo Decoder Does Everything," by L.A. Kaplan, H.M. Kleinman, A.L. Limberg.

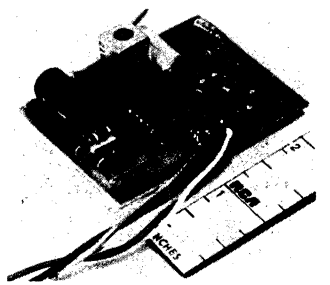


*Fig. 2 – Integrated-circuit multiplex stereo decoder.*

**Table I – Performance Data**

| | | |
|---|---|---|
| SEPARATION | | 40 dB |
| DISTORTION | 2nd Harmonic | <0.2% |
| | 3rd Harmonic | <0.1% |
| | 4th Harmonic | <0.1% |
| | 5th Harmonic | <0.1% |
| CAPTURE (% of CENTER FREQUENCY) | | 10% |
| SCA REJECTION | | –55 dB |
| MONAURAL GAIN (75 μs DE-EMPHASIS, 1 kHz) | | 6 dB |
| GAIN BALANCE BETWEEN CHANNELS | | <0.5 dB |
| STERO/MONAURAL GAIN BALANCE | | <0.5 dB |
| INPUT IMPEDANCE | | 50 kilohms |
| TEMPERATURE COEFFICIENT OF LOCAL OSCILLATOR | | –16 Hz/°C |
| LAMP DRIVER CURRENT | | 100 mA |

## DESIGN REQUIREMENTS AND OBJECTIVES

The stereo multiplex demodulator has simply defined tasks. First, it must reconstruct the 38-kHz carrier which was suppressed in forming the stereo signal. This reconstructed carrier must be properly phased to accomplish the demodulation process. Second, it must be substantially noise free to avoid further significant degradation of the signal-to-noise ratio of the output. This signal has already been degraded from that achieved in monaural transmission because of the wider system bandwidth of the stereo transmission.

A further function which demands narrow bandwidth in each channel is the stereo indicator which detects the presence of the 19-kHz pilot and energizes a lamp to inform the listener that stereo is being transmitted. If the bandwidth of the 19-kHz filters is too wide, noise energy in the pass-band of the filter can be sufficient to cause the light to blink during tuning between stations. This effect is undesirable in a high-quality system.

In essence, the demodulator must use the reconstructed carrier to demodulate the composite signal without introducing objectionable distortion. It must also have provisions for inhibiting the demodulation function when poor signal-to-noise conditions exist and, finally, must ignore completely the SCA signal transmitted by some stations. This signal is a second subcarrier bearing FM information modulated at about 67 kHz. Unless care is taken, the intermodulation products of the 38-kHz subcarrier (stereo) and the 67-kHz subcarrier (SCA) form audible beats.

These requirements of phase fidelity and low noise are difficult to achieve simultaneously in a compact, inexpensive system using traditional techniques because of the method of carrier synchronization. The 19-kHz pilot signal must be selected, amplified, and doubled without disturbing its phase relationship with the 38-kHz difference-signal (L-R) information. When conventional LC filtering techniques are used, conflicts are established. If noise is to be reduced in the subcarrier regeneration process, narrow bandwidth is needed in that channel. Narrow band filters, unless they are both accurately designed and precisely tuned, can cause substantial phase shift.

Analysis shows that 26 degrees of phase shift of the 38-kHz subcarrier relative to the 38-kHz sidebands will degrade the separation of an otherwise perfect system from infinity to 26 dB. Because a degradation of 20 dB would cause the system to fail most instrument specifications and would be detectable by critical listeners in some situations, it is reasonable to demand that phase shift in the subcarrier not consume all of the permitted degradation.

If each transformer were to have a 9-degree phase shift at 38 kHz, the reactance factor X for the 38 kHz trans.=0.158, where $X = 2\Delta fQ/f_0$. This condition is obtained when the attenuation in that transformer is computed from $X = \tan^{-1}\theta$ and the attenuation $(\rho) = \sqrt{1 + X^2}$ so that $\rho = \sqrt{1 + (.1582)^2} = 1.012$ or less than 0.1 dB. Because only 4.5 degrees are permitted in each of the 19-kHz transformers, the attenuation for permissible phase shift will be less than 0.1 dB.

This analysis clearly shows that manual tuning of the subcarrier channel cannot be achieved by the traditional peaking methods, rather, it must be aligned by measuring channel separation characteristics. Further, once correct tuning is achieved, the permissible mistuning resulting from mechanical or environmental conditions must be low. If quality factors (Q's) of 25 are assumed, the permissible mistuning of a 19-kHz transformer is given by

$$\frac{\Delta f}{f} = \frac{\tan 4.50^\circ}{2Q} = \frac{0.08}{50} \text{ or } 0.16\%$$

and for the 38-kHz coil:

$$\frac{\tan 9^\circ}{50} = \frac{0.16}{50} \text{ or } 0.32\%$$

These values represent a mistuning of 30 Hz at 19 kHz and 120 Hz at 38 kHz, respectively. If the mistuning is due only to temperature over a ±50°C ambient temperature range, the following temperature compensation is required:

$$\frac{\Delta f}{f} \Big/ \Delta T = \frac{0.0016}{50} = \frac{0.0032}{100} = 0.000032$$

or 32 PPM/°C for the 19-kHz transformer and 64 PPM/°C for the 38-kHz one. Finally, if higher Q coils are used to improve selectivity and to reduce noise in the subcarrier, the stability of the circuits must be even better.

Non-distorting demodulation and stereo disabling can be accomplished easily, but care must be taken to insure that the latter be accomplished in a manner that eliminates transient level shifts when the switching occurs. Rejection of the SCA channel is generally guaranteed to some extent by LC filtering at the input to the demodulator which removes signal components above 60 kHz. This method requires either expensive pretuned components, or an additional alignment, and runs the risk of causing phase shift of the higher subcarrier sideband frequencies, thereby degrading separation for the highest frequency components of the program.

There are three specific problems which the designer of a stereo multiplex demodulator must consider if he has to achieve an economical high performance design:

1. Provide a narrow band carrier regeneration channel with negligible phase shift over the ambient temperature range and life of the equipment. This setup should preferably be alignable with a single simple adjustment.
2. Develop a system which inherently rejects the 67-kHz SCA subcarrier so that an LC filter is not required for that purpose.
3. Provide stereo-monaural switching without audio "plops".

In addition to these rather difficult problems, the designer must not ignore distortion which must be kept well below 0.5 precent, and, of course, he must minimize the cost of external components.

### Description of the RCA CA3090AQ Stereo Multiplex Demodulator IC

Fig. 3 shows the CA3090AQ as it is used in a typical FM receiver. From this illustration, the solutions to the problems

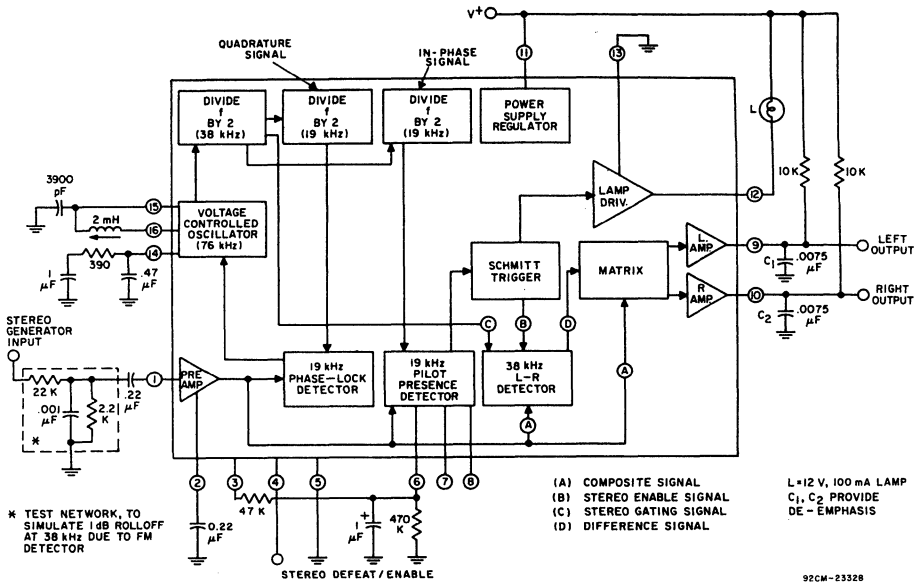



*Fig. 3 – Block diagram of the RCA CA3090AQ system.*

posed previously will be studied. In this circuit, carrier regeneration is accomplished by use of a phase-lock automatic frequency and phase control (AFPC) loop made up of a voltage-controlled oscillator operating at 76 kHz, a series of flip-flops to obtain the required signals needed in the system, and a synchronous detector the DC output of which is proportional to the relative phase angle between the frequency-divider output and the 19-kHz component of the composite signal. Bandwidth of the loop is determined by an external RC filter and, as will be shown later, the steady-state phase error is only indirectly related to the bandwidth of the phase-locked loop.

The voltage-controlled oscillator (VCO) used in this circuit is an LC oscillator. This type was chosen over the apparently simpler RC oscillator on the basis of its superior long-term and temperature stabilities. It is noted that the oscillator operates at 76 kHz, while the maximum frequency required by the signal processing circuits is 38 kHz. The higher frequency is used at the expense of extra chip complexity to insure that the reinserted 38-kHz carrier is perfectly symmetrical, because any loss of symmetry will impair audio-channel separation. By starting at 76 kHz and dividing by two to get the required 38 kHz, symmetry is guaranteed, though the phase of the 38 kHz may shift relative to the 76-kHz voltage. This shift, however, is not significant.

Fig. 3 also shows that the switching input to the phase-detector (AFPC) is not in phase with the pilot frequency but is displaced by 90 degrees. This condition will exist when there is no phase error, because the demodulator is a multiplier whose output is proportional to the cosine of the angle between the inputs. Because the output of this detector may be considered as an error voltage in a feedback loop, the system will attempt to make it zero, hence, the 90° displacement so that the required 38-kHz signal is of the proper phase. And because the output of the AFPC detector is zero when both the uncontrolled frequency of the oscillator is correct and when there is no 19-kHz pilot, and extra detector, the pilot presence detector, is needed to signal the presence of a stereo broadcast. The 19-kHz output from the frequency-divider is in phase with the pilot signal and will, therefore, provide a signal to the stereo-mono switch to enable stereo reception. An external RC network sets the threshold sensitivity and time constant of this detector. This filtering, along with the hysteresis in the stereo-mono switch, eliminates all interstation flicker of the stereo indicator lamp.

The L-R synchronous detector is a fully degenerated doubly-balanced detector. Great care is taken to guarantee that the composite signal currents fed to it are as nearly distortion-free as possible to preserve both fidelity and SCA rejection. Should significant distortion exist, intermodulation products of the sidebands of the 38-kHz and 67-kHz subcarriers would be formed before demodulation. Many of these spurious signals will be within the 23- to 53-kHz bandwidth of the demodulation and would therefore show up in the output as audible whistles and beats.

The outputs of the L-R detector are added to the composite signal in summing networks where precisely matched resistors provide the proper scale factors. Theoretically, the sum signal (L+R) channel must be attenuated by the ratio $2/\pi$ to obtain perfect separation. This ratio holds true only for perfect

composite inputs. Experinece has shown that nearly all commercial FM tuners attenuate the high-frequency components of the composite signal by some amount, usually in the order of 1 dB and 38 kHz. Therefore, the L+R is attenuated slightly more than $2/\pi$ to compensate for this degradation of the input signal. (See Fig. 12 for a curve of error caused by imperfect detector response.) If the CA3090AQ is called upon to process a "perfect" composite signal, audio-channel separation will be in the order of 26 dB because of this deliberate deviation.

The phase-splitter, post-amplifiers, and the stereo-mono switch which contains an enabling circuit capable of responding to an external DC voltage to permit stereo reception complete the integrated circuit. This latter circuit may be connected at the users option and can inhibit stereo reception until a positive going DC voltage exceeds 1.6 volts. As in the case of the primary stereo-mono switch, hysteresis is provided to reduce the flicker of the stereo indicator under weak signal conditions.

### Phase Lock Loop (AFPC Loop) Operation

The operation of phase-lock loops (PLL) is well documented in the literature and is treated mathematically at some length in the Appendix section. It will be discussed briefly here to indicate the degree to which the phase-lock can provide superior performance to that achievable by conventional filter methods.

The functional blocks of the PLL are shown in Fig. 4. The multiplier is the phase-detector with the reference signal $E_2 \sin\omega_0 t$ and the VCO signal $A\cos(\omega_0 t - \theta)$ ($\theta$ is the phase error in radians) applied to it. The output of the detector is K $\cos\theta$ in which K is a function of $E_2$ as well as the parameters of the multiplier. The phase error output is proportional to $\sin\theta$ because of the phases of the angles selected. It is noted that, if the frequency of the VCO differs from that of the input, $\theta$ will

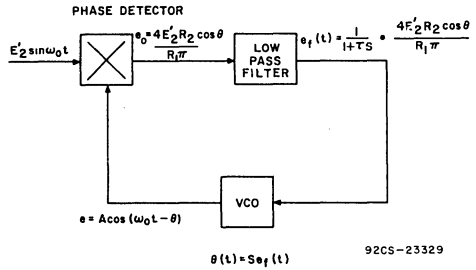



*Fig. 4 – Block diagram of a phase-locked loop (PLL).*

equal $+\omega_d t$ in which $\omega_d t$ is $2\pi$ times the frequency difference between the two oscillators. This condition will occur before frequency-lock is achieved. The error voltage, K sin $\theta$; is passed through a low-pass filter and applied to the control terminal of the VCO. Once the VCO is locked in frequency to the input signal, $\theta$ will become a constant and the output of the detector will be a DC voltage which is proportional to the phase-error. It can be reasoned, without resorting to mathematics, that this resultant voltage must be just the voltage required to change the frequency of the VCO from its natural frequency to that of the input frequency, i.e.:

$$K \sin\theta = \frac{\omega d}{S}$$

where $\omega d$ is the previously noted difference frequency and S is the sensitivity of the VCO. This equation can be expressed in easily measured terms and solved for $\theta$, where

$$\theta = \frac{\omega d}{KS} \text{ for small angles.}$$

In this case, $f_d$ and S can be measured at any point along the frequency divider. Because the oscillator is available, measurement is taken at that point and it is found that S equals about 400 Hz per millivolt. The phase-detector output K is measured at 2 millivolts per degree of phase differential at 19 kHz, which is the equivalent of 1 millivolt per degree at 38 kHz. The resultant phase-error in the PLL is $f_d/400$ or, more usefully 1.9 degrees per percent in oscillator shift. In other words, if the VCO is adjusted to a nominal 76-kHz frequency and then shifted by 3.8 kHz because of aging, temperature effects, or other reasons, this frequency shift of 5 percent would cause a shift of 9.5 degrees in phase of the regenerated 38-kHz carrier. Curves (Fig. 13) show that such a 5 percent frequency-shift would cause the audio-channel separation of an otherwise perfect system to drop to 42 dB, virtually unnoticeably.

The degradation caused by a 5-percent frequency shift may be compared with the 26-dB separation characteristic resulting when the three coils of the classical filter-approach shift by only 0.3 percent. It is noted that the final phase-error is not a function of the filter placed in the loop (see Appendix B). That time constant is constrained by the stability of the VCO's unlocked natural frequency. In the present system, a filter with a 54-Hz bandwidth is used and provides a capture capability in excess of 4 kHz at 76 kHz. The classical filter-approach previously described has a 3-dB bandwidth or nearly 200 Hz at 19 kHz with proportionally poorer noise performance.

### The LC Oscillator and Reactance Circuit

The LC oscillator is undoubtedly the most controversial portion of the CA3090AQ system. The demand for "inductorless designs" was not ignored during the development, but performance sacrifices were required to reliably implement such a design if low-cost external components were to be used. Comparisons were made on two levels, that of stability of the semiconductor portion of the oscillator circuit with both aging and temperature and stability of the oscillator frequency as the external components varied with both aging and temperature.

Tests on the CA3090AQ indicated oscillator sensitivity to temperature changes to be less than 1.5 percent for 50°C temperature changes. Data sheets for commercially available integrated-circuit voltage-controlled RC oscillators show changes of 4 to 7 percent for the same temperature change. These changes do not indicate that better RC oscillators cannot be built, but suggests that such designs will be an interesting challenge to the IC designer.

More compelling than the previous discussion is the problem of the external components. Because some method of tuning must be used if the nominal frequency is to be set accurately, either a tunable inductor, variable capacitor, or potentiometer must be used.

The resonant frequency for a general RC oscillator is $\omega = K/RC$ while $\omega$ for the LC oscillator is $1/\sqrt{LC}$. Differentiating each of these with respect to the assumed variable components (R or L) shows that:

$$\frac{d\omega}{dR} = -\frac{\omega_o}{R} \text{ for the RC oscillator and}$$

$$\frac{d\omega}{dL} = -\frac{\omega_o}{2L} \text{ for the LC oscillator}$$

In other words, it would take twice the parameter variation for the LC oscillator as it does for the RC oscillator to create the equivalent frequency shift.

The most attractive adjustment for an RC oscillator is the inexpensive carbon-composition trimmer. Available data indicate temperature coefficient of the order of 1000 PPM/°C and changes with humidity of 3 percent nominal value after exposure and drying. It is noted that this 3 percent change for an RC oscillator would generate a 2.3-kHz shift in frequency due to humidity alone. Trimmers with far more stable characteristics are available, but at a substantial cost preminum.

### Stereo Defeat Circuit

In most modern FM receivers the RF/IF gain is high enough to cause limiting on noise alone. The signal-to-noise ratio increases as the incoming signal increases but it may be desirable to prevent stereo operation, with its attendant signal-to-noise degradation, until the input signal-to-noise is above a selected threshold.

A stereo defeat circuit has been incorporated into the CA3090AQ for this purpose as shown in Fig. 5. It is a fairly conventional Schmitt trigger which allows the unit to function in stereo when the voltage at pin 4 exceeds plus 1.6 volts. The hysteresis is about 0.1 volts, thereby assuring the continuance of stereo function despite small changes in signal level.

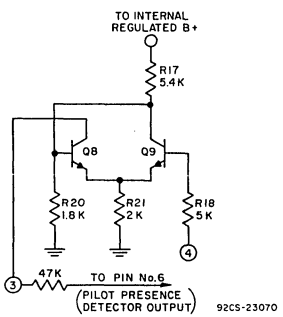



*Fig. 5 – Stereo-defeat circuit.*

### DC Coupled Flip-Flop

It was apparent at the outset of the design that a direct-coupled flip-flop was required. If the capacitors needed for a conventional flip-flop were designed "on-chip", these capacitors would spread over very large amounts of chip area, and, if they were placed "off-chip", they would use up the limited number of package terminals.

The flip-flop design is shown in Fig. 6. Transistors Q1 and Q2 are connected as the storage flip-flop and Q3 and Q4 as the

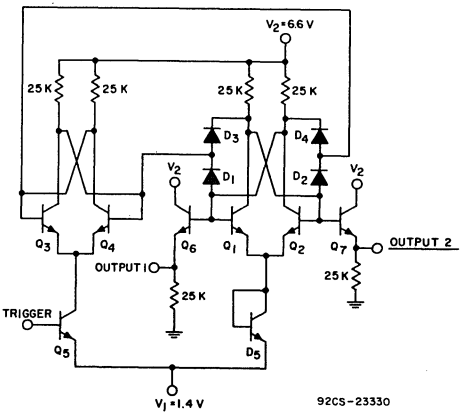



*Fig. 6 – DC coupled flip-flop.*

commutation flip-flop. The information stored in the storage flip-flop is coupled through diodes D1 and D2 to guide the biasing of the commutating flip-flop when Q5 is triggered into conducting by a positive pulse. When the commutating flip-flop is placed into conduction, diodes D1 and D2 are biased out of conduction. Current is coupled through one of the diodes D3 and D4 to cause the storage flip-flop to change state. At the end of the positive pulse triggering Q5 into conduction, the module is again ready to accept trigger to change the state of the storage flip-flop.

If the trigger pulses applied to Q5 have regularly timed leading edges, the outputs of the module taken from the storage flip-flop through emitter followers Q6 and Q7 are push-pull square waves between 1.4 and 2.1 volts.

### Preamplifier Phase Splitter

The preamplifier phase splitter is illustrated in Fig. 7. The circuit is symmetrical, and is most easily analyzed by considering one half of it. In this case, Q78 is an emitter follower supplied by Q4, and Q6 is a shunt regulator stage; Q1 and Q2 are current sources. When current in Q4 and Q78 tends to increase, the potential at the base of Q6 rises and causes Q6 to draw more current. The increased current demanded by Q6 must come from the emitter of Q4. If Q4 passes a constant current, its base-emitter potential will not vary, and the base current will be constant. Thus, the input impedance to ac will be high and the signal will be passed with low distortion.

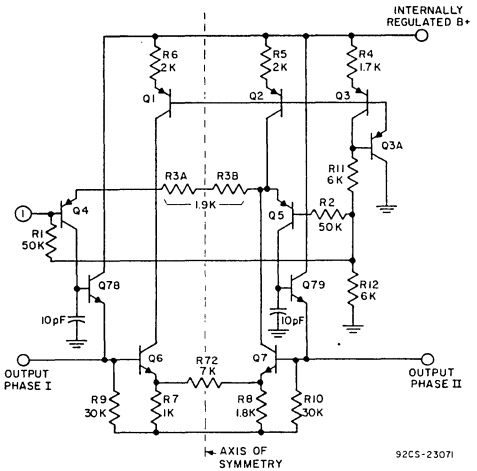



*Fig. 7 – Preamplifier phase splitter.*

The accurately reproduced input signal which appears at the emitter of Q4 then forces a current through the 1.9-kilohm resistor connected to the emitter of Q5. Because the emitter current of Q4 is held constant by the shunt regulator Q6, the collector current of Q6 must be complementary to the current in the 1.9-kilohm resistor and also proportional to the input signal.

Any transistors having identical geometry and emitter resistors with bases connected to the base of Q6 will have collector currents identical to that of Q6. By similar analysis, Q7 will have collector current exactly proportional to the current in the 1.9-kilohm resistor, and identical transistors connected in phase to those connected to Q6.

## PERFORMANCE

Pertinent performance data for the CA3090AQ are summarized in Table I. The variation in capture range is shown in Fig. 8 as the phase-lock filter capacitor is varied (see Appendix C). The effects of the level of pilot on the capture range are illustrated in Fig. 9. In both graphs the clear areas represent sufficient conditions for "capture" into stereo operation, while the shaded areas indicate probable failure to "capture."

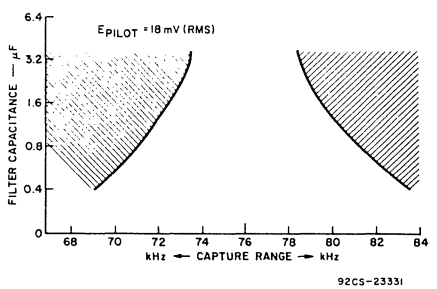



*Fig. 8 – Capture range as a function of the filter capacitance.*

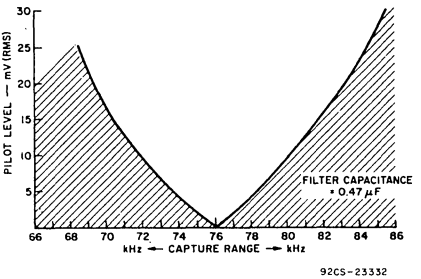



*Fig. 9 – Capture range as a function of pilot level.*

## CONCLUSION

The RCA CA3090AQ integrated-circuit provides features heretofore unavailable to the receiver designer. This device needs only a single tuning adjustment which reduces to a minimum the manual effort during assembly, while the phase-locked loop maintains performance under conditions of temperature variations, humidity, and aging. The compactness of the CA3090AQ and of external components, added to the other attributes, makes this stereo decoder a significant advancement in the state of the art.

## APPENDIX A

### Detector Response

Most practical FM receivers are designed so that the audio response at the second detector rolls off somewhere above the audio range for IF filtering and reduction of "tweet" effects. The voltage response V in the time domain is given by

$$V = \frac{\sin\left(\omega t - \tan^{-1}\omega/\omega_o\right)}{\sqrt{1+\left(\frac{\omega}{\omega_o}\right)^2}} \qquad (1)$$

where t is the time, $\omega$ is the frequency, and $\omega_o$ is the cutoff frequency of the detector.

A properly tuned phase-lock detector will lock to the 19-kHz pilot and reconstruct the 38-kHz gating signal at zero phase. The 38-kHz sidebands will be delayed in time with respect to the 19-kHz pilot-tone. The time-delay difference $\Delta t$ between the two is given by

$$\Delta t = \frac{\tan^{-1}\frac{2\omega_1}{\omega_o} - 2\tan^{-1}\frac{\omega_1}{\omega_o}}{2\omega_1} \qquad (2)$$

where $\omega_1 = 2\pi \times 19$ kHz

The corresponding phase angle $\Delta$ is given by:

$$\Delta = \tan^{-1}\frac{2\omega_1}{\omega_o} - 2\tan^{-1}\frac{\omega_1}{\omega_o}$$

A composite signal, S, is assumed in the form:

$$S = L + R + f(\omega_o)(L\text{-}R)\cos\phi + \text{Pilot} \quad (3)$$

where the gate signal is at reference phase $\theta$ and input signal is at phase $\phi$ separated from $\theta$ by the phase error $\Delta$ and

$$f(\omega_o) = \frac{1}{\sqrt{1+\frac{4\omega_1^2}{\omega_o^2}}} \quad \text{(amplitude error function)} \quad (4)$$

The gate signals G are given by

$$G^+ = \frac{1}{2} + \frac{2}{\pi}\sum_{N=o}^{\infty}\frac{1}{2N+1}\cos(2N+1)\theta$$
$$G^- = \frac{1}{2} - \frac{2}{\pi}\sum_{N=o}^{\infty}\frac{1}{2N+1}\cos(2N+1)\theta \quad (5)$$

The gated signals are

$$SG^+ = S \times G^+$$
$$SG^- = S \times G^- \quad (6)$$

The output signal $S_{out}$ is given by

$$S_{out} = S + SG^+ + (-SG^-) \quad (7)$$

Substitution of Eqs 3, 5, and 6 into Eq. 7 results in the following:

$$S_{out} = \frac{2}{\pi}(L+R) + \frac{2}{\pi}f(\omega_o)\cos(\theta - \Delta) + \frac{4}{\pi}(L+R)\sum_{N=o}^{\infty}\frac{1}{2N+1}\cos(2N+1)\theta + \frac{4}{\pi}f(\omega_o)(L-R)\cos(\theta-\Delta)\sum_{N=o}^{\infty}\frac{1}{2N+1}\cos(2N+1)\theta \quad (8)$$

The signal separation L/R is given by

$$\frac{L}{R} = \frac{1 + f(\omega_o)\cos(\theta-\Delta) + 2\left[\sum_{N=o}^{\infty}\frac{1}{2N+1}\cos(2N+1)\theta\right]\left[1+f(\omega_o)\cos(\theta-\Delta)\right]}{1 - f(\omega_o)\cos(\theta-\Delta) + 2\left[\sum_{N=o}^{\infty}\frac{1}{2N+1}\cos(2N+1)\theta\right]\left[1-f(\omega_o)\cos(\theta-\Delta)\right]} \quad (9)$$

The decoded information is the integral of the output averaged over one cycle of carrier frequency and is given by

$$\frac{L}{R} = \frac{1 + f(\omega_o)\cos\Delta}{1 - f(\omega_o)\cos\Delta} \quad (10)$$

A curve of this function is shown in Fig. 10.

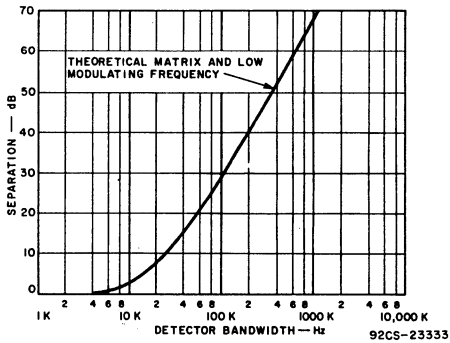



*Fig. 10 — Theoretical separation as a function of detector bandwidth.*

**Matrix Error and Fixed Phase Error**

When the oscillator has been incorrectly tuned and when the system has "captured" and locked to the pilot-tone, there will be a fixed phase error $\Delta$ which is a function of the original amount of detuning and the phase-lock loop gain discussed in Appendix B. This fixed phase error will produce a loss of audio-channel separation as will an error in the resistor ratios of the matrix. The equations are as above except that a fixed gain-error constant k is introduced into the signal term as follows:

$$S_{out} = kS + SG^+ + (-SG^-) \quad (11)$$

Substitution of Eqs. 3, 5, and 7 again yields the following:

$$S_{out} = k(L+R) + k(L-R)\cos(\theta-\Delta) + \frac{4}{\pi}(L+R)\sum_{N=o}^{\infty}\frac{1}{2N+1}\cos(2N+1)\theta + \frac{4}{\pi}(L-R)\cos(\theta-\Delta)\sum_{N=o}^{\infty}\frac{1}{2N+1}\cos(2N+1)\theta \quad (12)$$

The separation is then given by

$$\frac{L}{R} = \frac{k[1+\cos(\theta-\Delta)] + \left[\frac{4}{\pi}\sum_{N=o}^{\infty}\frac{1}{2N+1}\cos(2N+1)\theta\right]\left[1+\cos(\theta-\Delta)\right]}{k[1-\cos(\theta-\Delta)] + \left[\frac{4}{\pi}\sum_{N=o}^{\infty}\frac{1}{2N+1}\cos(2N+1)\theta\right]\left[1-\cos(\theta-\Delta)\right]} \quad (13)$$

Integrating and averaging as before reduces this equation to the following:

$$\frac{L}{R}=\frac{k+\frac{2}{\pi}\cos\Delta}{k-\frac{2}{\pi}\cos\Delta}$$

A new constant K is defined such that

$$\frac{L}{R}=\frac{K+\cos\Delta}{K-\cos\Delta}$$

Families of curves generated by this function are given in Fig. 11.

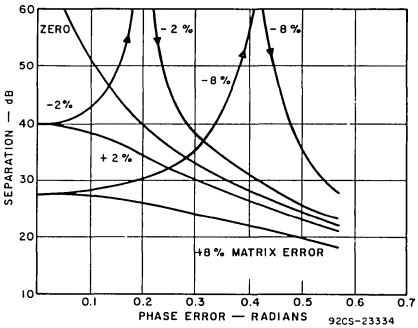



*Fig. 11 — Separation as a function of static phase error and matrix error.*

## APPENDIX B

### Doubly-Balanced Phase-Detector

A doubly-balanced phase detector is sketched in Fig. 12(a). The pilot-tone is present as the bases of the lower transistors Q19 and Q27, which are operating linearly. The bases are driven at opposite phases of the phase splitter (Fig. 7). The voltages $E_1$, and $\bar{E}_1$, are derived from the counter and are assumed large enough to gate transistors Q20, Q21, Q25, Q26 on and off. Thus, if the period is T and $E_2 = E_2' \sin(\omega_0 t + \theta)$, emitter currents at half cycles are given by

$$\left[I_{Q20}\right]_0^{T/2}=\frac{E_2}{R_1};\ \left[I_{Q20}\right]_{T/2}^{T}=0;\ \left[I_{Q21}\right]_0^{T/2}=0;\left[I_{Q21}\right]_{T/2}^{T}=\frac{E_2}{R_1};$$
$$\left[I_{Q25}\right]_0^{T/2}=-\frac{E_2}{R_1};\ \left[I_{Q25}\right]_{T/2}^{T}=0;\ \left[I_{Q26}\right]_0^{T/2}=0;\left[I_{Q26}\right]_{T/2}^{T}=-\frac{E_2}{R_1} \quad (14)$$

where R1 is the effective value of the emitter resistor. The DC output ($E_3$ - $E_4$) is the average of the currents in the load resistors R2, integrated over one cycle as follows:

$$I_{Q20(AV)}=\frac{1}{T}\int_0^{T/2} I_{Q20}dt=\frac{E_2'}{R_1\pi}\cos\theta$$
$$I_{Q21(AV)}=\frac{1}{T}\int_{T/2}^{T} I_{Q21}dt=-\frac{E_2'}{R_1\pi}\cos\theta \quad (15)$$

and similarly

$$I_{Q25(AV)}=-\frac{E_2'}{R_1\pi}\cos\theta;\ I_{Q26(AV)}=\frac{E_2'}{R_1\pi}\cos\theta$$

Summing these currents, the detected output is given by

$$E_4-E_3=\frac{4E_2'R_2}{R_1\pi}\cos\theta \quad (16)$$

In this case, $E_2$ is the peak value of the 19-kHz pilot tone on the line. The effective value of the emitter resistor $R_{eff}$ in the actual circuit (Fig. 12(b)) is given by:

$$R_{eff}=\frac{R_e R_{1\text{-}2}}{2R_e+R_{1\text{-}2}} \quad (17)$$

### Loop Operation

Phase-locked loops, derivations and theory, are covered in the references 2, 3, and 4. Terminology used in this paper will conform to that in reference 2.

The differential equation governing the loop behavior is

$$\Delta\omega=\omega_P-\omega_{VCO}+F(s)\,S\,E_{3\text{-}4}\cos\theta \quad (18)$$

where $\Delta\omega$ is the difference between the free-running frequency of the controlled-oscillator, the reference signal $\theta$ is the phase difference between the reference signal and the instantaneous frequency of the controlled oscillator, $\omega p$ is the reference frequency; $\omega VCO$ is the VCO frequency; F(s) is the transfer function of the control network; E3-4 cos $\theta$ is the output of the phase detector and is $4E_2R2/R1\pi \cos\theta$; and S is the sensitivity of the VCO in radians/second/volt (see Appendix C).

The steady-state solution of the system is as follows:

$$\cos\theta = \frac{\Delta\omega R_1\pi}{4E_2'R_2S} \tag{19}$$

The steady-state phase error $\theta_{SS}$ is $\frac{\pi}{2} - \theta$ or

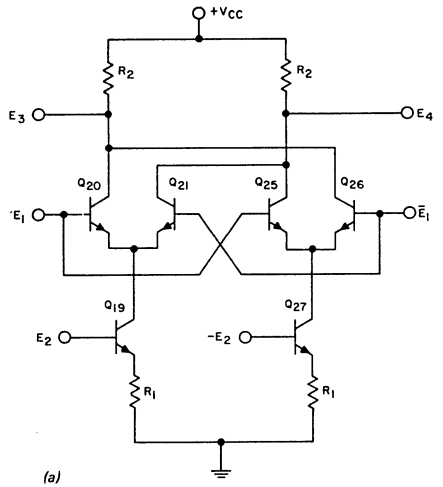
$$\sin\theta_{SS} = \frac{\Delta\omega R_1\pi}{4E_2'R_2S} \tag{20}$$

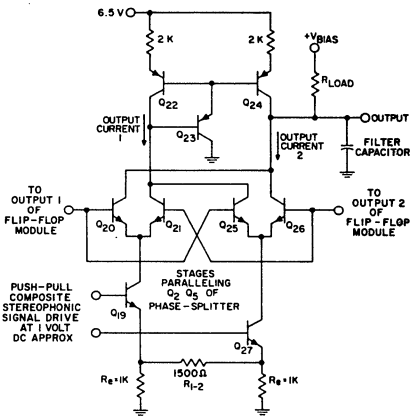
Because the maximum value that the sine can assume is one, the maximum hold-in is as follows:

$$|\Delta\omega_{hold\text{-}in}| \leq \frac{4E_2'R_2S}{R_1\pi} \tag{21}$$

In the case where the loop filter is a simple lag network, $\tau = RC$ and $F(s) = 1/1 + \tau s$, the capture range (pull-in) approaches the hold in range as $\tau$ becomes smaller. At the edge of the lock range pull-in is assured for[3]

$$\sqrt{\frac{1}{\tau} \cdot \frac{4E_2'R_2S}{R_1\pi}} \approx 1.2 \tag{22}$$




92CM-23335

*Fig. 12(a) — Doubly-balanced phase detector used for purposes of analysis and (b) actual IC phase detector.*

## APPENDIX C

### VCO Sensitivity

By reference to the schematic representation of the reactance circuit in Fig. 13 the admittance Y at the collector of Q2 is found to be

$$Y = \frac{1}{j\omega L} + j\omega C + \frac{KA}{1 + A(1 - K)} \cdot \frac{1}{j\omega L} \tag{23}$$

From this expression the resonant frequency is found to be

$$\omega = \omega_o \left[\frac{1 + A}{1 + A(1 - K)}\right]^{1/2} \tag{24}$$

where $\omega_o$ is the resonant frequency of just the passive components, A is the loop gain of the internal circuit ($\alpha$ of transistor Q3 is assumed to be very close to one), and K is a fraction of the current from the current source Ail. The rate of change of $\omega$ with respect to K is given by

$$\frac{d\omega}{dK} = \frac{\omega_o A}{2(A + 1)} \left[\frac{1 + A(1 - K)}{A + 1}\right]^{-3/2} \tag{25}$$

The change in the frequency must be defined in terms of the control voltage from the phase detector, which is the differential voltage between the bases of Q1 and Q2.

The expression for K is found from the standard differential amplifier equations given as:

$$K = \frac{1}{1 + \exp.\left[\frac{V_{BE_1} - V_{BE_2}}{kT/q}\right]} \quad (26)$$

If $VBE_1 - VBE_2$ is designated as the differential control voltage, V and kT/q is set equal to 26 millivolts at 25°C, then the differentiated Eq. 26 becomes

$$\frac{dK}{dv} = \frac{-\frac{1}{26}e^{V/26}}{(1 + e^{V/26})^2} \quad (27)$$

At balance condition when V = 0, K = 1/2 and $\frac{dK}{dv} = -\frac{1}{104}$

The value of A may be calculated without direct measurement by solving Eq (24) knowing both $\omega$ and $\omega_o$, as follows:

$$A = \frac{1 - \frac{\omega^2}{\omega_o^2}}{\frac{\omega^2}{\omega_o^2}(1 - K) - 1} \text{ and } A = \frac{2\left(1 - \frac{\omega^2}{\omega_o^2}\right)}{\frac{\omega^2}{\omega_o^2} - 2} \text{ at balance} \quad (28)$$

The rate of change of $\omega$ with respect to v is given by

$$\frac{d\omega}{dK}\frac{dK}{dv} = \frac{\omega_o A}{2(A+1)}\left[\frac{1 + A(1 - K)}{A + 1}\right]^{-3/2} \times \frac{\frac{1}{26}e^{V/26}}{(1 + e^{V/26})^2} \quad (29)$$

By use of Eq 28 at balance and substituted into Eq 29, a typical unit in which the resonant frequency of the passive components equals 59-kHz (and f = 76-kHz), df/dv is found to be 442 Hz per millivolt. This value is the constant S of the Appendix B.

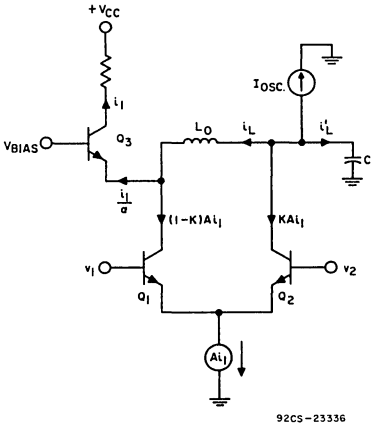



*Fig. 13 – Reactance circuit.*


## ACKNOWLEDGEMENT

The authors acknowledge the work of Mr. B. Zuk, RCA Solid State Division, who is responsible for invention of the DC coupled flip flop and the preamplifier phase splitter described in this paper.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# Features and Applications of RCA-CD2500E-Series MSI BCD-to-7-Segment Decoder-Drivers

by J. Lee

The RCA BCD-to-7-segment decoder-drivers, types CD2500E, CD2501E, CD2502E, and CD2503E, are medium-scale-integration (MSI) monolithic circuits designed to accept four inputs in BCD 8-4-2-1 code and provide decoded outputs that represent a decimal number from 0 to 9 on a 7-segment incandescent display device. The decoder-drivers are supplied in 16-terminal dual-in-line plastic packages that can be used over the operating temperature range from 0°C to +75°C.

The CD2500E and CD2501E are 30-milliampere-per-line drivers intended for use with 7-segment incandescent display devices such as the RCA DR2000 and DR2010 Numitrons. The CD2502E and CD2503E are 80-milliampere-per-line drivers intended for use with high-current lamps and relays and may also be used for multiplex operation of RCA Numitrons. The CD2500E and CD2502E include a decimal-point driver, and the CD2501E and CD2503E have a special terminal that may be used for ripple blanking and/or intensity control. The basic features of the CD2500E-series 7-segment decoder-drivers are as follows:

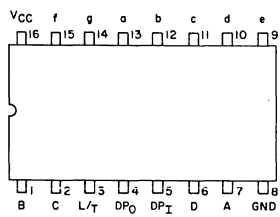
- High current-sink capability for direct display driving (no external discrete components are required)
- Provision for lamp test
- Operation from a 5-volt dc power supply
- Clamp diodes on all inputs
- Provision for ripple blanking and/or intensity control (CD2501E and CD2503E only)
- Decimal-point output (CD2500E and CD2502E only)
- BCD inputs that are compatible with commercially available diode-transistor-logic (DTL) and transistor-transistor-logic (TTL) devices
- Over-range detection (automatic blanking of display device when BCD inputs correspond to a number greater than 9)

## LOGIC DESCRIPTION

Table I shows the logic levels ("0" or "1") required at each input terminal for selection of the appropriate segments on the display device to represent a specific decimal number from 0 to 9 and for the decimal-point output, the lamp test, or the ripple-blanking function. The lower-case letters over the OUTPUT columns in the table identify the segments on the display device to which each output is applied. The last column in the table indicates the type of displays obtained on the display devices for each specific combination of BCD inputs. Figs. 1 and 2 show the terminal numbers on the decoder drivers that correspond to these outputs, and Fig. 3 shows the segment arrangement and designations for two 7-segment incandescent display devices, the RCA DR2000 and DR2010 Numitrons.

### Conversion of BCD Data Inputs to 7-Segment Display Outputs

The basic BCD-to-7-segment decoder-driver logic system consists of inverters, buffers, NAND gates (positive logic), TTL inputs, and open-collector transistor outputs, as shown in Fig. 4. Four information bits in BCD 8-4-2-1 code are applied to the BCD inputs. Eight input gates, Nos. 1 through




$DP_O$ = DECIMAL POINT OUTPUT
$DP_I$ = DECIMAL POINT INPUT

D,C,B, AND A REPRESENT THE FOUR INPUTS TO THE DECODER DRIVER (IN BCD 8-4-2-1 CODE) THAT ARE REQUIRED TO PRODUCE THE APPROPRIATE DECIMAL NUMBER ON THE DISPLAY DEVICE.

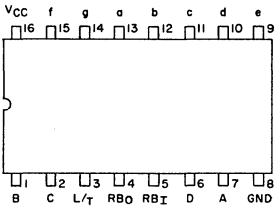
*Fig. 1 - Terminal diagram for the CD2500E or CD2502E decoder-driver.*

## TABLE I – TRUTH TABLE FOR DECODER–DRIVER CIRCUITS

| INPUT 0 = Low Level 1 = High Level | | | | | | | OUTPUT 0 = Filament Lit 1 = Filament OUT | | | | | | | | | DISPLAY |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| D | C | B | A | L/T | $DP_I$ | $RB_I$ | a | b | c | d | e | f | g | $DP_O$ | $RB_O$ | |
| X | X | X | X | 0 | – | X | 0 | 0 | 0 | 0 | 0 | 0 | 0 | – | 1 | 8 |
| 0 | 0 | 0 | 0 | 1 | – | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | – | 0 | |
| 0 | 0 | 0 | 0 | 1 | – | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | – | 1 | 0 |
| 0 | 0 | 0 | 1 | 1 | – | X | 1 | 0 | 0 | 1 | 1 | 1 | 1 | – | 1 | 1 |
| 0 | 0 | 1 | 0 | 1 | – | X | 0 | 0 | 1 | 0 | 0 | 1 | 0 | – | 1 | 2 |
| 0 | 0 | 1 | 1 | 1 | – | X | 0 | 0 | 0 | 0 | 1 | 1 | 0 | – | 1 | 3 |
| 0 | 1 | 0 | 0 | 1 | – | X | 1 | 0 | 0 | 1 | 1 | 0 | 0 | – | 1 | 4 |
| 0 | 1 | 0 | 1 | 1 | – | X | 0 | 1 | 0 | 0 | 1 | 0 | 0 | – | 1 | 5 |
| 0 | 1 | 1 | 0 | 1 | – | X | 0 | 1 | 0 | 0 | 0 | 0 | 0 | – | 1 | 6 |
| 0 | 1 | 1 | 1 | 1 | – | X | 0 | 0 | 0 | 1 | 1 | 1 | 1 | – | 1 | 7 |
| 1 | 0 | 0 | 0 | 1 | – | X | 0 | 0 | 0 | 0 | 0 | 0 | 0 | – | 1 | 8 |
| 1 | 0 | 0 | 1 | 1 | – | X | 0 | 0 | 0 | 0 | 1 | 0 | 0 | – | 1 | 9 |
| 1 | 0 | 1 | 0 | 1 | – | X | 1 | 1 | 1 | 1 | 1 | 1 | 1 | – | 1 | |
| 1 | 0 | 1 | 1 | 1 | – | X | 1 | 1 | 1 | 1 | 1 | 1 | 1 | – | 1 | |
| 1 | 1 | 0 | 0 | 1 | – | X | 1 | 1 | 1 | 1 | 1 | 1 | 1 | – | 1 | |
| 1 | 1 | 0 | 1 | 1 | – | X | 1 | 1 | 1 | 1 | 1 | 1 | 1 | – | 1 | |
| 1 | 1 | 1 | 0 | 1 | – | X | 1 | 1 | 1 | 1 | 1 | 1 | 1 | – | 1 | |
| 1 | 1 | 1 | 1 | 1 | – | X | 1 | 1 | 1 | 1 | 1 | 1 | 1 | – | 1 | |
| – | – | – | – | 1 | 1 | – | – | – | – | – | – | – | – | 0 | – | . |
| – | – | – | – | 1 | 0 | – | – | – | – | – | – | – | – | 1 | – | |
| – | – | – | – | 0 | X | – | – | – | – | – | – | – | – | 0 | – | . |

X – 0 or 1 entry has no effect
L/T = Lamp Test
$RB_I$ = Ripple Blanking Input
$RB_O$ = Ripple Blanking Output

$DP_I$ = Decimal Point Input
$DP_O$ = Decimal Point Output




RBO = RIPPLE-BLANKING OUTPUT AND INTENSITY CONTROL INPUT

RBI = RIPPLE-BLANKING INPUT

D, C, B, AND A REPRESENT THE FOUR INPUTS TO THE DECODER DRIVER (IN BCD 8-4-2-1 CODE) THAT ARE REQUIRED TO PRODUCE THE APPROPRIATE DECIMAL NUMBER ON THE DISPLAY DEVICE.

*Fig. 2 - Terminal diagram for the CD2501E or CD2503E decoder-driver.*

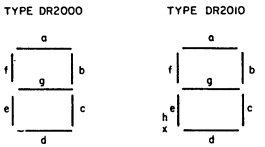



*Fig. 3 - Segment arrangement and designations for two 7-segment incandescent display devices.*

8, are connected in four pairs to provide the BCD data and the complements of these data to the input of ten NAND gates, Nos. 10 through 19. The ten NAND gates decode the data into their mutually exclusive outputs that represent the decimal numbers from 0 through 9 only; any BCD data that

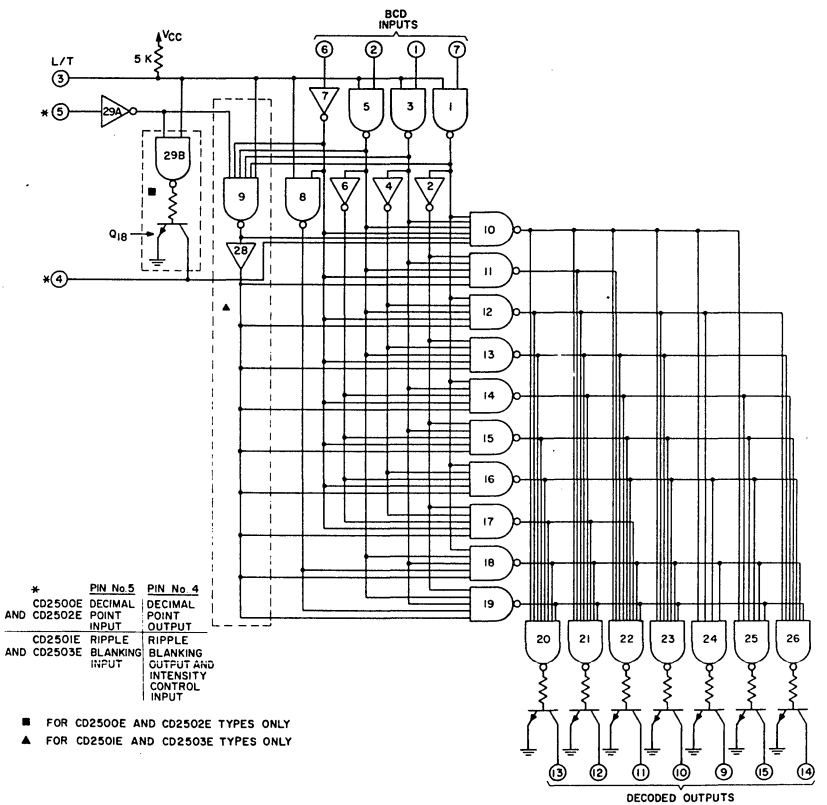



*Fig. 4 - Logic diagram for the BCD-to-7-segment decoder drivers.*

correspond to a number greater than 9 is inhibited. The outputs of these ten NAND gates are then encoded into seven outputs used to control the operation of a 7-segment incandescent display device by seven additional NAND gates, Nos. 20 through 26. The outputs of these seven NAND gates are applied through seven open-collector transistors that provide high current-sink capability and make possible direct-driving of the display device.

### Decimal-Point Output

In the CD2500E and CD2502E decoder-drivers, gates Nos. 29A and 29B, shown in Fig. 4, develop a decimal-point output ($DP_O$) in response to a decimal-point-input ($DP_I$) control signal supplied from an external source. Transistor Q18 provides the inverter-driver function required to energize the decimal-point filament on the display device. This unique feature eliminates the necessity for separate external decimal-point driving circuitry.

### Ripple-Blanking Function

The ripple-blanking feature of the CD2501E and CD2503E decoder-drivers allows suppression of leading- and/or trailing-edge zeroes in a multidigital display. This action does not affect the numerical value and provides easier reading of the decimal display.

The ripple-blanking function is performed by gates Nos. 9, 28, and 29A, shown in Fig. 4. The ripple-blanking input ($RB_I$) is inverted by gate No. 29A and applied to gate No. 9. Gate No. 28 is used as a buffer for gate No. 9. When the ripple-blanking input is at logical "0", gate No. 29A provides a logical "1" at the input of the ripple-blanking gate No. 9. Gate No. 9 also receives the complements of the BCD input data. This gate provides an inhibiting function for the decimal zero. When this inhibiting function occurs, i.e., when the ripple-blanking input ($RB_I$) and the BCD inputs are at logical "0", the ripple-blanking output ($RB_O$) goes to a logical "0", and all seven segment outputs to a logical "1". A logical "1" of the seven-segment output corresponds to the filament-off condition on the incandescent display device.

The ripple-blanking output terminal may also be used to provide an over-riding blanking input, regardless of other input conditions. When the ripple-blanking output is maintained at a logical "0", it inhibits all seven segment outputs, i.e., the segment outputs are maintained at a logical "1". For operation with a fixed lamp power supply, the ripple-blanking output may be used with external resistor-pull-up output gates to control lamp intensity by control of the pulse width of the gate input signal.

### Lamp-Test Function

All four BCD-to-7-segment decoder-drivers include a lamp-test (L/T) input for use in testing the filaments of the display device. This input is normally maintained at a logical "1" by an internal resistor (no external circuit elements are required for the lamp-test function). For the lamp test, the L/T terminal is grounded. All segment outputs are then maintained at a logical "0", so that all lamp filaments on the display device are lighted. For the CD2500E and CD2502E, which include a decimal-point output, the L/T terminal can be grounded at any time to test all filaments in the display device including the filament for the decimal point. For the CD2501E and CD2503E, which include a ripple-blanking feature, care must be taken to assure that the ripple-blanking output is not grounded externally during the lamp test; otherwise, the test is performed in the same way as for the types CD2500E and CD2502E.

## OPERATING CHARACTERISTICS

All inputs (terminals 1, 2, 5, 6, and 7) of the CD2500E-series decoder-drivers are TTL types and include clamp diodes to prevent the ringing that may result when long interconnecting leads are used. Fig. 5 shows an equivalent circuit for any one of these inputs.

Each output (terminals 9 through 15 and also terminal 4 of the CD2500E and the CD2502E) of the BCD-to-7-segment decoder-drivers consists of an open-collector transistor, together with its collector-to-substrate diode, as shown in Fig. 6. These outputs, in standard CD2500E-series devices, are specified to withstand up to 8 volts at a maximum collector-to-emitter leakage current of 200 microamperes over the operating temperature range. The transistor has a minimum collector-to-emitter breakdown voltage $V_{(BR)CEO}$ of 12 volts at a collector-to-emitter current $I_{CEO}$ of 10 milliamperes. The output circuit, therefore, can safely withstand any load at supply voltages up to 8 volts without the occurrence of a dc-latched condition; damage to the output transistor because of excessive power dissipation is, therefore, avoided. The probability of an ac-latched condition depends upon the type

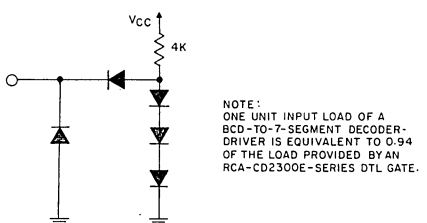



*Fig. 5 - Equivalent input circuit at terminals 1, 2, 5, 6, and 7 of the decoder-drivers.*

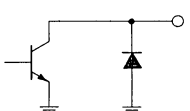


*Fig. 6 - Equivalent output circuit at terminals 9 through 15 (and terminal 4 of the CD2500E and the CD2502E) of the decoder-drivers.*

of load used. The circuit may become ac-latched during operation with a large inductive load. The "rule of thumb" for minimization of this probability is to ensure that the sum of the supply voltage and the counterelectromotive force developed across the lamp filament inductance does not exceed the collector-to-emitter breakdown voltage $V_{(BR)CEO}$ of the transistor.

For applications in which the output voltage may exceed the specified value of 8 volts, such as multiplex operation of RCA Numitrons, special selections of the CD2500E-series decoder-drivers are available.

The ac line voltage may also be used as the segment-voltage (lamp) supply provided that it is either half-wave or full-wave rectified so that only positive alternations remain. This type of rectification is necessary because the output transistors of the decoder-drivers cannot sustain negative voltages greater than 0.5 volt. Fig. 7 shows the relationship of the output voltage to the segment and decimal-point output currents of the CD2500E-series decoder-drivers.

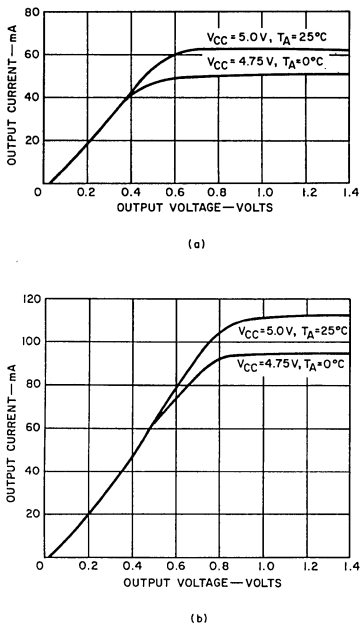



*Fig. 7 - Relationship between segment and decimal-point output current (logical "0" state) and output voltage: (a) segment output currents for the CD2500E and CD2501E and decimal-point output current for the CD2500E; (b) segment output currents for the CD2502E and CD2503E and decimal-point output current for the CD2502E.*

Fig. 8 shows an equivalent circuit of the ripple-blanking output (terminal 4). When the BCD code represents decimal zero and the ripple-blanking input (terminal 5) is at a logical "0", transistor Q then turns on and provides blanking of the decimal zero. When the BCD code represents a decimal number between 0 and 9, transistor Q is open-circuited. When the BCD code represents a number greater than 9, transistor Q and diode A are both open-circuited, and the ripple-blanking output circuit consists of only the 2-kilohm resistor between terminal 4 and the $V_{CC}$ supply.

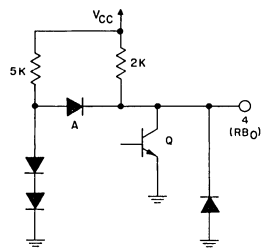



*Fig. 8 - Equivalent circuit for the ripple-blanking output (terminal 4) of the CD2501E and CD2503E decoder drivers.*

Supply- and ground-line noises can be effectively removed by addition of sufficient capacitance between the $V_{CC}$ and ground lines, as near as possible to the integrated-circuit terminals. Use of separate integrated-circuit and display-device dc power supplies, although not an essential requirement, is recommended. The advantage of separate supplies is that the noise generated by high transient currents that result from lamp switching would be reduced.

## DISPLAY-LAMP TURN-ON CHARACTERISTICS

The turn-on characteristics of the display lamps is an important factor in the operation of the decoder-drivers. The main consideration in these turn-on characteristics is the lamp in-rush current. For most incandescent lamps, the in-rush current may be several times greater than the normal operating current because the resistance of a cold filament is much less than that of the same filament after it has been heated to the normal operating temperature. Fig. 9 shows that the initial current of the RCA DR2000 Numitron is approximately five times greater than the normal operating current and that 2 milliseconds is required for the in-rush current to decrease to one-half the initial value. The output transistors of the decoder-drivers, therefore, must be able to handle large surge currents that are several times greater than the normal operating current of the incandescent display device. If desired, a resistor may be connected between each segment output terminal of the decoder-driver and ground so

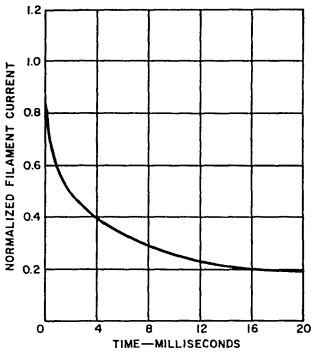
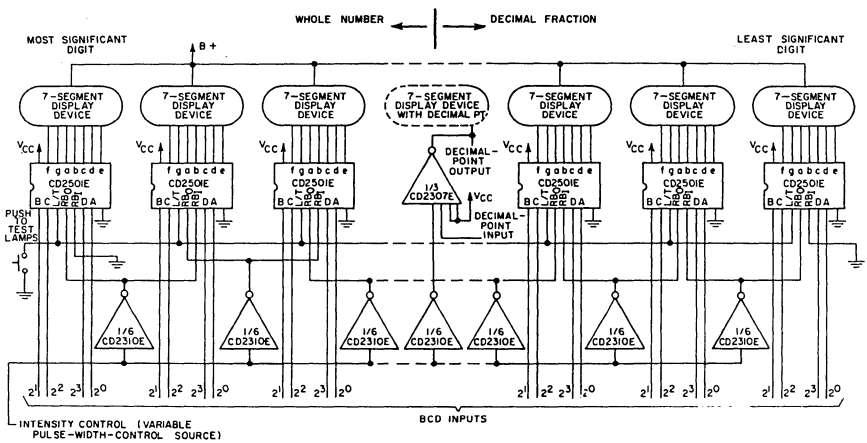



*Fig. 9 - Turn-on characteristics for an RCA DR2000 Numitron.*

that a small current is allowed to flow through the lamp filament during the lamp off period. This current should be sufficient to keep the filament warm, but not sufficient to illuminate the lamp. In this way, a high initial in-rush current can be avoided during the lamp turn-on period.

## STATIC-DRIVE APPLICATIONS

The zeroes that have no value at both ends of a multidigital display can be suppressed by grounding the $RB_I$ terminal of the most significant digit of the whole number and the least significant digit of the fraction, as shown in Fig. 10. The $RB_O$ of the most significant digit is connected to the $RB_I$ of the next lower digit, and the $RB_O$ of this latter digit is, in turn, connected to the $RB_I$ of the following digit. The $RB_O$ of the least significant digit of the fraction side is connected to the $RB_I$ of the next higher digit, and so on. Therefore, for the whole number, the ripple signal flow originates from the most significant digit, and for the fraction, the ripple signal flow starts from the least




CHARACTERISTICS OF THE DISPLAY DEVICES

| DISPLAY DEVICE TYPE | TYPE OF DISPLAY | CHARACTERISTICS |
|---|---|---|
| DR2000 | 8 | REQUIRED DRIVING CURRENT • 24 ±2 mA PER SEGMENT |
| DR2010 | 8 | LETTER HEIGHT • 0.6 INCH |

*Fig. 10 - Typical ripple-blanking and intensity-control application using the CD2501E decoder driver with a 7-segment incandescent display device, such as the RCA DR2000 or DR2010.*

significant digit. As soon as the BCD data inputs for a non-zero digit is encountered, the corresponding $RB_O$ output assumes a logical "1" state, and any further signal rippling is inhibited. For example, the number 0102,0110 would be displayed as 102.011. The $RB_I$ of the least significant digit of the whole number and the $RB_I$ of the most significant digit of the fractional portion should be left open, because the suppression of zeroes in these two digits is not desirable in practice, e.g., 000.200 would be displayed as 0.2, and 000.000 would be 0.0.

The ripple-blanking arrangement described above is employed in the standard multiple-digit display. For other applications, however, ripple blanking may be used to blank out zeroes serially in time, as shown in Fig. 11. For this type of blanking, the ripple-blanking input $RB_I$ and the ripple-blanking output $RB_O$ are connected together. Fig. 11 shows that the zeroes that occur at time frames $t_1$ and $t_2$ are blanked out, and those that occur at time frames $t_4$ and $t_6$ are not. A ground-level strobe pulse must be injected at the

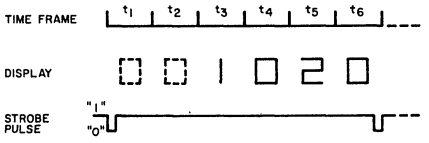



*Fig. 11 - Timing diagram for ripple blanking that occurs serially in time.*

connection of the $RB_I$ and $RB_O$ terminals to cause these terminals to be latched at the logical "0" level. This strobe pulse initiates the blanking operation. The $RB_I$ and $RB_O$ terminals are maintained at the "0" level until the BCD input data for a non-zero digit is applied. The $RB_I$ and $RB_O$ terminals are then shifted to a logical "1" level, and further zero blanking is inhibited.

The ripple-blanking output can also be used simultaneously as an intensity-control input when the lamp power-supply voltage is fixed. For this intensity-control effect, external gates are required, and an RCA CD2310E DTL type is chosen for this purpose, as shown in Fig. 10. The intensity control is achieved by variation of the pulse width of the signal at the intensity-control input ($RB_O$ terminal). Pulse-width-controlled flip-flops can be used as the source for the intensity-control input. The logical "0" state of the external gates at the point of connection to the intensity control terminal should not be greater than 0.35 volt. For the CD2500E and CD2502E decoder-drivers, intensity control can be provided by variation of the segment power-supply voltage. Fig. 12 shows the relative light output of an RCA DR2000 Numitron at 50Hz as a function of pulse duty cycles for operation with a supply voltage of +5 volts.

The CD2500E decoder-driver is frequently used in counting applications, as shown in Fig. 13. A display-hold circuit is included to hold counts for the display device while

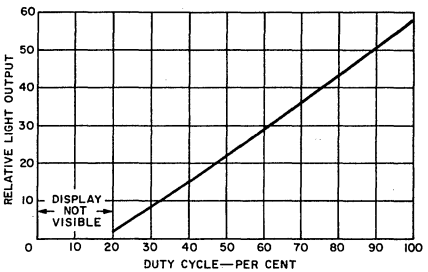



*Fig. 12 - Relative light output of a DR2000 Numitron at 50 Hz as a function of pulse duty cycle for operation from a lamp-supply voltage of 5 volts.*

the input count continues. The display-hold signal is usually synchronized with the count input signal. The hold circuit, which can be formed by use of latching flip-flops, is used because no data storage is provided in the decoder-driver. The decoder-driver simply operates as a slave circuit for the input data; the outputs of the decoder-driver, therefore, follow directly any change in the data applied to its inputs.

Fig. 14 illustrates the use of six CD2301E stages in a floating-decimal-point application. The selection of a decimal point requires that the corresponding decimal-point-select

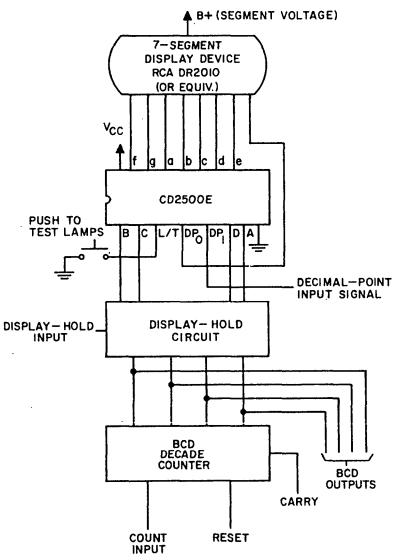



*Fig. 13 - Counting circuit using the CD2500E decoder-driver.*

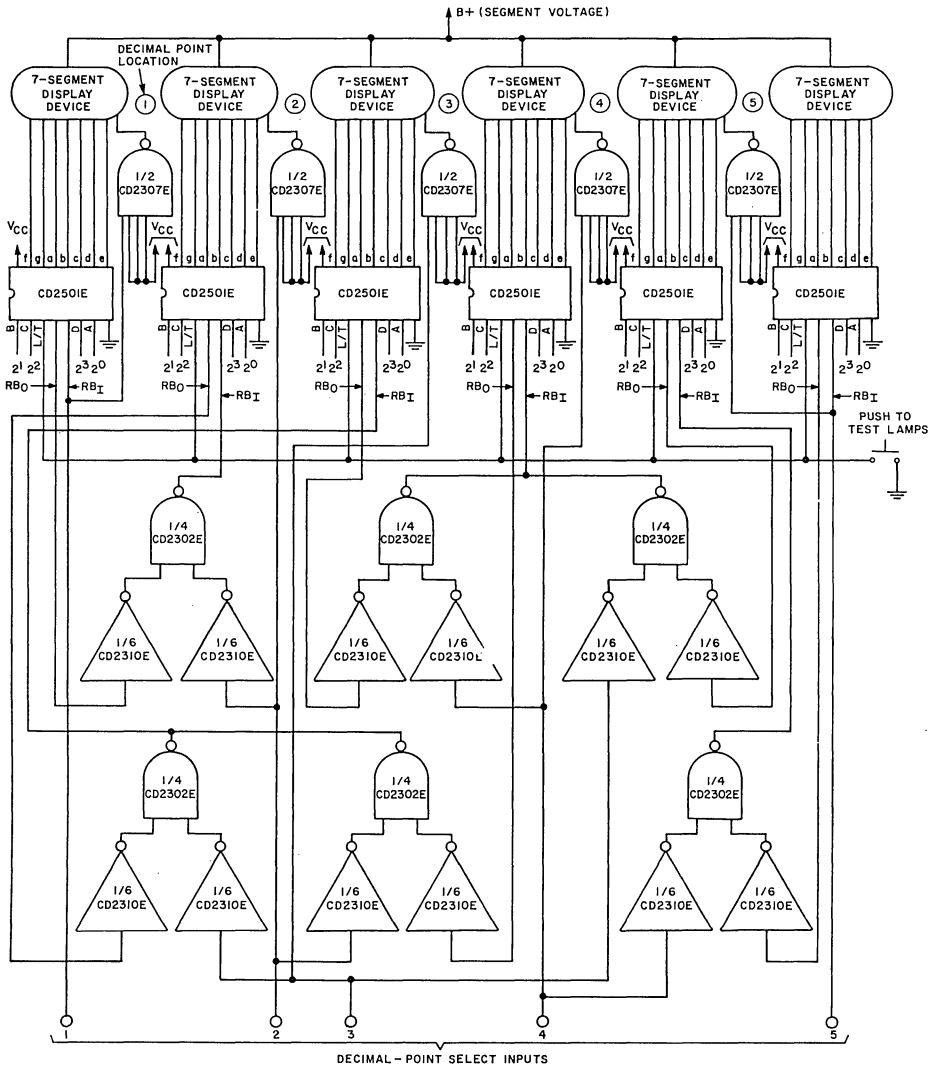



*Fig. 14 - Floating-decimal-point application using six CD2501E decoder-drivers.*

input be held at logical "1" with the other decimal-point-select inputs at logical "0". The operation is similar to the ripple-blanking application shown in Fig. 10, in which the flow of the ripple signals always starts from the extreme ends and move toward the chosen decimal point. The ripple input of the immediately adjacent stages on either side of the decimal point is made a logical "1" by the external gates, so that the ripple signal flow is terminated at these points and, therefore, cannot suppress zeroes in the two digits adjacent to the chosen decimal point.

The RCA CD2307E gate is used to energize the decimal-point filament in the display device, and CD2302E and CD2310E gates are used to enable the ripple-blanking circuits to blank out the no-value zeroes.

## MULTIPLEX MODE OF OPERATION

In the standard static-drive application, a given number of display devices requires an equal number of decoder drivers for simultaneous display of the BCD data. In the time-multiplex system, however, one decoder-driver can be operated to drive a number of display devices sequentially with no noticeable flicker when the multiplexing repetition rate is greater than 50Hz. Fig. 15 shows a typical application of the CD2502E decoder-driver in the multiplexing mode of operation.

The complementary BCD data information is fed to the multiplexing NAND gate inputs and multiplexed in sequence by the trains of pulses, shown in Fig. 16, obtained from a ring counter. The complementary BCD data available at the input of a given set of multiplexing NAND gates during the pulse duration is inverted to BCD data and applied to the decoder driver. This decoder data, in turn, causes the proper decoder-driver output transistor to turn on. At the same time, the pulse complement is fed to the corresponding digit control gate, as shown in Fig. 15, so that the associated transistor $Q_m$ is caused to conduct and provide segment current to the appropriate filaments of the display device.

Isolation diodes are required in series with each segment coil of the display devices, to prevent "sneak paths" which would simultaneously light segment coils of adjacent devices. In this circuit, one CD2502E 7-segment decoder-driver, which is specially selected for an output voltage rating $V_{oh}$ of 12 volts, can be used to drive up to a maximum of six DR2010 Numitrons with a 16.7 per cent duty cycle. When the specially selected CD2503E is used, a blanking circuit may be incorporated at the ripple-blanking input terminal to blank out the no-value zeroes, if desired. Care must be taken to ascertain that, during multiplexing operation, the breakdown-voltage rating and the maximum output current rating of the decoder-driver are not exceeded, and transistor $Q_m$, shown in Fig. 15, must be carefully chosen to handle the maximum current required.

From the standpoint of packaging, troubleshooting, and system reliability, the static-drive mode of operation is generally preferable to the multiplexing mode. However, on the basis of the present costs of a decade that includes a decade counter and a readout device, an economic advantage can result for a display that employs more than six readout devices when the readout devices are multiplexed so that only one decoder driver is required. With the advances being made in integrated-circuit technology and as the demand for readout devices increases, it is anticipated that, during the next few years, the cost of decade devices will decrease to less than one-half the present cost. The multiplexing mode of operation then will no longer offer a significant economic advantage and will become even less desirable.

## FAIL-SAFE CIRCUIT

Fig. 17 shows the diagram of a circuit designed to monitor the currents through filaments a, b, e, f, and g (refer to Fig. 3) of a display device. If any one of these five filaments should fail (open), the complete digit being displayed will be blanked out to avoid incorrect readings. Filaments c and d are not monitored, because failure of either of these filaments is readily indicated by incomplete or distorted digit displays.

With this circuit included in the display system, the standard lamp test can still be performed at any time. Moreover the over-range blanking provided by all four decoder-driver circuits and the ripple-blanking feature of the CD2501E and CD2503E circuits are not affected by the fail-safe circuit.

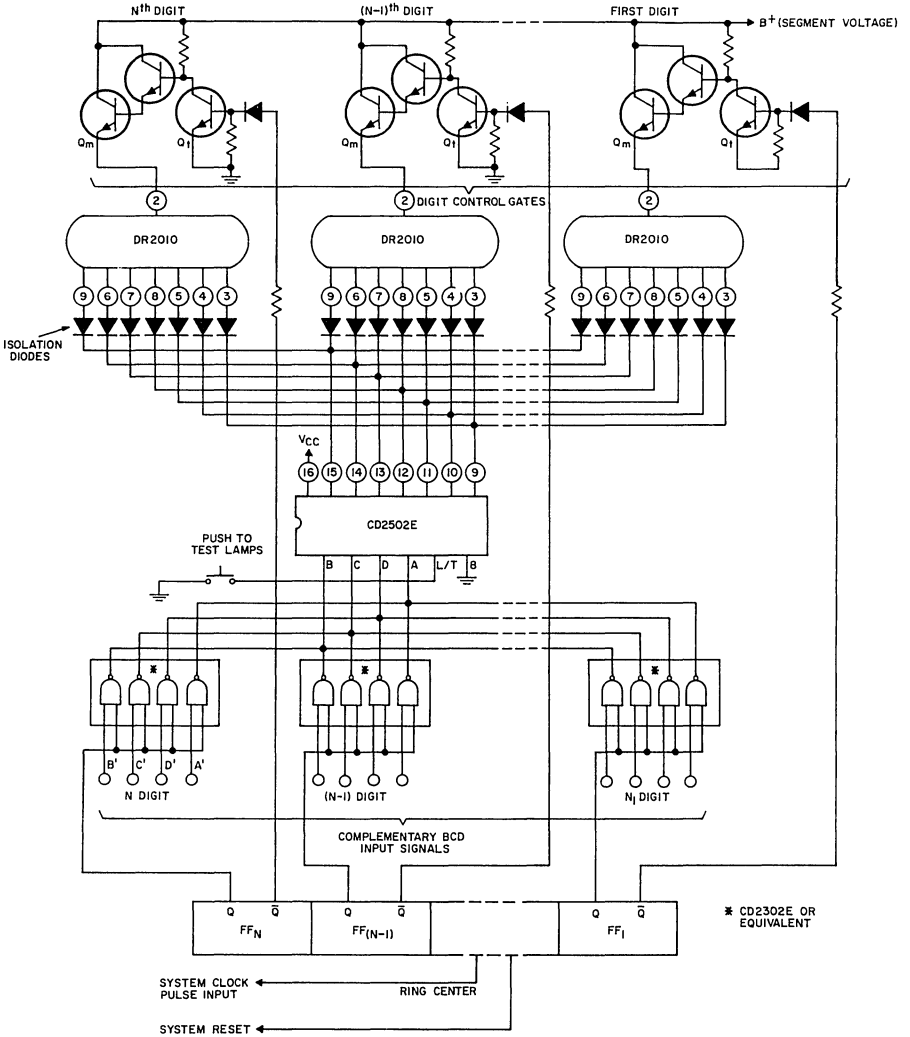



*Fig. 15 - Typical multiplexing system using the CD2502E decoder-driver.*

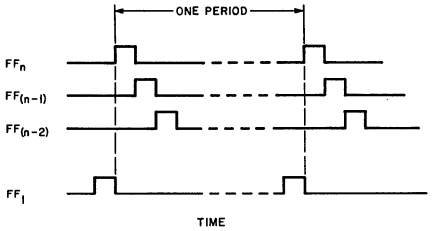



*Fig. 16 - Timing relationship of the pulse trains supplied by the ring counter in the multiplexing system shown in Fig. 15.*

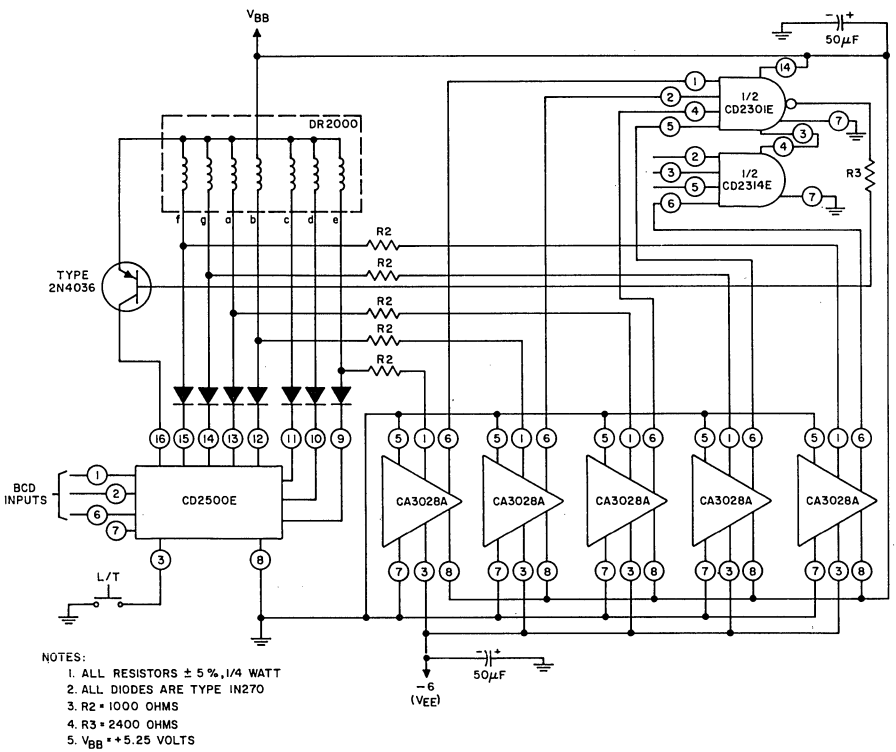



*Fig. 17 - Fail-safe circuit designed to monitor filaments of the display devices.*

# Description and Application of the RCA-CA3120E Integrated-Circuit TV-Signal Processor

by W. Sensenig

The RCA-CA3120E is a 16-pin, dual-in-line, monolithic-silicon integrated circuit that processes a video signal and provides the following outputs:

Non-inverted video output
Noise-processed, inverted video output
Dual-polarity, composite synchronization signals
Automatic gain-control signals (agc):
  Undelayed forward agc for i f amplifier
  Delayed forward agc for tuners with bipolar transistors
  Delayed reverse agc for tuners with FET's

The IC, which can be used in color or monochrome TV receivers, requires a single-polarity power supply (positive) and includes impulse noise inversion and delay circuits that reduce the deleterious effects of impulse noise in the receiver agc and synchronization (sync) circuits. Standard agc strobing techniques are also used. The agc and impulse-noise thresholds are automatically set and require no controls. The i f maximum-gain bias and the tuner agc delay may be adjusted for optimum TV-receiver performance; the time constant for the sync-separator input can also be optimized by the set designer.

## CIRCUIT DESCRIPTION

Fig. 1 is a simplified block diagram of the CA3120E signal processor; the circuit consists of four major blocks:

1. Noise processor circuit
2. AGC circuit
3. Synchronizing separator circuit
4. Internal dc reference supplies

An emitter-follower output is also provided for the un-processed video signal (non-inverted). The four circuits are used to generate the output sync and agc signals as described below.

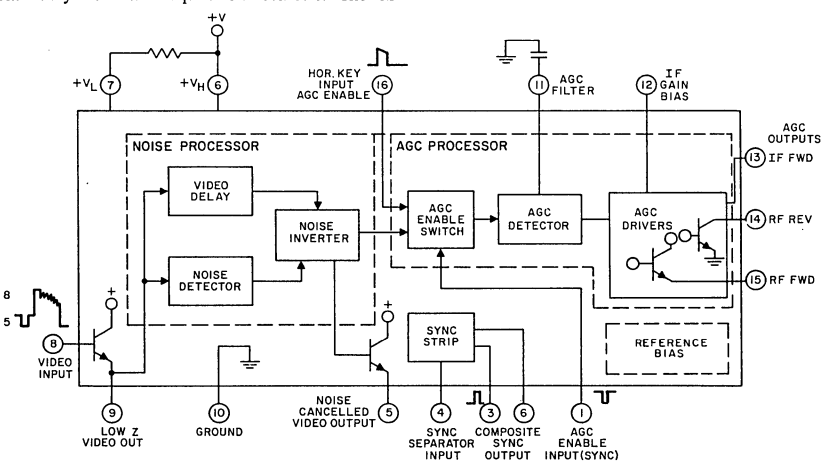



*Fig. 1. Simplified block diagram of the CA3120E signal processor.*

### Noise Processor

The function of the noise processor is to reduce the effect of impulse noise interference (from automobile ignition, etc.) on the agc and synchronizing circuits of the TV receiver. Fig. 2 is a simplified schematic diagram of the noise processor. The input video signal applied at terminal 8 is white, positive-going with sync tips at $V_{TH}$ (the agc threshold-voltage level), which is approximately 5 volts. The unprocessed video output signal from the emitter of Q1 is available at terminal 9. The video signal from the emitter of Q1 is also connected to the base of Q2. In the absence of any negative-going noise pulse, Q2 functions as an emitter follower, and transistors Q3, Q5, and Q12 are cut off. The output of emitter-follower Q2 is connected to the video RC delay line consisting of R42 through R49 and the emitter base capacitors of multiple-emitter transistor Q6.

The delayed video signal (delay is approximately 300 nanoseconds) at the emitter of Q14 is shown in Fig. 3(b). If negative-going impulse noise crosses the noise threshold voltage (approximately 1.8 volts below $V_{TH}$), transistor Q3 conducts and turns on transistors Q5 and Q12. Transistor Q5 generates a noise-cancelling pulse whose duration is approximately 500 nanoseconds wider than the detected noise pulse, as shown in Fig. 3(d). Pinch resistor R7 limits the amplitude of the generated pulse. Transistor Q17 limits the amplitude of the impulse noise through the delay channel, as shown in Fig. 3(b).

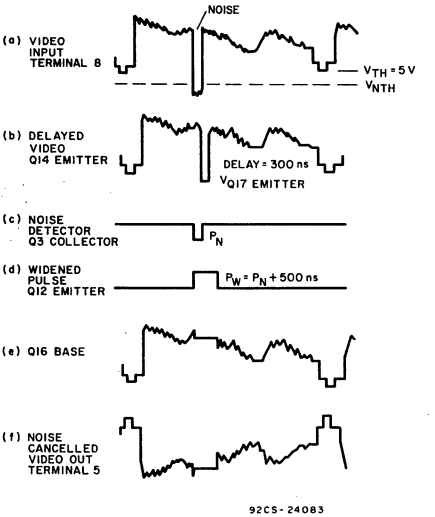



*Fig. 3. Operating waveforms for the noise processor.*

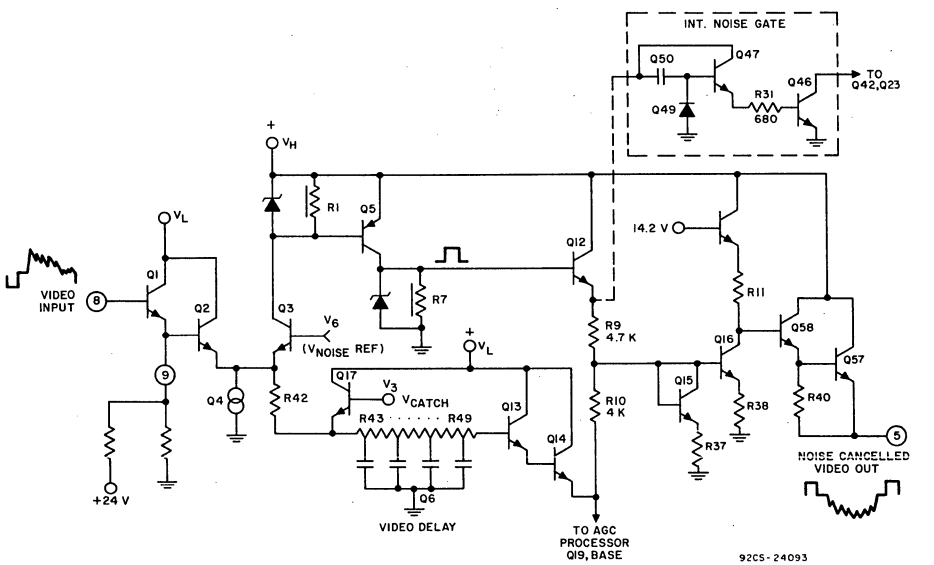



*Fig. 2. Simplified schematic diagram of the noise-processor section of the CA3120E.*

The delayed video at the emitter of Q14 and the generated noise pulse are summed at the input to current amplifier Q15, Q16. Transistor Q16 inverts and amplifies the noise-processed video signal. Since the video signal has been delayed approximately 300 nanoseconds and the noise pulse has been stretched approximately 500 nanoseconds, the output of the combined signal (at emitter follower Q57) no longer contains impulse noise signals. The derived noise-gating pulse "surrounds" and effectively eliminates the effects of the impulse noise, as shown in Fig. 3(f).

After amplification, inversion, and buffering, the noise-processed video signal is available at terminal 5 for use in the sync-separator stage. The peak-to-peak amplitude of the signal is approximately twice the amplitude of the video signal at terminal 8. The dc level of the sync tip at terminal 5 is approximately 8.5 volts. The agc generator uses the delayed video to generate the agc voltage. In the CA3120E, an ac-coupled noise gate disables the agc generator for approximately 10 microseconds under heavy noise conditions. The noise gate from the emitter of Q12 is connected to transistor Q50, which acts as a monolithic capacitor. Q49 is used as a dc restorer. Emitter follower Q47 feeds control transistor Q46, which disables the agc generator for the duration of the noise gate pulse. AC coupling is used to prevent agc lockout.

### AGC System

The function of the agc system is to provide control voltage to the i f and tuner stages of the TV receiver, the amount of voltage is a function of the amplitude of the detected video signal; thus a constant-amplitude video signal is maintained.

The CA3120E agc amplifier uses a sample and hold system to develop the required agc bias voltages. The sync-tip voltage is compared to an internal reference voltage during the horizontal synchronization (retrace) interval. A coincidence-gate circuit is included to compare the timing of the synchronizing pulse with a horizontal keying pulse derived from the horizontal flyback transformer.

Fig. 4 is a simplified schematic diagram of the agc generator. The delayed video signal from the emitter of Q14 is connected to the base of the agc-gated comparator-amplifier Q19, Q20. In normal operation, Q21 is turned on during the horizontal retrace period, thus enabling the comparator, and the dc level of the sync tip is compared to reference voltage V5. The difference between the sync and reference voltages is amplified and fed to current amplifiers Q24, Q25. The output of Q25 is used to charge the external agc filter capacitor connected to terminal 11. Transistor Q23 is also gated on during the retrace interval, and provides a constant rate of discharge to the agc filter capacitor connected to terminal 11. The net capacitor charge is the difference between the charge current and the discharge current for a given offset voltage condition at the comparator. If the antenna signal decreases to a lower level and is held constant, the detector output voltage will decrease; this decrease in the voltage causes the charge current to decrease. As the capacitor is discharged, the TV-system gain is increased to the value where equilibrium is reached, and the charge current again equals the constant discharge current.

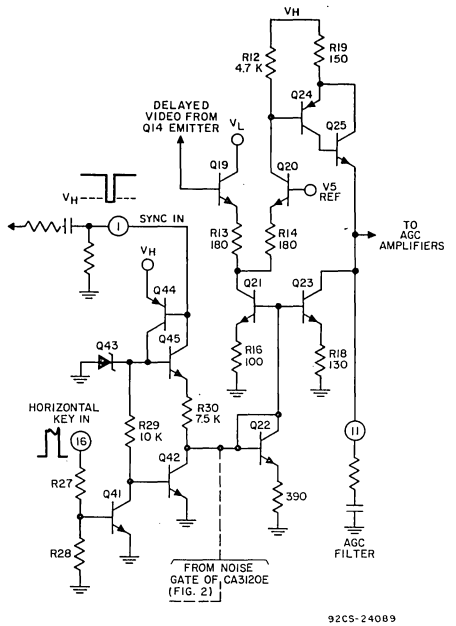



*Fig. 4. Simplified schematic diagram of the agc generator.*

Since the discharge current is constant, the same offset voltage will appear at the comparator. By this action, the offset between the sync tips and the agc threshold is held nearly constant.

To provide noise immunity for the agc system and to assure that only the delayed-video sync tips are sampled, agc strobing is employed. This technique prevents the detected video from being sampled by the agc comparator when the TV system is out of horizontal sync, as a result of changing channels for example. If the video were sampled with the TV system out of horizontal sync, the detector output would contain picture modulation components which would cause horizontal-synchronization problems. This effect grows worse as the agc time constant is reduced to provide the rapid agc action required to counteract doppler modulation of the TV signal resulting from multipath reflections of aircraft.

The agc coincidence strobing system is also shown in Fig. 4. Negative sync signals are ac coupled to the latch circuit consisting of Q44, Q45, and Q43. The tip of the sync signal is clamped at the base potential of Q44, which is one $V_{BE}$ below the supply voltage $V_{CC}$. During the sync period when Q44 is turned on, the base potential of Q45 is increased to the zener voltage of Q43 (approximately 7 volts). A current of approximately 0.8 milliampere then flows from the emitter of Q45 through R30. If the horizontal key pulse is not simultaneously present, this current is bypassed through transistor Q42 to ground, and the agc comparator remains off. The agc filter capacitor remains at its original potential.

Under conditions of synchronization, transistor Q41 is turned off, and the current from Q45 through R30 is diverted to current mirror Q22. Constant-current transistor Q21 and Q23 are turned on, thus enabling the agc comparator and the filter-capacitor charge/discharge current generators. To prevent agc lockout during turn-on or channel changes, ac coupling must be employed to sync input terminal 1.

The agc output stages are shown in Fig. 5. The agc filter-capacitor voltage at terminal 11 is connected to Darlington transistors Q28 and Q29. A bias voltage applied at the base of transistor Q26 (terminal 12) will set the minimum voltage on the filter capacitor connected to terminal 11. The potential at terminal 11 (minus $1V_{BE}$) is transferred to the emitter of p-n-p transistor Q31 and terminal 13, the forward agc output terminal for the i f amplifier. The potential at terminal 12 is selected by the TV receiver designer to provide the "no-signal", maximum, i f gain bias. As the TV input-signal amplitude increases, the potential at terminal 11 rises, and forward bias is applied to the receiver i f amplifier from the emitter of Q31 at terminal 13. Tuner delay bias is also applied to the emitter of Q31 at terminal 13. As shown in Fig. 6, no change in output voltage occurs at terminal 14 or 15 at the low and intermediate signal-level conditions represented by abscissa points A and C. The tuner(s) will operate at maximum gain and provide good signal-to-noise ratios at these equivalent input-signal levels.

Point C, Fig. 6, is a turnover point determined by the open-circuit potential of the tuner delay-bias voltage divider. As shown in Fig. 5, the voltage divider acts as a load for emitter follower Q31. As long as the emitter of transistor Q29 is at least one $V_{BE}$ drop less than the open-circuit delay-bias voltage, transistor Q31 performs as an emitter follower, and

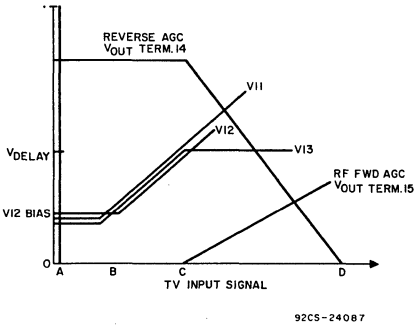



*Fig. 6. AGC transfer curves.*

forward-i f control voltage is developed. At higher signal levels, the voltage at the emitter of Q29 increases and Q31 turns off; further change in the i f agc output is inhibited (for good dynamic range) and the forward and reverse agc outputs of the turner are activated (represented by points C and D in Fig. 6). As shown in Fig. 5, at signal levels below the turnover point, the emitter potential of Q32 is equal to and follows the emitter potential of Q29. Above the turnover point, the emitter potential of Q32 is fixed by the tuner-delay voltage divider, and consequently the current of transistor Q35 is fixed, as determined by mirror-transistor Q34. Further increases in signal level turn on amplifier Q36, which in turn drives the two agc output amplifiers in the tuner. Transistors Q39 and Q40 provide the delayed forward agc output at

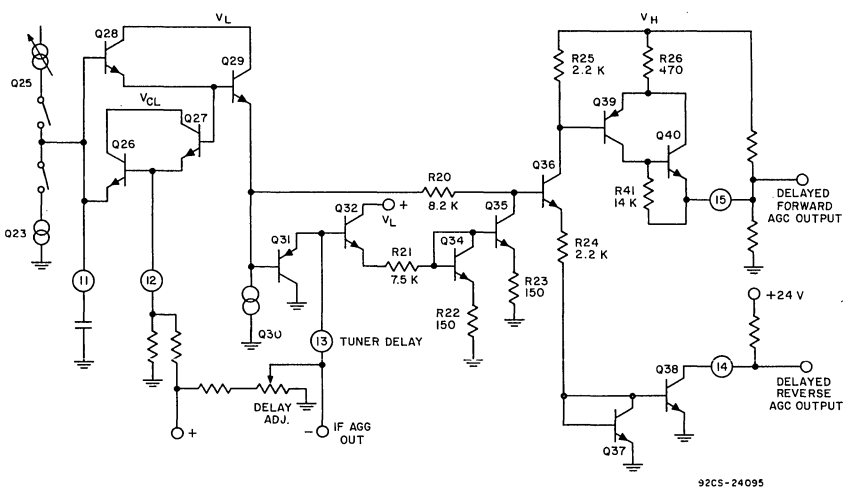



*Fig. 5. AGC output stages.*

terminal 15 for use with tuners using n-p-n transistors. Transistors Q37, Q38 provide the reverse agc output at terminal 13 for use with tuners using MOSFET's or vacuum tubes. Note that in forward-type agc systems, increased signal into the tuner results in increased agc voltage. The increased agc voltage decreases the gain of the amplifier by reducing the collector-to-emitter voltage of the amplifier as a result of the increased base-to-emitter potential. In reverse-type agc systems, increased signal into the tuner results in decreased agc voltage. The decreased voltage reduces the transconductance of the amplifier, thus reducing its gain.

### Sync Separator

The schematic diagram of the sync separator is shown in Fig. 7. The sync-separation stage Q56 clamps the sync tips to

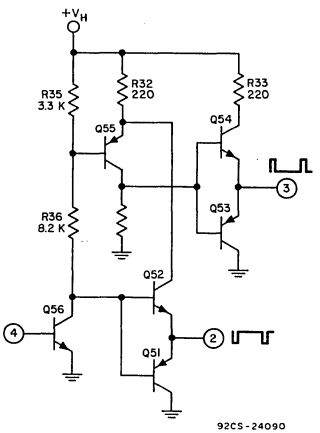



*Fig. 7. Schematic diagram of the sync separator.*

the forward bias reference potential (approximately 0.7 volt) of the base-emitter junction, and amplifies the stripped portion of the sync signal to provide dual-polarity sync-signal outputs at terminals 2 (negative) and 3 (positive). The output signals are derived from low-impedance, complementary, emitter-follower stages. Full-amplitude sync signals are generated if the input signal current at terminal 4 is 100 microamperes.

### Reference Bias

The excellent performance of the CA3120E is based upon matching of $V_{BE}$ voltage drops and control of voltage references and resistance ratios. Fig. 8 is a simplified schematic diagram of the reference-bias supplies.

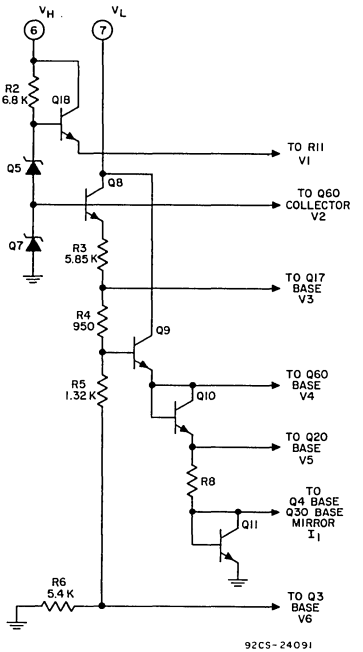



*Fig. 8. Simplified schematic diagram of the reference-bias supplies.*

## APPLICATION OF THE CA3120E

Fig. 9 shows a typical application of the CA3120E. The video input at terminal 8 is direct coupled to the second detector of the TV receiver. The video signal should be white positive and have an amplitude of approximately 3 volts peak-to-peak. The dc level of the sync tips, agc threshold voltage ($V_{TH}$), is approximately 5 volts. This level will be maintained by the closed loop of the agc system which includes the CA3120E and the receiver rf and i f amplifiers.

Fig. 6 illustrates the operation of the agc circuits. Under very-low amplitude (or zero amplitude) signal conditions, terminal 12 is biased to approximately 4.9 volts by the voltage-divider network at terminal 12. The agc filter capacitor (at terminal 11) is charged to a potential one $V_{BE}$ below the bias potential. The i f -agc output level at terminal 13 is two $V_{BE}$ drops (approximately 1.4 volts) below the bias voltage on terminal 12. This bias voltage represents the maximum receiver-gain condition. As the input signal is increased (represented by line-segment BC in Fig. 6) the capacitor is charged to a higher potential and the i f -agc control potential at terminal 13 also increases, thus applying forward agc to the i f amplifier, as shown in Fig. 10. The rf stage of the tuner

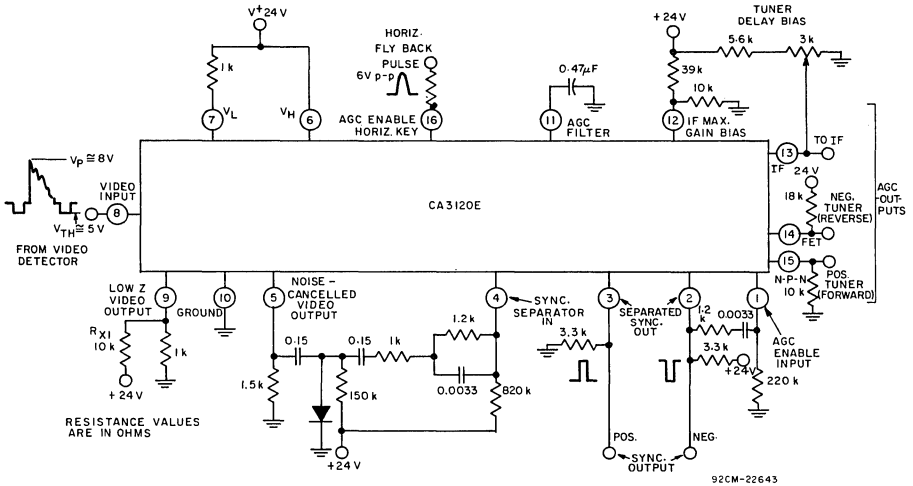



*Fig. 9. Typical application of the CA3120E.*

operates at maximum gain for best signal-to-noise ratio as the i f stage gain is reduced by forward bias. Point C in Fig. 6 is the agc-delay turnover point determined by the open-circuit potential of the voltage divider connected to terminal 13. At this potential, further reduction in the i f -agc gain is inhibited (for good dynamic range) and the tuner agc is activated (represented by line segment CD in Fig. 6).

The agc output at terminal 14 is used for tuners employing reverse agc, such as those incorporating MOS FET's, as shown in simplified form in Fig. 10. The agc at terminal 15 is used for tuners employing n-p-n bipolar transistors requiring forward bias for the agc gain reduction, also as depicted in Fig. 10. The value of the agc filter capacitor is determined by the maximum rate of gain change desired; a typical value is 0.47 microfarad. The detector must be pre-biased, as shown in Fig. 10. With no signal (no carrier) the bias potential should be approximately 8 volts.

The available ratio of charge current to discharge current for the agc filter capacitor during the keying interval is approximately 12 to 1. The nominal peak charging current available is 20 milliamperes. The voltage applied to terminal 12 should not exceed 5.2 volts; the maximum open-circuit delay-bias voltage applied to terminal 13 should not exceed 10 volts. In typical designs, V12 is operated at approximately 2 to 5 volts, and the open-circuit bias voltage at terminal 13 is set to approximately 6 volts.

Transistor Q38, (Fig. 5), connected to terminal 14 (reverse agc output for tuners), can typically sink 3.5 milliamperes. The typical forward agc current available at terminal 15 (supplied by Q40) is 10 milliamperes.

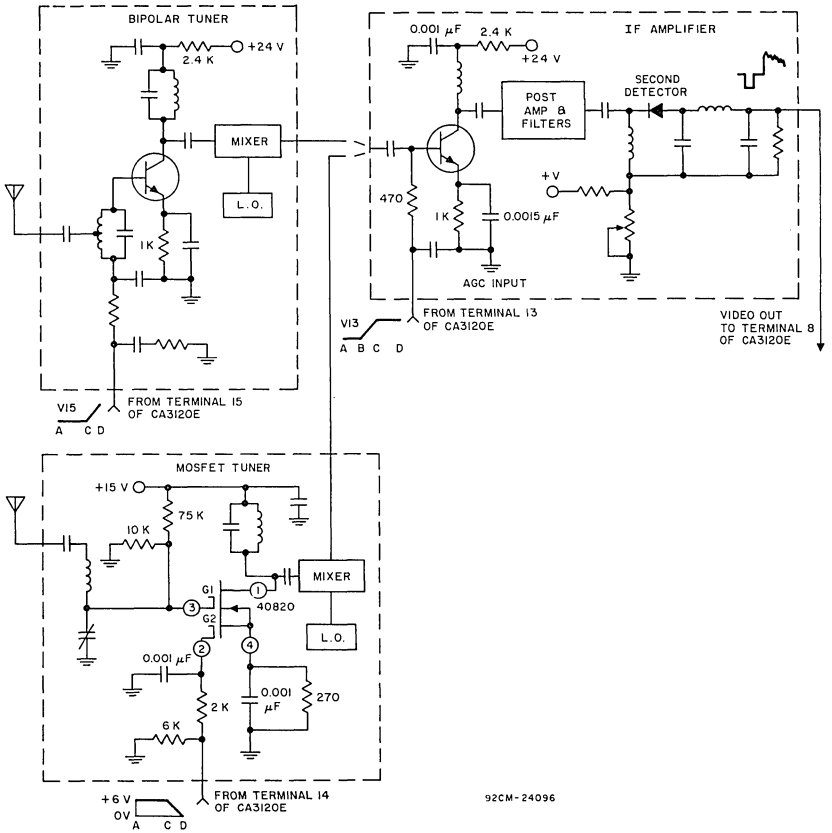



*Fig. 10. Interface of i f amplifier with bipolar and MOS FET tuners.*

**Sync Separator**

Fig. 11 shows a simplified schematic diagram of the sync separator and its equivalent circuits. The choice of the coupling network from the noise-cancelled video output at terminal 5 to the sync-separator input at terminal 4 is a user option. Fig. 12 shows three typical coupling networks. The choice of the network depends on the anticipated input signals. In an NTSC TV signal (see Fig. 13) the sync tips are at peak voltage (and power). Blanking level is at 75 percent, black level is approximately 70.3 percent, and white level is 12.5 percent. The gray level varies between black and white levels.

The function of the sync separator is to take a portion of the sync signal at a level between the sync tips and the blanking level and generate a local sync signal for the deflection circuits of the TV receiver. By choosing the proper portion of the sync signal, the effect of thermal noise or distortion on the sync tips is minimized, and the sync signal is freed of contamination by the video signal.

As shown in Figs. 7 and 11, the sync separator is the base-to-emitter junction of transistor Q56. Base current flows when the application of a positive sync signal from terminal 5 produces a charge on the external coupling capacitor. During the remaining period of time, the base current ceases and the capacitor discharges through the bias and source resistors. The ratio of the charge current to the discharge current sets the bias potential (i.e., sync clamp level).

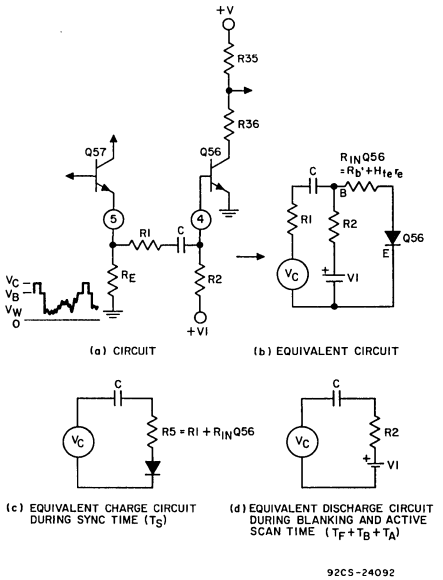



*Fig. 11. Simplified schematic diagram of the sync separator and its equivalent circuits.*

During the sync period, the transistor should be saturated (i.e., removing noise existing at sync tips); during the remaining blanking and active scan period, the transistor should be cut off, thus removing video contamination from the amplified sync pulse. To prevent a large shift in the bias level during the vertical sync interval, the time constants must be large.

Other factors affecting the design of the sync separator are the effects of doppler flutter of the input signal caused by aircraft. If the time constant is excessive, some of the sync pulses may be clipped off; if the time constant is too short, the vertical sync can cause trouble. This problem may be solved by connecting a multiple-time-constant network between terminals 4 and 5 of the CA3120E as shown in Fig. 12. These networks also reduce the effect of impulse noise from hand drills, etc. The short time-constant section of the network allows rapid recovery after a noise burst of long duration, while the long time-constant prevents degradation resulting from short, individual noise pulses. As shown in Fig. 12(a) diodes may also be used to improve the performance of the separator: the diode is used to isolate the coupling capacitors and enhance the operation of the double-time-constant coupling network. In closed-circuit TV systems in which impulse noise or aircraft doppler flutter is not a problem, the simple network described above and shown in Fig. 12(b) may be used.

The optimum clamp level is usually chosen as 30 to 60 percent of the actual sync amplitude (C-B in Fig. 13) to prevent thermal noise on the sync tip from degrading the derived sync signal. The amplitude of the sync signal at terminal 5 is approximately 1.5 volts for a 2- to 3-volt peak-to-peak video signal at terminal 8. This choice also prevents overshoots on blanking from generating spurious sync pulses. Since, in most cases, thermal noise is more tolerable than video contamination, it may be preferable to place the

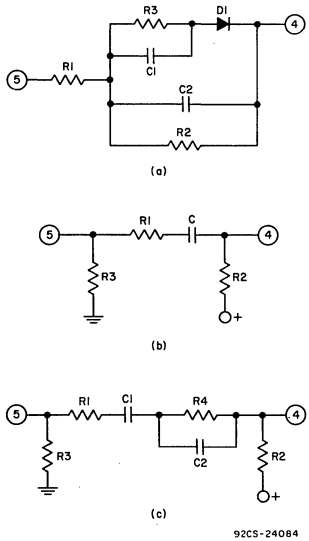



*Fig. 12. Typical coupling networks.*

clamp level nearer to the sync tip. This arrangement reduces the susceptibility of the system to any residual color-burst signals, and is more suitable for use with some industrial TV-camera systems which may not include any set up (blanking level to black level) in the video. The clamp level will shift somewhat as a result of scene changes; but the shift can be

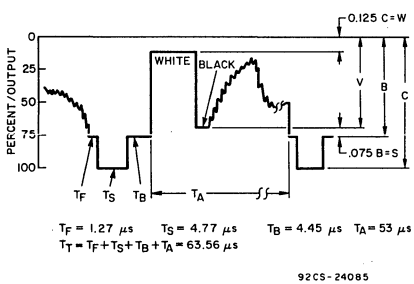



*Fig. 13. Video waveforms.*

minimized by returning the external bias resistor R2 to $V_{CC}$ (Fig. 11), since this results in a much higher ratio of discharge to charge resistance. For example, if V1=0, the resistance ratio is only 120; if the bias resistor is returned to V1= +24 volts, the ratio is greater than 1100. As can be deduced from the above, the change in clamp level for white to black scenes is greatly reduced by returning R2 (Fig. 11) to the 24-volt supply, provided the supply is relatively stable.

If the clamp level is to be set for an all-white signal at 50 percent (CL = 0.5) down from the sync tip, then, in Fig. 11, $R5 = [\,0.5\,(V_C\text{-}V_B)\text{-}V_{4on}]/I_4$. Since $I_4$ is typically 70 microamperes, $V_{4on}$ is approximately 0.7 volt, and $V_C\text{-}V_B$ at terminal 5 is approximately 1.5 volts; therefore:

$$R5 = [0.5(1.5) - 0.7\,]/70(10^{-6}) = 714 \text{ ohms}$$

This value of resistance includes the output resistance of emitter-follower Q57 and the input resistance of Q56. The output resistance of Q57 is low, approximately 5 ohms. The input resistance of Q56 at the threshold of saturation is approximately 500 ohms. An additional series resistance of 100 to 200 ohms may be used. Using the value of R5 calculated above, the value of R2 returned to +24 volts may be calculated (Figs. 11, 13):

$$\frac{R2 + R5}{R5} \cong \frac{T_T}{T_S} \times \frac{V_1}{CL(V_C\text{-}V_B)} \cong 13.3 \times \frac{24}{0.5\,(1.5)}$$

$$R2 \cong 750 \text{ kilohms.}$$

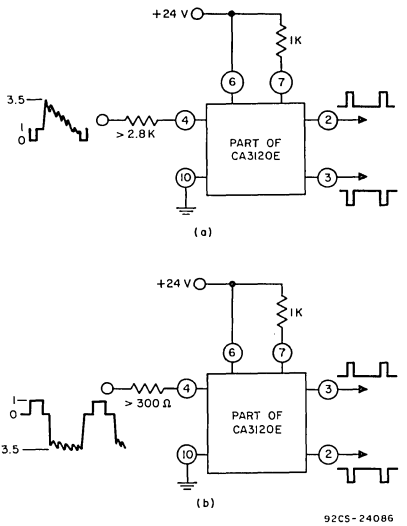



*Fig. 14. Methods of direct coupling sync input terminal to video signal: (a) white, positive; (b) white, negative.*

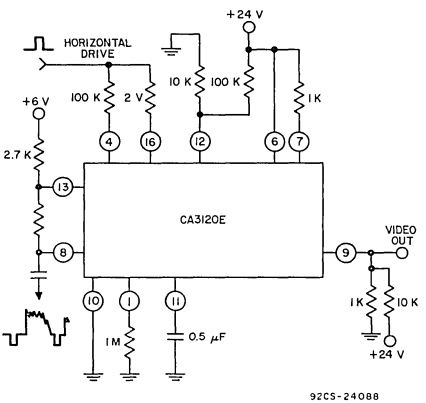



*Fig. 15. Video dc reinsertion amplifier.*

### Video Application of the CA3120E

A sync stripper is often required when the CA3120E is used in industrial-TV (ITV) applications. Fig. 14(a) indicates a method of direct coupling the sync input terminal to the video signal. Note that in this arrangement the sync output polarities are opposite to those used in normal operation. Fig. 14(b) indicates the opposite phase video signal applied to terminal 5. The maximum negative potential applied to terminal 4 should not exceed 5 volts. AC coupling may be used, of course; the design of the ac coupling is the same as previously discussed.

Other video applications for the CA3120E include a method of reinserting the dc component of the video signal (this method is often used in "Stab-Amps"). Fig. 15 shows a possible method of using the CA3120E for this purpose. In the circuit, the clamp voltage is derived by the internal comparator, Q19, Q20 in Fig. 4.

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Wendt, K.R., "TV DC Component," RCA Review, Vol. IX, No. 1, March, 1948.

# A Single IC for the Complete PIX-IF-System in TV Receivers

by M. Caputo

The RCA-CA3068 linear integrated circuit is a PIX-IF-subsystem in a shielded, quad-formed, dual-in-line, 20-lead, plastic package. This package contains all the active devices and most of the passive elements necessary for a high performance, PIX-if-system for a TV receiver. This Note describes the receiver functions performed by the CA3068, and its application to color and monochrome TV receivers.

Specifically, the receiver functions performed by the CA3068 are:

- Video if amplification
- Linear video detection
- Noise-limited amplification of detected video
- Keyed agc, with noise-immunity circuits
- AGC delay for tuner rf stage
- Buffered output signal to drive Automatic-Fine-Tuning (AFT) circuits
- Amplification of intercarrier frequencies
- Sound-carrier detection
- Sound-carrier amplification
- Zener reference diode for voltage regulation.

The only external components required for the operation of this if subsystem are bandwidth shaping networks, biasing networks, and a power supply. A complete functional block diagram of a typical color-TV receiver is shown in Fig. 1. A detailed block diagram of the CA3068, together with its peripheral tuned-circuits, is provided in Fig. 2.

This Note contains a detailed description of circuit functions within the integrated circuit, together with examples of the use of the CA3068 in PIX-IF amplifier PC-boards for color and monochrome TV.

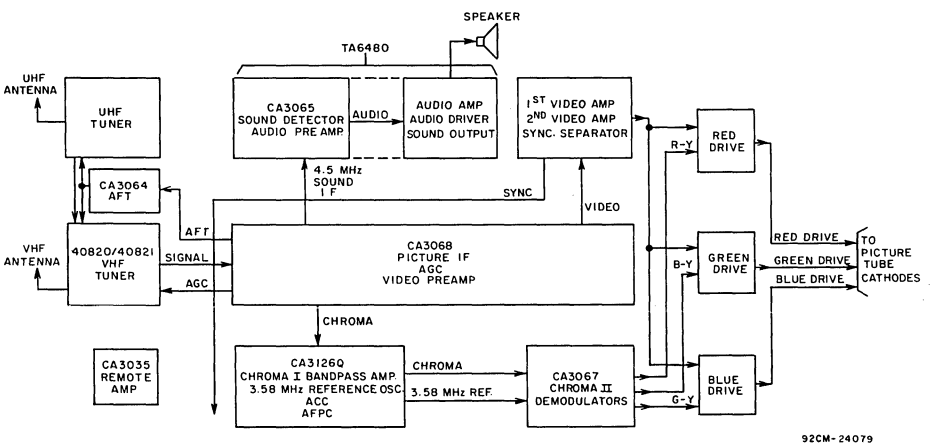



*Fig. 1. Block diagram of typical color-TV signal circuits using the CA3068.*

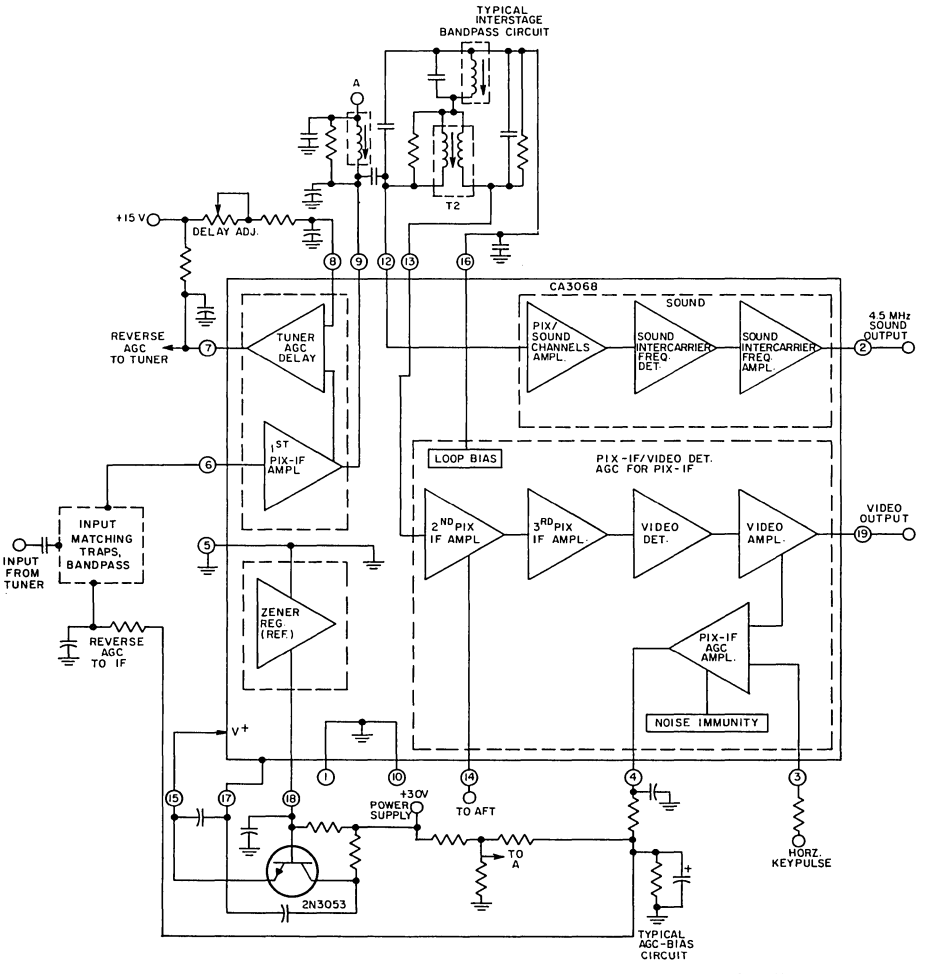



*Fig. 2. Detailed block diagram of the CA3068 together with its peripheral tuned circuits.*

## GENERAL DESCRIPTION OF CIRCUIT FUNCTIONS IN THE CA3068

As shown in the block diagram of Fig. 2, the if signal from the tuner is applied to the input (terminal 6) of the cascode if amplifier. Output from the cascode amplifier is then coupled to a wideband amplifier at terminal 13 through the interstage transformer (T2). Under maximum-gain conditions, the over-all gain of the CA3068 is typically 75 dB at PIX-IF frequencies. This signal is then applied to a linear video detector whose output signal is fed to a video amplifier having a gain of 12 dB.

Bandpass shaping is accomplished by means of tuned-circuits preceding the input stage (terminal 6) and at the interstage circuit comprising input and output terminations via terminals 9, 12 and 13, as shown in Fig. 2. Terminal 16 is tied in at this point to provide loop bias for the input stages of the amplifiers connected to terminals 12 and 13. The agc voltage developed within the CA3068 is applied to its input stage by an external path from terminal 4 to terminal 6 through the input circuitry, as shown in Fig. 2. The developed agc is gated by a keying pulse applied to terminal 3 from the horizontal sweep circuit of the TV

receiver. Delayed agc for the rf amplifier in the tuner is obtained from terminal 7; the delay is variable by adjustment of a resistance (25 kilohms) in series with the supply to terminal 8.

The zener reference voltage for the power-supply regulating pass-transistor is developed at terminal 18 when this terminal is connected to a voltage supply through a current-limiting resistor. This resistor value should be selected to provide a quiescent current into the zener of 0.5 to 1.5 milliamperes (excluding the base current for the pass transistor).

Terminal 15 is the dc input terminal that provides power for most of the CA3068 and should be connected to the 11.2-volt regulated supply as shown in Fig. 2. The CA3068 package has a 20-lead configuration with 18 active terminals. Terminals 11 and 20 have been omitted from the package; their corresponding leads are internally connected to the shield. Terminals 1, 5, and 10 are grounding terminals. In addition, terminal 17 is at ground potential. Additional information relative to dc grounding is given in the section concerning if design.

## DETAILED CIRCUIT FUNCTIONS

Fig. 3 is a schematic diagram of the CA3068. The diagram is partitioned to facilitate the explanation of the circuit configuration and its functions.

The cascode input amplifier (first if) is a unique circuit designed for dual-mode operation. At low-level input signals, the buffer stages formed by Q3 and Q4 drive the base of the cascode-if amplifier composed of Q7 and Q6. Negative-going agc applied to Q3 (through an external connection to terminal 6) increases in proportion to the increase of the input signal level. After approximately 40 dB of gain reduction is reached in this operational mode, Q7 is cut off, and its function is assumed by Q5. Emitter degeneration in Q5 increases the dynamic input range of the cascode amplifier sufficiently to cope with the higher range of input signal level. The point at which Q5 assumes the input amplifier function is sensed by Q11. It should be understood that transistors Q11, Q4, and Q7 approach cut-off at essentially the same signal level. As Q11 approaches cut-off, it

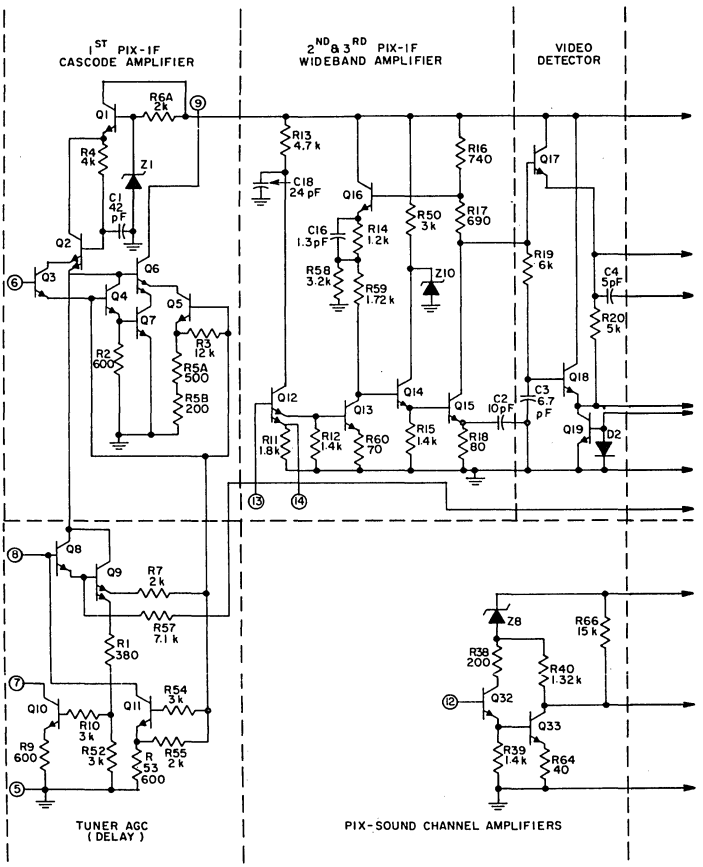
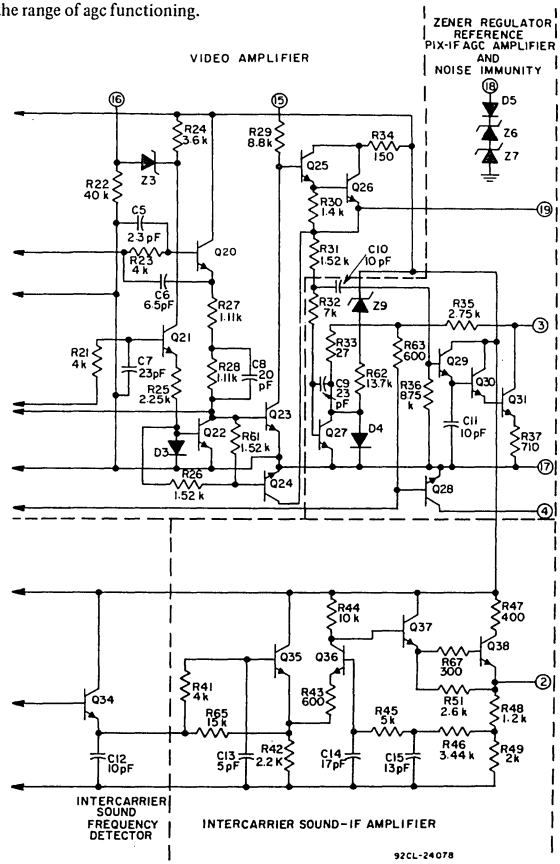



*Fig. 3. Schematic diagram of the CA3068.*

draws less shunting current from terminal 8, and base current drive to Q8 is increased. The point at which sufficient base current is available to drive Q8 into conduction is determined by an external-delay agc potentiometer connected in series with the V+ supply-lead and terminal 8. As Q11 cuts-off, the voltage increases at terminal 8, and current flowing into terminal 8 is diverted to the base of Q8. When Q8 starts to conduct, it turns on Q9 and Q10, thereby causing the open-circuit voltage at terminal 7 to drop and produce a negative-going agc voltage for the rf stage of the tuner. Q8 is also part of the if-agc feedback loop, and provides an increase in agc loop-gain. This increase compensates for the decrease in agc loop-gain that occurs when the cascode if amplifier is transitioned to its modified cut-off characteristic. After tuner gain reduction has reached its maximum, an additional 10 dB of gain reduction can be obtained in the cascode-amplifier under this modified cut-off condition.

This reverse-agc system is used for the cascode input stages because the stability achieved under maximum-gain conditions is maintained throughout the range of agc functioning.

The wideband if amplifier consists of transistors Q12, Q13, Q14 and Q15. Q12 serves as a buffer stage between the interstage tuned-circuits and the automatic-fine-tuning (AFT) output-signal terminal. The actual if signal amplification takes place in Q13, Q14 and Q15, which effectively serve the function of second and third PIX-IF stages. Transistor Q15 is the driving source to Q17, the video detector. This driving source impedance is approximately 500 ohms as a result of the degenerative feedback loop through Q16. The feedback network also extends the 3-dB-down frequency response to beyond 70 MHz. It is this low detector-driving-point impedance and the absence of a tuned-circuit at this interstage point that contribute to the superior performance of the detector system. In most conventional detection systems, the detector is driven from a high-impedance source involving a double-tuned interstage transformer with unequal primary and secondary Q's. In such a system, variations in detector impedance (caused by normal video excursions) can produce significant phase shifts



that adversely affect color fidelity. In the CA3068, the untuned, low-impedance detector drive circuit produces a nearly optimum condition for the detector circuit.

The detector circuit consists of transistor Q17 and its biasing network Q18, Q19 and R20. Q18 is biased to the same potentials as Q17 because the bases are tied together through the resistance element of the low-pass filter that consists of R19 and C3. R20 and C4 form a conventional peak detector in which the time constants are selected for optimum detector efficiency and desired video bandwidth. This system detects chroma subcarrier without introducing differential phase errors as a function of the video signal, and detects the video signals with a minimum of amplitude distortion. The low signal-level requirements for the detector, the absence of tuned-circuits in the detector drive circuit, and the low source impedance for the detector, all contribute to the superior detector performance.

The video detector is direct-coupled to the video amplifier. Consequently, a dc input voltage above the level of one $V_{be}$ (0.7 volt) drop at the input to Q23 determines the condition for white level (dc) at the output (terminal 19). It is necessary, therefore, to bias Q23 to the threshold of conduction in the absence of detected video. This function is accomplished by the differential-amplifier circuit arrangement consisting of transistors Q20 and Q21. In the absence of signal, the dc potentials at the emitters of Q20 and Q21 are identical. The current through Q20 must equal the current through Q21 because R25 is similar in value to (R27 + R28). This current also flows through D3 (which has the same geometry as Q22). Consequently, Q22 carries all the current supplied by Q20, and no current is available for the base of Q23, so that Q23 is held on the edge of conduction. When an rf carrier is present, the current in Q20 increases in direct proportion to the carrier level; however, the current in Q21 remains fixed. When the current increases in Q20, this increase can only flow to the base of Q23. Since the current in Q23 is directly proportional to its base current flow, a corresponding increase in current through Q20 as a result of rf carrier detection produces a video output at terminal 19.

As the video carrier signal increases, the dc level at the base of Q23 increases, and there is an accompanying decrease in the dc level at the base of Q25 and, consequently, at terminal 19. With a sufficiently strong rf signal, the current through Q23 and R29 increases such that the base voltage of Q25 is driven toward dc ground. The "bottoming" level at terminal 19 under nominal signal conditions is locked to about 0.8-volt as a result of the high loop gain of the agc system. Any further increase in the signal, after "bottoming" is reached, will be clipped. This operational feature serves as a highly effective mechanism to limit impulse noise.

When a signal is present at the input, the composite video signal at the base of Q25 appears at terminal 19 through the Darlington connection to the emitter of Q26. The sync tips in this composite waveform drive the keyed agc amplifier Q27, which in turn drives Q28. Without a video rf signal there is no video signal output, and Q27 conducts during the keying intervals (the horizontal pulse is connected to terminal 3). As the detected signal level increases in amplitude and the output voltage at terminal 19 approaches its typical operational level of 7 volts peak-to-peak, the peak potential at the base of Q27 begins to fall below 0.8 volt. Under these conditions, the keying current formerly channeled through Q27 is diverted through diode D4. As the signal level rises even higher, a greater portion of the Q27 collector current is diverted through D4, and the base current to Q28 is proportionately increased. A 10-microfarad capacitor is normally connected between terminal and ground and is, by this connection, put in shunt with Q28. The charge on this external capacitor is maintained through a bleeder resistor to V+. As the base current to Q28 increases, Q28 discharges the capacitor at a rate that is proportional to the base current of Q28. Integration of the total charge on the capacitor over the keying interval yields a dc level (agc voltage) that is inversely proportional to the incoming signal level; i.e., agc voltage approaches zero as the signal increases.

Any high-performance agc system must have noise-immunity characteristics in order to avoid the establishment of false agc levels. AGC voltage developed from random noise can produce "wash-out", "blank raster" and/or a momentary "loss of sync". The CA3068 is designed with an improved noise-immunity circuit that essentially removes the keying current during periods of high noise input. The active devices responsible for providing protection against this deleterious effect of the impulse noise are the "noise detector", Q29, and the "noise clamp" Q31, which is driven by Q30. Impulse noise is channeled through the high-pass filter network consisting of C10 and R36 to the detector input Q29. Q29 and C11 comprise a conventional peak detector. The dc level across C11, which is proportional to the level of impulse noise, turn on Q30 and Q31, thereby clamping the keying supply voltage (terminal 3) to ground. In actual operation, the terminal-3 supply has a series resistance that is large enough to limit the peak current into the zener diode (Z5) to approximately 0.8 milliampere. When Q31 conducts, it shunts this current to ground.

The sound-if-channel and PIX-IF-channel signals whose "carrier" frequencies are 41.25 MHz and 45.75 MHz, respectively, are applied to terminal 12. Q32 functions as a buffer between the interstage-tuned-circuits associated with terminal 12 and the PIX/sound-channels amplifier, Q33. The intercarrier frequency (the difference frequency between the PIX and sound "carrier" frequencies) is detected by the peak detector Q34 and C12. The resultant 4.5 MHz FM sound-intercarrier signal is fed to transistor Q35. This transistor and Q36 form a differential pair that provides an amplified intercarrier sound-if signal to the base of Q37. A feedback system through the RC networks in the Darlington emitter-follower output of Q37 provides bandpass shaping in the region of 4.5 MHz while maintaining a low dc gain. The low level of dc gain is desirable because the circuit receives its bias in an open-loop manner from terminal 16. The bandpass of this amplifier system is fairly broad, and even though it is optimized for 4.5 MHz operation, there is relatively high output at other intercarrier frequencies, as shown in the curve in Fig. 4.

The internal zener reference-diode consists of the series diode arrangement shown connected between terminal 18 and the substrate in Fig. 3. A regulator-circuit configuration showing the pass transistor interconnected with the reference diode is given as part of the color and monochrome if amplifier circuits that are discussed in the following paragraphs. Similarly, the regula-

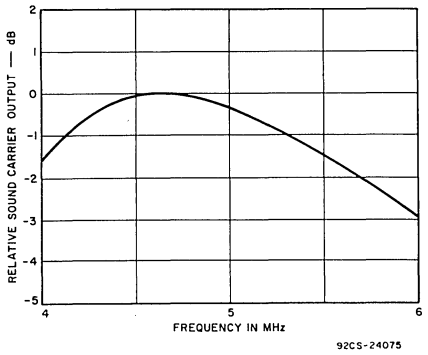



*Fig. 4. Relative sound-carrier output as a function of frequency.*

tion curves shown in Figs. 5 (a) and 5 (b) are discussed below in more detail. It should be noted that (with a heat sink for the 2N3053 and a lower value for the resistor in series with the collector) the regulated voltage from this supply may be used to provide power to other circuits in addition to the CA3068.

The distribution of tuned circuits around the CA3068 amplifier circuit is a matter of preference of the circuit designer. In general, a total of five tuned circuits will be required subsequent to the mixer for proper selectivity and bandpass shaping. In addition, at least one 47.25 MHz adjacent sound-channel and one 41.25 MHz sound-channel trap will be required. The systems to be discussed in this Note are designed to be driven from a single tuned circuit connected to the mixer output. In addition, both the color and monochrome if systems described subsequently utilize tuned circuits at the input and output to the cascode amplifier. The second transformer is used to couple output from the cascode if amplifier to the wideband if amplifier (i.e., the output from terminal 9 to input terminal 13 for the PIX-channel and input terminal 12 for the sound-channel). All of the if transformers are synchronously tuned.

## PIX–IF SYSTEM DESIGNS

The use of the CA3068 in the two major categories of PIX-IF application, PIX-IF for color-TV receivers and PIX-IF for monochrome receivers, is described below. To illustrate the use of the CA3068 in a tuner requiring "reverse" agc action, the rf-stage of the tuner employed in the PIX-IF for color-TV receiver contains a MOSFET. In contrast, the rf-stage of the tuner employed in the PIX-IF for the monochrome receiver makes use of a bipolar transistor in a "forward" agc arrangement.

## COLOR TV

A block diagram of a color-TV receiver is shown in Fig. 1. In the design to be described, the input to the if system is intended to be coupled through a 50-ohm cable from the TV mixer; the mixer employs a single tuned-output coil having an impedance transformed down to 50 ohms. The if input circuit drives a cascode if amplifier with a gain capability of 35 dB. The input impedance to the cascode if amplifier is greater than 4000-ohms at minimum signal levels and increases with agc action. The source impedance as seen by the CA3068 should be approximately 500 ohms to dominate the input-circuit conductance node. Similarly, the output impedance of the cascode amplifier should be loaded by a tuned circuit with an impedance of approximately 3000 ohms to dominate the output node. The if amplifier stability is then unaffected by the IC impedance variations, but is a function of the feedback component. This feedback component consists of coupling within the IC packaging, PC-board stray capacitances, and PC-board common impedances. It can be shown that with the maximum device

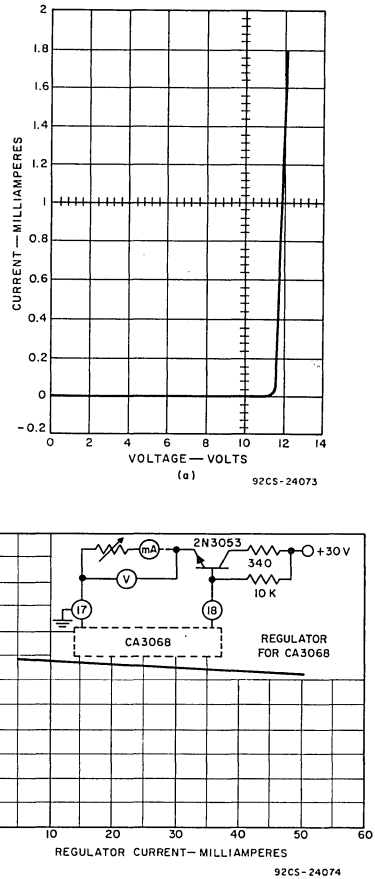



*Fig. 5. Regulated supply of the CA3068: (a) voltage-versus-current for zener reference diode of CA3068; (b) voltage-versus-current for regulated supply of CA3068.*

feedback capacitance the amplifier is stable. For example, with circuit bias conditions of I9 = 2 mA, Y21 = 50 mmhos, and $C_{fb}$ (max) = 0.005pF, the maximum usable gain (MUG) is 42 dB (which allows for a 20 percent skew factor). The fact that this value of MUG is greater than the actual circuit gain (35 dB) substantiates the stability.

Although these calculations show the device to be theoretically stable, it must be realized that it is possible for external feedback mechanisms, in effect, to raise the level of feedback in any high-gain, physically small rf amplifier and produce instabilities. For this reason, the PC-board layout is extremely important, and any high-gain if amplifier design should include a board layout.

As mentioned previously, the interstage transformer should load the cascode amplifier with approximately 3000 ohms, and should provide a 500-ohm source impedance to input terminal 13 (the wideband if amplifier section). The impedance at terminal 13 is approximately 5000 ohms. The driving-point impedance to sound-if terminal 12 should be about 1000 ohms, this terminal looks into a 5000-ohm input circuit. The 41.25 MHz trap is a rejection filter for the video amplifier and allows the carrier to pass into the sound system.

The circuit design in Fig. 6 shows a typical cable-link circuit which includes a 47.25 MHz bridged "T" adjacent-sound-channel trap at the input circuit. It also includes a 39.75-MHz trap for an adjacent video carrier for operation in CATV systems or in areas where adjacent channels are available. This trap may consist of a 39.75-MHz bridge "T" connected in parallel directly across the 47.25-MHz trap. Both traps provide the additional selectivity necessary for attenuation of the undesired frequencies by more that 40 dB.

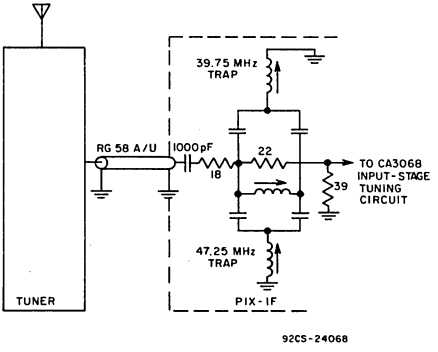



*Fig. 6. Schematic diagram of a typical tuner-to-PIX-IF link circuit.*

The second and third PIX-IF amplifier stages provide two extra stages of gain (approximately 40 dB). The stages present a very low driving-point impedance to the linear detector, as described earlier. The detected signal then undergoes an additional 12 dB of video amplification. The video output at terminal 19 is nominally 7 volts (peak-to-peak). AGC is developed when the input signal reaches and exceeds the magnitude necessary to produce this video output level. Fig. 7 (a) shows the developed agc bias (terminal-4 voltage) as a function of signal level at terminal 6. Fig. 7 (b) shows the delayed agc voltage at terminal 7 (for application to the tuner) with R1 adjusted so that this delay-bias is generated whenever the input signal at terminal 6 exceeds 8 millivolts.

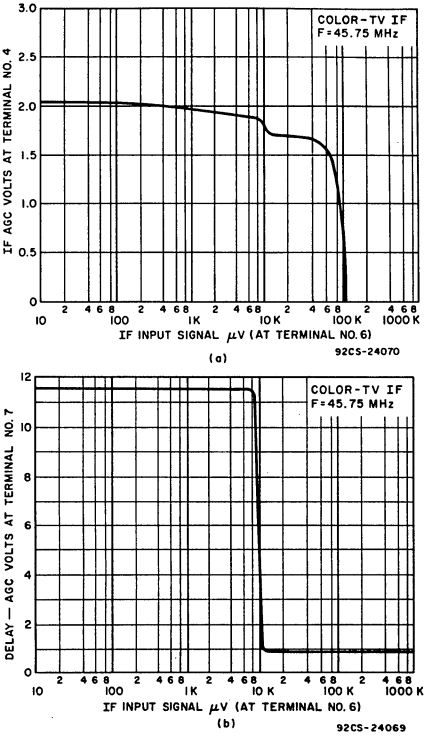



*Fig. 7. (a) Developed agc bias as a function of signal level at terminal 7; (b) delayed agc voltage at terminal 7.*

Fig. 8 shows the CA3068 coupled to a tuner that uses an RCA type 40820 MOSFET in the rf-amplifier stage. AGC voltages are applied (shown in Fig.8) to optimize over-all TV-receiver performance, so that, when maximum receiver sensitivity is required (such as during the reception of weak signals from the antenna) the tuner will operate at optimum noise factor and maximum gain. As the input signal level increases, it is still desirable to operate the rf stage at optimum signal-to-noise ratio until the signal level is of sufficient magnitude to override any tuner noise degradation brought about by the application of agc. Therefore, the gain-reduction voltage to the tuner should be delayed until the signal level builds up. Fig. 7 (b) shows that this agc is delayed until the if signal level reaches an 8-millivolt level. Then the tuner gain-reduction mode is initiated. After the tuner gain re-

duction is expended, at least another 10-dB gain reduction is still available in the cascode portion of the if amplifier.

An output signal is available at terminal 14 to drive an automatic-fine-tuning (AFT) subsystem-IC, such as the RCA CA3064. This connection is a buffered output from an emitter follower as described earlier. The level of signal at 45.75 MHz to drive the AFT circuit is nominally 15 millivolts.

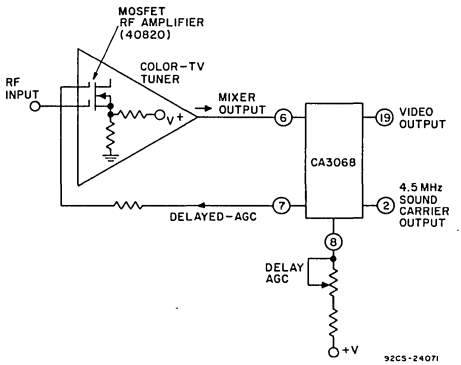



*Fig. 8. Block diagram of a color if system.*

As shown in Fig. 2, the agc system is, for the most part, self-contained. An optimized agc response characteristic can be achieved by use of a high-quality tantalum 10-microfarad capacitor connected between terminal 4 and ground. An RC decoupling network smooths the agc ripple associated with the charge and discharge of the 10-microfarad capacitor at the horizontal-oscillator frequency rate. The agc system is normally keyed from the horizontal-output circuit in the TV system. This keying pulse should be applied to terminal 3. The magnitude of the pulse should be sufficient to supply a nominal peak current value of 0.8 milliampere into terminal 3. The value of the series resistor $R_S$ associated with terminal 3 may be computed as follows: During the conduction period (with keying applied), the constant-voltage components within the integrated circuit account for:

$V_k = 8.2$ V

(It is assumed that I3 = 0.8 mA)

If the keying-pulse magnitude, $V_p$, is 15 V, then:

$$I3 = 0.8 \text{ mA} = \frac{15 - V_k}{R_S} = \frac{(15 - 8.2) \text{ V}}{R_S}$$

$R_S = 8.5$ kilohms

The sound output is derived from terminal 2 at a level compatible with the input requirements of a TV-sound-if-subsystem IC, such as the RCA CA3065. There is also a dc component of approximately 6.7 volts present at terminal 2. Coupling networks to subsequent circuits must contain a suitable dc-blocking capacitor.

Small chokes located in the sound and video outputs (terminals 2 and 19) should be self-resonating at the intermediate frequencies to prevent if leakage into subsequent stages.

The CA3068 if subsystem has an internal zener reference-diode that permits operation of the subsystem with an external voltage-regulator pass transistor. A suggested circuit arrangement is shown as part of the over-all if schematic diagram in Fig. 5 (b). The voltage-regulator pass-transistor has a nominal output voltage of 11.2 volts. Bypassing of the V+ supply with reference to the if subsystem is important, and the suggested arrangement shown in the application circuit (Fig. 10) should be used. Specifically, terminal 15 should be bypassed to terminal 17 on the CA3068. Even though terminal 17 is at dc ground potential, it should not be tied to ground but rather should be bypassed in the manner shown to avoid mutual impedance coupling within the CA3068.

## MONOCHROME TV

The delayed-agc circuits used in the CA3068 were originally intended to control a MOSFET in the rf-stage of the TV tuner. This arrangement permits direct application of the delayed-agc voltage from the CA3068 to the tuner. In monochrome receivers, however, it is common practice to employ a bipolar transistor in the rf-stage of the tuner, and a circuit with a "forward"-agc characteristic is required to control the rf-stage. This characteristic is easily established by means of an inverter network utilizing a p-n-p transistor, as shown in the circuit of Fig. 9.

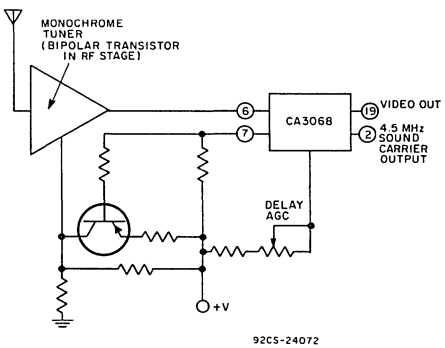



*Fig. 9. Block diagram of an if system for a monochrome receiver showing peripheral agc circuit.*

As the input signal level increases, the forward-agc delay voltage is developed at the tuner when the voltage at terminal 7 of the CA3068 decreases. The agc voltage applied to the rf-stage of the tuner (Fig. 9) is derived from the collector of the p-n-p transistor. As the delay-agc voltage is generated at terminal 7 of the CA3068, the base of the p-n-p inverter is driven into conduction, which causes more current to flow through the collector circuit, so that a positive (or forward) agc potential is generated for the bipolar transistor in the tuner.

## TV RECEIVER PIX–IF CIRCUIT APPLICATIONS

In this section, the application of the CA3068 integrated circuit in a color and a monochrome TV receiver is described. The circuits shown were constructed on single-sided copper PC boards.

As previously noted, because of the high gain encountered in PIX-IF design, positive feedback must be avoided if the amplifier is to remain free of spurious oscillation. To this end, the optimization of printed board layout and component placement is essential. The proper choice of bypassing components and signal-path layout is necessary to avoid feedback through ground loops.

### IF CIRCUIT FOR COLOR TV RECEIVER

The schematic diagram of an if system for a color-TV receiver is shown in Fig. 10. A parts list and illustrations showing the PC-board component layout (top view) and the actual printed circuit (bottom view of board) are shown in Appendix A. Since most current color-TV receivers employ automatic-fine-tuning (AFT) systems, an AFT system using the CA3064 has also been included on the same board; Fig. 10 includes the AFT circuit.

The if-response is determined by the triple-tuned circuit, which consists of three traps: two preceding the IC and an interstage double-tuner circuit with one trap. In the tripled-tuned circuit, the two bridge-T traps are used to provide attenuation of the adjacent-channel picture carrier (frequency 39.75 MHz) and adjacent-channel sound carrier frequency (49.25MHz). A common bridge impedance consisting of parallel-connected L1 and R2 is used. Adjustment of L1 for best null of the 47.25 MHz trap assures the desired 60-dB minimum attenuation.

The triple-tuned circuit provides, at center frequency, a source resistance to the IC of 800 ohms and a voltage gain of three from the input to pin 6 of the IC. The first section of the triple-tuned circuit consists of L2 and C6. Capacitor C6 is in parallel resonance with coil L2 at 44 MHz. The third section of the triple-tuned circuit consists of coil L4 and capacitor C14. Coupling and voltage-gain from L2 to L4 are provided by the second section, coil L3 and capacitors C10, C11, and C12. The inductive reactance of L3 is made 75 times larger than that of L2 to provide a high degree of tuned-circuit isolation for ease of alignment.

The circuit provides protection against interference resulting from a strong rf signal which might inadvertently be introduced between the tuner and the if stage. Parasitic resonance and

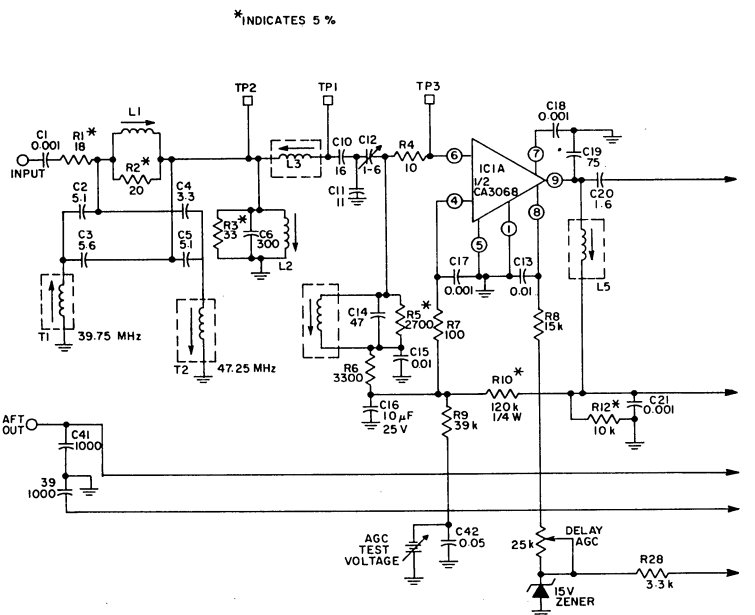



*Fig. 10. Schematic diagram of a typical application of the CA3068 to a PIX-IF circuit for a color-TV system. A template of the printed circuit board used to construct this circuit, a diagram of the position of all components on the board, a block diagram of the location of major components on the board, and a circuit parts list are given in Appendix A.*

couplings have been minimized to maintain a high degree of attenuation at frequencies remote from the if-resonance frequency.

The interstage double-tuned bandpass circuit, with a bifilar T-trap at 41.25 MHz, is similar to that commonly used in the third stage of color-TV receivers. The sound and picture carriers are present at the input (terminal 12) to the 4.5 MHz sound-if detector circuit. Trapping action removes the 41.25 MHz sound carrier at terminal 13 to prevent a difference-frequency beat of 0.92 MHz with the chroma subcarrier at 42.17 MHz. The picture carrier and chroma subcarrier entering terminal 13 are amplified, detected, and additionally amplified as detected video signal. If the sound carrier is not attenuated by the 41.25 MHz trap, the carrier will be detected as a large 4.5 MHz difference-signal in the video output. A 4.5 MHz trap (T5) is included to prevent interference of a residual 4.5 MHz intercarrier signal in the chroma and luminance circuits.

The chroma peaking circuit compensates for the slope of the video response, as shown in Figs. 11 (a), 11 (b) and 11 (c). The actual slope and shape of the video response between 3.08 MHz and 4.08 MHz will vary because of normal component tolerance. The chroma-peaking coil, L7, has two cores, one to adjust inductance to center the response at 3.58 MHz, and the other to adjust chroma output level and bandwidth. The latter core controls circuit Q with little effect on over-all inductance.

Photographs of the detected sweep-response characteristics are shown in Fig. 12. The sweep-response of Fig. 12 (f) shows the interstage alignment from TP3 (of Fig. 10) to terminal 9 of the CA3068. The sweep-response curves in Figs. 12 (a) through 12 (e) show 60 dB of agc range from a level of 100 microvolts (Fig. 12 (e)) to 100 millivolts (Fig. 12 (a)).

The alignment procedure for the color-TV PIX-IF system using the CA3068, Fig. 10, is given in Appendix A.

## IF CIRCUIT FOR MONOCHROME TV RECEIVER

The schematic diagram for a PIX-IF system for a monochrome TV system that employs the CA3068 is shown in Fig. 13. A PC-board component-layout diagram (top view), the actual printed circuit (bottom view of board), and a circuit parts list are shown in Appendix B. A sound-if system using the CA3065 has been included to show the simplicity with which it can be used in conjunction with the CA3068.

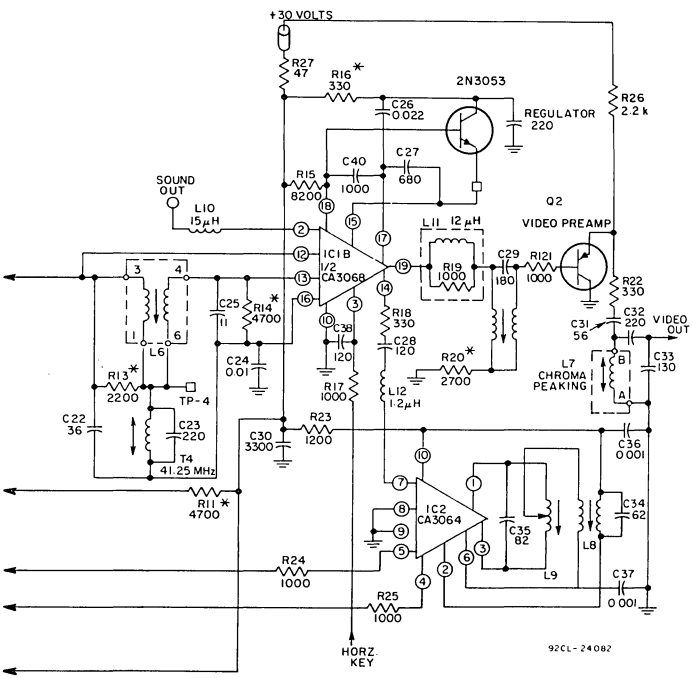



*Fig. 10. Schematic diagram of a typical application of the CA3068 to a PIX-IF circuit for a color-TV system. A template of the printed circuit board used to construct this circuit, a diagram of the position of all components on the board, a block diagram of the location of major components on the board, and a circuit parts list are given in Appendix A.*

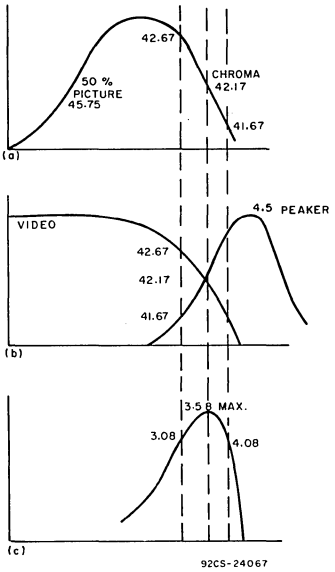



*Fig. 11. (a) Over-all if response, (b) video and peaking circuit response, (c) chroma response for the circuit of Fig. 10 (frequency values in MHz).*

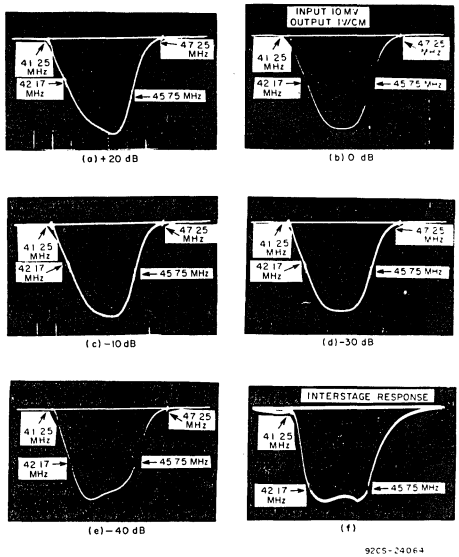



*Fig. 12. Detected sweep-response characteristics for the circuit of Fig. 10.*

The selectivity is provided in two sections, an input single-tuned circuit with trap, and a double-tuned interstage circuit. The resistive pad, R1, R2, and R3 of Fig. 13, is used to terminate the link-cable and isolate cable effects from the high-Q input circuit. The bridge-T trap-circuit is used to give maximum attenuation to the adjacent-channel sound carrier. Precision components (R2, C1, C2) achieve a good null at 47.25 MHz without the need for additional components. The circuit Q is controlled by R11 and the resistive input network to yield a 3-dB bandwidth of 3 MHz centered at 44.5 MHz. The "T"-equivalent circuit is used for interstage coupling to realize a miniature, precision, double-tuned transformer. The mutual coupling element, L5, is an air-core, spring-winding coil which is actually calibrated by physical dimensions. If necessary, this coil may be "knifed" to provide a simple and effective coupling adjustment. The circuit Q's are each set at 21, and are controlled by R17 and R18, which also feed bias for the broadband amplifier and sound channels, respectively. The picture-carrier at 45.75 MHz is set at 50 percent to yield proper reception of the vestigial sideband. The color subcarrier at 42.17 MHz is placed comparatively low on the response curve, since the resulting beat with the 41.25 MHz is placed at greater than 5 percent but less than 10 percent to produce an adequate sound-if intercarrier signal at 4.5 MHz, and yet maintain low intermodulation. Typical over-all sensitivity of the if circuit is approximately 150 microvolts for full video output.

Interference from the 45-MHz high-level signals and harmonics is prevented by care in passing and filtering. A 12-microhenry choke (L4 of Fig. 13), self-resonant at the fourth harmonic, is used in the video output lead; the sound output contains a ferrite bead. The B+ supply must be bypassed to provide a low-impedance source for the video driver stages and to provide high-frequency filtering. The 1-microhenry choke (L3 of Fig. 13) is made very lossy to prevent resonance with C8. The ferrite bead and C9 provide high-frequency filtering for harmonics of the 45-MHz signal.

Typical sweep-response characteristics are shown in Fig. 14. The alignment instructions for the monochrome, PIX-IF circuit are given in Appendix B.

## SUMMARY

A complete if subsystem has been described for use in both color and monochrome TV receivers. The only signal inputs required by the CA3068 are if signals from the tuner and a keying pulse from the horizontal circuitry. The CA3068 provides all outputs needed to drive the video output stage, delay line, sync-separator circuitry, RCA CA3065 sound if subsystem, RCA CA3064 AFT subsystem, and delayed-agc voltage for the rf stage in the tuner. Additionally, circuits for noise immunity and signal overload protection are an integral part of the CA3068 design. These subsystems have typical input

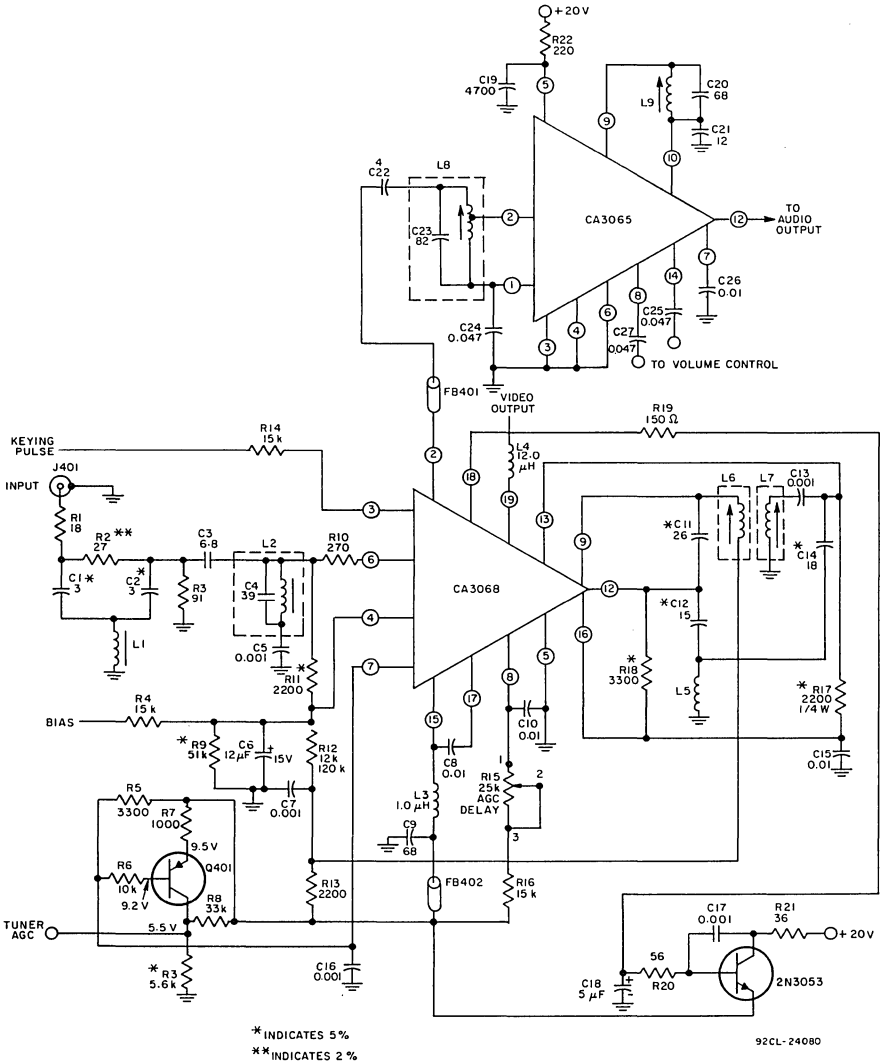



*Fig. 13. Schematic diagram of a typical application of the CA3068 to a PIX-IF circuit for a monochrome-TV system. A template of the printed-circuit board used to construct this circuit, a diagram of the position of all components on the board, and a circuit parts list are given in Appendix B.*

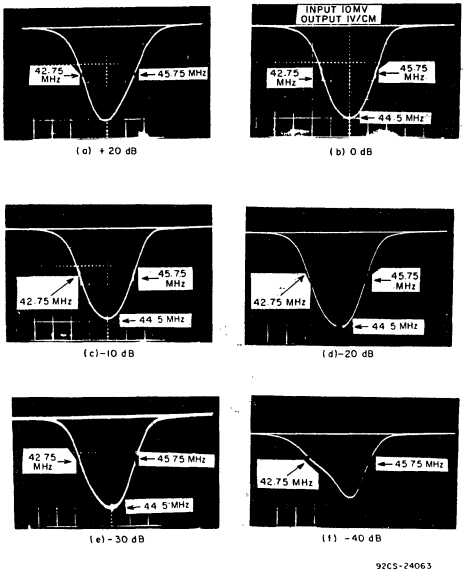



*Fig. 14. Typical sweep-response characteristics for the circuit of Fig. 13.*

sensitivities of 100 microvolts for a 4-volt, peak-to-peak video output. A unique video detector arrangement provides extremely linear output throughout the 7-volt, peak-to-peak, video-output range of the system.

Although this Application Note describes subsystem designs in TV receivers, the CA3068 is also applicable in AM communications systems requiring performance at frequencies within the range of 10 to 70 MHz.

## REFERENCES

1. RCA Data Bulletin File No. 396 concerning the CA3064 and CA3064E, "TV Automatic Fine Tuning Circuit", or the RCA DATABOOK, 1974 Series SSD-201B.
2. RCA Data Bulletin File No. 412 concerning the CA3065, "TV IF Sound System", or the RCA DATABOOK, 1974 Series SSD-201B.

## ACKNOWLEDGMENT

The original general description of circuit functions of the CA3068 were written by S. Reich and R. T. Peterson.

## APPENDIX A – THE COLOR CIRCUIT

## ALIGNMENT PROCEDURE FOR THE COLOR CIRCUIT

### Preliminary Adjustments and Calibration

1. Adjust delay-agc (noise pot) fully cw.
2. Connect supplies as indicated on schematic diagram (Fig. 10), set bias to zero.
3. Set sweep generator to 10 millivolts as indicated on Boonton 91DA meter with 56-ohm termination.

### Step 1 - IF Interstage Alignment

a. Ground TP1 with short clip lead.
b. Connect sweep generator with 56-ohm termination and 1000-picofarad decoupling capacitor to TP3.
c. Connect oscilloscope to video output.
d. Adjust bias for 5-volt peak-to-peak response on oscilloscope.
e. Adjust bottom core of T4 for minimum at 41.25 MHz.
f. Adjust L5 and L6 for symmetrical response with PIX and color markers equal (Fig. 12 (a)): L5 controls markers and L6 controls tilt.
g. Adjust top and bottom cores of T4 simultaneously, top core for maximum rejection of 41.25 MHz and bottom core to maintain minimum 41.25 MHz.

### Step 2 - IF Overall Alignment

a. Leave ground clip lead on TP1.
b. Remove sweep input from TP3.
c. Connect TP2 through a 1000-picofarad capacitor to TP3.
d. Connect sweep generator to input.
e. Readjust variable bias to maintain 5-volts peak-to-peak response on oscilloscope.
f. Adjust T1 for minimum 39.75 MHz.
g. Adjust T2 for minimum 47.25 MHz.
h. Adjust L2 for equal height of PIX and color markers.
i. Remove ground-clip lead from TP1 and 1000-picofarad capacitor from between TP2 and TP3.
j. Maintain 5-volts peak-to-peak response on oscilloscope by re-adjusting bias.
k. Adjust L3 and L4 simultaneously for symmetrical response with PIX and color markers equal: L4 controls markers and L3 controls tilt.
l. Adjust bandpass trimmer, C12, to place PIX and color markers at 40 percent while readjusting L3 and L4 (Fig. 12 (b)).
m. Re-adjust T1 for minimum at 39.75 MHz if necessary.
n. Re-adjust T2 for minimum at 49.25 MHz. Then adjust L2 to maximize the rejection at 47.25 MHz.

### AFT Alignment

a. With oscilloscope on AFT output, adjust bias for 10-volts peak-to-peak response.
b. Adjust L8 for maximum 45.75 MHz.
c. Adjust L9 for crossover at 45.75 MHz.
d. Re-adjust L8 and L9 to obtain symmetry.
e. Adjust L8 to obtain maximum width.

### Color-Circuit Parts List

| Capacitors | | Resistors (All values in ohms) | |
|---|---|---|---|
| C1 | 0.001μF | R1 | 18 |
| C2 | 5.1pF | R2 | 20 |
| C3 | 5.6pF | R3 | 33 |
| C4 | 3.3pF | R4 | 10 |
| C5 | 5.1pF | R5 | 2.7k |
| C6 | 300pF | R6 | 3.3k |
| C10 | 16pF | R7 | 100 |
| C11 | 11pF | R8 | 15k |
| C12 | 1-6pF | R9 | 39k |
| C13 | 0.01μF | R10 | 120k |
| C14 | 47pF | R11 | 4.7k |
| C15 | 0.01μF | R12 | 10k |
| C16 | 10μF | R13 | 2.2k |
| C17 | 0.001μF | R14 | 4.7k |
| C18 | 0.001μF | R15 | 8.2k |
| C19 | 7.5pF | R16 | 330 |
| C20 | 1.6pF | R17 | 1k |
| C21 | 0.001μF | R18 | 330 |
| C22 | 3.6pF | R19 | 1k |
| C23 | 220pF | R20 | 2.7k |
| C24 | 0.01μF | R21 | 1k |
| C25 | 11pF | R22 | 330 |
| C26 | 0.022μF | R23 | 1.2k |
| C27 | 680pF | R24 | 1k |
| C28 | 120pF | R25 | 1k |
| C29 | 180pF | R26 | 2.2k |
| C30 | 0.022μF | R27 | 47 |
| C31 | 56pF | R28 | 3.3k |
| C32 | 220pF | R29 | 25k |
| C33 | 130pF | | |
| C34 | 62pF | | |
| C35 | 82pF | | |
| C36 | 0.001μF | | |
| C40 | 1000pF | | |
| C41 | 1000pF | | |
| C42 | 1000pF | | |

| Inductors | RCA Stock No. |
|---|---|
| L1 | 132159 |
| L2 | 132161 |
| L3 | 132839 |
| L4 | 132658 |
| L5 | 137126 |
| L6 | 132146 |
| T1 | 132839 |
| T2 | 132157 |
| T4 | 132150 |
| T5 | 132135 |

## APPENDIX B – THE MONOCHROME CIRCUIT

### ALIGNMENT PROCEDURE FOR THE MONOCHROME-CIRCUIT

**Step 1 -**

1. Connect +20 volts to appropriate points on board.
2. Connect sweep generator to input
3. Connect dc bias voltage to appropriate point on board.
4. Adjust sweep generator for 10-millivolt input.
5. Adjust bias voltage for 5-volt, peak-to-peak output.

**Step 2 -**

1. Adjust LT for minimum response at 47.25 MHz.
2. Adjust L2 for maximum at 44.5 MHz.
3. Adjust L6, L7 for bandpass shown in Fig. 14 (b). The curve should have 3-MHz bandwidth centered at 44.5 MHz.

**Monochrome-Circuit Parts List**

**Capacitors**

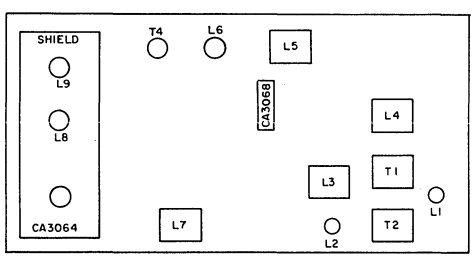
| | |
|---|---|
| C1 | 3.0pF |
| C2 | 3.0pF |
| C3 | 6.8pF |
| C4 | 3.9pF |
| C5 | 0.001μF |
| C6 | 12μF |
| C7 | 0.001μF |
| C8 | 0.001μF |
| C9 | 6.8pF |
| C10 | 0.01μF |
| C11 | 20pF |
| C12 | 15pF |
| C13 | 0.001μF |
| C14 | 18pF |
| C15 | 0.01μF |
| C16 | 0.001μF |
| C17 | 0.001μF |
| C18 | 5μF |
| C19 | 4700pF |
| C20 | 68pF |
| C21 | 12pF |
| C22 | 4pF |
| C23 | 82pF |
| C24 | 0.047μF |
| C25 | 0.047μF |
| C26 | 0.01μF |
| C27 | 0.047μF |

| Inductors | RCA Stock No. |
|---|---|
| L1 | 131655 |
| L2 | 133463 |
| L3 | 1.0μH |
| L4 | 12.0μH |
| L5 | 134754* |
| L6 | 131465 |
| L7 | 133546 |
| L8 | 130120 |
| L9 | 130121 |

*(9 turns No. 23 wire; use 1/2 W resistor to form coil)

**Resistors (All values in ohms)**

| | |
|---|---|
| R1 | 18 |
| R2 | 27 |
| R3 | 91 |
| R4 | 15k |
| R5 | 3.3k |
| R6 | 10k |
| R7 | 1.0k |
| R8 | 33k |
| R9 | 51k |
| R10 | 270 |
| R11 | 2.2k |
| R12 | 120k |
| R13 | 2.2k |
| R14 | 15k |
| R15 | 25k |
| R16 | 8.2k |
| R17 | 2.2k |
| R18 | 3.3k |
| R19 | 150 |
| R20 | 56 |
| R21 | 36 |
| R22 | 220 |
| R23 | 5.6k |

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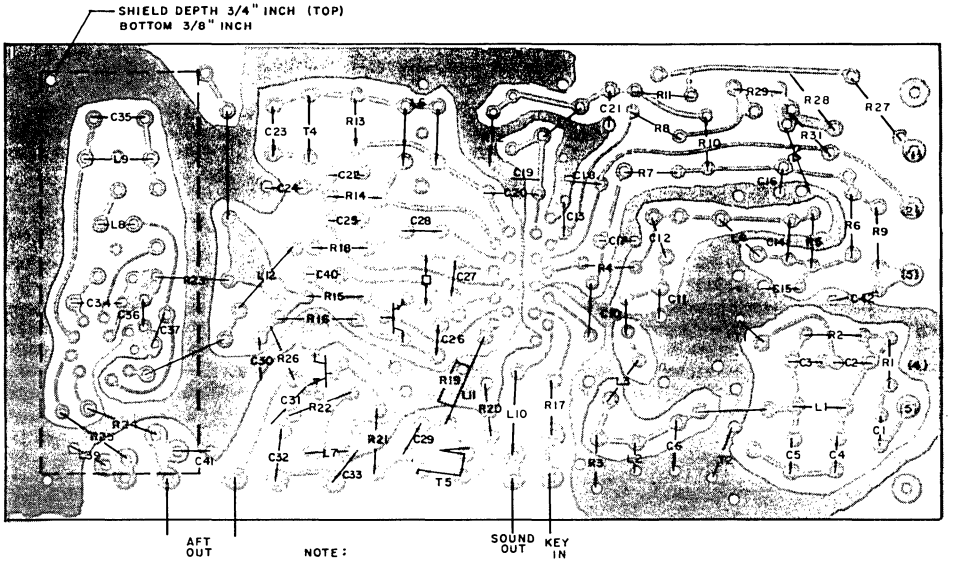
## THE COLOR CIRCUIT




NOTE:

(1) + 30 VOLTS
(2) TUNER AGC
(3) CONTROL AGC
(4) GND
(5) INPUT

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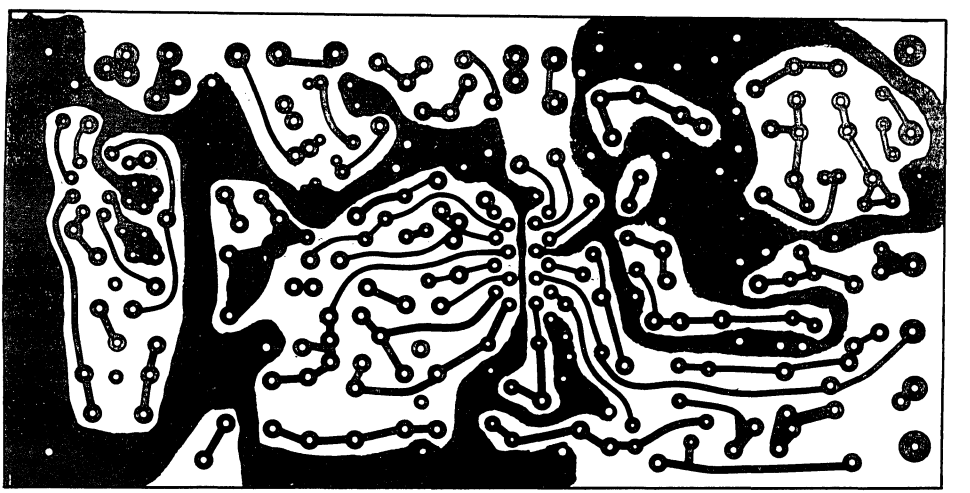
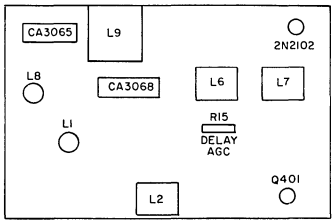


## THE MONOCHROME CIRCUIT

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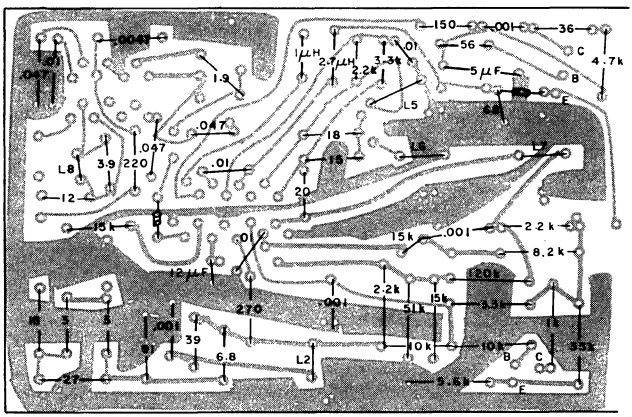
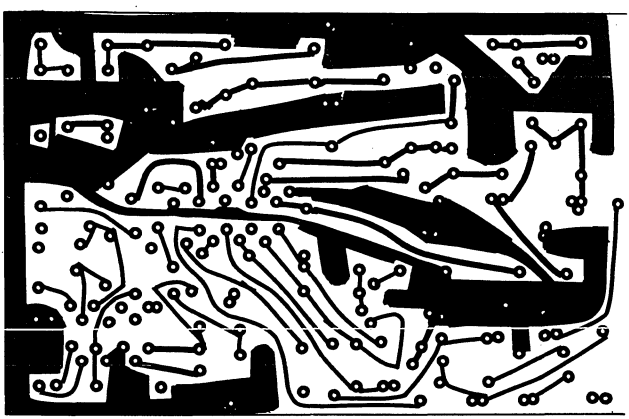


# Applications of the RCA-CA3062 IC Photo-Detector and Power Amplifier in Switching Circuits

by J. D. Mazgy

The RCA CA3062 is a monolithic silicon integrated circuit consisting of a photosensitive detector and a switching amplifier with a pair of high current output transistors. This note describes how the CA3062 with only 3 resistors can provide a light activated switch which will drive a variety of practical loads; such as solenoids, relays, triacs, SCR's, etc. "Normally ON" and "Normally OFF" outputs are available simultaneously.

### Circuit Description

The circuit diagram and terminal connections for the CA3062 are shown in Fig. 1. The circuit consists of a photo-Darlington pair and a differential amplifier which is emitter-follower coupled to a pair of high-current output transistors, $Q_6$ and $Q_7$.

### Circuit Operation

The CA3062 is designed for operation from power supply voltages of 5 to 15 volts between terminal Nos. 4 and 8, and voltages as high as 30 volts V+ on the output transistors.

The photo-detector system consists of four silicon transistors $Q_1$ and $Q_9$, with $Q_{10}$ and $Q_{11}$ in a parallel-connected Darlington circuit. The Darlington configuration is used to provide maximum photo current from the available detector area. The area of each photo-transistor is $1.3 \times 10^{-4}$ cm$^2$. However, the effective photo-sensitive area is $2.6 \times 10^{-4}$cm$^2$ because transistors $Q_1$ and $Q_{11}$ of each Darlington contribute a relatively small percentage of the total photo-current.

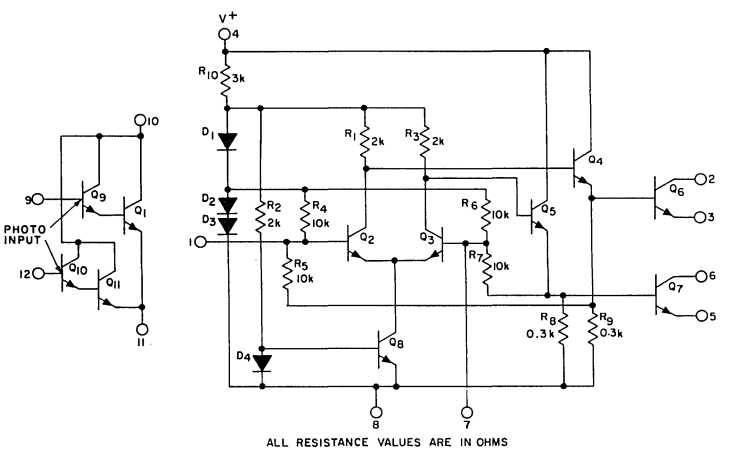



*Fig. 1 – Schematic diagram of CA3062.*

Fig. 2 shows a typical curve of photo-current in the collector and base as a function of light intensity. Fig. 3a & b shows the test set up used to obtain the data for Fig. 2. A typical spectral response curve of the photo sensitive Darlington is shown in Fig. 4. Fig. 5 shows typical rise and fall times for the photo detector output.

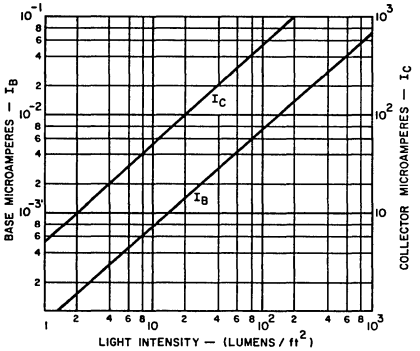



*Fig. 2 – Typical $I_C$, $I_B$ as a function of light intensity at 25°C.*

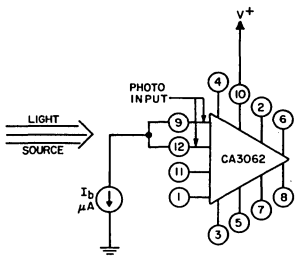



*Fig. 3a – Base current test set-up.*

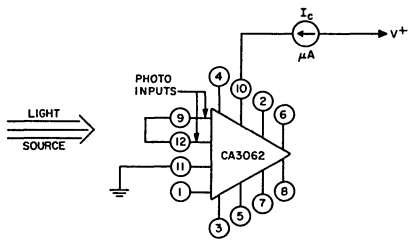



*Fig. 3b – Collector current test set-up.*

*Fig. 3 – Test circuits.*

The photo Darlington pair can be either emitter-coupled or collector-coupled to the differential amplifier consisting of $Q_2$ and $Q_3$ and constant current sink $Q_8$, operating with a total current of 0.7mA as shown in Figs. 6a and 6b,

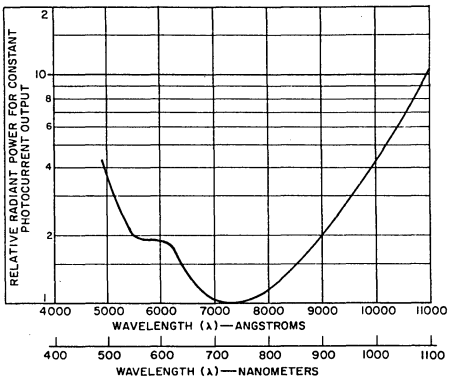



*Fig. 4 – Typical spectral response of photosensitive Darlington unit.*

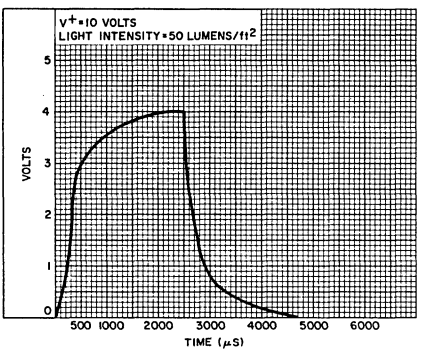



*Fig. 5 – Typical photo-Darlington response.*

respectively. The emitter-coupled mode is generally recommended. However, there are applications in which the collector-coupled mode is advantageous. Examples of the collector-coupled mode are shown in Figs. 8, 12 & 13.

In a balanced condition $Q_2$ and $Q_3$ are conducting 0.35mA each, which sets the dc voltage of each of the collectors of $Q_2$ and $Q_3$ at 0.7 volt below the three diode drops of $D_1$, $D_2$ and $D_3$.

With the dc potential on collectors $Q_2$ and $Q_3$ determined to be +1.4 volts above reference terminal No. 8, the voltage on the emitters of $Q_4$ and $Q_5$ then is 0.7 volt below the respective base, and, therefore, +0.7 volt above the reference point. Thus, the base potentials of $Q_2$ and $Q_3$ are set to +1.05 volts and +0.7 volt for $Q_6$ and $Q_7$, respectively. The emitter currents of $Q_4$ and $Q_5$ are set to approximately 2.33mA each under the balanced condition.

The input resistance at terminal No. 1 is approximately 1.4kΩ in the balanced mode with signals less than ±25mV.

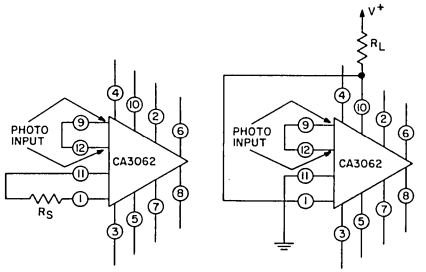



*Fig. 6a – Emitter Coupled.* *Fig. 6b – Collector Coupled.*

*Fig. 6 – Methods of coupling photo-detector to amplifier portion of CA3062.*

**Recommended Operating Circuit:**

To assure positive transistion between the "ON" and "OFF"states, Schmitt trigger operation is recommended.

Schmitt trigger operation can be achieved by connecting the CA3062 as shown in the circuit of Fig. 7. $R_f$ provides the positive feedback which causes $Q_3$ to conduct and holds $Q_7$ in cut-off. A positive going voltage applied to terminal No. 1 will result in a change of output state. Resistor $R_S$ limits the drive to the differential amplifier when high light levels are encountered. $R_S$ is chosen to insure that the voltage at terminal No. 1 does not exceed 1.9 volts. If this voltage is exceeded, $Q_6$ will turn on. This overdrive condition causes both output transistors to be "ON". ($Q_6$ is supposed to be cutoff when the voltage at terminal No. 1 is more positive than the voltage at terminal No. 7). If the "Normally ON" output at terminal No. 2 is not being used, resistor $R_S$ is not required, and terminal Nos. 2 and 3 should be left unconnected. (See Fig. 7.) The magnitude of the threshold voltage and the amount of hysteresis provided are determined by the value of the feedback resistor Rf. (See appendix for calculations.)

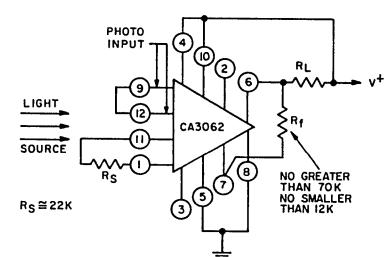



*Fig. 7 – Schmitt-circuit.*

## Typical Applications

**Latched Memory Circuit**

A latched memory system can be used to stop clocks, record an intrusion, or activate light-actuated dark-room controls.

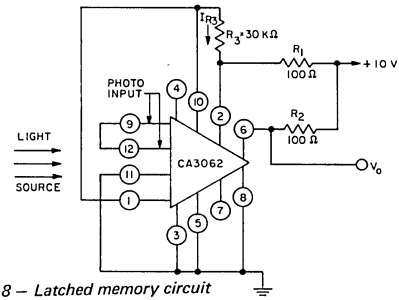



*Fig. 8 – Latched memory circuit*

**Circuit Operation of Latched Memory**

The initial conditions are: terminal No. 2 at "high"-output-voltage and terminal No. 6 at "low"-output-voltage. This condition is assured by the 30kΩ Resistor ($R_3$), which biases $Q_2$ on, $Q_6$ off and $Q_7$ on. When a light pulse is received, $Q_1$ turns on and takes base drive away from $Q_2$, turning on $Q_6$ thereby reversing the initial conditions. $Q_6$ remains on because terminal No. 1 is now more negative than terminal No. 7. Momentary interrupting of V+ will reset the circuit.

The photo current required to trigger a typical circuit is:

$$I_{R_3} \cong \frac{V^+ - V_{B21}}{R_3} = \frac{9}{(30)(10^{-3})} = (300)(10^{-6}) \text{ ampere}$$

More exactly:

$$I_{B3} = \frac{V \pm V_{B21}}{R_3} + \frac{60mV}{R_{B2}}$$

$$I_{R3} = \frac{9}{30 \times 10^{+3}} + \frac{60 \times 10^{-3}}{5 \times 10^{-3}} = \frac{300 \times 10^{-6}}{1} + \frac{60 \times 10^{-6}}{5} = 312 \times 10^{-6}$$

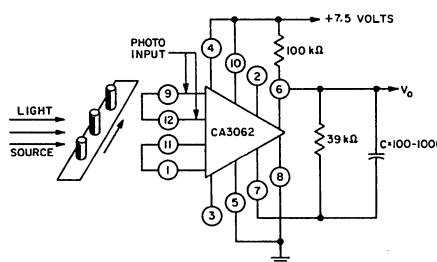



*Fig. 9 – Circuit for slow speed counting level control, position sensor and end-of-tape control.*

or an $I_C$ produced by approximately 50 lumen/ft$^2$ at the photo-detector input. (See Fig. 3.)

Fig. 9 shows a circuit for a Photo-Detector Counting Control, Position Sensor or End-of-Tape Control.

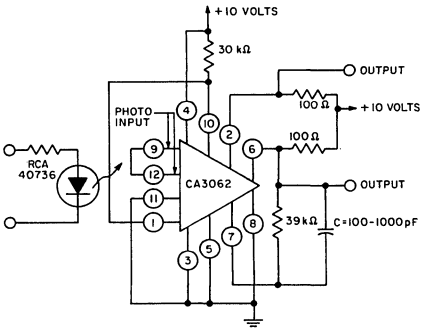



*Fig. 10 – Isolator circuit.*

## TRIAC CONTROL SYSTEMS

### A. Light Activated Triac Control

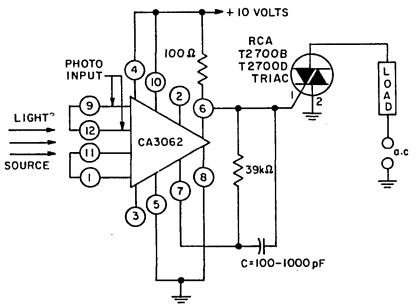



*Fig. 11 – Light activated triac control.*

An Optically Coupled Isolator Circuit, used to transfer signals that are at substantially different voltage levels, is shown in Fig. 10. Both polarity outputs are available. Current transfer ratios of as high as 10:1 can be achieved with this circuit. The design equations for this system are the same as those presented in the appendix.

### B. Triac Control With Safety Feature Providing Automatic Shut Off And Alarm.

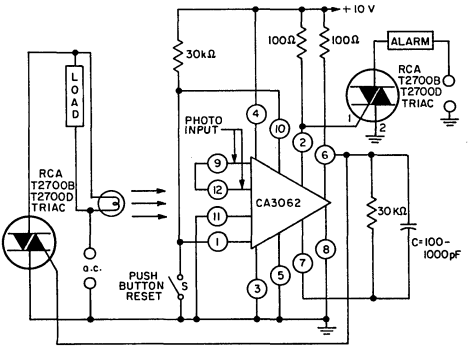



*Fig. 12 – Triac automatic shut off and alarm.*

In this system ac is supplied to the load as long as the light source is "on". If the light path to the CA3062 is broken, then the ac to the load and light source is opened, thereby activating the alarm circuit. The system can be reset with the push-button shown.

### C. Triac Intrusion Alarm System.

If the light path is broken or the ac is interrupted, the alarm system will be activated, provided the battery is adequately charged.

The V+ acts as a charging circuit for the battery while the circuit is operating from the ac supply.

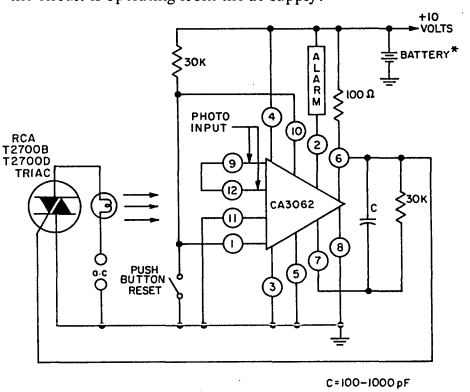



*Fig. 13 – Triac intrusion alarm system.*

## APPENDIX

In general, Schmitt circuits have three voltages of interest.

$V_I$ trigger: the voltage required to trigger the Schmitt from state I to state II.

$V_{II}$ trigger: the voltage required to trigger the Schmitt from state II back to state I.

V hysteresis: the difference between the $V_1$ trigger and $V_2$ trigger. The hysteresis voltage for the configuration described is altered by the internal feedback of the CA3062 circuit which modifies the hysteresis expression.

Fig. a shows a typical configuration for operation as a Schmitt-Circuit.

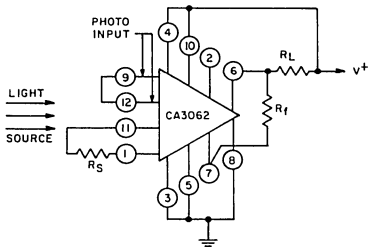



*Fig. a — Schmitt-circuit*

The trigger potential ($V_I$) to go from state I to state II is:

$$V_I \text{ trigger} = \frac{(V^+ - V_{B31})\,R_{B3}}{R_{B3} + R_f + R_L} + \frac{V_{B31}}{1}:$$

Where state I is defined as the case with pin 6 at a "high" output voltage, with no light into the Darlington photodetector. State II is defined as the case with pin 6 at a "low" output voltage, with no light into the Darlington photodetector.

and: $V_{B21} = 1.050\ V$ $\quad R_{B2} = R_4 // R_5$ (Refer to Fig. 1)
$V_{B31} = 0.700\ V$ $\quad R_{B3} = R_6 // R_7$
$V_{B22} = 0.700\ V$
$V_{B32} = 1.050\ V$

The trigger potential ($V_{II}$) to go from state II back to state I is--

$$V_{II} \text{ trigger} = \frac{V_{B32}}{1} - \frac{(V_{B32} - V_{SAT})\,R_{B3}}{R_{B3} + R_f}$$

The hysteresis voltage of the CA3062 Schmitt system is:

$$V \text{ hysteresis} = \left[\frac{(V^+ - V_{B31})\,R_{B3}}{R_{B3} + R_f + R_L} + \frac{V_{B31}}{1} + \frac{V_{B22}}{1} - \frac{V_{B21}}{1}\right] - \left[\frac{V_{B32}}{1} - \frac{(V_{B32} - V_{SAT})\,R_{B3}}{R_{B3} + R_f}\right]$$

The light intensity required to switch from state I to state II is determined from Fig. 2, which shows the number of lumens/ft$^2$ necessary to generate $I_{CI}$.

$$I_{CI} = \frac{V_{SIG\ I}}{R_{B2}} = \frac{V_{SIG\ I}}{5 \times 10^3}$$

where:

$$V_{SIG\ I} = \frac{(V^+ - V_{B31})\,R_{B3}}{R_{B3} + R_f + R_L} + \frac{V_{B31}}{1} - \frac{V_{B21}}{1}$$

To determine the lumens/ft$^2$ required to go from state II back to state I, it is necessary to calculate $V_{SIG\ II} + V_{B22}$, (the voltage required to cause the Schmitt circuit to switch).

$$V_{SIG\ II} + V_{B22} = \frac{V_{B32}}{1} - \frac{(V_{B32} - V_{SAT})\,R_{B3}}{R_{B3} + R_f}$$

Thus:

$$V_{SIG\ II} = V_{B32} - \left[\frac{(V_{B32} - V_{SAT})\,R_{B3}}{R_{B3} + R_f}\right] - \left[\frac{V_{B22}}{1}\right]$$

and:

$$I_{CII} = \frac{V_{SIG\ II}}{R_{B2}} = \frac{V_{SIG\ II}}{5k}$$

The rate at which $V_{SIG}$ rises is governed by the response of the photo Darlington pair.

$V_{SIG}$ during the rise time assumes a value:

$$V_{SIG} = V_m\,(1 - e^{\frac{-t}{RC}});$$

where $V_m$ is the maximum signal voltage developed across terminal No. 1 and reference terminal No. 8 for any given light intensity. [See Fig. 4.].

The rise time of a typical photo Darlington of the CA3062 is:

$$t_r = \frac{RC \log \left[\frac{1}{1 - \frac{V_c}{V_m}}\right]}{\log e}$$

where $R = 40 \times 10^6$ and $C = 8 \times 10^{-12}$ and $V_C$ any part of $V_m$.

**APPENDIX (cont'd.)**

By setting $V_C = V_{SIG\ I}$ the delay time, $t_d$, of the pulse output of the Schmitt circuit can be determined for any given light intensity.

The rate at which the photo Darlington output decreases is:

$$V_{SIG} = V_m e^{\frac{-t}{RC}}$$

Thus the fall time is

$$t_f = \frac{RC \log \frac{V_m}{V'_c}}{\log e}$$

Setting $V_C = V_{SIG\ II}$, then $t_f$ becomes $t_d$ which is turn off delay time, or the time the Schmitt circuit turns off with respect to the time the light input to the photo Darlington has been turned off. See Fig. b.

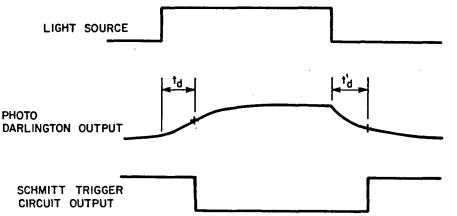



*Fig. b — Waveforms for rise and fall response.*

# Applications of the CA3080 and CA3080A High-Performance Operational Transconductance Amplifiers

by H. A. Wittlinger

The CA3080 and CA3080A are similar in generic form to conventional operational amplifiers, but differ sufficiently to justify an explanation of their unique characteristics. This new class of operational amplifier not only includes the usual differential input terminals, but also contains an additional control terminal which enhances the device's flexibility for use in a broad spectrum of applications. The amplifier incorporated in these devices is referred to as an Operational Transconductance Amplifier (OTA), because its output signal is best described in terms of the output-current that it can supply. (Transconductance $g_m = \frac{\triangle i_{out}}{\triangle e_{in}}$). The amplifier's output-current is proportional to the voltage difference at its differential input terminals.

This Note describes the operation of the OTA and features various circuits using the OTA. For example, communications and industrial applications including modulators, multiplexers, sample-and-hold-circuits, gain control circuits and micropower comparators are shown and discussed. In addition, circuits have been included to show the operation of the OTA being used in conjunction with RCA COS/MOS devices as post-amplifiers.

Fig. 1 shows the equivalent circuit for the OTA. The output signal is a "current" which is proportional to the transconductance (gm) of the OTA established by the amplifier bias current ($I_{ABC}$) and the differential input voltage. The OTA can either source or sink current at the output terminals, depending on the polarity of the input signal.

The availability of the amplifier bias current ($I_{ABC}$) terminal significantly increases the flexibility of the OTA and permits the circuit designer to exercise his creativity in the utilization of this device in many unique applications not possible with the conventional operational amplifier.

### Circuit Description

A simplified block diagram of the OTA is shown in Fig. 2. Transistors Q1 and Q2 comprise the differential input amplifier found in most operational amplifiers, while the lettered-circles (with arrows leading either into or out of the circles) denote "current-mirrors". Fig. 3a shows the basic type of current-mirror which is comprised of two transistors, one of which is diode-connected. In a "current-mirror", with similar geometries for $Q_A$ and $Q_B$, the current I' establishes a second current I whose value is essentially equal to that of I'.

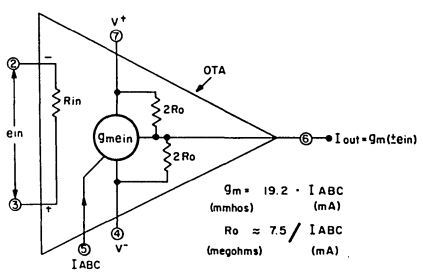



*Fig. 1— Basic equivalent circuit of the OTA.*

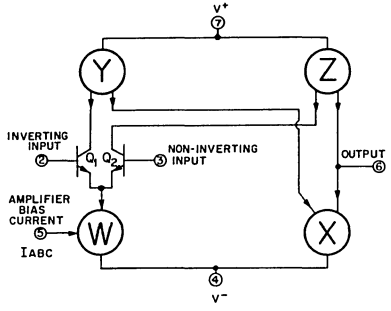



*Fig. 2— Simplified diagram of OTA.*

This basic current-mirror configuration is sensitive to the transistor beta ($\beta$). The addition of another active transistor, shown in Fig. 3b, greatly diminishes the circuit sensitivity to transistor beta ($\beta$) and increases the current-source output impedance in direct proportion to the transistor beta ($\beta$). Current-mirror W (Fig. 2) uses the configuration shown in Fig. 3a, while mirrors X, Y, and Z are basically the version shown in Fig. 3b. Mirrors Y and Z employ p-n-p transistors, as depicted by the arrows pointing outward from the mirrors. Appendix 1 describes "current-mirrors" in more detail.

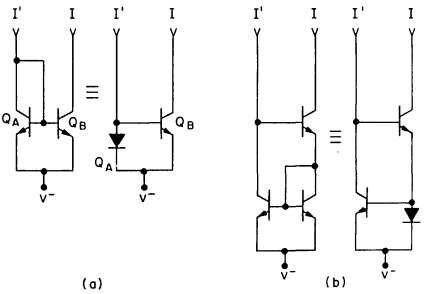



*Fig. 3— Basic types of current mirrors; a) diode-connected transistor paired with transistor; b) improved version: employs an extra transistor.*

Fig. 4 is the complete schematic diagram of the OTA. The OTA employs only active devices (transistors and diodes). Current applied to the amplifier-bias-current terminal, $I_{ABC}$, establishes the emitter current of the input differential amplifier Q1 and Q2. Hence, effective control of the differential transconductance ($g_m$) is achieved.

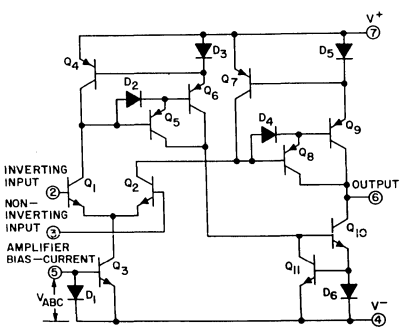



*Fig. 4— Schematic diagram of OTA types CA3080 and CA3080A.*

The $g_m$ of a differential amplifier is equal to

$$\frac{qaI_C}{2KT}$$

(see Ref. 2 for derivation) where q is the charge on an electron, $a$ is the ratio of collector current to emitter current of the differential amplifier transistors, (assumed to be 0.99 in this case), $I_C$ is the collector current of the constant-current source ($I_{ABC}$ in this case), K is Boltzman's constant, and T is the ambient temperature in degrees Kelvin. At room temperature, $g_m = 19.2 \times I_{ABC}$, where gm is in mmho and $I_{ABC}$ is in milliamperes. The temperature coefficient of $g_m$ is approximately -0.33%/°C (at room temperature).

Transistor Q3 and diode D1 (shown in Fig. 4) comprise the current mirror "W" of Fig. 2. Similarly, transistors Q7, Q8 and Q9 and diode D5 of Fig. 4 comprise the generic current mirror "Z" of Fig. 2. Darlington-connected transistors are employed in mirrors "Y" and "Z" to reduce the voltage sensitivity of the mirror, by the increase of the mirror output impedance. Transistors Q10, Q11, and diode D6 of Fig. 2 comprise the current-mirror "X" of Fig. 2. Diodes D2 and D4 are connected across the base-emitter junctions of Q5 and Q8, respectively, to improve the circuit speed. The amplifier output signal is derived from the collectors of the

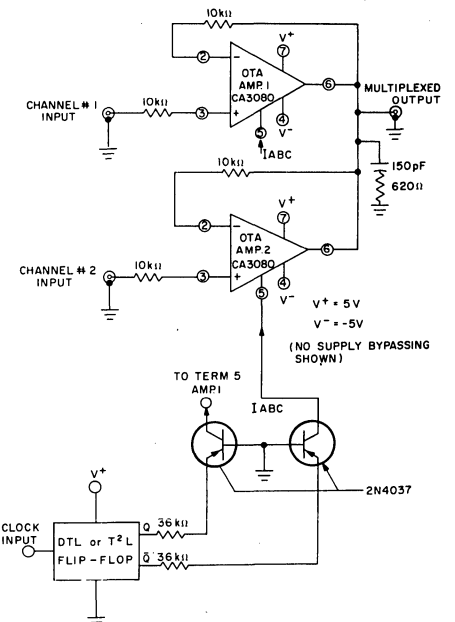



*Fig. 5— Schematic diagram of OTAs in a two-channel linear time-shared multiplex circuit.*

"Z" and "X" current-mirror of Fig. 2, providing a push-pull Class A output stage that produces full differential $g_m$. This circuit description applies to both the CA3080 and CA3080A. The CA3080A offers tighter control of $g_m$ and input offset voltage, less variation of input offset voltage with variation of $I_{ABC}$ and controlled cut-off leakage current. In the CA3080A, both the output and the input cut-off leakage resistances are greater than 1,000 MΩ.

## APPLICATIONS

### Multiplexing

The availability of the bias current terminal, $I_{ABC}$, allows the device to be gated for multiplex applications. Fig. 5 shows a simple two-channel multiplex system using two CA3080 OTA devices. The maximum level-shift from input to output is low (approximately 2mV for the CA3080A and 5mV for the CA3080). This shift is determined by the amplifier input offset voltage of the particular device used, because the open-loop gain of the system is typically 100dB when the loading on the output of the CA3080A is low. To further increase the gain and reduce the effects of loading, an additional buffer and/or gain-stage may be added. Methods will be shown to successfully perform these functions.

In this example positive and negative 5-V power-supplies were used, with the IC flip-flop powered by the positive supply. The negative supply-voltage may be increased to -15 V, with the positive-supply at 5 V to satisfy the logic supply voltage requirements. Outputs from the clocked flip-flop are applied through p-n-p transistors to gate the CA3080 amplifier-bias-current terminals. The grounded-base configuration is used to minimize capacitive feed-through coupling via the base-collector junction of the p-n-p transistor.

Another multiplex system using the OTA's clocked by a COS/MOS flip-flop is shown in Fig. 6. The high output voltage capability of the COS/MOS flip-flop permits the circuit to be driven directly without the need for p-n-p level-shifting transistors.

A simple RC phase-compensation network is used on the output of the OTA in the circuits shown in Figs. 5 & 6. The values of the RC-network are chosen so that $\frac{1}{2\pi RC} \simeq 2\text{MHz}$. This RC-network is connected to the point shown because the lowest-frequency pole for the system is usually found at this point. Fig. 7 shows an oscilloscope photograph of the multiplex circuit functioning with two input signals. Fig. 8 shows an oscilloscope photograph of the output of the multiplexer with a 6-V p-p, sine wave signal (22 kHz) applied to one amplifier and the input to the other amplifier grounded. This photograph demonstrates an isolation of at least 80 dB between channels.

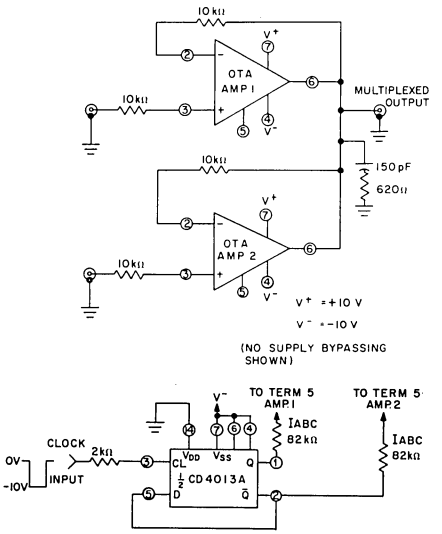
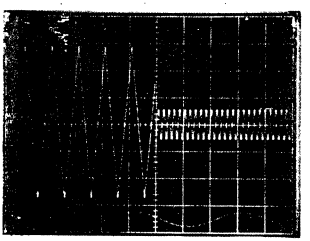
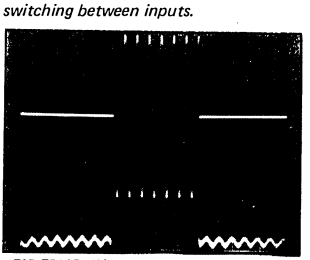



*Fig. 6— Schematic diagram of a two-channel linear multiplex system using a COS/MOS flip-flop to gate two OTAs.*



TOP TRACE: MULTIPLEXED OUTPUT 1 V/DIV & 100μsec/DIV
BOTTOM TRACE: TIME EXPANSION OF SWITCHING BETWEEN INPUTS 2 V/DIV & 5 μsec/DIV

*Fig. 7— Voltage waveforms for circuit of Fig. 6; top trace: multiplexed output; lower trace: time expansion of switching between inputs.*



TOP TRACE: 1 V/DIV & 100μsec/DIV —OUTPUT
BOTTOM TRACE: VOLTAGE EXPANSION OF OUTPUT 1mV/DIV & 100μsec/DIV ISOLATION IS IN EXCESS OF 80 db

*Fig. 8— Voltage waveforms for circuit of Fig. 6; top trace: output; lower trace: voltage expansion of output; isolation in excess of 80 dB.*

**Sample-and-Hold Circuits**

An extension of the multiplex system application is a sample-and-hold circuit (Fig. 9), using the strobing characteristics of the OTA amplifier bias-current (ABC) terminal as a means of control. Fig. 9 shows the basic system using the CA3080A as an OTA in a simple voltage-follower configuration with the phase-compensation capacitor serving the additional function of sampled-signal storage. The major consideration for the use of this method to "hold" charge is that neither the charging amplifier nor the signal readout device significantly alter the charge stored on the capacitor. The CA3080A is a particularly suitable capacitor-charging amplifier because its output resistance is more than 1000 MΩ under cut-off conditions, and the loading on the storage capacitor during the hold-mode is minimized. An effective solution to the read-out requirement involves the use of an RCA 3N138 insulated-gate field-effect transistor (MOS/FET) in the feedback loop. This transistor has a maximum gate-leakage current of 10 picoamperes; its loading on the charge "holding" capacitor is negligible. The open-loop voltage-gain of the system (Fig. 9) is approximately 100 dB if the MOS/FET is used in the source-follower mode to the CA3080A as the input amplifier. The open-loop output impedance $(\frac{1}{g_m})$ of the 3N138 is approximately 220 Ω because its transconductance is about 4,600 μmho at an operating current of 5 mA. When the CA3080A drives the 3N138 (Fig. 9), the closed loop operational-amplifier output impedance characteristic

$$Z_{out} \cong \frac{Z_o \text{ (open-loop)}}{A \text{ (open-loop voltage-gain)}}$$

$$\cong \frac{220\ \Omega}{100\text{dB}} \cong \frac{220\ \Omega}{10^5} \cong 0.0022\ \Omega$$

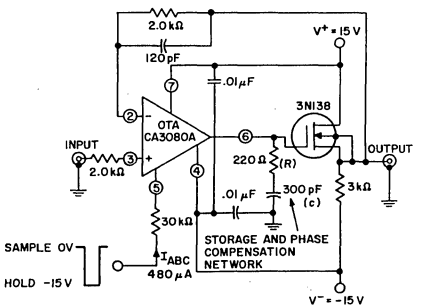
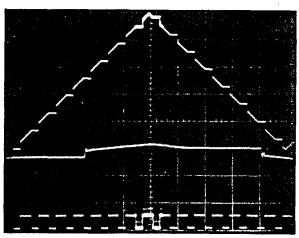



*Fig. 9— Schematic diagram of OTA in a sample-and-hold circuit.*

Fig. 10 shows a "sampled" triangular signal. The lower trace in the photograph is the sampling signal. When this signal goes negative, the CA3080A is cutoff and the signal is "held" on the storage capacitor, as shown by the plateaus on the triangular wave-form. The center trace is a time expansion of the top-most transition (in the upper trace) with a time scale of 2 μsec/div.

Once the signal is acquired, variation in the stored-signal level during the hold-period is of concern. This variation is primarily a function of the cutoff leakage current of the CA3080A (a maximum limit of 5 ηA), the leakage of the storage element, and other extraneous paths. These leakage currents may be either "positive" or "negative" and, consequently, the stored-signal may rise or fall during the "hold" interval. The term "tilt" is used to describe this condition. Fig. 11 shows the expected pulse "tilt" in microvolts as a function of time for various values of the compensation/storage capacitor. The horizontal axis shows three scales representing leakage currents of 50 ηA, 5 ηA, 500 pA.

Fig. 12 shows a dual-trace photograph of a triangular signal being "sampled-and-held" for approximately 14 ms with a 300 pF storage capacitor. The center trace (expanded to 20 mV/div) shows the worst-case "tilt" for all the steps shown in the upper trace. The total equivalent leakage current in this case is only 170 pA $(I = C\frac{dv}{dt})$.



TOP TRACE:SAMPLED SIGNAL 1V/DIV & 20μsec/DIV
CENTER TRACE:TOP PORTION OF UPPER SIGNAL 1 V/DIV & 2μsec/DIV
BOTTOM TRACE:SAMPLING SIGNAL 20V/DIV & 20μsec/DIV

*Fig. 10— Waveforms for circuit of Fig. 9; top trace: sampled signal; center trace: top portion of upper signal; lower trace: sampling signal.*

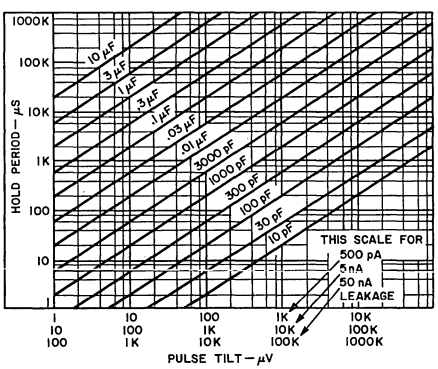
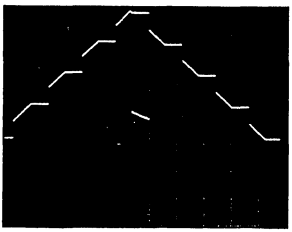


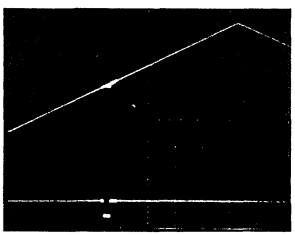

*Fig. 11— Chart showing "tilt" in sample-and-hold potentials as a function of hold time with load capacitance as a parameter.*

Fig. 13 is an oscilloscope photograph of a ramp voltage being sampled by the "sample-and-hold" circuit of Fig. 9. The input signal and sampled-output signal are superimposed. The lower trace shows the sampling signal. Data shown in Fig. 13 were recorded with supply voltages of ±10 V and the series input resistor at terminal 5 was 22 kΩ.



TOP TRACE:SAMPLED SIGNAL 1V/DIV & 20msec/DIV
CENTER TRACE:WORSE CASE TILT 20mV/DIV & 20msec/DIV

*Fig. 12– Oscilloscope photo of "triangular-voltage" being sampled by circuit of Fig. 9.*



TOP TRACE:INPUT AND OUTPUT SUPERIMPOSED 1V/DIV & 2μsec/DIV
BOTTOM TRACE:SAMPLING SIGNAL 20V/DIV & 2μsec/DIV

*Fig. 13– Oscilloscope photo of "ramp-voltage" being sampled by circuit of Fig. 9.*

In Fig. 14, the trace of Fig. 13 has been expanded (100 mV/div and 100 ηsec/div) to show the response of the sample-and-hold circuit with respect to the sampling signal. After the sampling interval, the amplifier overshoots the signal level and settles (within the amplifier offset voltage) in approximately 1 μs. The resistor in series with the 300 pF phase-compensation capacitor was adjusted to 68 ohms for minimum recovery time.

Fig. 15 shows the basic circuit of Fig. 9 implemented with an RCA 2N4037 p-n-p transistor to minimize capacitive feedthrough. Fig. 16 shows oscilloscope photographs taken with the circuit of Fig. 15 operating in the sampling mode at supply-voltage of ±15 V. The 9.1 kΩ resistor in series with the p-n-p transistor emitter establishes amplifier-bias-current ($I_{ABC}$) conditions similar to those used in the circuit of Fig. 9.

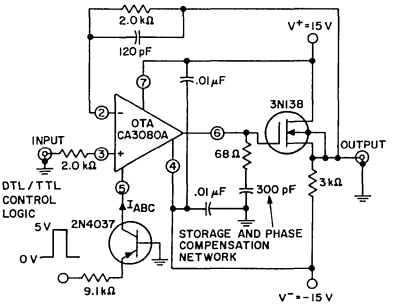
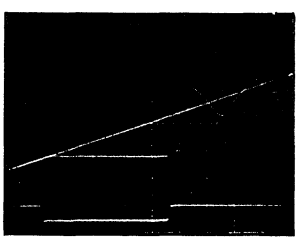


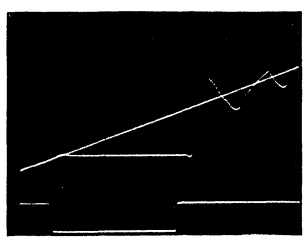

*Fig. 15– Schematic diagram of the OTA in a sample-and-hold configuration (DTL/TTL control logic).*

Considerations of circuit stability and signal retention require the use of the largest possible phase-compensation capacitor, compatible with the required slew rate. In most systems the capacitor is chosen for the maximum allowable "tilt" in the storage mode and the resistor is chosen so that $\frac{1}{2\pi RC} \simeq$ 2MHz, corresponding to the first pole in the



TOP TRACE: INPUT AND SAMPLED OUTPUT SUPERIMPOSED 100mV/DIV & 100 ns/DIV
BOTTOM TRACE:SAMPLING SIGNAL 20V/DIV & 100 ns/DIV

*Fig. 14– Oscilloscope photo showing response of sample-and-hold circuit (Fig. 9).*



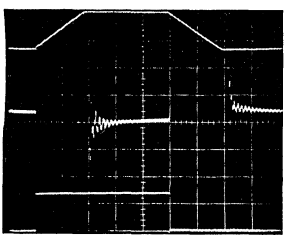
TOP TRACE:INPUT AND SAMPLED OUTPUT SUPERIMPOSED 100mV/DIV & 100ns/DIV
BOTTOM TRACE:SAMPLING SIGNAL 5V/DIV & 100 ns/DIV

*Fig. 16– Oscilloscope photo for circuit of Fig. 15 operating in sampling mode.*

amplifier at an output current level of 500 μA. It is frequently desirable to optimize the system response by the placement of a small variable resistor in series with the capacitor, as is shown in Figs. 9 and 15. The 120 pF capacitor shunting the 2 kΩ resistor improves the amplifier transient response.

Fig. 17 shows a multi-trace oscilloscope photograph of input and output signals for the circuit of Fig. 9, operating in the linear mode. The lower portion of the photograph shows the input signal, and the upper portion shows the output signal. The amplifier slew-rate is determined by the output current and the capacitive loading: in this case the slew rate (dV/dt) = 1.8V/μs.

The center trace in Fig. 17 shows the difference between the input and output signals as displayed on a Tektronix 7A13 differential amplifier at 2 mV/div. The output of the amplifier system settles to within 2 mV (the offset voltage specification for the CA3080A) of the input level in 1 μs after slewing.



TOP TRACE: OUTPUT 5V/DIV & 2μsec/DIV
CENTER TRACE: DIFFERENTIAL COMPARSION OF INPUT AND OUTPUT 2mV/DIV— 0 VOLTS THROUGH CENTER— 2μsec/DIV
BOTTOM TRACE: INPUT 5V/DIV & 2μsec/DIV

*Fig. 17— Oscilloscope photo showing circuit of Fig. 9 operating in the linear sample-mode.*

Fig. 18 is a curve of slew-rate as a function of amplifier-bias-current ($I_{ABC}$) with various storage/compensation capacitors. The magnitude of the current being supplied to the storage/compensation capacitor is equal to the amplifier-bias-current ($I_{ABC}$) when the OTA is supplying its maximum output current.

**Gain Control — Amplitude Modulation**

Effective gain control of a signal may be obtained by controlled variation of the amplifier-bias-current ($I_{ABC}$) in the OTA because its $g_m$ is directly proportional to the amplifier-bias-current ($I_{ABC}$). For a specified value of amplifier-bias-current, the output current ($I_O$) is equal to the product of $g_m$ and the input signal magnitude. The output voltage swing is the product of output current ($I_O$) and the load resistance ($R_L$).

Fig. 19 shows the configuration for this form of basic gain control (a modulation system). The output signal current ($I_O$) is equal to $-g_m V_x$; the sign of the output signal is negative because the input signal is applied to the inverting input terminal of the OTA. The transconductance of the OTA is controlled by adjustment of the amplifier bias current, $I_{ABC}$. In this circuit the level of the unmodulated carrier output is established by a particular amplifier-bias-current ($I_{ABC}$) through resistor Rm. Amplitude modulation of the carrier frequency occurs because variation of the voltage Vm forces a change in the amplifier-bias-current ($I_{ABC}$) supplied via resistor Rm. When Vm goes positive the bias current increases which causes a corresponding increase in the $g_m$ of the OTA. When the Vm goes in the negative direction (toward the amplifier-bias-current terminal potential), the amplifier-bias-current decreases, and reduces the $g_m$ of the OTA.

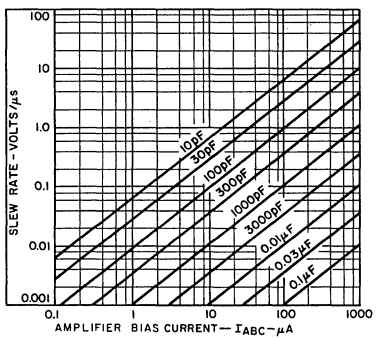



*Fig. 18— Slew rate as a function of amplifier-bias-current ($I_{ABC}$) with phase-compensation capacitance as a parameter.*

As discussed earlier, $g_m = 19.2 \times I_{ABC}$, where $g_m$ is in millimhos when $I_{ABC}$ is in milliamperes. In this case, $I_{ABC}$ is approximately equal to:

$$\frac{Vm - (V^-)}{Rm} = I_{ABC}$$

$$(I_O) = -g_m V_x$$

$$g_m V_x = (19.2)(I_{ABC})(V_x)$$

$$I_O = \frac{-19.2\,[Vm - (V^-)]\,V_x}{Rm}$$

$$I_O = \frac{19.2\,(Vx)\,(V^-)}{Rm} - \frac{19.2\,(Vx)\,(Vm)}{Rm}$$ (Modulation Equation).

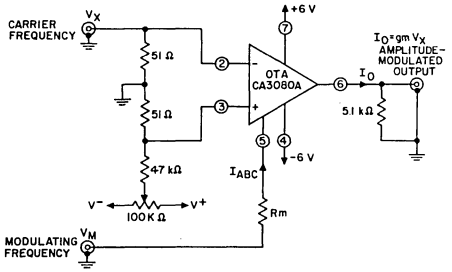



*Fig. 19– Amplitude modulator circuit using the OTA.*

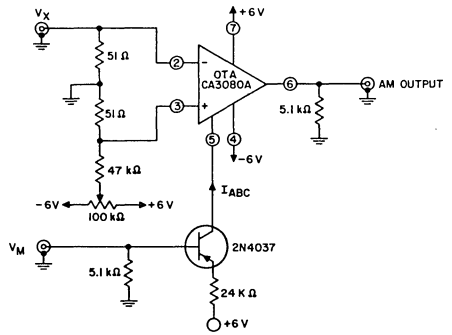



*Fig. 20– Amplitude modulator using OTA controlled by p-n-p transistor.*

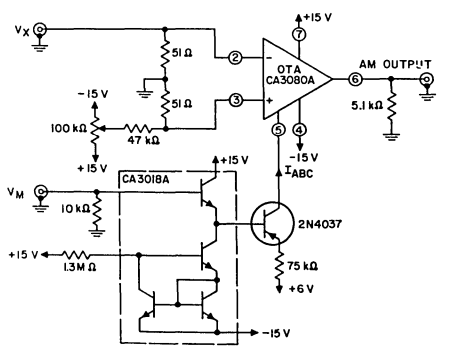



*Fig. 21– Amplitude modulator using OTA controlled by p-n-p and n-p-n transistors.*

There are two terms in the modulation equation: the first term represents the fixed carrier input, independent of Vm, and the second term represents the modulation, which either adds to or subtracts from the first term. When Vm is equal to the V- term, the output is reduced to zero.

In the preceding modulation equations the term

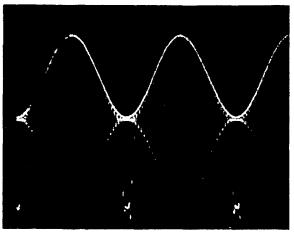
$$(19.2)\,(Vx)\ \frac{V_{ABC}}{Rm}$$

involving the amplifier-bias-current terminal voltage ($V_{ABC}$) (see Fig. 4 for $V_{ABC}$) was neglected. This term was assumed to be small because $V_{ABC}$ is small compared with V- in the equation. If the amplifier-bias-current terminal is driven by a current-source (such as from the collector of a p-n-p transistor), the effect of $V_{ABC}$ variation is eliminated and transferred to the involvement of the p-n-p transistor base-emitter junction characteristics. Fig. 20 shows a method of driving the amplifier-bias-current terminal to effectively remove this latter variation. If an n-p-n transistor is added to the circuit of Fig. 20 as an emitter-follower to drive the p-n-p transistor, variations due to base-emitter characteristics are considerably reduced due to the complementary nature of the n-p-n base-emitter junctions. Moreover, the temperature coefficients of the two base-emitter junctions tend to cancel one another. Fig. 21 shows a configuration using one transistor in the RCA type CA3018A n-p-n transistor-array as an input emitter-follower, with the three remaining transistors of the transistor-array connected as a current-source for the emitter – followers. The 100-kΩ potentiometer shown in these schematics is used to null the effects of amplifier input offset voltage. This potentiometer is adjusted to set the output voltage symmetrically about zero. Figs. 22a and 22b show oscilloscope photographs of the output voltages obtained when the circuit of Fig. 19 is used as a modulator for both sinusoidal and triangular modulating signals. This method of modulation permits a range exceeding 1000:1 in the gain, and thus provides modulation of the carrier input in excess of 99%. The photo in Fig. 22c shows the excellent isolation achieved in this modulator during the "gated-off" condition.

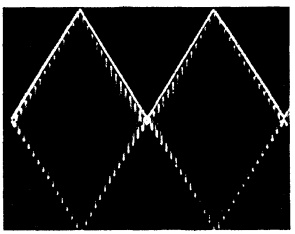
### Four-Quadrant Multipliers

A single CA3080A is especially suited for many low-frequency, low-power four-quadrant multiplier applications. The basic multiplier circuit of Fig. 23 is particularly useful for waveform generation, doubly balanced modulation, and other signal processing applications, in portable equipment, where low-power consumption is essential and accuracy requirements are moderate. The multiplier configuration is basically an extension of the previously discussed gain-controlled configuration (Fig. 19).

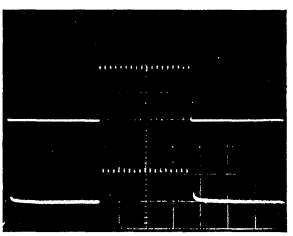
To obtain a four-quadrant multiplier, the first term of the modulation equation (which represents the fixed carrier) must be reduced to zero. This term is reduced to zero by the placement of a feedback resistor (R) between the output and the inverting input terminal of the CA3080A, with the value of the feedback resistor (R) equal to $1/g_m$. The output current is $I_O = g_m\,(-Vx)$ because the input is applied to the



TOP TRACE: MODULATION FREQUENCY INPUT
≃20 VOLTS P-P & 50μsec/DIV
CENTER TRACE: AMPLITUDE MODULATE OUTPUT
500mV/DIV & 50μsec/DIV
BOTTOM TRACE: EXPANDED OUTPUT TO SHOW
DEPTH OF MODULATION 20mV/DIV
& 50μsec/DIV



TOP TRACE: MODULATION FREQUENCY INPUT
20 VOLTS & 50μsec/DIV
BOTTOM TRACE: AMPLITUDE MODULATED OUTPUT
500mV/DIV & 50μsec/DIV



TOP TRACE: GATED OUTPUT 1V/DIV AND 50μsec/DIV
BOTTOM TRACE: VOLTAGE EXPANSION OF ABOVE
SIGNAL-SHOWING NO RESIDUAL
1mV/DIV AND 50μsec/DIV— AT
LEAST 80 db OF ISOLATION
fq = 100 kHz

*Fig. 22– a) Oscilloscope photo of amplitude modulator circuit of Fig. 19 with $R_m$ = 40 kΩ, $V^+$ = 10 v and V- = -10 V. Top trace: modulation frequency input ≃ 20-V p-p; center trace: amplitude modulated output 500-mV/div.; lower trace: expanded output to show depth of modulation, 20 mV/div.; b) triangular modulation; top trace: modulation frequency input ≃ 20 V; lower trace: amplitude modulated output 500 mV/div.; c) square wave modulation, top trace: gated output 1 V/div.; lower trace: expanded scale, showing no residual (1 mV/div) and at least 80 dB of isolation at fq = 100 kHz.*

inverting terminal of the OTA. The output current due to the resistor (R) is $\frac{Vx}{R}$. Hence, the two signals cancel when R = $1/g_m$. The current for this configuration is:

$$I_O = \frac{-19.2\ Vx\ Vm,}{Rm} \text{ and } Vm = Vy$$

The output signal for these configurations is a "current" which is best terminated by a short-circuit. This condition can be satisfied by making the load resistance for the multiplier output very small. Alternatively, the output can be applied to a current-to-voltage converter shown in Fig. 24.

In Fig. 23, the current "cancellation" in the resistor R is a direct function of the OTA differential amplifier linearity. In the following example, the signal excursion is limited to ±10 mV to preserve this linearity. Greater signal-excursions on the input terminal will result in a significant departure from linear operation (which may be entirely satisfactory in many applications).

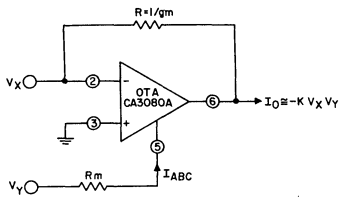



*Fig. 23– Basic four quadrant analog multiplier using an OTA.*

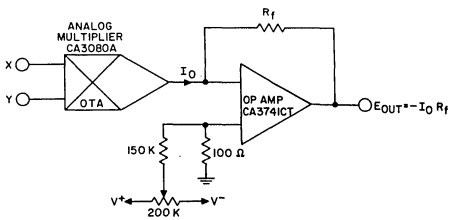



*Fig. 24– OTA analog multiplier driving an op-amp that operates as a current-to-voltage converter.*

Fig. 25 shows a schematic diagram of the basic multiplier with the adjustments set-up to give the multiplier an accuracy of approximately ±7 percent "full-scale". There are only three adjustments: 1) one is on the output, to

compensate for slight variations in the current-transfer ratio of the current-mirrors (which would otherwise result in a symmetrical output about some current level other than zero); 2) the adjustment of the 20-kΩ potentiometer establishes the $g_m$ of the system equal to the value of the fixed resistor shunting the system when the Y-input is zero; 3) compensates for error due to input offset voltage.

Procedure for adjustment of the circuit:

1. a) Set the 1 MΩ output-current balancing potentiometer to the center of its range
   b) Ground the X- and Y- inputs
   c) Adjust the 100 kΩ potentiometer until a zero-V reading is obtained at the output.

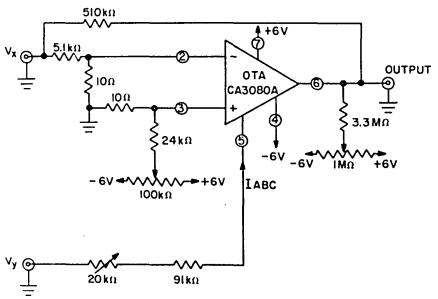



*Fig. 25– Schematic diagram of analog multiplier using OTA.*

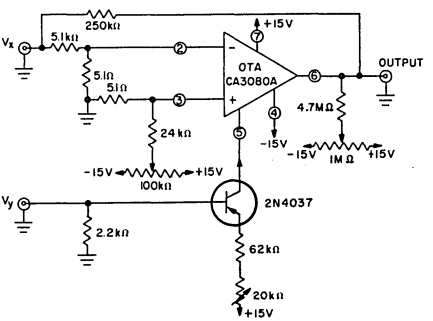
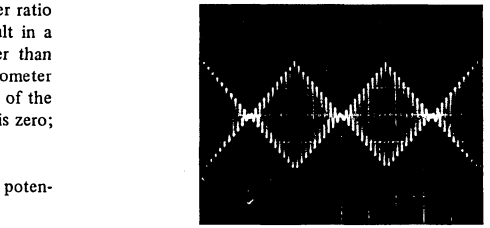
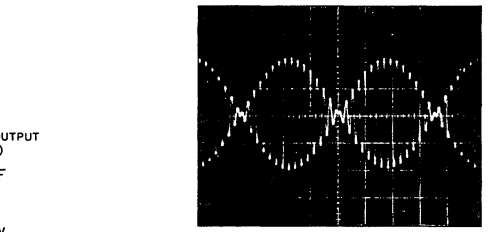


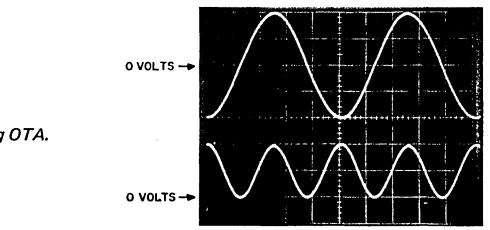

*Fig. 26– Schematic diagram of analog multiplier using OTA controlled by a p-n-p transistor.*



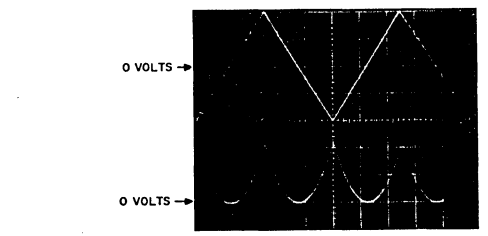
500 mV/DIV AND 200 μsec/DIV
TRIANGLAR INPUT 700 Hz TO $V_Y$ INPUT 5 VPP
CARRIER INPUT 21 kHz TO $V_X$ INPUT 13.5 VPP



500 mV/DIV AND 200μsec/DIV
MODULATING FREQUENCY 700 Hz TO $V_Y$ INPUT 5VPP
CARRIER INPUT 21 kHz TO $V_X$ INPUT 13.5 VPP




TOP TRACE: INPUT TO X AND Y 2V/DIV AND
1 msec/DIV – 200Hz
BOTTOM TRACE: OUTPUT 500mV/DIV AND
1msec/DIV – 400Hz




SAME SCALE AS 27C

*Fig. 27– a) Waveforms observed with OTA analog multiplier used as a suppressed carrier generator; b) waveforms observed with OTA analog multiplier used in signal-squaring circuits.*

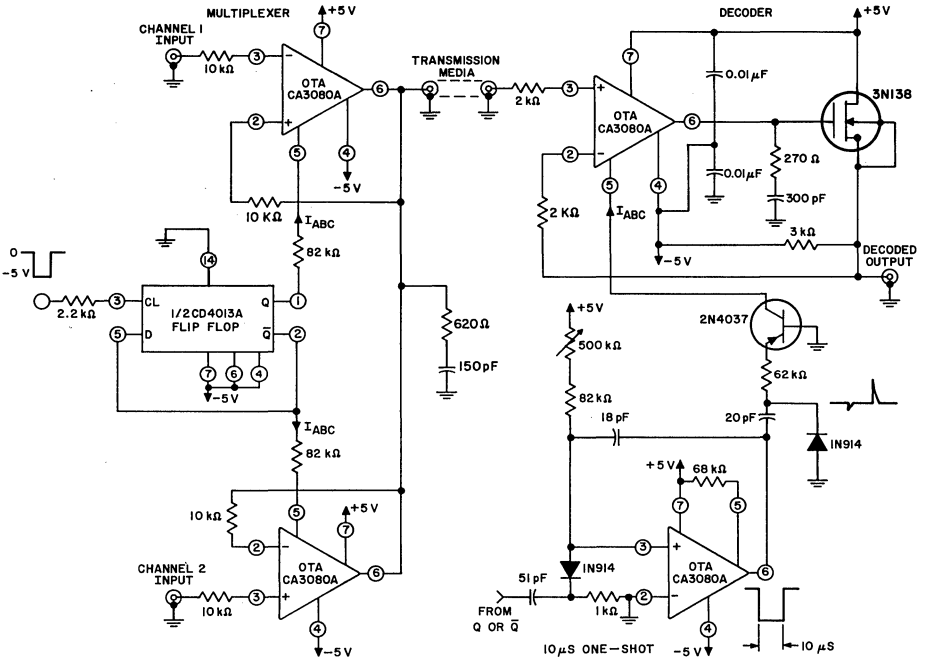



*Fig. 28– Two-channel multiplexer and decoder using OTAs.*

2. a) Ground the Y-input and apply a signal to the X-input through a low source-impedance generator. (It is essential that a low impedance source be used; this minimizes any change in the $g_m$ balance or zero-point due to the 50-μA Y-input bias current).
   b) Adjust the 20-kΩ potentiometer in series with Y-input until a reading of zero-V is obtained at the output. This adjustment establishes the $g_m$ of the CA3080A at the proper level to cancel the output signal. The output current is diverted through the 510-kΩ resistor.
3. a) Ground the X-input and apply a signal to the Y-input through a low source-impedance generator.
   b) Adjust the 1-MΩ resistor for an output voltage of zero-V.

There will be some interaction among the adjustments and the procedure should be repeated to optimize the circuit performance.

Fig. 26 shows the schematic of an analog multiplier circuit with a 2N4037 p-n-p transistor replacing the Y-input "current" resistor. The advantage of this system is the higher input resistance resulting from the current-gain of the p-n-p transistor. The addition of another emitter-follower preceding the p-n-p transistor (shown in Fig. 21) will further increase the current gain while markedly reducing the effect of the $V_{be}$ temperature-dependent characteristic and the offset voltage of the two base-emitter junctions.

Figs. 27a and 27b show oscilloscope photographs of the output signals delivered by the circuit of Fig. 26 which is connected as a suppressed-carrier generator. Figs. 27c and 27d contain photos of the outputs obtained in signal "squaring" circuits, i.e. "squaring" sine-wave and triangular-wave inputs.

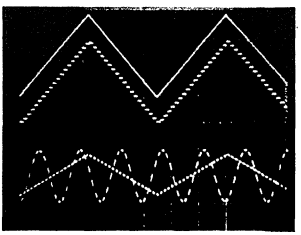
If ±15-V power supplies are used (shown in Fig. 26), both inputs can accept ±10-V input signals. Adjustment of this multiplier circuit is similar to that already described above.

The accuracy and stability of these multipliers are a direct function of the power supply-voltage stability because the Y-input is referred to the negative supply-voltage. Tracking of the positive and negative supply is also important because the balance adjustments for both the offset voltage and output current are also referenced to these supplies.

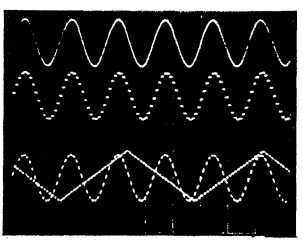
Other forms of four-quadrant multipliers using operational transconductance amplifiers have been published. (See Ref. 2.) the circuit shown in Ref. 2 tends to reduce the effects of the previously discussed $g_m$ temperature dependency.

**Linear Multiplexer – Decoder**

A simple, but effective system for multiplexing and decoding can be assembled with the CA3080 shown in Fig. 28. Only two channels are shown in this schematic, but the number of channels may be extended as desired. Fig. 29 shows oscilloscope photos taken during operation of the multiplexer and decoder. A CA3080 is used as a 10 μsec delay- "one-shot" multivibrator in the decoder to insure that the sample-and-hold circuit can sample only after the input signal has settled. Thus, the trailing edge of the "one-shot" output-signal is used to sample the input at the sample-and-

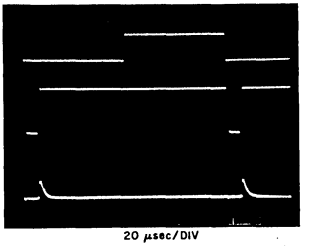


20 msec/DIV
TOP TRACE: INPUT SIGNAL (1 VOLT/DIV)
CENTER TRACE: RECOVERED OUTPUT (1 VOLT/DIV)
BOTTOM TRACE: MULTIPLEXED SIGNALS (2 VOLTS/DIV)

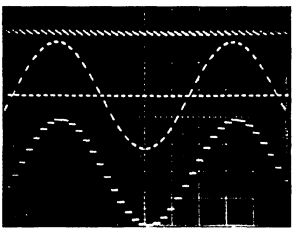


20 msec/DIV
TOP TRACE: INPUT SIGNAL (1 VOLT/DIV)
CENTER TRACE: RECOVERED OUTPUT (1 VOLT/DIV)
BOTTOM TRACE: MULTIPLEXED SIGNALS (1 VOLT/DIV)

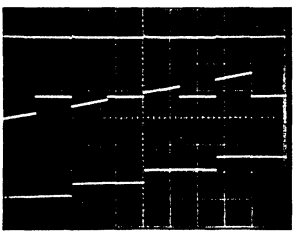
*Fig. 29– Waveforms showing operation of linear multiplexer/sample-and-hold decode circuitry (Fig. 28).*



20 μsec/DIV
TOP TRACE: FLIP-FLOP OUTPUT (5 VOLTS/DIV)
CENTER TRACE: "ONE-SHOT" OUTPUT (5 VOLTS/DIV)
BOTTOM TRACE: PULSE AT THE COLLECTOR OF THE 2N4037 TRANSISTOR (0.1 VOLTS/DIV)



TOP TRACE: COLLECTOR OF PNP TRANSISTOR (0.5 V/DIV)
CENTER TRACE: MULTIPLEXED OUTPUT WITH ONE CHANNEL INPUT GROUND (0.5V/DIV)
LOWER TRACE: DECODED OUTPUT (0.5 V/DIV)
TIME ALL SCALES: 5 msec/DIV



TIME EXPANSION TO 500 μsec/DIV

*Fig. 30– (a) Waveforms showing timing of flip-flop, delay– "one-shot" and the strobing pulse to the sample-and-hold circuit (Fig. 28): top trace: flip-flop output (5 V/div); center trace: "one-shot" output (5 V/div); lower trace: pulse at collector of 2N4037 transistor (0.1 V/div); b) Waveforms showing the decoding operation from the decoder keying pulse (top traces) to the recovered "decoded" sampled output (lower traces). 1) top trace: collector of 2N4037; center trace: multiplexed output with one channel input grounded; lower trace: decoded output; 2) Expanded scale of (1).*

hold circuit for approximately 1 μs. Fig. 30 shows oscilloscope photos of various waveforms observed during operation of the multiplexer/decoder circuit. Either the Q or $\overline{Q}$ output from the flip-flop may be used to trigger the 10 μsec "one-shot" to decode a signal.

### High-Gain, High-Current Output Stages

In the previously discussed examples, the OTA has been buffered by a single insulated-gate field-effect-transistor (MOS/FET) shown in Fig. 9. This configuration yields a voltage gain equal to the $(g_m)$ $(R_o)$ product of the CA3080, which is typically 142,000 (103dB). The output voltage and current-swing of the operational amplifier formed by this configuration (Fig. 9) are limited by the 3N138 MOS/FET performance and its source-terminal load. In the positive direction, the MOS/FET may be driven into saturation; the source-load resistance and the MOS/FET characteristics become the factors limiting the output-voltage swing in the negative direction. The available negative-going load current may be kept constant by the return of the source-terminal to a constant-current transistor. Phase compensation is applied at the interface of the CA3080 and the 3N138 MOS/FET shown in Fig. 9.

Another variation of this generic form of amplifier utilizes the RCA CA3600E (COS/MOS) "inverter" as an amplifier driven by the CA3080. Each of the three "inverter"/amplifiers in the CA3600E has a typical voltage gain of 30 dB. The gain of a single COS/MOS "inverter"/amplifier coupled with the 100 dB gain of the CA3080 yields a total forward-gain of about 130 dB. Use of a two-stage

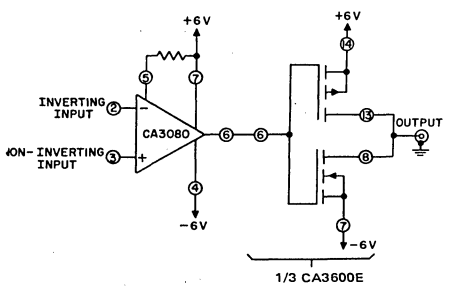



*Fig. 31– Schematic diagram showing OTA driving COS/MOS Inverter/Amplifier (open-loop mode). For greater current output the two remaining amplifiers of the CA3600E may be connected in parallel with the single stage shown. Open-loop gain ≃ 130 dB.*

COS/MOS amplifier configuration will increase the total open-loop gain of the system to about 160 dB (100,000,000). Figs. 31 through 34 show examples of these configurations. Each COS/MOS "inverter"/amplifier can sink or source a current of 6 mA (typ.). In Figs. 33 and 34, two COS/MOS "inverter"/amplifiers have been connected in parallel to provide additional output current.

The open-loop slew-rate of the circuit in Fig. 31 is approximately 65 V/μsec. When compensated for the unity-gain voltage-follower mode, the slew-rate is about 1 V/μsec (shown in Fig. 32). Even when the three "inverter"/

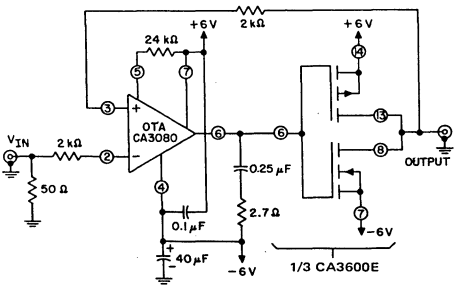



*Fig. 32– Schematic diagram showing OTA driving COS/MOS Inverter/Amplifier (unity-gain closed-loop mode). For greater current output, the two remaining amplifiers of the CA3600E may be connected in parallel with the single stage shown.*

amplifiers in the CA3600E are connected as shown in Fig. 33, the open-loop slew-rate remains at 65 V/μsec. A slew-rate of about 1 V/μsec is maintained with this circuit connected in the unity-gain voltage-follower mode, as shown in Fig. 34. Fig. 35 contains oscilloscope photos of input-output waveforms under small-signal and large-signal conditions for the circuits of Figs. 32 and 34. These photos illustrate the inherent stability of the OTA and COS/MOS circuits operating in concert.

### Precision Multistable Circuits

The micropower capabilities of the CA3080, when combined with the characteristics of the CA3600E COS/MOS "inverter"/amplifiers, are ideally suited for use in connection with precision multistable circuits. In the circuits of Figs. 31, 32, 33, and 34, for example, power-supply current drawn by the COS/MOS "inverter"/amplifier approaches zero as the output voltage swings either positive or negative, while the CA3080 current-drain remains constant.

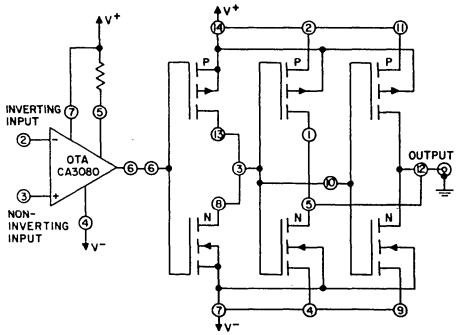



*Fig. 33– Schematic diagram showing OTA driving two-stage COS/MOS Inverter/Amplifier (open-loop mode). gain ≃ 160 dB.*

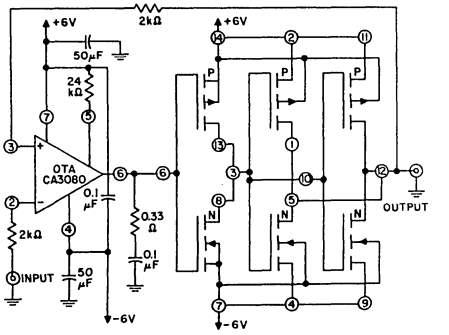
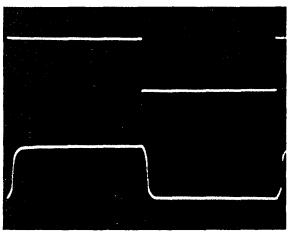


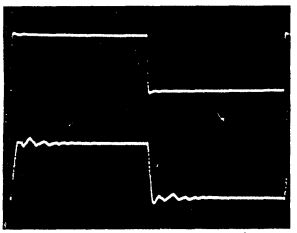

*Fig. 34– Schematic diagram showing OTA driving two-stage COS/MOS Inverter/Amplifier (unity gain closed-loop mode).*

(a)



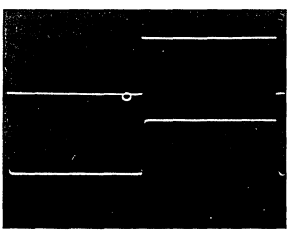
TOP TRACE: INPUT–5 V/DIV–100 μsec/DIV
BOTTOM TRACE : OUTPUT SAME SCALE

(b)



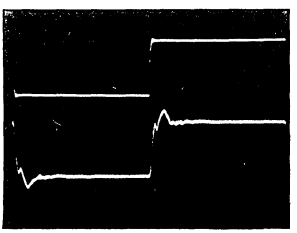
TOP TRACE:INPUT–50 mV/DIV–1 μsec/DIV
BOTTOM TRACE:OUTPUT–SAME SCALE

(c)



TOP TRACE:INPUT–5 V/DIV–100 μsec/DIV
BOTTOM TRACE:OUTPUT–SAME SCALE

(d)



TOP TRACE:INPUT–50 mV/DIV–1 μsec/DIV
BOTTOM TRACE:OUTPUT–SAME SCALE

*Fig. 35– a) Waveforms for circuit of Fig. 32 with large signal input; b) Waveforms for circuit of Fig. 32 with small signal input; c) Waveforms for circuit of Fig. 34 with large signal input; d) Waveforms for circuit of Fig. 34 with small signal input.*

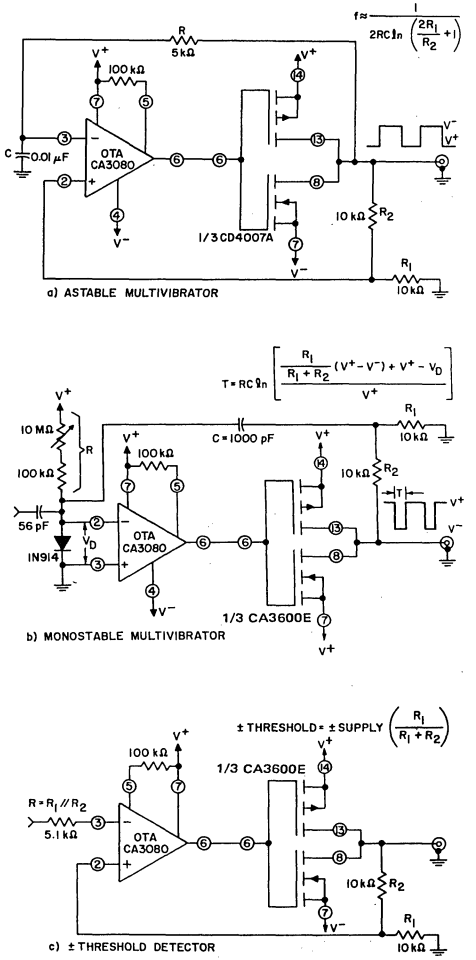



*Fig. 36– Multistable circuits using the OTA and COS/MOS Inverter/Amplifiers: a) astable multivibrator; b) monostable multivibrator; c) threshold detector (plus or minus). For greater current output, the remaining amplifiers in the CA3600E may be connected in parallel with the single stage shown.*

Fig. 36 shows a variety of circuits that can be assembled using the CA3080 to drive one "inverter"/amplifier in the CA3600E.. Precise timing and thresholds are assured by the stable characteristics of the input differential amplifier in the CA3080. Moreover, speed vs. power consumption tradeoffs may be made by adjustment of the $I_{ABC}$ current to the CA3080. The quiescent power consumption of the circuits shown in Fig. 36 is typically 6 mW, but can be made to operate in the micropower region by suitable circuit modifications.

### Micropower Comparator

The schematic diagram of a micropower comparator is shown in Fig. 37. Quiescent power consumption of this circuit is about 10 μW (typ). When the comparator is strobed "ON", the CA3080A becomes active and consumes 420 μW. Under these conditions, the circuit responds to a differential input signal in about 8 μsec. By suitably biasing the CA3080A, the circuit response time can be decreased to about 150 nsec., but the power consumption rises to 21 mW.

The differential amplifier input common-mode range for the circuit of Fig. 37 is -1V to +10.5 V. Voltage of the micropower comparator is typically 130 dB. For example, a 5 μV input signal will toggle the output.

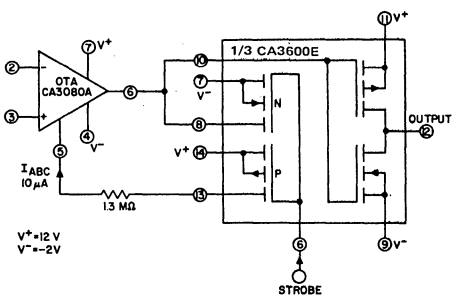



*Fig. 37– Schematic diagram of micropower comparator using the CA3080A and COS/MOS CA3600E.*

## APPENDIX I
## CURRENT MIRRORS

The basic current-mirror, described in the beginning of this note, in its rudimentary form, is a transistor with a second transistor connected as a diode. Fig. A shows this basic configuration of the current-mirror. Q2 is a diode connected transistor. Because this diode-connected transistor is not in saturation and is "active", the "diode" formed by this connection may be considered as a transistor with 100% feedback. Therefore, the base current still controls the collector current as is the case in normal transistor action, i.e., $I_C = \beta I_b$. If a current $I_1$ is forced into the diode-connected transistor, the base-to-emitter voltage will rise until equilibrium is reached and the total current being supplied is divided between the collector and base regions. Thus, a base-to-emitter voltage is established in Q2 such that Q2 "sinks" the applied current $I_1$.

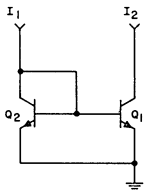



*Fig. A— Diode – transistor current source.*

If the base of a second transistor (Q1) is connected to the base-to-collector junction of Q2, shown in Fig. A, Q1 will also be able to "sink" a current approximately equal to that flowing in the collector lead of the diode-connected transistor Q2. This assumes that both transistors have identical characteristics, a prerequisite established by the IC fabrication technique. The difference in current between the input current ($I_1$) and the collector current ($I_2$) of transistor Q, is due to the fact that the base-current for both transistors is supplied from $I_1$. Fig. B shows this current division, using a unit of base current (1) to each transistor base. This base

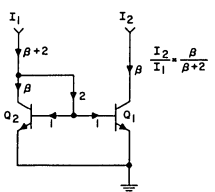



*Fig. B— Diode – transistor current source. Analysis of current flow.*

current causes a collector current to flow in direct proportion to the $\beta$ of each transistor. The ratio of the "sinking" current $I_2$ to the input current $I_1$ is therefore equal to $\frac{I_2}{I_1} = \beta/(\beta+2)$. Thus, as $\beta$ increases, the output "sinking" current ($I_2$) level approaches that of the input current ($I_1$). The curves in Fig. C show this ratio as a function of the transistor $\beta$. When the transistor $\beta$ is equal to 100, for example, the difference between the two currents is only two percent.

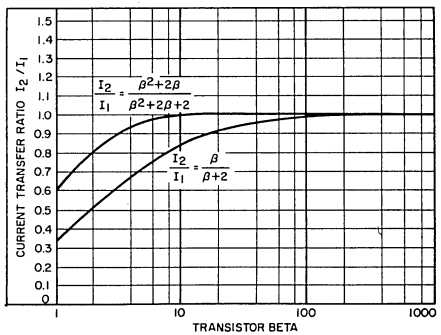



*Fig. C— Current transfer ratio $I_2/I_1$ as a function of transistor beta.*

Fig. D shows a curve-tracer photograph of characteristics for the circuit of Figs. A and B. No consideration in this discussion is given to the variation of the transistor (Q1) collector current as a function of its collector-to-emitter voltage. The output resistance characteristic of Q1 retains its similarity to that of a single transistor operating under similar conditions. An improvement in its output resistance characteristic can be made by the insertion of a diode-connected transistor in series with the emitter of Q1.

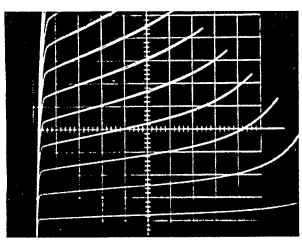



*Fig. D— Photo showing results of Figs. A & B.*

This diode-connected transistor (Q3 in Fig. E) may be considered as a current-sampling diode that senses the emitter-current of Q1 and adjusts the base current Q1 (via Q2) to maintain a constant-current in $I_2$. Because all controlling transistors are operated at relatively fixed voltages, the previously discussed effects due to voltage coefficients do not exist. The curve-tracer photograph of Fig. F shows the improved output resistance characteristics of the circuit of Fig. E. (Compare Fig. D and F).

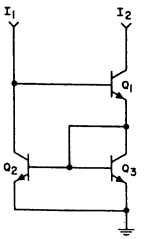



*Fig. E— Diode — 2 transistor current source.*

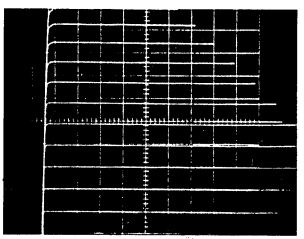



*Fig. F— Photo showing results of Fig. E.*

Fig. G shows the current-division within the "mirror" assuming a "unit" (1) of current in transistors (Q2 and Q3.

The resulting current-transfer ratio $I_2/I_1 = \frac{\beta^2 + 2\beta}{\beta^2 + 2\beta + 2}$. Fig. C shows this equation plotted as a function of beta. It is significant that the current transfer ratio ($I_2/I_1$) is improved by the $\beta^2$ term, and reduces the significance of the $2\beta + 2$ term in the denominator.

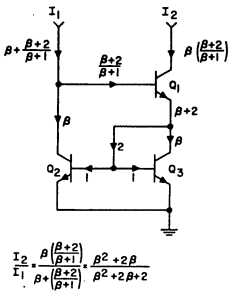



*Fig. G— Current flow analysis of Fig. E.*

## Conclusions

The Operational Transconductance Amplifier (OTA) is a unique device with characteristics particularly suited to applications in multiplexing, amplitude modulation, analog multiplications, gain control, switching circuitry, multivibrators, comparators, and a broad spectrum of micropower circuitry. The CA3080 is ideal for use in conjunction with COS/MOS (Complementary-Symmetry MOS) IC's being operated in the linear mode.

## Acknowledgements

The author is indebted to C. F. Wheatly for many helpful discussions. Valued contributions in circuit evaluation were made by A. J. Visioli Jr. and J. H. Klinger.

## References

1 RCA's Linear Integrated Circuits Manual, Basic Circuits Section.
2 RCA published data for CA3060 File No. 404

# A Flexible Integrated-Circuit Color Demodulator for Color Television

By W. M. Austin

New color-TV receiver designs indicate a rapidly changing trend toward all solid-state circuitry with special emphasis on monolithic integrated circuits. The solid-state color-demodulator circuits in these receivers provide excellent demodulation gain, linearity, and uniformity. These advantages are easily achieved by the integrated-circuit design of the balanced demodulator. At present, the integrated circuit is economically adaptable to the current design requirements of the color-picture-tube drive circuits. The choice between a color- difference (CD) or a red-green-blue (RGB) receiver system has changed in favor of the RGB which has additional design advantages. Because of improved phosphors and improved color picture tubes in general, color shifting has caused the establishment of a new reference for the demodulation parameters. Consideration of these references and of many other recent requirements have set the design guidelines for the RCA CA3067 demodulator integrated circuit.

The CA3067, which is supplied in a quad-in-line 16-lead plastic package, provides the following color-demodulator circuit functions:

(1) Amplification

(2) Blanced chroma demodulation*

(3) DC-operated tint (phase) control

(4) Zener-diode voltage regulation

This Note describes the circuit operation and application of the CA3067 in a color television receiver. Fig. 1 shows the CA3067 interconnected with other units in a complete receiver.

The CA3067 has a phase-shift circuit for tint control and a limiting amplifier for the elimination of amplitude modulation on the reference subcarrier.** In addition, it has preamplifier circuits which amplify the subcarrier signal before it is injected into the balanced demodulators. Because integral rf tilters remove the high-frequency products of demodulation, external filtering is unnecessary. The R-Y and B-Y color-difference signals are obtained by demodulation and the G-Y signal is derived from a matrix of the complementary R-Y and B-Y signals. The output amplifier for each of the color-difference signals has a very low output impedance for positive and negative signals and a sufficient drive capability for high-level voltage amplifiers for either a Red-Green-Blue (RGB) or a color-difference (CD) circuit. The operation of the CA3067 is described in the reverse signal-flow order to emphasize the output drive capability and requirements in direct-coupled circuit applications. Fig. 2(a) shows the CA3067 in a typical application.

### The Output Amplifiers of the CA3067

An outstanding feature of the CA3067 output amplifier circuit is the feedback emitter-follower arrangement which keeps the output impedance low during both the positive and negative peak signal swings of the output stage. This arrangement assures sufficient drive capability for the high-voltage output transistors of present color systems without degradation of bandwidth characteristics, particularly when signal amplitudes are at peak values. The largest output drive capability from the B-Y color-difference stage is a voltage drive in excess of 3.0 V peak-to-peak. This range of output drive will satisfy the design requirements of most RGB or color-difference systems.

As shown in Fig. 2(b), the B-Y amplifier, which is similar to the R-Y and G-Y color-difference output circuits, has a feedback path from the collector of the emitter-follower $Q_{30}$ to the base of $Q_{29}$. The zener diode, $Z_1$, has a voltage drop of

* "Chroma", defined here, means side bands of the modulated chrominance subcarrier.

** "Reference subcarrier", as used in this Note, means the same as "chrominance-carrier reference."

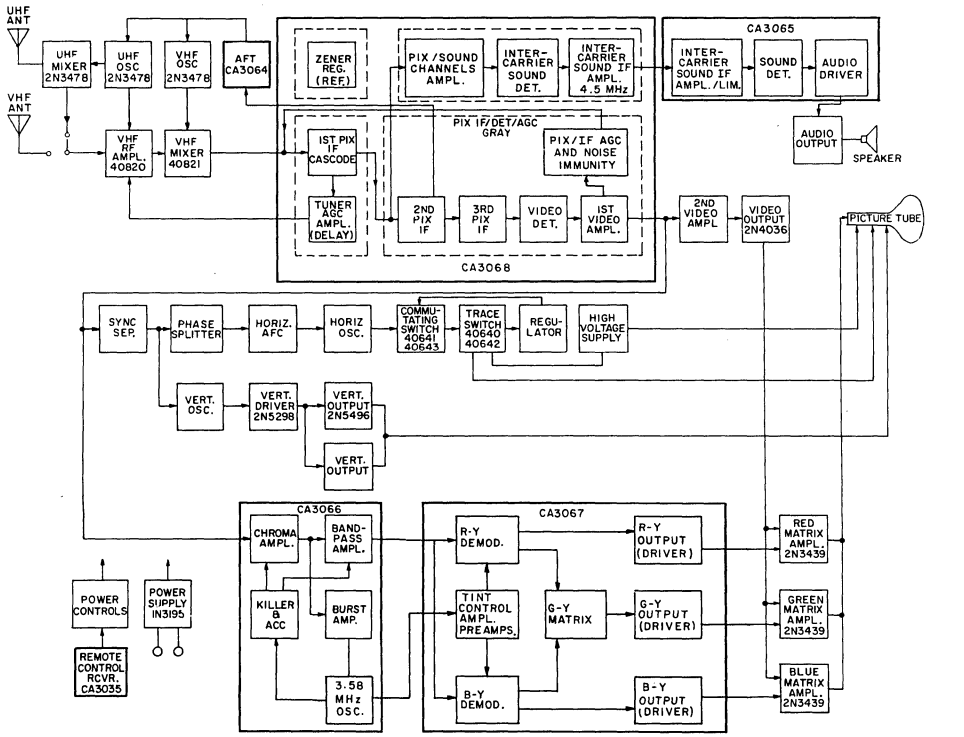



*Fig.1—Block diagram of a typical color-TV receiver utilizing the RCA CA3067.*

approximately 7 V (dc) and, with resistors $R_{46}$ and $R_{47}$, establishes a bias voltage of 0.7 V (dc) at the base of $Q_{29}$. Because $Z_1$, $R_{46}$, and $R_{47}$ are the feedback-loop components, they also establish the correction current that must flow in the collectors of $Q_{29}$ and $Q_{30}$ to provide the required voltage drop across $R_{50}$. The current in $Q_{29}$ and $Q_{30}$ is typically 1.5 mA; the current in the feedback loop is 0.5 mA. The loop gain is sufficient to keep the voltage errors small at the emitter-to-collector output junction (terminal No. 8). Within a normal range of circuit tolerances, $Q_{29}$ and $Q_{30}$ may have minimum values of collector-to-emitter current of approximately 1.1 mA. When external current loads are connected to terminal No. 8, no appreciable change in the voltage at this terminal occurs unless the maximum load current exceeds 1.1 mA.

When there is a high-current drain at terminal No. 8, the collector voltage of $Q_{30}$ decreases and the reduced bias to $Q_{29}$ may cut off $Q_{29}$. Consequently, excessive loading at terminal No. 8 can bias $Q_{29}$ and $Q_{30}$ out of their feedback range of operation. For this reason, loads that draw current in excess of 1.1 mA are not recommended.

### Demodulation and Matrix

The demodulator is a balanced type that provides both positive and negative color-difference output signals. The chroma signal of terminal No. 14 is applied to the chroma amplifier transistors $Q_{13}$, $Q_{14}$, $Q_{20}$, and $Q_{21}$ [Fig. 2(b)]. These chroma amplifiers provide the emitter drive to the demodulator-switching transistors $Q_{15}$, $Q_{16}$, $Q_{17}$, and $Q_{18}$ in the B-Y demodulator and $Q_{22}$, $Q_{23}$, $Q_{24}$, and $Q_{25}$ in the R-Y demodulator. Transistors $Q_{22}$ and $Q_{25}$ sum the positive output of the R-Y demodulator in resistors $R_{38}$ and $R_{39}$. The transistors $Q_{23}$ and $Q_{24}$ provide the negative output voltage of the R-Y demodulator across the load resistors $R_{37}$ and $R_{32}$.

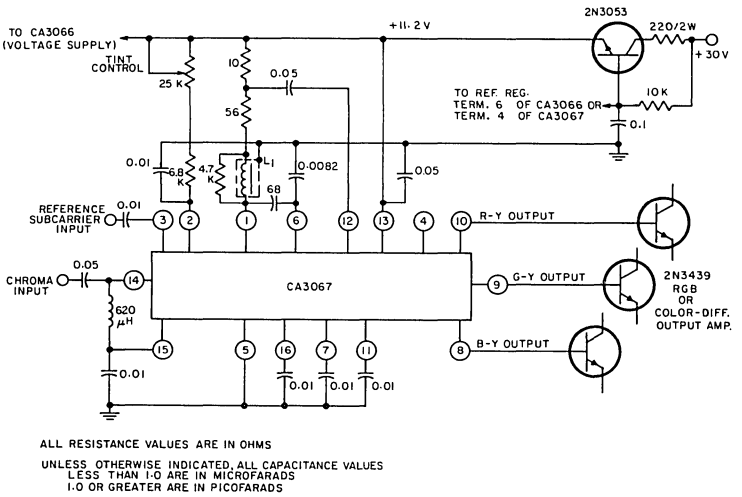



*Fig. 2(a)—RCA-CA3067 in a typical application.*

The positive output voltage of the B-Y demodulator provided by $Q_{16}$ and $Q_{17}$ is developed across the load resistor $R_{33}$, and the negative output voltage is the sum of the $Q_{15}$ and $Q_{18}$ outputs developed across resistor $R_{32}$. Thus, the addition of the negative outputs of the R-Y and B-Y demodulators provides the G-Y color difference signal. In this process, the negative outputs of the B-Y and R-Y demodulators are added in a ratio of 1.05:2.25, which are, respectively, the resistance values of $R_{32}$ and $R_{32} + R_{37}$. Fig. 3 shows the vector additions of the complementary R-Y and B-Y color-difference signals that yield the G-Y color-difference signal. The matrix circuit at the CA3067 demodulator stages establishes the ratio of R-Y to B-Y color-difference signals as 1.0:1.2. This value is the ratio of $R_{38} + R_{39}$ to $R_{33}$ resistance values, which are 6.7 and 8.2 kilohms, respectively.

An internal matrix circuit may, at first, appear to be disadvantageous. However, the ability to process uniform monolithic resistors on a single chip makes it desirable to matrix the R-Y and B-Y for the G-Y color-difference signal and to set a fixed ratio for all color-difference signals at the demodulator stages. The ratio of color-difference signal amplitudes at terminal Nos. 8, 9, 10 is easily modified by alteration of the gain- controlling circuit components that are either added to or used as a part of the high-level output stages.

The angle of demodulation is determined by the user's choice of reference-subcarrier phase applied to terminal Nos. 6 and 12. The signal input at terminal No. 6 relative to that of terminal No. 12 must be of opposite polarity to provide the same demodulation angle in each of the two demodulators. The CA3067 is presently being used in systems having demodulation angles separated by more than 90°. The reference-subcarrier signal at terminal No. 6 is displaced by 76° relative to the signal at terminal No. 12. This displacement produces a demodulation angle of 0° and (180° – 76°) or 104° in the B-Y and R-Y demodulator stages. This phase relationship relative to the color-difference signal amplitudes at terminal Nos. 8, 9, and 10 (which are respectively the B-Y, G-Y, and R-Y color-difference output terminals) is shown in the polar plot of Fig. 3.

Fig. 4 shows the typical demodulator voltage linearity and amplitudes at terminal Nos. 8, 9, and 10 for the circuit of Fig. 2(a). For a 76° phase difference of the voltage at terminal No. 6 relative to the voltage at terminal No. 12, (which is a 104° separation of the demodulation angles), the G-Y amplitude relative to the R-Y amplitude is 33 per cent. In a true quadrature demodulation, when the demodulation angles have 90° of phase separation, this ratio is 37/100.

### Polarity

The polarity of the color-difference output signals may be reversed by the choice of chroma drive signal to terminal Nos. 14 or 15 [Fig. 2(b)]. Both terminal Nos. 14 and 15 are accessible to permit selection of the polarity for either the grid or cathode drive to the picture tube or to minimize the cost of the phase-shift components. Terminal No. 14 is the preferred chroma-signal input terminal for an RGB system which drives the cathodes of the picture tube when the CA3066 chroma processor system is used. An rf coil or

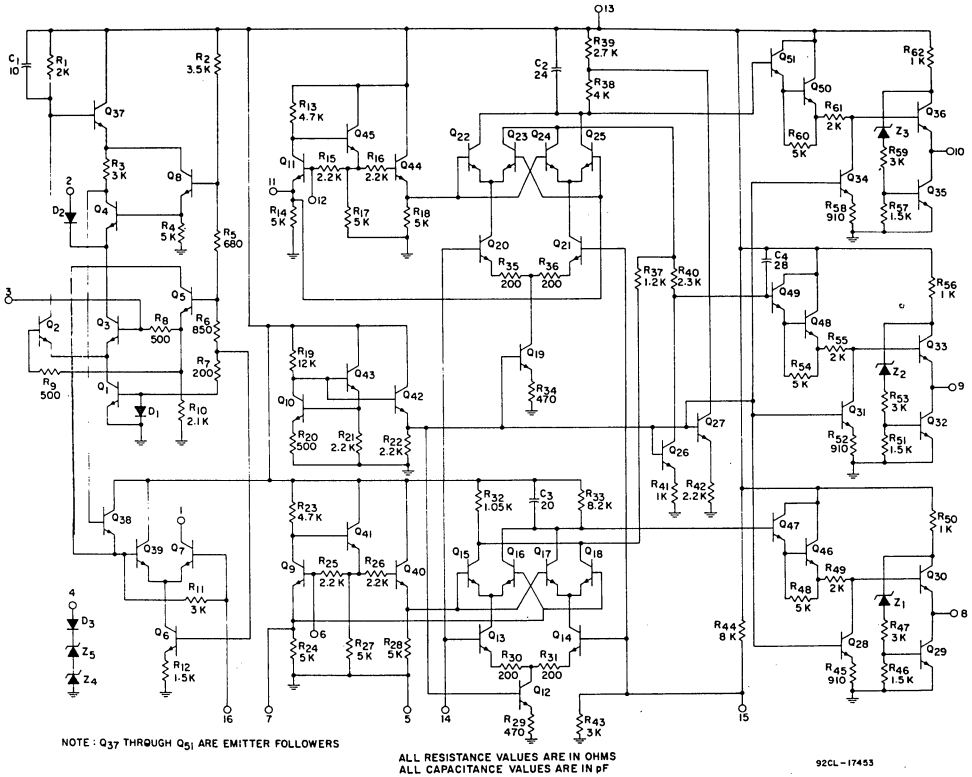



*Fig.2(b)—RCA-CA3067, schematic diagram.*

choke coupling is used between terminal Nos. 14 and 15. This coupling provides nearly equal bias to the chroma amplifiers $Q_{13}$, $Q_{14}$, $Q_{20}$, and $Q_{21}$. The balanced connections of the demodulators compensate for an unbalance in the external bias, if unbalance is not excessive. Resistors $R_{43}$ and $R_{44}$ may cause some signal loss when terminal No. 15 is the chroma-input terminal. The input impedance, however, is approximately 10 times greater than the output impedance of the chroma amplifier of the CA3066.

### Filtering Capacitors

Capacitors $C_2$, $C_3$, and $C_4$ serve as ripple filters to reduce the 3.58-MHz and higher harmonic components of demodulation. The tolerance of the RC time constant is set for a minimum bandwidth of 450 kHz. Even without precise control over the RC time constant, there are three important advantages for the use of monolithic capacitor filtering at the output of the demodulator stages. First, ripple filtering before the output amplifiers extends the linear dynamic-voltage-swing capability of the output stages of the CA3067. Second, a savings in cost is realized because no added external ripple filter components are required. Third, the performance of the RGB high-level amplifier system is improved by the very low drive impedance from the output of the CA3067. This low output impedance is not degraded because no external filtering components are needed.

### Demodulator Preamplifier

The R-Y and B-Y demodulators are driven by their respective subcarrier preamplifiers, which are transistors $Q_{11}$, $Q_{44}$, $Q_{45}$, and $Q_9$, $Q_{40}$, $Q_{41}$ [Fig. 2(b)]. Although the preferred signal-drive voltage level is approximately 2.5 mV (rms), as little as 1.0 mV (rms) of signal at terminal Nos. 6 and 12 provides efficient demodulator conversion gain. Curves of the demodulation sensitivity as a function of signal levels at terminal No. 12 are shown in Fig. 5. These curves are determined from the circuit shown in Fig. 2(a). The drive voltage is applied to terminal No. 3 of the tint-control amplifier.

Each subcarrier preamplifier has a voltage gain of 100 when operated as a common-emitter amplifier having termi-

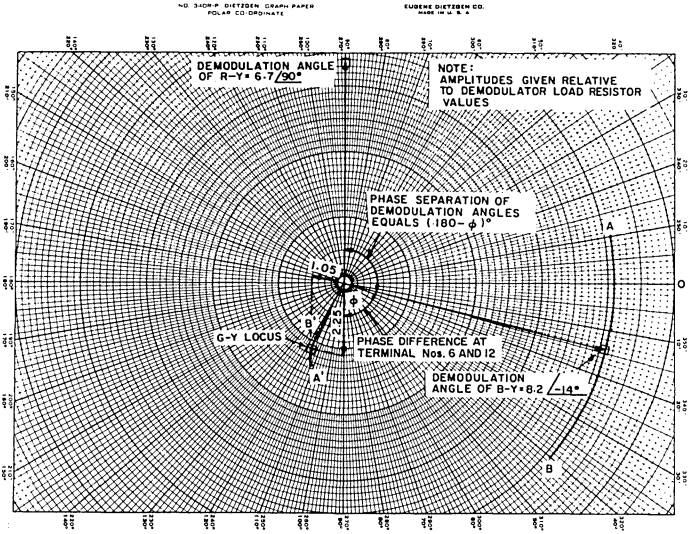



*Fig.3—Vector plot of color-difference signals.*

nal Nos. 7 and 11 bypassed for rf. Because of the collector-to-base feedback, each subcarrier preamplifier has a low input impedance which is a function of the amplifier gain. Terminal Nos. 6 and 12 have drive requirements of a few millivolts; there are no disadvantages associated with input attenuation caused by the low input impedance. Phase shift of the injected subcarrier caused by stray capacitance coupling is minimized.

### Tint Control Amplifier

The tint-control section of the CA3067 contains the phase-shift and limiting-amplifier circuits that control the reference subcarrier signal (3.58-MHz). This signal is received from the CA3066 oscillator circuit and is adjusted to a nominally correct phase reference for the CA3067 tint-control system. The phase errors caused by transmission, circuit tolerance, and oscillator drift are corrected by the tint control. The tint control in the CA3067 circuit is a potentiometer which controls the direct current flowing into terminal No. 2. The 3.58-MHz signal is ac-coupled to the

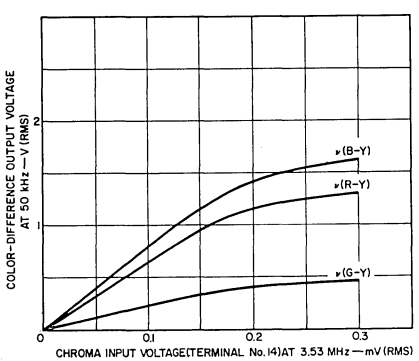



*Fig.4—Demodulation linearity.*

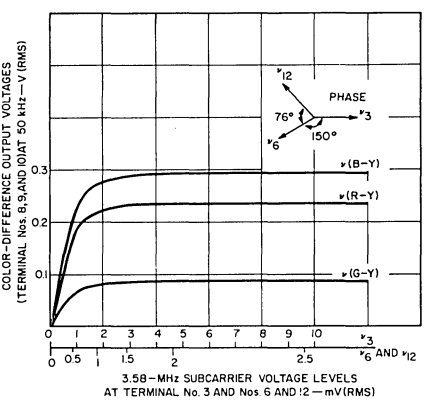



*Fig.5—Demodulation sensitivity as a function of subcarrier signal level at terminal No. 3 and terminal Nos. 6 and 12.*

tint-control amplifier input terminal No. 3. The amplitude-limited output signal is available at the collector of $Q_7$, terminal No. 1 [Fig. 2(b)].

The 3.58-MHz signal is differentially amplified following its injection into the base of $Q_3$, which is common to terminal No. 3. The differential amplifier consisting of $Q_2$ and $Q_3$ amplifies and divides the reference-subcarrier signal into two out-of-phase components. The current into the collector of $Q_2$ is in phase with the base current of $Q_3$; the current into the collector of $Q_3$ is out of phase with the base current of $Q_3$. Resistor $R_1$ in parallel with the cumulative circuit stray capacitance and the capacitance of $C_1$ form an RC time constant which causes a phase delay of approximately 45° at the collector of $Q_2$. Thus, the two components of the reference-subcarrier signal current are the "delayed phase" at the collector of $Q_2$ and the "reverse-phase" at the collector of $Q_3$. The "reverse-phase" signal current is divided between the diode $D_2$ and the emitter of $Q_4$ at the collector of $Q_3$; the amount of this division depends on the position of the tint-control adjustment. The divided current that passes through diode $D_2$ is bypassed to ground at terminal No. 2. The "delayed-phase" signal current at the collector of $Q_2$ is amplified in $Q_{37}$ (an emitter-follower) and added to the "reverse-phase" signal which is present at the collector of $Q_4$. Because the current flow in the collector of $Q_3$ is typically 1.0 mA, the resistance range of the tint control shown in Fig. 2(a) is adequate for the full range of adjustment desired.

The vector addition of the "delayed-phase" and "reverse-phase" signals provides a controlled phase shift that is typically 105°. Fig. 6 shows the phase diagram for the minimum and maximum settings of the tint control. Vector B, in Fig. 6, is the maximum "reverse-phase" signal amplitude that may be obtained at the collector of $Q_4$ [Fig. 2(b)] and vector A is the "delayed-phase" signal amplitude. The relative voltage amplitude of each phase-separated signal is proportional to the load impedances at the collectors of $Q_2$ and $Q_4$. The "reverse-phase" signal amplitude is approximately two times greater than that of the "delayed phase". A minimum adjustment of the tint control will decrease the "reverse phase" signal at the collector of $Q_4$ to approximately zero amplitude. The resultant vector is determined from the addition of the "delayed–phase" and "reverse-phase" signals at the collector of $Q_4$ and may be any vector between vectors A and C shown in Fig. 6.

The resulting signal for any setting of the tint-control adjustment is amplified in the limiter-amplifier circuit consisting of $Q_{37}$, $Q_{38}$, and $Q_{39}$ [Fig. 2(b)]. There is no further phase shift in the limiter-amplifier, which serves to limit any amplitude modulation of the reference-subcarrier signal, including the amplitude variations caused by the tint-control adjustment. The complete tint-control amplifier circuit limits the output signal at terminal No. 1 when the input signal amplitude at terminal No. 3 is greater than 7.0 mV (rms). Characteristic curves of the limiting of the CA3067 tint-control amplifier are shown in Fig. 7. In addition, curves of phase as a function of frequency are shown in Fig. 8.

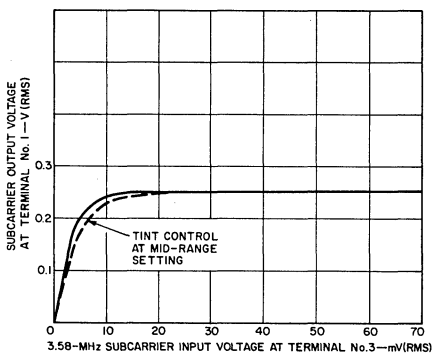



*Fig.7—Limiting-characteristic curve for tint-control amplifier.*

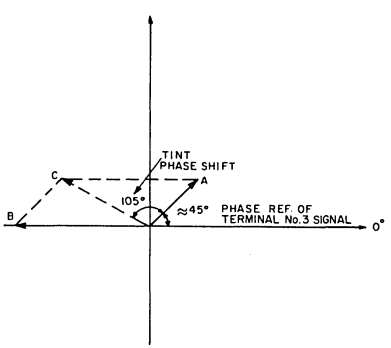



*Fig.6—Vector addition of tint-control amplifier.*

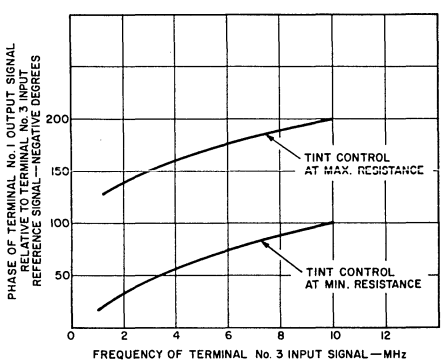



*Fig.8—Typical phase characteristic of the tint-control amplifier as a function of frequency.*

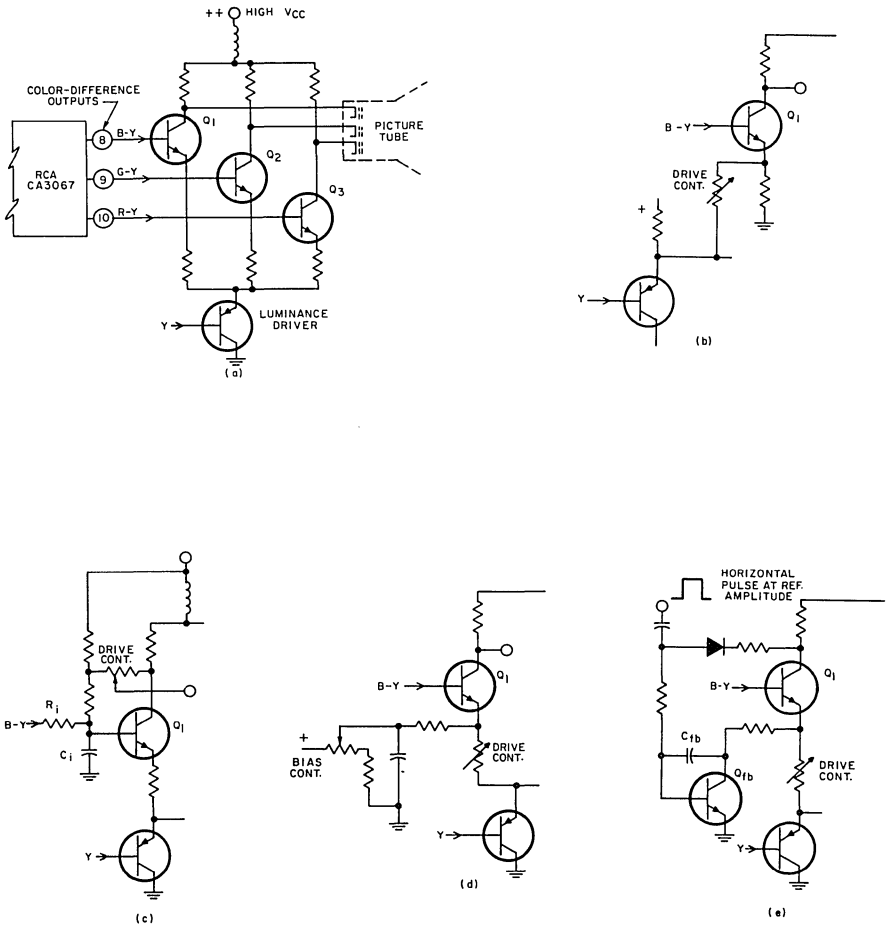



*Fig.9—Use of RCA-CA3067 in RGB system of color drive to the picture tube: (a) basic systems; (b) emitter-drive control; (c) collector-feedback drive control; (d) emitter drive and bias controls; (e) automatic bias and drive control in the RCA CTC46 and CTC49 color-TV receivers.*

The circuit of Fig. 2(a) shows one possible method of providing phase separation of signals to the R-Y and B-Y subcarrier amplifier. The tint-control amplifier output signal, which is the processed reference subcarrier, is separated in an RLC signal-tuned circuit that provides a phase separation of 76° at terminal Nos. 6 and 12. This circuit is considered a preferred matching network because it relates to the published data characterization. However, it is an arbitrary choice which yields the desired amplitude and phase separation to match the tint-control amplifier to the R-Y and B-Y subcarrier amplifiers. Fixed-tuned RC or delay-line circuits may also be considered as possible matching networks to meet the application needs in other systems which include monitoring equipment and test instruments.

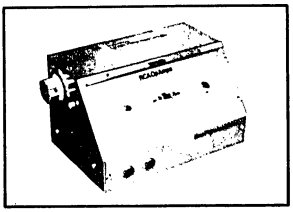
#### CA3067 Application in RGB Color System

The basic connections for an RGB system are shown in Fig. 9(a). The CA3067 output amplifiers are direct-coupled to the RGB output amplifier circuits. Regardless of the direct-coupled bias considerations, it is always necessary to provide drive control to obtain proper gray-scale tracking. This control is accomplished by the adjustment of the relative gains of the RGB amplifiers. Usually the emitter or collector resistors are varied for gain-control adjustment. The emitter-resistor adjustment provides feedback gain control, and the collector-resistor adjustment is used for either attenuation or feedback control. Four different drive control methods are shown in Figs. 9(b) through 9(e).

When a design-center drive condition is established, the circuit of Fig. 9(b) is correct for center-value components. The dc shift at the limit adjustments of the drive control resulting from component tolerance require other supplementary adjustments such as a grid-to-cathode voltage adjustment at the picture tube. Fig. 9(c) shows a circuit that uses voltage feedback to stabilize the bias. Because an isolation resistance $R_i$ must be added at the base of $Q_1$ to develop feedback voltage at that point, a capacitor $C_i$ may be added to peak the luminance signal response. This capacitor is not needed to filter the 3.58-MHz signal and higher harmonics of demodulation; the CA3067 has internal filtering for this purpose.

The two circuits shown in Figs. 9(d) and 9(e) illustrate a more precise method of adjustment. The circuit of Fig. 9(d) has a dc-bias control which can be adjusted to compensate for any dc change caused by the drive control. The disadvantages of this circuit are the added bias control and the adjustment interaction of the drive and bias controls. The circuit of Fig. 9(e), which is presently used in the RCA CTC-46 and CTC-49 color-TV receivers, illustrates an emitter-type drive-control adjustment and an automatic bias-control circuit which compensates for both short-and long-term drift of the output circuit. The automatic bias-control circuit samples the voltage level at the output of the RGB amplifier during the horizontal retrace period. This voltage is compared with a fixed reference, and an error signal is fed back to the emitter of $Q_1$. The collector of transistor $Q_{fb}$ acts as a voltage source with the correct line-by-line value of voltage to stablize the RGB output amplifier. The feedback error from the sampling circuit is returned to the base of $Q_{fb}$, and provides the correction for any temperature drift as well as for the voltage error caused by the drive-control adjustment.

The design of an RGB amplifier circuit to be driven from the CA3067 depends on the economics and the performance requirements of the application. Because the CA3067 output amplifiers have a very low source impedance, networks that add to the source impedance at the CA3067 output terminals detract from the inherent advantage of the use of the CA3067. An obvious performance advantage of the circuit of Fig. 9(e) is that the added cost of the feedback and the sampling components is offset by the performance gains of a self-adjusting system. Also, rigid specifications related to thermal tracking such as leakage currents and heat sinking may be relaxed. When modular construction and trouble-free interchangeability are primary design considerations, both cost and performance advantages are realized by the use of the CA3067.



# Measurement of Burst ("Popcorn") Noise in Linear Integrated Circuits

by T. J. Robe

The advent in recent years of very high-gain operational amplifiers operating in the l/f noise-frequency spectrum has placed emphasis on the need for very low-noise devices. This need is particularly true for operational amplifiers which have either low-offset characteristics and/or offset-null capability.

The traditional methods used to select such devices involve the measurement of either spot or wideband (≈ 10 kHz) noise figures in the l/f frequency range (10 Hz to 10 kHz) at various source resistances. This type of measurement, however, only provides an indication of the average noise power at the measurement frequency and does not reveal the burst ("popcorn") noise characteristics of the Device Under Test (DUT). The metering circuits cannot respond fast enough to measure the effects of burst-noise. Fig. 1a shows a photograph of typical burst-noise as a function of time for an operational amplifier having poor burst-noise characteristics. This photo illustrates burst-noise which is characterized by random abrupt output voltage-level changes that persist for periods from approximately 1/2 millisecond to several seconds. Additionally, the random rate at which the bursts occur ranges from approximately several hundred per second to less than one per minute. Furthermore, these rates are not necessarily repetitive and predictable. Consequently, the nature of burst-noise prevents its measurement by means of the standard averaging techniques. Instead, a technique to detect individual bursts must be used and a DUT must be under observation for a period in the order of 10 seconds to one minute. Fig. 1b shows a photo of the output of a virtually burst noise-free operational amplifier, the RCA-CA6741T.

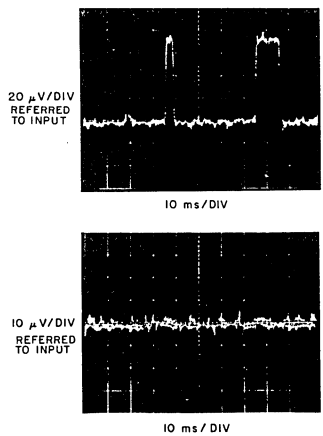



*Fig. 1— (a) Photo of output waveforms for amplifier with poor burst-noise characteristics; (b) photo of output waveform for the RCA-CA6741T.*

### Test Configuration

Some of the major questions relevant to the type of test required are:

1. What characteristics of the burst-noise should be detected?
2. What test-circuit configuration is most suitable to detect these characteristics?
3. What are the "Pass-Fail" criteria?

There are three major characteristics of the noise burst which have an impact on the suitability of a device from the standpoint of applications: burst amplitude, duration, and rate of occurrence. Of these, burst-amplitude and rate of occurrence are of primary interest to potential users of a particular device. Long duration bursts (of sufficient amplitude) seriously degrade the performance of dc amplifiers; however, suitable devices could be selected by the rejection of any unit which produced even one burst during some prescribed test period. Therefore, an absolute measurement of burst duration is not a prime necessity.

The rate of occurrence, on the other hand, as measured by the burst-count in a given test period could conceivably

be considered as a variable of prime importance in the selection process. For instance, a burst-rate of 100 per second is clearly objectionable in almost any low-level low-frequency application, whereas the occurrence of only one low-amplitude burst in a one-minute period might be quite acceptable. Consequently, it is desirable to include flexibility in the testing system so that "Pass-Fail" criteria can be established on the basis of burst-noise count in some prescribed period of time. The test equipment described herein detects total noise (1/f noise plus burst noise) bursts with amplitudes above a preset threshold level during a given test period and allows acceptance or rejection on the basis of the number of noise voltage excursions beyond the threshold level, in the selected test period.

Another factor to be considered is the bandwidth of the test system. Excessive bandwidth allows the normal "white" noise of the terminating resistors and the DUT to obscure burst-noise occurrences and does not realistically simulate the low-frequency applications in which burst-noise is particularly objectionable. On the other hand, a test circuit having excessively narrow bandwidth prevents detection of the shorter-duration bursts ($\approx$ 1/2 ms) even if their amplitude is relatively high. A suitable compromise is chosen in which the system rise time permits a burst of "minimum" duration to reach essentially its full amplitude. Because the rise time and bandwidth of an amplifier are related by the equation:

$$BW \approx \frac{0.4}{t_r}$$

the minimum bandwidth to detect a 0.5 ms burst is approximately:

$$BW_{min} = \frac{0.4}{(0.5)\,(10^{-3})} = 0.8 \text{ kHz}.$$

Consequently, a 1 kHz bandwidth has been selected as a reasonable one for a burst-noise test system and, therefore, prescribes the need for a low-pass filter in the system.

The test requirements outlined above can be implemented with the following circuit elements shown in the block diagram of Fig. 2a. Fig. 2b shows the complete system schematic:

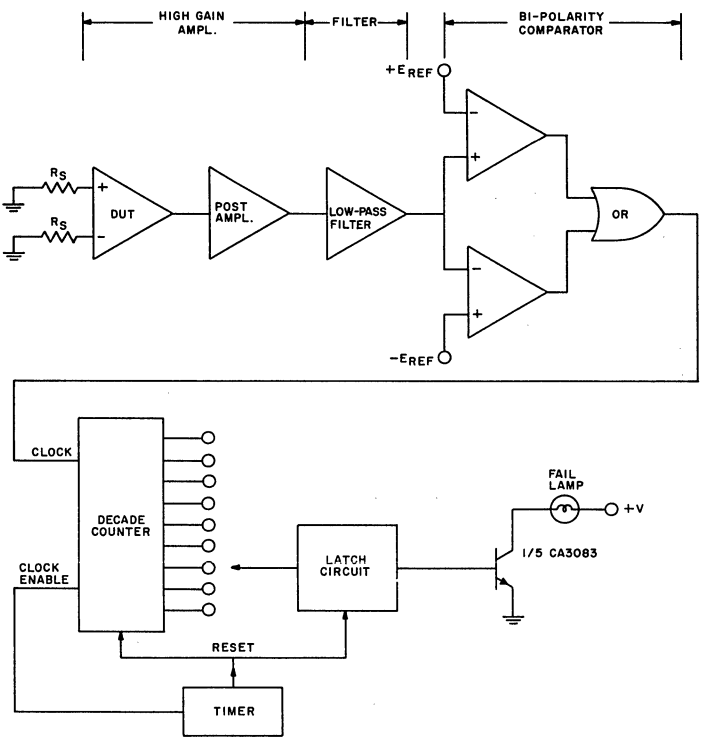



*Fig. 2a— Block diagram of burst-noise test set-up.*

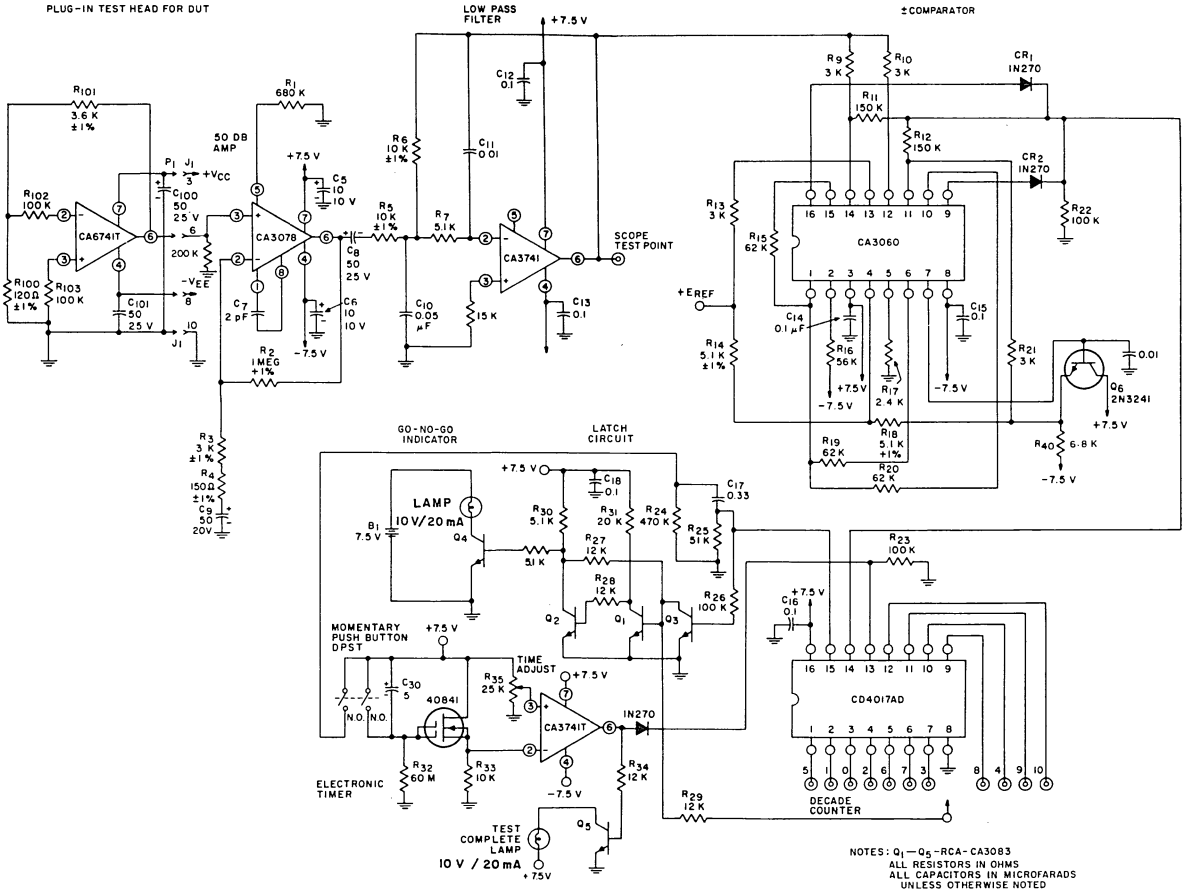



*Fig. 2b— Complete schematic diagram for burst noise test-set.*

1. A fixed high-gain amplifier incorporating the DUT as the first stage to amplify the microvolt-level burst to an easily detectable level (this should be a burst noise-free unit);
2. A low-pass filter to limit the test bandwidth to approximately 1 kHz,
3. A comparator to produce a fast-rise high-level single-polarity output pulse whenever an input burst-noise pulse (of either polarity) exceeds a preset (but adjustable) threshold level;
4. A counter to tally the number of pulses emanating from the comparator during the test period: a single decade counter is adequate.
5. A latch circuit which trips to the "latched" state when the count exceeds a preselected number (e.g. 1 to n). The latch circuit, if tripped, energizes an indicator lamp.
6. A timer to control the period over which the counter is enabled. It should incorporate the capability to reset both the counter and the latch circuit at the beginning of each test period.
7. Power supplies for the DUT and other auxiliary circuits.

**Test Conditions**

Some of the conditions which affect the burst-noise performance of the DUT include bias-level, source resistance (Rs), and ambient temperature ($T_A$).

The quiescent operating conditions in operational amplifiers are normally set by the magnitude of the positive and negative supplies. Many of the newer Op-Amp types, however, have bias-terminals into which fixed currents can be injected to set their performance characteristics. The RCA-CA3060, CA3080, and CA3080A Operational Transconductance Amplifiers (OTA's) and; the RCA-CA3078 and CA3078A Micropower Op-Amps are examples of such devices. For best low-frequency and burst-noise performance, these amplifiers should be operated at the lowest bias currents consistent with the gain-bandwidth requirements of the particular application.

In the test for burst noise, the source resistance (Rs) seen by the input terminals of the DUT, is a key test parameter. Burst noise causes effects which are equivalent to a spurious current-source at the device input and, therefore, burst-noise current generates an equivalent input noise-voltage in proportion to the magnitude of the source resistance through which it flows. Accordingly, to increase the sensitivity of the test system, it is desirable to use the highest source resistance consistent with the input offset-current of the DUT. For example, an Op-Amp which has 0.1 $\mu$A input offset current could realistically be tested with source-resistance in the order of 100K$\Omega$ (10 mV input offset), whereas a 1 M$\Omega$ source-resistance (100 mV input offset) could cause excessive offset in the output. For 741 type Op-Amps a 100k$\Omega$ resistance is recommended.

Burst-noise generation in amplifiers is usually more pronounced at lower temperatures (particularly below 0°C). Consequently, consideration must be given to the temperature of the DUT in relation to the temperature range under which the device is expected to perform in a particular operation.

A test parameter of importance is the time duration of observation. Because the frequency of burst-noise occurrence is frequently less than once every few seconds, the minimum test period should be in the range of from 15 to 30 seconds.

**Pass-Fail Criteria**

A test system built to accommodate the test philosophy outlined above has the ability to reject or pass a DUT on the basis of two variables: burst-amplitude and the frequency of burst occurrence. The burst-amplitude which will trip the counter can be no lower than the background l/f noise peaks of burst-free units, otherwise normal background noise will fail the DUT.

The background noise peaks depend on the source termination Rs, the wide band l/f noise figure of the DUT, and the test system bandwidth. A good estimate of the normal background noise-peak levels can be computed from the definition of noise factor and an empirically determined noise-crest factor of approximately 6:1. The crest-factor is the ratio of the maximum peak-noise voltage to the RMS noise voltage. The noise factor is defined as the ratio of the total noise power at the amplifier output to the output-noise power due to the source resistors alone. In terms of the RMS noise voltages at the input terminals of the amplifier this is equivalent to:

$$\text{Noise Factor (F)} = \frac{E^2\text{input noise total}}{E^2\text{noise source resist}} = \frac{(E_{NTi})^2}{(E_{NRS})^2} \quad (1)$$

$E_{NTi}$ is the total input noise-voltage, i.e., the sum of noise generated in the source termination resistance and noise generated by the DUT.

$E_{NRs}$ is that part of $E_{NTi}$ due to Rs alone.

$$\text{Therefore,} \quad E_{NTi} = (\sqrt{F})\,(E_{NRs}). \quad (2)$$

$E_{NRs}$ can be computed by using the well known expression for "white-noise" generated across the terminals of a resistor (R):

$$E_{NR}(RMS) = \sqrt{4kTBR} \quad (3)$$

where k = Boltzmans Constant = $1.372 \times 10^{-23}$ j/°K

T = Absolute Temperature in °K
B = Noise Bandwidth in Hz
R = Value of the resistor in ohms.

Thus, at a room temperature of 290°K

$$E_{NR}(RMS) = 1.28 \times 10^{-10} \sqrt{BR}$$

For example, a 100 kΩ resistor preceding a system with a bandwidth of 1 kHz will generate a noise-voltage of

$$(1.28 \times 10^{-10}) \quad (\sqrt{10^3 \cdot 10^5}) \quad = 1.28\ \mu V_{RMS}$$

Both inputs of an Op-Amp are usually terminated in Rs, hence it is necessary to combine the effects of both resistors to determine the effective $E_{NRs}$ at the input of the DUT. Because the noise voltages from these two resistors are uncorrelated their voltages must be added vectorally rather than algebraically.

$$E_{NRs}\ (\text{effective}) = \sqrt{(E_{NRs1})^2 + (E_{NRs2})^2} \qquad (4)$$

because $E_{NRs1} = E_{NRs2}$, when $R_{s1} = R_{s2}$

$$E_{NRs}\ (\text{effective} = (\sqrt{2})\ (E_{NRs})$$

and for 1 kHz bandwidth at 290°K

$$E_{NRs}\ (\text{effective}) = (\sqrt{2})\ (1.28\ \mu V) = 1.81\ \mu V_{RMS}.$$

If in this example, the DUT has a wideband 1/f noise figure of 4 dB (2.5:1 power ratio) the total RMS background noise-voltage at the input will be

$$E_{NTi} = (\sqrt{F})\ (E_{NRs})\ \text{(from eq.(2))}$$
$$= (\sqrt{2.5})\ (1.81) = 2.9\ \mu V_{RMS}$$

If a crest factor of 6:1 is assumed, the peaks of the background noise will be approximately (6) (2.9) = 17 μV peak. This voltage is the lower limit of the burst-amplitude rejection level. A reasonable threshold for burst detection and rejection might be 50-100% greater than this minimum value.

An alternate method used to set the burst-threshold limit involves a direct measurement (at the output of the high gain amplifier-filter combination) using a storage oscilloscope or a "true RMS" voltmeter. By this method the noise peak or RMS noise voltage of burst-free units is determined. This measurement provides a good practical check on the accuracy of the computation outlined above. Selection of the acceptable number of burst counts in the test period is arbitrary, but dependent on the type of application intended for the DUT. To be acceptable in some critical applications, the DUT may not generate even a single burst-pulse in a relatively long period of time.

### Burst-Noise Test System Circuits

#### 1. High gain Amplifier – Filter

Fig. 3 shows the schematic diagram of the high-gain amplifier-filter which provides a fixed gain of 80 dB with a 12 dB octave roll-off above 1 kHz. The gain-function is somewhat arbitrarily distributed between the DUT and

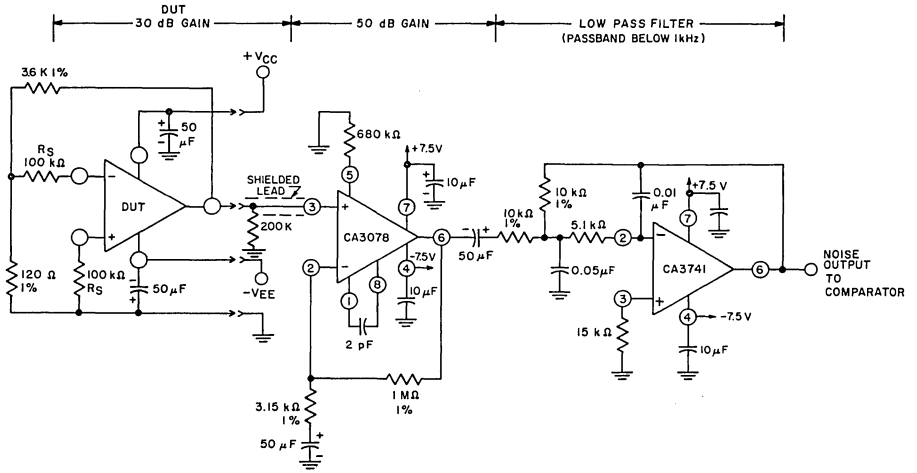



*Fig. 3— Schematic diagram of high-gain amplifier/filter.*

post-amplifier: 30 dB and 50 dB respectively. This distribution is based on the need for sufficient gain in the DUT portion to eliminate significant noise-signal contributions from the second stage while simultaneously allowing adequate loop-gain in each stage to provide accurate gain-setting with precise external resistors. The first stage is shown as a plug-in module so that any type of DUT configuration having 30 dB gain can be tested.

The capacitive coupling employed provides a low frequency cutoff of about 1 Hz and eliminates the need for dc-offset zero-adjustments. The dc offset-voltage at the filter output is less than 5 mV which corresponds to less than 0.5 $\mu$V error when referred to the noise input (an 80 dB gain is assumed.) Several seconds must be allowed, however, for the DC operating point to stabilize after the power is applied to the DUT.

### 2. Bi-Polarity Comparator

Fig. 4 shows the schematic diagram for the threshold-detecting comparator. Because bursts of either polarity must be detected and converted to positive output pulses, two comparators are required: one having a positive-threshold reference and the other having a negative-threshold reference of equal magnitude. The RCA CA3060 triple OTA is convenient to use because a single package provides circuits for both comparators plus a reference inverter for the negative threshold reference. The positive feedback provided by the $R_f$ and $R_i$ connections produces a hysteresis effect with reference to the input switching threshold, (i.e., the comparator does not return to its quiescent state until the input noise signal drops well below the initial threshold trip-level). This feature is necessary to prevent multiple triggering by the background noise signals superimposed on top of the burst-noise pulse. By this means, multiple counting of a single burst-noise pulse is avoided.

The magnitude of the threshold reference voltage $E_R$ determines the burst-level which trips the comparator. If a voltage gain of 80 dB is provided by the amplifiers, a 200 mV reference voltage will enable the circuit to be triggered when a burst-noise pulse (whose amplitude is equivalent to the level of 20 $\mu$V referred to the DUT input) is present.

### 3. Counter-Latch-Timer Control Circuits

The remaining circuits of the go-no-go burst-noise tester are shown in Fig. 5. The decade-counter is incorporated in a single COS/MOS IC (RCA CD4017AE) which has clock, reset, and enable inputs, and an output terminal for each of ten count-positions (0 to 9). A carry-out signal is available if the use of more than a single decade is desired. The clock input-signal must be positive-going and have a magnitude of

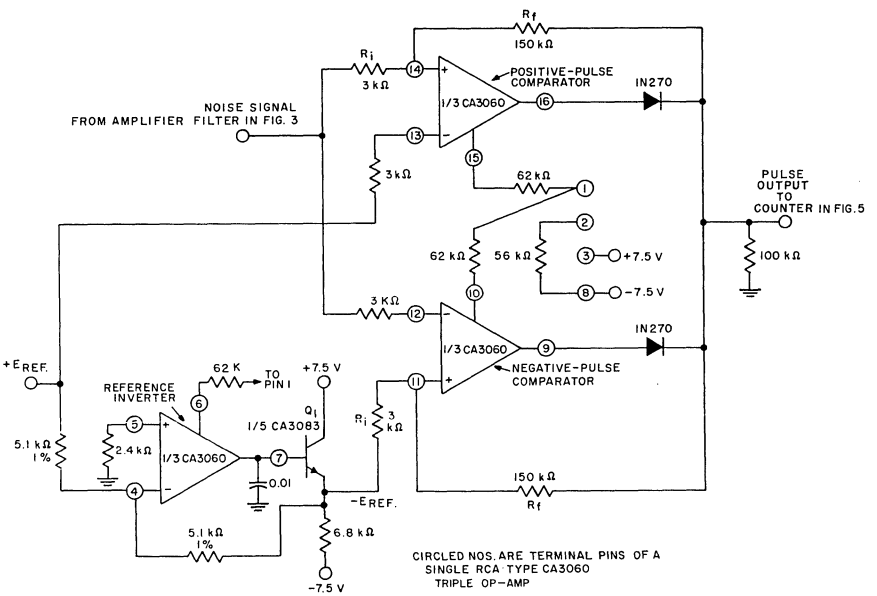



*Fig. 4— Schematic diagram of threshold-detecting comparator.*

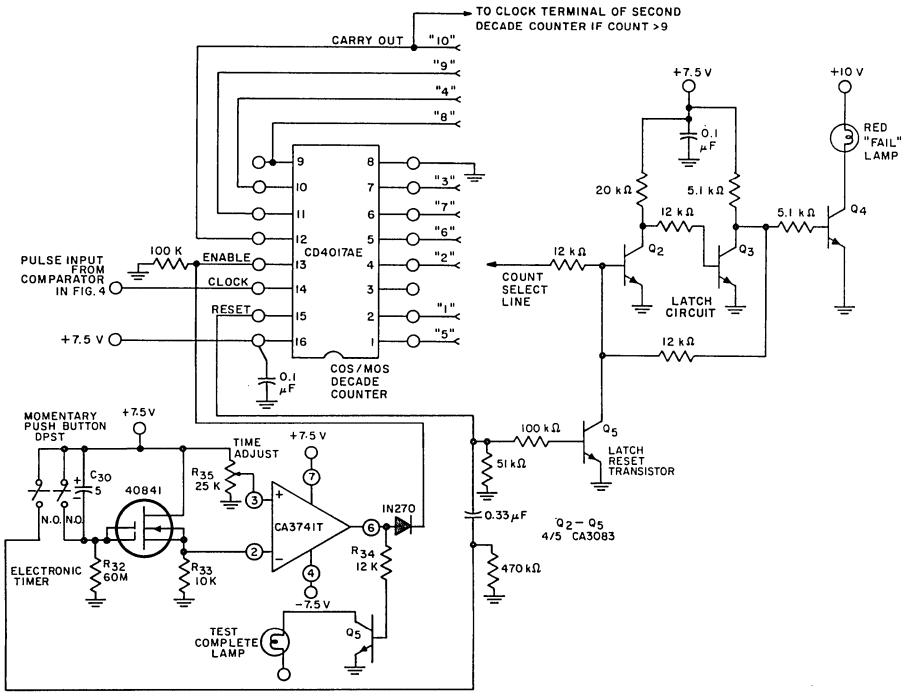



*Fig. 5— Counter-latch-timer-control circuit schematic.*

at least 70% of the supply-voltage and rise-time equal to or less than 15 μs. The comparator shown in Fig. 4 provides an output signal which meets these requirements.

Selection of the reject count is made by a pin-jack connection of the latch-circuit input-lead to the appropriate output terminal of the counter. Whenever the selected count-position voltage goes "high" the latch-circuit is switched to the latched-state, and the fail-indicator lamp "on". The latch and lamp will remain "on" until the reset button of the electronic timer is switched to the "Timer On" position. This action provides a momentary reset signal (≈ 20 ms) to both the latch and counter circuits and places a continuous enable voltage on the counter for the duration of the test period.

### Spurious Noise Sources and Their Suppression

The very low voltage levels and the high source impedances normally used for burst testing render the system highly susceptable to external spurious noise sources. This problem is particularly serious if a test unit is going to be rejected for as little as one or two input burst-noise pulses exceeding 20-30 μV. The major sources of spurious noise encountered in the development of this test system were:

1. 60-Hz hum pickup,
2. power supply transients,
3. electromagnetic pick up of switching transients.

60-Hz hum is introduced by capacitive or inductive coupling or as power-supply ripple. Power-supply ripple is not normally a problem when testing operational amplifiers with regulated supplies, because the Op Amps generally have good power-supply rejection. This source of noise must be considered, however, when testing devices that do not have good inherent power-supply rejection. Capacitive or inductive coupling of hum can occur when 60-Hz line cord leads are within a few inches of the input terminals of the DUT. Precautions, such as proper lead dress and twisting of the 60-Hz leads, eliminate this problem.

Power-supply transients, as distinguished from power-supply ripple, can be of sufficient amplitude to introduce detectable noise pulses at the operational amplifier input. Such transients are produced when other equipment on the same ac line is switched on or off. A typical power-supply rejection ratio for an operational amplifier is 50 μV/V (i.e. a 1 volt transient on the power-supply is equivalent to a 50 μV noise pulse at the DUT input). This example demonstrates that the test system cannot tolerate power-supply transients greater than approximately 100 mV even when testing units with good power-supply rejection. Unless the power-supply is

known to be free of such transients, a battery-operated system is recommended. Even when this system is battery-operated, "On-Off" switching of nearby equipment introduces detectable transients into the system. These problems are eliminated by placing the test circuitry in a completely shielded enclosure with a hinged top for easy access to the test unit. The external noise problem is best solved by use of a shielded enclosure and by use of a battery-operated power-supply contained within the enclosure. Fig. 6 shows a photo of the circuit board layouts of the test unit.

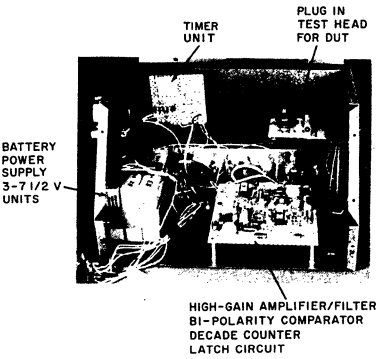



*Fig. 6— Photo of circuit-board layout.*

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