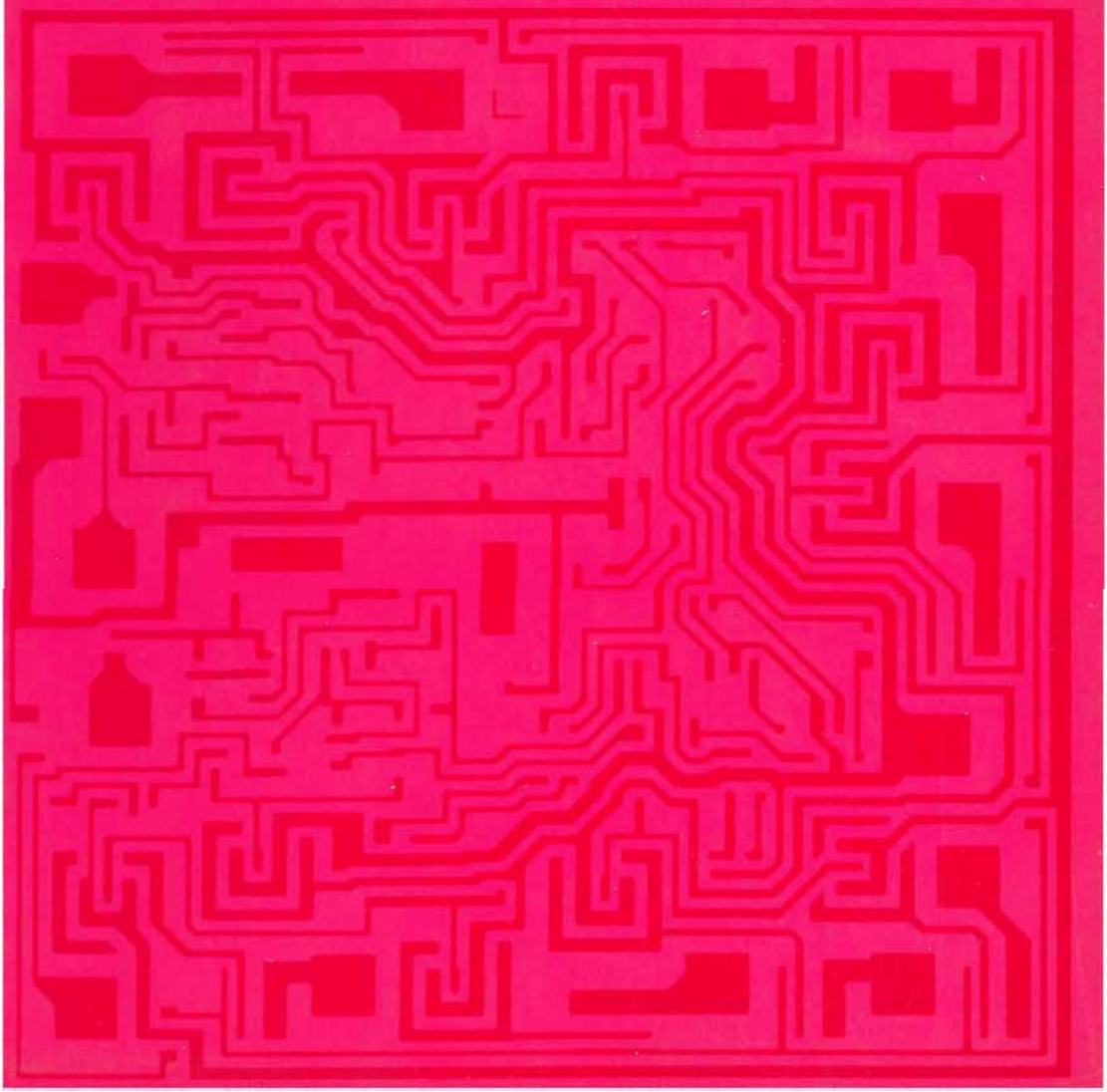
PROFESSIONAL SEMICONDUCTOR

DATABOOK 2

SGS ATES

LINEAR INTEGRATED CIRCUITS
DIGITAL INTEGRATED CIRCUITS
1973/74



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1973/74

INTRODUCTION

This databook contains data sheets on the SGS-ATES range of silicon integrated circuits intended for professional applications. To permit ease of consultation, it has been divided into seven main sections:
Index, Linear, DTL, LPDTL, TTL, HLL and MOS integrated circuits.
In addition, the Company has a number of RTL integrated circuits in production as specified on page 509. These devices are not recommended for new designs, but data sheets can be supplied on request.
At the beginning of each section, an analytical index of applications refers to the corresponding pages containing fully characterized data on the appropriate types. The information on each product has been specially presented in order that the performance of the product can be readily evaluated within any required equipment design.
Particular attention has been given to the measurement of the characteristics of all integrated circuits to ensure that they conform to the Company's Semiconductor Users' Reliability Evaluation programme (SURE).
The SURE programme has been carefully devised so as to be compatible with any national or international quality assurance programme. It is continuous (performed on all production batches), repetitive (performed under fixed conditions) and comprehensive (represents as many military and industrial specifications as possible).
It is emphasised that all products are produced from the same high grade silicon material and by the same manufacturing processes, the only difference in their classification being in the number and severity of tests applied and the degree of information supplied on each test.

OTHER SGS-ATES DATABOOKS

Data sheets on the SGS-ATES range of discrete devices for professional applications, discrete devices and integrated circuits for consumer applications, and high power devices for consumer and professional applications can be found in the following databooks:

SGS-ATES Professional Semiconductor Databook 1

SGS-ATES Consumer Semiconductor Databook

SGS-ATES Power Semiconductor Databook

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GENERAL ALPHA-NUMERICAL INDEX

E. = Extended temperature range
S. = Standard temperature range
* Intermediate temperature range

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9915	RTL	509	509
9926	RTL	509	509
9927	RTL	509	509
9930	DTL	139	169
9932	DTL	144	175
9933	DTL	147	178
9934	DTL	—	170
9935	DTL	140	171
9936	DTL	141	172
9944	DTL	145	176
9945	DTL	149	179
9946	DTL	142	173
9948	DTL	149	179
9951	DTL	156	186
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9974	RTL	509	509

E. = Extended temperature range
S. = Standard temperature range
* Intermediate temperature range

LINEAR INTEGRATED CIRCUITS

LINEAR INTEGRATED CIRCUITS

Voltage regulator

STANDARD TEMPERATURE RANGE, 0°C ÷ 70°C

- OUTPUT CURRENT > 600 mA
- TIGHT TOLERANCE FOR OUTPUT VOLTAGE
- LOAD REGULATION LESS THAN 1%
- RIPPLE REJECTION 62 dB TYPICAL
- OVERLOAD AND SHORT CIRCUIT PROTECTION

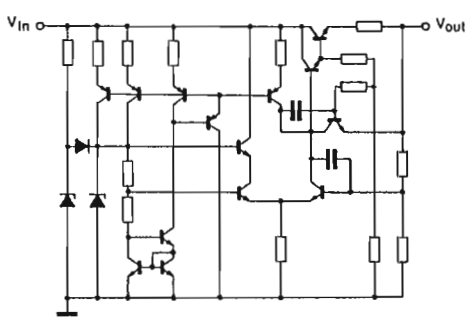
The L 005 T1 is a monolithic 5V voltage regulator which can supply more than 600 mA.
The device features high temperature stability, internal overload and short circuit protection, low output impedance and excellent transient response.
The L 005 T1 is intended for use as voltage supply for digital circuits and for any other industrial application.

ABSOLUTE MAXIMUM RATINGS

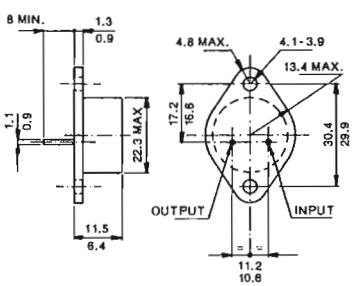
Input Voltage	20V
Power Dissipation (free air, $T_A = 25°C$)	3.25W
Power Dissipation (with infinite heat sink, $T_C = 25°C$)	12.75W
Storage Temperature Range	−55°C ÷ 150°C
Operating Temperature Range	0°C to + 70°C

ORDERING NUMBER
L005 T1

SCHEMATIC DIAGRAM



PHYSICAL DIMENSIONS
In accordance with
JEDEC TO - 3 outline



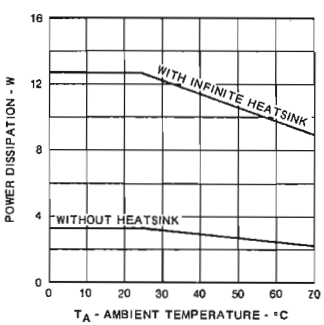
Notes:
All dimensions in mm.
Leads 1 and 2 electrically isolated from case.
Case is third electrical connection (ground).
Leads are gold-plated nickel-alloy.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

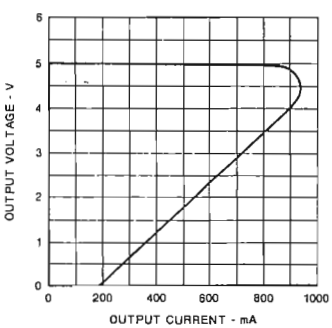
PARAMETER	CONDITIONS	Min.	Typ.	Max.	Unit
Output Voltage	V_{in} = 7.5V ÷ 20V, C_L = 10 μF, I_L = 10 mA	4.75	5.0	5.25	V
Load Regulation	V_{in} = 12V, I_L = 0 ÷ 600 mA		0.3	1	% Vout
Regulated Output Current	V_{in} = 12V, $\frac{\Delta Vout}{Vout} \leq 1\%$	600	850		mA
Maximum Output Current	V_{in} = 12V		930	1200	mA
Output Resistance	V_{in} = 12V, I_L = 0.6A		15		mΩ
Line Regulation	V_{in} = 7.5V ÷ 12V, C_L = 10 μF, I_L = 10 mA		0.1	0.5	% Vout
Ripple Rejection	V_{in} = 10V, ΔV_{in} = 4V_{pp}, f = 100 Hz	46	62		dB
Output Noise Voltage	V_{in} = 12V, I_L = 10 mA, C_L = 20 μF BW = 10 Hz ÷ 100 KHz		0.07		mV
Standby Current	V_{in} = 20V, I_L = 0		9		mA
Temperature Coefficient	V_{in} = 12V, I_L = 10 mA, C_L = 10 μF T_A = 0°C ÷ 60°C		003		%/°C
Short Circuit Current	V_{in} = 12V, V_{out} = 0		190	250	mA

TYPICAL ELECTRICAL CHARACTERISTICS

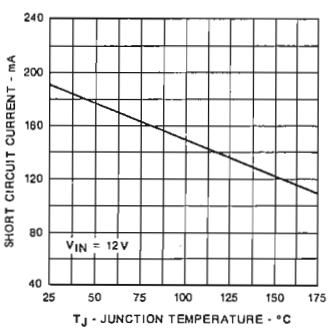
MAX ALLOWABLE POWER DISSIPATION VERSUS AMBIENT TEMPERATURE



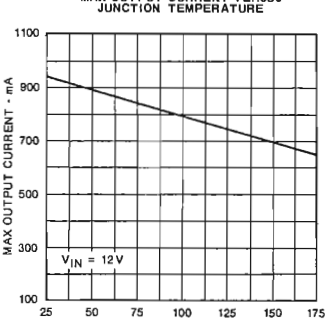
OUTPUT VOLTAGE VERSUS OUTPUT CURRENT



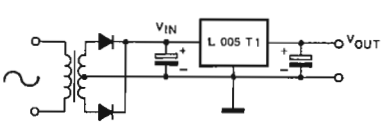
SHORT CIRCUIT CURRENT VERSUS JUNCTION TEMPERATURE



MAX OUTPUT CURRENT VERSUS JUNCTION TEMPERATURE



TYPICAL APPLICATION CIRCUIT



Balanced modulator

STANDARD TEMPERATURE RANGE -20° C TO 85° C

- SINGLE OR DUAL SUPPLY OPERATION
- LOW POWER CONSUMPTION
- LOW CARRIER LEAKAGE
- LOW DISTORTION
- LOW NOISE

The L 025 T9 is a linear integrated circuit intended for use as channel modulator and demodulator in FDM telephone equipment and as analogue AC multiplier in industrial and professional applications.
It features low quiescent power consumption, low distortion and intermodulation. The circuit requires a minimum number of external components.

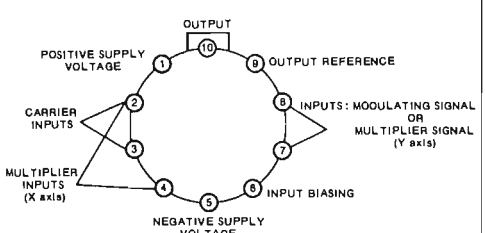
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	30 V
Differential Input Voltage	± 5 V
Power Dissipation (T_A = 70°C) (1)	300 mW
Storage Temperature	-55°C to 150°C
Operating Temperature	-20°C to 85°C

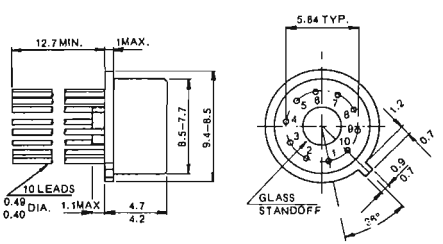
ORDERING NUMBER
L 025 T9

(1) Derate linearly at 3.75 mW/° C for ambient temperature above 70° C

CONNECTION DIAGRAM
(top view)



PHYSICAL DIMENSIONS
in accordance with
JEDEC TO-100 outline



Note: all dimensions in mm.

ELECTRICAL CHARACTERISTICS:

WORKING CONDITIONS FOR THE CIRCUIT SHOWN IN FIG. 2
(unless otherwise specified)

Supply Voltage	V_{CC} = -20V
Carrier Frequency	f_c = 130 KHz
Modulating Signal Frequency	f_m = 25 KHz
Output Signal Level $[f_c \pm f_m = (130 \pm 25)KHz]$	V_o = -15dBv
Input Carrier Signal Level	V_c = -13dBv
Load Resistance	R_L = 600Ω
Ambient Temperature	T_A = 25°C

PARAMETER	CONDITIONS	Min.	Typ.	Max.	UNIT
Operating Supply Voltage Range		12		30	V
Supply Current	V_{CC} = ± 10V		2	2.5	mA
Input Bias Current: $\frac{I_2 + I_3}{2}$	V_{CC} = ± 10V		0.7	2	μA
$\frac{I_2 + I_4}{2}$	V_{CC} = ± 10V		0.7	2	μA
$\frac{I_7 + I_8}{2}$	V_{CC} = ± 10V		1.4	4	μA
Input Offset Current: $I_2 - I_3$ $I_2 - I_4$ $I_7 - I_8$	V_{CC} = ± 10V V_{CC} = ± 10V V_{CC} = ± 10V		50 70 100		nA nA nA
Input Common Mode Voltage: Pos. Neg.	V_{CC} = ± 10V		 4.5 -8		 V V
DC Output Voltage (pin 10)		-3.2	-3.8	-4.6	V
Differential Output Voltage (pins 9; 10)			25	100	mV
Input Biasing Reference Voltage (pin 6)			-7.5		V
Input Resistance: pins 2 and 3 pins 2 and 4 pins 7 and 8			30 300 150		KΩ KΩ KΩ
Output Resistance	f = 1 KHz		3	10	Ω
Output Voltage Swing		1	1.3		Vpp
Common Mode Rejection Ratio:					
CM Signal: pins 2 and 3	{ CM signal (2-3) (V=700mV rms; f_1 = 10KHz) { Diff. signal (7-8) (V=350mV rms; f_2 = 40KHz)		98		dB
CM Signal: pins 2 and 4	{ CM signal (2-4) (V=700mV rms; f_1 = 10 KHz) { Diff. signal (7-8) (V=350mV rms; f_2 = 40KHz)		86		dB
CM Signal: pins 7 and 8	{ CM signal (7-8) (V=350mV rms; f_1 = 10KHz) { Diff. signal (2-3) (V=175mV rms; f_2 = 40KHz)		80		dB
Supply Voltage Rejection Ratio: Pos. Neg.	V_{CC} = ± 10V f = 1 KHz		 33 80		 dB dB
Scale Factor K	V_{CC} = ± 10V		3.2		V^{-1}
Conversion Gain G_c		4.5	5	5.5	dB
Carrier Leakage	$V_{modulating}$ = 0		-35		dBv
Modulating Signal Leakage $\frac{V_{fm}}{V_{(fc \pm fm)}}$			-35	-50	dBmo
2nd Harmonic Modulating Signal Leakage $\frac{V_{(2fm)}}{V_{(fc \pm fm)}}$				-75	dBmo
2nd Harmonic Distortion $\frac{V_{(fc \pm 2fm)}}{V_{(fc \pm fm)}}$			-60	-75	dBmo
2nd Harmonic Distortion $\frac{V_{2(fc \pm fm)}}{V_{(fc \pm fm)}}$			-55	-80	dBmo
3rd Harmonic Distortion $\frac{V_{(fc \pm 3fm)}}{V_{(fc \pm fm)}}$			-60	-79	dBmo
Low Frequency Thermal Noise	$V_{modulating}$ = 0 f = 1KHz BW = 100 Hz	-115	-125		dBv
High Frequency Thermal Noise	$V_{modulating}$ = 0 f = 30KHz BW = 100 Hz		-127		dBv
Conversion Gain Change	T_A = 10°C to 50°C		±0.1		dB

ELECTRICAL DIAGRAM

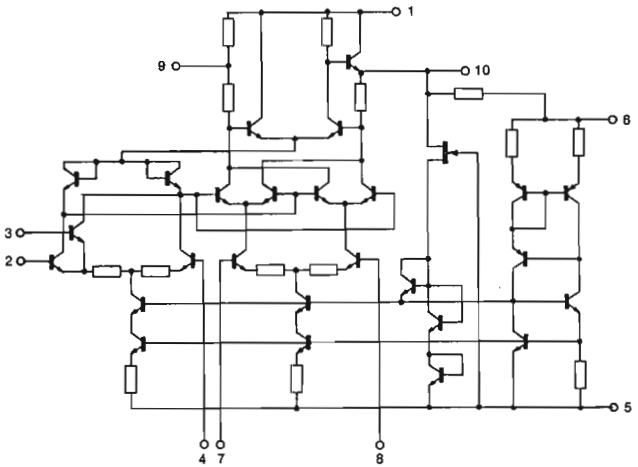


FIG. 1

TYPICAL APPLICATION OF MODULATOR WITH ONE SUPPLY VOLTAGE

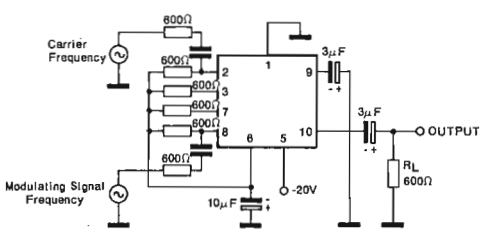


FIG. 2

DEFINITION OF UNITS:

dBm: power gain ($10 \lg \frac{P_2}{P_1}$) is expressed in dBm when P_1 is 1mW, therefore 0 dBm = 1mW.

dBmo: the power is expressed in dBmo when referred to an established power level in the circuit, generally the output signal level.

e.g. if the output level is -15 dBm and this level is chosen as reference, then we say 0 dBmo = -15 dBm; if another signal, i.e. the distortion measured at the same point of the circuit is -90 dBm, we can say that the distortion is -75 dBmo.

dBv: $20 \text{ Log } \frac{V_2}{V_1}$ when $V_1 = 775$ mVrms

DEFINITION OF TERMS:

Common mode rejection ratio: $CMRR = 20 \lg \frac{V_{CM}G}{V_{out}}$

with G = Conversion gain with specified circuit conditions
V_{CM} = Common mode signal level
V_{out} = Output signal level at frequency = $f_2 \pm f_1$

Scale factor: $K = \frac{V_{out}}{V_x V_y}$

with V_x = voltage input 2 - 4
V_y = voltage input 7 - 8

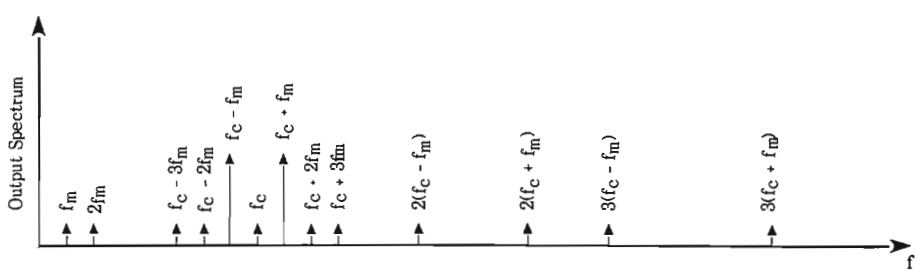
Conversion gain: $G_c = 20 \log \frac{V_{out\ (f_c \pm f_m)}}{V_{in\ (f_m)}}$

Carrier leakage: is defined as the output voltage at carrier frequency with only the carrier applied to the input (modulating voltage = 0)

Modulating signal leakage: is defined as the output voltage, at modulating frequency, referred to fundamental carrier sidebands

$M.S.L. = 20 \log \frac{V_{out\ (f_m)}}{V_{out\ (f_c \pm f_m)}}$

OUTPUT SPECTRUM VS. FREQUENCY



f_c = carrier fundamental (leakage)

f_m = mod. sig. (leakage)

nf_m = harmonic modulating signal (leakage)

$f_c \pm f_m$ = fundamental carrier sidebands

$f_c \pm nf_m$ = fundamental carrier sideband harmonics

$n(f_c \pm f_m)$ = carrier harmonic sidebands

Voltage regulator

STANDARD TEMPERATURE RANGE, 0°C ÷ 70°C

- OUTPUT CURRENT > 500 mA
- TIGHT TOLERANCE FOR OUTPUT VOLTAGE
- LOAD REGULATION LESS THAN 1%
- RIPPLE REJECTION 61 dB TYP.
- OVERLOAD AND SHORT CIRCUIT PROTECTION

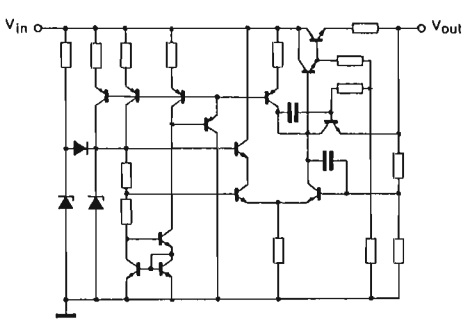
ORDERING NUMBER
L036 T1

The L 036 T1 is a monolithic 12V voltage regulator which can supply more than 500 mA.
The device features high temperature stability, internal overload and short circuit protection, low output impedance and excellent transient response.
The L 036 T1 is intended for use as voltage supply for digital circuit with high noise immunity, linear integrated circuits and for any other industrial application.

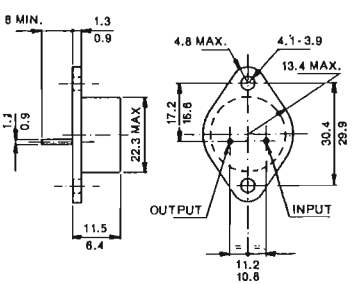
ABSOLUTE MAXIMUM RATINGS

Input Voltage	27V
Power Dissipation (free air, $T_A = 25°C$)	3.25W
Power Dissipation (with infinite heat sink, $T_C = 25°C$)	12.75W
Storage Temperature Range	−55°C ÷ 150°C
Operating Temperature Range	0°C to + 70°C

SCHEMATIC DIAGRAM



PHYSICAL DIMENSIONS
In accordance with
JEDEC TO - 3 outline



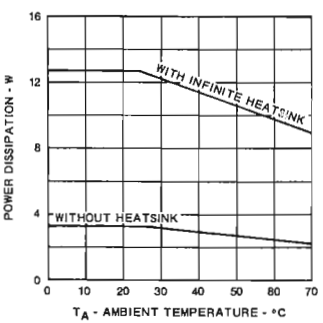
Notes:
All dimensions in mm.
Leads 1 and 2 electrically isolated from case.
Case is third electrical connection (ground).
Leads are gold-plated nickel-alloy.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

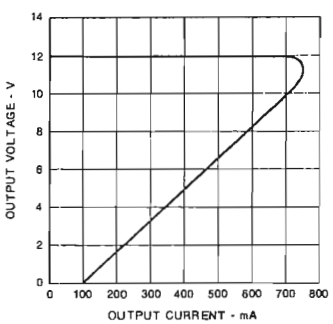
PARAMETER	CONDITIONS	Min.	Typ.	Max.	Unit
Output Voltage	V_{in} = 14.5 ÷ 27V, I_L = 10 mA, C_L = 10 μF	11.4	12	12.6	V
Load Regulation	V_{in} = 21V, I_L = 0 ÷ 500 mA		0.3	1	% Vout
Regulated Output Current	V_{in} = 21V, $\frac{\Delta Vout}{Vout} \leq 1\%$	500	720		mA
Maximum Output Current	V_{in} = 21V		750	1000	mA
Output Resistance	V_{in} = 21V, I_L = 500 mA		20		mΩ
Line Regulation	V_{in} = 14.5 ÷ 21V, C_L = 10 μF, I_L = 10 mA		0.1	0.5	%
Ripple Rejection	V_{in} = 19V, ΔV_{in} = 4 V_{pp}, f = 100 Hz, I_L = 10 mA	46	60		dB
Output Noise Voltage	V_{in} = 21V, I_L = 10 mA, C_L = 20 μF, BW = 10Hz ÷ 100 KHz		0.15		mV
Standby Current	V_{in} = 27V, I_L = 0		10		mA
Temperature Coefficient	V_{in} = 21V, I_L = 10 mA, T_A = 0°C ÷ 60°C		003		%/°C
Short Circuit Current	V_{in} = 21V, V_{out} = 0		100	200	mA

TYPICAL ELECTRICAL CHARACTERISTICS

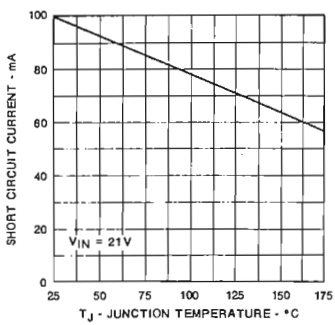
MAX ALLOWABLE POWER DISSIPATION VERSUS AMBIENT TEMPERATURE



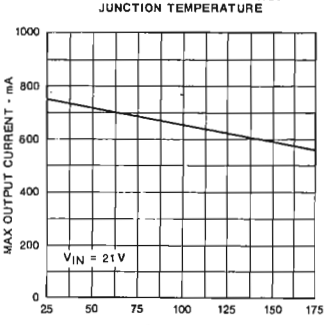
OUTPUT VOLTAGE VERSUS OUTPUT CURRENT



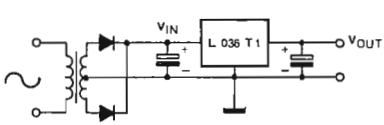
SHORT CIRCUIT CURRENT VERSUS JUNCTION TEMPERATURE



MAX OUTPUT CURRENT VERSUS JUNCTION TEMPERATURE



TYPICAL APPLICATION CIRCUIT



Voltage regulator

STANDARD TEMPERATURE RANGE, 0°C ÷ 70°C

- OUTPUT CURRENT > 450 mA
- TIGHT TOLERANCE FOR OUTPUT VOLTAGE
- LOAD REGULATION LESS THAN 1%
- RIPPLE REJECTION 56 dB
- OVERLOAD AND SHORT CIRCUIT PROTECTION

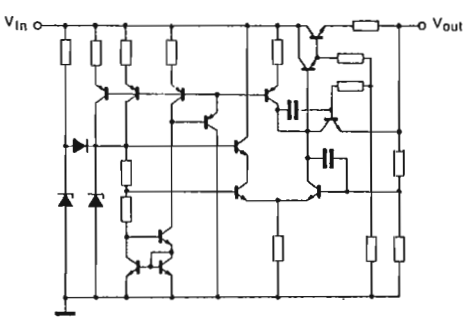
The L 037 T1 is a monolithic 15 V voltage regulator which can supply more than 450 mA.
The device features high temperature stability, internal overload and short circuit protection, low output impedance and excellent transient response.
The L 037 T1 is intended for use as voltage supply for linear integrated circuits, for digital circuits with high noise immunity and for any other industrial application.

ABSOLUTE MAXIMUM RATINGS

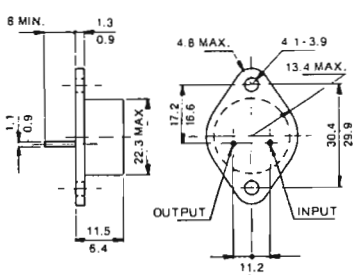
Input Voltage	27V
Power Dissipation (free air, T_A=25°C)	3.25W
Power Dissipation (with infinite heat sink, T_C=25°C)	12.75W
Storage Temperature Range	−55°C ÷ 150°C
Operating Temperature Range	0°C to + 70°C

ORDERING NUMBER
L037 T1

SCHEMATIC DIAGRAM



PHYSICAL DIMENSIONS
in accordance with
JEDEC TO - 3 outline



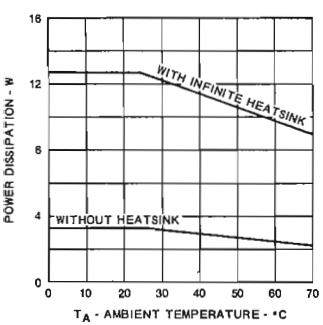
Notes
All dimensions in mm.
Leads 1 and 2 electrically isolated from case.
Case is third electrical connection (ground).
Leads are gold-plated nickel-alloy.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

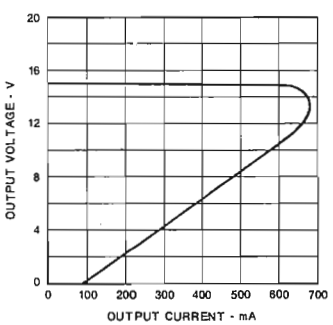
PARAMETER	CONDITIONS	Min.	Typ.	Max.	Unit
Output Voltage	V_{in}=17.5V÷27V, I_L=10 mA, C_L=10 μF	14.25	15	15.75	V
Load Regulation	V_{in}=24V, I_L=0÷450 mA		0.3	1	%Vout
Regulated Output Current	V_{in}=24V, $\frac{\Delta Vout}{Vout} \leq 1\%$	450	600		mA
Maximum Output Current	V_{in}=24V		680	900	mA
Output Resistance	V_{in}=24V, I_L=450 mA		27		mΩ
Line Regulation	V_{in}=17.5V÷24V, I_L=10 mA, C_L=10 μF		0.16	0.5	%
Ripple Rejection	V_{in}=22V, ΔV_{in}=4 Vpp, f = 100 Hz, I_L = 10 mA	46	56		dB
Output Noise Voltage	V_{in}=24V, I_L=10mA, C_L=20μF, BW=10Hz÷100KHz		0.18		mV
Standby Current	V_{in}=27V, I_L=0		10		mA
Temperature Coefficient	V_{in}=24V, I_L=10 mA, C_L=10μF, T_A=0÷60°C		003		%/°C
Short Circuit Current	V_{in}=24V		85	160	mA

TYPICAL ELECTRICAL CHARACTERISTICS

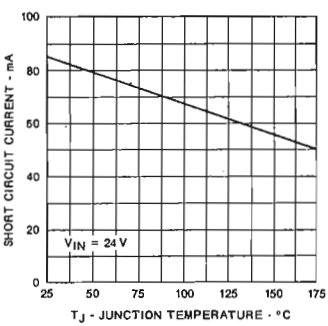
MAX ALLOWABLE POWER DISSIPATION VERSUS AMBIENT TEMPERATURE



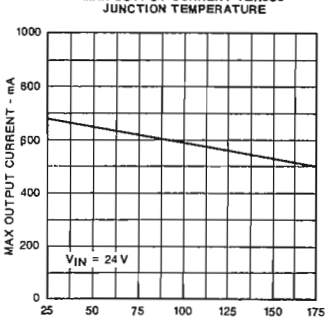
OUTPUT VOLTAGE VERSUS OUTPUT CURRENT



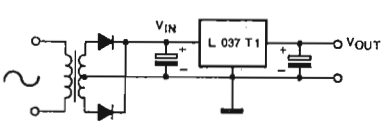
SHORT CIRCUIT CURRENT VERSUS JUNCTION TEMPERATURE



MAX OUTPUT CURRENT VERSUS JUNCTION TEMPERATURE



TYPICAL APPLICATION CIRCUIT



Channel amplifier

STANDARD TEMPERATURE RANGE, -20°C to +85°C

- LOW QUIESCENT POWER CONSUMPTION
- LOW DISTORTION
- HIGH GAIN
- SHORT CIRCUIT PROTECTION

The L 045 T9 is a linear integrated circuit intended for use as channel amplifier in FDM and PCM telephone equipments.
It features low quiescent power consumption, low distortion, high gain.
The L 045 T9 is short circuit protected and shows an offset voltage null capability.

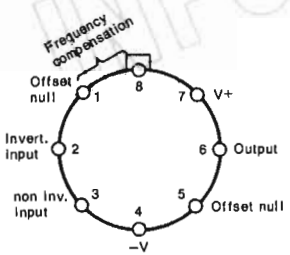
ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage	36V
Differential Input Voltage	±30V
Input Voltage	±12V
Power Dissipation (T_A = 70°C, see note 2)	500mW
Storage Temperature	−65°C ÷ 150°C
Operating Temperature	−20°C ÷ 85°C
Output short circuit duration	indefinite

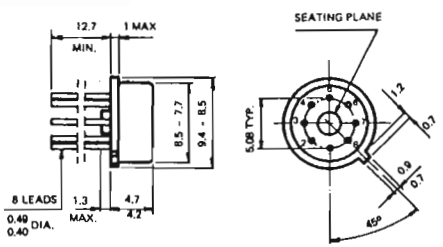
ORDERING NUMBER
L045 T9

Notes on the following page.

CONNECTION DIAGRAM
(top view)



PHYSICAL DIMENSIONS
in accordance with
JEDEC TO-99 outline



Notes: All dimensions in mm.

ELECTRICAL CHARACTERISTICS (note 3)

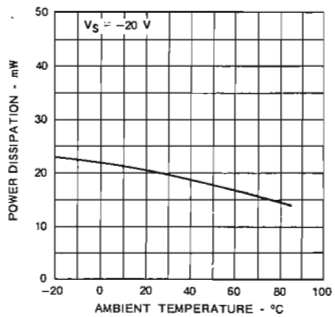
PARAMETER	CONDITIONS	Min.	Typ.	Max.	Unit
Input Offset Voltage	$R_S = 10\ K\Omega$		±1.5	±10	mV
Input Bias Current			100	750	nA
Input Resistance	open loop		2		MΩ
Output Resistance	open loop		75		Ω
Voltage Gain	$R_L = 2\ K\Omega$	83	100		dB
Total Harmonic Distortion	$P_{out} = -5dBm$ $G = 40dB$ $R_L eq. = 470\Omega$ $f = 1KHz$		1.5	3	‰
Total Harmonic Distortion	$P_{out} = 8dBm$ $G = 40dB$ $R_L eq. = 470\Omega$ $f = 1KHz$		1.5	3	‰
Quiescent Power Dissipation	$P_{out} = 0$		20	30	mW
Max Output Power	$R_L eq. = 470\Omega$ $THD \leq 1\%$ $G = 40dB$	14	16		dBm
Noise Power Referred to Input	$R_S \leq 1.5K\Omega$ $G = 40dB$ $f = 1KHz$ $BW = 100Hz$			-120.5	dBm
Supply Voltage Rejection Ratio Referred to Output	$f = 1KHz$ $G = 40dB$	30	36		dB
The Following Specifications apply for $-20°C \leq T_A \leq +85°C$:					
Input Offset Voltage	$R_S = 10\ K\Omega$			±15	mV
Input Bias Current				1.5	μA
Voltage Gain	$R_L = 2\ K\Omega$	78			dB

NOTES:

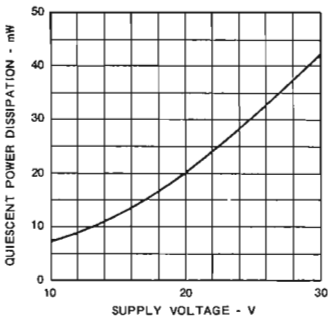
(1) T_A = 25°C unless otherwise noted.
(2) Derate linearly at 6.25 mW/°C for ambient temperature above 70°C.
(3) T_A = 25°C, V_S = −20V, V_R = −10V unless otherwise noted, for V_R see "Typical channel amplifier circuit".

TYPICAL ELECTRICAL CHARACTERISTICS (25° C free air temperature unless otherwise noted)

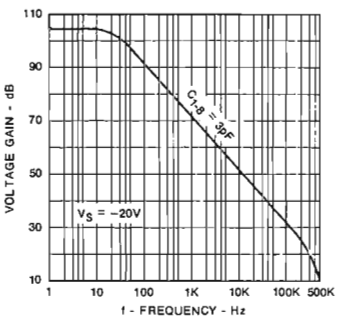
QUIESCENT POWER DISSIPATION VERSUS AMBIENT TEMPERATURE



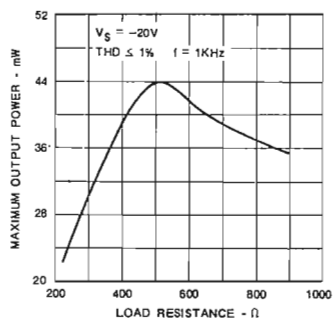
QUIESCENT POWER DISSIPATION VERSUS SUPPLY VOLTAGE



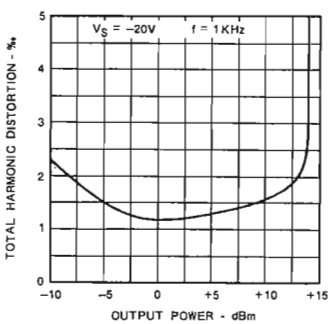
OPEN LOOP GAIN VERSUS FREQUENCY



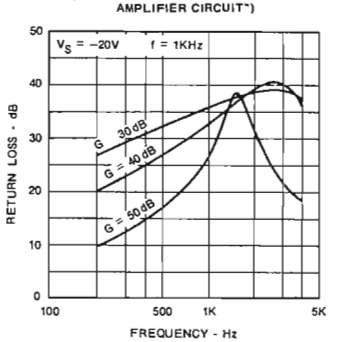
MAXIMUM OUTPUT POWER VERSUS LOAD RESISTANCE



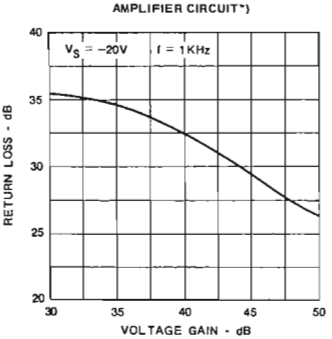
TOTAL HARMONIC DISTORTION VERSUS OUTPUT POWER



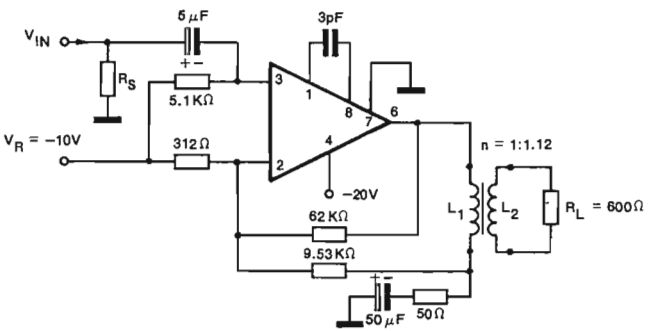
RETURN LOSS VERSUS FREQUENCY (RELATIVE TO "TYPICAL CHANNEL AMPLIFIER CIRCUIT")



RETURN LOSS VERSUS VOLTAGE GAIN (RELATIVE TO "TYPICAL CHANNEL AMPLIFIER CIRCUIT")



TYPICAL CHANNEL AMPLIFIER CIRCUIT



L_1 = 120 mH. Series resistance of: L_1 = 20Ω

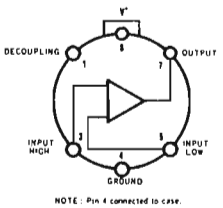
L_2 = 20Ω

RF-IF amplifier

EXTENDED TEMPERATURE RANGE, - 55°C + 125°C

The L 103 is an RF - IF amplifier constructed on a single silicon chip and is intended for use as a limiting or non-limiting amplifier, harmonic mixer, or oscillator to 150 MHz. The low internal feedback of the device insures a higher stability-limited gain than that available from conventional circuitry. Including the biasing network in the same package reduces the number of external components required, thereby increasing the reliability of the device.

CONNECTION DIAGRAM
(Top view)



ABSOLUTE MAXIMUM RATINGS
(above which the useful life may be impaired)

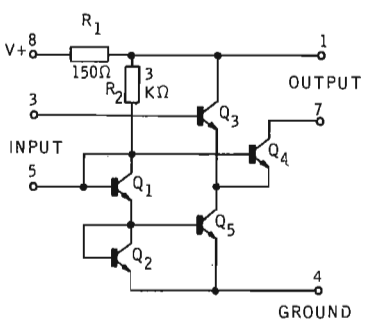
Supply Voltage	20 V
Output Collector Voltage	24 V
Voltage Between Input Terminals	±5 V
Internal Power Dissipation (1)	200 mW
Operating Temperature Range	- 55°C to + 125°C
Storage Temperature Range	- 65°C to + 150°C
Lead Temperature (Soldering, 60 sec)	+ 300°C

ORDERING NUMBER

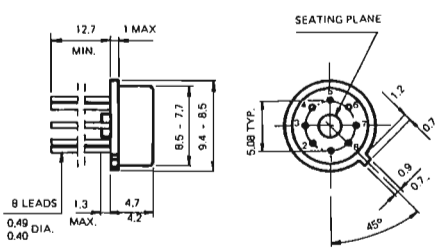
L 103 T2

NOTE 1 : Rating applies for ambient temperatures to 125°C.

SCHEMATIC DIAGRAM



PHYSICAL DIMENSIONS
in accordance with
JEDEC TO-99 outline

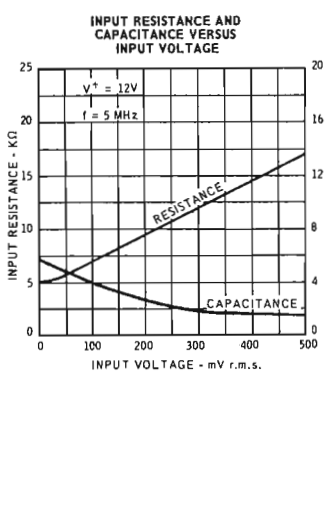


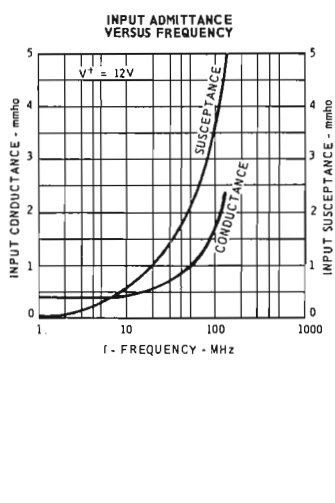
Notes: All dimensions in mm.

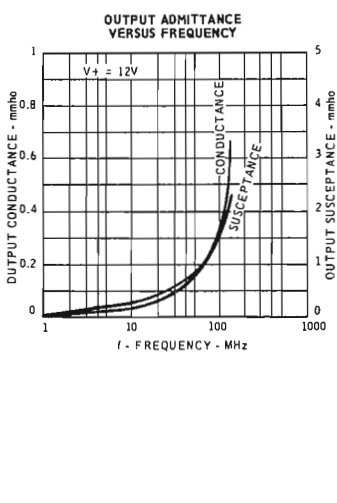
ELECTRICAL CHARACTERISTICS (T_A = 25°C, V^+ = 12 V unless otherwise noted)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Power Consumption	$e_{in} = 0$		110	170	mW
Quiescent Output Current	$e_{in} = 0$	2.1	2.5	2.8	mA
Peak-to-Peak Output Current	e_{in} = 400 mV rms, f = 1KHz	4			mA
Output Saturation Voltage				1.7	V
Forward Transadmittance	e_{in} = 10 mV rms, f = 1 KHz	29	35		mmho
Input Conductance	e_{in} < 10 mV rms, f ≤ 5 MHz		0.20	0.28	mmho
Input Capacitance	e_{in} < 10 mV rms, f ≤ 5 MHz		6	9	pF
Output Capacitance	f ≤ 5 MHz		2	3	pF
Output Conductance	f ≤ 5 MHz		0.02	0.04	mmho
Noise figure	f = 30 MHz, R_S = 500 Ω		6.5		dB
	f = 100 MHz, R_S = 500 Ω		8		dB
The following specifications apply for −55°C ≤ T_A ≤ +125 °C					
Quiescent Output Current	$e_{in} = 0$	1.7		2.8	mA
Peak-to-Peak Output Current	e_{in} = 400 mV rms, f = 1 KHz	3.2			mA
Output Saturation Voltage				1.8	V
Forward Transadmittance	e_{in} = 10 mV rms, f = 1 KHz	21			mmho
Input Conductance	e_{in} < 10 mV rms, f ≤ 5 MHz			0.48	mmho
Output Conductance	f ≤ 5 MHz			0.05	mmho

TYPICAL ELECTRICAL CHARACTERISTICS (25°C free air temperature unless otherwise noted)

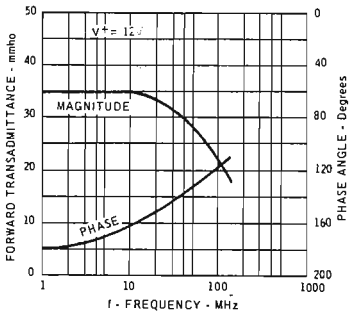




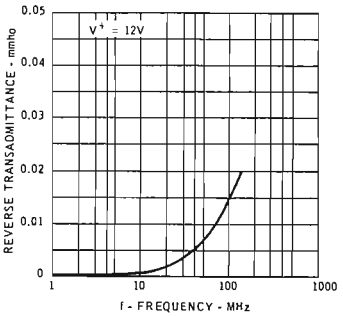


TYPICAL ELECTRICAL CHARACTERISTICS (25°C free air temperature unless otherwise noted)

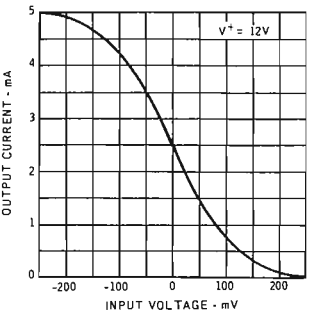
FORWARD TRANSADMITTANCE VERSUS FREQUENCY



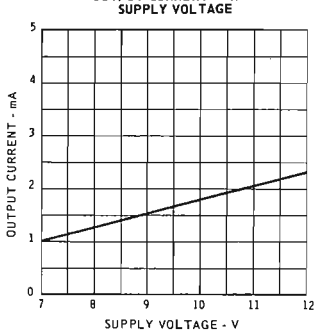
REVERSE TRANSADMITTANCE VERSUS FREQUENCY



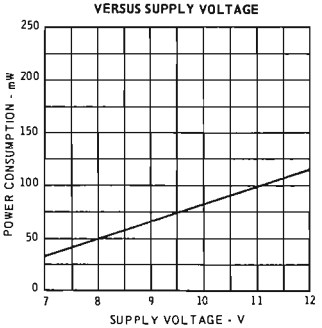
OUTPUT CURRENT VERSUS INPUT VOLTAGE



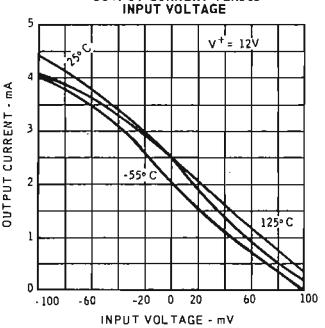
OUTPUT CURRENT VERSUS SUPPLY VOLTAGE



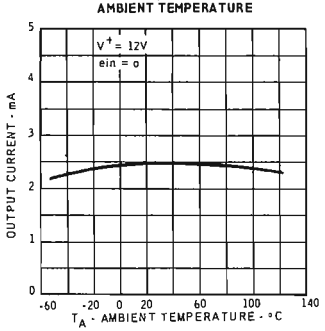
POWER CONSUMPTION VERSUS SUPPLY VOLTAGE



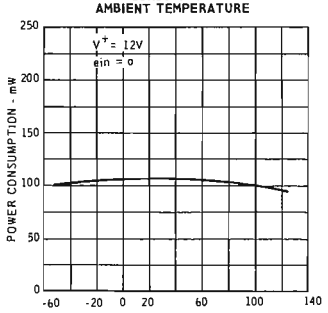
OUTPUT CURRENT VERSUS INPUT VOLTAGE



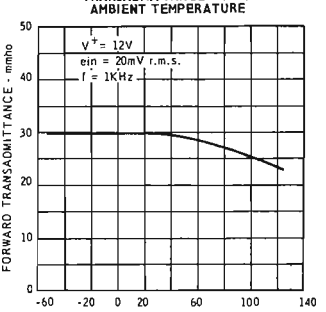
OUTPUT CURRENT VERSUS AMBIENT TEMPERATURE



POWER CONSUMPTION VERSUS AMBIENT TEMPERATURE



TRANSADMITTANCE VERSUS AMBIENT TEMPERATURE



DEFINITION OF TERMS

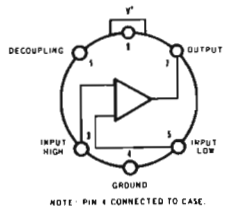
POWER CONSUMPTION – The DC power required to operate the device with no signal applied.
QUIESCENT OUTPUT CURRENT – The DC current delivered to the load with the input terminals short - circuited.
PEAK-TO-PEAK OUTPUT CURRENT - The short-circuit output current excursion for a large-signal input voltage.
OUTPUT SATURATION VOLTAGE - The minimum voltage to which the output collector may be reduced without degrading circuit performance.
TRANSADMITTANCE - The ratio of the output current to the input voltage.
INPUT ADMITTANCE - The admittance between the input terminals with the output short-circuited.
OUTPUT ADMITTANCE - The admittance between the output terminals with the input short-circuited.

RF-IF amplifier

STANDARD TEMPERATURE RANGE, 0°C ÷ 70°C

The L 103 is an RF - IF amplifier constructed on a single silicon chip and is intended for use as a limiting or non - limiting amplifier, harmonic mixer, or oscillator to 150 MHz. The low internal feedback of the device insures a higher stability limited gain than that available from conventional circuitry. Including the biasing network in the same package reduces the number of external components required, thereby increasing the reliability of the device.

CONNECTION DIAGRAM
(top view)



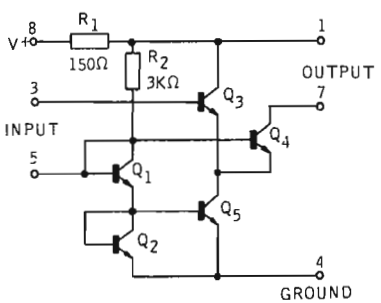
ABSOLUTE MAXIMUM RATINGS
(above which the useful life may be impaired)

Supply Voltage	20 V
Output Collector Voltage	24 V
Voltage Between Input Terminals	± 5 V
Internal Power Dissipation (1)	200 mW
Operating Temperature Range	0°C to + 70°C
Storage Temperature Range	- 65°C to + 150°C
Lead Temperature (Soldering, 60 sec.)	+ 300°C

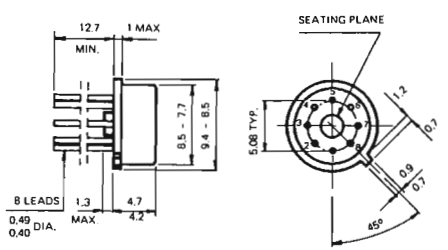
ORDERING NUMBER
L 103T1

Note 1 : Rating applies for ambient temperature to 70°C

SCHEMATIC DIAGRAM



PHYSICAL DIMENSIONS
in accordance with
JEDEC TO-99 outline

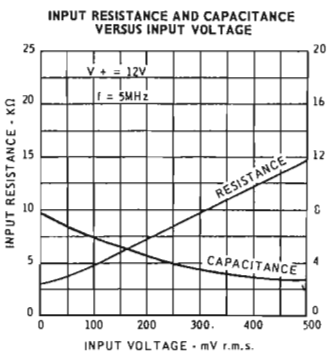


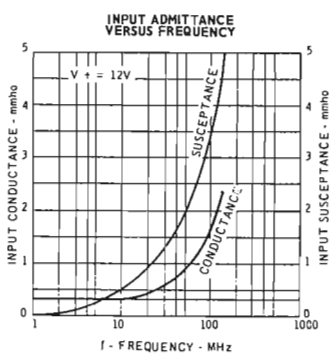
Notes: All dimensions in mm.

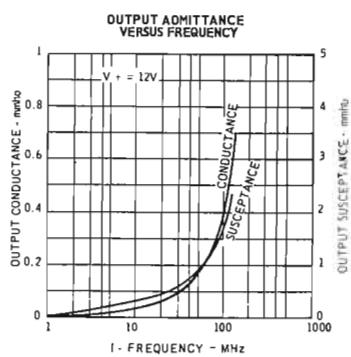
ELECTRICAL CHARACTERISTICS (T_A = 25°C, V^+ = 12 V unless otherwise noted)

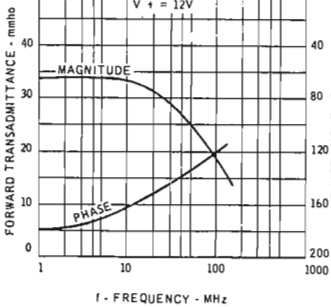
PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Power Consumption	e_{in} = 0		110	170	mW
Quiescent Output Current	e_{in} = 0	1.9	2.5	3.3	mA
Peak - to - Peak Output Current	e_{in} = 400 mV, f = 1 KHz	3.6			mA
Output Saturation Voltage				1.7	V
Forward Transadmittance	e_{in} = 10 mV rms, f = 1 KHz	23	33		mmho
Input Conductance	e_{in} < 10 mV rms, f ≤ 5 MHz		0.35	0.50	mmho
Input Capacitance	e_{in} < 10 mV rms, f ≤ 5 MHz		8	11	pF
Output Capacitance	f ≤ 5 MHz		2	3	pF
Output Conductance	f ≤ 5 MHz			0.05	mmho
Noise Figure	f = 30 MHz, R_S = 500 Ω		6.5		dB
	f = 100 MHz, R_S = 500 Ω		8		dB
The following specifications apply for 0°C ≤ T_A ≤ 70°C :					
Quiescent Output Current	e_{in} = 0	1.7		3.5	mA
Peak - to - Peak Output Current	e_{in} = 400 mV rms, f = 1 KHz	3.2			mA
Output Saturation Voltage				1.8	V
Forward Transadmittance	e_{in} = 10 mV rms, f = 1 KHz	22			mmho
Input Conductance	e_{in} ≤ 10 mV rms, f ≤ 5 MHz			0.71	mmho
Output Conductance	f ≤ 5 MHz			0.06	mmho

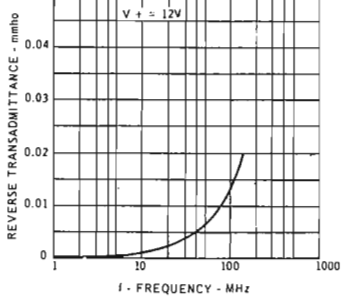
TYPICAL ELECTRICAL CHARACTERISTICS (25°C free air temperature unless otherwise noted)

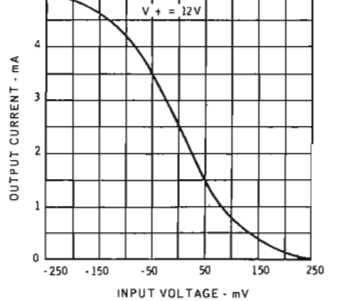












High speed operational amplifier

STANDARD TEMPERATURE RANGE,
0°C to 70°C

- HIGH SLEW RATE : 100V/ μS
- FAST SETTLING TIME : 300 ns
- WIDE BANDWIDTH : 65 MHz
- WIDE OPERATING SUPPLY RANGE
- WIDE INPUT VOLTAGE RANGES

The L 115 is a high speed, high gain, monolithic operational amplifier constructed on a single chip using the planar epitaxial process. It is intended for use in a wide range of applications where fast signal acquisition or wide bandwidth is required. The L 115 features fast settling time, high slew rate, low offsets, and high output swing for large signal applications. In addition, the device displays excellent temperature stability and will operate over a wide range of supply voltages. The L 115 is ideally suited for use in A to D and D to A converters, active filters, deflection amplifiers, video amplifiers, phase locked loops, multiplexed analogue gates, precision comparators, sample and holds, and general feedback applications requiring wide (including DC) bandwidth operation.

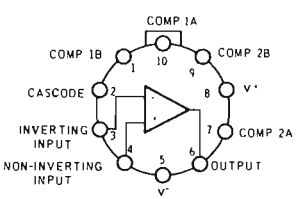
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	± 18 V
Internal Power Dissipation (note 1)	500 mW
Differential Input Voltage	± 6.5V
Input Voltage (note 2)	± 15V
Storage Temperature Range	-55°C to 150°C
Operating Temperature Range	0°C to 70°C
Lead Temperature (Soldering, 60 secs)	300°C

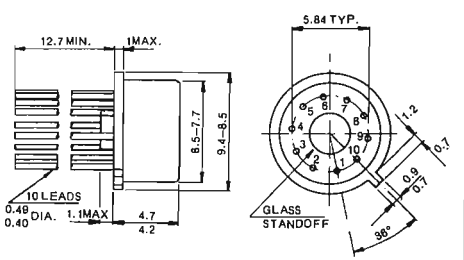
ORDERING NUMBER
L 115 T1

Notes on the following page.

CONNECTION DIAGRAM
(top view)



PHYSICAL DIMENSIONS
in accordance with
JEDEC TO-100 outline



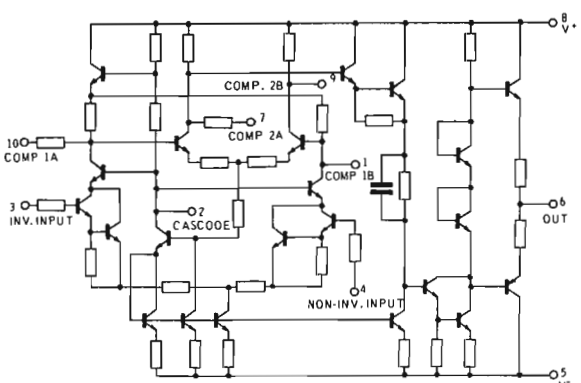
Note : all dimensions in mm.

STANDARD TEMPERATURE RANGE

ELECTRICAL CHARACTERISTICS (V_{CC} = ± 15V, T_A =25°C unless otherwise noted)

PARAMETER	CONDITIONS	Min.	Typ.	Max.	UNIT
Input Offset Voltage	$R_S \leq 10\ k\Omega$		± 2	± 7.5	mV
Input Offset Current			± 70	± 250	nA
Input Bias Current			0.4	1.5	µA
Input Resistance			1		MΩ
Input Voltage Range		± 10	± 12		V
Common Mode Rejection Ratio	$R_S \leq 10\ k\Omega$	74	92		dB
Supply Voltage Rejection Ratio	$R_S \leq 10\ k\Omega$		45	400	µV / V
Large Signal Voltage Gain	$R_L \geq 2k\Omega$ V_{OUT}= ± 10V	10,000	30,000		
Output Resistance			75		Ω
Supply Current			5.5	10	mA
Power Consumption			165	300	mW
Acquisition Time (Unity Gain)	V_{OUT} = + 5V		800		ns
Settling Time (Unity Gain)			300		ns
Transient Response (Unity Gain)	V_{IN} = 400 mV				
Rise Time			30	75	ns
Overshoot			25-	50	%
Slew Rate	A_V = 100		70		V/ µs
	A_V = 10		38		V/ µs
	A_V = 1 (non-inverting)	10	18		V/ µs
	A_V = 1 (inverting)		100		V/ µs
The following apply for $0°C \leq T_A \leq +70°C$:					
Input Offset Voltage	$R_S \leq 10\ k\Omega$			± 10	mV
Input Offset Current	T_A = + 70°C			± 250	nA
	T_A = 0°C			± 750	nA
Input Bias Current	T_A = + 70°C			1.5	µA
	T_A = 0°C			7.5	µA
Large Signal Voltage Gain	$R_L \geq 2\ k\Omega$ V_{OUT} =± 10V	8,000			
Output Voltage Swing	$R_L \geq 2\ k\Omega$	± 10	± 13		V

EQUIVALENT CIRCUIT

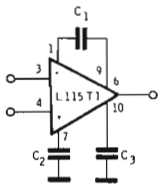


NOTES :

1) Rating applies for ambient temperatures to +70°C.
2) For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

COMPENSATION COMPONENTS VALUES

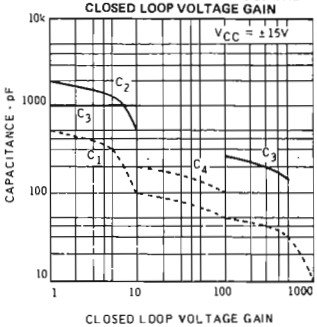
FREQUENCY COMPENSATION CIRCUIT



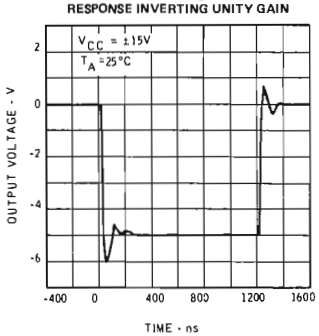
CLOSED LOOP GAIN	C_1	C_2	C_3
1000	10 pF		
100	50 pF		250 pF
10*	100 pF	500 pF	1000 pF
1	500 pF	2000 pF	1000 pF

* For Gain 10, compensation may be simplified by removing C_2, C_3 and adding a 200 pF capacitor (C_4) between Pin 7 and 10.

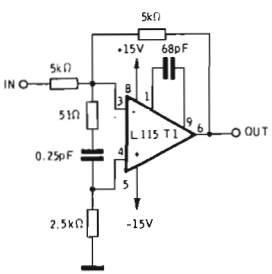
SUGGESTED VALUES OF COMPENSATION CAPACITORS AS A FUNCTION OF THE CLOSED LOOP VOLTAGE GAIN



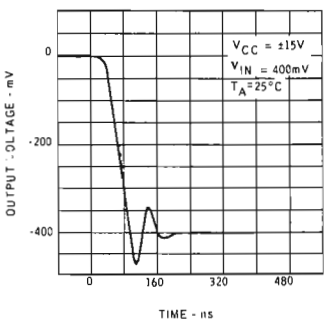
LARGE SIGNAL PULSE RESPONSE INVERTING UNITY GAIN



INVERTING UNITY GAIN HIGH SLEW RATE CIRCUIT

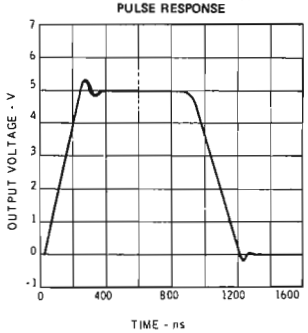


SMALL SIGNAL PULSE RESPONSE INVERTING UNITY GAIN

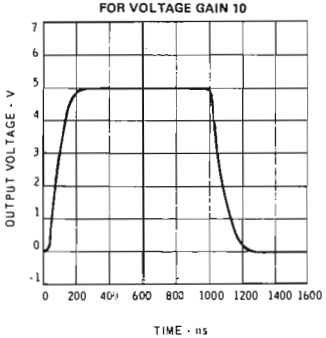


TYPICAL ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = ±15V unless otherwise noted)

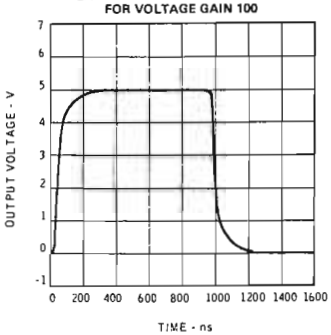
UNITY GAIN LARGE SIGNAL PULSE RESPONSE



LARGE SIGNAL PULSE RESPONSE FOR VOLTAGE GAIN 10

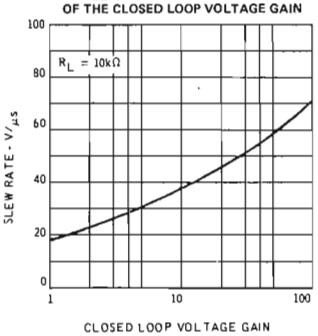


LARGE SIGNAL PULSE RESPONSE FOR VOLTAGE GAIN 100

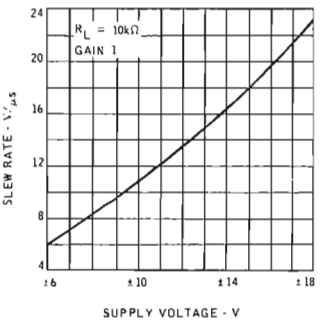


TYPICAL ELECTRICAL CHARACTERISTICS (T_A = 25°C. V_{CC} = ±15V unless otherwise noted)

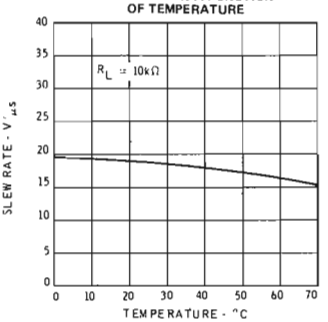
SLEW RATE AS A FUNCTION OF THE CLOSED LOOP VOLTAGE GAIN



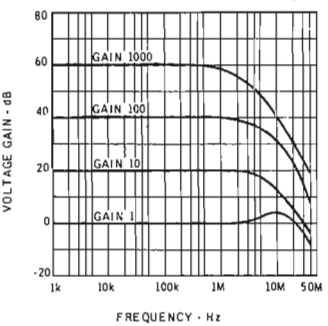
SLEW RATE AS A FUNCTION OF SUPPLY VOLTAGE



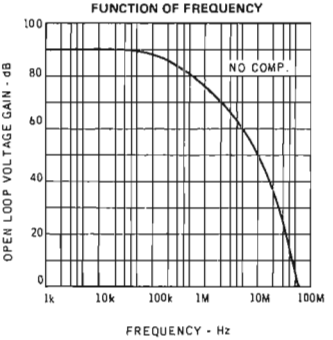
SLEW RATE AS A FUNCTION OF TEMPERATURE



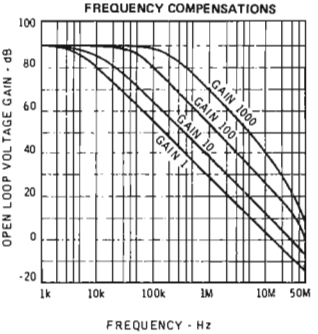
CLOSED LOOP FREQUENCY RESPONSE FOR VARIOUS GAIN CONFIGURATIONS



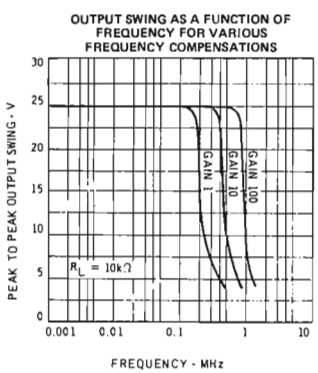
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



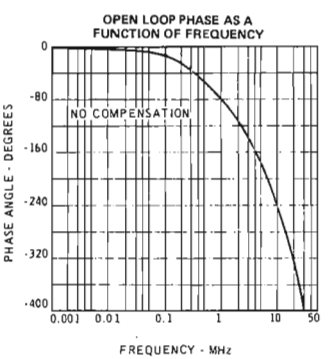
OPEN LOOP RESPONSE WITH COMPENSATION NECESSARY FOR VARIOUS FREQUENCY COMPENSATIONS



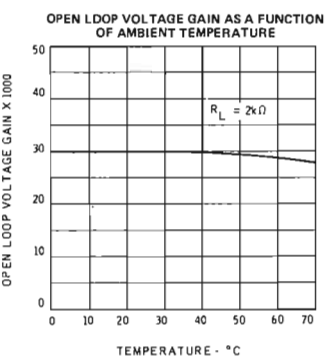
OUTPUT SWING AS A FUNCTION OF FREQUENCY FOR VARIOUS FREQUENCY COMPENSATIONS



OPEN LOOP PHASE AS A FUNCTION OF FREQUENCY

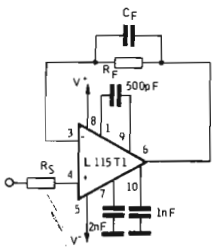


OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE

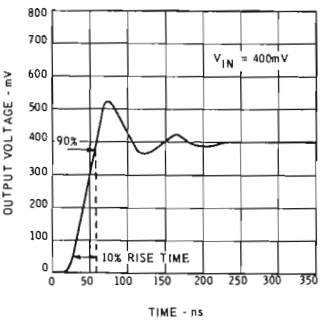


TYPICAL ELECTRICAL CHARACTERISTICS (T_A = 25°C: V_{CC} = ±15V unless otherwise noted)

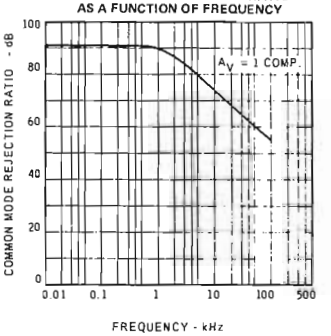
VOLTAGE FOLLOWER



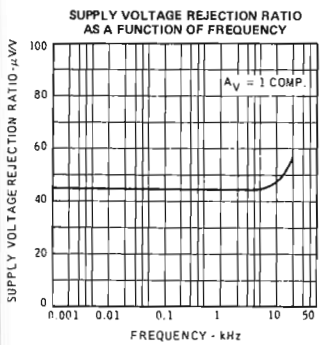
VOLTAGE FOLLOWER TRANSIENT RESPONSE



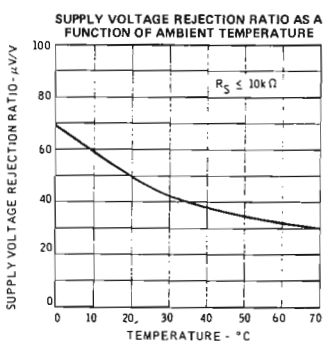
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



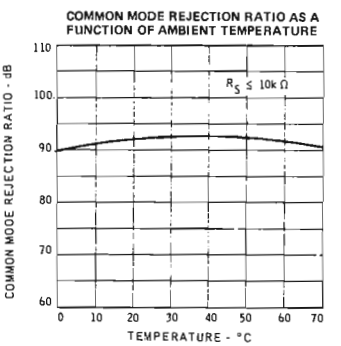
SUPPLY VOLTAGE REJECTION RATIO AS A FUNCTION OF FREQUENCY



SUPPLY VOLTAGE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE

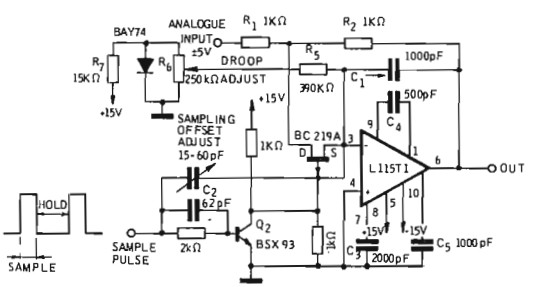


COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



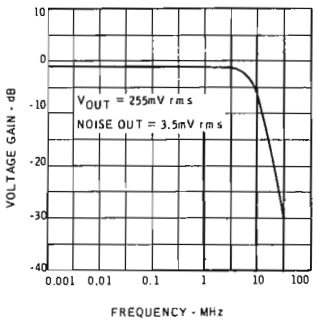
TYPICAL APPLICATIONS

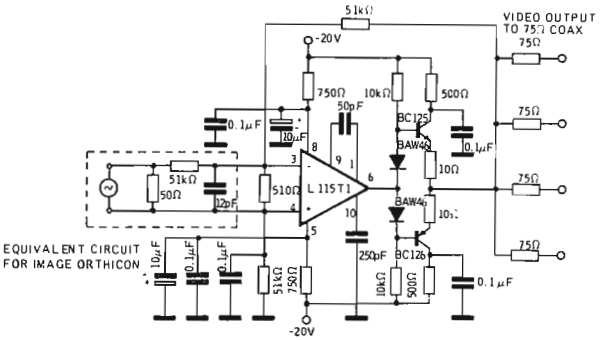
HIGH SPEED SAMPLE AND HOLD



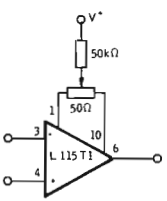
TYPICAL APPLICATIONS (contd)

WIDE BAND VIDEO AMPLIFIER WITH
75Ω COAX CABLE DRIVE CAPABILITY

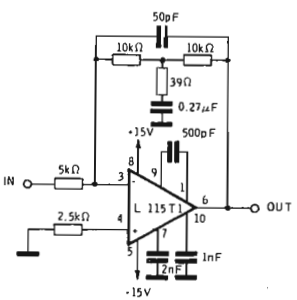


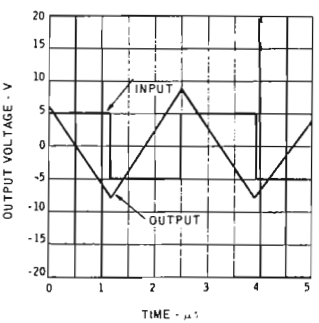


VOLTAGE OFFSET
NULL CIRCUIT



HIGH SPEED INTEGRATOR





DEFINITION OF TERMS

INPUT OFFSET VOLTAGE – That voltage which must be applied between the input terminals to obtain zero output voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT OFFSET CURRENT – The difference in the currents into the two input terminals with the output at zero volts.

INPUT RESISTANCE – The resistance looking into either input terminal with the other grounded.

INPUT BIAS CURRENT – The average of the two input currents.

INPUT VOLTAGE RANGE – The range of voltage which, if exceeded on either input terminal, could cause the amplifier to cease functioning properly.

INPUT COMMON MODE REJECTION RATIO – The ratio of the input voltage range to the maximum change in input offset voltage over this range.

SUPPLY VOLTAGE REJECTION RATIO – The ratio of the change in input offset voltage to the change in supply voltage producing it.

LARGE-SIGNAL VOLTAGE GAIN – The ratio of the maximum output voltage swing with load to the change in input voltage required to drive the output from zero to this voltage.

OUTPUT VOLTAGE SWING – The peak output swing, referred to zero, that can be obtained without clipping.

OUTPUT RESISTANCE – The resistance seen looking into the output terminal with the output at null. This parameter is defined only under small-signal conditions at frequencies above a few hundred cycles to eliminate the influence of drift and thermal feedback.

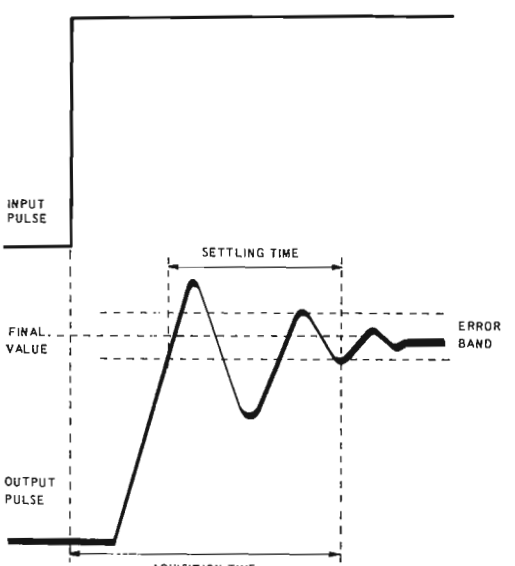
POWER CONSUMPTION – The DC power required to operate the amplifier with the output at zero and with no load current.

TRANSIENT RESPONSE – The closed-loop step-function response of the amplifier under small-signal conditions.

ACQUISITION TIME – The time from change of input until last time output exceeds specified percent of final value.

SLEW RATE – The maximum rate of change of output under large-signal conditions.

SETTLING TIME – The time from output first reaching final value until last time output exceeds specified percent of final value.



HELPFUL HINTS

LAYOUT – The layout should besuch that stray capacitance is minimal.

SUPPLIES – The supplies should be adequately bypassed. Use of 0.1 μF high quality ceramic capacitors is recommended.

RINGING – Excessive ringing (long acquisition time) may occur with large capacitive loads. This may be reduced by isolating the capacitive load with a resistance of 100 Ω. Large source resistances may also give rise to the same problem and this may be decreased by the addition of a capacitance across the feedback resistance. A value of around 50 pF for unity gain configuration and around 3 pF for gain 10 should be adequate.

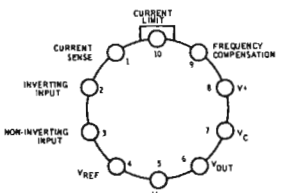
LATCH UP – This may occur when the amplifier is used as a voltage follower. The inclusion of a diode between pins 6 and 2 with the cathode towards pin 2 is the recommended preventive.

precision voltage regulator

EXTENDED TEMPERATURE RANGE -55°C to +125°C

- **Positive or negative supply operation**
- **Series, shunt, switching or floating operation**
- **.01% line and load regulation**
- **Output voltage adjustable from 2 to 37 volts**
- **Output current to 150 mA without external pass transistor**

CONNECTION DIAGRAM
Top view



NOTE : PIN 5 IS CONNECTED TO CASE

ORDERING NUMBER

L123T2

The L123 is a monolithic voltage regulator constructed on a single silicon chip using the Planar-epitaxial process. The device consists of a temperature compensated reference amplifier, error amplifier, power series pass transistor and current limit circuitry. Additional NPN or PNP pass elements may be used when output currents exceeding 150 mA are required. Provisions are made for adjustable current limiting and remote shutdown. In addition to the above, the device features low standby current drain, low temperature drift and high ripple rejection. The L123 is intended for use with positive or negative supplies as a series, shunt, switching or floating regulator. Applications include laboratory power supplies, isolation regulators for low level data amplifiers, logic card regulators, small instrument power supplies, airborne systems and other power supplies for digital and linear circuits.

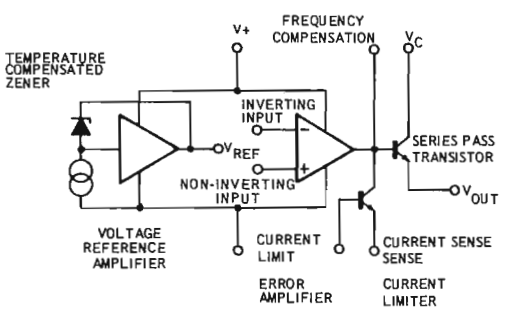
ABSOLUTE MAXIMUM RATINGS

(above which the useful life may be impaired)

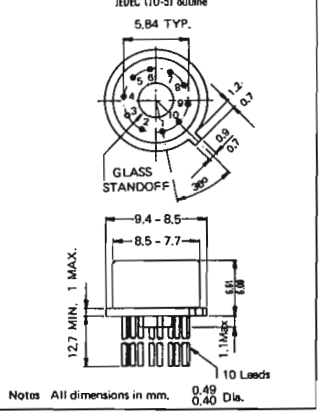
Pulse Voltage from V^+ to V^- (50 msec)	50V
Continuous Voltage from V^+ to V^-	40V
Input-Output Voltage Differential	40V
Maximum Output Current	150 mA
Current from V_{REF}	15 mA
Internal Power Dissipation (Note 1)	800 mW
Operating Temperature Range	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 60 sec.)	300°C

NOTES : On the following page.

EQUIVALENT CIRCUIT



PHYSICAL DIMENSIONS
similar to
JEDEC (TO-5) outline



ELECTRICAL CHARACTERISTICS (Note 2)

PARAMETER (see definitions)	CONDITIONS	Min.	Typ.	Max.	UNITS
Line Regulation	V_{IN} = 12 V to V_{IN} = 15 V		0.01	0.1	% V_{OUT}
	V_{IN} = 12 V to V_{IN} = 40 V		0.02	0.2	% V_{OUT}
	-55°C ≤ T_A ≤ +125°C, V_{IN} = 12 V to V_{IN} = 15V			0.3	% V_{OUT}
Load Regulation	I_L = 1 mA to I_L = 50 mA		0.03	0.15	% V_{OUT}
	55°C ≤ T_A ≤ +125°C, I_L = 1 mA to I_L = 50 mA			0.6	% V_{OUT}
Ripple Rejection	f = 50 Hz to 10 kHz, C_{REF} = 0		74		dB
	f = 50 Hz to 10 kHz, C_{REF} = 5 μF		86		dB
Average Temperature Coefficient of Output Voltage	-55°C ≤ T_A ≤ +125°C		0.002	0.015	%/°C
Short Circuit Current Limit	R_{SC} = 10 Ω, V_{OUT} = 0		65		mA
Reference Voltage		6.95	7.15	7.35	V
Output Noise Voltage	BW = 100 Hz to 10 kHz, C_{REF} = 0		20		μV_{rms}
	BW = 100 Hz to 10 kHz, C_{REF} = 5 μF		2.5		μV_{rms}
Long Term Stability			0.1		%/1000 hrs
Standby Current Drain	I_L = 0, V_{IN} = 30V		2.3	3.5	mA
Input Voltage Range		9.5		40	V
Output Voltage Range		2		37	V
Input-Output Voltage Differential		3		38	V

DEFINITION OF TERMS

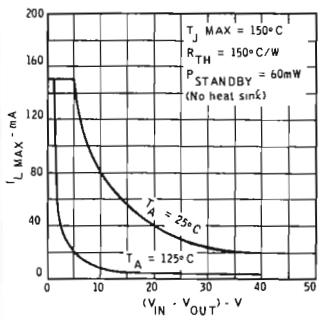
LINE REGULATION – The percentage change in output voltage for a specified change in input voltage.
LOAD REGULATION – The percentage change in output voltage for a specified change in load current.
RIPPLE REJECTION – The ratio of the peak to peak input ripple voltage to the peak to peak output ripple voltage.
AVERAGE TEMPERATURE COEFFICIENT OF OUTPUT VOLTAGE – The percentage change in output voltage for a specified change in ambient temperature.
SHORT CIRCUIT CURRENT LIMIT – The output current of the regulator with the output shorted to the negative supply.
REFERENCE VOLTAGE- The output of the reference amplifier measured with respect to the negative supply.
OUTPUT NOISE VOLTAGE – The rms output noise voltage with constant load and no input ripple.
STANDBY CURRENT DRAIN – The supply current drawn by the regulator with no output load and no reference voltage load.
INPUT VOLTAGE RANGE – The range of supply voltage over which the regulator will operate.
OUTPUT VOLTAGE RANGE – The range of output voltage over which the regulator will operate.
INPUT-OUTPUT VOLTAGE DIFFERENTIAL – The range of voltage difference between the supply voltage and the regulated output voltage over which the regulator will operata.
SENSE VOLTAGE – The voltage between current sense and current limit terminals necessary to cause current limiting.
TRANSIENT RESPONSE – The closed-loop step function response of the regulator under small-signal conditions.

NOTES :

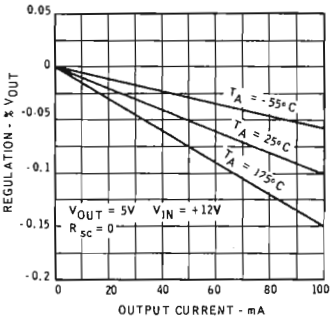
(1) Derate linearly at 6.4 mW/°C for operation at ambient temperatures above 25°C,
(2) Unless otherwise specified, T_A = 25°C, V_{IN} = V^+ = V_C = 12V, V^- = 0, V_{OUT} = 5V, I_L = 1 mA, R_{SC} = 0, C_1 = 100 pF C_{REF} = 0 and divider impedance as seen by error amplifier ≤ 10 KΩ connected as shown in Fig. 1.
(3) L_1 is 40 turns of # 20 enameled copper wire wound on Ferroxcube P36/22-3B7 pot core or equivalent with 0.009" air gap.
(4) Figures in parentheses may be used if R_1/R_2 divider is placed on opposite of error amp.
(5) Replace R_1/R_2 in figures with divider shown in figure 13.
(6) V^+ must be connected to a +3 V or greater supply.

ELECTRICAL CHARACTERISTICS (25° free air temperature unless otherwise noted)

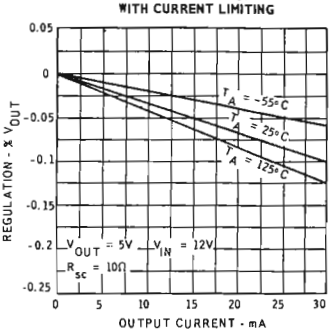
MAXIMUM LOAD CURRENT AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL



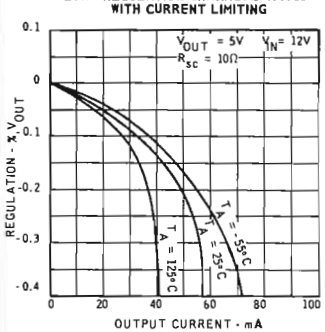
LOAD REGULATION CHARACTERISTICS WITHOUT CURRENT LIMITING



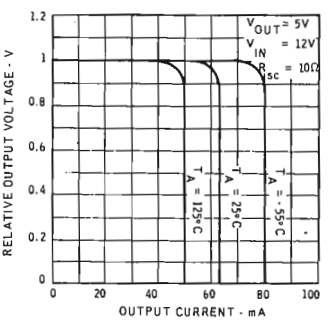
LOAD REGULATION CHARACTERISTICS WITH CURRENT LIMITING



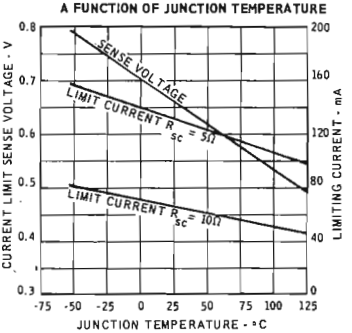
LOAD REGULATION CHARACTERISTICS WITH CURRENT LIMITING



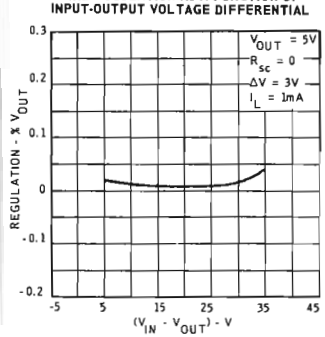
CURRENT LIMITING CHARACTERISTICS



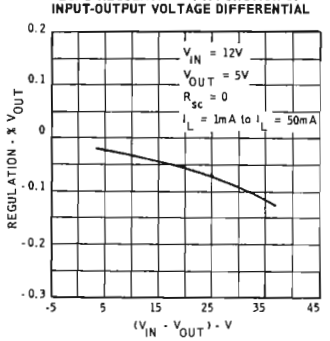
CURRENT LIMITING CHARACTERISTICS AS A FUNCTION OF JUNCTION TEMPERATURE



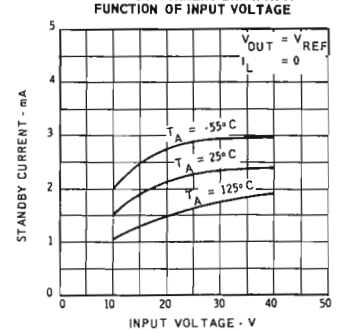
LINE REGULATION AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL



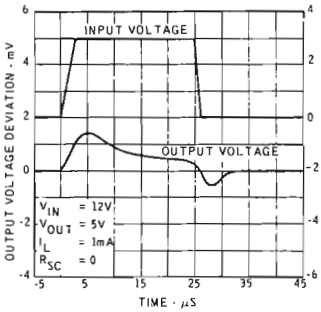
LOAD REGULATION AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL



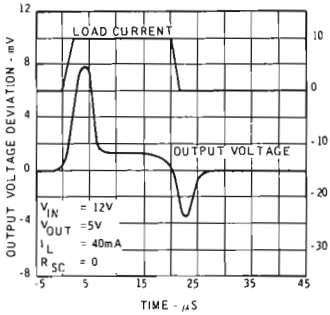
STANDBY CURRENT DRAIN AS A FUNCTION OF INPUT VOLTAGE



LINE TRANSIENT RESPONSE



LOAD TRANSIENT RESPONSE



OUTPUT IMPEDANCE AS A FUNCTION OF FREQUENCY

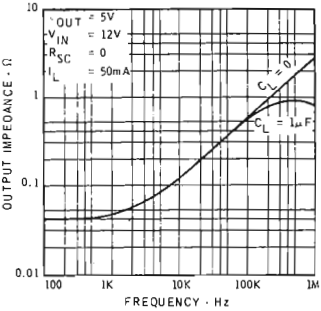


TABLE I

RESISTOR VALUES (kΩ) for standard output voltages

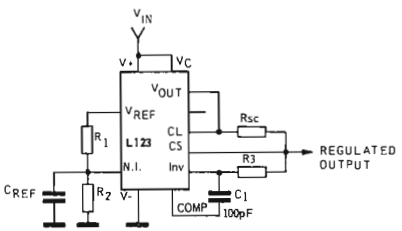
Positive Output Voltage	Applicable Figures	Fixed output ± 5%		Output adjustable ± 10% (Note 5)			Negative Output Voltage	Applicable Figures	Fixed output ± 5%		5% Output adjustable ± 10%		
	(Note 4)	R_1	R_2	R_1	P_1	R_2			R_1	R_2	R_1	P_1	R_2
+ 3	1, 5, 6, 9, 12 (4)	4.12	3.01	1.8	0.5	1.2	+100	7	3.57	102	2.2	10	91
+3.6	1, 5, 6, 9, 12 (4)	3.57	3.65	1.5	0.5	1.5	+250	7	3.57	255	2.2	10	240
+5	1, 5, 6, 9, 12 (4)	2.15	4.99	0.75	0.5	2.2	- 6 (note 6)	3, (10)	3.57	2.43	1.2	0.5	0.75
+6	1, 5, 6, 9, 12 (4)	1.15	6.04	0.5	0.5	2.7	-9	3, 10	3.48	5.36	1.2	0.5	2
+9	2, 4, (5, 6, 12, 9)	1.87	7.15	0.75	1	2.7	-12	3, 10	3.57	8.45	1.2	0.5	3.3
+12	2, 4, (5, 6, 9, 12)	4.87	7.15	2	1	3	-15	3, 10	3.65	11.5	1.2	0.5	4.3
+15	2, 4, (5, 6, 9, 12)	7.87	7.15	3.3	1	3	-28	3, 10	3.57	24.3	1.2	0.5	10
+28	2, 4, (5, 6, 9, 12)	21	7.15	5.6	1	2	-45	8	3.57	41.2	2.2	10	33
+45	7	3.57	48.7	2.2	10	39	-100	8	3.57	97.6	2.2	10	91
+ 75	7	3.57	78.7	2.2	10	68	-250	8	3.57	249	2.2	10	240

TABLE II

FORMULAE FOR INTERMEDIATE OUTPUT VOLTAGES

Outputs from +2 to +7 volts [Figures 1, 5, 6, 9, 12, (4)] $V_{OUT} = [V_{REF} \times \frac{R_2}{R_1 + R_2}]$	Outputs from +4 to +250 volts [Figure 7] $V_{OUT} = [\frac{V_{REF}}{2} \times \frac{R_2 - R_1}{R_1}]$; $R_3 = R_4$	Current Limiting $I_{LIMIT} = \frac{V_{SENSE}}{R_{SC}}$
Outputs from +7 to +37 volts [Figures 2, 4, (5, 6, 9, 12)] $V_{OUT} = [V_{REF} \times \frac{R_1 + R_2}{R_2}]$	Outputs from −6 to −250 volts [Figures 3, 8, 10] $V_{OUT} = [\frac{V_{REF}}{2} \times \frac{R_1 + R_2}{R_1}]$; $R_3 = R_4$	Foldback Current Limiting $I_{KNEE} = [\frac{V_{OUT} R_3}{R_{SC} R_4} + \frac{V_{SENSE}(R_3 + R_4)}{R_{SC} R_4}]$ $I_{SHORT\ CKT} = [\frac{V_{SENSE}}{R_{SC}} \times \frac{R_3 + R_4}{R_4}]$

BASIC LOW VOLTAGE REGULATOR FIG. 1
(V_{OUT} = 2 to 7 Volts)

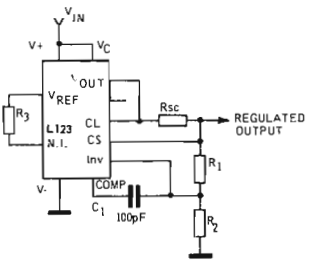


Note: $R3 = \frac{R1\,R2}{R1+R2}$ for minimum temperature drift.

TYPICAL PERFORMANCE

Regulated Output Voltage	5V
Line Regulation (ΔV_{IN} = 3V)	0.5 mV
Load Regulation (ΔI_L = 50mA)	1.5 mV

BASIC HIGH VOLTAGE REGULATOR FIG. 2
(V_{OUT} = 7 to 37 Volts)



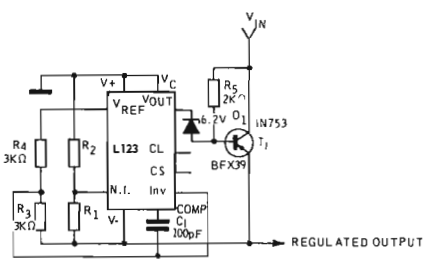
Note: $R3 = \frac{R1\,R2}{R1+R2}$ for minimum temperature drift

R3 may be eliminated for minimum component count.

TYPICAL PERFORMANCE

Regulated Output Voltage	15V
Line Regulation (ΔV_{IN} = 3V)	1.5 mV
Load Regulation (ΔI_L = 50mA)	4.5 mV

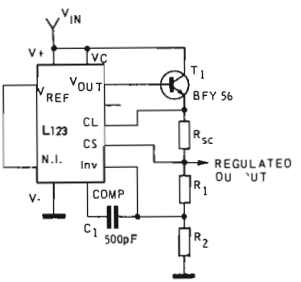
NEGATIVE VOLTAGE REGULATOR FIG. 3



TYPICAL PERFORMANCE

Regulated Output Voltage	-15 V
Line Regulation (ΔV_{IN} = 3V)	1 mV
Load Regulation (ΔI_L = 100mA)	2 mV

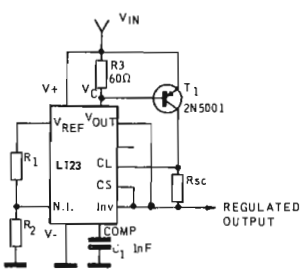
POSITIVE VOLTAGE REGULATOR FIG. 4
(External NPN Pass Transistor)



TYPICAL PERFORMANCE

Regulated Output Voltage	+ 15 V
Line Regulation (ΔV_{IN} = 3V)	1.5 mV
Load Regulation (ΔI_L = 1A)	15 mV

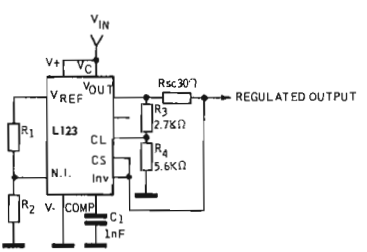
POSITIVE VOLTAGE REGULATOR FIG. 5
(External PNP Pass Transistor)



TYPICAL PERFORMANCE

Regulated Output Voltage	+ 5 V
Line Regulation (ΔV_{IN} = 3V)	0.5mV
Load Regulation (ΔI_L = 1A)	5mV

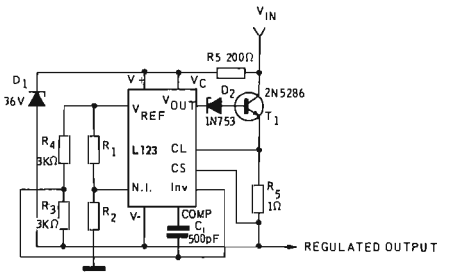
FOLDBACK CURRENT LIMITING FIG. 6



TYPICAL PERFORMANCE

Regulated Output Voltage	+5V
Line Regulation (ΔV_{IN} = 3V)	0.5mV
Load Regulation (ΔI_L = 10mA)	1mV
Current Limit Knee	20mA

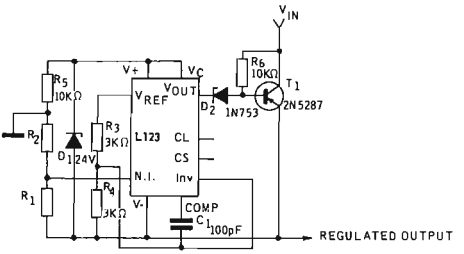
POSITIVE FLOATING REGULATOR FIG. 7



TYPICAL PERFORMANCE

Regulated Output Voltage	+ 50 V
Line Regulation (ΔV_{IN} = 20V)	15 mV
Load Regulation (ΔI_L = 50mA)	20 mV

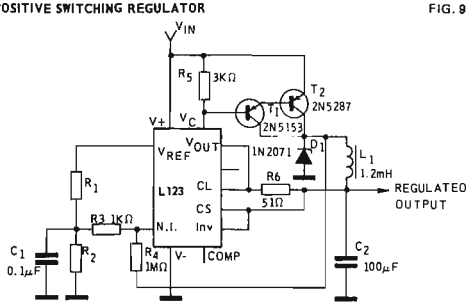
NEGATIVE FLOATING REGULATOR FIG. 8



TYPICAL PERFORMANCE

Regulated Output Voltage	-100V
Line Regulation (ΔV_{IN} = 20V)	30mV
Load Regulation (ΔI_L = 100mA)	20mV

POSITIVE SWITCHING REGULATOR FIG. 9

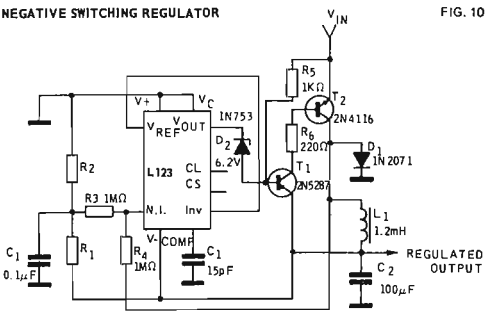


NOTE 3

TYPICAL PERFORMANCE

Regulated Output Voltage	+5 V
Line Regulation (ΔV_{IN} = 30V)	10 mV
Load Regulation (ΔI_L = 2A)	80 mV

NEGATIVE SWITCHING REGULATOR FIG. 10

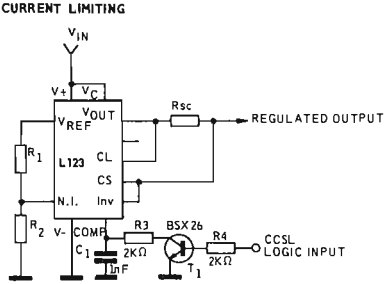


NOTE 3

TYPICAL PERFORMANCE

Regulated Output Voltage	- 15 V
Line Regulation (ΔV_{IN} = 20V)	8 mV
Load Regulation (ΔI_L = 2A)	6 mV

REMOTE SHUTDOWN REGULATOR WITH CURRENT LIMITING FIG. 11

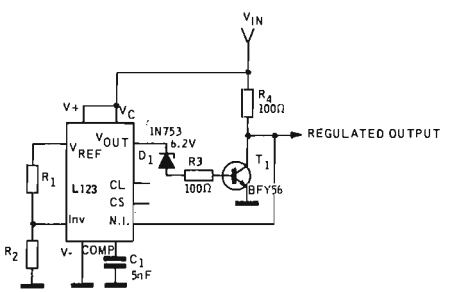


Note :
Current limit transistor may be used for shutdown if current limiting is not required.

TYPICAL PERFORMANCE

Regulated Output Voltage	+ 5 V
Line Regulation (ΔV_{IN} = 3V)	0.5 mV
Load Regulation (ΔI_L = 50mA)	1.5 mV

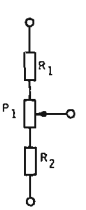
SHUNT REGULATOR FIG. 12



TYPICAL PERFORMANCE

Regulated Output Voltage	+ 5 V
Line Regulation (ΔV_{IN} = 10V)	0.5 mV
Load Regulation (ΔI_L = 100mA)	1.5 mV

OUTPUT VOLTAGE ADJUST FIG. 13



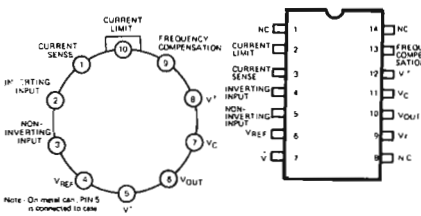
precision voltage regulator

STANDARD TEMPERATURE RANGE, 0°C ÷ 70°C

- Positive or negative supply operation
- Series, shunt, switching or floating operation
- .01 % line and load regulation
- Output voltage adjustable from 2 to 37 volts
- Output current to 150 mA without external pass transistor

The L 123 is a monolithic voltage regulator constructed on a single silicon chip using the Planar epitaxial process. The device consists of a temperature compensated reference amplifier, error amplifier, power series pass transistor and current limit circuitry. Additional NPN or PNP pass elements may be used when output currents exceeding 150 mA are required. Provisions are made for adjustable current limiting and remote shutdown. In addition to the above, the device features low standby current drain, low temperature drift and high ripple rejection. The L 123 is intended for use with positive or negative supplies as a series, shunt, switching or floating regulator. Applications include laboratory power supplies, isolation regulators for low level data amplifiers, logic card regulators, small instrument power supplies, airborne systems and in other power supplies for digital and linear circuits.

CONNECTION DIAGRAM
TOP VIEW



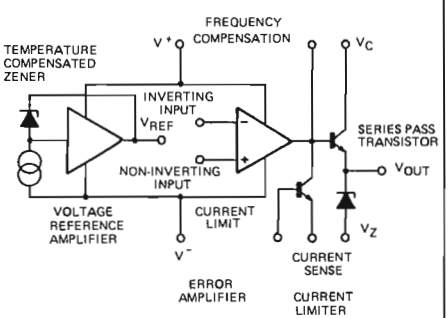
ABSOLUTE MAXIMUM RATINGS (1)

(T_A = 25° C unless otherwise noted)

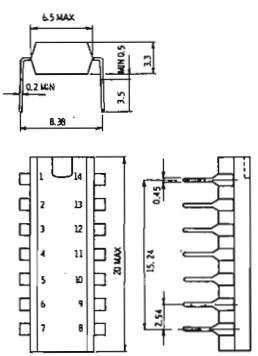
Voltage from V^+ to V^-	40 V
Input-Output Voltage Differential	40 V
Maximum Output Current	150 mA
Current from V_{REF}	25 mA
Internal Power Dissipation (1)	800 mW
Operating Temperature Range	0°C to + 70° C
Storage Temperature Range (Metal Can)	- 65° C to + 150° C
Storage Temperature Range (DIP)	- 55°C to + 125° C
Lead Temperature (Soldering, 60 sec.)	300° C

NOTE ON PAGE 2

EQUIVALENT CIRCUIT

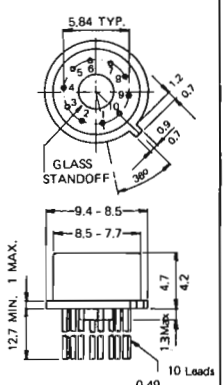


PHYSICAL DIMENSIONS
14-pin plastic DIP



Note : all dimensions in mm.

PHYSICAL DIMENSIONS
similar to
Jedec TO 100 outline



Notes All dimensions in mm.
Leads are gold-plated Kovar.

ORDERING NUMBER

L123 B1 (for TO 116 package)
L123 T1 (for TO 5 package)

ELECTRICAL CHARACTERISTICS (note 2)

PARAMETER (see definitions)	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Line Regulation	V = 12 V to V = 15 V		0.01	0.1	% V_{OUT}
	V_{IN}=12 V to V_{IN} = 40 V		0.1	0.5	% V_{OUT}
	0°C ≤ T_A ≤ 70°C, V_{IN}= 12V to V_{IN}= 15V			0.3	% V_{OUT}
Load Regulation	I_L = 1 mA to I_L = 50 mA		0.03	0.2	% V_{OUT}
	0°C ≤ T_A ≤ 70°C, I_L = 1 mA to I_L = 50 mA			0.6	% V_{OUT}
Ripple Rejection	f = 50 Hz to 10 kHz, C_{REF} = 0		74		dB
	f = 50 Hz to 10 kHz, C_{REF} = 5 μF		86		dB
Average Temperature Coefficient of Output Voltage	0°C ≤ T_A ≤ 70°C		0.003	0.015	%/°C
Short Circuit Current Limit	R_{SC} = 10 Ω, V_{OUT} = 0		65		mA
Reference Voltage		6.80	7.15	7.50	V
Output Noise Voltage	BW = 100 Hz to 10 kHz, C_{REF} = 0		20		μV_{rms}
	BW = 100 Hz to 10 kHz, C_{REF} = 5 μF		2.5		μV_{rms}
Long Term Stability			0.1		%/1000 hrs
Standby Current Drain	I_L = 0, V_{IN} = 30 V		2.3	4	mA
Input Voltage Range		9.5		40	V
Output Voltage Range		2		37	V
Input-Output Voltage Differential		3		38	V

DEFINITION OF TERMS

LINE REGULATION - The percentage change in output voltage for a specified change in input voltage.

LOAD REGULATION- The percentage change in output voltage for a specified change in load current.

RIPPLE REJECTION - The ratio of the peak to peak input ripple voltage to the peak to peak output ripple voltage.

AVERAGE TEMPERATURE COEFFICIENT OF OUTPUT VOLTAGE - The percentage change in output voltage for a specified change in ambient temperature.

SHORT CIRCUIT CURRENT LIMIT - The output current of the regulator with the output shorted to the negative supply.

REFERENCE VOLTAGE - The output of the reference amplifier measured with respect to tha negative supply.

OUTPUT NOISE VOLTAGE - The rms output noise voltage with constant load and no input ripple.

STANDBY CURRENT DRAIN - The supply current drawn by the regulator with no output load and no reference voltage load.

INPUT VOLTAGE RANGE - The range of supply voltage over which the regulator will operate.

OUTPUT VOLTAGE RANGE - The range of output voltage over which the regulator will operate.

INPUT-OUTPUT VOLTAGE DIFFERENTIAL - The range of voltage difference between the supply voltage and the regulated output voltage over which the regulator will operate.

SENSE VOLTAGE - The voltage between current sense and current limit terminals necessary to cause current limiting.

TRANSIENT RESPONSE - The closed-loop step function response of the regulator under small-signal conditions.

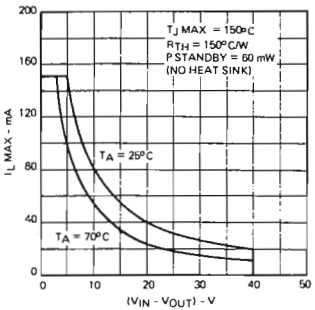
NOTES:

(1) Derate metal can package at 6.4 mW/°C and dual in-line package at 8 mW/°C for operation at ambient temperatures above 25°C.
(2) Unless otherwise specified, T_A = 25°C, V_{IN} = V_+ = V_C = 12 V, V_- = 0, V_{OUT} = 5 V, I_L = 1 mA, R_{SC} = 0, C_I = 100 pF and divider impedance as seen by the error amplifier ≤ 10 KΩ
(3) For metal can applications where V_Z is required, an external 6.2 zener should be connected in series with V_{OUT}.
(4) Figures in parentheses may be used if R_1/R_2 divider is placed on opposite of error amp.
(5) Replace R_1/R_2 in figures with divider shown in figure 13.
(6) V_+ and V_C must be connected to a + 3 V or greater supply.
(7) L_1 is 40 turns of # 20 enameled copper wire wound on Ferroxcube P36/22-3B7 pot core or equivalent with 0,23 mm. air gap.

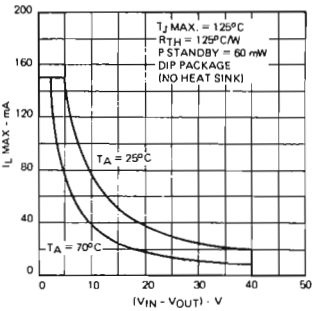
STANDARD TEMPERATURE RANGE

TYPICAL ELECTRICAL CHARACTERISTICS (25°C free air temperature unless otherwise noted)

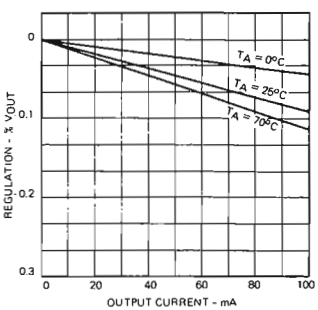
MAXIMUM LOAD CURRENT AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL



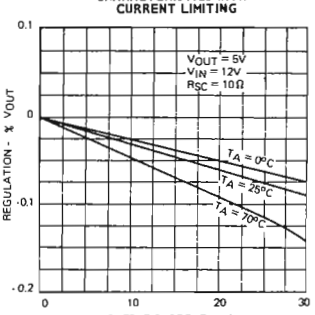
MAXIMUM LOAD CURRENT AS A FUNCTION OF INPUT - OUTPUT VOLTAGE DIFFERENTIAL



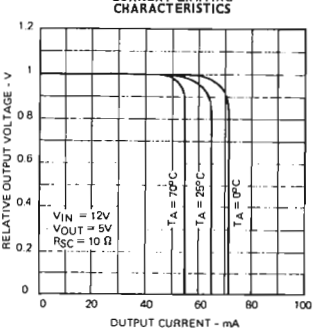
LOAD REGULATION CHARACTERISTICS WITHOUT CURRENT LIMITING



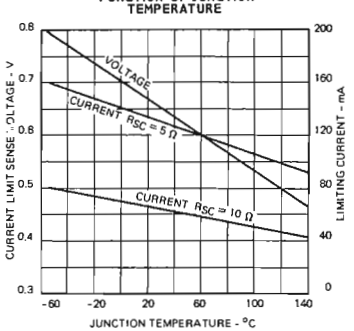
LOAD REGULATION CHARACTERISTICS WITH CURRENT LIMITING



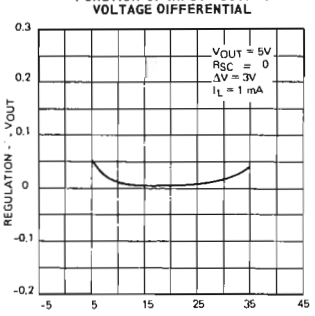
CURRENT LIMITING CHARACTERISTICS



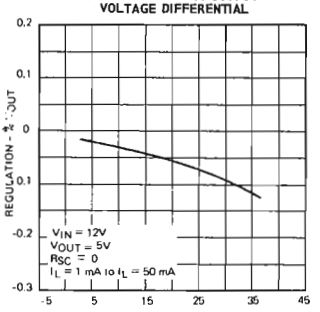
CURRENT LIMITING CHARACTERISTICS AS A FUNCTION OF JUNCTION TEMPERATURE



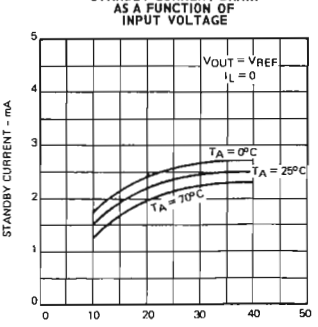
LINE REGULATION AS A FUNCTION OF INPUT - OUTPUT VOLTAGE DIFFERENTIAL



LOAD REGULATION AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL



STANDBY CURRENT DRAIN AS A FUNCTION OF INPUT VOLTAGE



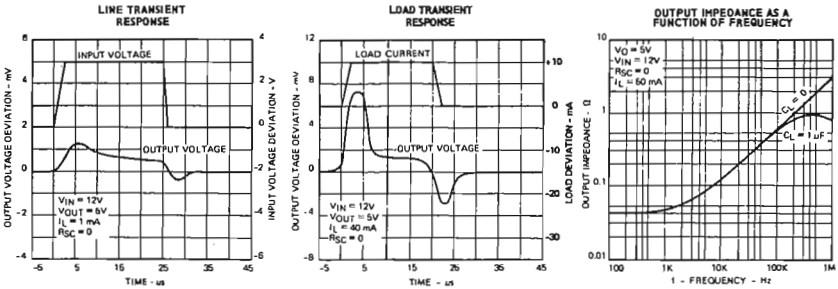


TABLE I
RESISTOR VALUES (KΩ) FOR STANDARD OUTPUT VOLTAGES

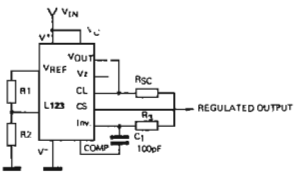
POSITIVE OUTPUT VOLTAGE	APPLICABLE FIGURES	FIXED OUTPUT ±5 %		OUTPUT ADJUSTABLE ± 10%(Note 5)			NEGATIVE OUTPUT VOLTAGE	APPLICABLE FIGURES	FIXED OUTPUT ±5 %		5% OUTPUT ADJUSTABLE ± 10%		
	(Note 4)	R_1	R_2	R_1	P_1	R_2			R_1	R_2	R_1	P_1	R_2
+ 3	1, 5, 6, 9 12 (4)	4.12	3.01	1.8	0.5	1.2	+ 100	7	3.57	102	2.2	10	91
+ 3.6	1, 5, 6, 9, 12 (4)	3.57	3.65	1.5	0.5	1.5	+250	7	3.57	255	2.2	10	240
+ 5	1, 5, 6, 9, 12 (4)	2.15	4.99	0.75	0.5	2.2	- 6 (note 6)	3, (10)	3.57	2.43	1.2	0.5	0.75
+ 6	1, 5, 6, 9, 12 (4)	1.15	6.04	0.5	0.5	2.7	- 9	3, 10	3.48	6.36	1.2	0.5	2
+ 9	2, 4, (5,6, 12, 9)	1.87	7.15	0.75	1	2.7	- 12	3, 10	3.57	8.45	1.2	0.5	3.3
+ 12	2, 4, (5,6, 9, 12)	4.87	7.15	2	1	3	- 15	3, 10	3.65	11.5	1.2	0.5	4.3
+ 15	2,4, (5, 6, 9, 12)	7.87	7.15	3.3	1	3	- 28	3, 10	3.57	24.3	1.2	0.5	10
+28	2, 4, (5, 6, 9, 12)	21	7.15	5.6	1	2	- 45	8	3.57	41.2	2.2	10	33
+45	7	3.57	48.7	2.2	10	39	- 100	8	3.57	97.6	2.2	10	91
+75	7	3.57	78.7	2.2	10	68	- 250	8	3.57	249	2.2	10	240

TABLE II
FORMULAE FOR INTERMEDIATE OUTPUT VOLTAGES

Outputs from +2 to +7 volts [Figures 1, 5, 6, 9, 12, (4)] $V_{OUT} = [V_{REF} \times \frac{R_2}{R_1 + R_2}]$	Outputs from +4 to +250 volts [Figure 7] $V_{OUT} = [\frac{V_{REF}}{2} \times \frac{R_2 - R_1}{R_1}]$; $R_3 = R_4$	Current Limiting $I_{LIMIT} = \frac{V_{SENSE}}{R_{sc}}$
Outputs from +7 to +37 volts [Figures 2, 4, (5, 6, 9, 12)] $V_{OUT} = [V_{REF} \times \frac{R_1 + R_2}{R_2}]$	Outputs from —6 to —250 volts [Figures 3, 8, 10] $V_{OUT} = [\frac{V_{REF}}{2} \times \frac{R_1 + R_2}{R_1}]$; $R_3 = R_4$	Foldback Current Limiting $I_{KNEE} = [\frac{V_{OUT} R_3}{R_{sc} R_4} + \frac{V_{SENSE}(R_3 + R_4)}{R_{sc} R_4}]$ $I_{SHORT\ CKT} = [\frac{V_{SENSE}}{R_{sc}} \times \frac{R_3 + R_4}{R_4}]$

BASIC LOW VOLTAGE REGULATOR FIG. 1

(V_{OUT} = 2 to 7 V)



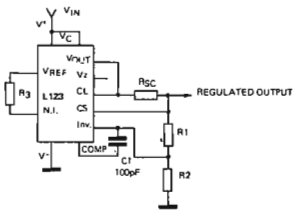
NOTE: R3 = $\frac{R1 \cdot R2}{R1+R2}$ for minimum temperature drift.
R3 may be eliminated for minimum component count.

TYPICAL PERFORMANCE

Regulated output Voltage	5 V
Line Regulation (ΔV_{IN} = 3 V)	0.5mV
Load Regulation (ΔI_L = 50mA)	1.5mV

BASIC HIGH VOLTAGE REGULATOR FIG. 2

(V_{OUT} = 7 to 37 V)

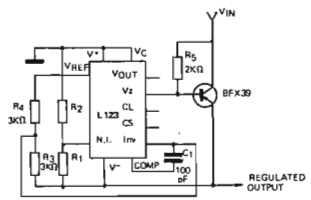


NOTE: R3 = $\frac{R1 \cdot R2}{R1+R2}$ for minimum temperature drift.
R3 may be eliminated for minimum component count.

TYPICAL PERFORMANCE

Regulated Ouput Voltage	15 V
Line Regulation (ΔV_{IN} = 3 V)	1.5mV
Load Regulation (ΔI_L = 50mA)	4.5mV

NEGATIVE VOLTAGE REGULATOR FIG. 3



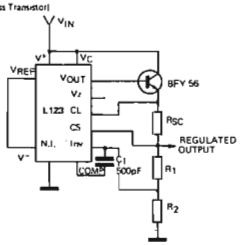
TYPICAL PERFORMANCE

Regulated Output Voltage	15 V
Line Regulation (ΔV_{IN} = 3 V)	1mV
Load Regulation (ΔI_L = 100mA)	2mV

NOTE 3

POSITIVE VOLTAGE REGULATOR FIG. 4

(External NPN Pass Transistor)

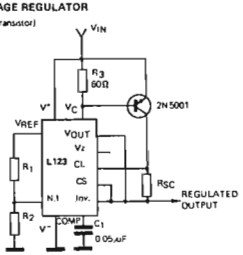


TYPICAL PERFORMANCE

Regulated Output Voltage	+ 15 V
Line Regulation (ΔV_{IN} = 3 V)	1.5mV
Load Regulation (ΔI_L = 1 A)	15mV

POSITIVE VOLTAGE REGULATOR FIG. 5

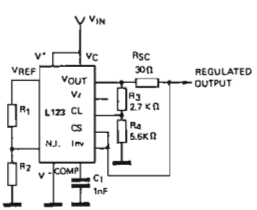
(External PNP Pass Transistor)



TYPICAL PERFORMANCE

Regulated Output Voltage	+ 5 V
Line Regulation (ΔV_{IN} = 3 V)	0.5mV
Load Regulation (ΔI_L = 1 A)	5mV

FOLDBACK CURRENT LIMITING FIG. 6

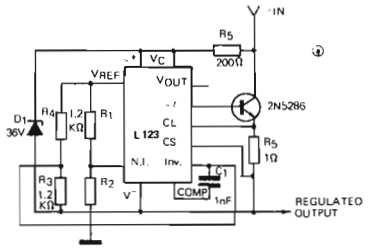


TYPICAL PERFORMANCE

Regulated Output Voltage	+ 5 V
Line Regulation (ΔV_{IN} = 3 V)	0.5mV
Load Regulation (ΔI_L = 10mA)	1mV
Current Limit Knee	20mA

POSITIVE FLOATING REGULATOR

FIG. 7



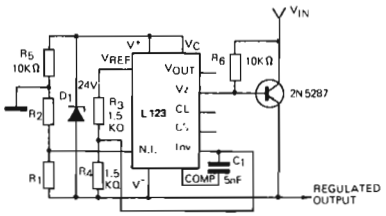
TYPICAL PERFORMANCE

Regulated Output Voltage	+ 100 V
Line Regulation (ΔV_{IN} = 20V)	15mV
Load Regulation (ΔI_L = 50mA)	20mV

NOTE 3

NEGATIVE FLOATING REGULATOR

FIG. 8



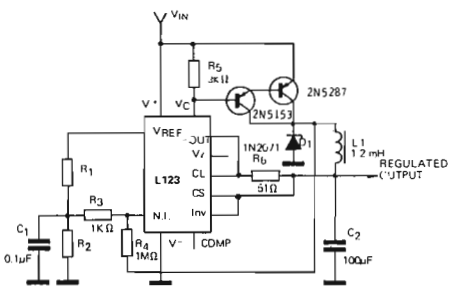
TYPICAL PERFORMANCE

Regulated Output Voltage	- 100 V
Line Regulation (ΔV_{IN} = 20V)	30mV
Load Regulation (ΔI_L = 100mA)	20mV

NOTE 3

POSITIVE SWITCHING REGULATOR

FIG. 9



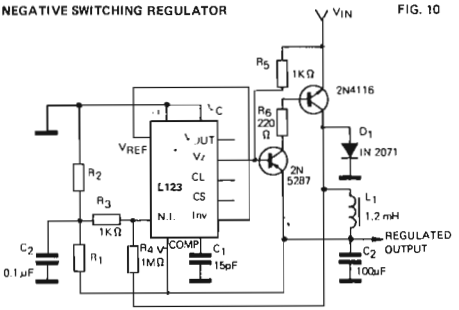
TYPICAL PERFORMANCE

Regulated Output Voltage	+ 5 V
Line Regulation (ΔV_{IN} = 30V)	10mV
Load Regulation (ΔI_L = 2A)	80mV

NOTE 7

NEGATIVE SWITCHING REGULATOR

FIG. 10



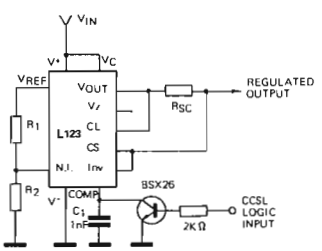
TYPICAL PERFORMANCE

Regulated Output Voltage	- 15 V
Line Regulation (ΔV_{IN} = 20V)	8mV
Load Regulation (ΔI_L = 2A)	6mV

NOTE 3
NOTE 7

REMOTE SHUTDOWN REGULATOR WITH CURRENT LIMITING

FIG. 11



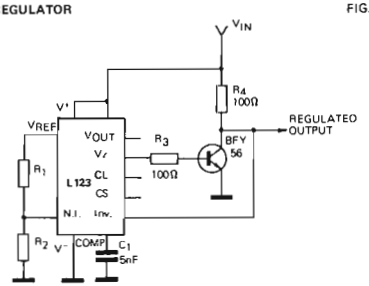
NOTE: Current limit transistor may be used for shutdown if current limiting is not required.

TYPICAL PERFORMANCE

Regulated Output Voltage	5 V
Line Regulation (ΔV_{IN} = 3V)	0.5mV
Load Regulation (ΔI_L = 50mA)	1.5mV

SHUNT REGULATOR

FIG. 12



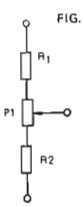
TYPICAL PERFORMANCE

Regulated Output Voltage	+ 5 V
Line Regulation (ΔV_{IN} = 10V)	2mV
Load Regulation (ΔI_L = 100mA)	5mV

NOTE 3

OUTPUT VOLTAGE ADJUST

FIG. 13



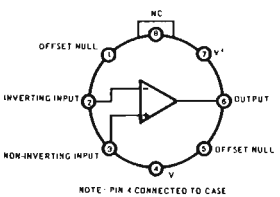
high performance operational amplifier

EXTENDED TEMPERATURE RANGE, - 55°C ÷ 125°C

- No frequency compensation required
- Short-circuit protection
- Offset voltage null capability
- Large common-mode and differential voltage ranges
- Low power consumption
- No latch up

The L 141 is a high performance monolithic operational amplifier constructed on a single silicon chip, using the Planar epitaxial process. It is intended for a wide range of analog applications. High common mode voltage range and absence of "latch-up" tendencies make the L 141 ideal for use as a voltage follower. The high gain and wide range of operating voltages provide superior performance in integrator, summing amplifier, and general feedback applications. The L141 is short-circuit protected, has the same pin configuration as the popular μA709 operational amplifier, but requires no external components for frequency compensation. The internal 6dB/octave roll-off insures stability in closed loop applications.

CONNECTION DIAGRAM
(Top view)

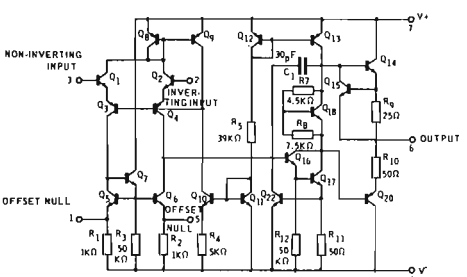


ABSOLUTE MAXIMUM RATINGS
(above which the useful life may be impaired)

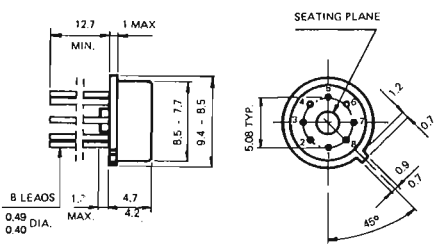
Supply Voltage	± 22 V
Internal Power Dissipation (1)	500 mW
Differential Input Voltage	± 30 V
Input Voltage (2)	± 15 V
Storage Temperature Range	- 65°C to + 150°C
Operating Temperature Range	- 55°C to + 125°C
Lead Temperature (Soldering, 60 sec.)	300°C
Output Short-Circuit Duration (3)	Indefinite

Notes :
1) Rating applies for case temperatures to 125°C; derate linearly at 6.5 mW/°C for ambient temperaturesabove + 75°C.
2) For supply voltages less than ± 15 V, the absolute maximum input voltage is equal to tha supply voltage.
3) Short circuit may be to ground or either supply. Rating applies to + 125°C case temperature or + 75°C ambient temperature.

SCHEMATIC DIAGRAM



PHYSICAL DIMENSIONS
in accordance with
JEDEC TO-99 outline



Notes: All dimensions in mm.

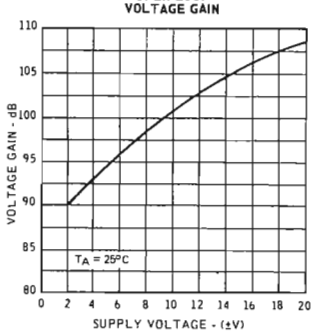
ORDERING NUMBER

L141 T2

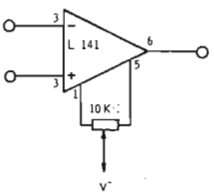
ELECTRICAL CHARACTERISTICS ($V_S = \pm 15V$, $T_A = 25°C$ unless otherwise specified)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input Offset Voltage	$R_S \leq 10\,k\Omega$		1	5	mV
Input Offset Current			30	200	nA
Input Bias Current			200	500	nA
Input Resistance		0.3	1		MΩ
Large-Signal Voltage Gain	$R_L \geq 2\,k\Omega$, $V_{OUT} = \pm 10V$	50.000	200.000		
Output Voltage Swing	$R_L \geq 10\,k\Omega$	± 12	± 14		V
	$R_L \geq 2\,k\Omega$	± 10	± 13		V
Input Voltage Range		± 12	± 13		V
Common Mode Rejection Ratio	$R_S \leq 10\,k\Omega$	70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10\,k\Omega$		30	150	µV/V
Power Consumption			50	85	mW
Transient Response (unity gain)	$V_{in} = 20$ mV, $R_L = 2$ kΩ, $C_L \leq 100$ pF				
Risetime			0.3		µs
Overshoot			5		%
Slew Rate (unity gain)	$R_L \geq 2\,k\Omega$		0.5		V/µs
The following specifications apply for $-55°C \leq T_A \leq +125°C$:					
Input Offset Voltage	$R_S \leq 10\,k\Omega$			6	mV
Input Offset Current				500	nA
Input Bias Current				1.5	µA
Large-Signal Voltage Gain	$R_L \geq 2\,k\Omega$ $V_{OUT} = \pm 10V$	25.000			
Output Voltage Swing	$R_L \geq 2\,k\Omega$	± 10			V

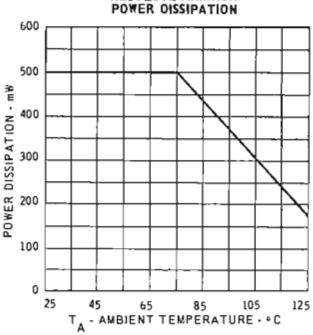
OPEN LOOP VOLTAGE GAIN



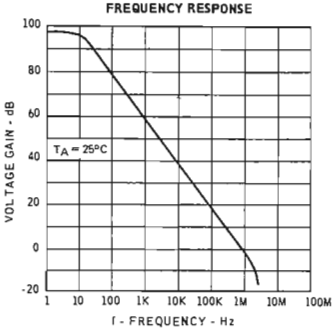
VOLTAGE OFFSET NULL CIRCUIT



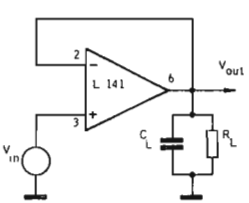
ABSOLUTE MAXIMUM POWER DISSIPATION



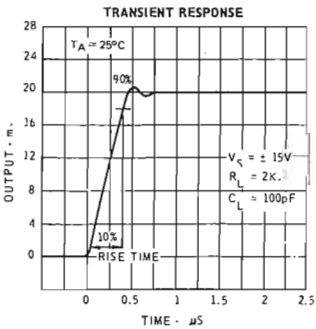
OPEN LOOP FREQUENCY RESPONSE



TRANSIENT RESPONSE TEST CIRCUIT



TRANSIENT RESPONSE



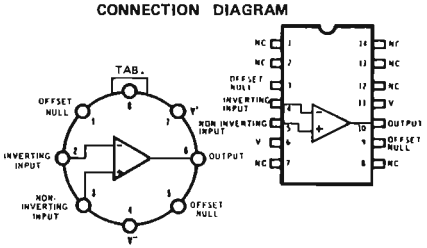
high performance operational amplifier

STANDARD TEMPERATURE RANGE, 0°C + 70°C

- No frequency compensation required
- Short-circuit protection
- Offset voltage null capability
- Large Common-Mode and differential voltage ranges
- Low power consumption
- No latch up

The L 141 is a high performance monolithic operational amplifier constructed on a single silicon chip, using the Planar epitaxial process. It is intended for a wide range of analog applications. High common mode voltage range and absence of "latch-up" tendencies make the L 141 ideal for use as a voltage follower. The high gain and wide range of operating voltages provide superior performance in integrator, summing amplifier, and general feedback applications. The L 141 is short-circuit protected, has the same pin configuration as the popular μA709 operational amplifier, but requires no external components for frequency compensation. The internal 6dB/octave roll-off insures stability in closed loop applications.

CONNECTION DIAGRAM



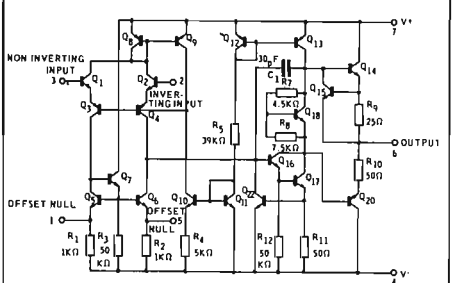
(top view)

ABSOLUTE MAXIMUM RATINGS
(above which the useful life may be impaired)

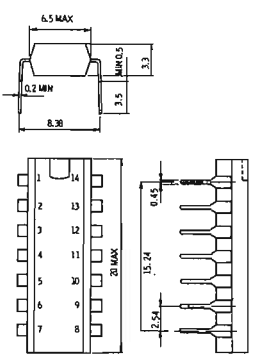
Supply Voltage	± 18 V
Internal Power Dissipation	500 mW
Differential Input Voltage	± 30 V
Input Voltage (1)	± 15 V
Storage Temperature Range	- 65°C to + 150°C
Operating Temperature Range	0°C to + 70°C
Lead Temperature (Soldering, 60 sec)	300°C
Output Short-Circuit Duration (2)	Indefinite

Notes :
1) For supply voltages less than ± 15V, the absolute maximum input voltage is equal to the supply voltage.
2) Short circuit may be to ground or either supply.

SCHEMATIC DIAGRAM

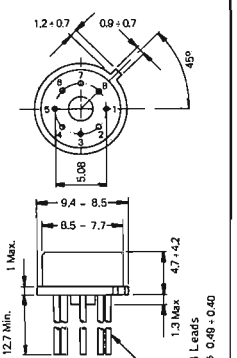


PHYSICAL DIMENSIONS
14-pin plastic DIP



Note : all dimensions in mm.

PHYSICAL DIMENSIONS
similar to
Jedec TO 99 outline



Notes : All dimensions in mm.

ORDERING NUMBER

L141 B1 (for TO116 package)
L141 T1 (for TO 99 package)

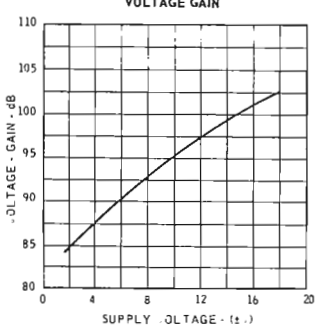
MAY 1969

ELECTRICAL CHARACTERISTICS ($V_S = \pm 15$ V, $T_A = 25°C$ unless otherwise specified)

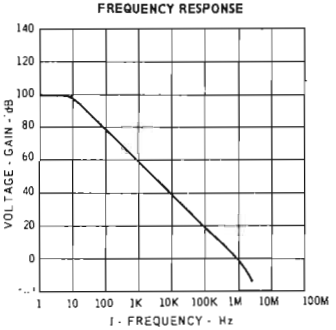
PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input Offset Voltage	$R_S \leq 10\,k\Omega$		2	6	mV
Input Offset Current			30	200	nA
Input Bias Current			200	500	nA
Input Resistance		0.3	1		MΩ
Large-Signal Voltage Gain	$R_L \geq 2\,k\Omega$, $V_{OUT} = \pm 10$ V	20.000	100.000		
Output Voltage Swing	$R_L \geq 10\,k\Omega$	±12	±14		V
	$R_L \geq 2\,k\Omega$	±10	±13		V
Input Voltage Range		±12	±13		V
Common Mode Rejection Ratio	$R_S \leq 10\,k\Omega$	70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10\,k\Omega$		30	150	µV/V
Power Consumption			50	85	mW
Transient Response (unity gain)	$V_{in} = 20$ mV, $R_L = 2\,k\Omega$ $C_L \leq 100$ pF				
Risetime			0.3		µs
Overshoot			5		%
Slew Rate (unity gain)	$R_L \geq 2\,k\Omega$		0.5		V/µs
The following specifications apply for $0°C \leq T_A \leq +70°C$:					
Input Offset Voltage	$R_S \leq 10\,k\Omega$			7.5	mV
Input Offset Current				300	nA
Input Bias Current				800	nA
Large-Signal Voltage Gain	$R_L \geq 2\,k\Omega$ $V_{OUT} = \pm 10$V	15.000			
Output Voltage Swing	$R_L \geq 2\,k\Omega$	± 10			V

TYPICAL PERFORMANCE CURVES (25°C free air temperature unless otherwise noted)

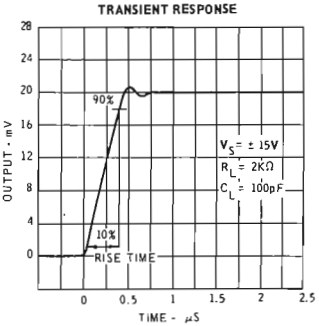
OPEN LOOP VOLTAGE GAIN



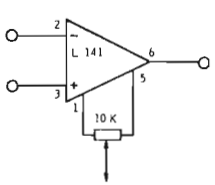
OPEN LOOP FREQUENCY RESPONSE



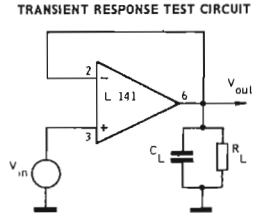
TRANSIENT RESPONSE



VOLTAGE OFFSET NULL CIRCUIT



TRANSIENT RESPONSE TEST CIRCUIT



Dual frequency compensated operational amplifier

STANDARD TEMPERATURE RANGE.
0°C to 70°C

- NO FREQUENCY COMPENSATION REQUIRED
- SHORT-CIRCUIT PROTECTION
- OFFSET VOLTAGE NULL CAPABILITY
- LARGE COMMON MODE AND DIFFERENTIAL VOLTAGE RANGES
- LOW POWER CONSUMPTION
- NO LATCH-UP

The L147B1 is a pair of high performance monolithic operational amplifiers intended for a wide range of analogue applications where board space or weight are important. High common mode voltage range and absence of "latch-up" make the L147B1 ideal for use as a voltage follower. The high gain and wide range of operating voltage provide superior performance in integrator, summing amplifier and general feedback applications. The L147B1 is short-circuit protected and requires no external components for frequency compensation. The internal 6 dB/octave roll-off ensures stability in closed loop applications. For single amplifier performance see L 141 data sheet.

ABSOLUTE MAXIMUM RATINGS

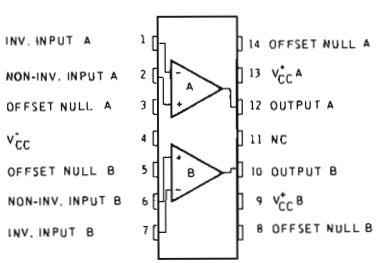
Supply Voltage	±18 V
Differential Input Voltage	± 30 V
Input Voltage Range (Note 1)	± 15 V
Voltage Between Offset Null and V_{CC}^-	± 0.5 V
Storage Temperature Range	-55°C to 125°C
Power Dissipation ($T_A \leq 70°C$)	500 mW
Operating Temperature Range	0°C to 70°C
Thermal Resistance J-A	110°C/W
Output Short-Circuit Duration (Note 2)	Indefinite
Lead Temperature (Soldering, 10 sec time limit)	260°C
Max Junction Temperature	125°C

ORDERING NUMBER

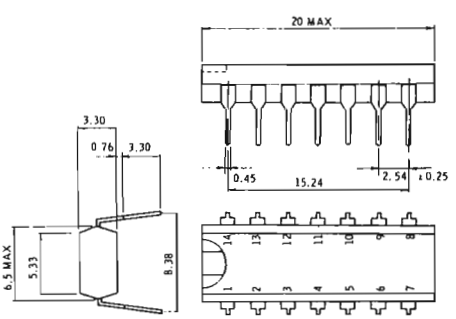
L 147 B1

Notes on the following page.

CONNECTION DIAGRAM
(Top view)



PHYSICAL DIMENSIONS
14 pin plastic DIP



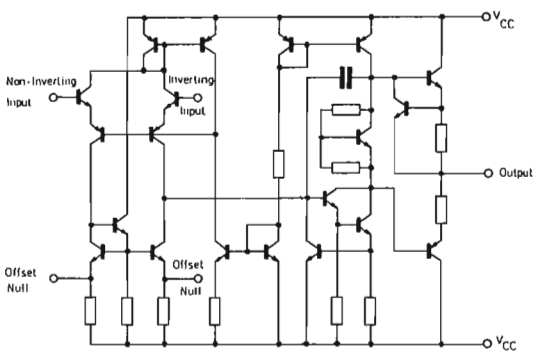
Note : all dimensions in mm.

STANDARD TEMPERATURE RANGE

ELECTRICAL CHARACTERISTICS (T_A = 25°C; V_{CC}=±15V unless otherwise specified), for each amplifier.

PARAMETER	CONDITIONS	Min.	Typ.	Max.	UNIT
Input Offset Voltage	$R_S \leq 10\,k\Omega$		± 1	± 6	mV
Input Offset Current			20	200	nA
Input Bias Current			80	500	nA
Input Resistance		0.3	2		MΩ
Input Capacitance			1.4		pF
Offset Voltage Adjustment Range			±15		mV
Input Voltage Range		± 12	±13		V
Large Signal Voltage Gain	$R_L \geq 2\,k\Omega$ V_{OUT} = ± 10V	50.000	200.000		
Common Mode Rejection Ratio	$R_S \leq 10\,k\Omega$	70	90		dB
Output Resistance			75		Ω
Supply Voltage Rejection Ratio	$R_S \leq 10\,k\Omega$		30	150	µV/ V
Output Short-Circuit Current			25		mA
Supply Current			1.7	2.8	mA
Output Voltage Swing	$R_L \geq 2\,k\Omega$	±10	± 13		V
	$R_L \geq 10\,k\Omega$	±12	± 14		V
Power Consumption			50	85	mW
Transient Response (unity gain):	V_{IN} = 20mV R_L=2kΩ $C_L \leq$100pF				
Risetime			0.3		µs
Overshoot			5		%
Slew Rate	$R_L \geq 2\,k\Omega$		0.5		V/ µs
Channel Separation			120		dB
The following specifications apply for $0°C \leq T_A \leq 70°C$:					
Input Offset Voltage	$R_S \leq 10\,k\Omega$		± 1	± 7.5	mV
Input Offset Current				300	nA
Input Bias Current			30	800	nA
Large Signal Voltage Gain	$R_L \geq 2\,k\Omega$ V_{OUT} = ± 10V	25.000			
Output Voltage Swing	$R_L \geq 2\,k\Omega$	±10	± 13		V

EQUIVALENT CIRCUIT (Each side)

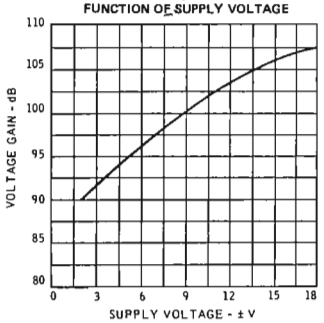


Notes :
1) For supply voltages less than ± 15V, the absolute maximum input voltage is equal to the supply voltage.
2) Short-circuit to ground for both sections or to either supply (for one section only).

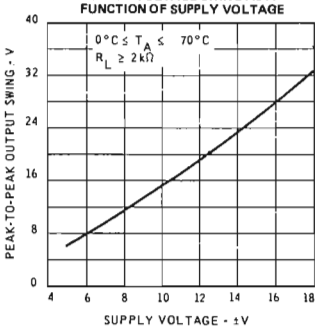
STANDARD TEMPERATURE RANGE

TYPICAL ELECTRICAL CHARACTERISTICS (Each amplifier)

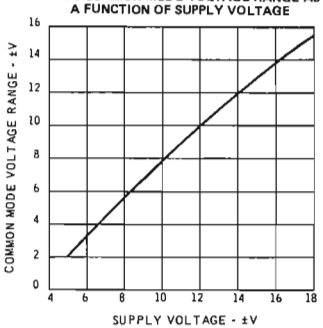
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



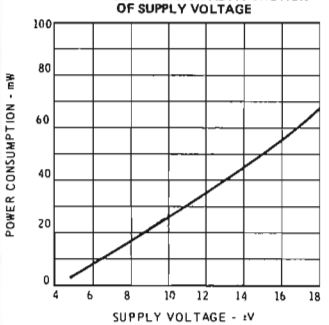
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



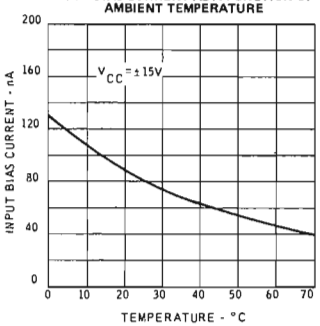
INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



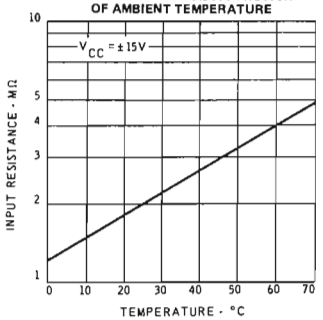
POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE



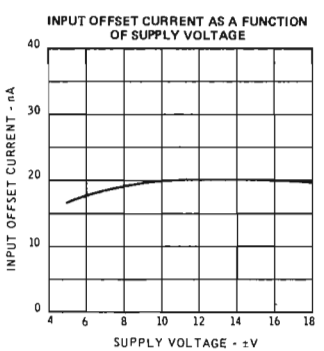
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



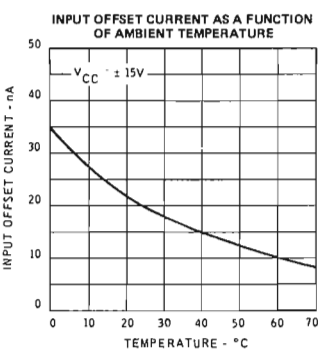
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



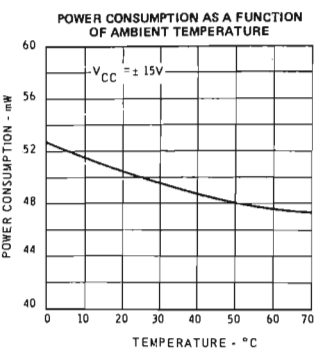
INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

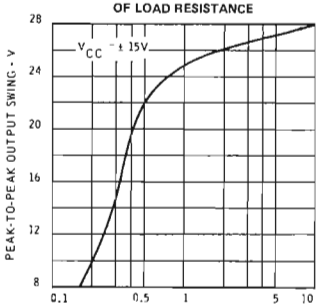


POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE

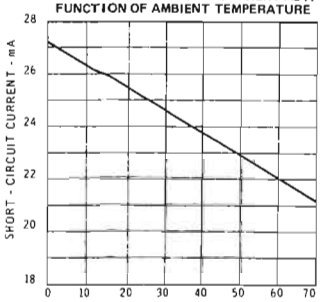


TYPICAL ELECTRICAL CHARACTERISTICS (Each amplifier)

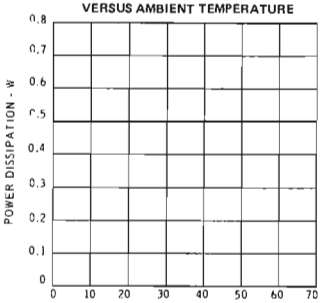
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



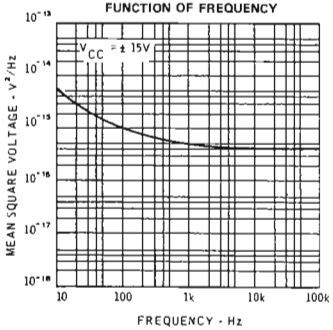
OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



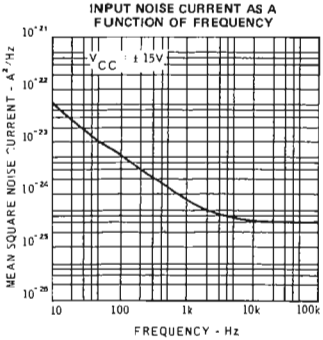
MAX ALLOWABLE POWER DISSIPATION VERSUS AMBIENT TEMPERATURE



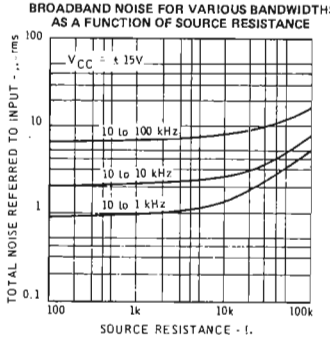
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



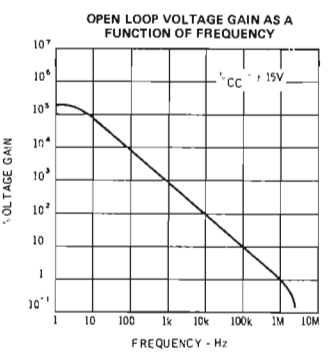
INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY



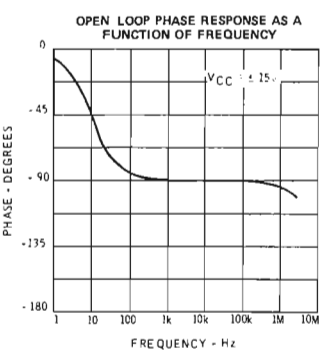
BROADBAND NOISE FOR VARIOUS BANDWIDTHS AS A FUNCTION OF SOURCE RESISTANCE



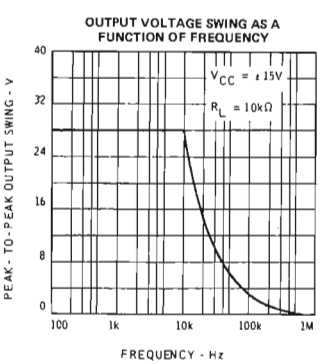
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



OPEN LOOP PHASE RESPONSE AS A FUNCTION OF FREQUENCY

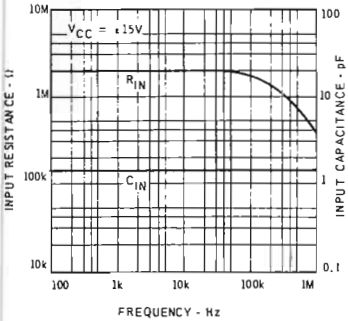


OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY

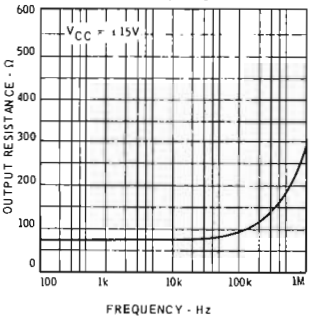


TYPICAL ELECTRICAL CHARACTERISTICS (Each amplifier)

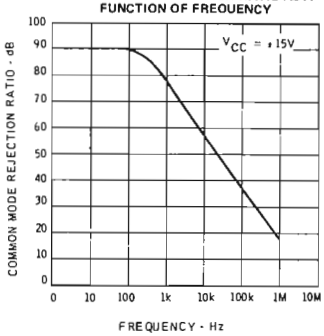
INPUT RESISTANCE AND INPUT CAPACITANCE AS A FUNCTION OF FREQUENCY



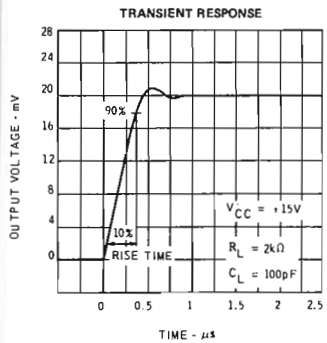
OUTPUT RESISTANCE AS A FUNCTION OF FREQUENCY



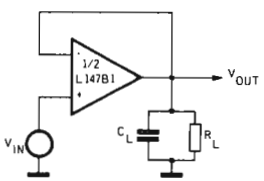
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



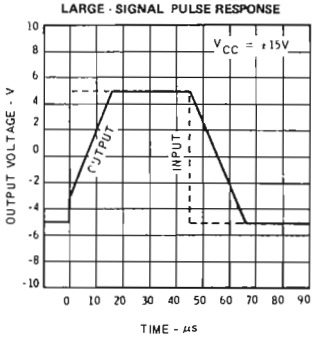
TRANSIENT RESPONSE



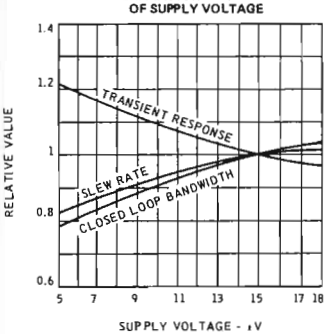
TRANSIENT RESPONSE TEST CIRCUIT



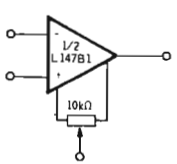
VOLTAGE FOLLOWER LARGE-SIGNAL PULSE RESPONSE



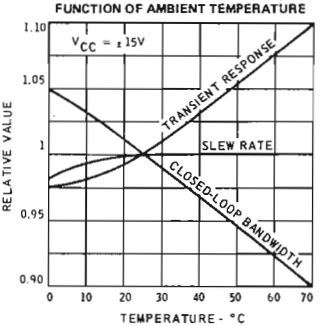
FREQUENCY CHARACTERISTICS AS A FUNCTION OF SUPPLY VOLTAGE



VOLTAGE OFFSET NULL CIRCUIT

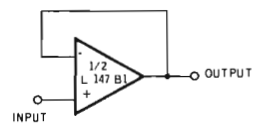


FREQUENCY CHARACTERISTICS AS A FUNCTION OF AMBIENT TEMPERATURE



TYPICAL APPLICATIONS

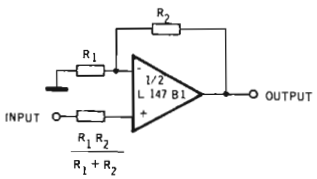
UNITY-GAIN VOLTAGE FOLLOWER



$R_{IN} = 400\ M\Omega$ $\quad R_{out} << 1\ \Omega$

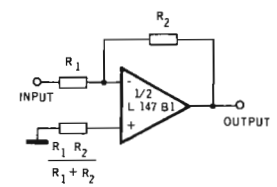
$C_{IN} = 1\ pF$ $\quad$ B.W. = 1 MHz

NON-INVERTING AMPLIFIER



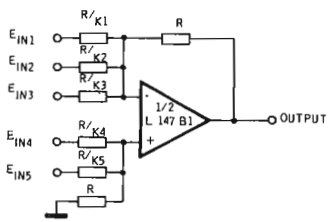
GAIN	R_1	R_2	B.W.	R_{IN}
10	1 kΩ	9 kΩ	100kHz	400MΩ
100	100 Ω	9.9k Ω	10kHz	280MΩ
1000	100 Ω	99.9k Ω	1kHz	80MΩ

INVERTING AMPLIFIER



GAIN	R_1	R_2	B.W.	R_{IN}
1	10k Ω	10k Ω	1 MHz	10kΩ
10	1kΩ	10k Ω	100kHz	1kΩ
100	1kΩ	100k Ω	10kHz	1 Ω
1000	100Ω	100k Ω	1kHz	100 Ω

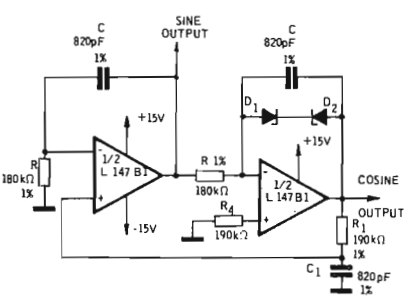
WEIGHTED AVERAGING AMPLIFIER



If $k_1 + k_2 + k_3 = k_4 + k_5$ the response equation is given by

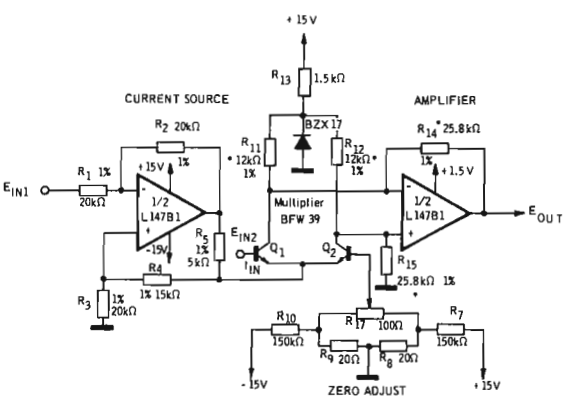
$E_{out} = E_{IN1} K_1 + E_{IN2} K_2 + E_{IN3} - E_{IN4} K_4 - E_{IN5} K_5$

QUADRATURE OSCILLATOR



$$f = \frac{1}{2\pi RC}$$

ANALOGUE-MULTIPLIER

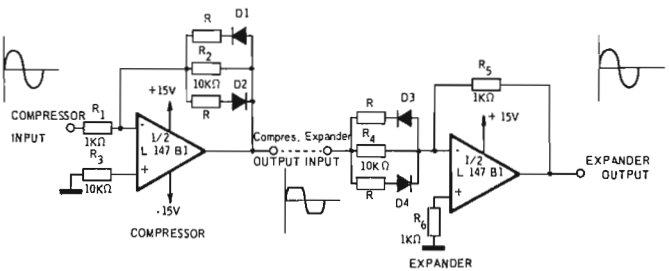


* Matched to 0.1%

$E_{OUT} = 100\ E_{IN1} \times E_{IN2}$

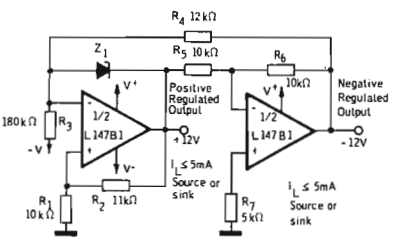
TYPICAL APPLICATIONS (contd)

COMPRESSOR/EXPANDER AMPLIFIERS



Maximum compression expansion ratio = R_1/R $(10k\Omega > R > 0)$
Note : diodes D_1 through D_4 are matched BAW 55 or equivalent

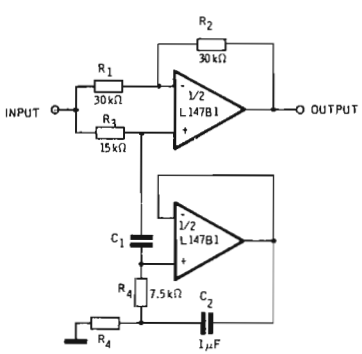
TRACKING POSITIVE AND NEGATIVE VOLTAGE REFERENCES



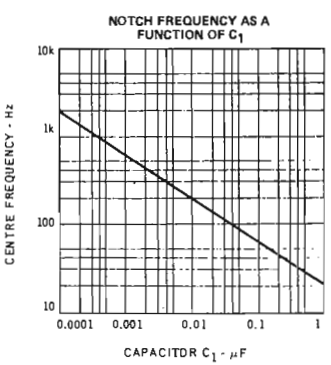
$$\text{Positive output} = V_{Z1} \times \frac{R_1 + R_2}{R_2}$$

$$\text{Negative output} = -\text{ positive output } \times \frac{R_6}{R_5}$$

NOTCH FILTER USING THE L 147B1 AS A GYRATOR



Trim R_3 such that $\frac{R_1}{R_2} = \frac{R_3}{2R_4}$



DEFINITION OF TERMS :

INPUT OFFSET VOLTAGE – That voltage which must be applied between the input terminals to obtain zero output voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT OFFSET CURRENT – The difference in the currents into the two input terminals with the output at zero volts.

INPUT BIAS CURRENT – The average of the two input currents.

INPUT RESISTANCE – The resistance looking into either input terminal with the other grounded.

INPUT CAPACITANCE – The capacitance looking into either input terminal with the other grounded.

LARGE-SIGNAL VOLTAGE GAIN – The ratio of the maximum output voltage swing with load to the change in input voltage required to drive the output from zero to this voltage.

OUTPUT RESISTANCE – The resistance seen looking into the output terminal with the output at null. This parameter is defined only under small signal conditions at frequencies above a few hundred cycles to eliminate the influence of drift and terminal feedback.

OUTPUT SHORT-CIRCUIT CURRENT – The maximum output current available from the amplifier with the output shorted to ground or to either supply

SUPPLY CURRENT – The DC current from the supplies required to operate the amplifier with the output at zero and with no load current.

POWER CONSUMPTION – The DC power required to operate the amplifier with the output at zero and with no load current.

TRANSIENT RESPONSE – The closed-loop step-function response of the amplifier under small-signal conditions.

INPUT VOLTAGE RANGE – The range of voltage which, if exceeded on either input terminal, could cause the amplifier to cease functioning properly.

INPUT COMMON MODE REJECTION RATIO – The ratio of the input voltage range to the maximum change in input offset voltage over this range.

SUPPLY VOLTAGE REJECTION RATIO – The ratio of the change in input voltage to the change in supply voltage producing it.

OUTPUT VOLTAGE SWING – The peak output swing, referred to zero, that can be obtained without clipping.

EXTENDED TEMPERATURE RANGE,
-55 °C ÷ +125°C

- SHORT-CIRCUIT PROTECTION
- OFFSET VOLTAGE NULL CAPABILITY
- LARGE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGES
- LOW POWER CONSUMPTION
- NO LATCH-UP

High performance operational amplifier

The L 148 T2 is a high performance monolithic operational amplifier intended for a wide range of analog applications where tailoring of frequency characteristics is desirable. High common mode voltage range and absence of "latch-up" make the L 148 T2 ideal for use as a voltage follower. The high gain and wide range of operating voltages provide superior performance in integrator, summing amplifier and general feedback applications. The L 148 T2 is short-circuit protected and has the same pin configuration as the L 141 operational amplifier. Unity gain frequency compensation is achieved by means of a single 30pF capacitor.

ABSOLUTE MAXIMUM RATINGS

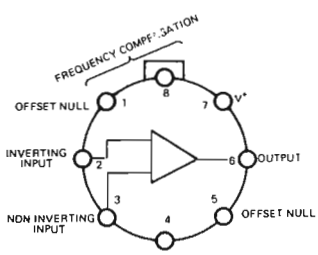
Supply Voltage	± 22 V
Internal Power Dissipation (1)	500 mW
Differential Input Voltage	± 30 V
Input Voltage (2)	± 15 V
Storage Temperature Range	-65°C ÷ 150°C
Operating Temperature Range	-55°C ÷ 125°C
Lead Temperature (Soldering, 60 sec.)	300°C
Output Short-Circuit Duration (3)	Indefinite

ORDERING NUMBER

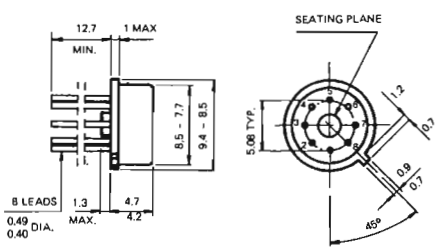
L148 T2

Notes on the following page.

CONNECTION DIAGRAM
(Top view)



PHYSICAL DIMENSIONS
in accordance with
JEDEC TO-99 outline



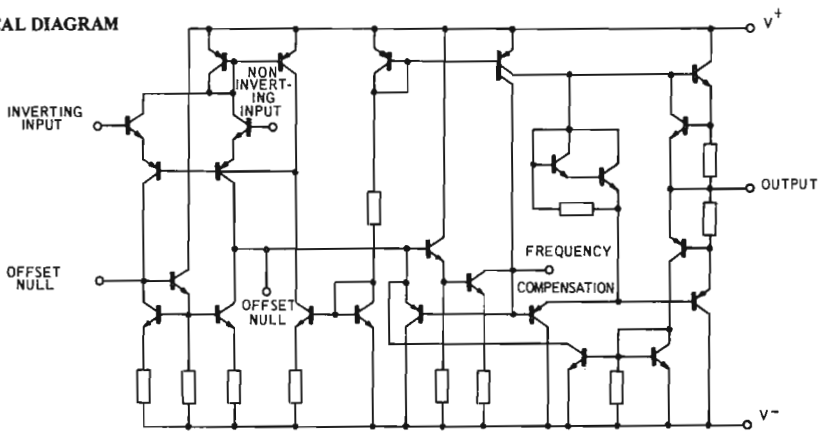
Note : All dimensions in mm.

EXTENDED TEMPERATURE RANGE

ELECTRICAL CHARACTERISTICS ($V_S = \pm 15V$, $T_A = 25°C$ unless otherwise specified)

PARAMETER	CONDITION	Min.	Typ.	Max.	Unit
Input Offset Voltage	$R_S \leq 10\,K\Omega$		1	5	mV
Input Offset Current			20	200	nA
Input Bias Current			80	500	nA
Input Resistance		0.3	2		M Ω
Input Capacitance			1.4		pF
Large-Signal Voltage Gain	$R_L \geq 2K\Omega$ $V_{OUT} = \pm 10V$	50.000	200.000		
Output Resistance			75		Ω
Output Short-Circuit Current			25		mA
Power Consumption			50	85	mW
Transient Response (Unity Gain) :	$V_{in} = 20$ mV $C_C = 30$ pF $R_L = 2\,K\Omega$ $C_L \leq 100$ pF				
Risetime			0.3		µS
Overshoot			5		%
Slew Rate	$R_L \geq 2\,K\Omega$ $C_C = 30$ pF		0.5		V/µS
The following specification apply for $-55°C \leq T_A \leq +125°C$:					
Input Offset Voltage	$R_S \leq 10\,K\Omega$		1	6	mV
Input Offset Current	$T_A = +125°C$		7	200	nA
	$T_A = -55°C$		85	500	nA
Input Bias Current	$T_A = +125°C$		0.03	0.5	µA
	$T_A = -55°C$		0.3	1.5	µA
Input Voltage Range		± 12	± 13		V
Common Mode Rejection Ratio	$R_S \leq 10\,K\Omega$	70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10\,K\Omega$		30	150	µV/V
Large-Signal Voltage Gain	$R_L \geq 2\,K\Omega$ $V_{OUT} = \pm 10V$	25.000			
Output Voltage Swing	$R_L \geq 10K\Omega$	± 12	± 14		V
	$R_L \geq 2\,K\Omega$	± 10	± 13		V
Power Consumption	$T_A = +125°C$		45		mW
	$T_A = -55°C$		60		mW

ELECTRICAL DIAGRAM

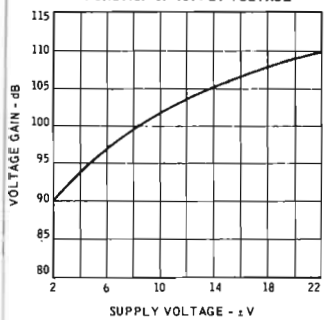


NOTES :

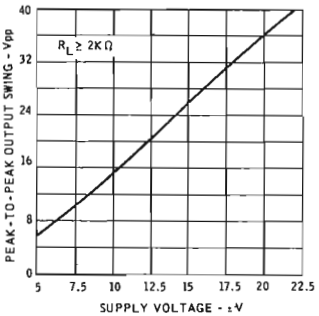
1) Rating applies for case temperatures to 125°C; derate linearly at 10 mW/°C for ambient temperatures above +75°C.
2) For supply voltage less than ± 15V, the absolute maximum input voltage is equal to the supply voltage.
3) Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature.

TYPICAL ELECTRICAL CHARACTERISTICS (25° C free air temperature unless otherwise noted)

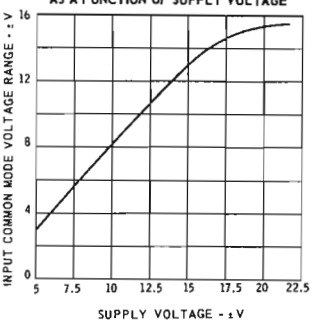
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



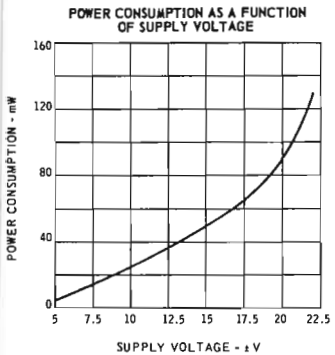
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



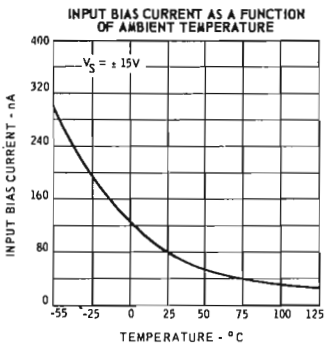
INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



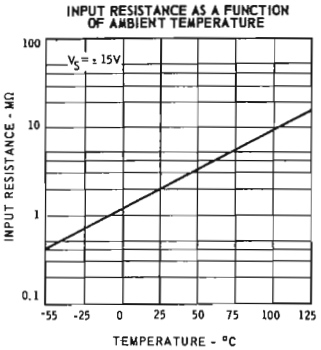
POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE



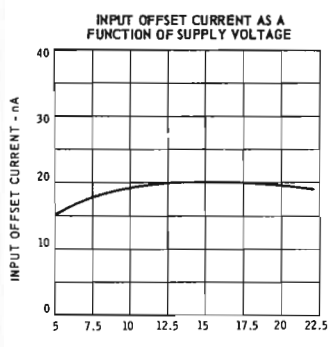
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



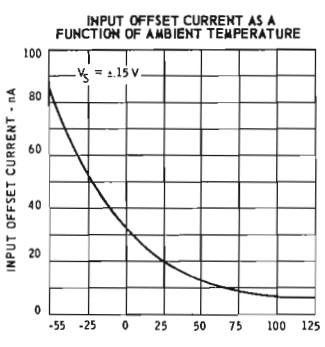
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



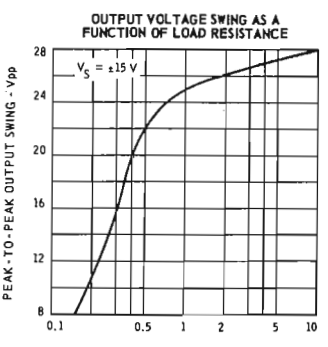
INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



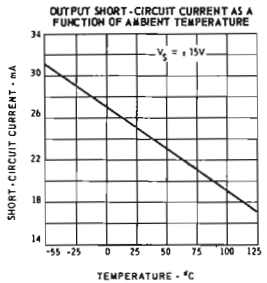
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

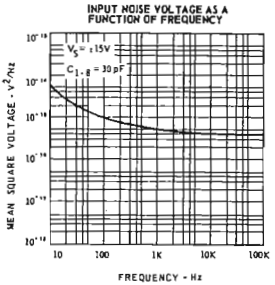


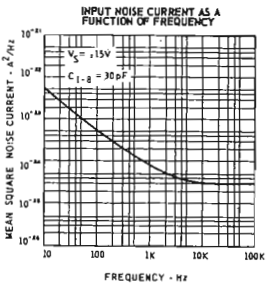
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE

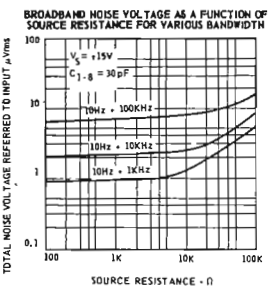


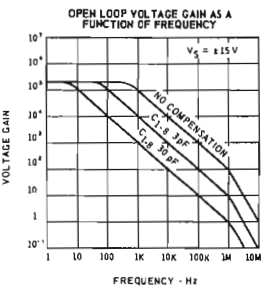
TYPICAL ELECTRICAL CHARACTERISTICS (25° C free air temperature unless otherwise noted)

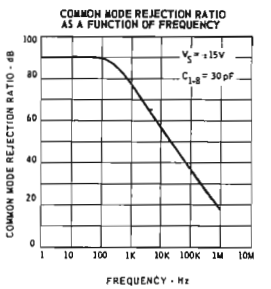


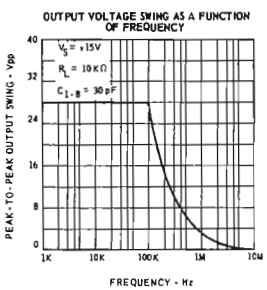


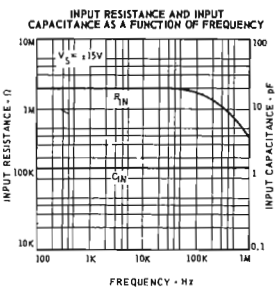


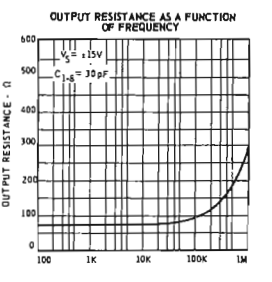




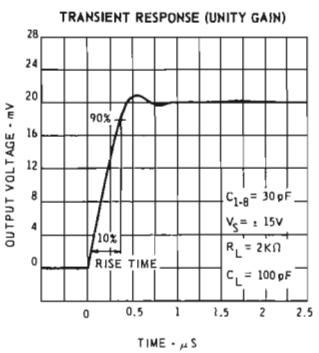


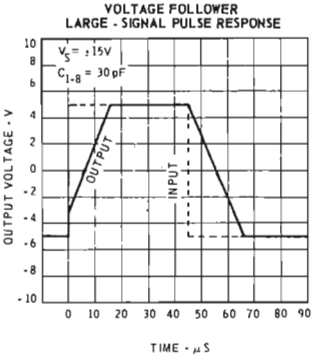


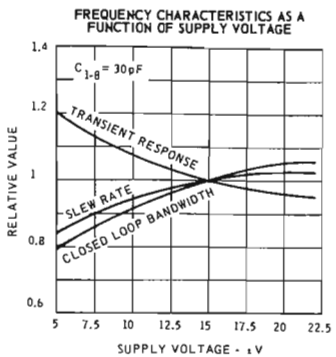


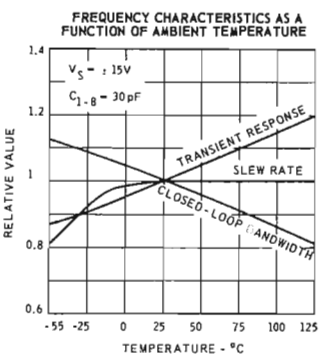


TYPICAL ELECTRICAL CHARACTERISTICS (25° C free air temperature unless otherwise noted)









STANDARD TEMPERATURE RANGE, 0°C ÷ 70°C

High performance operational amplifier

- SHORT-CIRCUIT PROTECTION
- OFFSET VOLTAGE NULL CAPABILITY
- LARGE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGES
- LOW POWER CONSUMPTION
- NO LATCH-UP

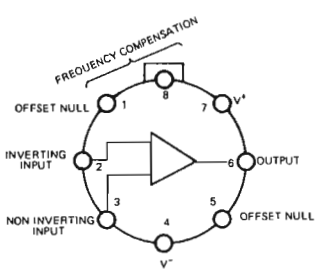
The L 148 T1 is a high performance monolithic operational amplifier intended for a wide range of analog applications where tailoring of frequency characteristics is desirable. High common mode voltage range and absence of "latch-up" make the L 148 T1 ideal for use as a voltage follower. The high gain and wide range of operating voltages provide superior performance in integrator, summing amplifier, and general feedback applications. The L 148 T1 is short-circuit protected and has the same pin configuration as the L 141 operational amplifier. Unity gain frequency compensation is achieved by means of a single 30 pF capacitor. For full temperature range operation (-55°C ÷ +125°C), see L 148 T2 data sheet.

ABSOLUTE MAXIMUM RATINGS

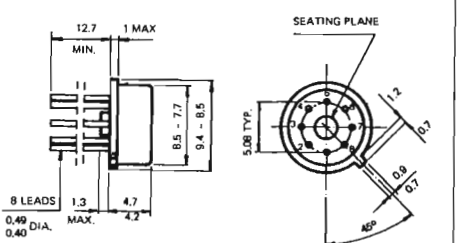
Supply Voltage	± 18V
Internal Power Dissipation (1)	500 mW
Differential Input Voltage	± 30V
Input Voltage (2)	± 15V
Storage Temperature Range	-55°C ÷ +150°C
Operating Temperature Range	0°C ÷ + 70°C
Lead Temperature (soldering, 60 secs)	300°C
Output Short-Circuit Duration (3)	Indefinite

Notes on the following page.

CONNECTION DIAGRAM
(Top view)



PHYSICAL DIMENSIONS
in accordance with
JEDEC TO-99 outline



Note : All dimensions in mm.

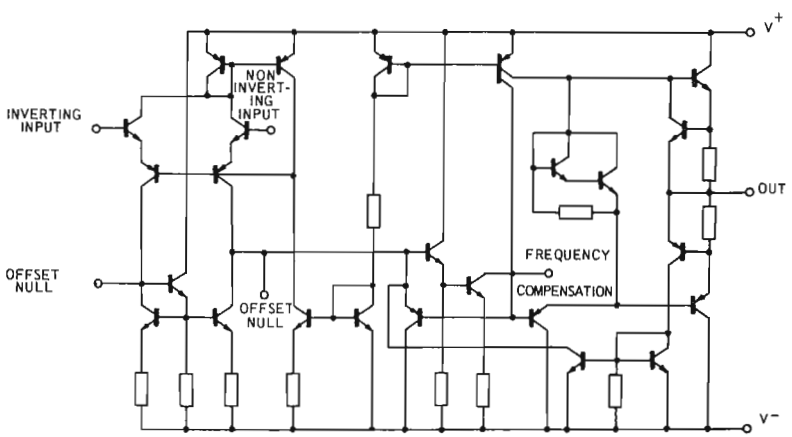
ORDERING NUMBER
L148 T1

STANDARD TEMPERATURE RANGE

ELECTRICAL CHARACTERISTICS ($V_S = \pm 15V$, $T_A = 25°C$ unless otherwise noted)

PARAMETER	CONDITIONS		Min.	Typ.	Max.	Units
Input Offset Voltage	$R_S \leq 10K\Omega$			1	6	mV
Input Offset Current				20	200	nA
Input Bias Current				80	500	nA
Input Resistance			0.3	2		MΩ
Input Capacitance				1.4		pF
Large-Signal Voltage Gain	$R_L \geq 2K\Omega$	$V_{OUT} = \pm 10V$	50.000	200.000		
Output Resistance				75		Ω
Output Short-Circuit Current				25		mA
Power Consumption				50	85	mW
Transient Response (Unity Gain):	$V_{in} = 20mV$	$C_C = 30$ pF				
	$R_L = 2K\Omega$	$C_L \leq 100$ pF				
Risetime				0.3		µs
Overshoot				5.0		%
Slew Rate	$R_L \geq 2K\Omega$			0.5		V/µS
The following specifications apply for $0°C \leq T_A \leq +70°C$:						
Input Offset Voltage	$R_S \leq 10K\Omega$			1	7.5	mV
Input Offset Current					300	nA
Input Bias Current					800	nA
Large-Signal Voltage Gain	$R_L \geq 2K\Omega$	$V_{OUT} = \pm 10V$	25.000			
Output Voltage Swing	$R_L \geq 2K\Omega$		±10	±13		V
Power Consumption				50		mW

ELECTRICAL DIAGRAM



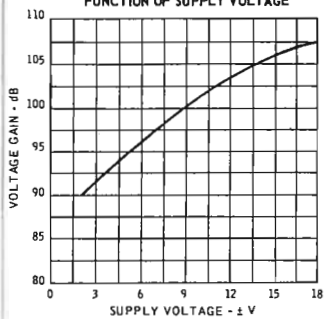
NOTES :

1) Rating applies for case temperatures to + 70°C.
2) For supply voltages less than ± 15V, the absolute maximum input voltage is equal to the supply voltage.
3) Short circuit may be to ground or either supply. Rating applies to + 70°C ambient temperature.

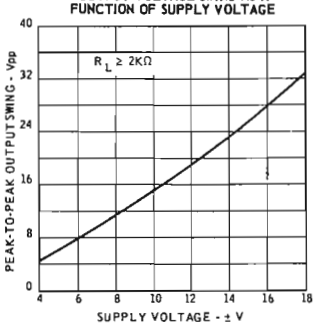
STANDARD TEMPERATURE RANGE

TYPICAL ELECTRICAL CHARACTERISTICS (25° C free air temperature unless otherwise noted)

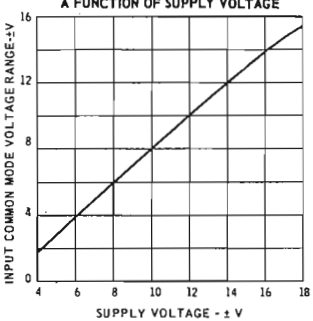
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



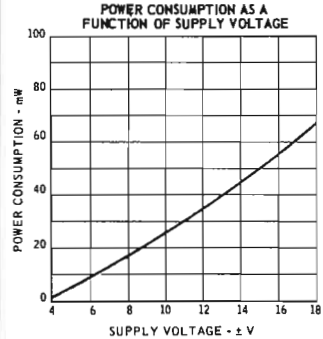
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



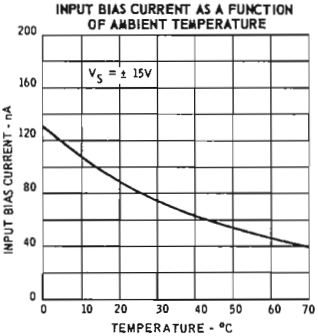
INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



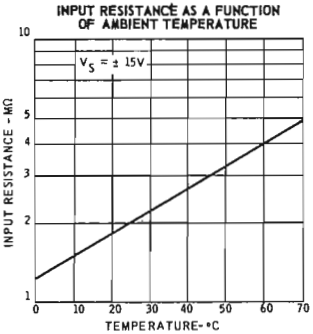
POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE



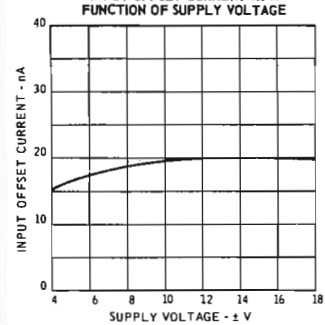
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



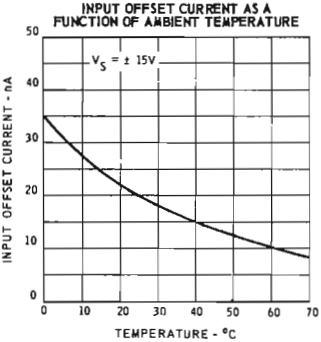
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



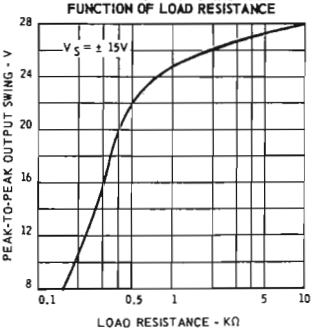
INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

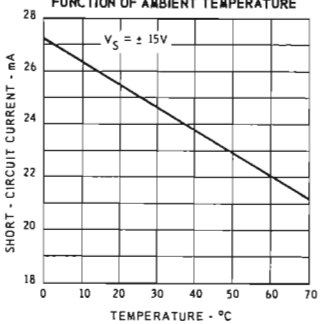


OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE

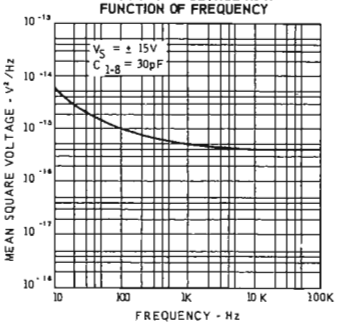


TYPICAL ELECTRICAL CHARACTERISTICS (25° C free air temperature unless otherwise noted)

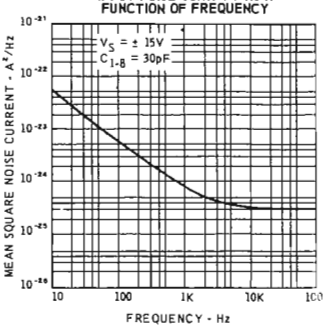
OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



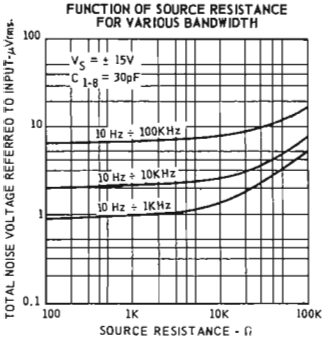
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



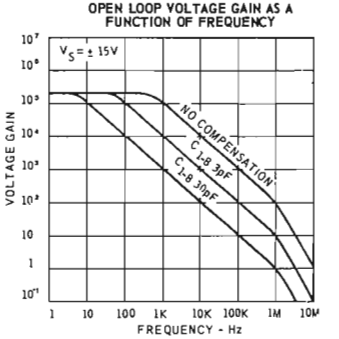
INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY



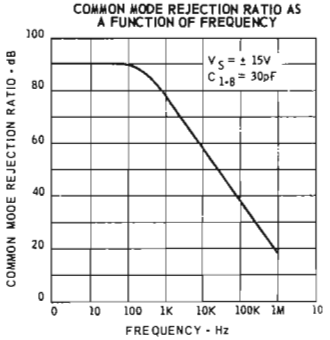
BROADBAND NOISE VOLTAGE AS A FUNCTION OF SOURCE RESISTANCE FOR VARIOUS BANDWIDTH



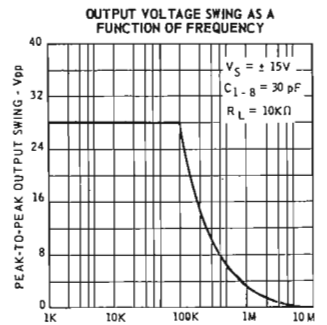
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



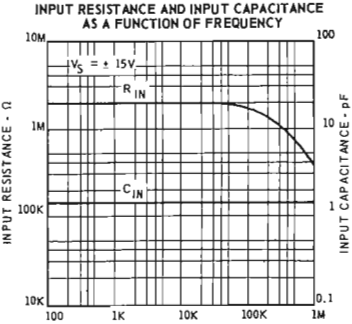
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



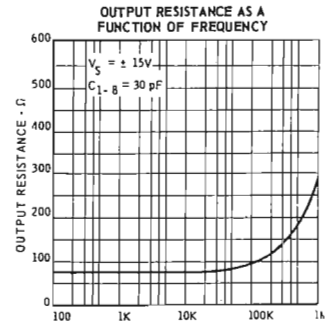
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



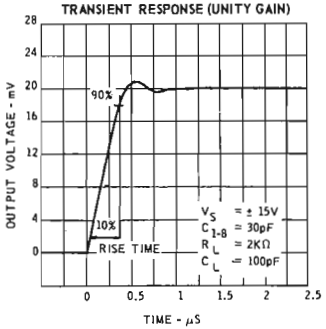
INPUT RESISTANCE AND INPUT CAPACITANCE AS A FUNCTION OF FREQUENCY

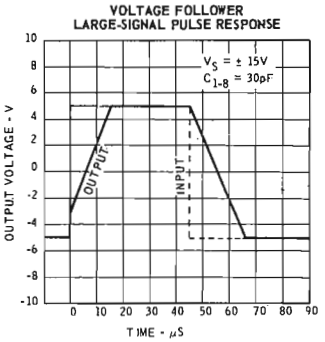


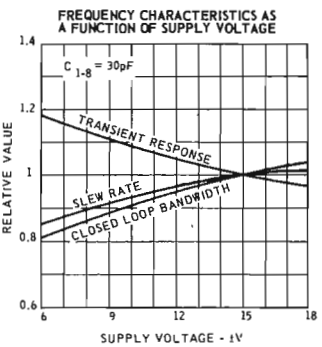
OUTPUT RESISTANCE AS A FUNCTION OF FREQUENCY

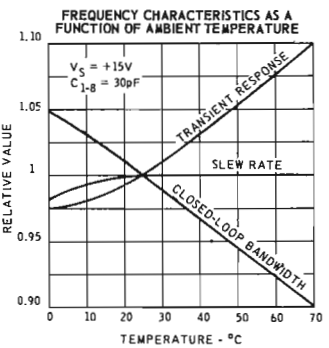


TYPICAL ELECTRICAL CHARACTERISTICS (25° C free air temperature unless otherwise noted)









Audio amplifier

INTERMEDIATE TEMPERATURE RANGE, −40°C to 85°C

- HIGH OUTPUT POWER
- LOW DISTORTION
- LOW QUIESCENT CURRENT
- SELF CENTERING BIAS
- HIGH INPUT IMPEDANCE

The TAA 611E is a monolithic integrated circuit particularly designed for use as audio amplifier where a temperature range of -40°C to 85°C is required. The usable range of supply voltage varies from 6V to 10V. Special features of the circuit include low quiescent current, self-centering bias and direct coupling of the input. The circuit requires a minimum number of external components.

ABSOLUTE MAXIMUM RATINGS

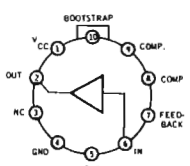
Max Supply Voltage	12 V
Input Voltage (see note)	-0.5 to + 12 V
Peak Output Current	1 A
Operating Temperature Range	-40°C to +85°C
TAA 611E 55	
Storage Temperature	-55°C to + 150°C
Maximum Junction Temperature	150°C
Power Dissipation ($T_A \leq 25°C$)	570 mW
Power Dissipation ($T_C \leq 85°C$)	1.3 W
Thermal Resistance J-A	220° C/W
Thermal Resistance J-C	50° C/W
TAA 611E 12	
Storage Temperature	-55°C to + 125°C
Maximum Junction Temperature	150°C
Power Dissipation ($T_A \leq 25°C$)	1.35 W
Thermal Resistance J-A	93° C/W

Note : for supply voltages less than 12V, the absolute max input voltage is equal to the supply voltage.

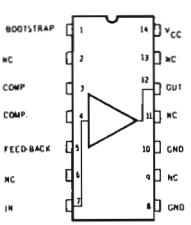
ORDERING NUMBERS

TAA 611E 55 (for package No. 1)
TAA 611E 12 (for package No. 2)

CONNECTION DIAGRAMS
(top view)



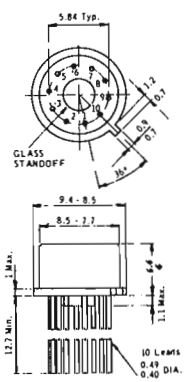
Package No. 1



Package No. 2

PACKAGE No. 1

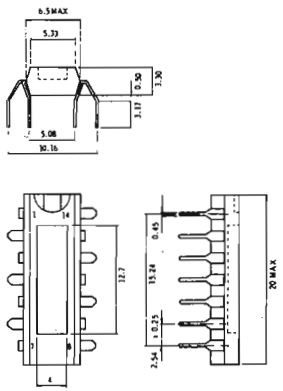
PHYSICAL DIMENSIONS
in accordance with
JEDEC TO-5 outline



Note : All dimensions in mm.

PACKAGE No. 2

PHYSICAL DIMENSIONS
power plastic split DIP



Note : All dimensions in mm.

OUTPUT POWER AS A FUNCTION OF SUPPLY VOLTAGE AND LOADING CONDITIONS

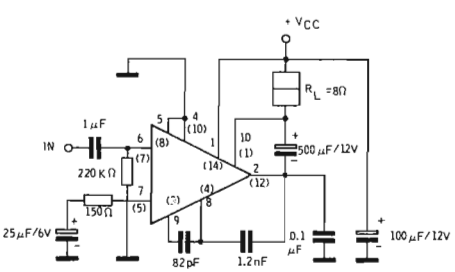
(Typical values at ambient temperature $T_A = 25°C$)

V_{CC} (Ω)	R_L (Ω)	P_{out} (W) at THD = 2%	P_{out} (W) THD = 10%			External Heat Sink
			Min.	Typ.	Typ. -40°C	
6	4	0.50		0.65	0.6	Not Required
	8	0.35		0.45	0.42	Not Required
9	4	1.4		1.8	1.7	For TAA 611E 55 only
	8	0.9	0.85	1.15	1.1	Not Required

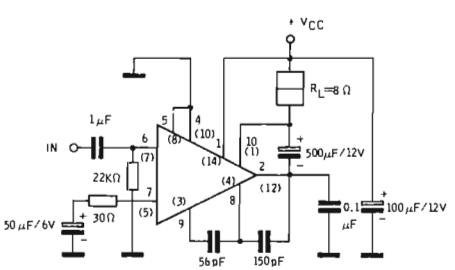
TYPICAL ELECTRICAL CHARACTERISTICS ($T_A = 25°C$, $V_{CC} = 9V$ unless otherwise noted)

PARAMETER	CONDITIONS	VALUE	UNIT
Total Current (I_{CC})		3	mA
Quiescent Current of Output Transistors (I_O)		1	mA
Input Bias Current		60	nA
DC Output Voltage	$R_S = 220\ K\Omega$	4.8	V
Open Loop Voltage Gain	$R_L = 8\ \Omega$	68	dB
Supply Current	$P_{out} = 1.15W \quad R_L = 8\ \Omega$	170	mA
The Following Specifications Apply for $-40°C \leq T_A \leq 85°C$:			
Quiescent Current of Output Transistors (I_O)		1.1	mA
Open Loop Voltage Gain	$R_L = 8\ \Omega$	67	dB
Total Harmonic Distortion	Test Circuit 1: $R_L = 8\ \Omega$, f = 1KHz		
	$P_{out} = 50mW$	0.4	%
	$R_L = 8\ \Omega$, f = 1KHz, $P_{out} = 0.5W$	0.3	%
	Test Circuit 2: $R_L = 8\ \Omega$, f = 1KHz		
	$P_{out} = 50mW$	1.7	%
	$R_L = 8\ \Omega$, f = 1KHz, $P_{out} = 0.5W$	1.2	%
Feedback Resistance	Pin 2 to 7 (TAA 611E 55)	7.5	KΩ
	Pin 5 to 12 (TAA 611E 12)	7.5	KΩ
Input Impedance	Open Loop	0.75	MΩ

TEST CIRCUIT 1 ($A_V = 50$)

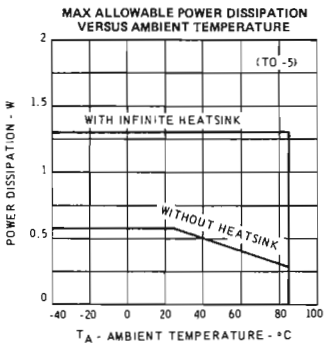


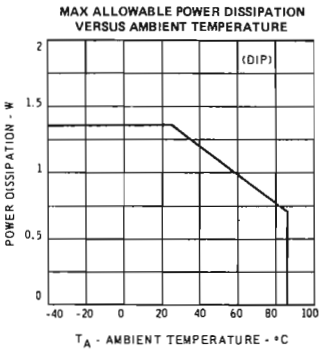
TEST CIRCUIT 2 ($A_V = 250$)

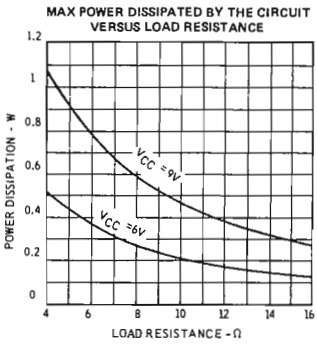


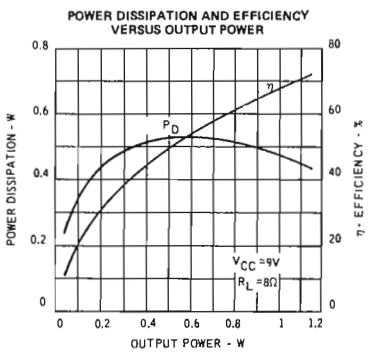
The pin numbers in brackets refer to the TAA 611E 12, and those without brackets refer to the TAA 611E 55.

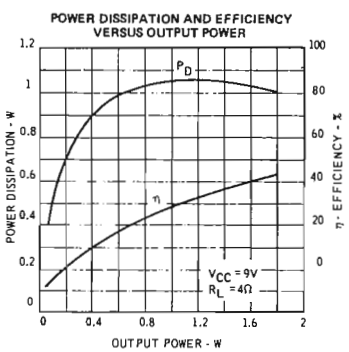
TYPICAL ELECTRICAL CHARACTERISTICS (25°C free air temperature unless otherwise noted)

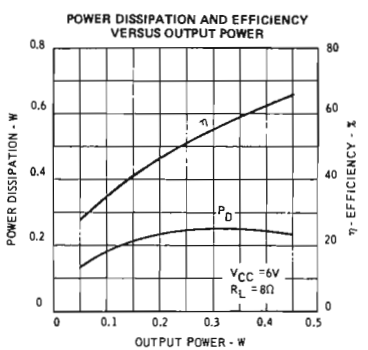


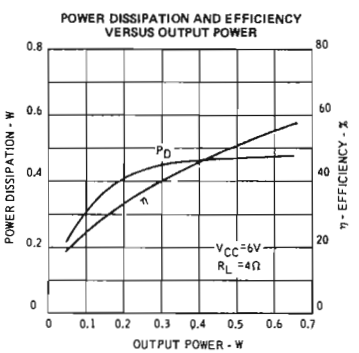




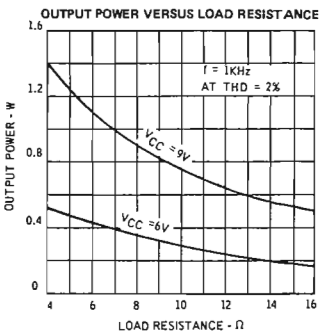


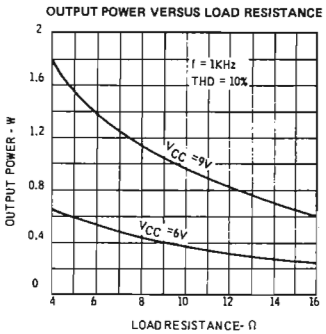


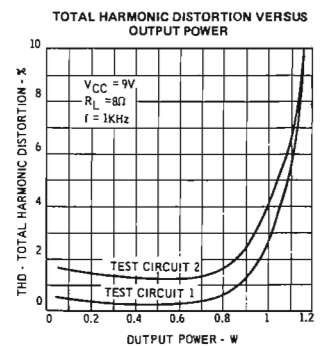


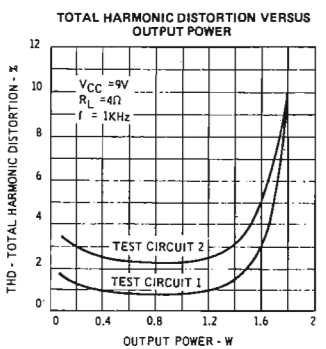


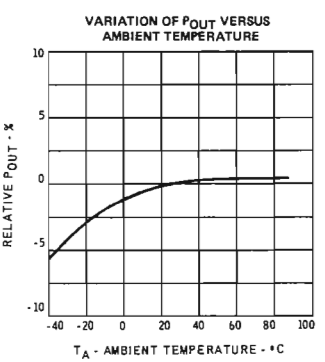
TYPICAL ELECTRICAL CHARACTERISTICS (25°C free air temperature unless otherwise noted)

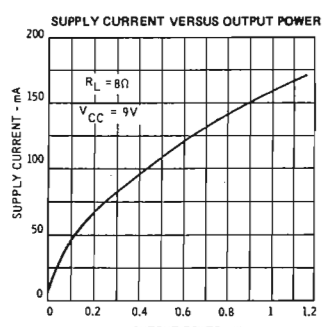




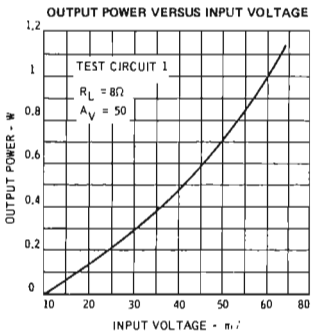


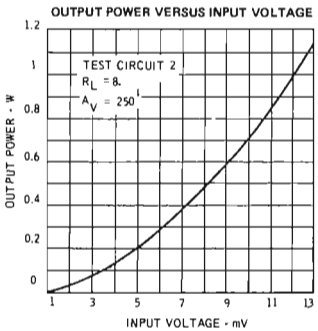


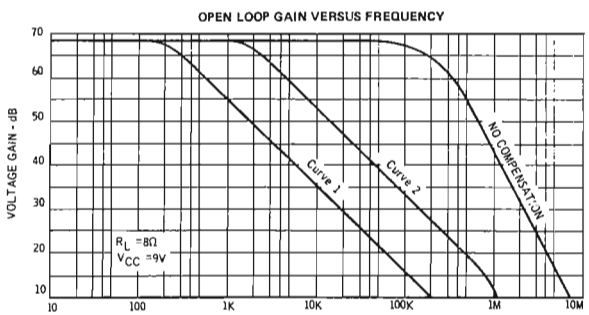




TYPICAL ELECTRICAL CHARACTERISTICS (25° free air temperature unless otherwise noted)



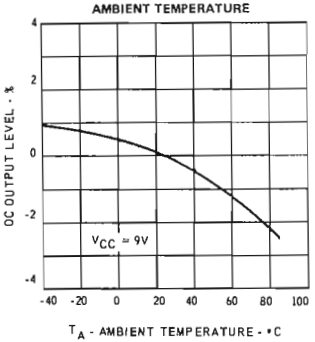




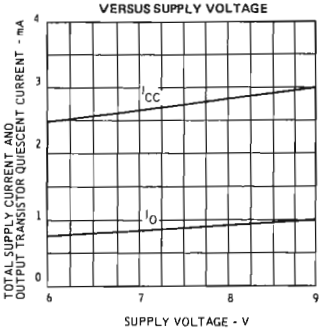
Curve 1: TAA611E 55, C_{9-8} = 82pF C_{8-2} = 1.2 nF C_{10-1} = 0.1 µF
TAA611E 12, C_{3-4} = 82pF C_{4-12} = 1.2nF C_{1-14} = 0.1 µF
Curve 2: TAA611E 55, C_{9-8} = 56pF C_{8-2} = 150pF C_{10-1} = 0.1 µF
TAA611E 12, C_{3-4} = 56pF C_{4-12} = 150pF C_{1-14} = 0.1 µF

TYPICAL ELECTRICAL CHARACTERISTICS (25° free air temperature unless otherwise noted)

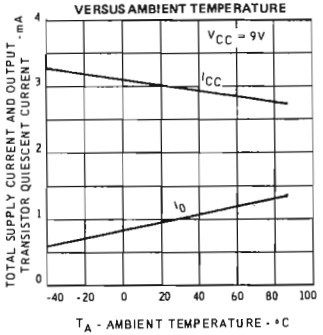
VARIATION OF DC OUTPUT LEVEL VERSUS AMBIENT TEMPERATURE



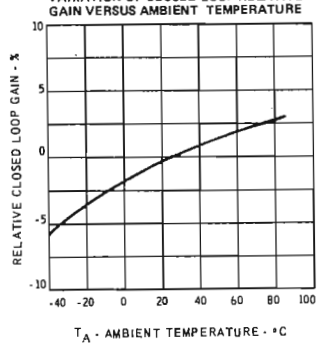
TOTAL SUPPLY CURRENT AND OUTPUT TRANSISTOR QUIESCENT CURRENT VERSUS SUPPLY VOLTAGE



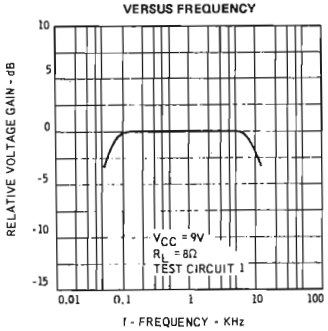
TOTAL SUPPLY CURRENT AND OUTPUT TRANSISTOR QUIESCENT CURRENT VERSUS AMBIENT TEMPERATURE



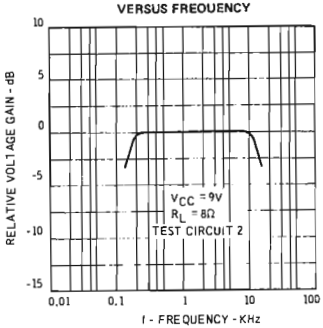
VARIATION OF CLOSED LOOP RELATIVE GAIN VERSUS AMBIENT TEMPERATURE



RELATIVE VOLTAGE GAIN VERSUS FREQUENCY



RELATIVE VOLTAGE GAIN VERSUS FREQUENCY



Audio amplifier

INTERMEDIATE TEMPERATURE RANGE, - 40° C to 85° C

- OUTPUT POWER 2.1 W
- LOW DISTORTION
- LOW QUIESCENT CURRENT
- SELF CENTERING BIAS
- HIGH INPUT IMPEDANCE

The TAA 611 F is a monolithic integrated circuit particularly designed for use as audio amplifier where a temperature range of -40°C to 85°C is required. The usable range of supply voltage varies from 6 to 15V. Special features of the circuit include low quiescent current, self-centering bias and direct coupling of the input. The circuit requires a minimum number of external components. The package is a special plastic DIP with a copper bar inserted in the plastic which ensures low thermal resistance.

ABSOLUTE MAXIMUM RATINGS

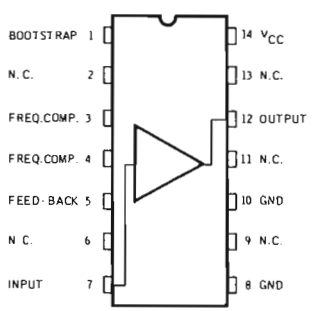
Maximum Operating Supply Voltage	15 V
Input Voltage (see note)	-0.5V to +15 V
Peak Output Current	1 A
Storage Temperature	-55°C to +125°C
Operating Temperature Range	-40°C to +85°C
Max Junction Temperature	150°C
Power Dissipation $T_A \leq 25°C$	1.35W
Thermal Resistance J-A	93°C/W

Note : For supply voltages less than 15V, the absolute max input voltage is equal to the supply voltage.

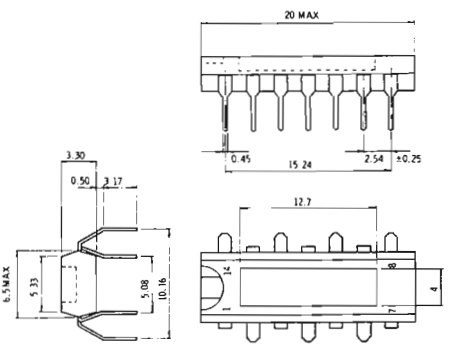
ORDERING NUMBER

TAA 611F 12

CONNECTION DIAGRAM
(Top view)



PHYSICAL DIMENSIONS
Power plastic split DIP



Note : All dimensions in mm.

OUTPUT POWER AS A FUNCTION OF SUPPLY VOLTAGE AND LOADING CONDITIONS

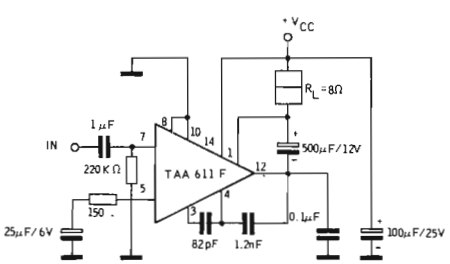
(Typical values at ambient temperature $T_A = 25°C$)

V_{CC} (V)	R_L (Ω)	P_{out} (W) at THD = 2%	P_{out} (W) at THD = 10%		
			Min.	Typ.	Typ. -40°C
9	8	0.9		1.15	1.1
12	8	1.7	1.5	2.1	2

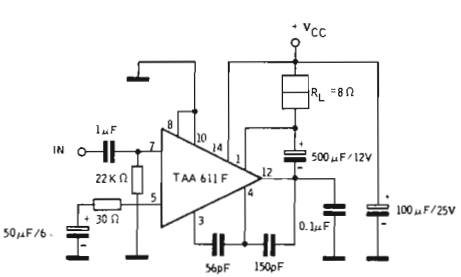
TYPICAL ELECTRICAL CHARACTERISTICS ($T_A = 25°C$ unless otherwise noted)

PARAMETER	CONDITIONS	VALUES		UNIT
		(V_{CC} = 9V)	(V_{CC} = 12V)	
Total Current (I_{CC})		3	3.5	mA
Quiescent Current of Output Transistors (I_O)		1	1.2	mA
Input Bias Current		60	75	nA
DC Output Voltage	R_S = 220 KΩ	4.8	6.3	V
Open Loop Voltage Gain	R_L = 8Ω	68	70	dB
Total Harmonic Distortion	Test Circuit 1: R_L = 8 Ω, f = 1KHz P_{out} = 1W		0.2	%
	Test Circuit 2: R_L = 8 Ω, f = 1KHz P_{out} = 1W		1	%
Supply Current	R_L = 8 Ω P_{out} = 1.15W	170		mA
	R_L = 8 Ω P_{out} = 2.1		235	mA
The Following Specifications Apply for -40°C ≤ T_A ≤ 85°C:				
Quiescent Current of Output Transistors (I_O)		1.1	1.3	mA
Open Loop Voltage Gain	R_L = 8 Ω	67	70	dB
Total Harmonic Distortion	Test Circuit 1: R_L = 8 Ω, f = 1KHz P_{out} = 50mW	0.4	0.3	%
	R_L = 8 Ω, f = 1KHz, P_{out} = 0.5W	0.3		%
	Test Circuit 2: R_L = 8 Ω, f = 1KHz P_{out} = 50mW	1.7	1.5	%
	R_L = 8 Ω, f = 1KHz, P_{out} = 0.5W	1.2		%
Feedback Resistance	Pin 5 to 12	7.5	7.5	KΩ
Input Impedance	Open Loop	0.75	0.75	MΩ

TEST CIRCUIT 1 (A_V = 50)

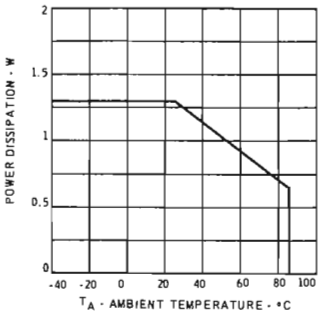


TEST CIRCUIT 2 (A_V = 250)

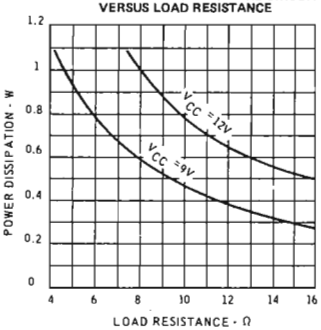


TYPICAL ELECTRICAL CHARACTERISTICS (25°C free air temperature unless otherwise noted)

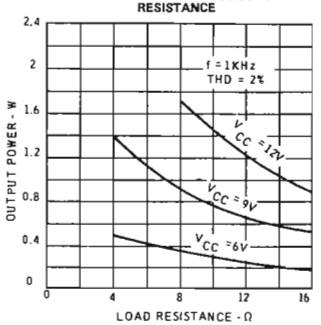
MAX ALLOWABLE POWER DISSIPATION VERSUS AMBIENT TEMPERATURE



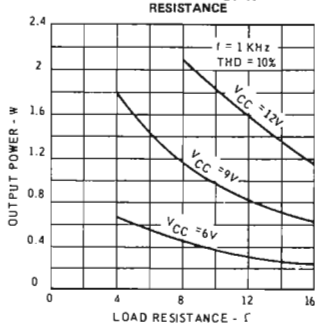
MAX POWER DISSIPATED BY THE CIRCUIT VERSUS LOAD RESISTANCE



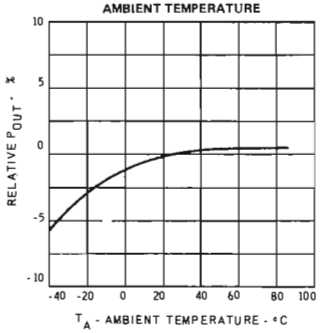
OUTPUT POWER VERSUS LOAD RESISTANCE



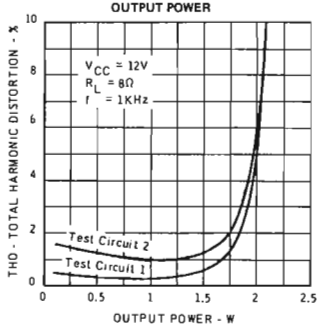
OUTPUT POWER VERSUS LOAD RESISTANCE



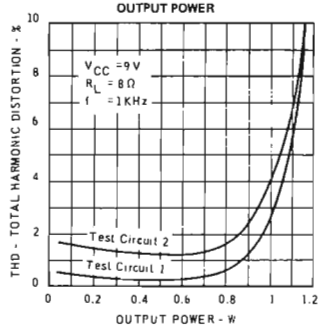
VARIATION OF P_{OUT} VERSUS AMBIENT TEMPERATURE



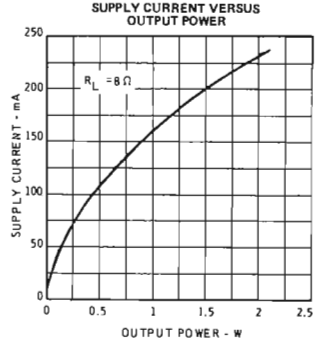
TOTAL HARMONIC DISTORTION VERSUS OUTPUT POWER



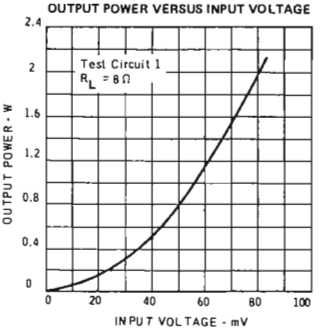
TOTAL HARMONIC DISTORTION VERSUS OUTPUT POWER



SUPPLY CURRENT VERSUS OUTPUT POWER

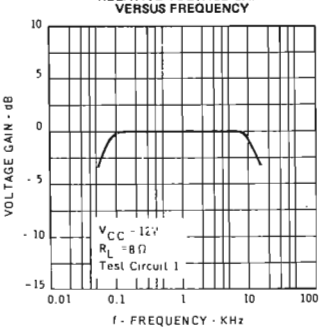


OUTPUT POWER VERSUS INPUT VOLTAGE

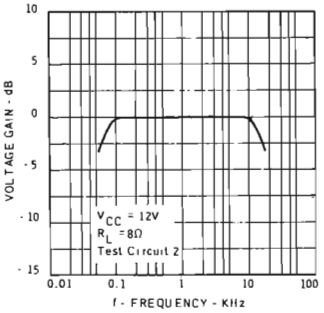


TYPICAL ELECTRICAL CHARACTERISTICS (25 °C free air temperature unless otherwise noted)

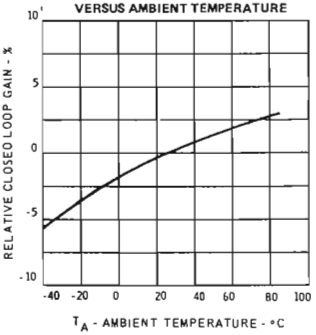
RELATIVE VOLTAGE GAIN VERSUS FREQUENCY



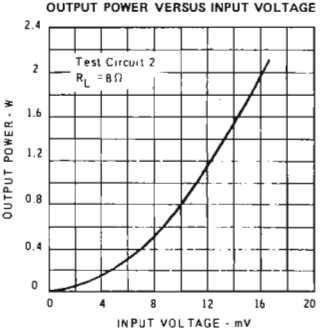
VOLTAGE GAIN VERSUS FREQUENCY



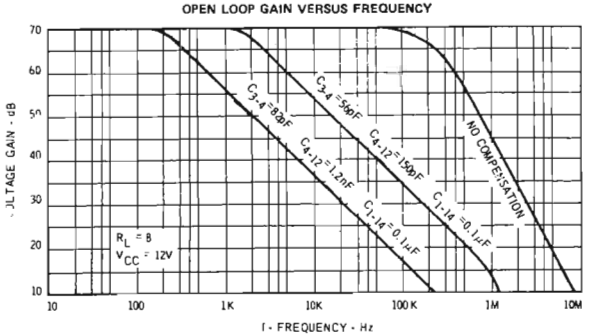
VARIATION OF CLOSED LOOP RELATIVE VERSUS AMBIENT TEMPERATURE



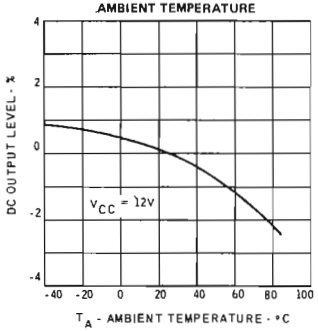
OUTPUT POWER VERSUS INPUT VOLTAGE

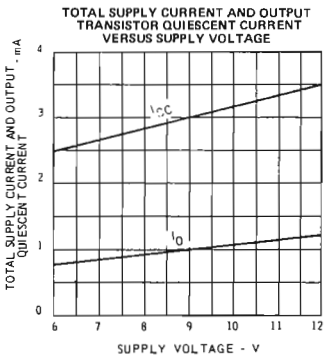


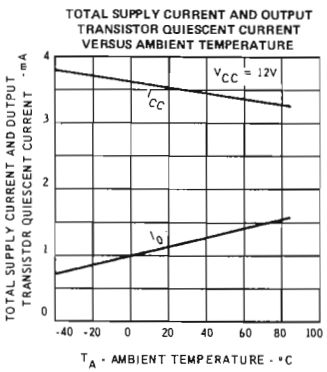
OPEN LOOP GAIN VERSUS FREQUENCY



TYPICAL ELECTRICAL CHARACTERISTICS (25°C free air temperature unless otherwise noted)





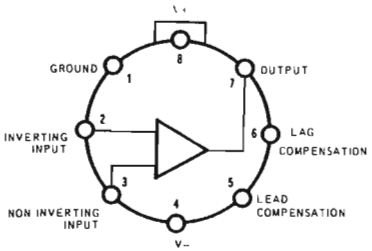


high gain, wideband dc amplifier

EXTENDED TEMPERATURE RANGE, −55°C ÷ 125°C

The μA702A is a complete DC amplifier constructed on a single silicon chip, using the Planar epitaxial process. It is intended for use as an operational amplifier in high speed analog computers, as a precision instrumentation amplifier, or in other applications requiring a feedback amplifier useful from DC to 30 MHz.

CONNECTION DIAGRAM
(Top View)



Note : Pin 4 connected to case

ORDERING NUMBER
U5B771231X

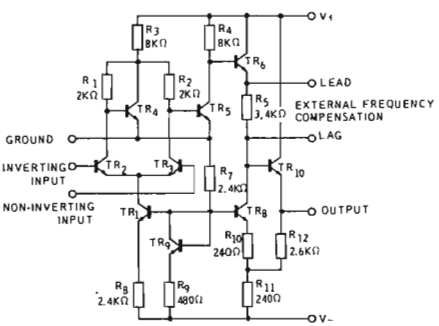
ABSOLUTE MAXIMUM RATINGS
(above which the useful life may be impaired)

Total Supply Voltage Between V + and V− Terminals	21 V
Peak Load Current	50 mA
Internal Power Dissipation (Note 1)	300 mW
Storage Temperature Range	-65°C to + 150°C
Operating Temperature Range	-55°C to + 125°C
Differential Input Voltage	± 5 V
Input Voltage, Either Input	+ 1.5 V to -6V
Lead Temperature (Soldering, 60 sec)	300°C

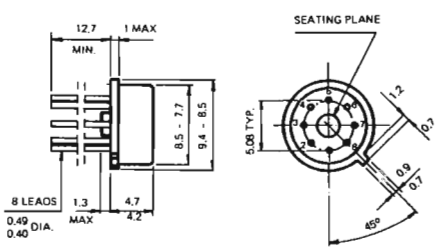
NOTE :

(1) Rating applies for case temperatures to 125°C; derate linearly at 6.6 mW/°C for ambient temperatures above 105°C.

SCHEMATIC DIAGRAM



PHYSICAL DIMENSIONS
in accordance with
JEDEC TO-99 outline



Notes: All dimensions in mm.

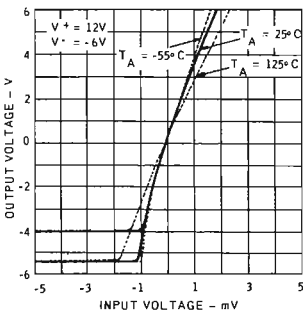
EXTENDED TEMPERATURE RANGE

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

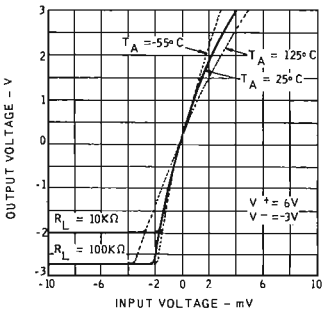
PARAMETER (see definitions)	CONDITIONS	V+ = 12V, V− = -6 V			V+ = 6 V, V− = -3V			
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNIT
Input Offset Voltage	$R_S \leq 2$ kΩ		0.5	2		0.7	3	mV
Input Offset Current			180	500		120	500	nA
Input Bias Current			2	5		1.2	3.5	μA
Input Resistance		16	40		22	67		kΩ
Input Voltage Range		-4		0.5	-1.5		0.5	V
Common Mode Rejection Ratio	$R_S \leq 2$ kΩ, f = 1 kHz	80	100		80	100		dB
Large-Signal Voltage Gain	$R_L \geq 100$ kΩ, $V_{out} = \pm 5$V	2500	3600	6000				
	$R_L \geq 100$ kΩ, $V_{out} = \pm 2.5$V				600	900	1500	
Output Resistance			200	500		300	700	Ω
Supply Current	$V_{out} = 0$		5	6.7		2.1	3.3	mA
Power Consumption	$V_{out} = 0$		90	120		19	30	mW
Transient Response (unity-gain)	$C_1 = 0{,}01$ μF, $R_1 = 20$ Ω, $R_L \geq 100$ kΩ, $V_{in} = 10$ mV							
Risetime			25	120				ns
Overshoot	$C_L \leq 100$ pF		10	50				%
Transient Response (x100 gain)	$C_3 = 50$ pF, R_L 100 kΩ $V_{in} = 1$ mV							
Risetime			10	30				ns
Overshoot			20	40				%
The following specifications apply for -55°C ≤ T_A ≤ 125°C:								
Input Offset Voltage	$R_S \leq 2$ kΩ			3			4	mV
Average Temperature Coefficient of Input Offset Voltage	$R_S \leq 50$ Ω, T_A = 25°C to T_A = 125°C		2.5	10		3.5	15	μV/°C
	$R_S = 50$ Ω, T_A = 25°C to T_A = -55°C		2	10		3	15	μV/°C
Input Offset Current	T_A = 125°C		80	500		50	500	nA
	T_A = -55°C		400	1500		280	1500	nA
Average Temperature Coefficient of Input Offset Current	T_A = 25°C to T_A = 125°C		1	5		0.7	4	nA/°C
	T_A = 25°C to T_A = -55°C		3	16		2	13	nA/°C
Input Bias Current	T_A = -55°C		4.3	10		2.6	7.5	μA
Input Resistance		6			8			kΩ
Common Mode Rejection Ratio	$R_S \leq 2$ kΩ, f ≤ 1 kHz	70	95		70	95		dB
Supply Voltage Rejection Ratio	V+ = 12V, V− = -6 V to V+ = 6 V, V− = -3 V, $R_S \leq 2$ KΩ		75	200		75	200	μV/V
Large-Signal Voltage Gain	$R_L \geq 100$ kΩ, $V_{out} = \pm 5$V	2000		7000				
	$R_L \geq 100$ kΩ, $V_{out} = \pm 2.5$V				500		1750	
Output Voltage Swing	$R_L \geq 100$ kΩ	±5	±5.3		±2.5	±2.7		V
	$R_L \geq 10$ kΩ	±3.5	±4		±1.5	±2		V
Supply Current	T_A = 125°C, $V_{out} = 0$		4.4	6.7		1.7	3.3	mA
	T_A = -55°C, $V_{out} = 0$		5	7.5		2,1	3.9	mA
Power Consumption	T_A = 125°C, $V_{out} = 0$		80	120		15	30	mW
	T_A = -55°C, $V_{out} = 0$		90	135		19	35	mW

TYPICAL ELECTRICAL CHARACTERISTICS (25°C free air temperature unless otherwise noted)

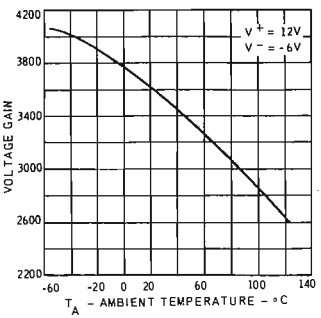
VOLTAGE TRANSFER CHARACTERISTIC



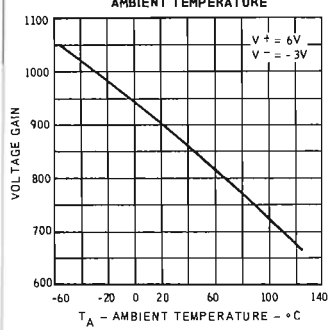
VOLTAGE TRANSFER CHARACTERISTIC



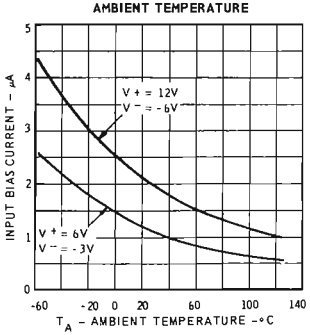
VOLTAGE GAIN VERSUS AMBIENT TEMPERATURE



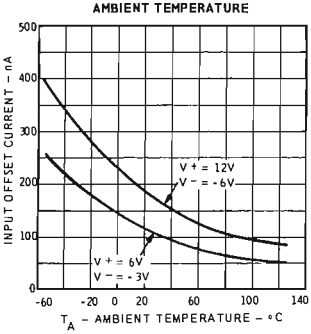
VOLTAGE GAIN VERSUS AMBIENT TEMPERATURE



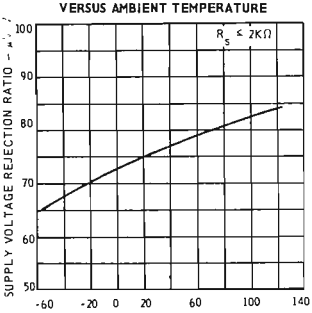
INPUT BIAS CURRENT VERSUS AMBIENT TEMPERATURE



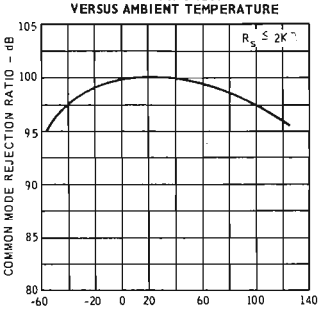
INPUT OFFSET CURRENT VERSUS AMBIENT TEMPERATURE



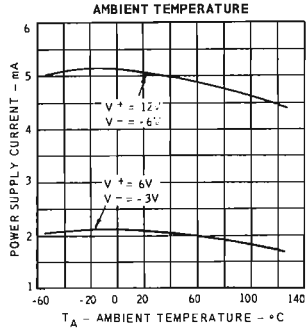
SUPPLY VOLTAGE REJECTION RATIO VERSUS AMBIENT TEMPERATURE



COMMON MODE REJECTION RATIO VERSUS AMBIENT TEMPERATURE

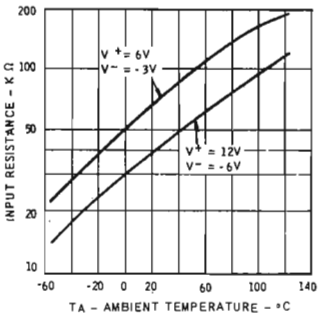


POWER SUPPLY CURRENT VERSUS AMBIENT TEMPERATURE

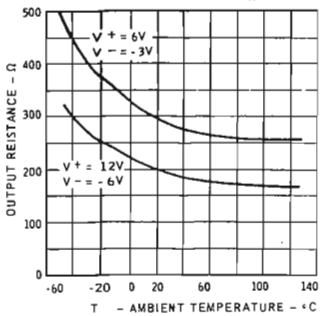


TYPICAL ELECTRICAL CHARACTERISTICS (25°C free air temperature unless otherwise noted)

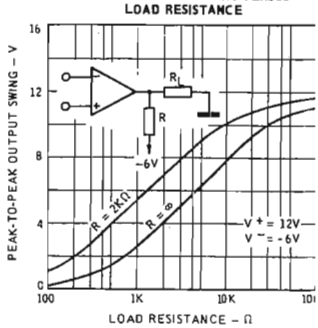
INPUT RESISTANCE VERSUS AMBIENT TEMPERATURE



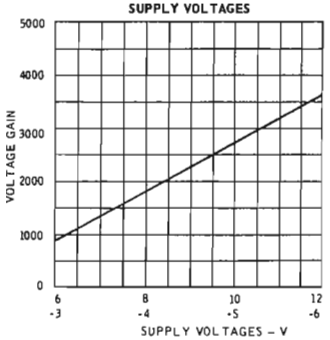
OUTPUT RESISTANCE VERSUS AMBIENT TEMPERATURE



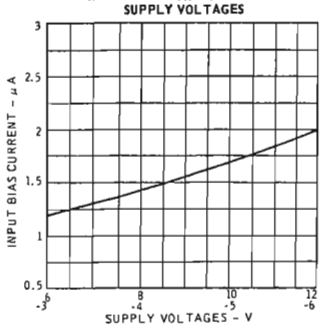
OUTPUT VOLTAGE SWING VERSUS LOAD RESISTANCE



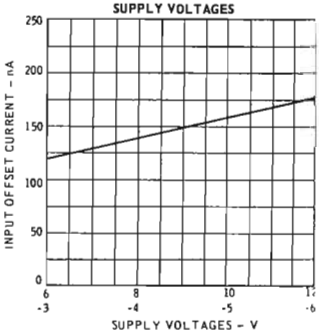
VOLTAGE GAIN VERSUS SUPPLY VOLTAGES



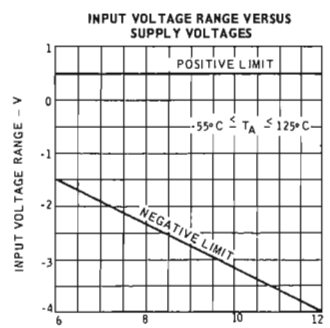
INPUT BIAS CURRENT VERSUS SUPPLY VOLTAGES



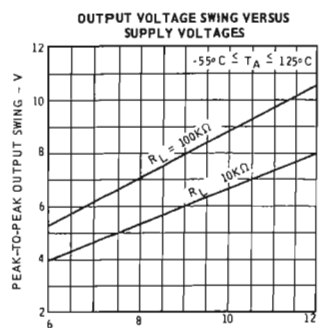
INPUT OFFSET CURRENT VERSUS SUPPLY VOLTAGES



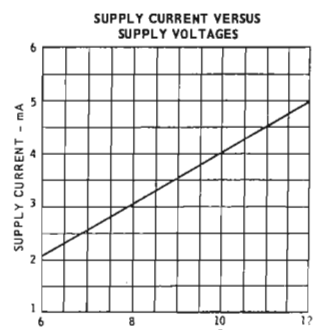
INPUT VOLTAGE RANGE VERSUS SUPPLY VOLTAGES



OUTPUT VOLTAGE SWING VERSUS SUPPLY VOLTAGES

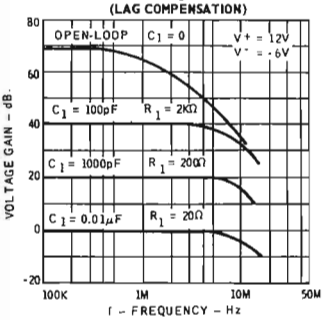


SUPPLY CURRENT VERSUS SUPPLY VOLTAGES

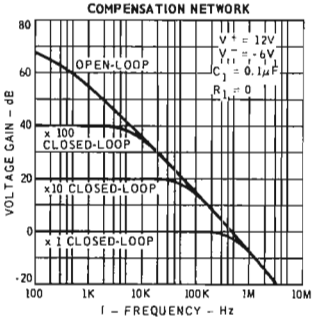


TYPICAL ELECTRICAL CHARACTERISTICS (25°C free air temperature unless otherwise noted)

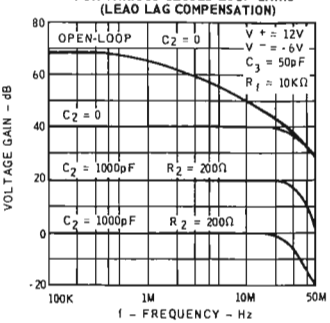
FREQUENCY RESPONSE FOR VARIOUS CLOSED-LOOP GAINS (LAG COMPENSATION)



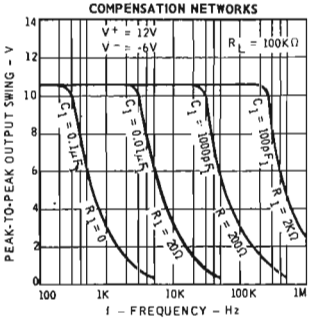
FREQUENCY RESPONSE WITH CONSERVATIVE COMPENSATION NETWORK



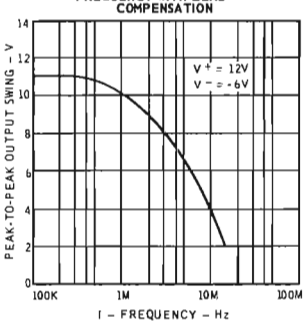
FREQUENCY RESPONSE FOR VARIOUS CLOSED-LOOP GAINS (LEAO LAG COMPENSATION)



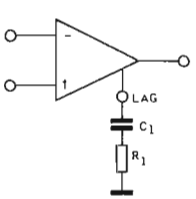
OUTPUT VOLTAGE SWING VERSUS FREQUENCY FOR VARIOUS LAG COMPENSATION NETWORKS



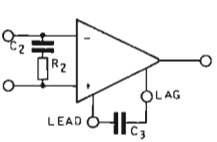
OUTPUT VOLTAGE SWING VERSUS FREQUENCY WITH LEAD-LAG COMPENSATION



FREQUENCY COMPENSATION CIRCUITS



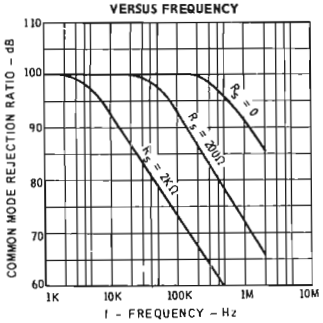
LAG COMPENSATION



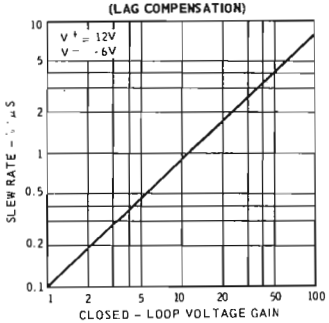
LEAD-LAG COMPENSATION

TYPICAL ELECTRICAL CHARACTERISTICS (25°C free air temperature unless otherwise noted)

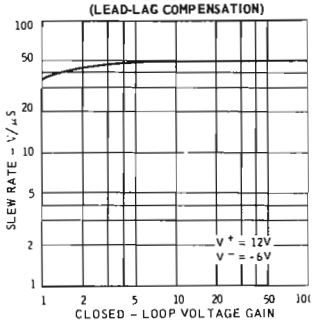
COMMON MODE REJECTION RATIO VERSUS FREQUENCY



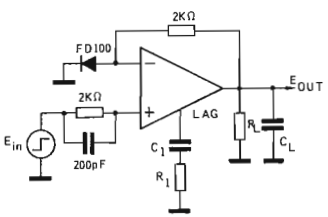
SLEW RATE VERSUS CLOSED-LOOP VOLTAGE GAIN (LAG COMPENSATION)



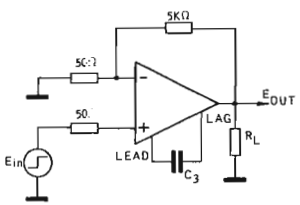
SLEW RATE VERSUS CLOSED-LOOP VOLTAGE GAIN (LEAD-LAG COMPENSATION)



TRANSIENT RESPONSE TEST CIRCUIT

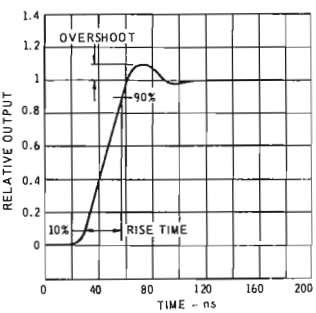


UNITY-GAIN AMPLIFIER (LAG COMPENSATION)



X 100 AMPLIFIER (LEAD COMPENSATION)

TRANSIENT RESPONSE



DEFINITION OF TERMS

INPUT OFFSET VOLTAGE - That voltage which must be applied between the input terminals to obtain zero output voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT OFFSET CURRENT - The difference in the currents into the two input terminals with the output at zero volts.

INPUT RESISTANCE - The resistance looking into either input terminal with the other grounded.

INPUT BIAS CURRENT - The average of the two input currents.

INPUT VOLTAGE RANGE - The range of voltage which, if exceeded on either input terminal, could cause the amplifier to cease functioning properly.

INPUT COMMON MODE REJECTION RATIO - The ratio of the input voltage range to the maximum change in input offset voltage over this range.

SUPPLY VOLTAGE REJECTION RATIO - The ratio of the change in input offset voltage to the change in supply voltage producing it.

LARGE-SIGNAL VOLTAGE GAIN - The ratio of the maximum output voltage swing with load to the change in input voltage required to drive the output from zero to this voltage.

OUTPUT VOLTAGE SWING - The peak output swing, referred to zero, that can be obtained without clipping.

OUTPUT RESISTANCE - The resistance seen looking into the output terminal with the output at null. This parameter is defined only under small signal conditions at frequencies above a few hundred cycles to eliminate the influence of drift and thermal feedback.

POWER CONSUMPTION - The DC power required to operate the amplifier with the output at zero and with no load current.

TRANSIENT RESPONCE - The closed - loop step - function response of the amplifier under small - signal conditions.

PEAK OUTPUT CURRENT - The maximum current that may flow in the output load without causing damage to the unit.

High gain, wideband dc amplifier

STANDARD TEMPERATURE RANGE,
0°C to 70°C

- HIGH GAIN
- WIDEBAND (DC to 30 MHz)

The μA702C is a complete DC amplifier constructed on a single silicon chip, using the planar epitaxial process. It is intended for use as an operational amplifier in high speed analogue computers, as a precision instrumentation amplifier, or in other applications requiring a feedback amplifier usable from DC to 30 MHz. For full temperature range operation (-55°C to 125°C) see μA702A data sheet.

ORDERING NUMBERS

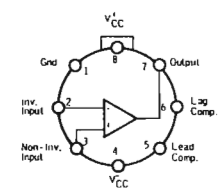
U5B771239X (for package No. 1)
U6E7712393 (for package No. 2)

ABSOLUTE MAXIMUM RATINGS
(above which the useful life may be impaired)

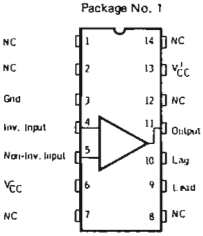
Total Supply Voltage Between V^+_{CC} and V^-_{CC} Terminals	21 V
Peak Load Current	50 mA
Internal Power Dissipation (see note)	300 mW
Storage Temperature Range	-55°C to + 150°C
Operating Temperature Range	0°C to + 70°C
Differential Input Voltage	± 5 V
Input Voltage, Either Input	+ 1.5V to - 6 V
Lead Temperature	
(Soldering 60 sec. for package No. 1)	300°C
(Soldering 10 sec. for package No. 2)	260°C

Note : rating applies for ambient temperature to 70°C.

CONNECTION DIAGRAMS
(top view)

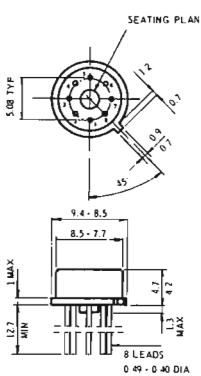


Package No. 1



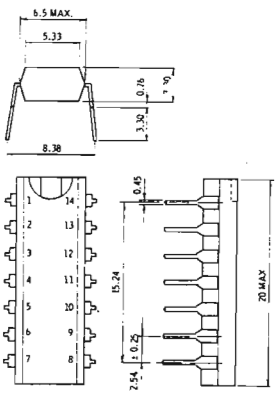
Package No. 2

PACKAGE No. 1
PHYSICAL DIMENSIONS
in accordance with
JEDEC TO-99 outline



Note. all dimensions in mm.

PACKAGE No. 2
PHYSICAL DIMENSIONS
14-pin plastic DIP

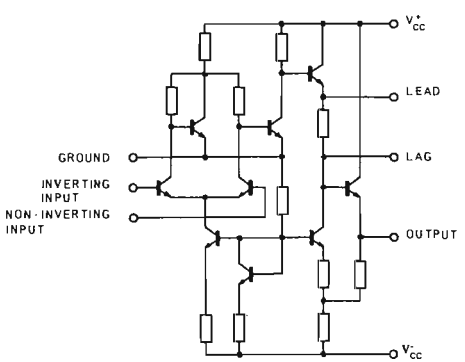


Note: all dimensions in mm.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

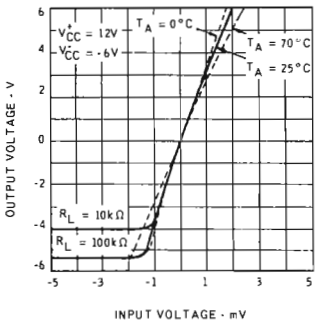
PARAMETER	CONDITIONS	V_{CC}^+=12V, V_{CC}^-=-6V			V_{CC}^+=6V, V_{CC}^-=-3V			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage	$R_S \leq 2\ k\Omega$		±1.5	±5		±1.7	±6	mV
Input Offset Current			±0.5	±2		±0.3	±2	μA
Input Bias Current			2.5	7.5		1.5	5	μA
Input Resistance		10	32		16	55		kΩ
Input Voltage Range		-4		+0.5	-1.5		+0.5	V
Common Mode Rejection Ratio	$R_S \leq 2\ k\Omega$, $f \leq 1$ kHz	70	92		70	92		dB
Large-Signal Voltage Gain	$R_L \geq 100\ k\Omega$, $V_{OUT} = \pm 5V$	2000	3400	6000				
	$R_L \geq 100\ k\Omega$, $V_{OUT} = \pm 2.5V$				500	800	1500	
Output Resistance			200	600		300	800	Ω
Supply Current	$V_{OUT} = 0$		5	6.7		2.1	3.3	mA
Power Consumption	$V_{OUT} = 0$		90	120		19	30	mW
Transient Response (unity gain):	$R_L \leq 100\ k\Omega$, V_{IN}=20mV, $C_L \leq 100$pF							
Rise Time	C_1= 0.01 μF, R_1 = 20 Ω		25	120				ns
Overshoot			10	50				%
Transient Response (x 100 gain):	C_3=50 pF, $R_L \geq 100\ k\Omega$, V_{IN}=1 mV							
Rise Time			10	30				ns
Overshoot			20	40				%
The following specifications apply for 0°C ≤ T_A ≤ 70°C :								
Input Offset Voltage	$R_S \leq 2\ k\Omega$			±6.5			±7.5	mV
Average Temperature Coefficient of Input Offset Voltage	T_A=70°C to T_A= 0°C, R_S=50 Ω		5	20		7.5	25	μV/°C
Input Offset Current				2.5			2.5	μA
Average Temperature Coefficient of Input Offset Current	T_A=25°C to T_A= 70°C		4	10		3	8	nA/°C
	T_A=25°C to T_A= 0°C		6	20		5.5	18	nA/°C
Input Bias Current	T_A= 0°C		4	12		2.7	8	μA
Input Resistance		6	18		9	27		kΩ
Common Mode Rejection Ratio	$R_S \leq 2\ k\Omega$, $f \leq 1$ kHz	65	86		65	86		dB
Supply Voltage Rejection Ratio	V_{CC}^+=12V, V_{CC}^-=-6V, to V_{CC}^+=6V, V_{CC}^-=-3V, $R_S \leq 2\ k\Omega$		90	300		90	300	μV/V
Large-Signal Voltage Gain	$R_L \geq 100\ k\Omega$, $V_{OUT} = \pm 5V$	1500		7000				
	$R_L \geq 100\ k\Omega$, $V_{OUT} = \pm 2.5V$				400		1750	
Output Voltage Swing	$R_L \geq 100\ k\Omega$	±5	±5.3		±2.5	±2.7		V
	$R_L \geq 10\ k\Omega$	±3.5	±4		±1.5	±2		V
Supply Current	$V_{OUT} = 0$		5	7		2.1	3.9	mA
Power Consumption	$V_{OUT} = 0$		90	125		19	35	mW

EQUIVALENT CIRCUIT

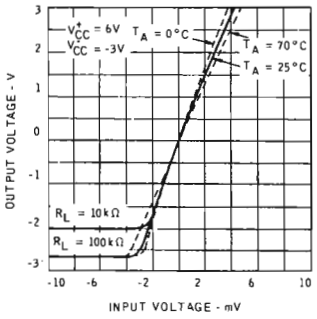


TYPICAL ELECTRICAL CHARACTERISTICS (25°C free air temperature unless otherwise noted)

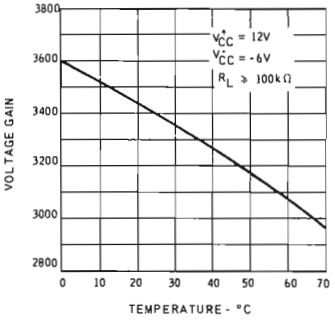
VOLTAGE TRANSFER CHARACTERISTIC



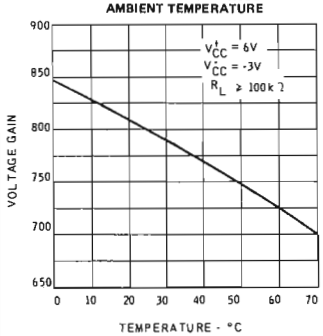
VOLTAGE TRANSFER CHARACTERISTIC



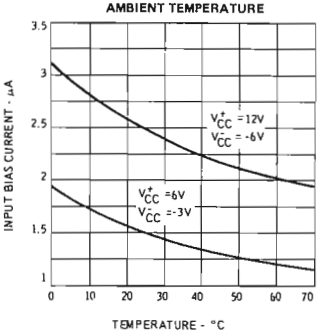
VOLTAGE GAIN VERSUS AMBIENT TEMPERATURE



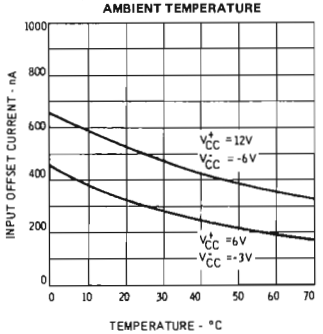
VOLTAGE GAIN VERSUS AMBIENT TEMPERATURE



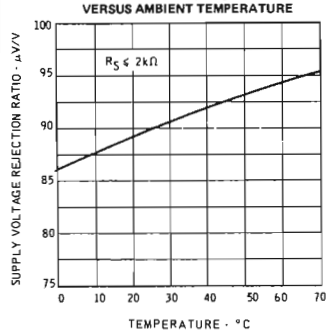
INPUT BIAS CURRENT VERSUS AMBIENT TEMPERATURE



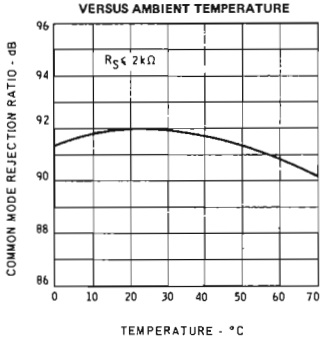
INPUT OFFSET CURRENT VERSUS AMBIENT TEMPERATURE



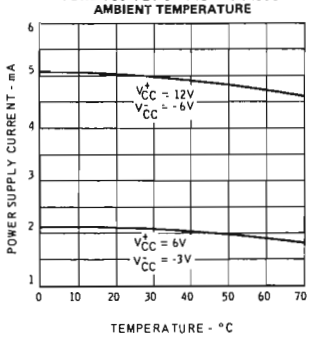
SUPPLY VOLTAGE REJECTION RATIO VERSUS AMBIENT TEMPERATURE



COMMON MODE REJECTION RATIO VERSUS AMBIENT TEMPERATURE

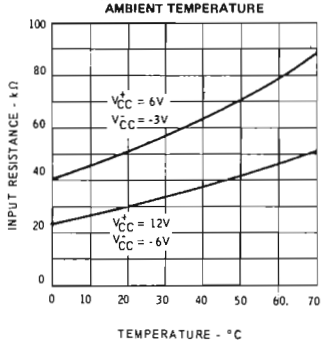


POWER SUPPLY CURRENT VERSUS AMBIENT TEMPERATURE

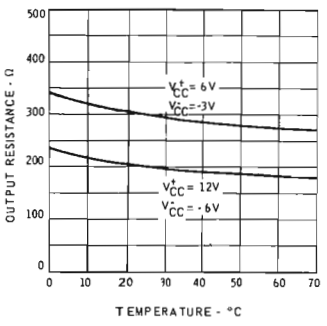


TYPICAL ELECTRICAL CHARACTERISTICS (25°C free air temperature unless otherwise noted)

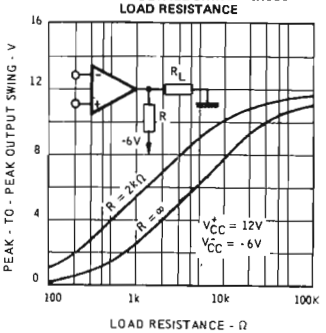
INPUT RESISTANCE VERSUS AMBIENT TEMPERATURE



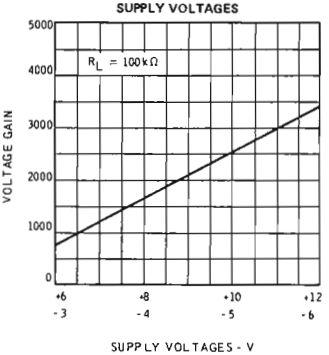
OUTPUT RESISTANCE VERSUS AMBIENT TEMPERATURE



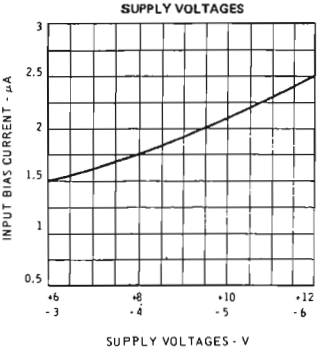
OUTPUT VOLTAGE SWING VERSUS LOAD RESISTANCE



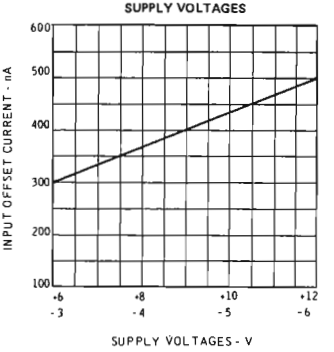
VOLTAGE GAIN VERSUS SUPPLY VOLTAGES



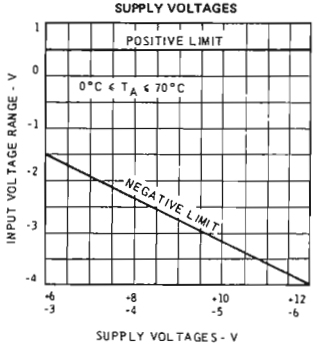
INPUT BIAS CURRENT VERSUS SUPPLY VOLTAGES



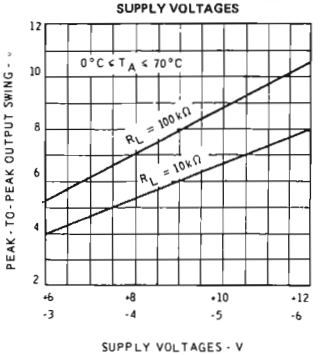
INPUT OFFSET CURRENT VERSUS SUPPLY VOLTAGES



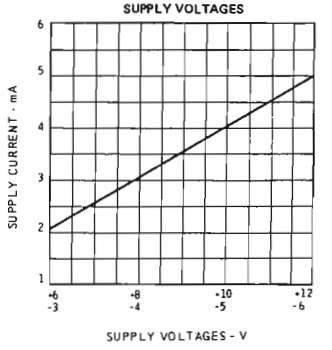
INPUT VOLTAGE RANGE VERSUS SUPPLY VOLTAGES



OUTPUT VOLTAGE SWING VERSUS SUPPLY VOLTAGES

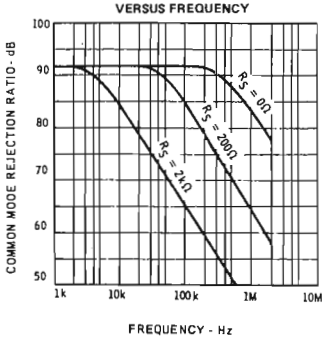


SUPPLY CURRENT VERSUS SUPPLY VOLTAGES

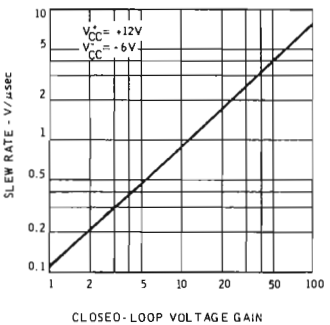


TYPICAL ELECTRICAL CHARACTERISTICS (25°C free air temperature unless otherwise noted)

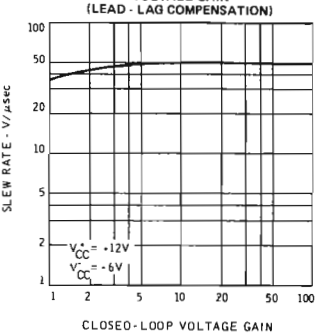
COMMON MODE REJECTION RATIO VERSUS FREQUENCY



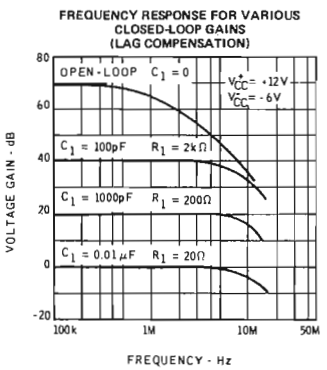
SLEW RATE VERSUS CLOSED-LOOP VOLTAGE GAIN (LAG COMPENSATION)



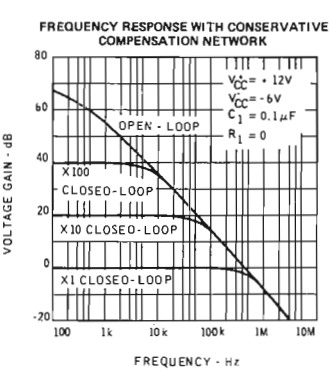
SLEW RATE VERSUS CLOSED-LOOP VOLTAGE GAIN (LEAD-LAG COMPENSATION)



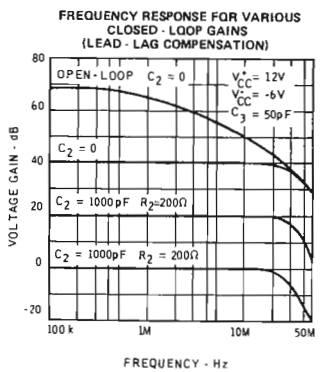
FREQUENCY RESPONSE FOR VARIOUS CLOSED-LOOP GAINS (LAG COMPENSATION)



FREQUENCY RESPONSE WITH CONSERVATIVE COMPENSATION NETWORK

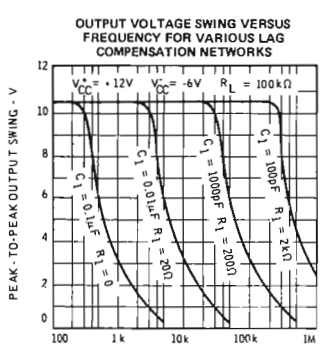


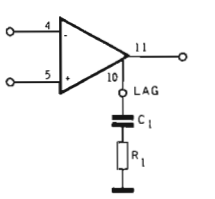
FREQUENCY RESPONSE FOR VARIOUS CLOSED-LOOP GAINS (LEAD-LAG COMPENSATION)



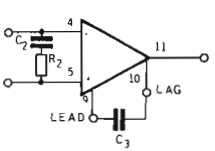
FREQUENCY COMPENSATION CIRCUITS

OUTPUT VOLTAGE SWING VERSUS FREQUENCY FOR VARIOUS LAG COMPENSATION NETWORKS



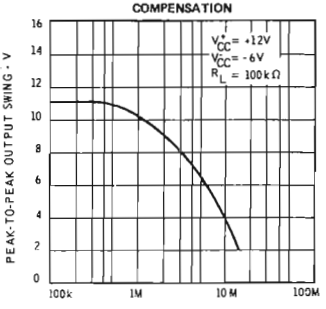


LAG COMPENSATION

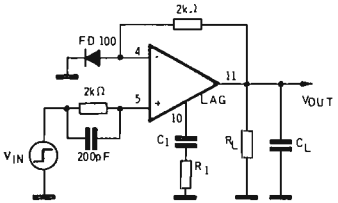


LEAD-LAG COMPENSATION

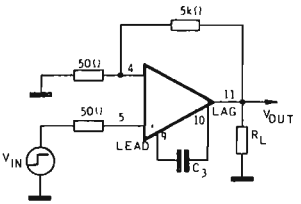
OUTPUT VOLTAGE SWING VERSUS FREQUENCY WITH LEAD-LAG COMPENSATION



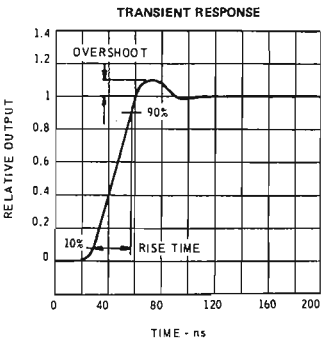
TRANSIENT RESPONSE TEST CIRCUITS



UNITY-GAIN AMPLIFIER
(LAG COMPENSATION)



X 100 AMPLIFIER
(LEAD COMPENSATION)



DEFINITION OF TERMS

INPUT OFFSET VOLTAGE – That voltage which must be applied between the input terminals to obtain zero output voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT OFFSET CURRENT – The difference in the currents into the two input terminals with the output at zero volts.

INPUT RESISTANCE – The resistance looking into either input terminal with the other grounded.

INPUT BIAS CURRENT – The average of the two input currents.

INPUT VOLTAGE RANGE – The range of voltage which, if exceeded on either input terminal, could cause the amplifier to cease functioning properly.

INPUT COMMON MODE REJECTION RATIO – The ratio of the input voltage range to the maximum change in input offset voltage over this range.

SUPPLY VOLTAGE REJECTION RATIO – The ratio of the change in input offset voltage to the change in supply voltage producing it.

LARGE-SIGNAL VOLTAGE GAIN – The ratio of the maximum output voltage swing with load to the change in input voltage required to drive the output from zero to this voltage.

OUTPUT VOLTAGE SWING – The peak output swing, referred to zero, that can be obtained without clipping.

OUTPUT RESISTANCE – The resistance seen looking into the output terminal with the output at null. This parameter is defined only under small signal conditions at frequencies above a few hundred cycles to eliminate the influence of drift and thermal feedback.

POWER CONSUMPTION – The DC power required to operate the amplifier with the output at zero and with no load current.

TRANSIENT RESPONSE – The closed-loop step-function response of the amplifier under small-signal conditions.

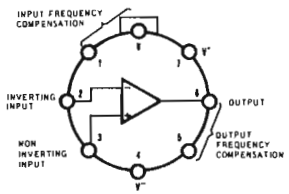
PEAK OUTPUT CURRENT – The maximum current that may flow in the output load without causing damage to the unit.

high performance operational amplifier

EXTENDED TEMPERATURE RANGE, - 55°C + 125°C

The μA709 is a High-Gain Operational amplifier constructed on a single silicon chip using the Planar epitaxial process. It features low offset, high input impedance, large input common mode range, high output swing under load and low power consumption. The device displays exceptional temperature stability and will operate over a wide range of supply voltages with little degradation of performance. The amplifier is intended for use in DC servo systems, high impedance analog computers, in low-level instrumentation applications and for the generation of special linear and nonlinear transfer functions.

CONNECTION DIAGRAM
(Top view)



Note : Pin 4 connected to case.

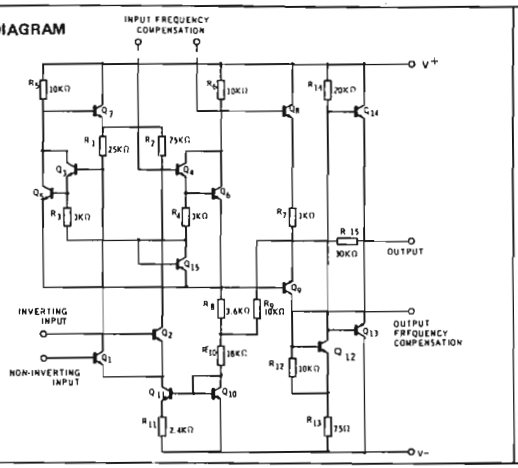
ABSOLUTE MAXIMUM RATINGS
(above which the useful life may be impaired)

Supply Voltage	± 18 V
Internal Power Dissipation (Note 1)	300 mW
Differential Input Voltage	± 5 V
Input Voltage	± 10 V
Output Short-Circuit Duration ($T_A = 25°C$)	5 sec
Storage Temperature Range	-65°C to + 150°C
Operating Ambient Temperature Range	-55°C to + 125°C
Lead Temperature (Soldaring, 60 sec)	300°C

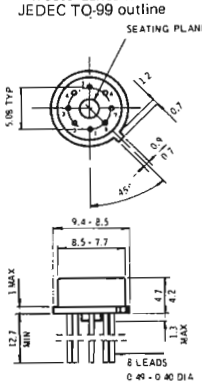
ORDERING NUMBER
U5B770931X

NOTE 1 : Rating applies for case temperatures to + 125°C; derate linearly at 5.5 mW/°C for ambient temperature above + 95°C.

SCHEMATIC DIAGRAM



PHYSICAL DIMENSIONS
in accordance with
JEDEC TO-99 outline



Nota: all dimensions in mm.

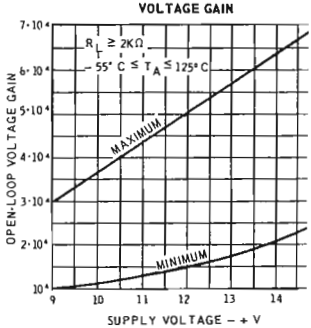
ELECTRICAL CHARACTERISTICS ($T_A = +25°C$, $\pm 9\ V \leq V_S \leq \pm 15\ V$ unless otherwise noted)

PARAMETER (see definitions)	CONDITIONS	Min.	Typ.	Max.	UNIT
Input Offset Voltage	$R_S \leq 10\ K\Omega$		1	5	mV
Input Offset Current			50	200	nA
Input Bias Current			200	500	nA
Input Resistance		150	400		KΩ
Output Resistance			150		Ω
Power Consumption	$V_S = \pm 15V$		80	165	mW
Transient Response	$V_{IN} = 20\ mV$, $R_L = 2\ K\Omega$,				
Risetime	$C_1 = 5000\ pF$, $R_1 = 1.5\ K\Omega$, $C_2 = 200\ pF$, $R_2 = 50\ \Omega$		0.3	1	μs
Overshoot	$C_L \leq 100\ pF$		10	30	%
The following specifications apply for $-55°C \leq T_A \leq +125°C$:					
Input Offset Voltage	$R_S \leq 10\ K\Omega$			6	mV
Average Temperature Coefficient of Input Offset Voltage	$R_S = 50\ \Omega$		3		μV/°C
	$R_S \leq 10\ K\Omega$		6		μV/°C
Large - Signal Voltage Gain	$V_S = \pm 15\ V$, $R_L \geq 2\ K\Omega$, $V_{OUT} = \pm 10\ V$	25,000	45,000	70,000	
Output Voltage Swing	$V_S = \pm 15V$, $R_L \geq 10\ K\Omega$	± 12	± 14		V
	$V_S = \pm 15V$, $R_L \geq 2\ K\Omega$	± 10	± 13		V
Input Voltage Range	$V_S = \pm 15\ V$	± 8	+10		V
Common Mode Rejection Ratio	$R_S \leq 10\ K\Omega$	70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10\ K\Omega$		25	150	μV/C
Input Offset Current	$T_A = +125°C$		20	200	nA
	$T_A = -55°C$		100	500	nA
Input Bias Current	$T_A = -55°C$		0.5	1.5	μA
Input Resistance		40	100		KΩ

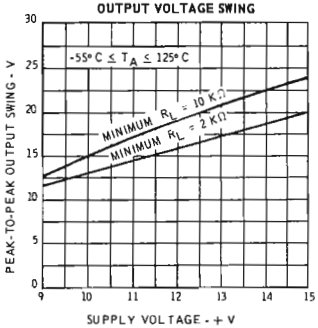
GUARANTEED ELECTRICAL CHARACTERISTICS

(25°C free air temperature unless otherwise noted)

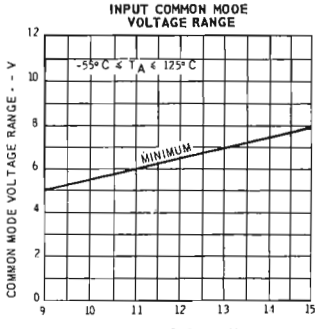
VOLTAGE GAIN



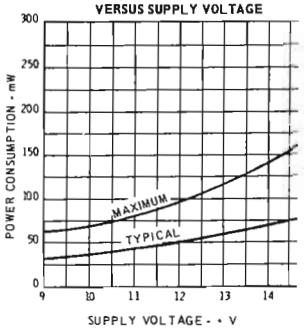
OUTPUT VOLTAGE SWING



INPUT COMMON MODE VOLTAGE RANGE

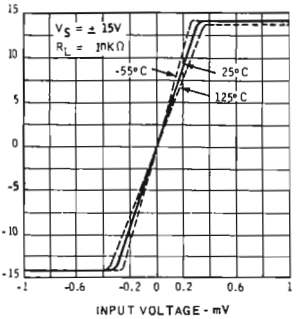


POWER CONSUMPTION VERSUS SUPPLY VOLTAGE

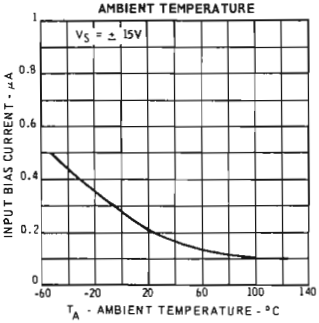


YPICAL ELECTRICAL CHARACTERISTICS (25°C free air temperature unless otherwise noted)

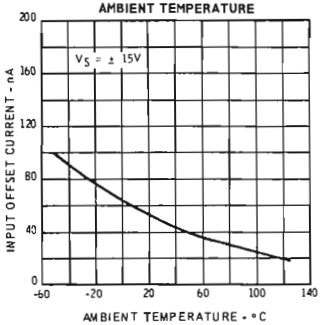
VOLTAGE TRANSFER CHARACTERISTIC



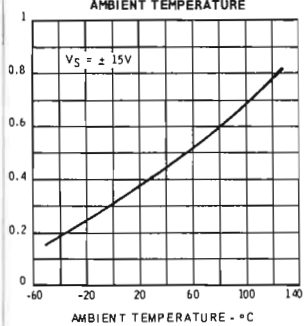
INPUT BIAS CURRENT VERSUS AMBIENT TEMPERATURE



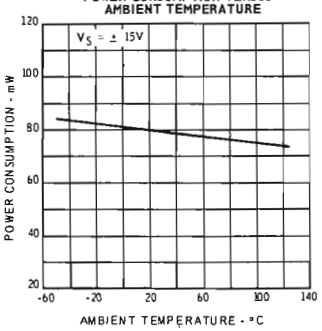
INPUT OFFSET CURRENT VERSUS AMBIENT TEMPERATURE



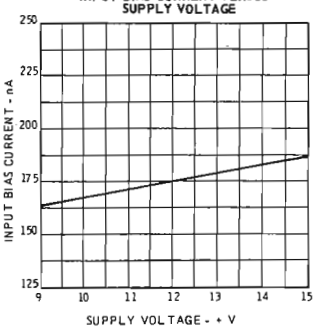
INPUT RESISTANCE VERSUS AMBIENT TEMPERATURE



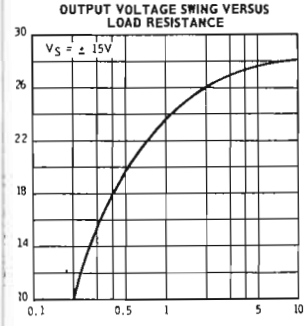
POWER CONSUMPTION VERSUS AMBIENT TEMPERATURE



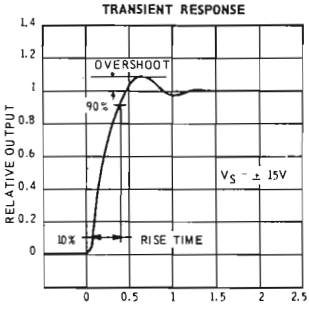
INPUT BIAS CURRENT VERSUS SUPPLY VOLTAGE



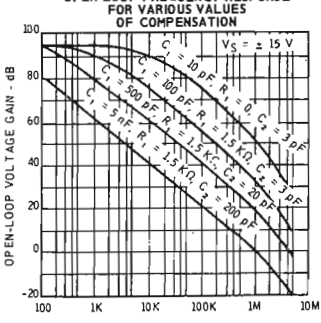
OUTPUT VOLTAGE SWING VERSUS LOAD RESISTANCE



TRANSIENT RESPONSE

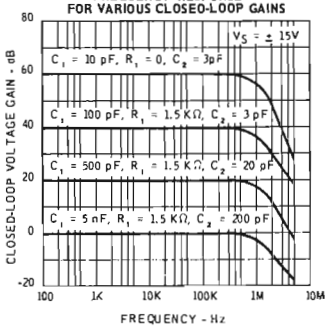


OPEN-LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF COMPENSATION

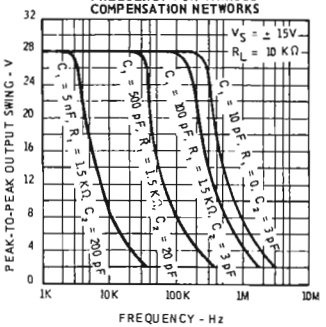


TYPICAL ELECTRICAL CHARACTERISTICS (25°C free air temperature unless otherwise noted)

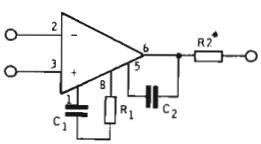
FREQUENCY RESPONSE FOR VARIOUS CLOSED-LOOP GAINS



OUTPUT VOLTAGE SWING VERSUS FREQUENCY FOR VARIOUS COMPENSATION NETWORKS

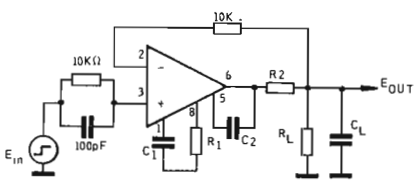


FREQUENCY COMPENSATION CIRCUIT



* Use R_2 = 50Ω when the amplifier is operated with capacitive Loading

TRANSIENT RESPONSE TEST CIRCUIT



DEFINITION OF TERMS

INPUT OFFSET VOLTAGE - That voltage which must be applied between the input terminals to obtain zero output voltage. The input offset vo ge may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT OFFSET CURRENT - The difference in the currents into the two input terminals with the output at zero volts.

INPUT RESISTANCE - The resistance looking into either input terminal with the other grounded.

INPUT BIAS CURRENT - The average of the two input currents.

INPUT VOLTAGE RANGE - A range of voltage which, if exceeded on either input terminal, could cause the amplifier to cease functioning p perly.

INPUT COMMON MODE REJECTION RATIO - The ratio of the input voltage range to the maximum change in input offset voltage over this ra

LARGE-SIGNAL VOLTAGE GAIN - The ratio of the maximum output voltage swing with load to the change in input voltage required to drive output from zero to this voltage.

OUTPUT VOLTAGE SWING - The peak output swing, referred to zero, that can be obtained without clipping.

OUTPUT RESISTANCE - The resistance seen looking into the output terminal with the output at null. This parameter is defined only under s signal conditions at frequencies above a few hundred cycles to eliminate the influence of drift and thermal feedback.

POWER CONSUMPTION - The DC power required to operate the amplifier with the output at zero and with no load current.

SUPPLY VOLTAGE REJECTION RATIO - The ratio of the change in input offset voltage to the change in supply voltage producing it.

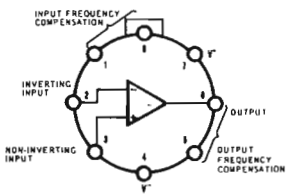
TRANSIENT RESPONSE - The closed - loop step function response of the amplifier under small - signal conditions.

high performance operational amplifier

EXTENDED TEMPERATURE RANGE, - 55°C + 125°C

The μA709A is a High-Gain Operational amplifier constructed on a single silicon chip using the Planar epitaxial process. It features low offset, high input impedance, large input common mode range, high output swing under load and low power consumption. The device displays exceptional temperature stability and will operate over a wide range of supply voltages with little degradation of performance. The amplifier is intended for use in DC servo systems, high impedance analog computers, in low-level instrumentation applications and for the generation of special linear and nonlinear transfer functions.

CONNECTION DIAGRAM
(Top view)



Note : Pin 4 connected to case.

ORDERING NUMBER

U5B 7709311

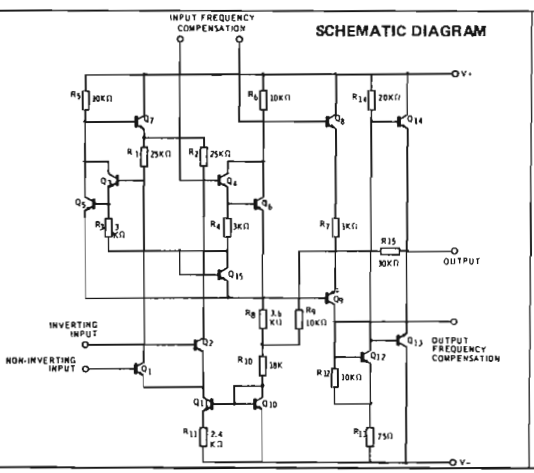
ABSOLUTE MAXIMUM RATINGS
(above which the useful life may be impaired)

Supply Voltage	±18V
Internal Power Dissipation (Note 1)	300 mW
Differential Input Voltage	±5 V
Input Voltage	±10 V
Output Short - Circuit Duration ($T_A = 25°C$)	5 sec
Storage Temperature Range	- 65°C to 150°C
Operating Ambient Temperature Range	- 55°C to 125°C
Lead Temperature (Soldering, 60 sec)	300°C

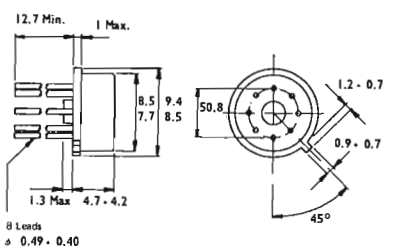
NOTE 1:

Rating applies for case temperatures to 125°C; derate linearly at 5.6 mW/°C for ambient temperatures above 95°C.

SCHEMATIC DIAGRAM



PHYSICAL DIMENSIONS
similar to
Jedec TO 99 outline



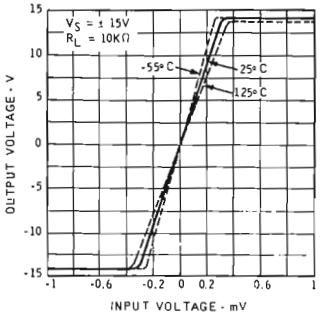
Notes : All dimensions in mm.
Leads are gold-plated Kovar.

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$, $\pm 9\ V \leq V_S \leq \pm 15V$ unless otherwise specified)

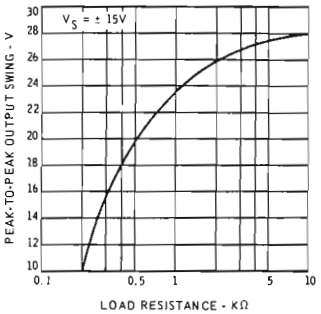
PARAMETER (see definitions)	CONDITIONS	Min.	Typ.	Max.	UNIT
Input Offset Voltage	$R_S \leq 10\ k\Omega$		0.6	2	mV
Input Offset Current			10	50	nA
Input Bias Current			100	200	nA
Input Resistance		350	700		kΩ
Output Resistance			150		Ω
Supply Current	$V_S = \pm 15\ V$		2.5	3.6	mA
Power Consumption	$V_S = \pm 15\ V$		75	108	mW
Transient Response	$V_S = \pm 15\ V$, $V_{IN} = 20\ mV$, $R_L = 2\ k\Omega$, $C_1 = 5\ nF$, $R_1 = 1.5\ k\Omega$, $C_2 = 200\ pF$, $R_2 = 50\ \Omega$				
Risetime				1.5	μsec
Overshoot	$C_L \leq 100\ pF$			30	%
The following specifications apply for $-55°C \leq T_A \leq 125°C$:					
Input Offset Voltage	$R_S \leq 10\ k\Omega$			3	mV
Average Temperature Coefficient	$R_S = 50\ \Omega$, $T_A = 25°C$ to $T_A = 125°C$		1.8	10	μV/°C
of Input Offset Voltage	$R_S = 50\ \Omega$, $T_A = 25°C$ to $T_A = -55°C$		1.8	10	μV/°C
	$R_S = 10\ k\Omega$, $T_A = 25°C$ to $T_A = 125°C$		2	15	μV/°C
	$R_S = 10\ k\Omega$, $T_A = 25°C$ to $T_A = -55°C$		4.8	25	μV/°C
Input Offset Current	$T_A = 125°C$		3.5	50	nA
	$T_A = -55°C$		40	250	nA
Average Temperature Coefficient	$T_A = 25°C$ to $T_A = 125°C$		0.08	0.5	nA/°C
of Input Offset Current	$T_A = 25°C$ to $T_A = -55°C$		0.45	2.8	nA/°C
Input Bias Current	$T_A = -55°C$		300	600	nA
Input Resistance	$T_A = -55°C$	85	170		kΩ
Input Voltage Range	$V_S = \pm 15\ V$	± 8			V
Common Mode Rejection Ratio	$R_S \leq 10\ k\Omega$	80	110		dB
Supply Voltage Rejection Ratio	$R_S \leq 10\ k\Omega$		40	100	μV/V
Large - Signal Voltage Gain	$V_S = \pm 15\ V$, $R_L \geq 2\ k\Omega$, $V_{OUT} = \pm 10V$	25,000		70,000	
Output Voltage Swing	$V_S = \pm 15V$, $R_L \geq 10\ k\Omega$	± 12	± 14		V
	$V_S = \pm 15\ V$, $R_L \geq 2\ k\Omega$	± 10	± 13		V
Supply Current	$T_A = 125°C$, $V_S = \pm 15\ V$		2.1	3	mA
	$T_A = -55°C$, $V_S = \pm 15\ V$		2.7	4.5	mA
Power Consumption	$T_A = 125°C$, $V_S = \pm 15\ V$		63	90	mW
	$T_A = -55°C$, $V_S = \pm 15\ V$		81	135	mW

TYPICAL ELECTRICAL CHARACTERISTICS (25°C free air temperature unless otherwise noted)

VOLTAGE TRANSFER CHARACTERISTIC

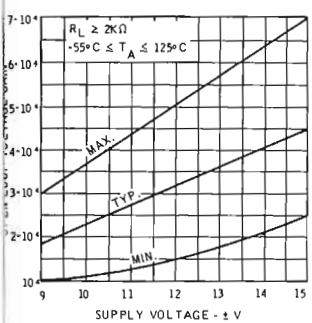


OUTPUT VOLTAGE SWING VERSUS LOAD RESISTANCE

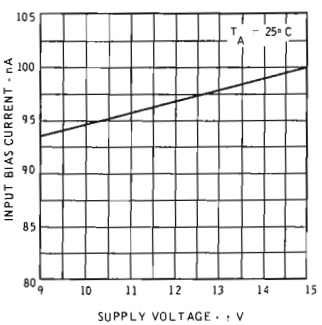


DC CHARACTERISTICS AS A FUNCTION OF SUPPLY VOLTAGE

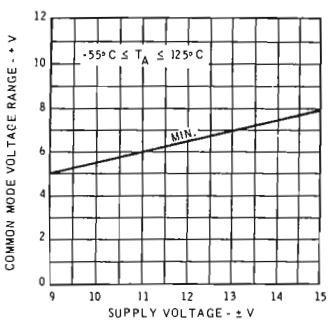
VOLTAGE GAIN



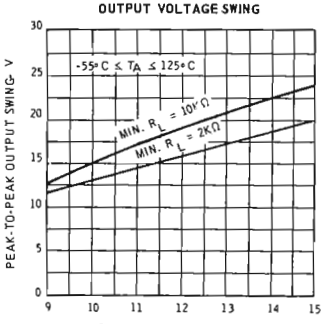
INPUT BIAS CURRENT VERSUS SUPPLY VOLTAGE



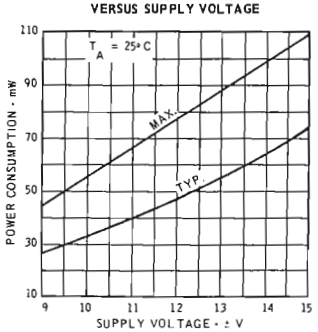
INPUT COMMON MODE VOLTAGE RANGE



OUTPUT VOLTAGE SWING

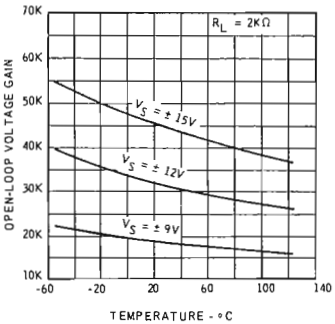


POWER CONSUMPTION VERSUS SUPPLY VOLTAGE

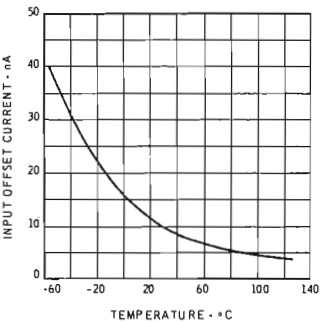


DC CHARACTERISTICS AS A FUNCTION OF AMBIENT TEMPERATURE

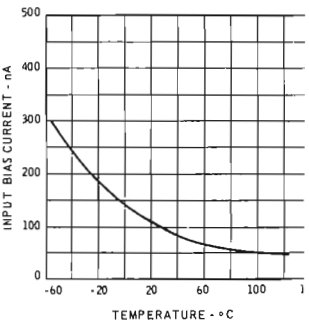
VOLTAGE GAIN VERSUS AMBIENT TEMPERATURE



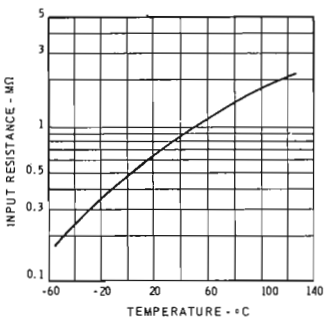
INPUT OFFSET CURRENT VERSUS AMBIENT TEMPERATURE



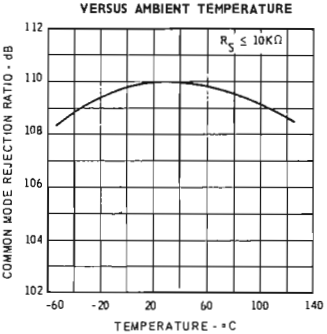
INPUT BIAS CURRENT VERSUS AMBIENT TEMPERATURE



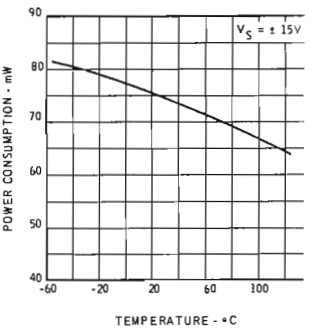
INPUT RESISTANCE VERSUS AMBIENT TEMPERATURE



COMMON MODE REJECTION RATIO VERSUS AMBIENT TEMPERATURE

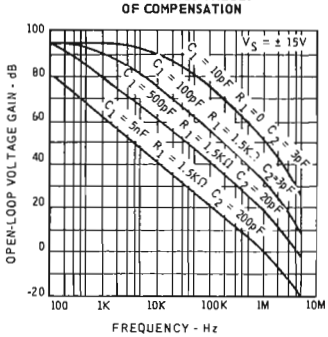


POWER CONSUMPTION VERSUS AMBIENT TEMPERATURE

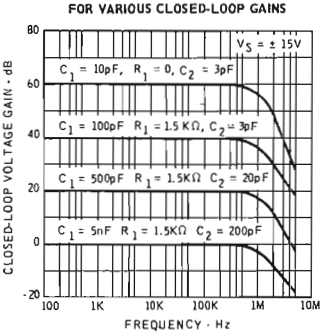


AC CHARACTERISTICS

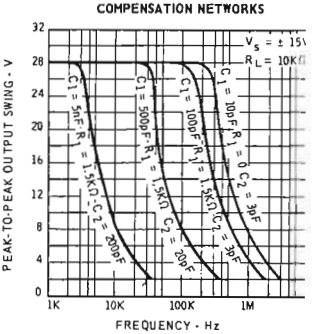
OPEN-LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF COMPENSATION



FREQUENCY RESPONSE FOR VARIOUS CLOSED-LOOP GAINS

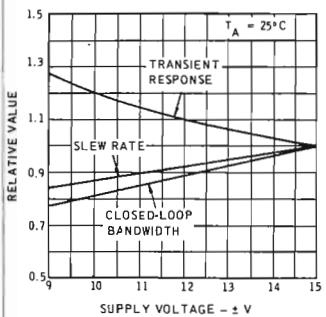


OUTPUT VOLTAGE SWING VERSUS FREQUENCY FOR VARIOUS COMPENSATION NETWORKS

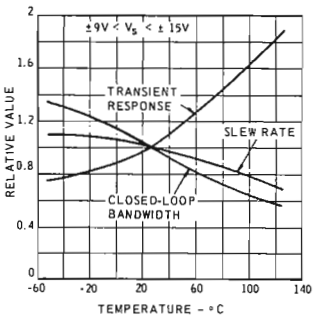


AC CHARACTERISTICS

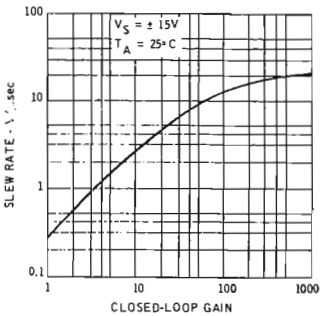
FREQUENCY CHARACTERISTICS VERSUS SUPPLY VOLTAGE



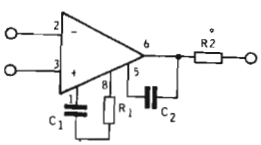
FREQUENCY CHARACTERISTICS VERSUS AMBIENT TEMPERATURE



SLEW RATE VERSUS CLOSED-LOOP GAIN USING RECOMMENDED COMPENSATION NETWORKS

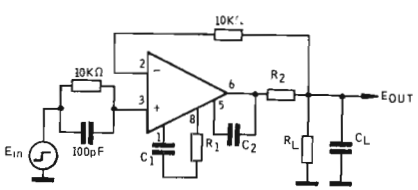


FREQUENCY COMPENSATION CIRCUIT

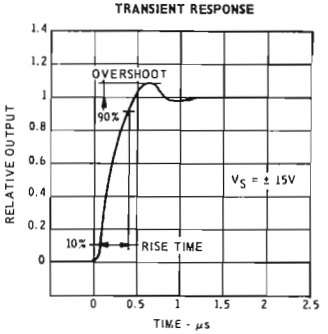


° Use R_2 = 50Ω when the amplifier is operated with capacitive Loading

TRANSIENT RESPONSE TEST CIRCUIT



TRANSIENT RESPONSE



DEFINITION OF TERMS

INPUT OFFSET VOLTAGE - That voltage which must be applied between the input terminals to obtain zero output voltage. The input offset volt age may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT OFFSET CURRENT - The difference in the currents into the two input terminals with the output at zero volts.

INPUT RESISTANCE - The resistance looking into either input terminal with the other grounded.

INPUT BIAS CURRENT - The average of the two input currents.

INPUT VOLTAGE RANGE - A range of voltage which, if exceeded on either input terminal, could cause the amplifier to cease functioning properly

INPUT COMMON MODE REJECTION RATIO - The ratio of the input voltage range to the maximum change in input offset voltage over this rang

LARGE-SIGNAL VOLTAGE GAIN - The ratio of the maximum output voltage swing with load to the change in input voltage required to drive t output from zero to this voltage.

OUTPUT VOLTAGE SWING - The peak output swing, referred to zero, that can be obtained without clipping.

OUTPUT RESISTANCE - The resistance seen looking into the output terminal with the output at null. This parameter is defined only under sma signal conditions at frequencies above a few hundred cycles to eliminate the influence of drift and thermal feedback.

POWER CONSUMPTION - The DC power required to operate the amplifier with the output at zero and with no load current.

SUPPLY VOLTAGE REJECTION RATIO - The ratio of the change in input offset voltage to the change in supply voltage producing it.

TRANSIENT RESPONSE - The closed - loop step function response of the amplifier under small - signal conditions.

High performance operational amplifier

STANDARD TEMPERATURE RANGE
0°C to 70°C

- LOW OFFSET
- HIGH INPUT IMPEDANCE
- LOW POWER CONSUMPTION

The μA709C is a high-gain operational amplifier constructed on a single silicon chip using the planar epitaxial process. It features low offset, high input impedance, large input common mode range, high output swing under load and low power consumption. The device displays exceptional temperature stability and will operate over a wide range of supply voltages with little degradation of performance. The amplifier is intended for use in DC servo systems, high impedance analogue computers, in low-level instrumentation applications and for the generation of special linear and nonlinear transfer functions. For full temperature range operation (-55°C to +125°C) see μa709 data sheet.

ABSOLUTE MAXIMUM RATINGS
(above which the useful life may be impaired)

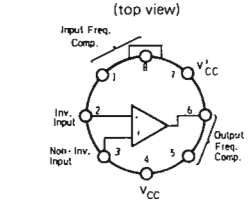
Supply Voltage	± 18 V
Internal Power Dissipation (see note)	300 mW
Differential Input Voltage	± 5 V
Input Voltage	± 10V
Output Short-Circuit Duration (T_A=25°C)	5 sec
Storage Temperature Range	-55°C to +150°C
Operating Temperature Range	0°C to + 70°C
Lead Temperature	
(Soldering 60 sec for package No. 1)	300°C
(Soldering 10 sec for package No. 2)	260°C

Note : rating applies for ambient temperature to + 70°C

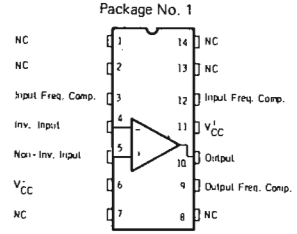
ORDERING NUMBERS

U5B770939X (for package No. 1)
U6E7709393 (for package No. 2)

CONNECTION DIAGRAMS
(top view)

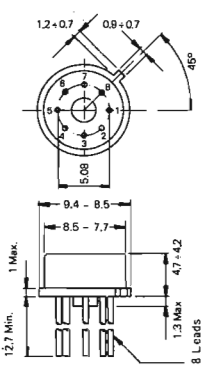


Package No. 1



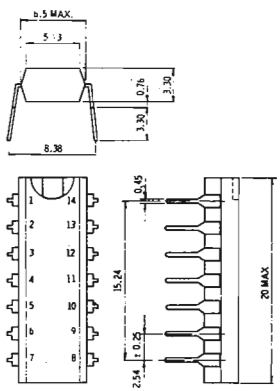
Package No. 2

PACKAGE No. 1
PHYSICAL DIMENSIONS
similar to
Jedec TO 99 outline



Note : All dimensions in mm.

PACKAGE No. 2
PHYSICAL DIMENSIONS
14- pin plastic DIP

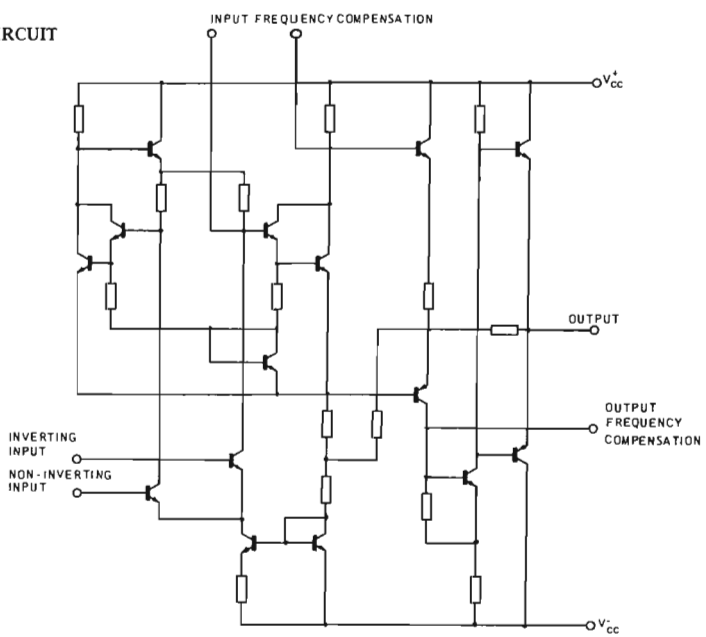


Note: all dimensions in mm.

ELECTRICAL CHARACTERISTICS (V_{CC}= ± 15V, T_A= 25°C unless otherwise specified)

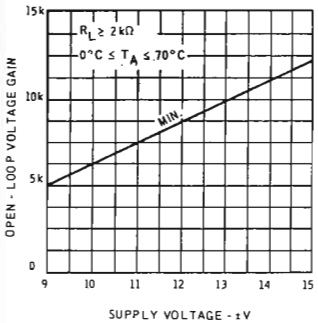
PARAMETER	CONDITIONS	Min.	Typ.	Max.	Unit
Input Offset Voltage	$R_S \leq 10\ k\Omega$, ± 9V ≤ V_{CC} ≤ ± 15V		± 2	± 7.5	mV
Input Offset Current			± 100	±500	nA
Input Bias Current			0.3	1.5	uA
Input Resistance		50	250		kΩ
Output Resistance			150		Ω
Large-Signal Voltage Gain	$R_L \geq 2\ k\Omega$, V_{OUT}= ±10V	15,000	45,000		
Output Voltage Swing	$R_L \geq 10\ k\Omega$	± 12	± 14		V
	$R_L \geq 2\ k\Omega$	± 10	± 13		V
Input Voltage Range		± 8	± 10		V
Common Mode Rejection Ratio	$R_S \leq 10\ k\Omega$	65	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10\ k\Omega$		25	200	μV/V
Power Consumption	V_{OUT} = 0		80	200	mW
Transient Response (Unity Gain)	V_{IN}=20 mV, R_L = 2kΩ, C_1 = 5000 pF				
Rise Time	R_1= 1.5 kΩ, C_2= 200 pF, R_2 = 50 Ω		0.3		μs
Overshoot	$C_L \leq 100$ pF		10		%
The following specifications apply for 0°C ≤ T_A ≤ + 70°C:					
Input Offset Voltage	$R_S \leq 10\ k\Omega$, ±9V ≤ V_{CC} ≤± 15V			± 10	mV
Input Offset Current				±750	nA
Input Bias Current				2	μA
Large-Signal Voltage Gain	$R_L \geq 2\ k\Omega$, V_{OUT}= ± 10V	12,000			
Input Resistance		35			kΩ

EQUIVALENT CIRCUIT

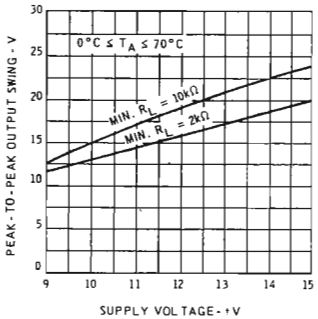


GUARANTEED ELECTRICAL CHARACTERISTICS

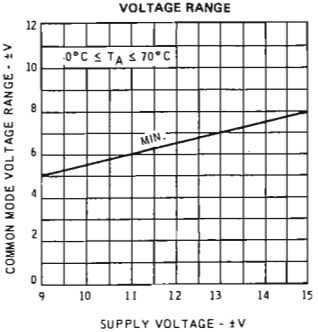
VOLTAGE GAIN



OUTPUT VOLTAGE SWING

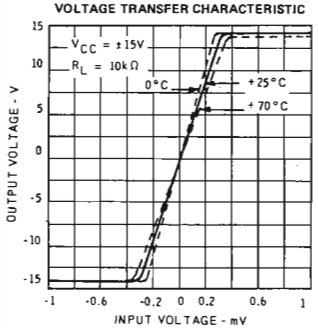


INPUT COMMON MODE VOLTAGE RANGE

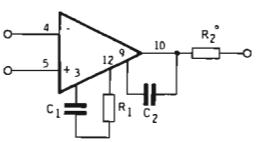


TYPICAL PERFORMANCE CURVES

VOLTAGE TRANSFER CHARACTERISTIC

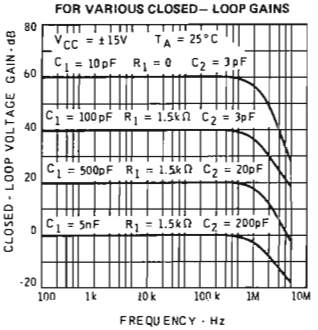


FREQUENCY COMPENSATION CIRCUIT



* Use R_2 = 50Ω when the amplifier is operated with capacitive loading

FREQUENCY RESPONSE FOR VARIOUS CLOSED– LOOP GAINS



DEFINITION OF TERMS

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INPUT OFFSET CURRENT - The difference in the currents into the two input terminals with the output at zero volts.

INPUT RESISTANCE - The resistance looking into either input terminal with the other grounded.

INPUT BIAS CURRENT - The average of the two input currents.

INPUT VOLTAGE RANGE - A range of voltage which, if exceeded on either input terminal, could cause the amplifier to cease functioning properly.

INPUT COMMON MODE REJECTION RATIO - The ratio of the input voltage range to the maximum change in input offset voltage over this range.

LARGE-SIGNAL VOLTAGE GAIN - The ratio of the maximum output voltage swing with load to change in input voltage required to drive the output from zero to this voltage.

OUTPUT VOLTAGE SWING - The peak output swing, referred to zero, that can be obtained without clipping.

OUTPUT RESISTANCE - The resistance seen looking into the output terminal with the output at null. This parameter is defined only under small signal conditions at frequencies above a few hundred cycles to eliminate the influence of drift and thermal feedback.

POWER CONSUMPTION - The DC power required to operate the amplifier with the output at zero and with no load current

SUPPLY VOLTAGE REJECTION RATIO - The ratio of the change in input offset voltage to the change in supply voltage producing it.

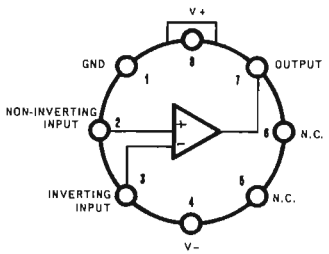
TRANSIENT RESPONSE - The closed-loop step function response of the amplifier under small-signal conditions.

high speed differential comparator

EXTENDED TEMPERATURE RANGE, –55°C ÷ 125°C

The μA 710 is a differential voltage comparator intended for applications requiring high accuracy and fast response times. It is constructed on a single silicon chip using the Planar epitaxial process. The device is useful as a variable threshold Schmitt trigger, a pulse height discriminator, a voltage comparator in high-speed A-D converters, a memory sense amplifier or a high-noise immunity line receiver. The output of the comparator is compatible with all integrated logic forms.

CONNECTION DIAGRAM
(Top View)



Note : Pin 4 connected to case.

ORDERING NUMBER

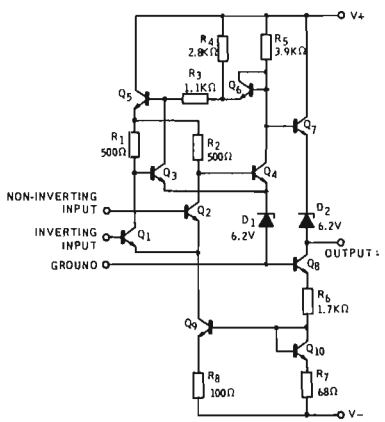
U5B771031X

ABSOLUTE MAXIMUM RATINGS
(above which the useful life may be impaired)

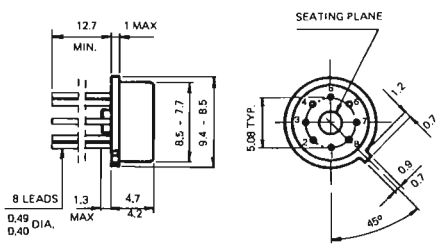
Positive Supply Voltage	14 V
Negative Supply Voltage	7 V
Peak Output Current	10 mA
Differential Input Voltage	± 5 V
Input Voltage	± 7 V
Internal Power Dissipation (Note 1)	300 mW
Operating Temperature Range	-55°C to 125°C
Storage Temperature Range	-65°C to 150°C
Lead Temperature (Soldering, 60 sec)	300°C

NOTES : on the following page.

SCHEMATIC DIAGRAM



PHYSICAL DIMENSIONS
in accordance with
JEDEC TO-99 outline



Notes: All dimensions in mm.

ELECTRICAL CHARACTERISTICS (T_A = +25°C, V^+ = 12V, V^- = -6V unless otherwise specified)

PARAMETER (see definitions)	CONDITIONS	MIN.	TYP.	MAX.	UNIT.
Input Offset Voltage (Note 3)	$R_S \leq 200\,\Omega$		0.6	2	mV
Input Offset Current (Note 3)			0.75	3	μA
Input Bies Current			13	20	μA
Voltage Gain		1250	1700		
Output Resistance			200		Ω
Output Sink Current	$\Delta V_{in} \geq 5mV$, $V_{out} = 0$	2	2.5		mA
Response Time (Note 2)			40		ns
The following specifications apply for -55°C ≤ T_A ≤ +125°C:					
Input Offset Voltage (Note 3)	$R_S \leq 200\,\Omega$			3	mV
Average Temperature Coefficient of	$R_S = 50\,\Omega$				
Input Offset Voltage	T_A = 25°C to T_A = 125°C		3.5	10	μV/°C
	T_A = 25°C to T_A = -55°C		2.7	10	μV/°C
Input Offset Current (Note 3)	T_A = +125°C		0.25	3	μA
	T_A = -55°C		1.8	7	μA
Average Temperature Coefficient of	T_A = 25°C to T_A = + 125°C		5	25	nA/°C
Input Offset Current	T_A = 25°C to T_A = -55°C		15	75	nA/°C
Input Bias Current	T_A = -55°C		27	45	μA
Input Voltage Range	V^- = -7V	±5			V
Common Mode Rejection Ratio	$R_S \leq 200\,\Omega$	80	100		dB
Differential Input Voltage Range		±5			V
Voltage Gain		1000			
Positive Output Level	$\Delta V_{in} \geq 5mV$, $0 \leq I_{out} \leq 5mA$	2.5	3.2	4	V
Negative Output Level	$\Delta V_{in} \geq 5mV$	-1	-0.5	0	V
Output Sink Current	$\Delta V_{in} \geq 5mV$, $V_{out} = 0$				
	T_A = +125°C	0.5	1.7		mA
	T_A = -55°C	1	2.3		mA
Positive Supply Current	$V_{out} \leq 0$		5.2	9	mA
Negative Supply Current			4.6	7	mA
Power Consumption			90	150	mW

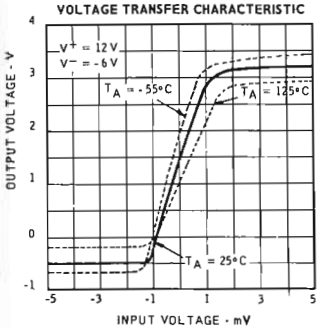
NOTES:

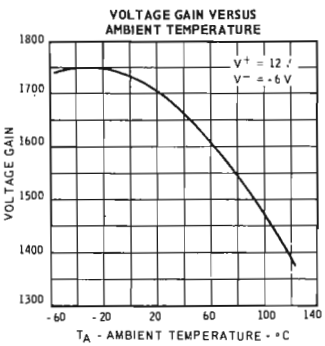
(1) Rating applies for case temperatures to +125°C; derate linearly at 6.6 mW/°C for ambient temperatures above +105°C.

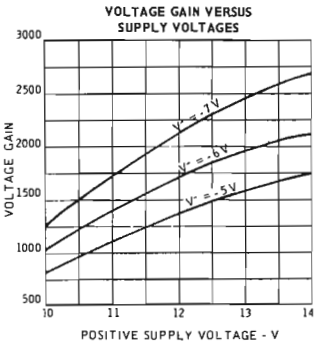
(2) The response time specified (see definitions) is for a 100 mV input step with 5mV overdrive.

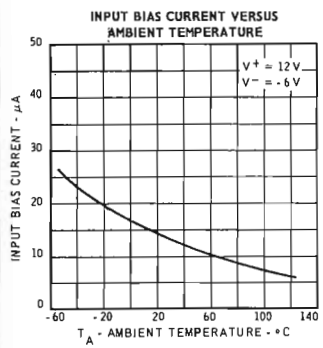
(3) The input offset voltage and input offset current (see definitions) are specified for a logic threshold voltage of 1.8V at -55°C, 1.4V at + 25°C and 1V at +125°C.

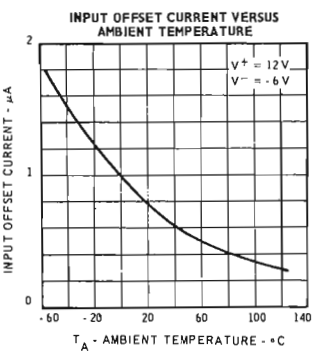
TYPICAL ELECTRICAL CHARACTERISTICS (25°C free air temperature unless otherwise noted)

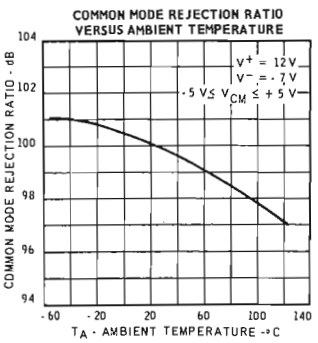


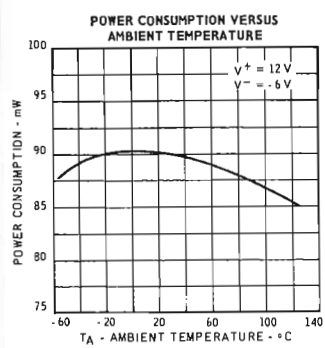


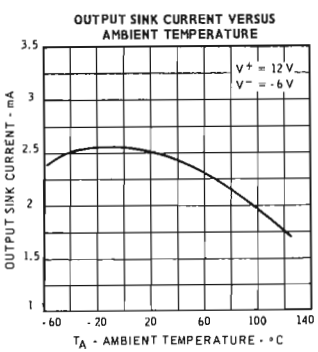


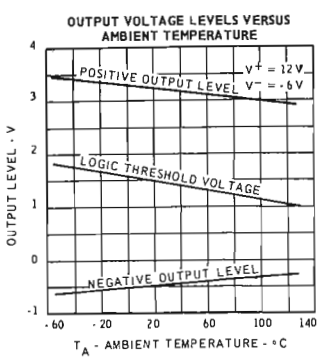




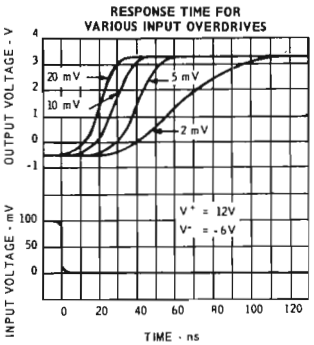


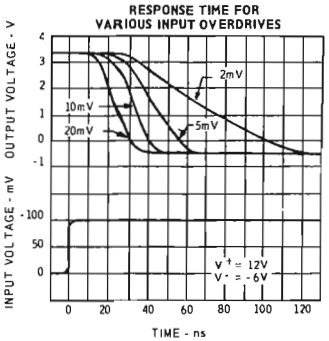


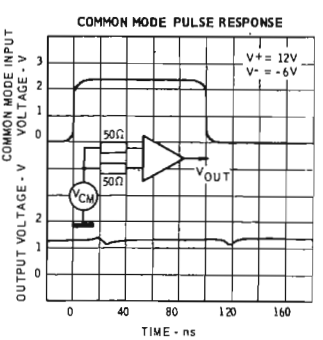




TYPICAL ELECTRICAL CHARACTERISTICS (25°C free air temperature unless otherwise noted)







DEFINITION OF TERMS

LOGIC THRESHOLD VOLTAGE - The approximate voltage at the output of the comparator at which the loading logic circuitry changes its digita state. For the μA 710 this voltage has been fixed at + 1.4V (see note 3).

INPUT OFFSET VOLTAGE - The voltage between the input terminals when the output is at the logic threshold voltage. The input offset voltag may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT OFFSET CURRENT - The difference in the currents into the two input terminals with the output at the logic threshold voltage.

INPUT BIAS CURRENT - The average of the two input currents.

INPUT VOLTAGE RANGE - The range of voltage on the input terminals for which the comparator will operate within specifications.

INPUT COMMON MODE REJECTION RATIO - The ratio of the input voltage range to the maximum change in input offset voltage over this range

DIFFERENTIAL INPUT VOLTAGE RANGE - The range of voltage between the input terminals for which operation within specifications is assured

VOLTAGE GAIN - The ratio of the change in output voltage to the change in voltage between the input terminals producing it with the DC outpu level in the vicinity of the logic threshold voltage.

RESPONSE TIME - The interval between the application of an input step function and the time when the output crosses the logic threshold voltage The input step drives the comparator from some initial, saturated input voltage to an input level just barely in excess of that required to bring the output from saturation to the logic threshold voltage. This excess is referred to as the voltage overdrive.

POSITIVE OUTPUT LEVEL - The DC output voltage in the positive direction with the input voltage equal to or greater than a minimum specifiec amount.

NEGATIVE OUTPUT LEVEL - The DC output voltage in the negative direction with the input voltage equal to or greater than a minimum specifiec amount.

OUTPUT SINK CURRENT - The maximum negative current than can be delivered by the comparator.

PEAK OUTPUT CURRENT - The maximum current that may flow into the output load without causing damage to the comparator.

OUTPUT RESISTANCE - The resistance seen looking into the output terminal with the DC output level at the logic threshold voltage.

POWER CONSUMPTION - The DC power into the amplifier with no output load. The DC power will vary with signal level, but is specified as a maximum for the entire range of input - signal conditions.

High-speed differential comparator

STANDARD TEMPERATURE RANGE,
0°C to 70°C

- IMPROVED SPECIFICATIONS
- 5mV MAXIMUM OFFSET VOLTAGE
- 5 μA MAXIMUM OFFSET CURRENT
- 1000 MINIMUM VOLTAGE GAIN
- 20 μV/°C MAXIMUM OFFSET VOLTAGE DRIFT

The μA 710C is a differential voltage comparator intended for applications requiring high accuracy and fast response times. It is constructed on a single silicon chip using the planar epitaxial process. The device is useful as a variable threshold Schmidt trigger, a pulse height discriminator, a voltage comparator in high-speed A-D converters, a memory sense amplifier or a high-noise immunity line receiver. The output of the comparator is compatible with all integrated logic forms. For full temperature range operation (-55°C to +125°C) see μA 710 data sheet.

ABSOLUTE MAXIMUM RATINGS
(above which the useful life may be impaired)

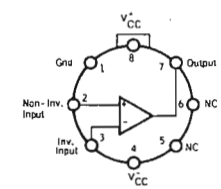
Positive Supply Voltage	14 V
Negative Supply Voltage	-7 V
Peak Output Current	10 mA
Differential Input Voltage	±5 V
Input Voltage	±7 V
Internal Power Dissipation (Note 1)	300 mW
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	-55°C to +150°C
Lead Temperature	
(Soldering 60 sec for package No. 1)	300°C
(Soldering 10 sec for package No. 2)	260°C

ORDERING NUMBERS

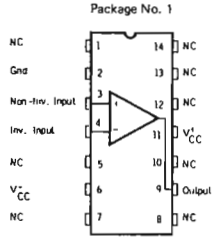
U5B771039X (for package No. 1)
U6E7710393 (for package No. 2)

Notes on the following page.

CONNECTION DIAGRAMS
(top view)

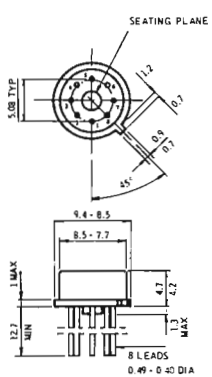


Package No. 1



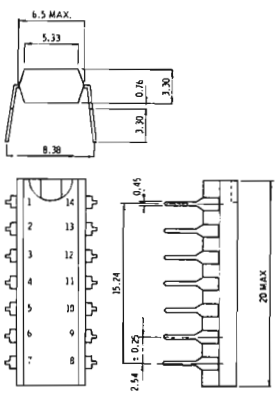
Package No. 2

PACKAGE No. 1
PHYSICAL DIMENSIONS
in accordance with
JEDEC TO-99 outline



Note: all dimensions in mm.

PACKAGE No. 2
PHYSICAL DIMENSIONS
14-pin plastic DIP



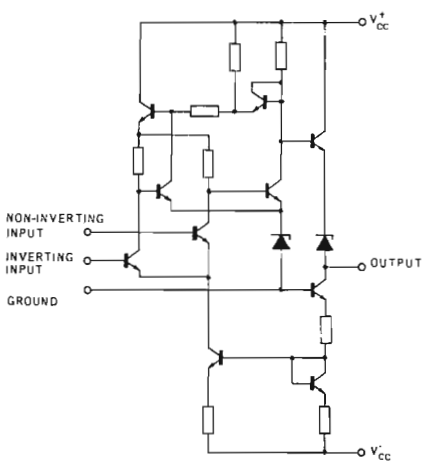
Note: all dimensions in mm.

STANDARD TEMPERATURE RANGE

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC}^+= 12V, V_{CC}^-= -6V unless otherwise specified)

PARAMETER	CONDITIONS (Note 3)	Min.	Typ.	Max.	Unit
Input Offset Voltage (Note 3)	$R_S \leq 200\ \Omega$		± 1.6	± 5	mV
Input Offset Current (Note 3)			± 1.8	± 5	μA
Input Bias Current			16	25	μA
Voltage Gain		1000	1500		
Output Resistance			200		Ω
Output Sink Current	$\Delta V_{IN} \leq$ 5 mV, V_{OUT} = 0	1.6	2.5		mA
Response Time (Note 2)			40		nsec
The following specifications apply for 0°C ≤ T_A ≤ + 70°C:					
Input Offset Voltage (Note 3)	$R_S \leq 200\ \Omega$			± 6.5	mV
Average Temperature Coefficient of Input Offset Voltage	R_S = 50 Ω, T_A = 0°C to T_A = + 70°C		5	20	μV/°C
Input Offset Current (Note 3)				± 7.5	μA
Average Temperature Coefficient of Input Offset Current	T_A = 25°C to T_A = + 70°C		15	50	nA/°C
	T_A = 25°C to T_A = 0°C		24	100	nA/°C
Input Bias Current	T_A = 0°C		25	40	μA
Input Voltage Range	V_{CC}^- = -7V	± 5			V
Common Mode Rejection Ratio	$R_S \leq 200\ \Omega$ V_{CM} = ± 5V	70	98		dB
Differential Input Voltage Range		± 5			V
Voltage Gain		800			
Positive Output Level	$\Delta V_{IN} \geq$ 5 mV, 0 ≤ $I_{OUT} \leq$ 5 mA	2.5	3.2	4	V
Negative Output Level	$\Delta V_{IN} \geq$ 5 mV	-1	-0.5	0	V
Output Sink Current	$\Delta V_{IN} \geq$ 5 mV, V_{OUT} = 0	0.5			mA
Positive Supply Current	$V_{OUT} \leq 0$		5.2	9	mA
Negative Supply Current	$V_{OUT} \leq 0$		-4.6	- 7	mA
Power Consumption	$V_{OUT} \leq 0$		90	150	mW

EQUIVALENT CIRCUIT

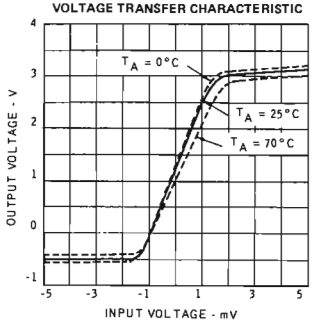


NOTES :

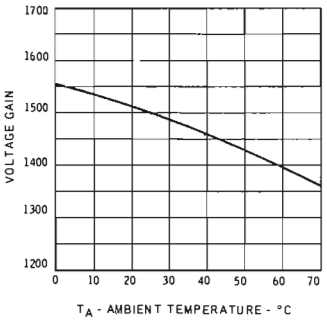
1) Ratings apply for ambient temperature to +70°C.
2) The response time specified (see definitions) is for a 100 mV input step with 5 mV overdrive.
3) The input offset voltage and input offset current (see definitions) are specified for a logic threshold voltage of 1.5V at 0°C, 1.4V at +25°C and 1.2V at +70°C.

TYPICAL ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC}^+ = 12 V, V_{CC}^- = -6 V unless otherwise specified)

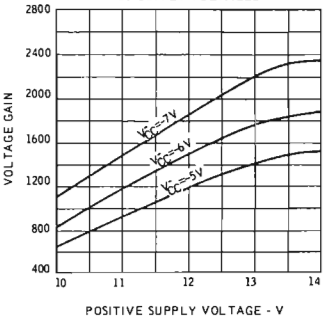
VOLTAGE TRANSFER CHARACTERISTIC



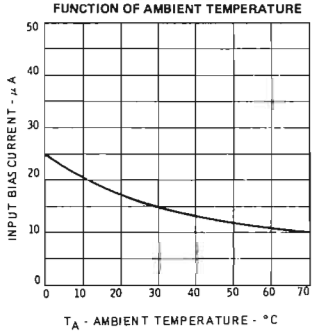
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



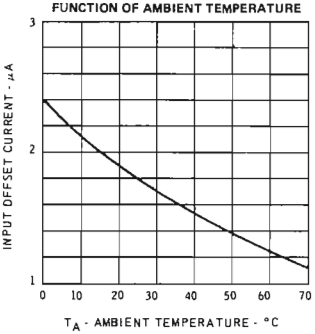
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGES



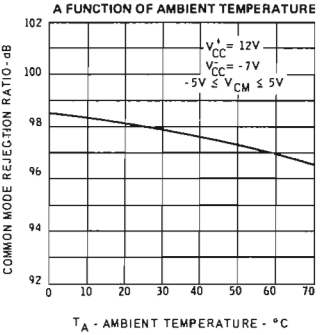
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



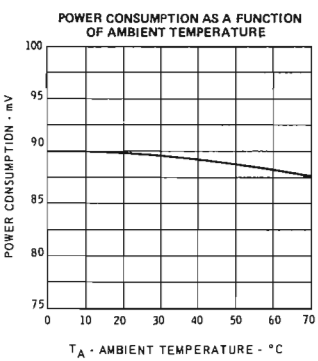
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



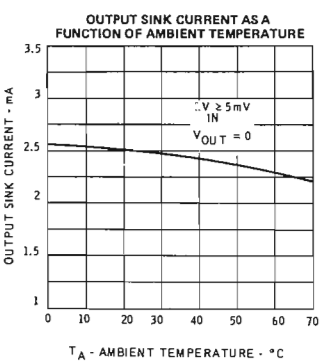
COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



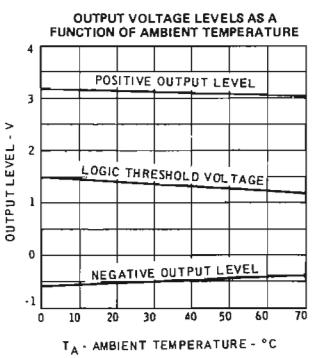
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



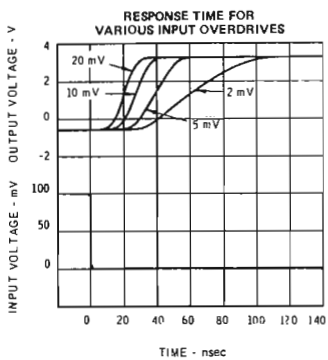
OUTPUT SINK CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

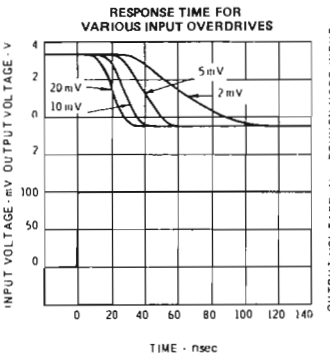


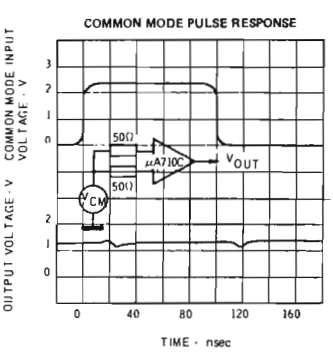
OUTPUT VOLTAGE LEVELS AS A FUNCTION OF AMBIENT TEMPERATURE



TYPICAL ELECTRICAL CHARACTERISTICS (T_A = 25°C, V^+_{CC} = 12V, V^-_{CC} = – 6V unless otherwise specified)







DEFINITION OF TERMS

LOGIC THRESHOLD VOLTAGE – The approximate voltage at the output of the comparator at which the loading logic circuitry changes its digital state.

INPUT OFFSET VOLTAGE – The voltage between the input terminals when the output is at the logic threshold voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT OFFSET CURRENT – The difference in the currents into the two input terminals with the output at the logic threshold voltage.

INPUT BIAS CURRENT – The average of the two inputs currents.

INPUT VOLTAGE RANGE – The range of voltage on the input terminals for which the comparator will operate within specifications.

INPUT COMMON MODE REJECTION RATIO – The ratio of the input voltage range to the maximum change in input offset voltage over this range.

DIFFERENTIAL INPUT VOLTAGE RANGE – The range of voltage between the input terminals for which operation within specifications is assured.

VOLTAGE GAIN – The ratio of the change in output voltage to the change in voltage between the input terminals producing it with the DC output level in the vicinity of the logic threshold voltage.

RESPONSE TIME – The interval between the application of an input step function and the time when the output crosses the logic threshold voltage. The input step drives the comparator from some initial, saturated input voltage to an input level just barely in excess of that required to bring the output from saturation to the logic threshold voltage. This excess is referred to as the voltage overdrive.

POSITIVE OUTPUT LEVEL – The DC output voltage in the positive direction with the input voltage equal to or greater than a minimum specified amount.

NEGATIVE OUTPUT LEVEL – The DC output voltage in the negative direction with the input voltage equal to or greater than a minimum specified amount.

OUTPUT SINK CURRENT – The maximum negative current that can be delivered by the comparator.

PEAK OUTPUT CURRENT – The maximum current that may flow into the output load without causing damage to the comparator.

OUTPUT RESISTANCE – The resistance seen looking into the output terminal with the DC output level at the logic threshold voltage.

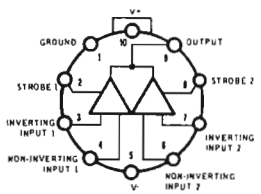
POWER CONSUMPTION – The DC power into the amplifier with no output load. The DC power will vary with signal level, but is specified as a maximum for the entire range of input-signal conditions.

dual comparator

EXTENDED TEMPERATURE RANGE, – 55°C ÷ + 125°C

The μA711 is a dual, differential voltage comparator intended primarily for core-memory sense amplifier applications. The device features high accuracy, fast response times, large input voltage range, low power consumption and compatibility with practically all integrated logic forms. When used as a sense amplifier, the threshold voltage can be adjusted over a wide range, almost independent of the integrated circuit characteristics. Independent strobing of each comparator channel is provided, and pulse stretching on the output is easily accomplished. Other applications of the dual comparator include a window discriminator in pulse height detectors and a double-ended limit detector for automatic go/no-go test equipment. The μA711, which is similar to the μA710 differential comparator, is constructed on a 40-mil square silicon chip using the Planar epitaxial process.

CONNECTION DIAGRAM
(Top view)



Note : Pin 5 connected to case.

ABSOLUTE MAXIMUM RATINGS
(above which the useful life may be impaired)

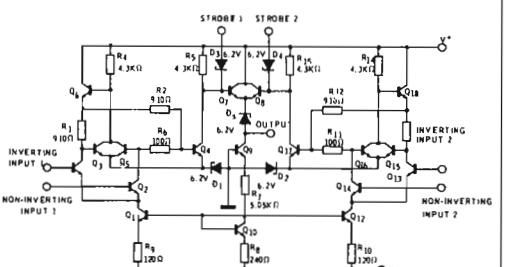
Positive Supply Voltage	14 V
Negative Supply Voltage	7 V
Peak Output Current	50 mA
Differential Input Voltage	± 5 V
Input Voltage	± 7 V
Strobe Voltage	0 to +6 V
Internal Power Dissipation (Note 1)	300 mW
Operating Temperature Range	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 60 sec)	+300°C

ORDERING NUMBER

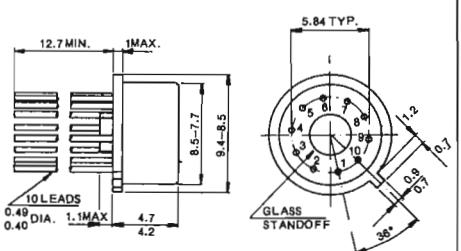
U5F771131X

NOTES : On the following page.

SCHEMATIC DIAGRAM



PHYSICAL DIMENSIONS
in accordance with
JEDEC TO-100 outline



Note : all dimensions in mm.

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$, $V^+ = 12$ V, $V^- = -6$ V unless otherwise noted)

PARAMETER (see definitions)	CONDITIONS	Min.	Typ.	Max.	UNIT
Input Offset Voltage	$V_{OUT} = +1.4$V, $R_S \leq 200\,\Omega$, $V_{CM} = 0$		1	3.5	mV
	$V_{OUT} = +1.4$ V, $R_S \leq 200\,\Omega$		1	5	mV
Input Offset Current	$V_{OUT} = +1.4$ V		0.5	10	μA
Input Bias Current			25	75	μA
Voltage Gain		750	1500		
Response Time (Note 2)			40		nsec
Strobe Release Time			12		nsec
Input Voltage Range	$V^- = -7$ V	±5			V
Differential Input Voltage Range		±5			V
Output Resistance			200		Ω
Positive Output Level	$V_{IN} \geq 10$ mV		4.5	5	V
Loaded Positive Output Level	$V_{IN} \geq 10$ mV, $I_O = 5$ mA	2.5	3.5		V
Negative Output Level	$V_{IN} \geq 10$ mV	-1	-0.5	0	V
Strobed Output Level	$V_{strobe} \leq 0.3$ V	-1		0	V
Output Sink Current	$V_{IN} \geq 10$ mV, $V_{OUT} \geq 0$	0.5	0.8		mA
Strobe Current	$V_{strobe} = 0$		1.2	2.5	mA
Positive Supply Current	$V_{OUT} \leq 0$		8.6		mA
Negative Supply Current			3.9		mA
Power Consumption			130	200	mW
The following specifications apply for $-55°C \leq T_A \leq +125°C$:					
Input Offset Voltage (Note 3)	$R_S \leq 200\,\Omega$, $V_{CM} = 0$			4.5	mV
	$R_S \leq 200\,\Omega$			6	mV
Input Offset Current (Note 3)				20	μA
Input Bias Current				150	μA
Temperature Coefficient of Input Offset Voltage			5		μV/°C
Voltage Gain		500			

NOTES:

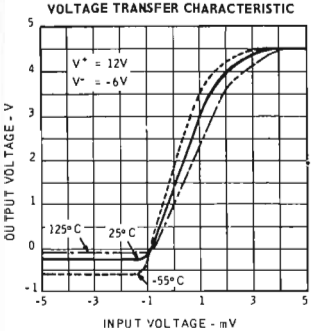
(1) Rating applies for case temperatures to +125°C; derate linearly at 6.6 mW/°C for ambient temperature above 105°C.

(2) The response time specified (see definitions) is for a 100 mV input step with 5 mV overdrive.

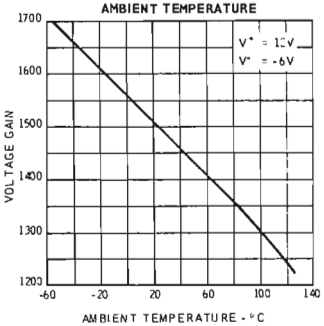
(3) The input offset voltage (see definitions) is specified for a logic threshold voltage of 1.8 V at -55°C, 1.4 V at +25°C and 1 V at +125°C.

TYPICAL ELECTRICAL CHARACTERISTICS (25°C free air temperature unless otherwise noted)

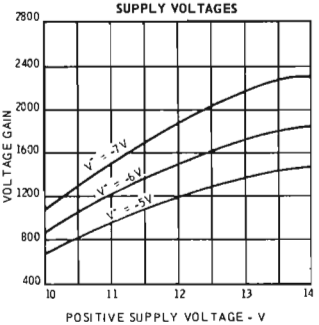
VOLTAGE TRANSFER CHARACTERISTIC



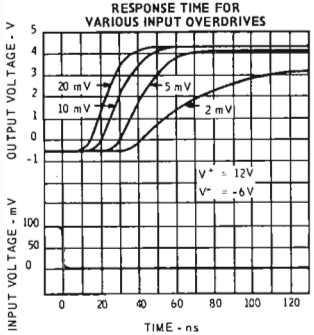
VOLTAGE GAIN VERSUS AMBIENT TEMPERATURE



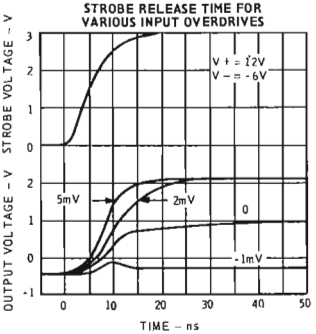
VOLTAGE GAIN VERSUS SUPPLY VOLTAGES



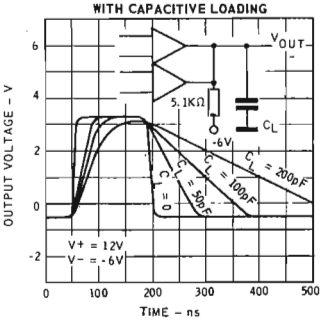
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



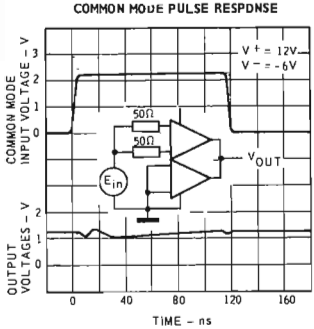
STROBE RELEASE TIME FOR VARIOUS INPUT OVERDRIVES



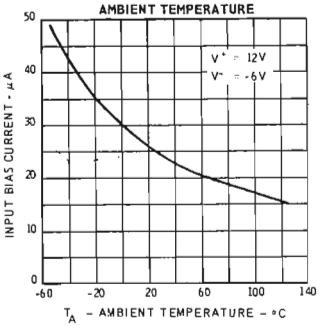
OUTPUT PULSE STRETCHING WITH CAPACITIVE LOADING



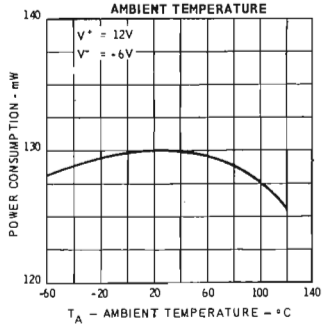
COMMON MODE PULSE RESPONSE



INPUT BIAS CURRENT VERSUS AMBIENT TEMPERATURE



POWER CONSUMPTION VERSUS AMBIENT TEMPERATURE



DEFINITION OF TERMS

LOGIC THRESHOLD VOLTAGE - The approximate voltage at the output of the comparator at which the loading logic circuitry changes its digital state. For the μA711 this voltage has been fixed at + 1.4 V (see note 3).

INPUT OFFSET VOLTAGE* - The voltage between the input terminals when the output is at the logic threshold voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT OFFSET CURRENT* - The difference in the currents into the two input terminals with the output at the logic threshold voltage.

INPUT BIAS CURRENT* - The average of the two input currents.

INPUT VOLTAGE RANGE* - The range of voltage on the input terminals for which the comparator will operate within specifications.

DIFFERENTIAL INPUT VOLTAGE RANGE* - The range of voltage between the input terminals for which operation within specifications is assured

VOLTAGE GAIN* - The ratio of the change in output voltage to the change in voltage between the input terminals producing it with the DC output level in the vicinity of the logic threshold voltage.

RESPONSE TIME* - The interval between the application of an input step function and the time when the output crosses the logic threshold voltage. The input step drives the comparator from some initial, saturated input voltage to an input level just barely in excess of that required to bring the output from saturation to the logic threshold voltage. This excess is referred to as the voltage overdrive.

STROBE RELEASE TIME* - The time required for the output to rise to the logic threshold voltage after the strobe terminal has been driven from the zero to the one logic level. Appropriate input conditions are assumed.

POSITIVE OUTPUT LEVEL* - The DC output voltage in the positive direction with the input voltage equal to or greater than a minimum specified amount.

NEGATIVE OUTPUT LEVEL* - The DC output voltage in the negative direction with the input voltage equal to or greater than a minimum specified amount.

OUTPUT SINK CURRENT - The maximum negative current that can be delivered by the comparator.

PEAK OUTPUT CURRENT - The maximum current that may flow into the output load without causing damage to the comparator.

OUTPUT RESISTANCE* - The resistance seen looking into the output terminal with the DC output level at the logic threshold voltage.

STROBED OUTPUT LEVEL* - The DC output voltage, independent of input voltage, with the voltage on the strobe terminal equal to or less than a minimum specified amount.

STROBE CURRENT - The maximum current drawn by the strobe terminal when it is at zero logic level.

POWER CONSUMPTION - The DC power into the amplifier with no output load. The DC power will vary with signal level, but is specified as a maximum for the entire range of input-signal conditions.

*These definitions apply for either side with the other disabled with the strobe.

Dual comparator

STANDARD TEMPERATURE RANGE,
0°C to 70°C

- FAST RESPONSE TIMES
- LOW POWER CONSUMPTION
- COMPATIBLE WITH LOGIC FAMILIES

The μA711C is a dual, differential voltage comparator intended primarily for core-memory sense amplifier applications. The device features high accuracy, fast response times, wide input voltage range, low power consumption and compatibility with pratically all integrated logic forms. When used as a sense amplifier, the threshold voltage can be adjusted over a wide range, almost independent of the integrated circuit characteristics. Independent strobing of each comparator channel is provided, and pulse stretching on the output is easily accomplished. Other applications of the dual comparator include as window discriminator in pulse height detectors and as double-ended limit detector for automatic go/no-go test equipment. The μA711C, which is similar to the μA710C differential comparator, is constructed on a silicon chip by means of the planar epitaxial process. For full temperature range operation (-55°C to + 125°C) see μA711 data sheet.

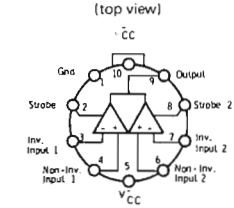
ABSOLUTE MAXIMUM RATINGS

Positive Supply Voltage	14 V
Negative Supply Voltage	-7 V
Peak Output Current	50 mA
Differential Input Voltage	± 5 V
Input Voltage	± 7 V
Strobe Voltage	0V to 6 V
Internal Power Dissipation (Note 1, over)	300 mW
Operating Temperature Range	0°C to + 70°C
Storage Temperature Range	-55°C to + 150°C
Lead Temperature	
(Soldering 60 sec. for package No. 1)	300°C
(Soldering 10 sec. for package No. 2)	260°C

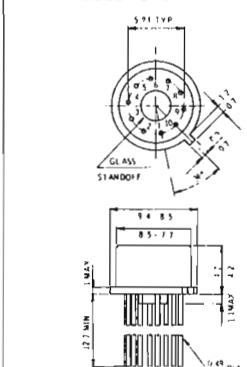
ORDERING NUMBERS

U5F771139X (for package No. 1)
U6E7711393 (for package No. 2)

CONNECTION DIAGRAMS
(top view)

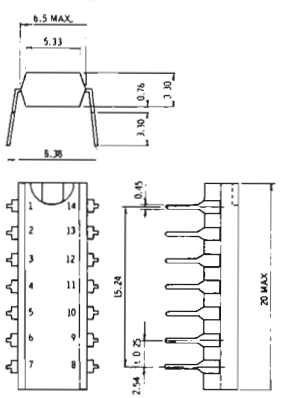


PACKAGE No. 1
PHYSICAL DIMENSIONS
in accordance with
JEDEC TO-100 outline



Note: all dimensions in mm.

PACKAGE No. 2
PHYSICAL DIMENSIONS
14-pin plastic DIP



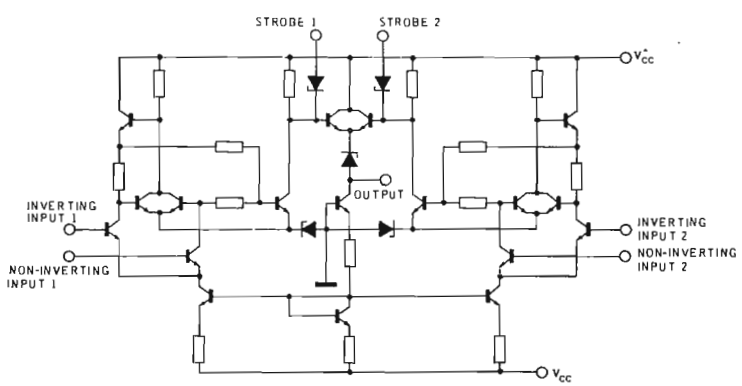
Note: all dimensions in mm.

STANDARD TEMPERATURE RANGE

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC}^+ = 12V, V_{CC}^- = -6V unless otherwise noted)

PARAMETER	CONDITIONS	Min.	Typ.	Max.	Unit
Input Offset Voltage	V_{OUT} = + 1.4V, R_S ≤ 200 Ω		± 1	± 5	mV
	V_{OUT} = + 1.4V, R_S ≤ 200 Ω, V_{CM} = ± 5V				
	V_{CC}^- = - 7V		± 1	± 7.5	mV
Input Offset Current	V_{OUT} = + 1.4V		± 0.5	± 15	μA
Input Bias Current	V_{CM} = + 5V		25	100	uA
Voltage Gain		700	1500		
Response Time (Note 2)			40		nsec
Strobe Release Time			12		nsec
Input Voltage Range	V_{CC}^- = -7V	± 5			V
Differential Input Voltage Range		± 5			V
Output Resistance			200		Ω
Positive Output Level	V_{IN} ≥ 10 mV		4.5	5	V
Loaded Positive Output Level	V_{IN} ≥ 10 mV, I_O = 5 mA	2.5	3.5		V
Negative Output Level	V_{IN} ≤ 10 mV	-1	-0.5	0	V
Strobed Output Level	V_{strobe} ≤ 0.3V	-1		0	V
Output Sink Current	V_{IN} ≥ 10 mV, V_{OUT} = 0	0.5	0.8		mA
Strobe Current	V_{strobe} = 100mV		-1.2	-2.5	mA
Positive Supply Current	V_{OUT} = 0		8.6		mA
Negative Supply Current	V_{OUT} = 0		-3.9		mA
Power Consumption	V_{OUT} = 0		130	230	mW
The following specifications apply for 0°C ≤ T_A ≤ + 70°C:					
Input Offset Voltage (Note 3)	R_S ≤ 200 Ω			± 6	mV
	R_S ≤ 200 Ω, V_{CM} = ± 5V, V_{CC}^- = -7V			± 10	mV
Input Offset Current (Note 3)				± 25	μA
Input Bias Current	V_{CM} = + 5V			150	μA
Average Temperature Coefficient of Input Offset Voltage	R_S ≤ 200 Ω		5		μV/°C
Voltage Gain		500			

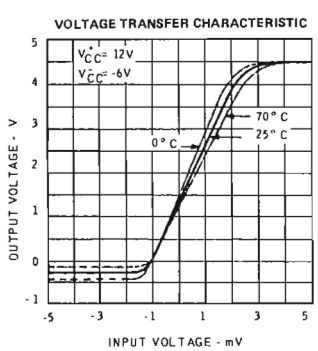
EQUIVALENT CIRCUIT

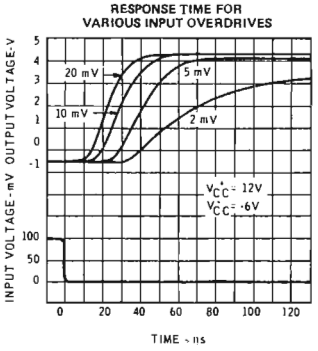


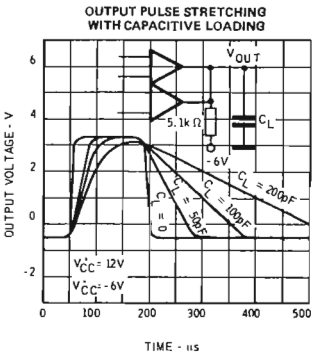
NOTES :

1) Rating applies for ambient temperature to + 70°C.
2) The response time specified is for a 100mV input step with 5mV overdrive.
3) The input offset voltage is specified for a logic threshold voltage of 1.5V at 0°C, 1.4V at + 25°C and 1.2V at + 70°C.

TYPICAL ELECTRICAL CHARACTERISTICS (25°C free air temperature unless otherwise noted)







DEFINITION OF TERMS

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PEAK OUTPUT CURRENT - The maximum current that may flow into the output load without causing damage to the comparator.

OUTPUT RESISTANCE* - The resistance seen looking into the output terminal with the DC output level at the logic threshold voltage.

STROBE OUTPUT LEVEL* - The DC output voltage, independent of input voltage, with the voltage on the strobe terminal equal to or less than a minimum specified amount.

STROBE CURRENT - The maximum current drawn by the strobe terminal when it is at zero logic level.

POWER CONSUMPTION - The DC power into the amplifier with no output load. The DC power will vary with signal level, but is specified as a maximum for the entire range of input-signal conditions.

* These definitions apply for either side with the other disabled with the strobe.

DTL INTEGRATED CIRCUITS

DTL INTEGRATED CIRCUITS

DTL 930 SERIES

GATES	Page E.	Page S.
9930	139	169
9932	144	175
9933	147	178
9934	—	170
9935	140	171
9936	141	172
9944	145	176
9946	142	173
9962	143	174

FLIP-FLOPS	Page E.	Page S.
9093	152	182
9094	152	182
9097	153	183
9099	153	183
9945	149	179
9948	149	179

OTHER FUNCTIONS	Page E.	Page S.
9951 Monostable	156	186

E. = Extended temperature range
S. = Standard temperature range

diode-transistor logic family

EXTENDED TEMPERATURE RANGE - 55°C+ 125°C

- Compatible with TTL and LPDTL products
- Noise Immunity 1V
- Output drive capability of 10
- Power dissipation 8.5 mW per gate
- Fan-in expansion capability
- Wired-OR capability
- Same pin configuration as the corresponding TTL and LPDTL products

The SGS Diode-Transistor Logic (DTL) Family consists of a set of compatible integrated circuits designed for medium power, medium speed applications.
The circuits are fabricated within a silicon monolithic substrate using the standard Planar epitaxial process.
DTL elements are available in two hermetically sealed ceramic packages : the Dual in-Line Package (6A) designed for low cost insertion, and the 14 leads flat package (3I) for maximum component density.

ORDERING NUMBER

U6A XXXX51X
(for Dual in-Line Package, XXXX is type number)
U3I XXXX51X
(for Flat Package, XXXX is type number)

ABSOLUTE MAXIMUM RATINGS

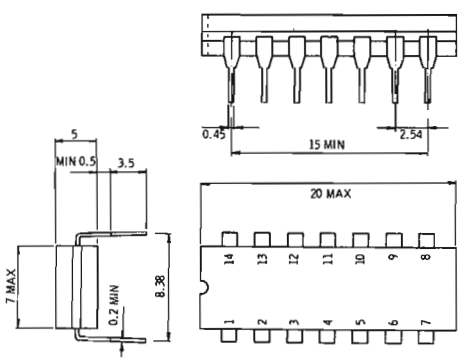
(above which the useful life may be impaired)

Supply voltage (V_{CC}), continuous	8 V
Supply voltage (V_{CC}), pulsed < 1 sec	12 V
Output current, into outputs	
DTL 9932 - 9944	100 mA
Other elements	30 mA
Input forward current	-10 mA
Input reverse current	1 mA
Temperature (ambient) under bias	- 55°C to 125°C
Storage temperature	- 65°C to 150°C

OPERATING CONDITIONS

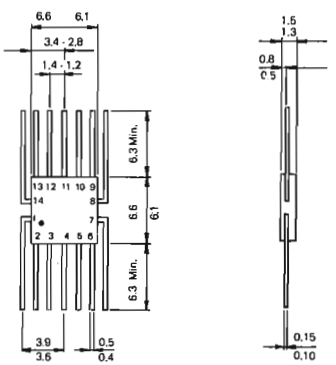
Temperature range	- 55°C to 125°C
Supply voltage	5 V ± 10 %

PHYSICAL DIMENSIONS
Dual-in-Line ceramic package



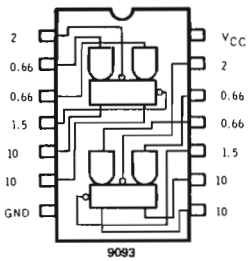
Note : all dimensions in mm.

PHYSICAL DIMENSIONS
Flat ceramic package



NOTE : All dimensions in mm.

INPUT-OUTPUT LOAD/DRIVE FACTORS



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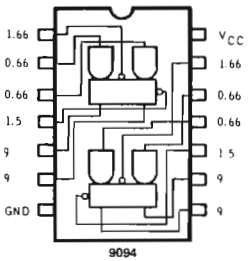

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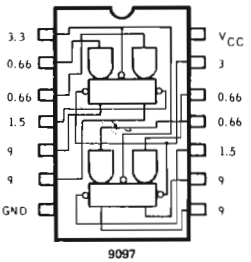
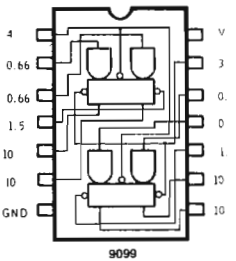
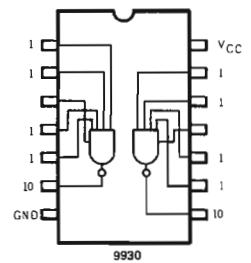


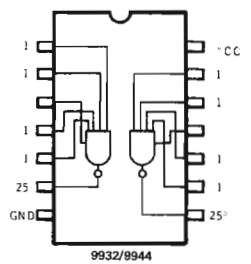
9097



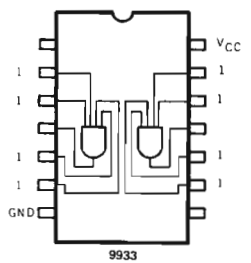
9099



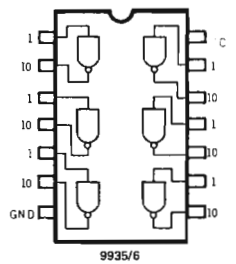
9930



9932/9944



9933



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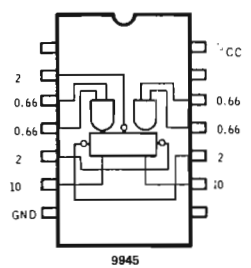
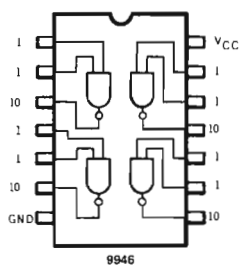
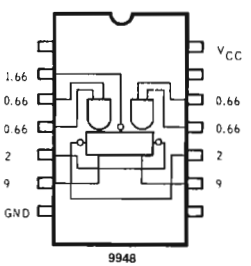


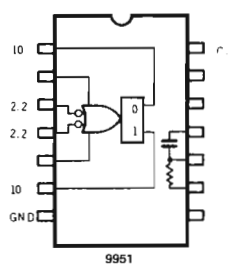
9945



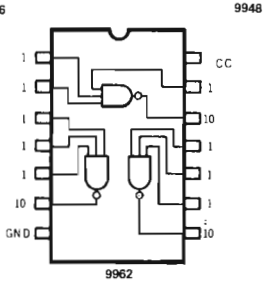
9946



9948



9951



9962

* See Miscellaneous Rules for 9944

MISCELLANEOUS RULES

The number of elements driven by an output terminal may consist of any combination of elements whose sum of input load factors does no exceed the output drive factor.

An external resistor should be used with 9944. With an external resistor R the following output drive factors will be obtained :

R = 6 KΩ Drive Factor = 26
R = 2 KΩ Drive Factor = 25
R = 1 KΩ Drive Factor = 23
R = 510Ω Drive Factor = 20

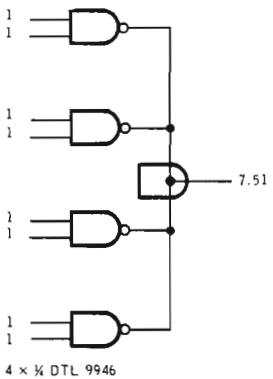
For increased output drive, the inputs and outputs of 1/2 DTL 9944 may be paralleled, up to 4 common outputs. For 4 paralleled elements:

each combined input, load factor = 4
each combined output, drive factor = 100 (R = 2 KΩ)

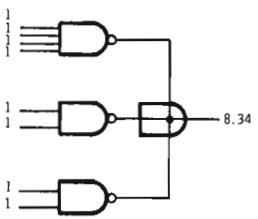
"WIRED OR" CONNECTION

1. Outputs of DTL gates may be tied together for the "wired OR" function
   ($\overline{ABCD} \cdot \overline{GHIJ} = \overline{ABCD + GHIJ}$). Subtract, for each added gate, 0.83 unit load from output drive factor.
2. Outputs of DTL 9932 may not be tied together for the "wired OR" function.

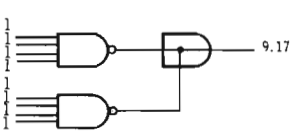
"WIRED OR" Examples:



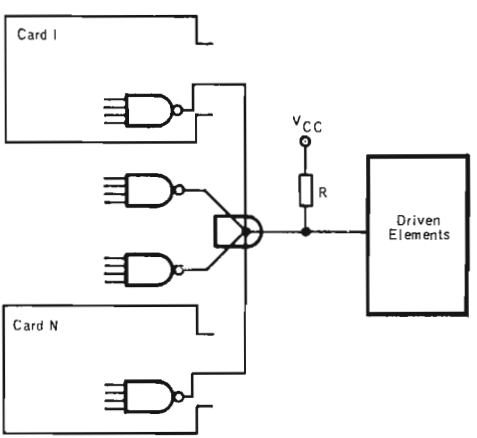
4 × ¼ DTL 9946



¼ 9930 and
2 × ¼ 9946



DTL 9930 WIRED OR



Each output driver is 1/2 DTL 9944. Note that the DTL 9944 is a direct high fan-out replacement for DTL 9930, except that an external resistor must be used. The F.O. will be the same as one 1/2 DTL 9944 buffer used with that resistor.

DELAY TIME PERFORMANCE INTO CAPACITIVE LOADS

Most delay attributable to capacitive loads is associated with the positive going output. Two R-C time constants are seen in the positive going output. In the 1st time period, from the saturated low level to threshold, the R of the RC time constant can be given by 6 kΩ in parallel with $\frac{3.75\ K\Omega}{\text{active fanout}}$

Above the threshold which occurs at about 1.4 to 1.5 volts at 25°C, the R of the 2nd R C time constant is 6 kΩ and the rate of the voltage rise above threshold is slow. The logic signal propagates through at the threshold level, so voltage rise above threshold does not effect speed. By noting that both rise domains drive toward V_{CC}, the voltage rise waveform may be calculated. DTL gate inputs are ~ 2 pf per input for active or inactive fanout; the remaining capacitance is from board, wiring, and connectors.

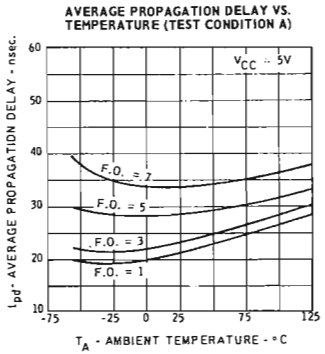


FIG. 1

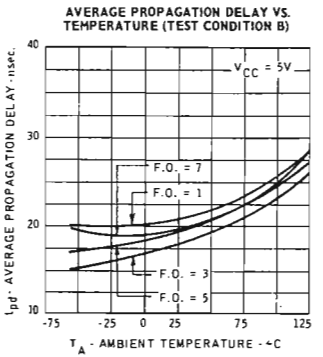
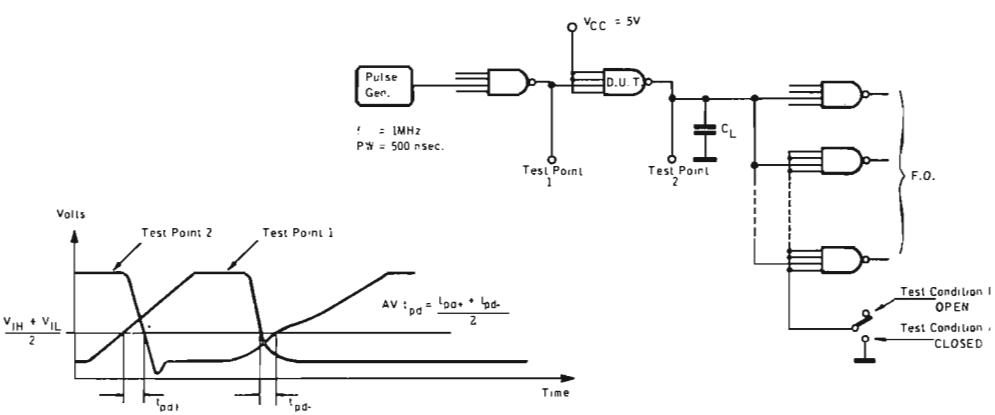


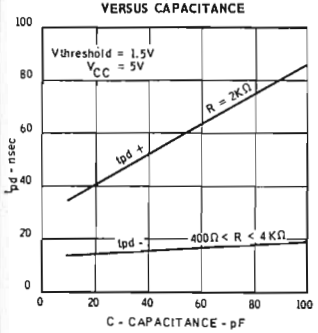
FIG. 2

TEST CONDITIONS FOR FIG. 1 AND 2

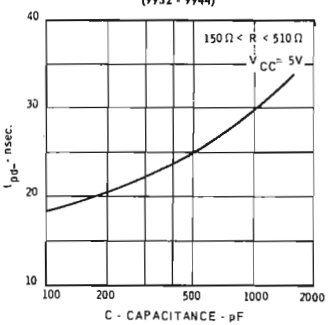


t_{pd} CURVES VERSUS OUTPUT CAPACITANCE ($T_A = 25°C$ unless otherwise noted)

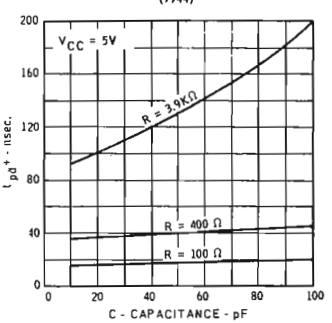
TYPICAL t_{pd} OF GATES VERSUS CAPACITANCE



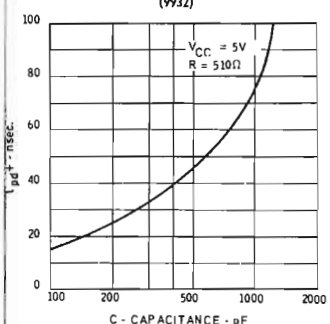
t_{pd-} VERSUS CAPACITANCE (9932 - 9944)



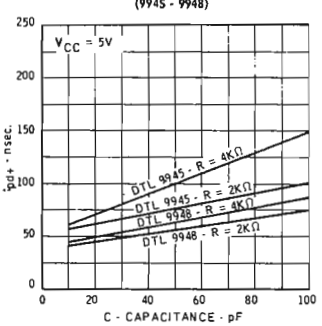
t_{pd+} VERSUS CAPACITANCE (9944)



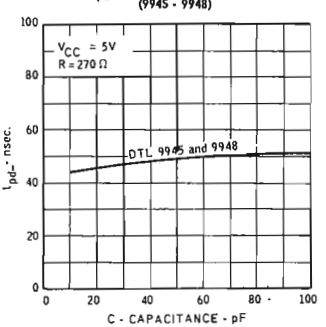
t_{pd+} VERSUS CAPACITANCE (9932)



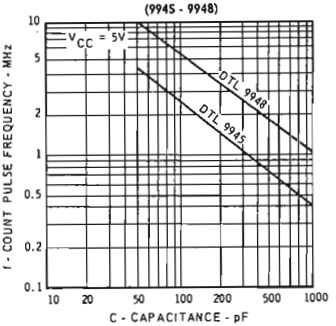
t_{pd} VERSUS CAPACITANCE (9945 - 9948)



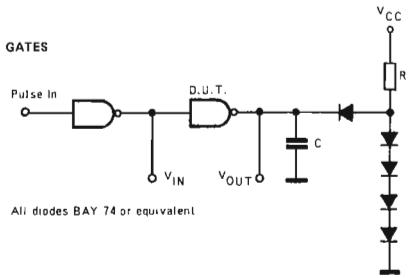
t_{pd-} VERSUS CAPACITANCE (9945 - 9948)

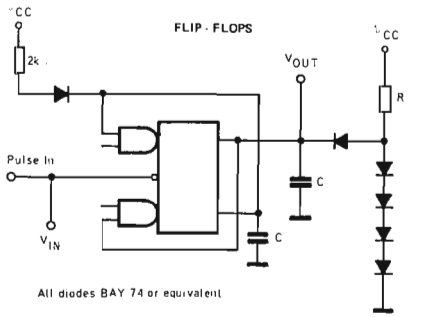


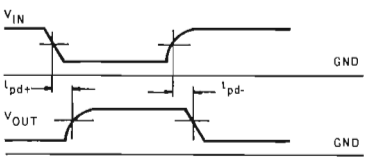
MAXIMUM BINARY COUNTING RATE VERSUS CAPACITANCE (9945 - 9948)

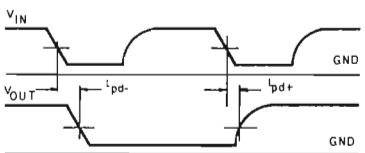


TEST CIRCUITS

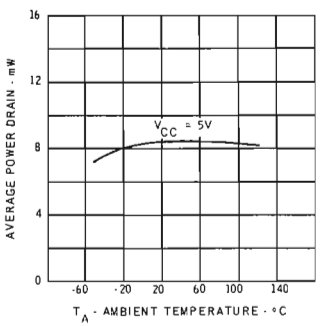


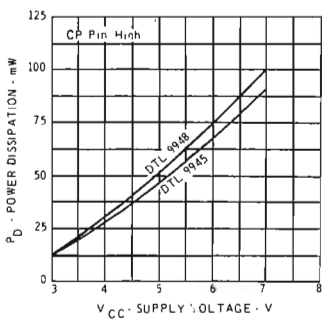


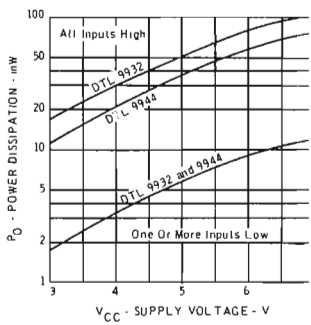




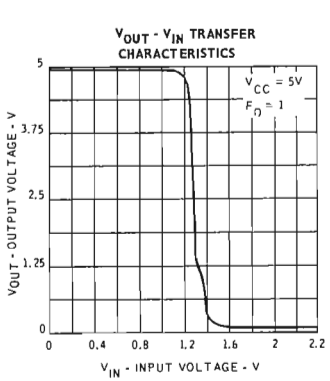
POWER DISSIPATION CURVES (T_A = 25° unless otherwise noted)

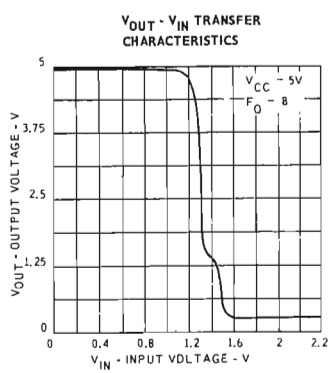


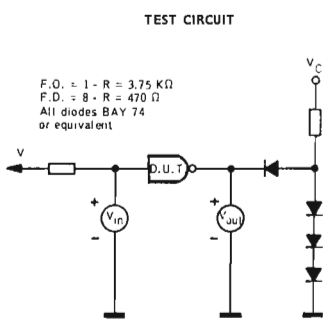




TRANSFER CHARACTERISTICS (T_A = 25° C unless otherwise noted)







NOISE IMMUNITY

There are two types of noise immunity which can be guaranteed : Signal Noise Immunity or Ground Noise Immunity.

(A) Signal noise immunity $|V_{IL} - V_{OL}| = V_{NS}$
or $|V_{OH} - V_{IH}| = V_{NC}$

where V_{IL} = Maximum Low Input Voltage that guarantees V_{OH}
V_{OL} = Maximum Low Output Voltage
V_{IH} = Minimum High Input Voltage that guarantees V_{OL}
V_{OH} = Minimum High Output Voltage

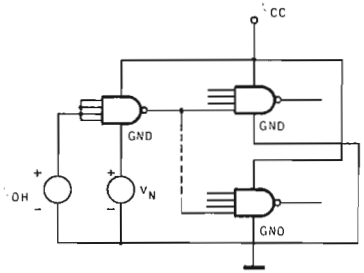
(B) Ground noise immunity, V_{NG}. The worst case noise immunity for diode-transistor logic circuits is usually ground noise V_{NG}.

Note that some curves show two values of V_{CC} at given temperature for the same noise immunity. The upper V_{CC} corresponds to noise immunity such that $V_N \approx V_{NS} \approx V_{NG} \approx V_{IL} - V_{OL}$. The driving device is hard in saturation and V_{NG} simply adds to V_{OL}. The lower V_{CC} corresponds to soft saturation where V_{NG} tends to turn off the drive gate. There is voltage gain therefore between V_{NG} and the output node and V_{NG} is significantly less than $V_{IL} - V_{OL}$.

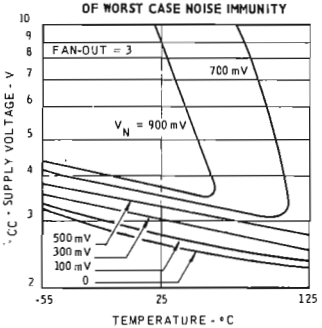
Each of the curves on this page shows V_N, the worst case of V_{NG} and V_{NS}.

As an example the curves for fan-out of 7 show a worst case $V_N = V_{NG}$ of 200 mV at V_{CC} = 4 V and -55°C. This, however, corresponds to a worst case signal noise immunity of $V_{IL} - V_{OL}$ 500 mV for the same fan-out, temperature, and V_{CC}.

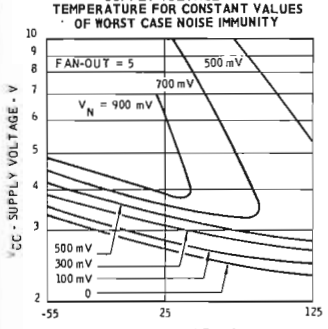
TEST CIRCUIT



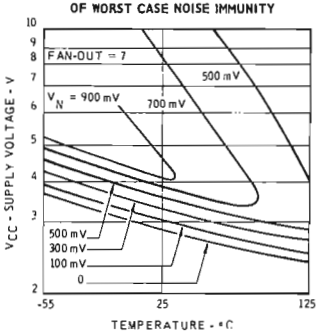
SUPPLY VOLTAGE VS.
TEMPERATURE FOR CONSTANT VALUES
OF WORST CASE NOISE IMMUNITY



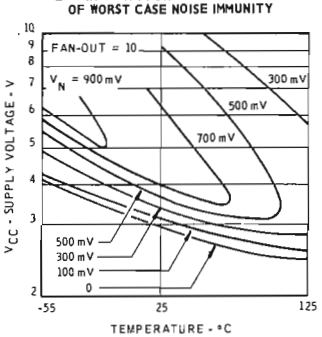
SUPPLY VOLTAGE VS.
TEMPERATURE FOR CONSTANT VALUES
OF WORST CASE NOISE IMMUNITY



SUPPLY VOLTAGE VS.
TEMPERATURE FOR CONSTANT VALUES
OF WORST CASE NOISE IMMUNITY



SUPPLY VOLTAGE VS.
TEMPERATURE FOR CONSTANT VALUES
OF WORST CASE NOISE IMMUNITY



MINIMUM - MAXIMUM DC CURVES, I_F VS. V_{CC} & V_F

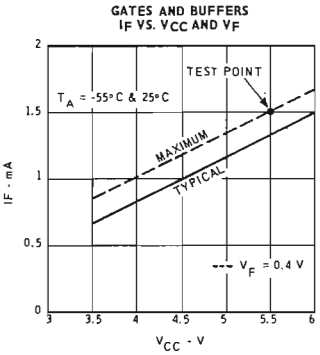


FIG. 1

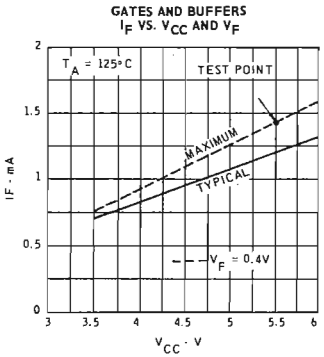


FIG. 2

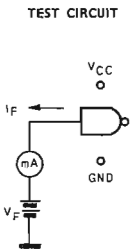


FIG. 3

OUTPUT LOW CURRENT VS. V_{CC} & V_{OL} FOR GATES

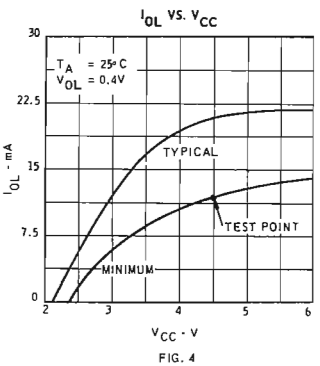


FIG. 4

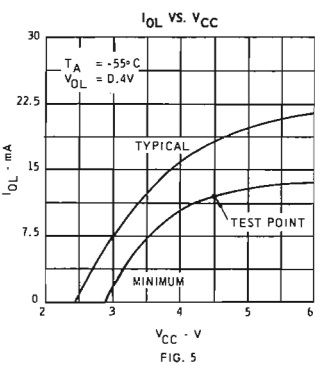


FIG. 5

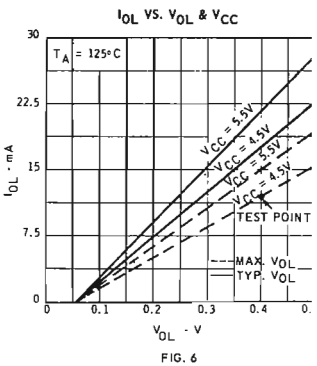


FIG. 6

BUFFERS GATES INPUT THRESHOLD VS. TEMPERATURE

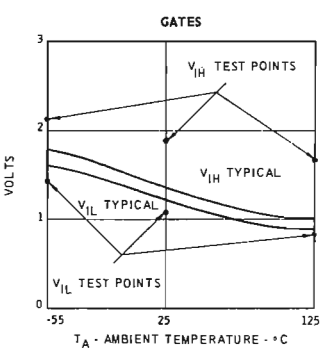


FIG. 7

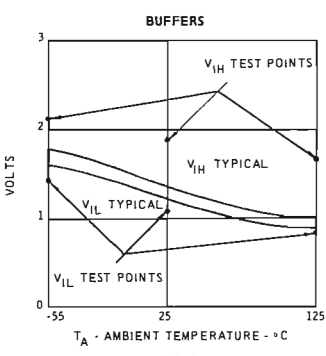


FIG. 8

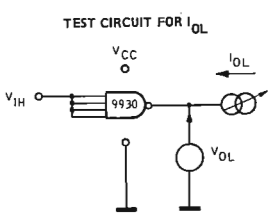
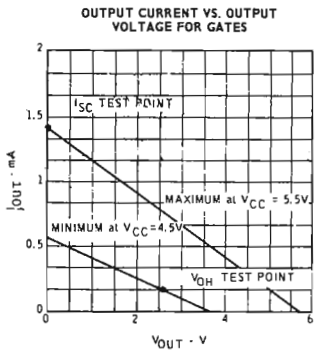
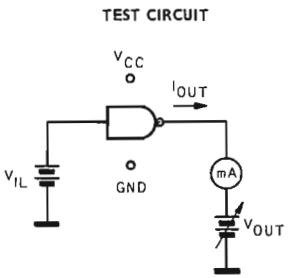


FIG. 9

OUTPUT CURRENT VS. OUTPUT VOLTAGE FOR GATES

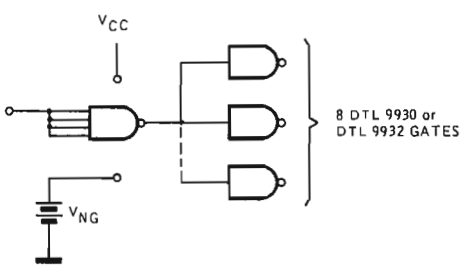




EXAMPLES OF USES FOR THE MINIMUM-MAXIMUM DC CURVES (Page 136)

EXAMPLE 1.

A low DTL 9930 output at -55°C fans out to 8 inputs of DTL 9930 or 9932 V_{CC} = 5 V. Positive DC ground noise (V_{NG}) of 350 mV is applied to the 1st 9930. Its output may thus rise to 0.75 Volt (V_{NG} + V_{OL}). 4.65 Volts (V_{CC} - V_{NG}) remain from V_{CC} pin to ground pin; this is above V_{CCL} = 4.5 V, and test I_{OL} is conservative. Maximum current flowing in each input of the 8 9930/9932's is given by Fig. 1 on Page 136 with V_F = 0.75 V and V_{CC} = 5 V : the current (I_F) is less then 1.25 mA and total current ($\leq$ 8 x 1.25 = 10 mA) is less than the I_{OL} test current used at -55°C to saturate the low output.
Above the 350 mV of V_{NG} already applied, the difference between the common node voltage (< 0.75 V) and the low input threshold (V_{IL} = 1.40 V) of the 8 9930/9932's is still $\geq$ 350 mV, allowing for signal noise to be superposed above ground noise.



EXAMPLE 2.

The I_F and I_{OL} curves on Page 136 may be expressed in analytical form, as follows

$$I_F \leq \frac{V_{CC} - V_F - V_{FD}}{3\,k\Omega} \quad T_A < 25°C$$

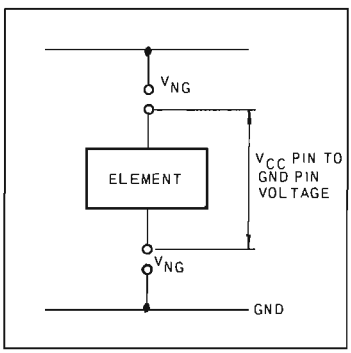
For T_A greater than 25°C, the 3 kΩ rises by 0.12%/°C to approximately 3.36 kΩ at 125°C. V_{FD} is the temperature dependent silicon forward diode drop and is about 0.7 V at 25°C and 1 mA. $\angle V_{FD}/°C$ is roughly 1.8 mV/°C.
The ratio of I_{OL}, on gates (figs. 4,5, and 6 at page 136) at V_{CC} below test V_{CC}, to I_{OL} at test V_{CC} can be given by

$$\frac{I_{OL} \text{ @ } -55°C}{\text{Test } I_{OL} \text{ @ } V_{CCL} = 4.5\,V} > \frac{V_{CC} - 3\,V}{4.5\,V - 3\,V} \quad \text{and by} \quad \frac{I_{OL} \text{ @ } 25°C}{\text{Test } I_{OL} \text{ @ } V_{CCL} = 4.5\,V} > \frac{V_{CC} - 2.3\,V}{4.5\,V - 2.3\,V}$$

Since, at 25°C, I_{OL} > 12 mA at V_{CCL} = 4.5 is guaranteed by the test point fig. 4 page 136 I_{OL} at V_{CC} pin to GND pin voltage of 3.6 V is $\frac{3.6 - 2.3}{4.5 - 2.3}$ 12 mA = 7.1 mA.
The similer expression for the 9932 power gate gives a very conservative value due to the phase splitter gain. Above V_{CCL}, I_{OL} is limited by V_{OL} with an essentially resistive ($\frac{V_{OL}}{I_{OL}}$ saturation resistance slope). Fig. 6 at 125°C shows this, with V_{CC} having relatively small effect.

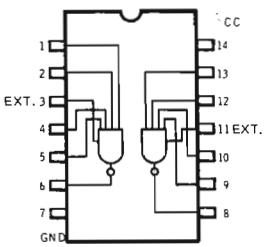
EXAMPLE 3.

The test sequences and tables of conditions and limits use two values of V_{CC}, V_{CCL} and V_{CCH}. With a nominal 5 volts V_{CC}, for example, and assuming $\Delta V_{CC} = +0.2V$, testing at $V_{CCL} = 4.5$ V and $V_{CCH} = 5.5$ V allows simulation of ± 0.3 V ground noise V_{NG} or V_{CC} line noise V_{NG}. Since there is gain associated with V_{NG}, particularly at lower temperatures and V_{CC} values : the test guarantees of output low current and voltage are the worst case test conditions to simulate worst case ground noise. Much better numbers could be shown, for example, in the ratio of output current to input current (I_{OL}/I_F) if both I_{OL} and I_F were measured at identical V_{CC} values and if input current was sunk into $V_F = V_{OL}$, the worst case low output level, or even into $V_F = V_{IL}$, the input threshold value. However, the test values would then guarantee only signal line noise immunity, where there is no gain associated with V_{NS}. By use of the Minimum/Maximum DC curves on Page 95 or by the Example 2 equations, limits for the single V_{CC} testing approach could be recovered. More important, each design or components engineer can develop the fanout, power, and noise margin tradeoffs for this unique application.

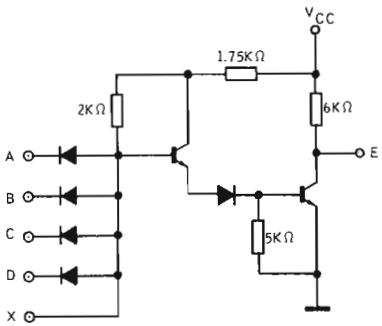


EXTENDED TEMPERATURE RANGE

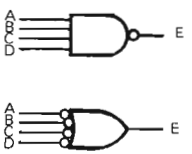
CONNECTION DIAGRAM
(top view)



SCHEMATIC DIAGRAM
(one gate only)



LOGIC FUNCTION



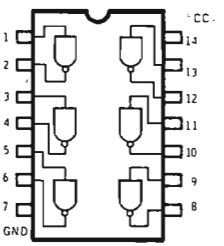
POSITIVE $E = \overline{A \cdot B \cdot C \cdot D}$
(NAND)
LOGIC

NEGATIVE $E = \overline{A + B + C + D}$
(NOR)
LOGIC

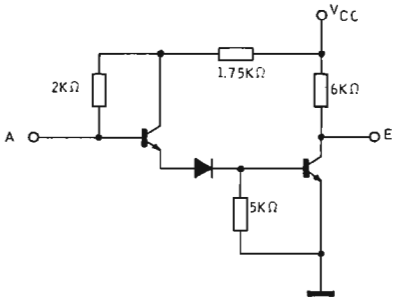
ELECTRICAL CHARACTERISTICS ($V_{CC} = 5\ V \pm 10\%$)

SYMBOL	CHARACTERISTICS	LIMITS						UNIT	CONDITIONS AND COMMENTS
		-55°C		25°C		125°C			
		Min.	Max.	Min.	Typ. Max.	Min.	Max.		
V_{OH}	Output High Voltage	2.5		2.6		2.5		V	$V_{CC} = 4.5\ V$, $I_{OH} = -0.18\ mA$ one input at V_{IL} (see below)
V_{OL}	Output Low Voltage		0.4		0.4		0.4	V	$V_{CC} = 4.5\ V$ $I_{OL} = 12\ mA$ inputs at V_{IH} (see below) $V_{CC} = 5.5V$, $I_{OL} = 15\ mA$ all inputs at $V_R = 5.5\ V$
V_{IH}	Input High Voltage	2.1		1.9		1.7		V	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		1.4		1.1		0.8	V	Guaranteed input low threshold for all inputs
I_F	Input Load Current		-1.5		-1.5		1.4	mA	$V_{CC} = 5.5\ V$ $V_F = 0.4\ V$ on other inputs $V_R = 4\ V$
I_R	Input Leakage Current		2		2		5	μA	$V_{CC} = 5.5\ V$ $V_R = 4\ V$ ground on other inputs
I_{SC}	Output Short Circuit Current	-0.68	-1.33	-0.68	-1.33	-0.59	-1.33	mA	$V_{CC} = 5.5\ V$ one input grounded output grounded
I_{PD}	Power Dissipation Current (each gate)				3.25			mA	$V_{CC} = 5V$ inputs open
t_{pd+}	Turn-off delay			25	80			nsec	$V_{CC} = 5\ V$ see test circuit
t_{pd-}	Turn-on delay			10	30			nsec	

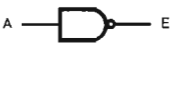
CONNECTION DIAGRAM
(top view)



SCHEMATIC DIAGRAM
(one gate only)



LOGIC FUNCTION



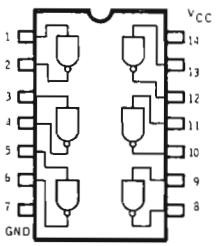
$A = \bar{E}$

ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V ± 10 %)

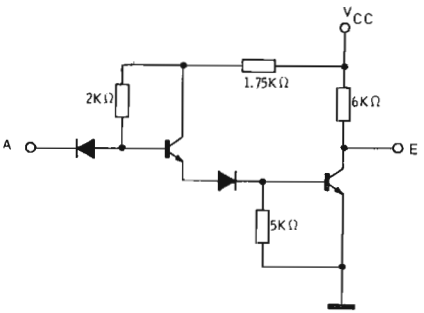
SYMBOL	CHARACTERISTICS	LIMITS -55°C Min.	LIMITS -55°C Max.	LIMITS 25°C Min.	LIMITS 25°C Typ.	LIMITS 25°C Max.	LIMITS 125° Min.	LIMITS 125° Max.	UNIT	CONDITIONS AND COMMENTS
V_{OH}	Output High Voltage	2.5		2.6			2.5		V	V_{CC} = 4.5 V, I_{OH} = - 0.18 mA one input at V_{IL} (see below)
V_{OL}	Output Low Voltage		0.4			0.4		0.4	V	V_{CC} = 4.5 V I_{OL} = 12 mA inputs at V_{IH} (see below) V_{CC} = 5.5 V, I_{OL} = 15 mA all inputs at V_R = 5.5 V
V_{IH}	Input High Voltage	2.1		1.9			1.7		V	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		1.4			1.1		0.8	V	Guaranteed input low threshold for all inputs
I_F	Input Load Current		-1.5			-1.5		-1.4	mA	V_{CC} = 5.5 V V_F = 0.4 V on other inputs V_R = 4 V
I_{SC}	Output Short Circuit Current	-0.68	-1.33	-0.68		-1.33	-0.60	-1.33	mA	V_{CC} = 5.5 V one input grounded output grounded
I_{PD}	Power Dissipation Current (each gate)					3.25			mA	V_{CC} = 5 V inputs open
t_{pd} +	Turn - off delay				25	80			nsec	V_{CC} = 5 V see test circuit
t_{pd} -	Turn - on delay				10	40			nsec	

NOTE : BAY-74 Diode must be connected to each gate when testing this element.

CONNECTION DIAGRAM
(top view)



SCHEMATIC DIAGRAM
(one gate only)



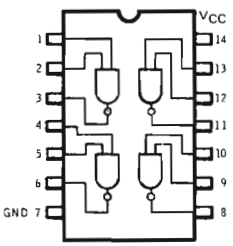
LOGIC FUNCTION

$A = \bar{E}$

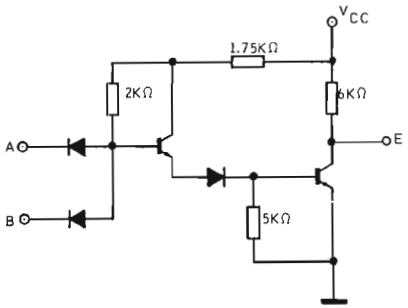
ELECTRICAL CHARACTERISTICS ($V_{CC} = 5\ V \pm 10\%$)

SYMBOL	CHARACTERISTICS	LIMITS -55°C Min.	LIMITS -55°C Max.	LIMITS 25°C Min.	LIMITS 25°C Typ.	LIMITS 25°C Max.	LIMITS 125°C Min.	LIMITS 125°C Max.	UNIT	CONDITIONS AND COMMENTS
V_{OH}	Output High Voltage	2.5		2.6			2.5		V	$V_{CC} = 4.5\ V$, $I_{OH} = -0.18\ mA$ one input at V_{IL} (see below)
V_{OL}	Output Low Voltage		0.4			0.4		0.4	V	$V_{CC} = 4.5\ V$ $I_{OL} = 12\ mA$ inputs at V_{IH} (see below) $V_{CC} = 5.5V$, $I_{OL} = 15\ mA$ all inputs at $V_R = 5.5\ V$
V_{IH}	Input High Voltage	2.1		1.9			1.7		V	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		1.4			1.1		0.8	V	Guaranteed input low threshold for all inputs
I_F	Input Load Current		-1.5			-1.5		-1.4	mA	$V_{CC} = 5.5\ V$ $V_F = 0.4\ V$ on other inputs $V_R = 4\ V$
I_R	Input Leakage Current		2			2		5	μA	$V_{CC} = 5.5\ V$ $V_R = 4\ V$ ground on other inputs
I_{SC}	Output Short Circuit Current	-0.68	-1.33	-0.68		-1.33	-0.59	-1.33	mA	$V_{CC} = 5.5\ V$ one input grounded output grounded
I_{PD}	Power Dissipation Current (each gate)					3.25			mA	$V_{CC} = 5\ V$ inputs open
t_{pd}^+	Turn-off delay			25		80			nsec	$V_{CC} = 5\ V$ see test circuit
t_{pd}^-	Turn-on delay			10		30			nsec	

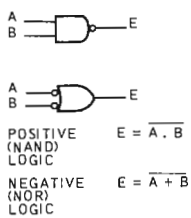
CONNECTION DIAGRAM
(top view)



SCHEMATIC DIAGRAM
(one gate only)



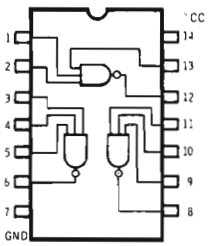
LOGIC FUNCTION



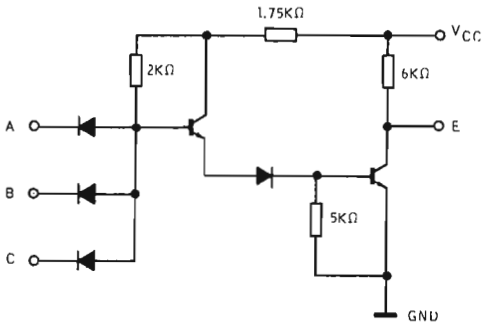
ELECTRICAL CHARACTERISTICS ($V_{CC} = 5\ V \pm 10\%$)

SYMBOL	CHARACTERISTICS	LIMITS -55°C Min.	LIMITS -55°C Max.	LIMITS 25°C Min.	LIMITS 25°C Typ.	LIMITS 25°C Max.	LIMITS 125°C Min.	LIMITS 125°C Max.	UNIT	CONDITIONS AND COMMENTS
V_{OH}	Output High Voltage	2.5		2.6			2.5		V	$V_{CC} = 4.5\ V$, $I_{OH} = -0.18\ mA$ one input at V_{IL} (see below)
V_{OL}	Output Low Voltage		0.4			0.4		0.4	V	$V_{CC} = 4.5\ V$ $I_{OL} = 12\ mA$ inputs at V_{IH} (see below) $V_{CC} = 5.5V$, $I_{OL} = 15\ mA$ all inputs at $V_R = 5.5\ V$
V_{IH}	Input High Voltage	2.1		1.9			1.7		V	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		1.4			1.1		0.8	V	Guaranteed input low threshold for all inputs
I_F	Input Load Current		-1.5			-1.5		-1.4	mA	$V_{CC} = 5.5\ V$ $V_F = 0.4\ V$ on other inputs $V_R = 4\ V$
I_R	Input Leakage Current		2			2		5	μA	$V_{CC} = 5.5\ V$ $V_R = 4\ V$ ground on other inputs
I_{SC}	Output Short Circuit Current	-0.68	-1.33	-0.68		-1.33	-0.59	-1.33	mA	$V_{CC} = 5.5\ V$ one input grounded output grounded
I_{PD}	Power Dissipation Current (each gate)					3.25			mA	$V_{CC} = 5\ V$ inputs open
t_{pd+}	Turn-off delay				25	80			nsec	$V_{CC} = 5\ V$ see test circuit
t_{pd-}	Turn on delay				10	30			nsec	

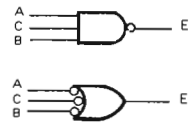
CONNECTION DIAGRAM
(top view)



SCHEMATIC DIAGRAM
(one gate only)



LOGIC FUNCTION



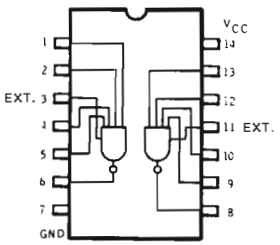
POSITIVE (NAND) LOGIC $E = \overline{A \cdot B \cdot C}$

NEGATIVE (NOR) LOGIC $E = \overline{A + B + C}$

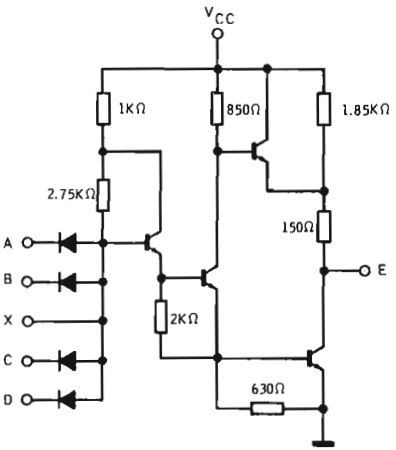
ELECTRICAL CHARACTERISTICS ($V_{CC} = 5\ V \pm 10\%$)

SYMBOL	CHARACTERISTICS	LIMITS -55°C Min.	LIMITS -55°C Max.	LIMITS 25°C Min.	LIMITS 25°C Typ.	LIMITS 25°C Max.	LIMITS 125°C Min.	LIMITS 125°C Max.	UNIT	CONDITIONS AND COMMENTS
V_{OH}	Output High Voltage	2.5		2.6			2.5		V	$V_{CC} = 4.5\ V$, $I_{OH} = -0.18\ mA$ one input at V_{IL} (see below)
V_{OL}	Output Low Voltage		0.4			0.4		0.4	V	$V_{CC} = 4.5\ V$ $I_{OL} = 12\ mA$ inputs at V_{IH} (see below) $V_{CC} = 5.5V$, $I_{OL} = 15\ mA$ all inputs at $V_R = 5.5\ V$
V_{IH}	Input High Voltage	2.1		1.9			1.7		V	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		1.4			1.1		0.8	V	Guaranteed input low threshold for all inputs
I_F	Input Load Current		-1.5			-1.5		-1.4	mA	$V_{CC} = 5.5\ V$ $V_F = 0.4\ V$ on other inputs $V_R = 4\ V$
I_R	Input Leakage Current		2			2		5	µA	$V_{CC} = 5.5\ V$ $V_R = 4\ V$ ground on other inputs
I_{SC}	Output Short Circuit Current	-0.68	-1.33	-0.68		-1.33	-0.59	-1.33	mA	$V_{CC} = 5.5\ V$ one input grounded output grounded
I_{PD}	Power Dissipation Current (each gate)					3.25			mA	$V_{CC} = 5\ V$ inputs open
t_{pd+}	Turn-off delay			25		80			nsec	$V_{CC} = 5\ V$ see test circuit
t_{pd-}	Turn-on delay			10		30			nsec	

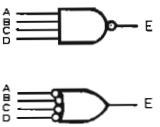
CONNECTION DIAGRAM
(top view)



SCHEMATIC DIAGRAM
(one gate only)



LOGIC FUNCTION



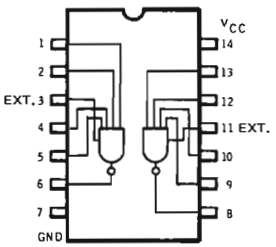
POSITIVE $E = \overline{A \cdot B \cdot C \cdot D}$
(NAND)
LOGIC

NEGATIVE $E = \overline{A+B+C+D}$
(NOR)
LOGIC

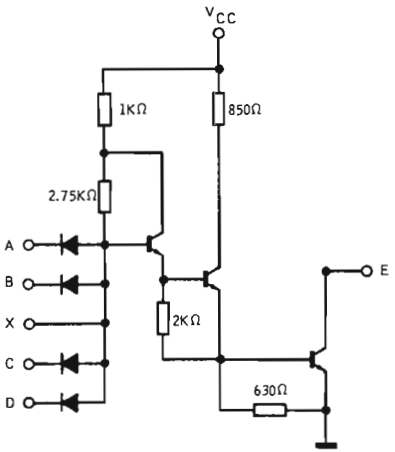
ELECTRICAL CHARACTERISTICS ($V_{CC} = 5\ V \pm 10\%$)

SYMBOL	CHARACTERISTICS	LIMITS 55°C Min.	55°C Max.	25°C Min.	25°C Typ.	25°C Max.	125°C Min.	125°C Max.	UNIT	CONDITIONS AND COMMENTS
V_{OH}	Output High Voltage	2.5		2.6			2.5		V	$V_{CC} = 4.5\ V$ $I_{OH} = -2$ @ -55°C inputs $= -2.5$ @ 25°C at V_{IL} $= -4$ @ 125°C (see below)
V_{OL}	Output Low Voltage		0.4			0.4		0.4	V	$V_{CC} = 4.5\ V$ $I_{OL} = 36$ mA inputs at V_{IH} (see below) $V_{CC} = 5.5\ V$ $I_{OL} = 37.5$ mA all inputs at 5.5 V
V_{IH}	Input High Voltage	2.1		1.9			1.7		V	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		1.4			1.1		0.8	V	Guaranteed input low threshold for all inputs
I_F	Input Load Current		-1.5			-1.5		1.4	mA	$V_{CC} = 5.5\ V$ $V_F = 0.4\ V$ on other inputs $V_R = 4\ V$
I_R	Input Leakage Current		2			2		5	μA	$V_{CC} = 5.5\ V$ $V_R = 4\ V$ ground on other inputs
I_{SC}	Output Short Circuit Current	16		18			16		mA	$V_{CC} = 5.5\ V$ one input grounded, output grounded
I_{PD}	Power Dissipation Current (each gate)					13.3			mA	$V_{CC} = 5\ V$ inputs open
t_{pd+}	Turn-off delay			25		80			nsec	$V_{CC} = 5\ V$ see test circuit
t_{pd-}	Turn - on delay			15		40			nsec	$V_{CC} = 5\ V$ see test circuit

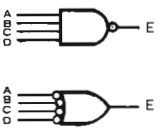
CONNECTION DIAGRAM
(top view)



SCHEMATIC DIAGRAM
(one gate only)



LOGIC FUNCTION



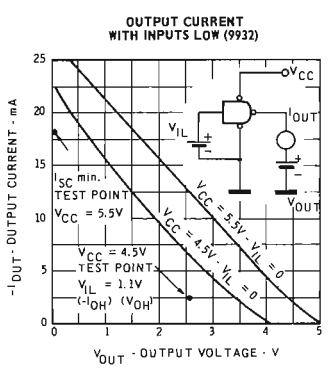
POSITIVE $E = \overline{A \cdot B \cdot C \cdot D}$
(NAND)
LOGIC

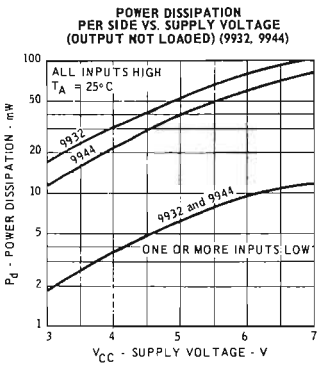
NEGATIVE $E = \overline{A+B+C+D}$
(NOR)
LOGIC

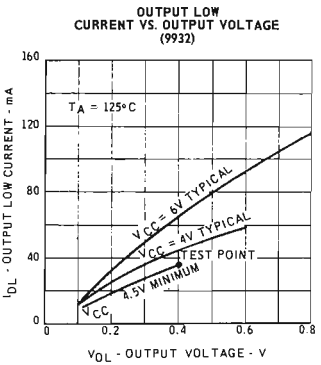
ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V ±10%)

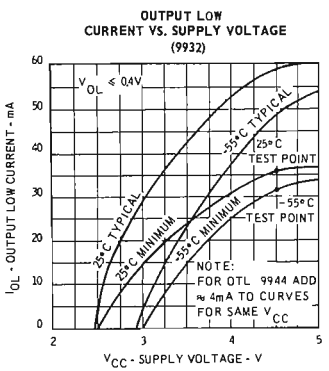
SYMBOL	CHARACTERISTICS	LIMITS						UNIT	CONDITIONS AND COMMENTS
		-55°C		25°C			125°C		
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
V_{OL}	Output Low Voltage		0.4			0.4		0.4	V	V_{CC} = 4.5 V I_{OL} = 36 mA inputs at V_{IH} (see below) V_{CC} = 5.5 V I_{OL} = 40.5 mA all inputs at V_R = 5.25 V
V_{IH}	Input High Voltage	2.1		1.9			1.7		V	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		1.4			1.1		0.8	V	Guaranteed input low threshold for all inputs
I_F	Input Load Current		-1.5			-1.5		-1.4	mA	V_{CC} = 5.5 V V_F = 0.4 V on other inputs V_R = 4 V
I_R	Input Leakage Current		2			2		5	µA	V_{CC} = 5.5 V V_R = 4 V Ground on other inputs
I_{CEX}	Output Leakage Current		50			100		200	µA	V_{CC} = 4.5 V one input grounded, output at V_{CC}
I_{PD}	Power Dissipation Current (each gate)					10			mA	V_{CC} = 5 V inputs open
t_{pd+}	Turn - off delay			15		50			nsec	V_{CC} = 5 V see test circuits
t_{pd-}	Turn - on delay			10		35			nsec	

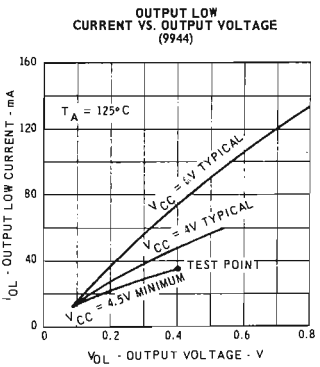
MINIMUM - MAXIMUM AND TYPICAL DC CURVES







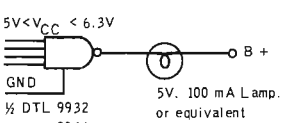




MISCELLANEOUS APPLICATIONS

LAMP DRIVING

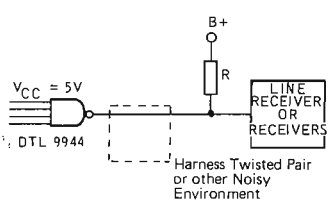
SUGGESTED RATINGS	DIP	FLAT
Power Dissipation	400 mW	240 mW
Max Hot Lamp Current one side only ON	120 mA	100 mA
Max Hot Lamp Current both sides ON	90 mA	75 mA



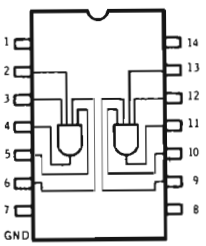
"Cold" lamp current is limited by saturation resistance, emitter resistance, and base current to about 200 to 250 mA. Most significant thermal time constants for 9932 and 9944 : DIP 50 msec Flat 100 msec.
Thermal time constant is measured by forward diode drop in one gate with power pulsed into opposite gate.

INTERFACING

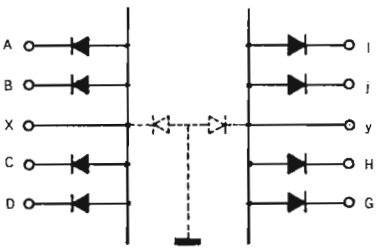
B + up to 12 volts. Line Receiver may have nominal low level of 1 volt; nominal threshold ≈ 4 V and nominal high level 8 V, for example. Resistor selected should be as low as possible consistent with required low input level of receiver, number of receivers, and power dissipation of system For guaranteed operation in both applications the use of selected units is desirable. Operation as a lamp driver requires high gain units, and for interfacing high voltage units may be required.



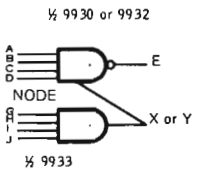
CONNECTION DIAGRAM
(top view)



SCHEMATIC DIAGRAM



LOGIC FUNCTION



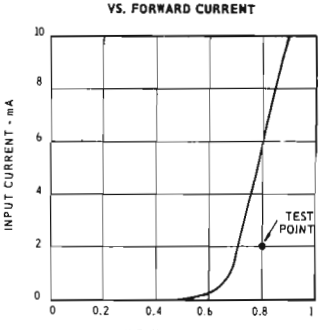
POS. LOGIC $E = \overline{A \cdot B \cdot C \cdot D \cdot G \cdot H \cdot I \cdot J}$

NEG. LOGIC $E = \overline{A + B + C + D + G + H + I + J}$

ELECTRICAL CHARACTERISTICS

SYMBOL	CHARACTERISTICS	LIMITS						UNIT	CONDITIONS AND COMMENTS
		-55°C		25°C		125°			
		Min.	Max.	Min.	Typ. Max.	Min.	Max.		
V_{FD}	Forward Drop Voltage	0.84	0.98	0.70	0.82	0.48	0.62	V	$I_{FD} = 2$ mA applied to output, input grounded
I_R	Reverse Current		2		2		5	µA	$V_R = 4$ V, ground on other inputs
I_R	Output Reverse Current		10		10		25	µA	$V_R = 4$ V on output

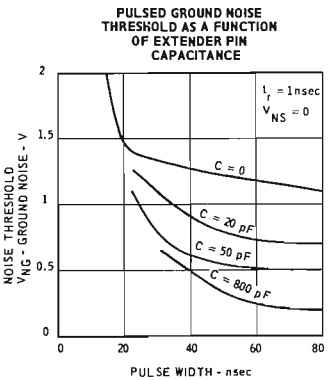
FORWARD VOLTAGE VS. FORWARD CURRENT

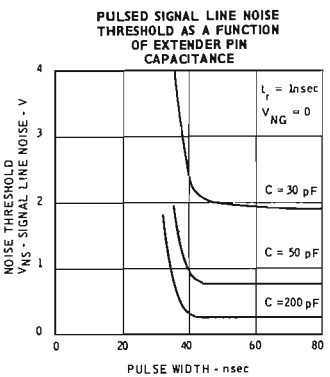


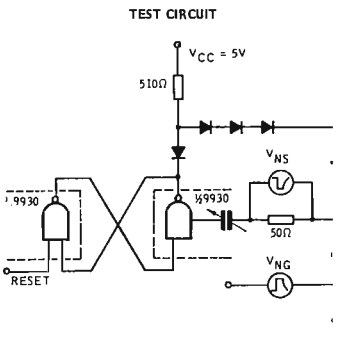
FAN-IN EXTENSION

DTL 9933 elements may be used to extend fan in capability to more than 20 without adversely affecting the noise immunity or load driving capability of the element to which they are connected.
Good practice dictates that extension interconnection paths be as short as possible to minimize the effects of distributed capacitance on circuit performance. The effects of capacitance are summarized on the back page. Typical input capacitance of DTL 9933 is 2 pF and output capacitance is 5 pF.

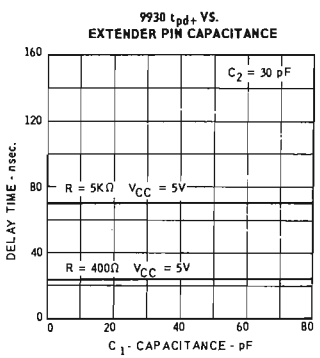
TYPICAL CURVES TO SHOW THE EFFECTS OF EXTENDER PIN CAPACITANCE ON NOISE THRESHOLD OF DTL 9930 DUAL GATE

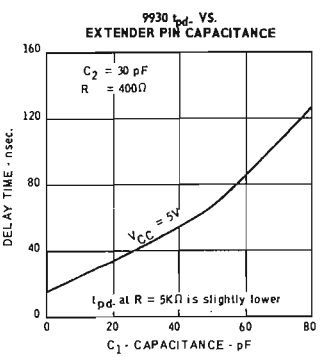


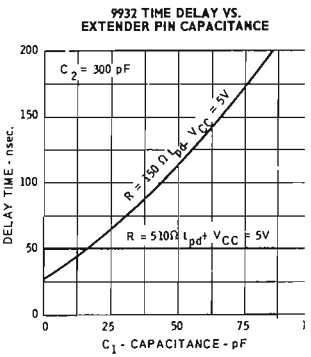


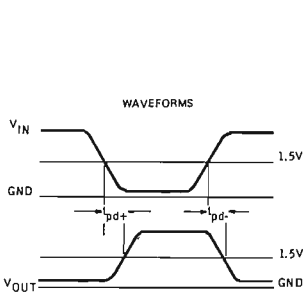


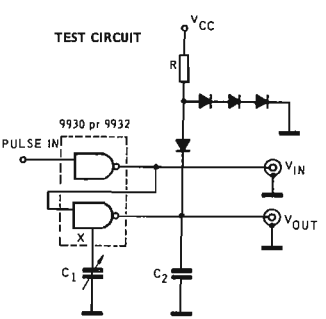
TYPICAL CURVES TO SHOW THE EFFECTS OF EXTENDER PIN CAPACITANCE (Using DTL 9933) ON TIME DELAY OF DTL 9930 DUAL GATE AND DTL 9932 DUAL BUFFER





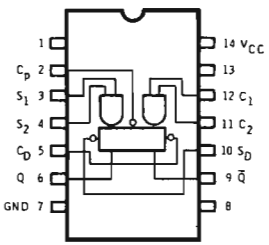




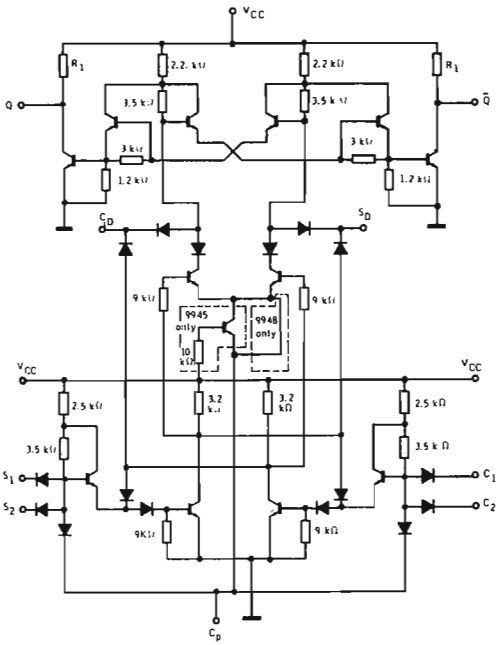


C_1 represents the sum of the DTL 9933 Dual Extender Element output capacitances (~ 5 pF per output) and associated board, connector and wiring capacitances.

CONNECTION DIAGRAM
(top view)



SCHEMATIC DIAGRAM



NOTE: The DTL 9945 incorporates the standard 6KΩ output pull-up resistor, while the DTL 9948 features a 2kΩ output pull-up resistor for improved switching times, thus reducing however the drive capability.

Note :
DTL 9945 - $R_1 = 6k\Omega$
DTL 9948 - $R_1 = 2k\Omega$

LOGIC FUNCTION

Synchronous Entry					Asynchronous Entry				J · K Mode Truth Table			
Inputs				Outputs	Inputs		Outputs		Inputs		Outputs	
t_n				$t_n + 1$					t_n		$t_n + 1$	
S_1	S_2	C_2	C_1	Q	C_D	S_D	Q	$\bar{Q}$	S_1	C_1	Q	$\bar{Q}$
L	X	L	X	NC	H	H	NC	NC	L	H	L	H
L	X	X	L	NC	H	L	H	L	H	L	H	L
X	L	L	X	NC	L	H	L	H	H	H	$\bar{Q}_n$	Q_n
X	L	X	L	NC	L	L	H	H	L	L	Q_n	$\bar{Q}_n$
L	X	H	H	L								
X	L	H	H	L					For J - K Mode Operation :			
H	H	L	X	H					Connected 4 to 9 and 11 to 6.			
H	H	X	L	H								
H	H	H	H	Undeter-mined								

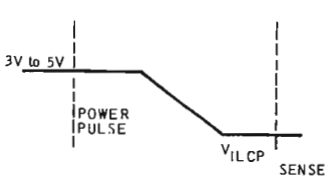
NOTES :

1) Abbreviation used in the body of tables :
   L = low, the more negative voltage level
   H = high, the more positive voltage level (In all cases, unused pins have the same effect as high).
   X = immaterial, either H or L has equal effect
   NC = no change, the clock pulse has no effect on outputs
   Q_n = outputs state at time t_n
2) The L symbol in the S and C input column is defined as meaning that the input does not go high at any time while the clock is high . The H symbol in the S and C input column is defined as meaning that the input is high at same time while the clock is high.

9945 ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V ± 10%)

SYMBOL	CHARACTERISTICS	LIMITS						UNIT	CONDITIONS AND COMMENTS
		-55°C		25°C		125°C			
		Min.	Max.	Min.	Typ. Max.	Min.	Max.		
V_{OH}	Output High Voltage	2.5		2.6		2.5		V	V_{CC} = 4.5 V, I_{OH} = -0.18 mA V_{IL} (see below) on proper asynchronous input
V_{OL}	Output Low Voltage		0.4		0.4		0.4	V	V_{CC} = 4.5 V I_{OL} = 12 mA V_{CC} = 5.5 V I_{OL} = 15 mA V_{IH} (see below) on proper asynchronous input
V_{IH}	Input High Voltage	2.1		1.9		1.7		V	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		1.4		1.1		0.8	V	Guaranteed input low threshold for all inputs
I_F	S & C Inputs Load Current		-0.98		-0.98		-0.92	mA	V_{CC} = 5.5 V V_F = 0.4 V V_R = 4 V on other inputs
I_{FS}	S_D, C_D Inputs Load Current		-2.93		-2.93		-2.57	mA	V_{CC} = 5.5 V V_F = 0.4 V V_R = 4 V on other inputs
I_{FCP}	Clock Input Load Current		-2.93		-2.93		-2.57	mA	V_{CC} = 5.5 V V_F = 0.4 V V_{IL} on S_D
I_R	S, C, S_D, C_D Inputs Leakaga Current		2		2		5	µA	V_{CC} = 5.5 V V_R = 4 V ground on othar inputs
I_{RCP}	Clock Input Leakage Current		10		10		20	µA	V_{CC} = 4 V V_R = 4 V S and C_D inputs grounded
I_{PD}	Power Dissipation Current				14			mA	V_{CC} = 5 V
I_{SC}	Output Short Circuit Current	-0.70	-1.33	-0.70	-1.33	-0.63	-1.30	mA	V_{CC} = 5.5 V high output grounded
t_{pd+}	Turn-off delay			35	75			nsec	V_{CC} = 5 V see test circuit
t_{pd-}	Turn-on delay			30	75			nsec	

CLOCK PULSE DESCRIPTION



$V_{IL\,CP}$ = 1 V @ 25° C
= 0V @ -55° C and 125° C

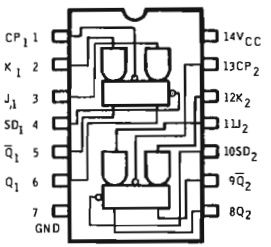
9948 ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V ± 10 %)

SYMBOL	CHARACTERISTICS	LIMITS						UNIT	CONDITIONS AND COMMENTS
		-55°C		25°C			125°C		
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
V_{OH}	Output High Voltage	2.5		2.6			2.5		V	V_{CC} = 4.5 V I_{OH} = - 0.54 mA V_{IL} (see below) on proper asynchronous input
V_{OL}	Output Low Voltage		0.4			0.4		0.4	V	V_{CC} = 4.5 V I_{OL} = 13 mA V_{CC} = 5.5 V I_{OL} = 13.6 mA V_{IH} (see below) on proper asynchronous input
V_{IH}	Input High Voltage	2		1.9			1.7		V	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		1.4			1.1		0.8	V	Guaranteed input low threshold for all inputs
I_F	S & C Inputs Load Current		-0.98			-0.98		-0.92	mA	V_{CC} = 5.5 V V_F = 0.4 V on other inputs V_R = 4 V
I_{FS}	C_D, S_D Input Load Current		-2.93			-2.93		-2.57	mA	V_{CC} = 5.5 V V_F = 0.4 V
I_{FCP}	Clock Input Load Current		-2.35			-2.35		-2.03	mA	V_{CC} = 5.5 V V_F = 0.4 V V_{IL} on S_D
I_R	S, C, S_D, C_D Inputs Leakage Current		2			2		5	µA	V_{CC} = 5.5 V V_R = 4 V ground on other inputs
I_{RCP}	Clock Input Leakage Current		10			10		20	µA	V_{CC} = 4 V V_R = 4 V S and C_D inputs grounded
I_{PD}	Power Dissipation Current					16.2			mA	V_{CC} = 5 V
I_{SC}	Output Short Circuit Current	-2.10	-3.96	-2.10		-3.96	-1.86	-3.54	mA	V_{CC} = 5.5 V high output groundad
t_{pd} +	Turn off delay			30		65			nsec	V_{CC} = 5 V see test circuit
t_{pd} -	Turn on delay			30		75			nsec	

CLOCK PULSE DESCRIPTION : SEE 9945

NOTE : The DTL 9093 and 9094 are respectively dual DTL 9945 and 9948 flip-flops.

CONNECTION DIAGRAM
(top view)



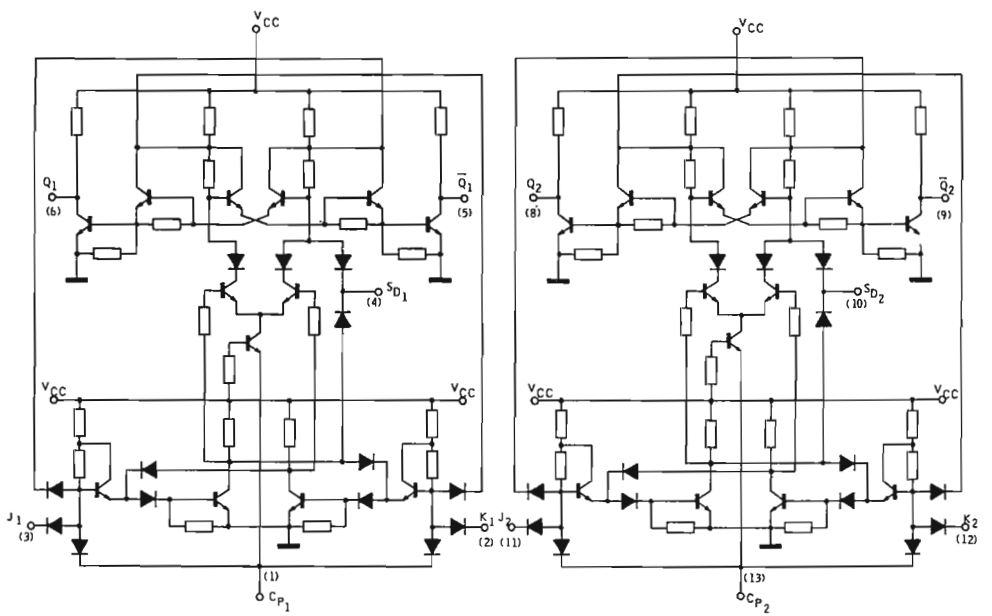
LOGIC FUNCTION

Asynchronous Entry			J-K Mode Truth Teble			
Input	Outputs		Inputs		Outputs	
			t_n		$t_n + 1$	
4 (10)	6 (8)	5 (9)	3 (11)	2 (12)	6 (8)	5 (9)
H	NC	NC	L	H	L	H
L	H	L	H	L	H	L
			H	H	$\bar{Q}_n$	Q_n
			L	L	Q_n	$\bar{Q}_n$

NOTES :

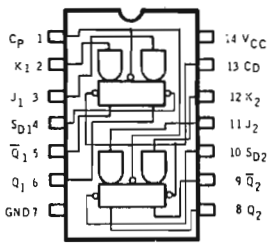
1) Abbreviations used in the body of tables :
   L = low, the more negative voltage level
   H = high, the more positive voltage level
   (In all cases, unused pins have the same effect as high).
   NC = no change, the clock pulse has no effect on outputs.
   Q_n = outputs state at time t_n
2) The L symbol in the J and K input column is defined as meaning that the input does not go high at any time while the clock is high.
   The H symbol in the J and K input column is defined as meaning that the input is high at same time while the clock is high.

SCHEMATIC DIAGRAM 9093/9094 (9093 SHOWN)



NOTE : The DTL 9097 and 9099 are respectively dual DTL 9948 and 9945 flip-flops.

CONNECTION DIAGRAM
(top view)



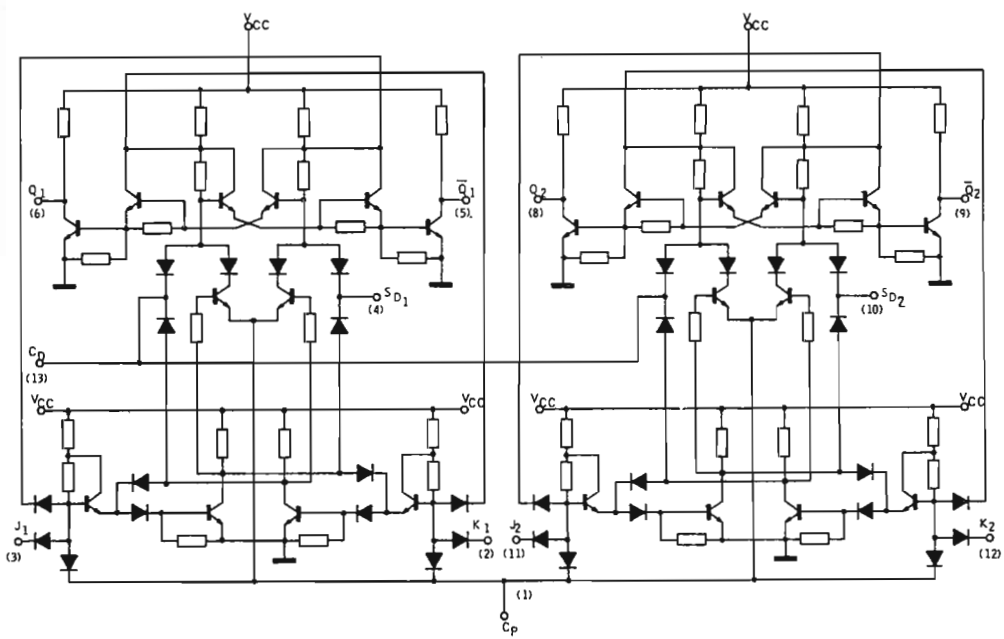
LOGIC FUNCTION

Asynchronous Entry				J-K Mode Truth Table			
Inputs		Outputs		Inputs		Outputs	
				t_n		t_n+1	
13	4 (10)	6 (8)	5 (9)	3 (11)	2 (12)	6 (8)	5 (9)
H	H	NC	NC	L	H	L	H
H	L	H	L	H	L	H	L
L	H	L	H	H	H	$\overline{Q}_n$	Q_n
L	L	H	H	L	L	Q_n	$\overline{Q}_n$

NOTES :

1) Abbreviation used in the body of tables :
   L = low, the more negative voltage level
   H = high, the more positive voltage level
   (In all cases, unused pins have the same effect as high).
   NC = no change, the clock pulse has no effect on outputs.
   Q_n = outputs state at time t_n
2) The L symbol in the J and K input column is defined as meaning that the input does not go high at any time while the clock is high.
   The H symbol in the J and K input column is defined as that meaning the input is high at same time while the clock is high.

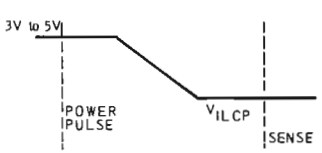
SCHEMATIC DIAGRAM 9097/9099 (9097 SHOWN)



ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V ± 10 %)

SYMBOL	CHARACTERISTICS	LIMITS						UNIT	CONDITIONS AND COMMENTS
		-55°C		25°C		125° C			
		Min.	Max.	Min.	Typ. Max.	Min.	Max.		
V_{OH}	Output High Voltage	2.5		2.6		2.5		V	V_{CC} = 4.5 V I_{OH} = - 0.18 mA V_{IL} (see below) and V_R = 4 V on asynchronous inputs
V_{OL}	Output Low Voltage		0.4		0.4		0.4	V	V_{CC} = 4.5 V I_{OL} = 13.8 mA V_{CC} = 5.5 V I_{OL} = 15 mA Ground and V_R = 4 V on asynchronous inputs
V_{IL}	Input Low Voltage		1.4		1.1		0.8	V	Guaranteed input low threshold for all inputs
V_{IH}	Input High Voltage	2.1		1.9		1.7		V	Guaranteed input high threshold for all inputs
I_F	Input Load Current J and K Inputs		-0.98		-0.98		-0.92	mA	V_{CC} = 5.5 V V_F = 0.4 V
I_{FCP}	Clock Input Load Current 9093 9099		 -2.93 -5.86		 -2.93 -5.86		 -2.57 -5.14	mA	V_{CC} = 5.5 V V_F = 0.4 V V_{IL} (see above) on asynchronous input
I_{FS}	Set Input Load Current		-2.2		-2.2		-1.93	mA	V_{CC} = 5.5 V V_F = 0.4 V ground on J inputs
I_{FC}	Clear Input Load Current		-4.40		-4.40		-3.86	mA	V_{CC} = -5.5 V V_F = 0.4 V Ground on K inputs
I_R	Input Leakage Current J and K Inputs		2		2		5	µA	V_{CC} = 5.5 V V_R = 4 V Ground on clock
I_{RS}	Set Input Leakage Current		2		2		5	µA	V_{CC} = 5.5 V V_R = 4 V Ground on K inputs
I_{RC}	Clear Input Leakage Current		4		4		10	µA	V_{CC} = 5.5 V V_R = 4 V Ground on J inputs
I_{RCP}	Clock Input Leakage Current 9093 9099		 10 20		 10 20		 20 40	µA	V_{CC} = 4 V V_R = 4 V Ground on J inputs
I_{SC}	Output Short Circuit Current	-0.70	-1.33	0.70	-1.33	-0.63	-1.30	mA	V_{CC} = 5.5 V High output grounded
I_{PD}	Power Dissipation Current				28			mA	V_{CC} = 5 V
t_{pd+}	Turn-off delay			35	75			nsec	V_{CC} = 5 V
t_{pd-}	Turn-on delay			30	75			nsec	see test circuit

CLOCK PULSE DESCRIPTION :



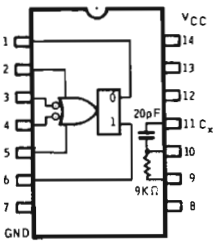
V_{ILCP} = 1 V @ 25° C
= 0V @ -55° C and 125° C

ELECTRICAL CHARACTERISTICS ($V_{CC} = 5\ V \pm 10\%$)

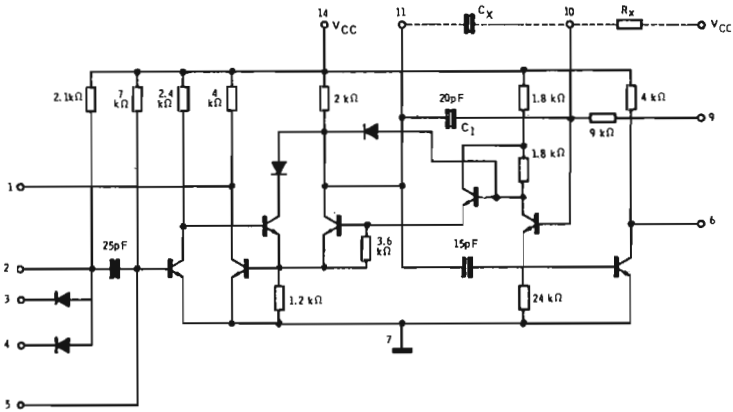
SYMBOL	CHARACTERISTICS	LIMITS						UNIT	CONDITIONS AND COMMENTS
		-55°C		25°C		125°C			
		Min.	Max.	Min.	Typ. Max.	Min.	Max.		
V_{OH}	Output High Voltage	2.5		2.6		2.5		V	$V_{CC} = 4.5\ V$ $I_{OH} = -0.54\ mA$ V_{IL} (see below) and $V_R = 4\ V$ on asynchronous inputs
V_{OL}	Output Low Voltage		0.4		0.4		0.4	V	$V_{CC} = 4.5\ V$ $I_{OL} = 12.3\ mA$ $V_{CC} = 5.5\ V$ $I_{OL} = 13.6\ mA$ Ground and $V_R = 4\ V$ on esynchronous inputs
V_{IH}	Input High Voltage	2.1		1.9		1.7		V	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		1.4		1.1		0.8	V	Guaranteed input low threshold for all inputs
I_F	Input Load Current J and K Inputs		-0.98		-0.98		-0.92	mA	$V_{CC} = 5.5\ V$ $V_F = 0.4\ V$
I_{FCP}	Clock Input Load Current 9094 9097		 -2.35 -4.68		 -2.35 -4.68		 -2.03 -4.04	mA	$V_{CC} = 5.5\ V$ $V_F = 0.4\ V$ V_{IL} (see above) on asynchronous input
I_{FS}	Set Input Load Current		-2.2		-2.2		-1.93	mA	$V_{CC} = 5.5\ V$ $V_F = 0.4\ V$ Ground on J input
I_{FC}	Clear Input Load Current		4.4		4.4		3.86	mA	$V_{CC} = 5.5\ V$ $V_F = 0.4\ V$ Ground on K inputs
I_R	Input Leakage Current J and K Inputs		2		2		5	µA	$V_{CC} = 5.5\ V$ $V_R = 4\ V$ Ground on clock
I_{RCP}	Clock Input Leakage Current 9094 9097		 10 20		 10 20		 20 40	µA	$V_{CC} = 4\ V$ $V_R = 4\ V$ Ground on J inputs
I_{RS}	Set Input Leakage Current		2		2		5	µA	$V_{CC} = 5.5\ V$ $V_R = 4\ V$ Ground on K inputs
I_{RC}	Clear Input Leakage Current		4		4		10	µA	$V_{CC} = 5.5\ V$ $V_R = 4\ V$ Ground on J inputs
I_{SC}	Output Short Circuit Current	-2.1	-3.96	-2.1	-3.96	-1.86	-3.54	mA	$V_{CC} = 5.5\ V$ High output grounded
I_{PD}	Power Dissipation Current				32.4			mA	$V_{CC} = 5\ V$
t_{pd+}	Turn-off delay			30	65			nsec	$V_{CC} = 5\ V$ see test circuit
t_{pd-}	Turn-on delay			30	75			nsec	

CLOCK PULSE DESCRIPTION : **SEE 9093 - 9099**

LOGIC DIAGRAM
(top view)



SCHEMATIC DIAGRAM



GENERAL DESCRIPTION :

The DTL 9951 Monostable Multivibrator provides complementery output pulses which are typical 100 nsec wide. This pulse width is adjustable by the addition of external discrete passive components.
The output pulse width is very stable as either V_{CC} or temperature (or both) is varied when an external timing resistor is used instead of the internal diffused resistor.

ABSOLUTE MAXIMUM RATINGS (above which useful life may be impaired) (1)

Output Current, into outputs	50 mA
Current into Pin 10	5 mA

NOTE: 1) In addition to abs. max. rating, pag. 87

ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V ± 10%)

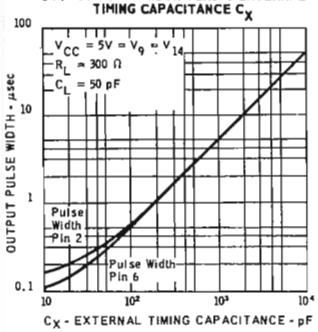
SYMBOL	CHARACTERISTICS	LIMITS						UNIT	CONDITIONS AND COMMENTS
		-55°C		25°C		125°C			
		Min.	Max.	Min.	Typ. Max.	Min.	Mex.		
V_{OH}	Output High Voltage	2.5		2.5		2.5		V	V_{CC} = 4.5 V I_{OH} = - 0.18 mA Pin 2 grounded, Pin 9 at V_{CC}
V_{OL}	Output Low Voltage		0.4		0.4		0.45	V	V_{CC} = 4.5 V I_{OL} = 15 mA V_{CC} = 5.5 V I_{OL} = 15 mA when testing Pin 1, ground Pin 10 when testing Pin 6, V_{CC} on Pin 9
I_F	Input Load Current		-3.2		-3.2		-3	mA	V_{CC} = 5.5 V V_F = 0 V V_R = 4 V
I_R	Input Leakage Current		5		5		10	µA	V_{CC} = 5.5 V V_R = 4 V Ground on Pin 2
I_{PD}	Power Dissipation Current				9			mA	V_{CC} = 5 V inputs grounded, V_{CC} on Pin 9
t_{pd+}	Turn-off delay (Pin 6)				40			nsec	V_{CC} = 5 V see test circuit
t_{pd-}	Turn-on delay (Pin 1)				40			nsec	
P_W	Pulse width (Pin 1)			90	220			nsec	
P_W	Pulse width (Pin 6)			70	160			nsec	

RULES FOR USE OF DTL 9951

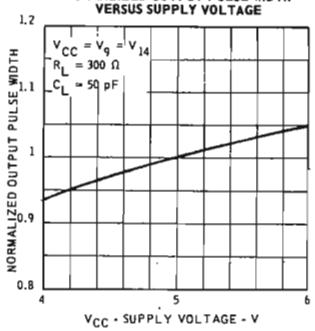
1) With Pin 9 connected to V_{CC} and no external capacitor (C_X), the output pulse width is approximately 150 nsec.
2) With Pin 9 connected to V_{CC} and an external capacitor (C_X) connected between Pins 10 and 11, the output pulse width (T) is: $T \approx 4.5\ (C_X + 20)$ with C_X in pF and T in nsec.
3) For Improved pulse width control, Pin 9 is left open and a stable external resistor (R_X) of 9 kΩ minimum to 15 kΩ maximum is connected from Pin 10 to V_{CC}. The output pulse width is given by the expression : $T \approx 0.5\ R_X\ (C_X + 20)$ with R_X in kΩ, C_X in pF and T in nsec.
4) The output duty cycle (pulse width/period) should not exceed 40%. It may be increased to 50% by adding a 2 kΩ resistor between Pin11 and V_{CC}. Higher duty cycles are obtainable but the output pulse width and performance are less predictable.
5) The maximum input fall time to trigger : 15 nsec for a 1.4 volt swing; 40 nsec for a 2.4 volt swing; 80 nsec for a 4.4 volt swing.
6) The AC sensitivity of the inputs may be decreased by connecting a capacitor between Pin 5 and ground.
7) The minimum pulse width at output Pin 1 is approximately 100 nsec. This pulse width may be decreased to 50 nsec by connecting a 10 kΩ resistor between Pin 5 and V_{CC}.

TIMING CHARACTERISTICS

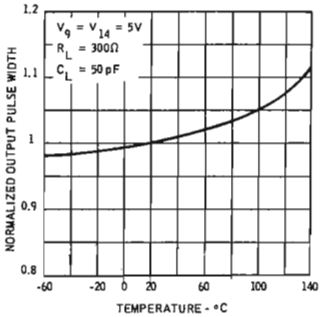
OUTPUT PULSE WIDTH VERSUS EXTERNAL TIMING CAPACITANCE C_X



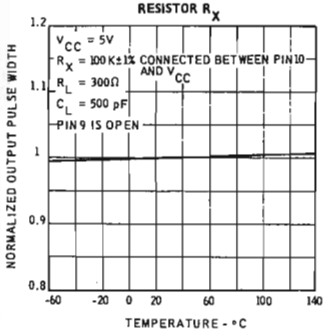
NORMALIZED OUTPUT PULSE WIDTH VERSUS SUPPLY VOLTAGE



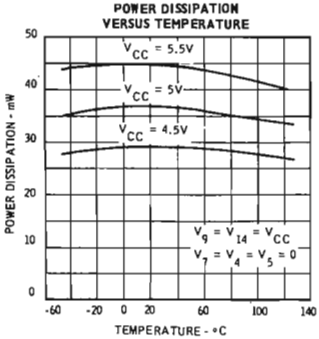
NORMALIZED OUTPUT PULSE WIDTH VERSUS TEMPERATURE



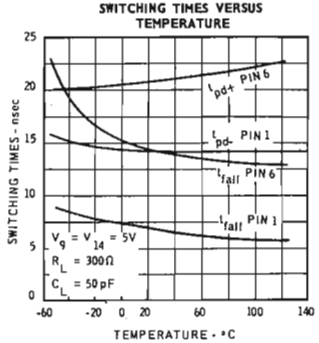
NORMALIZED OUTPUT PULSE WIDTH VERSUS TEMPERATURE USING EXTERNAL TIMING RESISTOR R_X



POWER DISSIPATION VERSUS TEMPERATURE

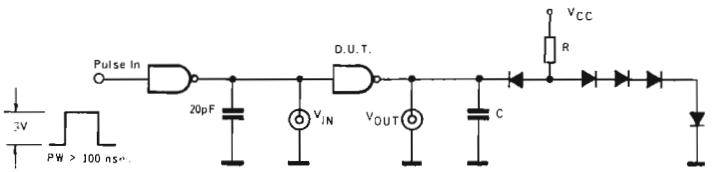


SWITCHING TIMES VERSUS TEMPERATURE



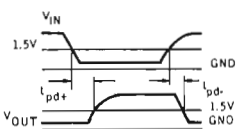
SWITCHING TIME TEST CIRCUITS

9930 - 9936 - 9946 - 9962 GATES t_{pd} TEST CIRCUIT



All diodes BAY 74 or equivalent
V_{CC} at PIN 14, GND at PIN 7

WAVEFORMS

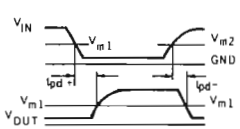


TEST CONDITIONS

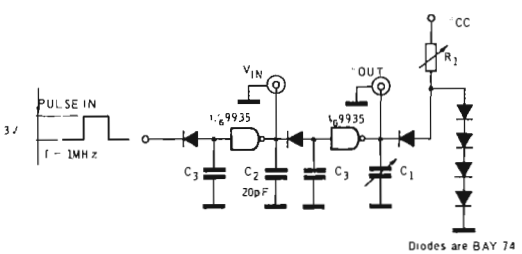
	R	C
t_{pd+}	3.9 kΩ	30 pF
t_{pd-}	400 Ω	50 pF

9935 GATE t_{pd} TEST CIRCUIT

WAVEFORMS



V_{m1}	V_{m2}
1.5 V	1.3V



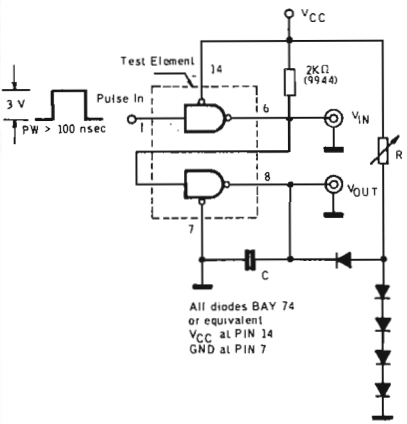
Diodes are BAY 74

TEST CONDITIONS

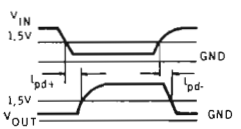
	R_1	C_1	C_2	C_3
t_{pd+}	3.9 KΩ	30pF	20pF	5pF
t_{pd-}	400 Ω	50pF	20pF	5pF

SWITCHING TIME TEST CIRCUITS

9932 · 9944 GATES t_{pd} TEST CIRCUIT



WAVEFORMS

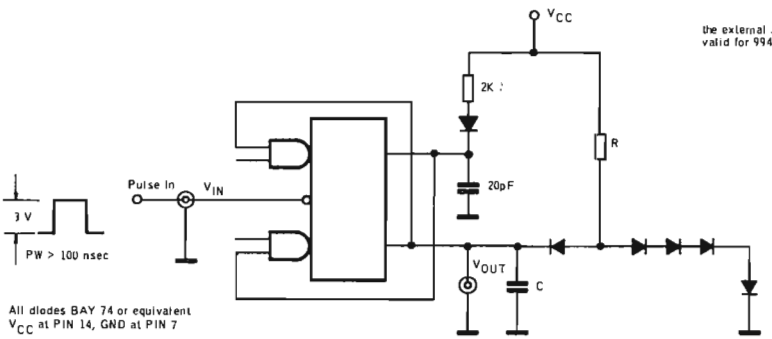


TEST CONDITIONS

	R	C
9944 t_{pd+}	510Ω	20pF
9944 t_{pd-}	150Ω	100pF
9932 t_{pd+}	510Ω	500pF
9932 t_{pd-}	150Ω	500pF

SWITCHING TIME TEST CIRCUITS

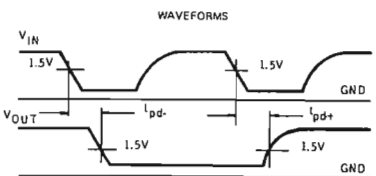
9945 - 9948 - 9093 - 9094 - 9097 - 9099 FLIP-FLOPS t_{pd} TEST CIRCUIT



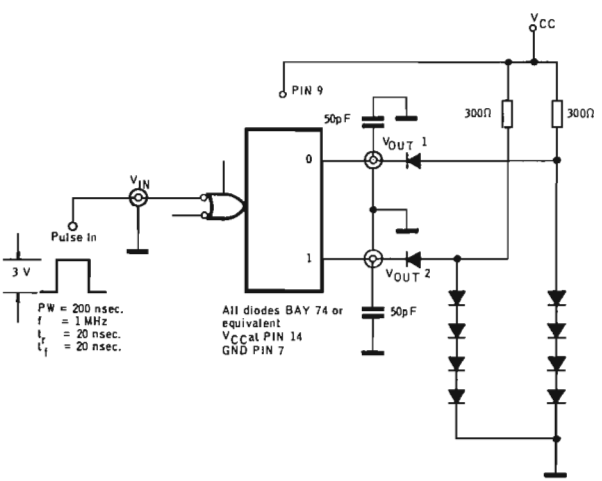
TEST CONDITIONS

	R	C
t_{pd+}	2KΩ	30pF
t_{pd-}	330Ω	50pF

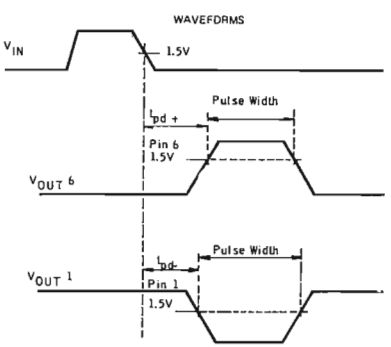
WAVEFORMS



9951 MONOSTABLE t_{pd} TEST CIRCUIT



WAVEFORMS



Diode-transistor logic

STANDARD TEMPERATURE RANGE 0°C ÷ 75°C

- COMPATIBLE WITH TTL, LPDTL PRODUCTS
- NOISE IMMUNITY 1 V
- OUTPUT DRIVE CAPABILITY OF 10
- POWER DISSIPATION 8.5mW PER GATE
- FAN-IN EXPANSION CAPABILITY
- WIRED-OR CAPABILITY
- SAME PIN CONFIGURATION AS THE CORRESPONDING TTL AND LPDTL PRODUCTS

ORDERING NUMBERS

U6A XXXX 59X (for ceramic DIP; XXXX is type number)
U7A XXXX 59X (for plastic DIP; XXXX is type number)
U3I XXXX 59X (for flat package; XXXX is type number)

The SGS Diode-Transistor Logic (DTL) family consists of a set of compatible integrated circuits designed for medium power, medium speed applications.
The circuits are fabricated within a silicon monolithic substrate using the standard planar epitaxial process.
These devices are available in the following packages: dual in-line ceramic package, dual in-line plastic package, flat ceramic package.

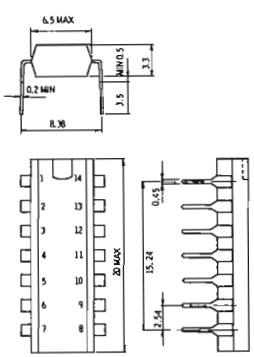
ABSOLUTE MAXIMUM RATINGS
(above which the useful life may be impaired)

Supply Voltage (V_{CC}), Continuous	8 V
Supply Voltage (V_{CC}), Pulsed < 1 sec.	12 V
Output Current, Into Outputs	
DTL 9932 - 9944	100 mA
Other Elements	30 mA
Input Forward Current	-10 mA
Input Reverse Current	1 mA
Storage Temperature, Plastic	-55°C to 125°C
Storage Temperature, Ceramic	-65°C to 150°C
Temperature (Amb.) Under Bias, Ceramic	-55°C to 125°C

OPERATING CONDITIONS

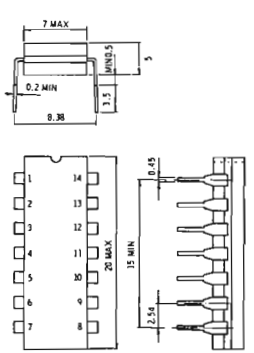
Temperature Range	0° to 75°C
Supply Voltage	5V ± 5%

PHYSICAL DIMENSIONS
14-pin plastic DIP



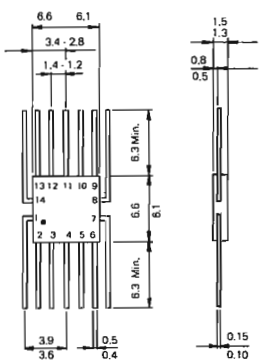
Note : all dimensions in mm.

PHYSICAL DIMENSIONS
14-pin ceramic DIP



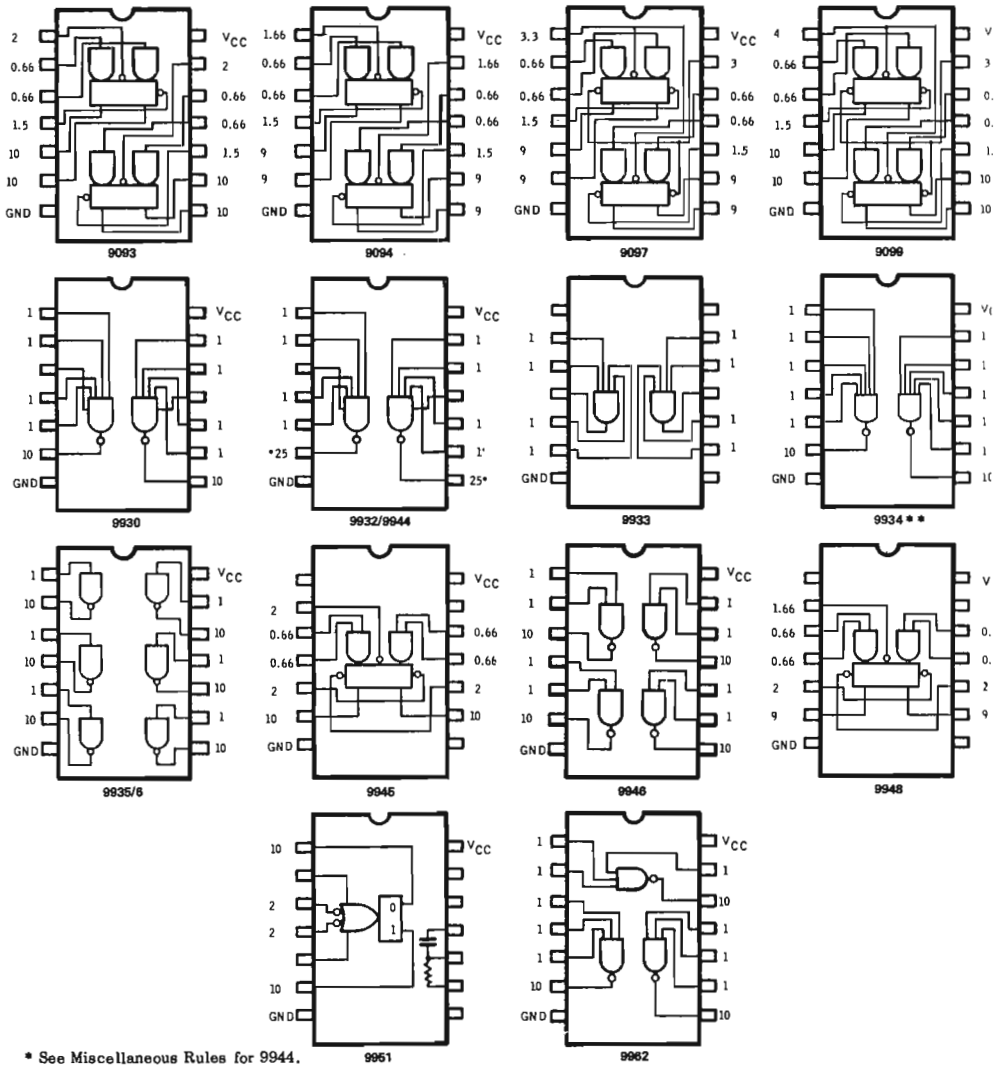
Note : all dimensions in mm.

PHYSICAL DIMENSIONS
Flat package



NOTE : All dimensions in mm.

INPUT - OUTPUT LOAD/DRIVE FACTORS



* See Miscellaneous Rules for 9944.
** Plastic DIP only.

MISCELLANEOUS RULES

The number of elements driven by an output terminal may consist of any combination of elements whose sum of inp load factors does not exceed the output drive factor.
An external resistor should be used with 9944. With an external resistor R the following output drive factors will obtained:

R = 6 KΩ	Drive Factor = 26
R = 2 KΩ	Drive Factor = 25
R = 1 KΩ	Drive Factor = 23
R = 510Ω	Drive Factor = 20

For increased output drive, the inputs and outputs of 1/2 DTL 9944 may be paralleled, up to 4 common outputs. For 4 paralleled elements:

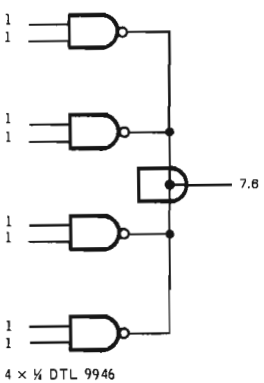
Each combined input, load factor = 4
Each combined output, drive factor = 100 (R = 2 KΩ)

"WIRED OR" CONNECTION

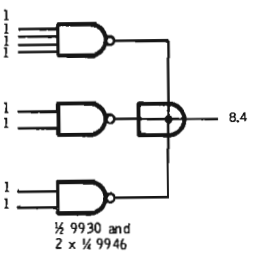
. Outputs of DTL gates may be tied together for the "wired OR" function:
$(\overline{ABCD} \cdot \overline{GHIJ} = \overline{ABCD + GHIJ})$. Subtract, for each added gate, 0.8 unit load from output drive factor.

. Outputs of DTL 9932 may not be tied together for the "wired OR" function.

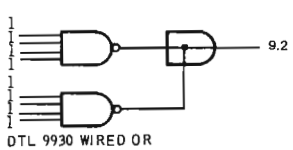
"WIRED OR" Examples:



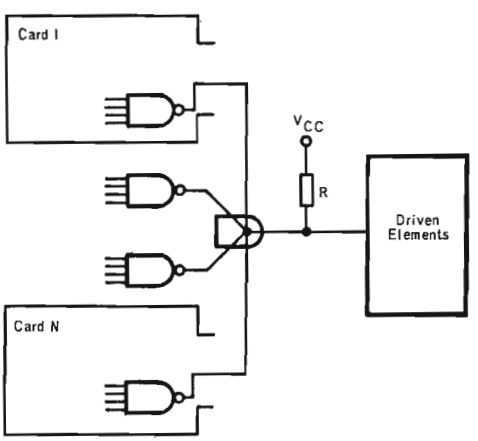
4 × ¼ DTL 9946



½ 9930 and
2 × ¼ 9946



DTL 9930 WIRED OR



Each output driver is 1/2 DTL 9944. Note that the DTL 9944 is a direct high fan-out replacement for DTL 9930, except that an external resistor must be used. The F.O. will be the same as one 1/2 DTL 9944 buffer used with that resistor.

DELAY TIME PERFORMANCE INTO CAPACITIVE LOADS

Most delay attributable to capacitive loads is associated with the positive going output. Two RC time constants a seen in the positive going output. In the 1st time period, from the saturated low level to threshold, the R of the RC tin constant can be given by 6 KΩ in parallel with $\frac{3.75\ K\Omega}{\text{active fanout}}$.

Above the threshold which occurs at about 1.4 to 1.5 volts at 25°C, the R of the 2nd RC time constant is 6 kΩ and t rate of the voltage rise above threshold is slow. The logic signal propagates through at the threshold level, so volta rise above threshold does not affect speed. By noting that both rise domains drive toward V_{CC}, the voltage ri waveform may be calculated. DTL gate inputs are ~ 2 pf per input for active or inactive fanout; the remaining capa tance is from board, wiring, and connectors.

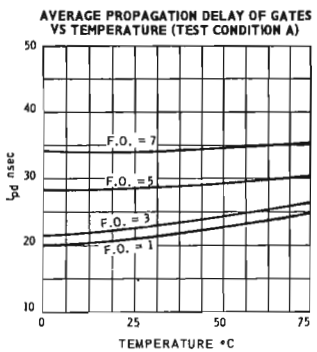


FIG. 1

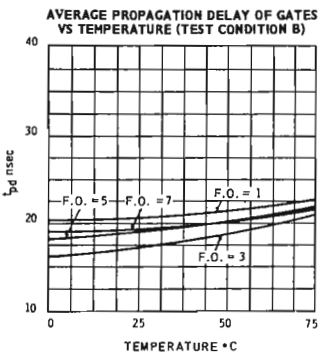
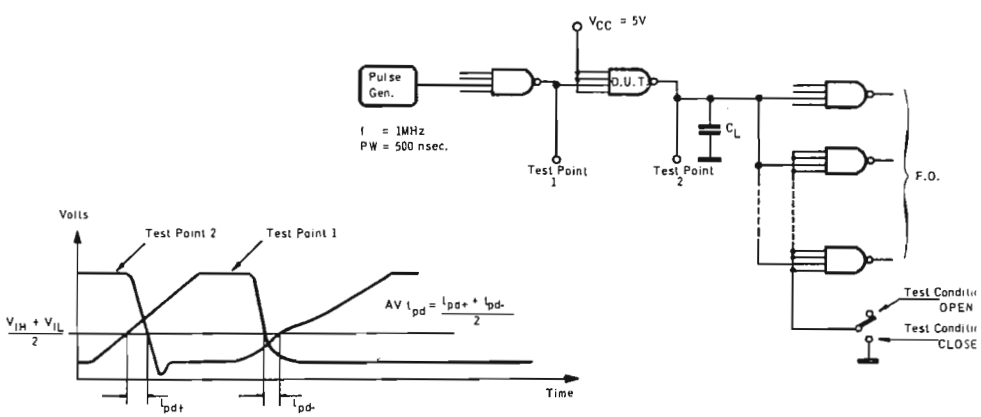


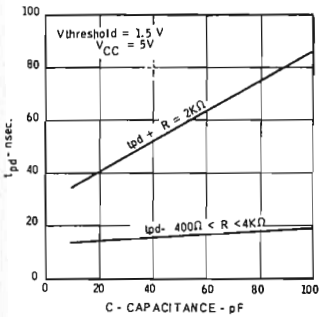
FIG. 2

TEST CONDITIONS FOR FIG. 1 AND 2

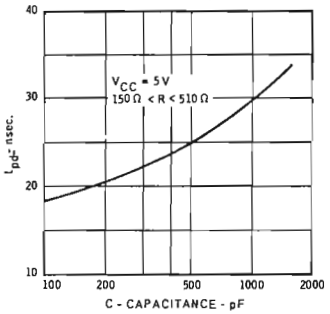


t_{pd} CURVES VERSUS OUTPUT CAPACITANCE (T_A = 25°C unless otherwise noted)

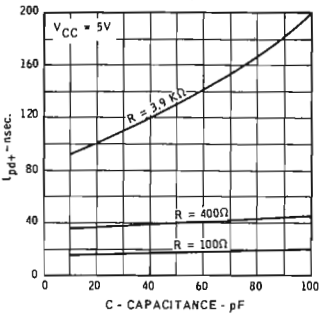
t_{pd} OF GATES VERSUS CAPACITANCE



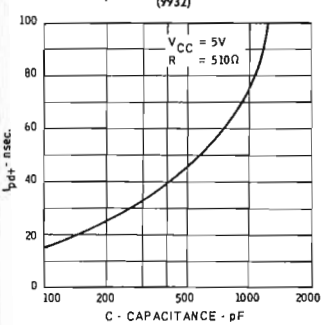
t_{pd-} VERSUS CAPACITANCE (9932 - 9944)



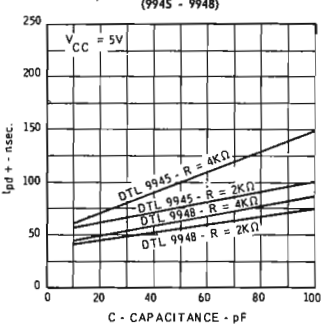
t_{pd+} VERSUS CAPACITANCE (9944)



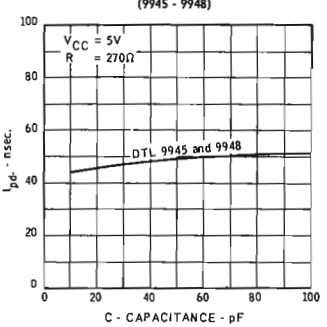
t_{pd+} VERSUS CAPACITANCE (9932)



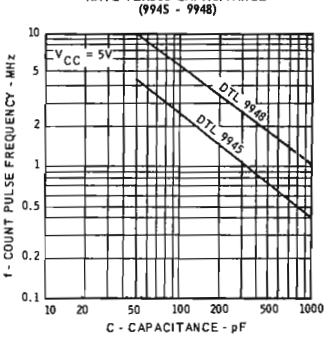
t_{pd+} VERSUS CAPACITANCE (9945 - 9948)



t_{pd-} VERSUS CAPACITANCE (9945 - 9948)

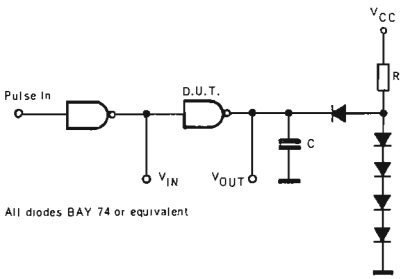


MAXIMUM BINARY COUNTING RATE VERSUS CAPACITANCE (9945 - 9948)



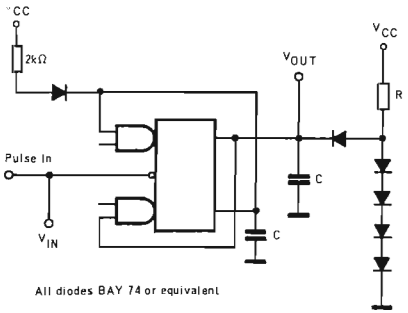
TEST CIRCUITS

GATES

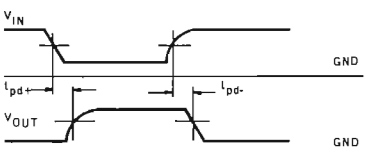


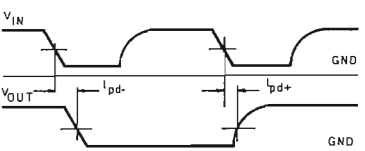
All diodes BAY 74 or equivalent

FLIP-FLOPS



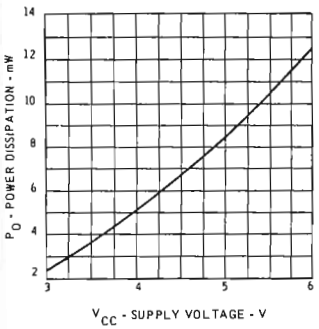
All diodes BAY 74 or equivalent



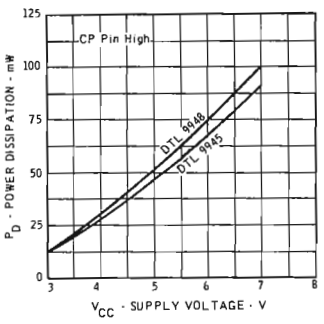


POWER DISSIPATION CURVES (T_A = 25°C unless otherwise noted)

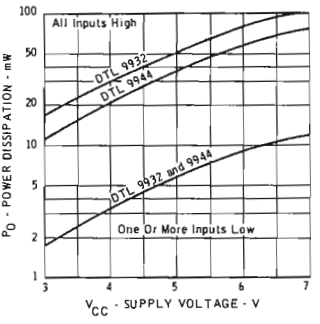
POWER DISSIPATION
VS SUPPLY VOLTAGE, EACH GATE
(9930, 9936, 9946, 9962)



POWER DISSIPATION
VS. SUPPLY VOLTAGE
(9945 - 9948)

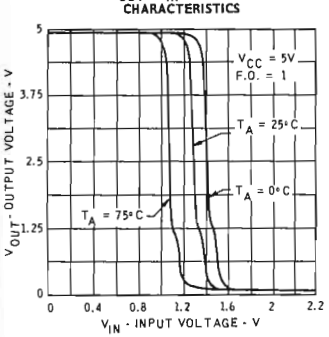


POWER DISSIPATION
PER SIDE VS. SUPPLY VOLTAGE
(OUTPUT NOT LOADED) (9932 - 9944)

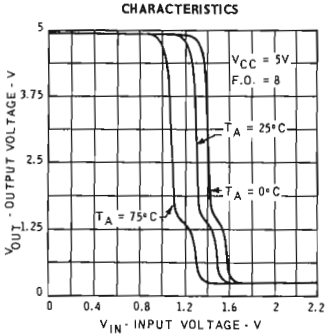


TRANSFER CHARACTERISTICS

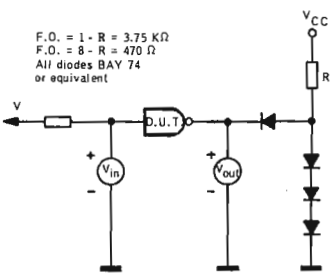
V_{OUT} - V_{IN} TRANSFER
CHARACTERISTICS



V_{OUT} - V_{IN} TRANSFER
CHARACTERISTICS



TEST CIRCUIT



NOISE IMMUNITY

V_{NS} is the maximum voltage which may be applied in the signal line without affecting the driven gate.
V_{NG} is the maximum voltage which may be applied in the ground connection without affecting the driven gate.
The variation of these two noise voltages with temperature and V_{CC} is shown in figures 1 through 5.
The guaranteed worst case noise curve shown on figure 5 is obtained by:

$$V_N = |V_{IL} - V_{OL}| \quad \text{or} \quad |V_{OH} - V_{IH}| \quad \text{whichever is smaller.}$$

where: V_{IL} = Maximum Low Input Voltage that guarantees V_{OH}

V_{OL} = Maximum Low Output Voltage

V_{IH} = Minimum High Input Voltage that guarantees V_{OL}

V_{OH} = Minimum High Output Voltage

(See the table of forcing functions and test limita for the values of these parameters).

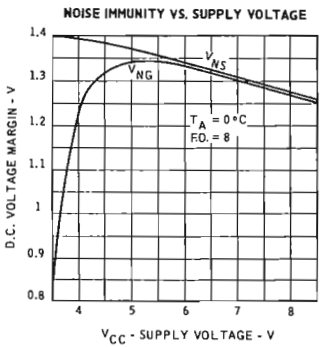


FIG. 1

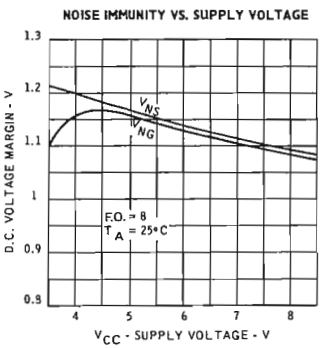


FIG. 2

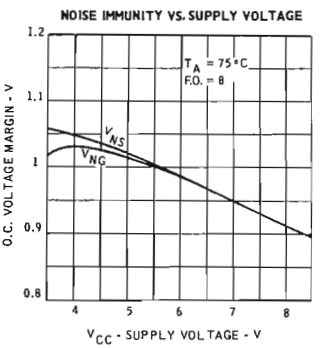


FIG. 3

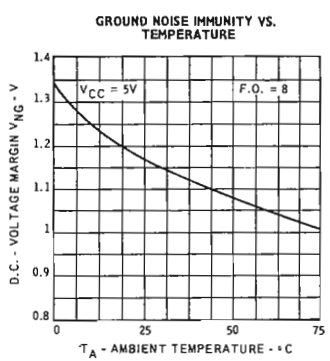


FIG. 4

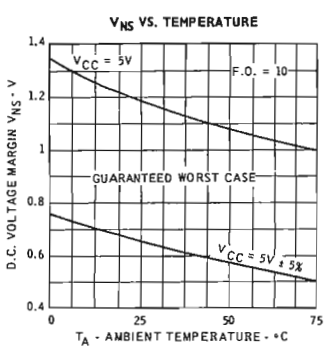
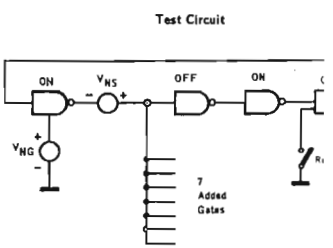
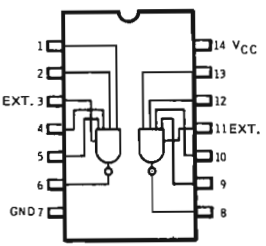


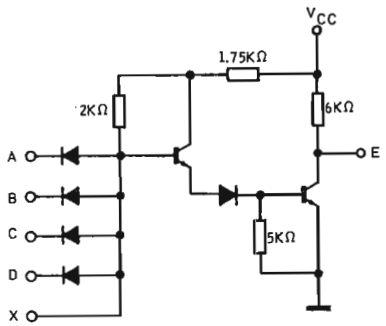
FIG. 5



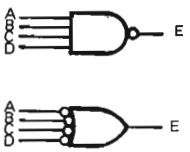
CONNECTION DIAGRAM
(top view)



SCHEMATIC DIAGRAM
(one gate only)



LOGIC FUNCTION



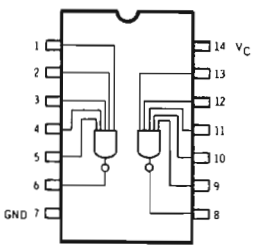
POSITIVE (NAND) LOGIC $E = \overline{A \cdot B \cdot C \cdot D}$

NEGATIVE (NOR) LOGIC $E = \overline{A + B + C + D}$

ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V ± 5%)

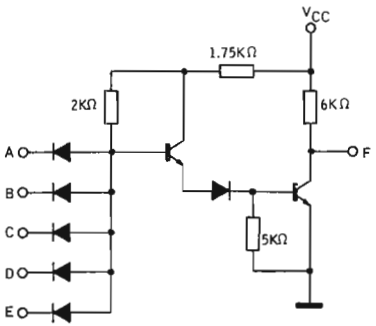
SYMBOL	CHARACTERISTICS	LIMITS 0°C Min.	0°C Max.	25°C Min.	25°C Typ.	25°C Max.	75°C Min.	75°C Max.	UNIT	CONDITIONS AND COMMENTS
V_{OH}	Output High Voltage	2.5		2.6	3.5		2.5		V	V_{CC} = 4.75V, I_{OH} = -0.18 mA one input at V_{IL} (see below)
V_{OL}	Output Low Voltage		0.45		0.25	0.45		0.45	V	V_{CC} = 4.75V, I_{OL} = 13.3 mA inputs at V_{IH} (see below) V_{CC} = 5.25V, I_{OL} = 15.2 mA all inputs at V_R = 5.25 V
V_{IH}	Input High Voltage	2		1.9			1.8		V	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		1.2			1.1		0.95	V	Guaranteed input low threshold for all inputs
I_F	Input Load Current		-1.52		-1.1	-1.52		-1.52	mA	V_{CC} = 5.25 V, V_F = 0.45 V on other inputs V_R = 4 V
I_R	Input Leakage Current		5			5		10	μA	V_{CC} = 5.25 V, V_R = 4 V ground on other inputs
I_{SC}	Output Short Circuit Current	-0.65	-1.33	-0.65		-1.33	-0.56	-1.33	mA	V_{CC} = 5.25V one input grounded, output grounded
I_{PD}	Power Dissipation Current (each gate)				3	4			mA	V_{CC} = 5V inputs open
$t_{pd}+$	Turn-Off Delay			25	45	100			nsec	V_{CC} = 5 V see test circuit
$t_{pd}-$	Turn-On Delay			10	20	40			nsec	V_{CC} = 5 V see test circuit

CONNECTION DIAGRAM
(top view)

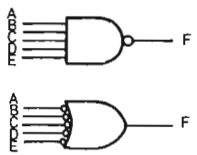


Plastic DIP only

SCHEMATIC DIAGRAM
(one gate only)



LOGIC FUNCTION



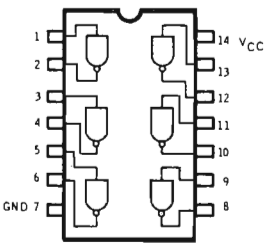
POSITIVE (NAND) LOGIC $F = \overline{A \cdot B \cdot C \cdot D \cdot E}$

NEGATIVE (NOR) LOGIC $F = \overline{A+B+C+D+E}$

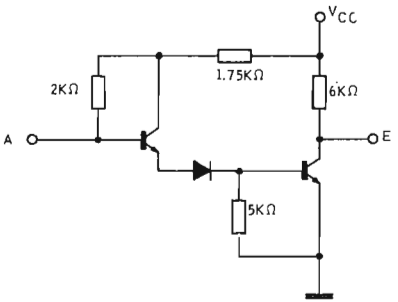
ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V ± 5%)

SYMBOL	CHARACTERISTICS	LIMITS 0°C Min.	LIMITS 0°C Max.	LIMITS 25°C Min.	LIMITS 25°C Typ.	LIMITS 25°C Max.	LIMITS 75°C Min.	LIMITS 75°C Max.	UNIT	CONDITIONS AND COMMENTS
V_{OH}	Output High Voltage	2.5		2.6	3.5		2.5		V	V_{CC} = 4.75V, I_{OH} = -0.18 mA one input at V_{IL} (see below)
V_{OL}	Output Low Voltage		0.45		0.25	0.45		0.45	V	V_{CC} = 4.75V, I_{OL} = 13.3 mA inputs at V_{IH} (see below) V_{CC} = 5.25V, I_{OL} = 15.2 mA all inputs at V_R = 5.25 V
V_{IH}	Input High Voltage	2		1.9			1.8		V	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		1.2			1.1		0.95	V	Guaranteed input low threshold for all inputs
I_F	Input Load Current		-1.52		-1.1	-1.52		-1.52	mA	V_{CC} = 5.25 V, V_F = 0.45 V on other inputs V_R = 4 V
I_R	Input Leakage Current		5			5		10	μA	V_{CC} = 5.25 V, V_R = 4 V ground on other inputs
I_{SC}	Output Short Circuit Current	-0.65	-1.33	-0.65		-1.33	-0.56	-1.33	mA	V_{CC} = 5.25V one input grounded, output grounded
I_{PD}	Power Dissipation Current (each gate)				3	4			mA	V_{CC} = 5V inputs open
$t_{pd}+$	Turn-Off Delay			25	45	100			nsec	V_{CC} = 5 V see test circuit
$t_{pd}-$	Turn-On Delay			10	20	40			nsec	V_{CC} = 5 V see test circuit

CONNECTION DIAGRAM
(top view)



SCHEMATIC DIAGRAM
(one gate only)



LOGIC FUNCTION

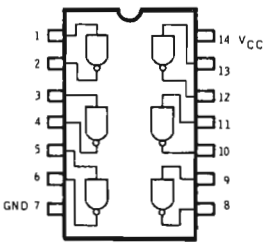
$A = \overline{E}$

ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V ± 5%)

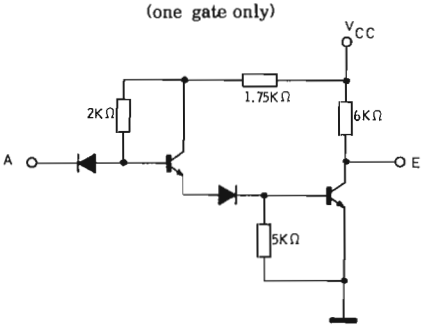
SYMBOL	CHARACTERISTICS	LIMITS 0°C Min.	LIMITS 0°C Max.	LIMITS 25°C Min.	LIMITS 25°C Typ.	LIMITS 25°C Max.	LIMITS 75°C Min.	LIMITS 75°C Max.	UNIT	CONDITIONS AND COMMENTS
V_{OH}	Output High Voltage	2.5		2.6	3.5		2.5		V	V_{CC} = 4.75 V, I_{OH} = -0.18 mA one input at V_{IL} (see below)
V_{OL}	Output Low Voltage		0.45		0.25	0.45		0.45	V	V_{CC} = 4.75 V, I_{OL} = 13.3 mA inputs at V_{IH} (see below) V_{CC} = 5.25 V, I_{OL} = 15.2 mA all inputs at V_R = 5.25 V
V_{IH}	Input High Voltage	2		1.9			1.8		V	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		1.2			1.1		0.95	V	Guaranteed input low threshold for all inputs
I_F	Input Load Current		-1.52			-1.52		-1.52	mA	V_{CC} = 5.25V, V_F = 0.45V on other inputs V_R = 4V
I_{SC}	Output Short Circuit Current	-0.65	-1.33	-0.65		-1.33	-0.56	-1.33	mA	V_{CC} = 5.25V one input grounded, output grounded
I_{PD}	Power Dissipation Current (each gate)					4			mA	V_{CC} = 5V inputs open
$t_{pd}+$	Turn-Off Delay			25	45	100			nsec	V_{CC} = 5V see test circuit
$t_{pd}-$	Turn-On Delay			10	30	40			nsec	V_{CC} = 5V see test circuit

NOTE : BAY-74 diode must be connected to each gate when testing this element.

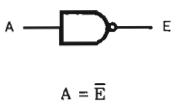
CONNECTION DIAGRAM
(top view)



SCHEMATIC DIAGRAM
(one gate only)



LOGIC FUNCTION

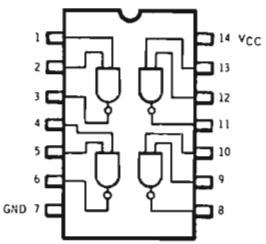


ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V ± 5%)

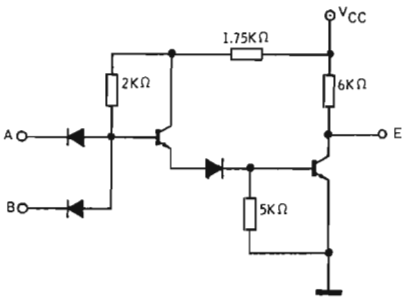
SYMBOL	CHARACTERISTICS	LIMITS 0°C Min.	LIMITS 0°C Max.	LIMITS 25°C Min.	LIMITS 25°C Typ.	LIMITS 25°C Max.	LIMITS 75°C Min.	LIMITS 75°C Max.	UNIT	CONDITIONS AND COMMENTS
V_{OH}	Output High Voltage	2.5		2.6	3.5		2.5		V	V_{CC} = 4.75V, I_{OH} = -0.18 mA one input at V_{IL} (see below)
V_{OL}	Output Low Voltage		0.45		0.25	0.45		0.45	V	V_{CC} = 4.75V, I_{OL} = 13.3 mA inputs at V_{IH} (see below) V_{CC} = 5.25V, I_{OL} = 15.2 mA all inputs at V_R = 5.25 V
V_{IH}	Input High Voltage	2		1.9			1.8		V	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		1.2			1.1		0.95	V	Guaranteed input low threshold for all inputs
I_F	Input Load Current		-1.52		-1.1	-1.52		-1.52	mA	V_{CC} = 5.25 V, V_F = 0.45 V on other inputs V_R = 4 V
I_R	Input Leakage Current		5			5		10	μA	V_{CC} = 5.25 V, V_R = 4 V ground on other inputs
I_{SC}	Output Short Circuit Current	-0.65	-1.33	-0.65		-1.33	-0.56	-1.33	mA	V_{CC} = 5.25V one input grounded, output grounded
I_{PD}	Power Dissipation Current (each gate)				3	4			mA	V_{CC} = 5V inputs open
$t_{pd}+$	Turn-Off Delay			25	45	100			nsec	V_{CC} = 5 V see test circuit
$t_{pd}-$	Turn-On Delay			10	20	40			nsec	V_{CC} = 5 V see test circuit

STANDARD TEMPERATURE RANGE

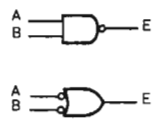
CONNECTION DIAGRAM
(top view)



SCHEMATIC DIAGRAM
(one gate only)



LOGIC FUNCTION



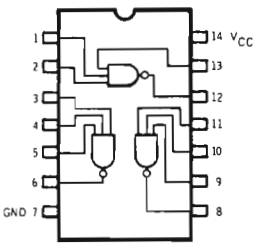
POSITIVE (NAND) LOGIC $E = \overline{A \cdot B}$

NEGATIVE (NOR) LOGIC $E = \overline{A + B}$

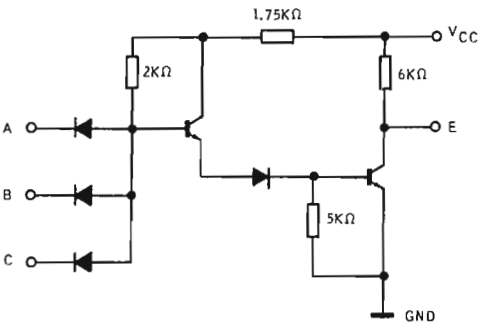
ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V ± 5%)

SYMBOL	CHARACTERISTICS	LIMITS 0°C Min.	0°C Max.	25°C Min.	25°C Typ.	25°C Max.	75°C Min.	75°C Max.	UNIT	CONDITIONS AND COMMENTS
V_{OH}	Output High Voltage	2.5		2.6	3.5		2.5		V	V_{CC} = 4.75V, I_{OH} = -0.18 mA one input at V_{IL} (see below)
V_{OL}	Output Low Voltage		0.45		0.25	0.45		0.45	V	V_{CC} = 4.75V, I_{OL} = 13.3 mA inputs at V_{IH} (aee below) V_{CC} = 5.25V, I_{OL} = 15.2 mA all inputs at V_R = 5.25 V
V_{IH}	Input High Voltage	2		1.9			1.8		V	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		1.2			1.1		0.95	V	Guaranteed input low threshold for all inputs
I_F	Input Load Current		-1.52		-1.1	-1.52		-1.52	mA	V_{CC} = 5.25 V, V_F = 0.45 V on other inputs V_R = 4 V
I_R	Input Leakage Current		5			5		10	μA	V_{CC} = 5.25 V, V_R = 4 V ground on other inputs
I_{SC}	Output Short Circuit Current	-0.65	-1.33	-0.65		-1.33	-0.56	-1.33	mA	V_{CC} = 5.25V one input grounded output grounded
I_{PD}	Power Dissipation Current (each gate)					4			mA	V_{CC} = 5V inputs open
$t_{pd}+$	Turn-Off Delay			25	45	100			nsec	V_{CC} = 5 V see test circuit
$t_{pd}-$	Turn-On Delay			10	20	40			nsec	V_{CC} = 5 V see test circuit

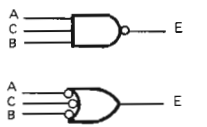
CONNECTION DIAGRAM
(top view)



SCHEMATIC DIAGRAM
(one gate only)



LOGIC FUNCTION



POSITIVE (NAND) LOGIC $E = \overline{A \cdot B \cdot C}$

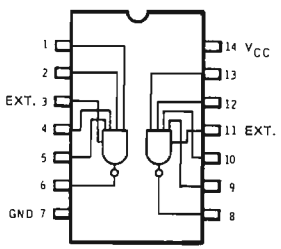
NEGATIVE (NOR) LOGIC $E = \overline{A + B + C}$

ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V ± 5%)

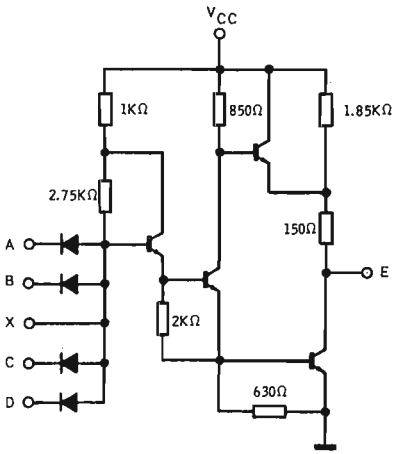
SYMBOL	CHARACTERISTICS	LIMITS 0°C Min.	0°C Max.	25°C Min.	25°C Typ.	25°C Max.	75°C Min.	75°C Max.	UNIT	CONDITIONS AND COMMENTS
V_{OH}	Output High Voltage	2.5		2.6	3.5		2.5		V	V_{CC} = 4.75V, I_{OH} = -0.18 mA one input at V_{IL} (see below)
V_{OL}	Output Low Voltage		0.45		0.25	0.45		0.45	V	V_{CC} = 4.75V, I_{OL} = 13.3 mA inputs at V_{IH} (see below) V_{CC} = 5.25V, I_{OL} = 15.2 mA all inputs at V_R = 5.25 V
V_{IH}	Input High Voltage	2		1.9			1.8		V	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		1.2			1.1		0.95	V	Guaranteed input low threshold for all inputs
I_F	Input Load Current		-1.52		-1.1	-1.52		-1.52	mA	V_{CC} = 5.25 V, V_F = 0.45 V on other inputs V_R = 4 V
I_R	Input Leakage Current		5			5		10	μA	V_{CC} = 5.25 V, V_R = 4 V ground on other inputs
I_{SC}	Output Short Circuit Current	-0.65	-1.33	-0.65		-1.33	-0.56	-1.33	mA	V_{CC} = 5.25V one input grounded, output grounded
I_{PD}	Power Dissipation Current (each gate)					4			mA	V_{CC} = 5V inputs open
$t_{pd}+$	Turn-Off Delay			25	45	100			nsec	V_{CC} = 5 V see test circuit
$t_{pd}-$	Turn-On Delay			10	20	40			nsec	V_{CC} = 5 V see test circuit

STANDARD TEMPERATURE RANGE

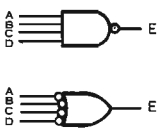
CONNECTION DIAGRAM
(top view)



SCHEMATIC DIAGRAM
(one gate only)



LOGIC FUNCTION



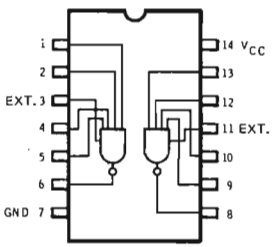
POSITIVE (NAND) LOGIC $E = \overline{A \cdot B \cdot C \cdot D}$

NEGATIVE (NOR) LOGIC $E = \overline{A+B+C+D}$

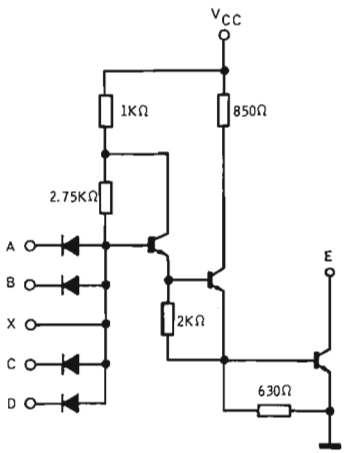
ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V ± 5%)

SYMBOL	CHARACTERISTICS	LIMITS 0°C Min.	0°C Max.	25°C Min.	25°C Typ.	25°C Max.	75°C Min.	75°C Max.	UNIT	CONDITIONS AND COMMENTS
V_{OH}	Output High Voltage	2.5		2.6	2.8		2.5		V	V_{CC} = 4.75V, I_{OH} = -2 mA @ 0°C one input = -2.5mA @ 25°C at V_{IL} = -3 mA @ 75°C (see below)
V_{OL}	Output Low Voltage		0.45			0.45		0.45	V	V_{CC} = 4.75V, I_{OL} = 33.3 mA inputs at V_{IH} (see below) V_{CC} = 5.25V, I_{OL} = 38 mA all inputs at V_R = 5.25 V
V_{IH}	Input High Voltage	2		1.9			1.8		V	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		1.2			1.1		0.95	V	Guaranteed input low threshold for all inputs
I_F	Input Load Current		-1.52		-1.1	-1.52		-1.52	mA	V_{CC} = 5.25 V, V_F = 0.45 V on other inputs V_R = 4 V
I_R	Input Leakage Current		5			5		10	μA	V_{CC} = 5.25 V, V_R = 4 V ground on other inputs
I_{SC}	Output Short Circuit Current	15		16			14		mA	V_{CC} = 5V one input grounded, output grounded
I_{PD}	Power Dissipation Current (each gate)					15			mA	V_{CC} = 5 V inputs open
$t_{pd}+$	Turn-Off Delay			25	50	100			nsec	V_{CC} = 5 V see test circuit
$t_{pd}-$	Turn-On Delay			15	25	50			nsec	V_{CC} = 5 V see test circuit

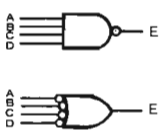
CONNECTION DIAGRAM
(top view)



SCHEMATIC DIAGRAM
(one gate only)



LOGIC FUNCTION



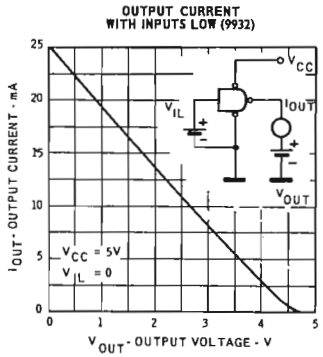
POSITIVE (NAND) LOGIC $E = \overline{A \cdot B \cdot C \cdot D}$

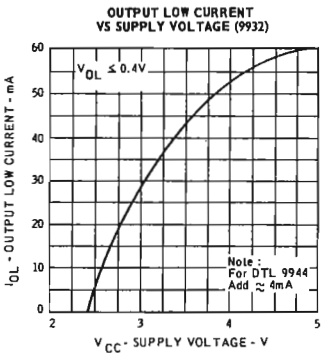
NEGATIVE (NOR) LOGIC $E = \overline{A+B+C+D}$

ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V ± 5%)

SYMBOL	CHARACTERISTICS	LIMITS						UNIT	CONDITIONS AND COMMENTS
		0°C		25°C			75°C		
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
V_{OL}	Output Low Voltage		0.45		0.27	0.45		0.45	V	V_{CC} = 4.75V, I_{OL} = 34 mA inputs at V_{IH} (see below) V_{CC} = 5.25V, I_{OL} = 41 mA all inputs at V_R = 5.25 V
V_{IH}	Input High Voltage	2		1.9			1.8		V	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		1.2			1.1		0.95	V	Guaranteed input low threshold for all inputs
I_F	Input Load Current		-1.52		-1.1	-1.52		-1.52	mA	V_{CC} = 5.25V, V_F = 0.45V on other inputs V_R = 4 V
I_R	Input Leakage Current		5			5		10	μA	V_{CC} = 5.25V, V_R = 4 V ground on other inputs
I_{CEX}	Output Leakage Current		50			100		200	μA	V_{CC} = 4.5V one input grounded, output at V_{CC}
I_{PD}	Power Dissipation Current (each gate)					10			mA	V_{CC} = 5 V inputs open
$t_{pd}+$	Turn-Off Delay			15	35	70			nsec	V_{CC} = 5 V see test circuit
$t_{pd}-$	Turn-On Delay			10	20	45			nsec	V_{CC} = 5 V see test circuit

OUTPUT CHARACTERISTICS (T_A = 25° C unless otherwise noted)

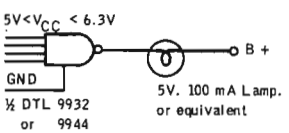




MISCELLANEOUS APPLICATIONS

Lamp Driving

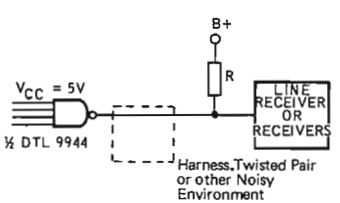
SUGGESTED RATINGS	DIP	FLAT	DIP pl.
Power Dissipation	400 mW	240 mW	300 mW
Max Hot Lamp Current one side only ON	120 mA	100 mA	110 mA
Max Hot Lamp Current both sides ON	90 mA	75 mA	80 mA



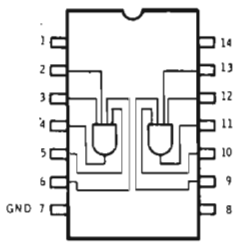
"Cold" lamp current is limited by saturation resistance, emitter resistance, and base current to about 200 to 250 mA. Thermal time constant is measured by forward diode drop in one gate with power pulsed into opposite gate.

Interfacing

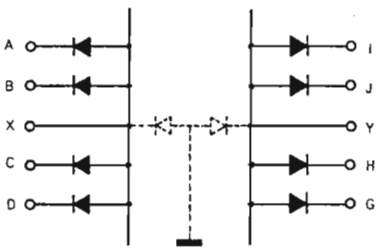
B + up to 12 volts. Line Receiver may have nominal low level of 1 volt; nominal threshold ≈ 4 V and nominal high level 8 V, for example. Resistor selected should be as low as possible consistent with required low input level of receiver, number of receivers, and power dissipation of system. For guaranteed operation in both applications the use of selected units is desirable. Operation as a lamp driver requires high gain units, and for interfacing high voltage units may be required.



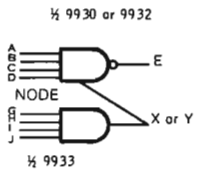
CONNECTION DIAGRAM
(top view)



SCHEMATIC DIAGRAM



LOGIC FUNCTION



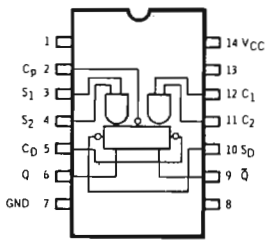
POS.LOGIC $E = \overline{A \cdot B \cdot C \cdot D \cdot G \cdot H \cdot I \cdot J}$

NEG.LOGIC $E = \overline{A+B+C+D+G+H+I+J}$

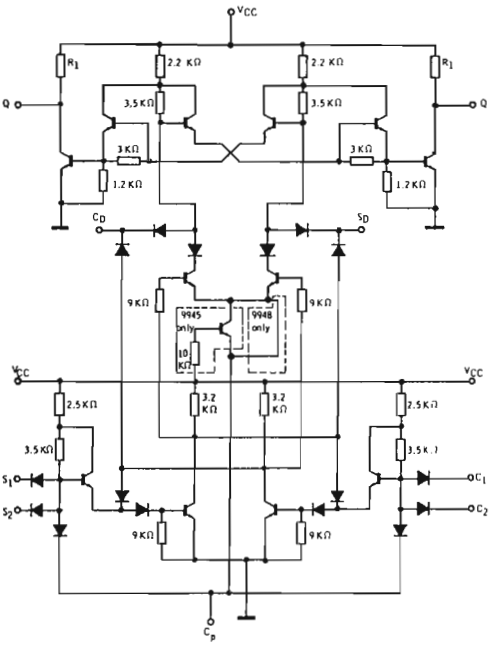
ELECTRICAL CHARACTERISTICS

SYMBOL	CHARACTERISTICS	LIMITS						UNIT	CONDITIONS AND COMMENTS
		0°C		25°C		75°C			
		Min.	Max.	Min.	Max.	Min.	Max.		
V_{FD}	Forward Drop Voltage	0.70	0.90	0.66	0.84	0.56	0.76	V	I_{FD} = 2 mA applied to output, input grounded
I_R	Reverse Current		5		5		10	μA	V_R = 4 V, ground on other inputs
I_R	Output Reverse Current		25		25		50	μA	V_R = 4 V on output

CONNECTION DIAGRAM
(top view)



SCHEMATIC DIAGRAM



NOTE: The DTL 9945 incorporates the standard 6KΩ output pull-up resistor, while the DTL 9948 features a 2KΩ output pull-up resistor for improved switching times, thus reducing however the drive capability.

Note:
DTL 9945 - R_1 = 6kΩ
DTL 9948 - R_1 = 2kΩ

LOGIC FUNCTION

Synchronous Entry Inputs				Output	Asynchronous Entry Inputs		Outputs		J - K Mode Truth Table Inputs		Outputs	
t_n				$t_n + 1$					t_n		$t_n + 1$	
S_1	S_2	C_2	C_1	Q	C_D	S_D	Q	$\overline{Q}$	S_1	C_1	Q	$\overline{Q}$
L	X	L	X	NC	H	H	NC	NC	L	H	L	H
L	X	X	L	NC	H	L	H	L	H	L	H	L
X	L	L	X	NC	L	H	L	H	H	H	$\overline{Q}_n$	Q_n
X	L	X	L	NC	L	L	H	H	L	L	Q_n	$\overline{Q}_n$
L	X	H	H	L								
X	L	H	H	L					For J - K Mode Operation: Connected 4 to 9 and 11 to 6.			
H	H	L	X	H								
H	H	X	L	H								
H	H	H	H	Undetermined								

NOTES:

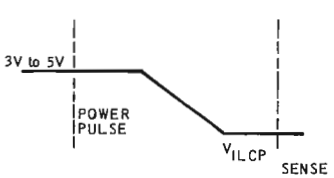
1) Abbreviation used in the body of tables:
L = low, the more negative voltage level.
H = high, the more positive voltage level (in all cases, unused pins have the same effect as high).
X = immaterial, either H or L has equal effect.
NC = no change, the clock pulse has no effect on outputs.
Q_n = outputs state at time t_n

2) The L symbol in the S and C input column is defined as meaning that the input does not go high at any time while the clock is high. The H symbol in the S and C input column is defined as meaning that the input is high at the same time as the clock is high.

9945 ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V ± 5%)

SYMBOL	CHARACTERISTICS	LIMITS						UNIT	CONDITIONS AND COMMENTS
		0°C		25°C			75°C		
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
V_{OH}	Output High Voltage	2.5		2.6	3.3		2.5		V	V_{CC} = 4.75V, I_{OH} = −0.18 mA V_{IL} (see below) on proper asynchronous input
V_{OL}	Output Low Voltage		0.45		0.25	0.45		0.45	V	V_{CC} = 4.75V, I_{OL} = 16 mA V_{CC} = 5.25V, I_{OL} = 16 mA V_{IH} (see below) on proper asynchronous input
V_{IH}	Input High Voltage	2		1.9			1.8		V	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		1.2			1.1		0.95	V	Guaranteed input low threshold for all inputs
I_F	S & C Inputs Load Current		-1			-1		-0.95	mA	V_{CC} = 5.25V, V_F = 0.45V V_R = 4 V on other inputs
I_{FS}	S_D, C_D Inputs Load Current		-2.96			-2.96		-2.85	mA	V_{CC} = 5.25V, V_F = 0.45V V_R = 4 V on other inputs
I_{FCP}	Clock Input Load Current		-2.96			-2.96		-2.85	mA	V_{CC} = 5.25V, V_F = 0.45V V_{IL} on S_D
I_R	S, C, S_D, C_D Inputs Leakage Current		5			5		10	μA	V_{CC} = 5.25V, V_R = 4 V ground on other inputs
I_{RCP}	Clock Input Leakage Current		20			20		30	μA	V_{CC} = 4 V, V_R = 4 V S and C_D inputs grounded
I_{PD}	Power Dissipation Current					15			mA	V_{CC} = 5 V
I_{SC}	Output Short Circuit Current	-0.65	-1.33	-0.65		-1.33	-0.56	-1.33	mA	V_{CC} = 5.25V high output grounded
$t_{pd}+$	Turn-Off Delay				30	90			nsec	V_{CC} = 5 V see test circuit
$t_{pd}-$	Turn-On Delay				30	90			nsec	V_{CC} = 5 V see test circuit

CLOCK PULSE DESCRIPTION



V_{ILCP} = 1V @ 25°C

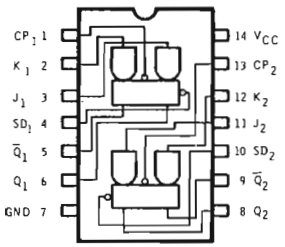
9948 ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V ± 5%)

SYMBOL	CHARACTERISTICS	LIMITS						UNIT	CONDITIONS AND COMMENTS
		0°C		25°C			75°C		
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
V_{OH}	Output High Voltage	2.5		2.6	3.3		2.5		V	V_{CC} = 4.75V, I_{OH} = −0.54 mA V_{IL} (see below) on proper asynchronous input
V_{OL}	Output Low Voltage		0.45		0.25	0.45		0.45	V	V_{CC} = 4.75V, I_{OL} = 14.6 mA V_{CC} = 5.25V, I_{OL} = 14.6 mA V_{IH} (see below) on proper asynchronous input
V_{IH}	Input High Voltage	2		1.9			1.8		V	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		1.2			1.1		0.95	V	Guaranteed input low threshold for all inputs
I_F	S & C Inputs Load Current		-1			-1		-0.95	mA	V_{CC} = 5.25V, V_F = 0.45V on other inputs V_R = 4 V
I_{FS}	C_D, S_D Inputs Load Current		-2.96			-2.96		-2.85	mA	V_{CC} = 5.25V, V_F = 0.45V
I_{FCP}	Clock Input Load Current		-2.38			-2.38		-2.26	mA	V_{CC} = 5.25V, V_F = 0.45V V_{IL} on S_D
I_R	S, C, S_D, C_D Inputs Leakage Current		5			5		10	μA	V_{CC} = 5.25V, V_R = 4 V ground on other inputs
I_{RCP}	Clock Input Leakage Current		20			20		30	μA	V_{CC} = 4 V, V_R = 4 V S and C_D inputs grounded
I_{PD}	Power Dissipation Current					17.5			mA	V_{CC} = 5 V
I_{SC}	Output Short Circuit Current	-1.86	-4.41	-1.86		-4.41	-1.68	-4.20	mA	V_{CC} = 5.25V high output grounded
t_{pd+}	Turn-Off Delay			30		80			nsec	V_{CC} = 5 V see test circuit
t_{pd-}	Turn-On Delay			30		80			nsec	V_{CC} = 5 V see test circuit

CLOCK PULSE DESCRIPTION : SEE 9945

NOTE: The DTL 9093 and 9094 are respectively dual DTL 9945 and 9948 flip-flops.

CONNECTION DIAGRAM
(top view)



LOGIC FUNCTION

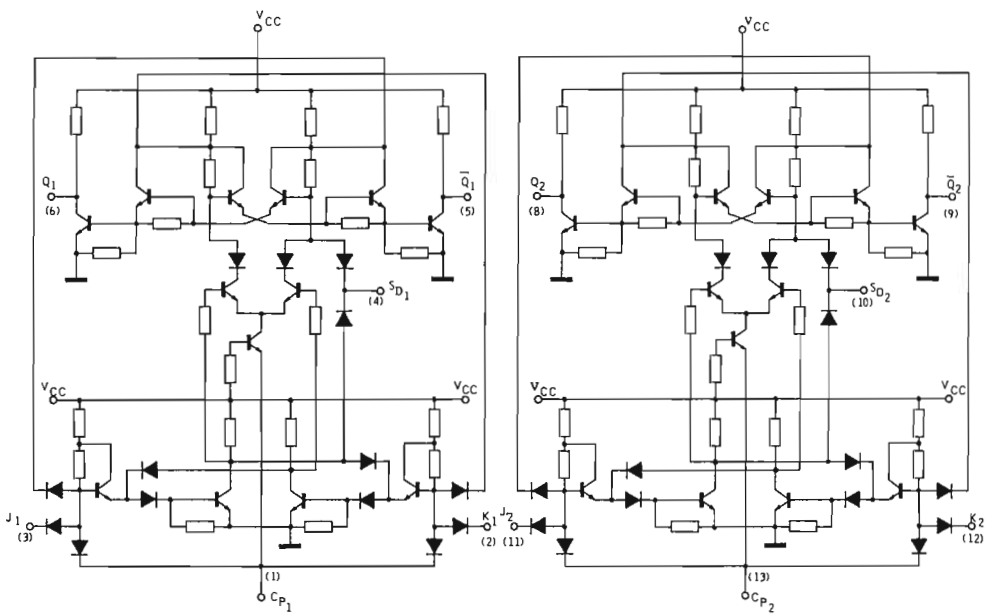
Asynchronous Entry			J-K Mode Truth Table			
Input	Outputs		Inputs		Outputs	
			t_n		$t_n + 1$	
4 (10)	6 (8)	5 (9)	3 (11)	2 (12)	6 (8)	5 (9)
H	NC	NC	L	H	L	H
L	H	L	H	L	H	L
			H	H	$\bar{Q}_n$	Q_n
			L	L	Q_n	$\bar{Q}_n$

NOTES:

1) Abbreviations used in the body of tables:
   L = low, the more negative voltage level
   H = high, the more positive voltage level
   (in all cases, unused pins have the same effect as high).
   NC = no change, the clock pulse has no effect on outputs.
   Q_n = outputs state at time tn

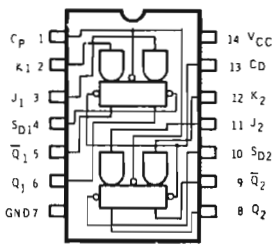
2) The L symbol in the J and K input column is defined as meaning that the input does not go high at any time while the clock is high.
   The H symbol in the J and K input column is defined as meaning that the input is high at the same time as the clock is high.

SCHEMATIC DIAGRAM 9093/9094 (9093 SHOWN)



NOTE: The DTL 9097 and 9099 are respectively dual DTL 9948 and 9945 flip-flops.

CONNECTION DIAGRAM
(top view)



LOGIC FUNCTION

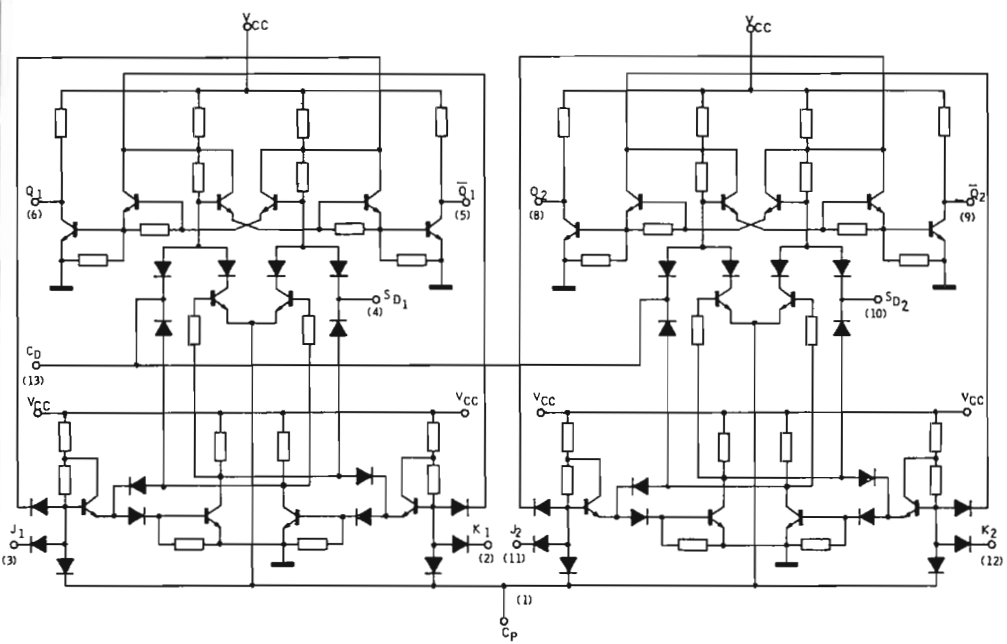
Asynchronous Entry				J-K Mode Truth Table			
Inputs		Outputs		Inputs		Outputs	
13	4 (10)	6 (8)	5 (9)	t_n 3 (11)	2 (12)	t_n+1 6 (8)	5 (9)
H	H	NC	NC	L	H	L	H
H	L	H	L	H	L	H	L
L	H	L	H	H	H	$\overline{Q}_n$	Q_n
L	L	H	H	L	L	Q_n	$\overline{Q}_n$

NOTES:

1) Abbreviations used in the body of tables:
   L = low, the more negative voltage level
   H = high, the more positive voltage level
   (in all cases, unused pins have the same effect as high).
   NC = no change, the clock pulse has no effect on outputs.
   Q_n = outputs state at time t_n.

2) The L symbol in the J and K input column is defined as meaning that the input does not go high at any time while the clock is high.
   The H symbol in the J and K input column is defined as meaning that the input is high at the same time as the clock is high.

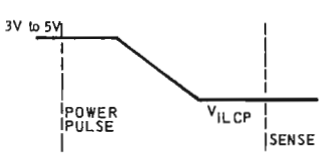
SCHEMATIC DIAGRAM 9097/9099 (9097 SHOWN)



ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V ± 5%)

SYMBOL	CHARACTERISTICS	LIMITS						UNIT	CONDITIONS AND COMMENTS
		0°C		25°C		75°C			
		Min.	Max.	Min.	Max.	Min.	Max.		
V_{OH}	Output High Voltage	2.5		2.6		2.5		V	V_{CC} = 4.75V, I_{OH} = -0.18 mA V_{IL} (see below) and V_R = 4 V on asynchronous inputs
V_{OL}	Output Low Voltage		0.45		0.45		0.45	V	V_{CC} = 4.75V, I_{OL} = 16 mA V_{CC} = 5.25V, I_{OL} = 16 mA ground and V_R = 4 V on asynchronous inputs
V_{IL}	Input Low Voltage		1.2		1.1		0.95	V	Guaranteed input low threshold for all inputs
V_{IH}	Input High Voltage	2		1.9		1.8		V	Guaranteed input high threshold for all inputs
I_F	Input Load Current J and K Inputs		-1		-1		-0.95	mA	V_{CC} = 5.25V, V_F = 0.45V
I_{FCP}	Clock Input Load Current 9093 9099		 -2.98 -5.96		 -2.98 -5.96		 -2.86 -5.72	mA	V_{CC} = 5.25V, V_F = 0.45V V_{IL} (see above) on asynchronous input
I_{FS}	Set Input Load Current		-2.23		-2.23		-2.15	mA	V_{CC} = 5.25V, V_F = 0.45V ground on J inputs
I_{FC}	Clear Input Load Current		-4.40		-4.40		-4.28	mA	V_{CC} = 5.25V, V_{CC} = 0.45V ground on K inputs
I_R	Input Leakage Current J and K Inputs		5		5		10	μA	V_{CC} = 5.25V, V_R = 4 V ground on clock
I_{RS}	Set Input Leakage Current		5		5		10	μA	V_{CC} = 5.25V, V_R = 4 V ground on K inputs
I_{RC}	Clear Input Leakage Current		10		10		20	μA	V_{CC} = 5.25V, V_R = 4 V ground on J inputs
I_{RCP}	Clock Input Leakage Current 9093 9099		 20 40		 20 40		 30 60	μA	V_{CC} = 4 V, V_R = 4 V ground on J inputs
I_{SC}	Output Short Circuit Current	-0.65	-1.33	-0.65	-1.33	-0.56	-1.33	mA	V_{CC} = 5.25V high output grounded
IPD	Power Dissipation Current 9093 9099				 30 28			mA	V_{CC} = 5 V
$t_{pd}+$	Turn-Off Delay			30	90			nsec	V_{CC} = 5 V see test circuit
$t_{pd}-$	Turn-On Delay			30	90			nsec	V_{CC} = 5 V see test circuit

CLOCK PULSE DESCRIPTION:



V_{ILCP} = 1V @ 25° C

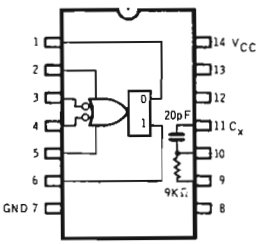
STANDARD TEMPERATURE RANGE

ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V ± 5%)

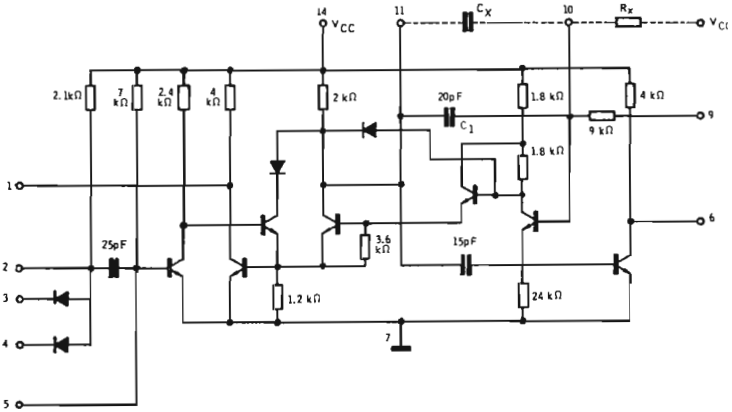
SYMBOL	CHARACTERISTICS	LIMITS 0°C Min.	0°C Max.	25°C Min.	25°C Max.	75°C Min.	75°C Max.	UNIT	CONDITIONS AND COMMENTS
V_{OH}	Output High Voltage	2.5		2.6		2.5		V	V_{CC} = 4.75V, I_{OH} = 0.54 mA V_{IL} (see below) and V_R = 4 V on asynchronous inputs
V_{OL}	Output Low Voltage		0.45		0.45		0.45	V	V_{CC} = 5.25V, I_{OL} = 14.6 mA V_{CC} = 4.75V, I_{OL} = 14.6 mA ground and V_R = 4 V on asynchronous inputs
V_{IH}	Input High Voltage	2		1.9		1.8		V	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		1.2		1.1		0.95	V	Guaranteed input low threshold for all inputs
I_F	Input Load Current J and K Inputs		-1		-1		-0.95	mA	V_{CC} = 5.25V, V_F = 0.45V
I_{FCP}	Clock Input Load Current 9094 9097		-2.38 -4.76		-2.38 -4.76		-2.20 -4.76	mA	V_{CC} = 5.25V, V_F = 0.45V V_{IL} (see above) on asynchronous input
I_{FS}	Set Input Load Current		-2.23		-2.23		-2.15	mA	V_{CC} = 5.25V, V_F = 0.45V ground on J inputs
I_{FC}	Clear Input Load Current		-4.40		-4.40		-4.28	mA	V_{CC} = 5.25V, V_F = 0.45V ground on K inputs
I_R	Input Leakage Current J and K inputs		5		5		10	μA	V_{CC} = 5.25V, V_R = 4 V ground on clock
I_{RCP}	Clock Input Leakage Current 9094 9097		20 40		20 40		30 60	μA	V_{CC} = 4 V, V_R = 4 V ground on J inputs
I_{RS}	Set Input Leakage Current		5		5		10	μA	V_{CC} = 5.25V, V_R = 4 V ground on K inputs
I_{RC}	Clear Input Leakage Current		10		10		20	μA	V_{CC} = 5.25V, V_R = 4 V ground on J inputs
I_{SC}	Output Short Circuit Current	-1.86	-4.41	-1.86	-4.41	-1.68	-4.20	mA	V_{CC} = 5.25V high output grounded
I_{PD}	Power Dissipation Current 9094 9097				35 32.4			mA	V_{CC} = 5 V
$t_{pd}+$	Turn-Off Delay			30	80			nsec	V_{CC} = 5 V see test circuit
$t_{pd}-$	Turn-On Delay			30	80			nsec	V_{CC} = 5 V see test circuit

CLOCK PULSE DESCRIPTION : SEE 9093 - 9099

CONNECTION DIAGRAM
(top view)



SCHEMATIC DIAGRAM



ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V)

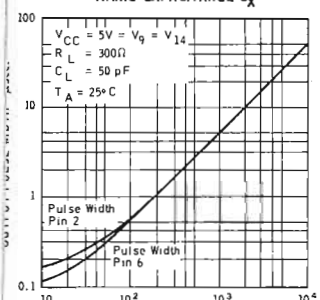
SYMBOL	CHARACTERISTICS	LIMITS 0°C Min.	0°C Max.	25°C Min.	25°C Max.	75°C Min.	75°C Max.	UNIT	CONDITIONS AND COMMENTS
V_{OH}	Output High Voltage	3.2		3.2		3.2		V	V_{CC} = 5V, I_{OH} = 0.15 mA Pin 2 grounded, Pin 9 at V_{CC}
V_{OL}	Output Low Voltage		0.45		0.45		0.5	V	V_{CC} = 5V, I_{OL}=14.8 mA @ 0°C and 25°C I_{OL}=14 mA @ 75°C when testing Pin 1, ground Pin 10 when testing Pin 6, V_{CC} on Pin 9
I_F	Input Load Current	-2.8		-2.8		-2.66		mA	V_{CC} = 5V, V_F = V_{OL} V_R = 4 V (see above)
I_R	Input Leakage Current		5		5		10	μA	V_{CC} = 5V, V_R = 4 V ground on Pin 2
I_{PD}	Power Dissipation Current				10.8			mA	V_{CC} = 5 V inputs grounded, V_{CC} on Pin 9
$t_{pd}+$	Turn-Off Delay (Pin 6)				40			nsec	V_{CC} = 5 V see test circuit
$t_{pd}-$	Turn-On Delay (Pin 1)				40			nsec	V_{CC} = 5 V see test circuit
P_W	Pulse Width (Pin 1)			90	330			nsec	V_{CC} = 5 V see test circuit
P_W	Pulse Width (Pin 6)			70	270			nsec	V_{CC} = 5 V see test circuit

RULES FOR USE OF DTL 9951

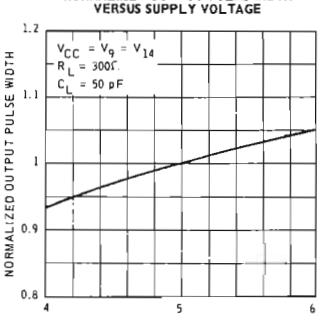
1) With Pin 9 connected to V_{CC} and no external capacitor (C_x), the output pulse width is approximately 100 nsec.
2) With Pin 9 connected to V_{CC} and an external capacitor (C_x) connected between Pins 10 and 11, the output pulse width (T) is: $T \sim 6.4 (C_x + 20)$ with C_x in pF and T in nsec.
3) For improved pulse width control, Pin 9 is left open and a stable external resistor (R_x) of 9 kΩ minimum to 15 kΩ maximum is connected from Pin 10 to V_{CC}. The output pulse width is given by the expression: $T \sim 0.64 R_x (C_x + 20)$ with R_x in kΩ, C_x in pF and T in nsec.
4) The output duty cycle (pulse width/period) should not exceed 40%. It may be increased to 50% by adding a 2kΩ resistor between Pin 11 and V_{CC}. Higher duty cycles are obtainable but the output pulse width and performance are less predictable.
5) The maximum input fall time to trigger: 15 nsec for a 1 V swing; 40 nsec for a 2 V swing; 80 nsec for a 4 V swing.
6) The AC sensitivity of the inputs may be decreased by connecting a capacitor between Pin 5 and ground.
7) The minimum pulse width at output Pin 1 is approximately 100 nsec. This pulse width may be decreased to 50 nsec by connecting a 10 kΩ resistor between Pin 5 and V_{CC}.

TIMING CHARACTERISTICS

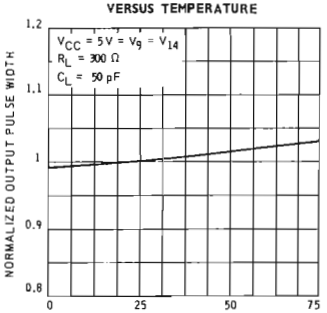
OUTPUT PULSE WIDTH VERSUS EXTERNAL TIMING CAPACITANCE C_X



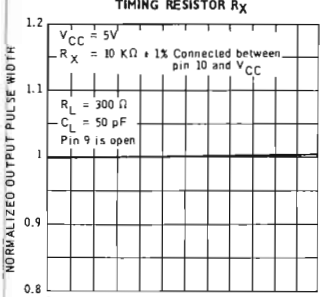
NORMALIZED OUTPUT PULSE WIDTH VERSUS SUPPLY VOLTAGE



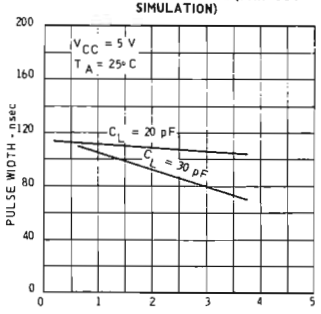
NORMALIZED OUTPUT PULSE WIDTH VERSUS TEMPERATURE



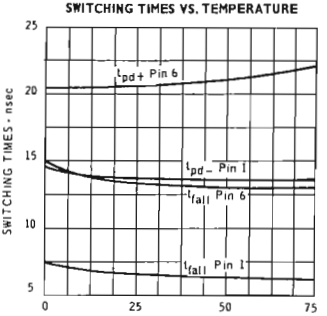
NORMALIZED OUTPUT PULSE WIDTH VS. TEMPERATURE USING EXTERNAL TIMING RESISTOR R_X



PIN 6 OUTPUT PULSE WIDTH VERSUS LOAD RESISTANCE (FAN-OUT SIMULATION)

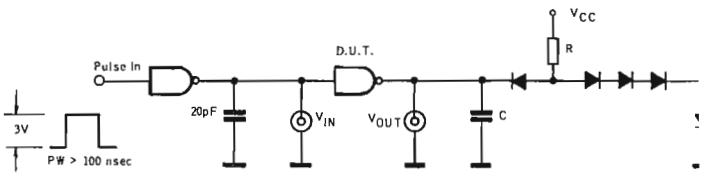


SWITCHING TIMES VS. TEMPERATURE



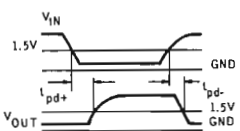
SWITCHING TIME TEST CIRCUITS

9930 - 9934 - 9936 - 9946 - 9962 GATES t_{pd} TEST CIRCUIT



Diodes are BAY 74

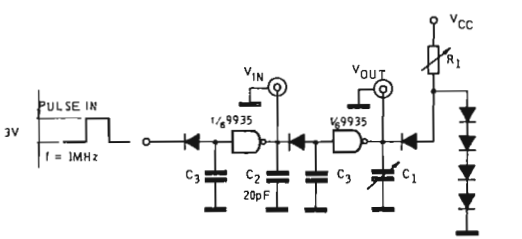
WAVEFORMS



TEST CONDITIONS

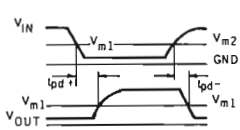
	R	C
t_{pd} +	3.9 kΩ	30 pF
t_{pd} -	400 Ω	50 pF

9935 GATE t_{pd} TEST CIRCUIT



Diodes are BAY 74

WAVEFORMS



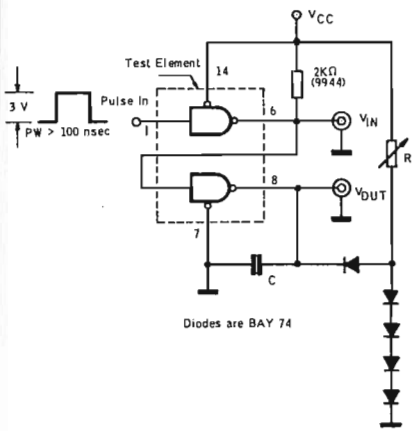
V_{m1}	V_{m2}
1.5 V	1.3V

TEST CONDITIONS

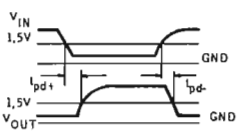
	R_1	C_1	C_2	C_3
t_{pd} +	3.9 kΩ	30 pF	20 pF	5 pF
t_{pd} -	400 Ω	50 pF	20 pF	5 pF

SWITCHING TIME TEST CIRCUITS

9932 - 9944 GATES t_{pd} TEST CIRCUIT



WAVEFORMS

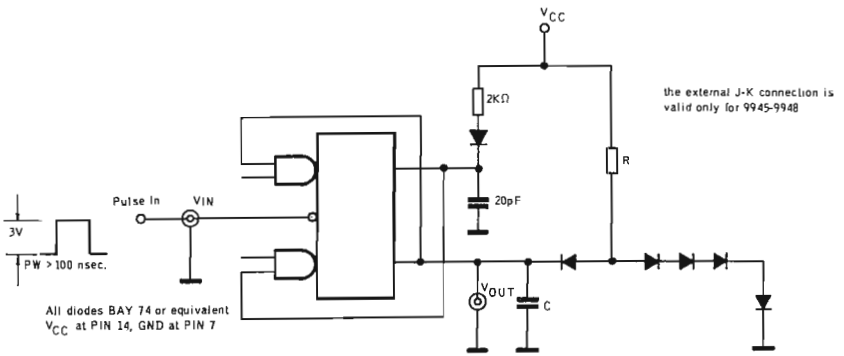


TEST CONDITIONS

	R	C
9944 t_{pd} +	510Ω	20 pF
9944 t_{pd} -	150Ω	100 pF
9932 t_{pd} +	510Ω	500 pF
9932 t_{pd} -	150Ω	500 pF

SWITCHING TIME TEST CIRCUITS

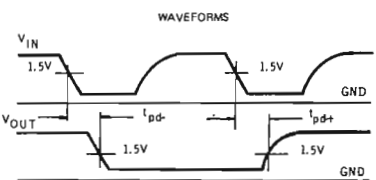
9945 - 9948 - 9093 - 9094 - 9097 - 9099 FLIP-FLOPS t_{pd} TEST CIRCUIT



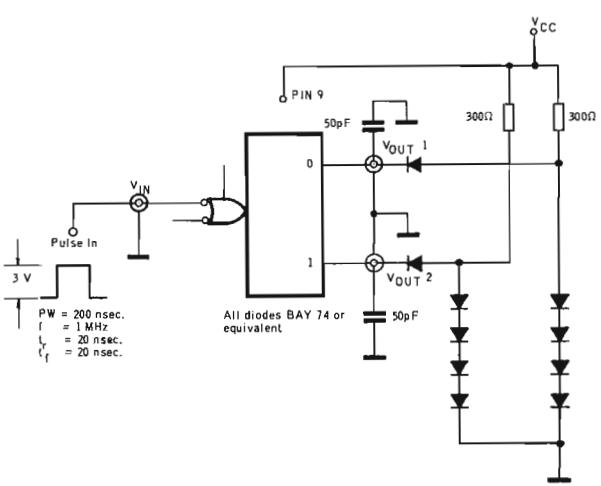
TEST CONDITIONS

	R	C
$t_{pd}+$	2KΩ	30 pF
$t_{pd}-$	330Ω	50 pF

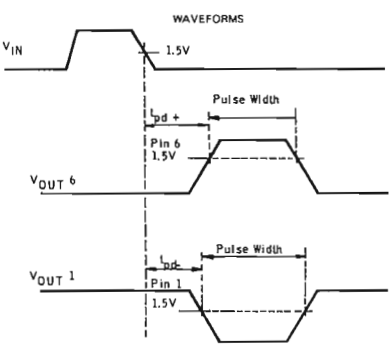
WAVEFORMS



9951 MONOSTABLE t_{pd} TEST CIRCUIT



WAVEFORMS



LPDTL INTEGRATED CIRCUITS

LPDTL INTEGRATED CIRCUITS

LPDTL E 300 SERIES

GATES	Page E.	S.
E 301	196	208
E 302	197	209
E 303	198	210
E 304	199	211
E 305	200	212
E 306	201	213

FLIP-FLOPS	Page E.	S.
E 300	202	214

E. = Extended temperature range
S. = Standard temperature range

low - power diode - transistor logic family

EXTENDED TEMPERATURE RANGE, - 55°C ÷ 125°C

- Compatible with DTL and TTL products
- Power dissipation 1 mW per gate
- Noise immunity 1V
- Worst case noise immunity 450 mV
- Output drive capability of 10
- Fan-in expansion capability
- Wired-OR capability
- Same pin configuration as the corresponding DTL and TTL products

ORDERING NUMBERS

E 3XXD2 (for Dual in-Line package, 3XX is type number)
E3XXF2 (for flat package, 3XX is type number)

The SGS LPDTL Integrated Circuit Family consists of a set of compatible, integrated logic circuits specifically designed for low power, medium speed applications.
The circuits are fabricated within a silicon monolithic substrate using the standard Planar epitaxial process.
LPDTL elements are available in two hermetically sealed ceramic packages : the Dual In-Line Package (D) designed for low cost insertion, and the 14 lead flat package (F) for maximum density.

ABSOLUTE MAXIMUM RATINGS

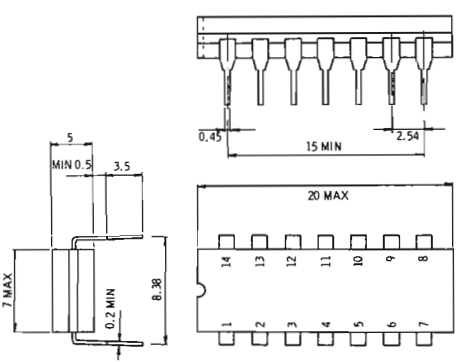
(above which the useful life may be impaired)

Supply Voltage (V_{CC}), continuous	8 V
Supply Voltage (V_{CC}), pulsed, 1 sec.	12 V
Storage Temperature Range	- 65°C to 150°C
Temperature (Ambient) under bias	- 55°C to 125°C

OPERATING CONDITIONS

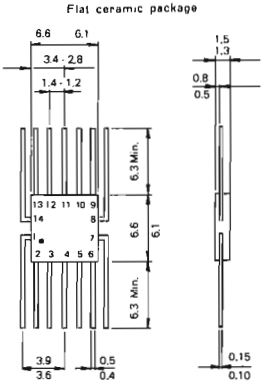
Temperature range	55°C to 125°C
Supply voltage (V_{CC})	5 V ± 10 %

PHYSICAL DIMENSIONS
14-pin ceramic DIP



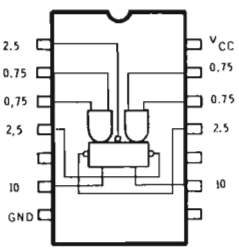
Note : all dimensions in mm.

PHYSICAL DIMENSIONS
Flat ceramic package

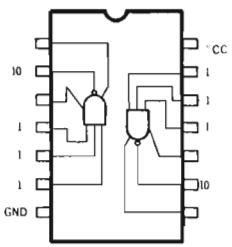


NOTE - All dimensions in mm.

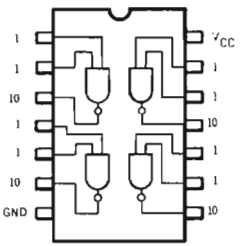
INPUT-OUTPUT LOAD/DRIVE FACTORS



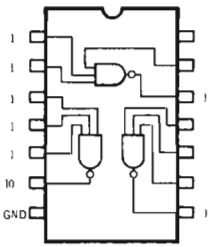
E 300



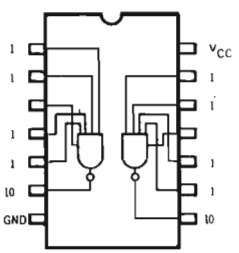
* E 301



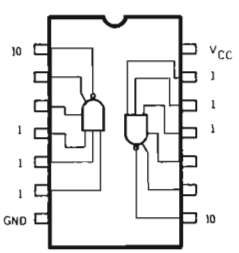
E 302



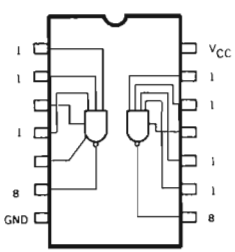
E 303



E 304



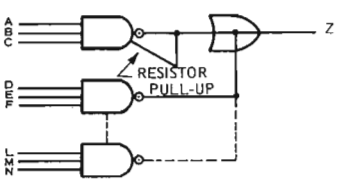
E 305



* E 306

* NOTE
Wired-OR operation is allowe
only with E301 and E306.

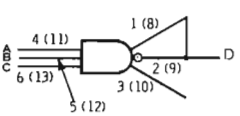
WIRED "OR" APPLICATIONS



$\overline{A\,B\,C + D\,E\,F + \ldots\ldots\ldots L\,M\,N} = Z$

Output drive factor = (10 - 3 n) unit load
(n = No. of resistor pull-ups)

One pull-up resistor is required for every 13 gates connected to the common "OR" node.



E 301

$\overline{A\,B\,C} = D$

Output drive factor = 10 unit load
= 7 U.L. with resistor pull
up connected

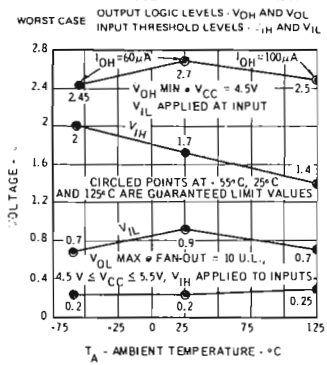
Either the emitter follower or resistor pull-up mu
be connected to the output to establish the high
vel.

NOTE (Buffer Element)

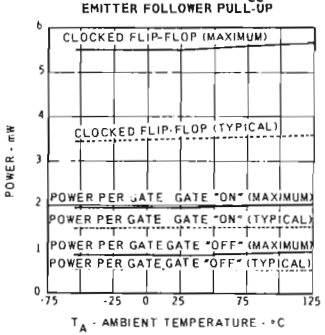
For applications requiring a fan-out exceeding 10, the SGS DTL 9930 Dual 4 - Input Gate may be used. The DTL 9930 will drive 18 LPDTL un
loads, while maintaining the same output logic levels as the LPDTL circuits.
The input of a DTL 9930 requires the equivalent of 10 LPDTL unit loads. Therefore, a low power circuit can drive only one DTL 9930 input.

LECTRICAL CHARACTERISTICS

OPERATING VOLTAGE CHARACTERISTICS

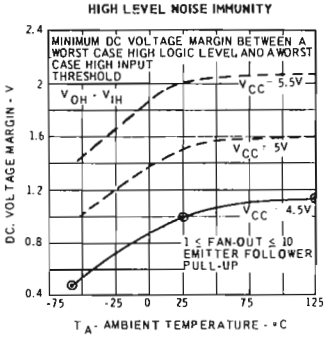


POWER CHARACTERISTICS V_{CC} 5 V
EMITTER FOLLOWER PULL-UP

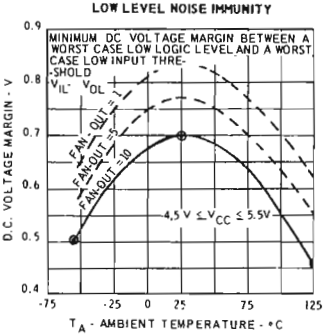


OISE IMMUNITY

HIGH LEVEL NOISE IMMUNITY

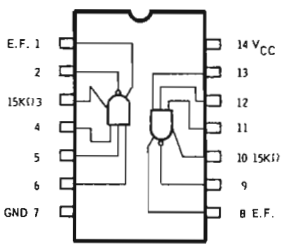


LOW LEVEL NOISE IMMUNITY

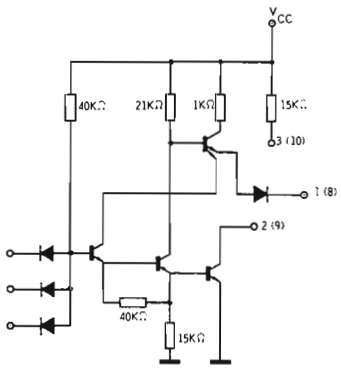


This element consists of two, 3 - input positive logic NAND gates suitable for general logic gate and inverter applications. The peculiar feature of this gate is that the output transistor collector and the amitter follower pull-up ara not internally connected. This allows the user to tie collectors to a common node for the wired "OR" logic function.

CONNECTION DIAGRAM
(top view)



SCHEMATIC DIAGRAM
(one gate only)



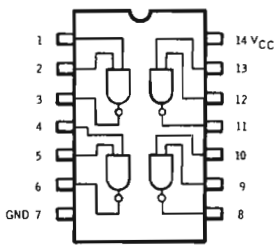
ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10 %)

SYMBOL	CHARACTERISTICS	LIMITS						UNIT	CONDITIONS AND COMMENTS
		-55°C		25°C			125°C		
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
V_{OH}	Output High Voltage	2.45		2.70			2.50		V	V_{CC} = 4.5 V I_{OH} = -60 µA @ -55°C = -60 µA @ 25°C = -100 µA @ 125°C One input at V_{IL} (see below)
V_{OL}	Output Low Voltage		0.2			0.2		0.25	V	V_{CC} = 5.5 V I_{OL} = 1.58 mA @ -55°C = 1.60 mA @ 25°C = 1.46 mA @ 125°C Inputs at V_{IH} (see below)
V_{IL}	Input Low Voltage		0.7			0.9		0.7	V	Guaranteed input low threshold for all inputs
V_{IH}	Input High Voltage	2		1.7			1.4		V	Guaranteed input high threshold for all inputs
I_F	Input Load Current		-158			-160		-146	µA	V_{CC} = 5.5 V $V_F = V_{OL}$ (see above) on other inputs V_R = 5.5 V
I_R	Input Leakage Current		1			1		10	µA	V_{CC} = 4.5 V V_R = 4.5 V Ground on other inputs
I_{SC}	Output Short Circuit Current	-1	-6.5	-2.8		-6.5	-2	-6.5	mA	V_{CC} = 5.5 V Inputs and output V_{CC} = 4.5 V grounded
I_{PD}	Power Dissipation Current (each gate)		390 165			390 165		410 175	µA	V_{CC} = 5 V Inputs open V_{CC} = 5 V Inputs grounded
t_{pd+}	Turn-off delay					150			nsec	V_{CC} = 5 V See test circuit
t_{pd-}	Turn-on delay					150			nsec	

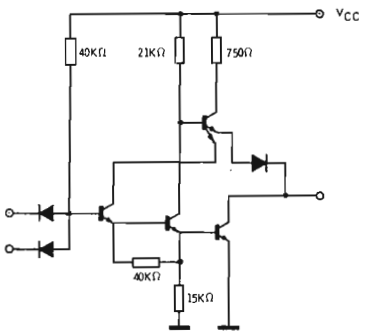
Note : Pin 1 and Pin 2 (8 and 9) must be tied together when testing this element

This element consists of four, 2 - input NAND gates with active pull-up. Its logic function and pin configuration are identical to the DTL 9946, and TTL T102 gate elements. This element is suitable for general logic, latches and inverter applications where minimum power consumption is important.

CONNECTION DIAGRAM
(top view)



SCHEMATIC DIAGRAM
(one gate only)

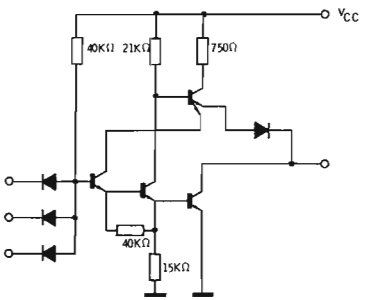


ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%)

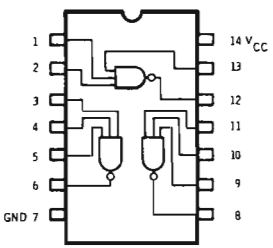
SYMBOL	CHARACTERISTICS	LIMITS						UNIT	CONDITIONS AND COMMENTS
		-55°C		25°C		125°C			
		Min.	Max.	Min.	Typ. Max.	Min.	Max.		
V_{OH}	Output High Voltege	2.45		2.70		2.50		V	V_{CC} = 4.5 V I_{OH} = -60 µA @ - 55°C = -60 µA @ 25°C = -100 µA @ 125°C One input at V_{IL} (see below)
V_{OL}	Output Low Voltage		0.2		0.2		0,25	V	V_{CC} = 5.5 V I_{OL} = 1.58 mA @ - 55°C = 1.60 mA @ 25°C = 1.46 mA @ 125°C Inputs at V_{IH} (see below)
V_{IL}	Input Low Voltage		0.7		0.9		0,7	V	Guaranteed input low threshold for all inputs
V_{IH}	Input High Voltage	2		1.7		1,4		V	Guaranteed input high threshold for all inputs
I_F	Input Load Current		- 158		-160		-146	µA	V_{CC} = 5.5 V V_F = V_{OL} (see above) on other inputs V_R = 5.5 V
I_R	Input Leakage Current		1		1		10	µA	V_{CC} = 4.5 V V_R = 4.5 V Ground on other inputs
I_{SC}	Output Short Circuit Current	-1	-8.5	-2.8	-8.5	-2	-8.5	mA	V_{CC} = 5.5 V Inputs and output V_{CC} = 4.5 V grounded
I_{PD}	Power Dissipation Current (each gate)		390 165		390 165		410 175	µA	V_{CC} = 5 V Inputs at V_{IH} (see above) V_{CC} = 5 V Inputs grounded
t_{pd+}	Turn-off delay				90			nsec	V_{CC} = 5 V See test circuit
t_{pd-}	Turn-on delay				60			nsec	

This element consists of three, 3 - input NAND gate with active pull-up. Its logic function and pin configuration are identical to the DTL 9962 and TTL T103 gate elements.

SCHEMATIC DIAGRAM
(one gate only)



CONNECTION DIAGRAM
(top view)



ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V \pm 10\%$)

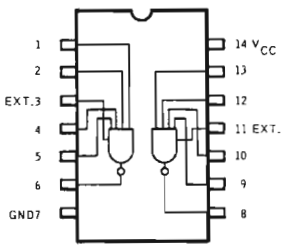
SYMBOL	CHARACTERISTICS	LIMITS						UNIT	CONDITIONS AND COMMENTS
		-55°C		25°C		125°C			
		Min.	Max.	Min.	Typ. Max.	Min.	Max.		
V_{OH}	Output High Voltage	2.45		2.70		2.50		V	$V_{CC} = 4.5$ V $I_{OH} = -60\,\mu A$ @ -55°C $= -60\,\mu A$ @ 25°C $= -100\,\mu A$ @ 125°C One input at V_{IL} (see below)
V_{OL}	Output Low Voltage		0.2		0.2		0.25	V	$V_{CC} = 5.5$ V $I_{OL} = 1.58$ mA @ -55°C $= 1.60$ mA @ 25°C $= 1.46$ mA @ 125°C Inputs at V_{IH} (see below)
V_{IL}	Input Low Voltage		0.7		0.9		0.7	V	Guaranteed input low threshold for all inputs
V_{IH}	Input High Voltage	2		1.7		1.4		V	Guaranteed input high threshold for all inputs
I_F	Input Load Current		-158		-160		-146	μA	$V_{CC} = 5.5$ V $V_F = V_{OL}$ (see above) on other inputs $V_R = 5.5$ V
I_R	Input Leakage Current		1		1		10	μA	$V_{CC} = 4.5$ V $V_R = 4.5$ V Ground on other inputs
I_{SC}	Output Short Circuit Current	-1	-8.5	-2.8	-8.5	-2	-8.5	mA	$V_{CC} = 5.5$ V Inputs and output $V_{CC} = 4.5$ V grounded
I_{PD}	Power Dissipation Current (each gate)		390 165		390 165		410 175	μA	$V_{CC} = 5$ V Inputs open $V_{CC} = 5$ V Inputs grounded
t_{pd+}	Turn-off delay				100			nsec	$V_{CC} = 5$ V See test circuit
t_{pd-}	Turn-on delay				60			nsec	

Dual 4-Input Nand Gate With Extender E 304

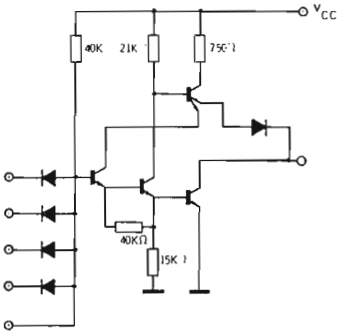
EXTENDED TEMPERATURE RANGE

This element consists of two 4-input NAND gates with extender input and active pull-up. Its logic function and pin configuration are identical to the DTL 9930 gate and the TTL T104 gate. It combines the advantages of the active pull-ups with the advantages offered by the extender inputs (see note).

CONNECTION DIAGRAM
(top view)



SCHEMATIC DIAGRAM
(one gate only)

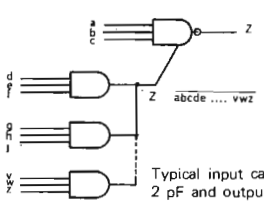


ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V ± 10%)

SYMBOL	CHARACTERISTICS	LIMITS						UNIT	CONDITIONS AND COMMENTS
		-55°C		25°C		125°C			
		Min.	Max.	Min.	Typ. Max.	Min.	Max.		
V_{OH}	Output High Voltage	2.45		2.70		2.50		V	V_{CC} = 4.5 V I_{OH} = -60µA @ -55°C = -60µA @ 25°C = -100µA @ 125°C One input at V_{IL} (see below)
V_{OL}	Output Low Voltage		0.2		0.2		0.25	V	V_{CC} = 5.5 V I_{OL} = 1.58 mA @ -55°C = 1.60 mA @ 25°C = 1.46 mA @ 125°C Inputs at V_{IH} (see below)
V_{IL}	Input Low Voltage		0.7		0.9		0,7	V	Guaranteed input low threshold for all inputs
V_{IH}	Input High Voltage	2		1.7		1.4		V	Guaranteed input high threshold for all inputs
I_F	Input Load Current		-158		-160		-146	µA	V_{CC} = 5.5 V $V_F = V_{OL}$ (see above) on other inputs V_R = 5.5 V
I_R	Input Leakage Current		1		1		10	µA	V_{CC} = 4.5 V V_R = 4.5 V Ground on other inputs
I_{SC}	Output Short Circuit Current	-1	-8.5	-2.8	-8.5	-2	-8.5	mA	V_{CC} = 5.5 V Inputs and output V_{CC} = 4.5 V grounded
I_{PD}	Power Dissipation Current (each gate)		390 165		390 165		410 175	µA	V_{CC} = 5 V Inputs open V_{CC} = 5 V Inputs grounded
t_{pd} +	Turn-off delay				100			nsec	V_{CC} = 5 V
t_{pd} -	Turn-on delay				90			nsec	See test circuit

NOTE (INPUT EXTENSION)

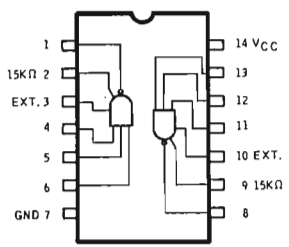
The DTL 9933 4 - input extender element or equivalent - may be used to provide additional diode inputs. Any capacitance added to the extender input will increase the turn-on delay of the LPDTL E305 gate. Typically, the increase is 10 ns/picofarad. Turn - off delay is not affected.



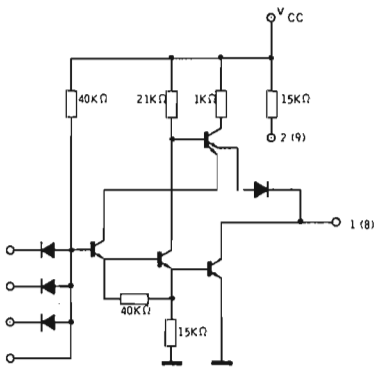
Typical input capacitance of the 9933 is 2 pF and output capacitance is 5 pF.

This element consists of two 3 - input positive logic NAND gates with extender inputs. This element in the family allows the user to implement logic applications requiring a gate fan - in exceeding three. (See E 304 note).

CONNECTION DIAGRAM
(top view)



SCHEMATIC DIAGRAM
(one gate only)

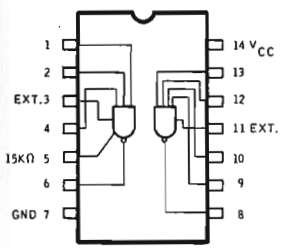


ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%)

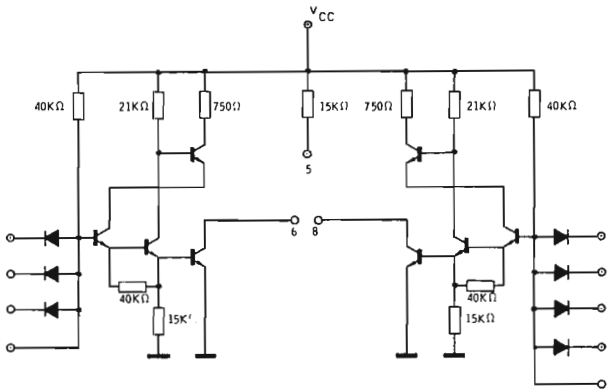
SYMBOL	CHARACTERISTICS	LIMITS						UNIT	CONDITIONS AND COMMENTS
		-55°C		25°C		125°C			
		Min.	Max.	Min.	Typ. Max.	Min.	Max.		
V_{OH}	Output High Voltage	2.45		2.70		2.50		V	V_{CC} = 4.5 V I_{OH} =-60 µA @ - 55°C =-60 µA @ 25°C =-100 µA @ 125°C One input at V_{IL} (see below)
V_{OL}	Output Low Voltage		0.2		0.2		0.25	V	V_{CC} = 5.5 V I_{OL} = 1.58 mA @ - 55°C = 1.60 mA @ 25°C = 1.46 mA @ 125°C Inputs at V_{IH} (see below)
V_{IL}	Input Low Voltage		0.7		0.9		0.7	V	Guaranteed input low threshold for all inputs
V_{IH}	Input High Voltage	2		1.7		1.4		V	Guaranteed input high threshold for all inputs
I_F	Input Load Current		- 158		-160		-146	µA	V_{CC} = 5.5 V $V_F = V_{OL}$ (see above) on other inputs V_R = 5.5 V
I_R	Input Leakage Current		1		1		10	µA	V_{CC} = 4.5 V V_R = 4.5 V Ground on other inputs
I_{SC}	Output Short Circuit Current	-1	-6.5	-2.8	-6.5	-2	-6.5	mA	V_{CC} = 5.5 V Inputs and output V_{CC} = 4.5 V grounded
I_{PD}	Power Dissipation Current (each gate)		390 165		390 165		410 175	µA	V_{CC} = 5 V Inputs open V_{CC} = 5 V Inputs grounded
t_{pd+}	Turn-off delay				150			nsec	V_{CC} = 5 V See test circuit
t_{pd-}	Turn-on delay				150			nsec	

This element consists of one 3 - input, one 4 - input NAND gate with extender input and bare collector output.
It also has one pull-up resistor available which may be used for "wired OR" applications or implementing logic applications requiring interfacing into different logic levels (for fan-in extension see E 304 note).

CONNECTION DIAGRAM
(top view)



SCHEMATIC DIAGRAM

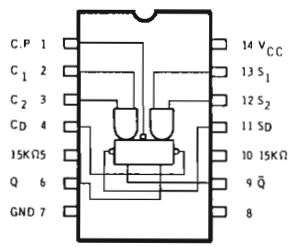


ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V ± 10%)

SYMBOL	CHARACTERISTICS	LIMITS -55°C Min.	LIMITS -55°C Max.	LIMITS 25°C Min.	LIMITS 25°C Typ.	LIMITS 25°C Max.	LIMITS 125°C Min.	LIMITS 125°C Max.	UNIT	CONDITIONS AND COMMENTS
V_{OH}	Output High Voltage	2.70		2.70			2.50		V	V_{CC} = 4.5 V I_{OH} = - 80 µA @ -55°C = - 80 µA @ 25°C = - 80 µA @ 125°C Pin 6 (8) and Pin 5 tied together one input at V_{IL} (see below)
V_{OL}	Output Low Voltage		0.2		0.2			0.25	V	V_{CC} = 5.5 V I_{OL} = 1.58 mA @ - 55°C = 1.60 mA @ 25°C = 1.46 mA @ 125°C inputs at V_{IH} (see below)
V_{IL}	Input Low Voltage		0.7		0.9			0.7	V	Guaranteed input low threshold for all inputs
V_{IH}	Input High Voltage	2		1.7			1,4		V	Gueranteed input high threshold for all inputs
I_F	Input Load Current		-158		-160			-146	µA	V_{CC} = 5.5 V V_F = V_{OL} (see above) on other inputs V_R = 5.5 V
I_R	Input Leakage Current		1		1			10	µA	V_{CC} = 4.5 V V_R = 4.5 V ground on other inputs
I_{PD}	Power Dissipation Current (each gate)		390 165		390 165			410 175	µA	V_{CC} = 5 V inputs open V_{CC} = 5 V inputs grounded
t_{pd+} t_{pd-}	Turn-off delay Turn-on delay				400 90				nsec	V_{CC} = 5 V See test circuit

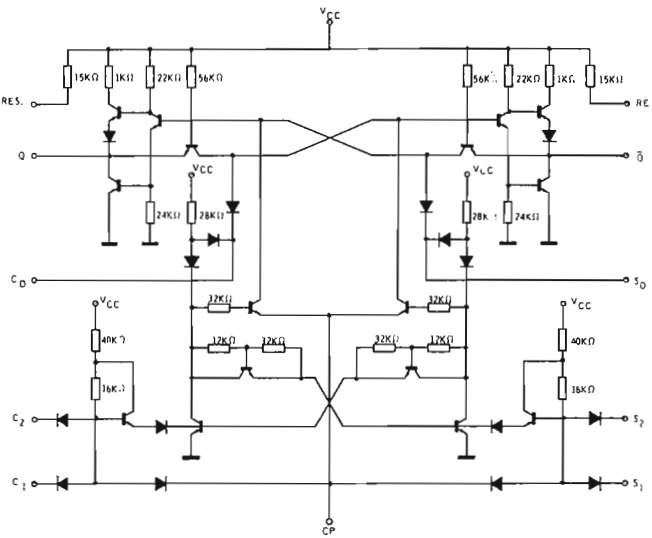
This element is a directly coupled, master-slave flip-flop suitable for use in counters, shift registers and other storage applications. Either R - S or J - K mode operation is possible. Direct set and clear inputs are provided which override all other data inputs.

CONNECTION DIAGRAM
(top view)



For flat package, pin 8 (unconnected) is missing from package.

SCHEMATIC DIAGRAM



TRUTH TABLE

Synchronous Entry Truth Tables										Asynchronous Entry Truth Table			
R - S Mode Operation						J - K Mode Operation							
INPUTS @ t_n				OUTPUTS @ $t_n + 1$		INPUTS @ t_n		OUTPUTS @ t_n+1		INPUTS		OUTPUTS	
S_1	S_2	C_1	C_2	Q	$\bar{Q}$	S_1	C_1	Q	$\bar{Q}$	S_D	C_D	Q	$\bar{Q}$
13	12	2	3	6	9	13	2	6	9	11	4	6	9
L	X	L	X	NC	NC	L	L	NC	NC	H	H	NC	NC
L	X	X	L	NC	NC	L	H	L	H	H	L	L	H
X	L	L	X	NC	NC	H	L	H	L	L	H	H	L
X	L	X	L	NC	NC	H	H	TOGGLES		L	L	H	H
L	X	H	H	L	H								
X	L	H	H	L	H								
H	H	L	X	H	L								
H	H	X	L	H	L								
H	H	H	H	AMBIGUOUS									

Symbols
H - Most positive logic level
L - Most negative logic level
X - Either H or L can be present
NC- No change in state

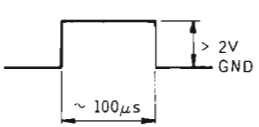
NOTES :

1) For J - K mode operation connect Pin 6 to Pin 3 and Pin 9 to 12.
2) Asynchronous entries override all synchronous entries.

ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V ± 10 %)

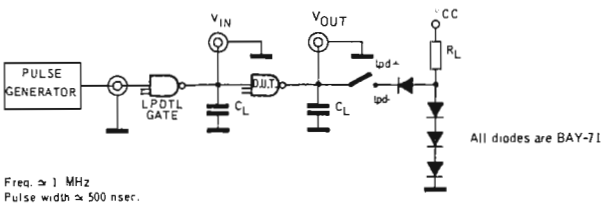
SYMBOL	CHARACTERISTICS	LIMITS -55°C Min.	LIMITS -55°C Max.	LIMITS 25°C Min.	LIMITS 25°C Typ.	LIMITS 25°C Max.	LIMITS 125°C Min.	LIMITS 125°C Max.	UNIT	CONDITIONS AND COMMENTS
V_{OH}	Output High Voltage	2.45		2.70			2.50		V	V_{CC} = 4.5 V I_{OH} = -60 µA @ -55°C = -60 µA @ 25°C = -100 µA @ 125°C V_{ILS} (see below) and V = 4.5 V on proper asynchronous inputs
V_{OL}	Output Low Voltage		0.2			0.2		0.25	V	V_{CC} = 5.5 V I_{OL} = 1.58 mA @ -55°C = 1.60 mA @ 25°C = 1.46 mA @ 125°C V = 5.5 V and V = -0.5 V on proper asynchronous inputs
V_{IL}	Input Low Voltage		0.7			0.9		0.7	V	Guaranteed input low threshold for synchronous inputs
V_{ILS}	Input Low Voltage		0.7			0.6		0.4	V	Guaranteed input low threshold for asynchronous inputs
V_{IH}	Input High Voltage	2		1.7			1.4		V	Guaranteed input high threshold for synchronous inputs
I_F	Input Load Current C and S Inputs		-119			-120		-110	µA	V_{CC} = 5.5 V V_F = V_{OL} (see above) 5.5 V on clock and other input
I_F	Input Load Current C_D and S_D Inputs		-395			-400		-365	µA	V_{CC} = 5.5 V V_F = V_{OL} (see above) ground on clock and other asynchronous input
I_F	Input Load Current Clock Input		-395			-400		-365	µA	V_{CC} = 5.5 V V_F = V_{OL} (see above) V_{ILS} on one asynchronous input 5.5 V on all other inputs
I_R	Input Leakage Current C and S Inputs		1			1		10	µA	V_{CC} = 4.5 V V_R = 4.5 V ground on other input and clock
I_R	Input Leakage Current C_D and S_D Inputs		1			1		10	µA	V_{CC} = 4.5 V V_R = 4.5 V on asynchronous inputs, ground on other inputs
I_R	Input Leakage Current Clock Input		15			15		25	µA	V_{CC} = 5.5 V V_R = 4.5 V one asynchronous input open all other inputs grounded
I_{SC}	Output Short Circuit Current	-0.9	-9	-2.8		-9	-2	-9	mA	V_{CC} = 5.5 V one asynchronous input V_{CC} = 4.5 V grounded
I_{PD}	Power Dissipation Current		1.10			1.10		1.35	mA	V_{CC} = 5 V one asynchronous input grounded
t_{pd} +	Turn-off delay					100			nsec	V_{CC} = 5 V
t_{pd} -	Turn-on delay					250			nsec	See test circuit

CP - DESCRIPTION



GATES : SWITCHING TIME CHARACTERISTICS

t_{pd} TEST CIRCUIT

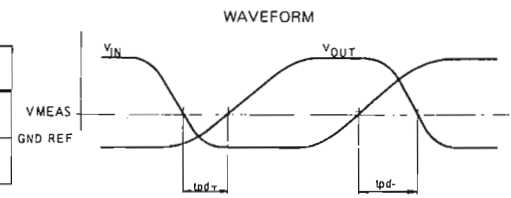


Freq. ≃ 1 MHz
Pulse width ≃ 500 nsec.
Rise time < 50 nsec.
Fall time < 50 nsec.
Ampl. = 4V ± 25%

TEST CONDITIONS

Test	V_{CC}	R_L	R_L E3060only	C_L*	V measure
t_{pd} +	5 V	∞	** ∞	50 pF	1.3V
t_{pd} -	5 V	3.9 KΩ	2.8 KΩ	50 pF	1.3V

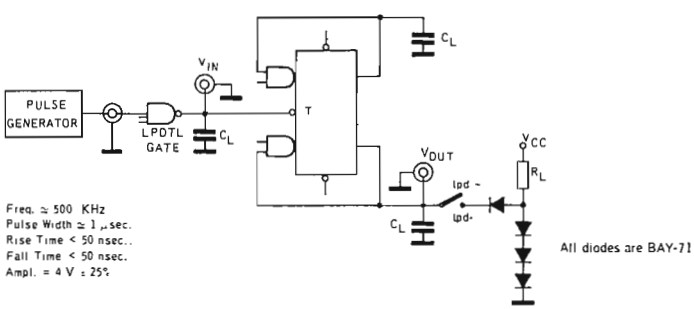
WAVEFORM



* Includes all probe and test jig capacitance
** Pin 5 connected To 6 (8)

FLIP-FLOP : SWITCHING TIME CHARACTERISTICS

t_{pd} TEST CIRCUIT



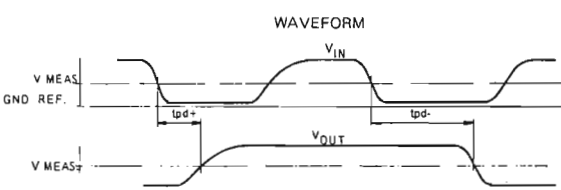
Freq. ≃ 500 KHz
Pulse Width ≃ 1 μsec.
Rise Time < 50 nsec..
Fall Time < 50 nsec.
Ampl. = 4 V ± 25%

TEST CONDITIONS

Test	V_{CC}	R_L	C_L *	V measure
t_{pd} +	5 V	∞	50 pF	1.3V
t_{pd} -	5 V	3.9K Ω	50 pF	1.3V

* includes all probe and test jig capacitance

WAVEFORM



low - power diode - transistor logic family

STANDARD TEMPERATURE RANGE - 20°C ÷ 100°C

- **Compatible with DTL and TTL products**
- **Power dissipation 1 mW per gate**
- **Noise immunity 1V**
- **Worst case noise immunity 450 mV**
- **Output drive capability of 10**
- **Fan-in expansion capability**
- **Wired-OR capability**
- **Same pin configuration as the corresponding DTL and TTL products**

The SGS LPDTL Integrated Circuit Family consists of a set of compatible, integrated logic circuits specifically designed for low power, medium speed applications.
The circuits are fabricated within a silicon monolithic substrate using the standard Planar epitaxial process.
LPDTL elements are available in two hermetically sealed ceramic packages : the Dual In-Line Package (D) designed for low cost insertion, and the 14 leads flat package (F) for maximum density.

ORDERING NUMBERS

E3XXD7 (for Dual in-Line package, 3XX is Type number)
E3XXF7 (for Flat package, 3XX is Type number)

ABSOLUTE MAXIMUM RATINGS

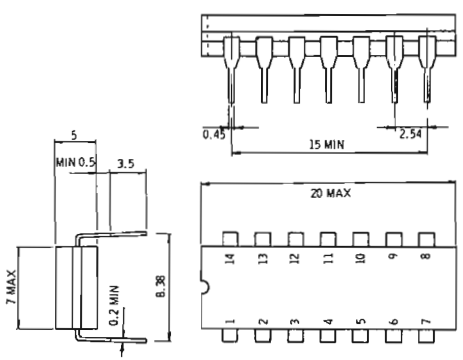
(above which the useful life may be impaired)

Supply Voltage (V_{CC}), continuous	8 V
Supply Voltage (V_{CC}), pulsed, 1 sec.	12 V
Storage Temperature Range	- 65°C to 150°C
Temperature (Ambient) under bias	- 55°C to 125°C

OPERATING CONDITIONS

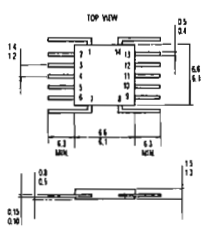
Temperature range	- 20°C to 100°C
Supply voltage (V_{CC})	5 V ± 10 %

PHYSICAL DIMENSIONS
14-pin ceramic DIP



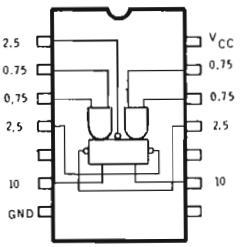
Note : all dimensions in mm.

PHYSICAL DIMENSIONS
FLAT PACKAGE

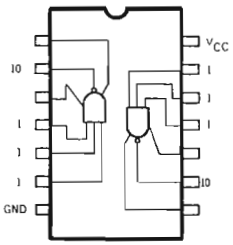


Note: All dimensions in mm.

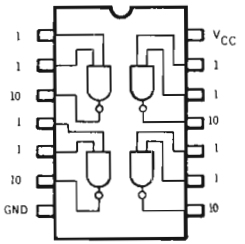
INPUT-OUTPUT LOAD/DRIVE FACTORS



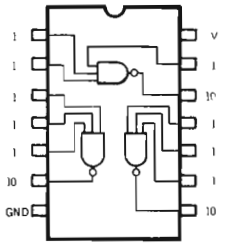
E 300



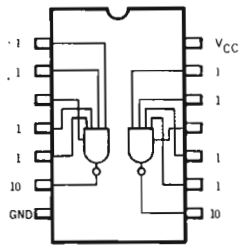
* E 301



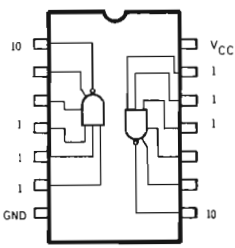
E 302



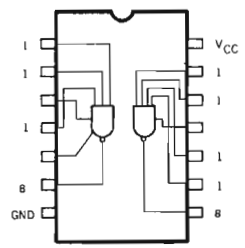
E 303



E 304



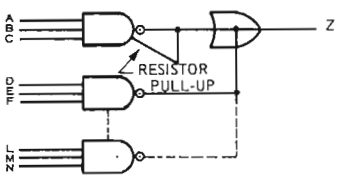
E 305



* E 306

* NOTE :
Wired-OR operation is allowed only with E301 and E306.

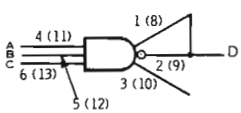
WIRED "OR" APPLICATIONS



$\overline{A\ B\ C + D\ E\ F + \ldots\ldots\ldots\ L\ M\ N} = Z$

Output drive factor = (10 · 3 n) unit load
(n = No. of resistor pull-ups)

One pull-up resistor is required for every 13 gates connected to the common "OR" node.



E 301

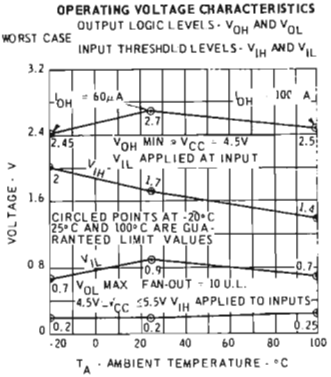
$\overline{A\ B\ C} = D$

Output drive factor = 10 unit load
= 7 U.L. with resistor pull-up connected

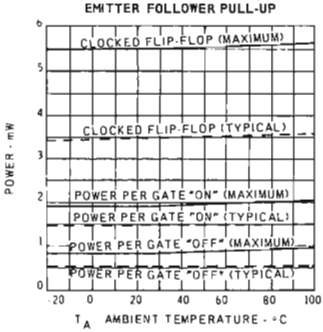
Either the emitter follower or resistor pull-up must be connected to the output to establish the high level.

ELECTRICAL CHARACTERISTICS

OPERATING VOLTAGE CHARACTERISTICS

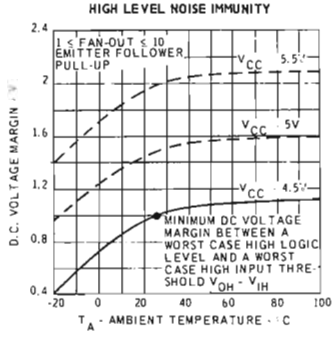


POWER CHARACTERISTICS V_{CC} 5V
EMITTER FOLLOWER PULL-UP

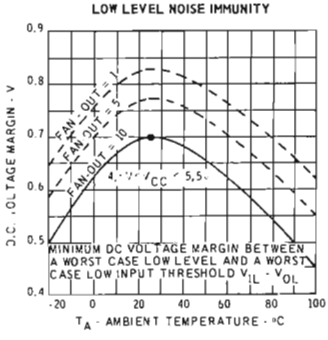


NOISE IMMUNITY

HIGH LEVEL NOISE IMMUNITY

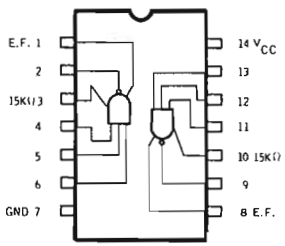


LOW LEVEL NOISE IMMUNITY

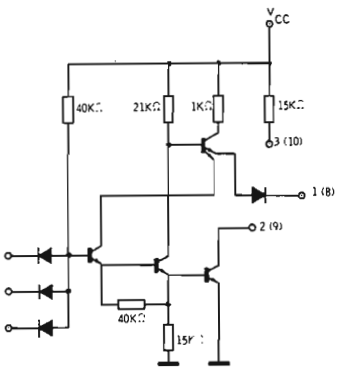


This element consists of two, 3 - input positive logic NAND gates suitable for general logic gate and inverter applications. The peculiar feature of this gate is that the output transistor collector and the emitter follower pull-up are not internally connected. This allows the user to tie collectors to a common node for the wired "OR" logic function.

CONNECTION DIAGRAM
(top view)



SCHEMATIC DIAGRAM
(one gate only)



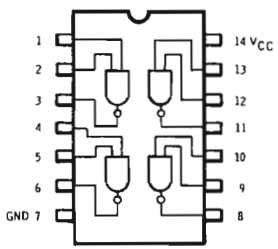
ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10 %)

SYMBOL	CHARACTERISTICS	LIMITS -20°C Min.	LIMITS -20°C Max.	LIMITS 25°C Min.	LIMITS 25°C Typ.	LIMITS 25°C Max.	LIMITS 100°C Min.	LIMITS 100°C Max.	UNIT	CONDITIONS AND COMMENTS
V_{OH}	Output High Voltage	2.45		2.7			2.5		V	V_{CC} = 4.5 V I_{OH} = -60 µA @ -20°C = -60 µA @ 25°C = -100 µA @ 100°C One input at V_{IL} (see below)
V_{OL}	Output Low Voltage		0.2			0.2		0.25	V	V_{CC} = 5.5 V I_{OL} = 1.6 mA @ -20°C = 1.6 mA @ 25°C = 1.5 mA @ 100°C Inputs at V_{IH} (see below)
V_{IL}	Input Low Voltage		0.7			0.9		0.7	V	Guaranteed input low threshold for all inputs
V_{IH}	Input High Voltage	2		1.7			1.4		V	Guaranteed input high threshold for all inputs
I_F	Input Load Current		-160			-160		-150	µA	V_{CC} = 5.5 V V_F = V_{OL} (see above) on other inputs V_R = 5.5 V
I_R	Input Leakage Current		1			1		10	µA	V_{CC} = 4.5 V V_R = 4.5 V Ground on other inputs
I_{SC}	Output Short Circuit Current	-1	-6.5	- 2.2		-6.5	-1.95	-6.5	mA	V_{CC} = 5.5 V Inputs and output V_{CC} = 4.5 V grounded
I_{PD}	Power Dissipation Current (each gate)		390 165			390 165		410 175	µA	V_{CC} = 5 V Inputs at V_{IH} (see above) V_{CC} = 5 V Inputs grounded
t_{pd+}	Turn-off delay					150			nsec	V_{CC} = 5 V See test circuit
t_{pd-}	Turn-on delay					150			nsec	

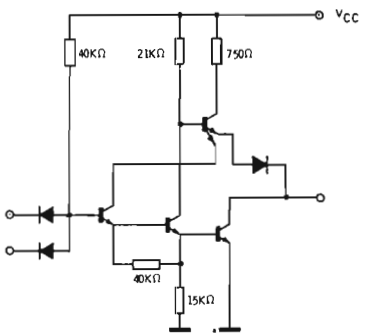
Note : Pin 1 and Pin 2 (8 and 9) must be tied together when testing this element

This element consists of four, 2 - input NAND gates with active pull-up. Its logic function and pin configuration are identical to the DTL 9946, and TTL T102 gate elements. This element is suitable for general logic, latches and inverter applications where minimum power consumption is important.

CONNECTION DIAGRAM
(top view)



SCHEMATIC DIAGRAM
(one gate only)

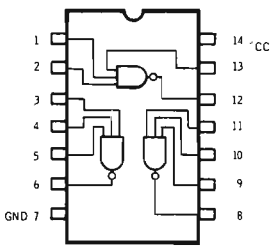


ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%)

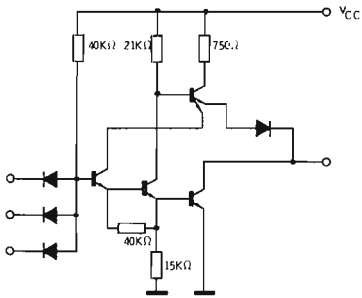
SYMBOL	CHARACTERISTICS	LIMITS - 20°C Min.	LIMITS - 20°C Max.	LIMITS 25°C Min.	LIMITS 25°C Typ.	LIMITS 25°C Max.	LIMITS 100°C Min.	LIMITS 100°C Max.	UNIT	CONDITIONS AND COMMENTS
V_{OH}	Output High Voltage	2.45		2.70			2.50		V	V_{CC} = 4.5 V I_{OH} = -60 µA @ - 20°C = -60 µA @ 25°C = -100 µA @ 100°C One input at V_{IL} (see below)
V_{OL}	Output Low Voltage		0.2		0.2			0.25	V	V_{CC} = 5.5 V I_{OL} = 1.6 mA @ - 20°C = 1.6 mA @ 25°C = 1.5 mA @ 100°C Inputs at V_{IH} (see below)
V_{IL}	Input Low Voltage		0.7		0.9			0.7	V	Guaranteed input low threshold for all inputs
V_{IH}	Input High Voltage	2		1.7			1.4		V	Guaranteed input high threshold for all inputs
I_F	Input Load Current		-160		-160			-150	µA	V_{CC} = 5.5 V V_F = V_{OL} (see above) on other inputs V_R = 5.5 V
I_R	Input Leakage Current		1		1			10	µA	V_{CC} = 4.5 V V_R = 4.5 V Ground on other inputs
I_{SC}	Output Short Circuit Current	-1	-8.5	-2.2	-8.5		-1.95	-8.5	mA	V_{CC} = 5.5 V Inputs and output V_{CC} = 4.5 V grounded
I_{PD}	Power Dissipation Current (each gate)		390 165		390 165			410 175	µA	V_{CC} = 5 V Inputs at V_{IH} (see above) V_{CC} = 5 V Inputs grounded
t_{pd+}	Turn-off delay				90				nsec	V_{CC} = 5 V See test circuit
t_{pd-}	Turn-on delay				60				nsec	

This element consists of three, 3 - input NAND gate with active pull-up. Its logic function and pin configuration are identical to the DTL 9962 and TTL T103 gate elements.

CONNECTION DIAGRAM
(top view)



SCHEMATIC DIAGRAM
(one gate only)



ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%)

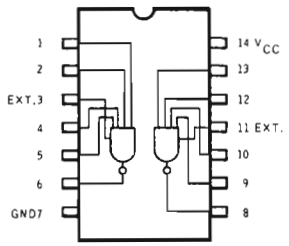
SYMBOL	CHARACTERISTICS	LIMITS - 20°C Min.	LIMITS - 20°C Max.	LIMITS 25°C Min.	LIMITS 25°C Typ.	LIMITS 25°C Max.	LIMITS 100°C Min.	LIMITS 100°C Max.	UNIT	CONDITIONS AND COMMENTS
V_{OH}	Output High Voltage	2.45		2.7			2.5		V	V_{CC} = 4.5 V I_{OH} = -60 µA @ - 20°C = -60 µA @ 25°C = -100 µA @ 100°C One input at V_{IL} (see below)
V_{OL}	Output Low Voltage		0.2		0.2			0.25	V	V_{CC} = 5.5 V I_{OL} = 1.6 mA @ - 20°C = 1.6 mA @ 25°C = 1.5 mA @ 100°C Inputs at V_{IH} (see below)
V_{IL}	Input Low Voltage		0.7		0.9			0.7	V	Guaranteed input low threshold for all inputs
V_{IH}	Input High Voltage	2		1.7			1.4		V	Guaranteed input high threshold for all inputs
I_F	Input Load Current		-160			-160		-150	µA	V_{CC} = 5.5 V V_F = V_{OL} (see above) on other inputs V_R = 5.5 V
I_R	Input Leakage Current		1			1		10	µA	V_{CC} = 4.5 V V_R = 4.5 V Ground on other inputs
I_{SC}	Output Short Circuit Current	-1	-3.5	-2.2		-8.5	-1.95	-8.5	mA	V_{CC} = 5.5 V Inputs and output V_{CC} = 4.5 V grounded
I_{PD}	Power Dissipation Current (each gate)		390 165			390 165		410 175	µA	V_{CC} = 5 V Inputs at V_{IH} (see above) V_{CC} = 5 V Inputs grounded
t_{pd+}	Turn-off delay					100			nsec	V_{CC} = 5 V See test circuit
t_{pd-}	Turn-on delay					60			nsec	

Dual 4-Input Nand Gate With Extender **E 304**

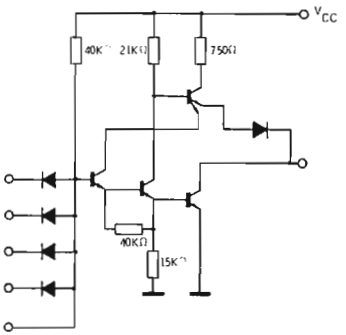
STANDARD TEMPERATURE RANGE

This element consists of two 4-input NAND gates with extender input and active pull-up. Its logic function and pin configuration are identical to the DTL 9930 gate and the TTL T104 gate. It combines the advantages of the active pull-ups, with the advantages offered by the extender inputs (see note).

CONNECTION DIAGRAM
(top view)



SCHEMATIC DIAGRAM
(one gate only)

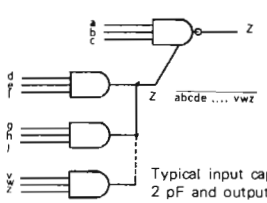


ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V ± 10%)

SYMBOL	CHARACTERISTICS	LIMITS - 20°C Min.	LIMITS - 20°C Max.	LIMITS 25°C Min.	LIMITS 25°C Typ.	LIMITS 25°C Max.	LIMITS 100°C Min.	LIMITS 100°C Max.	UNIT	CONDITIONS AND COMMENTS
V_{OH}	Output High Voltage	2.45		2.7			2.5		V	V_{CC} = 4.5 V I_{OH} = -60µA @ - 20°C = -60µA @ 25°C = -100µA @ 100°C One input at V_{IL} (see below)
V_{OL}	Output Low Voltage		0.2			0.2		0.25	V	V_{CC} = 5.5 V I_{OL} = 1.6 mA @ - 20°C = 1.6 mA @ 25°C = 1.5 mA @ 100°C Inputs at V_{IH} (see below)
V_{IL}	Input Low Voltage		0.7			0.9		0.7	V	Guaranteed input low threshold for all inputs
V_{IH}	Input High Voltage	2		1.7			1.4		V	Guaranteed input high threshold for all inputs
I_F	Input Load Current		-160			-160		-150	µA	V_{CC} = 5.5 V V_F = V_{OL} (see above) on other inputs V_R = 5.5 V
I_R	Input Leakage Current		1			1		10	µA	V_{CC} = 4.5 V V_R = 4.5 V Ground on other inputs
I_{SC}	Output Short Circuit Current	-1	-8.5	-2.2		-8.5	-1.95	-8.5	mA	V_{CC} = 5.5 V Inputs and output V_{CC} = 4.5 V grounded
I_{PD}	Power Dissipation Current (each gate)		390 165			390 165		410 175	µA	V_{CC} = 5 V Inputs at V_{IH} (see above) V_{CC} = 5 V Inputs grounded
t_{pd} +	Turn-off delay					100			nsec	V_{CC} = 5 V
t_{pd} -	Turn-on delay					90			nsec	See test circuit

NOTE (INPUT EXTENSION)

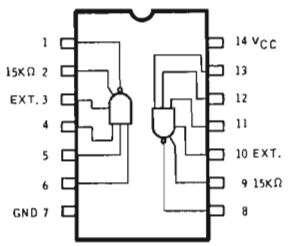
The DTL 9933 4 - input extender element or equivalent - may be used to provide additional diode inputs. Any capacitance added to the extender input will increase the turn-on delay of the LPDTL E305 gate. Typically, the increase is 10 ns/picofarad. Turn - off delay is not affected.



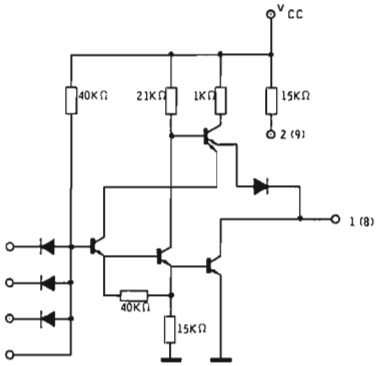
Typical input capacitance of the 9933 is 2 pF and output capacitance is 5 pF.

This element consists of two 3 - input positive logic NAND gates with extender inputs. This element in the family allows the user to implement logic applications requiring a gate fan - in exceeding three. (See E 304 note).

CONNECTION DIAGRAM
(top view)



SCHEMATIC DIAGRAM
(one gate only)



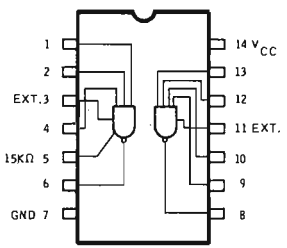
ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V \pm 10\%$)

SYMBOL	CHARACTERISTICS	LIMITS - 20°C Min.	LIMITS - 20°C Max.	LIMITS 25°C Min.	LIMITS 25°C Typ.	LIMITS 25°C Max.	LIMITS 100°C Min.	LIMITS 100°C Max.	UNIT	CONDITIONS AND COMMENTS
V_{OH}	Output High Voltage	2.45		2.7			2.5		V	$V_{CC} = 4.5$ V $I_{OH} = -60\,\mu A$ @ -20°C $= -60\,\mu A$ @ 25°C $= -100\,\mu A$ @ 100°C One input at V_{IL} (see below)
V_{OL}	Output Low Voltage		0.2		0.2	0.25			V	$V_{CC} = 5.5$ V $I_{OL} = 1.6$ mA @ -20°C $= 1.6$ mA @ 25°C $= 1.5$ mA @ 100°C Inputs at V_{IH} (see below)
V_{IL}	Input Low Voltage		0.7		0.9	0.7			V	Guaranteed input low threshold for all inputs
V_{IH}	Input High Voltage	2		1.7			1.4		V	Guaranteed input high threshold for all inputs
I_F	Input Load Current		-160		-160	-150			µA	$V_{CC} = 5.5$ V $V_F = V_{OL}$ (see above) on other inputs $V_R = 5.5$ V
I_R	Input Leakage Current		1		1	10			µA	$V_{CC} = 4.5$ V $V_R = 4.5$ V Ground on other inputs
I_{SC}	Output Short Circuit Current	-1	-6.5	2.2	-6.5	-6.5	-1.95		mA	$V_{CC} = 5.5$ V Inputs and output $V_{CC} = 4.5$ V grounded
I_{PD}	Power Dissipation Current (each gate)		390 165		390 165	410 175			µA	$V_{CC} = 5$ V Inputs at V_{IH} (see above) $V_{CC} = 5$ V Inputs grounded
t_{pd+}	Turn-off delay				150				nsec	$V_{CC} = 5$ V See test circuit
t_{pd-}	Turn-on delay				150				nsec	

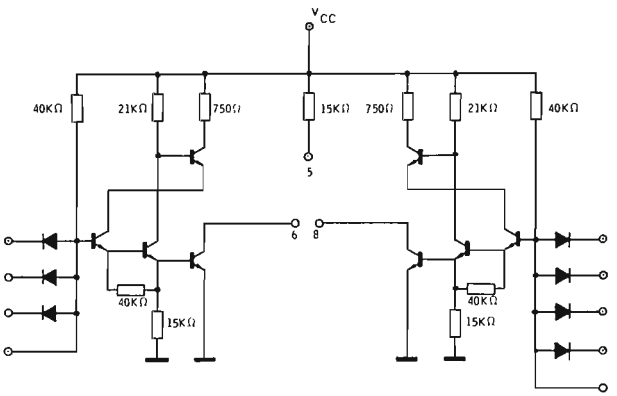
STANDARD TEMPERATURE RANGE

This element consists of one 3 - input, one 4 - input NAND gate with extender input and bare collector output.
It also has one pull-up resistor available which may be used for "wired OR" applications or implementing logic applications requiring interfacing into differant logic levels (for fan-in extension see E 304 note).

CONNECTION DIAGRAM
(top view)



SCHEMATIC DIAGRAM

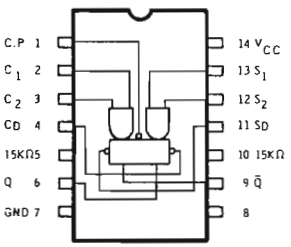


ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V ± 10%)

SYMBOL	CHARACTERISTICS	LIMITS - 20°C Min.	LIMITS - 20°C Max.	LIMITS 25°C Min.	LIMITS 25°C Typ.	LIMITS 25°C Max.	LIMITS 100°C Min.	LIMITS 100°C Max.	UNIT	CONDITIONS AND COMMENTS
V_{OH}	Output High Voltage	2.7		2.7			2.5		V	V_{CC} = 4.5 V I_{OH} = - 80 µA @ - 20°C = - 80 µA @ 25°C = - 80 µA @ 100°C Pin 6 (8) and Pin 5 tied together one input at V_{IL} (see below)
V_{OL}	Output Low Voltage		0.2		0.2			0.25	V	V_{CC} = 5.5 V I_{OL} = 1.6 mA @ - 20°C = 1.6 mA @ 25°C = 1.5 mA @ 100°C inputs at V_{IH} (see below)
V_{IL}	Input Low Voltage		0.7		0.9			0.7	V	Guaranteed input low threshold for all inputs
V_{IH}	Input High Voltage	2		1.7			1.4		V	Guaranteed input high threshold for all inputs
I_F	Input Load Current		-160		-160			-150	µA	V_{CC} = 5.5 V $V_F = V_{OL}$ (see above) on other inputs V_R = 5.5 V
I_R	Input Leakage Current		1		1			10	µA	V_{CC} = 4.5 V V_R = 4.5 V ground on other inputs
I_{PD}	Power Dissipation Current (each gata)		390 165		390 165			410 175	µA	V_{CC} = 5 V inputs at V_{IH} (see above) V_{CC} = 5 V inputs grounded
t_{pd+} t_{pd-}	Turn-off delay Turn-on delay				400 90				nsec	V_{CC} = 5 V See test circuit

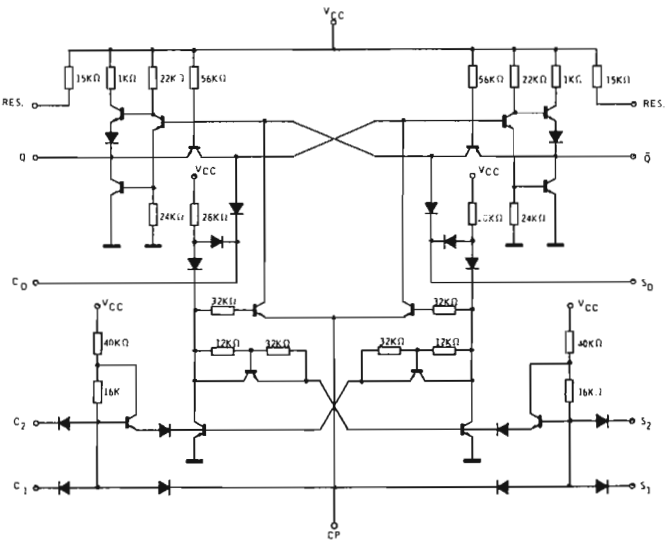
This element is a directly coupled, master-slave flip-flop suitable for use in counters, shift registers and other storage applications. Either R - S or J - K mode operation is possible. Direct set and clear inputs are provided which override all other data inputs.

CONNECTION DIAGRAM
(top view)



For flat package, pin 8 (unconnected) is missing from package.

SCHEMATIC DIAGRAM



TRUTH TABLE

Synchronous Entry Truth Tables										Asynchronous Entry Truth Table			
R - S Mode Operation						J - K Mode Operation							
INPUTS @ t_n				OUTPUTS @ $t_n + 1$		INPUTS @ t_n		OUTPUTS @ $t_n + 1$		INPUTS		OUTPUTS	
S_1	S_2	C_1	C_2	Q	$\bar{Q}$	S_1	C_1	Q	$\bar{Q}$	S_D	C_D	Q	$\bar{Q}$
13	12	2	3	6	9	13	2	6	9	11	4	6	9
L	X	L	X	NC	NC	L	L	NC	NC	H	H	NC	NC
L	X	X	L	NC	NC	L	H	L	H	H	L	L	H
X	L	L	X	NC	NC	H	L	H	L	L	H	H	L
X	L	X	L	NC	NC	H	H	TOGGLES		L	L	H	H
L	X	H	H	L	H								
X	L	H	H	L	H								
H	H	L	X	H	L								
H	H	X	L	H	L								
H	H	H	H	AMBIGUOUS									

Symbols
H - Most positive logic level
L - Most negative logic level
X - Either H or L can be present
NC- No change in state

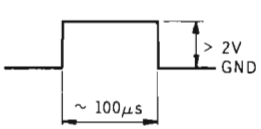
NOTES :

1) For J - K mode operation connect Pin 6 to Pin 3 and Pin 9 to 12.
2) Asynchronous entries override all synchronous entries.

ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V ± 10 %)

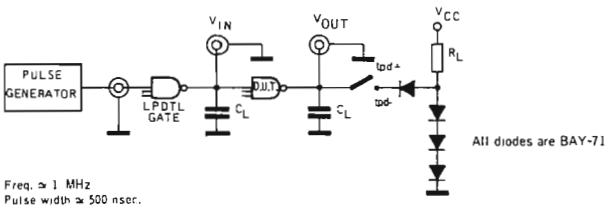
SYMBOL	CHARACTERISTICS	LIMITS						UNIT	CONDITIONS AND COMMENTS
		-20°C		25°C		100°C			
		Min.	Max.	Min.	Typ. Max.	Min.	Max.		
V_{OH}	Output High Voltage	2.45		2.70		2.50		V	V_{CC} = 4.5 V I_{OH} = - 60 µA @ - 55°C = - 60 µA @ 25°C = -100 µA @ 125°C V_{ILS} (see below) and V = 4.5 V on proper asynchronous inputs
V_{OL}	Output Low Voltage		0.2		0.2		0.25	V	V_{CC} = 5.5 V I_{OL} = 1.6 mA @ -55°C = 1.6 mA @ 25°C = 1.5 mA @ 125°C V = 5.5 V and V = - 0.5 V on proper asynchronous inputs
V_{IL}	Input Low Voltage		0.7		0.9		0.7	V	Guaranteed input low threshold for asynchronous inputs
V_{ILS}	Input Low Voltage		0.7		0.6		0.4	V	Guaranteed input low threshold for asynchronous inputs
V_{IH}	Input High Voltage	2		1.7		1.4		V	Guaranteed input high threshold for asynchronous inputs
I_F	Input Load Current C and S Inputs		-119		-120		-110	µA	V_{CC} = 5.5 V V_F = V_{OL} (see above) 5.5 V on clock and other input
I_F	Input Load Current C_D and S_D Inputs		-395		-400		-365	µA	V_{CC} = 5.5 V V_F = V_{OL} (see above) ground on clock and other asynchronous input
I_F	Input Load Current Clock Input		-395		-400		-365	µA	V_{CC} = 5.5 V V_F = V_{OL} (see above) V_{ILS} on one asynchronous input 5.5 V on all other inputs
I_R	Input Leakage Current C and S Inputs		1		1		10	µA	V_{CC} = 4.5 V V_R = 4.5 V ground on other input and clock
I_R	Input Leakage Current C_D and S_D Inputs		1		1		10	µA	V_{CC} = 4.5 V V_R = 4.5 V on asynchronous inputs, ground on other inputs
I_R	Input Leakage Current Clock Input		15		15		25	µA	V_{CC} = 5.5 V V_R = 4.5 V one asynchronous input open,all other inputs grounded
I_{SC}	Output Short Circuit Current	-0.9	- 9	-2	- 9	-1.75	- 9	mA	V_{CC} = 5.5 V one asynchronous input V_{CC} = 4.5 V and output grounded
I_{PD}	Power Dissipation Current		1.10		1.10		1.35	mA	V_{CC} = 5 V one asynchronous input grounded
t_{pd} +	Turn-off delay				100			nsec	V_{CC} = 5 V
t_{pd} -	Turn-on delay				250			nsec	See test circuit

CP - DESCRIPTION



GATES : SWITCHING TIME CHARACTERISTICS

t_{pd} TEST CIRCUIT



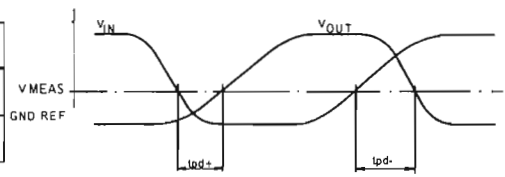
Freq. ≃ 1 MHz
Pulse width ≃ 500 nser.
Rise time < 50 nsec.
Fall time < 50 nsec.
Ampl. = 4V ± 25%

TEST CONDITIONS

Test	V_{CC}	R_L	R_L E306Only	C_L*	V measure
t_{pd} +	5 V	∞	** ∞	50 pF	1.3V
t_{pd} -	5 V	3.9 KΩ	2.8 KΩ	50 pF	1.3V

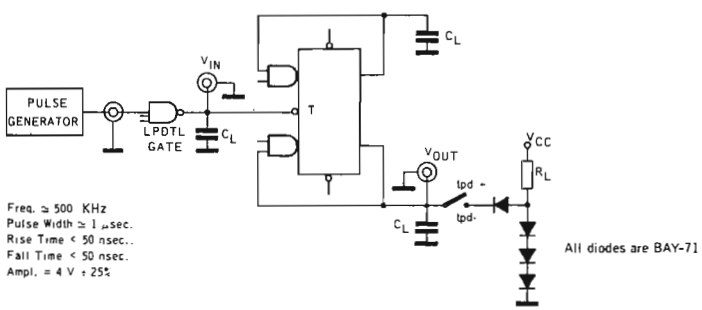
* Ineludes all probe and test jig capacitance
** Pin 5 connected To 6(8)

WAVEFORM



FLIP-FLOP : SWITCHING TIME CHARACTERISTICS

t_{pd} TEST CIRCUIT



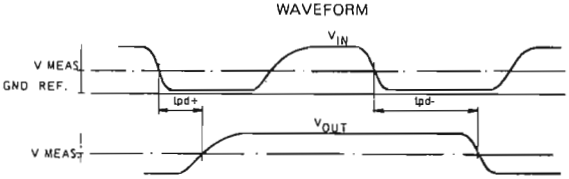
Freq. ≃ 500 KHz
Pulse Width ≃ 1 μsec.
Rise Time < 50 nsec..
Fall Time < 50 nsec.
Ampl. = 4 V ± 25%

TEST CONDITIONS

Test	V_{CC}	R_L	C_L *	V measure
t_{pd} +	5 V	∞	50 pF	1.3V
t_{pd} -	5 V	3.9K Ω	50 pF	1.3V

* includes all probe and test jig capacitance

WAVEFORM



TTL INTEGRATED CIRCUITS

TTL INTEGRATED CIRCUITS

transistor-transistor logic family

EXTENDED TEMPERATURE RANGE - 55°C + 125°C

- Compatible with DTL and LPDTL products
- Input diode clamping
- Noise immunity 1V
- Worst case noise immunity 0.4V
- Output drive capability of 10
- Power dissipation 11 mW per gate
- Gate propagation delay of 6 nsec
- Output pull-up circuit
- Same pin configuration as the corresponding DTL and LPDTL products

The Transistor-Transistor logic integrated circuit family (TTL) combines a high fanout, high noise immunity, low power dissipation and good capacitive load driving capability with low propagation delay times. The circuits are fabricated within a silicon monolithic substrate using Planar Epitaxial processes.

TTL elements are available in two hermetically sealed ceramic packages: the Dual in Line Package (D), designed for low cost insertion, and the 14 lead flat package (F) for maximum component density.

ABSOLUTE MAXIMUM RATINGS

(above which the useful life may be impaired)

V_{CC} pin potential to Ground	- 0.5 V to 8 V
Input Voltage (see Note)	- 0.5 V to 5.5 V
Gate Output Voltage, Inputs Low	- 0.5 V to V_{CC}
Gate Current Into Output Terminal, Inputs High (except T109)	50 mA
Gate Current Into Output Terminal, Inputs High T109	100 mA
Flip-Flop Output Voltage when output is normally high	- 0.5 V to V_{CC}
Flip-Flop Current Into Output Terminal when output is normally low	50 mA
Storage Temperature Range	- 65°C to 150°C
Temperature (Ambient) Under Bias	- 55°C to 125°C

OPERATING CONDITIONS

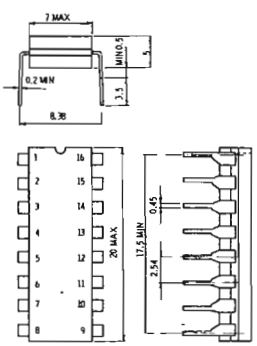
Temperature Range	- 55°C to 125°C
Supply Voltage (V_{CC})	5 V ± 10%

ORDERING NUMBER

TXXXD2 (for Dual in-Line Package, XXX is type number)
TXXXF2 (for Flat Package, XXX is type number)

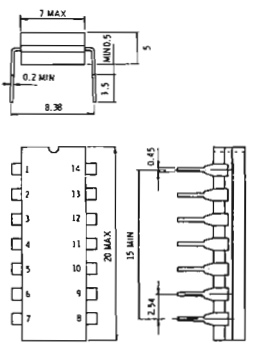
NOTE - Because of the input clamp diodes, excess current can be drawn out of the inputs if the D.C. input voltage is more negative than -0.5 V. The diode is designed to clamp off large negative A.C. swings associated with fast fall times and long lines. This maximum rating is intended only to limit the steady state input voltage and current.

PHYSICAL DIMENSIONS
16-pin ceramic DIP



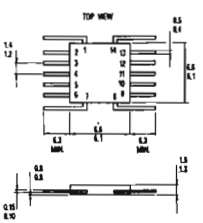
Note : all dimensions in mm.

PHYSICAL DIMENSIONS
14-pin ceramic DIP



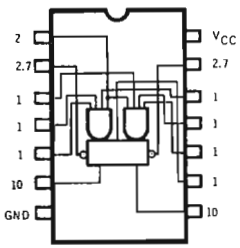
Note : all dimensions in mm.

PHYSICAL DIMENSIONS
Flat ceramic package

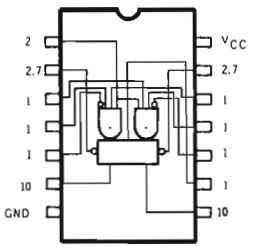


Note: All dimensions in mm.

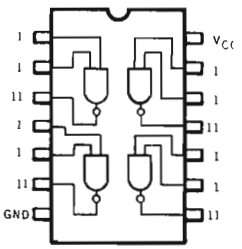
INPUT-OUTPUT LOAD DRIVE FACTORS



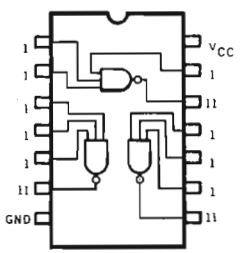
T 100



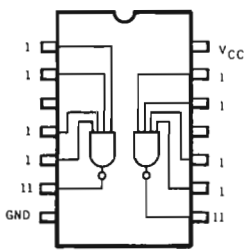
T 101



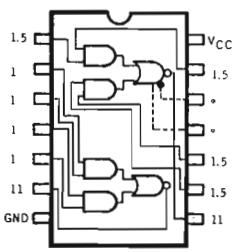
T 102



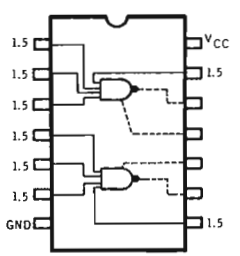
T 103



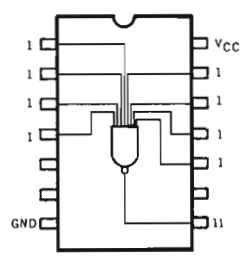
T 104



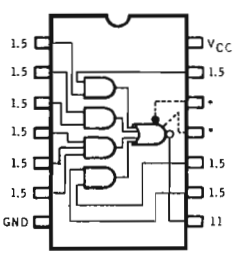
T 105



T 106



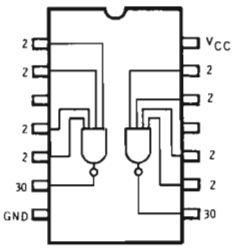
T 107



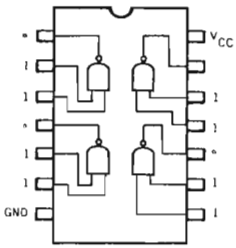
T 108

* Four expanders (T 106) may be tied to these terminals.

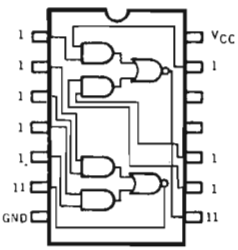
INPUT-OUTPUT LOAD DRIVE FACTORS



T 109



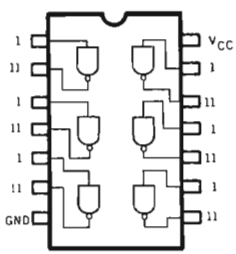
T 112



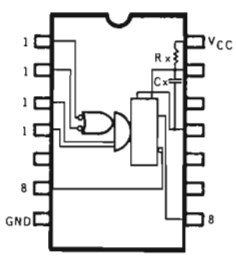
T 115

The number of elements driven by an output terminal depends on the resistance value externally connected between V_{CC} and output pin. When such a resistance is connected, drive factor is given by :

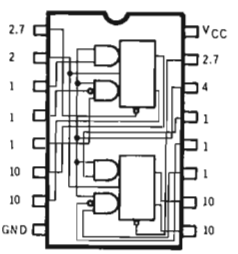
$$\text{drive factor} = 11 - \frac{3.18}{R_{(K\Omega)}}$$



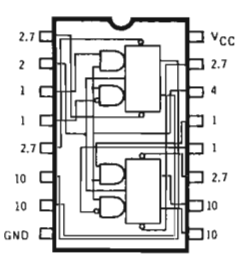
T 116



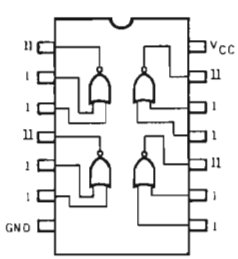
T 118



T 120



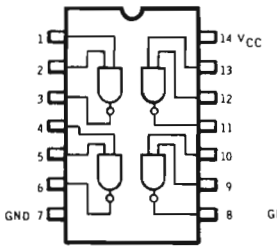
T 121



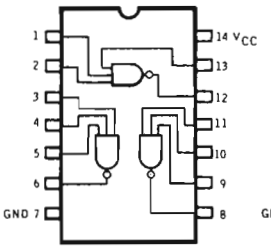
T 122

EXTENDED TEMPERATURE RANGE

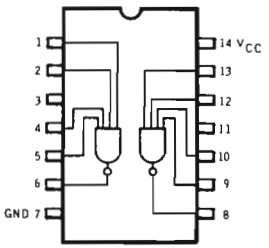
CONNECTION DIAGRAMS (top view)



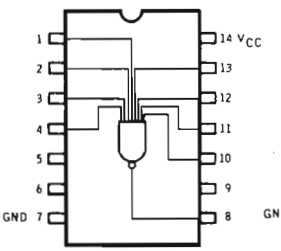
T 102



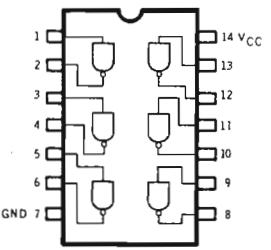
T 103



T 104

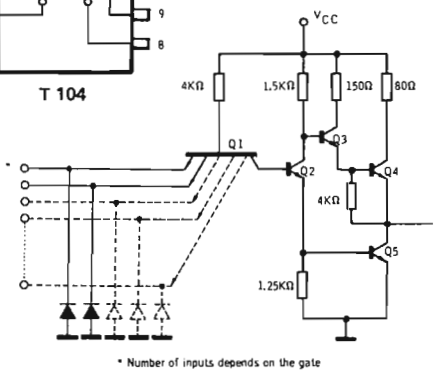


T 107



T 116

BASIC GATE CIRCUIT



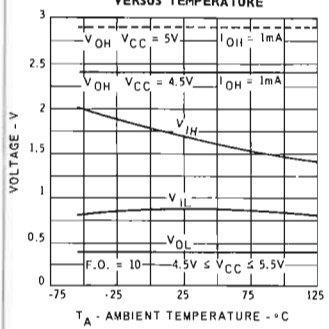
* Number of inputs depends on the gate

ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V ± 10%)

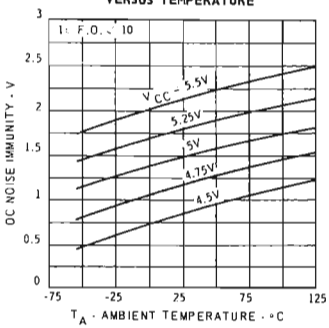
SYMBOL	CHARACTERISTICS	LIMITS						UNIT	CONDITIONS AND COMMENTS
		- 55°C		25°C			125°C		
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		V	V_{CC} = 4.5 V, I_{OH} = -1.32 mA V_{IL} = value indicated below
V_{OL}	Output Low Voltage		0.4		0.21	0.4		0.4	V	V_{CC} = 5.5 V, I_{OL} = 17.6 mA V_{CC} = 4.5 V, I_{OL} = 13.6 mA V_{IH} = value indicated below
V_{IH}	Input High Voltage	2		1.7			1.4		V	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8			0.9		0.8	V	Guaranteed input low threshold for all inputs
I_F	Input Load Current		- 1.6		-1.1	-1.6		-1.6	mA	V_{CC} = 5.5 V, V_F = 0.4 V V_R = 5.5 V on other inputs
I_R	Input Leakage Current				10	60		60	µA	V_{CC} = 5.5 V, V_R = 4.5 V, Gnd on other inputs
I_{SC}	Output Short Circuit Current	-30	-100	-30		-100	-30	-100	mA	V_{CC} = 5.5 V Inputs and output grounded
I_{PD}	Power Dissipation Current (each gate)		5.5		3.5	5.5		5 5	mA	V_{CC} = 5 V inputs open
t_{pd+} t_{pd-}	Turn Off Delay Turn On Delay			3 3		10 12			nsec nsec	V_{CC} = 5 V, C_L = 15 pF See test circuit

EXTENDED TEMPERATURE RANGE

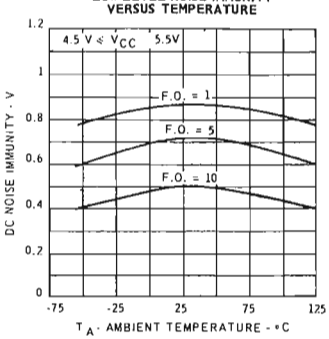
WORST CASE LOGIC LEVELS VERSUS TEMPERATURE



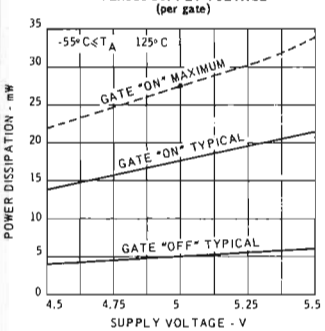
HIGH LEVEL NOISE IMMUNITY VERSUS TEMPERATURE



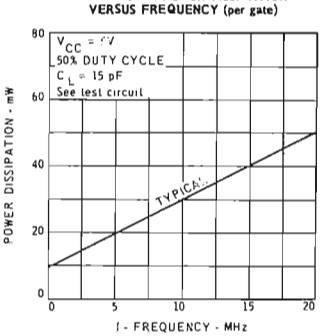
LOW LEVEL NOISE IMMUNITY VERSUS TEMPERATURE



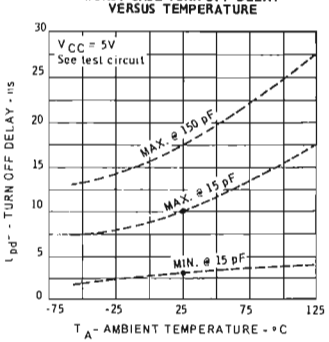
WORST CASE POWER DISSIPATION VERSUS SUPPLY VOLTAGE (per gate)



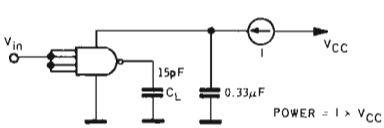
WORST CASE POWER DISSIPATION VERSUS FREQUENCY (per gate)



WORST CASE TURN OFF DELAY VERSUS TEMPERATURE

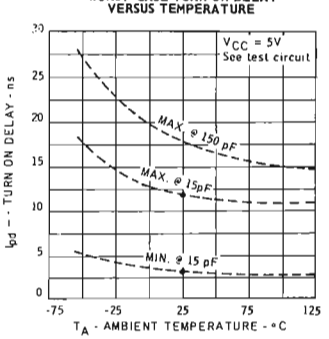


AC POWER TEST CIRCUIT

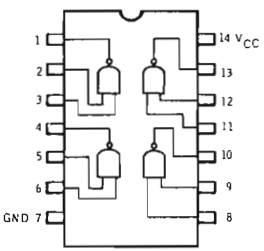


Note: Capacitance includes probe and jig capacity
All inputs to be tied together

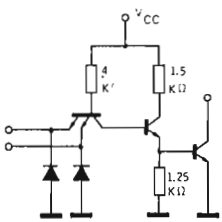
WORST CASE TURN ON DELAY VERSUS TEMPERATURE



CONNECTION DIAGRAM
(top view)



SCHEMATIC DIAGRAM
(one gate only)



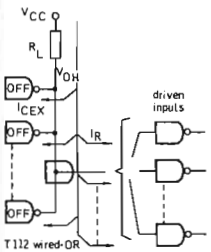
ELECTRICAL CHARACTERISTICS (T_A - 55°C to 125°C, V_{CC} = 5 V ± 10%)

SYMBOL AND CHARACTERISTICS		LIMITS						UNIT	CONDITIONS AND COMMENTS
		- 55°C		25°C		125°C			
		Min.	Max.	Min.	Typ. Max.	Min.	Max.		
V_{OL}	Output Low Voltage		0.4		0.21 0.4		0.4	V	V_{CC} = 5.5V I_{OL} = 17.6 mA V_{IH} = value indicated below
V_{IH}	Input High Threshold	2		1.7		1.4		V	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Threshold		0.8		0.9		0.8	V	Guaranteed input low threshold for all inputs
I_F	Input Load Current		1.6		-1 -1.6		-1.6	mA	V_{CC} = 5.5 V V_F = 0.4V V_R = 5.5V on other input
I_R	Input Leakage Current				10 60		60	µA	V_{CC} = 5.5V V_R = 4.5V ground on other input
I_{CEX}	Output Leakage Current				150		150	µA	V_{CC} = 4.5V inputs grounded 4.5V applied to output
I_{PD}	Power Dissipation Current (each gate)		5.5		3.5 5.5		5.5	mA	V_{CC} = 5V inputs open
t_{pd+}	Turn-Off Delay				32			nsec	V_{CC} = 5V
t_{pd-}	Turn-On Delay				12				C_L = 15 pF see test circuit

RED-OR APPLICATIONS

T102 allows wired-OR operation when a proper load resistor (R_L) is connected between V_{CC} and output pins. General rules to calculate the wed number of wired-OR gates with a requested drive factor are explained here below.
a given number (K) of wired-OR gates and a given number (n) of driven CCSL gates, two equations can be written in order to determine the value he external resistor (R_L) that guarantees a correct operation with respect to the same Noise Immunity levels as the CCSL family.

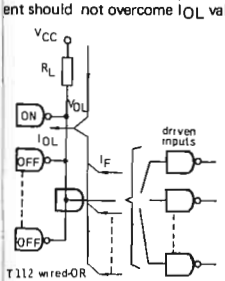
Level : if all the wired-OR gates outputs are at the high level, a total current flows from supply through the external resistor R_L, that is the sum of the output leakage current I_{CEX} of the output wired-OR transistor and the input leakage current I_R of the driven gates. This current takes the output voltage to a value that should not be less than the V_{OH} voltage, that guarantees the high level Noise Immunity. Therefore, to limit this voltage drop, following R_L limitation should be respected :



$$R_{L\,max} = \frac{V_{CC} - V_{OH}}{K I_{CEX} + n\, I_R}$$

note that the resulting R_L value is a worst case as I_{CEX} given in present data sheet is measured at 4.5V instead of 2.4V. Besides even I_R is measured at 4.5 V.

level : when almost one of the wired-OR gates is at the low level (ON), a current flow from supply, through R_L, to the output of the ON transistor current is the ratio of R_L and the allowed voltage drop, (the output leakage current of the OFF wired-OR gates is negligible). In addition, the output ON transistor sinks the output load current I_F of the driven inputs - The V_{OL} voltage guarantees the low level Noise Immunity, that is total sunk ent should not overcome I_{OL} value; therefore, to limit the current through R_L, following limitation should be respected :



$$R_{L\,min} = \frac{V_{CC} - V_{OL}}{I_{OL} - n\, I_F}$$

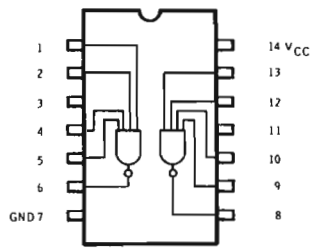
If more than one gate is ON, allowed R_L value is higher.
The two combined equations give maximum and minimum values among which should range R_L value :

$$\frac{V_{CC} - V_{OL}}{I_{OL} - n I_F} \leq R_L \leq \frac{V_{CC} - V_{OH}}{K I_{CEX} + n\, I_R}$$

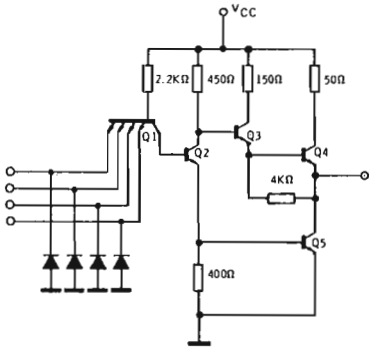
n = number of driven inputs

K = number of wired-OR T112 gates

CONNECTION DIAGRAM
(top view)



SCHEMATIC DIAGRAM
(one gate only)

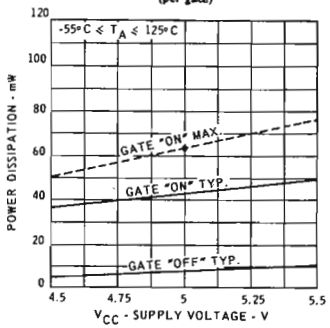


For noise immunity and operating level curves, refer to the gate section.

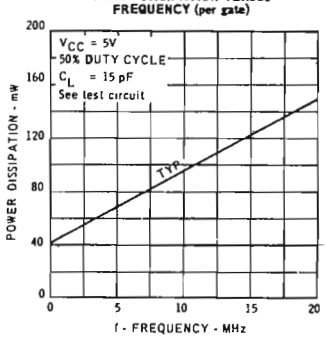
ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V ± 10%)

SYMBOL	CHARACTERISTICS	LIMITS						UNIT	CONDITIONS AND COMMENT
		-55°C		25°C			125°C		
		Min.	Max.	Min.	Typ.	Max.	Min. Max.		
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4	V	V_{CC} = 4.5 V, I_{OH} = - 3.6 mA V_{IL} = value indicated below
V_{OL}	Output Low Voltage		0.4		0.21	0.4	0.4	V	V_{CC} = 5.5 V, I_{OL} = 48 mA V_{CC} = 4.5 V, I_{OL} = 40.8 mA V_{IH} = value indicated below
V_{IH}	Input High Voltage	2		1.7			1.4	V	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8			0.9	0.8	V	Guaranteed input low threshold for all inputs
I_F	Input Load Current		-3.2		-2.2	-3.2	-3.2	mA	V_{CC} = 5.5 V V_F = 0.4 V, V_R = 5.5 V on other inputs
I_R	Input Leakage Current				20	120	120	µA	V_{CC} = 5.5 V, V_R = 4.5 V, Gnd on other inputs
I_{PD}	Power Dissipation Current (each gate)		12.9		8.6	12,9	12,9	mA	V_{CC} = 5 V inputs open
I_{SC}	Output Short Circuit Current	-40	-150	-40		-150	-40 -150	mA	V_{CC}= 5.5 V inputs and output grounded
t_{pd+} t_{pd-}	Turn Off Delay Turn On Delay			4 3		15 10		nsec nsec	V_{CC} = 5 V, C_L = 15 pF See test circuit

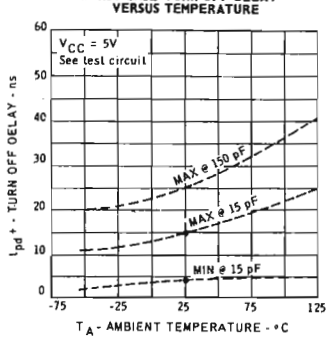
WORST CASE POWER DISSIPATION VERSUS SUPPLY VOLTAGE (per gate)



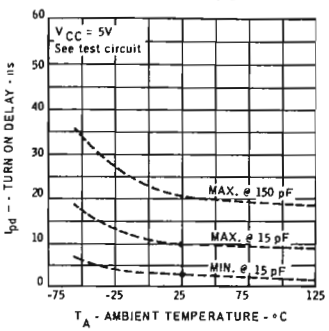
POWER DISSIPATION VERSUS FREQUENCY (per gate)



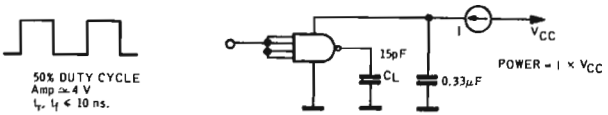
WORST CASE TURN OFF DELAY VERSUS TEMPERATURE



WORST CASE TURN ON DELAY VERSUS TEMPERATURE



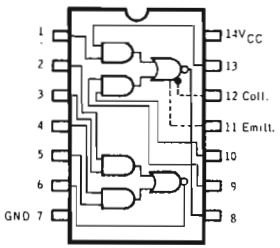
AC POWER TEST CIRCUIT



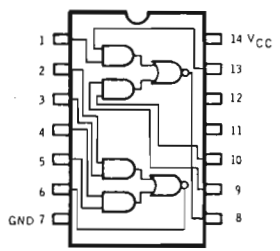
NOTE : Capacitance includes probe and jig capacity - All inputs are to be tied together

The TTL T105 and T108 are AND – NOR gates which may be NOR expanded with the use of the T106 element.

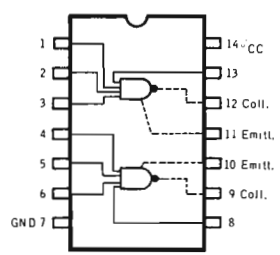
CONNECTION DIAGRAMS
(top view)



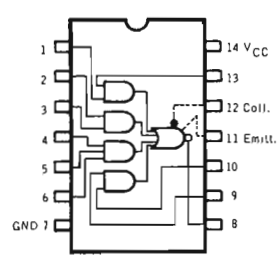
T 105



T 115

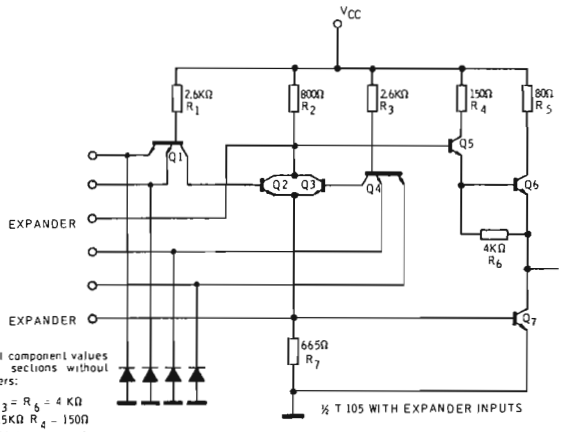


T 106

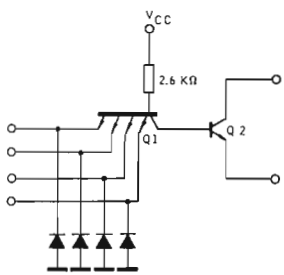


T 108

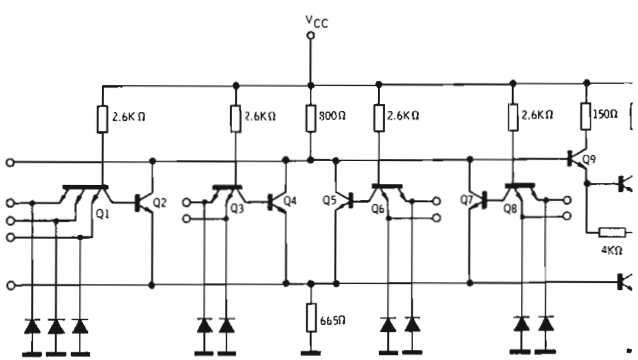
SCHEMATIC DIAGRAMS



T 105 - T 115



T 106 (one gate)



T 108

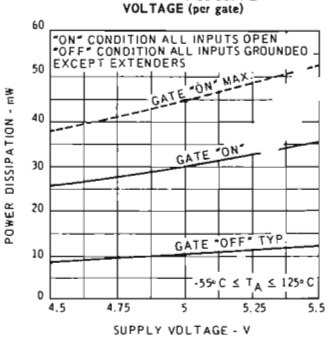
ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V ± 10%)

SYMBOL	CHARACTERISTICS	LIMITS						UNIT	CONDITIONS AND COMMENTS
		-55°C		25°C			125°C		
		Min.	Max.	Min.	Typ.	Max.	Min. Max.		
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4	V	V_{CC} = 4.5 V I_{OH} = - 1.32 mA V_{IL} See below
V_{OL}	Output Low Voltage		0.4		0.2	0.4	0.4	V	V_{CC} = 5.5 V I_{OL} = 17.6 mA V_{IH} = 5.5 V V_{CC} = 4.5 V I_{OL} = 13.6 mA V_{IH} See below
V_{IH}	Input High Voltage	2		1.7			1.4	V	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8			0.9	0.8	V	Guaranteed input low threshold for all inputs
I_F	Input Load Current T105 (non exp. section)and T115 T105 (exp. section) T106 and T108		-1.6 -2.4		-1.1 -1.5	-1.6 -2.4	-1.6 -2.4	mA	V_{CC} = 5.5 V V_F = 0.4V 5.5 V on other inputs
I_R	Input Leakage Current T105 (non exp. section) and T115 T105 (exp. section) T106 and T108				5 7.5	60 90	60 90	µA	V_R = 4.5 V V_{CC} = 5.5 V Gnd on all other inputs
I_{PD}	Power Dissipation Current T105 T115 T108		17.8 13 12.5		12.1 9.5 9.3	17.8 13 12.5	17.8 13 12.5	mA	V_{CC} = 5 V All inputs open
ΔI_{PD}	Extra Current Drain when one T106 expander is attached to a T105 "ON"		1.61		1.08	1.61	1.61	mA	V_{CC} = 5 V all inputs high
I_{SC}	Output Short Circuit Current	-30	-100	-30		-100	-30 -100	mA	V_{CC} = 5.5 V Inputs and output grounded
t_{pd+}	Turn off delay			4		12		nsec	T105 (non expandable section) and T115 V_{CC} = 5 V C_L = 15 pF See test circuit
t_{pd-}	Turn on delay			3		14		nsec	
t_{pd+}	Turn off delay			3		15		nsec	T105 (exp. section) and T108 V_{CC} = 5V C_L = 15 pF See test circuit
t_{pd-}	Turn on delay			3		12		nsec	
Δt_{pd+}	Turn off delay			-1		4		nsec	T106 only - the T106 is tested by measuring its t_{pd} through the T105 - see test circuit
Δt_{pd-}	Turn on delay			-1		4		nsec	

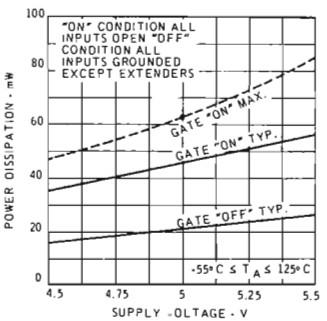
Note : 1) Output characteristics above apply to T105 - T115 and T108

2) Input characteristics above apply to T105, T115 and T108 using either the internal gates or an external T106 extender

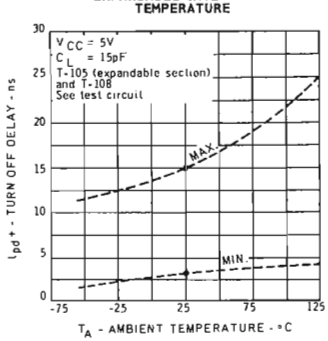
WORST CASE POWER DISSIPATIDN OF T 105 VERSUS SUPPLY VOLTAGE (per gate)



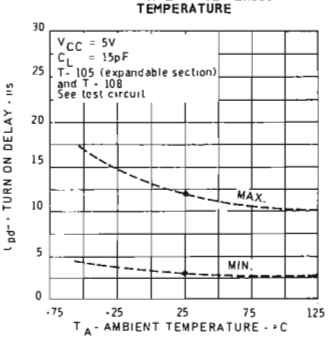
WORST CASE POWER DISSIPATION OF T 108 VERSUS SUPPLY VOLTAGE



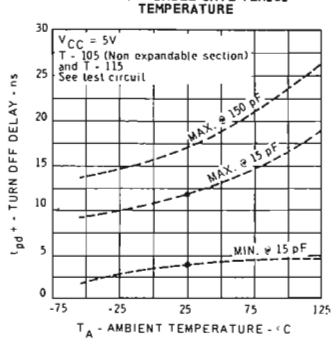
WORST CASE TURN OFF DELAY OF EXPANDABLE GATE VERSUS TEMPERATURE



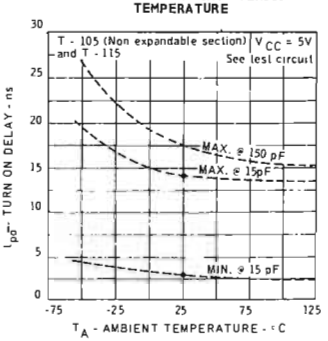
WORST CASE TURN ON DELAY OF EXPANDABLE GATE VERSUS TEMPERATURE



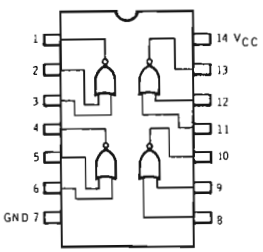
WORST CASE TURN OFF DELAY OF NONEXPANDABLE GATE VERSUS TEMPERATURE



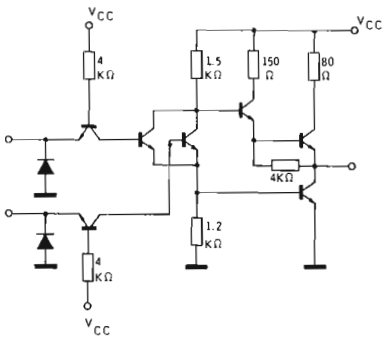
WORST CASE TURN ON DELAY OF NONEXPANDABLE GATE VERSUS TEMPERATURE



CONNECTION DIAGRAM
(Top view)



SCHEMATIC DIAGRAM
(one gate only)



ELECTRICAL CHARACTERISTICS (T_A = - 55°C to 125°C, V_{CC} = 5 V ± 10%)

SYMBOL	CHARACTERISTICS	LIMITS							UNIT	CONDITIONS AND COMMENTS
		- 55°		25°C			125°C			
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.		
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		V	V_{CC} = 4.5 V I_{OH} = - 1.32 mA V_{IL} = value indicated below
V_{OL}	Output Low Voltage		0.4		0.21	0.4		0.4	V	V_{CC} = 5.5 V I_{OL} = 17.6 mA V_{CC} = 4.5 V I_{OL} = 13.6 mA V_{IH} = value indicated below
V_{IH}	Input High Voltage	2		1.7			1.4		V	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8			0.9		0.8	V	Guaranteed input low threshold for all inputs
I_F	Input Load Current		-1.6			-1.6		-1.6	mA	V_{CC} = 5.5 V V_F = 0.4 V 5.5 V on other input
I_R	Input Leakage Current				10	60		60	μA	V_{CC} = 5.5 V V_R = 4.5 V
I_{SC}	Output Short Circuit Current	-30	-100	-30		-100	-30	-100	mA	V_{CC} = 5.5 V inputs and output grounded
I_{PD}	Power Dissipation Current (each gate)		5.5		3.5	5.5		5.5	mA	V_{CC} = 5 V inputs open
t_{pd+} t_{pd-}	Turn-Off Delay Turn-On Delay					10 12			nsec	V_{CC} = 5 V C_L = 15 pF see test circuit

GENERAL DESCRIPTION

The TTL family includes the T100 and T101 flip-flops to satisfy the storage element needs of a logic system. Each is a master-slave JK flip-flop with the same multi-emitter inputs and low impedance active pull-up outputs common to the gate elements.

The internal JK connections assure the user of non-ambiguous operation for all input states. The master-slave design with buffered clock input offers high noise immunity, low clock loading and eliminates the need for careful control of clock pulse rise or fall times. Data is accepted by the master when the clock is in the low logic state. Transfer from master to slave occurs when the clock goes from the low to the high logic level. When the clock is in the high logic level both J and K inputs are inhibited. For this reason it is desirable to maintain the clock pulse in the high level most of the duty cycle. Direct set and reset inputs provide true asynchronous control of both master and slave flip-flops independent of logic and clock input levels.

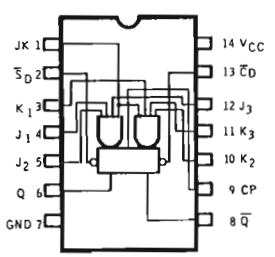
A common J-K input is provided which is useful in the physical layout of most logic configurations.

The two circuits are almost identical. The T100 has capacitors at the outputs of the J and Kdata input gates in the master flip-flop. The capacitors serve to lengthen the time requirements between J or K data and the low to-high clock transition. This feature makes the T100 particularly attractive for applications where clock shew is an important consideration.

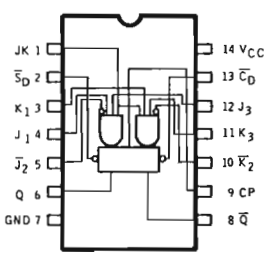
The T101 provides one $\overline{J}$ and one $\overline{K}$ input for additional logic flexibility. It has no master flip-flop capacitors to extend the set-up time and therefore has a higher toggling rate.

The important characteristics of the two flip-flops are illustrated in the following curves and specifications. Noise immunity and operating level curves shown in the gate section of the data sheet are applicable to the flip-flops as well.

CONNECTION DIAGRAMS
(top view)



T 100



T 101

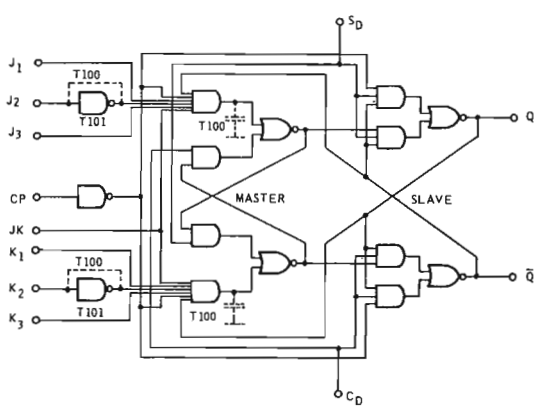
TRUTH TABLES

SYNCHRONOUS ENTRY J - K MODE OPERATION									ASYNCHRONOUS ENTRY Independent of Clock and Synchronous Input			
INPUTS @ t_n							OUTPUTS @ $t_n + 1$		INPUTS		OUTPUTS	
		(5)			(5)							
JK	J_1	J_2	J_3	K_1	K_2	K_3	Q	$\overline{Q}$	S_D	C_D	Q	$\overline{Q}$
1	4	5	12	3	10	11	6	8	2	13	6	8
L		X			X		No Change (4)					
H		L			L		No Change (4)		L	L	H	H
H		L			H		L	H	L	H	H	L
H		H			L		H	L	H	L	L	H
H		H			H		Toggles		H	H	No Change	

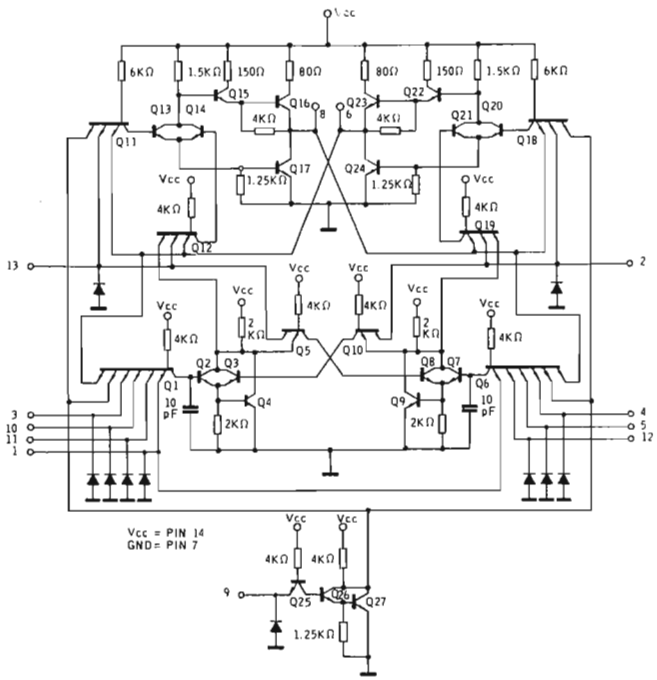
NOTES :

1) H = Most positive logic level.
2) L = Most negative voltage level.
3) X = Could be high or low.
4) For no change of outputs, the J and K inputs of the common JK input must remain low from the time the clock goes low to the time the clock goes high again.
5) The T101 has inverted J_2 (Pin 5) and K_2 (Pin 10) inputs. When not in use, they must be grounded.
6) The L symbol in the J and K input column is defined as meaning that the input does not go high at any time while the clock is low. The H symbol in the J and K input column is defined as meaning that the input has been high at same time while the clock was low.

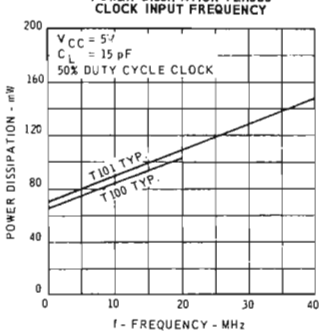
T100 AND T101 FUNCTIONAL LOGIC DIAGRAM



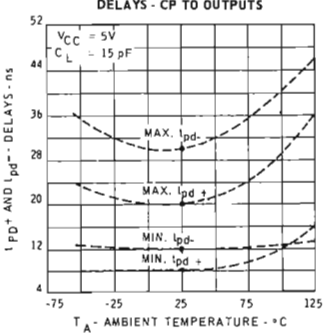
T 100 SCHEMATIC DIAGRAM



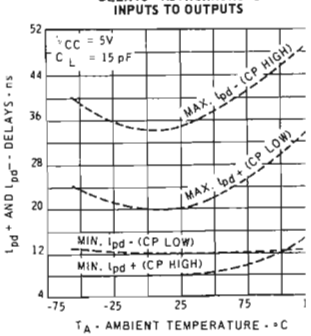
POWER DISSIPATION VERSUS CLOCK INPUT FREQUENCY



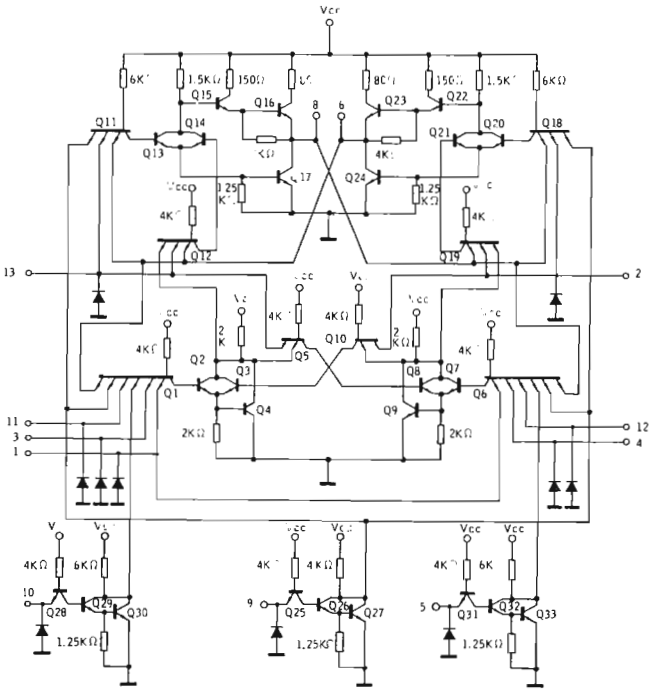
WORST CASE MAX. & MIN. $t_{pd}+$ & $t_{pd}-$ PROPAGATION DELAYS - CP TO OUTPUTS



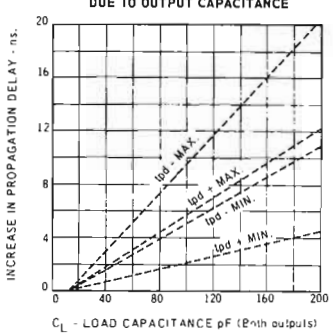
WORST CASE MAX. & MIN. $t_{pd}+$ & $t_{pd}-$ PROPAGATION DELAYS - ASYNCHRONOUS INPUTS TO OUTPUTS



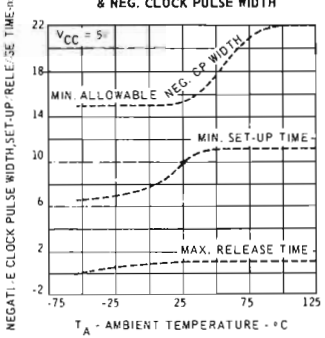
T 101 SCHEMATIC DIAGRAM



INCREASE IN ASYNCHRONOUS OR CLOCK INPUT t_{pd} - AND t_{pd}+ DUE TO OUTPUT CAPACITANCE



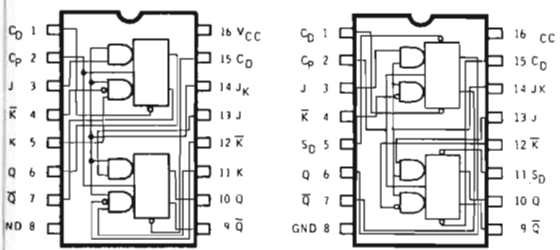
WORST CASE SET UP/RELEASE TIME & NEG. CLOCK PULSE WIDTH



ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V ±10%)

SYMBOL	CHARACTERISTICS	LIMITS -55°C Min.	LIMITS -55°C Max.	LIMITS 25°C Min.	LIMITS 25°C Typ.	LIMITS 25°C Max.	LIMITS 125°C Min.	LIMITS 125°C Max.	UNIT	CONDITIONS AND COMMENTS
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		V	V_{CC} = 4.5 V, I_{OH} = -1.2 mA V_{IL} on asynchronous input
V_{OL}	Output Low Voltage		0.4		0.21	0.4		0.4	V	V_{CC} = 4.5 V I_{OL} = 12.4 mA V_{IH} on asynchronous input V_{CC} = 5.5 V I_{OL} = 16 mA V_{IH} = 5.5 V on asynchronous input
V_{IH}	Input High Voltage	2		1.7			1.4		V	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8			0.9		0.8	V	Guaranteed input low threshold for all inputs
I_R	Input Leakage Current									
	J, K, $\overline{J}$, $\overline{K}$ & Clock Inputs				5	60		60	µA	V_{CC} = 5.5 V V_R = 4.5 V
	J - K Input				10	120		120		Gnd on other inputs
	Asynchronous input				14	162		162		
I_F	Input Load Current									
	J, K, $\overline{J}$, $\overline{K}$ & Clock inputs		-1.6		-1	-1.6		-1.6	mA	V_{CC} = 5.5V V_F = 0.4V
	J - K Inputs		-3.2		-2	-3.2		-3.2		5.5 V on other
	Asynchronous input		-4.32		-2.7	-4.32		-4.32		inputs
I_{PD}	Power Dissipation Current (each flip-flop)									
	T100		23		13	23		23	mA	V_{CC} = 5 V S_D at ground
	T101		28		14	28		28		
I_{SC}	Output Short Circuit Current	-30	-100	-30		-100	-30	-100	mA	V_{CC} = 5.5 V ground on output and asynchronous input
t_{pd+}	Turn-off delay			8	12	20			nsec	
t_{pd-}	Turn-on delay			12	20	30			nsec	
$t_{release}$	T100			10	18				nsec	
	T101			1	7					V_{CC} = 5 V
t set-up	T100				22	30			nsec	C_L = 15 pF
	T101				8	10				see test circuits and curves
	Negative clock pulse width									
	T100				25				nsec	
	T101				10					
	Toggle frequency									
	T100				20				MHz	
	T101				50					

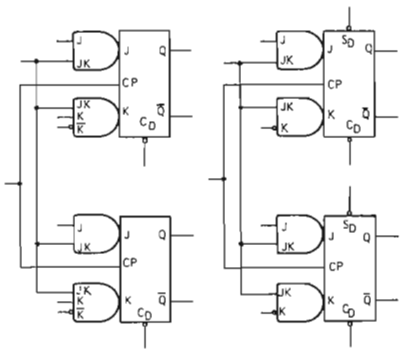
CONNECTION DIAGRAMS
(top view)



T 120 T 121

Available in Dip only

FUNCTIONAL LOGIC DIAGRAMS



T 120 T 121

TRUTH TABLE

SYNCHRONOUS ENTRY J-K MODE OPERATION

T120 INPUTS @ t_n			T121 INPUTS @ t_n			OUTPUTS @ t_n + 1	
JK	J	K - K̄	JK	J	K̄	Q	Q̄
14	3(13)	5(11)-4(12)	14	3(13)	4(12)	6(10)	7(9)
L	X	X	L	X	X	No Change	(1)
H	L	L	H	L	H	No Change	(1)
H	L	H	H	L	L	L	H
H	H	L	H	H	H	H	L
H	H	H	H	H	L	Toggles	

ASYNCHRONOUS ENTRY INDEPENDENT OF CLOCK & SYNCHRONOUS INPUTS

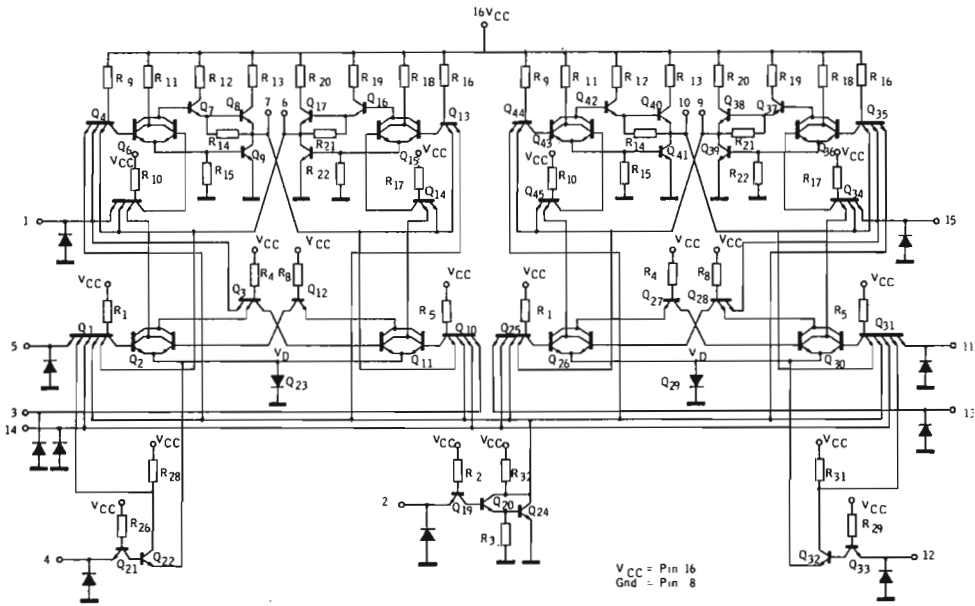
T120 INPUTS	T121 INPUTS		OUTPUTS	
C_D	S_D	C_D	Q	Q̄
1(15)	5(11)	1(15)	6(10)	7 (9)
L	H	L	L	H
H	H	H	No Change	
	L	L	H	H
	L	H	H	L

H = Most positive logic level
L = Most negative logic level
X = Could be high or low

NOTES :

1) K̄ inputs should be grounded when not in use.
2) The L symbol in the J and K input column is defined as meaning that the input does not go high at any time while the clock is low. The H symbol in the J and K input column is defined as meaning that the input has been high at same time while the clock was low.

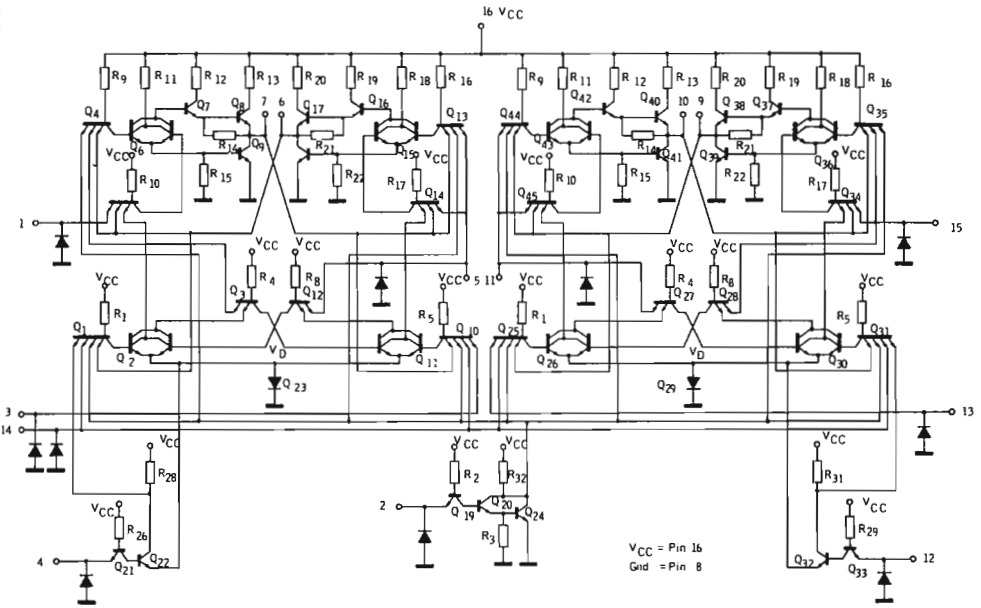
T 120 SCHEMATIC DIAGRAM



NOMINAL COMPONENT VALUES

R_1, R_4, R_5, R_8, R_{10}, R_{14}, R_{17}, R_{21}, R_{22}, R_{23}, R_{24}, R_{26}, R_{29} = 4 KΩ
R_2, R_3, R_6, R_7 = 2 KΩ
R_9, R_{16}, R_{28}, R_{31} = 6 KΩ
R_{11}, R_{18} = 1.5 KΩ
R_{12}, R_{19} = 150Ω
R_{13}, R_{20} = 80Ω
R_{15}, R_{22}, R_{25}, R_{27}, R_{30} = 1.25 KΩ
R_{32} = 1 KΩ
C_1, C_2 = 10 pF

T 121 SCHEMATIC DIAGRAM



NOMINAL COMPONENT VALUES

R_1, R_4, R_5, R_8, R_{10}, R_{14}, R_{17}, R_{21}, R_{22}, R_{23}, R_{24}, R_{26}, R_{29} = 4 KΩ
R_2, R_3, R_6, R_7 = 2 KΩ
R_9, R_{16}, R_{28}, R_{31} = 6 KΩ
R_{11}, R_{18} = 1.5 KΩ
R_{12}, R_{19} = 150Ω
R_{13}, R_{20} = 80Ω
R_{15}, R_{22}, R_{25}, R_{27}, R_{30} = 1.25 KΩ
R_{32} = 1 KΩ
C_1, C_2 = 10 pF

ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V ±10%)

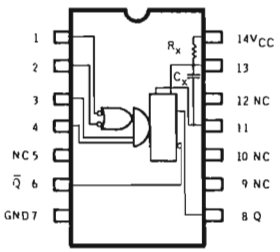
SYMBOL	CHARACTERISTICS	LIMITS -55°C Min.	LIMITS -55°C Max.	LIMITS 25°C Min.	LIMITS 25°C Typ.	LIMITS 25°C Max.	LIMITS 125°C Min.	LIMITS 125°C Max.	UNIT	CONDITIONS AND COMMENTS
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		V	V_{CC} = 4.5 V I_{OH} = - 1.2 mA V_{IL} on asynchronous input
V_{OL}	Output Low Voltage		0.4		0.21	0.4		0.4	V	V_{CC} = 4.5 V I_{OL} = 12.4 mA V_{IH} on asynchronous input V_{CC} = 5.5 V I_{OL} = 16 mA V_{IH} = 5.5 V on asynchronous input
V_{IH}	Input High Voltage	2		1.7			1.4		V	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8			0.9		0.8	V	Guaranteed input low threshold for all inputs
I_R	Input Leakage Current									
	J, K and $\overline{R}$ inputs				5	60		60	µA	V_{CC} = 5.5 V
	Clock input				10	120		120		V_R = 4.5 V
	JK input				20	240		240		Ground on other inputs
	Asynchronous inputs				14	160		160		
I_F	Input Load Current									
	J, K and $\overline{R}$ inputs		-1.6		-1.1	-1.6		-1.6	mA	V_{CC} = 5.5 V
	Clock input		-3.2		-2.2	-3.2		-3.2		V_F = 0.4 V
	JK input		-6.4		-4.4	-6.4		-6.4		5.5 V on other inputs
	Asynchronous inputs		-4.32		- 3	-4.32		-4.32		
I_{PD}	Power Dissipation Current (each flip-flop)		27		14	27		27	mA	V_{CC} = 5 V C_D at ground
I_{SC}	Output Short Circuit Current	-30	- 100	-30		- 100	-30	-100	mA	V_{CC} = 5.5 V ground on output and asynchronous input
t_{pd+}	Turn-off delay			8	13	22			nsec	V_{CC} = 5 V C_L = 15 pF see test circuits
t_{pd-}	Turn-on delay			12	21	32			nsec	
t release				1	7				nsec	
t set- up					8	16			nsec	
	Negative Clock Pulse Width				10				nsec	
	Toggle frequency				50				MHz	

EXTENDED TEMPERATURE RANGE

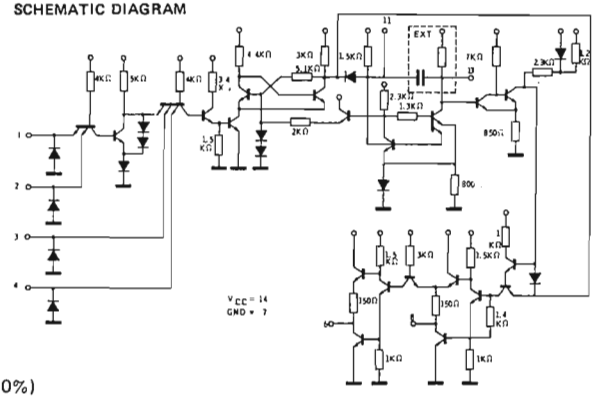
GENERAL DESCRIPTION

This retriggerable monostable multivibrator (or one-shot) provides an output pulse with high accuracy and a very wide duration range (50 nsec to ∞). The T118 will respond to trigger inputs even when already in its active timing state, and will time itself out from the last input pulse received.

CONNECTION DIAGRAM
(top view)



SCHEMATIC DIAGRAM



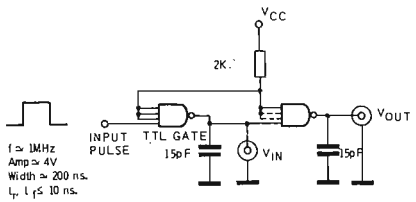
ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%)

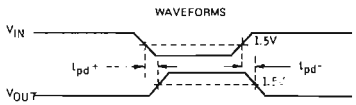
SYMBOL	CHARACTERISTICS	LIMITS -55°C Min.	LIMITS -55°C Max.	LIMITS 25°C Min.	LIMITS 25°C Typ.	LIMITS 25°C Max.	LIMITS 125°C Min.	LIMITS 125°C Max.	UNIT	CONDITIONS AND COMMENTS
V_{OH}	Output High Voltage	2.4		2.4	3.3		2.4		V	V_{CC} = 4.5 V I_{OH} = -1 mA for pin 6 open pin 11 for pin 8 ground pin 11
V_{OL}	Output Low Voltage		0.4		0.2	0.4		0.4	V	V_{CC} = 4.5 V I_{OL} = 10 mA for pin 6 open pin 11 for pin 8 ground pin 11
V_{IH}	Input High Voltage	2		2	1.7				V	V_{CC} = 4.5 V minimum pulse width 40 nsec
V_{IL}	Input Low Voltage				1.4	0.85		0.85	V	V_{CC} = 5.5 V minimum pulse width 40 nsec
I_F	Input Load Current		-1.6		-1.1	-1.6		-1.6	mA	V_{CC} = 5.5 V V_F = 0.4 V 4.5V on other input
I_R	Input Leakage Current				15	60		60	µA	V_{CC} = 5.5 V V_R = 4.5 V ground on other input
I_{PD}	Power Dissipation Current		25			25		25	mA	V_{CC} = 5.5 V ground on true inputs and 4.5V on complemented inputs
t_{pd+}	Negative trigger input to Q output				25	50			nsec	V_{CC} = 5V R_X = 5 KΩ C_X = 0 C_L = 15 pF see test circuit
t_{pd-}	Negative trigger input to $\bar{Q}$ output				25	50			nsec	
t_{pw}	Min Q output pulse width (1)				45	65			nsec	
C_{stray}	Max. allowable Wiring Cap (pin 13)		50			50		50	pF	Gnd on pin 13 This capacitance, if present, will add to C_X in determining output pulse width
R_X	Timing Resistor (2)	5	20	5		20	5	20	KΩ	

Notes : 1) Pulse width calculation : Tpw = 0.36 R_X C_X.
2) Unless otherwise noted, 10 KΩ resistor (R_X) is placed between Pin 13 and V_{CC} for all tests.

SWITCHING TIME TEST CIRCUITS

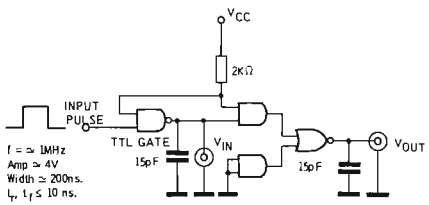
T102 - T103 - T104 - T107 - T109 - T116 t_{pd} TEST CIRCUIT

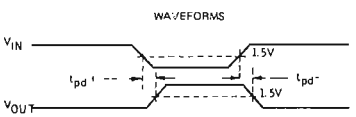




NOTE Capacitance includes probe and jig capacity

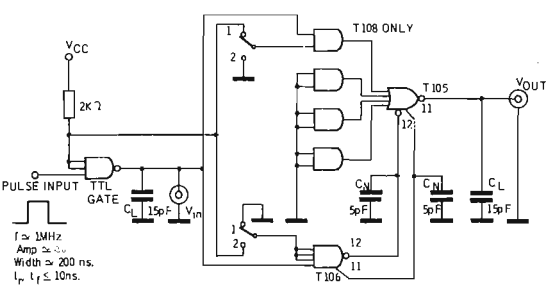
t_{pd} TEST CIRCUIT T105-T115 NONEXPANDABLE SECTION ONLY





NOTE Capacitance includes probe and jig capacity

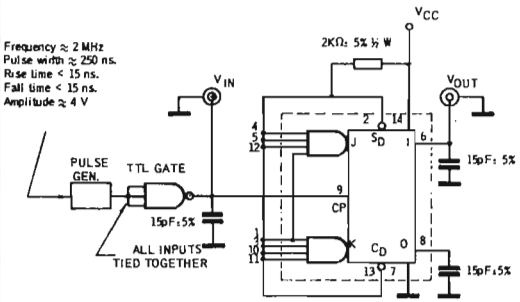
t_{pd} TEST CIRCUIT T105-T108 EXPANDABLE GATE AND T106 EXPANDER

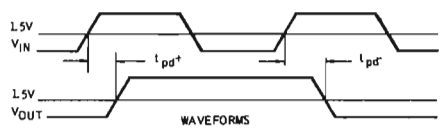


NOTE
With switch in position 1 measure t_{pd} of T105 - With switch in position 2 measure t_{pd} (T105 - T108) + t_{pd} (T106). Capacitance includes probe and jig capacitances.

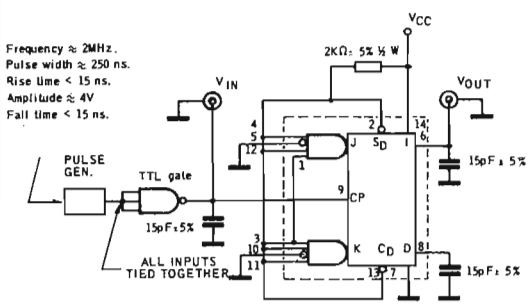
SWITCHING TIME TEST CIRCUITS

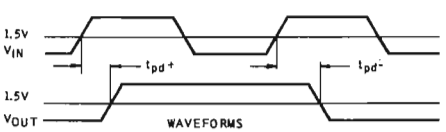
T100 t_{pd} TEST CIRCUIT





T101 t_{pd} TEST CIRCUIT





SWITCHING NOTES

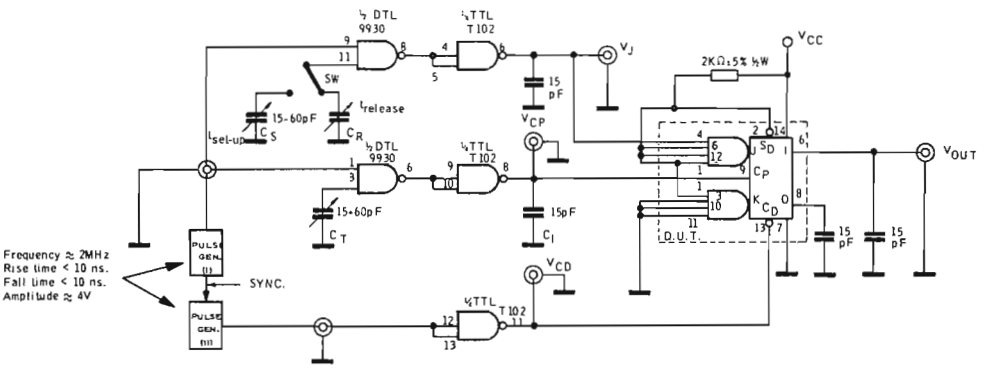
1) The load capacitance indicated in test circuits includes the capacitance of probe and jig.

2) Sensitivity of all switching parameters to supply voltage change (within range of 5 V ± 10%) and D.C. loading is very small.

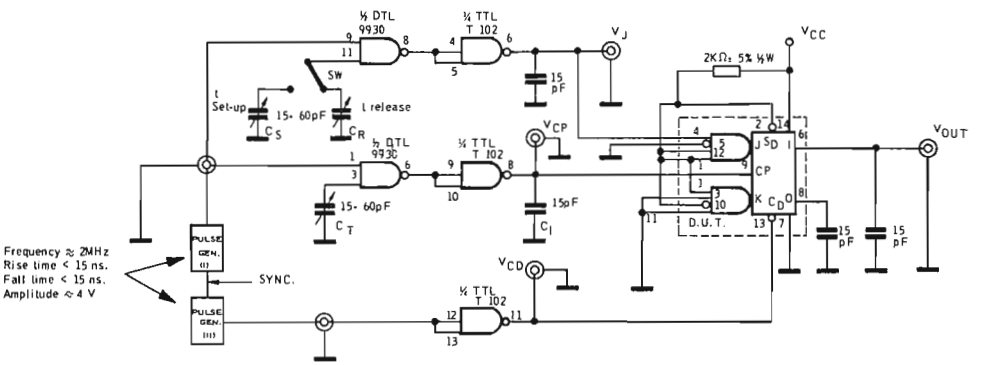
3) Allowable clock skew ≤ t_{pd} + (max) + $t_{release}$ (min.).

SWITCHING TIME TEST CIRCUITS

T100 t_{set-up} and $t_{release}$ TEST CIRCUIT



T101 t_{set-up} and $t_{release}$ TEST CIRCUIT

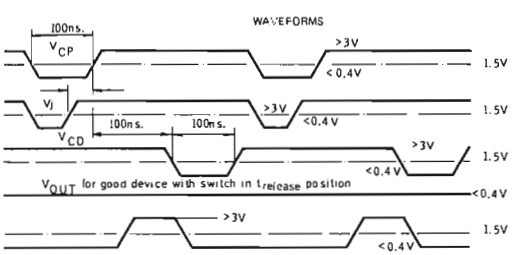


INITIAL ADJUSTMENT

1. With switch in t release position adjust pulse generators, C_T & C_R for proper V_{CP}, V_J & V_D waveforms and t release limit value.
2. With switch in t set-up position adjust C_S for t set-up limit value.

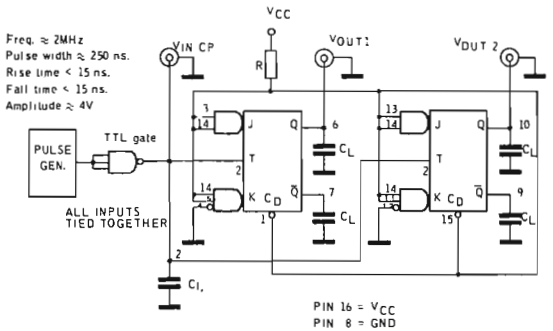
t set-up is defined as the minimum time required for a High to be present at a synchronous logic input at any time during the low state of the clock in order for the flip-flop to respond to the data.

t release is defined as the maximum time allowed for a High to be present at a synchronous logic input at any time during the low state of the clock and not be recognized.

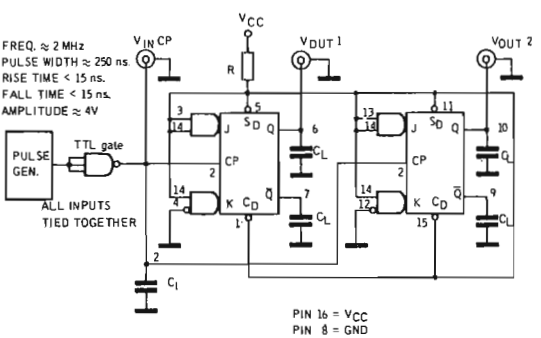


SWITCHING TIME TEST CIRCUITS

T120 t_{pd} TEST CIRCUIT



T121 t_{pd} TEST CIRCUIT

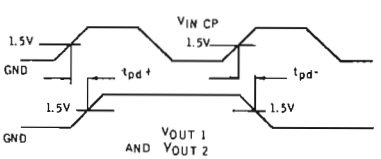


R = 2KΩ, ± 5%, 1/2W
C_I = 15 pF ± 5%
C_L = 15 pF ± 5%

C_I & CL include all probe and jig capacity. Very short stranded or printed wire should be used for all interconnections.
Probes should be connected directly to the input & output pins.

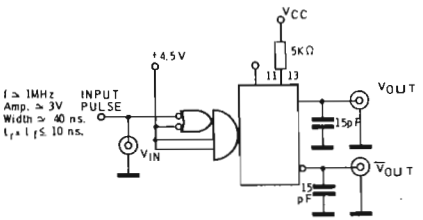
NOTE :
For $t_{set\text{-}up}$ and $t_{release}$ see T 100 and T 101 test circuits.

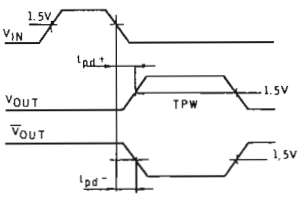
WAVEFORMS



SWITCHING TIME TEST CIRCUITS

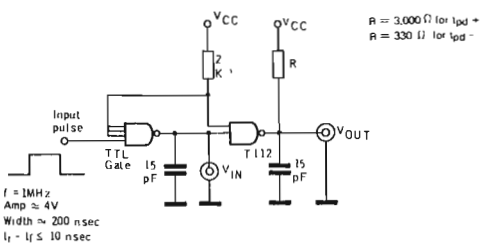
T118 t_{pd} TEST CIRCUIT



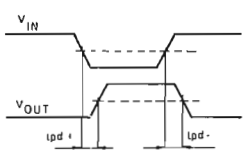


Note: Capacitance includes jig and probe capacity.

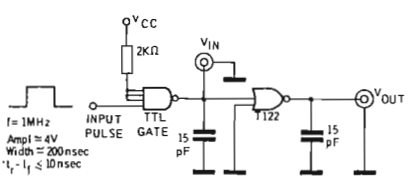
T112 t_{pd} TEST CIRCUIT

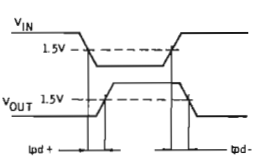


Note : capacitance includes probe and jig capacity.



T122 t_{pd} TEST CIRCUIT





NOTE: Capacitance includes probe and jig capacity.

Transistor-transistor logic

STANDARD TEMPERATURE RANGE, 0°C to 75°C

- COMPATIBLE WITH DTL AND LPDTL PRODUCTS
- INPUT DIODE CLAMPING
- NOISE IMMUNITY, 1 V
- WORST CASE NOISE IMMUNITY, 0.4 V
- OUTPUT DRIVE CAPABILITY OF 10
- POWER DISSIPATION, 11 mW PER GATE
- GATE PROPAGATION DELAY OF 6 nsec
- ACTIVE PULL UP OUTPUT CIRCUIT
- SAME PIN CONFIGURATION AS THE CORRESPONDING DTL AND LPDTL PRODUCTS

ORDERING NUMBERS

TXXXD1 for ceramic DIP
TXXXB1 for plastic DIP
TXXXF1 for flat package
(xxx is type number)

The Transistor - Transistor Logic integrated circuit family (TTL) combines a high fan-out, high noise immunity, low power dissipation and good capacitive load driving capability with low propagation delay times.
The circuits are fabricated within a silicon monolithic substrate using planar epitaxial processes.
These devices are available in the following packages: ceramic DIP (14 or 16 leads), plastic DIP (14 or 16 leads), flat ceramic package.

ABSOLUTE MAXIMUM RATINGS
(above which the useful life may be impaired)

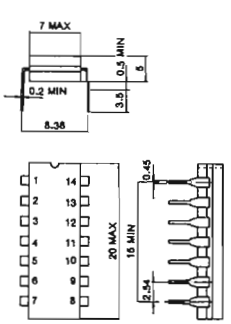
V_{CC} Pin Potential to Ground	-0.5V to 8V
Input Voltage (see note 1)	-0.5V to 5.5V
Gate Output Voltage, Inputs Low	-0.5V to V_{CC}
Gate Current into Output Terminal, Inputs High (except T109)	50 mA
Gate Current into Output Terminal, Inputs High T109	100 mA
Flip-Flop Output Voltage when Output is normally High	-0.5V to V_{CC}
Flip-Flop Current into Output Terminal when Output is normally Low	50 mA
Storage Temperature, Plastic	-55°C to 125°C
Storage Temperature, Ceramic	-65°C to 150°C
Temperature (Amb.) Under Bias, Ceramic	-55°C to 125°C

OPERATING CONDITIONS

Temperature Range	0°C to 75°C
Supply Voltage	5V ± 5%

Notes: see over

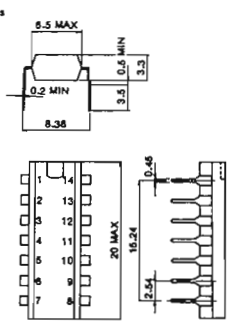
PHYSICAL DIMENSIONS
14 pin ceramic DIP



NOTE: all dimensions in mm.

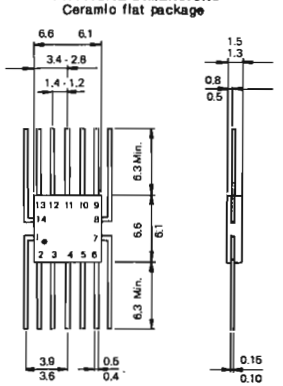
For 16 pin packages see next page.

PHYSICAL DIMENSIONS
14 pin plastic DIP



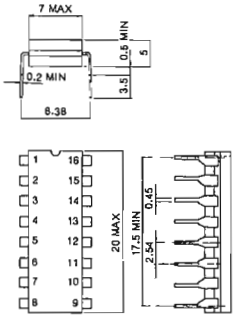
NOTE: all dimensions in mm.

PHYSICAL DIMENSIONS
Ceramic flat package



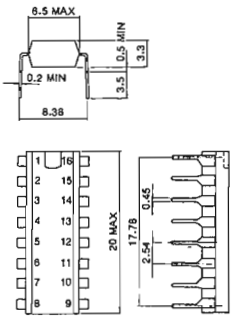
NOTE: all dimensions in mm.

PHYSICAL DIMENSIONS
16 pin ceramic DIP



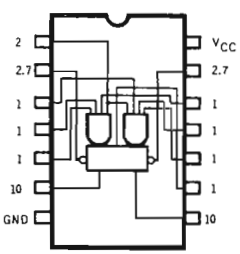
NOTE: all dimensions in mm.

PHYSICAL DIMENSIONS
16 pin plastic DIP

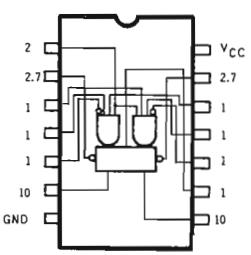


NOTE: all dimensions in mm.

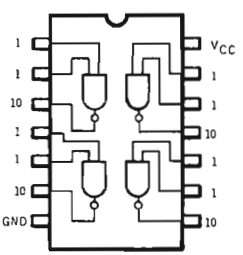
INPUT - OUTPUT LOAD/DRIVE FACTORS



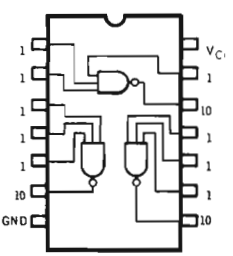
T 100



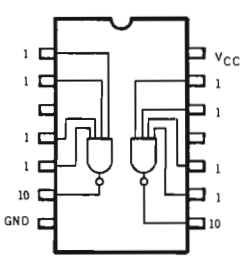
T 101



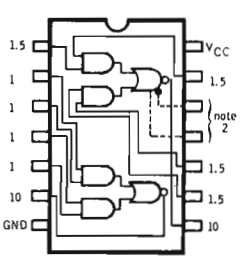
T 102



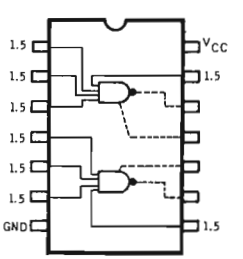
T 103



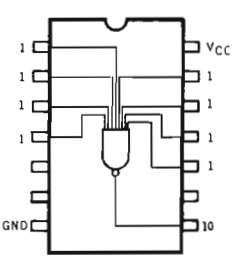
T 104



T 105

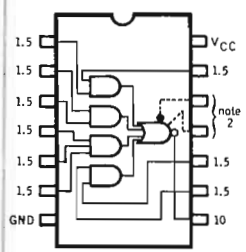


T 106

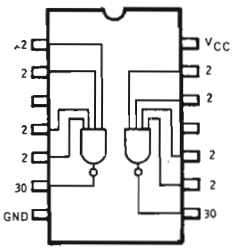


T 107

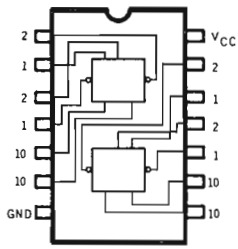
INPUT-OUTPUT LOAD/DRIVE FACTORS (contd.)



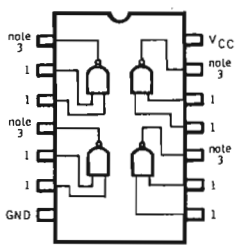
T 108



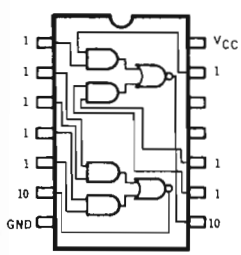
T 109



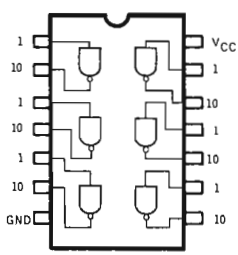
T 110



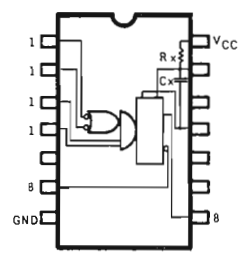
T 112



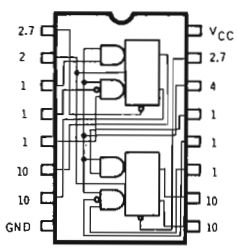
T 115



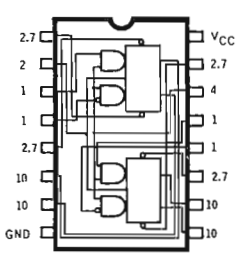
T 116



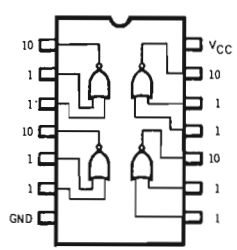
T 118



T 120



T 121

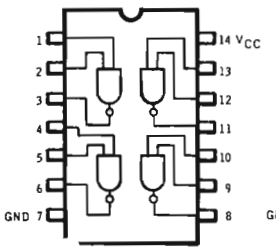


T 122

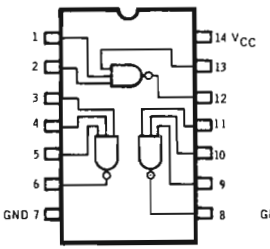
NOTES:

1) Because of the input clamp diodes, excess current can be drawn out of the inputs, if the DC input voltage is more negative than-0.5V. The diode is designed to clamp off large negative AC swings associated with fast fall times and long lines. This maximum rating is intended only to limit the steady state input voltage and current.
2) Four expanders (T106) may be tied to these terminals.
3) The number of elements driven by an output terminal depends on the resistance value externally connected between V_{CC} and output pin (see "WIRED-OR APPLICATIONS").

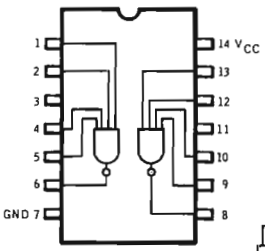
CONNECTION DIAGRAMS (top view)



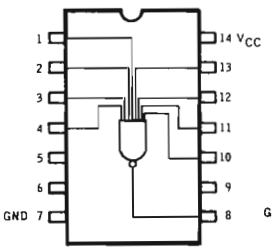
T 102



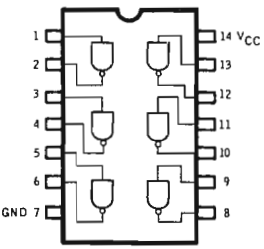
T 103



T 104

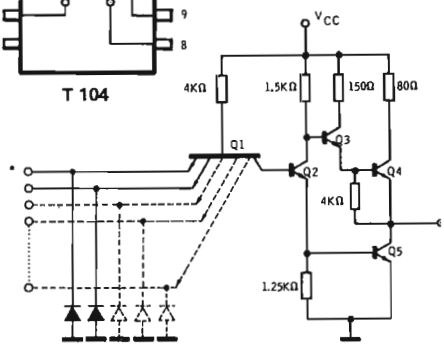


T 107



T 116

EQUIVALENT CIRCUIT
(one gate only)

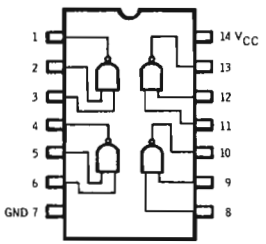


* Number of inputs depends on the gate

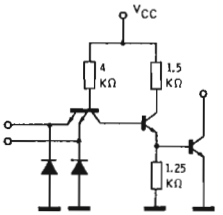
ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V ± 5%)

SYMBOL	CHARACTERISTICS	LIMITS 0°C Min.	0°C Max.	25°C Min.	25°C Typ.	25°C Max.	75°C Min.	75°C Max.	UNIT	CONDITIONS AND COMMENTS
V_{OH}	Output High Voltage	2.4		2.4	3.1		2.4		V	V_{CC} = 4.75V I_{OH} = -1.2 mA V_{IL} = value indicated below
V_{OL}	Output Low Voltage		0.45		0.21	0.45		0.45	V	V_{CC} = 5.25 V I_{OL} = 16 mA V_{CC} = 4.75 V I_{OL} = 14.1 mA V_{IH} = value indicated below
V_{IH}	Input High Voltage	1.9		1.8			1.6		V	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	V	Guaranteed input low threshold for all inputa
I_F	Input Load Current		-1.6		-1	-1.6		-1.6	mA	V_{CC} = 5.25 V V_F = 0.45 V V_R = 5.25 V on other inputa
I_R	Input Leakage Current				10	60		60	μA	V_{CC} = 5.25 V V_R = 4.5 V Gnd on other inputs.
I_{PD}	Power Dissipation Current (each gate)		6.1		3.6	6.1		6.1	mA	V_{CC} = 5 V inputs open
I_{SC}	Output Short-Circuit Current	-30	-120	-30		-120	-30	-120	mA	V_{CC} = 5.25 V inputs and output grounded
t_{pd+}	Turn-off Delay			3		13			nsec	V_{CC} = 5 V C_L = 15 pF See test circuit
t_{pd-}	Turn-on Delay			3		15			nsec	

CONNECTION DIAGRAM
(top view)



EQUIVALENT CIRCUIT
(one gate only)



ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V ± 5%)

SYMBOL	CHARACTERISTICS	LIMITS 0°C Min.	0°C Max.	25°C Min.	25°C Typ.	25°C Max.	75°C Min.	75°C Max.	UNIT	CONDITIONS AND COMMENTS
V_{OL}	Output Low Voltage		0.45		0.21	0.45		0.45	V	V_{CC} = 5.25V I_{OL} = 16 mA V_{IH} = value indicated below
V_{IH}	Input High Voltage	1.9		1.8			1.6		V	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	V	Guaranteed input low threshold for all inputs
I_F	Input Load Current		-1.6		-1	-1.6		-1.6	mA	V_{CC} = 5.25V V_F = 0.45V V_R = 5.25V on other input
I_R	Input Leakage Current				10	60		60	μA	V_{CC} = 5.25V V_R = 4.5V ground on other input
I_{CEX}	Output Leakage Current					200		200	μA	V_{CC} = 4.75V inputs guaranteed 4.5V applied to output
I_{PD}	Power Dissipation Current (each gate)		6.1		3.6	6.1		6.1	mA	V_{CC} = 5V inputs open
t_{pd+}	Turn-off Delay					35			nsec	V_{CC} = 5V
t_{pd-}	Turn-on Delay					15			nsec	C_L = 15 pF see test circuit

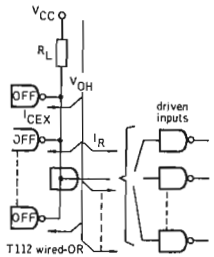
WIRED-OR APPLICATIONS

The T112 allows wired-OR operation when a proper load resistor (R_L) is connected between V_{CC} and output pins. Gen eral rules to calculate the allowed number of wired-OR gates with a requested drive factor are explained below.
For a given number (K) of wired-OR gates a given number (n) of driven gates, two equations can be written in order t determine the value of the external resistor (R_L) that guarantees a correct operation with respect to the same nois immunity levels as the TTL family.

High Level: if all the wired-OR gates outputs are at the high level, a total current flows from supply through the external resistor R_L, that is the sum of the output leakage current I_{CEX} of the output wired-OR transistor and the input leakage current I_R of the driven gates. This current takes the output voltage to a value that should not be less than the V_{OH} voltage that guarantees the high level noise immunity. Therefore, to limit this voltage drop, the following R_L limitation should be respected:

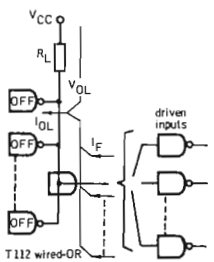
$$R_{Lmax} = \frac{V_{CC} - V_{OH}}{KI_{CEX} + n\, I_R}$$

note that the resulting R_L value is a worst case as I_{CEX} given in present data sheet is measured at 4.5V instead of 2.4V. Besides even I_R is measured at 4.5V.



Low Level: when almost one of the wired-OR gates is at the low level (ON), a current flow from supply, through R_L, to the output of the ON transistor. This current is the ratio of R_L and the allowed voltage drop, (the output leakage current of the OFF wired-OR gates is negligible). In addition, the output ON transistor sinks the output load current I_F of the driven inputs. The V_{OL} voltage guarantees the low level noise immunity, that is total sunk current should not overcome I_{OL} value; therefore, to limit the current through R_L, following limitation should be respected:

$$R_{Lmin} = \frac{V_{CC} - V_{OL}}{I_{OL} - n\, I_F}$$



If more than one gate is ON, allowed R_L value is higher.
The two combined equations give maximum and minimum values among which should range R_L value:

$$\frac{V_{CC}-V_{OL}}{I_{OL}-nI_F} \le R_L \le \frac{V_{CC}-V_{OH}}{KI_{CEX}+n\, I_R}$$

n = number of driven inputs

K = number of wired-OR T112 gates

DRIVING TTL LOADS

The adjoining table gives minimum and maximum resistance values to be used when one or more wired-OR T112s are driving TTL loads. When K (1 to 10) T112s are wired-OR and at the same time n TTL gates are driven, the resistance value to be externally connected to the output should be comprised between minimum and maximum given values. The table is calculated for the worst case of all the electrical parameters shown in the equations and the noise immunity of the TTL family is widely respected.

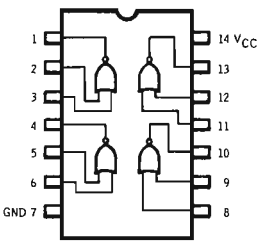
STANDARD TEMPERATURE RANGE (0°C to 75°C)

n	R_{min}	R_{max}									
		K=1	K=2	K=3	K=4	K=5	K=6	K=7	K=8	K=9	K=10
1	330	9040	5100	3560	2740	2220	1870	1610	1420	1260	1140
2	375	7340	4500	3260	2560	2100	1780	1500	1370	1220	1110
3	428	6180	4050	3010	2400	1990	1710	1490	1320	1190	1080
4	500	5340	3700	2800	2260	1900	1630	1430	1280	1150	1050
5	600	4700	3380	2610	2140	1810	1570	1380	1240	1120	1020
6	750	4200	3100	2450	2030	1730	1510	1340	1200	1090	995
7	1000	3790	2880	2300	1930	1650	1450	1290	1170	1060	X
8	1500	3460	2680	2180	1840	1590	X	X	X	X	X
9	3000	3180	X	X	X	X	X	X	X	X	X
10	∞	X	X	X	X	X	X	X	X	X	X

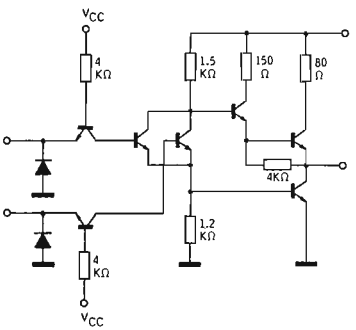
X means not allowed
n = number of driven TTL gates
K = number of T112s wired-OR

driven gate: I_F = 1.6 mA
I_R = 60 μA
V_{OH} = 2.4V

CONNECTION DIAGRAM
(top view)



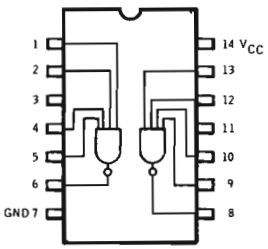
EQUIVALENT CIRCUIT
(one gate only)



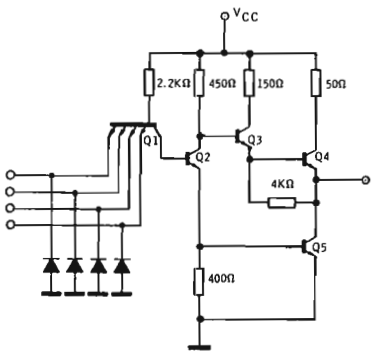
ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V ± 5%)

SYMBOL	CHARACTERISTICS	LIMITS 0°C Min.	0°C Max.	25°C Min.	25°C Typ.	25°C Max.	75°C Min.	75°C Max.	UNIT	CONDITIONS AND COMMENTS
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		V	V_{CC} = 4.75V I_{OH} = -1.2 mA V_{IL} = value indicated below
V_{OL}	Output Low Voltage		0.45		0.21	0.45		0.45	V	V_{CC} = 5.25V I_{OL} = 16 mA V_{CC} = 4.75V I_{OL} = 14.1 mA V_{IH} = value indicated below
V_{IH}	Input High Voltage	1.9		1.8			1.6		V	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	V	Guaranteed input low threshold for all inputs
I_F	Input Load Current		-1.6		-1	-1.6		-1.6	mA	V_{CC} = 5.25V V_F = 0.45V 5.25V on other inputs
I_R	Input Leakage Current				10	60		60	μA	V_{CC} = 5.25V V_R = 4.5V
I_{SC}	Output Short-Circuit Current	-30	-120	-30		-120	-30	-120	mA	V_{CC} = 5.25V inputs and output grounded
I_{PD}	Power Dissipation Current (each gate)		6.1		3.6	6.1		6.1	mA	V_{CC} = 5V inputs open
t_{pd+}	Turn-off Time					13			nsec	V_{CC} = 5V C_L = 15 pF see test circuit
t_{pd-}	Turn-on Time					15			nsec	

CONNECTION DIAGRAM
(top view)



EQUIVALENT CIRCUIT
(one gate only)



ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 5%)

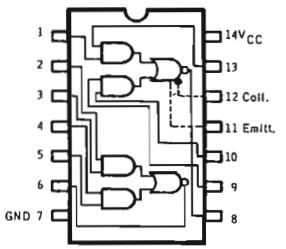
SYMBOL	CHARACTERISTICS	LIMITS 0°C Min.	LIMITS 0°C Max.	LIMITS 25°C Min.	LIMITS 25°C Typ.	LIMITS 25°C Max.	LIMITS 75°C Min.	LIMITS 75°C Max.	UNIT	CONDITIONS AND COMMENTS
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		V	V_{CC} = 4.75V I_{OH} = -3.6 mA V_{IL} = value indicated below
V_{OL}	Output Low Voltage		0.45		0.21	0.45		0.45	V	V_{CC} = 5.25V I_{OL} = 48 mA V_{CC} = 4.75V I_{OL} = 42.3 mA V_{IH} = value indicated below
V_{IH}	Input High Voltage	1.9		1.8			1.6		V	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	V	Guaranteed input low threshold for all inputs
I_F	Input Load Current		-3.2		-2	-3.2		-3.2	mA	V_{CC} = 5.25V V_F = 0.45V V_R = 5.25V on other inputs
I_R	Input Leakage Current				25	120		120	μA	V_{CC} = 5.25V V_R = 4.5V Gnd on other inputs
I_{PD}	Power Dissipation Current (each gate)		14		8.6	14		14	mA	V_{CC} = 5V open
I_{SC}	Output Short-Circuit Current	-40	-150	-40		-150	-40	-150	mA	V_{CC} = 5.25V inputs and output grounded
t_{pd+}	Turn-off Delay			3		17			nsec	V_{CC} = 5V C_L = 15 pF
t_{pd-}	Turn-on Delay			2		13			nsec	See test circuit

AND-NOR gates **T105 - T108 - T115**, expander **T106**

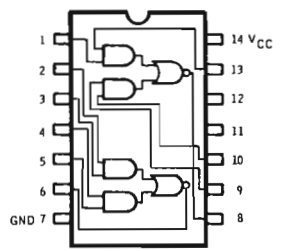
STANDARD TEMPERATURE RANGE

The TTL T105 and T108 are AND – NOR gates which may be NOR expanded with the use of the T106 element.

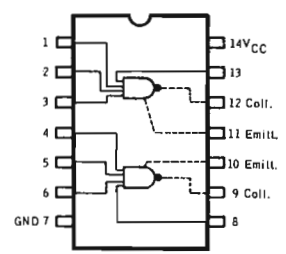
CONNECTION DIAGRAMS
(top view)



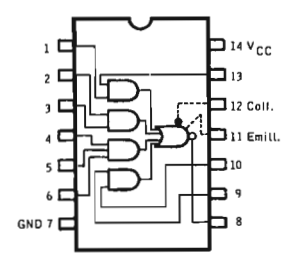
T 105



T 115

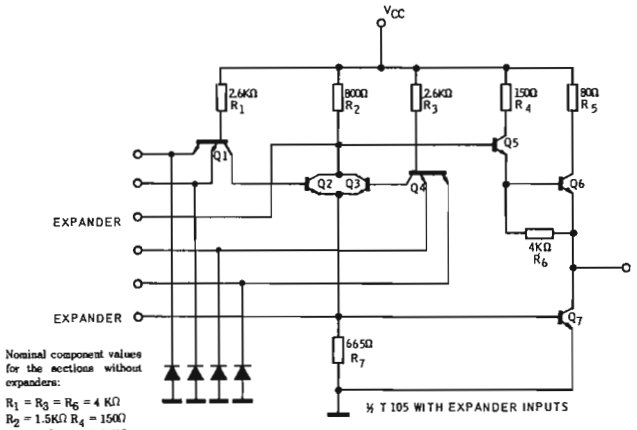


T 106



T 108

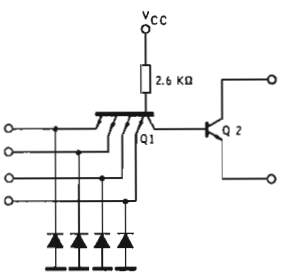
EQUIVALENT CIRCUITS



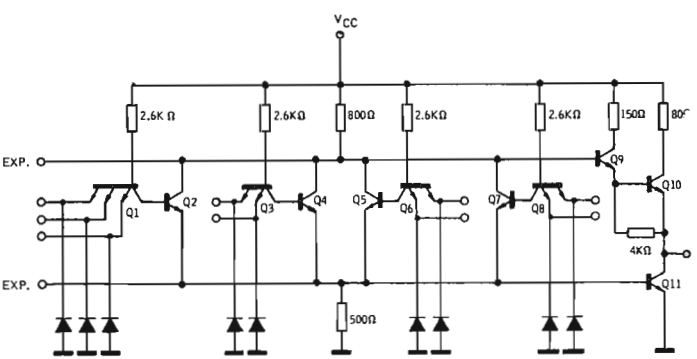
Nominal component values for the sections without expanders:

$R_1 = R_3 = R_6 = 4\ K\Omega$
$R_2 = 1.5K\Omega$ $R_4 = 150\Omega$
$R_5 = 80\Omega$ $R_7 = 1.25K\Omega$

T 105 - T 115



T 106 (one gate)



T 108

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 5%)

SYMBOL	CHARACTERISTICS	LIMITS						UNIT	CONDITIONS AND COMMENTS
		0°C		25°C			75°C		
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
V_{OH}	Output High Voltage	2.4		2.4	2.9		2.4		V	V_{CC} = 4.75V I_{OH} = -1.2 mA V_{IL} see below
V_{OL}	Output Low Voltage		0.45		0.2	0.45		0.45	V	V_{CC} = 5.25V I_{OL} = 16 mA V_{IH} = 5.25V V_{CC} = 4.75V I_{OL} = 14.1 mA V_{IH} see below
V_{IH}	Input High Voltage	1.9		1.8			1.6		V	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	V	Guaranteed input low threshold for all inputs
I_F	Input Load Current T105 (non exp.section) and T115 T105 (exp.section) T106 and T108		-1.6 -2.4		-1.04 -1.65	-1.6 -2.4		-1.6 -2.4	mA mA	V_{CC} = 5.25V V_F = 0.45V 5.25V on other inputs
I_R	Input Leakage Current T105 (non exp.section) and T115 T105 (exp.section) T106 and T108				5 15	60 90		60 90	μA μA	V_R = 4.5V V_{CC} = 5.25V Gnd on all other inputs
I_{PD}	Power Dissipation Current T105 T115 T108		21.3 15.4 17.7		12.1 9 9.3	21.3 15.4 17.7		21.3 15.4 17.7	mA mA mA	V_{CC} = 5V All inputs open
ΔI_{PD}	Extra Current Drain when one T106 expander is attached to a T105 "on"		2.05		1.08	2.05		2.05	mA	V_{CC} = 5V All inputs high
I_{SC}	Output Short-Circuit Current	-30	-120	-30		-120	-30	-120	mA	V_{CC} = 5.25V inputs and output grounded
t_{pd+}	Turn-off Delay			3		15			nsec	T105 (non expandable section) and T115
t_{pd-}	Turn-on Delay			3		15			nsec	V_{CC} = 5V C_L = 15pF see test circuit
t_{pd+}	Turn-off Delay			3		18			nsec	T105 (expandable section) and T108
t_{pd-}	Turn-on Delay			3		13			nsec	V_{CC} = 5V C_L = 15pF see test circuit
Δt_{pd+}	Turn-off Delay			-2		5			nsec	T106 only - The T106 is tested by measuring its t_{pd} through the T105 - see test circuit.
Δt_{pd-}	Turn-on Delay			-2		5			nsec	

GENERAL DESCRIPTION

The TTL family includes the T100 and T101 flip-flops to satisfy the storage element needs of a logic system. Each is a master-slave J-K flip-flop with the same multi-emitter inputs and low impedance active pull-up outputs common to the gate elements.

The internal J-K connections assure the user of non-ambiguous operation for all input states. The master-slave design with buffered clock input offers high noise immunity, low clock loading and eliminates the need for careful control of clock pulse rise or fall times. Data is accepted by the master when the clock is in the low logic state. Transfer from master to slave occurs when the clock goes from the low to the high logic level. When the clock is in the high logic level both J and K inputs are inhibited. For this reason it is desirable to maintain the clock pulse in the high level most of the duty cycle. Direct set and reset inputs provide true asynchronous control of both master and slave flip-flops independent of logic and clock input levels.

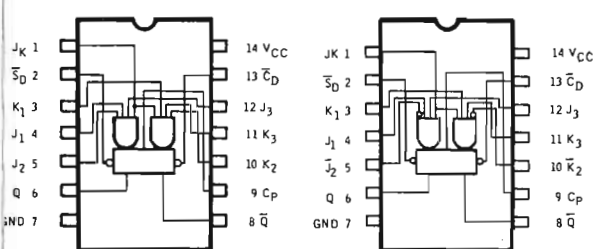
A common J-K input is provided which is useful in the physical layout of most logic configurations.

The two circuits are almost identical. The T100 has capacitors at the outputs of the J and K data input gates in the master flip-flop. The capacitors serve to lengthen the time requirements between J or K data and the low to high clock transition. This feature makes the T100 particularly attractive for applications where clock skew is an important consideration.

The T101 provides one $\overline{J}$ and one $\overline{K}$ input for additional logic flexibility. It has no master flip-flop capacitors to extend the set-up time and therefore has a higher toggling rate.

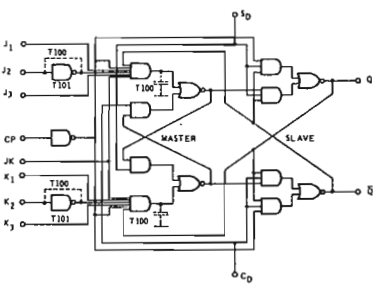
The important characteristics of the two flip-flops are illustrated in the following curves and specifications. Noise immunity and operating level curves shown in the gate section of the data sheet are applicable to the flip-flops as well.

CONNECTION DIAGRAMS
(top view)



T 100 T 101

FUNCTIONAL LOGIC DIAGRAM



TRUTH TABLES

SYNCHRONOUS ENTRY
J-K MODE OPERATION

INPUTS @ t_n							OUTPUTS @ t_{n+1}	
JK 1	J_1 4	J_2 5	J_3 12	K_1 3	$\overline{K}_2$ 10	K_3 11	Q 6	$\overline{Q}$ 8
L		X			X		No Change (note 4)	
H		L			L		No Change (note 4)	
H		L			H		L	H
H		H			L		H	L
H		H			H		Toggles	

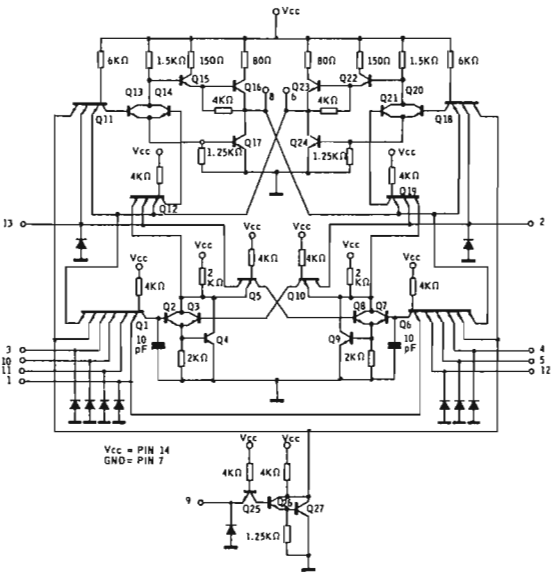
ASYNCHRONOUS ENTRY
Independent of Clock and Synchronous Input

INPUTS		OUTPUTS	
S_D 2	C_D 13	Q 6	$\overline{Q}$ 8
L	L	H	H
L	H	H	L
H	L	L	H
H	H	No Change	

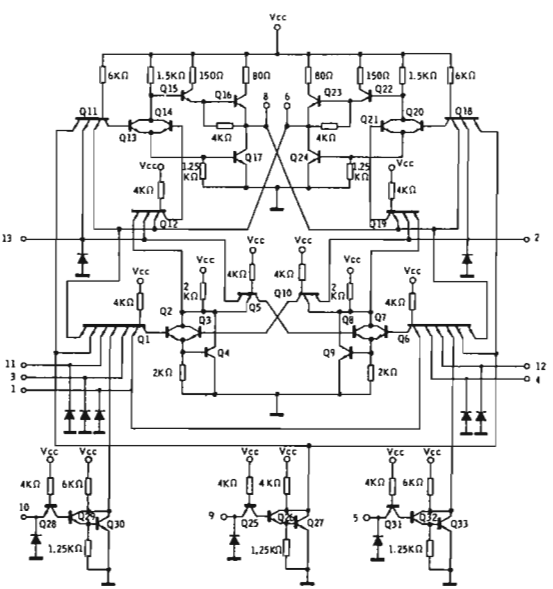
NOTES:

1) H = Most positive logic level.
2) L = Most negative voltage level.
3) X = Could be high or low.
4) For no change of outputs, the J and K inputs of the common J-K input must remain low from the time the clock goes low to the time the clock goes high again.
5) The T101 has inverted J2 (Pin 5) and K2 (Pin 10) inputs. When not in use, they must be grounded.
6) The L symbol in the J and K input column is defined as meaning that the input does not go high at any time while the clock is low. The H symbol in the J and K input column is defined as meaning that the input has been high at same time as the clock was low.

T100 EQUIVALENT CIRCUIT



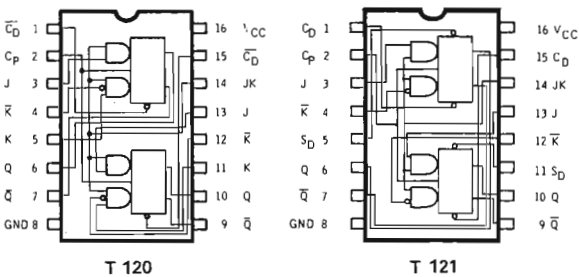
T101 EQUIVALENT CIRCUIT



ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V ± 5%)

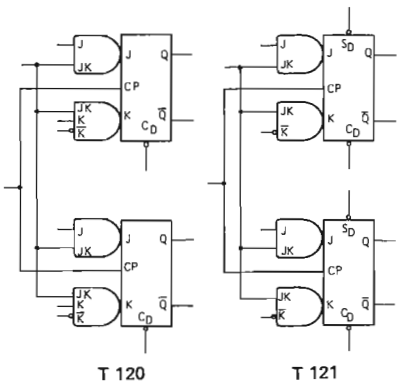
SYMBOL	CHARACTERISTICS	LIMITS 0°C Min.	0°C Max.	25°C Min.	25°C Typ.	25°C Max.	75°C Min.	75°C Max.	UNIT	CONDITIONS AND COMMENTS
V_{OH}	Output High Voltage	2.4		2.4	3		2.4		V	V_{CC} = 4.75V I_{OH} = -1.2 mA V_{IL} on asynchronous input
V_{OL}	Output Low Voltage		0.45		0.21	0.45		0.45	V	V_{CC} = 4.75V I_{OL} = 14.1 mA V_{IH} on asynchronous input V_{CC} = 5.25V I_{OL} = 16 mA V_{IH} = 5.25V on asynchronous input
V_{IH}	Input High Voltage	1.9		1.8			1.6		V	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	V	Guaranteed input low threshold for all inputs
I_R	Input Leakage Current J, K, $\overline{J}$, $\overline{K}$ & Clock Inputs J - K input Asynchronous Input				5 10 14	60 120 162		60 120 162	μA	V_{CC} = 5.25V V_R = 4.5V Gnd on other inputs
I_F	Input Load Current J, K, $\overline{J}$, $\overline{K}$ & Clock Inputs J - K input Asynchronous Input		-1.6 -3.2 -4.32		-1 -2 -2.7	-1.6 -3.2 -4.32		-1.6 -3.2 -4.32	mA	V_{CC} = 5.25V V_F = 0.45V 5.25V on other inputs
P_D	Power Dissipation Current (each flip-flop) T100 T101		28 33		14 16	28 33		28 33	mA	V_{CC} = 5V S_D at ground
I_{SC}	Output Short-Circuit Current	-30	-120	-30		-120	-30	-120	mA	V_{CC} = 5.25V ground on output and asynchronous input
t_{pd+}	Turn-off Delay			8	12	20			nsec	V_{CC} = 5V C_L = 15 pF see test circuits
t_{pd-}	Turn-on Delay			12	20	30			nsec	
$t_{release}$	T100 T101			10 1	18 7				nsec	
t_{set-up}	T100 T101				22 8	35 15			nsec	
	Negative Clock Pulse Width T100 T101				25 10				nsec	
	Toggle Frequency T100 T101				20 50				MHz	

CONNECTION DIAGRAMS
(top view)



Available in DIP only

FUNCTIONAL LOGIC DIAGRAMS



TRUTH TABLES

SYNCHRONOUS ENTRY J-K MODE OPERATION

T120 INPUTS @ t_n			T121 INPUTS @ t_n			OUTPUTS @ t_{n+1}	
JK	J	$K \cdot \overline{K}$	JK	J	$\overline{K}$	Q	$\overline{Q}$
14	3(13)	5(11)·4(12)	14	3(13)	4(12)	6(10)	7(9)
L	X	X	L	X	X	No Change (note 5)	
H	L	L	H	L	H	No Change (note 5)	
H	L	H	H	L	L	L	H
H	H	L	H	H	H	H	L
H	H	H	H	H	L	Toggles	

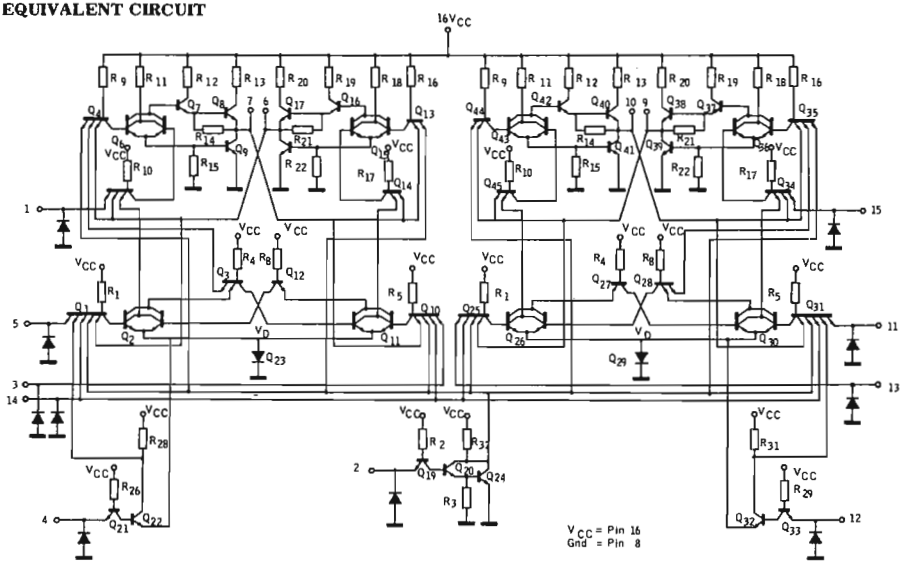
ASYNCHRONOUS ENTRY
Independent of Clock and Synchronous Input

T120 INPUTS	T121 INPUTS		OUTPUTS	
C_D	S_D	C_D	Q	$\overline{Q}$
1(15)	5(11)	1(15)	6(10)	7(9)
L	H	L	L	H
H	H	H	No Change	
	L	L	H	H
	L	H	H	L

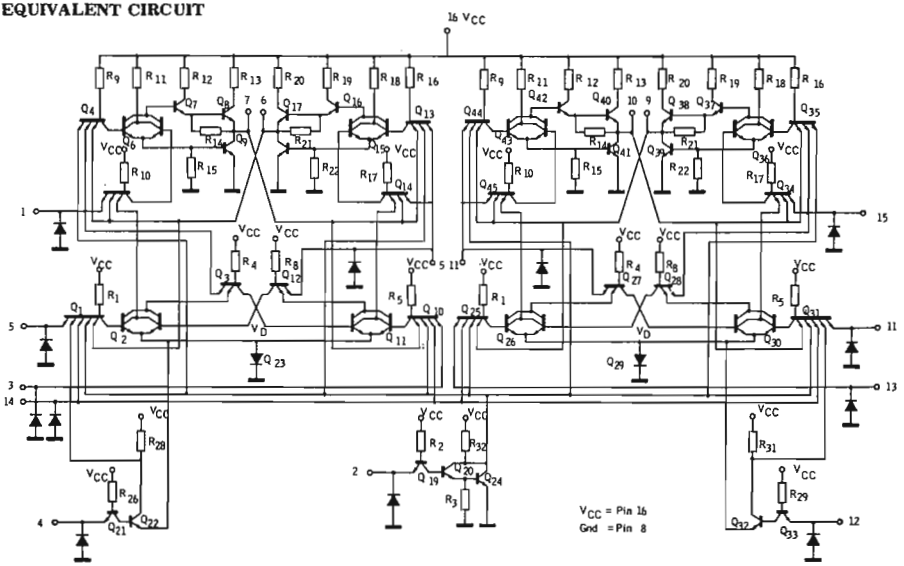
NOTES:

1) H = Most positive logic level
2) L = Most negative logic level
3) X = Could be high or low
4) $\overline{K}$ inputs should be grounded when not in use
5) The L symbol in the J and K input column is defined as meaning that the input does not go high at any time while the clock i low. The H symbol in the J and K input column is defined as meaning that the input has been high at same time as the cloc was low.

T120 EQUIVALENT CIRCUIT



T121 EQUIVALENT CIRCUIT



NOMINAL COMPONENTS VALUES (Both diagrams)

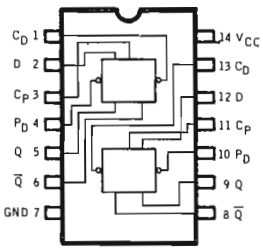
$R_1, R_4, R_5, R_8, R_{10}, R_{14}, R_{17}, R_{21}, R_{22}, R_{23}, R_{24}, R_{26}, R_{29} = 4\,k\Omega$; $R_2, R_3, R_6, R_7 = 2\,k\Omega$; $R_9, R_{16}, R_{28}, R_{31} = 6\,k\Omega$

$R_{11}, R_{18} = 1.5\,k\Omega$; $R_{12}, R_{19} = 150\,\Omega$; $R_{13}, R_{20} = 80\,\Omega$; $R_{15}, R_{22}, R_{25}, R_{27}, R_{30} = 1.25\,k\Omega$; $R_{32} = 1\,k\Omega$; $C_1, C_2 = 10$ pF

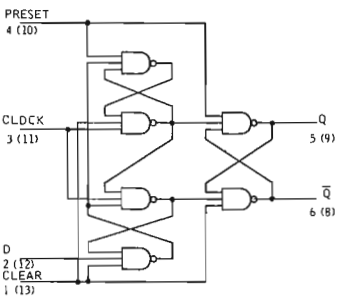
ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V ± 5%)

SYMBOL	CHARACTERISTICS	LIMITS						UNIT	CONDITIONS AND COMMENTS
		0°C		25°C			75°C		
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
V_{OH}	Output High Voltage	2.4		2.4	3		2.4		V	V_{CC} = 4.75V I_{OH} = -1.2 mA V_{IL} on asynchronous input
V_{OL}	Output Low Voltage		0.45		0.21	0.45		0.45	V	V_{CC} = 4.75V I_{OL} = 14.1 mA V_{CC} = 5.25V I_{OL} = 16 mA V_{IH} on asynchronous input
V_{IH}	Input High Voltage	1.9		1.8			1.6		V	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	V	Guaranteed input low threshold for all inputs
I_R	Input Leakage Current									
	J, K and $\overline{K}$ Inputs				5	60		60	μA	V_{CC} = 5.25V
	Clock Input				10	120		120		V_R = 4.5V
	J-K Input				20	240		240		Ground on other inputs
	Asynchronous Input				14	160		160		
I_F	Input Load Current									
	J, K and $\overline{K}$ Inputs		-1.6		-1.1	-1.6		-1.6	mA	V_{CC} = 5.25V
	Clock Input		-3.2		-2.2	-3.2		-3.2		V_F = 0.45V
	J-K Input		-6.4		-4.4	-6.4		-6.4		5.25V on other inputs
	Asynchronous Input		-4.32		-3	-4.32		-4.32		
I_{PD}	Power Dissipation Current (each flip-flop)		30			30		30	mA	V_{CC} = 5V C_D at ground
I_{SC}	Output Short-Circuit Current	-30	-120	-30		-120	-30	-120	mA	V_{CC} = 5.25V ground on output and asynchronous input
t_{pd+}	Turn-off Delay			8	13	22			nsec	
t_{pd-}	Turn-on Delay			12	21	32			nsec	V_{CC} = 5V
$t_{release}$				1	7				nsec	C_L = 15 pF
$t_{set\text{-}up}$					8	16			nsec	see test circuit
	Negative Clock Pulse Width				10				nsec	
	Toggle Frequency				50				MHz	

CONNECTION DIAGRAM
(top view)



FUNCTIONAL LOGIC DIAGRAM



TRUTH TABLES

SYNCHRONOUS ENTRY D MODE OPERATION

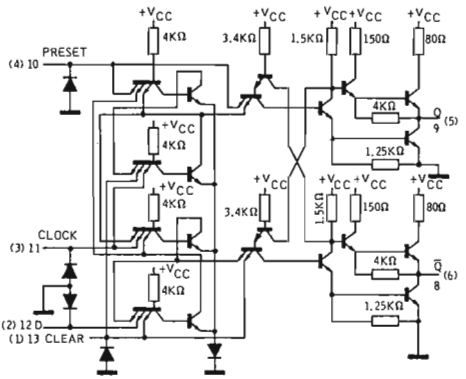
INPUTS @ t_n	OUTPUTS @ t_{n+1}	
D	Q	$\overline{Q}$
2(12)	5(9)	6(8)
L	L	H
H	H	L

ASYNCHRONOUS ENTRY INDEPENDENT OF CLOCK & SYNCHRONOUS INPUTS

INPUTS		OUTPUTS	
Clear	Preset	Q	$\overline{Q}$
1(13)	4(10)	5(9)	6(8)
L	L	H	H
L	H	L	H
H	L	H	L
H	H	No Change	

H = Most positive logic level
L = Most negative logic level

EQUIVALENT CIRCUIT
(one side only)



ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 5%)

SYMBOL	CHARACTERISTICS	LIMITS 0°C Min.	0°C Max.	25°C Min.	25°C Typ.	25°C Max.	75°C Min.	75°C Max.	UNIT	CONDITIONS AND COMMENTS
V_{OH}	Output High Voltage	2.4		2.4	3		2.4		V	V_{CC} = 4.75V I_{OH} = -0.6 mA V_{IL} on asynchronous input
V_{OL}	Output Low Voltage		0.45		0.2	0.45		0.45	V	V_{CC} = 5.25V I_{OL} = 16 mA V_{IH} on asynchronous input
V_{IH}	Input High Voltage	1.9		1.8			1.6		V	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	V	Guaranteed input low threshold for all inputs
I_F	Input Load Current D and P_D Inputs Cp and C_D Inputs		-1.6 -3.2		-1	-1.6 -3.2		-1.6 -3.2	mA	V_{CC} = 5.25V V_F = 0.45V other inputs high
I_R	Input Leakage Current D Input Cp and P_D Inputs C_D Input		60 120 180			60 120 180		60 120 180	μA	V_{CC} = 5.25V V_R = 4.5V
I_{PD}	Power Dissipation Current (each flip-flop)		12			12		12	mA	Ground on C_D V_{CC} = 5V
I_{SC}	Output Short-Circuit Current	-30	-120	-30		-120	-30	-120	mA	V_{CC} = 5.25V ground on output and synchronous input
t_{pd1+}	Turn-off Delay			10	20	35			nsec	D input
t_{pd1-}	Turn-on Delay			10	20	50			nsec	D input
t_{pd2+}	Turn-off Delay					25			nsec	C_D, S_D inputs
t_{pd2-}	Turn-on Delay					40			nsec	C_D, S_D inputs
t_{set-up}	Set-up Time					20			nsec	
$t_{release}$	Release Time			5					nsec	
	Clock Frequency			15					MHz	

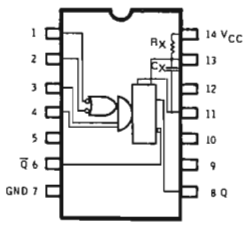
V_{CC} = 5V, C_L = 15pF, see test circuits

STANDARD TEMPERATURE RANGE

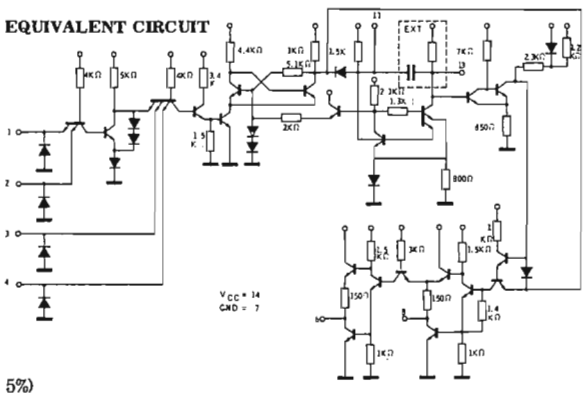
GENERAL DESCRIPTION

This retriggerable monostable multivibrator (or one-shot) provides an output pulse with high accuracy and a very wide duration range (50 nsec to ∞). The T118 will respond to trigger inputs even when already in its active timing state, and will time itself out from the last input pulse received.

CONNECTION DIAGRAM
(top view)



EQUIVALENT CIRCUIT



ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 5%)

SYMBOL	CHARACTERISTICS	LIMITS 0°C Min.	LIMITS 0°C Max.	LIMITS 25°C Min.	LIMITS 25°C Typ.	LIMITS 25°C Max.	LIMITS 75°C Min.	LIMITS 75°C Max.	UNIT	CONDITIONS AND COMMENTS
V_{OH}	Output High Voltage	2.4		2.4	3.4		2.4		V	V_{CC} = 4.75V I_{OH} = -0.72 mA for pin 6 open pin 11 for pin 8 ground pin 11
V_{OL}	Output Low Voltage		0.45		0.2	0.45		0.45	V	V_{CC} = 4.75V I_{OL} = 13 mA for pin 6 ground pin 11 for pin 8 open pin 11
V_{IH}	Input High Voltage	2		2	1.7				V	V_{CC} = 4.75V minimum pulse width 40 nsec
V_{IL}	Input Low Voltage				1.4	0.8		0.8	V	V_{CC} = 5.25V minimum pulse width 40 nsec
I_F	Input Load Current		-1.6		-1	-1.6		-1.6	mA	V_{CC} = 5.25V V_F = 0.45V 4.5V on other input
I_R	Input Leakage Current				15	60		60	μA	V_{CC} = 5.25V V_R = 4.5V ground on other input
I_{PD}	Power dissipation Current		25			25		25	mA	V_{CC} = 5.25V ground on true inputs and 4.5V on complemented inputs
t_{pd+}	Negative Trigger Input to Q Output				25	50			nsec	V_{CC} = 5V R_X = 5 KΩ C_X = 0 C_L = 15 pF see test circuit
t_{pd-}	Negative Trigger Input to Q̄ Output				25	50			nsec	
t_{pw}	Min Q Output Pulse Width (1)				45	65			nsec	
C_{stray}	Max. Allowable Wiring Cap (pin 13)		50			50		50	pF	Gnd on pin 13 This capacitance, if present, will add to C_X in determining output pulse width
R_X	Timing Resistor (2)	5	40	5		40	5	40	KΩ	

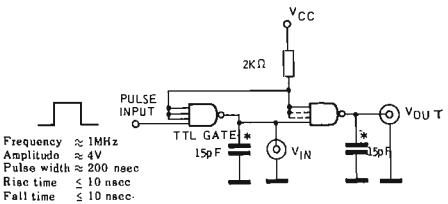
NOTES:

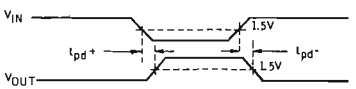
1) Pulse width calculation: $T_{pw} \simeq 0.36\ R_X\ C_X$.
2) Unless otherwise noted, 10 KΩ resistor (R_X) is placed between Pin 13 and V_{CC} for all tests.

SWITCHING TIME TEST CIRCUITS

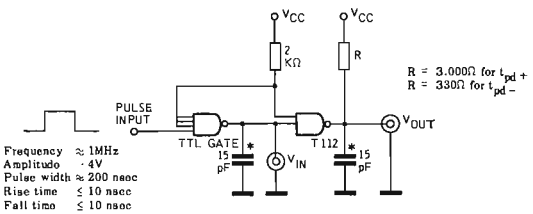
-Sensitivity of all switching parameters to supply voltage change (within range of 5 V ± 10%) and DC loading is very small.

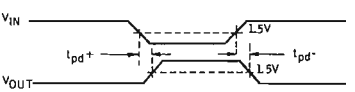
T102-T103-T104-T107-T109-T116 t_{pd} TEST CIRCUIT AND WAVEFORMS



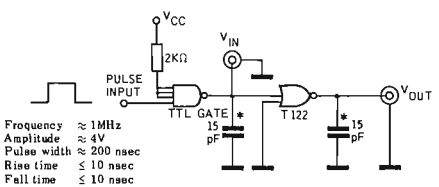


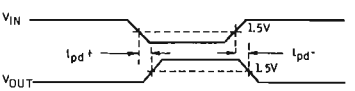
T112 t_{pd} TEST CIRCUIT AND WAVEFORMS



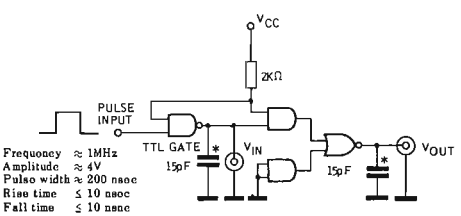


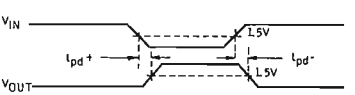
T122 t_{pd} TEST CIRCUIT AND WAVEFORMS





T105 and T115 t_{pd} TEST CIRCUIT (NON-EXPANDABLE SECTION ONLY) AND WAVEFORMS



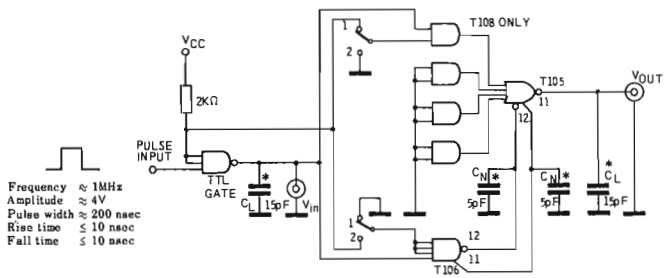


* Capacitance includes probe and Jig capacity.

SWITCHING TIME TEST CIRCUITS

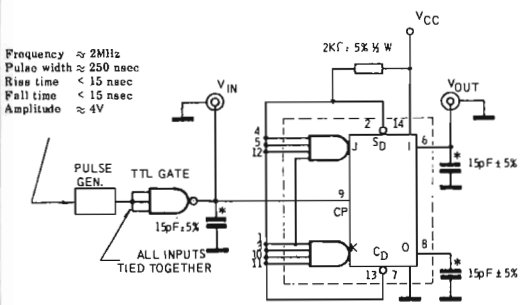
- Sensitivity of all switching parameters to supply voltage change (within range of 5 V ± 10%) and DC loading is very small.
- For Flip-Flops allowable clock skew ≤ t_{pd} (max) + $t_{release}$ (min).

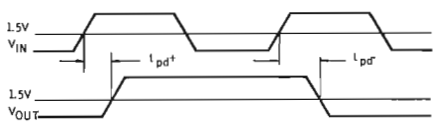
T105-T108 EXPANDABLE GATE AND T106 EXPANDER t_{pd} TEST CIRCUIT



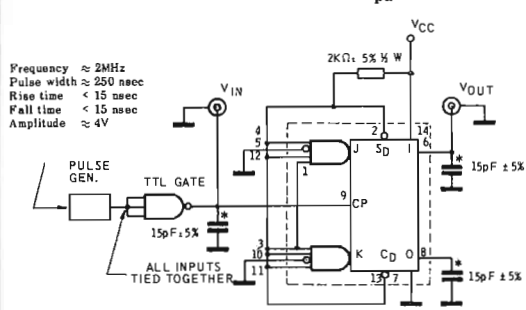
With switch in position 1 measure t_{pd} of T105 - With switch in position 2 measure t_{pd} (T105 - T108) + Δt_{pd} (T106).

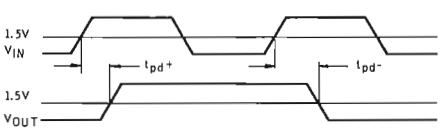
T100 t_{pd} TEST CIRCUIT AND WAVEFORMS





T101 t_{pd} TEST CIRCUIT AND WAVEFORMS



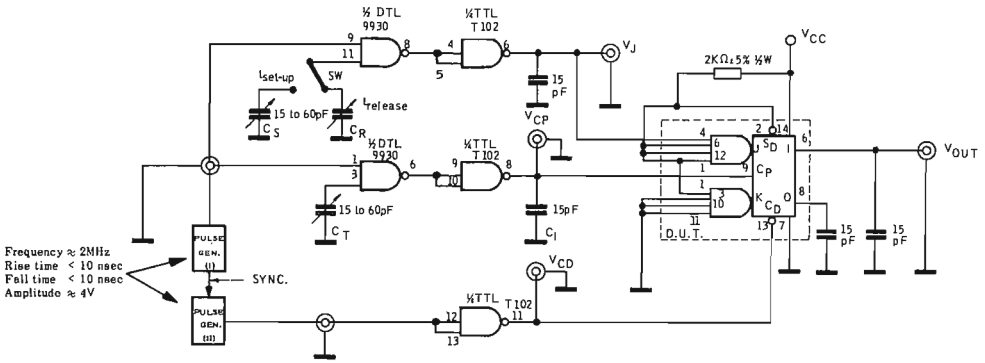


* Capacitance includes probe and Jig capacity.

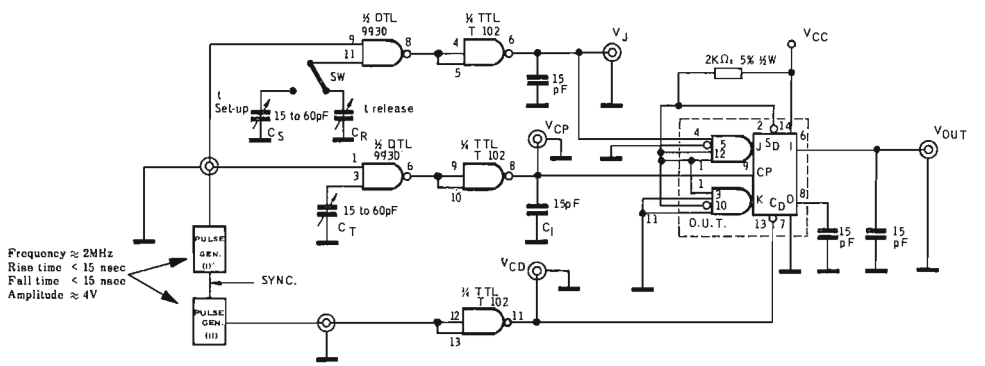
SWITCHING TIME TEST CIRCUITS

- Sensitivity of all switching parameters to supply voltage change (within range of 5 V ± 10%) and D C loading is very small.
- Allowable clock skew ≤ t_{pd} (max) + $t_{release}$ (min).

T100 t_{set-up} and $t_{release}$ TEST CIRCUIT



T101 t_{set-up} and $t_{release}$ TEST CIRCUIT

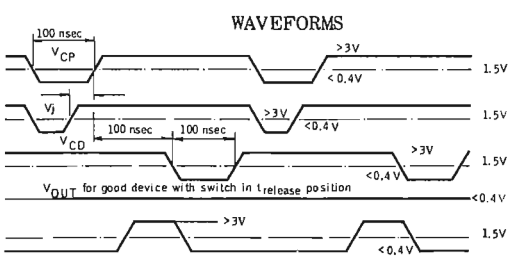


INITIAL ADJUSTMENT

1. With switch in $t_{release}$ position adjust C_T & C_R for proper V_{CP}, V_J & V_D waveforms and $t_{release}$ limit value.
2. With switch in t_{set-up} position adjust C_S for t_{set-up} limit value.

t_{set-up} is defined as the minimum time required for a High to be present at a synchronous logic input at any time during the low state of the clock in order for the flip-flop to respond to the data. $t_{release}$ is defined as the maximum time allowed for a High to be present at a synchronous logic input at any time during the low state of the clock and not be recognized.

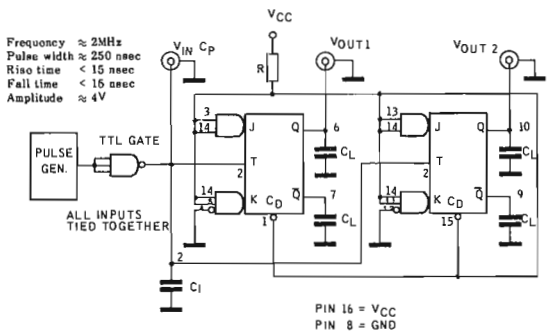
WAVEFORMS



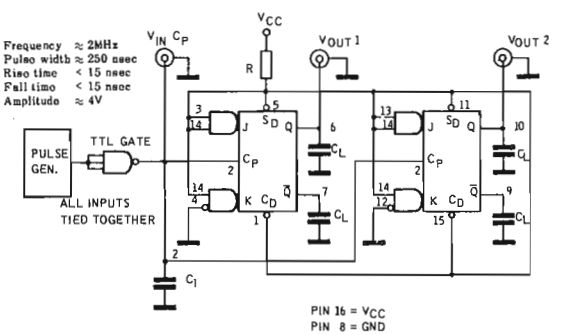
SWITCHING TIME TEST CIRCUITS

- Sensitivity of all switching parameters to supply voltage change (within range of 5 V ± 10%) and D C loading is very small.
- Allowable clock skew ≤ t_{pd} (max) + $t_{release}$ (min).

T120 t_{pd} TEST CIRCUIT



T121 t_{pd} TEST CIRCUIT



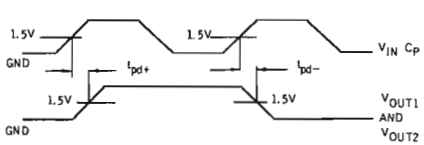
R = 2KΩ ± 5% 1/2W
C_I = 15 pF ± 5%
C_L = 15 pF ± 5%

C_I & C_L include all probe and jig capacity. Very short stranded or printed wire should be used for all interconnections. Probes should be connected directly to the input & output pins.

NOTE:

For $t_{set\text{-}up}$ and $t_{release}$ see T100 and T101 test circuits.

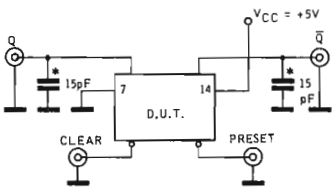
WAVEFORMS

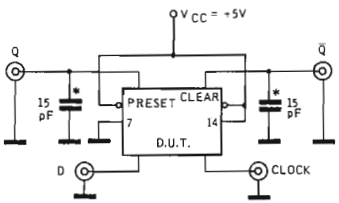


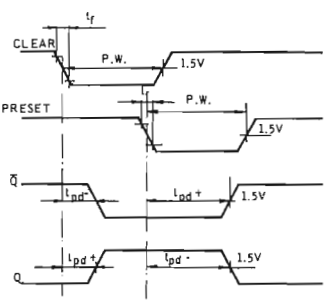
SWITCHING TIME TEST CIRCUITS

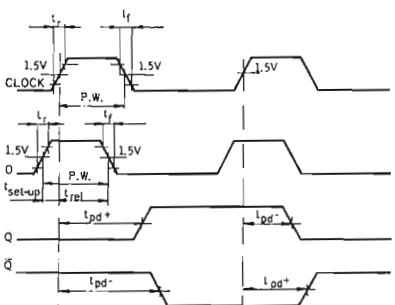
- Sensitivity of all switching parameters to supply voltage change (within range of 5 V ± 10%) and D C loading is very small.
- Allowable clock skew ≤ t_{pd} (max) + $t_{release}$ (min).

T110 t_{pd} TEST CIRCUIT AND WAVEFORMS









Clear: t_f =3 to 6 nsec P.W.=30 nsec f=1 MHz
Amplitude = 0.4 to 2.4 V.

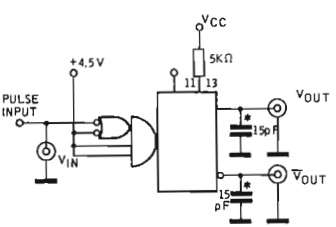
Preset: t_f=3 to 6 nsec P.W.=30 nsec f=1 MHz
Amplitude = 0.4 to 2.4 V.

Clock: t_r=15 nsec t_f=15 nsec P.W.=30 nsec f=1 MHz
Amplitude = 0.4 to 2.4 V.

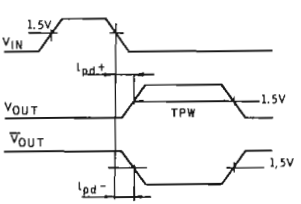
D: t_r=15 nsec t_f= 15 nsec P.W.=25 nsec t_{set-up}=20 nsec
$t_{rel.}$=5 nsec f = 500 kHz Amplitude = 0.4 to 2.4 V.

NOTE:
This Jig is used to test the minimum clock frequency.

T118 t_{pd} TEST CIRCUIT AND WAVEFORMS



Frequency ≈ 1MHz
Amplitude ≈ 3V
Pulse width ≈ 40 nsec
Rise time ≤ 10 nsec
Fall time ≤ 10 nsec



* Capacitance includes probe and Jig capacity.

4-bit shift register

EXTENDED TEMPERATURE RANGE -55°C to 125°C
STANDARD TEMPERATURE RANGE 0°C to 75°C

- INPUT DIODE CLAMPING
- 20 MHz SHIFT FREQUENCY
- SYNCHRONOUS PARALLEL ENTRY
- J,$\overline{K}$ INPUTS TO FIRST STAGE
- ASYNCHRONOUS COMMON RESET
- POWER DISSIPATION OF 300 mW
- CERAMIC HERMETIC AND PLASTIC 16 PIN DUAL IN-LINE PACKAGE

The T 150 4-bit shift-register is constructed on a single silicon chip using the planar epitaxial process. The T 150 has serial and parallel entry, serial and parallel output and Master Reset (MR). Serial input is provided as a J and $\overline{K}$ input, which may be tied together externally to form a "D" input. The MR input clears all stages independent of clock pin level. A logic HIGH on the PE input ensures serial shift operation and a logic LOW enables parallel entry concurrent with low to high transition on the clock input. The J and $\overline{K}$ inputs make the circuit useful as a 4-bit modulo N counter ($N \leq 15$) needing only one additional gate element. The circuit utilizes TTL logic for high speed and high fan-out capability.

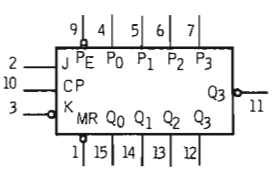
ABSOLUTE MAXIMUM RATINGS
(above which the useful life may be impaired)

Supply Voltage, Continuous	-0.5V to 7V
Input Voltage	-0.5V to 5.5V
Output Voltage	-0.5V to V_{CC}
Storage Temperature Range	-65°C to 150°C

OPERATING CONDITIONS

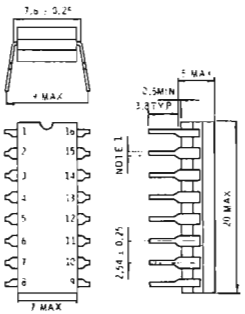
Extended	
Temperature Range	-55°C to 125°C
Supply Voltage	5V ± 10 %
Standard	
Temperature Range	0°C to 75°C
Supply Voltage	5V ± 5%

LOGIC DIAGRAM AND PIN CONNECTION



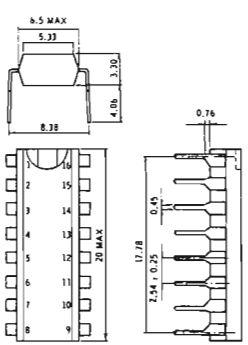
V_{CC} = PIN 16
GND = PIN 8

PHYSICAL DIMENSIONS
16 pin ceramic DIP



NOTES:
1) Board-drilling dimensions should equal your practice for a conventional 0.51 mm. diameter lead.
2) All dimensions in mm.

PHYSICAL DIMENSIONS
16 pin plastic DIP



NOTE: All dimensions in mm.

ORDERING NUMBERS

T 150 D1 (For Ceramic DIP and Standard Temperature Range)
T 150 D2 (For Ceramic DIP and Extended Temperature Range)
T 150 B1 (For Plastic DIP and Standard Temperature Range)

ELECTRICAL CHARACTERISTICS (T_A = 0°C to 75°C, V_{CC} = 5 V ± 5%)

SYMBOL	CHARACTERISTICS	LIMITS 0°C Min.	Max.	25°C Min.	Typ.	Max.	75°C Min.	Max.	Unit	CONDITIONS AND COMMENTS
V_{OH}	Output High Voltage	2.4		2.4	3		2.4		V	V_{CC}=4.75V I_{OH}= -0.36 mA
V_{OL}	Output Low Voltage		0.45		0.2	0.45		0.45	V	V_{CC}=5.25V I_{OL}= 9.6 mA
										V_{CC}=4.75V I_{OL}= 8.5 mA
V_{IH}	Input High Voltage	1.9		1.8			1.6		V	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	V	Guaranteed input low threshold for all inputs
I_F	Input Load Current		-1.6		- 1	-1.6		-1.6	mA	V_{CC}=5.25V V_F = 0.45V other inputs high
I_F	Input Load Current (CP)		-6.4		- 4	-6.4		-6.4	mA	V_{CC}=5.25V V_F = 0.45V other inputs high
I_F	Input Load Current (PE)		-3.7		-2.3	-3.7		-3.7	mA	V_{CC}=5.25V V_F = 0.45V other inputs high
I_R	Input Leakage Current		60		15	60		60	µA	V_{CC}=5.25V V_R = 4.5V
I_R	Input Leakage Current (CP)		240		45	240		240	µA	V_{CC}=5.25V V_R = 4.5V
I_R	Input Leakage Current (PE)		140		35	140		140	µA	V_{CC}=5.25V V_R = 4.5V
I_{SC}	Output Short Circuit Current	-10	-70	-10		-70	-10	-70	mA	V_{CC}= 7V 1.5V on output and 5.25V on P input
I_{PD}	Power Dissipation Current		85			85		85	mA	V_{CC}= 5V

ELECTRICAL CHARACTERISTICS (T_A = -55°C to 125°C, V_{CC} = 5V ± 10%)

SYMBOL	CHARACTERISTICS	LIMITS -55°C Min.	Max.	25°C Min.	Typ.	Max.	125°C Min.	Max.	Unit	CONDITIONS AND COMMENTS
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		V	V_{CC}=4.5V I_{OH}= -0.36 mA
V_{OL}	Output Low Voltage		0.4		0.2	0.4		0.4	V	V_{CC}=5.5V I_{OL}= 9.6 mA
										V_{CC}=4.5V I_{OL}= 7.5 mA
V_{IH}	Input High Voltage	2		1.7			1.4		V	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8			0.9		0.8	V	Guaranteed input low threshold for all inputs
I_F	Input Load Current		-1.6		-1.1	-1.6		-1.6	mA	V_{CC}=5.5V V_F = 0.4V other inputs high
I_F	Input Load Current (CP)		-6.4		-4.2	-6.4		-6.4	mA	V_{CC}=5.5V V_F = 0.4V other inputs high
I_F	Input Load Current (PE)		-3.7		-2.5	-3.7		-3.7	mA	V_{CC}=5.5V V_F = 0.4V other inputs high
I_R	Input Leakage Current		60		15	60		60	µA	V_{CC}=5.5V V_R = 4.5V
I_R	Input Leakage Current (CP)		240		45	240		240	µA	V_{CC}=5.5V V_R = 4.5V
I_R	Input Leakage Current (PE)		140		35	140		140	µA	V_{CC}=5.5V V_R = 4.5V
I_{SC}	Output Short Circuit Current	-10	-70	-10		-70	-10	-70	mA	V_{CC}= 7V 1.5V on output and 5.5V on P input
I_{PD}	Power Dissipation Current		85			85		85	mA	V_{CC}= 5V

FUNCTIONAL DESCRIPTION

CP (common clock input) - shift or parallel entry operation occurs during low to high transition.
$\overline{PE}$ (parallel entry enable) - for parallel entry operation $\overline{PE}$ must be low; for shift operation it must be high.
$\overline{MR}$ (Master Reset) - when $\overline{MR}$ is low, all Q outputs are low independently of the condition of any other inputs.

$J, \overline{K}$ = serial inputs
P_0, P_1, P_2, P_3 = parallel inputs
$Q_3, \overline{Q}_3$ = serial outputs
Q_0, Q_1, Q_2, Q_3 = parallel outputs

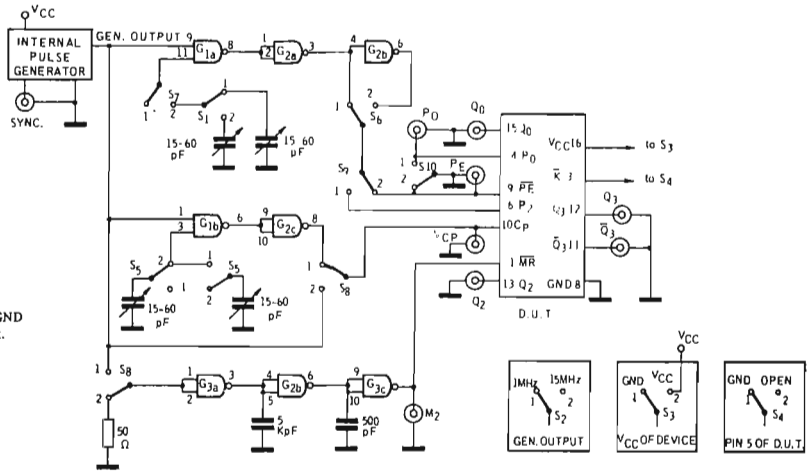
LOADING RULES (1 U.L. = 1 TTL Gate Input Unit Load)

INPUTS :	$J, \overline{K}, \overline{MR}, P_0, P_1, P_2, P_3$	LOADING FACTOR :	1 U.L.
	$\overline{PE}$		2.3 U.L.
	CP		4 U.L.
OUTPUTS:	$Q_0, Q_1, Q_2, Q_3, \overline{Q}_3$	DRIVE FACTOR :	6 U.L.

SWITCHING CHARACTERISTICS ($T_A = 25°C$)

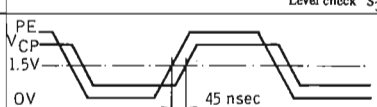
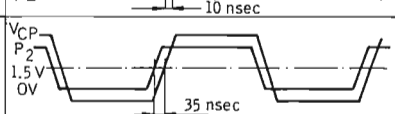
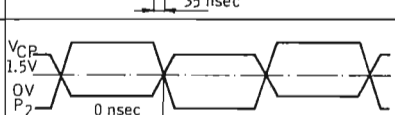
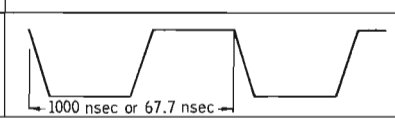
SYMBOL	CHARACTERISTICS	Min	Typ.	Max.	UNIT	CONDITIONS AND COMMENTS
t_{pd+}	Turn-Off Delay	10	20	35	ns	$V_{CC} = 5V$ $C_L = 15pF$ (see figures)
t_{pd-}	Turn-On Delay	10	25	45	ns	
CP_{pw}	Clock Pulse Width	35			ns	
t_s	Set-up Time		17		ns	
t_r	Release Time		17		ns	
$t_{s(\overline{PE})}$	Set-up Time for $\overline{PE}$		26		ns	
$t_{r(\overline{PE})}$	Release Time for $\overline{PE}$		26	10	ns	
$t_{pd-(\overline{MR})}$	Reset Time for $\overline{MR}$		35		ns	
$t_{rec(\overline{MR})}$	Recovery Time for $\overline{MR}$		20		ns	
$\overline{MR}_{pw}$	Min. Reset Pulse Width		15		ns	

T150 SWITCHING TEST JIG

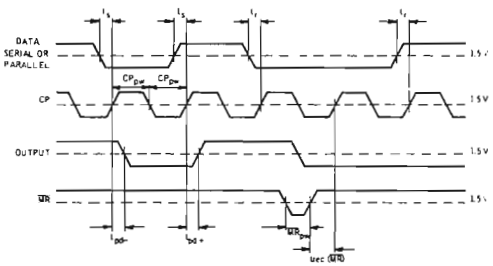


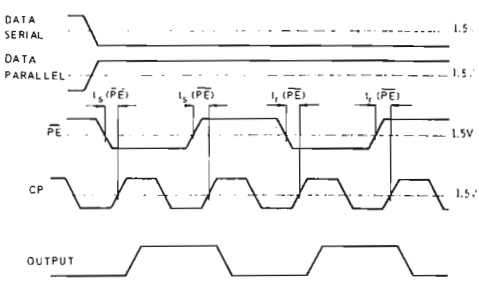
NOTES
G_1 = 9930
G_2 = T102
G_3 = T102
V_{CC} = 5V
S_3 is used for GND reference check.

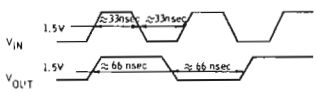
TABLE TO BE USED TO CHECK JIG FOR CALIBRATION

Test Type	Switch Numbers										Probe "A"	Probe "B"	TEST POINT LIMITATIONS (V_{CC} = 5V Scope trigger connected to sync. Level check "S_3")
	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10			
(PE) SET CHECK	1 or 2	1	2	2	1	1	1	1	2	1	VCP	PE	
(PE) RELEASE CHECK	2	1	2	2	1	2	2	1	2	1	VCP	PE	
(P2) SET CHECK	1 or 2	1	2	2	2	1	1	1	1	2	VCP	P2	
(P2) RELEASE CHECK	1	1	2	2	2	2	2	1	1	2	VCP	P2	
RESET CHECK	1 or 2	1	2	1	1	1	1	1	1	1 or 2	VCP	RESET	
FREQ. CHECK	1 or 2	1 and 2	2	2	2	2	2	2	2	1 or 2	VCP	VCP	

SWITCHING TIME AND SHIFT FREQUENCY WAVEFORMS



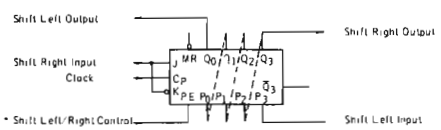




(PIN 12 or 11) V_{OUT} Frequency = ½ X V_{IN} Frequency

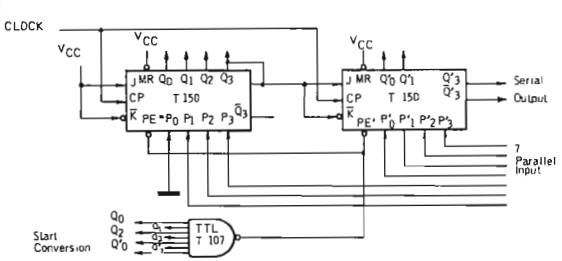
APPLICATIONS

A. 4-BIT LEFT/RIGHT SHIFT REGISTER



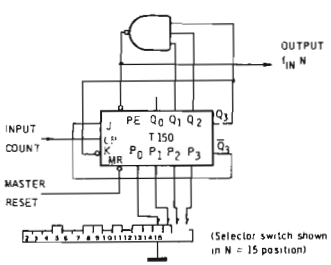
* To Shift Right-Input HIGH
To Shift Left-Input LOW

B. 7 - BIT PARALLEL - TO - SERIAL CONVERTER



* This circuit uses a marker bit to count the data bits shifted out so that a parallel load enable is generated to load the next parallel word for conversion at the correct time.

C. DIVIDE BY "N" COUNTER ("N" = 2 to 15)



One-of-ten decoder

EXTENDEND TEMPERATURE RANGE
-55°C to 125°C
STANDARD TEMPERATURE RANGE
0°C to 75°C

- INPUT DIODE CLAMPING
- TYPICAL INPUT/OUTPUT PROPAGATION DELAY 20 ns
- MULTI-FUNCTION CAPABILITY
- MUTUALLY EXCLUSIVE OUTPUTS
- DEMULTIPLEXING CAPABILITY
- TYPICAL POWER DISSIPATION OF 145 mW
- CERAMIC HERMETIC AND PLASTIC 16 PIN DUAL IN-LINE PACKAGE

The T 151 one-of-ten decoder is a circuit constructed on a single silicon chip by means of the planar epitaxial process. The T 151 is a multifunction decoder. Designed to accept four weighted inputs and provide ten mutually exclusive outputs, the circuit utilizes TTL logic for high speed and high fan-out capability. The unique logic of this device makes it very versatile in decoding and logic conversion applications.

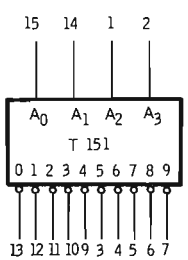
ABSOLUTE MAXIMUM RATINGS
(above which the useful life may be impaired)

Supply Voltage, Continuous	-0.5V to 7 V
Input Voltage	-0.5 V to 5.5 V
Output Voltage	-0.5 V to V_{CC}
Storage Temperature Range	-65°C to 150°C

OPERATING CONDITIONS

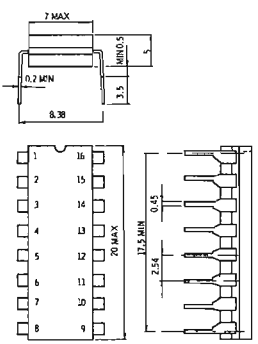
Extended	
Temperature Range	-55°C to 125°C
Supply Voltage	5 V ± 10%
Standard	
Temperature Range	0°C to 75°C
Supply Voltage	5 V ± 5%

LOGIC DIAGRAM AND PIN CONNECTION



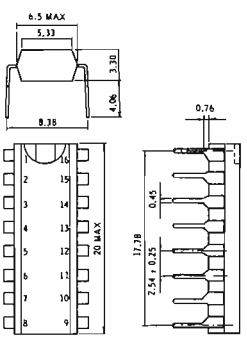
V_{CC} = PIN 16
GND = PIN 8

PHYSICAL DIMENSIONS
16-pin ceramic DIP



Note : all dimensions in mm.

PHYSICAL DIMENSIONS
16 pin plastic DIP



NOTE: All dimensions in mm.

ORDERING NUMBERS

T 151 D1 (For Ceramic DIP and Standard Temperature Range)
T 151 D2 (For Ceramic DIP and Extended Temperature Range)
T 151 B1 (For Plastic DIP and Standard Temperature Range)

ELECTRICAL CHARACTERISTICS (0°C to 75°C, V_{CC} = 5V ± 5%)

SYMBOL	CHARACTERISTIC	LIMITS						Unit	CONDITIONS AND COMMENTS
		0°C		25°C			75°C		
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
V_{OH}	Output High Voltage	2.4		2.4	3		2.4		V	V_{CC}=4.75V, I_{OH}= -0.6 mA
V_{OL}	Output Low Voltage		0.45		0.2	0.45		0.45	V	V_{CC}=4.75V, I_{OL}= 14.1 mA
										V_{CC}=5.25V, I_{OL}= 16 mA
V_{IH}	Input High Voltage	1.9		1.8			1.6		V	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	V	Guaranteed input low threshold for all inputs
I_F	Input Load Current		-1.6		-1	-1.6		-1.6	mA	V_{CC}=5.25V, V_F= 0.45 V
I_R	Input Leakage Current		60		15	60		60	µA	V_{CC}=5.25V, V_R= 4.5 V
I_{SC}	Output Short Circuit Current	-10	-70	-10		-70	-10	-70	mA	V_{CC}=5.25V, output grounded
I_{PD}	Power Dissipation Current		45			45		45	mA	V_{CC}= 5V, A_0, A_1, A_2, A_3 inputs grounded

ELECTRICAL CHARACTERISTICS (-55°C to 125°C, V_{CC} = 5V ± 10%)

SYMBOL	CHARACTERISTICS	LIMITS						Unit	CONDITIONS AND COMMENTS
		-55°C		25°C			125°C		
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		V	V_{CC}=4.5V, I_{OH}= -0.6 mA
V_{OL}	Output Low Voltage		0.4		0.2	0.4		0.4	V	V_{CC}=4.5V, I_{OL}= 12.4 mA
										V_{CC}=5.5V, I_{OL}= 16 mA
V_{IH}	Input High Voltage	2		1.7			1.4		V	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8			0.9		0.8	V	Guaranteed input low threshold for all inputs
I_F	Input Load Current		-1.6		-1.1	-1.6		-1.6	mA	V_{CC}=5.5V, V_F = 0.4 V
I_R	Input Leakage Current		60		15	60		60	µA	V_{CC}=5.5V, V_R =4.5V
I_{SC}	Output Short Circuit Current	-10	-70	-10		-70	-10	-70	mA	V_{CC}=5.5V, output grounded
I_{PD}	Power Dissipation Current		45			45		45	mA	V_{CC}= 5V, A_0, A_1, A_2, A_3 inputs grounded

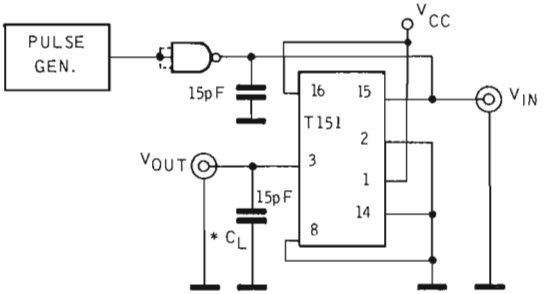
LOADING RULES (1 U.L. = 1 TTL Gate Input Unit Load)

INPUTS : A_0, A_1, A_2, A_3 — LOADING FACTOR : 1 U.L.
OUTPUTS : 0, 1, 2, 3, 4, 5, 6, 7, 8, 9 — DRIVE FACTOR : 10 U.L.

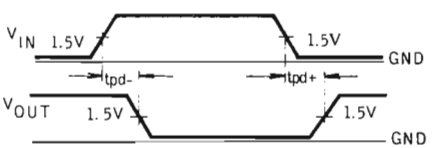
SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	CHARACTERISTICS	Min.	Typ.	Max.	Unit	CONDITIONS AND COMMENTS
t_{pd+}	Turn-Off Delay	10	20	35	nsec	V_{CC} = 5V C_L = 15 pF
t_{pd-}	Turn-On Delay	7	20	30	nsec	

TEST CIRCUIT



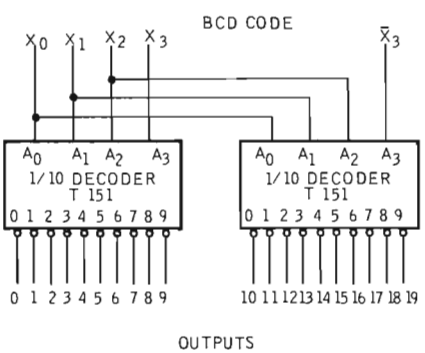
WAVEFORMS



* The capacitance shall be within ± 5% including jig, probe and wiring capacitance.

APPLICATIONS

A. DECODER FOR ANY BCD CODE

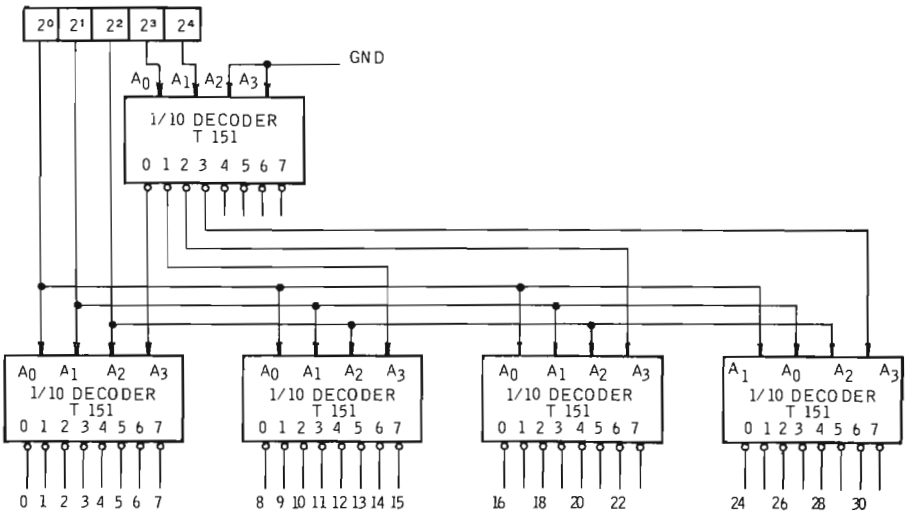


DECIMAL DIGIT	OUTPUT BCD CODE			
	8421	5421	Excess 3	4221
0	0.18	0.18	3	0.18
1	1.19	1.19	4	1.19
2	2	2	5	2
3	3	3	6	3
4	4	4	7	6
5	5	8.10	8.10	9.11
6	6	9.11	9.11	14
7	7	12	12	15
8	8.10	13	13	16
9	9.11	14	14	17

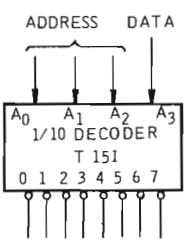
Decode any BCD code using two T 151 elements. Any 4 bit BCD code may be decoded by selecting outputs as shown in the table.

APPLICATIONS (contd)

B. ONE OF THIRTY-TWO DECODING



C. DIGITAL DEMULTIPLEXER



ADDRESS			OUTPUT LINE
A	B	C	
0	0	0	0
1	0	0	1
0	1	0	2
1	1	0	3
0	0	1	4
1	0	1	5
0	1	1	6
1	1	1	7

The single-line input data may be routed to any one of 8 outputs by addressing that output as shown. All non-addressed outputs remain high.

NOTE : Complements of output lines 0 and 1 are available on output lines 8 and 9 respectively.

EXTENDED TEMPERATURE RANGE,
-55°C to 125°C
STANDARD TEMPERATURE RANGE,
0°C to 75°C

- INPUT DIODE CLAMPING
- MULTI-FUNCTION CAPABILITY
- 8ns CARRY PROPAGATION DELAY
- COMPLEMENTARY INPUTS AND OUTPUTS
- TYPICAL POWER DISSIPATION OF 150 mW
- CERAMIC HERMETIC AND PLASTIC 16 PIN DUAL IN-LINE PACKAGE

Dual full adder

The T 152 dual full adder is a medium scale integrated circuit constructed on a single silicon chip using the planar epitaxial process. The T 152 consists of two independent, high-speed, binary full adders with complementary sum (S and $\bar{S}$) outputs. One adder features inverted carry ($\bar{C}_{OUT}$) output, while the second adder has complementary ($\bar{A}_2$ and $\bar{B}_2$) inputs and an inverted carry ($\bar{C}_{IN}$) input. By connecting the inverted carry output of the first adder to the inverted carry input of the second adder, the device performs the addition of two 2-bit binary numbers. Designed especially for multiple-bit, parallel-add/serial-carry applications, the circuit utilizes TTL logic for high-speed, high fan-out operation. The single inversion unique circuitry of the serial-carry outputs minimizes the necessity for complicated "look-ahead" and carry-cascading circuits.

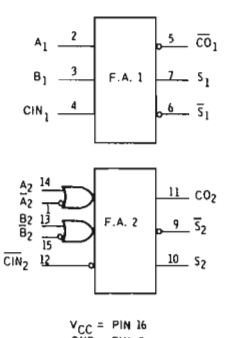
ABSOLUTE MAXIMUM RATINGS
(above which the useful life may be impaired)

Supply Voltage, Continuous	-0.5 V to 7 V
Input Voltage	-0.5 V to 5.5 V
Output Voltage	-0.5 V to V_{CC}
Storage Temperature Range	-65°C to 150°C

OPERATING CONDITIONS

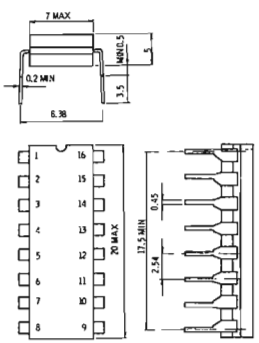
Extended	
Temperature Range	-55°C to 125°C
Supply Voltage	5 V ± 10%
Standard	
Temperature Range	0°C to 75°C
Supply Voltage	5 V ± 5 %

LOGIC DIAGRAM AND PIN CONNECTION



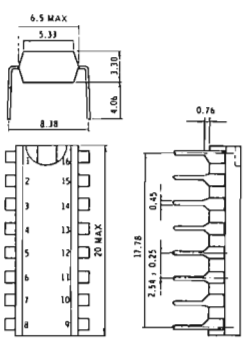
V_{CC} = PIN 16
GND = PIN 8

PHYSICAL DIMENSIONS
16 pin ceramic DIP



Note : all dimensions in mm.

PHYSICAL DIMENSIONS
16 pin plastic DIP



NOTE: All dimensions in mm.

ORDERING NUMBER :

T 152 D1 (For Ceramic DIP and Standard Temperature Range)
T 152 D2 (For Ceramic DIP and Extended Temperature Range)
T 152 B1 (For Plastic DIP and Standard Temperature Range)

ELECTRICAL CHARACTERISTICS (0°C to 75°C, V_{CC} = 5 V ± 5%)

SYMBOL	CHARACTERISTICS	LIMITS 0°C Min.	0°C Max.	25°C Min.	25°C Typ.	25°C Max.	75°C Min.	75°C Max.	Unit	CONDITIONS AND COMMENTS
V_{OH}	Output High Voltage	2.4		2.4	3		2.4		V	V_{CC}=4.75V I_{OH}=-0.6 mA $S_1, \overline{S}_2$ I_{OH}=-0.54mA $\overline{S}_1, S_2$ I_{OH}=-0.42mA $\overline{CO}_1, CO_2$
V_{OL}	Output Low Voltage		0.45		0.21	0.45		0.45	V	V_{CC}=5.25V I_{OL}=16mA $S_1, \overline{S}_2$ I_{OL}=14.4mA $\overline{S}_1, S_2$ I_{OL}=11.2mA $\overline{CO}_1, CO_2$
V_{IH}	Input High Voltage	1.9		1.8			1.6		V	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	V	Guaranteed input low threshold for all inputs
I_F	Input Load Current A_2 and B_2 Inputs		-1.6		-1.1	-1.6		-1.6	mA	V_{CC}=5.25V V_F= 0.45V
	Other Inputs		-6.4		-4.4	-6.4		-6.4	mA	
I_R	Input Leakage Current A_2 and B_2 Inputs		60		15	60		60	µA	V_{CC}=5.25V V_R=4.5V
	Other Inputs		240		60	240		240	µA	
I_{SC}	Output Short Circuit Current	-30	-100	-30		-100	-30	-100	mA	V_{CC}=5.75V output grounded
I_{PD}	Power Dissipation Current		55			55		55	mA	V_{CC}=5V A_2 and B_2 grounded

ELECTRICAL CHARACTERISTICS (-55°C to 125°C, V_{CC} = 5 V ± 10%)

SYMBOL	CHARACTERISTICS	LIMITS -55°C Min.	-55°C Max.	25°C Min.	25°C Typ.	25°C Max.	125°C Min.	125°C Max.	Unit	CONDITIONS AND COMMENTS
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		V	V_{CC}=4.5V I_{OH}=-0.6mA $S_1, \overline{S}_2$ I_{OH}=-0.54mA $\overline{S}_1, S_2$ I_{OH}=-0.42mA $\overline{CO}_1, CO_2$
V_{OL}	Output Low Voltage		0.4		0.21	0.4		0.4	V	V_{CC}=5.5V I_{OL}=16 mA $S_1, \overline{S}_2$ I_{OL}=14.4mA $\overline{S}_1, S_2$ I_{OL}=11.2mA $\overline{CO}_1, CO_2$
V_{IH}	Input High Voltage	2		1.7			1.4		V	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8			0.9		0.8	V	Guaranteed input low threshold for all inputs
I_F	Input Load Current A_2 and B_2 Inputs		-1.6		-1.1	-1.6		-1.6	mA	V_{CC}=5.5V V_F=0.4V
	Other Inputs		-6.4		-4.4	-6.4		-6.4	mA	
I_R	Input Leakage Current A_2 and B_2 Inputs		60		15	60		60	µA	V_{CC}=5.5V V_R = 4.5V
	Other Inputs		240		60	240		240	µA	
I_{SC}	Output Short Circuit Current	-30	-100	-30		-100	-30	-100	mA	V_{CC}= 6V output grounded
I_{PD}	Power Dissipation Current		55			55		55	mA	V_{CC}= 5V A_2 and B_2 grounded

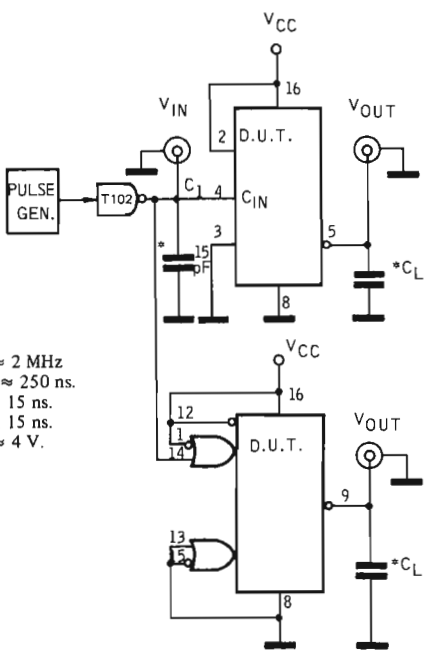
LOADING RULES (1 U.L. = 1 TTL gate input unit load)

INPUTS	A_1, B_1, C_{IN1}	LOADING FACTOR	:	4 U.L.
	$\bar{A}_2$, $\bar{B}_2$, $\bar{C}_{IN1}$			4 U.L.
	A_2, B_2,			1 U.L.
OUTPUTS	$\bar{C}_{01}$, C_{02}	DRIVE FACTOR	:	7 U.L.
	$\bar{S}_1$, S_2			9 U.L.
	S_1, $\bar{S}_2$			10 U.L.

SWITCHING CHARACTERISTICS ($T_A = 25°C$)

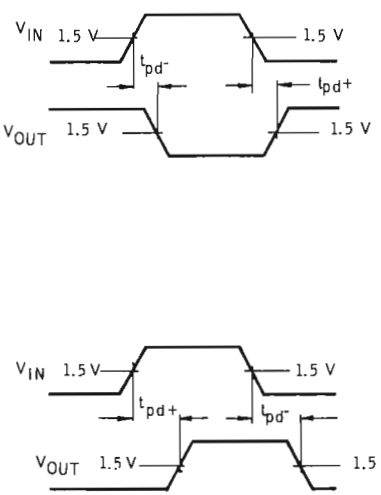
SYMBOL	CHARACTERISTICS	Min.	Typ.	Max.Ext.	Max.Std.	Unit	CONDITIONS AND COMMENTS
t_{pd+}	C_{IN} to $\bar{C}_{OUT}$ and $\bar{C}_{IN}$ to C_{OUT}	2	8	13	15	nsec	V_{CC} = 5V C_L = 15 pF (see test circuit)
t_{pd-}	C_{IN} to $\bar{C}_{OUT}$ and $\bar{C}_{IN}$ to C_{OUT}	2	8	13	15	nsec	
t_{pd+}	A_2 to $\bar{S}_2$	8	25	40	45	nsec	
t_{pd-}	A_2 to $\bar{S}_2$	8	20	35	40	nsec	

tpd TEST CIRCUIT



Frequency ≈ 2 MHz
Pulse Width ≈ 250 ns.
Rise Time < 15 ns.
Fall Time < 15 ns.
Amplitude ≈ 4 V.

WAVEFORMS



* The capacitance shall be within ± 5% including jig, probe and wiring capacitance.

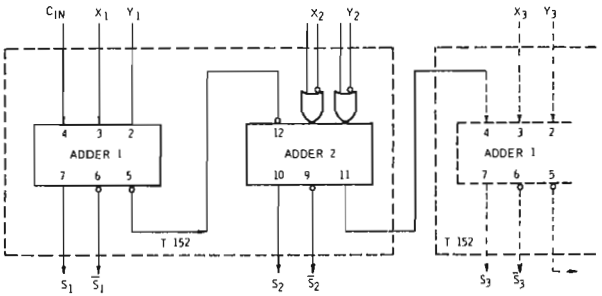
TRUTH TABLE

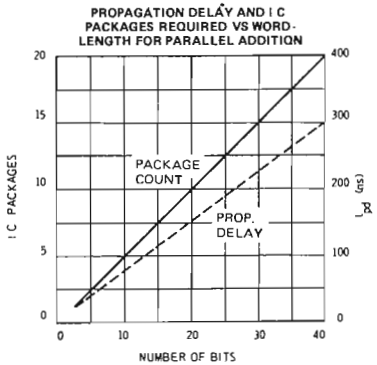
ADDER 1					
INPUTS			OUTPUTS		
C_{IN}	B	A	$\overline{C}_{OUT}$	$\overline{S}$	S
0	0	0	1	1	0
0	0	1	1	0	1
0	1	0	1	0	1
0	1	1	0	1	0
1	0	0	1	0	1
1	0	1	0	1	0
1	1	0	0	1	0
1	1	1	0	0	1

ADDER 2							
INPUTS					OUTPUTS		
$\overline{C}_{IN}$	B_2	A_2	$\overline{B}_2$	$\overline{A}_2$	C_{OUT}	S	$\overline{S}$
0	0	0	0	0	1	1	0
0	0	0	0	1	1	0	1
0	0	0	1	0	1	0	1
0	0	0	1	1	0	1	0
0	0	1	0	0	1	1	0
0	0	1	0	1	1	1	0
0	0	1	1	0	1	0	1
0	0	1	1	1	1	0	1
0	1	0	0	0	1	1	0
0	1	0	0	1	1	0	1
0	1	0	1	0	1	1	0
0	1	0	1	1	1	0	1
0	1	1	0	0	1	1	0
0	1	1	0	1	1	1	0
0	1	1	1	0	1	1	0
0	1	1	1	1	1	1	0
1	0	0	0	0	1	0	1
1	0	0	0	1	0	1	0
1	0	0	1	0	0	1	0
1	0	0	1	1	0	0	1
1	0	1	0	0	1	0	1
1	0	1	0	1	1	0	1
1	0	1	1	0	0	1	0
1	0	1	1	1	0	1	0
1	1	0	0	0	1	0	1
1	1	0	0	1	0	1	0
1	1	0	1	0	1	0	1
1	1	0	1	1	0	1	0
1	1	1	0	0	1	0	1
1	1	1	0	1	1	0	1
1	1	1	1	0	1	0	1
1	1	1	1	1	1	0	1

APPLICATIONS

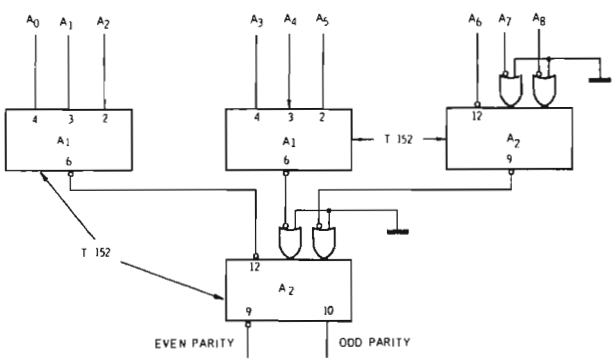
A. PARALLEL ADDITION – RIPPLE CARRY





The curve shows propagation delay of the ripple - carry adder shown in the above figure and also the low package count resulting from this-ripple-carry configuration.

B. PARITY - GENERATION OR CHECKING



The above configuration uses the T152 elements to generate parity for an 8 - bit byte or check parity over 9 - bits. Additional adder blocks can be used to generate or check parity over larger word lengths.

256-bit read only memory

STANDARD TEMPERATURE RANGE 0°C to 75°C

- COMPATIBLE WITH OTHER DTL OR TTL FAMILY PRODUCTS
- INPUT DIODE CLAMPING
- OPEN-COLLECTOR OUTPUTS PERMIT WIRED-OR CAPABILITY
- SINGLE TTL LOAD INPUTS
- ALL CERAMIC HERMETIC 16 PIN DUAL IN-LINE PACKAGE

The T 154 is a 256-bit bipolar transistor-transistor logic read only memory. The memory is organized as 32 words of 8 bits each. The words are selected through 5 address lines. The 8 outputs of the words are uncommitted collectors which may be wired-OR connected with the outputs of other ROM's. An Enable input is provided for additional decoding flexibility. A high Enable forces all outputs to be high. The contents of the memory are permanently programmed on customer request.

ORDERING NUMBER

T154 D1XXXX, where XXXX are letters identifying the particular content.

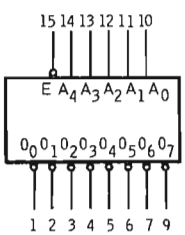
ABSOLUTE MAXIMUM RATINGS
(above which the useful life may be impaired)

V_{CC} Pin Potential to Ground	- 0.5V to 8V
Input Voltage	- 0.5V to 5.5V
Current Into Output Terminal	100 mA
Output Voltages	- 0.5 to V_{CC} value
Storage Temperature Range	- 65°C to 150°C
Temperature (Ambient) Under Bias	- 55°C to 125°C

OPERATING CONDITIONS

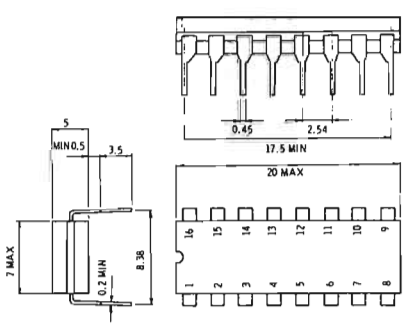
Temperature Range	0°C to 75°C
Supply Voltage	5V ± 5%

LOGIC DIAGRAM AND PIN CONNECTION



GND = 8
V_{CC} = 16

PHYSICAL DIMENSIONS
16-pin ceramic DIP



Note: all dimensions in mm.

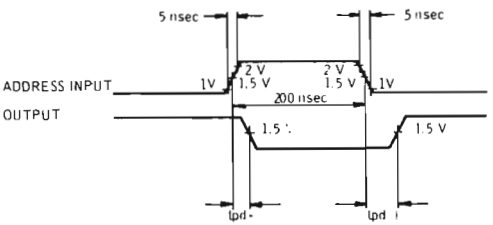
ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 5%)

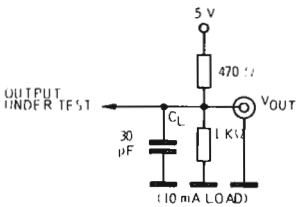
SYMBOL	CHARACTERISTICS	LIMITS			Unit	CONDITIONS AND COMMENTS
		Min.	Typ.	Max.		
V_{OL}	Output Low Voltage			0.45	V	V_{CC} = 4.75V I_{OL} = 10 mA Monitor appropriate output to perform this test.
V_{IL}	Input Low Voltage			0.85	V	V_{CC} = 5.25V Monitor appropriate output to perform this test.
V_{IH}	Input High Voltage	2			V	V_{CC} = 4.75V Monitor appropriate output to perform this test.
I_F	Input Load Current			- 1.6	mA	V_{CC} = 5.25V V_F = 0.45V
I_R	Input Leakage Current			100	µA	V_{CC} = 5.25V V_R = 4.5V
I_{CEX}	Output Leakage Current			100	µA	V_{CC} = 4.75V 5.25V on output.
I_{PD}	Power Dissipation Current		55	80	mA	V_{CC} = 5.25V Enable and Address inputs grounded.

SWITCHING CHARACTERISTICS (T_A = 25°C)

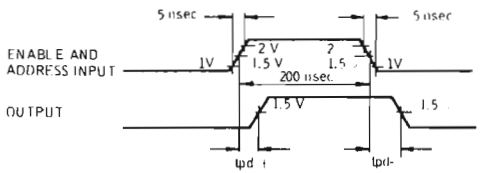
SYMBOL	CHARACTERISTICS	LIMITS			Unit	CONDITIONS AND COMMENTS
		Min.	Typ.	Max.		
t_{pd+}	Enable and Address to Output Delay		30	50	ns	10 mA load } Monitor appropriate outputs to perform these tests. (See fig. 1)
t_{pd-}	Enable and Address to Output Delay		30	50	ns	10 mA load

SWITCHING TIME TEST:OUTPUT LOAD AND WAVEFORMS (Fig. 1)





C_L includes probe and jig capacitance.



TRUTH TABLE

	WORD	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
INPUTS	ENABLE	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
	ADDRESS 1	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H
	ADDRESS 2	L	L	H	H	L	L	H	H	L	L	H	H	L	L	H	H	L	L	H	H	L	L	H	H	L	L	H	H	L	L	H	H
	ADDRESS 3	L	L	L	L	H	H	H	H	L	L	L	L	H	H	H	H	L	L	L	L	H	H	H	H	L	L	L	L	H	H	H	H
	ADDRESS 4	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H
	ADDRESS 5	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
OUTPUTS	OUTPUT 0_0																																
	OUTPUT 0_1																																
	OUTPUT 0_2																																
	OUTPUT 0_3																																
	OUTPUT 0_4																																
	OUTPUT 0_5																																
	OUTPUT 0_6																																
	OUTPUT 0_7																																

NOTES :

1) A high Enable forces all outputs to be high, irrespective of the selected word.
2) The output levels are not shown on the truth table since the customer specifies the output condition he desires at each of the eight outputs for each of the 32 words.
3) The output truth table has to be filled up with an X where a low level is required.
4) H = high level; L = low level.

HOW TO HAVE A CUSTOMIZED ROM

The SGS CAD facilities are used to customize the ROM. A large computer drives a photocomposition machine to make, from your content-punched cards, the test sequence, the truth table and the masks.
This unique system eliminates pattern conversion errors; upon request a computer generated truth table could be supplied for customer re-check purposes.

Punched card format

The punched cards suitable for SGS CAD are the 80 column type and one card per word is needed.

1st to 12th column – part number, alphanumeric. Each custom ROM is assigned its unique part number. First column shows the first character.

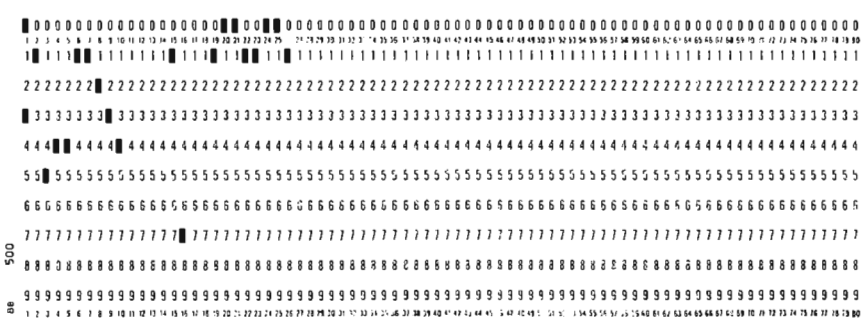
13th to 16th column – word number, numeric. First word is always called N° zero. Last column is the unit digit.

17th and 18th columns- blanks b.

19th to 26th column – word content expressed in one's and zero's. Column 19 corresponds to the output 0_0, the 20th to 0_1, etc.

EXAMPLE :

T154D1ABCD 17 10011001



8-input multiplexer

TTL family product

EXTENDED TEMPERATURE RANGE
-55°C + 125°C
STANDARD TEMPERATURE RANGE
0°C + 75°C

- COMPATIBLE WITH ALL OTHER DTL AND TTL FAMILY PRODUCTS
- INPUT DIODE CLAMPING
- TYPICAL DELAY-TIME 25 n SEC.
- TYPICAL POWER-DISSIPATION 135 mW
- MULTIFUNCTION CAPABILITY
- DATA INPUT ENABLE
- CERAMIC HERMETIC AND PLASTIC 16 PIN DUAL IN-LINE PACKAGE

The T 163 is a high speed eight input digital multiplexer circuit constructed on a single silicon chip using the planar epitaxial process. It provides, in one package, the ability to select one bit of data from up to eight sources. The T 163 can be used as a universal function generator to generate any logic function of four variables. Both assertion and negation outputs are provided. The active pull-ups on the outputs provide high speed, high fan-out and the TTL circuitry makes the T 163 compatible with all other devices of the CCSL family.

ABSOLUTE MAXIMUM RATINGS
(above which the useful life may be impaired)

Supply Voltage, Continuous	-0.5V to 7V
Input Voltage	-0.5V to 5.5V
Output Voltage	-0.5V to V_{CC}
Storage Temperature Range	-65°C to 150°C
Temperature (Ambient) Under Bias	-55°C to 125°C

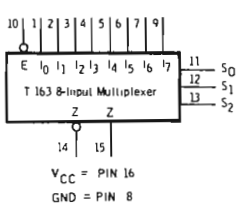
OPERATING CONDITIONS

Extended	
Temperature Range	-55°C to 125°C
Supply Voltage	5V ± 10%
Standard	
Temperature Range	0°C to 75°C
Supply Voltage	5V ± 5%

ORDERING NUMBERS

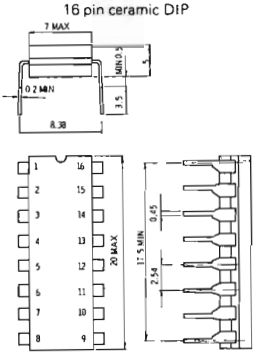
T 163 D1 (For Ceramic DIP and Standard Temperature Range)
T 163 D2 (For Ceramic DIP and Extended Temperature Range)
T 163 B1 (For Plastic DIP and Standard Temperature Range)

LOGIC DIAGRAM AND PIN CONNECTION



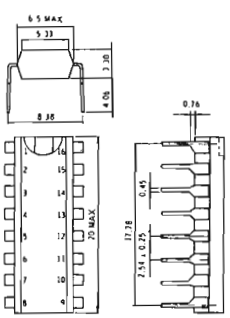
V_{CC} = PIN 16
GND = PIN 8

PHYSICAL DIMENSIONS
16 pin ceramic DIP



Note : all dimensions in mm.

PHYSICAL DIMENSIONS
16 pin plastic DIP



NOTE: All dimensions in mm.

ELECTRICAL CHARACTERISTICS (0°C to 75°C, V_{CC} = 5V ± 5%)

Symbol	CHARACTERISTICS	LIMITS 0°C Min.	0°C Max.	25°C Min.	25°C Typ.	25°C Max.	75°C Min.	75°C Max.	UNIT	CONDITIONS AND COMMENTS
V_{OH}	Output High Voltage	2.4		2.4	3		2.4		V	V_{CC} = 4.75V I_{OH} = -0.6 mA
V_{OL}	Output Low Voltage		0.45		0.21	0.45		0.45	V	V_{CC} = 4.75V I_{OL}=14.1mA(Pin15 I_{OL}=12.95mA(Pin1
										V_{CC} = 5.25V I_{OL}=16 mA (Pin15 I_{OL}=14.4mA(Pin14
V_{IH}	Input High Voltage	1.9		1.8			1.6		V	Guaranteed Input High Threshold fo All Inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	V	Guaranteed Input Low Threshold fo All Inputs
I_F	Input Load Current		-1.6		-1	-1.6		-1.6	mA	V_{CC} = 5.25V V_F = 0.45V
I_R	Input Leakage Current		60		15	60		60	µA	V_{CC} = 5.25V V_R = 4.5V
I_{SC}	Output Short Circuit Current	-30	-100	-30		- 100	-30	-100	mA	V_{CC} = 5.25V Output Grounded
I_{PD}	Power Dissipation Current		43			43		43	mA	V_{CC} = 5V

ELECTRICAL CHARACTERISTICS (-55°C to 125°C, V_{CC} =5V ± 10%)

Symbol	CHARACTERISTICS	LIMITS -55°C Min.	-55°C Max.	25°C Min.	25°C Typ.	25°C Max.	125°C Min.	125°C Max.	UNIT	CONDITIONS AND COMMENTS
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		V	V_{CC} = 4.5V I_{OH}=-0.6 mA
V_{OL}	Output Low Voltage		0.4		0.2	0.4		0.4	V	V_{CC} = 4.5V I_{OL}=12.4mA (Pin 1 I_{OL}=11.2mA (Pin 1
										V_{CC} = 5.5V I_{OL}=16 mA (Pin 1 I_{OL}=14.4mA (Pin 1
V_{IH}	Input High Voltage	2		1.7			1.4		V	Guaranteed Input High Threshold fo All Inputs
V_{IL}	Input Low Voltage		0.8			0.9		0.8	V	Guaranteed Input Low Threshold fo All Inputs
I_F	Input Load Current		-1.6		-1.1	-1.6		-1.6	mA	V_{CC} = 5.5V V_F = 0.4V
I_R	Input Leakage Current		60		15	60		60	µA	V_{CC} = 5.5V V_R = 4.5V
I_{SC}	Output Short Circuit Current	-30	-100	-30		-100	-30	-100	mA	V_{CC} = 5.5V Output Grounded
I_{PD}	Power Dissipation Current		40			40		40	mA	V_{CC} = 5V

FUNCTIONAL DESCRIPTION

The T 163 is a logic implementation of a single pole - 8 position switch with the switch position controlled by the state of three select inputs, S_0, S_1, S_2. Both assertion and negation outputs are provided. The enable input (E) is active low. When it is not activated the negation output is high and the assertion output is low regardless of all other inputs.
The logic function provided at the output is :

$$Z = E \cdot (I_0 \cdot \bar{S}_0 \cdot \bar{S}_1 \cdot \bar{S}_2 + I_1 \cdot S_0 \cdot \bar{S}_1 \cdot \bar{S}_2 + I_2 \cdot \bar{S}_0 \cdot S_1 \cdot \bar{S}_2 + I_3 \cdot S_0 \cdot S_1 \cdot \bar{S}_2 + I_4 \cdot \bar{S}_0 \cdot \bar{S}_1 \cdot S_2 + I_5 \cdot S_0 \cdot \bar{S}_1 \cdot S_2 + I_6 \cdot \bar{S}_0 \cdot S_1 \cdot S_2 + I_7 \cdot S_0 \cdot S_1 \cdot S_2).$$

The T 163 provides the ability, in one package, to select from eight sources of data or control information.
By proper manipulation of the inputs, the T 163 can provide any logic function of four variables and its negation.
Thus any number of random topic elements used to generate unusual truth tables can be replaced by one T 163.

E	S_2	S_1	S_0	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	$\bar{Z}$	Z
H	X	X	X	X	X	X	X	X	X	X	X	H	L
L	L	L	L	L	X	X	X	X	X	X	X	H	L
L	L	L	L	H	X	X	X	X	X	X	X	L	H
L	L	L	H	X	L	X	X	X	X	X	X	H	L
L	L	L	H	X	H	X	X	X	X	X	X	L	H
L	L	H	L	X	X	L	X	X	X	X	X	H	L
L	L	H	L	X	X	H	X	X	X	X	X	L	H
L	L	H	H	X	X	X	L	X	X	X	X	H	L
L	L	H	H	X	X	X	H	X	X	X	X	L	H
L	H	L	L	X	X	X	X	L	X	X	X	H	L
L	H	L	L	X	X	X	X	H	X	X	X	L	H
L	H	L	H	X	X	X	X	X	L	X	X	H	L
L	H	L	H	X	X	X	X	X	H	X	X	L	H
L	H	H	L	X	X	X	X	X	X	L	X	H	L
L	H	H	L	X	X	X	X	X	X	H	X	L	H
L	H	H	H	X	X	X	X	X	X	X	L	H	L
L	H	H	H	X	X	X	X	X	X	X	H	L	H

H = High voltage level L = Low voltage level
X = Level does not affect output

LOADING RULES

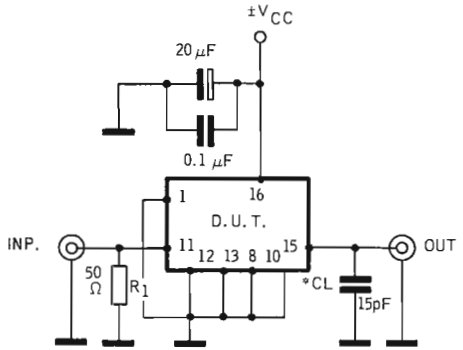
(1 U.L. = 1 TTL Gate Input Unit Load)

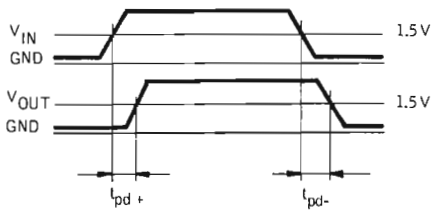
INPUTS : 1, 2, 3, 4, 5, 6, 7, 9, 10, 11, 12, 13 — LOADING FACTOR : 1 U.L.
OUTPUT: 15 — DRIVING FACTOR : 10 U.L.
OUTPUT: 14 — DRIVING FACTOR : 9 U.L.

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	CHARACTERISTICS	Min.	Typ.	Max.	UNIT	CONDITIONS AND COMMENTS	
tpd+	Turn - Off Delay		23	34	nsec	V_{CC} = 5V	C_L = 15 pF
tpd-	Turn - On Delay		25	36	nsec	V_{CC} = 5V	C_L = 15 pF

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS



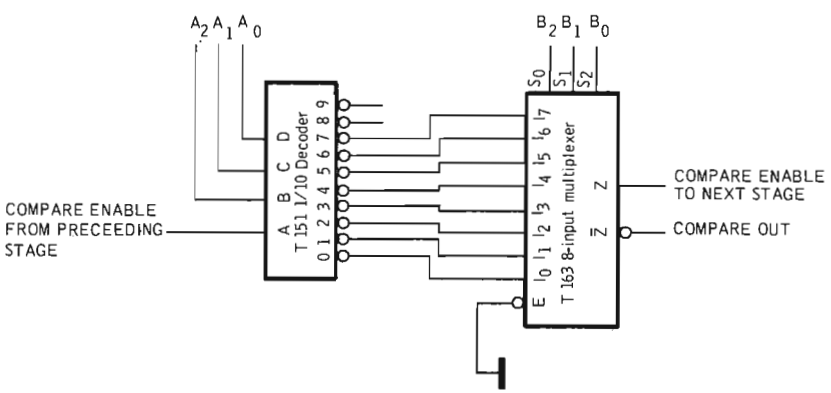


* The capacitance shall be within ± 5% including jig, probe and wiring capacitance.

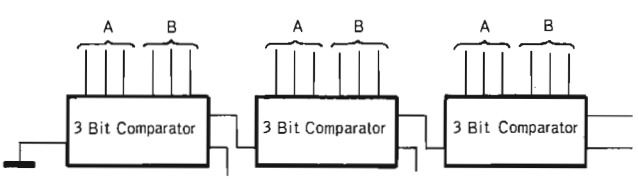
APPLICATIONS :

3 BIT COMPARATOR

Three bits of data to be compared are supplied to the address and select inputs of the T 151 and T 163 respectively.
If A_0, A_1, A_2 and B_0, B_1, B_2 compare, the mutually exclusive active low output of the T 151 1/10 decoder and the selected in put of the T 163 multiplexer will be coincidental and COMPARE OUT will be high. The COMPARE ENABLE must be low t permit compare operation.



INTERCONNECTION DIAGRAM FOR 9 BITS



Dual four-input multiplexer

EXTENDED TEMPERATURE RANGE
-55°C to 125°C
STANDARD TEMPERATURE RANGE
0°C to 75°C

- TYPICAL PROPAGATION DELAY 25 ns
- ON-CHIP SELECT LOGIC DECODING
- FULLY BUFFERED COMPLEMENTARY OUTPUTS
- INPUT CLAMPING DIODES
- CERAMIC OR PLASTIC 16 PIN DUAL-IN-LINE PACKAGE
- COMPATIBLE WITH ALL DTL AND TTL FAMILY PRODUCTS

The T 164 is a monolithic, high speed dual four input digital multiplexer circuit. It consists of two multiplexing circuits with common input select logic, and each circuit contains four inputs and fully buffered complementary outputs. Active pullups in the outputs ensure high drive and high speed performance. Because of its high speed performance and on-chip select decoding the T164 may be cascaded to multiple levels so that any number of lines can be multiplexed onto a single output bus. The circuit utilizes TTL logic for high speed and high fanout capability, and is compatible with all DTL and TTL family products.

ABSOLUTE MAXIMUM RATINGS
(above which the useful life may be impaired)

Supply Voltage, Continuous	-0.5V to 7V
Input Voltage	-0.5V to 5.5V
Output Voltage	-0.5V to V_{CC}
Storage Temperature Range (Ceramic DIP)	-65°C to 150°C
Storage Temperature Range (Plastic DIP)	-55°C to 125°C

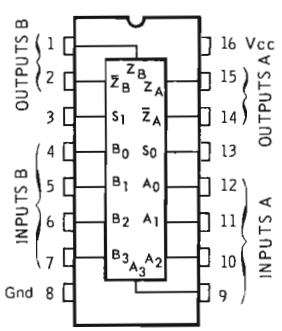
OPERATING CONDITIONS

Extended	
Temperature Range	-55°C to 125°C
Supply Voltage	5V ± 10%
Standard	
Temperature Range	0°C to 75°C
Supply Voltage	5V ± 5%

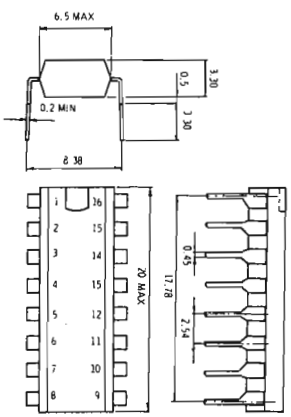
ORDERING NUMBERS

T 164 D1 (Ceramic DIP Standard Temperature Range)
T 164 D2 (Ceramic DIP Extended Temperature Range)
T 164 B1 (Plastic DIP Standard Temperature Range)

CONNECTION DIAGRAM
(Top view)

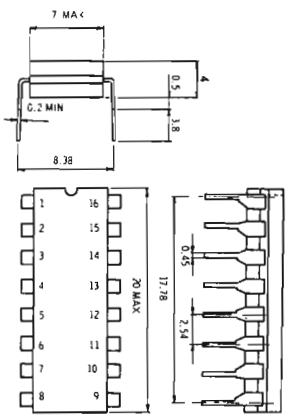


PHYSICAL DIMENSIONS
16 - pin plastic DIP



Note : all dimensions in mm.

PHYSICAL DIMENSIONS
16 - pin ceramic DIP



Note : all dimensions in mm.

ELECTRICAL CHARACTERISTICS (T_A = 0°C to 75°C, V_{CC} = 5V ± 5%)

SYMBOL	CHARACTERISTICS	Min.	Typ.	Max.	Unit	CONDITIONS
V_{OH}	Output High Voltage	2.4	3.0		V	V_{CC} = 4.75V I_{OH}= -1.2mA (Pins 1-15) V_{CC} = 4.75V I_{OH}=-1.08mA (Pins 2-14)
V_{OL}	Output Low Voltage		0.21	0.45	V	V_{CC} = 5.25V I_{OL}= 16mA (Pins 1-15) I_{OL}= 14.4mA (Pins 2-14) V_{CC} = 4.75V I_{OL}= 14.1mA (Pins 1-15) I_{OL}= 12.7mA (Pins 2-14)
V_{IH}	Input High Voltage	1.9			V	Guaranteed input high threshold for all inputs.
V_{IL}	Input Low Voltage			0.85	V	Guaranteed input low threshold for all inputs.
I_F	Input Load Current		-1.1	-1.6	mA	V_{CC} = 5.25V V_F= 0.45V
I_R	Input Reverse Current		15	60	µA	V_{CC} = 5.25V V_R= 4.5
I_{PDH}	Power Dissipation Current		30	43	mA	V_{CC} = 5V All inputs high.

ELECTRICAL CHARACTERISTICS (T_A = -55°C to 125°C; V_{CC} = 5V ± 10%)

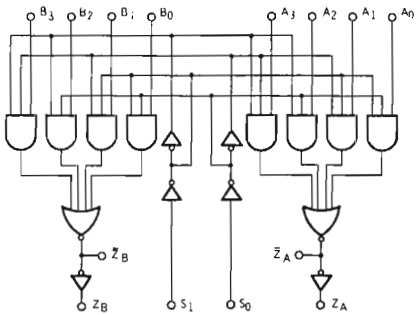
SYMBOL	CHARACTERISTICS	Min.	Typ.	Max.	Unit	CONDITIONS
V_{OH}	Output High Voltage	2.4	2.7		V	V_{CC} = 4.5V I_{OH}= -1.2mA (Pins 1-15) V_{CC} = 4.5V I_{OH}= -1.08mA (Pins 2-14)
V_{OL}	Output Low Voltage		0.21	0.4	V	V_{CC} = 5.5V I_{OL}= 16mA (Pins 1-15) I_{OL}= 14.4mA (Pins 2-14) V_{CC} = 4.5V I_{OL}= 12.4mA (Pins 1-15) I_{OL}= 11.2mA (Pins 2-14)
V_{IH}	Input High Voltage	2.0			V	Guaranteed input high threshold for all inputs.
V_{IL}	Input Low Voltage			0.8	V	Guaranteed input low threshold for all inputs.
I_F	Input Load Current		- 1.0	-1.6	mA	V_{CC} = 5.5V V_F= 0.4V
I_R	Input Reverse Current		10	60	µA	V_{CC} = 5.5V V_R= 4.5V
I_{PDH}	Power Dissipation Current		30	40	mA	V_{CC} = 5V All inputs high.

TRUTH TABLE

INPUTS						OUTPUTS	
S_0	S_1	A_0	A_1	A_2	A_3	Z_A	$\overline{Z}_A$
L	L	L	X	X	X	L	H
L	L	H	X	X	X	H	L
H	L	X	L	X	X	L	H
H	L	X	H	X	X	H	L
L	H	X	X	L	X	L	H
L	H	X	X	H	X	H	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	H	L

INPUTS						OUTPUTS	
S_0	S_1	B_0	B_1	B_2	B_3	Z_B	$\overline{Z}_B$
L	L	L	X	X	X	L	H
L	L	H	X	X	X	H	L
H	L	X	L	X	X	L	H
H	L	X	H	X	X	H	L
L	H	X	X	L	X	L	H
L	H	X	X	H	X	H	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	H	L

LOGIC DIAGRAM



L = LOW VOLTAGE LEVEL
H = HIGH VOLTAGE LEVEL
X = DON'T CARE

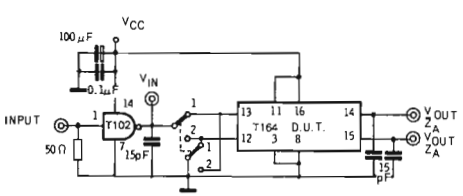
LOADING RULES (1 U.L. = 1 TTL GATE INPUT UNIT LOAD)

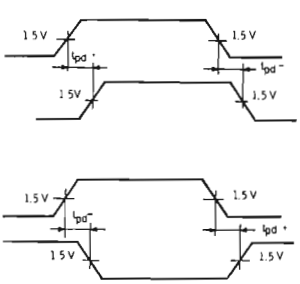
INPUTS : ALL — LOADING FACTOR : 1 U.L.
OUTPUTS: 1.15 — DRIVING FACTOR : 10 U.L.
OUTPUTS: 2.14 — DRIVING FACTOR : 9 U.L.

SWITCHING CHARACTERISTICS (T_A = 25°C)

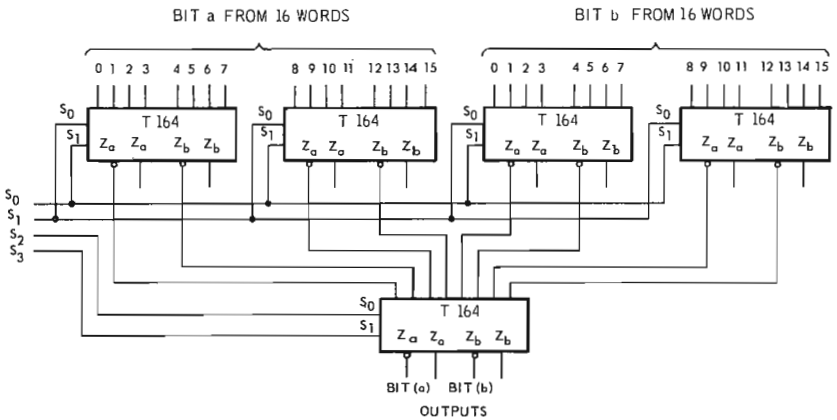
SYMBOL	CHARACTERISTICS	Min.	Typ.	Max.	Unit	CONDITIONS AND COMMENTS
t_{pd}	Turn-Off and On Delay S to Z		24	32	ns	See Test Circuit
t_{pd}	Turn-Off and On Delays S to $\overline{Z}$		18		ns	
t_{pd}	Turn-Off and On Delays A or B to $\overline{Z}$		14		ns	

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

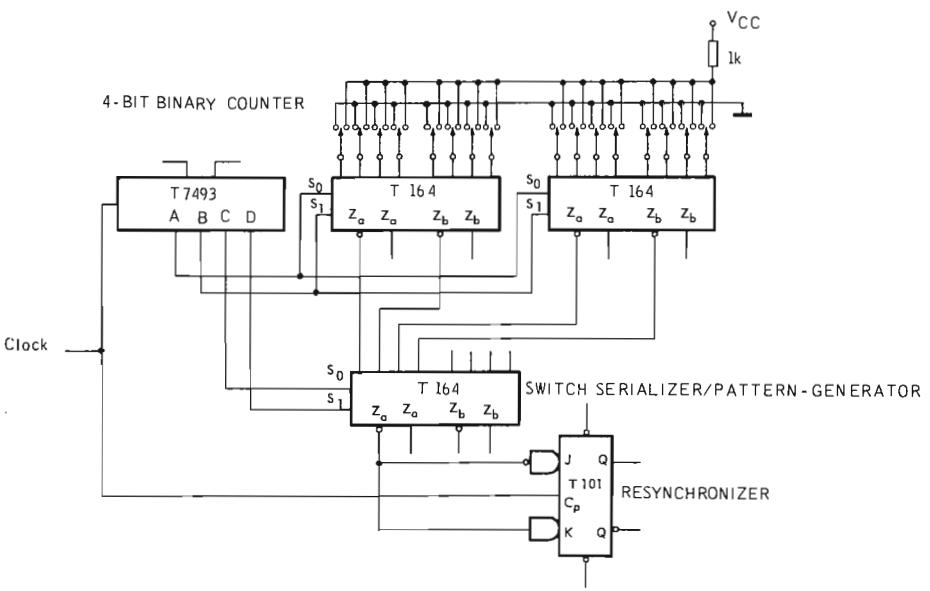




APPLICATIONS



A. Five T164's provide switching of data from sixteen two-bit words onto a two-bit output data bus. The selection of which bit to be transferred is made by the address inputs S_0, S_1, S_2 and S_3.



B. Sixteen-bit pattern generator

64-bit random access memory

STANDARD TEMPERATURE RANGE
0°C to 85°C

- FAST ACCESS TIME: 60nsec
- LOW POWER DISSIPATION: 6mW/BIT
- DTL AND TTL COMPATIBLE
- FULLY DECODED: ON CHIP ADDRESS, DECODE AND BUFFER
- CERAMIC 16-PIN DUAL IN-LINE PACKAGE
- OUTPUT OPEN COLLECTORS ALLOW WIRED-OR CAPABILITY FOR WORD EXPANSION
- SIMPLE MEMORY EXPANSION: CHIP SELECT INPUT LEAD
- MINIMUM LINE REFLECTION: LOW VOLTAGE INPUT CLAMP DIODES

The T 165 is a 64-bit random access memory. Its high speed makes it ideal in scratch pad applications. The use of Schottky barrier diode clamped transistors to obtain fast switching speeds results in higher performance than with a gold diffusion process. The T 165 is packaged in a hermetically sealed 16-pin dual in-line package, and its performance is specified over a temperature range from 0° to 85°C. The memory is organized as a 16-word by 4-bit array. The storage flip-flops are addressed through an on chip 1 out of 16 binary decoder using four input address leads. A separate Chip Select lead allows easy selection of an individual package when outputs are OR-tied. In addition to the address leads and the Chip Select lead, there is a write input which allows data presented at the data leads to be entered at the addressed storage cells.

ABSOLUTE MAXIMUM RATINGS
(above which the useful life may be impaired)

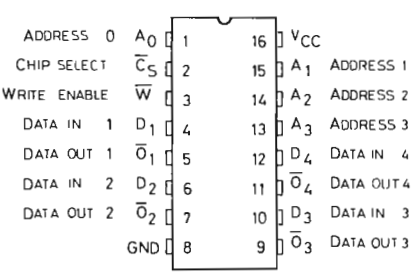
Supply Voltage (V_{CC}) Continuous	-0.5V to 7V
Input Voltage	5.25V
Storage Temperature Range	-65°C to 150°C
Temperature (Case) Under Bias	-55°C to 125°C

OPERATING CONDITIONS

Temperature Range	0°C to 85°C
Supply Voltage	5V ±5%

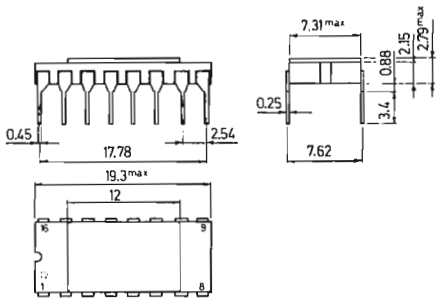
ORDERING NUMBER
T165 DI

CONNECTION DIAGRAM
(top view)



E-0007

PHYSICAL DIMENSIONS
16 - lead ceramic DIP



Note : all dimensions in mm.

ELECTRICAL CHARACTERISTICS (0°C to 85°C, V_{CC} = 5V ± 5%)

SYMBOL	CHARACTERISTICS	Min.	Typ.	Max.	Unit	CONDITIONS
V_{OL}	Output Low Voltage			0.45	V	V_{CC} = 4.75V $V_W = V_{IL}$ $V_S = V_D$ = 2.5V I_{OL} = 15mA
						V_{CC} = 4.75V $V_S = V_W$=GND $V_D = V_{IH}$ I_{OL} = 15mA
I_{CEX}	Output Leakage Current			100	µA	V_{CC} = 5.25V V_{CEX} = 5.25V V_S = 2.5V $V_W = V_{IH}$ V_D = GND
						V_{CC} = 5.25V V_{CEX} = 5.25V $V_S = V_W$ = GND $V_D = V_{IL}$
V_{IH}	Input High Voltage	2			V	Guaranteed high threshold voltage
V_{IL}	Input Low Voltage			0.85	V	Guaranteed low threshold voltage
I_{FD}	Input Load Current Data			-1.6	mA	V_{CC} = 5.25V V_{IN} = 0.45V V_W = GND
I_F	Input Load Current A-W-C_S			-1.6	mA	V_{CC} = 5.25V V_{IN} = 0.45V
I_{RD}	Input Reverse Current Data			40	µA	V_{CC} = 5.25V V_{IN} = 5.25V V_W = 2.5V
I_R	Input Reverse Current A-W-C_S			40	µA	V_{CC} = 5.25V V_{IN} = 5.25V
V_{FC}	Input Clamp Voltage			-1	V	V_{CC} = 4.75V I_{IN} = -5mA
C_{IN}	Input Capacitance (All Pins)		6		pF	V_{IN} = 2V
C_{OUT}	Output Capacitance		8		pF	V_{OUT} = 2V
I_{PD}	Power Dissipation Current			110	mA	V_{CC} = 5.25V $V_A = V_S = V_D$=GND

SWITCHING CHARACTERISTICS (T_A = 0°C to 85°C, V_{CC} = 5V)

SYMBOL	CHARACTERISTICS	Min.	Typ.	Max.	Unit	CONDITIONS
$T_{A(CS)}$	Read Access Time From Chip Select			60	ns	Figure 3
$T_{R(CS)}$	Recovery Time From Chip Select			60	ns	Figure 3
$T_{A(A)}$	Read Access Time From Address			60	ns	Figure 4
$T_{R(A)}$	Recovery Time From Address			60	ns	Figure 4
T_{WP}	Write Pulse Width	40			ns	Figure 2
T_{WR}	Write Recovery Time			50	ns	Figure 2
T_{DO}	Data To Output Delay			25	ns	V_W = GND Figure 5

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS

Condition of test :

Input pulse amplitude 2.5V

Input pulse rise and fall time must be 5nsec between 1V and 2V

Speed measurements are made at 1.5V levels

FIG. 1

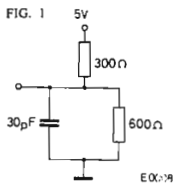
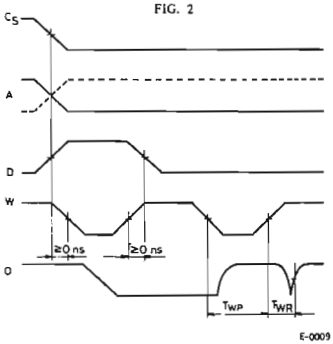


FIG. 2

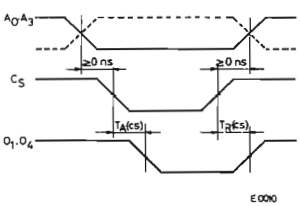


OPERATION

READ: The memory is addressed through A_0-A_3 which select one of the 16 words. The chip is enabled by placing chip select (C_S) to logic "0". If the write enable (W) is at a logic "1" the four stored bits are read out of 0_1-0_4 in parallel.

WRITE: The memory is addressed through A_0-A_3 which select one of the 16 words. The chip is enabled by placing C_S to logic "0". If the W is at a logic "0", the data on terminals D_1-D_4 is written into the addressed word in parallel and in complementary form. When W returns to logic "1", the information that was written in is now read out. However, each bit readout is the complement of what was written.

FIG. 3



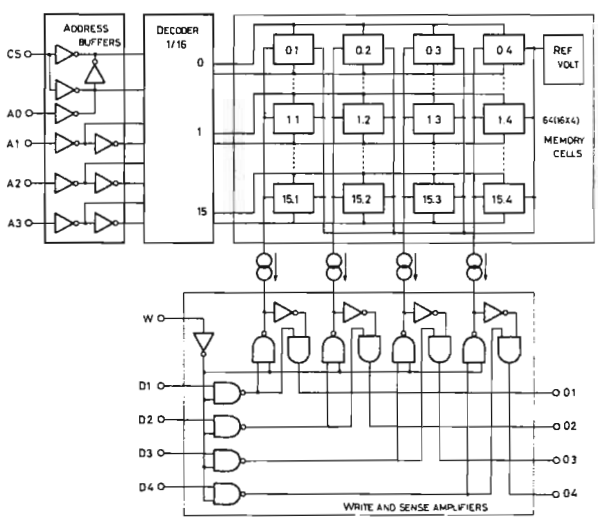


FIG. 6

FIG. 4

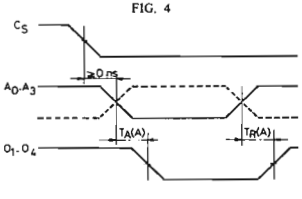
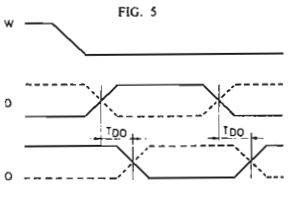
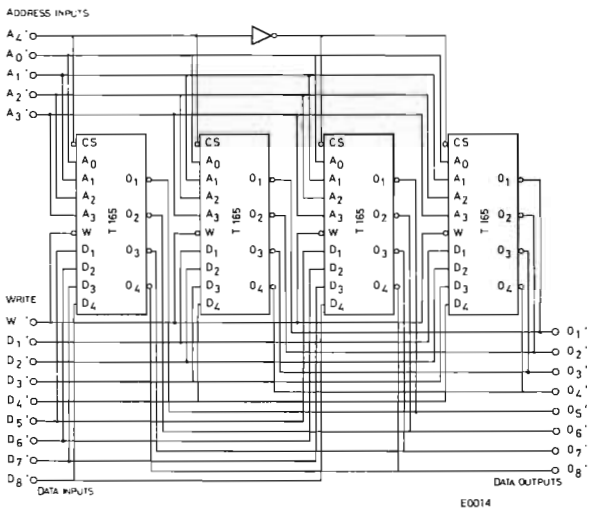


FIG. 5



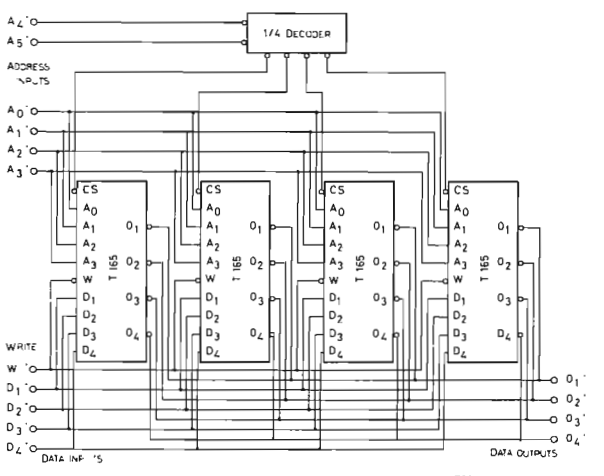
32 WORD x 8 BIT MEMORY

Two T 165 devices are used to increase the number of bits per word to 8. This is accomplished by connecting the Chip Select and Address inputs in parallel.To increase the number of words to 32, two of such parallel combinations are used.



64 WORD x 4 BIT MEMORY

The 64 word memory is made up of 4 T 165 memory devices. Word expansion is made possible by utilizing the Chip Select input as an additional address line. A 1 out of 4 decoder is used to drive the Chip Select input, and the outputs of each T 165 are OR-tied.



TTL INTEGRATED CIRCUIT

T 167

PRELIMINARY DATA

9 - BIT PARITY GENERATOR AND CHECKER

- BOTH EVEN AND ODD OUTPUT AVAILABLE
- HIGH VERSATILITY PROVIDED
- INPUT CLAMPING DIODES
- 14-PIN CERAMIC OR PLASTIC DUAL IN-LINE PACKAGE
- COMPATIBLE WITH ALL DTL AND TTL FAMILY PRODUCTS

The T 167, 9-input parity generator/parity checker, is a versatile MSI device commonly used to detect errors in data transmission or data retrieval. Two outputs (EVEN and ODD) are provided for versatility. An INHIBIT input is provided to disable both outputs of the T 167 (a logic 1 on the INHIBIT input forces both outputs to a logic 0).

When used as a parity generator, the T 167 supplies a parity bit which is transmitted together with the data word.

At the receiving end, the T 167 acts as a parity checker and indicates that data has been received correctly or that an error has been detected. Available in standard temperature range (0 to 75 °C), it comes in plastic and ceramic dual in-line package similar to Jedec TO-116.

ABSOLUTE MAXIMUM RATINGS

V_{CC}	Supply voltage, continuous	-0.5 to 7	V
V_i	Input voltage	-0.5 to 5.5	V
V_o	Output voltage	-0.5 to 5.5	V
T_{op}	Operating temperature	0 to 75	°C
T_{stg}	Storage temperature		
	for ceramic package	- 65 to 150	°C
	for plastic package	- 55 to 125	°C

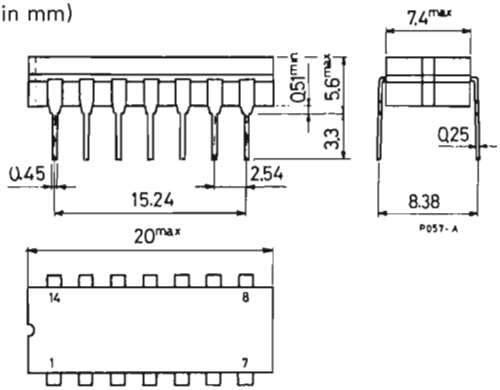
ORDERING NUMBERS

T 167 D1 (for ceramic dual in-line package and standard temperature range)
T 167 B1 (for plastic dual in-line package and standard temperature range)

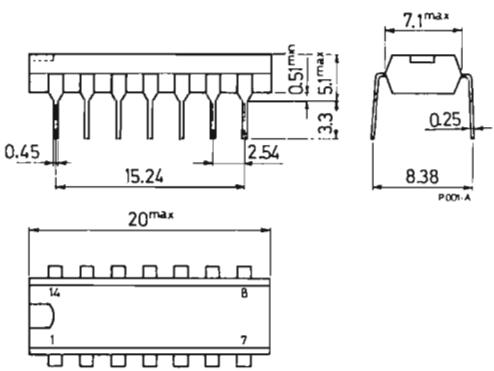
T167

MECHANICAL DATA (Dimensions in mm)

Ceramic dual in-line package
(similar to TO-116)

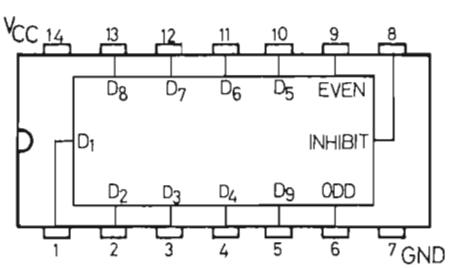


Plastic dual in-line package
(similar to TO-116)

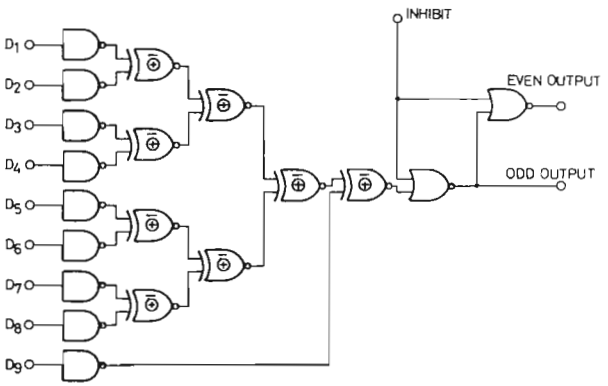


CONNECTION DIAGRAM

(top view)



FUNCTIONAL LOGIC DIAGRAM



TRUTH TABLE

INPUTS			OUTPUTS	
D_9	INHIBIT	Σ of 1's at D_1 thru D_8	EVEN	ODD
X	1	X	0	0
1	0	EVEN	0	1
1	0	ODD	1	0
0	0	EVEN	1	0
0	0	ODD	0	1

X : any level present at those inputs does not affect the output.

RECOMMENDED OPERATING CONDITIONS

V_{CC}	Supply voltage	4.75 to 5.25	V
T_{op}	Operating temperature	0 to 75	°C

ELECTRICAL CHARACTERISTICS

(over recommended operating conditions unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit	Fig.
V_{IH}	Input high voltage		2			V	1
V_{IL}	Input low voltage				0.8	V	1
V_{OH}	Output high voltage	EVEN $V_{CC} = 4.75V$ $V_i = 0.8V$ $I_{OH} = -800\ \mu A$ $V_{INHIBIT} = 0.8V$	2.6			V	1
		ODD $V_{CC} = 4.75V$ $V_i = 2V$ $I_{OH} = -800\ \mu A$ $V_{INHIBIT} = 0.8V$	2.6			V	
V_{OL}	Output low voltage	EVEN $V_{CC} = 4.75V$ $V_i = 2V$ $I_{OL} = 16$ mA $V_{INHIBIT} = 0.8V$			0.4	V	1
		ODD $V_{CC} = 4.75V$ $V_i = 0.8V$ $I_{OL} = 16$ mA $V_{INHIBIT} = 0.8V$			0.4	V	
I_{IL}	Input low current at data inputs	$V_{CC} = 5.25V$ $V_i = 0.4V$			-1.6	mA	2
I_{IH}	Input high current at data inputs	$V_{CC} = 5.25V$ $V_i = 5.5V$			1	mA	2
		$V_{CC} = 5.25V$ $V_i = 2.4V$			40	µA	
I_{IL}	Input low current at inhibit input	$V_{CC} = 5.25V$ $V_i = 0.4V$			-3.2	mA	2
I_{IH}	Input high current at inhibit input	$V_{CC} = 5.25V$ $V_i = 5.5V$			1	mA	2
		$V_{CC} = 5.25V$ $V_i = 2.4V$			80	µA	
I_{SC}*	Short-circuit output current	$V_{CC} = 5.25V$ $V_{INHIBIT} = 0.8V$	-20		-70	mA	3
I_{CC}	Power supply current	$V_{CC} = 5.25V$			70	mA	3

* Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_{amb} = 25°C, N = 10)

Parameter		Test Conditions **		Min.	Typ.	Max.	Unit
		from input	to output				
t_{pd1}	Propagation delay time to logical 1 level	Data 1-8	Even		38	55	ns
		Data 1-8	Odd		32	45	ns
		Data 9	Even		23	40	ns
		Data 9	Odd		20	35	ns
		Inhibit	Even or Odd		10	18	ns
t_{pd0}	Propagation delay time to logical 0 level	Data 1-8	Even		35	50	ns
		Data 1-8	Odd		30	45	ns
		Data 9	Even		20	35	ns
		Data 9	Odd		15	30	ns
		Inhibit	Even or Odd		8	15	ns

** See switching times test circuit, waveforms and truth table.

DC TEST CIRCUITS (arrows indicate actual direction of current flow. Current into a terminal is a positive value).

Fig. 1 - V_{IH}, V_{IL}, V_{OH}, V_{OL}

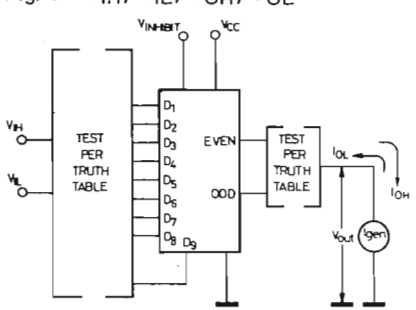
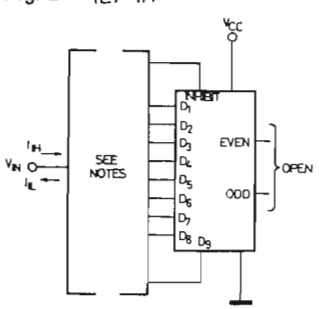


Fig. 2 - I_{IL}, I_{IH}

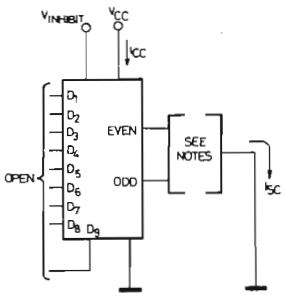


Each input is tested separately.

DC TEST CIRCUITS (continued)

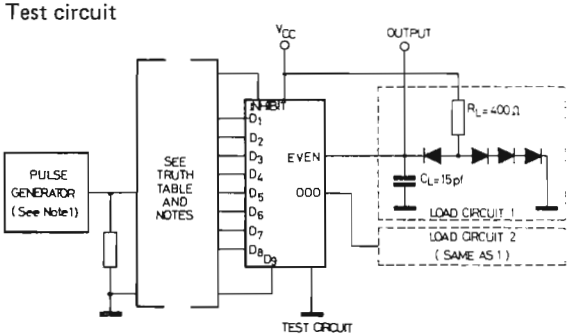
When testing I_{SC} each output is tested separately in accordance with the truth table. When testing I_{CC} both outputs are open.

Fig. 3 - I_{SC}, I_{CC}



SWITCHING TIMES

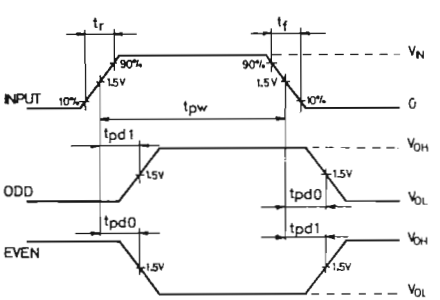
Test circuit



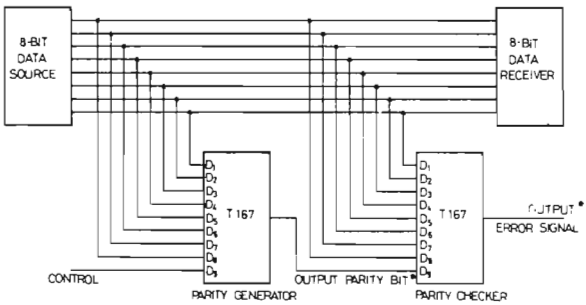
NOTES :

1. The pulse generator has the following characteristics : $V_i = 3V$, $t_r = t_f = 10$ ns, $t_{pw} = 500$ ns, PRR = 1 MHz and $Z_{out} \approx 50\Omega$
2. C_L includes probe and jig capacitance.
3. All diodes are 1N3064.

Waveforms



TYPICAL APPLICATION



* Output can be conditioned for odd or even parity. An "even parity bit" checking code has a parity bit such that the sum of the 1's in the data word plus the parity bit is always an even number.
An "odd parity bit" checking code has a parity bit such that the sum of the 1's in the data word plus the parity bit is always an odd number.

TTL INTEGRATED CIRCUIT

T 172

PRELIMINARY DATA

QUAD LINE RECEIVER

- INPUT CLAMP DIODES
- ACTIVE OUTPUT PULL-UP
- TYP. POWER DISSIPATION 150 mW
- 14-PIN DUAL IN-LINE PLASTIC PACKAGE

The T 172 is a quad two-input line receiver, constructed on a single silicon chip using the planar epitaxial process. Compatible with other TTL and DTL family products, it combines high noise immunity with high logic speed. The T 172, available in standard temperature range (0 to 75°C), comes in a dual in-line plastic package similar to Jedec TO-116.

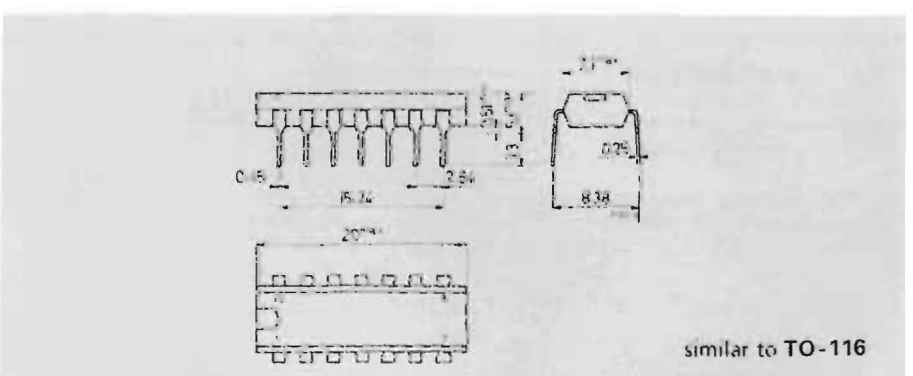
ABSOLUTE MAXIMUM RATINGS

V_{CC}	Supply voltage, continuous	-0.5 to 7	V
V_I	Input voltage	-0.5 to 5.5	V
V_o	Output voltage	-0.5 to 5.5	V
T_{op}	Operating temperature	0 to 75	°C
T_{stg}	Storage temperature	- 55 to 125	°C

ORDERING NUMBER : T 172 B1

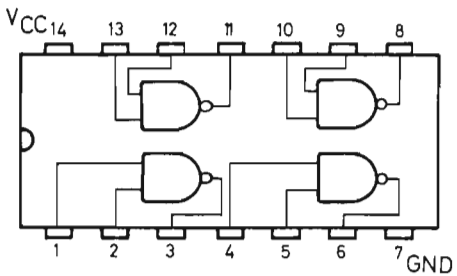
MECHANICAL DATA

Dimensions in mm



T172

CONNECTION DIAGRAM (top view)



RECOMMENDED OPERATING CONDITIONS

V_{CC}	Supply voltage	4.75 to 5.25	V
T_{op}	Operating temperature	0 to 75	°C

ELECTRICAL CHARACTERISTICS

(over recommended operating conditions unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_{IH}	Input high voltage	Guaranteed input high threshold for all inputs	2.6			V
V_{IL}	Input low voltage	Guaranteed input low threshold for all inputs			1.5	V
V_{OH}	Output high voltage	V_{CC} = 4.75V I_{OH} = -500μA V_{IL} = 1.5V Other input to V_{CC}	2.6			V
		V_{CC} = 4.75V I_{OH} = -500μA V_{IL} = 1.1V Other input to V_{CC}	2.8			V

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
V_{OL}	Output low voltage	V_{CC} = 4.75V I_{OL} =20 mA V_{IH} = 2.6V			0.4	V
I_{IH}	Input high current	V_{CC} = 5.25V V_{IH} = 2.6V V_{CC} = 5.25V V_{IH} = 5.5V			50 1	µA mA
I_{IL}	Input low current	V_{CC} = 5.25V V_{IL} = 0.4V			-2.0	mA
I_{SC}*	Short-circuit output current	V_{CC} = 5.25V Output and inputs grounded	-40		-100	mA
I_{CCH}	High level power supply current	V_{CC} = 5.25V Inputs high			50	mA
I_{CCL}	Low level power supply current	V_{CC} = 5.25V Inputs low			20	mA
V_C	Input clamp diode voltage	V_{CC} = 4.75V I_i = -12mA			-1.5	V

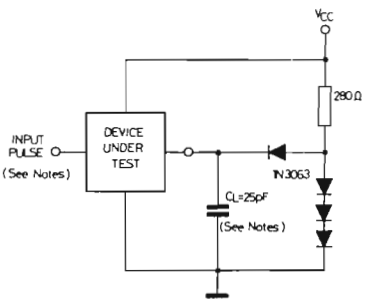
* Only one gate shorted at a time

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_{amb} = 25°C)

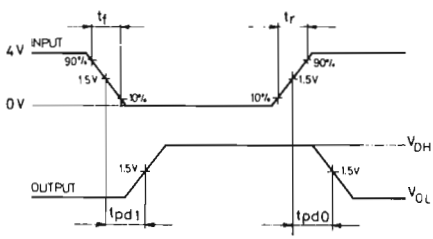
Parameter		Test Conditions	Min.	Typ.	Max.	Unit
t_{pd1}	Propagation delay time to logical "1"	See switching time test circuit and waveforms			12	ns
t_{pd0}	Propagation delay time to logical "0"				12	ns

SWITCHING TIMES

Test circuit



Waveforms



Notes :

- The input pulse has the following characteristics : P.R.R. 1MHz, duty cycle 50%, $t_f = t_r = 7$ ns
- C_L includes probe and jig capacitance.

Transistor transistor logic

STANDARD TEMPERATURE RANGE 0°C to 70°C

- COMPATIBLE WITH OTHER TTL or DTL FAMILY PRODUCTS
- NOISE IMMUNITY 1 V
- WORST CASE NOISE IMMUNITY 0.4 V
- OUTPUT DRIVE CAPABILITY OF 10
- POWER DISSIPATION 10mW PER GATE
- GATE PROPAGATION DELAY 10 nsec
- DUAL IN-LINE PLASTIC PACKAGE

The T7400 series of TTL integrated circuit combines high fan-out, high noise immunity, low power dissipation and low propagation delay times and can therefore be used in any digital system. The elements are available in plastic Dual In-line Packages.

ABSOLUTE MAXIMUM RATINGS
(above which the useful life may be impaired, see also note 1)

Supply Voltage V_{CC} (note 2)	7 V
Input Voltage V_{in} (note 2)	5.5 V
Storage Temperature Range	-65°C to 150°C

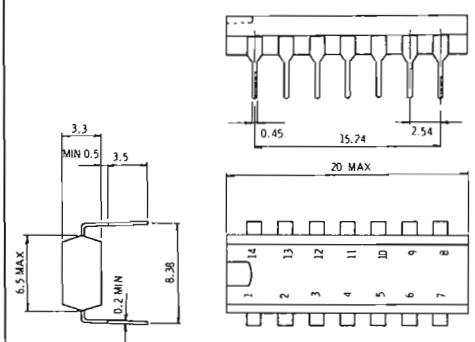
OPERATING CONDITIONS (note 1)

Temperature Range	0°C to 70°C
Supply Voltage V_{CC}	5V ± 5%
Normalised Fan-Out from each output, N	10

ORDERING NUMBER
T74XXB1 or T74XXXB1
(where 74XX or 74XXX is type number)

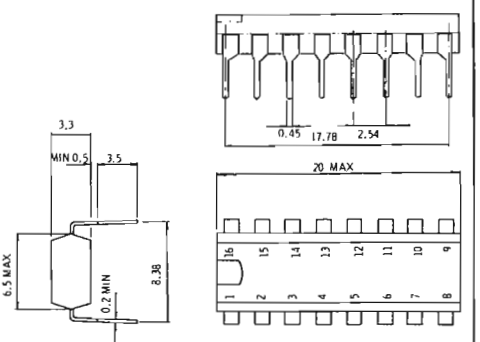
NOTES :
1) Abs.max.ratings and operating conditions appliable to particular devices, are listed under the device concerned.
2) Voltage values are with respect to network ground terminal.

PHYSICAL DIMENSIONS
14-pin plastic DIP



Note : all dimensions in mm.

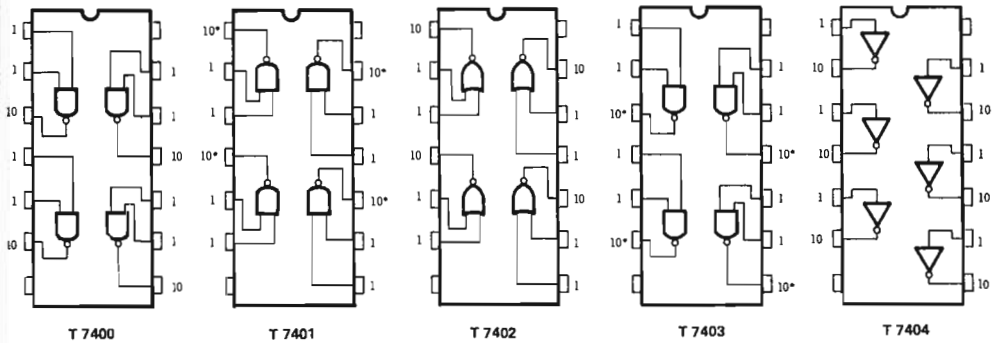
PHYSICAL DIMENSIONS
16-pin plastic DIP



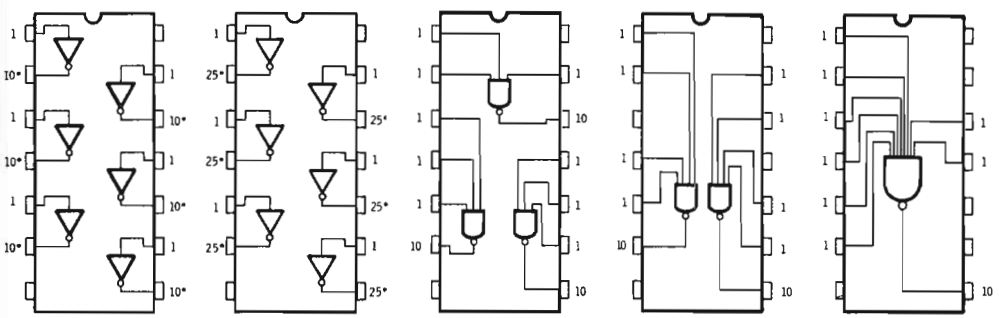
Note : all dimensions in mm.

INDEX

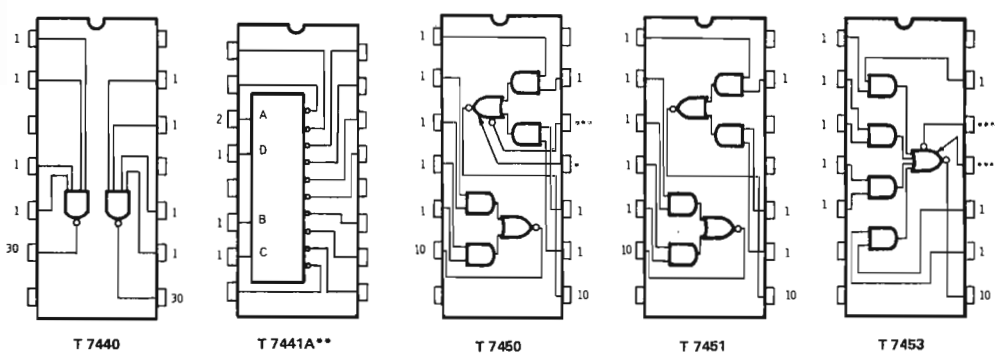
INPUT/OUTPUT LOAD/DRIVE FACTORS



T 7400 T 7401 T 7402 T 7403 T 7404



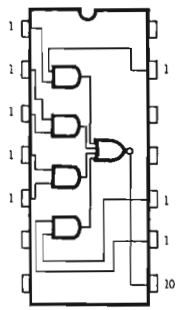
T 7405 T 7406/T 7416 T 7410 T 7420 T 7430



T 7440 T 7441A** T 7450 T 7451 T 7453

* These outputs are open collector transistors and, therefore, need external pull-up resistors.
** For output load capability, see electrical characteristics.
*** A total of four expander gates can be connected to the expander inputs.

INPUT/OUTPUT LOAD/DRIVE FACTORS (contd.)



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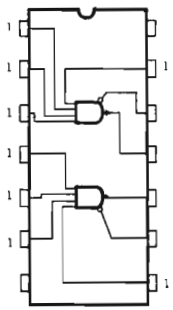

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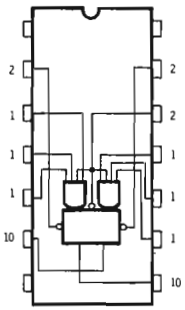

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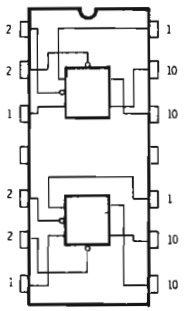
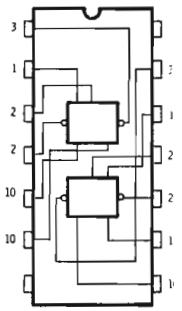


T 7473



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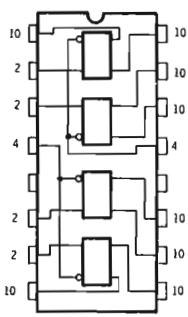

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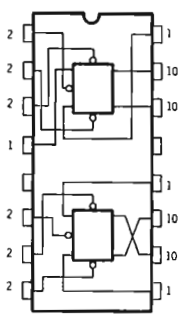

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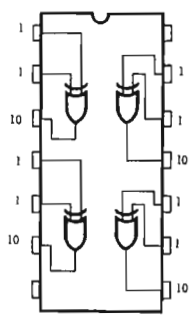

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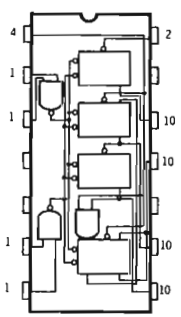
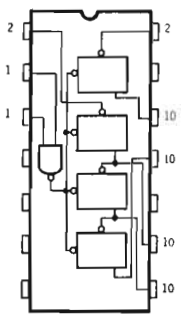


T 7490



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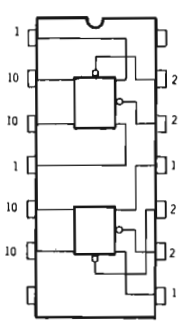

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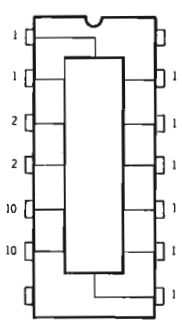
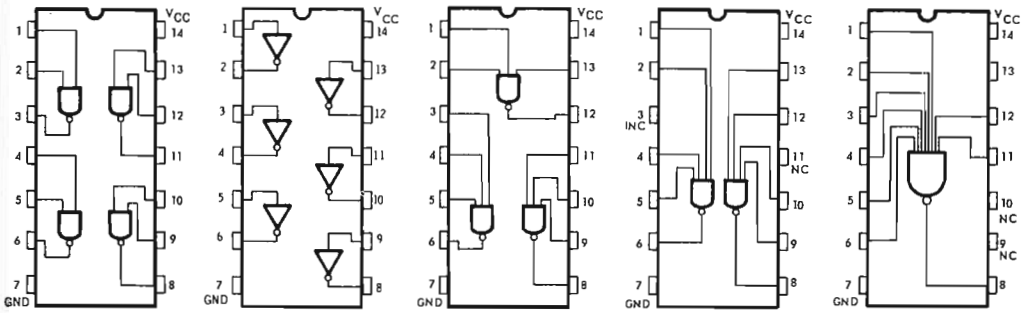


T 74180

CONNECTION DIAGRAMS (Top view)



T 7400 T 7404 T 7410 T 7420 T 7430

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

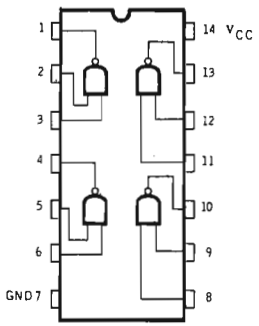
PARAMETER		TEST CONDITIONS (*)	MIN.	TYP.(**)	MAX.	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	V_{CC}= MIN	2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	V_{CC}= MIN			0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC}= MIN V_{in}= 0.8 V I_{load} = -400 µA	2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	V_{CC}= MIN V_{in}= 2 V I_{sink} = 16 mA		0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC}= MAX V_{in}= 0.4V			- 1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC}= MAX V_{in}= 2.4V V_{CC}= MAX V_{in}= 5.5V			40 1	µA mA
I_{OS}	Short circuit output current (***)	V_{CC}= MAX	- 18		- 55	mA
$I_{CC(0)}$	Logical 0 level supply current/gate	V_{CC}= MAX V_{in}= 5 V		3	5.5	mA
$I_{CC(1)}$	Logical 1 level supply current/gate	V_{CC}= MAX V_{in}= 0		1	2	mA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C, N = 10)

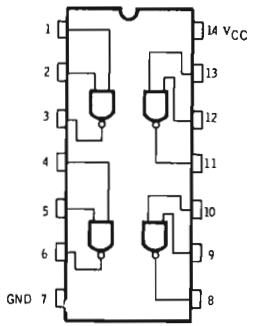
PARAMETER		Test Fig.	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{pd0}	Propagation delay time to logical 0 level	26	C_L =15pF R_L=400Ω		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	26	C_L =15pF R_L=400Ω		12	22	ns

(*) For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions.
(**) All typical values are at V_{CC} = 5V, T_A = 25°C.
(***) Not more than one output should be shorted at a time.

CONNECTION DIAGRAMS (Top view)



T 7401



T 7403

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS (*)	MIN.	TYP.(**)	MAX.	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 (on) level at output	V_{CC}= MIN	2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 (off) level at output	V_{CC}= MIN			0.8	V
$I_{out(1)}$	Output reverse current	V_{CC}= MIN V_{in} =0.8V $V_{out(1)}$ =5.5V			250	µA
$V_{out(0)}$	Logical 0 output voltage (on level)	V_{CC}= MIN V_{in}= 2 V I_{sink} = 16 mA			0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC}= MAX V_{in} =0.4 V			-1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC}= MAX V_{in} =2.4 V			40	µA
		V_{CC}= MAX V_{in} =5.5 V			1	mA
$I_{CC(0)}$	Logical 0 level supply current /gate	V_{CC}= MAX V_{in} = 5 V		3	5.5	mA
$I_{CC(1)}$	Logical 1 level supply current /gate	V_{CC}= MAX V_{in} = 0		1	2	mA

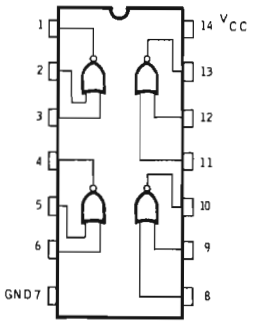
SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C, N = 10)

PARAMETER		Test Fig.	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{pd0}	Propagation delay time to logical 0 level	27	C_L=15pF R_L=400 Ω		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	27	C_L=15pF R_L=4KΩ		35	45	ns

(*) For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions

(**) All typical values are at V_{CC} = 5V, T_A = 25°C.

CONNECTION DIAGRAM (Top view)



T 7402

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

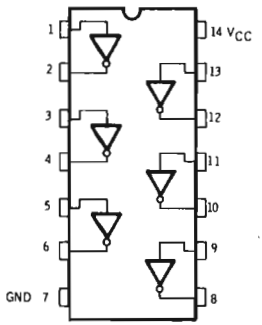
PARAMETER		TEST CONDITIONS (*)	MIN.	TYP.(**)	MAX.	UNIT
$V_{in(1)}$	Logical 1 input voltage required at either input terminal to ensure logical 0 level at output	V_{CC}= MIN	2			V
$V_{in(0)}$	Logical 0 input voltage required at both input terminals to ensure logical 1 level at output	V_{CC}= MIN			0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC}=MIN V_{in}= 0.8V I_{load} = - 400 µA	2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} =MIN V_{in}= 2 V I_{sink}= 16 mA		0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC}= MAX V_{in}= 0.4 V			-1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC}= MAX V_{in}= 2.4 V			40	µA
		V_{CC}= MAX V_{in}= 5.5 V			1	mA
I_{OS}	Short-circuit output current (***)	V_{CC}= MAX	-18		- 55	mA
$I_{CC(0)}$	Logical 0 level supply current	V_{CC}= MAX V_{in} = 5 V		14	27	mA
$I_{CC(1)}$	Logical 1 level supply current	V_{CC}= MAX V_{in} = 0		8	16	mA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C, N = 10)

PARAMETER		Test Fig.	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_{pd0}	Propagation delay time to logical 0 level	26	C_L=15pF R_L=400 Ω		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	26	C_L=15pF R_L=400 Ω		12	22	ns

(*) For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions
(**) All typical values are at V_{CC} = 5 V, T_A = 25°C
(***) Not more than one output should be shorted at a time.

CONNECTION DIAGRAM (Top view)



T 7405 - T 7406 - T 7416

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

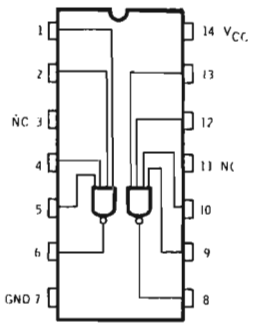
PARAMETER		TEST CONDITIONS (*)			Min.	Typ.(**)	Max.	Unit
$V_{in(1)}$	Logical 1 input voltage required at input terminal to ensure logical 0 (on) level at output	V_{CC} = MIN			2			V
$V_{in(0)}$	Logical 0 input voltage required at input terminal to ensure logical 1 (off) level at output	V_{CC} = MIN					0.8	V
$I_{out(1)}$	Output reverse current	V_{CC} = MIN, V_{in} = 0.8V	$V_{out(1)}$ = 5.5V	T7405			250	µA
			$V_{out(1)}$ = 30V	T7406				
			$V_{out(1)}$ = 15V	T7416				
$V_{out(0)}$	Logical 0 output voltage (on) level	V_{CC} = MIN, V_{in} = 2V, I_{sink} = 16mA					0.4	V
		V_{CC} = MIN, V_{in} = 2V, I_{sink} = 40 mA		T7406 T7416			0.7	
$I_{in(0)}$	Logical 0 level input current	V_{CC} = MAX, V_{in} = 0.4V					- 1.6	mA
$I_{in(1)}$	Logical 1 level input current	V_{CC} = MAX, V_{in} = 2.4V					40	µA
		V_{CC} = MAX, V_{in} = 5.5V					1	mA
$I_{CC(0)}$	Logical 0 level supply current/ gate	V_{CC} = 5V, V_{in} = 5V, T_A = 25°C		T7405		3	5.5	mA
				T7406 T7416		4.5	6.3	
$I_{CC(1)}$	Logical 1 level supply current/ gate	V_{CC} = 5V, V_{in} = 0, T_A = 25°C		T7405		1	2	mA
				T7406 T7416		5	7	

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_A = 25° C)

PARAMETER		Test Figure	TEST CONDITIONS		Min.	Typ.	Max.	Unit
t_{pd0}	Propagation delay time to logical 0 level	27	C_L = 15pF, R_L = 400Ω	T7405		8	15	ns
			C_L = 15pF, R_L = 110Ω	T7406 T7416		13	20	
t_{pd1}	Propagation delay time to logical 1 level	27	C_L = 15pF, R_L = 4K Ω	T7405		40	55	ns
			C_L = 15pF, R_L = 110Ω	T7406 T7416		17	26	

(*) For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
(**) All Typical values are at V_{CC} = 5V, T_A = 25°C.

CONNECTION DIAGRAM (Top view)



T 7440

ELECTRICAL CHARACTERISTICS (over recommended free-air temperature range unless otherwise noted)

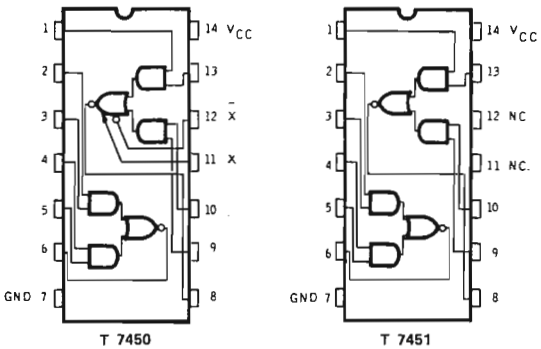
PARAMETER		TEST CONDITIONS (*)	Min.	Typ.(**)	Max.	Unit
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	V_{CC} = MIN	2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	V_{CC} = MIN			0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN V_{in} = 0.8V I_{load} = - 1.2mA	2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN V_{in} = 2V I_{sink} = 48mA		0.28	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX V_{in} = 0.4V			-1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = MAX V_{in} = 2.4V			40	µA
		V_{CC} = MAX V_{in} = 5.5V			1	mA
I_{OS}	Short-circuit output current (***)	V_{CC} = MAX	-18		-70	mA
$I_{CC(0)}$	Logical 0 level supply current	V_{CC} = MAX V_{in} = 5V		17	27	mA
$I_{CC(1)}$	Logical 1 level supply current	V_{CC} = MAX V_{in} = 0		4	8	mA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C, N = 30)

PARAMETER		TEST FIGURE	TEST CONDITIONS	Min.	Typ.	Max.	Unit
t_{pd0}	Propagation delay time to logical 0 level	26	C_L = 15pF R_L = 133 Ω		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	26	C_L = 15pF R_L = 133 Ω		13	22	ns

(*) For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions
(**) All typical values are at V_{CC} = 5V, T_A = 25°C.
(***) Not more than one output should be shorted at a time.

CONNECTION DIAGRAMS (Top view)



ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS (*)	MIN.	TYP.(**)	MAX.	UNIT
$V_{in(1)}$	Logical 1 input voltage required at both input terminals of either AND section to ensure logical 0 at output	V_{CC}= MIN	2			V
$V_{in(0)}$	Logical 0 input voltage required at one input terminal of each AND section to ensure logical 1 at output	V_{CC}= MIN			0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC}= MIN V_{in}= 0.8 V I_{load} = - 400 µA	2.4	3.3		V
Vout(0)	Logical 0 output voltage	V_{CC}= MIN V_{in}= 2 V I_{sink} = 16 mA		0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC}= MAX V_{in}= 0.4 V			- 1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC}= MAX V_{in}= 2.4 V			40	µA
		V_{CC}= MAX V_{in}= 5.5 V			1	mA
I_{OS}	Short-circuit output current (***)	V_{CC}= MAX	-18		- 55	mA
$I_{CC(0)}$	Logical 0 level supply current	V_{CC}= MAX V_{in} = 5 V		7.4	14	mA
$I_{CC(1)}$	Logical 1 level supply current	V_{CC}= MAX V_{in} = 0		4	8	mA

(*) For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions. Expander inputs X and $\overline{X}$ are open.

(**) All typical values are at V_{CC} = 5 V, T_A = 25°C.

(***) Not more than one output should be shorted at a time.

ELECTRICAL CHARACTERISTICS (T 7450 circuit) using expander inputs, V_{CC} = 4.75 V, T_A = 0°C

PARAMETER		Test Fig.	TEST CONDITIONS	MIN.	TYP.(**)	MAX.	UNIT
I_X	Expander current	1	V_I = 0.4V I_{sink}=16 mA			3.1	mA
$V_{BE(Q)}$	Base emitter voltage of output transistor (Q)	2	I_{sink}=16 mA I_I=0.62 mA R_I=0			1	V
$V_{out(1)}$	Logical 1 output voltage	3	I_{load}=-400µA I_I =-I_2 =270µA	2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	2	I_{sink}=16mA I_I= 0.43mA R_I = 130 Ω		0.22	0.4	V

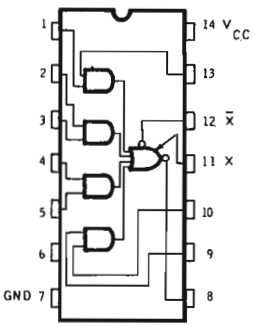
SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_A = 25° C, N = 10)

PARAMETER		Test Fig.	TEST CONDITIONS (*)	MIN.	TYP.	MAX.	UNIT
t_{pd0}	Propagation delay time to logical 0 level	28	C_L=15 pF R_L=400 Ω		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	28	C_L=15 pF R_L=400 Ω		13	22	ns

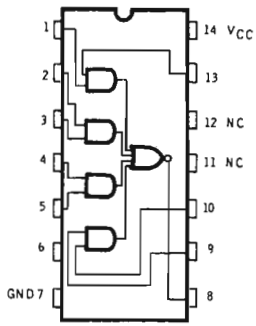
(*) Expander inputs X and $\overline{X}$ are open .

(**) All typical values are at V_{CC}=5 V, T_A=25°C .

CONNECTION DIAGRAMS (Top view)



T 7453



T 7454

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS (*)	MIN.	TYP.(**)	MAX.	UNIT
$V_{in(1)}$	Logical 1 input voltage required at both input terminals of one AND section to ensure logical 0 level at output	V_{CC}= MIN	2			V
$V_{in(0)}$	Logical 0 input voltage required at one input terminal of each AND section to ensure logical 1 level at output	V_{CC}= MIN			0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC}= MIN V_{in}= 0.8 V I_{load} = - 400 µA	2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN V_{in} = 2 V I_{sink} = 16 mA		0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX V_{in} =0.4 V			- 1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = MAX V_{in} =2.4 V			40	µA
		V_{CC} = MAX V_{in} =5.5 V			1	mA
I_{OS}	Short-circuit output current (***)	V_{CC} = MAX	- 18		- 55	mA
$I_{CC(0)}$	Logical 0 level supply current	V_{CC} = MAX V_{in} = 5 V		5.1	9.5	mA
$I_{CC(1)}$	Logical 1 level supply current	V_{CC} = MAX V_{in} = 0		4	8	mA

(*) For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions. Expander inputs X and $\overline{X}$ are open.

(**) All typical values are at V_{CC} = 5 V, T_A = 25°C.

(***) Not more than one output should be shorted at a time.

ELECTRICAL CHARACTERISTICS (T7453 circuit) using expander inputs, V_{CC} = 4.75 V, T_A = 0°C

PARAMETER		Test Fig.	TEST CONDITIONS	MIN.	TYP.(**)	MAX.	UNIT
I_X	Expander current	1	V_I =0.4V I_{sink}=10 mA			3.1	mA
$V_{BE(Q)}$	Base-emitter voltage of output transistor (Q)	2	I_{sink}=16mA I_I=0.62 mA R_I = 0			1	V
$V_{out(1)}$	Logical 1 output voltage	3	I_{load}=-400μA I_1=-I_2=270 μA	2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	2	I_{sink}=16 mA I_I=0.43 mA R_I= 130 Ω		0.22	0.4	V

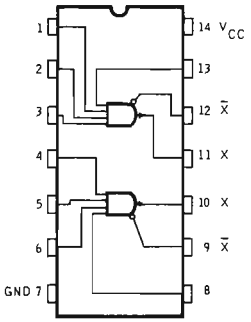
SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C, N = 10)

PARAMETER		Test Fig.	TEST CONDITIONS (*)	MIN.	TYP.	MAX.	UNIT
t_{pd0}	Propagation delay time to logical 0 level	28	C_L=15pF R_L=400 Ω		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	28	C_L=15pF R_L=400 Ω		13	22	ns

(*) Expander inputs X and $\overline{X}$ are open.

(**) All typical values, are at V_{CC} = 5V, T_A = 25°C.

CONNECTION DIAGRAM (Top view)



T 7460

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		Test Fig.	TEST CONDITIONS (*)	MIN.	TYP.(**)	MAX.	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure that the output is in the on state	4	V_{CC}=MIN	2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure that the output is in the off state	5	V_{CC}=MIN			0.8	V
V_{on}	On-state output voltage	4	V_{CC}=MIN V_{in} = 2 V V_I=1V R=1.1K T_A=0°C			0.4	V
I_{off}	Off-state output current	5	V_{CC}=MIN, V_{in}=0.8V, T_A=0°C V_I=4.5V R=1.2 K			270	µA
I_{on}	On-state output current	6	V_{CC}=MIN, V_{in}=2V, V_I=1V	-0.43			mA
$I_{in(0)}$	Logical 0 level input current (each input)		V_{CC}=MAX, V_{in}=0.4V			-1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)		V_{CC}=MAX, V_{in}=2.4V V_{CC}=MAX, V_{in}=5.5V			40 1	uA mA
$I_{CC(on)}$	On-state supply current	7	V_{CC}=MAX, V_{in}=5 V, V_I = 0.85 V		1.2	2.5	mA
$I_{CC(off)}$	Off-state supply current	7	V_{CC}=MAX, V_{in}= 0, V_I= 0.85 V		2	4	mA

(*) For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions.
(**) All typical values are at V_{CC} = 5V, T_A = 25°C.

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C, N = 10)

PARAMETER		Test Fig.	TEST CONDITIONS	MIN.	TYP.	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	29	C_L=15pF R_L=400 Ω		10	20	ns
t_{pd1}	Propagation delay time to logical 1 level	29	C_L=15pF R_L=400 Ω		15	30	ns

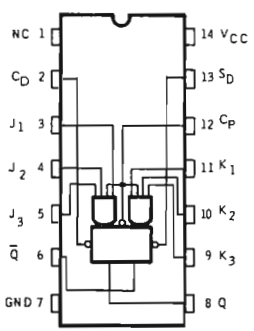
DESCRIPTION

This J-K flip-flop is based on the master-slave principle and has AND gate inputs for entry into the master section which is controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows :

1) Isolate slave from master.
2) Enter information from AND gate inputs to master.
3) Disable AND gate inputs.
4) Transfer information from master to slave.

CLOCK WAVEFORM

CONNECTION DIAGRAM (Top view)



T 7472

TRUTH TABLE

t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

NOTES :
1) $J = J1 \cdot J2 \cdot J3$
2) $K = K1 \cdot K2 \cdot K3$
3) t_n = Bit time before clock pulse
4) t_{n+1} = Bit time after clock pulse
5) NC = No internal connection.

RECOMMENDED OPERATING CONDITIONS

– Width of clock pulse, t_p (clock)	20 ns (min)
– Width of preset pulse t_p (preset)	25 ns (min)
– Width of clear pulse, t_p (clear)	25 ns (min)
– Input setup time, t_{setup}	$\geqslant t_p$ (clock)
– Input hold time, t_{hold}	0 (min)

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS (*)	MIN.	TYP.(**)	MAX.	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	V_{CC}=MIN	2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	V_{CC}=MIN			0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC}=MIN I_{load}=-400µA	2.4	3.5		V
$V_{out(0)}$	Logical 0 output voltage	V_{CC}=MIN I_{sink}= 16 mA		0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current at J1, J2, J3, K1, K2, or K3	V_{CC}=MAX V_{in} = 0.4 V			- 1.6	mA
$I_{in(0)}$	Logical 0 level input current at preset, clear, or clock	V_{CC}=MAX V_{in} = 0.4 V			- 3.2	mA
$I_{in(1)}$	Logical 1 level input current at J1, J2, J3, K1, K2, or K3	V_{CC}=MAX V_{in} = 2.4 V V_{CC}=MAX V_{in} = 5.5 V			40 1	µA mA
$I_{in(1)}$	Logical 1 level input current at preset, clear, or clock	V_{CC}=MAX V_{in} = 2.4 V V_{CC}=MAX V_{in} = 5.5 V			80 1	µA mA
I_{OS}	Short - circuit output current (***)	V_{CC}=MAX V_{in} = 0	- 18		- 57	mA
I_{CC}	Supply current	V_{CC}=MAX V_{in} = 5 V		10	20	mA

(*) For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions.
(**) All typical values are at V_{CC} = 5 V, T_A = 25°C.
(***) Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C, N = 10)

PARAMETER		Test Fig.	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{clock}	Maximum clock frequency	31	C_L=15pF R_L=400Ω	15	20		MHz
t_{pd1}	Propagation delay time to logical 1 level from clear or preset to output	32	C_L=15pF R_L=400Ω		16	25	ns
t_{pd0}	Propagation delay time to logical 0 level from clear or preset to output	32	C_L=15pF R_L=400Ω		25	40	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	31	C_L=15pF R_L=400Ω	10	16	25	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	31	C_L=15pF R_L=400Ω	10	25	40	ns

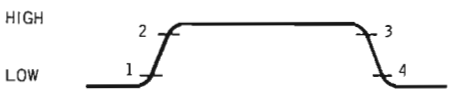
POSITIVE LOGIC

Low Input to Preset sets Q to Logical 1. Low Input to Clear sets Q to Logical 0. Preset and Clear are independent of clock.

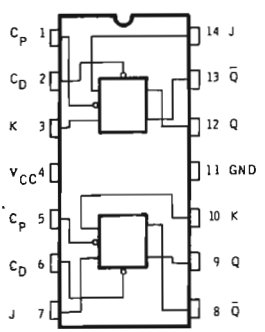
DESCRIPTION

These J-K flip-flops are based on the master-slave principle. Inputs to the master section are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections.
The sequence of operation is as follows :
1) Isolate slave from master.
2) Enter information from J and K inputs to master.
3) Disable J and K inputs.
4) Transfer information from master to slave.

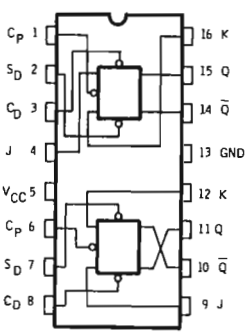
CLOCK WAVEFORM



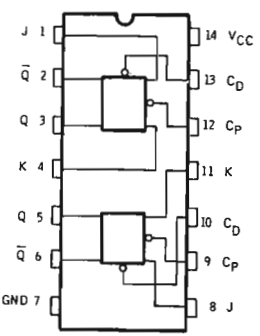
CONNECTION DIAGRAMS (Top view)



T 7473



T 7476



T 74107

TRUTH TABLE
(each flip-flop)

t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\bar{Q}_n$

NOTES
1) t_n = Bit time before clock pulse.
2) t_{n+1} = Bit time after clock pulse.

RECOMMENDED OPERATING CONDITIONS

– Width of clock pulse, t_p (clock)	20 ns (min)
– Width of preset pulse (T7476 only), t_p (preset)	25 ns (min)
– Width of clear pulse, t_p (clear)	25 ns (min)
– Input setup time, t_{setup}	$\geq t_p$ (clock)
– Input hold time, t_{hold}	0 (min)

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS (*)	MIN.	TYP.(**)	MAX.	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	V_{CC}=MIN	2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	V_{CC}=MIN			0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC}=MIN I_{load}=-400μA	2.4	3.5		V
$V_{out(0)}$	Logical 0 output voltage	V_{CC}=MIN I_{sink}= 16 mA		0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current at J or K	V_{CC}=MAX V_{in} = 0.4 V			- 1.6	mA
$I_{in(0)}$	Logical 0 level input current at clear, preset (T7476 only), or clock	V_{CC}=MAX V_{in} = 0.4 V			- 3.2	mA
$I_{in(1)}$	Logical 1 level input current at J or K	V_{CC}=MAX V_{in} = 2.4 V V_{CC}=MAX V_{in} = 5.5 V			40 1	μA mA
$I_{in(1)}$	Logical 1 level input current at clear, preset (T7476 only), or clock	V_{CC}=MAX V_{in} = 2.4 V V_{CC}=MAX V_{in} = 5.5 V			80 1	μA mA
I_{OS}	Short circuit output current (***)	V_{CC}=MAX V_{in} = 0	-18		- 57	mA
I_{CC}	Supply current	V_{CC}=MAX V_{in} = 5 V		20	40	mA

(*) For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions.

(**) All typical values, are at V_{CC} = 5V, T_A = 25°C.

(***) Not more than one output should be shorted at a time; only for T7473 and T74107 when measuring Q, apply 2.4V to clear, ground $\bar{Q}$ and limit test time to 100 ms.

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C, N = 10)

PARAMETER		Test Fig.	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{clock}	Maximum clock frequency	31	C_L=15pF R_L=400Ω	15	20		MHz
t_{pd1}	Propagation delay time to logical 1 level from clear to output	32	C_L=15pF R_L=400Ω		16	25	ns
t_{pd0}	Propagation delay time to logical 0 level from clear to output	32	C_L=15pF R_L=400Ω		25	40	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	31	C_L=15pF R_L=400Ω	10	16	25	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	31	C_L=15pF R_L=400Ω	10	25	40	ns

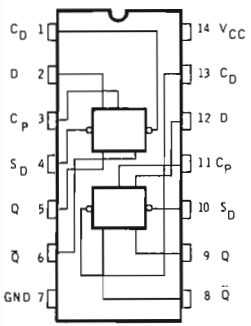
POSITIVE LOGIC:

Low Input to clear sets Q to logical 0. Clear is independent of clock.

DESCRIPTION

These monolithic, dual, D-type, edge-triggered flip-flops feature direct clear and preset inputs and complementary Q and $\bar{Q}$ outputs. Input information is transferred to the outputs on the positive edge of the clock pulse.
Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive going pulse. After the clock input threshold voltage has been passed, the data input (D) is locked out.
This dual flip-flop is ideally suited for medium-to-high-speed applications. It can result in a significant saving in system power dissipation and package count in applications where input gating is not required.

CONNECTION DIAGRAM (Top view)



T 7474

TRUTH TABLE

SYNCHRONOUS ENTRY D MODE OPERATION

INPUTS t_n	OUTPUTS t_{n+1}	
D	Q	$\bar{Q}$
0	0	1
1	1	0

RECOMMENDED OPERATING CONDITIONS

Width of Clock Pulse $t_{p(clock)}$	30 ns
Width of Preset Pulse $t_{p(preset)}$	30 ns
Width of Clear Pulse $t_{p(clear)}$	30 ns

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS (*)	MIN.	TYP.(**)	MAX.	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	V_{CC}=MIN	2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	V_{CC}=MIN			0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC}=MIN I_{load}= -400µA	2.4	3.5		V
$V_{out(0)}$	Logical 0 output voltage	V_{CC}=MIN I_{sink}= 16 mA		0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current at preset or D	V_{CC}=MAX V_{in} = 0.4 V			- 1.6	mA
$I_{in(0)}$	Logical 0 level input current at clear or clock	V_{CC}=MAX V_{in} = 0.4 V			- 3.2	mA
$I_{in(1)}$	Logical 1 level input current at D	V_{CC}=MAX V_{in} = 2.4 V			40	µA
		V_{CC}=MAX V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at preset or clock	V_{CC}=MAX V_{in} = 2.4 V			80	µA
		V_{CC}=MAX V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at clear	V_{CC}=MAX V_{in} = 2.4 V			120	µA
		V_{CC}=MAX V_{in} = 5.5 V			1	mA
I_{OS}	Short circuit output current (***)	V_{CC}=MAX V_{in} = 0	-18		- 57	mA
I_{CC}	Supply current	V_{CC}=MAX V_{in} = 5 V		17	30	mA

Notes: see the following page.

SWITCHING CHARACTERISTICS (V_{CC} =5V, T_A = 25° C, N = 10)

PARAMETER		Test Fig.	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{clock}	Maximum clock frequency	33	C_L=15pF R_L=400 Ω	15	25		MHz
t_{setup}	Minimum input setup time	33	C_L=15pF R_L=400 Ω		15	20	ns
t_{hold}	Minimum input hold time	33	C_L=15pF R_L=400 Ω		2	5	ns
t_{pd1}	Propagation delay time to logical 1 level from clear or preset to output	34	C_L=15pF R_L=400Ω			25	ns
t_{pd0}	Propagation delay time to logical 0 level from clear or preset to output	34	C_L=15pF R_L=400Ω			40	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	33	C_L=15pF R_L=400 Ω	10	14	25	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	33	C_L=15pF R_L=400 Ω	10	20	40	ns

POSITIVE LOGIC

Low Input to preset sets Q to logical 1. Low input to clear sets Q to logical 0. Preset and clear are independent of clock.

NOTES :

(*) For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions.

(**) All typical values are at V_{CC} = 5 V, T_A = 25°C.

(***) Not more than one output should be shorted at a time.

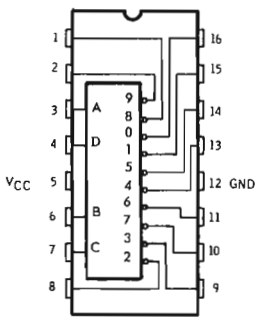
MSI

STANDARD TEMPERATURE RANGE

DESCRIPTION

The T7441A is a monolithic, BCD-to-decimal decoder incorporating high performance output transistors designed for use as indicator or relay drivers.
The BCD-to-decimal decoder consists of familiar transistor - transistor logic (TTL) gate circuits which select one of the ten decimal output drivers. The BCD inputs are fully compatible with Series T74 logic outputs; and, in addition, physical placement of these inputs is coincidental with the BCD outputs of the T7490 decade counter. Decoding and DC switching for components such as miniature lamps and relays may be performed by the T7441A within the ranges specified for the electrical characteristics.

CONNECTION DIAGRAM (Top view)



T 7441 A

positive logic : see truth table.

TRUTH TABLE

INPUT				OUTPUT ON *
D	C	B	A	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9

* All other outputs are off.

ABSOLUTE MAXIMUM RATING (above which the useful life may be impaired)
Current into any Output (off-state) 2 mA

OPERATING CONDITION
Maximum Voltage on any Output 70V

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

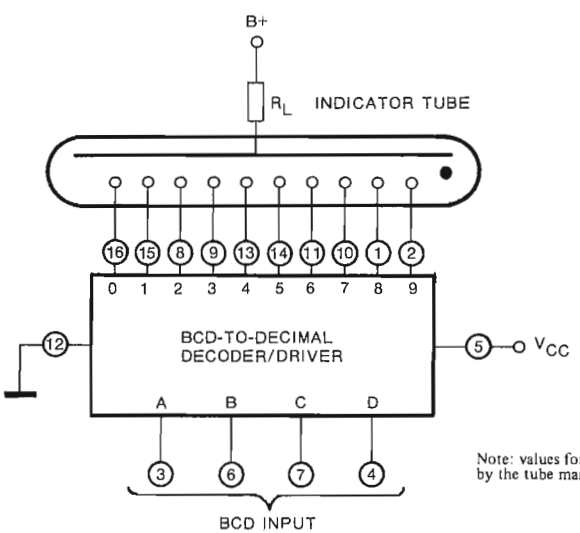
PARAMETER		Test Fig.	TEST CONDITIONS		Min.	Typ.(*)	Max.	Unit
$V_{in(1)}$	Logical 1 input voltage	8	V_{CC} = MIN		2			V
$V_{in(0)}$	Logical 0 input voltage	8	V_{CC} = MIN				0.8	V
V_{on}	On-state output voltage	8	V_{CC} = MIN	I_{on} = 7mA			2.5	V
I_{off}	Off-state reverse current	9	V_{CC} = MAX	V_{out} = 55V			50	µA
			V_{CC} = MAX	V_{out} = 70V			2	mA
$I_{in(1)}$	Logical 1 level input current at B, C or D	10	V_{CC} = MAX	V_{in} = 2.4V			40	µA
			V_{CC} = MAX	V_{in} = 5.5V			1	mA
$I_{in(1)}$	Logical 1 level input current at A	10	V_{CC} = MAX	V_{in} = 2.4V			80	µA
			V_{CC} = MAX	V_{in} = 5.5V			1	mA
$I_{in(0)}$	Logical 0 level input current at B, C or D	11	V_{CC} = MAX	V_{in} = 0.4V			-1.6	mA
$I_{in(0)}$	Logical 0 level input current A	11	V_{CC} = MAX	V_{in} = 0.4V			-3.2	mA
I_{CC}	Supply current	10	V_{CC} = MAX			21	42	mA

* This typical value is at V_{CC} = 5V, T_A = 25°C.

TYPICAL APPLICATION DATA

The T7441A output transistors are capable of withstanding voltages and sinking current required to operate most types of gas-filled indicator tubes.

When these decoder/drivers are used in close proximity (on the same circuit board) with standard digital integrated circuits, care should be exercised to ensure that the impedance of the ground bus (including interconnections) is sufficiently low to absorb the normal energy levels resulting from switching the tube elements.



Note: values for B + and R_L are as specified by the tube manufacturer.

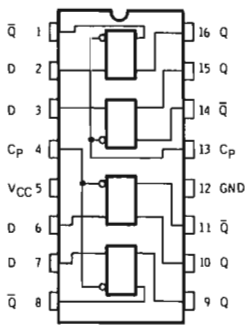
MSI

STANDARD TEMPERATURE RANGE

DESCRIPTION

This latch is ideally suited for use as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data (D) input is transferred to the Q output when the clock is high, and the Q output will follow the data input as long as the clock remains high. When the clock goes low,the information(which was present at the data input at the time the transition occured) is retained at the Q output until the clock is permitted to go high.
The T7475 features complementary Q and $\overline{Q}$ outputs from a 4-bit latch, and is available in the 16-pin package.
This circuit is completely compatible with all popular TTL or DTL families. Typical power dissipation is 40 milliwatts per latch.

CONNECTION DIAGRAM (Top view)



T 7475

TRUTH TABLE
(each latch)

t_n	t_{n+1}
D	Q
1	1
0	0

NOTES :
t_n = bit time before clock pulse transition..
t_{n+1} = bit time after clock pulse transition.

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		Test Figure	TEST CONDITIONS (*)		Min.	Typ.(**)	Max.	Unit
$V_{in(1)}$	Input voltage required to ensure logical 1 level at any input terminal	12	V_{CC} = MIN		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 level at any input terminal	13	V_{CC} = MIN				0.8	V
Vout(1)	Logical 1 output voltage	12 and 13	V_{CC} = MIN	I_{load} = -400µA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	12 and 13	V_{CC} = MIN	I_{sink}=16 mA			0.4	V
$I_{in(0)}$	Logical 0 level input current at D	14	V_{CC} = MAX	V_{in} = 0.4V			-3.2	mA
$I_{in(0)}$	Logical 0 level input current at clock	14	V_{CC} = MAX				-6.4	mA
$I_{in(1)}$	Logical 1 level input current at D	14	V_{CC} = MAX	V_{in} = 2.4V			80	µA
			V_{CC} = MAX	V_{in} = 5.5V			1	mA
$I_{in(1)}$	Logical 1 level input current at clock	14	V_{CC} = MAX	V_{in} = 2.4V			160	µA
			V_{CC} = MAX	V_{in} = 5.5V			1	mA
I_{OS}	Short-circuit output current(***)	15	V_{CC}= MAX	V_{out} = 0	-18		-57	mA
I_{CC}	Supply current	16	V_{CC} = MAX			32	53	mA

(*)For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
(**)All typical values are at V_{CC} = 5V, T_A = 25°C. (***) Not more than one output should be shorted at a time

SWITCHING CHARACTERISTICS, (V_{CC} = 5V, T_A = 25°C, N = 10)

PARAMETER		Test Figure	TEST CONDITIONS	Min.	Typ.	Max.	Unit
$t_{setup\ 1}$	Minimum logical 1 level input setup time at D input	35	C_L = 15pF R_L = 400 Ω		7	20	ns
$t_{setup\ 0}$	Minimum logical 0 level input setup time at D input	35	C_L = 15pF R_L = 400 Ω		14	20	ns
$t_{hold\ 1}$	Maximum logical 1 level input hold time required at D input	35	C_L = 15pF R_L = 400 Ω	0	15 *		ns
$t_{hold\ 0}$	Maximum logical 0 level input hold time required at D input	35	C_L = 15pF R_L = 400 Ω	0	6 *		ns
$t_{pd\ 1(D-Q)}$	Propagation delay time to logical 1 level from D input to Q output	35	C_L = 15pF R_L = 400 Ω		16	30	ns
$t_{pd\ 0(D-Q)}$	Propagation delay time to logical 0 level from D input to Q output	35	C_L = 15pF R_L = 400 Ω		14	25	ns
$t_{pd\ 1(D-\bar{Q})}$	Propagation delay time to logical 1 level from D input to $\bar{Q}$ output	35	C_L = 15pF R_L = 400 Ω		24	40	ns
$t_{pd\ 0(D-\bar{Q})}$	Propagation delay time to logical 0 level from D input to $\bar{Q}$ output	35	C_L = 15pF R_L = 400 Ω		7	15	ns
$t_{pd\ 1(C-Q)}$	Propagation delay time to logical 1 level from clock input to Q output	35	C_L = 15pF R_L = 400 Ω		16	30	ns
$t_{pd\ 0(C-Q)}$	Propagation delay time to logical 0 level from clock input to Q output	35	C_L = 15pF R_L = 400 Ω		7	15	ns
$t_{pd\ 1(C-\bar{Q})}$	Propagation delay time to logical 1 level from clock input to $\bar{Q}$ output	35	C_L = 15pF R_L = 400 Ω		16	30	ns
$t_{pd\ 0(C-\bar{Q})}$	Propagation delay time to logical 0 level from clock input to $\bar{Q}$ output	35	C_L = 15pF R_L = 400 Ω		7	15	ns

* These typical times indicate that period occurring prior to the fall of clock pulse (t_0) below 1.5V when data at the D input will still be recognized and stored.

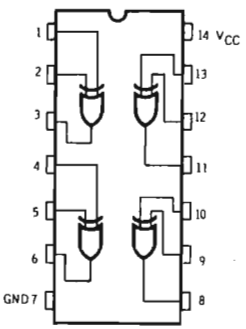
MSI

STANDARD TEMPERATURE RANGE

DESCRIPTION

This monolithic, quadruple 2-input exclusive-OR gate utilizes TTL circuitry to perform the function : $Y = A\overline{B} + \overline{A}B$. When the input states are complementary, the output goes to a logical 1.
This circuit is fully compatible for use with other TTL or DTL circuits. Input clamping diodes are provided to minimize transmission line effects and thereby simplify system design. Input buffers are used to lower the fan-in requirement to only one normalized series T74 load. A full fan out to 10 normalized series T74 loads is available from each of the outputs in the logical 0 state. A fan-out of 20 is provided in the logical 1 state. Propagation delay is 12 nanoseconds and power dissipation is 37.5 milliwatts typically for each exclusive-OR function.

CONNECTION DIAGRAM (Top view)



T 7486

TRUTH TABLE

Inputs		Output
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS (*)		Min.	Typ.(**)	Max.	Unit
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	V_{CC} = MIN		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	V_{CC} = MIN				0.8	V
V_{out} (1)	Logical 1 output voltage	V_{CC} = MIN $V_{in(0)}$ = 0.8V	$V_{in(1)}$ = 2V I_{load} = -800µA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN $V_{in(0)}$ = 0.8V	$V_{in(1)}$ = 2V I_{sink} = 16mA			0.4	V
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = MAX	V_{in} = 2.4V			40	µA
		V_{CC} = MAX	V_{in} = 5.5V			1	mA
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX	V_{in} = 0.4V			- 1.6	mA
I_{OS}	Short circuit output current (***)	V_{CC} = MAX $V_{in(0)}$ = 0	$V_{in(1)}$= 4.5V	- 18		- 55	mA
I_{CC}	Supply current	V_{CC} = MAX	V_{in} = 4.5V		30	50	mA

(*) For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
(**) All typical values are at V_{CC} = 5V, T_A = 25°C.
(***) Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C, N = 10)

PARAMETER		Test Figure	TEST CONDITIONS	Min.	Typ.	Max.	Unit
t_{pd0}	Propagation delay time to logical 0 level (other input low)	30	C_L = 15pF R_L = 400 Ω		11	17	ns
t_{pd1}	Propagation delay time to logical 1 level (other input low)	30	C_L = 15pF R_L = 400 Ω		15	23	ns
t_{pd0}	Propagation delay time to logical 0 level (other input high)	30	C_L = 15pF R_L = 400 Ω		13	22	ns
t_{pd1}	Propagation delay time to logical 1 level (other input high)	30	C_L = 15pF R_L = 400 Ω		18	30	ns

DESCRIPTION AND TYPICAL COUNT CONFIGURATIONS

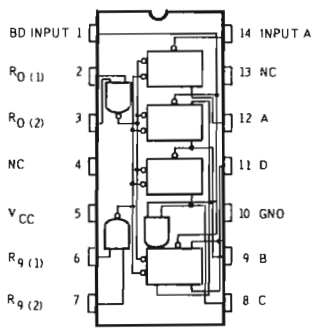
This high-speed, monolithic decade counter consists of four dual-rank, master-slave flip-flops internally interconnected to provide a divide-by-two counter and a divide-by-five counter. Gated direct reset lines are provided to inhibit count inputs and return all outputs to logical zero or to a binary coded decimal (BCD) count of 9. As the output from flip-flop A is not internally connected to the succeeding stages, the count may be separated in three independent count modes :

1) When used as a binary coded decimal decade counter, the BD input must be externally connected to the A output. The A input receives the incoming count, and a count sequence is obtained in accordance with the BCD count sequence truth table shown below. In addition to a conventional zero reset, inputs are provided for a reset to nine.

2) If a symmetrical divide-by-ten count is desired for frequency synthesizers or other applications requiring division of a binary count by a power of ten, the D output must be externally connected to the A input. The input count is then applied at the BD input and a divide-by-ten square wave is obtained at output A.

3) For operation as a divide-by-two counter and a divide-by-five counter, no external interconnections are required. Flip-flop A is used as a binary element for the divide-by-two function. The BD input is used to obtain binary divide-by-five operation at the B, C, and D outputs. In this mode, the two counters operate independently; however, all four flip-flops are reset simultaneously.

CONNECTION DIAGRAM (Top view)



T 7490

TRUTH TABLES

BCD COUNT SEQUENCE (note 1)

COUNT	OUTPUT			
	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

RESET/COUNT (note 2)

RESET INPUTS				OUTPUT			
$R_{0(1)}$	$R_{0(2)}$	$R_{9(1)}$	$R_{9(2)}$	D	C	B	A
1	1	0	X	0	0	0	0
1	1	X	0	0	0	0	0
X	X	1	1	1	0	0	1
X	0	X	0	COUNT			
0	X	0	X	COUNT			
0	X	X	0	COUNT			
X	0	0	X	COUNT			

NOTES :

1) Output A connected to input BD for BCD count.
2) X indicates that either a logical 1 or a logical 0 may be present.

MSI STANDARD TEMPERATURE RANGE

OPERATING CONDITIONS

Width of Input Count Pulse, $t_{p(in)}$ 50 ns (min)
Width of Reset Pulse, $t_{p(reset)}$ 50 ns (min)

NOTE: Fan-out from output A to input BD and to 10 additional series T74 loads is permitted.

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		Test Figure	TEST CONDITIONS (*)	Min.	Typ.(**)	Max.	Unit
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	17	V_{CC} = MIN	2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	18	V_{CC} = MIN			0.8	V
$V_{out(1)}$	Logical 1 output voltage	18	V_{CC} = MIN I_{load}=-400µA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	17	V_{CC} = MIN I_{sink}=16mA			0.4	V
$I_{in(1)}$	Logical 1 level input current at $R_{0(1)}$, $R_{0(2)}$, $R_{9(1)}$, or $R_{9(2)}$	19	V_{CC} = MAX V_{in} = 2.4V			40	µA
			V_{CC} = MAX V_{in} = 5.5V			1	mA
$I_{in(1)}$	Logical 1 level input current at input A	19	V_{CC} = MAX V_{in} = 2.4V			80	µA
			V_{CC} = MAX V_{in} = 5.5V			1	mA
$I_{in(1)}$	Logical 1 level input current at input BD	19	V_{CC} = MAX V_{in} = 2.4V			160	µA
			V_{CC} = MAX V_{in} = 5.5V			1	mA
$I_{in(0)}$	Logical 0 level input current at $R_{0(1)}$, $R_{0(2)}$, $R_{9(1)}$, or $R_{9(2)}$	20	V_{CC} = MAX V_{in} = 0.4V			-1.6	mA
$I_{in(0)}$	Logical 0 level input current at input A	20	V_{CC} = MAX V_{in} = 0.4V			-3.2	mA
$I_{in(0)}$	Logical 0 level input current at input BD	20	V_{CC} = MAX V_{in} = 0.4V			-6.4	mA
I_{OS}	Short-circuit output current (***)	21	V_{CC} = MAX V_{out} = 0	-18		-57	mA
I_{CC}	Supply current	19	V_{CC} = MAX V_{in} = 4.5V		32	53	mA

NOTES :
(*) For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
(**) All typical values are at V_{CC} = 5V, T_A = 25°C.
(***) Not more than one output should be grounded at a time.

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C, N = 10)

PARAMETER		Test Figure	TEST CONDITIONS	Min.	Typ.	Max.	Unit
f_{max}	Maximum frequency of input count pulses		C_L = 15pF R_L = 400Ω	10	18		MHz
t_{pd1}	Propagation delay time to logical 1 level from input count pulse to output C	36	C_L = 15pF R_L = 400Ω		60	100	ns
t_{pd0}	Propagation delay time to logical 0 level from input count pulse to output C	36	C_L = 15pF R_L = 400Ω		60	100	ns

MSI

STANDARD TEMPERATURE RANGE

DESCRIPTION

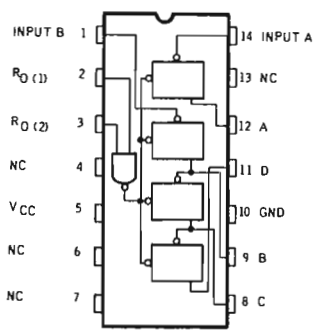
This high-speed, monolithic 4-bit binary counter consists of four master-slave flip-flops which are internally interconnected to provide a divide-by-two counter and a divide-by-eight counter. A gated direct reset line is provided which inhibits the count inputs and simultaneously returns the four flip-flop outputs to a logical 0.

As the output from flip-flop A is not internally connected to the succeeding flip-flops the counter may be operated in two independent modes :

1) When used as a 4-bit ripple-through counter, output A must be externally connected to input B. The input count pulses are applied to input A. Simultaneous divisions of 2, 4, 8, and 16 are performed at the A, B, C, and D outputs as shown in the truth table below.

2) When used as a 3-bit ripple-through counter, the input count pulses are applied to input B. Simultaneous frequency divisions of 2,4, and 8 are available at the B, C and D outputs . independent use of flip-flop A is available if the reset function coincides with the reset of the 3-bit ripple-through counter.

CONNECTION DIAGRAM (Top view)



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TRUTH TABLE (Notes 1, 2 and 3)

COUNT	OUTPUT			
	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

NOTES :

1) Output A connected to input B.
2) To reset all outputs to logical 0 both $R_{O(1)}$ and $R_{O(2)}$ inputs must be at a logical 1.
3) Either (or both) reset inputs $R_{O(1)}$ and $R_{O(2)}$ must be at a logical 0 to count.

OPERATING CONDITIONS

Width of Input Count Pulse, $t_{p(in)}$	50 ns (min)
Width of Reset Pulse, $t_{p(reset)}$	50 ns (min)

NOTE : Fan-out from output A to input B and to 10 additional series T 74 loads is permitted.

ELECTRICAL CHARACTERISTICS (over recommended free air temperature range unless otherwise noted)

PARAMETER		Test Figure	TEST CONDITIONS (*)	Min.	Typ.(**)	Max.	Unit
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	17	V_{CC} = MIN	2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	18	V_{CC} = MIN			0.8	V
$V_{out(1)}$	Logical 1 output voltage	18	V_{CC} = MIN I_{load} = -400µA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	17	V_{CC} = MIN I_{sink} = 16mA			0.4	V
$I_{in(1)}$	Logical 1 level input current at $R_{0(1)}$ or $R_{0(2)}$ inputs	19	V_{CC} = MAX V_{in} = 2.4V			40	µA
			V_{CC} = MAX V_{in} = 5.5V			1	mA
$I_{in(1)}$	Logical 1 level input current at A or B inputs	19	V_{CC} = MAX V_{in} = 2.4V			80	µA
			V_{CC} = MAX V_{in} = 5.5V			1	mA
$I_{in(0)}$	Logical 0 level input current at $R_{0(1)}$ or $R_{0(2)}$ inputs	20	V_{CC} = MAX V_{in} = 0.4V			-1.6	mA
$I_{in(0)}$	Logical 0 level input current at A or B inputs	20	V_{CC} = MAX V_{in} = 0.4V			-3.2	mA
I_{OS}	Short-circuit output current (***)	21	V_{CC} = MAX V_{out} = 0	-18		-57	mA
I_{CC}	Supply current	19	V_{CC} = MAX V_{in} = 4.5V		32	53	mA

NOTES :
(*) For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
(**) All typical values are at V_{CC} = 5V, T_A = 25°C.
(***) Not more than one output should be grounded at a time.

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C. N = 10)

PARAMETER		Test Figure	TEST CONDITIONS	Min.	Typ.	Max.	Unit
f_{max}	Maximum frequency of input count pulses		C_L = 15pF R_L = 400 Ω	10	18		MHz
t_{pd1}	Propagation delay time to logical 1 level from input count pulse to output D	36	C_L = 15pF R_L = 400 Ω		75	135	ns
t_{pd0}	Propagation delay time to logical 0 level from input count pulse to output D	36	C_L = 15pF R_L = 400 Ω		75	135	ns

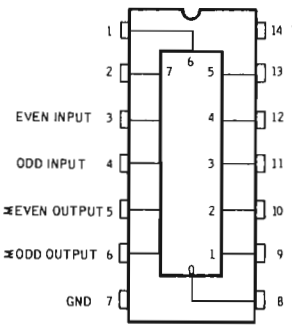
MSI

STANDARD TEMPERATURE RANGE

DESCRIPTION

This universal, monolithic, 8-bit parity generator/checker, utilizing familiar Series T74 TTL circuitry, features odd/even outputs and control inputs to facilitate operation in either odd-or even-parity applications. The word-length capability is easily expanded by cascading. Typical applications are shown for this parity circuit being used to generate and check parity.
The T74180 is fully compatible with other TTL or DTL circuits. Input buffers are provided so that each data input represents only one normalized series T74 load. A full fan-out to 10 normalized series T74 loads is available from each of the outputs in the logical 0 state. A fan-out to 20 normalized loads is provided in the logical 1 state. Typical power dissipation is 170 mW.

CONNECTION DIAGRAM (Top view)



T 74180

Positive logic : see truth table

TRUTH TABLE

INPUTS			OUTPUTS	
Σ OF 1's AT 0 THRU 7	EVEN	ODD	Σ EVEN	Σ ODD
EVEN	1	0	1	0
ODD	1	0	0	1
EVEN	0	1	0	1
ODD	0	1	1	0
X	1	1	0	0
X	0	0	1	1

X = irrelevant

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		Test Figure	TEST CONDITIONS (*)	Min.	Typ(**)	Max.	Unit
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	22	V_{CC} = MIN	2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	22	V_{CC} = MIN			0.8	V
$V_{out(1)}$	Logical 1 output voltage	22	V_{CC} = MIN $V_{in(1)}$ = 2V $V_{in(0)}$=0.8V I_{load} = - 800 µA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	22	V_{CC} = MIN $V_{in(1)}$ = 2V, $V_{in(0)}$=0.8V I_{sink} = 16 mA			0.4	V
$I_{in(1)}$	Logical 1 level input current at each data input	23	V_{CC} = MAX V_{in} = 2.4V			40	µA
			V_{CC} = MAX V_{in} = 5.5V			1	mA
$I_{in(0)}$	Logical 0 level input current at each data input	23	V_{CC} = MAX V_{in} = 0.4V			- 1,6	mA
$I_{in(1)}$	Logical 1 level input current at even or odd input	23	V_{CC} = MAX V_{in} = 2.4V			80	µA
			V_{CC} = MAX V_{in} = 5.5V			1	mA
$I_{in(0)}$	Logical 0 level input current at even or odd input	23	V_{CC} = MAX V_{in} = 0.4V			- 3.2	mA
I_{OS}	Short circuit output current (***)	24	V_{CC} = MAX	-18		- 55	mA
I_{CC}	Supply current	24 and 25	V_{CC} = MAX		34	56	mA

(*) For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
(**) All typical values are at V_{CC} = 5V, T_A = 25°C.
(***) Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C, N = 10)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	Test Figure	TEST CONDITIONS	Min.	Typ.	Max.	Unit
t_{pd1}	Data	Σ Even	37	C_L = 15pF R_L = 400 Ω		40	60	ns
t_{pd0}	Data	Σ Even	37	C_L = 15pF R_L = 400 Ω		25	38	ns
t_{pd1}	Data	Σ Odd	37	C_L = 15pF R_L = 400 Ω		32	48	ns
t_{pd0}	Data	Σ Odd	37	C_L = 15pF R_L = 400 Ω		45	68	ns
t_{pd1}	Data	Σ Even	37	C_L = 15pF R_L = 400 Ω		32	48	ns
t_{pd0}	Data	Σ Even	37	C_L = 15pF R_L = 400 Ω		45	68	ns
t_{pd1}	Data	Σ Odd	37	C_L = 15pF R_L = 400 Ω		40	60	ns
t_{pd0}	Data	Σ Odd	37	C_L = 15pF R_L = 400 Ω		25	38	ns
t_{pd1}	Even or Odd	Σ Even or Σ Odd	37	C_L = 15pF R_L = 400 Ω		13	20	ns
t_{pd0}	Even or Odd	Σ Even or Σ Odd	37	C_L = 15pF R_L = 400 Ω		7	10	ns

TYPICAL APPLICATIONS

VERIFYING TRANSMITTED DATA

In this example (Figure A), data is being transmitted from data register A to data register B. Parity generators A1 and A2 are connected to generate an even-parity bit Q_{16} which is transmitted to register B. Parity checkers B1 and B2 verify the accuracy of the transmitted data and generate an even true (logical 1) or false (logical 0) parity output signal.

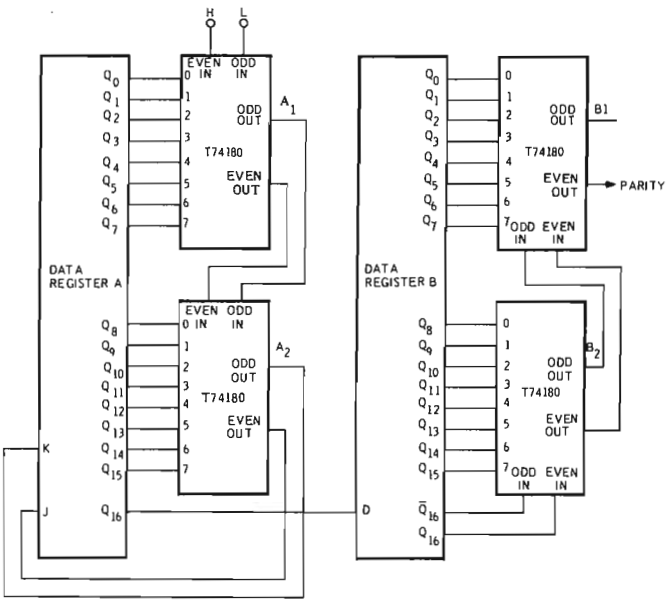


FIG. A

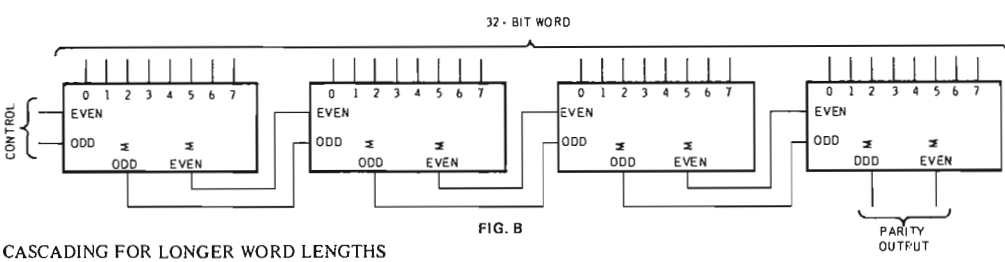


FIG. B

CASCADING FOR LONGER WORD LENGTHS

The parity generator/checker may be cascaded for applications requiring longer word lengths. See Figure B. The ODD IN control is grounded for even parity generation and the EVEN IN control is grounded for odd parity generation. Two control inputs and two outputs ensure faster operation when cascading for word lengths over 8 bits, as only one gate delay is added for each additional 8-bit group. For a 32-bit word, parity can be generated in approximately 65 ns.

D-C TEST CIRCUITS*

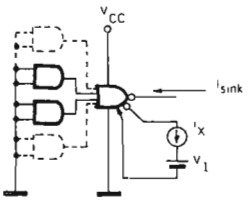


FIG. 1

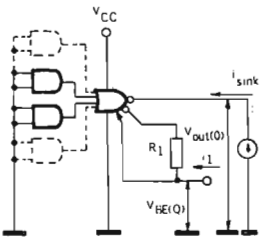


FIG. 2

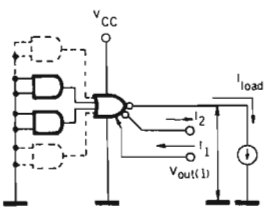


FIG. 3

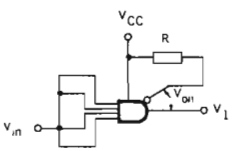


FIG. 4

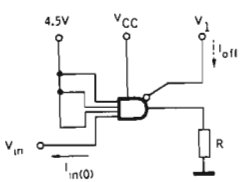


FIG. 5

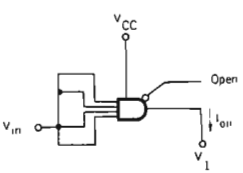
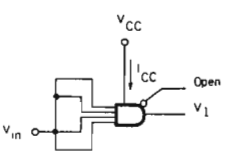


FIG. 6

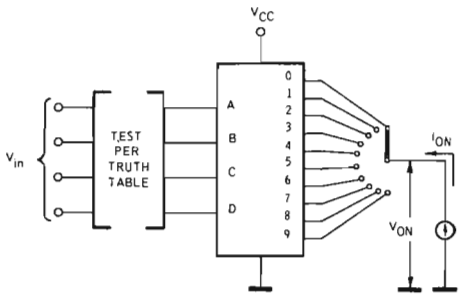


1) "On" and "off" conditions are tested separately
2) Each gate is tested separately.

FIG. 7

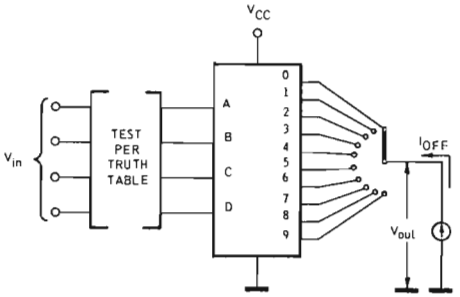
*Arrows indicate actual direction of current flow.

DC TEST CIRCUITS* (contd.)



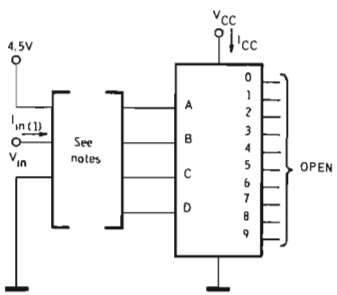
1. Each output is tested separately in the ON state.

FIG. 8



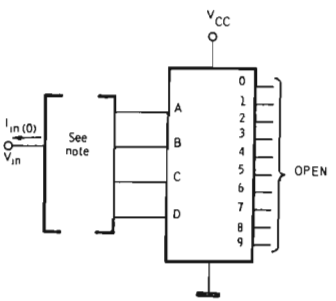
1. Each output is tested separately in the OFF state.

FIG. 9



1. When testing $I_{in(1)}$ each input is tested separately.
2. When testing I_{CC} all outputs are open, inputs A, B, and C are at 4.5V, and input D is grounded.

FIG. 10

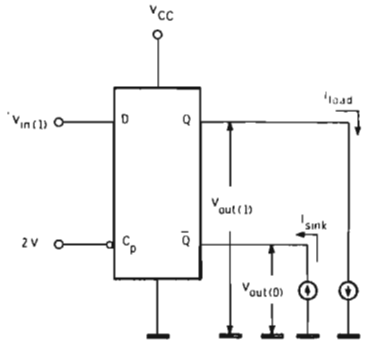


1. Each input is tested separately

FIG. 11

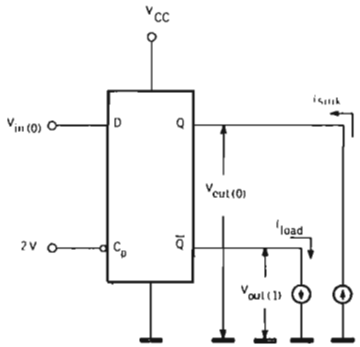
* Arrows indicate actual direction of current flow.

D-C TEST CIRCUITS* (contd.)



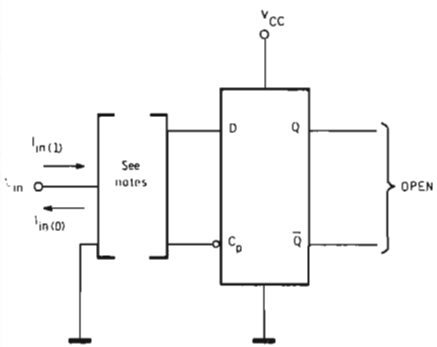
1. Each latch is tested separately.

FIG. 12



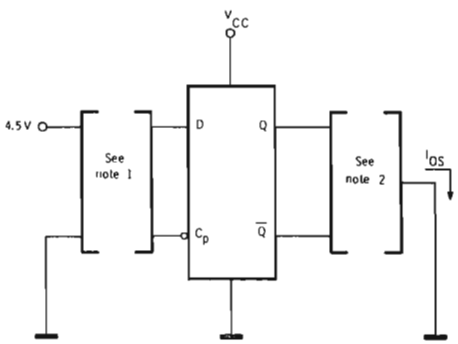
1. Each latch is tested separately.

FIG. 13



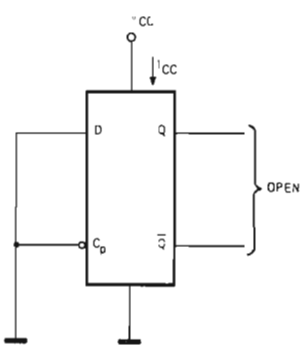
1. Each input is tested separately.
2. When testing $I_{in(1)}$ at D,ground clock.
3. When testing $I_{in(1)}$ at clock,ground all D inputs.

FIG. 14



1. Input conditions are in accordance with truth table.
2. Each latch and each output is tested separately.

FIG. 15

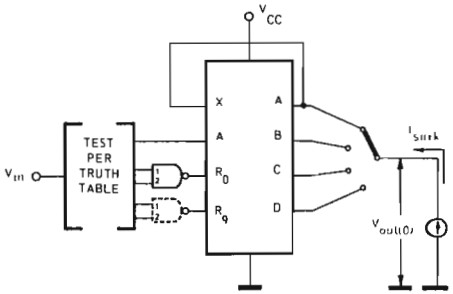


1. All latches are tested simultaneously.

FIG. 16

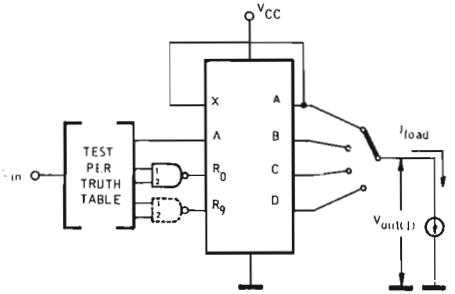
* Arrows indicate actual direction of current flow.

D-C TEST CIRCUITS* (contd.)



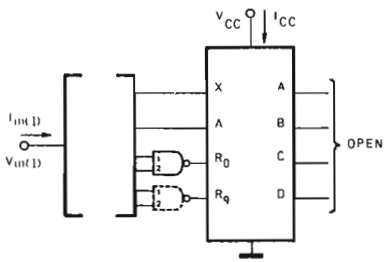
1. Each output is tested in the logical 0 state.

FIG. 17



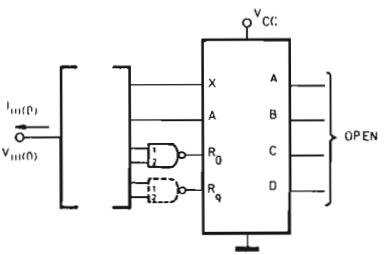
1. Each output is tested in the logical 1 state.

FIG. 18



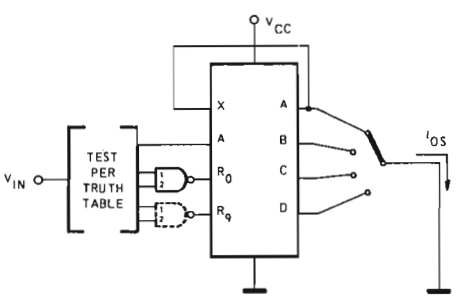
1. Each input is tested separately.
2. When testing $R_{0(1)}$ or $R_{9(1)}$ ground $R_{0(2)}$ or $R_{9(2)}$.
3. When testing $R_{0(2)}$ or $R_{9(2)}$ ground $R_{0(1)}$ or $R_{9(1)}$.
4. When testing I_{CC} reset all outputs to logical 0, ground all inputs, then measure I_{CC}.

FIG. 19



1. Each input is tested separately.
2. When testing $R_{0(1)}$ or $R_{9(1)}$ apply 4.5V to $R_{0(2)}$ or $R_{9(2)}$.
3. When testing $R_{0(2)}$ or $R_{9(2)}$ apply 4.5V to $R_{0(1)}$ or $R_{9(1)}$.

FIG. 20



1. Each output is tested in the logical 1 state.

FIG. 21

* – Arrows indicate actual direction of current flow.
– X (pin Nº 1) is BD input when testing T7490, B input when testing T7493.
– R_9 (pins Nº 6 - Nº 7) has to be connected only when testing T7490.

D-C TEST CIRCUITS* (contd.)

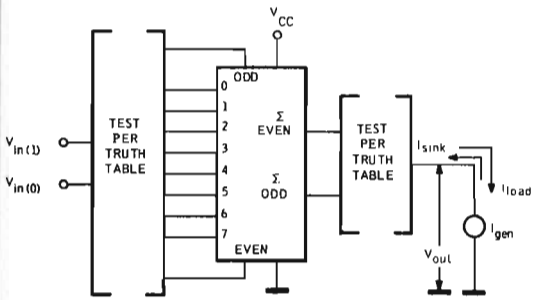
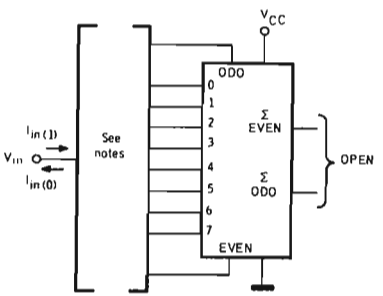
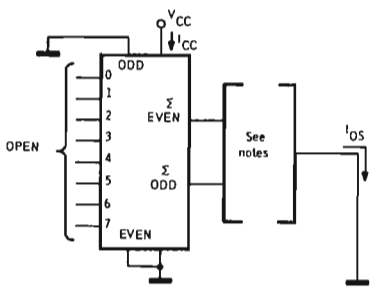


FIG. 22



1. Each input is tested separately.
2. Odd and even inputs are each tested for $I_{in(1)}$ and $I_{in(0)}$ with both an even-code and an odd-code applied at the data inputs.

FIG. 23



1. Each output is tested separately.
2. When testing I_{CC} both outputs are open.

FIG. 24

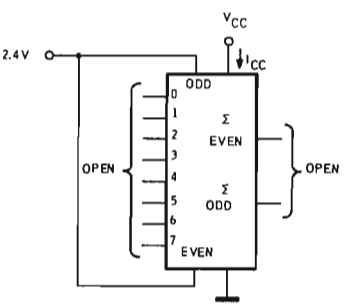


FIG. 25

* Arrows indicate actual direction of current flow.

SWITCHING TIME TEST CIRCUITS

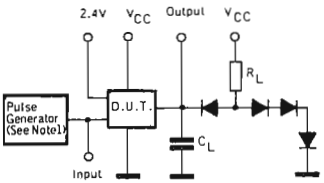


FIG. 26

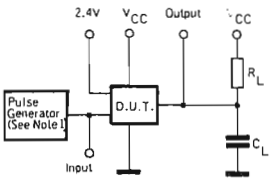


FIG. 27

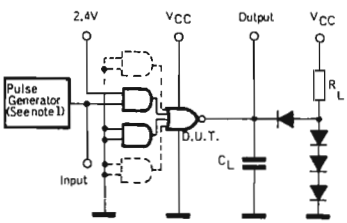


FIG. 28

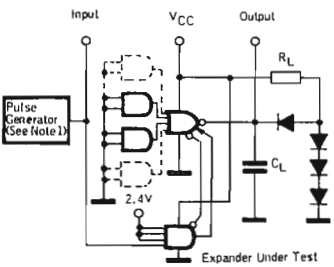
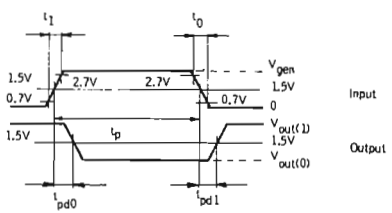


FIG. 29

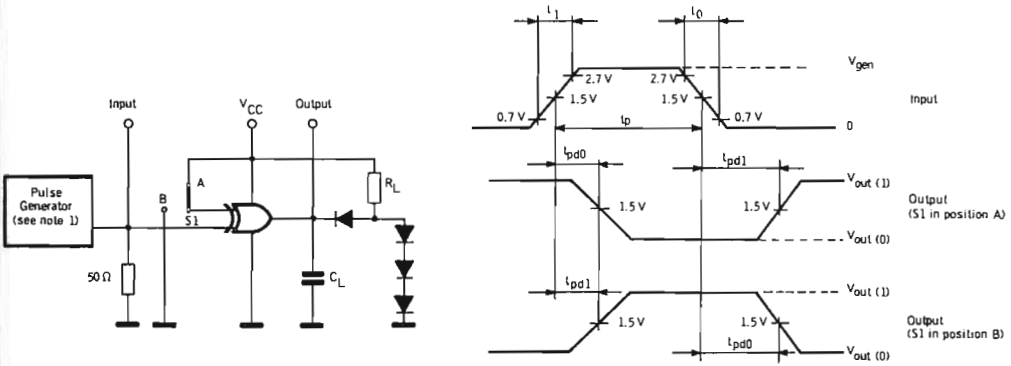
SWITCHING WAVEFORMS FOR FIG. 26 - 27 - 28 - 29



NOTES :

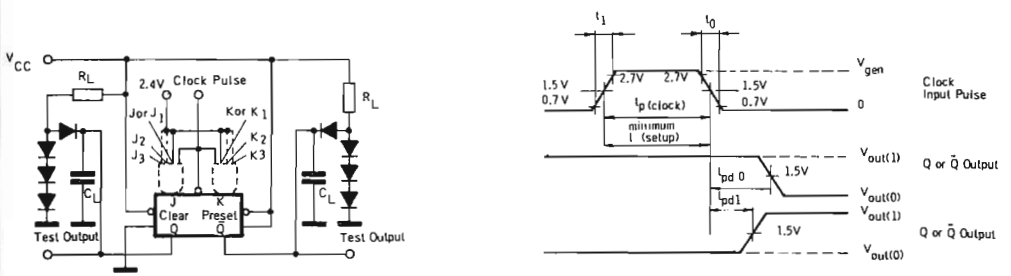
1) The generator has the following characteristics : V_{gen} = 3.5V; t_p = 0.5 µs; PRR = 1 MHz; $Z_{out} \simeq 50\ \Omega$; t_o = 5 ns and t_1 = 10 ns (for T 7406 a T7416; to = $t_1 \leqslant 10$ ns.).
2) All diodes are BAY 71.
3) $t_{pd} = \frac{t_{pd0} + t_{pd1}}{2}$
4) C_L includes probe and jig capacitance.

SWITCHING TIME TEST CIRCUITS (contd)



NOTES : 1) The generator has the following characteristics; $V_{gen} = 3V$, $t_0 = t_1 \leqslant 15$ ns, $t_p = 0.5$ µs, PRR = 1 MHz, $Z_{out} \simeq 50\ \Omega$.
2) All diodes are BAY 71. – 3) $t_{pd} = \frac{t_{pd0} + t_{pd1}}{2}$ – 4) C_L includes probe and Jig capacitance. – 5) Each gate tested separately.

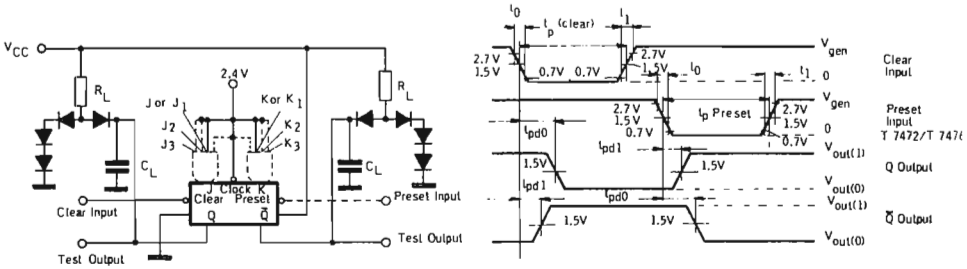
FIG. 30



NOTES : 1) Clock, J and K input pulse characteristics : $V_{gen} = 3.5V$, $t_0 = 5$ ns, $t_1 = 10$ ns, $t_p = 20$ ns, and PRR = 1MHz. When testing f_{clock} vary PRR.
2) For the T7472, $J = J_1 \cdot J_2 \cdot J_3$ and $K = K_1 \cdot K_2 \cdot K_3$.
3) Gates inputs (shown with dotted lines) are for the T7472 only. The T7473, T7476, T74107 dual Flip-Flops have direct J and K inputs and preset is not available on the T 7473 or T74107.
4) All diodes are BAY 71.
5) C_L includes probe and Jig capacitance.

FIG. 31

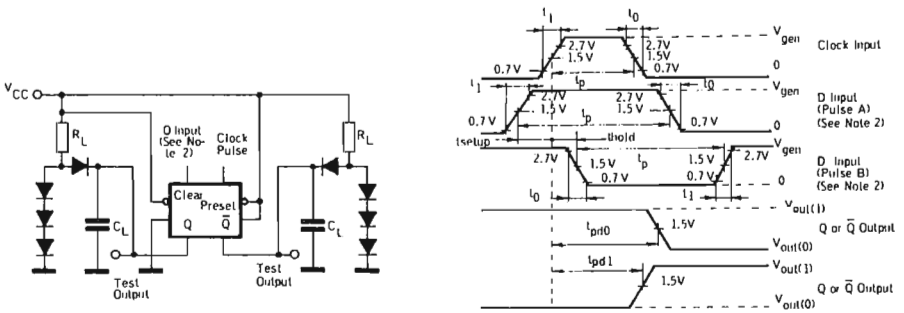
SWITCHING TIME TEST CIRCUITS (contd.)



NOTES :

1) Clear or preset inputs dominate regardless of the state of clock or J-K inputs.
2) Clear or preset input pulse characteristics: V_{gen} = 3.5V, t_0 = 5ns, t_1 = 10ns, $t_{p(clear)} = t_{p(preset)}$ = 25ns. PRR = 1MHz, and $Z_{out} \simeq 50\,\Omega$.
3) Gates inputs (shown with dotted lines) are for the T7472 only. The T7473, T7476 and T74107, dual Flip-Flops have direct J and K inputs, and preset is not available on the 7473 or 74107.
4) All diodes are BAY71.
5) C_L includes probe and Jig capacitance.

FIG. 32

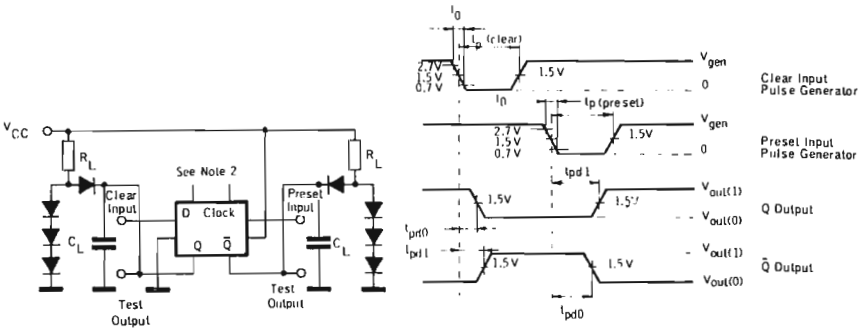


NOTES:

1) Clock input pulse has the following characteristics: V_{gen}=3.5V, t_0=5ns, t_1=10ns, t_p=30ns, and PRR=1 MHz. When testing f_{clock}, vary PRR
2) D Input (pulse A) has the following characteristics: V_{gen}=3.5V, t_0=5ns, t_1=10ns, t_{setup}=20ns, t_p=60ns, and PRR is 50%of the clock PRR.
   D Input (pulse B) has the following characteristics: V_{gen}=3.5V, t_0=5ns, t_1=10ns, t_{hold}=5ns, t_p=60ns, and PRR is 50%of the clock PRR.
3) All diodes are BAY 71
4) C_L includes probe and Jig capacitance.

FIG. 33

SWITCHING TIME TEST CIRCUIT (contd.)



NOTES :

1) Clear and preset inputs of the T7474 dominate regardless of the state of clock or D inputs. 2) All diodes are BAY 71.
3) C_L includes probe and Jig capacitance. 4) Clear or preset input pulse characteristics : V_{gen} =3.5V, t_0 =5ns, and t_p =30 ns.

FIG. 34

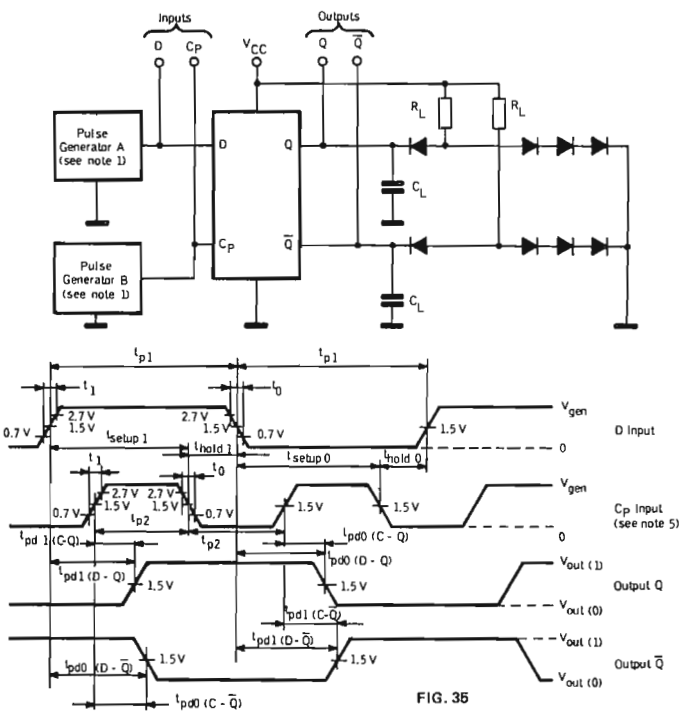
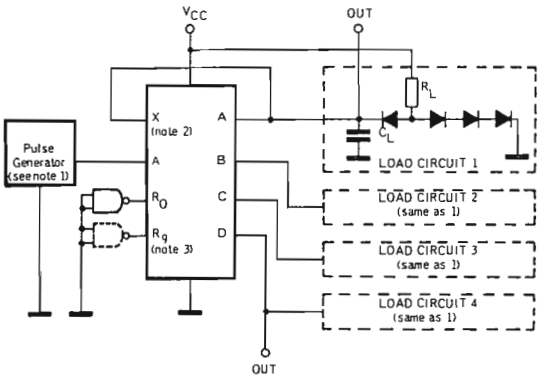


FIG. 35

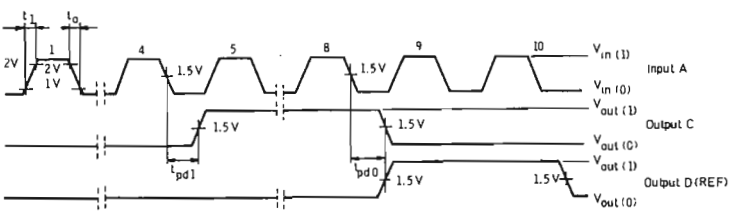
NOTES : 1) The pulse generators have the following characteristics : V_{gen} = 3V, $t_1 = t_0 \leq 10$ ns, and $Z_{out} \simeq 50\ \Omega$. For pulse generator A t_{p1} =1µs and PRR = 500 kHz. For pulse generator B, t_{p2} = 500 ns and PRR = 1 MHz. Positions of D-input and clock-input pulses are varied with respect to each other to verify setup and hold times.

2) Each latch is tested separately.
3) C_L includes probe and jig capacitance.
4) All diodes are BAY 71.
5) When measuring t_{pd1} (D-Q) and t_{pd0} (D-Q) or t_{pd0} (D-$\bar{Q}$) and t_{pd1} (D-$\bar{Q}$), clock input must be held at logical 1.

SWITCHING TIME TEST CIRCUITS (contd.)



SWITCHING WAVEFORMS FOR T 7490



SWITCHING WAVEFORMS FOR T 7493

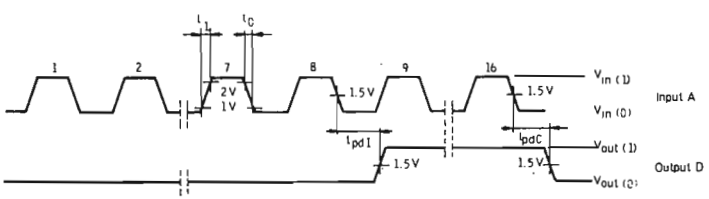


FIG. 36

NOTES :

1) The pulse generator has the following characteristics: $V_{gen} = 3V$; $t_0 = t_1 \leqslant 15ns$, $t_p = 0.5\ \mu s$, PRR = 1 MHz, $Z_{out} \simeq 50\Omega$

2) X (pin N. 1) is BD input when testing T7490, B input when testing T7493

3) R_0 (pins N. 6 - N. 7) has to be connected only when testing T7490.

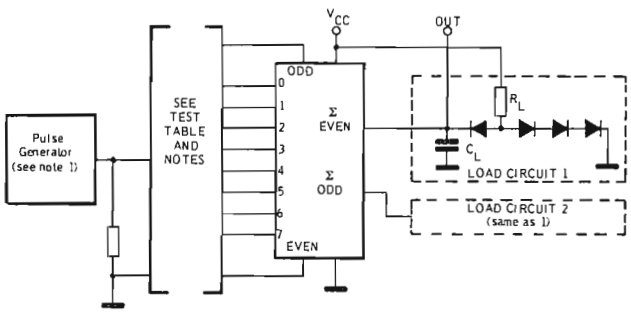
4) All diodes are BAY71

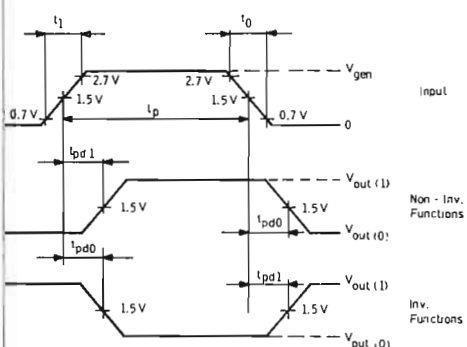
5) C_L includes probe and Jig capacitance

6) $t_{pd} = \frac{t_{pd0} + t_{pd1}}{2}$

7) Voltage values are with respect to ground terminal.

SWITCHING TIME TEST CIRCUITS (contd)





TEST TABLE

INPUT CONDITIONS		OUTPUT TESTED
PULSE	GND	
0	ODD	Σ EVEN
1	ODD	Σ EVEN
2	ODD	Σ EVEN
3	ODD	Σ EVEN
4	ODD	Σ EVEN
5	ODD	Σ EVEN
6	ODD	Σ EVEN
7	ODD	Σ EVEN
0	ODD	Σ ODD
1	ODD	Σ ODD
2	ODD	Σ ODD
3	ODD	Σ ODD
4	ODD	Σ ODD
5	ODD	Σ ODD
6	ODD	Σ ODD
7	ODD	Σ ODD
EVEN	NONE	Σ EVEN
ODD	0	Σ EVEN
EVEN	0	Σ ODD
ODD	NONE	Σ ODD

NOTES :

1) The pulse generator has the following characteristics:
   $V_{gen} = 3V$, $t_1 = t_0 = 10$ ns, $t_p = 500$ ns,
   PRR = 1 MHz, and $Z_{out} \simeq 50\,\Omega$.
2) Inputs not specified are open.
3) C_L includes probe and Jig capacitance.
4) All diodes are BAY 71.

FIG. 37

TTL INTEGRATED CIRCUITS

T 7408
T 7409

QUAD 2-INPUT POSITIVE "AND" GATES

- TOTEM-POLE OUTPUTS (T 7408 only)
- OPEN COLLECTOR OUTPUTS (T 7409 only)
- DIODE-CLAMPED INPUTS
- NORMALIZED FAN-OUT OF 10
- 14-PIN PLASTIC DIP

The T 7408 and T 7409 are monolithic quad two input AND gates in a 14-lead dual in-line plastic package similar to Jedec TO-116.
The T 7408, with totem-pole outputs, drives 10 normalized Series 74 loads. The T 7409, with open-collector outputs, provides additional logic flexibility, as the outputs may be wire-AND connected to extend the AND function. They are available in the standard temperature range (0 to +70 °C).

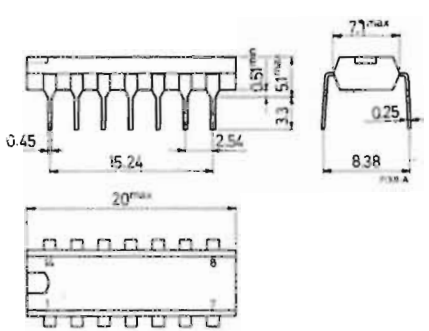
ABSOLUTE MAXIMUM RATINGS

V_{CC}	Supply voltage	7	V
V_i	Input voltage	5.5	V
V_{IE}	Interemitter voltage	5.5	V
V_{OH}	Output high voltage (T 7409 only)	5.5	V
T_{op}	Operating temperature	0 to 70	°C
T_{stg}	Storage temperature	-65 to 150	°C

ORDERING NUMBERS: T 7408 B1, T 7409 B1.

MECHANICAL DATA

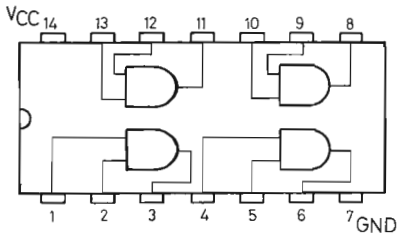
Dimensions in mm



similar to **TO-116**

T 7408
T 7409

CONNECTION DIAGRAM (top view)



RECOMMENDED OPERATING CONDITIONS

V_{CC}	Supply voltage	4.75 to 5.25	V
N	Normalized fan-out from each output	max 10	—
T_{op}	Operating temperature	0 to 70	°C

ELECTRICAL CHARACTERISTICS

(over recommended operating conditions unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.*	Max.	Unit	Fig.
V_{IH}	Input high voltage		2			V	1
V_{IL}	Input low voltage				0.8	V	2
V_{OH}	Output high voltage (for T 7408 only)	V_{CC} = 4.75 V V_{IN} = 2 V I_{OH} = -800µA	2.4			V	1
V_{OL}	Output low voltage	V_{CC} = 4.75 V V_{IN} = 0.8 V I_{OL} = 16 mA			0.4	V	2
I_{IH}	Input high current (each input)	V_{CC} = 5.25 V V_{IN} = 2.4 V V_{CC} = 5.25 V V_{IN} = 5.5 V			40 1	µA mA	3
I_{IL}	Input low current (each input)	V_{CC} = 5.25 V V_{IN} = 0.4 V			-1.6	mA	4
I_{CEX}	Output leakage current (for T 7409 only)	V_{CC} = 4.75 V V_{IN} = 2 V V_{OH} = 5.5 V			250	µA	1
I_{SC}**	Short-circuit output current (for T 7408 only)	V_{CC} = 5.25 V	-18		-55	mA	5

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test Conditions	Min.	Typ.*	Max.	Unit	Fig.
I_{CCL}	Supply current, low level output	V_{CC} = 5.25 V V_{IN} = 0		20	33	mA	6
I_{CCH}	Supply current, high level output	V_{CC} = 5.25 V V_{IN} = 5 V		11	21	mA	6

* All typical values are at V_{CC} = 5 V, T_{amb} = 25 °C.

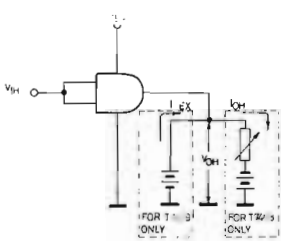
** Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_{amb} = 25 °C, N = 10)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit	Fig.
t_{pd0}	Propagation delay time to logical 0 level	C_L = 15 pF R_L = 400 Ω					
		for **T 7408**		12	19	ns	7-8
		for **T 7409**		16	24	ns	
t_{pd1}	Propagation delay time to logical 1 level	C_L = 15 pF R_L = 400 Ω					
		for T **7408**		17.5	27	ns	7-8
		for **T 7409**		21	32	ns	

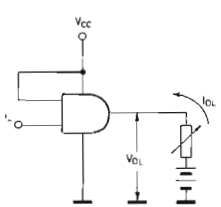
DC TEST CIRCUITS (Arrows indicate actual direction of current flow. Current into a terminal is a positive value).

Fig. 1 - V_{IH}, V_{OH}, I_{CEX}



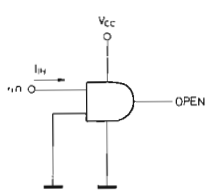
Both inputs are tested simultaneously.

Fig. 2 - V_{IL}, V_{OL}



Each input is tested separately.

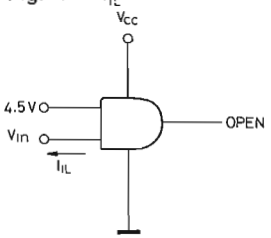
Fig. 3 - I_{IH}



Each input is tested separately.

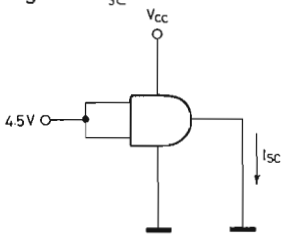
DC TEST CIRCUITS (continued)

Fig. 4 - I_{IL}



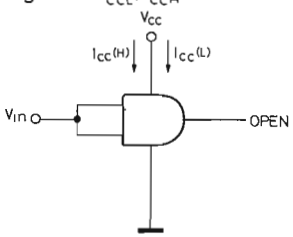
Each input is tested separately.

Fig. 5 - I_{SC}



Each gate is tested separately.

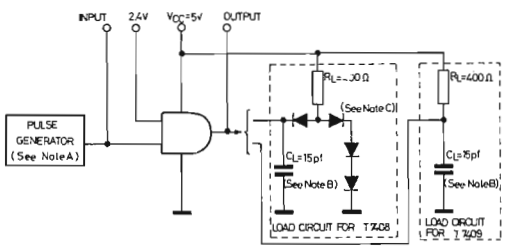
Fig. 6 - I_{CCL}, I_{CCH}



High level and low-level conditions are tested. All gates are tested simultaneously.

SWITCHING TIMES

Fig. 7 - Test circuit



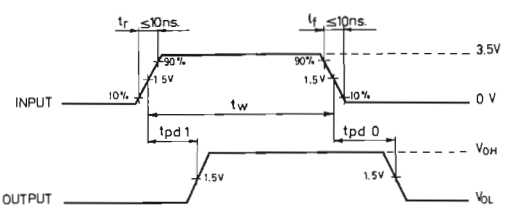
NOTES:

A) The generator has following characteristics: $t_{pw} = 0.5\ \mu s$; PRR = 1 MHz; $Z_{out} \approx 50\ \Omega$

B) C_L includes probe and jig capacitance

C) All diodes are 1N3064

Fig. 8 - Waveforms



Quad 2-input high-voltage interface NAND gate

STANDARD TEMPERATURE RANGE
0°C to 70°C

- OPEN COLLECTOR OUTPUT
- HIGH BREAKDOWN OUTPUT VOLTAGE
- TYPICAL APPLICATION AS DRIVER FOR LOW-THRESHOLD-VOLTAGE MOS INPUTS
- 14-PIN PLASTIC DIP

This open-collector NAND gate features high output voltage ratings for interfacing with low-threshold-voltage MOS logic circuits or other 12V systems. Although the output is rated to withstand 15V, the V_{CC} terminal is connected to the standard 5V source. The output transistor will sink 16mA while maintaining a low-level output voltage of 0.4V maximum, thus providing a high-fan-out driver with the nominal power dissipation of standard series T74 gates.

ABSOLUTE MAXIMUM RATINGS
(above which the useful life may be impaired)

Supply Voltage V_{CC} (1)	7V
Input Voltage (1 and 2)	5.5V
Output Voltage (1 and 3)	15V
Storage Temperature Range	-65°C to 150°C

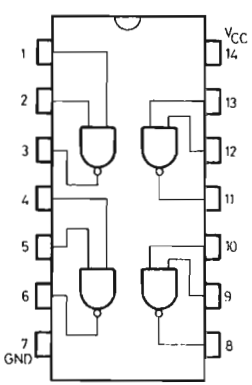
OPERATING CONDITIONS

Supply Voltage V_{CC} (1)	4.75V to 5.25V
Maximum Voltage on any Output (1)	12V
Free-Air Temperature Range	0°C to 70°C

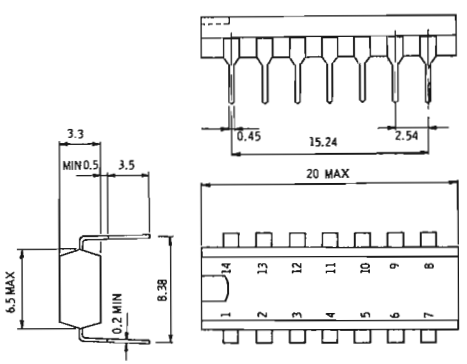
ORDERING NUMBER
T 7426 B1

Notes : see next page.

CONNECTION DIAGRAM



PHYSICAL DIMENSIONS
14-pin plastic DIP



Note : all dimensions in mm.

STANDARD TEMPERATURE RANGE

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

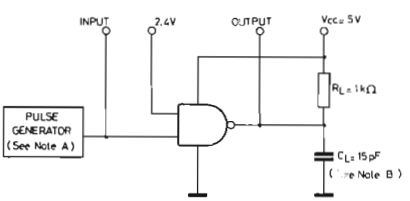
PARAMETER		TEST CONDITIONS (*)	Min.	Typ (**)	Max.	Unit
$V_{in(1)}$	Logical 1 input voltage required at either input terminal to ensure logical 0 level at output	V_{CC} =MIN	2			V
$V_{in(0)}$	Logical 0 input voltage required at both input terminals to ensure logical 1 level at output	V_{CC} =MIN			0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} =MIN V_{in}=0.8V, I_{load}=1mA	15			V
I_{off}	Off-state reverse current	V_{CC}=MIN V_{in}=0.8V, $V_{out(1)}$=12V			50	µA
$V_{out(0)}$	Logical 0 output voltage	V_{CC}=MIN V_{in}=2V, I_{sink}=16mA			0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC}=MAX V_{in}=0.4V			-1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC}=MAX V_{in}=2.4V V_{CC}=MAX V_{in}=5.5V			40 1	µA mA
$I_{CC(0)}$	Logical 0 level supply current	V_{CC}=MAX V_{in}=5V		12	22	mA
$I_{CC(1)}$	Logical 1 level supply current	V_{CC}=MAX V_{in}=0		4	8	mA

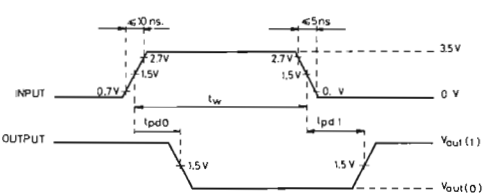
SWITCHING CHARACTERISTICS (V_{CC}=5V, T_A=25°C, N = 10)

PARAMETER		TEST CONDITIONS	Min.	Typ.	Max.	Unit
t_{pd0}	Propagation delay time to logical 0 level	C_L=15pF R_L=1KΩ		11	17	ns
t_{pd1}	Propagation delay time to logical 1 level	C_L=15pF R_L=1KΩ		16	24	ns

(*) For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions.
(**) All typical values are at V_{CC}=5V, T_A=25°C.

SWITCHING TIMES TEST CIRCUIT AND WAVEFORMS





Notes : A. The generator has the following characteristics: t_w = 0.5µs, PRR = 1MHz, Z_{out} ≈50Ω
B. C_L includes probe and jig capacitance

NOTES :
1) Voltage values are with respect to network ground terminal.
2) Input signals must be zero or positive with respect to network ground terminal.
3) This is the maximum voltage which should be applied to any output when it is in the off state.

T7442
T7443
T7444

4-LINE-TO-10-LINE DECODERS (1 - OF - 10)

- TYPICAL DC NOISE IMMUNITY OF 1 V
- TYPICAL POWER DISSIPATION OF 140 mW
- DIODE-CLAMPED INPUTS
- NORMALIZED FAN-OUT OF 10
- 16-PIN DUAL IN-LINE PLASTIC PACKAGE

These monolithic decimal decoders consist of eight inverters and ten four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. The T7442 BCD-to-decimal, T7443 excess-3-to-decimal, and T7444 excess-3-gray-to-decimal decoders feature familiar transistor-transistor-logic circuits with inputs and outputs which are compatible with other TTL and DTL circuits. Available in the standard temperature range (0 to 70°C), they come in 16-pin dual in-line plastic package.

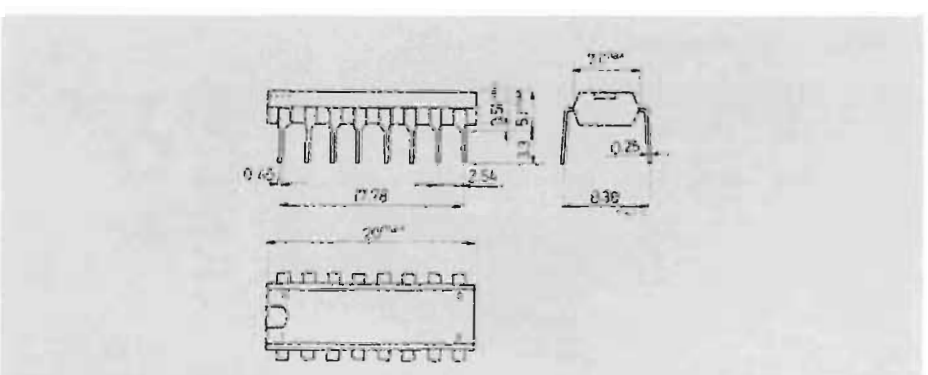
ABSOLUTE MAXIMUM RATINGS

V_{CC}	Supply voltage	7	V
V_i	Input voltage	5.5	V
T_{op}	Operating temperature	0 to 70	°C
T_{stg}	Storage temperature	-65 to 150	°C

ORDERING NUMBERS : T 7442 B1, T 7443 B1, T 7444 B1

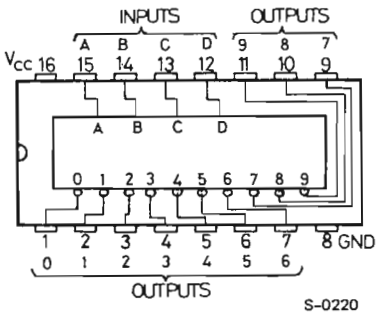
MECHANICAL DATA

Dimensions in mm



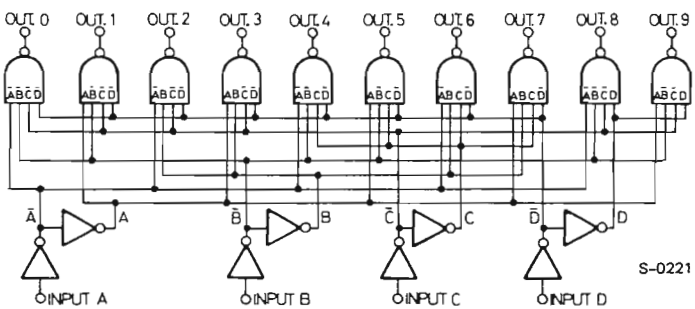
T7442
T7443
T7444

CONNECTION DIAGRAM (top view)

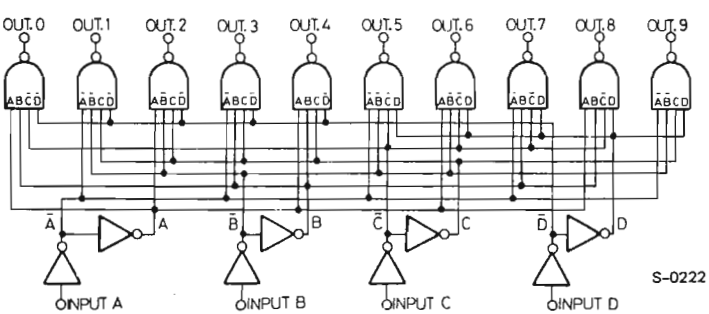


FUNCTIONAL LOGIC DIAGRAMS

T7442 BCD-to-decimal

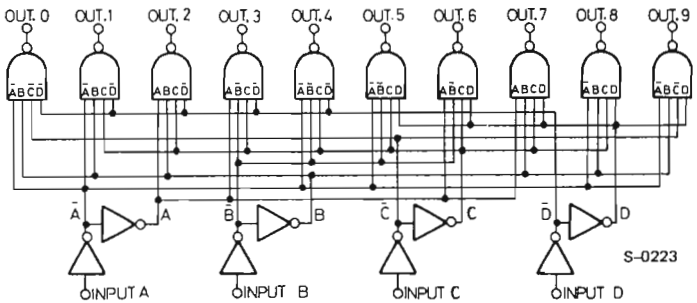


T 7443 Excess-3-to-decimal



FUNCTIONAL LOGIC DIAGRAMS (continued)

T 7444 Excess-3-gray-to-decimal



TRUTH TABLES

T7442 INPUT				T7443 INPUT				T7444 INPUT				ALL TYPES DECIMAL OUTPUT									
D	C	B	A	D	C	B	A	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	0	0	0	0	0	1	1	0	0	1	0	0	1	1	1	1	1	1	1	1	1
0	0	0	1	0	1	0	0	0	1	1	0	1	0	1	1	1	1	1	1	1	1
0	0	1	0	0	1	0	1	0	1	1	1	1	1	0	1	1	1	1	1	1	1
0	0	1	1	0	1	1	0	0	1	0	1	1	1	1	0	1	1	1	1	1	1
0	1	0	0	0	1	1	1	0	1	0	0	1	1	1	1	0	1	1	1	1	1
0	1	0	1	1	0	0	0	1	1	0	0	1	1	1	1	1	0	1	1	1	1
0	1	1	0	1	0	0	1	1	1	0	1	1	1	1	1	1	1	0	1	1	1
0	1	1	1	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1	0	1	1
1	0	0	0	1	0	1	1	1	1	1	0	1	1	1	1	1	1	1	1	0	1
1	0	0	1	1	1	0	0	1	0	1	0	1	1	1	1	1	1	1	1	1	0
1	0	1	0	1	1	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	0	1	0	0	1	1	1	1	1	1	1	1	1	1	1
1	1	0	0	1	1	1	1	1	0	0	0	1	1	1	1	1	1	1	1	1	1
1	1	0	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
1	1	1	0	0	0	0	1	0	0	0	1	1	1	1	1	1	1	1	1	1	1
1	1	1	1	0	0	1	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1

RECOMMENDED OPERATING CONDITIONS

V_{CC}	Supply voltage	4.75 to 5.25	V
N	Normalized fan-out from each output	max 10	–
T_{op}	Operating temperature	0 to 70	°C

ELECTRICAL CHARACTERISTICS

(over recommended operating conditions unless otherwise specified)

Parameter		Test Conditions	Min.	Typ.*	Max.	Unit	Fig.
V_{IH}	Input high voltage		2			V	1-2
V_{IL}	Input low voltage				0.8	V	1-2
V_{OH}	Output high voltage	V_{CC} = 4.75V V_{IH} = 2V V_{IL} = 0.8V I_{OH} = -400 µA	2.4			V	2
V_{OL}	Output low voltage	V_{CC} = 4.75V V_{IH} = 2V V_{IL} = 0.8V I_{OL} = 16mA			0.4	V	1
I_{IH}	Input high current (each input)	V_{CC} = 5.25V V_i = 2.4V V_{CC} = 5.25V V_i = 5.5V			40 1	µA mA	3
I_{IL}	Input low current (each input)	V_{CC} = 5.25V V_i = 0.4V			-1.6	mA	3
I_{SC}**	Short-circuit output current	V_{CC} = 5.25V	-18		- 55	mA	4
I_{CC}	Supply current	V_{CC} = 5.25V		28	56	mA	3

* All typical values are at V_{CC} = 5V, T_{amb} = 25°C

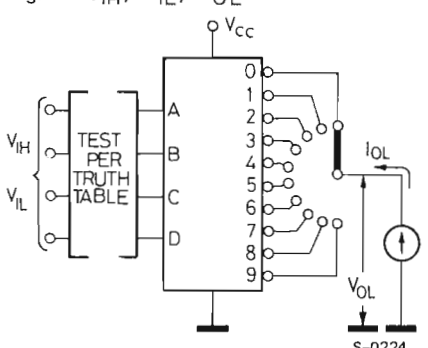
** Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS (V_{CC}=5V, T_{amb} = 25°C, N = 10)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit	Fig.
t_{pd0}	Propagation delay time to logical 0 level through two logic levels	C_L = 15 pF R_L = 400Ω	10	22	30	ns	5-6
t_{pd0}	Propagation delay time to logical 0 level through three logic levels	C_L = 15 pF R_L = 400Ω		23	35	ns	5-6
t_{pd1}	Propagation delay time to logical 1 level through two logic levels	C_L = 15 pF R_L = 400Ω	10	17	25	ns	5-6
t_{pd1}	Propagation delay time to logical 1 level through three logic levels	C_L = 15 pF R_L = 400 Ω		26	35	ns	5-6

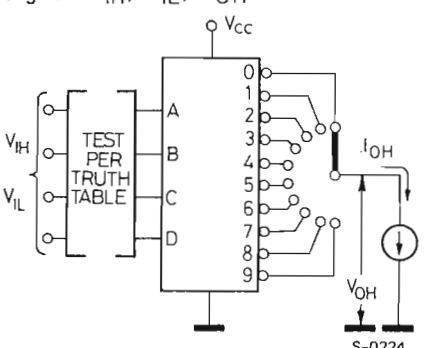
DC TEST CIRCUITS (Arrows indicate actual direction of current flow. Current into a terminal is a positive value).

Fig. 1 - V_{IH}, V_{IL}, V_{OL}



Each output is tested separately.

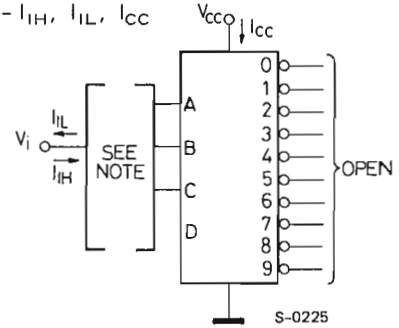
Fig. 2 – V_{IH}, V_{IL}, V_{OH}



Each output is tested separately.

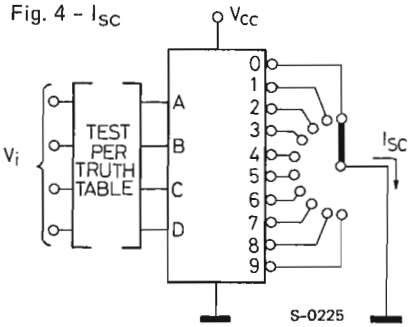
DC TEST CIRCUITS (continued)

Fig. 3 - I_{IH}, I_{IL}, I_{CC}



When testing I_{IH}, I_{IL} each input is tested separately.
When testing I_{CC} all inputs are grounded and outputs are open.

Fig. 4 - I_{SC}



Each output is tested separately

SWITCHING TIMES

Fig. 5 - Test circuit

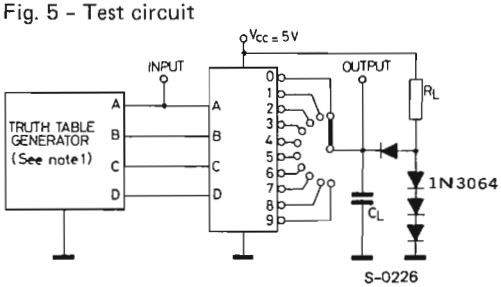
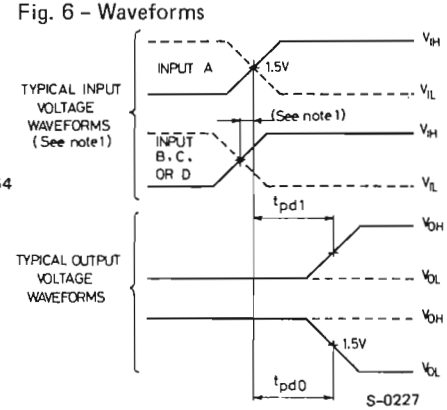


Fig. 6 - Waveforms



Notes :

1. The truth table generator has the following characteristics:
   $V_{OH} \geq 2.4$ V, $V_{OL} \leq 0.4$ V, t_r and $t_f < 10$ ns, and PRR = 1 MHz. Input B, C, and D transitions occur simultaneously with or prior to input A transitions.
2. C_L includes probe and jig capacitance.

Dual peripheral positive AND driver

STANDARD TEMPERATURE RANGE
0°C to 70°C

- OUTPUT CURRENT CAPABILITY 300mA
- HIGH-VOLTAGE OUTPUTS
- HIGH-SPEED SWITCHING
- CIRCUIT FLEXIBILITY FOR VARIED APPLICATIONS
- TTL OR DTL COMPATIBLE DIODE-CLAMPED INPUTS
- STANDARD SUPPLY VOLTAGE
- 8-PIN PLASTIC DIP

ORDERING NUMBER : T 75451A B1

The T 75451A is a dual peripheral driver designed for use in systems that employ TTL and DTL logic. Typical applications include high speed logic buffer, power driver, relay driver, lamp driver, MOS driver and memory driver. The T 75451A offers large freedom from latch-up, diode-clamped inputs to simplify system design and can drive lamps, relays, and memories to rated levels of voltage and current without external loading capacitors. The device is available in eight pin plastic mini-DIP.

ABSOLUTE MAXIMUM RATINGS
(above which the useful life may be impaired)

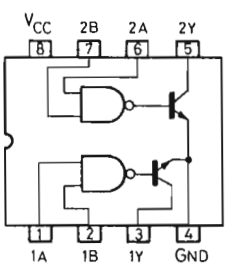
Supply Voltage V_{CC} (1)	7V
Input Voltage V_{in} (1 and 2)	5.5V
Intermitter Voltage (3)	5.5V
Continuous Output Current (5)	300 mA
Continuous Total Power Dissipation	800 mW
Storage Temperature Range	-65°C to 150°C

OPERATING CONDITIONS

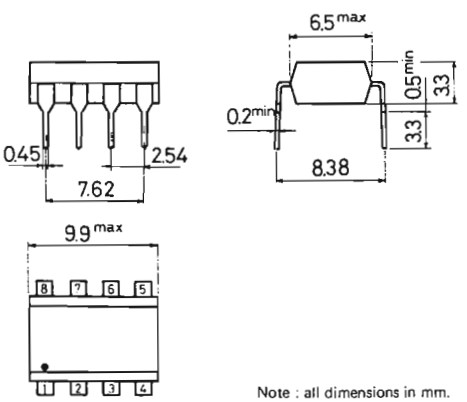
Supply Voltage V_{CC} (1)	4.75V to 5.25V
Maximum Voltage on any Output (1 and 4)	30V
Free-Air Temperature Range	0°C to 70°C

NOTES : see next page.

CONNECTION DIAGRAM



PHYSICAL DIMENSIONS
8-pin plastic DIP
(MINI DIP)



Note : all dimensions in mm.

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS (*)	Min.	Typ.(**)	Max.	Unit
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 (on) level at output	V_{CC} = MIN	2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 (off) level at output	V_{CC} = MIN			0.8	V
V_c	Input clamp voltage	V_{CC} = MIN I_C = -12mA			- 1.5	V
$I_{out(1)}$	Output reverse current	V_{CC} = MIN V_{in} = 2V $V_{out(1)}$ = 30V			100	µA
$V_{out(0)}$	Logical 0 output voltage (on level)	V_{CC} = MIN V_{in} = 0.8V I_{sink} = 100mA			0.4	V
		V_{CC} = MIN V_{in} = 0.8V I_{sink} = 300mA			0.7	V
$I_{in(0)}$	Logical 0 level input current (each input)	V_{CC} = MAX V_{in} = 0.4V			- 1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	V_{CC} = MAX V_{in} = 2.4V			40	µA
		V_{CC} = MAX V_{in} = 5.5V			1	mA
$I_{CC(0)}$	Logical 0 level supply current	V_{CC} = MAX V_{in} = 0		52	65	mA
$I_{CC(1)}$	Logical 1 level supply current	V_{CC} = MAX V_{in} = 5V		7	11	mA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C)

PARAMETER		TEST CONDITIONS	Min.	Typ.	Max.	Unit
t_{pd0}	Propagation delay time to logical 0 level	$I_{sink} \approx$ 200mA C_L = 15pF R_L = 50Ω		45		ns
t_{pd1}	Propagation delay time to logical 1 level			25		ns
t_{T0}	Transition time, high-to-low level output			12		ns
t_{T1}	Transition time, low-to-high level output			10		ns

(*) For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions.

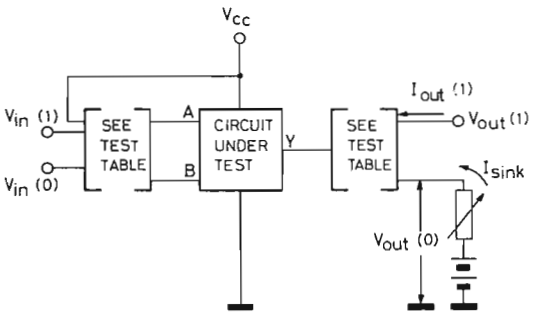
(**) All typical values at V_{CC} = 5V, T_A = 25°C.

NOTES :

1) These voltage values are with respect to network ground terminal unless otherwise specified.
2) Input signals must be zero or positive with respect to network ground terminal.
3) This is the voltage between two emitters of a multiple emitter transistor.
4) This is the maximum voltage which should be applied to any output when it is in the off state.
5) Both halves of this dual circuit may conduct rated current simultaneously.

DC TEST CIRCUITS (arrows indicate actual direction of current flow. Current into a terminal is a positive value)

$V_{in(1)} - V_{in(0)} - I_{out(1)} - V_{out(0)}$ TEST CIRCUIT

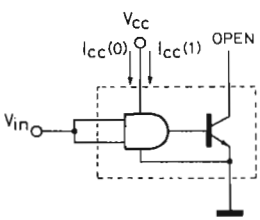


TEST TABLE

INPUT UNDER TEST	OTHER INPUT	OUTPUT	
		APPLY	MEASURE
$V_{in(1)}$	$V_{in(1)}$	$V_{out(1)}$	$I_{out(1)}$
$V_{in(0)}$	V_{CC}	I_{out} (0)	$V_{out(0)}$

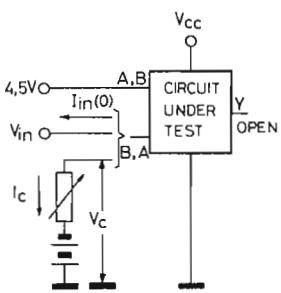
Note : Each input is tested separately

$I_{CC(0)}$ - $I_{CC(1)}$ TEST CIRCUIT



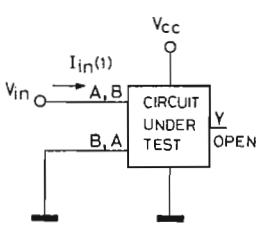
Note : Both gates are tested simultaneously

V_C - $I_{in(0)}$ TEST CIRCUIT



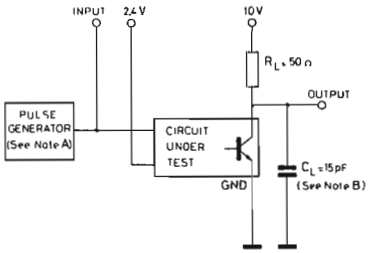
Note : Each input is tested separately

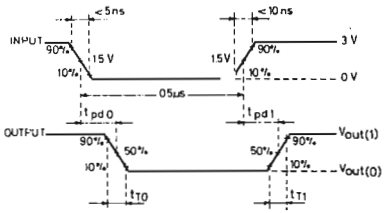
$I_{in(1)}$ TEST CIRCUIT



Note : Each input is tested separately

SWITCHING TIME TEST CIRCUITS AND WAVEFORMS

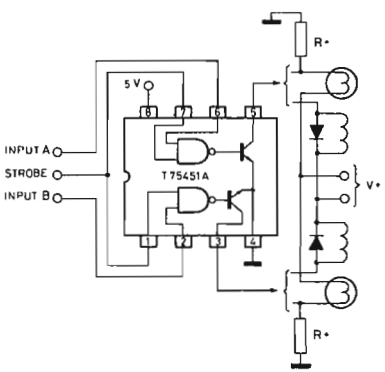




Notes :
A) The pulse generator has the following characteristics : PRR = 1 MHz, $Z_{out} \approx 50\Omega$
B) C_L includes probe and jig capacitance.

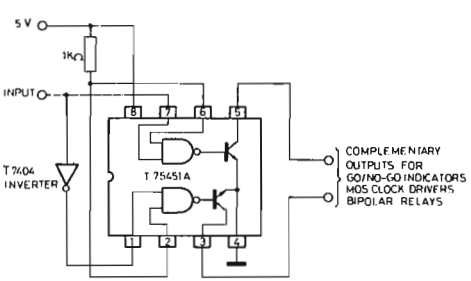
TYPICAL APPLICATION DATA

A) DUAL LAMP OR RELAY DRIVER



Note: Optional keep alive resistors, maintain off-state lamp current at ≈ 10% to reduce surge current.

B) COMPLEMENTARY DRIVER



HLL INTEGRATED CIRCUITS

HLL INTEGRATED CIRCUITS

HLL H 100 SERIES

GATES	Page I.	Page S.
H 102	377	393
H 103	377	393
H 104	377	393
H 105	407	407
H 109	378	394
H 122	384	400
H 124	384	400

FLIP-FLOPS	Page I.	Page S.
H 110	379	395
H 111	379	395

OTHER FUNCTIONS	Page I.	Page S.
H 112 Hex inverter (open collector)	409	409
H 113 High to low level converter	381	397
H 114 Low to high level converter	383	399
H 115 Hex inverter with strobe (open collector)	411	411
H 117 One-shot multivibrator	413	413
H 118 Hex inverter (active pull-up)	419	419
H 119 Hex inverter with strobe (active pull-up)	421	421
H 156 Binary counter	423	423
H 157 BCD counter	—	429
H 158 BCD to decimal decoder/driver	—	433

I. = Intermediate temperature range
S. = Standard temperature range

High level logic family

INTERMEDIATE TEMPERATURE RANGE
-40°C TO 85°C

- WIDE RANGE OF SUPPLY VOLTAGE 10.8V TO 16V
- HIGH DC NOISE IMMUNITY 5V (TYP.) AT V_{CC} = 15V
- HIGH FAN-OUT 25 (WORST CASE)
- COMPATIBLE WITH MOS I C's (Note 2)

High Level Logic is a family of high threshold integrated circuits.
It offers the advantages of 5V DC noise immunity, high signal levels, large supply voltage tolerances and unusually high fan-out.
These features make the family particularly suitable for industrial, avionic and telephone applications where the high noise environment might prohibit the use of a low threshold integrated circuit.
The H 100 series elements are available in the hermetically sealed ceramic dual in-line package.

ABSOLUTE MAXIMUM RATINGS (Note 1)

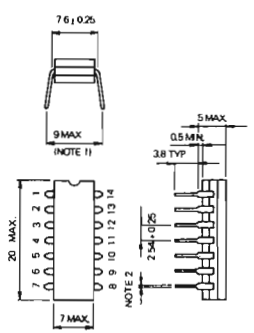
Supply Voltage (V_{CC}) continuous		18V
Input Voltage	-0.5V to	16V
Storage Temperature Range	-65° C to	150° C

OPERATING CONDITIONS

Operating Temperature	-40° C to	85° C
Supply Voltage	10.8V to	16V

Notes on following page.

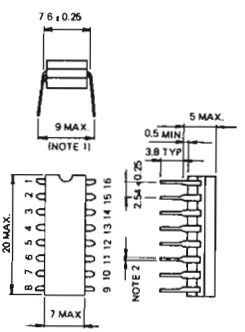
PHYSICAL DIMENSIONS
14 pin ceramic DIP



NOTES

1) Leads are intended for insertion in hole rows on 7.6 mm. centres. They are purposely shipped with "positive" (9 mm.) misalignment to facilitate insertion.
2) Board-drilling dimensions should equal your practice for a conventional 0.1 mm. diameter lead.
3) All dimensions in mm.

PHYSICAL DIMENSIONS
16 pin ceramic DIP



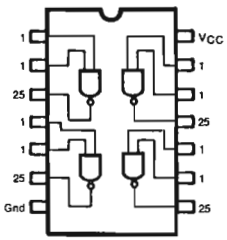
NOTES

1) Leads are intended for insertion in hole rows on 7.6 mm. centres. They are purposely shipped with "positive" (9 mm.) misalignment to facilitate insertion.
2) Board-drilling dimensions should equal your practice for a conventional 0.51 mm. diameter lead.
3) All dimensions in mm.

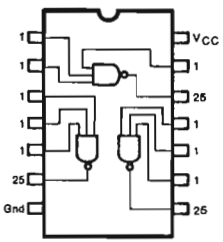
ORDERING NUMBER

HXXX D6 (XXX is type number)

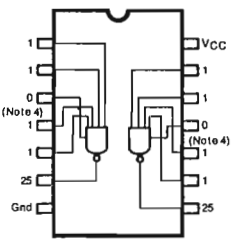
INPUT-OUTPUT LOAD/DRIVE FACTORS (T_A = -40° C to 85° C; V_{CC} = 10.8V to 16V)



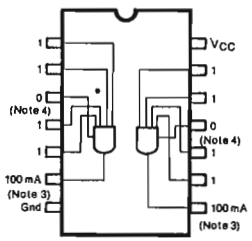
H 102



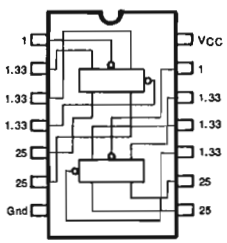
H 103



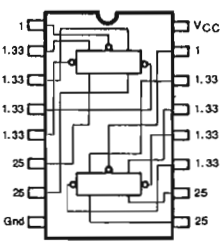
H 104



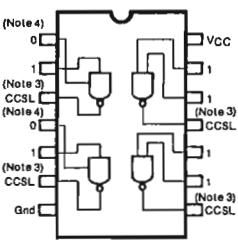
H 109



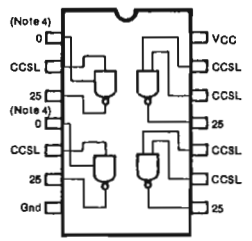
H 110



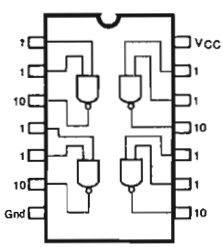
H 111



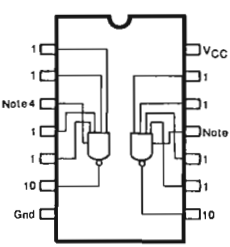
H 113



H 114



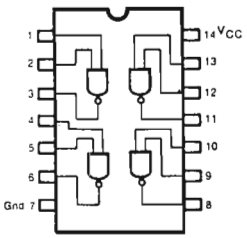
H 122



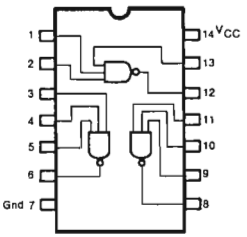
H 124

NOTES: 1) Ratings above which the useful life may be impaired
2) For details please refer to MOS IC's data sheet
3) The outputs of H 109 and H 113 are open transistor collectors and therefore need external pull-up resistors.
4) The expander input has a loading factor of 2.75 when connected with appropriate diodes (EB 383)

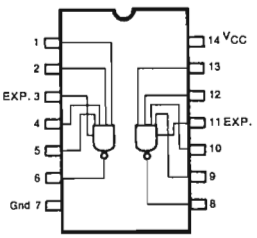
CONNECTION DIAGRAMS (Top view)



H 102

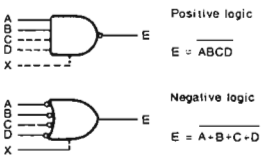


H 103

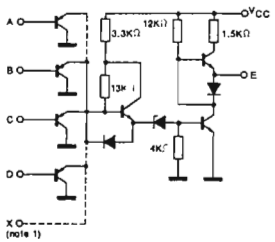


H 104

LOGIC FUNCTION



SCHEMATIC DIAGRAM
(one gate only)

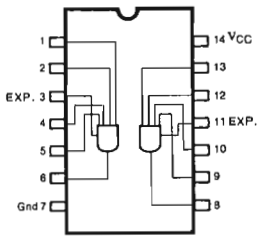


ELECTRICAL CHARACTERISTICS

SYMBOL	CHARACTERISTIC	−40°C		25°C			85°C		UNIT	CONDITIONS	
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.			
V_{OH}	Output High Voltage	14.5 9.3		14.5 9.3	15 9.8		14.5 9.3		V V	V_{CC} = 16V V_{CC} = 10.8V V_{IN} = V_{IL}	I_{OH} = −200μA I_{OH} = −200μA (see below)
V_{OL}	Output Low Voltage		1.5		1	1.5		1.5	V	V_{CC} = 16V V_{CC} = 10.8V V_{IN} = V_{IH}	I_{OL} = 12.5mA I_{OL} = 9mA (see below)
V_{IL}	Input Low Voltage		6			6		6	V	Guaranteed Input Low Threshold for All Inputs	
V_{IH}	Input High Voltage	8		8			8		V	Guaranteed Input High Threshold for All Inputs	
I_F	Input Low Current		-0.5 -0.36		-0.08 -0.06	-0.5 -0.36		-0.5 -0.36	mA mA	V_{CC} = 16V V_{CC} = 10.8V	V_F = 1.5V
I_{FEX}	Expander Input Low Current (Note 2)		-1.4 -1		-0.9 -0.75	-1.4 -1		-1.4 -1	mA mA	V_{CC} = 16V V_{CC} = 10.8V	V_{FEX} = 2V
I_R	Reverse Input Current		5		0.1	5		5	μA	V_{CC} = 16V	V_R = 16V
I_{SC}	Output Short Circuit Current	-6.5	-20	-6.5	-13.5	-20	-6.5	-20	mA	V_{CC} = 16V	Inputs and Output Grounded
I_{PDH}	High Level Power Dissipation Current (Each Gate)		6		4.4	6		6	mA	V_{CC} = 16V	Inputs High
I_{PDL}	Low Level Power Dissipation Current (Each Gate)		2		1.2	2		2	mA	V_{CC} = 16V	Inputs Low
TPD+	Turn-Off Delay				160	250			nsec	V_{CC} = 15V	See Test Circuit
TPD−	Turn-On Delay				50	100			nsec	V_{CC} = 15V	See Test Circuit

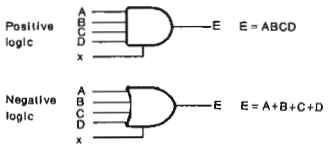
NOTES: 1) The node can be expanded using EB 383 or BAY 72 diodes
2) For H 104 only

CONNECTION DIAGRAM (top view)

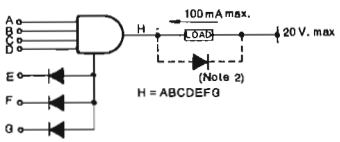


H 109

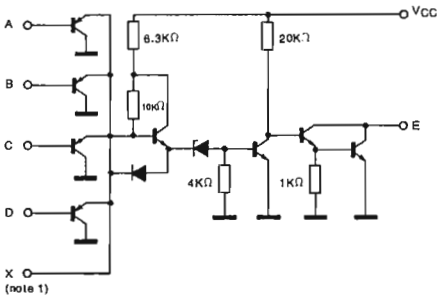
LOGIC FUNCTION



USE OF H109 POWER GATE



SCHEMATIC DIAGRAM (one gate only)

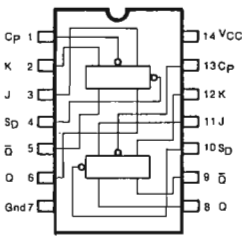


ELECTRICAL CHARACTERISTICS

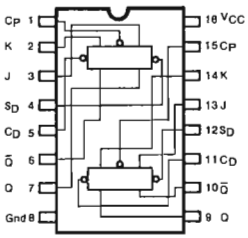
SYMBOL	CHARACTERISTIC	−40°C		25°C			85°C		UNIT	CONDITIONS
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.		
V_{OL}	Output Low Voltage		1.5		1	1.5		1.5	V	V_{CC} = 16V.or 10.8V; I_{OL} = 100mA; V_{IN} = V_{IL} (see below)
V_{IL}	Input Low Voltage		6			6		6	V	Guaranteed Input Low Threshold for All Inputs
V_{IH}	Input High Voltage	8		8			8		V	Guaranteed Input High Threshold for All Inputs
I_F	Input Low Current		-0.5 -0.36		-0.08 -0.06	-0.5 -0.36		-0.5 -0.36	mA mA	V_{CC} = 16V V_{CC} = 10.8V; V_F = 1.5V
I_{FEX}	Expander Input Low Current		-1.4 -1		-0.9 -0.75	-1.4 -1		-1.4 -1	mA mA	V_{CC} = 16V V_{CC} = 10.8V; V_{FEX} = 2V
I_R	Reverse Input Current		5		0.1	5		5	μA	V_{CC} = 16V V_R = 16V
I_{CEX}	Output Leakage Current		100			100		100	μA	V_{CC} = 16V V_{CEX} = 16V
I_{PDH}	High Level Power Dissipation Current (Each Gate)		4.75		3.5	4.75		4.75	mA	V_{CC} = 16V Inputs High
I_{PDL}	Low Level Power Dissipation Current (Each Gate)		3.75		2.6	3.75		3.75	mA	V_{CC} = 16V Inputs Low
TPD+	Turn-Off Delay				80	250			nsec	V_{CC} = 15V See Test Circuit
TPD−	Turn-On Delay				50	100			nsec	V_{CC} = 15V See Test Circuit

NOTES: 1) The node can be expanded using EB 383 or BAY 72 diodes
2) Use a diode when operating with an inductive load

CONNECTION DIAGRAMS (top view)

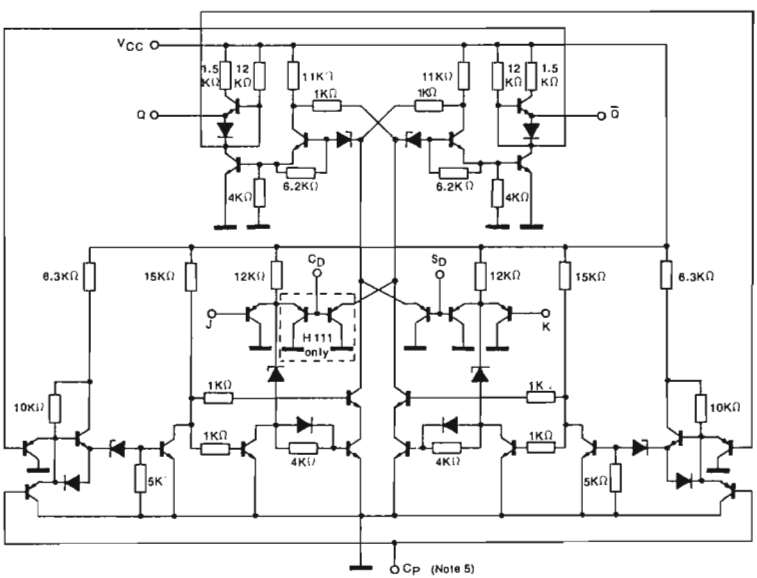


H 110 (Note 4)



H 111 (Note 4)

SCHEMATIC DIAGRAM (one flip-flop only)



TRUTH TABLES

Synchronous entry (note 1)			
time t_n		time t_n+1	
J	K	Q	$\bar{Q}$
H	H	$\bar{Q}_n$	Q_n
H	L	H	L
L	H	L	H
L	L	NC	NC

Asynchronous entry (note 2)			
inputs		outputs	
S_D	C_D (note 3)	Q	$\bar{Q}$
H	H	NC	NC
H	L	L	H
L	H	H	L
L	L	H	H

SYMBOLS:
NC = no change
Q_n = output state at time t_n

OUTPUTS:
L = V_{OL}
H = V_{OH}

INPUTS:
L = V_{IL}
H = V_{IH}

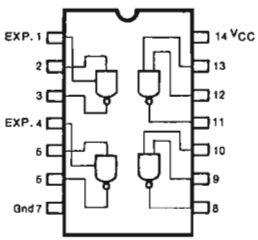
ELECTRICAL CHARACTERISTICS

SYMBOL	CHARACTERISTIC	−40°C		25°C			85°C		UNIT	CONDITIONS
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.		
V_{OH}	Output High Voltage	14.5 9.3		14.5 9.3	15 9.8		14.5 9.3		V V	V_{CC} = 16V V_{CC} = 10.8V V_{IN} see truth table — I_{OH} = -200μA
V_{OL}	Output Low Voltage		1.5			1.5		1.5	V	V_{CC} = 16V I_{OL} = 12.5mA V_{CC} = 10.8V I_{OL} = 9mA V_{IN} see truth table
V_{IL}	Input Low Voltage		6			6		6	V	Guaranteed Input Low Threshold for All Inputs
V_{IH}	Input High Voltage	8		8			8		V	Guaranteed Input High Threshold for All Inputs
I_F	Input Low Current (J-K-SD-CD Inputs)		-0.65 -0.48		-0.1 -0.08	-0.65 -0.48		-0.65 -0.48	mA mA	V_{CC} = 16V V_{CC} = 10.8V — V_F = 1.5V
I_{FCP}	Input Low Current (Clock Input)		-0.5 -0.36		-0.08 -0.06	-0.5 -0.36		-0.5 -0.36	mA mA	V_{CC} = 16V V_{CC} = 10.8V — V_{FCP} = 1.5V
I_R	Reverse Input Current (J-K Inputs)		5		0.1	5		5	μA	V_{CC} = 16V V_R = 16V
I_R	Reverse Input Current (CP-SD-CD Inputs)		10		0.2	10		10	μA	V_{CC} = 16V V_R = 16V
I_{SC}	Output Short Circuit Current	-6.5	-20	-6.5	-13.5	-20	-6.5	-20	mA	V_{CC} = 16V Output and Asynchronous Grounded
I_{PD}	Power Dissipation Current		28		22	28		28	mA	V_{CC} = 16V SD Grounded
TPD+	Turn-Off Delay				250	600			nsec	V_{CC} = 15V
TPD−	Turn-On Delay				200	400			nsec	See Test Circuit
f_{clock}	Toggle Frequency (Max Clock Frequency)			500	1000				kHz	

NOTES:
1) JK mode operation
2) Indipendent of clock and synchronous inputs
3) Truth table for H 110. C_D not connected
4) Unused flip flop input pins must be connected to V_{CC}
5) The fall time of the clock pulse must be lower than 1 μSEC/Volt.

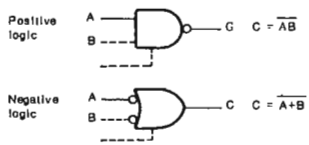
The H113 could be used as a quad high to low level converter or as a quad HLL gate with open collector output ORing function.

CONNECTION DIAGRAM (top view)

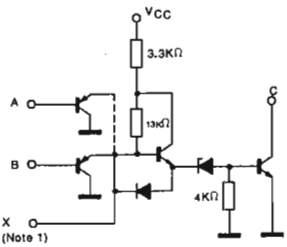


H 113

LOGIC FUNCTION



SCHEMATIC DIAGRAM (one gate only)



ELECTRICAL CHARACTERISTICS

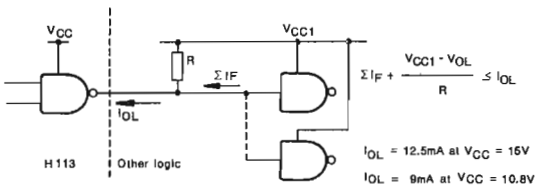
SYMBOL	CHARACTERISTIC	−40°C		25°C			85°C		UNIT	CONDITIONS	
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.			
V_{OL}	Output Low Voltage		0.45		0.3	0.45		0.45	V	V_{CC} = 16V V_{CC} = 10.8V V_{IN} = V_{IH}	I_{OL} = 12.5mA I_{OL} = 9mA (see below)
V_{IL}	Input Low Voltage		6			6		6	V	Guaranteed Input Low Threshold for All Inputs	
V_{IH}	Input High Voltage	8		8			8		V	Guaranteed Input High Threshold for All Inputs	
I_F	Input Low Current		-0.5 -0.36		-0.08 -0.06	-0.5 -0.36		-0.5 -0.36	mA mA	V_{CC} = 16V V_{CC} = 10.8V	V_F = 1.5V
I_{FEX}	Expander Input Low Current		-1.4 -1		-0.9 -0.75	-1.4 -1		-1.4 -1	mA mA	V_{CC} = 16V V_{CC} = 10.8V	V_{FEX} = 2V
I_R	Reverse Input Current		5		0.1	5		5	μA	V_{CC} = 16V	V_R = 16V
I_{CEX}	Output Leakage Current		80 24			80 24		80 24	μA μA	V_{CC} = 16V V_{CC} = 16V	V_{CEX} = 16V V_{CEX} = 5.25V
I_{PDH}	High Level Power Dissipation Current (Each Gate)		5		3.5	5		5	mA	V_{CC} = 16V	Inputs High
I_{PDL}	Low Level Power Dissipation Current (Each Gate)		2		1.2	2		2	mA	V_{CC} = 16V	Inputs Low
TPD+	Turn-Off Delay				110	250			nsec	V_{CC} = 15V See Test Circuit	
TPD−	Turn-On Delay				40	100			nsec		

USE OF H113 HIGH TO LOW LEVEL CONVERTER

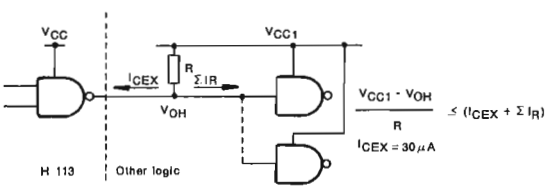
The output of H 113 is an open collector, therefore it needs a pull-up resistor.

The output swing is a function of the voltage at which the pull-up resistor is connected, so the H 113 could also be considered as an open collector HLL gate which allows the output OR-ing function.

1) OUTPUT LOW

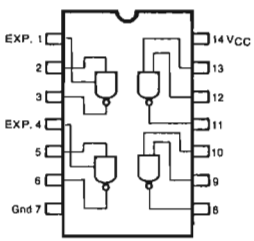


2) OUTPUT HIGH



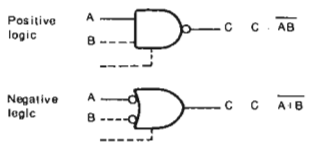
NOTE: 1) The node can be expanded using EB 383 or BAY 72 diodes

CONNECTION DIAGRAM (top view)

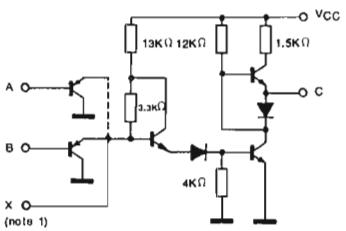


H 114

LOGIC FUNCTION



SCHEMATIC DIAGRAM (one gate only)

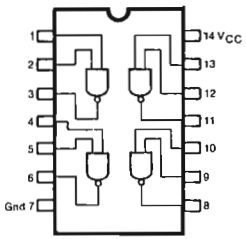


ELECTRICAL CHARACTERISTICS

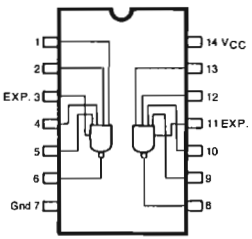
SYMBOL	CHARACTERISTIC	−40°C		25°C			85°C		UNIT	CONDITIONS	
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.			
V_{OH}	Output High Voltage	14.5 9.3		14.5 9.3	15 9.8		14.5 9.3		V V	V_{CC} = 16V V_{CC} = 10.8V V_{IN} = V_{IL}	I_{OH} = -200μA (see below)
V_{OL}	Output Low Voltage		1.5		1	1.5		1.5	V	V_{CC} = 16V V_{CC} = 10.8V V_{IN} = V_{IH}	I_{OL} = 12.5mA I_{OL} = 9mA (see below)
V_{IL}	Input Low Voltage		0.85			0.85		0.85	V	Guaranteed Input Low Threshold for All Inputs	
V_{IH}	Input High Voltage	2.1		1.8			1.55		V	Guaranteed Input High Threshold for All Inputs	
I_F	Input Low Current		-0.5 -0.36		-0.08 -0.06	-0.5 -0.36		-0.5 -0.36	mA mA	V_{CC} = 16V V_{CC} = 10.8V	V_F = 0.45V
I_{FEX}	Expander Input Low Current		-1.4 -1		-0.9 -0.75	-1.4 -1		-1.4 -1	mA mA	V_{CC} = 16V V_{CC} = 10.8V	V_{FEX} = 0.9V
I_R	Reverse Input Current		5		0.1	5		5	μA	V_{CC} = 16V	V_R = 4.5V
I_{SC}	Output Short Circuit Current	-6.5	-20	-6.5	-13.5	-20	-6.5	-20	mA	V_{CC} = 16V	Inputs and Output Grounded
I_{PDH}	High Level Power Dissipation Current (Each Gate)		4		3	4		4	mA	V_{CC} = 16V	Inputs High
I_{PDL}	Low Level Power Dissipation		2		1.2	2		2	mA	V_{CC} = 16V	Inputs Low
TPD+	Turn-Off Delay				160	250			nsec	V_{CC} = 15V See Test Circuit	
TPD−	Turn-On Delay				50	100			nsec		

NOTE: 1) The node can be expanded using the DTL 9933 or BAY 74 diodes

CONNECTION DIAGRAMS (top view)

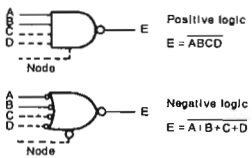


H 122

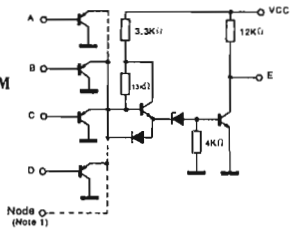


H 124

LOGIC FUNCTION



SCHEMATIC DIAGRAM
(one gate only)



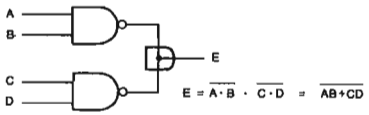
ELECTRICAL CHARACTERISTICS

SYMBOL	CHARACTERISTIC	-40°C		25°C			85°C		UNIT	CONDITIONS	
		Min.	Max.	Min.	Typ.	Max.	Min.	Max.			
V_{OH}	Output High Voltage	14.5 9.3		14.5 9.3	15 9.8		14.5 9.3		V V	V_{CC} = 16V V_{CC} = 10.8V V_{IN} = V_{IL}	I_{OH} = -50μA (see below)
V_{OL}	Output Low Voltage		1.5		0.2	1.5		1.5	V	V_{CC} = 16V V_{CC} = 10.8V V_{IN} = V_{IH}	I_{OL} = 12.5mA I_{OL} = 9mA (see below)
V_{IL}	Input Low Voltage		6			6		6	V	Guaranteed Input Low Threshold for All Inputs	
V_{IH}	Input High Voltage	8		8			8		V	Guaranteed Input High Threshold for All Inputs	
I_F	Input Low Current		-0.5 -0.36		-0.08 -0.06	-0.5 -0.36		-0.5 -0.36	mA mA	V_{CC} = 16V V_{CC} = 10.8V	V_F = 1.5V
I_{FEX}	Expander Input Low Current (H124 only)		-1.4 -1		-0.9 -0.75	-1.4 -1		-1.4 -1	mA mA	V_{CC} = 16V V_{CC} = 10.8V	V_{FEX} = 2V
I_R	Reverse Input Current		5		0.1	5		5	μA	V_{CC} = 16V	V_R = 16V
I_{CEX}	Output Leakage Current		45			45		45	μA	V_{CC} = 16V	V_{CEX} = 16V
I_{SC}	Output Short Circuit Current	-0.9	-2.05	-0.9	-1.6	-2.05	-0.9	-2.05	mA	V_{CC} = 16V	Inputs and Output Grounded
I_{PDH}	High Level Power Dissipation Current (Each Gate)		6		4.8	6		6	mA	V_{CC} = 16V	Inputs High
I_{PDL}	Low Level Power Dissipation Current (Each Gate)		2		1.2	2		2	mA	V_{CC} = 16V	Inputs Low
TPD+	Turn-Off Delay				250	400			nsec	V_{CC} = 15V	See Test Circuit
TPD−	Turn-On Delay				40	100			nsec	V_{CC} = 15V	

NOTES: 1) The node can be expanded using diode EB 383 or BAY 72
2) For H 124 only

WIRED - OR CONNECTION

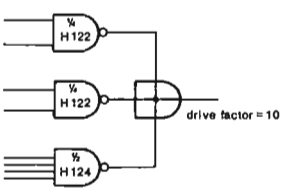
Outputs of H 122 and H 124 may be tied together for the wired - OR function.



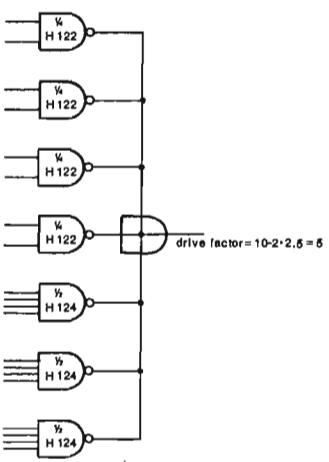
If 2, 3, 4, or 5 H 122 (or H 124) are OR-ed, the drive factor is 10.

For each additional gate over 5 a unit load of 2.5 should be subtracted from the drive factor of the gate.

EXAMPLE 1

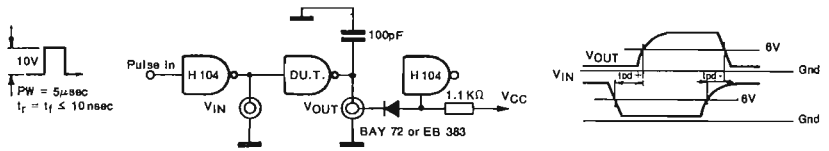


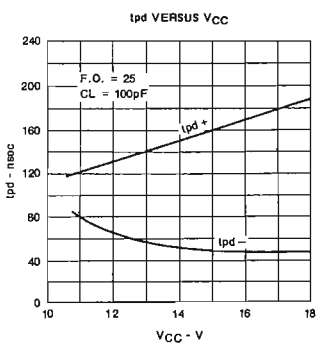
EXAMPLE 2

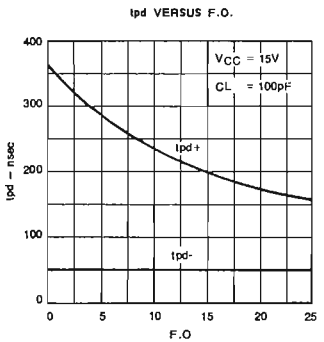


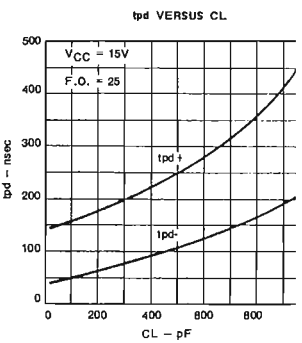
SWITCHING TIME TEST CIRCUITS

Gates H102-H103-H104

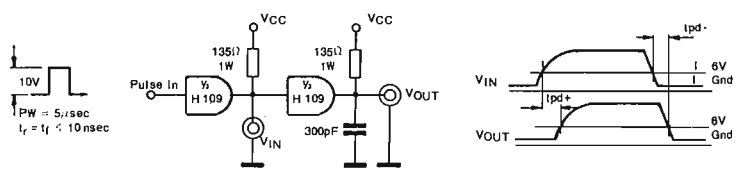


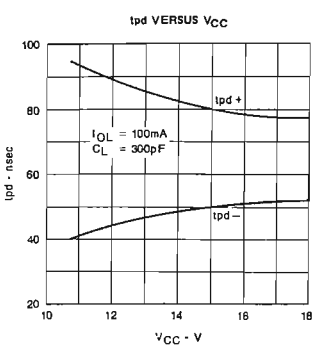


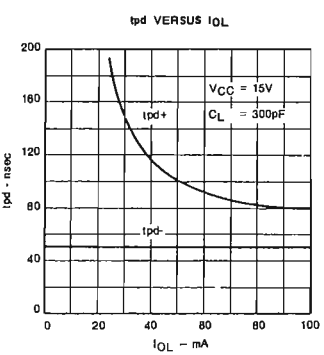


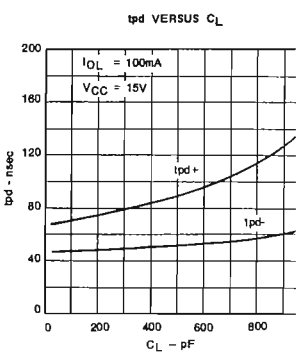


Power Gate H 109

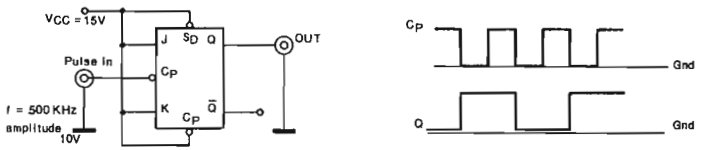




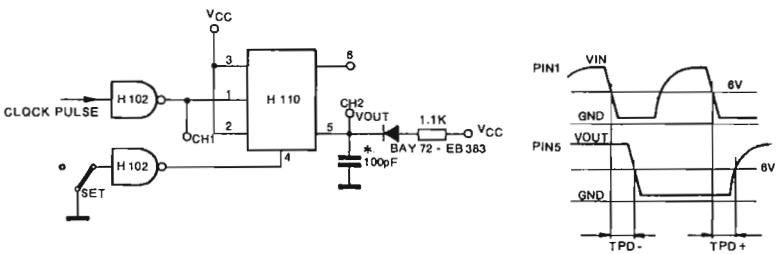




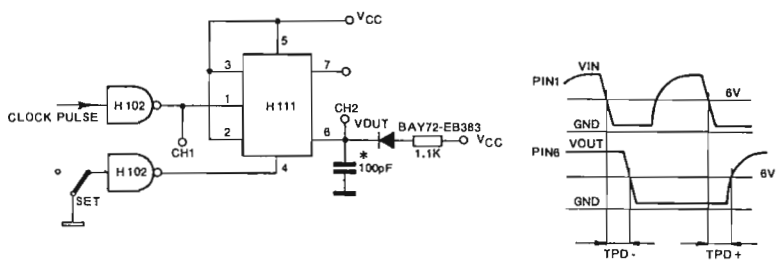
Dual J-K Flip-Flops H110-H111

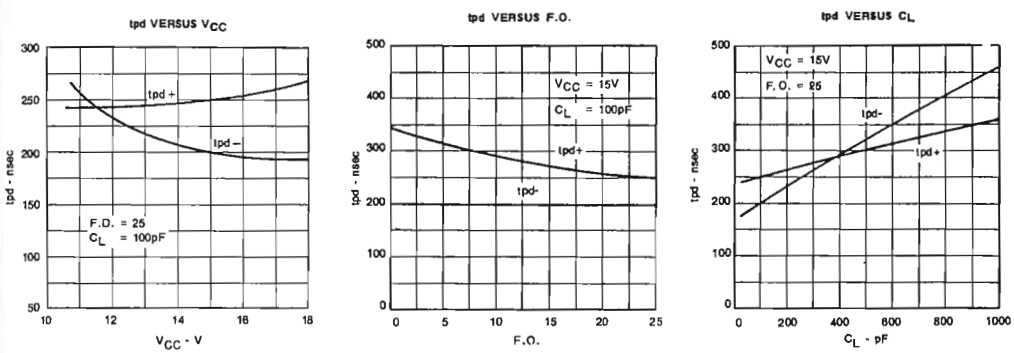


Dual J-K Flip-Flop H110



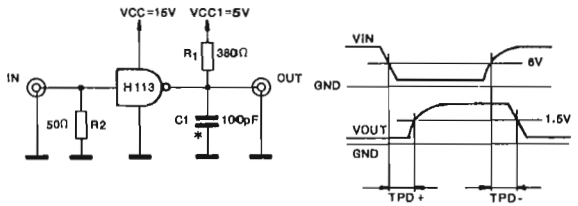
Dual J-K Flip-Flop H111

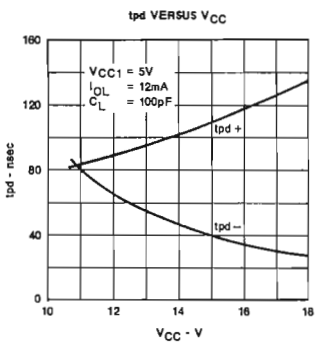


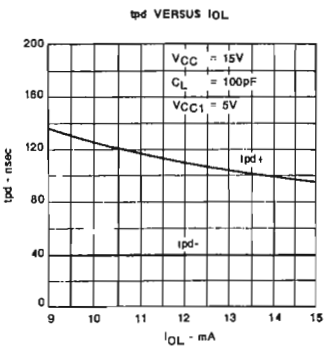


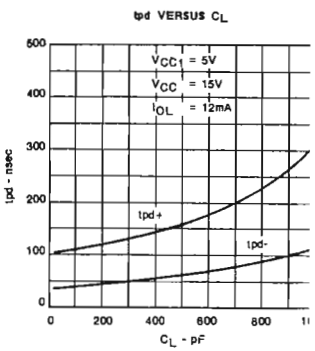
* The capacitance shall be within ± 5% including jig., probe and wiring capacitance.

High to Low Level Quad Converter H 113

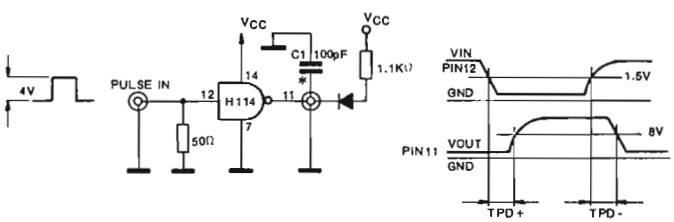


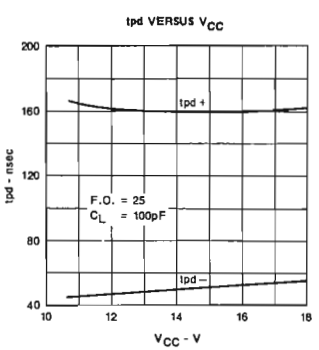


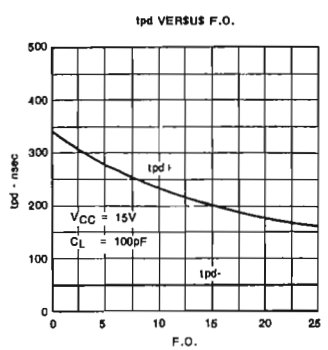


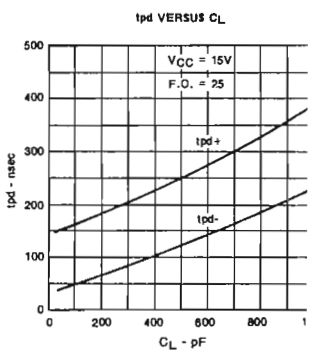


Low to High Level Quad Converter H 114



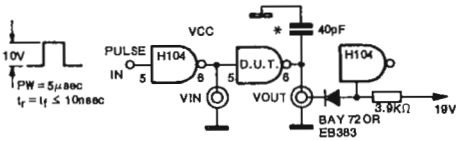


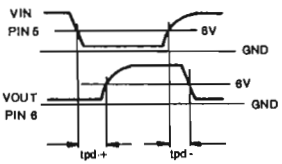




* The capacitance shall be within ± 5% including jig., probe and wiring capacitance.

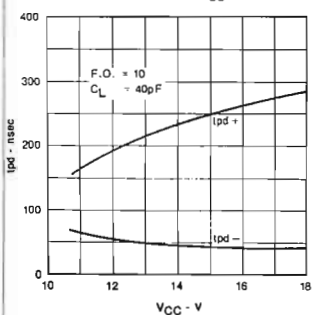
Gates With Passive Pull-Up H 122 - H 124



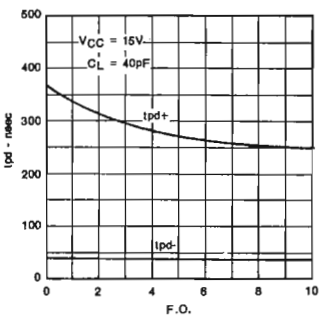


* The capacitance shall be within ± 5% including jig., probe and wiring capacitance.

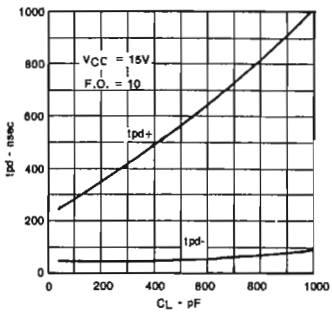
tpd VERSUS V_{CC}



tpd VERSUS F.O.

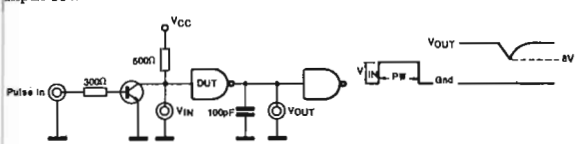


tpd VERSUS C_L

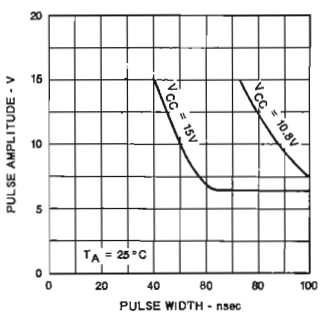


AC NOISE IMMUNITY TEST CIRCUIT (FOR GATES ONLY)

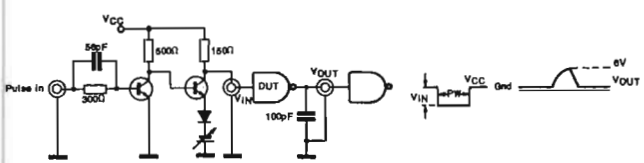
Input low



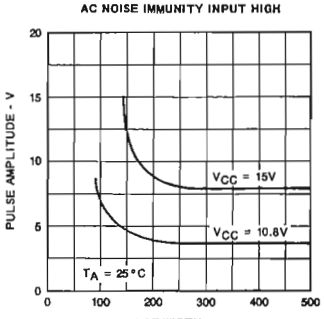
AC NOISE IMMUNITY INPUT LOW



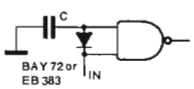
Input high

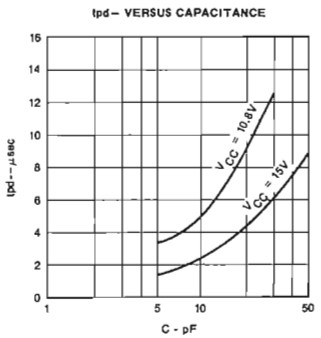


AC NOISE IMMUNITY INPUT HIGH

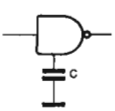


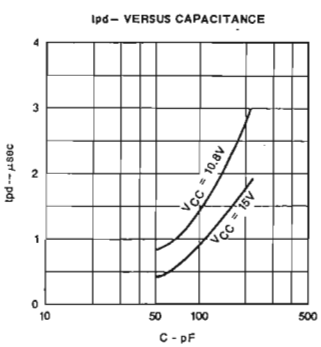
SLOW DOWN OF TPD - (FOR GATES)





SLOW DOWN OF TPD - (FOR EXPANDER)





High level logic family

STANDARD TEMPERATURE RANGE, 0°C TO 75°C

- WIDE RANGE OF SUPPLY VOLTAGE 10.8 TO 20V
- HIGH DC NOISE IMMUNITY 5V (TYP.) AT V_{CC}=15V
- HIGH FAN-OUT 25 (WORST CASE)
- COMPATIBLE WITH MOS I.C's (Note 2)

High Level Logic is a family of high threshold integrated circuits.
It offers the advantages of 5V DC noise immunity, high signal levels, large supply voltage tolerances and unusually high fan-out.
These features make the family particularly suitable for industrial, avionic and telephone applications where the high noise environment might prohibit the use of a low threshold integrated circuit.
The H 100 series elements are available in the hermetically sealed ceramic Dual-in-Line package.

ABSOLUTE MAXIMUM RATINGS (Note 1)

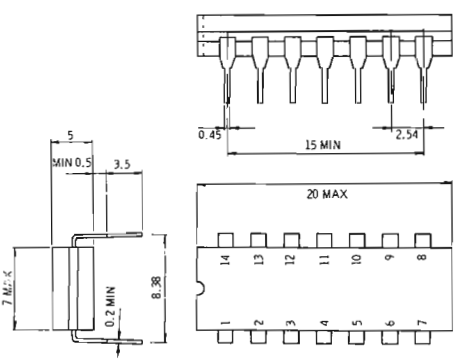
Supply Voltage (V_{CC}) continuous	22V
Input Voltage	-0.5V to 20V
Storage Temperature Range	-65°C to 150°C

OPERATING CONDITIONS

Operating Temperature	0°C to 75°C
Supply Voltage	10.8V to 20V

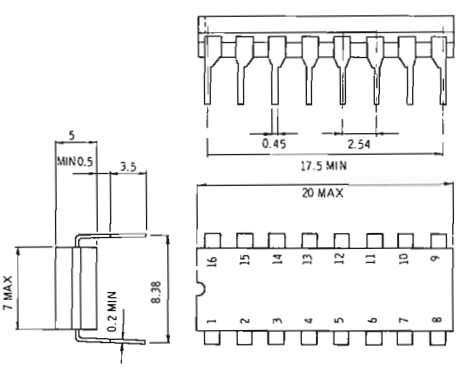
Notes on page 392

PHYSICAL DIMENSIONS
14-pin ceramic DIP



Note : all dimensions in mm.

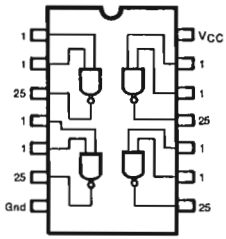
PHYSICAL DIMENSIONS
16-pin ceramic DIP



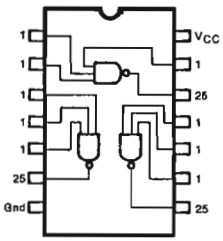
Note : all dimensions in mm.

ORDERING NUMBER
HXXX D1 (XXX is type number)

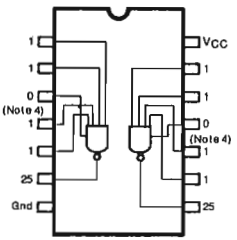
INPUT-OUTPUT LOAD/DRIVE FACTORS (T_A = 0°C to 75°C; V_{CC} = 10.8 V to 20 V)



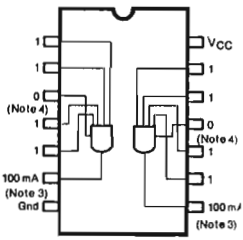
H 102



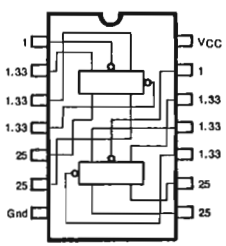
H 103



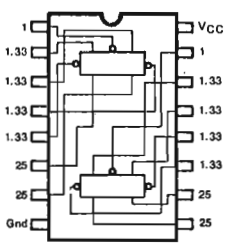
H 104



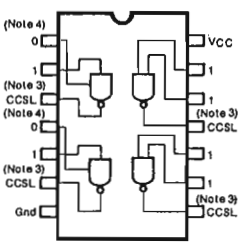
H 109



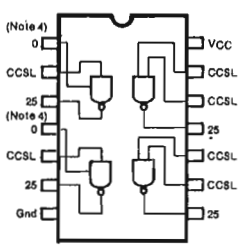
H 110



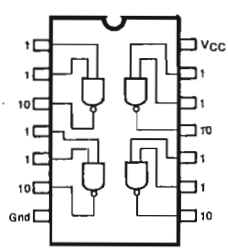
H 111



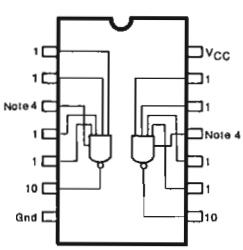
H 113



H 114



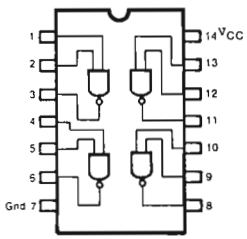
H 122



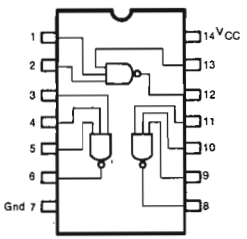
H 124

NOTES: 1) Ratings above which the useful life may be impaired
2) For details please refer to MOS I.C.'s data sheet
3) The outputs of H 109 and H 113 are open transistors collectors and therefore need external pull-up resistors.
4) The expander input has a loading factor of 2.75 when connected with appropriate diodes (EB 383)

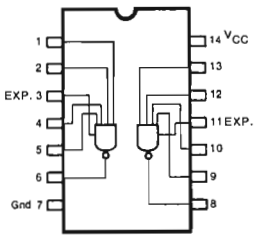
CONNECTION DIAGRAMS (Top view)



H 102

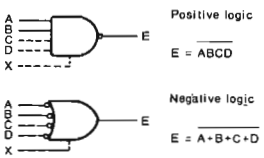


H 103

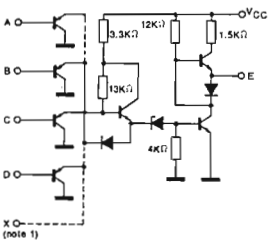


H 104

LOGIC FUNCTION



SCHEMATIC DIAGRAM
(one gate only)

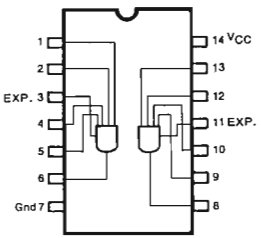


ELECTRICAL CHARACTERISTICS

SYMBOL	CHARACTERISTICS	LIMITS 0°C Min.	Max.	25°C Min.	Typ.	Max.	75°C Min.	Max.	Unit	CONDITIONS
V_{OH}	Output High Voltage	18.5		18.5	19		18.5		V	V_{CC} = 20V I_{OH} - 200µA
		13.5		13.5	14		13.5		V	V_{CC} = 15V I_{OH} - 200µA
		9.3		9.3	9.8		9.3		V	V_{CC} = 10.8V I_{OH} - 200µA V_{IN} = V_{IL} (see below)
V_{OL}	Output Low Voltage		1.5		1	1.5		1.5	V	V_{CC} = 20V I_{OL} = 15mA or V_{CC} = 15V I_{OL} = 12mA or V_{CC} = 10.8V I_{OL} = 9 mA V_{IN} = V_{IH} (see below)
V_{IL}	Input Low Voltage		6			6		6	V	Guaranteed Input Low Threshold for All Inputs
V_{IH}	Input High Voltage	8		8			8		V	Guaranteed Input High Threshold for All Inputs
I_F	Input Low Current		-0.6		-0.1	-0.6		-0.6	mA	V_{CC} = 20V
			-0.48		-0.08	-0.48		-0.48	mA	V_{CC} = 15V V_F = 1.5V
			-0.36		-0.06	-0.36		-0.36	mA	V_{CC} = 10.8V
I_{FEX}	Expander Input Low Current (Note 2)		-1.65		-1.25	-1.65		-1.65	mA	V_{CC} = 20V
			-1.33		-0.90	-1.33		-1.33	mA	V_{CC} = 15V V_{FEX} = 2V
			-1		-0.75	-1		-1	mA	V_{CC} = 10.8V
I_R	Reverse Input Current		5		0.1	5		5	µA	V_{CC} = 20V V_R = 20V
I_{SC}	Output Short Circuit Current	-9	-25	-9	-15	-25	-9	-25	mA	V_{CC} = 20V Inputs and Output Grounded
I_{PDH}	High Level Power Dissipation Current (Each Gate)		7.5		6	7.5		7.5	mA	V_{CC} = 20V Inputs High
I_{PDL}	Low Level Power Dissipation Current (Each Gate)		2.5		1.5	2.5		2.5	mA	V_{CC} = 20V Inputs Low
TPD_+	Turn-Off Delay				160	250			nS	V_{CC} = 15V See Test Circuit
TPD_-	Turn-On Delay				50	100			nS	V_{CC} = 15V See Test Circuit

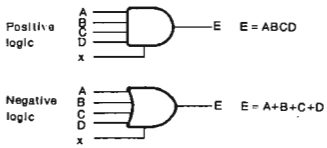
NOTES: 1) The node can be expanded using EB383 or BAY72 diodes
2) For H 104 only

CONNECTION DIAGRAM (top view)

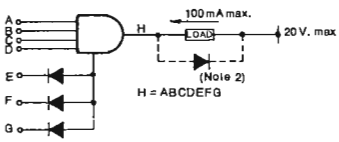


H 109

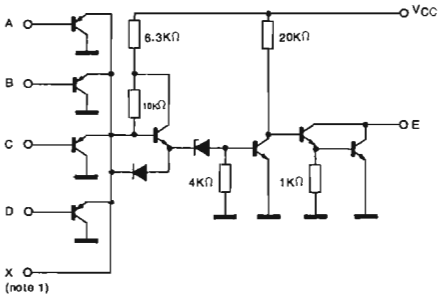
LOGIC FUNCTION



USE OF H109 POWER GATE



SCHEMATIC DIAGRAM (one gate only)

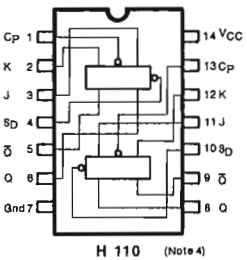


ELECTRICAL CHARACTERISTICS

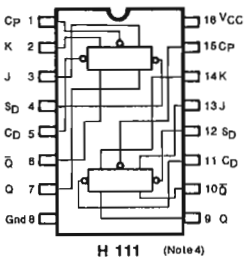
SYMBOL	CHARACTERISTICS	LIMITS 0°C Min.	0°C Max.	25°C Min.	25°C Typ.	25°C Max.	75°C Min.	75°C Max.	Unit	CONDITIONS
V_{OL}	Output Low Voltage		1.5		1	1.5		1.5	V	V_{CC} = 20V or 15V or 10.8V; I_{OL} = 100mA; $V_{IN} = V_{IL}$ (see below)
V_{IL}	Input Low Voltage		6			6		6	V	Guaranteed Input Low Threshold for All Inputs
V_{IH}	Input High Voltage	8		8			8		V	Guaranteed Input High Threshold for All Inputs
I_F	Input Low Current		-0.6		-0.1	-0.6		-0.6	mA	V_{CC} = 20V
			-0.48		-0.08	-0.48		-0.48	mA	V_{CC} = 15V; V_F = 1.5V
			-0.36		-0.06	-0.36		-0.36	mA	V_{CC} = 10.8V
I_{FEX}	Expander Input Low Current		-1.65		-1.25	-1.65		-1.65	mA	V_{CC} = 20V
			-1.33		-0.90	-1.33		-1.33	mA	V_{CC} = 15V; V_{FEX} = 2V
			-1		-0.75	-1		-1	mA	V_{CC} = 10.8V
I_R	Reverse Input Current		5		0.1	5		5	μA	V_{CC} = 20V; V_R = 20V
I_{CEX}	Output Leakage Current		100			100		100	μA	V_{CC} = 20V; V_{CEX} = 20V
I_{PDH}	High Level Power Dissipation Current (Each Gate)		6		4.5	6		6	mA	V_{CC} = 20V; Inputs High
I_{PDL}	Low Level Power Dissipation Current (Each Gate)		4.5		3.5	4.5		4.5	mA	V_{CC} = 20V; Inputs Low
TPD+	Turn-Off Delay				80	250			nS	V_{CC} = 15V; See Test Circuit
TPD-	Turn-On Delay				50	100			nS	V_{CC} = 15V; See Test Circuit

NOTES: 1) The node can be expanded using EB 383 or BAY 72 diodes
2) Use a diode when operating with an inductive load

CONNECTION DIAGRAMS (top view)

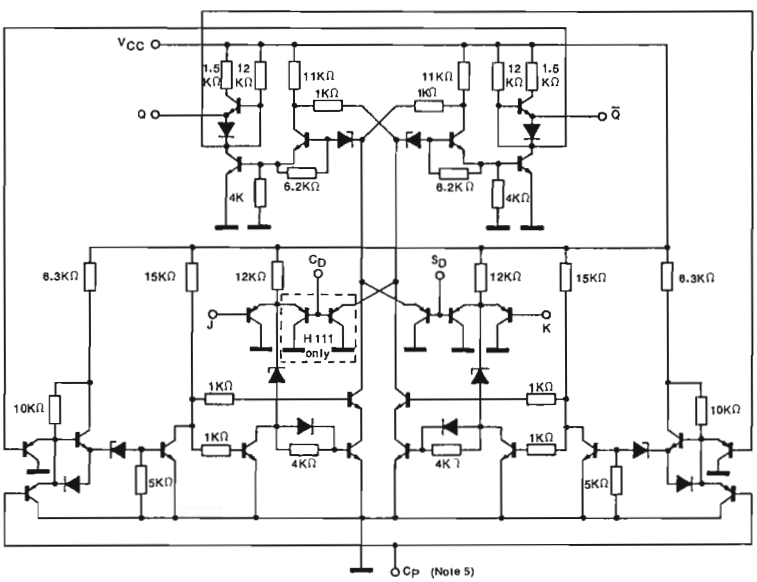


H 110 (Note 4)



H 111 (Note 4)

SCHEMATIC DIAGRAM (one flip-flop only)



TRUTH TABLES

Synchronous entry (note 1)			
time t_n		time t_n+1	
J	K	Q	$\bar{Q}$
H	H	$\bar{Q}_n$	Q_n
H	L	H	L
L	H	L	H
L	L	NC	NC

Asynchronous entry (note 2)			
inputs		outputs	
S_D	C_D (note 3)	Q	$\bar{Q}$
H	H	NC	NC
H	L	L	H
L	H	H	L
L	L	H	H

SYMBOLS:
NC = no change
Q_n = output state at time t_n

OUTPUTS:
L = V_{OL}
H = V_{OH}

INPUTS:
L = V_{IL}
H = V_{IH}

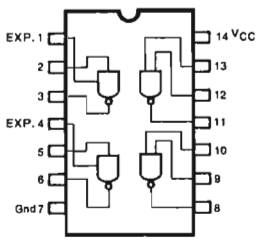
ELECTRICAL CHARACTERISTICS

SYMBOL	CHARACTERISTICS	LIMITS 0°C Min.	0°C Max.	25°C Min.	25°C Typ.	25°C Max.	75°C Min.	75°C Max.	Unit	CONDITIONS
V_{OH}	Output High Voltage	18.5		18.5	19		18.5		V	V_{CC} = 20V
		13.5		13.5	14		13.5		V	V_{CC} = 15V } I_{OH} = -200μA
		9.3		9.3	9.8		9.3		V	V_{CC} = 10.8V
										V_{IN} see truth table
V_{OL}	Output Low Voltage		1.5			1.5		1.5	V	V_{CC} = 20V I_{OL} = 15mA or
										V_{CC} = 15V I_{OL} = 12mA or
										V_{CC} = 10.8V I_{OL} = 9mA
										V_{IN} see truth table
V_{IL}	Input Low Voltage		6			6		6	V	Guaranteed Input Low Threshold for All Inputs
V_{IH}	Input High Voltage	8		8			8		V	Guaranteed Input High Threshold for All Inputs
I_F	Input Low Current (J-K-SD-CD Inputs)		-0.8		-0.130	-0.8		-0.8	mA	V_{CC} = 20V
			-0.64		-0.100	-0.64		-0.64	mA	V_{CC} = 15V } V_F = 1.5V
			-0.48		-0.08	-0.48		-0.48	mA	V_{CC} = 10.8V
I_{FCP}	Input Low Current (Clock Input)		-0.6		-0.1	-0.6		-0.6	mA	V_{CC} = 20V
			-0.48		-0.08	-0.48		-0.48	mA	V_{CC} = 15V } V_{FCP} = 1.5V
			-0.36		-0.06	-0.36		-0.36	mA	V_{CC} = 10.8V
I_R	Reverse Input Current (J-K Inputs)		5		0.1	5		5	μA	V_{CC} = 20V V_R = 20V
I_R	Reverse Input Current (CP, SD, CD Inputs)		10		0.2	10		10	μA	V_{CC} = 20V V_R = 20V
I_{SC}	Output Short Circuit Current	-9	-25	-9	-15	-25	-9	-25	mA	V_{CC} = 20V Output and Asynchronous Grounded
I_{PD}	Power Dissipation Current		35		24	35		35	mA	V_{CC} = 20V SD Grounded
TPD+	Turn-Off Delay				250	600			nS	} V_{CC} = 15V
TPD-	Turn-On Delay				200	400			nS	} See Test Circuit
f	Toggle Frequency			500	1000				KHz	

NOTES :
1) J-K mode operation
2) Independent of clock and synchronous inputs
3) Truth table for H 110. C_D not connected
4) Unused flip-flop input pins must be connected to V_{CC}
5) The fall time of the clock pulse must be lower than 1 μSEC/Volt.

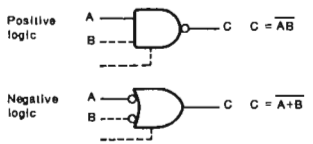
The H113 could be used as a quad high to low level converter or as a quad HLL gate with open collector output ORing function.

CONNECTION DIAGRAM (top view)

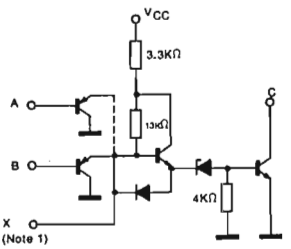


H 113

LOGIC FUNCTION



SCHEMATIC DIAGRAM (one gate only)



ELECTRICAL CHARACTERISTICS

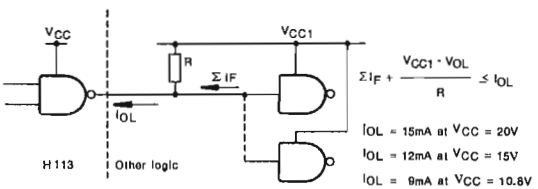
SYMBOL	CHARACTERISTICS	LIMITS 0°C Min.	0°C Max.	25°C Min.	25°C Typ.	25°C Max.	75°C Min.	75°C Max.	Unit	CONDITIONS
V_{OL}	Output Low Voltage		0.45		0.3	0.45		0.45	V	V_{CC} = 20V I_{OL} = 15mA or V_{CC} = 15V I_{OL} = 12mA or V_{CC} = 10.8V I_{OL} = 9mA V_{IN} = V_{IH} (see below)
V_{IL}	Input Low Voltage		6			6		6	V	Guaranteed Input Low Threshold for All Inputs
V_{IH}	Input High Voltage	8		8			8		V	Guaranteed Input High Threshold for All Inputs
I_F	Input Low Current		-0.6		-0.1	-0.6		-0.6	mA	V_{CC} = 20V
			-0.48		-0.08	-0.48		-0.48	mA	V_{CC} = 15V } V_F = 1.5V
			-0.36		-0.06	-0.36		-0.36	mA	V_{CC} = 10.8V
I_{FEX}	Expander Input Low Current		-1.65		-1.21	-1.65		-1.65	mA	V_{CC} = 20V
			-1.33		-0.90	-1.33		-1.33	mA	V_{CC} = 15V } V_{FEX} = 2V
			-1		-0.75	-1		-1	mA	V_{CC} = 10.8V
I_R	Reverse Input Current		5		0.1	5		5	μA	V_{CC} = 20V V_R = 20V
I_{CEX}	Output Leakage Current		100			100		100	μA	V_{CC} = 20V V_{CEX} = 20V
			30			30		30	μA	V_{CC} = 20V V_{CEX} = 5.25V
I_{PDH}	High Level Power Dissipation Current (Each Gate)		6		4.5	6		6	mA	V_{CC} = 20V Inputs High
I_{PDL}	Low Level Power Dissipation Current (Each Gate)		2.5		1.5	2.5		2.5	mA	V_{CC} = 20V Inputs Low
TPD+	Turn-Off Delay				110	250			nS	V_{CC} = 15V
TPD-	Turn-On Delay				40	100			nS	See Test Circuit

USE OF H113 HIGH TO LOW LEVEL CONVERTER

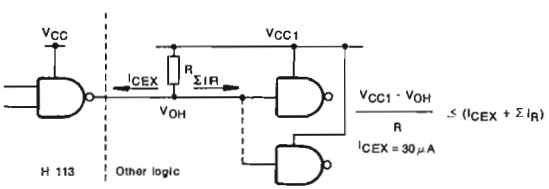
The output of H 113 is an open collector therefore it needs a pull-up resistor.

The output swing is a function of the voltage at which the pull-up resistor is connected, so the H 113 could also be considered as an open collector HLL gate which allows the output OR-ing function.

1) OUTPUT LOW

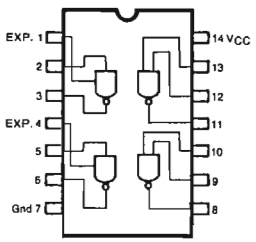


2) OUTPUT HIGH



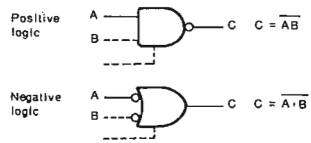
NOTE: 1) The node can be expanded using EB 383 or BAY 72 diodes

CONNECTION DIAGRAM (top view)

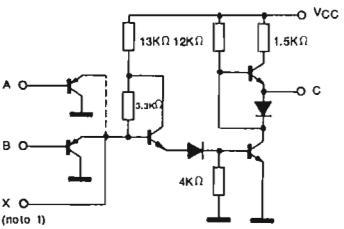


H 114

LOGIC FUNCTION



SCHEMATIC DIAGRAM (one gate only)

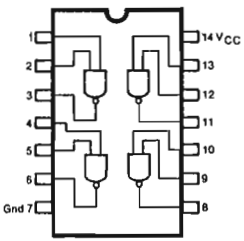


ELECTRICAL CHARACTERISTICS

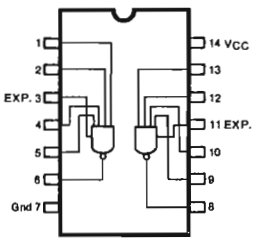
SYMBOL	CHARACTERISTICS	LIMITS 0°C Min.	Max.	25°C Min.	Typ.	Max.	75°C Min.	Max.	Unit	CONDITIONS
V_{OH}	Output High Voltage	18.5		18.5	19		18.5		V	V_{CC} = 20V
		13.5		13.5	14		13.5		V	V_{CC} = 15V
		9.3		9.3	9.8		9.3		V	V_{CC} = 10.8V } I_{OH} = -200μA
										V_{IN} = V_{IL} (see below)
V_{OL}	Output Low Voltage		1.5		1	1.5		1.5	V	V_{CC} = 20V I_{OL} = 15mA or V_{CC} = 15V I_{OL} = 12mA or V_{CC} = 10.8V I_{OL} = 9mA V_{IN} = V_{IH} (see below)
V_{IL}	Input Low Voltage		0.85			0.85		0.85	V	Guaranteed Input Low Threshold for All Inputs
V_{IH}	Input High Voltage	1.9		1.8			1.6		V	Guaranteed Input High Threshold for All Inputs
I_F	Input Low Current		-0.6		-0.1	-0.6		-0.6	mA	V_{CC} = 20V
			-0.48		-0.08	-0.48		-0.48	mA	V_{CC} = 15V } V_F = 0.45V
			-0.36		-0.06	-0.36		-0.36	mA	V_{CC} = 10.8V
I_{FEX}	Expander Input Low Current		-1.65		-1.25	-1.65		-1.65	mA	V_{CC} = 20V
			-1.33		-0.90	-1.33		-1.33	mA	V_{CC} = 15V } V_{FEX} = 0.9V
			-1		-0.75	-1		-1	mA	V_{CC} = 10.8V
I_R	Reverse Input Current		5		0.1	5		5	μA	V_{CC} = 20V V_R = 4.5V
I_{SC}	Output Short Circuit Current	-9	-25	-9	-15	-25	-9	-25	mA	V_{CC} = 20V Inputs and Output Grounded
I_{PDH}	High Level Power Dissipation Current (Each Gate)		5		4	5		5	mA	V_{CC} = 20V Inputs High
I_{PDL}	Low Level Power Dissipation		2.5		1.5	2.5		2.5	mA	V_{CC} = 20V Inputs Low
TPD+	Turn-Off Delay				160	250			nS	V_{CC} = 15V
TPD-	Turn-On Delay				50	100			nS	See Test Circuit

NOTE: 1) The node can be expanded using the DTL 9933 or BAY 74 diodes

CONNECTION DIAGRAMS (top view)

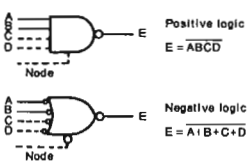


H 122

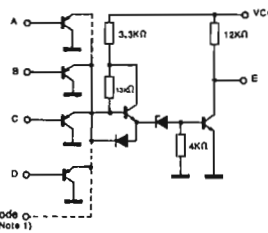


H 124

LOGIC FUNCTION



SCHEMATIC DIAGRAM
(one gate only)



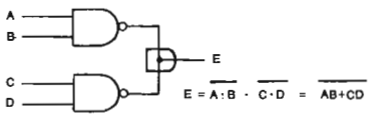
ELECTRICAL CHARACTERISTICS

SYMBOL	CHARACTERISTICS	LIMITS 0°C Min.	Max.	25°C Min.	Typ.	Max.	75°C Min.	Max.	Unit	CONDITIONS
V_{OH}	Output High Voltage	18.5		18.5	18		18.5		V	V_{CC} = 20V
		13.5		13.5	14		13.5		V	V_{CC} = 15V } I_{OH} = -50μA
		9.3		9.3	9.8		9.3		V	V_{CC} = 10.8V
										V_{IN} = V_{IL} (see below)
V_{OL}	Output Low Voltage		1.5		0.2	1.5		1.5	V	V_{CC} = 20V I_{OL} = 15mA or
										V_{CC} = 15V I_{OL} = 12mA or
										V_{CC} = 10.8V I_{OL} = 9mA
										V_{IN} = V_{IH} (see below)
V_{IL}	Input Low Voltage		6			6		6	V	Guaranteed Input Low Threshold for All Inputs
V_{IH}	Input High Voltage	8		8			8		V	Guaranteed Input High Threshold for All Inputs
I_F	Input Low Current		-0.6		-0.1	-0.6		-0.6	mA	V_{CC} = 20V
			-0.48		-0.08	-0.48		-0.48	mA	V_{CC} = 15V } V_F = 1.5V
			-0.36		-0.06	-0.36		-0.36	mA	V_{CC} = 10.8V
I_{FEX}	Expander Input Low Current (H 124 only)		-1.65		-1.25	-1.65		-1.65	mA	V_{CC} = 20V
			-1.33		-0.90	-1.33		-1.33	mA	V_{CC} = 15V } V_{FEX} = 2V
			-1		-0.75	-1		-1	mA	V_{CC} = 10.8V
I_R	Reverse Input Current		5		0.1	5		5	μA	V_{CC} = 20V V_R = 20V
I_{CEX}	Output Leakage Current		45			45		45	μA	V_{CC} = 20V V_{CEX} = 20V
I_{SC}	Output Short Circuit Current	-1.15	-2.5	-1.15	-2	-2.5	-1.15	-2.5	mA	V_{CC} = 20V Inputs and Output Grounded
I_{PDH}	High Level Power Dissipation Current (Each Gate)		7.5		6	7.5		7.5	mA	V_{CC} = 20V Inputs High
I_{PDL}	Low Level Power Dissipation Current (Each Gate)		2.5		1.5	2.5		2.5	mA	V_{CC} = 20V Inputs Low
TPD+	Turn-Off Delay				250	400			nS	V_{CC} = 15V } See Test Circuit
TPD-	Turn-On Delay				40	100			nS	V_{CC} = 15V }

NOTES: 1) The node can be expanded using diode EB 383 or BAY 72
2) For H 124 only

WIRED - OR CONNECTION

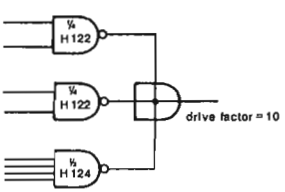
Outputs of H 122 and H 124 may be tied together for the wired - OR function.



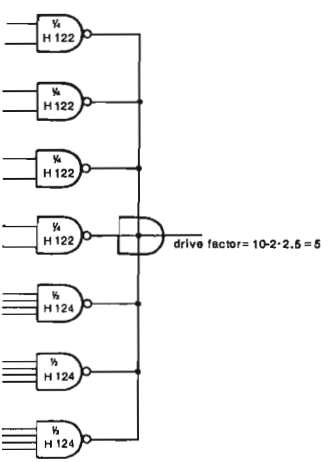
If 2, 3, 4, or 5 H 122 (or H 124) are OR-ed, the drive factor is 10.

For each additional gate over 5 a unit load of 2.5 should be subtracted from the drive factor of the gate.

EXAMPLE 1

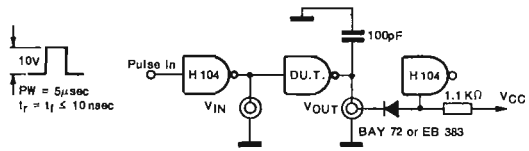


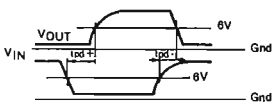
EXAMPLE 2

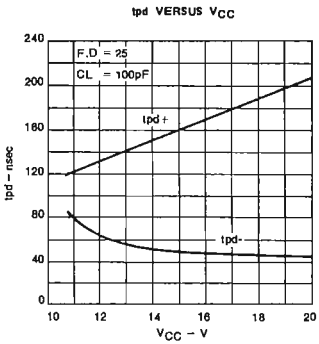


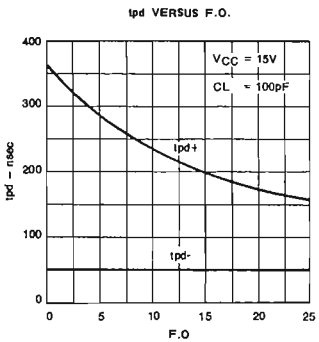
SWITCHING TIME TEST CIRCUITS

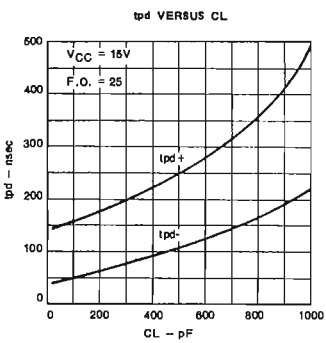
Gates H102-H103-H104



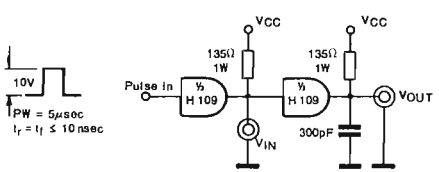


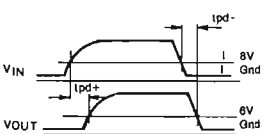


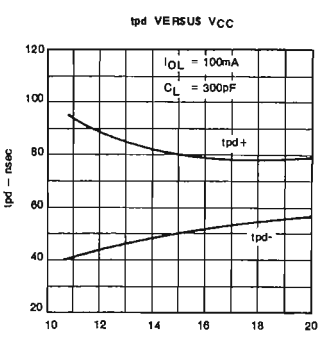


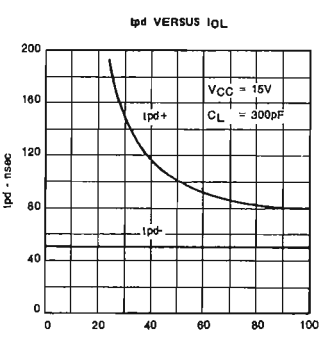


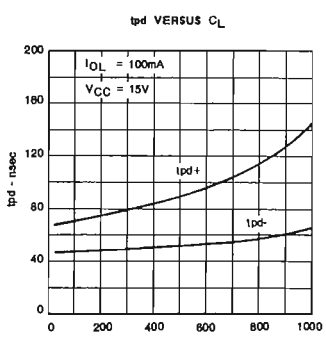
Power Gate H109



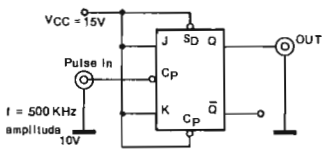


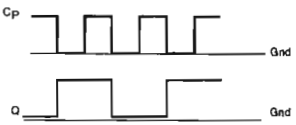




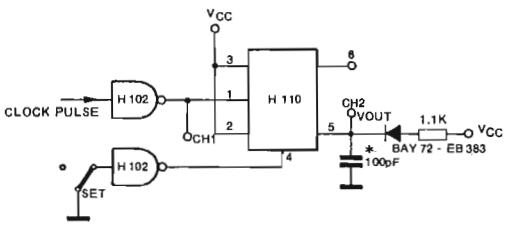


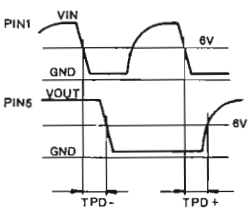
Dual J-K Flip-Flops H110-H111



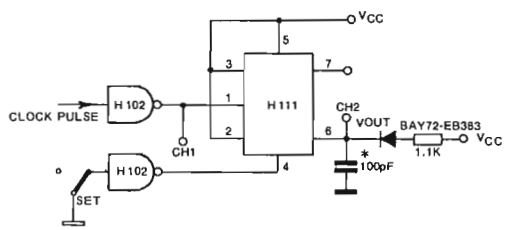


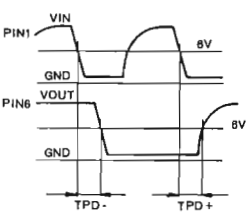
Dual J-K Flip-Flop H110

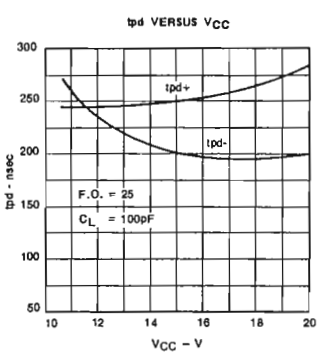


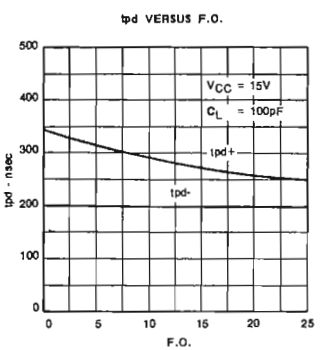


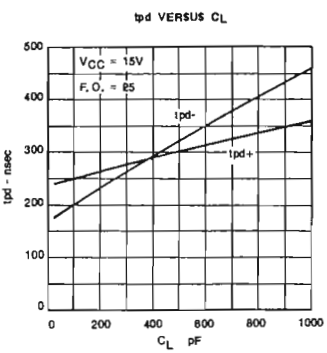
Dual J-K Flip-Flop H111





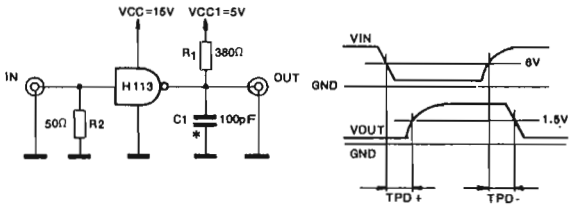


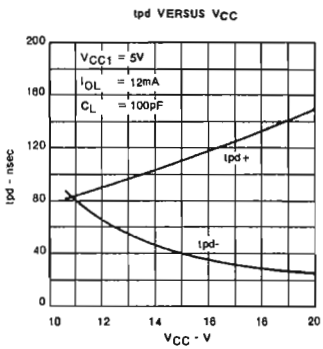


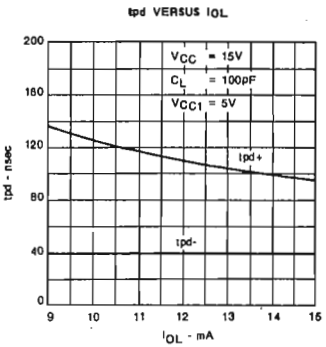


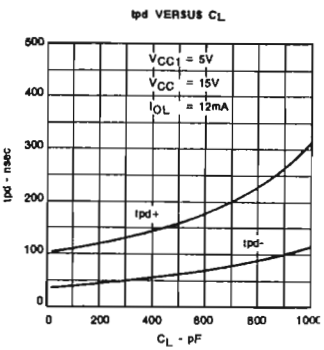
* The capacitance shall be within ± 5% including jig., probe and wiring capacitance.

High to Low Level Quad Converter H113

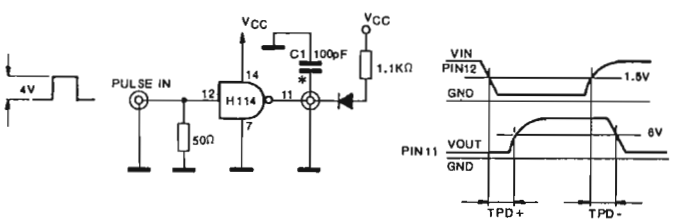


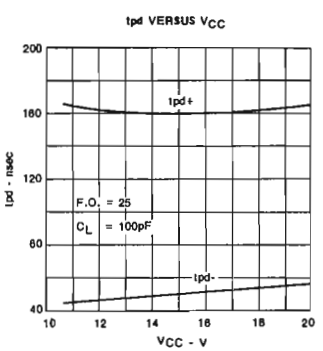


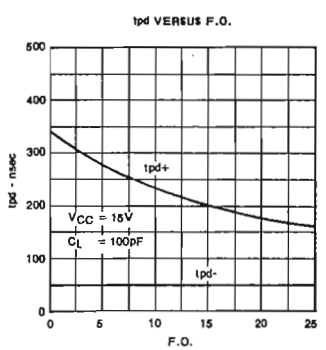


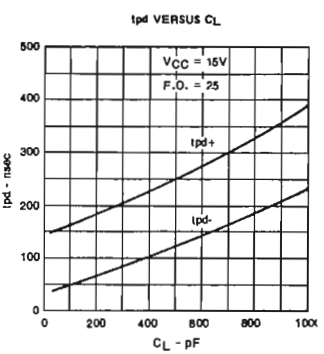


Low to High Level Quad Converter H114



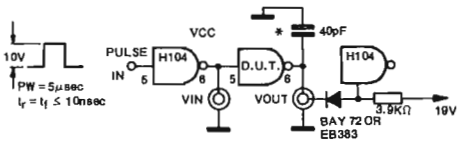


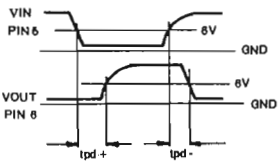




* The capacitance shall be within ± 5% including jig., probe and wiring capacitance.

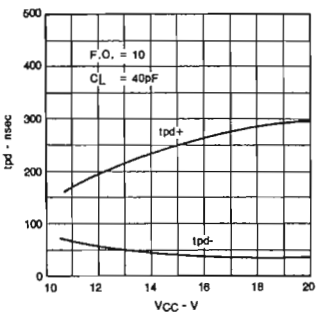
Gates With Passive Pull-Up H 122 - H 124



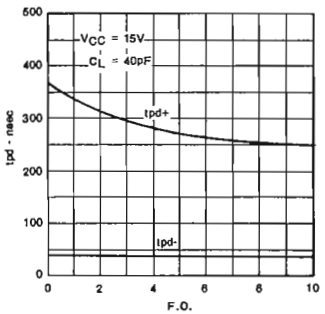


* The capacitance shall be within ± 5% including jig., probe and wiring capacitance.

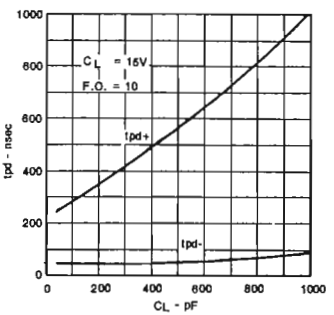
tpd VERSUS V_{CC}



tpd VERSUS F.O.

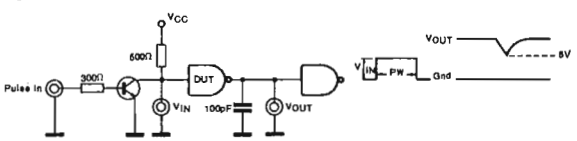


tpd VERSUS C_L

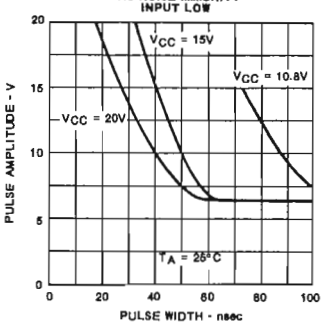


AC NOISE IMMUNITY TEST CIRCUIT

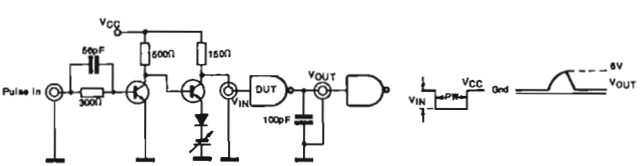
Input low



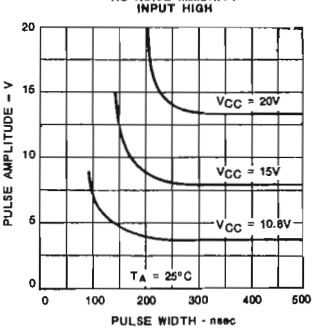
AC NOISE IMMUNITY INPUT LOW



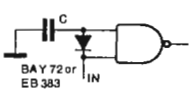
Input high



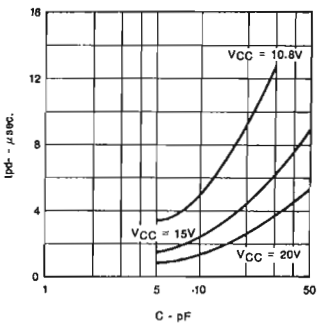
AC NOISE IMMUNITY INPUT HIGH

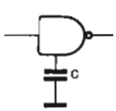


SLOW DOWN OF TPD -

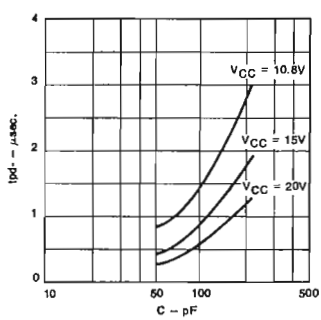


tpd- VERSUS CAPACITANCE





tpd- VERSUS CAPACITANCE



Expandable dual 2-wide 2-input AND-OR-INVERT gate

STANDARD TEMPERATURE RANGE
0° C to 75° C
INTERMEDIATE TEMPERATURE RANGE
-40° C to 85° C

The H 105 is a dual unit with each unit consisting of two-2 input AND gates (one with an input expander node available) that are internally ORed together into an inverting output configuration.
In accordance with the High Level Logic family characteristics, it offers the advantages of 5V DC noise immunity, high segnal levels, wide supply voltage tolerances and unusually low fan-in. These features make the H 105 particularly suitable for industrial, avionic and telephone applications where the high noise environment might prohibit the use of a low threshold integrated circuit.

- ACTIVE PULL-UP OUTPUT
- WIDE RANGE OF SUPPLY VOLTAGE
- HIGH DC NOISE IMMUNITY, 5V AT V_{CC} = 15V
- HIGH FAN-OUT 25 (WORST CASE)
- 14-PIN CERAMIC DIP

ABSOLUTE MAXIMUM RATINGS
(above which the useful life may be impaired)

Supply Voltage V_{CC}, continuous	H105 D1	22V
	H105 D6	18V
Input Voltage	H105 D1	-0.5V to 20V
	H105 D6	-0.5V to 16V
Storage Temperature Range		-65° C to 150° C

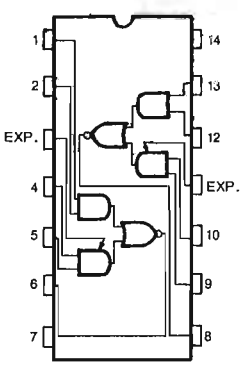
OPERATING CONDITIONS

Temperature Range	H105 D1	0° C to 75° C
	H105 D6	-40° C to 85° C
Supply Voltage	H105 D1	10.8V to 20V
	H105 D6	10.8V to 16V

ORDERING NUMBERS

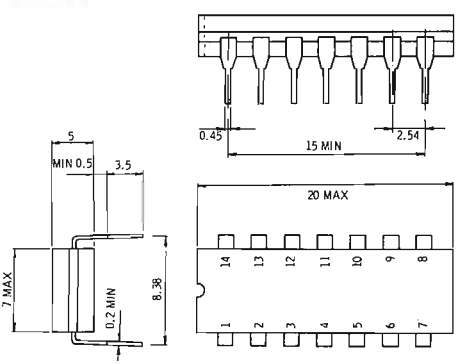
H105 D1 (Standard Temperature Range)
H105 D6 (Intermediate Temperature Range)

CONNECTION DIAGRAM



GND = PIN 7
V_{CC} = PIN 14

PHYSICAL DIMENSIONS
14 pin ceramic DIP



Note: all dimensions in mm.

FEBRUARY 1973 - Preliminary Information

ELECTRICAL CHARACTERISTICS (T_A = 0°C to 75°C, V_{CC} = 10.8 V to 20 V)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
V_{OH}	Output High Voltage	18.5 13.5 9.3	19 14 9.8		V V V	V_{CC} = 20 V I_{OH} = -200 μA V_{CC} = 15 V I_{OH} = -200 μA V_{CC} = 10.8 V I_{OH} = -200 μA V_{IN} = V_{IL} (see below)
V_{OL}	Output Low Voltage		1	1.5	V	V_{CC} = 20 V I_{OL} = 15 mA or V_{CC} = 15 V I_{OL} = 12 mA or V_{CC} = 10.8 V I_{OL} = 9 mA V_{IN} = V_{IH} (see below)
V_{IL}	Input Low Voltage			6	V	Guaranteed Input Low Threshold for All Inputs
V_{IH}	Input High Voltage	8			V	Guaranteed Input High Threshold for All Inputs
I_F	Input Low Current		-0.1 -0.08 -0.06	-0.6 -0.48 -0.36	mA mA mA	V_{CC} = 20 V V_{CC} = 15 V V_{CC} = 10.8 V } V_F = 1.5 V
I_{FEX}	Expander Input Low Current		-1.25 -0.90 -0.75	-1.65 -1.33 -1	mA mA mA	V_{CC} = 20 V V_{CC} = 15 V V_{CC} = 10.8 V } V_{FEX} = 2 V
I_R	Reverse Input Current		0.1	5	μA	V_{CC} = 20 V V_R = 20 V
I_{SC}	Output Short Circuit Current	-9	-15	-25	mA	V_{CC} = 20 V Inputs and Output Grounded
I_{PDH}	High Level Power Dissipation Current (Each Gate)		9.5	12.5	mA	V_{CC} = 20 V Inputs High
I_{PDL}	Low Level Power Diasipation Current (Each Gate)		3.0	5	mA	V_{CC} = 20 V Inputs Low
t_{pd1}	Turn-Off Delay		160		ns	V_{CC} = 15 V
t_{pd0}	Turn-On Delay		50		ns	

ELECTRICAL CHARACTERISTICS (T_A = -40°C to 85°C. V_{CC} = 10.8 V to 16 V)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
V_{OH}	Output High Voltage	14.5 9.3	15 9.8		V V	V_{CC} = 16 V I_{OH} = -200 μA V_{CC} = 10.8 V I_{OH} = -200 μA V_{IN} = V_{IL} (see below)
V_{OL}	Output Low Voltage		1	1.5	V	V_{CC} = 16 V I_{OL} = 12.5 mA V_{CC} = 10.8 V I_{OL} = 9 mA V_{IN} = V_{IH} (see below)
V_{IL}	Input Low Voltage			6	V	Guaranteed Input Low Threshold for All Inputs
V_{IH}	Input High Voltage	8			V	Guaranteed Input High Threshold for All Inputs
I_F	Input Low Current		-0.08 -0.06	-0.5 -0.36	mA mA	V_{CC} = 16 V V_{CC} = 10.8 V } V_F = 1.5 V
I_{FEX}	Expander Input Low Current		-0.9 -0.75	-1.4 -1	mA mA	V_{CC} = 16 V V_{CC} = 10.8 V } V_{FEX} = 2 V
I_R	Reverse Input Current		0.1	5	μA	V_{CC} = 16 V V_R = 16 V
I_{SC}	Output Short Circuit Current	-6.5	-13.5	-20	mA	V_{CC} = 16 V Inputs and Output Grounded
I_{PDH}	High Level Power Dissipation Current (Each Gate)		6.2	8.7	mA	V_{CC} = 16 V Inputs High
I_{PDL}	Low Level Power Dissipation Current (Each Gate)		2.8	4	mA	V_{CC} = 16 V Inputs Low
t_{pd1}	Turn-Off Delay		180		ns	V_{CC} = 15 V
t_{pd0}	Turn-On Delay		50		ns	

Hex inverter open collector output

STANDARD TEMPERATURE RANGE
0° C to 75° C
INTERMEDIATE TEMPERATURE RANGE
-40° C to 85° C

- OPEN COLLECTOR OUTPUT
- WIDE RANGE OF SUPPLY VOLTAGE
- HIGH DC NOISE IMMUNITY, 5V AT V_{CC} = 15V
- HIGH FAN–OUT 25 (WORST CASE)
- 14–PIN CERAMIC DIP

The H112 hex inverter is designed to drive low current lamps, interface with discrete components, and facilitate the implementation of the Wired Collector function with minimum power dissipation.
Belonging to the High Level Logic family, the high threshold family of integrated circuits, it offers the advantages of 5V DC noise immunity, high signal levels, wide supply voltage tolerance and unusually high fan-out. These features make the H112 particularly suitable for industrial, avionic and telephone applications, where the high noise environment might prohibit the use of a low threshold integrated circuit.

ABSOLUTE MAXIMUM RATINGS
(above which the useful life may be impaired)

Supply Voltage V_{CC}, continuous	H112D1	22V
	H112D6	18V
Input Voltage	H112D1	-0.5V to 20V
	H112D6	-0.5V to 16V
Storage Temperature Range		-65° C to 150° C

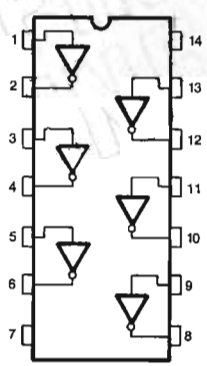
OPERATING CONDITIONS

Temperature Range	H112D1	0° C to 75° C
	H112D6	-40° C to 85° C
Supply Voltage	H112D1	10.8V to 20V
	H112D6	10.8V to 16V

ORDERING NUMBERS

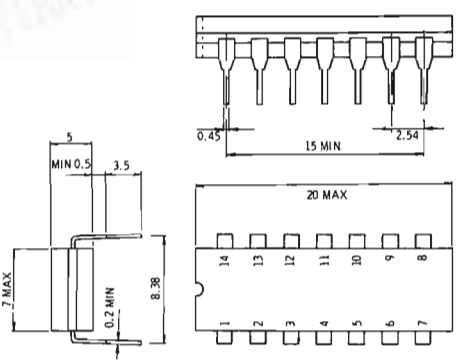
H112D1 (Standard Temperature Range)
H112D6 (Intermediate Temperature Range)

CONNECTION DIAGRAM



GND = PIN 7
V_{CC} = PIN 14

PHYSICAL DIMENSIONS
14 pin ceramic DIP



Note: all dimensions in mm.

ELECTRICAL CHARACTERISTICS (T_A = 0°C to 75°C, V_{CC} = 10.8 V to 20 V)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
V_{OL}	Output Low Voltage		0.2	1.5	V	V_{CC} = 20 V, I_{OL} = 15 mA or V_{CC} = 15 V, I_{OL} = 12 mA or V_{CC} = 10.8 V, I_{OL} = 9 mA; $V_{IN} = V_{IH}$ (see below)
V_{IL}	Input Low Voltage			6	V	Guaranteed Input Low Threshold for All Inputs
V_{IH}	Input High Voltage	8			V	Guaranteed Input High Threshold for All Inputs
I_F	Input Low Current		-0.1 -0.08 -0.06	-0.6 -0.48 -0.36	mA mA mA	V_{CC} = 20 V V_{CC} = 15 V V_{CC} = 10.8 V } V_F = 1.5 V
I_R	Reverse Input Current		0.1	5	μA	V_{CC} = 20 V, V_R = 20 V
I_{CEX}	Output Leakage Current			100	μA	V_{CC} = 20 V, V_{CEX} = 20 V
I_{PDH}	High Level Power Dissipation Current (Each Gate)		4.5	6	mA	V_{CC} = 20 V, Input High
I_{PDL}	Low Level Power Dissipation Current (Each Gate)		1.5	2.5	mA	V_{CC} = 20 V, Input Low
t_{pd1}	Turn-Off Delay		110		ns	} V_{CC} = 15 V
t_{pd0}	Turn-On Delay		40		ns	}

ELECTRICAL CHARACTERISTICS (T_A = -40°C to 85°C, V_{CC} = 10.8 V to 16 V)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
V_{OL}	Output Low Voltage		0.2	1.5	V	V_{CC} = 16 V, I_{OL} = 12.5 mA or V_{CC} = 10.8 V, I_{OL} = 9 mA; $V_{IN} = V_{IH}$ (see below)
V_{IL}	Input Low Voltage			6	V	Guaranteed Input Low Threshold for All Inputs
V_{IH}	Input High Voltage	8			V	Guaranteed Input High Threshold for All Inputs
I_F	Input Low Current		-0.08 -0.06	-0.5 -0.36	mA mA	V_{CC} = 16 V V_{CC} = 10.8 V } V_F = 1.5 V
I_R	Reverse Input Current		0.1	5	μA	V_{CC} = 16 V, V_R = 16 V
I_{CEX}	Output Leakage Current			80	μA	V_{CC} = 16 V, V_{CEX} = 16 V
I_{PDH}	High Level Power Dissipation Current (Each Gate)		3.5	5	mA	V_{CC} = 16 V, Input High
I_{PDL}	Low Level Power Dissipation Current (Each Gate)		1.2	2	mA	V_{CC} = 16 V, Input Low
t_{pd1}	Turn-Off Delay		110		ns	} V_{CC} = 15 V
t_{pd0}	Turn-On Delay		40		ns	}

Strobed hex inverter open collector output

STANDARD TEMPERATURE RANGE
0°C to 75°C
INTERMEDIATE TEMPERATURE RANGE
-40°C to 85°C

- OPEN COLLECTOR OUTPUT
- ENABLE AND STROBE INPUT
- WIDE RANGE OF SUPPLY VOLTAGE
- HIGH DC NOISE IMMUNITY, 5V AT V_{CC} = 15V
- HIGH FAN-OUT 25 (WORST CASE)
- 16–PIN CERAMIC DIP

The H115 hex inverter is designed to drive low-current lamps, interface with discrete components, and facilitate the implementation of the Wired Collector function with minimum power dissipation.
Belonging to the High Level Logic family, the high threshold family of integrated circuits, it offers the advantages of 5V DC noise immunity high signal levels, wide supply voltage tolerance and unusually high fan-out. These features make the H115 particularly suitable for industrial, avionic and telephone applications, where the high noise environment might prohibit the use of a low threshold integrated circuit.

ABSOLUTE MAXIMUM RATINGS
(above which the useful life may be impaired)

Supply Voltage V_{CC}, continuous	H115D1	22V
	H115D6	18V
Input Voltage	H115D1	-0.5V to 20V
	H115D6	-0.5V to 16V
Storage Temperature Range		-65°C to 150°C

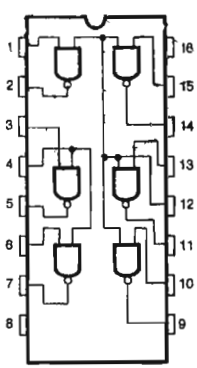
OPERATING CONDITIONS

Temperature Range	H115D1	0°C to 75°C
	H115D6	-40°C to 85°C
Supply Voltage	H115D1	10.8V to 20V
	H115D6	10.8V to 16V

ORDERING NUMBERS

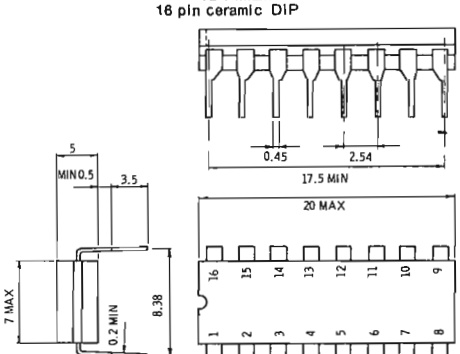
H115 D1 (Standard Temperature Range)
H115 D6 (Intermediate Temperature Range)

CONNECTION DIAGRAM



GND = PIN 8
V_{CC} = PIN 16

PHYSICAL DIMENSIONS
16 pin ceramic DIP



NOTE:
1) Board-drilling dimensions should equal your practice for a conventional 0.51 mm. diameter lead.
2) All dimensions in mm.

ELECTRICAL CHARACTERISTICS (T_A = 0°C to 75°C, V_{CC} = 10.8 V to 20 V)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
V_{OL}	Output Low Voltage		0.2	1.5	V	V_{CC} = 20 V, I_{OL} = 15 mA or V_{CC} = 15 V, I_{OL} = 12 mA or V_{CC} = 10.8 V, I_{OL} = 9 mA ; $V_{IN} = V_{IH}$ (see below)
V_{IL}	Input Low Voltage			6	V	Guaranteed Input Low Threshold for All Inputs
V_{IH}	Input High Voltage	8			V	Guaranteed Input High Thereshold for All Inputs
*I_F	Input Low Current		-0.1 -0.08 -0.06	-0.6 -0.48 -0.36	mA mA mA	V_{CC} = 20 V V_{CC} = 15 V V_{CC} = 10.8 V } V_F = 1.5 V
**I_R	Reverse Input Current		0.1	5	µA	V_{CC} = 20 V V_R = 20 V
I_{CEX}	Output Leakage Current			100	µA	V_{CC} = 20 V V_{CEX} = 20 V
I_{PDH}	High Level Power Dissipation Current (Each Gate)		4.5	6	mA	V_{CC} = 20 V Inputs High
I_{PDL}	Low Level Power Dissipation Current (Each Gate)		1.5	2.5	mA	V_{CC} = 20 V Inputs Low
t_{pd1}	Turn-Off Delay		110		ns	} V_{CC} = 15 V
t_{pd0}	Turn-On Delay		40		ns	

ELECTRICAL CHARACTERISTICS (T_A = -40°C to 85°C, V_{CC} = 10.8 V to 16 V)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
V_{OL}	Output Low Voltage		0.2	1.5	V	V_{CC} = 16 V, I_{OL} = 12.5 mA ; V_{CC} = 10.8 V, I_{OL} = 9 mA ; $V_{IN} = V_{IH}$ (see below)
V_{IL}	Input Low Voltage			6	V	Guaranteed Input Low Threshold for All Inputs
V_{IH}	Input High Voltage	8			V	Guaranteed Input High Threshold for All Inputs
*I_F	Input Low Current		-0.08 -0.06	-0.5 -0.36	mA mA	V_{CC} = 16 V V_{CC} = 10.8 V } V_F = 1.5 V
**I_R	Reverse Input Current		0.1	5	µA	V_{CC} = 16 V V_R = 16 V
I_{CEX}	Output Leakage Current			80	µA	V_{CC} = 16 V V_{CEX} = 16 V
I_{PDH}	High Level Power Dissipation Current (Each Gate)		3.5	5	mA	V_{CC} = 16 V Inputs High
I_{PDL}	Low Level Power Dissipation Current (Each Gate)		1.2	2	mA	V_{CC} = 16 V Inputs Low
t_{pd1}	Turn-Off Delay		110		ns	} V_{CC} = 15 V
t_{pd0}	Turn-On Delay		40		ns	

* Input Low Current : at pin 4 is equal to 2 · I_F; at pin 12 is equal to 4 · I_F
** Reverse Input Current : at pin 4 is equal to 2 · I_R; at pin 12 is equal to 4 · I_R

One-shot multivibrator

STANDARD TEMPERATURE RANGE,
0°C to 75°C
INTERMEDIATE TEMPERATURE RANGE,
- 40°C to 85°C

- MONOSTABLE AND ASTABLE FUNCTIONING
- VERY WIDE DURATION RANGE (FROM 1 μsec TO MORE THAN 100 sec.)
- OUTPUT PULSE WIDTH DEFINED ONLY BY EXTERNAL TIMING NETWORK
- PULSE TRIGGERING LARGELY INDEPENDENT OF THE INPUT PULSE WIDTH AND FORM
- EXTREMELY STABLE OPERATION WITH RESPECT TO POWER SUPPLY AND TEMPERATURE
- COMPLEMENTARY OUTPUTS
- POSSIBILITY OF DRIVING TTL AND DTL CIRCUITS
- WIDE RANGE OF SUPPLY VOLTAGE
- HIGH DC NOISE IMMUNITY, 5V AT V_{CC}=15V
- HIGH FAN-OUT, 25 MINIMUM
- 14-PIN CERAMIC DIP

ORDERING NUMBERS
H 117 D1 (Standard Temperature Range)
H 117 D6 (Intermediate Temperature Range)

The H 117 is a monostable multivibrator designed for a wide range of pulse duration, practically independent of variation in ambient temperature and power supply voltage. Belonging to the High Level Logic family, the high threshold family of integrated circuits, it offers the advantages of 5V DC ground and supply voltage noise immunity at V_{CC} = 15V, high signal levels, wide supply voltage tolerances and unusually high fan-out. These features make the family particularly suitable for industrial, avionic and telephone applications where the high noise environment might prohibit the use of a low threshold integrated circuit.

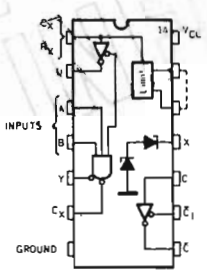
ABSOLUTE MAXIMUM RATINGS
(above which the useful life may be impaired)

Supply Voltage V_{CC}, continuous	
H 117 D1	22V
H 117 D6	18V
Input Voltage	
H 117 D1	- 0.5V to 20V
H 117 D6	- 0.5V to 16V
Storage Temperature Range	- 55°C to 150°C

OPERATING CONDITIONS

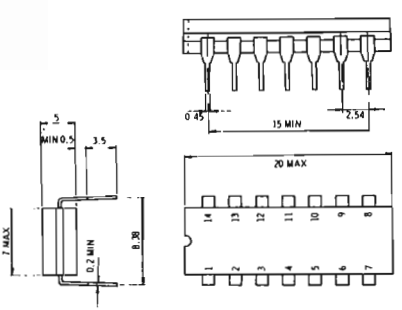
Temperature range	
H 117 D1	0°C to 75°C
H 117 D6	- 40°C to 85°C
Supply Voltage	
H 117 D1	10.8V to 20V
H 117 D6	10.8V to 16V

CONNECTION DIAGRAM
(Top view)



X = Pre-limiter connection

PHYSICAL DIMENSIONS
14-pin ceramic DIP



Note : all dimensions in mm.

ELECTRICAL CHARACTERISTICS (V_{CC} = 10.8V to 20V, T_A 0°C to 75°C)

SYMBOL	CHARACTERISTICS	Min.	Typ.	Max.	Unit	TEST CONDITIONS
V_{OH}	Output High Voltage	18.5	19		V	V_{CC} = 20V } I_{OH} = - 200 µA
		13.5	14		V	V_{CC} = 15V }
		9.3	9.8		V	V_{CC} = 10.8V }
V_{OL}	Output Low Voltage		1	1.5	V	V_{CC} = 20V I_{OL} = 15 mA or V_{CC} = 15V I_{OL} = 12 mA or V_{CC} = 10.8V I_{OL} = 9 mA
V_{IL}	Input Low Voltage			6	V	Guaranteed input low threshold at inputs A, B and C.
V_{IH}	Input High Voltage	8			V	Guaranteed input high threshold at inputs A, B and C.
I_F	Input Low Current		-0.1	-0.6	mA	V_{CC} = 20V } V_F = 1.5V at
			-0.08	-0.48	mA	V_{CC} = 15V } pins A, B and C.
			-0.06	-0.36	mA	V_{CC} = 10.8V }
I_R	Reverse Input Current		0.1	5	µA	V_{CC} = 20V V_R = 20V at pins A, B and C.
I_{SC}	Output Short Circuit Current	-9		-25	mA	V_{CC} = 20V at pins Q and $\overline{C}$.
I_{PD}	Power Dissipation Current		15	25	mA	V_{CC} = 20V all inputs high.

ELECTRICAL CHARACTERISTICS (V_{CC} = 10.8V to 16V, T_A = - 40°C to 85°C)

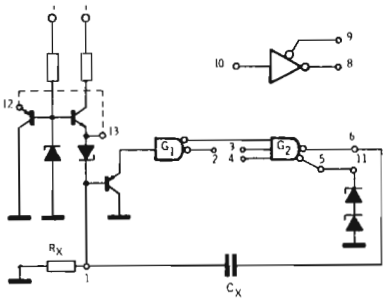
SYMBOL	CHARACTERISTICS	Min.	Typ.	Max.	Unit	TEST CONDITIONS
V_{OH}	Output High Voltage	14.5	15		V	V_{CC} = 16V } I_{OH} = - 200 µA
		9.3	9.8		V	V_{CC} = 10.8V }
V_{OL}	Output Low Voltage		1	1.5	V	V_{CC} = 16V I_{OL} = 12 mA or V_{CC} = 10.8V I_{OL} = 9 mA
V_{IL}	Input Low Voltage			6	V	Guaranteed input low threshold at inputs A, B and C.
V_{IH}	Input High Voltage	8			V	Guaranteed input high threshold at inputs A, B and C.
I_F	Input Low Current		-0.08	-0.5	mA	V_{CC} = 16V } V_F = 1,5V at
			-0.06	-0.36	mA	V_{CC} = 10.8V } pins A, B and C.
I_R	Reverse Input Current		0.1	5	µA	V_{CC} = 16V V_R = 16V at pins A, B and C.
I_{SC}	Output Short Circuit Current	-9		-25	mA	V_{CC} = 16V at pins Q and $\overline{C}$.
I_{PD}	Power Dissipation Current		15	25	mA	V_{CC} = 16V all inputs high.

DESCRIPTION

This monolithic HLL monostable multivibrator features DC triggering from gated negative going input. Both positive and negative going output pulses are provided, with the customary large HLL family fan-out. Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. Input pulses, with transition time as slow as 0.2 V/ms, allow jitter-free output. DC noise immunity, both V_{CC} and ground, as high as 5V at V_{CC} = 15V is guaranteed. Once fired the output is independent of further transition of the inputs and is a function only of the external timing components. Input pulses may be of any duration relative to the output pulse. Output pulse duration may vary from 1 µsec to more than 100 sec by choosing appropriate timing components. Output rise and fall times are independent of pulse length. Pulse width is virtually independent of V_{CC} (*1) and temperature (*2); in most applications pulse stability will only be determined by C_X and R_X stability. Jitter-free operation is maintained over the full temperature and V_{CC} range, for nearly six decades of timing capacitance and one decade of timing resistance. Throughout these ranges, pulse width is defined by the relationship $T_{PW} \simeq 0.83\ C_X\ R_X$. Duty cycles as high as 95 % are achieved when using R_X = 100 kΩ and C_X = 100 uF at V_{CC} = 15V.

*1) With a typical variation of 0.1% per Volt
*2) With a typical variation of 0.02% per °C for R_X 100k Ω and $C_X \geqslant 1000pF$.

LOGIC DIAGRAM

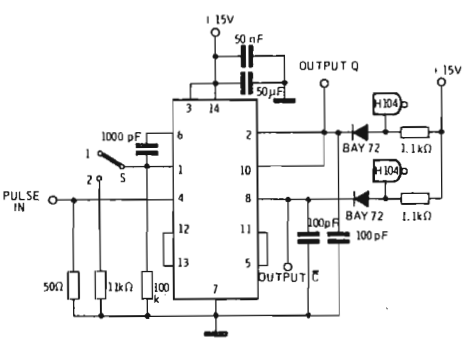


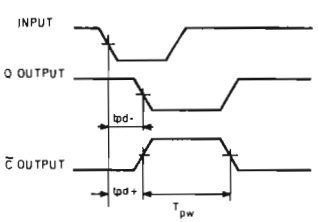
SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	CHARACTERISTICS	Min.	Typ.	Max.	Unit	TEST CONDITIONS
t_{pd+}	Turn-Off Delay Inputs 3 and 4 to Output 8		700	1000	ns	C_X = 1000pF R_X = 10kΩ V_{CC} = 15V
t_{pd-}	Turn-On Delay Inputs 3 and 4 to Output 2		500	800	ns	C_X = 1000pF R_X = 10kΩ V_{CC} = 15V
t_{PW}	Duration of Trigger Pulse	1			µs	C_X = 1000pF R_X = 10 kΩ
R_X	Maximum Timing Resistance	100			kΩ	
C_X	Timing Capacitance					No limit if trigger pulse is shorter than output pulse. Otherwise $C_X \leqslant 200$ µF.
T_{PW}	Output Pulse Width (See note)	75	83	91	µs	C_X = 1000pF R_X = 100 kΩ

Note : Output pulse width calculation : $T_{PW} \simeq 0.83\ R_X\ C_X$

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

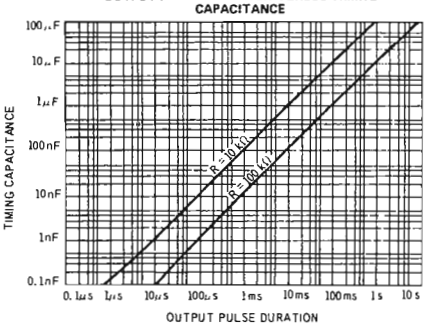




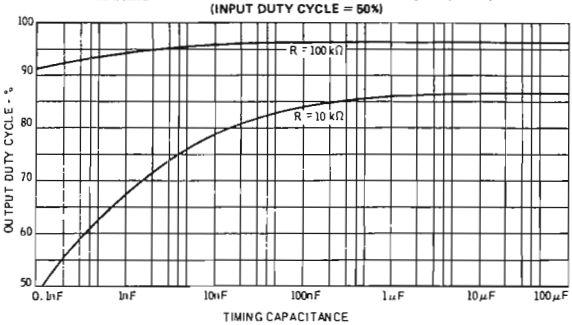
NOTES :
1) When testing t_{pd} switch S must be in position 2.
2) When testing T_{pw} switch S must be in position 1.

TYPICAL ELECTRICAL CHARACTERISTICS (V_{CC} = 15V, T_A = 25°C unless otherwise noted)

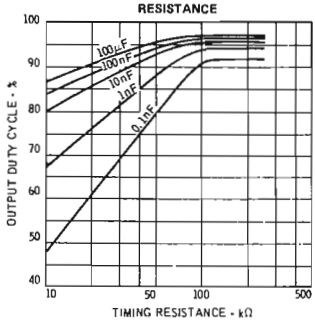
OUTPUT PULSE DURATION VERSUS TIMING CAPACITANCE



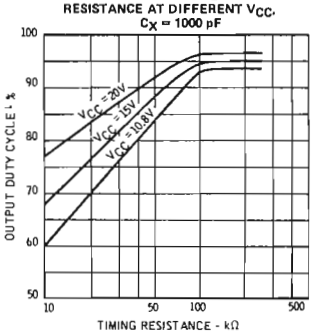
MAXIMUM OUTPUT DUTY CYCLE VERSUS TIMING CAPACITANCE (INPUT DUTY CYCLE = 50%)



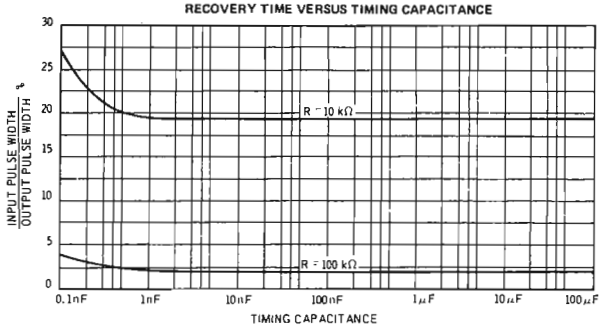
OUTPUT DUTY CYCLE VERSUS TIMING RESISTANCE



OUTPUT DUTY CYCLE VERSUS TIMING RESISTANCE AT DIFFERENT V_{CC}. C_X = 1000 pF

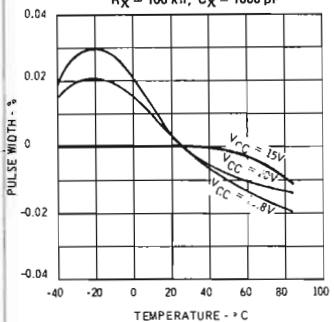


RECOVERY TIME VERSUS TIMING CAPACITANCE

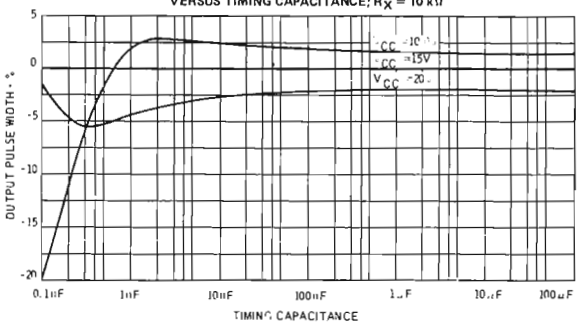


TYPICAL ELECTRICAL CHARACTERISTICS (V_{CC} = 15V, T_A =25°C unless otherwise noted)

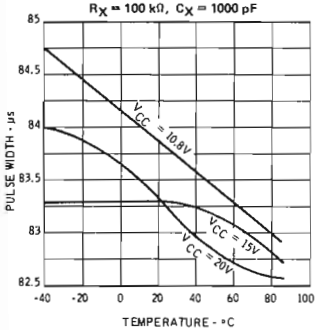
PULSE STABILITY VERSUS TEMPERATURE
R_X = 100 kΩ, C_X = 1000 pF



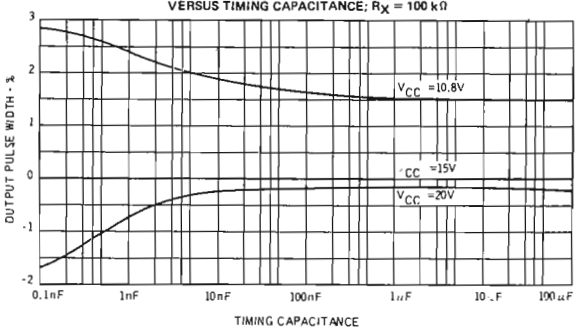
OUTPUT PULSE WIDTH VARIATION AT EXTREMES V_{CC} (PERCENTAGE) VERSUS TIMING CAPACITANCE; R_X = 10 kΩ



PULSE WIDTH VERSUS TEMPERATURE
R_X = 100 kΩ, C_X = 1000 pF



OUTPUT PULSE WIDTH VARIATION AT EXTREMES V_{CC} (PERCENTAGE), VERSUS TIMING CAPACITANCE; R_X = 100 kΩ

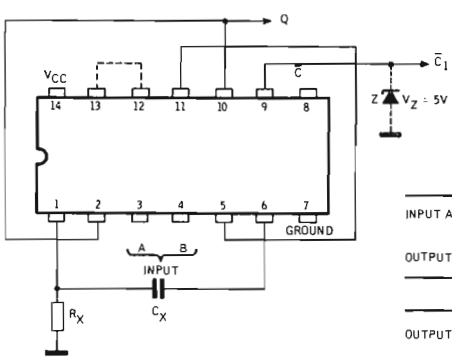


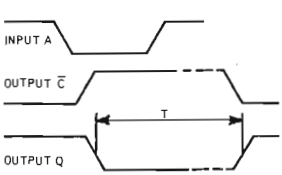
APPLICATIONS

MONOSTABLE MULTIVIBRATOR TRIGGERING ON PULSE TRAILING EDGE, COMPLEMENTARY OUTPUTS

t_n input		t_{n+1} input		Output	
A	B	A	B	Q	$\overline{C}$
1	1	0	1	one shot	
1	0	0	0	inhibit	
1	1	1	0	one shot	
0	1	0	0	inhibit	

t_n = time before input transition
t_{n+1} = time after input transition



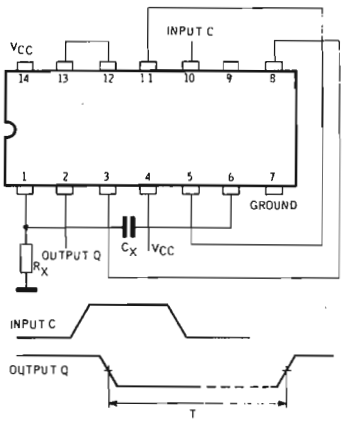


NOTES :

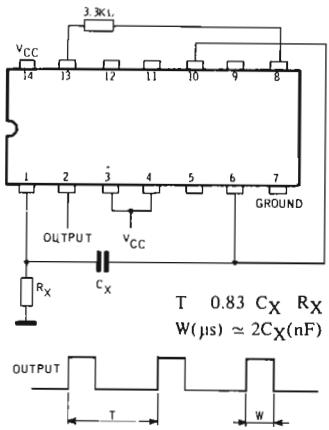
1) If pin 5 is connected to pin 11 and pin 12 is connected to pin 13, T = 0.83 C_X R_X at V_{CC} = 10.8V to 20V. If pins 5, 11, 12, 13 are not connected, T = 1.2 R_X C_X at V_{CC} = 16V to 20V.
2) If diode Z is connected, $\overline{C}_1$ may drive TTL or DTL circuits.

APPLICATIONS (Contd.)

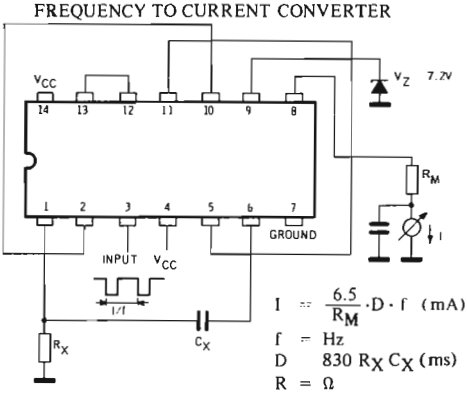
MONOSTABLE MULTIVIBRATOR
TRIGGERING ON PULSE LEADING EDGE



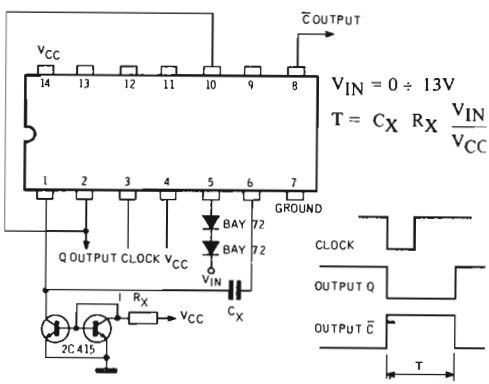
HIGH STABILITY CLOCK



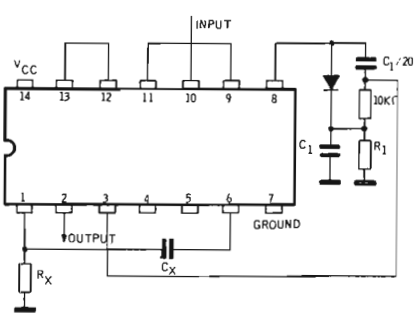
FREQUENCY TO CURRENT CONVERTER

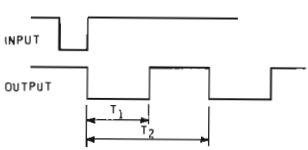


VOLTAGE TO PULSE WIDTH CONVERTER



DOUBLE PULSE GENERATOR





VCC = 14.5 to 17V
T1 = 0.83 RX CX
T2 = 0.55 R1 C1

Hex inverter active pull-up output

STANDARD TEMPERATURE RANGE
0°C to 75°C
INTERMEDIATE TEMPERATURE RANGE
-40°C to 85°C

- ACTIVE PULL-UP OUTPUT
- WIDE RANGE OF SUPPLY VOLTAGE
- HIGH DC NOISE IMMUNITY, 5V AT V_{CC} = 15V
- HIGH FAN-OUT 25 (WORST CASE)
- 14-PIN CERAMIC DIP

ORDERING NUMBERS

H118 D1 (Standard Temperature Range)
H118 D6 (Intermediate Temperature Range)

The H 118 hex inverter performs the function $B=\overline{A}$ and utilizes an active pull-up to minimize output impendance. Belonging to the High Level Logic family, the high threshold family of integrated circuits, it offers the advantages of 5V DC noise immunity, high signal levels, wide supply voltage tolerance and unusually high fan-out. These features make the H 118 particularly suitable for industrial, avionic and telephone applications, where the high noise environment might prohibit the use of a low threshold integrated circuit.

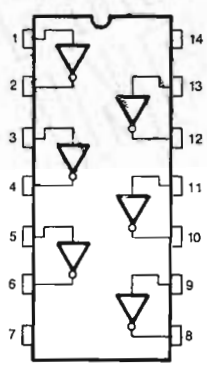
ABSOLUTE MAXIMUM RATINGS
(above which the usefull life may be impaired)

Supply Voltage V_{CC}, continuous	H118 D1	22V
	H118 D6	18V
Input Voltage	H118 D1	-0.5V to 20V
	H118 D6	-0.5V to 16V
Storage Temperature Range		-65°C to 150°C

OPERATING CONDITIONS

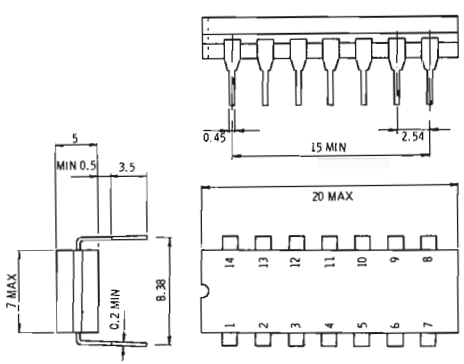
Temperature Range	H118 D1	0°C to 75°C
	H118 D6	-40°C to 85°C
Supply Voltage	H118 D1	10.8V to 20V
	H118 D6	10.8V to 16V

CONNECTION DIAGRAM



GND = PIN 7
V_{CC} = PIN 14

PHYSICAL DIMENSIONS
14 pin ceramic DIP



Note: all dimensions in mm.

ELECTRICAL CHARACTERISTICS (T_A = 0°C to 75° C, V_{CC} = 10.8 to 20 V)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
V_{OH}	Output High Voltage	18.5 13.5 9.3	19 14 9.8		V V V	V_{CC} = 20 V I_{OH} = -200 μA V_{CC} = 15 V I_{OH} = -200 μA V_{CC} = 10.8 V I_{OH} = -200 μA V_{IN} = V_{IL} (see below)
V_{OL}	Output Low Voltage		1	1.5	V	V_{CC} = 20 V I_{OL} = 15 mA or V_{CC} = 15 V I_{OL} = 12 mA or V_{CC} = 10.8 V I_{OL} = 9 mA V_{IN} = V_{IH} (see below)
V_{IL}	Input Low Voltage			6	V	Guaranteed Input Low Threshold for All Inputs
V_{IH}	Input High Voltage	8			V	Guaranteed Input High Threshold for All Inputs
I_F	Input Low Current		-0.1 -0.08 -0.06	-0.6 -0.48 -0.36	mA mA mA	V_{CC} = 20 V V_{CC} = 15 V V_{CC} = 10.8 V } V_F = 1.5 V
I_R	Reverse Input Current		0.1	5	μA	V_{CC} = 20 V V_R = 20 V
I_{SC}	Output Short Circuit Current	-9	-15	-25	mA	V_{CC} = 20 V Input and Output Grounded
I_{PDH}	High Level Power Dissipation Current (Each Gate)		6	7.5	mA	V_{CC} = 20 V Input High
I_{PDL}	Low Level Power Dissipation		1.5	2.5	mA	V_{CC} = 20 V Input Low
t_{pd1}	Turn-Off Delay		160		ns	} V_{CC} = 15 V
t_{pd0}	Turn-On Delay		50		ns	}

ELECTRICAL CHARACTERISTIC (T_A = -40°C to 85°C, V_{CC} = 10.8 to 16 V)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
V_{OH}	Output High Voltage	14.5 9.3	15 9.8		V V	V_{CC} = 16 V I_{OH} = -200 μA V_{CC} = 10.8 V I_{OH} = -200 μA V_{IN} = V_{IL} (see below)
V_{OL}	Output Low Voltage		1	1.5	V	V_{CC} = 16 V I_{OL} = 12.5 mA V_{CC} = 10.8 V I_{OL} = 9 mA V_{IN} = V_{IH} (see below)
V_{IL}	Input Low Voltage			6	V	Guaranteed Input Low Threshold for All Inputs
V_{IH}	Input High Voltage	8			V	Guaranteed Input High Threshold for All Inputs
I_F	Input Low Current		-0.08 -0.06	-0.5 -0.36	mA mA	V_{CC} = 16 V V_{CC} = 10.8 V } V_F = 1.5 V
I_R	Reverse Input Current		0.1	5	μA	V_{CC} = 16 V V_R = 16 V
I_{SC}	Output Short Circuit Current	-6.5	-13.5	-20	mA	V_{CC} = 16 V Input and Output Grounded
I_{PDH}	High Level Power Dissipation Current (Each Gate)		4.4	6	mA	V_{CC} = 16 V Input High
I_{PDL}	Low Level Power Dissipation Current (Each Gate)		1.2	2	mA	V_{CC} = 16 V Input Low
t_{pd1}	Turn-Off Delay		160		ns	} V_{CC} = 15 V
t_{pd0}	Turn-On Delay		50		ns	}

Strobed hex inverter active pull-up output

STANDARD TEMPERATURE RANGE
0°C to 75°C
INTERMEDIATE TEMPERATURE RANGE
-40°C to 85°C

- ACTIVE PULL-UP OUTPUT
- ENABLE AND STROBE INPUT
- WIDE RANGE OF SUPPLY VOLTAGE
- HIGH DC NOISE IMMUNITY, 5V AT V_{CC} = 15V
- HIGH FAN-OUT 25 (WORST CASE)
- 16-PIN CERAMIC DIP

The H 119 hex inverter can replace 1-1/2 quad two - input NAND gate packages in several applications through use of the enable or strobe inputs. The device consist of six two-input NAND gates with one input common to four gates and another common to two gates. Active Pull-up are utilize to minimize output impendance.
Belonging to the High Level Logic family, the high threshold family of integrated circuits, it offers the advantages of 5V DC noise immunity, high signal levels, wide supply voltage tolerance and unusually high fan-out. These features make the H 119 particularly suitable for industrial, avionic and telephone applications, where the high noise environment might prohibit the use of a low threshold integrated circuit.

ABSOLUTE MAXIMUM RATINGS
(above which the useful life may be impaired)

Supply Voltage V_{CC}, continuous	H119 D1	22V
	H119 D6	18V
Input Voltage	H119 D1	-0.5V to 20V
	H119 D6	-0.5V to 16V
Storage Temperature Range		-65°C to 150°C

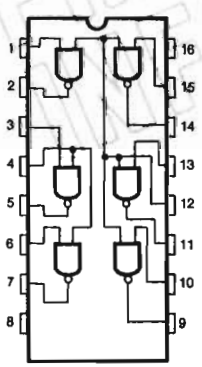
OPERATING CONDITIONS

Temperature Range	H119 D1	0°C to 75°C
	H119 D6	-40°C to 85°C
Supply Voltage	H119 D1	10.8V to 20V
	H119 D6	10.8V to 16V

ORDERING NUMBERS

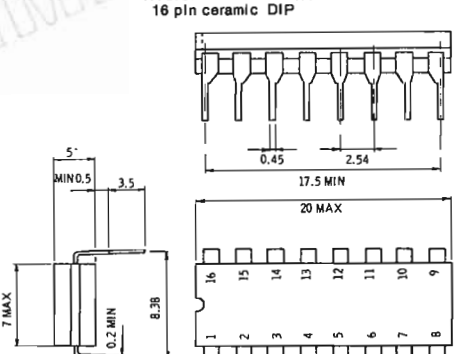
H119 D1 (Standard Temperature Range)
H119 D6 (Intermediate Temperature Range)

CONNECTION DIAGRAM



GND = PIN 8
V_{CC} = PIN 16

PHYSICAL DIMENSIONS
16 pin ceramic DIP



NOTE:
1) Board-drilling dimensions should equal your practice for a conventional 0.61 mm. diameter lead.
2) All dimensions in mm.

ELECTRICAL CHARACTERISTICS (T_A = 0°C to 75°C, V_{CC} = 10.8 V to 20 V)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
V_{OH}	Output High Voltage	18.5 13.5 9.3	19 14 9.8		V V V	V_{CC} = 20 V I_{OH} = -200 μA V_{CC} = 15 V I_{OH} = -200 μA V_{CC} = 10.8 V I_{OH} = -200 μA V_{IN} = V_{IL} (see below)
V_{OL}	Output Low Voltage		1	1.5	V	V_{CC} = 20 V I_{OL} = 15 mA or V_{CC} = 15 V I_{OL} = 12 mA or V_{CC} = 10.8 V I_{OL} = 9 mA V_{IN} = V_{IH} (see below)
V_{IL}	Input Low Voltage			6	V	Guaranteed Input Low Threshold for All Inputs
V_{IH}	Input High Voltage	8			V	Guaranteed Input High Threshold for All Inputs
*I_F	Input Low Current		-0.1 -0.08 -0.06	-0.6 -0.48 -0.36	mA mA mA	V_{CC} = 20 V V_{CC} = 15 V V_{CC} = 10.8 V } V_F = 1.5 V
**I_R	Reverse Input Current		0.1	5	μA	V_{CC} = 20 V V_R = 20 V
I_{SC}	Output Short Circuit Current	-9	- 15	- 25	mA	V_{CC} = 20 V Inputs and Outputs Grounded
I_{PDH}	High Level Power Dissipation Current (Each Gate)		6	7.5	mA	V_{CC} = 20 V Inputs High
I_{PDL}	Low Level Power Dissipation Current (Each Gate)		1.5	2.5	mA	V_{CC} = 20 V Inputs Low
t_{pd1}	Turn-Off Delay		160		ns	} V_{CC} = 15 V
t_{pd0}	Turn-On Delay		50		ns	}

ELECTRICAL CHARACTERISTICS (T_A = -40° C to 85°C, V_{CC} = 10.8 V to 16)V)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
V_{OH}	Output High Voltage	14.5 9.3	15 9.8		V V	V_{CC} = 16 V I_{OH} = -200 μA V_{CC} = 10.8 V I_{OH} = -200 μA V_{IN} = V_{IL} (see below)
V_{OL}	Output Low Voltage		1	1.5	V	V_{CC} = 16 V I_{OL} = 12.5 mA V_{CC} = 10.8 V I_{OL} = 9 mA VIN = VIH (see below)
VIL	Input Low Voltage			6	V	Guaranteed Input Low Threshold for All Inputs
V_{IH}	Input High Voltage	8			V	Guaranteed Input High Threshold for All Inputs
*I_F	Input Low Current		-0.08 -0.06	-0.5 -0.36	mA mA	V_{CC} = 16 V V_{CC} = 10.8 V } V_F = 1.5 V
**I_R	Reverse Input Current		0.1	5	μA	V_{CC} = 16 V V_R = 16 V
I_{SC}	Output Short Circuit Current	-6.6	-13.5	-20	mA	V_{CC} = 16 V Inputs and Output Grounded
I_{PDH}	High Level Power Dissipation Current (Each Gate)		4.4	6	mA	V_{CC} = 16 V Inputs High
I_{PDL}	Low Level Power Dissipation Current (Each Gate)		1.2	2	mA	V_{CC} = 16 V Inputs Low
t_{pd1}	Turn-Off Delay		160		ns	} V_{CC} = 15 V
t_{pd0}	Turn-On Delay		50		ns	}

* Input Low Current : at pin 4 is equal to 2 · I_F; at pin 12 is equal to 4 · I_F
** Reverse Input Current : at pin 4 is equal to 2 · I_R; at pin 12 is equal to 4 · I_R

Binary counter

STANDARD TEMPERATURE RANGE
0°C to 75°C
INTERMEDIATE TEMPERATURE RANGE
-40°C to 85°C

- SYNCHRONOUS COUNTING
- ASYNCHRONOUS PRESET
- ASYNCHRONOUS RESET
- WIDE RANGE OF SUPPLY VOLTAGE
- HIGH DC NOISE IMMUNITY, 5V AT V_{CC}=15V
- HIGH FAN-OUT 25 (WORST CASE)
- 14-PIN CERAMIC DIP

ORDERING NUMBERS

H 156 D1 (Standard Temperature Range)
H 156 D6 (Intermediate Temperature Range)

The H 156 is a synchronous binary counter. It is an asynchronously presettable, multifunctional building block usable in a large number of counting applications.
Belonging to the High Level Logic family, the high threshold family of integrated circuits, it offers the advantages of 5V DC noise immunity, high signal levels, wide supply voltage tolerance and unusually high fan-out. These features make the H 156 particularly suitable for industrial, avionic and telephone applications, where the high noise environment might prohibit the use of a low threshold integrated circuit.

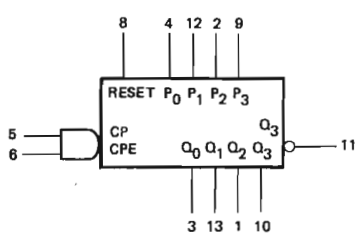
ABSOLUTE MAXIMUM RATINGS
(above which the useful life may be impaired)

Supply Voltage V_{CC}, continuous	
H 156 D1	22V
H 156 D6	18V
Input Voltage	
H 156 D1	-0.5V to 20V
H 156 D6	-0.5V to 16V
Storage Temperature Range	-65°C to 150°C

OPERATING CONDITIONS

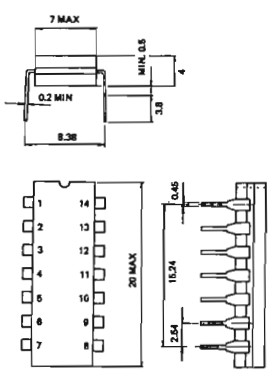
Temperature Range	
H 156 D1	0°C to 75°C
H 156 D6	-40°C to 85°C
Supply Voltage	
H 156 D1	10.8V to 20V
H 156 D6	10.8V to 16V

CONNECTION DIAGRAM



GND = PIN 7
V_{CC} = PIN 14

PHYSICAL DIMENSIONS
14 pin ceramic DIP



Note: all dimensions in mm.

ELECTRICAL CHARACTERISTICS (V_{CC}=10.8V to 20V, T_A= 0°C to 75°C)

SYMBOL	CHARACTERISTIC	MIN.	TYP	MAX.	UNIT	TEST CONDITIONS
V_{OH}	Output High Voltage	18.5	19		V	V_{CC} = 20V I_{OH} = - 200 μA
		13.5	14		V	V_{CC} = 15V I_{OH} = - 200 μA
		9.3	9.8		V	V_{CC} = 10.8V I_{OH} = - 200 μA
						V_{IN} (async.) = V_{IL} (see below)
V_{OL}	Output Low Voltage		I	1.5	V	V_{CC} = 20V I_{OL} = 15mA or
						V_{CC} = 15V I_{OL} = 12mA or
						V_{CC} = 10.8V I_{OL} = 9mA
						$V_{IN}(P_0,P_1,P_2,P_3) = V_{IH}$; $V_{IN(R)} = V_{IL}$
V_{IL}	Input Low Voltage			6	V	Guaranteed input low threshold for all inputs
V_{IH}	Input High Voltage	8			V	Guaranteed input high threshold for all inputs
I_F	Input Low Current		-0.15	-0.8	mA	V_{CC} = 20V V_F = 1.5V
	P_0, P_1, P_2, P_3 Inputs		-0.1	-0.64	mA	V_{CC} = 15V V_F = 1.5V
			-0.05	-0.48	mA	V_{CC} = 10.8V V_F = 1.5V
						Reset input grounded
	Reset Input		-0.6	-3.2	mA	V_{CC} = 20V V_F = 1.5V
			-0.4	-2.56	mA	V_{CC} = 15V V_F = 1.5V
			-0.2	-1.92	mA	V_{CC} = 10.8V V_F = 1.5V
						Preset inputs grounded
I_{FCP}	Input Low Current Clock		-0.1	-0.6	mA	V_{CC} = 20V V_F = 1.5V
	Inputs		-0.07	-0.48	mA	V_{CC} = 15V V_F = 1.5V
			-0.04	-0.36	mA	V_{CC} = 10.8V V_F = 1.5V
						V_{CC} on the clock input not under test
I_R	Reverse Input Current					
	P_0, P_1, P_2, P_3, Inputs		1	5	μA	V_{CC} = 20V V_R = 20V
						V_{CC} on reset and clock inputs
	Reset Input		5	20	μA	V_{CC} = 20V V_R = 20V
						V_{CC} on preset and clock inputs
I_{RCP}	Reverse Input Current Clock Inputs		1	5	μA	V_{CC} = 20V V_R = 20V
						Ground on the clock input not under test
I_{SC}	Output Short Circuit Current	-9	-16	-25	mA	V_{CC} = 20V
						Output and proper asynchronous inputs grounded
I_{PD}	Power Dissipation Current		28	36	mA	V_{CC} = 20V
						Reset grounded

ELECTRICAL CHARACTERISTICS (V_{CC}=10.8V to 16V, T_A= - 40°C to 85°C)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
V_{OH}	Output High Voltage	14.5	15		V	V_{CC} = 16V I_{OH} = - 200μA
		9.3	9.8		V	V_{CC} = 10.8V I_{OH} = - 200μA
						V_{IN} (async.) = V_{IL} (see below)
V_{OL}	Output Low Voltage		1	1.5	V	V_{CC} = 16V I_{OL} = 12.5mA or
						V_{CC} = 10.8V I_{OL} = 9mA
						$V_{IN(P_0,P_1,P_2,P_3)}$=V_{IH};$V_{IN(R)}$=V_{IL}
V_{IL}	Input Low Voltage			6	V	Guaranteed input low threshold for all inputs
V_{IH}	Input High Voltage	8			V	Guaranteed input high threshold for all inputs
I_F	Input Low Current					
	P_0, P_1, P_2, P_3 Inputs		-0.1	-0.7	mA	V_{CC} = 16V V_F = 1.5V
			-0.05	-0.48	mA	V_{CC} = 10.8V V_F = 1.5V
						Reset input grounded
	Reset Input		-0.4	-2.8	mA	V_{CC} = 16V V_F = 1.5V
			-0.2	-1.92	mA	V_{CC} = 10.8V V_F = 1.5V
						Preset inputs grounded
I_{FCP}	Input Low Current Clock		-0.07	-0.5	mA	V_{CC} = 16V V_F = 1.5V
	Inputs		-0.04	-0.36	mA	V_{CC} = 10.8V V_F = 1.5V
						V_{CC} on the clock input not under test
I_R	Reverse Input Current					
	P_0, P_1, P_2, P_3 Inputs		1	5	μA	V_{CC} = 16V V_R = 16V
						V_{CC} on reset and clock inputs
	Reset Input		5	20	μA	V_{CC} = 16V V_R = 16V
						V_{CC} on preset and clock inputs
I_{RCP}	Reverse Input Current Clock		1	5	μA	V_{CC} = 16V V_R = 16V
	Inputs					Ground on the clock input not under test
I_{SC}	Output Short Circuit Current	-6.5	-13.5	-20	mA	V_{CC} = 16V
						Output and proper asynchronous inputs grounded
I_{PD}	Power Dissipation Current		20	29	mA	V_{CC} = 16V
						Reset grounded

GENERAL DESCRIPTION

A clock buffer drives the four JK master slave flip-flops in parallel, so that synchronous operation is obtained. The information contained in the master is transferred to the slave flip-flops during the clock pulse high-to-low transition; the information contained in the slaves is available on their outputs Q_0, Q_1, Q_2 and Q_3.

Four asynchronous preset (P) inputs are provided, allowing the counter to be positioned to any counting number from 0 to 15. In order to preset the counter the following operations are necessary:

1) Disable the counter by applying a low level to CPE input;
2) Reset the counter by applying a low level to Reset input;
3) Insert in the counter the desired output configuration by applying to Preset inputs the levels shown in the Preset Count truth table (for example: if the desired preset is the count position 7, required preset inputs are $P_0=P_1=P_2=L$ $P_3=H$);
4) Apply a high level to Reset input;
5) Apply high levels to Preset inputs;
6) Enable the counter by applying a high level to CPE input; at this point of the example outputs are: $Q_0=Q_1=Q_2=H$, $Q_3=L$; that is a count of 7. The next CP high-to-low transition sets the counter on $Q_0=Q_1=Q_2=L$, $Q_3=H$; that is the count position 8.

Counter disabling by low level on CPE, operation N°1, is not strictly required: it is recommended in order to avoid spike generation on the first stage due to CP transition during reset operations.

From the above it can be seen that zero reset during count sequence, when P inputs are already high, can be accomplished by the simplified operation sequence:

1) CPE H to L
2) Reset H to L
4) Reset L to H
6) CPE L to H

TRUTH TABLES

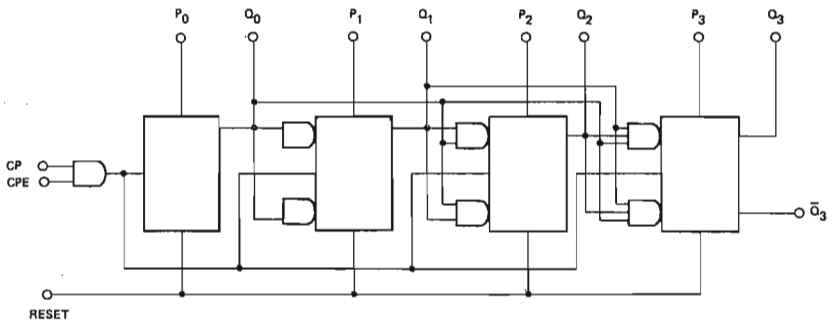
COUNT SEQUENCE (see note)				
OUTPUTS				COUNT
Q0	Q1	Q2	Q3	
L	L	L	L	0
H	L	L	L	1
L	H	L	L	2
H	H	L	L	3
L	L	H	L	4
H	L	H	L	5
L	H	H	L	6
H	H	H	L	7
L	L	L	H	8
H	L	L	H	9
L	H	L	H	10
H	H	L	H	11
L	L	H	H	12
H	L	H	H	13
L	H	H	H	14
H	H	H	H	15
L	L	L	L	0

PRESET COUNT								
INPUTS				OUTPUTS				COUNT
P0	P1	P2	P3	Q0	Q1	Q2	Q3	
H	H	H	H	L	L	L	L	0
L	H	H	H	H	L	L	L	1
H	L	H	H	L	H	L	L	2
L	L	H	H	H	H	L	L	3
H	H	L	H	L	L	H	L	4
L	H	L	H	H	L	H	L	5
H	L	L	H	L	H	H	L	6
L	L	L	H	H	H	H	L	7
H	H	H	L	L	L	L	H	8
L	H	H	L	H	L	L	H	9
H	L	H	L	L	H	L	H	10
L	L	H	L	H	H	L	H	11
H	H	L	L	L	L	H	H	12
L	H	L	L	H	L	H	H	13
H	L	L	L	L	H	H	H	14
L	L	L	L	H	H	H	H	15
H	H	H	H	L	L	L	L	0

Note: CPE, R, P_0, P_1, P_2, and P_3 inputs are all High; transition from a count position to the following one is attained through a high – to – low CP input transition.

OUTPUTS: $L = V_{OL}$
$H = V_{OH}$
INPUTS: $L = V_{IL}$
$H = V_{IH}$

LOGIC DIAGRAM



LOADING RULES (1 U.L. = 1 HLL gate input unit load)

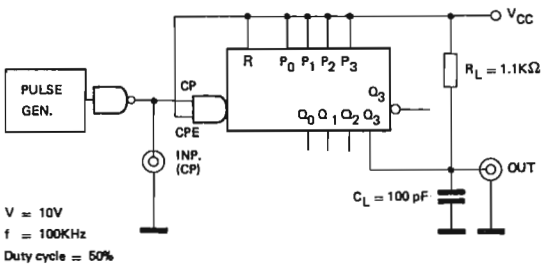
INPUTS:	CP, CPE	LOADING FACTOR	= 1 U.L.
	P_0, P_1, P_2, P_3		= 1.4 U.L.
	R		= 5.4 U.L.
OUTPUTS:	$Q_0, Q_1, Q_2, Q_3, \bar{Q}_3$	DRIVING FACTOR	= 25 U.L.

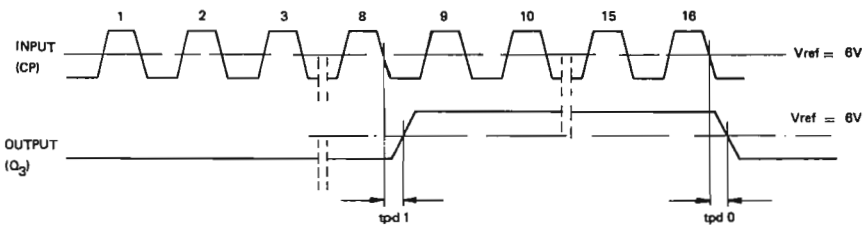
SWITCHING CHARACTERISTICS ($T_A = 25°C$)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
t_{pd1}	Turn-Off Delay		350	600	nsec	V_{CC} = 15V R_L = 1.1KΩ
t_{pd0}	Turn-On Delay		220	400	nsec	C_L = 100pF
f	Max. Input Clock Frequency	0.5	1		MHz	See test circuit

Notes: The rise and fall times of the clock pulse must be lower than 5 μsec/V.
The clock pulse width at high level must be higher than 300 ns.

tpd TEST CIRCUIT





decade counter

STANDARD TEMPERATURE RANGE, 0°C TO 75°C

- SYNCHRONOUS COUNTING
- ASYNCHRONOUS PRESET
- ASYNCHRONOUS RESET
- WIDE RANGE OF SUPPLY VOLTAGE 10.8 TO 20 V
- HIGH DC NOISE IMMUNITY, 5 V AT V_{CC} = 15V
- HIGH FAN-OUT 25 (WORST CASE)
- 14 PIN CERAMIC DIP

The H 157 is a synchronous 8421 BCD Counter. It is an asynchronously presettable, multifunctional building block usable in a large number of counting applications. Belonging to the High Level Logic family, the high threshold family of integrated circuits, it offers the advantages of 5V DC noise immunity, high signal levels, wide supply voltage tolerance and unusually high fan-out. These features make the H 157 particularly suitable for industrial, avionic and telephone applications, where the high noise environment might prohibit the use of a low threshold integrated circuit.

ABSOLUTE MAXIMUM RATINGS
(above which the useful life may be impaired)

Supply Voltage (V_{CC}) continuous	22 V
Input Voltage	- 0.5 V to 20V
Storage Temperature Range	-55°C to 150°C

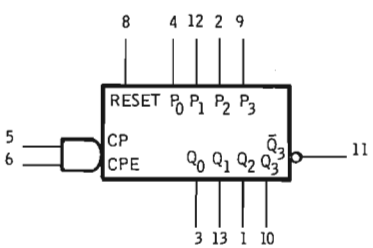
OPERATING CONDITIONS

Temperature Range	0°C to 75°C
Supply Voltage	10.8 V to 20 V

ORDERING NUMBER

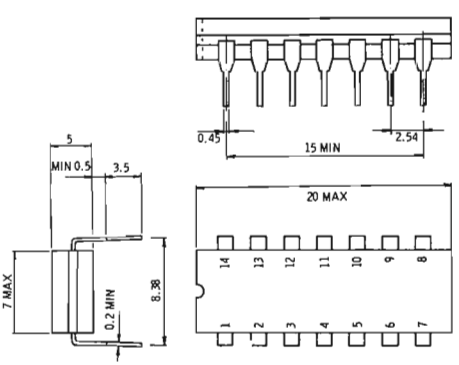
H157 D1

LOGIC DIAGRAM AND PIN CONNECTION



GND = PIN 7
V_{CC} = PIN 14

PHYSICAL DIMENSIONS
14-pin ceramic DIP



Note : all dimensions in mm.

ELECTRICAL CHARACTERISTICS (T_A = 0°C to 75°C, V_{CC} = 10.8V to 20 V)

SYMBOL	CHARACTERISTICS	LIMITS 0°C Min.	LIMITS 0°C Max.	LIMITS 25°C Min.	LIMITS 25°C Max.	LIMITS 75°C Min.	LIMITS 75°C Max.	UNIT	CONDITIONS
V_{OH}	Output High Voltage	18.5		18.5		18.5		V	V_{CC}= 20V I_{OH} =-200 µA
		13.5		13.5		13.5		V	V_{CC}= 15V I_{OH} =-200 µA
		9.3		9.3		9.3		V	V_{CC}= 10.8V I_{OH} =-200 µA
									$V_{IN(async.)}$= V_{IL} (see below)
V_{OL}	Output Low Voltage		1.5		1.5		1.5	V	V_{CC}= 20V I_{OL} = 15 mA or
									V_{CC}= 15V I_{OL} = 12 mA or
									V_{CC}= 10.8V I_{OL} = 9 mA
									$V_{IN(async.)}$ = V_{IH} (see below)
V_{IL}	Input Low Voltage		6		6		6	V	Guaranteed input low threshold for all inputs
V_{IH}	Input High Voltage	8		8		8		V	Guaranteed input high threshold for all inputs
I_F	Input Low Current		-0.8		-0.8		-0.8	mA	V_{CC}= 20V V_F = 1.5 V
	P_0, P_1, P_2, P_3 Inputs		-0.64		-0.64		-0.64	mA	V_{CC}= 15V V_F = 1.5 V
			-0.48		-0.48		-0.48	mA	V_{CC}= 10.8V V_F = 1.5 V
									Reset grounded
	Reset Input		-3.2		-3.2		-3.2	mA	V_{CC}= 20V V_F = 1.5V
			-2.56		-2.56		-2.56	mA	V_{CC}= 15V V_F = 1.5V
			-1.92		-1.92		-1.92	mA	V_{CC}= 10.8V V_F = 1.5 V
									Preset inputs grounded
I_{FCP}	Input Low Current		-0.6		-0.6		-0.6	mA	V_{CC}= 20V V_F = 1.5V
	Clock Inputs		-0.48		-0.48		-0.48	mA	V_{CC}= 15V V_F = 1.5V
			-0.36		-0.36		-0.36	mA	V_{CC}= 10.8V V_F = 1.5V
									V_{CC} on the clock input not under test
I_R	Reverse Input Current								
	P_0, P_1, P_2, P_3 Inputs		5		5		5	µA	V_{CC}= 20V V_R = 20V
									V_{CC} on reset and clock inputs
	Reset Input		20		20		20	µA	V_{CC}= 20V V_R = 20V
									V_{CC} on preset and clock inputs
I_{RCP}	Reverse Input Current Clock Inputs		5		5		5	µA	V_{CC}= 20V V_R = 20V
									Ground on the clock input not under test
I_{SC}	Output Short Circuit Current	-9	-25	-9	-25	-9	-25	mA	V_{CC}= 20V
									Output and proper asynchronous inputs grounded
I_{PD}	Power Dissipation Current		36		36		36	mA	V_{CC}= 20V
									Reset grounded

FUNCTIONAL DESCRIPTION

A clock buffer drives the four JK master slave flip-flops in parallel,so that synchronous operation is obtained.
The information contained in the master is transferred to the slave flip-flops during the clock pulse high-to-low transition; the information contained in the slaves is available on their outputs Q_0, Q_1, Q_2, and Q_3.
Four asynchronous preset (P) inputs are provided, allowing the counter to be positioned to any counting number from 0 to 9. In order to preset the counter the following operations are necessary :

1. Disable the counter by applying a low level to CPE input,
2. Reset the counter by applying a low level to Reset input,
3. Insert in the counter the desired output configuration by applying to Preset inputs the levels shown in the Preset Count truth table (for example : if the desired preset is the count position 7, required preset inputs are $P_0 = P_1 = P_2 = L$, $P_3 = H$),
4. Apply a high level to Reset input,
5. Apply high levels to Preset inputs,
6. Enable the counter by applying a high level to CPE input; at this point of the example outputs are :
   $Q_0 = Q_1 = Q_2 = H$, $Q_3 = L$, that is a count of 7. The next CP high-to-low transition sets the counter on $Q_0 = Q_1 = Q_2 = L$, $Q_3 = H$,that is the count position 8.

Counter disabling by low level on CPE, operation N° 1, is not strictly required : it is recommended in order to avoid spike generation on the first stage due to CP transition during reset operations.
From the above it can be seen that zero reset during BCD count sequence, when P inputs are already high, can be accomplished by the simplified operation sequence:

1. CPE H to L,
2. Reset H to L,
4. Reset L to H,
6. CPE L to H.

TRUTH TABLES

BCD COUNT SEQUENCE (see note)

OUTPUTS				COUNT
Q_0	Q_1	Q_2	Q_3	
L	L	L	L	0
H	L	L	L	1
L	H	L	L	2
H	H	L	L	3
L	L	H	L	4
H	L	H	L	5
L	H	H	L	6
H	H	H	L	7
L	L	L	H	8
H	L	L	H	9
L	L	L	L	0

Note: CPE, R, P_0, P_1, P_2 and P_3 inputs are all H; transition from a count position to the following one is attained through a high-to-low CP input transition.

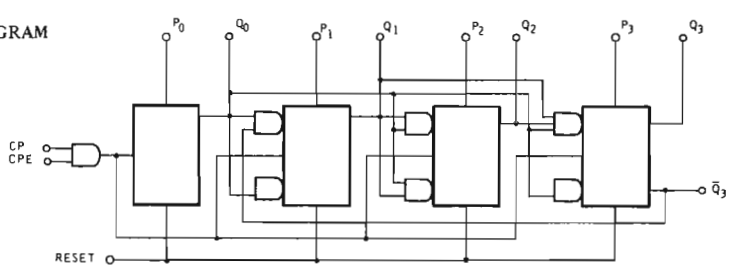
PRESET COUNT

INPUTS				OUTPUTS				COUNT
P_0	P_1	P_2	P_3	Q_0	Q_1	Q_2	Q_3	
H	H	H	H	L	L	L	L	0
L	H	H	H	H	L	L	L	1
H	L	H	H	L	H	L	L	2
L	L	H	H	H	H	L	L	3
H	H	L	H	L	L	H	L	4
L	H	L	H	H	L	H	L	5
H	L	L	H	L	H	H	L	6
L	L	L	H	H	H	H	L	7
H	H	H	L	L	L	L	H	8
L	H	H	L	H	L	L	H	9

OUTPUTS : L = V_{OL}, H = V_{OH}

INPUTS : L = V_{IL}, H = V_{IH}

LOGIC DIAGRAM



LOADING RULES (1 U.L. = 1 HLL gate input unit load)

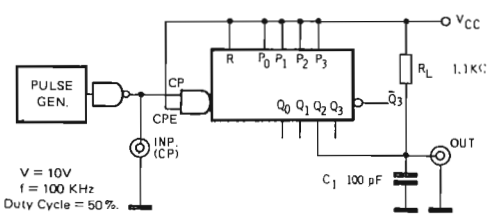
INPUTS :	CP, CPE	LOADING FACTOR	= 1 U.L.
	P0, P1, P2, P3		= 1.4 U.L.
	R		= 5.4 U.L.
OUTPUTS :	Q0, Q1, Q2, Q3, $\bar{Q}3$	DRIVING FACTOR	= 25 U.L.

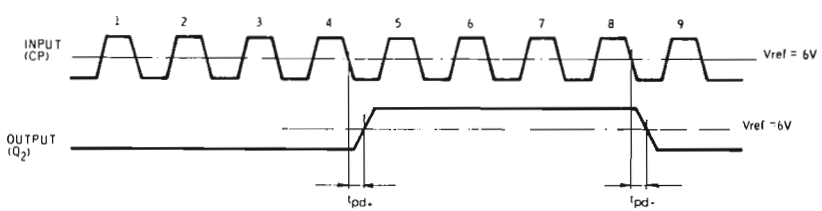
SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	CHARACTERISTICS	Min.	Typ.	Max.	UNIT	CONDITIONS
t_{pd+}	Turn-off Delay		350	600	nsec	V_{CC} = 15 V
t_{pd-}	Turn-on Delay		220	400	nsec	C_L = 100 pF
						R_L = 1.1 KΩ
f	Max. Input Clock Frequency	0.5	1		MHz	See test circuit

NOTES : The rise and fall times of the clock pulse must be lower than 5 μsec/V.
The clock pulse width at high level must be higher than 300 nS.

t_{pd} TEST CIRCUIT





STANDARD TEMPERATURE RANGE
0°C to 75°C

BCD to Decimal Decoder/Driver

The H 158 is an HLL compatible BCD to Decimal Decoder/Driver. It accepts 8421 binary coded decimal inputs and provides ten mutually exclusive outputs which are able to directly drive gas-filled, cold-cathode indicator tubes. In accordance with the High Level Logic family characteristics, it offers the advantages of 5V DC noise immunity, high signal levels, wide supply voltage tolerances and unusually low fan-in. These features make the H 158 particularly suitable for industrial, avionic and telephone applications where the high noise environment might prohibit the use of a low threshold integrated circuit.

- STABLE HIGH-VOLTAGE OUTPUT CHARACTERISTICS AT 55V
- DIRECT DISPLAY DRIVE CAPABILITY
- WIDE RANGE OF SUPPLY VOLTAGE 10.8 V to 20V
- HIGH DC NOISE IMMUNITY, 5V AT V_{CC} = 15V
- 16-PIN CERAMIC DIP

ABSOLUTE MAXIMUM RATINGS
(above which the useful life may be impaired)

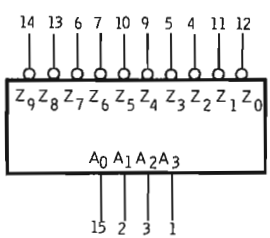
Supply Voltage (V_{CC}) Continuous	22 V
Input Voltage	-0.5 V to 20 V
Storage Temperature Range	-65°C to 150°C

OPERATING CONDITIONS

Temperature Range	0°C to 75°C
Supply Voltage	10.8 V to 20 V

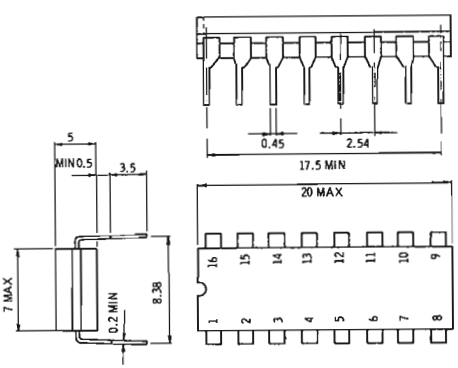
ORDERING NUMBER
H 158 D1

LOGIC DIAGRAM AND PIN CONNECTION



GND = PIN 8
V_{CC} = PIN 16

PHYSICAL DIMENSIONS
16-pin ceramic DIP



Note : all dimensions in mm.

ELECTRICAL CHARACTERISTICS (T_A = 0°C to 75°C, V_{CC} = 10.8V to 20V)

SYMBOL	CHARACTERISTICS	LIMITS 0°C Min.	LIMITS 0°C Max.	LIMITS 25°C Min.	LIMITS 25°C Max.	LIMITS 75°C Min.	LIMITS 75°C Max.	UNIT	CONDITIONS
V_{OH}	Output High Voltage	55		55		55		V	V_{CC}=10.8 to 20V I_{OH}=100 µA V_{IN} at input thresholds
I_{CEX}	Output Leakage Current		20		20		20	µA	V_{CC}=10.8 to 20V V_{OUT}=20V V_{IN} at ground or V_{CC}
V_{OL}	Output Low Voltage		2		2		2	V	V_{CC}=10.8 to 20V I_{OL}=7mA V_{IN} at input thresholds
V_{IL}	Input Low Voltage		6		6		6	V	Guaranteed input low threshold for all inputs
V_{IH}	Input High Voltage	8		8		8		V	Guaranteed input high threshold for all inputs
I_F	Input Low Current		-0.6		-0.6		-0.6	mA	V_{CC}=20V
			-0.48		-0.48		-0.48	mA	V_{CC}=15V V_F=1.5V
			-0.36		-0.36		-0.36	mA	V_{CC}=10.8V
I_R	Input Reverse Current		5		5		5	µA	V_{CC} and V_R = 10.8 to 20 V
I_{PD}	Power Dissipation Current		30		30		30	mA	V_{CC}=20V Inputs Grounded

LOADING RULES (1 U.L. = 1 HLL GATE INPUT UNIT LOAD)

INPUTS : A_0 A_1 A_2 A_3 LOADING FACTOR = 1 U.L.

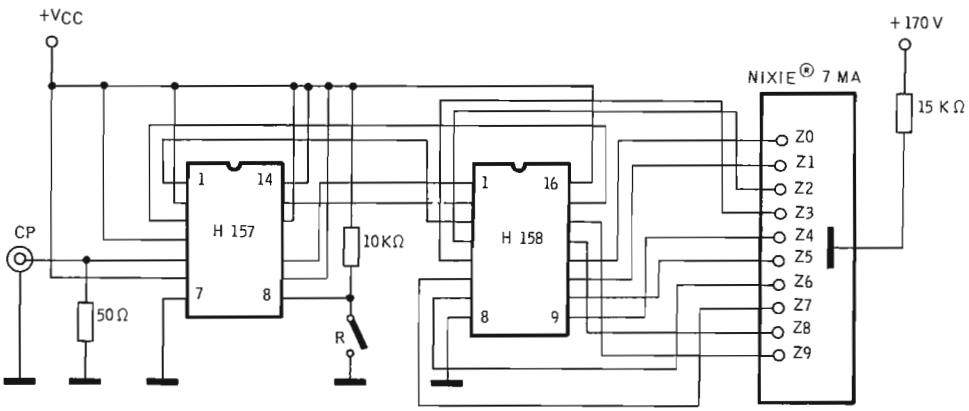
FUNCTIONAL DESCRIPTION

The BCD to Decimal Decoder/Driver accepts BCD inputs from HLL or MOS circuits and produces the correct output selection to directly drive gas-filled, cold-cathode indicator tubes.
The outputs are selected as shown in the Truth Table. The H 158 is capable of driving all known available cold cathode indicator tubes having 7mA or less cathode current.

A_0	A_1	A_2	A_3	Z_0	Z_1	Z_2	Z_3	Z_4	Z_5	Z_6	Z_7	Z_8	Z_9
L	L	L	L	L									
H	L	L	L		L								
L	H	L	L			L							
H	H	L	L				L						
L	L	H	L					L					
H	L	H	L						L				
L	H	H	L							L			
H	H	H	L								L		
L	L	L	H									L	
H	L	L	H										L

Note : Positions not shown are High.

COUNTING TEST CIRCUIT



MOS INTEGRATED CIRCUITS

MOS INTEGRATED CIRCUITS

Multifunction gate

STANDARD TEMPERATURE RANGE 0° C TO 70° C

- INPUT GATE PROTECTION
- OUTPUT DRIVE VERSATILITY
- LOW POWER CONSUMPTION
- TWO DIFFERENT SUPPLY VOLTAGES ($-V_{DD}$; $-V_{GG}$)

The M001 is a monolithic integrated circuit utilizing channel enhancement mode MOS technology. The device can be used to gain familiarity with MOS integrated circuit logic versatility as a building block in a MOS system, or as a breadboarding gate in the design of complex custom integrated circuits.

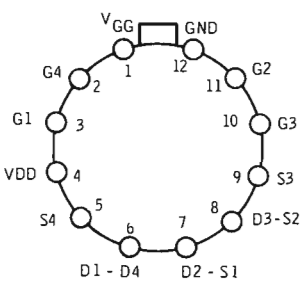
ABSOLUTE MAXIMUM RATINGS
(above which the useful life may be impaired)

Voltage on any Pin (V_{body} = 0)	-30V to +0.3V
Storage Temperature	-55° C to +150° C
Operating Temperature	0° C to +70° C

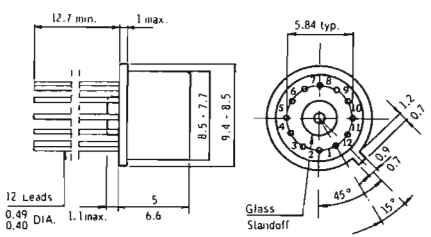
ORDERING NUMBER

M001 T1

CONNECTION DIAGRAM
(Top view)



PHYSICAL DIMENSIONS
In accordance with
JEDEC TO-73 outline



Notes : All dimensions in mm.
Lead No. 6 internally connected to case.

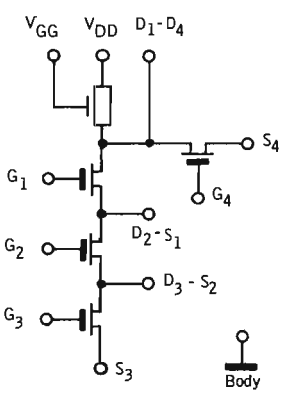
ELECTRICAL CHARACTERISTICS ($V_{body} = 0$; $T_A = 25°C$)

PARAMETER	CONDITIONS		Min.	Typ.	Max.	UNIT
Load Resistance	$V_{DD} = V_{GG} = -27 \pm 1V$	$V_{D1-D4} = GND$	23	32		K Ω
	$V_{DD} = -13V \pm 1V$	$V_{GG} = -27V \pm 1V$				
	$V_{D1-D4} = GND$		13	18		K Ω
On Resistance	$V_{in} = -19V$	$I_{Ron} = -100\ \mu A$		350	1000	Ω
	$V_{in} = -9V$	$I_{Ron} = -100\ \mu A$		500	1200	Ω
Input Leakage Current	$V_{in} = -20V$				1	μA
Threshold Voltage (VTH)	$V_{DD} = V_{GG} = GND$	$I_D = -10\ \mu A$	3.3		5.7	V
Input High Voltage			-9			V
Input Low Voltage					-3	V
Power Consumption	$V_{DD} = -28V$			20		mW

TYPICAL RESISTANCE CHARACTERISTICS

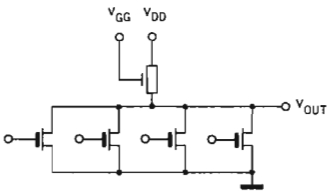
PARAMETER	CONDITIONS			VALUE
R_{Load}	$V_{DD} = -13V$	$V_{GG} = -27V$	$V_{D1} = 0V$	18 KΩ
	$V_{DD} = -27V$	$V_{GG} = -27V$	$V_{D1} = 0V$	32 KΩ
R_{on}	$V_{GS} = -19V$	$V_{DS} \leq -1V$	$V_{D2} = 0V$	350 Ω
	$V_{GS} = 9V$	$V_{DS} \leq -1V$	$V_{D2} = 0V$	500 Ω

SCHEMATIC DIAGRAM



BASIC APPLICATIONS :

NOR GATE CONFIGURATION



Pin 8 = Pin 6 = V_{out}
Pin 9 = Pin 7 = Pin 5 = GND
V_{DD} = V_{GG} = -27V

Logic Level	Voltage Level Min.	Max.
VOH (1)	-14V	
VOL (0)		-1.2V

Pin 8 = Pin 6 = V_{out}
Pin 9 = Pin 7 = Pin 5 = GND
V_{DD} = -13V V_{GG} = -27V

Logic Level	Voltage Level Min.	Max.
VOH (1)	-10V	
VOL (0)		- 1V

NAND GATE CONFIGURATION

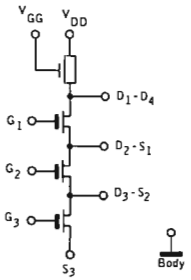
3-Input Gate

Pin 9 = GND
Pin 6 = Output
V_{GG} = V_{DD} = -27V

Logic Level	Voltage Level Min.	Max.
VOH (1)	-14V	
VOL (0)		-2.7V

Pin 9 = GND
Pin 6 = Output
V_{DD} = -13V
V_{GG} = -27V

Logic Level	Voltage Level Min.	Max.
VOH (1)	-10V	
VOL (0)		-2.5V



2-Input Gate

Pin 8 = GND
Pin 6 = Output
V_{GG} = V_{DD} = -27V

Logic Level	Voltage Level Min.	Max.
VOH (1)	-14V	
VOL (0)		-2V

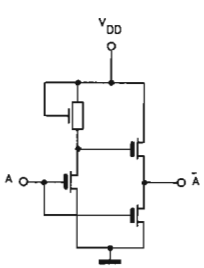
Pin 8 = GND
Pin 6 = Output
V_{DD} = -13V
V_{GG} = -27V

Logic Level	Voltage Level Min.	Max.
VOH (1)	-10V	
VOL (0)		-1.8V

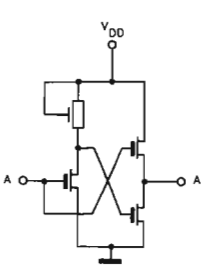
OTHER APPLICATIONS

MOS logic provides the versatility to build many different functions. The following circuits show how to build functions using one or two M001 packages. (V_{DD} = - 27V)

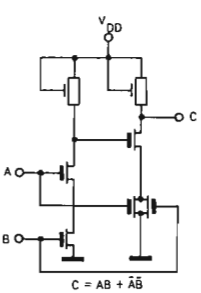
INVERTING BUFFER



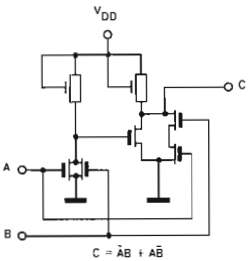
NON-INVERTING BUFFER



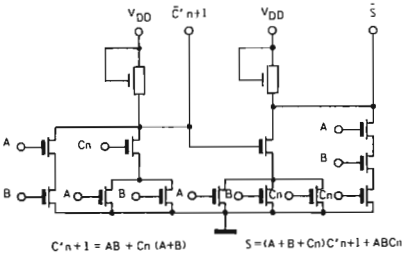
EXCLUSIVE NOR



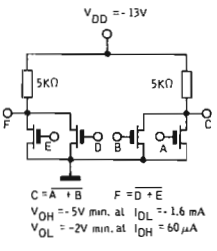
EXCLUSIVE OR



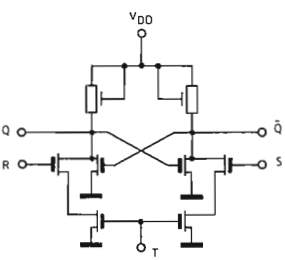
FULL ADDER



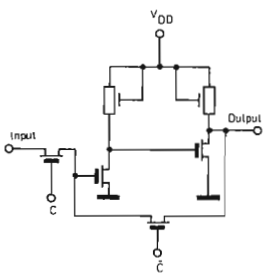
TTL INTERFACE



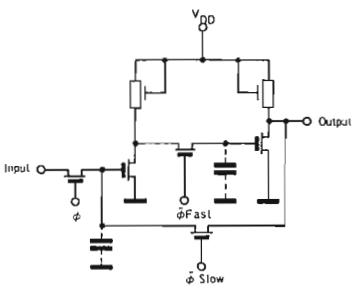
RST FLIP-FLOP



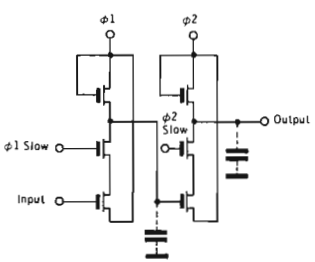
TYPE D FLIP-FLOP



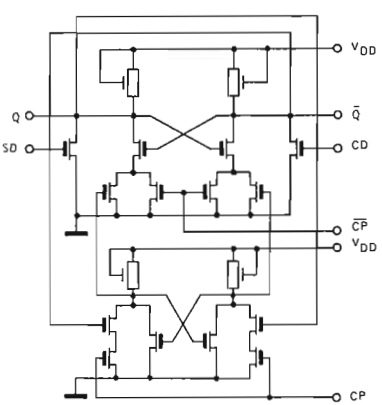
STATIC (DC) SHIFT REGISTER BIT



DYNAMIC 4-PHASE (4 Φ) SHIFT REGISTER BIT



FREQUENCY DIVIDER (Input = CP)



4-phase clock driver

STANDARD TEMPERATURE RANGE
0°C to 70°C

- HIGH OUTPUT VOLTAGE SWING
- ONLY ONE INPUT SIGNAL REQUIRED
- FOUR PHASES IN ONE TO-100 PACKAGE
- THREE DIFFERENT PHASE MODES
- BIPOLAR COMPATIBLE SYNCHRONIZING PULSE

The M002 is a P-channel enhancement mode monolithic MOS integrated circuit. The device generates four clock signals and is capable of directly driving dynamic, high threshold, MOS circuits or systems. It requires an external reference frequency and produces output clock signals at a rate equal to one-fourth the input clock frequency. The output states change after the positive transition of the input clock. The output clock signals are available in three different timing modes which satisfy the majority of all four-phase systems requirements. These modes are selectable by two external control lines (M, N) which can be grounded ("0") or left floating ("1"). Low output source impedance in the "0" and the "1" states is obtained by high efficiency push-pull drivers. The bipolar compatible sync. pulse is available via an open drain MOS transistor.

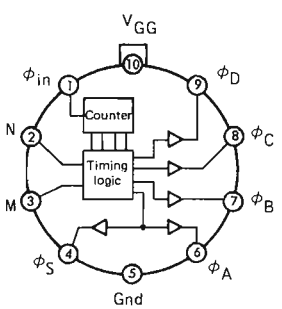
ABSOLUTE MAXIMUM RATINGS
(above which the useful life may be impaired)

Input voltage (1)	-30V to +0.3V
Supply Voltage (1)	-30V to+ 0.3V
Storage Temperature	-55°C to + 150°C
Power Dissipation (2)	500 mW at T_A = 70°C

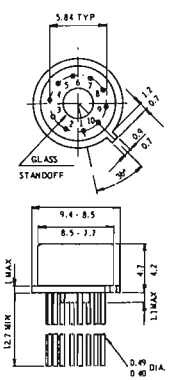
Note 1 : This voltage is with respect to the Gnd pin voltage
Note 2 : See following page

ORDERING NUMBER
M 002 T1

CONNECTION DIAGRAM
(Top view)



PHYSICAL DIMENSIONS
in accordance with
JEDEC TO-100



Note : all dimensions in mm.

ELECTRICAL CHARACTERISTICS : (T_A = 0°C to 70°C, V_{GG} = -27V ± 1V unless otherwise noted)

SYMBOL	CHARACTERISTIC	Min.	Max.	Unit	TEST CONDITIONS
	INPUT CLOCK (Φ_{in})				
f_{in}	Repetition Rate Range	4	2000	kHz	
V_{ILcp}	"0" Level Voltage		-2	V	
V_{IHcp}	"1" Level Voltage	-9		V	
V_{Ipw}	Pulse Width	200		nsec	
	PHASE OUTPUTS (Φ_A-Φ_B-Φ_C-Φ_D)				
f_{out}	Repetition Rate Range	1	500	kHz	
V_{OL}	"0" Level Voltage		-0.5	V	I_{OL} = 2 mA
V_{OH}	"1" Level Voltage	-25.5		V	I_{OH} = 2 mA
t_r	Rise Time		100	nsec	C_L = 200 pF, T_A = 25°C
t_f	Fall Time		200	nsec	see fig. 1
V_{OV}	Overlap Voltage		-5	V	see fig. 2
	SYNC. OUTPUT (Φ_S)				
R_{on}	"On" resistance		900	Ω	V_{out} = 0 to -3V
I_L	Leakage Current (off)		1	μA	V_{out} = -5V

Note 2 : Power limits are:
500 mW at T_A = 70°C } without heat-sink
700 mW at T_A = 25°C }
800 mW at T_A = 70°C with a 50°C/W heat-sink

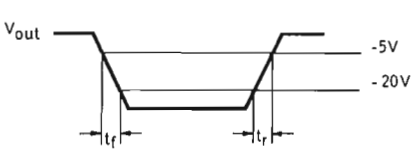


Fig. 1

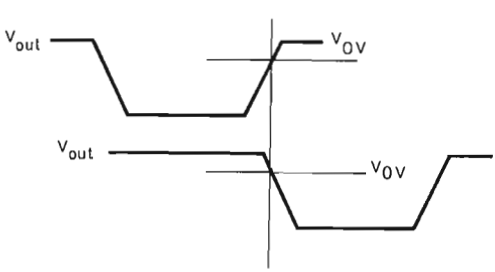
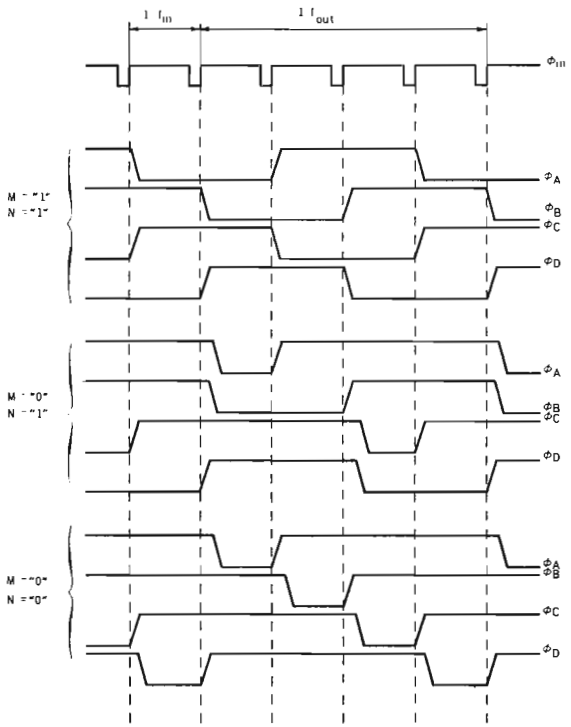
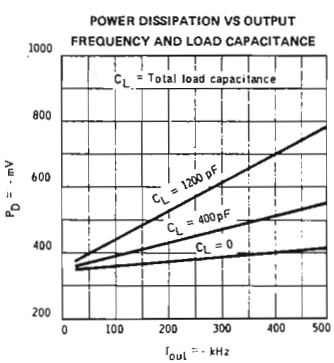
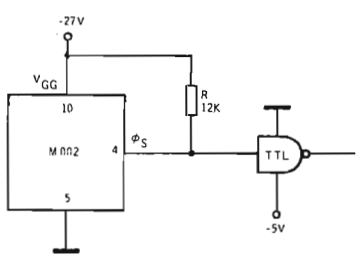


Fig. 2

TYPICAL TIMING DIAGRAM







Sync. out driving TTL

Quad up/down decade counter

EXTENDED TEMPERATURE RANGE
-55°C to 125°C
STANDARD TEMPERATURE RANGE
0°C to 70°C

- FULLY TTL COMPATIBLE
- DC TO 1MHz OPERATION
- SINGLE PHASE CLOCK
- INPUT GATE PROTECTION

The M003 is a quad up/down decade counter arranged as two subsystems of two decades each. Each subsystem has a single up/down control, zero and nine reset, and clock line. Common count enable input is provided for all decades, while synchronous carry-in inputs are available for each single counter. Constructed on a single monolithic chip using silicon nitride P-channel technology, the M003 has its reliability level enhanced by the use of the exclusive Planox process.

ABSOLUTE MAXIMUM RATINGS
(above which the useful life may be impaired)

Input Voltage (1)	-20V to 0.3V
Clock Voltage (1)	-20V to 0.3V
Supply Voltage (1)	-20V to 0.3V
Storage Temperature Range	-55°C to 150°C

ORDERING NUMBER

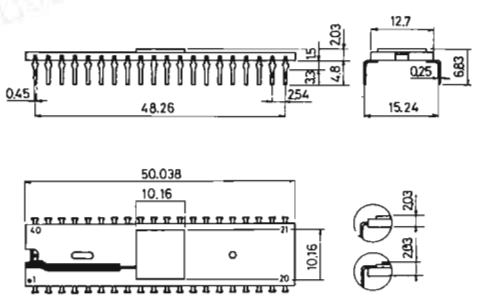
M003 T1 (for standard temperature range)
M003 T2 (for extended temperature range)

Note 1 This voltage is with respect to the V_{SS} pin voltage.

PIN CONNECTION

1	GND		21	VGG	
2	$\overline{\text{Carry OUT 3}}$		22	$\overline{\text{Carry OUT 2}}$	
3	CP (3-4)		23	$\overline{\text{Carry IN 2c}}$	
4	$\overline{\text{Carry IN 3b}}$		24	$\overline{\text{Carry IN 2b}}$	
5	$\overline{\text{Carry IN 3a}}$		25	$\overline{\text{Carry IN 2a}}$	
6	Reset 0 (3-4)		26	Reset to 9 (1-2)	
7	A3 LSD	Third decade outputs	27	A2 LSD	Second decade outputs
8	B3		28	B2	
9	C3		29	C2	
10	D3 MSD		30	D2 MSD	
11	Up/Down (3-4)		31	Up/Down (1-2)	
12	D4 MSD	Fourth decade outputs	32	D1 MSD	First decade outputs
13	C4		33	C1	
14	B4		34	B1	
15	A4 LSD		35	A1 LSD	
16	VGI		36	Reset to 0 (1-2)	
17	Reset to 9 (3-4)		37	$\overline{\text{Carry IN 1a}}$	
18	$\overline{\text{Carry IN 4}}$		38	$\overline{\text{Carry IN 1b}}$	
19	$\overline{\text{CP Enable}}$		39	CP (1-2)	
20	$\overline{\text{Carry OUT 4}}$		40	$\overline{\text{Carry OUT 1}}$	

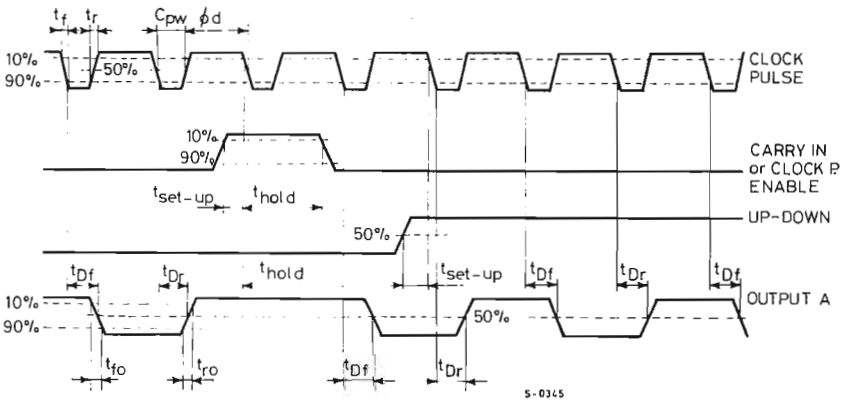
PHYSICAL DIMENSIONS
40 lead ceramic DIP



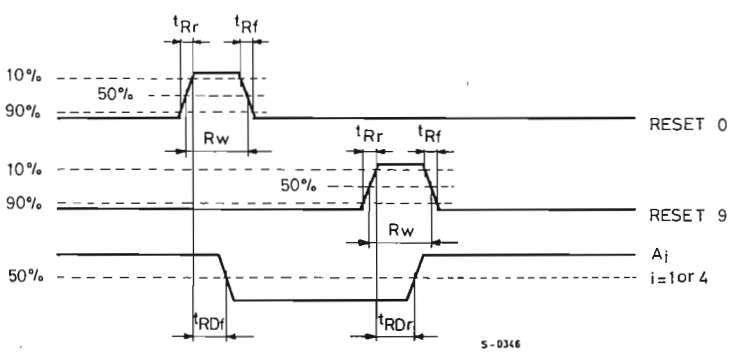
ELECTRICAL CHARACTERISTICS (T_A = 0°C to 70°C; V_{GG} = -12V ± 1V; V_{GI} = -5V ± 0.25V; V_{SS} = +5V ± 0.25V, unless otherwise noted)

SYMBOL	CHARACTERISTICS	Min.	Typ.	Max.	Unit	TEST CONDITIONS	
	CLOCK PULSES						
f	Repetition Rate Range	0		1	MHz		
C_{pw}	Pulse Width	500			ns		
ϕd	Pulse Separation	500			ns		
tr, tf	Rise and Fall Time			1000	ns	T_A=25°C	see waveforms
V_{ILcp}	"0" Level Voltage			V_{SS} -4.2	V		
V_{IHcp}	"1" Level Voltage	V_{SS} -1.5			V		
I_{Lcp}	Leakage Current			1	µA	V_{cp}=V_{SS} -15V	T_A=25°C
C_{cp}	Input Capacitance			10	pF	V_{cp}=V_{SS}	f = 1 MHz
	CONTROL INPUTS						
V_{IL}	"0" Level Voltage			V_{SS}-4.2	V		
V_{IH}	"1" Level Voltage	V_{SS} -1.5			V		
t_{set-up}	Set-up Time	200			ns		
t_{hold}	Hold Time	200			ns		
I_L	Leakage Current			1	µA	V_{cp}=V_{SS} -15V	T_A=25°C
C_{in}	Input Capacitance			10	pF	V_{cp}=V_{SS}	f = 1 MHz
	RESET 0 and 9						
V_{IL}	"0" Level Voltage			V_{SS} -4.2	V		
V_{IH}	"1" Level Voltage	V_{SS} - 1.5			V		
R_W	Reset Pulse Width	300			ns		
t_{Rf}, t_{Rr}	Reset Rise and Fall Time			1000	ns		
	DATA OUTPUTS						
V_{OL}	"0" Level Voltage			0.4	V	load = 10pF	I_{sink} = 1.6mA
V_{OH}	"1" Level Voltage	V_{SS} - 1			V	I_{OL} = 100µA	
t_{ro}	Rise Time		120		ns	see waveforms	
t_{fo}	Fall Time		200		ns	see waveforms	
	SWITCHING TIMES						
t_{Df}	Delay Time to Fall		300		ns	see waveforms	
t_{Dr}	Delay Time to Rise		250		ns	see waveforms	
t_{RDf}	Reset Delay Time to Fall		280		ns	see waveforms	
t_{RDr}	Reset Delay Time to Rise		280		ns	see waveforms	
	POWER CONSUMPTION						
I_{GG}	Gate Supply Current		6		mA		
I_{GI}	Buffer Supply Current		10		mA	T_A = 25°C	f = 1 MHz

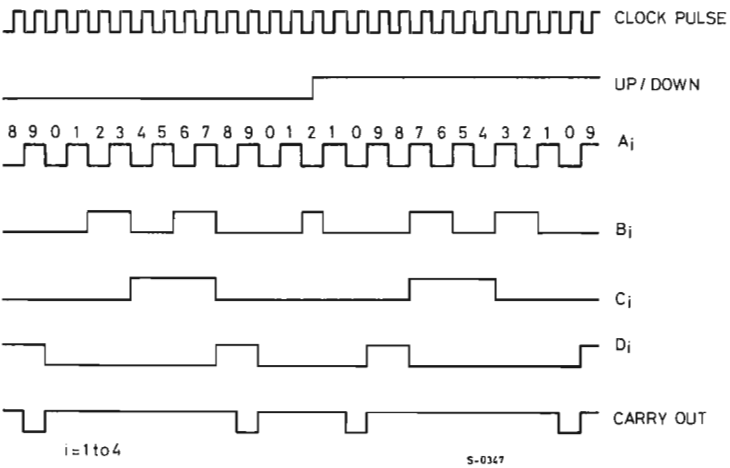
WAVEFORMS (SYNCHRONOUS INPUTS)



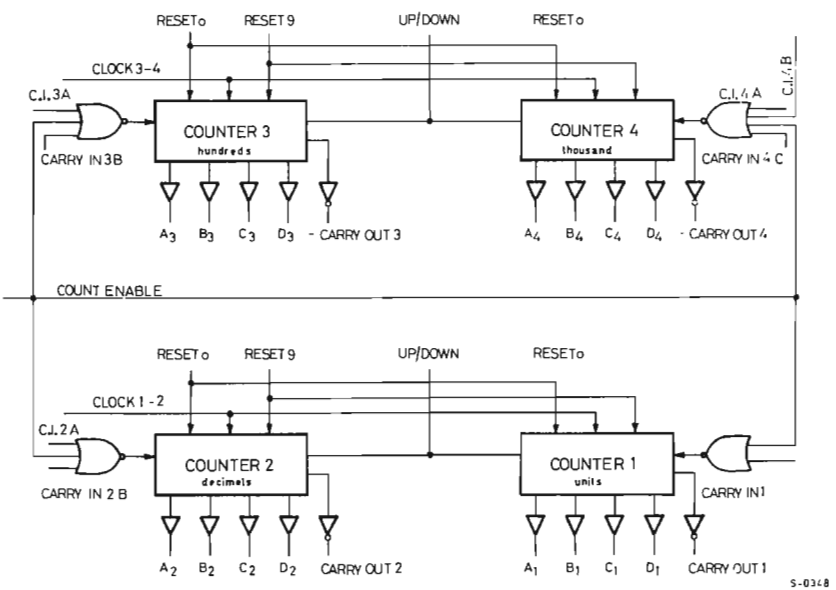
WAVEFORMS (ASYNCHRONOUS INPUTS)



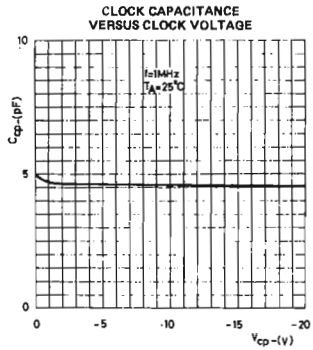
TYPICAL TIMING DIAGRAMS

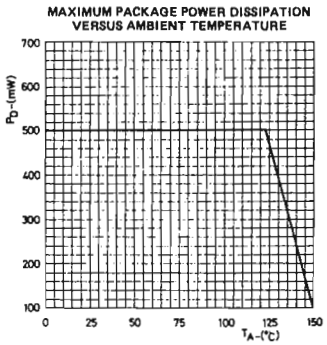


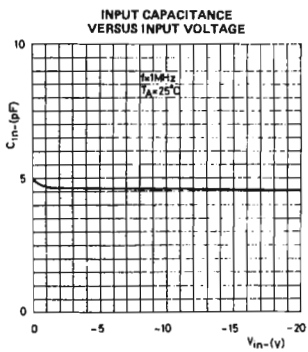
BLOCK DIAGRAM (FIG. 1)



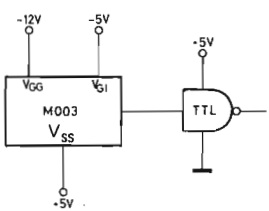
TYPICAL ELECTRICAL CHARACTERISTICS (contd.)



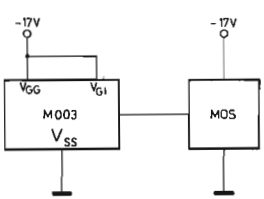




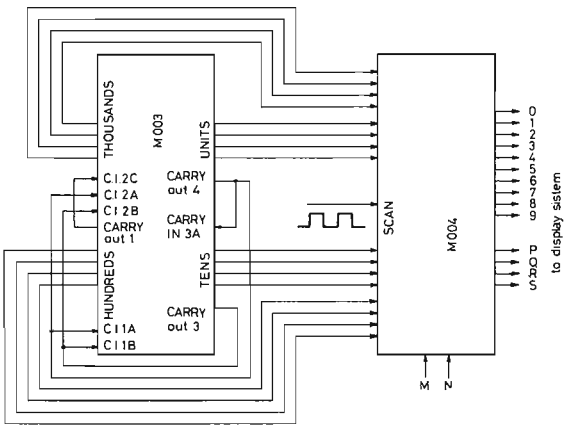
POWER CONNECTION FOR M003 DRIVING TTL (FIG. 2)



POWER CONNECTION FOR M003 DRIVING MOS (FIG. 3)



TYPICAL APPLICATION FOR a 4 DIGIT COUNTER (FIG. 4)



M004 Brief Description

The contents of 4 decades are memorized on 16 latch flip-flops. The content of one decade is shifted towards the decoder by means of the multiplexer; the selection is performed by control signals P, Q, R, S, which also appear at the output so as to select one display at a time.

Multiplexer scanning takes place at external "scan" signal frequency.

It is also possible to read the content of 2, 3 or 4 decades by means of the control signals M and N.

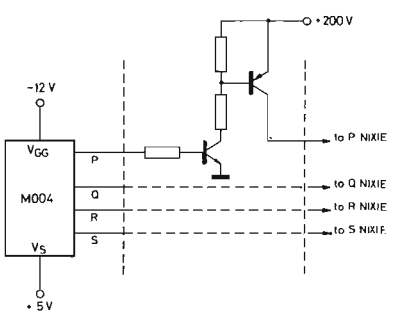
TYPICAL APPLICATION

The M 003 and M 004 devices find their typical application in all counting and display systems, such as digital instruments, watches, etc.

It follows that we can realize a binary-decoder (able to count up to 9999) with only two packages. The circuitry related to this application is shown in fig. 4.

For driving displays such as nixie tubes, the interface circuit shown in fig. 5 should be used, so allowing the unselected displays to be kept OFF, according to the signal logic level selected.

FIG. 5



4 - digit multiplexer/decoder

EXTENDED TEMPERATURE RANGE
-55°C to 125°C

STANDARD TEMPERATURE RANGE
0°C to 70°C

- FULLY TTL COMPATIBLE
- D.C. TO 1MHz OPERATION
- SINGLE PHASE CLOCK
- INPUT GATE PROTECTION

The contents of 4 decades are memorized by 16 latch flip-flops. The content of one decade is shifted towards the decoder by means of the multiplexer; selection is preformed by control signals P,Q,R,S, which also appear at the output so as to select only one display at a time. The M 004 also has a decoder with 10 decimal outputs. Two control signals M and N, allow the number of channels for scanning to be decided. Four outputs (P,Q,R,S,) indicate the channel selected and allow switch-on of one display and switch-off of the others. Display switch-off is also possible asynchronously by means of the blank signals. All the outputs are open-drain and the inputs are fully compatible with DTL/TTL. The device is realized on a single monolithic chip by means of the silicon-nitride Planox technology.

ABSOLUTE MAXIMUM RATINGS
(above which the useful life may be impaired)

Input Voltage (1)	-20 to 0.3V
Clock Voltage (1)	-20 to 0.3V
Supply Voltage (1)	-20 to 0.3V
Storage temperature range	-55°C to + 150°C

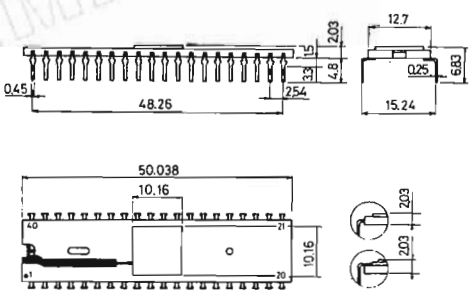
1) Note. This voltage is with respect to the V_{SS} pin voltage

ORDERING NUMBER
M 004 T1 (for standard temperature range)
M 004 T2 (for extended temperature range)

PIN CONNECTION

1	V_{SS}	21	B4
2	"9"	22	B3
3	"8"	23	B2
4	"7"	24	B1
5	"6"	25	A4
6	"5"	26	A3 } LSD
7	"4"	27	A2 } LSD
8	"3"	28	A1 } LSD
9	"2"	29	V_{GG}
10	"1"	30	M
11	"0"	31	N
12	SAMPLE	32	P
13	D4 } MSD	33	Q
14	D3 } MSD	34	R
15	D2 } MSD	35	S
16	D1 } MSD	36	BLANK S
17	C4	37	BLANK R
18	C3	38	BLANK Q
19	C2	39	BLANK P
20	C1	40	SCAN

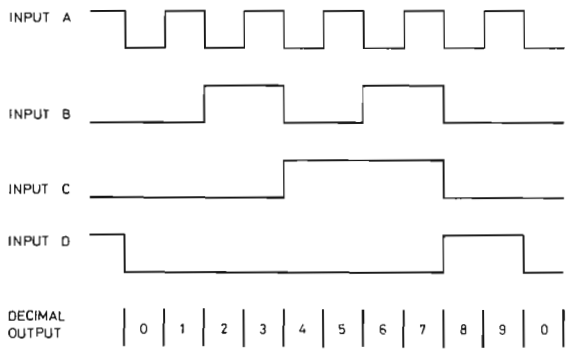
PHYSICAL DIMENSIONS
40 lead ceramic DIP



ELECTRICAL CHARACTERISTICS (V_{GG}= -12V ± 1V; V_{SS}= + 5V ± 0.5V unless otherwise noted)

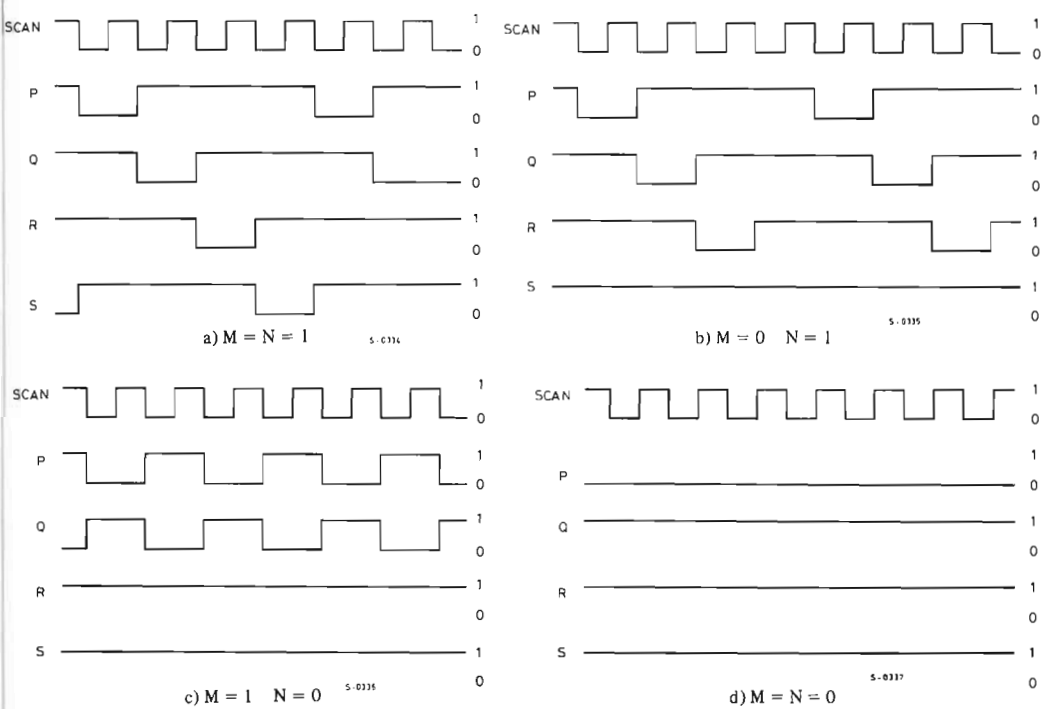
SYMBOL	CHARACTERISTICS	Min.	Typ.	Max.	UNIT	TEST CONDITIONS	
	CLOCK INPUTS (SAMPLE, SCAN)						
f	Repetition Rate Range	0		1	MHz		
C_{pw}	Pulse Width	400			ns		
ϕd	Pulse Separation	400			ns		
tr, tf	Rise and Fall Time			1	μs	T_A=25°C	
V_{ILcp}	"0" Level Voltage			V_{SS}-4.2	V		
V_{IHcp}	"1" Level Voltage	V_{SS}-1.5			V		
t set-up	Sample Set-up Time	200			ns	see waveforms	
t hold	Sample Hold Time	200			ns	see waveforms	
I_{Lcp}	Leakage Current			1	μA	$V_{cp}=V_{SS}$-15V	T_A = 25°C
C_{cp}	Input Capacitance			10	pF	$V_{cp}=V_{SS}$	f = 1 MHz
	DATA AND CONTROL INPUTS						
V_{IL}	"0" Level Voltage			V_{SS}-4.2	V		
V_{IH}	"1" Level Voltage	V_{SS}-1.5			V		
I_L	Leakage Current			1	μA	$V_{in}=V_{SS}$-15V	T_A = 25°C
C_{in}	Input Capacitance			10	pF	$V_{in}=V_{SS}$	f = 1 MHz
	DATA OUTPUTS						
R_{on}	Output ON Resistance			3.5	kΩ	I_{source} = 1mA	
R_{off}	Output OFF Resistance	100			MΩ		
	POWER CONSUMPTION						
I_{GG}	Gate Supply Current		18		mA		
P_d	Total Power Consumption		300		mW		

DECADE INPUTS/DECIMAL OUTPUT WAVEFORMS (Note 1)



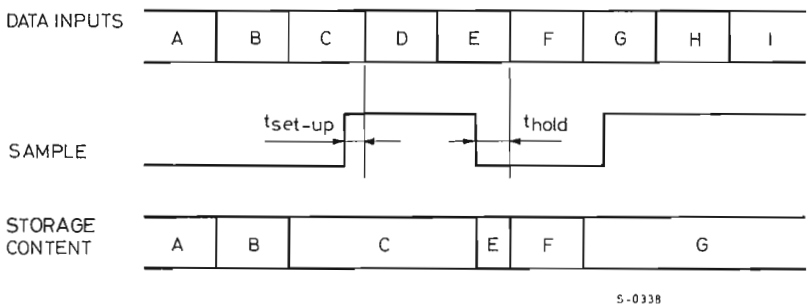
Note 1 : with sample at "1" level

MULTIPLEXER WAVEFORMS (Note 2)

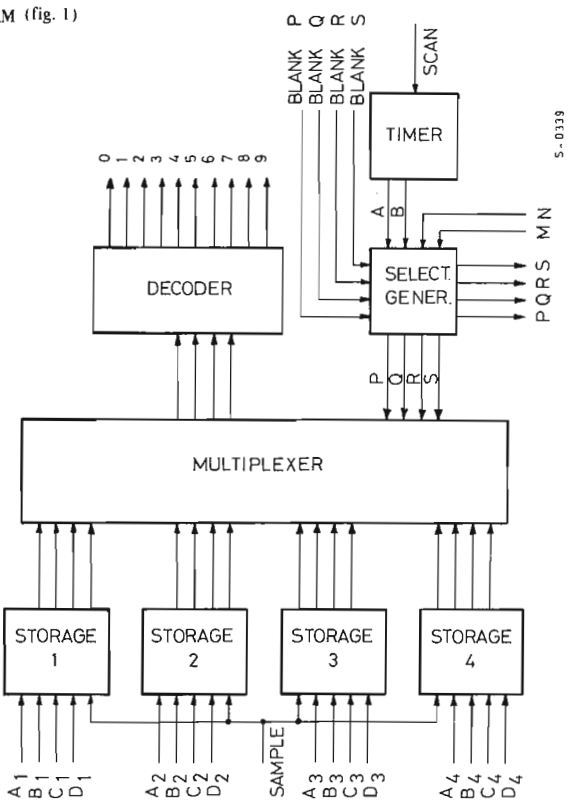


Note 2 : a V_{IH} level on a blank input forces the corresponding output transistor in the OFF state

SAMPLE FUNCTION

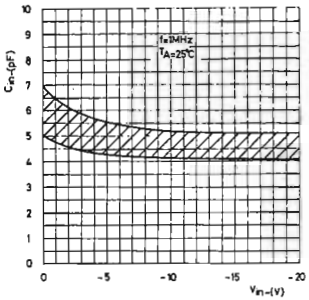


BLOCK DIAGRAM (fig. 1)

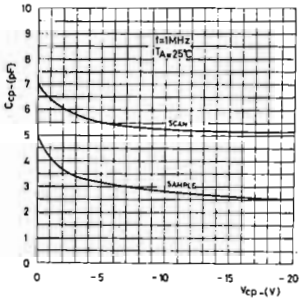


TYPICAL ELECTRICAL CHARACTERISTICS

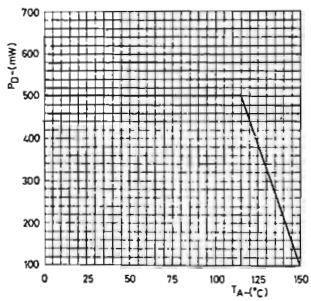
INPUT CAPACITANCE
VERSUS INPUT VOLTAGE



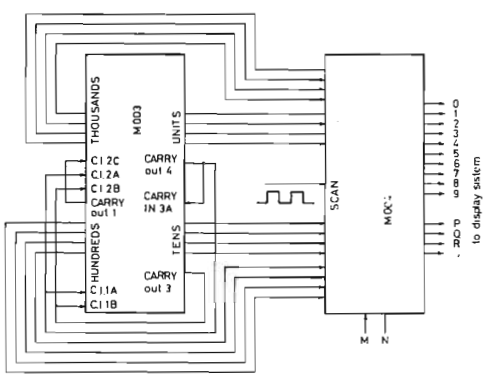
CLOCK CAPACITANCE
VERSUS CLOCK VOLTAGE



MAXIMUM PACKAGE POWER OISSIPATION
VERSUS AMBIENT TEMPERATURE



TYPICAL APPLICATION FOR a 4-DIGIT COUNTER (fig. 2)

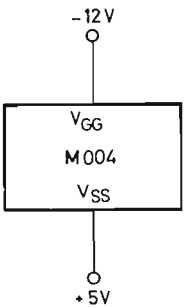


The M 003 and M 004 devices find their typical application in all counting and display systems, such as digital instruments, watches, etc.. It follows that we can realize a binary-decoder (able to count up to 9999) with only two packages (chips). The circuitry related to this application is shown in fig. 2.
For driving displays such as nixie tubes, the interface circuits shown in figs. 3, 4 should be used, so allowing the unselected displays to be kept OFF, according to the select signal logic level.

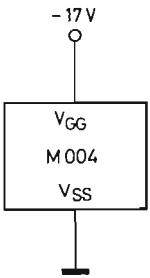
Brief description of the M 003.

The M 003 is a quad up/down decade counter arranged as two subsystems of two decades each.
Each subsystem has a single up/down control zero and nine reset clock line. Common count enable input is provided for all decades, while synchronous carry-in inputs are available for each single counter.

POWER CONNECTION OF M004 (fig. 3).



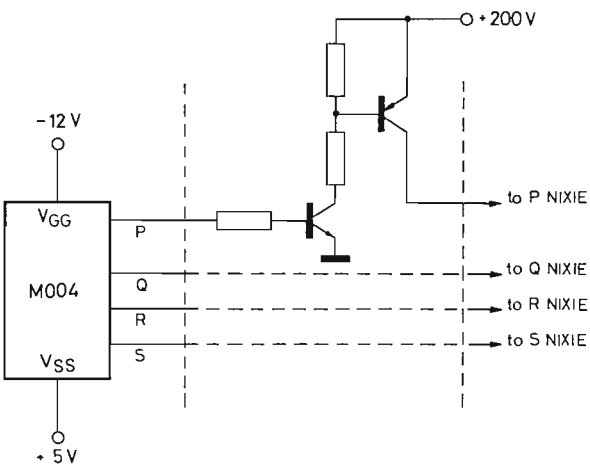
M004 used with TTL only



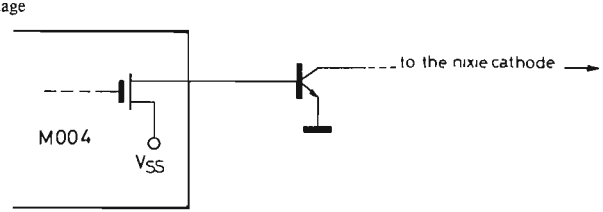
M004 used with MOS only

DISPLAY INTERFACES (fig. 4)

to drive nixie anode voltage



to drive nixie cathode voltage



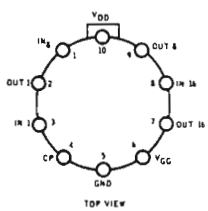
25 bit static shift register

EXTENDED TEMPERATURE RANGE, - 55°C + 85°C
STANDARD TEMPERATURE RANGE, 0°C + 70°C

The M 120 is a 25 bit Static Shift Register. It is a monolithic integrated circuit utilizing P-channel enhancement mode MOS technology. Input and output access is made available in 16,8 and 1 bit increments. This device is designed for use in single phase clock sequential digital systems as a delay line or memory element.

- **Input gate protection**
- **Low power 2 mW/bit**
- **Single phase clock**
- **Good capacitive driving capability**

CONNECTION DIAGRAM



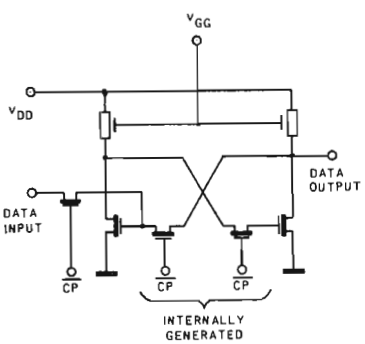
ABSOLUTE MAXIMUM RATINGS
(above which the useful life may be impaired)

Storage Temperature	-55°C to + 150°C
Voltage on Clock, Inputs and Supply Pins	-30°V to + 0,3 V

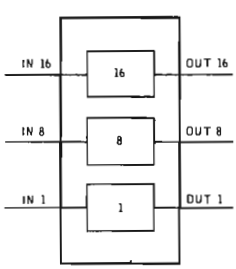
OPERATING LIMITS

Supply Voltages	$V_{GG} = -27\ V \pm 1V$ $V_{DD} = -13\ V \pm 1V$

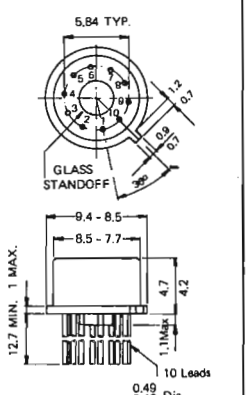
SCHEMATIC DIAGRAM
(ONE BIT)



BLOCK DIAGRAM



PHYSICAL DIMENSIONS
similar to
Jedec TO 100 outline



Notes All dimensions in mm.
Leads are gold plated K var.

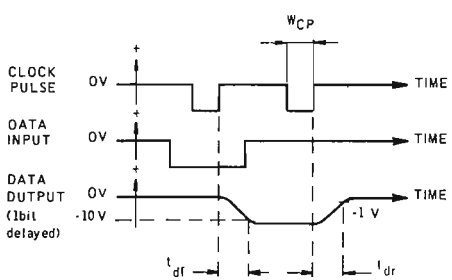
ORDERING NUMBER

M120 T1 (for standard temperature range)
M120 T8 (for extended temperature range)

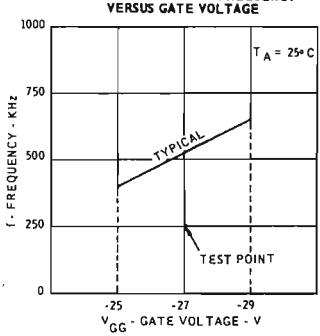
ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{GG} (Pin 6) = - 27 ± 1V, V_{DD} (Pin 10) = - 13 ± 1V, Load 10 Mohm 10 pF, unless otherwise specified)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	CONDITIONS
	Power Consumption		50		mW	V_{clock} = 0 V
	Operating Frequency	0		250	kHz	V_{GG} = - 27 V
V_{CP}	Clock Pulse Amplitude "0" level			- 2	V	
	"1" level	-9			V	
W_{CP}	Clock Pulse Width	1		100	µs	
	Clock Pulse Rise and Fall Time			10	µs	
	Clock Capacitance		3		pF	V_{CP} = 0 V
I_{CL}	Clock Leakage Current			- 1	µA	V_{CP} = - 20 V
V_{IL}	Input Amplitude "0" level			- 2	V	
V_{IH}	"1" level	-9			V	
C_{in}	Input Capacitance		2.5		pF	V_{in} = 0 V
I_{IL}	Input Leakage Current			- 1	µA	V_{in} = - 20 V
V_{OL}	Output Levels "0" level			- 1	V	I_{OUT} = - 10 µA
V_{OH}	"1" level	-10			V	I_{OUT} = - 10 µA
t_{df}	Time Delay-Fall		1		µs	
t_{dr}	Time Delay-Rise		1.2		µs	

TIMING DIAGRAM



TYPICAL OPERATING FREQUENCY VERSUS GATE VOLTAGE



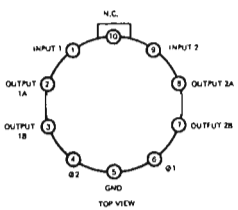
dual 25-bit dynamic shift register

EXTENDED TEMPERATURE RANGE - 55° C + 85° C
STANDARD TEMPERATURE RANGE - 0 + 70° C

- Input gate protection
- Low power - 2mW/Bit
- Two phases clock
- Output drive versatility

The M 121 is a Dual 25 Bit Dynamic Shift Register. It is a monolithic integrated circuit utilizing P-Channel enhancement mode MOS technology. A two phase clock is used to reduce power consumption and increase speed.

CONNECTION DIAGRAM



ABSOLUTE MAXIMUM RATINGS

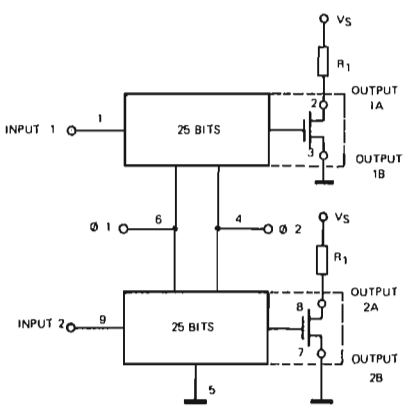
(above which the useful life may be impaired)

Clock Voltages ($V_{\phi 1} = V_{\phi 2}$)	- 30V to + 0.3V
Data Input Voltage (V_{in})	- 30V to + 0.3V
Supply Voltage	- 30V to + 0.3V
Storage Temperature	-55°C to + 150°C

OPERATING CONDITIONS

Clock Voltage	V_{ϕ} = - 27 V ± 1V
Temperature range (Extended)	- 55° C ÷ 85° C
Temperature range (Standard)	0° C + 70° C

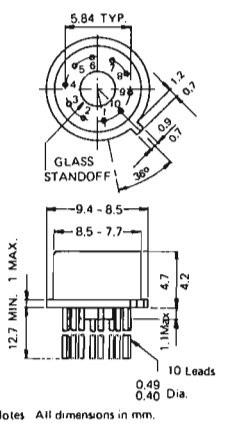
LOGIC DIAGRAM



The output device requires an external resistor (R_1), ground and power supply (V_S) and can be used either as an inverter or source follower (inverter shown).

PHYSICAL DIMENSIONS

similar to JEDEC to 100 outline



Notes All dimensions in mm.

ORDERING NUMBER

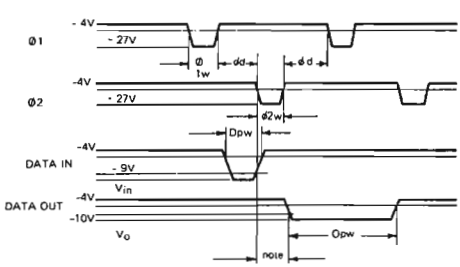
M 121 T1 (for standard temperature range)
M 121 T8 (for extended temperature range)

ELECTRICAL CHARACTERISTICS

V_s = −15 V ± 1 V, V_ϕ = − 27 V ± 1 V, R_1 = 20 KΩ, Load = 10 MΩ and 10 pF, T_A = − 55°C to 85°C or 0°C to 70°C according to the type No., unless otherwise specified.

SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNIT	CONDITIONS
ϕ_1, ϕ_2	Clock Repetition Rate	10		500	kHz	
ϕ_{1w}, ϕ_{2w}	Clock Pulse Width	0.4		45	μs	
ϕ_d	Clock Delay	0.4			μs	
V_ϕ	Clock Pulse Amplitude "0" Level "1" Level	 0 −26		 − 0.5 − 28	 V V	
	Clock Pulse Rise and Fall Time (10% − 90%)			100	ns	
V_{in}	Data Input Logic Levels Logic "0" Logic "1"	 0 −9		 − 2	 V V	ϕ_1 = 0.4 μs ϕ_2 = 0.4 μs
D_{pw}	Data Pulse Width	200			ns	
V_o	Output Logic Levels Logic "0" Logic "1"	 −10		 − 1	 V V	
	Output Fall Time			550	ns	
O_{pw}	Output Pulse Width	1			μs	
R_o	Output Impedance to Ground			1000	Ω	
I_{CL}	Clock Input Leakage Current			100	μA	V_ϕ = − 26V
	Data Input Capacitance		4		pF	V_ϕ = 0 V
	Clock Input Capacitance		20		pF	V_ϕ = 0 V
	Fan In			1		
	Fan Out			5		

TIMING DIAGRAM



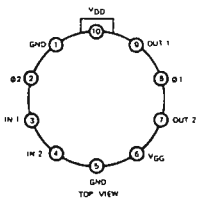
NOTE Delayed 25 Bit Times

dual 16-bit static shift register

EXTENDED TEMPERATURE RANGE - 55 °C + 85°C
STANDARD TEMPERATURE RANGE 0 + 70° C

The M 122 is a Dual 16-Bit Static Shift Register. It is a monolithic integrated circuit utilizing P-Channel Enhancement Mode MOS technology. It is designed to operate on a two phase clock in delay line or in serial binary or BCD data storage applications. For DC storage conditions, it is important that $\emptyset_1$ is a logic "0" and $\emptyset_2$ is a logic 1.

CONNECTION DIAGRAM



ABSOLUTE MAXIMUM RATINGS

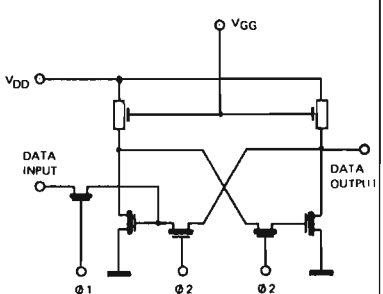
(above which the useful life may be impaired)

Drain Voltage (V_{DD})	- 30V to + 0.3V
Gate Voltage (V_{GG})	- 30V to + 0.3V
Clock and Data Input Voltages	- 30V to + 0.3V
Storage Temperature	- 55° C to + 150°C

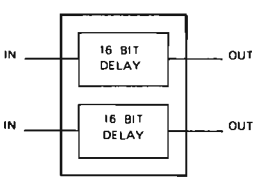
OPERATING CONDITIONS

Temperature range (Extended)	- 55 ÷ 85° C
Temperature range (Standard)	0 ÷ 70° C
Supply Voltage	V_{DD} = -13V ± 1V V_{GG} = -27V ± 1V

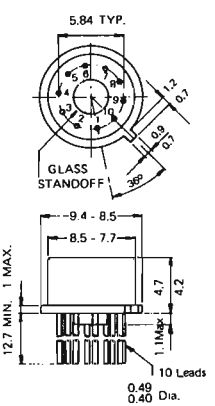
SCHEMATIC DIAGRAM
(one bit)



BLOCK DIAGRAM



PHYSICAL DIMENSIONS
similar to
JEDEC to 100 outline



Notes. All dimensions in mm.

ORDERING NUMBER

M 122 T1 (for standard temperature range)
M 122 T8 (for extended temperature range)

ELECTRICAL CHARACTERISTICS

V_{DD} = - 13 V ± 1V, V_{GG} = - 27 ± 1 V, Load = 10 MΩ and 10pF, T_A = - 55°C to 85°C or 0°C to 70°C according to the type No., unless otherwise specified.

CHARACTERISTICS	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Clock Repetition Rate	D.C.		1	MHz	
Clock Pulse widths $Ø_1$ pw $Ø_2$ pw	 0.4 0.4		 10 10	 μs μs	 See Figure 1 See Figure 1
Clock Delay (ø d)	0.01			μs	See Figure 1
Clock Pulse Rise and Fall Time (10% to 90%)			5	μs	See Figure 1
Clock Pulse Logic Levels ($ø_1$ & $ø_2$) Logic "0" Logic "1"	 -26		 - 2 -28	 V V	
Clock Pulse Input Capacitance ($ø_1$ & $ø_2$)		4		pF	$ø_1 = ø_2 = 0V$
Data Pulse Width (Dpw)	0.4			μs	
Data Input Capacitance		2		pF	V_{IN} = 0 Volt
Data Input Logic Levels Logic "0" Logic "1"	 - 9		 - 2 	 V V	
Data Input Leakage Current			1	μA	V_{IN} = - 20V
Clock Input Leakage Current			100	μA	V_{IN} = - 26V
Clock ($ø_2$) Input Impedance	60			KΩ	$ø_1$ = - 26V $ø_2$ = 0V
Output Logic Levels Logic "0" Logic "1"	 - 10	 - 0.5 - 11	 - 1 	 V V	
Output Impedance to Ground		2	3	KΩ	Output at Logic "0"
Output Drive Capability	- 5			V	R_L = 4 kΩ to Ground
Power Supply Current Drain V_{DD}			10	mA	V_{DD} = - 13V
Power Supply Current Drain V_{GG}			2	mA	V_{GG} = - 27V

TIMING DIAGRAMS

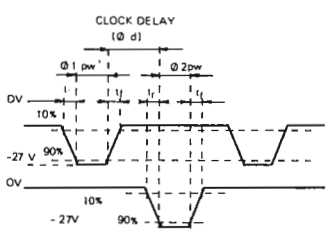


Figure 1

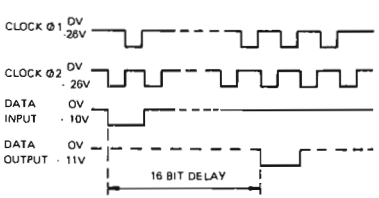


Figure 2

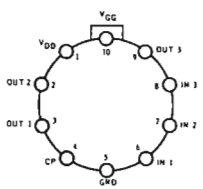
64 bit 1 ø static shift register

EXTENDED TEMPERATURE RANGE, -55°C + 85°C
STANDARD TEMPERATURE RANGE, 0°C + 70°C

- Single phase clock
- Low power consumption - less than 3 mW/bit
- High speed operation - DC to 1 MHz

The M 124 is a 64-bit 1 Ø static shift register arranged as a Dual 16, Single 32 in a TO-100 package. It is a monolithic integrated circuit utilizing P-channel Enhancement Mode Technology. Its main applications as delay line or bit storing device are in computer, data acquisition and data control systems, telemetry and peripheral equipments.

CONNECTION DIAGRAM
(Top view)



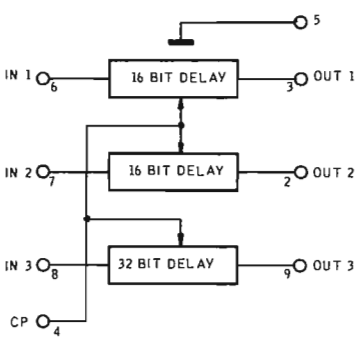
ABSOLUTE MAXIMUM RATINGS
(above which the useful life may be impaired)

Drain Voltage (V_{DD})	- 30V to + 0.3 V
Gate Voltage (V_{GG})	- 30V to + 0.3 V
Clock and Data Input Voltages	- 30V to + 0.3 V
Storage Temperature	- 55°C to +150°C

OPERATING CONDITIONS

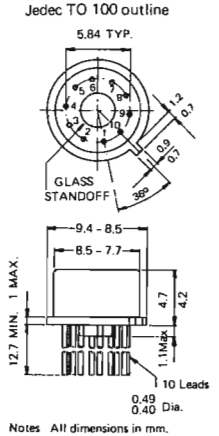
Supply Voltage	$V_{DD} = -13V \pm 1V$ $V_{GG} = -27V \pm 1V$
Temperature Range (extended)	-55°C to 85°C
Temperature Range (standard)	0°C to 70°C

BLOCK DIAGRAM



V_{GG} pin 10
V_{DD} pin 1
Gnd pin 5

PHYSICAL DIMENSIONS
similar to
Jedec TO 100 outline



Notes All dimensions in mm.

ORDERING NUMBER

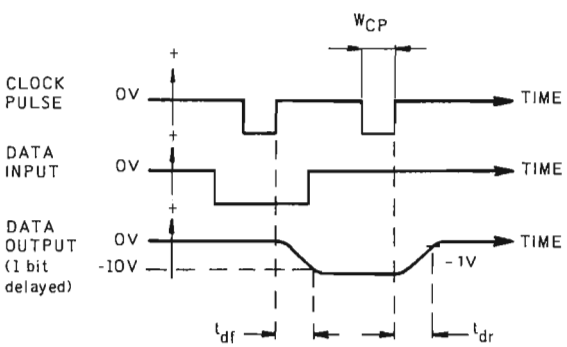
M 124 T8 (for extended temperature range)
M 124 T1 (for standard temperature range)

MAY 1969

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$, $V_{GG} = -27 \pm 1V$, $V_{DD} = +13 \pm 1V$, unless otherwise specified)

SYMBOL	CHARACTERISTICS		MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
	Power Consumption			200		mW	
	Operating Frequency		DC		1	MHz	$V_{GG} = -27$ V
V_{CP}	Clock Pulse Amplitude	"0" level			+2	V	
		"1" level	-9			V	
W_{CP}	Clock Pulse Width		0.3		100	µs	
	Clock Pulse Rise and Fall Time				10	µs	
	Clock Capacitance			8		pF	$V_{CP} = 0$ V
I_{CL}	Clock Leakage Current				±1	µA	$V_{CP} = -20$ V
V_{IL}	Input Amplitude	"0" level			+2	V	
V_{IH}		"1" level	-9			V	
C_{in}	Input Capacitance			2.5		pF	$V_{in} = 0$ V
I_{IL}	Input Leakage Current				±1	µA	$V_{in} = -20$ V
V_{OL}	Output Levels	"0" level			+1	V	$I_{OUT} = -10$ µA
V_{OH}		"1" level	-10			V	$I_{OUT} = -10$ µA
t_{df}	Time Delay Fall			0.4	0.5	µs	$V_{GG} = -27$ V
t_{dr}	Time Delay-Rise			0.4	0.5	µs	$V_{GG} = -27$ V

TIMING DIAGRAM



Dual 256-bit dynamic shift register

STANDARD TEMPERATURE RANGE
0°C to 70°C

- INPUT GATE PROTECTION
- TTL DRIVE CAPABILITY
- ON-CHIP RECIRCULATING LOGIC

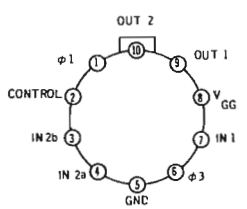
M125 consists of two separate 256-bit dynamic shift registers with independent input and output terminals, while clocks, power and ground are common. One power supply and two external clocks are required for operation with two further clocks generated internally. The entire device is constructed on a single monolithic chip using MOS P-channel technology. One section incorporates recirculating logic for application as an accumulator. The two sections could be cascaded to have a 512-bit serial accumulator. Input data should be stable from the leading edge of ϕ 1 to the leading edge of ϕ 3; while output data starts changing with the leading edge of ϕ 3. The control input allows the device to accept data from either the 2a or 2b inputs.

ABSOLUTE MAXIMUM RATINGS

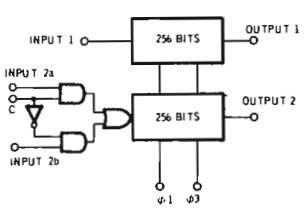
Input Voltage	-30V to +0.3V
Clock Voltage	-30V to +0.3V
Supply Voltage	-30V to +0.3V
Storage Temperature Range	-55°C to 150°C

ORDERING NUMBER
M125 T1

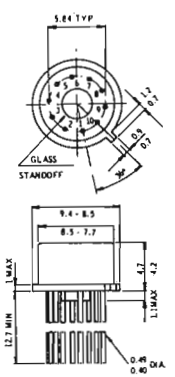
CONNECTION DIAGRAM
(top view)



LOGIC DIAGRAM



PHYSICAL DIMENSIONS
in accordance with
JEDEC TO-100



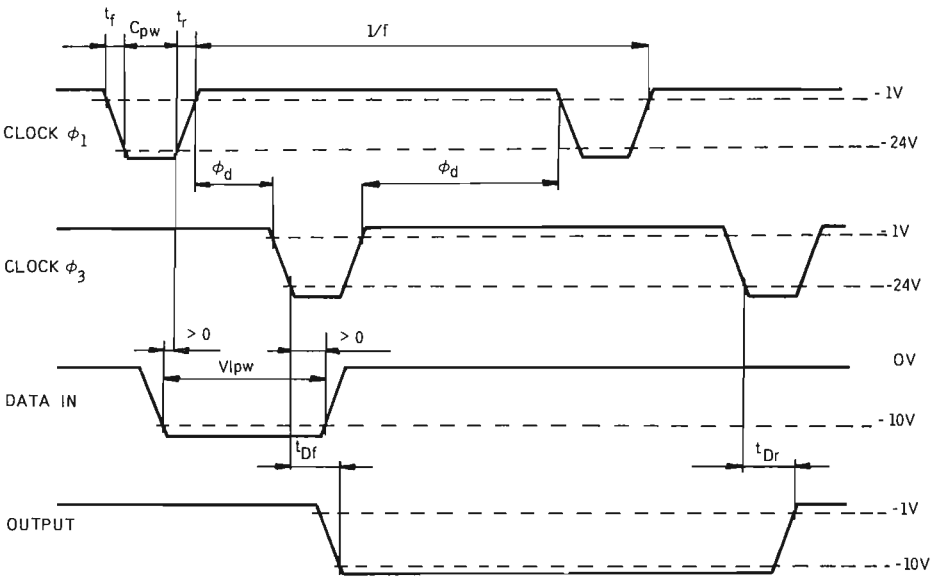
Note : all dimensions in mm.

ELECTRICAL CHARACTERISTICS

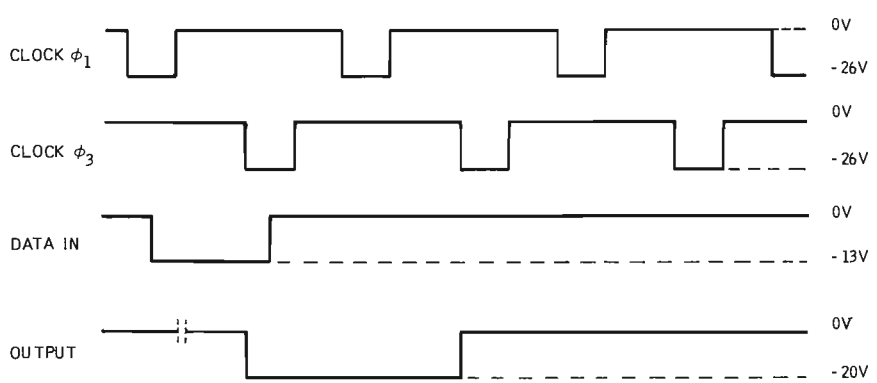
(T_A = 25°C; V_{GG} = - 27V ± 1V; load = 10M Ω and 10 pF unless otherwise noted)

SYMBOL	CHARACTERISTIC	Min.	Typ.	Max.	Unit	TEST CONDITIONS
	CLOCK PULSES					
f	Repetition Rate Range	10		1000	kHz	
C_{pw}	Pulse Width	0.15			μsec	See Fig. 1
Ø d	Pulse Separation	0.2			μsec	See Fig. 1
V_{ILcp}	"O" Level Voltage			- 1	V	
V_{IHcp}	"1" Level Voltage	-25			V	
C_{cp}	Input Capacitance		120		pF	V = 0 f = 1 MHz
$I_{L\,cp}$	Leakage Current			1	μA	V_{cp} = - 27V
	DATA INPUT AND CONTROL INPUT					
V_{IL}	"O" Level Voltage			- 2	V	
V_{IH}	"1" Level Voltage	-10			V	
C_{in}	Input Capacitance		3		pF	V = 0 f = 1 MHz
I_L	Leakage Current			1	μA	V_{in} =-20V
	DATA OUTPUT					
V_{OL}	"O" Level Voltage		-0.5	- 1	V	I_{OL} =-10 μA
V_{OH}	"1" Level Voltage	-11			V	I_{OH} = -10 μA
R_{on}	"O" Level On Resistance			6	k Ω	
R_{on}	"1" Level On Resistance			6	k Ω	
	POWER CONSUMPTION					
I_{GG}	Gate Current		3.5	6	mA	V_{GG}= -27V f = 1 MHz
	RESPONSE TIME					
t_{Df}	Delay Time to Fall		100	150	nsec	See Fig. 1
t_{Df}	Delay Time to Rise		300	350	nsec	See Fig. 1

WAVEFORMS (Fig. 1)

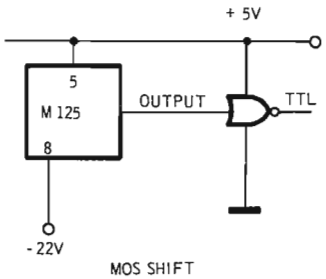


TYPICAL TIMING DIAGRAM

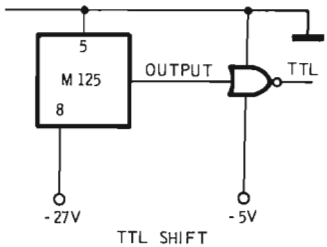


TYPICAL INTERFACE CIRCUITS

TTL DRIVE

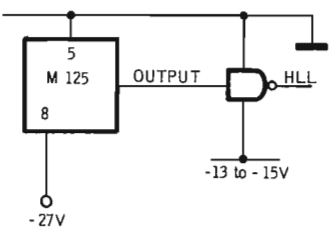


MOS SHIFT

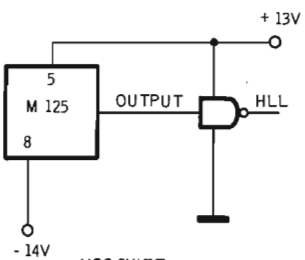


TTL SHIFT

HLL DRIVE

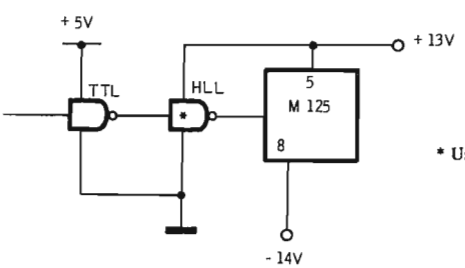


HLL SHIFT



MOS SHIFT

MOS DRIVE



* Use H114 HLL device for TTL interface

STANDARD TEMPERATURE RANGE
0°C to 70°C

Dual 100-bit static shift register

- INPUT GATE PROTECTION
- TTL DRIVE CAPABILITY
- HIGH SPEED (1 MHz)
- STATIC OPERATION

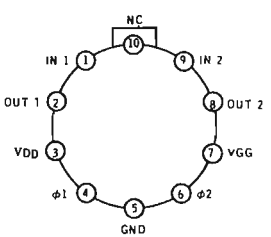
The M 127 consists of two separate 100-bit static shift registers with independent input and output terminals, and common clocks, power, and ground. Two power supplies and two external clocks are required for operation with a third clock generated internally. The entire device is constructed on a single monolithic chip using MOS P-channel technology. Transferring data into the register is accomplished when the ϕ 1 clock is at a logical 1. Shifting the data occurs when the ϕ 1 clock is momentarily pulsed to logical 1 and the ϕ 2 clock to logical 0. For long term data storage, the ϕ 1 clock must be held at logical 0 and ϕ 2 clock must be held at logic "1". Output data appears on the negative-going edge of the ϕ 2 clock pulse. Output low impedance allows direct drive of TTL gates.

ORDERING NUMBER
M 127 T1

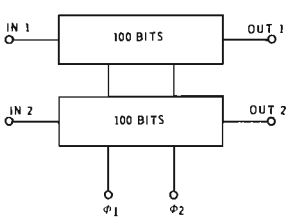
ABSOLUTE MAXIMUM RATINGS

Input Voltage	-30V to 0.3V
Clock Voltage	-30V to 0.3V
Supply Voltage	-30V to 0.3V
Storage Temperature Range	-55°C to 150°C

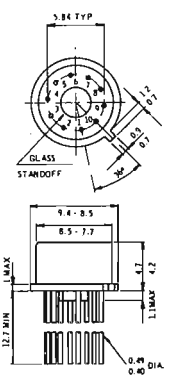
CONNECTION DIAGRAM
(Top view)



LOGIC DIAGRAM



PHYSICAL DIMENSIONS
in accordance with
JEDEC TO-100

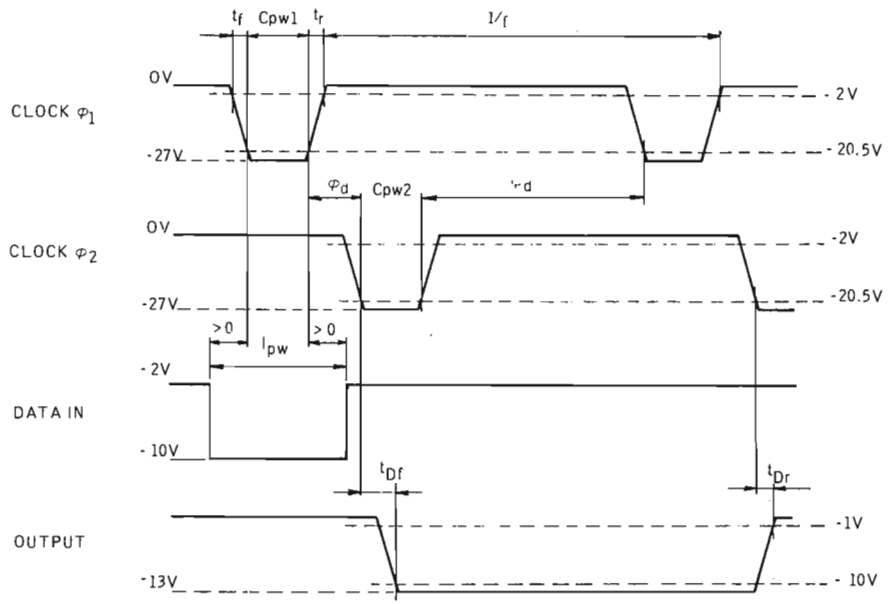


Note : all dimensions in mm.

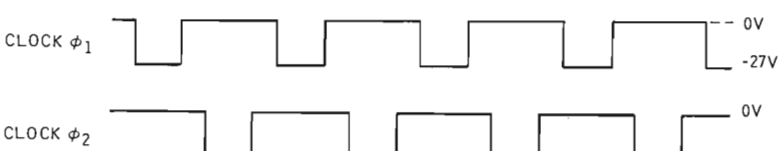
ELECTRICAL CHARACTERISTICS :
(T_A = 0°C to 70°C; V_{DD} = -13V ± 1V; V_{GG} = -27V ± 1V; Load = 10MΩ and 10pF unless otherwise noted)

SYMBOL	CHARACTERISTIC	Min.	Typ.	Max.	Unit	TEST CONDITIONS
	CLOCK PULSES					
f	Repetition Rate Range	0		1	MHz	
C_{pw1}	Pulse Width Ø 1	0.4		10	µsec	T_A = 25°C see waveforms
C_{pw2}	Pulse Width Ø 2	0.4			µsec	
Ø d	Pulse Separation	0.01		10	µsec	
t_r , tf	Rise and Fall Time			5	µsec	
V_{ILcp}	"0" Level Voltage			-2	V	
V_{IHcp}	"1" Level Voltage	- 26			V	
I_{Lcp}	Leakage Current			-50	µA	V = -28V
C_{cp}	Input Capacitance		28	33	pF	V = 0 T_A = 25°C f=1MHz
	DATA INPUT					
V_{IL}	"0" Level Voltage			- 2	V	
V_{IH}	"1" Level Voltage	- 9			V	
V_{Ipw}	Pulse Width	0.4			µsec	see waveforms
I_L	Leakage Current			- 1	µA	V = - 20V
C_{in}	Input Capacitance		3	5	pF	V=0 T_A=25°C f=1MHz
	DATA OUTPUT					
V_{OL}	"0" Level Voltage		-0.3	- 1	V	
V_{OL1}	"0" Level Voltage		-1	- 2	V	I_{OL1} = - 60µA
V_{OH}	"1" Level Voltage	- 10	-12		V	
V_{OH1}	"1" Level Voltage		-10.5		V	I_{OH} = 400 µA
V_{OH2}	"1" Level Voltage	-4.8			V	I_{OH} = 1.6 mA
	RESPONSE TIME					
t_{Dr}	Delay Time to Rise		300	400	nsec	T_A = 25°C see waveforms
t_{Df}	Delay Time to Fall		300	400	nsec	
	POWER CONSUMPTION					
I_{DD}	Drain Current		-18	-25	mA	V_{DD}=-14V V_{GG}=-28V
I_{GG}	Gate Current		-1.5	-2.9	mA	V_{DD}=-14V V_{GG}=-28V

WAVEFORMS

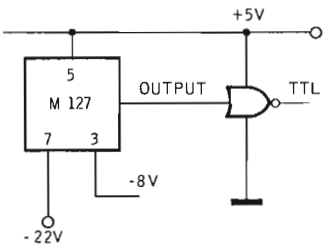


TYPICAL TIMING DIAGRAM

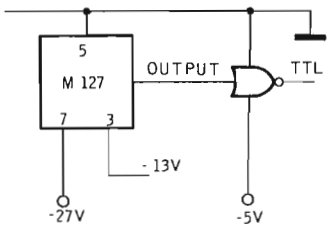


TYPICAL INTERFACE CIRCUITS

TTL DRIVE

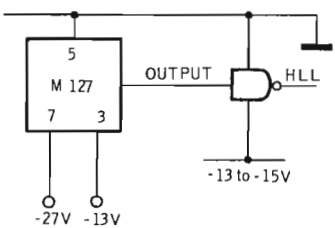


MOS SHIFT

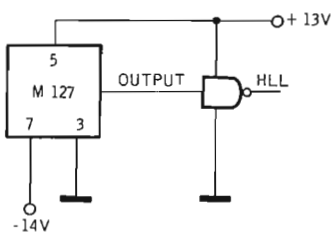


TTL SHIFT

HLL DRIVE

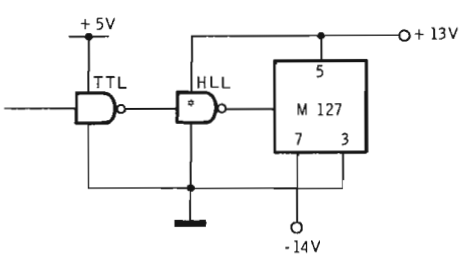


HLL SHIFT



MOS SHIFT

MOS DRIVE



* Use H 114 HLL device for TTL interface

Triple 64-bit dynamic shift register

STANDARD TEMPERATURE RANGE
0° C to 70° C

- FULLY TTL COMPATIBLE ON OUTPUT
- HIGH FREQUENCY : 1KHz to 6MHz
- INPUT GATE PROTECTION

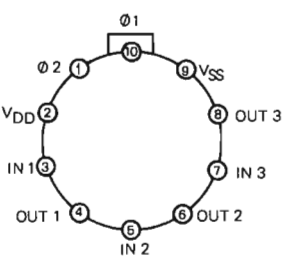
The M 128 consists of 3 separate 64-bit dynamic shift registers with independent input and output terminals, while clocks, power and ground are common. One power supply and two external clocks are required for operation. The entire device is constructed on a single monolithic chip using MOS P-channel technology. The 3 sections could be cascaded to have a 192-bit serial accumulator. Transferring data into the register is accomplished when the clock ϕ_1 is at logical 1. Shifting of data occurs when the ϕ_2 clock is momentarily pulsed to a logic 1 and clock ϕ_1 to a logic 0. Ouptut data appears on the negative going edge of the clock ϕ_2. Output low impedance allows direct drive of TTL gates.

ORDERING NUMBER
M 128 T1

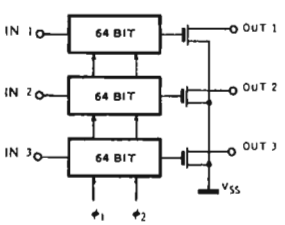
ABSOLUTE MAXIMUM RATINGS

Input Voltage	-30V to +0.3V
Clock Voltage	-30V to +0.3V
Supply Voltage	-30V to +0.3V
Storage Temperature Range	-55°C to +150°C
Operating Temperature Range	0°C to +70°C

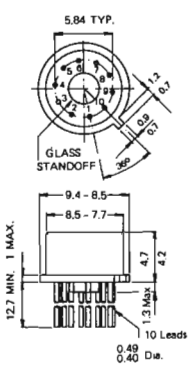
CONNECTION DIAGRAM
(Top view)



LOGIC DIAGRAM



PHYSICAL DIMENSIONS
in accordance with
JEDEC TO-100 outline



Note : All dimensions in mm.

ELECTRICAL CHARACTERISTICS :
(T_A=0°C to 70°C; V_{DD} = -13V ± 1V; Load = 10 MΩ /10pF; unless otherwise noted)

SYMBOL	CHARACTERISTIC	Min.	Typ.	Max.	Unit	TEST CONDITIONS
	CLOCK PULSES					
f_{min}	Minimum Repetition Rate	1			KHz	C_{pw} = 250 µsec ϕ_d = 250 µsec
f_{max}	Maximum Repetition Rate			6	MHz	C_p duty cycle = 35%
						$V_{IH_{cp}}$ = -26V $t_r = t_f$ = 10 nsec
C_{pw}	Pulse Width	0.06		250	µsec	see fig. 1
V_{OV}	Overlap Voltage			-3	V	see fig. 2
ϕ_d	Clock Delay			250	µsec	see fig. 1
t_r - t_f	Rise and Fall Time			5	µsec	see fig. 1
$V_{IL_{cp}}$	"0" Level Voltage	0	- 1.5	- 2.5	V	
$V_{IH_{cp}}$	"1" Level Voltage	- 20	- 26	- 30	V	
C_{cp}	Input Capacitance		50	60	pF	V = 0V
$I_{L_{cp}}$	Leakage Current			1	µA	V_{DD} = 0V $V_{\phi 1}$=$V_{\phi 2}$= - 28V
	DATA INPUT					
V_{IL}	"0" Level Voltage			- 2.5	V	
V_{IH}	"1" Level Voltage	- 8			V	
C_{IN}	Input Capacitance		3	4	pF	V_{IN} = 0V
I_L	Input Leakage Current			1	µA	V_{IN} = - 28V
$t_{set\text{-}up}$	Set-Up Time	0.06			µsec	see fig. 1
t_{hold}	Hold Time	0.01			µsec	see fig. 1
	DATA OUTPUT					
V_{OL}	"0" Level Voltage		- 1	- 2	V	V_A = -14V R_L = 10KΩ
V_{OH}	"1" Level Voltage	- 12	- 13		V	V_A = -14V R_L = 10KΩ
R_{ON}	Output "On" Resistance		0.7	1.5	KΩ	V_{OUT} = 0V to -3V
I_L	Output Leakage Current			1	µA	V_{OUT} = - 28V
	RESPONSE TIME @ T_A = 25°C					
t_{dfl}	Delay Time to Fall-MOS Load			160	nsec	R_L = 10KΩ V_A = -14V C_L = 20pF (see fig. 1)
t_{drl}	Delay Time to Rise-MOS Load		70	80	nsec	R_L = 10KΩ V_A = -14V C_L = 20pF (see fig. 1)
t_{dfl}	Delay Time to Fall-TTL Load		45	60	nsec	R_L = 3.9KΩ V_A = -14V C_L = 20pF (see fig. 1)
t_{drl}	Delay Time to Rise-TTL Load		25	40	nsec	R_L = 3.9KΩ V_A = -14V C_L = 20pF (see fig. 1)
	POWER CONSUMPTION					
I_{DD}	Drain Current		15	18	mA	V_{DD} = -14V C_p duty cycle = 25% f = 6MHz

WAVEFORMS

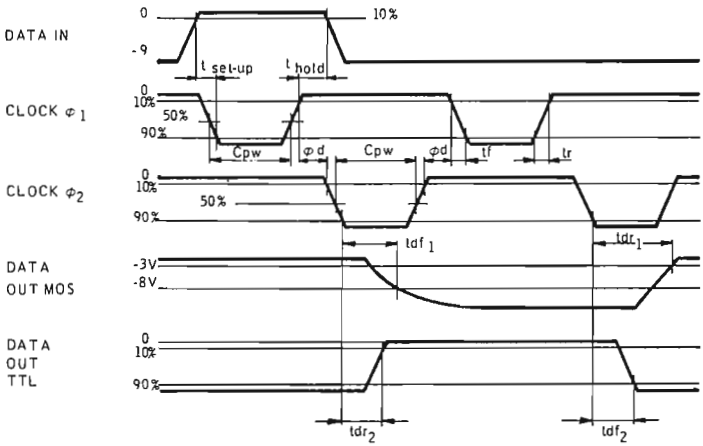


FIG. 1

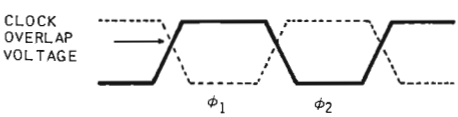
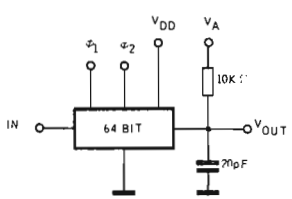
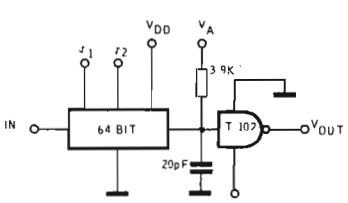


FIG. 2

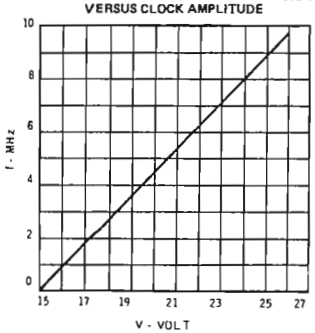
MOS LOAD TEST CIRCUIT



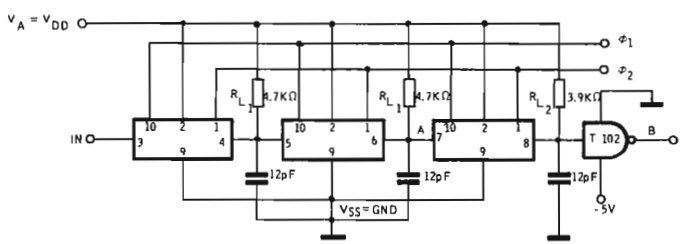
TTL LOAD TEST CIRCUIT

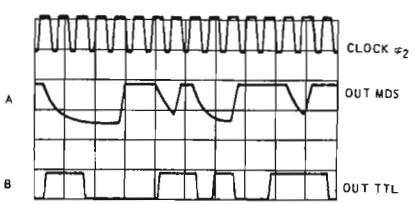


TYPICAL MAX FREQUENCY OF OPERATION VERSUS CLOCK AMPLITUDE



8 MHz OPERATION MEASUREMENT CIRCUIT





A = WAVE FORM WITH MOS-TO-MOS CONNECTION
B = WAVE FORM WITH MOS-TO-TTL CONNECTION

$V_{IN(1)} = -10V$
$V_{\Phi_1(1)} = V_{\Phi_2(1)} = -26V$
$V_{\Phi_1(0)} = V_{\Phi_2(0)} = -2V$
$V_{DD} = -14V$
$R_{L_1} = 4.7K\Omega$
$R_{L_2} = 3.9K\Omega$

$0°C < T_A < 70°C$
200 nsec/cm Horizontal
CLOCK 20V/cm
OUT MOS 10V/cm } Vertical
OUT TTL 5V/cm

Triple 66-bit dynamic shift register

STANDARD TEMPERATURE RANGE
0°C.to 70°C

- FULLY TTL COMPATIBLE ON OUTPUT
- HIGH FREQUENCY : 1KHz to 6MHz
- INPUT GATE PROTECTION

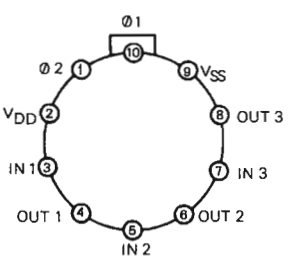
The M 129 consists of 3 separate 66-bit dynamic shift registers with independent input and output terminals, while clocks, power and ground are common. One power supply and two external clocks are required for operation. The entire device is constructed on a single monolithic chip using MOS P-channel technology. The 3 sections could be cascaded to have a 198-bit serial accumulator. Transferring data into the register is accomplished when the clock Φ_1 is at logical 1. Shifting of data occurs when the Φ_2 clock is momentarily pulsed to a logic 1 and clock Φ_1 to a logic 0. Ouptut data appears on the negative going edge of the clock Φ_2. Output low impedance allows direct drive of TTL gates.

ORDERING NUMBER
M 129 T1

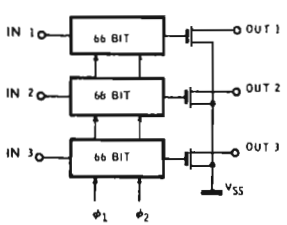
ABSOLUTE MAXIMUM RATINGS

Input Voltage	-30V to +0.3V
Clock Voltage	-30V to +0.3V
Supply Voltage	-30V to +0.3V
Storage Temperature Range	-55°C to +150°C
Operating Temperature Range	0°C to +70°C

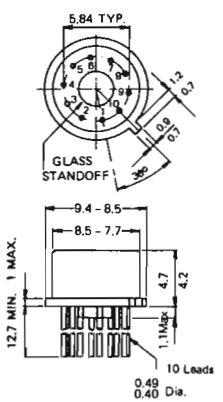
CONNECTION DIAGRAM
(Top view)



LOGIC DIAGRAM



PHYSICAL DIMENSIONS
in accordance with
JEDEC TO-100 outline



Note : All dimensions in mm.

ELECTRICAL CHARACTERISTICS :
(T_A=0°C to 70°C; V_{DD} = -13V ± 1V; Load = 10 MΩ / 10pF; unless otherwise noted)

SYMBOL	CHARACTERISTIC	Min.	Typ.	Max.	Unit	TEST CONDITIONS
	CLOCK PULSES					
f_{min}	Minimum Repetition Rate	1			KHz	C_{pw} = 250 µsec ϕ_d = 250 µsec
f_{max}	Maximum Repetition Rate			6	MHz	C_p duty cycle = 35%
						$V_{IH_{cp}}$ = -26V $t_r = t_f$ = 10 nsec
C_{pw}	Pulse Width	0.06		250	µsec	see fig. 1
V_{OV}	Overlap Voltage			-3	V	see fig. 2
ϕ_d	Clock Delay			250	µsec	see fig. 1
t_r - t_f	Rise and Fall Time			5	µsec	see fig. 1
$V_{IL_{cp}}$	"0" Level Voltage	0	- 1.5	- 2.5	V	
$V_{IH_{cp}}$	"1" Level Voltage	- 20	- 26	- 30	V	
C_{cp}	Input Capacitance		50	60	pF	V = 0V
$I_{L_{cp}}$	Leakage Current			1	µA	V_{DD} = 0V $V_{\phi 1}=V_{\phi 2}$ = - 28V
	DATA INPUT					
V_{IL}	"0" Level Voltage			- 2.5	V	
V_{IH}	"1" Level Voltage	- 8			V	
C_{IN}	Input Capacitance		3	4	pF	V_{IN} = 0V
I_L	Input Leakage Current			1	µA	V_{IN} = - 28V
$t_{set\text{-}up}$	Set-Up Time	0.06			µsec	see fig. 1
t_{hold}	Hold Time	0.01			µsec	see fig. 1
	DATA OUTPUT					
V_{OL}	"0" Level Voltage		- 1	- 2	V	V_A = -14V R_L = 10KΩ
V_{OH}	"1" Level Voltage	- 12	- 13		V	V_A = -14V R_L = 10KΩ
R_{ON}	Output "On" Resistance		0.7	1.5	KΩ	V_{OUT} = 0V to -3V
I_L	Output Leakage Current			1	µA	V_{OUT} = - 28V
	RESPONSE TIME @ T_A = 25°C					
t_{df1}	Delay Time to Fall-MOS Load			160	nsec	R_L = 10KΩ V_A = -14V
						C_L = 20pF (see fig. 1)
t_{dr1}	Delay Time to Rise-MOS Load		70	80	nsec	R_L = 10KΩ V_A = -14V
						C_L = 20pF (see fig. 1)
t_{df1}	Delay Time to Fall-TTL Load		45	60	nsec	R_L = 3.9KΩ V_A = -14V
						C_L = 20pF (see fig. 1)
t_{dr1}	Delay Time to Rise-TTL Load		25	40	nsec	R_L = 3.9KΩ V_A = -14V
						C_L = 20pF (see fig. 1)
	POWER CONSUMPTION					
I_{DD}	Drain Current		15	18	mA	V_{DD} = -14V C_p duty cycle = 25% f = 6MHz

WAVEFORMS

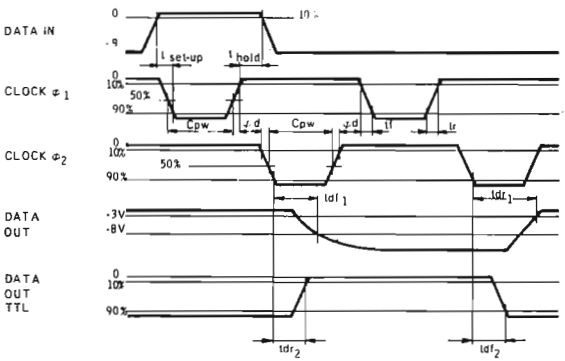


FIG. 1

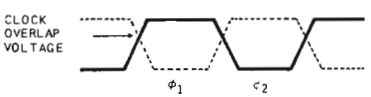
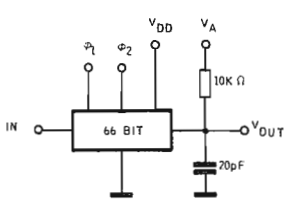
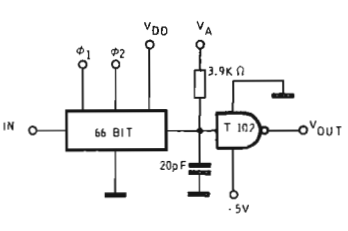


FIG. 2

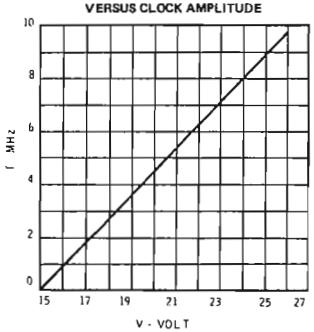
MOS LOAD TEST CIRCUIT



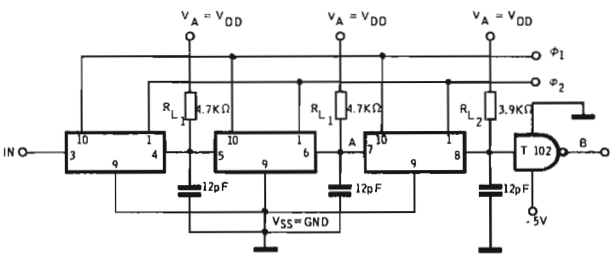
TTL LOAD TEST CIRCUIT

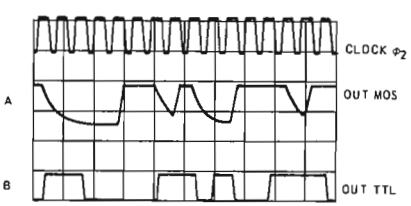


TYPICAL MAX FREQUENCY OF OPERATION VERSUS CLOCK AMPLITUDE



8 MHz OPERATION MEASUREMENT CIRCUIT





V_{IN} = -10V

$V_{\phi_1(1)} = V_{\phi_2(1)}$ = -26V

$V_{\phi_1(0)} = V_{\phi_2(0)}$ = -2V

V_{DD} = -14V

R_{L_1} = 4.7KΩ

R_{L_2} = 3.9K Ω

0°C < T_A ≤ 70°C

200 nsec/cm

CLOCK 20V/cm

OUT MOS 10V/cm

OUT TTL 5V/cm

A = WAVE FORM WITH MOS-TO-MOS CONNECTION

B = WAVE FORM WITH MOS-TO-TTL CONNECTION

1024-bit dynamic shift register

STANDARD TEMPERATURE RANGE
0°C ÷ 70°C

- HIGH FREQUENCY OPERATION : 10 MHz
- LOW POWER DISSIPATION : 60 μW/bit @ 1 MHz
- DTL, TTL COMPATIBLE
- INPUT GATE PROTECTION

The M 130 is a 1024-bit dynamic shift register using low threshold silicon gate technology, which allows high speed (8 MHz guaranteed) while reducing power dissipation compared to conventional technologies. The registers can be driven directly by standard integrated circuits (TTL, DTL, etc.) or by MOS circuits. The circuit design makes the M 130 very popular in applications such as low cost memory and delay line.

ABSOLUTE MAXIMUM RATINGS
(above which the useful life may be impaired)

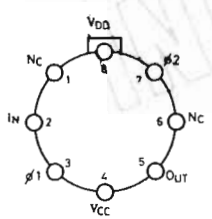
Input Voltage (1)	-17 to 0.3 V
Clock Voltage (1)	-17 to 0.3 V
Supply Voltage (1)	-17 to 0.3 V
Storage Temperature Range	-65°C ÷ 150°C

ORDERING NUMBER

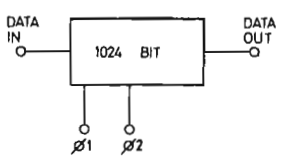
M 130 T1

(1) This voltage is with respect to the V_{CC} pin voltage.

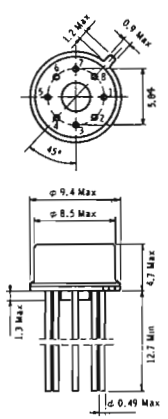
CONNECTION DIAGRAM
(top view)



LOGIC DIAGRAM



PHYSICAL DIMENSIONS



Note : all dimensions in mm.

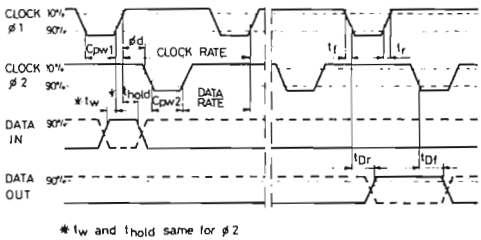
ELECTRICAL CHARACTERISTICS (T_A = 0°C to 70°C; V_{CC} = 5V ± 5%; V_{DD} = -5V ± 5%; unless otherwise noted)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
	CLOCK PULSES					
C_{pw}	Pulse Width		90		ns	see timing diagram
ϕd	Pulse Delay		10		ns	see timing diagram
t_r, t_f	Pulse Transition			1000	ns	
V_{IHcp}	"1" Level Voltage	V_{CC} - 1		V_{CC}+0.3	V	
V_{ILcp}	"0" Level Voltage	V_{CC} -17		V_{CC}-15	V	
I_{Lcp}	Leakage Current		0.1	1	μA	V_{ILcp}-V_{CC}=-14V T_A = 25°C (*)
C_{cp}	Clock Capacitance		135÷150		pF	V =0V at 1 MHz
	DATA INPUT					
f_{min}	Min. Data Rate		100		Hz	C_{pw} = 100 μs R_L = 3 KΩ V_{in} = 0 ÷ -4V V_{ILcp}=0÷-14V V_{DD} = -10V
f_{max}	Max. Data Rate	8	10		MHz	C_{pw} = 50 ns R_L = 3 KΩ V_{in} = 0 ÷ -4V V_{ILcp}=0÷-14V V_{DD} = -10V V_{CC} = 0
V_{IH}	"1" Level Voltage		V_{CC} -1.7÷0.3		V	
V_{IL}	"0" Level Voltage		V_{CC} -4.2÷-10		V	
I_{Li}	Input Leakage Current		0.01	500	nA	V_{in} = -14V T_A = 25°C (*)
C_{in}	Input Capacitance		3 ÷ 3.5		pF	V = 0 V at 1 MHz
	DATA OUTPUT					
V_{OL}	"0" Level Voltage	-3		+0.5	V	R_L = 3 KΩ I_L = 1.6 mA
V_{OH1}	"1" Level Voltage Driving MOS	V_{CC}-1.6			V	R_L = 4.7 KΩ C_L=10pF 35% d.c.
V_{OH2}	"1" Level Voltage Driving TTL	V_{CC}-2.4			V	R_L = 3 KΩ I_L=100μA 35% d.c.
I_{Lo}	Output Leakage Current		0.01	1000	nA	V_{OUT}=-14V T_A=25°C (*)
	SWITCHING TIME					
t_{Dr}, t_{Df}	Delay Time to Rise and to Fall		60		ns	
t_{hold}	Input Hold Time	60			ns	
t_w	Data Write Time (set-up)		30		ns	
	POWER CONSUMPTION					
I_{DD}	Drain Supply Current		25	35	mA	output at logic "0" 25 KHz data rate 35% duty cycle (Note 1) R_L = 3 KΩ V_{DD} = -10V V_{ILcp}= 0÷-14V V_{CC} = 0

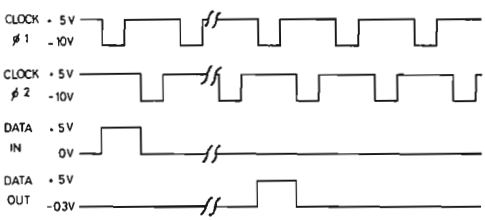
(*) All other pins grounded.

Note 1 : T is understood as measured half way between high and low level.

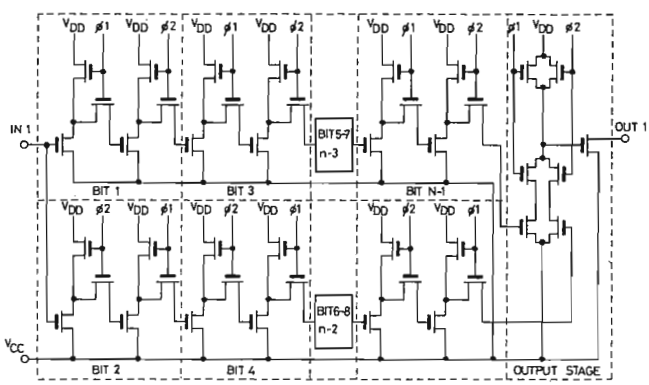
WAVEFORMS



TIMING DIAGRAM

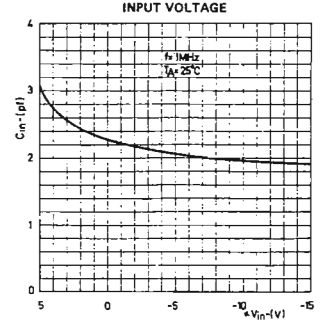


CIRCUIT SCHEMATIC

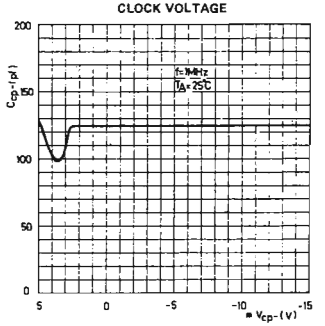


TYPICAL ELECTRICAL CHARACTERISTICS

INPUT CAPACITANCE VERSUS INPUT VOLTAGE

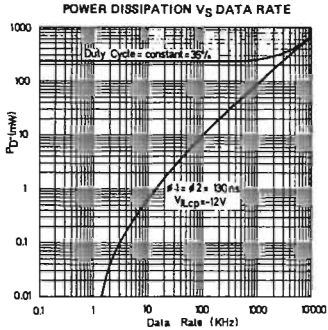


CLOCK CAPACITANCE VERSUS CLOCK VOLTAGE

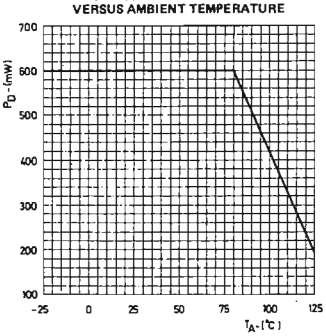


• These voltages are with respect to V_{CC} voltage

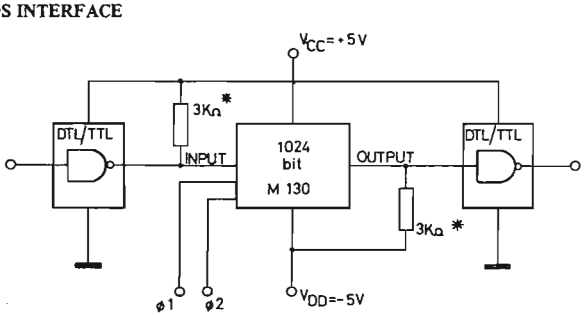
POWER DISSIPATION V_S DATA RATE



MAXIMUM PACKAGE POWER DISSIPATION VERSUS AMBIENT TEMPERATURE



TYPICAL DTL/TTL/MOS INTERFACE



* All resistors 3KΩ 5%

Dual 64-bit fully DC shift register

EXTENDED TEMPERATURE RANGE
-55°C to 125°C
STANDARD TEMPERATURE RANGE
0°C to 70°C

- FULLY TTL COMPATIBLE
- DC TO 2MHz OPERATION
- SINGLE PHASE CLOCK
- INPUT GATE PROTECTION

The M 137 consists of 2 separate 64-bit shift registers with independent input and output terminals and common single phase clock. Data inputs and clock can be driven directly from DTL/TTL levels and the outputs can drive DTL/TTL directly. The entire device is constructed on a single monolithic chip utilizing nitride-Planox technology. Transferring data into the register is accomplished while the clock is low and output data appears on the positive going edge of the clock.

ABSOLUTE MAXIMUM RATINGS
(above which the useful life may be impaired)

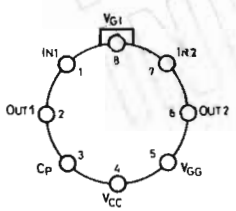
Input Voltage (1)	-20 to +0.3V
Clock Voltage (1)	-20 to +0.3V
Supply Voltage (1)	-20 to +0.3V
Storage Temperature Range	-65°C to 150°C

ORDERING NUMBER

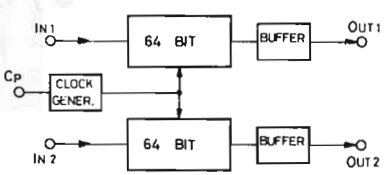
M 137 T1 (for Standard Temperature Range)
M 137 T2 (for Extended Temperature Range)

Note 1 With respect to V_{CC}

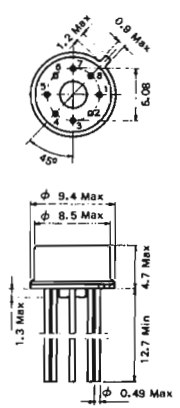
CONNECTION DIAGRAM
(top view)



LOGIC DIAGRAM



PHYSICAL DIMENSIONS
in accordance with
JEDEC TO-99 outline

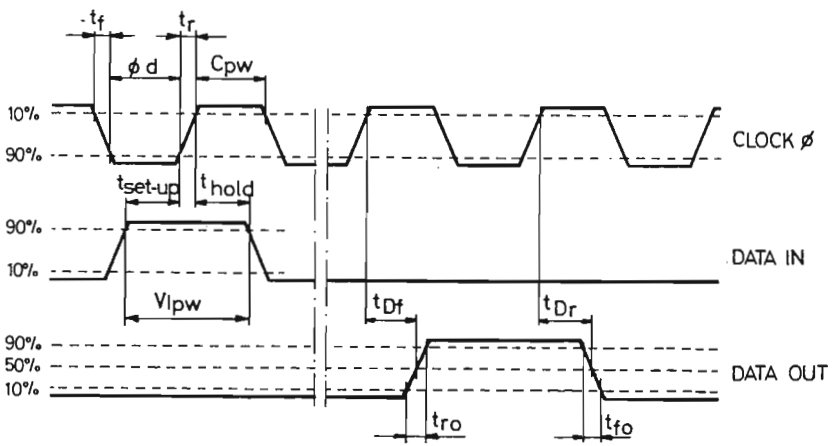


Note: all dimensions in mm.

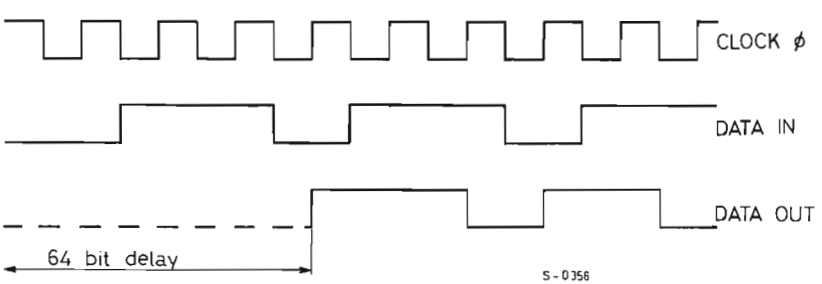
ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 0.5V; V_{GI} = GND; V_{GG} = -12V ± 1V; unless otherwise noted)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
	CLOCK PULSES					
f	Repetition Rate Range	0		2	MHz	
C_{pw}	Pulse Width	200			ns	
ϕd	Pulse Separation	200			ns	
t_r,t_f	Rise and Fall Time			1	μs	f = 100 kHz
V_{ILcp}	"0" Level Voltage			V_{CC}-4.2	V	
V_{IHcp}	"1" Level Voltage	V_{CC}-1.5			V	
I_{Lcp}	Leakage Current			1	μA	$V_{cp}=V_{CC}$ - 15V T_A = 25°C
C_{cp}	Input Capacitance			15	pF	$V_{cp}=V_{CC}$ f = 1 MHz
	DATA INPUT					
V_{IL}	"0" Level Voltage			V_{CC}-4.2	V	
V_{IH}	"1" Level Voltage	V_{CC}-1.5			V	
V_{Ipw}	Pulse Width	250			ns	T_A = 25°C f = 2 MHz
I_L	Leakage Current			1	μA	$V_{in}=V_{CC}$-15V T_A = 25°C
C_{in}	Input Capacitance			5	pF	$V_{in}=V_{CC}$ T_A=25°C f=1MHz
t_{set-up}	Set-up Time		100		ns	see waveforms
t_{hold}	Hold Time		150		ns	see waveforms
	DATA OUTPUT					
V_{OL}	"0" Level Voltage			0.4	V	load = 10 pF I_{sink} = 1.6 mA
V_{OH}	"1" Level Voltage	V_{CC} - 1			V	I_{OH} = 100 μA
t_{ro}	Rise Time		60		ns	T_A = 25°C see waveforms
t_{fo}	Fall Time		90		ns	T_A = 25°C see waveforms
	SWITCHING TIME					
t_{Dr}	Delay Time to Rise		300		ns	T_A = 25°C see waveforms
t_{Df}	Delay Time to Fall		300		ns	T_A = 25°C see waveforms
	POWER CONSUMPTION					
I_{GG}	Gate Supply Current		13		mA	
P_D	Total Power Consumption		220		mW	nominal power supply

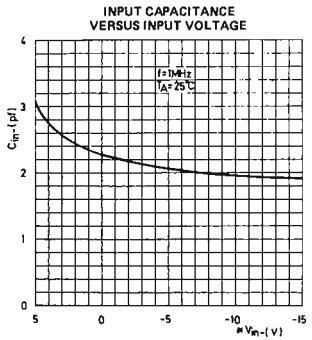
WAVEFORMS

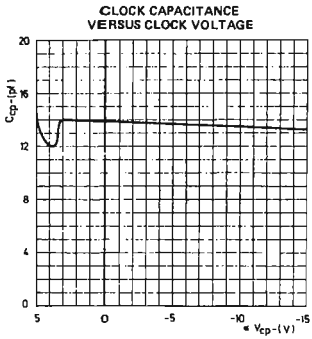


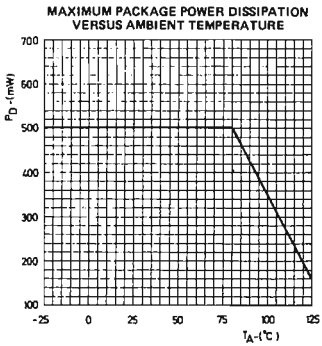
TYPICAL TIMING DIAGRAM



TYPICAL ELECTRICAL CHARACTERISTICS

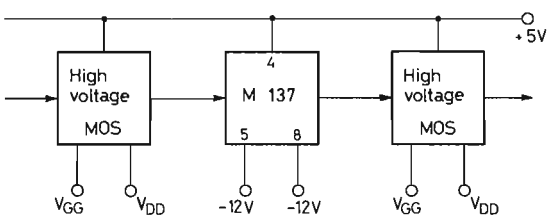


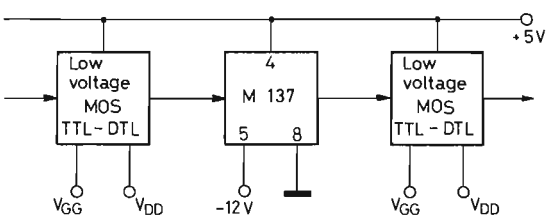




* Note : These voltages are with respect to V_{CC} pin voltage

TYPICAL INTERFACE CIRCUITS





Quad 40-bit dynamic shift register

STANDARD TEMPERATURE RANGE
0°C to 70°C

- LOW THRESHOLD TECHNOLOGY
- INPUT AND OUTPUT TTL COMPATIBLE
- LOW POWER DISSIPATION
- INPUT GATE PROTECTION
- 2MHz OPERATION GUARANTEED

The M 139 consists of 4 separate 40-bit dynamic shift registers with independent input and output terminals, while clocks, power and ground are common. The entire device is constructed on a single monolithic chip using silicon nitride-Planox, P-channel technology. The 4 sections could be cascated to have a 160-bit serial shift register. Shifting of data occurs when the $\phi 2$ clock is momentarily pulsed to a logic "1" and clock $\phi 1$ to a logic "0". Output data appears on the negative going edge of the clock $\phi 2$. Output low impedance allows direct drive of TTL gates.

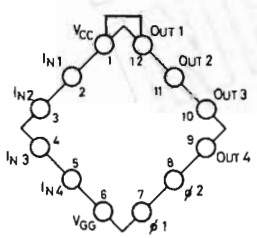
ABSOLUTE MAXIMUM RATINGS
(above which the useful life may be impaired)

Input Voltage (1)	-20V to 0.3V
Clock Voltage (1)	-20V to 0.3V
Supply Voltage (1)	-20V to 0.3V
Storage Temperature Range	-55°C to 150°C

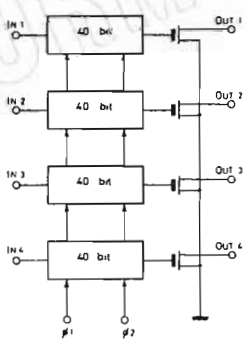
ORDERING NUMBER
M 139 T1

Note 1: this voltage is with respect to the V_{CC} pin voltage

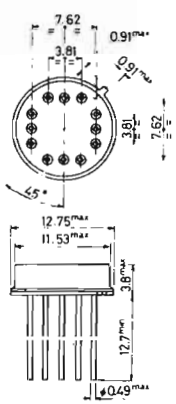
CONNECTION DIAGRAM



BLOCK DIAGRAM



PHYSICAL DIMENSIONS
TO-8



ELECTRICAL CHARACTERISTICS (T_A = 0°C ÷ 70°C; V_{CC} = + 5V; V_{GG} = -12V ± 1V unless otherwise noted)

SYMBOL	CHARACTERISTICS	Min.	Typ.	Max.	Unit	TEST CONDITIONS
	CLOCK PULSES					
f	Repetition Rate Range	0.01		2	MHz	T_A = 25°C see waveforms
C_{pw1}	Pulse Width ϕ1	0.2		75	µs	
C_{pw2}	Pulse Width ϕ2	0.2		2	µs	
ϕd	Pulse Separation			80	µs	
t_r, t_f	Rise and Fall Time			0.5	µs	
V_{IHcp}	"1" Level Voltage	V_{CC}		V_{CC}-0.8	V	
V_{ILcp}	"0" Level Voltage	V_{CC}-15.2		V_{CC}-18.2	V	
I_{Lcp}	Leakage Current			1000	nA	V_{ILcp} = -7V T_A = 25°C
C_{cp}	Input Capacitance			50	pF	V_{ILcp} = 0V T_A = 25°C f = 1 MHz
	DATA INPUTS					
V_{IL}	"0" Level Voltage	V_{CC}-4.1		V_{CC}-18.2	V	
V_{IH}	"1" Level Voltage	V_{CC}		V_{CC}-0.8	V	
I_L	Leakage Current			50	nA	V_{in} = -7V
C_{in}	Input Capacitance			5	pF	V_{in} = 0V T_A = 25°C f = 1 MHz
	DATA OUTPUTS					
V_{OH}	"1" Level Voltage	V_{CC}-0.8			V	I_{OH} = 100 µA
V_{OL}	"0" Level Voltage			0.4	V	load = 10pF I_{sink} = 1.6mA
R_{ON}	Output ON Resistance	50		800	Ω	see fig. 3
C_{out}	Output Capacitance			8	pF	V_{out} = 0V
	SWITCHING TIMES					
t_{Dr}	Delay Time to Rise			150	ns	see waveforms and fig. 3
t_{Df}	Delay Time to Fall			150	ns	
t_{in}	Lead Time	0.15			µs	
t_{hold}	Input Hold Time	10			ns	
	POWER CONSUMPTION					
I_{GG}	Gate and Drain Current		4		mA	
P_D	Power Dissipation		68		mW	

WAVEFORMS

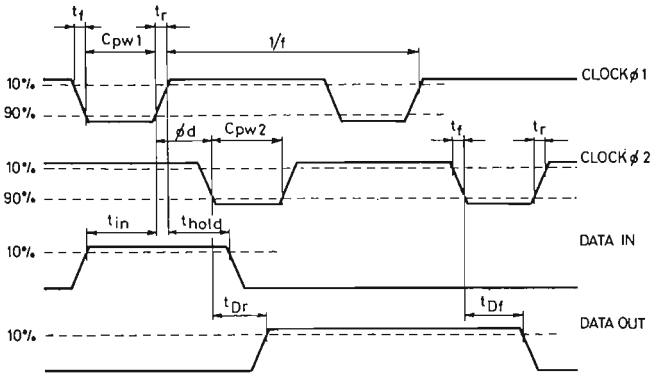


fig. 1

TIMING DIAGRAMS

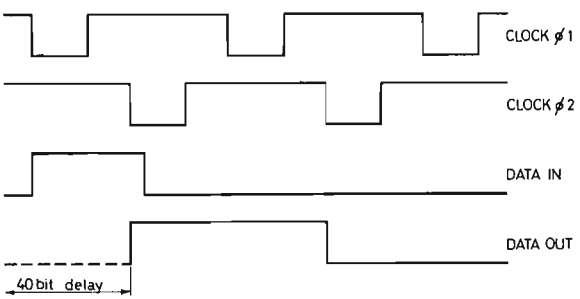


fig. 2

PARAMETER MEASUREMENT

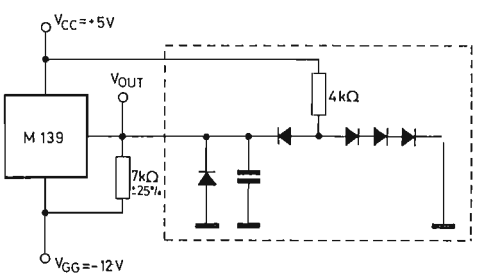
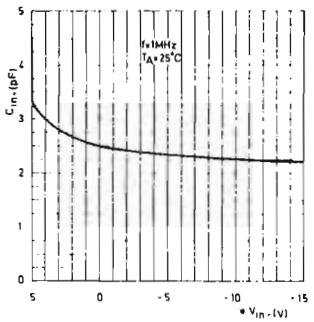


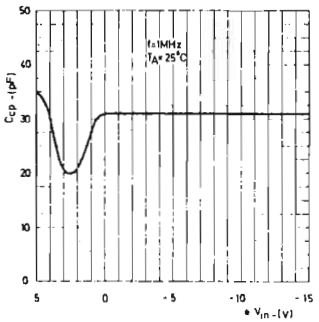
fig. 3

TYPICAL ELECTRICAL CHARACTERISTICS

INPUT CAPACITANCE
VERSUS INPUT VOLTAGE



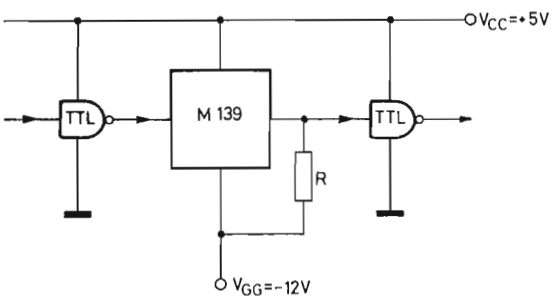
CLOCK CAPACITANCE
VERSUS CLOCK VOLTAGE



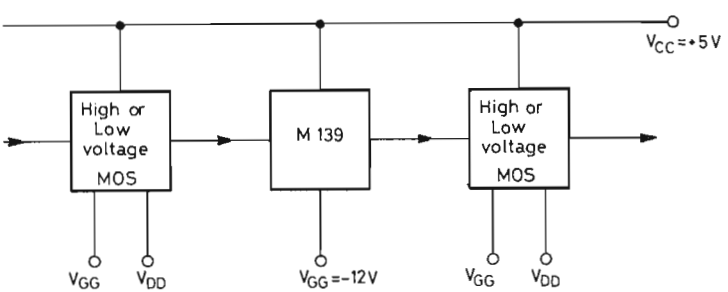
* Note : These voltages are with respect to the V_{CC} pin voltage

TYPICAL INTERFACE CIRCUITS

TTL OPERATION



MOS OPERATION



Dual 32-bit fully DC shift register

EXTENDED TEMPERATURE RANGE
-55°C to 125°C
STANDARD TEMPERATURE RANGE
0°C to 70°C

- FULLY TTL COMPATIBLE
- DC TO 2 MHz OPERATION
- SINGLE PHASE CLOCK
- INPUT GATE PROTECTION
- INPUT SELECT

The M 140 is a dual 32-bit fully DC shift register constructed on a single chip using silicon nitride-Planox, P-channel technology. The M 140 requires only a single phase and may be operated till 2 MHz over the temperature range -55°C to 125°C. The device contains two separate 32-bit registers utilizing common power and clock line and having low impedance output buffers capable of sinking TTL/DTL load current without using external components. The patented Planox technology minimizes the parasitic capacitances for higher speed operation and provides the best reliability.

ABSOLUTE MAXIMUM RATINGS
(above which the useful life may be impaired)

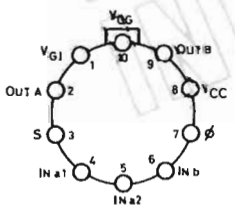
Input Voltage (1)	-20 V to 0.3 V
Clock Voltage (1)	-20 V to 0.3 V
Supply Voltage (1)	-20 V to 0.3 V
Storage Temperature Range	-65°C to 150°C

ORDERING NUMBER

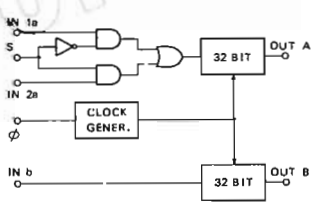
M 140 T1 (for standard temperature range)
M 140 T2 (for extended temperature range)

(1) This voltage is with respect to the V_{CC} pin voltage.

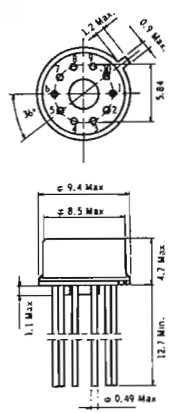
CONNECTION DIAGRAM
(top view)



LOGIC DIAGRAM



PHYSICAL DIMENSIONS
in accordance with
JEDEC TO-100

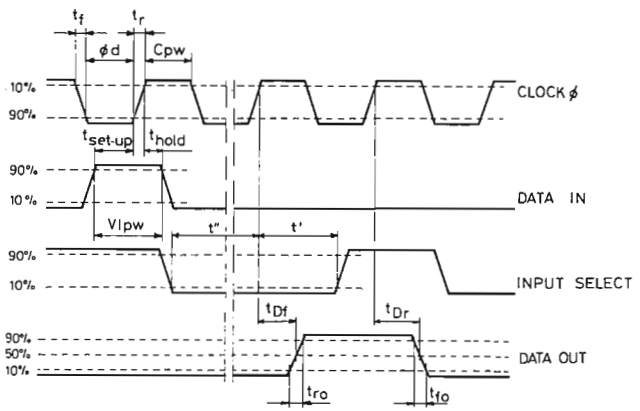


Note : all dimensions in mm.

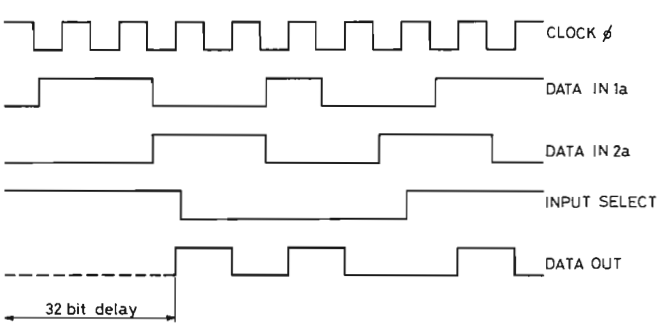
ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 0.5V; V_{GI} = GND; V_{GG} = -12V ± 1V; unless otherwise noted)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
	CLOCK PULSES					
f	Repetition Rate Range	0		2	MHz	
C_{pw}	Pulse Width	200			ns	
ϕd	Pulse Separation	200			ns	
t_r,t_f	Rise and Fall Time			1	μs	f = 100 kHz
V_{ILcp}	"0" Level Voltage			V_{CC}-4.2	V	
V_{IHcp}	"1" Level Voltage	V_{CC}-1.5			V	
I_{Lcp}	Leakage Current			1	μA	$V_{cp} = V_{CC}$ - 15V T_A = 25°C
C_{cp}	Input Capacitance			15	pF	$V_{cp} = V_{CC}$ f = 1 MHz
	DATA AND SELECT INPUTS					
V_{IL}	"0" Level Voltage			V_{CC}-4.2	V	
V_{IH}	"1" Level Voltage	V_{CC}-1.5			V	
V_{lpw}	Pulse Width	250			ns	T_A = 25°C f = 2 MHz
I_L	Leakage Current			1	μA	$V_{in} = V_{CC}$ - 15V T_A = 25°C
C_{in},C_S	Input and Select Capacitance			5	pF	$V_{in} = V_{CC}$ T_A = 25°C f = 1 MHz
$t_{set\text{-}up}$	Set-up Time		100		ns	see waveforms
t_{hold}	Hold Time		150		ns	see waveforms
t"	Select Set-up Time		100		ns	} f = 1 MHz d.c. ϕ = 50%
t'	Select Hold Time		10		ns	} see waveforms
	DATA OUTPUTS					
V_{OL}	"0" Level Voltage			0.4	V	load = 10 pF Isink=1.6mA
V_{OH}	"1" Level Voltage	V_{CC} - 1			V	I_{OH} = 100 μA
t_{ro}	Rise Time		60		ns	T_A = 25°C see waveforms
t_{fo}	Fall Time		90		ns	T_A = 25°C see waveforms
	SWITCHING TIME					
t_{Dr}	Delay Time to Rise		150		ns	T_A = 25°C see waveforms
t_{Df}	Delay Time to Fall		100		ns	T_A = 25°C see waveforms
	POWER CONSUMPTION					
I_{GG}	Gate Supply Current		6		mA	
P_D	Total Power Consumption		100		mW	nominal power supply

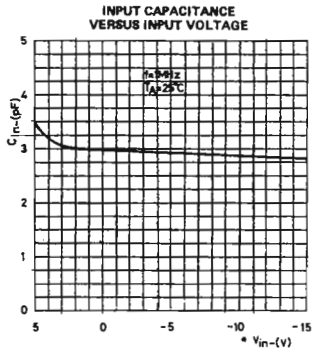
WAVEFORMS

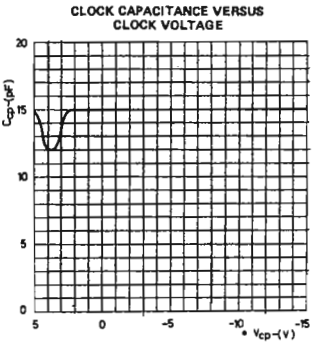


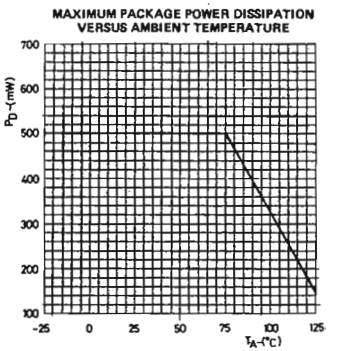
TIMING DIAGRAM



TYPICAL ELECTRICAL CHARACTERISTICS



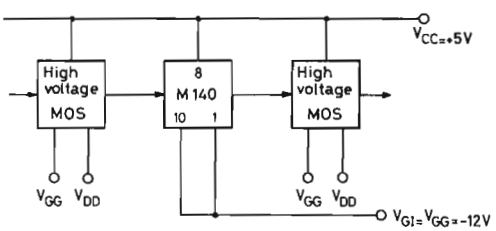




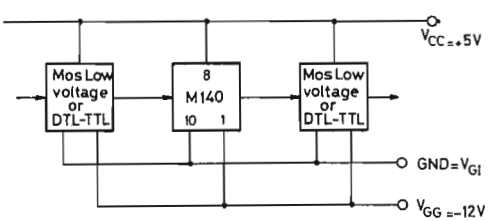
* These voltages are with respect to the V_{CC} pin voltage.

TYPICAL INTERFACE CIRCUITS

MOS OPERATION (one supply voltage)



MOS AND TTL OPERATION



1024-bit static read only memory

STANDARD TEMPERATURE RANGE,
0°C to 70°C

- INPUT GATE PROTECTION
- LOW POWER 150 mW
- CHIP SELECT INPUT
- DIRECT DRIVE OF DTL AND TTL FAMILY

The M 200 is a monolithic integrated circuit constructed on a single silicon chip by means of the P-channel MOS process. It is organized as an array of 128 words of 8 bits each and is ideally suited for code conversion, random logic synthesis, table look-up and character generation. Programming of the content is accomplished by changes in one mask during the device fabrication. Output buffers allow direct TTL interface and, in conjunction with "chip select" (CS) input, many M 200's could be used together to expand either the number of words or the number of bits per word.

ABSOLUTE MAXIMUM RATINGS
(above which the useful life may be impaired)

Input Voltage	-30 V to 0.3V
Supply Voltage	-30 V to 0.3V
Storage Temperature	-55°C to 150°C

ORDERING NUMBER :

M 200 M1AA When the content is that shown on page **503**
M 200 M1XX For your own content where **XX** will indicate your type.
In this case instructions given on page **504** should be followed.

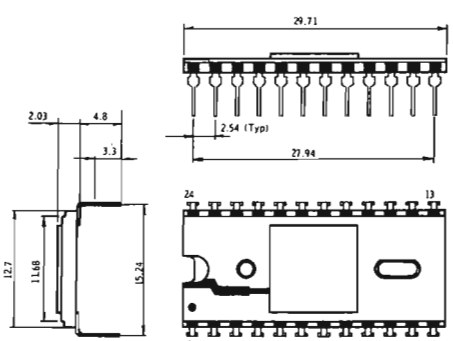
OPERATING CONDITIONS

Drain Supply Voltage (V_{DD})	-13V ± 1V
Output Buffer Supply Voltage (V_{CC})	-12V to -28V
Gate Supply Voltage (V_{GG})	-27V ± 1V

PIN CONNECTION

FUNCTION	PIN No.	FUNCTION	PIN No.
V_{DD}	1	V_{CC} Buffer Supply	13
V_{GG}	2	Output 8	14
NC	3	Output 7	15
NC	4	Output 6	16
NC	5	Output 5	17
NC	6	Output 4	18
Address 1	7	Output 3	19
Address 2	8	Output 2	20
Address 3	9	Output 1	21
Address 4	10	Address 7	22
Address 5	11	Address 6	23
Ground	12	Chip Select	24

PHYSICAL DIMENSIONS
24 pin ceramic DIP



Note : All dimensions in mm.

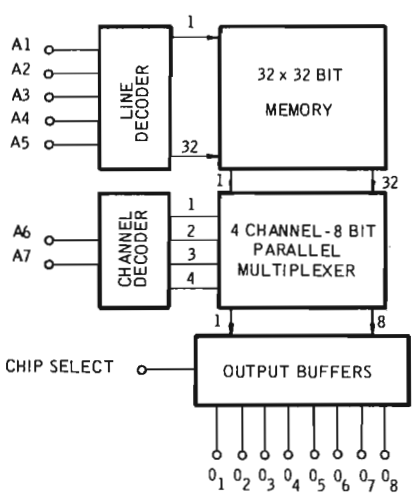
STANDARD TEMPERATURE RANGE

ELECTRICAL CHARACTERISTICS

(T_A = 0°C to 70°C unless otherwise noted; V_{DD} = -13V ± 1V; V_{CC} = -27V ± 1V; V_{CC} = -13V ± 1V; Load = 10M Ω and 10 pF).

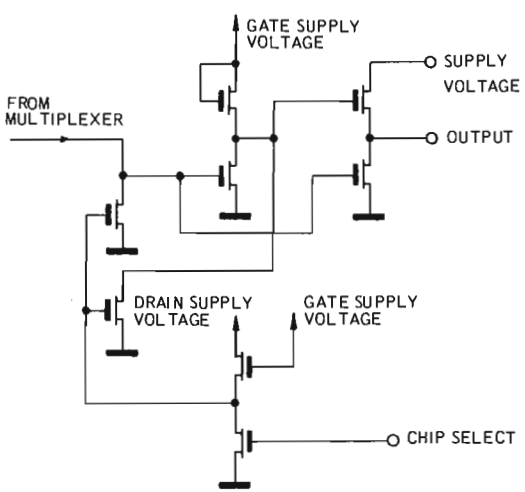
SYMBOL	CHARACTERISTICS	Min.	Typ.	Max.	Unit	TEST CONDITIONS
	ADDRESS INPUT					
V_{IL}	"0" Level Voltage			-2	V	
V_{IH}	"1" Level Voltage	-9			V	
I_L	Leakage Current			5	µA	V_{IN} = -20V
C_{in}	Input Capacitance		7		pF	
	OUTPUTS					
V_{OL}	"0" Level Voltage		-0.5	-1	V	
V_{OL1}	"0" Level Voltage			-2	V	I_{OL1} = -60µA
V_{OH}	"1" Level Voltage	-10	-13		V	
V_{OH1}	"1" Level Voltage	- 5	- 8		V	I_{OH} = 1.6mA
V_{OH2}	"1" Level Voltage		-10		V	I_{OH} = 500 µA V_{CC} = -15V
I_L	Leakage Current			-1	µA	CS = -2V V_{OUT} = -20V
	PROPAGATION DELAY					
	Address Input to Output		2.5	4	µsec	See waveforms T_A = 25°C
	POWER CONSUMPTION					
I_{DD}	Drain Current		5		mA	
I_{GG}	Gate Current		3		mA	

BLOCK DIAGRAM

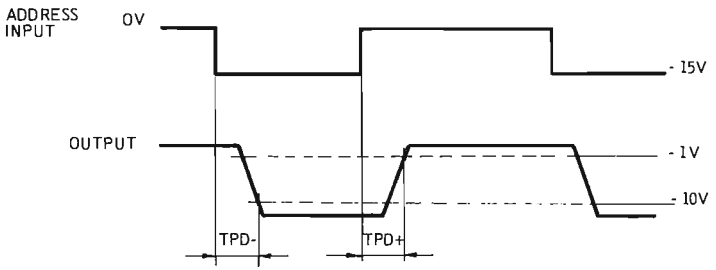


Note: When "chip select" input is "0" (-2V maw.) the outputs are floating.

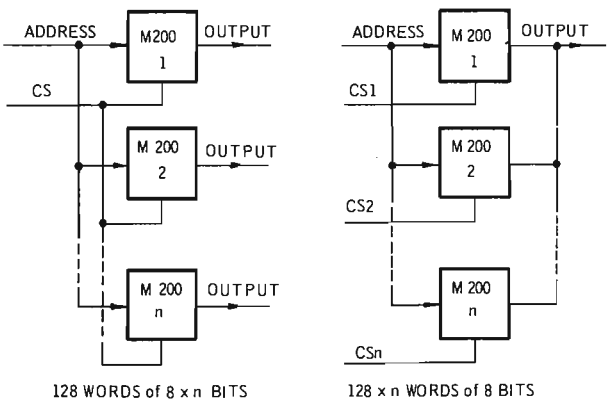
OUTPUT BUFFER CIRCUIT DIAGRAM



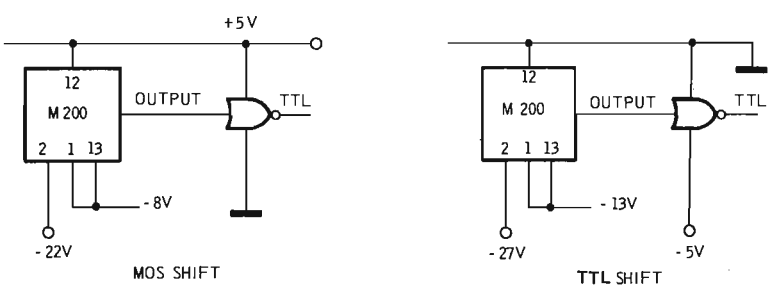
WAVEFORMS



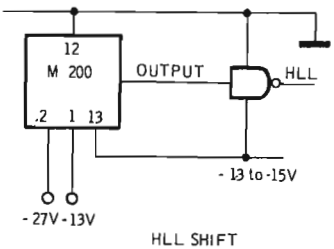
MEMORY EXPANSION

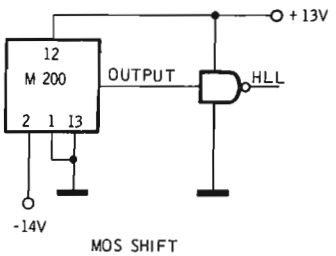


TTL DRIVE

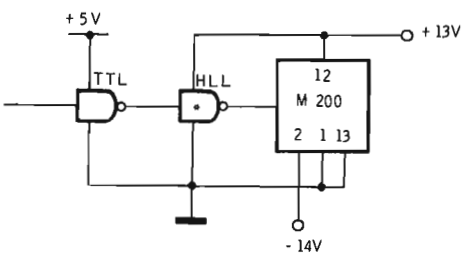


HLL DRIVE



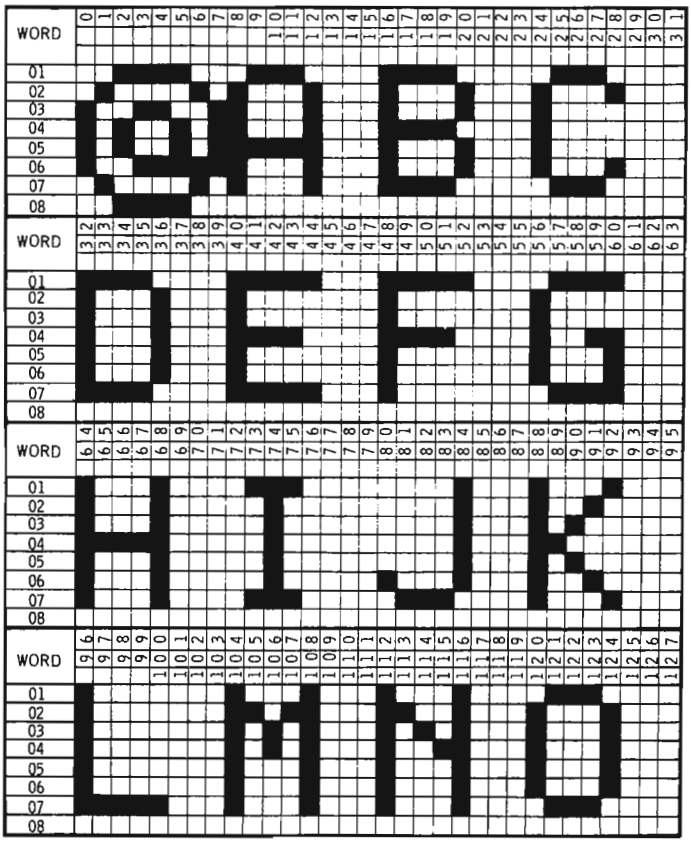


MOS DRIVE



* Use H 114 HLL device for TTL interface

M 200 M1AA CONTENT



STANDARD TEMPERATURE RANGE

HOW TO HAVE A CUSTOMIZED ROM

The SGS CAD facilities are used to customize the ROM. A large computer drives a photocomposition machine to make, from your content punched cards, the test sequence, the truth table and the masks.
This unique system eliminates pattern conversion errors; upon request a computer generated truth table can be supplied for customer re-check purposes.

Punched card format

The punched cards suitable for SGS CAD are the 80 column IBM type and one card per word is needed.

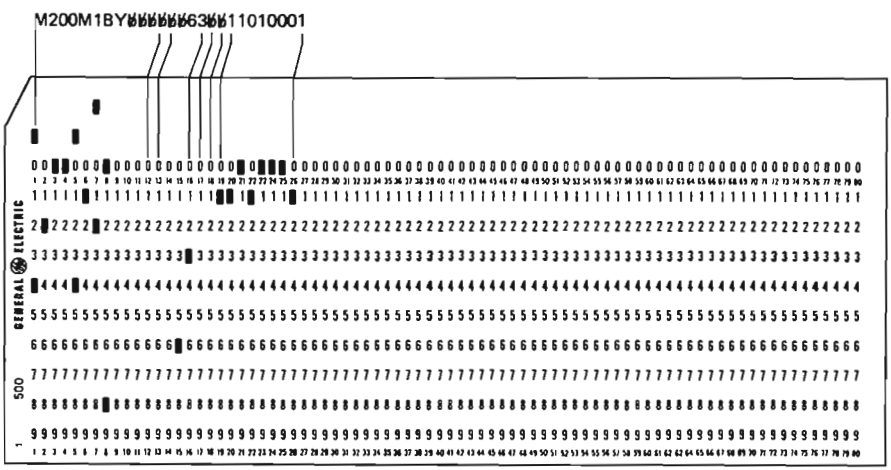
1st to 12th column - part number, alphanumeric. Each custom ROM is assigned its unique part number. First column shows the first character.

13th to 16th column - word number, numeric. First word is always called no. zero. Last column is the unity digit.

17th and 18th column - blanks ß

19th to 26th column - word content expressed in one's and zero's. Column 19th corresponds to the output 0_1, the 20th to 0_2, etc.

EXAMPLE



2048-bit two ⌀ dynamic read only memory

STANDARD TEMPERATURE RANGE,
0°C to 70°C

- INPUT GATE PROTECTION
- LOW POWER 250 μW PER BIT
- CHIP SELECT INPUT
- SIMPLE DRIVING OF TTL
- WIRED OR OUTPUT CAPABILITY

The M 210 is a monolithic integrated circuit constructed on a single silicon chip by means of the P-channel MOS process. It is organized as an array of 256 words of 8 bits each and is ideally suited for code conversion, random logic synthesis, table look-up, character generation and sequence generation. Programming of the content is accomplished by changes in one mask during device fabrication. Output buffers allow easy TTL interface, and in conjunction with "chip select" (CS) input, many M210's could be used together to expand either the number of words or the number of bits per word.

ABSOLUTE MAXIMUM RATINGS
(above which the useful life may be impaired)

Input Voltages	-30V to + 0.3V
Supply Voltages	-30V to + 0.3V
Clock Voltages	-30V to + 0.3V
Storage Temperature	-65°C to 150°C

OPERATING CONDITIONS

V_{GG}	-27V
Clock Levels	-1V to -26V

ORDERING NUMBERS :

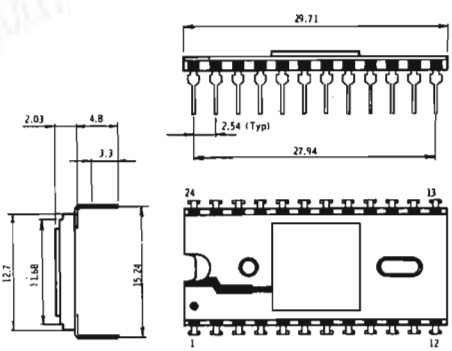
M 210 M1AA see note 1.
M 210 M1XX see last page of data sheet :
"How To Have A Customized ROM"

Note 1 : Intended for 8-bit binary counter application (see also note 3)

PIN CONNECTION

FUNCTION	Pin No	FUNCTION	Pin No.
Ground	1	Address 1 L.S.D.	13
Output 8 M.S.D	2	Address 2	14
Output 7	3	Address 3	15
Output 6	4	Address 8 M.S.D.	16
Ouptut 5	5	Address 7	17
Ouptut 4	6	Address 6	18
Ouptut 3	7	Address 5	19
Ouptut 2	8	Address 4	20
Ouptut 1 L.S.D.	9	N.C.	21
N.C.	10	V_{GG}	22
N.C.	11	$\emptyset_3$	23
Chip Select	12	$\emptyset_1$	24

PHYSICAL DIMENSIONS
24 pin ceramic DIP



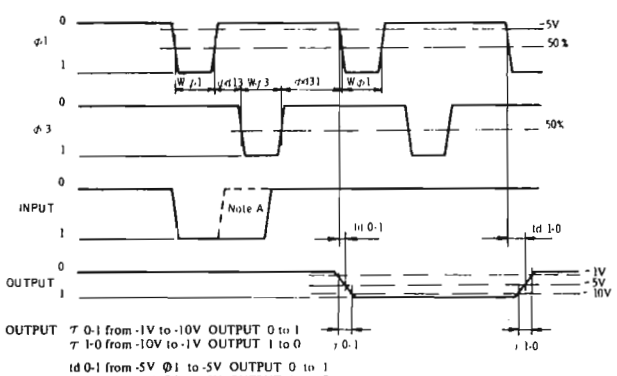
Note : all dimensions in mm.

ELECTRICAL CHARACTERISTICS

(T_A = 0 ÷ 70°C unless otherwise noted; V_{GG} = -27V ± 1V; Load = 10MΩ and 10pF)

SYMBOL	CHARACTERISTICS	Min.	Typ.	Max	Unit	TEST CONDITIONS
	CLOCK PULSES					
f	Repetition Rate	10		1000	kHz	
C_{pw}	Pulse Width	200			nsec	See figure 1
$\emptyset d13$	Pulse Separation $\emptyset 1$ to $\emptyset 3$	0			nsec	See figure 2
$\emptyset d31$	Pulse Separation $\emptyset 3$ to $\emptyset 1$	500			nsec	See figure 1
V_{ILcp}	"0" Level Voltage			-1	V	
V_{IHcp}	"1" Level Voltage	-25			V	
$C_{in\emptyset_1}$	$\emptyset 1$ Clock Input Capacitance		25	45	pF	f=1 MHz V=0V
$C_{in\emptyset_3}$	$\emptyset 3$ Clock Input Capacitance		70	90	pF	f=1 MHz V=0V
$I_{L\emptyset_1}$	Input $\emptyset 1$ Leakage			1	µA	$V_{\emptyset 3}$ = 0V
$I_{L\emptyset_3}$	Input $\emptyset 2$ Leakage			1	µA	$V_{\emptyset 1}$ = 0V V_{GG}= -27V
	ADDRESS and CS INPUTS					
V_{IL}	"0" Level Voltage			-2	V	
V_{IH}	"1" Level Voltage	-10			V	
V_{Ipw}	Address Pulse Width	250			nsec	See figure 1
I_L	Address Input and Chip Select Leakage			1	µA	V = -20V
C_{in}	Address Input Capacitance		3	5	pF	V = 0V @ 1 MHz
C_{in}	Chip Select Input Capacitance		10	13	pF	V = 0V @ 1 MHz
	DATA OUTPUT					
V_{OL}	"0" Level Voltage			-1	V	
V_{OH}	"1" Level Voltage	-11			V	
R_{on}	"ON" Resistance "1" Level		1.4		kΩ	V_{GG}= -27V $\emptyset_1 = \emptyset_3$ = -27V
R_{on}	"ON" Resistance "0" Level		2.6		kΩ	C.S. = GND f = 200 kHz
R_{off}	"OFF" Resistance	1			MΩ	
	SWITCHING DATA					
t_{d0-1}	Delay Time to "1"			200	ns	
t_{d1-0}	Delay Time to "0"			120	ns	$\emptyset_1$ and $\emptyset_3$ $\tau_r = \tau_f$ = 30 ns
$\tau 0-1$	Fall Time -1V to -10V			250	ns	
$\tau 1-0$	Rise Time -10V to -1V			350	ns	
	POWER CONSUMPTION					
I_{GG}	Current Drain from V_{GG}		15		mA	f = 10 kHz @ 25°C

WAVEFORMS



Note A : The data must be good before ø1 arrives and may change after ø1 goes to 0

FIG. 1

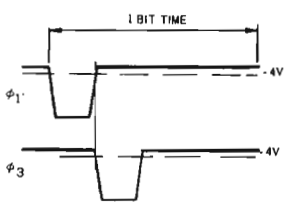
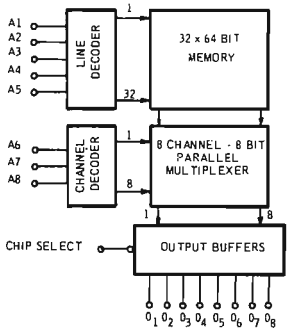
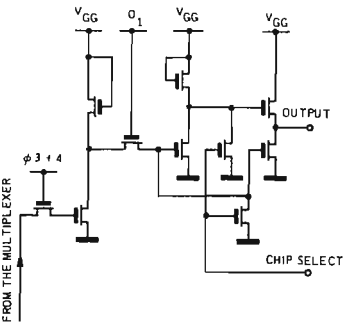


FIG. 2

BLOCK DIAGRAM



OUTPUT BUFFER CIRCUIT DIAGRAM



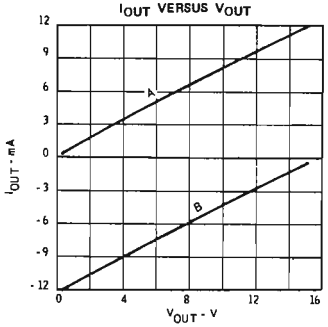
Notes : 2) When chip select input is "1" (-10V min.) the output is floating.

3) For 8-bit binary counter application each output should be connected to the corresponding input, i.e. :

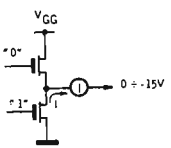
O_1 connected to A_1

O_2 connected to A_2 etc.

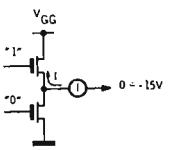
I_{OUT} VERSUS V_{OUT}



CONDITIONS OF CURVE A
OUTPUT = 0

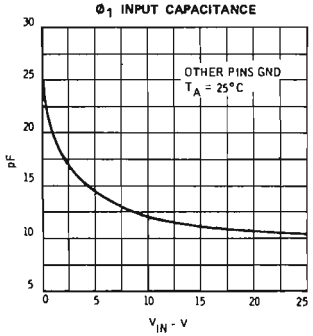


CONDITIONS OF CURVE B
OUTPUT = 1

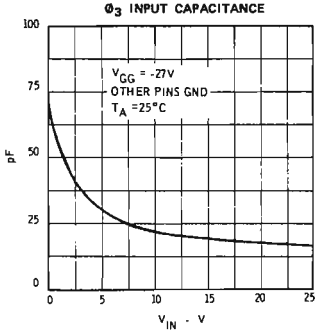


V_{OH} = -27V
V_{GG} = -27V
C.S. = GND
f = 200 kHz

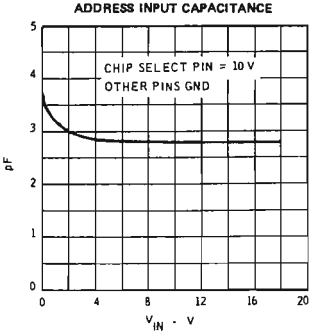
ϕ_1 INPUT CAPACITANCE

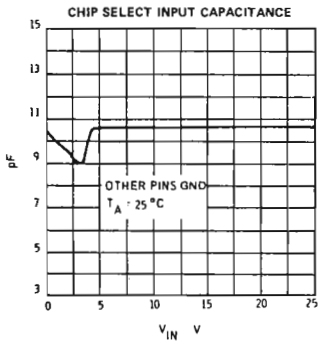


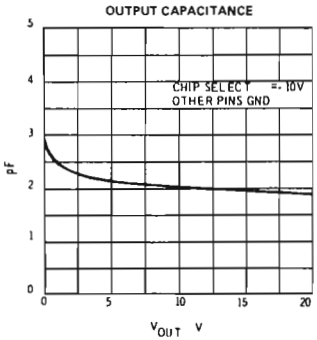
ϕ_3 INPUT CAPACITANCE



ADDRESS INPUT CAPACITANCE







HOW TO HAVE A CUSTOMIZED ROM

The SGS CAD facilities are used to customize the ROM. A large computer with a photocomposition machine creates the test sequence, the truth table and the masks from your content-punched cards.

This unique system eliminates pattern conversion errors; upon request a computer generated truth table could be supplied for customer re-check purposes.

PUNCHED CARD FORMAT

The punched cards suitable for SGS CAD are the 80 column IBM type and one card per word is needed.

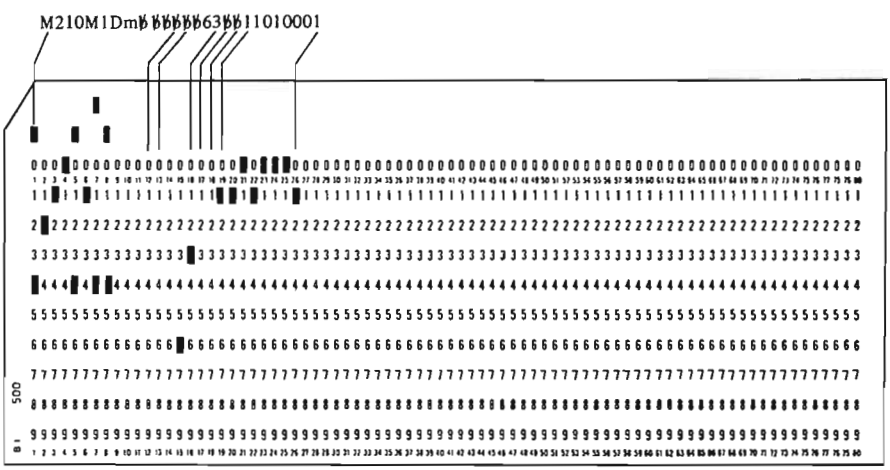
1st to 12th column - part number, alphanumeric. Each custom ROM is assigned its unique part number. First column shows the first character.

13th to 16th column - word number, numeric. First word is always called no. zero. Last column is the unity digit.

17th and 18th column - blanks ϕ

19th to 80th column - word content expressed in one's and zero's. Column 19th corresponds to the output 0_1, the 20th to 0_2, etc.

EXAMPLE



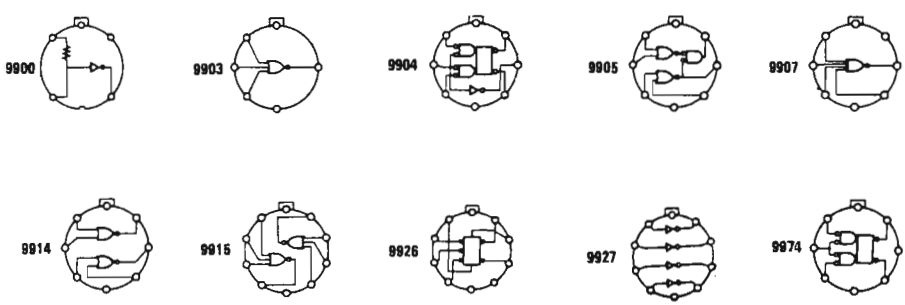
RTL INTEGRATED CIRCUITS

The following RTL devices are currently in production. Data sheets can be supplied on request.

		t_{pd} (ns)	P_D (mW)	f (MHz)	Fan Out
GATES					
9900	NOR buffer	10	20		80
9903*	NOR 3-Input	10	20		16
9907	NOR 4-Input	10	40		16
9914	NOR Dual 2-Input	15	40		16
9915	NOR Dual 3-Input	10	40		16
FLIP-FLOPS					
9926	JK		90	20	
9974	JK		90		
OTHER FUNCTIONS					
9904	Half adder	20	75		16
9905*	Half shift register	20	77		16
9927	Quad Inverter	10	30		16

* Standard temp. range only

CONNECTION DIAGRAMS



Extended temperature range (55°C to +125°C): TO-99/TO-100 packages.
Standard temperature range (0°C to +70°C): TO-99/TO-100 packages.

Printed in Italy by Pirovano - Segrate - Milano

ALPHA-NUMERICAL INDEX

LINEAR INTEGRATED CIRCUITS

DTL INTEGRATED CIRCUITS

LPDTL INTEGRATED CIRCUITS

TTL INTEGRATED CIRCUITS

HLL INTEGRATED CIRCUITS

MOS INTEGRATED CIRCUITS