SDAD003

Supplement to TTL Data Book

Volume 3

1984

Advanced Low-Power Schottky
Advanced Schottky

TEXAS INSTRUMENTS

Supplement to
The TTL Data Book
Volume 3

General Information 1

ALS and AS Circuits 2

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Supplement to The TTL Data Book

Volume 3

TEXAS INSTRUMENTS

IMPORTANT NOTICE

Texas Instruments reserves the right to make changes at any time in order to improve design and to supply the best product possible.

TI cannot assume any responsibility for any circuits shown or represent that they are free from patent infringement.

Information contained herein supersedes data published in The TTL Data Book, Volume 3, 1984, SDAD001A.

INTRODUCTION

This supplement is provided to complete the detailed specifications on 51 new Advanced Low-Power Schottky† (ALS) and Advanced Schottky† (AS) functions. Included in these recent announcements are:

- 10 gates in standard, buffer, and driver options
- 21 bus-interface devices including octal, 9-bit, and 10-bit bus buffers/drivers, transceivers, and registers with varying output designs
- 20 LSI and complex functions wih single-chip design solutions

Also, 29 of these 51 new functions are pin-for-pin equivalents for LS and S products.

This supplement also includes a general ALS/AS applications note which provides additional detailed information to aid the system designer in achieving the highest levels of performance and cost-effectiveness with TI's products.

Additionally, this supplement provides:

- Complete errata for The TTL Data Book, Volume 3, 1984 (SDAD001A). The errata contains corrections that have been made on the pages which are reprinted in this supplement. Please note or reference them in your Volume 3.
- Complete functional index for all TI bipolar digital devices available or under development. All logic technologies (TTL, LS, S, ALS, and AS), field programmable logic, programmable read-only memories, and bipolar complex LSI are included.

Please ensure that routine references to TI's data books include monitoring the current supplements and errata for updated information.

†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments, U.S. Patent Number 3,463,975.

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‡See Revisions Sections of this Supplement for changes to the *TTL Data Book, Volume 3,* 1984.

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GATES AND INVERTERS

POSITIVE-NAND GATES AND INVERTERS

DESCRIPTION	TYPE	TECHNOLOGY							VOLUME
		STD TTL	ALS	AS	H	L	LS	S	
Hex 2-Input Gates	'804		●	A					3
Hex Inverters	'04	●			●	●	●	●	2
			A	●					3
	'1004		●	●					
Quadruple 2-Input Gates	'00	●			●	●	●	●	2
			A	●					3
	'1000		A	●					
Triple 3-Input Gates	'10	●			●	●	●	●	2
			A	●					3S
	'1010		A						3
Dual 4-Input Gates	'20	●			●	●	●	●	2
			A	●					3
	'1020		A						
8-Input Gates	'30	●			●	●	●	●	2
			A	●					3S
13-Input Gates	'133							●	2
			●						3
Dual 2-Input Gates	'8003		●						

POSITIVE-NAND GATES AND INVERTERS WITH OPEN-COLLECTOR OUTPUTS

DESCRIPTION	TYPE	TECHNOLOGY							VOLUME
		STD TTL	ALS	AS	H	L	LS	S	
Hex Inverters	'05	●			●		●	●	2
			A						3
	'1005		●						
Quadruple 2-Input Gates	'01	●			●		●		2
			●						3
	'03	●				●	●	●	2
			A						3
	'1003		A						
Triple 3-Input Gates	'12	●					●		2
			A						3S
Dual 4-Input Gates	'22	●			●		●	●	2
			B						3S

POSITIVE-AND GATES

DESCRIPTION	TYPE	TECHNOLOGY						VOLUME
		STD TTL	ALS	AS	H	S	LS	
Hex 2-Input Gates	'808		●	A				3
Quadruple 2-Input Gates	'08	●				●	●	2
			●	●				3
	'1008		A	●				
Triple 3-Input Gates	'11				●	●	●	2
			A	●				3S
	'1011		A					3
Dual 4-Input Gates	'21					●		2
			●	●				3
Triple 4-Input AND/NAND	'800			▲				

POSITIVE-AND GATES WITH OPEN-COLLECTOR OUTPUTS

DESCRIPTION	TYPE	TECHNOLOGY						VOLUME
		STD TTL	ALS	AS	H	LS	S	
Quadruple 2-Input Gates	'09	●				●	●	2
			●					3
Triple 3-Input Gates	'15				●	●	●	2
			●					3

POSITIVE-OR GATES

DESCRIPTION	TYP	TECHNOLOGY					VOLUME
		STD TTL	ALS	AS	LS	S	
Hex 2-Input Gates	'832		●	A			3
Quadruple 2-Input Gates	'32	●			●	●	2
			●	●			3
	'1032		A	●			
Triple 4-Input OR/NOR	'802			▲			

POSITIVE-NOR GATES

DESCRIPTION	TYPE	TECHNOLOGY						VOLUME
		STD TTL	ALS	AS	L	LS	S	
Hex 2-Input Gates	'805		●	A				3
Quadruple 2-Input Gates	'02	●			●	●	●	2
			●	●				3
	'1002		A					
Triple 3-Input Gates	'27	●				●		2
			●	●				3
Dual 4-Input Gates with Strobe	'25	●						2
Dual 5-Input Gates	'260						●	

SCHMITT-TRIGGER POSITIVE-NAND GATES AND INVERTERS

DESCRIPTION	TYPE	TECHNOLOGY					VOLUME
		STD TTL	ALS	AS	LS	S	
Hex Inverters	'14	●			●		2
	'19				●		
Octal Inverters	'619				●		
Dual 4-Input Positive-NAND	'13	●			●		
	'18				●		
Triple 4-Input Positive-NAND	'618				●		
Quadruple 2-Input Positive-NAND	'24				●		
	'132	●			●	●	

CURRENT-SENSING GATES

DESCRIPTION	TYPE	TECHNOLOGY			VOLUME
		ALS	AS	LS	
Hex	'63			●	2

DELAY ELEMENTS

DESCRIPTION	TYP	TECHNOLOGY			VOLUME
		ALS	AS	LS	
Inverting and Noninverting Elements, 2-Input NAND Buffers	'31			●	2

● Denotes available technology.
▲ Denotes planned new products.
A Denotes "A" suffix version available in the technology indicated.
B Denotes "B" suffix version available in the technology indicated.
S Denotes supplement to data book.

GATES, EXPANDERS, BUFFERS, DRIVERS, AND TRANSCEIVERS

AND-OR-INVERT GATES

DESCRIPTION	TYPE	TECHNOLOGY							VOLUME
		STD TTL	ALS	AS	H	L	LS	S	
2-Wide 4-Input	'55				●	●	●		2
4-Wide 4-2-3-2 Input	'64							●	
4-Wide 2-2-3-2 Input	'54				●				
4-Wide 2-Input	'54	●							
4-Wide 2-3-3-2 Input	'54					●	●		
Dual 2-Wide 2-Input	'51	●			●	●	●	●	

AND-OR-INVERT GATES WITH OPEN-COLLECTOR OUTPUTS

DESCRIPTION	TYPE	TECHNOLOGY				VOLUME
		STD TTL	ALS	AS	S	
4-Wide 4-2-3-2-Input	'65				●	2

EXPANDABLE GATES

DESCRIPTION	TYPE	TECHNOLOGY						VOLUME
		STD TTL	ALS	AS	H	L	LS	
Dual 4-Input Positive-NOR With Strobe	'23	●						2
4-Wide AND-OR	'52				●			
4-Wide AND-OR-INVERT	'53	●			●			
2-Wide AND-OR-INVERT	'55				●	●	●	
Dual 2-Wide AND-OR-INVERT	'50	●			●			

EXPANDERS

DESCRIPTION	TYPE	TECHNOLOGY				VOLUME
		STD TTL	ALS	AS	H	
Dual 4-Input	'60	●			●	2
Triple 3-Input	'61				●	
3-2-2-3-Input AND-OR	'62				●	

BUFFER AND INTERFACE GATES WITH OPEN-COLLECTOR OUTPUTS

DESCRIPTION	TYPE	TECHNOLOGY					VOLUME
		STD TTL	ALS	AS	LS	S	
Hex	'07	●					2
	'17	●					
	'35		●				3S
	'1035		●				3
Hex Inverter	'06	●					2
	'16	●					
	'1005		●				3
Quad 2-Input Positive-NAND	'26	●					2
	'38	●			●	●	
			A				3
	'39	●					2
	'1003		A				3
Quad 2-Input Positive-NOR	'33	●			●		2
			A				3

BUFFERS, DRIVERS, AND BUS TRANSCEIVERS WITH OPEN-COLLECTOR OUTPUTS

DESCRIPTION	TYPE	TECHNOLOGY					VOLUME
		STD TTL	ALS	AS	LS	S	
Noninverting Octal Buffers/Drivers	'743		▲				CF
	'757			●			3S
	'760			●			
Inverting Octal Buffers/Drivers	'742		▲				CF
	'756			●			3S
	'763			●			
Inverting and Noninverting Octal Buffers/Drivers	'762			●			
Noninverting Quad Transceivers	'759			●			
Inverting Quad Transceivers	'758			●			

GATES, BUFFERS, DRIVERS, AND BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

DESCRIPTION	TYPE	TECHNOLOGY					VOLUME
		STD TTL	ALS	AS	LS	S	
Noninverting Octal Buffers/Drivers	'241				●	●	2
			A	●			3
	'244				●	●	2
			A	●			3
	'465				●		2
			A				3
	'467				●		2
			A				3
	'541				●		2
			▲				
	'1241¶		▲				3
	'1244¶		A				
Inverting Octal Buffers/Drivers	'231			●			
	'240				●	●	2
			A	●			3
	'466				●		2
			A				3
	'468				●		2
			A				3
	'540				●		2
			▲				
	'1240¶		●				3
Inverting and Noninverting Octal Buffers/Drivers	'230			●			
Octal Transceivers	'245				●		2
			A	▲			3
	'1245		A				3S
Noninverting Hex Buffers/Drivers	'365	A			A		2
			▲				3
	'367	A			A		2
			▲				3
Inverting Hex Buffers/Drivers	'366	A			A		2
			▲				3
	'368	A			A		2
			▲				3
Quad Buffers/Drivers with Independent Output Controls	'125	●			A		2
	'126	●			A		
	'425	●					
	'426	●					
Noninverting Quad Transceivers	'243				●		3
			A	●			
	'1243¶		▲				
Inverting Quad Transceivers	'242				●		2
			A	●			3
	'1242¶		▲				
Quad Transceivers with Storage	'226					●	2
12-Input NAND Gate	'134					●	
Controller and Bus Driver for 8080A System	'428					●	

50-OHM/75-OHM LINE DRIVERS

DESCRIPTION	TYPE	TECHNOLOGY				VOLUME
		STD TTL	ALS	AS	S	
Hex 2-Input Positive-NAND	'804		●	A		3
Hex 2-Input Positive-NOR	'805		●	A		
Hex 2-Input Positive-AND	'808		●	A		
Hex 2-Input Positive-OR	'832		●	A		
Quad 2-Input Positive-NOR	'128	●				2
Dual 4-Input Positive-NAND	'140				●	

CF Denotes Contact Factory
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¶ Denotes very low power.
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BUFFERS, DRIVERS, TRANSCEIVERS, AND CLOCK GENERATORS

BUFFERS, CLOCK/MEMORY DRIVERS

DESCRIPTION	TYPE	TECHNOLOGY						VOLUME
		STD TTL	ALS	AS	H	LS	S	
Hex 2-Input Positive-NAND	'804		●	A				3
Hex 2-Input Positive-NOR	'805		●	A				
Hex 2-Input Positive-AND	'808		●	A				
Hex 2-Input Positive-OR	'832		●	A				
Hex Inverter	'1004		●	●				
Hex Buffer	'34		▲	●				
	'1034		●	●				
Quad 2-Input Positive-NAND	'37	●				●	●	2
			A					3
	'1000		A	●				
Quad 2-Input Positive-NOR	'28	●				●		2
			A					3
	'1002		A					
	'1036			●				
Quad 2-Input Positive-AND	'1008		A	●				
Quad 2-Input Positive-OR	'1032		A	●				
Triple 3-Input Positive-NAND	'1010		A					
Triple 3-Input Positive-AND	'1011		A					
Triple 4-Input AND-NAND	'800			▲				
Triple 4-Input OR-NOR	'802			▲				
Dual 4-Input Positive-NAND	'40	●			●	●	●	2
			A					3
	'1020		A					
Line Driver/Memory Driver with Series Damping Resistor	'436						●	2
Line Driver/Memory Driver	'437						●	

BI-/TRI-DIRECTIONAL BUS TRANSCEIVERS AND DRIVERS

DESCRIPTION	TYPE OF OUTPUT	TYPE	TECHNOLOGY				VOLUME
			ALS	AS	LS	S	
Quad with Bit Direction	3-State	'446			●		2
Controls	3-State	'449			●		
Quad Tridirection	OC	'440			●		
	OC	'441			●		
	3-State	'442			●		
	3-State	'443			●		
	3-State	'444			●		
	OC	'448			●		
4-Bit with Storage	3-State	'226				●	
Controller and Bus Driver for 8080A Systems		'428				●	4

OCTAL BUS TRANSCEIVERS/MOS DRIVERS

DESCRIPTION	TYPE	TECHNOLOGY					VOLUME
		STD TTL	ALS	AS	LS	S	
Inverting Outputs, 3-State	'2620			●			3
	'2640			●			
True Outputs, 3-State	'2623			●			
	'2645			●			

OCTAL BUFFERS AND LINE DRIVERS WITH INPUT/OUTPUT RESISTORS

DESCRIPTION		TYPE	TECHNOLOGY					VOLUME
			STD TTL	ALS	AS	LS	S	
Input Resistors	Inverting Outputs	'746		▲				CF
	Noninverting Outputs	'747		▲				
Output Resistors	Inverting Outputs	'2540		▲				
	Noninverting Outputs	'2541		▲				

OCTAL BI-/TRI-DIRECTIONAL BUS TRANSCEIVERS

DESCRIPTION		TYPE OF OUTPUT	TYPE	TECHNOLOGY			VOLUME
				ALS	AS	LS	
12 mA/24 mA/48 mA/64 mA Sink, True Outputs	Low Power	3-State	'245	A	▲		3
						●	2
		OC	'621	A	●		3S
						●	2
		3-State	'623	A	●		3S
						●	2
		OC, 3-State	'639	A	●		3
						●	2
		3-State	'652	▲	●		3S
						●	2
		OC, 3-State	'654	▲			3
						●	2
	Very Low Power	OC	'1621	▲			3
		3-State	'1623	▲			
		OC, 3-State	'1639	▲			
12 mA/24 mA/48 mA/64 mA Sink, Inverting Outputs	Low Power	3-State	'620	A	●		3S
						●	2
		OC	'822	A	●		3S
						●	2
		OC, 3-State	'638	A	●		3
						●	2
		3-State	'651	▲	●		3S
						●	2
		OC, 3-State	'653	▲			3
						●	2
	Very Low Power	3-State	'1620	▲			3
		OC	'1622	▲			
		OC, 3-State	'1638	▲			
12 mA/24 mA/48 mA/64 mA Sink, True Outputs	Low Power	OC	'641	A	●		2
						●	
		3-State	'645	A	●		3
						●	2
	Very Low Power	OC	'1641	▲			3
		3-State	'1645	A			
12 mA/24 mA/48 mA/64 mA Sink, Inverting Outputs	Low Power	3-State	'640	A	●		2
						●	
		OC	'642	A	●		3
						●	2
	Very Low Power	3-State	'1640	A			3
		OC	'1642	▲			
12 mA/24 mA/48 mA/64 mA Sink, True and Inverting Outputs	Low Power	3-State	'643	A	●		2
						●	
		OC	'644	A	●		3
						●	2
	Very Low Power	3-State	'1643	▲			3
		OC	'1644	▲			
Registered with Multiplex 12 mA/24 mA/48 mA/64 mA True Outputs		3-State	'646	▲	●		3S
						●	2
		OC	'647	▲			3
						●	2
Registered with Multiplexed 12 mA/24 mA/48 mA/64 mA Inverting Outputs		3-State	'648	▲	●		3S
						●	2
		OC	'649	▲			3
						●	2
Universal Transceiver/ Port Controllers		3-State	'877		●		3S
			'852		▲		3
			'856		▲		

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1 GENERAL INFORMATION

FLIP-FLOPS

DUAL AND SINGLE FLIP-FLOPS

DESCRIPTION	TYPE	TECHNOLOGY							VOLUME
		STD TTL	ALS	AS	H	L	LS	S	
Dual J-K Edge-Triggered	'73						A		2
	'76						A		
	'78						A		
	'103				●				
	'106				●				
	'107						A		
	'108				●				
	'109	●					A		
			A	●					3S
	'112						A	●	2
			A	▲					3
	'113						A	●	2
			A	▲					3
	'114						A	●	2
			A	▲					3
Single J-K Edge-Triggered	'70	●							2
	'101				●				
	'102				●				
Dual Pulse-Triggered	'73	●			●	●			
	'76	●			●				
	'78				●	●			
	'107	●							
Single Pulse-Triggered	'71				●	●			
	'72	●			●	●			
	'104	●							
	'105	●							
Dual J-K with Data Lockout	'111	●							
Single J-K with Data Lockout	'110	●							
Dual D-Type	'74	●			●	●	A	●	
			A	●					3S

QUAD AND HEX FLIP-FLOPS

DESCRIPTION	NO. OF FFs	OUTPUTS	TYPE	TECHNOLOGY					VOLUME
				STD TTL	ALS	AS	LS	S	
D Type	6	Q	'174	●			●	●	2
					●	●			3
			'378				●		2
	4	Q, $\overline{Q}$	'171				●		
			'175	●			●	●	
					●	●			3S
			'379				●		2
J-K	4	Q	'276	●					
			'376	●					

OCTAL, 9-BIT, AND 10-BIT D-TYPE FLIP-FLOPS

DESCRIPTION	NO. OF BITS	OUTPUT	TYPE	TECHNOLOGY					VOLUME
				STD TTL	ALS	AS	LS	S	
True Data	Octal	3-State	'374		●	●			3
							●	●	2
		3-State	'574		●	●			3
True Data with Clear	Octal	2-State	'273		●				
				●			●		2
		3-State	'575		●	●			3
		3-State	'874		●	●			
		3-State	'878		●	●			
True with Enable	Octal	2-State	'377				●		2
Inverting	Octal	3-State	'534		●	●			3
		3-State	'564		●				
			'576		●	●			
Inverting with Clear	Octal	3-State	'577		●	●			
		3-State	'879		●	●			
Inverting with Preset	Octal	3-State	'876		●	●			
True	Octal	3-State	'825			▲			
Inverting	Octal	3-State	'826			▲			
True	9-Bit	3-State	'823			▲			
Inverting	9-Bit	3-State	'824			▲			
True	10-Bit	3-State	'821			●			
Inverting	10-Bit	3-State	'822			●			

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LATCHES AND MULTIVIBRATORS

QUAD LATCHES

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY					VOLUME
			STD TTL	ALS	AS	L	LS	
Dual 2-Bit Transparent	2-State	'75	●			●	●	2
	2-State	'77	●			●	●	
	2-State	'375					●	
S-R	2-State	'279	●				A	

RETRIGGERABLE MONOSTABLE MULTIVIBRATORS

DESCRIPTION	TYPE	TECHNOLOGY					VOLUME
		STD TTL	ALS	AS	LS	L	
Single	'122	●			●	●	2
	'130	●					
	'422				●		
Dual	'123	●			●	●	
	'423				●		

D-TYPE OCTAL, 9-BIT, AND 10-BIT RAD-BACK LATCHES

DESCRIPTION	NO. OF BITS	TYPE	TECHNOLOGY					VOLUME
			STD TTL	ALS	AS	LS	S	
Edge-Triggered Inverting and Noninverting	Octal	'996		▲				CF
Transparent True	Octal	'990		▲				
	9-Bit	'992		▲				
	10-Bit	'994		▲				
Transparent Noninverting	Octal	'991		▲				
	9-Bit	'992		▲				
	10-Bit	'994		▲				
Transparent with Clear True Outputs	Octal	'666		▲				
Transparent with Clear Inverting Outputs	Octal	'667		▲				

OCTAL, 9-BIT, AND 10-BIT LATCHES

DESCRIPTION	NO. OF BITS	OUTPUT	TYPE	TECHNOLOGY					VOLUME
				STD TTL	ALS	AS	LS	S	
Transparent	Octal	3-State	'268					●	2
			'373				●	●	
					●	●			3
		3-State	'573		●	●			
Dual 4-Bit Transparent	Octal	2-State	'100	●					2
		2-State	'116	●					
		3-State	'873		●	●			
Inverting Transparent	Octal	3-State	'533		●	●			3
		3-State	'563		●				
		3-State	'580		●	●			
Dual 4-Bit Inverting Transparent	Octal	3-State	'880		●	●			
2-Input Multiplexed	Octal	3-State	'604				●		2
		OC	'605				●		
		3-State	'606				●		
		OC	'607				●		
Addressable	Octal	2-State	'259	●			●		
					▲				3
Multi-Mode Buffered	Octal	3-State	'412					●	2
True	Octal	3-State	'845		▲	●			3S
Inverting	Octal	3-State	'846		▲	▲			
True	9-Bit	3-State	'843		▲	●			
Inverting	9-Bit	3-State	'844		▲	●			
True	10-Bit	3-State	'841		▲	●			
Inverting	10-Bit	3-State	'842		▲	●			

MONOSTABLE MULTIVIBRATORS WITH SCHMITT-TRIGGER INPUTS

DESCRIPTION	TYPE	TECHNOLOGY					VOLUME
		STD TTL	ALS	AS	LS	S	
Single	'121	●					2
Dual	'221	●			●		

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REGISTERS

SHIFT REGISTERS

DESCRIPTION	NO. OF BITS	MODES S/R	MODES S/L	MODES LOAD	MODES HOLD	TYPE	TECHNOLOGY STD TTL	TECHNOLOGY ALS	TECHNOLOGY AS	TECHNOLOGY L	TECHNOLOGY LS	TECHNOLOGY S	VOLUME
Sign-Protected		X		X	X	'322					A		
Parallel-In, Parallel-Out, Bidirectional	8	X	X	X	X	'198	●						2
		X	X	X	X	'299					●	●	
								●	▲				3
		X	X	X	X	'323					●		2
								●	▲				3
	4	X	X	X	X	'194	●				A	●	2
									▲				3
Parallel-In, Parallel-Out, Registered Outputs	4	X	X	X	X	'671					●		
		X	X	X	X	672					●		2
Parallel In, Parallel Out	8	X		X	X	'199	●						
	5	X		X		'96	●			●	●		
	4	X		X		'95	A			●	B		2
									●				3S
		X		X		'99				●			
		X		X	X	'178	●						2
		X		X	X	'179	●						
		X		X		'195	●				A	●	2
									▲				3
		X		X		'295					B		2
		X		X		'395					A		2
									▲				3
Serial-In Parallel-Out	16	X		X	X	'673					●		2
	8	X				'164	●			●	●		
								▲					3
Parallel-In, Serial-Out	16	X		X	X	'674					●		2
	8	X		X	X	'165	●				A		
								▲					3
		X		X	X	'166	●				A		2
								▲					3
Serial-In, Serial-Out	8	X				'91	A			●	●		2
	4	X		X		'94	●						

SHIFT REGISTERS WITH LATCHES

DESCRIPTION	NO. OF BITS	OUTPUTS	TYPE	TECHNOLOGY ALS	TECHNOLOGY AS	TECHNOLOGY LS	VOLUME
Parallel-In, Parallel-Out with Output Latches	4	3-State	'671			●	2
		3-State	'672			●	
Serial-In, Parallel-Out with Output Latches	16	2-State	'673			●	
	8	Buffered	'594			●	
		3-State	'595			●	
		OC	'596			●	
		OC	'599			●	
Parallel-In, Serial-Out, with Input Latches	8	2-State	'597			●	
		3-State	'589			●	
Parallel I/O Ports with Input Latches, Multiplexed Serial Inputs	8	3-State	'598			●	

SIGN-PROTECTED REGISTERS

DESCRIPTION	NO. OF BITS	MODES S/R	MODES S/L	MODES LOAD	MODES HOLD	TYPE	TECHNOLOGY ALS	TECHNOLOGY AS	TECHNOLOGY LS	VOLUME
Sign-Protected Register	8	X		X	X	'322			A	2

REGISTER FILES

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY STD TTL	TECHNOLOGY ALS	TECHNOLOGY AS	TECHNOLOGY LS	VOLUME
8 Words × 2 Bits	3-State	'172	●				
4 Words × 4 Bits	OC	'170	●			●	2
	3-State	'670				●	
Dual 16 Words × 4 Bits	3-State	'870			▲		3
	3-State	'871			▲		

OTHER REGISTERS

DESCRIPTION	TYPE	TECHNOLOGY STD TTL	TECHNOLOGY ALS	TECHNOLOGY AS	TECHNOLOGY L	TECHNOLOGY LS	TECHNOLOGY S	VOLUME
Quadruple Multiplexers with Storage	'98				●			2
	'298	●				●		
				●				3S
	'398				●			2
	'399				●			
9-Bit Universal Shift Registers	'299			●	▲		●	●	3
Quadruple Bus-Buffer Registers	173	●				A		2
Octal Storage Register	396					●		

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COUNTERS

SYNCHRONOUS COUNTERS — POSITIVE-EDGE TRIGGERED

DESCRIPTION	PARALLEL LOAD	TYPE	TECHNOLOGY							VOLUME
			STD TTL	ALS	AS	L	LS	S		
Decade	Sync	'160	●				A			2
				A	●					3S
	Sync	'162	●				A	●		2
				A	●					3S
	Sync	'560		A						3
	Sync	'668					●			2
	Sync	'690					●			
	Sync	'692					●			
Decade Up/Down	Sync	'168			B	●				3S
							B	●		
	Async	'190	●				●			2
				●						3
	Async	192	●			●	●			2
				●						3
	Sync	'568		A						
	Sync	696					●			2
	Sync	'698					●			
Decade Rate Multiplier, $\frac{1}{N10}$	Async Set-to-9	'167	●							2
4-Bit Binary	Sync	'161	●				A			2
				A	●					3S
	Sync	163	●				A	●		2
				A	●					3S
	Sync	'561		A						3
	Sync	'669					●			2
	Sync	'691					●			
	Sync	'693					●			
	Sync	'169			B	●				3S
							B	●		
4-Bit Binary Up-Down	Async	'191	●				●			2
				●						3
	Async	'193	●			●	●			2
				●						3
	Sync	'569		A						
	Sync	'697					●			2
	Sync	'699					●			
6-Bit Binary Rate Multiplier, $\frac{1}{N2}$		'97	●							2
8-Bit Up-Down	Async CLR	'867			●					3
	Sync CLR	'869			●					

ASYNCHRONOUS COUNTERS (RIPPLE CLOCK) — NEGATIVE-EDGE TRIGGERED

DESCRIPTION	PARALLEL LOAD	TYPE	TECHNOLOGY						VOLUME
			STD TTL	ALS	AS	L	LS	S	
Decade	Set-to-9	'90	A			●	●		2
		'68					●		
	Yes	'176	●						
	Yes	'196	●				●	●	
	Set-to-9	'290	●				●		
4-Bit Binary	None	'93	A			●	●		
		'69					●		
	Yes	'177	●						
	Yes	'197	●				●	●	
	None	'293	●				●		
Divide-by-12	None	'92	A				●		
Dual Decade	None	'390	●				●		
	Set-to-9	'490	●				●		
Dual 4-Bit Binary	None	'393	●				●		

8-BIT BINARY COUNTERS WITH REGISTERS

DESCRIPTION	TYPE OF OUTPUT	TYPE	TECHNOLOGY			VOLUME
			ALS	AS	LS	
Parallel Register Outputs	3-State	'590			●	2
	OC	'591			●	
Parallel Register Inputs	2-State	'592			●	
Parallel I/O	3-State	'593			●	

FREQUENCY DIVIDERS, RATE MULTIPLIERS

DESCRIPTION	TYPE	TECHNOLOGY				VOLUME
		STD TTL	ALS	AS	LS	
50-to-1 Frequency Divider	'56				●	2
60-to-1 Frequency Divider	'57				●	
60-Bit Binary Rate Multiplier	'97	●				
Decade Rate Multiplier	'167	●				

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DECODERS, ENCODERS, DATA SELECTORS/MULTIPLEXERS AND SHIFTERS

DATA SELECTORS/MULTIPLEXERS

DESCRIPTION	TYPE OF OUTPUT	TYPE	TECHNOLOGY						VOLUME
			STD TTL	ALS	AS	L	LS	S	
16-To-1	2-State	'150	●						2
	3-State	'250			●				3S
	3-State	'850			●				
	3-State	'851			●				
Dual 8-To-1	3-State	'351	●						2
8-To-1	2-State	'151	A				●	●	
					●	●			3S
	2-State	'152	A				●		2
	3-State	'251	●				●	●	
					●	▲			3
	3-State	'354					●		2
	2-State	'355					●		
	3-State	'356					●		
	OC	'357					●		
Dual 4-To-1	2-State	'153	●			●	●	●	2
					●	●			3
	3-State	'253					●	●	2
					●	●			3
	2-State	'352					●		2
					●	●			3
	3-State	'353					●		2
					●	●			3
Octal 2-To-1 with Storage	3-State	'604					●		2
	OC	'605					●		
	3-State	'606					●		
	OC	'607					●		
Quad 2-To-1 with Storage	2-State	'98				●			2
	2-State	'298	●				●		
					●				3S
	2-State	'398					●		2
	2-State	'399					●		
Quad 2-To-1	2 State	'157	●			●	●	●	3
					●	●			
	2-State	'158					●	●	2
					●	●			3
	3-State	'257					B	●	2
					●	●			3
	3-State	'258					B	●	2
					●	●			3
6-to-1 Universal Multiplexer	3-State	'857			●	●			

DECODERS/DEMULTIPLEXERS

DESCRIPTION	TYPE OF OUTPUT	TYPE	TECHNOLOGY						VOLUME
			STD TTL	ALS	AS	L	LS	S	
4-To-16	3-State	'154	●			●			2
	OC	'159	●						
4-To-10 BCD-To-Decimal	2-State	'42	A			●	●		
4-To-10 Excess 3-To-Decimal	2-State	'43	A			●			
4-To-10 Excess 3-Gray-To-Decimal	2-State	'44	A			●			
3-To-8 with Address Latches	2-State	'131		●	▲				3
		'137		●	▲				
							●		2
3-To-8	2-State	'138		●	▲				3
							●	●	2
	3-State	'538		▲					3
Dual 2-To-4	2-State	'139		▲	●				
							A	●	2
	2-State	'155	●				A		
	OC	'156	●				●		
Dual 1 To-4 Decoders	3-State	'539		▲					3

CODE CONVERTERS

DESCRIPTION	TYPE	TECHNOLOGY		VOLUME
		STD TTL	S	
6-Line-BCD to 6-Line Binary, Or 4-Line to 4-Line BCD 9's/BCD 10's Converters	'184	●		2
6-Bit-Binary to 6-Bit BCD Converters	'185	A		
BCD-to-Binary Converters	'484		A	4
Binary-to-BCD Converters	'485		A	

PRIORITY ENCODERS/REGISTERS

DESCRIPTION	TYPE	TECHNOLOGY				VOLUME
		STD TTL	ALS	AS	LS	
Full BCD	'147	●			●	2
Cascadable Octal	'148	●			●	
Cascadable Octal with 3-State Outputs	'348				●	
4-Bit Cascadable with Registers	'278	●				

SHIFTERS

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY						VOLUME
			STD TTL	ALS	AS	L	LS	S	
4-Bit Shifter	3-State	'350						●	2
Parallel 16 Bit Multi-Mode Barrel Shifter	3 State	'897			▲				4

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DISPLAY DECODERS/DRIVERS, MEMORY/MICROPROCESSOR CONTROLLERS, AND VOLTAGE-CONTROLLED OSCILLATORS

OPEN-COLLECTOR DISPLAY DECODERS /DRIVERS

DESCRIPTION	OFF-STATE OUTPUT VOLTAGE	TYPE	TECHNOLOGY					VOLUME
			STD TTL	ALS	AS	L	LS	
BCD-To-Decimal	30 V	'45	●					2
	60 V	'141	●					
	15 V	'145	●				●	
	7 V	'445					●	
BCD-To-Seven-Segment	30 V	'46	A			●		
	15 V	'47	A			●	●	
	5.5 V	'48	●				●	
	5.5 V	'49	●				●	
	30 V	'246	●					
	15 V	'247	●				●	
	7 V	'347					●	
	7 V	'447					●	
	5.5 V	'248	●				●	
	5.5 V	'249	●				●	

OPEN COLLECTOR DISPLAY DECODERS/DRIVERS WITH COUNTERS/LATCH

DESCRIPTION	TYPE	TECHNOLOGY			VOLUME
		STD TTL	ALS	AS	
BCD Counter/4-Bit Latch/BCD-To-Decimal Decoder/Driver	'142	●			2
BCD Counter/4-Bit Latch/BCD-To-Seven-Segment Decoder/Lad Driver	'143	●			
BCD Counter/4-Bit Latch/BCD-To-Seven-Segment Decoder/Lamp Driver	'144	●			

VOLTAGE-CONTROLLED OSCILLATORS

DESCRIPTION						TYPE	TECHNOLOGY		VOLUME
No. VCOs	COMP'L Z_{OUT}	ENABLE	RANGE INPUT	R_{ext}	f_{max} MHz		LS	S	
Single	Yes	Yes	Yes	No	20	'624	●		2
Single	Yes	Yes	Yes	Yes	20	'628	●		
Dual	No	Yes	Yes	No	60	'124		●	
Dual	Yes	Yes	No	No	20	'626	●		
Dual	No	No	No	No	20	'627	●		
Dual	No	Yes	Yes	No	20	'629	●		

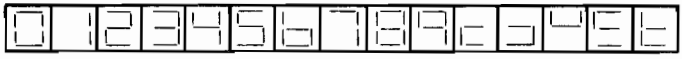
MEMORY/MICROPROCESSOR CONTROLLERS

DESCRIPTION			TYPE	TECHNOLOGY				VOLUME
				ALS	AS	LS	S	
System Controllers For 8080A			'428				●	4
System Controller, Universal			'482				●	
System Controllers, Universal (or For 888)			'890		▲			2
Memory Refresh Controllers	Transparent,	4K, 16K	'600			A		
	Burst Modes	64K	'601			A		
	Cycle Steal,	4K, 16K	'602			A		
	Burst Modes	64K	'603			A		
Memory Cycle Controller			'608			●		
Memory Mappers		3-State	'612			●		
		OC	'613			●		
Memory Mappers With Output Latches		3-State	'610			●		
		OC	'611			●		
Multi-Mode Latches (8080A Applications)			'412				●	

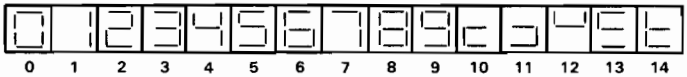
CLOCK GENERATOR CIRCUITS

DESCRIPTION	TYPE	TECHNOLOGY					VOLUME
		STD TTL	ALS	AS	LS	S	
Quadruple Complementary-Output Logic Elements	'265	●					2
Dual Pulse Synchronizers/Drivers	'120	●					
Crystal-Controlled Oscillators	'320				●		
	'321				●		
Digital Phase-Lock Loop	'297				●		
Programmable Frequency Dividers/Digital Timers	'292				●		
	'294				●		
Triple 4-Input AND/NAND Drivers	'800			▲			3
Triple 4-Input OR/NOR Drivers	'802			▲			
Dual VCO	'124					●	2

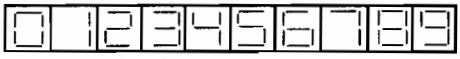
RESULTANT DISPLAYS USING '46A, '47A, '48, '49, 'L46, 'L47, 'LS47, 'LS48, 'LS49, 'LS347



RESULTANT DISPLAYS USING '246, '247, '248, '249, 'LS247, 'LS248, 'LS249, 'LS447



RESULTANT DISPLAYS USING '143, '144



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COMPARATORS AND ERROR DETECTION CIRCUITS

4-BIT COMPARATORS

DESCRIPTION					TYPE	TECHNOLOGY						VOLUME
P = Q	P > Q	P < Q	OUTPUT	OUTPUT ENABLE		STD TTL	ALS	AS	L	LS	S	
Yes	Yes	No	2-State	Yes	'85	●			●	●	●	2

8-BIT COMPARATORS

DESCRIPTION							TYPE	TECHNOLOGY			VOLUME
INPUTS	P = Q	$\overline{P=Q}$	P > Q	P < Q	OUTPUT	OUTPUT ENABLE		ALS	AS	LS	
20-kΩ Pull-Up	Yes	No	No	No	OC	Yes	'518	●			3
	No	Yes	No	No	2-State	Yes	'520	●			
	No	Yes	No	No	OC	Yes	'522	●			
	Yes	No	Yes	No	2-State	No	'682			●	2
	Yes	No	Yes	No	OC	No	'683			●	
Standard	Yes	No	No	No	OC	Yes	'519	●			3
	No	Yes	No	No	2-State	Yes	'521	●			
	Yes	No	Yes	No	2-State	No	'684			●	2
	Yes	No	Yes	No	OC	No	'685			●	
	Yes	No	Yes	No	2-State	Yes	'686			●	
	Yes	No	Yes	No	OC	Yes	'687			●	
	No	Yes	No	Yes	2-State	Yes	'688	●			3
										●	2
	No	Yes	No	No	OC	Yes	'689	●			3
										●	2
Latched P	No	No	Yes	Yes	2-State	Yes	'885		●		3
Latched P and Q	Yes	No	Yes	Yes	Latched	Yes	'866		●		

ADDRESS COMPARATORS

DESCRIPTION	OUTPUT ENABLE	LATCHED OUTPUT	TYPE	TECHNOLOGY		VOLUME
				ALS	AS	
16-Bit to 4-Bit	Yes		'677	●		3S
		Yes	'678	●		
12-Bit to 4-Bit	Yes		'679	●		
		Yes	'680	●		

PARITY GENERATORS/CHECKERS, ERROR DETECTION AND CORRECTION CIRCUITS

DESCRIPTION		NO. OF BITS	TYPE	TECHNOLOGY					VOLUME
				STD TTL	ALS	AS	LS	S	
Odd/Even Parity Generators/Checkers		8	'180	●					2
		9	'280			●	●		
						▲			3
		9	'286			▲			3
Parallel Error Detection/Correction Circuits	3-State	8	'636				●		2
	OC	8	'637				●		
	3-State	16	'616		▲				CF
	OC	16	'617		▲				
	3-State	16	'630				●		2
	OC	16	'631				●		
	3-State	32	'632		●				3
	OC	32	'633		▲				
	3-State	32	'634		▲				
	OC	32	'635		▲				

FUSE-PROGRAMMABLE COMPARATORS

DESCRIPTION	TYPE	TECHNOLOGY					VOLUME
		STD TTL	ALS	AS	LS	S	
16-Bit Identity Comparator	'526		▲				3
12-Bit identity Comparator	'528		▲				
8-Bit Identity Comparator and 4-Bit Comparator	'527		▲				

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ARITHMETIC CIRCUITS AND PROCESSOR ELEMENTS

PARALLEL BINARY ADDERS

DESCRIPTION	TYPE	TECHNOLOGY						VOLUME
		STD TTL	ALS	AS	H	LS	S	
1-Bit Gated	'80	●						2
2-Bit	'82	●						
4-Bit	'83	A				A		
	'283	●				●	●	
Dual 1-Bit Carry-Save	'183				●	●		

ACCUMULATORS, ARITHMETIC LOGIC UNITS, LOOK-AHEAD CARRY GENERATORS

DESCRIPTION		TYPE	TECHNOLOGY					VOLUME
			STD TTL	ALS	AS	LS	S	
4-Bit parallel Binary Accumulators		'281					●	2
		'681				●		
4-Bit Arithmetic Logic Units/ Function Generators		'181	●			●	●	3
					A			
		'381				A		2
							●	
		'881			A			3
4-Bit Arithmetic Logic Unit with Ripple Carry		'382				●		2
Look-Ahead Carry Generators	16-Bit	'182	●				●	2
					▲			3
		'282			▲			
	32-Bit	'882			●			3
Quad Serial Adder/Subtractor		'385				●		2
4-Bit Slice Elements		'481				●		4
8-Bit Slice Elements		'888			▲			

MULTIPLIERS

DESCRIPTION	TYPE	TECHNOLOGY					VOLUME
		STD TTL	ALS	AS	LS	S	
2-Bit-by-4-Bit Parallel Binary Multipliers	'261				●		2
4-Bit-by-4-Bit Parallel Binary Multipliers	'274					●	
	'284	●					
	'285	●					
25-MHz 6-Bit Binary Rate Multipliers	'97	●					
25-MHz Decade Rate Multipliers	'167	●					
8-Bit × 1-Bit 2's Complement Multipliers	'384				●		
16-Bit Parallel Multiplier	'1616		▲				4

OTHER ARITHMETIC OPERATORS

DESCRIPTION	TYPE	TECHNOLOGY							VOLUME
		STD TTL	ALS	AS	H	L	LS	S	
Quad 2-Input Exclusive-OR Gates with Totem-Pole Outputs	'86	●				●	A	●	2
	'386		●				A		3S
Quad 2-Input Exclusive-OR Gates with Open-Collector Outputs	'136	●						●	2
			●						3S
Quad 2-Input Exclusive-NOR Gates	'266						●		2
	'810		●	▲					3S
Quad 2-Input Exclusive-NOR Gates with Open-Collector Outputs	'811		●	▲					3S
Quad Exclusive OR/NOR Gates	'135							●	2
4-Bit True/Complement, Element	'87				●				

BIPOLAR BIT-SLICE PROCESSOR ELEMENTS

DESCRIPTION	CASCADABLE TO N-BITS	TYPE	TECHNOLOGY				VOLUME
			ALS	AS	LS	S	
4-Bit-Slice	Yes	'481			●	●	4
8-Bit-Slice	Yes	'888		▲			

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MEMORIES

USER-PROGRAMMABLE READ-ONLY MEMORIES (PROM's)

STANDARD PROM's

DESCRIPTION	TYPE	ORGANIZATION	TYPE OUTPUT	S	VOLUME
16K-Bit Arrays	TBP28S166	2048W × 8B	3-State	●	4
	TBP38S165	2048W × 8B	3-State	▲	
	TBP38S166	2048W × 8B	3-State	▲	
	TBP38SA165	2048W × 8B	OC	▲	
	TBP38SA166	2048W × 8B	OC	▲	
8K-Bit Arrays	TBP24S81	2048W × 4B	3-State	●	
	TBP24SA81	2048W × 4B	OC	●	
	TBP28S85A	1024W × 8B	3-State	▲	
	TBP28S86A	1024W × 8B	3-State	●	
	TBP28SA86A	1024W × 8B	OC	●	
4K-Bit Arrays	TBP24S41	1024W × 4B	3-State	●	
	TBP24SA41	1024W × 4B	OC	●	
	TBP28S42	512W × 8B	3-State	●	
	TBP28SA42	512W × 8B	OC	●	
	TBP28S46	512W × 8B	3-State	●	
	TBP28SA46	512W × 8B	OC	●	
1K-Bit Arrays	TBP24S10	256W × 4B	3-State	●	
	TBP24SA10	256A × 4B	OC	●	
256-Bit Arrays	TBP18S030	32W × 8B	3-State	●	
	TBP18SA030	32W × 8B	OC	●	
	TBP38S030	32W × 8B	3-State	▲	
	TNP38SA030	32W × 8B	OC	▲	

LOW-POWER PROM's

DESCRIPTION	TYPE	ORGANIZATION	TYPE OUTPUT	S	VOLUME
16K-Bit Arrays	TBP28L166	2048W × 8B	3-State	●	4
	TBP38L165	2048W × 8B	3-State	▲	
	TBP38L166	2048W × 8B	3-State	▲	
8K-Bit Arrays	TBP28L85A	1024W × 8B	3-State	▲	
	TBP28L86A	1024W × 8B	3-State	●	
4K-Bit Arrays	TBP28L42	512W × 8B	3-State	●	
	TBP28L46	512W × 8B	3-State	●	
2K-Bit Arrays	TBP28L22	256W × 8B	3-State	●	
	TBP28LA22	256W × 8B	OC	●	
256-Bit Arrays	TBP38L030	32W × 8B	3-State	▲	

READ-ONLY MEMORIES (ROM's)

DESCRIPTION	ORGANIZATION	TYPE OF OUTPUT	TYPE	TECHNOLOGY				VOLUME
				STD TTL	ALS	AS	S	
1024-Bit Arrays	256 × 4	OC	'187	●				4
256-Bit Arrays	32 × 8	OC	'88	A				

RANDOM-ACCESS READ-WRITE MEMORIES (RAM's)

DESCRIPTION	ORGANIZATION	TYPE OF OUTPUT	TYPE	TECHNOLOGY					VOLUME
				STD TTL	ALS	AS	LS	S	
256-Bit Arrays	256 × 1	3-State	'201					●	4
		OC	'301					●	
64-Bit Arrays	16 × 4	OC	'89	●					
		3-State	'189				A	B	
		3-State	'219				A		
		OC	'289				A	B	
		OC	'319				A		
16-Bit Multiple-Port Register File	8 × 2	3-State	'172	●					2
16-Bit Register File	4 × 4	OC	'170	●			●		
		3-State	'670				●		
Dual 64-Bit Register Files	16 × 4	3-State	'870			●			3
			'871			●			

FIRST-IN FIRST-OUT MEMORIES (FIFO'S)

DESCRIPTION	TYPE OF OUTPUT	TYPE	TECHNOLOGY				VOLUME
			ALS	AS	LS	S	
16 Words × 5 Bits	3-State	'225				●	4
16 Words × 4 Bits	3-State	'222			●		
	3-State	'224			●		
	OC	'227			●		
	OC	'228			●		
64 Words × 5 Bits	3-State	'7403	▲				
64 Words × 4 Bits	3-State	'236	▲				
	2-State	'7401	▲				

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PROGRAMMABLE LOGIC ARRAYS

PROGRAMMABLE LOGIC ARRAYS

DESCRIPTION	INPUTS	OUTPUTS NO.	OUTPUTS TYPE	TYPE NO	ALS	NO. OF PINS	VOLUME
Impact PAL*	16	8	Active-Low	*PAL16L8-15	●	20	
		4	Registered	*PAL16R4-15	●		
		6		*PAL16R6-15	●		
		8		*PAL16R8-15	●		
High-Performance PAL*	16	8	Active-Low	*PAL16L8A	●	20	
		4	Registered	*PAL16R4A	●		
		6		*PAL16R6A	●		
		8		*PAL16R8A	●		
Half-Power PAL*	16	8	Active-Low	*PAL16L8A-2	●	20	
		4	Registered	*PAL16R4A-2	●		
		6		*PAL16R6A-2	●		
		8		*PAL16R8A-2	●		
High-Performance PAL*	20	8	Active-Low	*PAL20L8A	▲	24	
		4	Registered	*PAL20R4A	▲		
		6		*PAL20R6A	▲		
		8		*PAL20R8A	▲		
Half-Power PAL*	20	8	Active-Low	*PAL20L8A-2	▲	24	
		4	Registered	*PAL20R4A-2	▲		
		6		*PAL20R6A-2	▲		
		8		*PAL20R8A-2	▲		
Exclusive-OR PAL*	20	10	Active-Low	*PAL20L10-20	▲	24	4
		4	Registered	*PAL20X4-20	▲		
		8		*PAL20X8-20	▲		
		10		*PAL20X10-20	▲		
Exclusive-OR PAL*	20	8	Active-Low	*PAL20L10-35	▲	24	
		4	Registered	*PAL20X4-35	▲		
		8		*PAL20X8-35	▲		
		10		*PAL20X10-35	▲		
Registered-Input PAL*	19	8	Active-Low	*PALR19L8-25	▲	24	
		4	Registered	*PALR19R4-25	▲		
		6		*PALR19R6-25	▲		
		8		*PALR19R8-25	▲		
Registered-Input PAL*	19	8	Active-Low	*PALR19L8-40	▲	24	
		4	Registered	*PALR19R4-40	▲		
		6		*PALR19R6-40	▲		
		8		*PALR19R8-40	▲		
Latched-Input PAL*	19	8	Active-Low	*PALT19L8-25	▲	24	
		4	Registered	*PALT19R4-25	▲		
		6		*PALT19R6-25	▲		
		8		*PALT19R8-25	▲		
Latched-Input PAL*	19	8	Active-Low	*PALT19L8-40	▲	24	
		4	Registered	*PALT19R4-40	▲		
		6		*PALT19R6-40	▲		
		8		*PALT19R8-40	▲		
Field-Programmable 14×32×6 Logic Arrays	14	6	3-State	*PL839	●	24	
			OC	*PL840	●		

*PAL is a registered trademark of Monolithic Memories Incorporated.

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▲ Denotes planned new products.

Revisions to the TTL Data Book, Volume 3, 1984

<table>
<tr><th>PAGE</th><th>DATA SHEET</th><th>CHANGE</th></tr>
<tr><td>v</td><td>Third paragraph, second line</td><td>The word "connection" to correction.</td></tr>
<tr><td>2-27 and 2-28</td><td>'ALS10</td><td>Revised to 'ALS10A. Data sheet printed in the Supplement to the TTL Data Book, Volume 3, 1984.</td></tr>
<tr><td>2-31 and 2-32</td><td>'ALS11</td><td>Revised to 'ALS11A. Data sheet printed in the Supplement to the TTL Data Book, Volume 3, 1984.</td></tr>
<tr><td>2-35 and 2-36</td><td>'ALS12</td><td>Revised to 'ALS12A. Data sheet printed in the Supplement to the TTL Data Book, Volume 3, 1984.</td></tr>
<tr><td>2-47 and 2-48</td><td>'ALS22A</td><td>Revised to 'ALS22B. Data sheet printed in the Supplement to the TTL Data Book, Volume 3, 1984.</td></tr>
<tr><td>2-55 and 2-56</td><td>'ALS30</td><td>Revised to 'ALS30A. Data sheet printed in the Supplement to the TTL Data Book, Volume 3, 1984.</td></tr>
<tr><td>2-69 and 2-70</td><td>'ALS35</td><td>Production released. Data sheet printed in the Supplement to the TTL Data Book, Volume 3, 1984.</td></tr>
<tr><td>2-77 and 2-78</td><td>'ALS74</td><td>Revised to 'ALS74A. Data sheet printed in the Supplement to the TTL Data Book, Volume 3, 1984.</td></tr>
<tr><td>2-79</td><td>'AS74</td><td>electrical characteristics: I_{IH} and I_{IL} parameters to the following:
<table>
<tr><td>I_{IH}</td><td>CLK or D</td><td rowspan="2">V_{CC} = 5.5 V, V_I = 2.7 V</td><td>20</td><td>20</td><td rowspan="2">μA</td></tr>
<tr><td>$\overline{PRE}$ or $\overline{CLR}$</td><td>40</td><td>40</td></tr>
<tr><td>I_{IL}</td><td>CLK or D</td><td rowspan="2">V_{CC} = 5.5 V, V_I = 0.4 V</td><td>−0.5</td><td>−0.5</td><td rowspan="2">mA</td></tr>
<tr><td>$\overline{PRE}$ or $\overline{CLR}$</td><td>−1.8</td><td>−1.8</td></tr>
</table></td></tr>
<tr><td>2-81 and 2-82</td><td>'ALS86</td><td>Production released. Data sheet printed in the Supplement to the TTL Data Book, Volume 3, 1984.</td></tr>
<tr><td>2-83 and 2-84</td><td>'AS95</td><td>Production released. Data sheet printed in the Supplement to the TTL Data Book, Volume 3, 1984.</td></tr>
<tr><td>2-87 and 2-88</td><td>'ALS109</td><td>Revised to 'ALS109A. Data sheet printed in the Supplement to the TTL Data Book, Volume 3, 1984.</td></tr>
<tr><td>2-89</td><td>'AS109</td><td>electrical characteristics: I_{IH} and I_{IL} parameter to the following:
<table>
<tr><td>I_{IH}</td><td>CLK, J or K</td><td rowspan="2">V_{CC} = 5.5 V, V_I = 2.7 V</td><td>20</td><td>20</td><td rowspan="2">μA</td></tr>
<tr><td>$\overline{PRE}$ or $\overline{CLR}$</td><td>40</td><td>40</td></tr>
<tr><td>I_{IL}</td><td>CLK, J or $\overline{K}$</td><td rowspan="2">V_{CC} = 5.5 V, V_I = 0.4 V</td><td>−0.5</td><td>−0.5</td><td rowspan="2">mA</td></tr>
<tr><td>$\overline{PRE}$ or $\overline{CLR}$</td><td>−1.8</td><td>−1.8</td></tr>
</table>
Note 1 to read, I_{CC} is measured with J, $\overline{K}$, CLK, and $\overline{PRE}$ grounded, then with J, $\overline{K}$, CLK, and $\overline{CLR}$ grounded.</td></tr>
<tr><td></td><td>'ALS136</td><td>New device. Data sheet printed in the Supplement to the TTL Data Book, Volume 3, 1984.</td></tr>
<tr><td>2-117</td><td>'AS139</td><td>Delete SN54AS139 and SN74AS139, 4 places each. Delete 'AS139, 2 places.</td></tr>
</table>

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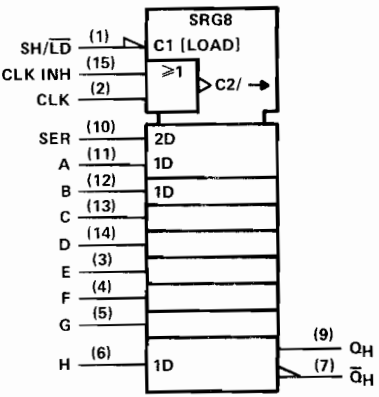
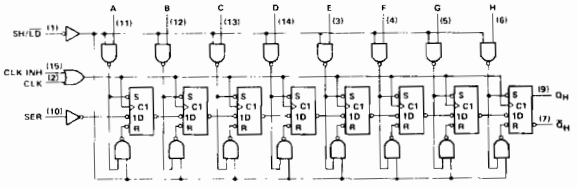
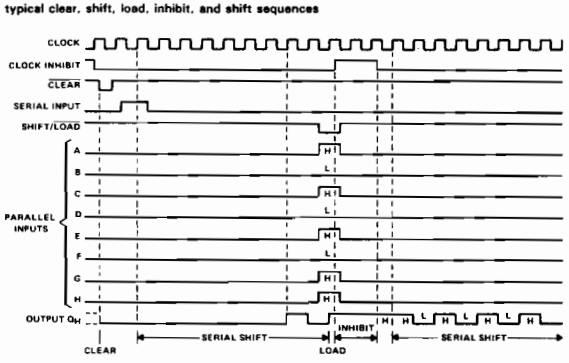
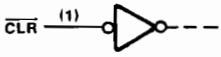
PAGE	DATA SHEET	CHANGE
2-118	'AS139	Delete SN54AS139 and SN74AS139, 2 places each.
2-120	'AS139	Delete page.
2-124	'AS151	Production released. Data sheet printed in the Supplement to the TTL Data Book, Volume 3, 1984.
2-139 and 2-141	'ALS/'AS161, 'ALS/'AS163	Title: **SYNCHRONOUS 4-BIT BINARY COUNTERS.**
2-140	'ALS/'AS160, 'ALS/'AS162	Title: **SYNCHRONOUS 4-BIT DECADE COUNTERS.**
2-144 and 2-145	'AS160 thru 'AS163	Production released. Data sheet printed in the Supplement to the TTL Data Book, Volume 3, 1984.
2-151	'ALS165	**logic symbol:** 
2-152	'ALS165	**logic diagram (positive logic)**  Pin numbers shown are for J and N packages.

PAGE	DATA SHEET	CHANGE
2-154	'ALS166	**timing diagram:** typical clear, shift, load, inhibit, and shift sequences 
2-157 thru 2-165	'ALS168A, 'ALS169A 'AS168, 'AS169	'ALS168A and 'ALS169A are revised to 'ALS168B and 'ALS169B. 'AS168 and 'AS169 are production released. New data sheet is printed in the Supplement to the TTL Data Book, Volume 3, 1984.
2-168	'ALS174, 'ALS175, 'AS174, and 'AS175	**logic diagrams:** The $\overline{CLR}$ input on both diagrams to the following: 
2-171 and 2-172	'AS175	'AS175 is production released. Data sheet is printed in the Supplement to the TTL Data Book, Volume 3, 1984.
2-185	'AS182	FH and FN Package: Pin 17 to C_n, Pin 15 to C_{n+x}, Pin 14 to C_{n+y}
2-186	'AS182	FUNCTION TABLES NOTE: First Note to, H = High level, L = Low level, X = Irrelevant
2-187	'AS182	**electrical characteristics:** I_{IL} parameter ($\overline{P}2$, $\overline{P}1$, $\overline{G}3$) to ($\overline{P}0$, $\overline{P}1$, $\overline{G}3$).
2-188	'AS182	**switching characteristics:** TI (Output) to TO (Output) output of first parameter from C_{n+y}, C_{n+y}, C_{n+z} to C_{n+x}, C_{n+y}, C_{n+z}

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PAGE	DATA SHEET	CHANGE
2-202	'ALS192, 'ALS193	**recommended operating conditions**: Add the following parameters: t_{su} Setup time UP high before DOWN↑ 17 ns MIN , 2 places DOWN high before UP↑ 15 ns MIN , 2 places The following parameters: t_h Hold time UP high after DOWN↑ from 0 ns MIN , 2 places to 5 ns MIN , 2 places DOWN high after UP↑ from 0 ns MIN , 2 places to 8 ns, MIN, 2 places
2-221	'AS240, 'AS241	Title: LILNE to LINE
2-225	'ALS242A	**switching characteristics**: Limit headings from SN54AS242A to SN54ALS242A from SN74AS242A to SN74ALS242A
2-226	'AS242, 'AS243	**electrical characteristics**: I_{IH} limits for A or B ports‡ from 50 μA MAX to 70 μA MAX, 2 places.
2-230	'ALS244A	**electrical characteristics**: Delete I_{IL} limit of −0.1 mA typ Add I_{IL} limit of −0.1 mA MAX
2-235	'ALS245A	**description**: In the first sentence, change the word synchronous to asynchronous.
2-241 thru 2-244	'AS250	Production released. Data sheet is printed in the Supplement of the TTL Data Book, Volume 3, 1984.
2-255 thru 2-260	'ALS257, 'ALS258, 'AS257, 'AS258	Title: **QUADRUPLE 1 OF 2 DATA SELECTORS/ MULTIPLEXERS WITH 3-STATE OUTPUTS**
2-258	'ALS258	**switching characteristics:** t_{PLH} / t_{PHL} | $\overline{A}$/B | Any Y | 8 23 / 5 28 | 8 20 / 5 25 | ns
2-263	'AS264	**positive logic equations**: For ACTIVE LOW-CARRY COUNTERS, change the equation CO = $\overline{B0}$ to CO = $\overline{\overline{B0}}$
2-267	'AS264	**TYPICAL APPLICATION INFORMATION**: In the first sentence, change 'AS624 to 'AS264.
2-271	'ALS273	**switching characteristics**: In the last line of the "FROM" column, change CLR to CLK.
2-278	'AS282	**logic diagram**: outputs (15) C_{n+x} to (11) C_{n+z} and (11) C_{n+z} to (15) C_{n+x}.
2-282	'AS286	**recommended operating conditions**: For the SN74AS286, change I_{OL} parity error limit of 10 mA MAX to 20 mA MAX
2-287 thru 2-290	'AS298	Production released. Data sheet is printed in the Supplement of the TTL Data Book, Volume 3, 1984.
2-294	'ALS299, 'ALS323	**electrical characteristics**: I_{IL} parameter: S0, S1, SR, SL to "All other" and "All other" to $\overline{G}1$, $\overline{G}2$, CLK, CLR.

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PAGE	DATA SHEET	CHANGE
2-295	'ALS299, 'ALS323	**switching characteristics**: t_{PLZ} (FROM) S0, S1 (TO) Q_A thru Q_H change limits from 8 ns MIN, 30 ns MAX to 3 ns MIN, 20 ns MAX for SN54ALS299 and SN54ALS323. Change limits from 8 ns MIN, 25 ns MAX to 3 ns MIN, 15 ns MAX for SN74ALS299 and SN74ALS323.
2-299	'ALS323, 'AS323	Add: 2-291 after, "see page ."
2-335	'ALS518, 'ALS519, 'ALS522	**electrical characteristics**: I_{OH} parameter: test condition V_{CC} = 4.5 V to V_{CC} = 5.5 V
2-385	'ALS564 'ALS564	**recommended operating conditions**:For the SN54ALS564 change f_{clock} from 30 MHz MAX to 25 MHz and for SN74ALS564 change from 35 MHz MAX to 30 MHz MAX. **switching characteristics**: f_{max} from 30 MIN to 25 MIN for the SN54ALS564 and from 35 MIN to 30 MIN for the SN74ALS564.
2-399	'ALS573	**recommended operating conditions**: t_w Pulse duration, enable C high from 10 ns MIN to 15 ns MIN, 2 places.
2-421 thru 2-424	'AS622, 'AS623	Production released. Data sheets printed in the Supplement of the TTL Data Book, Volume 3, 1984.
2-421	'AS620, 'AS623	**electrical characteristics**: I_{IH} limits (A or B ports) from 50 μA MAX to 70 μA MAX. I_O limits from −30 mA MIN, −112 mA MAX to −50 mA MIN, −150 mA MAX, 2 places.
2-423	'AS621, 'AS622	**electrical characteristics**: I_{IH} limits (A or B ports) from 20 μA MAX to 70 μA MAX. I_{IL} limits (A or B ports) from −0.5 mA MAX to −0.75 mA MAX.
2-424	'AS621, 'AS622	**switching characteristics**: R_L = 680 Ω to R_L = 500 Ω, 2 places.
2-430	'ALS634, 'ALS635	**TABLE 8**: In the third row of the "DB CONTROL $\overline{OE}CB$" column, change H to L.
2-431	'ALS632, 'ALS633	**logic diagram**: Last note below diagram. Change (◇) to (◇).
2-443	'AS638, 'AS639	**electrical characteristics**: I_{IH} limits (A or B ports) from 50 μA MAX to 70 μA MAX. I_O limits from −30 mA MIN, −112 mA MAX to −50 mA MIN, −150 mA MAX, 2 places.
2-444	'AS638, 'AS639	**switching characteristics**: R_L = 680 Ω (A outputs) to R_L = 500 Ω (A outputs) in 2 places.
2-451	'AS640, 'AS643, 'AS645	**electrical characteristics**: I_{IH} limits (A or B ports) from 50 μA MAX to 70 μA MAX. I_O limits from −30 mA MIN, −112 mA MAX to −50 mA MIN, −150 mA MAX, 2 places.
2-453	'AS641, 'AS642, 'AS644	**electrical characteristics**: I_{IH} limits (A or B ports) from 50 μA MAX to 70 μA MAX, 2 places.

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PAGE	DATA SHEET	CHANGE
2-454	'AS641, 'AS642, 'AS644	**switching characteristics**: R_L = 680 Ω to R_L = 500 Ω, 3 places. Delete Product Preview at bottom of page.
2-455	'ALS646 thru 'ALS648, 'AS646, 'AS648	**Bus-Management functions diagrams**: REAL-TIME TRANSFER BUS B TO BUS A. Under CBA change X to H or L. REAL-TIME TRANSFER BUS A TO BUS B, under CAB change X to H or L.
2-456	'ALS646 thru 'ALS648, 'AS646, 'AS648	**FUNCTION TABLE**: In the fifth row of the ''CAB'' column, change X to H or L. In the last row of the ''CAB'' column, change X to H or L.
2-462	'AS646, 'AS648	**electrical characteristics**: V_{OH} limit (I_{OH} = −12 mA) from 2.4 V MIN to 2 V MIN. V_{OH} limit (I_{OH} = −15 mA) from 2.4 V MIN to 2 V MIN. I_{IH} limit (A or B port) from 50 μA MAX to 70 μA MAX, 2 places. I_{IL} limit (A or B port) from −0.5 mA MAX to −0.75 mA MAX, 2 places.
2-465	'ALS651 thru 'ALS654, 'AS651, 'AS652	**Bus-Management function diagrams**: TRANSFER STORED DATA TO A AND/OR B, under SBA change X to H.
2-467	'ALS652, 'AS652, 'ALS654	**logic symbols**: Inside of the control blocks of both logic diagrams. Change G6 to G5.
2-473	'AS651, 'AS652	**electrical characteristics**: V_{OH} limit (I_{OH} = −12 mA) from 2.4 V MIN to 2 V MIN. V_{OH} limit (I_{OH} = −15 mA) from 2.4 V MIN to 2 V MIN. I_{IH} limit (A or B ports) from 50 μA MAX to 70μA MAX, 2 places. I_{IL} limit (A or B ports) from −0.5 mA MAX to −0.75 mA MAX, 2 places.
2-475 thru 2-480	'ALS678	Production released. Data sheet printed in the Supplement of the TTL Data Book, Volume 3, 1984.
2-479	'ALS677	**switching characteristics**: T_{PHL} limits (FROM) Any A, (TO) Y from 35 ns MAX to 40 ns MAX for SN54ALS677, and from 30 ns MAX to 35 ns MAX for SN74ALS677.
2-481 thru 2-486	'ALS680	Production released. Data sheet printed in the Supplement of the TTL Data Book, Volume 3, 1984.
2-490	'ALS689	**electrical characteristics**: I_{OH} parameter, change test condition V_{CC} = 4.5 V to V_{CC} = 5.5 V.
2-491 thru 2-503	'AS756 'AS757, 'AS758, 'AS759, 'AS760, 'AS762, 'AS763	Production released. Data sheets are printed in the Supplement of the TTL Data Book, Volume 3, 1984.
2-515	'AS804A	**switching characteristics**: All MIN limits from 2 ns to 1 ns.
	'ALS810 'ALS811	New devices. Data sheets are printed in the Supplement of the TTL Data Book, Volume 3, 1984.

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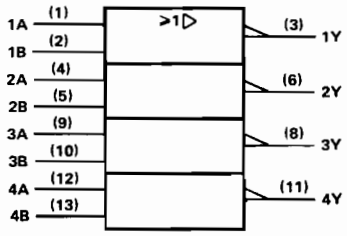
PAGE	DATA SHEET	CHANGE
2-552 and 2-553	'AS841, 'AS842	Production released. Data sheet is printed in the Supplement of the TTL Data Book, Volume 3, 1984.
2-560 and 2-561	'AS843, 'AS844	Production released. Data sheet is printed in the Supplement of the TTL Data Book, Volume 3, 1984.
2-566 and 2-567	'AS845	Production released. Data sheet is printed in the Supplement of the TTL Data Book, Volume 3, 1984.
2-571 thru 2-580	'AS850, 'AS851	Production released. Data sheet is printed in the Supplement of the TTL Data Book, Volume 3, 1984.
2-579	'AS850	**TYPICAL APPLICATION:** In the drawing, the E input is connected to the input of an inverter. The output of the inverter is connected to $\overline{G}$ inputs of two separate 'AS850s. Change this part of the drawing as follows: The E input is connected directly to the $\overline{G}$ input of the top 'AS850. The E input is also connected to the input of an inverter. The output of the inverter is connected to the $\overline{G}$ input of the bottom 'AS850.
2-598	'AS857	**electrical characteristics:** I_O limits from −30 mA MIN, −112 mA MAX to −50 mA MIN, −150 mA MAX, 2 places.
2-621	'ALS873	**recommended operating conditions:** t_w Pulse duration (Enable C high) limit from 10 ns MIN to 15 ns MIN, 2 places.
2-631 thru 2-636	'AS877	Production released. Data sheet is printed in the Supplement of the TTL Data Book, Volume 3, 1984.
2-697	'AS1036	**logic symbol:** Replace the logic symbol with the following: 
2-711 thru 2-713	'ALS1245	Revised to 'ALS1245A. Data sheet is printed in the Supplement to the TTL Data Book, Volume 3, 1984.
2-733	'AS2620, 'AS2623	**electrical characteristics:** I_{IH} limits (A or B port) from 50 μA MAX to 70 μA MAX, 2 places. I_{IL} limits (A or B port) from −0.5 mA MAX to −0.75 mA MAX, 2 places. I_O limits from −30 mA MIN, −112 mA MAX to −50 mA MIN, −150 mA MAX, 2 places.

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PAGE	DATA SHEET	CHANGE
2-737	'AS2640, 'AS2645	**electrical characteristics:** I_{IH} limits (A or B port) from 50 μA MAX to 70μA MAX, 2 places. I_{IL} limits (A or B port) from −0.5 mA MAX to −0.75 mA MAX, 2 places. I_O limits from −30 mA MIN, −112 mA MAX to −50 mA MIN, −150 mA MAX, 2 places.

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2

ALS AND AS CIRCUITS

March 1984

- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

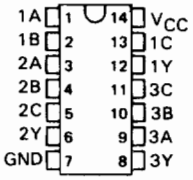
These devices contain three independent 3-input NAND gates. They perform the Boolean functions $Y = \overline{A \cdot B \cdot C}$ or $Y = \overline{A} + \overline{B} + \overline{C}$ in positive logic.

The SN54ALS10A and SN54AS10 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS10A and SN74AS10 are characterized for operation from 0°C to 70°C.

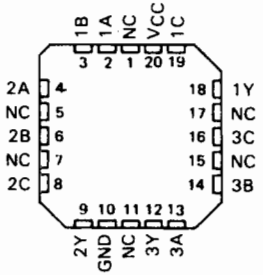
FUNCTION TABLE (each gate)

INPUTS			OUTPUT
A	B	C	Y
H	H	H	L
L	X	X	H
X	L	X	H
X	X	L	H

SN54ALS10A, SN54AS10 . . . J PACKAGE
SN74ALS10A, SN74AS10 . . . N PACKAGE
(TOP VIEW)

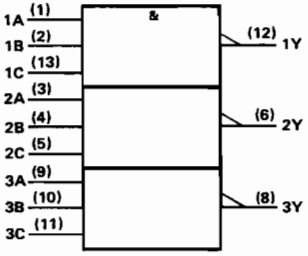


SN54ALS10A, SN54AS10 . . . FH PACKAGE
SN74ALS10A, SN74AS10 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

logic symbol



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS10A . . . . . −55 °C to 125 °C
SN74ALS10A . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS10A			SN74ALS10A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS10A			SN74ALS10A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		0.32	0.6		0.32	0.6	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		1.2	2.2		1.2	2.2	mA

†All typical values are at V_{CC} = 5 V, T_A = 25 °C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS10A		SN74ALS10A		
			MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	2	13	2	11	ns
t_{PHL}	Any	Y	2	12	2	10	ns

NOTE 1: For load circuit and voltage waveforms, see page 1-12 of The TTL Data Book, Volume 3.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS10 . . . . . −55 °C to 125 °C
SN74AS10 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54AS10			SN74AS10			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−2			−2	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS10			SN74AS10			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5		0.35	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		1.5	2.4		1.5	2.4	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		8.1	13		8.1	13	mA

†All typical values are at V_{CC} = 5 V, T_A = 25 °C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS10		SN74AS10		
			MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	1	5	1	4.5	ns
t_{PHL}	Any	Y	1	5	1	4.5	ns

NOTE 1: For load circuit and voltage waveforms, see page 1-12 of The TTL Data Book, Volume 3.

March 1984

- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

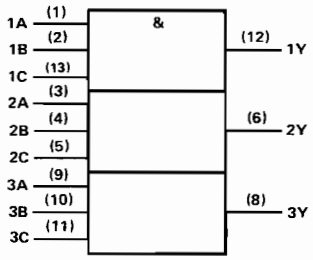
These devices contain three independent 3-input AND gates. They perform the Boolean functions $Y = A \cdot B \cdot C$ or $Y = \overline{\overline{A}+\overline{B}+\overline{C}}$ in positive logic.

The SN54ALS11A and SN54AS11 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS11A and SN74AS11 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

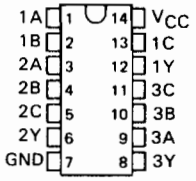
INPUTS			OUTPUT
A	B	C	Y
H	H	H	H
L	X	X	L
X	L	X	L
X	X	L	L

logic symbol

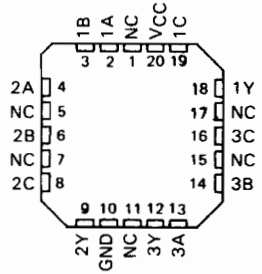


Pin numbers shown are for J and N packages.

SN54ALS11A, SN54AS11 . . . J PACKAGE
SN74ALS11A, SN74AS11 . . . N PACKAGE
(TOP VIEW)



SN54ALS11A, SN54AS11 . . . FH PACKAGE
SN74ALS11A, SN74AS11 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS11A . . . . . −55 °C to 125 °C
SN74ALS11A . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS11A			SN74ALS11A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS11A			SN74ALS11A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4.5 V		1	1.8		1	1.8	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0 V		1.6	3		1.6	3	mA

† All typical values are at V_{CC} = 5 V, T_A = 25 °C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS11A		SN74ALS11A		
			MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	2	16	2	13	ns
t_{PHL}	Any	Y	2	12	2	10	ns

NOTE 1: For load circuit and voltage waveforms, see page 1-12 of The TTL Data Book, Volume 3.

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POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS11 . . . . . −55 °C to 125 °C
SN74AS11 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54AS11			SN74AS11			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−2			−2	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS11			SN74AS11			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5		0.35	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4.5 V		4.3	7		4.3	7	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0 V		11.2	18		11.2	18	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS11		SN74AS11		
			MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	1	6.5	1	6	ns
t_{PHL}	Any	Y	1	6.5	1	5.5	ns

NOTE 1: For load circuit and voltage waveforms, see page 1-12 of The TTL Data Book, Volume 3.

MARCH 1984

- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

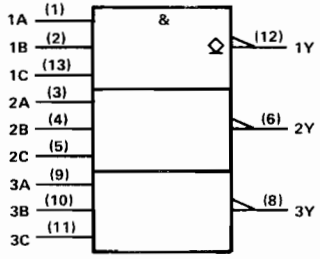
These devices contain three independent 3-input NAND gates with open-collector outputs. These gates perform the Boolean functions $Y = \overline{A \cdot B \cdot C}$ or $Y = \overline{A}+\overline{B}+\overline{C}$ in positive logic. The open-collector outputs require pull-up resistors to perform correctly. They may be connected to other open-collector outputs to implement active-low wired-OR or active-high wired-AND functions. Open-collector devices are often used to generate higher V_{OH} levels.

The SN54ALS12A is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS12A is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

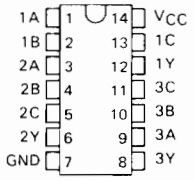
INPUTS			OUTPUT
A	B	C	Y
H	H	H	L
L	X	X	H
X	L	X	H
X	X	L	H

logic symbol

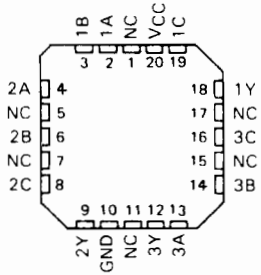


Pin numbers shown are for J and N packages.

SN54ALS12A . . . J PACKAGE
SN74ALS12A . . . N PACKAGE
(TOP VIEW)



SN54ALS12A . . . FH PACKAGE
SN74ALS12A . . . FN PACKAGE
(TOP VIEW)



NC No internal connection

2

ALS AND AS CIRCUITS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS12A . . . . . −55°C to 125°C
SN74ALS12A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS12A			SN74ALS12A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS12A			SN74ALS12A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
I_{OH}	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		0.32	0.6		0.32	0.6	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		1.2	2.2		1.2	2.2	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 2 kΩ, T_A = MIN to MAX				UNIT
			SN54ALS12A		SN74ALS12A		
			MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	23	59	23	54	ns
t_{PHL}	Any	Y	5	22	5	18	ns

NOTE 1: For load circuit and voltage waveforms, see page 1-12 of the TTL Data Book, Volume 3.

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- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

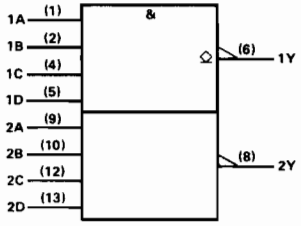
These devices contain two independent 4-input NAND gates. These gates perform the Boolean functions $Y = \overline{A \cdot B \cdot C \cdot D}$ or $Y = \overline{A} + \overline{B} + \overline{C} + \overline{D}$ in positive logic. The open-collector outputs require pull-up resistors to perform correctly. They may be connected to other open-collector outputs to implement active-low wired-OR or active-high wired-AND functions. Open-collector devices are often used to generate higher V_{OH} levels.

The SN54ALS22B is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS22B is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

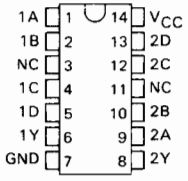
INPUTS				OUTPUT
A	B	C	D	Y
H	H	H	H	L
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H

logic symbol

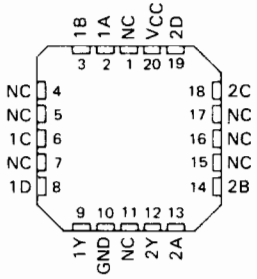


Pin numbers shown are for J and N packages.

SN54ALS22B . . . J PACKAGE
SN74ALS22B . . . N PACKAGE
(TOP VIEW)



SN54ALS22B . . . FH PACKAGE
SN74ALS22B . . . FN PACKAGE
(TOP VIEW)



NC — No internal connection

2

ALS AND AS CIRCUITS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS22B . . . . . −55 °C to 125 °C
SN74ALS22B . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS22B			SN74ALS22B			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS22B			SN74ALS22B			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
I_{OH}	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		0.22	0.4		0.22	0.4	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		0.8	1.5		0.8	1.5	mA

†All typical values are at V_{CC} = 5 V, T_A = 25 °C

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 2 kΩ, T_A = MIN to MAX				UNIT
			SN54ALS22B		SN74ALS22B		
			MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	23	50	23	45	ns
t_{PHL}	Any	Y	4	21	4	18	ns

NOTE 1: For load circuit and voltage waveforms, see page 1-12 of The TTL Data Book, Volume 3.

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March 1984

- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These devices contain a single 8-input NAND gate and perform the following Boolean functions in positive logic:

$$Y = \overline{A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H} \text{ OR}$$

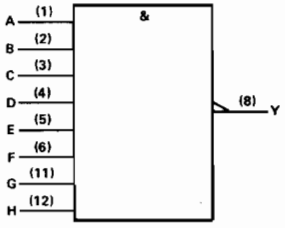
$$Y = \overline{A} + \overline{B} + \overline{C} + \overline{D} + \overline{E} + \overline{F} + \overline{G} + \overline{H}$$

The SN54ALS30A and SN54AS30 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS30A and SN74AS30 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE

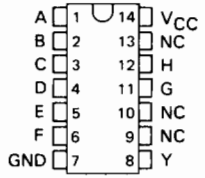
INPUTS A THRU H	OUTPUT Y
All inputs H	L
One or more inputs L	H

logic symbol

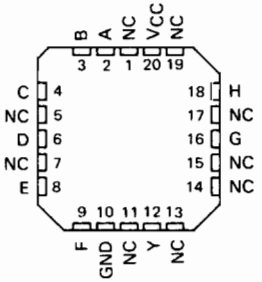


Pin numbers shown are for J and N packages.

SN54ALS30A, SN54AS30 . . . J PACKAGE
SN74ALS30A, SN74AS30 . . . N PACKAGE
(TOP VIEW)



SN54ALS30A, SN54AS30 . . . FH PACKAGE
SN74ALS30A, SN74AS30 . . . FN PACKAGE
(TOP VIEW)



NC – No internal connection

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS30A . . . . . −55 °C to 125 °C
SN74ALS30A . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS30A			SN74ALS30A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS30A			SN74ALS30A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		0.22	0.36		0.22	0.36	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		0.54	0.9		0.54	0.9	mA

† All typical values are at V_{CC} = 5 V, T_A = 25 °C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS30A		SN74ALS30A		
			MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	3	12	3	10	ns
t_{PHL}	Any	Y	3	15	3	12	ns

NOTE 1: For load circuit and voltage waveforms, see page 1-12 of The TTL Data Book, Volume 3.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS30 . . . . . −55 °C to 125 °C
SN74AS30 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54AS30			SN74AS30			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−2			−2	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS30			SN74AS30			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5		0.35	0.5	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 0 V		0.9	1.5		0.9	1.5	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 4.5 V		3	4.9		3	4.9	mA

† All typical values are at V_{CC} = 5 V, T_A = 25 °C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS30		SN74AS30		
			MIN	MAX	MIN	MAX	
t_{PLH}	Any	Y	1	5.5	1	5	ns
t_{PHL}	Any	Y	1	5	1	4.5	ns

NOTE 1: For load circuit and voltage waveforms, see page 1-12 of The TTL Data Book, Volume 3.

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ALS AND AS CIRCUITS

D2661, DECEMBER 1983—REVISED MARCH 1984

- **Noninverters with Open-Collector Outputs**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

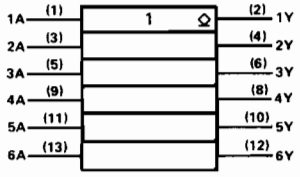
These devices contain six independent noninverters. They perform the Boolean functions Y = A. The open-collector outputs require pull-up resistors to perform correctly. They may be connected to other open-collector outputs to implement active-low wired-OR or active-high wired-AND functions. Open-collector devices are often used to generate higher V_{OH} levels.

The SN54ALS35 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS35 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each buffer)

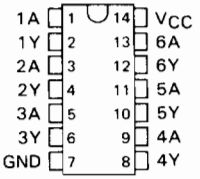
INPUT A	OUTPUT Y
H	H
L	L

logic symbol

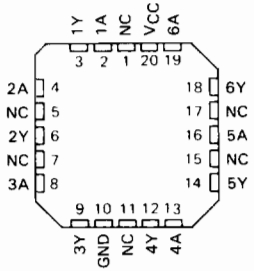


Pin numbers shown are for J and N packages.

SN54ALS35 . . . J PACKAGE
SN74ALS35 . . . N PACKAGE
(TOP VIEW)



SN54ALS35 . . . FH PACKAGE
SN74ALS35 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

2

ALS AND AS CIRCUITS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS35 . . . . . −55 °C to 125 °C
SN74ALS35 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS35			SN74ALS35			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS35			SN74ALS35			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
I_{OH}	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_{CCH}	V_{CC} = 5.5 V,	V_I = 4.5 V		2.7	4.1		2.7	4.1	mA
I_{CCL}	V_{CC} = 5.5 V,	V_I = 0 V		4.1	6.3		4.1	6.3	mA

† All typical values are at V_{CC} = 5 V, T_A = 25 °C

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 680 Ω, T_A = MIN to MAX				UNIT
			SN54ALS35		SN74ALS35		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	20	55	20	50	ns
t_{PHL}	A	Y	2	15	2	12	ns

NOTE 1: For load circuit and voltage waveforms, see page 1-12 of the TTL Data Book, Volume 3.

TEXAS INSTRUMENTS
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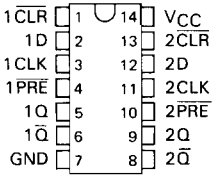
D2661, APRIL 1982—REVISED FEBRUARY 1984

- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY (C_L = 50 pF)	TYPICAL POWER DISSIPATION PER FLIP-FLOP
'ALS74A	50 MHz	6 mW
'AS74	134 MHz	26 mW

SN54ALS74A, SN54AS74 . . . J PACKAGE
SN74ALS74A, SN74AS74 . . . N PACKAGE
(TOP VIEW)

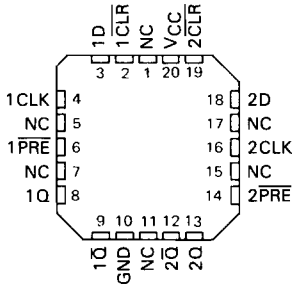


description

These devices contain two independent D-type positive-edge-triggered flip-flops. A low level at the Preset or Clear inputs sets or resets the outputs regardless of the levels of the other inputs. When Preset and Clear are inactive (high), data at the D input meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the D input may be changed without affecting the levels at the outputs.

The SN54ALS74A and SN54AS74 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS74A and SN74AS74 are characterized for operation from 0°C to 70°C.

SN54ALS74A, SN54AS74 . . . FH PACKAGE
SN74ALS74A, SN74AS74 . . . FN PACKAGE
(TOP VIEW)



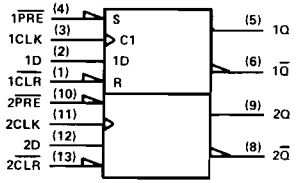
NC—No internal connection

FUNCTION TABLE

INPUTS				OUTPUTS	
PRESET	CLEAR	CLOCK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

* The output levels in this configuration are not guaranteed to meet the minimum levels for V_{OH} if the lows at Preset and Clear are near V_{IL} maximum. Furthermore, this configuration is nonstable; that is, it will not persist when either Preset or Clear returns to its inactive (high) level.

logic symbol



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS74A, SN54AS74 . . . . . −55°C to 125°C
SN74ALS74A, SN74AS74 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS74A			SN74ALS74A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−0.4			−0.4	mA
I_{OL}	Low-level output current				4			8	mA
f_{clock}	Clock frequency		0		30	0		34	MHz
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	15			15			ns
		CLK high	16.5			14.5			
		CLK low	16.5			14.5			
t_{su}	Setup time before CLK↑	Data	15			15			ns
		$\overline{PRE}$ or $\overline{CLR}$ inactive	10			10			
t_h	Hold time, data after CLK↑		0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS74A			SN74ALS74A			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC} − 2			V_{CC} − 2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	CLK or D	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	$\overline{PRE}$ or $\overline{CLR}$					0.2			0.2	
I_{IH}	CLK or D	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	$\overline{PRE}$ or $\overline{CLR}$					40			40	
I_{IL}	CLK or D	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
	$\overline{PRE}$ or $\overline{CLR}$					−0.4			−0.4	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V,	See Note 1		2.4	4		2.4	4	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: I_{CC} is measured with D, CLK, and $\overline{PRE}$ grounded, then with D, CLK, and $\overline{CLR}$ grounded.

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS74A		SN74ALS74A		
			MIN	MAX	MIN	MAX	
f_{max}			30		34		MHz
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	3	15	3	13	ns
t_{PHL}			5	17	5	15	
t_{PLH}	CLK	Q or $\overline{Q}$	5	18	5	16	ns
t_{PHL}			5	20	5	18	

NOTE 2: For load circuit and voltage waveforms, see page 1-12 of the TTL Data Book, Volume 3.

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recommended operating conditions

			SN54AS74			SN74AS74			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−2			−2	mA
I_{OL}	Low-level output current				20			20	mA
f_{clock}	Clock frequency		0		90	0		105	MHz
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	4			4			ns
		CLK high	4			4			
		CLK low	5.5			5.5			
t_{su}	Setup time before CLK↑	Data	4.5			4.5			ns
		$\overline{PRE}$ or $\overline{CLR}$ inactive	2			2			
t_h	Hold time, data after CLK↑		0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS74			SN74AS74			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.25	0.5		0.25	0.5	V
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	CLK or D	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	$\overline{PRE}$ or $\overline{CLR}$					40			40	
I_{IL}	CLK or D	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
	$\overline{PRE}$ or $\overline{CLR}$					−1.8			−1.8	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V	See Note 1		10.5	16		10.5	16	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-current output current, I_{OS}.
NOTE 1: I_{CC} is measured with D, CLK, and $\overline{PRE}$ grounded, then with D, CLK, and $\overline{CLR}$ grounded.

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS74		SN74AS74		
			MIN	MAX	MIN	MAX	
f_{max}			90		105		MHz
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	3	8.5	3	7.5	ns
t_{PHL}			3.5	11.5	3.5	10.5	
t_{PLH}	CLK	Q or $\overline{Q}$	3.5	9	3.5	8	ns
t_{PHL}			4.5	10.5	4.5	9	

NOTE 2: For load circuit and voltage waveforms, see page 1-12 of the TTL Data Book, Volume 3.

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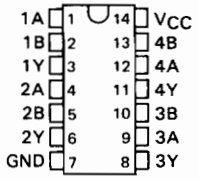
ALS AND AS CIRCUITS

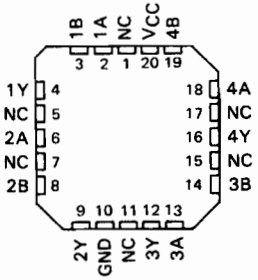
D2661, APRIL 1982—REVISED MARCH 1984

- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS86 . . . J PACKAGE
SN74ALS86 . . . N PACKAGE
(TOP VIEW)



SN54ALS86 . . . FH PACKAGE
SN74ALS86 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

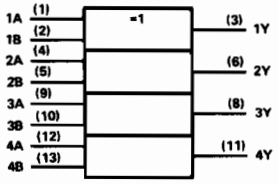
description

These devices contain four independent 2-input Exclusive-OR gates. They perform the Boolean functions $Y = A \oplus B = \overline{A}B + A\overline{B}$ in positive logic.

A common application is as a true/complement element. If one of the inputs is low, the other input will be reproduced in true form at the output. If one of the inputs is high, the signal on the other input will be reproduced inverted at the output.

The SN54ALS86 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS86 is characterized for operation from 0°C to 70°C.

logic symbol



FUNCTION TABLE
(each gate)

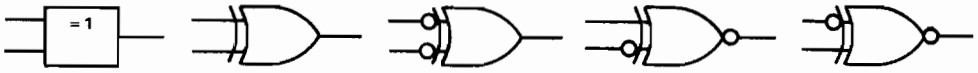
INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

Pin numbers shown are for J and N packages.

exclusive-OR logic

An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.

EXCLUSIVE-OR

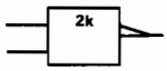


These are five equivalent Exclusive-OR symbols valid for an 'ALS86 gate in positive logic; negation may be shown at any two ports.

LOGIC IDENTITY ELEMENT

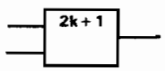
The output is active (low) if all inputs stand at the same logic level (i.e., A = B).

EVEN-PARITY



The output is active (low) if an even number of inputs (i.e., 0 or 2) are active.

ODD-PARITY ELEMENT



The output is active (high) if an odd number of inputs (i.e., only 1 of the 2) are active.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS86 . . . . . −55 °C to 125 °C
SN74ALS86 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS86			SN74ALS86			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS86			SN74ALS86			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V,	All inputs at 4.5 V		3.9	5.9		3.9	5.9	mA

†All typical values are at V_{CC} = 5 V, T_A = 25 °C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS86		SN74ALS86		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B (other input low)	Y	3	22	3	17	ns
t_{PHL}			2	14	2	12	
t_{PLH}	A or B (other input high)	Y	3	22	3	17	ns
t_{PHL}			2	12	2	10	

NOTE 1: For load circuit and voltage waveforms, see page 1-12 of the TTL Data Book, Volume 3.

TEXAS INSTRUMENTS
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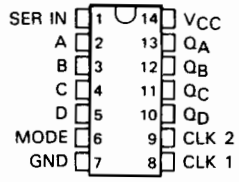
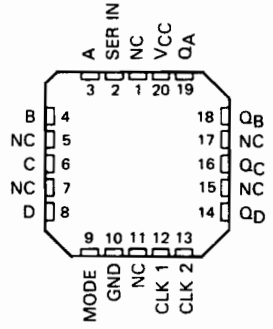
D2661, DECEMBER 1983—REVISED FEBRUARY 1984

- **Serial-to-Parallel Conversions**
- **Parallel Synchronous Loading**
- **Right or Left Shifts**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54AS95 . . . J PACKAGE
SN74AS95 . . . N PACKAGE
(TOP VIEW)



SN54AS95 . . . FH PACKAGE
SN74AS95 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

description

These four-bit registers feature parallel and serial inputs, parallel outputs, mode control, and two clock inputs. The registers have three modes of operation:

Parallel (broadside) load
Shift right (the direction Q_A toward Q_D)
Shift left (the direction Q_D toward Q_A)

Parallel loading is accomplished by applying the four bits and taking the mode control input high. The data is loaded into the associated flip-flops and appears at the outputs after the high-to-low transition of the Clock-2 input. During loading, the entry of serial data is inhibited.

Shift right is accomplished on the high-to-low transition of Clock 1 when the mode control is low; shift left is accomplished on the high-to-low transition of Clock 2 when the mode control is high by connecting the output of each flip-flop to the parallel input of the previous flip-flop (Q_D to input C, etc.); and serial data is entered at input D. The clock input may be applied commonly to Clock 1 and Clock 2 if both modes can be clocked from the same source. Changes at the mode control input should normally be made while both clock inputs are low. However, conditions described in the last three lines of the function table will also ensure that the register contents are protected.

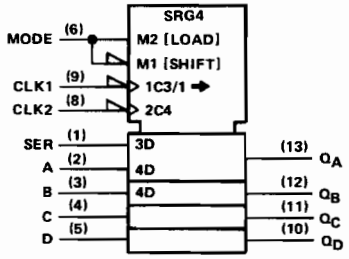
The SN54AS95 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74AS95 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

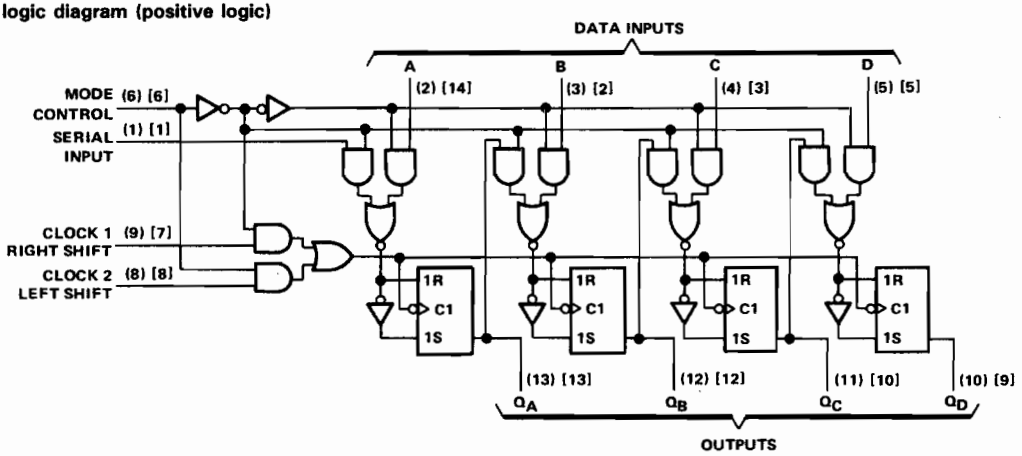
INPUTS								OUTPUTS			
MODE	CLOCKS		SERIAL	PARALLEL							
CONTROL	2 (L)	1 (R)		A	B	C	D	Q_A	Q_B	Q_C	Q_D
H	H	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	↓	X	X	a	b	c	d	a	b	c	d
H	↓	X	X	Q_B†	Q_C†	Q_D†	d	Q_{Bn}	Q_{Cn}	Q_{Dn}	d
L	L	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
L	X	↓	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
L	X	↓	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
↑	L	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↓	L	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↓	L	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↑	H	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↑	H	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

†Shifting left requires external connection of Q_B to A, Q_C to B, and Q_D to C. Serial data is entered at input D.
H = high level (steady state), L = low level (steady state), X = irrelevant (any input, including transitions).
↓ = transition from high to low level, ↑ = transition from low to high level.
a, b, c, d = the level of steady-state input at inputs A, B, C, or D, respectively.
Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the most-recent ↓ transition of the clock.

logic symbol



logic diagram (positive logic)



TEXAS INSTRUMENTS
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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS95 . . . . . −55°C to 125°C
SN74AS95 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54AS95			SN74AS85			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−2			−2	mA
I_{OL}	Low-level output current				20			20	mA
f_{clock}	Clock frequency		0		100	0		100	MHz
t_w	Pulse duration, CLK high or low		5			5			ns
t_{su}	Setup time, data before CLK↓		2.5			2			ns
t_h	Hold time after CLK↓ (see Figure 1)	Data	2.5			2.5			ns
		CLK 1 to Mode	3.5			3			
		CLK 2 to Mode	1			0			
t_{en}	Clock enable time (see Figure 1)	CLK 1	13			12			ns
		CLK 2	13			12			
t_{in}	Clock inhibit time (see Figure 1)	CLK 1	3			2.5			ns
		CLK 2	1			0			
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS95			SN74AS95			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5		0.35	0.5	V
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	Mode	V_{CC} = 5.5 V,	V_{IL} = 0.4 V			−1			−1	mA
	All other					−0.5			−0.5	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.35 V	−30		−112	−30		−112	mA
I_{CCH}		V_{CC} = 5.5 V			21	34		21	34	mA
I_{CCL}		V_{CC} = 5.5 V			26	39		26	39	mA

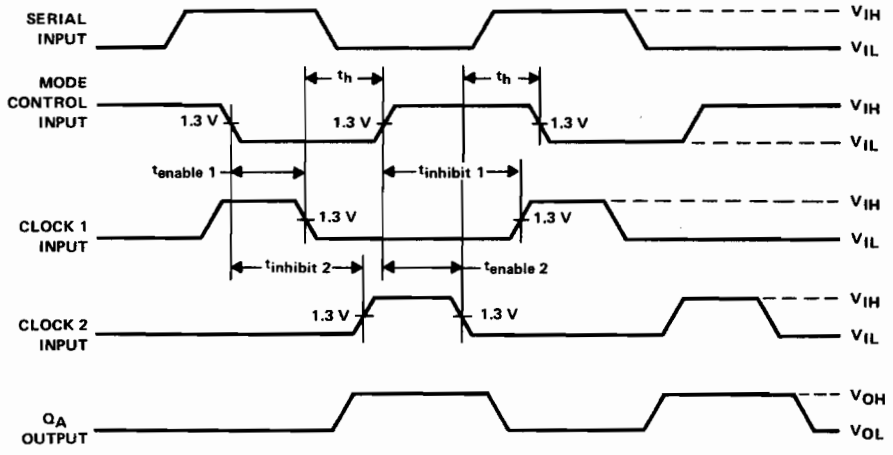
†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristice (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS95		SN74AS95		
			MIN	MAX	MIN	MAX	
f_{max}			100		100		MHz
t_{PLH}	CLK	Q	2	11	2	10	ns
t_{PHL}			2	10.5	2	9.5	

NOTE 1: For load circuit and voltage waveforms, see page 1-12 of the TTL Data Book, Volume 3.

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

NOTES: A. Input A is at a low level.
B. V_{IH} = 3.5 V, V_{IL} = 0.3 V.

FIGURE 1—CLOCK ENABLE, INHIBIT, AND HOLD TIMES

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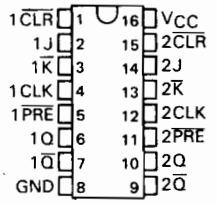
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION PER FLIP-FLOP
'ALS109A	50 MHz	6 mW
'AS109	129 MHz	29 mW

SN54ALS109A, SN54AS109 . . . J PACKAGE
SN74ALS109A, SN74AS109 . . . N PACKAGE
(TOP VIEW)

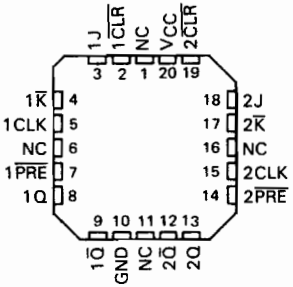


description

These devices contain two independent J-$\overline{K}$ positive-edge-triggered flip-flops. A low level at the Preset or Clear inputs sets or resets the outputs regardless of the levels of the other inputs. When Preset and Clear are inactive (high), data at the J and $\overline{K}$ input meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and $\overline{K}$ inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by grounding $\overline{K}$ and trying J high. They also can perform as D-type flip-flops if J and $\overline{K}$ are tied together.

The SN54ALS109A and SN54AS109 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS109A and SN74AS109 are characterized for operation from 0°C to 70°C.

SN54ALS109A, SN54AS109 . . . FH PACKAGE
SN74ALS109A, SN74AS109 . . . FN PACKAGE
(TOP VIEW)



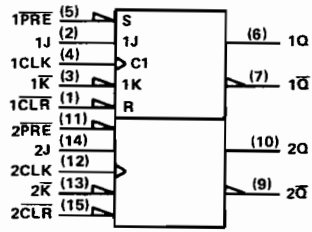
NC—No internal connection

FUNCTION TABLE
(EACH FLIP-FLOP)

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	$\overline{K}$	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↑	L	L	L	H
H	H	↑	H	L	TOGGLE	
H	H	↑	L	H	Q_0	$\overline{Q}_0$
H	H	↑	H	H	H	L
H	H	L	X	X	Q_0	$\overline{Q}_0$

* The output levels in this configuration are not guaranteed to meet the minimum levels for V_{OH} if the lows at Preset and Clear are near V_{IL} maximum. Furthermore, this configuration is nonstable; that is, it will not persist when either Preset or Clear returns to its inactive (high) level.

logic symbol



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS109A, SN54AS109 . . . . . −55°C to 125°C
SN74ALS109A, SN74AS109 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS109A			SN74ALS109A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−0.4			−0.4	mA
I_{OL}	Low-level output current				4			8	mA
f_{clock}	Clock frequency		0		30	0		34	MHz
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	15			15			ns
		CLK high	16.5			14.5			
		CLK low	16.5			14.5			
t_{su}	Setup time before CLK↑	Data	15			15			ns
		$\overline{PRE}$ or $\overline{CLR}$ inactive	10			10			
t_h	Hold time, data after CLK↑		0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS109A			SN74ALS109A			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	CLK, J, or $\overline{K}$	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	$\overline{PRE}$ or $\overline{CLR}$					0.2			0.2	
I_{IH}	CLK, J, or $\overline{K}$	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	$\overline{PRE}$ or $\overline{CLR}$					40			40	
I_{IL}	CLK, J or $\overline{K}$	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
	$\overline{PRE}$ or $\overline{CLR}$					−0.4			−0.4	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V,	See Note 1		2.4	4		2.4	4	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: I_{CC} is measured with J, $\overline{K}$, CLK, and $\overline{PRE}$ grounded, then with J, $\overline{K}$, CLK, and $\overline{CLR}$ grounded.

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS109A		SN74ALS109A		
			MIN	MAX	MIN	MAX	
f_{max}			30		34		MHz
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	3	15	3	13	ns
t_{PHL}			5	17	5	15	
t_{PLH}	CLK	Q or $\overline{Q}$	5	18	5	16	ns
t_{PHL}			5	20	5	18	

NOTE 2: For load circuit and voltage waveforms, see page 1-12 of the TTL Data Book, Volume 3.

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

recommended operating conditions

			SN54AS109			SN74AS109			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−2			−2	mA
I_{OL}	Low-level output current				20			20	mA
f_{clock}	Clock frequency		0		90	0		105	MHz
t_w	Pulse duration	$\overline{PRE}$ or $\overline{CLR}$ low	4			4			ns
		CLK high	4			4			
		CLK low	5.5			5.5			
t_{su}	Setup time before CLK↑	Data	5.5			5.5			ns
		$\overline{PRE}$ or $\overline{CLR}$ inactive	2			2			
t_h	Hold time, data after CLK↑		0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS109			SN74AS109			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.25	0.5		0.25	0.5	V
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	CLK, J or $\overline{K}$	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	$\overline{PRE}$ or $\overline{CLR}$					40			40	
I_{IL}	CLK, J or $\overline{K}$	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			0.5	mA
	$\overline{PRE}$ or $\overline{CLR}$					−1.8			−1.8	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V,	See Note 1		11.5	17		11.5	17	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: I_{CC} is measured with J, $\overline{K}$, CLK, and $\overline{PRE}$ grounded, then with J, $\overline{K}$, CLK, and $\overline{CLR}$ grounded.

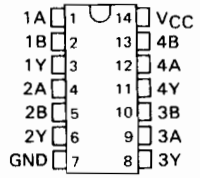
switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS109		SN74AS109		
			MIN	MAX	MIN	MAX	
f_{max}			90		105		MHz
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	3	9	3	8	ns
t_{PHL}			3.5	11.5	3.5	10.5	
t_{PLH}	CLK	Q or $\overline{Q}$	3.5	10	3.5	9	ns
t_{PHL}			4.5	10.5	4.5	9	

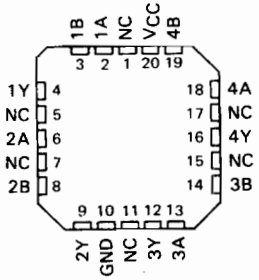
NOTE 2: For load circuit and voltage wavforms, see page 1-12 of the TTL Data Book, Volume 3.

- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS136 . . . J PACKAGE
SN74ALS136 . . . N PACKAGE
(TOP VIEW)



SN54ALS136 . . . FH PACKAGE
SN74ALS136 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

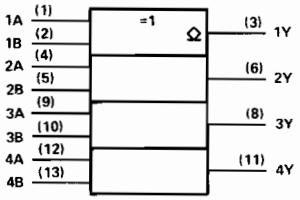
description

These devices contain four independent Exclusive-OR gates with open-collector outputs. They perform the Boolean functions $Y = A \oplus B = \overline{A}B + A\overline{B}$ in positive logic.

A common application is a true/complement element. If one of the inputs is low, the other input will be reproduced in true form at the output. If one of the inputs is high, the signal on the other input will be reproduced inverted at the output.

The SN54ALS136 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS136 is characterized for operation from 0°C to 70°C.

logic symbol



Pin numbers shown are for J and N packages.

FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

exclusive-OR logic

An Exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.

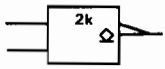
EXCLUSIVE-OR

These are five equivalent Exclusive-OR symbols valid for an 'ALS136 gate in positive logic; negation may be shown at any two ports.

LOGIC IDENTITY ELEMENT

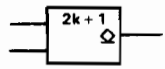
The output is active (low) if all inputs stand at the same logic level (i.e., A = B).

EVEN-PARITY



The output is active (low) if an even number of inputs (i.e., 0 or 2) are active.

ODD-PARITY ELEMENT



The output is active (high) if an odd number of inputs (i.e., only 1 of the 2) are active.

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS136 . . . . . −55°C to 125°C
SN74ALS136 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS136			SN74ALS136			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS136			SN74ALS136			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
I_{OH}	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_{CC}	V_{CC} = 5.5 V,	All inputs at 4.5 V		3.9	5.9		3.9	5.9	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 2 kΩ, T_A = MIN to MAX				UNIT
			SN54ALS136		SN74ALS136		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	20	55	20	50	ns
t_{PHL}	(other input low)		3	18	3	15	
t_{PLH}	A or B	Y	20	55	20	50	ns
t_{PHL}	(other input high)		3	15	3	12	

NOTE 1: For load circuit and voltage waveforms, see page 1-12 of the TTL Data Book, Volume 3.

TEXAS INSTRUMENTS
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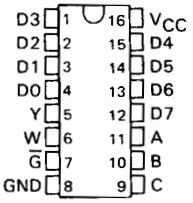
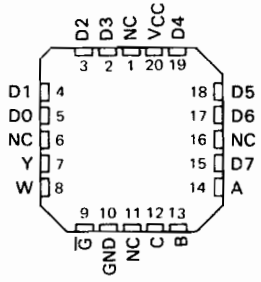
D2661, APRIL 1982—REVISED FEBRUARY 1984

- **8-Line to 1-Line Multiplexers Can Perform As:**
  - **Boolean Function Generators**
  - **Parallel-to-Serial Converters**
  - **Data Source Selectors**
- **Input Clamping Diodes Simplify System Design**
- **Fully Compatible With Most TTL Circuits**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS151, SN54AS151 . . . J PACKAGE
SN74ALS151, SN74AS151 . . . N PACKAGE
(TOP VIEW)



SN54ALS151, SN54AS151 . . . FH PACKAGE
SN74ALS151, SN74AS151 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

description

These monolithic data selectors/multiplexers provide full binary decoding to select one of eight data sources. The strobe input ($\overline{G}$) must be at a low logic level to enable the inputs. A high level at the strobe terminal forces the W output high and the Y output low.

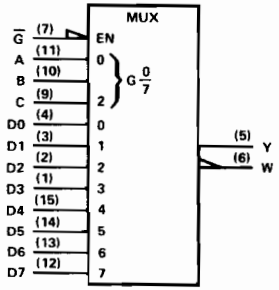
The SN54ALS151 and SN54AS151 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS151 and SN74AS151 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS				OUTPUTS	
SELECT			STROBE		
C	B	A	$\overline{G}$	Y	W
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

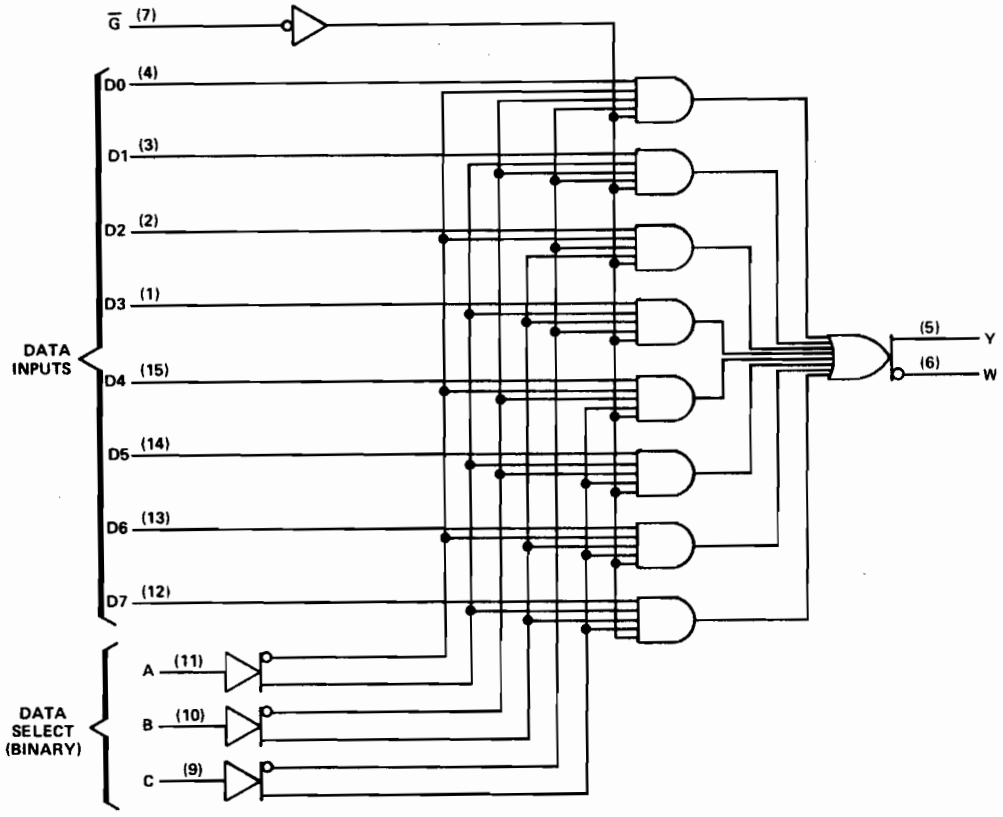
H = high level, L = low level, X = irrelevant
D0, D1 . . . D7 = the level of the D respective input

logic symbol



Pin numbers shown are for J and N packages.

logic diagram (positive logic)



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS151, SN54AS151 . . . . . −55 °C to 125 °C
SN74ALS151, SN74AS151 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150°C

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

recommended operating conditions

		SN54ALS151			SN74ALS151			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−1			−2.6	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS151			SN74ALS151			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
	V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
	V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V,	Inputs at 4.5 V		7.5	12		7.5	12	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS151		SN74ALS151		
			MIN	MAX	MIN	MAX	
t_{PLH}	A, B, or C	Y	4	21	4	18	ns
t_{PHL}			8	28	8	24	
t_{PLH}	A, B, or C	W	7	28	7	24	ns
t_{PHL}			7	26	7	23	
t_{PLH}	Any D	Y	3	12	3	10	ns
t_{PHL}			5	18	5	15	
t_{PLH}	Any D	W	3	18	3	15	ns
t_{PHL}			4	18	4	15	
t_{PLH}	$\overline{G}$	Y	4	21	4	18	ns
t_{PHL}			4	23	4	19	
t_{PLH}	$\overline{G}$	W	5	23	5	19	ns
t_{PHL}			5	26	5	23	

NOTE 1: For load circuit and voltage waveforms, see page 1-12.

recommended operating conditions

		SN54AS151			SN74AS151			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			32			48	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS151			SN74AS151			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4	3.2					
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2.4	3.3		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.25	0.5				V
		V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
I_I	A, B, or C	V_{CC} = 5.5 V,	V_I = 7 V			0.2			0.2	mA
	All others					0.1			0.1	
I_{IH}	A, B, or C	V_{CC} = 5.5 V,	V_I = 2.7 V			40			40	μA
	All others					20			20	
I_{IL}	A, B, or C	V_{CC} = 5.5 V,	V_I = 0.4 V			−1			−1	mA
	All others					−0.5			−0.5	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V,			18.6	30		18.6	30	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS151		SN74AS151		
			MIN	MAX	MIN	MAX	
t_{PLH}	A, B, or C	Y	4.5	16	4.5	14.5	ns
t_{PHL}			4.5	16	4.5	15	
t_{PLH}	A, B, or C	W	4	14.5	4	12	ns
t_{PHL}			4	14.5	4	12	
t_{PLH}	Any D	Y	3	11.5	3	10.5	ns
t_{PHL}			3	12	3	11	
t_{PLH}	Any D	W	2	8	2	6.5	ns
t_{PHL}			1	5.5	1	4.5	
t_{PLH}	$\overline{G}$	Y	4.5	16	4.5	14	ns
t_{PHL}			3	12.5	3	11	
t_{PLH}	$\overline{G}$	W	1.5	7	1.5	6	ns
t_{PHL}			3	11	3	10	

NOTE 1: For load circuit and voltage waveforms, see page 1-12 of The TTL Data Book, Volume 3.

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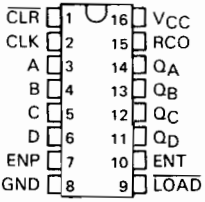
TYPES SN54ALS160A THRU SN54ALS163A, SN54AS160 THRU SN54AS163
SN74ALS160A THRU SN74ALS163A, SN74AS160 THRU SN74AS163
SYNCHRONOUS 4-BIT DECADE AND BINARY COUNTERS

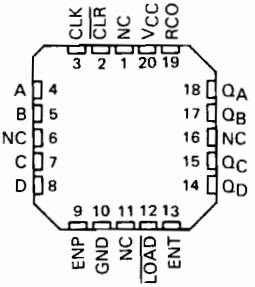
D2661, APRIL 1982–REVISED FEBRUARY 1984

- **Internal Look-Ahead for Fast Counting**
- **Carry Output for n-Bit Cascading**
- **Synchronous Counting**
- **Synchronously Programmable**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS', SN54AS' . . . J PACKAGE
SN74ALS', SN74AS' . . . N PACKAGE
(TOP VIEW)



SN54ALS', SN54AS . . . FH PACKAGE
SN74ALS', SN74AS' . . . FN PACKAGE
(TOP VIEW)



NC – No internal connection

description

These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting designs. The 'ALS160A, 'ALS162A, 'AS160, and 'AS162 are decade counters, and the 'ALS161A, 'ALS163A, 'AS161, and 'AS163 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes that are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform.

These counters are fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs.

The clear function for the 'ALS160A, 'ALS161A, 'AS160, and 'AS161 is asynchronous and a low level at the clear input sets all four of the flip-flop outputs low regardless of the levels of the clock, load, or enable inputs.

The clear function for the 'ALS162A, 'ALS163A, 'AS162, and 'AS163 is synchronous and a low level at the clear input sets all four of the flip-flop outputs low after the next clock pulse, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily as decoding the maximum count desired can be accomplished with one external NAND gate. The gate output is connected to the clear input to synchronously clear the counter to 0000 (LLLL).

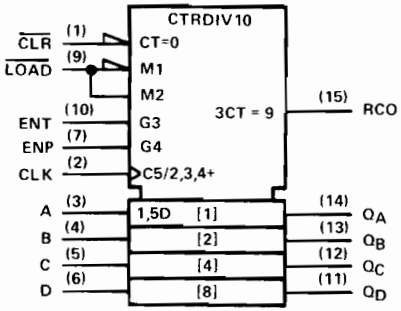
The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output. Both count-enable inputs (ENP and ENT) must be high to count, and ENT is fed forward to enable the ripple carry output. The ripple carry output (RCO) thus enabled will produce a high-level pulse while the count is maximum (9 or 15 with Q_A high). This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. Transitions at the ENP or ENT are allowed regardless of the level of the clock input.

These counters feature a fully independent clock circuit. Changes at control inputs (ENP, ENT, or $\overline{\text{LOAD}}$) that will modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

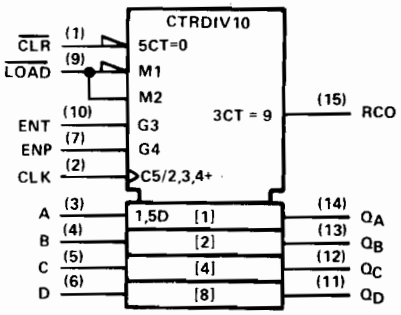
The SN54ALS160A through SN54ALS163A and SN54AS160 through SN54AS163 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS160A through SN74ALS163A and SN74AS160 through SN74AS163 are characterized for operation from 0°C to 70°C.

logic symbols

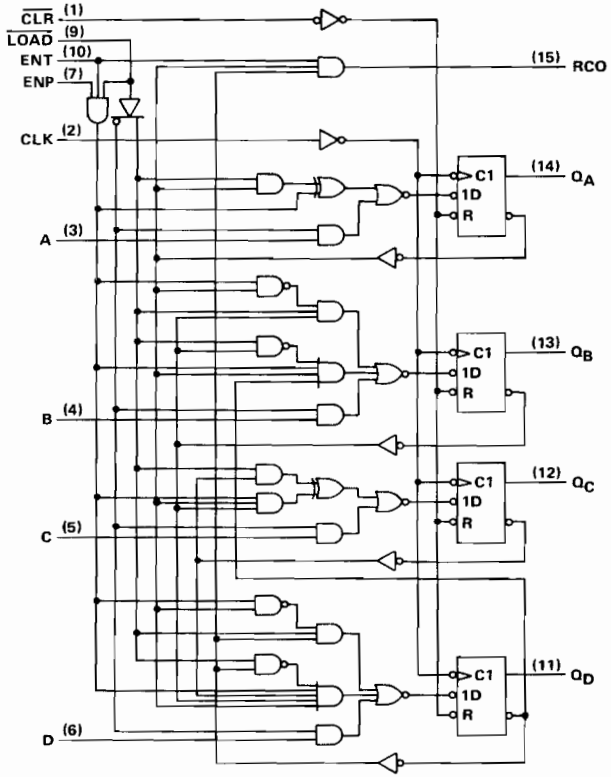
'ALS160A AND 'AS160 DECADE COUNTERS WITH DIRECT CLEAR



'ALS162A AND 'AS162 DECADE COUNTERS WITH SYNCHRONOUS CLEAR



'ALS160A and 'AS160 logic diagram (positive logic)



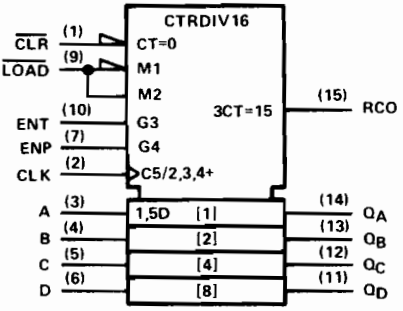
'ALS162A and 'AS162 decade counters are similar; however the clear is synchronous as shown for the 'ALS163A and 'AS163 binary counters.

Pin numbers shown are for J and N packages.

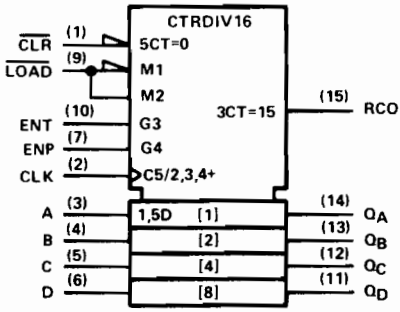
TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

logic symbols

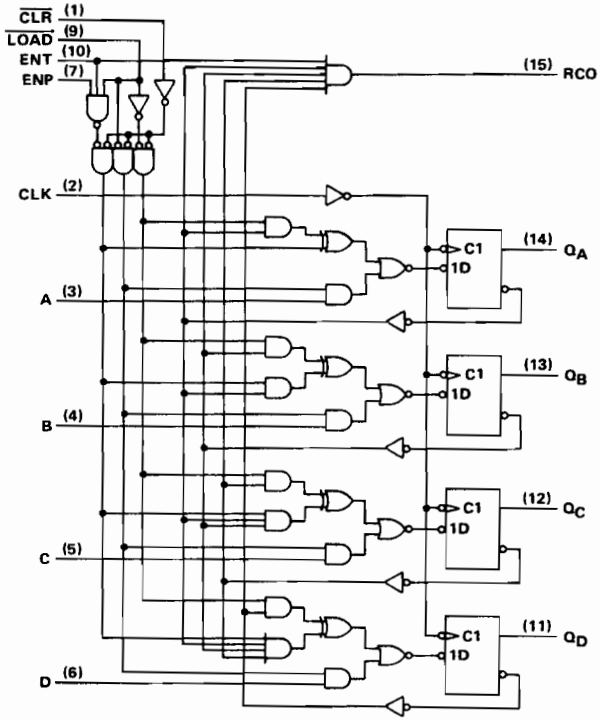
'ALS161A AND 'AS161 BINARY COUNTERS WITH DIRECT CLEAR



'ALS163A AND 'AS163 BINARY COUNTERS WITH SYNCHRONOUS CLEAR



'ALS163A and 'AS163 logic diagram (positive logic)



'ALS161A and 'AS161 synchronous binary counters are similar; however the clear is asynchronous as shown for the 'ALS160A and 'AS160 decade counters.

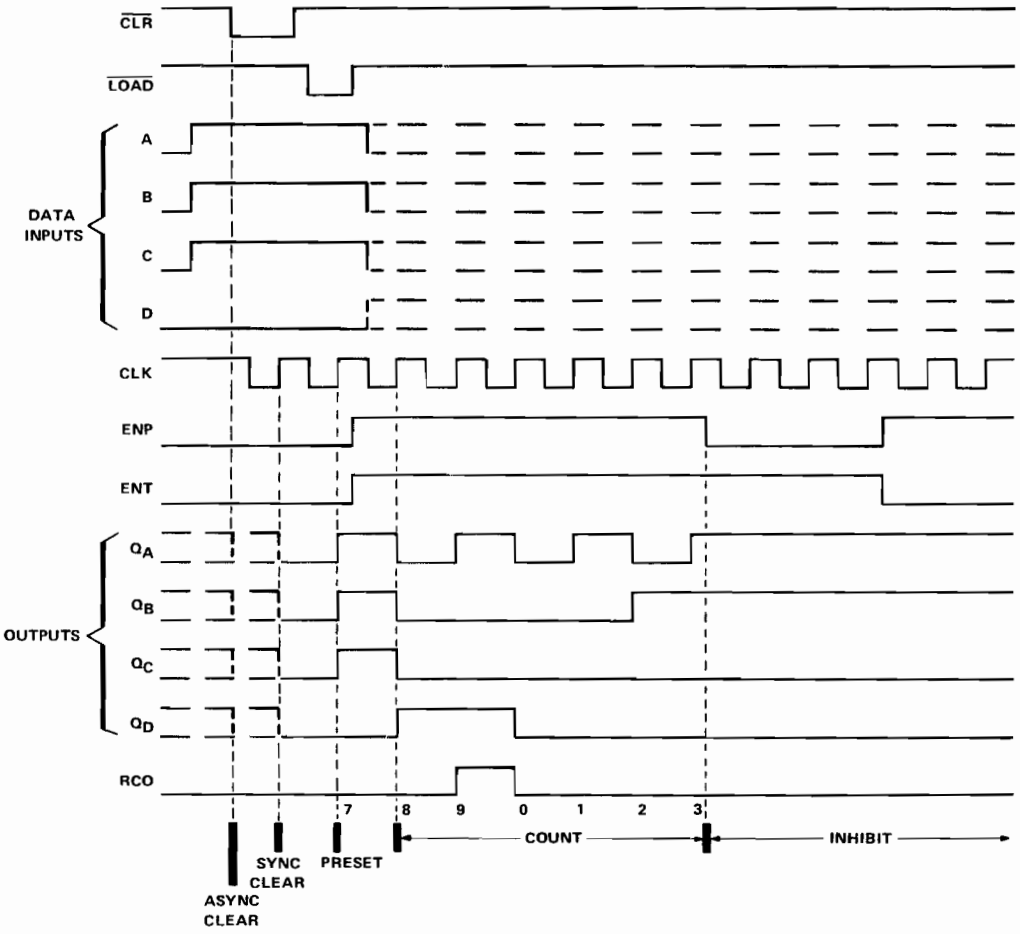
Pin numbers shown are for J and N packages.

typical clear, preset, count, and inhibit sequences

'ALS160A, 'AS160, 'ALS162A, 'AS162

Illustrated below is the following sequence:

1. Clear outputs to zero ('ALS160A and 'AS160 are asynchronous; 'ALS162A and 'AS162 are synchronous)
2. Preset to BCD seven
3. Count to eight, nine, zero, one, two, and three
4. Inhibit

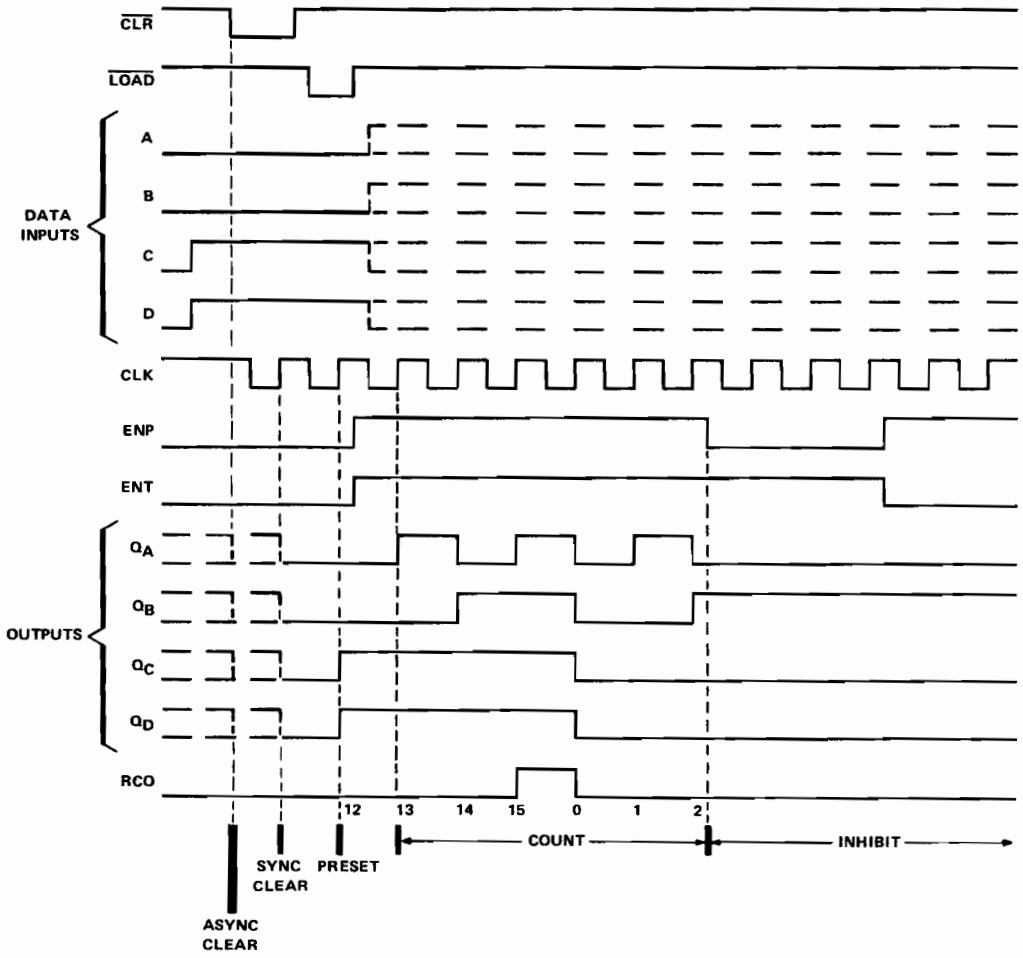


typical clear, preset, count, and inhibit sequences

'ALS161A, 'AS161, 'ALS163A, 'AS163

Illustrated below is the following sequence:

1. Clear outputs to zero ('ALS161A and 'AS161 are asynchronous; 'ALS163A and 'AS163 are synchronous)
2. Preset to binary twelve
3. Count to thirteen, fourteen, fifteen, zero, one, and two
4. Inhibit



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS160A thru SN54ALS163A . . . . . −55°C to 125°C
SN74ALS160A thru SN74ALS163A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

				SN54ALS160A THRU SN54ALS163A			SN74ALS160A THRU SN74ALS163A			UNIT
				MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage			4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
I_{OH}	High-level output current					−0.4			−0.4	mA
I_{OL}	Low-level output current					4			8	mA
f_{clock}	Clock frequency			0		25	0		30	MHz
t_w	Pulse duration	CLK high or low		20			16.5			ns
		'ALS160A, 'ALS161A, $\overline{CLR}$ low		20			15			
t_{su}	Setup time before CLK↑	A, B, C, D		20			15			ns
		$\overline{LOAD}$		20			15			
		ENP, ENT	'ALS160A, 'ALS161A	25			20			
			'ALS162A, 'ALS163A	30			25			
		'ALS160A, 'ALS161A	$\overline{CLR}$ inactive	10			10			
		'ALS162A, 'ALS163A	$\overline{CLR}$ low	20			15			
			$\overline{CLR}$ high (inactive)	10			10			
t_h	Hold time, all synchronous inputs after CLK↑			0			0			ns
T_A	Operating free-air temperature			−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS160A THRU SN54ALS163A			SN74ALS160A THRU SN74ALS163A			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	$\overline{LOAD}$, CLK or ENT	V_{CC} = 5.5 V,	V_I = 7 V			0.2			0.2	mA
	All other					0.1			0.1	
I_{IH}	$\overline{LOAD}$, CLK or ENT	V_{CC} = 5.5 V,	V_I = 2.7 V			40			40	μA
	All other					20			20	
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
I_O‡	$\overline{RCO}$	V_{CC} = 5.5 V,	V_O = 2.25 V	−15		−70	−15		−70	mA
	Q			−30		−112	−30		−112	
I_{CC}		V_{CC} = 5.5 V			12	21		12	21	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

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'ALS160A, 'ALS161A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS160A SN54ALS161A		SN74ALS160A SN74ALS161A		
			MIN	MAX	MIN	MAX	
f_{max}			25		30		MHz
t_{PLH}	CLK	RCO	8	30	8	26	ns
t_{PHL}			7	25	7	23	
t_{PLH}	CLK	Any Q	4	18	4	15	ns
t_{PHL}			6	20	6	17	
t_{PLH}	ENT	RCO	3	16	3	13	ns
t_{PHL}			3	16	3	13	
t_{PHL}	$\overline{CLR}$	Any Q	8	27	8	24	ns
t_{PHL}	$\overline{CLR}$	RCO	11	31	11	28	ns

'ALS162A, 'ALS163A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS162A SN54ALS163A		SN74ALS162A SN74ALS163A		
			MIN	MAX	MIN	MAX	
f_{max}			25		30		MHz
t_{PLH}	CLK	RCO	8	30	8	26	ns
t_{PHL}			7	25	7	23	
t_{PLH}	CLK	Any Q	4	18	4	15	ns
t_{PHL}			6	20	6	17	
t_{PLH}	ENT	RCO	3	20	3	17	ns
t_{PHL}			3	16	3	13	

NOTE 1: For load circuit and voltage waveforms, see page 1-12 of The TTL Data Book, Volume 3.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS160 thru SN54AS163 . . . . . −55°C to 125°C
SN74AS160 thru SN74AS163 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

				SN54AS160 THRU SN54AS163			SN74AS160 THRU SN74AS163			UNIT
				MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage			4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
I_{OH}	High-level output current					−2			−2	mA
I_{OL}	Low-level output current					20			20	mA
f_{clock}	Clock frequency			0		65	0		75	MHz
t_w	Pulse duration	CLK high or low		7.7			6.7			ns
		'AS160, 'AS161 $\overline{CLR}$ low		10			8			
t_{su}	Setup time before CLK↑	A, B, C, D		10			8			ns
		$\overline{LOAD}$		10			8			
		ENP, ENT		10			8			
		'AS160, 'AS161 $\overline{CLR}$ inactive		10			8			
		'AS162, 'AS163	$\overline{CLR}$ low	14			12			
			$\overline{CLR}$ high (inactive)	10			9			
t_h	Hold time, all synchronous inputs after CLK↑			2			0			ns
T_A	Operating free-air temperature			−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS160 THRU SN54AS163			SN74AS160 THRU SN74AS163			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.25	0.5		0.25	0.5	V
I_I	$\overline{LOAD}$	V_{CC} = 5.5 V,	V_I = 7 V			0.3			0.3	mA
	ENT					0.2			0.2	
	All other					0.1			0.1	
I_{IH}	$\overline{LOAD}$	V_{CC} = 5.5 V,	V_I = 2.7 V			60			60	μA
	ENT					40			40	
	All other					20			20	
I_{IL}	$\overline{LOAD}$	V_{CC} = 5.5 V,	V_I = 0.4 V			−1.5			−1.5	mA
	ENT					−1			−1	
	All other					−0.5			−0.5	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V			35	53		35	53	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

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'AS160, 'AS161 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS160 SN54AS161		SN74AS160 SN74AS161		
			MIN	MAX	MIN	MAX	
f_{max}			65		75		MHz
t_{PHL}	CLK	RCO	2	14	2	12.5	ns
t_{PLH}		RCO (with $\overline{LOAD}$ high)	1	8.5	1	8	
t_{PLH}		RCO (with $\overline{LOAD}$ low)	3	17.5	3	16.5	
t_{PLH}	CLK	Any Q	1	7.5	1	7	ns
t_{PHL}			2	14	2	13	
t_{PLH}	ENT	RCO	1.5	10	1.5	9	ns
t_{PHL}			1	9.5	1	8.5	
t_{PHL}	$\overline{CLR}$	Any Q	2	14	2	13	ns
t_{PHL}	$\overline{CLR}$	RCO	2	14	2	12.5	ns

'AS162, 'AS163 switching characteristics (see Note 1)

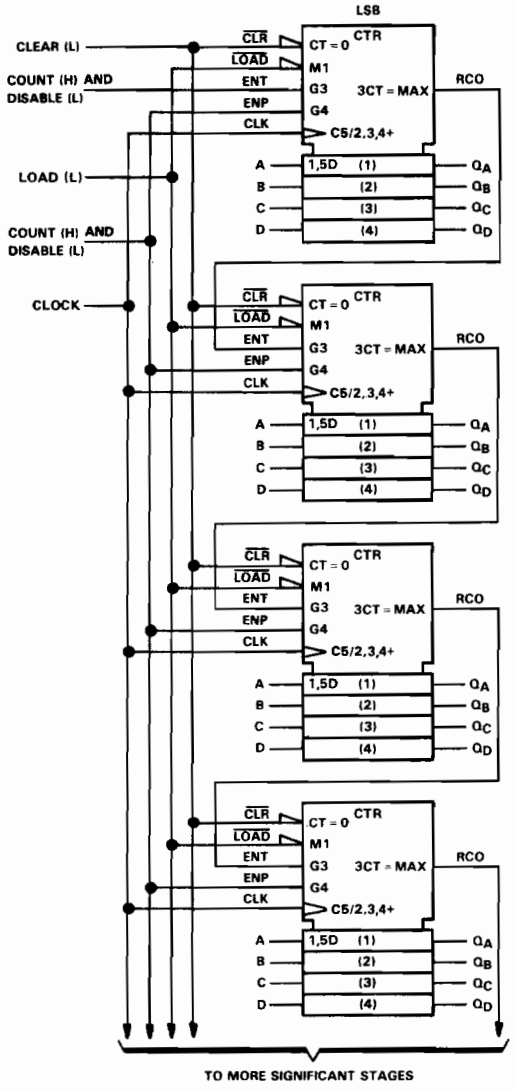
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS162 SN54AS163		SN74AS162 SN74AS163		
			MIN	MAX	MIN	MAX	
f_{max}			65		75		MHz
t_{PHL}	CLK	RCO	2	14	2	12.5	ns
t_{PLH}		RCO (with $\overline{LOAD}$ high)	1	8.5	1	8	
t_{PLH}		RCO (with $\overline{LOAD}$ low)	3	17.5	3	16.5	
t_{PLH}	CLK	Any Q	1	7.5	1	7	ns
t_{PHL}			2	14	2	13	
t_{PLH}	ENT	RCO	1.5	10	1.5	9	ns
t_{PHL}			1	9.5	1	8.5	

NOTE 1: For load circuit and voltage waveforms, see page 1-12 of The TTL Data Book, Volume 3.

TYPICAL APPLICATION DATA

N-BIT SYNCHRONOUS COUNTERS

This application demonstrates how the look-ahead carry circuit can be used to implement a high-speed n-bit counter. The 'ALS160A, 'AS160, 'ALS162A, and 'AS162 will count in BCD and the 'ALS161A, 'AS161, 'ALS163A and 'AS163 will count in binary. Virtually any count mode (modulo-N, N_1-to-N_2, N_1-to-maximum) can be used with this fast look-ahead circuit.



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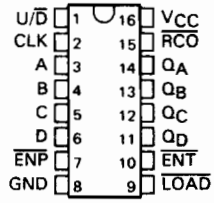
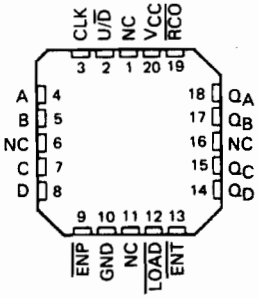
- **Fully Synchronous Operation for Counting and Programming**
- **Internal Look-Ahead for Fast Counting**
- **Carry Output for n-Bit Cascading**
- **Fully Independent Clock Circuit**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS', SN54AS' . . . J PACKAGE
SN74ALS', SN74AS' . . . N PACKAGE
(TOP VIEW)



SN54ALS', SN54AS' . . . FH PACKAGE
SN74ALS', SN74AS' . . . FN PACKAGE
(TOP VIEW)



NC – No internal connection

description

These synchronous presettable counters feature an internal carry look-ahead for cascading in high-speed counting applications. The 'ALS168B and 'AS168 are decade counters and the 'ALS169B and 'AS169 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation helps eliminate the output counting spikes that are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock waveform.

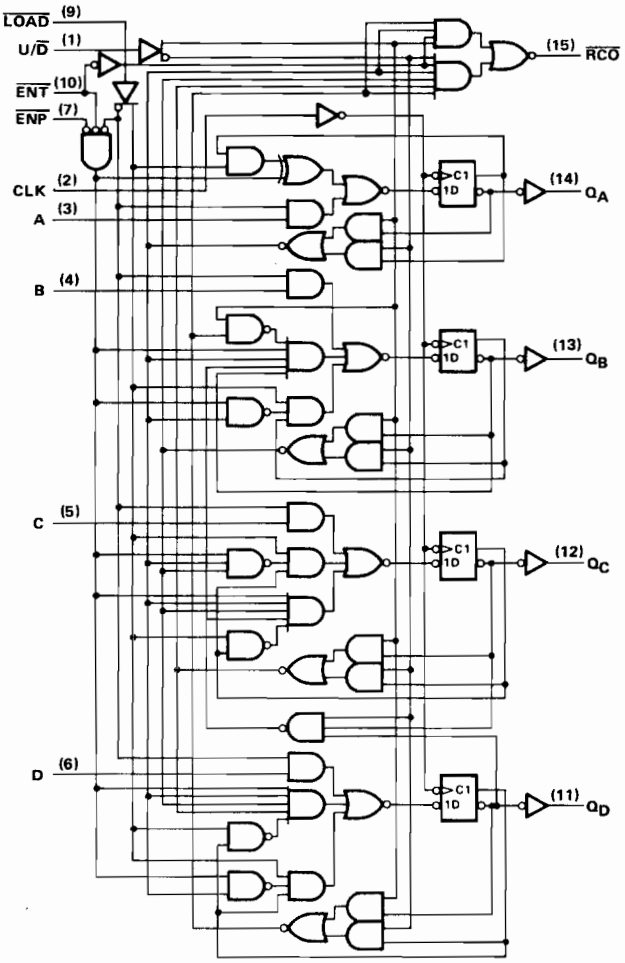
These counters are fully programmable; that is, the outputs may each be preset to either level. The load input circuitry allows loading with the carry-enable output of cascaded counters. As loading is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the data inputs after the next clock pulse.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous application without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a carry output. Both count enable inputs ($\overline{ENP}$ and $\overline{ENT}$) must be low to count. The direction of the count is determined by the level of the U/$\overline{D}$ input. When U/$\overline{D}$ is high, the counter counts up; when low, it counts down. Input $\overline{ENT}$ is fed forward to enable the carry output. The riple carry output ($\overline{RCO}$) thus enabled will produce a low-level pulse while the count is zero (all inputs low) counting down or maximum (9 or 15) counting up. This low-level overflow carry pulse can be used to enable successive cascaded stages. Transistions at $\overline{ENP}$ or $\overline{ENT}$ are allowed regardless of the level of the clock input. All inputs are diode-clamped to minimize transmission-line effects, thereby simplifying system design.

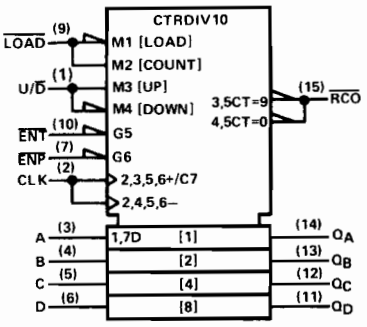
These counters feature a fully independent clock circuit. Changes at control inputs ($\overline{ENP}$, $\overline{ENT}$, $\overline{LOAD}$, U/$\overline{D}$) that will modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

The SN54ALS168B, SN54AS168, SN54ALS169B, and SN54AS169 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS168B, SN74AS168, SN74ALS169B, and SN74AS169 are characterized for operation from 0°C to 70°C.

'ALS168B, 'AS168 logic diagram (positive logic)



'ALS168B, 'AS168 logic symbol



Pin numbers shown are for J and N packages.

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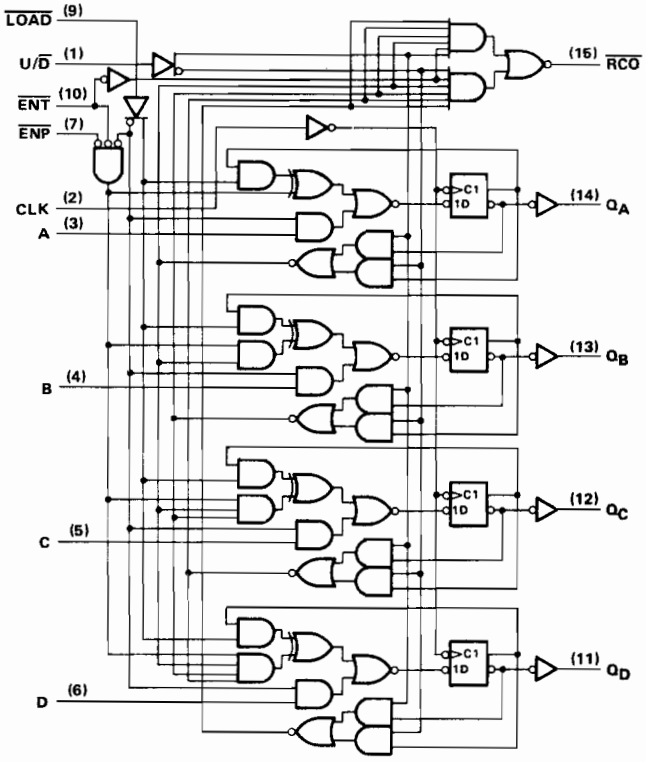
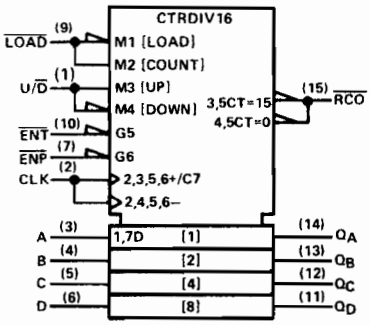
'ALS169B, 'AS169 logic diagram (positive logic)



'ALS169B, 'AS169 logic symbol

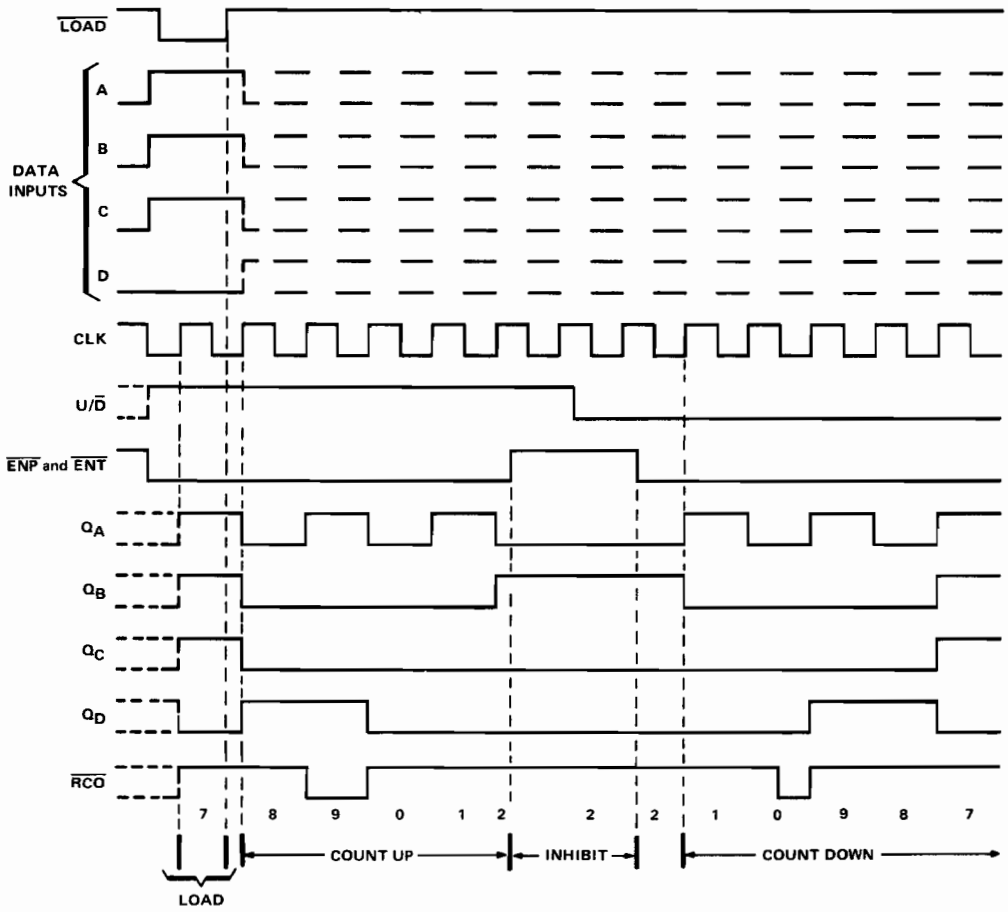


Pin numbers shown are for J and N packages.

'ALS168B, 'AS168 typical load, count, and inhibit sequences

Illustrated below is the following sequence:

1. Load (preset) to BCD seven
2. Count up to eight, nine (maximum), zero, one, and two
3. Inhibit
4. Count down to one, zero (minimum), nine, eight, and seven



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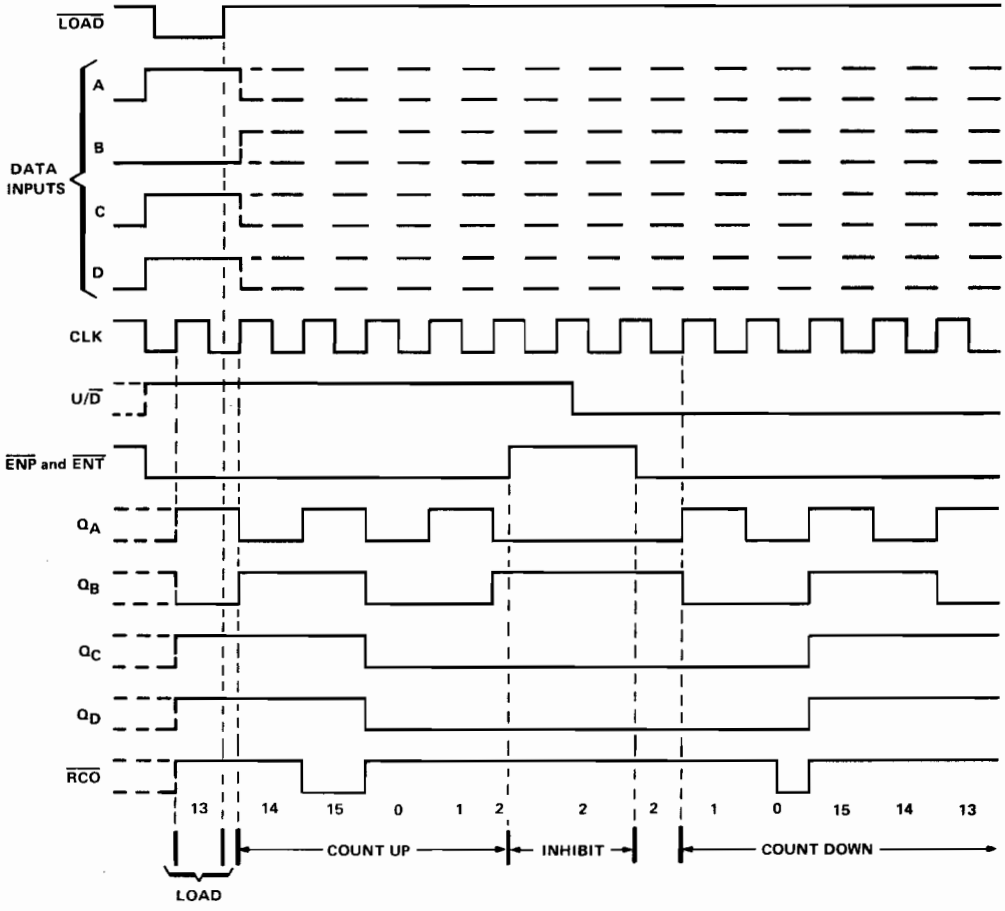
'ALS169B, 'AS169 typical load, count, and inhibit sequences

Illustrated below is the following sequence:

1. Load (preset) to binary thirteen
2. Count up to fourteen, fifteen (maximum), zero, one, and two
3. Inhibit
4. Count down to one, zero (minimum), fifteen, fourteen, and thirteen



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS168B, SN54ALS169B . . . . . −55°C to 125°C
SN74ALS168B, SN74ALS169B . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS168B SN54ALS169B			SN74ALS168B SN74ALS169B			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−0.4			−0.4	mA
I_{OL}	Low-level output current				4			8	mA
f_{clock}	Clock frequency		0		25	0		30	MHz
t_w	Pulse duration	CLK high or low	20			16.5			ns
t_{su}	Setup time before CLK↑	A, B, C, or D	20			15			ns
		$\overline{ENP}$ or $\overline{ENT}$	25			20			
		$\overline{LOAD}$	20			15			
		U/$\overline{D}$	20			15			
t_h	Hold time, data after CLK↑		0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS168B SN54ALS169B			SN74ALS168B SN74ALS169B			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.2			−0.2	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V			15	25		15	25	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'ALS168B, 'ALS169B switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, RL = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS168B SN54ALS169B		SN74ALS168B SN74ALS169B		
			MIN	MAX	MIN	MAX	
f_{max}			25		30		MHz
t_{PLH}	CLK	$\overline{RCO}$	3	15	3	13	ns
t_{PHL}			6	22	6	18	
t_{PLH}	CLK	Any Q	2	15	2	13	ns
t_{PHL}			5	20	5	16	
t_{PLH}	$\overline{ENT}$	$\overline{RCO}$	2	15	2	12	ns
t_{PHL}			3	16	3	13	
t_{PLH}	U/$\overline{D}$	$\overline{RCO}$	5	21	5	18	ns
t_{PHL}			5	21	5	18	

NOTE 1: For load circuit and voltage waveforms, see page 1-12 of the TTL Data Book, Volume 3.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS168, SN54AS169 . . . . . −55°C to 125°C
SN74AS168, SN74AS169 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54AS168 SN54AS169			SN74AS168 SN74AS169			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−2			−2	mA
I_{OL}	Low-level output current				20			20	mA
f_{clock}	Clock frequency		0		65	0		75	MHz
t_w	Pulse duration	CLK high or low	7.7			6.7			ns
t_{su}	Setup time before CLK↑	A, B, C, or D	10			8			ns
		$\overline{ENP}$ or $\overline{ENT}$	10			8			
		$\overline{LOAD}$	10			8			
		U/$\overline{D}$	10			8			
t_h	Hold time, data after CLK↑		2			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS168 SN54AS169			SN74AS168 SN74AS169			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.25	0.5		0.25	0.5	V
I_I	$\overline{LOAD}$, $\overline{ENT}$, U/$\overline{D}$	V_{CC} = 5.5 V,	V_I = 7 V			0.2			0.2	mA
	All others					0.1			0.1	
I_{IH}	$\overline{LOAD}$, $\overline{ENT}$, U/$\overline{D}$	V_{CC} = 5.5 V,	V_I = 2.7 V			40			40	μA
	All others					20			20	
I_{IL}	$\overline{LOAD}$, $\overline{ENT}$, U/$\overline{D}$	V_{CC} = 5.5 V,	V_I = 0.4 V			−1			−1	mA
	All others,					−0.5			−0.5	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V			41	63		41	63	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

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'AS168, 'AS169 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, RL = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS168 SN54AS169		SN74AS168 SN74AS169		
			MIN	MAX	MIN	MAX	
f_{max}			65		75		MHz
t_{PLH}	CLK	$\overline{RCO}$	3	17.5	3	16.5	ns
t_{PHL}		($\overline{LOAD}$ high or low)	2	14	2	13	
t_{PLH}	CLK	Any Q	1	7.5	1	7	ns
t_{PHL}			2	14	2	13	
t_{PLH}	$\overline{ENT}$	$\overline{RCO}$	1.5	10	1.5	9	ns
t_{PHL}			1.5	10	1.5	9	
t_{PLH}	U/$\overline{D}$	$\overline{RCO}$	2	14	2	12	ns
t_{PHL}			2	14.5	2	13	

NOTE 1: For load circuit and voltage waveforms, see page 1-12 of the TTL Data Book, Volume 3.

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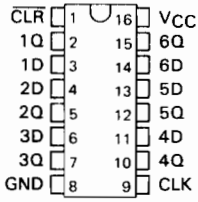
ALS AND AS CIRCUITS

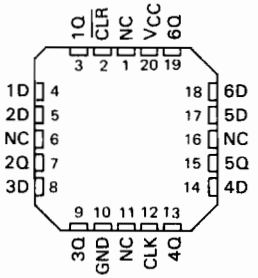
D2661, APRIL 1982 – REVISED FEBRUARY 1984

- **'ALS174 and 'AS174 Contain Six Flip-Flops with Single-Rail Outputs**
- **'ALS175 and 'AS175 Contain Four Flip-Flops with Double-Rail Outputs**
- **Buffered Clock and Direct Clear Inputs**
- **Applications Include:**
  Buffer/Storage Registers
  Shift Registers
  Pattern Generators
- **Fully Buffered Outputs for Maximum Isolation from External Disturbance ('AS only)**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

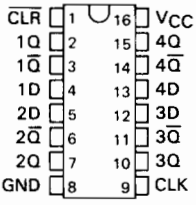
SN54ALS174, SN54AS174 . . . J PACKAGE
SN74ALS174, SN74AS174 . . . N PACKAGE
(TOP VIEW)



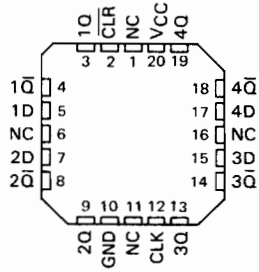
SN54ALS174, SN54AS174 . . . FH PACKAGE
SN74ALS174, SN74AS174 . . . FN PACKAGE
(TOP VIEW)



SN54ALS175, SN54AS175 . . . J PACKAGE
SN74ALS175, SN74AS175 . . . N PACKAGE
(TOP VIEW)



SN54ALS175, SN54AS175 . . . FH PACKAGE
SN74ALS175, SN74AS175 . . . FN PACKAGE
(TOP VIEW)



NC – No internal connection.

description

These monolithic, positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic. All have a direct clear input and the 'ALS175 and 'AS175 feature complementary outputs from each flip-flop.

Information at the D inputs meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

These circuits are fully compatible for use with most TTL circuits.

The SN54ALS174, SN54ALS175, SN54AS174, and SN54AS175 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS174, SN74ALS175, SN74AS174, and SN74AS175 are characterized for operation from 0°C to 70°C.

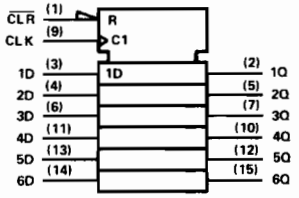
FUNCTION TABLE
(EACH FLIP-FLOP)

INPUTS			OUTPUTS	
$\overline{CLR}$	CLK	D	Q	$\overline{Q}$†
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q}_0$

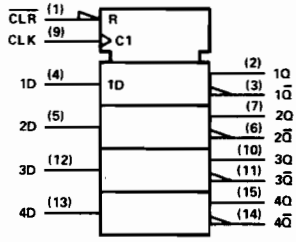
† 'ALS175 and 'AS175 only

logic symbols

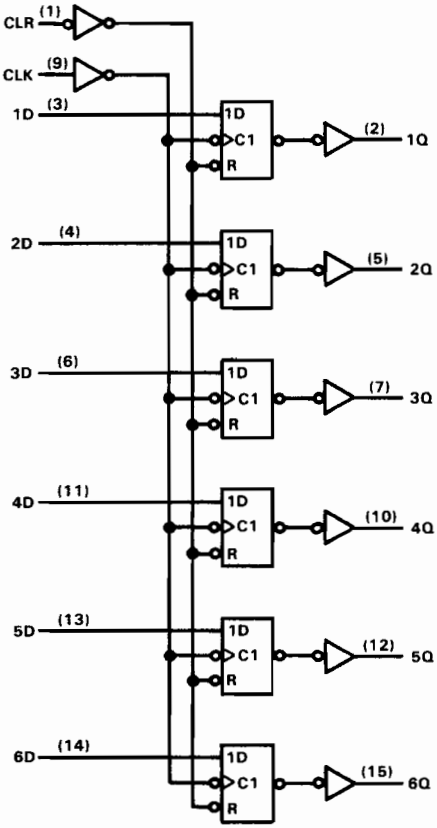
'ALS174, 'AS174

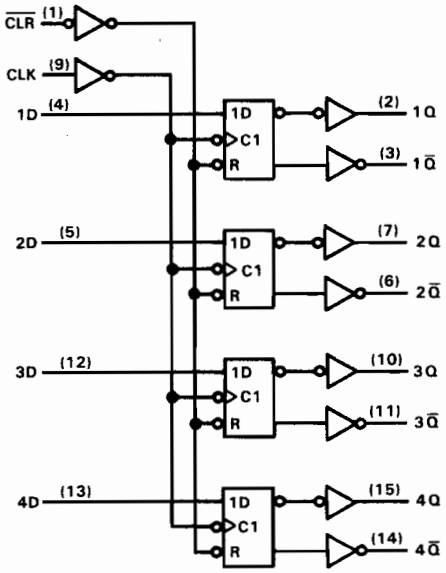


'ALS175, 'AS175



logic diagrams (positive logic)





Pin numbers shown are for J and N packages.

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS174, SN54ALS175 . . . . . −55°C to 125°C
SN74ALS174, SN74ALS175 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS174 SN54ALS175			SN74ALS174 SN74ALS175			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−0.4			−0.4	mA
I_{OL}	Low-level output current				4			8	mA
f_{clock}	Clock frequency		0		40	0		50	MHz
t_w	Pulse duration	$\overline{CLR}$ low	15			10			ns
		CLK high	12.5			10			
		CLK low	12.5			10			
t_{su}	Setup time before CLK↑	Data	15			10			ns
		$\overline{CLR}$ inactive	8			6			
t_h	Hold time, data after CLK↑		0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS174 SN54ALS175			SN74ALS174 SN74ALS175			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V	I_{OL} = 8 mA					0.35	0.5	
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'ALS174	V_{CC} = 5.5 V,	See Note 1		11	19		11	19	mA
	'ALS175				8	14		9	14	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: I_{CC} is measured with D inputs and $\overline{CLR}$ grounded, and CLK at 4.5 V.

switching characteristics (see Note 2)

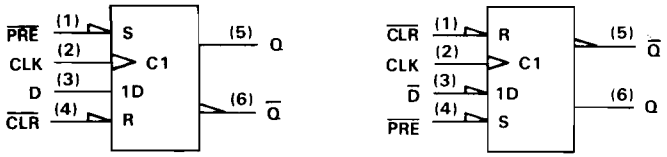
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS174 SN54ALS175		SN74ALS174 SN74ALS175		
			MIN	MAX	MIN	MAX	
f_{max}			40		50		MHz
t_{PLH}	$\overline{CLR}$	Any $\overline{Q}$ ('ALS175)	5	20	5	18	ns
t_{PHL}		Any Q	8	26	8	23	
t_{PLH}	CLK	Any Q	3	17	3	15	ns
t_{PHL}		(or $\overline{Q}$, 'ALS175)	5	20	5	17	

NOTE 2: For load circuit and voltage waveforms, see page 1-12.

D flip-flop signal conventions

It is TI practice to name the outputs and other inputs of a D-type flip-flop and to draw its logic symbol based on the assumption of true data (D) inputs. Then outputs that produce data in phase with the data inputs are called Q and those producing complementary data are called $\overline{Q}$. An input that causes a Q output to go high or a $\overline{Q}$ output to go low is called Preset; an input that causes a $\overline{Q}$ output to go high or a Q output to go low is called Clear. Bars are used over these pin names ($\overline{PRE}$ and $\overline{CLR}$) if they are active low.

In some applications it may be advantageous to redesignate the data input $\overline{D}$. In that case all the other inputs and outputs should be renamed as shown below. Also shown are corresponding changes in the graphical symbol. Arbitrary pin numbers are shown in parentheses.



Notice that Q and $\overline{Q}$ exchange names, which causes Preset and Clear to do likewise. Also notice that the polarity indicators (▷) on $\overline{PRE}$ and $\overline{CLR}$ remain since these inputs are still active-low, but that the presence or absence of the polarity indicator changes at $\overline{D}$, Q, and $\overline{Q}$. Of course pin 5 ($\overline{Q}$) is still in phase with the data input $\overline{D}$, but now both are considered active-low.

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS174, SN54AS175 . . . . . −55°C to 125°C
SN74AS174, SN74AS175 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

				SN54AS174 SN54AS175			SN74AS174 SN74AS175			UNIT
				MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage			4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
I_{OH}	High-level output current					−2			−2	mA
I_{OL}	Low-level output current					20			20	mA
f_{clock}	Clock frequency			0		100	0		100	MHz
t_w	Pulse duration	$\overline{CLR}$ low		5.5			5			ns
		CLK high		4			4			
		CLK low	'AS174	6			6			
			'AS175	5			3			
t_{su}	Setup time before CLK↑	Data	'AS174	4			4			ns
			'AS175	3			3			
		$\overline{CLR}$ inactive		6			6			
t_h	Hold time, data after CLK↑			1			1			ns
T_A	Operating free-air temperature			−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS174 SN54AS175			SN74AS174 SN74AS175			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5		0.35	0.5	V
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'AS174	V_{CC} = 5.5 V,	See Note 1		30	45		30	45	mA
	'AS175				22.5	34		22.5	34	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 1: I_{CC} is measured with D, CLK, and PRE grounded, then with D, CLK, and CLR grounded.

'AS174 switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS174		SN74AS174		
			MIN	MAX	MIN	MAX	
f_{max}			100		100		MHz
t_{PHL}	$\overline{CLR}$	Any Q	5	15	5	14	ns
t_{PLH}	CLK	Any Q	3.5	9.5	3.5	8	ns
t_{PHL}			4.5	11.5	4.5	10	

'AS175 switching characteristics (see Note 2)

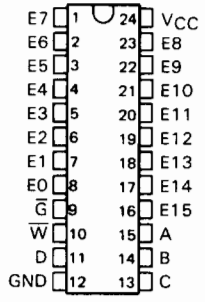
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS175		SN74AS175		
			MIN	MAX	MIN	MAX	
f_{max}			100		100		MHz
t_{PLH}	$\overline{CLR}$	Any Q or $\overline{Q}$	4	10	4	9	ns
t_{PHL}			4.5	15	4.5	13	
t_{PLH}	CLK	Any Q or $\overline{Q}$	4	8.5	4	7.5	ns
t_{PHL}			4	11	4	10	

NOTE 2: For load circuit and voltage waveforms, see page 1-12 of The TTL Data Book, Volume 3.

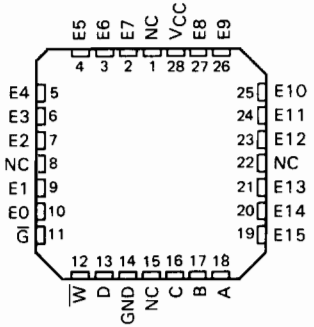
TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

- **4-Line to 1-Line Multiplexer that can Select 1 of 16 Data Inputs**
- **Applications:**
  Boolean Function Generator
  Parallel-to-Serial Converter
  Data Source Selector
- **Buffered 3-State Bus Driver Inputs Permit Multiplexing from N Lines to One Line**
- **Dependable Texas Instruments Quality and Reliability**

SN54AS250 . . . JT PACKAGE
SN74AS250 . . . NT PACKAGE
(TOP VIEW)



SN54AS250 . . . FH CHIP CARRIER PACKAGE
SN74AS250 . . . FN CHIP CARRIER PACKAGE
(TOP VIEW)



NC – No internal connection

description

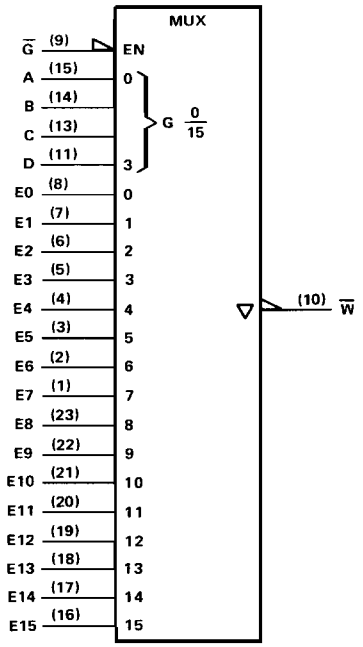
The 'AS250 provides full binary decoding to select one of sixteen data sources with an inverting $\overline{W}$ output. The selected sources are buffered with symmetrical propagation delay times. This reduces the possibility of transients occurring at the output.

A buffered enable output ($\overline{G}$) may be used for n-line-to-one-line cascading. Taking the $\overline{G}$ high will place the output in a high-impedance state. In the high-impedance state, the output neither loads nor drives the bus lines significantly.

The enable ($\overline{G}$) does not affect the internal operations of the data selector/multiplexer. New data can be set up while the outputs are disabled.

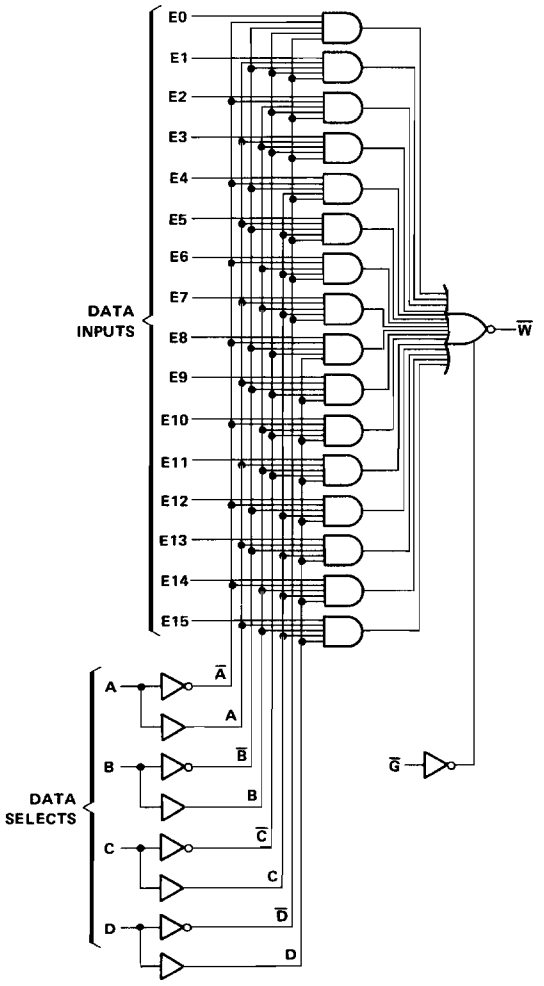
The SN54AS250 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74AS250 is characterized for operation from 0°C to 70°C.

logic symbol



Pin numbers shown are for J or N packages.

logic diagram (positive logic)



TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

FUNCTION TABLE

INPUT						OUTPUT
$\overline{G}$	A	B	C	D	Ei	$\overline{W}$
L	L	L	L	L	E0	E0
L	H	L	L	L	E1	E1
L	L	H	L	L	E2	E2
L	H	H	L	L	E3	E3
L	L	L	H	L	E4	E4
L	H	L	H	L	E5	E5
L	L	H	H	L	E6	E6
L	H	H	H	L	E7	E7
L	L	L	L	H	E8	E8
L	H	L	L	H	E9	E9
L	L	H	L	H	E10	E10
L	H	H	L	H	E11	E11
L	L	L	H	H	E12	E12
L	H	L	H	H	E13	E13
L	L	H	H	H	E14	E14
L	H	H	H	H	E15	E15
H	X	X	X	X	X	Z

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS250 . . . . . −55°C to 125°C
SN74AS250 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS250			SN74AS250			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			32			48	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS250			SN74AS250			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC} −2			V_{CC} −2			V
	V_{CC} = 4.5 V,	I_{OH} = −12 mA	2.4	3.2					
	V_{CC} = 4.5 V,	I_{OH} = −15 mA				2.4	3.3		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.25	0.5				V
	V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			−50			−50	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		26			26	42	mA
		Outputs low		31			31	50	
		Outputs disabled		30			30	48	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX					UNIT
			SN54AS250			SN74AS250		
			MIN	TYP†	MAX	MIN	MAX	
t_{PLH}	DATA	$\overline{W}$		5		3	8	ns
t_{PHL}				3.5		2	6	
t_{PLH}	SELECT	$\overline{W}$		7.5		4	13	ns
t_{PHL}				7.5		4	10	
t_{PZH}	$\overline{G}$	$\overline{W}$		4.5		2	7	ns
t_{PZL}				12		4	20	
t_{PHZ}	$\overline{G}$	$\overline{W}$		3.5		2	6	ns
t_{PLZ}				4.5		2	6	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: For load circuit and voltage waveforms, see page 1-12 of the TTL Data Book, Volume 3.

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

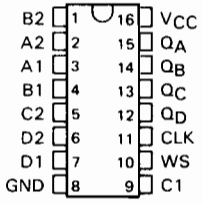
D2661, DECEMBER 1983 – REVISED FEBRUARY 1984

- **Selects One of Two 4-Bit Data Sources and Stores Data Synchronously with System Clock**
- **Applications:**
  Dual Source for Operands and Constants in Arithmetic Processor; Can Release Processor Register Files for Acquiring New Data

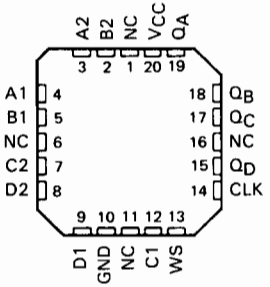
  Implements Separate Registers Capable of Parallel Exchange of Contents, yet Retains External Load Capability

  Has Universal-Type Register for Implementing Various Shift Patterns; even Has Compound Left-Right Capability
- **Dependable Texas Instruments Quality and Reliability**

SN54AS298 . . . J PACKAGE
SN74AS298 . . . N PACKAGE
(TOP VIEW)



SN54AS298 . . . FH PACKAGE
SN74AS298 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

description

This quadruple two-input multiplexer with storage provides essentially the equivalent functional capabilities of two separate MSI functions (SN54AS157/SN74AS157 and SN54AS175/SN74AS175) in a single 16-pin package.

When the word-select (WS) input is low, Word 1 (A1, B1, C1, D1 is applied to the flip-flops. A high input to the word-select (WS) will cause the selection of Word 2 (A2, B2, C2, D2). The selected word is clocked to the output terminals on the negative-going edge of the clock pulse.

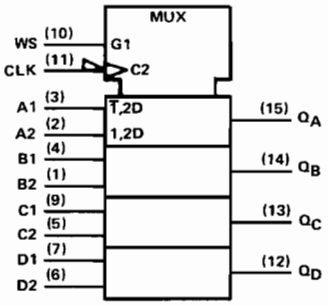
The SN54AS298 is characterized for operation over the full military range of −55°C to 125°C. The SN74AS298 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

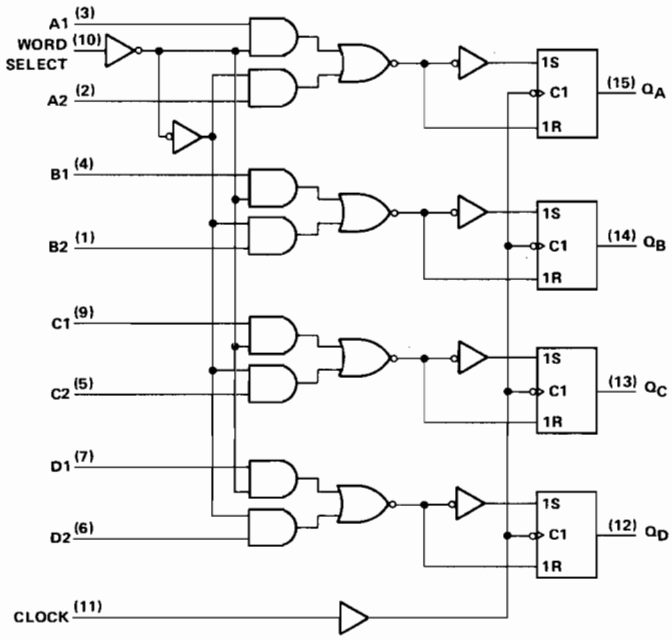
INPUTS		OUTPUTS			
WORD SELECT	CLOCK	Q_A	Q_B	Q_C	Q_D
L	↓	a1	b1	c1	d1
H	↓	a2	b2	c2	d2
X	H	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

H = high level (steady state)
L = low level (steady state)
X = irrelevant (any input, including transitions)
↓ = transition from high to low level
a1, a2, etc. = the level of steady-state input at A1, A2, etc.
Q_{A0}, Q_{B0}, etc. = the level of Q_A, Q_B, etc. entered on the most-recent ↓ transition of the clock input.

logic symbol



logic diagram (positive logic)



Pin numbers shown are for J and N packages.

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS298 . . . . . −55°C to 125°C
SN74AS298 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54AS298			SN74AS298			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−2			−2	mA
I_{OL}	Low-level output current				20			20	mA
f_{clock}	Clock frequency		0		100	0		100	MHz
t_w	Pulse duration, CLK high or low		5			5			ns
t_{su}	Setup time before CLK ↓	Data	4.5			4.5			ns
		Word Select	13			13			
t_h	Hold time after CLK ↓	Data	3.5			3.5			ns
		Word Select	1			1			
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS298			SN74AS298			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1			−1	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5		0.35	0.5	V
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	WS	V_{CC} = 5.5 V,	V_I = 2.7 V			40			40	μA
	All other					20			20	
I_{IL}	WS	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.75			−0.75	mA
	All other					−0.5			−0.5	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CCH}		V_{CC} = 5.5 V			21	33		21	33	mA
I_{CCL}		V_{CC} = 5.5 V			22	36		22	36	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characterisitcs (see Note 1)

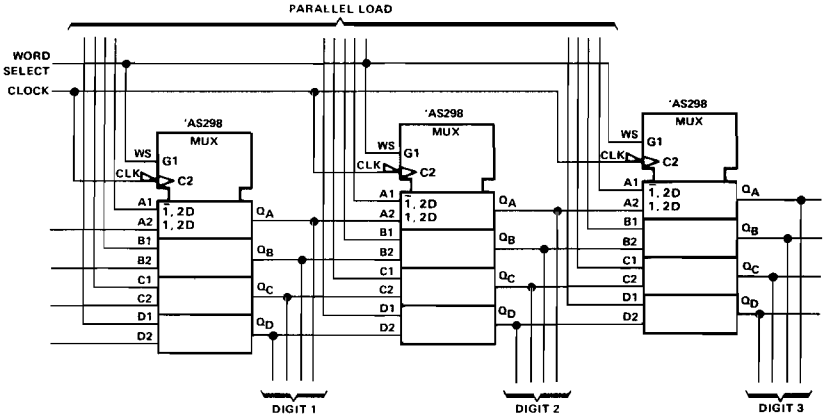
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS298		SN74AS298		
			MIN	MAX	MIN	MAX	
f_{max}			100		100		MHz
t_{PLH}	CLK	Q	2	16	2	9	ns
t_{PHL}			1	12	1	11	

NOTE 1: For load circuit and voltage waveforms, see page 1-12 of the TTL Data Book, Volume 3.

TYPICAL APPLICATION DATA

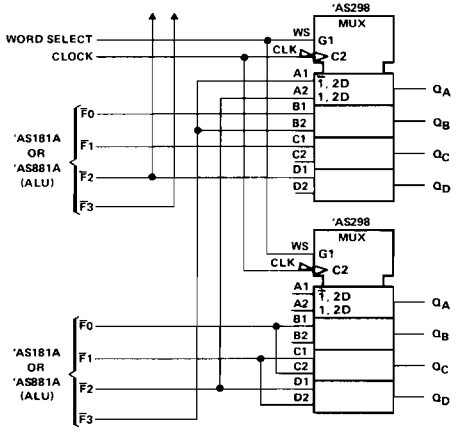
This versatile multiplexer/register can be connected to operate as a shift register that can shift N-places in a single clock pulse.

The following figure illustrates a BCD shift register that will shift an entire 4-bit BCD digit in one clock pulse.



When the word-select input is high and the registers are clocked, the contents of register 1 is transferred (shifted) to register 2, etc. In effect, the BCD digits are shifted one position. In addition, this application retains a parallel-load capability which means that new BCD data can be entered in the entire register with one clock pulse. This arrangement can be modified to perform the shifting of binary data for any number of bit locations.

Another function that can be implemented with the 'AS298 is a register that can be designed specifically for supporting multiplier or division operations. The example below is a one-place/two-place shift register.



When word select is low and the register is clocked, the outputs of the arithmetic/logic units (ALUs) are shifted one place. When word select is high and the registers are clocked, the data is shifted two places.

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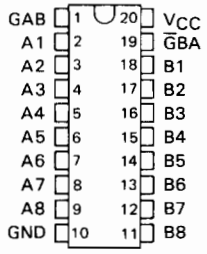
D2661, DECEMBER 1982—REVISED FEBRUARY 1984

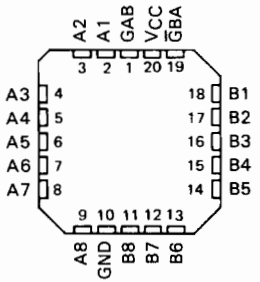
- **Bus Transceivers in High-Density 20-Pin DIP and the New Plastic and Ceramic Chip Carriers**
- **Local Bus-Latch Capability**
- **Choice of True or Inverting Logic**
- **Choice of 3-State or Open-Collector Outputs**
- **Dependable Texas Instruments Quality and Reliability**

DEVICE	OUTPUT	LOGIC
'ALS620A, 'AS620	3-State	Inverting
'ALS621A, 'AS621	Open-Collector	True
'ALS622A, 'AS622	Open-Collector	Inverting
'ALS623A, 'AS623	3-State	True

SN54ALS', SN54AS' . . . J PACKAGE
SN74ALS', SN74AS' . . . N PACKAGE
(TOP VIEW)



SN54ALS', SN54AS' . . . FH PACKAGE
SN74ALS', SN74AS' . . . FN PACKAGE
(TOP VIEW)



description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation allows for maximum flexibility in timing.

These devices allow data transmission from A bus to the B bus or from the B bus to the A bus depending upon the logic levels at the enable inputs ($\overline{G}BA$ and GAB).

The enable inputs can be used to disable the device so that the buses are effectively isolated.

The dual-enable configuration gives the octal bus transceivers the capability to store data by simultaneous enabling of $\overline{G}BA$ and GAB. Each output reinforces its input in this transceiver configuration. Thus, when both control inputs are enabled and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines (16 in all) will remain at their last states. The 8-bit codes appearing on the two sets of buses will be identical for the 'ALS621A, 'AS621 and 'ALS623A, 'AS623 or complementary for the 'ALS620A, 'AS620 and 'ALS622A, 'AS622.

The -1 versions of the SN74ALS' parts are identical to their standard versions except that the recommended maximum I_{OL} is increased to 48 mA. There are no -1 versions of the SN54ALS' parts.

The SN54' family is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74' family is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

ENABLE INPUTS		OPERATION	
$\overline{G}BA$	GAB	'ALS620A, 'ALS622A 'AS620, 'AS622	'ALS621A, 'ALS623A 'AS621, 'AS623
L	L	$\overline{B}$ data to A bus	B data to A bus
H	H	$\overline{A}$ data to B bus	A data to B bus
H	L	Isolation	Isolation
L	H	$\overline{B}$ data to A bus, $\overline{A}$ data to B bus	B data to A bus, A data to B bus

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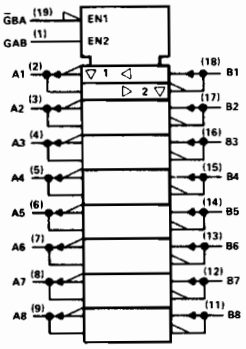
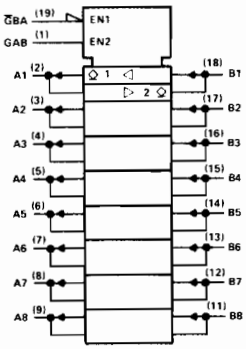
logic symbols

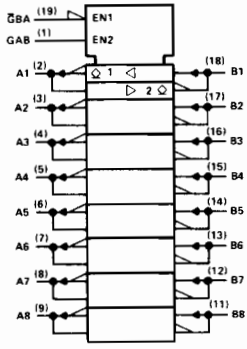
'ALS620A, 'AS620



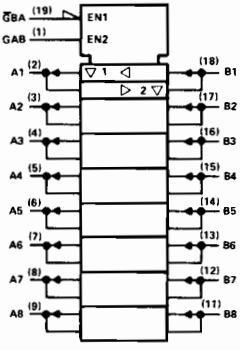
'ALS621A, 'AS621



'ALS622A, 'AS622



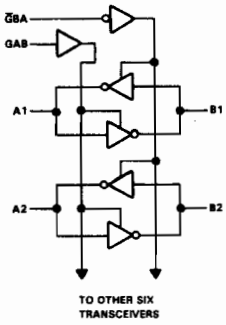
'ALS623A, 'AS623



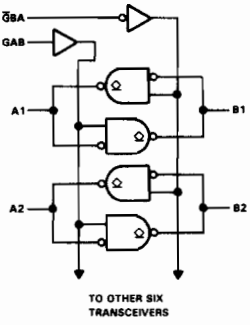
Pin numbers shown are for J and N packages.

logic diagrams (positive logic)

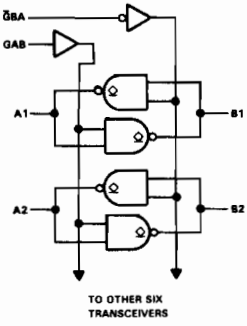
'ALS620A, 'AS620



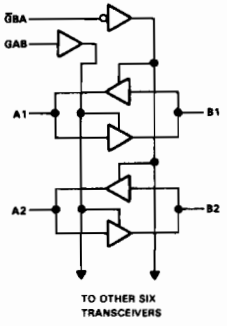
'ALS621A, 'AS621



'ALS622A, 'AS622



'ALS623A, 'AS623



TEXAS INSTRUMENTS
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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN54ALS620A, SN54ALS623A . . . . . −55°C to 125°C
SN74ALS620A, SN74ALS623A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS620A SN54ALS623A			SN74ALS620A SN74ALS623A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			12			24	mA
							48†	
T_A	Operating free-air temperature	−55		125	0		70	°C

†The extended limits apply only if V_{CC} is maintained between 4.75 V and 5.25 V.
The 48-mA limit applies for the SN74ALS620A-1 and SN74ALS623A-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS620A SN54ALS623A			SN74ALS620A SN74ALS623A			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V, (I_{OL} = 48 mA for −1 versions)	I_{OL} = 24 mA					0.35	0.5	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	A or B ports§					20			20	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
	A or B ports§					−0.1			−0.1	
I_O¶		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'ALS620A	V_{CC} = 5.5 V	Outputs high		24	39		24	34	mA
			Outputs low		31	49		31	44	
			Outputs disabled		33	52		33	47	
	'ALS623A	V_{CC} = 5.5 V	Outputs high		32	48		32	43	
			Outputs low		39	55		39	50	
			Outputs disabled		42	60		42	55	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C
§For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
¶The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'ALS620A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS620A		SN74ALS620A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	B	2	12	2	10	ns
t_{PHL}			2	12	2	10	
t_{PLH}	B	A	2	12	2	10	ns
t_{PHL}			2	12	2	10	
t_{PZH}	$\overline{G}$BA	A	3	23	3	17	ns
t_{PZL}			5	31	5	25	
t_{PHZ}	$\overline{G}$BA	A	2	14	2	12	ns
t_{PLZ}			3	22	3	18	
t_{PZH}	GAB	B	3	23	3	18	ns
t_{PZL}			5	31	5	25	
t_{PHZ}	GAB	B	2	14	2	12	ns
t_{PLZ}			3	22	3	18	

'ALS623A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS623A		SN74ALS623A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	B	2	15	2	13	ns
t_{PHL}			3	13	3	11	
t_{PLH}	B	A	2	15	2	13	ns
t_{PHL}			3	13	3	11	
t_{PZH}	$\overline{G}$BA	A	5	25	5	22	ns
t_{PZL}			5	25	5	22	
t_{PHZ}	$\overline{G}$BA	A	2	19	2	16	ns
t_{PLZ}			2	23	2	19	
t_{PZH}	GAB	B	5	25	5	22	ns
t_{PZL}			5	25	5	22	
t_{PHZ}	GAB	B	2	19	2	16	ns
t_{PLZ}			2	23	2	19	

NOTE 1: For load circuit and voltage waveforms, see page 1-12 of the TTL Data Book, Volume 3.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs and I/O ports . . . . . 7 V
Operating free-air temperature range: SN54ALS621A, SN54ALS622A . . . . . −55°C to 125°C
SN74ALS621A, SN74ALS622A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS621A SN54ALS622A			SN74ALS621A SN74ALS622A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			12			24	mA
							48†	
T_A	Operating free-air temperature	−55		125	0		70	°C

†The extended limits apply only if V_{CC} is maintained between 4.75 V and 5.25 V.
The 48-mA limit applies for the SN74ALS621A-1 and SN74ALS622A-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS621A SN54ALS622A			SN74ALS621A SN74ALS622A			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V, I_I = −18 mA				−1.5			−1.5	V
I_{OH}		V_{CC} = 4.5 V, V_{OH} = 5.5 V				0.1			0.1	mA
V_{OL}		V_{CC} = 4.5 V, I_{OL} = 12 mA			0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V, I_{OL} = 24 mA (I_{OL} = 48 mA for -1 versions)						0.35	0.5	
I_I	Control inputs	V_{CC} = 5.5 V, V_I = 7 V				0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V, V_I = 5.5 V				0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V, V_I = 2.7 V				20			20	μA
	A or B ports§					20			20	
I_{IL}	Control inputs	V_{CC} = 5.5 V, V_I = 0.4 V				−0.1			−0.1	mA
	A or B ports§					−0.1			−0.1	
I_{CC}	'ALS621A	V_{CC} = 5.5 V	Outputs high		29	45		29	40	mA
			Outputs low		35	53		35	48	
	'ALS622A	V_{CC} = 5.5 V	Outputs high		11	20		11	15	
			Outputs low		20	33		20	28	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

'ALS621A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 680 Ω, T_A = MIN to MAX				UNIT
			SN54ALS621A		SN74ALS621A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	B	10	45	10	33	ns
t_{PHL}			5	24	5	20	
t_{PLH}	B	A	10	45	10	33	ns
t_{PHL}			5	24	5	20	
t_{PLH}	$\overline{G}BA$	A	10	47	10	39	ns
t_{PHL}			12	40	12	35	
t_{PLH}	GAB	B	10	47	10	39	ns
t_{PHL}			12	40	12	35	

'ALS622A switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 680 Ω, T_A = MIN to MAX				UNIT
			SN54ALS622A		SN74ALS622A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	B	8	42	8	35	ns
t_{PHL}			5	23	5	19	
t_{PLH}	B	A	8	42	8	35	ns
t_{PHL}			5	23	5	19	
t_{PLH}	$\overline{G}BA$	A	8	45	8	38	ns
t_{PHL}			10	40	10	35	
t_{PLH}	GAB	B	8	45	8	38	ns
t_{PHL}			10	40	10	35	

NOTE 1: For load circuit and voltage waveforms, see page 1-12 of the TTL Data Book, Volume 3.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN54AS620, SN54AS623 . . . . . −55°C to 125°C
SN74AS620, SN74AS623 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS620 SN54AS623			SN74AS620 SN74AS623			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			48			64	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS620 SN54AS623			SN74AS620 SN74AS623			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 48 mA		0.30	0.55				V
		V_{CC} = 4.5 V,	I_{OL} = 64 mA					0.35	0.55	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	A or B ports‡					70			70	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
	A or B ports‡					−0.75			−0.75	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−50		−150	−50		−150	mA
I_{CC}	'AS620	V_{CC} = 5.5 V	Outputs high		35	57		35	57	mA
			Outputs low		74	122		74	122	
			Outputs disabled		48	77		48	77	
	'AS623	V_{CC} = 5.5 V	Outputs high		57	93		57	93	
			Outputs low		116	189		116	189	
			Outputs disabled		71	116		71	116	

†All typical values are at V_{CC2} = 5 V, T_A = 25°C.
‡For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'AS620 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS620		SN74AS620		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	B	1	8	1	7	ns
t_{PHL}			2	7	2	6	
t_{PLH}	B	A	1	8	1	7	ns
t_{PHL}			2	7	2	6	
t_{PZH}	$\overline{G}$BA	A	2	8.5	2	8	ns
t_{PZL}			2	10	2	9	
t_{PHZ}	$\overline{G}$BA	A	1	7.5	1	6	ns
t_{PLZ}			2	15	2	12	
t_{PZH}	GAB	B	2	9	2	8	ns
t_{PZL}			2	10.5	2	9	
t_{PHZ}	GAB	B	1	6.5	1	6	ns
t_{PLZ}			2	16	2	13	

'AS623 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS623		SN74AS623		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	B	1	10	1	9	ns
t_{PHL}			1	9	1	8	
t_{PLH}	B	A	1	10	1	9	ns
t_{PHL}			1	9.5	1	8.5	
t_{PZH}	$\overline{G}$BA	A	2	11.5	2	11	ns
t_{PZL}			2	11	2	10	
t_{PHZ}	$\overline{G}$BA	A	1	8.5	1	7.5	ns
t_{PLZ}			1	13.5	1	11.5	
t_{PZH}	GAB	B	2	13	2	11.5	ns
t_{PZL}			2	12	2	11	
t_{PHZ}	GAB	B	1	8	1	7	ns
t_{PLZ}			1	10.5	1	9	

NOTE 1: For load circuit and voltage waveforms, see page 1-12 of the TTL Data Book, Volume 3.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs and I/O ports . . . . . 7 V
Operating free-air temperature range: SN54AS621, SN54AS622 . . . . . −55 °C to 125 °C
SN74AS621, SN74AS622 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54AS621 SN54AS622			SN74AS621 SN74AS622			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			48			64	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS621 SN54AS622			SN74AS621 SN74AS622			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
I_{OH}		V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 48 mA		0.30	0.5				V
		V_{CC} = 4.5 V,	I_{OL} = 64 mA					0.35	0.5	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	A or B ports‡					70			70	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
	A or B ports‡					−0.75			−0.75	
I_{CC}	'AS621	V_{CC} = 5.5 V	Outputs high		48	79		48	79	mA
			Outputs low		116	189		116	189	
	'AS622	V_{CC} = 5.5 V	Outputs high		24	39		24	39	
			Outputs low		63	103		63	103	

†All typical values are at V_{CC} = 5 V, T_A = 25 °C
‡For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

'AS621 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS621		SN74AS621		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	B	5	28.5	5	24	ns
t_{PHL}			1	8.5	1	7.5	
t_{PLH}	B	A	5	23	5	21	ns
t_{PHL}			1	8.5	1	7.5	
t_{PLH}	$\overline{G}BA$	A	5	24	5	21	ns
t_{PHL}			1	10	1	9	
t_{PLH}	GAB	B	5	26	5	22	ns
t_{PHL}			1	11	1	10	

'AS622 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS622		SN74AS622		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	B	5	28.5	5	24.5	ns
t_{PHL}			1	8.5	1	8	
t_{PLH}	B	A	5	30	5	25	ns
t_{PHL}			1	8.5	1	8	
t_{PLH}	$\overline{G}BA$	A	5	26	5	22	ns
t_{PHL}			1	11.5	1	10	
t_{PLH}	GAB	B	5	26	5	23	ns
t_{PHL}			1	11.5	1	10.5	

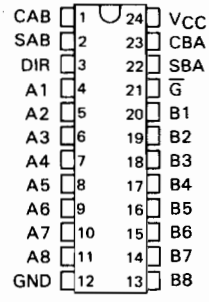
NOTE 1: For load circuit and voltage waveforms, see page 1-12 of the TTL Data Book, Volume 3.

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

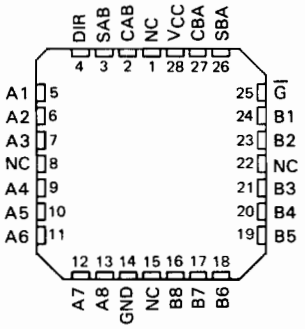
- **Independent Registers for A and B Buses**
- **Multiplexed Real-Time and Stored Data**
- **Choice of True or Inverting Data Paths**
- **Choice of 3-State or Open-Collector Outputs**
- **Included Among the Package Options Are Compact 24-pin 300-mil Wide DIPs and Both 28-pin Plastic and Ceramic Chip Carriers**
- **Dependable Texas Instruments Quality and Reliability**

DEVICE	OUTPUT	LOGIC
'ALS646, 'AS646	3-State	True
'ALS647	Open-Collector	True
'ALS648, 'AS648	3-State	Inverting
'ALS649	Open-Collector	Inverting

SN54ALS', SN54AS' . . . JT PACKAGE
SN74ALS', SN74AS' . . . NT PACKAGE
(TOP VIEW)



SN54ALS', SN54AS' . . . FH PACKAGE
SN74ALS', SN74AS' . . . FN PACKAGE
(TOP VIEW)



description

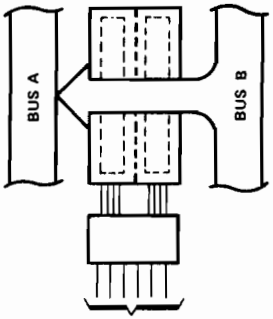
These devices consist of bus transceiver circuits with 3-state or open-collector outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers on the low-to-high transition of the appropriate clock pin (CAB or CBA). The following examples demonstrate the four fundamental bus-management functions that can be performed with the octal bus transceivers and registers.

Enable ($\overline{G}$) and direction (DIR) pins are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both. The select controls (SAB and SBA) can multiplex stored and real-time (transparent mode) data. The direction control determines which bus will receive data when enable $\overline{G}$ is active (low). In the isolation mode (control $\overline{G}$ high), A data may be stored in one register and/or B data may be stored in the other register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

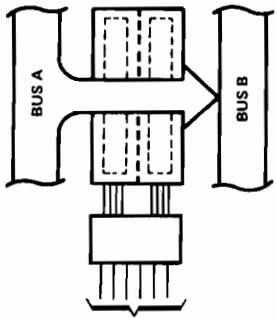
The –1 versions of the SN74ALS' parts are identical to the standard versions except that the recommended maximum I_{OL} is increased to 48 milliamperes. There are no –1 versions of the SN54ALS' parts.

The SN54' family is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74' family is characterized for operation from 0°C to 70°C.



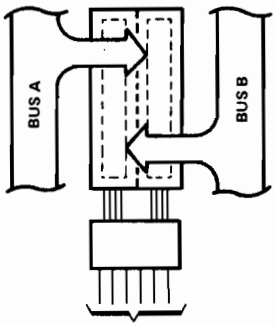
(21) G	(3) DIR	(1) CAB	(23) CBA	(2) SAB	(22) SBA
L	L	X	HorL	X	L

REAL-TIME TRANSFER
BUS B TO BUS A



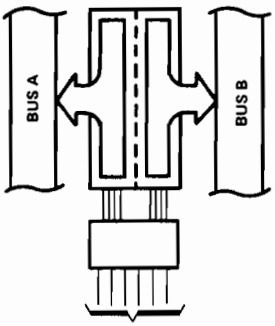
(21) G	(3) DIR	(1) CAB	(23) CBA	(2) SAB	(22) SBA
L	H	HorL	X	L	X

REAL-TIME TRANSFER
BUS A TO BUS B



(21) G	(3) DIR	(1) CAB	(23) CBA	(2) SAB	(22) SBA
X	X	↑	X	X	X
X	X	X	↑	X	X
H	X	↑	↑	X	X

STORAGE FROM
A, B, OR A AND B



(21) G	(3) DIR	(1) CAB	(23) CBA	(2) SAB	(22) SBA
L	L	X	X	X	H
L	H	X	X	H	X

TRANSFER
STORED DATA
TO A OR B

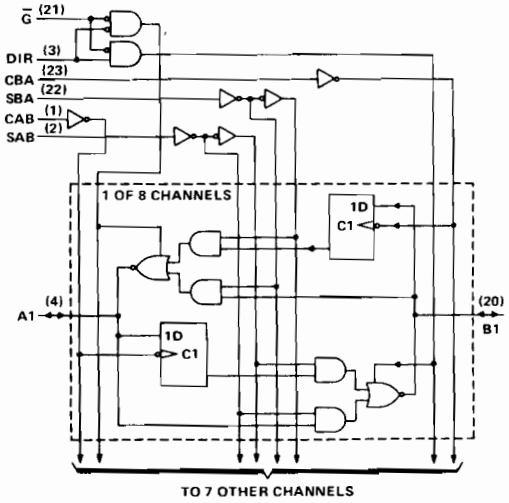
FUNCTION TABLE

INPUTS						DATA I/O*		OPERATION OR FUNCTION	
$\overline{G}$	DIR	CAB	CBA	SAB	SBA	A1 THRU A8	B1 THRU B8	'ALS646, 'ALS647 'AS646	'ALS648, 'ALS649 'AS648
X	X	↑	X	X	X	Input	Not specified	Store A, B unspecified	Store A, B unspecified
X	X	X	↑	X	X	Not specified	Input	Store B, A unspecified	Store B, A unspecified
H	X	↑	↑	X	X	Input	Input	Store A and B Data	Store A and B Data
H	X	H or L	H or L	X	X			Isolation, hold storage	Isolation, hold storage
L	L	X	H or L	X	L	Output	Input	Real-Time B Data to A Bus	Real-Time $\overline{B}$ Data to A Bus
L	L	X	X	X	H			Stored B Data to A Bus	Stored $\overline{B}$ Data to A Bus
L	H	H or L	X	L	X	Input	Output	Real-Time A Data to B Bus	Real-Time $\overline{A}$ Data to B Bus
L	H	X	X	H	X			Stored A Data to B Bus	Stored $\overline{A}$ Data to B Bus

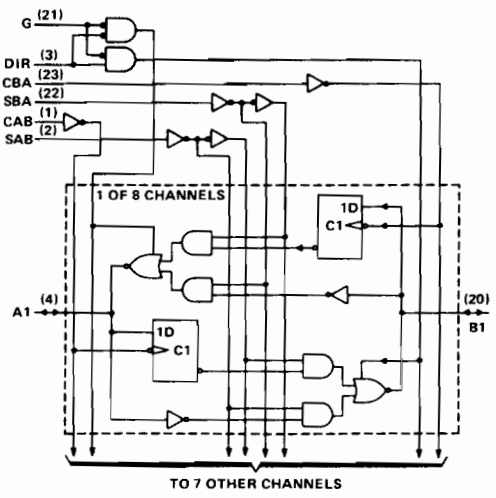
*The data output functions may be enabled or disabled by various signals at the $\overline{G}$ and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

functional block diagrams (positive logic)

ALS646, 'AS646, 'ALS647



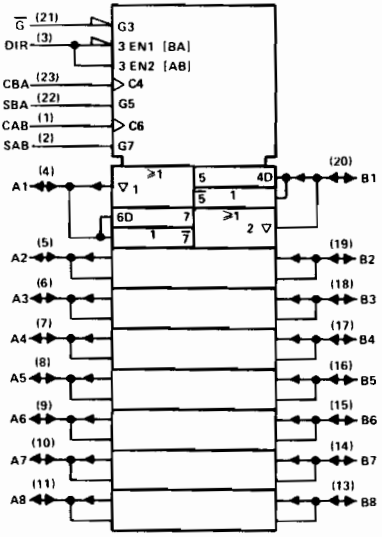
'ALS648, 'AS648, 'ALS649



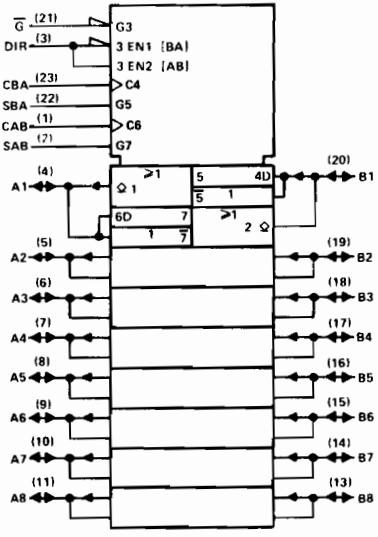
Pin numbers shown are for JT and NT packages.

logic symbols

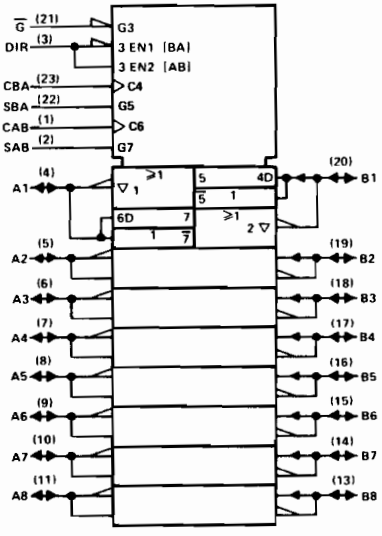
'ALS646, 'AS646



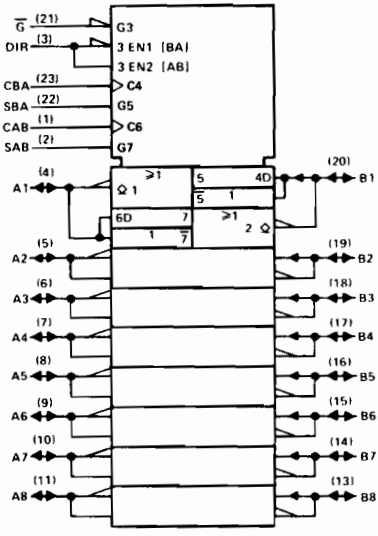
'ALS647



'ALS648, 'AS648



'ALS649



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: Control inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN54ALS646, SN54ALS648 . . . . . −55 °C to 125 °C
SN74ALS646, SN74ALS648 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS646 SN54ALS648			SN74ALS646 SN74ALS648			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			12			24	mA
							48†	
f_{clock}	Clock frequency							MHz
t_w	Pulse duration, clocks high or low							ns
t_{su}	Setup time, A before CAB† or B before CBA†							ns
t_h	Hold time, A after CAB† or B after CBA†							ns
T_A	Operating free-air temperature	−55		125	0		70	°C

† The extended condition applies if V_{CC} is maintained between 4.75 V and 5.25 V.
The 48-mA limit applies for the SN74ALS646-1 and SN74ALS648-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS646 SN54ALS648			SN74ALS646 SN74ALS648			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V, (I_{OL} = 48 mA for −1 versions)	I_{OL} = 24 mA					0.35	0.5	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	A or B ports§					20			20	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
	A or B ports§					−0.2			−0.2	
I_O¶		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'ALS646	V_{CC} = 5.5 V	Outputs high		60			60		mA
			Outputs low		68			68		
			Outputs disabled		68			68		
	'ALS648		Outputs high		52			52		
			Outputs low		57			57		
			Outputs disabled		58			58		

‡ All typical values are at V_{CC} = 5 V, T_A = 25 °C
§ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
¶ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
Additional information on these products can be obtained from the factory as it becomes available.

PRODUCT PREVIEW

This page contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

'ALS646 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS646			SN74ALS646			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
f_{max}									MHz
t_{PLH}	CBA or CAB	A or B		11			11		ns
t_{PHL}				13			13		
t_{PLH}	A or B	B or A		8			8		ns
t_{PHL}				8			8		
t_{PLH}	SBA or SAB‡ (with A or B high)	A or B		16			16		ns
t_{PHL}				16			16		
t_{PLH}	SBA or SAB‡ (with A or B low)	A or B		15			15		ns
t_{PHL}				12			12		
t_{PZH}	$\overline{G}$	A or B		17			17		ns
t_{PZL}				20			20		
t_{PHZ}	$\overline{G}$	A or B		10			10		ns
t_{PLZ}				12			12		
t_{PZH}	DIR	A or B		17			17		ns
t_{PZL}				20			20		
t_{PHZ}	DIR	A or B		10			10		ns
t_{PLZ}				12			12		

'ALS648 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS648			SN74ALS648			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
f_{max}									MHz
t_{PLH}	CBA or CAB	A or B		11			11		ns
t_{PHL}				13			13		
t_{PLH}	A or B	B or A		10			10		ns
t_{PHL}				12			12		
t_{PLH}	SBA or SAB‡ (with A or B high)	A or B		16			16		ns
t_{PHL}				16			16		
t_{PLH}	SBA or SAB‡ (with A or B low)	A or B		15			15		ns
t_{PHL}				15			15		
t_{PZH}	$\overline{G}$	A or B		17			17		ns
t_{PZL}				20			20		
t_{PHZ}	$\overline{G}$	A or B		10			10		ns
t_{PLZ}				12			12		
t_{PZH}	DIR	A or B		17			17		ns
t_{PZL}				20			20		
t_{PHZ}	DIR	A or B		10			10		ns
t_{PLZ}				12			12		

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

Additional information on these products can be obtained from the factory as it becomes available.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS647, SN54ALS649 . . . . . −55 °C to 125 °C
SN74ALS647, SN74ALS649 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54ALS647 SN54ALS649			SN74ALS647 SN74ALS649			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			12			24	mA
							48†	
f_{clock}	Clock frequency							MHz
t_w	Pulse duration, clocks high or low							ns
t_{su}	Setup time, A before CAB† or B before CBA†							ns
t_h	Hold time, A after CAB† or B after CBA†							ns
T_A	Operating free-air temperature	−55		125	0		70	°C

† The extended condition applies if V_{CC} is maintained between 4.75 and 5.25 V.
The 48-mA limit applies for the SN74ALS647-1 and SN74ALS649-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS647 SN54ALS649			SN74ALS647 SN74ALS649			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
I_{OH}		V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4				V
		V_{CC} = 4.5 V, (I_{OL} = 48 mA for −1 versions)	I_{OL} = 24 mA					0.35	0.5	
I_I	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	mA
	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	
I_{IH}	A or B ports§	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	Control inputs					20			20	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
	A or B ports§					−0.2			−0.2	
I_{CC}	'ALS647	V_{CC} = 5.5 V	Outputs high		52			52		mA
			Outputs low		62			62		
	'ALS649		Outputs high		50			50		
			Outputs low		60			60		

‡ All typical values are at V_{CC} = 5 V, T_A = 25 °C
§ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
Additional information on these products can be obtained from the factory as it becomes available.

'ALS647 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 680 Ω, T_A = MIN to MAX						UNIT
			SN54ALS647			SN74ALS647			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
f_{max}									MHz
t_{PLH}	CBA or CAB	A or B		24			24		ns
t_{PHL}				15			15		
t_{PLH}	A or B	B or A		24			24		ns
t_{PHL}				12			12		
t_{PLH}	SBA or SAB‡ (with A or B high)	A or B		26			26		ns
t_{PHL}				15			15		
t_{PLH}	SBA or SAB‡ (with A or B low)	A or B		26			26		ns
t_{PHL}				15			15		
t_{PLH}	$\overline{G}$	A or B		24			24		ns
t_{PHL}				17			17		
t_{PLH}	DIR	A or B		24			24		ns
t_{PHL}				17			17		

'ALS649 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 680 Ω, T_A = MIN to MAX						UNIT
			SN54ALS649			SN74ALS649			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
f_{max}									MHz
t_{PLH}	CBA or CAB	A or B		24			24		ns
t_{PHL}				15			15		
t_{PLH}	A or B	B or A		24			24		ns
t_{PHL}				10			10		
t_{PLH}	SBA or SAB‡ (with A or B high)	A or B		26			26		ns
t_{PHL}				15			15		
t_{PLH}	SBA or SAB‡ (with A or B low)	A or B		26			26		ns
t_{PHL}				15			15		
t_{PLH}	$\overline{G}$	A or B		24			24		ns
t_{PHL}				17			17		
t_{PLH}	DIR	A or B		24			24		ns
t_{PHL}				17			17		

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡These parameters are measured with the internal output state of the storage register opposite to that of the bus input.
NOTE 1: For load circuit and voltage waveforms, see page 1-12.
Additional information on these products can be obtained from the factory as it becomes available.

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: Control inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN54AS646, SN54AS648 . . . . . −55°C to 125°C
SN74AS646, SN74AS648 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54AS646 SN54AS648			SN74AS646 SN74AS648			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−12			−15	mA
I_{OL}	Low-level output current				48			64	mA
f_{clock}	Clock frequency		0		75	0		90	MHz
t_w	Pulse duration	Clock high	6			5			ns
		Clock low	7			6			
t_{su}	Setup time, A before CAB↑ or B before CBA↑		7			6			ns
t_h	Hold time, A after CAB↑ or B after CBA↑		0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS646 SN54AS648			SN74AS646 SN74AS648			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 48 mA		0.35	0.55				V
		V_{CC} = 4.5 V,	I_{OL} = 64 mA					0.35	0.55	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	A or B ports‡					70			70	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
	A or B ports‡					−0.75			−0.75	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'AS646	V_{CC} = 5.5 V	Outputs high		120	195		120	195	mA
			Outputs low		130	211		130	211	
			Outputs disabled		130	211		130	211	
	'AS648		Outputs high		110	185		110	185	
			Outputs low		120	195		120	195	
			Outputs disabled		120	195		120	195	

†All typical values are at V_{CC} = 5 V, T_A = 25°C
‡For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'AS646 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS646		SN74AS646		
			MIN	MAX	MIN	MAX	
f_{max}			75		90		MHz
t_{PLH}	CBA or CAB	A or B	2	9.5	2	8.5	ns
t_{PHL}			2	10	2	9	
t_{PLH}	A or B	B or A	2	11	2	9	ns
t_{PHL}			1	8	1	7	
t_{PLH}	SBA or SAB† (with A or B high)	A or B	2	12	2	11	ns
t_{PHL}			2	10	2	9	
t_{PZH}	$\overline{G}$	A or B	2	10	2	9	ns
t_{PZL}			3	15	3	14	
t_{PHZ}	$\overline{G}$	A or B	2	11	2	9	ns
t_{PLZ}			2	11	2	9	
t_{PZH}	DIR	A or B	3	19	3	16	ns
t_{PZL}			3	21	3	18	
t_{PHZ}	DIR	A or B	2	12	2	10	ns
t_{PLZ}			2	12	2	10	

'AS648 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS648		SN74AS648		
			MIN	MAX	MIN	MAX	
f_{max}			75		90		MHz
t_{PLH}	CBA or CAB	A or B	2	9.5	2	8.5	ns
t_{PHL}			2	10	2	9	
t_{PLH}	A or B	B or A	2	9	2	8	ns
t_{PHL}			1	8	1	7	
t_{PLH}	SBA or SAB† (with A or B high)	A or B	2	12	2	11	ns
t_{PHL}			2	10	2	9	
t_{PZH}	$\overline{G}$	A or B	2	10	2	9	ns
t_{PZL}			3	18	3	15	
t_{PHZ}	$\overline{G}$	A or B	2	11	2	9	ns
t_{PLZ}			2	11	2	9	
t_{PZH}	DIR	A or B	3	19	3	16	ns
t_{PZL}			3	21	3	18	
t_{PHZ}	DIR	A or B	2	12	2	10	ns
t_{PLZ}			2	12	2	10	

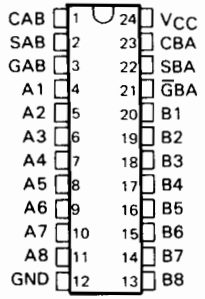
† These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

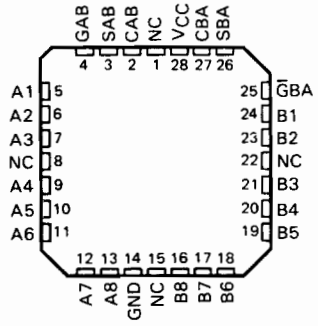
- **Bus Transceivers/Registers**
- **Independent Registers and Enables for A and B Buses**
- **Multiplexed Real-Time and Stored Data**
- **Choice of True and Inverting Data Paths**
- **Choice of 3-State or Open-Collector Outputs to A Bus**
- **Included Among the Package Options Are Compact 24-Pin 300-mil-Wide DIPs and Both 28-Pin Plastic and Ceramic Chip Carriers**
- **Dependable Texas Instruments Quality and Reliability**

DEVICE	A OUTPUT	B OUTPUT	LOGIC
'ALS651, 'AS651	3-State	3-State	Inverting
'ALS652, 'AS652	3-State	3-State	True
'ALS653	Open-Collector	3-State	Inverting
'ALS654	Open-Collector	3-State	True

SN54ALS', SN54AS' . . . JT PACKAGE
SN74ALS', SN74AS' . . . NT PACKAGE
(TOP VIEW)



SN54ALS', SN54AS' . . . FC PACKAGE
SN74ALS', SN74AS' . . . FN PACKAGE
(TOP VIEW)



NC — No internal connection

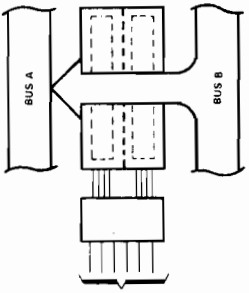
description

These devices consist of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Enable GAB and $\overline{\text{GBA}}$ are provided to control the transceiver functions. SAB and SBA control pins are provided to select whether real-time or stored data is transferred. A low input level selects real-time data, and a high selects stored data. The following examples demonstrate the four fundamental bus-management functions that can be performed with the octal bus transceivers and registers.

Data on the A or B data bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock pins (CAB or CBA) regardless of the select or enable control pins. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling GAB and $\overline{\text{GBA}}$. In this configuration each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state.

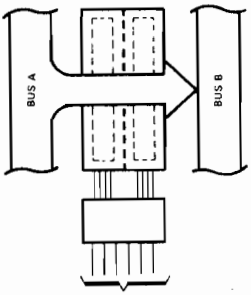
The −1 versions of the SN74ALS651 through SN74ALS654 are identical to the standard versions except that the recommended maximum I_{OL} is increased to 48 milliamperes. There are no −1 versions of the SN54ALS651 through SN54ALS654.

The SN54' family is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74' family is characterized for operation from 0°C to 70°C.



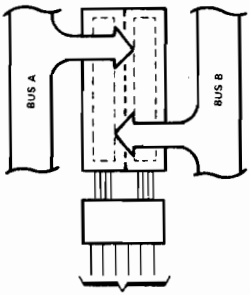
GAB	$\overline{G}$BA	CAB	CBA	SAB	SBA
L	L	X	X	X	L

REAL-TIME TRANSFER
BUS B TO BUS A



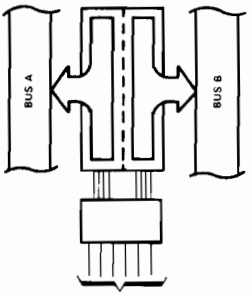
GAB	$\overline{G}$BA	CAB	CBA	SAB	SBA
H	H	X	X	L	X

REAL-TIME TRANSFER
BUS A TO BUS B



GAB	$\overline{G}$BA	CAB	CBA	SAB	SBA
X	H	↑	X	X	X
L	X	X	↑	X	X
L	H	↑	↑	X	X

STORAGE FROM
A AND/OR B



GAB	$\overline{G}$BA	CAB	CBA	SAB	SBA
H	L	HorL	HorL	H	H

TRANSFER
STORED DATA
TO A AND/OR B

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

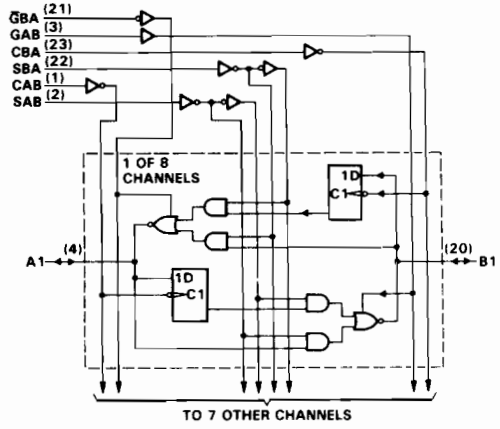
FUNCTION TABLE

INPUTS						DATA I/O*		OPERATION OR FUNCTION	
GAB	$\overline{GBA}$	CAB	CBA	SAB	SBA	A1 THRU A8	B1 THRU B8	'ALS651, 'ALS653 'AS651	'ALS652, 'ALS654 'AS652
L	H	H or L	H or L	X	X	Input	Input	Isolation	Isolation
L	H	↓	↑	X	X			Store A and B Data	Store A and B Data
X	H	↓	H or L	X	X	Input	Not specified	Store A, Hold B	Store A, Hold B
H	H	↑	↓	X	X	Input	Output	Store A in both registers	Store A in both registers
L	X	H or L	↑	X	X	Not specified	Input	Hold A, Store B	Hold A, Store B
L	L	↑	↑	X	X	Output	Input	Store B in both registers	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-Time $\overline{B}$ Data to A Bus	Real-Time B Data to A Bus
L	L	X	H or L	X	H			Stored $\overline{B}$ Data to A Bus	Stored B Data to A Bus
H	H	X	X	L	X	Input	Output	Real-Time $\overline{A}$ Data to B Bus	Real-Time A Data to B Bus
H	H	H or L	X	H	X			Stored $\overline{A}$ Data to B Bus	Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored $\overline{A}$ Data to B Bus and Stored $\overline{B}$ Data to A Bus	Stored A Data to B Bus and Stored B Data to A Bus

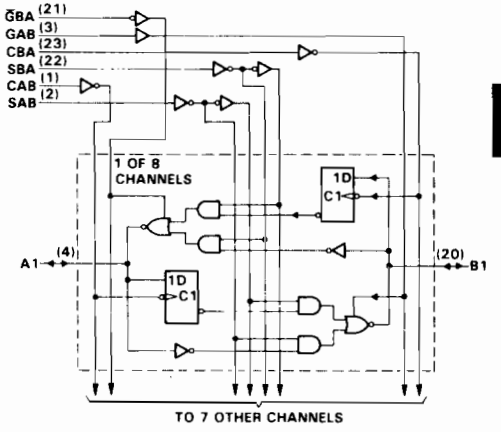
* The data output functions may be enabled or disabled by various signals at the GAB and $\overline{GBA}$ inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

logic diagrams (positive logic)

'ALS651, 'AS651, 'ALS653



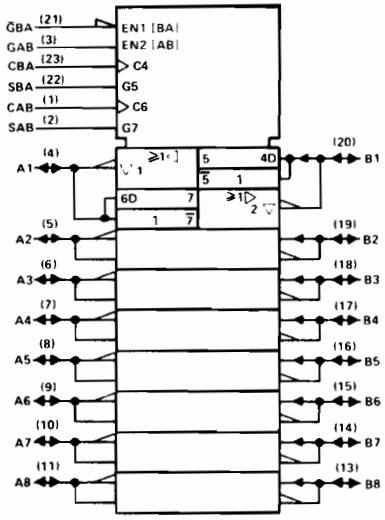
'ALS652, 'AS652, 'ALS654



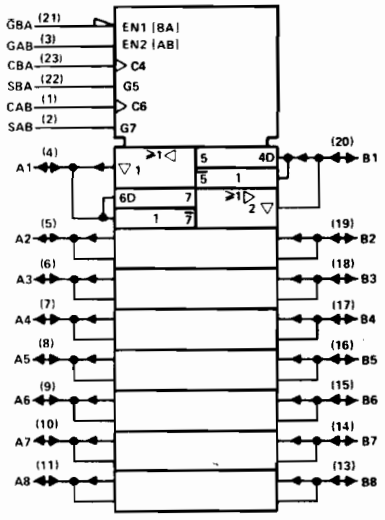
Pin numbers shown are for JT and NT packages.

logic symbols

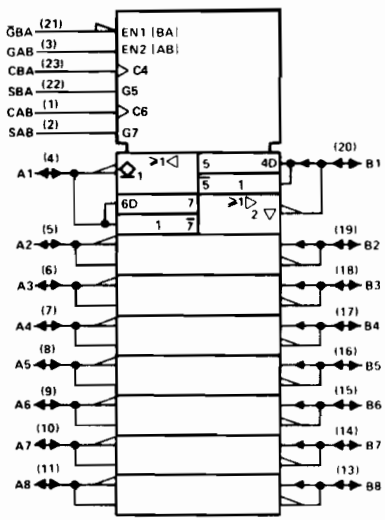
'ALS651, 'AS651



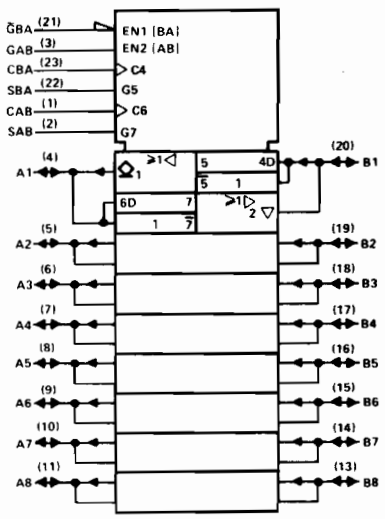
'ALS652, 'AS652



'ALS653



'ALS654



Pin numbers shown are for JT and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: Control inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN54ALS651, SN54ALS652 . . . . . −55 °C to 125 °C
SN74ALS651, SN74ALS652 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

			SN54ALS651 SN54ALS652			SN74ALS651 SN74ALS652			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−12			−15	mA
I_{OL}	Low-level output current				12			24	mA
								48†	
f_{clock}	Clock frequency								MHz
t_w	Pulse duration	CBA or CAB high							ns
		CBA or CAB low							
t_{su}	Setup time before CAB↑ or CBA↑	A or B							ns
t_h	Hold time after CAB↑ or CBA↑	A or B							ns
T_A	Operating free-air temperature		−55		125	0		70	°C

†The extended condition applies if V_{CC} is maintained between 4.75 V and 5.25 V.
The 48-mA limit applies for the SN74ALS651-1 and SN74ALS652-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS651 SN54ALS652			SN74ALS651 SN74ALS652			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V, (I_{OL} = 48 mA for −1 versions)	I_{OL} = 24 mA					0.35	0.5	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	A or B ports§					20			20	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
	A or B ports§					−0.2			−0.2	
I_O¶		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'ALS651	V_{CC} = 5.5 V	Outputs high		52			52		mA
			Outputs low		57			57		
			Outputs disabled		58			58		
	'ALS652		Outputs high		60			60		
			Outputs low		68			68		
			Outputs disabled		68			68		

‡All typical values are at V_{CC} = 5 V, T_A = 25 °C
§For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
¶The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

PRODUCT PREVIEW

This page contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

'ALS651 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS651			SN74ALS651			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
f_{max}									MHz
t_{PLH}	CBA or CAB	A or B		11			11		ns
t_{PHL}				13			13		
t_{PLH}	A or B	B or A		10			10		ns
t_{PHL}				12			12		
t_{PLH}	SBA or SAB‡ (with A or B high)	A or B		16			16		ns
t_{PHL}				16			16		
t_{PLH}	SBA or SAB‡ (with A or B low)	A or B		15			15		ns
t_{PHL}				15			15		
t_{PZH}	$\overline{G}$BA	A		17			17		ns
t_{PZL}				20			20		
t_{PHZ}	$\overline{G}$BA	A		10			10		ns
t_{PLZ}				12			12		
t_{PZH}	GAB	B		19			19		ns
t_{PZL}				22			22		
t_{PHZ}	GAB	B		12			12		ns
t_{PLZ}				14			14		

'ALS652 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS652			SN74ALS652			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
f_{max}									MHz
t_{PLH}	CBA or CAB	A or B		11			11		ns
t_{PHL}				13			13		
t_{PLH}	A or B	B or A		8			8		ns
t_{PHL}				8			8		
t_{PLH}	SBA or SAB‡ (with A or B high)	A or B		16			16		ns
t_{PHL}				16			16		
t_{PLH}	SBA or SAB‡ (with A or B low)	A or B		15			15		ns
t_{PHL}				12			12		
t_{PZH}	$\overline{G}$BA	A		17			17		ns
t_{PZL}				20			20		
t_{PHZ}	$\overline{G}$BA	A		10			10		ns
t_{PLZ}				12			12		
t_{PZH}	GAB	B		19			19		ns
t_{PZL}				22			22		
t_{PHZ}	GAB	B		12			12		ns
t_{PLZ}				14			14		

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡These parameters are measured with the internal output state of the storage register opposite to that of the bus input.
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs and A I/O ports . . . . . 7 V
B I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN54ALS653, SN54ALS654 . . . . . −55 °C to 125 °C
SN74ALS653, SN74ALS654 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

			SN54ALS653 SN54ALS654			SN74ALS653 SN74ALS654			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_{OH}	High-level output voltage	A ports			5.5			5.5	V
I_{OH}	High-level output current	B ports			−12			−15	mA
I_{OL}	Low-level output current				12			24	mA
								48†	
f_{clock}	Clock frequency								MHz
t_w	Pulse duration	CBA or CAB high							ns
		CBA or CAB low							
t_{su}	Setup time before CAB↑ or CBA↑	A or B							ns
t_h	Hold time after CAB↑ or CBA↑	A or B							ns
T_A	Operating free-air temperature		−55		125	0		70	°C

†The extended condition applies if V_{CC} is maintained between 4.75 V and 5.25 V.
The 48-mA limit applies for the SN74ALS653–1 and SN74ALS654–1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS653 SN54ALS654			SN74ALS653 SN74ALS654			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	B ports	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
I_{OH}	A ports	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.75 V, (I_{OL} = 48 mA for −1 versions)	I_{OL} = 24 mA					0.35	0.5	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	A or B ports§					20			20	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
	A or B ports§					−0.2			−0.2	
I_O¶	B ports	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'ALS653	V_{CC} = 5.5 V	Outputs high		52			52		mA
			Outputs low		57			57		
			Outputs disabled		58			58		
	'ALS654		Outputs high		60			60		
			Outputs low		68			68		
			Outputs disabled		68			68		

‡All typical values are at V_{CC} = 5 V, T_A = 25 °C
§For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
¶The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

'ALS653 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 680 Ω, (A outputs) R1 = R2 = 500 Ω, (B outputs) T_A = MIN to MAX						UNIT
			SN54ALS653			SN74ALS653			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
f_{max}									MHz
t_{PLH}	CBA	A		24			24		ns
t_{PHL}				15			15		
t_{PLH}	CAB	B		11			11		ns
t_{PHL}				13			13		
t_{PLH}	A	B		10			10		ns
t_{PHL}				12			12		
t_{PLH}	B	A		24			24		ns
t_{PHL}				10			10		
t_{PLH}	SBA‡ (with B high)	A		26			26		ns
t_{PHL}				15			15		
t_{PLH}	SBA‡ (with B low)	A		26			26		ns
t_{PHL}				15			15		
t_{PLH}	SAB‡ (with A high)	B		16			16		ns
t_{PHL}				16			16		
t_{PLH}	SAB‡ (with A low)	B		15			15		ns
t_{PHL}				15			15		
t_{PLH}	$\overline{G}$BA	A		24			24		ns
t_{PHL}				17			17		
t_{PZH}	GAB	B		19			19		ns
t_{PZL}				22			22		
t_{PHZ}	GAB	B		12			12		ns
t_{PLZ}				14			14		

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡These parameters are measured with the internal output state of the storage register opposite to that of the bus input.
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

Additional information on these products can be obtained from the factory as it becomes available.

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'ALS654 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 680 Ω, (A outputs) R1 = R2 = 500 Ω, (B outputs) T_A = MIN to MAX						UNIT
			SN54ALS654			SN74ALS654			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
f_{max}									MHz
t_{PLH}	CBA	A		24			24		ns
t_{PHL}				15			15		
t_{PLH}	CAB	B		11			11		ns
t_{PHL}				13			13		
t_{PLH}	A	B		8			8		ns
t_{PHL}				8			8		
t_{PLH}	B	A		24			24		ns
t_{PHL}				10			10		
t_{PLH}	SBA‡ (with B high)	A		26			26		ns
t_{PHL}				15			15		
t_{PLH}	SBA‡ (with B low)	A		26			26		ns
t_{PHL}				15			15		
t_{PLH}	SAB‡ (with A high)	B		16			16		ns
t_{PHL}				16			16		
t_{PLH}	SAB‡ (with A low)	B		15			15		ns
t_{PHL}				12			12		
t_{PLH}	$\overline{G}$BA	A		24			24		ns
t_{PHL}				17			17		
t_{PZH}	GAB	B		19			19		ns
t_{PZL}				22			22		
t_{PHZ}	GAB	B		12			12		ns
t_{PLZ}				14			14		

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡These parameters are measured with the internal output state of the storage register opposite to that of the bus input.
NOTE 1: For load circuit and voltage waveforms, see page 1-12.
Additional information on these products can be obtained from the factory as it becomes available.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: Control inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN54AS651, SN54AS652 . . . . . −55°C to 125°C
SN74AS651, SN74AS652 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54AS651 SN54AS652			SN74AS651 SN74AS652			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−12			−15	mA
I_{OL}	Low-level output current				48			64	mA
f_{clock}			0		75	0		90	MHz
t_w	Pulse duration	CBA or CAB high	6			5			ns
		CBA or CAB low	7			6			
t_{su}	Setup time before CAB↑ or CBA↑	A or B	7			6			ns
t_h	Hold time after CAB↑ or CBA↑	A or B	0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS651 SN54AS652			SN74AS651 SN74AS652			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 48 mA		0.35	0.55				V
		V_{CC} = 4.5 V,	I_{OL} = 64 mA					0.35	0.55	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	A or B ports‡					70			70	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
	A or B ports‡					−0.75			−0.75	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'AS651	V_{CC} = 5.5 V	Outputs high		110	185		110	185	mA
			Outputs low		120	195		120	195	
			Outputs disabled		130	195		130	195	
	'AS652		Outputs high		120	195		120	195	
			Outputs low		130	211		130	211	
			Outputs disabled		130	211		130	211	

†All typical values are at V_{CC} = 5 V, T_A = 25°C
‡For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

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'AS651 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS651		SN74AS651		
			MIN	MAX	MIN	MAX	
f_{max}			75		90		MHz
t_{PLH}	CBA or CAB	A or B	2	9.5	2	8.5	ns
t_{PHL}			2	10	2	9	
t_{PLH}	A or B	B or A	2	9	2	8	ns
t_{PHL}			1	8	1	7	
t_{PLH}	SBA or SAB†	A or B	2	12	2	11	ns
t_{PHL}			2	10	2	9	
t_{PZH}	$\overline{G}$BA	A	2	11	2	10	ns
t_{PZL}			3	18	3	16	
t_{PHZ}	$\overline{G}$BA	A	2	10	2	9	ns
t_{PLZ}			2	10	2	9	
t_{PZH}	GAB	B	3	12	3	11	ns
t_{PZL}			3	20	3	16	
t_{PHZ}	GAB	B	2	11	2	10	ns
t_{PLZ}			2	12	2	11	

'AS652 switching characteristics (see Note 1)

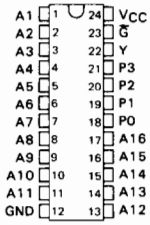
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS652		SN74AS652		
			MIN	MAX	MIN	MAX	
f_{max}			75		90		MHz
t_{PLH}	CBA or CAB	A or B	2	9.5	2	8.5	ns
t_{PHL}			2	10	2	9	
t_{PLH}	A or B	B or A	2	11	2	9	ns
t_{PHL}			1	8	1	7	
t_{PLH}	SBA or SAB†	A or B	2	12	2	11	ns
t_{PHL}			2	10	2	9	
t_{PZH}	$\overline{G}$BA	A	2	11	2	10	ns
t_{PZL}			3	18	3	16	
t_{PHZ}	$\overline{G}$BA	A	2	10	2	9	ns
t_{PHL}			2	10	2	9	
t_{PZH}	GAB	B	3	12	3	11	ns
t_{PZL}			3	20	3	16	
t_{PHZ}	GAB	B	2	11	2	10	ns
t_{PLZ}			2	12	2	11	

† These parameters are measured with the internal output state of the storage register opposite to that of the bus input.
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

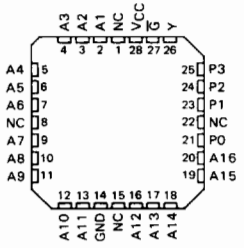
D2661, JUNE 1982–REVISED MARCH 1984

- **'ALS677 is a 16-bit Address Comparator with Enable**
- **'ALS678 is a 16-bit Address Comparator with Latch**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS677 . . . JT PACKAGE
SN74ALS677 . . . NT PACKAGE
(TOP VIEW)



SN54ALS677 . . . FH PACKAGE
SN74ALS677 . . . FN PACKAGE



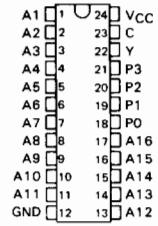
description

The 'ALS677 and 'ALS678 address comparators simplify addressing of memory boards and/or other peripheral devices. The four P inputs are normally hard wired with a preprogrammed address. An internal decoder determines what input information applied to the 16 A inputs must be low or high to cause a low state at the output (Y). For example, a positive-logic bit combination of 0111 (decimal 7) at the P input determines that inputs A1 through A7 must be low and that inputs A8 through A16 must be high to cause the output to go low. Equality of the address applied at the A inputs to the preprogrammed address is indicated by the output being low.

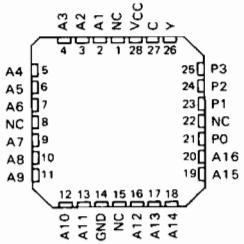
The 'ALS677 features an enable input (G). When G is low, the device is enabled. When G is high, the device is disabled and the output is high regardless of the A and P inputs. The 'ALS678 features a transparent latch and a latch enable input (C). When C is high, the device is in the transparent mode. When C is low, the previous logic state of Y is latched.

The SN54ALS677 and SN54ALS678 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN54ALS677 and SN74ALS678 are characterized for operation from 0°C to 70°C.

SN54ALS678 . . . JT PACKAGE
SN74ALS678 . . . NT PACKAGE
(TOP VIEW)



SN54ALS678 . . . FH PACKAGE
SN74ALS678 . . . FN PACKAGE
(TOP VIEW)



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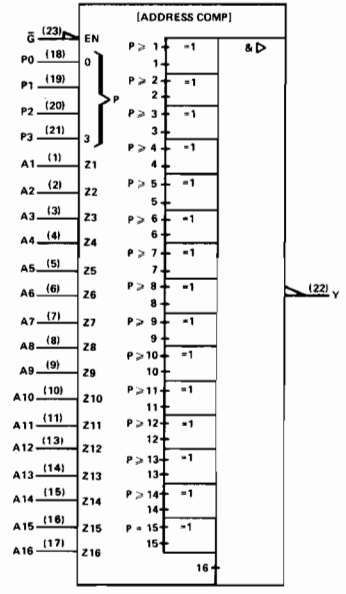
ALS AND AS CIRCUITS

FUNCTION TABLE

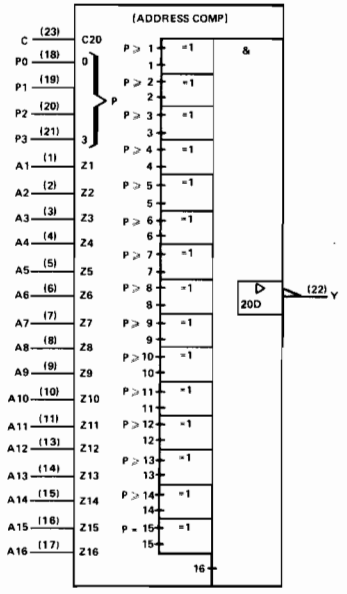
'ALS677	'ALS678	INPUTS COMMON TO 'ALS677 AND 'ALS678																				OUTPUT
$\overline{G}$	C	P3	P2	P1	P0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13	A14	A15	A16	Y
L	H	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	L	L	H	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	L	L	H	H	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	L	H	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	L	H	L	H	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	L
L	H	L	H	H	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	L
L	H	L	H	H	H	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	L
L	H	H	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	L
L	H	H	L	L	H	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	L
L	H	H	L	H	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	L
L	H	H	L	H	H	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	L
L	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	L
L	H	H	H	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	L
L	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	L
L	H	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L
L	H	All other combinations																				H
H		'ALS677: Any combination																				H
	L	'ALS678: Any combination																				Latched

logic symbols

'ALS677



'ALS678

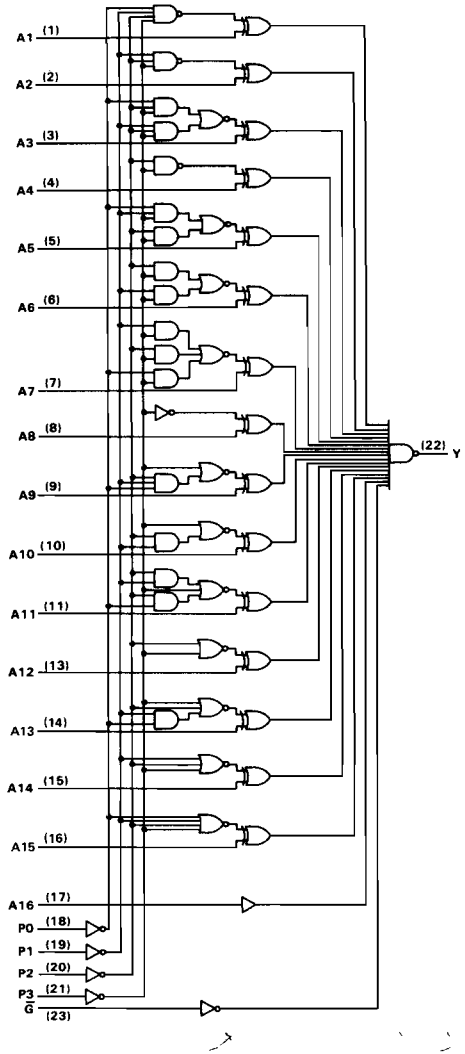


Pin numbers shown are for JT and NT packages.

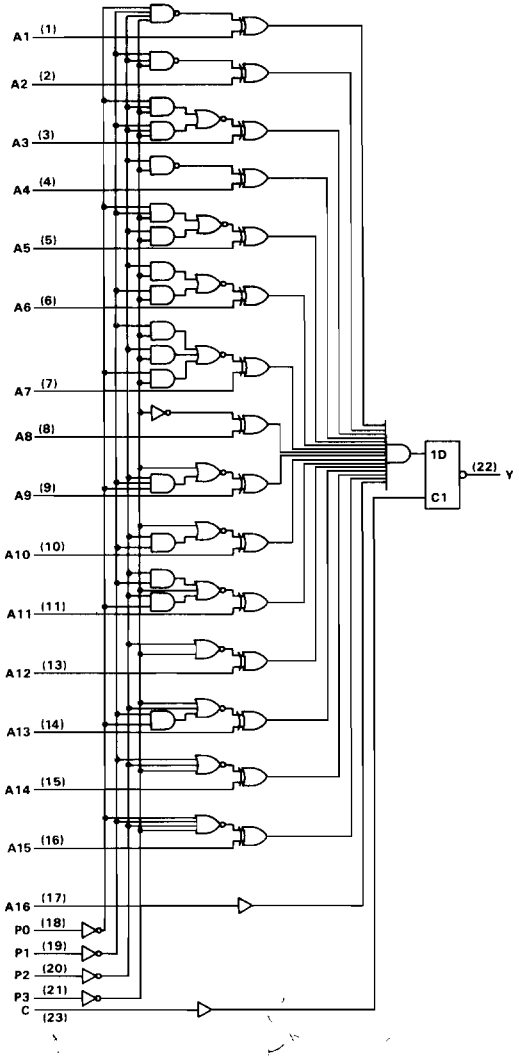
TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

logic diagrams (positive logic)

'ALS677



'ALS678



Pin numbers shown are for JT and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS677, SN54ALS678 . . . . . −55°C to 125°C
SN74ALS677, SN74ALS678 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS677 SN54ALS678			SN74ALS677 SN74ALS678			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−1			−2.6	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS677 SN54ALS678			SN74ALS677 SN74ALS678			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
		V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'ALS677	V_{CC} = 5.5 V			21	33		21	33	mA
	'ALS678				21	35		21	35	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

'ALS677 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS677		SN74ALS677		
			MIN	MAX	MIN	MAX	
t_{PLH}	Any P	Y	4	28	4	25	ns
t_{PHL}			8	40	8	35	
t_{PLH}	Any A	Y	5	26	5	22	ns
t_{PHL}			5	40	5	35	
t_{PLH}	$\overline{G}$	Y	3	15	3	13	ns
t_{PHL}			5	30	5	25	

'ALS678 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS678		SN74ALS678		
			MIN	MAX	MIN	MAX	
t_{PLH}	Any P	Y	6	27	6	22	ns
t_{PHL}			10	52	10	43	
t_{PLH}	Any A	Y	5	25	5	21	ns
t_{PHL}			5	40	5	35	
t_{PLH}	C	Y	3	25	3	20	ns
t_{PHL}			15	54	15	48	

NOTE 1: For load circuit and voltage waveforms, see page 1-12 of the TTL Data Book, Volume 3.

TYPICAL APPLICATION INFORMATION

The 'ALS677 and 'ALS678 can be wired to recognize any one of $2^{16} - 1$ addresses. The number of "lows" in the address determines the input pattern for the P inputs. Then those system address lines that are low in the address to be recognized are connected to the lowest numbered A inputs of the address comparator and the system address lines that are high are connected to the highest numbered A inputs.

For example, assume the comparator is to enable a device when the 16-bit system address is:

A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
H	H	L	L	H	H	L	L	H	H	L	L	H	H	H	H

Since the address contains 6 lows and 10 highs, the following connections are made:

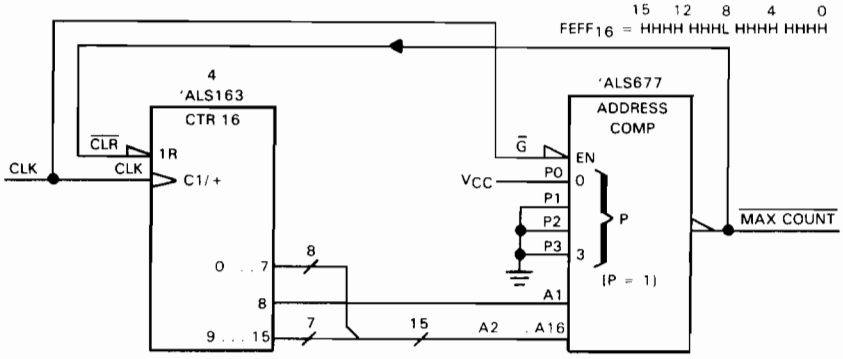
P3 to 0 V, P2 to V_{CC}, P1 to V_{CC}, and P0 to 0 V.

System address lines A13, A12, A9, A8, A5, and A4 to comparator inputs A1 through A6 in any convenient order.

The remaining ten system address lines to comparator inputs A7 through A16 in any convenient order.

The output provides an active-low enabling signal.

The following circuit is a modulo-N synchronous counter. The 'ALS163 is connected to provide a low-level clear signal when $N = FEFF_{16}$.



MODULO-N SYNCHRONOUS COUNTER

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

D2661, JUNE 1982–REVISED MARCH 1984

- **'ALS679 is a 12-Bit Address Comparator With Enable**
- **'ALS680 is a 12-Bit Address Comparator With Latch**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

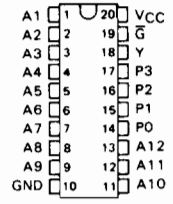
description

The 'ALS679 and 'ALS680 address comparators simplify addressing of memory boards and/or other peripheral devices. The four P inputs are normally hard wired with a preprogrammed address. An internal decoder determines what input information applied to the 12 A inputs must be low or high to cause a low state at the output (Y). For example, a positive-logic bit combination of 0111 (decimal 7) at the P input determines that inputs A1 through A7 must be low and that inputs A8 through A12 must be high to cause the output to go low. Equality of the address applied at the A inputs to the preprogrammed address is indicated by the output being low.

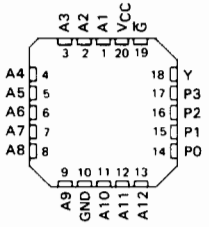
The 'ALS679 features an enable input ($\overline{G}$). When $\overline{G}$ is low, the device is enabled. When $\overline{G}$ is high, the device is disabled and the output is high regardless of the A and P inputs. The 'ALS680 features a transparent latch and a latch enable input (C). When C is high, the device is in the transparent mode. When C is low, the previous logical state of Y is latched.

The SN54ALS679 and SN54ALS680 are characterized for operation over the full military temperature of −55°C to 125°C. The SN74ALS679 and SN74ALS680 are characterized for operation from 0°C to 70°C.

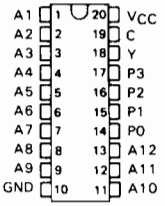
SN54ALS679 . . . J PACKAGE
SN74ALS679 . . . N PACKAGE
(TOP VIEW)



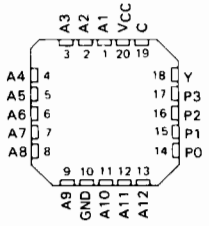
SN54ALS679 . . . FH PACKAGE
SN74ALS679 . . . FN PACKAGE
(TOP VIEW)



SN54ALS680 . . . J PACKAGE
SN74ALS680 . . . N PACKAGE
(TOP VIEW)



SN54ALS680 . . . FH PACKAGE
SN74ALS680 . . . FN PACKAGE
(TOP VIEW)

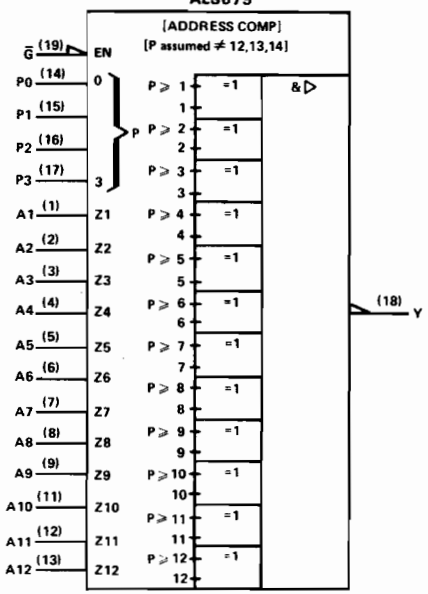


FUNCTION TABLE

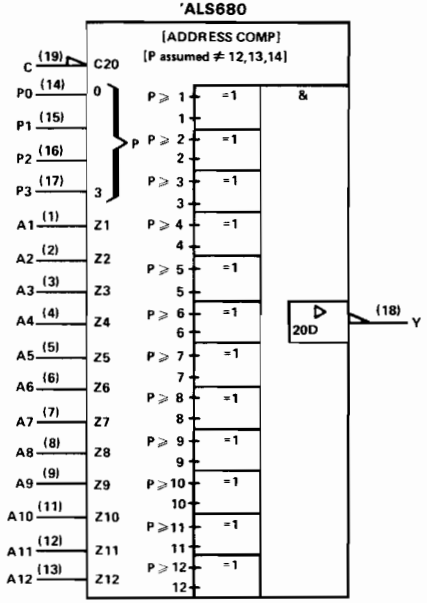
'ALS679	'ALS680	INPUTS COMMON TO 'ALS679 AND 'ALS680																OUTPUT
$\overline{G}$	C	P3	P2	P1	P0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	Y
L	H	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	L
L	H	L	L	H	L	L	L	H	H	H	H	H	H	H	H	H	H	L
L	H	L	L	H	H	L	L	L	H	H	H	H	H	H	H	H	H	L
L	H	L	H	L	L	L	L	L	L	H	H	H	H	H	H	H	H	L
L	H	L	H	L	H	L	L	L	L	L	H	H	H	H	H	H	H	L
L	H	L	H	H	L	L	L	L	L	L	L	H	H	H	H	H	H	L
L	H	L	H	H	H	L	L	L	L	L	L	L	H	H	H	H	H	L
L	H	H	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	L
L	H	H	L	L	H	L	L	L	L	L	L	L	L	L	H	H	H	L
L	H	H	L	H	L	L	L	L	L	L	L	L	L	L	L	H	H	L
L	H	H	L	H	H	L	L	L	L	L	L	L	L	L	L	L	H	L
L	H	H	H	L	L	L	L	L	L	L	L	L	L	H	H	H	L	L*
L	H	H	H	L	H	L	L	L	L	L	L	L	L	L	H	H	L	L*
L	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	H	L	L*
L	H	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L
L	H	All other combinations																H
H		'ALS679: Any combination																H
	L	'ALS680: Any combination																Latched

logic symbols

'ALS679



'ALS680



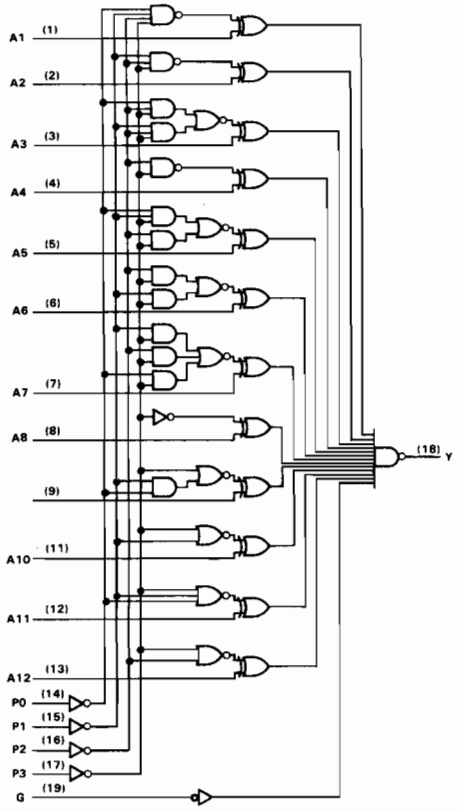
*The three shaded rows of the function table show combinations that would normally not be used in address comparator applications. The logic symbols above are not valid for these combinations in which P = 12, 13, and 14. If symbols valid for all combinations are required, starting with the fourth Exclusive-OR from the bottom, change P ≥ 9 to P = 9...11/13...15, P ≥ 10 to P = 10/11/14/15, and P ≥ 11 to P = 11/15.

Pin numbers shown are for J and N packages.

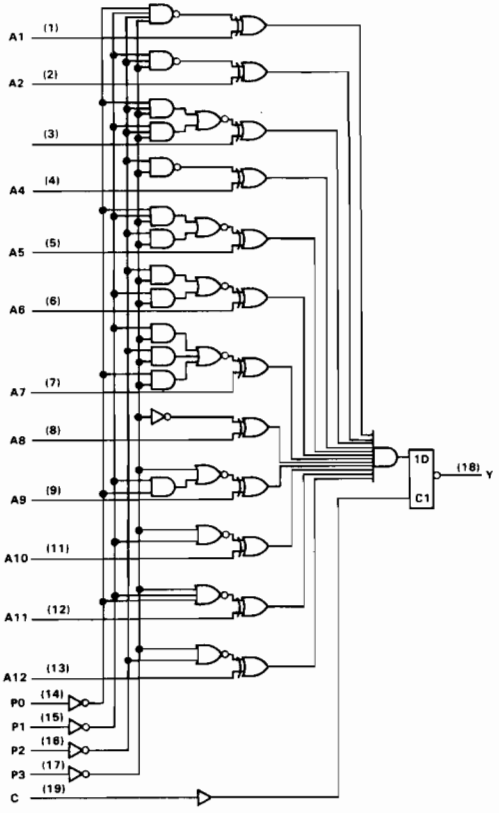
TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

logic diagrams (positive logic)

'ALS680



'ALS679



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS679, SN54ALS680 . . . . . −55°C to 125°C
SN74ALS679, SN74ALS680 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS679 SN54ALS680			SN74ALS679 SN74ALS680			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−1			−2.6	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS679 SN54ALS680			SN74ALS679 SN74ALS680			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC} − 2			V_{CC} − 2			V
		V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
		V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'ALS679	V_{CC} = 5.5 V			17	28		17	28	mA
	'ALS680				18	27		18	27	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

'ALS679 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS679		SN74ALS679		
			MIN	MAX	MIN	MAX	
t_{PLH}	Any P	Y	4	28	4	25	ns
t_{PHL}			8	40	8	35	
t_{PLH}	Any A	Y	5	26	5	22	ns
t_{PHL}			5	35	5	30	
t_{PLH}	$\overline{G}$	Y	3	15	3	13	ns
t_{PHL}			5	30	5	25	

'ALS680 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS680		SN74ALS680		
			MIN	MAX	MIN	MAX	
t_{PLH}	Any P	Y	6	27	6	22	ns
t_{PHL}			10	43	10	38	ns
t_{PLH}	Any A	Y	5	25	5	21	ns
t_{PHL}			5	28	5	25	
t_{PLH}	C	Y	3	25	3	20	ns
t_{PHL}			15	48	15	42	

NOTE 1: For load circuit and voltage waveforms, see page 1-12 of the TTL Data Book, Volume 3.

TYPICAL APPLICATION INFORMATION

The 'ALS679 and 'ALS680 can be wired to recognize any one of 2^{12} addresses. The number of "lows" in the address determines the input pattern for the P inputs. Then those system address lines that are low in the address to be recognized are connected to the lowest numbered A inputs of the address comparator and the system address lines that are high are connected to the highest numbered A inputs.

For example, assume the comparator is to enable a device when the 12-bit system address is:

A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
H	H	L	L	H	H	L	L	H	H	H	H

Since the address contains 4 lows and 8 highs, the following connections are made:

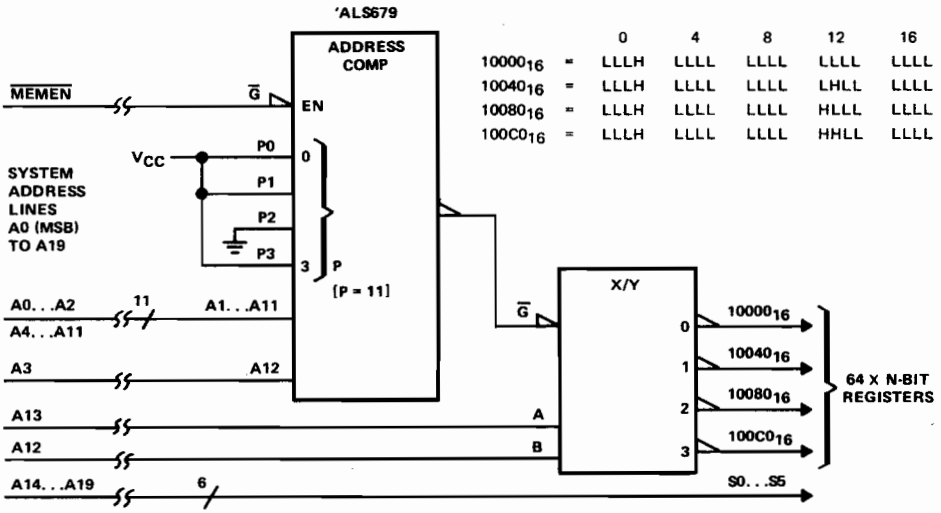
P3 to 0 V, P2 to V_{CC}, P1 to 0 V, and P0 to 0 V.

System address lines A9, A8, A5, and A4 to comparator inputs A1 through A4 in any convenient order.

The remaining eight system address lines to comparator inputs A5 through A12 in any convenient order.

The output provides an active-low enabling signal.

The following circuit is a register bank decoder that examines the 14 most significant bits (A0 through A13) of a 20-bit address to select banks corresponding to the hex addresses 10000, 10040, 10080, and 100C0.



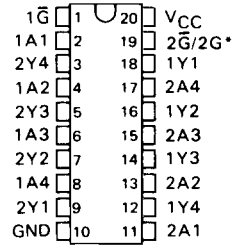
REGISTER BANK DECODER

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

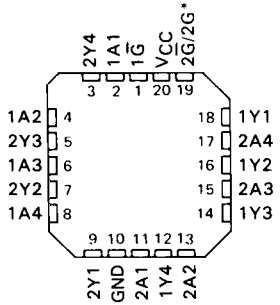
D2261, DECEMBER 1983 – REVISED FEBRUARY 1984

- **Open-Collector Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **Eliminates the Need for 3-State Overlap Protection**
- **P-N-P Inputs Reduce DC Loading**
- **Dependable Texas Instruments Quality and Reliability**
- **Open-Collector Versions of 'AS240, 'AS241**

SN54AS' . . . J PACKAGE
SN74AS' . . . N PACKAGE
(TOP VIEW)



SN54AS' . . . FH PACKAGE
SN74AS' . . . FN PACKAGE
(TOP VIEW)



*2G̅ for 'AS756 or 2G for 'AS757

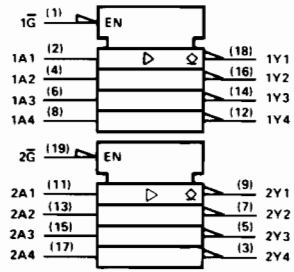
description

These octal bus transceivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters by eliminating the need for three-state overlap protection. The designer has a choice of selected combinations of inverting and noninverting outputs, symmetrical $\overline{G}$ (active-low output control) inputs, and complementary G and $\overline{G}$ inputs. These devices feature high fan-out and improved fan-in.

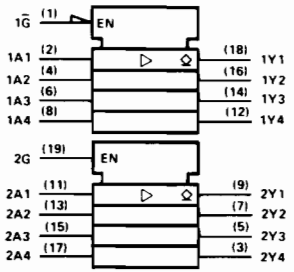
The SN54' family is characterized for operation over the full military temperature range of −55 °C to 125 °C. The SN74' family is characterized for operation from 0 °C to 70 °C.

logic symbols

'AS756

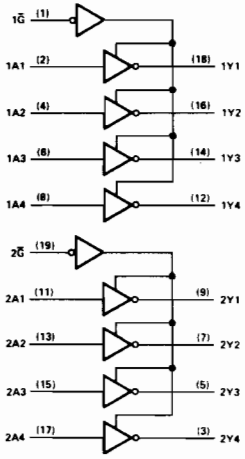


'AS757

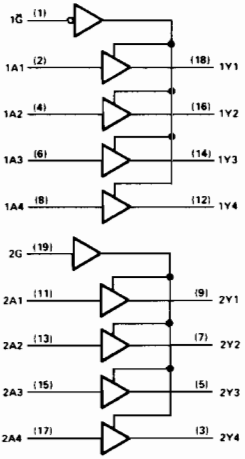


logic diagrams (positive logic)

'AS756



'AS757



Pin numbers shown are for J and N packages.

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 7 V
Operating free-air temperature range: SN54AS756, SN54AS757 . . . . . −55°C to 125°C
SN74AS756, SN74AS757 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS756 SN54AS757			SN74AS756 SN74AS757			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			48			64	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS756 SN54AS757			SN74AS756 SN74AS757			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
I_{OH}		V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 48 mA			0.55				V
		V_{CC} = 4.5 V,	I_{OL} = 64 mA						0.55	
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	'AS757 A inputs only	V_{CC} = 5.5 V,	V_I = 0.4 V			−1			−1	mA
	All other					−0.5			−0.5	
I_{CC}	'AS756	V_{CC} = 5.5 V	Output high		9	15		9	15	mA
			Output low		51	80		51	80	
	'AS757		Output high		21	33		21	33	
			Output low		61	95		61	95	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

'AS756 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS756		SN74AS756		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	3	20	3	19	ns
t_{PHL}			1	7	1	6	
t_{PLH}	$\overline{G}$	Y	3	22	3	19.5	ns
t_{PHL}			1	8.5	1	7.5	

'AS757 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS757		SN74AS757		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	3	19.5	3	18.5	ns
t_{PHL}			1	7	1	6	
t_{PLH}	$1\overline{G}$	Y	3	21	3	20	ns
t_{PHL}			1	8	1	7	
t_{PLH}	2G	Y	3	22.5	3	21	ns
t_{PHL}			1	8.5	1	7.5	

NOTE 1: For load circuit and voltage waveforms, see page 1-12 of the TTL Data Book, Volume 3.

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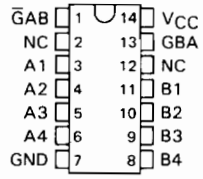
- **2-Way Asynchronous Communication Between Data Buses**
- **P-N-P Inputs Reduce Loading**
- **Dependable Texas Instruments Quality and Reliability**
- **Open-Collector Versions of 'AS242, 'AS243**

description

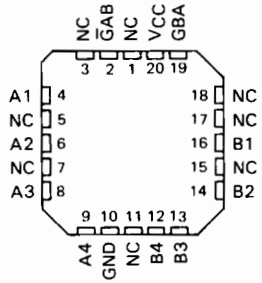
These four-data-line transceivers are designed for asynchronous two-way communications between data buses.

The SN54' family is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74' family is characterized for operation from 0°C to 70°C.

SN54' . . . J PACKAGE
SN74' . . . N PACKAGE
(TOP VIEW)

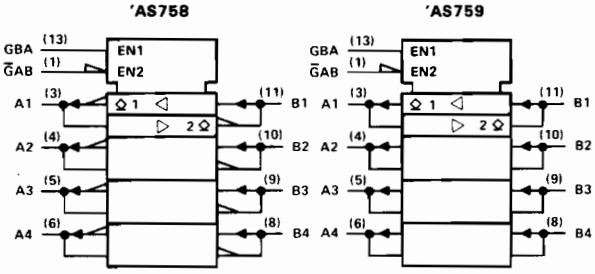


SN54' . . . FH PACKAGE
SN74' . . . FN PACKAGE
(TOP VIEW)

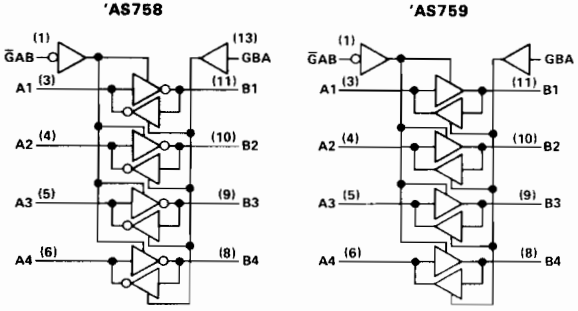


NC – No internal connection

logic symbol



logic diagrams (positive logic)



Pin numbers shown are for J and N packages.

FUNCTION TABLE

INPUTS		'AS758	'AS759
GAB	GBA		
L	L	A to B	A to B
H	H	B to A	B to A
H	L	Isolation	Isolation
L	H	Latch A and B (A = B)	Latch A and B (A = B)

2

ALS AND AS CIRCUITS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs and I/O ports . . . . . 7 V
Operating free-air temperature range: SN54AS758, SN54AS759 . . . . . −55°C to 125°C
SN74AS758, SN74AS759 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS758 SN54AS759			SN74AS758 SN74AS759			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			48			64	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS758 SN54AS759			SN74AS758 SN74AS759			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
I_{OH}		V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 48 mA			0.55				V
		V_{CC} = 4.5 V,	I_{OL} = 64 mA						0.55	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	A or B ports	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	A or B ports					50			50	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
	'AS758 A or B ports‡					−0.5			−0.5	
	'AS759 A or B ports‡					−1			−1	
I_{CC}	'AS758	V_{CC} = 5.5 V	Outputs high		17	27		17	27	mA
			Outputs low		38	60		38	60	
	'AS759		Outputs high		27	43		27	43	
			Outputs low		47	74		47	74	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

'AS758 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS758		SN74AS758		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	3	20.5	3	19.5	ns
t_{PHL}			1	7	1	6	
t_{PLH}	GBA	A	3	22	3	19.5	ns
t_{PHL}			1	8.5	1	7.5	
t_{PLH}	$\overline{G}$AB	B	3	22	3	21	ns
t_{PHL}			1	8.5	1	8	

'AS759 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS759		SN74AS759		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	3	21	3	20	ns
t_{PHL}			1	7	1	6	
t_{PLH}	GBA	A	3	21	3	20	ns
t_{PHL}			1	8	1	7	
t_{PLH}	$\overline{G}$AB	B	3	22.5	3	21	ns
t_{PHL}			1	8.5	1	7.5	

NOTE 1: For load circuit and voltage waveforms, see page 1-12 of the TTL Data Book, Volume 3.

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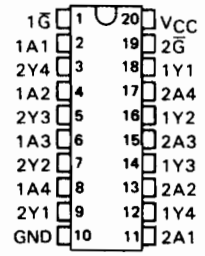
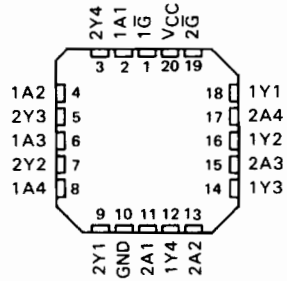
- **Open-Collector Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **Eliminates the Need For 3-State Overlap Protection**
- **P-N-P Inputs Reduce DC Loading**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**
- **Open-Collector Version of 'AS244**

SN54AS760 . . . J PACKAGE
SN74AS760 . . . N PACKAGE
(TOP VIEW)



SN54AS760 . . . FH PACKAGE
SN74AS760 . . . FN PACKAGE
(TOP VIEW)

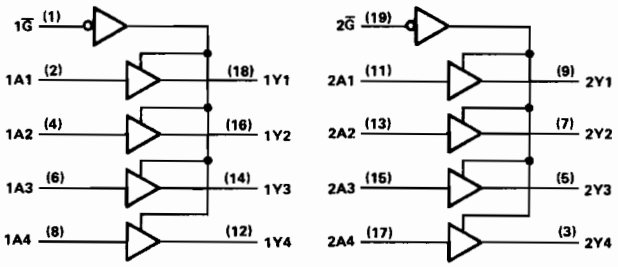


description

These octal buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters by eliminating the need for 3-state overlap protection. Taken together with the 'AS756 and 'AS757, these devices provide the choice of selected combinations of inverting outputs, symmetrical $\overline{G}$ (active-low input control) inputs, and complementary G and $\overline{G}$ inputs.

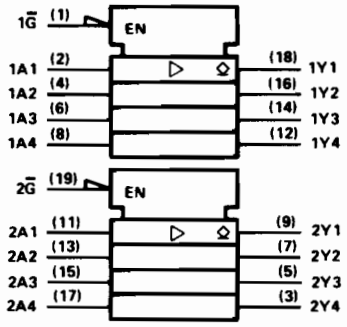
The SN54AS760 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74AS760 is characterized for operation from 0°C to 70°C.

functional block diagram (positive logic)



Pin numbers shown are for J and N packages

logic symbol



2

ALS AND AS CIRCUITS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 7 V
Operating free-air temperature range: SN54AS760 . . . . . −55 °C to 125 °C
SN74AS760 . . . . . 0 °C to 70 °C
Storage temperature range . . . . . −65 °C to 150 °C

recommended operating conditions

		SN54AS760			SN74AS760			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			48			64	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS760			SN74AS760			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
I_{OH}		V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 48 mA			0.55				V
		V_{CC} = 4.5 V,	I_{OL} = 64 mA						0.55	
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	$\overline{G}$	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
	A					−1			−1	
I_{CC}		V_{CC} = 5.5 V	Outputs high		20	32		20	32	mA
			Outputs low		60	94		60	94	

'AS760 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS760		SN74AS760		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	3	19.5	3	18.5	ns
t_{PHL}			1	7	1	6	
t_{PLH}	$\overline{G}$	Y	3	19.5	3	18.5	ns
t_{PHL}			1	8	1	7	

NOTE 1: For load circuit and voltage waveforms, see page 1-12 of the TTL Data Book, Volume 3.

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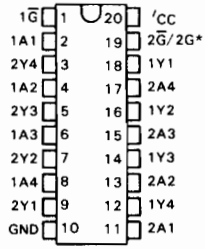
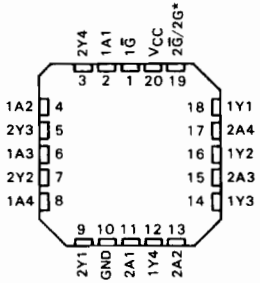
- **Included Among the Package Options Are 20-Pin DIPs and Both Plastic and Ceramic Chip Carriers**
- **'AS762 Has True and Complementary Outputs**
- **'AS763 Has Complementary G and $\overline{G}$ Inputs**
- **Open-Collector Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **Eliminates the Need for 3-State Overlap Protection**
- **Current Sinking Capability Up to 64 mA**
- **Dependable Texas Instruments Quality and Reliability**

SN54AS' . . . J PACKAGE
SN74AS' . . . N PACKAGE
(TOP VIEW)



SN54AS' . . . FH PACKAGE
SN74AS' . . . FN PACKAGE
(TOP VIEW)



*$2\overline{G}$ for 'AS762 or 2G for 'AS763

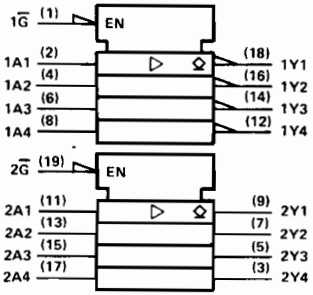
description

These octal buffers and line drivers are designed specifically to improve the performance of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters by eliminating the need for 3-state overlap protection. The designer has a choice of selected combinations of inverting and noninverting outputs, symmetrical $\overline{G}$ (active-low output control) inputs, and complementary G and $\overline{G}$ inputs.

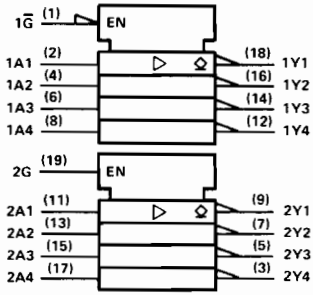
The SN54AS762 and SN54AS763 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74AS762 and SN74AS763 are characterized for operation from 0°C to 70°C.

logic symbols

'AS762



'AS763



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 7 V
Operating free-air temperature range: SN54AS762, SN54AS763 . . . . . −55°C to 125°C
SN74AS762, SN74AS763 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54AS762 SN54AS763			SN74AS762 SN74AS763			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			48			64	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS762 SN54AS763			SN74AS762 SN74AS763			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
I_{OH}		V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 48 mA			0.55				V
		V_{CC} = 4.5 V,	I_{OL} = 64 mA						0.55	
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	'AS762 2A inputs only	V_{CC} = 5.5 V,	V_I = 0.4 V			−1			−1	mA
	All other					−0.5			−0.5	
I_{CC}	'AS762	V_{CC} = 5.5 V	Output high		15	23		15	23	mA
			Output low		55	87		55	87	
	'AS763	V_{CC} = 5.5 V	Output high		10	16		10	16	
			Output low		52	82		52	82	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

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'AS762 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS762		SN74AS762		
			MIN	MAX	MIN	MAX	
t_{PLH}	1A	1Y	3	20	3	19	ns
t_{PHL}			1	7	1	6	
t_{PLH}	2A	2Y	3	19.5	3	18.5	ns
t_{PHL}			1	7	1	6	
t_{PLH}	$\overline{G}$	1Y	3	22	3	19.5	ns
t_{PHL}			1	8	1	7.5	
t_{PLH}	$\overline{G}$	2Y	3	20	3	19	ns
t_{PHL}			1	8	1	7	

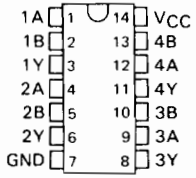
'AS763 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS763		SN74AS763		
			MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	3	20	3	19	ns
t_{PHL}			1	7	1	6	
t_{PLH}	$\overline{G}$	Y	3	22	3	19.5	ns
t_{PHL}			1	8.5	1	7.5	
t_{PLH}	G	Y	3	22	3	20	ns
t_{PHL}			1	8.5	1	8	

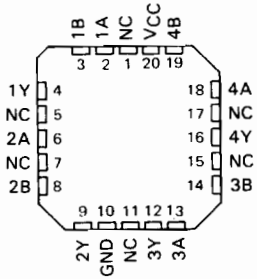
NOTE 1: For load circuit and voltage waveforms, see page 1-12 of the TTL Data Book, Volume 3.

- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS810 . . . J PACKAGE
SN74ALS810 . . . N PACKAGE
(TOP VIEW)



SN54ALS810 . . . FH PACKAGE
SN74ALS810 . . . FN PACKAGE
(TOP VIEW)



NC – No internal connection

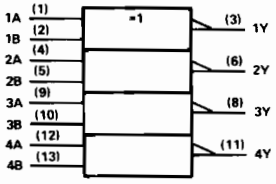
description

These devices contain four independent Exclusive-NOR gates. They perform the Boolean functions $Y = \overline{A \oplus B} = (A+\overline{B})\cdot(\overline{A}+B)$ in positive logic.

A common application is a true/complement element. If one of the inputs is high, the other input will be reproduced in true form at the output. If one of the inputs is low, the signal on the other input will be reproduced inverted at the output.

The SN54ALS810 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS810 is characterized for operation from 0°C to 70°C.

logic symbol



Pin numbers shown are for J and N packages.

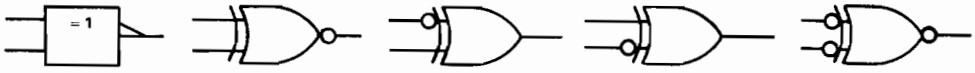
FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	H

exclusive-NOR logic

An exclusive-NOR gate has many applications, some of which can be represented better by alternative logic symbols.

EXCLUSIVE-NOR

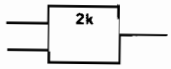


These are five equivalent Exclusive-NOR symbols valid for an 'ALS810 gate in positive logic; negation may be shown at any one port, or at all three of them.

LOGIC IDENTITY ELEMENT

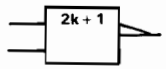
The output is active (High) if all inputs stand at the same logic level (i.e., A = B).

EVEN-PARITY



The output is active (High) if an even number of inputs (i.e., 0 or 2) are active.

ODD-PARITY ELEMENT



The output is active (Low) if an odd number of inputs (i.e., only 1 of the 2) are active.

PRODUCT PREVIEW
This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS810 . . . . . −55°C to 125°C
SN74ALS810 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS810			SN74ALS810			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−0.4			−0.4	mA
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS810			SN74ALS810			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC} − 2			V_{CC} − 2			V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = 5.5 V,	A at 4.5 V, B at 0 V		5	7.5		5	7.5	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS810		SN74ALS810		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	5	23	5	20	ns
t_{PHL}	(other input low)		3	17	3	14	
t_{PLH}	A or B	Y	5	21	5	18	ns
t_{PHL}	(other input high)		3	17	3	14	

NOTE 1: For load circuit and voltage waveforms, see page 1-12 of the TTL Data Book, Volume 3.

TEXAS INSTRUMENTS
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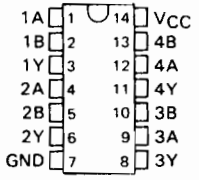
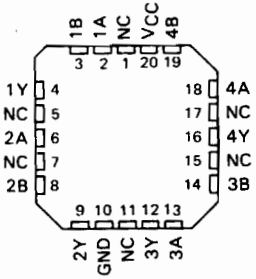
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS811 . . . J PACKAGE
SN74ALS811 . . . N PACKAGE
(TOP VIEW)



SN54ALS811 . . . FH PACKAGE
SN74ALS811 . . . FN PACKAGE
(TOP VIEW)



NC – No internal connection

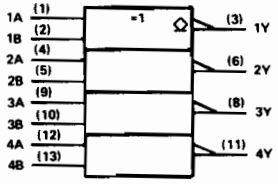
description

These devices contain four independent Exclusive-NOR gates with open-collector outputs. They perform the Boolean functions $Y = A \oplus B = (A + \overline{B}) \cdot (\overline{A} + B)$ in positive logic.

A common application is a true/complement element. If one of the inputs is high, the other input will be reproduced in true form at the output. If one of the inputs is low, the signal on the other input will be reproduced inverted at the output.

The SN54ALS811 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS811 is characterized for operation from 0°C to 70°C.

logic symbol



Pin numbers shown are for J and N packages.

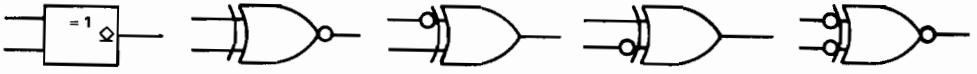
FUNCTION TABLE
(each gate)

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	H

exclusive-NOR logic

An exclusive-NOR gate has many applications, some of which can be represented better by alternative logic symbols.

EXCLUSIVE-NOR

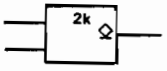


These are five equivalent Exclusive-NOR symbols valid for an 'ALS811 gate in positive logic; negation may be shown at any one port, or at all three of them.

LOGIC IDENTITY ELEMENT

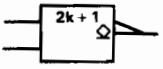
The output is active (high) if all inputs stand at the same logic level (i.e., A = B).

EVEN-PARITY



The output is active (high) if an even number of inputs (i.e., 0 or 2) are active.

ODD-PARITY ELEMENT



The output is active (low) if an odd number of inputs (i.e., only 1 of the 2) are active.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 7 V
Operating free-air temperature range: SN54ALS811 . . . . . −55°C to 125°C
SN74ALS811 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS811			SN74ALS811			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			4			8	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS811			SN74ALS811			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
I_{OH}	V_{CC} = 4.5 V,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
	V_{CC} = 4.5 V,	I_{OL} = 8 mA					0.35	0.5	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_{CC}	V_{CC} = 5.5 V,	A at 4.5 V, B at 0 V		5	7.5		5	7.5	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 2 kΩ, T_A = MIN to MAX				UNIT
			SN54ALS811		SN74ALS811		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	Y	25	60	25	55	ns
t_{PHL}	(other input low)		5	30	5	28	
t_{PLH}	A or B	Y	20	55	20	50	ns
t_{PHL}	(other input high)		5	28	5	23	

NOTE 1: For load circuit and voltage waveforms, see page 1-12 of The TTL Data Book, Volume 3.

TEXAS INSTRUMENTS
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- **3-State Buffer-Type Outputs Drive Bus-Lines Directly**
- **Bus-Structured Pinout**
- **Provide Extra Bus Driving Latches Necessary for Wider Address/Data Paths or Buses with Parity**
- **Buffered Control Inputs to Reduce DC Loading**
- **Power-Up High-Impedance State**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

description

These 10-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

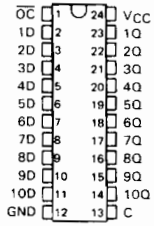
The ten latches are transparent D-type. The 'ALS841 and 'AS841 have noninverting data (D) inputs. The 'ALS842 and 'AS842 have inverting $\overline{D}$ inputs.

A buffered output control ($\overline{OC}$) input can be used to place the ten outputs in either a normal logic state (high or low levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

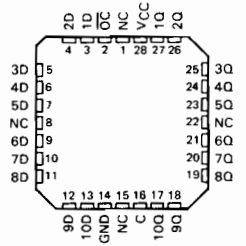
The output control does not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are off.

The SN54ALS841, SN54AS841, SN54ALS842, and SN54AS842 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS841, SN74AS841, SN74ALS842, and SN74AS842 are characterized for operation from 0°C to 70°C.

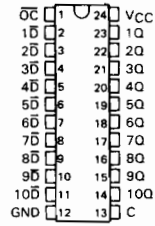
SN54ALS841, SN54AS841 . . . JT PACKAGE
SN74ALS841, SN74AS841 . . . NT PACKAGE
(TOP VIEW)



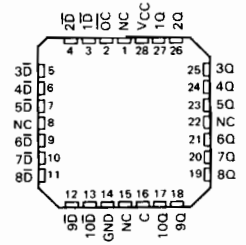
SN54ALS841, SN54AS841 . . . FH PACKAGE
SN74ALS841, SN74AS841 . . . FN PACKAGE
(TOP VIEW)



SN54ALS842, SN54AS842 . . . JT PACKAGE
SN74ALS842, SN74AS842 . . . NT PACKAGE
(TOP VIEW)



SN54ALS842, SN54AS842 . . . FH PACKAGE
SN74ALS842, SN74AS842 . . . FN PACKAGE
(TOP VIEW)



NC – No internal connection

FUNCTION TABLES

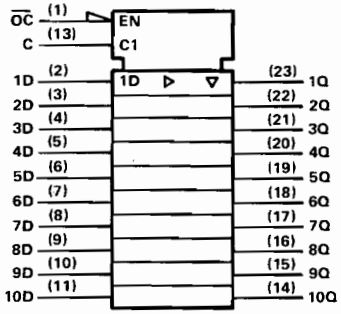
'ALS841, 'AS841

INPUTS			OUTPUT
$\overline{OC}$	C	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

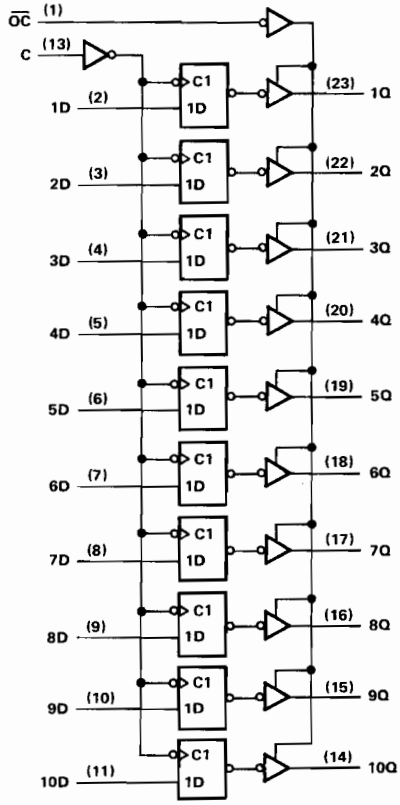
'ALS842, 'AS842

INPUTS			OUTPUT
$\overline{OC}$	C	$\overline{D}$	Q
L	H	H	L
L	H	L	H
L	L	X	Q_0
H	X	X	Z

'ALS841, 'AS841 logic symbol



'ALS841, 'AS841 logic diagram (positive logic)



Pin numbers shown are for JT and NT packages.

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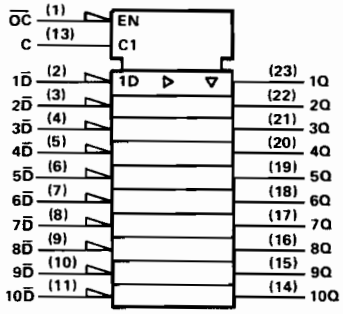
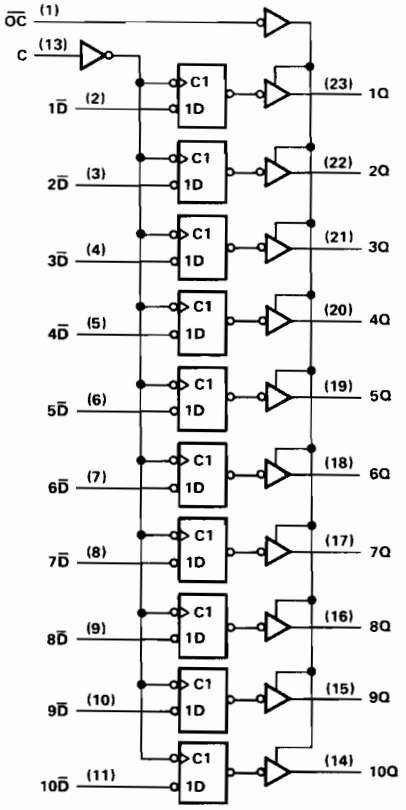
'ALS842, 'AS842 logic symbol



'ALS842, 'AS842 logic diagram (positive logic)



Pin numbers shown are for JT and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range:
SN54ALS841, SN54AS841, SN54ALS842, SN54AS842 . . . . . −55°C to 125°C
SN74ALS841, SN74AS841, SN74ALS842, SN74AS842 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS841 SN54ALS842			SN74ALS841 SN74ALS842			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−1			−2.6	mA
I_{OL}	Low-level output current				12			24	mA
t_w	Pulse duration, enable C high	'ALS841							ns
		'ALS842							
t_{su}	Setup time, data before enable C↓								ns
t_h	Hold time, data after enable C↓	'ALS841							ns
		'ALS842							
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS841 SN54ALS842			SN74ALS841 SN74ALS842			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
		V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−15		−70	−15		−70	mA
I_{CC}	'ALS841	V_{CC} = 5.5 V	Outputs high							mA
			Outputs low							
			Outputs disabled		25			25		
	'ALS842		Outputs high							
			Outputs low							
			Outputs disabled		28			28		

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

Additional information on these products can be obtained from the factory as it becomes available.

TEXAS INSTRUMENTS
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'ALS841 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS841			SN74ALS841			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	D	Q		7			7		ns
t_{PHL}				9			9		
t_{PLH}	C	Q							ns
t_{PHL}									
t_{PZH}	$\overline{OC}$	Q							ns
t_{PZL}									
t_{PHZ}	$\overline{OC}$	Q							ns
t_{PLZ}									

'ALS842 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS842			SN74ALS842			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	$\overline{D}$	Q		11			11		ns
t_{PHL}				9			9		
t_{PLH}	C	Q							ns
t_{PHL}									
t_{PZH}	$\overline{OC}$	Q							ns
t_{PZL}									
t_{PHZ}	$\overline{OC}$	Q							ns
t_{PLZ}									

†All typical values are at T_A = 25°C.
NOTE 1: For load circuit and voltage waveforms, see page 1-12 of the TTL Data Book, Volume 3.

Additional information on these products can be obtained from the factory as it becomes available.

recommended operating conditions

		SN54AS841 SN54AS842			SN74AS841 SN74AS842			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−24			−24	mA
I_{OL}	Low-level output current			32			48	mA
t_w	Pulse duration, enable C high	5			4			ns
t_{su}	Setup time, data before enable C↓	3.5			2.5			ns
t_h	Hold time, data after enable C↓	3.5			2.5			ns
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS841 SN54AS842			SN74AS841 SN74AS842			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −15 mA	2.4	3.2		2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −24 mA	2			2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.25	0.5				V
		V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−50			−50	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'AS841	V_{CC} = 5.5 V	Outputs high		36	60		36	60	mA
			Outputs low		58	94		58	94	
			Outputs disabled		56	92		56	92	
	'AS842		Outputs high		38	62		38	62	
			Outputs low		60	97		60	97	
			Outputs disabled		58	95		58	95	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

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'AS841 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS841		SN74AS841		
			MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	1	8.5	1	6.5	ns
t_{PHL}			1	10	1	9	
t_{PLH}	C	Q	2	13	2	12	ns
t_{PHL}			2	13	2	12	
t_{PZH}	$\overline{OC}$	Q	2	13.5	2	10.5	ns
t_{PZL}			2	14.5	2	11.5	
t_{PHZ}	$\overline{OC}$	Q	1	10	1	8	ns
t_{PLZ}			1	10	1	8	

'AS842 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS842		SN74AS842		
			MIN	MAX	MIN	MAX	
t_{PLH}	$\overline{D}$	Q	1	11	1	8.5	ns
t_{PHL}			1	10	1	9	
t_{PLH}	C	Q	2	13	2	12	ns
t_{PHL}			2	13	2	12	
t_{PZH}	$\overline{OC}$	Q	2	14.5	2	12	ns
t_{PZL}			2	15	2	12.5	
t_{PHZ}	$\overline{OC}$	Q	1	10	1	8	ns
t_{PLZ}			1	10	1	8	

NOTE 1: For load circuits and voltage waveforms, see page 1-12 of the TTL Data Book, Volume 3.

DECEMBER 1983—REVISED FEBRUARY 1984

- **3-State Buffer-Type Outputs Drive Bus-Lines Directly**
- **Bus-Structured Pinout**
- **Provide Extra Bus Driving Latches Necessary for Wider Address/Data Paths or Buses with Parity**
- **Buffered Control Inputs to Reduce DC Loading**
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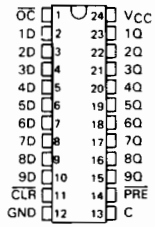
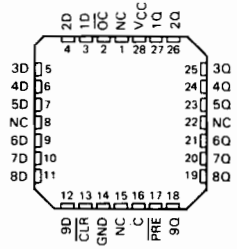
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

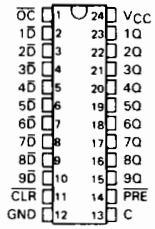
SN54ALS843, SN54AS843 . . . JT PACKAGE
SN74ALS843, SN74AS843 . . . NT PACKAGE
(TOP VIEW)



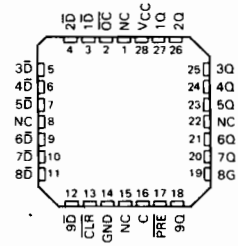
SN54ALS843, SN54AS843 . . . FH PACKAGE
SN74ALS843, SN74AS843 . . . FN PACKAGE
(TOP VIEW)



SN54ALS844, SN54AS844 . . . JT PACKAGE
SN74ALS844, SN74AS844 . . . NT PACKAGE
(TOP VIEW)



SN54ALS844, SN54AS844 . . . FH PACKAGE
SN74ALS844, SN74AS844 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

description

These 9-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The nine latches are transparent D-type. The 'ALS843 and 'AS843 have noninverting data (D) inputs. The 'ALS844 and 'AS844 have inverting D inputs.

A buffered output control ($\overline{OC}$) input can be used to place the nine outputs in either a normal logic state (high or low levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

The output control ($\overline{OC}$) does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are off.

The SN54ALS843, SN54AS843, SN54ALS844, and SN54AS844 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS843, SN74AS843, SN74ALS844, and SN74AS844 are characterized for operation from 0°C to 70°C.

FUNCTION TABLES

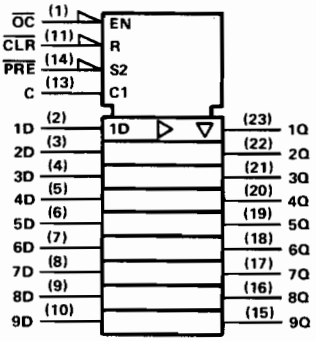
'ALS843, 'AS843

INPUTS					OUTPUT
$\overline{PRE}$	$\overline{CLR}$	$\overline{OC}$	C	D	Q
L	H	L	X	X	H
H	L	L	X	X	L
L	L	L	X	X	H
H	H	L	H	L	L
H	H	L	H	H	H
H	H	L	L	X	Q_0
X	X	H	X	X	Z

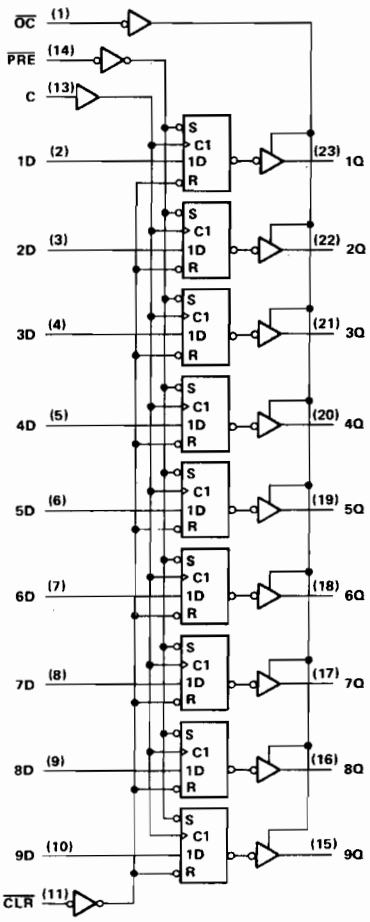
'ALS844, 'AS844

INPUTS					OUTPUT
$\overline{PRE}$	$\overline{CLR}$	$\overline{OC}$	C	$\overline{D}$	Q
L	H	L	X	X	H
H	L	L	X	X	L
L	L	L	X	X	H
H	H	L	H	L	H
H	H	L	H	H	L
H	H	L	L	X	Q_0
X	X	H	X	X	Z

logic symbol



'ALS843, 'AS843 logic diagram (positive logic)



Pin numbers shown are for JT and NT packages.
This symbol is in accordance with IEEE Std 9 and recent decisions of IEEE.

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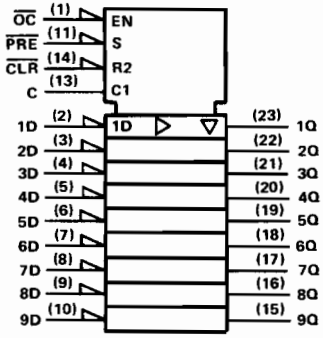
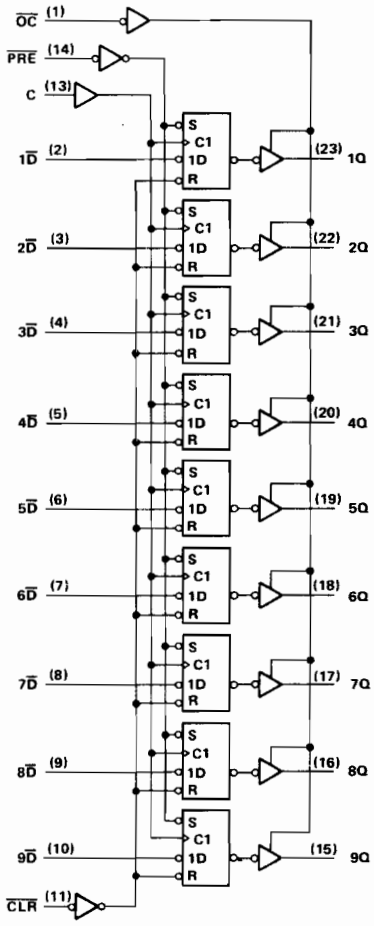
logic symbol



'ALS844, 'AS844 logic diagram (positive logic)



Pin numbers shown are for JT and NT packages.
This symbol is in accordance with IEEE Std 9 and recent decisions of IEEE.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54AS843, SN54AS844 . . . . . −55°C to 125°C
SN74AS843, SN74AS844 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS843 SN54ALS844			SN74ALS843 SN74ALS844			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	55	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−1			−2.6	mA
I_{OL}	Low-level output current				12			24	mA
t_w	Pulse duration, enable C high	'ALS843							ns
		'ALS844							
t_{su}	Setup time, data before enable C↓								ns
t_h	Hold time, data after enable C↓	'ALS843							ns
		'ALS844							
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS843 SN54ALS844			SN74ALS843 SN74ALS844			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 to 5.5 V,	I_{OH} = −0.4 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
		V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−15		−70	−15		−70	mA
I_{CC}	'ALS843	V_{CC} = 5.5 V	Outputs high							mA
			Outputs low							
			Outputs disabled		25			25		
	'ALS844		Outputs high							
			Outputs low							
			Outputs disabled		28			28		

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

Additional information on these products can be obtained from the factory as it becomes available.

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'ALS843 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS843			SN74ALS843			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	D	Q		7			7		ns
t_{PHL}				9			9		
t_{PLH}	C	Q							ns
t_{PHL}									
t_{PLH}	$\overline{PRE}$	Q							ns
t_{PHL}	$\overline{CLR}$	Q							ns
t_{PZH}	$\overline{OC}$	Q							ns
t_{PZL}									
t_{PHZ}	$\overline{OC}$	Q							ns
t_{PLZ}									

'ALS844 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS844			SN74ALS844			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	$\overline{D}$	Q		7			7		ns
t_{PHL}				9			9		
t_{PLH}	C	Q							ns
t_{PHL}									
t_{PLH}	$\overline{PRE}$	Q							ns
t_{PHL}	$\overline{CLR}$	Q							ns
t_{PZH}	$\overline{OC}$	Q							ns
t_{PZL}									
t_{PHZ}	$\overline{OC}$	Q							ns
t_{PLZ}									

†All typical values are at T_A = 25°C.
NOTE 1: For load circuit and voltage waveforms, see page 1-12 of The TTL Data Book, Volume 3.

Additional information on these products can be obtained from the factory as it becomes available.

recommended operating conditions

			SN54AS843 SN54AS844			SN74AS843 SN74AS844			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	55	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−24			−24	mA
I_{OL}	Low-level output current				32			48	mA
t_w	Pulse duration, enable C high	$\overline{CLR}$ or $\overline{PRE}$ low	5			4			ns
		C high	5			4			
t_{su}	Setup time, data before enable C↓		3.5			2.5			ns
t_h	Hold time, data after enable C↓		3.5			2.5			ns
t_r	Recovery time	$\overline{PRE}$	17			15			ns
		$\overline{CLR}$	16			14			
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS843 SN54AS844			SN74AS843 SN74AS844			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −15 mA	2.4	3.2		2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} −24 mA	2						
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.25	0.5				V
		V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−50			−50	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'AS843	V_{CC} = 5.5 V,	Outputs high		37	62		37	62	mA
			Outputs low		56	92		56	92	
			Outputs disabled		56	92		56	92	
	'AS844		Outputs high		39	64		39	64	
			Outputs low		58	95		58	95	
			Outputs disabled		58	95		58	95	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

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'ALS843 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS843		SN74AS843		
			MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	1	8.5	1	6.5	ns
t_{PHL}			1	10	1	9	
t_{PLH}	C	O	2	13	2	12	ns
t_{PHL}			2	13	2	12	
t_{PLH}	$\overline{PRE}$	Q	2	12	2	10	ns
t_{PHL}	$\overline{CLR}$	Q	2	14	2	13	ns
t_{PZH}	$\overline{OC}$	Q	2	13.5	2	10.5	ns
t_{PZL}			2	14.5	2	11.5	
t_{PHZ}	$\overline{OC}$	Q	1	10	1	8	ns
t_{PLZ}			1	10	1	8	

'ALS844 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS844		SN74AS844		
			MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	1	11	1	8.5	ns
t_{PHL}			1	11	1	10	
t_{PLH}	C	O	2	14	2	12.5	ns
t_{PHL}			2	14	2	13	
t_{PLH}	$\overline{PRE}$	Q	2	12	2	10	ns
t_{PHL}	$\overline{CLR}$	Q	2	14.5	2	13.5	ns
t_{PZH}	$\overline{OC}$	Q	2	14.5	2	12	ns
t_{PZL}			2	15	2	13.5	
t_{PHZ}	$\overline{OC}$	Q	1	10	1	8	ns
t_{PLZ}			1	10	1	8	

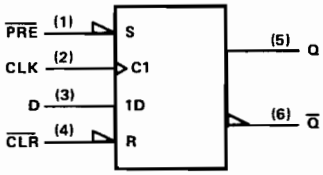
NOTE 1: For load circuit and voltage waveforms, see page 1-12 of The TTL Data Book, Volume 3.

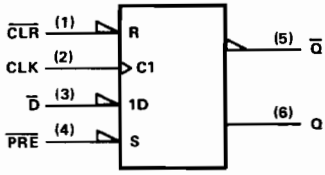
D flip-flop signal conventions

It is normal TI practice to name the outputs and other inputs of a D-type flip-flop and to draw its logic symbol based on the assumption of true data (D) inputs. Then outputs that produce data in phase with the data inputs are called $\overline{Q}$ and those producing complementary data are called Q. An input that causes a Q output to go high or a $\overline{Q}$ output to go low is called Preset; an input that causes a $\overline{Q}$ output to go high or a Q output to go low is called Clear. Bars are used over these pin names ($\overline{PRE}$ and $\overline{CLR}$) if they are active-low.

The devices on this data sheet are second-source designs and the pin-name convention used by the original manufacturer has been retained. That makes it necessary to designate the inputs and outputs of the inverting circuit $\overline{D}$ and Q. In some applications it may be advantageous to redesignate the inputs and outputs as D and $\overline{Q}$. In that case, outputs should be renamed as shown below. Also shown are corresponding changes in the graphical symbol. Arbitrary pin numbers are shown in parentheses.

Notice that Q and $\overline{Q}$ exchange names, which causes Preset and Clear to do likewise. Also notice that the polarity indicators ([▷]) on $\overline{PRE}$ and $\overline{CLR}$ remain since these inputs are still active-low, but that the presence or absence of the polarity changes at $\overline{D}$, Q, and $\overline{Q}$. Of course pin 5 (Q) is still in phase with the data input D, but now both are considered active high.





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- **3-State Buffer-Type Outputs Drive Bus-Lines Directly**
- **Bus-Structured Pinout**
- **Provides Extra Bus Driving Latches Necessary for Wider Address/Data Paths or Buses with Parity**
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- **Dependable Texas Instruments Quality and Reliability**

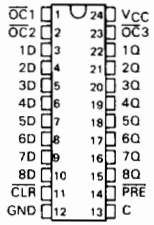
description

These 8-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

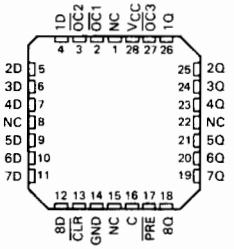
The eight latches are transparent D-type. The 'ALS845 and 'AS845 have noninverting data (D) inputs. The 'ALS846 and 'AS846 have inverting $\overline{D}$ inputs. Since $\overline{CLR}$ and $\overline{PRE}$ are independent of the clock, taking the $\overline{CLR}$ input low will cause the eight Q outputs to go low. Taking the $\overline{PRE}$ input low will cause the eight Q outputs to go high. When both $\overline{PRE}$ and $\overline{CLR}$ are taken low, the outputs will follow the preset condition.

A buffered output control ($\overline{OC}$) input can be used to place the eight outputs in either a normal logic state (high or low levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

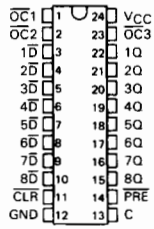
SN54ALS845, SN54AS845 . . . JT PACKAGE
SN74ALS845, SN74AS845 . . . NT PACKAGE
(TOP VIEW)



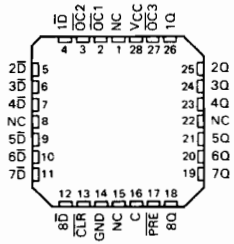
SN54ALS845, SN54AS845 . . . FH PACKAGE
SN74ALS845, SN74AS845 . . . FN PACKAGE
(TOP VIEW)



SN54ALS846, SN54AS846 . . . JT PACKAGE
SN74ALS846, SN74AS846 . . . NT PACKAGE
(TOP VIEW)



SN54ALS846, SN54AS846 . . . FH PACKAGE
SN74ALS846, SN74AS846 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

PRODUCT PREVIEW
This page contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

The output controls ($\overline{OC1}$, $\overline{OC2}$, $\overline{OC3}$) do not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54ALS845, SN54AS845, SN54ALS846, and SN54AS846 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS845, SN74AS845, SN74ALS846, and SN74AS846 are characterized for operation from 0°C to 70°C.

FUNCTION TABLES

'ALS845, 'AS845

INPUTS							OUTPUT
$\overline{PRE}$	$\overline{CLR}$	$\overline{OC1}$	$\overline{OC2}$	$\overline{OC3}$	C	D	Q
L	H	L	L	L	X	X	H
H	L	L	L	L	X	X	L
L	L	L	L	L	X	X	H
H	H	L	L	L	H	L	L
H	H	L	L	L	H	H	H
H	H	L	L	L	L	X	Q_0
X	X	L	L	H	X	X	Z
X	X	L	H	L	X	X	Z
X	X	L	H	H	X	X	Z
X	X	H	L	L	X	X	Z
X	X	H	L	H	X	X	Z
X	X	H	H	L	X	X	Z
X	X	H	H	H	X	X	Z

'ALS846, 'AS846

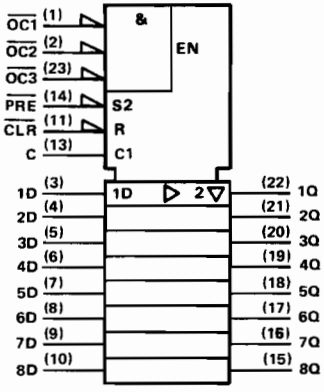
INPUTS							OUTPUT
$\overline{PRE}$	$\overline{CLR}$	$\overline{OC1}$	$\overline{OC2}$	$\overline{OC3}$	C	$\overline{D}$	Q
L	H	L	L	L	X	X	H
H	L	L	L	L	X	X	L
L	L	L	L	L	X	X	H
H	H	L	L	L	H	L	H
H	H	L	L	L	H	H	L
H	H	L	L	L	L	X	Q_0
X	X	L	L	H	X	X	Z
X	X	L	H	L	X	X	Z
X	X	L	H	H	X	X	Z
X	X	H	L	L	X	X	Z
X	X	H	L	H	X	X	Z
X	X	H	H	L	X	X	Z
X	X	H	H	H	X	X	Z

2

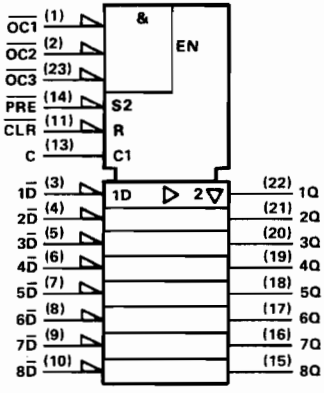
ALS AND AS CIRCUITS

logic symbols

'ALS845, 'AS845



'ALS846, 'AS846



Pin numbers shown are for JT and NT packages.
These symbols are in accordance with IEEE Std 9 and recent decisions of IEEE.

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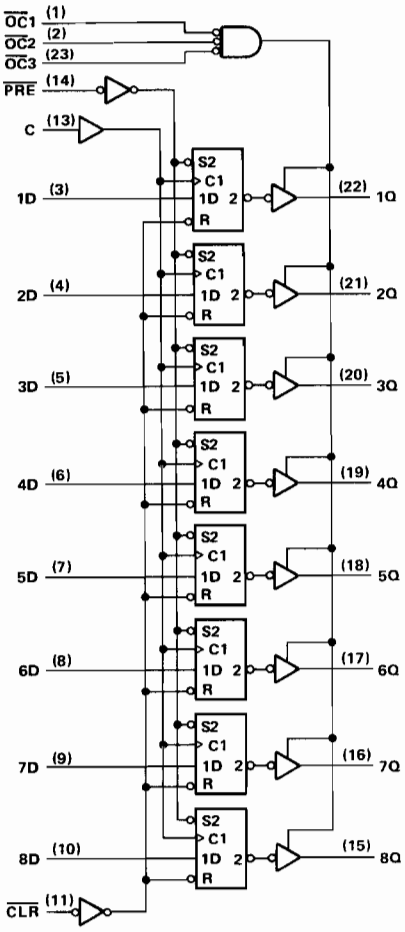
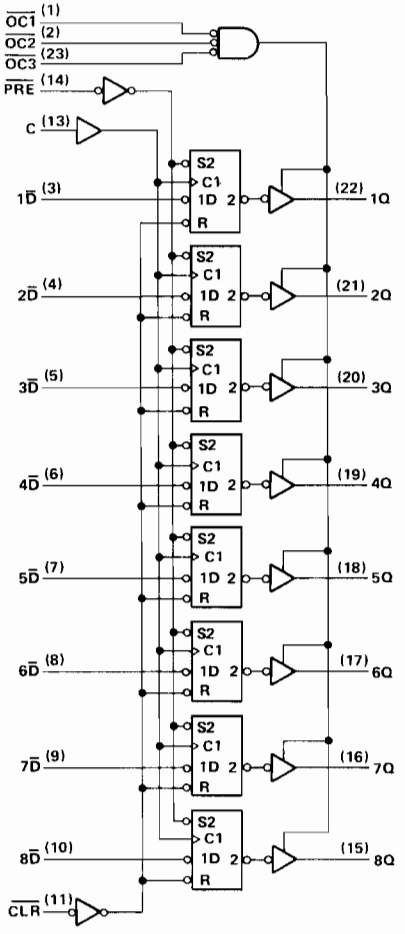
logic diagrams (positive logic)

'ALS845, 'AS845



'ALS846, 'AS846



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range:
SN54ALS845, SN54AS845, SN54ALS846, SN54AS846 . . . . . —55°C to 125°C
SN74ALS845, SN74AS845, SN74ALS846, SN74AS846 . . . . . −0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54ALS845 SN54ALS846			SN74ALS845 SN74ALS846			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−1			−2.6	mA
I_{OL}	Low-level output current				12			24	mA
t_w	Pulse duration	$\overline{CLR}$ or $\overline{PRE}$ low							ns
		C high							
t_{su}	Setup time, data before enable C↓								ns
t_h	Hold time, data after enable C↓	'ALS845							ns
		'ALS846							
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS845 SN54ALS846			SN74ALS845 SN74ALS846			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC} − 2			V_{CC} − 2			V
		V_{CC} = 4.5 V,	I_{OH} = −1 mA	2.4	3.3					
		V_{CC} = 4.5 V,	I_{OH} = −2.6 mA				2.4	3.2		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−20			−20	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−15		−70	−15		−70	mA
I_{CC}	'ALS845	V_{CC} = 5.5 V	Outputs high							mA
			Outputs low							
			Outputs disabled		25			25		
	'ALS846		Outputs high							
			Outputs low							
			Outputs disabled		28			28		

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

Additional information on these products can be obtained from the factory as it becomes available.

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'ALS845 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS845			SN74ALS845			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	D	Q		7			7		ns
t_{PHL}				9			9		
t_{PLH}	C	Q							ns
t_{PHL}									
t_{PLH}	$\overline{PRE}$	Q							ns
t_{PHL}	$\overline{CLR}$	Q							ns
t_{PZH}	$\overline{OC}$	Q							ns
t_{PZL}									
t_{PHZ}	$\overline{OC}$	Q							ns
t_{PLZ}									

'ALS846 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX						UNIT
			SN54ALS846			SN74ALS846			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	$\overline{D}$	Q		7			7		ns
t_{PHL}				9			9		
t_{PLH}	C	Q							ns
t_{PHL}									
t_{PLH}	$\overline{PRE}$	Q							ns
t_{PHL}	$\overline{CLR}$	Q							ns
t_{PZH}	$\overline{OC}$	Q							ns
t_{PZL}									
t_{PHZ}	$\overline{OC}$	Q							ns
t_{PLZ}									

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: For load circuit and voltage waveforms, see page 1-12 of the TTL Data Book, Volume 3.

Additional information on these products can be obtained from the factory as it becomes available.

recommended operating conditions

			SN54AS845 SN54AS846			SN74AS845 SN74AS846			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−24			−24	mA
I_{OL}	Low-level output current				32			48	mA
t_w	Pulse duration	$\overline{CLR}$ or $\overline{PRE}$ low	5			4			ns
		C high	5			4			
t_{su}	Setup time, data before enable C↑		3.5			2.5			ns
t_h	Hold time, data after enable C↑		3.5			2.5			ns
t_r	Recovery time	$\overline{PRE}$	17			15			ns
		$\overline{CLR}$	16			14			
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS845 SN54AS846			SN74AS845 SN74AS846			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = −2 mA	V_{CC} − 2			V_{CC} − 2			V
		V_{CC} = 4.5 V,	I_{OH} = −15 mA	2.4	3.2		2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −24 mA	2			2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.25	0.5				V
		V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−50			−50	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'AS845	V_{CC} = 5.5 V	Outputs high		35	58		35	58	mA
			Outputs low		52	85		52	85	
			Outputs disabled		52	85		52	85	
	'AS846		Outputs high		36			36		
			Outputs low		53			53		
			Outputs disabled		53			53		

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

Additional information on these products can be obtained from the factory as it becomes available.

ADVANCE INFORMATION
This page contains information on a new product. Specifications are subject to change without notice.

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'AS845 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS845		SN74AS845		
			MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	1	8.5	1	6.5	ns
t_{PHL}			1	10	1	9	
t_{PLH}	C	Q	2	13	2	12	ns
t_{PHL}			2	13	2	12	
t_{PLH}	$\overline{PRE}$	Q	2	12	2	10	ns
t_{PHL}	$\overline{CLR}$	Q	2	14	2	13	ns
t_{PZH}	$\overline{OC}$	Q	2	13.5	2	10.5	ns
t_{PZL}			2	14.5	2	11.5	
t_{PHZ}	$\overline{OC}$	Q	1	10	1	8	ns
t_{PLZ}			1	10	1	8	

'AS846 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX						UNIT
			SN54AS846			SN74AS846			
			MIN	TYP†	MAX	MIN	TYP†	MAX	
t_{PLH}	$\overline{D}$	Q		4			4		ns
t_{PHL}				4.5			4.5		
t_{PLH}	C	Q							ns
t_{PHL}									
t_{PLH}	$\overline{PRE}$	Q		5			5		ns
t_{PHL}	$\overline{CLR}$	Q		5.5			5.5		ns
t_{PZH}	$\overline{OC}$	Q		6			6		ns
t_{PZL}				6			6		
t_{PHZ}	$\overline{OC}$	Q		4			4		ns
t_{PLZ}				5			5		

†All typical values are at T_A = 25°C.

NOTE 1: For load circuit and voltage waveforms, see page 1-12 of The TTL Data Book, Volume 3.

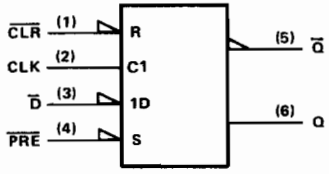
Additional information on these products can be obtained from the factory as it becomes available.

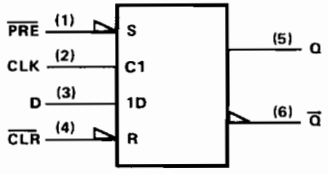
D flip-flop signal conventions

It is normal TI practice to name the outputs and other inputs of a D-type latch and to draw its logic symbol based on the assumption of true data (D) inputs. Then outputs that produce data in phase with the data inputs are called Q and those producing complementary data are called $\overline{Q}$. An input that causes a Q output to go high or a $\overline{Q}$ output to go low is called Preset; an input that causes a $\overline{Q}$ output to go high or a Q output to go low is called Clear. Bars are used over these pin names ($\overline{PRE}$ and $\overline{CLR}$) if they are active-low.

The devices on this data sheet are second-source designs and the pin name convention used by the original manufacturer has been retained. That makes it necessary to designate the inputs and outputs of the inverting circuit $\overline{D}$ and Q. In some applications it may be advantageous to redesignate the inputs and outputs as D and $\overline{Q}$. In that case, outputs should be renamed as shown below. Also shown are corresponding changes in the graphical symbol. Arbitrary pin numbers are shown in parentheses.

Notice that Q and $\overline{Q}$ exchange names, which causes Preset and Clear to do likewise. Also notice that the polarity indicators ( ) on $\overline{PRE}$ and $\overline{CLR}$ remain since these inputs are still active-low, but that the presence or absence of the polarity indicator changes at $\overline{D}$, Q, and $\overline{Q}$. Of course pin 5 (Q) is still in phase with the data input D, but now both are considered active high.





TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

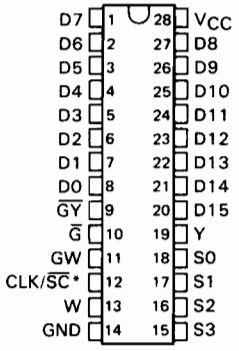
DECEMBER 1983—REVISED APRIL 1984

- **4-Line to 1-Line Data Selectors/Multiplexers That Can Select 1 of 16 Data Inputs. Typical Applications:**

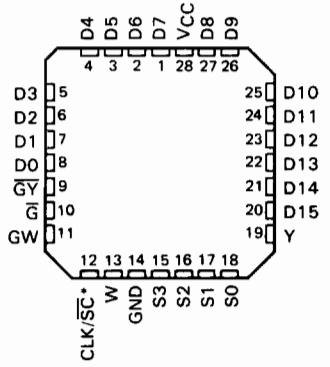
  Boolean Function Generators
  Parallel-to-Serial Converters
  Data Source Selectors

- **Cascadable to n-Bits**
- **3-State Bus Driver Outputs**
- **'AS850 Offers Clocked Selects; 'AS851 Offers Enable-Controlled Selects**
- **Has a Master Output Control ($\overline{G}$) for Cascading and Individual Output Controls ($\overline{GY}$, GW) for Each Output**
- **Package Options Include both Plastic and Ceramic Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54AS850, SN54AS851 . . . JD PACKAGE
SN74AS850, SN74AS851 . . . N PACKAGE
(TOP VIEW)



SN54AS850, SN54AS851 . . . FH PACKAGE
SN74AS850, SN74AS851 . . . FN PACKAGE
(TOP VIEW)



*CLK for 'AS850 or $\overline{SC}$ for 'AS851

description

These four-line to one-line data selectors/multiplexers provide full binary decoding to select one-of-sixteen data sources with complementary Y and W outputs. The 'AS850 has a clock-controlled select register allowing for a symmetrical presentation of the select inputs to the decoder while the 'AS851 has an enable-controlled select register allowing the user to select and hold one particular data line.

A buffered group of output controls ($\overline{G}$, $\overline{GY}$, GW) can be used to place the two outputs in either a normal logic (high or low logic level) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without the need for interface or pull-up components.

The output controls do not affect the internal operations of the data selector/multiplexer. New data can be setup while the outputs are in the high-impedance state.

The SN54AS850 and SN54AS851 are characterized for operation over the full military temperature range from −55°C to 125°C. The SN74AS850 and SN74AS851 are characterized for operation from 0°C to 70°C.

INPUT SELECTION TABLE

SELECT INPUTS				'AS850	'AS851	INPUT
S3	S2	S1	S0	CLK	$\overline{SC}$	SELECTED
L	L	L	L	↑	L	D0
L	L	L	H	↑	L	D1
L	L	H	L	↑	L	D2
L	L	H	H	↑	L	D3
L	H	L	L	↑	L	D4
L	H	L	H	↑	L	D5
L	H	H	L	↑	L	D6
L	H	H	H	↑	L	D7
H	L	L	L	↑	L	D8
H	L	L	H	↑	L	D9
H	L	H	L	↑	L	D10
H	L	H	H	↑	L	D11
H	H	L	L	↑	L	D12
H	H	L	H	↑	L	D13
H	H	H	L	↑	L	D14
H	H	H	H	↑	L	D15
X	X	X	X	H or L	H	Dn

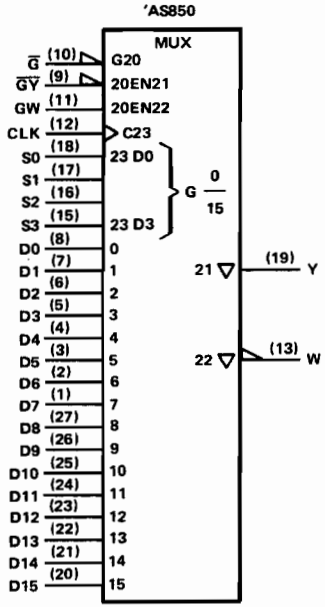
Dn = the input selected before the most-recent low-to-high transition of CLK or SC.

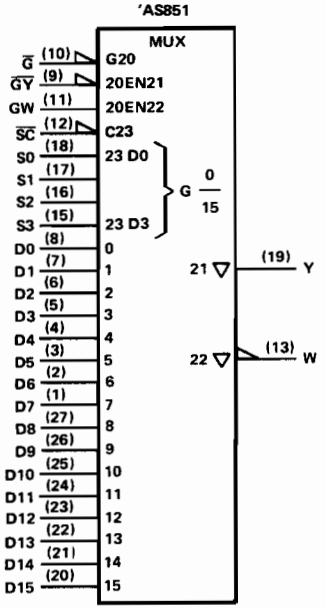
OUTPUT FUNCTION TABLE

$\overline{G}$	$\overline{GY}$	GW	OUTPUTS Y	OUTPUTS W
H	X	X	Z	Z
L	H	L	Z	Z
L	L	L	D	Z
L	H	H	Z	$\overline{D}$
L	L	H	D	$\overline{D}$

D = level of selected input D0–D15

logic symbols





TEXAS INSTRUMENTS
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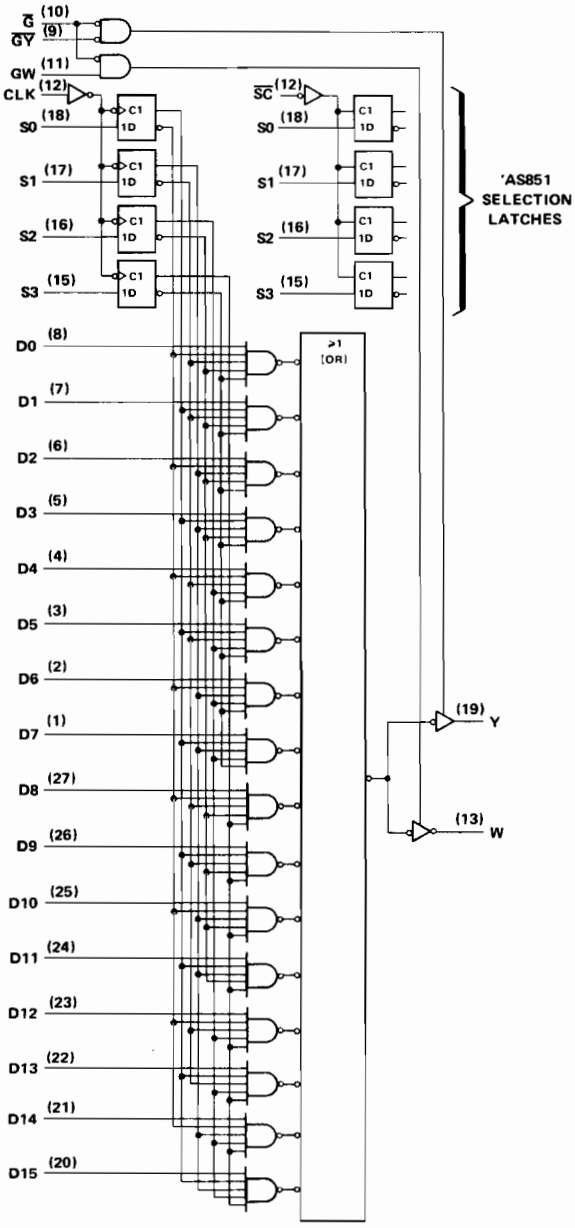
'AS850 logic diagram (positive logic) (see inset for 'AS851)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54AS850, SN54AS851 . . . . . −55°C to 125°C
SN74AS850, SN74AS851 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54AS850			SN74AS850			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−12			−15	mA
I_{OL}	Low-level output current				32			48	mA
f_{clock}	Clock frequency					0		60	MHz
t_w	Pulse duration	CLK high				8			ns
		CLK low				8			
t_{su}	Setup time, select inputs before CLK↑					10			ns
t_h	Hold time, select inputs after CLK↑					0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS850			SN74AS850			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2	3.2					
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2	3.3		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.25	0.5				V
		V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−50			−50	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	D, $\overline{G}$	V_{CC} = 5.5 V,	V_I = 0.4 V			−1			−1	mA
	All others					−0.5			−0.5	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V	Outputs active		50			50	81	mA
			Outputs disabled		52			52	85	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit current, I_{OS}.

Additional information on these products can be obtained from the factory as it becomes available.

TEXAS INSTRUMENTS
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switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS850			SN74AS850	
			MIN	TYP†	MAX	MIN	MAX	
f_{max}						60		MHz
t_{PLH}	Any D	Y		5		3	10.5	ns
t_{PHL}				7		3	11	
t_{PLH}	Any D	W		5		3	8	ns
t_{PHL}				3.5		1	6	
t_{PLH}	CLK	Y		10.5		3	14.5	ns
t_{PHL}				12		3	17.5	
t_{PLH}	CLK	W		10		3	15	ns
t_{PHL}				9		3.5	13	
t_{PZH}	$\overline{G}$	Y		5		2	8	ns
t_{PZL}				6		3	11	
t_{PHZ}	$\overline{G}$	Y		5		1	6	ns
t_{PLZ}				5.5		2	8	
t_{PZH}	$\overline{G}$	W		5		2	8	ns
t_{PZL}				11		3	21	
t_{PHZ}	$\overline{G}$	W		5		1	6	ns
t_{PLZ}				5.5		2	8	
t_{PZH}	$\overline{GY}$	Y		5		2	8	ns
t_{PZL}				6		3	11	
t_{PHZ}	$\overline{GY}$	Y		5		1	6	ns
t_{PLZ}				5.5		2	8	
t_{PZH}	GW	W		6		2	10	ns
t_{PZL}				11		3	25	
t_{PHZ}	GW	W		3.5		1	6	ns
t_{PLZ}				7.5		2	11	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: For load circuit and voltage waveforms, see page 1-12 of The TTL Data Book, Volume 3.

TEXAS INSTRUMENTS
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recommended operating conditions

			SN54AS851			SN74AS851			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−12			−15	mA
I_{OL}	Low-level output current				32			48	mA
t_w	Pulse duration	$\overline{SC}$ low				10			ns
t_{su}	Setup time, select inputs before $\overline{SC}$↑					4.5			ns
t_h	Hold time, select inputs after $\overline{SC}$↑					0			
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS851			SN74AS851			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2	3.2					
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2	3.3		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.25	0.5				V
		V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−50			−50	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	D, $\overline{G}$	V_{CC} = 5.5 V,	V_I = 0.4 V			−1			−1	mA
	All others					−0.5			−0.5	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V	Outputs active		50			50	81	mA
			Outputs disabled		52			52	85	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit current, I_{OS}.

Additional information on these products can be obtained from the factory as it becomes available.

TEXAS INSTRUMENTS
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switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS851			SN74AS851	
			MIN	TYP†	MAX	MIN	MAX	
t_{PLH}	Any D	Y		5		3	10.5	ns
t_{PHL}				7		3	11	
t_{PLH}	Any D	W		5		3	8	ns
t_{PHL}				3.5		1	6	
t_{PLH}	S0, S1, S2, S3	Y		12		3	18	ns
t_{PHL}				15		3	19	
t_{PLH}	S0, S1, S2, S3	W		12		3	16	ns
t_{PHL}				10		3	15	
t_{PLH}	$\overline{SC}$	Y		12		3	18	ns
t_{PHL}				15		3	20	
t_{PLH}	$\overline{SC}$	W		12		3	16	ns
t_{PHL}				11		3	15	
t_{PZH}	$\overline{G}$	Y		5.5		2	8	ns
t_{PZL}				7		3	11	
t_{PHZ}	$\overline{G}$	Y		3.5		1	6	ns
t_{PLZ}				5		2	8	
t_{PZH}	$\overline{G}$	W		5.5		2	8	ns
t_{PZL}				11		3	21	
t_{PHZ}	$\overline{G}$	W		3.5		1	6	ns
t_{PLZ}				5		2	8	
t_{PZH}	$\overline{GY}$	Y		5.5		2	8	ns
t_{PZL}				7		3	11	
t_{PHZ}	$\overline{GY}$	Y		3.5		1	6	ns
t_{PZL}				6		2	8	
t_{PZH}	GW	W		6		2	10	ns
t_{PZL}				12		3	25	
t_{PHZ}	GW	W		4		1	6	ns
t_{PLZ}				8		2	11	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: For load circuit and voltage waveforms, see page 1-12 of The TTL Data Book, Volume 3.

TYPICAL APPLICATION DATA

The 'AS850 or 'AS851 can be used as a 1-of-16 Boolean function generator. Figure 1 shows the 'AS850 in one example.

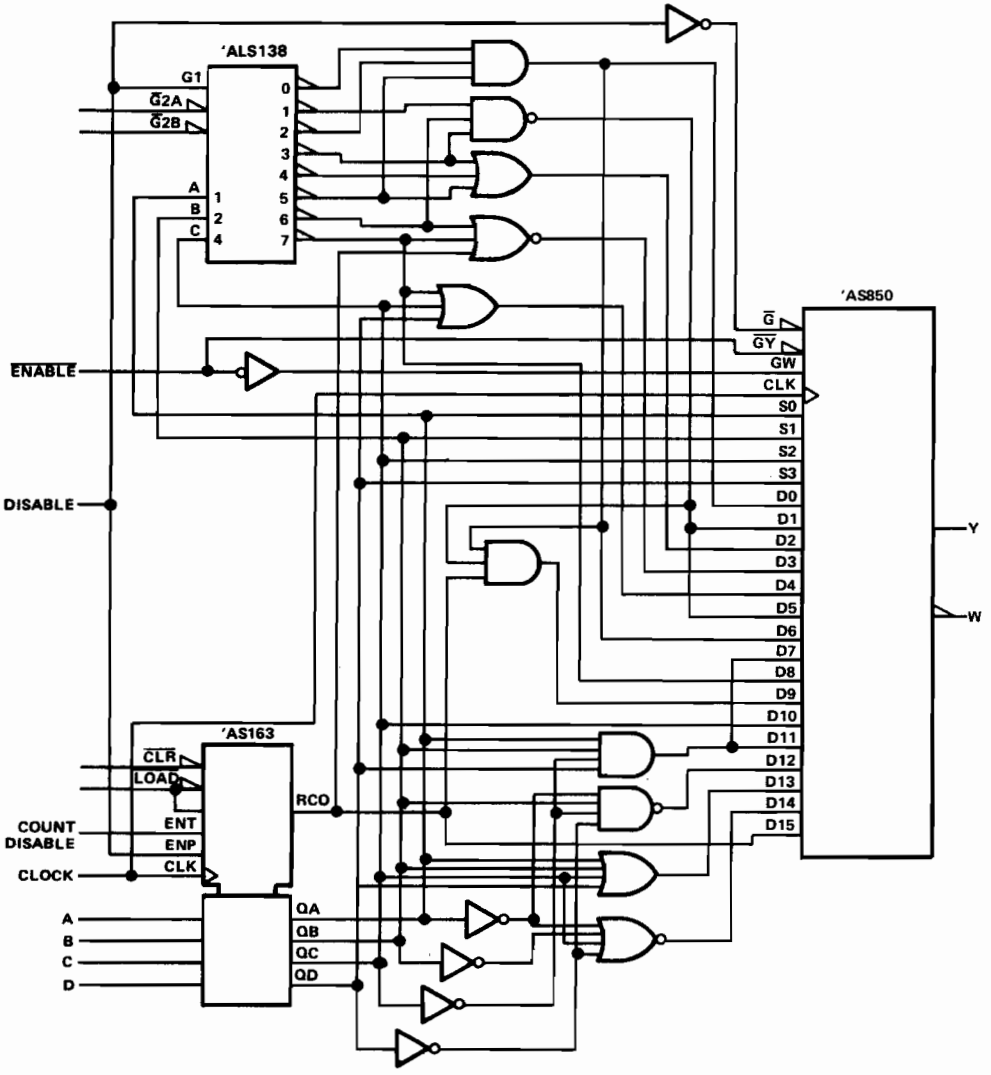

FIGURE 1—1-OF-16 BOOLEAN FUNCTION GENERATOR

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TYPICAL APPLICATION DATA

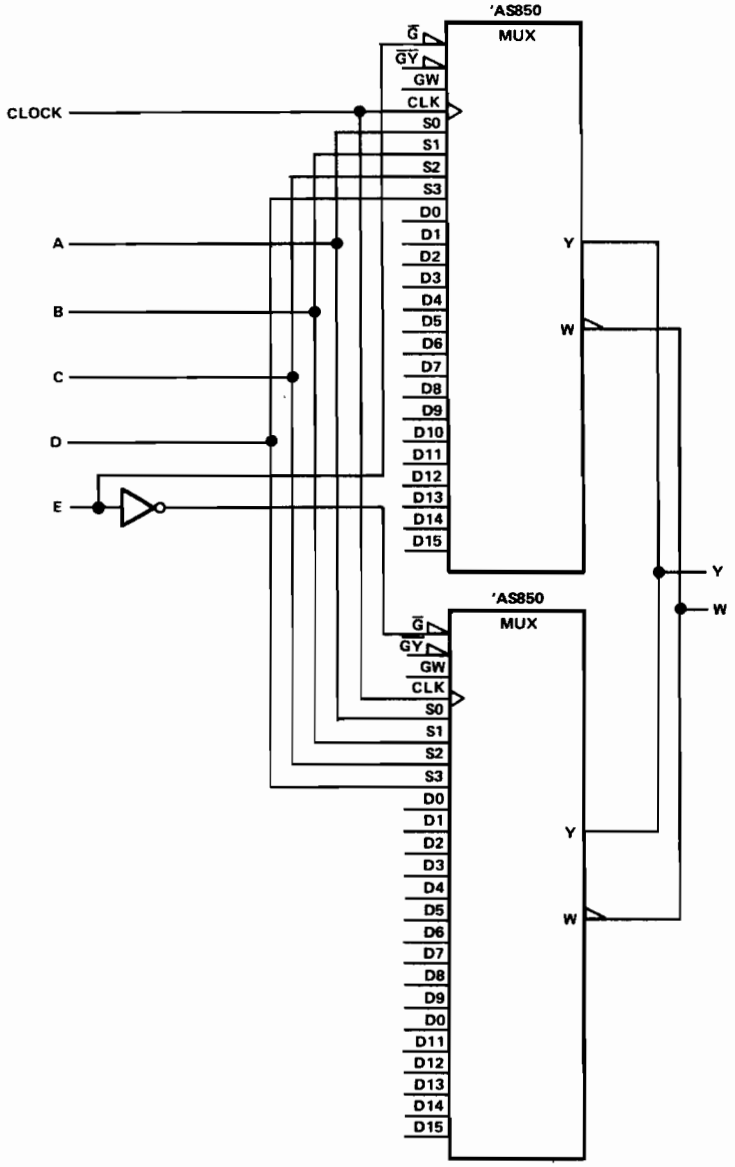

FIGURE 2–1-OF-32 DATA/SELECTOR/MULTIPLEXER

TYPICAL APPLICATION DATA

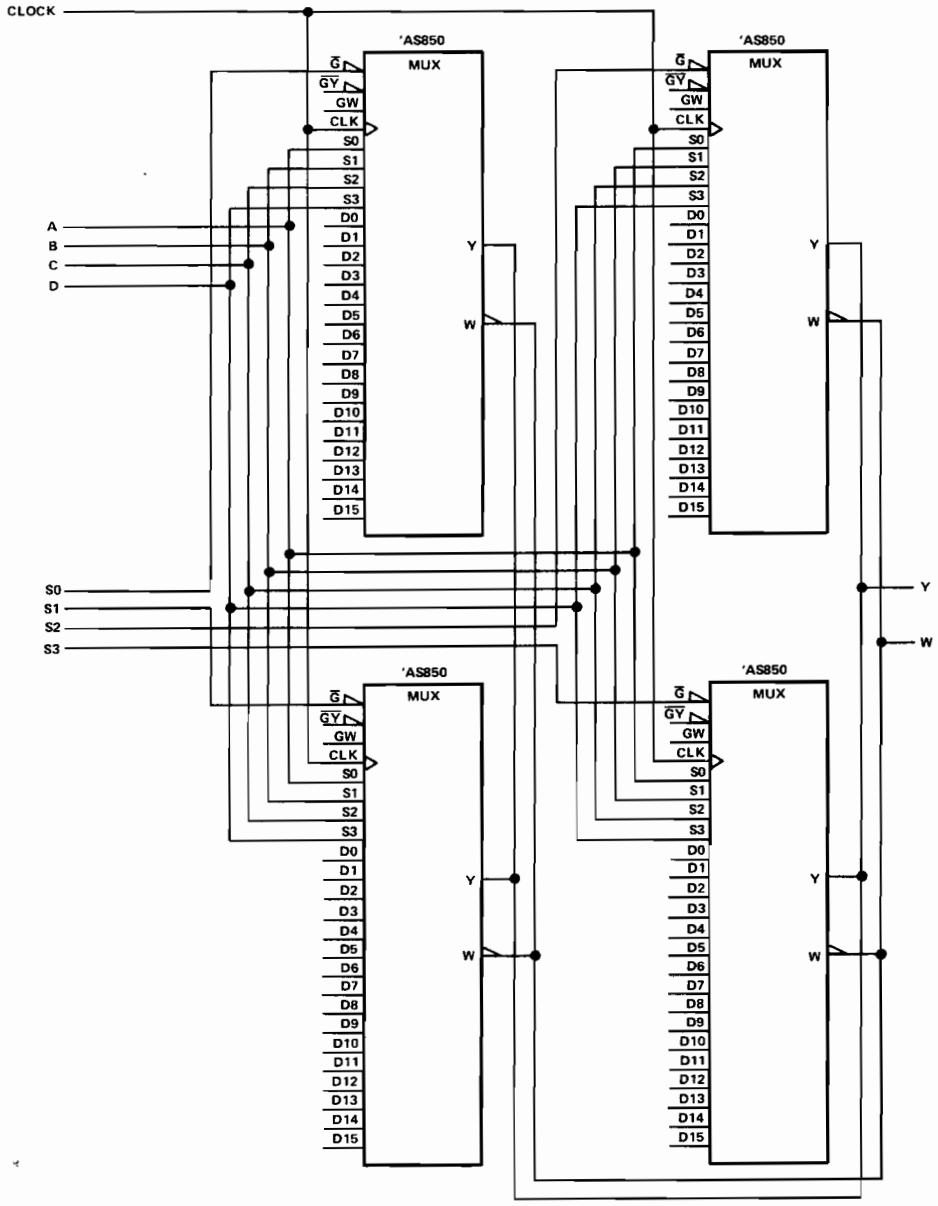

FIGURE 3–1-OF-64 DATA SELECTOR/MULTIPLEXER

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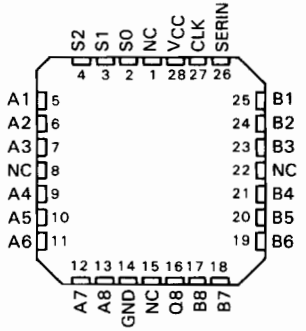
D2661, DECEMBER 1982–REVISED FEBRUARY 1984

- Included among the Package Options Are Compact, 24-Pin, 300-mil-Wide Dips and Both 28-Pin Plastic and Ceramic Chip Carriers
- Buffered 3-State Outputs Drive Bus Lines Directly
- Cascadable to n-Bits
- Eight Selectable Transceiver/Port Functions:
  - A to B or B to A
  - Register to A or Register to B
  - Shifted to A or Shifted to B
  - Off-Line Shifts (A and B Ports in High-Impedance State)
  - Register Clear
- Particularly Suitable for Use in Signature-Analysis Circuitry
- Serial Register Provides:
  - Parallel Storage of Either A or B Input Data
  - Serial Transmission of Data from Either A or B Port
- Dependable Texas Instruments Quality and Reliability

SN54AS877 . . . . JT PACKAGE
SN74AS877 . . . . NT PACKAGE
(TOP VIEW)

SN54AS877 . . . . FH PACKAGE
SN74AS877 . . . . FN PACKAGE
(TOP VIEW)



NC – No internal connection

description

The 'AS877 features two 8-bit I/O ports (A1-A8 and B1-B8), an 8-bit parallel-load, serial-in, parallel-out shift register, and control logic. With these features, this device is capable of performing eight selectable transceiver or port functions, depending on the state of the three select lines S0, S1, and S2. These functions include: transferring data from port A to port B or vice versa (i.e., the transceiver function), transferring data from the register to either port, serial shifting data to either port, performing off-line shifts (with A and B ports in high-impedance state), and clearing the register. Synchronous parallel loading of the internal register can be accomplished from either port on the positive transition of the clock while serially shifting data in via the SERIN input. The 'AS877 is ideally suited for applications needing signature-analysis circuitry to enhance system verification and/or fault analysis. All serial data is shifted right. All outputs are buffer-type outputs designed specifically to drive bus lines directly and all are 3-state except for Q8, which is a totem-pole output.

The SN54AS877 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74AS877 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

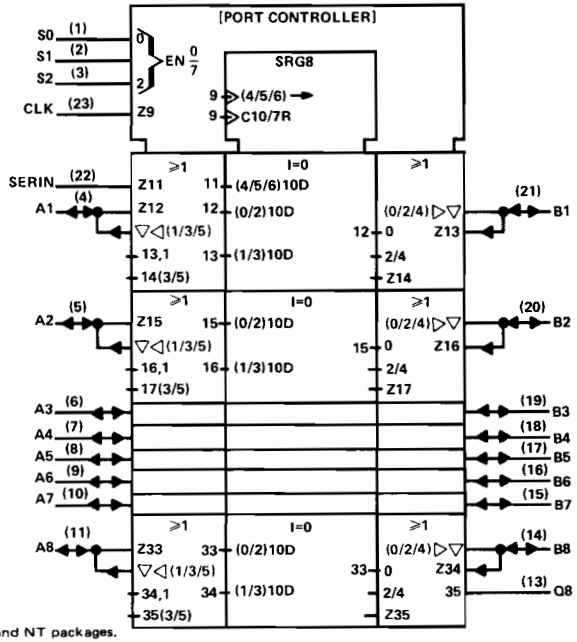
MODE S2 S1 S0	CLOCK	SERIN	A1 Q1 B1	A2 Q2 B2	A3 Q3 B3	A4 Q4 B4	A5 Q5 B5	A6 Q6 B6	A7 Q7 B7	A8 Q8 B8	PORT FUNCTION
L L L	H or L	X	Z Q_n A1	Z Q_n A2	Z Q_n A2	Z Q_n A4	Z Q_n A5	Z Q_n A6	Z Q_n A7	Z Q_n A8	A TO B
L L L	↑	X	Z A1 A1	Z A2 A2	Z A3 A3	Z A4 A4	Z A5 A5	Z A6 A6	Z A7 A7	Z A8 A8	
L L H	H or L	X	B1 Q_n Z	B2 Q_n Z	B3 Q_n Z	B4 Q_n Z	B5 Q_n Z	B6 Q_n Z	B7 Q_n Z	B8 Q_n Z	B TO A
L L H	↑	X	B1 B1 Z	B2 B2 Z	B3 B3 Z	B4 B4 Z	B5 B5 Z	B6 B6 Z	B7 B7 Z	B8 B8 Z	
L H L	H or L	X	X Q_n Q1	X Q_n Q2	X Q_n Q3	X Q_n Q4	X Q_n Q5	X Q_n Q6	X Q_n Q7	X Q_n Q8	Q_N TO B_N
L H L	↑	X	Z A1 A1	Z A2 A2	Z A3 A3	Z A4 A4	Z A5 A5	Z A6 A6	Z A7 A7	Z A8 A8	
L H H	H or L	X	Q1 Q_n X	Q2 Q_n X	Q3 Q_n X	Q4 Q_n X	Q5 Q_n X	Q6 Q_n X	Q7 Q_n X	Q8 Q_n X	Q_N TO A_N
L H H	↑	X	B1 B1 Z	B2 B2 Z	B3 B3 Z	B4 B4 Z	B5 B5 Z	B6 B6 Z	B7 B7 Z	B8 B8 Z	
H L L	H or L	X	Z Q_n Q1	Z Q_n Q2	Z Q_n Q3	Z Q_n Q4	Z Q_n Q5	Z Q_n Q6	Z Q_n Q7	Z Q_n Q8	SHIFT
H L L	↑	H	Z H H	Z Q1 Q1	Z Q2 Q2	Z Q3 Q3	Z Q4 Q4	Z Q5 Q5	Z Q6 Q6	Z Q7 Q7	TO
H L L	↑	L	Z L L	Z Q1 Q1	Z Q2 Q2	Z Q3 Q3	Z Q4 Q4	Z Q5 Q5	Z Q6 Q6	Z Q7 Q7	B
H L H	H or L	X	Q1 Q_n Z	Q2 Q_n Z	Q3 Q_n Z	Q4 Q_n Z	Q5 Q_n Z	Q6 Q_n Z	Q7 Q_n Z	Q8 Q_n Z	SHIFT
H L H	↑	H	H H Z	Q1 Q1 Z	Q2 Q2 Z	Q3 Q3 Z	Q4 Q4 Z	Q5 Q5 Z	Q6 Q6 Z	Q7 Q7 Z	TO
H L H	↑	L	L L Z	Q1 Q1 Z	Q2 Q2 Z	Q3 Q3 Z	Q4 Q4 Z	Q5 Q5 Z	Q6 Q6 Z	Q7 Q7 Z	A
H H L	H or L	X	Z Q_n Z	Z Q_n Z	Z Q_n Z	Z Q_n Z	Z Q_n Z	Z Q_n Z	Z Q_n Z	Z Q_n Z	SHIFT
H H L	↑	H	Z H Z	Z Q1 Z	Z Q2 Z	Z Q3 Z	Z Q4 Z	Z Q5 Z	Z Q6 Z	Z Q7 Z	
H H L	↑	L	Z L Z	Z Q1 Z	Z Q2 Z	Z Q3 Z	Z Q4 Z	Z Q5 Z	Z Q6 Z	Z Q7 Z	
H H H	H or L	X	Z Q_n Z	Z Qn Z	Z Q_n Z	Z Q_n Z	Z Q_n Z	Z Q_n Z	Z Q_n Z	Z Q_n Z	CLEAR
H H H	↑	X	Z L Z	Z L Z	Z L Z	Z L Z	Z L Z	Z L Z	Z L Z	Z L Z	

n = level of Q_n(n = 1, 2 . . . 8) established on most recent ↑ transition of CLK. Q1 thru Q8 are the shift register outputs; only Q8 is available externally. The double inversions that take place as data travels from port to port are ignored in this table.

2

ALS AND AS CIRCUITS

logic symbol



Pin numbers shown are for J and NT packages.

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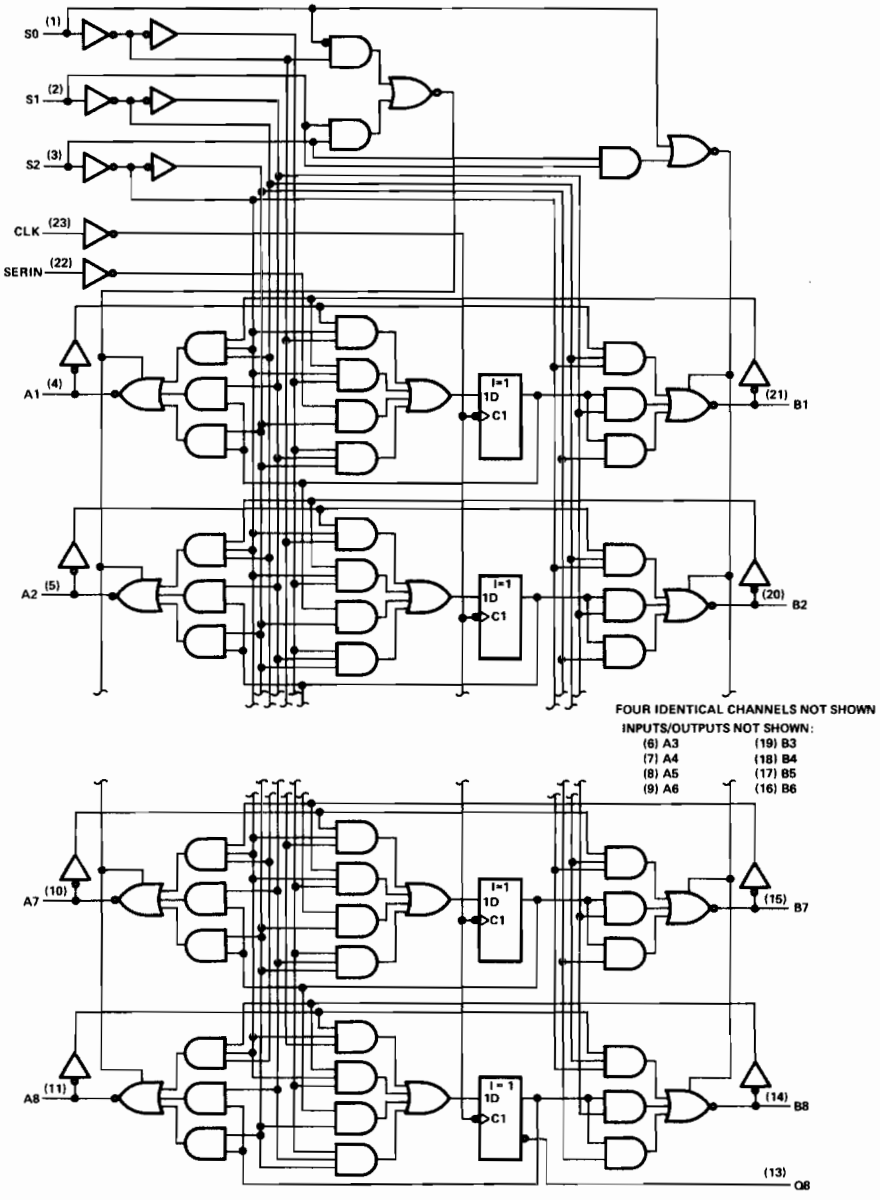
logic diagram (positive logic)



absolute maximum ratings over free-air temperature range

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range: SN54AS877 . . . . . −55°C to 125°C
SN74AS877 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

			SN54AS877			SN74AS877			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current	A1-A8, B1-B8			−12			−15	mA
		Q8			−2			−2	
I_{OL}	Low-level output current	A1-A8, B1-B8			32			48	mA
		Q8			20			20	
f_{clock}	Clock frequency		0		45	0		50	MHz
t_w	Duration of clock pulse		11			10			ns
t_{su}	Setup time before CLK↑	A1-A8, B1-B8 SERIN	5.5			5.5			ns
		S0, S1, S2	5.5			5.5			
t_h	Hold time, data after CLK↑	A1-A8, B1-B8 SERIN	0			0			ns
		S0, S1, S2	0			0			
T_A	Operating free-air temperature		−55		125	0		70	°C

Additional information on these products can be obtained from the factory as it becomes available.

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS877			SN74AS877			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	A1-A8	V_{CC} = 4.5 V,	I_{OH} = −12 mA	2	3.2					V
	B1-B8	V_{CC} = 4.5 V,	I_{OH} = −15 mA				2	3.3		
	All outputs	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC} − 2			V_{CC} − 2			
V_{OL}	All outputs except Q8	V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.25	0.5				V
		V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
	Q8	V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.25	0.5		0.25	0.5	
I_I	S0, S1, S2	V_{CC} = 5.5 V,	V_I = 7 V			0.3			0.3	mA
	CLK and SERIN					0.1			0.1	
	A1-A8, B1-B8	V_{CC} = 5.5 V,	V_I = 5.5 V			0.2			0.2	
I_{IH}	S0, S1, S2	V_{CC} = 5.5 V,	V_I = 2.7 V			60			60	μA
	CLK and SERIN					20			20	
	A1-A8, B1-B8‡					70			70	
I_{IL}	S0, S1, S2	V_{CC} = 5.5 V,	V_I = 0.4 V			−1			−1	mA
	CLK and SERIN					−0.5			−0.5	
	A1-A8, B1-B8‡					−0.75			−0.75	
I_O§	Except Q8	V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
	Q8			−20		−112	−20		−112	
I_{CC}		V_{CC} = 5.5 V			136	220		136	220	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡For I/O ports, the parameters I_{IH} and I_{IL} include the output currents I_{OZH} and I_{OZL}, respectively.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

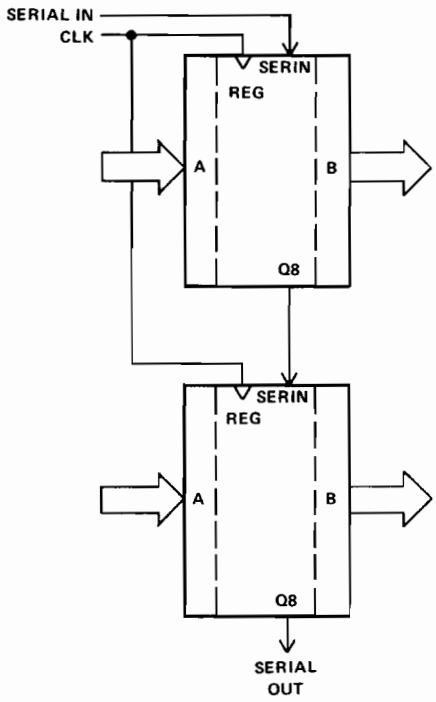
switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS877		SN74AS877		
			MIN	MAX	MIN	MAX	
f_{max}			45		50		MHz
t_{PLH}	Any A port	Any B port	2	8.5	2	7	ns
t_{PHL}			3	10.5	3	9	
t_{PLH}	Any B port	Any A port	2	9	2	7.5	ns
t_{PHL}			3	10.5	3	9	
t_{PLH}	S0, S1, S2	Any A or B port	3	11.5	3	10	ns
t_{PHL}			2	9.5	2	8	
t_{PLH}	CLK	Any A or B port	2	11	2	9	ns
t_{PHL}			3	13	3	11.5	
t_{PLH}	CLK	Q8	2	10.5	2	8	ns
t_{PHL}			3	10	3	8.5	
t_{PHZ}	S0, S1, S2	Any A or B port	2	7.5	2	6.5	ns
t_{PLZ}			3	13	3	10.5	
t_{PZH}			2	9	2	7	ns
t_{PZL}			3	11.5	3	9.5	

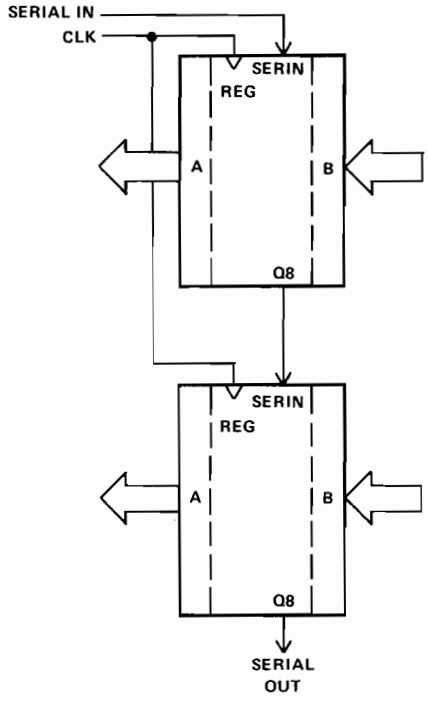
NOTE 1: For load circuit and voltage waveforms, see page 1-12.

TYPICAL APPLICATION DATA

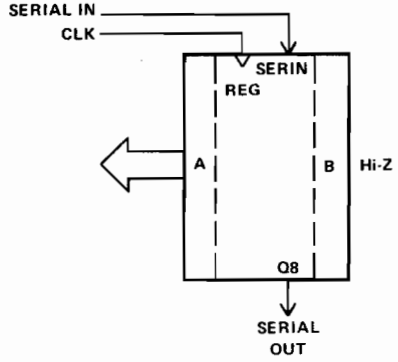
BUS A TO BUS B OR
SERIAL TRANSMISSION



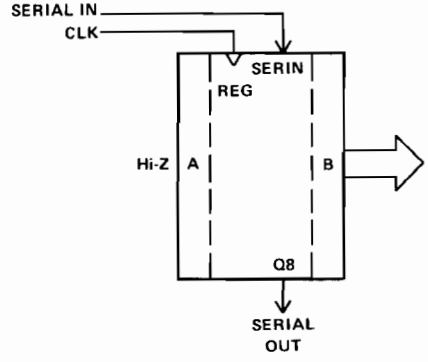
BUS B TO BUS A OR
SERIAL TRANSMISSION



SERIAL IN TO A PORT



SERIAL IN TO B PORT



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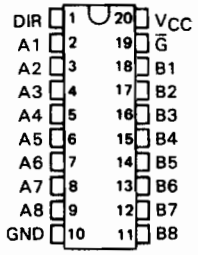
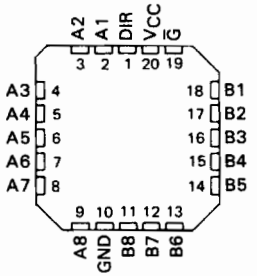
D2661, DECEMBER 1982—REVISED FEBRUARY 1984

- **'Bidirectional Bus Transceivers in High-Density 20-Pin Packages**
- **Lower-Power Version of 'ALS245A**
- **'ALS1245A is Identical to 'ALS1645A**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54ALS1245A . . . J PACKAGE
SN74ALS1245A . . . N PACKAGE



SN54ALS1245A . . . FH PACKAGE
SN74ALS1245A . . . FN PACKAGE



description

This octal bus transceiver is designed for asynchronous two-way communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input (G) can be used to disable the device so the buses are effectively isolated.

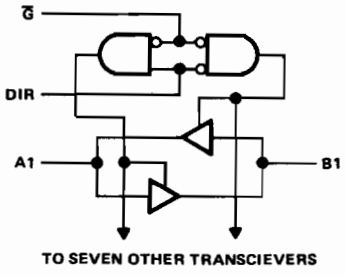
The -1 version of the SN74ALS1245A is identical to the standard versions except that the recommended maximum I_{OL} is increased to 24 milliamperes. There is no -1 version of the SN54ALS1245A.

The SN54ALS1245A is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ALS1245A is characterized for operation from 0°C to 70°C.

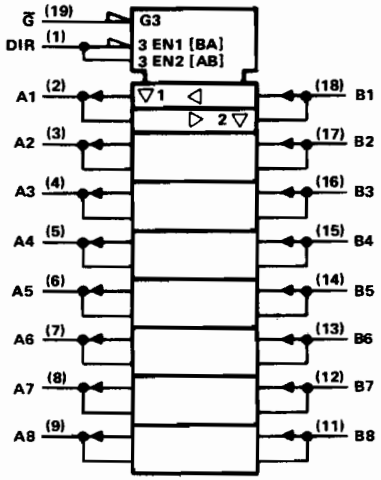
FUNCTION TABLE

CONTROL INPUTS		OPERATION
$\overline{G}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

logic diagram (positive logic)



logic symbol



Pin numbers shown are for J and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage: All inputs . . . . . 7 V
I/O ports . . . . . 5.5 V
Operating free-air temperature range: SN54ALS1245A . . . . . −55°C to 125°C
SN74ALS1245A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54ALS1245A			SN74ALS1245A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			8			16	mA
							24†	
T_A	Operating free-air temperature	−55		125	0		70	°C

†The extended limit applies only if V_{CC} is maintained between 4.75 V and 5.25 V.
The 24-mA limit applies for the SN74ALS1245A-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS1245A			SN74ALS1245A			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −0.4 mA	V_{CC} − 2			V_{CC} − 2			V
		V_{CC} = 4.5 V,	I_{OH} = −3 mA	2.4	3.2		2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −12 mA	2						
		V_{CC} = 4.5 V,	I_{OH} = −15 mA				2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 8 mA		0.25	0.4		0.25	0.4	V
		V_{CC} = 4.5 V, (I_{OL} = 24 mA for −1 version)	I_{OL} = 16 mA					0.35	0.5	
I_I	Control inputs	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
	A, B ports§	V_{CC} = 5.5 V,	V_I = 5.5 V			0.1			0.1	
I_{IH}	Control inputs	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
	A, B ports§					20			20	
I_{IL}	Control inputs	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.1			−0.1	mA
	A, B ports§					−0.1			−0.1	
I_O¶		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}		V_{CC} = 5.5 V	Output high		21	33		21	30	mA
			Output low		23	36		23	33	
			Output disabled		25	40		25	36	

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.
¶The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54ALS1245A		SN74ALS1245A		
			MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	2	15	2	13	ns
t_{PHL}			2	15	2	13	
t_{PZH}	$\overline{G}$	A or B	8	28	8	25	ns
t_{PZL}			8	28	8	25	
t_{PHZ}	$\overline{G}$	A or B	2	14	2	12	ns
t_{PLZ}			3	22	3	18	

NOTE 1: For load circuit and voltage waveforms, see page 1-12 of the TTL Data Book, Volume 3.

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General Information 1

ALS and AS Circuits 2

Applications 3

Advanced Schottky Family (ALS/AS) Application

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INTRODUCTION

The purpose of this Application Report is to assist the designers of high-performance digital logic systems in the use of the new series of Advanced Schottky-clamped* TTL integrated circuits.

Detailed electrical characteristics of these devices are provided and, if available, tables have been included that compare specific parameters of the devices with those of other logic families. In addition, interfamily information is provided to allow system designers to mix logic families in the same circuit. This allows the designer to use the relative merits of each logic family in high preformance state-of-the-art designs.

The major subject areas covered in this Application Report are as follows:

- Advanced Schottky process
- Fanouts
- Transfer characteristics
- Input and output parameters
- Speed and power information
- Noise margins
- Power supply considerations
- Noise sources and their abatement
- Back panel and printed circuit wiring guidelines
- Line driving and receiving

INTRODUCTION TO ADVANCED SCHOTTKY-CLAMPED TTL

Series 54/74 transistor-transistor logic (TTL) has, since its introduction in 1965, become the most popular digital integrated circuit logic family ever offered. Its popularity has allowed the development of high-volume production techniques which have made it the most economical approach to the implementation of major portions of medium-to-high performance digital logic systems. These systems range from simple decision making to highly complex real-time computer installations that handle worldwide data processing.

The proliferation of and economical impact of these digital logic systems has created a demand for constant improvement in efficiency. In response to demand, Texas Instruments examined the advantages gained by Schottky clamping. An increase in speed and performance was discovered in the use of Schottky barrier-diode clamping. The process was patented in the United States and the Schottky series 54S/74S catalog parts were made available in the early 1970s. A series 54LS/74LS was introduced later. The series 54LS/74LS was slower that the 54S/74S series but had a much lower power consumption.

*Integrated Schottky-Barrier-diode-clamped transistor is patented by Texas Instruments Incorporated, U.S. Patent Number 3,463,975.

Recent innovations in integrated circuit design have made it possible to develop two new families: the Advanced Schottky (54AS/74AS) series and the Advanced Low-Power Schottky (54ALS/74ALS) series. The 'ALS and 'AS series provide considerable higher speeds than the 'LS and 'S series, respectively. The 'ALS series offers a substantial reduction in power consumption over the 'LS series, and the 'AS series offers a substantial reduction in power consumption over the 'S series. The 'ALS/'AS series is pin-to-pin compatible with the 'LS/'S series.

SPEED-POWER SLOTS FILLED BY 'ALS AND 'AS TTL

Digital integrated circuits have historically been characterized for both speed and power. The series 54S/74S devices contain 19 mW NAND gates and 125-MHz flip-flops and the series 54LS/74LS devices contain 2-mW NAND gates and 45-MHz flip-flops. Either of these logic families could be used to design a 2-MHz system, therefore categorization strictly on the basis of power and speed is inconclusive with respect to system efficiency. To provide a means of measuring the overall circuit efficiency and performance, a speed-power product efficiency index for integrated circuits was developed. The rating of an integrated circuit is obtained by multiplying the gate propagation delay by the gate power dissipation.

Table I provides propagation delay times, power dissipation, and speed-power product for the Texas Instruments TTL series. In addition, it provides flip-flop frequency for each family as an indicator of system performance. The speed-power product rating system (measured in picojoules) is divided into circuits where speed is the prime factor and circuits where low-power is the prime factor. The 'ALS series speed-power product is approximately 4 times less than that of the 'LS series and the 'AS series speed-power product is approximately 4 times less than the 'S series. Figure 1 is a graphic analysis of the speed-power points for the various TTL families.

ADDITIONAL ADVANTAGES OFFERED BY 'ALS AND 'AS DEVICES

The 'ALS and 'AS devices offer the following additional advantages:

1. TTL compatible with 54/74, 54S/74S, 54L/74L, 54LS/74LS, and 54H/74H series gates for selectively upgrading existing systems
2. Suppresses the effects of line ringing and significantly reduces undershoot
3. Higher thresholds (noise immunity) and better stability across operating free-air temperature range
4. Input current requirement reduced by up to 50%

Table I. Typical Performance Characteristics by TTL Series

CIRCUIT TECHNOLOGY	MINIMIZING POWER					MINIMIZING DELAY TIME				
	FAMILY	PROP DELAY (ns)	PWR DISS (mW)	SPD/PWR PRODUCT (pJ)	MAXIMUM FLIP-FLOP FREQ (MHz)	FAMILY	PROP DELAY (ns)	PWR DISS (mW)	SPD/PWR PRODUCT (pJ)	MAXIMUM FLIP-FLOP FREQ (MHz)
Gold Doped	TTL	10	10	100	35	TTL	10	10	100	35
	L TTL	33	1	33	3	H TTL	6	22	132	50
Schottky Clamped	LS TTL	9	2	18	45	S TTL	3	19	57	125
	'ALS	4	1.2	4.8	70	'AS	1.7	8	13.6	200

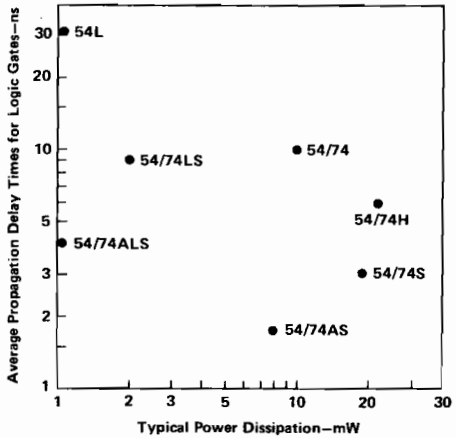


Figure 1. Speed-Power Relationships of Digital Integrated Circuits

5. Fanout is doubled
6. Terminated lines or controlled impedance circuit boards are normally not required.
7. The 'AS series offers shorter propagation delays and higher clock frequencies with relatively low power consumption.
8. The maximum flip-flop frequency has been increased to 200 MHz.

CONCEPTS OF DEFINING SERIES 'AS AND 'ALS

Both the 'ALS and 'AS series are electrically and pinout compatible with existing TTL series. The 'ALS series is suitable for replacing all TTL families except in the very highest frequency applications. Replacement with 'ALS will result in lower power consumption, smaller power supply current spikes, and, in some cases, better noise immunity than the other families. In those cases where a very high operating frequency is required, the 'AS series can be used. The 'AS devices require less than one-half of the supply current of the 'S series and has approximately twice the clocking frequency. The 'ALS devices are ideal for improving effeciency at the lower speeds. The 'AS devices are ideal for replacement of high-speed logic families including ECL 10K series.

Compatibility With Other TTL Families

To ensure complete electrical compatibility in systems using or intending to use a mixture of existing TTL families and the new 'ALS/'AS families, specific guidelines have been implemented. These guidelines ensure the continuation of desirable characteristics and incorporate newer techniques to improve performance and/or simplify the use of TTL families. Figure 2 illustrates the comparison of essential parameters of each family and shows that complete compatibility is maintained throughout the 54/74 families.

Fanout

The compatible ratings for fanout simplify the implementation of logic and provide a freedom of choice in the use of any of the seven performance ranges to design a digital logic system. Any of the Texas Instruments TTL series gates can be used to drive any other gate without the use of an interface or level-shifting circuit. The use of totem-pole-(push-pull) type output stages provides a low output impedance and the capability for both sourcing and sinking current. The output is easily adapted for driving MOS and CMOS circuits as well as the interface circuits between the output and the devices it controls. Figure 3 illustrates fanout capability.

USING THE SCHOTTKY BARRIER DIODE

The Advanced Schottky Family has been developed from two earlier concepts: the Baker Clamp and the Schottky Barrier-Diode (SBD). The use of the Baker Clamp and SBD concepts resulted in the Schottky Clamped Transistor. The Schottky clamped transistor produced the increased switching speed associated with the S series integrated circuits. The additional advances that have led to the development of 'ALS and 'AS gates and the actual gates are discussed later.

Analysis of the Schottky Clamped Transistor

The use of the Baker Clamp, shown in Figure 4, is a method of avoiding saturation of a discrete transistor. The diode forward voltage is 0.3 V to 0.4 V as compared to 0.7 V for the base-emitter junction diode. When the transistor is turned on, base current drives the transistor toward

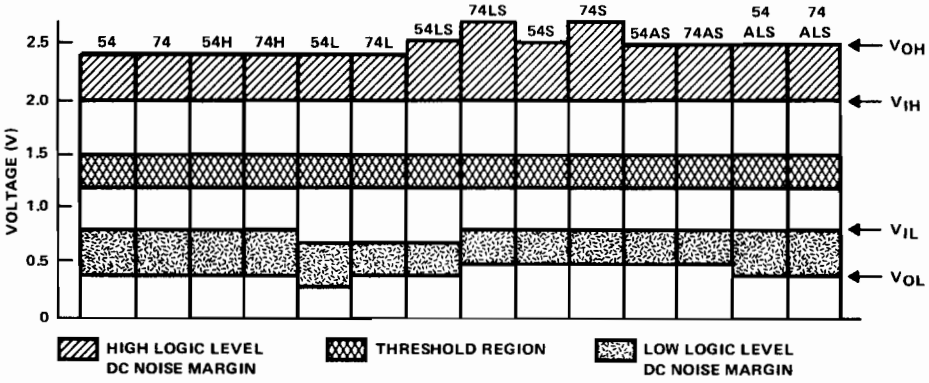


Figure 2. Series 54/74 TTL Family Compatible Levels Showing DC Noise Margins

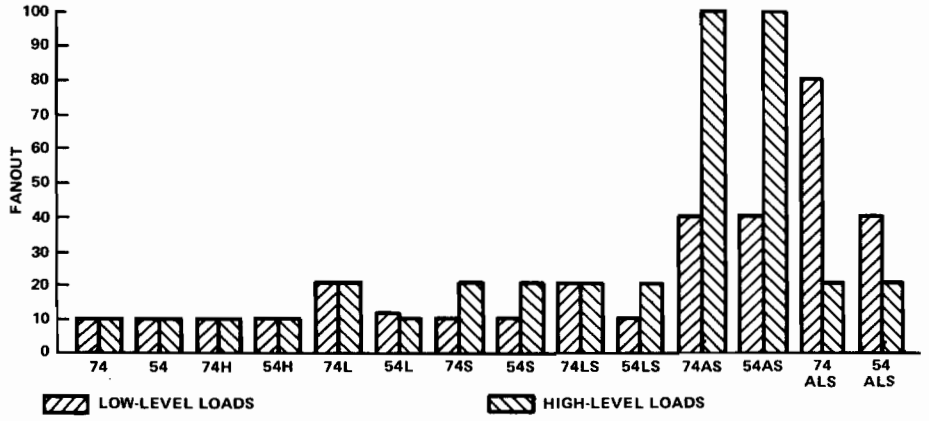


Figure 3. Fanout Capability

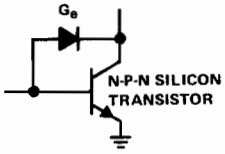


Figure 4. Baker Clamp

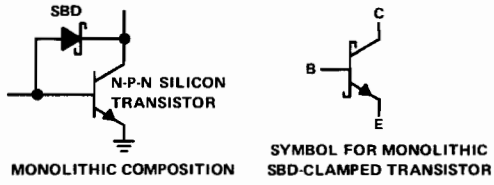


Figure 5. The Schottky-Clamped Transistor

saturation. The collector voltage drops, the germanium diode begins to conduct forward current, and excess base drive is diverted from the base-collector junction of the transistor. This causes the transistor to be held out of deep saturation, the excess base charge to not be stored, and the turn-off time to be dramatically reduced.

A germanium diode cannot be incorporated into a monolithic silicon integrated circuit. Therefore, the germanium diode must be replaced with a silicon diode which has a lower forward voltage drop than the base-collector junction of the transistor. A normal p-n diode will not meet this requirement. The SBD illustrated in Figure 5 can be used to meet the requirement.

The SBD illustrated in Figure 6 is a rectifying metal-semiconductor contact formed between a metal and a highly doped N semiconductor.

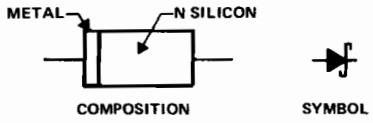


Figure 6. Schottky Barrier-Diode

The qualitative physics of an SBD is illustrated in Figure 7. The valence and conduction bands in a metal overlap make available a large number of free-energy states. The free-energy states can be filled by any electrons which are injected into the conduction band. A finite number of electrons exist in the conduction band of a semiconductor. The number of electrons depends mainly upon the thermal energy and the level of impurity atoms in the material. When a metal-semiconductor junction is formed, free electrons flow across the junction from the semiconductor, via the conduction band, and fill the free-energy states in the metal. This flow of electrons builds a depletion potential across the barrier. This depletion potential opposes the electron flow and, eventually, is sufficient to sustain a balance where there is no net electron flow across the barrier.

Under forward bias (metal positive), there are many electrons with enough thermal energy to cross the barrier potential into the metal. This forward bias is called "hot injection." Because the barrier width is decreased as forward bias V_F increases, forward current will increase rapidly with an increase in V_F.

When the SBD is reverse biased, electrons in the semiconductor require greater energy to cross the barrier. However, electrons in the metal see a barrier potential from the side essentially independent of the bias voltage and a small net reverse current will flow. Since this current flow is relatively independent of the applied reverse bias, the reverse current flow will not increase significantly until avalanche breakdown occurs.

A simple metal-n semiconductor collector contact is an ohmic contact while the SBD contact is a rectifying contact. The difference is controlled by the level of doping in the semiconductor material. As the doping is increased, the contact becomes more ohmic. Figure 8 illustrates the current-voltage characteristics according the doping applied.

Current in the SBD is carried by majority carriers. Current in the p-n junction is carried by minority carriers. The resultant minority carrier storage causes the switching

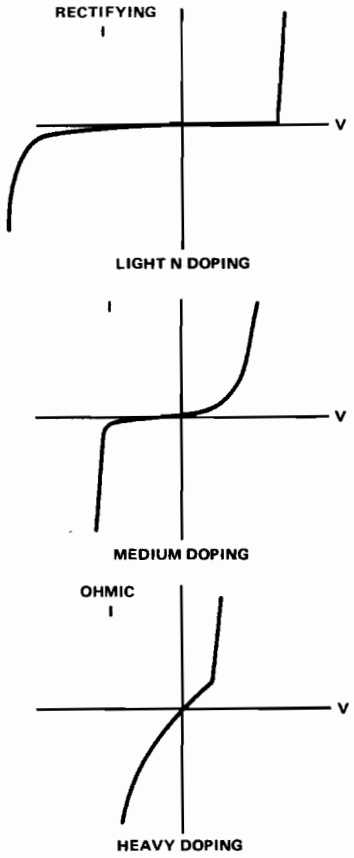


Figure 8. Metal-N Diode Current-Voltage Characteristics

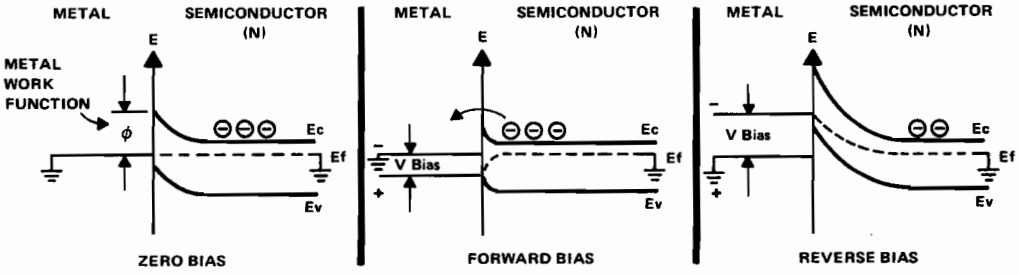


Figure 7. Schottky Barrier-Diode Energy Diagrams

time of a p-n junction to be limited when switched from forward bias to reverse bias. A p-n junction is inherently slower than an SBD even when doped with gold.

Another major difference between the SBD and p-n junction is the forward voltage drop. For diodes of the same surface area, the SBD will have a larger forward current at the same forward bias regardless of the type of metal used. The SBD forward voltage drop is lower at a given current than a p-n junction. Figure 9 illustrates the current carriers and forward current-voltage characteristics differences between the SBD and p-n junction. The SBD meets the requirements of a silicon diode which will clamp a silicon n-p-n transistor out of saturation.

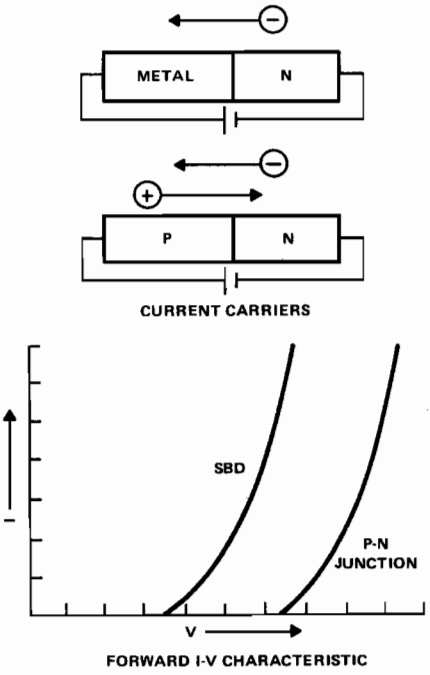


Figure 9. Differences Between P-N and Schottky Barrier-Diodes

The Advanced Schottky process differs from the Schottky process in that it uses ion implantation of impurities instead of diffusion. Ion implantation gives greater control on the depth of doping and resolution. Because of a thinner epitaxial layer and smaller all around geometries, smaller parasitic capacitances are encountered. The performance of the SBD is also enhanced by the use of oxide isolation of the transistors. This reduces the collector-substrate capacitance. Figure 10 illustrates the 'LS/'S process which consists of conventional masks, junction isolation, and a

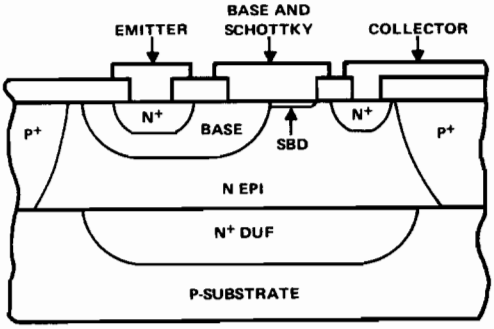


Figure 10. Standard Process ('LS/'S)

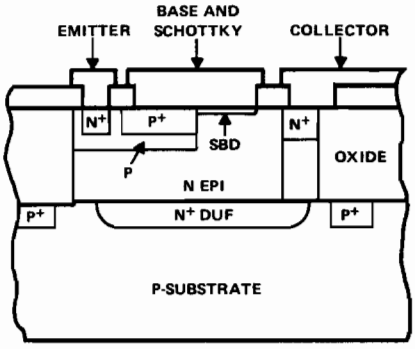


Figure 11. Advanced Process ('ALS/'AS)

standard metal system and Figure 11 illustrates the 'ALS/'AS process which consists of composed masks, ion implantation, oxide isolation, and a standard metal system.

Analysis of 'ALS and 'AS NAND Gates

The 'ALS and 'AS NAND gates in Figures 12 and 13 combine the desirable features of improved TTL circuits with the technological advantages of full Schottky clamping, ion implantation, and oxide isolation to achieve very fast switching times at a reduced speed-power product. The improvements and advantages are as follows:

1. Full Schottky clamping of all saturating transistors virtually eliminates storing excessive base charge and significantly enhances turn-off time of the transistors.
2. Elimination of transistor storage time provides stable switching times across the temperature range.
3. An active turn-off is added to square up the transfer characteristic and provide an improved high-level noise immunity.

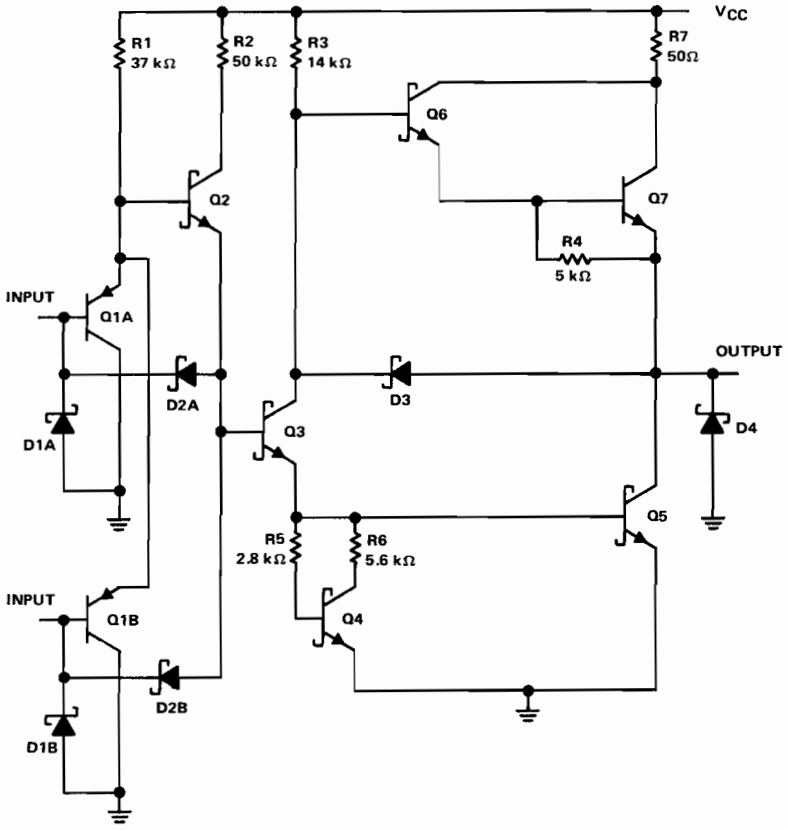


Figure 12. 'ALS00A NAND Gate Schematic

4. Input and output clamping is implemented with Schottky diodes to reduce negative-going excursions on the inputs and outputs. Because of its lower forward voltage drop and fast recovery time, the Schottky input diode provides improved clamping action over a conventional p-n junction diode.
5. The ion implantation process allows small geometries giving less parasitic capacitances so that switching times are decreased.
6. The reduction of the epi-substrate capacitance using oxide isolation also decreases switching times.

A key feature of the 'ALS and 'AS families is the improvement in typical input-threshold voltage. Figure 12 is a schematic diagram of the 'ALS00A NAND gate. Figure 13 is a schematic diagram of the 'AS00 NAND gate. The input threshold voltage of the devices is determined by the equation:

$$VT = V_{BE} \text{ of Q2} + V_{BE} \text{ of Q3} + V_{BE} \text{ of Q5} - V_{BE} \text{ of Q1A (or } V_{BE} \text{ of Q1B)} \quad (1)$$

From Eq. (1) it can be determined that the input threshold voltage is two times V_{BE} or approximately 1.4 V. Low-level input current I_{IL} is reduced in the 'ALS00A/'AS00 gates because of the improved input circuits. Buffering by transistors Q1A (or Q1B) and Q2 causes a significant reduction in low-level input current. Low-level input current is determined by the equation:

$$I_{IL} = V_{CC} - V_{BE} \text{ of Q1A} - V_I/[R(h_{FE} \text{ of Q1A} + 1)] \quad (2)$$

By using Eq. (2) low-level input current is reduced by at least the factor of h_{FE} of Q1A + 1 and is typically -10 μA for the 'ALS00A and -50 μA for the 'AS00. High-level output voltage V_{OH} is determined primarily by V_{CC},

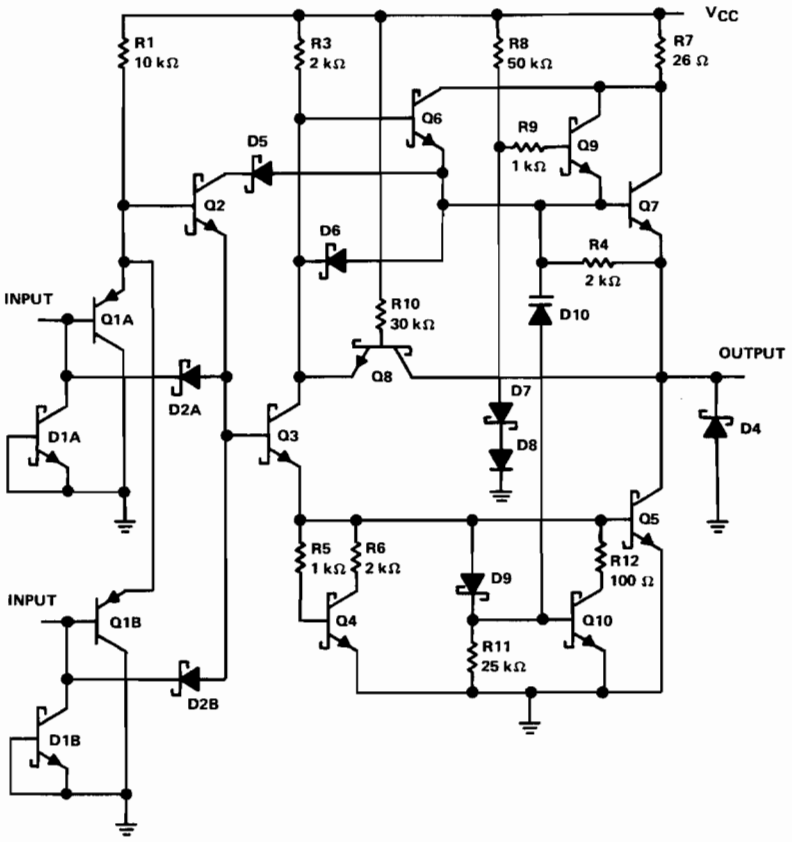


Figure 13. 'AS00 NAND Gate Schematic

resistors R4 and R7, and transistors Q6 and Q7. With no load, the high-level output voltage is approximately equal to $V_{CC} - V_{BE}$ of Q6 because the voltage across resistor R4 is 0 V. For medium-level currents, the high-level output voltage is equal to $V_{CC} - V_{BE}$ of Q6 $- V_{BE}$ of Q7 because of the Darlington gain of transistors Q6 and Q7. The current through resistor R3 is typically less than 1 μA and, therefore, the voltage drop is negligible. As conduction through transistors Q6 and Q7 is increased, the voltage drop across limiting resistor R7 will increase until the Schottky clamping diode of transistor Q6 starts to become forward biased. At this point, the current through resistor R3 (and the voltage drop) is no longer negligible and the high-level output voltage is determined by:

$$V_{OH} = V_{CC} - I_{OH \text{ through } R7} \times R7 - V_{CE} \text{ of Q6} - V_{BE} \text{ of Q7} \quad (3)$$

Low-level output voltage V_{OL} is determined by the turning on of transistor Q5. When the input is high and transistor Q2 is turned on, high-current transistor Q5 is turned on by a current path through transistor Q3 and resistor R3. Sufficient base drive is supplied to keep transistor Q5 fully turned on at an apparent output resistance of 14 Ω for 'ALS and 6Ω for 'AS.

The fanout is up to 40 for a '54ALS device that is driving a '54ALS device and up to 80 for a '74ALS device, that is driving a '74ALS device and provides a guaranteed low-level output current of 4 mA and 8 mA, respectively.

The increase in speed-power product of '54ALS/'74ALS devices, a factor four times better than '54LS/'74LS devices, is due to the design consideration of the quiescent and switching operations of the circuit. In the quiescent state, transistor Q2 allows the use of a reduced low-level input current. This reduces the fanout and reduces the overall quiescent current requirements.

The design of diodes D2 and D3 (or transistor Q8) and transistor Q4 enhances the speed-power product of the device. Transistor Q4 reduces the turn-off time and consequently the current transients caused by conduction

overlap of transistor Q5. The same principle is used by diodes D2 and D3 and transistor Q3 in turning off transistor Q7. In addition, the active turn-off design produces a square transfer characteristic.

The 'AS00 gate has additional circuits not on the 'ALS00A gate. The circuits are added to enhance the throughput of the 'AS Family.

Transistor Q10 has been added as a discharge path for the base-collector capacitance of transistor Q5. Without transistor Q10, rising voltages at the collector of transistor Q5 would force current, via the base-collector capacitance, into the base of transistor Q5 causing it to turn on. However, diode D10 causes transistor Q10 to turn on (during rising voltage) and keeps transistor Q5 turned off. Diodes D6 and D9 serve as a discharge path for capacitor-diode D10.

CIRCUIT PARAMETERS

Worst-case testing of 'ALS/'AS devices provides a margin of safety. [All dc limits shown on the data sheet are guaranteed over the entire temperature range (−55 °C to 125 °C) for series 54ALS/54AS and 0 °C to 70 °C for series 74ALS/74AS)]. In addition, the dc limits are guaranteed over the entire supply voltage range (4.5 V to 5.5 V).

Transfer Characteristics

Since the most common application for a logic gate is to drive a similar logic gate, the input and output logic levels must be compatible. The input and output logic levels for 'ALS/'AS devices are as follows:

- V_{IL} — The voltage value required for a low-level input voltage that guarantees operation
- V_{IH} — The voltage value required for a high-level input voltage that guarantees operation
- V_{OL} — The guaranteed maximum low-level output voltage of a gate
- V_{OH} — The guaranteed minimum high-level output voltage of a gate.

With the exception of high-level ouput voltage (which is a direct function of supply voltage), these values remain virtually unchanged over the temperature range and under normal operating conditions of the device.

Analysis of the input and output response characteristics of 'ALS/'AS TTL gates is necessary to understand the operation of these devices in most system applications. The dc response characteristics can best be depicted by an input voltage V_I versus output voltage V_O transfer plot.

Figure 14 plots the 'ALS/'AS characteristics as compared with members of other TTL logic families.

As shown in Figure 14, the 'ALS and 'AS devices exhibit a much better output savings when compared with standard TTL devices. The better high-level output voltage is primarily because of the active turn off of the low-level output transistor. The diode voltage drop in the normal output is replaced by a low-current V_{BE} voltage drop. This provides

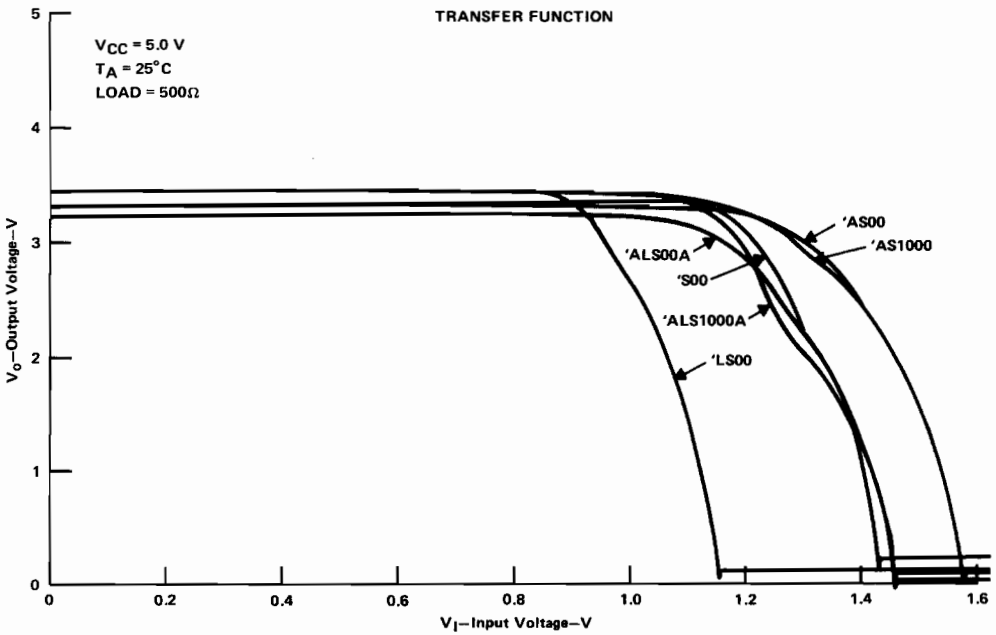


Figure 14. Input Voltage vs Output Voltage of 'ALS/'AS

a better high-level noise immunity in 'ALS and and 'AS over standard TTL devices.

Input Characteristics

To use 'ALS/'AS devices fully, a knowledge of the input and output characteristics is required. This is particularly true when a device interfaces with a device not in the same TTL series. In addition, knowledge of voltage and current relationships for all elements is important for proper design.

Figure 15 illustrates a typical plot for input current I_I versus input voltage, V_I, characteristics for 'ALS/'AS gate inputs during normal operation. A typical series 54/74 characteristic plot is also shown for reference. Any device used to drive a TTL gate must source and sink current. Conventionally, current flowing toward a device input terminal is designated as positive and current flowing out of a device input terminal is designated as negative. Low-level input current is negative current because it flows out of the input terminal. High-level input current is a positive current because it flows into the input terminal.

For transmission line conditions, a more accurate plot of the reverse bias section of these curves is required. These curves, Figure 16, are characteristic of the input clamping diode.

Low-Level Input Current

Figure 17 illustrates the dc equivalent of a standard 'ALS/'AS input circuit and shows the input current paths during a low-level input state. The low-level input current is primarily determined by resistor R1. However, low-level input current is also a function of the supply voltage, the ambient temperature, and the low-level input voltage. To

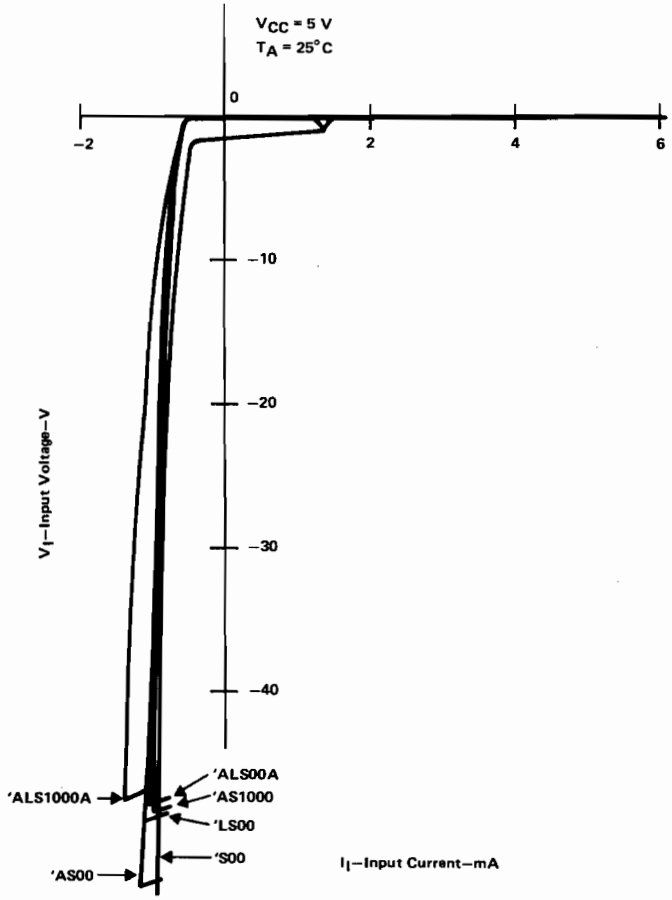


Figure 15. Input Current vs Input Voltage for TTL Families

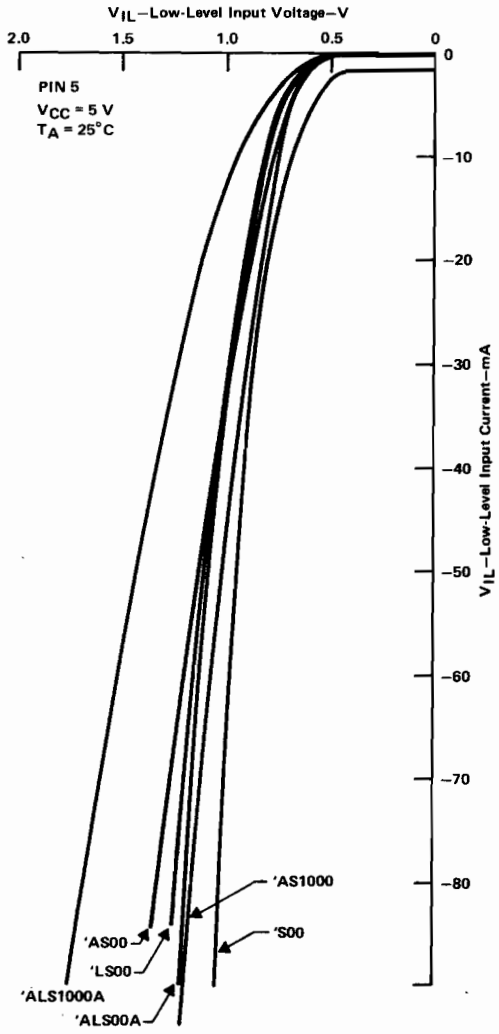


Figure 16. Low-Level Input Current vs High-Level Input Voltage for TTL Families

assure desired device operation under all possible conditions, the worst-case test is performed on all devices. Supply voltage is taken to the highest allowable value to cause the low-level input current to be at a maximum. With the exception of the input under test, all unused inputs are taken to a high level. This enhances any contribution of these inputs to the low-level input current of the emitter under test.

Input Clamping Diode Test

The quality of the input clamping SBD (D2 in Figure 17) is tested by ensuring that the forward voltage drop is not

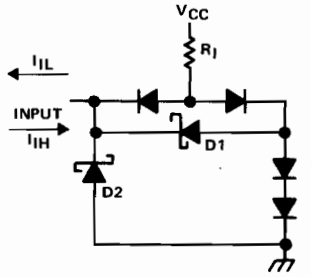


Figure 17. DC Equivalent Input Circuit for Series 'ALS Gate

greater than −1.2 V for 'AS and −1.5 V for 'ALS with a forward current of 18 mA. These values are guaranteed at minimum supply voltage and are valid across the operating temperature range. The characteristic of the input diode is illustrated in Figure 16.

High-Level Input Current

Another input parameter that must be measured and controlled is high-level input current. To ensure desired device operation under all possible conditions, the worst-case test is performed with all unused inputs grounded and supply voltage at its maximum value. This provides the highest value of low-level input current. Those devices with a high-level input current of sufficient magnitude to cause a degradation of high-level output voltage at an output must be screened out.

Input Breakdown Test

An additional high-level input current test is performed to check for base-emitter breakdown under the application of the full range of input voltages. This test is performed under the worst-case supply voltage conditions and is important because the base-emitter junction is small and can easily be overdissipated during the breakdown conditions.

Output Characteristics

The most versatile TTL output configuration is the push-pull (totem-pole) type. The totem-pole output has a low output impedance drive capability at both high and low logic levels. Both 'ALS and 'AS families use this configuration and have fanouts of 40 in both the high- and low-level states.

High-Level Output Characteristics

The ability of the totem-pole output to supply high-level output current is parametrically tested by applying a high-level input current value during measurement of high-level output voltage. However, the quality of the output stage is best indicated by parametrically measuring its current sourcing I_{OS} capability when connected to ground. Figure 18 shows the equivalent output circuit under high-level output conditions.

Figure 19 illustrates typical high-level characteristics. When measuring worst-case high-level output voltage, minimum supply voltage is used. A worst-case low-level

input voltage is applied to an input and all unused inputs are tied to supply voltage.

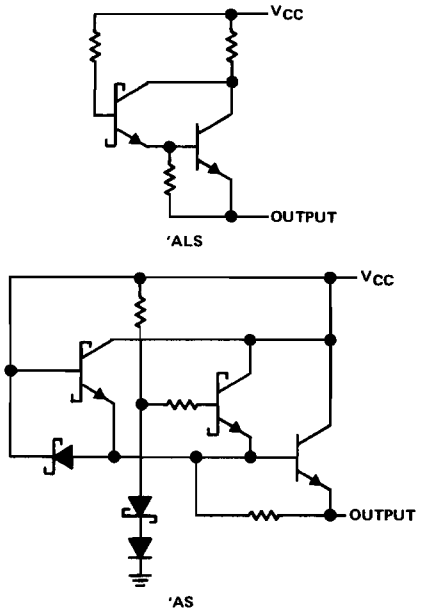


Figure 18. Equivalent Output Circuit for 'ALS/'AS Gates

Low-Level Output Characteristics

Figure 20 shows that section of the output drive circuit which produces a low-level output voltage V_{OL}. This characteristic is also tested at minimum supply voltage. Figure 21 illustrates the typical curve.

Switching Speed

Two switching-speed parameters are guaranteed on Series 'ALS and 'AS gates: propagation delay time for a high-level to a low-level at the output t_{PHL}, and a low-level to high-level transition time t_{PLH}. Both parameters are specified with respect to the input pulse using standard test conditions as follows:

V_{CC} = 4.5 V to 5.5 V
C_L = 50 pF
R_L = 500
T_A = MIN to MAX

Under these conditions, times in the order of 4 ns for 'ALS and 1.7 ns for 'AS are typical. Figures 22 and 23 illustrate how the propagation delay time for 'ALS and 'AS devices vary with load capacitance.

Most current in the output stage is drawn when both output transistors are on (i.e., during output transitions, the average power dissipation of a gate with a totem-pole output increases with operating frequency). This is caused by more high-current transitions per second at the output as the frequency increases. Figure 24 illustrates the effect for both 'ALS and 'AS devices.

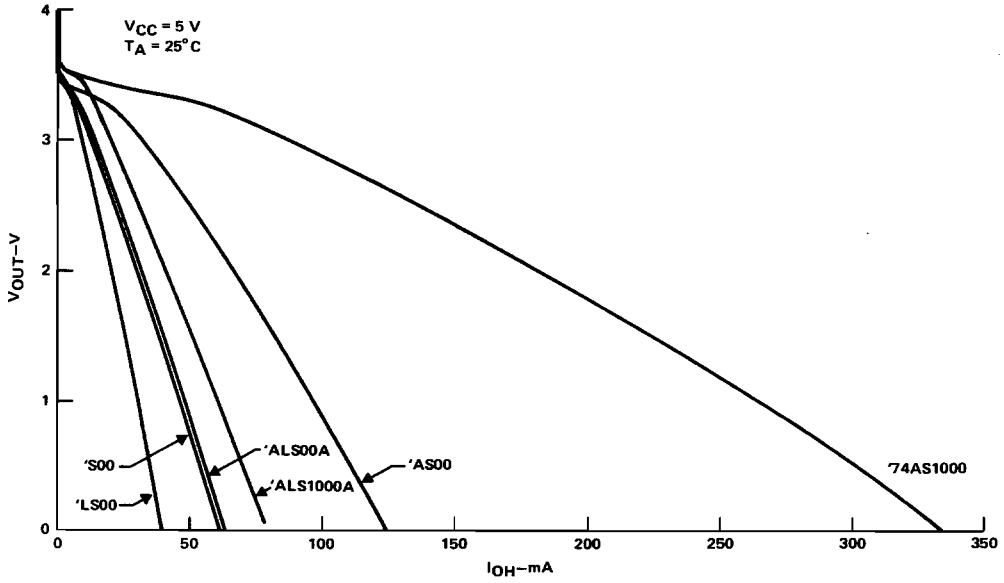


Figure 19. High-Level Output Voltage vs High-Level Output Current

DC Noise Margins

Noise margin is a voltage specification which guarantees the static dc immunity of a circuit to adverse operating conditions. Noise margin is defined as the difference between the worst-case input logic level (V_{IH} minimum or V_{IL} maximum) and the guaranteed worst-case output (V_{OH} minimum or V_{OL} maximum) specified to drive the inputs. Table II lists the worst-case output limits for the 'AS and 'ALS families.

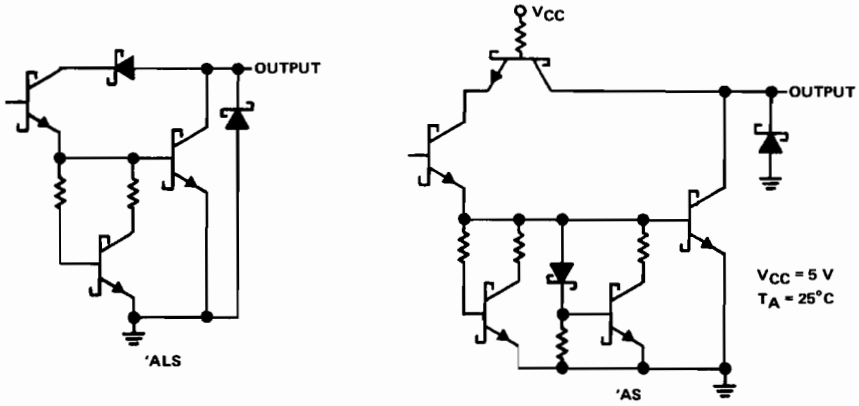


Figure 20. Low-Level Output Circuit for 'ALS/'AS Gates

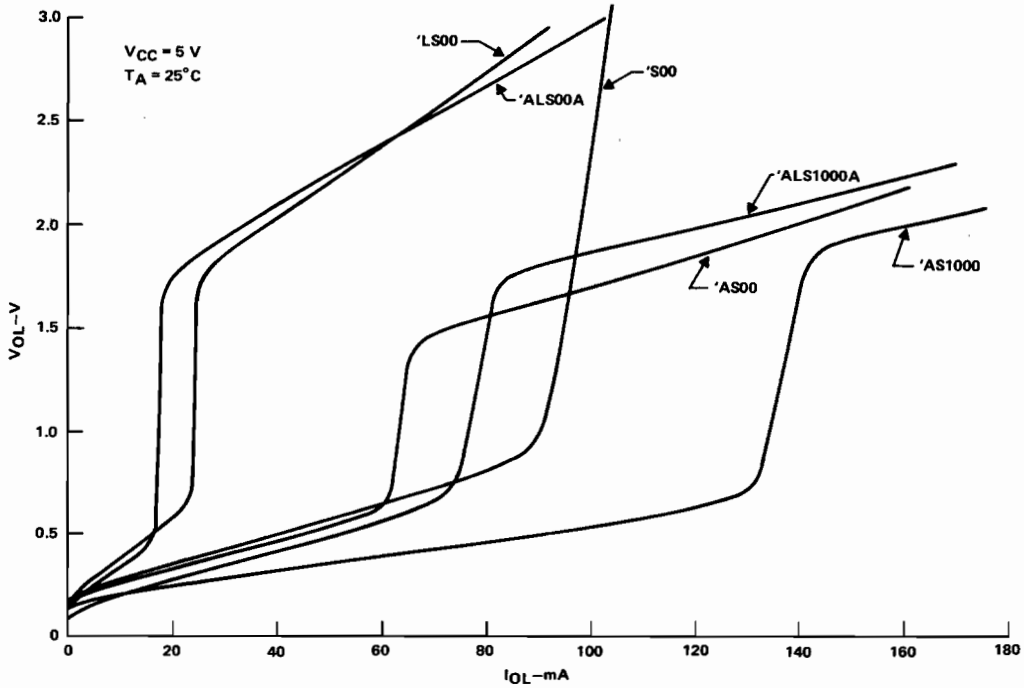


Figure 21. Low-Level Output Voltage vs Low-Level Output Current

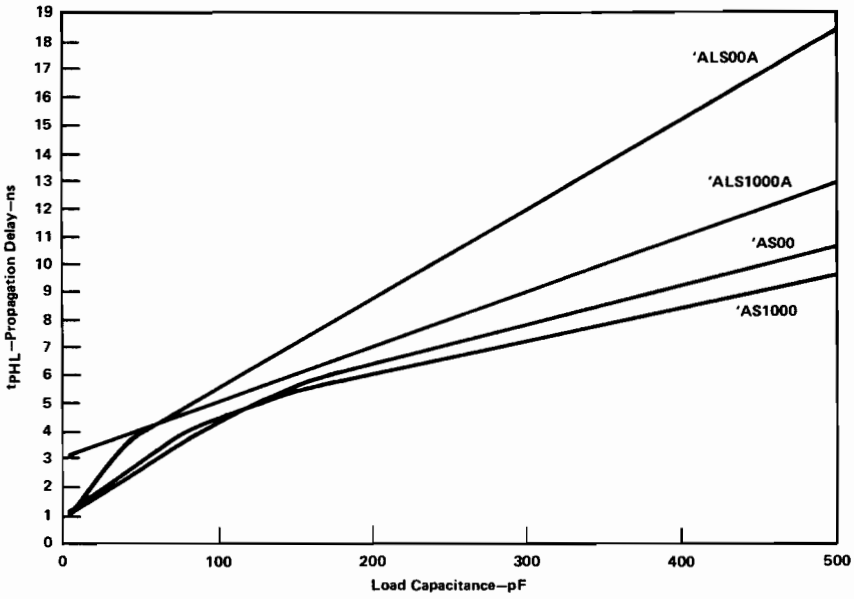


Figure 22. High- to Low-Level Propagation Delay vs Load Capacitance

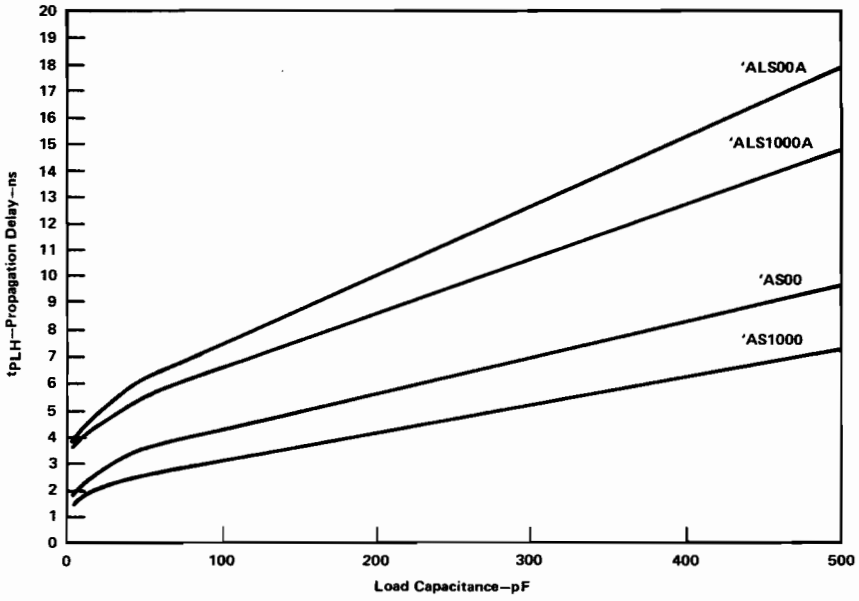


Figure 23. Low- to High-Level Propagation Delay vs Load Capacitance

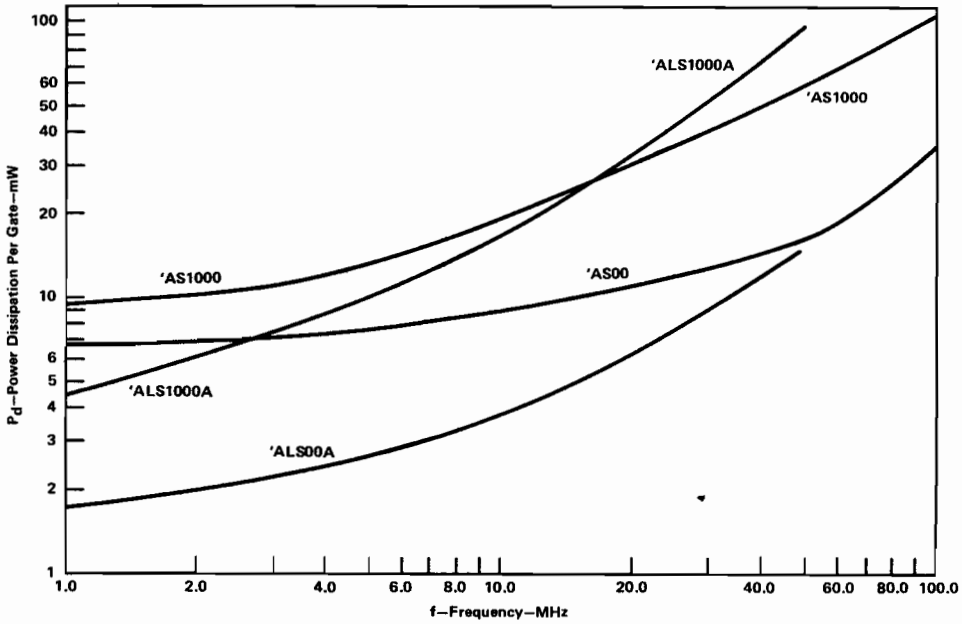


Figure 24. Power Dissipation per Gate vs Frequency

Specified Logic Levels and Thresholds

The high-level noise margin is obtained by subtracting V_{IH} minimum from V_{OH} minimum. The low-level noise margin is obtained by subtracting V_{IL} maximum from V_{OL} maximum. The worst-case high-level noise margin is guaranteed to be at least 500 mV for both 'AS and 'ALS devices and at least 300 mV for low-level noise immunity across the operating free-air temperature ranges.

The usefulness of noise margins at the system design level is the ability of a device to be impervious to noise spikes at the input. The input voltage falls into one of three categories: low-logic state (between ground and 0.8 V), threshold region (between 0.8 V and 2 V), or high-logic state (between 2 V and V_{CC}). If an input voltage remains exclusively in the low-logic or high-logic state, it can undergo any excursions within that state. A level change from 5.5 V to 2 V or from ground to 0.8 V should not affect the output state of the device. To guarantee an expected output level change, the appropriate input has to undergo a change from one input state to the other input state (i.e., a transition through the threshold region). If a device will not remain in the correct state when voltage excursions on the input are occurring, it is violating its truth table.

Noise Rejection

The ability of a logic element to operate in a noise environment involves more than the dc or ac noise margins previously discussed. To present a problem, an externally generated noise pulse must be received into the system and cause a malfunction. Stable logic systems with no storage

Table II. Worst Case Output Parameters

PARAMETER (V)	'AS (0°C to 70°C)	'ALS (0°C to 70°C)	'AS (−55°C to 125°C)	'ALS (−55°C to 125°C)
V_{IH}(MIN)	2	2	2	2
V_{IL}(MAX)	0.8	0.8	0.8	0.8
V_{OH}(MIN) @ $_{CC}$ = 4.5 V*	2.5	2.5	2.5	2.5
V_{OL}(MAX)	0.5	0.5	0.5	0.4
High Level Noise Margin ($V_{OH}-V_{IH}$)	0.5	0.5	0.5	0.5
Low Level Noise Margin ($V_{IL}-V_{OL}$)	0.3	0.3	0.3	0.4

*Actual specification for $V_{OH(min)}$ is V_{CC} − 2 V.

elements are practically impervious to ac noise. However, large dc voltages could cause noise problems. Systems with triggerable storage elements or those operating fast enough for the noise to appear as a signal are much more susceptible to noise.

The noise voltage must be radiated or coupled into the circuit. The amount of noise required to develop a given voltage is a function of the circuit impedance. Because of the low output impedance of TTL circuits, noise immunity is improved. Noise is transferred from the source (with some arbitrary impedance) through a coupling impedance to the impedance of the circuit under consideration.

Figure 25 shows a circuit where the coupling impedance is stray capacitance and the load impedance is provided by the gates. The relatively tight coupling of this circuit and the loading effect on the driving source is significant enough

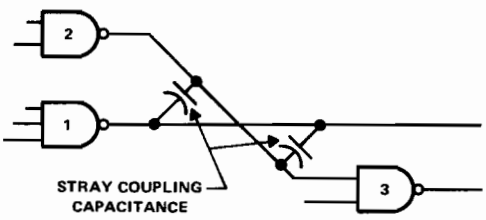


Figure 25. Stray Coupling Capacitance

to be considered. However, since the source effect is difficult to assess and is in a direction to improve rather than degrade the noise rejection, its effects are ignored. This results in a worst-case type of response indication. In the case of radiated noise, the source resistance is a definite factor in noise coupling and essentially replaces the reactive coupling impedance.

By ignoring the driving source impedance to make conditions more nearly standard, it is possible to determine a set of curves relating the developed noise pulse to the noise source amplitude, the noise rise or fall time, the coupling impedance, and the load impedance. Curves have been developed[1] for several different input waveforms. Since the 'ALS waveform is essentially a ramp with a dv/vt of 1 V/ns (approximately 2.5 V/ns for 'AS), the most applicable curve is that for a ramp input.

Figure 26(a) shows the equivalent circuit from which the ramp response plot in Figure 26(b) was developed. The input pulse (shown as a heavy line) is a step signal with a liner rise requiring unit time (normalized). The output pulse is represented analytically by

$$e_0 = \tau(1 - e^{-t/\tau})$$
$$\tau = RC$$

with holding for unit time. This is followed by an exponentially decaying voltage with a time constant τ. Values of τ and i on the figure are normalized by the value of the total rise time of the stimulated noise pulse e_i. Using Figure 26(b), the pulse width and amplitude of the coupled noise pulse can be estimated.

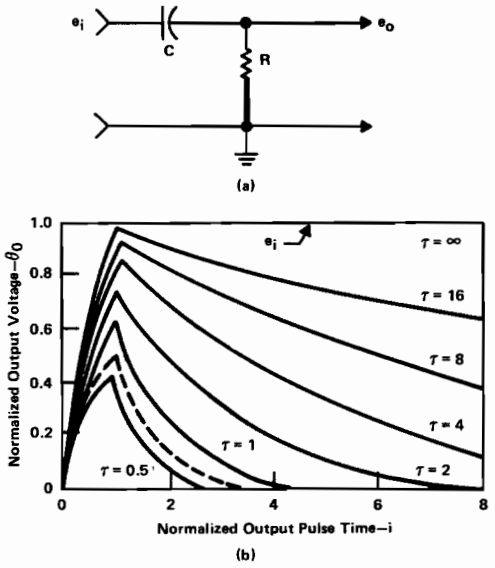


Figure 26. Evaluations of Gate Response to Fast Input Pulses

As an example, using the circuit shown in Figure 25, apply a noise pulse of 3 V in amplitude and rising at 1 V/ns with gate 2 at a high-logic state. Assume a nominal output impedance of 58 Ω (30 Ω for 'AS) and coupling capacitance of 10 pF. Use the following formula:

$$\tau = RC = (10 \times 10^{-12})(58)$$
$$= 0.58 \times 10^{-9} = 0.58 \text{ ns}$$

$$\text{Total rise time} = \frac{3 \text{ V}}{1 \text{ V/ns}^{**}} = 3 \text{ ns}^{\dagger}$$

**2.5 V/ns for 'AS

†1.2 ns for 'AS

To convert the normalized values of τ and i in Figure 26(b) to actual values, multiply by 3 ns. The output voltage scale will be multiplied by 3 V. Using the $\tau = 0.58$ curve gives a peak e_0 of 1.5 V (0.5 × 3) and a pulse width of 3 ns at the 50% points. To determine whether this pulse will cause interference, enter these values (1.5 V and 3 ns) on the graph shown in Figure 27. Since the gates have approximately 1.8 V of noise immunity at this point, they should not be affected.

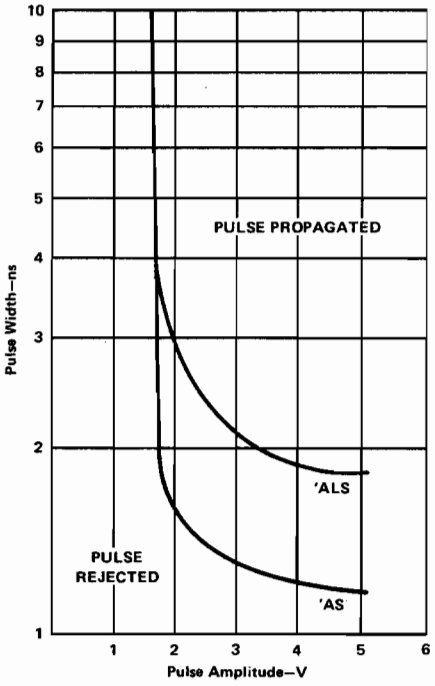


Figure 27. Theoretical Required Pulse Width vs Pulse Amplitude for 'AS and 'ALS Inputs

If an open-collector gate is used with a passive 1 kΩ pull-up resistor, the situation would change. Use the following formula:

$$\tau = (10 \times 10^{-12})(1 \times 10^{3}) = 10 \times 10^{-9} = 10 \text{ ns}$$

$$\text{Total rise time} = \frac{3 \text{ V}}{1 \text{ V/ns}^{**}} = 3 \text{ ns}^{\dagger}$$

**2.5 V/ns for 'AS

†1.2 ns for 'AS

Now the amplitude (from the curves) approaches 3 V (0.96 × 3) and the pulse width at the 50% points is approximately 10 ns (1 × 10). The next gate will propagate this pulse.

This example is an oversimplification. The coupling impedances are complex (but resolvable into RLC series coupling elements) and the gate output impedance changes with load. Our purpose is to show why and how the low impedance of the active TTL output rejects noise and to make a comparison with a passive pull-up.

The ability to operate in a noisy environment is an interaction of the built-in operating margins, the time required for the device to react, and the ease with which a noise voltage is developed. In all cases, except the ability to react to short noise pulses, the TTL design has emhasized noise rejection.

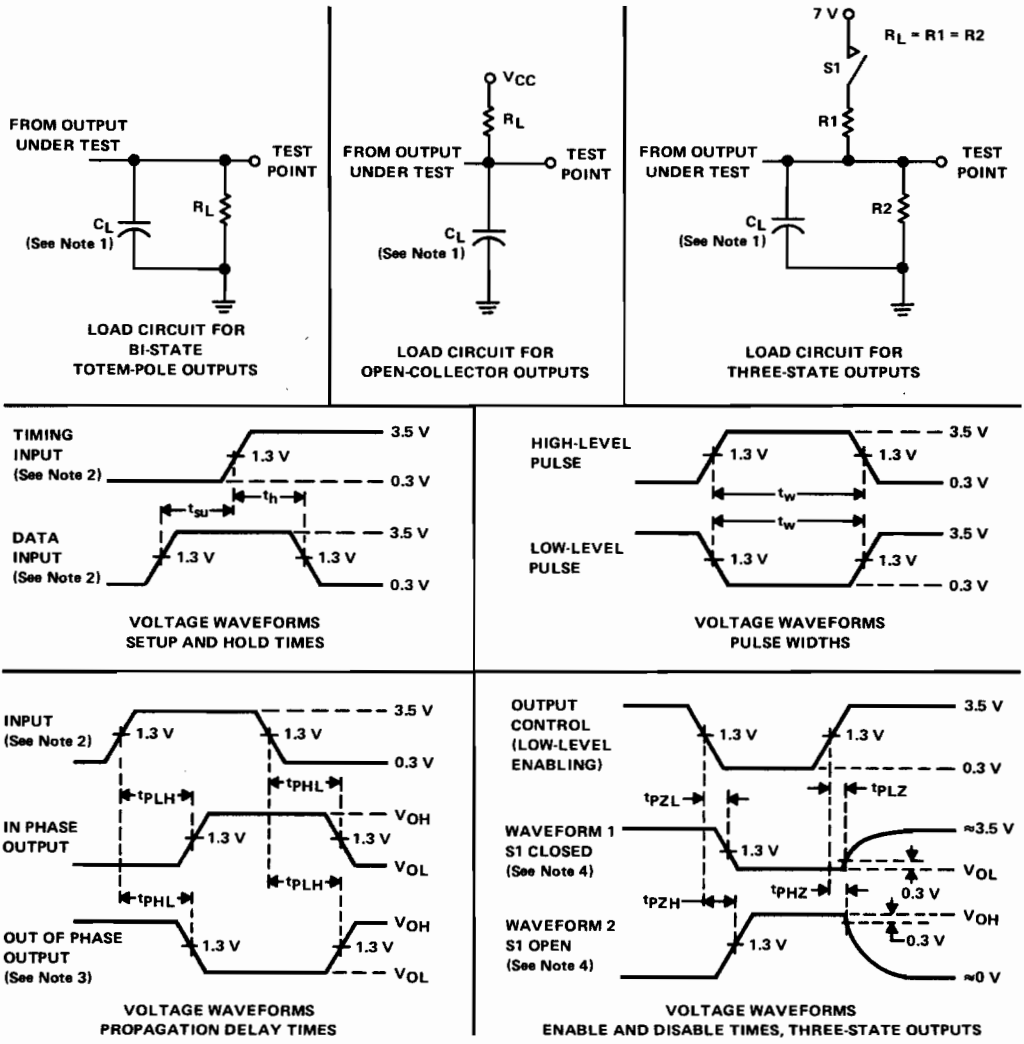
Nothing has been discussed concerning noise in devices other than gate circuits. Many MSI devices are complex gate networks and, because of their small size, are more superior

Table III. Guidelines for Systems Design for Advanced Schottky TTL

ITEM	GUIDELINE
Single wire connections	Wire lengths up to approximately 12 inches may be used. A form of ground plane is desirable. Use point-to-point routing rather than parallel. If the wire is longer than 12 inches, use either a dense ground plane with the wire routed as close to it as possible, or use a twisted-pair cable.
Coaxial and twisted-pair cables	Design around approximately 80 Ω to 100 Ω of characteristic impedance. Cross talk increases at higher impedances. Use a coaxial cable of 93 Ω impedance (e.g., Microdot 293—3913). For twisted-pair cable, use number 26 or number 28 wire with the insulation twisted at the rate of 30 turns per foot.
Transmission-line-ground	Ensure that transmission-line ground returns are carried through at both transmitting and receiving ends. V_{CC} decoupling ground, device ground, and transmission-line ground should have a common tie point.
Cross talk	Use point-to-point back-panel wiring to minimize noise pickup between lines. Avoid long unshielded parallel runs. However, if they must be used, they should carry signals that propagate in the same direction.
Reflections	Reflections occur when data interconnects become long enough that 2-line propagation delays are pulse transition times. For series TTL, reflections are normally of no importance for lines shorter than 12 inches.
Resistive pull-up	If fanout of driving output permits, use approximately 300 Ω of resistive pull-up at the receiving end of long cables. This provides added noise margin and more rapid rise times.

in a noisy environment operation than their discrete gate equivalents. Noise tolerance of latching devices is implied in the setup times, hold times, clock pulse width, data pulse widths, and similar parameters. Output impedances and input noise margins are quite similar to those of the gates and may be treated in a similar manner. If a latching device does become noise triggered, the effective error is stored and does not disappear with the noise.

Parameter measurement information is shown in Figure 28.



NOTES: 1. C_L includes probe and jig capacitance.
2. All input pulses have the following characteristics PRR ≤ 1 MHz, $t_r = t_f$ = 2 ns, duty cycle = 50%.
3. When measuring propagation delay times of 3-state outputs, switch S1 is open.
4. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

Figure 28. Parameter Measurement Information

GUIDELINES FOR SERIES 'ALS/'AS TTL SYSTEM DESIGN

System layout and design requirements for Advanced Schottky TTL circuits are essentially the same as those guidelines which have previously been established and are applicable for all high-performance digital systems. Tables III through VI provide a brief summary of the solutions to most design decisions needed to implement systems using Advanced Schottky TTL. Supplementary data which may be useful for developing specific answers to unique problems is provided later.

POWER SUPPLY REGULATION

Power supply regulation cannot be treated as if it is an independent characteristic of the device involved. Power supply regulation, along with temperature range, affects noise margins, fanout, switching-speed, and several other parameters. The characteristics most affected are noise margin and fanout. When these two parameters are within the specified limits, the power-supply regulation will normally be within specified limits. However, on a device where auxiliary parameters are more critically specified, a more restrictive power-supply regulation is normally required. When power-supply regulation is slightly outside the specified limits for TTL devices, the device may still operate satisfactorily. However, if high ambient-noise levels and extreme temperatures are encountered, failures may occur.

Application of a supply voltage above 7 V (absolute maximum rating) will result in damage to the circuit.

Since power dissipation in the package is directly related to supply voltage, the maximum recommended supply voltage for TTL devices is specified at 5.5 V. This provides an adequate margin to ensure that functional capability and long-term reliability are not jeopardized.

High-level output voltage is almost directly proportional to supply voltage (i.e., a drop in supply voltage causes a drop in high-level output voltage and an increase in supply voltage results in an increase in high-level output voltage). Because of this relationship, high-level output voltage for 'ALS/'AS devices is specified as supply voltage -2 V (V_{CC} -2 V).

Since high-level output voltage is directly related to supply voltage, the output current of the device is also directly related. The output current value is established by choosing output conditions to produce a current that is approximately one-half of the true short-circuit current.

It is advantageous to regulate or clamp the maximum supply voltage at 5.5 V including noise ripple and spikes. When this conditions exists, unused AND and NAND gates can be connected directly to the supply voltage.

SUPPLY VOLTAGE RIPPLE

Ripple in the supply voltage is generally considered a part of the supply voltage regulation. However, when combined with other effects (e.g., slow rise times), ripple voltage is more significant.

The effect of ripple voltage V_R can appear on either the supply voltage V_{CC} or the ground supply GND. When ripple appears on the supply voltage, it causes modulation of the input signal. The extent of the effect depends upon circuit parameters and source impedance.

The turning on of transistor Q5, shown in Figures 12 and 13, is controlled by the voltage at the base of transistor Q2 with respect to ground in accordance with the formula:

$$V_B = V_{BE} \text{ of Q2} + V_{BE} \text{ of Q3} + V_{BE} \text{ of Q5}$$

Table IV. Guidelines for Printed Circuit Board Layout for Advanced Schottky TTL

ITEM	GUIDELINE
Signal connections	Whenever possible, distribute loads along direct connections. Signal leads should be kept as short as possible. However, lead lengths of up to 15 inches will perform satisfactorily. This is especially for large boards that use a ground plane, ground, and/or V_{CC} plane. In addition, it will perform satisfactorily for small boards using ground mesh or grid. In high-frequency applications, avoid radial fanouts and stubs. If they must be used to drive some loads, reduce lead length proportionally and avoid sharp bends. Normal on-board fanouts and interconnections do not require terminations. Response of lines driving large numbers or highly capacitive loads can be improved with terminations of 300 Ω to V_{CC} and 600 Ω to ground in parallel with the last load if fanout of the driving output permits.
Conductor widths	Signal-line widths down to 0.015 inch are adequate for most signal leads.
Signal-line spacing	Signal-lead spacing on any layer down to 0.015 inch can be used especially if care is taken to avoid adjacent use of maximum length and minimum spacing. Increase spacing wherever layout permits. Pay particular attention to clock and/or other sensitive signals.
Insulator material	Thickness of insulation material used for a multilayer board is not critical. If ground and V_{CC} planes or meshes are used, their capacitive proximity can be used to reduce the number of decoupling capacitors needed and this also supplements the supply bypass capacitor.

Table V. Guidelines for General Usage of Advanced Schottky TTL

ITEM	GUIDELINE
Power supply	For RF bypass supply primary, maintain ripple and regulation at less than or equal to 10%.
V_{CC} decoupling	Decouple every 2 to 5 packages with RF capacitors of 0.01 to 0.1 μF. Capacitors should be located as near as possible to the decoupled devices. Decouple line driving or receiving devices separately with 0.1 μF capacitors between V_{CC} and the ground pins.
On-board grounding	A ground plane is essential when the PCB is relatively large (over 12 inches). Smaller boards will work with ground and/or V_{CC} mesh or grid.
System grounding	Try to simulate bus bars with a width to thickness ratio greater than or equal to 4. This can be accomplished by multiple parallel wires or by using flat braid. Performance will be enhanced when a copper or silver-copper bus is used. The width to thickness ratio required will vary between systems, but greater than or equal to 4 will satisfy most systems.

Table VI. Guidelines for Gates and Flip-Flops Using Advanced Schottky TTL

ITEM	GUIDELINE
Data input rise and fall times	Reduce input rise and fall times as driver output impedance increases. Rise and fall times should be equal to or less than 50 ns/V and essentially free of noise ripple.
Unused input of AND and NAND gates and unused preset and clear inputs of flip-flops	Tie the unused input of AND and NAND gates and the unused preset and/or clear inputs of flip-flops as follows: 1. Directly to V_{CC}, if the input voltage rating of 5.5 V maximum is not exceeded. 2. Through a resistor equal to or greater than 1 kΩ to V_{CC}. Several inputs can be tied to one resistor. 3. Directly to a used input of the same gate, if maximum fanout of driving device will not be exceeded. Only the high-level loading of the driver is increased. 4. Directly to an unused gate output, if the gate is wired to provide a constant high-level output. Input voltage should not exceed 5.5 V.
Unused input of NOR gates	Tie unused input to used input of same gate, if maximum fanout of driving device will not be exceeded or tie unused input to ground.
Unused gates	Tie input of unused NAND and NOR gates to ground for lowest power drain. Tie inputs of unused AND gates high and use output for driving unused AND or NAND gate inputs.
Increasing gate/buffer fanout	Connect gates of same package in parallel.
Clock pulse of flip-flops	Drive clock inputs with a TTL output. If not available, rise and fall times should be less than 50 ns/V and free of ripple noise spikes.

When ripple voltage is modulated onto the input voltage, the amplitude depends on the source impedance (Figure 29). The amplitude can be determined by the following equation:

$$\Delta V_R = V_R\left(\frac{R1/\beta}{R1/\beta + R2}\right)$$

$$= V_R\left(\frac{R1}{R1 + \beta R2}\right)$$

where $R1$ = source impedance
β = gain of transistor Q1.

Ripple voltage has the effect of adding extra pulses to the input signal (Figure 30). When ripple voltage appears in the ground supply, the threshold voltage is modulated and extra pulses occur (Figure 31).

Although decreasing the source impedance will reduce the effects of ripple voltage, it cannot be eliminated entirely because the emitter-base junction has an apparent resistance of approximately 30 Ω. Because of cancellation between the

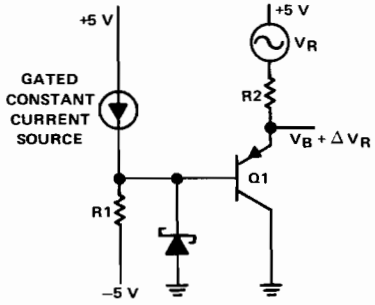


Figure 29. Effect of Source Impedance on Input Noise

driving gate and the driven gate, low-frequency ripple is not a problem.

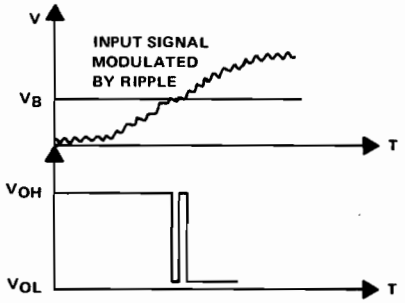


Figure 30. Spurious Output Produced by Supply Voltage Ripple

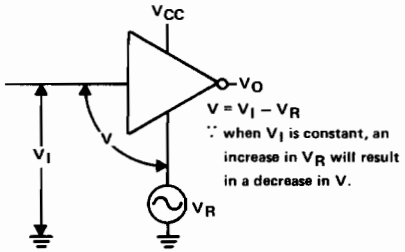


Figure 31. Effect of Ground Noise on Noise Margin

NOISE CONSIDERATIONS

Extraneous voltages and currents (called noise) introduced into a digital logic circuit are discussed in the following paragraphs. Figure 32(a) is a typical digital logic circuit consisting of a NAND gate and a J-K flip-flop. When a small noise pulse is coupled onto the clock input [(Figure 32(b)], the flip-flop does not respond and the Q output is correct. However, when a large noise pulse is coupled onto the clock input [(Figure 32(c)], the flip-flop sees the pulse as a clock transition and an erroneous Q output occurs. Therefore, it is essential to protect digital logic circuits from noise.

Noise Types and Control Methods

The noise types encountered in digital logic systems, their source, and the method of controlling them are as follows:

1. External noise — External noises radiated into the system. The sources include circuit breakers, motor brushes, arcing relay contacts, and magnetic-field-generating. The methods of controlled to be considered are shielding, grounding, or decoupling.
2. Power-line noise — Noise coupled through the ac or dc power distribution system. The initial sources and controlling methods are the same as for external noise.
3. Cross talk — Noise induced into signal lines from adjacent signal lines. Controlling methods to consider are shielding, grounding, decoupling, and, where possible, increasing the distance between the signal lines.
4. Signal-current noise — Noise generated in stray impedances throughout the circuit. The controlling methods to consider are shielding, grounding, decoupling, and, where possible, reduction of stray capacitance in the circuit.
5. Transmission-line reflections — Noise from unterminated transmission lines that cause ringing and overshoot. The method of control is to use, where possible, terminated transmission lines.
6. Supply-current spikes — Noise caused by switching several digital loads simultaneously. The controlling method is to design, where possible, the system so that digital loads are not switched simultaneously.

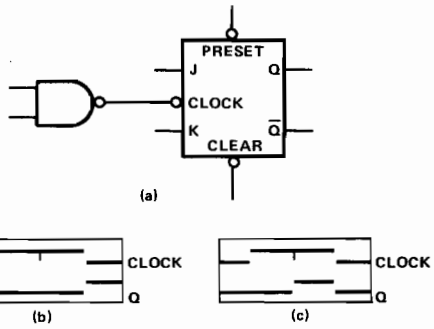


Figure 32. Typical Logic Circuit with Noisy Input

Shielding

In addition to its own internally generated noise, electrical equipment must operate in an extremely noisy environment. Noise pulses, which may come from a number of sources, consist of an electrostatic field, and electromagnetic field, or both. The noise waveform must be prevented from entering the equipment. This is accomplished by shielding. Since the noise fields are usually changing at a rapid rate, the shield required to exclude them may be very small. For effective exclusion, the sensitive circuits must be completely shielded.

Aluminum or similar materials are effective in stopping electrostatic noise. However, only a ferrous metal can successfully protect equipment against magnetic fields. While it is helpful to connect the system to earth ground, the shield

system must be complete and must be grounded to the system ground to prevent the shield from coupling noise into the system.

External noise may be conducted into the system by the power lines. Decoupling and filtering of these lines should be standard design procedure.

Grounding and Decoupling

The total propagation delay is of secondary importance in generation of internal noise. The actual transition time determines the amplitude and frequency spectrum of the generated signal at the higher harmonics. Application of the Fourier integral to series 'ALS/'AS waveforms shows frequency components of significant amplitude that exceed 100 MHz. Because of the frequency spectrum generated when an 'ALS/'AS device switches, a system using these devices must consider problems caused by radio frequency (RF) even though the repetition rates may be only a few megahertz. The transient currents generated by charging capacitors, changes in the levels of dc, line driving, etc., must be considered. In Figure 33 for example, a gate driving a transmission line is represented by a voltage source E, having an output impedance Z_S connected to an impedance Z_0, and loaded with a resistance R_L.

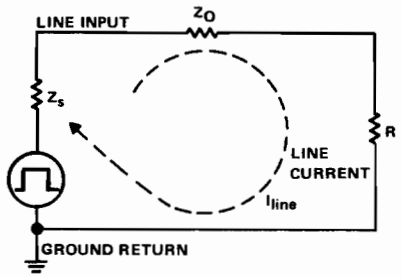


Figure 33. Diagram Representing a Gate Driving a Transmission Line

Until after a reflected pulse returns from the termination of the transmitting device, line termination is not a factor in drive current. In a practical TTL circuit, the line termination must be high relative to the line impedance. For explanation purposes, assume that the source voltage is 5 V in amplitude, the output impedance of the source is 50 Ω and the line impedance is 50 Ω. When the source voltage makes the transition from 0 V to 5 V, the voltage across the input of the line V_I is determined by the following equation:

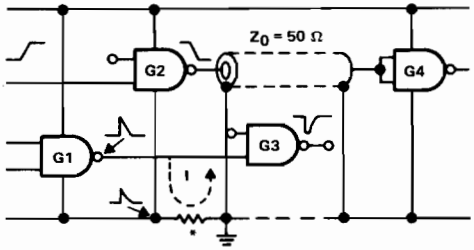
$$V_I = E \frac{Z_0}{Z_S + Z_0} = 2.5 \text{ V}$$

where E = source voltage
Z_0 = line impedance
Z_S = source impedance

For the 50 Ω line to become charged, the current that must flow onto the line is determined by the following equation:

$$I_{line} \quad \frac{V_{in}}{Z_0} = \frac{2.5}{50} = 50 \text{ mA}$$

In addition, this current flows in the ground return, which, in this case, is the transmission-line ground. If the line and return are originated and terminated close to the driving and receiving devices, there is no discontinuity in the line. Where the ground is poorly returned, the current flow sees the discontinuity in the cable as a high impedance and a noise spike is generated (i.e., the ground current sees a low impedance and a current cancellation if the ground is properly carried through and, if not, it sees a high impedance). Figure 34 presents a specific example. Assume that the gate driving the line is switched from the high to low state. Current flow is indicated by the arrow marked with an I. Since the line is improperly returned to the driver, a pulse is developed across the impedance. A possible consequence is the false output of gate 3 (G3).



*Impedance of poor ground return

Figure 34. Noise Generation Caused by Poor Transmission-Line Return

If the ground return is properly connected, the proper results are obtained. The impedance discontinuity is eliminated and current cancellation occurs at the ground point. Undesirable voltage spikes are then eliminated. Two empirical rules to reduce transmission-line currents have been established and have been found to be effective (Figure 35).

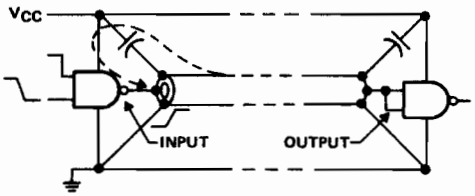
1. Carry all returns, including twisted pair and coaxial cables, to a good ground termination. Ground line returns close to the driving and receiving devices.
2. Decouple the supply voltage of line-driving and line-receiving gates with a 0.1-μF disk ceramic capacitor.

As the devices change state, current levels change because of the different device currents required in each state, the external loading, the transients caused by charging and

discharging capacitive loads, and the conduction overlap in the totem-pole output stage. When a gate changes states, its internal supply current changes from high to low (these values are stated on the data sheet for each device). In addition, any capacitance, stray or otherwise, must be charged or discharged for a logic state change. The capacitance must be charged by a current determined by

$$I = C \frac{dv}{dt} \quad (4)$$

If the total stray capacitance on a gate output, the logic-level voltage excursion, and the associated rise or fall times are known, then the ideal-case instantaneous current during the transition can be calculated.

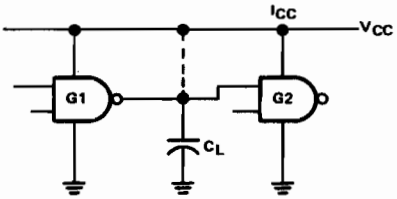


Broken arrow shows path of line-charging current

Figure 35. Ideal Transmission-Line Current Handling

From Eq. (4) it can be determined that the current transient for charging load capacitance will increase with higher speed TTL circuits. Therefore, the Series 54ALS/74ALS devices will have lower transient current than the Series 54AS/74AS devices. Another parameter that should be considered is the value of R7 (shown in Figures 12 and 13). Resistor R7 acts as a limit on the charging current.

The current required for charging load capacitance C_L (Figure 36) is supplied by the supply voltage when the transition is from logic low to logic high at the output of gate 1 (G1). When the output of G1 goes from high to low, the load capacitance is shorted to ground by transistor Q5 (shown in Figures 12 and 13) and has no effect on supply current.



C_L includes all capacitance: stray, device, etc.

Figure 36. Circuit with Effective Capacitive Loading

A characteristic common to all TTL totem-pole output stages contributes an additional current transient when the output changes from a logic low to a logic high. This transient, or spike, is caused by the overlap in conduction of the output transistors Q7 and Q5 (shown in Figures 12 and 13). The situation arises because transistor Q7 can turn on faster than transistor Q5 can turn off. This places a direct circuit consisting of transistors Q7 and Q5 and resistor R4 between supply voltage and ground. For all series 'ALS TTL circuits, the maximum possible peak current can be determined by

$$I_{CC}max = \frac{V_{CC} - V_{CEQ6} - V_{BEQ7} - V_{CEQ5}}{R7}$$

However, due to the active turnoff circuit (consisting of R5, R6, and Q4), Q5 will be only slightly in the linear region and the current spike will be less.

The total supply-current switching transient is then a combination of three major effects: the difference in high-level and low-level supply current, the charging of load capacitance, and the conduction overlap. Tests were performed to demonstrate these effects. The results are shown in Figure 37. Six types of series TTL devices were tested with no load (i.e., the oscilloscope was connected to the output only when measuring V_O and the photographs were double exposed). This was to approximate the effects of conduction overlap isolated from the transient caused by charging load capacitance. Different vertical scales were used on some of the photographs.

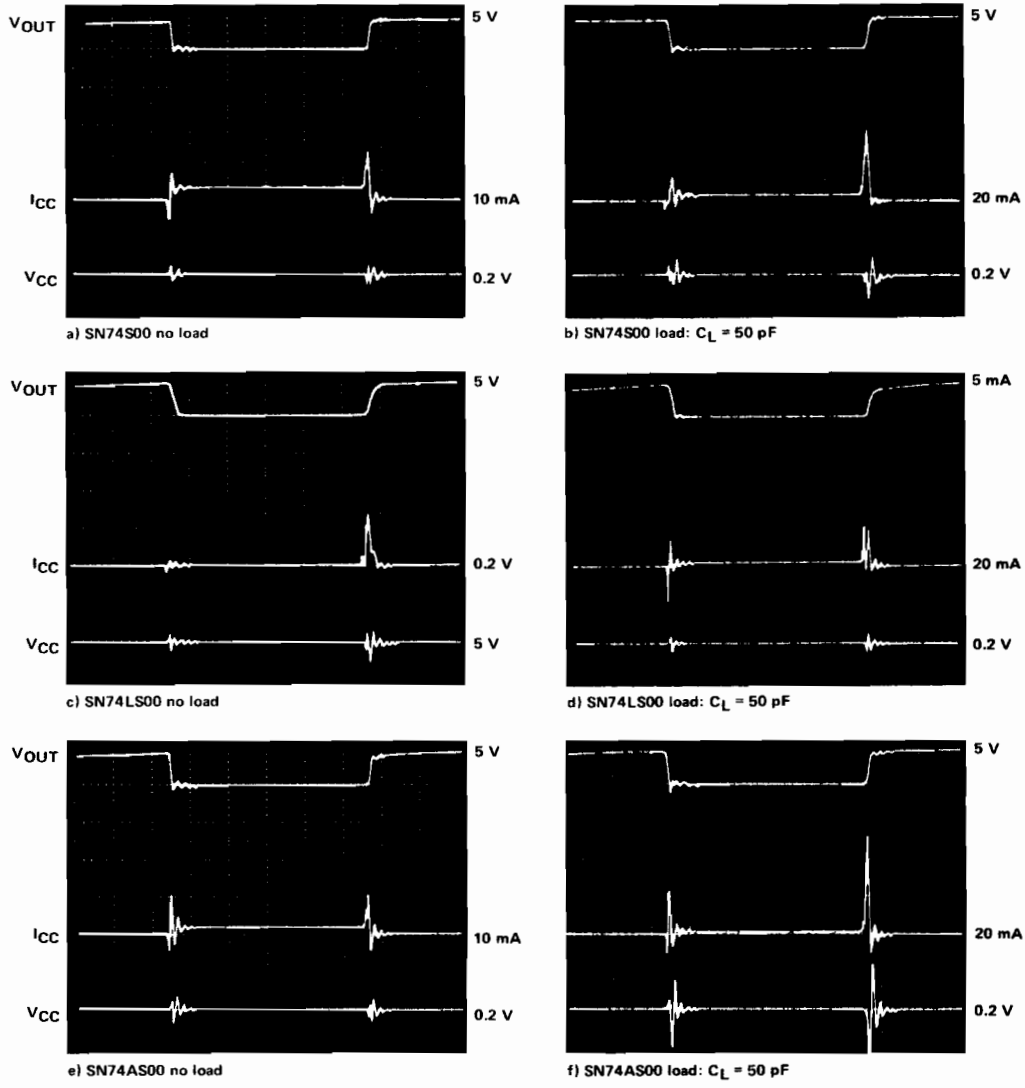
The results are almost as predicted. The low-power devices have the lower transients. Since it is the fastest circuit, the SN74AS00 device should be highest. However, a decrease is shown, and the reason for the decrease is explained (Figure 39). The additional circuits to reduce conduction overlap of the output transistors result in a smaller transient even though the typical switching time is 1.7 ns compared to 9 ns for the Series 54/74LS.

The second series of tests shown in Figure 37 cover a capacitive load of 50 pF. For this test, all of the supply current transient peaks increase in amplitude and width.

Because of the larger transient currents, voltage spikes on the supply voltage measured at the IC package are also increased.

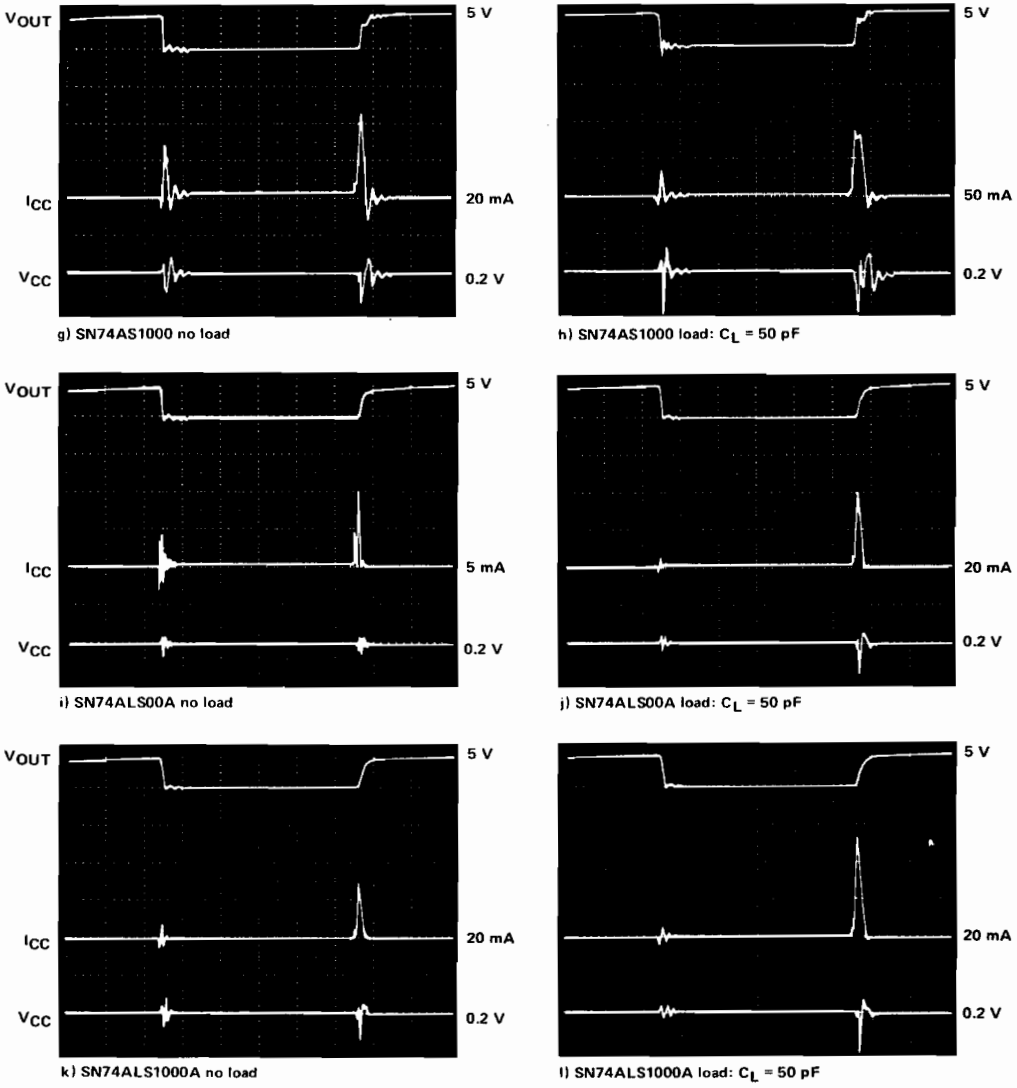
From these tests, it can be concluded that the condition to be avoided (the only one that can be avoided) is unnecessary stray capacitance in circuit wiring. The charging of load capacitance, in most cases, overshadows the other two effects with respect to noise produced on the supply voltage line by switching current transients.

The flow paths of these currents have been investigated to determine the grounding and decoupling necessary to counteract their effects. Supply voltage decoupling may be accomplished by one of two methods. Maintaining low impedance from the individual circuit supply voltage to



NOTES: 1. V_{CC} = 5 V
2. Sweep is 50 ns/division
3. Rise and fall times of input pulse are 1 ns
4. Vertical scales are in units shown per division

Figure 37(a). Supply-Current Transient Comparisons



NOTES: 1. V_{CC} = 5 V
2. Sweep is 50 ns/division
3. Rise and fall times of input pulse are 1 ns
4. Vertical scales are in units shown per division

Figure 37(b). Supply-Current Transient Comparisons

ground is common to both methods. In the first method, the supply voltage line may be considered as a transmission line back to a low impedance supply. The positive bus can be laminated with a ground bus to form a strip transmission line of extremely low impedance. This line can be electrically approximated with lumped capacitances as shown in Figure 38. The inductances are usually a distributed component which must be minimized to lower the line impedance.

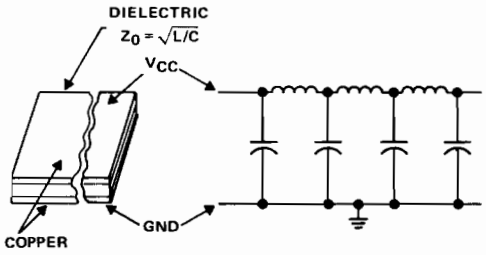


Figure 38. Transmission-Line Power Buses

The second method is to consider the supply voltage bus as a dc connecting element only and to provide a low-impedance path near the devices for the transient currents to be grounded (Figure 39).

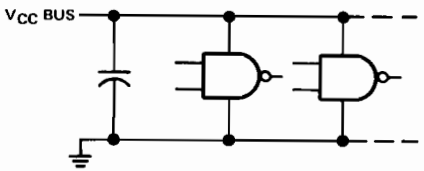


Figure 39. Capacitive Storage Supply Voltage System

For effective filtering and decoupling, the capacitors must be able to supply the change in current for a period of time greater than the pulse width of this current. Since the problem is essentially one of dc changes due to logic state coupled with high-frequency transients associated with the changes, two different values of time constant must be considered. Capacitors combining the high capacitance required for long periods with the low series reactance required for fast transients are prohibitive in cost and size. A good compromise is the arrangement shown in Figure 40.

The typical component values may be found for the RF capacitor C2 by assuming that the parameters have common values as follows:

$\Delta I_{CC} = 50$ mA
$\Delta V = 0.1$ V
$\Delta T = 20$ ns

Then the equation is as follows:

$$C2 = \frac{\Delta I_{CC}}{\Delta V/\Delta T} = \frac{(50)(20) \times 10^{-12}}{0.1/(20 \times 10^{-9})}$$

$$= \frac{50 \times 10^{-3}}{0.1} = 10{,}000 \times 10^{-12}$$

$$= 0.01\ \mu F$$

The same method may be used for the low-frequency capacitor C1. However, the factor ΔT, which was a worst-case transient time for calculating C1, now becomes a bit ambiguous. An analysis of the current cycling on a statistical basis is the best method in all but the simplest systems. The recommended procedure is to decouple using 10 μF to 50 μF capacitors.

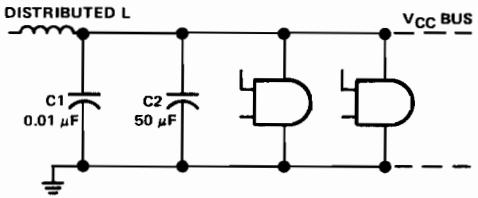


Figure 40. Commonly Used Power Distribution and Decoupling System

A discrete inductance of 2 μH to 10 μH is sometimes used for additional decoupling. However, its benefits are questionable and its usefulness should be evaluated for the individual system. The low-pass filter formed must be capable of keeping the transients confined and off the distribution bus. The possibility of resonance in the inductor or LC combination must be considered.

Noise spikes on the supply voltage line that do not force the gate output below the threshold level do not present a serious problem. Downward spikes as large as 3 V can be tolerated on the supply voltage line without propagating through the logic system. The system designer can be confident that supply voltage noise can be handled even with minimal consideration.

Ground noise, however, cannot be treated lightly. Pulses on a high-impedance ground line can easily exceed the noise threshold. Only if a good ground system is maintained can this problem be overcome. If proper attention is paid to the ground system, noise problems can be minimized.

The concept of a common-ground-plane structure as used in RF and high-speed digital systems is quite different from the concept of the common-ground point as used in low-frequency circuits. The more closely the chassis and ground can approach to being an integral unit, the better the noise suppression characteristics of the system. Consequently, all

parts of the chassis and ground bus system must be bound tightly together both electrically and mechanically. Floating or poorly grounded sections not only break the integrity of the ground system, but may actually act as a noise distribution system.

For grounds and decoupling on printed circuit boards, the most desirable arrangement is a double-clad or multilayer board with a solid ground plane or a mesh. Where component density prohibits this, the ideal should be relaxed only as far as necessary. Cross talk and ground noise can be reduced on large boards with a ground plane. Some suggestions for board grounds where a plane is not practical are as follows:

1. Use as wide a ground strap as possible.
2. Form a complete loop around the board by bringing both sides of the board through separate pins to the system ground.

The supply voltage line can provide part of the ground mesh on the board, provided it is properly decoupled. For a TTL system, a good guideline is 0.01 μF per synchronously driven gate and at least 0.1 μF for each 20 gates, regardless of synchronization. This capacitance may be lumped, but is more effective if distributed over the board. A good rule is to permit no more than 5 inches of wire between any two package supply-voltage points. Radio-frequency-type capacitors must be used for decoupling. Disk ceramics are best. It is sometimes a good practice to decouple the board from the external supply-voltage line with a 2.2 μF capacitor. However, this is optional and the RF capacitors are still required. In addition, it is recommended that gates driving long lines have the supply voltage decoupled at the gate supply voltage terminal and that the capacitor ground, device ground, and transmission-line ground be connected to a common point.

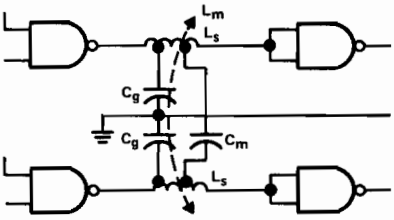
Cross Talk

When currents and voltages are impressed on a connecting line in a system, it is impossible for adjacent lines to remain unaffected. Static and magnetic fields interact and opposing ground currents flow, creating linking magnetic fields. These cross-coupling effects are lumped together and called cross talk.

Back-Panel Interconnections

Interconnecting signal lines can be grouped into three broad categories: coaxial lines, twisted-pair lines, and straight wire lines. Because of the low impedance and shielding characteristics of coaxial cable, its cross talk is minimal and is not a problem with TTL.

Figure 41 illustrates a practical type of signal transmission line. The mutual reactances L_m and C_m which form the noise coupling paths and the line parameters L_s and C_g which govern the line impedance, will vary with the type of line used. Since cross talk is a function of the ratio of the mutual impedances to the line characteristic impedances, the selection of transmission-line type must be at least partially a factor in cross-talk considerations.

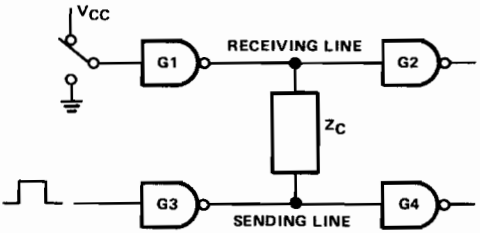


ALL GATES SN74ALS00

Figure 41. Equivalent Circuit for Sending Line

The use of direct-wired connections is the simplest and lowest cost method, but they are also the poorest for noise rejection. If the lead is not cabled tightly together with similar leads, direct leads up to 12 inches in length can be used.

When the length of the signal line is increased, the line impedance is seen by the driving and receiving gates. As shown in Figure 42, a pulse sent along the sending line G3 and G4 will be coupled via the coupling impedance Z_c onto the receiving line G1 and G2, which can be in either of the two logic states. The extent to which cross talk will occur depends on the type of lines used and their relationship to each other.



(Z_C) – COUPLING IMPEDANCE

Figure 42. Equivalent Circuit for Cross Talk

The voltage impressed on the sending line by gate G3 is determined by the equation:

$$V_{SL} = \frac{V_{G3}Z_0}{R_{S3} + Z_0} \quad (5)$$

where

V_{G3} = open-circuit logic voltage swing generated by gate G3
R_{S3} = output impedance of gate G3
Z_0 = line impedance
V_{SL} = voltage impressed on the sending line.

The relationship for the equation is illustrated in Figures 43 and 44.

The coupling from the sending line to the receiving line can be represented by taking coupling impedance Z_c into

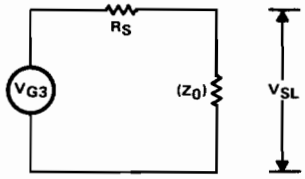


Figure 43. Capacitive Cross Talk Between Two Signal Lines

account. An equivalent circuit to represent the coupling from the sending line to the receiving line is shown in Figure 44.

As the voltage impressed on the sending line propagates farther along the line, it can be represented as voltage source V_{SL} with a source impedance of Z_{01} (Figure 45). V_{SL} is then coupled to the receiving line via the coupling capacitance, where the impedance looking into the line is line impedance in both directions. Therefore the equation becomes

$$V_{RL} = V_{SL} \frac{\frac{Z_0}{2}}{(1.5\ Z_0 + Z_c)}$$

The voltage impressed on the receiving line (V_{RL}) then propagates along the receiving line to gate G2 which can be considered as an open circuit and voltage doubling occurs. Therefore:

$$V_{in(2)} = 2\ V_{RL} = V_{G3}\left(\frac{1}{1.5 + \frac{Z_c}{Z_0}}\right)\left(\frac{Z_0}{RS3 + Z_0}\right)$$

In the switching period, the transistor has a very low output impedance. Then $R_{S3} \ll Z_0$ and $V_{in(2)}$ can be simplified to the following:

$$V_{in(2)} = V_{G3}\left(\frac{1}{1.5 + \frac{Z_c}{Z_0}}\right)$$

The term $V_{in(2)}/V_{G3}$ can be defined as the cross-talk coupling constant.

The worst-case for signal line cross talk occurs when sending and receiving lines are close together but widely separated from a ground return path. The lines then have a high characteristic impedance and a low coupling impedance.

For example, if we assume a coupling impedance of 50 pF at 150 MHz with a line impedance of approximately 200 Ω then:

$$\frac{V_{in(2)}}{V_{G3}} = 0.62$$

This level is unsatisfactory because none of the very high-speed logic circuits has a guaranteed noise margin greater than one-third of the logic swing. Such potential cross talk can be avoided by not using the close spacing of conductors.

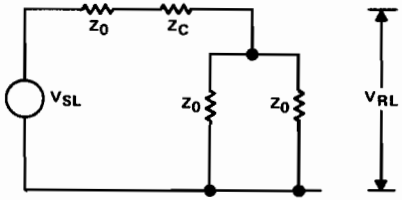


Figure 45. Equivalent Cross-Talk Network

Mutual coupling can be reduced by using coaxial cable or shielded twisted pairs. When mutual inductance and capacitance are decreased, line capacitance is increased and imposes restrictions on the driver. Coaxial cable combines very high mutual impedance with low characteristic impedance and shielding. It effectively eliminates cross talk, but is necessary in only the noisiest environments. Twisted pairs are adequate for most applications and are typically less expensive and easier to use.

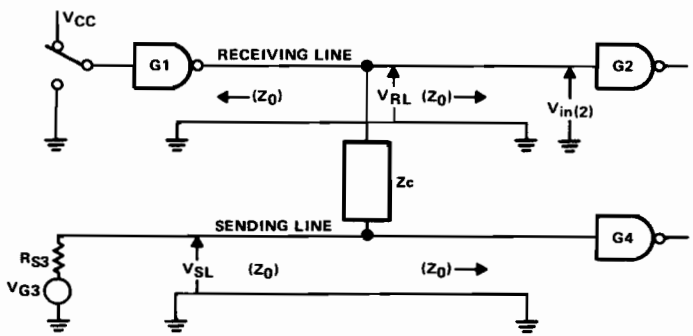


Figure 44. Coupling Impedances Involved in Cross Talk

Printed Circuit Card Conductors

Signal interconnections on a two-sided or multilayer printed circuit card can be grouped into two general categories: microstrip lines and strip lines. The microstrip line (Figure 46) consists of a signal conductor separated from a ground plane by a dielectric insulating material. A strip line (Figure 47) consists of a signal conductor within a dielectric insulating material and the conductor being centered between two parallel conductor planes. The important features of these type of printed circuit conductors are that the impedances are highly predictable, can be closely controlled, and the process is relatively inexpensive because standard printed circuit board manufacturing techniques are used. Typical impedances of these types of conductors with respect to their physical size and relative spacings are shown in Tables VII and VIII.

Table VII. Typical Impedance of Microstrip Lines

Dimensions		Line Impedance	Capacitance
H (mils)	W (mils)	Z_O (Ω)	per Foot (pF)
6	20	35	40
6	15	40	35
15	20	56	30
15	15	66	26
30	20	80	20
30	15	89	18
60	20	105	16
60	15	114	14
100	20	124	13
100	15	132	12

Relative dielectric constant ≈ 5

Table VIII. Typical Impedance of Strip Lines

Dimensions		Line Impedance	Capacitance
H'a = H'b = (mils)	W (mils)	Z_O (Ω)	per Foot (pF)
6	20	27	80
6	15	32	70
10	20	34	67
10	15	40	56
12	20	37	57
12	15	43	48
20	20	44	48
20	15	51	42
30	20	55	39
30	15	61	35

Relative dielectric constant ≈ 5, and H'a = H'b

Cross talk on a printed circuit board is also a function of the mutual reactances and the line parameters which govern the line impedance. A microstrip line and a strip line are, by definition, conductors placed relatively close to a ground plane. Therefore, they have at least one inherent property which tends to reduce cross talk. In addition, the thickness (H) of the dielectric and the spacing (S) of the conductors can be implemented selectively to reduce the amount of possible cross talk. The effects of these two dimensions on cross talk have been evaluated and are shown graphically in Figure 48. The data shown can be used to estimate the maximum crosstalk which will be encountered under the most unfavorable conditions.

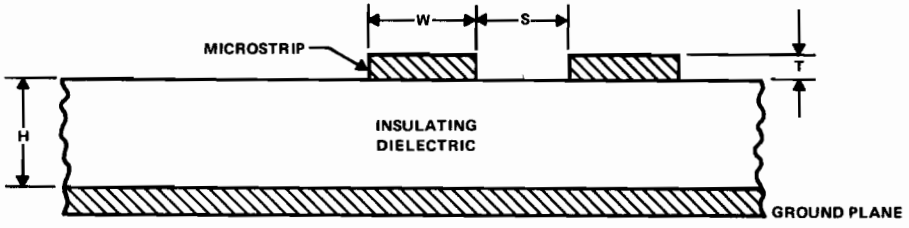


Figure 46. Microstrip Line

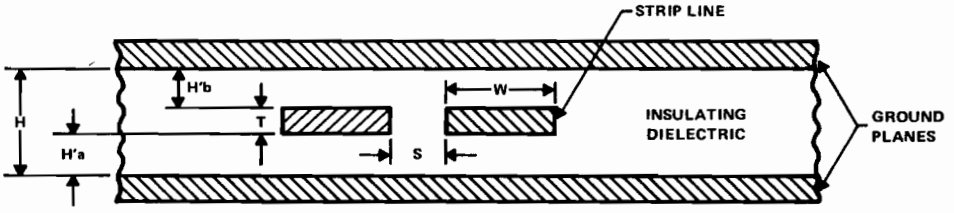


Figure 47. Strip Line

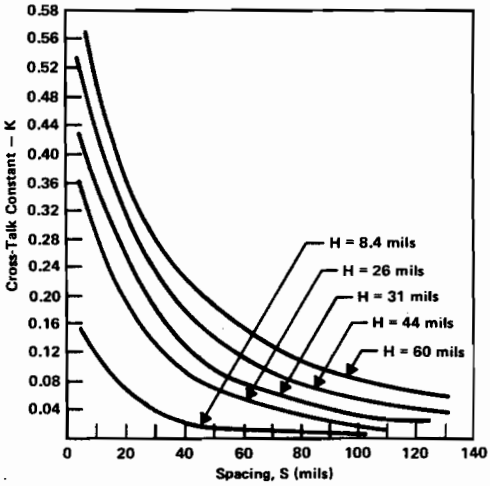


Figure 48. Line Spacing Versus Cross-Talk Constant

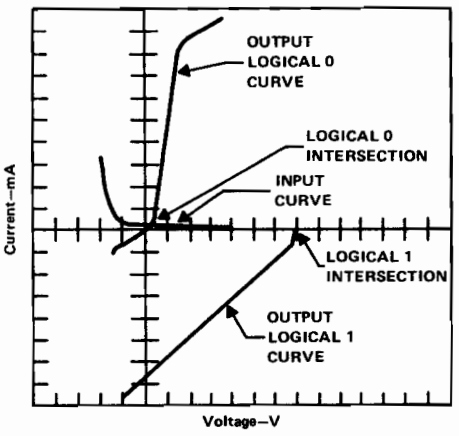


Figure 49. TTL Bergeron Diagram

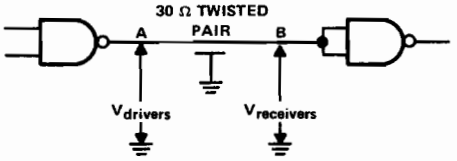


Figure 50. 'ALS/'AS Driving Twisted Pair

Transmission-Line Driving Reflections

When the interconnections used to transfer digital information become long enough so that line propagation delay is equal to or greater than the pulse transition times, the effects of reflections must be considered. These reflections are created because most TTL interconnections are not terminated in their characteristic impedance. Reflections lead to reduced noise margins, excessive delays, ringing, and overshoot. Some method must be used to analyze these reflections. Because neither the gate input nor output impedance is linear, basic transmission-line equations are applicable but unwieldy. Transmission-line characteristics of TTL interconnections can be analyzed by using a simple graphic technique.

Figure 49 shows piecewise linear plots of a gate input and both (logic-high and logic-low) states of the output for a typical TTL device. The output curves are plotted with positive slopes. The input is inverted because it is at the receiving end of a transmission line. The logic-high and logic-low intersections are indicated on the plot. These points are the steady-state values which will be observed on a lossless transmission line (Figure 50).

Figure 50 shows a typical TTL interconnection using a twisted-pair cable which, in this example, has a characteristic impedance of approximately 30 Ω. To evaluate a logic-high to logic-low 'AS transition see Figures 51 and 52. The equation $-1/Z_0$ (Z_0 = 30 Ω), which represents the transmission line, is superimposed on the output characteristic curves in the Bergeron plot. Since evaluation of a logic-high to logic-low transition is desired, the $-1/Z_0$ line starts at the point of intersection of the impedance curves of the input and output for a logic-high state. The slope $-1/Z_0$ then proceeds toward the logic-low output curve. At time t_0, the driver output voltage is determined by the intersection of $-1/Z_0$ and the logic-low output curve (1.2 V). The transmission-line slope now becomes $1/Z_0$ and is drawn toward the input curve. At time t_1 [$t_{(n+1)} - t_n$ = time delay of line], the receiving gate sees −1.7 V. Now the line slope changes back to $-1/Z_0$ and the output curve for a logic low is approached. This action continues until the logic-low intersection is reached. Figure 52 plots driver and receiver voltages versus time for this example.

A logic-low to logic-high transition is treated in approximately the same manner (Figure 53). The Bergeron line $-1/Z_0$ starts at the intersection for a logic low. At time t_0, the driver output rises to 2.2 V and, at time t_1, the receiving gate input goes to approximately 4.35 V. Both output and input voltages are plotted in Figure 54.

Figures 55 through 58 illustrate 'ALS transitions and are treated in the same manner as the 'AS.

The scope photographs in Figures 59 through 66 show the effectiveness of the graphic techniques. In most cases, the calculated and experimental values of voltage steps agree within reason. The ringing that appears for the open wire is not immediately obvious. This is because the input and output curves in this region lie practically along the positive horizontal axis. At the scale used for graphic analysis, it is difficult to go much beyond the first few reflections. The graphic analysis is idealized and stray capacitance and inductance are not considered.

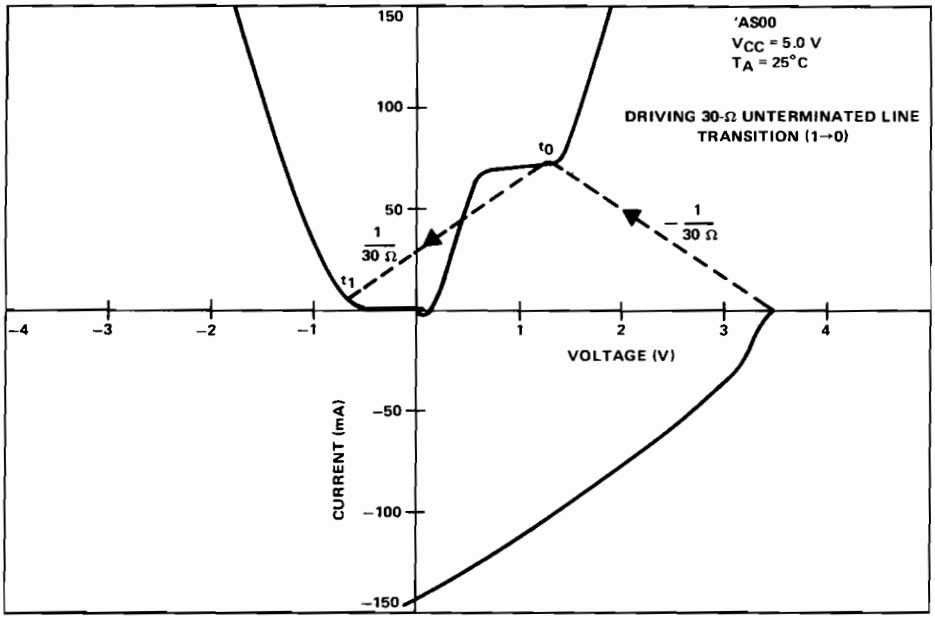


Figure 51. 'AS −ve Transition Bergeron Diagram

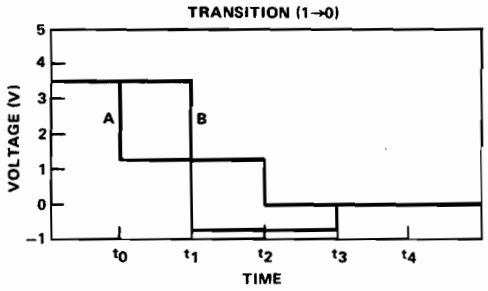


Figure 52. 'AS −ve Voltage/Time Plot

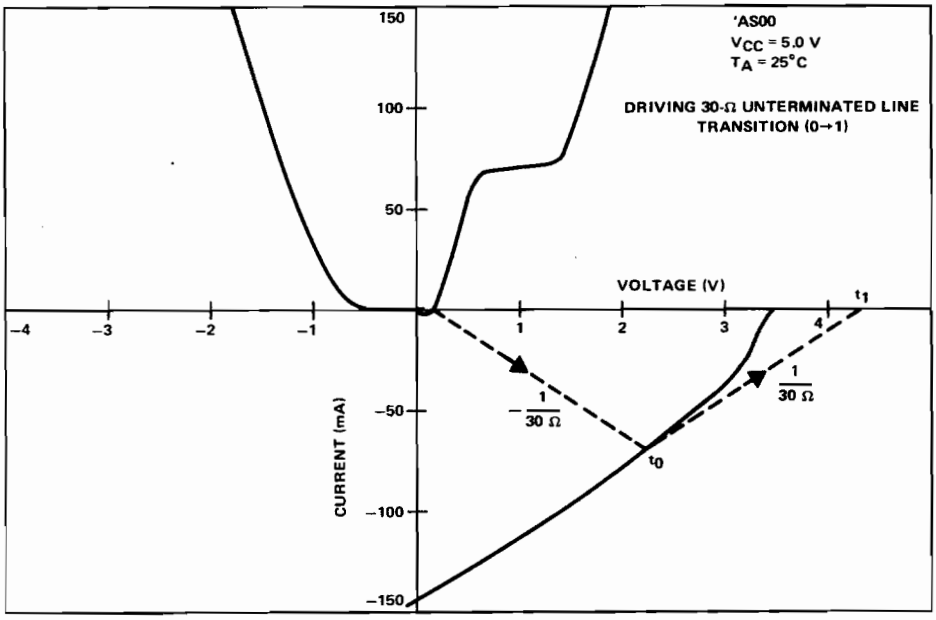


Figure 53. 'AS +ve Transition Bergeron Diagram

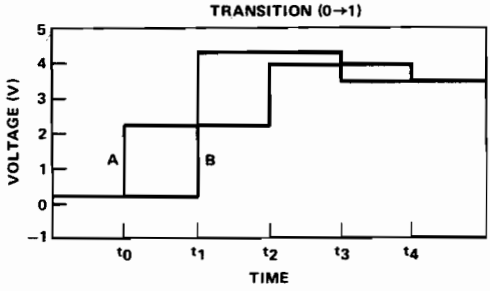


Figure 54. 'AS +ve Voltage/Time Plot

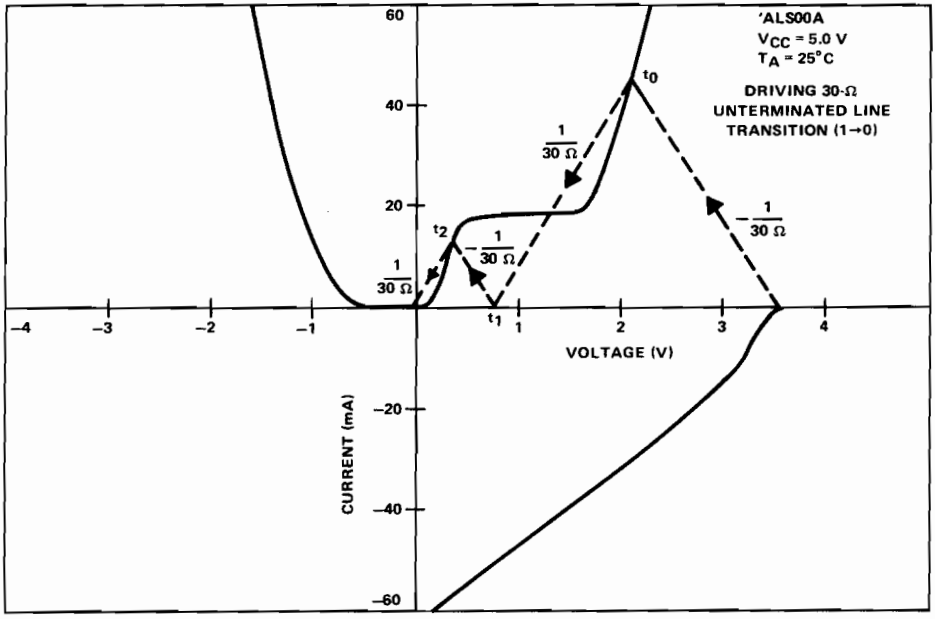


Figure 55. 'ALS −ve Transition Bergeron Diagram

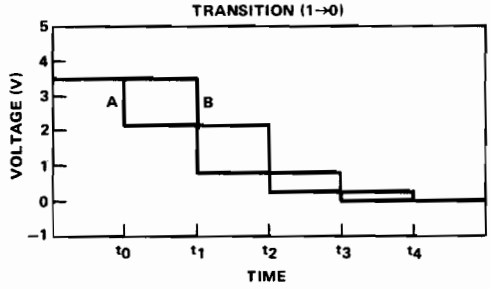


Figure 56. 'ALS −ve Voltage/Time Plot

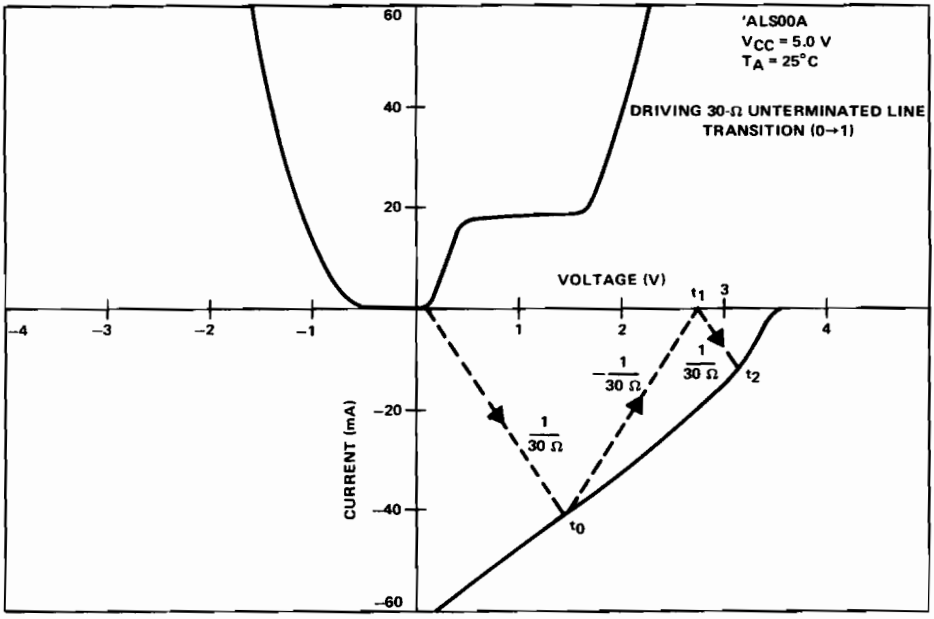


Figure 57. 'ALS +ve Transition Bergeron Diagram

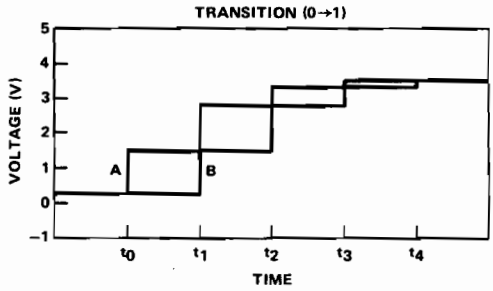


Figure 58. 'ALS +ve Voltage/Time Plot

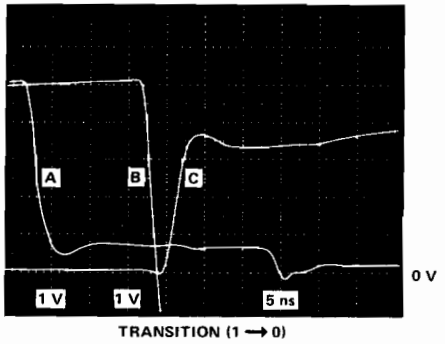


Figure 59. Oscilloscope Photograph of 'AS001 – ve Transition Using 50-Ohm Line

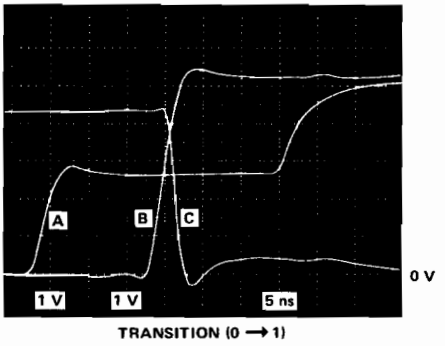


Figure 60. Oscilloscope Photograph of 'AS00 + ve Transition Using 50-Ohm Line

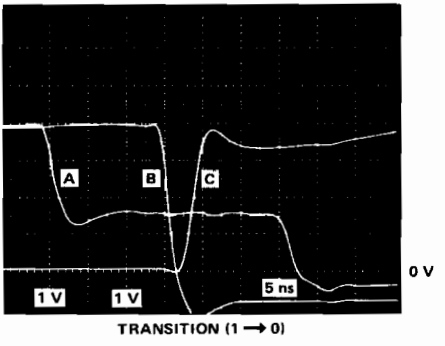


Figure 61. Oscilloscope Photograph of 'AS00 – ve Transition Using 25-Ohm Line

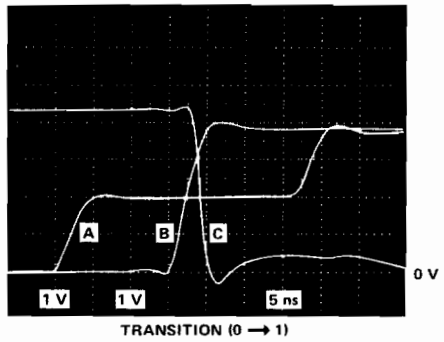


Figure 62. Oscilloscope Photograph of 'AS00 + ve Transition Using 25-Ohm Line

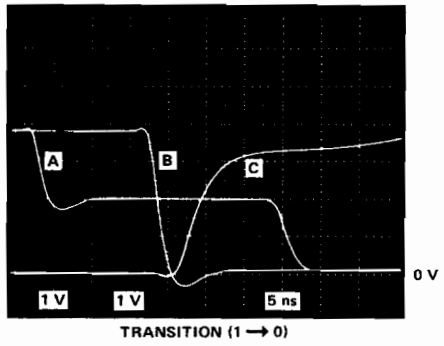


Figure 63. Oscilloscope Photograph of 'ALS00A – ve Transition Using 50-Ohm Line

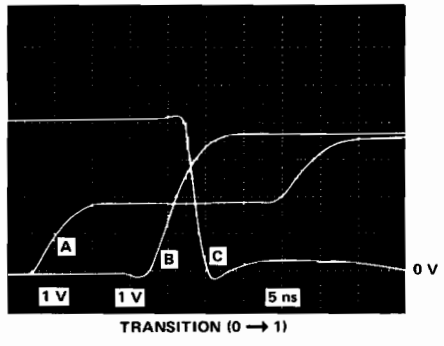


Figure 64. Oscilloscope Photograph of 'ALS00A + ve Transition Using 50-Ohm Line

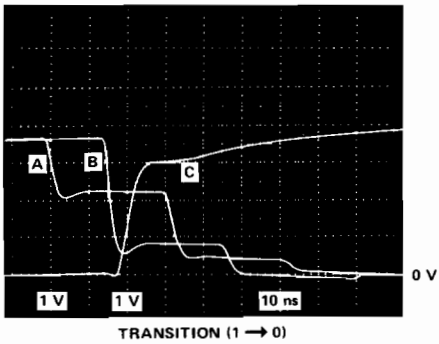


Figure 65. Oscilloscope Photograph of 'ALS00A −ve Transition Using 25-Ohm Line

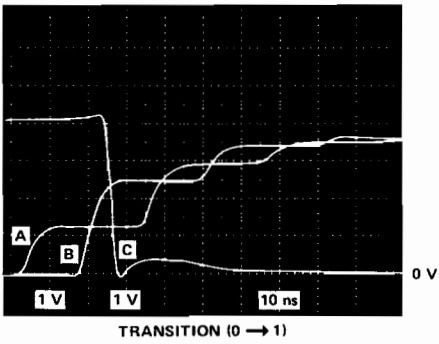


Figure 66. Oscilloscope Photograph of 'ALS00A +ve Transition Using 25-Ohm Line

References

1. W.C. Elmore and M. Sands, *Electronics Experimental Techniques*, McGraw-Hill Book Co., New York, 30ff. (1949).
2. M. Williams and S. Miller, *Series 54ALS/74ALS Schottky TTL Applications B215*, Texas Instruments Limited, Bedford, England, August 1982.

Acknowledgment

This application report is an updated version of Reference 2 with significant contributions by the technical engineering staff at Texas Instruments and particularly by Rock Cozad, Rich Moore, and Bob Strong.

Appendix A
Normalized Load Factors

Normalizing output drive capability and input current requirements can be very useful to designers of systems using two or more of the TI TTL series of devices. It provides a set of load factors (input cuurent requirements in Table A-I), which can be summed and compared directly to the fanout capability (see Table A-II) of the output being considered. The load factor values shown are valid for any input rated at one unit load.

The loading of these type of outputs can be checked from any column. However, most designs use one of the series as the basic building block and, since the tables cover each series individually, the designer has the choice of working from the column containing the normalized fanout. As an example, the designers of a system using series 'AS as the basic circuit will probably find that the use of the 'AS00 and 'AS1000 columns will suit best because both fanout and load factors are expressed for these series of devices.

The use of these simple and easy-to-remember numbers was developed within each series to make the verification of output loading a matter of counting the number of inputs connected to a particular output. When mixtures of series are used, a common denominator (normalized factor) becomes useful.

USE OF TABLES A-I AND A-II

Every possible combination of the seven 54/74 TTL families is included in these tables. If, for example, the existing system used 74S series logic and it is desired that some of it be replaced by series 74ALS logic, a quick check should be made on whether the 'ALS can be supplied with sufficient input current. By taking the 74S row and 'ALS, column figures of 2.5 and 20 are obtained for high- and low-level loads, respectively (see Table A-I). This indicates that, for high logic levels, two and one-half 'ALS gates can be driven for each 'S series gate removed. However, if more 74S series gates are being driven by this 'ALS device, the fanout between 'ALS and 'S series gate is required, you can now use Table A-II.

The 'ALS row and the 'S column are chosen. The figures are 8 for the high-logic level and 4 for the low-logic level. In this case the lowest figure is taken so that the interconnection is reliable for both logic states. So each 'ALS gate inserted will drive 4 'S series gates.

Table A-I is normally used (in combination with Table A-II) when replacing one logic family with another in an existing system.

Table A-II is normally used when originally designing a system which employs several TTL families to optimize performance.

Table A-I. Normalized Input Currents

SERIES	I/O	INPUT CURRENT (mA)	INPUT CURRENT NORMALIZED								
			'00	'H00	'L00	'LS00	'S00	'AS00	'ALS00A	'AS1000	'ALS1000A
54/7400	HI	0.04	1	0.8	4	2	0.8	2	2	2	2
54/7400	LO	1.6	1	0.8	8.89	4	0.8	3.2	16	3.2	16
54H/74H00	HI	0.05	1.25	1	5	2.5	1	2.5	2.5	2.5	2.5
54H/74H00	LO	2	1.25	1	11.11	5	1	4	20	4	20
54/74L00	HI	0.01	0.25	0.2	1	0.5	0.2	0.5	0.5	0.5	0.5
54/74L00	LO	0.18	0.11	0.09	1	0.45	0.09	0.36	1.8	0.36	1.8
54LS/74LS00	HI	0.02	0.5	0.4	2	1	0.4	1	1	1	1
54LS/74LS00	LO	0.4	0.25	0.2	2.22	1	0.2	0.8	4	0.8	4
54S/74S00	HI	0.05	1.25	1	5	2.5	1	2.5	2.5	2.5	2.5
54S/74S00	LO	2	1.25	1	11.11	5	1	4	20	4	20
54AS/74AS00	HI	0.02	0.5	0.4	2	1	0.4	1	1	1	1
54AS/74AS00	LO	0.5	0.31	0.25	2.78	1.25	0.25	1	5	1	5
54ALS/74ALS00A	HI	0.02	0.5	0.4	2	1	0.4	1	1	1	1
54ALS/74ALS00A	LO	0.1	0.06	0.05	0.56	0.25	0.05	0.2	1	0.2	1
54AS1000	HI	0.02	0.5	0.4	2	1	0.4	1	1	1	1
54AS1000	LO	0.5	0.31	0.25	2.78	1.25	0.25	1	5	1	5
54ALS1000A	HI	0.02	0.5	0.4	2	1	0.4	1	1	1	1
54ALS1000A	LO	0.1	0.06	0.05	0.56	0.25	0.05	0.2	1	0.2	1

Table A-II. Fanout Capability (Output Currents Normalized to Input Currents)

SERIES	I/O	OUTPUT CURRENT (mA)	OUTPUT DRIVE NORMALIZED								
			'00	'H00	'L00	'LS00	'S00	'AS00	'ALS00A	'AS1000	'ALS1000A
			*HI 0.04	0.05	0.01	0.02	0.05	0.02	0.02	0.02	0.02
			†LO 1.6	2	0.18	0.4	2	0.5	0.1	0.5	0.1
54/7400	HI	0.4	10	8	40	20	8	20	20	20	20
54/7400	LO	16	10	8	88.89	40	8	32	160	32	160
54H/74H00	HI	0.5	12.5	10	50	25	10	25	25	25	25
54H/74H00	LO	20	12.5	10	111.11	50	10	40	200	40	200
54L00	HI	0.1	2.5	2	10	5	2	5	5	5	5
54L00	LO	2	1.25	1	11.11	5	1	4	20	4	20
74L00	HI	0.2	5	4	20	10	4	10	10	10	10
74L00	LO	3.6	2.25	1.8	20	9	1.8	7.2	36	7.2	36
54LS/74LS00	HI	0.4	10	8	40	20	8	20	20	20	20
54LS00	LO	4	2.5	2	22.22	10	2	8	40	8	40
74LS00	LO	8	5	4	44.44	20	4	16	80	16	80
54S/74S00	HI	1	25	20	100	50	20	50	50	50	50
54S/74S00	LO	20	12.5	10	111.11	50	10	40	200	40	200
54AS/74AS00	HI	2	50	40	200	100	40	100	100	100	100
54AS/74AS00	LO	20	12.5	10	111.11	50	10	40	200	40	200
54ALS/74ALS00A	HI	0.4	10	8	40	20	8	20	20	20	20
54ALS00A	LO	4	2.5	2	22.22	10	2	8	40	8	40
74ALS00A	LO	8	5	4	44.44	20	4	16	80	16	80
54AS1000	HI	40	1000	800	4000	2000	800	2000	2000	2000	2000
54AS1000	LO	40	25	20	222.22	100	20	80	400	80	400
74AS1000	HI	48	1200	960	4800	2400	960	2400	2400	2400	2400
74AS1000	LO	48	30	24	266.67	120	24	96	480	96	480
54ALS1000A	HI	1	25	20	100	50	20	50	50	50	50
54ALS1000A	LO	12	7.5	6	66.67	30	6	24	120	24	120
74ALS1000A	HI	2	65	52	260	130	52	130	130	130	130
74ALS1000A	LO	24	15	12	133.33	60	12	48	240	48	240

*Input Current HI
†Input Curent LO

Appendix B

Letter Symbols, Terms, and Definitions

These symbols, terms, and definitions are in accordance with those currently agreed upon by the JEDEC Council of the Electronics Industries Association (EIA) for use in the USA and by the International Electrotechnical Commission (IEC) for international use. The definitions are grouped into sections applying to voltages, currents, switching characteristics, and classification of circuit complexity.

VOLTAGES

V_{IH} High-level input voltage
An input voltage level within the more positive (less negative) of the two ranges of values used to represent the binary variables. A minimum value is specified which is the least-positive (most-negative) value of high-level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{IL} Low-level input voltage
An input voltage level within the less positive (more negative) of the two ranges of values used to represent the binary variables. A maximum value is specified which is the most-positive (least-negative) value of low-level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{T+} Positive-going threshold voltage
The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage rises from a level below the negative-going threshold voltage, V_{T-}.

V_{T-} Negative-going threshold voltage
The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage falls from a level above the positive-going threshold voltage, V_{T+}.

V_{OH} High-level output voltage
The voltage at an output terminal for a specified output current I_{OH} with input conditions applied that according to the product specification will establish a high level at the output.

V_{OL} Low-level output voltage
The voltage at an output terminal for a specified output current I_{OL} with input conditions applied that according to the product specification will establish a low level at the output.

$V_{O(on)}$ On-state output voltage
The voltage at an output terminal for a specified output current with input conditions applied that according to the product specification will cause the output switching element to be in the on state.

Note: This characteristic is usually specified only for outputs not having internal pull-up elements.

$V_{O(off)}$ Off-state output voltage
The voltage at an output terminal for a specified output current with input conditions applied that according to the specification will cause the output switching element to be in the off state.

Note: This characteristic is usually specified only for outputs not having internal pull-up elements.

CURRENT

I_{IH} High-level input current
The current flowing into* an input when a specified high-level voltage is applied to that input.

I_{IL} Low-level input current
The current flowing into* an input when a specified low-level voltage is applied to that input.

*Current flowing out of a terminal is a negative value.

I_{OH} **High-level output current**
The current flowing into* the output with a specified high-level output voltage V_{OH} applied.

Note: This parameter is usually specified for open-collector outputs intended to drive other logic circuits.

$I_{O(off)}$ **Off-state output current**
The current flowing into* an output with a specified output voltage applied and input conditions applied that according to the product specification will cause the output switching element to be in the off state.

Note: This parameter is usually specified for open-collector outputs intended to drive devices other than logic circuits or for three-state outputs.

I_{OS} **Short-circuit output current**
The current flowing into* an output when that output is short-circuited to ground (or other specified potential) with input conditions applied to establish the output logic level farthest from ground potential (or other specified potential).

I_{CCH} **Supply current, output(s) high**
The current flowing into* the V_{CC} supply terminal of a circuit when the reference output(s) is (are) at a high-level voltage.

I_{CCL} **Supply current, output(s) low**
The current flowing into* the V_{CC} supply terminal of a circuit when the reference output(s) is (are) at a low-level voltage.

DYNAMIC CHARACTERISTICS

f_{max} **Maximum clock frequency**
The highest rate at which the clock input of a bistable circuit can be driven through its required sequence while maintaining stable transitions of logic level at the output with input conditions established that should cause a change of output state with each clock pulse.

t_{HZ} **Output disable time (of a three-state output) from high level**
The time between the specified reference points on the input and output voltage waveforms with the three-state output changing from the defined high level to a high-impedance (off) state.

t_{LZ} **Output disable time (of a three-state output) from low level**
The time between the specified reference points on the input and output voltage waveforms with the three-state output changing from the defined low level to a high-impedance (off) state.

t_{PLH} **Propagation delay time, low-to-high-level output**
The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined low level to the defined high level.

t_{PHL} **Propagation delay time, high-to-low-level output**
The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined high level to the defined low level.

t_{TLH} **Transition time, low-to-high-level output**
The time between a specified low-level voltage and a specified high-level voltage on a waveform that is changing from the defined low level to the defined high level.

t_{THL} **Transition time, high-to-low-level output**
The time between a specified high-level voltage and a specified low-level voltage on a waveform that is changing from the defined high level to the defined low level.

t_w **Average pulse width**
The time between 50% amplitude points (or other specified reference points) on the leading and trailing edges of a pulse.

*Current flowing out of a terminal is a negative value.

t_h **Hold time**
The time interval for which a signal or pulse is retained at a specified input terminal after an active transition occurs at another specified input terminal.

$t_{release}$ **Release time**
The time interval between the release from a specified input terminal of data intended to be recognized and the occurrence of an active transition at another specified input terminal.

Note: When specified, the interval designated "release time" falls within the setup interval and constitutes, in effect, a negative hold time.

t_{su} **Setup time**
The time interval for which a signal is applied and maintained at a specified input terminal before an active transition occurs at another specified input terminal.

t_{ZH} **Output enable time (of a three-state output) to high level**
The time between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to the defined high level.

t_{ZL} **Output enable time (of a three-state output) to low level**
The time between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to the defined low level.

CLASSIFICATION OF CIRCUIT COMPLEXITY

Gate equivalent circuit
A basic unit-of-measure of relative digital-circuit complexity. The number of gate equivalent circuits is that number of individual logic gates that would have to be interconnected to perform the same function.

LSI **Large-scale integration**
A concept whereby a complete major subsystem or system function is fabricated as a single microcircuit. In this context a major subsystem or system, whether logical or linear, is considered to be one that contains 100 or more equivalent gates or circuitry of similar complexity.

MSI **Medium-scale integration**
A concept whereby a complete subsystem or system function is fabricated as a single microcircuit. The subsystem or system is smaller than for LSI, but whether digital or linear, is considered to be one that contains 12 or more equivalent gates or circuitry of similar complexity.

SSI **Small-scale integration**
Integrated circuits of less complexity than medium-scale integration (MSI).

*Current flowing out of a terminal is a negative value.

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Interface Circuits Data Book, 1981, 700 pages.
Includes specifications and applications information on TTL logic interface circuits, as well as product profiles on the line drivers/receivers and peripheral drivers.

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TMS7000 Family Data Manual, 1983, 350 pages.
Detailed specifications and application information on TI's family of microprogrammable 8-bit microcomputers. Includes architecture description, device operation, instruction set, electrical characteristics, and mechanical data. TMS7000 microcomputers include versions in CMOS and SMOS and with on-board UART.

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TMS32010, 1983, 160 pages.
TMS99000, 1983, 322 pages.
TMS7000, 1983, 160 pages.
Include general programming information, assembly instructions, assembler directives, assembler output, and application notes.

TMS32010 User's Guide, 1984, 400 pages.
Detailed application information on the TMS32010 Digital Signal Processor. Detailed reference manual on use of the TMS320 instruction set. Data sheets included.

Fundamentals of Microcomputer Design, 1982, 584 pages.
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