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The TTL Data Book

Volume 4

1985

Bipolar Programmable Logic and Memory

TEXAS INSTRUMENTS

The TTL Data Book
Volume 4

TEXAS
INSTRUMENTS

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Specifications contained in this data book supersede all data for these products published by TI in the US before January 1985.

General Information 1

Functional Index 2

Field-Programmable Logic 3

PROMs 4

RAMs and Memory-Based Code Converters 5

Designing with Texas Instruments Field-Programmable Logic 6

Mechanical Data 7

General Information 1

Functional Index 2

Field-Programmable Logic 3

PROMs 4

RAMs and Memory-Based Code Converters 5

Designing with Texas Instruments Field-Programmable Logic 6

Mechanical Data 7

INTRODUCTION

In this volume, Texas Instruments presents technical information on field-programmable logic and memory devices, including Programmable Array Logic (PAL®) circuits, Field-Programmable Logic Array (FPLA) devices, and Schottky† TTL memories (PROMs, RAMs, and memory-based code converters).

TI's line of programmable array logic products includes high-speed leadership circuits as well as standard PALs which are pin-compatible and functionally equivalent with other programmable logic array devices available. This volume includes specifications on existing and future products including:

- High-performance IMPACT PALs and low-power IMPACT PALs with leadership speed at 15 ns and 25 ns (max), respectively
- 20-Pin and 24-pin standard and half-power PALs
- High-complexity Latched and Registered input PALs and Exclusive-OR arrays
- Simple PALs

Each of these offer the designer significant reductions in "custom" design cycle time, as well as savings in board space by reducing SSI/MSI package count by as much as 5 to 1.

Specifications for TI's two high-performance field-programmable logic arrays, TIFPLA839 and '840, are also detailed. Designed with both programmable AND and programmable OR arrays, these functions contain 32 product terms and six sum terms. Each of the sum-of-products output functions can be programmed either active high (true) or active low (true). They provide high-speed, data-path logic replacement where several conventional SSI functions can be implemented with a single FPLA package. Product preview information on six field programmable logic sequencers (FPLS) has been included.

TI's family of high-performance Schottky TTL memories offers a wide variety of organizations providing efficient solutions for virtually any size microcontrol or program memory application. This volume contains information on TI's standard PROMs and new high-speed Series 3 IMPACT PROMs, including:

- 256-Bit, 1K, and 2K PROMs suitable for logic replacement
- Standard and low-power 512 × 8, 4K PROM, and 1024 × 8, 8K PROM
- Series 3 PROMs:
  - High-speed, 15ns, 32 × 8, 256-Bit PROM
  - 1K, 2K, 8K IMPACT PROMs in 4- or 8-Bit word width configurations
  - 2K × 8 and 4K × 4, 16K IMPACT PROMs, in both high-speed and low-power options

Series 3 PROMs feature high-speed access times and dependable titanium-tungsten fuse link programming elements in both low-density configurations for logic replacement, and high density configurations for high-performance memory application. Package options for these PROMs will include plastic and ceramic chip carriers as well as the standard DIPs. To achieve significant reductions in board space, TI offers the 16K, 2K × 8 Series 3 PROMs in a 300-mil, 24-pin DIP, and 28-pin chip carrier packages.

TI's leadership PAL ICs and Series 3 PROMs utilize our new advanced bipolar technology, IMPACT (IMPlanted Advanced Composed Technology). This unique innovation offers performance advantages in speed, power, and circuit density over preceding bipolar technologies and includes such features as:

- 2-μm Feature size
- 7-μ Metal pitch
- Walled emitter
- Ion implant
- Oxide isolation
- Composed masks

PAL is a registered trademark of Monolithic Memories Inc.
†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments, U.S. Patent Number 3,463,975.

A new Field Programmable Logic Application Report has been incorporated in this data book as a reference tool. It provides the first-time user of field-programmable logic with a basic understanding of this powerful semicustom logic.

Also included in this volume is a Functional Index to all bipolar digital device types available or under development. All logic technologies (TTL, S, LS, ALS, AS), field-programmable logic, programmable read-only memories, and bipolar complex LSI are also included. Logic symbols and pin assignments for all bipolar devices are shown in the Product Guide section of Volume 1 with typical performance data and chip carrier information.

While this volume offers design and specification data for bipolar programmable logic and memory components, complete technical data for any TI semiconductor product is available from your nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at 1-800-232-3200, ext. 951.

Field-Programmable Logic		Page
PAL16L8A	PAL16L8A-2	3-33
PAL16R4A	PAL16R4A-2	3-3
PAL16R6A	PAL16R6A-2	3-3
PAL16R8A	PAL16R8A-2	3-3
PAL20L8A	PAL20L8A-2	3-17
PAL20R4A	PAL20R4A-2	3-17
PAL20R6A	PAL20R6A-2	3-17
PAL20R8A	PAL20R8A-2	3-17
TIBPAL12H10		3-31
TIBPAL12L10		3-31
TIBPAL12P10		3-31
TIBPAL14H8		3-33
TIBPAL14L8		3-33
TIBPAL14P8		3-33
TIBPAL16H6		3-35
TIBPAL16L6		3-35
TIBPAL16L8-15	TIBPAL16L8-25	3-37
TIBPAL16L8-20	TIBPAL16L8-30	3-37
TIBPAL16P6		3-35
TIBPAL16R4-15	TIBPAL16R4-25	3-37
TIBPAL16R4-20	TIBPAL16R4-30	3-37
TIBPAL16R6-15	TIBPAL16R6-25	3-37
TIBPAL16R6-20	TIBPAL16R6-30	3-37
TIBPAL16R8-15	TIBPAL16R8-25	3-37
TIBPAL16R8-20	TIBPAL16R8-30	3-37
TIBPAL18H4		3-51
TIBPAL18L4		3-51
TIBPAL18P4		3-51
TIBPAL20H2		3-53
TIBPAL20L2		3-53
TIBPAL20L10-XX	TIBPAL20L10-YY	3-55
TIBPAL20P2		3-53
TIBPAL20X4-XX	TIBPAL20X4-YY	3-55
TIBPAL20X8-XX	TIBPAL20X8-YY	3-55
TIBPAL20X10-XX	TIBPAL20X10-YY	3-55
TIBPALR19L8-XX	TIBPALR19L8-YY	3-71
TIBPALR19R4-XX	TIBPALR19R4-YY	3-71
TIBPALR19R6-XX	TIBPALR19R6-YY	3-71
TIBPALR19R8-XX	TIBPALR19R8-YY	3-71
TIBPALT19L8-XX	TIBPALT19L8-YY	3-89
TIBPALT19R4-XX	TIBPALT19R4-YY	3-89
TIBPALT19R6-XX	TIBPALT19R6-YY	3-89
TIBPALT19R8-XX	TIBPALT19R8-YY	3-89
TIFPLA839		3-107
TIFPLA840		3-107
TIFPLS104		3-115
TIFPLS105		3-115
TIFPLS167		3-117
82S104A		3-119
82S105A		3-119
82S167A		3-121

PROMs	Page
TBP18S030	4-5
TBP18SA030	4-5
TBP24S10	4-11
TBP24S41	4-11
TBP24S81	4-11
TBP24SA10	4-11
TBP24SA41	4-11
TBP24SA81	4-11
TBP28L22	4-11
TBP28L42	4-11
TBP28L46	4-11
TBP28L86A	4-11
TBP28L166	4-11
TBP28LA22	4-11
TBP28S42	4-11
TBP28S46	4-11
TBP28S86A	4-11
TBP28S166	4-11
TBP28S2708A	4-11
TBP28SA42	4 11
TBP28SA46	4-11
TBP28SA86A	4-11
TBP34L10	4-39
TBP34L162	4-47
TBP34R162	4-35
TBP34S10	4-39
TBP34S162	4-47
TBP34SA10	4-39
TBP34SA162	4-47
TBP34SR165	4-55
TBP38L030	4-63
TBP38L22	4-81
TBP38L85	4-79
TBP38L165	4-71
TBP38L166	4-71
TBP38S030	4-63
TBP38S22	4-81
TBP38S85	4-79
TBP38S165	4-71
TBP38S166	4-71
TBP38SA030	4-63
TBP38SA22	4-81
TBP38SA85	4-79
TBP38SA165	4-71
TBP38SA166	4-71

ALPHANUMERICAL INDEX

RAMs and Memory-Based Code Converters		Page
	SN7489	5-3
SN54184	SN74184	5-9
SN54185A	SN74185A	5-9
SN54LS189A	SN74LS189A	5-19
SN54S189B	SN74S189B	5-25
	SN74S201	5-29
SN54LS219A	SN74LS219A	5-19
SN54284	SN74284	5-33
SN54285	SN74285	5-33
SN54LS289A	SN74LS289A	5-19
SN54S289B	SN74S289B	5-25
	SN74S301	5-29
SN54LS319A	SN74LS319A	5-19
SN54S484A	SN74S484A	5-37
SN54S485A	SN74S485A	5-37

INTRODUCTION

These symbols, terms and definitions are in accordance with those currently agreed upon by the JEDEC Council of the Electronic Industries Association (EIA) for use in the USA and by the International Electrotechnical Commission (IEC) for international use.

PART I — GENERAL CONCEPTS AND CLASSIFICATIONS OF CIRCUIT COMPLEXITY

Chip-Enable Input

A control input that when active permits operation of the integrated circuit for input, internal transfer, manipulation, refreshing, and/or output of data and when inactive causes the integrated circuit to be in reduced-power standby mode.
NOTE: See "chip-select input".

Chip-Select Input

A gating input that when inactive prevents input or output of data to or from an integrated circuit.
NOTE: See "chip-enable input".

Field-Programmable Logic Array (FPLA)

A user-programmable integrated circuit whose basic logic structure consists of a programmable AND array and whose outputs feed a programmable OR array.

Gate Equivalent Circuit

A basic unit-of-measure of relative digital-circuit complexity. The number of gate equivalent circuits is that number of individual logic gates that would have to be interconnected to perform the same function.

Large-Scale Integration (LSI)

A concept whereby a complete major subsystem or system function is fabricated as a single microcircuit. In this context a major subsystem or system, whether digital or linear, is considered to be one that contains 100 or more equivalent gates or circuitry of similar complexity.

Mask-Programmed Read-Only Memory

A read-only memory in which the data content of each cell is determined during manufacture by the use of a mask, the data content thereafter being unalterable.

Medium-Scale Integration (MSI)

A concept whereby a complete subsystem or system function is fabricated as a single microcircuit. The subsystem or system is smaller than for LSI, but whether digital or linear, is considered to be one that contains 12 or more equivalent gates or circuitry of similar complexity.

Memory Cell

The smallest subdivision of a memory into which a unit of data has been or can be entered, in which it is or can be stored, and from which it can be retrieved.

Memory Integrated Circuit

An integrated circuit consisting of memory cells and usually including associated circuits such as those for address selection, amplifiers, etc.

Output-Enable Input

A gating input that when active permits the integrated circuit to output data and when inactive causes the integrated circuit output(s) to be at a high impedance (off).

Programmable Array Logic (PAL)

A user-programmable integrated circuit which utilizes proven fuse link technology to implement logic functions. Implements sum of products logic by using a programmable AND array whose outputs feed a fixed OR array.

Programmable Read-Only Memory (PROM)

A read-only memory that after being manufactured can have the data content of each memory cell altered once only.

Random-Access Memory (RAM)

A memory that permits access to any of its address locations in any desired sequence with similar access time for each location.
NOTE: The term RAM, as commonly used, denotes a read/write memory.

Read/Write Memory

A memory in which each cell may be selected by applying appropriate electronic input signals and the stored data may be either (a) sensed at appropriate output terminals, or (b) changed in response to other similar electronic input signals.

Small-Scale Integration (SSI)

Integrated circuits of less complexity than medium-scale integration (MSI).

Typical (TYP)

A calculated value representative of the specified parameter at nominal operating conditions (V_{CC} = 5 V, TA = 25°C), based on the measured value of devices processed, to emulate the process distribution.

Very-Large-Scale Integration (VLSI)

A concept whereby a complete system function is fabricated as a single microcircuit. In this context, a system, whether digital or linear, is considered to be one that contains 3000 or more gates or circuitry of similar complexity.

Volatile memory

A memory the data content of which is lost when power is removed.

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PART 2 — OPERATING CONDITIONS AND CHARACTERISTICS (IN SEQUENCE BY LETTER SYMBOLS)

f_{max} **Maximum clock frequency**
The highest rate at which the clock input of a bistable circuit can be driven through its required sequence while maintaining stable transitions of logic level at the output with input conditions established that should cause changes of output logic level in accordance with the specification.

I_{CC} **Supply current**
The current into* the V_{CC} supply terminal of an integrated circuit.

I_{CCH} **Supply current, outputs high**
The current into* the V_{CC} supply terminal of an integrated circuit when all (or a specified number) of the outputs are at the high level.

I_{CCL} **Supply current, outputs low**
The current into* the V_{CC} supply terminal of an integrated circuit when all (or a specified number) of the outputs are at the low level.

I_{IH} **High-level input current**
The current into* an input when a high-level voltage is applied to that input.

I_{IL} **Low-level input current**
The current into* an input when a low-level voltage is applied to that input.

I_{OH} **High-level output current**
The current into* an output with input conditions applied that, according to the product specification, will establish a high level at the output.

I_{OL} **Low-level output current**
The current into* an output with input conditions applied that, according to the product specification, will establish a low level at the output.

I_{OS} (I_O) **Short-circuit output current**
The current into* an output when that output is short-circuited to ground (or other specified potential) with input conditions applied to establish the output logic level farthest from ground potential (or other specified potential).

I_{OZH} **Off-state (high-impedance-state) output current (of a three-state output) with high-level voltage applied**
The current flowing into* an output having three-state capability with input conditions established that, according to the product specification, will establish the high-impedance state at the output and with a high-level voltage applied to the output.
NOTE: This parameter is measured with other input conditions established that would cause the output to be at a low level if it were enabled.

I_{OZL} **Off-state (high-impedance-state) output current (of a three-state output) with low-level voltage applied**
The current flowing into* an output having three-state capability with input conditions established that, according to the product specification, will establish the high-impedance state at the output and with a low-level voltage applied to the output.
NOTE: This parameter is measured with other input conditions established that would cause the output to be at a high level if it were enabled.

*Current out of a terminal is given as a negative value.

GLOSSARY

V_{IH} **High-level input voltage**
An input voltage within the more positive (less negative) of the two ranges of values used to represent the binary variables.
NOTE: A minimum is specified that is the least-positive value of high-level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{IK} **Input clamp voltage**
An input voltage in a region of relatively low differential resistance that serves to limit the input voltage swing.

V_{IL} **Low-level input voltage**
An input voltage level within the less positive (more negative) of the two ranges of values used to represent the binary variables.
NOTE: A maximum is specified that is the most-positive value of low-level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{OH} **High-level output voltage**
The voltage at an output terminal with input conditions applied that, according to the product specification, will establish a high level at the output.

V_{OL} **Low-level output voltage**
The voltage at an output terminal with input conditions applied that, according to the product specification, will establish a low level at the output.

t_a **Access time**
The time interval between the application of a specific input pulse and the availability of valid signals at an output.

t_{dis} **Disable time (of a three-state output)**
The time interval between the specified reference points on the input and output voltage waveforms, with the three-state output changing from either of the defined active levels (high or low) to a high-impedance (off) state. (t_{dis} = t_{PHZ} or t_{PLZ}).

t_{en} **Enable time (of a three-state output)**
The time interval between the specified reference points on the input and output voltage waveforms, with the three-state output changing from a high-impedance (off) state to either of the defined active levels (high or low). (t_{en} = t_{PZH} or t_{PZL}).

t_h **Hold time**
The time interval during which a signal is retained at a specified input terminal after an active transition occurs at another specified input terminal.
NOTES: 1. The hold time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.
2. The hold time may have a negative value in which case the minimum limit defines the longest interval (between the release of the signal and the active transition) for which correct operation of the digital circuit is guaranteed.

t_{pd} **Propagation delay time**
The time between the specified reference points on the input and output voltage waveforms with the output changing from one defined level (high or low) to the other defined level. (t_{pd} = t_{PHL} or t_{PLH}).

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t_{PHL} **Propagation delay time, high-to-low level output**
The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined high level to the defined low level.

t_{PHZ} **Disable time (of a three-state output) from high level**
The time interval between the specified reference points on the input and output voltage waveforms with the three-state output changing from the defined high level to a high-impedance (off) state.

t_{PLH} **Propagation delay time, low-to-high-level output**
The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined low level to the defined high level.

t_{PLZ} **Disable time (of a three-state output) from low level**
The time interval between the specified reference points on the input and output voltage waveforms with the three-state output changing from the defined low level to a high-impedance (off) state.

t_{PZH} **Enable time (of a three-state output) to high level**
The time interval between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to the defined high level.

t_{PZL} **Enable time (of a three-state output) to low level**
The time interval between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to the defined low level.

t_{sr} **Sense recovery time**
The time interval needed to switch a memory from a write mode to a read mode and to obtain valid data signals at the output.

t_{su} **Setup time**
The time interval between the application of a signal at a specified input terminal and a subsequent active transition at another specified input terminal.

NOTES: 1. The setup time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed.
2. The setup time may have a negative value in which case the minimum limit defines the longest interval (between the active transition and the application of the other signal) for which correct operation of the digital circuit is guaranteed.

t_w **Pulse duration (width)**
The time interval between specified reference points on the leading and trailing edges of the pulse waveform.

EXPLANATION OF FUNCTION TABLES

The following symbols are used in function tables on TI data sheets:

H	=	high level (steady state)
L	=	low level (steady state)
↑	=	transition from low to high level
↓	=	transition from high to low level
→	=	value/level or resulting value/level is routed to indicated destination
↶	=	value/level is re-entered
X	=	irrelevant (any input, including transitions)
Z	=	off (high-impedance) state of a 3-state-output
a..h	=	the level of steady-state inputs at inputs A through H respectively
Q_0	=	level of Q before the indicated steady-state input conditions were established
$\overline{Q}_0$	=	complement of Q_0 or level of $\overline{Q}$ before the indicated steady-state input conditions were established
Q_n	=	level of Q before the most recent active transition indicated by ↓ or ↑
⎍	=	one high-level pulse
⎎	=	one low-level pulse
TOGGLE	=	each output changes to the complement of its previous level on each transition indicated by ↓ or ↑.

If, in the input columns, a row contains only the symbols H, L, and/or X, this means the indicated output is valid whenever the input configuration is achieved and regardless of the sequence in which it is achieved. The output persists so long as the input configuration is maintained.

If, in the input columns, a row contains H, L, and/or X together with ↑ and/or ↓, this means the output is valid whenever the input configuration is achieved but the transition(s) must occur following the achievement of the steady-state levels. If the output is shown as a level (H, L, Q_0, or $\overline{Q}_0$), it persists so long as the steady-state input levels and the levels that terminate indicated transitions are maintained. Unless otherwise indicated, input transitions in the opposite direction to those shown have no effect at the output. (If the output is shown as a pulse, ⎍ or ⎎, the pulse follows the indicated input transition and persists for an interval dependent on the circuit.)

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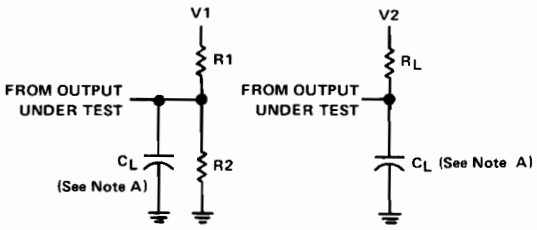
PARAMETER MEASUREMENT INFORMATION

FOR THREE-STATE OUTPUTS AND BI-STATE TOTEM-POLE OUTPUTS



LOAD CIRCUIT

THEVENIN EQUIVALENT CIRCUIT

VOLTAGE VALUES

MEASUREMENTS	V_{CC}	V1	V2
t_{PLH} and t_{PHL}	5.5 V	5.5 V	3.7 V
	5.25 V	5.25 V	3.5 V
	4.75 V	4.75 V	3.2 V
	4.5 V	4.5 V	3 V
t_{PHZ} and t_{PZH}	ALL	0 V	0 V
t_{PLZ} and t_{PZL}	ALL	5 V	3.3 V

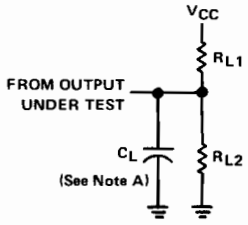
RESISTOR VALUES

I_{OL}MAX†	R1	R2	R_L
24 mA	200 Ω	400 Ω	133 Ω
20 mA	240 Ω	480 Ω	160 Ω
16 mA	300 Ω	600 Ω	200 Ω
12 mA	400 Ω	800 Ω	267 Ω
8 mA	600 Ω	1.2 kΩ	400 Ω

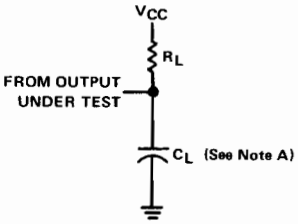
†See Recommended Operating Conditions.

NOTE A: C_L includes probe and jig capacitance.

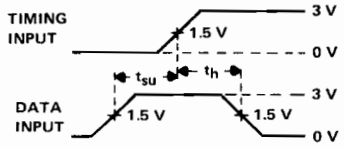
FOR OPEN-COLLECTOR OUTPUTS



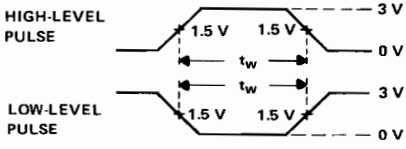
TEST CIRCUIT FOR USE WHEN R_{L1} AND R_{L2} ARE SPECIFIED



TEST CIRCUIT FOR USE WHEN SINGLE R_L IS SPECIFIED

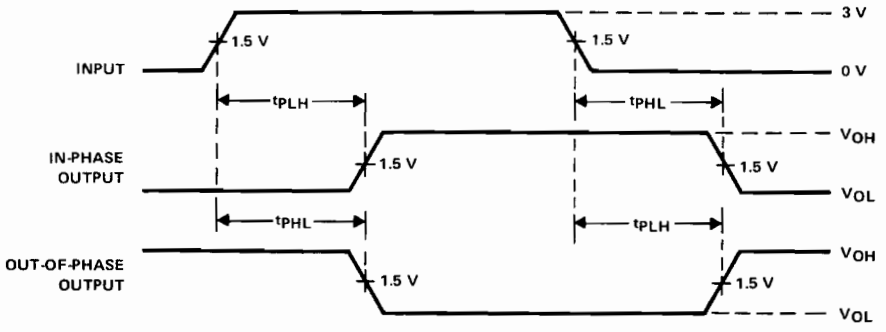


VOLTAGE WAVEFORMS SETUP AND HOLD TIMES

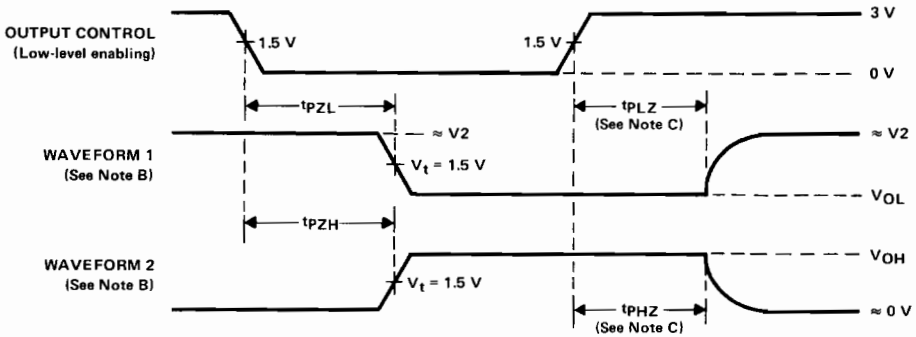


VOLTAGE WAVEFORMS PULSE WIDTHS

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

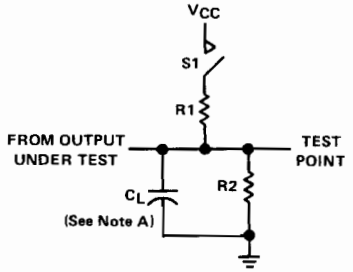
C. TI normally measures t_{PLZ} and t_{PHZ} by reading at the 1.5-volt (V_t) point on the waveform and subtracting the RC time from the reading.
For t_{PLZ}, RCin $\dfrac{V2 - V_{OL\ max}}{V2 - V_t}$ is subtracted from the reading.

For t_{PHZ}, RCin $\dfrac{V_{OH^{min}}}{V_t}$ is subtracted from the reading.

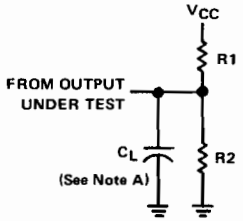
D. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.

E. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_{out} \approx 50\ \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT FOR THREE-STATE OUTPUTS



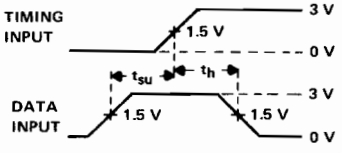
LOAD CIRCUIT FOR OPEN-COLLECTOR OUTPUTS

RESISTOR VALUES

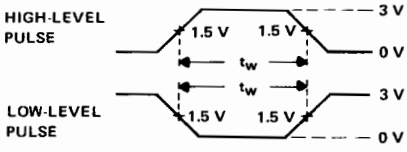
I_{OL} MAX†	R1*	R2*
24 mA	200 Ω	400 Ω
20 mA	240 Ω	480 Ω
16 mA	300 Ω	600 Ω
12 mA	400 Ω	800 Ω
8 mA	600 Ω	1.2 kΩ

†See Recommended Operating Conditions.
*Unless otherwise specified.

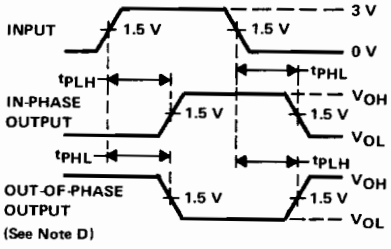
NOTE A: C_L includes probe and jig capacitance.



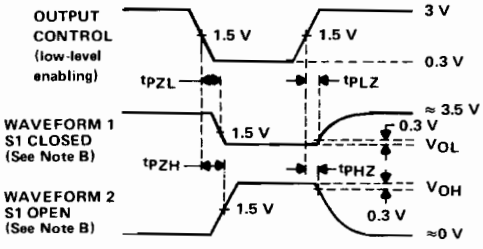
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PULSE WIDTHS



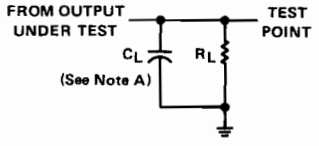
VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



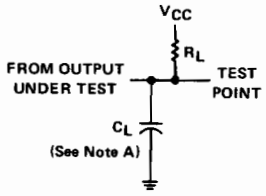
VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.

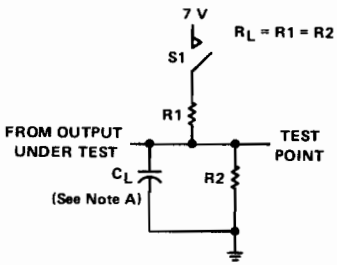
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT FOR BI-STATE TOTEM-POLE OUTPUTS

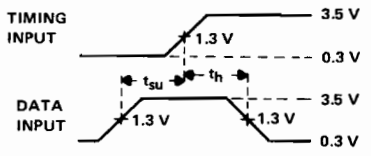


LOAD CIRCUIT FOR OPEN-COLLECTOR OUTPUTS

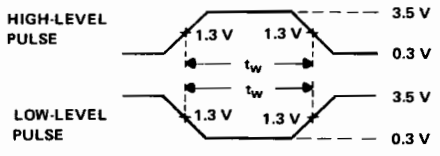


LOAD CIRCUIT FOR THREE-STATE OUTPUTS

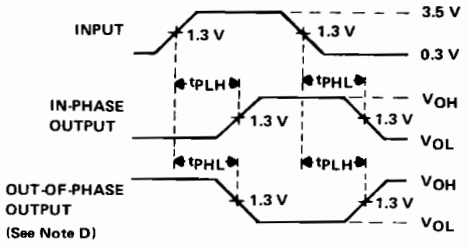
NOTE A: C_L includes probe and jig capacitance.



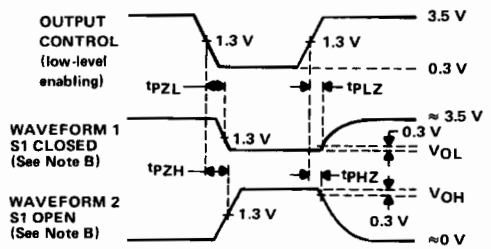
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PULSE WIDTHS



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.

RAM AND MEMORY-BASED CODE CONVERTERS NUMBERING SYSTEM AND ORDERING INSTRUCTIONS

Electrical characteristics presented in this data book, unless otherwise noted, apply for circuit type(s) listed in the page heading regardless of package. the availability of a circuit function in a particular package is denoted by an alphabetical reference above the pin-connection diagram(s). These alphabetical references refer to mechanical outline drawings shown in this section.

Factor orders for circuits described in this catalog should include a four-part type number as explained in the following example.

EXAMPLE: **SN** **54LS189A** **J** **-00**

Prefix

Must contain two to four letters

SN = Standard Prefix

Unique Circuit Description

Must contain four to eight characters

Examples:

7489
54185A
74LS319A
54S189B

Package

Must contain one or two letters

J, JD, JT, JW, N, NT, NW (Dual-in-line packages)†
(From pin-connection diagram on individual data sheet)

Instructions (Dash No.)

Must contain two numbers

– 00 No special instructions
– 10 Solder-dipped leads (N and NT packages only)

†These circuits in dual-in-line packages are shipped in one of the carriers shown below. Unless a specific method of shipment is specified by the customer (with possible additional costs), circuits will be shipped in the most practical carrier. Please contact your TI sales representative for the method that will best suit your particular needs.

Dual-in-line (J, JD, JT, JW, N, NT, NW)

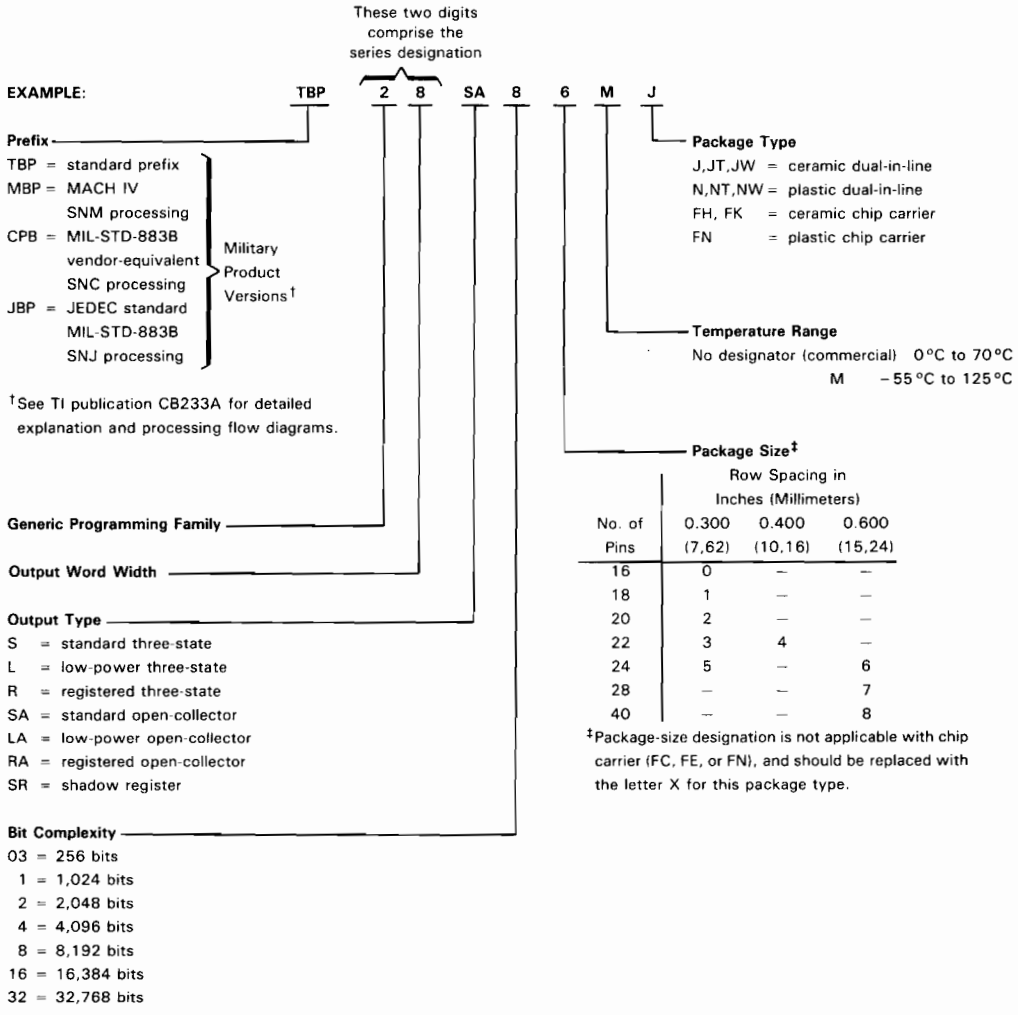
– Slide Magazines
– A-Channel Plastic Tubing
– Barnes Carrier (N only)
– Sectioned Cardboard Box
– Individual Plastic Box

ORDERING INFORMATION

PROM NUMBERING SYSTEM AND ORDERING INSTRUCTIONS

To complement Texas Instruments continually expanding line of bipolar PROMs, a new numbering system is being implemented. This system provides the user with information regarding the generic programming family, bit density, organization, temperature range, and the size and type of package without the necessity of looking up this information in tables. Below is a guide for use of this new numbering system.

Factory orders for PROMs described in this book should include a type number as explained in the following example.



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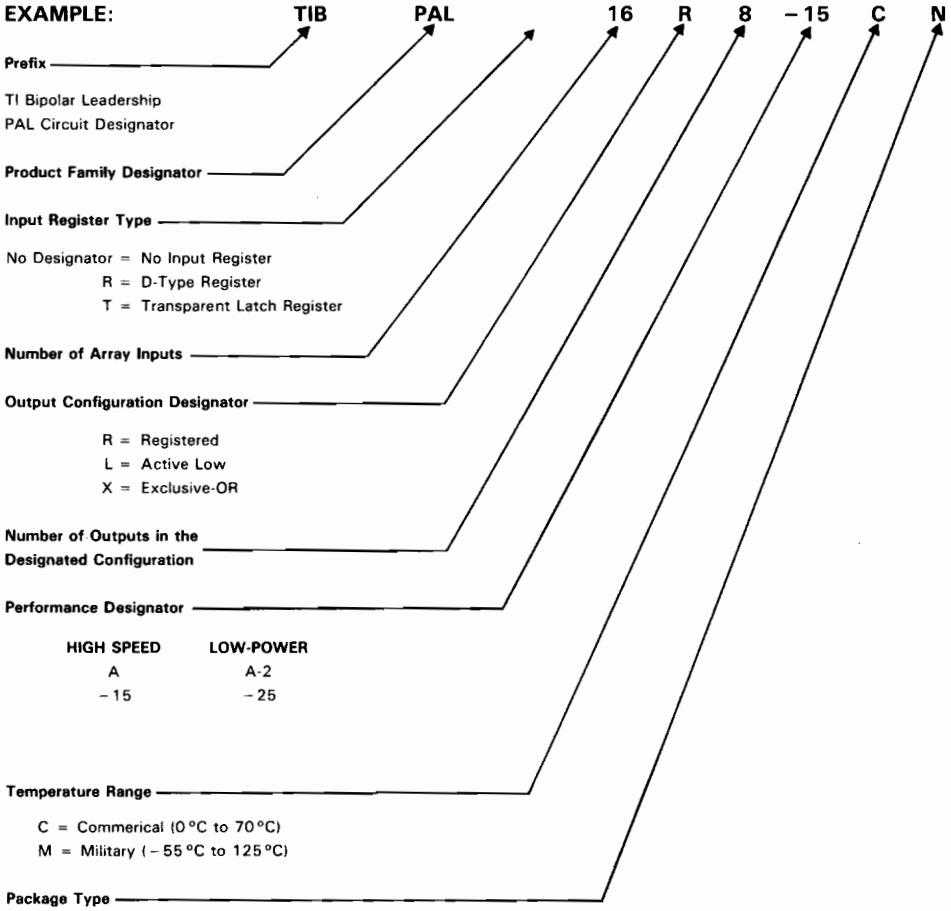
PAL® NUMBERING SYSTEM AND ORDERING INSTRUCTIONS

Factory orders for leadership PAL® circuits described in this catalog should include a nine-part type number as explained in the example below. Exclude the prefix when ordering standard PALs.



PAL is a registered trademark of Monolithic Memories Inc.

ADDRESS FOR PAL AND FPLA PROGRAMMING AND SOFTWARE MANUFACTURERS*

HARDWARE MANUFACTURERS

Citel
3060 Raymond St.
Santa Clara, CA 95050
(408) 727-6562

DATA I/O
10525 Willows Rd.
Redmond, WA 98052
(206) 881-6444

DIGITAL MEDIA
3178 Gibralter Ave.
Costa Mesa, CA 92626
(714) 751-1373

Kontron Electronics
630 Price Avenue
Redwood City, CA 94063
(415) 361-1012

Stag Micro Systems
528-5 Weddell Drive
Sunnyvale, CA 94086
(408) 745-1991

Storey Systems
3201 N. Hwy 67, Suite H
Mesquite, TX 75150
(214) 270-4135

Structured Design
1700 Wyatt Dr., Suite 7
Santa Clara, CA 95054
(408) 988-0725

Sunrise Electronics
524 S. Vermont Avenue
Glendora, CA 91740
(213) 914-1926

Valley Data Sciences
2426 Charleston Rd.
Mountain View, CA 94043
(415) 968-2900

Varix
1210 Campbell Rd.
Richardson, TX 75081
(214) 437-0777

Wavetec/Digelec
586 Weddel Dr. Suite 1
Sunnyvale, CA 94089
(408) 745-0722

SOFTWARE MANUFACTURERS

Assisted Technologies (CUPL)
2381 Zanker Road, Suite 150
Santa Clara, CA 95050
(408) 942-8787

DATA I/O (ABEL)
10525 Willows Rd.
Redmond, WA 98052
(206) 881-6444

Monolithic Memories Inc. (PALASM)
2175 Mission College Blvd.
Santa Clara, CA 95050
(408) 970-9700

*Texas Instruments does not endorse or warrant the suppliers referenced. Presently, Texas Instruments has certified DATA I/O, Sunrise, Structured Design and Digital Media. Other programmers are now in the certification process. For a current list of certified programmers, please contact your local TI sales representative.

ADDRESS FOR PROM PROGRAMMING AND SOFTWARE MANUFACTURERS*

HARDWARE MANUFACTURERS

Citel
3060 Raymond St.
Santa Clara, CA 95050
(408) 727-6562

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10525 Willows Rd.
Redmond, WA 98052
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586 Weddel Dr., Suite 1
Sunnyvale, CA 94089
(408) 745-0722

SOFTWARE MANUFACTURERS

Assisted Technologies (CUPL)
2381 Zanker Road, Suite 150
Santa Clara, CA 95050
(408) 942-8787

DATA I/O (ABEL), (PROMLINK)
10525 Willows Rd.
Redmond, WA 98052
(206) 881-6444

Monolithic Memories Inc. (PLEASM)
2175 Mission College Blvd.
Santa Clara, CA 95050
(408) 970-9700

*Texas Instruments does not endorse or warrant the suppliers referenced. Presently, Texas Instruments has certified DATA I/O. Other programmers are now in the certification process. For a current list of certified programmers, please contact your local TI sales representative.

General Information 1

Functional Index 2

Field-Programmable Logic 3

PROMs 4

RAMs and Memory-Based Code Converters 5

Designing with Texas Instruments Field-Programmable Logic 6

Mechanical Data 7

GATES AND INVERTERS

POSITIVE-NAND GATES AND INVERTERS

DESCRIPTION	TYPE	TECHNOLOGY							VOLUME
		STD TTL	ALS	AS	H	L	LS	S	
Hex 2 Input Gates	'804		●	B					CF
Hex Inverters	'04	●			●	●	●	●	2
			A	●					3
	'1004		●	●					
Quadruple 2 Input Gates	'00	●			●	●	●	●	2
			A	●					3
	'1000		A	●					
Triple 3 Input Gates	'10	●			●	●	●	●	2
			A	●					3S
	'1010		A						3
Dual 4 Input Gates	'20	●			●	●	●	●	2
			A	●					3
	'1020		A						
8 Input Gates	'30	●			●	●	●	●	2
			A	●					3S
13-Input Gates	'133							●	2
Dual 2 Input Gates	'8003		●						3

POSITIVE-NAND GATES AND INVERTERS WITH OPEN-COLLECTOR OUTPUTS

DESCRIPTION	TYPE	TECHNOLOGY							VOLUME
		STD TTL	ALS	AS	H	L	LS	S	
Hex Inverters	'05	●			●		●	●	2
			A						3
	'1005		●						
Quadruple 2-Input Gates	'01	●			●		●		2
			●						3
	'03	●				●	●	●	2
			A						3
	'1003		A						
Triple 3 Input Gates	'12	●					●		2
			A						3S
Dual 4 Input Gates	'22	●			●		●	●	2
			B						3S

POSITIVE-AND GATES

DESCRIPTION	TYPE	TECHNOLOGY							VOLUME
		STD TTL	ALS	AS	H	L	LS	S	
Hex 2 Input Gates	'808		●	B					CF
Quadruple 2 Input Gates	'08	●					●	●	2
			●	●					3
	'1008		A	●					
Triple 3 Input Gates	'11					●	●	●	2
			A	●					3S
	'1011		A						3
Dual 4 Input Gates	'21						●		2
			●	●					3
Triple 4 Input AND/NAND	'800			▲					

POSITIVE AND GATES WITH OPEN-COLLECTOR OUTPUTS

DESCRIPTION	TYPE	TECHNOLOGY						VOLUME
		STD TTL	ALS	AS	H	LS	S	
Quadruple 2 Input Gates	'09	●				●	●	2
			●					3
Triple 3 Input Gates	'15				●	●	●	2
			●					3

POSITIVE-OR GATES

DESCRIPTION	TYP	TECHNOLOGY					VOLUME
		STD TTL	ALS	AS	LS	S	
Hex 2 Input Gates	'832		●	B			CF
Quadruple 2 Input Gates	'32	●			●	●	2
			●	●			3
	'1032		A	●			
Triple 4 Input OR/NOR	'802			▲			

POSITIVE-NOR GATES

DESCRIPTION	TYPE	TECHNOLOGY						VOLUME
		STD TTL	ALS	AS	L	LS	S	
Hex 2 Input Gates	'805		●	B				CF
Quadruple 2 Input Gates	'02	●			●	●	●	2
			●	●				3
	1002		A					
Triple 3-Input Gates	'27	●				●		2
			●	●				3
Dual 4-Input Gates with Strobe	'25	●						2
Dual 5-Input Gates	'260						●	

SCHMITT-TRIGGER POSITIVE-NAND GATES AND INVERTERS

DESCRIPTION	TYPE	TECHNOLOGY					VOLUME
		STD TTL	ALS	AS	LS	S	
Hex Inverters	'14	●			●		2
	'19				●		
Octal Inverters	'619				●		
Dual 4 Input Positive NAND	'13	●			●		
	18				●		
Triple 4 Input Positive NAND	'618				●		
Quadruple 2 Input Positive NAND	'24				●		
	'132	●			●	●	

CURRENT-SENSING GATES

DESCRIPTION	TYPE	TECHNOLOGY			VOLUME
		ALS	AS	LS	
Hex	'63			●	2

DELAY ELEMENTS

DESCRIPTION	TYP	TECHNOLOGY			VOLUME
		ALS	AS	LS	
Inverting and Noninverting Elements, 2 Input NAND Buffers	'31			●	2

CF Denotes contact factory
● Denotes available technology.
▲ Denotes planned new products.
A Denotes "A" suffix version available in the technology indicated.
B Denotes "B" suffix version available in the technology indicated.
S Denotes supplement to data book.

GATES, EXPANDERS, BUFFERS, DRIVERS, AND TRANSCEIVERS

AND-OR-INVERT GATES

DESCRIPTION	TYPE	TECHNOLOGY							VOLUME
		STD TTL	ALS	AS	H	L	LS	S	
2-Wide 4-Input	'55				●	●	●		2
4-Wide 4-2-3-2-Input	'64							●	
4-Wide 2-2-3-2-Input	'54				●				
4-Wide 2-Input	'54	●							
4-Wide 2-3-3-2-Input	'54					●	●		
Dual 2-Wide 2-Input	'51	●			●	●	●	●	

AND-OR-INVERT GATES WITH OPEN-COLLECTOR OUTPUTS

DESCRIPTION	TYPE	TECHNOLOGY				VOLUME
		STD TTL	ALS	AS	S	
4-Wide 4-2-3-2-Input	'65				●	2

EXPANDABLE GATES

DESCRIPTION	TYPE	TECHNOLOGY						VOLUME
		STD TTL	ALS	AS	H	L	LS	
Dual 4-Input Positive-NOR With Strobe	23	●						2
4-Wide AND-OR	'52				●			
4-Wide AND-OR-INVERT	'53	●			●			
2-Wide AND-OR-INVERT	'55				●	●	●	
Dual 2-Wide AND-OR-INVERT	'50	●			●			

EXPANDERS

DESCRIPTION	TYPE	TECHNOLOGY				VOLUME
		STD TTL	ALS	AS	H	
Dual 4-Input	'60	●			●	2
Triple 3-Input	'61				●	
3-2-2-3-Input AND-OR	'62				●	

BUFFER AND INTERFACE GATES WITH OPEN-COLLECTOR OUTPUTS

DESCRIPTION	TYPE	TECHNOLOGY					VOLUME
		STD TTL	ALS	AS	LS	S	
Hex	'07	●					2
	'17	●					
	'35		●				35
	1035		●				3
Hex Inverter	'06	●					2
	'16	●					
	1005		●				3
Quad 2-Input Positive-NAND	26	●					2
	38	●			●	●	
			A				3
	'39	●					2
	1003		A				3
Quad 2-Input Positive-NOR	33	●			●		2
			A				3

BUFFERS, DRIVERS, AND BUS TRANSCEIVERS WITH OPEN-COLLECTOR OUTPUTS

DESCRIPTION	TYPE	TECHNOLOGY					VOLUME
		STD TTL	ALS	AS	LS	S	
Noninverting Octal Buffers Drivers	743		▲				CF
	757			●			35
	760			●			
Inverting Octal Buffers Drivers	742		▲				CF
	756			●			35
	763			●			
Inverting and Noninverting Octal Buffers Drivers	762			●			
Noninverting Quad Transceivers	759			●			
Inverting Quad Transceivers	758			●			

GATES, BUFFERS, DRIVERS, AND BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

DESCRIPTION	TYPE	TECHNOLOGY					VOLUME
		STD TTL	ALS	AS	LS	S	
Noninverting Octal Buffers Drivers	'241				●	●	2
			A	●			3
	'244				●	●	2
			A	●			3
	'465				●		2
			A				3
	'467				●		2
			A				3
	'541				●		2
			●				CF
	'1241[f]		▲				3
	'1244[f]		A				
Inverting Octal Buffers Drivers	231			●			2
	240				●	●	
			A	●			3
	466				●		2
			A				3
	'468				●		2
			A				3
	540				●		2
			●				CF
	'1240[f]		●				3
Inverting and Noninverting Octal Buffers Drivers	230			●			
Octal Transceivers	'245				●		2
			A	▲			3
	1245		A				3S
Noninverting Hex Buffers Drivers	'365	A			A		2
			▲				3
	367	A			A		2
			▲				3
Inverting Hex Buffers Drivers	366	A			A		2
			▲				3
	'368	A			A		2
			▲				3
Quad Buffers Drivers with Independent Output Controls	'125	●			A		2
	126	●			A		
	425	●					
	426	●					
Noninverting Quad Transceivers	243				●		3
			A	●			
	1243[f]		▲				
Inverting Quad Transceivers	'242				●		2
			A	●			3
	1242[f]		▲				
Quad Transceivers with Storage	226					●	2
12-Input NAND Gate	134					●	
Controller and Bus Driver for 8080A System	428					●	

50-OHM/75-OHM LINE DRIVERS

DESCRIPTION	TYPE	TECHNOLOGY				VOLUME
		STD TTL	ALS	AS	S	
Hex 2-Input Positive-NAND	'804		●	B		CF
Hex 2-Input Positive-NOR	'805		●	B		
Hex 2-Input Positive-AND	'808		●	B		
Hex 2-Input Positive-OR	'832		●	B		
Quad 2-Input Positive-NOR	'128	●				2
Dual 4-Input Positive-NAND	'140				●	

CF Denotes Contact Factory
● Denotes available technology.
▲ Denotes planned new products.
[f] Denotes very low power.
A Denotes "A" suffix version available in the technology indicated.
S Denotes supplement to data book.

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

BUFFERS, DRIVERS, TRANSCEIVERS, AND CLOCK GENERATORS

BUFFERS, CLOCK/MEMORY DRIVERS

DESCRIPTION	TYPE	TECHNOLOGY						VOLUME
		STD TTL	ALS	AS	H	LS	S	
Hex 2-Input Positive-NAND	'804		●	B				CF
Hex 2-Input Positive-NOR	'805		●	B				
Hex 2-Input Positive-AND	'808		●	B				
Hex 2-Input Positive-OR	'832		●	B				
Hex Inverter	'1004		●	●				3
Hex Buffer	'34		▲	●				
	'1034		●	●				
Quad 2-Input Positive-NAND	'37	●				●	●	2
			A					3
	'1000		A	●				
Quad 2-Input Positive-NOR	'28	●				●		2
			A					3
	'1002		A					
	'1036			●				
Quad 2-Input Positive-AND	'1008		A	●				
Quad 2-Input Positive-OR	'1032		A	●				
Triple 3-Input Positive-NAND	'1010		A					
Triple 3-Input Positive-AND	'1011		A					
Triple 4-Input AND-NAND	'800			▲				
Triple 4-Input OR-NOR	'802			▲				
Dual 4-Input Positive-NAND	'40	●				●	●	2
			A					3
	'1020		A					
Line Driver/Memory Driver with Series Damping Resistor	'436						●	2
Line Driver/Memory Driver	'437						●	

BI-/TRI-DIRECTIONAL BUS TRANSCEIVERS AND DRIVERS

DESCRIPTION	TYPE OF OUTPUT	TYPE	TECHNOLOGY				VOLUME
			ALS	AS	LS	S	
Quad with Bit Direction Controls	3-State	'446			●		2
	3-State	'449			●		
Quad Tridirection	OC	'440			●		
	OC	'441			●		
	3 State	'442			●		
	3 State	'443			●		
	3-State	'444			●		
	OC	'448			●		
4 Bit with Storage	3 State	'226				●	

OCTAL BUS TRANSCEIVERS/MOS DRIVERS

DESCRIPTION	TYPE	TECHNOLOGY					VOLUME
		STD TTL	ALS	AS	LS	S	
Inverting Outputs, 3 State	'2620			●			3
	2640			●			
True Outputs 3 State	'2823			●			
	'2645			●			

OCTAL BUFFERS AND LINE DRIVERS WITH INPUT/OUTPUT RESISTORS

DESCRIPTION		TYPE	TECHNOLOGY					VOLUME
			STD TTL	ALS	AS	LS	S	
Input Resistors	Inverting Outputs	746		▲				CF
	Noninverting Outputs	747		▲				
Output Resistors	Inverting Outputs	'2540		●				
	Noninverting Outputs	'2541		●				

OCTAL BI-/TRI-DIRECTIONAL BUS TRANSCEIVERS

DESCRIPTION		TYPE OF OUTPUT	TYPE	TECHNOLOGY			VOLUME
				ALS	AS	LS	
12 mA 24 mA 48 mA 64 mA Sink True Outputs	Low Power	3 State	245	A	●		3
						●	2
		OC	621	A	●		3S
						●	2
		3 State	623	A	●		3S
						●	2
		OC 3 State	639	A	●		3
						●	2
		3 State	652	▲	●		3S
						●	2
		OC 3 State	654	▲			3
						●	2
	Very Low Power	OC	'621	▲			3
		3 State	1623	▲			
		OC 3 State	1639	▲			
12 mA 24 mA 48 mA 64 mA Sink Inverting Outputs	Low Power	3 State	620	A	●		3S
						●	2
		OC	622	A	●		3S
						●	2
		OC 3 State	638	A	●		3
						●	2
		3 State	651	▲	●		3S
						●	2
		OC 3 State	653	▲			3
						●	2
	Very Low Power	3 State	1620	▲			3
		OC	1622	▲			
		OC 3 State	1638	▲			
12 mA 24 mA 48 mA 64 mA Sink True Outputs	Low Power	OC	641	A	●		3
						●	2
		3 State	645	A	●		3
						●	2
	Very Low Power	OC	'642	▲			3
		3 State	1645	A			
12 mA 24 mA 48 mA 64 mA Sink Inverting Outputs	Low Power	3 State	640	A	●		3
						●	2
		OC	642	A	●		3
						●	2
	Very Low Power	3 State	1640	A			3
		OC	'642	▲			
12 mA 24 mA 48 mA 64 mA Sink True and Inverting Outputs	Low Power	3 State	643	A	●		3
						●	2
		OC	644	A	●		3
						●	2
	Very Low Power	3 State	1643	▲			3
		OC	1644	▲			
Registered Arith Multiples 12 mA 24 mA 48 mA 64 mA True Outputs		3 State	646	▲	●		3S
						●	2
		OC	647	▲			3
						●	2
Registered with Multiplexed 12 mA 24 mA 48 mA 64 mA Inverting Outputs		3 State	648	▲	●		3S
						●	2
		OC	649	▲			3
						●	2
Universal Transceiver Port Controllers		3 State	877		●		3S
			852		●		CF
			856		●		

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FLIP-FLOPS

DUAL AND SINGLE FLIP FLOPS

DESCRIPTION	TYPE	TECHNOLOGY							VOLUME
		STD TTL	ALS	AS	H	L	LS	S	
Dual J K Edge Triggered	73						A		2
	76						A		
	78						A		
	103				●				
	106				●				
	107						A		
	108				●				
	109	●					A		
			A	●					4S
	112						A	●	2
			A	▲					3
	113						A	●	2
			A	▲					3
	114						A	●	2
			A	▲					3
Single J K Edge Triggered	70	●							2
	101				●				
	102				●				
Dual Pulse Triggered	73	●			●	●			
	76	●			●				
	78				●	●			
	107	●							
Single Pulse Triggered	71				●	●			
	72	●			●	●			
	104	●							
	105	●							
Dual J K with Data Lockout	111	●							
Single J K with Data Lockout	110	●							
Dual D Type	74	●			●	●	A	●	
			A	●					4S

QUAD AND HEX FLIP FLOPS

DESCRIPTION	NO OF FFs	OUTPUTS	TYPE	TECHNOLOGY					VOLUME
				STD TTL	ALS	AS	LS	S	
D Type	6	Q	174	●			●	●	2
			378		●	●			3
	4	Q	171				●		2
		Q $\bar{Q}$	175	●			●	●	
			379		●	●			4S
J K	4	Q	276	●			●		2
			376	●					

OCTAL, 9 BIT, AND 10 BIT D TYPE FLIP FLOPS

DESCRIPTION	NO OF BITS	OUTPUT	TYPE	TECHNOLOGY					VOLUME
				STD TTL	ALS	AS	LS	S	
True Data	Octal	3 State	374		●	●			3
		3 State	574		●	●	●	●	2
True Data with Clear	Octal	2 State	273		●				3
		3 State	575	●			●		2
		3 State	874		●	●			3
		3 State	878		●	●			
True with Enable	Octal	2 State	377				●		2
Inverting	Octal	3 State	534		●	●			4
		3 State	564		●				
		3 State	576		●	●			
Inverting with Clear	Octal	3 State	577		●	●			
		3 State	879		●	●			
Inverting with Preset	Octal	3 State	876		●	●			
True	Octal	3 State	825			●			CF
Inverting	Octal	3 State	826			●			
True	9 Bit	3 State	823			●			
Inverting	9 Bit	3 State	824			●			
True	10 Bit	3 State	821			●			
Inverting	10 Bit	3 State	822			●			

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LATCHES AND MULTIVIBRATORS

QUAD LATCHES

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY					VOLUME
			STD TTL	ALS	AS	L	LS	
Dual 2-Bit Transparent	2 State	75	●			●	●	2
	2 State	77	●			●	●	
	2 State	375					●	
S-R	2 State	279	●				A	

RETRIGGERABLE MONOSTABLE MULTIVIBRATORS

DESCRIPTION	TYPE	TECHNOLOGY					VOLUME
		STD TTL	ALS	AS	LS	L	
Single	122	●			●	●	2
	130	●					
	422				●		
Dual	123	●			●	●	
	423				●		

D-TYPE OCTAL, 9 BIT, AND 10-BIT RAD-BACK LATCHES

DESCRIPTION	NO. OF BITS	TYPE	TECHNOLOGY					VOLUME
			STD TTL	ALS	AS	LS	S	
Edge Triggered Inverting and Noninverting	Octal	996		▲				5
Transparent True	Octal	990		▲				
	9 Bit	992		▲				
	10 Bit	994		▲				
Transparent Noninverting	Octal	991		▲				
	9 Bit	992		▲				
	10 Bit	994		▲				
Transparent with Clear True Outputs	Octal	666		▲				
Transparent with Clear Inverting Outputs	Octal	667		▲				

OCTAL, 9 BIT, AND 10 BIT LATCHES

DESCRIPTION	NO. OF BITS	OUTPUT	TYPE	TECHNOLOGY					VOLUME
				STD TTL	ALS	AS	LS	S	
Transparent	Octal	3 State	268					●	2
			373				●	●	
					●	●			3
		3 State	573		●	●			
Dual 4-Bit Transparent	Octal	2 State	100	●					2
		2 State	116	●					
		3 State	873		●	●			
Inverting Transparent	Octal	3 State	533		●	●			3
		3 State	563		●				
		3 State	580		●	●			
Dual 4-Bit Inverting Transparent	Octal	3 State	880		●	●			
2-Input Multiplexed	Octal	3 State	604				●		2
		OC	605				●		
		3 State	606				●		
		OC	607				●		
Addressable	Octal	2 State	259	●			●		3
Multi-Mode Buffered	Octal	3 State	412					●	2
True	Octal	3 State	845		▲	●			3S & 5
Inverting	Octal	3 State	846		▲	●			
True	9 Bit	3 State	843		▲	●			
Inverting	9 Bit	3 State	844		▲	●			
True	10 Bit	3 State	841		▲	●			
Inverting	10 Bit	3 State	842		▲	●			

MONOSTABLE MULTIVIBRATORS WITH SCHMITT TRIGGER INPUTS

DESCRIPTION	TYPE	TECHNOLOGY					VOLUME
		STD TTL	ALS	AS	LS	S	
Single	121	●					2
Dual	221	●			●		

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REGISTERS

SHIFT REGISTERS

DESCRIPTION	NO OF BITS	MODES S/R	MODES S/L	MODES LOAD	MODES HOLD	TYPE	TECHNOLOGY STD TTL	TECHNOLOGY ALS	TECHNOLOGY AS	TECHNOLOGY L	TECHNOLOGY LS	TECHNOLOGY S	VOLUME
Sign Protected		X		X	X	'322					A		
Parallel In, Parallel Out Bidirectional	8	X	X	X	X	'198	•						2
		X	X	X	X	'299					•	•	
								•	▲				3
		X	X	X	X	'323					•		2
								•	▲				3
	4	X	X	X	X	'194	•				A	•	2
									▲				3
Parallel In, Parallel Out Registered Outputs	4	X	X	X	X	'671					•		
		X	X	X	X	'672					•		2
Parallel In Parallel Out	8	X		X	X	'199	•						
	5	X		X		'96	•			•	•		
	4	X		X		'95	A			•	B		2
									•				3S
		X		X		'99				•			
		X		X	X	'178	•						2
		X		X	X	'179	•						
		X		X		'195	•				A	•	2
									▲				3
		X		X		'295					B		2
		X		X		'395					A		2
									▲				3
Serial In Parallel Out	16	X		X	X	'673					•		2
	8	X				'164	•			•	•		
								▲					3
Parallel In, Serial Out	16	X		X	X	'674					•		2
	8	X		X	X	'165	•				A		
								▲					3
		X		X	X	'166	•				A		2
								▲					3
Serial In Serial Out	8	X				'91	A			•	•		2
	4	X		X		'94	•						

SHIFT REGISTERS WITH LATCHES

DESCRIPTION	NO OF BITS	OUTPUTS	TYPE	TECHNOLOGY ALS	TECHNOLOGY AS	TECHNOLOGY LS	VOLUME
Parallel In, Parallel-Out with Output Latches	4	3 State	'671			•	2
		3 State	'672			•	
Serial-In, Parallel-Out with Output Latches	16	2 State	'673			•	
	8	Buffered	'594			•	
		3 State	'595			•	
		OC	'596			•	
		OC	'599			•	
Parallel In, Serial Out, with Input Latches	8	2 State	'597			•	
		3 State	'589			•	
Parallel I/O Ports with Input Latches, Multiplexed Serial Inputs	8	3 State	'598			•	

SIGN-PROTECTED REGISTERS

DESCRIPTION	NO OF BITS	MODES S/R	MODES S/L	MODES LOAD	MODES HOLD	TYPE	TECHNOLOGY ALS	TECHNOLOGY AS	TECHNOLOGY LS	VOLUME
Sign Protected Register	8	X		X	X	'322			A	2

REGISTER FILES

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY STD TTL	TECHNOLOGY ALS	TECHNOLOGY AS	TECHNOLOGY LS	VOLUME
8 Words × 2 Bits	3-State	'172	•				
4 Words × 4 Bits	OC	'170	•			•	2
	3 State	'670				•	
Dual 16 Words × 4 Bits	3 State	'870			▲		3
	3 State	'871			▲		

OTHER REGISTERS

DESCRIPTION	TYPE	TECHNOLOGY STD TTL	TECHNOLOGY ALS	TECHNOLOGY AS	TECHNOLOGY L	TECHNOLOGY LS	TECHNOLOGY S	VOLUME
Quadruple Multiplexers with Storage	98				•			2
	298	•				•		
				•				3S
	398				•			2
	399				•			
8 Bit Universal Shift Registers	299					•	•	
			•	▲				3
Quadruple Bus Buffer Registers	125	•				A		2
Octal Storage Register	396					•		

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COUNTERS

SYNCHRONOUS COUNTERS – POSITIVE EDGE TRIGGERED

DESCRIPTION	PARALLEL LOAD	TYPE	TECHNOLOGY: STD TTL	ALS	AS	L	LS	S	VOLUME
Decade	Sync	'160	●				A		2
				B	●				CF
	Sync	162	●				A	●	2
				B	●				CF
	Sync	'560		A					3
	Sync	'668					●		2
	Sync	'690					●		
	Sync	'692					●		
Decade Up Down	Sync	'168					B	●	3S
				B	●				
	Async	190	●				●		2
				●					3
	Async	192	●			●	●		2
				●					3
	Sync	'568		A					
	Sync	696					●		2
	Sync	'698					●		
Decade Rate Multiplier, $\frac{1}{N10}$	Async Set to 9	'167	●						2
4 Bit Binary	Sync	'161	●				A		CF
				B	●				
	Sync	163	●				A	●	2
				B	●				CF
	Sync	'561		A					3
	Sync	669					●		2
	Sync	'691					●		
	Sync	'693					●		
	Sync	169					B	●	3S
				B	●				
4 Bit Binary Up Down	Async	'191	●				●		2
				●					3
	Async	193	●			●	●		2
				●					3
	Sync	569		A					
	Sync	697					●		2
	Sync	699					●		
6 Bit Binary Rate Multiplier, $\frac{1}{N2}$		97	●						2
8 Bit Up Down	Async CLR	867			●				3
	Sync CLR	869			●				

ASYNCHRONOUS COUNTERS (RIPPLE CLOCK) – NEGATIVE-EDGE TRIGGERED

DESCRIPTION	PARALLEL LOAD	TYPE	TECHNOLOGY: STD TTL	ALS	AS	L	LS	S	VOLUME
Decade	Set to 9	90	A			●	●		2
		68					●		
	Yes	176	●						
	Yes	196	●				●	●	
	Set to 9	'290	●				●		
4 Bit Binary	None	93	A			●	●		
		69					●		
	Yes	177	●						
	Yes	197	●				●	●	
	None	'293	●				●		
Divide by 12	None	'92	A				●		
Dual Decade	None	390	●				●		
	Set to 9	490	●				●		
Dual 4 Bit Binary	None	393	●				●		

8-BIT BINARY COUNTERS WITH REGISTERS

DESCRIPTION	TYPE OF OUTPUT	TYPE	TECHNOLOGY: ALS	AS	LS	VOLUME
Parallel Register	3 State	'590			●	2
Outputs	OC	591			●	
Parallel Register Inputs	2 State	592			●	
Parallel I/O	3 State	593			●	

FREQUENCY DIVIDERS, RATE MULTIPLIERS

DESCRIPTION	TYPE	TECHNOLOGY: STD TTL	ALS	AS	LS	VOLUME
50 to 1 Frequency Divider	56				●	2
60 to 1 Frequency Divider	57				●	
60 Bit Binary Rate Multiplier	97	●				
Decade Rate Multiplier	'167	●				

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DECODERS, ENCODERS, DATA SELECTORS/MULTIPLEXERS AND SHIFTERS

DATA SELECTORS/MULTIPLEXERS

DESCRIPTION	TYPE OF OUTPUT	TYPE	TECHNOLOGY						VOLUME
			STD TTL	ALS	AS	L	LS	S	
16 To 1	2 State	'150	●						2
	3 State	'250			●				3S
	3 State	'850			●				
	3 State	'851			●				
Dual 8 To 1	3 State	'351	●						2
8 To 1	2 State	'151	A				●	●	
				●	●				3S
	2 State	'152	A				●		2
			●				●	●	
	3 State	'251		●	▲				3
	3 State	'354					●		2
	2 State	'355					●		
	3 State	'356					●		
	OC	'357					●		
Dual 4 To 1	2 State	'153	●			●	●	●	3
				●	●				
	3 State	'253					●	●	2
				●	●				3
	2 State	'352					●		2
				●	●				3
	3 State	'353					●		2
				●	●				3
Octal 2 To 1 with Storage	3 State	'604					●		2
	OC	'605					●		
	3 State	'606					●		
	OC	'607					●		
Quad 2 To 1 with Storage	2 State	'98				●			2
	2 State	'298	●				●		
					●				3S
	2 State	'398					●		2
	2 State	'399					●		
Quad 2 To 1	2 State	'157	●			●	●	●	3
				●	●				
	2 State	'158					●	●	2
				●	●				3
	3 State	'257					B	●	2
				A	●				CF
	3 State	'258					B	●	2
				A	●				CF
6 to 1 Universal Multiplexer	3 State	'857		●	●				3

DECODERS/DEMULTIPLEXERS

DESCRIPTION	TYPE OF OUTPUT	TYPE	TECHNOLOGY						VOLUME
			STD TTL	ALS	AS	L	LS	S	
4 To 16	3 State	'154	●			●			2
	OC	'159	●						
4 To 10 BCD To Decimal	2 State	'42	A			●	●		
4 To 10 Excess 3 To Decimal	2 State	43	A			●			
4 To 10 Excess 3 Gray To Decimal	2 State	'44	A			●			
3 To 8 with Address Latches	2 State	'131		●	▲				3
		'137		●	▲				
							●		2
3 To 8	2 State	'138		●	▲				3
							●	●	2
	3 State	'538		▲					3
Dual 2 To 4	2 State	'139		▲	●				
							A	●	
	2 State	'155	●				A		2
	OC	'156	●				●		
Dual 1 To 4 Decoders	3 State	'539		▲					3

CODE CONVERTERS

DESCRIPTION	TYPE	TECHNOLOGY		VOLUME
		STD TTL	S	
6 Line BCD to 6 Line Binary Or 4 Line to 4 Line BCD 9's BCD 10's Converters	'184	●		2
6 Bit Binary to 6 Bit BCD Converters	'185	A		
BCD to Binary Converters	'484		A	4
Binary to BCD Converters	485		A	

PRIORITY ENCODERS/REGISTERS

DESCRIPTION	TYPE	TECHNOLOGY				VOLUME
		STD TTL	ALS	AS	LS	
Full BCD	'147	●			●	2
Cascadable Octal	'148	●			●	
Cascadable Octal with 3 State Outputs	'348				●	
4 Bit Cascadable with Registers	'278	●				

SHIFTERS

DESCRIPTION	OUTPUT	TYPE	TECHNOLOGY						VOLUME
			STD TTL	ALS	AS	L	LS	S	
4 Bit Shifter	3 State	350						●	2
Parallel 16 Bit Multi Mode Barrel Shifter	3 State	897			▲				5

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DISPLAY DECODERS/DRIVERS, MEMORY/MICROPROCESSOR CONTROLLERS, AND VOLTAGE-CONTROLLED OSCILLATORS

OPEN-COLLECTOR DISPLAY DECODERS /DRIVERS

DESCRIPTION	OFF-STATE OUTPUT VOLTAGE	TYPE	TECHNOLOGY					VOLUME
			STD TTL	ALS	AS	L	LS	
BCD To Decimal	30 V	'45	●					2
	60 V	'141	●					
	15 V	'145	●				●	
	7 V	'445					●	
BCD To Seven Segment	30 V	46	A			●		
	15 V	'47	A			●	●	
	5.5 V	'48	●				●	
	5.5 V	'49	●				●	
	30 V	'246	●					
	15 V	'247	●				●	
	7 V	'347					●	
	7 V	'447					●	
	5.5 V	'248	●				●	
	5.5 V	'249	●				●	

OPEN COLLECTOR DISPLAY DECODERS/DRIVERS WITH COUNTERS/LATCH

DESCRIPTION	TYPE	TECHNOLOGY			VOLUME
		STD TTL	ALS	AS	
BCD Counter/4 Bit Latch/BCD To Decimal Decoder/Driver	'42	●			2
BCD Counter/4 Bit Latch/BCD-To-Seven-Segment Decoder/Lad Driver	'143	●			
BCD Counter/4-Bit Latch/BCD-To-Seven-Segment Decoder/Lamp Driver	'144	●			

VOLTAGE-CONTROLLED OSCILLATORS

DESCRIPTION						TYPE	TECHNOLOGY		VOLUME
No VCOs	COMP'L Z_{OUT}	ENABLE	RANGE INPUT	R_{ext}	f_{max} MHz		LS	S	
Single	Yes	Yes	Yes	No	20	'624	●		2
Single	Yes	Yes	Yes	Yes	20	'628	●		
Dual	No	Yes	Yes	No	60	'124		●	
Dual	Yes	Yes	No	No	20	'626	●		
Dual	No	No	No	No	20	'627	●		
Dual	No	Yes	Yes	No	20	'629	●		

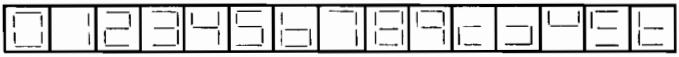
MEMORY MICROPROCESSOR CONTROLLERS

DESCRIPTION			TYPE	TECHNOLOGY				VOLUME
				ALS	AS	LS	S	
System Controllers, Universal or For 8881			890		▲			5
Memory Refresh Controllers	Transparent	4K, 16K	600			A		2
	Burst Modes	64K	'601			A		
	Cycle Steal	4K, 16K	602			A		
	Burst Modes	64K	'603			A		
Memory Cycle Controller			608			●		
Memory Mappers		3 State	612			●		
		OC	613			●		
Memory Mappers		3 State	610			●		
With Output Latches		OC	611			●		
Multi-Mode Latches (8080A Applications)			412				●	

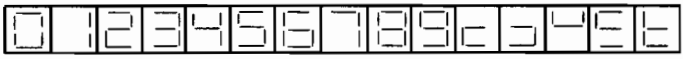
CLOCK GENERATOR CIRCUITS

DESCRIPTION	TYPE	TECHNOLOGY					VOLUME
		STD TTL	ALS	AS	LS	S	
Quadruple Complementary Output Logic Elements	'265	●					2
Dual Pulse Synchronizers Drivers	'120	●			●		
Crystal Controlled Oscillators	'320				●		
	'321				●		
Digital Phase Lock Loop	'297				●		
Programmable Frequency Dividers Digital Timers	'292				●		
	'294				●		
Triple 4 Input AND NAND Drivers	'800			▲			3
Triple 4 Input OR NOR Drivers	802			▲			
Dual VCO	'124					●	2

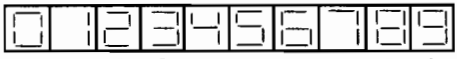
RESULTANT DISPLAYS USING '46A, '47A, '48, '49, 'L46, 'L47, 'LS47, 'LS48, 'LS49, 'LS347



RESULTANT DISPLAYS USING '246, '247, '248, '249, 'LS247, 'LS248, 'LS249, 'LS447



RESULTANT DISPLAYS USING '143, '144



● Denotes available technology.
▲ Denotes planned new products.
A Denotes "A" suffix version available in the technology indicated.

COMPARATORS AND ERROR DETECTION CIRCUITS

4-BIT COMPARATORS

DESCRIPTION					TYPE	TECHNOLOGY						VOLUME
P Q	P > Q	P < Q	OUTPUT	OUTPUT ENABLE		STD TTL	ALS	AS	L	LS	S	
Yes	Yes	No	2 State	Yes	85	●			●	●	●	2

8-BIT COMPARATORS

DESCRIPTION							TYPE	TECHNOLOGY			VOLUME
INPUTS	P Q	P Q	P > Q	P < Q	OUTPUT	OUTPUT ENABLE		ALS	AS	LS	
20 kΩ Pull Up	Yes	No	No	No	OC	Yes	518	●			3
	No	Yes	No	No	2 State	Yes	520	●			
	No	Yes	No	No	OC	Yes	522	●			
	Yes	No	Yes	No	2 State	No	682			●	2
	Yes	No	Yes	No	OC	No	683			●	
Standard	Yes	No	No	No	OC	Yes	519	●			3
	No	Yes	No	No	2 State	Yes	521	●			
	Yes	No	Yes	No	2 State	No	684			●	2
	Yes	No	Yes	No	OC	No	685			●	
	Yes	No	Yes	No	2 State	Yes	686			●	
	Yes	No	Yes	No	OC	Yes	687			●	
	No	Yes	No	Yes	2 State	Yes	688	●			3
										●	2
	No	Yes	No	No	OC	Yes	689	●			3
										●	2
Latched P	No	No	Yes	Yes	2 State	Yes	885		●		3
Latched P and Q	Yes	No	Yes	Yes	Latched	Yes	866		●		

ADDRESS COMPARATORS

DESCRIPTION	OUTPUT ENABLE	LATCHED OUTPUT	TYPE	TECHNOLOGY		VOLUME
				ALS	AS	
16-Bit to 4-Bit	Yes		'677	●		3S
		Yes	'678	●		
12-Bit to 4 Bit	Yes		679	●		
		Yes	680	●		

PARITY GENERATORS/CHECKERS, ERROR DETECTION AND CORRECTION CIRCUITS

DESCRIPTION		NO OF BITS	TYPE	TECHNOLOGY					VOLUME
				STD TTL	ALS	AS	LS	S	
Odd Even Parity Generators Checkers		8	'180	●					2
		9	280			●	●		
						▲			3
		9	'286			▲			3
Parallel Error Detection Correction Circuits	3 State	8	'636				●		2
	OC	8	'637				●		
	3 State	16	'616		▲				5
	OC	16	'617		▲				
	3 State	16	'630				●		2
	OC	16	'631				●		
	3 State	32	'632		A				CF
	OC	32	'633		▲				
	3 State	32	'634		▲				
	OC	32	'635		▲				

FUSE-PROGRAMMABLE COMPARATORS

DESCRIPTION	TYPE	TECHNOLOGY					VOLUME
		STD TTL	ALS	AS	LS	S	
16 Bit Identity Comparator	526		▲				3
12 Bit identity Comparator	528		▲				
8 Bit Identity Comparator and 4 Bit Comparator	527		▲				

CF Denotes contact factory.
● Denotes available technology.
▲ Denotes planned new products.
S Denotes supplement to data book.

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ARITHMETIC CIRCUITS AND PROCESSOR ELEMENTS

PARALLEL BINARY ADDERS

DESCRIPTION	TYPE	TECHNOLOGY						VOLUME
		STD TTL	ALS	AS	H	LS	S	
1 Bit Gated	'80	●						2
2 Bit	'82	●						
4 Bit	'83	A				A		
	'283	●				●	●	
Dual 1-Bit Carry Save	'183				●	●		

ACCUMULATORS, ARITHMETIC LOGIC UNITS, LOOK AHEAD CARRY GENERATORS

DESCRIPTION		TYPE	TECHNOLOGY					VOLUME
			STD TTL	ALS	AS	LS	S	
4 Bit parallel Binary Accumulators		281					●	2
		681				●		
4 Bit Arithmetic Logic Units Function Generators		181	●			●	●	3
					A			
		381				A		2
							●	
		881			A			3
4 Bit Arithmetic Logic Unit with Ripple Carry		382				●		2
Look Ahead Carry Generators	16 Bit	182	●				●	2
					▲			3
		282			▲			
	32 Bit	'882			●			3
Quad Serial Adder Subtractor		385				●		2
8 Bit Slice Elements		'888			▲			5

MULTIPLIERS

DESCRIPTION	TYPE	TECHNOLOGY					VOLUME
		STD TTL	ALS	AS	LS	S	
2 Bit by 4 Bit Parallel Binary Multipliers	261				●		2
4 Bit by 4 Bit Parallel Binary Multipliers	284	●					
	285	●					
25 MHz 6 Bit Binary Rate Multipliers	'97	●					
25 MHz Decade Rate Multipliers	167	●					
8 Bit × 1 Bit 2's Complement Multipliers	384				●		
16 Bit Parallel Multiplier	1616		▲				5

OTHER ARITHMETIC OPERATORS

DESCRIPTION	TYPE	TECHNOLOGY							VOLUME
		STD TTL	ALS	AS	H	L	LS	S	
Quad 2 Input Exclusive OR Gates with Totem Pole Outputs	'86	●				●	A	●	2
			●						3S
Quad 2 Input Exclusive OR Gates with Open Collector Outputs	'386						A		2
	'136	●						●	
			●						3S
Quad 2 Input Exclusive NOR Gates	'266						●		2
	'810		●	▲					3S
Quad 2 Input Exclusive NOR Gates with Open Collector Outputs	'811		●	▲					3S
Quad Exclusive OR NOR Gates	135							●	2
4 Bit True Complement Element	87				●				

BIPOLAR BIT SLICE PROCESSOR ELEMENTS

DESCRIPTION	CASCADABLE TO N-BITS	TYPE	TECHNOLOGY				VOLUME
			ALS	AS	LS	S	
8 Bit Slice	Yes	'888		▲			5

● Denotes available technology.
▲ Denotes planned new products.
A Denotes "A" suffix version available in the technology indicated.
S Denotes supplement to data book.

MEMORIES

USER PROGRAMMABLE READ-ONLY MEMORIES (PROM's)
STANDARD PROM's

DESCRIPTION	TYPE	ORGANIZATION	TYPE OUTPUT	S	VOLUME
16K Bit Arrays	TBP28S166	2048W × 8B	3 State	●	4
	TBP38S165	2048W × 8B	3 State	▲	
	TBP38S166	2048W × 8B	3 State	▲	
	TBP38SA165	2048W × 8B	OC	▲	
	TBP38SA166	2048W × 8B	OC	▲	
	TBP34S162	4096W × 4B	3 State	▲	
	TBP34SA162	4096W × 4B	OC	▲	
8K Bit Arrays	TBP24S81	2048W × 4B	3 State	●	
	TBP24SA81	2048W × 4B	OC	●	
	TBP28S85A	1024W × 8B	3 State	▲	
	TBP28S86A	1024W × 8B	3 State	●	
	TBP28SA86A	1024W × 8B	OC	●	
	TBP38S85	1024W × 8B	3 State	▲	
	TBP38S86	1024W × 8B	3 State	▲	
	TBP38SA85	1024W × 8B	OC	▲	
	TBP38SA86	1024W × 8B	OC	▲	
4K Bit Arrays	TBP24S41	1024W × 4B	3 State	●	
	TBP24SA41	1024W × 4B	OC	●	
	TBP28S42	512W × 8B	3 State	●	
	TBP28SA42	512W × 8B	OC	●	
	TBP28S46	512W × 8B	3 State	●	
	TBP28SA46	512W × 8B	OC	●	
2K Bit Arrays	TBP38S22	256W × 8B	3 State	▲	
	TBP38SA22	256W × 8B	OC	▲	
1K Bit Arrays	TBP24S10	256W × 4B	3 State	●	
	TBP24SA10	256W × 4B	OC	●	
	TBP34S10	256W × 4B	3 State	▲	
	TBP34SA10	256W × 4B	OC	▲	
256 Bit Arrays	TBP18S030	32W × 8B	3 State	●	
	TBP18SA030	32W × 8B	OC	●	
	TBP38S030	32W × 8B	3 State	●	
	TBP38SA030	32W × 8B	OC	●	

LOW-POWER PROM's

DESCRIPTION	TYPE	ORGANIZATION	TYPE OUTPUT	S	VOLUME
16K Bit Arrays	TBP28L166	2048W × 8B	3 State	●	4
	TBP38L165	2048W × 8B	3 State	●	
	TBP38L166	2048W × 8B	3 State	●	
	TBP34L162	4096W × 4B	3 State	▲	
8K Bit Arrays	TBP28L85A	1024W × 8B	3 State	▲	
	TBP28L86A	1024W × 8B	3 State	●	
	TBP38L85	1024W × 8B	3 State	▲	
	TBP38L86	1024W × 8B	3 State	▲	
4K Bit Arrays	TBP28L42	512W × 8B	3 State	●	
	TBP28L46	512W × 8B	3 State	●	
2K Bit Arrays	TBP28L22	256W × 8B	3 State	●	
	TBP28LA22	256W × 8B	OC	●	
	TBP38L22	256W × 8B	3 State	▲	
1K Bit Arrays	TBP34L10	256W × 4B	3 State	▲	
256 Bit Arrays	TBP38L030	32W × 8B	3 State	▲	

REGISTERED PROM's

DESCRIPTION	TYPE	ORGANIZATION	TYPE OUTPUT	S	VOLUME
16K Bit Arrays	TBP34R162	4096W × 4B	3 State	▲	4
	TBP34SR165	4096W × 4B	3 State	▲	

RANDOM-ACCESS READ-WRITE MEMORIES (RAM's)

DESCRIPTION	ORGANIZATION	TYPE OF OUTPUT	TYPE	TECHNOLOGY					VOLUME
				STD TTL	ALS	AS	LS	S	
256 Bit Arrays	256 × 1	3 State	'201					●	4
		OC	'301					●	
64 Bit Arrays	16 × 4	OC	'89	●					
		3 State	'189				A	B	
		3 State	'219				A		
		OC	'289				A	B	
		OC	'319				A		
16 Bit Multiple Port Register File	8 × 2	3 State	'172	●					2
16 Bit Register File	4 × 4	OC	'170	●			●		
		3 State	'670				●		
Dual 64 Bit Register Files	16 × 4	3 State	'870			●			3
			'871			●			

FIRST-IN FIRST-OUT MEMORIES (FIFO'S)

DESCRIPTION	TYPE OF OUTPUT	TYPE	TECHNOLOGY				VOLUME
			ALS	AS	LS	LS	
16 Words × 5 Bits	3 State	225				●	5
64 Words × 5 Bits	3 State	233	▲				
64 Words × 4 Bits	3 State	232	▲				

● Denotes available technology.
▲ Denotes planned new products.
A Denotes "A" suffix version available in the technology indicated.
B Denotes "B" suffix version available in the technology indicated.

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PROGRAMMABLE LOGIC ARRAYS

PROGRAMMABLE LOGIC ARRAYS

DESCRIPTION	INPUTS	OUTPUTS NO	OUTPUTS TYPE	TYPE NO	ALS	NO OF PINS	VOLUME
Standard High Speed PAL Circuits	16	8	Active Low	PAL16L8A	●	20	
		4	Registered	PAL16R4A	●		
		6		PAL16R6A	●		
		8		PAL16R8A	●		
Standard High Speed Half Power PAL Circuits	16	8	Active Low	PAL16L8A-2	●	20	
		4	Registered	PAL16R4A-2	●		
		6		PAL16R6A-2	●		
		8		PAL16R8A-2	●		
Standard High Speed PAL Circuits	20	8	Active Low	PAL20L8A	▲	24	
		4	Registered	PAL20R4A	▲		
		6		PAL20R6A	▲		
		8		PAL20R8A	▲		
Standard High Speed Half Power PAL Circuits	20	8	Active Low	PAL20L8A-2	▲	24	
		4	Registered	PAL20R4A-2	▲		
		6		PAL20R6A-2	▲		
		8		PAL20R8A-2	▲		
High Performance FIXED OR Impact PAL Circuits	12	10	Active High	TIBPAL*2H10	▲	24	
			Active Low	TIBPAL12L10	▲		
			Programmable	*TIBPAL12P10	▲		
	14	8	Active High	TIBPAL*4H8	▲	24	
			Active Low	*TIBPAL14L8	▲		
			Programmable	TIBPAL*4P8	▲		
	16	6	Active High	*TIBPAL16H6	▲	24	
			Active Low	TIBPAL16L6	▲		
			Programmable	TIBPAL16P6	▲		
	18	4	Active High	TIBPAL18H4	▲	24	
			Active Low	TIBPAL18L4	▲		
			Programmable	TIBPAL18P4	▲		
	20	2	Active High	TIBPAL20H2	▲	24	
			Active Low	TIBPAL20L2	▲		
			Programmable	TIBPAL20P2	▲		
High Performance Impact PAL Circuits	16	8	Active Low	TIBPAL16L8-15	●	20	
		4	Registered	TIBPAL16R4-15	●		
		6		TIBPAL16R6-15	●		
		8		TIBPAL16R8-15	●		
High Performance Half Power Impact PAL Circuits	16	8	Active Low	TIBPAL16L8-25	●	20	
		4	Registered	TIBPAL16R4-25	●		
		6		TIBPAL16R6-25	●		
		8		TIBPAL16R8-25	●		
High Performance EXCLUSIVE OR Impact PAL Circuits	20	10	Active Low	TIBPAL20L10-XX	▲	24	
		4	Registered	TIBPAL20X4-XX	▲		
		8		TIBPAL20X8-XX	▲		
		10		TIBPAL20X10-XX	▲		
High Performance Half Power EXCLUSIVE OR Impact PAL Circuits	20	10	Active Low	TIBPAL20L10-XX	▲	24	
		4	Registered	*TIBPAL20X4-XX	▲		
		8		TIBPAL20X8-XX	▲		
		10		TIBPAL20X10-XX	▲		
High Performance Registered Input PAL Circuits	19	8	Active Low	TIBPALR19L8-XX	▲	24	
		4	Registered	TIBPALR19R4-XX	▲		
		6		TIBPALR19R6-XX	▲		
		8		TIBPALR19R8-XX	▲		
High Performance Half Power Registered Input PAL Circuits	19	8	Active Low	TIBPALR19L8-XX	▲	24	
		4	Registered	TIBPALR19R4-XX	▲		
		6		TIBPALR19R6-XX	▲		
		8		TIBPALR19R8-XX	▲		
High Performance Latched Input PAL Circuits	19	8	Active Low	TIBPALT19L8-XX	▲	24	
		4	Registered	TIBPALT19R4-XX	▲		
		6		*TIBPALT19R6-XX	▲		
		8		*TIBPALT19R8-XX	▲		
High Performance Half Power Latched Input PAL Circuits	19	8	Active Low	*TIBPALT19L8-XX	▲	24	
		4	Registered	*TIBPALT19R4-XX	▲		
		6		TIBPALT19R6-XX	▲		
		8		TIBPALT19R8-XX	▲		
Field Programmable 14 × 32 × 8 Logic Arrays	14	8	3 State	TIFPLA839	●	24	
			OC	TIFPLA840	●		
Field Programmable 14 × 48 × 8 Logic Sequencer	14	8	3 State	*82S167	▲	24	
				82S167A	▲		
Field Programmable 16 × 48 × 8 Logic Sequencer	16	8	OC	*TMS*16	▲	28	
			3 State	*TPL510	▲		
			OC	82S105A	▲		
			3 State	82S106A	▲		

*PAL is a registered trademark of Monolithic Memories Incorporated

● Denotes available technology.

▲Denotes planned new products.

General Information 1

Functional Index 2

Field-Programmable Logic 3

PROMs 4

RAMs and Memory-Based Code Converters 5

Designing with Texas Instruments Field-Programmable Logic 6

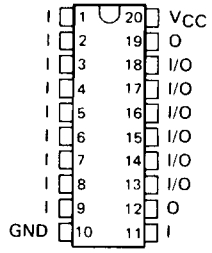
Mechanical Data 7

FEBRUARY 1984—REVISED JANUARY 1985

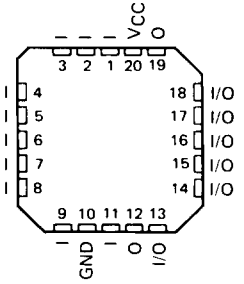
- **Standard High-Speed (25 ns) PAL Family**
- **Choice of Operating Speeds**
  HIGH SPEED, A Devices . . . 35 MHz
  HALF POWER, A-2 Devices . . . 18 MHz
- **Choice of Input/Output Configuration**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**

DEVICE	INPUTS	3-STATE O OUTPUTS	REGISTERED Q OUTPUTS	I/O PORTS
PAL16L8	10	2	0	6
PAL16R4	8	0	4 (3-state)	4
PAL16R6	8	0	6 (3-state)	2
PAL16R8	8	0	8 (3-state)	0

PAL16L8'
M SUFFIX . . . J PACKAGE
C SUFFIX . . . J OR N PACKAGE
(TOP VIEW)



PAL16L8'
M SUFFIX . . . FH OR FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



Pin assignments in operating mode (pins 1 and 11 less positive than V_{IHH})

description

These programmable array logic devices feature high speed and a choice of either standard or half-power devices. They combine Advanced Low-Power Schottky† technology with proven titanium-tungsten fuses. These devices will provide reliable, high-performance substitutes for conventional TTL logic. Their easy programmability allows for quick design of "custom" functions and typically result in a more compact circuit board. In addition, chip carriers are available for further reduction in board space.

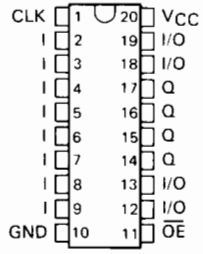
The Half-Power versions offer a choice of operating frequency, switching speeds, and power dissipation. In many cases, these Half-Power devices can result in significant power reduction from an overall system level.

The PAL16' M series is characterized for operation over the full military temperature range of −55°C to 125°C. The PAL16' C series is characterized for operation from 0°C to 70°C.

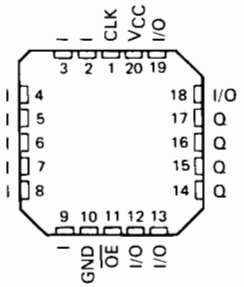
†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments, U.S. Patent Number 3,463,975.

PAL is a registered trademark of Monolithic Memories Inc.

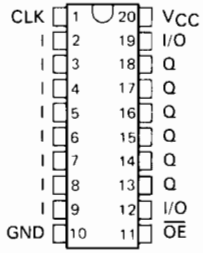
PAL16R4'
M SUFFIX . . . J PACKAGE
C SUFFIX . . . J OR N PACKAGE
(TOP VIEW)



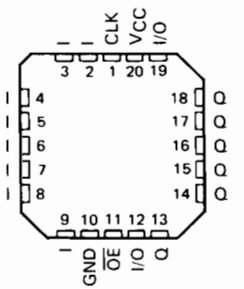
PAL16R4'
M SUFFIX . . . FH OR FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



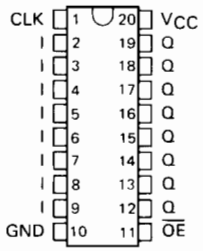
PAL16R6'
M SUFFIX . . . J PACKAGE
C SUFFIX . . . J OR N PACKAGE
(TOP VIEW)



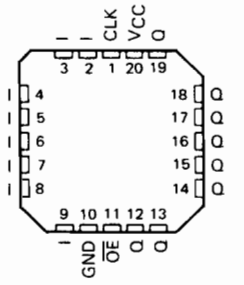
PAL16R6'
M SUFFIX . . . FH OR FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



PAL16R8'
M SUFFIX . . . J PACKAGE
C SUFFIX . . . J OR N PACKAGE
(TOP VIEW)



PAL16R8'
M SUFFIX . . . FH OR FK PACKAGE
C SUFFIX FN PACKAGE
(TOP VIEW)

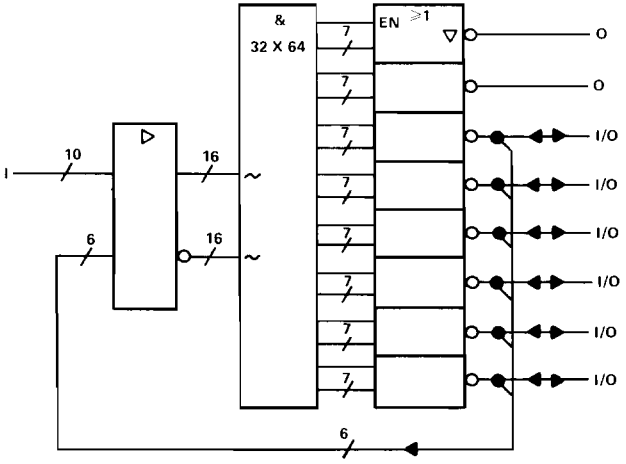


Pin assignments in operating mode (pins 1 and 11 less positive than V_{IHH})

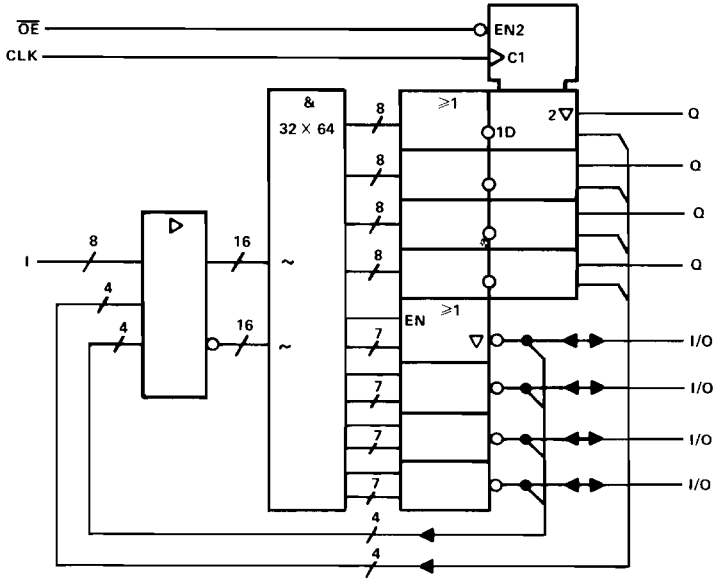
TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

functional block diagrams (positive logic)

'PAL16L8A
'PAL16L8A-2



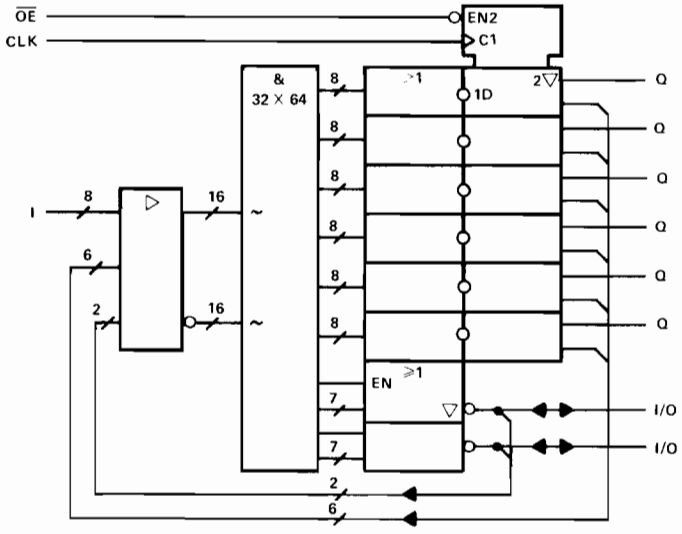
'PAL16R4A
'PAL16R4A-2



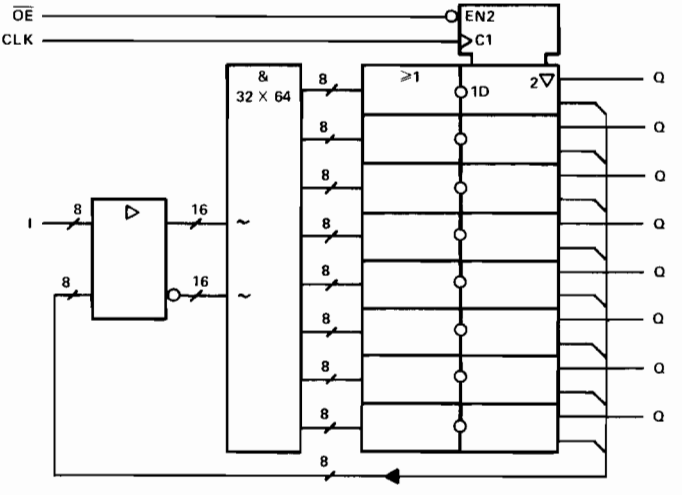
~ denotes fused inputs

functional block diagrams (positive logic)

'PAL16R6A
'PAL16R6A-2



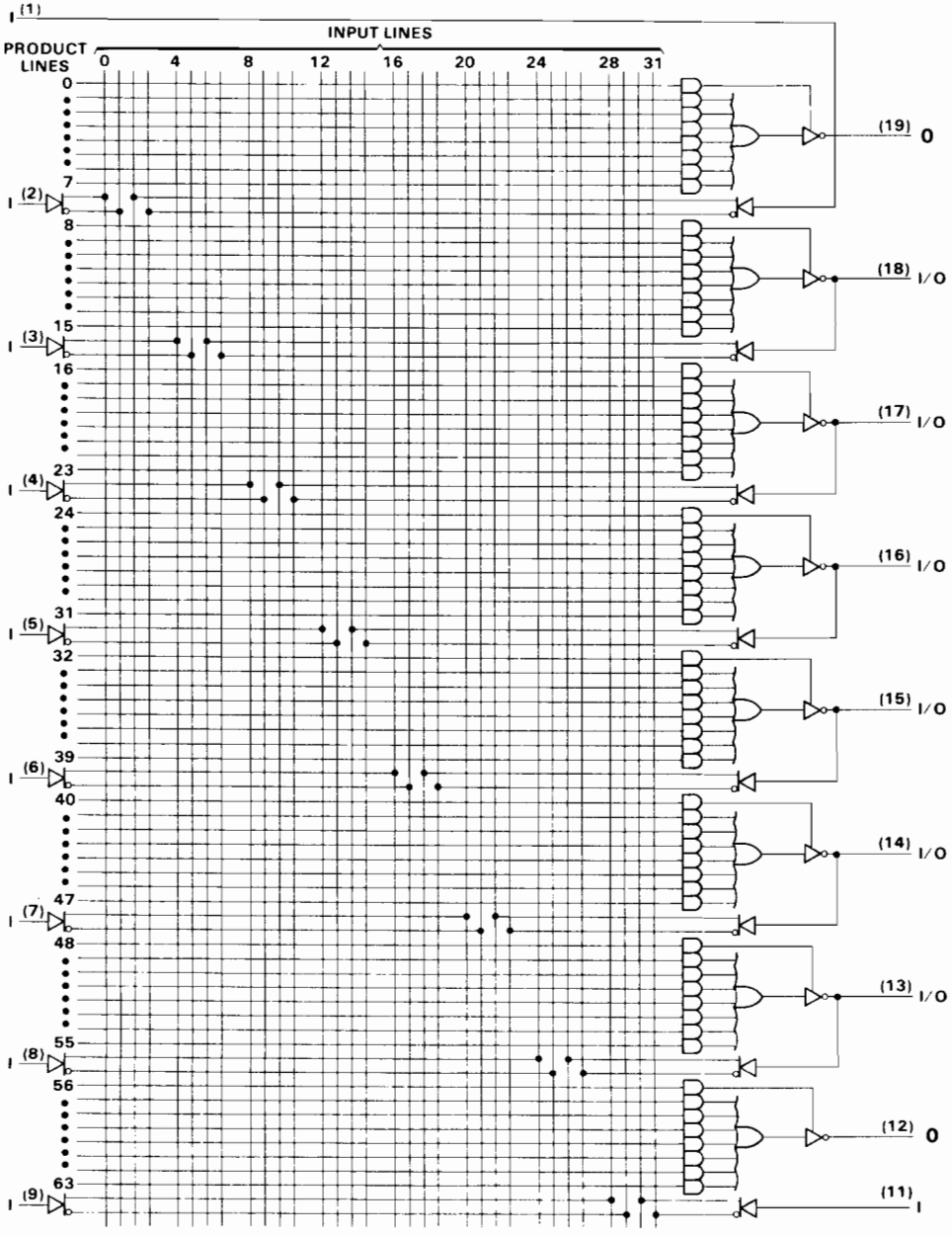
'PAL16R8A
'PAL16R8A-2



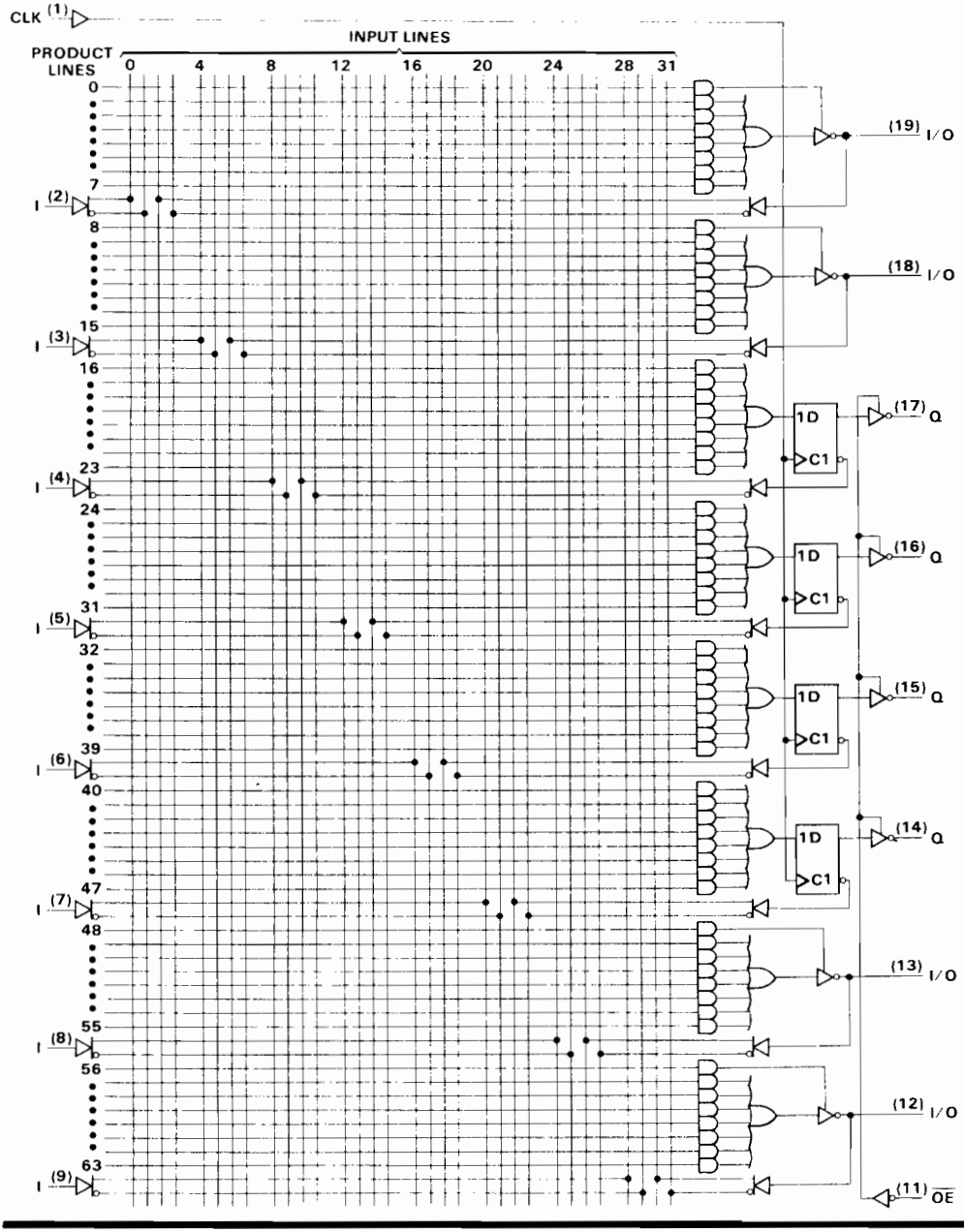
~ denotes fused inputs

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

logic diagram

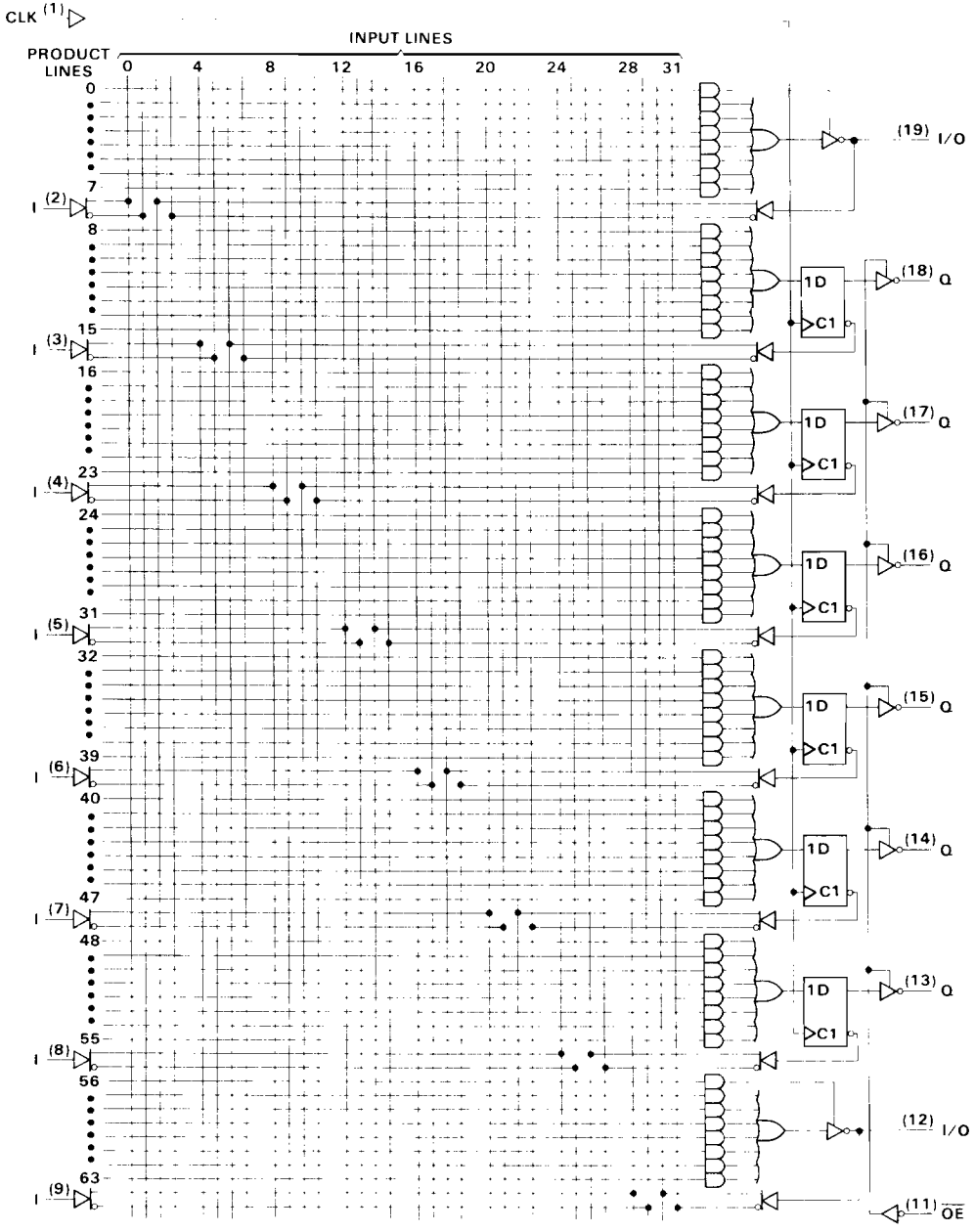


logic diagram

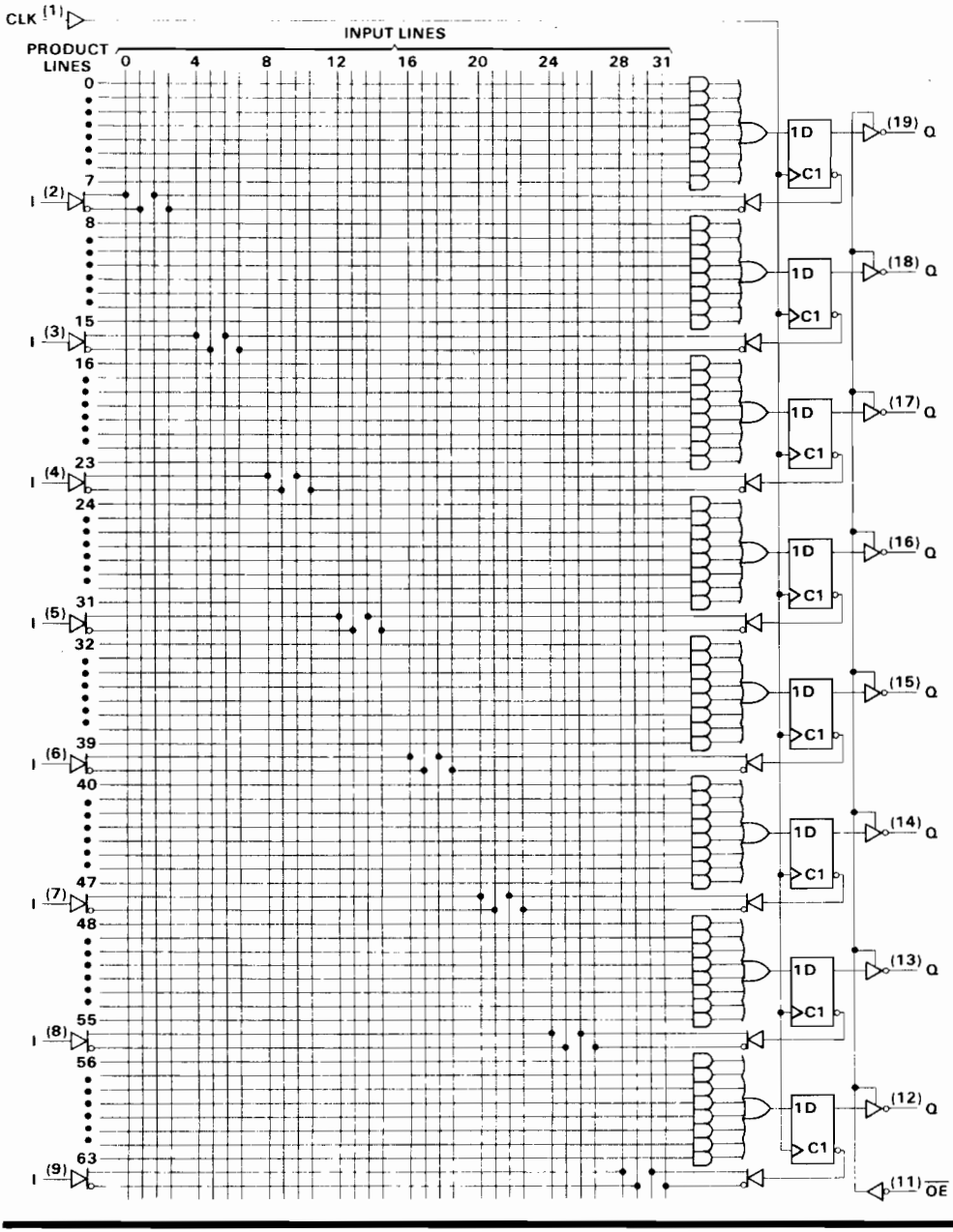


TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

logic diagram



logic diagram



TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Voltage applied to a disabled output (see Note 1) . . . . . 5.5 V
Operating free-air temperature range: M suffix . . . . . −55°C to 125°C
C suffix . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle.

recommended operating conditions

PARAMETER			M SUFFIX			C SUFFIX			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	$\overline{OE}$ input	2.4		5.5	2		5.5	V
		All others	2		5.5	2		5.5	
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−2			−3.2	mA
I_{OL}	Low-level output current				12			24	mA
T_A	Operating free-air temperature		−55		125	0		70	°C

programming parameters, T_A = 25°C

			MIN	NOM	MAX	UNIT
V_{CC}	Verify-level supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2		5.5	V
V_{IL}	Low-level input voltage				0.8	V
V_{IHH}	Program-pulse input voltage		10.25	10.5	10.75	V
I_{IHH}	Program-pulse input current	PO		20	50	mA
		PGM ENABLE, L/R		10	25	
		PI, PA		1.5	5	
		V_{CC}		250	400	
t_{w1}	Program-pulse duration at PO pins		10		50	μs
t_{w2}	Pulse duration at PGM VERIFY		100			ns
	Program-pulse duty cycle at PO pins				25	%
t_{su}	Setup time		100			ns
t_h	Hold time		100			ns
t_{d1}	Delay time from V_{CC} to 5 V to PGM VERIFY↑		100			μs
t_{d2}	Delay time from PGM VERIFY ↑ to valid output		200			ns
	Input voltage at pins 1 and 11 to open verify-protect (security) fuse		20	21	22	V
	Input current to open verify-protect (security) fuse				400	mA
t_{w3}	Pulse duration to open verify-protect (security) fuse		20		50	μs
	V_{CC} value during security fuse programming			0	0.4	V

3

Field-Programmable Logic

recommended operating conditions

			M SUFFIX			C SUFFIX			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
f_{clock}	Clock frequency		0		25	0		35	MHz
t_w	Pulse duration, see Note 2	Clock high	15			12			ns
		Clock low	20			16			
t_{su}	Setup time, input or feedback before CLK↑		25			20			ns
t_h	Hold time, input or feedback after CLK↑		0			0			ns

NOTE 2: The total clock period of clock high and clock low must not exceed clock frequency, f_{clock}. The minimum pulse durations specified are only for clock high or clock low, but not for both simultaneously.

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS†		M SUFFIX			C SUFFIX			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}		V_{CC} = MIN, I_{OH} = MAX		2.4	3.2		2.4	3.3		V
V_{OL}		V_{CC} = MIN, I_{OL} = MAX			0.25	0.4		0.35	0.5	V
I_{OZH}	Outputs	V_{CC} = MAX, V_O = 2.7 V				20			20	μA
	I/O ports					100			100	
I_{OZL}	Outputs	V_{CC} = MAX, V_O = 0.4 V				−20			−20	μA
	I/O ports					−250			−250	
I_I		V_{CC} = MAX, V_I = 5.5 V				0.2			0.1	mA
I_{IH}		V_{CC} = MAX, V_I = 2.7 V				25			20	μA
I_{IL}		V_{CC} = MAX, V_I = 0.4 V	$\overline{OE}$ INPUT			−0.25			−0.4	mA
			All others			−0.2			−0.2	
I_O§		V_{CC} = MAX, V_O = 2.25 V		−30		−125	−30		−125	mA
I_{CC}		V_{CC} = MAX, V_I = 0 V, Outputs Open			140	185		140	180	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely aproximates one half of the true short-circuit output current, I_{OS}.

switching characteristics over recommended supply voltage and operating free-air temperature ranges (unless otherwise noted)

PARAMETER	FROM	TO	TEST CONDITIONS	M SUFFIX			C SUFFIX			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
f_{max}				25	45		35	45		MHz
t_{pd}	I, I/O,	O, I/O			15	30		15	25	ns
t_{pd}	CLK↑	Q	R_L = 500 Ω,		10	20		10	15	ns
t_{en}	$\overline{OE}$↓	Q	C_L = 50 pF,		15	25		15	22	ns
t_{dis}	$\overline{OE}$↑	Q	See Note 3		10	25		10	15	ns
t_{en}	I, I/O	O, I/O			14	30		14	25	ns
t_{dis}	I, I/O	O, I/O			13	30		13	25	ns

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

recommended operating conditions

			M SUFFIX			C SUFFIX			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
f_{clock}	Clock frequency		0		16	0		18	MHz
t_w	Pulse duration, see Note 2	Clock high	28			25			ns
		Clock low	28			25			
t_{su}	Setup time, input or feedback before CLK↑		35			28			ns
t_h	Hold time, input or feedback after CLK↑		0			0			ns

NOTE 2: The total clock period of clock high and clock low must not exceed clock frequency, f_{clock}. The minimum pulse durations specified are only for clock high or clock low, but not for both simultaneously.

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS†			M SUFFIX			C SUFFIX			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = MIN,	I_I = −18 mA				−1.5			−1.5	V
V_{OH}		V_{CC} = MIN,	I_{OH} = MAX		2.4	3.2		2.4	3.3		V
V_{OL}		V_{CC} = MIN,	I_{OL} = MAX			0.25	0.4		0.35	0.5	V
I_{OZH}	Outputs	V_{CC} = MAX,	V_O = 2.7 V				20			20	μA
	I/O ports						100			100	
I_{OZL}	Outputs	V_{CC} = MAX,	V_O = 0.4 V				−20			−20	μA
	I/O ports						−250			−250	
I_I		V_{CC} = MAX,	V_I = 5.5 V				0.2			0.1	mA
I_{IH}		V_{CC} = MAX,	V_I = 2.7 V				25			20	μA
I_{IL}		V_{CC} = MAX,	V_I = 0.4 V	$\overline{OE}$ INPUT			−0.2			−0.2	mA
				All others			−0.1			−0.1	
I_O§		V_{CC} = MAX,	V_O = 2.25 V		−30		−125	−30		−125	mA
I_{CC}		V_{CC} = MAX, V_I = 0 V	Outputs Open			75	95		70	90	mA

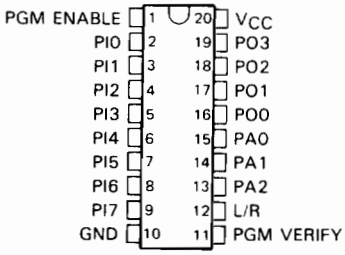
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely aproximates one half of the true short-circuit output current, I_{OS}.

switching characteristics over recommended supply voltage and operating free-air temperature ranges (unless otherwise noted)

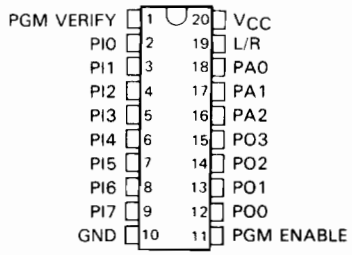
PARAMETER	FROM	TO	TEST CONDITIONS	M SUFFIX			C SUFFIX			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
f_{max}				16	25		18	25		MHz
t_{pd}	I, I/O,	O, I/O			25	40		25	35	ns
t_{pd}	CLK↑	Q	R_L = 500 Ω,		11	35		11	25	ns
t_{en}	$\overline{OE}$↓	Q	C_L = 50 pF,		20	35		20	25	ns
t_{dis}	$\overline{OE}$↑	Q	See Note 3		11	30		11	20	ns
t_{en}	I, I/O	O, I/O			25	40		25	35	ns
t_{dis}	I, I/O	O, I/O			25	35		25	30	ns

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

PRODUCT TERMS 0 THRU 31
(TOP VIEW)



PRODUCT TERMS 32 THRU 63
(TOP VIEW)



Pin assignments in programming mode (PGM ENABLE, pin 1 or 11, at V_{IHH})

TABLE 1 — INPUT LINE SELECT

INPUT LINE NUMBER	PIN NAME								
	PI7	PI6	PI5	PI4	PI3	PI2	PI1	PI0	L/R
0	HH	HH	HH	HH	HH	HH	HH	L	Z
1	HH	HH	HH	HH	HH	HH	HH	H	Z
2	HH	HH	HH	HH	HH	HH	HH	L	HH
3	HH	HH	HH	HH	HH	HH	HH	H	HH
4	HH	HH	HH	HH	HH	HH	L	HH	Z
5	HH	HH	HH	HH	HH	HH	H	HH	Z
6	HH	HH	HH	HH	HH	HH	L	HH	HH
7	HH	HH	HH	HH	HH	HH	H	HH	HH
8	HH	HH	HH	HH	HH	L	HH	HH	Z
9	HH	HH	HH	HH	HH	H	HH	HH	Z
10	HH	HH	HH	HH	HH	L	HH	HH	HH
11	HH	HH	HH	HH	HH	H	HH	HH	HH
12	HH	HH	HH	HH	L	HH	HH	HH	Z
13	HH	HH	HH	HH	H	HH	HH	HH	Z
14	HH	HH	HH	HH	L	HH	HH	HH	HH
15	HH	HH	HH	HH	H	HH	HH	HH	HH
16	HH	HH	HH	L	HH	HH	HH	HH	Z
17	HH	HH	HH	H	HH	HH	HH	HH	Z
18	HH	HH	HH	L	HH	HH	HH	HH	HH
19	HH	HH	HH	H	HH	HH	HH	HH	HH
20	HH	HH	L	HH	HH	HH	HH	HH	Z
21	HH	HH	H	HH	HH	HH	HH	HH	Z
22	HH	HH	L	HH	HH	HH	HH	HH	HH
23	HH	HH	H	HH	HH	HH	HH	HH	HH
24	HH	L	HH	HH	HH	HH	HH	HH	Z
25	HH	H	HH	HH	HH	HH	HH	HH	Z
26	HH	L	HH	HH	HH	HH	HH	HH	HH
27	HH	H	HH	HH	HH	HH	HH	HH	HH
28	L	HH	HH	HH	HH	HH	HH	HH	Z
29	H	HH	HH	HH	HH	HH	HH	HH	Z
30	L	HH	HH	HH	HH	HH	HH	HH	HH
31	H	HH	HH	HH	HH	HH	HH	HH	HH

TABLE 2 — PRODUCT LINE SELECT

PRODUCT LINE NUMBER	PIN NAME						
	PO0	PO1	PO2	PO3	PA2	PA1	PA0
0, 32	Z	Z	Z	HH	Z	Z	Z
1, 33	Z	Z	Z	HH	Z	Z	HH
2, 34	Z	Z	Z	HH	Z	HH	Z
3, 35	Z	Z	Z	HH	Z	HH	HH
4, 36	Z	Z	Z	HH	HH	Z	Z
5, 37	Z	Z	Z	HH	HH	Z	HH
6, 38	Z	Z	Z	HH	HH	HH	Z
7, 39	Z	Z	Z	HH	HH	HH	HH
8, 40	Z	Z	HH	Z	Z	Z	Z
9, 41	Z	Z	HH	Z	Z	Z	HH
10, 42	Z	Z	HH	Z	Z	HH	Z
11, 43	Z	Z	HH	Z	Z	HH	HH
12, 44	Z	Z	HH	Z	HH	Z	Z
13, 45	Z	Z	HH	Z	HH	Z	HH
14, 46	Z	Z	HH	Z	HH	HH	Z
15, 47	Z	Z	HH	Z	HH	HH	HH
16, 48	Z	HH	Z	Z	Z	Z	Z
17, 49	Z	HH	Z	Z	Z	Z	HH
18, 50	Z	HH	Z	Z	Z	HH	Z
19, 51	Z	HH	Z	Z	Z	HH	HH
20, 52	Z	HH	Z	Z	HH	Z	Z
21, 53	Z	HH	Z	Z	HH	Z	HH
22, 54	Z	HH	Z	Z	HH	HH	Z
23, 55	Z	HH	Z	Z	HH	HH	HH
24, 56	HH	Z	Z	Z	Z	Z	Z
25, 57	HH	Z	Z	Z	Z	Z	HH
26, 58	HH	Z	Z	Z	Z	HH	Z
27, 59	HH	Z	Z	Z	Z	HH	HH
28, 60	HH	Z	Z	Z	HH	Z	Z
29, 61	HH	Z	Z	Z	HH	Z	HH
30, 62	HH	Z	Z	Z	HH	HH	Z
31, 63	HH	Z	Z	Z	HH	HH	HH

L = V_{IL}, H = V_{IH}, HH = V_{IHH}, Z = high impedance (e.g. 10 kΩ to 5 V)

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

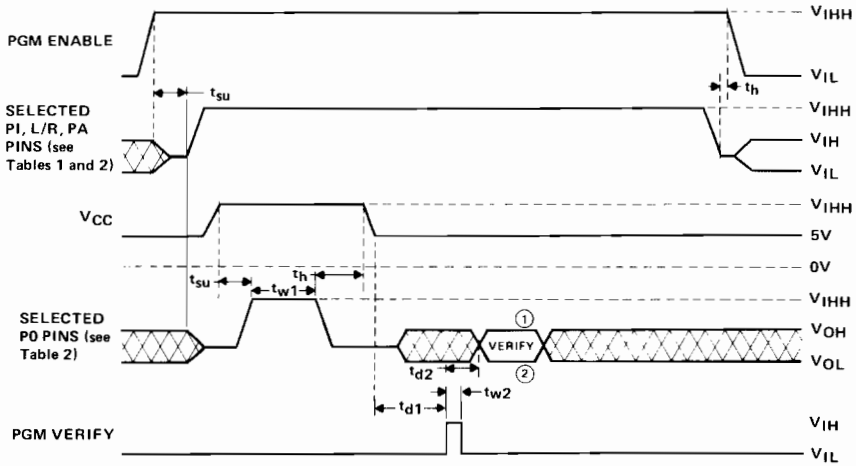
programming procedure for array fuses

Array fuses are programmed using a linear select method. Each fuse can be opened by selecting the appropriate (one of 32) input line and then pulsing the correct (one of 64) product line. The levels for selecting input lines and product lines are shown in Tables 1 and 2.

Step 1 Raise PGM ENABLE to V_{IHH}.
Step 2 Select an input line by applying appropriate levels to L/R and PI pins.
Step 3 Begin selection of the output line with appropriate conditions on PA pins.
Step 4 Raise V_{CC} to V_{IHH}.
Step 5 Blow the fuse by pulsing the appropriate PO pin to V_{IHH} as shown in Table 2 for the product line.
Step 6 Return V_{CC} to 5 volts and pulse PGM Verify. The PO pin selected in Step 5 will be less than V_{OL} if the fuse is open.

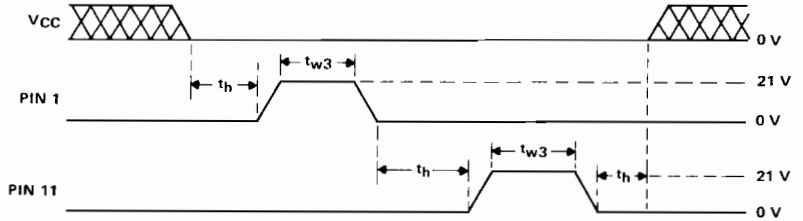
Steps 1 through 6 may be repeated if the verification does not indicate that the fuse was successfully programmed (blown), but no more than four times. Verification is possible only with the verify-protect fuse intact.

programming waveforms



(1) A high level during the verify interval indicates that programming has not been successful.
(2) A low level during the verify interval indicates that programming has been successful.

security fuse programming

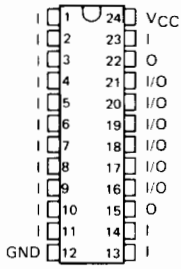


D2706, DECEMBER 1982 REVISED JANUARY 1985

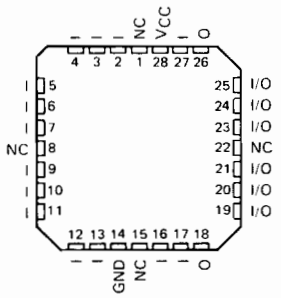
- Standard High Speed (25 ns) PAL Family
- Choice of Operating Speeds
  HIGH SPEED, A devices . . . 30 MHz
  HALF POWER, A-2 devices . . . 18 MHz
- Choice of Input/Output Configuration
- Preload Capability on Output Registers
- DIP Options Include Both 300-mil Plastic and 600-mil Ceramic

DEVICE	I INPUTS	3-STATE O OUTPUTS	REGISTERED Q OUTPUTS	I/O PORTS
'PAL20L8A	14	2	0	6
'PAL20R4A	12	0	4 (3-state buffers)	4
'PAL20R6A	12	0	6 (3-state buffers)	2
'PAL20R8A	12	0	8 (3-state buffers)	0

PAL20L8'
M SUFFIX . . . JW PACKAGE
C SUFFIX . . . JW OR NT PACKAGE
(TOP VIEW)



PAL20L8'
M SUFFIX . . . FH OR FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



DIP pin assignments in operating mode (voltages at pins 1 and 13 less then V_{IHH}). PLCC pin assignments in operating mode (voltages at pins 2 and 16 less then V_{IHH}).

description

These programmable array logic devices feature high speed and a choice of either standard or half-power speeds. They combine Advanced Low-Power Schottky† technology with proven titanium-tungsten fuses. These devices will provide reliable, high performance substitutes over conventional TTL logic. Their easy programmability allows for quick design of "custom" functions and typically result in a more compact circuit board. In addition, chip carriers are also available for further reduction in board space.

The Half-Power versions offer a choice of operating frequency, switching speeds, and power dissipation. In many cases, these Half-Power devices can result in significant power reduction from an overall system level.

In addition, extra circuitry has been provided to allow loading of each register asynchronously to either a high or low state. This feature simplifies testing because the registers can be set to an initial state prior to executing the test sequence.

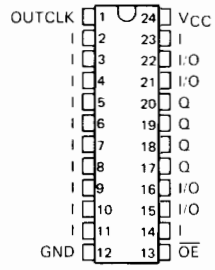
The PAL20' series is characterized for operation over the full military temperature range of −55°C to 125°C. The commercial range is characterized from 0°C to 70°C.

PAL is a registered trademark of Monolithic Memories Inc.
†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments, U.S. Patent Number 3,463,975.

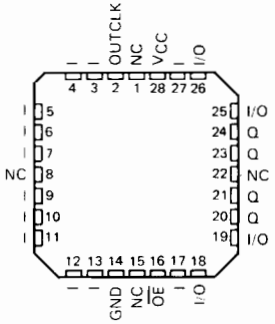
PRODUCT PREVIEW
This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

PAL20R4'
M SUFFIX . . . JW PACKAGE
C SUFFIX . . . JW OR NT PACKAGE
(TOP VIEW)



PAL20R4'
M SUFFIX . . . FH OR FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



PAL20R6'
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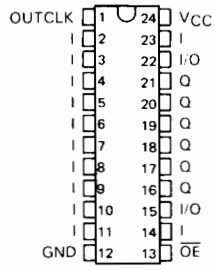
C SUFFIX . . . JW OR NT PACKAGE
(TOP VIEW)



PAL20R6'
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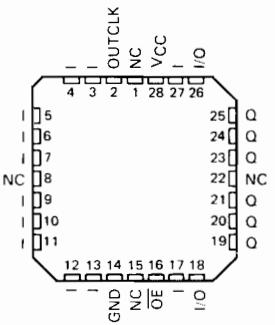
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



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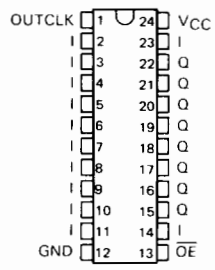
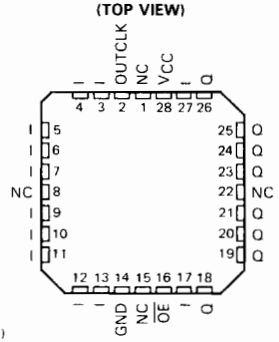
C SUFFIX . . . JW OR NT PACKAGE
(TOP VIEW)



PAL20R8'
M SUFFIX . . . FH OR FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



DIP pin assignments in operating mode (voltages at pins 1 and 13 less than V_{IHH})
PLCC pin assignments in operating mode (voltages at pins 2 and 16 less than V_{IHH})

TEXAS INSTRUMENTS
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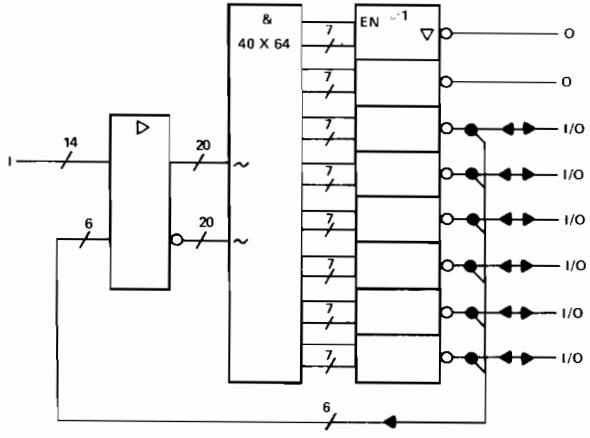
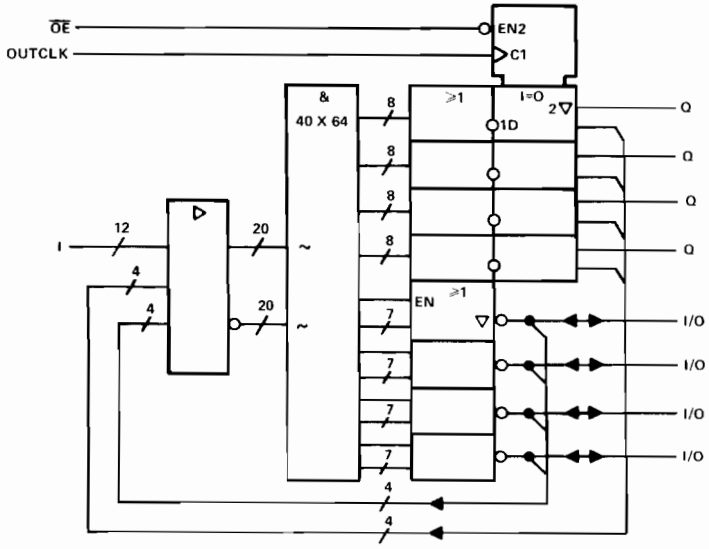
functional block diagrams (positive logic)

PAL20L8A
PAL20L8A-2

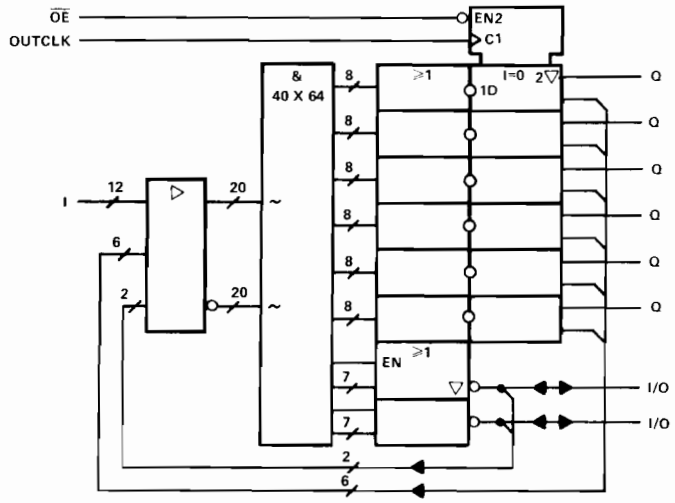


PAL20R4A
PAL20R4A-2

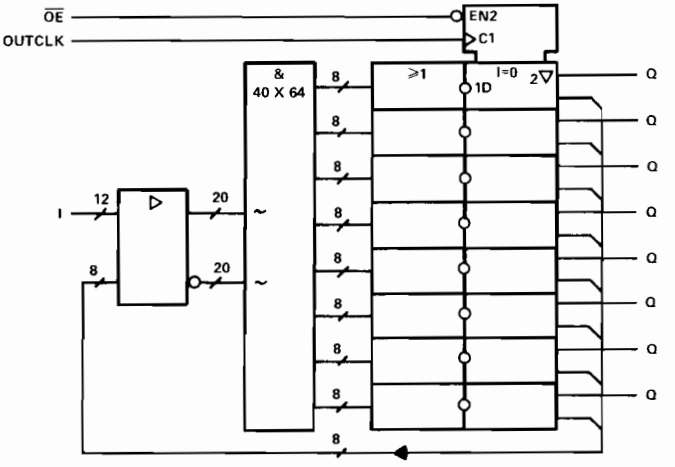


functional block diagrams (positive logic)

PAL20R6A
PAL20R6A-2



PAL20R8A
PAL20R8A-2



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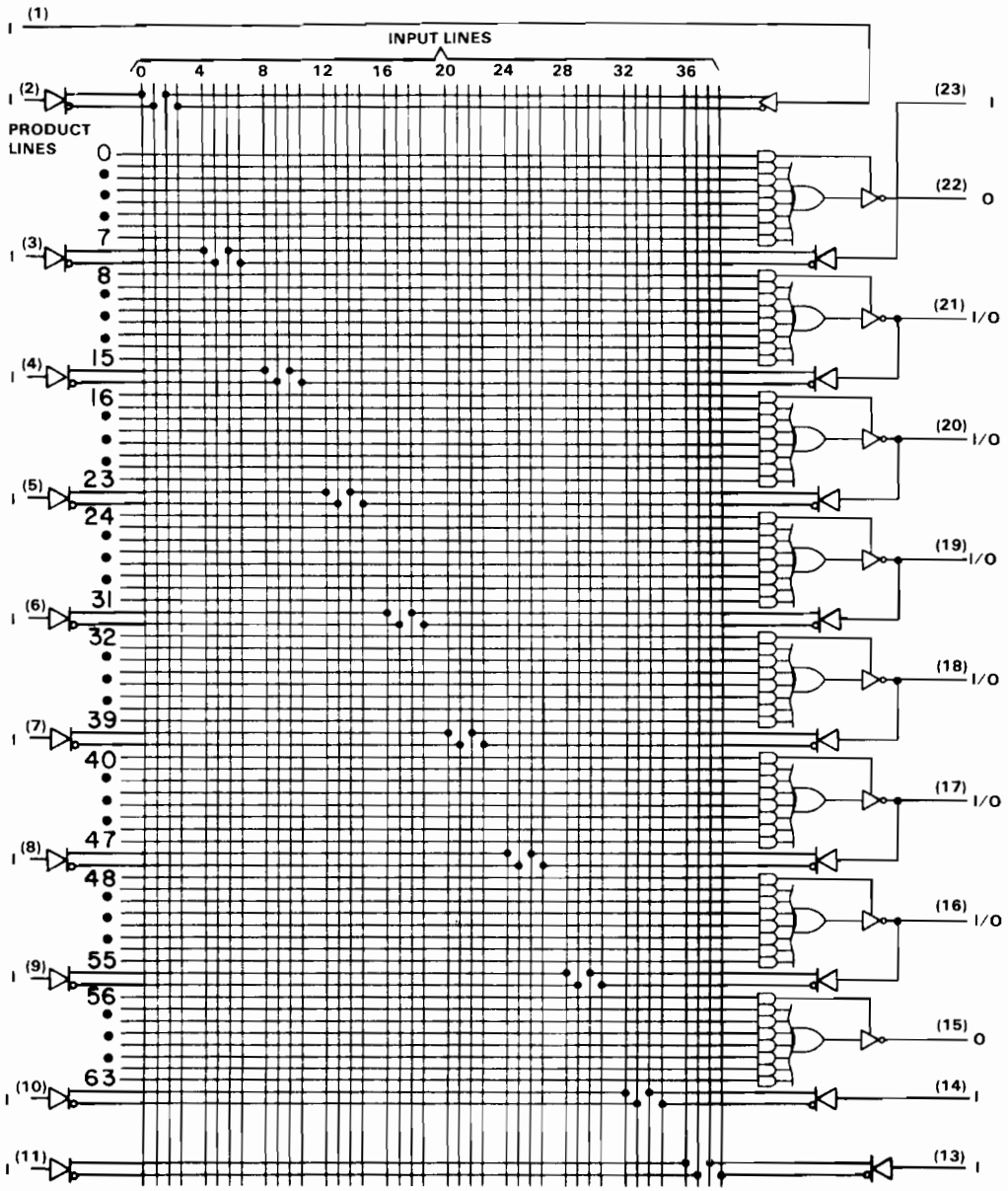
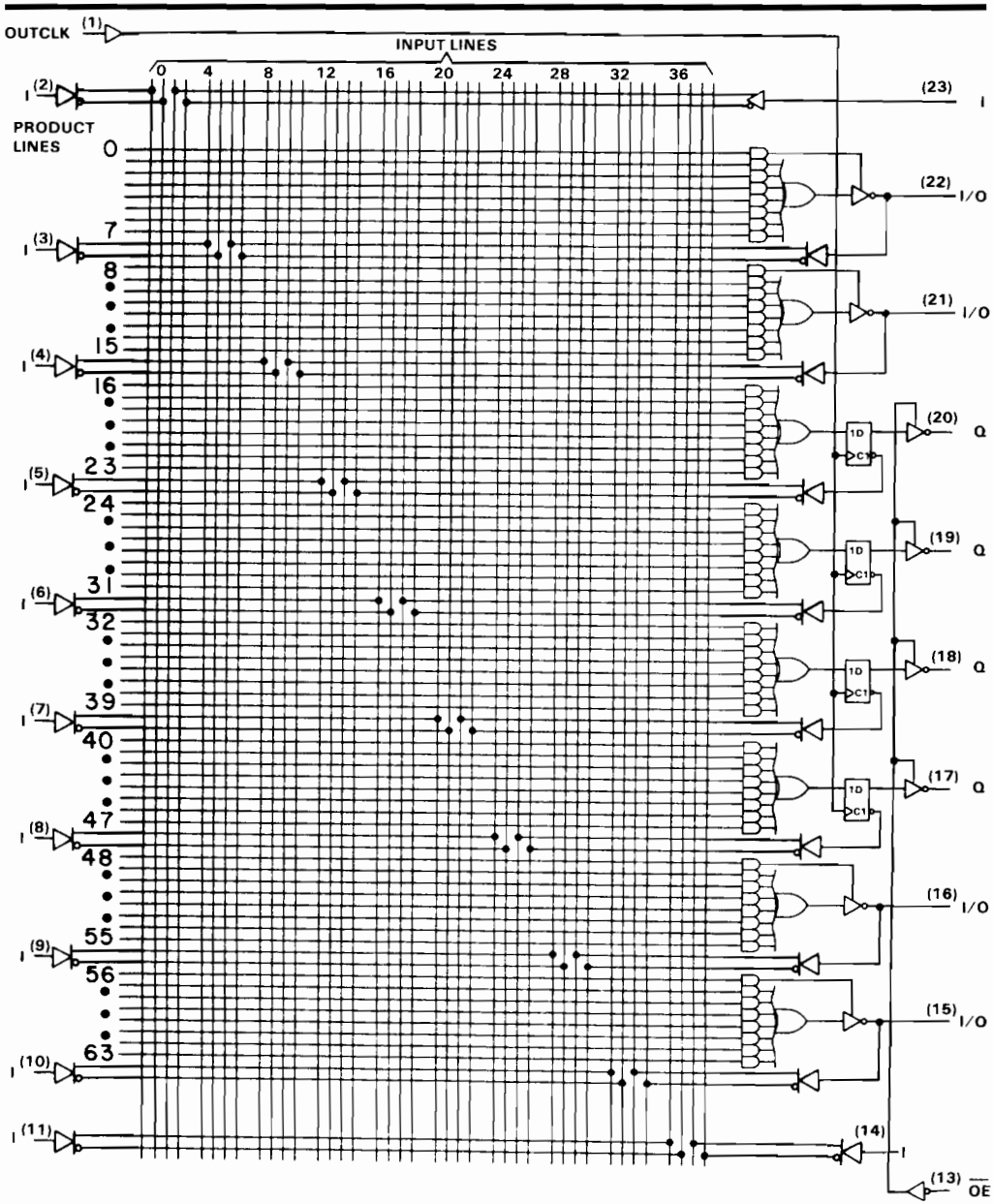

(1)
INPUT LINES
0 4 8 12 16 20 24 28 32 36
(2)
PRODUCT LINES
0
7
(3)
8
15
(4)
16
23
(5)
24
31
(6)
32
39
(7)
40
47
(8)
48
55
(9)
56
63
(10)
(11)
(23) I
(22) O
(21) I/O
(20) I/O
(19) I/O
(18) I/O
(17) I/O
(16) I/O
(15) O
(14) I
(13) I



TEXAS INSTRUMENTS
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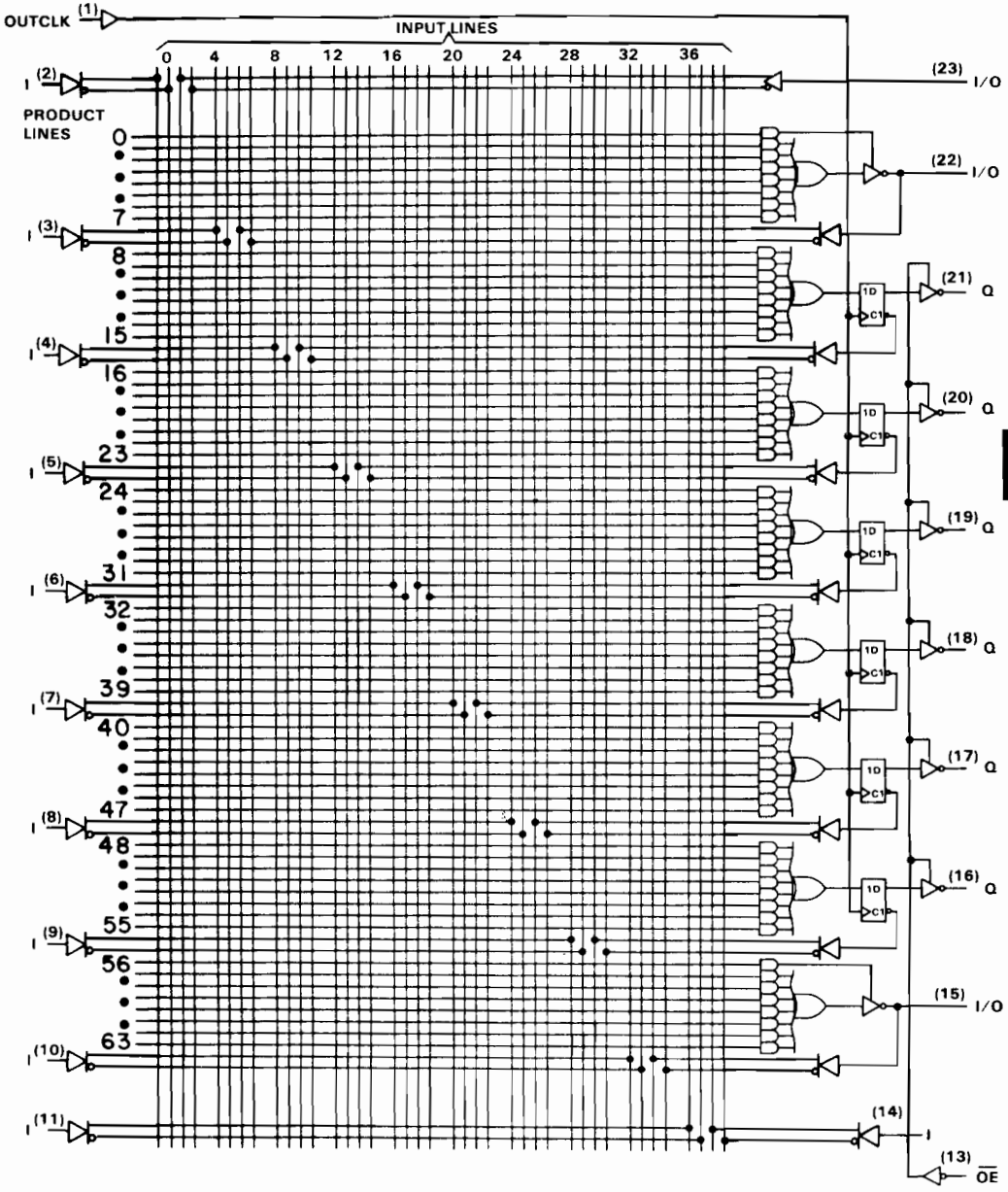
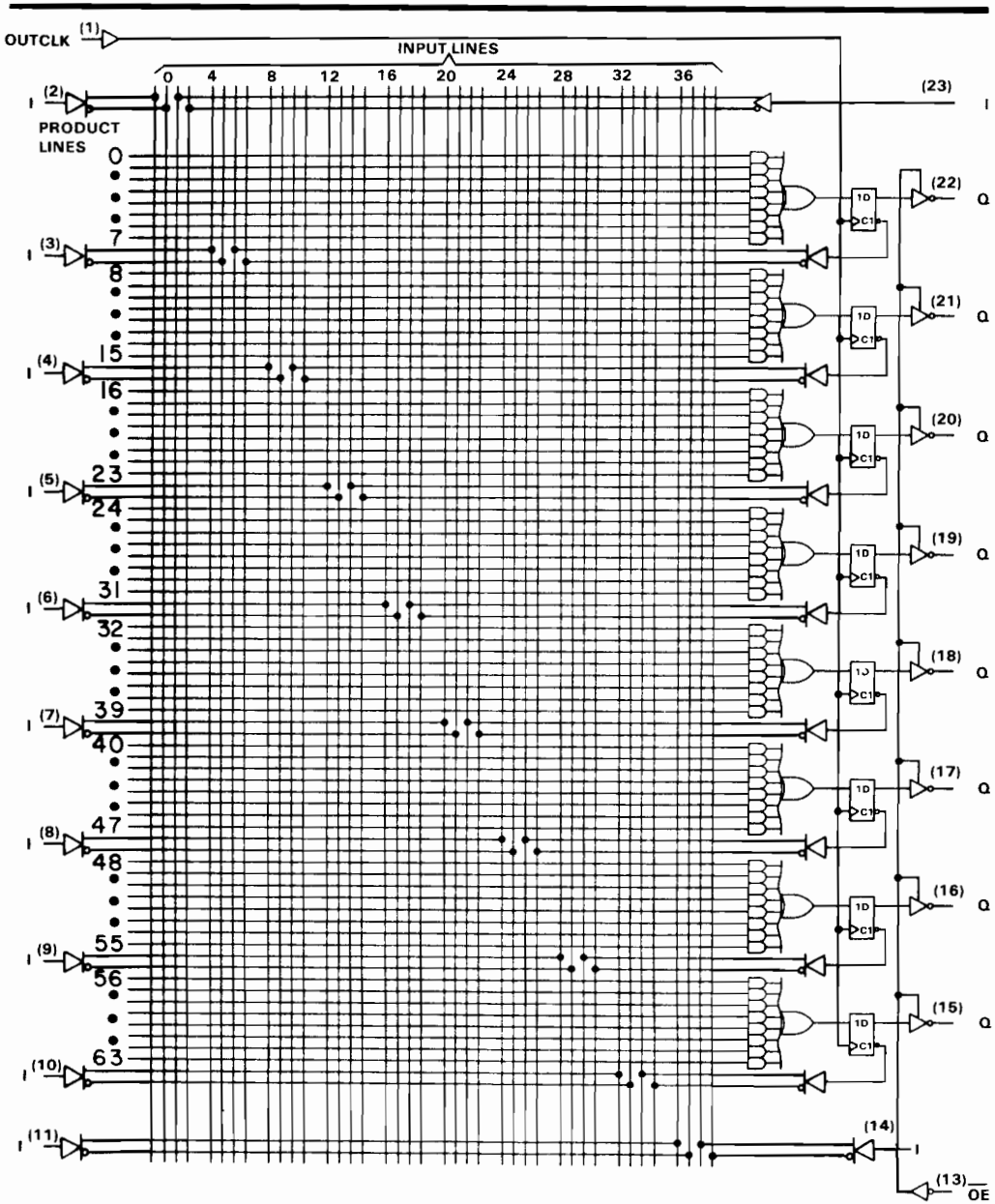

OUTCLK (1)
INPUT LINES
0 4 8 12 16 20 24 28 32 36
I (2)
PRODUCT LINES
0
7
I (3)
8
15
I (4)
16
23
I (5)
24
31
I (6)
32
39
I (7)
40
47
I (8)
48
55
I (9)
56
63
I (10)
I (11)
(23) I/O
(22) I/O
(21) Q
(20) Q
(19) Q
(18) Q
(17) Q
(16) Q
(15) I/O
(14) I
(13) OE
1D
C1



TEXAS INSTRUMENTS
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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Voltage applied to a disabled output (see Note 1) . . . . . 5.5 V
Operating free-air temperature range: M suffix . . . . . −55°C to 125°C
C suffix . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle.

recommended operating conditions

PARAMETER		M SUFFIX			C SUFFIX			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2		5.5	2		5.5	V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−2			−3.2	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

programming parameters, T_A = 25°C

			MIN	NOM	MAX	UNIT
V_{CC}	Verify-level supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2		5.5	V
V_{IL}	Low-level input voltage				0.8	V
V_{IHH}	Program-pulse input voltage		10.25	10.5	10.75	V
I_{IHH}	Program-pulse input current	PO		20	50	mA
		PGM ENABLE, L/R		10	25	
		PI, PA		1.5	5	
		V_{CC}		250	400	
t_{w1}	Program-pulse duration at PO pins		10		50	μs
t_{w2}	Pulse duration at PGM VERIFY		100			ns
	Program-pulse duty cycle at PO pins				25	%
t_{su}	Setup time		100			ns
t_h	Hold time		100			ns
t_{d1}	Delay time from V_{CC} to 5 V to PGM VERIFY†		100			μs
t_{d2}	Delay time from PGM VERIFY† to valid output		200			ns
	Input voltage at pins 1 and 11 to open verify-protect (security) fuse		20	21	22	V
	Input current to open verify-protect (security) fuse				400	mA
t_{w3}	Pulse duration to open verify-protect (security) fuse		20		50	μs
	V_{CC} value during security fuse programming			0	0.4	V

3 Field-Programmable Logic

recommended operating conditions

			M SUFFIX			C SUFFIX			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
f_{clock}	Clock frequency		0		20	0		30	MHz
t_w	Pulse duration, clock	High	20			15			ns
		Low	20			15			ns
t_{su}	Setup time, input or feedback before OUTCLK↑		30			25			ns
t_h	Hold time, input or feedback after OUTCLK↑		0			0			ns

electrical characteristics over recommended free-air operating temperature range

PARAMETER		TEST CONDITIONS†	M SUFFIX			C SUFFIX			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = MIN, I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = MIN, I_{OH} = MAX	2.4	3.2		2.4	3.3		V
V_{OL}		V_{CC} = MIN, I_{OL} = MAX		0.25	0.4		0.35	0.5	V
I_{OZH}	O, Q outputs	V_{CC} = MAX, V_{IH} = 2.7 V			20			20	μA
	I/O ports				100			100	
I_{OZL}	O, Q outputs	V_{CC} = MAX, V_{IH} = 0.4 V			−20			−20	μA
	I/O ports				−250			−250	
I_I	$\overline{OE}$ input	V_{CC} = MAX, V_I = 5.5 V			0.2			0.2	mA
	All others				0.1			0.1	
I_{IH}	$\overline{OE}$ input	V_{CC} = MAX, V_I = 2.7 V			40			40	μA
	All others				20			20	
I_{IL}	$\overline{OE}$ input	V_{CC} = MAX, V_I = 0.4 V			−0.4			−0.4	mA
	All others				−0.2			−0.2	
I_O§		V_{CC} = MAX, V_O = 2.25 V	−30		−125	−30		−125	mA
I_{CC}		V_{CC} = MAX, V_I = 0 V, Outputs open, $\overline{OE}$ at V_{IH}		150	210		150	210	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half the true short-circuit current, I_{OS}.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	TEST CONDITIONS	M SUFFIX			C SUFFIX			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
f_{max}				20			30			MHz
t_{pd}	I, I/O	O, I/O			15	30		15	25	ns
t_{pd}	OUTCLK↑	Q	R_L = 500 Ω,		10	20		10	15	ns
t_{en}	$\overline{OE}$	Q	C_L = 50 pF		10	25		10	20	ns
t_{dis}	$\overline{OE}$↑	Q	See Note 2		11	25		11	20	ns
t_{en}	I, I/O	O, I/O			14	30		14	25	ns
t_{dis}	I, I/O	O, I/O			12	30		12	25	ns

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

recommended operating conditions

			M SUFFIX			C SUFFIX			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
f_{clock}	Clock frequency		0		18	0		18	MHz
t_w	Pulse duration, clock	High							ns
		Low							ns
t_{su}	Setup time, input or feedback before OUTCLK↑								ns
t_h	Hold time, input or feedback after OUTCLK↑								ns

electrical characteristics over recommended free-air operating temperature range

PARAMETER		TEST CONDITIONS†	M SUFFIX			C SUFFIX			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = MIN, I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = MIN, I_{OH} = MAX	2.4	3.2		2.4	3.3		V
V_{OL}		V_{CC} = MIN, I_{OL} = MAX		0.25	0.4		0.35	0.5	V
I_{OZH}	O, Q outputs	V_{CC} = MAX, V_{IH} = 2.7 V			20			20	μA
	I/O ports				100			100	
I_{OZL}	O, Q outputs	V_{CC} = MAX, V_{IH} = 0.4 V			−20			−20	μA
	I/O ports				−250			−250	
I_I	$\overline{OE}$ input	V_{CC} = MAX, V_I = 5.5 V			0.2			0.2	mA
	All others				0.1			0.1	
I_{IH}	$\overline{OE}$ input	V_{CC} = MAX, V_I = 2.7 V			40			40	μA
	All others				20			20	
I_{IL}	$\overline{OE}$ input	V_{CC} = MAX, V_I = 0.4 V			−0.4			−0.4	mA
	All others				−0.2			−0.2	
I_O§		V_{CC} = MAX, V_O = 2.25 V	−30		−125	−30		−125	mA
I_{CC}		V_{CC} = MAX, V_I = 0 V, Outputs open, $\overline{OE}$ at V_{IH}		75	100		75	100	mA

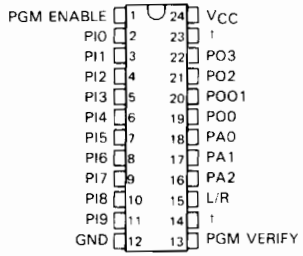
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half the true short-circuit current, I_{OS}.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

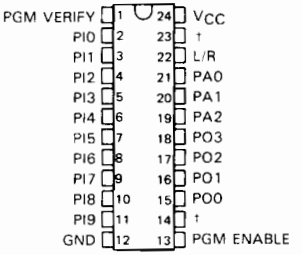
PARAMETER	FROM	TO	TEST CONDITIONS	M SUFFIX			C SUFFIX			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
f_{max}			R_L = 500 Ω, C_L = 50 pF, See Note 2	18			18			MHz
t_{pd}	I, I/O	O, I/O			25			25		ns
t_{pd}	OUTCLK↑	Q			20			20		ns
t_{en}	$\overline{OE}$	Q			15			15		ns
t_{dis}	$\overline{OE}$↑	Q			12			12		ns
t_{en}	I, I/O	O, I/O			25			25		ns
t_{dis}	I, I/O	O, I/O			20			20		ns

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

PRODUCT TERMS 0 THRU 31
(TOP VIEW)



PRODUCT TERMS 32 THRU 63
(TOP VIEW)



†Pins 14 and 23 have no programming function. Make no connection.
Pin assignments in programming mode (PGM ENABLE at V_{IHH})

TABLE 1. INPUT LINE SELECT

INPUT LINE NUMBER	PIN NAME										
	PI9	PI8	PI7	PI6	PI5	PI4	PI3	PI2	PI1	PI0	L/R
0	HH	HH	HH	HH	HH	HH	HH	HH	HH	L	Z
1	HH	HH	HH	HH	HH	HH	HH	HH	HH	H	Z
2	HH	HH	HH	HH	HH	HH	HH	HH	HH	L	HH
3	HH	HH	HH	HH	HH	HH	HH	HH	HH	H	HH
4	HH	HH	HH	HH	HH	HH	HH	HH	L	HH	Z
5	HH	HH	HH	HH	HH	HH	HH	HH	H	HH	Z
6	HH	HH	HH	HH	HH	HH	HH	HH	L	HH	HH
7	HH	HH	HH	HH	HH	HH	HH	HH	H	HH	HH
8	HH	HH	HH	HH	HH	HH	HH	L	HH	HH	Z
9	HH	HH	HH	HH	HH	HH	HH	H	HH	HH	Z
10	HH	HH	HH	HH	HH	HH	HH	L	HH	HH	HH
11	HH	HH	HH	HH	HH	HH	HH	H	HH	HH	HH
12	HH	HH	HH	HH	HH	HH	L	HH	HH	HH	Z
13	HH	HH	HH	HH	HH	HH	H	HH	HH	HH	Z
14	HH	HH	HH	HH	HH	HH	L	HH	HH	HH	HH
15	HH	HH	HH	HH	HH	HH	H	HH	HH	HH	HH
16	HH	HH	HH	HH	HH	L	HH	HH	HH	HH	Z
17	HH	HH	HH	HH	HH	H	HH	HH	HH	HH	Z
18	HH	HH	HH	HH	HH	L	HH	HH	HH	HH	HH
19	HH	HH	HH	HH	HH	H	HH	HH	HH	HH	HH
20	HH	HH	HH	HH	L	HH	HH	HH	HH	HH	Z
21	HH	HH	HH	HH	H	HH	HH	HH	HH	HH	Z
22	HH	HH	HH	HH	L	HH	HH	HH	HH	HH	HH
23	HH	HH	HH	HH	H	HH	HH	HH	HH	HH	HH
24	HH	HH	HH	L	HH	HH	HH	HH	HH	HH	Z
25	HH	HH	HH	H	HH	HH	HH	HH	HH	HH	Z
26	HH	HH	HH	L	HH	HH	HH	HH	HH	HH	HH
27	HH	HH	HH	H	HH	HH	HH	HH	HH	HH	HH
28	HH	HH	L	HH	HH	HH	HH	HH	HH	HH	Z
29	HH	HH	H	HH	HH	HH	HH	HH	HH	HH	Z
30	HH	HH	L	HH	HH	HH	HH	HH	HH	HH	HH
31	HH	HH	H	HH	HH	HH	HH	HH	HH	HH	HH
32	HH	L	HH	HH	HH	HH	HH	HH	HH	HH	Z
33	HH	H	HH	HH	HH	HH	HH	HH	HH	HH	Z
34	HH	L	HH	HH	HH	HH	HH	HH	HH	HH	HH
35	HH	H	HH	HH	HH	HH	HH	HH	HH	HH	HH
36	L	HH	HH	HH	HH	HH	HH	HH	HH	HH	Z
37	H	HH	HH	HH	HH	HH	HH	HH	HH	HH	Z
38	L	HH	HH	HH	HH	HH	HH	HH	HH	HH	HH
39	H	HH	HH	HH	HH	HH	HH	HH	HH	HH	HH

L = V_{IL}, H = V_{IH}, HH = V_{IHH}, Z = high impedance (e.g., 10 kΩ to 5 V)

TABLE 2. PRODUCT LINE SELECT

PRODUCT LINE NUMBER	PIN NAME						
	PO0	PO1	PO2	PO3	PA2	PA1	PA0
0, 32	Z	Z	Z	HH	Z	Z	Z
1, 33	Z	Z	Z	HH	Z	Z	HH
2, 34	Z	Z	Z	HH	Z	HH	Z
3, 35	Z	Z	Z	HH	Z	HH	HH
4, 36	Z	Z	Z	HH	HH	Z	Z
5, 37	Z	Z	Z	HH	HH	Z	HH
6, 38	Z	Z	Z	HH	HH	HH	Z
7, 39	Z	Z	Z	HH	HH	HH	HH
8, 40	Z	Z	HH	Z	Z	Z	Z
9, 41	Z	Z	HH	Z	Z	Z	HH
10, 42	Z	Z	HH	Z	Z	HH	Z
11, 43	Z	Z	HH	Z	Z	HH	HH
12, 44	Z	Z	HH	Z	HH	Z	Z
13, 45	Z	Z	HH	Z	HH	Z	HH
14, 46	Z	Z	HH	Z	HH	HH	Z
15, 47	Z	Z	HH	Z	HH	HH	HH
16, 48	Z	HH	Z	Z	Z	Z	Z
17, 49	Z	HH	Z	Z	Z	Z	HH
18, 50	Z	HH	Z	Z	Z	HH	Z
19, 51	Z	HH	Z	Z	Z	HH	HH
20, 52	Z	HH	Z	Z	HH	Z	Z
21, 53	Z	HH	Z	Z	HH	Z	HH
22, 54	Z	HH	Z	Z	HH	HH	Z
23, 55	Z	HH	Z	Z	HH	HH	HH
24, 56	HH	Z	Z	Z	Z	Z	Z
25, 57	HH	Z	Z	Z	Z	Z	HH
26, 58	HH	Z	Z	Z	Z	HH	Z
27, 59	HH	Z	Z	Z	Z	HH	HH
28, 60	HH	Z	Z	Z	HH	Z	Z
29, 61	HH	Z	Z	Z	HH	Z	HH
30, 62	HH	Z	Z	Z	HH	HH	Z
31, 63	HH	Z	Z	Z	HH	HH	HH

3 Field-Programmable Logic

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

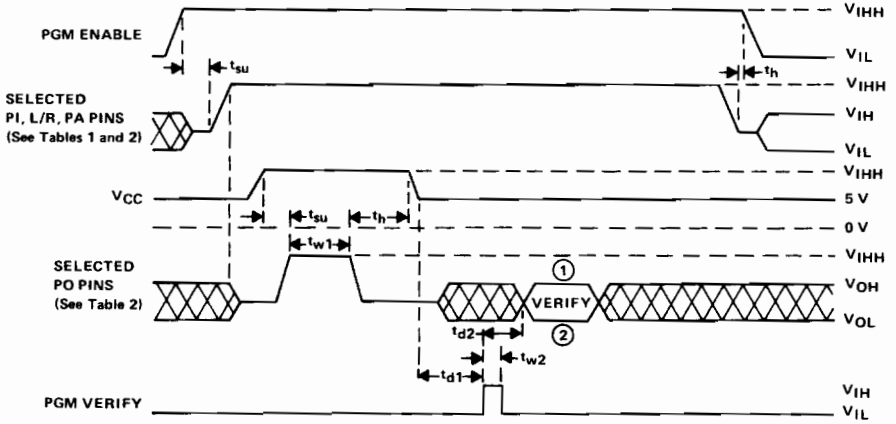
programming procedure for array fuses

Array fuses are programmed using a linear select method. Each fuse can be opened by selecting the appropriate (one of 40) input line and then pulsing the correct (one of 64) product line. The levels for selecting input lines and product lines are shown in Tables 1 and 2.

Step 1 Raise PGM ENABLE to V_{IHH}.
Step 2 Select an input line by applying appropriate levels to L/R and PI pins.
Step 3 Begin selection of the output line with appropriate conditions on PA pins.
Step 4 Raise V_{CC} to V_{IHH}.
Step 5 Blow the fuse by pulsing the appropriate PO pin to V_{IHH} as shown in Table 2 for the product line.
Step 6 Return V_{CC} to 5 volts and pulse PGM Verify. The PO pin selected in Step 5 will be less than V_{OL} if the fuse is open.

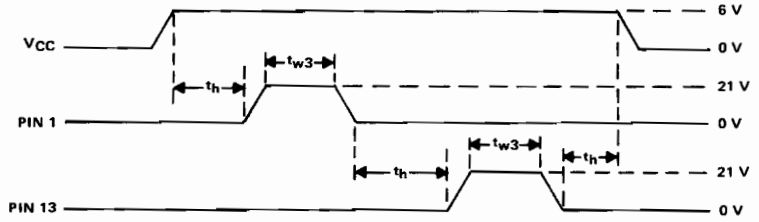
Steps 1 through 6 may be repeated if the verification does not indicate that the fuse was successfully programmed (blown), but no more than four times. Verification is possible only with the verify-protect fuse intact.

programming waveforms



(1) A high level during the verify interval indicates that programming has not been successful.
(2) A low level during the verify interval indicates that programming has been successful.

security fuse programming



PRELOAD PROCEDURES

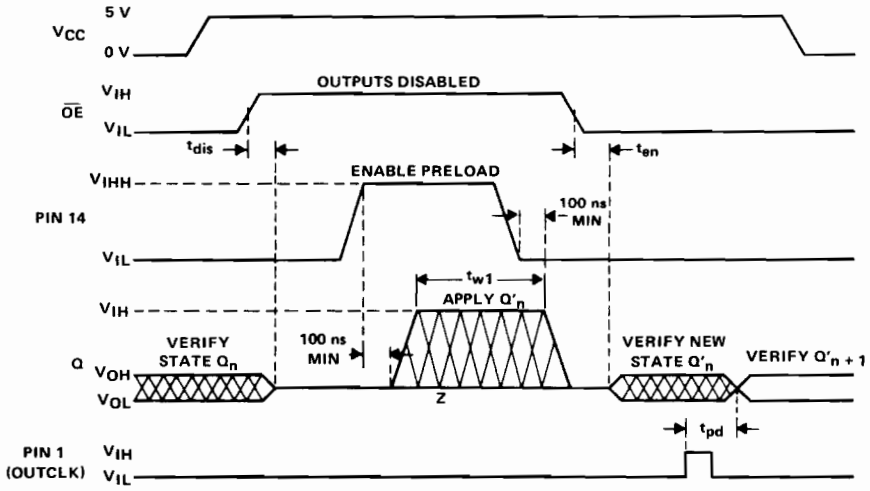


FIGURE 1. PRELOAD WAVEFORMS

preload procedure for registered outputs

Step 1	Pin 13 to V_{IH}, Pin 1 to V_{IL}, and V_{CC} to 5 volts.
Step 2	Pin 14 to V_{IHH} for 10 to 50 microseconds.
Step 3	Apply V_{IL} for a low and V_{IH} for a high at the Q outputs.
Step 4	Pin 14 to V_{IL}.
Step 5	Remove the voltages applied to the outputs.
Step 6	Pin 13 to V_{IL}.
Step 7	Check the output states to verify preload.

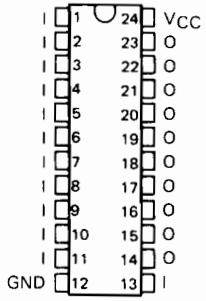
TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

JANUARY 1985

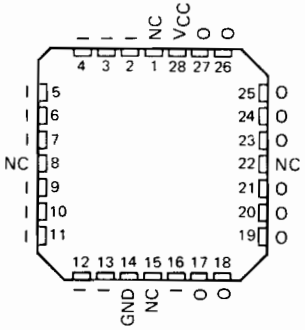
- **High-Performance Operation**
  Propagation Delay . . . 15 ns
  f_{max} . . . 50 MHz
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**

DEVICE	I INPUTS	O OUTPUTS	OUTPUT CONFIGURATION
PAL12H10	12	10	ACTIVE HIGH
PAL12L10	12	10	ACTIVE LOW
PAL12P10	12	10	POLARITY SELECT

TIBPAL12'
M SUFFIX . . . JT PACKAGE
C SUFFIX . . . JT OR NT PACKAGE
(TOP VIEW)



TIBPAL12'
M SUFFIX . . . FH OR FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



description

These programmable array logic devices feature high speed and functional equivalency when compared with currently available devices. They combine the latest Advanced Low-Power Schottky† technology "IMPACT" with proven titanium-tungsten fuses. These devices will provide reliable, high performance substitutes over conventional TTL logic. Their easy programmability allows for quick design of custom functions and typically result in a more compact circuit board. In addition, chip carriers are available for further reduction in board space.

The TIBPAL12P10 allows the user to select either active high or active low outputs. This feature is provided via a polarity fuse which is located on each EXCLUSIVE-OR output. If the fuse is left intact, the output polarity will be active high. If the fuse is blown, the output will be permanently active low.

The TIBPAL12' M series is characterized for operation over the full military temperature range of −55°C to 125°C. The TIBPAL12' C series is characterized for operation from 0°C to 70°C

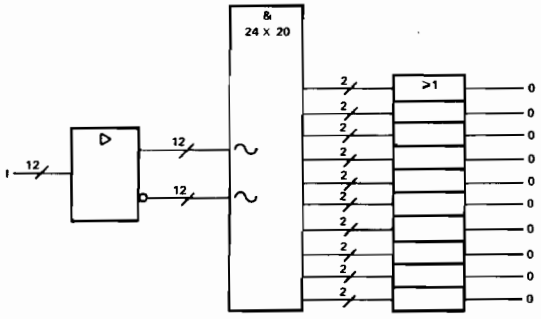
†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments, U.S. Patent Number 3,463,975.
PAL is a registered trademark of Monolithic Memories Inc.

185

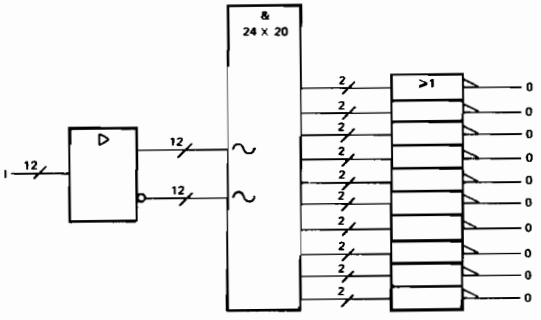
PRODUCT PREVIEW
This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

functional block diagrams (positive logic)

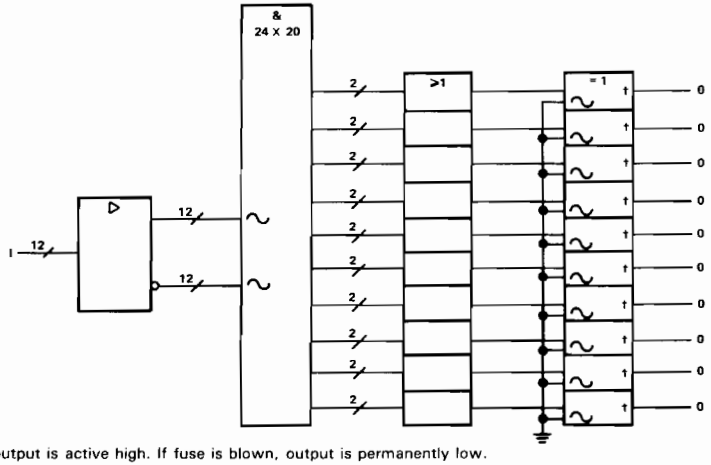
'PAL12H10



'PAL12L10



'PAL12P10



†If fuse is intact, output is active high. If fuse is blown, output is permanently low.

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

JANUARY 1985

- **High-Performance Operation**
  Propagation Delay . . . 15 ns
  f_{max} . . . 50 MHz
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**

DEVICE	I INPUTS	O OUTPUTS	OUTPUT CONFIGURATION
PAL14H8	14	8	ACTIVE HIGH
PAL14L8	14	8	ACTIVE LOW
PAL14P8	14	8	POLARITY SELECT

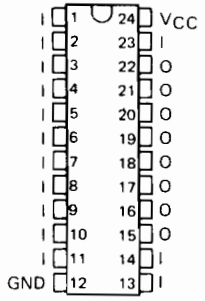
description

These programmable array logic devices feature high speed and functional equivalency when compared with currently available devices. They combine the latest Advanced Low-Power Schottky† technology "IMPACT" with proven titanium-tungsten fuses. These devices will provide reliable, high performance substitutes over conventional TTL logic. Their easy programmability allows for quick design of custom functions and typically result in a more compact circuit board. In addition, chip carriers are available for further reduction in board space.

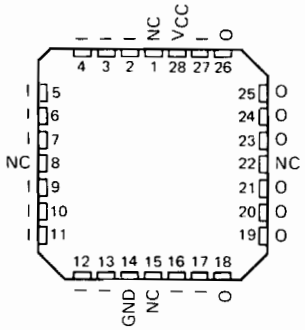
The TIBPAL14P8 allows the user to select either active high or active low outputs. This feature is provided via a polarity fuse which is located on each EXCLUSIVE-OR output. If the fuse is left intact, the output polarity will be active high. If the fuse is blown, the output will be permanently active low.

The TIBPAL14' M series is characterized for operation over the full military temperature range of −55°C to 125°C. The TIBPAL14' C series is characterized for operation from 0°C to 70°C.

TIBPAL14'
M SUFFIX . . . JT PACKAGE
C SUFFIX . . . JT OR NT PACKAGE
(TOP VIEW)



TIBPAL14'
M SUFFIX . . . FH OR FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



3

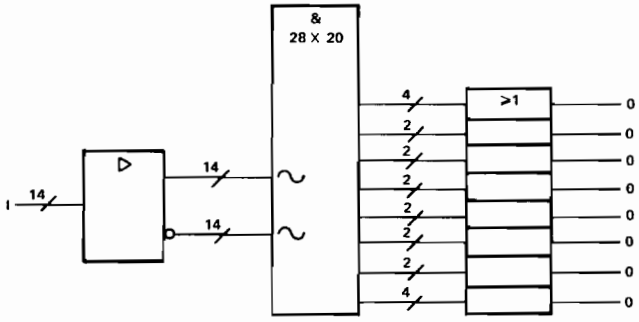
Field-Programmable Logic

†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments, U.S. Patent Number 3,463,975.
*PAL is a Trademark of Monolithic Memories Inc.

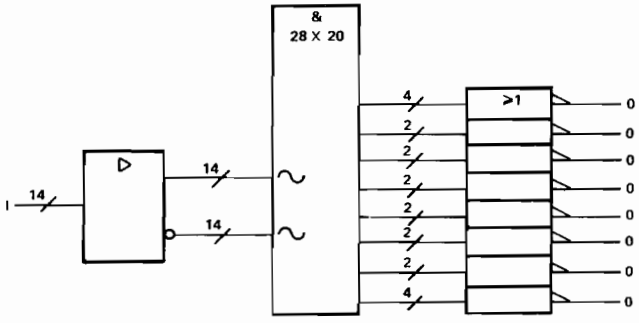
185

functional block diagrams (positive logic)

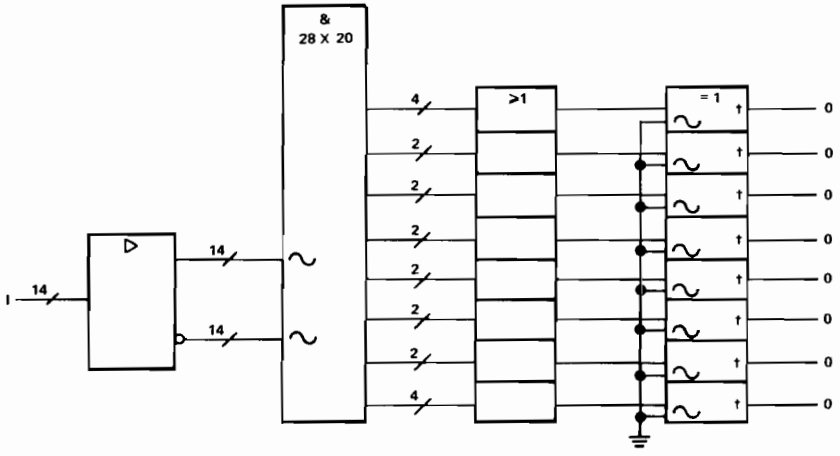
'PAL14H8



'PAL14L8



'PAL14P8



†If fuse is intact, output is active high. If fuse is blown, output is permanently low.

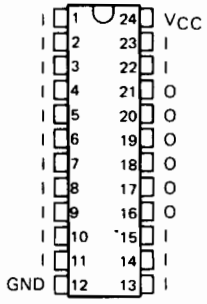
TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

JANUARY 1985

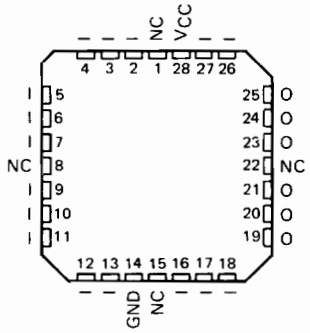
- **High-Performance Operation**
  Propagation Delay . . . 15 ns
  f_{max} . . . 50 MHz
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**

DEVICE	I INPUTS	O OUTPUTS	OUTPUT CONFIGURATION
PAL16H6	16	6	ACTIVE HIGH
PAL16L6	16	6	ACTIVE LOW
PAL16P6	16	6	POLARITY SELECT

TIBPAL16'
M SUFFIX . . . JT PACKAGE
C SUFFIX . . . JT OR NT PACKAGE
(TOP VIEW)



TIBPAL16'
M SUFFIX . . . FH OR FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



description

These programmable array logic devices feature high speed and functional equivalency when compared with currently available devices. They combine the latest Advanced Low-Power Schottky† technology "IMPACT" with proven titanium-tungsten fuses. These devices will provide reliable, high performance substitutes over conventional TTL logic. Their easy programmability allows for quick design of custom functions and typically result in a more compact circuit board. In addition, chip carriers are available for further reduction in board space.

The TIBPAL16P6 allows the user to select either active high or active low outputs. This feature is provided via a polarity fuse which is located on each EXCLUSIVE-OR output. If the fuse is left intact, the output polarity will be active high. If the fuse is blown, the output will be permanently active low.

The TIBPAL16' M series is characterized for operation over the full military temperature range of −55°C to 125°C. The TIBPAL16' C series is characterized for operation from 0°C to 70°C

3

Field-Programmable Logic

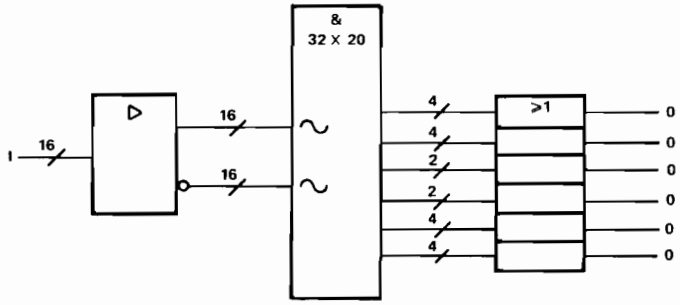
†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments, U.S. Patent Number 3,463,975.
PAL is a registered trademark of Monolithic Memories Inc.

185

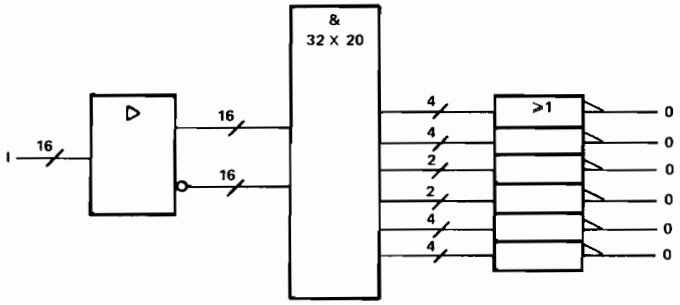
PRODUCT PREVIEW
This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

functional block diagrams (positive logic)

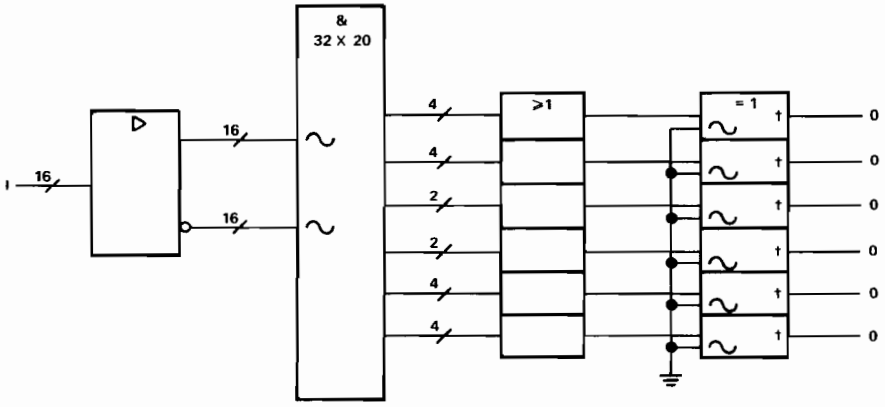
'PAL16H6



'PAL16L6



'PAL16P6



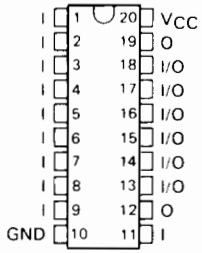
†If fuse is intact, output is active high. If fuse is blown, output is permanently low.

FEBRUARY 1984 · REVISED JANUARY 1985

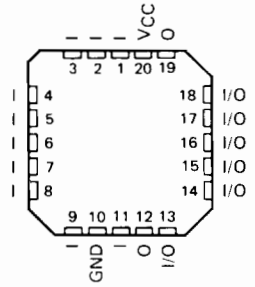
- **High-Performance Operation**
  Propagation Delay . . . 15 ns
  f_{MAX} . . . 50 MHz
- **Functionally Equivalent, but Faster than PAL16L8A, PAL16R4A, PAL16R6A, and PAL16R8A**
- **Power-Up Clear on Registered Devices (All Registered Outputs are Set Low)**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**

DEVICE	INPUTS	3-STATE O OUTPUTS	REGISTERED Q OUTPUTS	I/O PORTS
PAL16L8	10	2	0	6
PAL16R4	8	0	4 (3-state)	4
PAL16R6	8	0	6 (3-state)	2
PAL16R8	8	0	8 (3-state)	0

TIBPAL16L8'
M SUFFIX . . . J PACKAGE
C SUFFIX . . . J OR N PACKAGE
(TOP VIEW)



TIBPAL16L8'
M SUFFIX . . . FH OR FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



Pin assignments in operating mode (pins 1 and 11 less positive than $V_{(HH)}$)

description

These programmable array logic devices feature high speed and functional equivalency when compared with currently available devices. They combine the latest Advanced Low-Power Schottky† technology "IMPACT" with proven titanium-tungsten fuses. These devices will provide reliable, high-performance substitutes for conventional TTL logic. Their easy programmability allows for quick design of "custom" functions and typically results in a more compact circuit board. In addition, chip carriers are available for further reduction in board space.

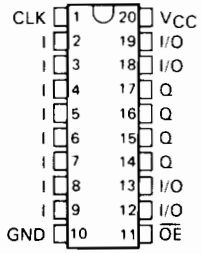
The half-power devices offer a choice of operating frequency, switching speeds, and power dissipation. In many cases, these half-power devices are fast enough to be used where the high-speed, or "A", devices are used. From an overall system level, this can amount to a significant reduction in power consumption, with no sacrifice in speed.

The PAL16' M series is characterized for operation over the full military temperature range of −55°C to 125°C. The PAL16' C series is characterized for operation from 0°C to 70°C.

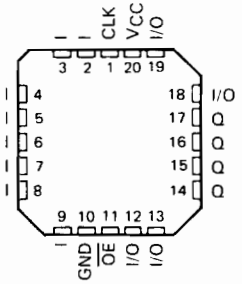
†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments, U.S. Patent Number 3,463,975.

PAL is a registered trademark of Monolithic Memories Inc.

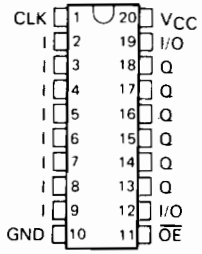
TIBPAL16R4'
M SUFFIX . . . J PACKAGE
C SUFFIX. . . J OR N PACKAGE
(TOP VIEW)



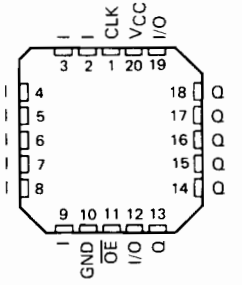
TIBPAL16R4'
M SUFFIX . . . FH OR FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



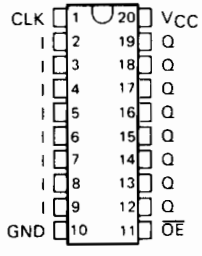
TIBPAL16R6'
M SUFFIX . . . J PACKAGE
C SUFFIX . . . J OR N PACKAGE
(TOP VIEW)



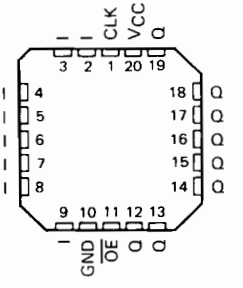
TIBPAL16R6'
M SUFFIX . . . FH OR FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



TIBPAL16R8'
M SUFFIX . . . J PACKAGE
C SUFFIX . . . J OR N PACKAGE
(TOP VIEW)



TIBPAL16R8'
M SUFFIX . . . FH OR FK PACKAGE
C SUFFIX. . . FN PACKAGE
(TOP VIEW)

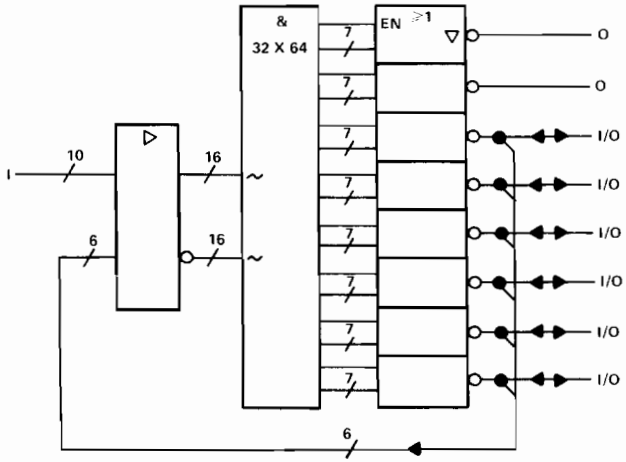


Pin assignments in operating mode (pins 1 and 11 less positive than V_{IHH})

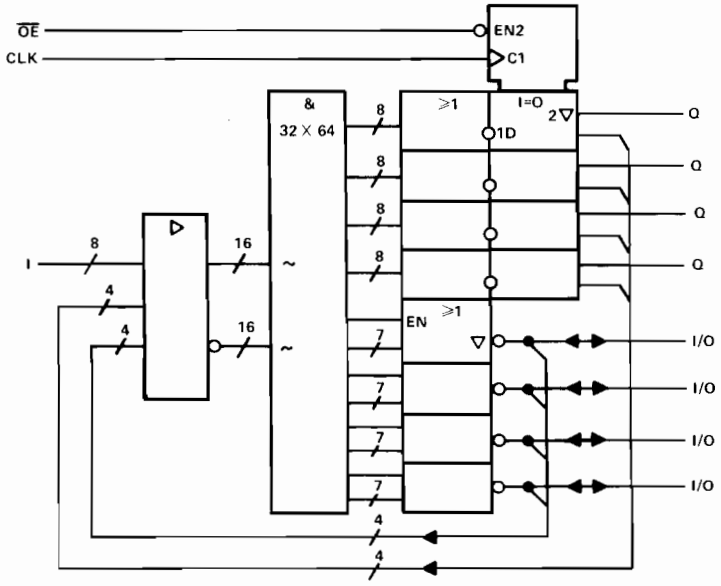
TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

functional block diagrams (positive logic)

'PAL16L8



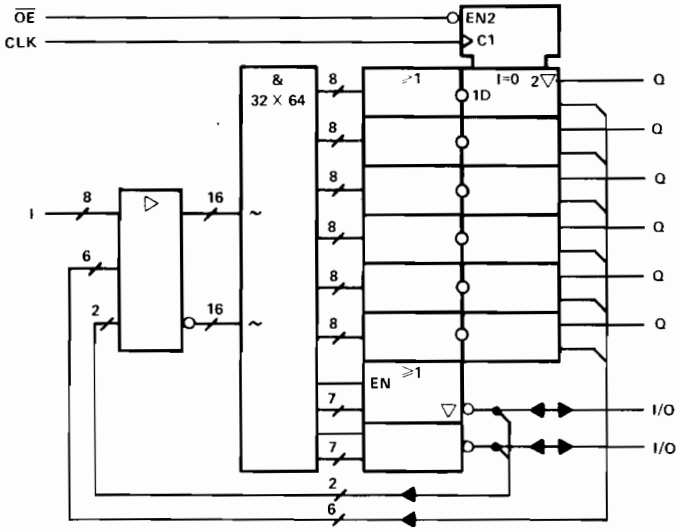
'PAL16R4



~ denotes fused inputs

functional block diagrams (positive logic)

'PAL16R6



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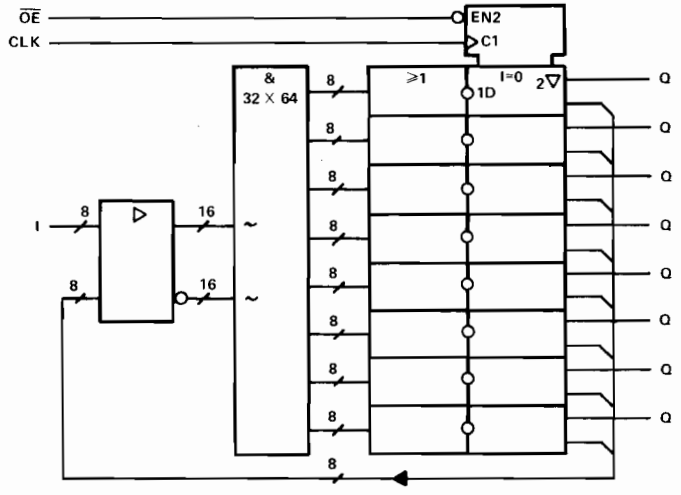
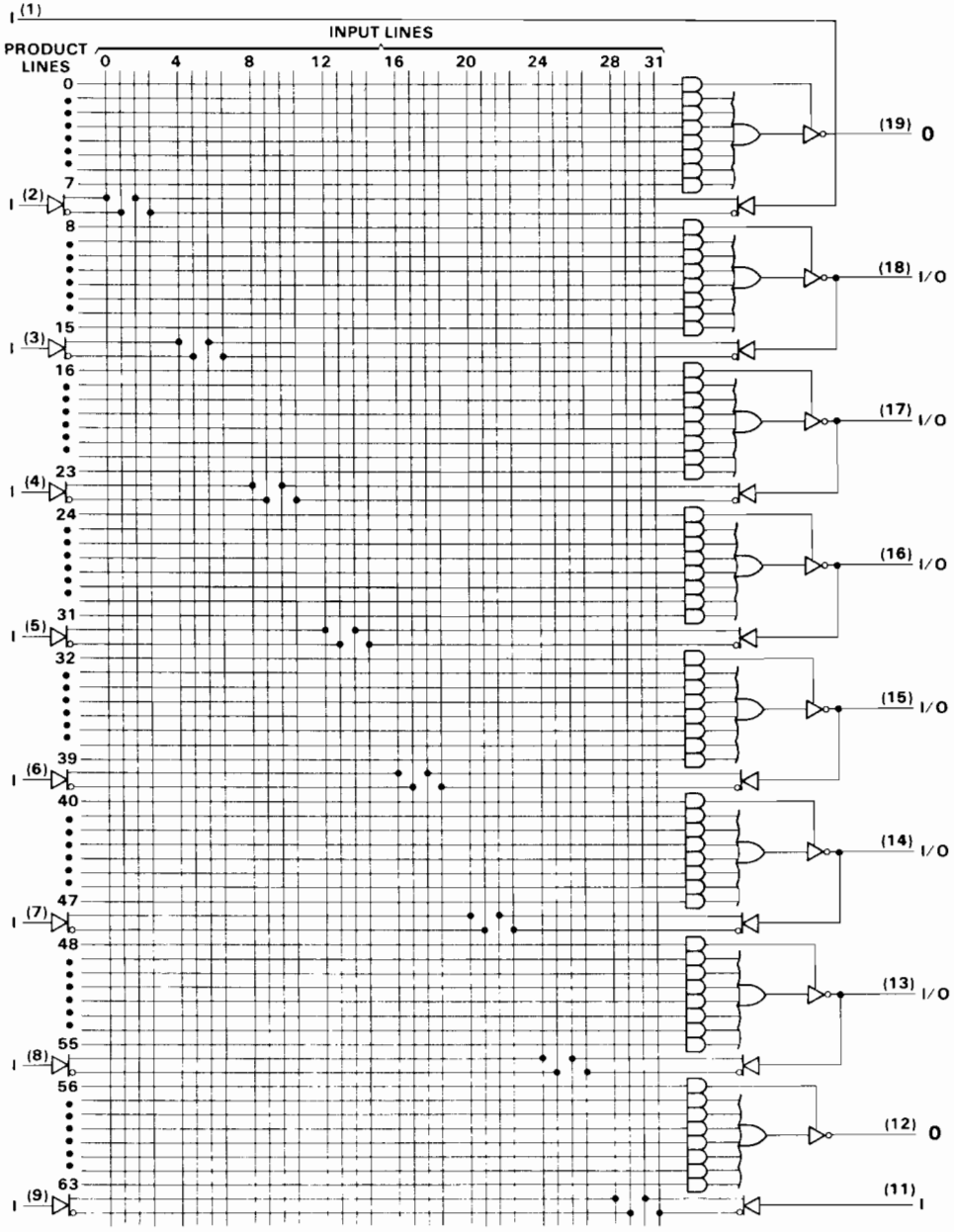
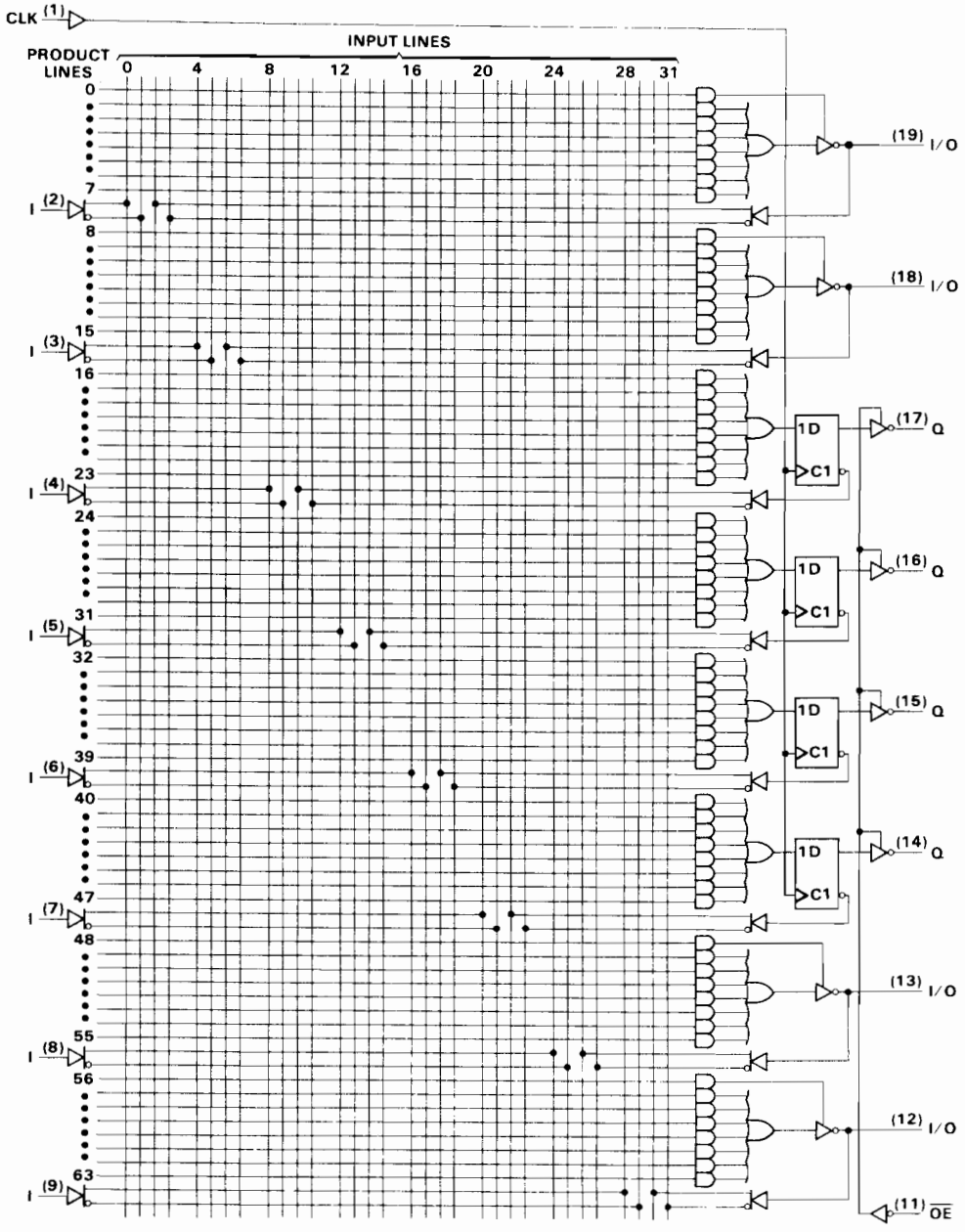


~ denotes fused inputs


(1)
INPUT LINES
PRODUCT LINES
0
4
8
12
16
20
24
28
31
0
7
(2)
8
15
(3)
16
23
(4)
24
31
(5)
32
39
(6)
40
47
(7)
48
55
(8)
56
63
(9)
(19) 0
(18) I/O
(17) I/O
(16) I/O
(15) I/O
(14) I/O
(13) I/O
(12) 0
(11) I



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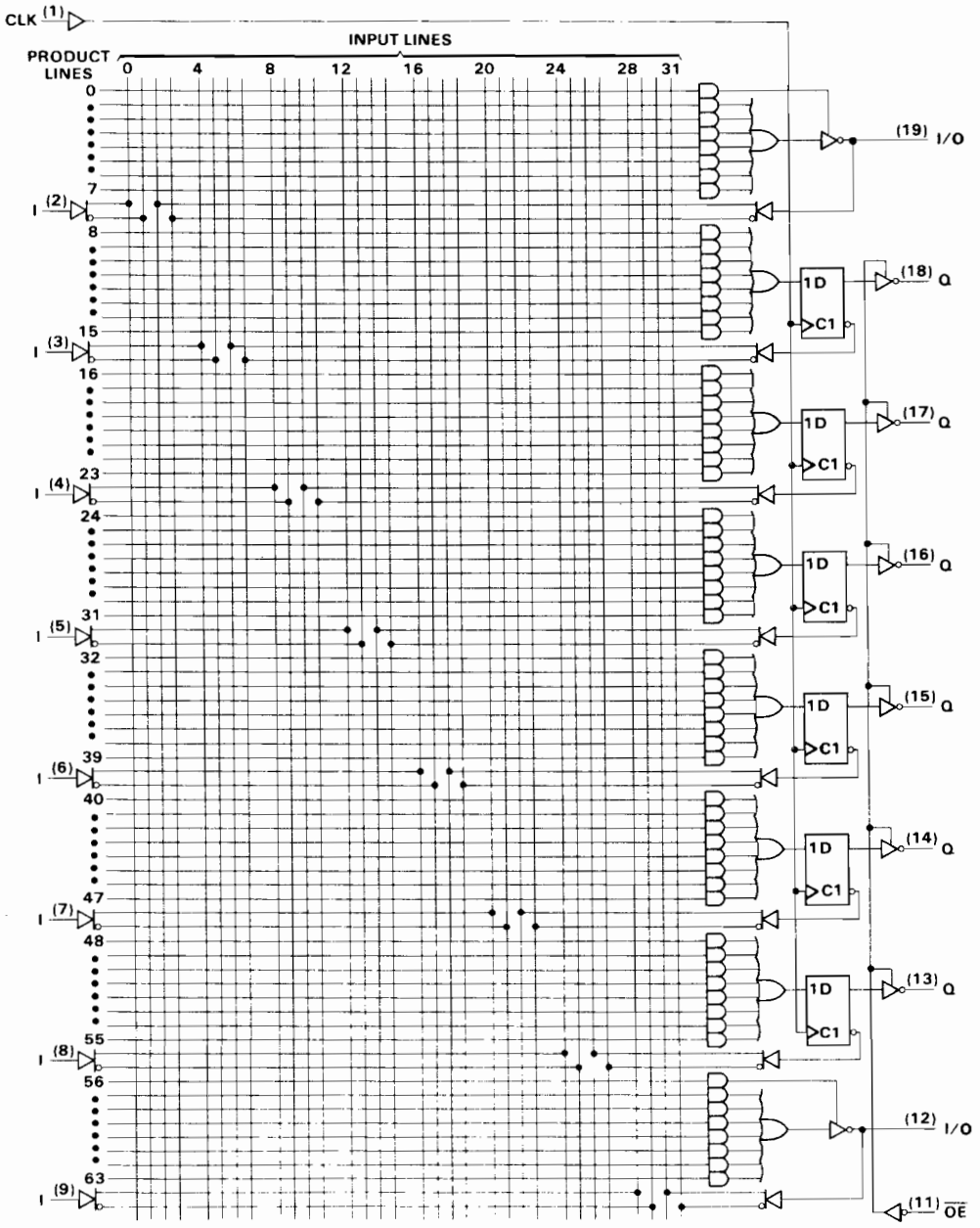
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INPUT LINES
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16
20
24
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24
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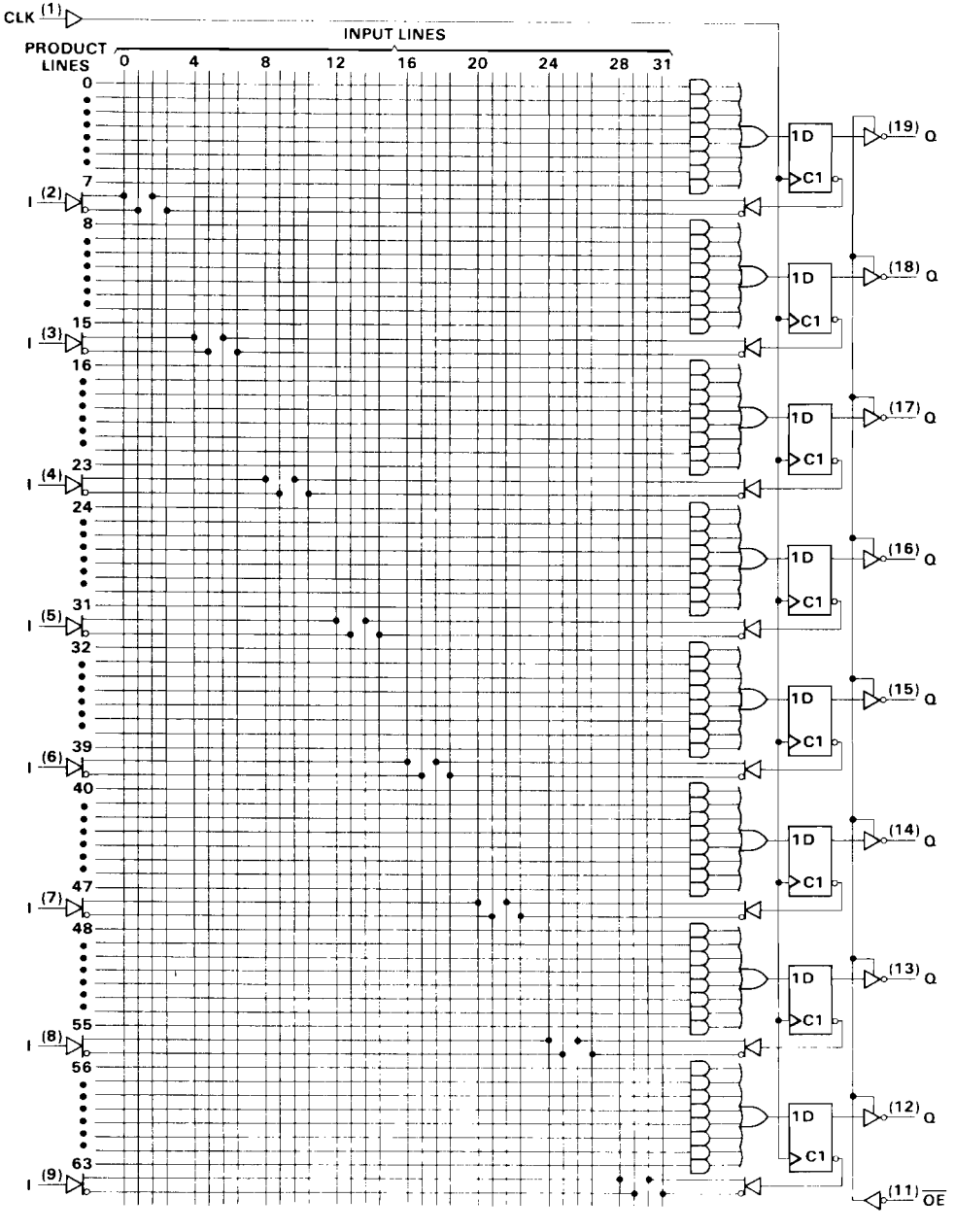
32
39
40
47
48
55
56
63
(2)
(3)
(4)
(5)
(6)
(7)
(8)
(9)
(19) I/O
(18) Q
(17) Q
(16) Q
(15) Q
(14) Q
(13) Q
(12) I/O
(11) OE
1D
C1


CLK (1)
INPUT LINES
PRODUCT LINES
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12
16
20
24
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0
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8
15
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39
40
47
48
55
56
63
(2)
(3)
(4)
(5)
(6)
(7)
(8)
(9)
1D
C1
(19) Q
(18) Q
(17) Q
(16) Q
(15) Q
(14) Q
(13) Q
(12) Q
(11) OE

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Voltage applied to a disabled output (see Note 1) . . . . . 5.5 V
Operating free-air temperature range: M suffix . . . . . −55°C to 125°C
C suffix . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1. These ratings apply except for programming pins during a programming cycle.

recommended operating conditions (see Note 2)

PARAMETER		M SUFFIX			C SUFFIX			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2		5.5	2		5.5	V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−2			−3.2	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

NOTE 2. These recommended operating conditions apply for all device dash numbers. Also refer to additional recommended operating conditions information pertaining to appropriate device dash number, i.e., −20, −15, etc.

programming parameters, T_A = 25°C

			MIN	NOM	MAX	UNIT
V_{CC}	Verify-level supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2		5.5	V
V_{IL}	Low-level input voltage				0.8	V
V_{IHH}	Program-pulse input voltage		10.25	10.5	10.75	V
I_{IHH}	Program-pulse input current	PO		20	50	mA
		PGM ENABLE, L/R		10	25	
		PI, PA		1.5	5	
		V_{CC}		250	400	
t_{w1}	Program-pulse duration at PO pins		10		50	μs
t_{w2}	Pulse duration at PGM VERIFY		100			ns
	Program-pulse duty cycle at PO pins				25	%
t_{su}	Setup time		100			ns
t_h	Hold time		100			ns
t_{d1}	Delay time from V_{CC} to 5 V to PGM VERIFY↑		100			μs
t_{d2}	Delay time from PGM VERIFY ↑ to valid output		200			ns
	Input voltage at pins 1 and 11 to open verify-protect (security) fuse		20	21	22	V
	Input current to open verify-protect (security) fuse				400	mA
t_{w3}	Pulse duration to open verify-protect (security) fuse		20		50	μs
	V_{CC} value during security fuse programming			0	0.4	V

3 Field-Programmable Logic

recommended operating conditions

			M SUFFIX –20			C SUFFIX –15			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
f_{clock}	Clock frequency		0		40	0		50	MHz
t_w	Pulse duration, clock, (see Note 3)	High	10			8			ns
		Low	11			9			
t_{su}	Setup time, input or feedback before CLK↑		20			15			ns
t_h	Hold time, input or feedback after CLK↑		0			0			ns

NOTE 3: The total clock period of CLK high and CLK low must not exceed clock frequency, f_{clock}. Minimum pulse durations specified are only for CLK high or CLK low, but not for both simultaneously.

electrical characteristics, over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS†		M SUFFIX –20			C SUFFIX –15			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = MIN, I_I = –18 mA				–1.5			–1.5	V
V_{OH}		V_{CC} = MIN, I_{OH} = MAX		2.4	3.2		2.4	3.3		V
V_{OL}		V_{CC} = MIN, I_{OL} = MAX			0.25	0.4		0.35	0.5	V
I_{OZH}	Outputs	V_{CC} = MAX, V_O = 2.7 V				20			20	μA
	I/O ports					100			100	
I_{OZL}	Outputs	V_{CC} = MAX, V_O = 0.4 V				–20			–20	μA
	I/O ports					–250			–250	
I_I		V_{CC} = MAX, V_I = 5.5 V	Pin 1, 11			0.2			0.1	mA
			All others			0.1			0.1	
I_{IH}		V_{CC} = MAX, V_I = 2.7 V	Pin 1, 11			50			20	μA
			All others			20			20	
I_{IL}		V_{CC} = MAX, V_I = 0.4 V				–0.2			–0.2	mA
I_O§		V_{CC} = MAX, V_O = 2.25 V		–30		–125	–30		–125	mA
I_{CC}		V_{CC} = MAX, V_I = 0 V, Outputs Open			140	190		140	180	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics over recommended supply voltage and operating free-air temperature ranges (unless otherwise noted)

PARAMETER	FROM	TO	TEST CONDITIONS	M SUFFIX –20			C SUFFIX –15			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
f_{max}			R_L = 500 Ω, C_L = 50 pF, See Note 4	40			50			MHz
t_{pd}	I, I/O	O, I/O			10	20		10	15	ns
t_{pd}	CLK↑	Q			8	15		8	12	ns
t_{en}	OE↓	Q			8	15		8	12	ns
t_{dis}	OE↑	Q			7	15		7	10	ns
t_{en}	I, I/O	O, I/O			10	20		10	15	ns
t_{dis}	I, I/O	O, I/O			10	20		10	15	ns

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 4: Load circuits and voltage waveforms are shown in Section 1.

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recommended operating conditions

			M SUFFIX −30			C SUFFIX −25			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
f_{clock}	Clock frequency		0		25	0		30	MHz
t_w	Pulse duration, clock, (see Note 3)	High	15			10			ns
		Low	20			15			
t_{su}	Setup time, input or feedback before CLK↑		25			20			ns
t_h	Hold time, input or feedback after CLK↑		0			0			ns

NOTE 3: The total clock period of CLK high and CLK low must not exceed clock frequency, f_{clock}. Minimum pulse durations specified are only for CLK high or CLK low, but not for both simultaneously.

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS†		M SUFFIX −30			C SUFFIX −25			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}		V_{CC} = MIN, I_{OH} = MAX		2.4	3.2		2.4	3.3		V
V_{OL}		V_{CC} = MIN, I_{OL} = MAX			0.25	0.4		0.35	0.5	V
I_{OZH}	Outputs	V_{CC} = MAX, V_O = 2.7 V				20			20	μA
	I/O ports					100			100	
I_{OZL}	Outputs	V_{CC} = MAX, V_O = 0.4 V				−20			−20	μA
	I/O ports					−250			−250	
I_I		V_{CC} = MAX, V_I = 5.5 V	Pin 1, 11			0.2			0.1	mA
			All others			0.1			0.1	
I_{IH}		V_{CC} = MAX, V_I = 2.7 V	Pin 1, 11			50			20	μA
			All others			20			20	
I_{IL}		V_{CC} = MAX, V_I = 0.4 V				−0.2			−0.2	mA
I_O§		V_{CC} = MAX, V_O = 2.25 V		−30		−125	−30		−125	mA
I_{CC}		V_{CC} = MAX, V_I = 0 V, Outputs Open			75	105		75	100	mA

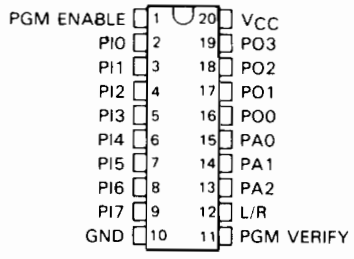
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics over recommended supply voltage and operating free-air temperature ranges (unless otherwise noted)

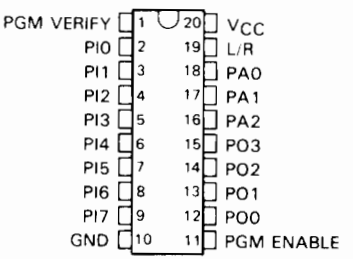
PARAMETER	FROM	TO	TEST CONDITIONS	M SUFFIX −30			C SUFFIX −25			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
f_{max}			R_L = 500 Ω, C_L = 50 pF, See Note 4	25			30			MHz
t_{pd}	I, I/O	O, I/O			15	30		15	25	ns
t_{pd}	CLK↑	Q			10	20		10	15	ns
t_{en}	OE↓	Q			15	25		15	20	ns
t_{dis}	OE↑	Q			10	25		10	20	ns
t_{en}	I, I/O	O, I/O			14	30		14	25	ns
t_{dis}	I, I/O	O, I/O			13	30		13	25	ns

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 4: Load circuits and voltage waveforms are shown in Section 1.

PRODUCT TERMS 0 THRU 31
(TOP VIEW)



PRODUCT TERMS 32 THRU 63
(TOP VIEW)



Pin assignments in programming mode (PGM ENABLE, pin 1 or 11, at V_{IHH})

TABLE 1 — INPUT LINE SELECT

INPUT LINE NUMBER	PIN NAME								
	PI7	PI6	PI5	PI4	PI3	PI2	PI1	PI0	L/R
0	HH	HH	HH	HH	HH	HH	HH	L	Z
1	HH	HH	HH	HH	HH	HH	HH	H	Z
2	HH	HH	HH	HH	HH	HH	HH	L	HH
3	HH	HH	HH	HH	HH	HH	HH	H	HH
4	HH	HH	HH	HH	HH	HH	L	HH	Z
5	HH	HH	HH	HH	HH	HH	H	HH	Z
6	HH	HH	HH	HH	HH	HH	L	HH	HH
7	HH	HH	HH	HH	HH	HH	H	HH	HH
8	HH	HH	HH	HH	HH	L	HH	HH	Z
9	HH	HH	HH	HH	HH	H	HH	HH	Z
10	HH	HH	HH	HH	HH	L	HH	HH	HH
11	HH	HH	HH	HH	HH	H	HH	HH	HH
12	HH	HH	HH	HH	L	HH	HH	HH	Z
13	HH	HH	HH	HH	H	HH	HH	HH	Z
14	HH	HH	HH	HH	L	HH	HH	HH	HH
15	HH	HH	HH	HH	H	HH	HH	HH	HH
16	HH	HH	HH	L	HH	HH	HH	HH	Z
17	HH	HH	HH	H	HH	HH	HH	HH	Z
18	HH	HH	HH	L	HH	HH	HH	HH	HH
19	HH	HH	HH	H	HH	HH	HH	HH	HH
20	HH	HH	L	HH	HH	HH	HH	HH	Z
21	HH	HH	H	HH	HH	HH	HH	HH	Z
22	HH	HH	L	HH	HH	HH	HH	HH	HH
23	HH	HH	H	HH	HH	HH	HH	HH	HH
24	HH	L	HH	HH	HH	HH	HH	HH	Z
25	HH	H	HH	HH	HH	HH	HH	HH	Z
26	HH	L	HH	HH	HH	HH	HH	HH	HH
27	HH	H	HH	HH	HH	HH	HH	HH	HH
28	L	HH	HH	HH	HH	HH	HH	HH	Z
29	H	HH	HH	HH	HH	HH	HH	HH	Z
30	L	HH	HH	HH	HH	HH	HH	HH	HH
31	H	HH	HH	HH	HH	HH	HH	HH	HH

TABLE 2 — PRODUCT LINE SELECT

PRODUCT LINE NUMBER	PIN NAME						
	PO0	PO1	PO2	PO3	PA2	PA1	PA0
0, 32	Z	Z	Z	HH	Z	Z	Z
1, 33	Z	Z	Z	HH	Z	Z	HH
2, 34	Z	Z	Z	HH	Z	HH	Z
3, 35	Z	Z	Z	HH	Z	HH	HH
4, 36	Z	Z	Z	HH	HH	Z	Z
5, 37	Z	Z	Z	HH	HH	Z	HH
6, 38	Z	Z	Z	HH	HH	HH	Z
7, 39	Z	Z	Z	HH	HH	HH	HH
8, 40	Z	Z	HH	Z	Z	Z	Z
9, 41	Z	Z	HH	Z	Z	Z	HH
10, 42	Z	Z	HH	Z	Z	HH	Z
11, 43	Z	Z	HH	Z	Z	HH	HH
12, 44	Z	Z	HH	Z	HH	Z	Z
13, 45	Z	Z	HH	Z	HH	Z	HH
14, 46	Z	Z	HH	Z	HH	HH	Z
15, 47	Z	Z	HH	Z	HH	HH	HH
16, 48	Z	HH	Z	Z	Z	Z	Z
17, 49	Z	HH	Z	Z	Z	Z	HH
18, 50	Z	HH	Z	Z	Z	HH	Z
19, 51	Z	HH	Z	Z	Z	HH	HH
20, 52	Z	HH	Z	Z	HH	Z	Z
21, 53	Z	HH	Z	Z	HH	Z	HH
22, 54	Z	HH	Z	Z	HH	HH	Z
23, 55	Z	HH	Z	Z	HH	HH	HH
24, 56	HH	Z	Z	Z	Z	Z	Z
25, 57	HH	Z	Z	Z	Z	Z	HH
26, 58	HH	Z	Z	Z	Z	HH	Z
27, 59	HH	Z	Z	Z	Z	HH	HH
28, 60	HH	Z	Z	Z	HH	Z	Z
29, 61	HH	Z	Z	Z	HH	Z	HH
30, 62	HH	Z	Z	Z	HH	HH	Z
31, 63	HH	Z	Z	Z	HH	HH	HH

L = V_{IL}, H = V_{IH}, HH = V_{IHH}, Z = high impedance (e.g., 10 kΩ to 5 V)

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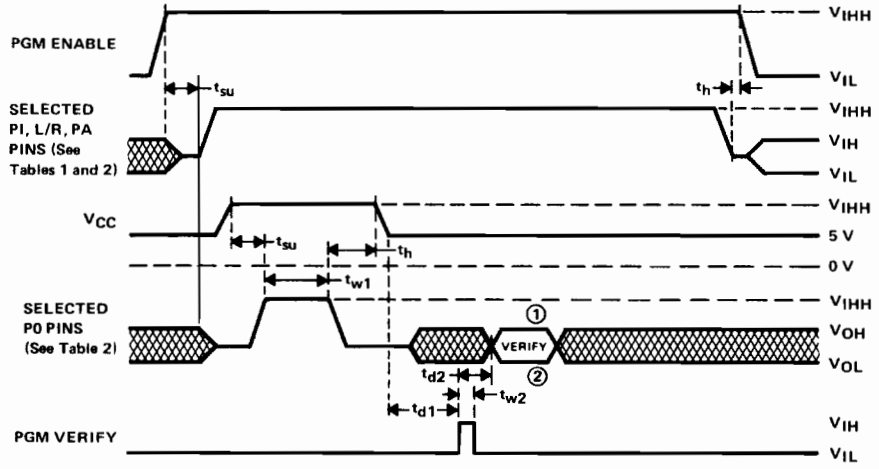
programming procedure for array fuses

Array fuses are programmed using a linear select method. Each fuse can be opened by selecting the appropriate (one of 32) input line and then pulsing the correct (one of 64) product line. The levels for selecting input lines and product lines are shown in Tables 1 and 2.

Step 1 Raise PGM ENABLE to V_{IHH}.
Step 2 Select an input line by applying appropriate levels to L/R and PI pins.
Step 3 Begin selection of the output line with appropriate conditions on PA pins.
Step 4 Raise V_{CC} to V_{IHH}.
Step 5 Blow the fuse by pulsing the appropriate PO pin to V_{IHH} as shown in Table 2 for the product line.
Step 6 Return V_{CC} to 5 volts and pulse PGM Verify. The PO pin selected in Step 5 will be less than V_{OL} if the fuse is open.

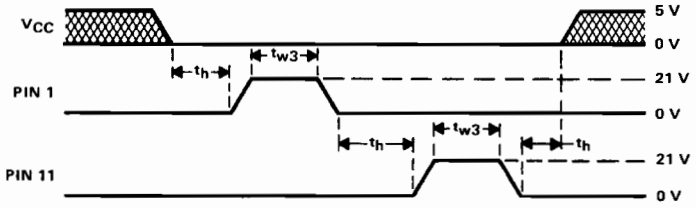
Steps 1 through 6 may be repeated if the verification does not indicate that the fuse was successfully programmed (blown), but no more than four times. Verification is possible only with the verify-protect fuse intact.

programming waveforms



① A high level during verify interval indicates that programming has not been successful.
② A low level during verify interval indicates that programming has been successful.

security fuse programming



JANUARY 1985

- **High-Performance Operation**
  Propagation Delay . . . 15 ns
  f_{max} . . . 50 MHz
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**

DEVICE	I INPUTS	O OUTPUTS	OUTPUT CONFIGURATION
TIBPAL18H4	18	4	ACTIVE HIGH
TIBPAL18L4	18	4	ACTIVE LOW
TIBPAL18P4	18	4	POLARITY SELECT

description

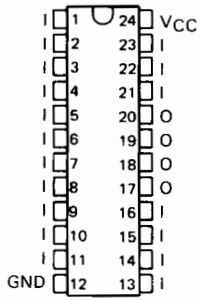
These programmable array logic devices feature high speed and functional equivalency when compared with currently available devices. They combine the latest Advanced Low-Power Schottky† technology "IMPACT" with proven titanium-tungsten fuses. These devices will provide reliable, high performance substitutes over conventional TTL logic. Their easy programmability allows for quick design of custom functions and typically result in a more compact circuit board. In addition, chip carriers are available for further reduction in board space.

The TIBPAL18P4 allows the user to select either active high or active low outputs. This feature is provided via a polarity fuse which is located on each EXCLUSIVE-OR output. If the fuse is left intact, the output polarity will be active high. If the fuse is blown, the output will be permanently active low.

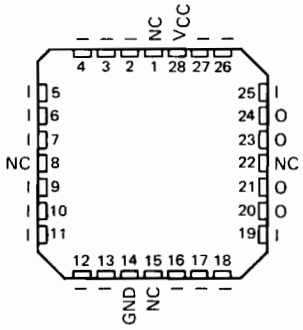
The TIBPAL18' M series is characterized for operation over the full military temperature range of −55°C to 125°C. The TIBPAL18' C series is characterized for operation from 0°C to 70°C.

†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments, U.S. Patent Number 3,463,975.
PAL is a registered trademark of Monolithic Memories Inc.

TIBPAL18'
M SUFFIX . . . JT PACKAGE
C SUFFIX . . . JT OR NT PACKAGE
(TOP VIEW)



TIBPAL18'
M SUFFIX . . . FH OR FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



3

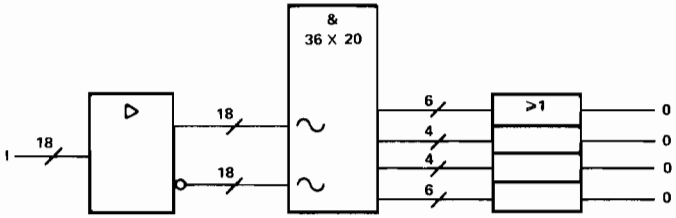
Field-Programmable Logic

5

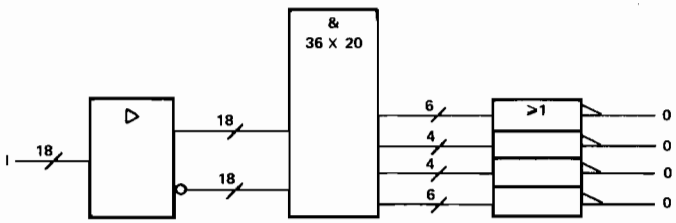
PRODUCT PREVIEW
This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

functional block diagrams (positive logic)

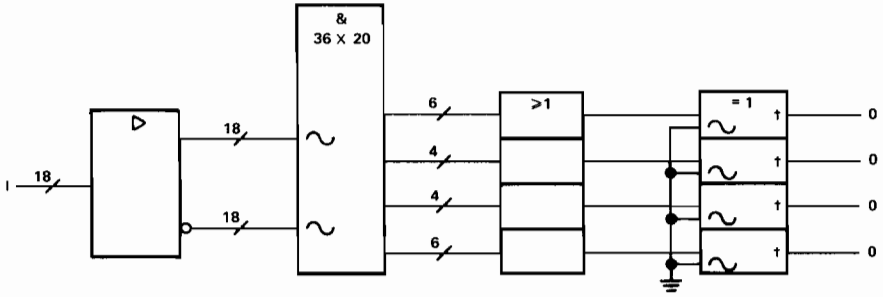
'PAL18H4



'PAL18L4



'PAL18P4



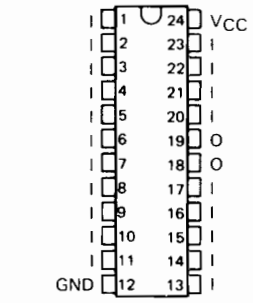
†If fuse is intact, output is active high. If fuse is blown, output is permanently low.

JANUARY 1985

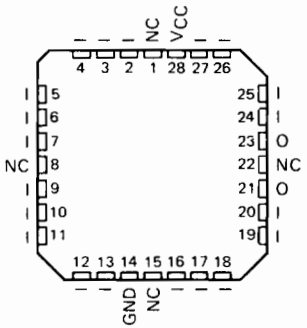
- **High-Performance Operation**
  Propagation Delay . . . 15 ns
  f_{max} . . . 50 MHz
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**

DEVICE	I INPUTS	O OUTPUTS	OUTPUT CONFIGURATION
TIBPAL20H2	20	2	ACTIVE HIGH
TIBPAL20L2	20	2	ACTIVE LOW
TIBPAL20P2	20	2	POLARITY SELECT

TIBPAL20'
M SUFFIX . . . JT PACKAGE
C SUFFIX . . . JT OR NT PACKAGE
(TOP VIEW)



TIBPAL20'
M SUFFIX . . . FH OR FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



description

These programmable array logic devices feature high speed and functional equivalency when compared with currently available devices. They combine the latest Advanced Low-Power Schottky† technology "IMPACT" with proven titanium-tungsten fuses. These devices will provide reliable, high performance substitutes over conventional TTL logic. Their easy programmability allows for quick design of custom functions and typically result in a more compact circuit board. In addition, chip carriers are available for further reduction in board space.

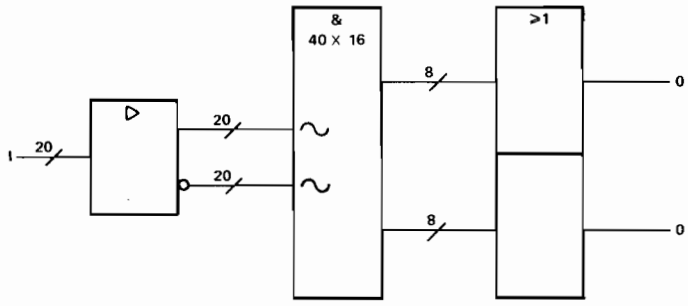
The TIBPAL20P2 allows the user to select either active high or active low outputs. This feature is provided via a polarity fuse which is located on each EXCLUSIVE-OR output. If the fuse is left intact, the output polarity will be active high. If the fuse is blown, the output will be permanently active low.

The TIBPAL20' M series is characterized for operation over the full military temperature range of −55°C to 125°C. The TIBPAL20' C series is characterized for operation from 0°C to 70°C

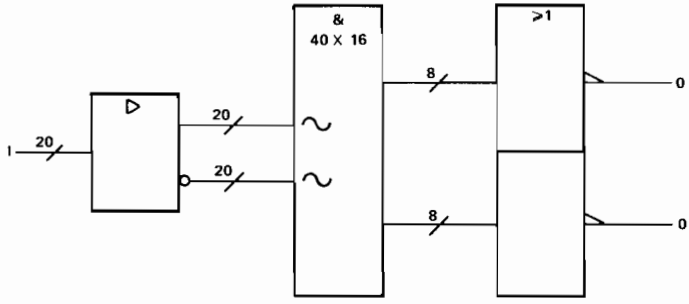
†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments, U.S. Patent Number 3,463,975.
PAL is a registered trademark of Monolithic Memories Inc.

functional block diagrams (positive logic)

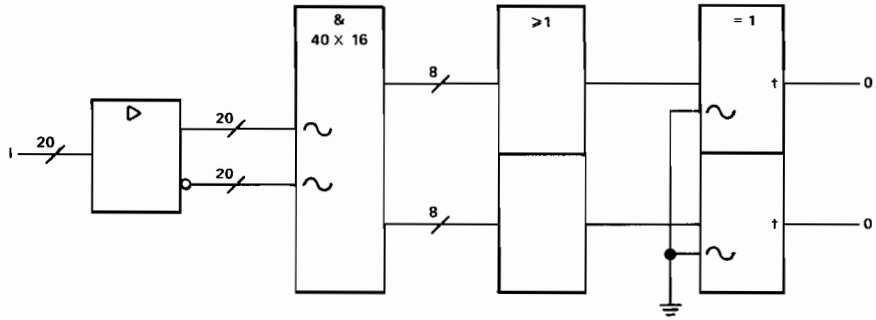
'PAL20H2



'PAL20L2



'PAL20P2



†If fuse is intact, output is active high. If fuse is blown, output is permanently low.

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

SEPTEMBER 1984

- **Choice of Operating Speeds**
  HIGH PERFORMANCE . . . 40 MHz Typical
  HALF-POWER . . . 25 MHz Typical
- **Preload Capability on Output Registers**
- **Power-Up Clear on Registered Devices**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**

DEVICE	I INPUTS	3-STATE O OUTPUTS	REGISTERED Q OUTPUTS	I/O PORTS
'PAL20L10	12	2	0	8
'PAL20X4	10	0	4 (3-state buffers)	6
'PAL20X8	10	0	8 (3-state buffers)	2
'PAL20X10	10	0	10 (3-state buffers)	0

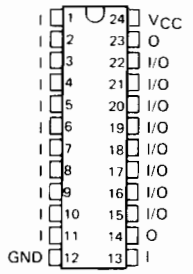
description

These programmable array logic devices feature high speed and functional equivalency when compared with currently available devices. They combine the latest Advanced Low-Power Schottky† technology "IMPACT" with proven titanium-tungsten fuses. These devices will provide reliable, high performance substitutes over conventional TTL logic. Their easy programmability allows for quick design of custom functions and typically result in a more compact circuit board. In addition, chip carriers are available for further reduction in board space.

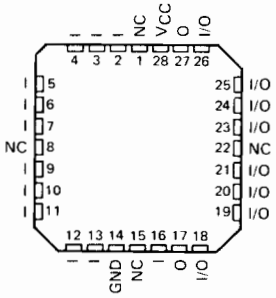
The Half-Power versions offer a choice of operating frequency, switching speeds, and power dissipation. In many cases, these Half-Power devices are as fast as the currently available "standard" devices.

All of the registered outputs are set to a low level during power-up. In addition, extra circuitry has been provided to allow loading of each register asynchronously to either a high or low state. This feature simplifies testing because the registers can be set to an initial state prior to executing the test sequence.

TIBPAL20L10'
M SUFFIX . . . JT PACKAGE
C SUFFIX . . . JT OR NT PACKAGE
(TOP VIEW)



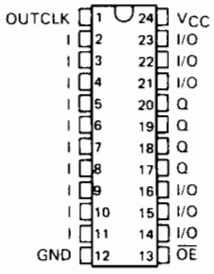
TIBPAL20L10'
M SUFFIX . . . FH OR FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



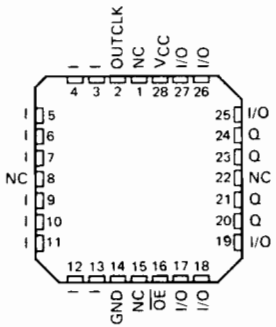
Pin assignments in operating mode (pins 1 and 11 less positive than V_{IHH})

†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments, U.S. Patent Number 3,463,975.
PAL is a registered trademark of Monolithic Memories Inc.

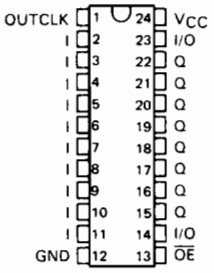
TIBPAL20X4'
M SUFFIX . . . JT PACKAGE
C SUFFIX . . . JT OR NT PACKAGE
(TOP VIEW)



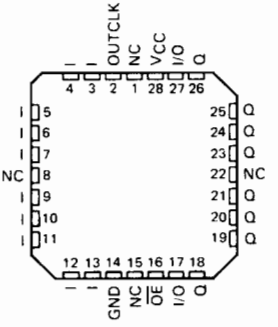
TIBPAL20X4'
M SUFFIX . . . FH OR FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



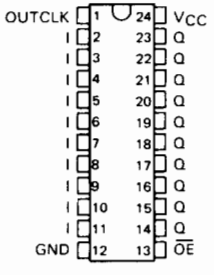
TIBPAL20X8'
M SUFFIX . . . JT PACKAGE
C SUFFIX . . . JT OR NT PACKAGE
(TOP VIEW)



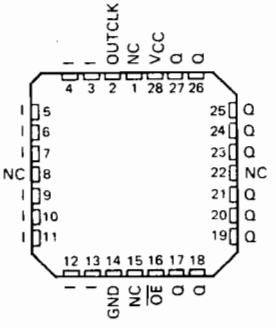
TIBPAL20X8'
M SUFFIX . . . FH OR FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



TIBPAL20X10'
M SUFFIX . . . JT PACKAGE
C SUFFIX . . . JT OR NT PACKAGE
(TOP VIEW)



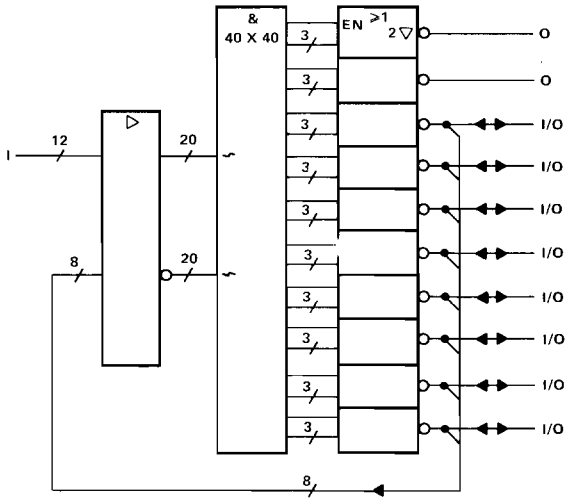
TIBPAL20X10'
M SUFFIX . . . FH OR FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



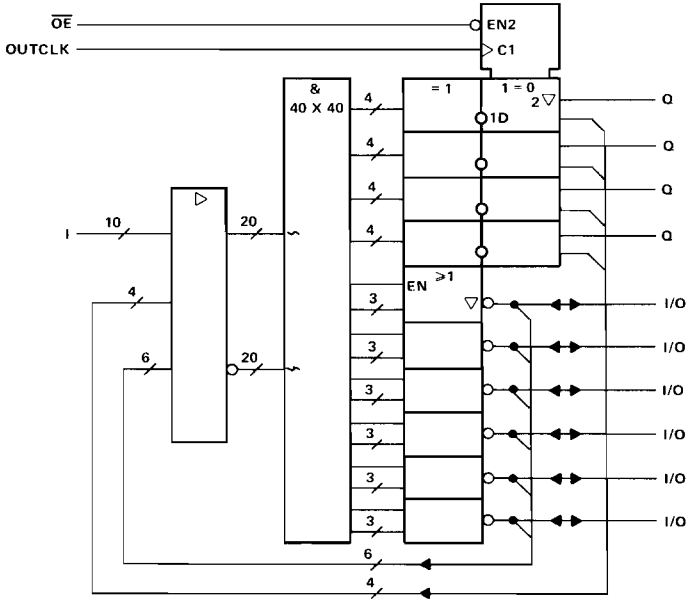
Pin assignments in operating mode (pins 1 and 11 less positive than V_{IHH})

functional block diagrams (positive logic)

'PAL20L10



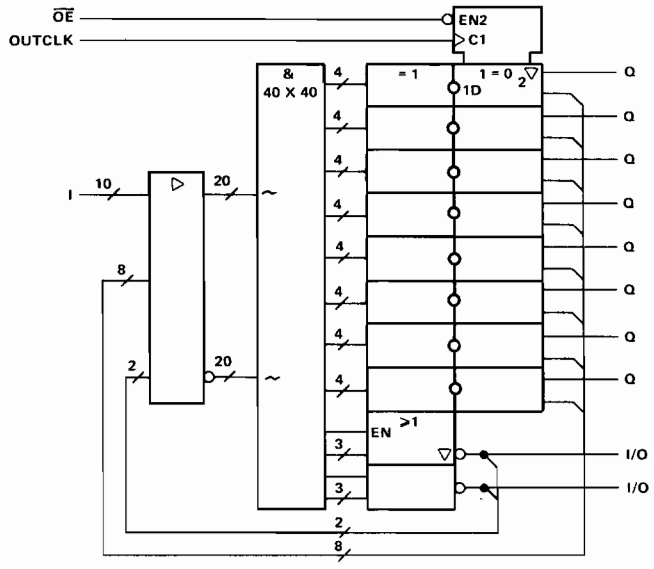
'PAL20X4



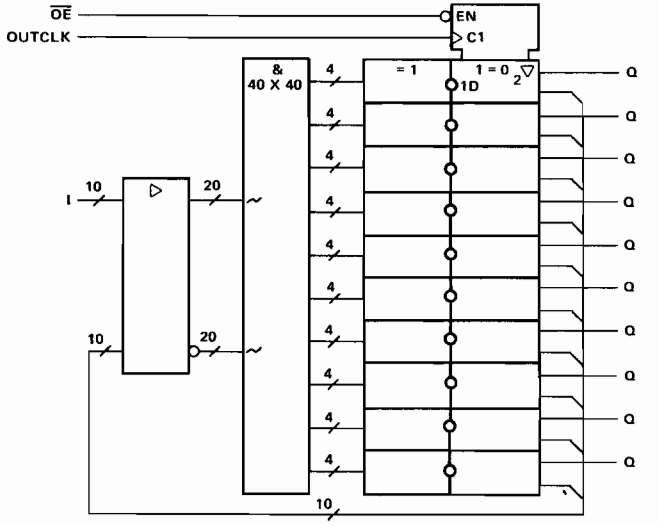
~ denotes fused inputs

functional block diagrams (positive logic)

'PAL20X8

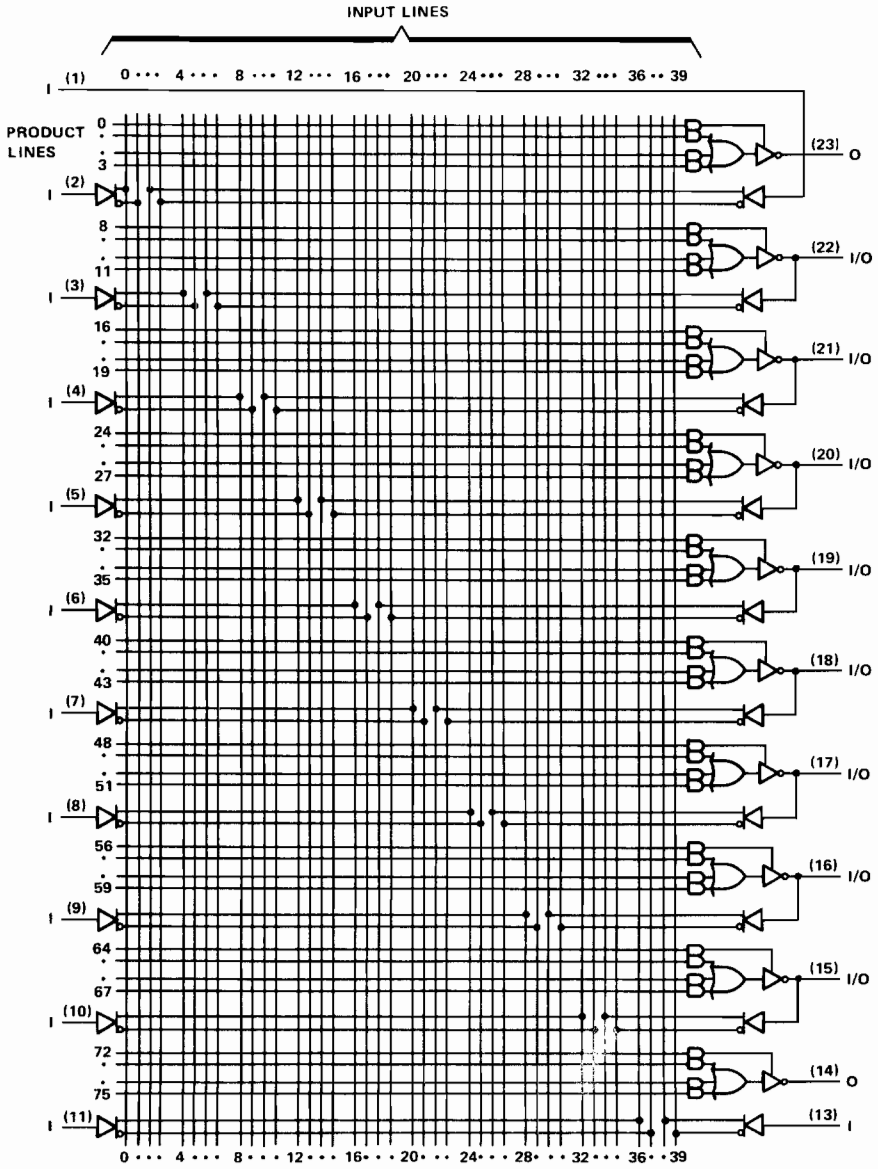


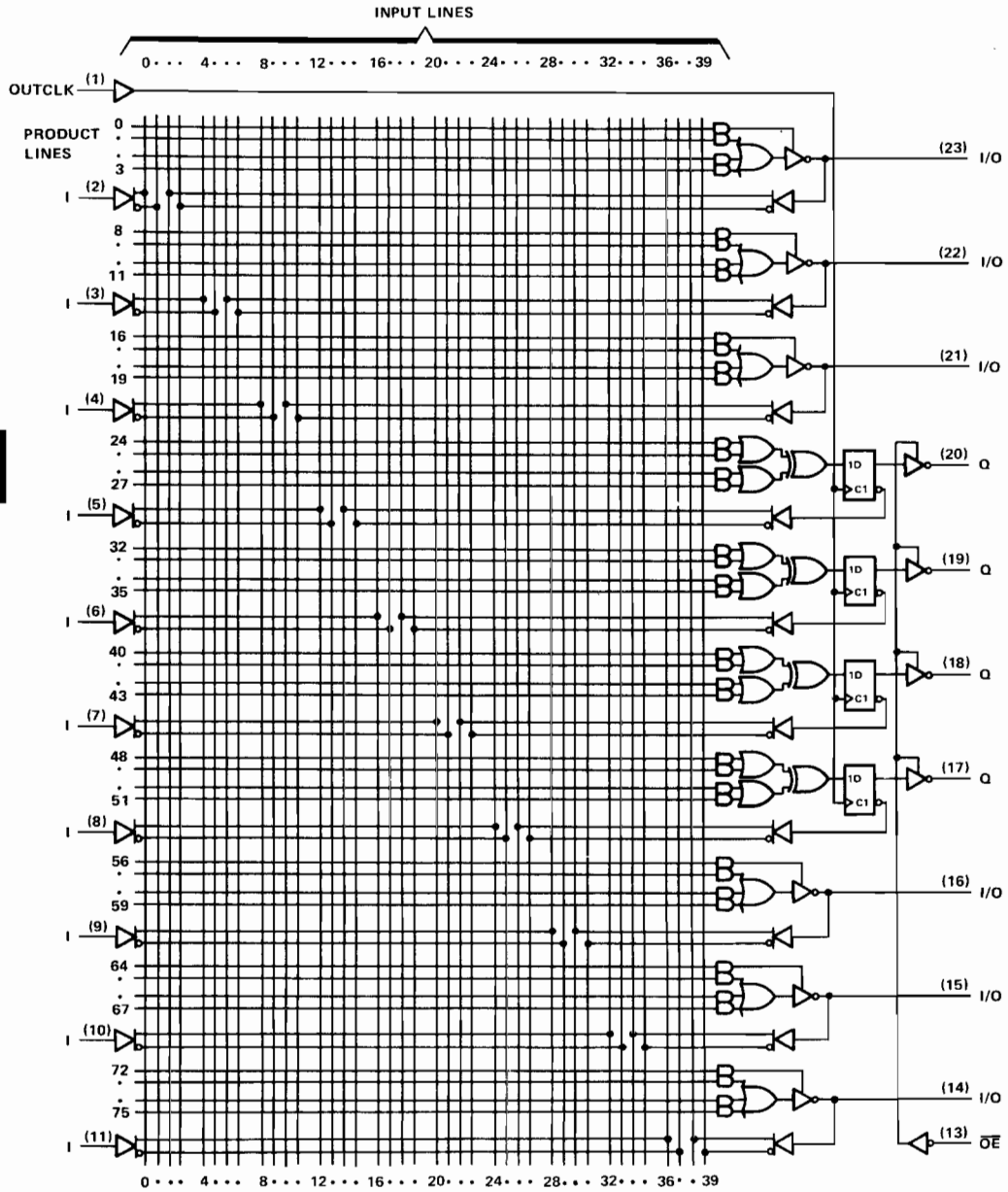
'PAL20X10



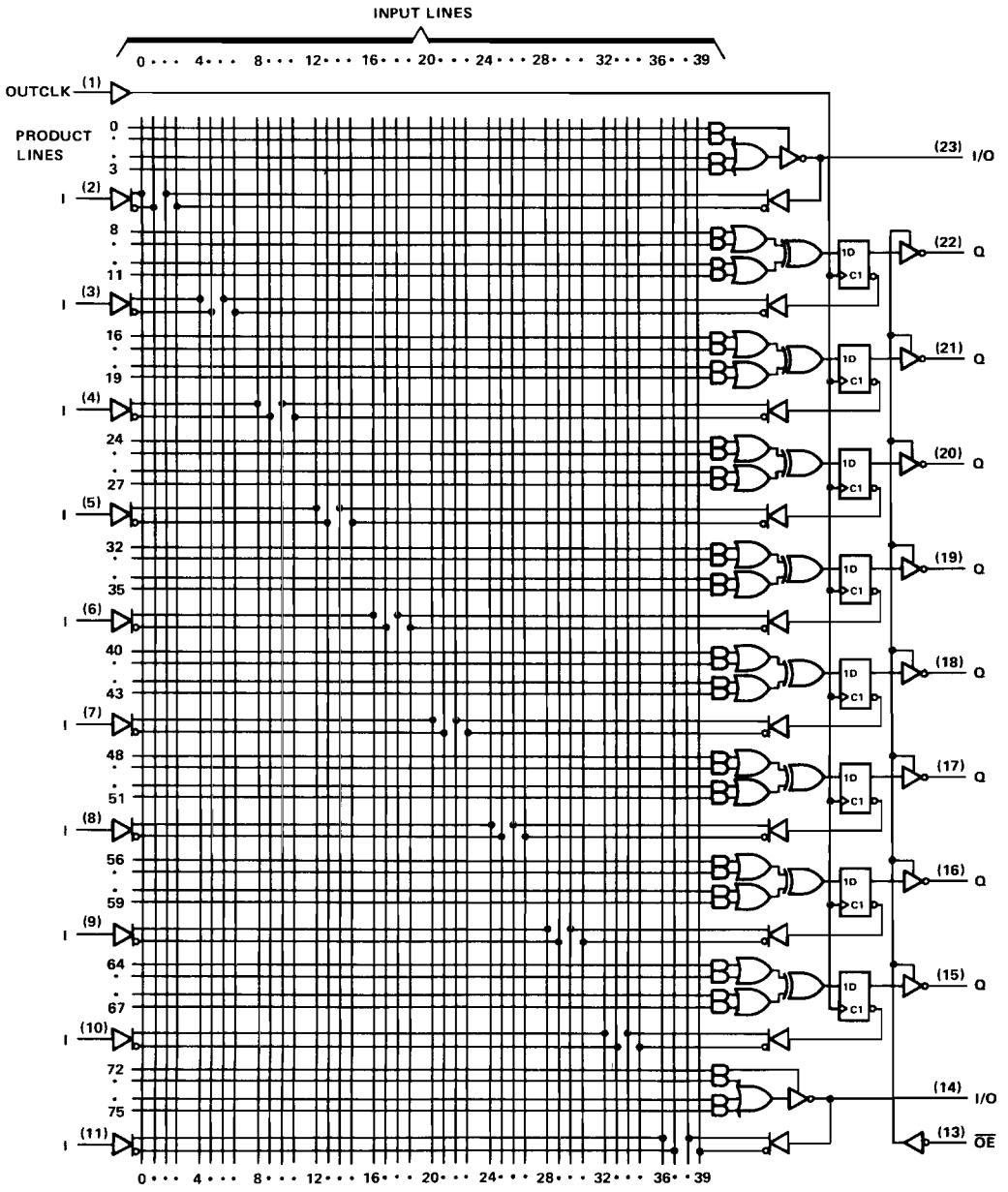
~ denotes fused inputs

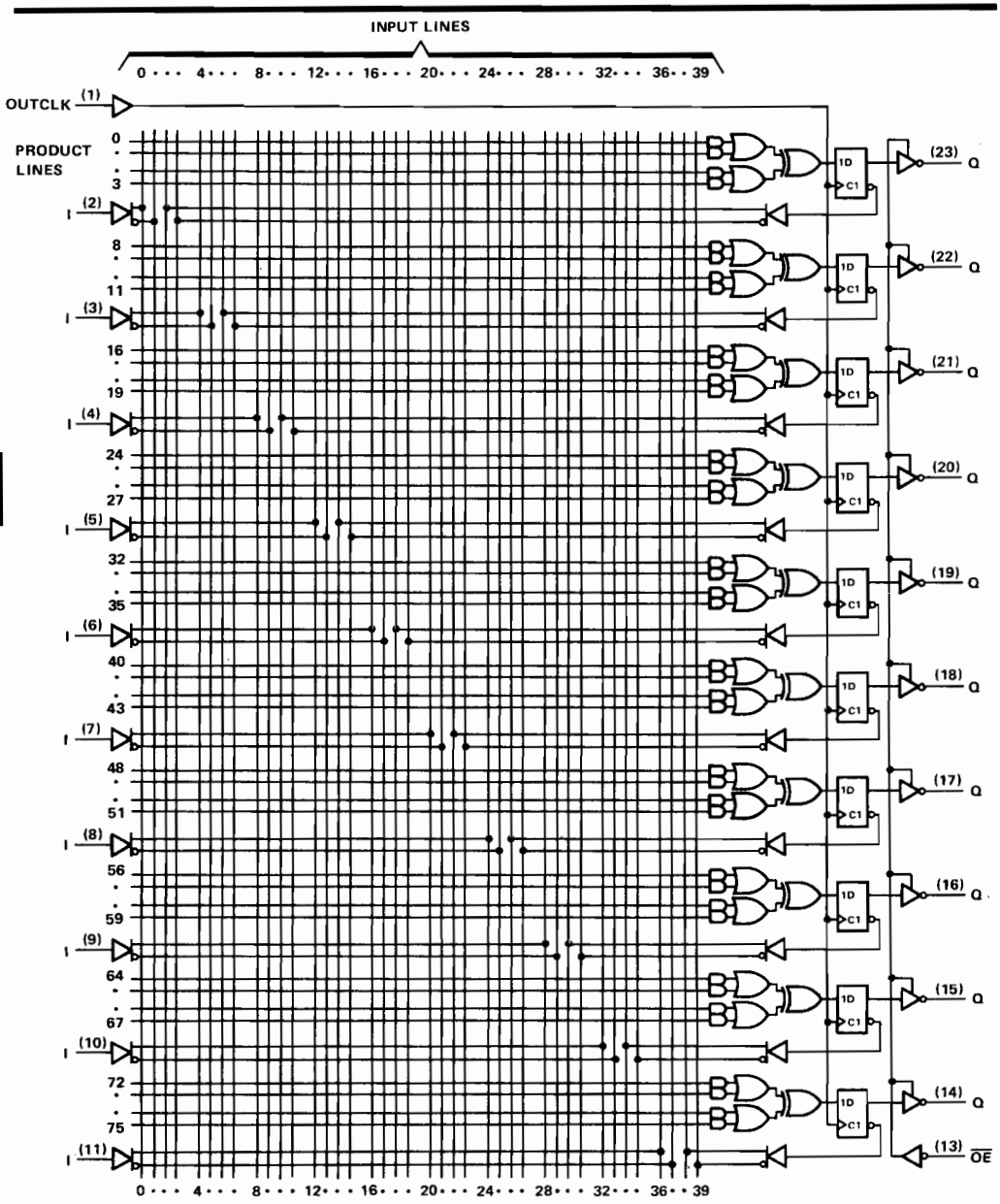
TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265


INPUT LINES
0 • • • 4 • • • 8 • • • 12 • • • 16 • • • 20 • • • 24 • • • 28 • • • 32 • • • 36 • • 39
PRODUCT LINES
(1)
(2)
(3)
(4)
(5)
(6)
(7)
(8)
(9)
(10)
(11)
(23) O
(22) I/O
(21) I/O
(20) I/O
(19) I/O
(18) I/O
(17) I/O
(16) I/O
(15) I/O
(14) O
(13) I



TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265


INPUT LINES
0 • • • 4 • • • 8 • • • 12 • • • 16 • • • 20 • • • 24 • • • 28 • • • 32 • • • 36 • • 39
OUTCLK
(1)
PRODUCT LINES
0
3
(2)
8
11
(3)
16
19
(4)
24
27
(5)
32
35
(6)
40
43
(7)
48
51
(8)
56
59
(9)
64
67
(10)
72
75
(11)
(23) I/O
(22) Q
(21) Q
(20) Q
(19) Q
(18) Q
(17) Q
(16) Q
(15) Q
(14) I/O
(13) OE
1D
C1



TEXAS INSTRUMENTS
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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Voltage applied to a disabled output (see Note 1) . . . . . 5.5 V
Operating free-air temperature range: M suffix . . . . . −55°C to 125°C
C suffix . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle.

recommended operating conditions

PARAMETER		M SUFFIX			C SUFFIX			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2		5.5	2		5.5	V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−2			−3.2	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

programming parameters, T_A = 25°C

			MIN	NOM	MAX	UNIT
V_{CC}	Verify-level supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2		5.5	V
V_{IL}	Low-level input voltage				0.8	V
V_{IHH}	Program-pulse input voltage					V
I_{IHH}	Program-pulse input current	PGM ENABLE				mA
		PO				
		V_{CC}				
t_{w1}	Pulse duration at V_{CC}					µs
t_{w2}	Pulse duration at PGM VERIFY					ns
t_{su}	Setup time $\overline{OE}$↑ before PO↑ (V_{IHH})					ns
	Setup time PO↑ (V_{IHH}) before V_{CC}↑ (V_{IHH})					
t_h	Hold time PO (V_{IHH}) after V_{CC}↓					ns
	Hold time $\overline{OE}$ high after PO↓					
t_{d1}	Delay time from $\overline{OE}$ low tc PGM VERIFY↑					µs
t_{d2}	Delay time from PGM VERIFY↑ to valid output					ns
	Input voltage at pins 1 and 13 to open verify-protect (security) fuse					V
	Input current to open verify-protect (security) fuse					mA
	Pulse duration to open verify-protect (security) fuse					ms

recommended operating conditions

			M SUFFIX-XX			C SUFFIX-XX			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
f_{clock}	Clock frequency		0		40	0		40	MHz
t_w	Pulse duration, clock	High							ns
		Low							ns
t_{su}	Setup time, input or feedback before OUTCLK↑		15			15			ns
t_h	Hold time, input or feedback after OUTCLK↑		0			0			ns

electrical characteristics over recommended free-air operating temperature range

PARAMETER		TEST CONDITIONS†	M SUFFIX-XX			C SUFFIX-XX			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = MIN, I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = MIN, I_{OH} = MAX	2.4	3.2		2.4	3.3		V
V_{OL}		V_{CC} = MIN, I_{OL} = MAX		0.25	0.4		0.35	0.5	V
I_{OZH}	Outputs	V_{CC} = MAX, V_{IH} = 2.7 V			20			20	μA
	I/O ports				100			100	
I_{OZL}	Outputs	V_{CC} = MAX, V_{IH} = 0.4 V			−20			−20	μA
	I/O ports				−250			−250	
I_I		V_{CC} = MAX, V_I = 5.5 V			0.1			0.1	mA
I_{IH}		V_{CC} = MAX, V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = MAX, V_I = 0.4 V			−0.2			−0.2	mA
I_O§		V_{CC} = MAX, V_O = 2.25 V	−30		−125	−30		−125	mA
I_{CC}		V_{CC} = MAX, V_I = 0 V,		140	180		140	180	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half the true short-circuit current, I_{OS}.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	TEST CONDITIONS	M SUFFIX-XX			C SUFFIX-XX			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
f_{max}				40			40			MHz
t_{pd}	I, I/O	O, I/O			15			15		ns
t_{pd}	OUTCLK↑	Q	R_L = 500 Ω,		10			10		ns
t_{en}	$\overline{OE}$	Q	C_L = 50 pF		10			10		ns
t_{dis}	$\overline{OE}$↑	Q	See Note 2		10			10		ns
t_{en}	I, I/O	O, I/O			15			15		ns
t_{dis}	I, I/O	O, I/O			15			15		ns

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

recommended operating conditions

			M-SUFFIX-XX			C SUFFIX-XX			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
f_{clock}	Clock frequency		0		25	0		25	MHz
t_w	Pulse duration, clock	High							ns
		Low							ns
t_{su}	Setup time, input or feedback before OUTCLK↑		15			15			ns
t_h	Hold time, input or feedback after OUTCLK↑		0			0			ns

electrical characteristics over recommended free-air operating temperature range

PARAMETER		TEST CONDITIONS†	M SUFFIX-XX			C SUFFIX-XX			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = MIN, I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = MIN, I_{OH} = MAX	2.4	3.2		2.4	3.3		V
V_{OL}		V_{CC} = MIN, I_{OL} = MAX		0.25	0.4		0.35	0.5	V
I_{OZH}	Outputs	V_{CC} = MAX, V_{IH} = 2.7 V			20			20	μA
	I/O ports				100			100	
I_{OZL}	Outputs	V_{CC} = MAX, V_{IH} = 0.4 V			−20			−20	μA
	I/O ports				−250			−250	
I_I		V_{CC} = MAX, V_I = 5.5 V			0.1			0.1	mA
I_{IH}		V_{CC} = MAX, V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = MAX, V_I = 0.4 V			−0.1			−0.1	mA
I_O§		V_{CC} = MAX, V_O = 2.25 V	−30		−125	−30		−125	mA
I_{CC}		V_{CC} = MAX, V_I = 0 V,		70	95		70	90	mA

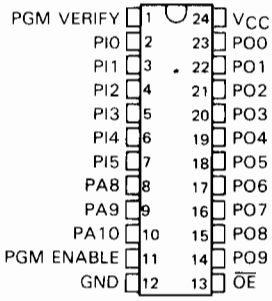
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half the true short-circuit current, I_{OS}.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	TEST CONDITIONS	M SUFFIX-XX			C SUFFIX-XX			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
f_{max}				25			25			MHz
t_{pd}	I, I/O	O, I/O			30			30		ns
t_{pd}	OUTCLK↑	Q	R_L = 500 Ω,		20			20		ns
t_{en}	$\overline{OE}$	Q	C_L = 50 pF		15			15		ns
t_{dis}	$\overline{OE}$↑	Q	See Note 2		15			15		ns
t_{en}	I, I/O	O, I/O			30			30		ns
t_{dis}	I, I/O	O, I/O			30			30		ns

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

PRODUCT TERMS
(TOP VIEW)



Pin assignments in programmming mode (PGM ENABLE, pin 11 at V_{IHH})

TABLE 2. PRODUCT LINE SELECT

PRODUCT LINE ADDRESS			PRODUCT LINE NUMBER									
PA8	PA9	PA10										
L	L	L	0	8	16	24	32	40	48	56	64	72
L	L	H	1	9	17	25	33	41	49	57	65	73
L	H	L	2	10	18	26	34	42	50	58	66	74
L	H	H	3	11	19	27	35	43	51	59	67	75
			PO0	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9
			OUTPUT PIN NAME									

L = V_{IL}, H = V_{IH}

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

TABLE 1. INPUT LINE SELECT

INPUT LINE NUMBER	PIN NAME					
	PI0	PI1	PI2	PI3	PI4	PI5
0	L	L	L	L	L	L
1	L	L	L	L	L	H
2	L	L	L	L	H	L
3	L	L	L	L	H	H
4	L	L	L	H	L	L
5	L	L	L	H	L	H
6	L	L	L	H	H	L
7	L	L	L	H	H	H
8	L	L	H	L	L	L
9	L	L	H	L	L	H
10	L	L	H	L	H	L
11	L	L	H	L	H	H
12	L	L	H	H	L	L
13	L	L	H	H	L	H
14	L	L	H	H	H	L
15	L	L	H	H	H	H
16	L	H	L	L	L	L
17	L	H	L	L	L	H
18	L	H	L	L	H	L
19	L	H	L	L	H	H
20	L	H	L	H	L	L
21	L	H	L	H	L	H
22	L	H	L	H	H	L
23	L	H	L	H	H	H
24	L	H	H	L	L	L
25	L	H	H	L	L	H
26	L	H	H	L	H	L
27	L	H	H	L	H	H
28	L	H	H	H	L	L
29	L	H	H	H	L	H
30	L	H	H	H	H	L
31	L	H	H	H	H	H
32	H	L	L	L	L	L
33	H	L	L	L	L	H
34	H	L	L	L	H	L
35	H	L	L	L	H	H
36	H	L	L	H	L	L
37	H	L	L	H	L	H
38	H	L	L	H	H	L
39	H	L	L	H	H	H

L = V_{IL}, H = V_{IH}

programming procedure for array fuses

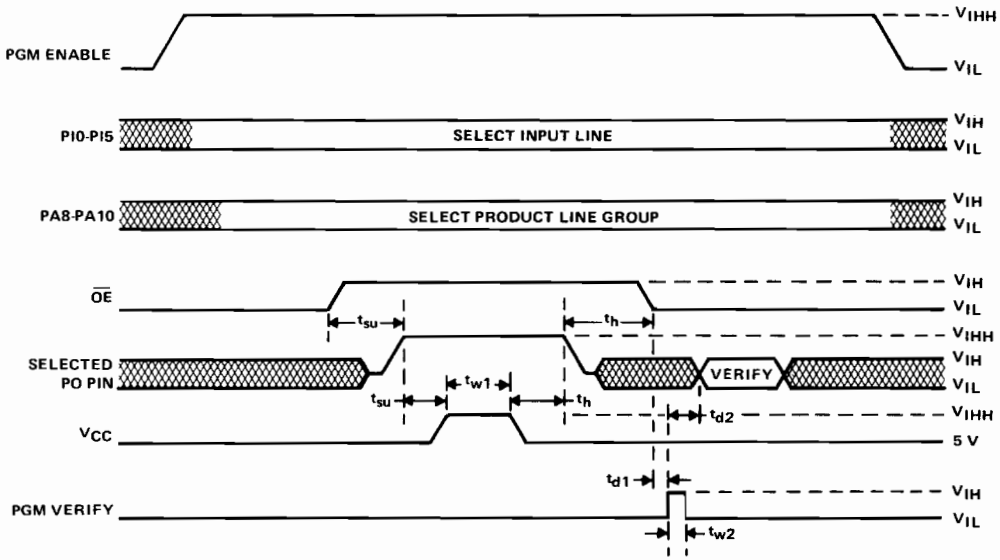
Array fuses are programmed by excuting the following programming sequence. Each fuse can be opened by selecting the appropriate (one of 40) input line and (one of 80) product line. The levels for selecting input lines and product lines are shown in Tables 1 and 2.

Step 1 Raise PGM ENABLE to V_{IHH}.
Step 2 Select an input line by applying appropriate logic levels to PI pins.
Step 3 Select a product line group by applying appropriate logic levels to PA pins. The actual product line selected will be determined by the PO pin (described in Step 5).
Step 4 Raise $\overline{OE}$ to V_{IH}.
Step 5 Raise the selected PO pin to V_{IHH}.
Step 6 Program the fuse by pulsing V_{CC} to V_{IHH}.
Step 7 Remove the output voltage
Step 8 Lower $\overline{OE}$ to V_{IL} to enable device
Step 9 Verify the blowing of the fuse by checking for a V_{OL}, at the selected PO pin. Register devices require a position pulse on the PGM verify pin.

Steps 1 through 9 may be repeated if the verification does not indicate that the fuse was successfully programmed (blown), but no more than four times. Verification is possible only with the verify-protect fuse intact.

3 Field-Programmable Logic

programming waveforms



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PRELOAD PROCEDURES

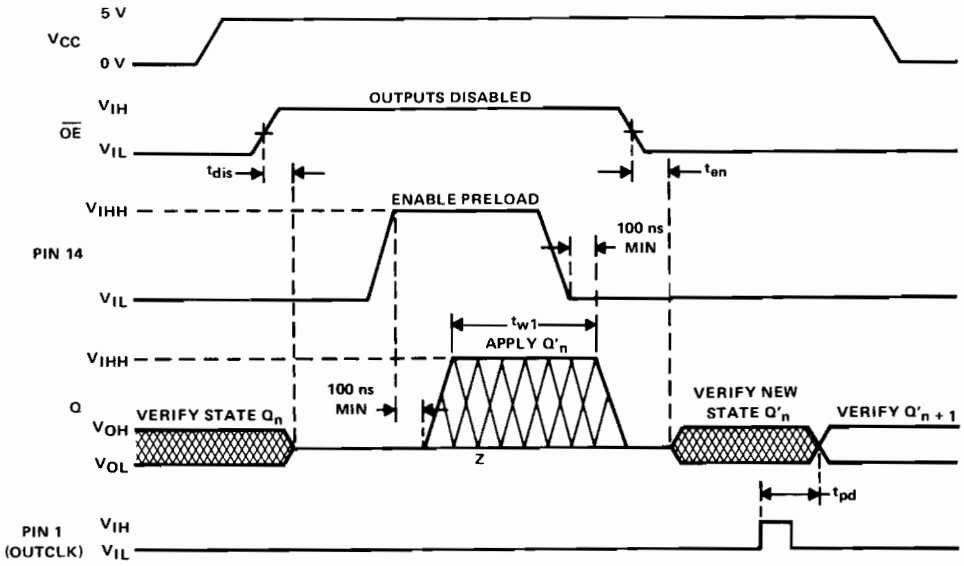
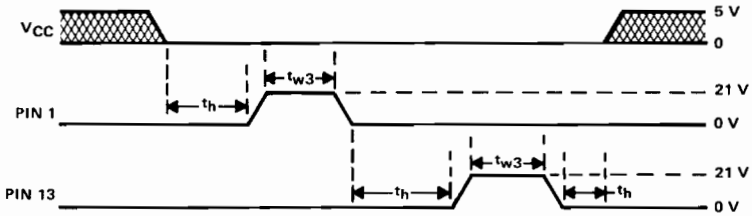


FIGURE 1. PRELOAD WAVEFORMS

preload procedure for registered outputs

Step 1	Pin 13 to V_{IH}, Pin 1 to V_{IL}, and V_{CC} to 5 volts.
Step 2	Pin 14 to V_{IHH} for 10 to 50 microseconds.
Step 3	Apply an open circuit for a low and V_{IHH} for a high at the Q outputs.
Step 4	Pin 14 to V_{IL}.
Step 5	Remove the voltages applied to the outputs.
Step 6	Pin 13 to V_{IL}.
Step 7	Check the output states to verify preload.

security fuse programming



D2709, DECEMBER 1982—REVISED AUGUST 1984

- **Choice of Operating Speeds**
  HIGH PERFORMANCE . . . 30 MHz Max
  HALF-POWER . . . 20 MHz Max
- **Preload Capability on Output Registers**
- **Power-up Clear on Registered Devices**
- **DIP Options Include Both 300-mil Plastic and 600-mil Ceramic**

DEVICE	I/D INPUTS	I INPUTS	3-STATE O OUTPUTS	REGISTERED Q OUTPUTS	I/O PORTS
'PALR19L8	11	2	2	0	6
'PALR19R4	11	0	0	4 (3-state buffers)	4
'PALR19R6	11	0	0	6 (3-state buffers)	2
'PALR19R8	11	0	0	8 (3-state buffers)	0

description

These programmable array logic devices feature high speed and functionality similar to the TIBPAL16L8, 16R4, 16R6, 16R8 series, but with the added advantage of D-type input registers. If any input register is not desired, it can be converted to an input buffer by simply programming the architectural fuse.

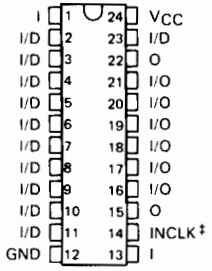
Combining Advanced Low-Power Schottky† technology, with proven titanium-tungsten fuses, these devices will provide reliable high performance substitutes over conventional TTL logic. Their easy programmability allows for quick design of custom functions and typically result in a more compact circuit board. In addition, chip carriers are available for further reduction in board space. The Half-power devices offer a choice of operating frequency, switching speed, and power dissipation.

All of the registered outputs are set to a low level during power-up. In addition, extra circuitry has been provided to allow loading of each register asynchronously to either a high or low state. this feature simplifies testing because the registers can be set to an initial state prior to executing the test sequence.

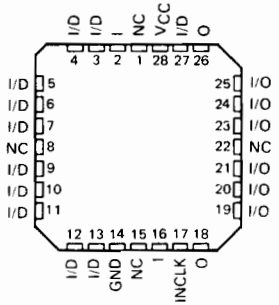
INPUT REGISTER FUNCTION TABLE

INPUT		OUTPUT OF
INCLK	D	INPUT REGISTER
↑	H	H
↑	L	L
L	X	Q_0

TIBPALR19L8'
M SUFFIX . . . JW PACKAGE
C SUFFIX . . . JW OR NT PACKAGE
(TOP VIEW)



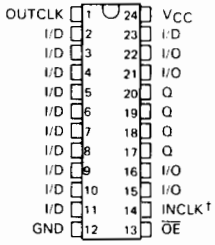
TIBPALR19L8'
M SUFFIX . . . FH OR FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



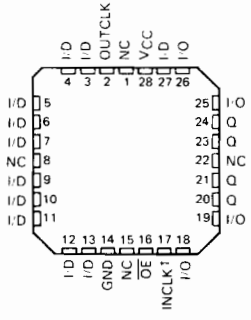
‡Pin 14 is also used for the preload
Pin assignments in operating mode (voltage at pins 1 and 13 less than V_{IHH})

†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments, U.S. Patent Number 3,463,975.
PAL is a registered trademark of Monolithic Memories Inc.

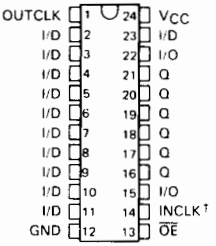
TIBPALR19R4'
M SUFFIX . . . JW PACKAGE
C SUFFIX . . . JW OR NT PACKAGE
(TOP VIEW)



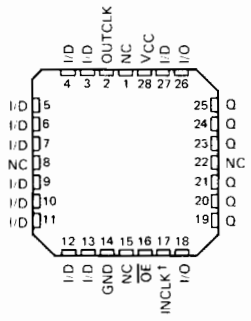
TIBPALR19R4'
M SUFFIX . . . FH OR FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



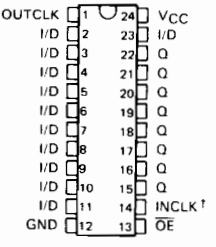
TIBPALR19R6'
M SUFFIX . . . JW PACKAGE
C SUFFIX . . . JW OR NT PACKAGE
(TOP VIEW)



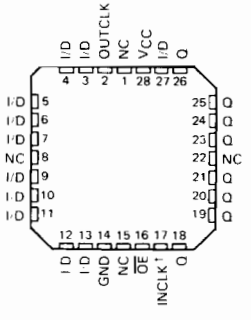
TIBPALR19R6'
M SUFFIX . . . FH OR FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



TIBPALR19R8'
M SUFFIX . . . JW PACKAGE
C SUFFIX . . . JW OR NT PACKAGE
(TOP VIEW)



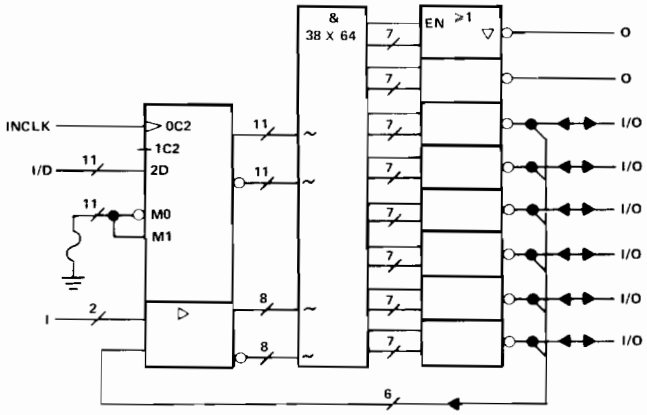
TIBPALR19R8'
M SUFFIX . . . FH OR FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



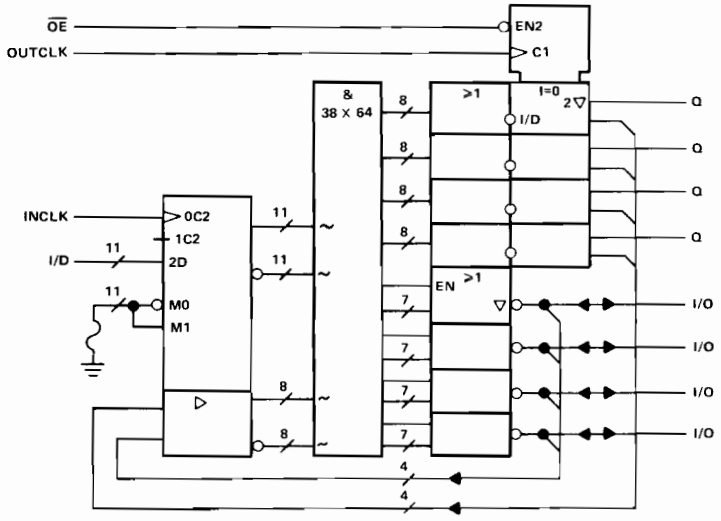
NC—No internal connection
†PIN 14 is also used for preload

functional block diagrams (positive logic)

'PALR19L8

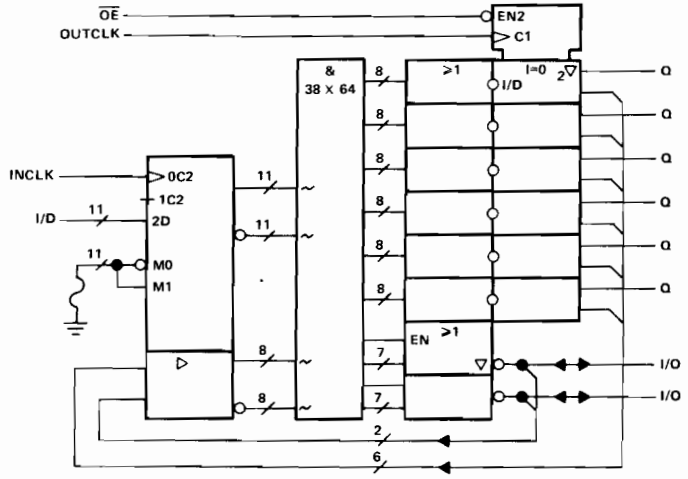


'PALR19R4

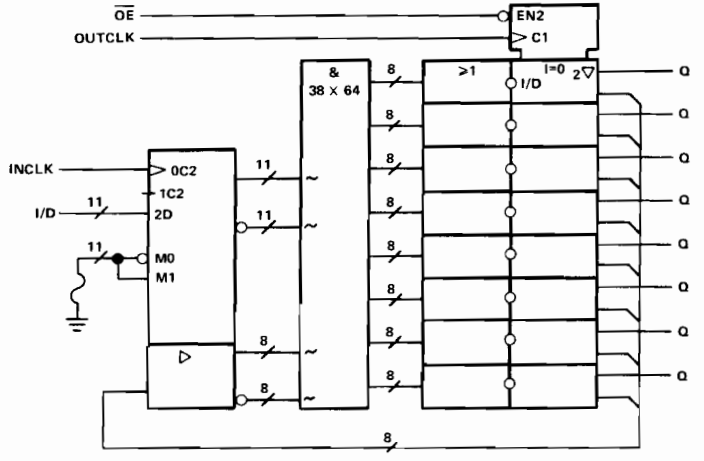


functional block diagrams (positive logic)

'PALR19R6



'PALR19R8



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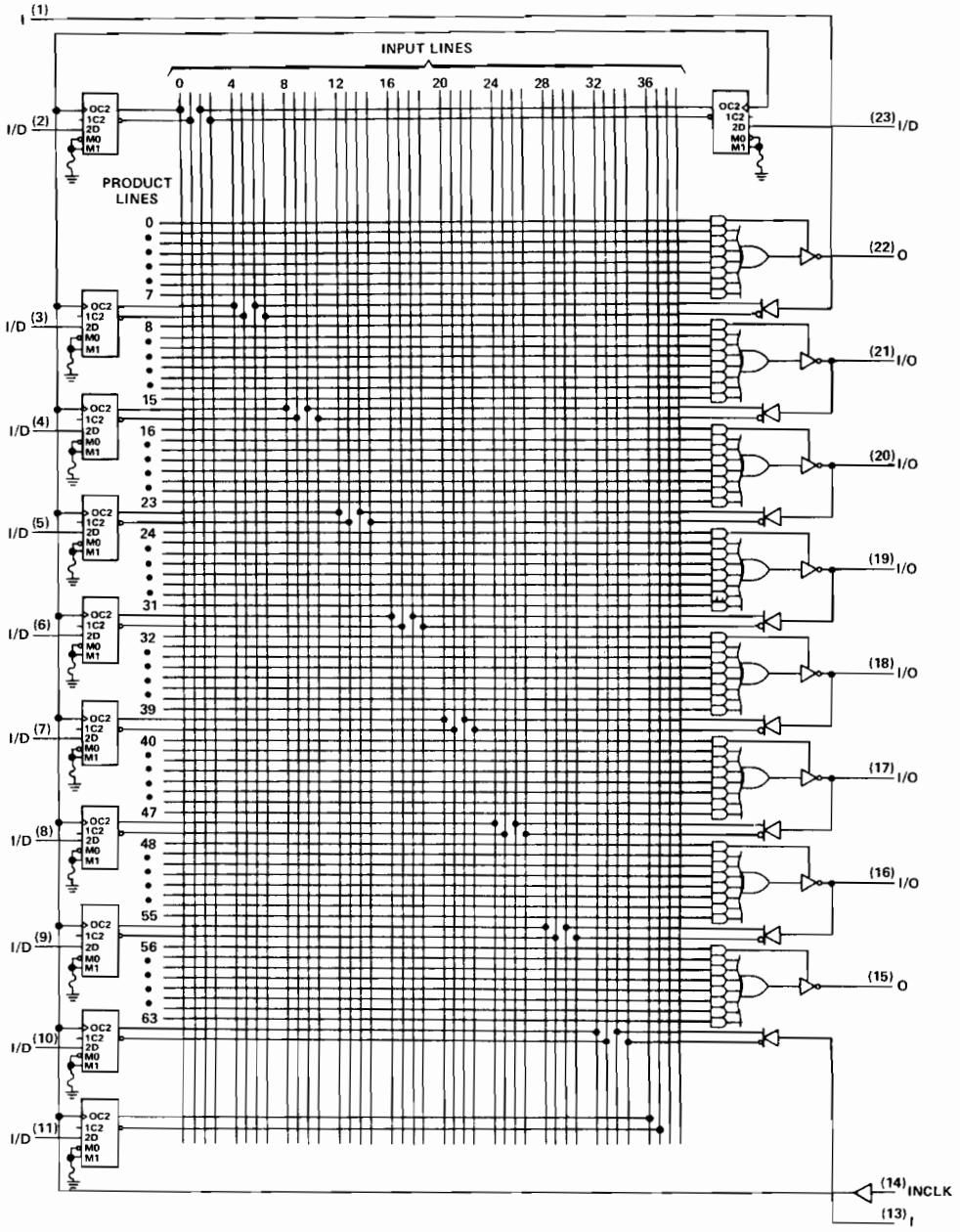
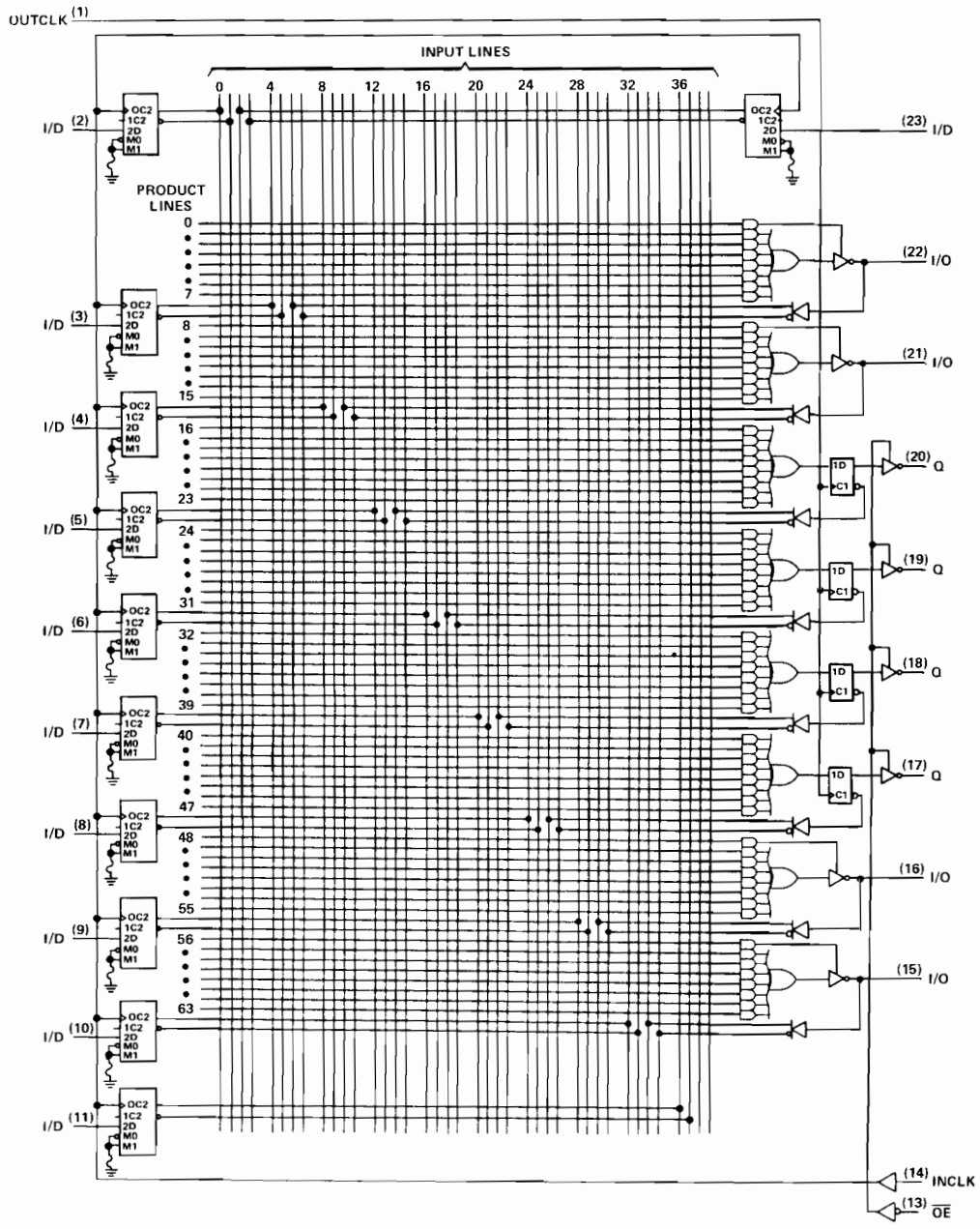

I (1)
INPUT LINES
0 4 8 12 16 20 24 28 32 36
I/D (2)
I/D (3)
I/D (4)
I/D (5)
I/D (6)
I/D (7)
I/D (8)
I/D (9)
I/D (10)
I/D (11)
OC2
1C2
2D
M0
M1
PRODUCT LINES
0
7
8
15
16
23
24
31
32
39
40
47
48
55
56
63
(23) I/D
(22) O
(21) I/O
(20) I/O
(19) I/O
(18) I/O
(17) I/O
(16) I/O
(15) O
(14) INCLK
(13) I

884



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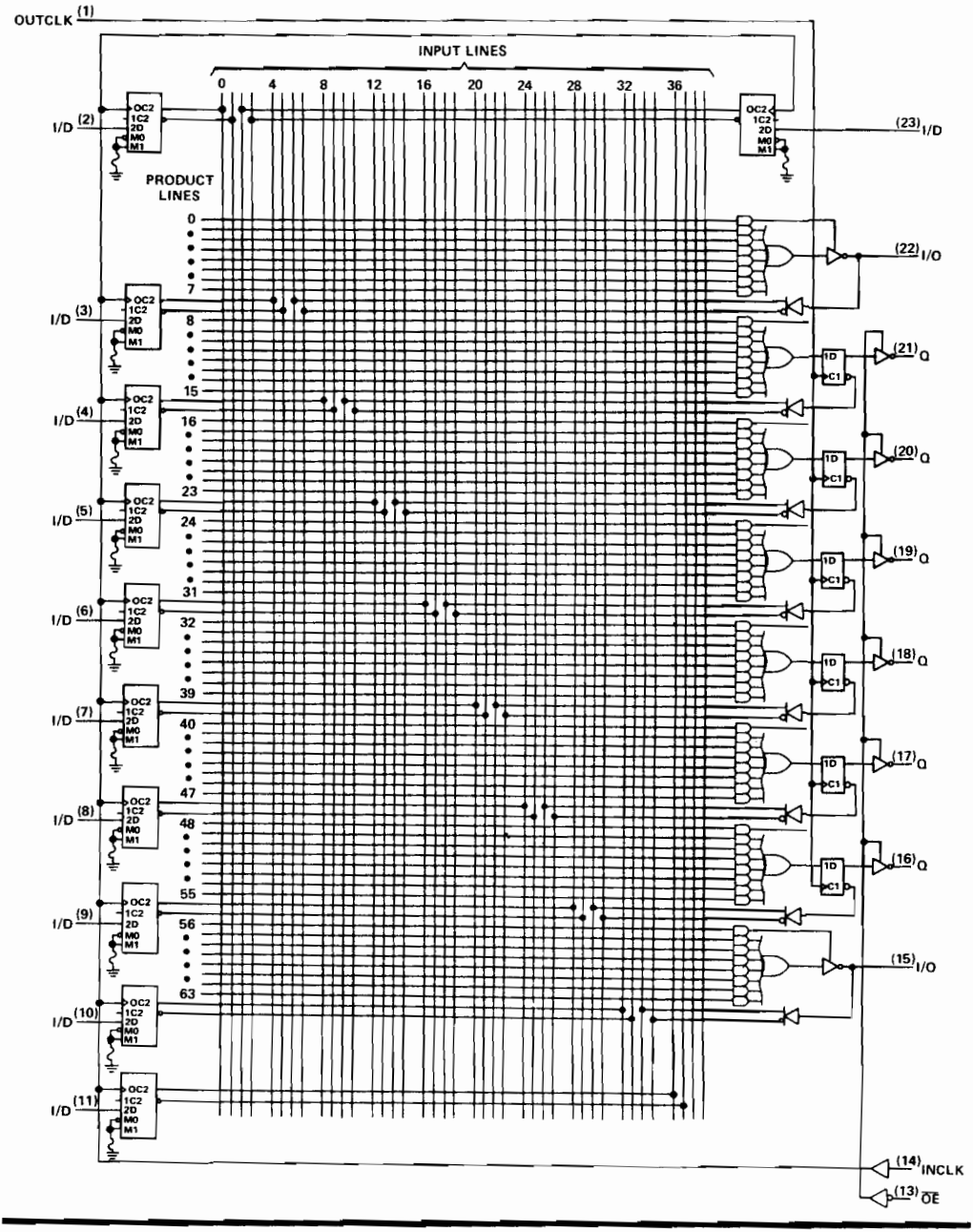
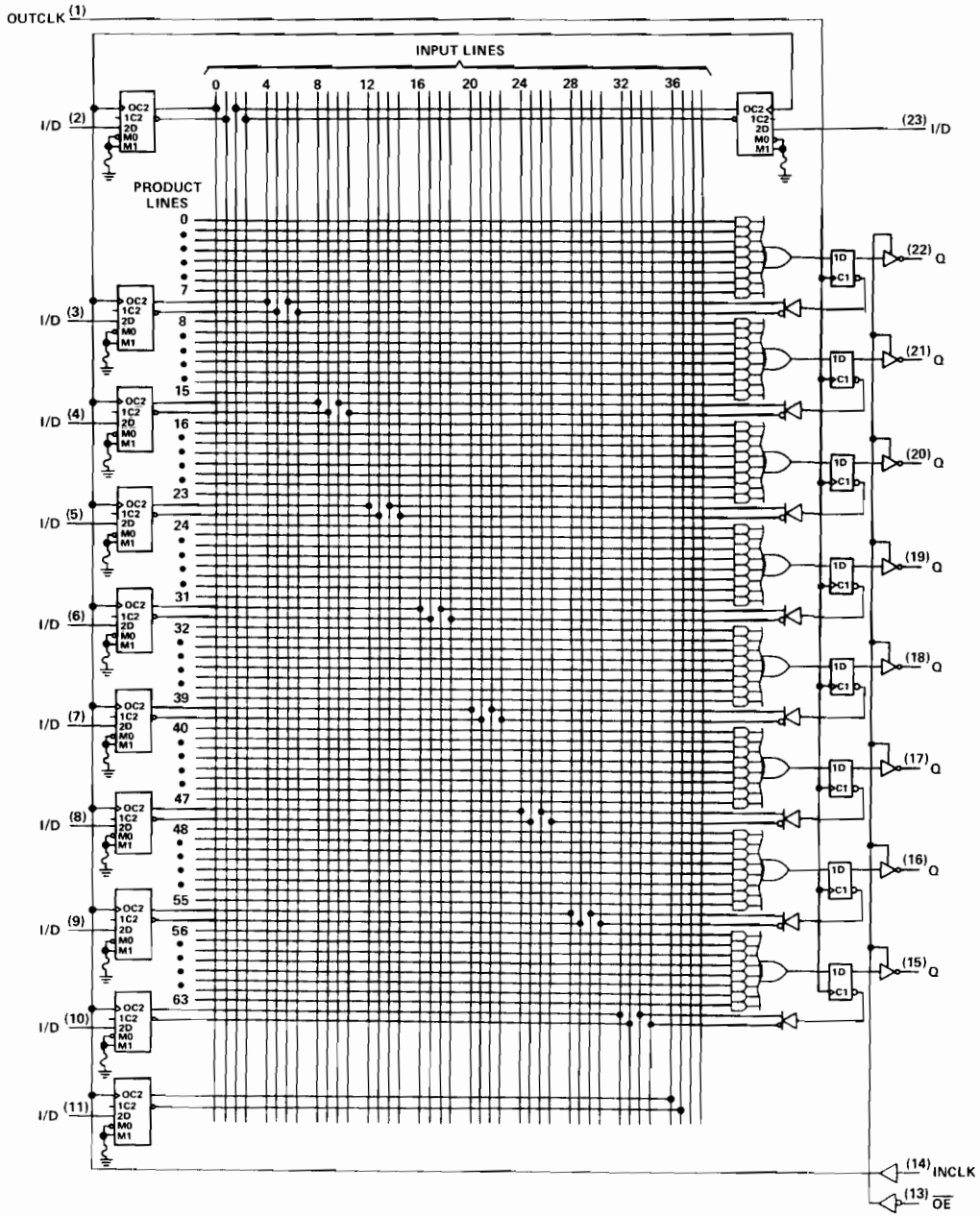

OUTCLK (1)
INPUT LINES
0 4 8 12 16 20 24 28 32 36
PRODUCT LINES
I/D (2)
I/D (3)
I/D (4)
I/D (5)
I/D (6)
I/D (7)
I/D (8)
I/D (9)
I/D (10)
I/D (11)
OC2 1C2 2D M0 M1
0 7 8 15 16 23 24 31 32 39 40 47 48 55 56 63
(23) I/D
(22) I/O
(21) Q
(20) Q
(19) Q
(18) Q
(17) Q
(16) Q
(15) I/O
1D C1
(14) INCLK
(13) OE

884



884

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Voltage applied to a disabled output (see Note 1) . . . . . 5.5 V
Operating free-air temperature range: M suffix . . . . . −55°C to 125°C
C suffix . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle or during preload cycle.

recommended operating conditions (see Note 2)

		M SUFFIX			C SUFFIX			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2		5.5	2		5.5	V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−2			−3.2	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

NOTE 2: These recommended operating conditions apply for all device dash numbers. Also refer to additional recommended operating conditions information pertaining to appropriate device dash numbers.

programming parameters, T_A = 25°C

			MIN	NOM	MAX	UNIT
V_{CC}	Verify-level supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2		5.5	V
V_{IL}	Low-level input voltage				0.8	V
V_{OH}	High-level output voltage				5.5	V
V_{IHH}	Program-pulse input voltage		10.25	10.5	10.75	V
I_{IHH}	Program-pulse input current	PO			50	mA
		PGM ENABLE, L/R			25	
		PI, PA			5	
		V_{CC}			400	
t_{w1}	Program-pulse duration at PO or I/D pins		10		50	μs
t_{w2}	Pulse duration at PGM VERIFY and INCLK		100			ns
t_{su}	Setup time		100			ns
t_h	Hold time		100			ns
t_{d1}	Delay time from V_{CC} to 5 V to PGM VERIFY↑		100			μs
t_{d2}	Delay time from PGM VERIFY↑ to verification of output		200			ns
t_{d3}	Delay time		100			ns
	Input voltage at pins 1 and 13 to open verify-protect (security) fuse		20	21	22	V
t_{w3}	Input current to open verify-protect (security) fuse				400	mA
	Pulse duration to open verify-protect (security) fuse		20		50	μs
	V_{CC} value during security fuse programming			0	0.4	V

3 Field-Programmable Logic

884

recommended operating conditions

			M SUFFIX-XX			C SUFFIX-XX			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
f_{clock}	Clock frequency	INCLK							MHz
		OUTCLK							
t_w	Pulse duration, clock	INCLK high							ns
		INCLK low							
		OUTCLK high							ns
		OUTCLK low							
t_{su}	Setup time, input or feedback before	INCLK↑							ns
		OUTCLK↑							
t_h	Hold time, input or feedback after INCLK↑ or OUTCLK↑		0			0			ns

electrical characteristics over recommended free-air operating temperature range

PARAMETER		TEST CONDITIONS†		M SUFFIX-XX			C SUFFIX-XX			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = MIN,	I_{OH} = MAX	2.4	3.2		2.4	3.3		V
V_{OL}		V_{CC} = MIN,	I_{OL} = MAX		0.25	0.4		0.35	0.5	V
I_{OZH}	Outputs	V_{CC} = MAX,	V_{IH} = 2.7 V			20			20	μA
	I/O ports					100			100	
I_{OZL}	Outputs	V_{CC} = MAX,	V_{IH} = 0.4 V			−20			−20	μA
	I/O ports					−250			−250	
I_I	$\overline{OE}$ Input	V_{CC} = MAX,	V_I = 5.5 V			0.2			0.2	mA
	I/D Inputs					0.1			0.1	
	All others					0.1			0.1	
I_{IH}	$\overline{OE}$ Input	V_{CC} = MAX,	V_I = 2.7 V			40			40	μA
	I/D Inputs					20			0.1	
	All others					20			0.1	
I_{IL}	$\overline{OE}$ Input	V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4	mA
	I/D Inputs					−0.6			−0.6	
	All others					−0.2			−0.2	
I_O§		V_{CC} = MAX,	V_O = 2.25 V	−30		−125	−30		−125	mA
I_{CC}		V_{CC} = MAX, Outputs open	V_I = 0 V,		150	210		150	210	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half the true short-circuit current, I_{OS}.

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	INPUT MODE	TEST CONDITIONS	M SUFFIX-XX			C SUFFIX-XX			UNIT
					MIN	TYP†	MAX	MIN	TYP†	MAX	
f_{max}			Either	R_L = 500 Ω, C_L = 50 pF, See Note 3	30			30			MHz
t_{pd}	I, I/O	I/O, O	Either			16			16		ns
t_{pd}	OUTCLK↑	Q	Either			12			12		ns
t_{en}	$\overline{OE}$↑	Q	Either			8			8		ns
t_{dis}	$\overline{OE}$↑	Q	Either			6			6		ns
t_{pd}	INCLK↑	I/O, O	Registered			23			23		ns
t_{en}	INCLK↑	I/O, O, Q	Registered			25			25		ns
t_{dis}	INCLK↑	I/O, O, Q	Registered			20			20		ns
t_{pd}	I/D	I/O, O	Buffered			20			20		ns
t_{en}	I/D, I/O	I/O	Buffered			22			22		ns
t_{dis}	I/D, I/O	I/O	Buffered			17			17		ns

†All typical values are V_{CC} = 5 V, T_A = 25°C.

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

recommended operating conditions

			M SUFFIX-XX			C SUFFIX-XX			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
f_{clock}	Clock frequency	INCLK							MHz
		OUTCLK							
t_w	Pulse duration clock	INCLK high							ns
		INCLK low							
		OUTCLK high							ns
		OUTCLK low							
t_{su}	Setup time, input or feedback before	INCLK↑							ns
		OUTCLK↑							
t_h	Hold time, input or feedback after INCLK↑ or OUTCLK↑		0			0			ns

electrical characteristics over recommended free-air operating temperature range

PARAMETER		TEST CONDITIONS†		M SUFFIX-XX			C SUFFIX-XX			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = MIN,	I_{OH} = MAX	2.4	3.2		2.4	3.3		V
V_{OL}		V_{CC} = MIN,	I_{OL} = MAX		0.25	0.4		0.35	0.5	V
I_{OZH}	Outputs	V_{CC} = MAX,	V_{IH} = 2.7 V			20			20	μA
	I/O ports					100			100	
I_{OZL}	Outputs	V_{CC} = MAX,	V_{IH} = 0.4 V			−20			−20	μA
	I/O ports					−250			−250	
I_I	$\overline{OE}$ Input	V_{CC} = MAX,	V_I = 5.5 V			0.2			0.2	mA
	I/D Inputs					0.1			0.1	
	All others					0.1			0.1	
I_{IH}	$\overline{OE}$ Input	V_{CC} = MAX,	V_I = 2.7 V			40			40	μA
	I/D Inputs					20			0.1	
	All others					20			0.1	
I_{IL}	$\overline{OE}$ Input	V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4	mA
	I/D Inputs					−0.6			−0.6	
	All others					−0.2			−0.2	
I_O§		V_{CC} = MAX,	V_O = 2.25 V	−30		−125	−30		−125	mA
I_{CC}		V_{CC} = MAX, Outputs open	V_I = 0 V,		75	105		75	105	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half the true short-circuit current, I_{OS}.

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

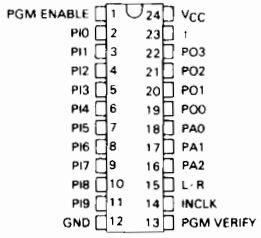
switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	INPUT MODE	TEST CONDITIONS	M SUFFIX-XX			C SUFFIX-XX			UNIT
					MIN	TYP†	MAX	MIN	TYP†	MAX	
f_{max}			Either		18			18			MHz
t_{pd}	I, I/O	I/O, O	Either			25			25		ns
t_{pd}	OUTCLK↑	Q	Either			20			20		ns
t_{en}	$\overline{OE}$↑	Q	Either			15			15		ns
t_{dis}	$\overline{OE}$↑	Q	Either			12			12		ns
t_{pd}	INCLK↑	I/O, O	Registered	R_L = 500 Ω,		32			32		ns
t_{en}	INCLK↑	I/O, O, Q	Registered	C_L = 50 pF,		35			35		ns
t_{dis}	INCLK↑	I/O, O, Q	Registered	See Note 3		30			30		ns
t_{pd}	I/D	I/O, O	Buffered			30			30		ns
t_{en}	I/D, I/O	I/O	Buffered			32			32		ns
t_{dis}	I/D, I/O	I/O	Buffered			26			26		ns

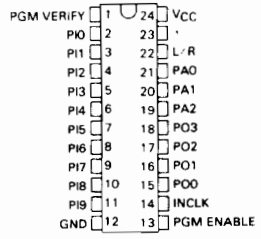
†All typical values are V_{CC} = 5 V, T_A = 25°C.
NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

PRODUCT TERMS 0 THRU 31
(TOP VIEW)



PRODUCT TERMS 32 THRU 63
(TOP VIEW)



†No programming function. Make no connections.
Pin assignments in programming mode (PGM ENABLE, pin 1 or 13, at V_{IHH})

TABLE 1. INPUT LINE SELECT

INPUT LINE NUMBER	PIN NAME										
	PI9	PI8	PI7	PI6	PI5	PI4	PI3	PI2	PI1	PI0	L/R
0	HH	HH	HH	HH	HH	HH	HH	HH	HH	L	Z
1	HH	HH	HH	HH	HH	HH	HH	HH	HH	H	Z
2	HH	HH	HH	HH	HH	HH	HH	HH	HH	L	HH
3	HH	HH	HH	HH	HH	HH	HH	HH	HH	H	HH
4	HH	HH	HH	HH	HH	HH	HH	HH	L	HH	Z
5	HH	HH	HH	HH	HH	HH	HH	HH	H	HH	Z
6	HH	HH	HH	HH	HH	HH	HH	HH	L	HH	HH
7	HH	HH	HH	HH	HH	HH	HH	HH	H	HH	HH
8	HH	HH	HH	HH	HH	HH	HH	L	HH	HH	Z
9	HH	HH	HH	HH	HH	HH	HH	H	HH	HH	Z
10	HH	HH	HH	HH	HH	HH	HH	L	HH	HH	HH
11	HH	HH	HH	HH	HH	HH	HH	H	HH	HH	HH
12	HH	HH	HH	HH	HH	HH	L	HH	HH	HH	Z
13	HH	HH	HH	HH	HH	HH	H	HH	HH	HH	Z
14	HH	HH	HH	HH	HH	HH	L	HH	HH	HH	HH
15	HH	HH	HH	HH	HH	HH	H	HH	HH	HH	HH
16	HH	HH	HH	HH	HH	L	HH	HH	HH	HH	Z
17	HH	HH	HH	HH	HH	H	HH	HH	HH	HH	Z
18	HH	HH	HH	HH	HH	L	HH	HH	HH	HH	HH
19	HH	HH	HH	HH	HH	H	HH	HH	HH	HH	HH
20	HH	HH	HH	HH	L	HH	HH	HH	HH	HH	Z
21	HH	HH	HH	HH	H	HH	HH	HH	HH	HH	Z
22	HH	HH	HH	HH	L	HH	HH	HH	HH	HH	HH
23	HH	HH	HH	HH	H	HH	HH	HH	HH	HH	HH
24	HH	HH	HH	L	HH	HH	HH	HH	HH	HH	Z
25	HH	HH	HH	H	HH	HH	HH	HH	HH	HH	Z
26	HH	HH	HH	L	HH	HH	HH	HH	HH	HH	HH
27	HH	HH	HH	H	HH	HH	HH	HH	HH	HH	HH
28	HH	HH	L	HH	HH	HH	HH	HH	HH	HH	Z
29	HH	HH	H	HH	HH	HH	HH	HH	HH	HH	Z
30	HH	HH	L	HH	HH	HH	HH	HH	HH	HH	HH
31	HH	HH	H	HH	HH	HH	HH	HH	HH	HH	HH
32	HH	L	HH	HH	HH	HH	HH	HH	HH	HH	Z
33	HH	H	HH	HH	HH	HH	HH	HH	HH	HH	Z
34	HH	L	HH	HH	HH	HH	HH	HH	HH	HH	HH
35	HH	H	HH	HH	HH	HH	HH	HH	HH	HH	HH
36	L	HH	HH	HH	HH	HH	HH	HH	HH	HH	Z
37	H	HH	HH	HH	HH	HH	HH	HH	HH	HH	Z

L = V_{IL}, H = V_{IH}, HH = V_{IHH}, Z = high impedance (e.g., 10 kΩ to 5 V)

TABLE 2. PRODUCT LINE SELECT

PRODUCT LINE NUMBER	PIN NAME						
	PO0	PO1	PO2	PO3	PA2	PA1	PA0
0, 32	Z	Z	Z	HH	Z	Z	Z
1, 33	Z	Z	Z	HH	Z	Z	HH
2, 34	Z	Z	Z	HH	Z	HH	Z
3, 35	Z	Z	Z	HH	Z	HH	HH
4, 36	Z	Z	Z	HH	HH	Z	Z
5, 37	Z	Z	Z	HH	HH	Z	HH
6, 38	Z	Z	Z	HH	HH	HH	Z
7, 39	Z	Z	Z	HH	HH	HH	HH
8, 40	Z	Z	HH	Z	Z	Z	Z
9, 41	Z	Z	HH	Z	Z	Z	HH
10, 42	Z	Z	HH	Z	Z	HH	Z
11, 43	Z	Z	HH	Z	Z	HH	HH
12, 44	Z	Z	HH	Z	HH	Z	Z
13, 45	Z	Z	HH	Z	HH	Z	HH
14, 46	Z	Z	HH	Z	HH	HH	Z
15, 47	Z	Z	HH	Z	HH	HH	HH
16, 48	Z	HH	Z	Z	Z	Z	Z
17, 49	Z	HH	Z	Z	Z	Z	HH
18, 50	Z	HH	Z	Z	Z	HH	Z
19, 51	Z	HH	Z	Z	Z	HH	HH
20, 52	Z	HH	Z	Z	HH	Z	Z
21, 53	Z	HH	Z	Z	HH	Z	HH
22, 54	Z	HH	Z	Z	HH	HH	Z
23, 55	Z	HH	Z	Z	HH	HH	HH
24, 56	HH	Z	Z	Z	Z	Z	Z
25, 57	HH	Z	Z	Z	Z	Z	HH
26, 58	HH	Z	Z	Z	Z	HH	Z
27, 59	HH	Z	Z	Z	Z	HH	HH
28, 60	HH	Z	Z	Z	HH	Z	Z
29, 61	HH	Z	Z	Z	HH	Z	HH
30, 62	HH	Z	Z	Z	HH	HH	Z
31, 63	HH	Z	Z	Z	HH	HH	HH

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

PROGRAMMING WAVEFORMS FOR ARRAY FUSES

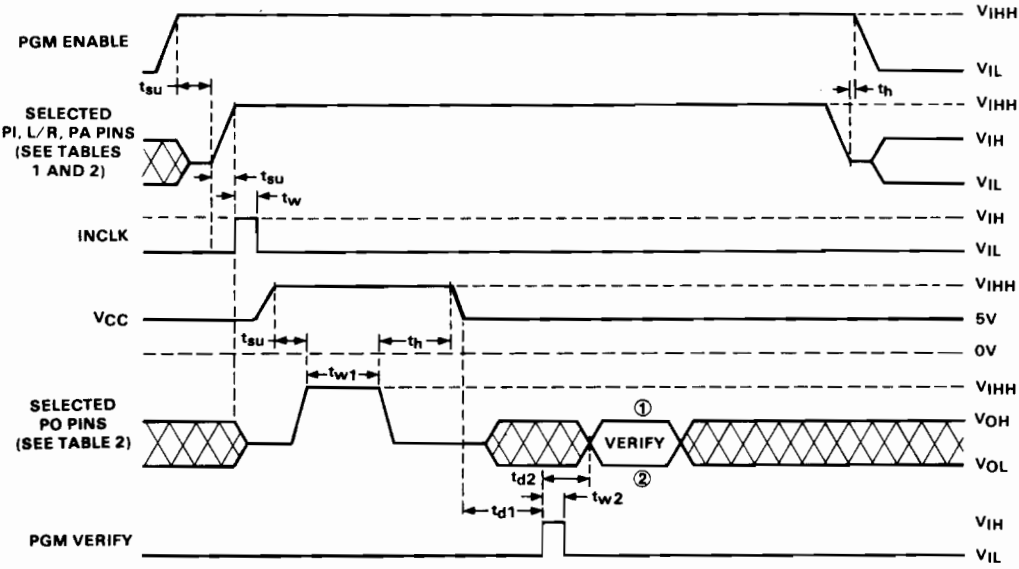
programming procedure for array fuses

Array fuses are programmed using a linear select method. Each fuse can be opened by selecting the appropriate (one of 40) input line and then pulsing the correct (one of 64) product line. The levels for selecting input lines and product lines are shown in Tables 1 and 2.

Step 1 Raise PGM ENABLE to V_{IHH}.
Step 2 Select an input line by applying appropriate levels to L/R and PI pins.
Step 3 Begin selection of the output line with appropriate conditions on PA pins.
Step 4 Pulse INCLK to V_{IH}.
Step 5 Raise V_{CC} to V_{IHH}.
Step 6 Blow the fuse by pulsing the appropriate PO pin to V_{IHH} as shown in Table 2 for the product line.
Step 7 Return V_{CC} to 5 volts and pulse PGM VERIFY. The PO pin selected in Step 6 will be less than V_{OL} if the fuse is open.

Steps 1 thru 7 may be repeated if the verification does not indicate that the fuse was successfully programmed (blown), but no more than 4 times. Verificatin is possible only with the verify-protect fuse intact.

To prevent further verification, two last fuses may be blown by raising pin 1 and pin 13 to 21 volts ±1 volts. V_{CC} is required to be at 0 during this operation.



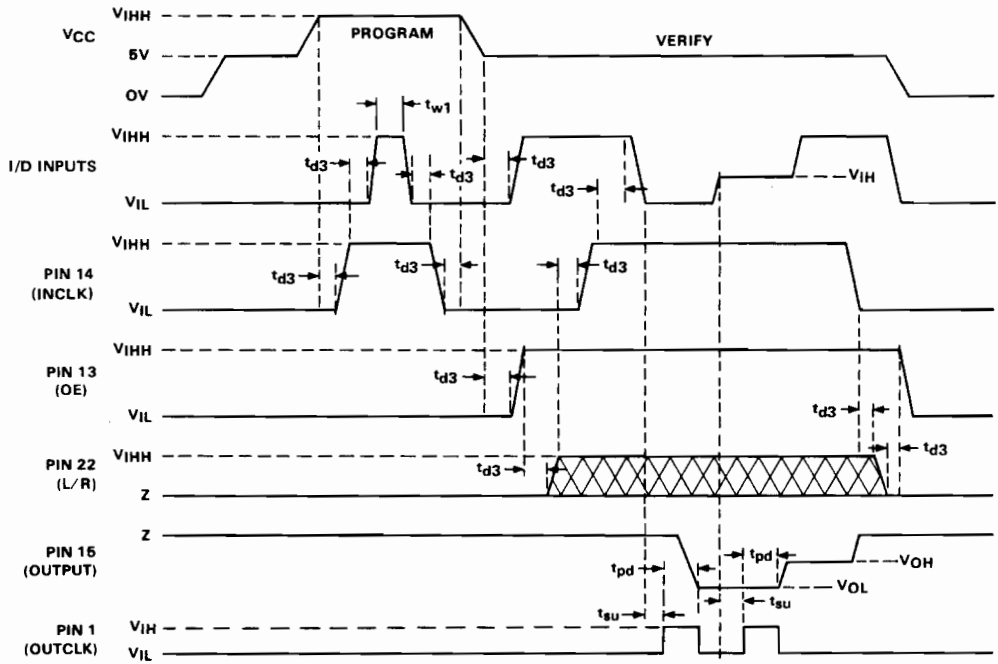
① A high level during the verify interval indicates that programming has not been successful.
② A low level during the verify interval indicates that programming has been successful.

programming procedure for architectural fuses (see Note 2)

Step 1	Apply low levefls to all I/D pins and 5 volts to the V_{CC} pin.
Step 2	Raise V_{CC} pin to V_{IHH}.
Step 3	Raise INCLK pin to V_{IHH}
Step 4	To program a D input pin into an I input pin pulse the selected pin to V_{IHH}.
Step 5	Lower INCLK to V_{IL} and V_{CC} to 5 volts.
Step 6	Raise pin 13 and all I/D input pins to V_{IHH}
Step 7	Set pin 22 to Z to select pins 2 thru 11 or set pin 22 to V_{IHH} to select pin 23.
Step 8	Raise INCLK to V_{IHH}.
Step 9	To verify that fuse has been blown, pulse selected I pin from V_{IHH} to V_{IL}, then to V_{IH} and back to V_{IHH} while clocking pin 1. If output at pin 15 follows the I input the fuse has been blown. The fuse on pin 25 is verified from pin 2.
Step 10	Repeat above steps 1 thru 9 for each D input to be programmed into an I input.

NOTE 2: Refer to pin assignments in operating mode for programming selected I/D pins from D input to I inputs.

programming waveforms



TEXAS INSTRUMENTS
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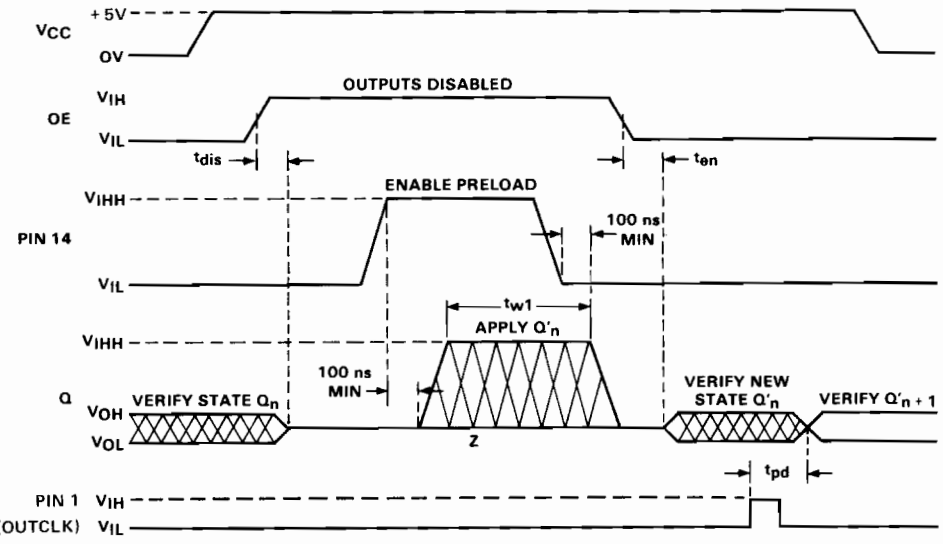
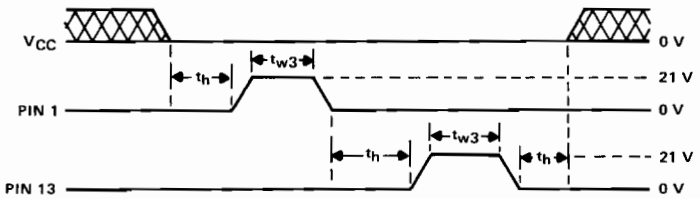
preload procedure for registered outputs

Step 1	Pin 13 to V_{IH}, Pin 1 to V_{IL}, and V_{CC} to 5 volts.
Step 2	Pin 14 to V_{IHH}.
Step 3	Apply an open circuit or V_{IL} for a low and V_{IHH} for a high at the Q outputs
Step 4	Pin 14 to V_{IL}
Step 5	Remove the voltages applied to the outputs.
Step 6	Pin 13 to V_{IL}.
Step 7	Check the output states to verify preload.

preload waveforms



security fuse programming



D2710, DECEMBER 1982 – REVISED JUNE 1984

- **Choice of Operating Speeds**
  HIGH PERFORMANCE . . . 30 MHz Max
  HALF-POWER . . . 18 MHz Max
- **Preload Capability on Output Registers**
- **Power-up Clear on Registered Devices**
- **DIP Options Include Both 300-mil Plastic and 600-mil Ceramic**

DEVICE	I/D INPUTS	I INPUTS	3-STATE O OUTPUTS	REGISTERED Q OUTPUTS	I/O PORTS
'PALT19L8	11	2	2	0	6
'PALT19R8	11	0	0	8 (3-state buffers)	4
'PALT19R6	11	0	0	6 (3-state buffers)	2
'PALT19R4	11	0	0	4 (3-state buffers)	0

description

These programmable array logic devices feature high speed and functionality similar to the TIBPAL16L8, 16R4, 16R6, 16R8 series, but with the added feature of D-type transparent latches on the inputs. If an input latch is not desired, it can be converted to an input buffer by simply programming the architectural fuse.

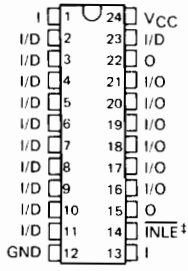
Combining Advanced Low-Power Schottky† technology, with proven titanium-tungsten fuses, these devices will provide reliable high performance substitutes over conventional TTL logic. Their easy programmability allows for quick design of custom functions and typically result in a more compact circuit board. In addition, chip carriers are available for further reduction in board space. The Half-power devices offer a choice of operating frequency, switching speed, and power dissipation.

All of the registered outputs are set to a low level during power-up. In addition, extra circuitry has been provided to allow loading of each register asynchronously to either a high or low state. This feature simplifies testing because the registers can be set to an initial state prior to executing the test sequence.

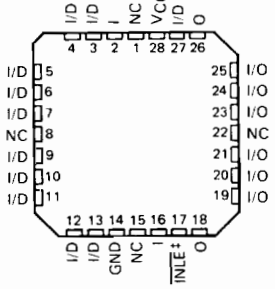
INPUT LATCH FUNCTION TABLE

$\overline{INLE}$	D	LATCH OUTPUT
L	L	L
L	H	H
H	X	Q_o

TIBPALT19L8'
M SUFFIX . . . JW PACKAGE
C SUFFIX . . . JW OR NT PACKAGE
(TOP VIEW)



TIBPALT19L8'
M SUFFIX . . . FH OR FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)

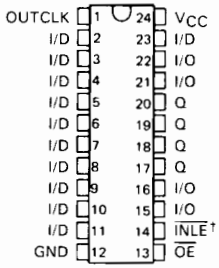


Pin assignments in operating mode (voltage at pins 1 and 13 less than V_{IHH})

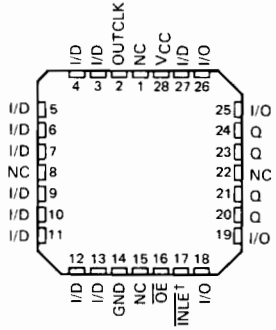
†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments, U.S. Patent Number 3,463,975.
‡$\overline{INLE}$ is also used for the preload.
PAL is a registered trademark of Monolithic Memories Inc.

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

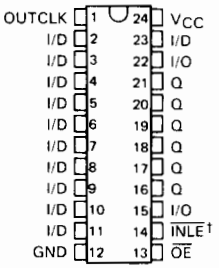
TIBPALT19R4'
M SUFFIX . . . JW PACKAGE
C SUFFIX . . . JW OR NT PACKAGE
(TOP VIEW)



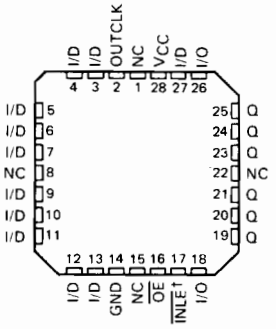
TIBPALT19R4'
M SUFFIX . . . FH OR FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



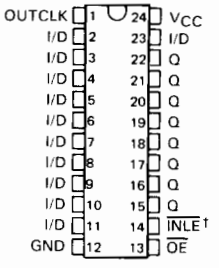
TIBPALT19R6'
M SUFFIX . . . JW PACKAGE
C SUFFIX . . . JW OR NT PACKAGE
(TOP VIEW)



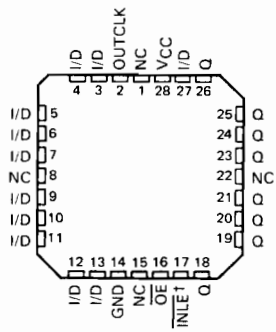
TIBPALT19R6'
M SUFFIX . . . FH OR FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



TIBPALT19R8'
M SUFFIX . . . JW PACKAGE
C SUFFIX . . . JW OR NT PACKAGE
(TOP VIEW)



TIBPALT19R8'
M SUFFIX . . . FH OR FK PACKAGE
C SUFFIX . . . FN PACKAGE
(TOP VIEW)



†INLE is also used for preload
Pin assignments in operating mode (voltage at pins 1 and 13 less than V_{IHH})

TEXAS INSTRUMENTS
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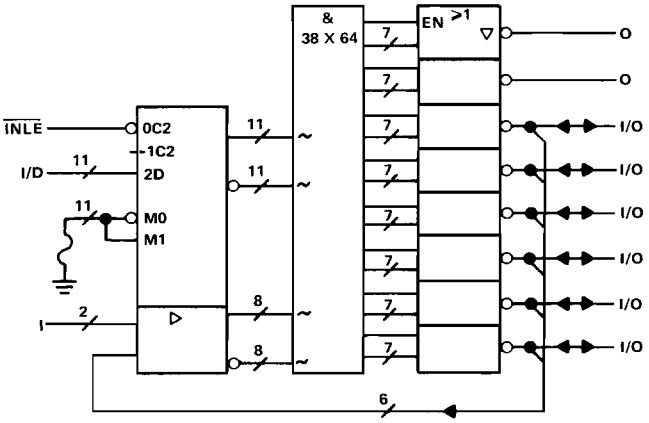
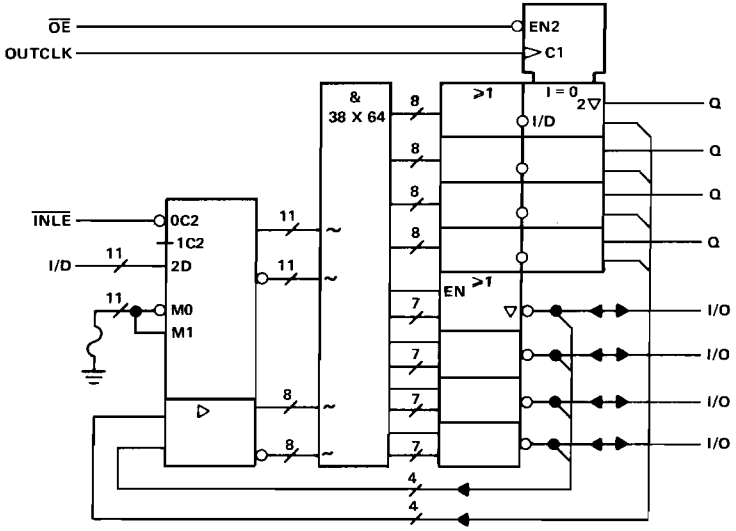
functional block diagrams (positive logic)

'PALT19L8



'PALT19R4



functional block diagrams (positive logic)

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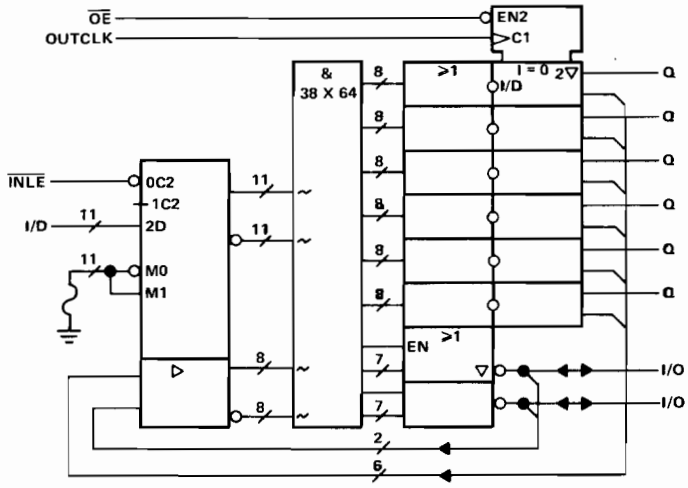

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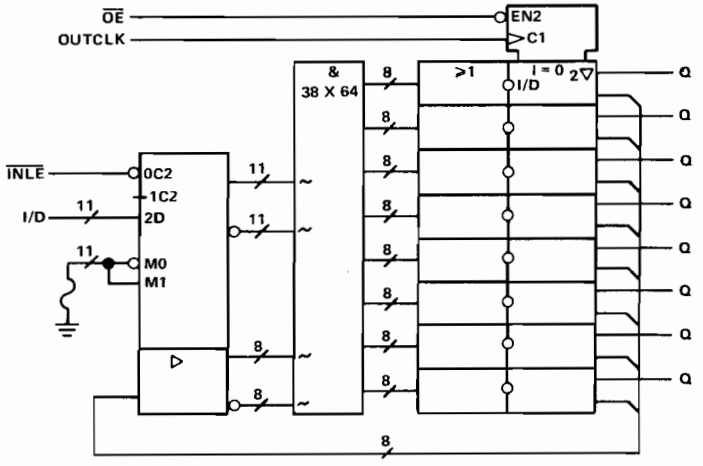
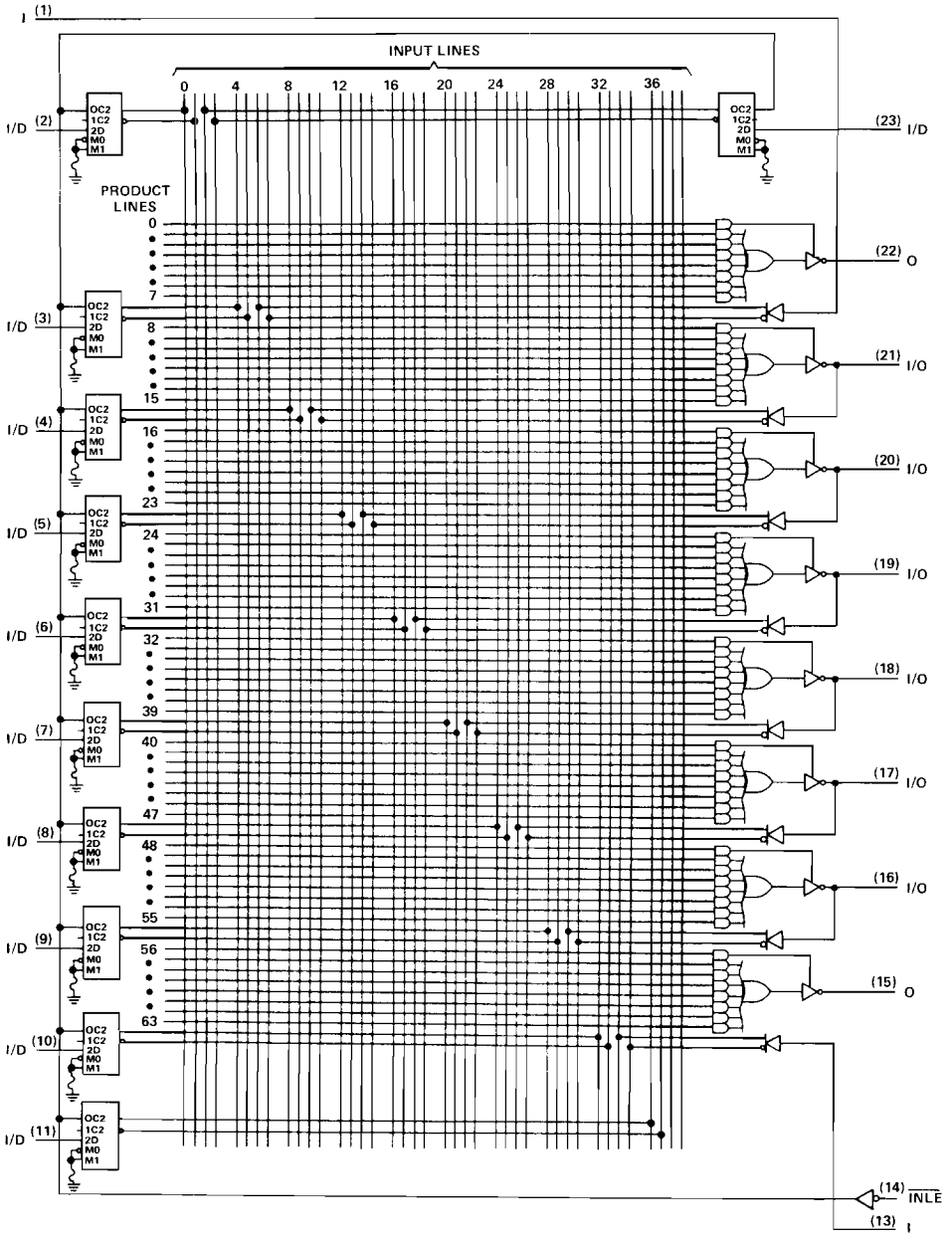
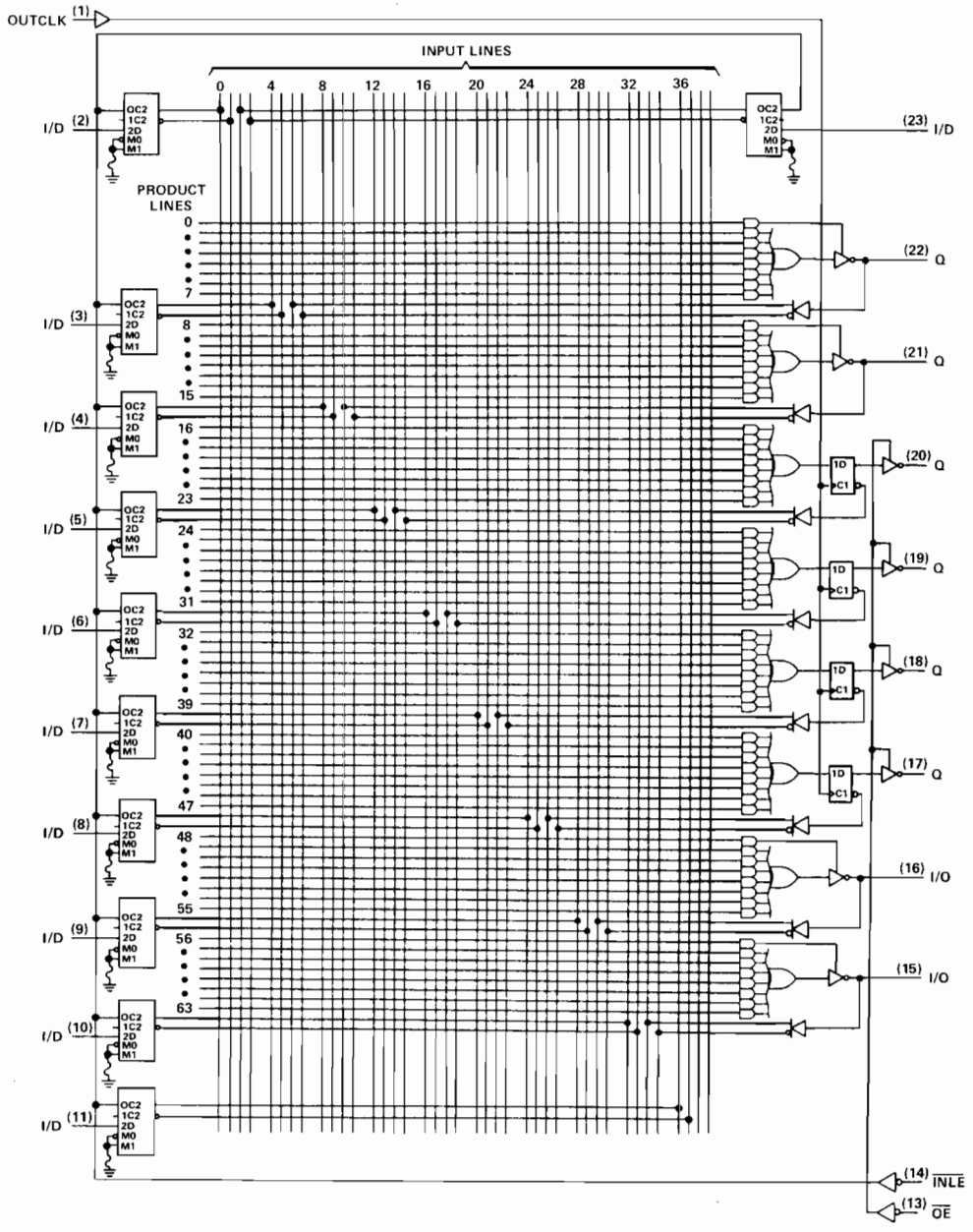


TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

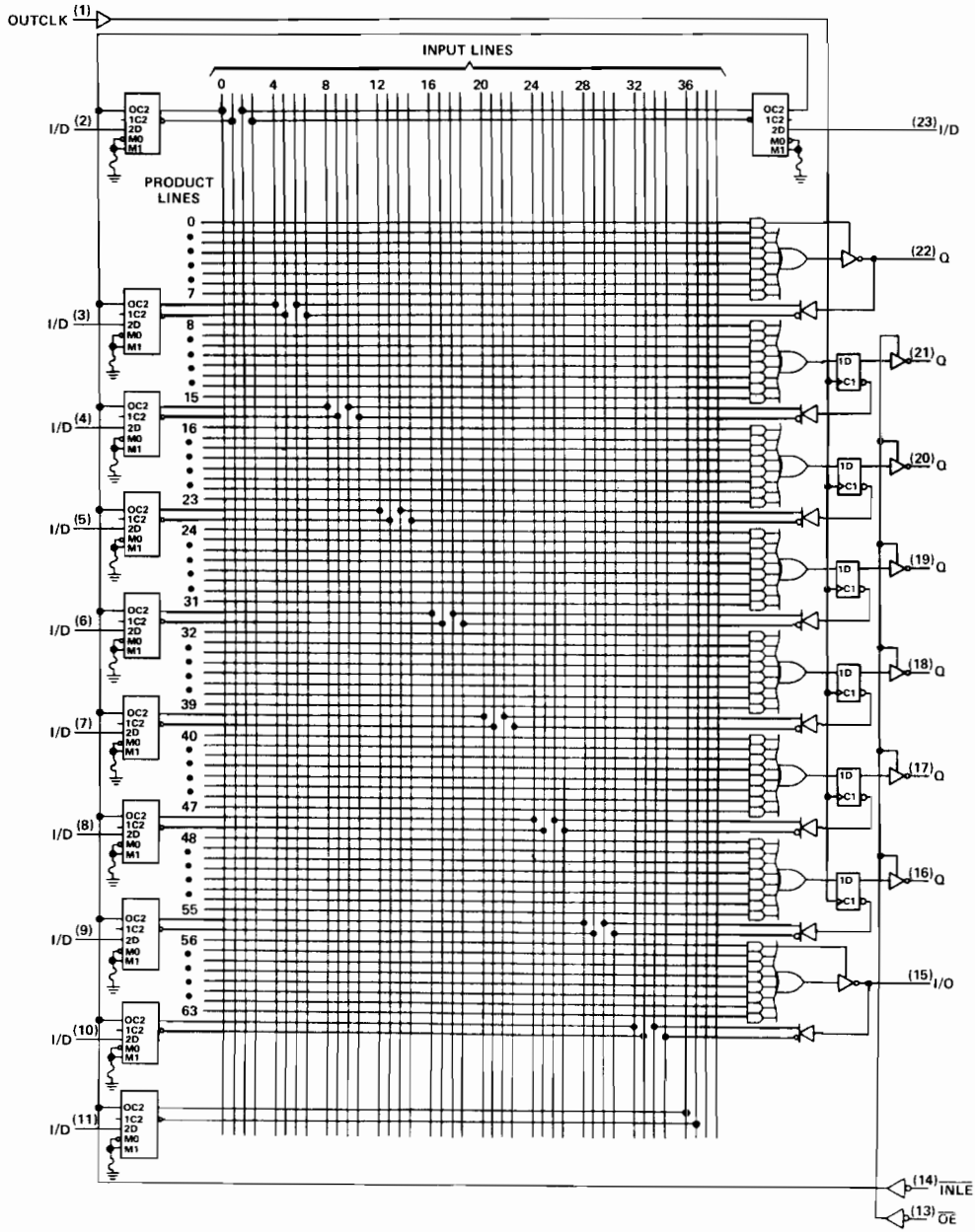


3

Field-Programmable Logic

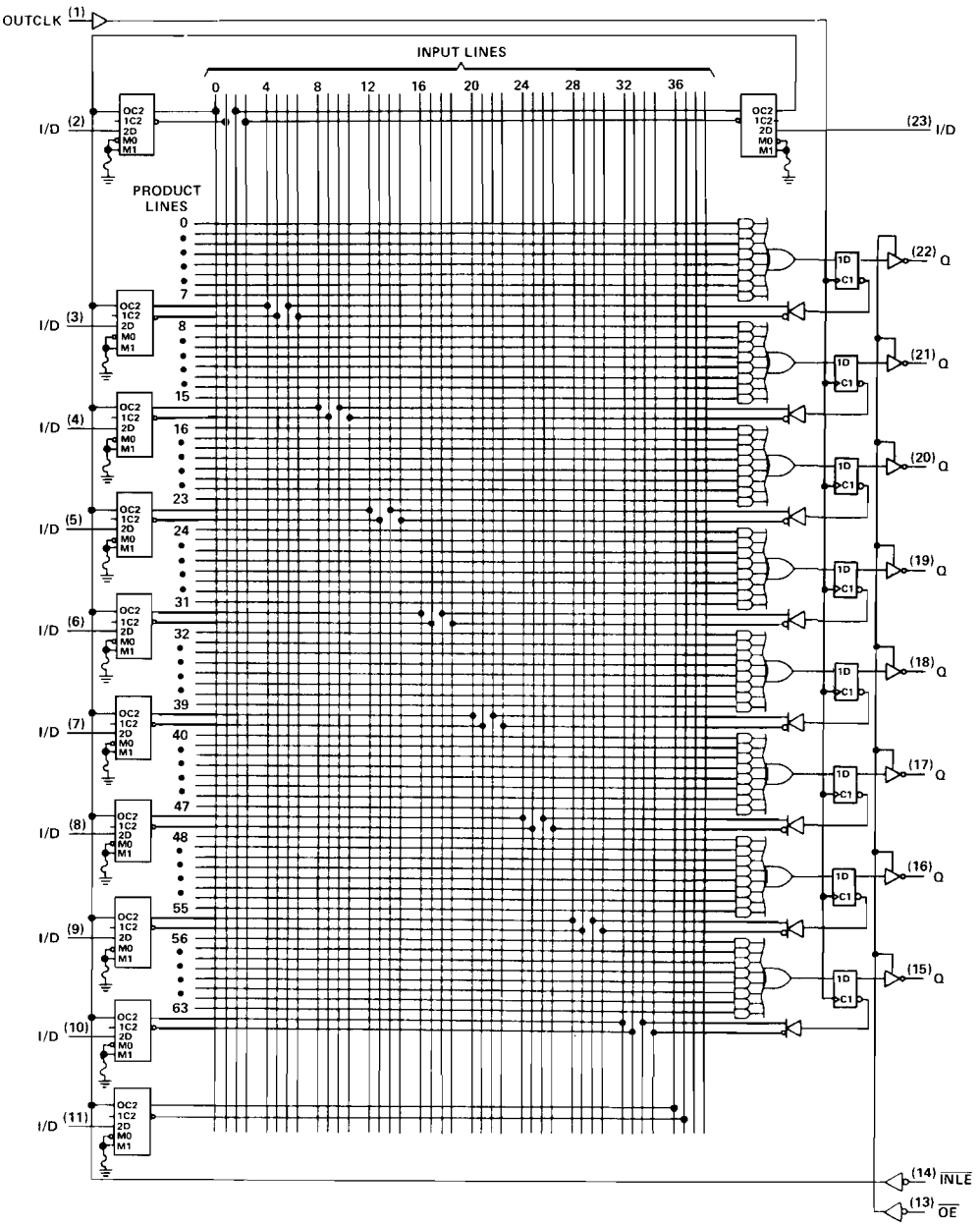


TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265



3

Field-Programmable Logic



TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Voltage applied to a disabled output (see Note 1) . . . . . 5.5 V
Operating free-air temperature range: M suffix . . . . . −55°C to 125°C
C suffix . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle or during preload cycle.

recommended operating conditions (see Note 2)

		M SUFFIX			C SUFFIX			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2		5.5	2		5.5	V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−2			−3.2	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

NOTE 2: These recommended operating conditions apply for all device dash numbers. Also refer to additional recommended operating conditions information pertaining to appropriate device dash numbers.

programming parameters, T_A = 25°C

			MIN	NOM	MAX	UNIT
V_{CC}	Verify-level supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2		5.5	V
V_{IL}	Low-level input voltage				0.8	V
V_{OH}	High-level output voltage				5.5	V
V_{IHH}	Program-pulse input voltage		10.25	10.5	10.75	V
I_{IHH}	Program-pulse input current	PO			50	mA
		PGM ENABLE, L/R			25	
		PI, PA			5	
		V_{CC}			400	
t_{w1}	Program-pulse duration at PO or I/D pins		10		50	μs
t_{w2}	Pulse duration at PGM VERIFY and INCLK		100			ns
t_{su}	Setup time		100			ns
t_h	Hold time		100			ns
t_{d1}	Delay time from V_{CC} to 5 V to PGM VERIFY↑		100			μs
t_{d2}	Delay time from PGM VERIFY↑ to verification of output		200			ns
t_{d3}	Delay time		100			ns
	Input voltage at pins 1 and 13 to open verify-protect (security) fuse		20	21	22	V
t_{w3}	Input current to open verify-protect (security) fuse				400	mA
	Pulse duration to open verify-protect (security) fuse		20		50	μs
	V_{CC} value during security fuse programming			0	0.4	V

recommended operating conditions

			M SUFFIX-XX			C SUFFIX-XX			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
f_{clock}	Clock frequency	OUTCLK							MHz
t_w	Pulse duration	$\overline{INLE}$ low							ns
		OUTCLK high							ns
		OUTCLK low							
t_{su}	Setup time, input or feedback before	$\overline{INLE}$↑							ns
		OUTCLK↑							
t_h	Hold time, input or feedback after $\overline{INLE}$↑ or OUTCLK↑		0			0			ns

electrical characteristics over recommended free-air operating temperature range

PARAMETER		TEST CONDITIONS†		M SUFFIX-XX			C SUFFIX-XX			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = MIN,	I_{OH} = MAX	2.4	3.2		2.4	3.3		V
V_{OL}		V_{CC} = MIN,	I_{OL} = MAX		0.25	0.4		0.35	0.5	V
I_{OZH}	Outputs	V_{CC} = MAX,	V_{IH} = 2.7 V			20			20	μA
	I/O ports					100			100	
I_{OZL}	Outputs	V_{CC} = MAX,	V_{IH} = 0.4 V		−20			−20		μA
	I/O ports					−250			−250	
I_I	$\overline{OE}$ input	V_{CC} = MAX,	V_I = 5.5 V			0.2			0.2	mA
	I/D inputs					0.1			0.1	
	All others					0.1			0.1	
I_{IH}	$\overline{OE}$ input	V_{CC} = MAX,	V_I = 2.7 V			40			40	μA
	I/D inputs					20			0.1	
	All others					20			0.1	
I_{IL}	$\overline{OE}$ input	V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4	mA
	I/D inputs					−0.6			−0.6	
	All others					−0.2			−0.2	
I_O§		V_{CC} = MAX,	V_O = 2.25 V	−30		−125	−30		−125	mA
I_{CC}		V_{CC} = MAX, Outputs open	V_I = 0 V,		150	210		150	210	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half the true short-circuit current, I_{OS}.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	INPUT MODE	TEST CONDITIONS	M SUFFIX-XX			C SUFFIX-XX			UNIT
					MIN	TYP†	MAX	MIN	TYP†	MAX	
f_{max}			Either	R_L = 500 Ω, C_L = 50 pF, See Note 3	30			30			MHz
t_{pd}	I, I/O	I/O, O	Either			16			16		ns
t_{pd}	OUTCLK↑	Q	Either			12			12		ns
t_{en}	$\overline{OE}$↓	Q	Either			8			8		ns
t_{dis}	$\overline{OE}$↑	Q	Either			6			6		ns
t_{pd}	$\overline{INLE}$↓	I/O, O	Latched			16			16		ns
t_{en}	$\overline{INLE}$↓	I/O, O, Q	Latched			25			25		ns
t_{dis}	$\overline{INLE}$↓	I/O, O, Q	Latched			20			20		ns
t_{pd}	I/D	I/O, O	Buffered			20			20		ns
t_{en}	I/D, I/O	I/O	Buffered			22			22		ns
t_{dis}	I/D, I/O	I/O	Buffered			17			17		ns

†All typical values are V_{CC} = 5 V, T_A = 25°C.
NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

recommended operating conditions

			M SUFFIX-XX			C SUFFIX-XX			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
f_{clock}	Clock frequency	OUTCLK							MHz
t_w	Pulse duration	$\overline{INLE}$ low							ns
		OUTCLK high							ns
		OUTCLK low							
t_{su}	Setup time, input or feedback before	$\overline{INLE}$↑							ns
		OUTCLK↑							
t_h	Hold time, input or feedback after $\overline{INLE}$↑ or OUTCLK↑		0			0			ns

electrical characteristics over recommended free-air operating temperature range

PARAMETER		TEST CONDITIONS†	M SUFFIX-XX			C SUFFIX-XX			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		V_{CC} = MIN, I_I = −18 mA			−1.5			−1.5	V
V_{OH}		V_{CC} = MIN, I_{OH} = MAX	2.4	3.2		2.4	3.3		V
V_{OL}		V_{CC} = MIN, I_{OL} = MAX		0.25	0.4		0.35	0.5	V
I_{OZH}	Outputs	V_{CC} = MAX, V_{IH} = 2.7 V			20			20	μA
	I/O ports				100			100	
I_{OZL}	Outputs	V_{CC} = MAX, V_{IH} = 0.4 V		−20			−20		μA
	I/O ports				−250			−250	
I_I	$\overline{OE}$ Input	V_{CC} = MAX, V_I = 5.5 V			0.2			0.2	mA
	I/D Inputs				0.1			0.1	
	All others				0.1			0.1	
I_{IH}	$\overline{OE}$ Input	V_{CC} = MAX, V_I = 2.7 V			40			40	μA
	I/D Inputs				20			0.1	
	All others				20			0.1	
I_{IL}	$\overline{OE}$ Input	V_{CC} = MAX, V_I = 0.4 V			−0.4			−0.4	mA
	I/D Inputs				−0.6			−0.6	
	All others				−0.2			−0.2	
I_O§		V_{CC} = MAX, V_O = 2.25 V	−30		−125	−30		−125	mA
I_{CC}		V_{CC} = MAX, V_I = 0 V, Outputs open		75	105		75	105	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half the true short-circuit current, I_{OS}.

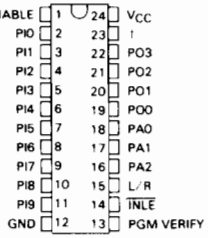
TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

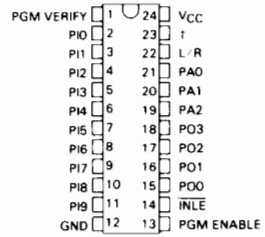
	FROM	TO	INPUT MODE	TEST CONDITIONS	M SUFFIX-XX MIN	M SUFFIX-XX TYP†	M SUFFIX-XX MAX	C SUFFIX-XX MIN	C SUFFIX-XX TYP†	C SUFFIX-XX MAX	UNIT
f_{max}			Either	R_L = 500 Ω, C_L = 50 pF, See Note 3	18			18			MHz
t_{pd}	I, I/O	I/O, O	Either			25			25		ns
t_{pd}	OUTCLK↑	Q	Either			20			20		ns
t_{en}	$\overline{OE}$↓	Q	Either			15			15		ns
t_{dis}	$\overline{OE}$↑	Q	Either			12			12		ns
t_{pd}	$\overline{INLE}$↓	I/O, O	Latched			25			25		ns
t_{en}	$\overline{INLE}$↓	I/O, O, Q	Latched			35			35		ns
t_{dis}	$\overline{INLE}$↓	I/O, O, Q	Latched			30			30		ns
t_{pd}	I/D	I/O, O	Buffered			30			30		ns
t_{en}	I/D, I/O	I/O	Buffered			32			32		ns
t_{dis}	I/D, I/O	I/O	Buffered			26			26		ns

†All typical values are V_{CC} = 5 V, T_A = 25°C.
NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

PRODUCT TERMS 0 THRU 31
(TOP VIEW)



PRODUCT TERMS 32 THRU 63
(TOP VIEW)



†No programming function. Make no connection.
Pin assignments in programming mode (PGM ENABLE, pin 1 or 13, at V_{IHH})

TABLE 1. INPUT LINE SELECT

INPUT LINE NUMBER	PIN NAME										
	PI9	PI8	PI7	PI6	PI5	PI4	PI3	PI2	PI1	PI0	L/R
0	HH	HH	HH	HH	HH	HH	HH	HH	HH	L	Z
1	HH	HH	HH	HH	HH	HH	HH	HH	HH	H	Z
2	HH	HH	HH	HH	HH	HH	HH	HH	HH	L	HH
3	HH	HH	HH	HH	HH	HH	HH	HH	HH	H	HH
4	HH	HH	HH	HH	HH	HH	HH	HH	L	HH	Z
5	HH	HH	HH	HH	HH	HH	HH	HH	H	HH	Z
6	HH	HH	HH	HH	HH	HH	HH	HH	L	HH	HH
7	HH	HH	HH	HH	HH	HH	HH	HH	H	HH	HH
8	HH	HH	HH	HH	HH	HH	HH	L	HH	HH	Z
9	HH	HH	HH	HH	HH	HH	HH	H	HH	HH	Z
10	HH	HH	HH	HH	HH	HH	HH	L	HH	HH	HH
11	HH	HH	HH	HH	HH	HH	HH	H	HH	HH	HH
12	HH	HH	HH	HH	HH	HH	L	HH	HH	HH	Z
13	HH	HH	HH	HH	HH	HH	H	HH	HH	HH	Z
14	HH	HH	HH	HH	HH	HH	L	HH	HH	HH	HH
15	HH	HH	HH	HH	HH	HH	H	HH	HH	HH	HH
16	HH	HH	HH	HH	HH	L	HH	HH	HH	HH	Z
17	HH	HH	HH	HH	HH	H	HH	HH	HH	HH	Z
18	HH	HH	HH	HH	HH	L	HH	HH	HH	HH	HH
19	HH	HH	HH	HH	HH	H	HH	HH	HH	HH	HH
20	HH	HH	HH	HH	L	HH	HH	HH	HH	HH	Z
21	HH	HH	HH	HH	H	HH	HH	HH	HH	HH	Z
22	HH	HH	HH	HH	L	HH	HH	HH	HH	HH	HH
23	HH	HH	HH	HH	H	HH	HH	HH	HH	HH	HH
24	HH	HH	HH	L	HH	HH	HH	HH	HH	HH	Z
25	HH	HH	HH	H	HH	HH	HH	HH	HH	HH	Z
26	HH	HH	HH	L	HH	HH	HH	HH	HH	HH	HH
27	HH	HH	HH	H	HH	HH	HH	HH	HH	HH	HH
28	HH	HH	L	HH	HH	HH	HH	HH	HH	HH	Z
29	HH	HH	H	HH	HH	HH	HH	HH	HH	HH	Z
30	HH	HH	L	HH	HH	HH	HH	HH	HH	HH	HH
31	HH	HH	H	HH	HH	HH	HH	HH	HH	HH	HH
32	HH	L	HH	HH	HH	HH	HH	HH	HH	HH	Z
33	HH	H	HH	HH	HH	HH	HH	HH	HH	HH	Z
34	HH	L	HH	HH	HH	HH	HH	HH	HH	HH	HH
35	HH	H	HH	HH	HH	HH	HH	HH	HH	HH	HH
36	L	HH	HH	HH	HH	HH	HH	HH	HH	HH	Z
37	H	HH	HH	HH	HH	HH	HH	HH	HH	HH	Z

TABLE 2. PRODUCT LINE SELECT

PRODUCT LINE NUMBER	PIN NAME						
	PO0	PO1	PO2	PO3	PA2	PA1	PA0
0, 32	Z	Z	Z	HH	Z	Z	Z
1, 33	Z	Z	Z	HH	Z	Z	HH
2, 34	Z	Z	Z	HH	Z	HH	Z
3, 35	Z	Z	Z	HH	Z	HH	HH
4, 36	Z	Z	Z	HH	HH	Z	Z
5, 37	Z	Z	Z	HH	HH	Z	HH
6, 38	Z	Z	Z	HH	HH	HH	Z
7, 39	Z	Z	Z	HH	HH	HH	HH
8, 40	Z	Z	HH	Z	Z	Z	Z
9, 41	Z	Z	HH	Z	Z	Z	HH
10, 42	Z	Z	HH	Z	Z	HH	Z
11, 43	Z	Z	HH	Z	Z	HH	HH
12, 44	Z	Z	HH	Z	HH	Z	Z
13, 45	Z	Z	HH	Z	HH	Z	HH
14, 46	Z	Z	HH	Z	HH	HH	Z
15, 47	Z	Z	HH	Z	HH	HH	HH
16, 48	Z	HH	Z	Z	Z	Z	Z
17, 49	Z	HH	Z	Z	Z	Z	HH
18, 50	Z	HH	Z	Z	Z	HH	Z
19, 51	Z	HH	Z	Z	Z	HH	HH
20, 52	Z	HH	Z	Z	HH	Z	Z
21, 53	Z	HH	Z	Z	HH	Z	HH
22, 54	Z	HH	Z	Z	HH	HH	Z
23, 55	Z	HH	Z	Z	HH	HH	HH
24, 56	HH	Z	Z	Z	Z	Z	Z
25, 57	HH	Z	Z	Z	Z	Z	HH
26, 58	HH	Z	Z	Z	Z	HH	Z
27, 59	HH	Z	Z	Z	Z	HH	HH
28, 60	HH	Z	Z	Z	HH	Z	Z
29, 61	HH	Z	Z	Z	HH	Z	HH
30, 62	HH	Z	Z	Z	HH	HH	Z
31, 63	HH	Z	Z	Z	HH	HH	HH

$L = V_{IL}$, $H = V_{IH}$, $HH = V_{IHH}$, Z = high impedance (e.g., 10 kΩ to 5 V)

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

programming procedure for array fuses

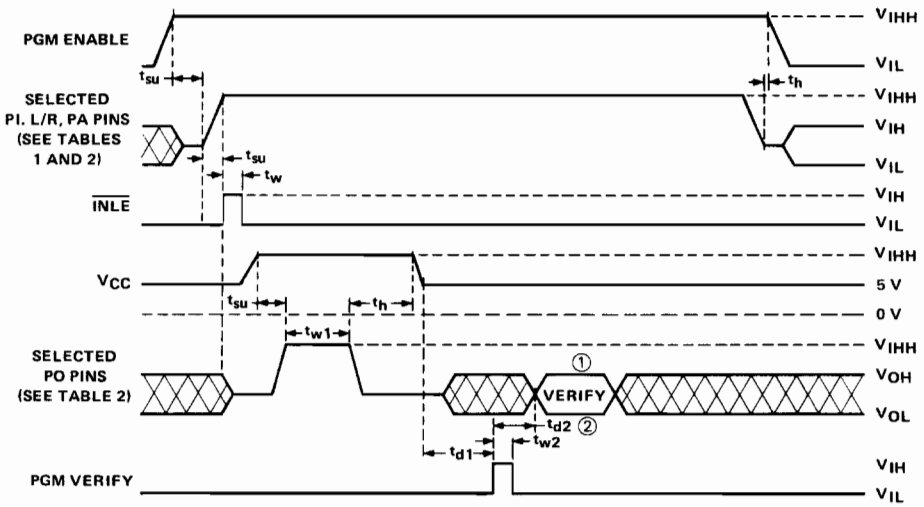
Array fuses are programmed using a linear select method. Each fuse can be opened by selecting the appropriate (one of 40) input line and then pulsing the correct (one of 64) product line. The levels for selecting input lines and product lines are shown in Tables 1 and 2.

Step 1 Raise PGM ENABLE to V_{IHH}.
Step 2 Select an input line by applying appropriate levels to L/R and PI pins.
Step 3 Begin selection of the output line with appropriate conditions on PA pins.
Step 4 Pulse $\overline{INLE}$ to V_{IH}.
Step 5 Raise V_{CC} to V_{IHH}.
Step 6 Blow the fuse by pulsing the appropriate PO pin to V_{IHH} as shown in Table 2 for the product line.
Step 7 Return V_{CC} to 5 volts and pulse PGM VERIFY. The PO pin selected in Step 6 will be less than V_{OL} if the fuse is open.

Steps 1 thru 7 may be repeated if the verification does not indicate that the fuse was successfully programmed (blown), but no more than 4 times. Verification is possible only with the verify-protect fuse intact.

To prevent further verification, two last fuses may be blown by raising pin 1 and pin 13 to 21 volts ± 1 volt. V_{CC} is required to be at 0 during this operation.

programming waveforms



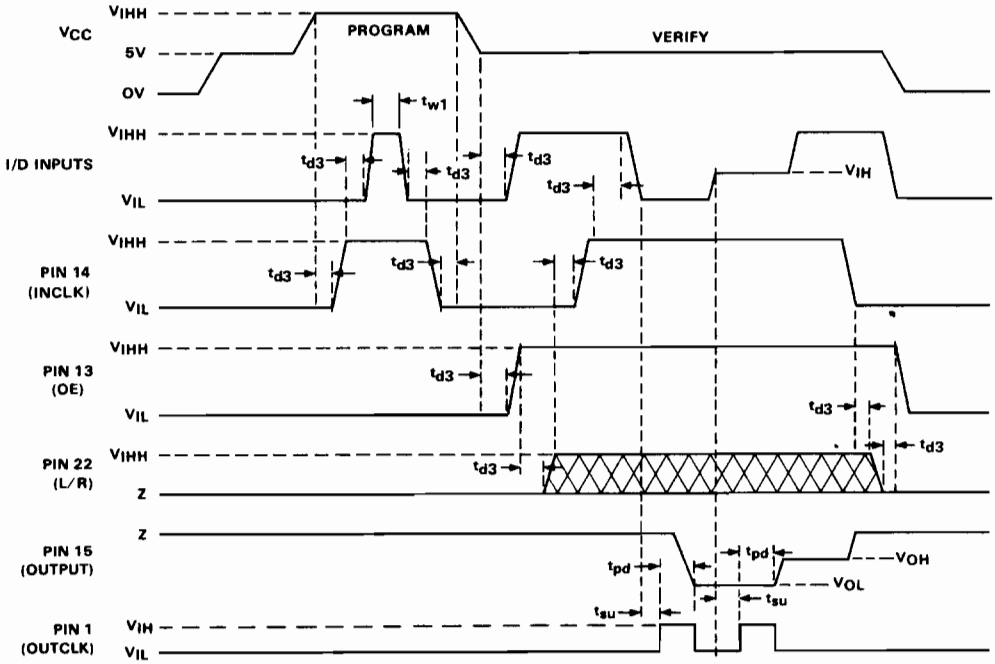
① A high level during the verify interval indicates that programming has not been successful.
② A low level during the verify interval indicates that programming has been successful.

programming procedure for architectural fuses (see Note 2)

Step 1 Apply low levels to all I/D pins and 5 volts to the V_{CC} pin.
Step 2 Raise V_{CC} pin to V_{IHH}.
Step 3 Raise INCLK pin to V_{IHH}.
Step 4 To program a D input pin into an I input pin pulse the selected pin to V_{IHH}.
Step 5 Lower INCLK to V_{IL} and V_{CC} to 5 volts.
Step 6 Raise pin 13 and all I/D input pins to V_{IHH}.
Step 7 Set pin 22 to Z to select pins 2 thru 11 or set pin 22 to V_{IHH} to select pin 23.
Step 8 Raise INCLK to V_{IHH}.
Step 9 To verify that fuse has been blown, pulse selected I pin from V_{IHH} to V_{IL}, then to V_{IH} and back to V_{IHH} while clocking pin 1. If output at pin 15 follows the I input the fuse has been blown. The fuse on pin 23 is verified from pin 2.
Step 10 Repeat above steps 1 thru 9 for each D input to be programmed into an I input.

NOTE 2: Refer to pin assignments in operating mode for programming selected I/D pins from D input to I inputs.

programming waveforms

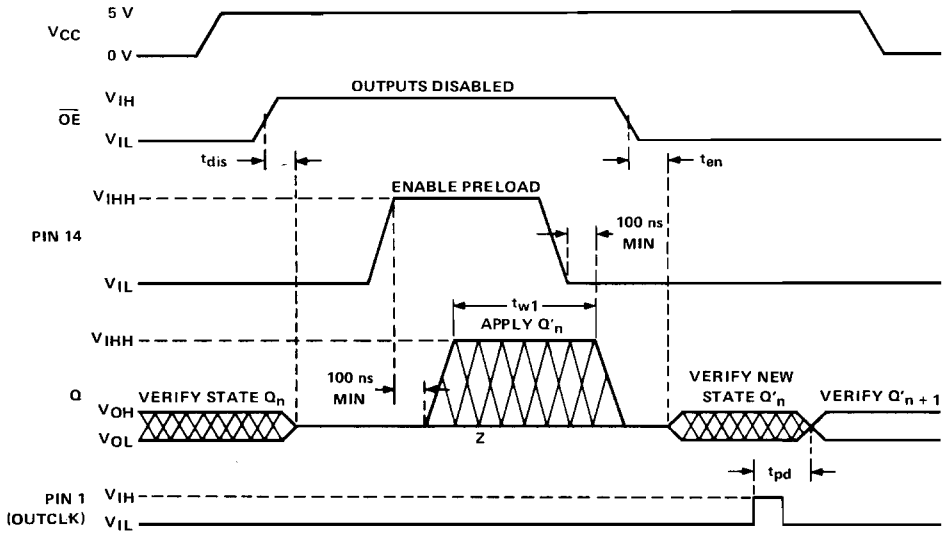


TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

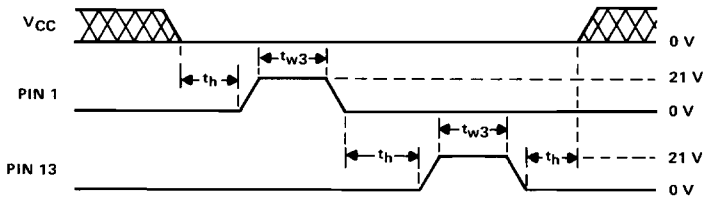
preload procedure for registered outputs

Step 1 Pin 13 to V_{IH}, Pin 1 to V_{IL}, and V_{CC} to 5 volts.
Step 2 Pin 14 to V_{IHH}.
Step 3 Apply an open circuit or V_{IL} for a low and V_{IHH} for a high at the Q outputs.
Step 4 Pin 14 to V_{IL}.
Step 5 Remove the voltages applied to the outputs.
Step 6 Pin 13 to V_{IL}.
Step 7 Check the output states to verify preload.

preload waveforms



security fuse programming



TIFPLA839, TIFPLA840
14 × 32 × 6 FIELD-PROGRAMMABLE LOGIC ARRAYS

JUNE 1984 - REVISED NOVEMBER 1984

- **Input-to-Output Propagation Delay . . . 10 ns Typical**
- **24-Pin, 300-mil Slim Line Packages**
- **Power Dissipation . . . 650 mW Typical**
- **Programmable Output Polarity**

description

The 'FPLA839 (3-state outputs) and the 'FPLA840 (open-collector outputs) are TTL field-programmable logic arrays containing 32 product terms (AND terms) and six sum terms (OR terms). Each of the sum-of-products output functions can be programmed either high true or low true. The true condition of each output function is activated by the programmed logical minterms of 14 input variables. The outputs are controlled by two chip-enable pins to allow output inhibit and expansion of terms.

These devices provide high-speed data-path logic replacement where several conventional SSI functions can be designed into a single package.

The 'FPLA839M and 'FPLA840M are characterized for operation over the full military temperature range of −55°C to 125°C. The 'FPLA839C and 'FPLA840C are characterized for operation from 0°C to 70°C.

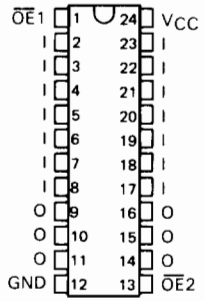
LOGIC FUNCTION

$f(I) = P0 + P1 \ldots P31$ for polarity link intact

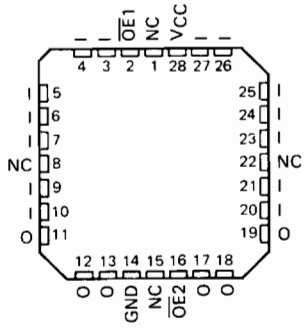
$f(I) = \overline{P0} * \overline{P1} * \ldots * \overline{P31}$ for polarity link open

where P0 through P31 are product terms

TIFPLA839M, TIFPLA840M . . . JT PACKAGE
TIFPLA839C, TIFPLA840C . . . JT OR NT PACKAGE
(TOP VIEW)



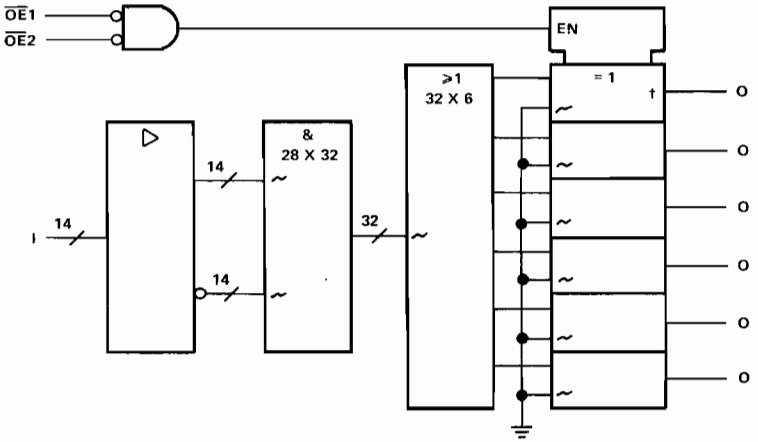
TIFPLA839M, TIFPLA840M . . . FH OR FK PACKAGE
TIFPLA839C, TIFPLA840C . . . FN PACKAGE
(TOP VIEW)



Pin assignments in operating mode (pin 1 is less positive than V_{IHH})

3 Field-Programmable Logic

functional block diagram (positive logic)



~denotes fused inputs.
†FPLA839 has 3-state (▽) outputs; FPLA840 has open-collector (◇) outputs.

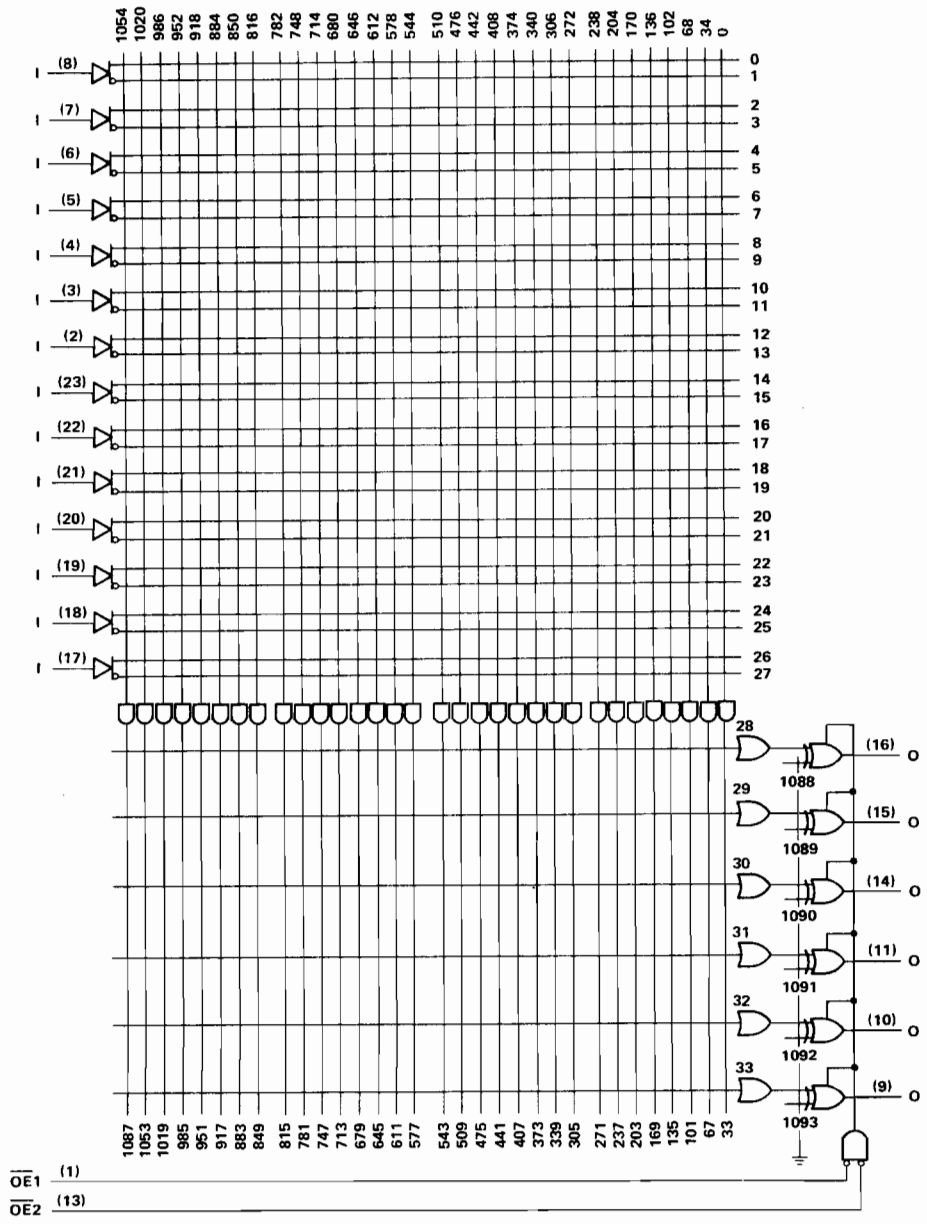
absolute maximum ratings

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage (see Note 1)	5.5 V
Off-state output voltage (see Note 1)	5.5 V
Operating free-air temperature range: 'FPLA839M, 'FPLA840M	−55°C to 125°C
'FPLA839C, 'FPLA840C	0°C to 70°C
Storage temperature	−65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle.

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

LOGIC DIAGRAM



recommended operating conditions

		M SUFFIX			C SUFFIX			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level input voltage, V_{IH}		2			2			V
Low-level input voltage, V_{IL}				0.8			0.8	V
High-level output voltage, V_{OH}	'FPLA840			5.5			5.5	V
High-level output current, I_{OH}	'FPLA839			−2			−3.2	mA
Low-level output current, I_{OL}				12			24	mA
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		M SUFFIX			C SUFFIX			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
I_{OH} 'FPLA840	V_{CC} = MIN,	V_{OH} = 5.5 V			0.1			0.1	mA
V_{OH} 'FPLA839	V_{CC} = MIN,	I_{OH} = MAX	2.4	3.2		2.4	3		V
V_{OL}	V_{CC} = MIN,	I_{OL} = MAX		0.25	0.5		0.37	0.5	V
I_I	V_{CC} = MAX,	V_I = 5.5 V			0.1			0.1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = MAX,	V_I = 0.4 V			−0.5			−0.5	mA
I_O§	V_{CC} = MAX,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{OZH}	V_{CC} = MAX,	V_O = 2.7 V			20			20	μA
I_{OZL}	V_{CC} = MAX,	V_O = 0.4 V			−20			−20	μA
I_{CC}	V_{CC} = MAX, $\overline{OE}$ inputs at V_{IH}	V_I = 0 V,		130	190		130	180	mA

'FPLA839 switching characteristics

PARAMETER	FROM	TO	TEST CONDITIONS	M SUFFIX			C SUFFIX			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{pd}	Input	Output	R_L = 500 to GND, C_L = 50 pF to GND		10	25		10	20	ns
t_{en}	Pin 1 or Pin 13	Output	R_{L1} = 500 to 7 V, R_L = 500 to GND, C_L = 50 pF to GND		10	25		10	20	ns
t_{dis}					8	20		8	15	

'FPLA840 switching characteristics

PARAMETER	FROM	TO	TEST CONDITIONS	M SUFFIX			C SUFFIX			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{pd}	Input	Output	R_L = 500 to V_{CC}, C_L = 50 pF to GND		10	30		10	25	ns
t_{en}	Pin 1 or Pin 13	Output	R_{L1} = 500 to 7 V, R_L = 500 to GND, C_L = 50 pF to GND		10	25		10	20	ns
t_{dis}					8	20		8	15	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit current, I_{OS}.

TEXAS INSTRUMENTS
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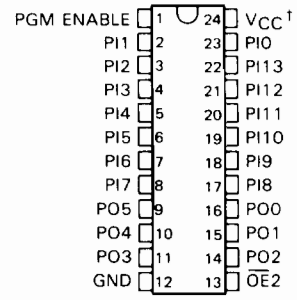
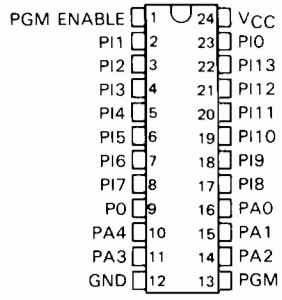
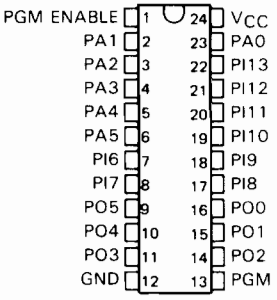
OUTPUT POLARITY
(PGM ENABLE = V_{ILL})



AND MATRIX
(V_{CC3})



OR MATRIX
(V_{CC1}, PA5 = V_{IL})



†V_{CC} = V_{CC2} for program and V_{CC1} for verify
Pin assignment in programming mode (pin 1 ≤ V_{IHH}) top views

programming parameters, T_A = 25°C

PARAMETER		MEASURED AT	PROGRAMMING MODE	MIN	TYP	MAX	UNIT
V_{IHH}	Program high-level input voltage	PGM ENABLE	AND, OR	16.5	17	17.5	V
		PO pins	Polarity				
V_{ILL}	Program low-level input voltage	PGM ENABLE	Any	0		0.4	V
I_{IHH}	Program-level input current	PO pins	Polarity		100		mA
		PGM ENABLE	AND, OR		150		
V_{IX}	Program-level input voltage	PO0 thru PO5	Polarity	9.5	10	10.5	V
		PGM	AND, OR				
I_{IX}	Program-level input current	PI pins	AND		0.6	2	mA
		$\overline{OE}2$	Polarity			5	
		PO0 thru PO5	OR		5	10	
V_{CC1}	Programming supply voltage	V_{CC}	OR	8.5	8.75	9	V
I_{CC1}	Programming supply current	V_{CC}	OR		250	400	mA
V_{CC2}	Programming supply voltage	V_{CC}	Polarity		0	0.4	V
V_{CC3}	Programming supply voltage	V_{CC}	AND	4.75	5	5.25	V
V_{IH}	High-level input voltage	Any	Any	2			V
V_{IL}	Low-level input voltage	Any	Any	0		0.8	V
V_{OH}	High-level output voltage	Any	Any	2.4	3.2		V
V_{OL}	Low-level output voltage	Any	Any		0.25	0.5	V
t_w	Program pulse duration	PO0 thru PO5	Polarity		50	1000	μs
		PGM	AND, OR				
	Program pulse duty cycle	PO0 thru PO5	Polarity		10	50	%
		PGM	AND, OR				
t_d	Delay time	Any	Any	10			μs
t_r	Rise time	Any	Any		25		μs

3

Field-Programmable Logic

PROGRAMMING PROCEDURE

OUTPUT POLARITY

Program

Load all output pins with a 10-kΩ resistor to 5 V and set pin 12 (GND) to 0 V. Program the output polarity before programming either the AND matrix or the OR matrix. An unprogrammed device has all six outputs noninverting. When the polarity link of an output is opened, the output function becomes inverting. Program one output at a time as follows:

Step 1: Set PGM ENABLE (pin 1) to V_{ILL}.
Step 2: Set V_{CC} (pin 24) to V_{CC2}; set $\overline{OE}2$ (pin 13) to V_{IH} and PI0 through PI13 to V_{IH}.
Step 3: Ramp the appropriate output to V_{IHH} and remove after t_w.
Step 4: Repeat step 3 for each output to be programmed low.

Verify

Step 1: Set PGM ENABLE (pin 1) to V_{ILL}; set V_{CC} (pin 24) to V_{CC2}; set PI0 through PI13 to V_{IH}.
Step 2: Wait t_d and raise V_{CC} (pin 24) to V_{CC1}.
Step 3: Enable the device by applying V_{IL} to $\overline{OE}2$ (pin 13).
Step 4: Sense the logic state of all six outputs. An output at V_{OH} has been programmed to be inverting, while an output at V_{OL} has remained noninverting.
Step 5: Remove V_{CC1}.

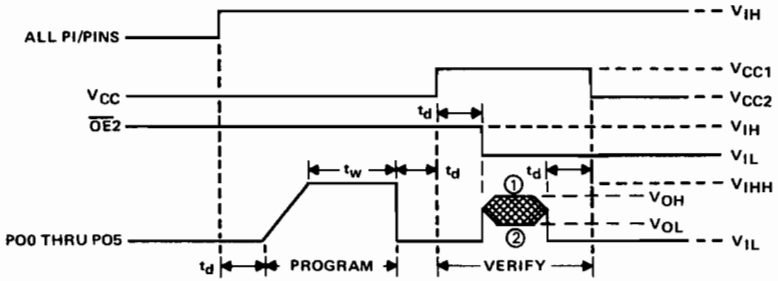


FIGURE 1. OUTPUT POLARITY PROGRAMMING WAVEFORMS

AND MATRIX

Program

Program the output polarity before programming either the AND matrix or the OR matrix. Load all output pins with a 10-kΩ resistor to 5 V and set pin 12 (GND) to V_{IL}. Program each input separately for each product term, one fuse at a time. Unused terms do not require fusing, however, all input variables of a selected product term must be programmed either true, complement, or don't care (both links are blown), as follows:

Step 1: Set PGM ENABLE (pin 1) to V_{ILL}; set V_{CC} (pin 24) to V_{CC3}.
Step 2: Disable all outputs by applying V_{IH} to PGM (pin 13).
Step 3: Disable all inputs by applying V_{IX} to the I inputs.
Step 4: Address the product term to be programmed (0 through 31) by applying its binary code (V_{IH} for a high and V_{IL} for a low) to outputs PA0 through PA4 with PA0 as the least significant bit.

TEXAS INSTRUMENTS
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PROGRAMMING PROCEDURE

Step 5: Lower the voltage on the first input to V_{IH} for a true, or to V_{IL} for the complement.
Step 6: After t_d, raise PGM ENABLE to V_{IHH}.
Step 7: After additional t_d, pulse the PGM input to V_{IH} for t_w.
Step 8: After additional t_d delay, lower PGM ENABLE to V_{ILL}.
Step 9: Disable programmed input by raising it back to V_{IH}.
Step 10: Repeat steps 5 through 9 for each input.
Step 11: Repeat steps 4 through 10 for each product term.

Verify

Step 1: Set PGM ENABLE (pin 1) to V_{ILL}; set V_{CC} (pin 24) to V_{CC3}.
Step 2: Enable PO output by setting PGM to V_{IX}.
Step 3: Disable all inputs by applying V_{IX} to the I inputs.
Step 4: Address the product term to be verified (0 through 31) by applying its binary code on outputs PA0 through PA4.
Step 5: Lower the input voltage on the first input to V_{IH} and check the logic level of output PO, then lower the same input to V_{IL} and again check the level of PO. The input variable state contained in the product term is determined from the following table. Two tests are required to verify the programmed state of each variable.

STATE	I	PO
TRUE	L	L
	H	H
COMPLEMENT	L	H
	H	L
DON'T CARE	L	H
	H	H
INACTIVE	L	L
	H	L

Step 6: Disable verified input by raising it back to V_{IX}.
Step 7: Repeat steps 5 and 6 for all other inputs.
Step 8: Repeat steps 4 through 7 for all other product terms.

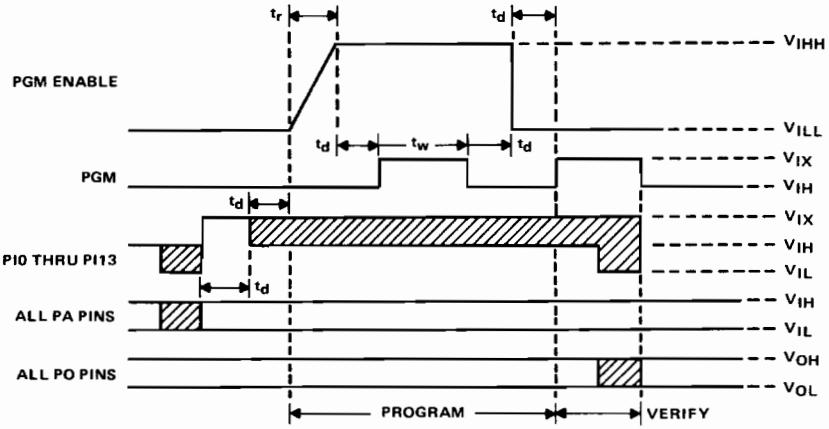


FIGURE 2. AND MATRIX PROGRAMMING WAVEFORMS

PROGRAMMING PROCEDURE

OR MATRIX

Program

Program the output polarity before programming either the AND matrix or the OR matrix. Load all output pins with a 10-kΩ resistor to 5 V and set pin 12 (GND) to 0 V. If the product term is contained in the output function, no fusing is required. Unwanted terms are deleted by programming one at a time, as follows:

Step 1: Set PGM ENABLE (pin 1) to V_{ILL}. Disable the outputs by setting PGM (pin 13) to V_{IH}. Set V_{CC} to V_{CC3}. Set PI6 through PI13 and PA0 through PA5 to V_{IH}.
Step 2: Wait t_d and raise V_{CC} (pin 24) to the program level, V_{CC1}.
Step 3: Use the inputs PA0 through PA5 to address the product term (0 through 31) that is to be removed by applying the corresponding binary code with input PA0 as the least significant bit.
Step 4: Raise the output pin to V_{IX}.
Step 5: Wait t_d, then raise PGM ENABLE to V_{IHH}.
Step 6: Wait t_d, then pulse PGM to V_{IX} for a period of t_p.
Step 7: Wait t_d, then lower PGM ENABLE to V_{ILL}.
Step 8: Wait t_d, then remove V_{IX} from output pin.
Step 9: Repeat steps 4 through 8 for all other output functions.
Step 10: Repeat steps 3 through 9 for all other product terms.
Step 11: Lower V_{CC} to V_{CC3}.

Verify

Step 1: Set PGM ENABLE (pin 1) to V_{ILL}. Disable the outputs by setting PGM (pin 13) to V_{IH}. Set V_{CC} to V_{CC3}. Set PI6 through PI13 and PA0 through PA5 to V_{IH}.
Step 2: Wait t_d and set V_{CC} (pin 24) to the verify level, V_{CC1}.
Step 3: Address the product term to be verified (0 through 31) by applying its binary code to inputs PA0 through PA5.
Step 4: Wait t_d, and set PGM (pin 13) to V_{IL}.
Step 5: Monitor the state of all six outputs (PO0 through PO5) and determine the status of the OR matrix from the following table:

OUTPUT		OR FUSE LINK
ACTIVE HIGH	ACTIVE LOW	
L	H	FUSED
H	L	PRESENT

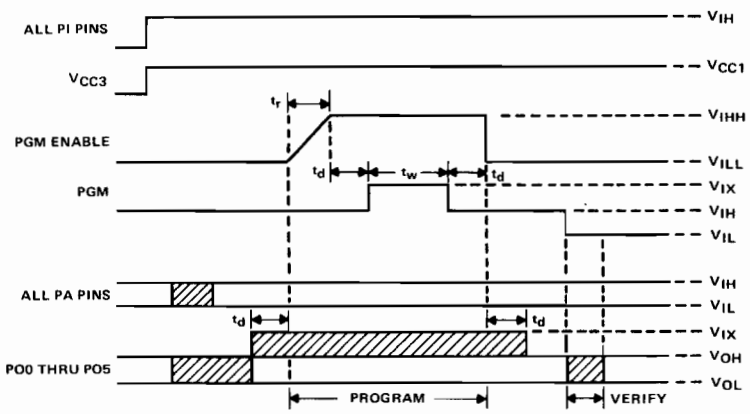


FIGURE 3. OR MATRIX PROGRAMMING WAVEFORMS

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

TIFPLS104, TIFPLS105
16 × 48 × 8 FIELD PROGRAMMABLE LOGIC SEQUENCER

JANUARY 1985

- 50-MHz Clock Rate
- Power-on Preset of All Flip-Flops
- 6-Bit Internal State Register with 8-Bit Output Register
- Power Dissipation . . . 650 mW Typical
- Programmable Asynchronous Preset or Output Control
- Functionally Equivalent to, but Faster than 82S104A and 82S105A

description

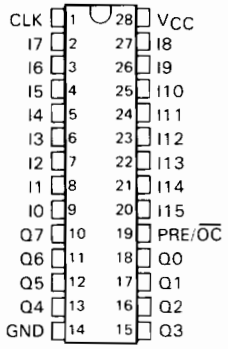
The TIFPLS104 (open collector outputs) and the TIFPLS105 (3-state outputs) are TTL field-programmable state machines of the Mealy type. These state machines (logic sequencers) contains 48 product terms (AND terms) and 14 pairs of sum terms (OR terms). The product and sum terms are used to control the 6-bit internal state register and the 8-bit output register.

The outputs of the internal state register (P0-P5) are fed back and combined with the 16 inputs (I0-I15) to form the AND array. In addition a single sum term is complemented and fed back to the AND array which allows any of the product terms to be summed, complemented and used as inputs to the AND array.

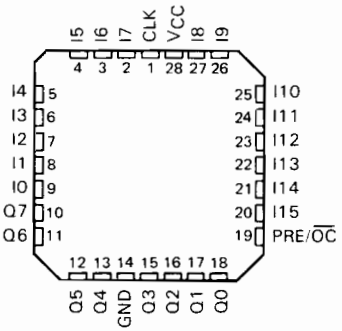
The state and output registers are positive-edge triggered S/R flip-flops. These registers are unconditionally preset to logical 1 on power-up. Pin 19 can be used to preset both registers or by blowing the proper fuse be converted to an output control function.

The TIFPLS104M and TIFPLS105M devices are characterized for operation over the full military temperature range of −55°C to 125°C. The TIFPLS104C and TIFPLS105C devices are characterized for operation from 0°C to 70°C.

TIFPLS104, TIFPLS105
M SUFFIX . . . JD PACKAGE
C SUFFIX . . . JD OR N PACKAGE
(TOP VIEW)



TIFPLS104, TIFPLS105
M SUFFIX . . . FK PACKAGE
C SUFFIX . . . FK OR FN PACKAGE
(TOP VIEW)



3

Field-Programmable Logic

PRODUCT PREVIEW
This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

TEXAS INSTRUMENTS
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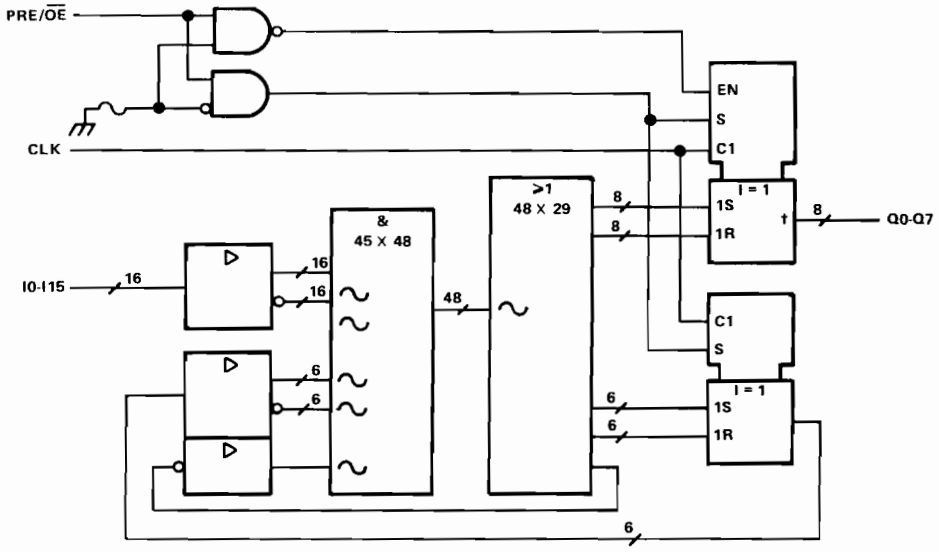
functional block diagram (positive logic)



~denotes fused inputs.
†TIFPLS104 has open collector (Ω) outputs; TIFPLS105 has 3-state (▽) outputs.

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

TIFPLS167
14 × 48 × 6 FIELD PROGRAMMABLE LOGIC SEQUENCER

JANUARY 1985

- **Programmable Asynchronous Preset or Output Control**
- **Power-on Preset of All Flip-Flops**
- **8-Bit Internal State Register with 4-Bit Output Register**
- **Power Dissipation . . . 650 mW Typical**
- **Functionally Equivalent to, but Faster than 82S167A**

description

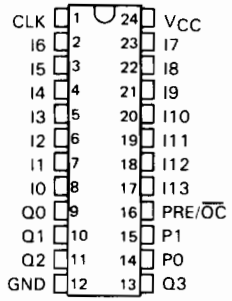
The TIFPLS167 is a TTL field-programmable state machine of the Mealy type. This state machine (logic sequencer) contains 48 product terms (AND terms) and 12 pairs of sum terms (OR terms). The product and sum terms are used to control the 8-bit internal state register and the 4-bit output register.

The outputs of the internal state register (P0-P7) are fed back and combined with the 14 inputs (I0-I13) to form the AND array. In addition the first two bits of the internal state register (P0-P1) are brought off-chip to allow the output register to be extended to 6 bits if desired. A single sum term is complemented and fed back to the AND array which allows any of the product terms to be summed, complemented and used as inputs to the AND array.

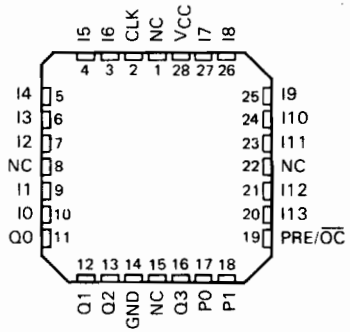
The state and output registers are positive-edge triggered S/R flip-flops. These registers are unconditionally preset to logical 1 on power-up. Pin 19 can be used to preset both registers or by blowing the proper fuse be converted to an output control function.

The TIFPLS167M is characterized for operation over the full military temperature range of −55°C to 125°C. The TIFPLS167C is characterized for operation from 0°C to 70°C.

M SUFFIX . . . JT PACKAGE
C SUFFIX . . . JT OR NT PACKAGE
(TOP VIEW)



M SUFFIX . . . FK PACKAGE
C SUFFIX . . . FK OR FN PACKAGE
(TOP VIEW)

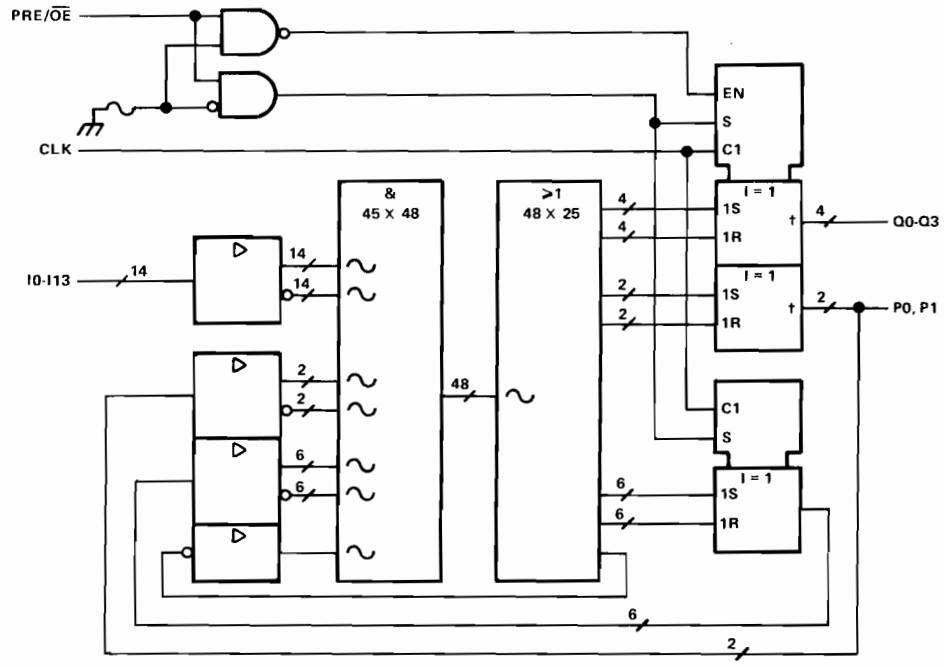


3

Field-Programmable Logic

PRODUCT PREVIEW
This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

functional block diagram (positive logic)



†Optional fuse-programmable 3-state (▽) outputs
∼ denotes fused inputs

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

82S104A, 82S105A
16 × 48 × 8 FIELD PROGRAMMABLE LOGIC SEQUENCER

JANUARY 1985

- Programmable Asynchronous Preset or Output Control
- Power-on Preset of All Flip-Flops
- 6-Bit Internal State Register with 8-Bit Output Register
- Power Dissipation . . . 650 mW Typical
- Functionally Equivalent to Signetics 82S104A/82S105A

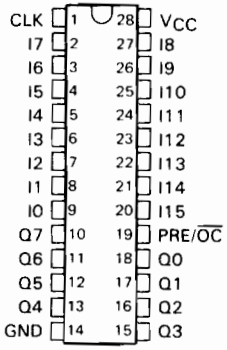
description

The 82S104A (open collector outputs) and the 82S105A (3-state outputs) are TTL field-programmable state machines of the Mealy type. These state machines (logic sequencers) contain 48 product terms (AND terms) and 14 pairs of sum terms (OR terms). The product and sum terms are used to control the 6-bit internal state register and the 8-bit output register.

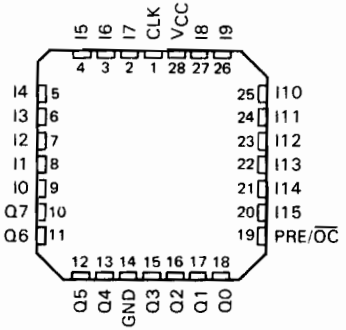
The outputs of the internal state registers (P0-P5) are fed back and combined with the 16 inputs (I0-I15) to form the AND array. In addition a single sum term is complemented and fed back to the AND array which allows any of the product terms to be summed, complemented and used as inputs to the AND array.

The state and output registers are positive-edge triggered S/R flip-flops. These registers are unconditionally preset to logical 1 on power-up. Pin 19 can be used to preset both registers or by blowing the proper fuse be converted to an Output Control function.

82S104A, 82S105A
M SUFFIX . . . JD PACKAGE
C SUFFIX . . . JD OR N PACKAGE
(TOP VIEW)



82S104A, 82S105A
M SUFFIX . . . FK PACKAGE
C SUFFIX . . . FK OR FN PACKAGE
(TOP VIEW)



3

Field-Programmable Logic

185

PRODUCT PREVIEW
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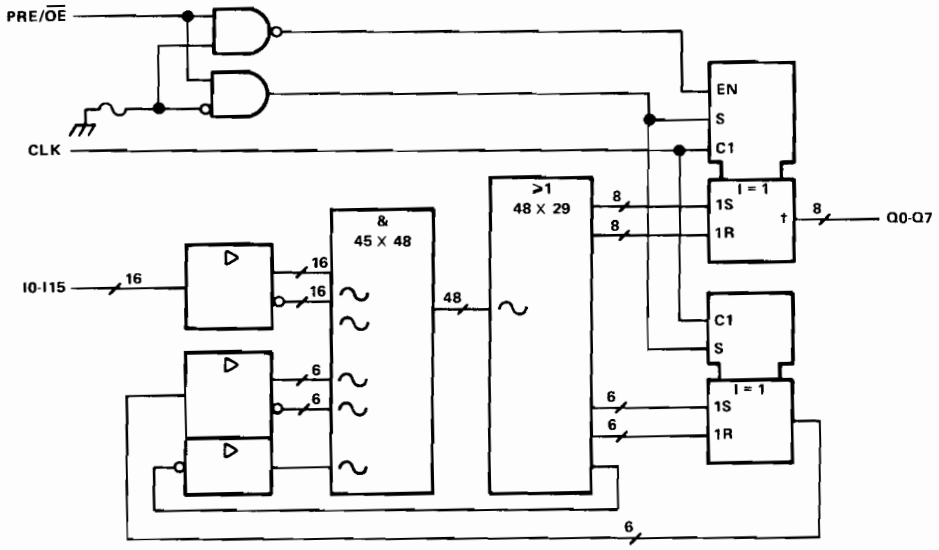
functional block diagram (positive logic)



~denotes fused inputs.
†82S104A has open collector (⏀) outputs, 82S105A has 3-state (▽) outputs.

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

82S167A
14 × 48 × 6 FIELD PROGRAMMABLE LOGIC SEQUENCER

JANUARY 1985

- **Programmable Asynchronous Preset or Output Control**
- **Power-on Preset of All Flip-Flops**
- **8-Bit Internal State Register with 4-Bit Output Register**
- **Power Dissipation . . . 650 mW Typical**
- **Functionally Equivalent to Signetics 82S167A**

description

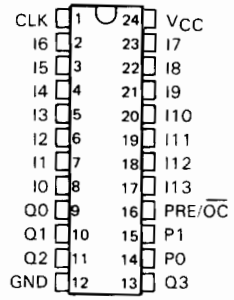
The 82S167A is a TTL field-programmable state machine of the Mealy type. This state machine (logic sequencer) contains 48 product terms (AND terms) and 12 pairs of sum terms (OR terms). The product and sum terms are used to control the 8-bit internal state register and the 4-bit output register.

The outputs of the internal state register (P0-P7) are fed back and combined with the 14 inputs (I0-I13) to form the AND array. In addition the first two bits of the internal state register (P0-P1) are brought off-chip to allow the output register to be extended to 6 bits if desired. A single sum term is complemented and fed back to the AND array which allows any of the product terms to be summed, complemented and used as inputs to the AND array.

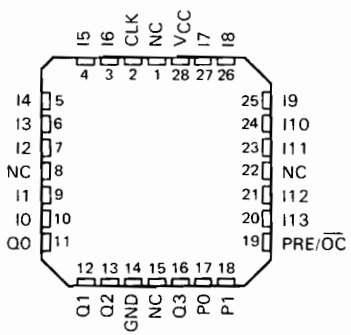
The state and output registers are positive-edge triggered S/R flip-flops. These registers are unconditionally preset to logical 1 on power-up. Pin 19 can be used to preset both registers or by blowing the proper fuse be converted to an output control function.

The 82S167AM is characterized for operation over the full military temperature range of −55°C to 125°C. The 82S167AC is characterized for operation from 0°C to 70°C.

M SUFFIX . . . JT PACKAGE
C SUFFIX . . . JT OR NT PACKAGE
(TOP VIEW)



M SUFFIX . . . FK PACKAGE
C SUFFIX . . . FK OR FN PACKAGE
(TOP VIEW)



3

Field-Programmable Logic

PRODUCT PREVIEW
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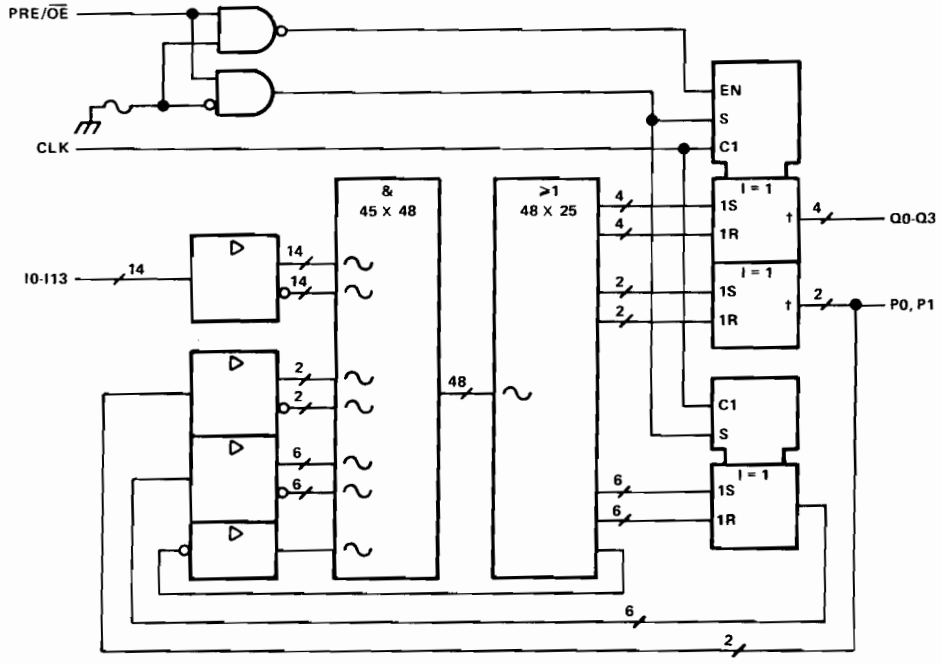
functional block diagram (positive logic)



†Optional fuse-programmable 3-state (▽) outputs
∼ denotes fused inputs

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

General Information 1

Functional Index 2

Field-Programmable Logic 3

PROMs 4

RAMs and Memory-Based Code Converters 5

Designing with Texas Instruments Field-Programmable Logic 6

Mechanical Data 7

BIPOLAR PROM CROSS-REFERENCE GUIDE

DEVICE	MANUFACTURER	TI
27S18	AMD	TBP18SA030
27S18A	AMD	TBP38SA030
27S19	AMD	TBP18S030
27S19A	AMD	TBP38S030
27S20	AMD	TBP24SA10
27S21	AMD	TBP24S10
27S28	AMD	TBP28SA42
27S29	AMD	TBP28S42
27S30	AMD	TBP28SA46
27S31	AMD	TBP28S46
27S32	AMD	TBP24SA41
27S33	AMD	TBP24S41
27S180	AMD	TBP28SA86A
27S181	AMD	TBP28S86A
27S184	AMD	TBP24SA81
27S185	AMD	TBP24S81
27S191	AMD	TBP38S166-45
27S191A	AMD	TBP38L166-35
3601	INTEL	TBP24SA10
3604	INTEL	TBP28SA46
3605	INTEL	TBP24SA41
3608	INTEL	TBP28SA86A
3621	INTEL	TBP24S10
3624	INTEL	TBP28S46
3625	INTEL	TBP24S41
3628	INTEL	TBP28S86A
3636	INTEL	TBP28S166
6300-1	MMI	TBP24SA10
6301-1	MMI	TBP24S10
6308-1	MMI	TBP28LA22
6309-1	MMI	TBP28L22
6330-1	MMI	TBP18SA030
6331-1	MMI	TBP18S030
6340-1	MMI	TBP28SA46
6341-1	MMI	TBP28S46
6348-1	MMI	TBP28SA42
6349-1	MMI	TBP28S42
6352-1	MMI	TBP24SA41
6353-1	MMI	TBP24S41
6380-1	MMI	TBP28SA86A
6381-1	MMI	TBP28S86A
6388-1	MMI	TBP24SA81
6389-1	MMI	TBP24S81
63S081	MMI	TBP38S030
63S1681	MMI	TBP28S166
63S1681A	MMI	TBP38L166-35
7117	FUJITSU	TBP28LA22
7118	FUJITSU	TBP28L22
7121	FUJITSU	TBP24SA41
7122	FUJITSU	TBP24S41
7123	FUJITSU	TBP28SA42
7124	FUJITSU	TBP28S42
7127	FUJITSU	TBP24SA81
7128	FUJITSU	TBP24S81
7131	FUJITSU	TBP28SA86A
7132	FUJITSU	TBP28S86A
7138	FUJITSU	TBP28S166
74S188	NATIONAL	TBP18SA030
74S287	NATIONAL	TBP24S10
74S288	NATIONAL	TBP18S030
74S387	NATIONAL	TBP24SA10
74S470	NATIONAL	TBP28LA22
74S471	NATIONAL	TBP28L22
74S472	NATIONAL	TBP28S42
74S473	NATIONAL	TBP28SA42
74S474	NATIONAL	TBP28S46
74S475	NATIONAL	TBP28SA46
74S572	NATIONAL	TBP24SA41
74S573	NATIONAL	TBP24S41
7602	HARRIS	TBP18SA030
7603	HARRIS	TBP18S030
7608	HARRIS	TBP28S2708A
7610	HARRIS	TBP24SA10
7611	HARRIS	TBP24S10
76161	HARRIS	TBP28S166
76161	MOTOROLA	TBP28S166
7640	HARRIS	TBP28SA46
7640	MOTOROLA	TBP28SA46
7641	HARRIS	TBP28S46
7641	MOTOROLA	TBP28S46
7642	HARRIS	TBP24SA41
7642	MOTOROLA	TBP24SA41
7643	HARRIS	TBP24S41
7643	MOTOROLA	TBP24S41
7648	HARRIS	TBP28SA42
7649	HARRIS	TBP28S42
7680	MOTOROLA	TBP28SA86A
7680	HARRIS	TBP28SA86A
7681	HARRIS	TBP28S86A
7681	MOTOROLA	TBP28S86A
7684	HARRIS	TBP24SA81
7684	MOTOROLA	TBP24SA81
7685	HARRIS	TBP24S81
7685	MOTOROLA	TBP24S81
82S23	SIGNETICS	TBP18SA030
82S23A	SIGNETICS	TBP38SA030
82S123	SIGNETICS	TBP18S030
82S123A	SIGNETICS	TBP38S030

BIPOLAR PROM CROSS-REFERENCE GUIDE

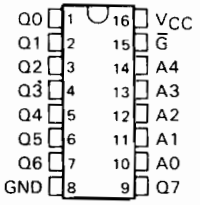
DEVICE	MANUFACTURER	TI
82S126	SIGNETICS	TBP24SA10
82S129	SIGNETICS	TBP24S10
82S136	SIGNETICS	TBP24SA41
82S137	SIGNETICS	TBP24S41
82S140	SIGNETICS	TBP28SA46
82S141	SIGNETICS	TBP28S46
82S146	SIGNETICS	TBP28SA42
82S147	SIGNETICS	TBP28S42
82S180	SIGNETICS	TBP28SA86A
82S181	SIGNETICS	TBP28S86A
82LS181	SIGNETICS	TBP28L86A
82S184	SIGNETICS	TBP24SA81
82S185	SIGNETICS	TBP24S81
82S191	SIGNETICS	TBP28S166
82S191B	SIGNETICS	TBP38L166-45
82S2708	SIGNETICS	TBP28S2708A
87S180	NATIONAL	TBP28SA86A
87S181	NATIONAL	TBP28S86A
87S184	NATIONAL	TBP24SA81
87S185	NATIONAL	TBP24S81
87S191	NATIONAL	TBP28S166
87S191A	NATIONAL	TBP38S166-45
87S191B	NATIONAL	TBP38S166-35
93417	FAIRCHILD	TBP24SA10
93427	FAIRCHILD	TBP24S10
93438	FAIRCHILD	TBP28SA46
93448	FAIRCHILD	TBP28S46
93450	FAIRCHILD	TBP28SA86A
93451	FAIRCHILD	TBP28S86A
93452	FAIRCHILD	TBP24SA41
93453	FAIRCHILD	TBP24S41
93511	FAIRCHILD	TBP28S166
93511C	FAIRCHILD	TBP38L166-45
93514	FAIRCHILD	TBP24SA81
93515	FAIRCHILD	TBP24S81

TBP18S030, TBP18SA030
256 BITS (32 WORDS BY 8 BITS)
PROGRAMMABLE READ-ONLY MEMORIES

SEPTEMBER 1979 – REVISED AUGUST 1984

- **Titanium-Tungsten (Ti-W) Fuse Link for Reliable Low-Voltage Full Family Compatible Programming**
- **Full Decoding and Fast Chip Select Simplify System Design**
- **P-N-P Inputs for Reduced Loading on System Buffers/Drivers**
- **Applications Include:**
  Microprogramming/Firmware Loaders
  Code Converters/Character Generators
  Translators/Emulators
  Address Mapping/Look-Up Tables
- **Choice of 3-State or Open-Collector Outputs**

TBP18SA030, TBP18S030 . . . J OR N PACKAGE
(TOP VIEW)



description

These monolithic TTL programmable read-only memories (PROMs) feature titanium-tungsten (Ti-W) fuse links with each link designed to program in 20 microseconds. The Schottky-clamped versions of these PROMs offer considerable flexibility for upgrading existing designs or improving new designs as they feature full Schottky clamping for improved performance, low-current MOS-compatible p-n-p inputs, choice of bus-driving three-state or open-collector outputs, and improved chip-select access times.

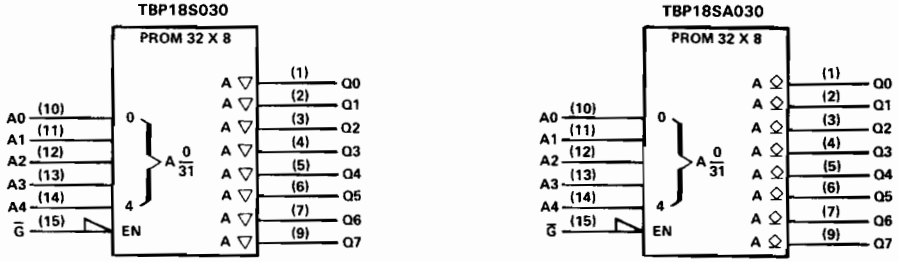
Data can be electronically programmed, as desired, at any bit location in accordance with the programming procedure specified. All PROMs are supplied with a low-logic level output condition stored at each bit location. The programming procedure open-circuits Ti-W metal links, which reverses the stored logic level at selected locations. The procedure is irreversible; once altered, the output for that bit location is permanently programmed. Outputs that have never been altered may later be programmed to supply the opposite output level. Operation of the unit within the recommended operating conditions will not alter the memory content.

A low level at the chip-select input(s) enables each PROM. The opposite level at any chip-select input causes the outputs to be off.

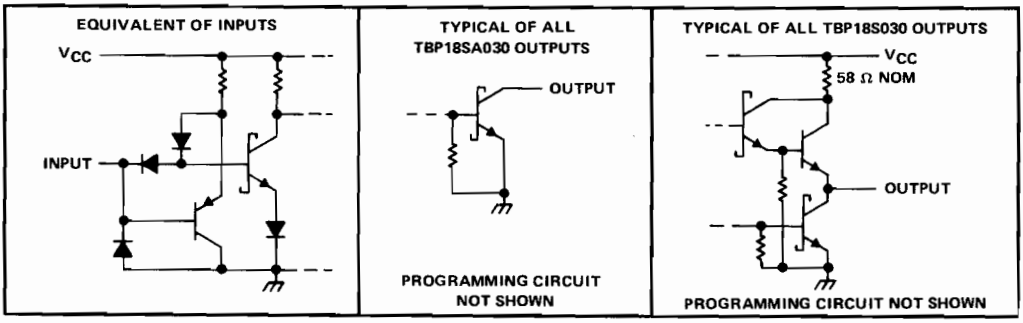
The three-state output offers the convenience of an open-collector with the speed of a totem-pole output; it can be bus-connected to other similar outputs yet it retains the fast rise time characteristic of the TTL totem-pole output. The open-collector output offers the capability of direct interface with a data line having a passive pull up.

A MJ suffix designates full-temperature circuits (formerly 54 Family) and are characterized for operation over the full military temperature range of −55°C to 125°C. A J or N suffix designates commercial-temperature circuits (formerly 74 Family) and are characterized for operation from 0°C to 70°C.

logic symbol



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage (see Note 1) 7V
Input voltage 5.5V
Off-state output voltage 5.5V
Operating free-air temperature range: Full-temperature-range circuits ..... −55°C to 125°C
Commercial-temperature-range circuits ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

recommended conditions for programming TBP18S', TBP18SA PROMs

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC} (see Note 1)	Steady state	4.75	5	5.25	V
	Program pulse	9	9.25	9.5	
Input voltage	High level, V_{IH}	2.4		5	V
	Low level, V_{IL}	0		0.5	
Termination of all outputs except the one to be programmed		See load circuit (Figure 1)			
Voltage applied to output to be programmed, $V_{O(pr)}$ (see Note 2)		0	0.25	0.3	V
Duration of V_{CC} programming pulse X (see Figure 2 and Note 3)		15	25	100	μs
Programming duty cycle for Y pulse			25	35	%
Free-air temperature		20	25	30	°C

NOTES: 1. Voltage values are with respect to network ground terminal. The supply voltage rating does not apply during programming.
2. The TBP18S030, TBP18SA030 are supplied with all bit locations containing a low logic level, and programming a bit changes the output of the bit to high logic level.
3. Programming is guaranteed if the pulse applied is 98 μs in duration.

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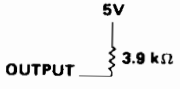
programming procedure

1. Apply steady-state supply voltage (V_{CC} = 5 V) and address the word to be programmed.
2. Verify that the bit location needs to be programmed. If not, proceed to the next bit.
3. If the bit requires programming, disable the outputs by applying a high-logic level voltage to the chip-select input(s).
4. Only one bit location is programmed at a time. Connect each output not being programmed to 5 V through 3.9 kΩ and apply the voltage specified in the table to the output to be programmed. Maximum current into the programmer output is 150 mA.
5. Step V_{CC} to 9.25 nominal. Maximum supply current required during programming is 750 mA.
6. Apply a low-logic-level voltage to the chip-select input(s). This should occur between 1 μs and 1 ms after V_{CC} has reached its 9.25 level. See programming sequence of Figure 2.
7. After the X pulse time is reached, a high logic level is applied to the chip-select inputs to disable the outputs.
8. Within the range of 1 μs to 1 ms after the chip-select input(s) reach a high logic level, V_{CC} should be stepped down to 5 V at which level verification can be accomplished.
9. The chip-select input(s) may be taken to a low logic level (to permit program verification) 1 μs or more after V_{CC} reaches its steady-state value of 5 V.
10. At a Y pulse duty cycle of 35% or less, repeat steps 1 through 8 for each output where it is desired to program a bit.
11. Verify accurate programming of every word after all words have been programmed using V_{CC} values of 4.5 and 5.5 volts.



LOAD CIRCUIT FOR EACH OUTPUT NOT BEING PROGRAMMED OR FOR PROGRAM VERIFICATION

FIGURE 1 – LOAD CIRCUIT

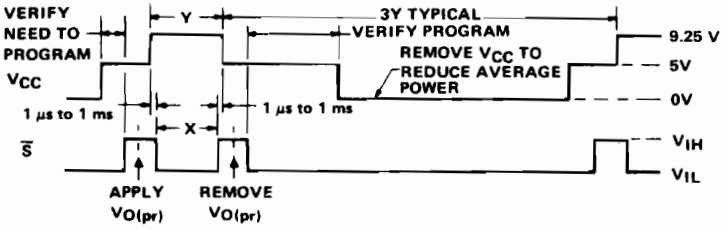


FIGURE 2 – VOLTAGE WAVEFORMS FOR PROGRAMMING

recommended operating conditions (see Note 4)

PARAMETER		TBP18S030			UNIT
		MIN	NOM	MAX	
Supply voltage, V_{CC}	MJ	4.5	5	5.5	V
	J, N	4.75	5	5.25	
High-level output current, I_{OH}	MJ			−2	mA
	J,N			−6.5	
Low-level output current, I_{OL}				20	mA
Operating free-air temperature, T_A	MJ	−55		125	°C
	J ,N	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Note 4)

PARAMETER		TEST CONDITIONS†	FULL TEMP (MJ)			COMM. TEMP (J,N)			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA			−1.2			−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = MAX	2.4	3.4		2.4	3.2		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = MAX			0.5			0.5	V
I_{OZH}	Off-state output current, high-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V, V_O = 2.4 V			50			50	μA
I_{OZL}	Off-state output current, low-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V, V_O = 0.5 V			−50			−50	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V,			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V			25			25	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5 V			−0.25			−0.25	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX,	−30		−100	−30		−100	mA
I_{CC}	Supply current	V_{CC} = MAX, Chip select(s) at 0 V, Outputs open, See Note 5		80	110		80	110	mA

switching characteristics over recommended ranges of T_A and V_{CC} (unless otherwise noted)

TYPE	TEST CONDITIONS	$t_{a(A)}$ ACCESS TIME FROM ADDRESS			$t_{a(S)}$ ACCESS TIME FROM CHIP SELECT (ENABLE TIME)			t_{dis} DISABLE TIME FROM HIGH OR LOW LEVEL			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
TBP18S030MJ	C_L = 30 pF for $t_{a(A)}$ and $t_{a(S)}$, 5 pF for t_{dis}, See Note 6		25	50		12	30		8	30	ns
TBP18S030			25	40		12	25		8	20	ns

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

NOTES: 4. MJ designates full-temperature circuits (formerly 54 Family), J and N designate commercial-temperature circuits (formerly 74 Family).
5. The typical values of I_{CC} are with all outputs low.
6. Load circuits and voltage waveforms are shown in Section 1.

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recommended operating conditions (see Note 4)

PARAMETER		TBP18SA030 MIN	TBP18SA030 NOM	TBP18SA030 MAX	UNIT
Supply voltage, V_{CC}	MJ	4.5	5	5.5	V
	J, N	4.75	5	5.25	
High-level output voltage, V_{OH}				5.5	V
Low-level output current, I_{OL}				20	mA
Operating free-air temperature, T_A	MJ	−55		125	°C
	J, N	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −18mA			−1.2	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V	V_{OH} = 2.4 V			50	μA
			V_{OH} = 5.5 V			100	
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = MAX			0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7 V			25	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.5 V			−0.25	mA
I_{CC}	Supply current	V_{CC} = MAX, Chip select(s) at 0 V, Outputs open, See Note 5			80	110	mA

switching characteristics over recommended ranges of T_A and V_{CC} (unless otherwise noted)

TYPE	TEST CONDITIONS	$t_{(A)}$ ACCESS TIME FROM ADDRESS MIN	TYP‡	MAX	$t_{a(S)}$ ACCESS TIME FROM CHIP SELECT (ENABLE TIME) MIN	TYP‡	MAX	t_{PLH} PROPAGATION DELAY TIME, LOW-TO-HIGH-LEVEL OUTPUT FROM CHIP SELECT (DISABLE TIME) MIN	TYP‡	MAX	UNIT
TBP18SA030MJ	C_L = 30pF, R_{L1} = 300 Ω,		25	50		12	30		12	30	ns
TBP18SA030	R_{L2} = 600 Ω, See Note 6		25	40		12	25		12	25	ns

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTES: 4. MJ designates full-temperature circuits (formerly 54 Family), J and N designate commercial-temperature circuits (formerly 74 Family).
5. The typical values of I_{CC} are with all outputs low.
6. Load circuits and voltage waveforms are shown in Section 1.

SERIES 24 AND 28
STANDARD AND LOW POWER PROGRAMMABLE READ-ONLY MEMORIES

SEPTEMBER 1979 – REVISED AUGUST 1984

- **Expanded Family of Standard and Low Power PROMs**
- **Titanium-Tungsten (Ti-W) Fuse Links for Reliable Low-Voltage Full-Family-Compatible Programming**
- **Full Decoding and Fast Chip Select Simplify System Design**
- **P-N-P Inputs for Reduced Loading On System Buffers/Drivers**
- **Each PROM Supplied With a High Logic Level Stored at Each Bit Location**
- **Applications Include:**
  Microprogramming/Firmware Loaders
  Code Converters/Character Generators
  Translators/Emulators
  Address Mapping/Look-Up Tables

description

The 24 and 28 Series of monolithic TTL programmable read-only memories (PROMs) feature an expanded selection of standard and low-power PROMs. This expanded PROM family provides the system designer with considerable flexibility in upgrading existing designs or optimizing new designs. Featuring proven titanium-tungsten (Ti-W) fuse links with low-current MOS-compatible p-n-p inputs, all family members utilize a common programming technique designed to program each link with a 20-microsecond pulse.

The 4096-bit and 8192-bit PROMs are offered in a wide variety of packages ranging from 18-pin 300 mil-wide thru 24 pin 600 mil-wide. The 16,384-bit PROMs provide twice the bit density of the 8192-bit PROMs and are provided in a 24 pin 600 mil-wide package.

All PROMs are supplied with a logic-high output level stored at each bit location. The programming procedure will produce open-circuits in the Ti-W metal links, which reverses the stored logic level at the selected location. The procedure is irreversible; once altered, the output for that bit location is permanently programmed. Outputs that have never been altered may later be programmed to supply the opposite output level. Operation of the unit within the recommended operating conditions will not alter the memory content.

Active level(s) at the chip-select input(s) (S or $\overline{S}$) enables all of the outputs. An inactive level at any chip-select input causes all outputs to be in the three-state, or off condition.

4

PROMs

standard PROMs

The standard PROM members of Series 24 and 28 offer high performance for applications which require the uncompromised speed of Schottky technology. The fast chip-select access times allow additional decoding delays to occur without degrading speed performance.

TYPE NUMBER	PACKAGE† AND TEMPERATURE RANGE DESIGNATORS	OUTPUT CONFIGURATION‡	BIT SIZE (ORGANIZATION)	TYPICAL PERFORMANCE		
				ACCESS TIMES		POWER DISSIPATION
				ADDRESS	SELECT	
TBP24S10	MJ, J, N	▽	1024 Bits (256W × 4B)	35 ns	20 ns	375 mW
TBP24SA10	MJ, J, N	Ω				
TBP28S42	MJ, J, N	▽	4096 Bits (512W × 8B)	35 ns	20 ns	500 mW
TBP28SA42	MJ, J, N	Ω				
TBP28S46	MJW, JW, NW	▽				
TBP28SA46	MJW, JW, NW	Ω				
TBP24S41	MJ, J, N	▽	4096 Bits (1024 × 4B)	40 ns	20 ns	475 mW
TBP24SA41	MJ, J, N	Ω				
TBP24S81	MJ, J, N	▽	8192 Bits (2048 × 4B)	45 ns	20 ns	625 mW
TBP24SA81	MJ, J, N	Ω				
TBP28S86A	MJW, JW, NW	▽	8192 Bits (1024 × 8B)	45 ns	20 ns	625 mW
TBP28SA86A	MJW, JW, NW	Ω				
TBP28S2708A	NW	▽				
TBP28S166	NW	▽	16,384 Bits (2048W × 8B)	35 ns	15 ns	650 mW

†MJ and MJW designates full-temperature-range circuits (formerly 54 Family), J, JW, N, and NW designates commercial-temperature-range circuits (formerly 74 Family).

‡ ▽ = three state, Ω = open collector.

884

low power PROMs

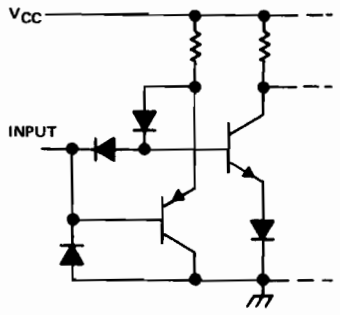
To upgrade systems utilizing MOS EPROMs or MOS PROMs, or when designing new systems which do not require maximum speed, the low-power PROM family offers the output drive and speed performance of bipolar technology, plus reduced power dissipation.

TYPE NUMBER	PACKAGE† AND TEMPERATURE RANGE DESIGNATORS	OUTPUT CONFIGURATION‡	BIT SIZE (ORGANIZATION)	TYPICAL PERFORMANCE		
				ACCESS TIMES		POWER DISSIPATION
				ADDRESS	SELECT	
TBP28L22	MJ, J,N	▽	2048 Bits (256W × 8B)	45 ns	20 ns	375 mW
TBP28LA22	MJ, J, N	◇				
TBP28L42	MJ, J, N	▽	4096 Bits (512W × 8B)	60 ns	30 ns	250 mW
TBP28L46	MJW, JW, NW	▽				
TBP28L86A	MJW, JW, NW	▽	8192 Bits (1024W × 8B)	80 ns	35 ns	350 mW
TBP28L166	NW	▽	16,384 Bits (2084W × 8B)	65 ns	30 ns	350 mW

†MJ and MJW designates full-temperature-range circuits (formerly 54 Family), J, JW, N, and NW designates commercial-temperature-range circuits (formerly 74 Family).
‡ ▽ = three state, ◇ = open collector.

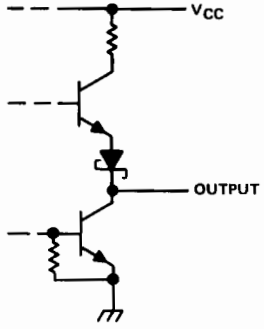
schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



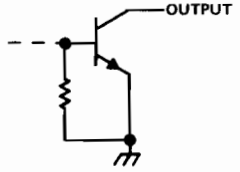
Programming circuit not shown

EQUIVALENT OF 3-STATE OUTPUTS



Programming circuits not shown

EQUIVALENT OF OPEN-COLLECTOR OUTPUTS



Programming circuit not shown

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Chip-select peak input voltage (S, S1, S2) (see Note 2) . . . . . 11 V
Off-state output voltage . . . . . 5.5 V
Off-state peak output voltage (see Note 2) . . . . . 16.25 V
Operating free-air temperature range: Full-temperature-range circuits (M suffix) . . −55°C to 125°C
Commercial-temperature-range circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. These ratings apply only under the conditions described in the programming procedure.

TEXAS INSTRUMENTS
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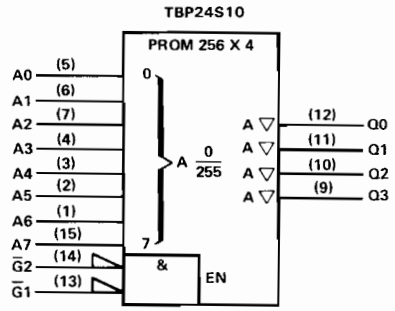
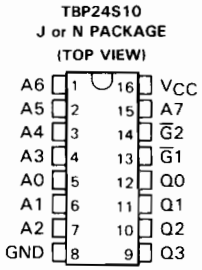
logic symbol



pin assignment



recommended operating conditions

PARAMETER		MJ			J OR N			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−2			−6.5	mA
I_{OL}	Low-level output current			16			16	mA
T_A	Operating free-air temperature range	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		MJ			J OR N			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = MIN,	I_{OH} = MAX	2.4	3.1		2.4	3.1		V
V_{OL}	V_{CC} = MIN,	I_{OL} = 16 mA			0.5			0.5	V
I_{OZH}	V_{CC} = MAX,	V_O = 2.4 V			50			50	μA
I_{OZL}	V_{CC} = MAX,	V_O = 0.5 V			−50			−50	μA
I_I	V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.7 V			25			25	μA
I_{IL}	V_{CC} = MAX,	V_I = 0.5 V			−0.25			−0.25	mA
I_{OS}§	V_{CC} = MAX		−30		−100	−30		−100	mA
I_{CC}	V_{CC} = MAX			75	100		75	100	mA

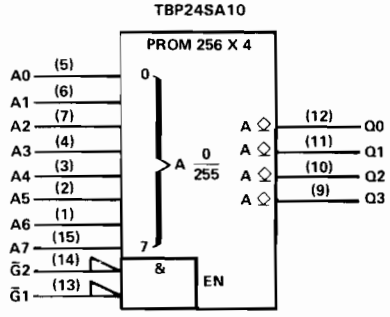
switching characteristics over recommended ranges of T_A and V_{CC} (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MJ			J OR N			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
$t_{a(A)}$	Access time from address	C_L = 30 pF		35	75		35	55	ns
$t_{a(S)}$	Access time from chip select (enable time)	See Note 3		20	40		20	35	ns
t_{dis}	Disable time	C_L = 5 pF See Note 3		15	40		15	35	ns

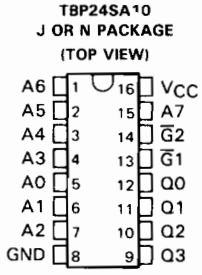
†For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.
NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

TBP24SA10
1024 BITS (256 WORDS BY 4 BITS)
STANDARD PROGRAMMABLE READ-ONLY MEMORIES WITH OPEN-COLLECTOR OUTPUTS

logic symbol



pin assignment



recommended operating conditions

PARAMETER		MJ			J OR N			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			16			16	mA
T_A	Operating free-air temperature range	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		MJ			J OR N			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN,	I_I = −18 mA			−1.2			−1.2	V
I_{OH}	V_{CC} = MIN,	V_{OH} = 2.4 V			0.05			0.05	mA
		V_{OH} = 5.5 V			0.1			0.1	
V_{OL}	V_{CC} = MIN,	I_{OL} = 16 mA			0.5			0.45	V
I_I	V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.7 V			25			25	μA
I_{IL}	V_{CC} = MAX,	V_I = 0.5 V			−0.25			−0.25	mA
I_{CC}	V_{CC} = MAX			75	100		75	100	mA

switching characteristics over recommended ranges of T_A and V_{CC} (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MJ			J OR N			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
$t_{a(A)}$	Access time from address	C_L = 30 pF		35	75		35	65	ns
$t_{a(S)}$	Access time from chip select (enable time)	R_{L1} = 300 Ω		20	40		20	35	ns
t_{PLH}	Propagation delay time low-to-high-level output from chip select	R_{L2} = 600 Ω See Note 3		15	40		20	35	ns

†For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

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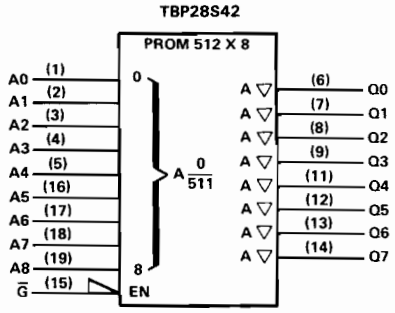
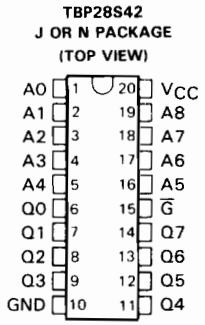
logic symbol



pin assignment



recommended operating conditions

PARAMETER		MJ			J OR N			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−2			−6.5	mA
I_{OL}	Low-level output current			16			16	mA
T_A	Operating free-air temperature range	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		MJ			J OR N			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = MIN,	I_{OH} = MAX	2.4	3.1		2.4	3.1		V
V_{OL}	V_{CC} = MIN,	I_{OL} = 16 mA			0.5			0.5	V
I_{OZH}	V_{CC} = MAX,	V_O = 2.4 V			50			50	μA
I_{OZL}	V_{CC} = MAX,	V_O = 0.5 V			−50			−50	μA
I_I	V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.7 V			25			25	μA
I_{IL}	V_{CC} = MAX,	V_I = 0.5 V			−0.25			−0.25	mA
I_{OS}§	V_{CC} = MAX		−30		−100	−30		−100	mA
I_{CC}	V_{CC} = MAX			100	135		100	135	mA

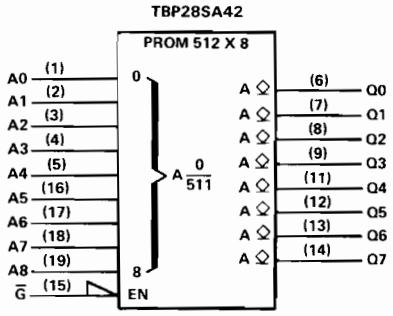
switching characteristics over recommended ranges of T_A and V_{CC} (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MJ			J OR N			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
$t_{a(A)}$	Access time from address	C_L = 30 pF		35	70		35	60	ns
$t_{a(S)}$	Access time from chip select (enable time)	See Note 3		20	45		20	45	ns
t_{dis}	Disable time	C_L = 5 pF See Note 3		15	45		15	40	ns

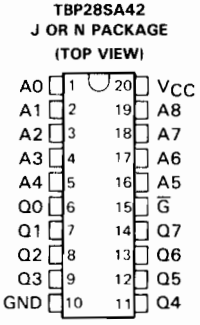
†For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.
NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

TBP28SA42
4096 BITS (512 WORDS BY 8 BITS)
STANDARD PROGRAMMABLE READ-ONLY MEMORIES WITH OPEN-COLLECTOR OUTPUTS

logic symbol



pin assignment



recommended operating conditions

PARAMETER		MJ			J OR N			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			16			16	mA
T_A	Operating free-air temperature range	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		MJ			J OR N			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN,	I_I = −18 mA			−1.2			−1.2	V
I_{OH}	V_{CC} = MIN,	V_{OH} = 2.4 V			0.05			0.05	mA
		V_{OH} = 5.5 V			0.1			0.1	
V_{OL}	V_{CC} = MIN,	I_{OL} = 16 mA			0.5			0.5	V
I_I	V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.7 V			25			25	μA
I_{IL}	V_{CC} = MAX,	V_I = 0.5 V			−0.25			−0.25	mA
I_{CC}	V_{CC} = MAX			105	135		105	135	mA

switching characteristics over recommended ranges of T_A and V_{CC} (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MJ			J OR N			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
$t_{a(A)}$	Access time from address	C_L = 30 pF		35	75		35	65	ns
$t_{a(S)}$	Access time from chip select (enable time)	R_{L1} = 300 Ω		20	45		20	35	ns
t_{PLH}	Propagation delay time low-to-high-level output from chip select	R_{L2} = 600 Ω See Note 3		15	45		15	35	ns

†For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

TEXAS INSTRUMENTS
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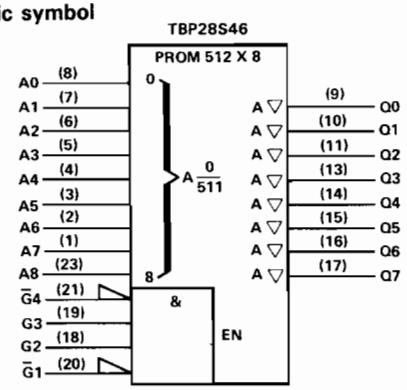
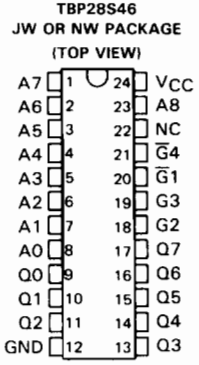
logic symbol



pin assignment



recommended operating conditions

PARAMETER		MJW			JW OR NW			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−2			−6.5	mA
I_{OL}	Low-level output current			16			16	mA
T_A	Operating free-air temperature range	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

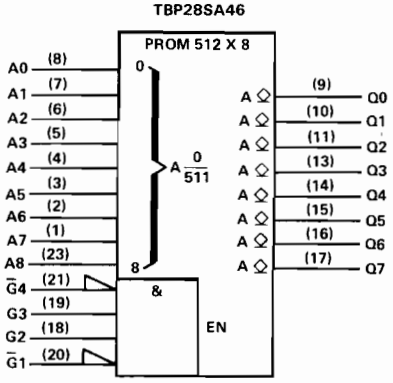
PARAMETER	TEST CONDITIONS†		MJW			JW OR NW			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = MIN,	I_{OH} = MAX	2.4	3.1		2.4	3.1		V
V_{OL}	V_{CC} = MIN,	I_{OL} = 16 mA			0.5			0.5	V
I_{OZH}	V_{CC} = MAX,	V_O = 2.4 V			50			50	μA
I_{OZL}	V_{CC} = MAX,	V_O = 0.5 V			−50			−50	μA
I_I	V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.7 V			25			25	μA
I_{IL}	V_{CC} = MAX,	V_I = 0.5 V			−0.25			−0.25	mA
I_{OS}§	V_{CC} = MAX		−15		−100	−20		−100	mA
I_{CC}	V_{CC} = MAX			100	135		100	135	mA

switching characteristics over recommended ranges of T_A and V_{CC} (unless otherwise noted)

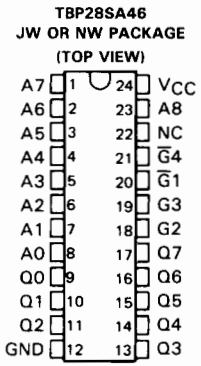
PARAMETER		TEST CONDITIONS	MJW			JW OR NW			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
$t_{a(A)}$	Access time from address	C_L = 30 pF		35	70		35	60	ns
$t_{a(S)}$	Access time from chip select (enable time)	See Note 3		20	45		20	35	ns
t_{dis}	Disable time	C_L = 5 pF See Note 3		15	40		15	35	ns

†For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.
NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

logic symbol



pin assignment



recommended operating conditions

PARAMETER		MJW			JW OR NW			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			16			16	mA
T_A	Operating free-air temperature range	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		MJW			JW OR NW			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN,	I_I = −18 mA			−1.2			−1.2	V
I_{OH}	V_{CC} = MIN,	V_{OH} = 2.4 V			0.05			0.05	mA
		V_{OH} = 5.5 V			0.1			0.1	
V_{OL}	V_{CC} = MIN,	I_{OL} = 16 mA			0.5			0.5	V
I_I	V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.7 V			25			25	μA
I_{IL}	V_{CC} = MAX,	V_I = 0.5 V			−0.25			−0.25	mA
I_{CC}	V_{CC} = MAX			100	135		100	135	mA

switching characteristics over recommended ranges of T_A and V_{CC} (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MJW			JW OR NW			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
$t_{a(A)}$	Access time from address	C_L = 30 pF		35	75		35	65	ns
$t_{a(S)}$	Access time from chip select (enable time)	R_{L1} = 300 Ω		20	45		20	35	ns
t_{PLH}	Propagation delay time low-to-high-level output from chip select	R_{L2} = 600 Ω See Note 3		15	40		15	35	ns

†For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

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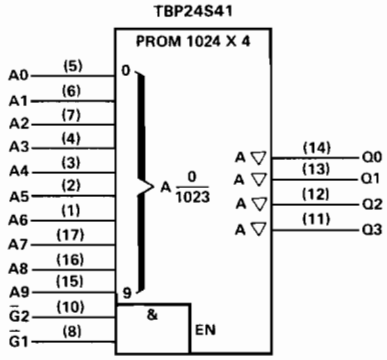
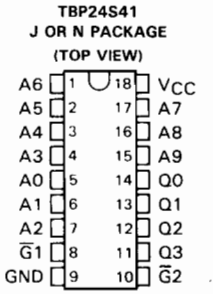
logic symbol



pin assignment



recommended operating conditions

PARAMETER		MJ			J OR N			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−2			−3.2	mA
I_{OL}	Low-level output current			16			16	mA
T_A	Operating free-air temperature range	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

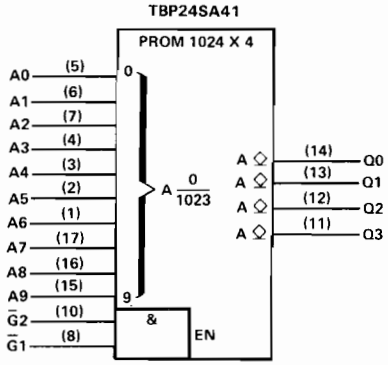
PARAMETER	TEST CONDITIONS†		MJ			J OR N			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = MIN,	I_{OH} = MAX	2.4	3.1		2.4	3.1		V
V_{OL}	V_{CC} = MIN,	I_{OL} = 16 mA			0.5			0.5	V
I_{OZH}	V_{CC} = MAX,	V_O = 2.4 V			50			50	μA
I_{OZL}	V_{CC} = MAX,	V_O = 0.5 V			−50			−50	μA
I_I	V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.7 V			25			25	μA
I_{IL}	V_{CC} = MAX,	V_I = 0.5 V			−0.25			−0.25	mA
I_{OS}§	V_{CC} = MAX		−15		−100	−20		−100	mA
I_{CC}	V_{CC} = MAX			95	140		95	140	mA

switching characteristics over recommended ranges of T_A and V_{CC} (unless otherwise noted)

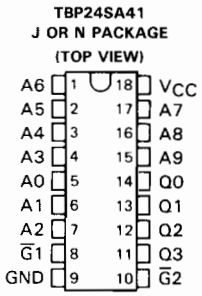
PARAMETER		TEST CONDITIONS	MJ			J OR N			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
$t_{a(A)}$	Access time from address	C_L = 30 pF See Note 3		40	75		40	60	ns
$t_{a(S)}$	Access time from chip select (enable time)			20	40		20	30	ns
t_{dis}	Disable time	C_L = 5 pF See Note 3		20	40		20	30	ns

†For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.
NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

logic symbol



pin assignment



recommended operating conditions

PARAMETER		MJ			J OR N			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			16			16	mA
T_A	Operating free-air temperature range	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		MJ			J OR N			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN,	I_I = −18 mA			−1.2			−1.2	V
I_{OH}	V_{CC} = MIN,	V_{OH} = 2.4 V			0.05			0.05	mA
		V_{OH} = 5.5 V			0.1			0.1	
V_{OL}	V_{CC} = MIN,	I_{OL} = 16 mA			0.5			0.5	V
I_I	V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.7 V			25			25	μA
I_{IL}	V_{CC} = MAX,	V_I = 0.5 V			−0.25			−0.25	mA
I_{CC}	V_{CC} = MAX			95	140		95	140	mA

switching characteristics over recommended ranges of T_A and V_{CC} (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MJ			J OR N			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
$t_{a(A)}$	Access time from address	C_L = 30 pF		40	75		40	60	ns
$t_{a(S)}$	Access time from chip select (enable time)	R_{L1} = 300 Ω		20	40		20	30	ns
t_{PLH}	Propagation delay time low-to-high-level output from chip select	R_{L2} = 600 Ω See Note 3		20	40		20	30	ns

†For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

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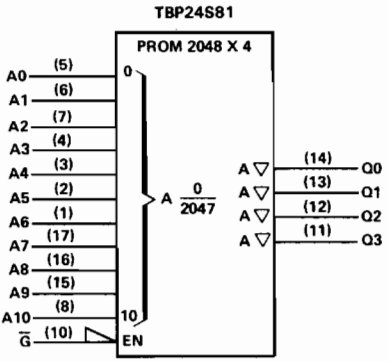
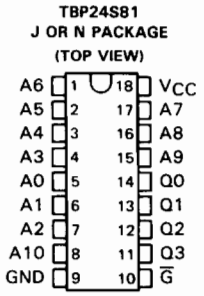
logic symbol



pin assignment



recommended operating conditions

PARAMETER		MJ			J OR N			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−2			−3.2	mA
I_{OL}	Low-level output current			16			16	mA
T_A	Operating free-air temperature range	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		MJ			J OR N			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = MIN,	I_{OH} = MAX	2.4	3.1		2.4	3.1		V
V_{OL}	V_{CC} = MIN,	I_{OL} = 16 mA			0.5			0.5	V
I_{OZH}	V_{CC} = MAX,	V_O = 2.4 V			50			50	μA
I_{OZL}	V_{CC} = MAX,	V_O = 0.5 V			−50			−50	μA
I_I	V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.7 V			25			25	μA
I_{IL}	V_{CC} = MAX,	V_I = 0.5 V			−0.25			−0.25	mA
I_{OS}§	V_{CC} = MAX		−15		−100	−20		−100	mA
I_{CC}	V_{CC} = MAX			125	175		125	175	mA

switching characteristics over recommended ranges of T_A and V_{CC} (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MJ			J OR N			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
$t_{a(A)}$	Access time from address	C_L = 30 pF		45	85		45	70	ns
$t_{a(S)}$	Access time from chip select (enable time)	See Note 3		20	50		20	40	ns
t_{dis}	Disable time	C_L = 5 pF See Note 3		20	50		20	40	ns

†For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.
NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

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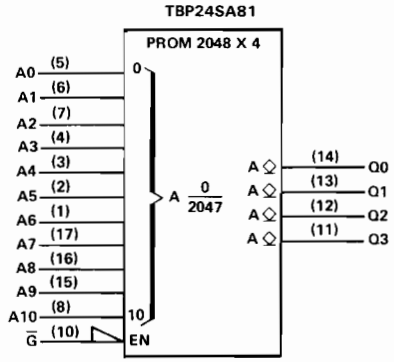
logic symbol



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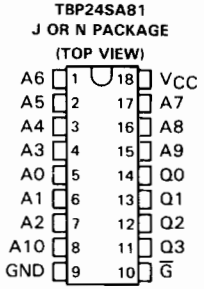


recommended operating conditions

PARAMETER		MJ			J OR N			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			16			16	mA
T_A	Operating free-air temperature range	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		MJ			J OR N			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN,	I_I = −18 mA			−1.2			−1.2	V
I_{OH}	V_{CC} = MIN,	V_{OH} = 2.4 V			0.05			0.05	VmA
		V_{OH} = 5.5 V			0.1			0.1	
V_{OL}	V_{CC} = MIN,	I_{OL} = 16 mA			0.5			0.5	V
I_I	V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.7 V			25			25	μA
I_{IL}	V_{CC} = MAX,	V_I = 0.5 V			−0.25			−0.25	mA
I_{CC}	V_{CC} = MAX			125	175		125	175	mA

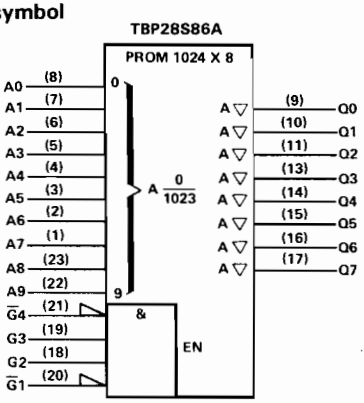
switching characteristics over recommended ranges of T_A and V_{CC} (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MJ			J OR N			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
$t_{a(A)}$	Access time from address	C_L = 30 pF		45	95		45	70	ns
$t_{a(S)}$	Access time from chip select (enable time)	R_{L1} = 300 Ω		20	50		20	40	ns
t_{PLH}	Propagation delay time low-to-high-level output from chip select	R_{L2} = 600 Ω See Note 3		20	50		20	40	ns

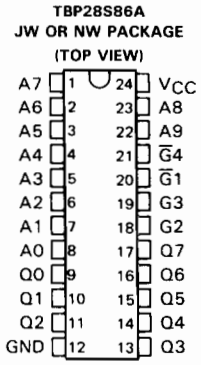
†For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

logic symbol



pin assignment



recommended operating conditions

PARAMETER		MJW			JW OR NW			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−2			−3.2	mA
I_{OL}	Low-level output current			12			12	mA
T_A	Operating free-air temperature range	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

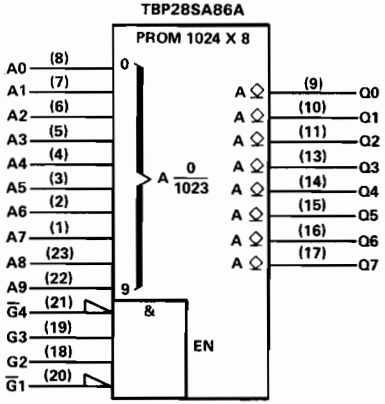
PARAMETER	TEST CONDITIONS†		MJW			JW OR NW			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = MIN,	I_{OH} = MAX	2.4	3.1		2.4	3.1		V
V_{OL}	V_{CC} = MIN,	I_{OL} = 12 mA			0.5			0.5	V
I_{OZH}	V_{CC} = MAX,	V_O = 2.4 V			50			50	μA
I_{OZL}	V_{CC} = MAX,	V_O = 0.5 V			−50			−50	μA
I_I	V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.7 V			25			25	μA
I_{IL}	V_{CC} = MAX,	V_I = 0.5 V			−0.25			−0.25	mA
I_{OS}§	V_{CC} = MAX		−15		−100	−20		−100	mA
I_{CC}	V_{CC} = MAX			110	170		110	165	mA

switching characteristics over recommended ranges of T_A and V_{CC} (unless otherwise noted)

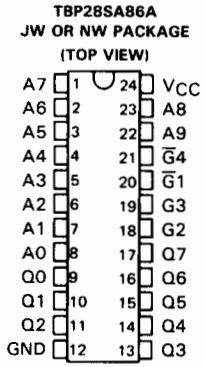
PARAMETER		TEST CONDITIONS	MJW			JW OR NW			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
$t_{a(A)}$	Access time from address	C_L = 30 pF		35	80		35	65	ns
$t_{a(S)}$	Access time from chip select (enable time)	See Note 3		20	50		20	40	ns
t_{dis}	Disable time	C_L = 5 pF See Note 3		15	40		15	35	ns

†For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.
NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

logic symbol



pin assignment



recommended operating conditions

PARAMETER		MJW			JW OR NW			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			12			12	mA
T_A	Operating free-air temperature range	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		MJW			JW OR NW			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN,	I_I = −18 mA			−1.2			−1.2	V
I_{OH}	V_{CC} = MIN,	V_{OH} = 2.4 V			0.05			0.05	mA
		V_{OH} = 5.5 V			0.1			0.1	
V_{OL}	V_{CC} = MIN,	I_{OL} = 12 mA			0.5			0.5	V
I_I	V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.7 V			25			25	μA
I_{IL}	V_{CC} = MAX,	V_I = 0.5 V			−0.25			−0.25	mA
I_{CC}	V_{CC} = MAX			125	175		125	175	mA

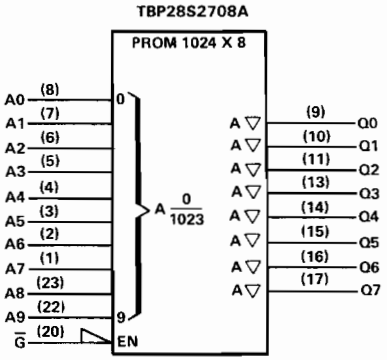
switching characteristics over recommended ranges of T_A and V_{CC} (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MJW			JW OR NW			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
$t_{a(A)}$	Access time from address	C_L = 30 pF		35	80		35	70	ns
$t_{a(S)}$	Access time from chip select (enable time)	R_{L1} = 300 Ω		20	50		20	40	ns
t_{PLH}	Propagation delay time low-to-high-level output from chip select	R_{L2} = 600 Ω See Note 3		15	40		15	35	ns

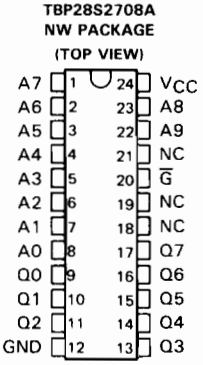
†For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

logic symbol



pin assignment



recommended operating conditions

PARAMETER		NW			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			−3.2	mA
I_{OL}	Low-level output current			12	mA
T_A	Operating free-air temperature range	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

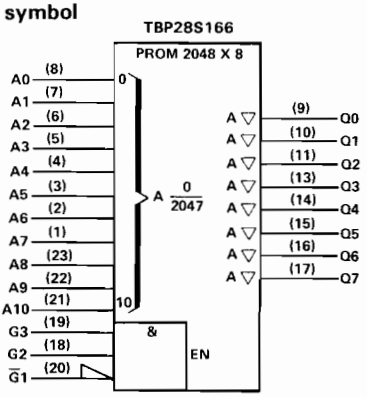
PARAMETER	TEST CONDITIONS		NW			UNIT
			MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.75,	I_I = −18 mA			−1.2	V
V_{OH}	V_{CC} = 4.75,	I_{OH} = −3.2 mA	2.4	3.1		V
V_{OL}	V_{CC} = 4.75,	I_{OL} = 12 mA			0.5	V
I_{OZH}	V_{CC} = 5.25,	V_O = 2.4 V			50	μA
I_{OZL}	V_{CC} = 5.25,	V_O = 0.5 V			−50	μA
I_I	V_{CC} = 5.25,	V_I = 5.5 V			1	mA
I_{IH}	V_{CC} = 5.25,	V_I = 2.7 V			25	μA
I_{IL}	V_{CC} = 5.25,	V_I = 0.5 V			−0.25	mA
I_{OS}‡	V_{CC} = 5.25		−20		−100	mA
I_{CC}	V_{CC} = 5.25			110	165	mA

switching characteristics over recommended ranges of T_A and V_{CC} (unless otherwise noted)

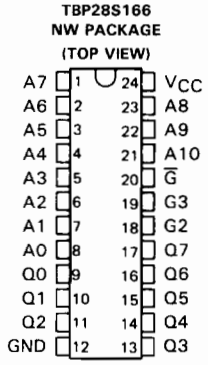
PARAMETER		TEST CONDITIONS	NW			UNIT
			MIN	TYP†	MAX	
$t_{a(A)}$	Access time from address	C_L = 30 pF		45	70	ns
$t_{a(S)}$	Access time from chip select (enable time)	See Note 3		20	40	ns
t_{dis}	Disable time	C_L = 5 pF See Note 3		20	40	ns

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.
NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

logic symbol



pin assignment



recommended operating conditions

PARAMETER		NW MIN	NW NOM	NW MAX	UNIT
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			−3.2	mA
I_{OL}	Low-level output current			16	mA
T_A	Operating free-air temperature range	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		NW MIN	NW TYP†	NW MAX	UNIT
V_{IK}	V_{CC} = 4.75,	I_I = −18 mA			−1.2	V
V_{OH}	V_{CC} = 4.75,	I_{OH} = −3.2 mA	2.4	3.1		V
V_{OL}	V_{CC} = 4.75,	I_{OL} = 16 mA			0.5	V
I_{OZH}	V_{CC} = 5.25,	V_O = 2.4 V			50	μA
I_{OZL}	V_{CC} = 5.25,	V_O = 0.5 V			−50	μA
I_I	V_{CC} = 5.25,	V_I = 5.5 V			1	mA
I_{IH}	V_{CC} = 5.25,	V_I = 2.7 V			25	μA
I_{IL}	V_{CC} = 5.25,	V_I = 0.5 V			−0.25	mA
I_{OS}‡	V_{CC} = 5.25		−20		−100	mA
I_{CC}	V_{CC} = 5.25			130	175	mA

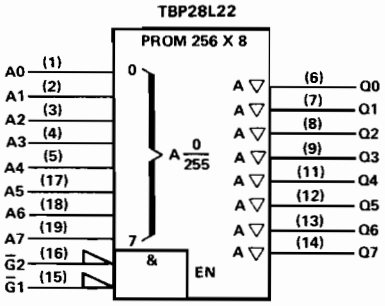
switching characteristics over recommended ranges of T_A and V_{CC} (unless otherwise noted)

PARAMETER		TEST CONDITIONS	NW MIN	NW TYP†	NW MAX	UNIT
$t_{a(A)}$	Access time from address	C_L = 30 pF		35	75	ns
$t_{a(S)}$	Access time from chip select (enable time)	See Note 3		15	40	ns
t_{dis}	Disable time	C_L = 5 pF See Note 3		15	40	ns

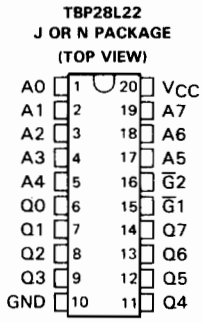
†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.
NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

logic symbol



pin assignment



recommended operating conditions

PARAMETER		MJ			J OR N			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−2			−6.5	mA
I_{OL}	Low-level output current			16			16	mA
T_A	Operating free-air temperature range	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		MJ			J OR N			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = MIN,	I_{OH} = MAX	2.4	3.1		2.4	3.1		V
V_{OL}	V_{CC} = MIN,	I_{OL} = 16 mA			0.5			0.5	V
I_{OZH}	V_{CC} = MAX,	V_O = 2.4 V			50			50	μA
I_{OZL}	V_{CC} = MAX,	V_O = 0.5 V			−50			−50	μA
I_I	V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.7 V			25			25	μA
I_{IL}	V_{CC} = MAX,	V_I = 0.5 V			−0.25			−0.25	mA
I_{OS}§	V_{CC} = MAX		−25		−100	−30		−100	mA
I_{CC}	V_{CC} = MAX			75	100		75	100	mA

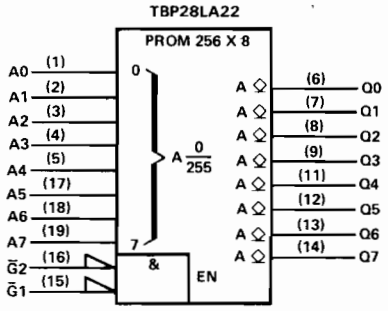
switching characteristics over recommended ranges of T_A and V_{CC} (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MJ			J OR N			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{aA}	Access time from address	C_L = 30 pF		45	75		45	70	ns
$t_{a(S)}$	Access time from chip select (enable time)	See Note 3		20	40		20	35	ns
t_{dis}	Disable time	C_L = 5 pF See Note 3		15	35		15	30	ns

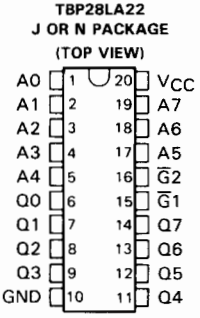
†For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.
NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

TBP28LA22
2048 BITS (256 WORDS BY 8 BITS)
LOW-POWER PROGRAMMABLE READ-ONLY MEMORIES WITH OPEN-COLLECTOR OUTPUTS

logic symbol



pin assignment



recommended operating conditions

PARAMETER		MJ			J OR N			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			16			16	mA
T_A	Operating free-air temperature range	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		MJ			J OR N			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN,	I_I = −18 mA			−1.2			−1.2	V
I_{OH}	V_{CC} = MIN,	V_{OH} = 2.4 V			0.05			0.05	mA
		V_{OH} = 5.5 V			0.1			0.1	
V_{OL}	V_{CC} = MIN,	I_{OL} = 16 mA			0.5			0.5	V
I_I	V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.7 V			25			25	μA
I_{IL}	V_{CC} = MAX,	V_I = 0.5 V			−0.25			−0.25	mA
I_{CC}	V_{CC} = MAX			75	100		75	100	mA

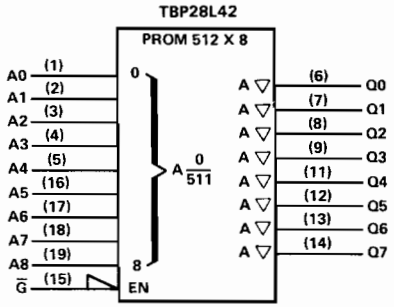
switching characteristics over recommended ranges of T_A and V_{CC} (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MJ			J OR N			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
$t_{a(A)}$	Access time from address	C_L = 30 pF		40	80		45	75	ns
$t_{a(S)}$	Access time from chip select (enable time)	R_{L1} = 300 Ω		20	40		20	35	ns
t_{PLH}	Propagation delay time low-to-high-level output from chip select	R_{L2} = 600 Ω See Note 3		15	35		15	30	ns

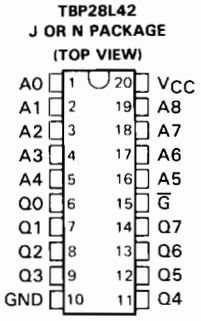
†For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

logic symbol



pin assignment



recommended operating conditions

PARAMETER		MJ			J OR N			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−1			−1.6	mA
I_{OL}	Low-level output current			8			8	mA
T_A	Operating free-air temperature range	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

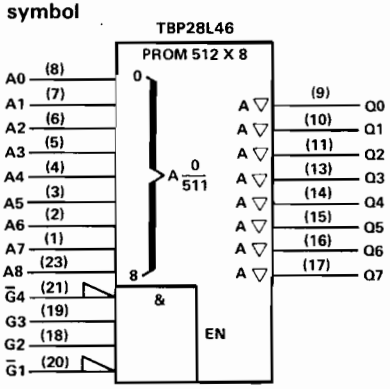
PARAMETER	TEST CONDITIONS†		MJ			J OR N			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = MIN,	I_{OH} = MAX	2.4	3.1		2.4	3.1		V
V_{OL}	V_{CC} = MIN,	I_{OL} = 8 mA			0.5			0.5	V
I_{OZH}	V_{CC} = MAX,	V_O = 2.4 V			50			50	μA
I_{OZL}	V_{CC} = MAX,	V_O = 0.5 V			−50			−50	μA
I_I	V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.7 V			25			25	μA
I_{IL}	V_{CC} = MAX,	V_I = 0.5 V			−0.25			−0.25	mA
I_{OS}§	V_{CC} = MAX		−10		−100	−10		−100	mA
I_{CC}	V_{CC} = MAX			50	85		50	85	mA

switching characteristics over recommended ranges of T_A and V_{CC} (unless otherwise noted)

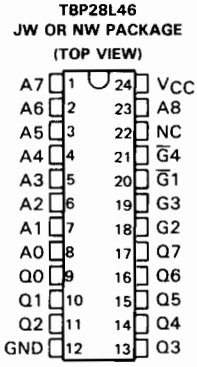
PARAMETER		TEST CONDITIONS	MJ			J OR N			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
$t_{a(A)}$	Access time from address	C_L = 30 pF		55	110		55	95	ns
$t_{a(S)}$	Access time from chip select (enable time)	See Note 3		25	60		25	60	ns
t_{dis}	Disable time	C_L = 5 pF See Note 3		25	50		25	40	ns

†For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.
NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

logic symbol



pin assignment



recommended operating conditions

PARAMETER		MJW			JW OR NW			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−1			−1.6	mA
I_{OL}	Low-level output current			8			8	mA
T_A	Operating free-air temperature range	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		MJW			JW OR NW			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = MIN,	I_{OH} = MAX	2.4	3.1		2.4	3.1		V
V_{OL}	V_{CC} = MIN,	I_{OL} = 8 mA			0.5			0.5	V
I_{OZH}	V_{CC} = MAX,	V_O = 2.4 V			50			50	μA
I_{OZL}	V_{CC} = MAX,	V_O = 0.5 V			−50			−50	μA
I_I	V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.7 V			25			25	μA
I_{IL}	V_{CC} = MAX,	V_I = 0.5 V			−0.25			−0.25	mA
I_{OS}§	V_{CC} = MAX		−10		−100	−10		−100	mA
I_{CC}	V_{CC} = MAX			50	85		50	85	mA

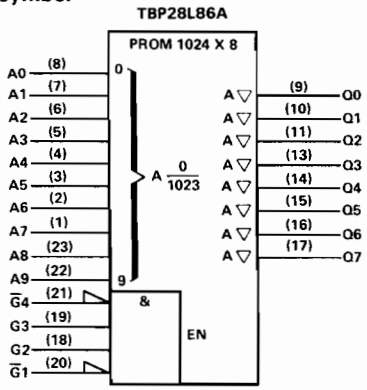
switching characteristics over recommended ranges of T_A and V_{CC} (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MJW			JW OR NW			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
$t_{a(A)}$	Access time from address	C_L = 30 pF		55	110		55	95	ns
$t_{a(S)}$	Access time from chip select (enable time)	See Note 3		25	60		25	60	ns
t_{dis}	Disable time	C_L = 5 pF See Note 3		25	50		25	40	ns

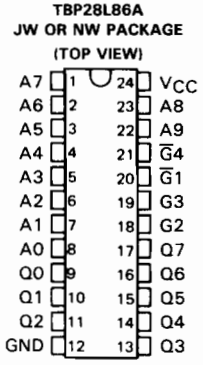
†For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.
NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

logic symbol



pin assignment



recommended operating conditions

PARAMETER		MJW			JW OR NW			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−1			−1.6	mA
I_{OL}	Low-level output current			8			8	mA
T_A	Operating free-air temperature range	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

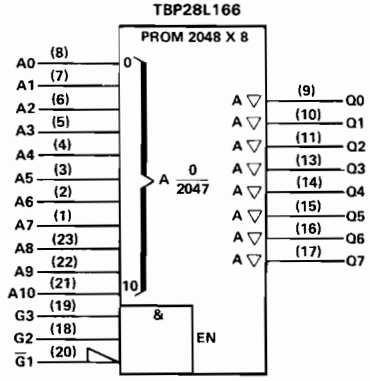
PARAMETER	TEST CONDITIONS†		MJW			JW OR NW			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = MIN,	I_{OH} = MAX	2.4	3.1		2.4	3.1		V
V_{OL}	V_{CC} = MIN,	I_{OL} = 8 mA			0.5			0.5	V
I_{OZH}	V_{CC} = MAX,	V_O = 2.4 V			50			50	μA
I_{OZL}	V_{CC} = MAX,	V_O = 0.5 V			−50			−50	μA
I_I	V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.7 V			25			25	μA
I_{IL}	V_{CC} = MAX,	V_I = 0.5 V			−0.25			−0.25	mA
I_{OS}§	V_{CC} = MAX		−10		−100	−10		−100	mA
I_{CC}	V_{CC} = MAX			55	95		55	80	mA

switching characteristics over recommended ranges of T_A and V_{CC} (unless otherwise noted)

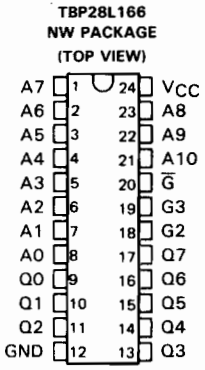
PARAMETER		TEST CONDITIONS	MJW			JW OR NW			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
$t_{a(A)}$	Access time from address	C_L = 30 pF		65	200		65	110	ns
$t_{a(S)}$	Access time from chip select (enable time)	See Note 3		40	125		40	80	ns
t_{dis}	Disable time	C_L = 5 pF See Note 3		25	100		25	60	ns

†For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.
NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

logic symbol



pin assignment



recommended operating conditions

PARAMETER		NW			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			−1.6	mA
I_{OL}	Low-level output current			8	mA
T_A	Operating free-air temperature range	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		NW			UNIT
			MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.75,	I_I = −18 mA			−1.2	V
V_{OH}	V_{CC} = 4.75,	I_{OH} = −1.6 mA	2.4	3.1		V
V_{OL}	V_{CC} = 4.75,	I_{OL} = 8 mA			0.5	V
I_{OZH}	V_{CC} = 5.25,	V_O = 2.4 V			50	μA
I_{OZL}	V_{CC} = 5.25,	V_O = 0.5 V			−50	μA
I_I	V_{CC} = 5.25,	V_I = 5.5 V			1	mA
I_{IH}	V_{CC} = 5.25,	V_I = 2.7 V			25	μA
I_{IL}	V_{CC} = 5.25,	V_I = 0.5 V			−0.25	mA
I_{OS}‡	V_{CC} = 5.25		−10		−100	mA
I_{CC}	V_{CC} = 5.25			75	110	mA

switching characteristics over recommended ranges of T_A and V_{CC} (unless otherwise noted)

PARAMETER		TEST CONDITIONS	NW			UNIT
			MIN	TYP†	MAX	
$t_{a(A)}$	Access time from address	C_L = 30 pF		80	125	ns
$t_{a(S)}$	Access time from chip select (enable time)	See Note 3		40	65	ns
t_{dis}	Disable time	C_L = 5 pF See Note 3		30	65	ns

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.
NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

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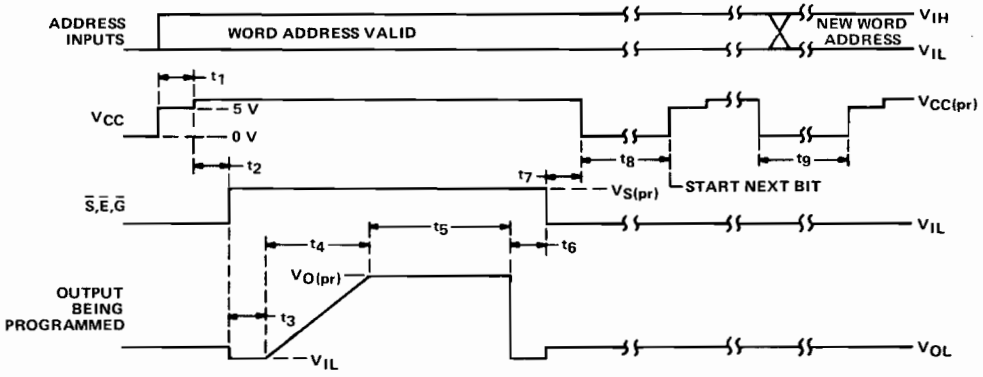
recommended operating conditions for programming (see Figure 1)

		MIN	NOM	MAX	UNIT
Steady-state supply voltage	V_{CC}	4.75	5	5.25	V
Input voltage	V_{IH}	3	4	5	V
	V_{IL}	0	0	0.5	
Voltage at all outputs except the one to be programmed		0	0	0.5	V
Supply voltage level to program a bit	$V_{CC(pr)}$	5.75	6	6.25	V
Select or enable level to program a bit	$V_{S(pr)}$	9.75	10	11	V
Output level during interval t_5	$V_{O(pr)}$	15.75	16	16.25	V
Supply voltage during verification (see step 14)	Low	4.4	4.5	4.6	V
	High	5.4	5.5	5.6	
Time from V_{CC} to settle and to verify need to program	t_1	0	5	10	μs
Time from V_{CC} = 6 V until chip select (enable) is at 10 V	t_2	5	5	10	μs
Time from chip select (enable) high to start of program ramp	t_3	0.1	5	10	μs
Ramp time, output program pulse	t_4	10	15	20	μs
Duration of output program pulse	t_5	15	20	20	μs
Time from end of program pulse to chip select (enable) low	t_6	5	5	10	μs
Time from chip select (enable) V_{CC} = 0 V	t_7	0.1	5	5	μs
Time for cooling between bits	t_8	30	50	100	μs
Time for cooling between words	t_9	30	50		μs
Free-air temperature	T_A	20	25	30	°C

step-by-step programming instruction (see Figure 1)

1. Address the word to be programmed, apply 5 volts to V_{CC} and active levels to all chip select (S and $\overline{S}$) or chip enable (E and $\overline{E}$) inputs.
2. Verify the status of a bit location by checking the output level.
3. Decreass V_{CC} to 0 volts.
4. For bit locations that do not require programming, skip steps 5 through 11.
5. Increase V_{CC} to $V_{CC(pr)}$ with a minimum current capability of 250 milliamperes.
6. Apply $V_{S(pr)}$ to all the $\overline{S}$, $\overline{E}$ or $\overline{G}$ inputs. $I_I \leq 25$ milliamperes. Active-high enables may be left high.
7. Connect all outputs, except the one to be programmed, to V_{IL}. Only one bit is to be programmed at a time.
8. Apply the output programming pulse for 20 microseconds. Minimum current capability of the programming supply should be 250 milliamperes.
9. After terminating the output pulse, disconnect all outputs from V_{IL} conditions.
10. Reduce the voltage at $\overline{S}$, $\overline{E}$, or $\overline{G}$ inputs to V_{II}.
11. Decrease V_{CC} to 0 volts.
12. Return to step 4 until all outputs in the word have been programmed.
13. Repeat steps 2 through 11 for each word in memory.
14. Verify programming of every word after all words have been programmed using V_{CC} values of 4.5 and 5.5 volts.



NOTE 4: Rise and fall times should be $\leq$ 1 μs.

FIGURE 1. TIMING DIAGRAM AND VOLTAGE WAVEFORMS FOR PROGRAMMING SEQUENCE

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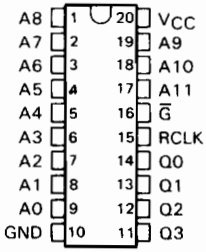
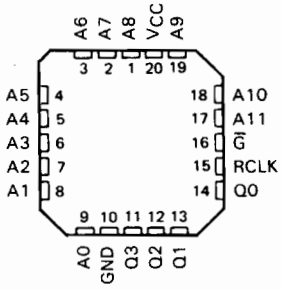
- **Fastest Schottky PROM Family**
- **High-Speed Access Times**
- **Allows Storage of Output Data**

TBP34R165 . . . JT OR NT PACKAGE
(TOP VIEW)



TBP34R16X . . . FN OR FK PACKAGE
(TOP VIEW)



description

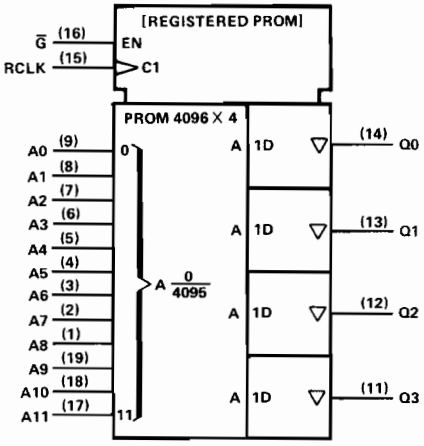
The TBP34R16 is a series-3 monolithic TTL programmable read-only memory (PROM) featuring high-speed access times and dependable titanium-tungsten fuse link program elements. It is organized as 4096 words by 4 bits, providing 16,384 bits.

The output register receives data from the PROM array on the rising edge of RCLK. Data is programmed at any bit location with the standard series 3 programming algorithm. The program elements store a low logic level before any programming, and are permanently set to a high logic level after programming. After execution of the programming procedure, the output for that bit location cannot be reversed. The series 3 programming procedure should be referred to for further details. Additional circuits have been designed into these devices to improve testability and ensure high programmability.

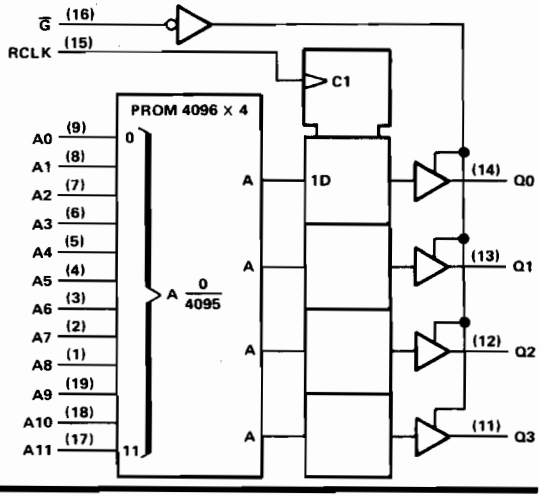
4

PROMs

logic symbol



logic diagram (positive logic)



TERMINAL FUNCTIONS

TERMINALS	FUNCTION
A0 – A11	Address inputs for data from PROM array
$\overline{G}$	If $\overline{G}$ is high, Q0 thru Q11 are high-impedance state. If $\overline{G}$ is low, Q0 thru Q11 are enabled.
RCLK	Low-to-high transition loads output register from PROM array.
Q0 – Q3	Register outputs under control of $\overline{G}$

recommended operating conditions for programming (see Figure 1)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage during verification	4.5	5	5.5	V
V_{IH}	High-level input voltage	3	4	5	V
V_{IL}	Low-level input voltage	0	0.2	0.4	V
	Enable $\overline{G}$ voltage during verification	0	0.2	0.4	V
	Enable $\overline{G}$ inactive voltage during programming	4.5	5	5.5	V
$V_{CC(pr)}$	Supply voltage program pulse amplitude	12	12.5	13	V
t_{w1}	V_{CC} program pulse duration, 1st attempt	10	11	12	μs
t_{w2}	V_{CC} program pulse duration, 2nd attempt	20	22	25	μs
t_{w3}	V_{CC} program pulse duration, 3rd attempt	20	22	25	μs
t_{su}	Setup time, enable $\overline{G}$ low before $V_{CC(pr)}$ †	0.1	0.5	1	μs
t_h	Hold time, enable $\overline{G}$ low after $V_{CC(pr)}$ ‡	0.1	0.5	1	μs
$t_{r(V_{CC})}$	Rise time, $V_{CC(pr)}$ (5 V to 12 V)	0.3	0.4	0.5	μs
$t_{f(V_{CC})}$	Fall time, $V_{CC(pr)}$ (12 V to 5 V)	0.05	0.1	0.2	μs
t_d	Delay time between successive $V_{CC(pr)}$ pulses	10	20	30	μs
t_{cool}	Cooling time between words	100	150	200	μs
T_A	Free-air temperature	20	25	30	°C

†Measured from 1.5 V on enable pin to 5.5 V on $V_{CC(pr)}$.
‡Measured from 5.5 V on $V_{CC(pr)}$ to 1.5 V on enable pin.

step-by-step programming instructions (see Figure 1)

1. Address the word to be programmed, apply 5 V to V_{CC} and a low logic level to the $\overline{G}$ input.
2. Verify the selected bit location that requires programming. Note: The only bit positions that require programming are outputs to be at a high logic level.
3. For bit locations that do not require programming, go to step 2 for the next bit, or to step 1 for the next word.
4. Deselect PROM by applying 5 V to $\overline{G}$.
5. Connect a 4-mA current source (clamped to V_{CC}) to the output to be programmed.
6. Increase V_{CC} to $V_{CC(pr)}$ for a pulse duration equal to t_{wX} (where X is determined by the number of programming attempts, i.e., 1, 2, 3). Minimum current capability for the V_{CC} power supply should be 400 mA.
7. Verify that the output has been programmed to a high logic level. If the output has been programmed correctly, go to the next bit. If not, repeat steps 2 through 7 and increment X (where X equals 1 on the first programming attempt). If the output has not been programmed by the third attempt, stop programming and go to a new device.
8. Verify programming of every word after all words have been programmed using V_{CC} values of 4.5 volts and 5.5 volts.

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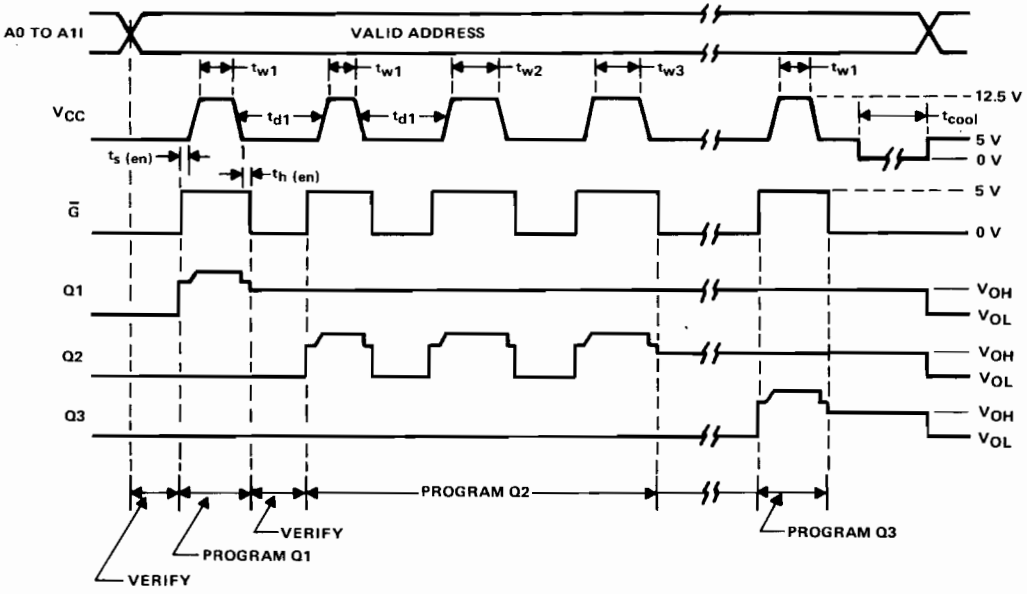
series 3 programming sequence



Illustrated above is the following sequence:

1) It is desired to program the selected address with 0111(Q0-Q3). Outputs Q1, Q2, and Q3 need programming.
2) Q1 is verified to be at a low logic level and then the programming sequence is executed. The output is then verified to be at a high logic level.
3) Q3 is an example of an output requiring three attempts to be programmed successfully.
4) Q3 is programmed to a high logic level.

FIGURE 1. SERIES 3 PROGRMMING SEQUENCE

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)		7 V
Input voltage, V_I		5.5 V
Off-state output voltage, $V_{O(off)}$		5.5 V
Operating free-air temperature range:	Military-temperature-range circuits	−55°C to 125°C
	Commercial-temperature-range circuits	0°C to 70°C
Storage temperature range		−65°C to 150°C

NOTE 1: All voltage values are with respect to network ground terminal. The supply voltage rating does not apply during programming.

recommended operating conditions

PARAMETER		MILITARY			COMMERCIAL			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−2			−3.2	mA
I_{OL}	Low-level output current			16			16	mA
t_{su}	Setup time, address before RCLK							ns
t_h	Hold time, address after RCLK							ns
T_A	Operating free-air temperature range	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	MILITARY			COMMERCIAL			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN, I_I = −18 mA			−1.2			1.2	V
V_{OH}	V_{CC} = MIN, I_{OH} = MAX	2.4	3.1		2.4	3.1		V
V_{OL}	V_{CC} = MIN, I_{OL} = 16 mA			0.5			0.5	V
I_{OZH}	V_{CC} = MAX, V_O = 2.4 V			50			50	μA
I_{OZL}	V_{CC} = MAX, V_O = 0.5 V			−50			−50	μA
I_I	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	V_{CC} = MAX, V_I = 2.7 V			25			25	μA
I_{IL}	V_{CC} = MAX, V_I = 0.5 V			−0.25			−0.25	mA
I_O§	V_{CC} = MAX, V_O = 2.25 V		60			60		mA
I_{CC}	V_{CC} = MAX					105		mA

switching characteristics over recommended ranges of T_A and V_{CC} (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITION (See Note 2)	MILITARY			COMMERCIAL			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{pd}	RCLK	Q0 – Q3	C_L = 30 pF							ns
t_{en}	G	Q0 – Q3								ns
t_{dis}	G	Q0 – Q3								ns

†For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely aproximates one half of the true short-circuit output current, I_{OS}.
NOTE 2: Load circuits and voltage waveforms are shown in Section 1 of *The TTL Data Book, Volume 4*, 1985.

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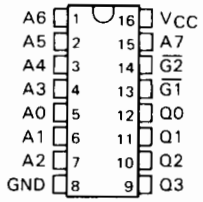
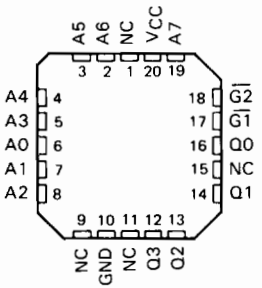
- **Fastest Schottky PROM Family**
- **High-Speed Access Times**
- **Low-Power, 3-State, and Open-Collector Options Available**
- **Titanium-Tungsten (Ti-W) Fuse Links for Reliable Low-Voltage Programming**
- **Applications Include:**
  Microprogramming/Firmware Loaders
  Code Converters/Character Generators
  Translators/Emulators
  Address Mapping/Look-Up Tables

TBP34S10, TBP34L10, TBP34SA10
N OR J PACKAGE
(TOP VIEW)



TBP34S1X, TBP34L1X, TBP34SA1X
FN OR FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

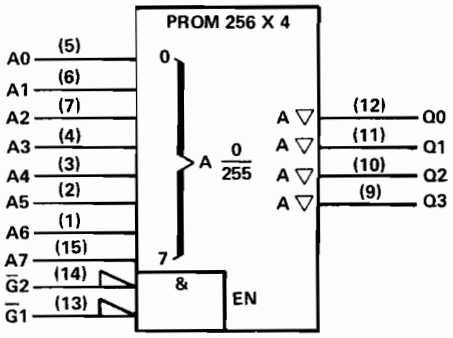
These Series-3 monolithic TTL programmable read-only memories (PROMs) feature high-speed access times and dependable titanium-tungsten fuse link program elements. They are organized as 256 words by 4 bits each, providing a total of 1024 bits. The '34S1 has three-state outputs. The '34SA1 is the open-collector version and allows the device to be connected directly to data buses utilizing passive pull-up resistors. The low-power '34L1 is available for applications that require power conservation while maintaining bipolar speeds. It also has three-state outputs.

Data is programmed at any bit location with the standard Series 3 programming algorithm. The program elements store a logic level low before any programming, and are permanently set to a logic level high after programming. After execution of the programming procedure, the output for that bit location cannot be reversed. The Series 3 programming procedure should be referred to for further details. Additional circuitry has been designed into these devices to improve testability and insure high programmability.

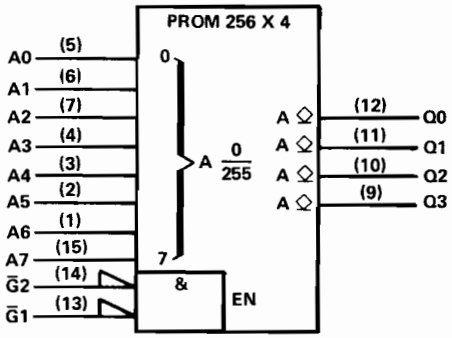
4 PROMs

logic symbol

TBP34S1, TBP34L1

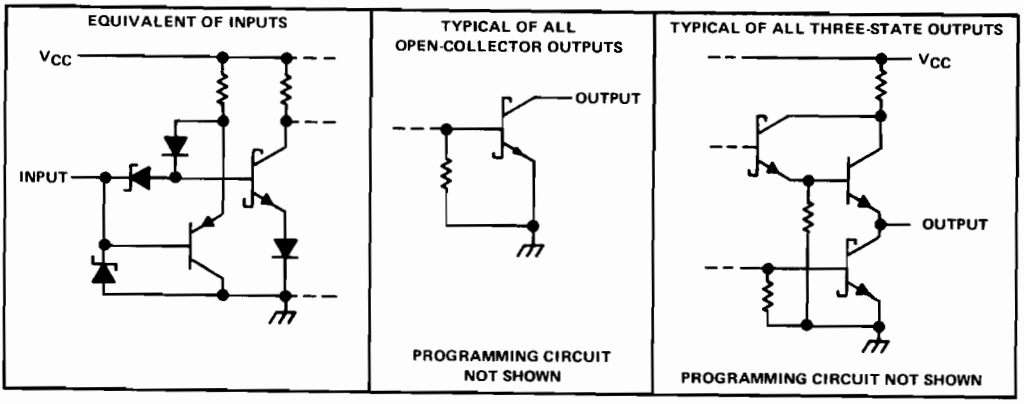


TBP34SA1



Pin numbers shown are for J or N packages.

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Off-state output voltage . . . . . 5.5 V
Operating free-air temperature range: Military-temperature-range circuits . . . . . −55°C to 125°C
Commercial-temperature-range circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal. The supply voltage rating does not apply during programming.

TEXAS INSTRUMENTS
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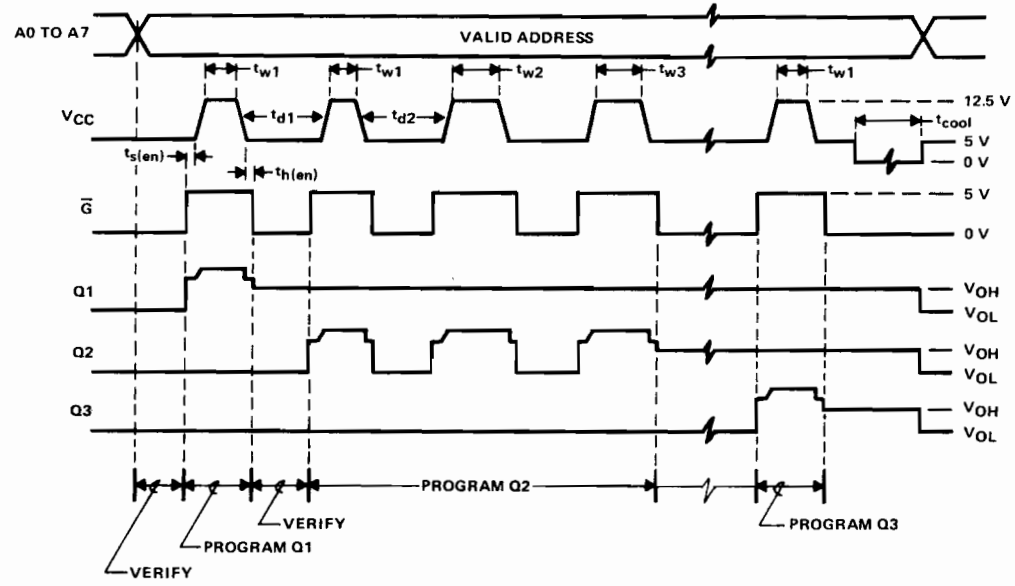
recommended operating conditions for programming (see Figure 1)

			MIN	NOM	MAX	UNIT
Supply voltage during verification		V_{CC}	4.5	5	5.5	V
Input voltage		V_{IH}	3	4	5	V
		V_{IL}	0	0.2	0.5	
Enable voltage during verification		$\overline{G}1$, $\overline{G}2$	0	0.2	0.4	V
Enable inactive voltage during programming		$\overline{G}1$, $\overline{G}2$	4.5	5	5.5	V
V_{CC} program pulse amplitude		$V_{CC(pr)}$	12	12.5	13	V
V_{CC} program pulse duration	1st attempt	t_{w1}	10	11	12	μs
	2nd attempt	t_{w2}	20	22	25	
	3rd attempt	t_{w3}	20	22	25	
Enable set-up time† before $V_{CC(pr)}$		$t_{s(en)}$	0.1	0.5	1	μs
Enable hold time‡ after $V_{CC(pr)}$		$t_{h(en)}$	0.1	0.5	1	μs
Rise time of $V_{CC(pr)}$§		$t_r(V_{CC})$	0.3	0.4	0.5	μs
Fall time of $V_{CC(pr)}$¶		$t_f(V_{CC})$	0.05	0.1	0.2	μs
Delay time between successive $V_{CC(pr)}$ pulses		t_{d1}	10	20	30	μs
Delay time between successive $V_{CC(pr)}$ pulses		t_{d2}	10	20	30	μs
Cooling time between words		t_{cool}	100	150	200	μs
Free-air temperature		T_A	20	25	30	°C

†Measured from 1.5 V on enable pin to 5.5 V on $V_{CC(pr)}$
‡Measured from 5.5 V on $V_{CC(pr)}$ to 1.5 V on enable pin
§Measured from 5 V to 12 V
¶Measured from 12 V to 5 V

step-by-step programming instructions (see Figure 1)

1. Address the word to be programmed, apply 5 volts to V_{CC} and active levels to all enable inputs ($\overline{G}1$, $\overline{G}2$).
2. Verify the selected bit location that requires programming. Note: The only bit positions that require programming are outputs needing a high logic level.
3. For bit locations that do not require programming, go to step 2 for the next bit, or to step 1 for next word.
4. Deselect PROM by applying 5 volts to $\overline{G}1$ or $\overline{G}2$.
5. Connect a 4-mA current source (clamped to V_{CC}) to the output that is to be programmed.
6. Increase V_{CC} to $V_{CC(pr)}$ for a pulse duration equal to t_{wX} (where X is determined by the number of programming attempts, i.e., 1,2,3). Minimum current capability for the V_{CC} power supply should be 400 mA.
7. Verify that the output has been programmed to a high logic level. If the output has been programmed correctly, go to the next bit. If not, repeat step 2 through step 7 and increment X (where X is equal to 1 on the first programming attempt). If the output has not been programmed by the third attempt, stop programming and go to a new device.
8. Verify programming of every word after all words have been programmed using V_{CC} values of 4.5 volts and 5.5 volts.



Illustrated above is the following sequence:

1) It is desired to program the selected address with 0111 (Q0-Q3). Only outputs Q1, Q2 and Q3 need programming.
2) Q1 is verified to be at a low logic level and then the programming sequence is executed. The output is then verified to be at a high logic level.
3) Q2 is an example of an output requiring three attempts to be programmed successfully.
4) Q3 is programmed to a high logic level.

FIGURE 1. SERIES 3 PROGRAMMING SEQUENCE

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

recommended operating conditions

PARAMETER		MILITARY			COMMERCIAL			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−2			−3.2	mA
I_{OL}	Low-level output current			16			16	mA
T_A	Operating free-air temperature range	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		MILITARY			COMMERCIAL			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = MIN,	I_{OH} = MAX	2.4	3.1		2.4	3.1		V
V_{OL}	V_{CC} = MIN,	I_{OL} = 16 mA			0.5			0.5	V
I_{OZH}	V_{CC} = MAX,	V_O = 2.4 V			50			50	μA
I_{OZL}	V_{CC} = MAX,	V_O = 0.5 V			−50			−50	μA
I_I	V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.7 V			25			25	μA
I_{IL}	V_{CC} = MAX,	V_I = 0.5 V			−0.25			−0.25	mA
I_O§	V_{CC} = MAX,	V_O = 2.25 V		60			60		mA
I_{CC}	V_{CC} = MAX			55			55	160	mA

†For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics over recommended ranges of T_A and V_{CC} (unless otherwise noted)

TYPE		TEST CONDITIONS	$t_{a(A)}$ ACCESS TIME FROM ADDRESS			$t_{a(S)}$ ACCESS TIME FROM ENABLE			t_{dis} DISABLE TIME			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	MIN	TYP†	MAX	
TBP34S1-20	Military	C_L = 30 pf See Note 2		12			6			5		ns
	Commercial			12			6			5		ns
TBP34S1	Military			15			6			5		ns
	Commercial			15			6			5		ns

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

4 PROMs

recommended operating conditions

PARAMETER		MILITARY			COMMERCIAL			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−1.6			−1.6	mA
I_{OL}	Low-level output current			8			8	mA
T_A	Operating free-air temperature range	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		MILITARY			COMMERCIAL			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = MIN,	I_{OH} = −1.6 mA	2.4	3.1		2.4	3.1		V
V_{OL}	V_{CC} = MIN,	I_{OL} = 8 mA			0.5			0.5	V
I_{OZH}	V_{CC} = MAX,	V_O = 2.4 V			50			50	μA
I_{OZL}	V_{CC} = MAX,	V_O = 0.5 V			−50			−50	μA
I_I	V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.7 V			25			25	μA
I_{IL}	V_{CC} = MAX,	V_I = 0.5 V			−0.25			−0.25	mA
I_O§	V_{CC} = MAX,	V_O = 2.25 V		60			60		mA
I_{CC}	V_{CC} = MAX			30			30		mA

†For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics over recommended ranges of T_A and V_{CC} (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MILITARY			COMMERCIAL			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
$t_{a(A)}$	Access time from address	C_L = 30 pF See Note 2		25			25		ns
$t_{a(S)}$	Access time from chip select (enable time)			15			15		ns
t_{dis}	Disable time			15			15		ns

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

recommended operating conditions

PARAMETER		MILITARY			COMMERCIAL			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			16			16	mA
T_A	Operating free-air temperature range	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		MILITARY			COMMERCIAL			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN,	I_I = −18 mA			−1.2			−1.2	V
I_{OH}	V_{CC} = MIN,	V_{OH} = 2.4 V			0.05			0.05	mA
		V_{OH} = 5.5 V			0.1			0.1	
V_{OL}	V_{CC} = MIN,	I_{OL} = 16 mA			0.5			0.5	V
I_I	V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.7 V			25			25	μA
I_{IL}	V_{CC} = MAX,	V_I = 0.5 V			−0.25			−0.25	mA
I_{CC}	V_{CC} = MAX			55			55		mA

†For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions.

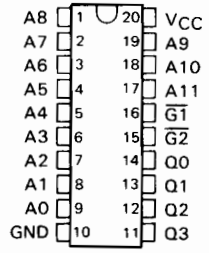
switching characteristics over recommended ranges of T_A and V_{CC} (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MILITARY			COMMERCIAL			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
$t_{a(A)}$	Access time from address	C_L = 30 pF See Note 2		15			15		ns
$t_{a(S)}$	Access time from chip select (enable time)			9			9		ns
t_{PLH}	Propagation delay time, low-to-high-level output from chip select			8			8		ns

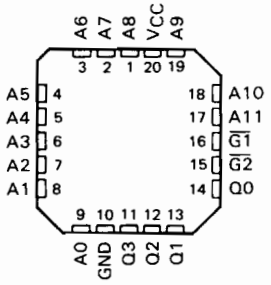
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

- **Fastest Schottky PROM Family**
- **High-Speed Access Times**
- **Low-Power, 3-State, and Open-Collector Options Available**
- **Titanium-Tungsten (Ti-W) Fuse Links for Reliable Low-Voltage Programming**
- **Applications Include:**
  Microprogramming/Firmware Loaders
  Code Converters/Character Generators
  Translators/Emulators
  Address Mapping/Look-Up Tables

TBP34S162, TBP34L162, TBP34SA162
N OR J PACKAGE
(TOP VIEW)



TBP34S16X, TBP34L16X, TBP34SA16X
FN OR FK PACKAGE
(TOP VIEW)



NC—No internal connection

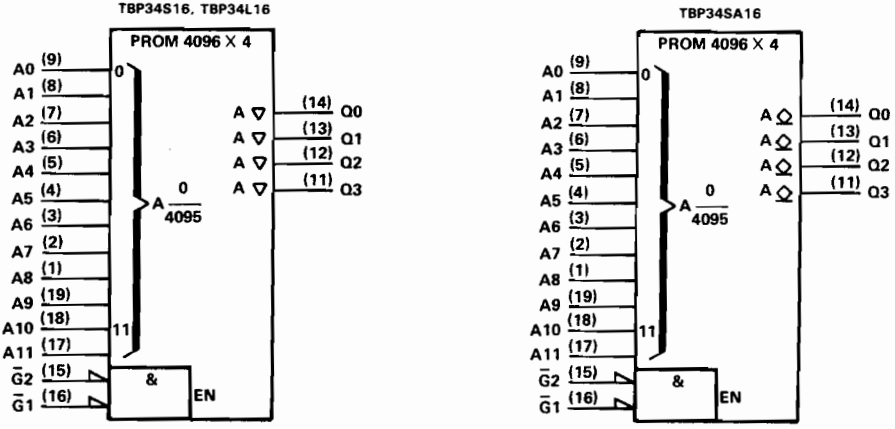
description

These Series-3 monolithic TTL programmable read-only memories (PROMs) feature high-speed access times and dependable titanium-tungsten fuse link program elements. They are organized as 4096 words by 4 bits each, providing a total of 16,384 bits. The '34S16 has three-state outputs. The '34SA16 is the open-collector version and allows the device to be connected directly to data buses utilizing passive pull-up resistors. The low-power '34L16 is available for applications that require power conservation while maintaining bipolar speeds. It also has three-state outputs.

Data is programmed at any bit location with the standard Series 3 programming algorithm. The program elements store a logic level low before any programming, and are permanently set to a logic level high after programming. After execution of the programming procedure, the output for that bit location cannot be reversed. The Series 3 programming procedure should be referred to for further details. Additional circuitry has been designed into these devices to improve testability and insure high programmability.

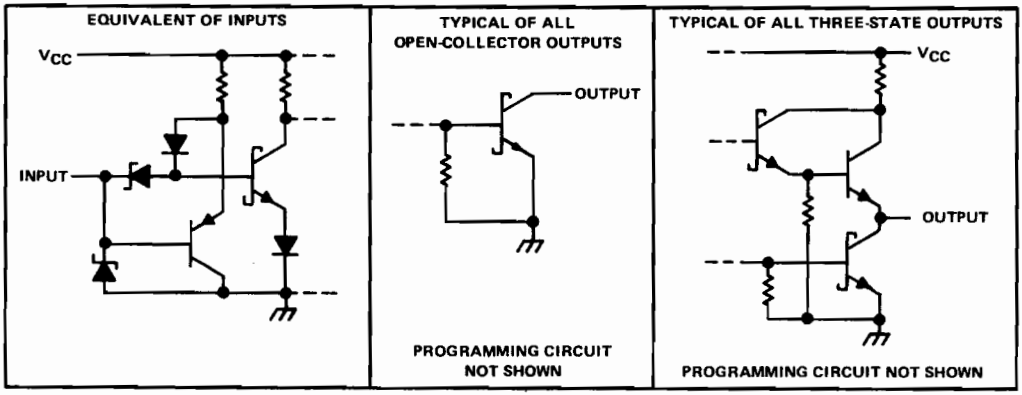
4 PROMs

logic symbols



Pin numbers shown are for J or N packages.

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Off-state output voltage . . . . . 5.5 V
Operating free-air temperature range: Military-temperature-range circuits . . . . . −55°C to 125°C
Commercial-temperature-range circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal. The supply voltage rating does not apply during programming.

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

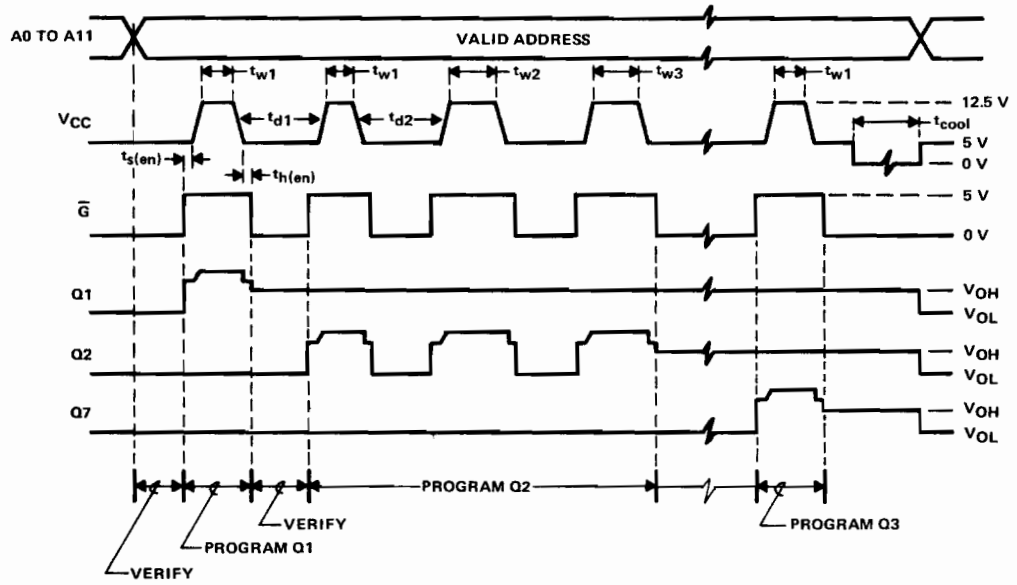
recommended operating conditions for programming (see Figure 1)

			MIN	NOM	MAX	UNIT
Supply voltage during verification		V_{CC}	4.5	5	5.5	V
Input voltage		V_{IH}	3	4	5	V
		V_{IL}	0	0.2	0.5	
Enable voltage during verification		$\overline{G}1$, $\overline{G}2$	0	0.2	0.4	V
Enable inactive voltage during programming		$\overline{G}1$, $\overline{G}2$	4.5	5	5.5	V
V_{CC} program pulse amplitude		$V_{CC(pr)}$	12	12.5	13	V
V_{CC} program pulse duration	1st attempt	t_{w1}	10	11	12	μs
	2nd attempt	t_{w2}	20	22	25	
	3rd attempt	t_{w3}	20	22	25	
Enable set-up time‡ before $V_{CC(pr)}$		$t_{s(en)}$	0.1	0.5	1	μs
Enable hold time‡ after $V_{CC(pr)}$		$t_{h(en)}$	0.1	0.5	1	μs
Rise time of $V_{CC(pr)}$§		$t_{r(VCC)}$	0.3	0.4	0.5	μs
Fall time of $V_{CC(pr)}$¶		$t_{f(VCC)}$	0.05	0.1	0.2	μs
Delay time between successive $V_{CC(pr)}$ pulses		t_{d1}	10	20	30	μs
Delay time between successive $V_{CC(pr)}$ pulses		t_{d2}	10	20	30	μs
Cooling time between words		t_{cool}	100	150	200	μs
Free-air temperature		T_A	20	25	30	°C

†Measured from 1.5 V on enable pin to 5.5 V on $V_{CC(pr)}$
‡Measured from 5.5 V on $V_{CC(pr)}$ to 1.5 V on enable pin
§Measured from 5 V to 12 V
¶Measured from 12 V to 5 V

step-by-step programming instructions (see Figure 1)

1. Address the word to be programmed, apply 5 volts to V_{CC} and active levels to all enable inputs ($\overline{G}1$, $\overline{G}2$).
2. Verify the selected bit location that requires programming. Note: The only bit positions that require programming are outputs needing a high logic level.
3. For bit locations that do not require programming, go to step 2 for the next bit, or to step 1 for next word.
4. Deselect PROM by applying 5 volts to $\overline{G}1$ or $\overline{G}2$.
5. Connect a 4-mA current source (clamped to V_{CC}) to the output that is to be programmed.
6. Increase V_{CC} to $V_{CC(pr)}$ for a pulse duration equal to t_{wX} (where X is determined by the number of programming attempts, i.e., 1,2,3). Minimum current capability for the V_{CC} power supply should be 400 mA.
7. Verify that the output has been programmed to a high logic level. If the output has been programmed correctly, go to the next bit. If not, repeat step 2 through step 7 and increment X (where X is equal to 1 on the first programming attempt). If the output has not been programmed by the third attempt, stop programming and go to a new device.
8. Verify programming of every word after all words have been programmed using V_{CC} values of 4.5 volts and 5.5 volts.



Illustrated above is the following sequence:

1) It is desired to program the selected address with 0111 (Q0-Q3). Only outputs Q1, Q2 and Q3 need programming.
2) Q1 is verified to be at a low logic level and then the programming sequence is executed. The output is then verified to be at a high logic level.
3) Q2 is an example of an output requiring three attempts to be programmed successfully.
4) Q3 is programmed to a high logic level.

FIGURE 1. SERIES 3 PROGRAMMING SEQUENCE

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

recommended operating conditions

PARAMETER		MILITARY			COMMERCIAL			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−2			−3.2	mA
I_{OL}	Low-level output current			16			16	mA
T_A	Operating free-air temperature range	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		MILITARY			COMMERCIAL			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = MIN,	I_{OH} = MAX	2.4	3.1		2.4	3.1		V
V_{OL}	V_{CC} = MIN,	I_{OL} = 16 mA			0.5			0.5	V
I_{OZH}	V_{CC} = MAX,	V_O = 2.4 V			50			50	μA
I_{OZL}	V_{CC} = MAX,	V_O = 0.5 V			−50			−50	μA
I_I	V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.7 V			25			25	μA
I_{IL}	V_{CC} = MAX,	V_I = 0.5 V			−0.25			−0.25	mA
I_O§	V_{CC} = MAX,	V_O = 2.25 V	60			60			mA
I_{CC}	V_{CC} = MAX			95			95		mA

†For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics over recommended ranges of T_A and V_{CC} (unless otherwise noted)

TYPE		TEST CONDITIONS	$t_{a(A)}$ ACCESS TIME FROM ADDRESS			$t_{a(S)}$ ACCESS TIME FROM ENABLE			t_{dis} DISABLE TIME			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	MIN	TYP†	MAX	
TBP34S16-30	Military	C_L = 30 pf See Note 2		18			10			10		ns
	Commercial			18			10			10		ns
TBP34S16	Military			20			10			10		ns
	Commercial			20			10			10		ns

‡All typical values are at V_{CC} = 5 V, T_A = 25°.
NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

recommended operating conditions

PARAMETER		MILITARY			COMMERCIAL			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−1.6			−1.6	mA
I_{OL}	Low-level output current			8			8	mA
T_A	Operating free-air temperature range	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		MILITARY			COMMERCIAL			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = MIN,	I_{OH} = −1.6 mA	2.4	3.1		2.4	3.1		V
V_{OL}	V_{CC} = MIN,	I_{OL} = 8 mA			0.5			0.5	V
I_{OZH}	V_{CC} = MAX,	V_O = 2.4 V			50			50	μA
I_{OZL}	V_{CC} = MAX,	V_O = 0.5 V			−50			−50	μA
I_I	V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.7 V			25			25	μA
I_{IL}	V_{CC} = MAX,	V_I = 0.5 V			−0.25			−0.25	mA
I_O§	V_{CC} = MAX,	V_O = 2.25 V		60			60		mA
I_{CC}	V_{CC} = MAX			55			55		mA

†For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics over recommended ranges of T_A and V_{CC} (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MILITARY			COMMERCIAL			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
$t_{a(A)}$	Access time from address	C_L = 30 pF See Note 2		35			35		ns
$t_{a(S)}$	Access time from chip select (enable time)			20			20		ns
t_{dis}	Disable time			20			20		ns

‡All typical values are at V_{CC} = 5 V, T_A = 25°.
NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

recommended operating conditions

PARAMETER		MILITARY			COMMERCIAL			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			16			16	mA
T_A	Operating free-air temperature range	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		MILITARY			COMMERCIAL			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN,	I_I = −18 mA			−1.2			−1.2	V
I_{OH}	V_{CC} = MIN,	V_{OH} = 2.4 V			0.05			0.05	mA
		V_{OH} = 5.5 V			0.1			0.1	
V_{OL}	V_{CC} = MIN,	I_{OL} = 16 mA			0.5			0.5	V
I_I	V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.7 V			25			25	μA
I_{IL}	V_{CC} = MAX,	V_I = 0.5 V			−0.25			−0.25	mA
I_{CC}	V_{CC} = MAX			95			95		mA

†For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions.

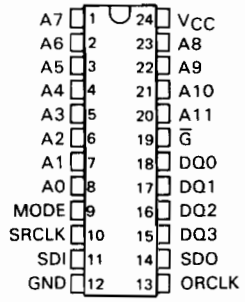
switching characteristics over recommended ranges of T_A and V_{CC} (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MILITARY			COMMERCIAL			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
$t_{a(A)}$	Access time from address	C_L = 30 pF See Note 2		25			25		ns
$t_{a(S)}$	Access time from chip select (enable time)			12			12		ns
t_{PLH}	Propagation delay time, low-to-high-level output from chip select			10			10		ns

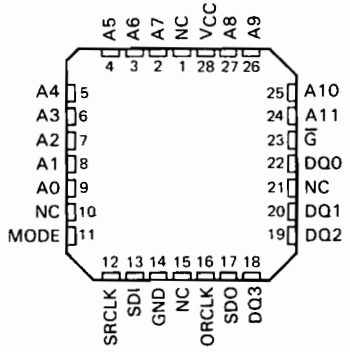
‡All typical values are at V_{CC} = 5 V, T_A = 25°.
NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

- **Fastest Schottky PROM Family**
- **High-Speed Access Times**
- **Allows Storage of Output Data**
- **Applications Include:**
  Microprogram Control Store with Built-In System Diagnostic Testing
  Serial Character Generator
  Parallel In/Serial Out Memory

TBP34SR165 . . . JT OR NT PACKAGE
(TOP VIEW)



TBP34SR16X . . . FN OR FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

The TBP34SR16 is a series-3 monolithic TTL programmable read-only memory (PROM) featuring high-speed access times and dependable titanium-tungsten fuse link program elements. It is organized as 4096 words by 4 bits each, providing 16,384 bits.

The TBP34SR16 features a 4-bit shadow register that allows diagnostic observation and control without introducing intermediate illegal states. It is loaded on the rising edge of SRCLK from either the output register or the serial data input (SDI). In addition, it can be loaded with parallel data from the outputs. The output register receives data from either the PROM array or the shadow register as determined by the mode control input. The output register is loaded on the rising edge of ORCLK. The mode-dependent function table should be referred to for further details.

During diagnostics, data loaded into the output register from the PROM array can be parallel-loaded into the shadow register and serially shifted out through the SDO output. This allows observation of the system without introducing intermediate illegal states. Similarly, diagnostic data can be serially loaded into the shadow register and parallel-loaded into the output register. This allows control and test scanning to be imposed on the system.

Data is programmed at any bit location with the standard series 3 programming algorithm. The program elements store a low logic level before any programming, and are permanently set to a high logic level after programming. After execution of the programming procedure, the output for that bit location cannot be reversed. The series 3 programming procedure should be referred to for further details. Additional circuits have been designed into these devices to improve testability and ensure high programmability.

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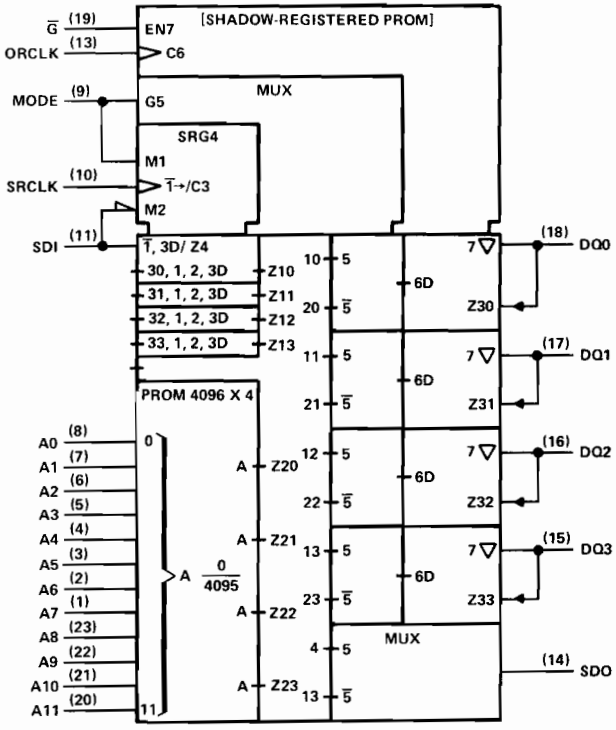
logic symbol



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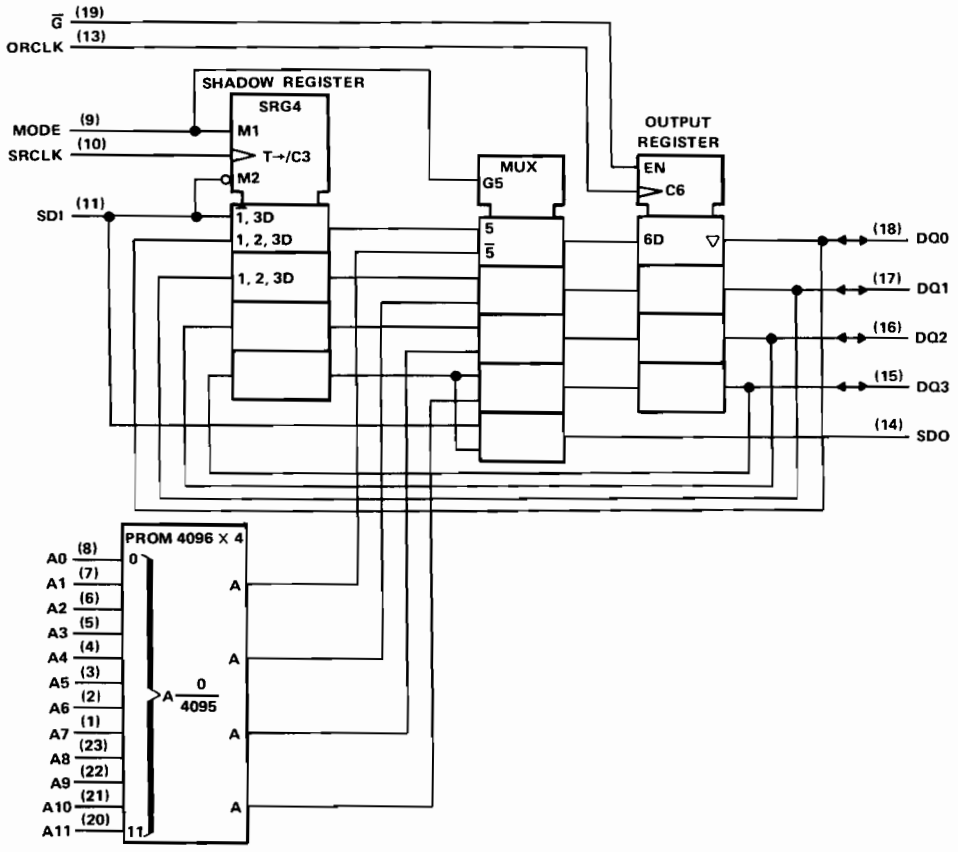
logic diagram (positive logic)



Pin numbers shown are for JT and NT packages.

MODE-DEPENDENT TERMINAL FUNCTIONS

TERMINAL	FUNCTION WHEN MODE INPUT IS HIGH	FUNCTION WHEN MODE INPUT IS LOW
SRCLK	Low-to-high transition loads data into shadow register under SDI control.	Low-to-high transition shifts data present on the SDI input into the shadow register.
SDI	If SDI is high, shadow register does nothing. If SDI is low, data may be clocked into shadow register from output bus.	Serial input to shadow register LSB
SDO	Output for data directly from SDI for cascading other shadow-registered PROMs	Output for shadow register MSB
RCLK	Low-to-high transition loads output register from shadow register.	Low-to-high transition loads output register from PROM array.

OTHER TERMINAL FUNCTIONS

TERMINALS	FUNCTION
A0 – A11	Address inputs for data from PROM array
$\overline{G}$	If $\overline{G}$ is high, DQ0 thru DQ11 are in high-impedance state and can accept external data for shadow register. If $\overline{G}$ is low, DQ0 thru DQ11 are outputs for data from output register.
DQ0–DQ3	Input/output ports under control of $\overline{G}$

recommended operating conditions for programming (see Figure 1)

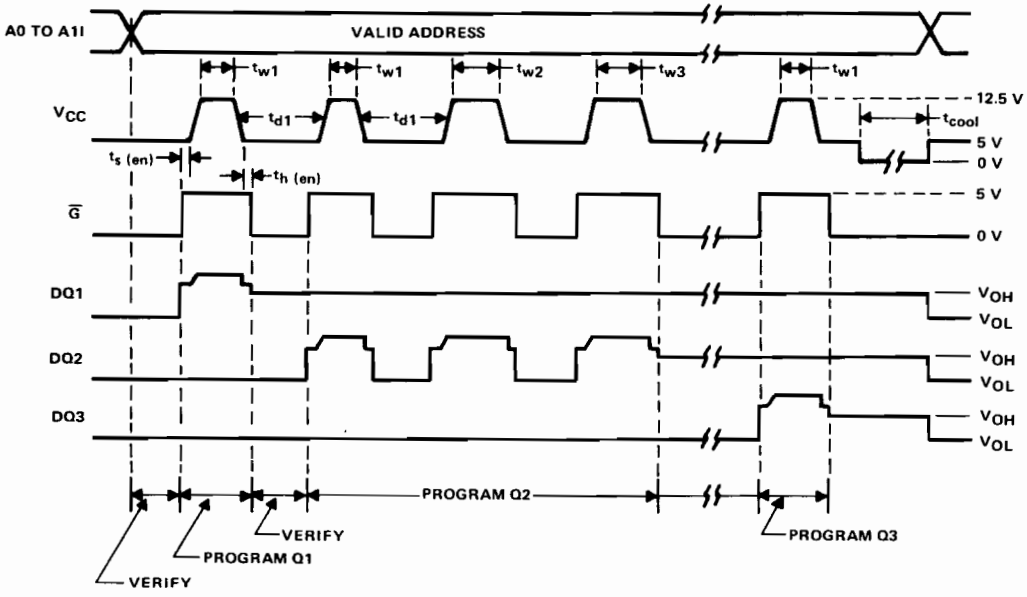
		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage during verification	4.5	5	5.5	V
V_{IH}	High-level input voltage	3	4	5	V
V_{IL}	Low-level input voltage	0	0.2	0.4	V
	Enable $\overline{G}$ voltage during verification	0	0.2	0.4	V
	Enable $\overline{G}$ inactive voltage during programming	4.5	5	5.5	V
$V_{CC(pr)}$	Supply voltage program pulse amplitude	12	12.5	13	V
t_{w1}	V_{CC} program pulse duration, 1st attempt	10	11	12	μs
t_{w2}	V_{CC} program pulse duration, 2nd attempt	20	22	25	μs
t_{w3}	V_{CC} program pulse duration, 3rd attempt	20	22	25	μs
t_{su}	Setup time, enable $\overline{G}$ low before $V_{CC(pr)}$ †	0.1	0.5	1	μs
t_h	Hold time, enable $\overline{G}$ low after $V_{CC(pr)}$ ‡	0.1	0.5	1	μs
$t_{r(VCC)}$	Rise time, $V_{CC(pr)}$ (5 V to 12 V)	0.3	0.4	0.5	μs
$t_{f(VCC)}$	Fall time, $V_{CC(pr)}$ (12 V to 5 V)	0.05	0.1	0.2	μs
t_d	Delay time between successive $V_{CC(pr)}$ pulses	10	20	30	μs
t_{cool}	Cooling time between words	100	150	200	μs
T_A	Free-air temperature	20	25	30	°C

†Measured from 1.5 V on enable pin to 5.5 V on $V_{CC(pr)}$.
‡Measured from 5.5 V on $V_{CC(pr)}$ to 1.5 V on enable pin.

step-by-step programming instructions (see Figure 1)

1. Address the word to be programmed, apply 5 V to V_{CC} and a low logic level to the G input.
2. Verify the selected bit location that requires programming. Note: The only bit positions that require programming are outputs to be at a high logic level.
3. For bit locations that do not require programming, go to step 2 for the next bit, or to step 1 for the next word.
4. Deselect PROM by applying 5 V to G.
5. Connect a 4-mA current source (clamped to V_{CC}) to the output to be programmed.
6. Increase V_{CC} to $V_{CC(pr)}$ for a pulse duration equal to t_{wX} (where X is determined by the number of programming attempts, i.e., 1, 2, 3). Minimum current capability for the V_{CC} power supply should be 400 mA.
7. Verify that the output has been programmed to a high logic level. If the output has been programmed correctly, go to the next bit. If not, repeat steps 2 through 7 and increment X (where X equals 1 on the first programming attempt). If the output has not been programmed by the third attempt, stop programming and go to a new device.
8. Verify programming of every word after all words have been programmed using V_{CC} values of 4.5 volts and 5.5 volts.

series 3 programming sequence



Illustrated above is the following sequence:

1) It is desired to program the selectd address with 0111 (Q0-Q3). Only outputs DQ1, DQ2, and DQ3 need programming.
2) Q1 is verified to be at a low logic level and then the programming sequence is executed. The output is then verified to be at a high logic level.
3) DQ2 is an example of an output requiring three attempts to be programmed successfully.
4) DQ3 is programmed to a high logic level.

FIGURE 1. SERIES 3 PROGRAMMING SEQUENCE

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage, V_I . . . . . 5.5 V
Off-state output voltage, $V_{O(off)}$ . . . . . 5.5 V
Operating free-air temperature range: Military-temperature-range circuits . . . . . −55°C to 125°C
Commercial-temperature-range circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: All voltage values are with respect to network ground terminal. The supply voltage rating does not apply during programming.

recommended operating conditions

PARAMETER			MILITARY			COMMERCIAL			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level input current				−2			−3.2	mA
I_{OL}	Low-level input current				16			16	mA
f_{clock}	Clock frequency, SRCLK (MODE = L)								MHz
t_w	Pulse duration	SRCLK high							ns
		SRCLK low							
		ORCLK high							
		ORCLK low							
t_{su}	Setup time	DQ3 thru DQ0 before SRCLK↑ ($\overline{G}$ and MODE = H, SDI = L)							ns
		SDI and MODE before SRCLK↑							
		Address before ORCLK↑ (MODE = L)							
		MODE before ORCLK↑							
		SRCLK↑ before ORCLK↑ ($\overline{G}$ and MODE = H, SDI = L)							
t_h	Hold time	DQ3 – DQ0 after SRCLK↑ ($\overline{G}$ and MODE = H, SDI = L)							ns
		SDI and MODE after SRCLK↑ or ORCLK↑							
		Address after ORCLK↑ (MODE = L)							
		MODE after ORCLK↑							
T_A	Operating free-air temperature range		−55		125	0		70	°C

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		MILITARY			COMMERCIAL			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = MIN,	I_{OH} = MAX	2.4	3.1		2.4	3.1		V
V_{OL}	V_{CC} = MIN,	I_{OL} = 16 mA			0.5			0.5	V
I_{OZH}	V_{CC} = MAX,	V_O = 2.4 V			50			50	μA
I_{OZL}	V_{CC} = MAX,	V_O = 0.5 V			−50			−50	μA
I_I	V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.7 V			25			25	μA
I_{IL}	V_{CC} = MAX,	V_I = 0.5 V			−0.25			−0.25	mA
I_O§	V_{CC} = MAX,	V_O = 2.25 V	60			60			mA
I_{CC}	V_{CC} = MAX,			120			120		mA

switching characteristics over recommended ranges of T_A and V_{CC} (unless otherwise noted)

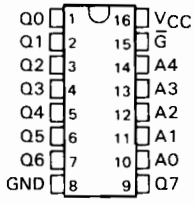
PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITION (See Note 2)	MILITARY			COMMERCIAL			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
f_{max}	SRCLK (MODE = L)		C_L = 30 pF							MHz
t_{pd}	ORCLK	DQ0 – DQ3								
t_{pd}	SRCLK (MODE = L)	SDO								
t_{pd}	SDI (MODE = H)	SDO								ns
t_{pd}	MODE (SDI = L)									
t_{en}	$\overline{G}$	DQ0 – DQ3								
t_{dis}	$\overline{G}$	DQ0 – DQ3								ns

†For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
NOTE 2: Load circuits and voltage waveforms are shown in Section 1 of *The TTL Data Book, Volume 4*, 1985.

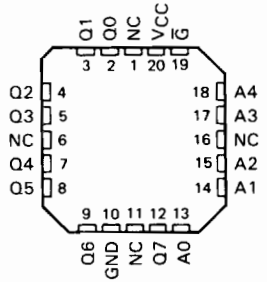
D2852, AUGUST 1984 – REVISED DECEMBER 1984

- **Fastest Schottky PROM Family**
- **High-Speed Access Times**
- **Low-Power, Open-Collector, and 3-State Options Available**
- **Titanium-Tungsten (Ti-W) Fuse Links for Reliable Low-Voltage Programming**
- **P-N-P Inputs for Reduced Loading on System Buffers/Drivers**
- **Applications Include:**
  Microprogramming/Firmware Loaders
  Code Converters/Character Generators
  Translators/Emulators
  Address Mapping/Look-Up Tables
- **Package Options Include 16-Pin DIP, and 20-Pin Chip-Carrier**

TBP38L030, TBP38S030, TBP38SA030 . . . J OR N PACKAGE
(TOP VIEW)



TBP38L03X, TBP38S03X, TBP38SA03X . . . FN OR FK PACKAGE
(TOP VIEW)



NC—No internal connection

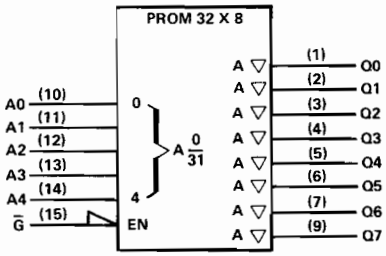
description

These Series-3 monolithic TTL programmable read-only memories (PROMs) feature high-speed access times and dependable titanium-tungsten fuse link program elements. They are organized as 32 words by 8 bits each, providing a total of 256 bits. The '38S030 has three-state outputs. The '38SA030 is the open-collector version and allows the device to be connected directly to data buses utilizing passive pull-up resistors. The low-power '38L030 is available for applications that require power conservation while maintaining bipolar speeds.

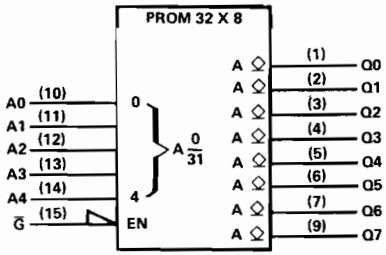
Data is programmed at any bit location with the standard Series 3 programming algorithm. The program elements store a logic level low before any programming, and are permanently set to a logic level high after programming. After execution of the programming procedure, the output for that bit location cannot be reversed. The Series 3 programming procedure should be referred to for further details. Additional circuitry has been designed into these devices to improve testability and insure high programmability.

logic symbols

TBP38S030, TBP38L030

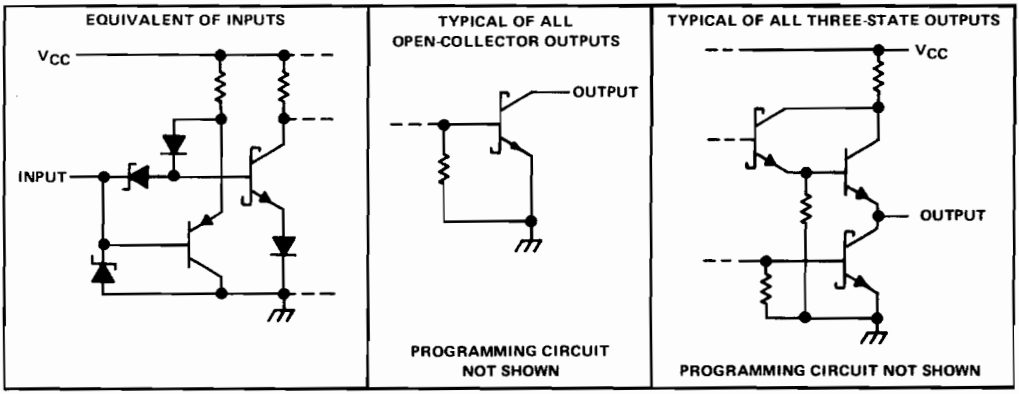


TBP38SA030



Pin numbers shown are for J and N packages.

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Off-state output voltage . . . . . 5.5 V
Operating free-air temperature range: Military-temperature-range circuits . . . . . −55°C to 125°C
Commercial-temperature-range circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal. The supply voltage rating does not apply during programming.

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

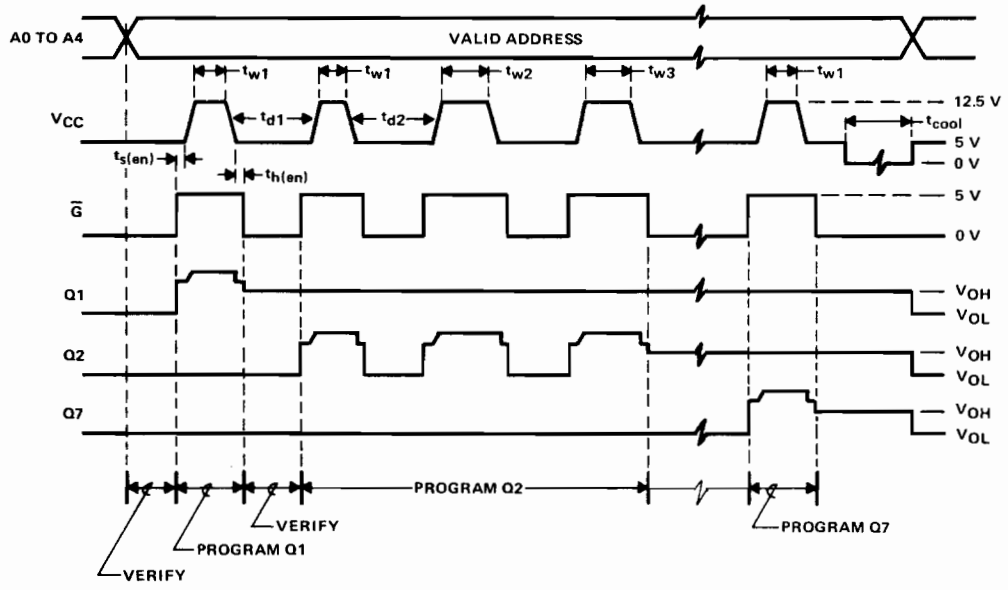
recommended operating conditions for programming (see Figure 1)

			MIN	NOM	MAX	UNIT
Supply voltage during verification		V_{CC}	4.5	5	5.5	V
Input voltage		V_{IH}	3	4	5	V
		V_{IL}	0	0.2	0.5	
Enable voltage during verification		$\overline{G}$	0	0.2	0.4	V
Enable inactive voltage during programming		$\overline{G}$	4.5	5	5.5	V
V_{CC} program pulse amplitude		$V_{CC(pr)}$	12	12.5	13	V
V_{CC} program pulse duration	1st attempt	t_{w1}	10	11	12	μs
	2nd attempt	t_{w2}	20	22	25	
	3rd attempt	t_{w3}	20	22	25	
Enable set-up time† before $V_{CC(pr)}$		$t_{s(en)}$	0.1	0.5	1	μs
Enable hold time‡ after $V_{CC(pr)}$		$t_{h(en)}$	0.1	0.5	1	μs
Rise time of $V_{CC(pr)}$§		$t_r(V_{CC})$	0.3	0.4	0.5	μs
Fall time of $V_{CC(pr)}$¶		$t_f(V_{CC})$	0.05	0.1	0.2	μs
Delay time between successive $V_{CC(pr)}$ pulses		t_{d1}	10	20	30	μs
Hold time between successive $V_{CC(pr)}$ pulses		t_{d2}	10	20	30	μs
Cooling time between words		t_{cool}	100	150	200	μs
Free-air temperature		T_A	20	25	30	°C

†Measured from 1.5 V on enable pin to 5.5 V on $V_{CC(pr)}$
‡Measured from 5.5 V on $V_{CC(pr)}$ to 1.5 V on enable pin
§Measured from 5 V to 12 V
¶Measured from 12 V to 5 V

step-by-step programming instructions (see Figure 1)

1. Address the word to be programmed, apply 5 volts to V_{CC} and a low-logic-level voltage to the enable $\overline{G}$ input.
2. Verify the selected bit location that requires programming. Note: The only bit positions that require programming are outputs needing a high logic level.
3. For bit locations that do not require programming, go to step 2 for the next bit, or to step 1 for next word.
4. Deselect PROM by applying 5 volts to $\overline{G}$.
5. Connect a 4-mA current source (clamped to V_{CC}) to the output that is to be programmed.
6. Increase V_{CC} to $V_{CC(pr)}$ for a pulse duration equal to t_{wX} (where X is determined by the number of programming attempts, i.e., 1,2,3). Minimum current capability for the V_{CC} power supply should be 400 mA.
7. Verify that the output has been programmed to a high logic level. If the output has been programmed correctly, go to the next bit. If not, repeat step 2 through step 7 and increment X (where X is equal to 1 on the first programming attempt). If the output has not been programmed by the third attempt, stop programming and go to a new device.
8. Verify programming of every word after all words have been programmed using V_{CC} values of 4.5 volts and 5.5 volts.



Illustrated above is the following sequence:

1) It is desired to program the selected address with 01100001 (Q0-Q7). Only outputs Q1, Q2 and Q7 need programming.
2) Q1 is verified to be at a low logic level and then the programming sequence is executed. The output is then verified to be at a high logic level.
3) Q2 is an example of an output requiring three attempts to be programmed successfully.
4) Q7 is programmed to a high logic level.

FIGURE 1. SERIES 3 PROGRAMMING SEQUENCE

recommended operating conditions

	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−2			−3.2	mA
I_{OL}	Low-level output current			16			16	mA
T_A	Operating free-air temperature range	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		MILITARY			COMMERCIAL			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = MIN,	I_{OH} = MAX	2.4	3.1		2.4	3.1		V
V_{OL}	V_{CC} = MIN,	I_{OL} = 16 mA			0.5			0.5	V
I_{OZH}	V_{CC} = MAX,	V_O = 2.4 V			50			50	μA
I_{OZL}	V_{CC} = MAX,	V_O = 0.5 V			−50			−50	μA
I_I	V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.7 V			25			25	μA
I_{IL}	V_{CC} = MAX,	V_I = 0.5 V			−0.25			−0.25	mA
I_O§	V_{CC} = MAX,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	V_{CC} = MAX			80	125		80	125	mA

†For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics over recommended ranges of T_A and V_{CC} (unless otherwise noted)

TYPE		TEST CONDITIONS	$t_{a(A)}$ ACCESS TIME FROM ADDRESS			$t_{a(S)}$ ACCESS TIME FROM ENABLE			t_{dis} DISABLE TIME			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
TBP38S030-20	Military	C_L = 30 pF See Note 2		10	20		5	15		3	10	ns
TBP38S030-15	Commercial			10	15		5	12		3	8	ns
TBP38S030-30	Military			10	30		5	15		3	10	ns
TBP38S030-25	Commercial			10	25		5	12		3	8	ns

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

4 PROMs

recommended operating conditions

PARAMETER		MILITARY			COMMERCIAL			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−1.6			−1.6	mA
I_{OL}	Low-level output current			8			8	mA
T_A	Operating free-air temperature range	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		MILITARY			COMMERCIAL			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = MIN,	I_{OH} = −1.6 mA	2.4	3.1		2.4	3.1		V
V_{OL}	V_{CC} = MIN,	I_{OL} = 8 mA			0.5			0.5	V
I_{OZH}	V_{CC} = MAX,	V_O = 2.4 V			50			50	μA
I_{OZL}	V_{CC} = MAX,	V_O = 0.5 V			−50			−50	μA
I_I	V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.7 V			25			25	μA
I_{IL}	V_{CC} = MAX,	V_I = 0.5 V			−0.25			−0.25	mA
I_O§	V_{CC} = MAX,	V_O = 2.25 V		80			80		mA
I_{CC}	V_{CC} = MAX			45			45		mA

†For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics over recommended ranges of T_A and V_{CC} (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MILITARY			COMMERCIAL			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
$t_{a(A)}$	Access time from address	C_L = 30 pF See Note 2			20			20	ns
$t_{a(S)}$	Access time from chip select (enable time)				15			15	ns
t_{dis}	Disable time				12			12	ns

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

recommended operating conditions

PARAMETER		MILITARY			COMMERCIAL			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			16			16	mA
T_A	Operating free-air temperature range	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		MILITARY			COMMERCIAL			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN,	I_I = −18 mA			−1.2			−1.2	V
I_{OH}	V_{CC} = MIN,	V_{OH} = 2.4 V			0.05			0.05	mA
		V_{OH} = 5.5 V			0.1			0.1	
V_{OL}	V_{CC} = MIN,	I_{OL} = 16 mA			0.5			0.5	V
I_I	V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.7 V			25			25	μA
I_{IL}	V_{CC} = MAX,	V_I = 0.5 V			−0.25			−0.25	mA
I_{CC}	V_{CC} = MAX			80	125		80	125	mA

†For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions.

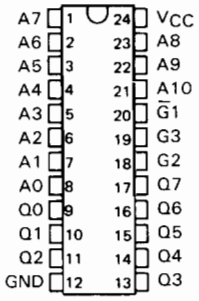
switching characteristics over recommended ranges of T_A and V_{CC} (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MILITARY			COMMERCIAL			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
$t_{a(A)}$	Access time from address	C_L = 30 pF See Note 2		15	25		15	20	ns
$t_{a(S)}$	Access time from chip select (enable time)			10	20		10	15	ns
t_{PLH}	Propagation delay time, low-to-high-level output from chip select			9	18		9	14	ns

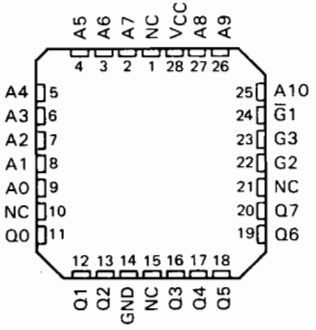
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

- **Fastest Schottky PROM Family**
- **High-Speed Access Times**
- **Low-Power, 3-State, and Open-Collector Options Available**
- **Titanium-Tungsten (Ti-W) Fuse Links for Reliable Low-Voltage Programming**
- **Applications Include:**
  Microprogramming/Firmware Loaders
  Code Converters/Character Generators
  Translators/Emulators
  Address Mapping/Look-Up Tables
- **Package Options Include 300-Mil or 600-Mil 24-Pin DIP, and 28-Pin Chip-Carrier Packages**

TBP38L165, TBP38S165, TBP38SA165 . . . NT OR JT PACKAGE
TBP38L166, TBP38S166, TBP38SA166 . . . NW OR JW PACKAGE
(TOP VIEW)



TBP38L16X, TBP38S16X, TBP38SA16X . . . FN OR FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

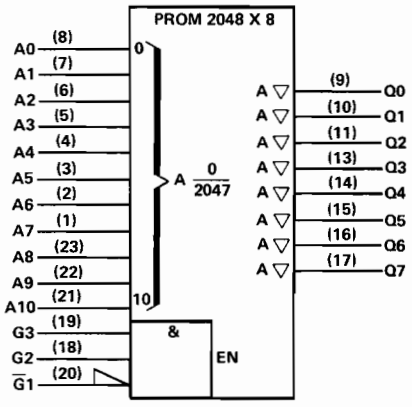
These Series-3 monolithic TTL programmable read-only memories (PROMs) feature high-speed access times and dependable titanium-tungsten fuse link program elements. They are organized as 2048 words by 8 bits each, providing a total of 16,384 bits. The '38S16 has three-state outputs. The '38SA16 is the open-collector version and allows the device to be connected directly to data buses utilizing passive pull-up resistors. The low-power '38L16 is available for applications that require power conservation while maintaining bipolar speeds. It also has three-state outputs.

Data is programmed at any bit location with the standard Series 3 programming algorithm. The program elements store a logic level low before any programming, and are permanently set to a logic level high after programming. After execution of the programming procedure, the output for that bit location cannot be reversed. The Series 3 programming procedure should be referred to for further details. Additional circuitry has been designed into these devices to improve testability and insure high programmability.

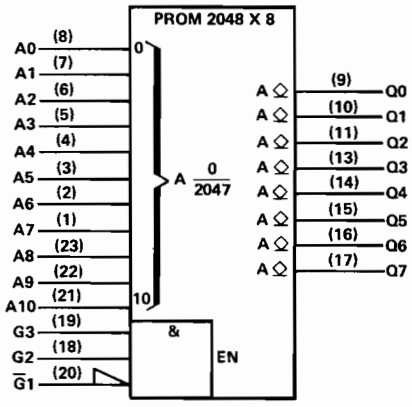
4 PROMs

logic symbols

TBP38S16, TBP38L16

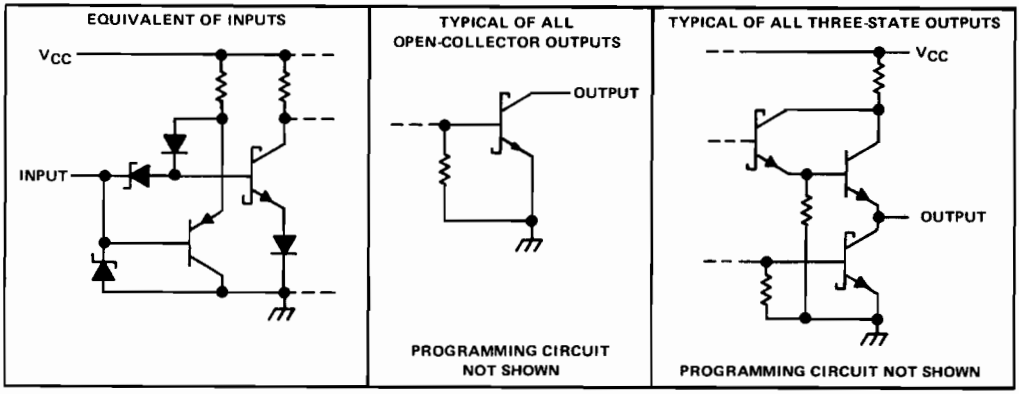


TBP38SA16



Pin numbers shown are for JT, JW, NT, or NW packages.

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Off-state output voltage . . . . . 5.5 V
Operating free-air temperature range: Military-temperature-range circuits . . . . . −55°C to 125°C
Commercial-temperature-range circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal. The supply voltage rating does not apply during programming.

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

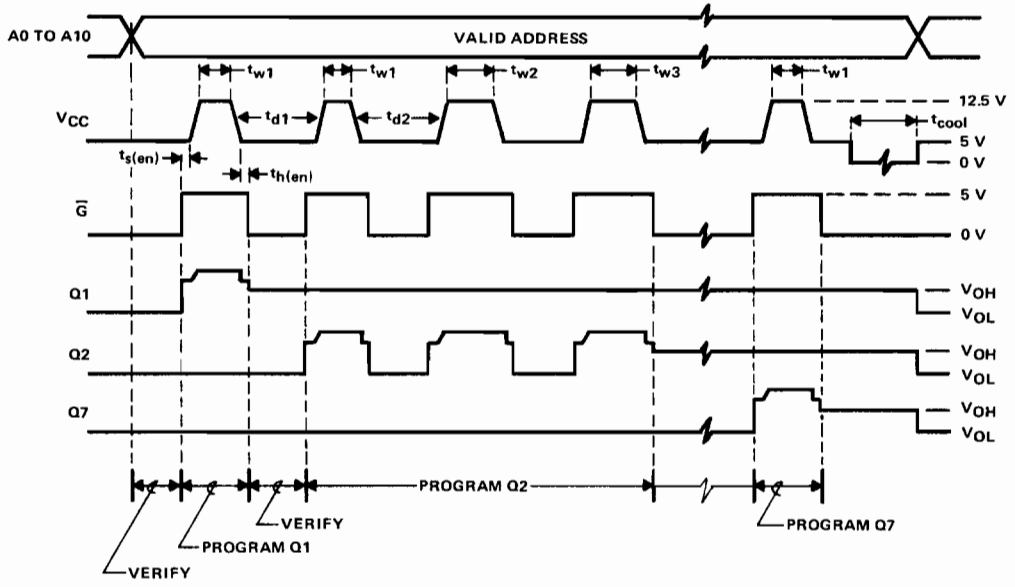
recommended operating conditions for programming (see Figure 1)

			MIN	NOM	MAX	UNIT
Supply voltage during verification		V_{CC}	4.5	5	5.5	V
Input voltage		V_{IH}	3	4	5	V
		V_{IL}	0	0.2	0.5	
Enable voltage during verification		$\overline{G}1$	0	0.2	0.4	V
		G2, G3	3	4	5	
Enable inactive voltage during programming		$\overline{G}1$	4.5	5	5.5	V
		G2, G3	0	0.2	0.4	
V_{CC} program pulse amplitude		$V_{CC(pr)}$	12	12.5	13	V
V_{CC} program pulse duration	1st attempt	t_{w1}	10	11	12	μs
	2nd attempt	t_{w2}	20	22	25	
	3rd attempt	t_{w3}	20	22	25	
Enable set-up time† before $V_{CC(pr)}$		$t_{s(en)}$	0.1	0.5	1	μs
Enable hold time‡ after $V_{CC(pr)}$		$t_{h(en)}$	0.1	0.5	1	μs
Rise time of $V_{CC(pr)}$§		$t_{r(VCC)}$	0.3	0.4	0.5	μs
Fall time of $V_{CC(pr)}$¶		$t_{f(VCC)}$	0.05	0.1	0.2	μs
Delay time between successive $V_{CC(pr)}$ pulses		t_{d1}	10	20	30	μs
Delay time between successive $V_{CC(pr)}$ pulses		t_{d2}	10	20	30	μs
Cooling time between words		t_{cool}	100	150	200	μs
Free-air temperature		T_A	20	25	30	°C

†Measured from 1.5 V on enable pin to 5.5 V on $V_{CC(pr)}$
‡Measured from 5.5 V on $V_{CC(pr)}$ to 1.5 V on enable pin
§Measured from 5 V to 12 V
¶Measured from 12 V to 5 V

step-by-step programming instructions (see Figure 1)

1. Address the word to be programmed, apply 5 volts to V_{CC} and active levels to all enable inputs ($\overline{G}1$, G2, G3).
2. Verify the selected bit location that requires programming. Note: The only bit positions that require programming are outputs needing a high logic level.
3. For bit locations that do not require programming, go to step 2 for the next bit, or to step 1 for next word.
4. Deselect PROM by applying 5 volts to $\overline{G}1$, or 0 volts to G2 or G3.
5. Connect a 4-mA current source (clamped to V_{CC}) to the output that is to be programmed.
6. Increase V_{CC} to $V_{CC(pr)}$ for a pulse duration equal to t_{wX} (where X is determined by the number of programming attempts, i.e., 1,2,3). Minimum current capability for the V_{CC} power supply should be 400 mA.
7. Verify that the output has been programmed to a high logic level. If the output has been programmed correctly, go to the next bit. If not, repeat step 2 through step 7 and increment X (where X is equal to 1 on the first programming attempt). If the output has not been programmed by the third attempt, stop programming and go to a new device.
8. Verify programming of every word after all words have been programmed using V_{CC} values of 4.5 volts and 5.5 volts.



Illustrated above is the following sequence:

1) It is desired to program the selected address with 01100001 (Q0-Q7). Only outputs Q1, Q2 and Q7 need programming.
2) Q1 is verified to be at a low logic level and then the programming sequence is executed. The output is then verified to be at a high logic level.
3) Q2 is an example of an output requiring three attempts to be programmed successfully.
4) Q7 is programmed to a high logic level.

FIGURE 1. SERIES 3 PROGRAMMING SEQUENCE

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

recommended operating conditions

PARAMETER		MILITARY			COMMERCIAL			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−2			−3.2	mA
I_{OL}	Low-level output current			16			16	mA
T_A	Operating free-air temperature range	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		MILITARY			COMMERCIAL			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = MIN,	I_{OH} = MAX	2.4	3.1		2.4	3.1		V
V_{OL}	V_{CC} = MIN,	I_{OL} = 16 mA			0.5			0.5	V
I_{OZH}	V_{CC} = MAX,	V_O = 2.4 V			50			50	μA
I_{OZL}	V_{CC} = MAX,	V_O = 0.5 V			−50			−50	μA
I_I	V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.7 V			25			25	μA
I_{IL}	V_{CC} = MAX,	V_I = 0.5 V			−0.25			−0.25	mA
I_O§	V_{CC} = MAX,	V_O = 2.25 V		60			60		mA
I_{CC}	V_{CC} = MAX			120			120	160	mA

†For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics over recommended ranges of T_A and V_{CC} (unless otherwise noted)

TYPE		TEST CONDITIONS	$t_{a(A)}$ ACCESS TIME FROM ADDRESS			$t_{a(S)}$ ACCESS TIME FROM ENABLE			t_{dis} DISABLE TIME			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
TBP38S16	Military	C_L = 30 pF See Note 2		18			10			10		ns
	Commercial			18			10			10		ns
TBP38S16	Military			20			10			10		ns
	Commercial			20			10			10		ns

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

recommended operating conditions

PARAMETER		MILITARY			COMMERCIAL			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−1.6			−1.6	mA
I_{OL}	Low-level output current			8			8	mA
T_A	Operating free-air temperature range	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		MILITARY			COMMERCIAL			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = MIN,	I_{OH} = −1.6 mA	2.4	3.1		2.4	3.1		V
V_{OL}	V_{CC} = MIN,	I_{OL} = 8 mA			0.5			0.5	V
I_{OZH}	V_{CC} = MAX,	V_O = 2.4 V			50			50	μA
I_{OZL}	V_{CC} = MAX,	V_O = 0.5 V			−50			−50	μA
I_I	V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.7 V			25			25	μA
I_{IL}	V_{CC} = MAX,	V_I = 0.5 V			−0.25			−0.25	mA
I_O§	V_{CC} = MAX,	V_O = 2.25 V		60			60		mA
I_{CC}	V_{CC} = MAX			65			65	100	mA

†For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics over recommended ranges of T_A and V_{CC} (unless otherwise noted)

TYPE		TEST CONDITIONS	$t_{a(A)}$ ACCESS TIME FROM ADDRESS			$t_{a(S)}$ ACCESS TIME FROM ENABLE			t_{dis} DISABLE TIME			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	MIN	TYP†	MAX	
TBP38L16-XX	Military	C_L = 30 pF See Note 2		26			12			8		ns
TBP38L16-45	Commercial			26	45		12	25		8	20	ns
TBP38L16-XX	Military			26			12			8		ns
TBP38L16-35	Commercial			26	35		12	20		8	15	ns

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

recommended operating conditions

PARAMETER		MILITARY			COMMERCIAL			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			16			16	mA
T_A	Operating free-air temperature range	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		MILITARY			COMMERCIAL			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN,	I_I = −18 mA			−1.2			−1.2	V
I_{OH}	V_{CC} = MIN,	V_{OH} = 2.4 V			0.05			0.05	mA
		V_{OH} = 5.5 V			0.1			0.1	
V_{OL}	V_{CC} = MIN,	I_{OL} = 16 mA			0.5			0.5	V
I_I	V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.7 V			25			25	μA
I_{IL}	V_{CC} = MAX,	V_I = 0.5 V			−0.25			−0.25	mA
I_{CC}	V_{CC} = MAX			120			120	160	mA

†For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions.

switching characteristics over recommended ranges of T_A and V_{CC} (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MILITARY			COMMERCIAL			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
$t_{a(A)}$	Access time from address	C_L = 30 pF See Note 2		25			25		ns
$t_{a(S)}$	Access time from chip select (enable time)			12			12		ns
t_{PLH}	Propagation delay time, low-to-high-level output from chip select			10			10		ns

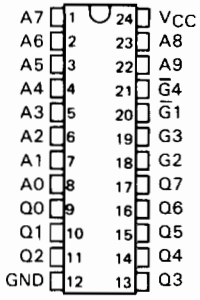
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

TBP38S8, TBP38L8, TBP38SA8
8,192-BIT (1024 WORDS BY 8 BITS) PROGRAMMABLE READ-ONLY MEMORIES

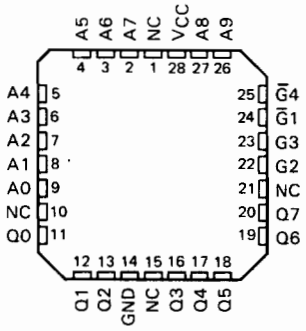
JANUARY 1985

- Fastest Schottky PROM Family
- High-Speed Access Times
- Low-Power, 3-State, and Open-Collector Options Available
- Titanium-Tungsten (Ti-W) Fuse Links for Reliable Low-Voltage Programming
- Applications Include:
  Microprogramming/Firmware Loaders
  Code Converters/Character Generators
  Translators/Emulators
  Address Mapping/Look-Up Tables
- Package Options Include 300-Mil or 600-Mil 24-Pin DIP, and 28-Pin Chip-Carrier Packages

TBP38L85, TBP38S85, TBP38SA85 . . . NT OR JT PACKAGE
TBP38L86, TBP38S86, TBP38SA86 . . . NW OR JW PACKAGE
(TOP VIEW)



TBP38L8X, TBP38S8X, TBP38SA8X . . . FN OR FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

These Series-3 monolithic TTL programmable read-only memories (PROMs) feature high-speed access times and dependable titanium-tungsten fuse link program elements. They are organized as 1024 words by 8 bits each, providing a total of 8,192 bits. The '38S8 has three-state outputs. The '38SA8 is the open-collector version and allows the device to be connected directly to data buses utilizing passive pull-up resistors. The low-power '38L8 is available for applications that require power conservation while maintaining bipolar speeds. It also has three-state outputs.

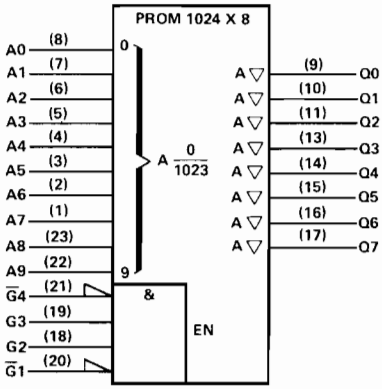
Data is programmed at any bit location with the standard Series 3 programming algorithm. The program elements store a logic level low before any programming, and are permanently set to a logic level high after programming. After execution of the programming procedure, the output for that bit location cannot be reversed. The Series 3 programming procedure should be referred to for further details. Additional circuitry has been designed into these devices to improve testability and insure high programmability.

4 PROMs

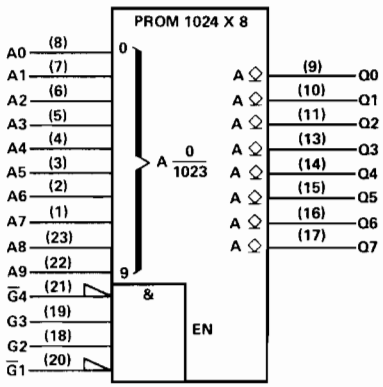
TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

logic symbols

TBP38S8, TBP38L8

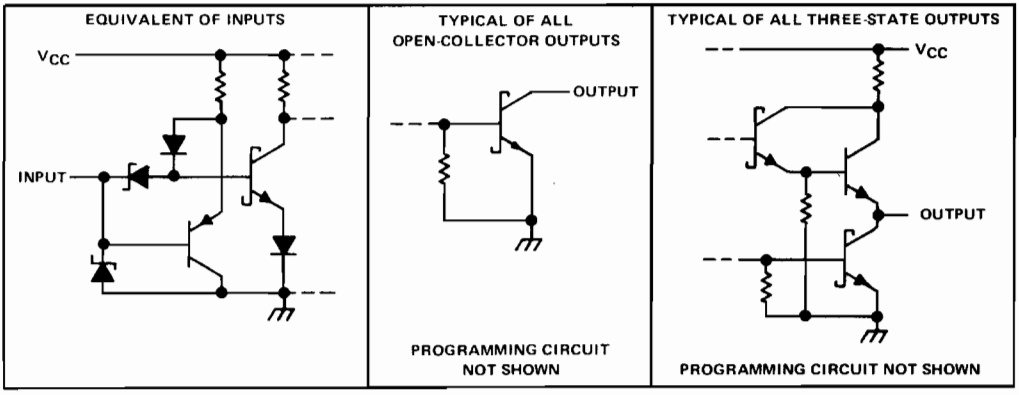


TBP38SA8



Pin numbers shown are for JT, JW, NT, or NW packages.

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Off-state output voltage . . . . . 5.5 V
Operating free-air temperature range: Military-temperature-range circuits . . . . . −55°C to 125°C
Commercial-temperature-range circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal. The supply voltage rating does not apply during programming.

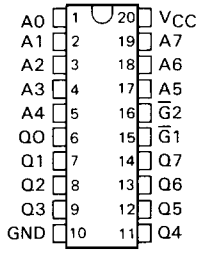
TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

2,048-BIT (256 WORDS BY 8 BITS) PROGRAMMABLE READ-ONLY MEMORIES

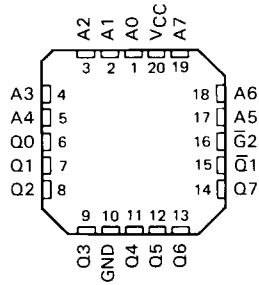
DECEMBER 1984

- Fastest Schottky PROM Family
- High-Speed Access Times
- Low-Power, Open-Collector, and 3-State Options Available
- Titanium-Tungsten (Ti-W) Fuse Links for Reliable Low-Voltage Programming
- P-N-P Inputs for Reduced Loading on System Buffers/Drivers
- Applications Include:
  Microprogramming/Firmware Loaders
  Code Converters/Character Generators
  Translators/Emulators
  Address Mapping/Look-Up Tables
- Package Options Include 20-Pin DIP, and 20-Pin Chip-Carrier

TBP38S22, TBP38L22, TBP38SA22 . . . J OR N PACKAGE
(TOP VIEW)



TBP38S2X, TBP38L2X, TBP38SA2X . . . FN OR FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These Series-3 monolithic TTL programmable read-only memories (PROMs) feature high-speed access times and dependable titanium-tungsten fuse link program elements. They are organized as 256 words by 8 bits each, providing a total of 2,048 bits. The '38S22 has three-state outputs. The '38SA22 is the open-collector version and allows the device to be connected directly to data buses utilizing passive pull-up resistors. The low-power '38L22 is available for applications that require power conservation while maintaining bipolar speeds.

Data is programmed at any bit location with the standard Series 3 programming algorithm. The program elements store a logic level low before any programming, and are permanently set to a logic level high after programming. After execution of the programming procedure, the output for that bit location cannot be reversed. The Series 3 programming procedure should be referred to for further details. Additional circuitry has been designed into these devices to improve testability and insure high programmability.

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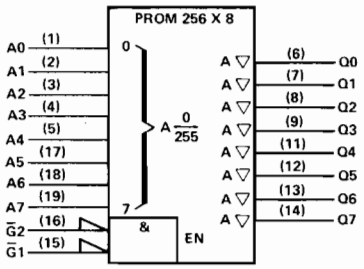
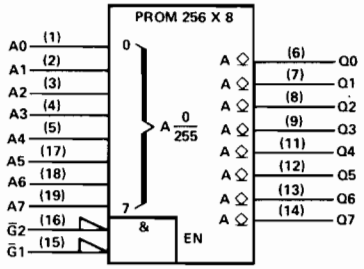
logic symbols

TBP38S22, TBP38L22

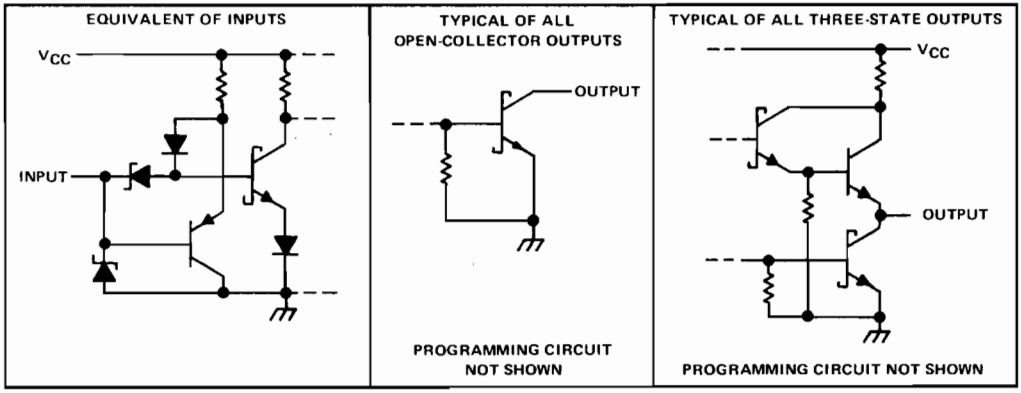


TBP38SA22



Pin numbers shown are for J or N packages.

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Off-state output voltage . . . . . 5.5 V
Operating free-air temperature range: Military-temperature-range circuits . . . . . −55°C to 125°C
Commercial-temperature-range circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal. The supply voltage rating does not apply during programming.

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

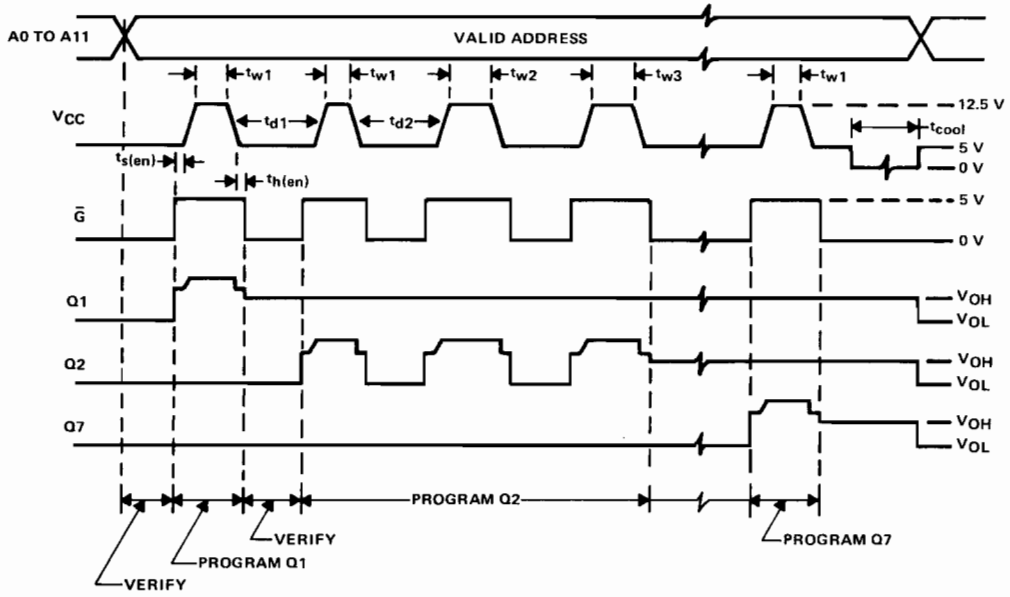
recommended operating conditions for programming (see Figure 1)

			MIN	NOM	MAX	UNIT
Supply voltage during verification		V_{CC}	4.5	5	5.5	V
Input voltage		V_{IH}	3	4	5	V
		V_{IL}	0	0.2	0.5	
Enable voltage during verification		$\overline{G}1$, $\overline{G}2$	0	0.2	0.4	V
Enable inactive voltage during programming		$\overline{G}1$, $\overline{G}2$	4.5	5	5.5	V
V_{CC} program pulse amplitude		$V_{CC(pr)}$	12	12.5	13	V
V_{CC} program pulse duration	1st attempt	t_{w1}	10	11	12	μs
	2nd attempt	t_{w2}	20	22	25	
	3rd attempt	t_{w3}	20	22	25	
Enable set-up time† before $V_{CC(pr)}$		$t_{s(en)}$	0.1	0.5	1	μs
Enable hold time‡ after $V_{CC(pr)}$		$t_{h(en)}$	0.1	0.5	1	μs
Rise time of $V_{CC(pr)}$§		$t_r(V_{CC})$	0.3	0.4	0.5	μs
Fall time of $V_{CC(pr)}$¶		$t_f(V_{CC})$	0.05	0.1	0.2	μs
Delay time between successive $V_{CC(pr)}$ pulses		t_{d1}	10	20	30	μs
Hold time between successive $V_{CC(pr)}$ pulses		t_{d2}	10	20	30	μs
Cooling time between words		t_{cool}	100	150	200	μs
Free-air temperature		T_A	20	25	30	°C

†Measured from 1.5 V on enable pin to 5.5 V on $V_{CC(pr)}$
‡Measured from 5.5 V on $V_{CC(pr)}$ to 1.5 V on enable pin
§Measured from 5 V to 12 V
¶Measured from 12 V to 5 V

step-by-step programming instructions (see Figure 1)

1. Address the word to be programmed, apply 5 volts to V_{CC} and a low-logic-level voltage to the enable inputs $\overline{G}1$ and $\overline{G}2$.
2. Verify the selected bit location that requires programming. Note: The only bit positions that require programming are outputs needing a high logic level.
3. For bit locations that do not require programming, go to step 2 for the next bit, or to step 1 for next word.
4. Deselect PROM by applying 5 volts to $\overline{G}1$ or $\overline{G}2$.
5. Connect a 4-mA current source (clamped to V_{CC}) to the output that is to be programmed.
6. Increase V_{CC} to $V_{CC(pr)}$ for a pulse duration equal to t_{wX} (where X is determined by the number of programming attempts, i.e., 1,2,3). Minimum current capability for the V_{CC} power supply should be 400 mA.
7. Verify that the output has been programmed to a high logic level. If the output has been programmed correctly, go to the next bit. If not, repeat step 2 through step 7 and increment X (where X is equal to 1 on the first programming attempt). If the output has not been programmed by the third attempt, stop programming and go to a new device.
8. Verify programming of every word after all words have been programmed using V_{CC} values of 4.5 volts and 5.5 volts.



Illustrated above is the following sequence:

1) It is desired to program the selected address with 01100001 (Q0-Q7). Only outputs Q1, Q2 and Q7 need programming.
2) Q1 is verified to be at a low logic level and then the programming sequence is executed. The output is then verified to be at a high logic level.
3) Q2 is an example of an output requiring three attempts to be programmed successfully.
4) Q7 is programmed to a high logic level.

FIGURE 1. SERIES 3 PROGRAMMING SEQUENCE

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recommended operating conditions

PARAMETER		MILITARY			COMMERCIAL			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{iL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−2			−3.2	mA
I_{OL}	Low-level output current			16			16	mA
T_A	Operating free-air temperature range	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		MILITARY			COMMERCIAL			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = MIN,	I_{OH} = MAX	2.4	3.1		2.4	3.1		V
V_{OL}	V_{CC} = MIN,	I_{OL} = 16 mA			0.5			0.5	V
I_{OZH}	V_{CC} = MAX,	V_O = 2.4 V			50			50	μA
I_{OZL}	V_{CC} = MAX,	V_O = 0.5 V			−50			−50	μA
I_I	V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.7 V			25			25	μA
I_{IL}	V_{CC} = MAX,	V_I = 0.5 V			−0.25			−0.25	mA
I_O§	V_{CC} = MAX,	V_O = 2.25 V		60			60		mA
I_{CC}	V_{CC} = MAX								mA

†For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics over recommended ranges of T_A and V_{CC} (unless otherwise noted)

TYPE		TEST CONDITIONS	$t_{a(A)}$ ACCESS TIME FROM ADDRESS			$t_{a(S)}$ ACCESS TIME FROM ENABLE			t_{dis} DISABLE TIME			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
TBP38S22-XX	Military	C_L = 30 pF See Note 2										ns
TBP38S22-XX	Commercial			14			8			7		ns
TBP38S22	Military											ns
	Commercial			14			8			7		ns

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: Load circuits and voltage waveforms are shown in Section 1 of *The TTL Data Book*, Volume 4, 1985.

recommended operating conditions

PARAMETER		MILITARY			COMMERCIAL			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			−1.6			−1.6	mA
I_{OL}	Low-level output current			8			8	mA
T_A	Operating free-air temperature range	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		MILITARY			COMMERCIAL			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = MIN,	I_{OH} = −1.6 mA	2.4	3.1		2.4	3.1		V
V_{OL}	V_{CC} = MIN,	I_{OL} = 8 mA			0.5			0.5	V
I_{OZH}	V_{CC} = MAX,	V_O = 2.4 V			50			50	μA
I_{OZL}	V_{CC} = MAX,	V_O = 0.5 V			−50			−50	μA
I_I	V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.7 V			25			25	μA
I_{IL}	V_{CC} = MAX,	V_I = 0.5 V			−0.25			−0.25	mA
I_O§	V_{CC} = MAX,	V_O = 2.25 V		60			60		mA
I_{CC}	V_{CC} = MAX								mA

†For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions.
§The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics over recommended ranges of T_A and V_{CC} (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MILITARY			COMMERCIAL			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
$t_{a(A)}$	Access time from address	C_L = 30 pF See Note 2							ns
$t_{a(S)}$	Access time from chip select (enable time)								ns
t_{dis}	Disable time								ns

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: Load circuits and voltage waveforms are shown in Section 1 of *The TTL Data Book*, Volume 4, 1985.

TEXAS INSTRUMENTS
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recommended operating conditions

PARAMETER		MILITARY			COMMERCIAL			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OL}	Low-level output current			16			16	mA
T_A	Operating free-air temperature range	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		MILITARY			COMMERCIAL			†UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = MIN,	I_I = −18 mA			−1.2			−1.2	V
I_{OH}	V_{CC} = MIN,	V_{OH} = 2.4 V			0.05			0.05	mA
		V_{OH} = 5.5 V			0.1			0.1	
V_{OL}	V_{CC} = MIN,	I_{OL} = 16 mA			0.5			0.5	V
I_I	V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	V_{CC} = MAX,	V_I = 2.7 V			25			25	μA
I_{IL}	V_{CC} = MAX,	V_I = 0.5 V			−0.25			−0.25	mA
I_{CC}	V_{CC} = MAX								mA

†For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions.

switching characteristics over recommended ranges of T_A and V_{CC} (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MILITARY			COMMERCIAL			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
$t_{a(A)}$	Access time from address	C_L = 30 pF See Note 2							ns
$t_{a(S)}$	Access time from chip select (enable time)								ns
t_{PLH}	Propagation delay time, low-to-high-level output from chip select								ns

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: Load circuits and voltage waveforms are shown in Section 1 of *The TTL Data Book*, Volume 4, 1985.

General Information 1

Functional Index 2

Field-Programmable Logic 3

PROMs 4

RAMs and Memory-Based Code Converters 5

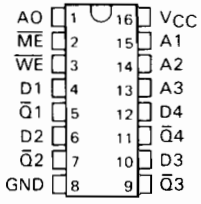
Designing with Texas Instruments Field-Programmable Logic 6

Mechanical Data 7

D1416, DECEMBER 1972—REVISED FEBRUARY 1984

- **For Application as a "Scratch Pad" Memory with Nondestructive Read-Out**
- **Fully Decoded Memory Organized as 16 Words of Four Bits Each**
- **Fast Access Time . . . 33 ns Typical**
- **Diode-Clamped, Buffered Inputs**
- **Open-Collector Outputs Provide Wire-AND Capability**
- **Typical Power Dissipation . . . 375 mW**
- **Compatible with Most TTL Circuits**

SN7489 . . . J OR N PACKAGE
(TOP VIEW)

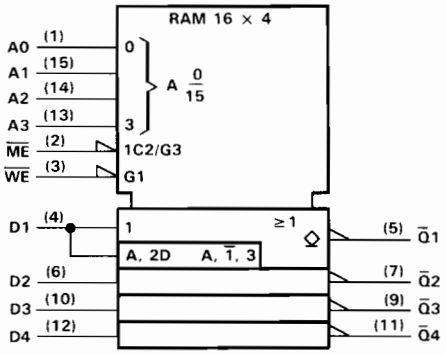


description

This 64-bit active-element memory is a monolithic, high-speed, transistor-transistor logic (TTL) array of 64 flip-flop memory cells organized in a matrix to provide 16 words of four bits each. Each of the 16 words is addressed in straight binary with full on-chip decoding.

The buffered memory inputs consist of four address lines, four data inputs, a write enable, and a memory enable for controlling the entry and access of data. The memory has open-collector outputs which may be wired-AND connected to permit expansion up to 4704 words of N-bit length without additional output buffering. Access time is typically 33 nanoseconds; power dissipation is typically 375 milliwatts.

logic symbol



FUNCTION TABLE

$\overline{ME}$	$\overline{WE}$	OPERATION	CONDITION OF OUTPUTS
L	L	Write	Complement of Data Inputs
L	H	Read	Complement of Selected Word
H	L	Inhibit Storage	Complement of Data Inputs
H	H	Do Nothing	High

write operation

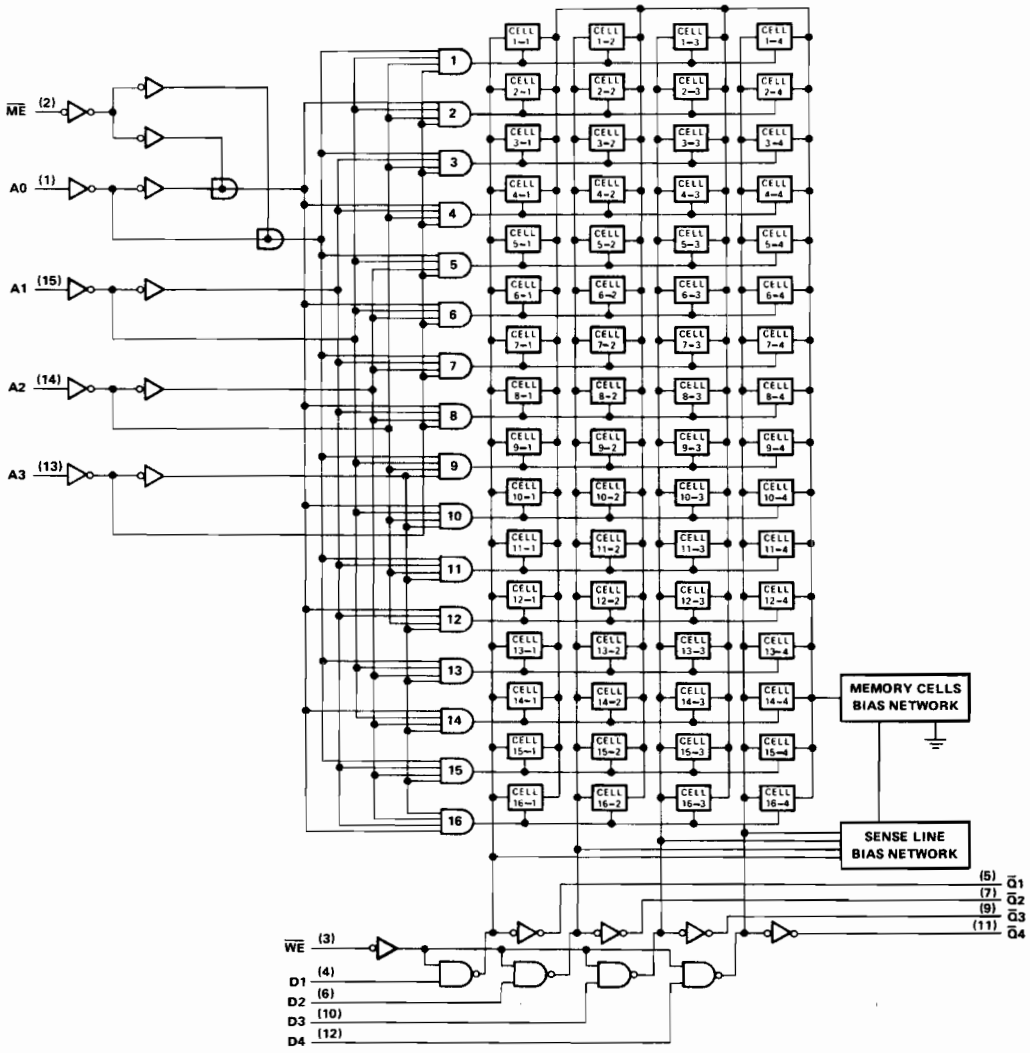
Information present at the data inputs is written into the memory by addressing the desired word and holding both the memory enable and write enable low. Since the internal output of the data input gate is common to the input of the sense amplifier, the sense output will assume the opposite state of the information at the data inputs when the write enable is low.

read operation

The complement of the information which has been written into the memory is nondestructively read out at the four sense outputs. This is accomplished by holding the memory enable low, the write enable high, and selecting the desired address.

5 RAMs

logic diagram



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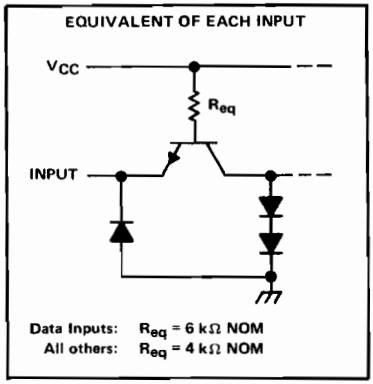
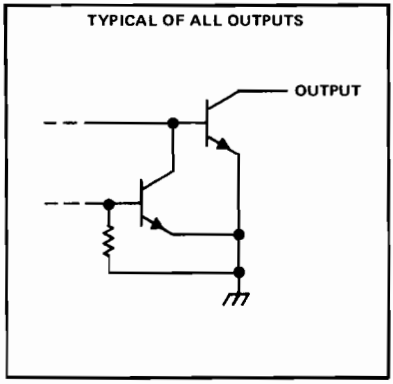
schematics of inputs and outputs





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
High-level output voltage, V_{OH} (see Notes 1 and 2) . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. This is the maximum voltage that should be applied to any output when it is in the off state.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Width of write-enable pulse, t_w	40			ns
Setup time, data input with respect to write enable, t_{su} (see Figure 1)	40			ns
Hold time, data input with respect to write enable, t_h (see Figure 1)	5			ns
Select input setup time with respect to write enable, t_{su}	0			ns
Select input hold time after writing, t_h (see Figure 1)	5			ns
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,		I_I = −12 mA			−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IL} = 0.8 V,		V_{IH} = 2 V, V_{OH} = 5.5 V			20	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V	V_{IH} = 2 V,	I_{OL} = 12 mA			0.4	V
				I_{OL} = 16 mA			0.45	
I_I	Input current at maximum input voltage	V_{CC} = MAX,		V_I = 5.5 V			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,		V_I = 2.4 V			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX,		V_I = 0.4 V			−1.6	mA
I_{CC}	Supply current	V_{CC} = MAX,		See Note 3		75	105	mA
C_o	Off-state output capacitance	V_{CC} = 5 V, f = 1 MHz		V_O = 2.4 V,		6.5		pF

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 3: I_{CC} is measured with the memory enable grounded, all other inputs at 4.5 V, and all outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from memory enable		C_L = 30 pF, R_{L1} = 300 Ω, R_{L2} = 600 Ω, See Figure 1		26	50	ns
t_{PHL}	Propagation delay time, high-to-low-level output from memory enable				33	50	
t_{PLH}	Propagation delay time, low-to-high-level output from any address input				30	60	ns
t_{PHL}	Propagation delay time, high-to-low-level output from any address input				35	60	
t_{SR}	Sense recovery time after writing	Output initially high			39	70	ns
		Output initially low			48	70	

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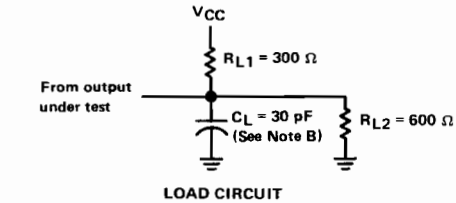
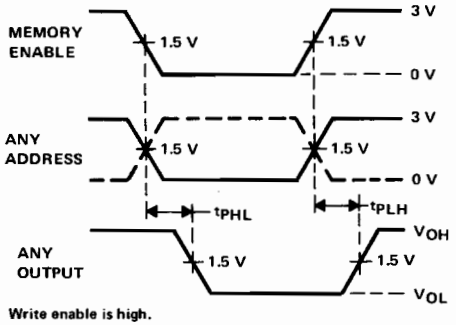
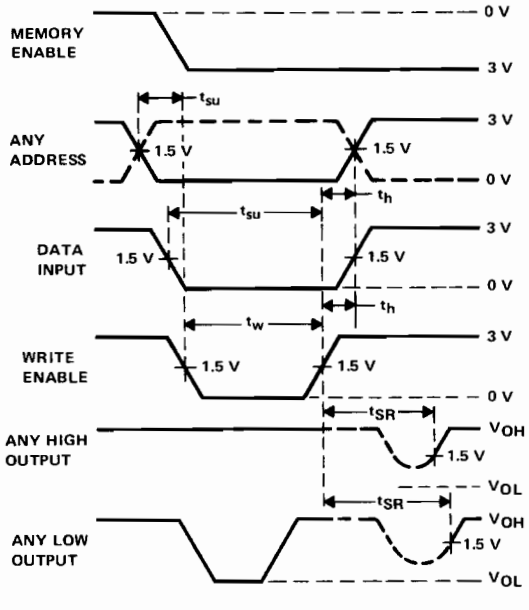
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



READ CYCLE



WRITE CYCLE FROM WRITE ENABLE

NOTES: A. The input pulse generators have the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.

FIGURE 1–SWITCHING CHARACTERISTICS

5 RAMs

TYPICAL CHARACTERISTICS

INPUT CURRENT
vs
INPUT VOLTAGE

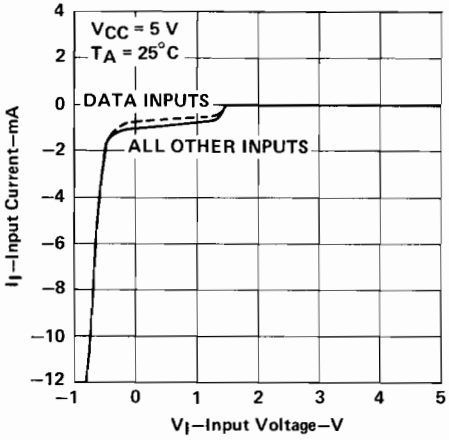


FIGURE 2

PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

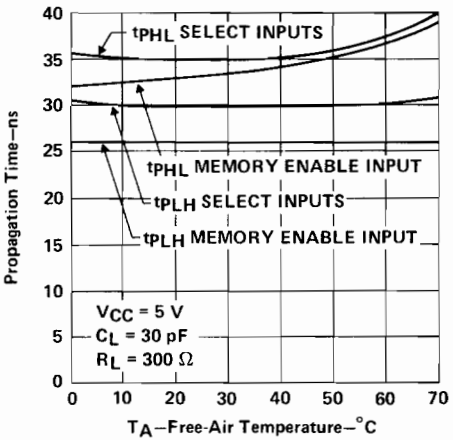


FIGURE 3

5 RAMs

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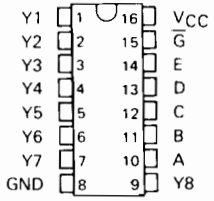
FEBRUARY 1971 REVISED DECEMBER 1972

SN54184, SN74184 BCD-TO-BINARY CONVERTERS
SN54185A, SN74185A BINARY-TO-BCD CONVERTERS

SN54184, SN54185A . . . J OR W PACKAGE
SN74184, SN74185A . . . J OR N PACKAGE
(TOP VIEW)



description

These monolithic converters are derived from the custom MSI 256-bit read-only memories SN5488 and SN7488. Emitter connections are made to provide direct read-out of converted codes at outputs Y8 through Y1 as shown in the function tables. These converters demonstrate the versatility of a read-only memory in that an unlimited number of reference tables or conversion tables may be built into a system using economical, customized read-only memories. Both of these converters comprehend that the least significant bits (LSB) of the binary and BCD codes are logically equal, and in each case the LSB bypasses the converter as illustrated in the typical applications. This means that a 6-bit converter is produced in each case. Both devices are cascadable to N bits.

TABLE I
SN54184, SN74184
PACKAGE COUNT AND DELAY TIMES
FOR BCD-TO-BINARY CONVERSION

INPUT (DECADES)	PACKAGES REQUIRED	TOTAL DELAY TIMES (ns)	
		TYP	MAX
2	2	56	80
3	6	140	200
4	11	196	280
5	19	280	400
6	28	364	520

An overriding enable input is provided on each converter which, when taken high, inhibits the function, causing all outputs to go high. For this reason, and to minimize power consumption, unused outputs Y7 and Y8 of the '185A and all "don't care" conditions of the '184 are programmed high. The outputs are of the open-collector type.

The SN54184 and SN54185A are characterized for operation over the full military temperature range of −55°C to 125°C; the SN74184 and SN74185A are characterized for operation from 0°C to 70°C.

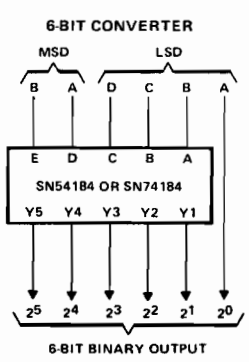
SN54184 and SN74184 BCD-to-binary converters

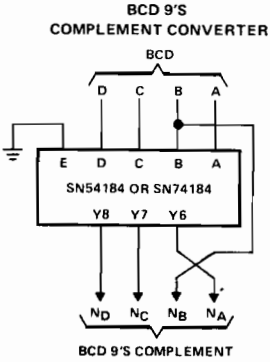
The 6-bit BCD-to-binary function of the SN54184 and SN74184 is analogous to the algorithm:

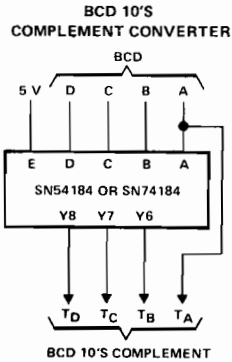
a. Shift BCD number right one bit and examine each decade. Subtract three from each 4-bit decade containing a binary value greater than seven.
b. Shift right, examine, and correct after each shift until the least significant decade contains a number smaller than eight and all other converted decades contain zeros.

In addition to BCD-to-binary conversion, the SN54184 and SN74184 are programmed to generate BCD 9's complement or BCD 10's complement. Again, in each case, one bit of the complement code is logically equal to one of the BCD bits; therefore, these complements can be produced on three lines. As outputs Y6, Y7, and Y8 are not required in the BCD-to-binary conversion, they are utilized to provide these complement codes as specified in the function table (following page, right) when the devices are connected as shown above the function table.

SN54184 and SN74184 BCD-to-binary converters (continued)







FUNCTION TABLE
BCD-TO-BINARY
CONVERTER

BCD WORDS	INPUTS (See Note A)						OUTPUTS (See Note B)				
	E	D	C	B	A	$\overline{G}$	Y5	Y4	Y3	Y2	Y1
0-1	L	L	L	L	L	L	L	L	L	L	L
2-3	L	L	L	L	H	L	L	L	L	L	H
4-5	L	L	L	H	L	L	L	L	L	H	L
6-7	L	L	L	H	H	L	L	L	L	H	H
8-9	L	L	H	L	L	L	L	L	H	L	L
10-11	L	H	L	L	L	L	L	L	H	L	H
12-13	L	H	L	L	H	L	L	L	H	H	L
14-15	L	H	L	H	L	L	L	L	H	H	H
16-17	L	H	L	H	H	L	L	H	L	L	L
18-19	L	H	H	L	L	L	L	H	L	L	H
20-21	H	L	L	L	L	L	L	H	L	H	L
22-23	H	L	L	L	H	L	L	H	L	H	H
24-25	H	L	L	H	L	L	L	H	H	L	L
26-27	H	L	L	H	H	L	L	H	H	L	H
28-29	H	L	H	L	L	L	L	H	H	H	L
30-31	H	H	L	L	L	L	L	H	H	H	H
32-33	H	H	L	L	H	L	H	L	L	L	L
34-35	H	H	L	H	L	L	H	L	L	L	H
36-37	H	H	L	H	H	L	H	L	L	H	L
38-39	H	H	H	L	L	L	H	L	L	H	H
ANY	X	X	X	X	X	H	H	H	H	H	H

H = high level, L = low level, X = irrelevant

NOTES: A. Input conditions other than those shown produce highs at outputs Y1 through Y5.

B. Outputs Y6, Y7, and Y8 are not used for BCD-to-binary conversion.

FUNCTION TABLE
BCD 9'S OR BCD 10'S
COMPLEMENT CONVERTER

BCD WORD	INPUTS (See Note C)						OUTPUTS (See Note D)		
	E†	D	C	B	A	$\overline{G}$	Y8	Y7	Y6
0	L	L	L	L	L	L	H	L	H
1	L	L	L	L	H	L	H	L	L
2	L	L	L	H	L	L	L	H	H
3	L	L	L	H	H	L	L	H	L
4	L	L	H	L	L	L	L	H	H
5	L	L	H	L	H	L	L	H	L
6	L	L	H	H	L	L	L	L	H
7	L	L	H	H	H	L	L	L	L
8	L	H	L	L	L	L	L	L	H
9	L	H	L	L	H	L	L	L	L
0	H	L	L	L	L	L	L	L	L
1	H	L	L	L	H	L	H	L	L
2	H	L	L	H	L	L	H	L	L
3	H	L	L	H	H	L	L	H	H
4	H	L	H	L	L	L	L	H	H
5	H	L	H	L	H	L	L	H	L
6	H	L	H	H	L	L	L	H	L
7	H	L	H	H	H	L	L	L	H
8	H	H	L	L	L	L	L	L	H
9	H	H	L	L	H	L	L	L	L
ANY	X	X	X	X	X	H	H	H	H

H = high level, L = low level, X = irrelevant

NOTES: C. Input conditions other than those shown produce highs at outputs Y6, Y7, and Y8.

D. Outputs Y1 through Y5 are not used for BCD 9's or BCD 10's complement conversion.

†When these devices are used as complement converters, input E is used as a mode control. With this input low, the BCD 9's complement is generated; when it is high, the BCD 10's complement is generated.

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SN54185A and SN74185A binary-to-BCD converters

The function performed by these 6-bit binary-to-BCD converters is analogous to the algorithm:

a. Examine the three most significant bits. If the sum is greater than four, add three and shift left one bit.
b. Examine each BCD decade. If the sum is greater than four, add three and shift left one bit.
c. Repeat step b until the least-significant binary bit is in the least-significant BCD location.

6-BIT CONVERTER

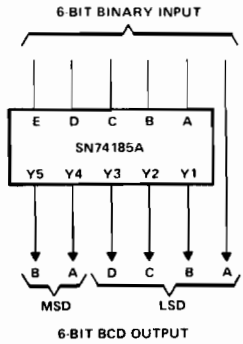

TABLE II

SN54185A, SN74185A

PACKAGE COUNT AND DELAY TIMES FOR BINARY-TO-BCD CONVERSION

INPUT (BITS)	PACKAGES REQUIRED	TOTAL DELAY TIME (ns)	
		TYP	MAX
4 to 6	1	25	40
7 or 8	3	50	80
9	4	75	120
10	6	100	160
11	7	125	200
12	8	125	200
13	10	150	240
14	12	175	280
15	14	175	280
16	16	200	320
17	19	225	360
18	21	225	360
19	24	250	400
20	27	275	440

FUNCTION TABLE

BINARY WORDS	INPUTS						OUTPUTS							
	BINARY SELECT					ENABLE								
	E	D	C	B	A	$\overline{G}$	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1
0 1	L	L	L	L	L	L	H	H	L	L	L	L	L	L
2 3	L	L	L	L	H	L	H	H	L	L	L	L	L	H
4 5	L	L	L	H	L	L	H	H	L	L	L	L	H	L
6 7	L	L	L	H	H	L	H	H	L	L	L	L	H	H
8 9	L	L	H	L	L	L	H	H	L	L	L	H	L	L
10 11	L	L	H	L	H	L	H	H	L	L	H	L	L	L
12 13	L	L	H	H	L	L	H	H	L	L	H	L	L	H
14 15	L	L	H	H	H	L	H	H	L	L	H	L	H	L
16 17	L	H	L	L	L	L	H	H	L	L	H	L	H	H
18 19	L	H	L	L	H	L	H	H	L	L	H	H	L	L
20 21	L	H	L	H	L	L	H	H	L	H	L	L	L	L
22 23	L	H	L	H	H	L	H	H	L	H	L	L	L	H
24 25	L	H	H	L	L	L	H	H	L	H	L	L	H	L
26 27	L	H	H	L	H	L	H	H	L	H	L	L	H	H
28 29	L	H	H	H	L	L	H	H	L	H	L	H	L	L
30 31	L	H	H	H	H	L	H	H	L	H	H	L	L	L
32 33	H	L	L	L	L	L	H	H	L	H	H	L	L	H
34 35	H	L	L	L	H	L	H	H	L	H	H	L	H	L
36 37	H	L	L	H	L	L	H	H	L	H	H	L	H	H
38 39	H	L	L	H	H	L	H	H	L	H	H	H	L	L
40 41	H	L	H	L	L	L	H	H	H	L	L	L	L	L
42 43	H	L	H	L	H	L	H	H	H	L	L	L	L	H
44 45	H	L	H	H	L	L	H	H	H	L	L	L	H	L
46 47	H	L	H	H	H	L	H	H	H	L	L	L	H	H
48 49	H	H	L	L	L	L	H	H	H	L	L	H	L	L
50 51	H	H	L	L	H	L	H	H	H	L	H	L	L	L
52 53	H	H	L	H	L	L	H	H	H	L	H	L	L	H
54 55	H	H	L	H	H	L	H	H	H	L	H	L	H	L
56 57	H	H	H	L	L	L	H	H	H	L	H	L	H	H
58 59	H	H	H	L	H	L	H	H	H	L	H	H	L	L
60 61	H	H	H	H	L	L	H	H	H	H	L	L	L	L
62 63	H	H	H	H	H	L	H	H	H	H	L	L	L	H
ALL	X	X	X	X	X	H	H	H	H	H	H	H	H	H

H = high level, L = low level, X = irrelevant

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN54184, SN54185A . . . . . −55°C to 125°C
SN74184, SN74185A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54184, SN54185A			SN74184, SN74185A			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Low-level output current, I_{OL}			12			12	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −12 mA			−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, V_{OH} = 5.5 V			100	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = 12 mA			0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4 V			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V			−1	mA
I_{CCH}	Supply current, all outputs high	V_{CC} = MAX			50		mA
I_{CCL}	Supply current, all programmed outputs low				62	99	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from enable $\overline{G}$	C_L = 30 pF,		19	30	ns
t_{PHL}	Propagation delay time, high-to-low-level output from enable $\overline{G}$	R_{L1} = 300 Ω,		22	35	ns
t_{PLH}	Propagation delay time, low-to-high-level output from binary select	R_{L2} = 600 Ω,		27	40	ns
t_{PHL}	Propagation delay time, high-to-low-level output from binary select	See Figure 1 and Note 2		23	40	ns

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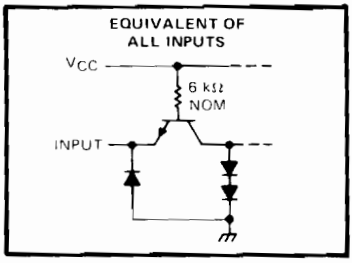
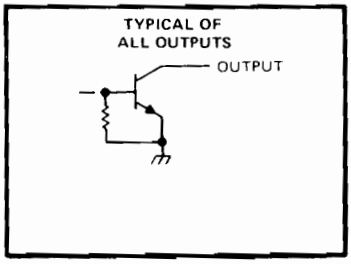
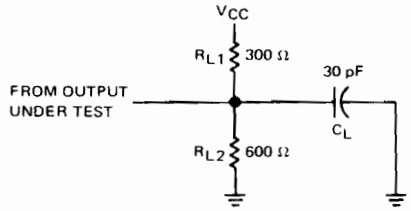
schematics of inputs and outputs





PARAMETER MEASUREMENT INFORMATION



C_L includes probe and jig capacitance.

LOAD CIRCUIT
FIGURE 1

NOTE 2: See General Information Section for load circuits and voltage waveforms.

TYPICAL APPLICATION DATA
SN54184, SN74184

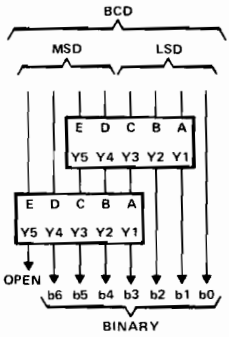


FIGURE 2–BCD-TO-BINARY CONVERTER FOR TWO BCD DECADES

MSD—most significant decade
LSD—least significant decade
Each rectangle represents an SN54184 or SN74184

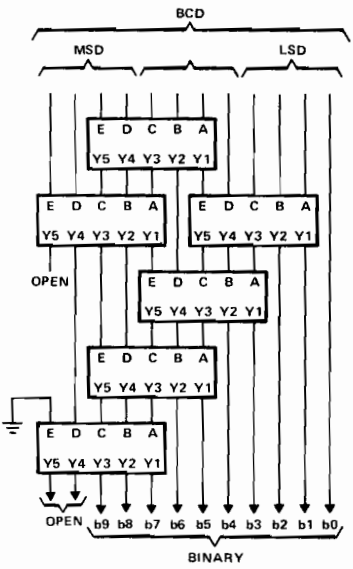
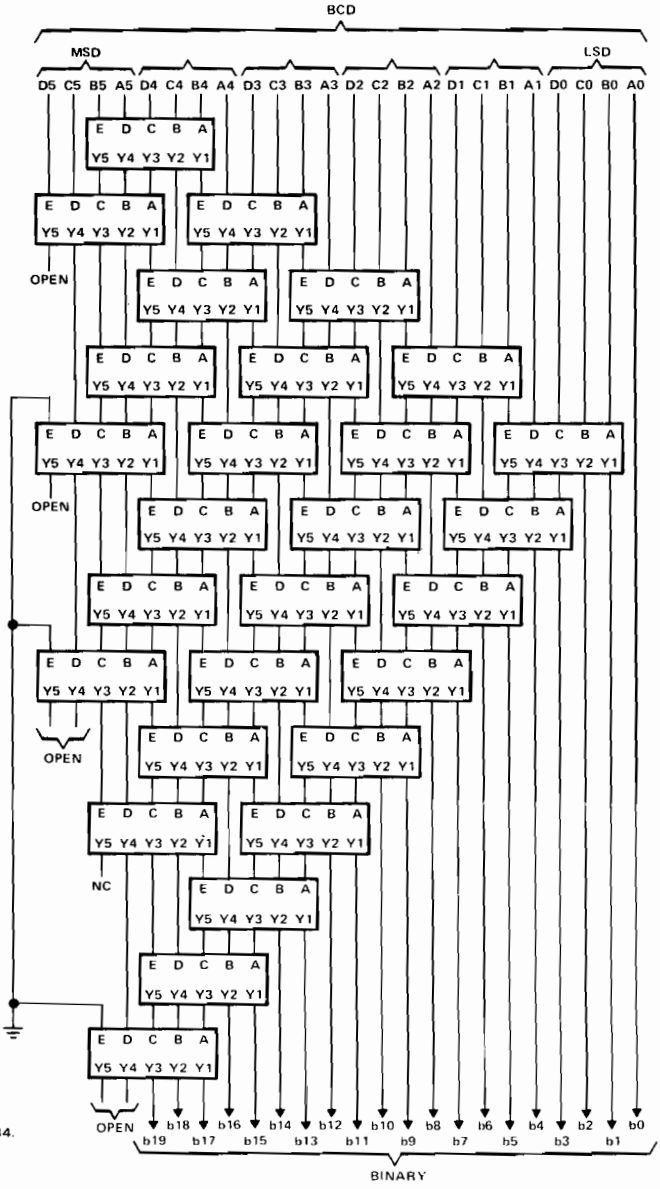


FIGURE 3–BCD-TO-BINARY CONVERTER FOR THREE BCD DECADES

5 RAMs

TYPICAL APPLICATION DATA
SN54184, SN74184



MSD–most significant decade
LSD–least significant decade
Each rectangle represents and SN54184 or SN74184.

FIGURE 4–BCD-TO-BINARY CONVERTER FOR SIX BCD DECADES

TYPICAL APPLICATION DATA
SN54185A, SN74185A

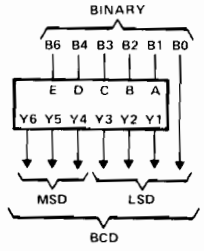


FIGURE 5–6-BIT BINARY-TO-BCD CONVERTER

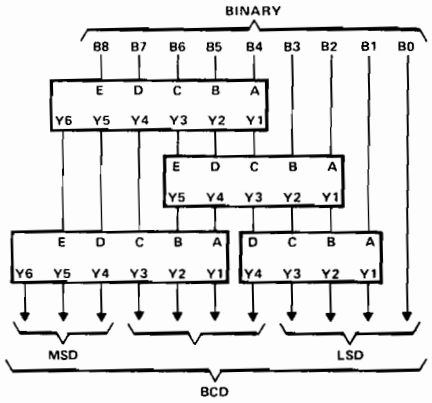


FIGURE 7–9-BIT BINARY-TO-BCD CONVERTER

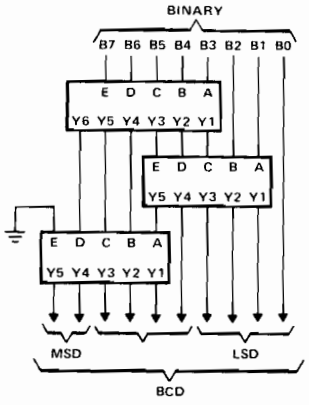


FIGURE 6–8-BIT BINARY-TO-BCD CONVERTER

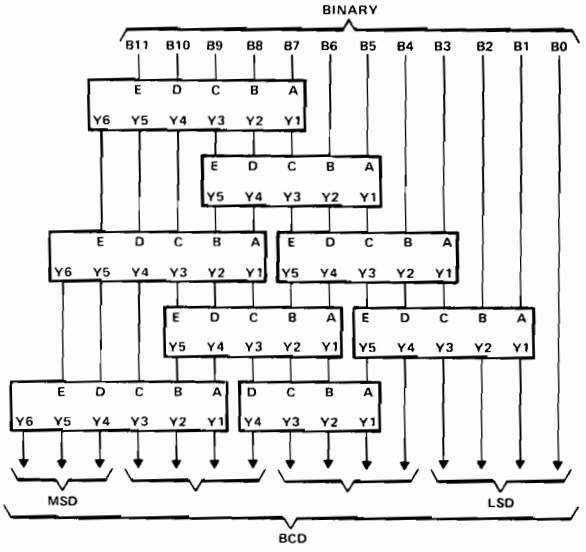


FIGURE 8–12-BIT BINARY-TO-BCD CONVERTER (SEE NOTE B)

MSD–Most significant decade
LSD–Least significant decade
NOTES: A. Each rectangle represents an SN54185A or an SN74185A.
B. All unused E inputs are grounded.

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

TYPICAL APPLICATION DATA
SN54185A, SN74185A

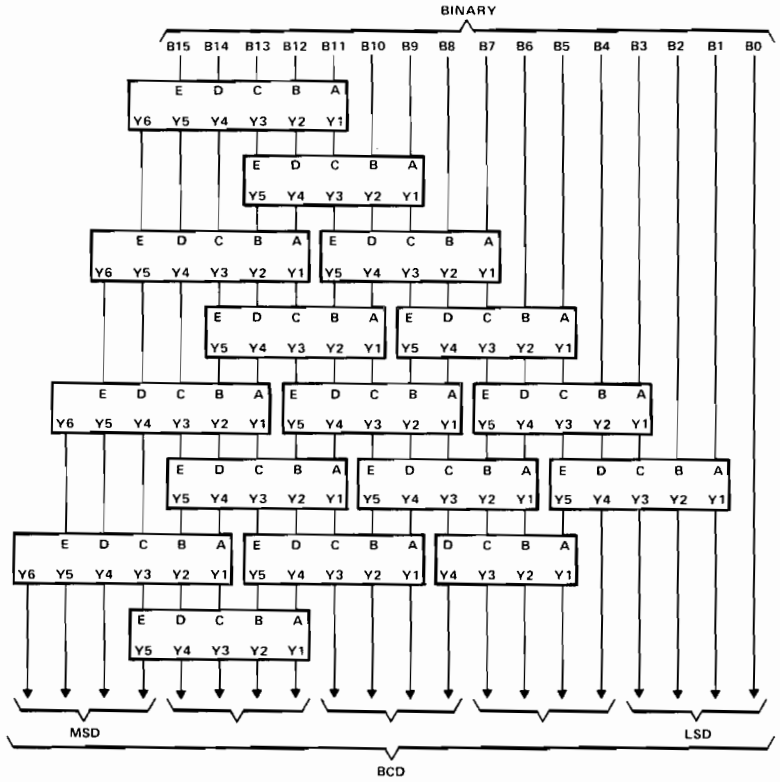
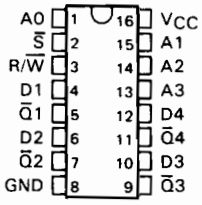


FIGURE 9–16 BIT BINARY-TO-BCD CONVERTER (SEE NOTE B)

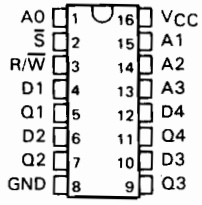
MSD—most significant decade
LSD—least significant decade
NOTES: A. Each rectangle represents an SN54185A or SN74185A.
B. All unused E inputs are grounded.

- **Organized as 16 Words of Four Bits Each**
- **Choice of Buffered 3-State or Open-Collector outputs**
- **Choice of Noninverted or Inverted Outputs**
- **Typical Access Time . . . 50 ns**

SN54LS189A, SN54LS289A . . . J PACKAGE
SN74LS189A, SN74LS289A . . . J OR N PACKAGE
(TOP VIEW)



SN54LS219A, SN54LS319A . . . J PACKAGE
SN74LS219A, SN74LS319A . . . J OR N PACKAGE
(TOP VIEW)



description

These monolithic TTL memories feature Schottky clamping for high performance and a fast chip-select access time to enhance decoding at the system level. A three-state output version and an open-collector-output version are offered for both of the logic choices. A three-state output offers the convenience of an open-collector output with the speed of a totem-pole output; it can be bus-connected to other similar outputs, yet it retains the fast rise time characteristic of the TTL totem-pole output. An open-collector output offers the capability of direct interface with a data line having a passive pull-up.

write cycle

Information to be stored in the memory is written into the selected address location when the chip-select ($\overline{S}$) and the write-enable ($R/\overline{W}$) inputs are low. While the write-enable input is low, the memory outputs are off (three-state = Hi-Z, open-collector = high). When a number of outputs are bus-connected, this off state neither loads nor drives the data bus; however, it permits the bus line to be driven by other active outputs or a passive pull-up.

read cycle

Information stored in the memory (see function table for input/output phase relationship) is available at the outputs when the write-enable input is high and the chip-select input is low. When the chip-select input is high, the outputs will be off.

FUNCTION TABLE

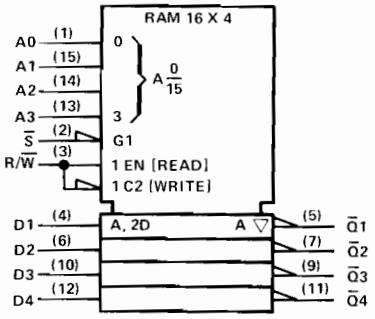
FUNCTION	INPUTS		OUTPUTS			
	CHIP SELECT	WRITE ENABLE	'LS189A	'LS289A	'LS219A	'LS319A
Write	L	L	Z	Off	Z	Off
Read	L	H	Complement of Data Entered	Complement of Data Entered	Data Entered	Data Entered
Inhibit	H	X	Z	Off	Z	Off

H = high level, L = low level, X = irrelevant, Z = high impedance

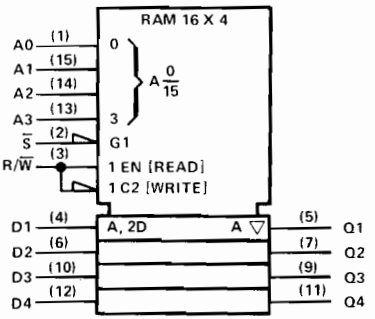
5 RAMs

logic symbols

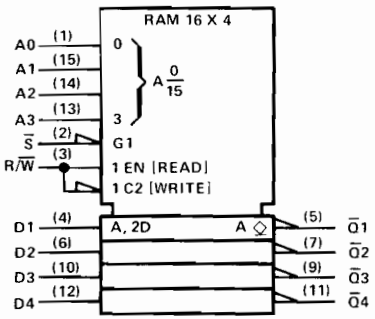
'LS189A



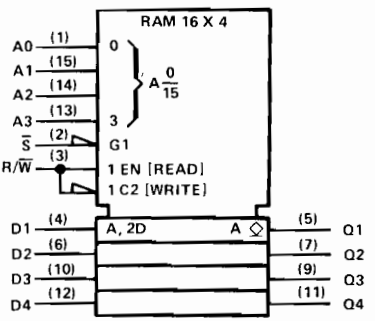
'LS219A



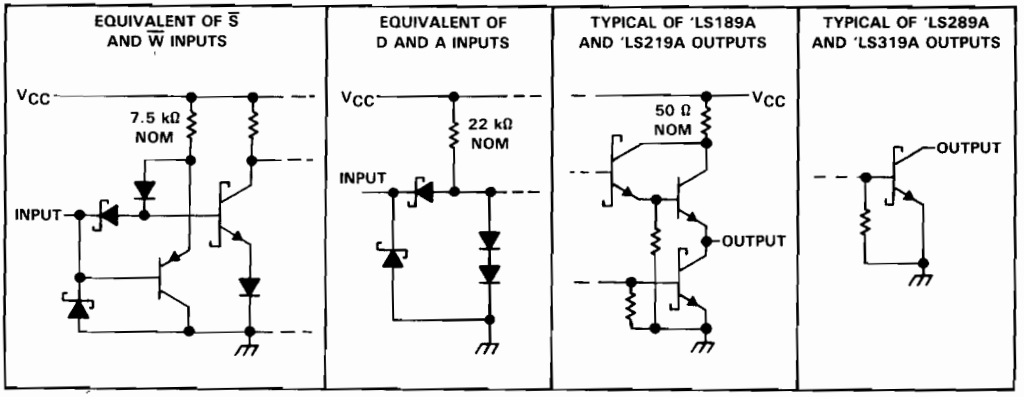
'LS289A



'LS319A



schematics of inputs and outputs



TEXAS INSTRUMENTS
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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage: 'LS189A, 'LS219A . . . . . 5.5 V
'LS289A, 'LS319A . . . . . 7 V
Operating free-air temperature range: SN54LS' Circuits . . . . . −55°C to 125°C
SN74LS' Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS189A, SN54LS219A			SN74LS189A, SN74LS219A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−1			−2.6	mA
Low-level output current, I_{OL}				12			24	mA
Width of write pulse (write enable low), $t_{w(wr)}$		100			70			ns
Setup time	Address before write pulse, $t_{su(ad)}$	0↓			0↓			ns
	Data before end of write pulse, $t_{su(da)}$	100↓			60↓			ns
	Chip-select before end of write pulse, $t_{su(S)}$	100↓			60↓			ns
Hold time	Address after write pulse, $t_{h(ad)}$	0↓			0↓			ns
	Data after write pulse, $t_{h(da)}$	0↓			0↓			ns
	Chip-select after write pulse, $t_{h(S)}$	0↓			0↓			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

↓↑The arrow indicates the transition of the write-enable input used for reference: ↑ for the low-to-high transition, ↓ for the high-to-low transition.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS189A SN54LS219A			SN74LS189A SN74LS219A			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL}max, I_{OH} = MAX		2.4	3.1		2.4	3.1		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL}max	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	Off-state output current high-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = V_{IL}max, V_O = 2.7 V				20			20	μA
I_{OZL}	Off-state output current, low-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = V_{IL}max, V_O = 0.4 V				−20			−20	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7 V				100			100	μA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−0.4			−0.4	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−30		−130	−30		−130	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2			35	60		35	60	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
NOTE 2: I_{CC} is measured with the write-enable and chip-select inputs grounded, all other inputs at 4.5 V, and all outputs open.

switching characteristics over recommended operating ranges of T_A and V_{CC} (unless otherwise noted)

PARAMETER			TEST CONDITIONS	SN54LS189A SN54LS219A			SN74LS189A SN74LS219A			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
$t_{a(ad)}$	Access time from address		C_L = 45 pF, See Note 3		50	90		50	80	ns
$t_{a(S)}$	Access time from chip select (enable time)				35	70		35	60	ns
t_{SR}	Sense recovery time				55	100		55	90	ns
t_{PXZ}	Disable time from high or low level	from $\overline{S}$	C_L = 5 pF, See Note 3		30	60		30	50	ns
		from R/$\overline{W}$			40	70		40	60	

‡All typical values are at V_{CC} = 5 V, T_A = 25°.
NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

recommended operating conditions

		SN54LS289A, SN54LS319A			SN74LS289A, SN74LS319A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}				5.5			5.5	V
Low-level output current, I_{OL}				12			24	mA
Width of write pulse (write enable low), $t_{w(wr)}$		100			70			ns
Setup time	Address before write pulse, $t_{su(ad)}$	0↓			0↓			ns
	Data before end of write pulse, $t_{su(da)}$	100↑			60↑			
	Chip-select before end of write pulse, $t_{su(S)}$	100↑			60↑			
Hold time	Address after write pulse, $t_{h(ad)}$	0↑			0↑			ns
	Data after write pulse, $t_{h(da)}$	0↑			0↑			
	Chip-select after write pulse, $t_{h(S)}$	0↑			0↑			
Operating free-air temperature, T_A		−55		125	0		70	°C

↑↓The arrow indicates the transition of the write-enable input used for reference: ↑ for the low-to-high transition, ↓ for the high-to-low transition.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS289A SN54LS319A			SN74LS289A SN74LS319A			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL}max,	V_O = 2.4 V			20			20	μA
			V_O = 5.5 V			100			100	
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL}max	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 24 mA					0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7 V				100			100	μA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−0.4			−0.4	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2			35	60		35	60	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
NOTE 2: I_{CC} is measured with the write-enable and chip-select inputs grounded, all other inputs at 4.5 V, and all outputs open.

switching characteristics over recommended operating ranges of T_A and V_{CC} (unless otherwise noted)

PARAMETER			TEST CONDITIONS	SN54LS289A SN54LS319A			SN74LS289A SN74LS319A			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
$t_{a(ad)}$	Access time from address		C_L = 45 pF, R_L = 667Ω, See Note 3		50	90		50	80	ns
$t_{a(S)}$	Access time from chip select (enable time)				35	70		35	60	ns
t_{SR}	Sense recovery time				55	100		55	90	ns
t_{PLH}	Propagation delay time, low-to-high-level output (disable time)	from $\overline{S}$			30	60		30	50	ns
		from R/$\overline{W}$			40	70		40	60	

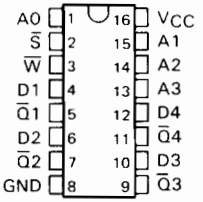
‡All typical values are at V_{CC} = 5 V, T_A = 25°.
NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

5 RAMs

STATIC RANDOM-ACCESS MEMORIES

- **Fully Decoded RAMs Organized as 16 Words of Four Bits Each**
- **Schottky-Clamped for High Speed:**
  Read Cycle Time . . . 25 ns Typical
  Write Cycle Time . . . 25 ns Typical
- **Choice of Three-State or Open-Collector Outputs**
- **Compatible with Most TTL and I^2L Circuits**
- **Chip-Select Input Simplifies External Decoding**

SN54S189B, SN54S289B . . . J OR W PACKAGE
SN74S189B, SN74S289B . . . J OR N PACKAGE
(TOP VIEW)



description

These 64-bit active-element memories are monolithic Schottky-clamped transistor-transistor logic (TTL) arrays organized as 16 words of four bits each. They are fully decoded and feature a chip-select input to simplify decoding required to achieve expanded system organization. The memories feature p-n-p input transistors that reduce the low-level input current requirement to a maximum of -0.25 milliamperes, only one-eighth that of a Series 54S/74S standard load factor. The chip-select circuitry is implemented with minimal delay times to compensate for added system decoding.

write cycle

The information applied at the data input is written into the selected location when the chip-select input and the write-enable input are low. While the write-enable input is low, the 'S189B output is in the high-impedance state and the 'S289B output is off. When a number of outputs are bus-connected, this high-impedance or off state will neither load nor drive the bus line, but it will allow the bus line to be driven by another active output or a passive pull-up.

read cycle

The stored information (complement of information applied at the data input during the write cycle) is available at the output when the write-enable input is high and the chip-select input is low. When the chip-select input is high, the 'S189B output will be in the high-impedance state and the 'S289B output will be off.

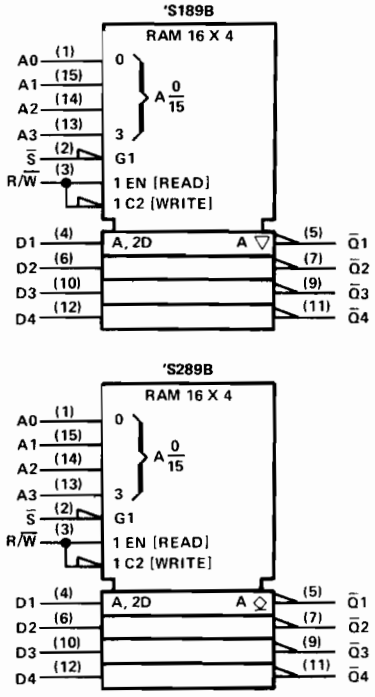
FUNCTION TABLE

FUNCTION	INPUTS		'S189B	'S289B
	CHIP SELECT	WRITE ENABLE	OUTPUT	OUTPUT
Write	L	L	High Impedance	Off
Read	L	H	Complement of Data Entered	Complement of Data Entered
Inhibit	H	X	High Impedance	Off

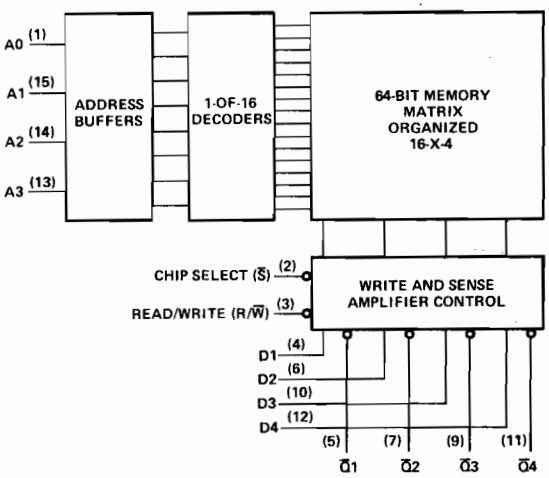
H = high level, L = low level, X = irrelevant

5 RAMs

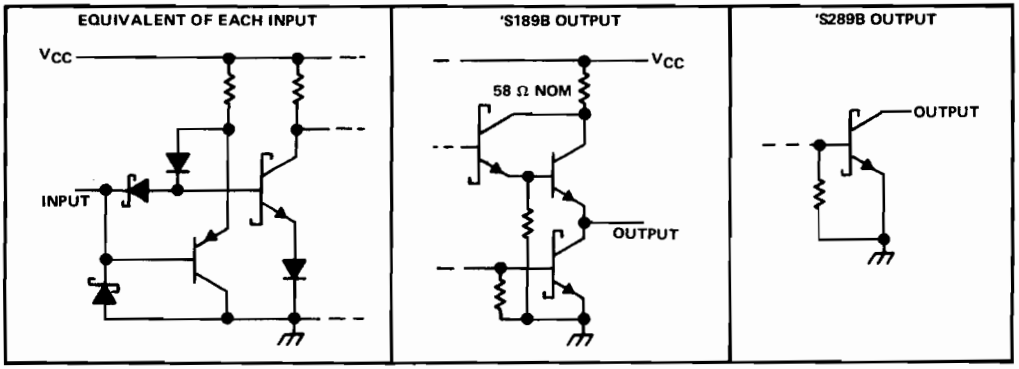
logic symbols



functional block diagram



schematics of inputs and outputs



5 RAMs

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Off-State output voltage . . . . . 5.5 V
Operating free-air temperature range: SN54S' Circuits . . . . . −55°C to 125°C
SN74S' Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

			SN54S'			SN74S'			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}			4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}		'S289B			5.5			5.5	V
High-level output current, I_{OH}		'S189B			−2			−6.5	mA
Low-level output current, I_{OL}					16			16	mA
Width of write pulse (write enable low), $t_{w(wr)}$			25			25			ns
Setup time	Address before write pulse, $t_{su(da)}$		0↓			0↓			ns
	Data before end of write pulse, $t_{su(da)}$		25↑			25↑			
	Chip-select before end of write pulse, $t_{su(\overline{S})}$		25↑			25↑			
Hold time	Address after write pulse, $t_{h(ad)}$		3↑			0↑			ns
	Data after write pulse, $t_{h(da)}$		0↑			0↑			
	Chip-select after write pulse, $t_{h(\overline{S})}$		0↑			0↑			
Operating free-air temperature, T_A			−55		125	0		70	°C

↑↓The arrow indicates the transition of the write-enable input used for reference: ↑ for the low-to-high transition, ↓ for the high-to-low transition.

5 RAMs

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		'S189B			'S289B			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.2			−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = MAX	SN54S'	2.4	3.4					V
			SN74S'	2.4	3.2					
I_{OH}	High-level output current	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V	V_O = 2.4 V						40	μA
			V_O = 5.5 V						100	
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA			0.35	0.5		0.35	0.5	V
I_{OZH}	Off-state output current, high-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = 0.8 V, V_{OH} = 2.4 V				50				μA
I_{OZL}	Off-state output current, low-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = 0.8 V, V_{OL} = 0.4 V				−50				μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				25			25	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5 V				−250			−250	μA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−30		−100				mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2			75	110		75	105	mA

NOTE 2: I_{CC} is measured with the read/write and chip-select inputs grounded. All other inputs at 4.5 V, and the outputs open.

'S189B switching characteristics over recommended operating ranges of T_A and V_{CC} (unless otherwise noted)

PARAMETER			TEST CONDITIONS	SN54S189B			SN74S189B			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
$t_{a(ad)}$	Access time from address		C_L = 30 pF, See Note 3		25	50		25	35	ns
$t_{a(S)}$	Access time from chip select (enable time)				18	25		18	22	ns
t_{SR}	Sense recovery time				22	40		22	35	ns
t_{PXZ}	Disable time from high or low level	From $\overline{S}$	C_L = 5 pF, See Note 3		12	25		12	17	ns
		From $\overline{W}$			12	30		12	25	

'S289B switching characteristics over recommended operating ranges of T_A and V_{CC} (unless otherwise noted)

PARAMETER			TEST CONDITIONS	SN54S289B			SN74S289B			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
$t_{a(ad)}$	Access time from address		C_L = 30 pF, R_{L1} = 300 Ω, R_{L2} = 600 Ω, See Note 3		25	50		25	35	ns
$t_{a(S)}$	Access time from chip-select (enable time)				18	25		18	22	ns
t_{SR}	Sense recovery time				22	40		22	35	ns
t_{PLH}	Propagation delay time, low-to-high-level output (disable time)	From $\overline{S}$			12	25		12	17	ns
		From $\overline{W}$			12	30		12	25	

†For conditions shown as MIN or MAX use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°.
§Duration of the short circuit should not exceed one second.
NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

TEXAS INSTRUMENTS
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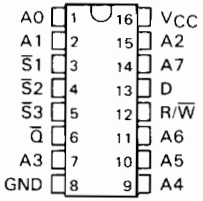
D2007, SEPTEMBER 1977 - FEBRUARY 1984

STATIC RANDOM-ACCESS MEMORIES

- **Static Fully Decoded RAM's Organized as 256 Words of One Bit Each**
- **Schottky-Clamped for High Performance**
- **Choice of Three-State or Open-Collector Outputs**
- **Compatible with Most TTL and I^2L Circuits**
- **Chip-Select Input Simplify External Decoding**
- **Typical Performance:**
  Read Access Time . . . 42 ns
  Power dissipation . . . 500 mW

SN74S201, SN74S301 . . . J OR N PACKAGE
(TOP VIEW)



description

These 256-bit active-element memories are monolithic transistor-transistor logic (TTL) arrays organized as 256 words of one bit. They are fully decoded and have three chip-select inputs to simplify decoding required to achieve expanded system organizations.

write cycle

The information applied at the data input is written into the selected location when the chip-select inputs and the write-enable input are low. While the write-enable input is low, the 'S201 outputs are in the high-impedance state and the 'S301 outputs are off. When a number of outputs are bus-connected, this high-impedance or off state will neither load nor drive the bus line, but it will allow the bus line to be driven by another active output or a passive pull-up.

read cycle

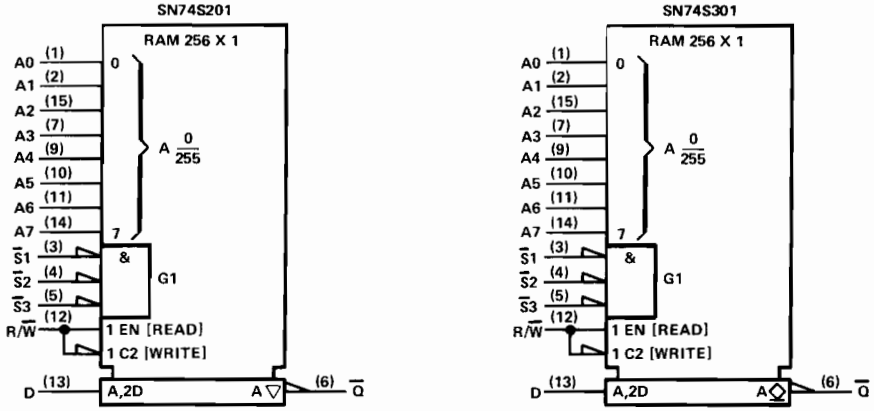
The stored information (complement of information applied at the data input during the write cycle) is available at the output when the write-enable input is high and the three chip-select inputs is low. When any one of the chip-select inputs are high, the 'S201 outputs will be in the high-impedance state and the 'S301 outputs will be off.

FUNCTION TABLE

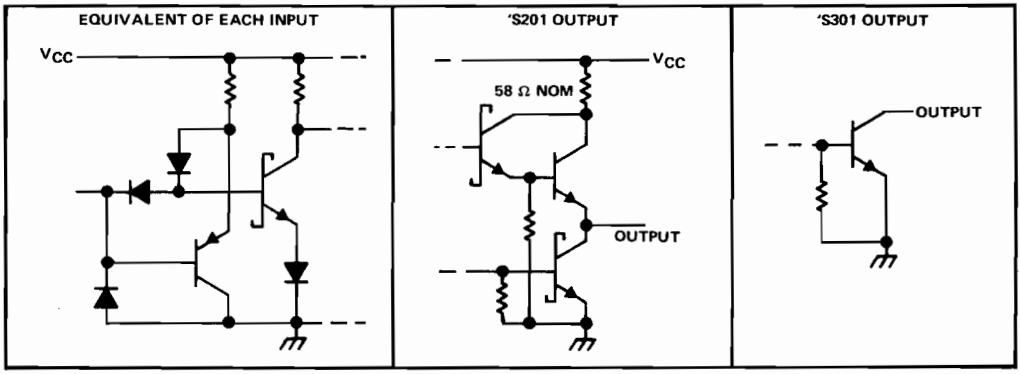
FUNCTION	INPUTS		'S201 OUTPUT ($\overline{Q}$)	'S301 OUTPUT ($\overline{Q}$)
	CHIP SELECT $\overline{S}$	WRITE ENABLE R/$\overline{W}$		
Write	L	L	High Impedance	Off
Read	L	H	Complement of Data Entered	Complement of Data Entered
Inhibit	H	X	High Impedance	Off

H = high level, L = low level, X = irrelevant
For chip-select: L = all $\overline{S}i$ inputs low, H = one or more $\overline{S}i$ inputs high

logic symbols



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Off-State output voltage	5.5 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

recommended operating conditions

		SN74S201			SN74S301			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 1)		4.75	5	5.25	4.75	5	5.25	V
High-level output voltage, V_{OH}							5.5	V
High-level output current, I_{OH}				−10.3				mA
Low-level output current, I_{OL}				16			16	mA
Width of write pulse (write enable low), $t_{w(wr)}$		65			65			ns
Setup time	Address before write pulse, $t_{su(ad)}$	0↓			0↓			ns
	Data before end of write pulse, $t_{su(da)}$	65↑			65↑			
	Chip-select before end of write pulse, $t_{su(\overline{S})}$	65↑			65↑			
Hold time	Address after write pulse, $t_{h(ad)}$	0↑			0↑			ns
	Data after write pulse, $t_{h(da)}$	0↑			0↑			
	Chip-select after write pulse, $t_{h(\overline{S})}$	0↑			0↑			
Operating free-air temperature, T_A		0		70	0		70	°C

↑↓The arrow indicates the transition of the write-enable input used for reference: ↑ for the low-to-high transition, ↓ for the high-to-low transition.
NOTE 1: Voltage values are with respect to network ground terminal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		'S201			'S301			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.2			−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = MAX		2.4						V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 16 mA				0.45			0.45	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V	V_O = 2.4 V						40	μA
			V_O = 5.5 V						100	
I_{OZH}	Off-state output current, high-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = 0.8 V, V_{OH} = 2.4 V				40				μA
I_{OZL}	Off-state output current, low-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = 0.8 V, V_{OL} = 0.5 V				−40				μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				25			25	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5 V				−250			−250	μA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−30		−100				mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2			100	140		100	140	mA

†For conditions shown as MIN or MAX use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Duration of the short circuit should not exceed one second.
NOTE 2: I_{CC} is measured with all chip-select inputs grounded, all other inputs at 4.5 V, and the output open.

'S201 switching characteristics over recommended operating ranges of T_A and V_{CC} (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
$t_{a(ad)}$	Access time from address		C_L = 30 pF, See Note 3		42	65	ns
$t_{a(S)}$	Access time from chip select (select time)				13	30	ns
t_{SR}	Sense recovery time				20	40	ns
t_{PXZ}	Disable time from high or low level	From $\overline{S}$	C_L = 5 pF, See Note 3		9	20	ns
		From R/$\overline{W}$					

'S301 switching characteristics over recommended operating ranges of T_A and V_{CC} (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
$t_{a(ad)}$	Access time from address		C_L = 30 pF, R_{L1} = 300 Ω, R_{L2} = 600 Ω, See Note 3		42	65	ns
$t_{a(S)}$	Access time from chip enable (enable time)				13	30	ns
t_{SR}	Sense recovery time				20	40	ns
t_{PLH}	Propagation delay time, low-to-high-level output (disable time)	From $\overline{S}$			8	20	ns
		From R/$\overline{W}$			15	35	

‡All typical values are at V_{CC} = 5 V, T_A = 25°.
NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

MAY 1972 -- REVISED DECEMBER 1983

- Fast Multiplication of Two Binary Numbers 8-Bit Product in 40 ns Typical
- Expandable for N-Bit-by-n-Bit Applications: 16-Bit Product in 70 ns Typical 32-Bit Product in 103 ns Typical
- Fully Compatible with Most TTL Circuits
- Diode-Clamped Inputs Simplify System Design

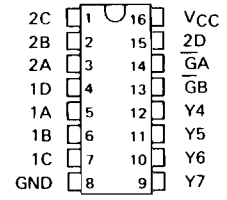
description

These high-speed TTL circuits are designed to be used in high-performance parallel multiplication applications. When connected as shown in Figure A, these circuits perform the positive-logic multiplication of two 4-bit binary words. The eight-bit binary product is generated with typically only 40 nanoseconds delay.

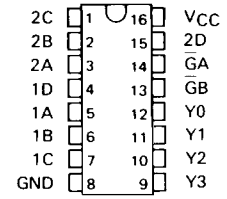
This basic four-by-four multiplier can be utilized as a fundamental building block for implementing larger multipliers. For example, the four-by-four building blocks can be connected as shown in Figure B to generate submultiple partial products. These results can then be summed in a Wallace tree, and, as illustrated, will produce a 16-bit product for the two eight-bit words typically in 70 nanoseconds. SN54H183/SN74H183 carry-save adders and SN54S181/SN74S181 arithmetic logic units with the SN54S182/SN74S182 look-ahead generator are used to achieve this high performance. The scheme is expandable for implementing N × M bit multipliers.

The SN54284 and SN54285 are characterized for operation over the full military temperature range of −55°C to 125°C; the SN74284 and SN74285 are characterized for operation from 0°C to 70°C.

SN54284 . . . J OR W PACKAGE
SN74284 . . . J OR N PACKAGE
(TOP VIEW)

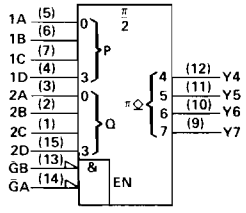


SN54285 . . . J OR W PACKAGE
SN74285 . . . J OR N PACKAGE
(TOP VIEW)

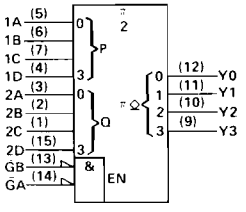


logic symbols

'284



'285



Pin numbers shown are for J and N packages.

5 RAMs

schematics

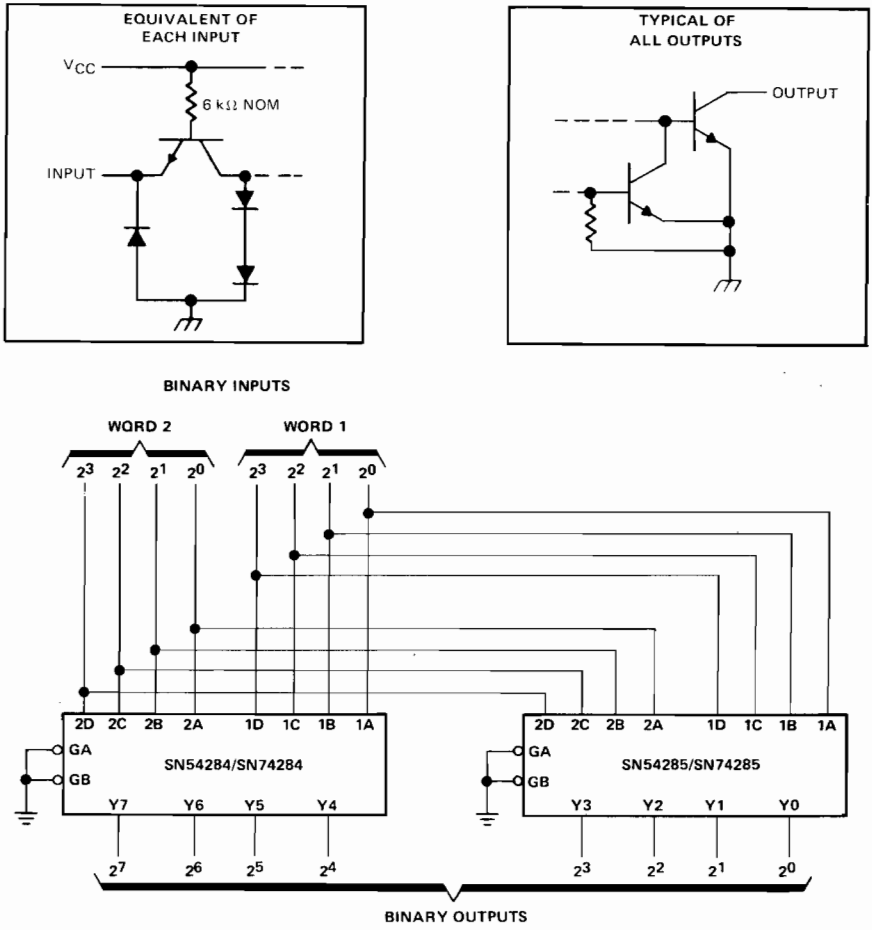


FIGURE A–4 X 4 MULTIPLIER

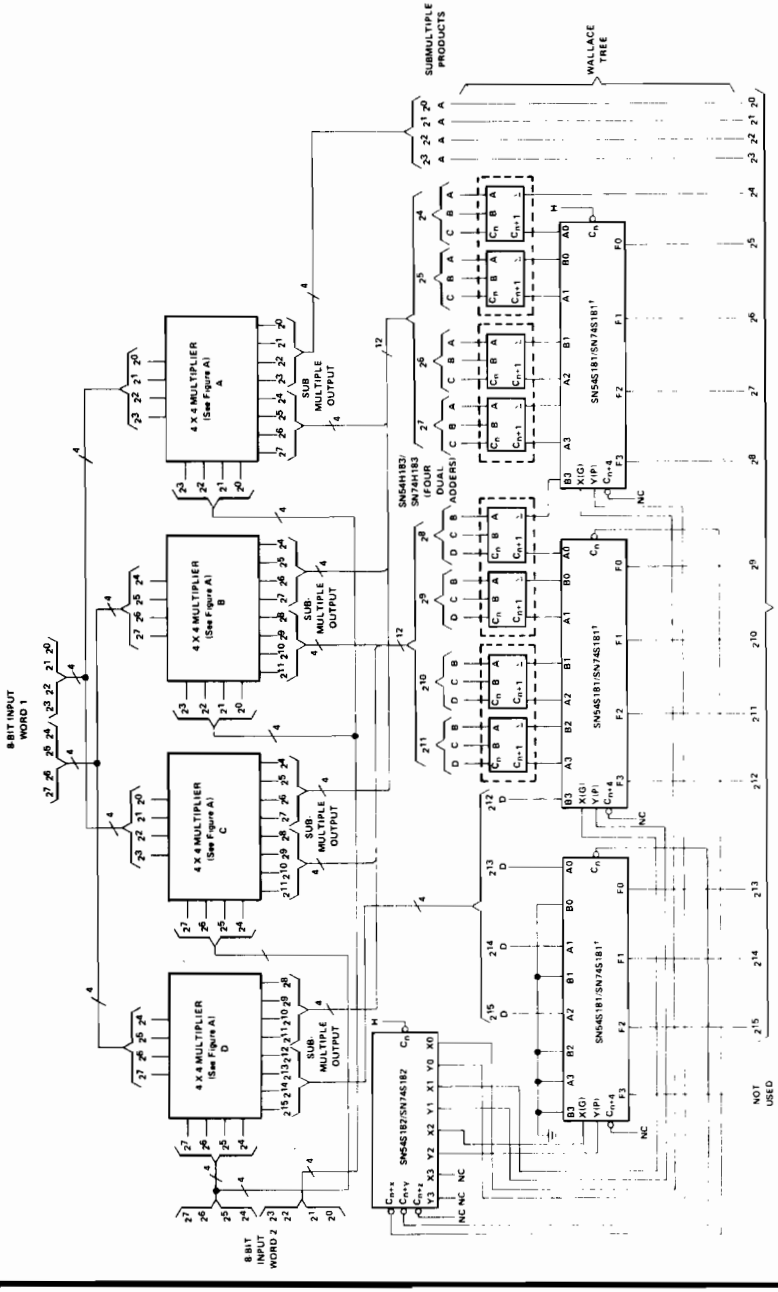


FIGURE 8–8 X 8 MULTIPLIER

† Other terminals of the three SN54S181/SN74S181 ALU's are connected as follows: S3 = H, S2 = L, S1 = L, S0 = H, M = L. Output A = B is not used for this application.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN54' Circuits . . . . . −55°C to 125°C
SN74' Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54284 SN54285			SN74284 SN74285			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}			5.5			5.5	V
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA				−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, V_{OH} = 5.5 V				40	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V	I_{OL} = 12 mA			0.4	V
			I_{OL} = 16 mA			0.45	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V				40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−1	mA
I_{CC}	Supply current	V_{CC} = MAX, T_A = 125°C, See Note 2	SN54284, SN54285 N package only			99	mA
		V_{CC} = MAX, See Note 2	SN54284, SN54285		92	110	
			SN74284, SN74285		92	130	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: With outputs open and both enable inputs grounded, I_{CC} is measured first by selecting an output product which contains three or more high-level bits, then by selecting an output product which contains four low-level bits.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from enable	C_L = 30 pF to GND, R_{L1} = 300 Ω to V_{CC}, R_{L2} = 600 Ω to GND, See Note 3		20	30	ns
t_{PHL}	Propagation delay time, high-to-low-level output from enable			20	30	
t_{PLH}	Propagation delay time, low-to-high-level output from word inputs			40	60	ns
t_{PHL}	Propagation delay time, high-to-low-level output from word inputs			40	60	

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

TEXAS INSTRUMENTS
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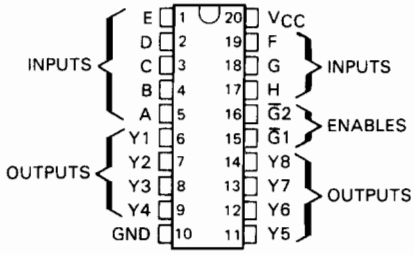
SN54S484A, SN54S485A, SN74S484A, SN74S485A
BCD-TO-BINARY AND BINARY-TO-BCD CONVERTERS

D2534, JUNE 1979–REVISED FEBRUARY 1984

SN54S484A, SN74S484A, BCD-TO-BINARY CONVERTERS
SN54S485A, SN74S485A BINARY-TO-BCD CONVERTERS

- **Significant Savings in Package Count Compared with SN54184, SN54185A, SN74184, or SN74185A (Over Half in Many Applications)**
- **Three-State Outputs**

SN54S484A, SN54S485A . . . J PACKAGE
SN54S484A, SN54S485A . . . J OR N PACKAGE
(TOP VIEW)



description

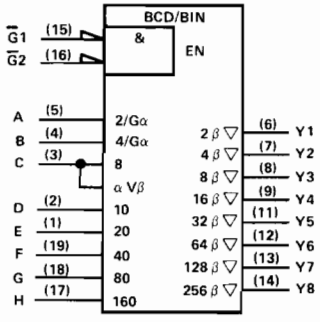
These monolithic converters are derived from the TBP28L22 factory-programmed read-only memories. Both of these converters comprehend that the least-significant bits (LSB) of the binary and BCD are logically equal, and in each case, the LSB bypasses the converter as shown in the typical applications. This means that a nine-bit converter is produced in each case. The devices are cascadable to N bits.

The three-state outputs offer the convenience of open-collector outputs with the speed of totem-pole outputs: they can be bus-connected to other similar outputs yet they retain the fast rise-time characteristic of totem-pole outputs. A high logic level at either enable ($\overline{G}$) input causes the outputs to be in high-impedance state.

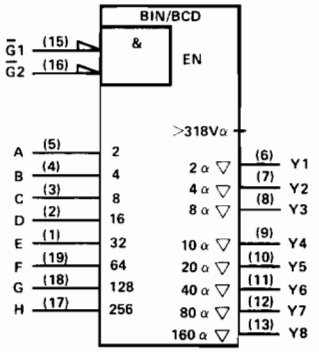
In many applications these converters can, by including 3 more bits than the SN54184/SN74184 or SN54185A/SN74185A, reduce power consumption significantly and package count by more than half as shown in the tables below.

logic symbols

SN54S484A
SN74S484A



SN54S485A
SN74S485A



5 RAMs

TEXAS INSTRUMENTS
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SN54S484A/SN74S484A vs SN54184/SN74184

DECADES	PACKAGE COUNT		MAXIMUM SUPPLY CURRENT (A)		TYPICAL ACCESS TIME @ T_A = 25°C (ns)	
	'S484A	'184	'S484A	'184	'S484A	'184
3	3	6	0.41	0.59	117	135
4	5	11	0.72	1.09	180	189
5	8	18	1.18	1.78	270	270
6	12	27	1.75	2.67	342	351
7	16	38	2.37	3.76	405	405
8	21	49	3.14	4.85	495	485
9	27	62	4.02	6.14	567	540

SN54S485A/SN74S485A vs SN54185A/SN74185A

BINARY BITS	PACKAGE COUNT		MAXIMUM SUPPLY CURRENT (A)		TYPICAL ACCESS TIME @ T_A = 25°C (ns)	
	'S485A	'185A	'485A	'185A	'S485A	'185A
8	2	3	0.25	0.30	72	81
16	8	16	1.12	1.58	252	216
24	19	40	2.67	3.96	459	351
32	33	74	4.78	5.45	612	486

TEXAS INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

SN54S484A, SN74S484A
BCD-TO-BINARY CONVERTER
FUNCTION TABLE

INPUTS								OUTPUTS							
H	G	F	E	D	C	B	A	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1
160	80	40	20	10	8	4	2	256	128	64	32	16	8	4	2
L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	H
L	L	L	L	L	L	H	L	L	L	L	L	L	L	H	L
L	L	L	L	L	L	H	H	L	L	L	L	L	L	H	H
L	L	L	L	L	H	L	L	L	L	L	L	L	H	L	L
L	L	L	L	L	H	L	H	Invalid BCD code (All outputs are high)							
L	L	L	L	L	H	H	L								
L	L	L	L	L	H	H	H								
L	L	L	L	H	L	L	L	L	L	L	L	L	H	L	H
L	L	L	L	H	L	L	H	L	L	L	L	L	H	H	L
L	L	L	L	H	L	H	L	L	L	L	L	L	H	H	H
H	H	H	H	L	L	H	L	H	L	L	H	H	L	L	L
H	H	H	H	L	L	H	H	H	L	L	H	H	L	L	H
H	H	H	H	L	H	L	L	H	L	L	H	H	L	H	L
H	H	H	H	L	H	L	H								
H	H	H	H	L	H	H	L								
H	H	H	H	L	H	H	H								
H	H	H	H	H	L	L	L	H	L	L	H	H	L	H	H
H	H	H	H	H	L	L	H	H	L	L	H	H	H	L	L
H	H	H	H	H	L	H	L	H	L	L	H	H	H	H	L
H	H	H	H	H	L	H	H	H	L	L	H	H	H	H	H
H	H	H	H	H	H	L	L								
H	H	H	H	H	H	L	H								
H	H	H	H	H	H	H	L								
H	H	H	H	H	H	H	H								
X	X	X	X	X	H	X	H	H	H	H	H	H	H	H	H
X	X	X	X	X	H	H	X	H	H	H	H	H	H	H	H

H = high level L = low level X = irrelevant

SN54S485A, SN74S485A
BINARY-TO-BCD CONVERTER
FUNCTION TABLE

INPUTS								OUTPUTS							
H	G	F	E	D	C	B	A	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1
256	128	64	32	16	8	4	2	160	80	40	20	10	8	4	2
L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	H
L	L	L	L	L	L	H	L	L	L	L	L	L	L	H	L
L	L	L	L	L	L	H	H	L	L	L	L	L	L	H	H
L	L	L	L	L	H	L	L	L	L	L	L	L	H	L	L
L	L	L	L	L	H	L	H	L	L	L	L	H	L	L	H
L	L	L	L	L	H	H	L	L	L	L	L	H	L	H	L
L	L	L	L	L	H	H	H	L	L	L	L	H	L	H	H
L	L	L	L	H	L	L	L	L	L	L	H	L	L	L	L
L	L	L	L	H	L	L	H	L	L	L	H	L	L	L	H
L	L	L	L	H	L	H	L	L	L	L	H	L	L	H	L
L	L	L	L	H	L	H	H	L	L	L	H	L	L	H	H
L	L	L	L	H	H	L	L	L	L	L	H	L	H	L	L
L	L	L	L	H	H	L	H	L	L	L	H	L	H	L	H
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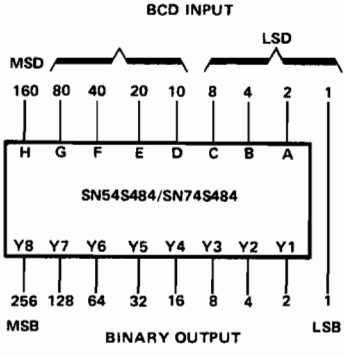
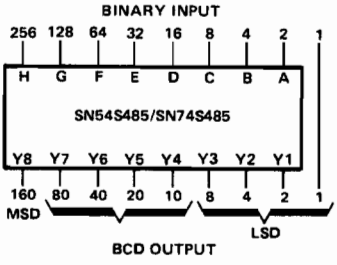
H	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H
H	L	L	H	H	L	L	L	H	H	H	H	L	L	L	L
H	L	L	H	H	L	L	H	H	H	H	H	L	L	L	H
H	L	L	H	H	L	H	L	H	H	H	H	L	L	H	L
H	L	L	H	H	L	H	H	H	H	H	H	L	L	H	H
H	L	L	H	H	H	L	L	H	H	H	H	L	H	L	L
H	L	L	H	H	H	L	H	H	H	H	H	L	H	L	H
H	L	L	H	H	H	H	L	H	H	H	H	L	H	H	L
H	L	L	H	H	H	H	H	H	H	H	H	L	H	H	H
H	L	H	L	L	L	L	L	H	H	H	H	H	H	H	H
thru															
H	H	H	H	H	H	H	H								





absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Off-state output voltage . . . . . 5.5 V
Operating free-air temperature range: SN54S484A, SN54S485A . . . . . −55°C to 125°C
SN74S484A, SN74S485A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

	SN54S'			SN74S'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−2			−6.5	mA
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA				−1.2	V
V_{OH}	High-level output voltage	V_{VV} = MIN, I_{OH} = MAX	V_{IH} = 2 V,	V_{IL} = 0.8 V,	2.4	3.1		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, I_{OL} = MAX	V_{IH} = 2 V,	V_{IL} = 0.8 V			0.5	V
I_{OZH}	Off-state output current, high-level voltage applied	V_{CC} = MAX,	V_{IH} = 2 V,	V_O = 2.4 V			50	μA
I_{OZL}	Off-state output current, low-level voltage applied	V_{CC} = MAX,	V_{IH} = 2 V,	V_O = 0.5 V			−50	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7 V				25	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.5 V				−0.25	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX,			−30		−100	mA
I_{CC}	Supply current	V_{CC} = MAX,	See Note 2			75	100	mA

switching characteristics over recommended ranges of T_A and V_{CC} (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN54S'			SN74S'			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
$t_{a(A)}$	Access time from address	C_L = 30 pF, See Note 3		45	75		45	70	ns
$t_{a(S)}$	Access time from chip select			20	40		20	35	ns
t_{PXZ}	Output disable time	C_L = 5 pF, See Note 3		15	35		15	30	ns

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating condtions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°.
§Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
NOTES: 1. Voltage values are with respect to network ground terminal.
2. With outputs open and enable (G) inputs grounded, I_{CC} is measured first by selecting a word that contains the maximum number of high-level outputs, then by selecting a word that contains the maximum number of low-level inputs.
3. Load circuits and voltage waveforms are shown in Section 1.

TEXAS INSTRUMENTS
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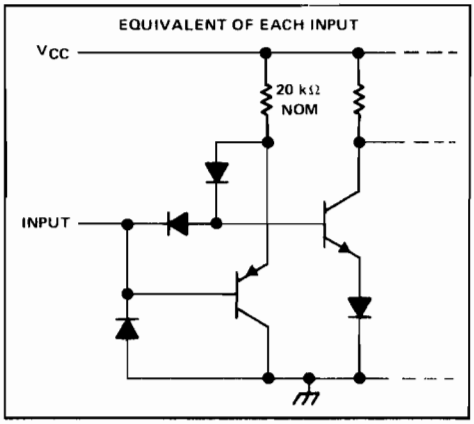
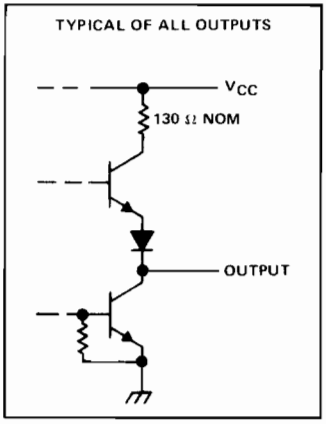
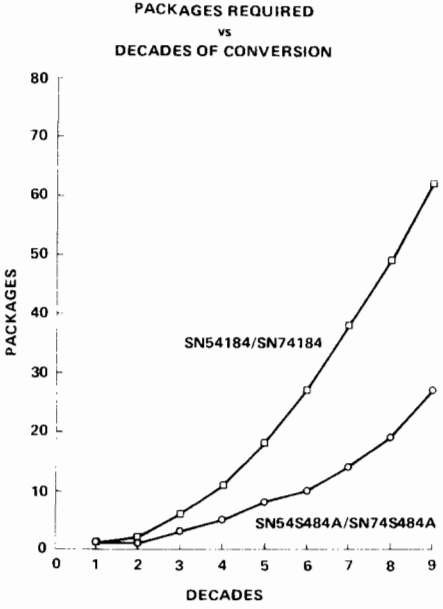
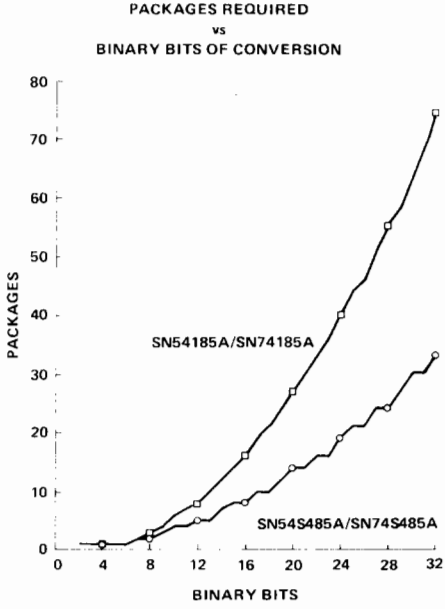
schematics of inputs and outputs



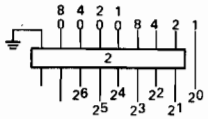


TYPICAL APPLICATION DATA

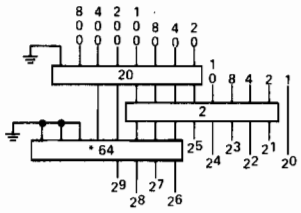




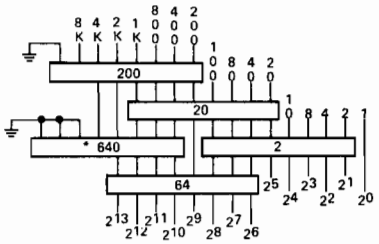
TYPICAL APPLICATION DATA
SN54S484A, SN74S484A



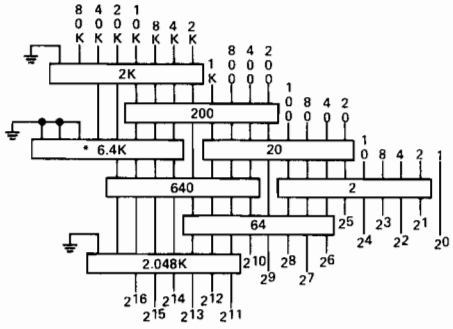
2-DECADE-
BCD-TO-BINARY
CONVERTER



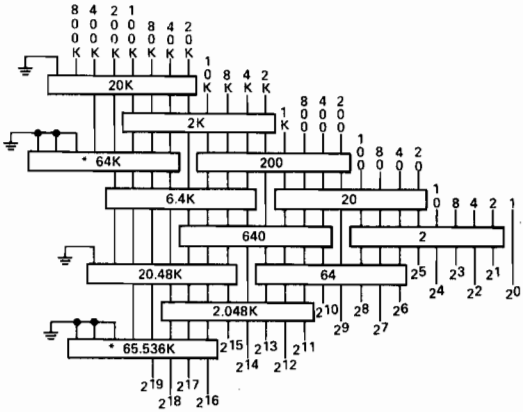
3-DECADE-
BCD-TO-BINARY
CONVERTER



4-DECADE-
BCD-TO-BINARY
CONVERTER



5-DECADE-
BCD-TO-BINARY
CONVERTER



6-DECADE-BCD-TO-BINARY
CONVERTER

*SN54184A/SN74184A can be used.
K = 10^3, M = 10^6

5 RAMs

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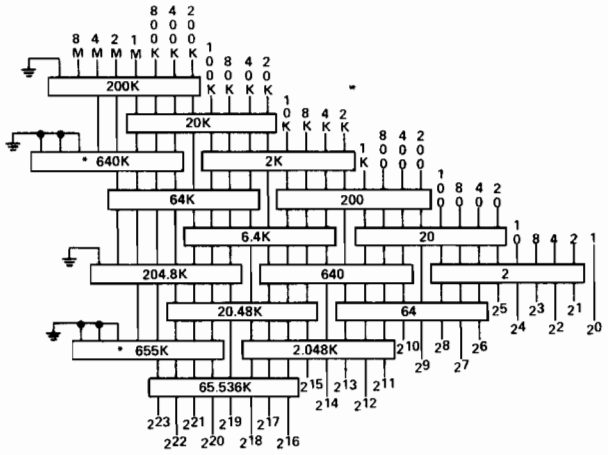
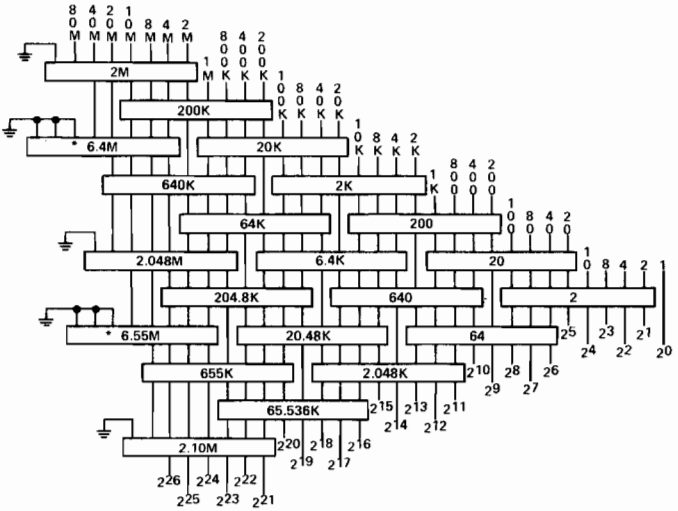
TYPICAL APPLICATION DATA
SN54S484A, SN74S484A



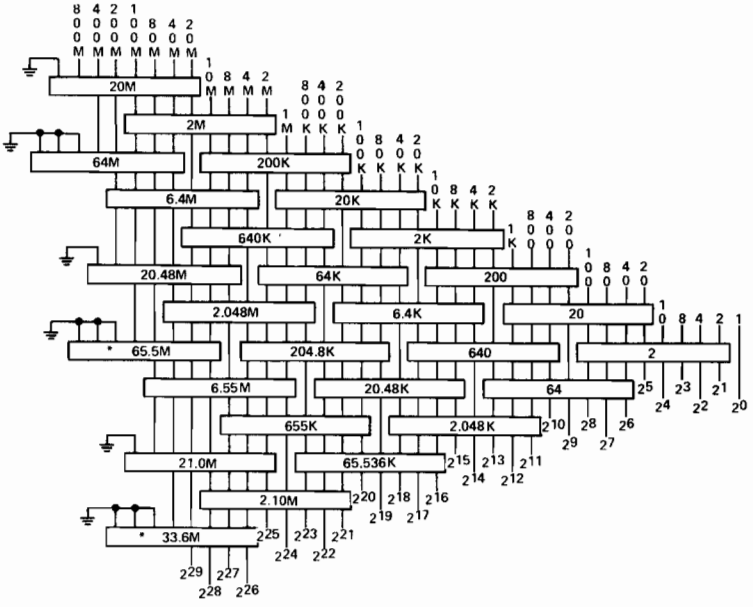
7-DECADE-BCD-TO-BINARY CONVERTER



8-DECADE-BCD-TO-BINARY CONVERTER

*SN54184A/SN74184A can be used.
K = 10^3, M = 10^6

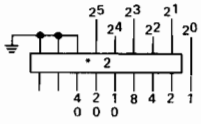
TYPICAL APPLICATION DATA
SN54S484A, SN74S484A



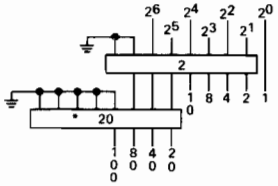
9-DECADE-BCD-TO-BINARY CONVERTER

*SN54184A/SN74184A can be used.
K = 10^3, M = 10^6

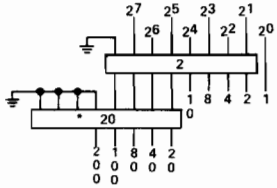
TYPICAL APPLICATION DATA
SN54S485A, SN74S485A



6-BIT-BINARY-TO-BCD CONVERTER



7-BIT-BINARY-TO-BCD CONVERTER



8-BIT-BINARY-TO-BCD CONVERTER

*SN54185A/SN74185A can be used.
K = 10^3, M = 10^6

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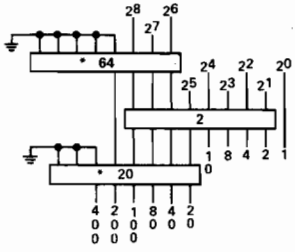
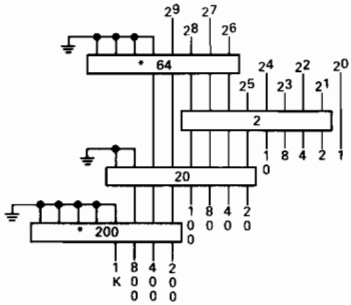
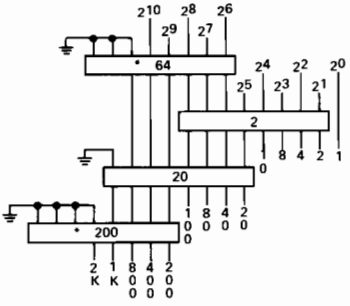
TYPICAL APPLICATION DATA
SN54S485A, SN74S485A



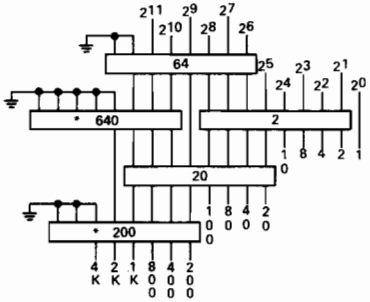
9-BIT-BINARY-TO-BCD CONVERTER



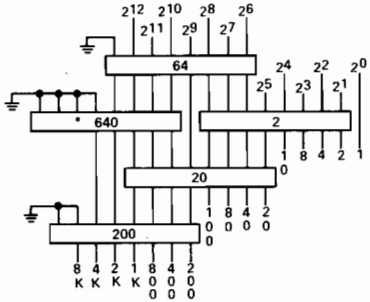
10-BIT-BINARY-TO-BCD CONVERTER



11-BIT-BINARY-TO-BCD CONVERTER



12-BIT-BINARY-TO-BCD CONVERTER

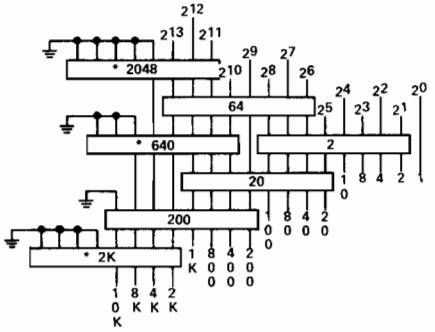


13-BIT-BINARY-TO-BCD CONVERTER

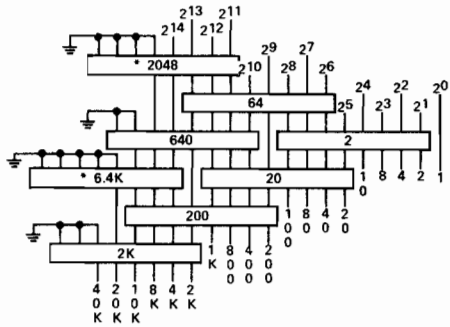
*SN54185A/SN74185A can be used.
K = 10^3, M = 10^6

5 RAMs

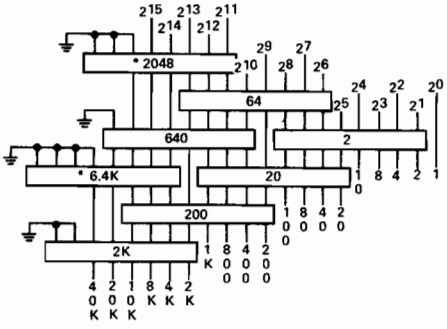
TYPICAL APPLICATION DATA
SN54S485A, SN74S485A



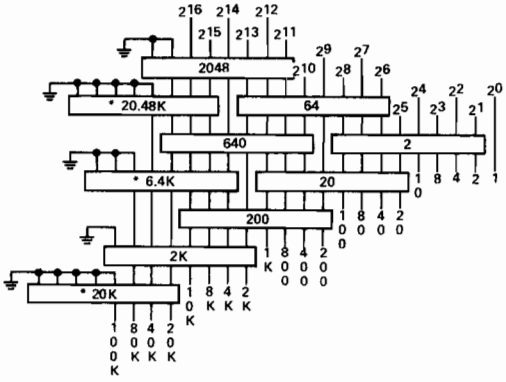
14-BIT-BINARY-TO-BCD CONVERTER



15-BIT-BINARY-TO-BCD CONVERTER



16-BIT-BINARY-TO-BCD CONVERTER



17-BIT-BINARY-TO-BCD CONVERTER

*SN54185A/SN74185A can be used.
K = 10^3, M = 10^6

5 RAMs

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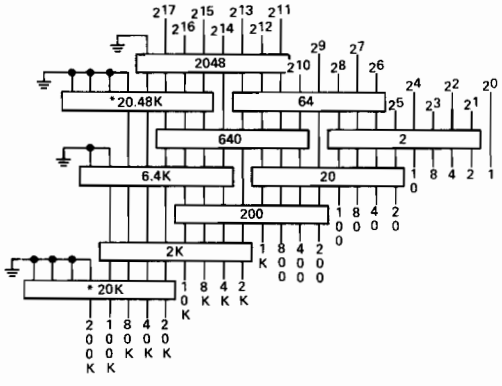
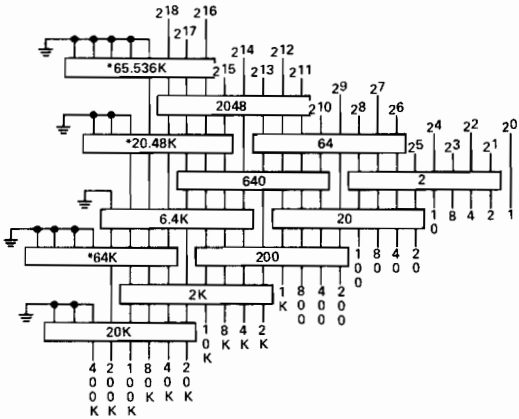
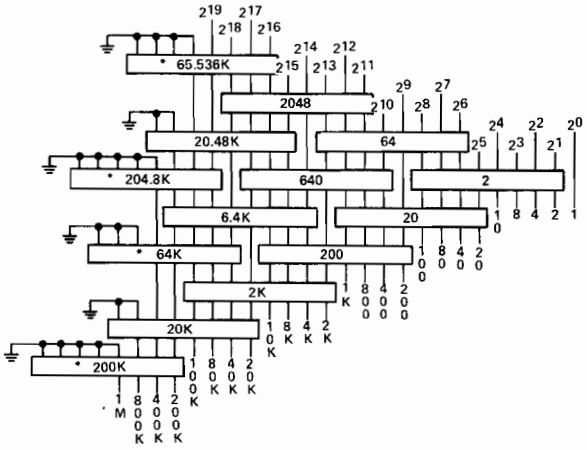
TYPICAL APPLICATION DATA
SN54S485A, SN74S485A



18-BIT-BINARY-TO-BCD CONVERTER



19-BIT-BINARY-TO-BCD CONVERTER

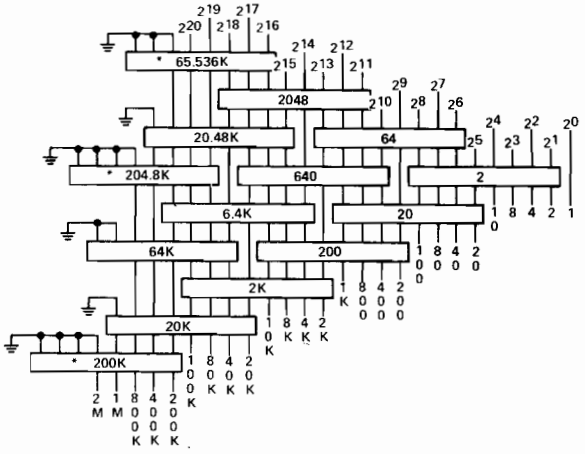


20-BIT-BINARY-TO-BCD CONVERTER

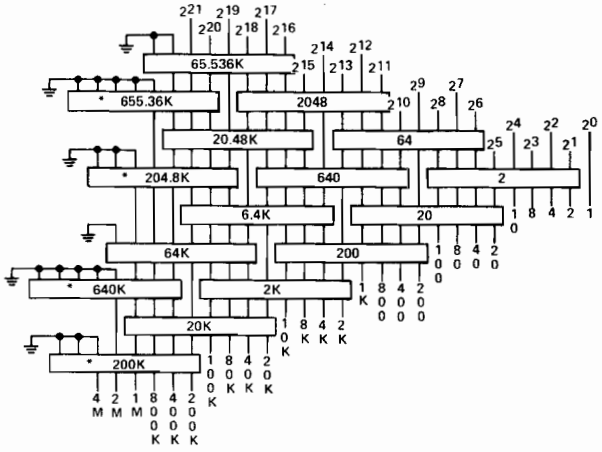
*SN54185A/SN74185A can be used.
K = 10^3, M = 10^6

5 RAMs

TYPICAL APPLICATION DATA
SN54S485A, SN74S485A



21-BIT-BINARY-TO-BCD CONVERTER



22-BIT-BINARY-TO-BCD CONVERTER

*SN54185A/SN74185A can be used.
K = 10^3, M = 10^6

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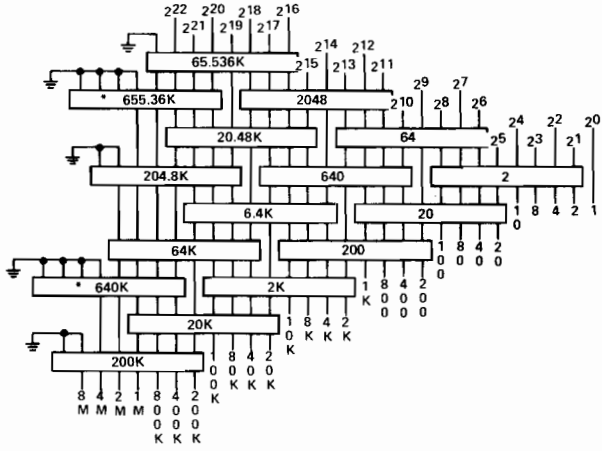
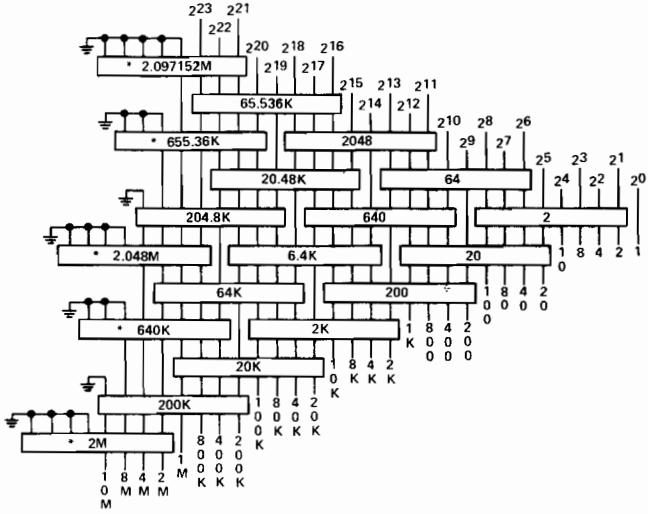
TYPICAL APPLICATION DATA
SN54S485A, SN74S485A



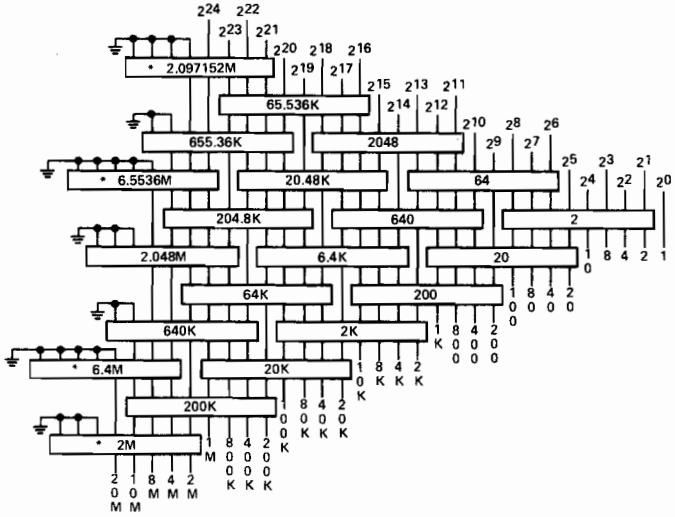
23-BIT-BINARY-TO-BCD-CONVERTER



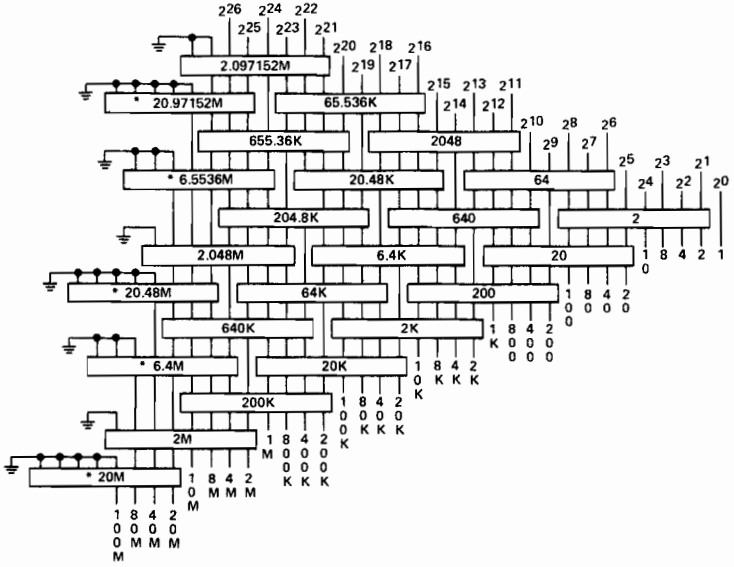
24-BIT-BINARY-TO-BCD CONVERTER

*SN54185A/SN74185A can be used.
K = 10^3, M = 10^6

TYPICAL APPLICATION DATA
SN54S485A, SN74S485A



25-BIT-BINARY-TO-BCD CONVERTER



26-BIT-BINARY-TO-BCD CONVERTER

*SN54185A/SN74185A can be used.
K = 10^3, M = 10^6

TEXAS INSTRUMENTS
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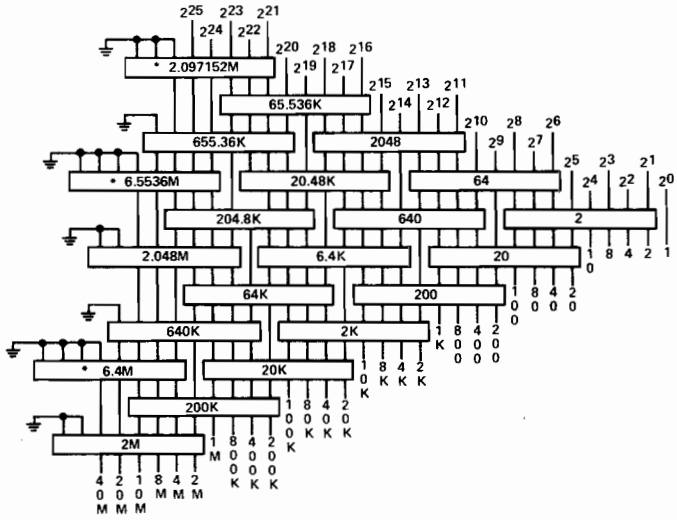
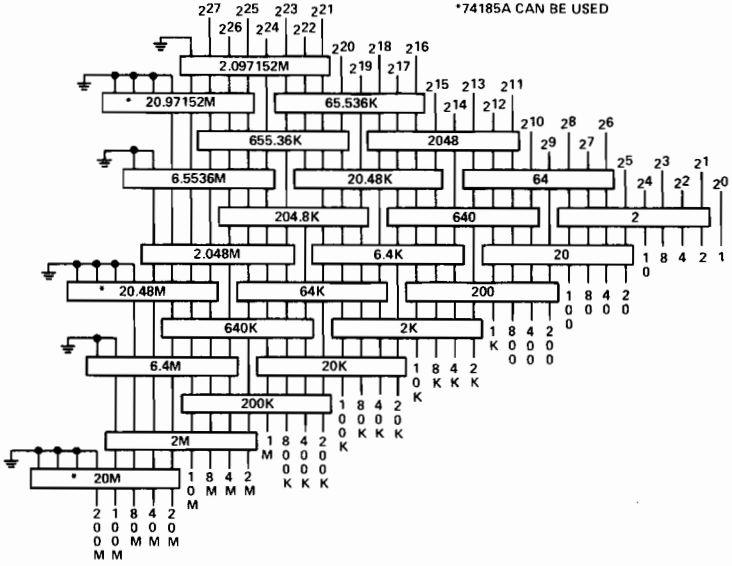
TYPICAL APPLICATION DATA
SN54S485A, SN74S485A



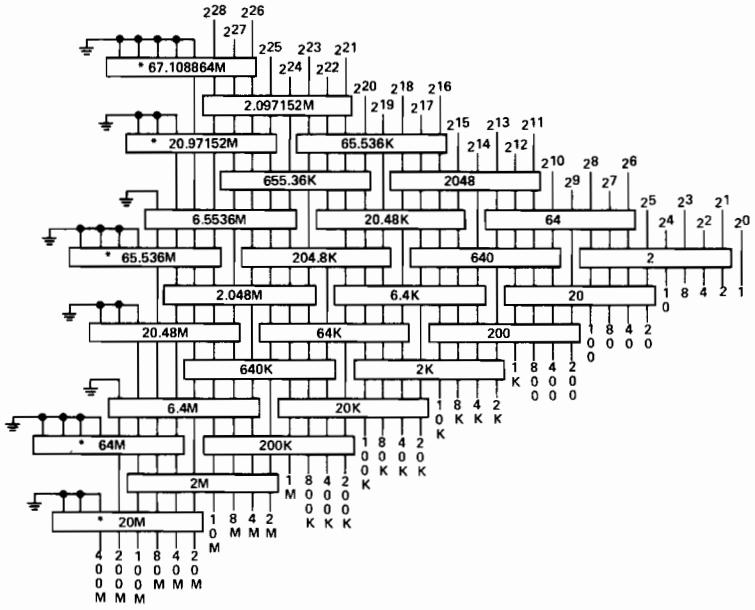
27-BIT-BINARY-TO-BCD CONVERTER



28-BIT-BINARY-TO-BCD CONVERTER

*SN54185A/SN74185A can be used.
K = 10^3, M = 10^6

TYPICAL APPLICATION DATA
SN54S485A, SN74S485A



29-BIT-BINARY-TO-BCD CONVERTER

*SN54185A/SN74185A can be used.
K = 10^3, M = 10^6

5 RAMs

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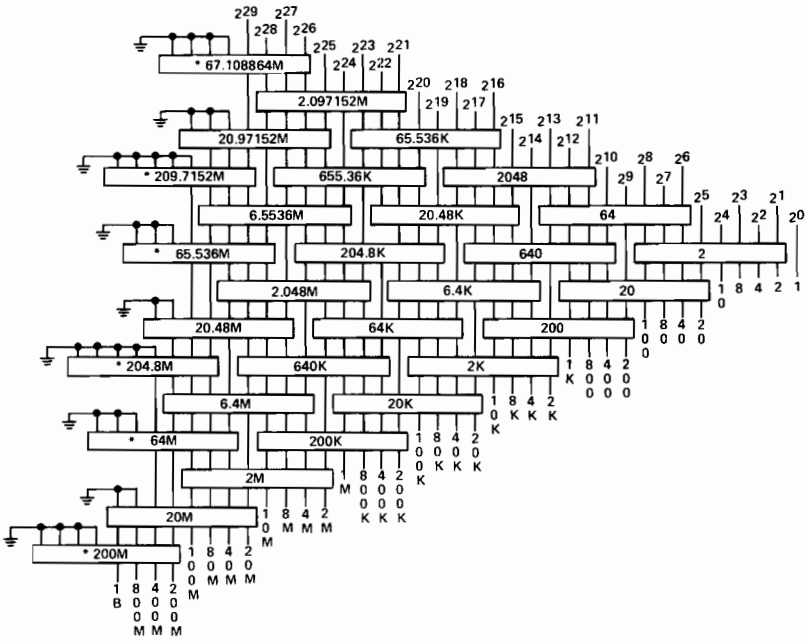
TYPICAL APPLICATION DATA
SN54S485A, SN74S485A



30-BIT-BINARY-TO-BCD CONVERTER

*SN54185A/SN74185A can be used.
K = 10^3, M = 10^6

TYPICAL APPLICATION DATA
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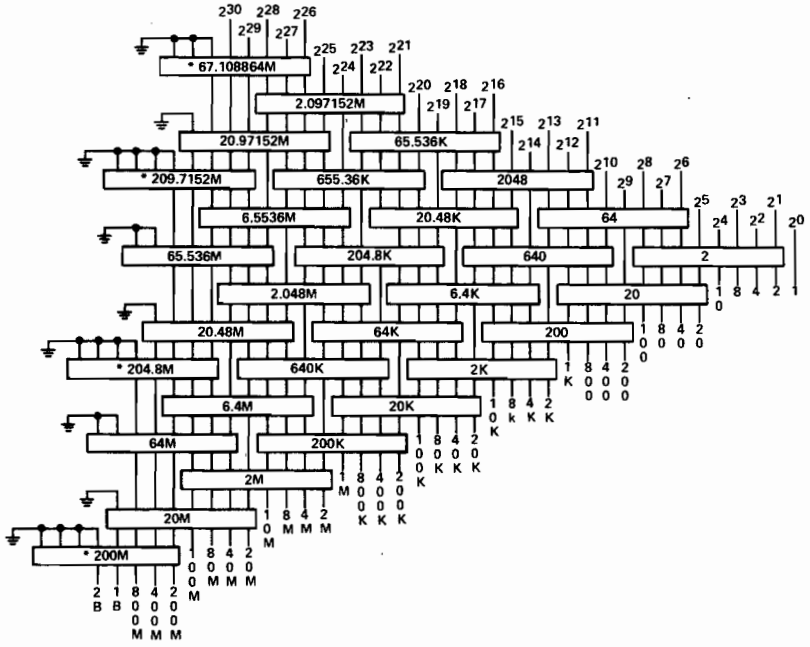

31-BIT-BINARY-TO-BCD CONVERTER

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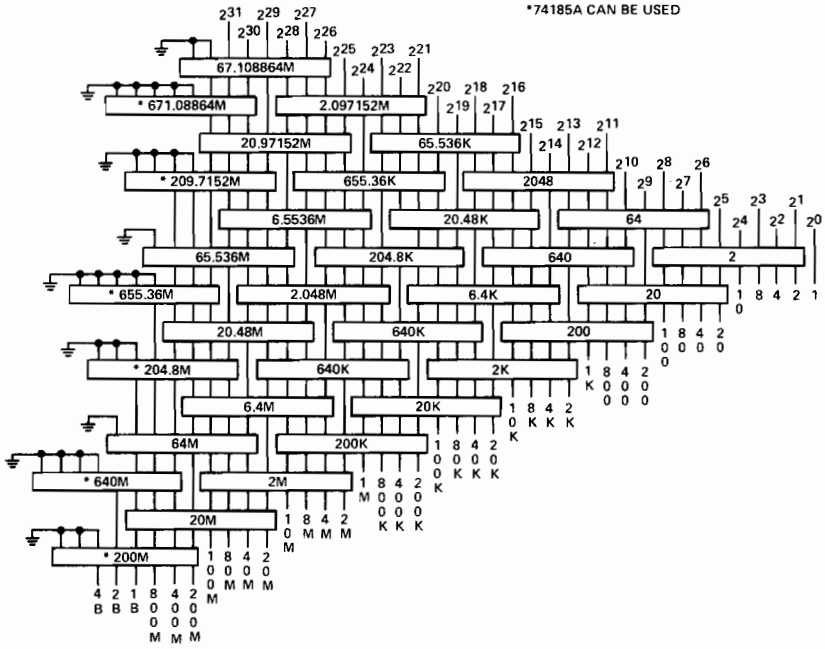
TYPICAL APPLICATION DATA
SN54S485A, SN74S485A



32-BIT-BINARY-TO-BCD CONVERTER

*SN54185A/SN74185A can be used.
K = 10^3, M = 10^6

General Information 1

Functional Index 2

Field-Programmable Logic 3

PROMs 4

RAMs and Memory-Based Code Converters 5

Designing with Texas Instruments Field-Programmable Logic 6

Mechanical Data 7

Designing with Texas Instruments Field-Programmable Logic

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Contents

Title	Page
FIELD-PROGRAMMABLE LOGIC ADVANTAGES	1
PAL® and FPLA Symbology	1
Family Architectures	2
PAL Options	3
Polarity Fuse	3
Input Registers	3
Input Latches	3
Programming	6
Design Example	6
Example Requirements	7
PAL Implementation	7
PAL Selection	8
Clock Selector Details	8
4-Bit Binary Counter Details	10
Binary/Decade Count Details	10
Fuse Map Details	11
Advanced Software	15
Performance	15
ADDRESS FOR PROGRAMMING AND SOFTWARE MANUFACTURERS	18
Hardware Manufacturers	18
Software Manufacturers	18

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List of Illustrations

Figure	*Title*	*Page*
1	Basic Symbology	1
2	Basic Symbology Example	2
3	PROM Architecture	2
4	PAL Architecture	2
5	FPLA Architecture	3
6	TIBPAL16L8 Logic Diagram	4
7	TIBPAL16R8 Logic Diagram	5
8	Polarity Selection	6
9	Input Register Selection	6
10	Input Latch Selection	7
11	PAL Process Flow Diagram	7
12	Counter Implementation With Standard Logic	8
13	TIBPAL16R4 Logic Diagram	9
14	Karnaugh Map for CLKOUT	10
15	Karnaugh Map for $\overline{\text{CLKOUT}}$	10
16	Karnaugh Maps	11
17	TIBPAL16R4 Logic Diagram	12
18	Pin ID and Logic Equations	13
19	Fuse Map	14
20	Source File for ABEL	16
21	ABEL Output Documentation	17

List of Tables

Table	*Title*	*Page*
1	Clock Selection	7
2	Function Table	8
3	Truth Table	10
4	Truth Table	11

INTRODUCTION

The purpose of this application report is to provide the first time user of field-programmable logic with a basic understanding of this new and powerful technology. The term "Field-Programmable Logic" refers to any device supplied with an uncommitted logic array, which the user programs to his own specific function. The most common, and widely known field-programmable logic family is the PROM, or Programmable Read-Only Memory. Relatively new entries into this expanding family of devices are the PAL® and FPLA. This report will primarily concentrate on the PAL family of programmable logic.

FIELD-PROGRAMMABLE LOGIC ADVANTAGES

Field-programmable logic offers many advantages to the system designer who presently is using several standard catalog SSI and MSI functions. Listed below are just a few of the benefits which are achievable when using programmable logic.

1. Package Count Reduction: typically, 3 to 6 MSI/SSI functions can be replaced with one PAL or FPLA.
2. PC Board Area Reduced: Fewer devices consume less PC board space. This results in lower PC board cost.
3. Circuit Flexibility: Programmability allows for minor circuit changes without changing PC boards.
4. Improved Reliability: With fewer PC interconnects, overall system reliability increases.
5. Shorter Design Cycle: When compared with standard-cell or gate-array approaches, custom functions can be implemented much more quickly.

The PAL and FPLA, will fill the gap between standard logic and large scale integration. The versatility of these devices provide a very powerful tool for the system designer.

PAL AND FPLA SYMBOLOGY

In order to keep PAL and FPLA logic easy to understand and use, a special convention has been adopted. Figure 1 is the representation for a 3-input AND gate. Note that only one line is shown as the input to the AND gate. This line is commonly refered to as the product line. The inputs are shown as vertical lines, and at the intersection of these lines are the programmable fuses. An X represents an intact fuse. This makes that input, part of the product term. No X represents a blown fuse. This means that input will not be part of the product term (in Figure 1, input B is not part of the product term). A dot at the intersection of any line represents a hard wire connection.

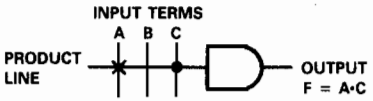

Figure 1. Basic Symbology

In Figure 2, we will extend the symbology to develop a simple 2-input programmable AND array feeding an OR gate. Notice that buffers have been added to the inputs, which provide both true and complement outputs to the product lines. The intersection of the input terms form a 4×3 programmable AND array. From the above symbology, we can see that the output of the OR gate is programmed to the following equation, $A\overline{B} + \overline{A}B$. Note that the bottom AND gate has an X marked inside the gate symbol. This means that all fuses are left intact, which results in that product line not having any effect on the sum term. In other words, the output of the AND gate will be a logic 0. **When all the fuses are blown on a product line, the output of the AND gate will always be a logic 1. This has the effect of locking up the output of the OR gate to a logic level 1.**

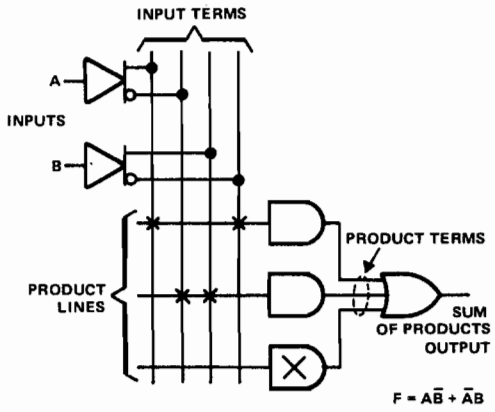

Figure 2. Basic Symbology Example

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FAMILY ARCHITECTURES

As stated before, the PROM was the first widely used programmable logic family. Its basic architecture is an input decoder configured from AND gates, combined with a programmable OR matrix on the outputs. As shown in Figure 3, this allows every output to be programmed individually from every possible input combination. In this example, a PROM with 4 inputs has 2^4, or 16 possible input combinations. With the output word width being 4 bits, each of the 16×4 bit words can be programmed individually. Applications such as data storage tables, character generators, and code converters, are just a few design examples which are ideally suited for the PROM. In general, any application which requires every input combination to be programmable, is a good candidate for a PROM. However, PROMs have difficulty accommodating large numbers of input variables. Eventually, the size of the fuse matrix will become prohibitive because for each input variable added, the size of the fuse matrix doubles. Currently, manufacturers are not producing PROMs with over 13 inputs.

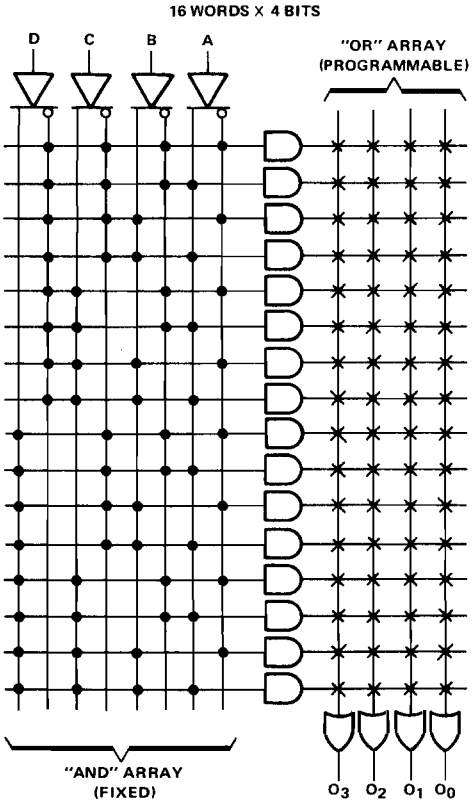


Figure 3. PROM Architecture

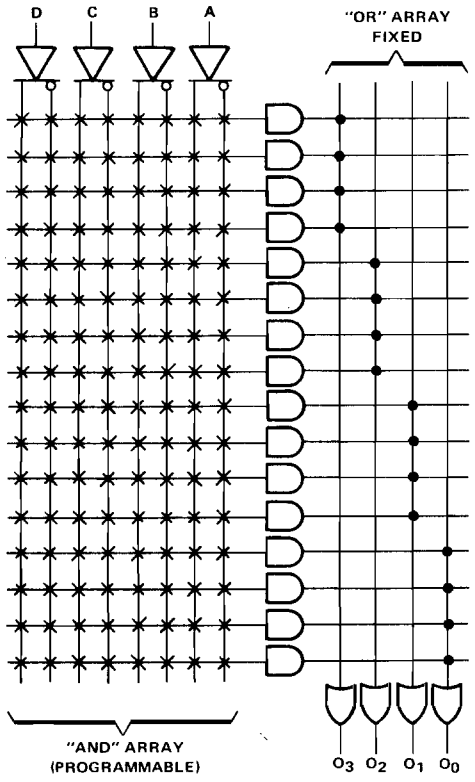


Figure 4. PAL Architecture

To overcome the limitation of a restricted number of inputs, the PAL utilizes a slightly different architecture as shown in Figure 4. The same AND-OR implementation is used as with PROMs, but now the input AND array is programmable instead of the output OR array. This has the effect of restricting the output OR array to a fixed number of input AND terms. The trade-off is that now, every output is not programmable from every input combination, but more inputs can be added without doubling the size of the fuse matrix. For example, If we were to expand the inputs on the PAL shown in Figure 4, to 10, and on the PROM in Figure 3, to 10, We would see that the fuse matrix required for the PAL would be 20×16 (320 fuses) vs 4×1024 (4096 fuses for the PROM). **It is important to realize that not every application requires every output be programmable from every input combination. This is what makes the PAL a viable product family.**

The FPLA goes one step further in offering both a programmable AND array, and a programmable OR array (Figure 5). This feature makes the FPLA the most versatile device of the three, but usually impractical in most low complexity applications.

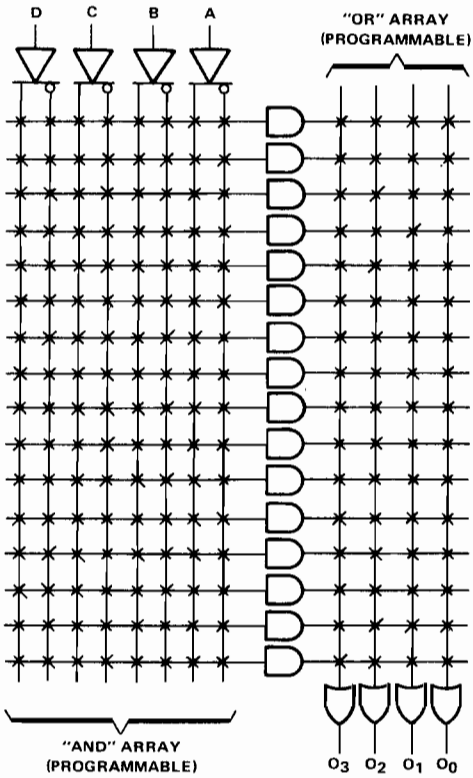


Figure 5. FPLA Architecture

All three field-programmable logic approaches discussed have their own unique advantages and limitations. The best choice depends on the complexity of the function being implemented and the current cost of the devices themselves. It is important to realize, that a circuit solution may exist from more than one of these logic families.

PAL OPTIONS

Figure 6 shows the logic diagram of the popular TIBPAL16L8. Its basic architecture is the same as discussed in the previous section, but with the addition of some special circuit features. First notice that the PAL has 10 simple inputs. In addition, 6 of the outputs operate as I/O ports. This allows feedback into the AND array. One AND gate in each product term controls each 3-state output. The architecture used in this PAL makes it very useful in generating all sorts of combinational logic.

Another important feature about the logic diagram, and all other block diagrams supplied from individual datasheets, are that there are no X's marked at every fuse location. From the previous convention, we stated that everywhere there was a intact fuse, there was an X. However, in order to make the logic diagram useful when generating specific functions, it is supplied with no X's. This allows the user to insert the X's wherever an intact fuse is desired.

The basic concept of the TIBPAL16L8 can be expanded further to include D-type flip-flops on the outputs. An example of this is shown in Figure 7 with the TIBPAL16R8. This added feature allows the device to be configured as a counter, simple storage register, or similar clocked function.

Circuit variations which are available on other members of the TI PAL and FPLA family are explained below.

Polarity Fuse

The polarity of the output can be selected via the fuse shown in Figure 8.

Input Registers

On PALs equipped with this special feature, the option of having D-type input registers is fuse programmable. Figure 9 shows an example of this type of input. If the fuse is left intact, data enters on a low-high transition of the clock. If the fuse is blown, the register becomes permanently transparent and is equivalent to a normal input buffer.

Input Latches

On PALs equipped with this special feature, the option of having input latches is fuse programmable.

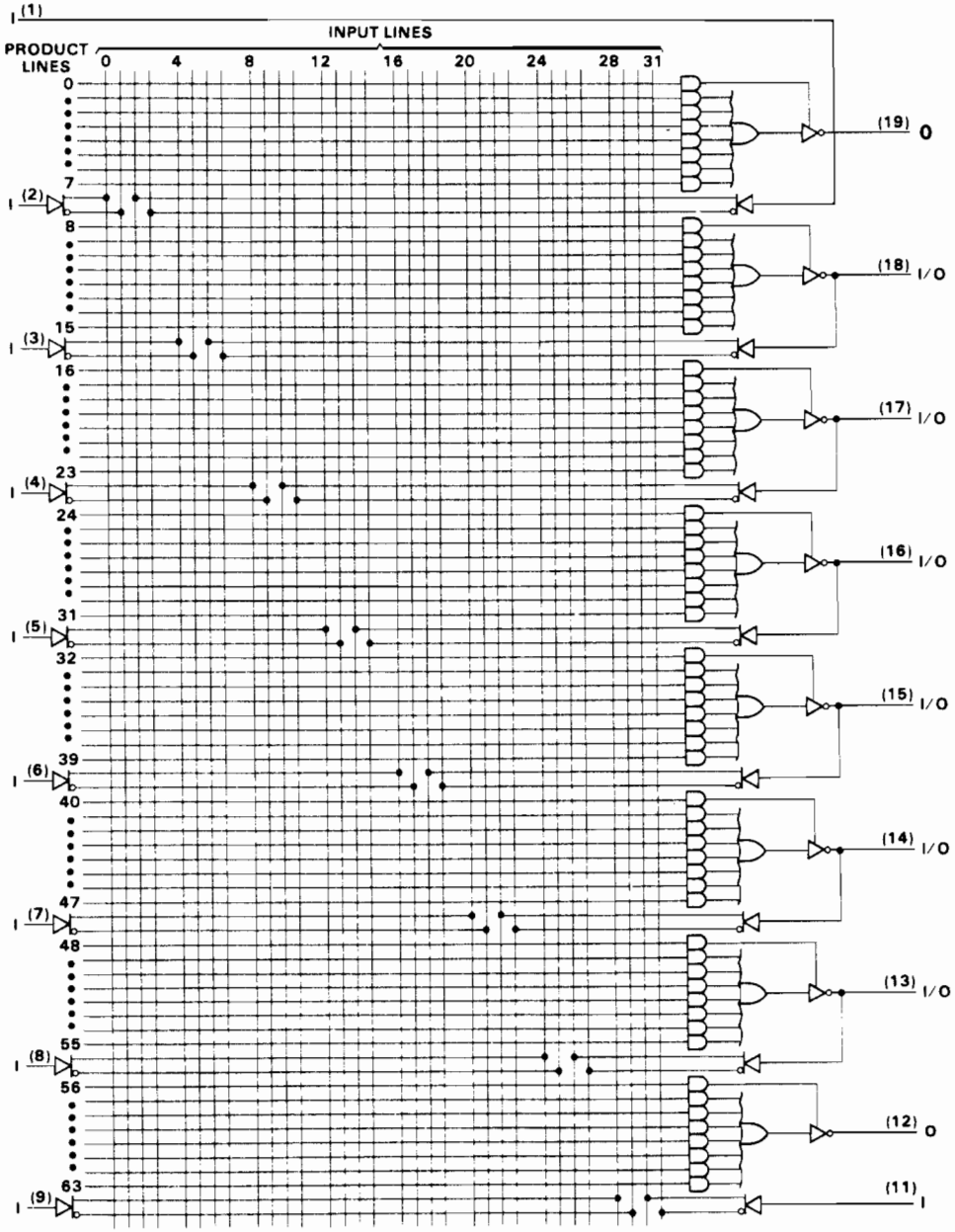


Figure 6. TIBPAL16L8 Logic Diagram

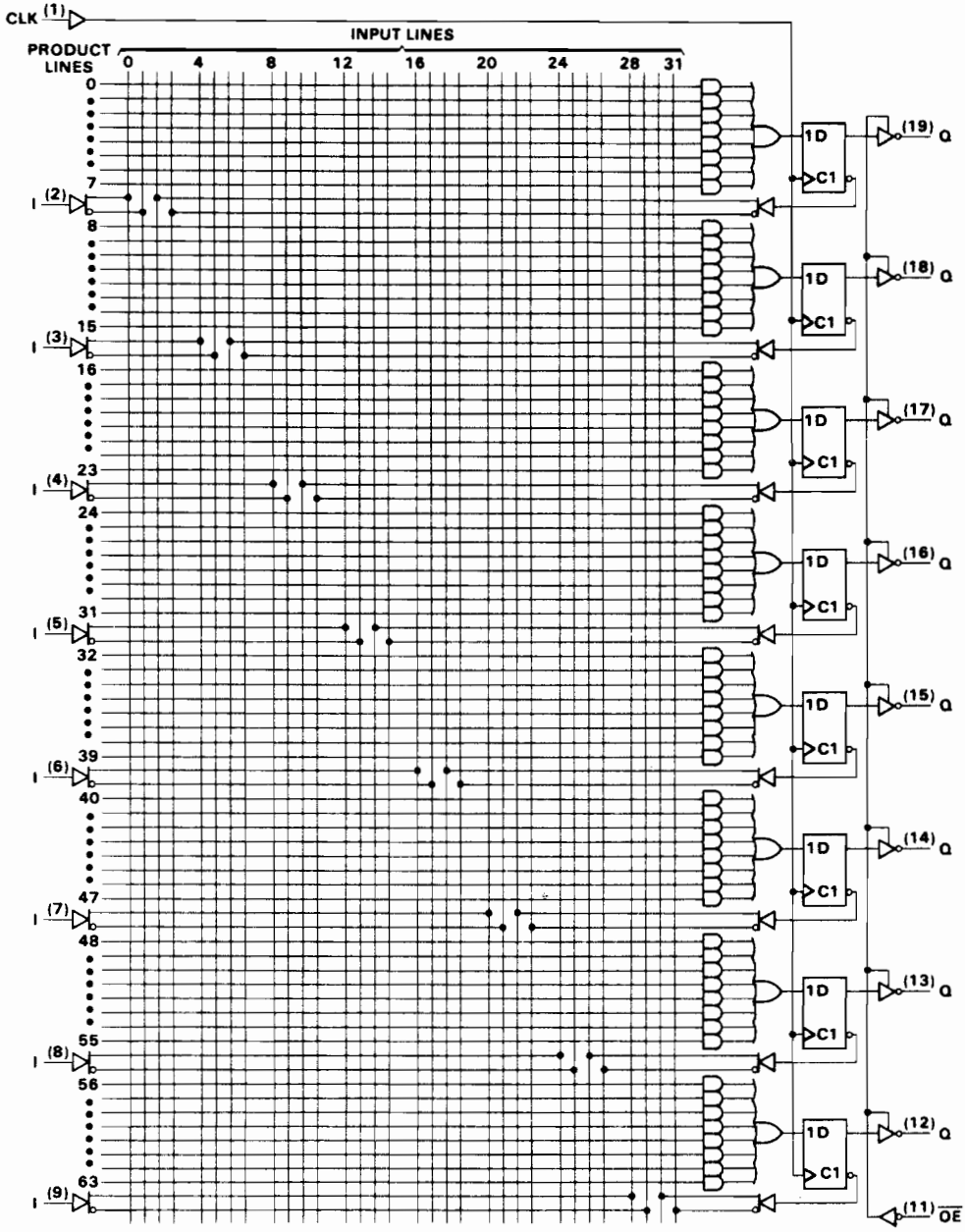
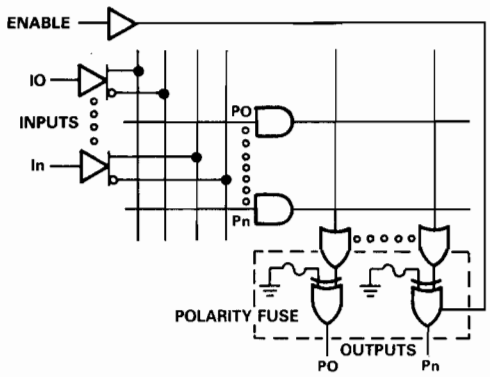


Figure 7. TIBPAL16R8 Logic Diagram



INTACT: OUTPUT = $\overline{P0} + \overline{P1} + ... + \overline{Pn}$
BLOWN: OUTPUT = $\overline{P0} \cdot \overline{P1} \cdot ... \cdot \overline{Pn}$

Figure 8. Polarity Selection

Figure 10 shows an example of this type of input. If the fuse is left intact, data enters while the control input is high. When the control input is low, the data that was present when the control input went low will be saved. If the fuse is blown, the latch becomes permanently transparent, and is equivalent to a normal input buffer.

PROGRAMMING

Notice in Figure 7, that the product and input lines are numbered. This allows any specific fuse to be located anywhere in the fuse matrix. When the device is in the programming mode (as defined in the device data sheet), the individual product and input lines can be selected. The fuse at the intersection of these lines, can then be blown (programmed) with the defined programming pulse. Fortunately, the user seldom has to get involved with these actual details of programming, because there exist several commercially available programmers which handle this function. Listed below are some of the manufacturers of this programming equipment.*

Citel	Storey Systems
DATA I/O	Structured Design
Digelec	Sunrise Electronics
Kontron	Valley Data Science
Wavetec	Varix
Stag Micro Systems	

At Texas Instruments, we have coordinated with DATA I/O using their Model 19 for device characterization. Currently, DATA I/O, Sunrise, and Structured Design have been certified by Texas Instruments. Other programmers are now in the certification process. For a current list of certified programmers, please contact your local TI sales representative.

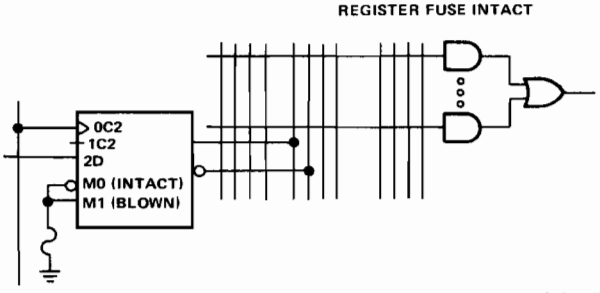
It should now be obvious to the reader, that the actual blowing of the fuses is not a problem. Instead, the real question is what fuses need to be blown to generate a particular function. Fortunately, this problem has also been greatly simplified by recent advances in computer software.

DATA I/O has developed a software package called ABEL™. Also available is CUPL™, from Assisted Technology. Both have been designed to be compatible with several different types of programmers. Both of these software packages greatly extend the capabilities of the original PALASM™ program, and both can be run on most professional computers.

Before proceeding to a design example, it would be instructive to look at the simplified process flow of a PAL (Figure 11). This should help give the reader a better understanding of the basic steps necessary to generate a working device.

DESIGN EXAMPLE

The easiest way to demonstrate the unique capabilities of the PAL is through a design example. It is



D-TYPE REGISTER FUNCTION TABLE

CLOCK	D	Q	$\overline{Q}$
↑	H	H	L
↑	L	L	H
L	X	Q_0	$\overline{Q}_o$

Q_O = THE STATE OF Q BEFORE CLOCK ↑

Figure 9. Input Register Selection

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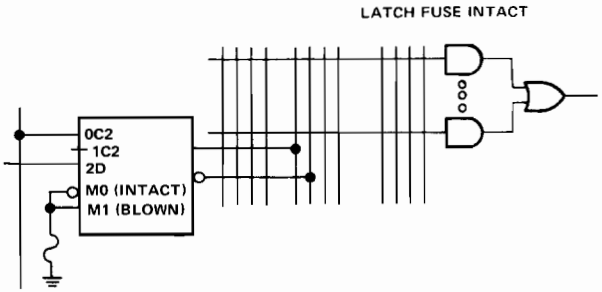
PALASM™ is a trademark of Monolithic Memories Inc.



TRANSPARENT LATCH FUNCTION TABLE

ENABLE	D	O	$\overline{O}$
H	L	L	H
H	H	H	L
L	X	Q_0	$\overline{Q}_0$

Q_0 = THE LEVEL OF Q BEFORE ENABLE ↓

Figure 10. Input Latch Selection

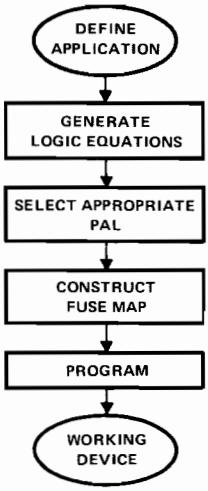


Figure 11. PAL Process Flow Diagram

hoped that through this example the reader will gain the basic understanding needed when applying the PAL in his own application. In some cases, this goal may only be to reduce existing logic, but the overall approach will be the same.

EXAMPLE REQUIREMENTS

It is desired to generate a 4-bit binary counter which is fed by one of four clocks. There are two lines available for selecting the clocks, SEL1 and SEL0. Table 1 shows the required input for the selection of the clocks. In addition, it is desired that the counter be able to switch from binary to decade count. This feature is controlled by an input called BD. When BD is high, the counter should count in binary. When low, the counter should count in decade.

Figure 12 shows how this example could be implemented if standard data book functions were used.

Table 1. Clock Selection

SEL1	SEL0	OUTPUT
0	0	CLKA
0	1	CLKB
1	0	CLKC
1	1	CLKD

As can be seen, three MSI functions are required. The 'LS162 is used to generate the 4-bit counter while the clock selection is handled by the 'LS253. The 'LS688 is an 8-bit comparator which is used for selecting either the binary or decade count. In this example, only five of the eight comparator inputs are used. Four are used for comparing the counter outputs, while the other is used for the BD input. The comparator is hard-wired to go low whenever the BD input is low and the counter output is "9". The $\overline{P=Q}$ output is then fed back to the synchronous clear input on the 'LS162. This will reset the counter to zero whenever this condition occurs.

PAL IMPLEMENTATION

As stated before, the problem in programming a PAL is not in blowing the fuses, but rather what fuses need to be blown to generate a particular function. Fortunately, this problem has been greatly simplified by computer software, but before we examine these techniques, it is beneficial to explore the methods used in generating the logic equations. This will help develop an understanding, and appreciation for these advanced software packages.

From digital logic theory, we know that most any type of logic can be implemented in either AND-OR-INVERT or AND-NOR form. This is the basic concept used in the PAL and FPLA. This allows classical techniques, such as Karnaugh Maps[1] to be used in generating specific logic functions. As with the separate component example above, it is easier to break it into separate functions. The first one that we will look at is the clock selector, but remember that the overall goal will be to reduce this design example into one PAL.

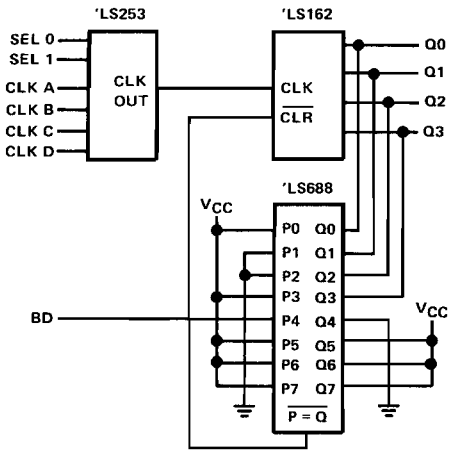


Figure 12. Counter Implementation With Standard Logic

PAL SELECTION

Before proceeding with the design for the clock selector, the first question which needs to be addressed is which PAL to use. As discussed earlier, there are several different types of output architectures. Looking at our example, we can see that four flip-flops with feedback will be required in the 4-bit counter, plus input clock and clear lines. In addition, seven inputs plus two simple outputs will be required in the clock selector and comparator. With this information in hand, we can see that the TIBPAL16R4 (Figure 13) will handle our application.

CLOCK SELECTOR DETAILS

The first step in determining the logic equation for the clock selector is to generate a function table with all the possible input combinations. This is shown in Table 2. From this table, the Karnaugh map can be generated and is shown in Figure 14. The minimized equation for CLKOUT comes directly from this.

Table 2. Function Table

SEL1	SEL0	CLKA	CLKB	CLKC	CLKD	CLKOUT	SEL1	SEL0	CLKA	CLKB	CLKC	CLKD	CLKOUT
0	0	0	0	0	0	0	1	0	0	0	0	0	0
0	0	0	0	0	1	0	1	0	0	0	0	1	0
0	0	0	0	1	0	0	1	0	0	0	1	0	1
0	0	0	0	1	1	0	1	0	0	0	1	1	1
0	0	0	1	0	0	0	1	0	0	1	0	0	0
0	0	0	1	0	1	0	1	0	0	1	0	1	0
0	0	0	1	1	0	0	1	0	0	1	1	0	1
0	0	0	1	1	1	0	1	0	0	1	1	1	1
0	0	1	0	0	0	1	1	0	1	0	0	0	0
0	0	1	0	0	1	1	1	0	1	0	0	1	0
0	0	1	0	1	0	1	1	0	1	0	1	0	1
0	0	1	0	1	1	1	1	0	1	0	1	1	1
0	0	1	1	0	0	1	1	0	1	1	0	0	0
0	0	1	1	0	1	1	1	0	1	1	0	1	0
0	0	1	1	1	0	1	1	0	1	1	1	0	1
0	0	1	1	1	1	1	1	0	1	1	1	1	1
0	1	0	0	0	0	0	1	1	0	0	0	0	0
0	1	0	0	0	1	0	1	1	0	0	0	1	1
0	1	0	0	1	0	0	1	1	0	0	1	0	0
0	1	0	0	1	1	0	1	1	0	0	1	1	1
0	1	0	1	0	0	1	1	1	0	1	0	0	0
0	1	0	1	0	1	1	1	1	0	1	0	1	1
0	1	0	1	1	0	1	1	1	0	1	1	0	0
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0	1	1	0	0	0	0	1	1	1	0	0	0	0
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0	1	1	0	1	0	0	1	1	1	0	1	0	0
0	1	1	0	1	1	0	1	1	1	0	1	1	1
0	1	1	1	0	0	1	1	1	1	1	0	0	0
0	1	1	1	0	1	1	1	1	1	1	0	1	1
0	1	1	1	1	0	1	1	1	1	1	1	0	0
0	1	1	1	1	1	1	1	1	1	1	1	1	1

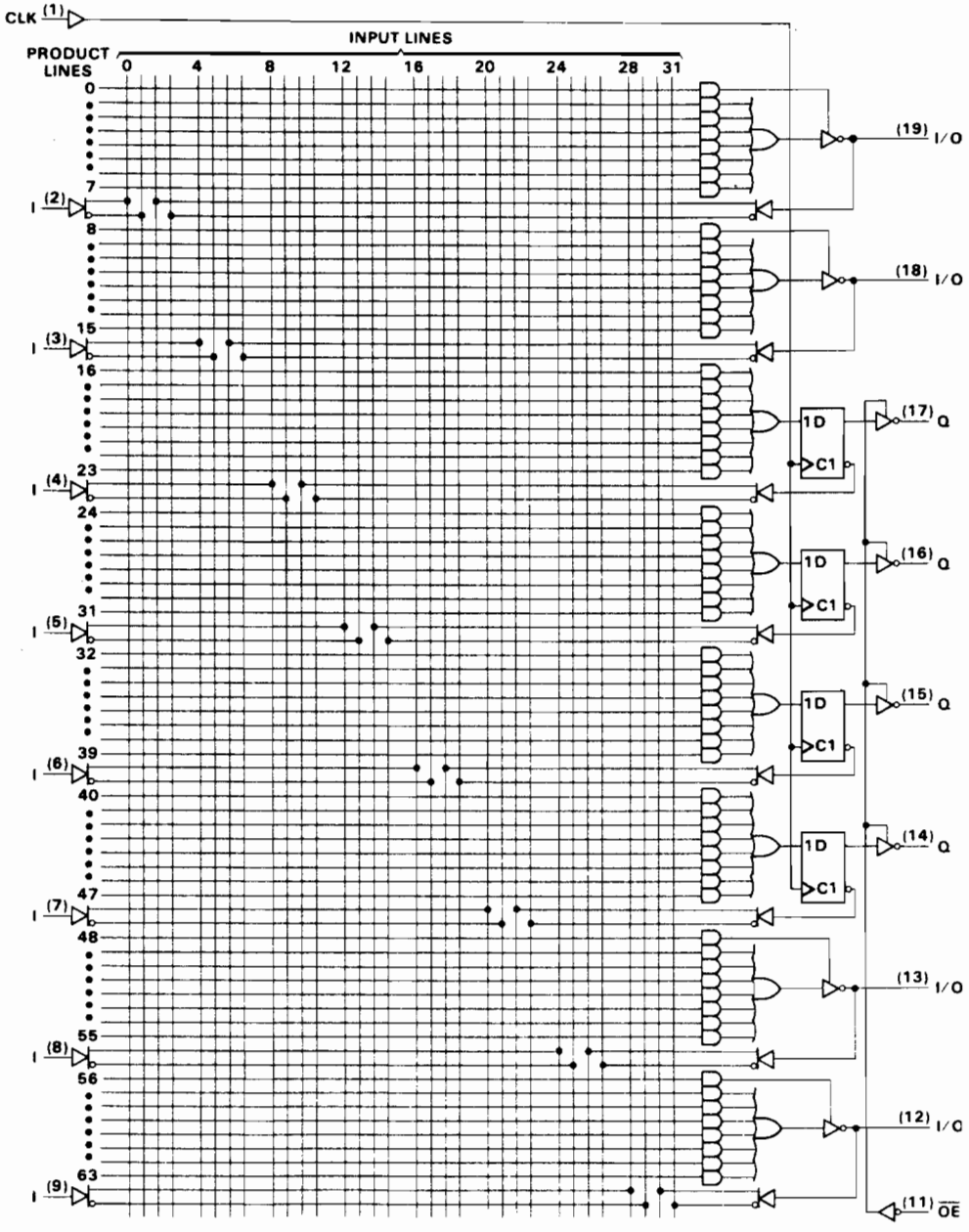
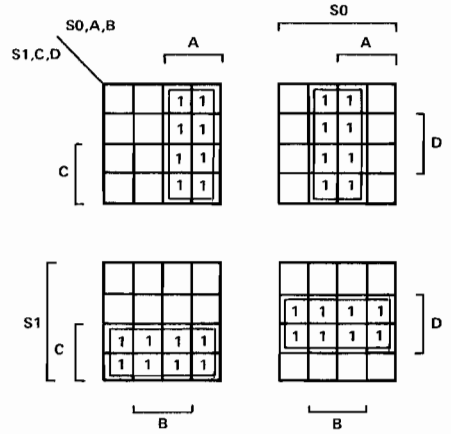


Figure 13. TIBPAL16R4 Logic Diagram

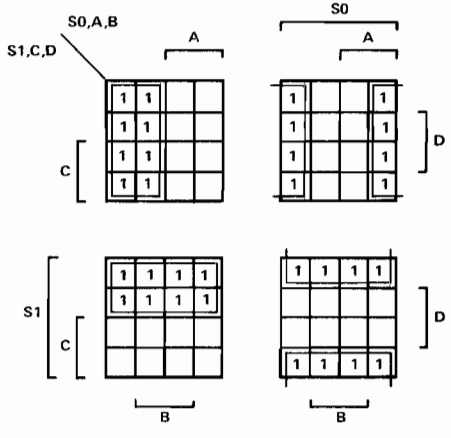
It is important to notice that the equation derived from the Karnaugh map is stated in AND-OR notation. The PAL that we have selected is implemented in AND-NOR logic. This means we either have to do DeMorgan's theorem on the equation, or solve the inverse of the Karnaugh map. Figure 15 shows the inverse of the Karnaugh map and the resulting equation. This equation can be easily implemented in the TIBPAL16R4.



$CLKOUT = \overline{S1}\,\overline{S0}A + \overline{S1}S0B + S1\overline{S0}C + S1S0D$

$CLKOUT = \overline{S1}\,\overline{S0}A + \overline{S1}S0B + S1\overline{S0}C + S1S0D$

Figure 14. Karnaugh Map for CLKOUT



$\overline{CLKOUT} = \overline{S1}\,\overline{S0}A + \overline{S1}S0B + S1\overline{S0}C + S1S0D$

$\overline{CLKOUT} = \overline{S1}\,\overline{S0}A + \overline{S1}S0B + S1\overline{S0}C + S1S0D$

Figure 15. Karnaugh Map for $\overline{CLKOUT}$

4-BIT BINARY COUNTER DETAILS

The same basic procedure used in determining the equations for the clock selector, is used in determining the equations for the 4-bit counter. The only difference is that now we are dealing with a present state, next state situation. This means a D-type flip-flop will be required in actual circuit implementation. As before, the truth table is generated first, and is shown in Table 3.

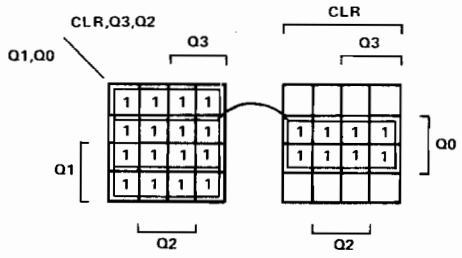
Table 3. Truth Table

	PRESENT STATE				NEXT STATE			
CLR	Q3	Q2	Q1	Q0	Q3	Q2	Q1	Q0
0	X	X	X	X	0	0	0	0
1	0	0	0	0	0	0	0	1
1	0	0	0	1	0	0	1	0
1	0	0	1	0	0	0	1	1
1	0	0	1	1	0	1	0	0
1	0	1	0	0	0	1	0	1
1	0	1	0	1	0	1	1	0
1	0	1	1	0	0	1	1	1
1	0	1	1	1	1	0	0	0
1	1	0	0	0	1	0	0	1
1	1	0	0	1	1	0	1	0
1	1	0	1	0	1	0	1	1
1	1	0	1	1	1	1	0	0
1	1	1	0	0	1	1	0	1
1	1	1	0	1	1	1	1	0
1	1	1	1	0	1	1	1	1
1	1	1	1	1	0	0	0	0

From the truth table, the equations for each output can be derived from the Karnaugh map. This is shown in Figure 16. Note that the inverse of the truth table is being solved so that the equation will come out in AND-NOR logic form.

BINARY/DECADE COUNT DETAILS

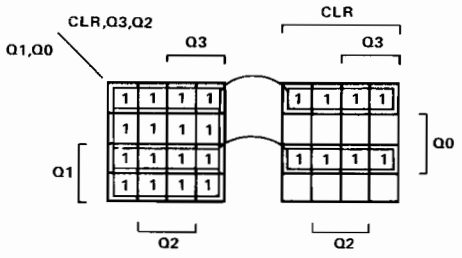
Recalling from the example requirements that the counter should count in decade whenever the BD input is low, we can again generate a truth table for this function (Table 4). Since the counter is already designed to count in binary, we can use this feature to simplify our design. What we desire is a circuit whose output goes low, whenever the BD input is equal to a logic level "0", and the counter output is equal to "9". This output can then be fed back to the CLR input of the counter so that it will reset whenever the BD input is low. Whenever the BD input is high, the output of the circuit should be a high since the counter will automatically count in binary. Notice that $\overline{Q}$ shown in the truth table is the function we desire.



$\overline{Q0} = \overline{CLR}\overline{Q3}\overline{Q2}\overline{Q1}\overline{Q0} + \overline{CLR}Q3\overline{Q2}\overline{Q1}\overline{Q0}$

$\overline{Q0} = \overline{CLR} + Q0$

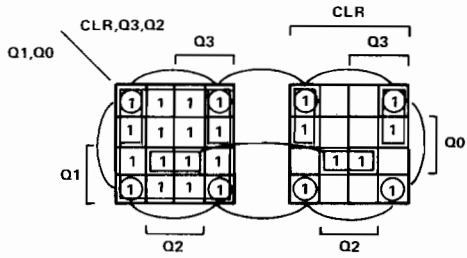
(a) KARNAUGH MAP FOR $\overline{Q0}$



$\overline{Q1} = \overline{CLR}\overline{Q3}\overline{Q2}\overline{Q1}\overline{Q0} + \overline{CLR}\overline{Q3}Q2\overline{Q1}\overline{Q0} + \overline{CLR}Q3\overline{Q2}Q1\overline{Q0}$

$\overline{Q1} = \overline{CLR} + \overline{Q1}\overline{Q0} + Q1Q0$

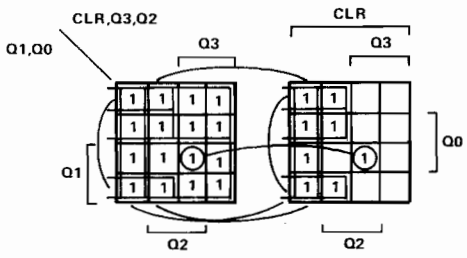
(b) KARNAUGH MAP FOR $\overline{Q1}$



$\overline{Q2} = \overline{CLR}\overline{Q3}\overline{Q2}\overline{Q1}\overline{Q0} + \overline{CLR}\overline{Q3}\overline{Q2}Q1\overline{Q0} + \overline{CLR}Q3\overline{Q2}Q1Q0 + \overline{CLR}\overline{Q3}Q2\overline{Q1}\overline{Q0}$

$\overline{Q2} = \overline{CLR} + \overline{Q2}\overline{Q1} + Q2Q1Q0 + \overline{Q2}\overline{Q0}$

(c) KARNAUGH MAP FOR $\overline{Q2}$



$\overline{Q3} = \overline{CLR}\overline{Q3}\overline{Q2}\overline{Q1}\overline{Q0} + \overline{CLR}\overline{Q3}\overline{Q2}Q1\overline{Q0} + \overline{CLR}\overline{Q3}Q2\overline{Q1}\overline{Q0} + \overline{CLR}Q3\overline{Q2}\overline{Q1}\overline{Q0} + \overline{CLR}Q3Q2Q1Q0$

$\overline{Q3} = \overline{CLR} + \overline{Q3}\overline{Q2} + \overline{Q3}\overline{Q1} + \overline{Q3}\overline{Q0} + Q3Q2Q1Q0$

(d) KARNAUGH MAP FOR $\overline{Q3}$

Figure 16. Karnaugh Maps

In this particular example, a Karnaugh map is not required because the equation cannot be further simplified. The resulting equation is given below.

$$\overline{BD\ OUT} = \overline{BD}Q3\overline{Q2}\overline{Q1}Q0$$

Table 4. Truth Table

BD	Q3	Q2	Q1	Q0	Q	$\overline{Q}$	BD	Q3	Q2	Q1	Q0	Q	$\overline{Q}$
0	0	0	0	0	0	1	1	0	0	0	0	0	1
0	0	0	0	1	0	1	1	0	0	0	1	0	1
0	0	0	1	0	0	1	1	0	0	1	0	0	1
0	0	0	1	1	0	1	1	0	0	1	1	0	1
0	0	1	0	0	0	1	1	0	1	0	0	0	1
0	0	1	0	1	0	1	1	0	1	0	1	0	1
0	0	1	1	0	0	1	1	0	1	1	0	0	1
0	0	1	1	1	0	1	1	0	1	1	1	0	1
0	1	0	0	0	0	1	1	1	0	0	0	0	1
0	1	0	0	1	1	0	1	1	0	0	1	0	1
0	1	0	1	0	0	1	1	1	0	1	0	0	1
0	1	0	1	1	0	1	1	1	0	1	1	0	1
0	1	1	0	0	0	1	1	1	1	0	0	0	1
0	1	1	0	1	0	1	1	1	1	0	1	0	1
0	1	1	1	0	0	1	1	1	1	1	0	0	1
0	1	1	1	1	0	1	1	1	1	1	1	0	1

FUSE MAP DETAILS

Now that the logic equations have been defined, the next step will be to specify which fuses need to be blown. Before we do this however, we first need to label the input and output pins on the TIBPAL16R4. By using Figure 12 as a guide, we can make the following pin assignments in Figure 17.

PIN

1 CLK	20 VCC
2 SEL0	19 CLKOUT
3 SEL1	18 NC
4 CLKA	17 Q0
5 CLKB	16 Q1
6 CLKC	15 Q2
7 CLKD	14 Q3
8 CLR	13 NC
9 BD	12 BD OUT
10 GND	11 OE

With this information defined, we now need to insert the logic equations into the logic diagram as shown in Figure 17.

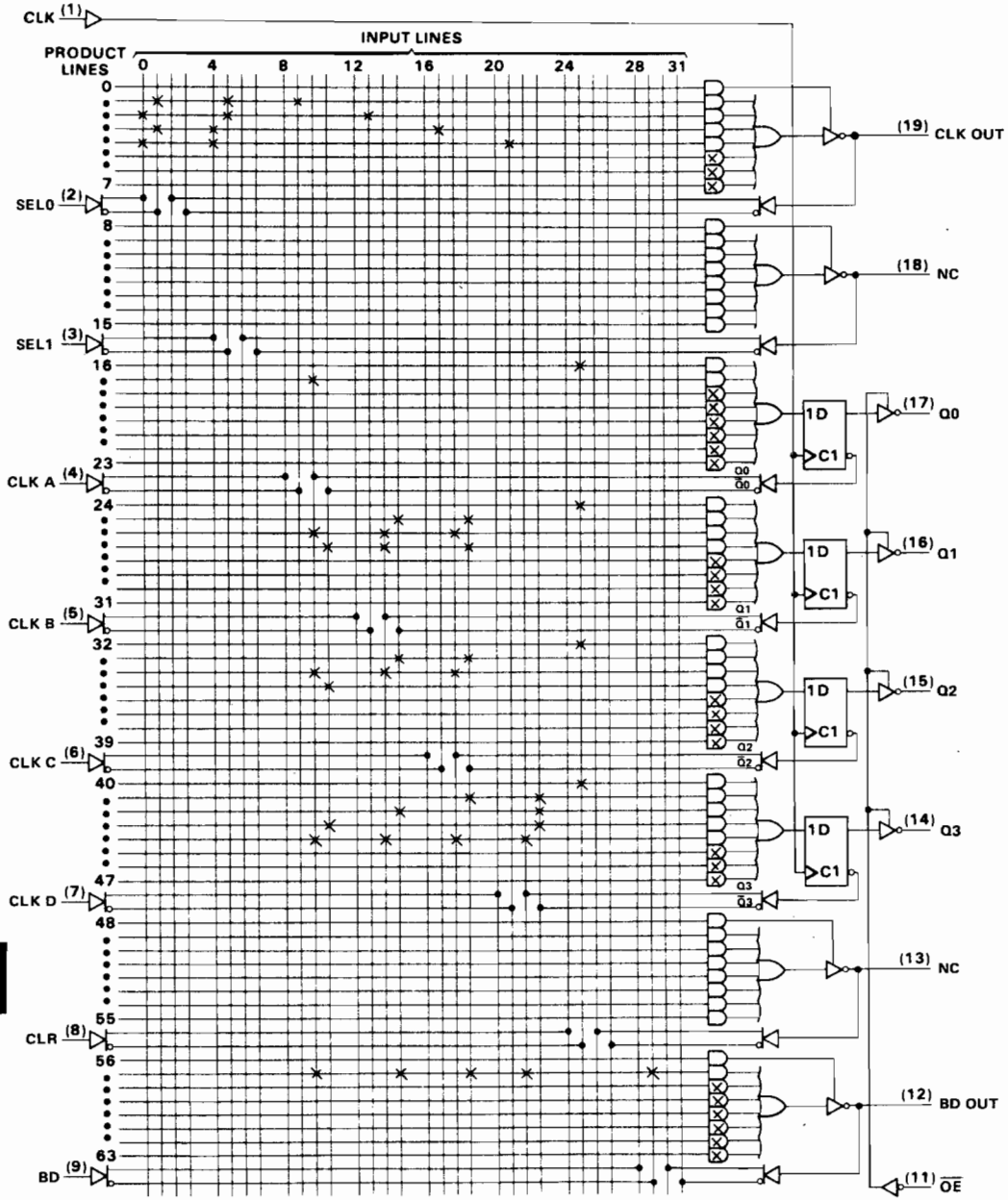


Figure 17. Programmed TIBPAL16R4

It is now probably obvious to the reader, that inserting the logic equations into the logic diagram is a tedious operation. Fortunately, a computer program called PALASM will perform this task automatically. All that is required is telling the program which device has been selected, and defining the input and output pins with their appropriate logic equations (Figure 18). The program will then generate a fuse map (Figure 19) for the device selected. Notice that the fuse map looks very similar to the block diagram (Figure 17) which we have just completed by hand. In addition, this information can now be down loaded into the selected device programmer.

```
DEVICE TYPE 16R4


PIN LIST NAMES =
PIN NUMBER =  1     PIN NAME = CLK
PIN NUMBER =  2     PIN NAME = SEL0
PIN NUMBER =  3     PIN NAME = SEL1
PIN NUMBER =  4     PIN NAME = CLKA
PIN NUMBER =  5     PIN NAME = CLKB
PIN NUMBER =  6     PIN NAME = CLKC
PIN NUMBER =  7     PIN NAME = CLKD
PIN NUMBER =  8     PIN NAME = CLR
PIN NUMBER =  9     PIN NAME = BD
PIN NUMBER = 10     PIN NAME = GND
PIN NUMBER = 11     PIN NAME = /OE
PIN NUMBER = 12     PIN NAME = BDOUT
PIN NUMBER = 13     PIN NAME = NC
PIN NUMBER = 14     PIN NAME = Q3
PIN NUMBER = 15     PIN NAME = Q2
PIN NUMBER = 16     PIN NAME = Q1
PIN NUMBER = 17     PIN NAME = Q0
PIN NUMBER = 18     PIN NAME = NC
PIN NUMBER = 19     PIN NAME = CLKOUT
PIN NUMBER = 20     PIN NAME = VCC


EXPRESSIONS  AND DESCRIPTION =
EXPRESSION[ 1] =
/CLKOUT=/SEL1*/SEL0*/CLKA +/SEL1*SEL0*/CLKB +SEL1*/SEL0*/CLKC +SEL1*SEL0*/CLKD


EXPRESSION[ 2] =
/Q0=/CLR +Q0


EXPRESSION[ 3] =
/Q1=/CLR +/Q1*/Q0 +Q1*Q0


EXPRESSION[ 4] =
/Q2=/CLR +/Q2*/Q1 +Q2*Q1*Q0 +/Q2*/Q0


EXPRESSION[ 5] =
/Q3=/CLR +/Q3*/Q2 +/Q3*/Q1 +/Q3*/Q0 +Q3*Q2*Q1*Q0


EXPRESSION[ 6] =
/BDOUT=/BD*Q3*/Q2*/Q1*Q0
```

Figure 18. Pin ID and Logic Equations

```
0000 0000 0011 1111 1111 2222 2222 2233
0123 4567 8901 2345 6789 0123 4567 8901
/CLKOUT   =
---- ---- ---- ---- ---- ---- ---- ----   0 -
-X-- -X-- -X-- ---- ---- ---- ---- ----   1 - /SEL1*/SEL0*/CLKA+
X--- -X-- ---- -X-- ---- ---- ---- ----   2 - /SEL1*SEL0*/CLKB+
-X-- X--- ---- ---- -X-- ---- ---- ----   3 - SEL1*/SEL0*/CLKC+
X--- X--- ---- ---- ---- -X-- ---- ----   4 - SEL1*SEL0*/CLKD
XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX   5 -
XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX   6 -
XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX   7 -
        =
XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX   8 -
XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX   9 -
XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX  10 -
XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX  11 -
XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX  12 -
XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX  13 -
XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX  14 -
XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX  15 -
/00       =
---- ---- ---- ---- ---- ---- -X-- ----  16 - /CLR+
---- ---- --X- ---- ---- ---- ---- ----  17 - 00
XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX  18 -
XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX  19 -
XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX  20 -
XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX  21 -
XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX  22 -
XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX  23 -
/01       =
---- ---- ---- ---- ---- ---- -X-- ----  24 - /CLR+
---- ---- ---X ---X ---- ---- ---- ----  25 - /01*/00+
---- ---- --X- --X- ---- ---- ---- ----  26 - 01*00
XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX  27 -
XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX  28 -
XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX  29 -
XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX  30 -
XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX  31 -
/02       =
---- ---- ---- ---- ---- ---- -X-- ----  32 - /CLR+
---- ---- ---- ---X ---X ---- ---- ----  33 - /02*/01+
---- ---- --X- --X- --X- ---- ---- ----  34 - 02*01*00+
---- ---- ---X ---- ---X ---- ---- ----  35 - /02*/00
XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX  36 -
XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX  37 -
XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX  38 -
XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX  39 -
/03       =
---- ---- ---- ---- ---- ---- -X-- ----  40 - /CLR+
---- ---- ---- ---- ---X ---X ---- ----  41 - /03*/02+
---- ---- ---- ---X ---- ---X ---- ----  42 - /03*/01+
---- ---- ---X ---- ---- ---X ---- ----  43 - /03*/00+
---- ---- --X- --X- --X- --X- ---- ----  44 - 03*02*01*00
XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX  45 -
XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX  46 -
XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX  47 -
        =
XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX  48 -
XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX  49 -
XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX  50 -
XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX  51 -
XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX  52 -
XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX  53 -
XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX  54 -
XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX  55 -
/BDOUT    =
---- ---- ---- ---- ---- ---- ---- ----  56 -
---- ---- --X- ---X ---X --X- ---- -X--  57 - /BD*03*/02*/01*00
XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX  58 -
XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX  59 -
XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX  60 -
XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX  61 -
XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX  62 -
XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX  63 -
```

Figure 19. Fuse Map

ADVANCED SOFTWARE

PALASM, while extremely useful in generating the fuse map, does little to help formulate the logic equations. This is what the new software packages such as ABEL and CUPL address. They not only generate the fuse map, but they also help in developing the logic equations. In most cases, they can generate the logic equations from simply providing the program with either a truth table or state diagram. In addition, they can test the logic equations against a set of test vectors. This helps ensure the designer gets the desired function.

These are only a few of the features available on these new advanced software packages. We recommend that the reader contact the specific manufacturers themselves to obtain the latest information available. For your convenience, at the end of this application note we have included the addresses and phone numbers for many of these programming and software companies.

As an example, we will approach our previous design utilizing DATA I/O's ABEL package. The purpose here is not to teach the reader how to use ABEL, but rather to give them a basic overview of this powerful software package. Figure 20 shows the source file required by ABEL. Note that the 4-bit counter has been described with a state diagram table. When the ABEL program is complied, the logic equations will be generated from this. The equations for CLK OUT and BD OUT have been given in their final form to demonstrate how ABEL would handle these. Also notice that test vectors are included for checking the logic equations. This is especially important when only the logic equations has been given.

Figure 21 shows some of the output documentation generated by the program. Notice that the equations generated for the counter, match the the ones generated by the Karnaugh maps. A pinout for the device has also been generated and displayed. The fuse map for the device has not been shown, but looks very similar to the one in Figure 19. As with the PALASM program, this information can be down loaded into the device programmer.

PERFORMANCE

Up to this point, nothing has been said about the performance of these devices. The Standard High Speed PAL (indicated by an "A" after the device number) offered by TI has a maximum propagation of 25 ns from input to output, and 35 MHz f_{max}. Also available is a new, higher speed family of devices called TIBPALs. These devices are functionally equivalent with the current family and offer a maximum propagation delay of 15 ns from input to output. They are also rated at 50 MHz f_{max}. The higher speeds on these devices make them compatible with most high-speed logic families. This allows them to be designed into more critical speed path applications.

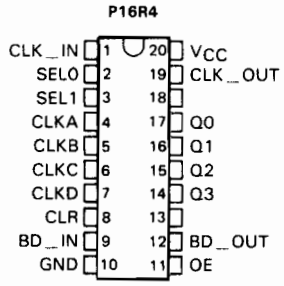
```
module BD_COUNT flag '-r2'
title '4-bit binary/decade counter

      IC1  device 'P16R4';

"  pin assignments and constant declarations
      CLK_IN SEL0 SEL1 CLKA      pin  1,2,3,4;
      CLKB,CLKC,CLKD             pin  5,6,7;
      CLR,BD_IN,OE               pin  8,9,11;
      BD_OUT,CLK_OUT             pin  12,19;
      Q3,Q2,Q1,Q0                pin  14,15,16,17;
      CK, L, H, X, Z  =          .C.  , 0 , 1 , .X. , .Z.;
      OUTPUT          =          [Q3,Q2,Q1,Q0];

"  counter states
      S0=^b0000;    S4=^b0100;    S8=^b1000;    S12=^b1100;
      S1=^b0001;    S5=^b0101;    S9=^b1001;    S13=^b1101;
      S2=^b0010;    S6=^b0110;   S10=^b1010;    S14=^b1110;
      S3=^b0011;    S7=^b0111;   S11=^b1011;    S15=^b1111;

equations
"  clock selector
      CLK_OUT = CLKA & !SEL0 & !SEL1 # CLKB & !SEL1 & SEL0
                # CLKC & SEL1 & !SEL0 # CLKD & SEL1 & SEL0;

"  count nine indicator for decade counting
      BD_OUT  = !(!BD_IN & Q3 & !Q2 & !Q1 & Q0);

state_diagram [Q3,Q2,Q1,Q0]
      State  S0:  IF CLR == 0 THEN S0 ELSE  S1;
      State  S1:  IF CLR == 0 THEN S0 ELSE  S2;
      State  S2:  IF CLR == 0 THEN S0 ELSE  S3;
      State  S3:  IF CLR == 0 THEN S0 ELSE  S4;
      State  S4:  IF CLR == 0 THEN S0 ELSE  S5;
      State  S5:  IF CLR == 0 THEN S0 ELSE  S6;
      State  S6:  IF CLR == 0 THEN S0 ELSE  S7;
      State  S7:  IF CLR == 0 THEN S0 ELSE  S8;
      State  S8:  IF CLR == 0 THEN S0 ELSE  S9;
      State  S9:  IF CLR == 0 THEN S0 ELSE S10;
      State S10:  IF CLR == 0 THEN S0 ELSE S11;
      State S11:  IF CLR == 0 THEN S0 ELSE S12;
      State S12:  IF CLR == 0 THEN S0 ELSE S13;
      State S13:  IF CLR == 0 THEN S0 ELSE S14;
      State S14:  IF CLR == 0 THEN S0 ELSE S15;
      State S15:  IF CLR == 0 THEN S0 ELSE  S0;

test_vectors   'clock selector'
     ([CLKA, CLKB, CLKC, CLKD, SEL1, SEL0] -> CLK_OUT)
      [ L  ,  X  ,  X  ,  X  ,  L  ,  L  ] ->  L;
      [ H  ,  X  ,  X  ,  X  ,  L  ,  L  ] ->  H;
      [ X  ,  L  ,  X  ,  X  ,  L  ,  H  ] ->  L;
      [ X  ,  H  ,  X  ,  X  ,  L  ,  H  ] ->  H;
      [ X  ,  X  ,  L  ,  X  ,  H  ,  L  ] ->  L;
      [ X  ,  X  ,  H  ,  X  ,  H  ,  L  ] ->  H;
      [ X  ,  X  ,  X  ,  L  ,  H  ,  H  ] ->  L;
      [ X  ,  X  ,  X  ,  H  ,  H  ,  H  ] ->  H;

test_vectors   'counter'
     ([CLK_IN, OE, CLR, BD_IN] -> [OUTPUT, BD_OUT])
      [  CK,   L ,  L ,    X  ] -> [  S0,  H ];
      [  CK,   L ,  H,     X  ] -> [  S1,  H ];
      [  CK,   L ,  H ,    X  ] -> [  S2,  H ];
      [  CK,   L ,  H,     X  ] -> [  S3,  H ];
      [  CK,   L ,  H ,    X  ] -> [  S4,  H ];
      [  CK,   L ,  H,     X  ] -> [  S5,  H ];
      [  CK,   L ,  H,     X  ] -> [  S6,  H ];
      [  CK,   L ,  H,     X  ] -> [  S7,  H ];
      [  CK,   L ,  H,     X  ] -> [  S8,  H ];
      [  CK,   L ,  H,     L  ] -> [  S9,  L ];
      [  CK,   L ,  H,     X  ] -> [ S10,  H ];
      [  CK,   L ,  H,     X  ] -> [ S11,  H ];
      [  CK,   L ,  H,     X  ] -> [ S12,  H ];
      [  CK,   L ,  H,     X  ] -> [ S13,  H ];
      [  CK,   L ,  H,     X  ] -> [ S14,  H ];
      [  CK,   L ,  H,     H  ] -> [ S15,  H ];
      [  CK,   L ,  H,     X  ] -> [  S0,  H ];
      [   X,   H ,  X,     X  ] -> [   Z ,  H ];
end BD_COUNT
```

Figure 20. Source File for ABEL

```
ABEL(tm) Version  1.00  - Document Generator
4-bit binary/decade counter

Equations for Module BD_COUNT

Device IC1


     Reduced Equations:

       CLK_OUT = !((SEL1 & SEL0 & !CLKD
                  # (SEL1 & !SEL0 & !CLKC
                  # (!SEL1 & SEL0 & !CLKB
                  # !SEL1 & !SEL0 & !CLKA)));


       BD_OUT = !(Q3 & !Q2 & !Q1 & Q0 & !BD_IN);

       Q3 := !((Q3 & Q2 & Q1 & Q0
              # (!Q3 & !Q2
              # (!Q3 & !Q1
              # (!Q3 & !Q0
              # !CLR)))));


       Q2 := !((Q2 & Q1 & Q0 # (!Q2 & !Q1 # (!Q2 & !Q0 # !CLR))));

       Q1 := !((Q1 & Q0 # (!Q1 & !Q0 # !CLR)));

       Q0 := !((Q0 # !CLR));
```



```
ABEL(tm) Version  1.00  - Document Generator
4-bit binary/decade counter

Chip diagram for Module BD_COUNT

Device IC1
```




```
end of module BD_COUNT
```

Figure 21. ABEL Output Documentation

ADDRESS FOR PROGRAMMING AND SOFTWARE MANUFACTURERS*

HARDWARE MANUFACTURERS

Citel
3060 Raymond St.
Santa Clara, CA 95050
(408) 727-6562

DATA I/O
10525 Willows Rd.
Redmond, WA 98052
(206) 881-6444

DIGITAL MEDIA
3178 Gibralter Ave.
Costa Mesa, CA 92626
(714) 751-1373

Kontron Electronics
630 Price Avenue
Redwood City, CA 94063
(415) 361-1012

Stag Micro Systems
528-5 Weddell Drive
Sunnyvale, CA 94086
(408) 745-1991

Storey Systems
3201 N. Hwy 67, Suite H
Mesquite, Tx 75150
(214) 270-4135

Structured Design
1700 Wyatt Dr., Suite 7
Santa Clara, CA 95054
(408) 988-0725

Sunrise Electronics
524 S. Vermont Avenue
Glendora, CA 91740
(213) 914-1926

Valley Data Sciences
2426 Charleston Rd.
Mountain View, CA 94043
(415) 968-2900

Varix
1210 Campbell Rd.
Richardson, TX 75081
(214) 437-0777

Wavetec/Digelec
586 Weddel Dr., Suite 1
Sunnyvale, CA 94089
(408) 745-0722

SOFTWARE MANUFACTURERS

Assisted Technologies (CUPL)
2381 Zanker Road, Suite 150
Santa Clara, CA 95050
(408) 942-8787

DATA I/O (ABEL)
10525 Willows Rd.
Redmond, WA 98052
(206) 881-6444

*Texas Instruments does not endorse or warrant the suppliers referenced.

Reference

1. H. Troy Nagle, Jr., B.D. Carroll, and David Irwin. *An Introduction to Computer Logic*. New Jersey: Prentice-Hall, Inc., 1975.

General Information 1

Functional Index 2

Field-Programmable Logic 3

PROMs 4

RAMs and Memory-Based Code Converters 5

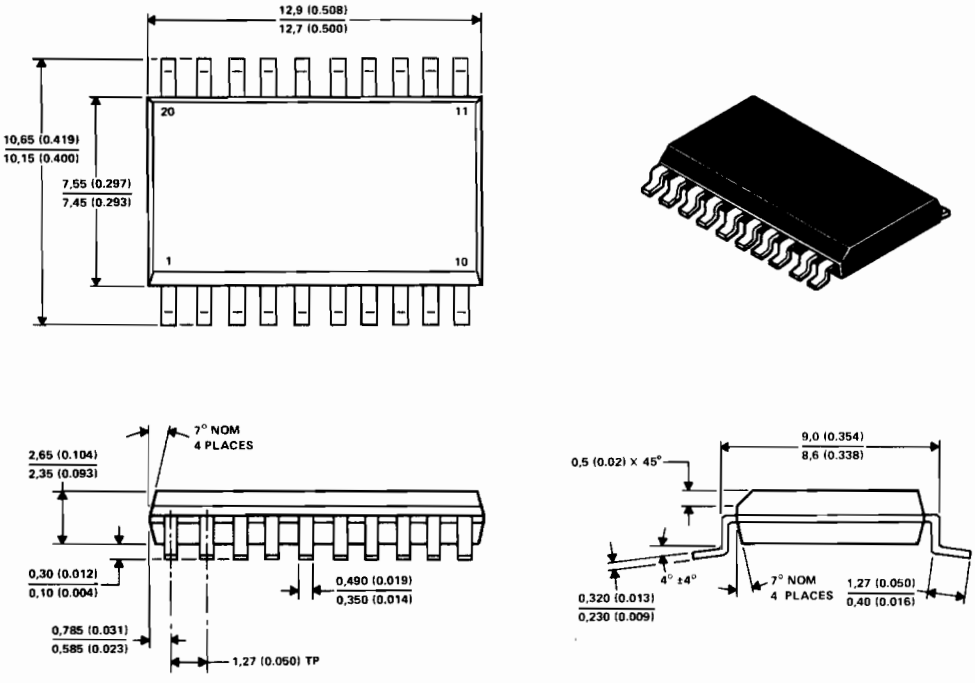
Designing with Texas Instruments Field-Programmable Logic 6

Mechanical Data 7

DW plastic dual-in-line packages

Each of these dual-in-line packages consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

20 PIN PACKAGE
(TENTATIVE SPECIFICATIONS)

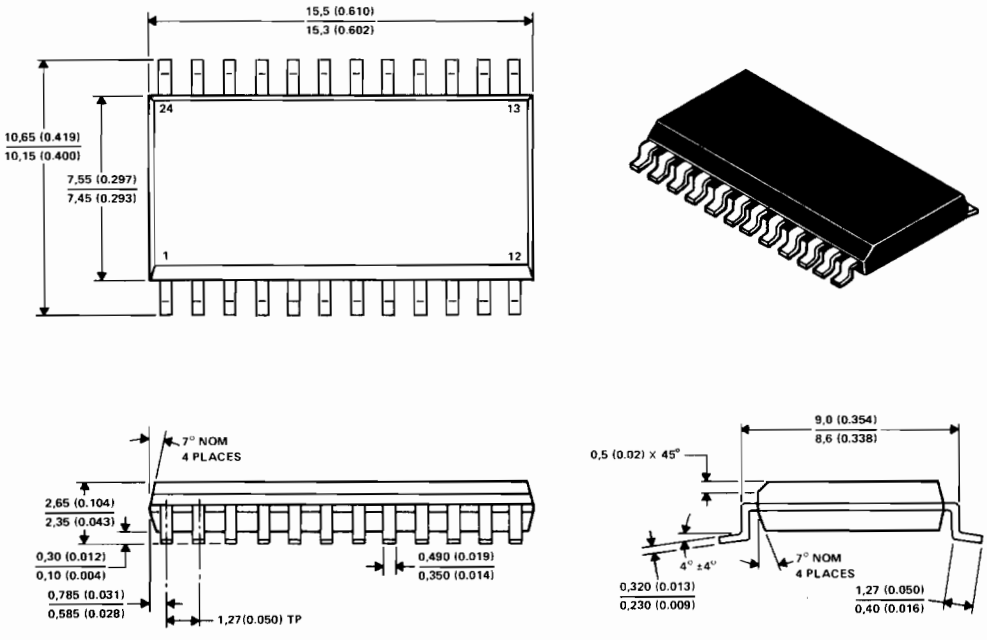


ALL LINEAR DIMENSIONS IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Body dimensions do not include mold flash or protrusion.
B. Mold flash or protrusion shall not exceed 0,15 (0.006).
C. Leads are within 0,25 (0.010) radius of true position at maximum material dimension.

DW plastic dual-in-line packages (continued)

24 PIN PACKAGE
(TENTATIVE SPECIFICATIONS)



ALL LINEAR DIMENSIONS IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Body dimensions do not include mold flash or protrusion.
B. Mold flash or protrusion shall not exceed 0,15 (0.006).
C. Leads are within 0,25 (0.010) radius of true position at maximum material dimension.

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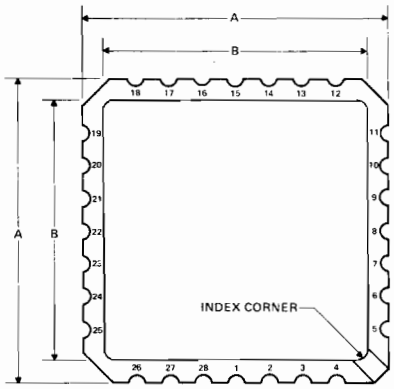
FK ceramic chip carrier packages

Each of these hermetically sealed chip carrier packages has a three-layer ceramic base with a metal lid and braze seal. The packages are intended for surface mounting on solder lands on 1,27 (0.050-inch) centers. Terminals require no additional cleaning or processing when used in soldered assembly.

FK package terminal assignments conform to JEDEC Standards 1 and 2.

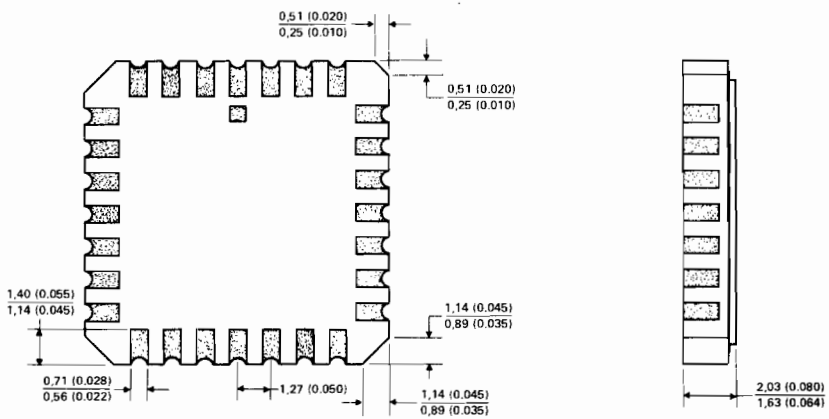
FK CERAMIC CHIP CARRIER PACKAGES
(28-terminal package shown)



CERAMIC CHIP CARRIERS

JEDEC OUTLINE DESIGNATION*	NO. OF TERMINALS	A MIN	A MAX	B MIN	B MAX
MS004CB	20	8,69 (0.342)	9,09 (0.358)	7,80 (0.307)	9,09 (0.358)
MS004CC	28	11,23 (0.442)	11,63 (0.458)	10,31 (0.406)	11,63 (0.458)
MS004CD	44	16,26 (0.640)	16,76 (0.660)	12,58 (0.495)	14,22 (0.560)
MS004CE	52	18,78 (0.739)	19,32 (0.761)	12,58 (0.495)	14,22 (0.560)
MS004CF	68	23,83 (0.938)	24,43 (0.962)	12,6 (0.495)	21,8 (0.862)
MS004CG	84	28,83 (1.135)	29,59 (1.165)	12,6 (0.495)	27,0 (1.065)

*All dimensions and notes for the specified JEDEC outline apply



ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

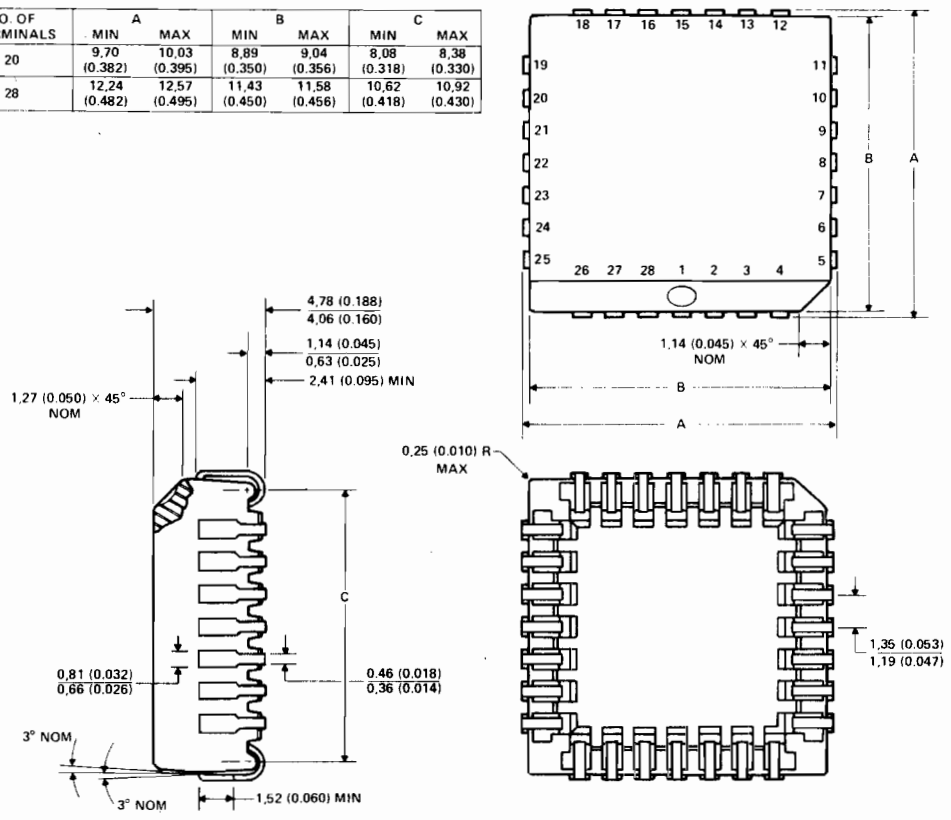
FN plastic chip carrier package

Each of these chip carrier packages consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound withstands soldering temperatures with no deformation, and circuit performance characteristics remain stable when the devices are operated in high-humidity conditions. The packages are intended for surface mounting on solder lands on 1,27 (0.050) centers. Leads require no additional cleaning or processing when used in soldered assembly.

FN PLASTIC CHIP CARRIER PACKAGE

(28-terminal package shown)

NO. OF TERMINALS	A		B		C	
	MIN	MAX	MIN	MAX	MIN	MAX
20	9,70 (0.382)	10,03 (0.395)	8,89 (0.350)	9,04 (0.356)	8,08 (0.318)	8,38 (0.330)
28	12,24 (0.482)	12,57 (0.495)	11,43 (0.450)	11,58 (0.456)	10,62 (0.418)	10,92 (0.430)



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

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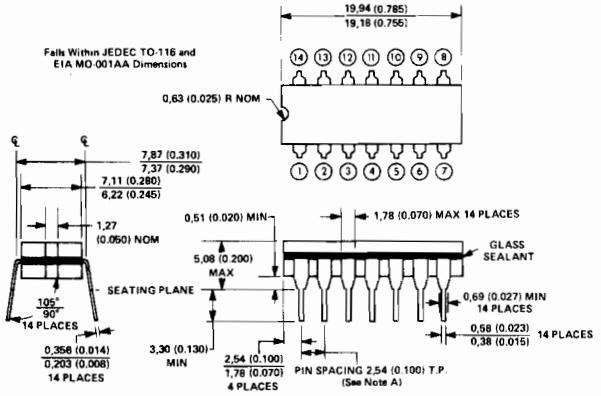
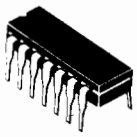
J ceramic packages (including JT and JW dual-in-line and JQ quad-in-line packages)

Each of these hermetically sealed dual-in-line packages consists of a ceramic base, ceramic cap, and a lead frame. Hermetic sealing is accomplished with glass. The JT packages are intended for insertion in mounting-hole rows on 7,62 (0.300) centers, JW packages for mounting-hole rows on 15,24 (0.600) centers, and the JQ quad-in-line package for mounting-hole rows on 15,24 (0.600) and 20,32 (0.800) centers. Once the leads are compressed and inserted sufficient tension is provided to secure the package in the board during soldering. Tin-plated ("bright-dipped") leads require no additional cleaning or processing when used in soldered assembly.

NOTE: For the 14-, 16-, 18-, and 20-pin packages, the letter J is used by itself since these packages are available only in the 7,62 (0.300) row spacing. For the 24-pin packages, if no second letter or row spacing is specified, the package is assumed to have 15,24 (0.600) row spacing.

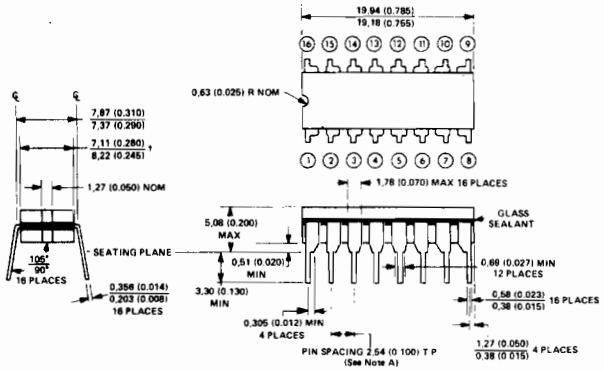
14-PIN J CERAMIC

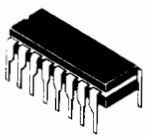




ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

16-PIN J CERAMIC





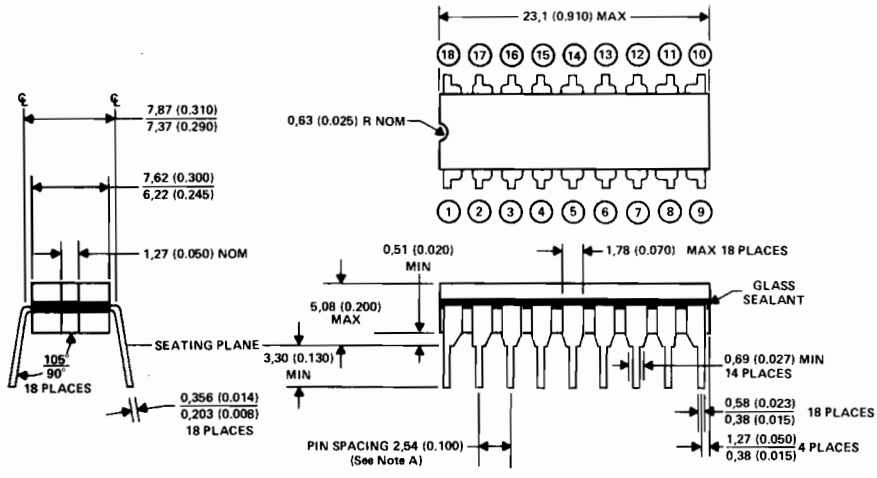
†For memories of 64 bits and up and a few MSI/LSI products in Series 54/74 and Series 54S/74S that are derived from memory circuit bars, this maximum is 7,62 (0.300). All other dimensions apply without modification.

ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

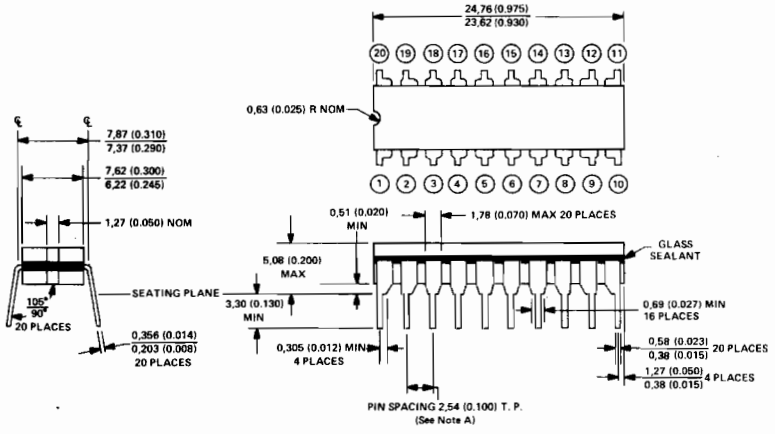
J ceramic dual-in-line packages (continued)

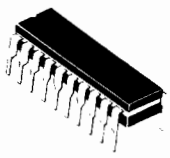
18-PIN J CERAMIC



ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

20-PIN J CERAMIC





ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

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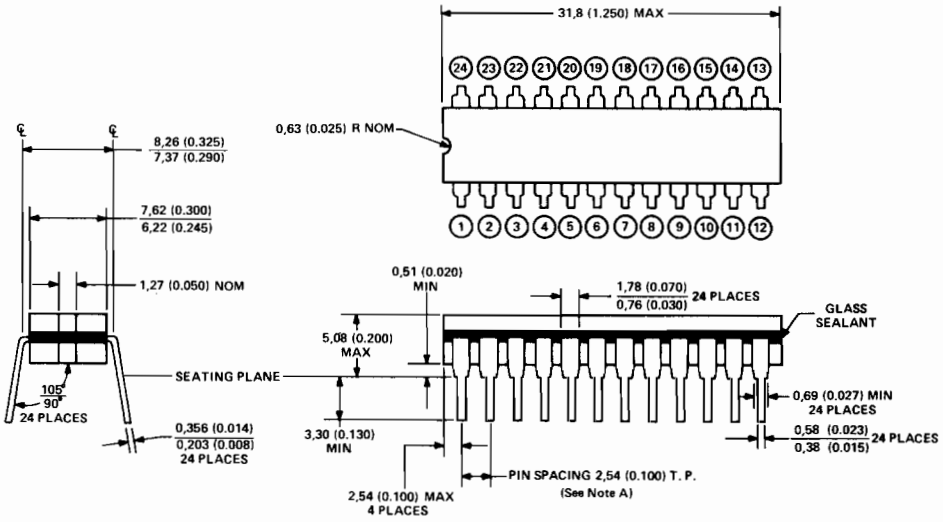
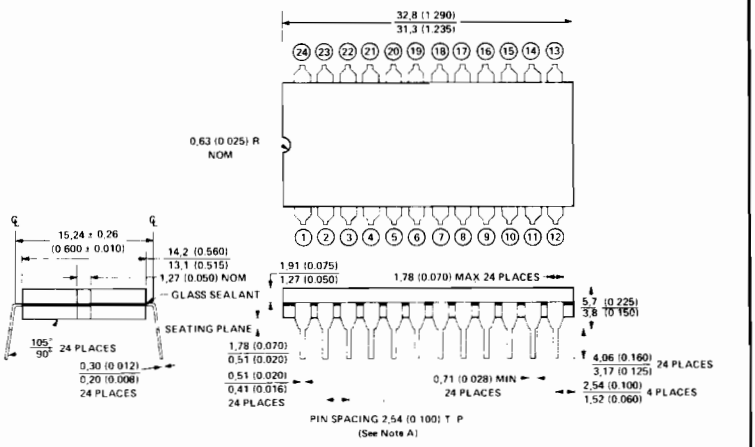
J ceramic dual-in-line packages (continued)

24-PIN JT CERAMIC, 0.300-INCH ROW SPACING



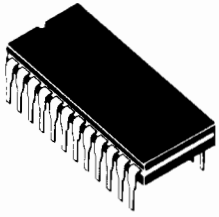
ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

24-PIN JW CERAMIC



Falls within JEDEC MO-015AA dimensions

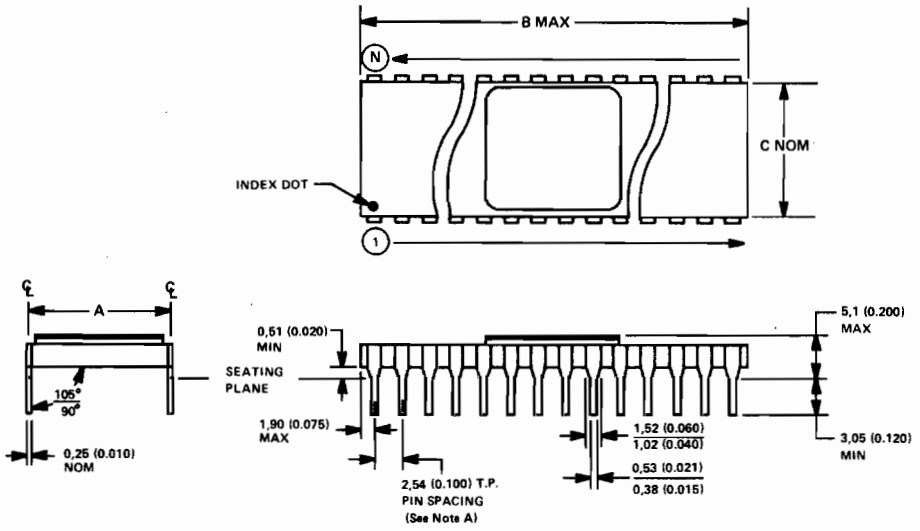
ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES



NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

ceramic packages – side-braze (JD suffix)

This is a hermetically sealed ceramic package with a metal cap and side-brazed tin-plated leads.



DIM \ PINS	24	28	40	48	52	64
A ± 0,25 (0.010)	15,24 (0.600)	15,24 (0.600)	15,24 (0.600)	15,24 (0.600)	15,24 (0.600)	22,86 (0.900)
B MAX	32,8 (1.290)	36,8 (1.450)	52,1 (2.050)	62,2 (2.450)	67,3 (2.650)	82,6 (3.250)
C NOM	15,1 (0.595)	15,1 (0.595)	15,1 (0.595)	15,1 (0.595)	15,1 (0.595)	22,6 (0.890)

ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

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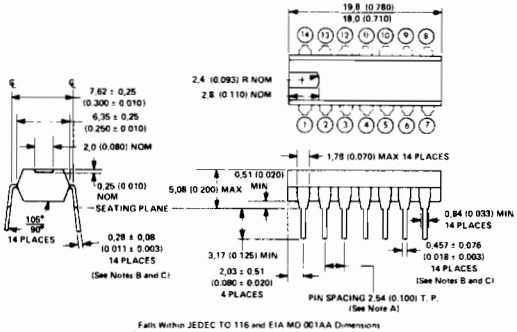
N plastic packages (including NT and NW dual-in-packages)

Each of these dual-in-line packages consists of a circuit mounted on a lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation and circuit performance characteristics remain stable when operated in high-humidity conditions. The packages are intended for insertion in mounting-hole rows on 7,62 (0.300) centers for the NT packages and on 15,24 (0.600) centers for the NW packages. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

NOTE: For the 14-, 16-, 18-, 20-, and 28-pin packages, the letter N is used by itself since these packages are available in only one row-spacing width: 7,62 (0.0300) for the 14-, 16-, 18-, and 20-pin packages or 15,24 (0.600) for the 28-pin package. For the 24-pin package, if no second letter or row spacing is specified, the package is assumed to have 15,24 (0.600) row spacing.

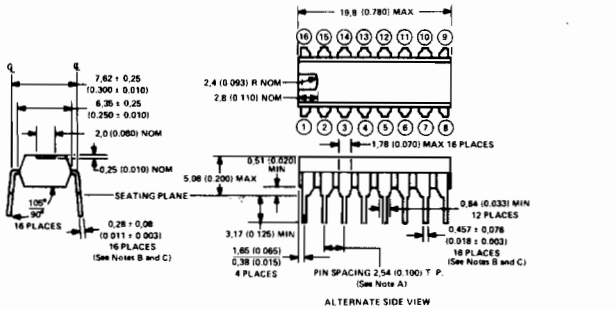
14-PIN N PLASTIC



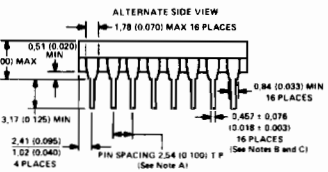
Falls Within JEDEC TO 116 and EIA MO 001AA Dimensions

ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

16-PIN N PLASTIC



ALTERNATE SIDE VIEW



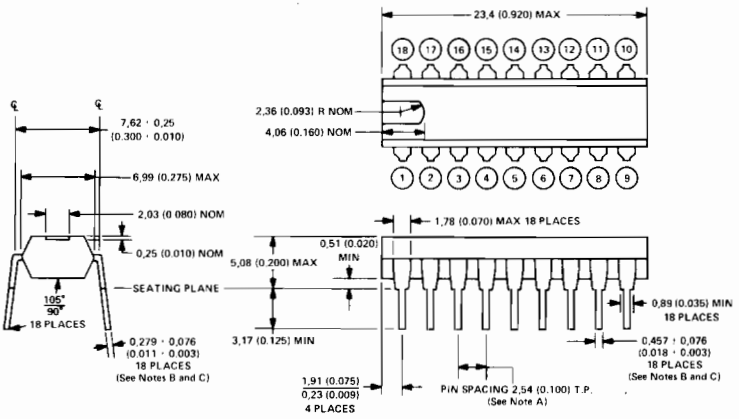
Parts may be supplied in accordance with the alternate side view at the option of TI plants located in Europe. In this case, the overall length of the package is 22,1 (0.870) max.

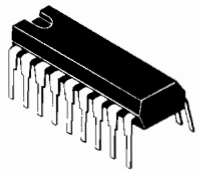
ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Each pin centerline is located with 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

N plastic dual-in-line packages (continued)

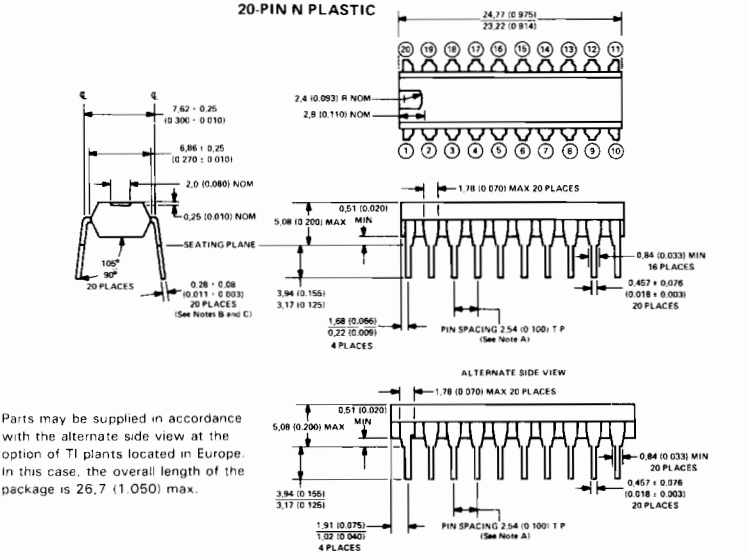
18-PIN N PLASTIC

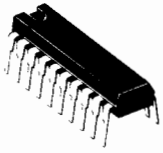




ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

20-PIN N PLASTIC





Parts may be supplied in accordance with the alternate side view at the option of TI plants located in Europe. In this case, the overall length of the package is 26,7 (1.050) max.

ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Each pin centerline is located with 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

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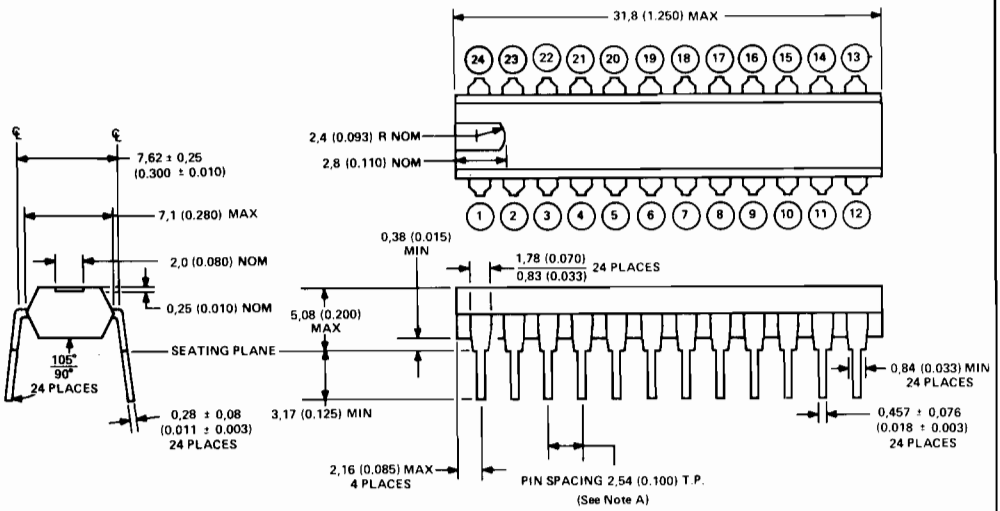
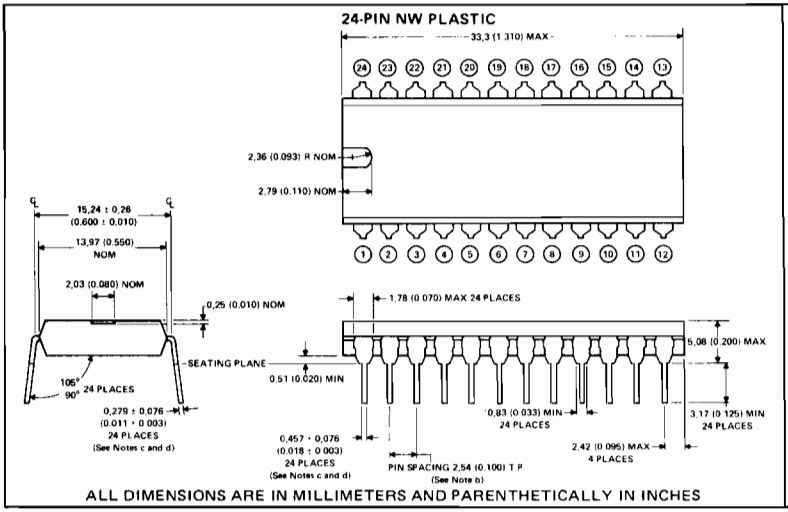
N plastic dual-in-line packages (continued)

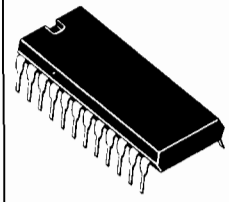
24-PIN NT PLASTIC, 0.300-INCH ROW SPACING



ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

24-PIN NW PLASTIC





ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Each pin centerline is located with 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

N plastic packages (continued)

NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

TEXAS INSTRUMENTS
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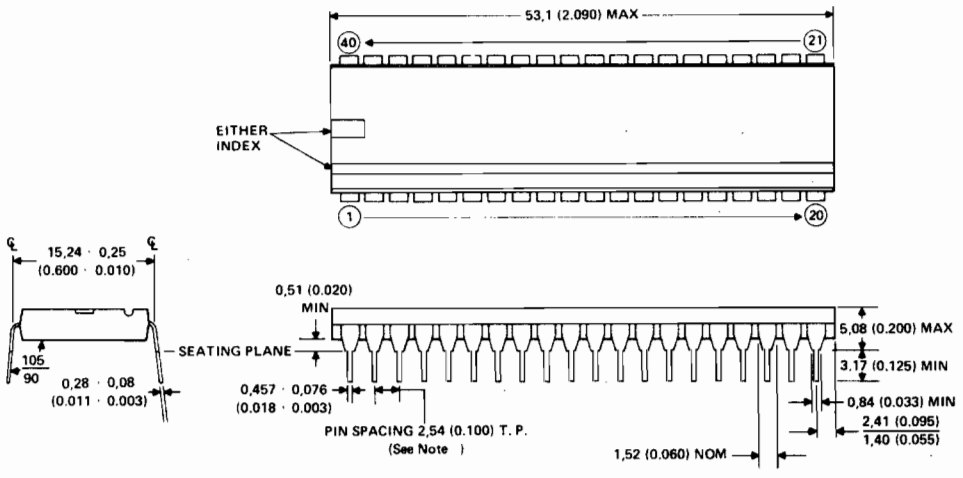
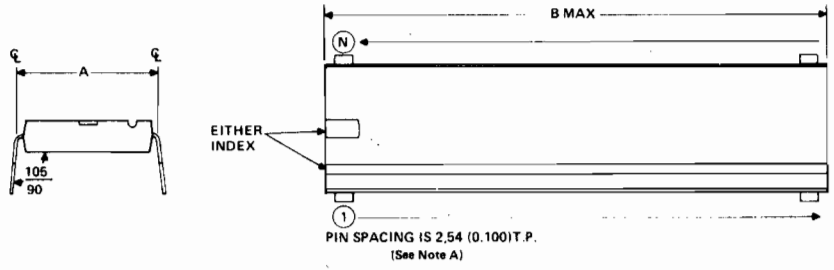
N plastic packages (continued)

40-PIN N PLASTIC



ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

48-PIN, 52-PIN, AND 64-PIN N PLASTIC



DIM \ PINS	48	52	64
A ± 0,25 (0.010)	15,24 (0.600)	15,24 (0.600)	22,86 (0.900)
B MAX	62,2 (2.45)	67,3 (2.65)	81,3 (3.20)

ALL DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

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NOTES

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