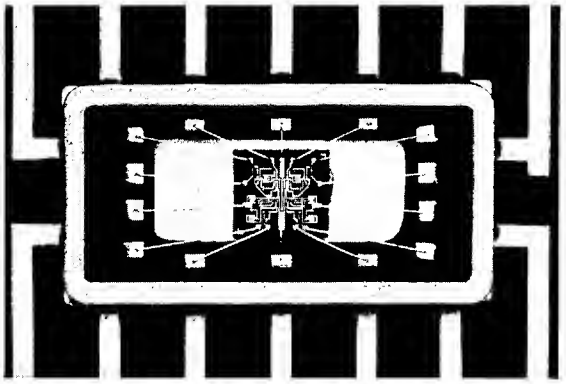
SERIES 74
BULLETIN NO. DL-S 657934, AUGUST 1965

HIGH-SPEED SATURATED DIGITAL CIRCUITS FOR GENERAL-PURPOSE INDUSTRIAL APPLICATIONS

description

Series 74 integroted circuits hove been designed and chorocterized for high-speed, generol-purpose digitol opplicotions where high d-c noise morgin and low power dissipation are importont system considerotions. Definitive specificotions ore provided for operoting chorocteristics over the temperoture ronge of 0°C to 70°C. This logic series includes the bosic goting ond flip-flop elements needed to perform procticolly all functions required of generol-purpose industriol digital systems.



TYPE SN7400 PRIOR TO CAPPING

features

LOW SYSTEM COST

- maximum number of circuits per package through use of 14-lead package

OPTIMUM CIRCUIT PERFORMANCE

- high speed — typical propagation delay time 13 nsec
- high d-c noise margin — typically one volt
- low output impedance provides low a-c noise susceptibility
- waveform integrity over full range of loading and temperature conditions
- low power dissipation — 10 mw per gate at 50% duty cycle
- full fan-out of 10

CONTENTS

†Patented by Texas Instruments Incorporated.

TEXAS INSTRUMENTS
INCORPORATED
SEMICONDUCTOR-COMPONENTS DIVISION
POST OFFICE BOX 5012 • DALLAS 22, TEXAS

design characteristics

Series 74 digitol integrated circuits effect on optimizotion between soturoted logic circuitry ond monolithic semiconductor technology yielding high performonce at lowest cost. In discrete component circuitry maximum use is made of lower cost components (diodes ond resistors) instead of the higher priced tronsistors. However, in monolithic circuitry it costs no more to build tronsistors thon diodes or resistors. Therefore, in Series 74, tronsistors ore used to buffer the fluctuotions in currents thot occur os resistor volues chonge. Also, the Series 74 multiple emitter tronsistor con eosily be built in o monolithic bor to eliminate the need for conventionol input diodes.

circuit operation

The tronsistor-transistor logic (TTL) used in Series 74 is onologous to diode-transistor logic (DTL) in certain respects. As shown in figure A, a low voltage at inputs A or B will ollow current to flow through the diode ossociated with the low input, ond no drive current will pass through diode D_3. If inputs A ond B ore roised to a high voltage, drive current will then pass through diode D_3.

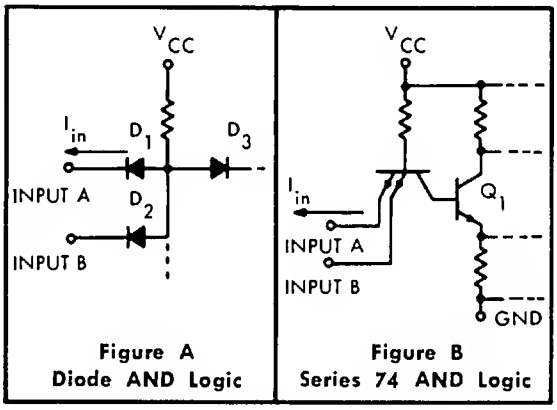


Figure A Diode AND Logic | **Figure B Series 74 AND Logic**

In Series 74 TTL circuitry, the multiple-emitter transistor performs the some function as the diodes in DTL (see figure B). However, the tronsistor oction of the multiple-emitter tronsistor couses tronsistor Q_1 to turn-off more ropidly, thus providing on inherent switching-time odvontoge over the DTL circuit.

Although one-volt d-c noise morgins ore typical for Series 74 circuits, an obsolute guorontee of 400 millivolts is ossured for every unit. This is accomplished by testing eoch output ond input os shown in figures C ond D.

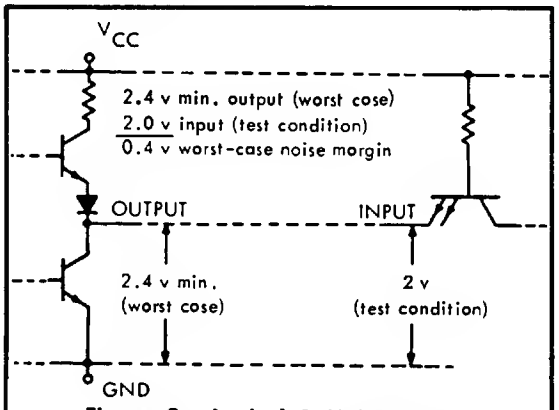


Figure C — Logical 1 Noise Margin

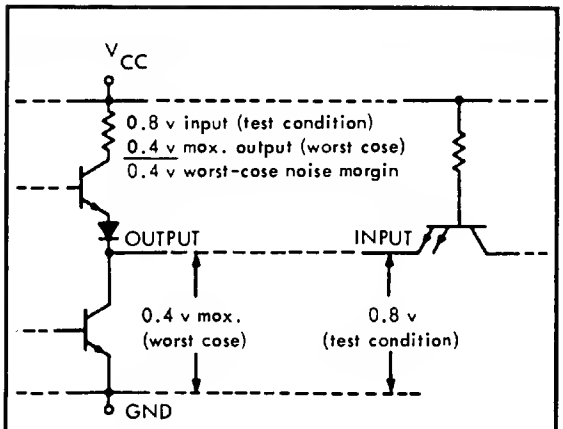


Figure D — Logical O Noise Margin

Eoch output is tested over the full temperoture ronge to ensure thot the logicol 1 output voltoge will not foll below 2.4 volts. This is done with full fon-out, lowest V_{CC}, ond 0.8 volts on the input — 400 mv more than the logicol 0 moximum.

Eoch output is tested over the full temperoture ronge to ensure thot the logicol 0 output voltoge will not exceed 0.4 volts. This is done with full fan-out, lowest V_{CC}, ond 2 volts on the input — 400 mv less thon the logicol 1 minimum.

In octuol system operation, the mojority of circuits do not experience worst-cose conditions of fon-out, supply voltoge, temperoture, and input voltoge simultoneously. In addition, the threshold voltoge of the Series 74 circuits is obout 1.5 volts. These chorocteristics allow o larger voltage chonge on on input without folse triggering. This typicol noise margin is shown in figure E.

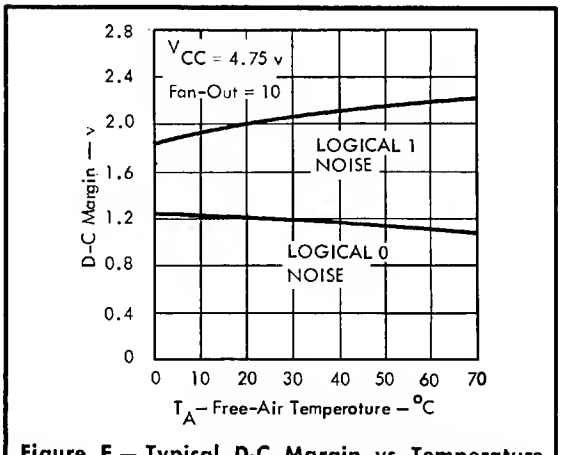


Figure E — Typical D-C Margin vs Temperature

Another importont feoture of the design is the output configurotion which both supplies current (in the logical 1 stote) ond sinks current (in the logical 0 state) from a low impedonce. Typically, logical 0 output impedonce is 12 Ω ond logicol 1 output impedonce is 100 Ω. This low output impedonce in either stote rejects cqpocitively coupled o-c pulses ond ensures small R-C time constants which preserve wove-shape integrity.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply Voltage, V_{CC} (See Note 1) . . . . . .8 v
Input Voltage, V_{in} (See Notes 1 and 2) . . . . . .5.5 v
Operating Free-Air Temperature Range . . . . . 0°C to +70°C
Storage Temperature Range . . . . . −65°C to +150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. Input signals must be zero or positive with respect to network ground terminal.

logic definition

Series 74 logic is defined in terms of standard POSITIVE LOGIC using the following definitions:

LOW VOLTAGE = LOGICAL 0
HIGH VOLTAGE = LOGICAL 1

input-current requirements

Input-current requirements reflect worst-case conditions for $T_A = 0°C$ to 70°C and $V_{CC} = 4.75$ to 5.25 v. Each input of the multiple-emitter input transistor requires that no more than 1.6 ma flow out of the input at a logical 0 voltage level; therefore, one load (N = 1) is 1.6 ma maximum. The flip-flop preset and clear inputs supply two multiple-emitter transistors; thus, each preset or clear input is the equivalent of N = 2 loads. Each input requires current into the input at a logical 1 voltage level. This current is 40 μa maximum for all inputs except for the preset and clear which are 80 μa maximum.

fan-out capability

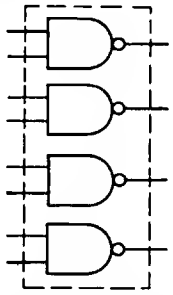
Fan-out reflects the ability of an output to sink current from a number of loads (N) at a logical 0 voltage level and to supply current at a logical 1 voltage level. Each output is capable of sinking current or supplying current to 10 loads (N = 10). The "power" gate is capable of sinking current or supplying current to 30 loads (N=30).

unused inputs

All unused inputs except J★ and K★ should be connected to V_{CC}. Unused J★ or K★ input should be connected to ground.

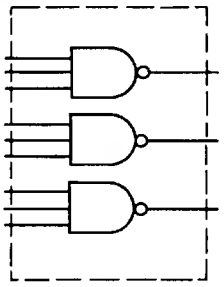
standard line summary

SN7400 See page 4



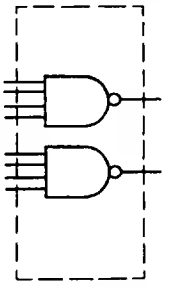
QUADRUPLE 2-INPUT POSITIVE NAND GATE

SN7410 See page 5



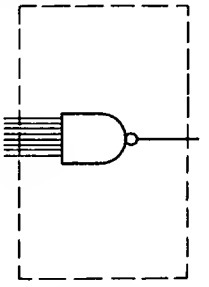
TRIPLE 3-INPUT POSITIVE NAND GATE

SN7420 See page 6



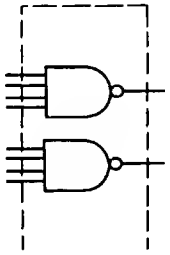
DUAL 4-INPUT POSITIVE NAND GATE

SN7430 See page 7



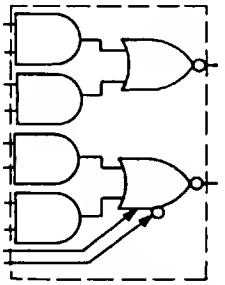
8-INPUT POSITIVE NAND GATE

SN7440 See page 8



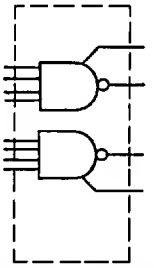
DUAL 4-INPUT POSITIVE NAND "POWER" GATE

SN7450 See page 9



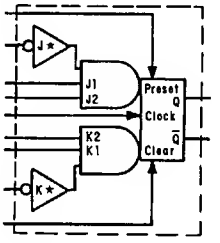
EXPANDABLE DUAL EXCLUSIVE-OR GATE

SN7460 See page 11



DUAL 4-INPUT EXPANDER FOR SN7450

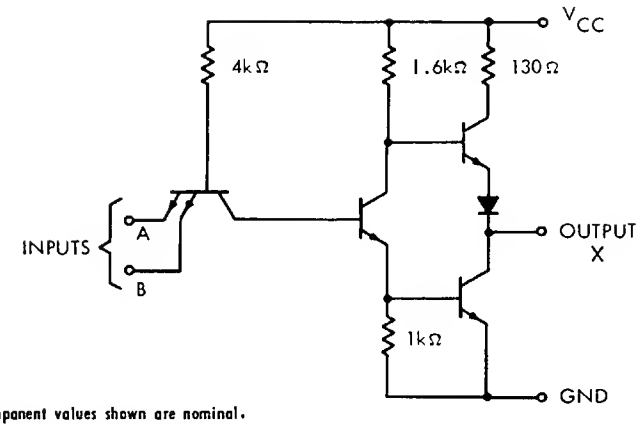
SN7470 See page 12



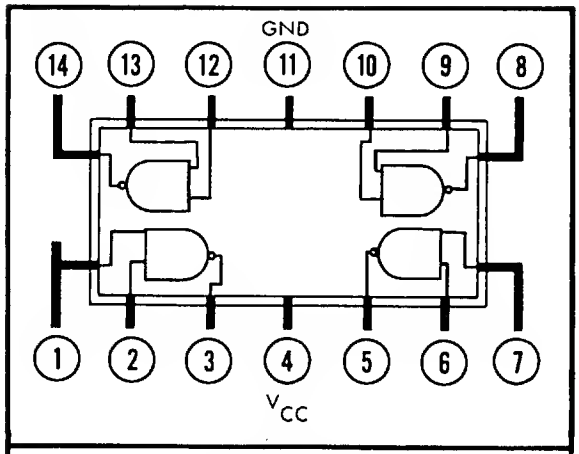
J-K FLIP-FLOP

TYPE SN7400
QUADRUPLE 2-INPUT POSITIVE NAND GATE

schematic (each gate)



Component values shown are nominal.



positive logic

$X = \overline{AB}$

recommended operating conditions

Supply Voltage, V_{CC} . . . . . 4.75 v to 5.25 v

Maximum Fan-Out From Each Output, N 10

electrical characteristics, $T_A = 0°C$ to $70°C$

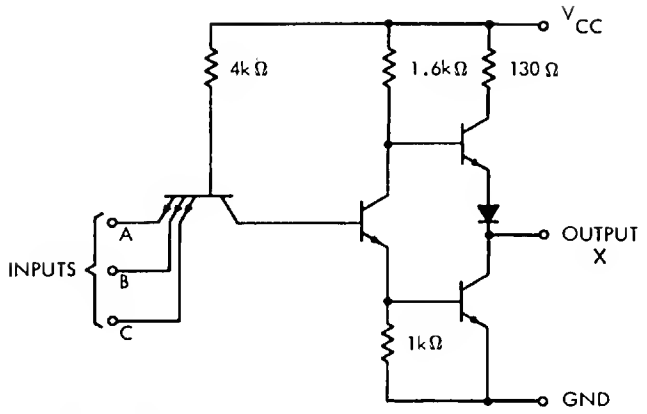
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals that will ensure logical 0 level ot output	1	V_{CC} = 4.75 v, $V_{out(0)} \leq$ 0.4 v, R = 272 Ω	2			v
$V_{in(0)}$	Logical 0 input valtage required at any input terminol that will ensure logicol 1 level at output	2	V_{CC} = 4.75 v, $V_{out(1)} \geq$ 2.4 v, R = 6 kΩ			0.8	v
$V_{out(1)}$	Logicol 1 output voltage	2	V_{CC} = 4.5 v, V_{in} = 0.8 v, $I_{load} \geq$ 400 μa, R = 6 kΩ	2.4			v
$V_{out(0)}$	Logicol 0 output voltage	1	V_{CC} = 4.75 v, V_{in} = 2 v, $I_{sink} \geq$ 16 ma, R = 272 Ω			0.4	v
I_{in}	Input current (each input)	3	V_{CC} = 5.25 v, V_{in} = 0.4 v			1.6	mo
I_{in}	Input current (each input)	4	V_{CC} = 5.25 v, V_{in} = 4.75 v			40	μa
I_{OS}	Short-circuit output current†	5	V_{CC} = 5.25 v	18		55	ma
$I_{CC(0)}$	Logical 0 level supply current (eoch gate)	6	V_{CC} = V_{in} = 5 v		3		mo
$I_{CC(1)}$	Logical 1 level supply current (each gate)	6	V_{CC} = 5 v, V_{in} = 0		1		ma

switching characteristics, $V_{CC} = 5$ v, $T_A = 25°C$

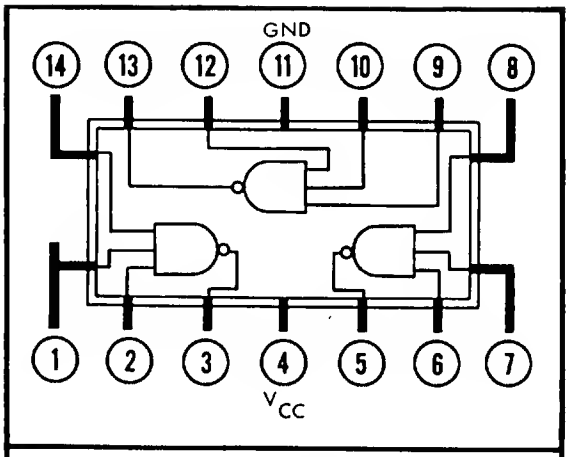
PARAMETER		TEST FIGURE	TEST CONDITIONS	TYP	MAX	UNIT
t_{d0}	Prapagatian time to logicol 0	27	C_1 = 15 pf, N = 10	8	15	nsec
t_{d1}	Propagation time ta lagical 1	27	C_1 = 15 pf, N = 1	18	29	nsec

†Nat more than ane autput should be shorted at a time.

schematic (each gate)



Component values shown are nominal.



positive logic

$X = \overline{ABC}$

recommended operating conditions

Supply Voltage, V_{CC} . . . . . 4.75 v to 5.25 v

Maximum Fan-Out From Each Output, N 10

electrical characteristics, $T_A = 0°C$ to $70°C$

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$	Logicol 1 input voltoge required ot oll input terminols thot will ensure logical 0 level at output	1	V_{CC} = 4.75 v, $V_{out(0)} \leq$ 0.4 v, R = 272 Ω	2			v
$V_{in(0)}$	Logicol 0 input voltage required ot ony input terminol thot will ensure logical 1 level at output	2	V_{CC} = 4.75 v, $V_{out(1)} \geq$ 2.4 v, R = 6 kΩ			0.8	v
$V_{out(1)}$	Logical 1 output voltage	2	V_{CC} = 4.75 v, V_{in} = 0.8 v, $I_{load} \geq$ 400 μa, R = 6 kΩ	2.4			v
$V_{out(0)}$	Logicol 0 output voltage	1	V_{CC} = 4.75 v, V_{in} = 2 v, $I_{sink} \geq$ 16 ma, R = 272 Ω			0.4	v
I_{in}	Input current (each input)	3	V_{CC} = 5.25 v, V_{in} = 0.4 v			1.6	ma
I_{in}	Input current (each input)	4	V_{CC} = 5.25 v, V_{in} = 4.75 v			40	μo
I_{OS}	Short-circuit output current†	5	V_{CC} = 5.25 v	18		55	ma
$I_{CC(0)}$	Logicol 0 level supply current (eoch gate)	6	$V_{CC} = V_{in}$ = 5 v		3		mo
$I_{CC(1)}$	Logicol 1 level supply current (eoch gate)	6	V_{CC} = 5 v, V_{in} = 0		1		ma

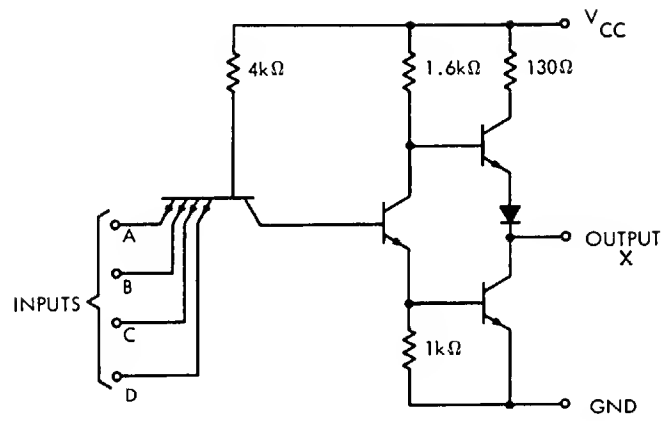
switching characteristics, $V_{CC} = 5$ v, $T_A = 25°C$

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{d0}	Propagation time to logical 0	27	C_l = 15 pf, N = 10		8	15	nsec
t_{d1}	Propogotion time to logicol 1	27	C_l = 15 pf, N = 1		18	29	nsec

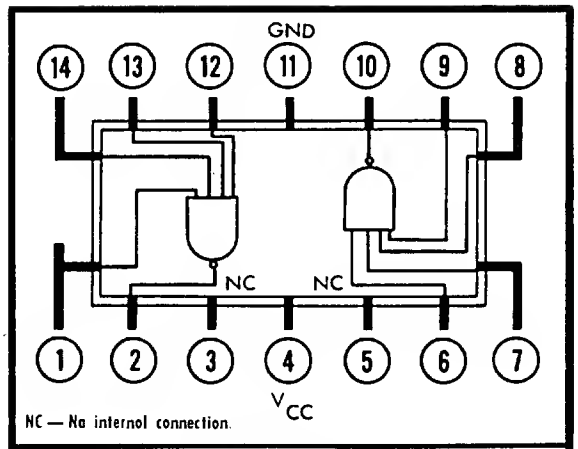
†Not more than one output should be shorted at a time.

TYPE SN7420
DUAL 4-INPUT POSITIVE NAND GATE

schematic (each gate)



Component values shown are nominal.



positive logic

$X = \overline{ABCD}$

recommended operating conditions

Supply Voltage, V_{CC} . . . . . 4.75 v to 5.25 v

Maximum Fan-Out From Each Output, N 10

electrical characteristics, T_A = 0°C to 70°C

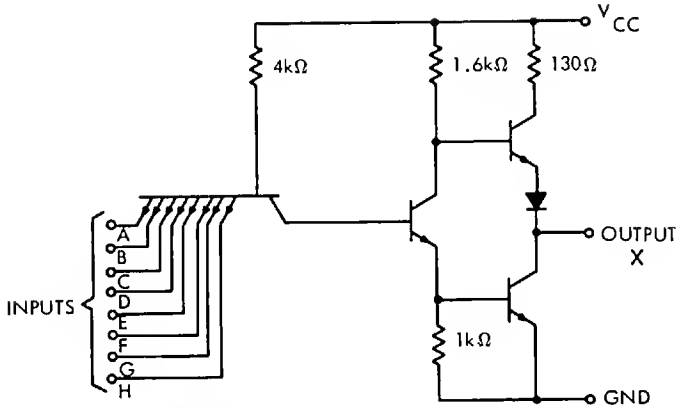
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals that will ensure logical 0 level at output	1	V_{CC} = 4.75 v, $V_{out(0)} \leq$ 0.4 v, R = 272 Ω	2			v
$V_{in(0)}$	Logical 0 input voltage required at any input terminal that will ensure logical 1 level at output	2	V_{CC} = 4.75 v, $V_{out(1)} \geq$ 2.4 v, R = 6 kΩ			0.8	v
$V_{out(1)}$	Logical 1 output voltage	2	V_{CC} = 4.75 v, V_{in} = 0.8 v, $I_{load} \geq$ 400 μa, R = 6 kΩ	2.4			v
$V_{out(0)}$	Logical 0 output voltage	1	V_{CC} = 4.75 v, V_{in} = 2 v, $I_{sink} \geq$ 16 ma, R = 272 Ω			0.4	v
I_{in}	Input current (each input)	3	V_{CC} = 5.25 v, V_{in} = 0.4 v			1.6	ma
I_{in}	Input current (each input)	4	V_{CC} = 5.25 v, V_{in} = 4.75 v			40	μa
I_{OS}	Short-circuit output current†	5	V_{CC} = 5.25 v	18		55	ma
$I_{CC(0)}$	Logical 0 level supply current (each gate)	6	V_{CC} = V_{in} = 5 v		3		ma
$I_{CC(1)}$	Logical 1 level supply current (each gate)	6	V_{CC} = 5 v, V_{in} = 0		1		ma

switching characteristics, V_{CC} = 5 v, T_A = 25°C

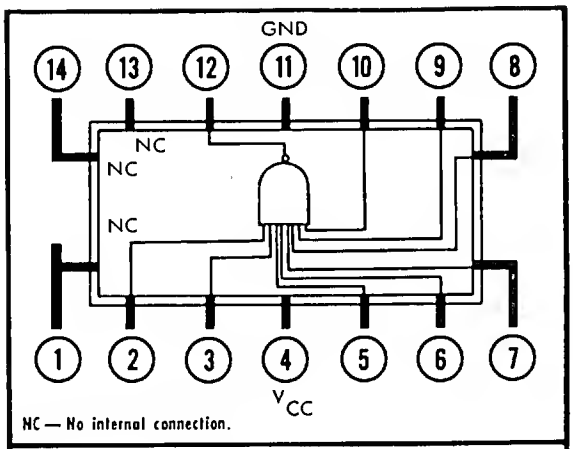
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{d0}	Propagation time to logical 0	27	C_l = 15 pf, N = 10		8	15	nsec
t_{d1}	Propagation time to logical 1	27	C_l = 15 pf, N = 1		18	29	nsec

†Not more than one output should be shorted at a time.

schematic (each gate)



Component values shown are nominal.



NC — No internal connection.

positive logic

$X = \overline{ABCDEFGH}$

recommended operating conditions

Supply Voltage, V_{CC}	4.75 v to 5.25 v
Maximum Fan-Out From Each Output, N	10

electrical characteristics, $T_A = 0°C$ to 70°C

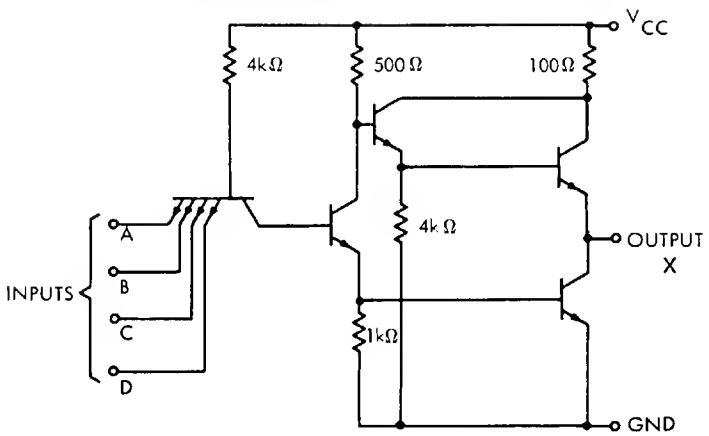
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals that will ensure logical 0 level at output	1	V_{CC} = 4.75 v, $V_{out(0)} \leq$ 0.4 v, R = 272 Ω	2			v
$V_{in(0)}$	Logical 0 input voltage required at any input terminal that will ensure logical 1 level at output	2	V_{CC} = 4.75 v, $V_{out(1)} \geq$ 2.4 v, R = 6 kΩ			0.8	v
$V_{out(1)}$	Logical 1 output voltage	2	V_{CC} = 4.75 v, V_{in} = 0.8 v, $I_{load} \geq$ 400 μa, R = 6 kΩ	2.4			v
$V_{out(0)}$	Logical 0 output voltage	1	V_{CC} = 4.75 v, V_{in} = 2 v, $I_{sink} \geq$ 16 ma, R = 272 Ω			0.4	v
I_{in}	Input current (each input)	3	V_{CC} = 5.25 v, V_{in} = 0.4 v			1.6	ma
I_{in}	Input current (each input)	4	V_{CC} = 5.25 v, V_{in} = 4.75 v			40	μa
I_{OS}	Short-circuit output current	5	V_{CC} = 5.25 v	18		55	ma
$I_{CC(0)}$	Logical 0 level supply current (each gate)	6	V_{CC} = V_{in} = 5 v		3		ma
$I_{CC(1)}$	Logical 1 level supply current (each gate)	6	V_{CC} = 5 v, V_{in} = 0		1		ma

switching characteristics, $V_{CC} = 5$ v, $T_A = 25°C$

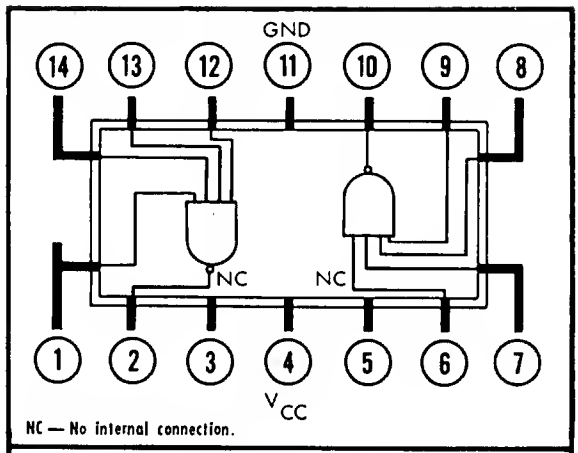
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{d0}	Propagation time to logical 0	27	C_l = 15 pf, N = 10		8	15	nsec
t_{d1}	Propagation time to logical 1	27	C_l = 15 pf, N = 1		18	29	nsec

TYPE SN7440
DUAL 4-INPUT POSITIVE NAND "POWER" GATE

schematic (each gate)



Component values shown are nominal



positive logic

$X = \overline{ABCD}$

recommended operating conditions

Supply Voltage, V_{CC}	4.75 v to 5.25 v
Maximum Fan-Out From Each Output, N	30

electrical characteristics, $T_A =$ 0°C to 70°C

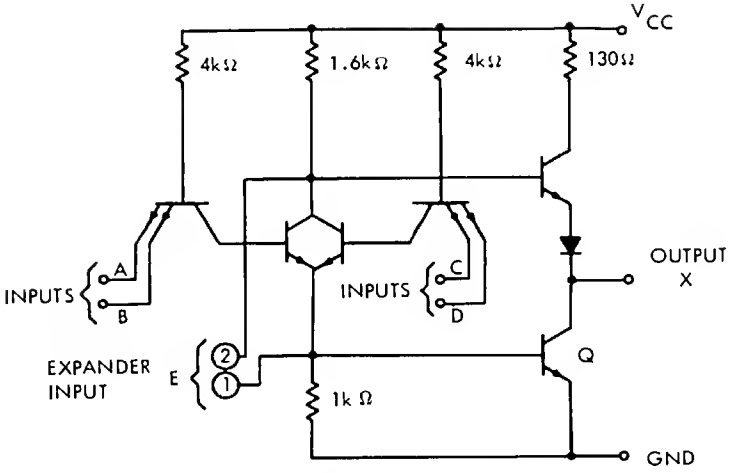
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$	Lagical 1 input voltage required ot all input terminols that will ensure logical 0 level at output	1	V_{CC} = 4.75 v, $V_{out(0)} \leq$ 0.4 v, R = 90 Ω	2			v
$V_{in(0)}$	Logical 0 input voltage required ot ony input terminol that will ensure logical 1 level at output	2	V_{CC} = 4.75 v, $V_{out(1)} \geq$ 2.4 v, R = 2 kΩ			0.8	v
$V_{out(1)}$	Logicol 1 output voltoge	2	V_{CC} = 4.75 v, V_{in} = 0.8 v, $I_{load} \geq$ 1.2ma, R = 2 kΩ	2.4			v
$V_{out(0)}$	Logical 0 output voltage	1	V_{CC} = 4.75 v, V_{in} = 2 v, $I_{sink} \geq$ 16 ma, R = 90 Ω			0.4	v
I_{in}	Input current (eoch input)	3	V_{CC} = 5.25 v, V_{in} = 0.4 v			1.6	mo
I_{in}	Input current (each input)	4	V_{CC} = 5.25 v, V_{in} = 4.75 v			40	μa
I_{OS}	Short-circuit output current†	5	V_{CC} = 5.25 v	18		70	mo
$I_{CC(0)}$	Logical 0 level supply current (each gate)	6	V_{CC} = V_{in} = 5 v		8.6		ma
$I_{CC(1)}$	Logicol 1 level supply current (eoch gate)	6	V_{CC} = 5 v, V_{in} = 0		2		mo

switching characteristics, $V_{CC} = 5$ v, $T_A = 25°C$

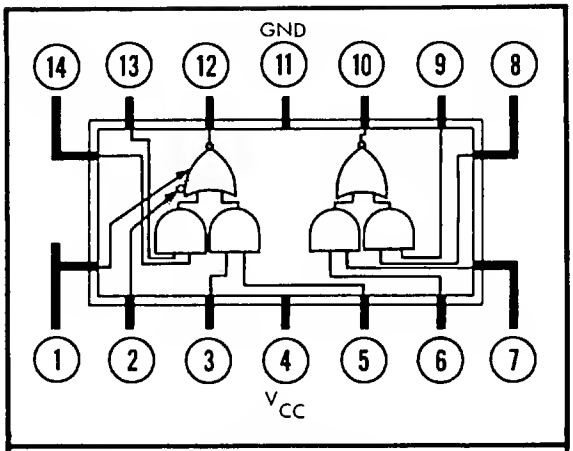
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{d0}	Propogation time to logical 0	27	C_l = 15 pf, N = 10		8	15	nsec
t_{d1}	Propagatian time to logical 1	27	C_l = 15 pf, N = 1		18	29	nsec

†Not more thon one output should be shorted ot a time.

schematic (each gate)



NOTES: 1. Component values shown are nominal.
2. Both expander inputs are used simultaneously for expanding with the SN7460.
3. If expander is not used leave pins (1) and (2) open.



positive logic

$X = \overline{(AB) + (CD) + E}$

$E = ABCD$ from SN7460

recommended operating conditions

Supply Voltage, V_{CC} . . . . . 4.75 v to 5.25 v

Maximum Fan-Out From Each Output, N 10

electrical characteristics, T_A = – 0°C to 70°C , pins (1) and (2) open

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals that will ensure logical 0 level ot output	7	V_{CC} = 4.75 v, $V_{out(0)} \leq$ 0.4 v, R = 272 Ω	2			v
$V_{in(0)}$	Logical 0 input voltage required at any input terminal thot will ensure logical 1 level at output	8	V_{CC} = 4.75 v, $V_{out(1)} \geq$ 2.4 v, R = 6 kΩ			0.8	v
$V_{out(1)}$	Logical 1 output voltage	8	V_{CC} = 4.75 v, V_{in} = 0.8 v, $I_{load} \geq$ 400 μa, R = 6 kΩ	2.4			v
$V_{out(0)}$	Logical 0 output voltage	7	V_{CC} = 4.75 v, V_{in} = 2 v, $I_{sink} \geq$ 16 ma, R = 272 Ω			0.4	v
I_{in}	Input current (each input)	9	V_{CC} = 5.25 v, V_{in} = 0.4 v			1.6	ma
I_{in}	Input current (each input)	10	V_{CC} = 5.25 v, V_{in} = 4.75 v			40	μa
I_{OS}	Short-circuit output current†	11	V_{CC} = 5.25 v	18		55	ma
$I_{CC(0)}$	Logical 0 level supply current (each gate)	12	V_{CC} = V_{in} = 5 v		3.7		ma
$I_{CC(1)}$	Logical 1 level supply current (each gate)	13	V_{CC} = 5 v, V_{in} = 0		2		ma

†Not more than one output should be shorted at a time.

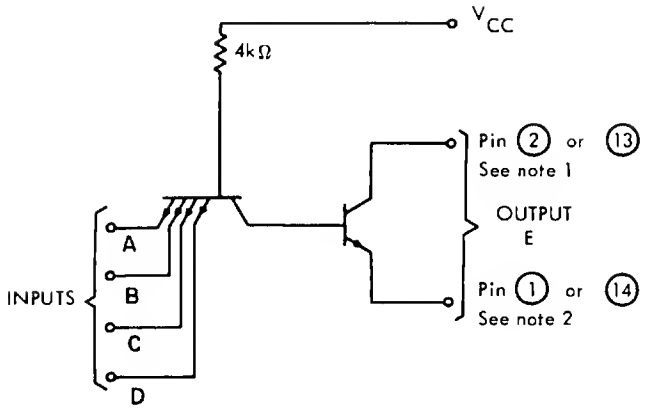
electrical characteristics using expander inputs, $T_A = 0°C$

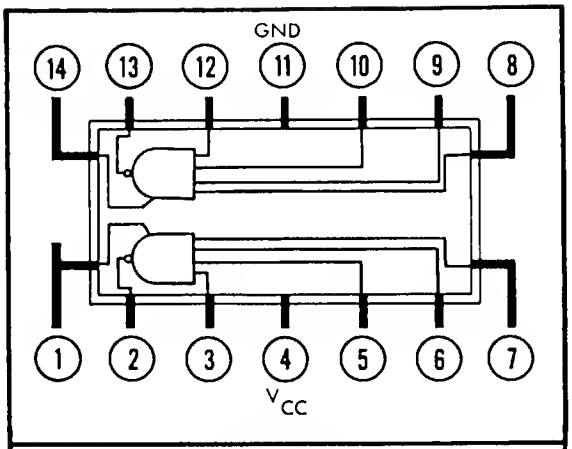
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
$I_{(X)}$	Expander current	14	$V_{CC} = 4.75$ v, $V_1 = 0.4$ v, $I_{sink} = 16$ ma	1.5	3.1	ma
$V_{BE(Q)}$	Output transistor (Q) base-emitter voltage	15	$V_{CC} = 4.75$ v, $V_2 = 1.4$ v, $I_{sink} = 16$ ma, $I_1 = 1.7$ mo, $R = 272\ \Omega$		1	v
$V_{out(0)}$	Lagical 0 output voltage	15	$V_{CC} = 4.75$ v, $V_2 = 1.4$ v, $I_{sink} = 16$ ma, $I_1 = 1.7$ ma, $R = 272\ \Omega$		0.4	v
$V_{out(1)}$	Logical 1 output voltage	16	$V_{CC} = 4.75$ v, $I_{load} = 400\ \mu a$ $I_1 = 0.27$ ma, $I_2 = 0.27$ ma, $R = 6\ k\Omega$	2.4		v

switching characteristics, $V_{CC} = 5$ v, $T_A = 25°C$

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{d0}	Propagation time to logical 0	27	$C_1 = 15$ pf, $N = 10$		8	15	nsec
t_{d1}	Propagation time to logical 1	27	$C_1 = 15$ pf, $N = 1$		18	29	nsec

schematic





positive logic
E = ABCD
When connected to pins (1) and (2) of SN7450

NOTES: 1. Connect pin (2) or (13) to pin (2) of SN7450.
2. Connect pin (1) or (14) to pin (1) of SN7450.
3. Component values shown are nominal.

recommended operating conditions

Supply Voltage, V_{CC} . . . . . 4.75 v to 5.25 v
Maximum number of expanders that may be fanned-in to one SN7450 4

electrical characteristics (unless otherwise noted $T_A = 0°C$ to $70°C$)

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in[1]}$	Logicol 1 input voltage required ot all input terminals that will ensure output on level	17	V_{CC} = 4.75 v, V_{in} = 2 v, V_1 = 1 v, R = 1.1 kΩ, T_A = 0°C	2			v
$V_{in[0]}$	Logicol 0 input voltage at any input terminal that will ensure output off level current	18	V_{CC} = 4.75 v, V_{in} = 0.8 v, V_1 = 4.75 v, R = 1.2 kΩ, I_{off} = 0.27 ma, T_A = 0°C			0.8	v
V_{on}	Output voltage on level	17	V_{CC} = 4.75 v, V_{in} = 2 v, V_1 = 1 v, R = 1.1 kΩ, T_A = 0°C			0.4	v
I_{off}	Output off level current	18	V_{CC} = 4.75 v, V_{in} = 0.8 v, V_1 = 4.75 v, R = 1.2 kΩ, T_A = 0°C			270	μa
I_{on}	Output an level current	19	V_{CC} = 4.75 v, V_{in} = 2 v, V_1 = 1 v, I_2 = 1.5 ma	1.7			mo
I_{in}	Input current (each input)	18	V_{CC} = 5.25 v, V_{in} = 0.4 v			1.6	ma
I_{in}	Input current (eoch input)	20	V_{CC} = 5.25 v, V_{in} = 4.75 v, T_A = 70°C			40	μa
$I_{CC[on]}$	On level supply current (each gate)	21	V_{CC} = V_{in} = 5 v, V_1 = 0.85 v		0.6		ma
$I_{CC[off]}$	Off level supply current (eoch gote)	21	V_{CC} = 5 v, V_{in} = 0, V_1 = 0.85 v		1		mo

switching characteristics, $V_{CC} = 5$ v, $T_A = 25°C$

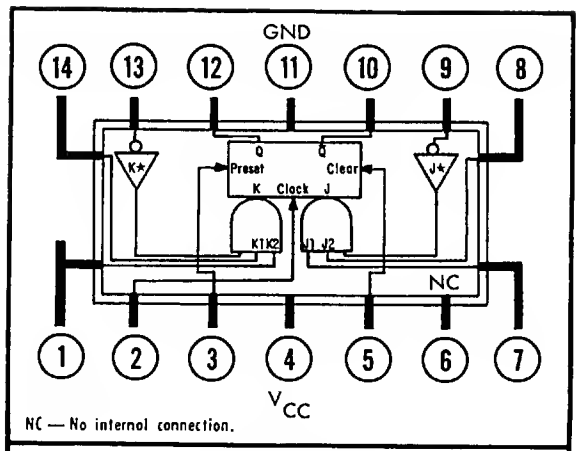
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{d0}	Propagatian time to logical 0 (through SN7450)	28	C_1 = 15 pf, N = 10		10	20	nsec
t_{d1}	Propagatian time to logical 1 (through SN7450)	28	C_1 = 15 pf, N = 1		20	34	nsec

TYPE SN7470
J-K FLIP-FLOP

logic

TRUTH TABLE		
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q_n}$

NOTES: 1. $J = J1 \cdot J2 \cdot \overline{J}\bigstar$
2. $K = K1 \cdot K2 \cdot \overline{K}\bigstar$
3. t_n = Bit time before clock pulse.
4. t_{n+1} = Bit time after clock pulse.
5. If inputs J★ or K★ are not used they must be grounded.



NC — No internal connection.

positive logic
Low input to preset sets Q to logical 1
Low input to clear sets Q to logical 0

recommended operating conditions

Supply Voltage, V_{CC}	4.75 v to 5.25 v
Maximum Fan-Out From Each Output, N	10
Maximum Rise Time of Clock Pulse, $t_{r(clock)}$	150 nsec
Minimum Width of Clock Pulse, $t_{p(clock)}$	20 nsec
Toggle Frequency, f_{toggle}	0 to 25 Mc
Minimum Set-Up Time At Inputs J★ or K★; $t_{set\text{-}up}$	20 nsec
Minimum Hold Time At Inputs J1, J2, K1, or K2; t_{hold}	15 nsec
Minimum Preset Time, t_{preset}	25 nsec
Minimum Cleor Time, t_{clear}	25 nsec

electrical characteristics (unless otherwise noted V_{CC} = 4.75 v to 5.25 v, T_A = 0°C to 70°C)

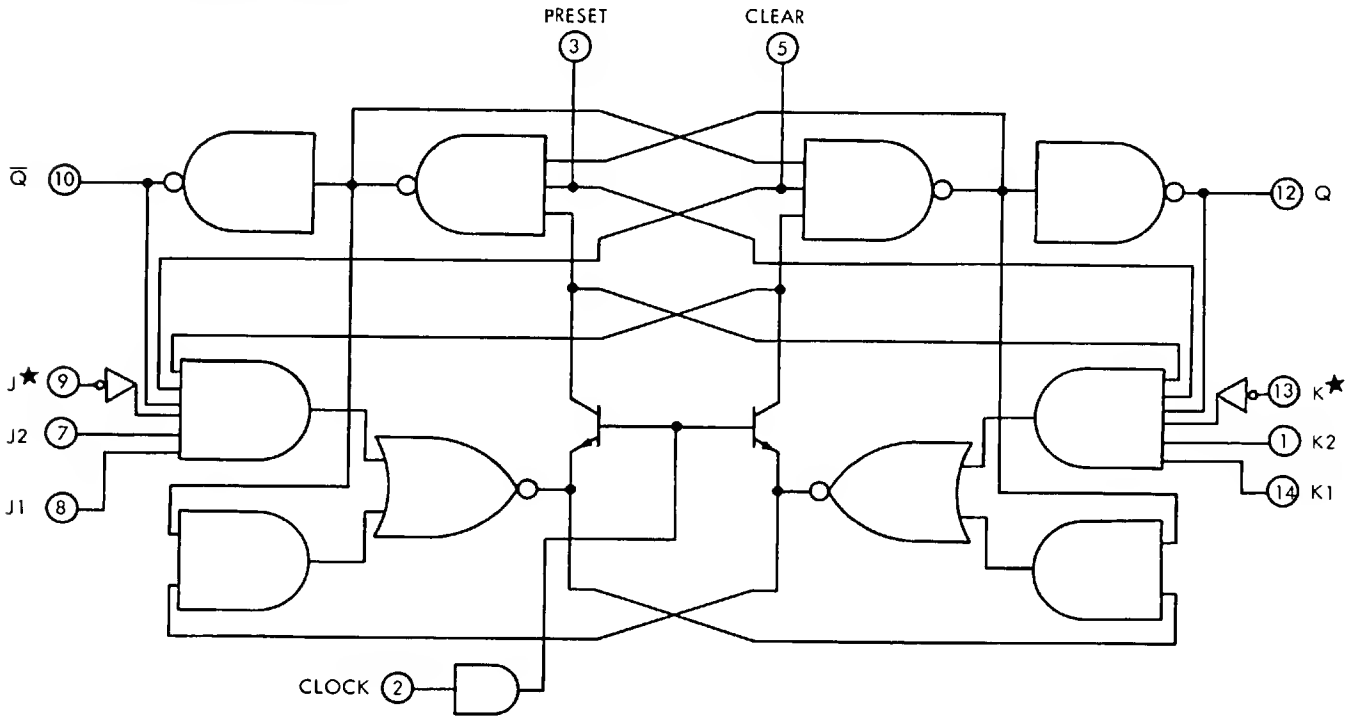
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{in(1)}$	Input voltage thot will ensure logicol 1 ot ony input terminol	22	V_{CC} = 4.75 v	2			v
$V_{in(0)}$	Input voltage thot will ensure logicol 0 ot ony input terminol	22	V_{CC} = 5.25 v			0.8	v
$V_{out(1)}$	Logical 1 output voltoge	22	V_{CC} = 4.75 v, I_{load} = 400 μo, R = 6 kΩ	2.4			v
$V_{out(0)}$	Logicol 0 output voltoge	23	V_{CC} = 4.75 v, I_{sink} = 16 mo, R = 272 Ω			0.4	v
I_{in}	J1, J2, J★, K1, K2, K★ or clock input current	24	V_{CC} = 5.25 v, V_{in} = 0.4 v			1.6	mo
I_{in}	Preset or cleor input current	24	V_{CC} = 5.25 v, V_{in} = 0.4 v			3.2	ma
I_{in}	J1, J2, J★, J1, K2, K★, or clock input current	25	V_{CC} = 5.25 v, V_{in} = 4.75 v, T_A = 70°C			40	μo
I_{in}	Preset or clear input current	25	V_{CC} = 5.25 v, V_{in} = 4.75 v, T_A = 70°C			80	μo
I_{OS}	Short-circuit output current†	26	V_{CC} = 5.25 v, V_{in} = 0	18		57	mo
$I_{CC(av)}$	Averoge supply current	25	V_{CC} = V_{in} = 5 v		14		mo

†Not more thon one output should be shorted at a time.

switching characteristics, $V_{CC} = 5$ v, $T_A = 25°C$

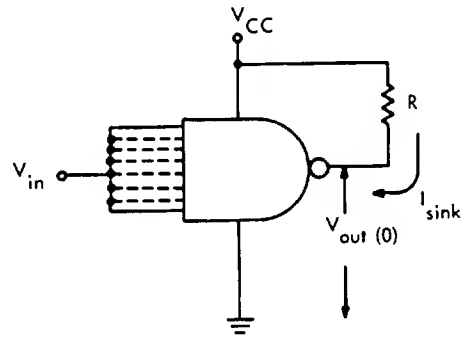
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{set\text{-}up}$	Minimum Input Set-Up Time	29			15		nsec
t_{hold}	Minimum Input Hold Time				10		nsec
t_{preset}	Minimum Preset Time	30			15		nsec
t_{clear}	Minimum Clear Time				15		nsec
t_{d0}	Propogation time to logical 0	29	C_l = 15 pf, N = 10		30	50	nsec
t_{d1}	Propogation time to logicol 1	29	C_l = 15 pf, N = 1		30	50	nsec

functional block diagram



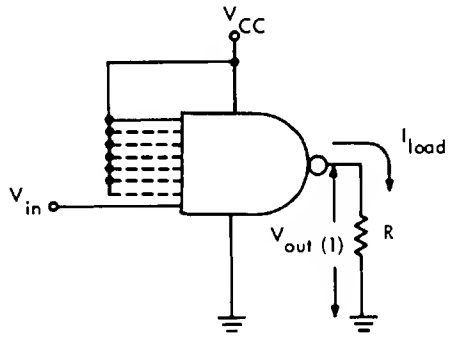
PARAMETER MEASUREMENT INFORMATION

d-c test circuits



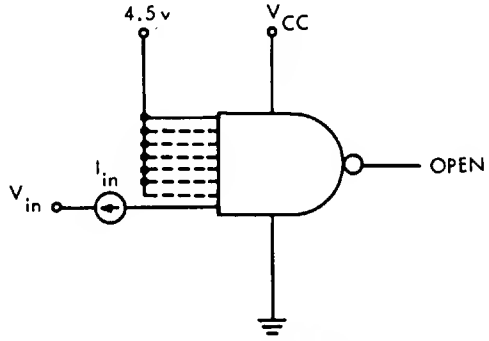
1. All inputs tested simultaneously.

FIGURE 1



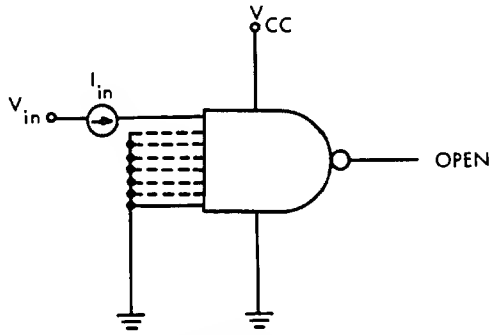
1. Each input tested separately.

FIGURE 2



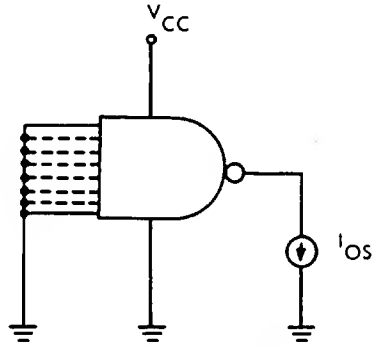
1. Each input tested separately.

FIGURE 3



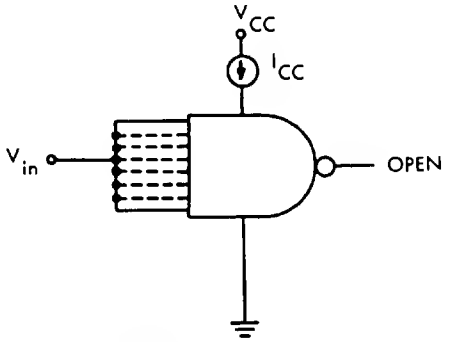
1. Each input tested separately.

FIGURE 4



1. Each gate tested separately.

FIGURE 5

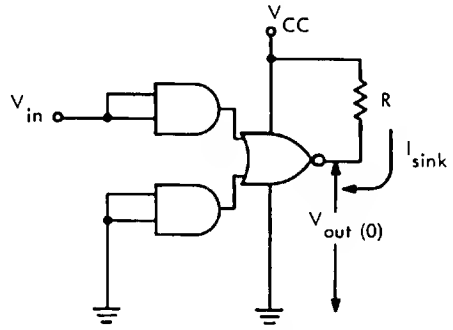


1. Test logical 0 and logical 1 conditions.

FIGURE 6

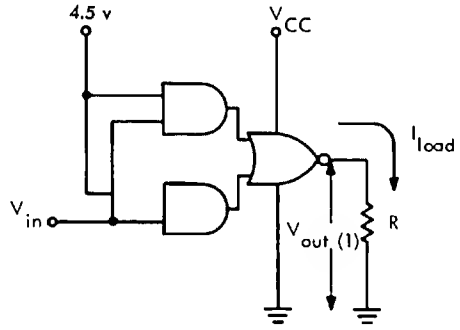
PARAMETER MEASUREMENT INFORMATION

d-c test circuits (continued)



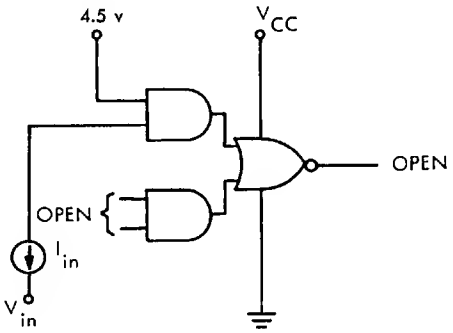
1. Each AND section tested separately.

FIGURE 7



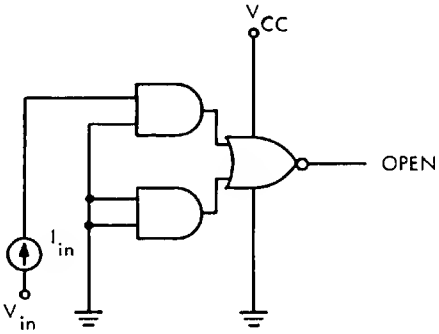
1. Each pair of inputs tested separately.

FIGURE 8



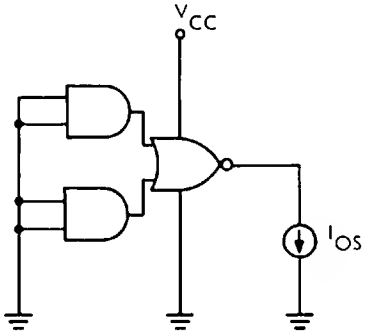
1. Each input tested separately.

FIGURE 9



1. Each input tested separately.

FIGURE 10



1. Each gate tested separately.

FIGURE 11

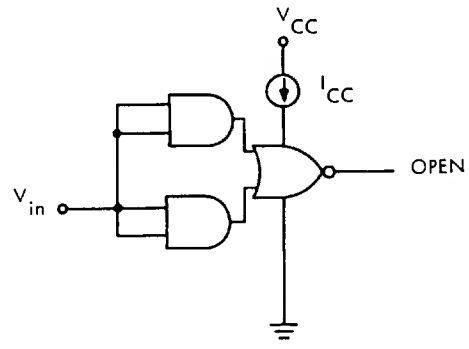


FIGURE 12

PARAMETER MEASUREMENT INFORMATION

d-c test circuits (continued)

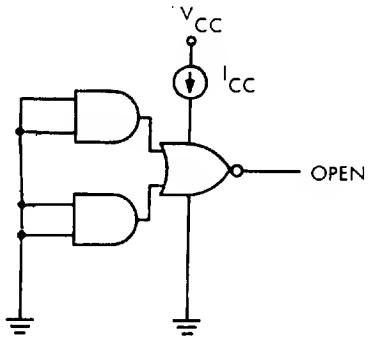


FIGURE 13

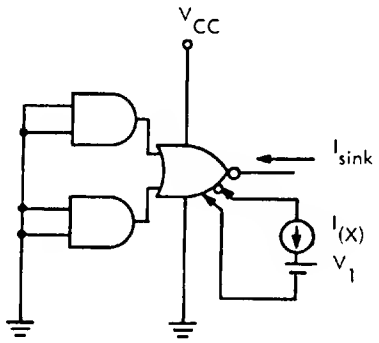


FIGURE 14

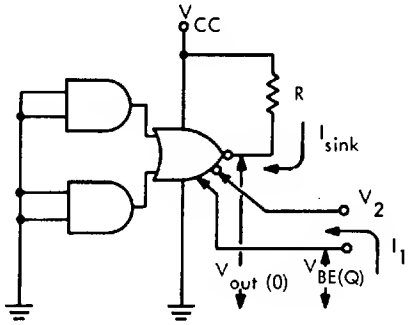


FIGURE 15

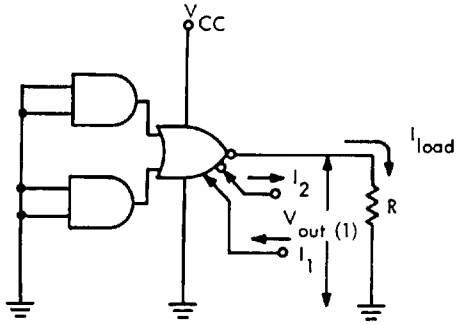
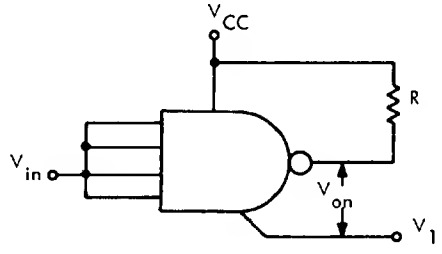
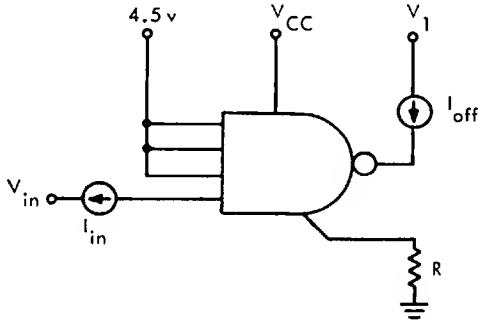


FIGURE 16



1. All inputs tested simultaneously.

FIGURE 17



1. Each input tested separately.

FIGURE 18

PARAMETER MEASUREMENT INFORMATION

d-c test circuits (continued)

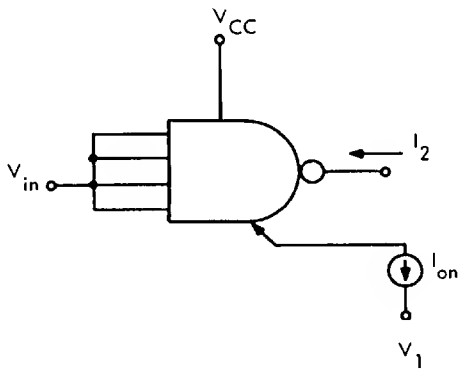
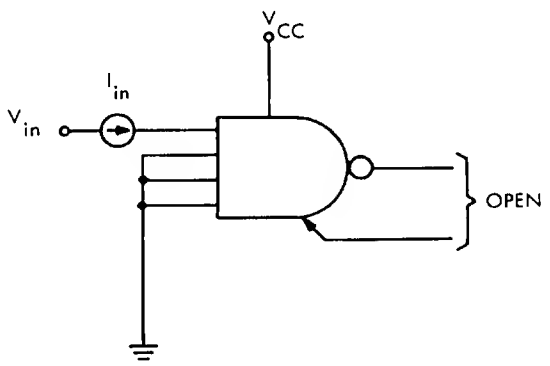
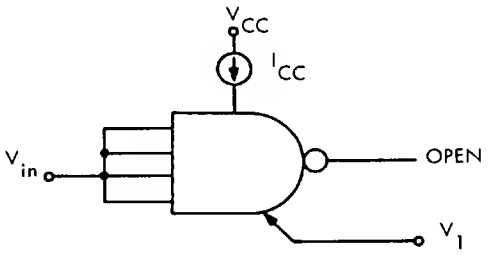


FIGURE 19



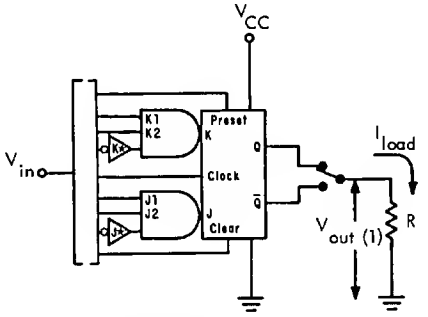
1. Each input tested seporotely.

FIGURE 20



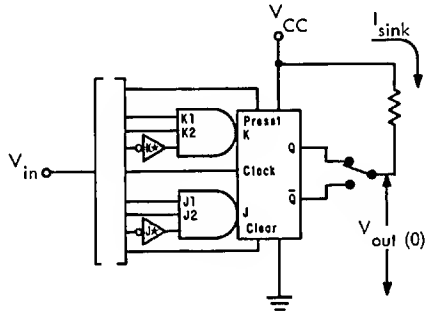
1. Test "on" and "off" conditions.

FIGURE 21



1. Each output is tested seporotely.
2. The flip-flop is tested to ensure conformance to truth table.
3. Preset and clear are tested with $V_{in(clock)} = 0$.
4. All unused inputs are connected to worst case voltages.

FIGURE 22

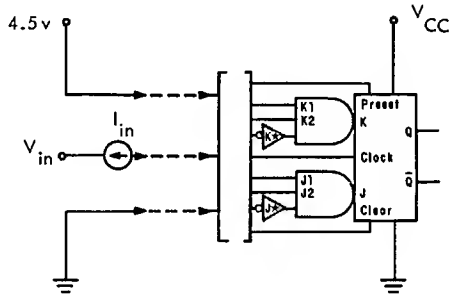


1. Each output is tested seporotely.

FIGURE 23

PARAMETER MEASUREMENT INFORMATION

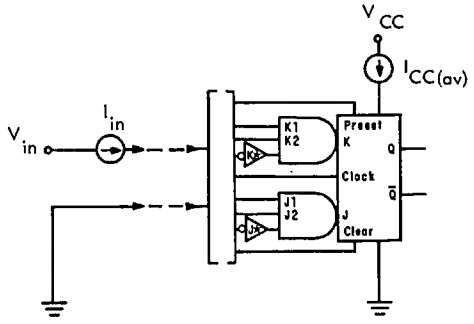
d-c test circuits (continued)



TEST TABLE		
Apply V_{in} (Test I_{in})	Apply 4.5 v	Ground
J2	J1	Cleor
J1	J2	Cleor
J★	None	None
K2	K1	Preset
K1	K2	Preset
K★	None	None
Clock	None	None
Preset	None	Clear
Cleor	None	Preset

1. Each input is tested separately.

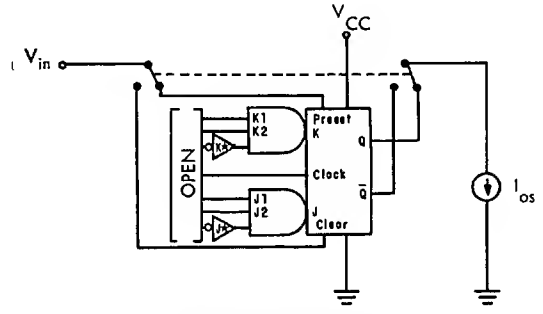
FIGURE 24



TEST TABLE (See Note 2)	
Apply V_{in} (Test I_{in})	Ground
J2	J1
J1	J2
J★	None
K2	K1
K1	K2
K★	None
Clock	None
Preset	(See Note 3)
Cleor	(See Note 3)

1. Each input is tested separately.
2. Test voltage and grounds are applied to inputs in accordance with the test table, and I_{in} is measured for input being tested.
3. A momentary ground is applied to preset or clear prior to applying V_{in} and testing I_{in} at these two inputs.

FIGURE 25

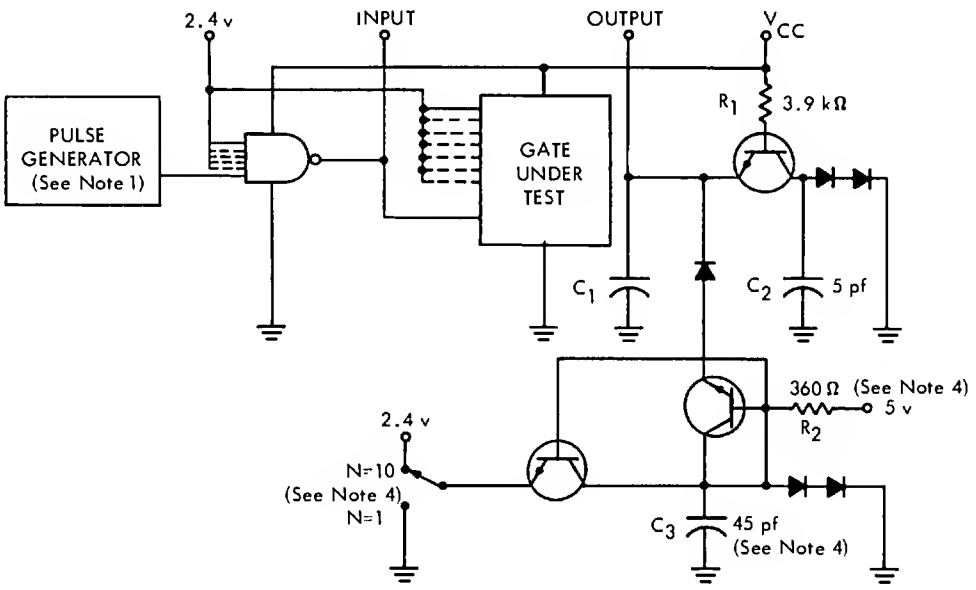


1. Each output is tested separately.

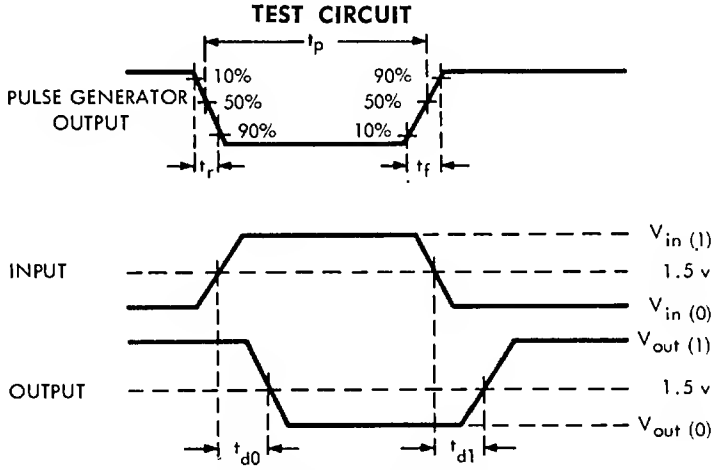
FIGURE 26

PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



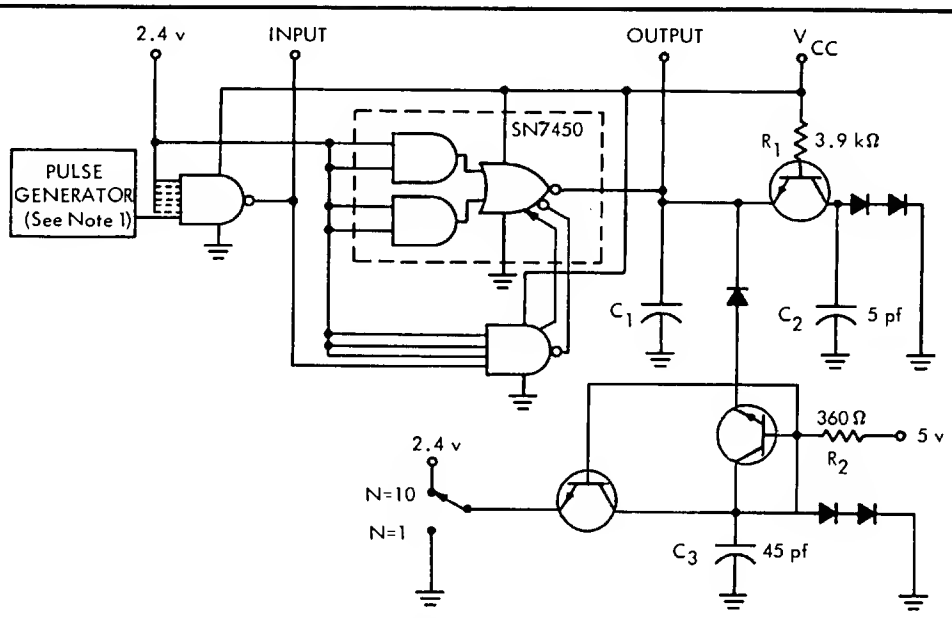
VOLTAGE WAVEFORMS

NOTES: 1. The generator has the following characteristics: $t_r = t_f \leq 15$ nsec, $t_p = 9.5$ μsec, PRR = 100 kc, $Z_{out} \approx 50$ Ω.
2. All transistors are 2N2368.
3. All diodes are 1N916.
4. Test SN7440 with $R_2 = 100$ Ω, $C_3 = 145$ pf, N = 30 for t_{d0}, and N = 1 for t_{d1}.
5. $t_{pd} = \frac{t_{d0} + t_{d1}}{2}$.

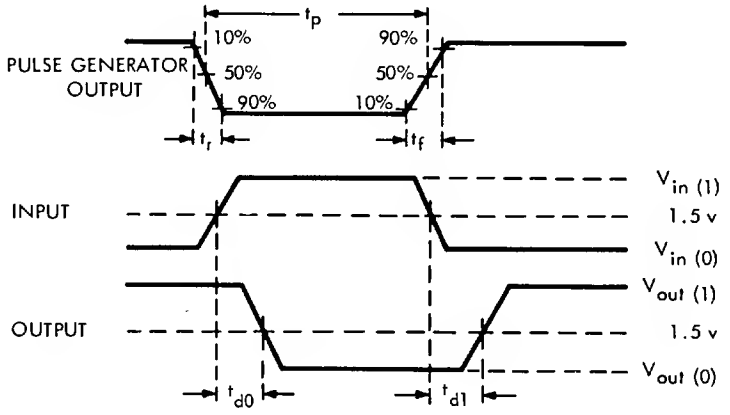
FIGURE 27 — GATE PROPAGATION DELAY

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



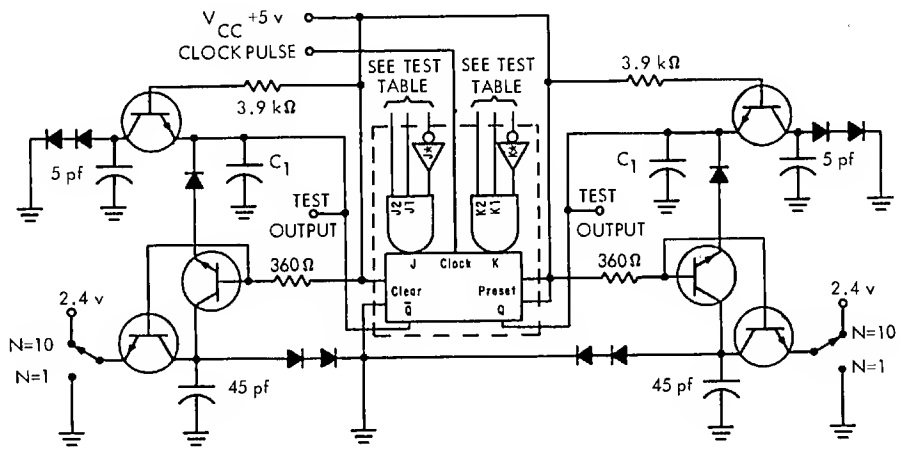
VOLTAGE WAVEFORMS

NOTES: 1. The generator has the following characteristics: $t_r = t_f \leq 15$ nsec, $t_p = 9.5$ μsec, PRR = 100 kc, $Z_{out} \approx 50\ \Omega$.
2. All transistors are 2N2368.
3. All diodes are 1N916.
4. $t_{pd} = \frac{t_{d0} + t_{d1}}{2}$

FIGURE 28 – EXPANDER PROPAGATION DELAY

PARAMETER MEASUREMENT INFORMATION

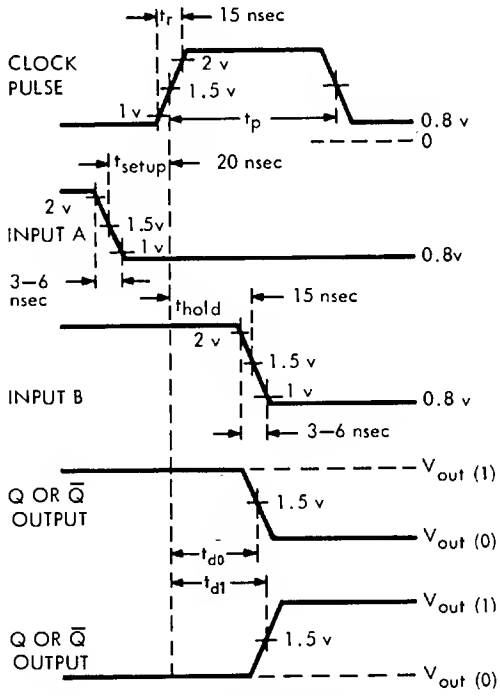
switching characteristics (continued)



TEST CIRCUIT

TEST TABLE					
TEST NO.	TEST	INPUT A	INPUT B	+2.4 v	GND
1	t_{d0} ($\bar{Q}$)	J★	J1, J2	K1, K2	K★
2	t_{d1} ($\bar{Q}$)	K★	K1, K2	J1, J2	J★
3	t_{d0} (Q)	K★	K1, K2	J1, J2	J★
4	t_{d1} (Q)	J★	J1, J2	K1, K2	K★

NOTES: 1. All transistors are 2N2368.
2. All diodes are 1N916.

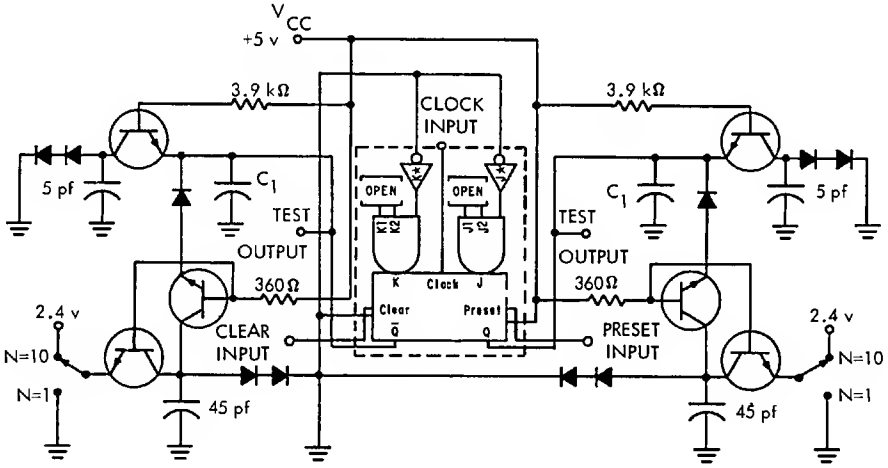


VOLTAGE WAVEFORMS

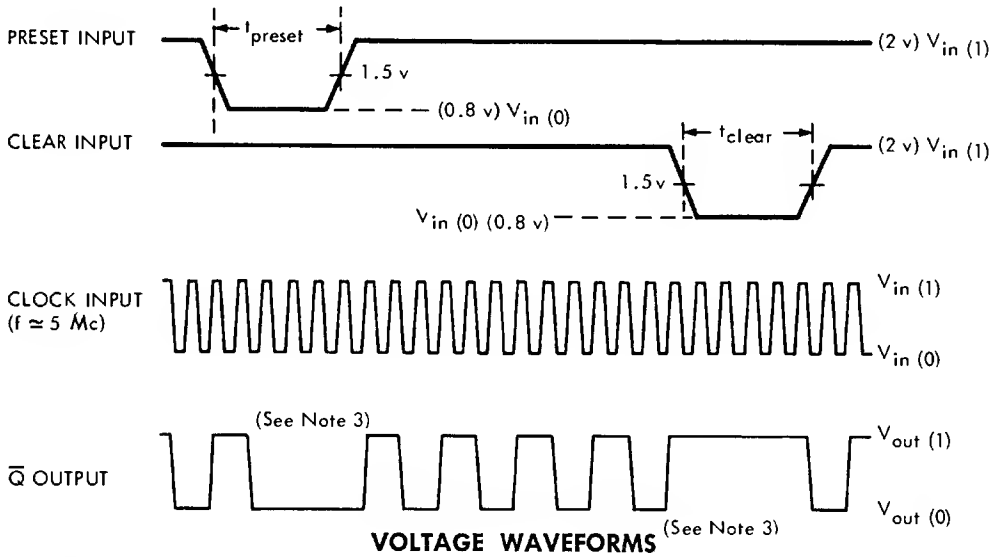
FIGURE 29 — FLIP-FLOP SWITCHING-TIME

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)



TEST CIRCUIT



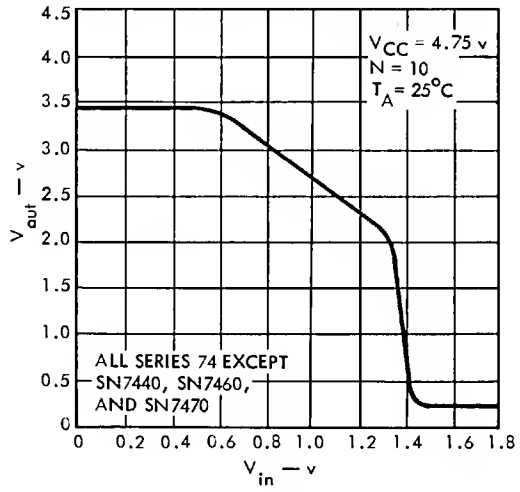
VOLTAGE WAVEFORMS

NOTES: 1. All transistors are 2N2368.
2. All diodes are 1N916.
3. Clock input of 5 Mc is used to verify that preset or clear input inhibits the clock function.

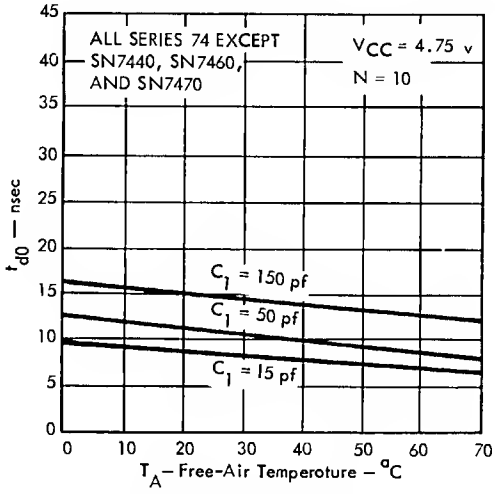
FIGURE 30 — PRESET/CLEAR TIME

TYPICAL CHARACTERISTICS

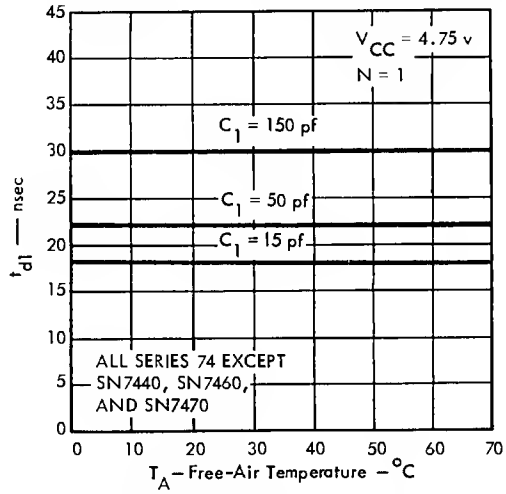
OUTPUT VOLTAGE vs INPUT VOLTAGE



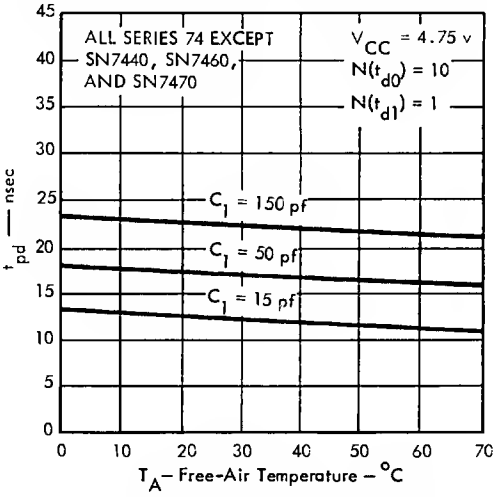
PROPAGATION TIME TO LOGICAL 0 vs TEMPERATURE



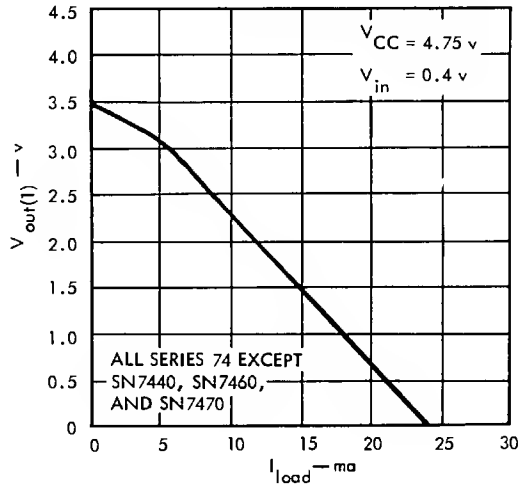
PROPAGATION TIME TO LOGICAL 1 vs TEMPERATURE



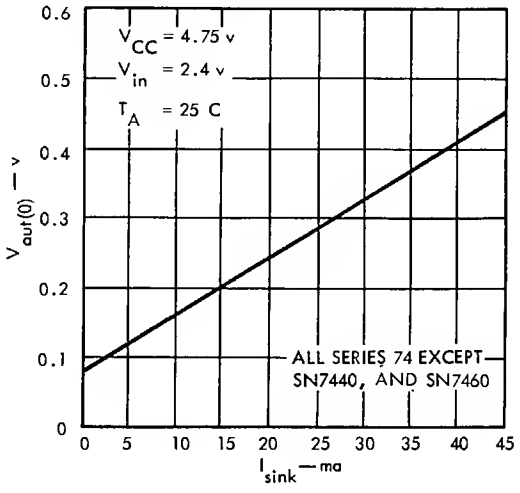
PROPAGATION DELAY TIME vs TEMPERATURE



OUTPUT VOLTAGE vs LOAD CURRENT



OUTPUT VOLTAGE vs SINK CURRENT

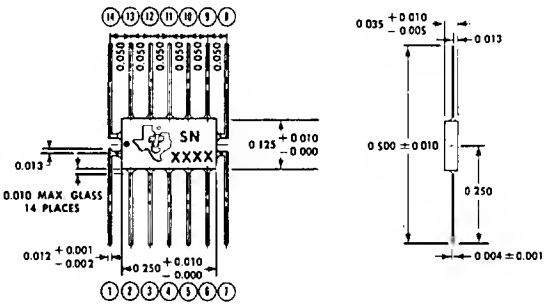


MECHANICAL DATA

general

SOLID CIRCUIT semiconductor netwarks are maunted in a glass-to-metal hermetically sealed, welded package. Package body and leads are gold-plated F-15‡ glass-sealing alloy. Approximate weight is 0.1 gram. All external surfaces are metallic and are insulated fram leads and circuit. All Series 74 netwarks are available with farmed leads, insulatar attached, and/ar mounted in a Mech-Pak carrier.

OUTLINE DRAWING — SEMICONDUCTOR NETWORK WELDED PACKAGE



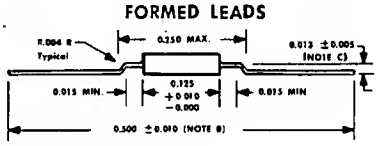
Falls Within TO-84 Dimensions

NOTES: a. All dimensians in inches.
b. All decimals ±0.005 except as noted.
c. Lead spacing talerance is ±0.015 at extremities and ±0.005 at package, nanaccumulative.
d. Lead centerlines are located within ±0.005 af their true positions relative to body centerlines.
e. Symbolizatian denates orientation of package.

leads

Gold-plated F-15‡ leads require na additianal cleaning ar processing when used in saldered ar welded assembly. Farmed leads are available ta facilitate planar mounting af netwarks an flat circuit baards. Standard lead length is 0.185 inches. Netwarks can be removed fram Mech-Pak carriers with lead lengths up ta 0.185 inches.

FORMED LEADS



NOTES: a. All dimensians in inches.
b. Nat applicable in Mech-Pak Carrier.
c. Measured fram center of lead to battam of package where lead emerges from body.

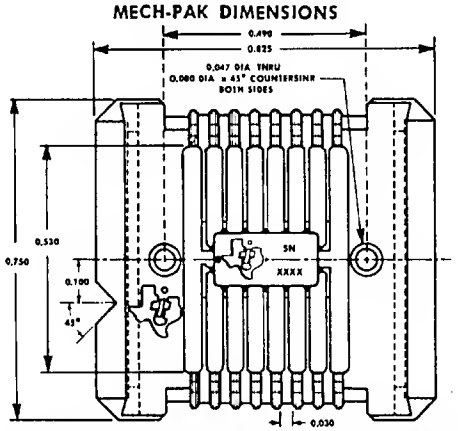
insulator

An insulator, secured ta the back surface af the package, permits maunting networks on circuit boards which have canductars passing beneath the package. The insulator is 0.0025 inches thick and has an insulatian resistance of 10 megahms at 25°C.

mech-pak carrier

The Mech-Pak carrier facilitates handling the network, and is campatible with autamatic equipment used for testing and assembly. The carrier is particularly appropriate far mechanized assembly operations and will withstand temperatures of 125°C for indefinite periads.

MECH-PAK DIMENSIONS



NOTES: 1. All dimensians are naminal in inches unless atherwise specified.
2. Overall thickness is 0.175 and nestled height is 0.150 each.

ordering instructions

Variatians in mechanical canfiguratian af semicanductar netwarks are identified by suffix numbers shown in a table at the right.

	NO MECH-PAK CARRIER				MECH-PAK CARRIER			
Lead Length	0.185 inch				Not Applicable			
Formed Leads	No	No	Yes	Yes	No	No	Yes	Yes
Insulators	No	Yes	No	Yes	No	Yes	No	Yes
Ordering Suffix	None	–6	–7	–1	–2	–3	–4	–5

†Patented by Texas Instruments Incorporated.

‡F-15 is the ASTM designation far an iran-nickel-cobalt alloy containing nominally 53% iron, 29% nickel, and 17% cobalt.

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