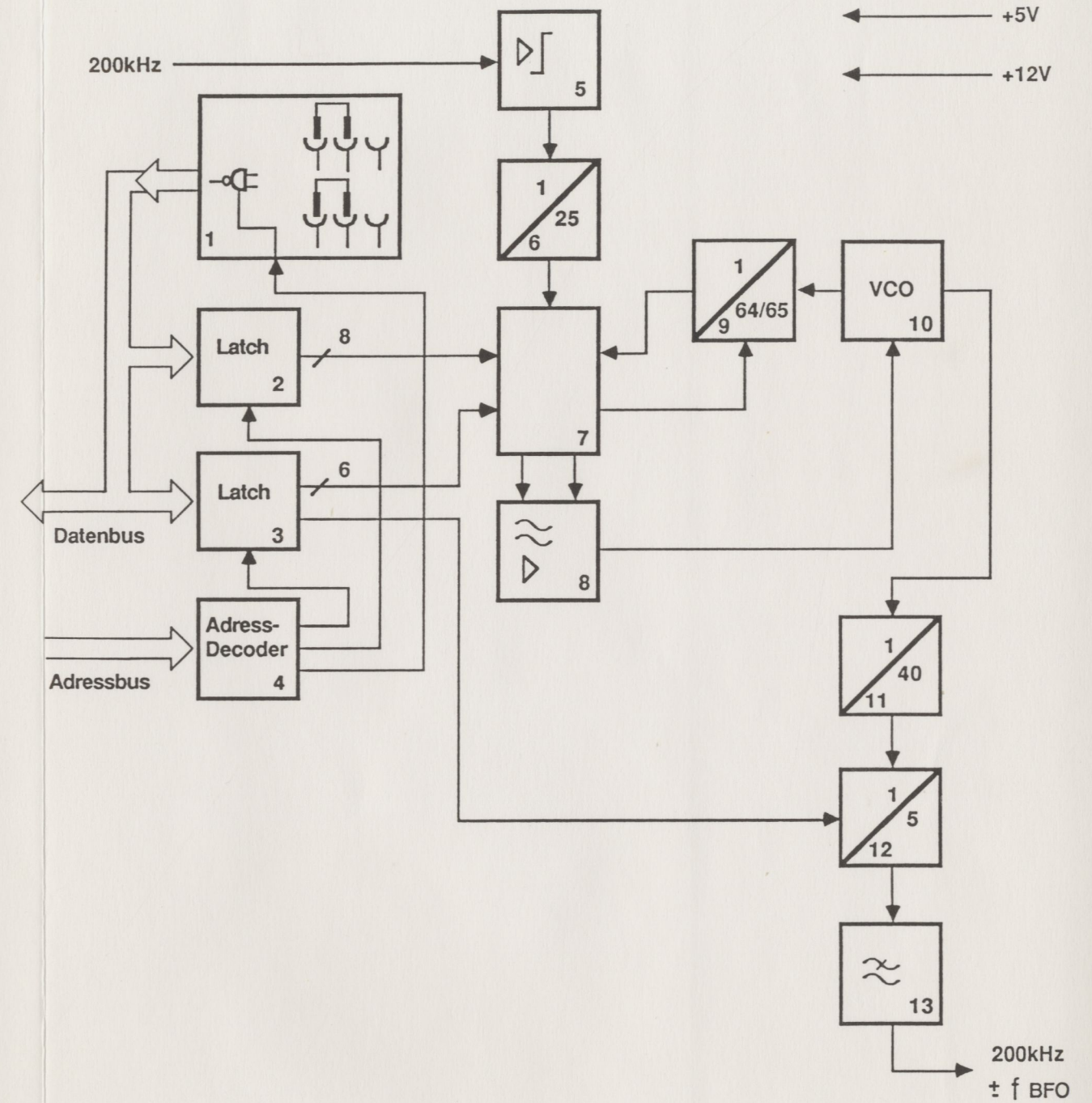
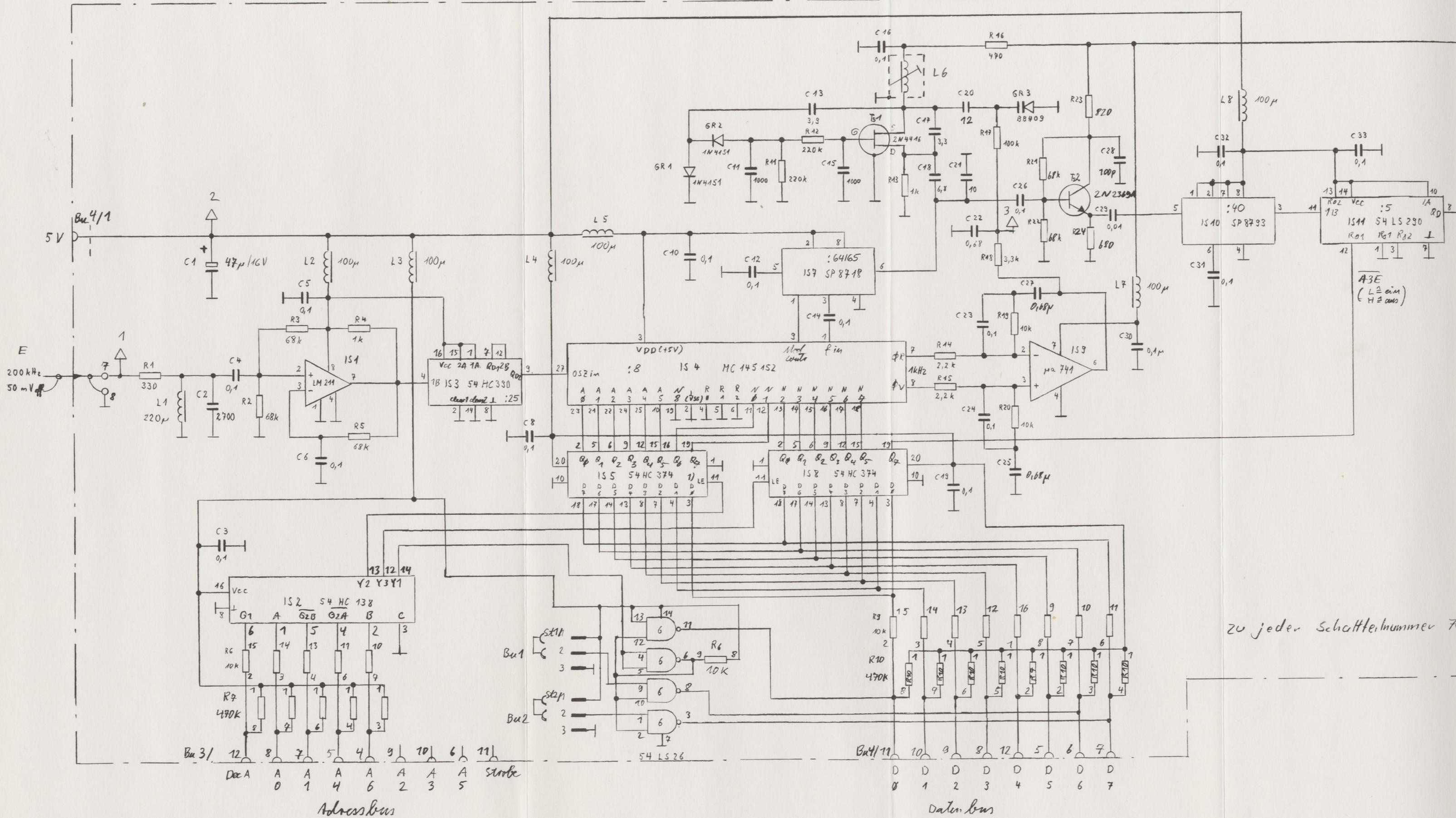
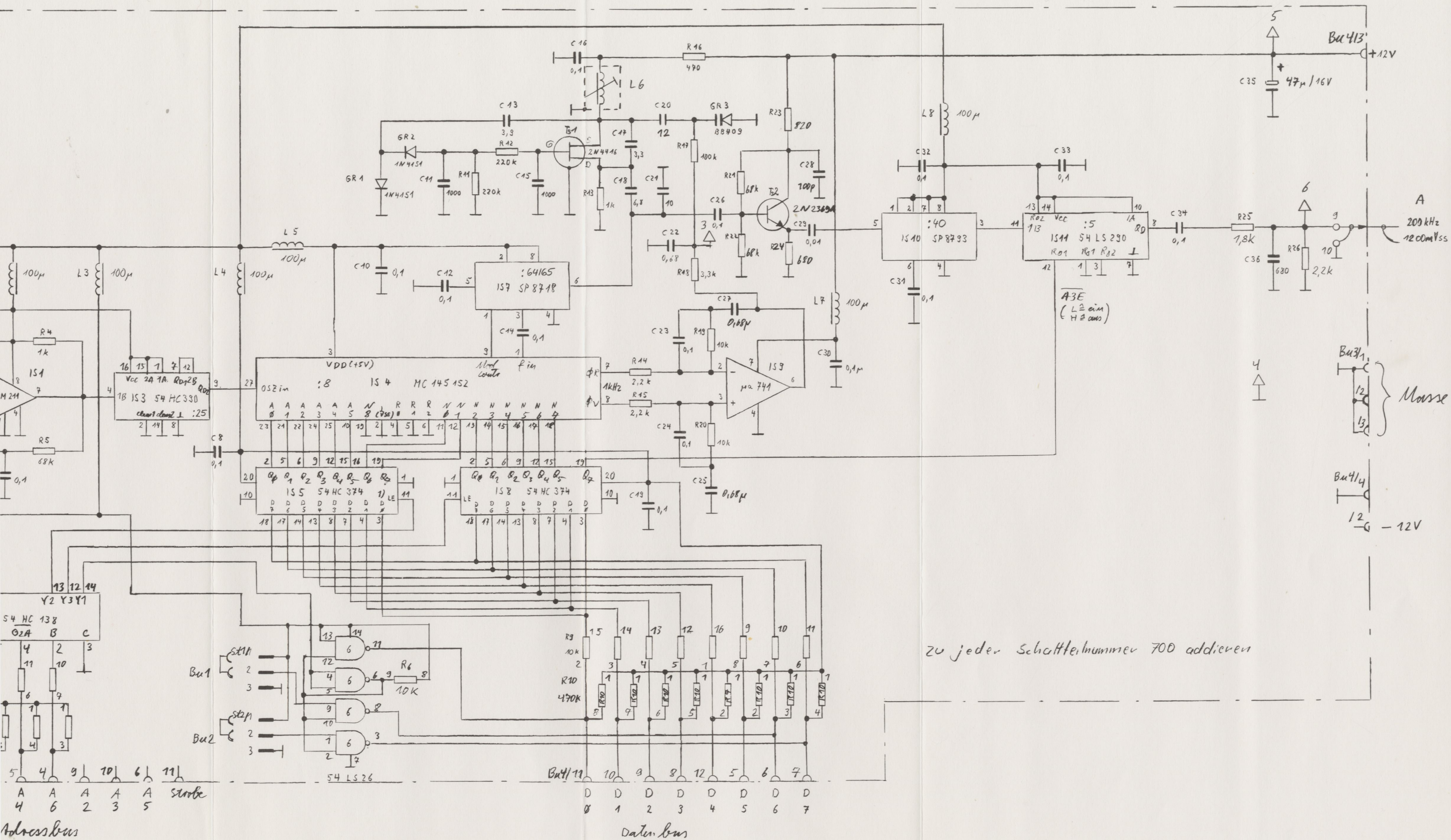


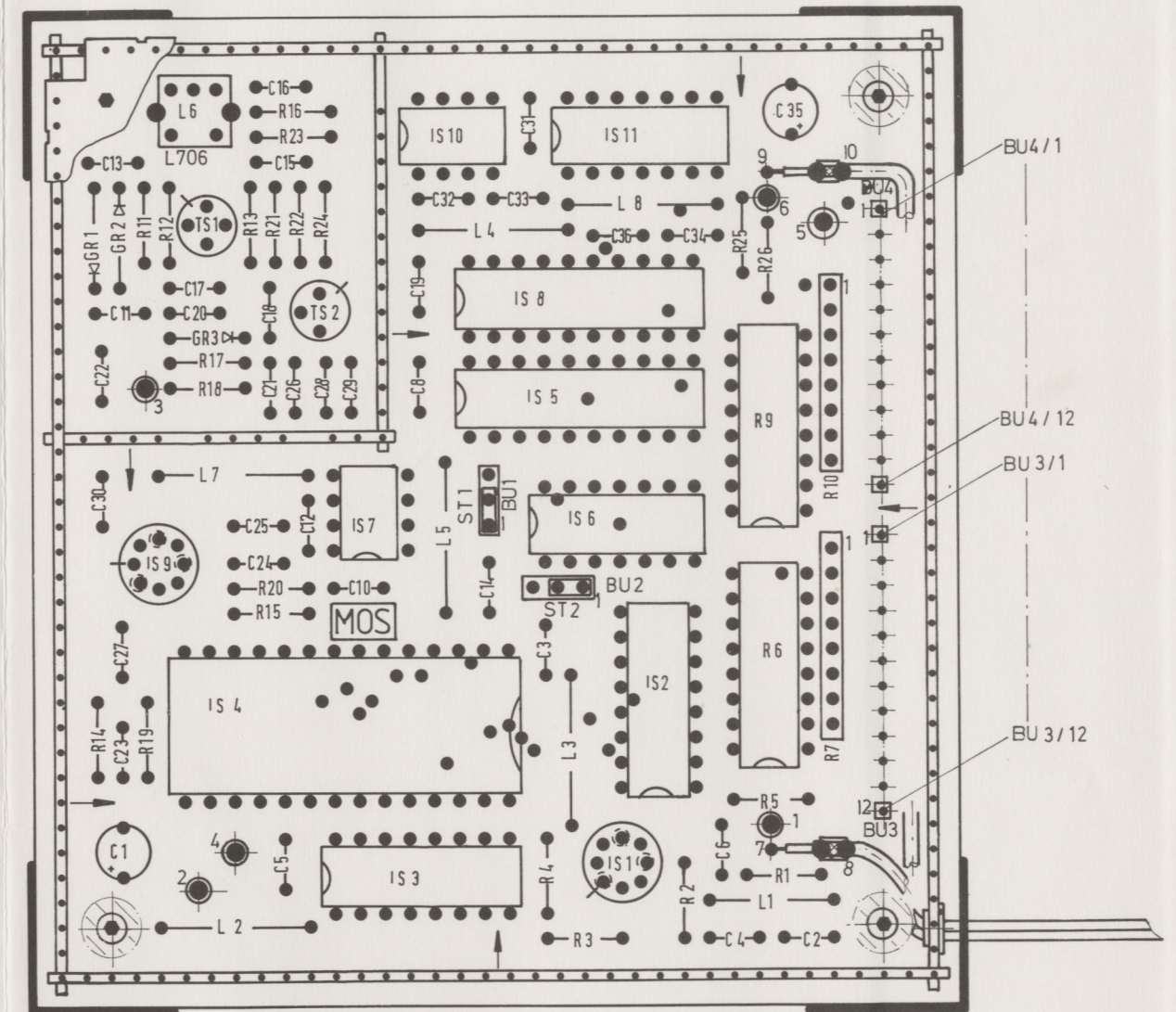
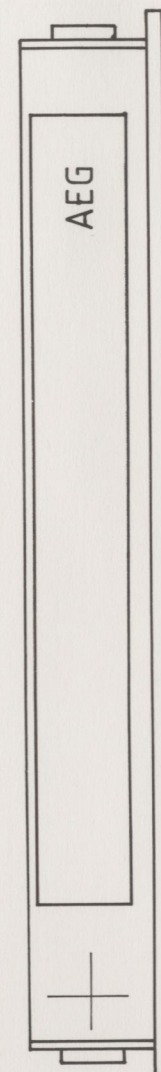
- 1 Open-collector-Gatter (für ausgehende Daten) mit Variantenstecker
- 2, 3 Latch (für eingehende Daten)
- 4 Adreßdecoder (für ein und aus)
- 5 Komparator
- 6 Teiler 1:25
- 7 PLL-Frequenz-Synthesizer (MC 145 152)
- 8 Loop-Filter (aktiv)
- 9 Umschaltbarer Teiler 1:64/65 (ECL)
- 10 VCO
- 11 Teiler 1:40 (ECL)
- 12 Teiler 1:5 (TTL), schaltbar
- 13 Tiefpaß (passiv)

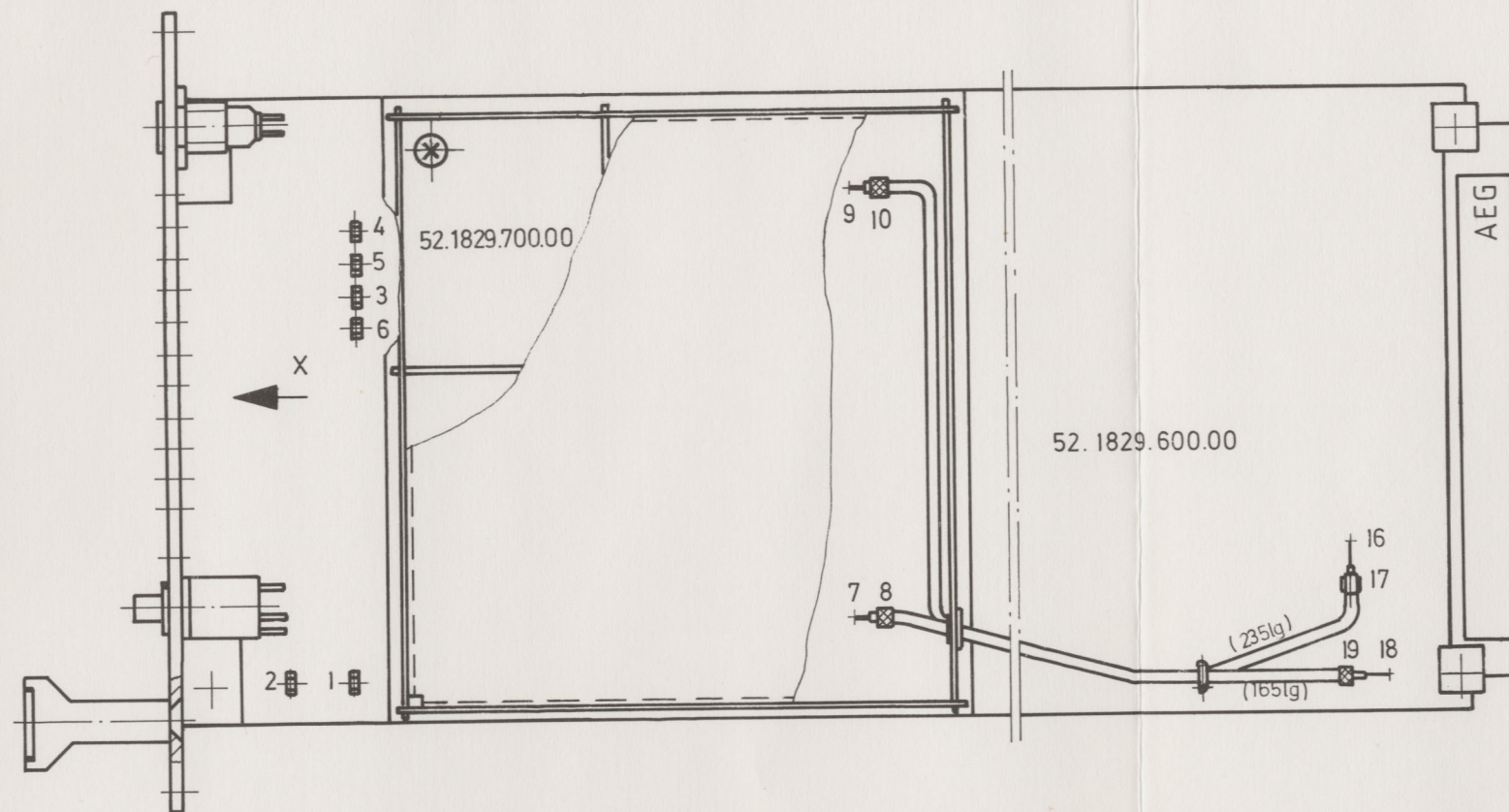
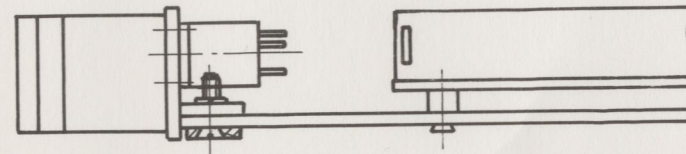






Stromlaufplan
Leiterkarte „Digitaler BFO“
Anlage 2





Ansicht X

