

### 1 General Description

The RDA5802/03 is a single-chip broadcast FM stereo radio tuner with fully integrated synthesizer, IF selectivity and MPX decoder. The tuner uses the CMOS process, support multi-interface and require the least external component. The package size is 4X4mm and is completely adjustment-free. All these make it very suitable for portable devices.

The RDA5802/03 has a powerful low-IF digital audio processor, this make it have optimum sound quality with varying reception conditions.

The RDA5802/03 can be tuned to the worldwide frequency band.

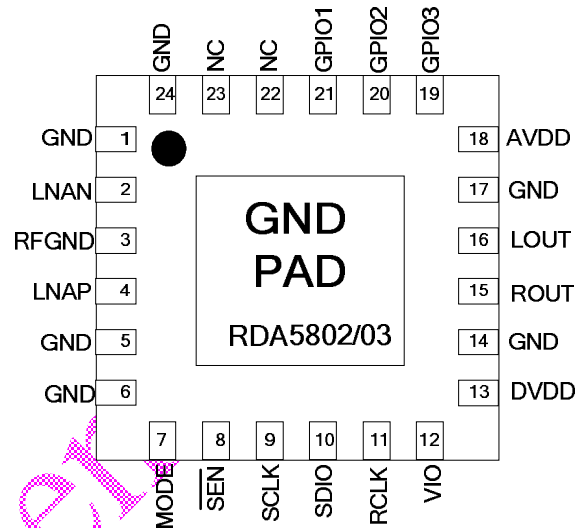


Figure 1-1. RDA5802/03 Top View

#### 1.1 Features

- I CMOS single-chip fully-integrated FM tuner
- I Low power consumption
  - Ø Total current consumption lower than 17mA at 3.0V power supply
- I Support worldwide frequency band
  - Ø 65 -108 MHz
- I Digital low-IF tuner
  - Ø Image-reject down-converter
  - Ø High performance A/D converter
  - Ø IF selectivity performed internally
- I Fully integrated digital frequency synthesizer
  - Ø Fully integrated on-chip RF and IF VCO
  - Ø Fully integrated on-chip loop filter
- I Autonomous search tuning
- I Support 32.768KHz crystal oscillator
- I Digital auto gain control (AGC)
- I Digital adaptive noise cancellation
  - Ø Mono/stereo switch
  - Ø Soft mute
  - Ø High cut
- I Programmable de-emphasis (50/75  $\mu$ s)
- I Receive signal strength indicator (RSSI)
- I Bass boost
- I volume control
- I I<sup>2</sup>S digital output interface
- I Line-level analog output voltage
- I 32.768 KHz 12M,24M,13M,26M,19.2M,38.4MHz Reference clock
- I 2-wire and 3-wire serial control bus interface
- I RDS/RBDS processor(RDA5803 only)
- I Directly support 32 $\Omega$  resistance loading
- I Integrated LDO regulator
  - Ø 2.7 to 5.5 V operation voltage
- I 4X4mm 24 pin QFN package

#### 1.2 Applications

- I Cellular handsets
- I MP3, MP4 players
- I Portable radios
- I PDAs, Notebook

*Confidential*

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### 3 Functional Description

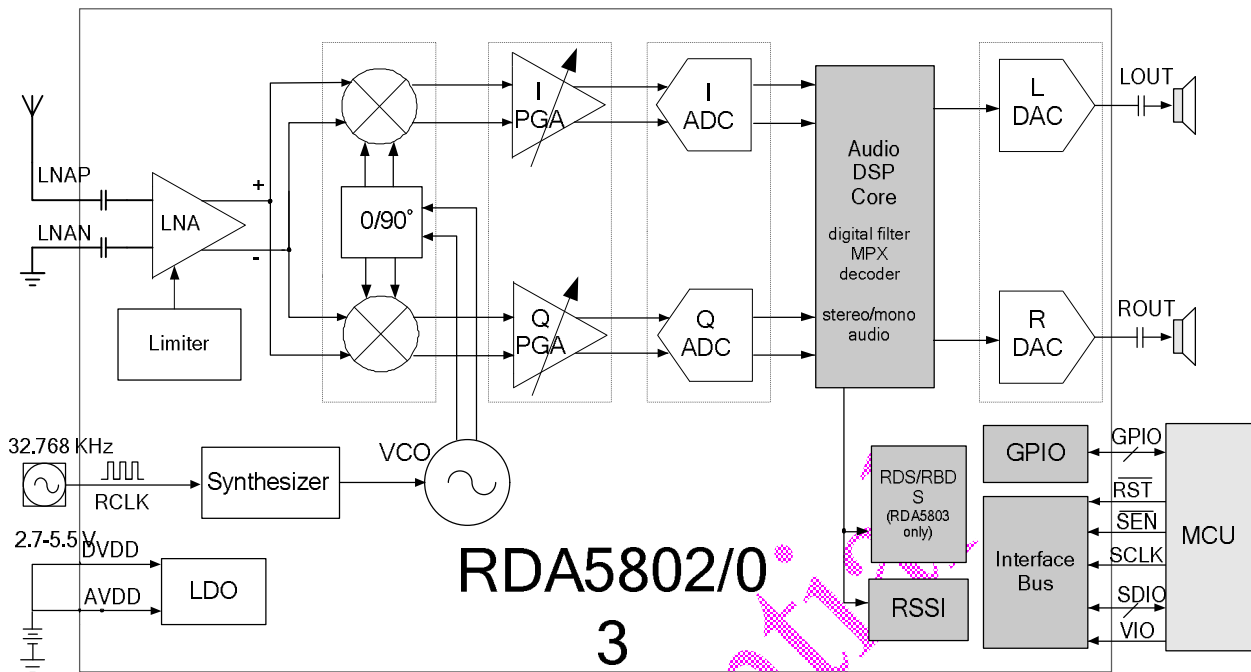


Figure 3-1. RDA5802/03 FM Tuner Block Diagram

#### 3.1 FM Receiver

The receiver uses a digital low-IF architecture that avoids the difficulties associated with direct conversion while delivering lower solution cost and reduces complexity, and integrates a low noise amplifier (LNA) supporting the FM broadcast band (65 to 108MHz), a quadrature image-reject mixer, a programmable gain control (PGA), a high resolution analog-to-digital converters (ADCs), an audio DSP and a high-fidelity digital-to-analog converters (DACs).

The LNA has differential input ports (LNAP and LNaN) and supports any input port by set according registers bits (LNA\_PORT\_SEL[1:0]). Its default input common mode voltage is GND.

The limiter prevents overloading and limits the amount of intermodulation products created by strong adjacent channels.

The quadrature mixer down converts the LNA output differential RF signal to low-IF, it also has image-reject function.

The PGA amplifies the mixer output IF signal and then digitized with ADCs.

The DSP core finishes the channel selection, FM demodulation, stereo MPX decoder and output audio signal. The MPX decoder can autonomous switch from stereo to mono to limit the output noise.

The DACs convert digital audio signal to analog and change the volume at same time. The DACs has low-pass feature and -3dB frequency is about 30 KHz.

#### 3.2 Synthesizer

The frequency synthesizer generates the local oscillator signal which divide to quadrature, then be used to downconvert the RF input to a constant low intermediate frequency (IF). The synthesizer reference clock is 32.768 KHz.

The synthesizer frequency is defined by bits CHAN[9:0] with the range from 65MHz to 108MHz.

#### 3.3 Power Supply

The RDA5802/03 integrated one LDO which supplies power to the chip. The external supply

voltage range is 2.7-5.5 V.

### 3.4 RESET and Control Interface select

The RDA5802/03 is RESET itself When VIO is Power up. And also support soft reset by trigger 02H BIT1 from 0 to 1. The control interface is select by MODE Pin. The MODE Pin is low ,I2C Interface is select. The MODE Pin is set to VIO, SPI Interface is select.

### 3.5 Control Interface

The RDA5802/03 supports three- wire and I<sup>2</sup>C control interface. User could select either of them to program the chip.

The three-wire interface is a standard SPI interface. It includes three pins: SEN, SCLK and SDIO. Each register write is 25-bit long, including 4-bit high register address, a r/w bit, 4-bit low register address, and 16-bit data (MSB is the first bit). RDA5802/03 samples command byte and data at posedge of SCLK. Each register read is also 25-bit long, including 4-bit high register address, a r/w bit, 4-bit low register address, and 16-bit data (MSB is the first bit) from RDA5802/03. The turn around cycle between command byte from MCU and data from RDA5802/03 is a half cycle. RDA5802/03 samples command byte at posedge of SCLK, and output data also at posedge of SCLK.

The I<sup>2</sup>C interface is compliant to I<sup>2</sup>C Bus Specification 2.1. It includes two pins: SCLK and SDIO. A I<sup>2</sup>C interface transfer begins with START condition, a command byte and data bytes, each byte has a followed ACK (or NACK) bit, and ends with STOP condition. The command byte includes a 7-bit chip address (0010000b) and a R/W bit. The ACK (or NACK) is always sent out by receiver. When in write transfer, data bytes is written out from MCU, and when in read transfer, data bytes is read out from RDA5802/03. There is no visible register address in I<sup>2</sup>C interface transfers. The I<sup>2</sup>C interface has a fixed start register address (0x02h for write transfer and 0x0Ah for read transfer), and an internal incremental address counter. If register address meets the end of register file, 0x3Ah, register address will wrap back to 0x00h. For write transfer, MCU programs registers from register 0x02h high byte, then register 0x02h low byte, then register 0x03h high byte, till the last register. RDA5802/03 always gives out ACK after every byte, and MCU gives out STOP condition when register programming is finished. For read transfer,

after command byte from MCU, RDA5802/03 sends out register 0x0Ah high byte, then register 0x0Ah low byte, then register 0x0Bh high byte, till receives NACK from MCU. MCU gives out ACK for data bytes besides last data byte. MCU gives out NACK for last data byte, and then RDA5802/03 will return the bus to MCU, and MCU will give out STOP condition.

Details refer to *RDA5802/03 Programming Guide*.

### 3.6 I<sup>2</sup>S Audio Data Interface

The RDA5802/03 supports I<sup>2</sup>S (Inter-IC Sound Bus) audio interface. The interface is fully compliant with I<sup>2</sup>S bus specification. When setting I2SEN bit high, RDA5802/03 will output SCK, WS, SD signals from GPIO3, GPIO1, GPIO2 as I<sup>2</sup>S master and transmitter, the sample rate is 48Kbps, 44.1kbps,32kbps..... RDA5802/03 also support as I<sup>2</sup>S slaver mode and transmitter, the sample rate is less than 100kbps.

Details refer to *RDA5802/03 Programming Guide*.

### 3.7 RDS/RBDS Processor(RDA5803 only)

The RDA5803 implements an RDS/RBDS processor for symbol decoding, block synchronization, error detection, and error correction. The RDA5803 device is user configurable and provides an optional interrupt when RDS is synchronized, loses synchronization, and/or the user configurable RDS FIFO threshold has been met.

Details refer to *RDA5802/03 Programming Guide*.

### 3.8 GPIO Outputs

The RDA5802/03 has three GPIOs. The function of GPIOs could programmed with bits GPIO1[1:0], GPIO2[1:0], GPIO3[1:0] and I2SEN.

If I2SEN is set to low, GPIO pins could be programmed to output low or high or high-Z, or be programmed to output interrupt and stereo indicator with bits GPIO1[1:0], GPIO2[1:0], GPIO3[1:0]. GPIO2 could be programmed to output a low interrupt (interrupt will be generated only with interrupt enable bit STCIEN is set to high) when seek/tune process completes. GPIO3 could be programmed to output stereo indicator bit ST.

Constant low, high or high-Z functionality is available regardless of the state of VA and VD supplies or the ENABLE bit.

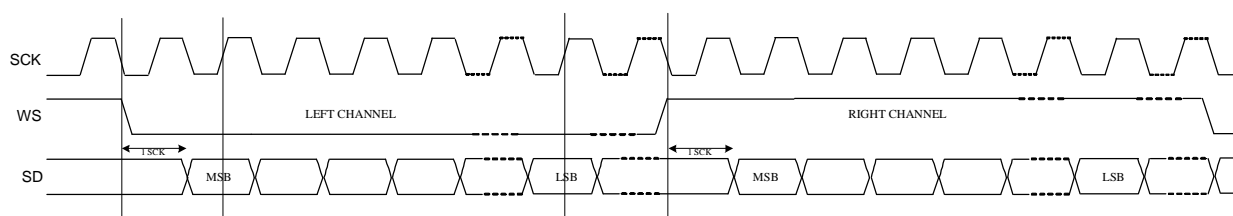


Figure 3-2. I2S Digital Audio Format

## 4 Electrical Characteristics

**Table 4-1 DC Electrical Specification (Recommended Operation Conditions):**

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
AVDD	Analog Supply Voltage	2.7	3.3	5.5	V
DVDD	Digital Supply Voltage	2.7	3.3	5.5	V
VIO	Interface Supply Voltage	1.5	-	3.6	V
T <sub>amb</sub>	Ambient Temperature	-20	27	+70	°C
V <sub>IL</sub>	CMOS Low Level Input Voltage	0		0.3*DVDD	V
V <sub>IH</sub>	CMOS High Level Input Voltage	0.7*VDD		DVDD	V
V <sub>TH</sub>	CMOS Threshold Voltage		0.5*VDD		V

**Table 4-2 DC Electrical Specification (Absolute Maximum Ratings):**

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
VIO	Interface Supply Voltage	-0.5		+4	V
T <sub>amb</sub>	Ambient Temperature	-40		+90	°C
I <sub>IN</sub>	Input Current <sup>(1)</sup>	-10		+10	mA
V <sub>IN</sub>	Input Voltage <sup>(1)</sup>	-0.3		VIO+0.3	V
V <sub>Ina</sub>	LNA FM Input Level			-20	dBm

Notes:

1. For Pin: SCLK, SDIO,  $\overline{SEN}$ , MODE

**Table 4-3 Power Consumption Specification**
(VDD = 2.7 to 5.5 V, T<sub>A</sub> = -25 to 85 °C, unless otherwise specified)

SYMBOL	DESCRIPTION	CONDITION	TYP	UNIT
I <sub>A</sub>	Analog Supply Current	ENABLE=1	13	mA
I <sub>D</sub>	Digital Supply Current	ENABLE=1	3	mA
I <sub>VIO</sub>	Interface Supply Current	SCLK and RCLK inactive	65	μA
I <sub>APD</sub>	Analog Powerdown Current	ENABLE=0	2	μA
I <sub>DPD</sub>	Digital Powerdown Current	ENABLE=0	2	μA
I <sub>VIO</sub>	Interface Powerdown Current	ENABLE=0	35	μA

## 5 Receiver Characteristics

**Table 5-1 Receiver Characteristics**

 (VDD = 2.7 to 5.5 V, T<sub>A</sub> = -25 to 85 °C, unless otherwise specified)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
<b>General specifications</b>						
F <sub>in</sub>	FM Input Frequency	BAND=00	87		108	MHz
		BAND=01	76		91	MHz
		BAND=10	76		108	MHz
		BAND=11	65		76	MHz
V <sub>rf</sub>	Sensitivity <sup>1,2,3</sup>	(S+N)/N=26dB		1.6	2	μV EMF
	RDS Sensitivity	Δf = 2 kHz, RDS BLER < 5%		15		μV EMF
R <sub>in</sub>	LNA Input Resistance <sup>7</sup>			150		Ω
C <sub>in</sub>	LNA Input Capacitance <sup>7</sup>		2	4	6	pF
IP3 <sub>in</sub>	Input IP3 <sup>4</sup>	AGCD=1	80		-	dBμV
α <sub>am</sub>	AM Suppression <sup>1,2</sup>	m=0.3	40	-	-	dB
S <sub>200</sub>	Adjacent Channel Selectivity	±200KHz	45		-	dB
V <sub>AFL</sub> ; V <sub>AFR</sub>	Left and Right Audio Frequency Output Voltage (Pins LOUT and ROUT)	Volume [3:0]=1111		110		mV
(S+N)/N	Maximum Signal Plus Noise to Noise Ratio <sup>1,2,3,5</sup>		54	60	-	dB
α <sub>SCS</sub>	Stereo Channel Separation		35	-	-	dB
THD	Audio Total Harmonic Distortion <sup>1,3,6</sup>			0.05	0.1	%
α <sub>AOI</sub>	Audio Output L/R Imbalance				0.1	dB
R <sub>L</sub>	Audio Output Loading Resistance	Single-ended	32	-	-	Ω
<b>Pins L<sub>NAN</sub>, L<sub>NAP</sub>, L<sub>OUT</sub>, R<sub>OUT</sub> and NC(22,23)</b>						
V <sub>com_rfin</sub>	Pins L <sub>NAN</sub> and L <sub>NAP</sub> Input Common Mode Voltage			Floating		V
V <sub>com</sub>	Audio Output Common Mode Voltage <sup>8</sup>		1.2	1.25	1.3	V
V <sub>com_nc</sub>	Pins NC (22, 23) Common Mode Voltage		0.45	0.5	0.55	V
<b>! The NC(22, 23) pins SHOULD BE left floating.</b>						

**Notes:**

- F<sub>in</sub>=65 to 108MHz; F<sub>mod</sub>=1KHz; de-emphasis=75μs; MONO=1; L=R unless noted otherwise;
- Δf=22.5KHz;
- B<sub>AF</sub> = 300Hz to 15KHz, RBW <=10Hz;
- |f<sub>2</sub>-f<sub>1</sub>|>1MHz, f<sub>0</sub>=2xf<sub>1</sub>-f<sub>2</sub>, AGC disable, F<sub>in</sub>=76 to 108MHz;
- P<sub>RF</sub>=60dBμV;
- Δf=75KHz.
- Measured at V<sub>EMF</sub> = 1 m V, f<sub>RF</sub> = 65 to 108MHz
- At LOUT and ROUT pins

## 6 Serial Interface

### 6.1 Three-wire Interface Timing

**Table 6-1 Three-wire Interface Timing Characteristics**

(VDD = 2.7 to 5.5 V, T<sub>A</sub> = -25 to 85 °C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
SCLK Cycle Time	t <sub>CLK</sub>		35			ns
SCLK Rise Time	t <sub>R</sub>				50	ns
SCLK Fall Time	t <sub>F</sub>				50	ns
SCLK High Time	t <sub>HI</sub>		10			ns
SCLK Low Time	t <sub>LO</sub>		10			ns
SDIO Input, $\overline{\text{SEN}}$ to SCLK $\uparrow$ Setup	t <sub>s</sub>		10	-	-	ns
SDIO Input, to SCLK $\uparrow$ Hold	t <sub>h</sub>		10	-	-	ns
SCLK $\uparrow$ to SDIO Output Valid	t <sub>cdv</sub>	Read	2	-	10	ns
$\overline{\text{SEN}}\uparrow$ to SDIO Output High Z	t <sub>sdz</sub>	Read	2	-	10	ns
Digital Input Pin Capacitance					5	pF

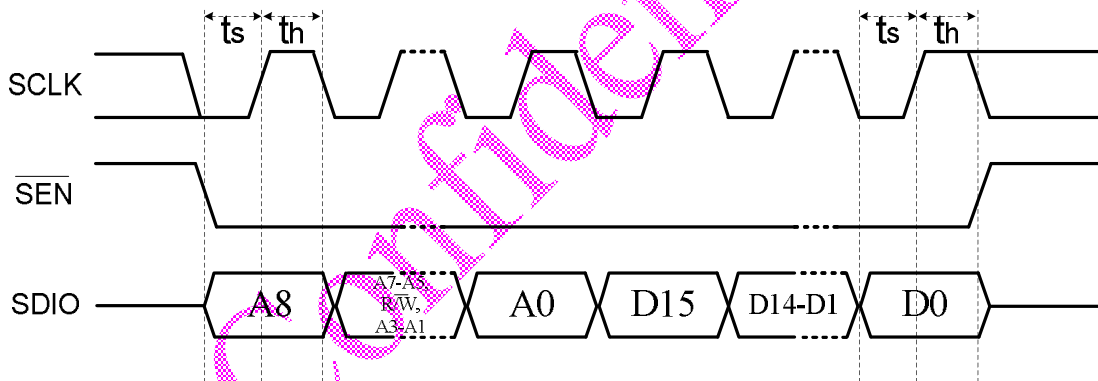


Figure 6-1. Three-wire Interface Write Timing Diagram

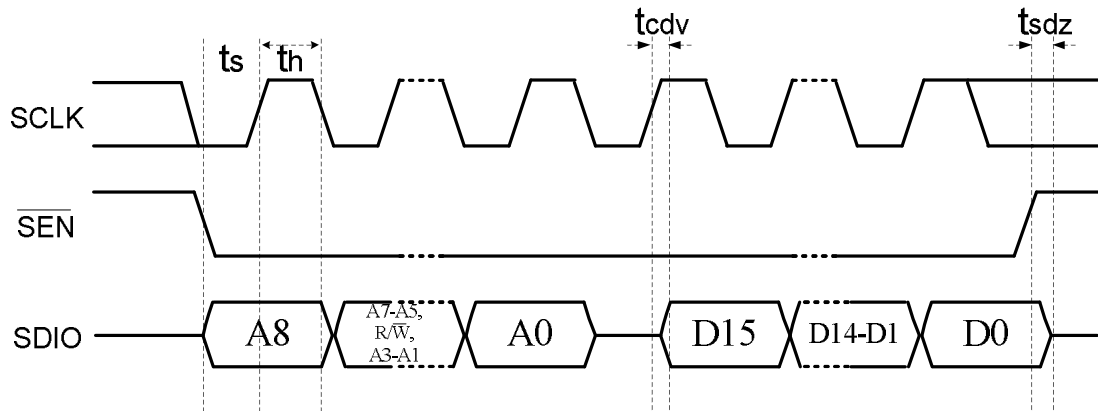


Figure 6-2. Three-wire Interface Read Timing Diagram



### 6.2 I<sup>2</sup>C Interface Timing

**Table 6-2 I<sup>2</sup>C Interface Timing Characteristics**

(VDD = 2.7 to 5.5 V, T<sub>A</sub> = -25 to 85 °C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
SCLK Frequency	f <sub>scl</sub>		0	-	400	KHz
SCLK High Time	t <sub>high</sub>		0.6	-	-	μs
SCLK Low Time	t <sub>low</sub>		1.3	-	-	μs
Setup Time for START Condition	t <sub>su:sta</sub>		0.6	-	-	μs
Hold Time for START Condition	t <sub>hd:sta</sub>		0.6	-	-	μs
Setup Time for STOP Condition	t <sub>su:sto</sub>		0.6	-	-	μs
SDIO Input to SCLK↑ Setup	t <sub>su:dat</sub>		100	-	-	ns
SDIO Input to SCLK↓ Hold	t <sub>hd:dat</sub>		0	-	900	ns
STOP to START Time	t <sub>buf</sub>		1.3	-	-	μs
SDIO Output Fall Time	t <sub>f:out</sub>		20+0.1C <sub>b</sub>	-	250	ns
SDIO Input, SCLK Rise/Fall Time	t <sub>r:in</sub> / t <sub>f:in</sub>		20+0.1C <sub>b</sub>	-	300	ns
Input Spike Suppression	t <sub>sp</sub>		-	-	50	ns
SCLK, SDIO Capacitive Loading	C <sub>b</sub>		-	-	50	pF
Digital Input Pin Capacitance					5	pF

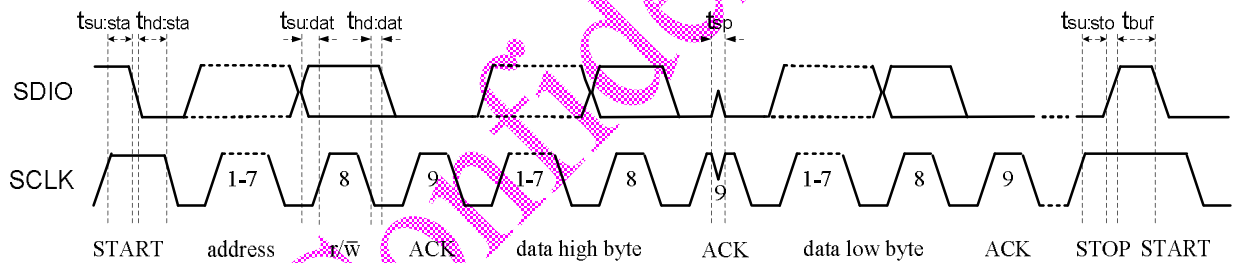


Figure 6-3. I<sup>2</sup>C Interface Write Timing Diagram

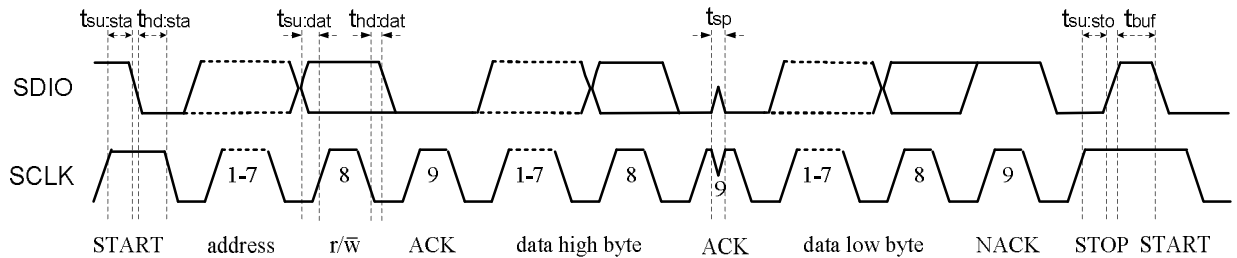


Figure 6-4. I<sup>2</sup>C Interface Read Timing Diagram

## 7 Register Definition

REG	BITS	NAME	FUNCTION	DEFAULT
00H	15:8	CHIPID[7:0]	Chip ID.	0x58
02H	15	DHIZ	Audio Output High-Z Disable. <i>0 = High impedance; 1 = Normal operation</i>	0
	14	DMUTE	Mute Disable. <i>0 = Mute; 1 = Normal operation</i>	0
	13	MONO	Mono Select. <i>0 = Stereo; 1 = Force mono</i>	0
	12	BASS	Bass Boost. <i>0 = Disabled; 1 = Bass boost enabled</i>	0
	9	SEEKUP	Seek Up. <i>0 = Seek down; 1 = Seek up</i>	0
	8	SEEK	Seek. <i>0 = Disable stop seek; 1 = Enable</i> <i>Seek begins in the direction specified by SEEKUP and ends when a channel is found with RSSI level above SEEKTH[5:0], or the entire band has been searched.</i> <i>The SEEK bit is set low and the STC bit is set high when the seek operation completes.</i>	0
	7	SKMODE	Seek Mode <i>0 = wrap at the upper or lower band limit and continue seeking</i> <i>1 = stop seeking at the upper or lower band limit</i>	0
	6:4	CLK_MODE[2:0]	000=32.768kHz 001=12Mhz 101=24Mhz 010=13Mhz 110=26Mhz 011=19.2Mhz 111=38.4Mhz	000
	3	RDS_EN(RDA5803 only)	RDS Enable <i>0 = Disabled</i> <i>1 = Enable</i>	0
	1	SOFT_RESET	Soft reset. If 0, not reset; If 1, reset.	0
	0	ENABLE	Power Up Enable. <i>0 = Disabled; 1 = Enabled</i>	0
03H	15:6	CHAN[9:0]	Channel Select. BAND = 0 Frequency = <i>Channel Spacing (kHz) x CHAN + 87.0 MHz</i> BAND = 1 or 2 Frequency =	0x00

REG	BITS	NAME	FUNCTION	DEFAULT
			$Channel\ Spacing\ (kHz) \times CHAN + 76.0\ MHz$ <b>BAND = 3</b> Frequency = $Channel\ Spacing\ (kHz) \times CHAN + 65.0\ MHz$ <b>CHAN is updated after a seek operation.</b>	
	4	TUNE	Tune 0 = Disable 1 = Enable The tune operation begins when the TUNE bit is set high. The STC bit is set high when the tune operation completes. The tune bit is reset to low automatically when the tune operation completes..	0
	3:2	BAND[1:0]	Band Select. 00 = 87–108 MHz (US/Europe) 01 = 76–91 MHz (Japan) 10 = 76–108 MHz (world wide) 11 = 65 –76 MHz (East Europe)	00
	1:0	SPACE[1:0]	Channel Spacing. 00 = 100 kHz 01 = 200 kHz 10 = 50kHz	00
04H	15	RDSIEN(RDA5803 only)	RDS Interrupt Enable 0 = Disable Interrupt(Default) 1 = Enable Interrupt Setting RDSIEN = 1 and GPIO2[1:0] = 01 will generate a low pulse int on GPIO2 when the RDSR 0Ah[15] bit is set.	0
	14	STCIEN	Seek/Tune Complete Interrupt Enable. 0 = Disable Interrupt 1 = Enable Interrupt Setting STCIEN = 1 will generate a low pulse on GPIO2 when the interrupt occurs.	0
	13	RBDS(RDA5803 only)	1=rlds 0=rds	0
	11	DE	De-emphasis. 0 = 75 $\mu$ s; 1 = 50 $\mu$ s	0
	10	RDSR _MODE (RDA5803 only)	0 = RDSR width fixed 40 ms high 1 = read reg0CH clr RDSR	1
	9	SOFTMUTE_EN	If 1, softmute enable	1
	8	AFCD	AFC disable. If 0, afc work; If 1, afc disabled.	0
	6	I2S_ENABLED	I2S bus enable	0

REG	BITS	NAME	FUNCTION	DEFAULT
			If 0, disabled; If 1, enabled.	
	5:4	GPIO3[1:0]	General Purpose I/O 3. 00 = High impedance 01 = Mono/Stereo indicator (ST) 10 = Low 11 = High	00
	3:2	GPIO2[1:0]	General Purpose I/O 2. 00 = High impedance 01 = Interrupt (INT) 10 = Low 11 = High	00
	1:0	GPIO1[1:0]	General Purpose I/O 1. 00 = High impedance 01 = Reserved 10 = Low 11 = High	00
05H	15	INT_MODE	If 0, generate 5ms interrupt; If 1, interrupt last until read reg0CH action occurs.	1
	14:8	SEEKTH[6:0]	Seek Threshold. RSSI scale is logarithmic. 0000000 = min RSSI	0001000
	7:6	LNA_PORT_SEL[1:0]	LNA input port selection bit: 00: no input 01: LNA1 10: LNA2 11: dual port input	10
	5:4	LNA_ICSEL_BIT[1:0]	Lna working current bit: 00=1.8mA 01=2.1mA 10=2.5mA 11=3.0mA	10
	3:0	VOLUME[3:0]	DAC Gain Control Bits (Volume). 0000=min; 1111=max Volume scale is logarithmic	1010
06H	12	I2s_mode_select	If 0, master mode; If 1, slave mode.	0
	7:4	I2s_ws_cnt[4:0] Only valid in master mode	4'b1000: WS_STEP=48; 4'b0111: WS_STEP=44.1kbps; 4'b0110: WS_STEP=32kbps; 4'b0101: WS_STEP=24kbps; 4'b0100: WS_STEP=22.05kbps; 4'b0011: WS_STEP=16kbps; 4'b0010: WS_STEP=12kbps; 4'b0001: WS_STEP=11.025kbps; 4'b0000: WS_STEP=8kbps;	0000
0AH	15	RDSR (RDA5803 only)	RDS ready 0 = No RDS/RBDS group ready 1 = New RDS/RBDS group ready	0
	14	STC	Seek/Tune Complete. 0 = Not complete	0

REG	BITS	NAME	FUNCTION	DEFAULT
			1 = Complete The seek/tune complete flag is set when the seek or tune operation completes.	
	13	SF	Seek Fail. 0 = Seek successful; 1 = Seek failure The seek fail flag is set when the seek operation fails to find a channel with an RSSI level greater than SEEKTH[5:0].	0
	12	RDSS (RDA5803 only)	RDS Synchronization 0=RDS decoder not synchronized(default) 1 = RDS decoder synchronized Available only in RDS Verbose mode	0
	10	ST	Stereo Indicator. 0 = Mono; 1 = Stereo Stereo indication is available on GPIO3 by setting GPIO1[1:0] =01.	1
	9:0	READCHAN[9:0]	Read Channel. BAND = 0 Frequency = Channel Spacing (kHz) x READCHAN[9:0]+ 87.0 MHz BAND = 1 or 2 Frequency = Channel Spacing (kHz) x READCHAN[9:0]+ 76.0 MHz BAND = 3 Frequency = Channel Spacing (kHz) x READCHAN[9:0]+ 65.0 MHz READCHAN[9:0] is updated after a tune or seek operation.	8'h00
0BH	15:9	RSSI[6:0]	RSSI. 000000 = min 111111 = max RSSI scale is logarithmic.	0
	8	FM TRUE	1 = the current channel is a station 0 = the current channel is not a station	0
	7	FM_READY	1=ready 0=not ready	0
	4	ABCD_E (RDA5803 only)	1 = the block id of register 0cH,0dH,0eH,0fH is E 0 = the block id of register 0cH,0dH,0eH,0fH is A,B,C,D	0
	3:2	BLERA[1:0] (RDA5803 only)	BLK Errors Level of RDS_DATA_0, and is always read as Errors Level of RDS BLOCK A( in RDS mode) or BLOCK E(in RBDS mode when ABCD_E flag is 1). 00 = 0 errors requiring correction 01 = 1~2 errors requiring correction 10 = 3~5 errors requiring correction	00

REG	BITS	NAME	FUNCTION	DEFAULT
			11 = 6+ errors or error in checkword, correctionnot possible Available only in RDS Verbose mode	
	1:0	BLERB[1:0] (RDA5803 only)	BLK Errors Level of RDS_DATA_1, and is always read as Errors Level of RDS BLOCK B( in RDS mode) or E(in RBDS mode when ABCD_E flag is 1). 00 = 0 errors requiring correction 01 = 1~2 errors requiring correction 10 = 3~5 errors requiring correction 11 = 6+ errors or error in checkword, correctionnot possible Available only in RDS Verbose mode	00
0CH	15:0	RDSA[15:0] (RDA5803 only)	BLOCK A (in RDS mode) or BLOCK E(in RBDS mode when ABCD_E flag is 1)	0
0DH	15:0	RDSB[15:0] (RDA5803 only)	BLOCK B (in RDS mode) or BLOCK E(in RBDS mode when ABCD_E flag is 1)	0
0EH	15:0	RDESC[15:0] (RDA5803 only)	BLOCK C/c' (in RDS mode) or BLOCK E(in RBDS mode when ABCD_E flag is 1)	0
0FH	15:0	RDS D[15:0] (RDA5803 only)	BLOCK D (in RDS mode) or BLOCK E(in RBDS mode when ABCD_E flag is 1)	0
10H	15:14	BLERC[1:0] (RDA5803 only)	BLK Errors Level of RDS_DATA_2, and is always read as Errors Level of RDS BLOCK C/c'( in RDS mode) or BLOCK E(in RBDS mdoe when ABCD_E flag is 1). 00 = 0 errors requiring correction 01 = 1~2 errors requiring correction 10 = 3~5 errors requiring correction 11 = 6+ errors or error in checkword, correctionnot possible Available only in RDS Verbose mode	00
	13:12	BLERD[1:0] (RDA5803 only)	BLK Errors Level of RDS_DATA_3, and is always read as Errors Level of RDS BLOCK D( in RDS mode) or BLOCK E(in RBDS mdoe when ABCD_E flag is 1). 00 = 0 errors requiring correction 01 = 1~2 errors requiring correction 10 = 3~5 errors requiring correction 11 = 6+ errors or error in checkword, correctionnot possible Available only in RDS Verbose mode	00

## 8 Pins Description

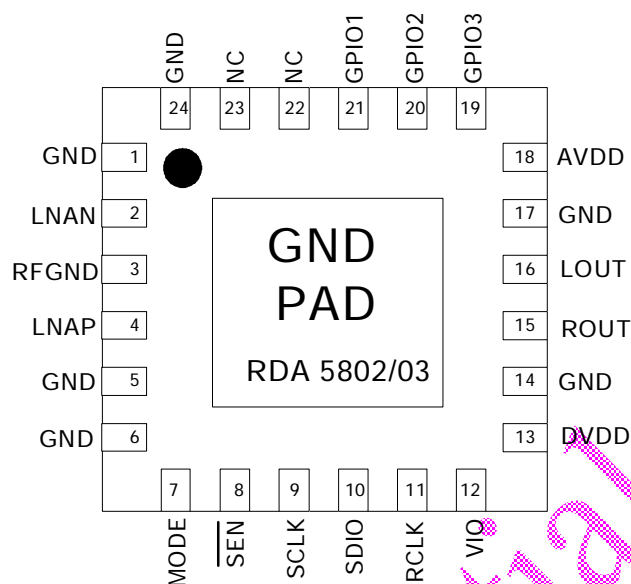


Figure 8-1. RDA5802/03 Top View

Table 8-1 RDA5802 Pins Description

SYMBOL	PIN	DESCRIPTION
GND	1,5,6,14,17,24	Ground. Connect to ground plane on PCB
LNaN,LNaP	2,4	LNA input port. For single-ended input, LNaN should be connected to RFGND
RFGND	3	LNA ground. Connect to ground plane on PCB
MODE	7	Control Interface select The MODE Pin is low ,I2C Interface is select. The MODE Pin is set to VIO, SPI Interface is select.
$\overline{SEN}$	8	Latch enable (active low) input for serial control bus
SCLK	9	Clock input for serial control bus
SDIO	10	Data input/output for serial control bus
RCLK	11	32.768KHz crystal oscillator and reference clock input
VIO	12	Power supply for I/O
AVDD	18	Power supply for analog section
ROUT,LOUt	15,16	Right/Left audio output
DVDD	14	Power supply for digital section
GPIO1,GPIO2,GPIO3	19,20,21	General purpose input/output
NC	22,23	No Connect

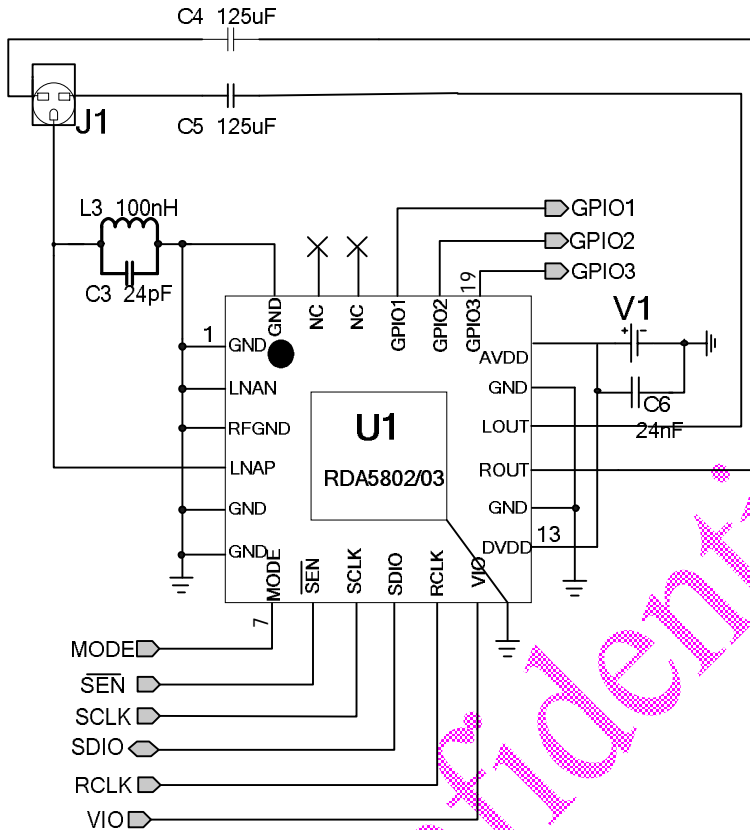
**Table 8-2 Internal Pin Configuration**

SYMBOL	PIN	DESCRIPTION
LNAN/LNAP	2/4	
RCLK	11	
SCLK/SDIO	9/10	
GPIO1/GPIO2/GPIO3	19/20/21	



## 9 Application Diagram

### 9.1 Audio Loading Resistance Larger than 32Ω & TCXO Application:



Notes:

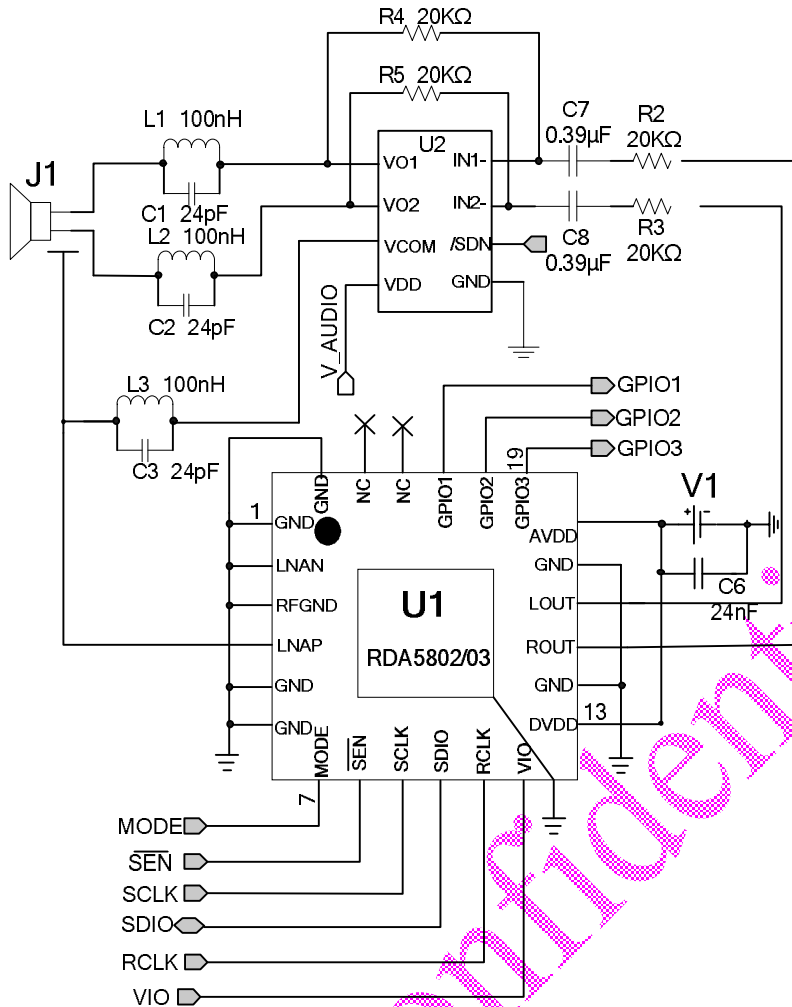
1. J1: Common 32Ω Resistance Headphone;
2. U1: RDA5802/03 Chip;
3. V1: Analog and Digital Power Supply (2.7~5.5V);
4. FM Choke (L3 and C3) for Audio Common and LNA Input Common;
5. Pins NC(22, 23), Should be Leaved Floating;
6. Set MODE to select control interface(GND—I2C,VIO—SPI);
6. Place C6 Close to AVDD pin.

Figure 9-1. RDA5802/03 FM Tuner Application Diagram (TCXO Application)

#### 9.1.1 Bill of Materials:

COMPONENT	VALUE	DESCRIPTION	SUPPLIER
U1	RDA5802/03	Broadcast FM Radio Tuner	RDA
J1		Common 32Ω Resistance Headphone	
L3/C3	100nH/24pF	LC Chock for LNA Input	Murata
C4,C5	125μF	Audio AC Couple Capacitors	Murata
C6	24nF	Power Supply Bypass Capacitor	Murata

**9.2 Audio Loading Resistance Lower than 32Ω & TCXO Application:**



**Notes:**

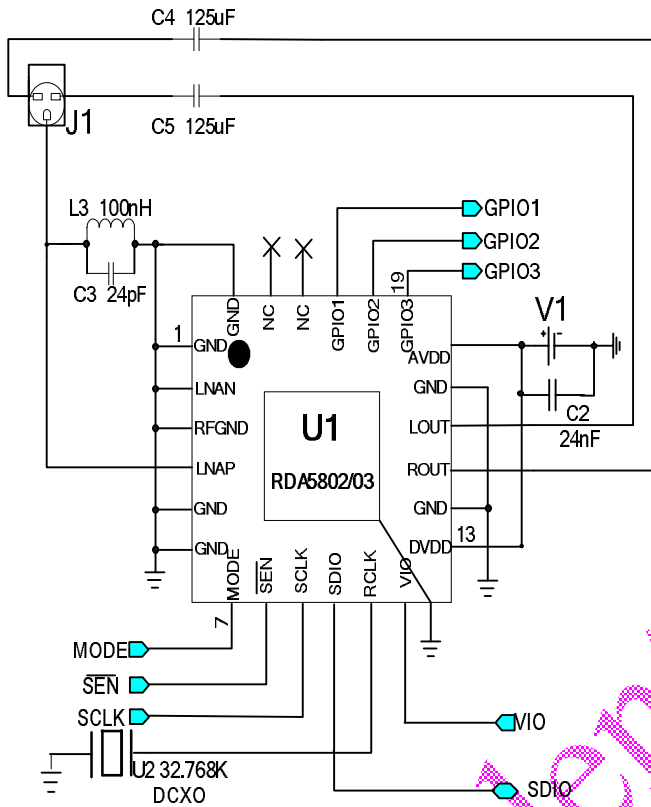
1. J1: Resistance Lower than 32Ω Audio Speaker or Headphone
2. U1: RDA5802/03 Chip
3. V1: Analog and Digital Power Supply (2.7~5.5V)
4. FM Choke (L3 and C3) for Audio Common and LNA Input Common
5. Pins NC(22, 23), Should be Leaved Floating;
6. Set MODE to select control interface(GND—I2C, VIO—SPI);
7. Place C6 Close to AVDD pin
8. Changing the Resistor R4 and R5 Value can Change the Output Volume.

Figure 9-2. RDA5802/03 FM Tuner Application Diagram (Audio Amplifier Application)

**9.2.1 Bill of Materials:**

COMPONENT	VALUE	DESCRIPTION	SUPPLIER
U1	RDA5802/03	Broadcast FM Radio Tuner	RDA
U2		Audio Amplifier	
J1		Audio Speaker	
L1/C1; L2/C2	100nH/24pF	LC Chock for Audio Output	Murata
L3/C3	100nH/24pF	LC Chock for LNA Input	Murata
C6	24nF	Power Supply Bypass Capacitor	Murata
R4,R5	20KΩ	Audio Amplifier Feedback Resistors	Murata
R2/C7; R3/C8	20KΩ/0.39μF	Audio High-passed Filter and Amplifier Input Resistors	Murata

**9.3 Audio Loading Resistance Larger than 32Ω & DCXO Application:**



**Notes:**

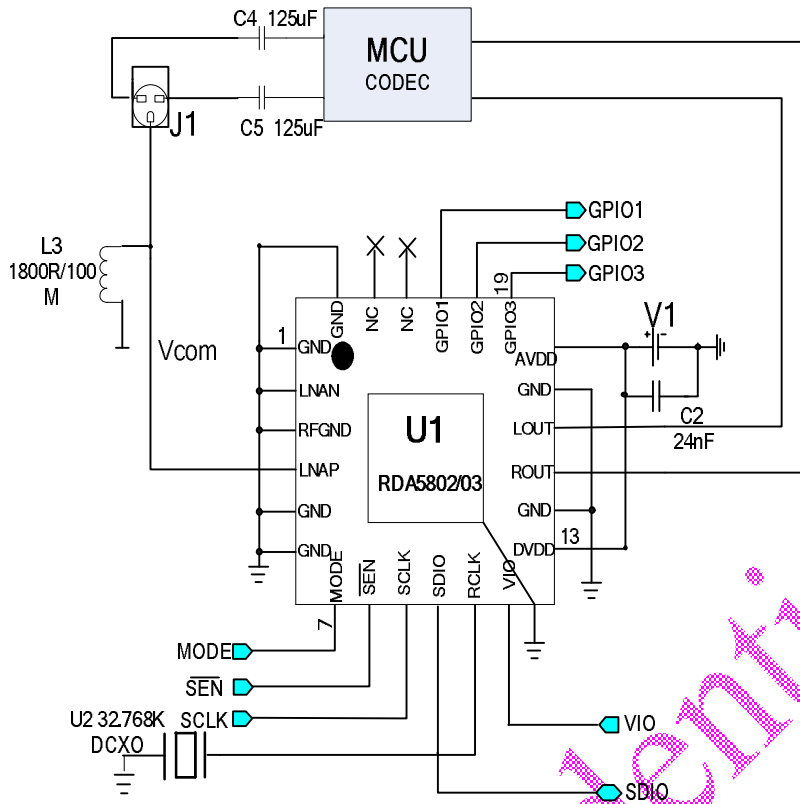
1. J1: Common 32Ω Resistance Headphone;
2. U1: RDA5802/03 Chip;
3. U2: 32.768KHz Crystal oscillator
4. V1: Analog and Digital Power Supply (2.7~5.5V);
5. FM Choke (L3 and C3) for Audio Common and LNA Input Common;
6. Pins NC(22, 23) Should be Leaved Floating;
7. Set MODE to select control interface(GND—I2C,VIO—SPI);
8. Place C6 Close to AVDD pin.
11. Place U2 Close to U1

Figure 9-3. RDA5802/03 FM Tuner Application Diagram (DCXO Application)

**9.3.1 Bill of Materials:**

COMPONENT	VALUE	DESCRIPTION	SUPPLIER
U1	RDA5802/03	Broadcast FM Radio Tuner	RDA
U2	DCXO	Crystal oscillator 32.768KHz	<=50PPM
J1		Common 32Ω Resistance Headphone	
L3/C3	100nH/24pF	LC Chock for LNA Input	Murata
C4,C5	125μF	Audio AC Couple Capacitors	Murata
C2	24nF	Power Supply Bypass Capacitor	Murata

9.4 MCU CODEC Application:



Notes:

1. J1: Common 32Ω Resistance Headphone;
2. U1: RDA5802/03 Chip;
3. U2: 32.768KHz Crystal oscillator
3. V1: Analog and Digital Power Supply (2.7~5.5V);
4. FM Choke L3 for LNA Input Common;
5. Pins NC(22, 23) Should be Leaved Floating;
6. Set MODE to select control interface(GND—I2C, VIO—SPI);
7. Place C6 Close to AVDD pin.
8. Place U2 Close to U1

Figure 9-4. RDA5802/03 FM Tuner Application Diagram (DCXO+MCU CODEC Application)

9.4.1 Bill of Materials:

COMPONENT	VALUE	DESCRIPTION	SUPPLIER
U1	RDA5802/03	Broadcast FM Radio Tuner	RDA
U2	DCXO	Crystal oscillator 32.768KHz	<=50PPM
J1		Common 32Ω Resistance Headphone	
L3	600R/100M	Common for LNA Input	Murata
C4,C5	125µF	Audio AC Couple Capacitors	Murata
C2	24nF	Power Supply Bypass Capacitor	Murata

### 10 Package Physical Dimension

Figure 10-1 illustrates the package details for the RDA5802. The package is lead-free and RoHS-compliant.

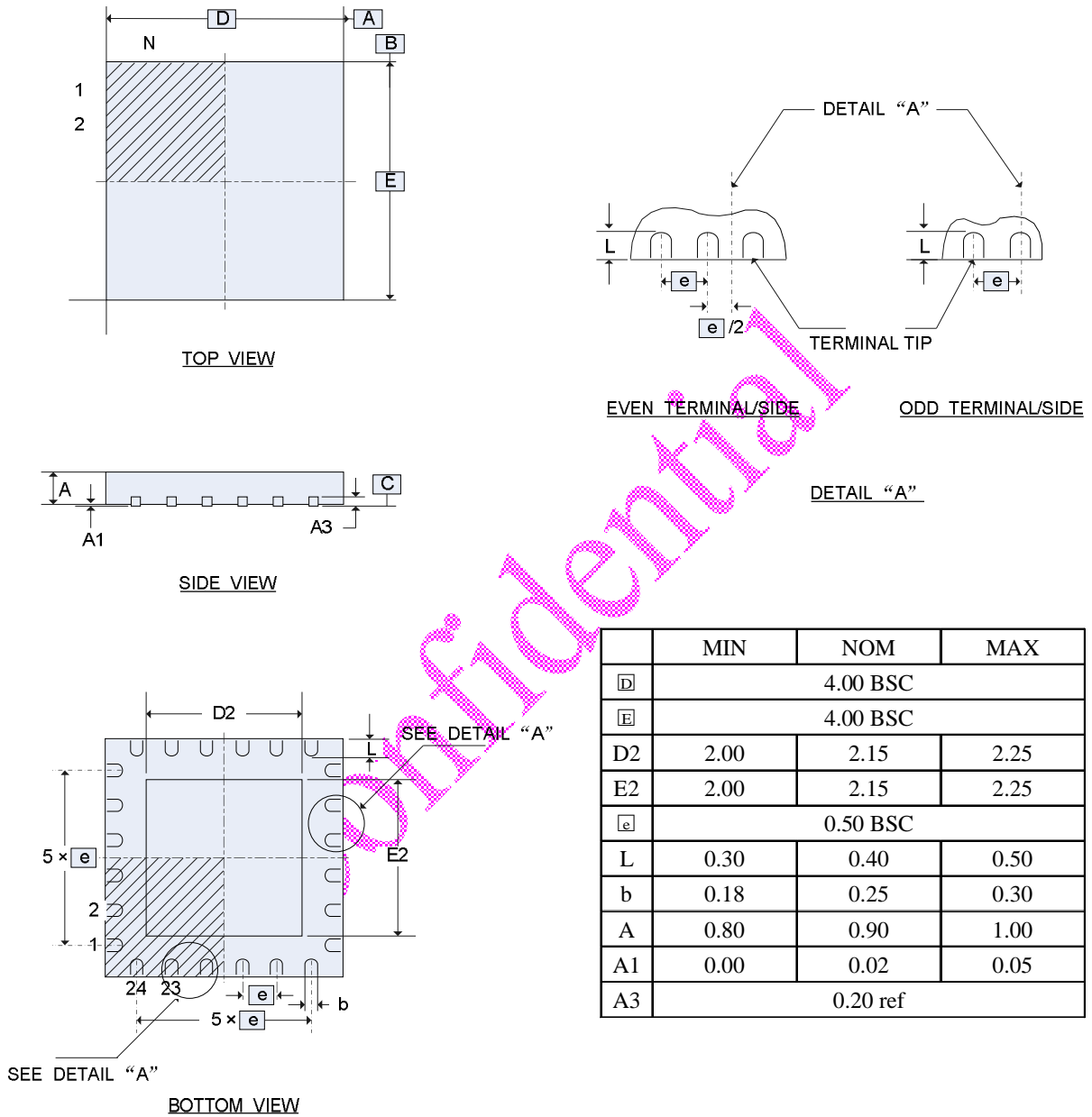


Figure 10-2. 24-Pin 4x4 Quad Flat No-Lead (QFN)

11 PCB Land Pattern

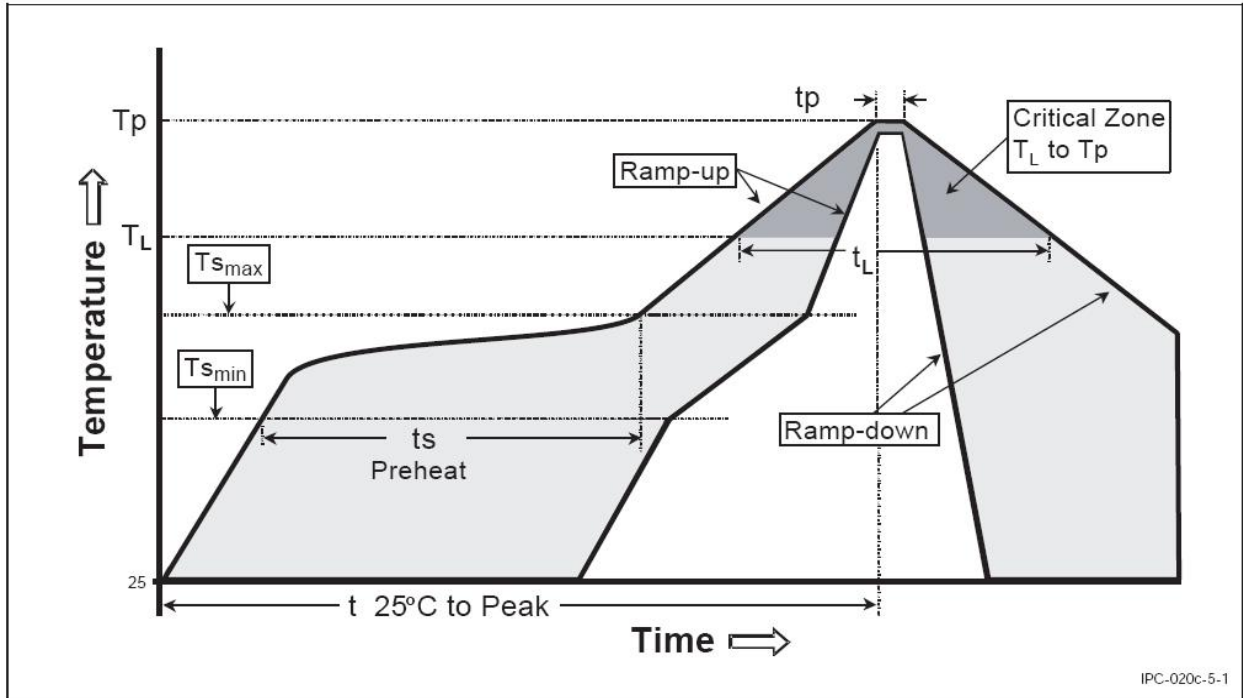


Figure 18. Classification Reflow Profile

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average Ramp-Up Rate ( $T_{smax}$ to $T_p$ )	3 °C/second max.	3 °C/second max.
<b>Preheat</b>		
-Temperature Min ( $T_{smin}$ )	100 °C	150 °C
-Temperature Max ( $T_{smax}$ )	100 °C	200 °C
-Time ( $t_{smin}$ to $t_{smax}$ )	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature ( $T_L$ )	183 °C	217°C
-Time ( $t_L$ )	60-150seconds	60-150 seconds
Peak /Classification Temperature( $T_p$ )	See Table-II	See Table-III
Time within 5 °C of actual Peak Temperature ( $t_p$ )	10-30 seconds	20-40 seconds
Ramp-Down Rate	6 °C/second max.	6 °C/seconds max.
Time 25 °C to Peak Temperature	6 minutes max.	8 minutes max.

Table-I Classification Reflow Profiles

Package Thickness	Volume mm <sup>3</sup> <350	Volume mm <sup>3</sup> ≥350
<2.5mm	240 + 0/-5 °C	225 + 0/-5 °C
≥2.5mm	225 + 0/-5 °C	225 + 0/-5 °C

**Table – II SnPb Eutectic Process – Package Peak Reflow Temperatures**

Package Thickness	Volume mm <sup>3</sup> <350	Volume mm <sup>3</sup> 350-2000	Volume mm <sup>3</sup> >2000
<1.6mm	260 + 0 °C *	260 + 0 °C *	260 + 0 °C *
1.6mm – 2.5mm	260 + 0 °C *	250 + 0 °C *	245 + 0 °C *
≥2.5mm	250 + 0 °C *	245 + 0 °C *	245 + 0 °C *

\*Tolerance : The device manufacturer/supplier **shall** assure process compatibility up to and including the stated classification temperature (this mean Peak reflow temperature + 0 °C. For example 260+ 0 °C ) at the rated MSL Level.

**Table – III Pb-free Process – Package Classification Reflow Temperatures**

- Note 1:** All temperature refer topside of the package. Measured on the package body surface.
- Note 2:** The profiling tolerance is + 0 °C, - X °C (based on machine variation capability) whatever is required to control the profile process but at no time will it exceed - 5 °C. The producer assures process compatibility at the peak reflow profile temperatures defined in Table –III.
- Note 3:** Package volume excludes external terminals(balls, bumps, lands, leads) and/or non integral heat sinks.
- Note 4:** The maximum component temperature reached during reflow depends on package the thickness and volume. The use of convection reflow processes reduces the thermal gradients between packages. However, thermal gradients due to differences in thermal mass of SMD package may still exist.
- Note 5:** Components intended for use in a “lead-free” assembly process **shall** be evaluated using the “lead free” classification temperatures and profiles defined in Table-I II III whether or not lead free.

## **RoHS Compliant**

The product does not contain lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB) or polybrominated diphenyl ethers (PBDE), and are therefore considered RoHS compliant.

## **ESD Sensitivity**

Integrated circuits are ESD sensitive and can be damaged by static electricity. Proper ESD techniques should be used when handling these devices.

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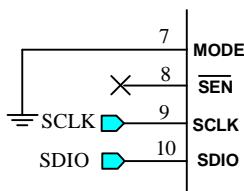


### 12 Change List

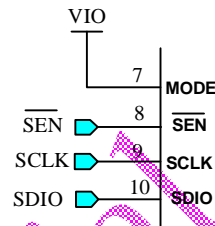
REV	DATE	AUTHER	CHANGE DESCRIPTION
V1.0	2008-03-07	ChunZhao,YananLiu,XiaoqiYou	Original Draft.
V2.0	2008-06-18	XiaoqiYou	Updata some test result

### 13 Notes:

1: 通过硬件电路设置芯片工作总线控制模式，详细电路如下图：



附图：I2C 总线电路接口电路



SPI 总线电路接口电路

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