SECTION 4

TECHNICAL DESCRIPTION

4.1 INTRODUCTION

The information in this section is in the following two broad categories:

- A general overview of RF-590 Receiver operation
- Specific electronic theory about circuits and/or concepts utilized in the RF-590

Included in the general receiver overview are the following items:

- Receiver signal path simplified block diagrams
- Receiver gain distribution chart
- Frequency synthesizer simplified block diagram
- Synthesizer operation example using a desired radio tune frequency

Included in the electronic theory section are the following items:

- Conversion between dBm and volts rms chart
- Discussion about the "heart" of the RF-590 frequency synthesizer, the phase-locked loop, and its many variations
- VCO frequency resolution reduction techniques

Many of these items appear in other sections of this manual and are discussed as necessary. For example, there are more extensive block diagrams provided with circuit descriptions, schematics, parts lists, and test procedures in each subassembly section describing a particular RF-590 assembly. However, items such as the dBm to Vrms conversion chart appear nowhere else in the text.

4.2 RECEIVER OPERATION

4.2.1 Receiver Signal Path

The information presented in this section details the signal processing in the receiver signal path from antenna RF input to audio output. The RF input range is from 10 kHz to 30 MHz. A dual conversion type receiver is employed, with the first intermediate frequency (IF) of 40.455 MHz and a second intermediate frequency (IF) of 455 kHz.

A variable first local oscillator (LO No. 1) of 40.465 to 70.455 MHz is employed for the first conversion to 40.455 MHz while a fixed second local oscillator (LO No. 2) at 40.000 MHz is employed for the second conversion to 455 kHz.

The RF signal path contains the following assemblies:

- Input Filter Assembly A1
- First Converter Assembly A2
- Second Converter Assembly A3
- IF Filter Assembly A4
- IF/Audio Assembly A5A1 and AGC Assembly A5A2
- Audio Amplifier Assembly A23

Additionally, Meter Board Assembly A13A3 provides monitoring capabilities, and ISB IF/Audio Assembly A18 provides ISB operation capabilities. Note that the A18 assembly is optional.

The following brief circuit descriptions follow figure 4-1, Simplified Receiver Block Diagram. A Receiver Gain Distribution Chart, figure 4-2, has also been included.

4.2.1.1 Input Filter Assembly A1

The antenna input to the receiver is applied to Input Filter Assembly A1. This assembly contains low pass filtering to provide more than 100 dB of rejection to undesired signals at input frequencies greater than 30 MHz.

Insertion loss is less than 1/2 dB, with a VSWR less than 2:1. Receiver input overload protection circuitry (up to 70 Vrms overload), muting, Built-In Test Equipment (BITE) detection, and BITE signal generation functions are also included.

4.2.1.2 First Converter Assembly A2

First Converter Assembly A2 accepts the 10 kHz to 30 MHz output from the A1 assembly and subtractively mixes with the first LO (40.465 to 70.455 MHz) to produce a first IF of 40.455 MHz. (Note that sideband inversion occurs during the mixing process.) Extensive filtering is utilized at 40.455 MHz before the first IF is directed to second Converter Assembly A3. Input signal levels of typically -120 to +10 dBm are gain controlled by an AGC signal which provides up to 20 dB of gain reduction. Typical conversion loss through the assembly is 0 dB.

A BITE detector operating at 40.455 MHz monitors the operation of the assembly.

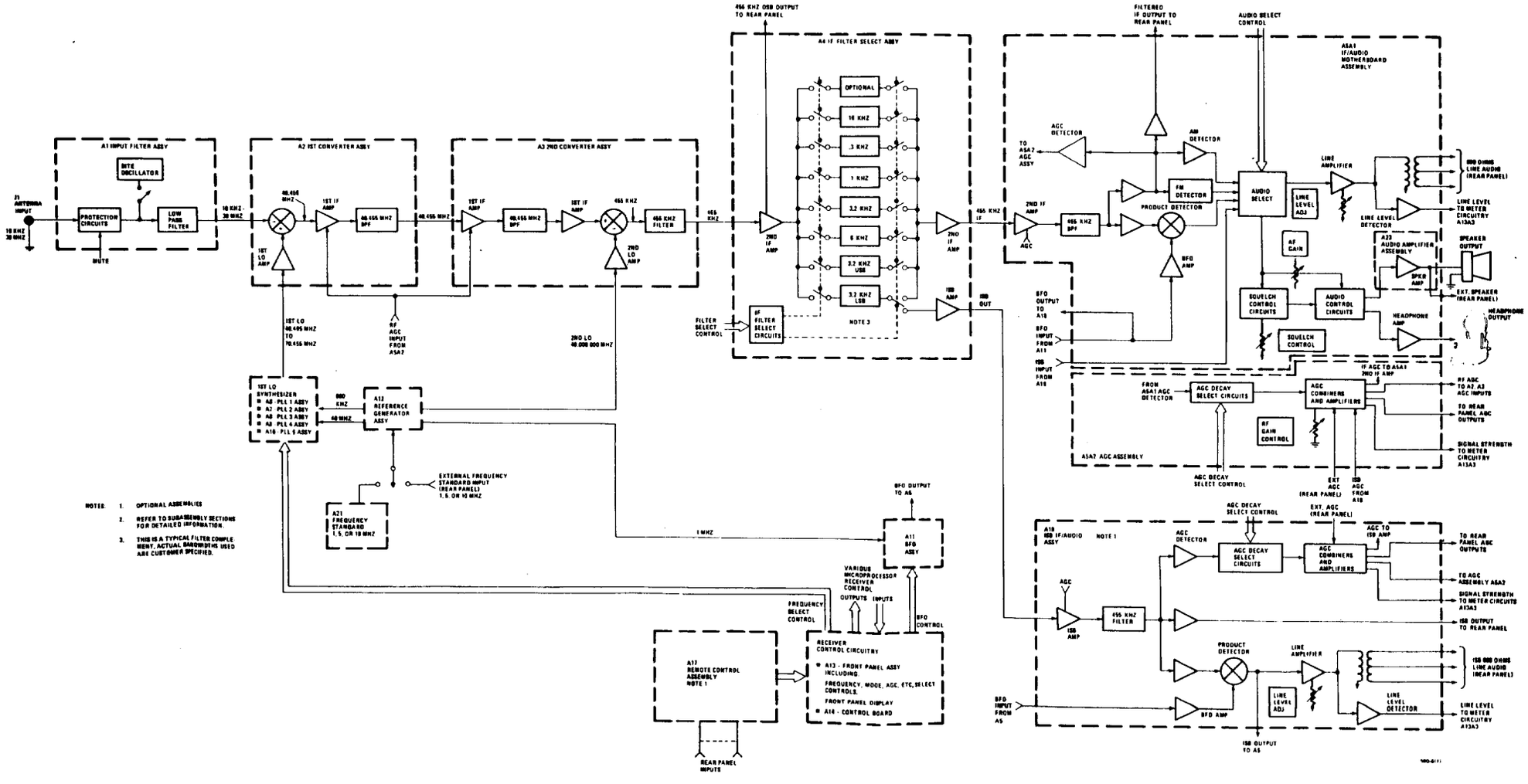

Figure 4-1. RF-590 Receiver Signal Path Block Diagram

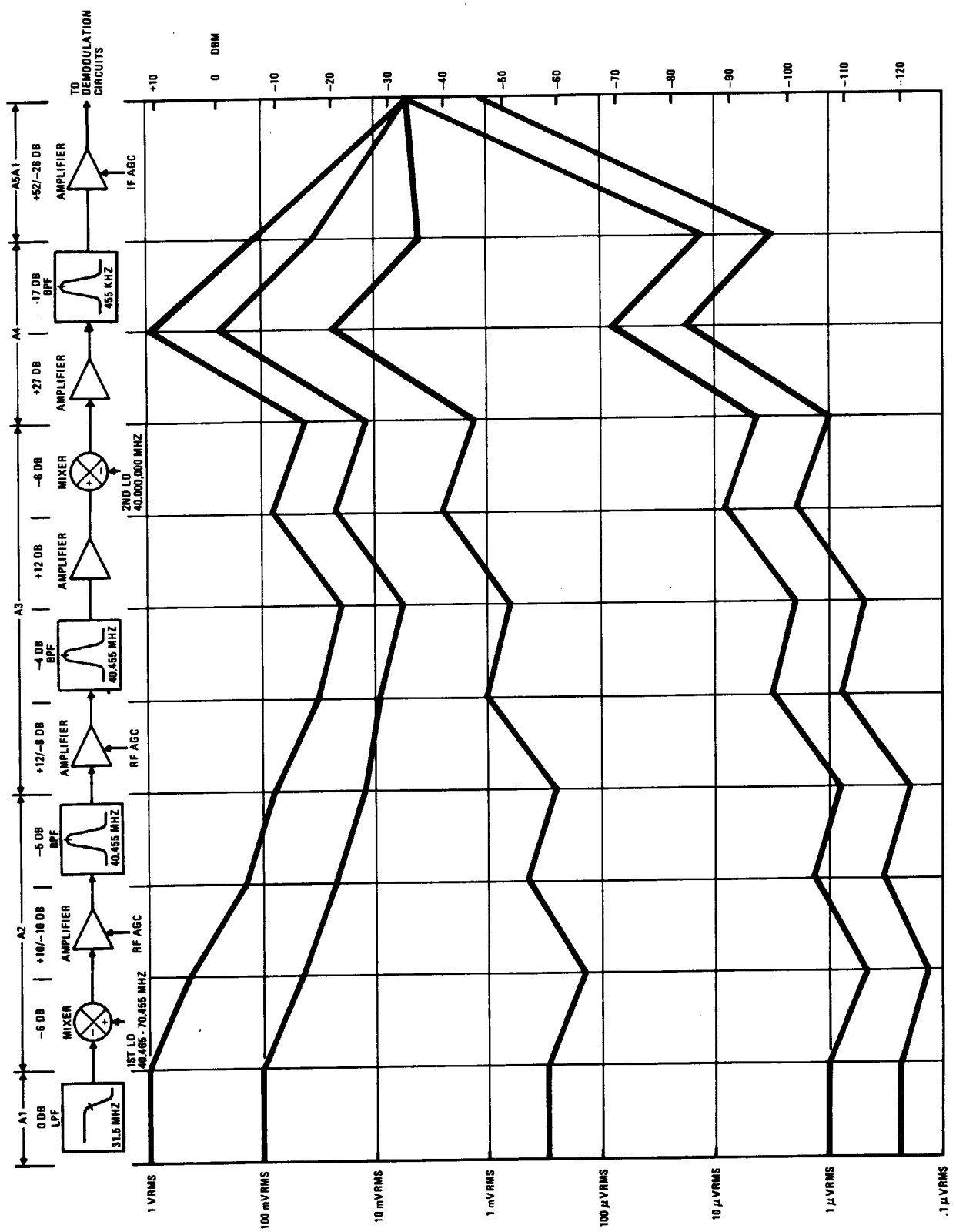

Figure 4-2. RF-590 Receiver Gain Distribution

4.2.1.3 Second Converter Assembly A3

Second Converter Assembly A3 converts the first IF of 40.455 MHz to a second IF of 455 kHz through subtractive mixing with the second LO frequency of 40.000000 MHz.

Filtering occurs at both IF frequencies. Overall module gain is approximately 16 dB and gain reduction of up to 20 dB is controlled by an AGC voltage.

A BITE detector operating at 455 kHz monitors the operation of the assembly.

4.2.1.4 IF Filter Assembly A4

IF Filter Assembly A4 accepts the second IF from the A3 assembly and provides the selection of one of eight filters for signal processing. (ISB operation requires selection of two filters.) The main signal frequency selectivity is determined by these filters. Module gain is +10 dB. An unfiltered 455 kHz signal output is tapped off and applied to a rear panel RF-590 connector for external demodulation or monitoring purposes. Two main signal outputs are fed off this board. The two signal outputs are:

- The normal 455 kHz second IF to the A5A1 IF/Audio assembly, (for AM, CW, FM, USB, or LSB operation).
- ISB output to the optional A18 ISB IF/Audio assembly (for ISB operation).

4.2.1.5 IF/Audio Assembly A5

IF/Audio Assembly A5 consists of the following two subassemblies:

- IF/Audio Motherboard A5A1
- AGC Board A5A2

4.2.1.5.1 IF/Audio Motherboard A5A1

The IF/Audio Motherboard A5A1 provides most of the receiver gain utilizing a cascaded 455 kHz second IF AGC controlled amplifier chain with a maximum gain of 80 dB. This amplifier works in conjunction with AGC controlled amplifiers on the A2 and A3 assemblies to provide a constant -34 dBm second IF output to the signal demodulators over an RF input range of -120 dBm to +10 dBm.

Additionally, the assembly contains circuits for the following functions:

- Signal demodulation (AM, FM, and Product Detection for USB, LSB, or CW signals)
- Audio amplification and control

- Squelch control
- BITE detection

Signal outputs include:

- Speaker audio output (to speaker Audio Amplifier Assembly A23)
- Headphones (+10 dBm (maximum)/600 ohms)
- Line output (-16 dBm to +10 dBm/600 ohms, rear panel)
- Filtered 455 kHz IF output (50 ohm, rear panel)

Note that audio outputs (speaker and headphone) and line output are independently adjustable.

4.2.1.5.2 AGC Board A5A2

AGC Board A5A2 contains AGC (Automatic Gain Control) voltage generation and shaping circuitry for slow, medium, or fast AGC decay speeds. BITE detection circuitry is also provided. Outputs include AGC control voltages to A2, A3, and A5A1 assemblies and a rear panel AGC output. Figure 4-2 (receiver gain distribution) shows the effectiveness of the AGC circuits in providing a constant -34 dBm input to the A5A1 signal demodulators.

4.2.1.6 Audio Amplifier A23

Audio Amplifier Assembly A23 receives demodulated audio from the A5A1 assembly. Amplifiers on this assembly provide enough power gain to drive the 8 ohm front panel speaker or an external 8 ohm speaker to a minimum of 2.5 watts at full audio.

4.2.1.7 ISB IF/Audio Assembly A18

ISB IF/Audio Assembly A18 is an option purchased when independent sideband operation (simultaneous LSB and USB) is required. A18 operation is virtually identical to A5 operation, except that the A18 assembly contains only one demodulator circuit (the ISB product detector). A 455 kHz ISB IF output, an ISB line audio output, and an ISB AGC voltage output are provided on the RF-590 rear panel.

4.2.1.8 Meter Board A13A3

Meter Board A13A3 contains the circuitry and switches required to monitor selected RF and AF signals. The following signals may be monitored on the front panel meter via front panel switch controls:

- USB-RF
- USB-AF

- LSB-RF
- LSB-AF

(Note that in ISB operation, the ISB channel is monitored in the LSB switch mode.)

Meter drive signals originate on IF/Audio Assembly A5. (ISB signals originate on ISB IF/Audio Assembly A18.) The meter itself is calibrated in microvolts rms or mVrms for RF signal strength and dBm/600 ohms for AF line level.

4.2.2 Frequency Synthesizer

The information presented in this section shows the signal processing required to cause the receiver to tune anywhere in the RF input range of 10 kHz to 30 MHz with a 1 Hz resolution.

The main function of the entire synthesizer is to provide a variable output frequency that functions as the first Local Oscillator injection for the first Converter A2 mixer. This first LO must have the following characteristics:

a. Tune exactly 40.455000 MHz higher in frequency than the desired RF input signal. This requires a range of 40.465 MHz to 70.455 MHz.

b. Respond to changes in the receiver's tuning controls to allow a 1 Hz resolution over the approximately 30,000,000 Hz tuning range.

c. Perform a. and b. within a tuning time of less than 20 milliseconds.

The Frequency Synthesizer consists of the following assemblies:

- PLL I Assembly A6
- PLL II Assembly A7
- PLL III Assembly A8
- PLL IV Assembly A9
- PLL V Assembly A10
- Reference Generator Assembly A12
- Frequency Standard Assembly A21

Reference Generator Assembly A12 also provides the 40.000000 MHz second LO injection for the A3 assembly's signal conversion of the 40.455 MHz frist IF to a 455 kHz second IF.

BFO Assembly A11 is also a frequency synthesizer covering a much smaller frequency range (445 kHz to 465 kHz). The BFO assembly is required to accomplish product detection.

Note that figure 4-3 shows a complete frequency synthesizer simplified block diagram and figure 4-4 shows how to compute the intermediate frequencies produced by the synthesizer assemblies for any given receiver tune frequency. Other information which may be helpful (towards the end of this section) is the discussion of programmable divide by N phase locked loops and frequency resolution reduction techniques. Also, all these assemblies are discussed in detail in their respective subsections.

4.2.2.1 Frequency Synthesizer - Basic Operation

The frequency synthesizer must be able to tune 40.465000 MHz to 70.455000 MHz with 1 Hz resolution. In order to do this, three main phase locked loop voltage controlled oscillators with programmable divide by N counters are utilized.

The frequency of each of these VCOs is a function of their associated programmable counter factor, N. N is a function of the values of the receiver's tuning positions (10 MHz, 1 MHz, . . . 1 Hz). Each of the programmable counters are wired to accept only a segment of the receiver's tuning positions. For example, the A7 assembly receives tune data relating to the 10 MHz, 1 MHz, and 100 kHz position's value. The A8 assembly receives tune data relating to the 10 kHz and 1 kHz values, and the A10 assembly receives tune data relating to the 100 Hz, 10 Hz, and 1 Hz values. (Note that this data is in the form of a serial data code generated by the receiver's Control Board Assembly A14).

If the values of the input tune data change (for any of these three assemblies), the programmable counter's divide by N factor changes. Since the programmable counter is in the VCO feedback path to a phase comparator, the phase comparator issues an error command to force the VCO to tune in the direction required to make the feedback signal equal to the reference signal at the phase comparator's inputs. The net result (for each of the three assemblies) is that the VCO output frequency is a unique frequency corresponding to exactly one value of the tune data at the input to the programmable counter, and hence to the receiver tune frequency.

The outputs of the A7, A8, and A10 assemblies undergo further processing in the synthesizer chain before they are combined in the A6 assembly. The result of the combination of these three unique frequencies is a single unique frequency directly relating to the settings of all the receiver's tune positions. Furthermore, it is controllable to 1 Hz resolution, and is used as the first LO injection for the First Converter Assembly A2 mixer to tune the radio.

4.2.2.2 Reference Generator Assembly A12 and Frequency Standard Assembly A21

Frequency Standard Assembly A21 is the key to the RF-590 frequency stability and accuracy. Three stability options are available: 1×10^{-6}, 1×10^{-7}, and 1×10^{-8} per day at either 1 MHz, 5 MHz, or 10 MHz.

The standard output phase locks a 40 MHz VCXO on the A12 assembly. Phase lock loop (PLL) references on all other assemblies are derived from this A12 VCXO. The A12 also provides 40 MHz to the A3 assembly for signal path conversion to the second IF of 455 kHz.

4.2.2.3 PLL V Assembly A10

The A10 assembly is a programmable divide by N PLL that provides the 1 Hz, 10 Hz, and 100 Hz tuning increments in the LO 1 output signal. The A10 output is from 50 to 60 kHz in 10 Hz controllable steps. The output frequency is 10 (6000 – $X_3X_2X_1$) Hz, where $X_3X_2X_1$ is the value of the 100 Hz, 10 Hz, and 1 Hz receiver tune positions, respectively.

4.2.2.4 PLL IV Assembly A9

The A9 assembly is a translational type phase locked loop which converts the low frequency A10 output of 50 to 60 kHz in 10 Hz increments into 40.05 to 40.06 MHz in 10 Hz increments. The A9 assembly provides the intermediate signal processing required before the A10 output can be combined with the PLL III A8 10 kHz and 1 kHz tuning increments. The A9 output may be computed from the formula 40,000,000 + 10 (6000 – $X_3X_2X_1$) Hz, where $X_3X_2X_1$ is the value of the 100 Hz, 10 Hz, and 1 Hz receiver tune positions, respectively.

4.2.2.5 PLL III Assembly A8

The A8 assembly is a programmable divide by N and translation PLL which performs the following two functions:

- Generation of the 10 kHz and 1 kHz tuning increments for LO 1 output
- Combination of these increments with the 100 Hz, 10 Hz, and 1 Hz tuning increments provided by the A9 assembly

The A8 output frequency can be determined by the following formula. Given that $X_3X_2X_1$ are the values of the receiver's 100 Hz, 10 Hz, and 1 Hz tuning positions and that X_5X_4 are the values of the 10 kHz and 1 kHz tuning positions, A8 frequency = [40,000,000 + 10 (6000 – $X_3X_2X_1$)] – [10,000 (361 + X_5X_4] Hz. Note that the A8 output frequency range is 35.45 MHz to 36.45 MHz.

4.2.2.6 PLL II Assembly A7

The A7 assembly is a programmable divide by N PLL which provides the 10 MHz, 1 MHz, and 100 kHz tuning increments in the LO 1 output. The A10 output is from 44.1 MHz to 74.0 MHz in 100 kHz controllable steps.

The A7 output frequency is 100,000 (441 + $X_8X_7X_6$), where $X_8X_7X_6$ is the value of the 10 MHz, 1 MHz, and 100 kHz receiver tuning positions, respectively.

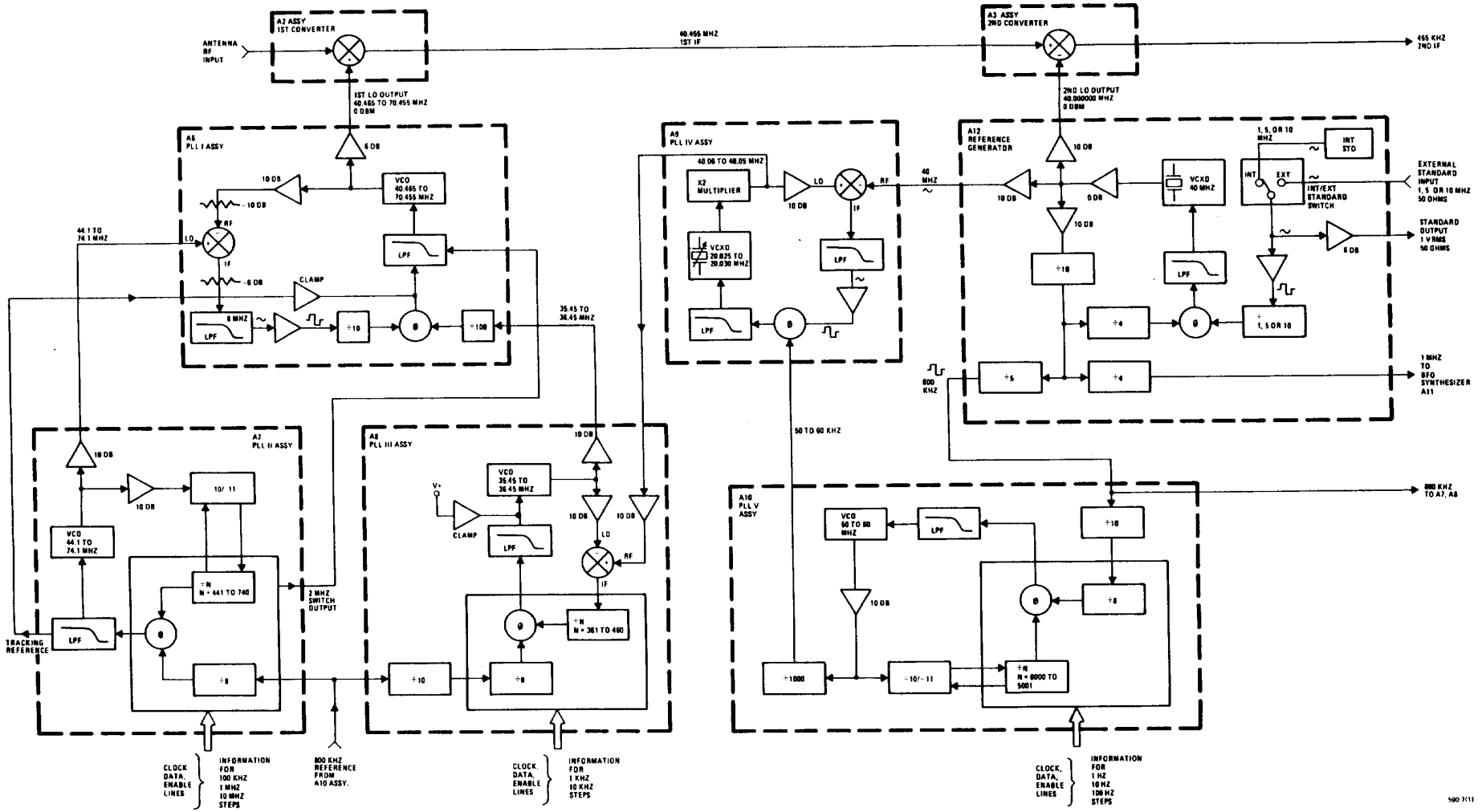

Figure 4-3. RF-590 Frequency Synthesizer Block Diagram

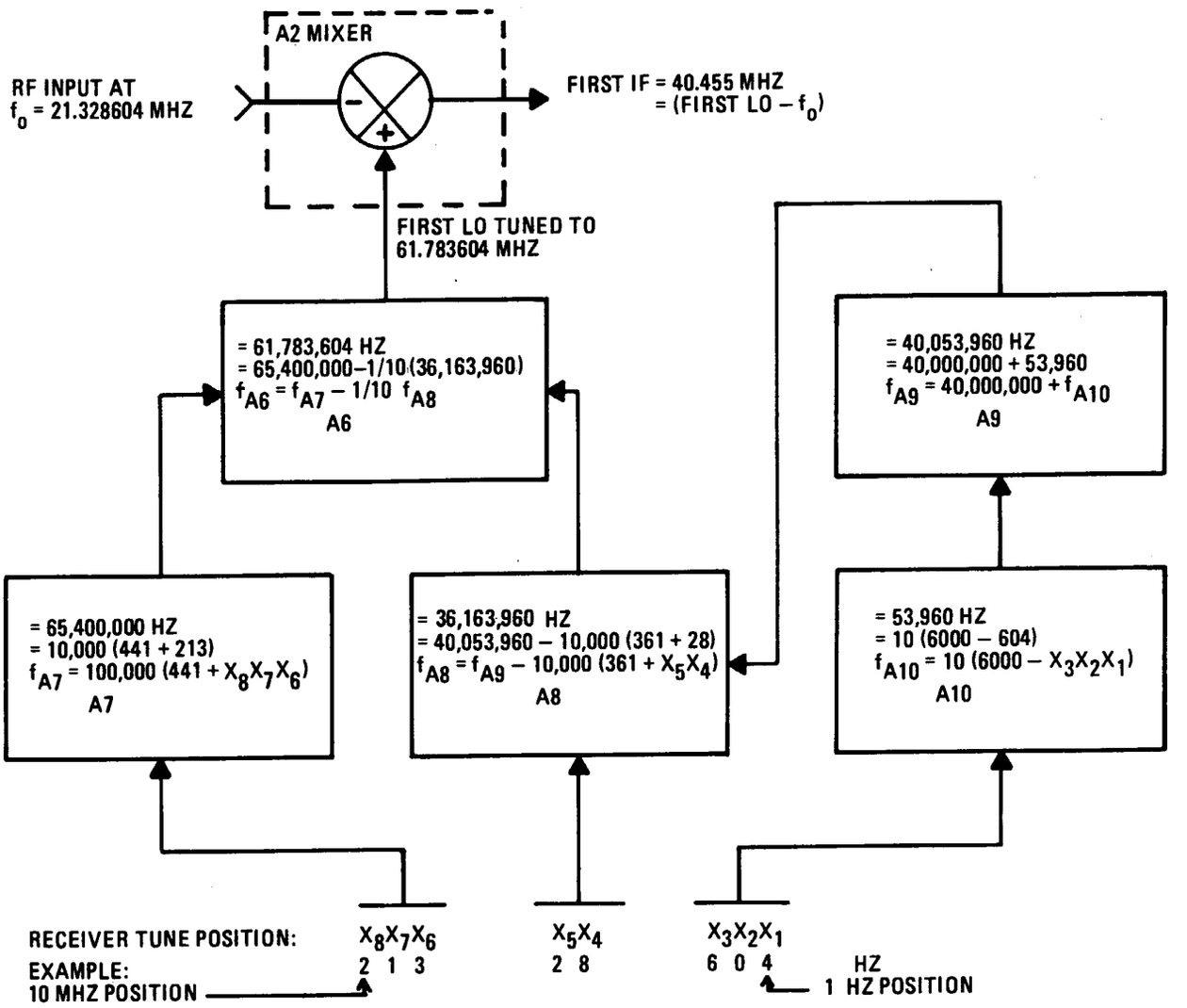

Figure 4-4. Frequency Synthesizer Tuning Example

4.2.2.7 PLL I Assembly A6

The A6 assembly is a translation type PLL which combines the 10 MHz through 1 Hz tuning increments for the LO 1 output from assemblies A7, A8, A9, and A10. The output signal will be the first LO injection signal. It will be variable from 40.465 kHz to 70.455 MHz in 1 Hz controllable steps. Given a receive tune frequency of $X_8X_7X_6X_5X_4X_3X_2X_1$ Hz where X_8 to X_1 are the values of the 10 MHz to 1 Hz receiver tuning positions, the A6 (and LO 1) output frequency is:

$$FA6 = FA7 - \frac{1}{10} FA8 \text{ Hz},$$

where

$$FA7 = (441 + X_8X_7X_6)\ 100{,}000 \text{ Hz}$$
$$FA8 = [40{,}000{,}000 + 10\ (6000 - X_3X_2X_1)] - [10{,}000\ (361 + X_5X_4)] \text{ Hz}$$

This signal will always be tuned exactly 40.455 MHz above the receiver tune frequency.

4.2.2.8 BFO Assembly A11

The A11 assembly is a programmable divide by N PLL which provides the BFO offset injection signal required on IF/Audio Motherboard Assembly A5A1 for proper CW or SB reception. The BFO output at 455 kHz ± 10 kHz mixes with the 455 kHz second IF signal at the product detector and provides an audio offset of up to 10 kHz. The A11 output frequency may be determined from the following formula where $X_AX_BX_C$ is the ± value of the 1 kHz, 100 Hz, and 10 Hz BFO offset tuning positions:

$$FA11 = 10\ (45{,}500 - X_AX_BX_C) \text{ Hz}$$

4.2.2.9 Frequency Synthesizer Tuning Example

The output frequencies of the A10, A9, A8, A7, and A6 assemblies at any given receiver tune frequency can be determined from the example shown in figure 4-4. Assume a receiver frequency f_o = 21,328,604 Hz and that $X_8X_7X_6X_5X_4X_3X_2X_1$ represent the values of the 10 MHz through 1 Hz positions.

Start at the A10 assembly, then move on to the A9, A8, A7, and A6 in that order.

The answer can always be checked since the following formula must always be true.

$$F_{LO\ 1} = f_o + 40.455 \text{ MHz}$$

Here,

$$f_o = 21.328{,}604 \text{ MHz}$$

therefore,

$$F_{LO\ 1} = 21.328{,}604 \text{ MHz} + 40.455 \text{ MHz}$$
$$= 61.783{,}604 \text{ MHz (which agrees with the result of figure 4-4)}$$

4.3 ADDITIONAL THEORY

4.3.1 Conversion Between dBm and Vrms

Power levels in this manual are stated in dBm, or decibels with respect to 1 milliwatt. For example, +6 dBm means 6 dB more than (above) 1 mW, or 4 mW. Similarly, -6 dBm is 6 dB less than (below) 1 mW, or 0.25 mW (250 uW). Notice that every value of dBm corresponds to a particular amount of power. If the impedance in which this power is dissipated is known, the corresponding voltage and current can be determined. Table 4-1 lists 50 ohm voltage equivalents for many dBm power levels. Note that for negative values of dBm, voltages are read in either of the two left-hand columns. For positive values of dBm, voltages are read in the right-hand column. For instance, -6 dBm is 0.112 V (112 mV), across 50 ohms, while +6 dBm is 0.446 V. Similarly, -20 dBm equals 22.4 mV, while +20 dBm equals 2.24 volts (across 50 ohms).

Table 4-1. Conversion of dBm to Vrms across 50 ohms
(0 dBm = 1 mWatt)

(Negative dBm)		dBm	(Positive dBm)
Volts	Millivolts		Volts
.224	224	0	.224
.199	199	1	.251
.178	178	2	.282
.158	158	3	.316
.141	141	4	.354
.126	126	5	.398
.112	112	6	.446
	99.9	7	.501
	89.0	8	.562
	79.3	9	.630
	70.7	10	.707
	63.0	11	.793
	56.2	12	.890
	50.1	13	.999
	44.6	14	1.12
	39.8	15	1.26

Table 4-1. Conversion of dBm to Vrms across 50 ohms (Cont.)
(0 dBm = 1 mWatt)

(Negative dBm)			(Positive dBm)
Volts	Millivolts	dBm	Volts
	35.4	16	1.41
	31.6	17	1.58
	28.2	18	1.78
	25.1	19	1.99
	22.4	20	2.24
	19.9	21	2.51
	17.8	22	2.82
	15.8	23	3.16
	14.1	24	3.54
	12.6	25	3.98
	12.0	25.41	4.17
	11.2	26	4.46
	10.0	27	5.01
	8.90	28	5.62
	7.93	29	6.30
	7.07	30	7.07
	3.98	35	12.6
	2.24	40	22.4
	1.26	45	39.8
	0.707	50	70.7

4.3.2 PLL Frequency Resolution Reduction Techniques

Use of a single frequency source to provide the variable first local oscillator signal in a radio such as the RF-590 would be virtually impossible (given the resolution requirements desired). This would require that the LO tune over the entire range (40.465000 MHz to 70.455000 MHz) with a resolution of 1 Hz or a total of 30,000,000 discrete 1 Hz steps. By using three sources, each with a much lower resolution requirement and combining their outputs, the net one part per 30,000,000 resolution can still be obtained.

Assume that a total of 30,000,000 1 Hz increments must be tuned. Allow each of the three sources to, produce an output response proportional to only a segment of the 30,000,000 necessary frequencies. The following three examples show how the three sources produce an output response.

- Let source no. 1 respond to changes in the 10 MHz, 1 MHz, and/or .1 MHz positions. Since these would be a maximum of 300.1 MHz possible changes between 00.0 MHz and 29.9 MHz, the resolution of source no. 1 would be one part per 300.

- Let source no. 2 respond to changes in the 10 kHz and/or 1 kHz position. There would be a maximum of 100 1 kHz changes between 00 kHz and 99 kHz (for a resolution of 1 part per 100).

- Let source no. 3 respond to changes in the 100 Hz, 10 Hz, and/or 1 Hz positions. There would be a maximum of 1000 1 Hz changes between 000 Hz and 999 Hz (for a resolution of one part per 1000).

Combining the three source outputs in a nonlinear device such as a mixer would yield the desired frequency range and 1 Hz resolution required. Figure 4-5 illustrates this.

Note that the sources used in this example would actually be voltage controlled oscillators (VCO) whose actual output frequency would be controlled by a programmable divide by N counter.

The RF-590 essentially uses this concept, except that the source frequencies run at a much higher frequency than those shown. There are three VCOs which respond to the tuning segments shown. (10 MHz, 1 MHz, and 100 kHz increment changes occur on the A7 assembly, the 10 kHz and 1 kHz increment changes occur on the A8 assembly, and the 100 Hz, 10 Hz, and 1 Hz increment changes occur on the A10 assembly.)

4.3.3 Phase Locked Loops (PLL)

The basic phase locked loop (PLL) consists of four components: a phase detector (or comparator), a low pass filter, a voltage controlled oscillator (VCO), and a divider (counter). The counter component may be either a fixed divisor or programmable. The RF-590 utilizes both types.

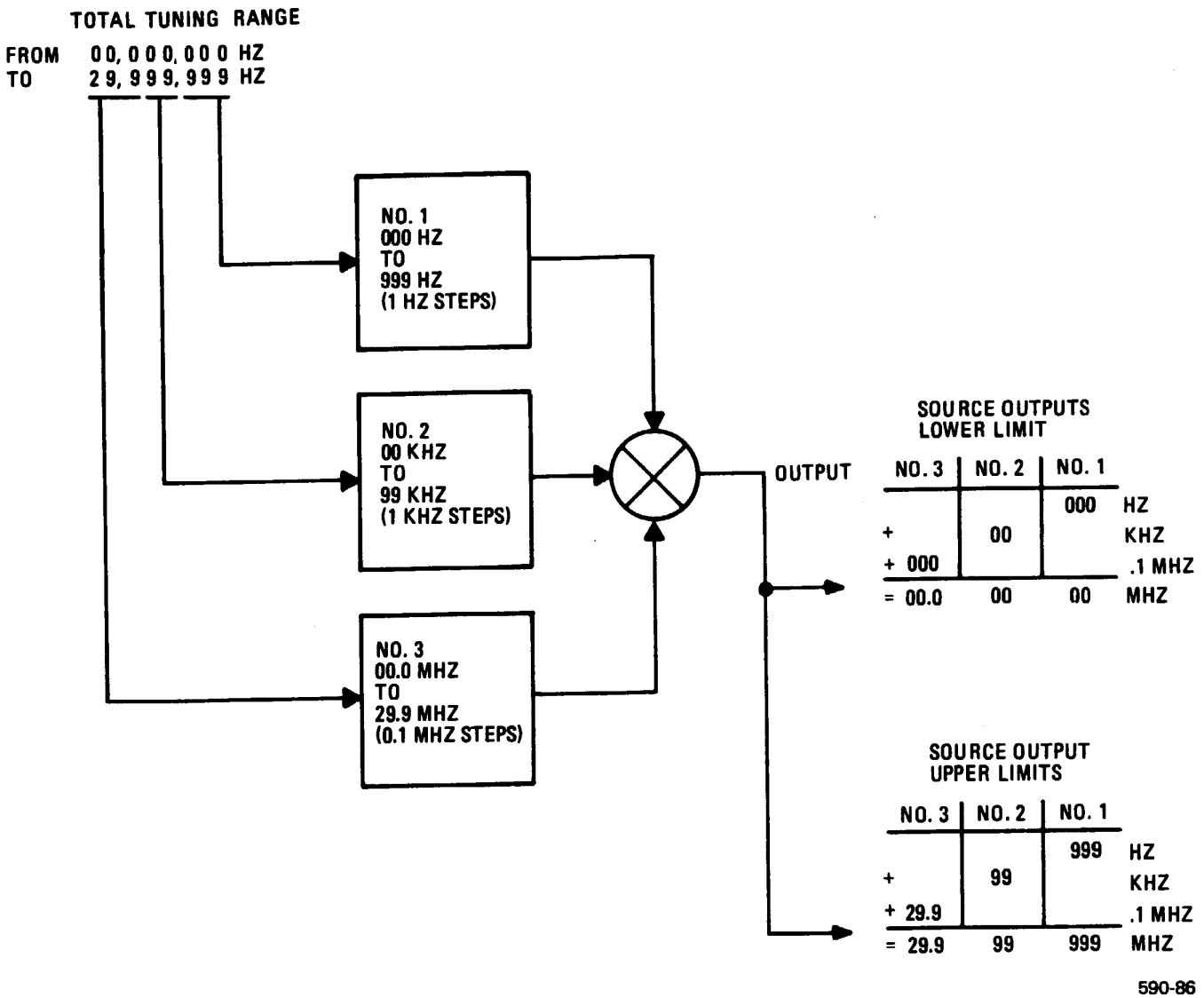

Figure 4-5. Resolution Reduction Example

4.3.3.1 Basic Phase Locked Loop

Figure 4-6 shows the four basic components of a phase locked loop. PLL operation involves comparing the frequency and phase of an incoming reference signal to the output of the voltage controlled oscillator (VCO). If the two signals differ in frequency and/or phase, an error voltage is generated by the phase detector and applied to the VCO. This causes it to correct in the direction required for decreasing the frequency/phase difference. The correction procedure continues until lock is achieved, after which the VCO will track the incoming reference signal.

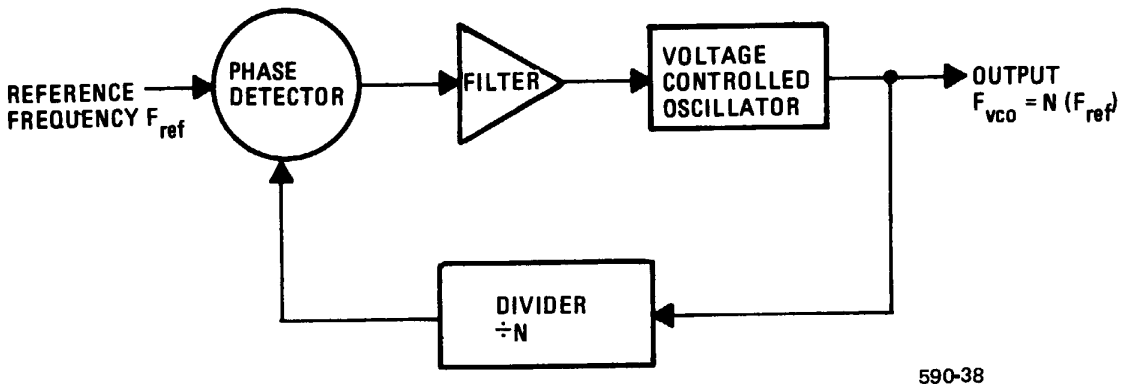

Figure 4-6. Basic Phase Locked Loop

4.3.3.2 PLL Programmable Counters

Dividing a VCO output by two before applying it to the phase detector results in an error voltage that drives the VCO to twice the reference frequency. A divide-by-three action results in an error voltage that drives the VCO to three times the reference frequency. From this, the following relationship can be given, $f_{VCO} = N (F_{REF})$.

An example of the basic phase lock loop technique, using numbers, will provide an understanding of its actual operation. Referring to figure 4-7, the desired frequency is obtained by programming the variable divider through selectable inputs. Assuming the VCO is locked at the desired frequency of 1 MHz, this signal enters the input of the (in this case) divide-by-100 counter (divider). The counter emits a pulse at its output each time 100 pulses enter its input. Therefore, dividing the 1 MHz input by 100 results in an output of 10 kHz. This 10 kHz signal is compared to the reference frequency of 10 kHz indicating a locked situation. If the divider's output had been less than 10 kHz, the phase detector would have produced pulses to drive the VCO to a higher frequency. Similarly, if the divider's output had been greater than 10 kHz, the VCO would have been driven to a lower frequency. Note that the phase lock loop's output is dependent upon the selectable inputs of the variable divider. The RF-590 provides this input to the ÷ N counter in the form of a serial data command word. The coding of this word determines the divisor ratio of the counter, and is supplied (under microprocessor control) from the information supplied by the RF-590 frequency select controls.

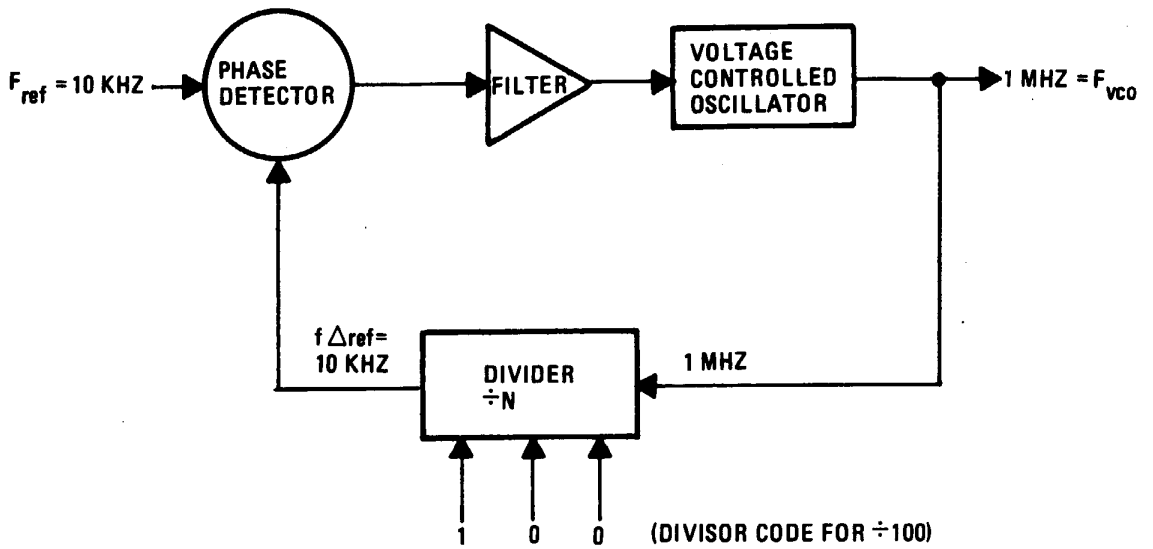

Figure 4-7. Programmable Phase Lock Loop

4.3.3.3 PLL Prescaling Operation

A variation of the basic PLL which involves division of the feedback VCO signal prior to application to the ÷ N counter is shown in figure 4-8. The total divider portion of the PLL now consists of two programmable counters and a two modulus prescaler.

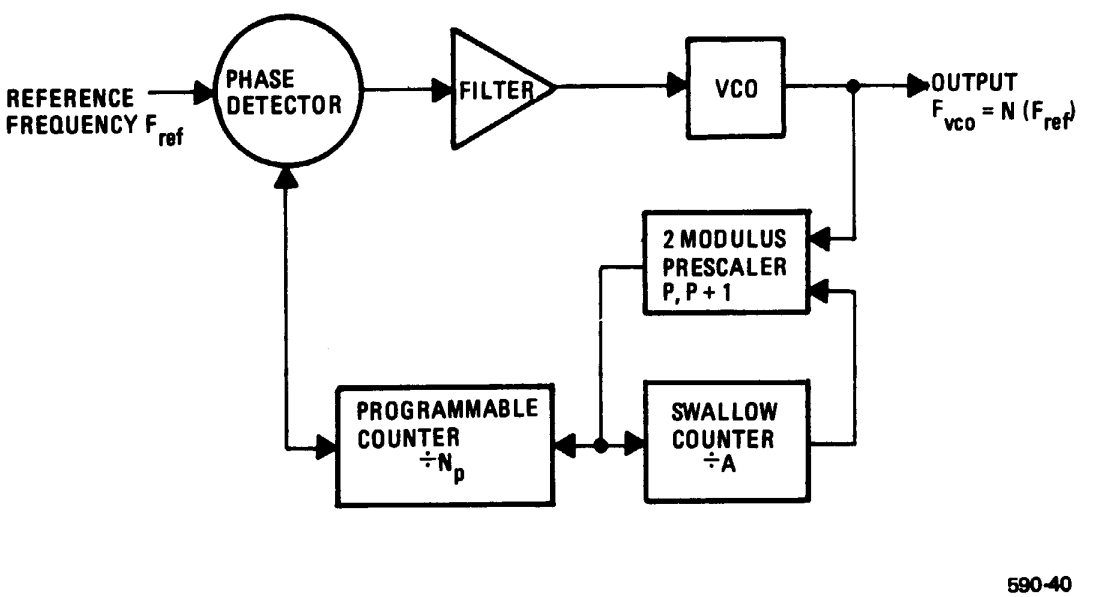

Figure 4-8. Phase Lock Loop Prescaling Technique

The two modulus prescaler begins operation by dividing the VCO output by the higher of its two possible divisors, P + 1. The programmable ÷ N counter counts the number of pulses from the prescaler. The swallow counter controls the number of times that the prescaler will be allowed to divide by (P + 1). (To be precise, A times.) After the swallow counter reaches A counts, it instructs the prescaler to change its division ratio to P. (Note that the RF-590 uses this scheme on the A7 and A10 assemblies, where the prescaler is a ÷10/÷11 counter, and the swallow counter is a counter internal to the ÷ N IC.)

In operation, the prescaler divides by P + 1, A times. For every P + 1 pulse from the prescaler, both the A counter and Np counter are decreased by 1. The prescaler divides by P + 1 until counter A reaches its zero state. At this point, the modulus of the prescaler changes to P. The prescaler then divides by P until the remaining count, (Np-A) in the Np counter, decreases to zero. At this time, the Np output emits a pulse while the A and Np counters reset. The cycle then repeats.

An example of the two modulus prescaling technique is given in figure 4-9 and table 4-2. For illustrative purposes, a VCO output of 50.7 MHz is desired.

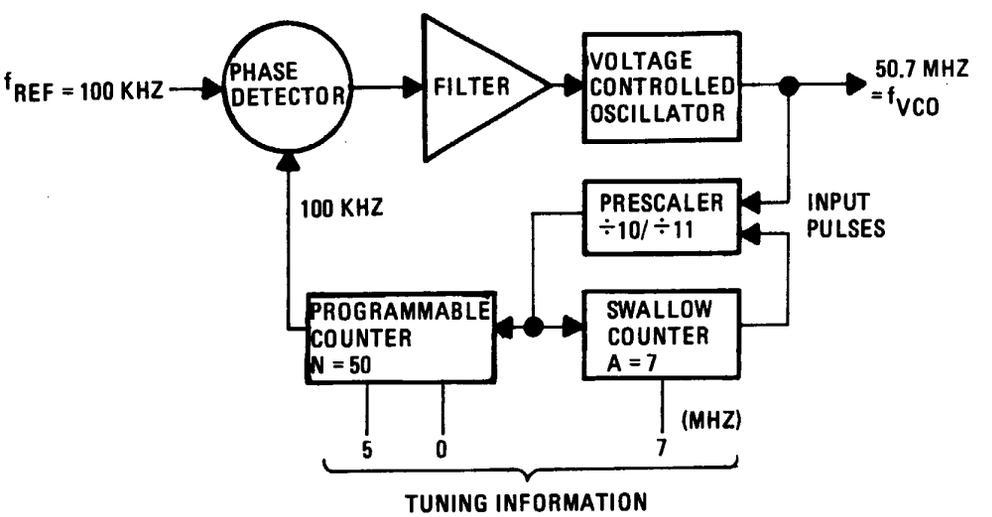

Figure 4-9. Prescaling Technique Example

Table 4-2. Prescaling Technique Example

Input Pulses	Prescaler Counts	Swallow Counter	Programmable Counter
0	0	7	50
11	11	6	49
22	11	5	48
33	11	4	47

Table 4-2. Prescaling Technique Example (Cont.)

Input Pulses	Prescaler Counts	Swallow Counter	Programmable Counter
44	11	3	46
55	11	2	45
66	11	1	44
77	11	0	43
87	10	0	42
97	10	0	41
107	10	0	40
477	10	0	3
487	10	0	2
497	10	0	1
507	10	0	0

507 input pulses = 1 output pulse

Selected into the programmable counter are the two most significant digits, 5 and 0. Selected into the swallow counter is the least significant digit, 7. Under locked conditions, the divider has an input (fVCO) of 50.7 MHz, and an output of 100 kHz.

To produce a 100 kHz signal from the 50.7 MHz fVCO signal, a divisor ratio of (50.7 ÷ 100) or 507 is required. Table 4-2 shows a count sequence of 507 input pulses resulting in 1 output pulse. Similarly, a 50.7 MHz input results in a 100 kHz output.

The programmable ÷ N counter emits a pulse every time it counts 50 input pulses. With the swallow counter set to seven, the prescaler divides by 11, seven times, and then switches to dividing by 10. At this point, the ÷ N counter needs 43 input pulses before emitting an output pulse. The prescaler will now divide by 10, 43 times, to finish the count sequence. With seven counts of 11 (7 x 11 = 77) and 43 counts of 10 (43 x 10 = 430), one pulse emits from the programmable counter every (77 + 430) or 507 input pulses.

4.3.4 Charge Pumps

The basic circuit employed in the RF-590 which converts the PLL phase comparator complementary pulse output error signals into an analog dc VCO control voltage is the charge pump. The three basic components of a charge pump circuit are a current source, a current sink, and an output filter. Figure 4-10 shows a typical charge pump circuit.

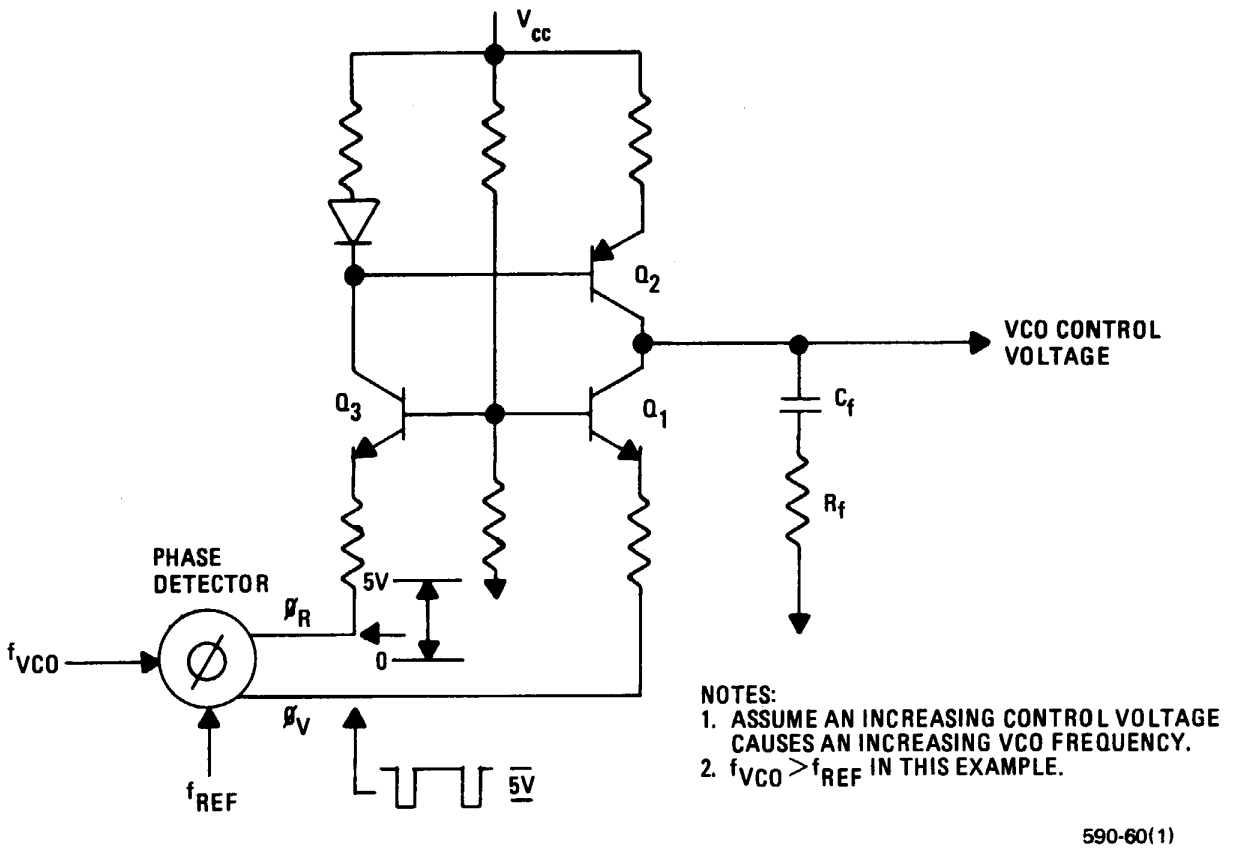

Figure 4-10. Basic Charge Pump Circuit

4.3.4.1 Phase Detector Outputs

The phase detector compares the phase and/or frequency of two inputs (f_{VCO} and f_{REF}) and issues an output error signal at one of its two outputs (ϕ_V or ϕ_R) whenever the inputs are not equal. The pulse widths of these output signals are directly proportional to the phase error of the two input signals.

If the frequency f_{VCO} is greater than f_{REF} or if the phase of f_{VCO} is leading, then error information is provided by ϕ_V pulsing low. ϕ_R remains essentially high (this is the situation shown in figure 4-10).

If the frequency f_{VCO} is less than f_{REF} or if the phase of f_{VCO} is lagging, then error information is provided by ϕ_R pulsing low. ϕ_V remains essentially high.

If the frequency of $f_{VCO} = f_{REF}$ and both are in phase, then both $\emptyset_V$ and $\emptyset_R$ remain high, except for a small minimum time period when both pulse low in phase. (This time period is too small to affect the charge pump's lead-lag filter network Cf-Rf however, and is ignored.)

4.3.4.2 Charge Pump Operation

The charge pump circuit functions as a current source/current sink network to lead-lag filter network Cf-Rf. Q2-Q3 function as a current source to dump charge into the filter network, while Q1 functions as a current sink to pull charge out of the network. The net result is that the output voltage across the network rises when Cf charges and falls when Cf discharges.

Assume that $f_{VCO} > f_{REF}$ as shown in figure 4-10. Output $\emptyset_R$ remains high, holding Q3 off. Output $\emptyset_V$ pulses low, turning Q1 on. This provides a low impedance discharge path to ground for Cf. As Cf discharges, the charge pump output voltage (VCO control voltage) decreases, causing f_{VCO} to decrease.

Now assume that $f_{VCO} < f_{REF}$. $\emptyset_V$ remains high, holding Q1 off. $\emptyset_R$ pulses low, turning on Q3, and allowing Q2 to turn on and dump charge into Cf. This causes the VCO control voltage to increase, causing f_{VCO} to increase.