

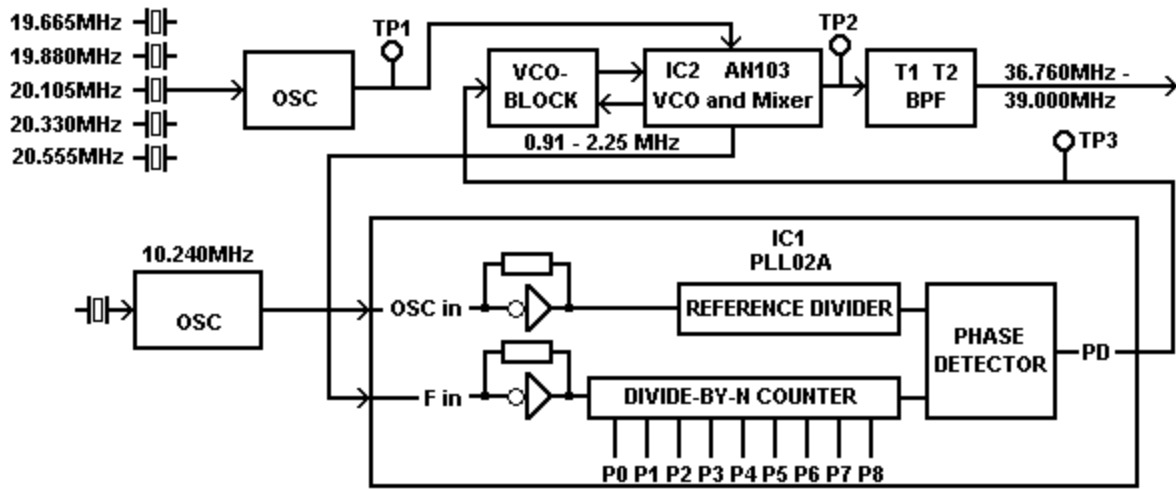
CHASSIS PCMA001S

Superstar 2200

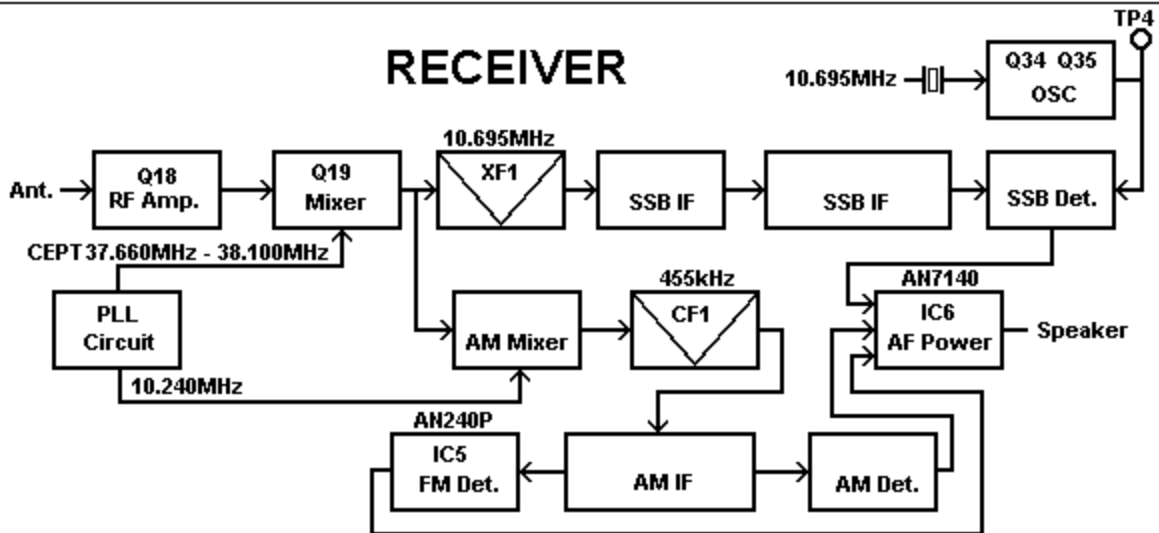
Alan 88S - Argus 5000 - Cobra 148GTL DX (fake)- Colt 2400 - Falcon 2000 - Ham International 8040 - HyGain 80 - Lafayette 240FM - Mongoose 2000 - Nato 2000 - Palomar 2400 - Palomar 5000 - TriStar 797 - TriStar 848

Block Schematic Diagram

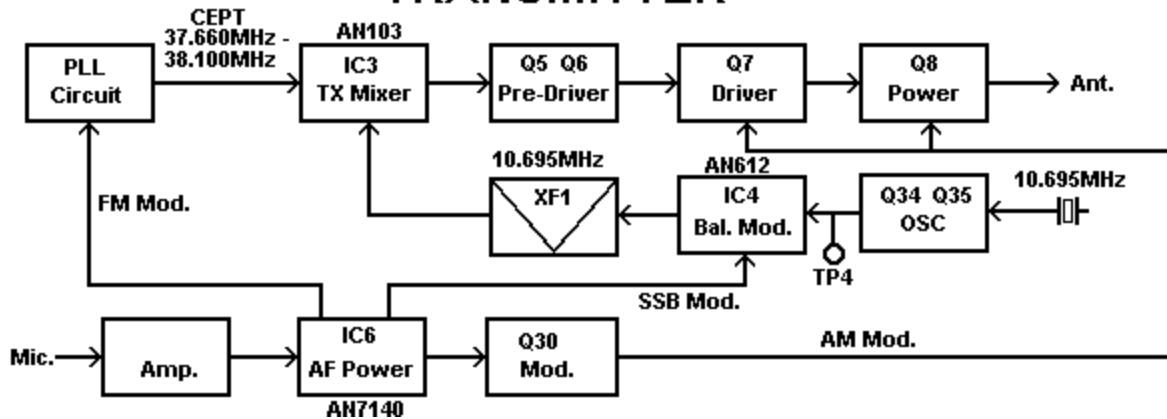
PLL CIRCUIT



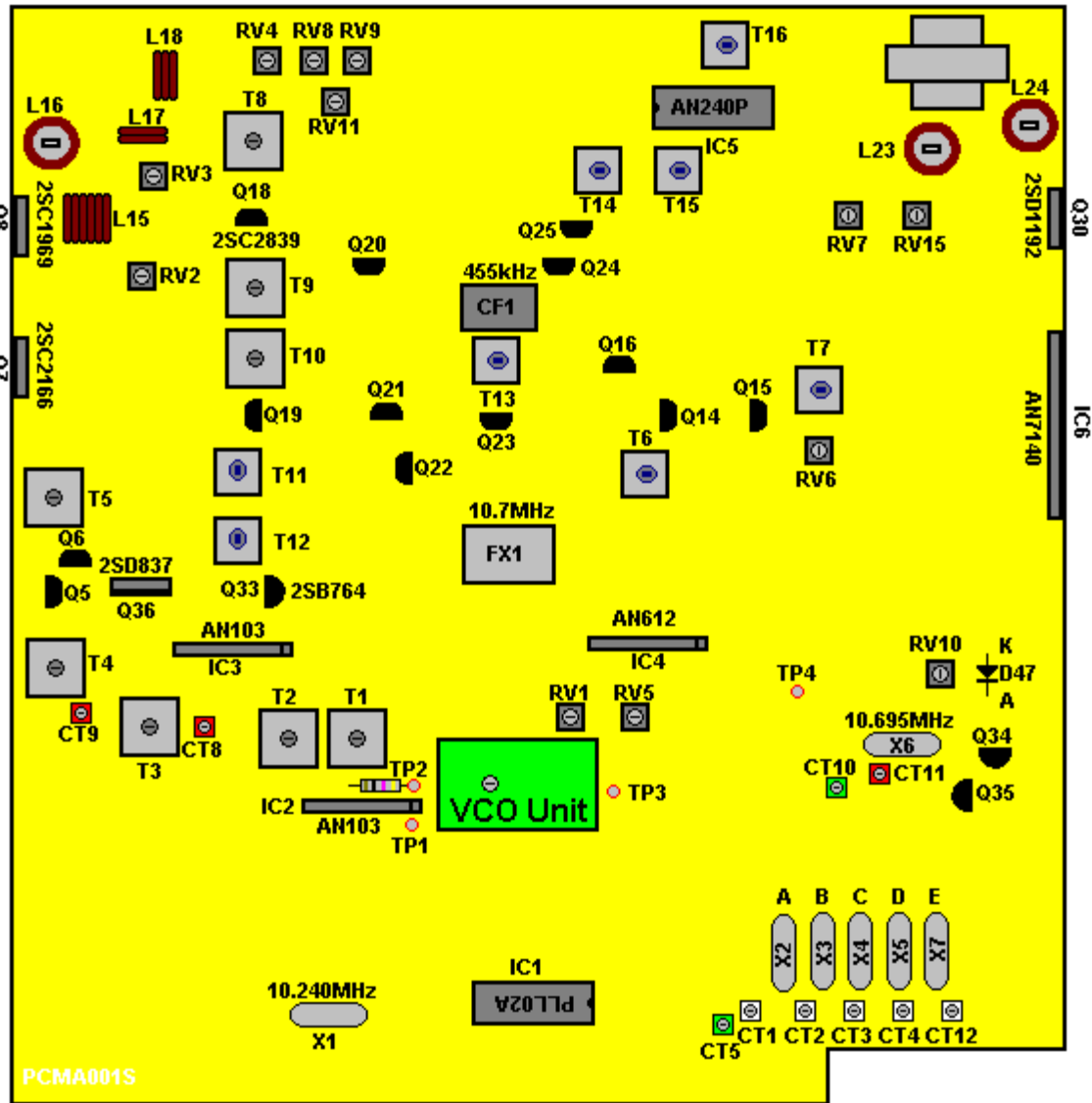
RECEIVER



TRANSMITTER



PCB Layout



Test Points

Reading Point	Adjustment	Description	Value
TP1	CT1	Band A -80 Ch.	19.655MHz
TP1	CT2	Band B -40 Ch.	19.880MHz
TP1	CT3	Band C CEPT	20.105MHz
TP1	CT4	Band D + 40 Ch.	20.330MHz
TP1	CT12	Band E + 80 Ch.	20.555MHz
TP1	CT5	Band C CEPT	20.1035MHz
TP2	T1	Output to RF local oscillator	37.660-38.100MHz for CEPT
TP3	VCO-Coil	VCO DC Voltage	2,5 Volt @ 27.175MHz
TP4	CT11	AM	10.695MHz
TP4	CT10	LSB	10.692MHz

Adjustment	Description	Value
RECEIVER		
T8	RF Input	
T9	RF Input	
T10	RF Input	
T11	1. IF	10,7MHz
T12	1. IF	10,7MHz
T13	AM IF	455kHz
T14	AM Detector	455kHz
T6	SSB IF	455kHz
T7	SSB Detector	
T16	FM Discriminator	
TRANSMITTER		
T1	PLL Output to Converter	37.660 - 38.100MHz for CEPT
T2	PLL Output to Converter	37.660 - 38.100MHz for CEPT
T3	Transmitter Output	26.965 - 27.405MHz for CEPT
T4	Transmitter Output	26.965 - 27.405MHz for CEPT
T5	Transmitter Output	26.965 - 27.405MHz for CEPT
L16	Transmitter Output	26.965 - 27.405MHz for CEPT
CT8	Transmitter Output USB/LSB	26.965 - 27.405MHz for CEPT
CT9	Transmitter Output USB/LSB	26.965 - 27.405MHz for CEPT
RV2	Bias Q8	
RV11	AM/FM Output Power	10 Watt
METER		
RV4	RF Power Meter	
RV8	RF S-Meter	SSB (USB/LSB)
RV9	RF S-Meter	AM/FM
.		
RV1	FM Modulation	+/- 2kHz
RV6	SSB Modulation	18 Watt p-p
RV11	AM Modulation	90%
RV5	Carrier at SSB	Adjust for NO Carrier

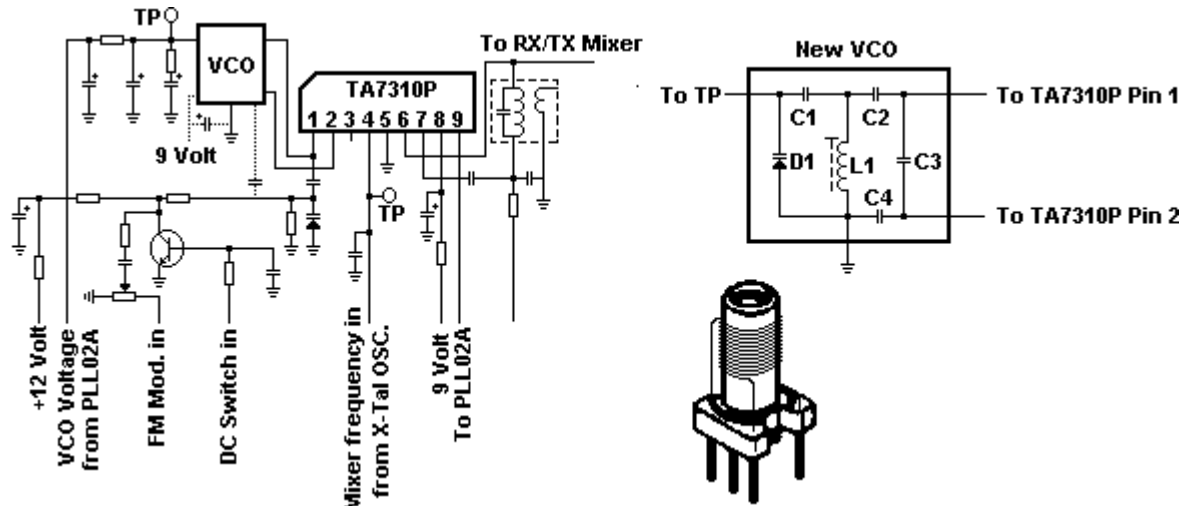
Modification for SuperStar 2200

To get 10-meter, cut trace from + 5 Volt to Pin 8 and 9.

To get 12-meter, cut trace from GND to Pin 7 and connect Pin 7 to + 5 Volt.

Make a new VCO Block.

VCO-Block for CB-Radio



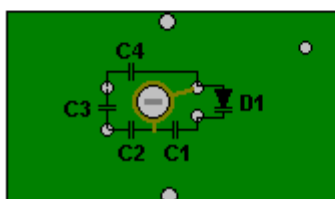
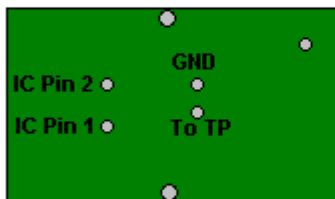
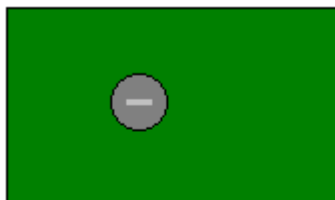
Re-tune both Transmitter and Receiver-part.

The VCO-Block is a part of the active oscillator in TA7310P. This will operate between 16MHz and 19MHz.

Output from TA7310P Pin 9 to PLL02A is: Mixer frequency - VCO frequency.
Output from TA7310P Pin 6 to Receiver/Transmitter Mixer is: Mixer frequency + VCO frequency.

The new "VCO-BLOCK" will operate between 14MHz and 21MHz, and will then cover 10-meter, 11-meter and 12-meter.

Top wiew



Components

D1 = BB156 (Phillips)

L1 = 5uH

C1 = 470pF

C2 = 470pF

C3 = 4,7pF

C4 = 12pF

VCO operates between 17.115MHz (Ch.1 Band A) and 18.445MHz (Ch.40 Band E),
output on Pin 6 is 36.780MHz (Ch.1 Band A) to 39.000MHz (Ch.40 Band E),
and output on Pin 9 is 2.550MHz to 2.110MHz inn all band.

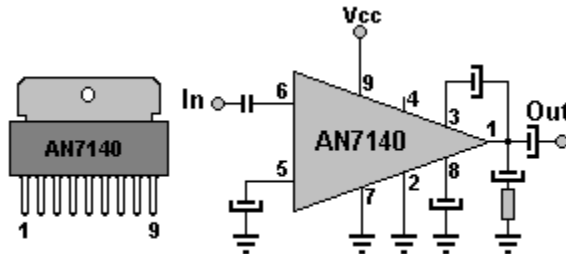
The VCO-voltage (TP1) operates between 4,5 Volt (Ch.1 Band A) and 0,5 Volt (Ch.40 Band E).

Frequency List

Ch.	A = - 80	B = - 40	C = CEPT	D = + 40	E = + 80
01	26.065	26.515	26.965	27.415	27.865
02	26.075	26.525	26.975	27.425	27.875
03	26.085	26.535	26.985	27.435	27.885
04	26.105	26.555	27.005	27.455	27.905
05	26.115	26.565	27.015	27.465	27.915
06	26.125	26.575	27.025	27.475	27.925
07	26.135	26.585	27.035	27.485	27.935
08	26.155	26.605	27.055	27.505	27.955
09	26.165	26.615	27.065	27.515	27.965
10	26.175	26.625	27.075	27.525	27.975
11	26.185	26.635	27.085	27.535	27.985
12	26.205	26.655	27.105	27.555	28.005
13	26.215	26.665	27.115	27.565	28.015
14	26.225	26.675	27.125	27.575	28.025
15	26.235	26.685	27.135	27.585	28.035
16	26.255	26.705	27.155	27.605	28.055
17	26.265	26.715	27.165	27.615	28.065
18	26.275	26.725	27.175	27.625	28.075
19	26.285	26.735	27.185	27.635	28.085
20	26.305	26.755	27.205	27.655	28.105
21	26.315	26.765	27.215	27.665	28.115
22	26.325	26.775	27.225	27.675	28.125
23	26.355	26.805	27.255	27.705	28.155
24	26.335	26.785	27.235	27.685	28.135
25	26.345	26.795	27.245	27.695	28.145
26	26.365	26.815	27.265	27.715	28.165
27	26.375	26.825	27.275	27.725	28.175
28	26.385	26.835	27.285	27.735	28.185
29	26.395	26.845	27.295	27.745	28.195
30	26.405	26.855	27.305	27.755	28.205
31	26.415	26.865	27.315	27.765	28.215
32	26.425	26.875	27.325	27.775	28.225
33	26.435	26.885	27.335	27.785	28.235
34	26.445	26.895	27.345	27.795	28.245
35	26.455	26.905	27.355	27.805	28.255
36	26.465	26.915	27.365	27.815	28.265
37	26.475	26.925	27.375	27.825	28.275
38	26.485	26.935	27.385	27.835	28.285
39	26.495	26.945	27.395	27.845	28.295
40	26.505	26.955	27.405	27.855	28.305

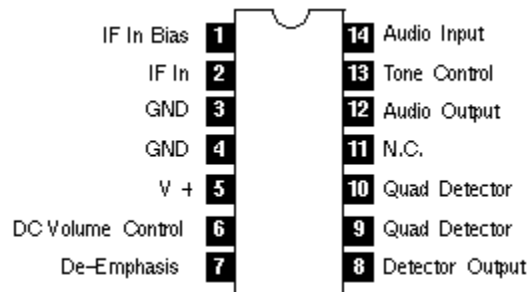
Components

AN252 and AN7140 5 Watt Audio Power Amplifier Similar to NTE1365



Pin	Name	Description
1		Output
2	GND	Ground
3		
4		
5		
6		Input
7	GND	Ground
8		
9	Vcc	Positive Supply Voltage

AN240P FM IF Amplifier and Discriminator Similar to LA1365 KA2101 TA7176P HA1125 LM3065N ULN2165N LSC1008P GL3201 SN7664N

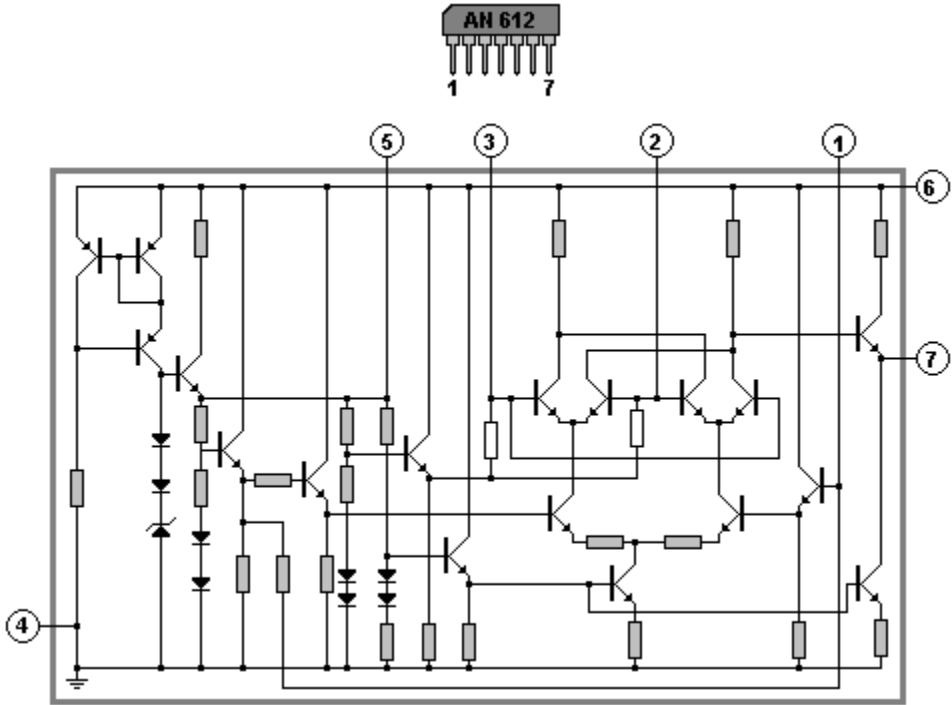


Description:

The AN240P is a versatile device in a 14-Lead DIP type package incorporating IF limiting, detection, electronic attenuation, audio amplifier, and audio driver capabilities.

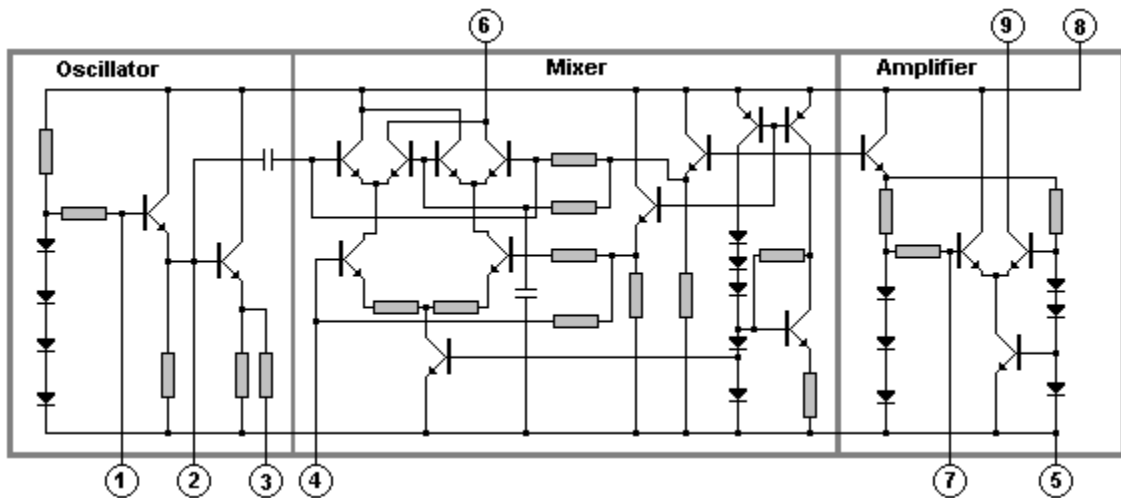
Pin	Name	Description
1	IFB	IF In Bias
2	IFI	IF Input
3	GND	Ground
4	GND	Ground
5	VCC	Positive Supply Voltage
6	DC	DC Volume Control
7	DE	De-Emphasis
8	DO	Detector Output
9	QD	Quad Detector
10	QD	Quad detector
11	NC	No Connection
12	AO	Audio Output
13	TC	Tone Control
14	AI	Audio Input

AN612 Modulator / Demodulator / Mixer
Similar to NTE1249



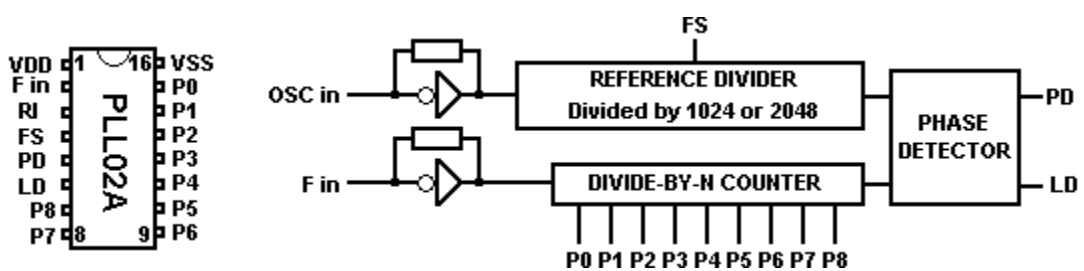
Pin	Name	Description
1		Signal input
2		Bias input
3		Signal input
4	GND	Ground
5		Bias output
6	VCC	Positive Supply Voltage
7		Output

AN103, KIA6410S, KIA7310P, SK3445, TA7310P
Oscillator, Mixer and Amplifier
VCO for Phase Lock Loop (PLL)



Pin	Name	Description
1		Oscillator Input
2		Oscillator Output
3		Oscillator Output - Buffered
4		Mixer Input
5	GND	Ground
6		Mixer Output
7		Amplifier Input
8	Vcc	Positive Supply Voltage - 9 Volt
9		Amplifier Output

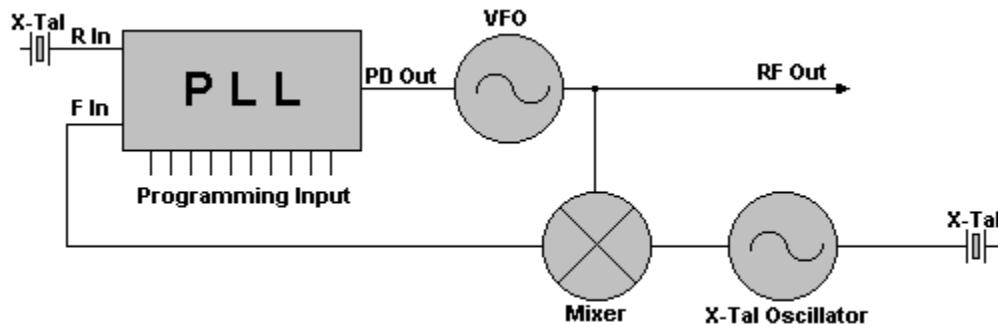
PLL02A
MC145109 MM48141 AN6040 MN6040 SM5109 TC9100
PLL Frequency Synthesizer



Overview

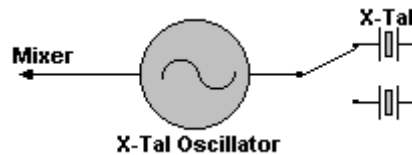
This PLL-circuit use a 9 bit BCD binary programmable divide-by-N counter.

Down-converting of the frequency to the divider



This PLL Circuit use a Mixer and a X-Tal Oscillator to convert the output frequency f_{OUT} to the f_{IN} to the PLL Circuit.

The X-Tal frequency is $f_{XTAL} = f_{OUT} - f_{IN}$



The output frequency can be changed by changing the mixing-xtal or add a new mixing-xtal to the oscillator.

Pin	Name	Description
1	VDD	Positive Power Supply
2	F in	VCO Oscillator Input
3	RI	Reference Oscillator Input (10.240MHz)
4	FS	HIGH=10kHz - LOW=5kHz
5	PD	VCO Voltage Out
6	LD	Loop Detected - HIGH=Locked LOW=Unlocked
7	P8	Programmable input (Binary)
8	P7	Programmable input (Binary)
9	P6	Programmable input (Binary)
10	P5	Programmable input (Binary)
11	P6	Programmable input (Binary)
12	P3	Programmable input (Binary)
13	P2	Programmable input (Binary)
14	P1	Programmable input (Binary)
15	P0	Programmable input (Binary)
16	Vss	Ground

Explanation of pin function terms

V_{CC} or V_{DD} This is the +DC supply voltage which actually provides the operating power to the chip, and is generally in the range of 4-8 volts.

GND or V_{SS} This is the DC power ground connection for the above. NOTE: A chip may be found to have one or more of its functional pins tied to either of the above sources. This may be done to enable a specific function by connecting that function to a "1" or "0", or to prevent an unused function pin from "floating" unconnected to prevent a possible change in its logic state.

RI Reference Oscillator input. This is where the (usually) 10.240 MHz crystal is connected. Crystal pins sometimes called "X" by the manufacturer.

RO Reference Oscillator output. In most chips the crystal is simply connected across RI and RO because the chip has a built-in oscillator circuit which only requires some external capacitors. However some chips such as the PLL02A don't have the built-in oscillator; thus there is no RO pin and an active transistor oscillator is required externally which connects to RI.

1/2R A built-in divided by 2 circuit which provides an output of half the 10.240 MHz Reference Oscillator frequency, or 5.12 MHz. If used, it normally connects to a tripler circuit to provide a 15.360 MHz signal (5.12 MHz x 3) which can be used for loop mixing with the 16 MHz VCO. This mixing provides a low-frequency signal input or downmix to the Programmable Divider.

RB Buffered output of the 10.240 MHz Reference Oscillator. This signal if present can be used for mixing with the 10.695 MHz receiver first IF or mixing with the 16 MHz VCO during TX mode to provide the 455 kHz second IF (RX) or the direct on-channel TX frequency.

F_{IN} Input to the Programmable Divider which is coming from the output of the VCO. Sometimes called "PI" (Programmable Input) or "DI" (Divider Input) by some manufacturers. This is the actual downmix signal or direct VCO signal in the faster chips which will be compared to the Reference Divider's output in the Phase Detector. It is the change in this signal's frequency which forces the Phase Detector and VCO to correct until the loop locks.

DO Phase Detector output. Sometimes called "PO" or "PD_{OUT}" (Phase Output) or "EO" (Error Output) by some manufacturers. This is the output which results from comparing RI and F_{IN}. If the two inputs don't match exactly, this circuit sends a DC correction output to the Loop Filter/VCO until the loop corrects itself and locks up.

LD Lock Detector. Sometimes called "LM" (Lock Monitor) by some manufacturers. This is a second output of the Phase Detector which is used to kill the transmitter (and sometimes the receiver) if the loop is not locked and operating correctly. Some chips have more than one Lock Detector pin and thus you'll sometimes see "LD1" and "LD2" on the specs. When two Lock Detectors are used, their normal outputs are usually opposite logic states; i.e., one LD is normally "1" and the other is normally "0". This is a convenient design feature which allows the manufacturer some flexibility because he can have a choice of inhibiting circuits; some work with LOW outputs, some work with HIGH outputs. Some rigs use both LD pins in their circuits.

MC Misprogram Code Detector. The same idea as the Lock Detector, this is found in the newer ROM chips. If you try to force an illegal program code on the chip, this pin is activated and will kill the transmitter, receiver, or in some cases, call up Ch.9 or Ch.19 instead.

T/R Transmit/Receive switch. This is used to provide the 455 kHz offset for the receiver's second IF stage in dual-conversion AM or FM rigs. Pressing the mike button changes this pin's logic state to its opposite state from the RX Mode. This shifts the ROM controlling the Programmable Divider, and in some chips also shifts the output of the Reference Divider from standard 5 kHz steps to 2.5 kHz steps. The T/R shift is the reason you'll see two different sets of N-Codes and VCO frequencies in a rig's service manual.

NOTE: Some manufacturers' chip spec sheets show a bar (-) above some pin functions, such as LM, T/R, etc. This bar is a digital logic symbol which indicates what state ("1" or "0") that pin is in when activated. For example, the T/R with the bar notation means that the pin is normally HIGH ("1") in the Receive Mode and normally LOW ("0") in the Transmit Mode. /LM means the Lock Monitor is "active LOW", i.e., it is normally HIGH but goes LOW if the loop is unlocked.

FS Frequency Select. This is a feature of some chips which allows them to synthesize frequencies in either 10 kHz CB steps, or 5 kHz steps. Remember, some older chips such as the PLL02A were intended for other uses besides CB, such as VHF marine radios, aircraft radios, etc., where 5 kHz channel spacing is common. In addition, this feature often makes it easier to synthesize SSB frequencies as well as AM/FM although the feature hasn't been used much for this. Depending upon whether the chip has an internal pull-up or pull-down resistor here, it is generally connected to produce 10 kHz CB spacings in the older chips. The newer chips having a T/R shift must use the 5 kHz spacing when the T/R pin is also used. IMPORTANT: You can't use this function to get 5 kHz channel spacings, because the Programmable divider must also change to match the spacing.

AI and AO Active Loop Filter Amplifier input and output. This circuit if present is used to smooth out the digital waveform coming from the Phase Detector, before it's applied to the VCO (See text.) This filter is found in the newer CB-only chips. The older chips (Eg, PLL02A) require external passive filters using capacitors and resistors. In many rigs you'll find that these pins are connected either directly or through a resistor so that they are placed in series between the Phase Detector output pin and the VCO input.

FIL Active filter. We're using this designation in certain very old chips when the exact spec sheets are not available but it's known from studying the chip's wiring in the rig that the pins are in fact part of a loop filter.

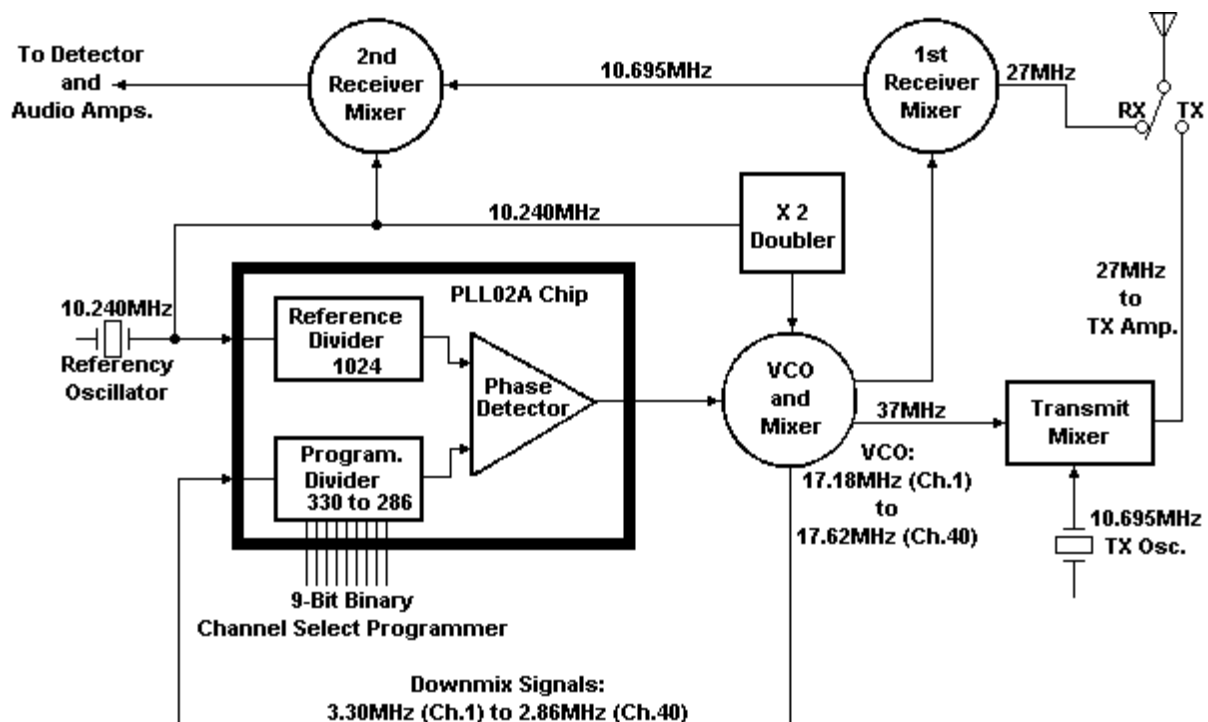
T and Q This is a wave-shaping circuit found in a few NEC chips (uPD2810, uPD2814, uPD2816, and uPD2824). It adds design flexibility but is often not even connected. This circuit consists of an input amplifier and a "flip-flop", and its purpose is to change a sine-wave input (T) to a square-wave output (Q) which is more compatible with digital electronic circuits.

P₀ P₁₀ Program Select pins from Channel Selector switch. (Sometimes called "D" for "Data" rather than "P" for "Program".) These pins control the actual channel selection. They may control selection through straight binary coding, BCD, or ROM. The sub-numbers indicate the weight or significance of each pin. For example if there were 8 programming pins, P1 to P8, P1 would be in the "least significant bit" and P8 would be the "most significant bit". The higher the sub-number, the greater the weight of that pin.

NC No Connection. An unused pin May actually be disconnected inside the chip, or simply not used for that particular rig's PLL circuit.

Modification methods

A TYPICAL PLL SYNTHESIZER



Refer to the figure, which is the PLL circuit of perhaps the most common AM PLL rig ever made. It's been sold under dozens of brand names, and uses the ever-popular PLL02A IC. The SSB and export multimode versions of this circuit are very similar; there are only minor differences relating to the SSB offsets and FMing the VCO.

A PLL design may be categorized very generally by the number of crystals it uses, and by whether its VCO is running on the low or high side of 27 MHz. This particular example is actually the second generation of the PLL02A AM circuit; the original PLL circuit used a total of 3 crystals.

The key to synthesizing all of the required frequencies lies in the Programmable Divider. That's the only PLL section that you can control from the outside world by means of the Channel Selector. Which is where it all starts.

Suppose you choose Ch., 26.965 MHz. When setting Ch.1 the Programmable Divider (PD) receives a very specific set of instructions at all its programming pins, which are directly connected to the Channel Selector. This specific set which we have called its "N-Code", applies only to Ch.1. It's just a number by which any signal appearing at the PD input pin will be divided.

Binary Programming

Refer now to Programming Chart, which summarizes the important operating conditions by specific channel number. A chart like this one is normally included with the radio's service manual. Often though certain facts not directly related to the legal 40-channel operation are left out, so I'll be filling in some missing blanks for you.

Programming Chart for PLL02A

Ch. No.	Frequency (MHz)	"N" digital codes	VCO freq. (MHz)	RX 1st IF freq. (MHz)	P0	P1	P2	P3	P4	P5	P6	P7	P8
1	26.965	330	17.18	37.66	0	1	0	1	0	0	1	0	1
2	26.975	329	17.19	37.67	1	0	0	1	0	0	1	0	1
3	26.985	328	17.20	37.68	0	0	0	1	0	0	1	0	1
4	27.005	326	17.22	37.70	0	1	1	0	0	0	1	0	1
5	27.015	325	17.23	37.71	1	0	1	0	0	0	1	0	1
6	27.025	324	17.24	37.72	0	0	1	0	0	0	1	0	1
7	27.035	323	17.25	37.73	1	1	0	0	0	0	1	0	1
8	27.055	321	17.27	37.75	1	0	0	0	0	0	1	0	1
9	27.065	320	17.28	37.76	0	0	0	0	0	0	1	0	1
10	27.075	319	17.29	37.77	1	1	1	1	1	1	0	0	1
11	27.085	318	17.30	37.78	0	1	1	1	1	1	0	0	1
12	27.105	316	17.32	37.80	0	0	1	1	1	1	0	0	1
13	27.115	315	17.33	37.81	1	1	0	1	1	1	0	0	1
14	27.125	314	17.34	37.82	0	1	0	1	1	1	0	0	1
15	27.135	313	17.35	37.83	1	0	0	1	1	1	0	0	1
16	27.155	311	17.37	37.85	1	1	1	0	1	1	0	0	1
17	27.165	310	17.38	37.86	0	1	1	0	1	1	0	0	1
18	27.175	309	17.39	37.87	1	0	1	0	1	1	0	0	1
19	27.185	308	17.40	37.88	0	0	1	0	1	1	0	0	1
20	27.005	306	17.42	37.90	0	1	0	0	1	1	0	0	1
21	27.215	305	17.43	37.91	1	0	0	0	1	1	0	0	1
22	27.225	304	17.44	37.92	0	0	0	0	1	1	0	0	1
23	27.255	301	17.47	37.95	1	0	1	1	0	1	0	0	1
24	27.235	303	17.45	37.93	1	1	1	1	0	1	0	0	1
25	27.245	302	17.46	37.94	0	1	1	1	0	1	0	0	1
26	27.265	300	17.48	37.96	0	0	1	1	0	1	0	0	1
27	27.275	299	17.49	37.97	1	1	0	1	0	1	0	0	1
28	27.285	298	17.50	37.98	0	1	0	1	0	1	0	0	1
29	27.295	297	17.51	37.99	1	0	0	1	0	1	0	0	1
30	27.305	296	17.52	38.00	0	0	0	1	0	1	0	0	1
31	27.315	295	17.53	38.02	1	1	1	0	0	1	0	0	1
32	27.325	294	17.54	38.03	0	1	1	0	0	1	0	0	1
33	27.335	293	17.55	38.04	1	0	1	0	0	1	0	0	1
34	27.345	292	17.56	38.05	0	0	1	0	0	1	0	0	1
35	27.355	291	17.57	38.06	1	1	0	0	0	1	0	0	1
36	27.365	290	17.58	38.07	0	1	0	0	0	1	0	0	1
37	27.375	289	17.59	38.08	1	0	0	0	0	1	0	0	1
38	27.385	288	17.60	38.09	0	0	0	0	0	1	0	0	1
39	27.395	287	17.61	38.10	1	1	1	1	1	0	0	0	1
40	27.405	286	17.62	38.00	0	1	1	1	1	0	0	0	1

From this chart you see the N-Code for Ch.1 is the number "330", with the numbers progressing down to "286" at Ch.40. This number 330 is the direct result of applying +DC voltages of about 5-10 VDC to certain PLL IC pins while grounding certain others. Thus, two possible voltage choices, and you'll recall that the PLL uses a digital or binary counting system instead of the decimal system people use. In a binary number system each successive chip programming pin or "bit" (*binary digit*) is worth exactly double (or half) that of the pin next to it: 1, 2, 4, 8, 16, etc. Thus each pin can be defined by its Power-of-2. We can also call them "1's bit", "2's bit", "4's bit", etc.

A series of "1"s and "0"s appears in the chart for each of the 40 channels. A "1" means +DC is applied to that pin, and a "0" means that pin is grounded. The pin having the highest binary value or "significance" controls the number of possible channels that can be programmed. In this example the highest Power-of-2 is "256" at Pin 7, which is called the "Host Significant Bit"; the "Least Significant Bit" is Pin 15, which is only worth a "1" in binary. A chart like this showing the logic states of each PLL program pin for each channel is called a "Truth Chart" and is helpful for troubleshooting.

How exactly was the number "330" decided? In Chart you see the truth states for Ch.1 only. Above each PLL program pin are numbers I've labelled "POWERS OF 2", such as 1, 2, 4, on up to 256 which is how a binary counter counts. By adding up the weight or significance of every pin showing a "1", the N-Code is determined. The "0" or grounded pins are always ignored. In this example we have: $256 + 64 + 8 + 2 = 330$.

Go back now to Programming Chart and notice how the logic states for Pin 7 and Pin 8 never change at all for any of the 40 channels. Then look again at Figure 11 and you'll see that those pins are Permanently hard-wired such that Pin 7 is always tied to +DC ("1"), and Pin 8 is always grounded ("0").

You'll often find that many service manuals won't even include these pin states in the Truth Chart because they never change when programming for the legal 40 channels only. This is a case of those missing blanks I'm filling in for you, and you can test this idea by checking the rig's schematic. Compare the total programming pins available to the total number needed for 40 N-Codes! It's an obvious modification source.

The original 18-channel Australian CB service was legally expanded recently to match the 40 FCC channels. Many of the older Aussie rigs, especially those with the Cybernet type PLL02A chassis, are simply American rigs with a limited Channel Selector switch. These can be easily expanded by replacing the 18-position switch and wiring up the unused binary bits on the PLL chip.

For example, the original Australian Ch.1 was 27.015 MHz, which corresponds to U.S. Ch.5. The N-Code here is "325". The N-Code for their old Ch.18 (27-225 MHz) is "304". Reprogramming an old PLL02A rig for N-Codes greater than "325" or less than "304" expands the channels.

This particular IC, the PLL02A., has a total of 9 binary programming pins, pins 7-15. So it has what's called a "9-bit" binary programmer. Some quick math should tell you that the chip has a potential channel capacity of $2^9 - 1$, or 511 channels! ($1+2+4+8+16+32+64+128+256 = 511$). Only 40 channels are used for CB purposes but by proper connection and switching of unused pins, many more frequencies are possible.

The VCO Circuit

Refer back to Figure. This VCO runs in the 17 MHz range, from 17.180 MHz on Ch.1 to 17.62 MHz on Ch.40. The VCO is controlled by an error voltage received from the PD, which is constantly looking for a match at the output of the Reference Divider and Programmable Divider.

The Reference Divider is accurately controlled by a 10.240 MHz crystal oscillator whose signal is divided down digitally by 1,024 to produce the required 10 kHz channel spacings. If the Programmable Divider should also happen to output the exact same 10 kHz the result would be perfect; no correction from the PD, and the loop would be locked.

What would it take to produce a perfect 10 kHz output from the Programmable Divider? We've already seen that the Programmable Divider is set to divide any signal it sees by the number 330. For example if it should see a signal of exactly 3.30 MHz at its input, the resulting output would be $3.30 \text{ MHz} \div 330 = 10 \text{ kHz}$. So if we can somehow get an input signal of 3.30 MHz, everything will fall perfectly into place.

Loop Mixing

It so happens there's a very easy way to do this by cleverly borrowing a bit of existing circuitry. If some 10.240 MHz energy from the Reference Divider is taken off and passed through a tuned Doubler stage, the result would be $2 \times 10.240 = 20.480 \text{ MHz}$. Here's where that very important loop mixing principle enters; by mixing the 20.480 MHz signal with the Ch.1 VCO signal of 17.180 MHz, sum and difference frequencies are generated. The sum is $20.480 + 17.180 = 37.660 \text{ MHz}$. The difference is $20.480 - 17.180 = 3.30 \text{ MHz}$. Just what's needed to lock the loop. And the 37.660 MHz energy isn't wasted either; it's used as the high-side mixer injection signal that produces the first- RX IF: $37.660 - \text{incoming } 26.965 = 10.695 \text{ MHz IF}$.

Phase Detector Correction

What happens if the mixing product to the Programmable Divider isn't exactly 3.30 MHz? Let's find out. Since the N-Code is 330, a signal of other than precisely 3.30 MHz would produce a slightly different output to the PD. For example a signal of say, 3.10 MHz results in $3.10 \text{ MHz} \div 330 = 9.39393 \text{ KHz}$. The PD will sense this error and try to correct it by applying a DC voltage to the VCO. This correction voltage will drive the VCO up or down slightly in frequency, with the PD always comparing

its two inputs, until an exact match occurs again. While this appears to be just a trial-and-error process, the whole thing happens in the time it takes you to change from Ch.1 to Ch.2!

Receiver IF's

We've now seen how the Ch.1 PLL mixer signal of 37.660 MHz provides the RX first IF injection. Now note from Figure that we can make even a third clever use of the 10.240 MHz Reference Oscillator. By mixing that with the 10.695 MHz first IF, the result will be $10.695 - 10.240 = 455$ kHz, the second RX IF. (The sum product is ignored.) Pretty smart these engineers...

Almost all AM or FM CBs use this method of dual-conversion for their receivers. It's also commonly used in car radios, scanners, FM stereos, etc. where a lot of the circuit hardware already existed.

Transmitter Section

In this example the TX carrier frequency is produced very simply. A local oscillator of 10.695 MHz is also mixed with the 37.660 MHz Ch.1 PLL output. The difference is $37.660 - 10.695 = 26.965$ MHz, which is then coupled through various tuned circuits and the standard RF amplifier chain.

The Truth Chart is the most important first step in determining how a modification can be made. or if it can be made. Let's examine it in greater detail now.

The example just described was a very easy PLL circuit using the binary type of programming code. It's quite possible for the same chip to have different N-Codes depending upon how many crystals are used, or if it's AM or AM/SSB. The preceding circuit is one of several used with the PLL02A; this is the "2-crystal AM" loop. It used N-Codes from 330 Ch.1 to 286 Ch.40, because those were the numbers needed for exact division, correct IFs, etc. An earlier AM loop used 3 crystals and N-Codes which went up, from 224 Ch.1 to 268 Ch.40. And in the ever-popular SSB chassis the N-Codes were 255 down to 211.

Notice that these N-Codes can go up or down with increasing channel numbers. It depends on the VCO design.

Those Infamous Channel "Skips"

Meanwhile, let's return to a portion of Programming Chart to study some of its other features. Programming Chart is a simplification showing only the channel number, frequency, and N-Codes from the original full chart.

Notice anything unusual in the N-Code sequence going from Ch.1 to Ch.40? The codes aren't all consecutive and skip some points that aren't legal CB frequencies. For example, Ch.3 is 26.985 MHz, and Ch.4 is 27.005 MHz. So what the heck happened to 26.995 MHz? Gee, it's not a legal FCC channel. This is known to CB'ers as an "A" channel, in this case, Ch.3A. There are also skips at Channels 7, 11, 15, and 19. And Ch.23, Ch.24, and Ch.25 of the FCC CB band are assigned out of sequence. (That's left over from the old 23-channel days.)

What this means is that all the N-Codes as well as VCO and mixer frequencies are also out of order in the chart. Many European countries that originally allowed only 22 channels simply adopted the American scheme exactly for those first 22 channels. Australia had 18 channels whose numbers didn't correspond to American/EEC numbers, but many of the actual frequencies were the same. And the UK originally assigned 40 consecutive channels with no skips at all. Remember these points when studying an older model's Truth Chart, or you may think your math is wrong when it really isn't.

LOOP MIXER MODIFICATIONS

Now let's examine the second possible conversion method, that of changing the Loop Mixer frequency itself. This is one of the easiest ways to modify a PLL circuit having a downmix signal. A few chips like the PLL02A can be modified by either of the programming pin change or downmix change methods. The choice depends upon the total number of extra channels desired, and how much modification work you're willing to do.

Changing the mixer crystal is most commonly done when jumping up to the 10-Meter HAM band. Since there's no intention of ever using the rig again for CB, it can be permanently retuned at the higher frequency. But many of you are still expanding from the CB band and adding an extra 40 or 80 channels. The European models like those from HAM International, Major, and SuperStar were basically just American model with the extra mixing crystals already there.