KENWOOD

SERVICE MANUAL

DG-5

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DIGITAL DISPLAY

CONTENTS

SPECIFICATIONS

Countable Digits	Six decimal digits.
Type	Light-emitting diode frequency display with hold memory.

DISPLAY (in combination with TS-520S)

Frequency Range	All TS-520S transmit and receive channel frequencies as precise as 0.1 kHz digit.
Accuracy	Reference time ±0.2 count.
Input	TS-520S heteryodne local oscillator signal, VFO signal, and all carrier oscillator signals.

COUNTER

Measurable Frequency Range	100 Hz to 40 MHz
Input Sensitivity (at Room Temperature)	50 mV r.m.s. at 10 kHz to 10 MHz 200 mV r.m.s. at 100 Hz to 40 MHz
Absolute Max. Input Level	200V (DC + peak). 5V r.m.s. (continuous at 100 Hz to 40 MHz).
Input Impedance	Approx. 5 kΩ, less than 22pF.
Accuracy	Reference time ±0.1 count.
Count Time	0.1 sec.
Least Significant Digit	0.1 kHz.

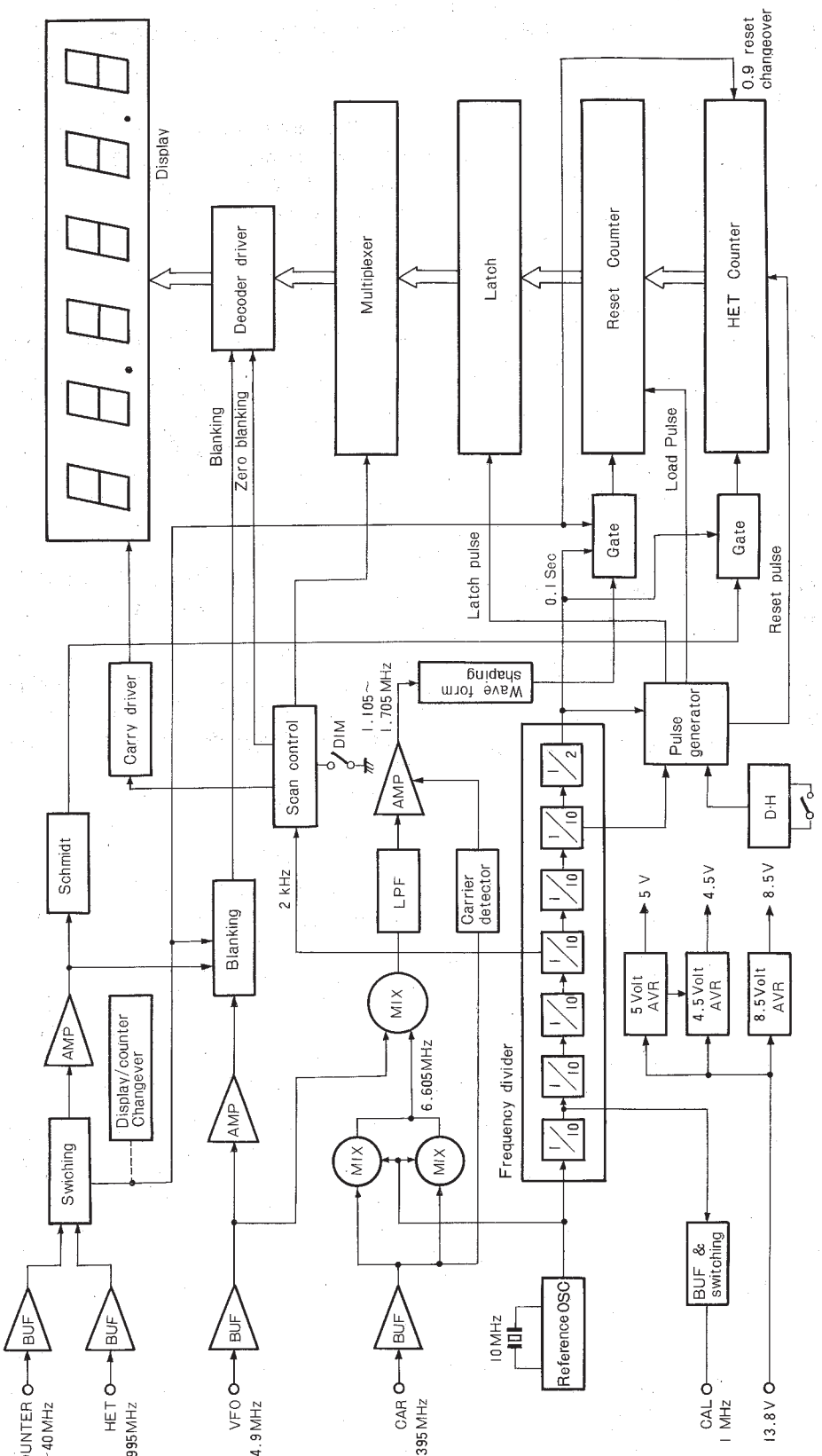
REFERENCE TIME

Frequency	10 MHz
Error	Less than 1×10^{-5} (at room temperature).
Temperature Stability	Greater than 3×10^{-5} (at 0°C to +50°C).
Aging Rate	Lower than 1×10^{-6}/month (at room temperature).

GENERAL

Ambient Temperature	−10°C to +50°C.
Power	Supplied from TS-520S.
External Power	12 to 16V, 0.9A DC (with 13.8V reference).
Dimensions	167mm (6-9/16") wide × 260 mm (10-1/64") [268mm (10-1/16"), max.] deep × (1-37/64") [43mm (1-11/16"), max.] high
Net Weight	1.27 kg (2.8 lbs.)
Semiconductors Used	42 ICs, 31 transistors, 19 diodes, 3 two-digit LEDs, and 1 LED indicator.

BLOCK DIAGRAM



GENERAL

1. TS-520S, frequency perfectly readable in units of 100 Hz

All local oscillation frequencies (heterodyne, VFO, carrier) supplied from the TS-520S are used to synthesize display frequencies. The true transmitting/receiving frequency is accurately displayed in units of 100Hz. No corrections by band or mode changeover, calibration, etc., are required.

2. Can be used as a frequency counter (up to 40MHz) by a single-touch changeover motion

With the operation of a switch on the front panel the DG-5 can be used as a frequency counter which covers frequencies up to 40MHz. This changeover is acomprished by a single touch. In this setting it functions as a measuring instrument, and in this case also the smallest unit of measured frequency is 100Hz.

3. Thin construction for compact combination with the master unit transceiver

The total thickness (with rubber legs) is only 43mm, and the width is 167mm. Because of its very thin construction, when combined with the master unit (transceiver) it gives the appearance of a single unit, and the esthetic quality is therefore good.

4. Large, easily discernible LED frequency display, with dimmer switch

Since a large, easily discernible LED display is used, this unit can be used as an independent display or a frequency counter. The LED's are provided with color filters and the dimmer switch can be used to reduce the LED brightness. This permits comfortable operation without any accompanying fatigue even when it has been operated for a long time or at night.

5. Easy connection with the master unit

By the use of the modified digital unit DK-520, it can be connected with either the TS-520. It can be easily connected with the TS-520S, through the 3-pin plug cord and the power cord. When making connection with the TS-520, the exclusively modified digital unit DK-520 must be added.

Easy checking and repair are possible, facilitated by the completely non-wire system.

The DG-5 is composed of the main printed circuit board (counter unit), the display (display unit), the right and left frames, and the front and rear panels. This construction, devoid of wiring, permits very simple checking and repair.

FUNCTIONAL DESCRIPTION

1. Configuration

The DG-5 is connected with its master unit, TS-520S for the main purpose of digital display of the transmitting of receiving frequency. By changing over, it is also available as a frequency counter of 100Hz to 40MHz. The thin body (43mm in height and 167mm in width) and the large digit size (approx. 10 x 7mm) utilizing 6 large LED's provide a very satisfactory external display.

The electrical configuration of this unit is as shown in the block diagram on page 4. The unit consists mainly of the input terminal, the buffer amplifier mixer unit, the digital counter, and the display unit. Power is supplied from the master unit, TS-520S.

For frequency display performance, the 3 types of local oscillation signals — heterodyne (HET), VFO, and carrier (CAR) — are taken from the master unit and mixed with the 10MHz source from the counter's reference oscillator. Since an additional 2 counters are employed and the frequency display component is synthesized in the analog/digital mode, undesirable effects upon the master unit such as spurious disturbance can be minimized.

For frequency counter performance the input circuit is changed over to the counter terminal by means of the diode switch, and the input signal is counted and displayed through the HET counter indicated in the block diagram.

In the counter section the standard frequency of 10MHz is frequency-divided down to 5Hz to obtain a reference gate time of 0.1 second. Though the smallest unit of display is 100Hz, the counter counts the frequency in units of 10Hz; therefore there is minimal fluctuation in the 100Hz units. Since the latch interval is 0.2 second, fluctuation is minimal during dial operation. This latch interval is correct for the operating speed. Each large-size LED on the display unit is provided with both a violet and a light smoke filter with transmission rates of 82%, thus providing a comfortable tone and an adequate luminous intensity.

2. Principle of Display Frequency Synthesis

In order to compose a frequency component for display, the DG-5 takes the HET (heterodyne), VFO, and CAR (carrier) frequencies from the master unit. In addition to the analog unit, the DG-5 employs 2 digital counter circuits for the digital synthesis, by which the desired display signal is obtained.

In the TS-520S the 3 local oscillation frequencies are mixed to synthesize the transmitting/receiving frequency under the following conditions:

HET − (VFO + CAR) ..... (1)

Though the display frequency can be composed by the same process, generation of the same frequency as that in the master unit is undesirable because of the existence of spurious disturbance. Hence a digital process is added in order not to produce a frequency which is analogously the same as that of the master unit. Fig. 1 shows the DG-5 frequency configuration through an example of the 14MHz band. The following explanation follows those actual figures.

The HET signal of 22.895MHz passes through the 0.1 second gate and is counted by the HET counter in units of 10Hz. In the HET counter the reset signal is applied to the "R9" terminal only for a unit of 10MHz and the output is reset at "9." Therefore, with an initial state of 9 in the

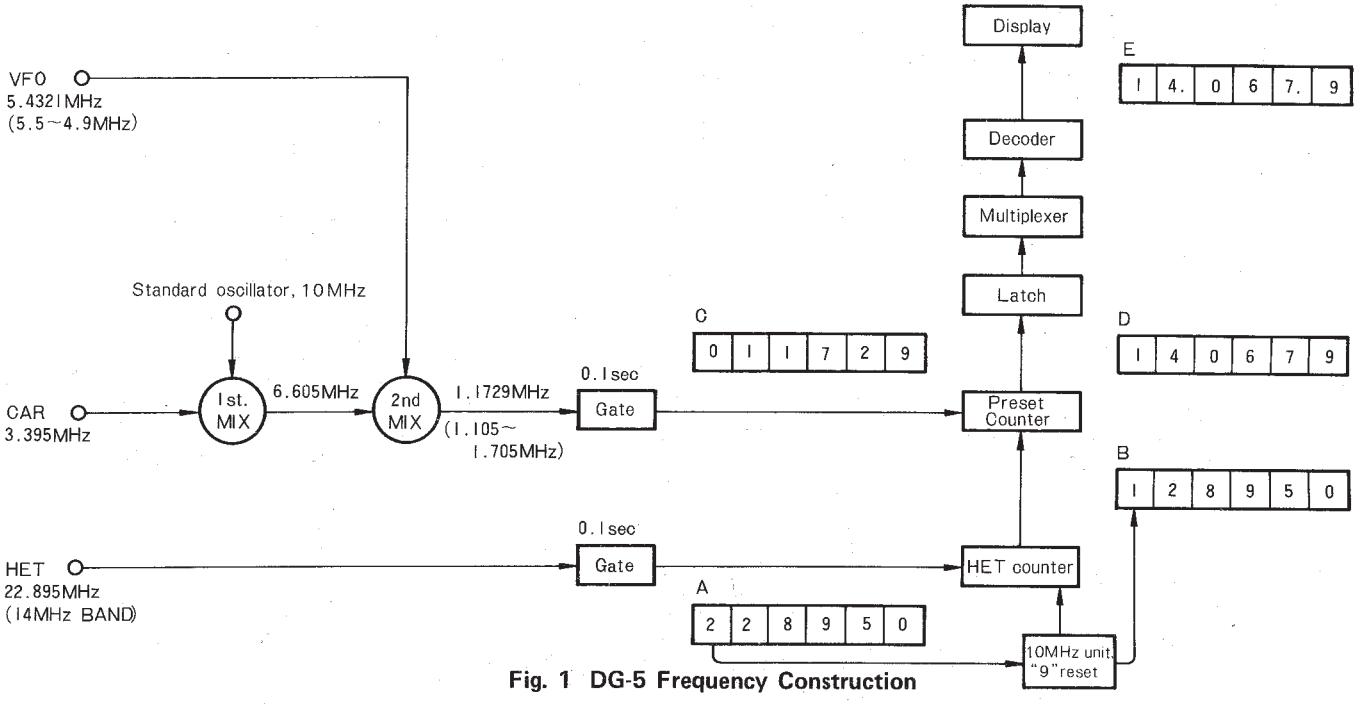


Fig. 1 DG-5 Frequency Construction

FUNCTIONAL DESCRIPTION

10MHz unit, each time one pulse inters, the output shows a digit which is always smaller by one than the number of input pulses. That is, as shown in Fig. 1, the 10MHz unit of the HET counter input A 2 2 8 9 5 0 loses "1" and the output B is shown as 1 2 8 9 5 0 . The squares show the input/output component of each digital unit ranging from the 10MHz unit to the 100Hz unit for the decimal counter. The respective digits of the output B of the HET counter are preset by the preset counters that are connected in series with the respective digital units.

The CAR signal of 3.395MH z is mixed with the reference oscillator signal of 10MHz at the first mixer and is converted to a frequency of 6.605MHz. This signal is further mixed with the VFO signal (5.4321MHz in Fig. 1) at the second mixer and is finally converted to a frequency of 1.1729MHz. This signal passes through another gate circuit and is counted by the preset counter in units of 10Hz.

In addition to the signal input terminal, the preset counter is provided with the preset input terminal to which an external BCD signal is applied to preset the initial state of the counter to an arbitrary value. The output is the sum of this preset value and the number of input signal pulses. In the DG-5 the output B of the HET counter 1 2 8 9 5 0 is preset by the preset counter. Therefore the preset counter output is the output D 1 4 0 6 7 9 , which is the sum of the preset value B and the input signal counter component C 0 1 1 7 2 9. This output D further passes through the latch, multiplexer, and decoder, and the correct frequency is indicated at the display E in the form of (14.067.9). Thus the display frequency synthesizing process in the DG-5 is as follows:

$$(HET - 10) + (10 - CAR) - VFO = HET - (VFO + CAR) \quad \cdots\cdots (2)$$

The above result is identical with the frequency relationship in the master unit, and the displayed frequency exactly coincides with the frequency of the master unit. The difference is that the analog block does not generate any frequency which causes direct interference with the transmitting/receiving frequency, IF frequency, etc. of the master unit. Therefore, even when the DG-5 is connected, the occurrence of direct beat trouble, spurious disturbance, etc., can be avoided.

3. Frequency Counter Operation

The frequency counter of the DG-5 is fundamentally used to read out the frequency of a measured signal which has been inputted to the HET counter. Fig. 2 shows the basic section. The signal to be measured is applied to the COUNT IN terminal on the rear panel. After passing through the buffer circuit, either the HET signal input or the signal to be measured is selected by the diode switch. The circuit after the wide-band amplifier is used in common with the HET signal. The signal finally enters the HET counter.

Though the HET counter is actuated by resetting the 10MHz unit at "9" during display operation, it operates in the "0" reset mode during frequency counter operation so that the input pulses can be directly indicated as an output.

In this case the preset counter is merely used to send out the HET counter preset value immediately to the output circuit. Therefore the gate circuit before the input terminal is switched over so that the signal input can be interrupted. Thus the frequency counter operation is equivalent to the condition that the frequency counted at the HET counter is directly displayed.

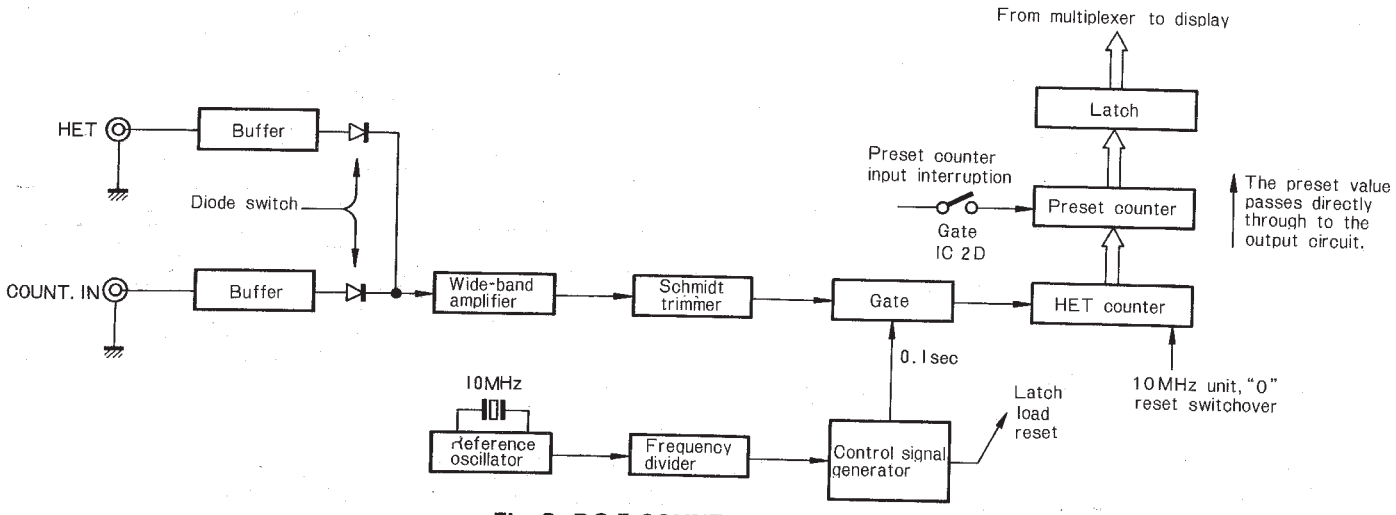


Fig. 2 DG-5 COUNTER Operation

CIRCUIT DESCRIPTION

1. HET/Counter Amplifier

Input Circuit

The HET terminal receives an HET signal of 10.695 ~ 37.995MHz from the HET oscillator of the TS-520S through the 75Ω coaxial cable. Therefore the terminal resistor 82Ω is connected and the HET terminal is connected to Q2 to obtain a buffer effect. The Q2 amplifier is arranged in an emitter follower connection.

The COUNT. IN terminal is also connected to the emitter follower type buffer amplifier consisting of Q1 to avoid being affected by the external circuit which is connected with a measuring cable. Since the frequency to be handled may range widely from 100Hz to 40MHz and the internal circuit must be protected against excessive input, there is an input protective circuit as shown in the dotted-line box in Fig. 3. This input protective circuit consists of the CR series-parallel circuit and the diode clamper. As the input voltage begins to increase in the initial state of operation, Q1 is applied with a voltage which is divided by R1 and R2 together with the input impedance (about 5kΩ) in the rear stage. If this voltage is higher than the potential difference (about 0.65V) between diodes D1 and D2, current begins to flow into the diode and a higher voltage above the threshould level cannot be applied to Q1. This phenomenon is inevitably a protective operation for the input circuit. The capacitor C1 is used for DC interruption, while capacitor C2 is used to prevent reduction in sensitivity by permitting the flow of high frequencies through the resistor R2, since the sensitivity will suddenly decrease at 10MHz or more because of the existence of the input capacitor. The limit of input voltage is 50 ~ 100V in a low-frequency band not higher than 2MHz. Since there is a decrease in the series resistance component at higher frequencies due to the effect of C2, withstand voltage decreases at the rate of 6dB/oct and is finally about 5 volts at 40MHz. If this limit is exceeded, the resistor R1 is designed to burn out.

Wide Band Amplifier

The input signal passing through the emitter follower circuit and the diode switch is amplified at the wide-band amplifier consisting of Q3 ~ Q5. Since this block disposes of a very wide frequency range of 100Hz ~ 40MHz, the transistor Q4 composes an amplifier with a collector load impedance of 470Ω, which is very low. At the same time both the input and output circuits are connected with the directly-coupled emitter follower circuits to avoid the effect of the former and latter stages. Thus the resultant gain is about 30 to 35dB between TP1 and TP2 throughout the frequency range. This amplifier has the input-output characteristic shown in Fig. 4, and in actual counting conditions it operates in an almost saturated zone. Therefore the apparent gain between the HET terminal and the TP2 is 15 to 20dB during actual operation when measured with a voltmeter and with the master unit connected.

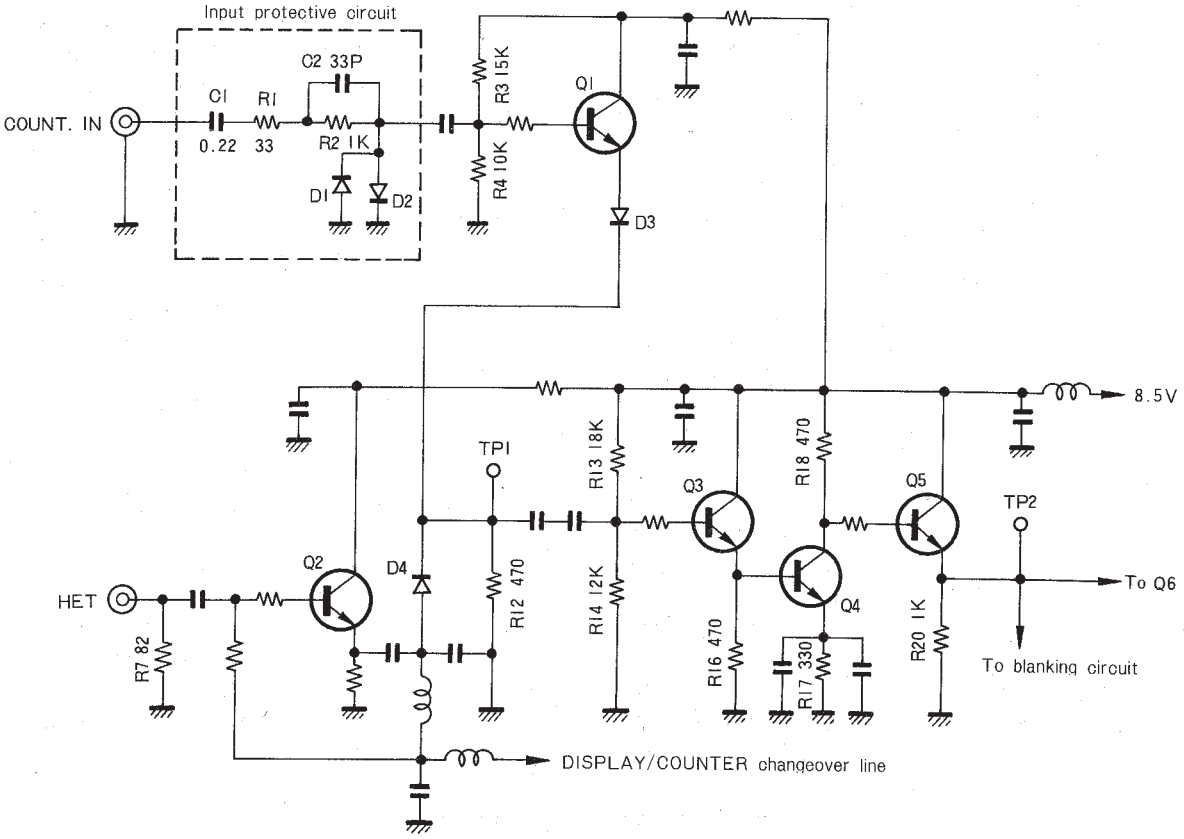


Fig. 3 HET/COUNTER AMP

CIRCUIT DESCRIPTION

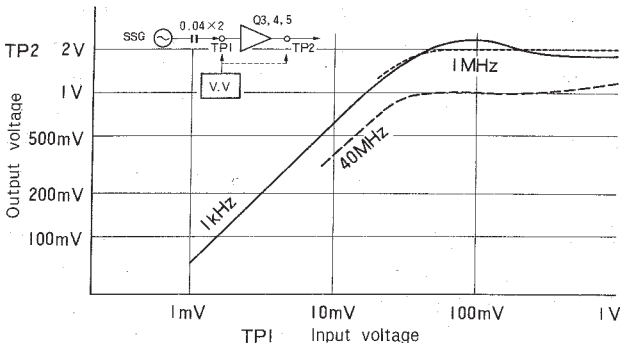


Fig. 4 Characteristic of Wide Band Amplifier

A/D Coupling Circuit and Schmidt Trigger Circuit

The wave form of a sufficiently amplified signal is pulse-shaped by the circuit shown in Fig. 5 and is then applied to the counter gate circuit. The transistor Q6 is a coupling circuit located between the analog system of the preceding stages and the 5V power supply system of the TTL. IC in the successive stages. Since the H and L level values of the TTL. IC are restricted by the power supply voltage of 5 volts, the power supply voltage of Q6 is also 5V. The Q6 circuit is arranged in an emitter follower connection since its output impedance must be low because of the characteristic requirement of the Schmidt circuit in the next stage.

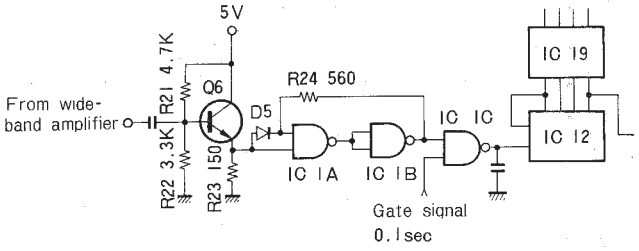


Fig. 5 Wave Form Shaping Circuit

The circuit consisting of IC1A ~ IC1B and D5 is Schmidt trigger or the wave form shaping circuit, which converts a gently changing wave form like a sine wave into a spulse wave. The counter circuit counts the number of input pulses. Since TTL. IC is arranged to operate under the restriction that the L level is 0.8V or below and the H level is 2.0V or above, the time necessary for switching over from L to H or H to L will increase if the rising and falling modes of the pulses are too gentle. If any noise enters during this time it will be counted as a pulse, thus leading to a mis-display.

In the Schmidt circuit the output from Q6 is applied to the 2-input NAND circuit. This output is directly applied to one gate of the 2-input NAD circuit, and simultaneously it is applied to the other gate through the diode D5. In this case the output is not reversed unless both the 2 inputs attain the H level at the IC1A. Therefore, as shown in Fig. 6, the IC1A is not triggered unless the input voltage is

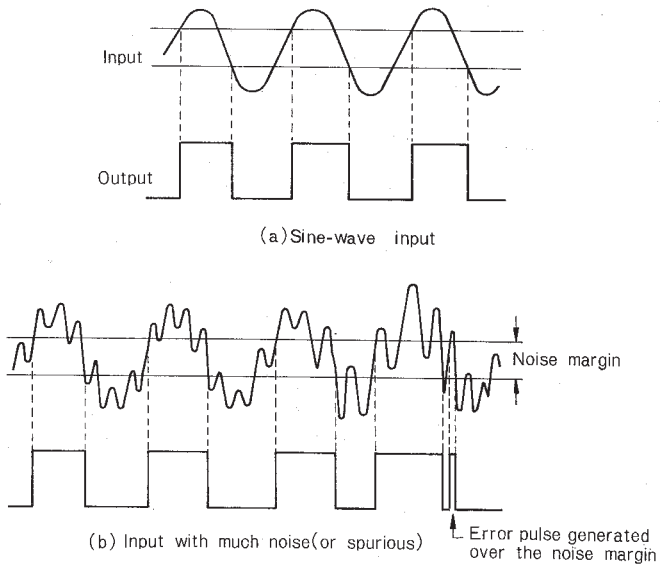


Fig. 6 Operation of Schmidt Trigger Circuit

higher than the sum of the D5 terminal voltage (about 0.65V) and the threshold voltage (a voltage at which the output suddenly changes from H to L, i.e. about 1.3V in terms of input voltage). The output caused as a result of reversal from H to L is again reversed by IC1B from L to H. The voltage reversed from L to H is positively fed back through the resistor R24 to the input gate of the first stage, which is provided with D5. Therefore, with the entry of even a gentle input a snap action takes place and a sharp rising mode is obtained. The falling mode is obtained similarly, but in the completely reverse order. In other words, this circuit has a hysteresis characteristic since there is a time lag in rising or falling performance by the amount of the terminal voltage component of D5. This voltage component is effective as a noise margin, as shown in Fig. 6.

The IC1C is a signal gate circuit for the HET counter. This circuit permits the flow of pulses from the Schmidt circuit while there is a 0.1-second gate signal generated by the standard oscillator. For this 0.1 second the HET counter counts the number of pulses which have passed the gate.

DISPLAY/COUNTER Changeover Circuit

Both HET and COUNTER. IN signals are fed to the HET counter. Therefore either signal is selected with the changeover switch on the front panel. Fig. 7 shows an overall diagram of the DISPLAY/COUNTER changeover circuit. Changing over is performed by the aid of the output diode switches of the input emitter follower circuit, the input gate of the preset counter, the "9" and "0" reset circuits for the 10MHz unit of the HET counter, and the blanking ON/OFF gate.

CIRCUIT DESCRIPTION

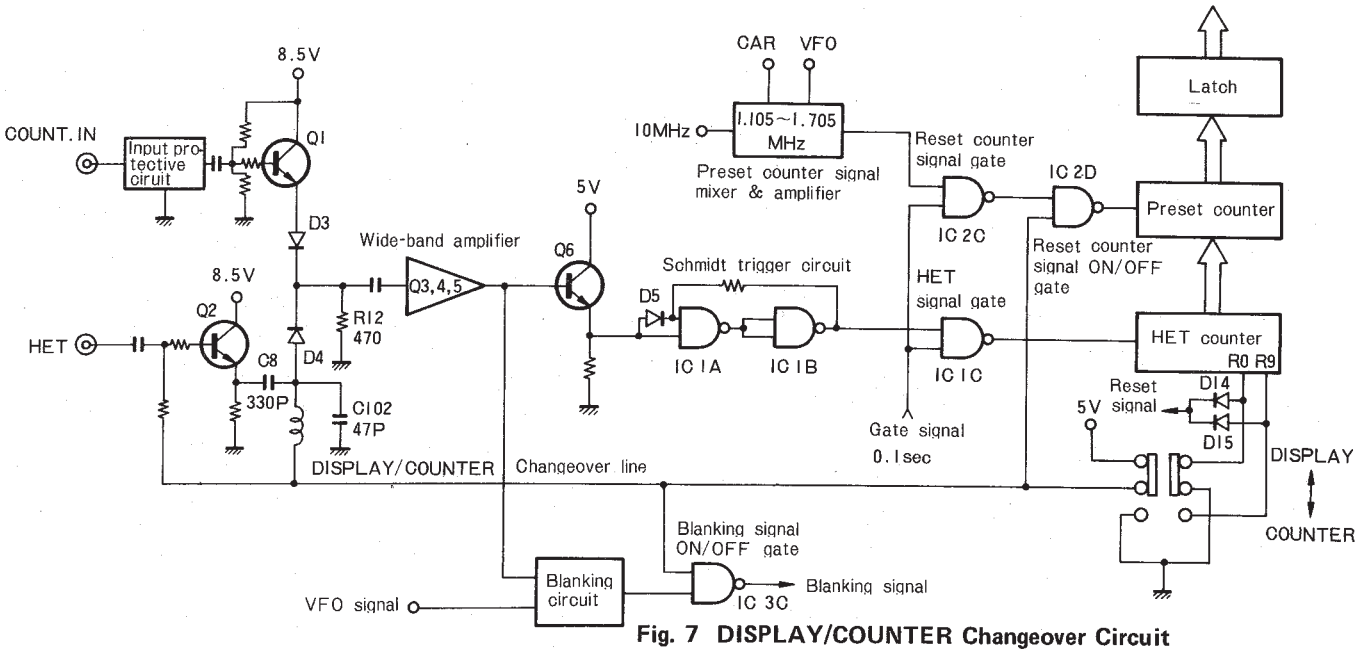


Fig. 7 DISPLAY/COUNTER Changeover Circuit

With 5 volts applied to the desired side, a bias voltage is applied to Q2 and the diode D4 is turned on to change over the input emitter follower circuit to the HET side. If the line voltage decreases to zero the bias disappears from Q2, causing D4 to turn off and D3 to turn on. Thus Q1 functions and the circuit is changed over to the COUNTER side. The preset counter and blanking ON/OFF gates are switched off if their gate voltages become zero. At that time both the preset counter and blanking signals are interrupted and the circuit is changed over to the COUNTER side. In the HET counter circuit for the 10MHz unit the resistor R0 is grounded in the DISPLAY mode and the resistor R9 is grounded in the COUNTER mode so that the reset signal cannot be applied to their respective reset terminals.

2. CAR/VFO Mixer and Amplifier

Input Buffer

In order to avoid the effectsof the preceding and succeeding stages, the VFO and CAR terminals are also provided with emitter follower type buffer amplifiers just as the HET terminal is. In particular, since the VFO buffer has the function of preventing reverse leakage into the master unit, it has 2 emitter follower stages in a Darlington connection.

CAR Mixer

The 3.395MHz carrier is mixed here with the 10MHz signal to obtain a 6.605MHz signal. If the input frequency leaks into the output terminal, it will give rise to a spurious component which causes of miscounting. Therefore Q16 and Q17 together with T1 and T2 are arranged to compose a balanced mixer which cancels the components in the same phase. However, this type of mixer must not receive too much input; both carrier and 10MHz signals must be maintained at about 100mV. Taking the selectivity of the output coil T2 into account, the suppression level is about 40dB.

VFO Mixer and Signal Amplifier

The 6.605MHz signal is mixed at Q18 with the VFO signal of 5.5 ~ 4.9MHz. The mixed output passes through the low-pass filter and is converted into a frequency ranging from 1.105 to 1.705MHz. This circuit is an ordinary FET mixer and the output from the low-pass filter is the lower side band only. Since the mixer output voltage is only 0.1 to 0.2V, it must be amplified by Q19 and Q20 to a level at which the TTL. IC can be actuated. The Q19 is an amplifier of about 20dB, while the Q20 is a coupling emitter follower circuit for the TTL. IC. The Q19 power supply is obtained from the carrier switching circuit. If there is no carrier input, the source voltage is interrupted and the effect of the amplifier disappears. Thus irregular and abnormal display due to leakage from the mixer can be avoided.

Signal Gate Circuit

The sufficiently amplified signal is shaped into a pulse wave through the inverter of IC2B and is then applied to the preset counter signal gate of IC2B. In this case the standard gate signal is applied for 0.1 second, and during this period the signal pulses are sent to the preset counter through the DISPLAY/COUNTER changeover gate. At this gate, a signal enters when a 5V input is applied to another input terminal of IC2B (in the display mode). The signal is interrupted when this terminal is grounded (in the counter mode).

CIRCUIT DESCRIPTION

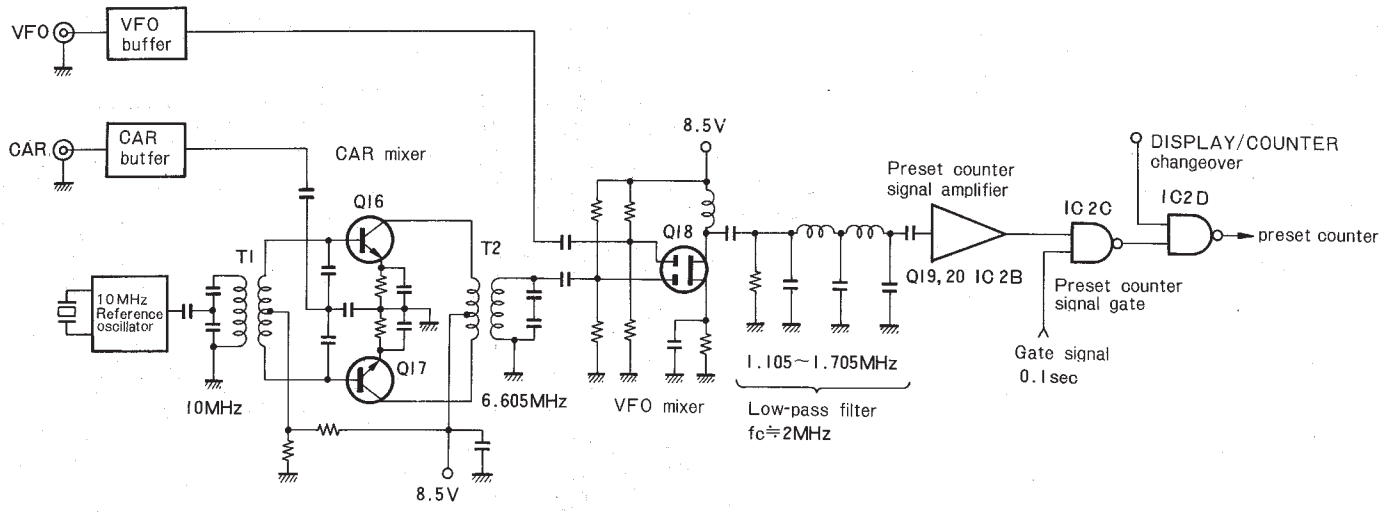


Fig. 8 CAR/VFO Mixer & Amplifier

3. Reference Oscillator and Calibration Circuit

Reference Oscillator

The reference oscillator employs a 10MHz quartz crystal unit. Since the counter display accuracy depends on the accuracy of the 0.1-second standard time which is obtained by frequency division, the reference oscillator is so to speak the heart of the counter. The quartz crystal unit used here is obtained by cutting to obtain a zero thermal coefficient, and its accuracy is guaranteed to the 100Hz unit in actual use.

As shown in Fig. 9, the oscillating circuit is a Colpitts circuit which generates a sine wave to be fed to the CAR mixer. The Q22 buffer circuit is installed in front of the IC block, and output is supplied to the frequency divider to make a standard time of 0.1 second.

Calibration Circuit

The reference oscillator is of no use if it does not oscillate at 10MHz exactly. For calibration the standard waves of WWV, etc. are the most accurate and handy frequency sources. Since the TS-520S, can receive a standard wave of 15MHz (the TS-520, for 10MHz), the output circuit of the reference oscillator is extracted for calibration with the standard wave in combination with the radio receiver. This mission is accomplished by the calibration circuit consisting of Q23 and therafter. Since the standard wave to be received is 15MHz or 10MHz, the oscillator output is divided into 1/10 and 1MHz is taken out. Also in this case the wave form is rectangular with excessive harmonics, and this is favorable for calibration.

Q23 and D13 compose a buffer circuit for calibration output. This circuit also functions as a switch, and it does not operate unless the attached coaxial cable is connected to the CAL output terminal and the receiver calibration input terminal (X-VERTER IN terminal for the TS-520). If nothing is connected to the CAL output terminal of a circuit, as shown in Fig. 9, the potential at the Q23 emitter and the D13 cathode is unfixed and the source voltage of 8.5V is applied directly. Simultaneously the Q23 collector and the D13 anode are applied with a potential which is produced from the source voltage divided by R92 and R93. In other words, Q23 and D13 are reversely biased and a cut-off condition is maintained. Thus the 1MHz output does not appear at the CAL terminal. When the separately furnished calibration connection cable is connected to the X-VERTER IN terminal of the master unit, the DC component at this terminal is grounded through the coil. Therefore in this case the emitter of Q23 is grounded and Q23 is turned on. Simultaneously D13 is turned on through R19, which is a current limiting resistor. Thus the 1MHz output (including harmonics) appears at the CAL terminal and is fed to the receiver.

Fine frequency adjustment for calibration is made by the trimmer capacitor TC1 of the reference oscillator. When the frequency is adjusted with a more accurate frequency counter (meaningful only if its accuracy is more than 10^{-7}), the CAL terminal is short-circuiited and the counter is connected to the test point TP9.

CIRCUIT DESCRIPTION

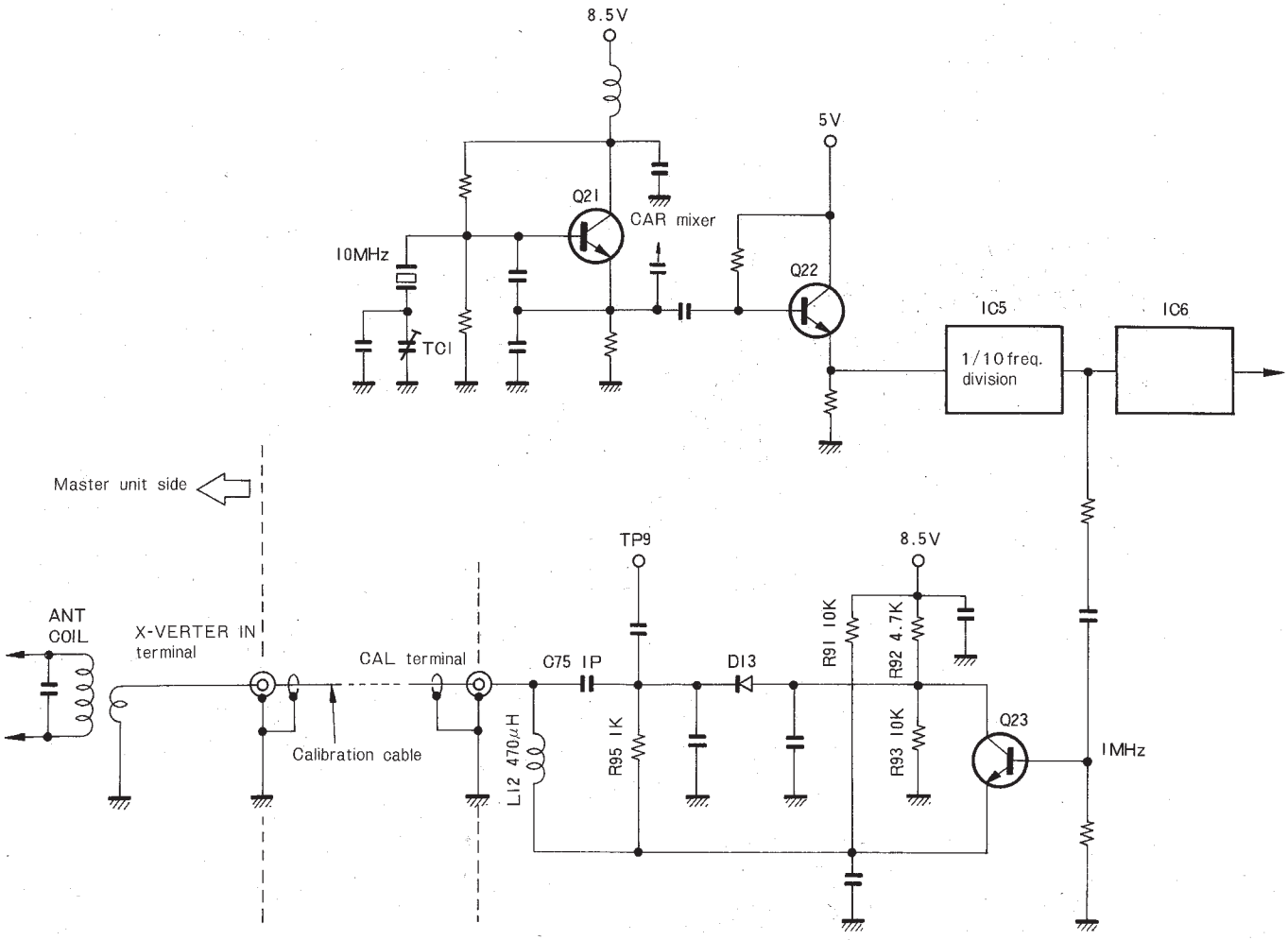


Fig. 9 Reference Oscillator & Calibrate Circuit

4. Blanking Circuit and Carrier Switching Circuit

Local OSC. Input Detection

While the DG-5 is in operation in the DISPLAY mode, it is fed the three outputs of HET, VFO, and CAR from the master unit. However the supply of local oscillation output may be interrupted due to trouble in the master unit, cable or terminal malfunction, misconnection, or to setting the FUNCTION and BAND switches of the master unit at incorrect positions. If the display is unchanged in such a case it will give unstable and meaningless indications due to intrusion of noise. Therefore the DG-5 is devised to detect the presence of the outputs, HET, VFO, and CAR. If there is no HET or VFO input, a blanking signal is generated to delete the indication on the display (except for the decimal point). If the CAR input disappears, the source voltage is removed from the preset counter signal amplifier of Q19 in Fig. 8 so that the display cannot change.

Blanking Circuit

When either the HET or VFO input from the master unit disapperars, the blanking circuit sends out a blanking signal to the decoder IC to blank out the dispplay. Both HET and VFO signals are amplified in the circuit in Fig. 10 and the output is detected and rectified by the iodes. If the signal is present, Q7 and Q11 are turned on by the effect of the rectified voltage. The 2 inputs from IC2A are at the H level and the output is at the L level, the IC3C output is maintained at the H level regardless of the other input level This output is applied to the BI terminal of the decoder IC39 through the blanking switch S3. As shown in the function table of Fig. 25 for SN74247N, blanking is not performed at the H level under normal operating conditions.

When either the HET Or VFO signal disappears, the IC2A input on the no-signal side is at the L level and the output is turned to the H level. Therefore in the DISPLAY

CIRCUIT DESCRIPTION

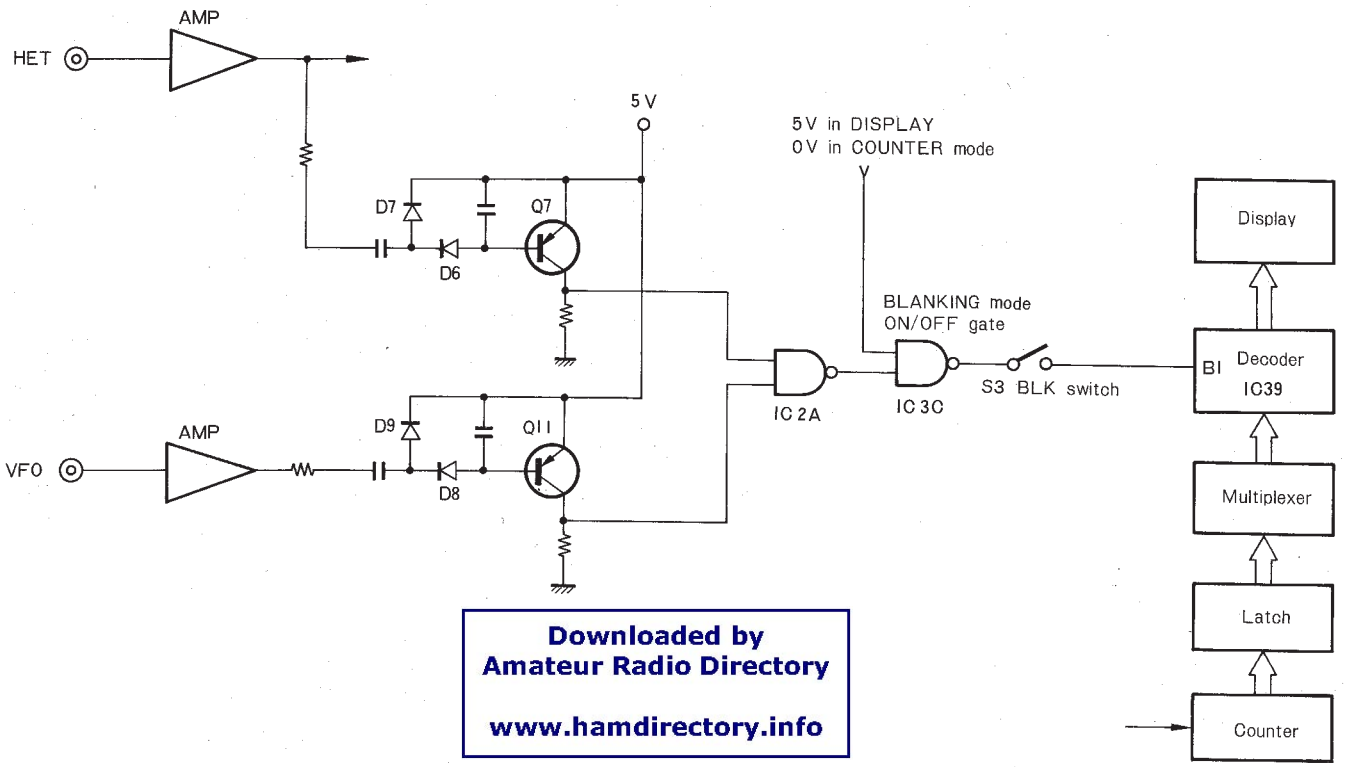


Fig. 10 Blanking Circuit

mode two IC3C inputs are at the H level and the output is at the L level, and thus the BI terminal of IC39 is maintained at the L level. The function table in Fig. 25 indicates that the decoder output is switched off and the display is blanked out.

During COUNTER operation both HET and VFO signals disappear as a matter of course. In this case IC3C is used to avoid blanking. Either input is put at the L level in interlock with the changeover switch on the panel surface. Since the display should not be blanked out during adjustment and repair, the switch S3 is installed for blanking OFF.

Carrier Switching Circuit

Like the blanking process for the HET and VFO inputs, the circuit in Fig. 11 detects the carrier with the diodes D10 and 11 and the transistor Q20. While the carrier signal is maintained at the input terminal, the source voltage is applied to the Q19 amplifier. If the carrier disappears, Q14 is turned off and the power supply is removed from Q19 to switch off the amplifier.

Q15 is a quartz crystal oscillator. When a 6.605MHz crystal unit is connected to the terminal and the carrier signal disappears, Q15 automatically begins to oscillate since the cut-off bias of Q14 applied to the Q15 emitter is lost. If an AM unit is connected with the DG-5, the carrier signal will disappear. Therefore, in place of this carrier signal, the oscillator output is fed to the input terminal of the VFO mixer. At that time the power is not supplied to Q19, and it is necessary to remove the connection to Q14 and to apply a separately obtained 8.5V to the Q19.

CIRCUIT DESCRIPTION

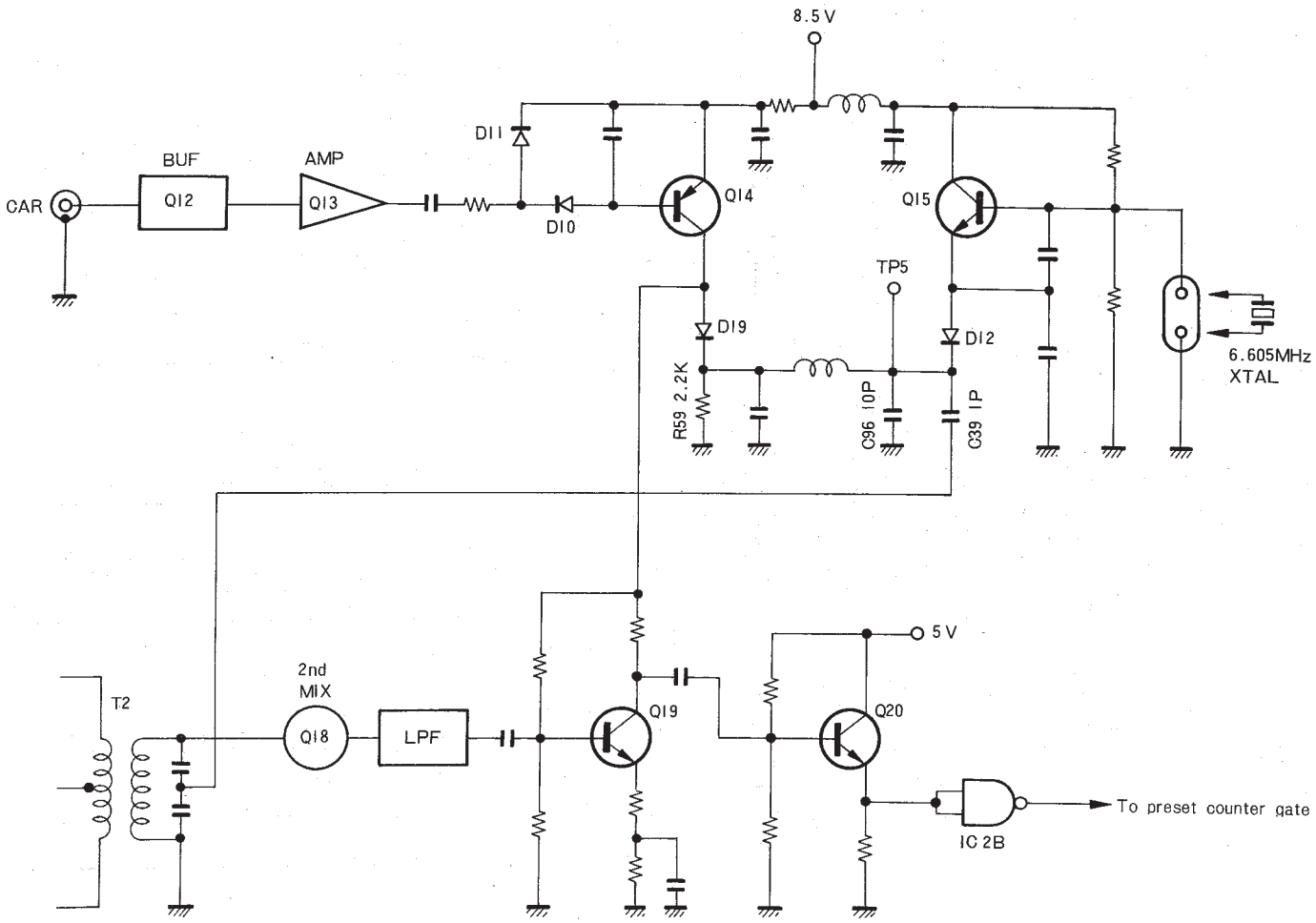


Fig. 11 Carrier Switching Circuit

5. Counter Circuit

Principle of Frequency Counter

The general principle of the frequency counter is explained by the block diagram shown in Fig. 12. The input signal to be measured is amplified, shaped, and converted into pulses. The gate circuit is open for a predetermined time period which is based on the reference time. The pulses passing through the gate while it is open are counted at the counter block and temporarily memorized in the latch circuit. At predetermined intervals the memorzed information is sent to the display. The sequential order for the above is as follows:

(1) With a reset signal the condition in the counter is made "0."
(2) With a gate signal the gate circuit is open, and the counter begins to count the pulses which pass the gate.
(3) When the gate signal disappears, the gate circuit is closed and the counter terminates its counting.
(4) With a latch signal the counted value memorized in the latch circuit is transferred to the display unit where the result is displayed.

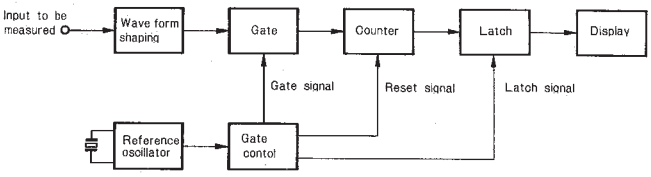


Fig. 12 Principle of Frequency Counter

(5) Return to state (1) and the same sequence is repeated.

The reset, gate, and latch signals control the respective blocks in proper sequence. As previously described for the principle of display frequency synthesis, the DG-5 is provided with an additional preset counter and the contents in the two counters are combined. Fig. 13 shows the time relationship for the control pulses. Compared with the case of Fig. 12, the load pulse (signal) is added and this is used for a preset command. The sequential order for the block diagram in Fig. 13 is as follows:

CIRCUIT DESCRIPTION

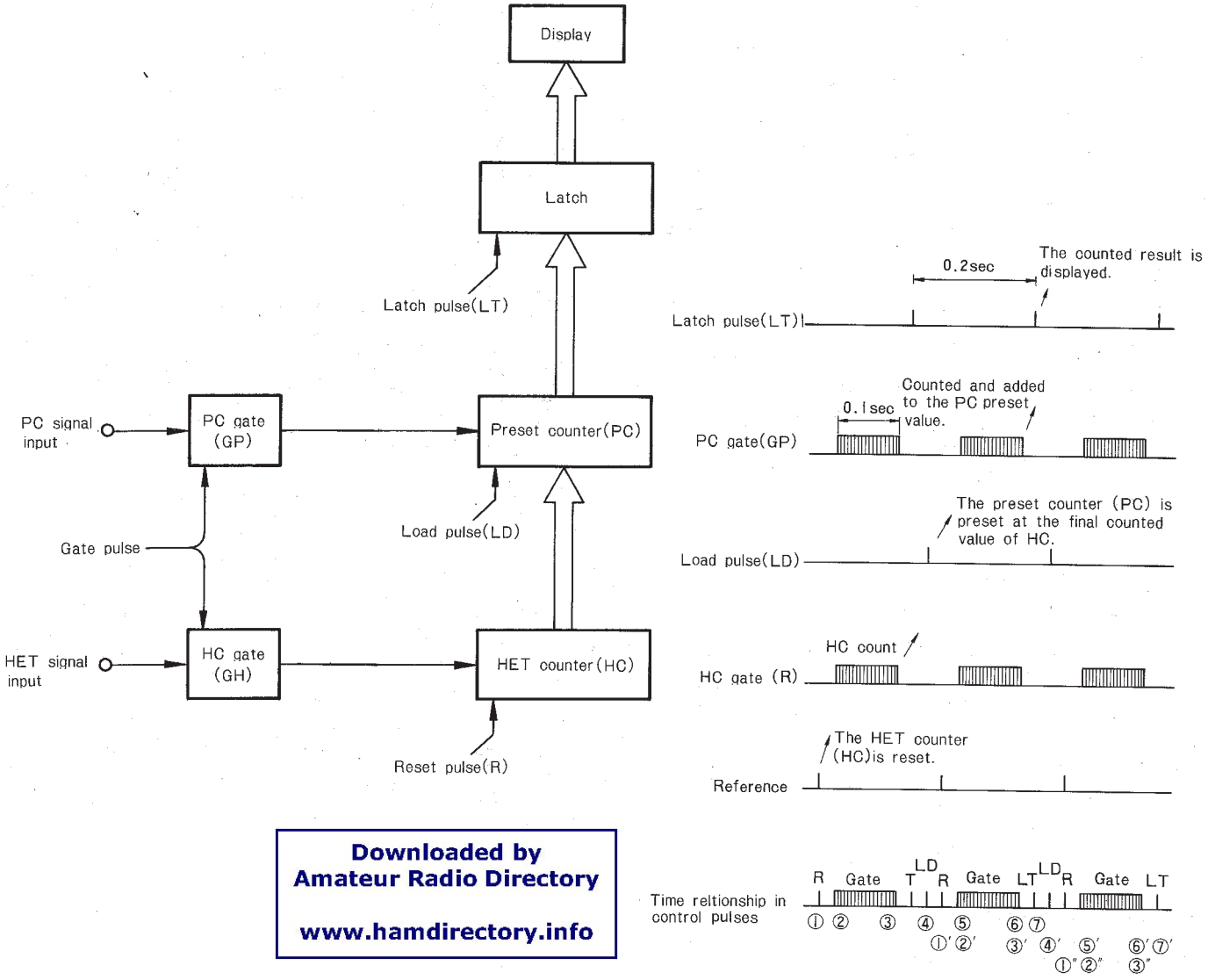


Fig. 13 Time Relations of Counter Control Pulse

(1) With a reset signal the condition in the HET counter is made "0."
(2) With a gate signal the HC gate circuit is open and the HET signal pulses pass through the gate. The HET counter begins to count the pulses which pass the gate.
(3) When the gate signal disappears, the HC gate circuit is closed and the HET counter terminates its counting.
(4) With a load signal the preset counter is preset at the final counting value at the HET counter.
(5) With a gate signal the PC gate is open and the PC signal pulses pass through the gate. The preset counter begins to count the passed pulses and to add the result to the preset value.
(6) When the gate signal disappears, the PC gate is closed and the preset counter terminates its counting.
(7) With the latch signal the preset counter value memorized in the latch circuit is delivered to the display unit where the result is displayed.
(8) Return to state (1) and the same sequence is repeated. In this case the HC gate and the PC gate operate simultaneously with the same gate signal. As shown in Fig. 13, the cycles (1) to (7) advance together, but there is always an overlap of half a cycle between the neighboring cycles.

CIRCUIT DESCRIPTION

Control Pulse Generator

For the orderly control of the DG-5 gate and counter in Fig. 13, the control pulse generator is employed. Fig. 14 shows this circuit together with the frequency divider circuit. Fig. 15 shows the timing chart for explaining the operating condition. In Fig. 15, the 10MHz signal from the reference oscillator is frequency-divided to units of 10Hz. This division is performed by the IC5 ~ 10 in 6 stages, each in charge of 1/10 division. When the obtained 10Hz signal is used to drive the flip-flop circuit of IC11, a 50% duty square wave of 5Hz is obtained. As shown in the timing chart of Fig. 15, the H level section corresponds to half a cycle of 5Hz, i.e. 0.1 second. Therefore this section is used as a gate signal. Similarly outputs of IC10 and IC11 are combined, and the NAND logic and the differential circuit are combined in the sequential order of Y1 to Y9 as shown in the timing chart. Thus the respective reset, load, and latch pulses are produced. There are two types of reset pulses, A and B, because the SN74196N of the HET counter is for the negative logical input while the SN74LS90N is for the positive logical input. Q24 is a transistor gate for the DH circuit. It is turned on when the DH is off.

Latch Circuit and DH Switch

Input pulses are continuously entering the counter circuit. If the counter output is directly transferred to the display, the displayed result will change erratically with each change in the counted result. Such a display cannot be read out in practical use. Therefore the counted results must be retained until the display requires them. The latch circuit is used for this purpose. It is a type of memory circuit which keeps the counted result and sends it to the display upon the reception of a latch signal. Each time the latch signal is delivered, the latch circuit gives to the display the counted value which was obtained while the gate was open before the reception of the latch signal. In the DG-5 the interval between the 2 neighboring latch signals is 0.2 second.

The DH circuit is such that the displayed result remains unchanged until another latch signal arrives. The transistor gate of Q24 is connected in series with the latch signal route and the entry of a latch pulse is interrupted when the DH circuit is on. As shown in Fig. 16, a reverse bias is applied to the Q24 base while the DH circuit is off and there is continuity between the emitter and the collector. When the DH circuit is on, the base loses its bias voltage and continuity is lost between the emitter and the collector. If the main power supply (of TS-520 in this case) is switched on and off while the DH switch is left switched on, a forward bias is applied to the base through the electrolytic capacitor C84 when the main switch is on. During the time constand which is dependent on C84, R100, and R101 (determined to be equivalent to several cycles in counter operation), Q24 is turned on and a correct frequency can be memorized. When the main switch is off, the capacitor C84 is quickly discharged through diode D16.

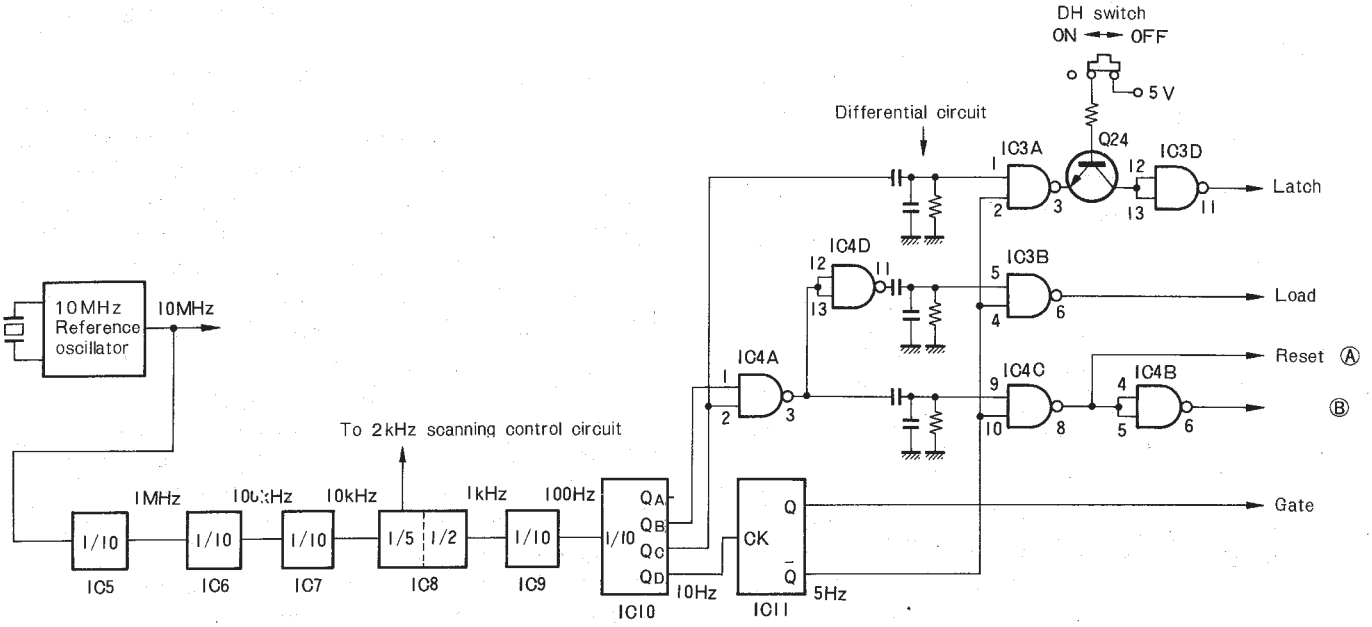


Fig. 14 Control Pulse Generator

CIRCUIT DESCRIPTION

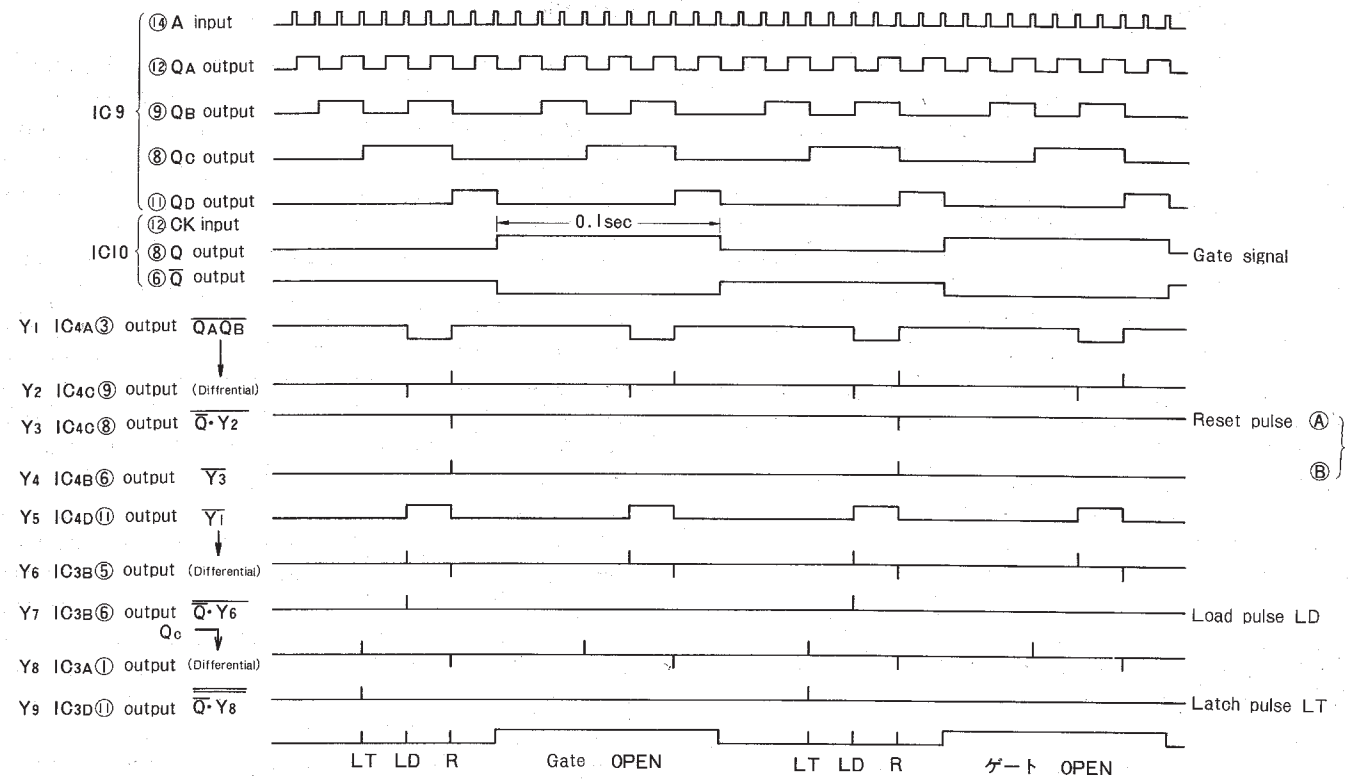


Fig. 15 Timing Chart of Control Pulse Generation

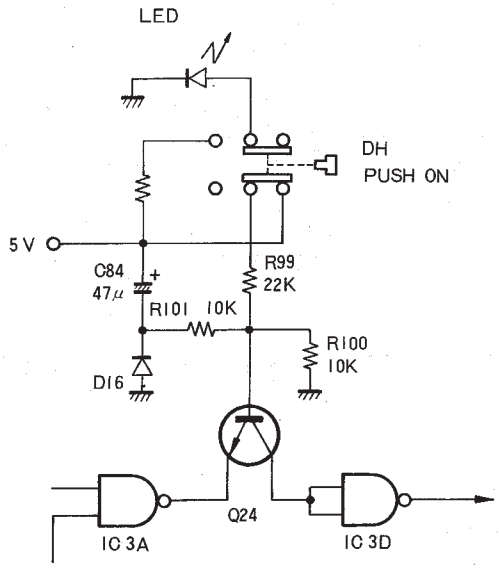


Fig. 16 DH Circuitry

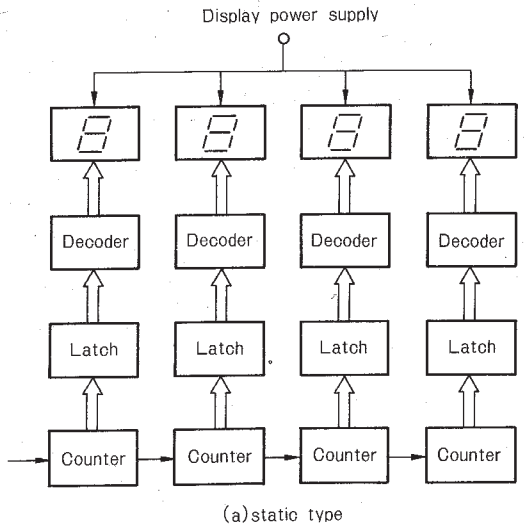
6. Dynamic Display and Multiplexer

The output from the latch circuit can be displayed for the respective digits when it is delivered to the display through the decoder. This is a static type display circuit, with a block diagram as shown in Fig. 17 (a). Theoretically this type of circuit is very reliable since counters, latches, decoders, and display circuits are independent of each other for each digital unit. However, as the number of digits to be displayed increases, very precious decoder IC's must be installed in a quantity to be displayed increases, very precious decoder IC's must be installed in a quantity which is equal to the number of digits. In addition, since the display section is generally independent of the main printed circuit board, the connections and wiring will be very complex. These are disadvantages of the static type display.

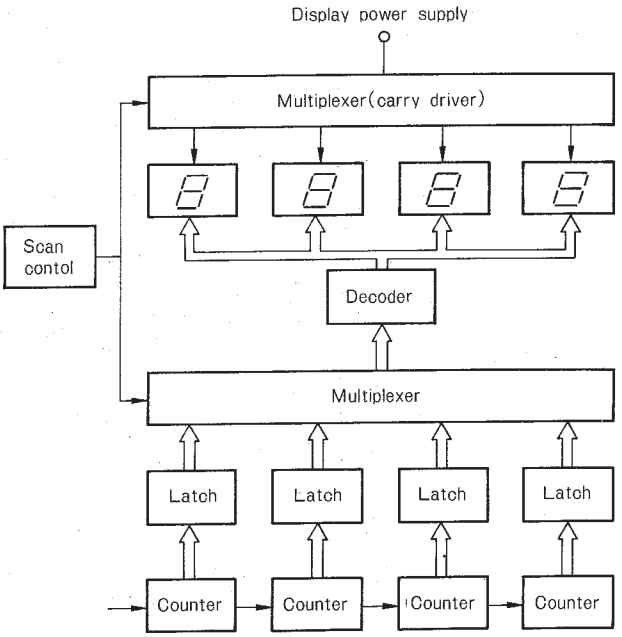
On the other hand there is another type of display, the dynamic dispaly circuit, which is adopted for the DG-5. In this case only one decoder is used. The latches and the display units for the respective digits are controlled through the multiplexer and the counted result is displayed by the time division system. In the circuit shown in Fig. 17 (B), outputs from the respective latches are gathered in the multiplexer. When a scanning control signal is applied to the multiplexer, components of the respective digits are processed by time division switching and sent to the decoder. The multiplexer on the display side is synchro-

CIRCUIT DESCRIPTION

nized with that on the latch side for similar switching for each digit. Each type has its own advantages. The disadvantages of this latter type of display are that the multiplexers and the scanning control are required, and that the entire circuit is complex and repair is difficult since the time division switching system is adopted. However, in the case of the DG-5 the number of wire connections to the display is 15 for the dynamic type and 45 for the static type. If in addition the wiring to switches and indicator lamps is taken into acount, the achievement of this same construction with the static type display seems very difficult to achieve.



(a)static type



(b)Dynamic Type

Fig. 17 Static Display and Dynamic Display

Multiplexer

The multiplexer is generally installed on the latch side. In the circuit diagram it is composed of the 7 IC's, IC32 to IC38. The latch output is expressed in the BCD (Binary Coded Decimal) mode and the output for one digit is expressed by the 4 BCD output components, A, B, C, and D. The multiplexer gathers components A (or B, ...) out of the whole 6 digits in one position and ejects these components A ~ D synchronized with the scanning control signal by time division switching system. Fig. 18 shows the logica diagram of the circuit blocks that are indicated by the boxes in the circuit diagram. The SN7454N of IC32, 34, 35, and 37 is a 4-input distributor, while the TD3451AP of IC33 and 36 is used as a 2-input 2-circuit distributor. For ease of understanding, Fig. 19 is a logic diagram of SN7454N. As shown in Fig. 19 (a), this IC contains 4 2-input AND circuits and an NOR circuit. When 8 outputs A~ H enter, the resultant output Y is as follows:

$$Y = AB + CD + EF + GH \quad \cdots\cdots\cdots\cdots \quad (3)$$

If these inputs are separated into 2 groups (A, B, C, D signal inputs in one group and T1 ~ 4 control signals in the other group), the resultant output Y1 is as follows:

$$Y1 = AT1 + BT2 + CT3 + DT4 \quad \cdots\cdots \quad (4)$$

When it is assumed that the signals T1 ~ 4 are the control signals scanned in turn as shown in Fig. 19 (c), the output Y1 will come out in the information train of component A for T1, component B for T2, ... , as is obvious from expression (4). The same operation is performed for the 6 digits by the circuit shown in Fig. 19. Since IC does not have any distributor for 6 inputs, outputs from 4-input and 2-input circuits are again combined at IC38 to obtain a function which is equivalent to one obtainable from a 6-input distributor. The control signal in this circuit is switched over in the order of A1, A2, A3, ... at the velocity of 2kHz. Therefore, as shown in Fig. 18 (b), each BCD digit is switched over to another by the rotary switch at the speed of 333Hz. The multiplexer (distributor) on the display side also operates in the same manner. In this case, however, the power supply to the display is merely switched on and off, and a control signal is delivered to the base of the transistor connected in series with the power supply of each display unit, in good timing with the latch side as shown in Fig. 20. Therefore the multiplexer on the display side is used merely to distribute current to the display units.

CIRCUIT DESCRIPTION

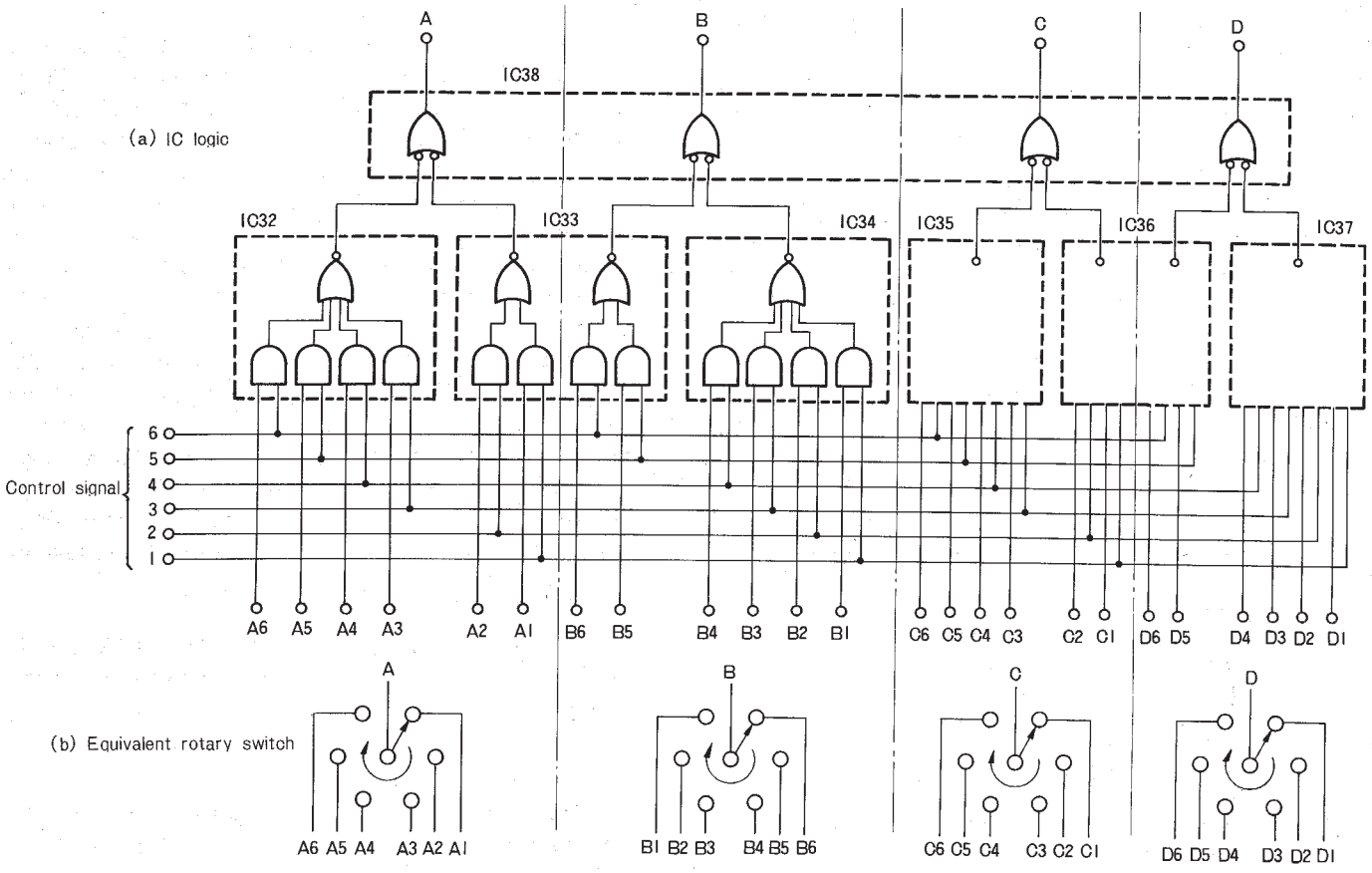


Fig. 18 Multiplexer Circuit

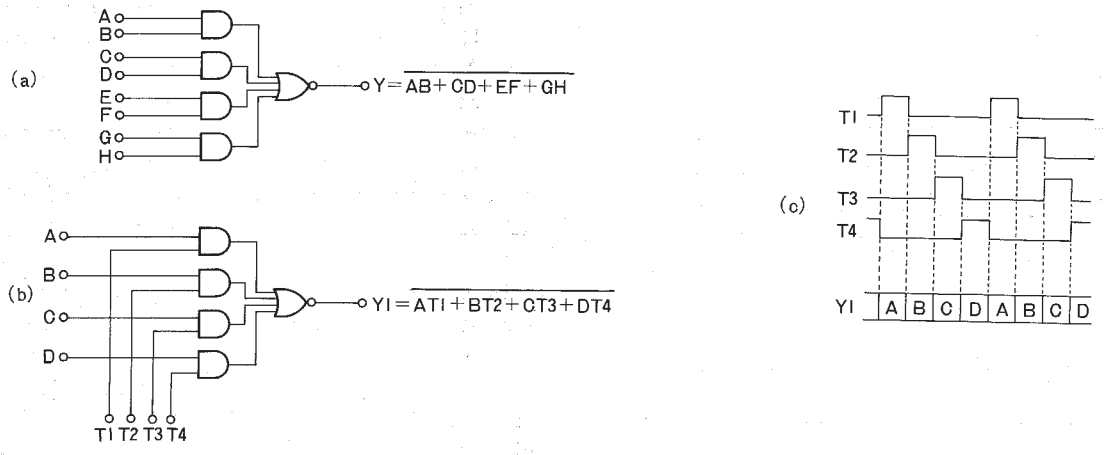


Fig. 19 4 Bits Multiplexer

CIRCUIT DESCRIPTION

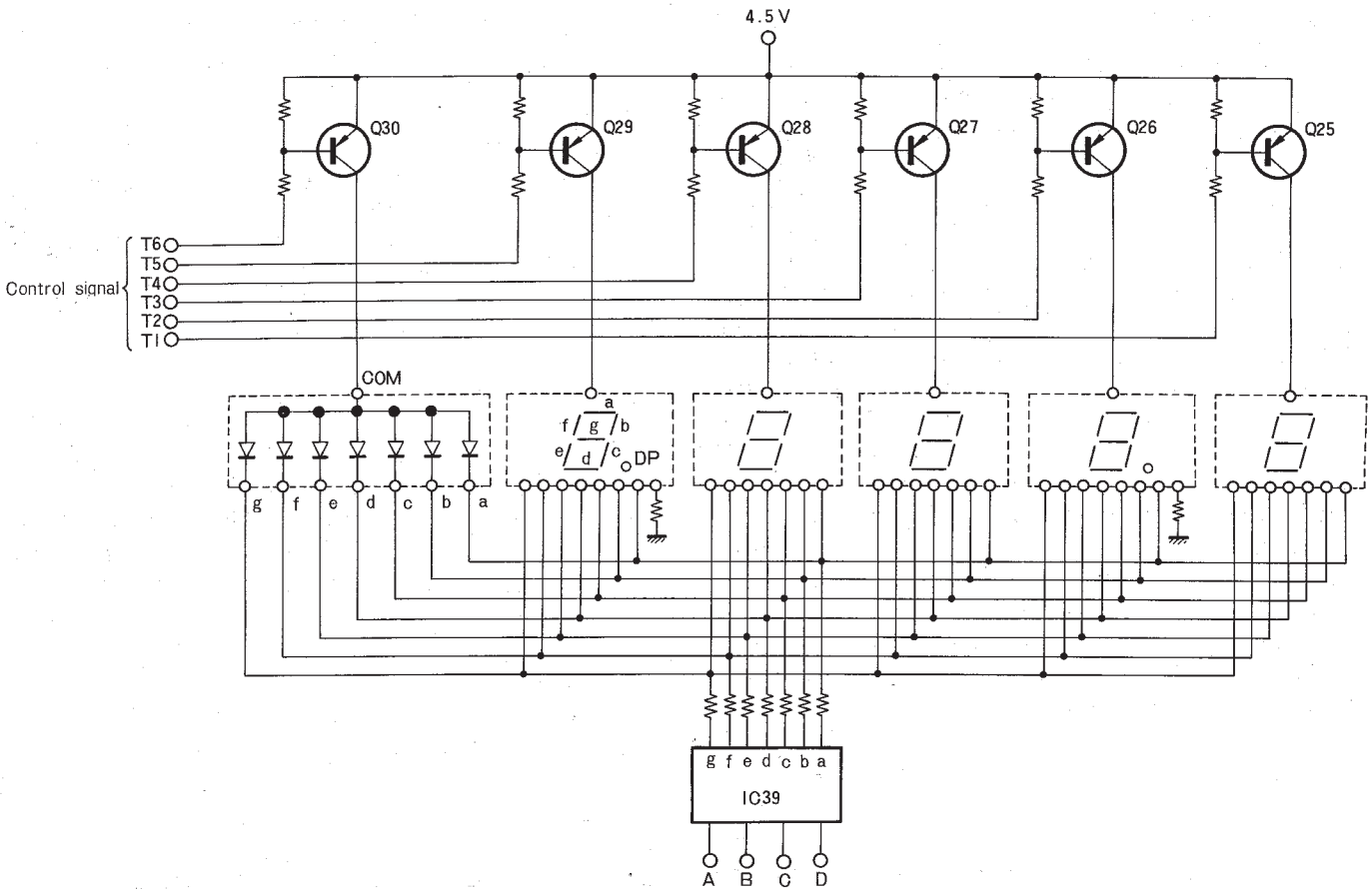


Fig. 20 Display Driver

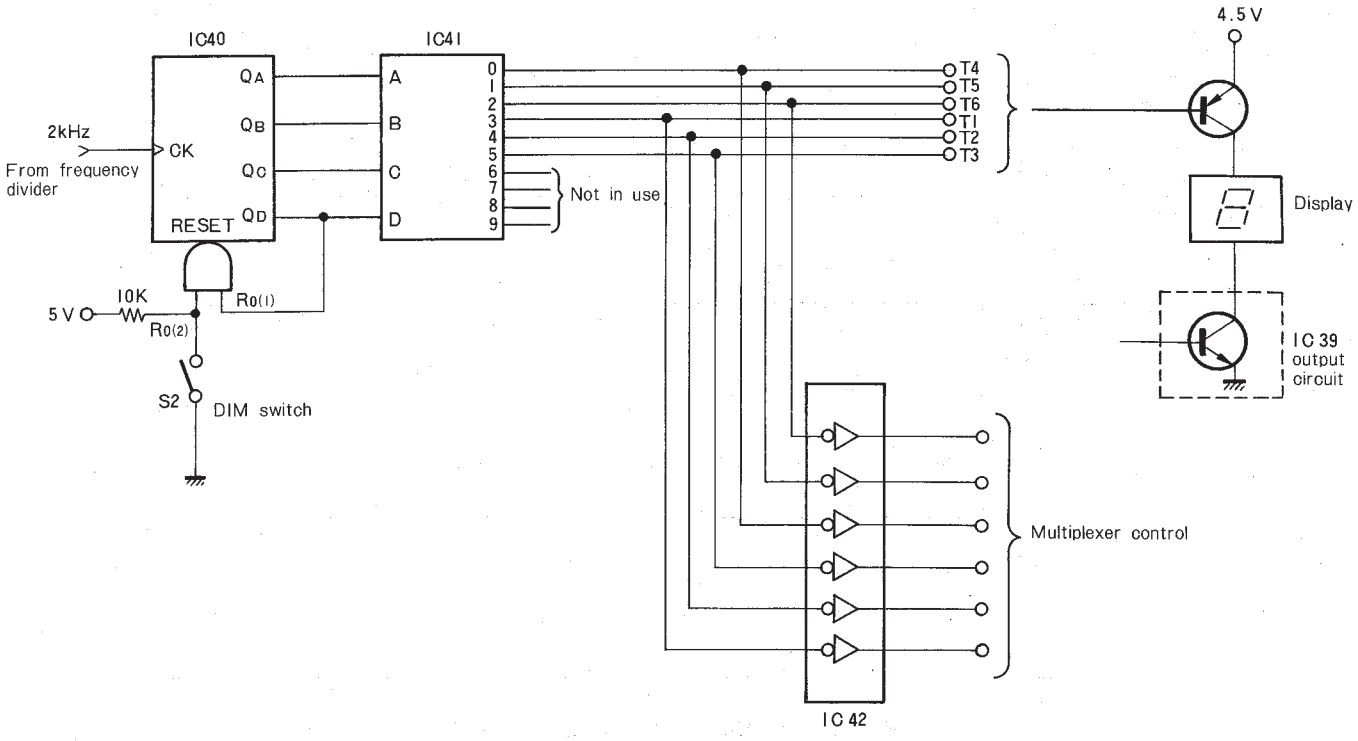


Fig. 21 Scanning Control Circuit

CIRCUIT DESCRIPTION

Scanning Control Circuit

The signals for controlling the multiplexer are generated in the circuit shown in Fig. 21. IC40 receives a 2kHz clock pulse which is obtained from the frequency distributor of the standard oscillator. The DIM siwtch is used to select either base 6 or base 12 counting. The output from IC40 is fed to the BCD decoder of IC41 which generates a negative logic changeover control signal. The operation of this circuit can be grasped from the timing chart in Fig. 22 and the function tables of TD3492BP (IC40) and TD3442AP (IC41) in Figs. 23 and 24. IC40 ordinarily operates as a base 12 counter, and it automatically operates as a base 12 counter when the DIM switch is on (or when either of the reset terminals is at the L level). If the DIM switch is off, one of the 2 reset terminals is at the H level and the other is connected to the QD output line. When counting advances from 0 to 1, ..., and finally to 6, the QD output is immediately at the H level and the C41 is simultaneously reset since the QD line is connected with the reset terminal. When the IC41 is reset, counting is returned to "0" again. That is, this circuit operates as a base 6 counter when the DIM switch is off.

IC41 receives BCD inputs and ejects negative logic outputs at its output terminals, 0 ~9. In the DG-5 the 6 outputs from 0 to 5 are used as control signals for the respective digital units. The display driving transistor operates with negative logic pulses and the latch-side multiplexer operates with positive logic pulses. Therefore the respective output circuits are connected with the IC42 inverter to convert the negative logic outputs into positive ones. Thereafter the multiplexer is controlled.

Dimmer Switch

Current flows in the display while the control signals are present. In the ordinary operating state, the 6-digit base 6 control is exercised. In other words the display unit for each digit is fed 1/6 duty pulse current. If the DIM switch is on in this state, the control is base 12 as described previously. Thus the current flowing in the display is of 1/12 duty and brightness is also reduced to half. This can be understood from the timing chart in Fig. 22.

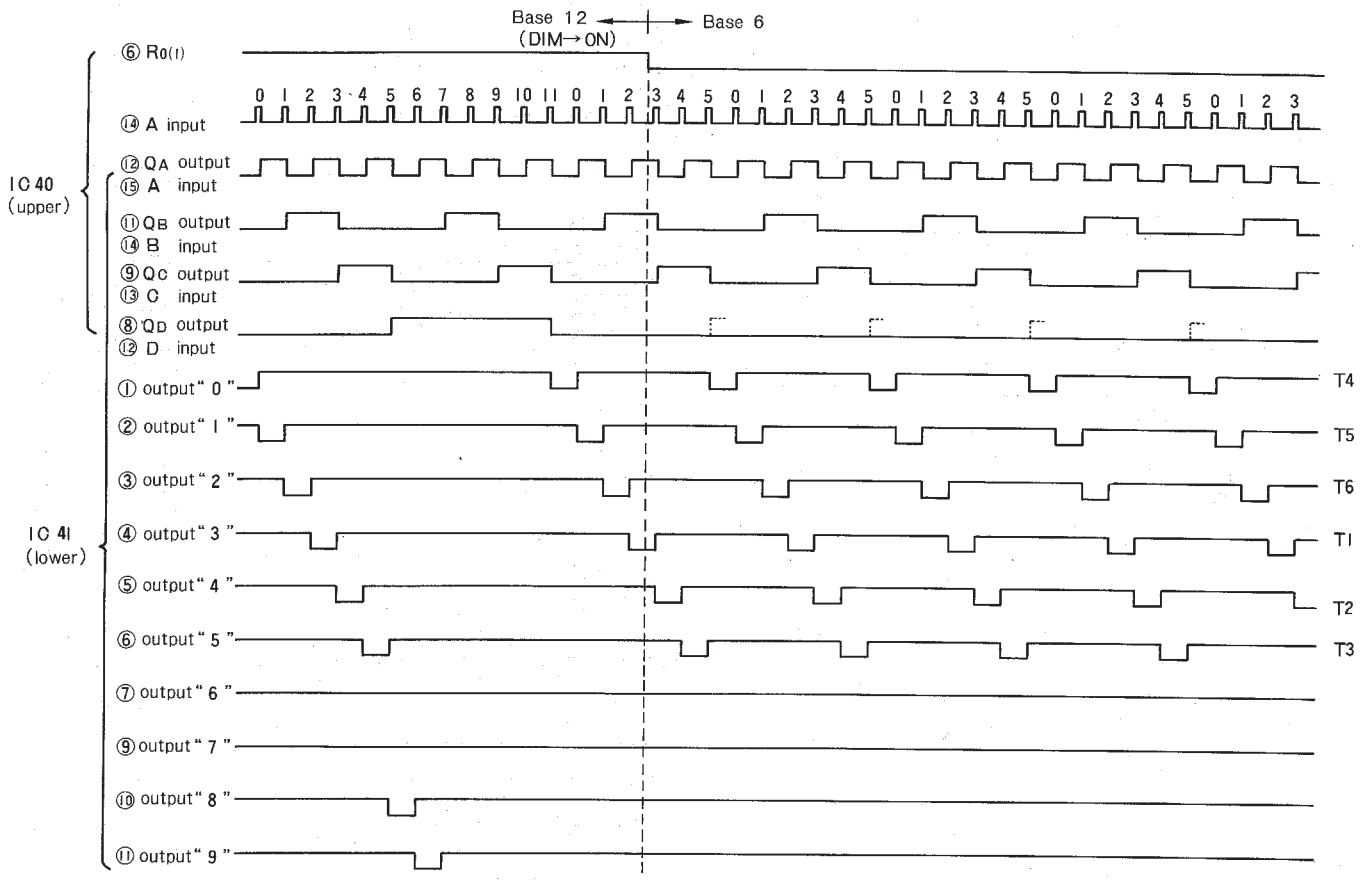


Fig. 22 Scanning Control Circuit & Timing Chart

CIRCUIT DESCRIPTION

TD3492BP(IC40)
COUNT SEQUENCE

COUNT	OUTPUT			
	D	C	B	A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	H	L	L	L
7	H	L	L	H
8	H	L	H	L
9	H	L	H	H
10	H	H	L	L
11	H	H	L	H

RESET-COUNT

INPUTS		OUTPUTS			
R0(1)	R0(2)	D	C	B	A
H	H	L	L	L	L
L	H	COUNT			
H	L				
L	L				

Fig. 23

TD3442AP(IC41)
FUNCTION TABLE

INPUTS				OUTPUTS									
D	C	B	A	0	1	2	3	4	5	6	7	8	9
L	L	L	L	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	H	H	L	H	H	H	H	H	H	H
L	L	H	H	H	H	H	L	H	H	H	H	H	H
L	H	L	L	H	H	H	H	L	H	H	H	H	H
L	H	L	H	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
L	H	H	H	H	H	H	H	H	H	H	L	H	H
H	L	L	L	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
H	L	H	L	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
H	H	L	L	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	H	L	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

Fig. 24

SN74247N(IC39)
FUNCTION TABLE

DECIMAL OR FUNCTION	INPUTS						BI	OUTPUTS							Display
	LT	RBI	D	C	B	A		a	b	c	d	e	f	g	
0	H	H	L	L	L	L	H	ON	ON	ON	ON	ON	ON	OFF	0
1	H	X	L	L	L	H	H	OFF	ON	ON	OFF	OFF	OFF	OFF	1
2	H	X	L	L	H	L	H	ON	ON	OFF	ON	ON	OFF	ON	2
3	H	X	L	L	H	H	H	ON	ON	ON	ON	OFF	OFF	ON	3
4	H	X	L	H	L	L	H	OFF	ON	ON	OFF	OFF	ON	ON	4
5	H	X	L	H	L	H	H	ON	OFF	ON	ON	OFF	ON	ON	5
6	H	X	L	H	H	L	H	ON	OFF	ON	ON	ON	ON	ON	6
7	H	X	L	H	H	H	H	ON	ON	ON	OFF	OFF	OFF	OFF	7
8	H	X	H	L	L	L	H	ON	ON	ON	ON	ON	ON	ON	8
9	H	X	H	L	L	H	H	ON	ON	ON	ON	OFF	ON	ON	9
10	H	X	H	L	H	L	H	OFF	OFF	OFF	ON	ON	OFF	ON	c
11	H	X	H	L	H	H	H	OFF	OFF	ON	ON	OFF	OFF	ON	ɔ
12	H	X	H	H	L	L	H	OFF	ON	OFF	OFF	OFF	ON	ON	u
13	H	X	H	H	L	H	H	ON	OFF	OFF	ON	OFF	ON	ON	c
14	H	X	H	H	H	L	H	OFF	OFF	OFF	ON	ON	ON	ON	t
15	H	X	H	H	H	H	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	
BI	X	X	X	X	X	X	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	
RBI	H	L	L	L	L	L	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	
LT	L	X	X	X	X	X	H	ON	ON	ON	ON	ON	ON	ON	8

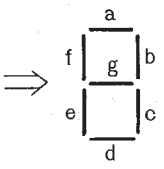


Fig. 25

CIRCUIT DESCRIPTION

7. Decoder and Display

Decoder

Signals flow within the counter in the BCD mode. Therefore they cannot be displayed immediately after passing through the latch and multiplexer circuits. The decoder is used to convert the BCD signals into the numerals 0 ~ 9 readable for us. Since the DG-5 display employs 7-segment LED's, the 7-segment decoder is used. The 7 segments mean that the digit 8 can be divided into 7 segments, and that the other digits 0 ~ 7 and 9 can be displayed by selecting those segments that should be lit. Based on the function table of SN74247N in Fig. 25, the open collector transistor is turned on when an input BCD signal enters. Thus the display receives currents to light up the required segments.

The RBI terminal of the decoder receives a control signal for the 10MHz unit. When this terminal is at the L level and the input BCD is "0," the display can be blanked out. Therefore if it is unnecessary to use this unit, as in the case of 7MHz, unwanted "0" is blanked out.

Display

The display employs 3 light emitting diodes (LED), each embracing 2 digital units. The size of each digit is 10.16mm x 6.60mm. The LED color is red since that color offers efficient luminance and its brightness, color uniformity, and distribution are all otpimum. In order to obtain color tones comfortable for the yes, the natural dark red of the LED's is softened with violet and light smoke filters.

As shown in Fig. 2., the display is connected to the decoder and the same segments of the respective LED's are connected in parallel with each other. The common anode of each LED is connected to the independent 4.5V power supply through the trnasistor switch driver which is provided to each digital unit.

8. Power Circuit

All power for the DG-5 is supplied from the master unit,TS-520S. However, the power cannot be used directly since it contains much ripple voltage. In terms of its power systems, the DG-5 can be roughly divided into the analog circuit system, the TTL. IC system, and the LED display system. As shown in Fig. 26, each system is provided with a stabilized power circuit. The analog system has an 8.5V non-adjustable power circuit stabilized by the zener diode and the transistor. The TTL. IC system employs an exclusively installed 3-terminal regulator since it requires a large current and its voltage regulation must be below 5% though its voltage of 5V is very low. The LED display power can be used in common with the 5V source. However there will be much current difference in such usage when all segments are lit up, and in addition the capacity of 5VIC regulator will almost lose its tolerance. Thus the LED display is also provided with an exclusive power supply. In this case the 5V AVR output is used as the standard stabilized voltage. If the 5V output is switched off, the 4.5V output simultaneously disappears and the LED's go out.

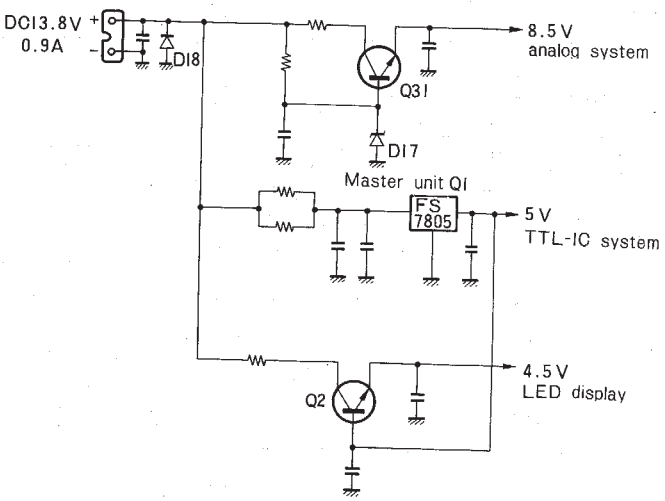
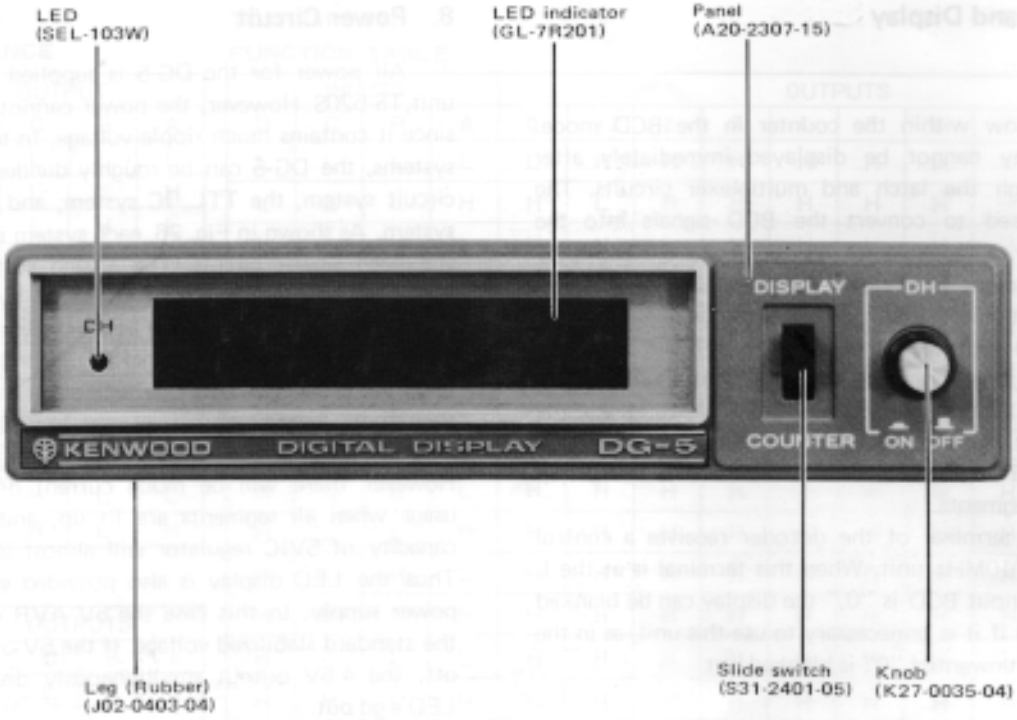
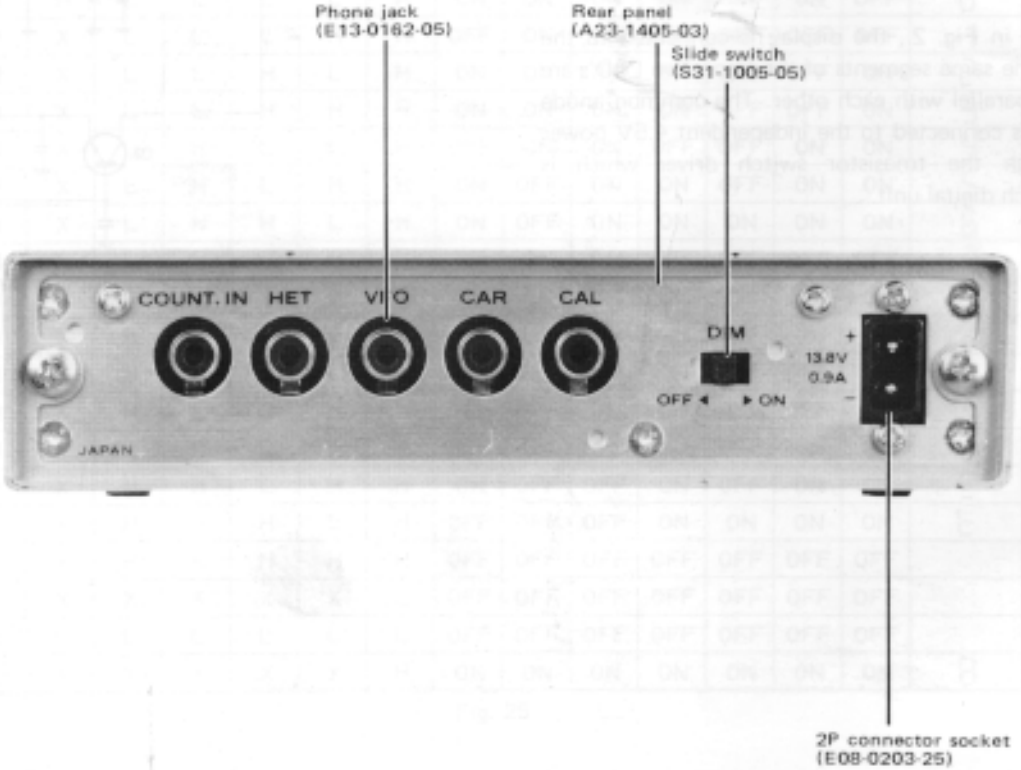


Fig. 26 Power Supply Circuit

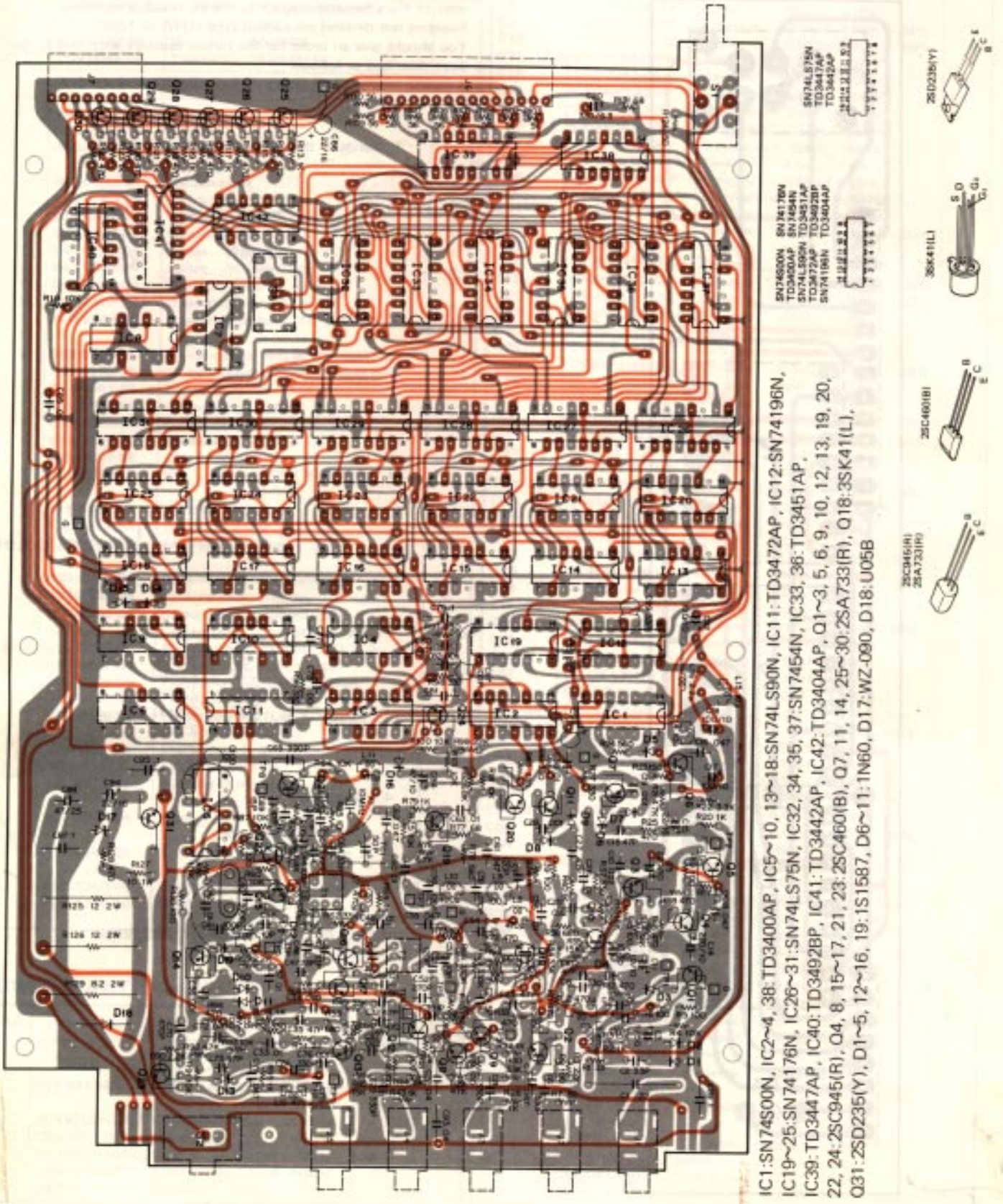
EXTERNAL VIEW





PC BOARD

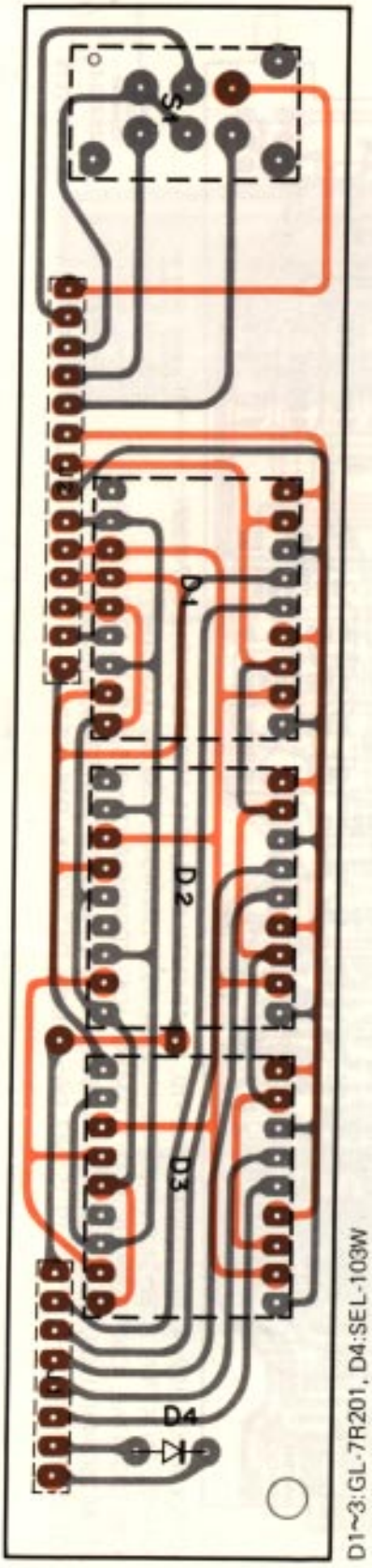
▼ Counter Unit (X54-1260-00)



IC1:SN74S00N, IC2~4, 38:TD3400AP, IC5~10, 13~18:SN74LS90N, IC11:TD3472AP, IC12:SN74196N, IC19~25:SN74176N, IC26~31:SN74LS75N, IC32, 34, 35, 37:SN7454N, IC33, 36:TD3451AP, IC39:TD3447AP, IC40:TD3492BP, IC41:TD3442AP, IC42:TD3404AP, Q1~3, 5, 6, 9, 10, 12, 13, 19, 20, 22, 24:2SC945(R), Q4, 8, 15~17, 21, 23:2SC460(B), Q7, 11, 14, 25~30:2SA733(R), Q18:3SK41(L), Q31:2SD235(Y), D1~5, 12~16, 19:1S1587, D6~11:1N60, D17:WZ-090, D18:U05B

PC BOARD/PARTS LIST

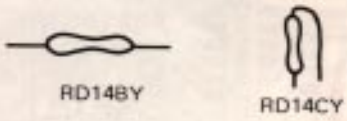
▼ Display Unit (X54-1270-00)



D1~3:GL-7R201, D4:SEL-103W

Note 1:
Resistors except the special type (example: cement, metal film, etc.) are not detailed in PARTS LIST. With regard to the value, refer to the schematic diagram or the PC board illustration.
Resistors not detailed are carbon type (1/4W or 1/8W).
You should give an order for the carbon resistors according to the ways described as follows:
A carbon resistor's part number is example RD14BY 2E 222J

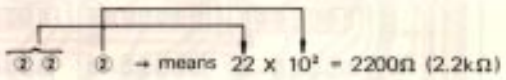
1. Kinds of the carbon resistor



2. Wattage

1/4W → 2E
1/8W → 2B

3. Resistance value



Significant figure Multiplier

Example:

221 → 220Ω
222 → 2.2kΩ
223 → 22kΩ
224 → 220kΩ
225 → 2.2MΩ

4. Tolerance

J = ±5% (Gold color)
K = ±10% (Silver color)

Note 2:
K: U.S.A. W: Europe T: Britain

PARTS LIST

TOTAL

Symbol ☆: New parts

Ref. No.	Parts No.	Description	Remarks
		CAPACITOR/SEMICONDUCTOR	
C1	CK45F1H103Z	Ceramic 0.01μF +80%, −20%	
Q1	V30-0158-05	IC FS-7805	
Q2	V04-0046-05	Transistor 2SD235(Y)	
		MISCELLANEOUS	
—	A01-0709-22	Case	☆
—	A20-2307-15	Panel	☆
—	A23-1405-03	Rear panel	☆
—	B03-0503-24	Switch mask	☆
—	B10-0604-04	Front glass	☆
—	B11-0402-04	Filter	☆
—	B40-2414-04	Name plate	☆
—	B43-0607-04	Badge (TRIO)	☆
—	B43-0608-04	Badge (KENWOOD)	☆
—	B46-0058-00	Warranty card (K only)	
—	B50-2536-00	Operating manual (K, W)	☆
—	B50-2537-00	Operating manual (T)	☆
—			
—	E08-0203-25	2P connector socket (Receptacle)	
—	E09-0203-25	2P connector socket (Plug) X 2	
—	E14-0061-05	Phono plug (Red) X 2	☆
—	E14-0062-05	Phono plug (White) X 2	☆
—	E14-0063-05	Phono plug (Black) X 2	☆
—	E14-0115-05	Phono plug (Gray) X 3	
—	E91-0017-05	Clip (Red)	
—	E91-0018-05	Clip (Black)	
—	F15-0605-04	Blinding plate	☆
—	F20-0078-05	Insulating plate	
—	F29-0014-05	Insulating washer	
—	H01-2530-04	Packing case (Inside) (T)	☆
—	H01-2531-04	Packing case (Inside) (K, W)	☆
—	H03-1630-04	Carton case (Outside) (T)	
—	H03-1631-04	Carton case (Outside) (K, W)	
—	H12-0460-04	Styrene foam cushion (A) X 2	☆
—	H12-0407-04	Styrene foam cusion (B)	☆
—	H25-0103-04	Protection bag (Attachment)	
—	H25-0106-04	Protection bag	
—	H25-0029-04	Protection bag (Leg X 2, screw X 2)	
—	J02-0069-05	Leg (Small X 2)	
—	J02-0403-04	Leg (Rubber X 4)	☆
—	J42-0401-04	Bushing (Knob)	
—	K27-0035-04	Knob	
—	N09-0601-05	Screw X 2	
—	X54-1260-00	Counter unit	☆
—	X54-1270-00	Display unit	☆

COUNTER UNIT (X54-1260-00)

Ref. No.	Parts No.	Description	Remarks
		CAPACITOR	
C1	C91-0411-05	Metallized polyester 0.22μF 0.22μF 250WV	☆
C2	CC45SL2H330J	Ceramic 33pF ±5%	
C3	CE04W1H010	Electrolytic 1μF 50WV	
C4	CK45F1H103Z	Ceramic 0.01μF +80%, −20%	
C5	CE04W1A221	Electrolytic 220μF 10WV	
C6	CK45B1H331K	Ceramic 330pF ±10%	
C7	C-90-0262-05	Ceramic 0.047μF 25WV	
C8	CK45B1H331K	Ceramic 330pF ±10%	
C9	CK45F1H103Z	Ceramic 0.01μF +80%, −20%	
C10	CK45F1H223Z	Ceramic 0.022μF+80%, −20%	
C11, 12	CS15E1A100M	Tantalum 10μF 10WV	
C13	C90-0262-05	Ceramic 0.047μF25WV	
C14	CE04W1A221	Electrolytic 220μF 10WV	
C15	CE04W1C220	Electrolytic 22μF 16WV	
C16	C90-0262-05	Ceramic 0.047μF 25WV	
C17	CE04W1A101	Electrolytic 100μF 10WV	
C18	CC45SL1H470J	Ceramic 47pF ±5%	
C19	CK45B1H102K	Ceramic 1000pF ±10%	
C20	CE04W0J331	Electrolytic 330μF 6.3WV	
C21	CK45B1H331K	Ceramic 330pF ±10%	
C22	CK45F1H473Z	Ceramic 0.047μF +80%, −20%	
C23	CC45SL1H470J	Ceramic 47pF ±5%	
C24	CC45CH1H050D	Ceramic 5pF ±0.5pF	
C25	CK45F1H223Z	Ceramic 0.022μF +80%, −20%	
C26	CK45F1H103Z	Ceramic 0.01μF +80%, −20%	
C27	CC45SL1H470J	Ceramic 47pF ±5%	
C28	CK45B1H102K	Ceramic 1000pF ±10%	
C29	CK45B1H331K	Ceramic 330pF ±10%	
C30	CK45F1H223Z	Ceramic 0.022μF +80%, −20%	
C31	CC45CH1H050D	Ceramic 5pF ±0.5pF	
C32	CC45SL1H470J	Ceramic 47pF ±5%	
C33	CK45F1H103Z	Ceramic 0.01μF +80%, −20%	
C34	CK45F1H223Z	Ceramic 0.022μF +80%, −20%	
C35	CC45SL1H470J	Ceramic 47pF ±5%	
C36	CK45B1H102K	Ceramic 1000pF ±10%	
C37, 38	CK45F1H103Z	Ceramic 0.01μF +80%, −20%	
C39	CC45CH1H010C	Ceramic 1pF ±0.25pF	
C40	CC45SL1H391J	Ceramic 390pF ±5%	
C41	CC45SL1H101J	Ceramic 100pF ±5%	
C42	CK45F1H103Z	Ceramic 0.01μF +80%, −20%	
C43	CC45SL1H680J	Ceramic 68pF ±5%	
C44	CC45SL1H101J	Ceramic 100pF ±5%	
C45~47	CC45CH1H330J	Ceramic 33pF ±5%	
C48, 49	CK45F1H103Z	Ceramic 0.01μF +80%, −20%	
C50	C90-0262-05	Ceramic 0.047μF 25WV	
C51	CC45SL1H121J	Ceramic 120pF ±5%	
C52	CC45SL1H271J	Ceramic 270pF ±5%	
C53	CC45CH1H100D	Ceramic 10pF ±0.5pF	
C54, 55	C90-0262-05	Ceramic 0.047μF 25WV	
C56	CK45F1H130Z	Ceramic 0.01μF +80%, −20%	
C57	CC45SL1H121J	Ceramic 120pF ±5%	
C58	CC45SL1H271J	Ceramic 270pF ±5%	
C59	CC45SL1H121J	Ceramic 120pF ±5%	
C60	CK45F1H103Z	Ceramic 0.01μF +80%, −20%	
C61, 62	C90-0262-05	Ceramic 0.047μF 25WV	
C63	CK45F1H103Z	Ceramic 0.01μF +80%, −20%	
C64	CC45CH1H560J	Ceramic 56pF ±5%	
C65	CC45SL1H391J	Ceramic 390pF ±5%	
C56	CC45CH1H470J	Ceramic 47pF ±5%	
C67	CK45F1H103Z	Ceramic 0.01μF +80%, −20%	
C68	CC45CH1H010C	Ceramic 1pF ±0.25pF	
C69	CC45CH1H150J	Ceramic 15pF ±5%	
C70	CK45B1H471K	Ceramic 470pF ±10%	
C71, 72	C90-0262-05	Ceramic 0.047μF 25WV	
C73	CC45SL1H470J	Ceramic 47pF ±5%	
C74	CK45B1H331K	Ceramic 330pF ±10%	
C75	CC45CH1H010C	Ceramic 1pF ±0.25pF	
C76	CK45B1H102K	Ceramic 1000pF ±10%	
C77	CQ92M1H104K	Mylar 0.1μF ±10%	
C78	CK45B1H102K	Ceramic 1000pF ±10%	
C79	CQ92M1H104K	Mylar 0.1μF ±10%	
C80	CK45B1H102K	Ceramic 1000pF ±10%	
C81	CQ92M1H104K	Mylar 0.1μF ±10%	
C82	CK45B1H102K	Ceramic 1000pF ±10%	
C83	CC45CH1H220J	Ceramic 22pF ±5%	
C84	CE04W1A470	Electrolytic 47μF 10WV	
C85	CK45F1H103Z	Ceramic 0.01μF +80%, −20%	

PARTS LIST

Ref. No.	Parts No.	Description	Remarks
C86	CE04W1C220	Electrolytic 22μF 16WV	
C87	CQ92M1H104K	Mylar 0.1μF ±10%	
C88	CE04W1E470	Electrolytic 47μF 25WV	
C89	CQ92M1H104K	Mylar 0.1μF ±10%	
C90			
C91, 92	CE04W1A101	Electrolytic 100μF 10WV	
C93	CK45F1H473Z	Ceramic 0.047μF+80%, −20%	
C94	CE04W1C220	Electrolytic 22μF 16WV	
C95	CQ92M1H104K	Mylar 0.1μF ±10%	
C96	CC45CH1H100D	Ceramic 10pF ±0.5pF	
C97	CC45SL1H101J	Ceramic 100pF ±5%	
C98	CK45F1H103Z	Ceramic 0.01μF +80%, −20%	
C99	CC45SL1H330J	Ceramic 33pF ±5%	
C10	CK45F1H103Z	Ceramic 0.01μF +80%, −20%	
C101			
C102	CC45SL1H470J	Ceramic 47pF ±5%	
RESISTOR			
R1~131	RD14CY2B○○○J	Carbon ○○○Ω ±5% 1/8W Refer to schematic diagram, on the value.	
R26, 41, R56~58,80			
R125, 126	RS14AB3D120J	Metallized film resistor 12Ω +5% 2W	
R127	RS14AB3A100J	Metallized film resistor 10Ω ±5% 2W	
R129	RS14AB3D8R2J	Metallized film resistor 8.2Ω ±5% 2W	
SEMICONDUCTOR			
IC1	V30-0181-05	IC SN74S00N	
IC2~4	V30-0132-05	IC TD3400AP	
IC5~10	V30-1005-26	IC SN74LS90N	☆
IC11	V30-0131-05	IC TD3472AP	
IC12	V30-1009-16	IC SN74196N	☆
IC13~18	V30-1005-26	IC SN74LS90N	☆
IC19~25	V30-0168-05	IC SN74176N	
IC26~31	V30-1005-16	IC SN74LS75N	☆
IC32	V30-1004-16	IC SN7454N	☆
IC33	V30-1006-16	IC TD3451AP	☆
IC34, 35	V30-1004-16	IC SN7454N	☆
IC36	V30-1006-16	IC TD3451AP	☆
IC37	V30-1004-16	IC SN7454N	☆
IC38	V30-0132-05	IC TD3400AP	
IC39	V30-1010-16	IC SN74247N	☆
IC40	V30-1007-16	IC TD3492BP	☆
IC41	V30-0164-05	IC TD3442AP	
IC42	V30-0163-05	IC TD3404AP	
Q1, 2	V03-0270-05	Transistor 2SC945(R)	
Q3	V03-0079-05	Transistor 2SC460(B)	
Q4	V03-0136-05	Transistor 2SC785(R)	
Q5	V03-0079-05	Transistor 2SC460(B)	
Q6	V03-0270-05	Transistor 2SC945(R)	
Q7	V01-0084-05	Transistor 2SA733(R)	
Q8	V03-0079-05	Transistor 2SC460(B)	
Q9, 10	V03-0270-05	Transistor 2SC945(R)	
Q11	V01-0084-05	Transistor 2SA733(R)	
Q12, 13	V03-0270-05	Transistor 2SC945(R)	
Q14	V01-0084-05	Transistor 2SA733(R)	
Q15~17	V03-0079-05	Transistor 2SC460(B)	
Q18	V09-0057-05	FET 3SK41(L)	
Q19, 20	V03-0270-05	Transistor 2SC945(R)	
Q21	V03-0079-05	Transistor 2SC460(B)	
Q22	V03-0270-05	Transistor 2SC945(R)	
Q23	V03-0079-05	Transistor 2SC460(B)	
Q24	V03-0270-05	Transistor 2SC945(R)	
Q25~30	V01-0032-05	Transistor 2SA562(Y)	
Q31	V04-0046-05	Transistor 2SD235(Y)	

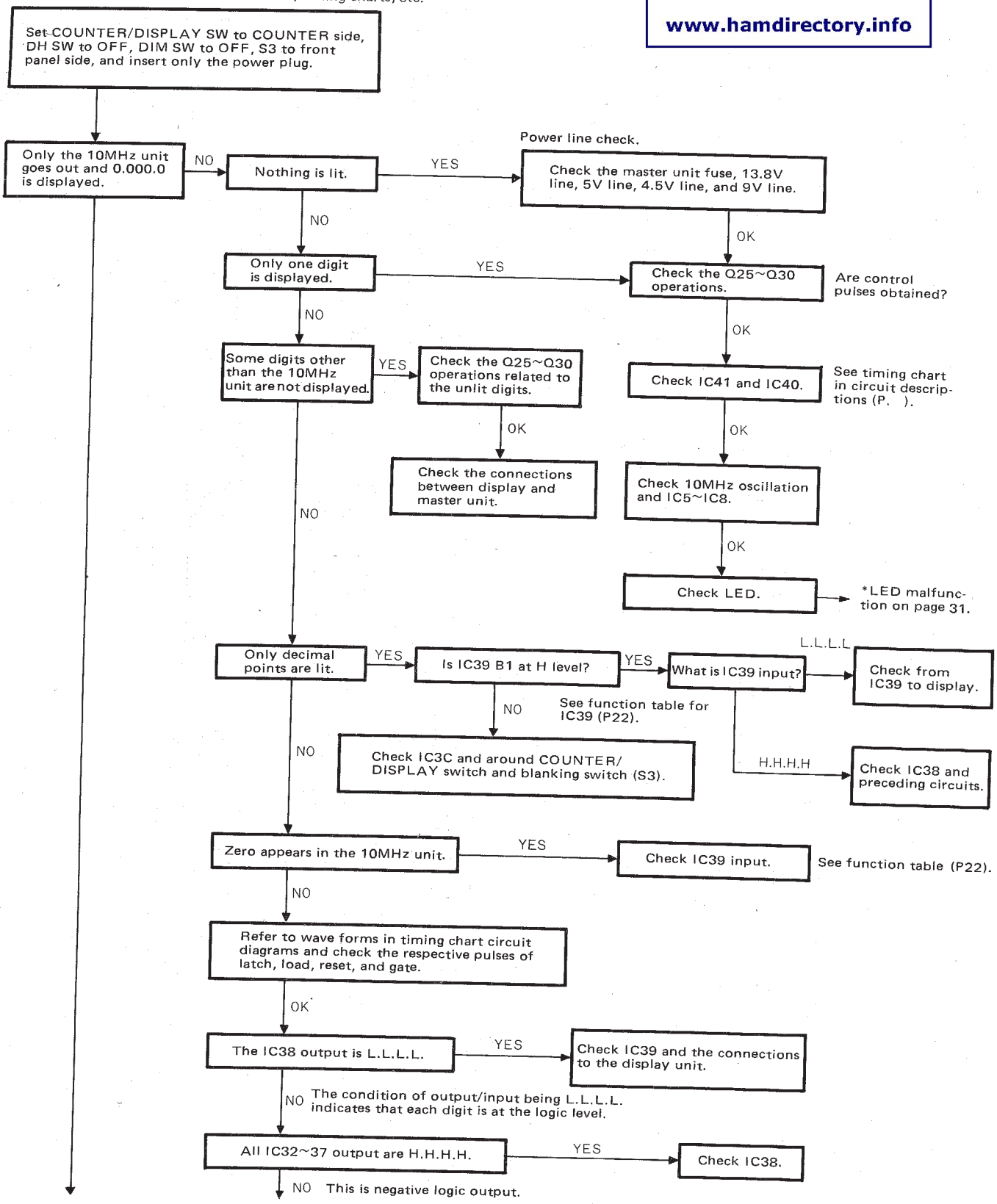
Ref. No.	Parts No.	Description	Remarks
D1~5	V11-0370-05	Diode 1S1587	
D6~11	V11-0051-05	Diode 1N60	
D12~16	V11-0370-05	Diode 1S1587	
D17	V11-0240-06	Zener diode WZ-090	
D18	V11-0270-05	Diode U05B	
D19	V11-0370-05	Diode 1S1587	
TRIMMER/CRYSTAL/COIL			
TC1	C05-0047-05	Ceramic trimmer 50pF	
X1	L77-0482-05	Crystal oscillator 10 MHz	
L1	L40-1001-03	Ferri-inductor 10μH	
L2~4	L40-4711-03	Ferri-inductor 470μF	
L5	L40-1511-03	Ferri-inductor 150μH	
L6~8	L40-4711-03	Ferri-inductor 470μH	
L9, 10	L40-1011-03	Ferri-inductor 100μH	
L11, 12	L40-4711-03	Ferri-inductor 470μH	
L14, 15	L40-1001-03	Ferri-inductor 10μH	
L16	L33-0601-05	Choke coil 2.2μH	
T1, 2	L34-0623-05	Tuning coil	☆
SWITCH			
S1	S40-2059-05	Push switch DH	
S2	S31-1005-05	Slide switch DIM	
S3	S31-1401-05	Slide switch BLK	☆
MISCELLANEOUS			
—	E02-0103-05	IC socket X 2	☆
—	E13-0162-05	Phone jack X 5	☆
—	E18-0201-05	Crystal socket	
—	E23-0046-04	Square terminal X 15	
—	E40-0816-05	Miniconductor wafer	
—	E40-1416-05	Miniconductor	

DISPLAY UNIT (X54-1270-00)

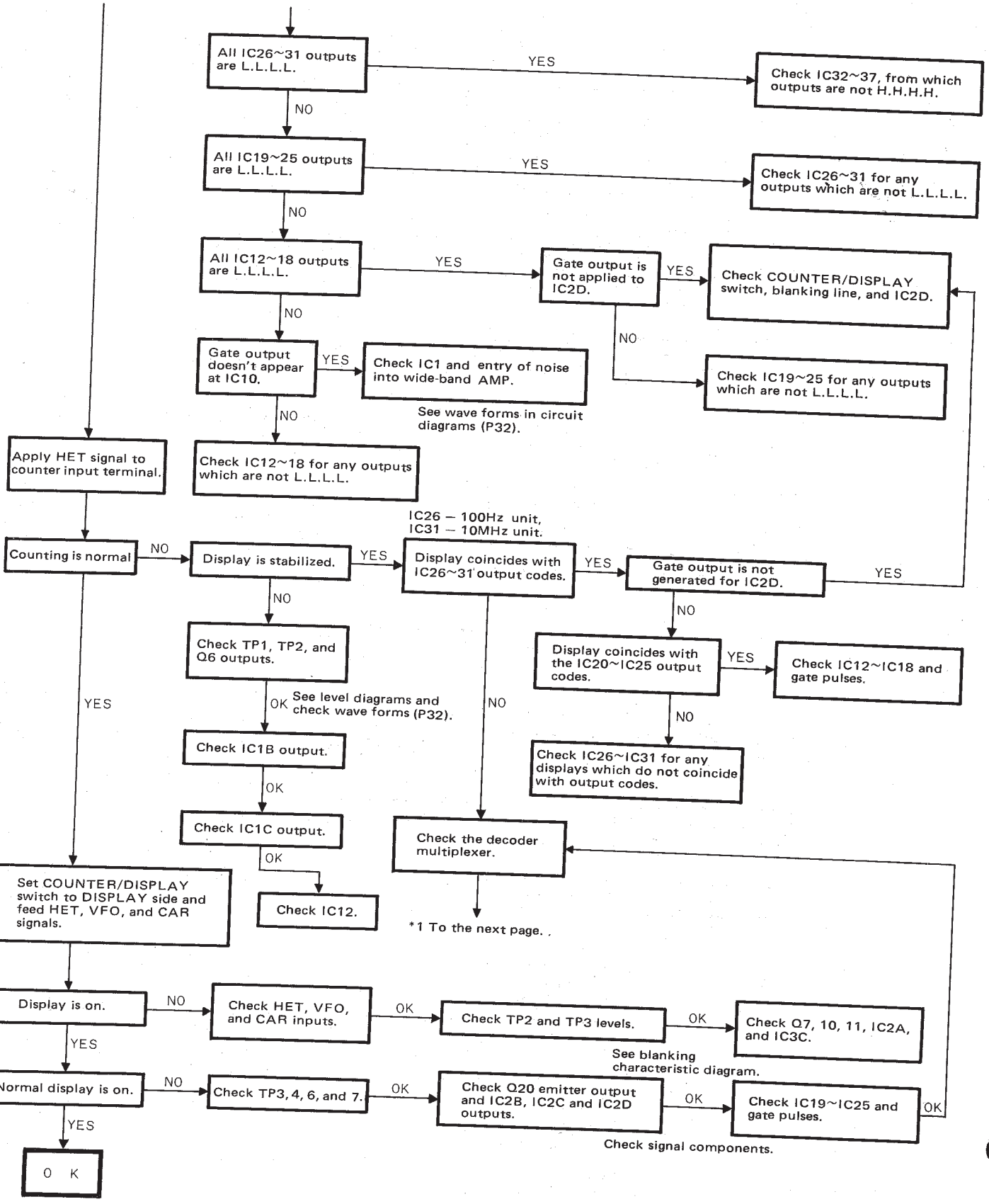
Ref. No.	Parts No.	Description	Remarks
D1~3	V11-3460-56	LED indicator GL-7R201	☆
D4	V11-0430-05	LED SEL-103W	
S1	S31-2401-05	Slide switch	☆
—	E40-0811-05	Miniconductor	
—	E40-1411-05	Miniconductor	
—	F15-0609-04	Blinding rubber	
—	F20-0501-04	Insulating plate	
—	J19-1301-04	Diode holder	

TROUBLE SHOOTING

Note: Check each item, and if any abnormality is found return to normal conditions before advancing to the next item. The following checks should always be carried out in accordance with the wave forms in circuit diagrams, level diagrams, IC function tables, timing charts, etc.



TROUBLESHOOTING



TROUBLESHOOTING

※ 1

The flow of signals in the multiplexer conforms to the selection off information for each digital unit as shown in the following table. Abnormality can be discovered easily if the control pulses are fixed to light up the defective LED only.

1) Stop the control pulses by cutting the pattern or jumper line between IC40 pin 14 and IC8 pin 11 .
2) When the control pulses are fixed, the lighting LED unit is fixed but its position cannot be determined in advance. To light the desired LED, use a lead wire which is connected to GND and touch it to the IC 14 pin. Each time the pin is touched, the lighting moves to the next LED unit. Repeat this process until the desired LED is lit.

Logic levels in multiplexer

Latch output/ multiplexer input	IC32 Y output	IC33 2Y	IC33 1Y	IC34 Y	IC35 Y	IC36 2Y	IC36 1Y	IC37 Y	IC38 2Y	IC38 2Y	IC38 1Y	IC38 4Y	Displayed unit:
A_1 B_1 C_1 D_1	H	$\overline{A_1}$	H	$\overline{B_1}$	H	$\overline{C_1}$	H	$\overline{D_1}$	A_1	B_1	C_1	D_1	100Hz unit
A_2 B_2 C_2 D_2	H	$\overline{A_2}$	H	$\overline{B_2}$	H	$\overline{C_2}$	H	$\overline{D_2}$	A_2	B_2	C_2	D_2	1kHz
A_3 B_3 C_3 D_3	$\overline{A_3}$	H	H	$\overline{B_3}$	$\overline{C_3}$	H	H	$\overline{D_3}$	A_3	B_3	C_3	D_3	10kHz
A_4 B_4 C_4 D_4	$\overline{A_4}$	H	H	$\overline{B_4}$	$\overline{C_4}$	H	H	$\overline{D_4}$	A_4	B_4	C_4	D_4	100kHz
A_5 B_5 C_5 D_5	$\overline{A_5}$	H	$\overline{B_5}$	H	$\overline{C_5}$	H	$\overline{D_5}$	H	A_5	B_5	C_5	D_5	1MHz
A_6 B_6 C_6 D_6	$\overline{A_6}$	H	$\overline{B_6}$	H	$\overline{C_6}$	H	$\overline{D_6}$	H	A_6	B_6	C_6	D_6	10MHz

A = L when $\overline{A}$ = H, A = H when $\overline{A}$ = L.
IC32~37 operate with negative logical outputs.

Calibration defective → Check Q23 and its vicinity. (See Fig. 9).

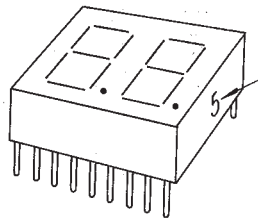
DH defective → Check Q24 and S1, and their vicinity. (See Fig. 16.)

DIM defective → Check IC40 and S2, and their vicinity. (See Fig. 21).

Refer to circuit descriptions.

※ 2 LED defective →

The luminance of LED's is classified into ranks. If those obtained cannot be in the same rank, then adjacent ranks may be used.



The rank indication (4~8) is here.

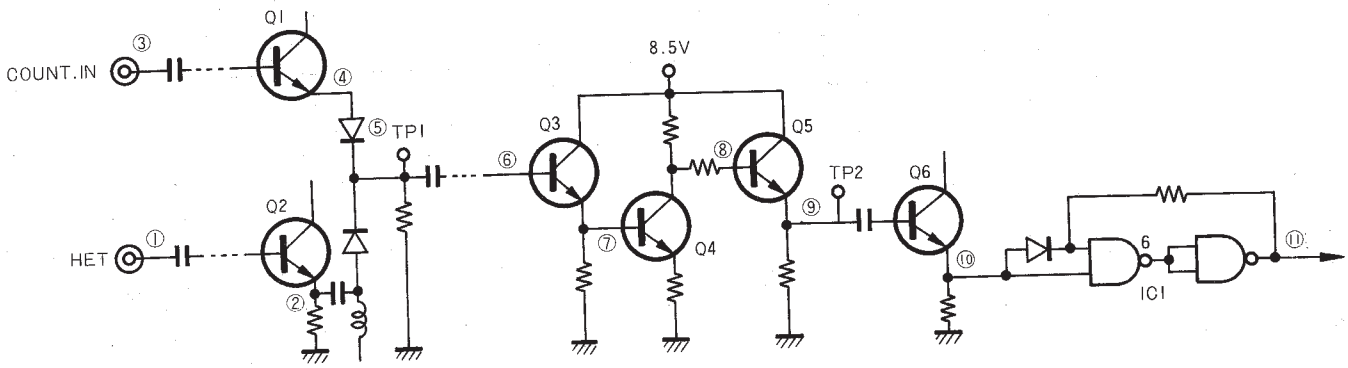
LEVEL DIAGRAM

* The levels at the HET, VFO, and CAR terminals are average values (in volts) when the DG-5 is connected to the master unit, TS-520S or V. If these values are changed, the levels in successive stages will also change.

Measuring Conditions

Use the TRIO VT-104 for 100kHz or below, and the Anritsu ML69 or M-316A for 100kHz or above.

HET/Counter Amplifier

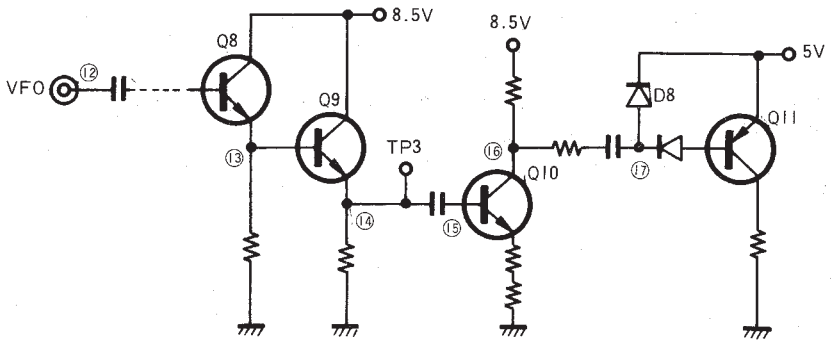


BAND or freq(MHz)	① ※ HET	② Q2(E)	③ COUNT.IN	④ Q1(E)	⑤ TP1	⑥ Q3(B)	⑦ Q4(B)
1.8	0.282	0.276			0.225	0.226	0.225
14.0	0.265	0.288			0.242	0.244	0.253
29.1	0.256	0.320			0.272	0.271	0.284
1kHz		AG-250	0.1	0.081	0.078	0.077	0.076
1MHz		SSG 50Ω 100dB INPUT	0.0915	0.075	0.0725	0.0705	0.0705
45MHz			0.0695	0.0535	0.0485	0.0335	0.0585

⑧ Q5(B)	⑨ TP2	⑩ Q6(E)	⑪ IC1 ⑥
1.77	1.34	1.02	1.37
1.52	1.23	1.06	1.40
1.30	1.08	1.03	1.40
2.58	2.45	2.45	1.48
2.25	1.97	1.97	1.11
0.805	0.735	0.73	0.755

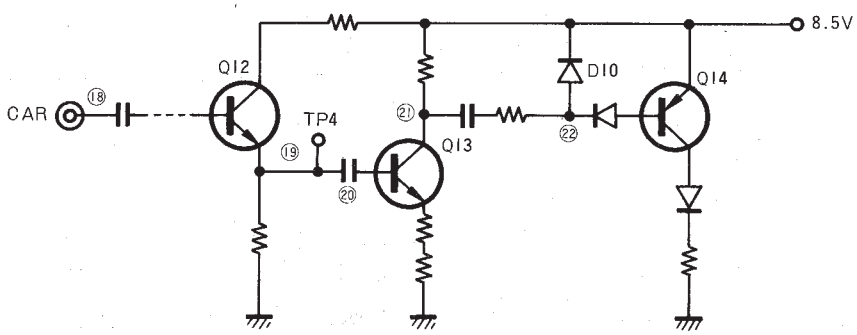
LEVEL DIAGRAM

VFO Amplifier



	⑫ ※ VFO	⑬ Q8(E)	⑭ TP3	⑮ Q10(B	⑯ Q10(C)	⑰ D8(K)
5.2MHz	0.325	0.32	0.315	0.106	1.52	0.61

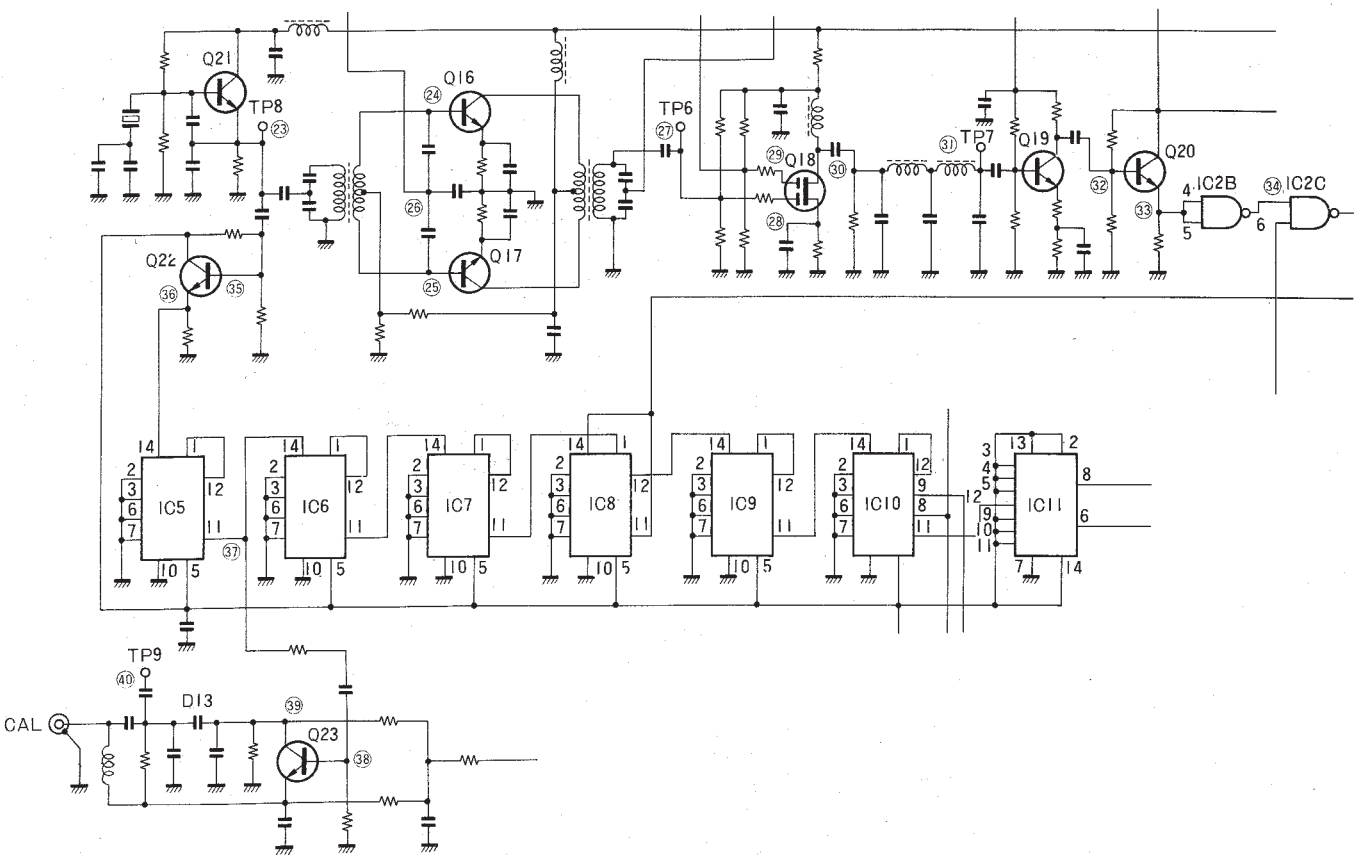
CAR Amplifier



	⑱ ※ CAR	⑲ TP4	⑳ Q13(B)	㉑ Q13(C)	㉒ D10(K)
3.395MHz	0.30	0.292	0.084	1.31	0.51

LEVEL DIAGRAM

Reference Oscillator, Calibration Circuit, Present Counter



㉓ TP8 (10MHz)	㉔ Q16(B)	㉕ Q17(B)	㉖ CAR IN (C47)	㉗ TP6	㉘ Q18(G1)	㉙ Q18(G2)	㉚ Q18(D)
2.31	0.159	0.0745	0.0385	0.33	0.31	0.123	0.65
			CAR OFF	CAR OFF	CAR OFF	VFO OFF	C.OFF 0.123
			0.032	0.03	0.0285	0.0455	V.OFF 0.53

㉛ TP7	㉜ Q20(B)	㉝ Q20(E)	㉞ IC2(6)	㉟ Q22(B)	㊱ Q22(E)	㊲ IC5(11)
0.142	1.27	1.03	1.44	1.2	1.08	1.46

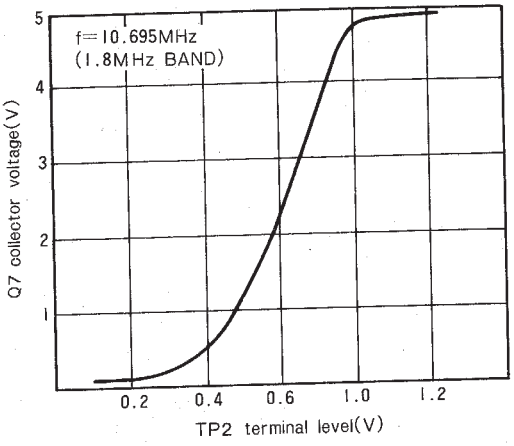
㊳ Q23(B)	㊴ Q23(C)	㊵ TP9
1.18	0.02	—
0.79	1.17	0.175
0.95	0.87	0.143

CAL terminal: OPEN,
CAL terminal: SHORT (GND)
CAL terminal connected to X VERTER IN terminal of master unit

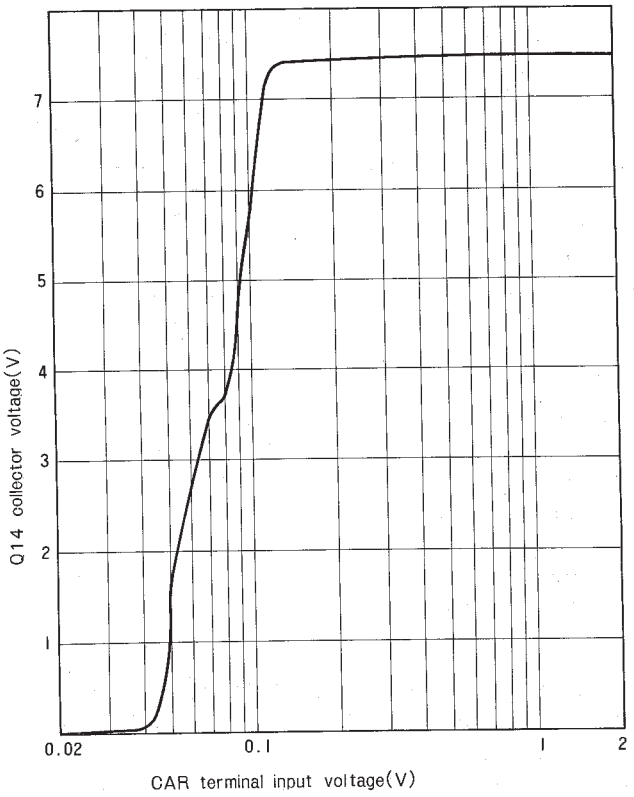
LEVEL DIAGRAM

Reference Data

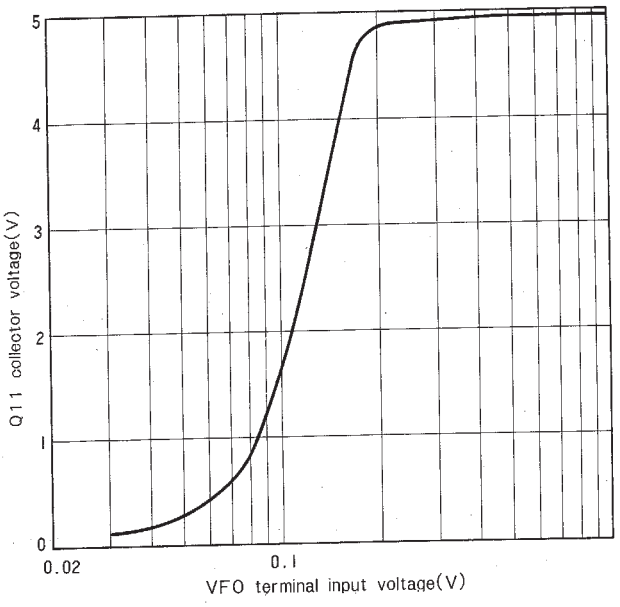
HET Blanking Switch Characteristic



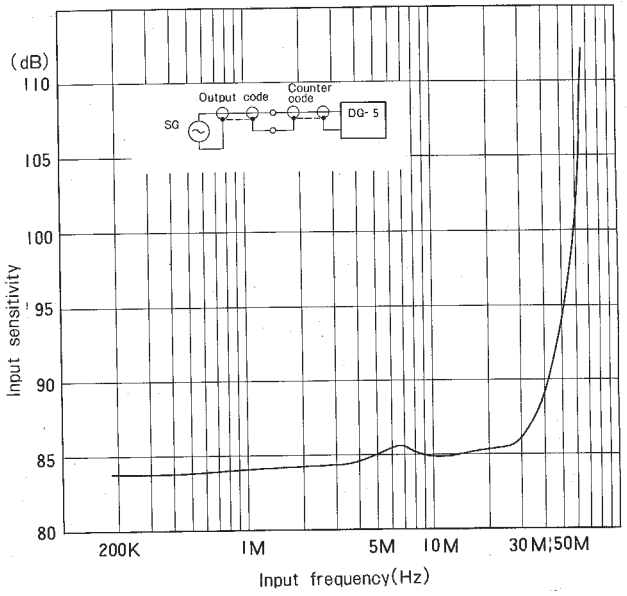
Switching Characteristic of CAR Detection



VFO Blanking Switch Characteristic



DG-5 Input Sensitivity VS Frequency Characteristic



DG-5

ADJUSTMENTS

Measuring Instruments

1. Voltmeter

1) Input resistance 1MΩ or more
2) Voltage range F.S. = 1.5~1000V AC, DC

2. RF valve voltmeter

1) Input impedance 1MΩ or more, 20pF or less
2) Voltage range F.S. = 10mV~300V
3) Measuring frequency range 50MHz or more

3. AF voltmeter

1) Measuring frequency 50Hz~10kHz
2) Input resistance 1MΩ or more
3) Voltage range F.S. = 10mV~30V

4. AF generator

1) Frequency range 100Hz~100kHz

5. SSG

1) Oscillating frequency 100kHz~40MHz
2) Output 120dB/μV or more

6. Oscilloscope

A 100MHz synchroscope is recommended (CS-1570 also acceptable).

7. Frequency counter

Stability should be 10^{-7} or more.

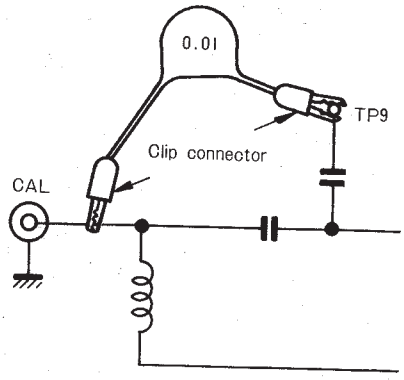


Fig. 27

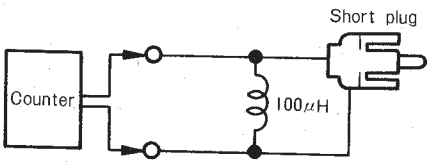


Fig. 28

1. Adjustment of 10MHz and 6.605MHz Tuning Coils (T1, T2)

(Instruments required)

RF valve voltmeter or oscilloscope

(Adjustment Procedure)

1) Apply the specified input (0.3V ± 3dB) to the VFO, CAR terminals from the master unit transceiver.
2) Connect TP7 with an RF valve voltmeter or an oscilloscope.
3) Adjust the T1 and T2 cores reciprocally to obtain a peak characteristic. The T1 core has a broad performance and it should not be turned too far.
4) Refer to the level diagram for the TP7 level.

2. Frequency Calibration for 10MHz Standard Oscillator

(Instruments required) o1) Frequency counter

1) Frequency counter
2) Measuring short plug

(Adjustment Procedure)

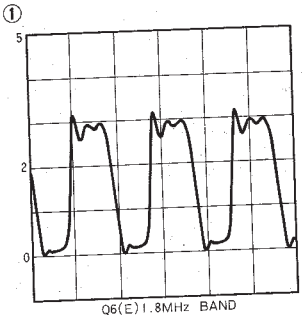
1) Insert a barium titanate capacitor (0.01μF) between DG-5TP9 and CAL terminal (Fig. 27).
2) Allow sufficient warm-up time (40 min. or more) in a case.
3) Connect a measuring short plug to the CAL terminal and also a frequency counter (Fig. 28).
4) Turn the trimmer capacitor (TC1) through the adjusting hole on the case bottom and adjust the frequency to 1MHz± 3Hz.
5) If a counter fails to measure because of cable capacitance, connect a 100 ~ 150MHz coil in series with TP9 so that the frequency can be adjusted to 1MHz. As another method, a WWV 15MHz wave can be used.

WAVEFORM

(The wave forms on the ICs

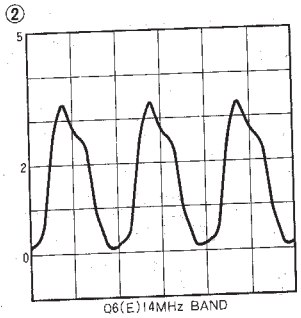
(See circuit diagrams.)

①



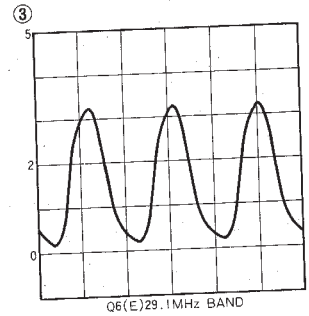
Q6(E) 1.8MHz BAND

②



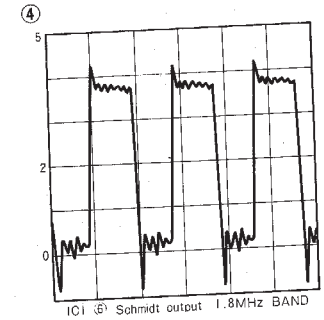
Q6(E) 14MHz BAND

③



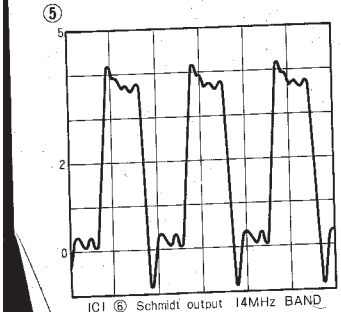
Q6(E) 29.1MHz BAND

④



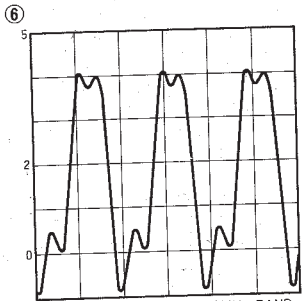
IC1 ⑥ Schmidt output 1.8MHz BAND

⑤



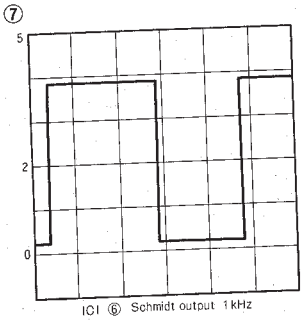
IC1 ⑥ Schmidt output 14MHz BAND

⑥



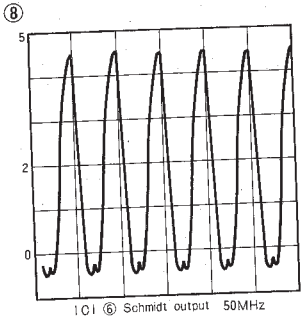
IC1 ⑥ Schmidt output 29.1MHz BAND

⑦



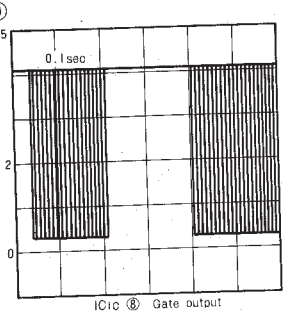
IC1 ⑥ Schmidt output 1kHz

⑧



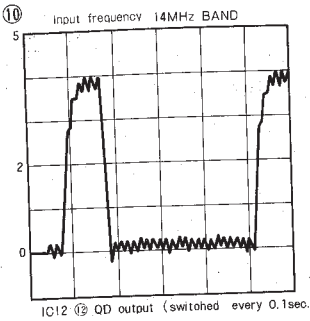
IC1 ⑥ Schmidt output 50MHz

⑨



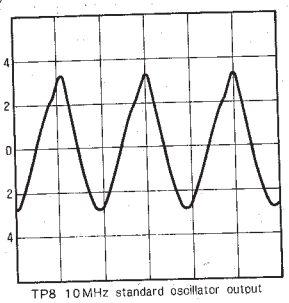
IC1c ⑧ Gate output

⑩ Input frequency 14MHz BAND



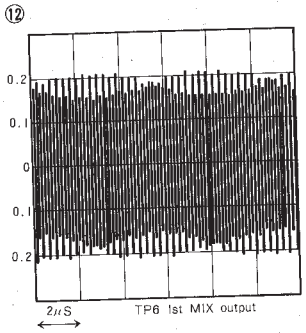
IC12 ⑫ QD output (switched every 0.1sec.)

⑪



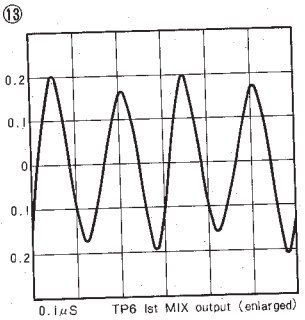
TP8 10MHz standard oscillator output

⑫



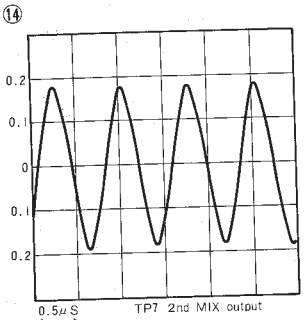
2μS TP6 1st MIX output

⑬



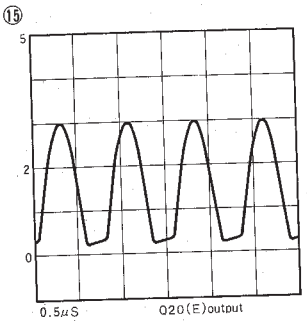
0.1μS TP6 1st MIX output (enlarged)

⑭



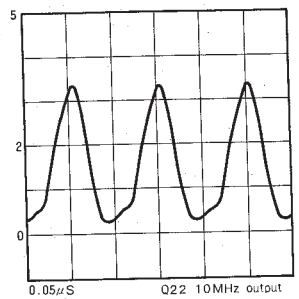
0.5μS TP7 2nd MIX output

⑮



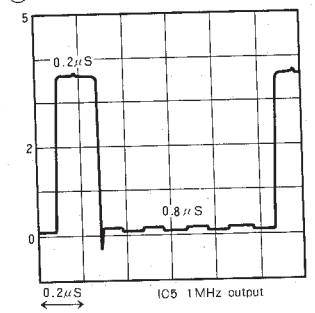
0.5μS Q20(E) output

⑯



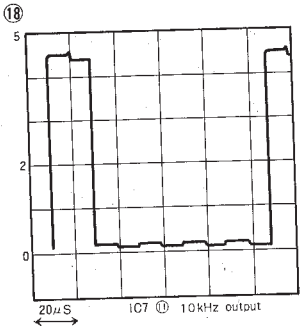
0.05μS Q22 10MHz output

⑰



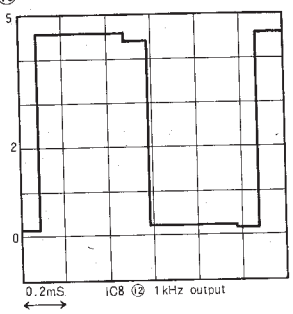
0.2μS IC5 1MHz output

⑱



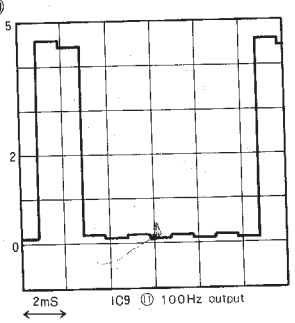
20μS IC7 ⑪ 10kHz output

⑲



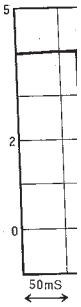
0.2mS IC8 ⑫ 1kHz output

⑳



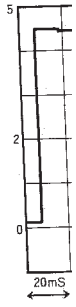
2mS IC9 ⑪ 100Hz output

㉑



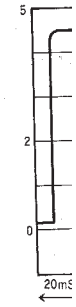
50mS

㉒



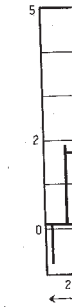
20mS

㉓



20mS

㉔



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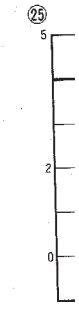
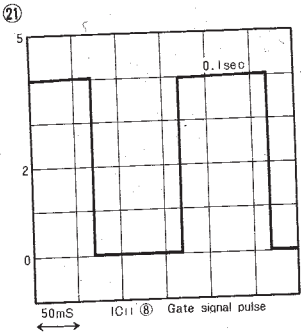


ORM

)rms on the ICs are closely related to the timing chart in the circuit descriptions.)

㉑



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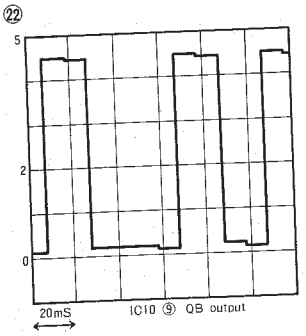

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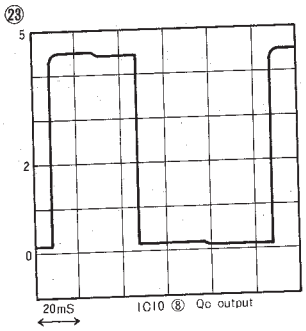

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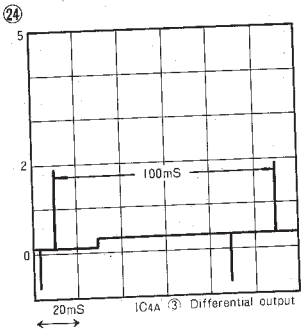

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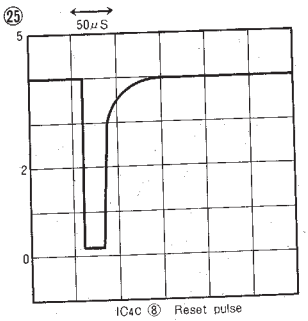

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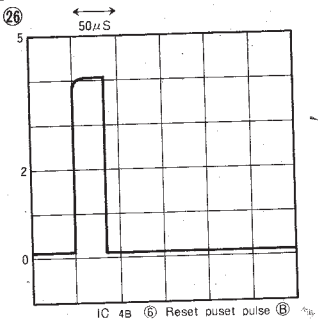

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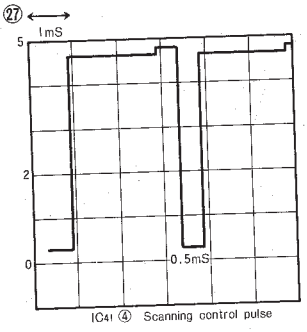

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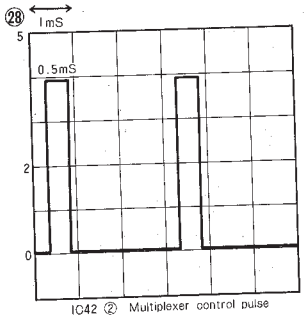

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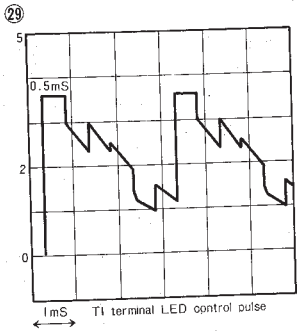

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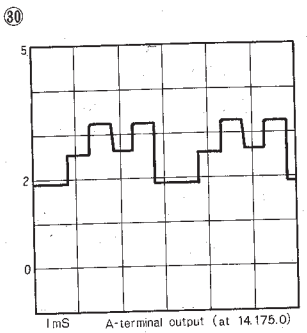
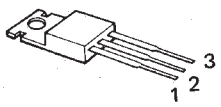
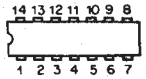


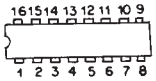
FS7805



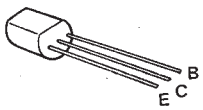
SN74S00N SN74176N
TD3400AP SN7454N
SN74LS90N TD3451AP
TD3472AP TD3492BP
SN74196N TD3404AP



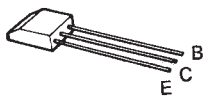
SN74LS75N
TD3447AP
TD3442AP



2SC945(R)
2SA733(R)

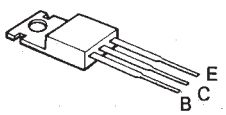


2SC460(B)



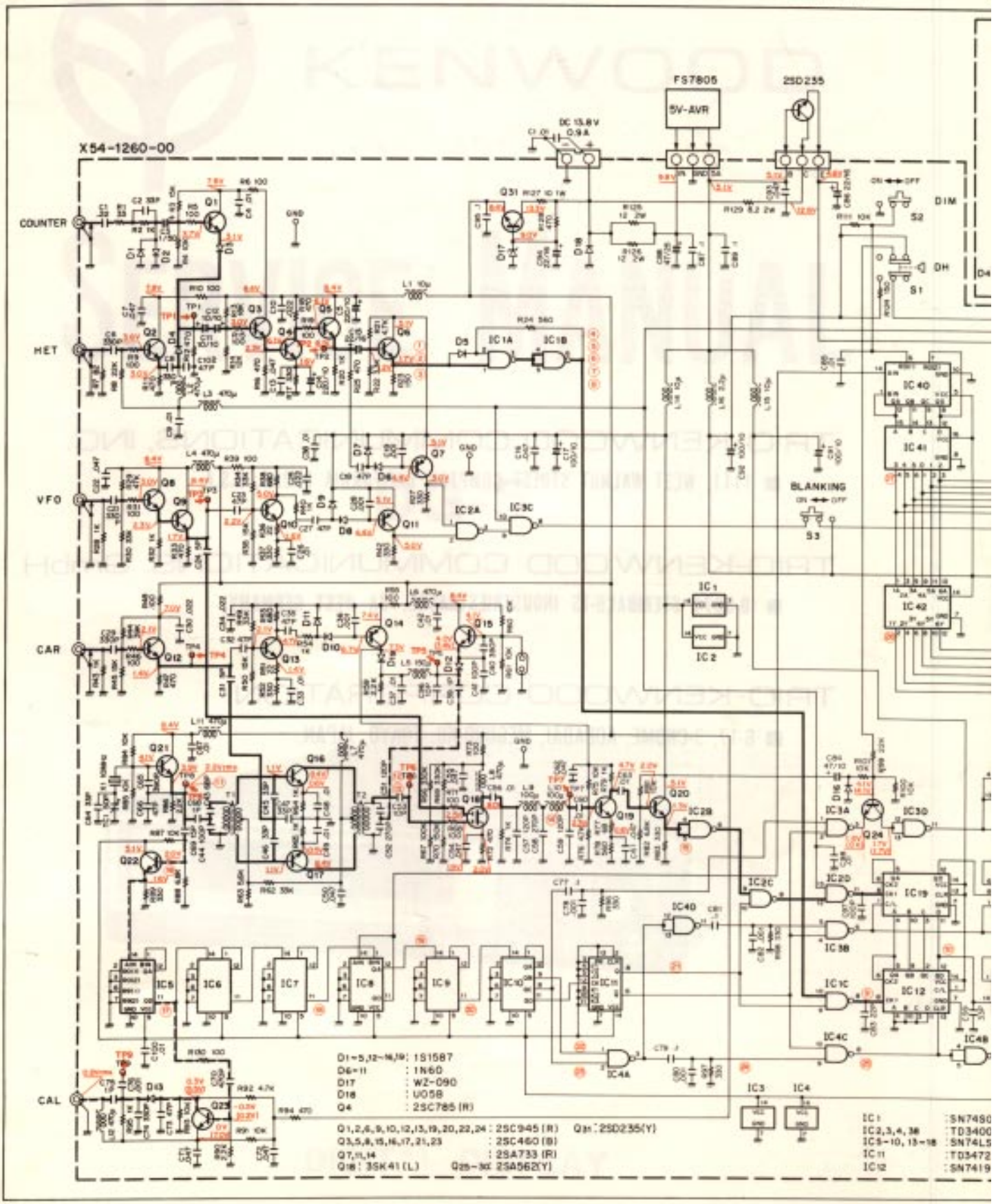
3SK41(L)

2SD235(Y)



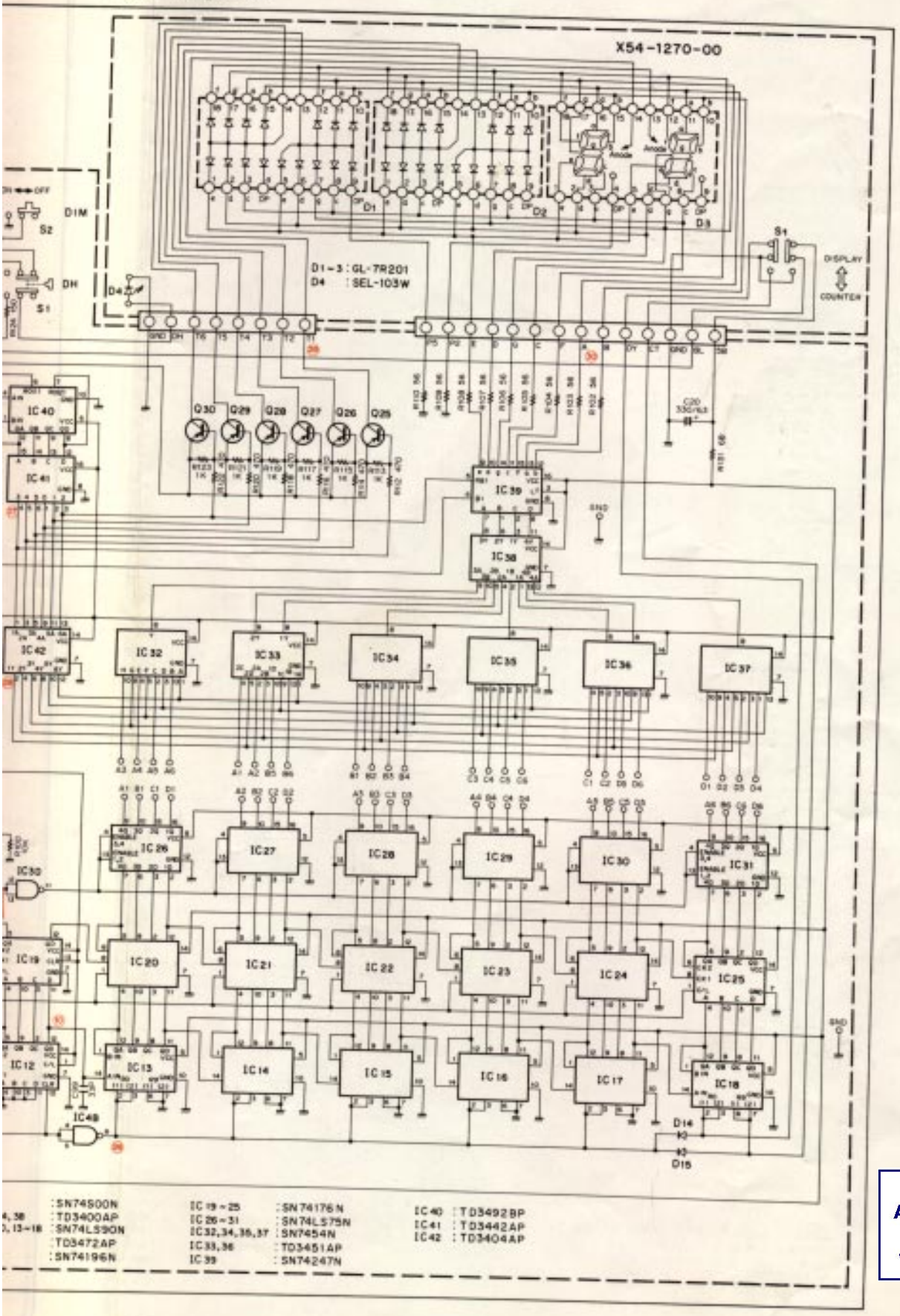
With regard to the numbers in this diagram, refer to the the wave forms on page 37.

——— Signal line ----------



SCHEMATIC DIAGRAM

..... Control signal line



	:SN74S00N	IC 19~25	:SN74176N	IC40	:TD3492BP
4, 38	:TD3400AP	IC 26~31	:SN74LS75N	IC41	:TD3442AP
0, 13~18	:SN74LS90N	IC32, 34, 35, 37	:SN7454N	IC42	:TD3404AP
	:TD3472AP	IC 33, 36	:TD3451AP		
	:SN74196N	IC 39	:SN74247N		

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■ D-6374 STEINBACH-TS INDUSTRIESTRASSE, 8A WEST GERMANY.

TRIO-KENWOOD CORPORATION

■ 6-17, 3-CHOME, AOBADAI, MEGURO-KU, TOKYO, JAPAN.