PUBLICATION NUMBER: 10372-0022-01A
JANUARY 1995

RT-1694(P)/PRC-138

SERVICE MANUAL

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When an Adult Stops Breathing

WARNING

DO NOT attempt to perform the rescue breathing techniques provided on this page, unless certified. Performance of these techniques by uncertified personnel could result in further injury or death to the victim.

1 Does the Person Respond?

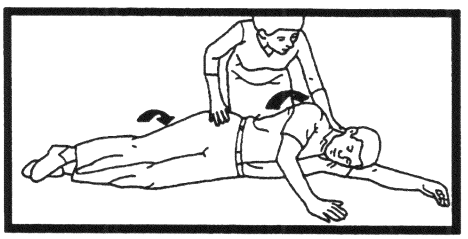
- Tap or gently shake victim.
- Shout, "Are you OK?"

2 Shout, "Help!"

- Call people who can phone for help.

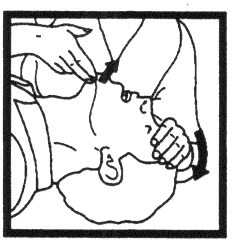
3 Roll Person Onto Back

- Roll victim toward you by pulling slowly.



4 Open Airway

- Tilt head back and lift chin.



5 Check for Breathing

- Look, listen, and feel for breathing for 3 to 5 seconds.

6 Give 2 Full Breaths

- Keep head tilted back.
- Pinch nose shut.
- Seal your lips tight around victim's mouth.
- Give 2 full breaths for 1 to 1-1/2 seconds each.

7 Check for Pulse at Side of Neck

- Feel for pulse for 5 to 10 seconds.

8 Phone for Help

- Send someone to call an ambulance.

9 Begin Rescue Breathing

- Keep head tilted back.
- Lift chin.
- Pinch nose shut.
- Give 1 full breath every 5 seconds.
- Look, listen, and feel for breathing between breaths.

10 Recheck Pulse Every Minute

- Keep head tilted back.
- Feel for pulse for 5 to 10 seconds.
- If victim has pulse but is not breathing, continue rescue breathing. If no pulse, begin CPR.

For more information about these and other life–saving techniques, contact your Red Cross chapter for training.
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ADDENDUM

ADDENDUM NO:	APPLIES TO (RF Model or Product Name):	DATE:
L1113	RT-1694(P)/PRC-138 Service Manual	August 1997

ADDENDUM TO (Publication Number/Revision):	FOR (Specific Application):
10372-0023-01 Rev. A	All Manuals

The following pages have been replaced in the RT-1694(P)/PRC-138 Service Manual:

- A1A1 Interface section, pages 17 through 37/38.
- A4 Signal Processor section, pages 5 through 42.
- A5 Receiver/Exciter section, pages 43 through 58.
- A8 Power Amplifier/Battery Charger Assembly section, pages 33 through 55/56.
- A9 Antenna Coupler section, pages 15 through 18, 31/32.
- A10 Front Panel section, pages 25 through 56.

HARRIS CORPORATION RF COMMUNICATIONS DIVISION ROCHESTER, NEW YORK 14610 USA
http://www.harris.com/rfc/

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SPECIFICATIONS FOR THE RT-1694(P)/PRC-138

GENERAL	
Frequency Range:	1.6 to 59.9999 MHz
Preset Channels:	100
Frequency Stability:	$\pm 1 \times 10^{-6}$ fo
Modes of Operation:	J3E (single sideband, upper or lower, suppressed carrier telephony H3E (compatible AM single sideband plus full carrier keyed tone) J2A (CW single sideband suppressed carrier keyed tone) F3E (FM telephony)
RF Input/Output Impedance:	50 ohms nominal, unbalanced
Power Input:	+24 Vdc
Antenna Tuning Capability:	50 ohm output: 1.6 to 60 MHz 8, 10, 16 ft. whips: 1.6 to 60 MHz AS-2259/GR (RF-1936): 3.5 to 10 MHz
Data Interfaces:	Synchronous and asynchronous RS-232C
Temperature Range:	–40° C to +70° C
Shock/Vibration:	MIL-STD-810D
Leakage:	MIL-STD-810D (1 meter depth)
Humidity:	MIL-STD-810D (0 to 95%)
Size:	RT-1694 only: 26.4W x 21.6D x 7.8H cm (10.4W x 8.5D x 3.1H in.) With battery: 26.4W x 33.8D x 7.8H cm (10.4W x 13.3D x 3.1H in.)
Weight:	3.86 kg (8.5 lb.) without battery 7.71 kg (17 lb.) with case and two Ni-Cd batteries

SPECIFICATIONS FOR THE RT-1694(P)/PRC-138 (CONT.)

RECEIVER

Sensitivity:	SSB: –110 dBm (0.7 uV) for 10 dB SINAD (2.7 kHz bandwidth) AM: –98 dBm (2.8 uV) for 10 dB SINAD (6 kHz bandwidth 30% modulation) CW: –117 dBm (0.3 uV) for 10 dB (S+N)/N (0.35 kHz bandwidth) FM: –113 dBm (0.5 uV) for 10 dB SINAD (with Preamplifier) FM: –107 dBm (1.0 uV) for 10 dB SINAD (without Preamplifier)
Audio Output:	15 mW @ 1000 ohms to external handset
Squelch:	Front panel adjustable
Image and IF Rejection:	Greater than 80 dB
Internal Spurious Responses:	Less than 10 greater than –90 dBm equivalent input fewer than 500 are greater than –120 dBm equivalent input
AGC Characteristics:	Mode dependent, selectable from front panel
Intermodulation Distortion:	In Band: –45 dB or better for two –20 dBm signals within the IF passband Out of Band: –80 dB or better for two –35 dBm signals separated 100 kHz or more
Overload Protection:	Receiver protected to 70 VRMS

TRANSMITTER

Power Output:	SSB, CW, AME: 1, 5, 20 watts PEP/Average FM: 1, 5, 10 watts
Carrier Suppression:	Greater than 60 dB below PEP output (J3E mode)
Undesired Sideband Rejection:	Greater than 60 dB below PEP output
Intermodulation Distortion:	1.6 – 29.9999 MHz: 24 dB minimum 30.0 – 59.9999 MHz: 18 dBm minimum
Audio Input:	Handset: 1.5 mVrms into 150 ohms Fixed Level: 0.774 Vrms into 600 ohms

NOTE

Because Harris engineers continuously strive to improve all aspects of our equipment, specifications are subject to change without notice.

SPECIFICATIONS FOR THE HIGH SPEED DATA MODEM

39-TONE MODE

Data Rates:	2400, 1200, 600, 300, 150, 75 bps
Transmission Mode:	Half duplex
FEC Coding:	(14, 10, 2) Reed-Solomon Code at 2400 bps (7, 3, 2) Reed-Solomon Code at lower bps rates
Interleaving:	Four levels (short, long, alternate short, alternate long)
Tone Library:	39 Tones, 675 to 2812.5 Hz, 56.25 Hz tone spacing; Doppler tracking tone: 393.75 Hz
Modulation:	TDQPSK (four-phase)
Demodulation:	128 point FFT
Doppler Correction:	+75 Hz; tracking up to 3.5 Hz per second
Channel Bandwidth:	3000 Hz

BINARY FSK MODE

Data Rate:	300, 150, 75 bps
Transmission Mode:	Half duplex
Signaling:	Phase Continuous Binary FSK
FSK Modes:	Front-Panel Selectable
	Wide Shift: 2000 Hz ±425 Hz (75, 150, 300 bps)
	Narrow Shift: 2805 Hz ±42.5 Hz (75 bps)
	Alternate: 2000 Hz ±85 Hz (75, 150 bps)
	Variable or Programmable Mark Space: 350 to 3000 Hz (75, 150, 300 bps)

DATA INTERFACES

Data:	Asynchronous (4800, 2400, 1200, 600, 300, 150, 75 baud), ASCII
	Synchronous (2400, 1200, 600, 300, 150, 75 baud; internal or external clock)
Control:	RTS CTS, XON-XOFF, CTRL-B (key), CTRL-C (unkey)
Electrical:	RS-232C, MIL-STD-188C
Remote Control:	Full function

SPECIFICATIONS FOR AUTOMATIC LINK ESTABLISHMENT MODULE

PROGRAMMING	
Parameters:	Radio channel groups, local addresses, individual (remote) addresses, network addresses, time of day, LQA start time and repeat interval, antenna coupler tune time, link timeout
Retention:	1 year minimum
CHANNELS	
Number:	100 simplex and/or half duplex
Frequency Range:	Operating: 1.6 to 59.9999 MHz Full Performance: 1.6 to 30 MHz
Modes:	USB, LSB, AME, FSK, CW, data, digital voice
SCAN	
Rate:	5 channels per second
Scanned Channels:	100 maximum
Channel Scan Groups:	10
SELECTIVE CALLING	
Types:	Individual, net, all call, selective all call may be placed from front panel or remote. Any calls, selective any calls, and wildcard calls may be placed from remote only. Group calls can be received, but not placed.
Link Protection:	Optional (per FED-STD-1045, when published)
Channel Selection:	Automatic or manual
Handshake:	3-way for individual, net, group, any, wildcard 1-way for allcalls
Other:	Digital squelch, listen before transmit (ALE traffic only), key-to-call
ADDRESSES	
Format:	1 to 15 character, alphanumeric
Local Addresses:	20 maximum
Network Addresses:	20 maximum
Individual Addresses:	200 maximum

SPECIFICATIONS FOR AUTOMATIC LINK ESTABLISHMENT MODULE (CONT.)

LINK QUALITY ANALYSIS	
Types:	Sounding (1 way) and exchange (3 way handshake)
Measurement:	Weighted average based on SINAD and pseudo bit error rate (PBER) as per MIL-STD-188-141A
Start Time:	Immediate, or programmed time-of-day
Repeat Interval:	One time, or interval (hours/minutes)
Addresses queued:	10 maximum
LQA score storage:	100 channels x 200 addresses x 2 directions
SIGNALING	
Modulation:	Phase continuous 8-ary FSK
Symbol Rate:	125 baud
Bit Rate:	375 bps
Coding:	Golay FEC, 2/3 majority vote, interleaving
Calling Cycle:	1 to 79 seconds (depending on call type, channels scanned, and call sign length)
BUILT IN TEST	
Functions Tested:	ALE, radio, power amplifier, antenna coupler
REMOTE CONTROL	
Interface:	RS-232C
Rate:	300 to 2400 baud asynchronous
Other:	2 stop bits, 8 data bits, no parity ASCII character based (compatible with existing RF-5000 remote control)

SPECIFICATIONS FOR THE VOICE PROCESSOR

GENERAL

Audio Input:	Handset connector: 1.5 mV RMS into 150 ohms 600-ohm auxiliary connector: 0/– 10 dBm

VOICE DIGITIZATION

Algorithm:	LPC-10-52E
Bit Rates:	2400 (single channel) or 800 bps (frequency hopping)
Bit Error Tolerance:	2×10^{-2} random BER for DRT greater than 80
Synchronization:	Frame synchronization at beginning of message
Tracking:	Continuous synchronization during message
End of Message:	End of message data or loss of tracking data for two seconds

ANALOG VOICE SECURITY (AVS)

Encryption Algorithm:	Split band inversion with time diversity scrambling
Bands:	24
Maximum Transmit Delay:	0.5 second
Number of Codes:	10^{+8}

SPECIFICATIONS FOR FREQUENCY HOPPING

GENERAL	
Frequency Range:	2.0 MHz to 29.9950 MHz
Hopping Restrictions:	Wide Band and List modes not available when internal antenna coupler is enabled or external antenna coupler is attached.
Hop Rate:	20 hops/second
Data Rate:	75, 150, 300 bps
Forward Error Correction:	Frequency diversity (all rates): 14, 10, 2 Reed-Solomon (75, 150, 300 bps)
Hop Nets:	10 (synchronization on only one of the ten nets)
Hopping Bandwidths:	Wide Band: Programmable Bandwidth: 70 kHz to 2 MHz Minimum Lower Frequency: 2.0 MHz Maximum Upper Frequency: 29.995 MHz Narrow Band: Center frequency: 15 MHz ≤ Fc ≤ 3.5 MHz Bandwidth: 300 kHz NB Spacing: 5 kHz Center frequency: 5 MHz ≤ Fc ≤ 15 MHz Bandwidth: 100 kHz NB Spacing: 2.5 kHz Center frequency: 3.5 MHz ≤ Fc ≤ 5 MHz Bandwidth: 50 kHz NB Spacing: 2.5 kHz Center frequency: 1.6 MHz ≤ Fc ≤ 3.5 MHz Bandwidth: 17.5 kHz (7.5 kHz – low; 10 kHz – high) Frequency List: Programmable Bandwidth: 70 kHz to 2 MHz Minimum Lower Frequency: 2.0 MHz Maximum Upper Frequency: 29.995 MHz
Frequency Spacing:	Wide Band Mode: 5 kHz Narrow Band Mode: 2.5 kHz, 5 kHz center frequency dependent Frequency List Mode: 5 kHz
Frequency List:	15 to 100 frequencies
Hopset Exclusions:	Sub-bands (10 total), Wide Band only
PN Generator:	Non-linear, repeat cycle > 5 years
Initial Sync Time:	29 seconds -- once per 24-hour period
Late Net Entry Time:	29 seconds

SPECIFICATIONS FOR FREQUENCY HOPPING (CONT.)

In-Net Message Sync:	Coarse Synchronization: continuous for up to 8 hours Fine Synchronization: 300 millisecond typical after key-down
Excision Filtering:	Excision of up to two single frequency interfering signals within the audio passband (typically provides greater than 25 dB equivalent filtering)

SPECIFICATIONS FOR DIGITAL ENCRYPTION

GENERAL	
Frequency Range:	The radio is capable of operating in digital voice mode from 1.6 MHz to 59.9999 MHz, and meets full performance specifications in this mode from 1.6 MHz to 29.9999 MHz
Algorithm:	LPC-10-52E
Bit Rates:	2400 bps in single channel or 800 bps in frequency hopping
Synchronization:	Frame synchronization at beginning of message
Tracking:	Continuous synchronization during message
End of Message:	End of message data or loss of tracking data for two seconds
PROGRAMMERS	
RF-5960 Master Code Programmer	The RF-5960 Master Code Programmer provides programming of the Data Encryption Option with six key codes with up to 1×10^{52} possible combinations in a portable configuration. Operates from 115/230 Vac, 50/60 Hz, or as a portable unit on an internal BB-590/U rechargeable Nickel-Cadmium battery. The internal battery is automatically recharged when operated on ac.
Available Codes:	1×10^{52} possible settings
Power:	115/230 Vac, 50/60 Hz, internal BB-590/U rechargeable Nickel-Cadmium battery
Size:	11.8H x 16.5W x 18.7D cm (5.38H x 7.5W x 8.5D in.)
Weight:	29 kg (11.5 lb.)
RF-5961 Field Code Programmer	The RF-5961 Field Code Programmer is a pocket-sized unit that permits programming of the Digital Encryption Unit option (each with six key codes having up to 10^{52} combinations). A self-contained lithium battery retains codes and has an emergency code dump feature. RF-5960 Master Code Programmer is required to insert codes.
Key Codes:	Stores six of the available 1×10^{52} codes for loading
Power:	Internal lithium battery
Size:	2.8H x 4.2W x 12.3D cm (1.25H x 1.93W x 5.6D in.)
Weight:	1.3 kg (0.5 lb.)

ABOUT THIS MANUAL

This manual contains information necessary to maintain and repair the RT-1694(P)/PRC-138 and its options.

SECTION 1

GENERAL INFORMATION

1.1 INTRODUCTION

The RT-1694(P)/PRC-138 Service Manual is intended for use with the FALCON™ Series Tactical Communications System AN/PRC-138 Manpack Installation & Operation Manual (10372-0008-01), which contains specifications and descriptions of the system components and options, as well as instructions for operation, programming, and remote control of the RT-1694(P)/PRC-138.

The RT-1694(P)/PRC-138 Service Manual describes maintenance procedures and troubleshooting of the RT-1694 through the use of self-test routines. These routines enable the user to isolate system faults to the board level. Instructions are given for interpreting failure codes and for replacing faulty assemblies. Where applicable, instructions are given for component-level repair by a skilled technician who has a good working knowledge of radio circuitry, microprocessor operation, and standard test equipment use, including voltmeters, logic probes, and oscilloscopes.

1.2 HOW TO USE THIS MANUAL

This General Information section contains general maintenance information for the RT-1694. It is important to read and understand this section before attempting the board-level maintenance procedures described in the following paragraphs.

Subsection 1.3 describes the physical characteristics of the RT-1694.

Subsection 1.4 describes general maintenance information, such as required tools and test equipment, maintenance repair kits, and general repair procedures.

Subsection 1.5 describes operational, warning, and fault messages that may appear on the front panel display of the RT-1694 during operation.

Subsection 1.6 covers preventive maintenance.

Subsection 1.7 contains battery information and precautions.

Subsection 1.8 describes performance of self-test routines, including a list of assembly numbers and fault codes.

Subsection 1.9 describes assembly access and removal, and use of extender cards and card guides.

Subsection 1.10 describes general techniques that should be followed when troubleshooting the assemblies of the manpack.

Subsection 1.11 provides procedures for checking receiver sensitivity.

Subsection 1.12 provides procedures for checking output power.

Subsection 1.13 provides procedures for measuring transmit frequency.

Subsection 1.14 includes block diagrams of the RT-1694 receive and transmit paths, and an interconnect diagram showing the flow of signals among the assemblies.

Following the General Information section are individual sections for each standard and optional assembly. Each of the assembly sections follows the same format:

- General Description: Provides an overview of the basic functions of each assembly, including the major subassemblies that comprise the assembly.
- Interface Connections: Includes tables for each assembly connector showing the names of signals, along with brief notes regarding signal functions and levels.
- Technical Description: Provides a functional description of each assembly, including block diagrams and theory of operation to assist in maintenance and troubleshooting operations.
- Testing and Alignment: Gives detailed test and alignment procedures.
- BITE Faults and Troubleshooting: Describes possible causes for each self-test fault code. Offers hints and suggestions for tracing the faults to specific components.
- Parts Lists, Component Location Diagrams, and Schematic Diagrams

1.3 PHYSICAL CHARACTERISTICS

Figure 1-1 shows the RT-1694 front panel controls, indicators, and connectors. Tables 1-1, 1-2, and 1-3 list functions and signal levels for the radio's front-panel connectors.

All operator interfacing with the RT-1694 is done through the front panel or remote port. The assembly numbers are shown in table 1-4. The locations of the internal assemblies in the chassis are shown in figure 1-2.

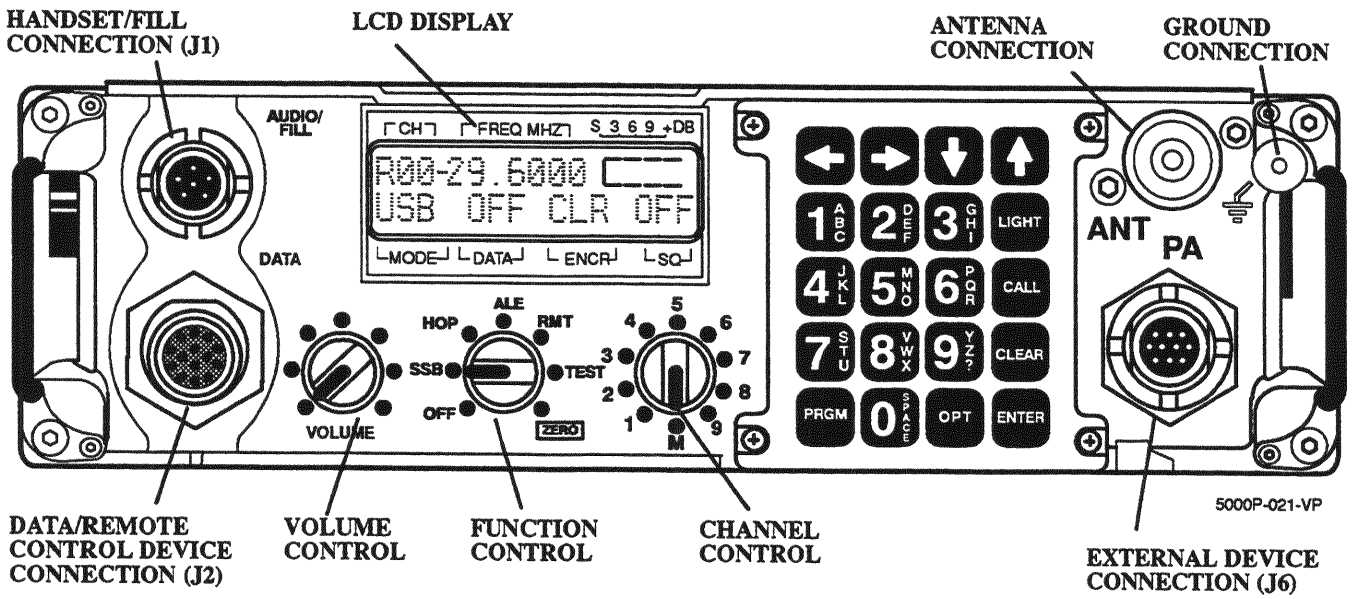


Figure 1-1. Front Panel Controls, Indicators, and Connectors

Table 1-1. Front-Panel Connector J1 AUDIO/FILL Input/Output Signals

Connector and Pin	Signal	Comments
J1-A	Ground analog	Ground
J1-B	Receiver audio output	≥3.87 volts rms audio into 1 K ohm load, variable vol.
J1-C	PTT keyline input or fill RTS input	PTT active low pull down to ground/or 0 V, +5 V CMOS levels
J1-D	Transmit microphone audio input	1.5 mV rms ±10%, Zin = 150 ohms ± 10%
J1-E	Retransmit keyline output or fill clock output	0 V, +5 V CMOS levels
J1-F	Fill data I/O	0 V, +5 V CMOS levels

Table 1-2. Front-Panel Connector J2 DATA Input/Output Signals

Connector and Pin	Signal	Comments
J2-A	Fixed level RX audio out	2.2 Vp-p, 10 Hz – 10 kHz, Rout = 600 ohms
J2-B	Fixed level TX audio in	2.2 Vp-p, 10 Hz – 10 kHz, Rin = 100 K
J2-C	Data out	RS-232C ±12 V levels or MIL-STD-188-114A ±6 V level
J2-D	Data in	RS-232C ±12 V levels or MIL-STD-188-114A ±6 V level
J2-E	+ Battery output /or remote power on input	+19.5 V to +32 V, 0.1A max/or active low pull down to ground (internal jumper selectable)
J2-F	TX keyline	+5 V CMOS input, active low pull down to ground
J2-H	RLSD	Output, RS-232C ±12 V levels or MIL-STD-188-114A ±6 V level
J2-J	Ground	Ground
J2-K	Remote async data in	RS-232C ±12 V levels or MIL-STD-188-114A ±6 V level
J2-L	CTS	Output, RS-232C ±12 V levels or MIL-STD-188-114A ±6 V level
J2-M	Sync clock in	RS-232C ±12 V levels or MIL-STD-188-114A ±6 V level
J2-N	Remote async data out	RS-232C ±12 V levels or MIL-STD-188-114A ±6 V level

Table 1-2. Front-Panel Connector J2 DATA Input/Output Signals (Cont.)

Connector and Pin	Signal	Comments
J2-P	RTS	Input, RS-232C ±12 V levels or MIL-STD-188-114A ±6 V level
J2-R	Sync clock out	RS-232C ±12 V levels or MIL-STD-188-114A ±6 V level

Table 1-3. Front-Panel Connector J6 PA CONTROL Input/Output Signals

Connector and Pin	Signal	Comments
J6-A	Hop clock	0 V, +5 V CMOS levels
J6-B	PA control data –	0 V, +5 V differential asynch control data, 150 K baud
J6-C	PA control data +	0 V, +5 V differential asynch control data, 150 K baud
J6-D	/PA POWER ON	0 V, +5 V CMOS levels, active low
J6-E	Ground return battery charger	DC ground return
J6-F	Ext R/T DC–	DC ground return
J6-G	PA feedback –	PA feedback ground return
J6-H	PA feedback +	PA analog feedback sense, minimum – +0.5 V, typical – +4.3 V, maximum – +7.0 V
J6-J	Ext Charger DC +	+10 V to +32 V, 4.0A maximum
J6-K	Ext R/T DC +	+19.5 V to +32.0 V, 1.0A maximum, (100 mW exciter mode only)

Table 1-4. Assembly Numbers for the Manpack

Assembly Number	Description
A1	Interface Assembly/Encryption Assembly
A3	LPC Assembly
A4	Signal Processor Assembly
A5	Receiver/Exciter Assembly
A6	Synthesizer/Reference Generator Assembly
A7	Power Supply Assembly
A8	Power Amplifier/Harmonic Filter Assembly

Table 1-4. Assembly Numbers for the Manpack (Cont.)

Assembly Number	Description
A9	Coupler Assembly
A10	Front Panel Assembly
A11	Motherboard/Interconnect Assembly

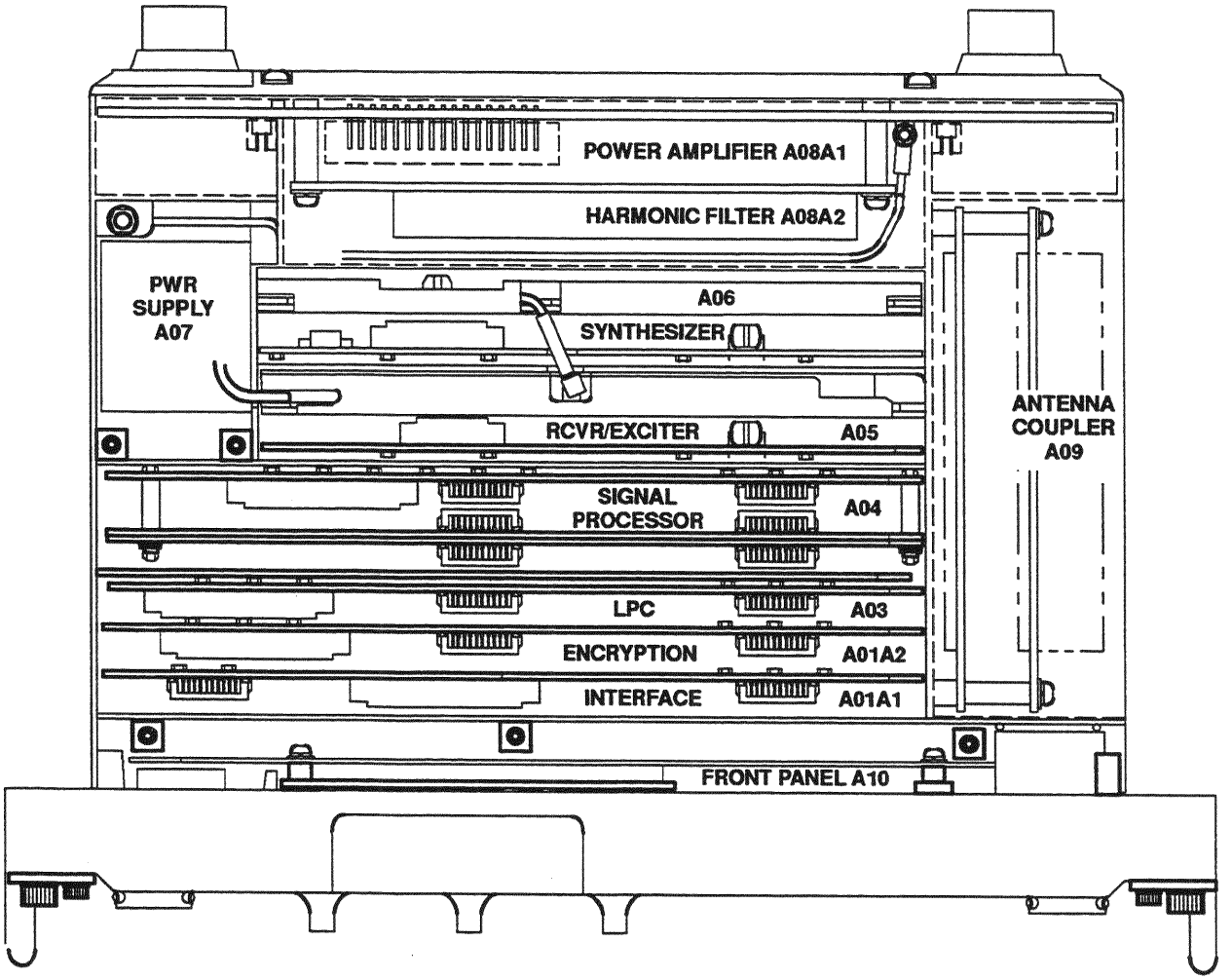


Figure 1-2. Location of Plug-In Assemblies

1.4 GENERAL MAINTENANCE

The RT-1694 Receiver-Transmitter is designed so that most repairs can be made by assembly substitution. The following subsections list recommended tools, test equipment, items contained in the maintenance repair kit, and general maintenance procedures.

1.4.1 Tools

Table 1-5 is a list of tools required for disassembly and reassembly of the RT-1694.

Table 1-5. Tools Required to Disassemble/Reassemble the RT-1694

Tools	
Phillips No. 1 Screwdriver	Nut Driver, 5/16 in.
Needle-Nose Pliers	Nut Driver, 3/16 in.
Bristol Spline Wrench .060"	Nut Driver. 1/8 in.
Allen Wrench, 3/32 in.	Spanner Wrench (Harris P/N 10150-0226)
Allen Wrench, 5/32 in.	Socket, 1-1/16 in.
Slide Bar Handle, 3/8 in.	Adapter, 3/8 in. to 1/2 in.

1.4.2 Test Equipment

Table 1-6 is a list of recommended test equipment for alignment and troubleshooting of RT-1694 assemblies. The recommended piece of equipment or its equivalent may be used.

Table 1-6. Test Equipment for RT-1694 Assemblies

Test Equipment	Required Characteristics
Power Supply	Regulated Voltage: 0 to 40.0 Vdc Current: 5 A Hewlett Packard HP-6291A
Spectrum Analyzer	Frequency Range: 30 Hz to 2.9 GHz Displayed average noise level to +30 dBm Hewlett Packard HP-8560 or equivalent
RF Signal Generator (2)	Synthesized Frequency Range: 100 kHz to 1040 MHz Resolution: 10 Hz Output Range: –143 dBm to +13 dBm Hewlett Packard HP-8657A or equivalent
Frequency Counter	Frequency Range: 30 Hz to 100 MHz Accuracy: 0.1 PPM Hewlett Packard HP-5316B or equivalent
Audio Analyzer	Frequency Range: 20 Hz to 100 kHz Resolution: 100% Hewlett Packard HP-8903B or equivalent
RF Millivoltmeter with T Voltage Sensor	200 uV to 3 V Boonton 92E or equivalent

Table 1-6. Test Equipment for RT-1694 Assemblies (Cont.)

Test Equipment	Required Characteristics
Digital Voltmeter	200 mV to 250 Vac 200 mV to 200 Vdc 0 to 20 Megohms Accuracy: 1% Fluke 8012A or equivalent
50-ohm Attenuator	30 dB, 50 ohms Narda 77B6-30 or equivalent
Remote Data Terminal	RS-232 Asynchronous, ASCII
Personal Computer	IBM PC Compatible with DOS 3.0 or higher and FALCOM software 10372-9868 Remote Control Data Cable
Oscilloscope	General Purpose Input Range: 5 mV to 200 V ac/dc Frequency Response: DC to 100 MHz Bandwidth Probes: 10X, 1 Megohm, and 100 MHz Tektronix 465 or equivalent

1.4.3 Repair/Maintenance Kit

A repair/maintenance kit is available that contains general items, tools, cables, and adaptors to facilitate servicing the RT-1694. The repair kit is intended to supplement a well-equipped service facility. Table 1-7 lists the contents of the RT-1694 Repair/Maintenance Kit.

Table 1-7. RT-1694 Repair/Maintenance Kit Parts List (1005-5188 Rev. B)

Ref. Desig.	Part Number	Description
	10372-7860	PWB ASSY, EXT, 1,2&3 CONV
	10372-7870	PWB ASSY, EXT, REFGEN/SYN
—	10372-7800	EXTENDER BD ASSY, INTERFA
—	10372-7810	EXTENDER BD ASSY, SIGNAL
—	10372-7820	EXTENDER BD ASSY,RCVR EXI
—	10372-7830	EXTENDER BD ASSY, SYNTHES
—	10372-7840	EXTENDER BD ASSY, ENCRYPT
—	10372-7850	EXTENDER BD ASSY, LPC
—	10181-1457-001	BNC/BNC 2 MTR COAX CABLE
—	Z80-0001-000	TUNING TOOL
—	Z80-0003-001	TUNING TOOL,4192
—	P60-0001-001	COMPOUND, HEATSINK 340
—	10372-7803	MOUNTING PLATE,ENCRYPTION
—	10372-7813	PLATE ASSEMBLY,3-BD SET
—	10303-9120	PWB ASSY, DISCRIM FIXTURE
—	10372-9320	CARD, PARTS LOCATOR
—	10372-9300	PRC-138 BREAKOUT KIT
—	10181-1455-220	CABLE ASSY, M-F RIBBON
—	10181-1455-234	CABLE ASSY, M-F RIBBON

Table 1-7. RT-1694 Repair/Maintenance Kit Parts List (1005-5188 Rev. B) (Cont.)

Ref. Desig.	Part Number	Description
—	10150-9543	BNC TO NANOHEX COAX CABLE
—	10372-1053-01	CABLE ASSY, RF (PA-R/E)
—	Z85-0016-001	TEST CABLE BLACK SMD 8"L
—	Z85-0016-201	TEST CABLE RED SMD 8"L
—	Z90-0012-002	WRENCH, BRISTOL, 6 SPLINE
—	Z90-0012-901	HANDLE,BRISTOL,SPLINE 2"L
—	SK-0421	SCRWDRVR PHILLIPS
—	SK-0422	SCRWDRVR PHILLIPS
—	Z90-0010-002	NUTDRIVER 5/16"
—	Z90-0024-002	NUTDRIVER 1/8"
—	Z90-0014-006	NUTDRIVER, 3/16",NARROW T
—	Z90-0021-001	SLIDE BAR HANDLE
—	Z90-0021-002	SOCKET ADAPT 3/8" TO 1/2"
—	Z90-0022-001	TORQUE SCREWDRIVER
—	Z90-0023-107	BIT 1/4" DRIVE #1PH
—	Z90-0015-301	PLIERS,NEEDLE NOE, LONG
—	Z90-0025-001	HEX WRENCH SET,INCH
—	Z90-0020-717	SOCKET 1/2" DIRVE X 1 1/1
—	J92-0027-001	CONN SSMB BHD ADPTR M-M
—	Z90-0023-108	BIT 1/4" DRIVE #2PH
—	Z90-0023-007	BIT 1/4" DRIVE 5/32 HEX
—	Z90-0023-003	BIT 1/4" DRIVE 3/32 HEX
—	UG-914/U	CONN ADP BNC F-F
—	UG-201A/U	CONN ADP BNC-M/N-F
—	10150-0226	SPANNER WRENCH
—	10372-9310-01	TRANSIT CASE ASSY
—	10181-1482-222	CABLE ASSY, HARM FLTR

1.4.4 General Maintenance Procedures

The design of modern communications equipment includes the use of complementary-metal-oxide-semiconductor (CMOS) devices, microprocessors, memory, and surface-mount devices to enhance operational performance and minimize size and power consumption requirements. Servicing of the RT-1694 should be performed in accordance with proper maintenance standards, especially with respect to static-sensitive devices, surface-mounted component removal, and soldering techniques.

1.4.4.1 Static-Sensitive Devices

Follow these precautions to protect static-sensitive CMOS devices from damage:

- Keep all static-sensitive devices in their protective packaging until needed. This packaging is usually conductive and should provide adequate protection for the device. Storing or transporting static-sensitive devices in conventional plastic containers could be destructive to the devices.
- Remove power to a unit before inserting or extracting a static-sensitive device. This also applies to printed wiring boards that contain static-sensitive devices.
- Double check test equipment voltages and polarities before conducting any tests. Verify that no transients exist.

CAUTION

Use only properly-grounded soldering irons and tools. The use of ungrounded soldering tips destroys these devices. Never use soldering guns.

- Avoid contact with the leads of the device. The component should always be handled very carefully by its ends or by the side opposite the leads.
- While handling static-sensitive devices or assemblies containing them, avoid contact between synthetic clothing and printed wiring board circuits or component leads.

It is good maintenance practice to equip each maintenance position with a static-safe work station. A static-safe work station consists of a table mat, floor mat, and associated grounding straps. The material used for the mats provides intrinsic conductivity which drains static charges on personnel, conductive storage bags, equipment, etc., to ground before the static charge is able to cause damage to microelectronic devices.

The 3M Corporation manufactures a series of static work station kits. It is recommended that the service area for the RT-1694 be equipped with the 3M™ 8020 Series Work Station or equivalent. The kits must be installed according to the manufacturer's instructions to ensure maximum effectiveness and safety.

All spare assemblies should be stored in static-shielding bags for protection from static discharge and dust.

1.4.4.2 Surface-Mount Devices

A number of modules in the RT-1694 contain surface-mount devices. Special repair equipment is required to replace and repair assemblies using surface-mount devices. Table 1-8 is a list of equipment recommended to establish a surface-mount device repair and rework station.

The 7A1 SMD Rework Kit is not suitable for use with the RT-1694, which requires the use of the Surmount I SMD Repair Station because of its greater positioning accuracy.

Repair of surface-mount devices should only be attempted by a skilled technician who has specific training in working with these devices and the associated repair equipment.

Table 1-8. Equipment for Surface-Mount Devices

Equipment	Manufacturer	Model Number	Quantity
Solder Removal Station	HAKKO	9670	1
Soldering Iron	HAKKO	926	2
Hot Plate	Thermolyne	HP-A1915B	1
SMD Repair Station	Vitronics	Surmount I	1

1.4.4.3 Suggested Torque Values for Stainless Steel and Nonferrous Fasteners (Inch Series)

The torque values listed in table 1-9 are suggested maximums. Dry or near dry fasteners should be wiped clean of chips and foreign matter before torqueing. For other friction conditions, significant adjustments in assembly torques may be required.

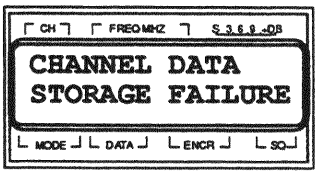
Table 1-9. Torque Tensioning

Nominal Fastener	Brass (in lbs)	Silicon Bronze (in lbs)	316 Stainless (in lbs)
2-56	2.0	2.3	2.6
4-40	4.3	4.8	5.5
6-32	7.9	8.9	10.1
8-32	16.2	18.4	20.7
10-24	18.6	21.2	23.8
10-32	25.9	29.3	33.1
1/4-20	61.5	68.8	78.8
5/16-18	107	123	138
5/16-24	116	131	147
3/8-16	192	219	247
3/8-24	212	240	271

1.5 RT-1694 SYSTEM MESSAGES

The following paragraphs show operational, warning, and fault messages that may appear on the front-panel display during operation. The messages include explanations and, where appropriate, recommendations for action.

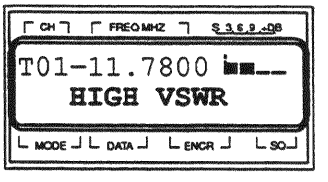
Situation: Each time the power is turned on, the channel data is checked. If the channel data has been corrupted, this message displays before initialization. The radio then zeroizes due to the RAM becoming corrupt.



Action: Reprogram radio; it may be appropriate to replace the memory backup battery (refer to subsection 1.7.5).

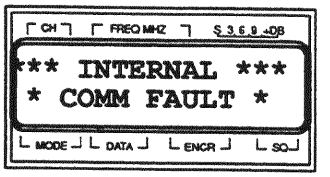
Situation: Antenna VSWR greater than 3.0:1.

Action: Retune by selecting RETUNE from the OPTION menu and pressing the ENTER key. Measure VSWR in TEST mode. If VSWR is still high, check the antenna, ground, and connectors.



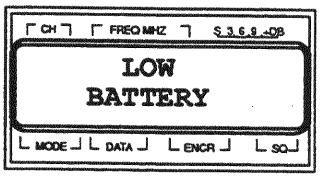
Situation: Front panel cannot communicate with main controller assembly.

Action: Turn power off and on. If condition still exists, check A1 Interface, A4 Signal Processor, or A10 Front Panel Assembly.



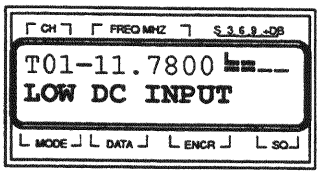
Situation: Battery or primary supply voltage low. The radio is still operational, but the front panel display will change to REPLACE BATTERY if no action is taken.

Action: Replace batteries or check primary power supply for voltage and proper operation.



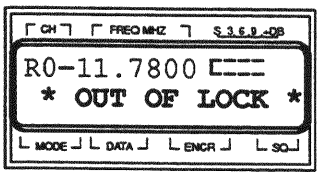
Situation: External power amplifier warning indicating low primary supply voltage.

Action: Check the primary supply voltage and supply cable.

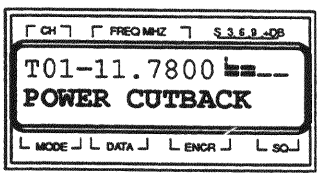


Situation: The synthesizer is out of lock (transceiver is not operational).

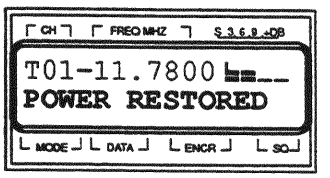
Action: Perform self test.



Situation: This indicates a high-temperature condition in the power amplifier assembly during transmitter operation. Maximum transmit power is limited to 5 watts.

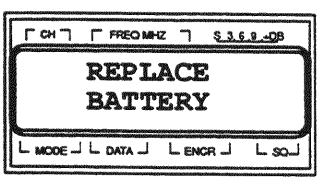


Action: None necessary. Full power will be restored if the power amplifier is allowed to cool.



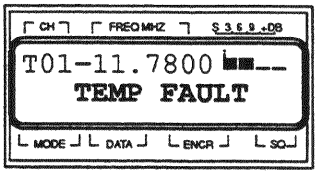
Situation: Battery or primary supply voltage is too low for proper operation.

Action: Replace batteries or check primary power supply for voltage and proper operation.



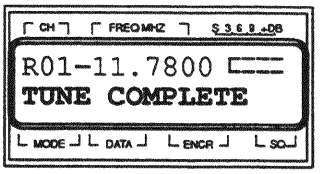
Situation: This indicates an over-temperature condition in the power amplifier assembly during transmitter operation. The transmitter will automatically unkey to prevent damage to the power amplifier.

Action: Allow amplifier to cool. Check ambient air temperature and ventilation in the area. Transmit capability will be restored when the over-temperature condition no longer exists.



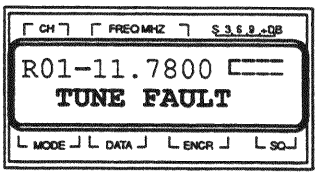
Situation: Antenna coupler tuning has been completed.

Action: None necessary.



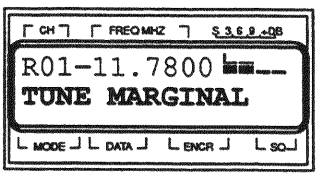
Situation: Antenna coupler tune fault. Antenna coupler is unable to tune the antenna at the operating frequency.

Action: Retune by selecting RETUNE from the OPTION menu and pressing the ENTER key. Measure VSWR in TEST mode. If VSWR is still high, check the antenna, ground, and connectors.



Situation: Most likely due to dynamic antenna conditions, the antenna has tuned to a VSWR of $\geq$ 2.0:1, but $\leq$ 3.0:1 communication is still possible.

Action: Retune by selecting RETUNE from the OPTION menu and pressing the ENTER key. Measure VSWR in TEST mode. If VSWR is still high, check the antenna, ground, and connectors.



1.6 PREVENTIVE MAINTENANCE

Preventive maintenance is the systematic care and inspection of equipment to prevent equipment failure. During any maintenance check, take note of any unusual equipment conditions that may indicate degrading or degraded performance and make any necessary corrections.

For reliable operation, prevent dirt build-up anywhere in the system. Keep electrical contacts clean and free from corrosion. To clean contacts, use a soft cloth or cotton dipped in alcohol. Use the protective covers provided for the front panel connectors when they are not in use.

Table 1-10 contains the checks and services that should be performed either on a daily basis when the equipment is in use or on a weekly basis when the equipment is in a standby condition. Table 1-11 contains the checks and services that should be performed on a weekly basis.

Table 1-10. Daily Preventive Maintenance Checks and Services

Check No.	Item to be Inspected	Procedure
1	Completeness	Check to see that the equipment is complete.
2	Exterior Surfaces	Remove dust, dirt, and moisture from all surfaces and clean front panel display window with a soft cloth.
3	Controls	Check all controls for looseness or damage; check mechanical action of each control for smooth operation.
4	Batteries	Inspect batteries for leakage or corrosion.
5	Operation	Perform self test.

Table 1-11. Weekly Preventive Maintenance Checks and Services

Check No.	Item to be Inspected	Procedure
1	Battery Condition	Remove battery case from R/T and check batteries for corrosion or leakage. Clean or replace, as required. Never store batteries in the battery case for over 30 days.
2	Connectors	Check all connectors for debris, damage, or corrosion. Elevate to a higher level of maintenance, if required.
3	Antenna	Check for breaks or strains – repair or replace, as required.
4	Memory Backup Battery	Replace every three to five years.

1.7 BATTERY INFORMATION

The manpack transceiver is supplied with a Battery Case (10372-1300) which holds two nickel-cadmium (rechargeable) or two lithium-sulfur dioxide (disposable) batteries. The batteries provide +24 Vdc (nominal) to the manpack transceiver.

1.7.1 Battery Voltage

The manpack transceiver continuously monitors battery voltage for acceptable levels. It displays the voltage during battery self test.

The BB-590/U Nickel-Cadmium (Ni-Cd) Battery (10075-1345-01) is rated for use at temperatures between –20° C and +70° C. These batteries are more effective at moderate to cooler temperatures; excessive heat or cold temperatures reduce battery life and degrade battery performance.

The BA-5590/U Lithium-Sulfur Dioxide (Li-SO_2) Battery is a high-energy battery with a longer operational life than the Ni-Cd battery. The Li-SO_2 battery performs effectively at temperatures between –20° C and +70° C, but voltage drops rapidly in high-power situations and during temperature extremes.

During self test, battery voltage and charge levels display on the front panel display. If the battery voltage is below +24.0V or if LOW BATTERY or REPLACE BATTERY appears on the front panel display, replace the batteries in the battery case.

1.7.2 Installing the Batteries in the Battery Case

Optimal performance requires using two Ni-Cd or two Li-SO_2 batteries in the battery case, but the manpack will operate from either a single BB-590/U Nickel-Cadmium or BA-5590/U Lithium-Sulfur Dioxide battery. (Operation from a single BA-5590/U Lithium-Sulfur Dioxide battery results in reduced power output.)

The batteries slide into the top section of the case and rest on the rubber pad on the bottom of the case. The connectors are in the outside corners.

WARNING

Never ship the battery case with batteries in it. Never store batteries in the battery case for over 30 days.

1.7.3 Charging Nickel-Cadmium Batteries

The Solar Battery Charger (10372-0950-01) is a lightweight photovoltaic power supply designed to recharge the BB-590/U Nickel-Cadmium batteries.

The solar panel is a notebook-style unit that weighs 1.7 lbs. Polycrystalline cells are laminated with Teflon into a sturdy heat-treated aluminum case tested to MIL-STD-810D.

When the connector, provided as part of the panel, is attached to the connector on the BB-590/U Nickel Cadmium battery, the battery is recharged in approximately 4 to 12 hours (depending on weather conditions and the condition of the battery).

WARNING

Do not use the Solar Battery Charger (or any other device) to charge lithium-sodium dioxide batteries.

1.7.4 Storing, Handling, and Disposing of Lithium-Sulfur Dioxide (Li-SO_2) Batteries

1.7.4.1 Storing Lithium-Sulfur Dioxide ($LiSO_2$) Batteries

Store the lithium-sulfur dioxide battery in its original shipping container. Recommended storage is in a cool, sprinkler protected, ventilated area where the temperature is maintained below 160° F (70° C).

WARNING

DO NOT store lithium-sulfur dioxide batteries with other hazardous materials.

1.7.4.2 Handling $LiSO_2$ Batteries

Many safety features are built into the lithium-sulfur dioxide battery to ensure stability under combat conditions; however, anyone who handles Li-SO_2 should observe the following warning.

WARNING

Do not charge, short circuit, incinerate, disassemble, or mutilate the BA-5590/U Lithium-Sulfur Dioxide Battery. Do not expose to fire or temperatures above 160° F (70° C); otherwise battery may rupture, releasing toxic material.

WARNING

Do not use any BA-5590/U Lithium-Sulfur Dioxide Battery built before 1980.

If a $LiSO_2$ battery accidentally ruptures, ventilate the area well and wash away any spilled residue with water.

WARNING

Do not use a Halon-type fire extinguisher on a lithium-sulfur dioxide battery fire. In the event of a fire near a $LiSO_2$ battery, rapid cooling is important. Use a carbon dioxide (CO_2) extinguisher. Control of the equipment fire and cooling may prevent the battery from venting and potentially exposing lithium metal. In the event that lithium metal becomes involved in the fire, the use of a graphite-based, Class-D fire extinguisher is recommended.

NOTE

Be sure to follow all of the battery manufacturer's safety precautions.

1.7.4.3 Disposing of Lithium-Sulfur Dioxide Batteries

CAUTION

DO NOT dispose of lithium-sulfur dioxide batteries with ordinary trash/refuse.

WARNING

A partially discharged lithium-sulfur dioxide battery is considered to be hazardous waste.

Completely discharged batteries are not considered hazardous or reactive. The BA-5590/U Lithium-Sulfur Dioxide Battery includes an internal discharge switch. To discharge the battery, activate this switch per the battery manufacturer's instructions.

WARNING

Keep lithium-sulfur dioxide batteries away from open flame or heat.

1.7.5 Replacing the Memory Lithium Backup Battery

There is a memory lithium battery in the RT-1694 on the A1A1 Interface Assembly that holds the memory for all the microprocessors in the radio. The projected life for this lithium battery is five years, but it should be replaced as required.

If the RT-1694 fails to retain programmed channel frequency, hopset data, encryption key data, or operating mode parameters, or if battery voltage falls below 2.5 volts (normal battery voltage is 3.5 volts), replace the memory lithium battery. The reference designator for the A1A1 back-up battery is BT1.

Perform the following procedure for replacing the back-up battery:

a. Follow the precautions outlined in subsection 1.4.4, General Maintenance Procedures.

WARNING

NEVER short across the plus (+) and minus (–) terminals of a lithium battery. The potential for explosion is present. Injury to personnel and equipment can occur.

b. Locate the battery on the A1A1 component location diagram.

c. Carefully desolder the battery from the PWB assembly. Ensure that the soldering station is temperature controlled and set to approximately 600° F (333° C).

d. Replace the lithium battery (part number B41-0013-002).

e. Solder new battery in place.

NOTE

The Material Safety Data Sheet (MSDS) for the memory lithium battery is found in the Appendix of this manual.

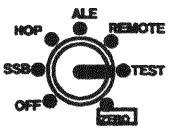
1.8 SELF TEST

Primary troubleshooting relies heavily on self test for isolating a faulted assembly. Using this procedure, the operator can quickly identify the faulty assembly, replace the assembly, and return the system to service.

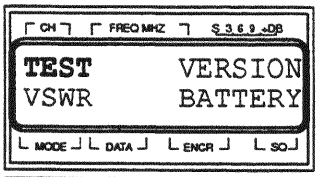
The self-test routine, initiated at the radio's front panel, performs numerous checks on the operational status of the manpack. The system self test is performed without on-the-air transmission.

The following self tests appear in the test selection menu:

- Single Self Test
- Version Report
- VSWR Measurement
- Battery Status

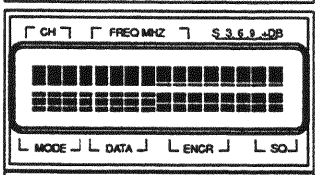


Single Self Test



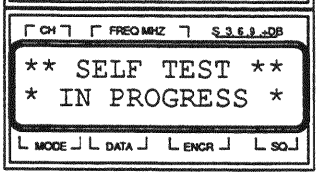
◄ ► Initiates a Single Self Test ENTER

Display Test. Check to make sure all blocks are shown in full (performed at start of self test).

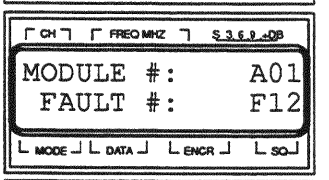


Four displays can appear during a Single Self Test.

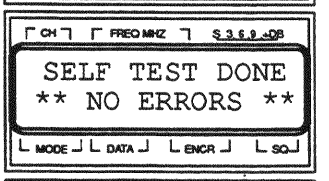
While test is running:



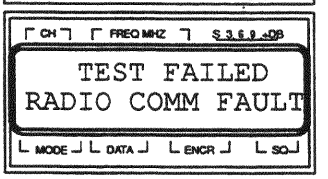
When a fault is found:



When test is completed with no faults:



When front panel cannot communicate with radio:



CLEAR or ENTER After completion of test, returns to the main test selection menu

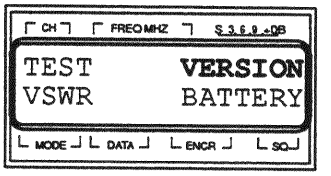
If a fault condition occurs, its source is shown on the display as a fault code. Table 1-4 lists the assembly identified by each fault code. Table 1-12 lists the fault codes.

NOTE

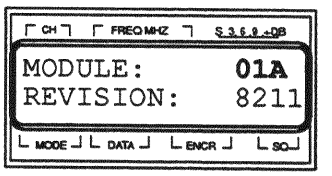
If the FUNCTION or CHANNEL control is changed during a self test, a fault condition may be displayed (because the test routine was not allowed to sequence through all of the tests). A test sequence should be allowed to finish before any new control, keyboard, or remote control command is issued.

Version

This routine allows the user to examine the firmware revision level of each assembly within the system.



◄ ► Initiates Version Report ENTER

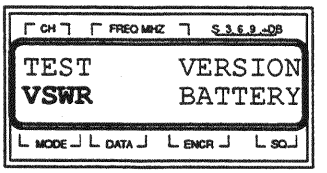


▼ ▲ Selects which assembly is being shown

CLEAR or ENTER Returns to the main test selection menu

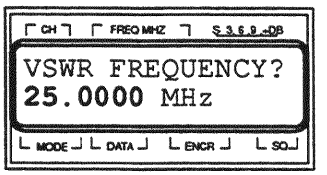
Voltage Standing Wave Ratio (VSWR)

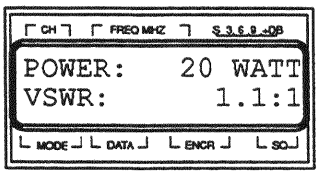
The VSWR measurement shows the amount of reflected power at the output of the power amplifier. It also displays the power (watts) being transmitted. The default frequency is the frequency of the currently selected SSB channel.



◄ ► Select VSWR; initiate VSWR test ENTER

▼ ▲ Selects frequencies programmed into other SSB channels (or use the alphanumeric keypad to choose any other frequency) ENTER

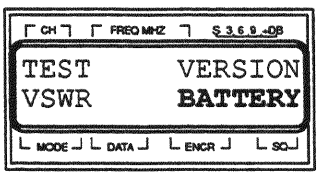




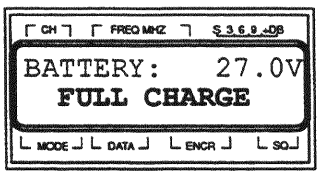
CLEAR or ENTER Returns to the main test selection menu

Battery

The BATTERY status shows battery voltage and charge levels. The selections are FULL, MEDIUM, LOW, and REPLACE and vary from 32.0 volts to 20.0 volts.



◄ ► Select BATTERY ENTER



ENTER Returns to the main test selection menu

Table 1-12. Fault Code Listing

Assembly No.	Fault Code No.	Description
A1A1 INTERFACE/ENCRYPTION ASSEMBLY		
A1A1	01	Communications fault
	02	Non-destructive internal RAM fault
	03	ROM checksum fault
	04	Non-destructive external RAM fault
	05	Asynchronous data channel fault
	06	Synchronous data channel fault
	09	Remote data channel fault
	10	PA DUART internal counter fault
	11	External PA communications channel fault
	0F[2]	Frame Clock not detected
	0A[1]	Dual Port RAM semaphore register fault
	0B[1]	Dual Port RAM fault
	51	Real time clock not installed or not working
	52	Internal real time clock RAM fault
	55	Real time clock rollover registers not operational
	56	RTC crystal oscillator failed
	81[1]	No communication with encryption board
A1A2 ENCRYPTION ASSEMBLY		
A1A2	81	No communication with interface board
	82	ROM checksum fault
	83	Non-destructive internal RAM fault
	84	Non-destructive external RAM fault
	85	Dual Port RAM fault
	86	Dual Port RAM semaphore register fault
	87	Decryption (ACE) chip fault
	88	HSS internal register fault
	89	Encryption/Decryption loop back fault

Notes: [1]Fault could either be on the Interface or Encryption Assembly
[2]Fault could be on any assembly containing the FRAME CLOCK or the motherboard

Table 1-12. Fault Code Listing (Cont.)

Assembly No.	Fault Code No.	Description
		A3 LPC ASSEMBLY
A03	01	8751 communications fault
	02	8751 ROM fault
	03	8751 microprocessor internal RAM fault
	05	8751 dual port RAM fault
	06	8751 dual port RAM busy fault
	07	8751 dual port RAM interrupt fault
	14	Hop clock fault
	15	Frame clock fault
	81	TMS320 internal RAM fault
	82	TMS320 external program RAM fault
	83	TMS320 external data RAM fault
	84	TMS320 ROM fault
	85	TMS320 dual port RAM fault
	86	Sample clock fault
	87	TMS320 AIC fault
	88	TMS320 DAC fault
	F5	8751 not finished fault
	FA	TMS320 not finished fault
		A4 SIGNAL PROCESSOR ASSEMBLY **Main Controller**
A4	41	No communications
	42	Non-destructive internal RAM fault
	43	ROM checksum fault
	44	Non-destructive external RAM fault
		AGC
	61	Communication fault
	62	Internal RAM fault
	63	ROM checksum fault
	64	External RAM fault
	67	Digital IF handshake fault (Dual Port RAM)
	6B	Digital IF not finished with BITE
	6C	Anti-Alias filter fault
	6D	28.8 kHz Sampler clock fault
	6E	24.0 kHz Sampler clock fault

Table 1-12. Fault Code Listing (Cont.)

Assembly No.	Fault Code No.	Description
A4 (Cont.)	74	Frame clock not detected
	75[3]	Hop Clock not detected
A4 SIGNAL PROCESSOR ASSEMBLY (Cont.) Digital IF		
	80	ROM checksum fault
	81	Internal RAM fault
	82	External RAM fault
	83	Dual port RAM to AGC fault
	84	Dual port RAM to FFT fault
Modem Processors: DIF = Digital IF TMS320 MDM = 80C186 FFT = Modem TMS320 FEC = Modem 80C51		
	01	Communication fault
	14[3]	Hop Clock error
	15[2]	Frame Clock error
	1F	FEC ROM checksum fault
	20	FEC External RAM fault
	21	FEC dual port RAM fault
	22	MDM not running
	23	FFT handshake fault
	24	FFT to MDM dual port RAM fault
	25	MDM to FFT dual port RAM fault
	26	MDM to FEC dual port RAM fault
	27	MDM ROM checksum fault
	28	MDM RAM fault
	29	Sample Clock error
	2A	FFT ROM checksum fault
	2B	FFT internal RAM fault
	2C	FFT external RAM fault
	2D	FFT to DIF dual port RAM fault
	2E[3]	Hop Clock error
	2F	FFT self test not complete
	30	FFT self test not complete
	31	Reserved
	32	Time Sample transfer

Notes: [2]Fault could be on any assembly containing the FRAME CLOCK or the motherboard
[3]Fault could be on any assembly containing the HOP CLOCK or the motherboard

Table 1-12. Fault Code Listing (Cont.)

Assembly No.	Fault Code No.	Description
A4 (Cont.)	33	MDM self test not complete
	34	FEC self test not complete
A5 RECEIVER/EXCITER ASSEMBLY		
A5	01	Receiver in-band analog attenuation too low
	02	Receiver in-band digital attenuation too low
	03	Receiver out-of-band analog attenuation too high
	04	Receiver out-of-band digital attenuation too high
	0F	Exciter Gain too low
	10	Exciter Gain too high
	11	Exciter Output too low
	12	Exciter Output too high
A6 SYNTHESIZER/REFERENCE ASSEMBLY		
A6	12	Combined lock detect fault
	20	Serial EEPROM data read fault
A8 POWER AMPLIFIER/HARMONIC FILTER ASSEMBLY		
	Harmonic filter bands are bit mapped as an 8 bit binary fault code. Each bit of the binary word represents a harmonic filter band, with the least significant bit representing Band 1. The most significant bit represents the 60 MHz lowpass roofing filter called Band 8. If any of the filter bands are found to be not operational, the corresponding bit of the fault code will be set to 1. A bit set to 0 represents a properly functioning filter band. For reporting purposes, the numerical value of the binary fault code is converted to hexidecimal. For example, if the result of BITE is "A08 F06," then bands 2 and 3 of the harmonic filter are not operating properly. 06 hexidecimal is equal to a binary fault code of 0000 0110, which indicates faulty bands 2 and 3. In order for this test to pass, all other assemblies must be operational. If BITE returns "A08 FFF,"meaning that all bands have failed, check all cables to assure that power and the RF signals are getting to the Power Amplifier/Harmonic Filter Assembly.	
A9 COUPLER ASSEMBLY		
A9	01	Coupler – PA Path broken
A10 FRONT PANEL		
A10	02	Non-destructive internal RAM fault
	03	ROM checksum fault
	04	Non-destructive external RAM fault
	05	The display driver's busy flag is not functional

1.9 ASSEMBLY ACCESS

The radio chassis contains assemblies A1 and A3 through A11. The assemblies are designed so no adjustments or alignments are necessary after replacement. Access to these assemblies is gained by removing the outer case and, in most cases, the shielded cover. The location of the plug-in assemblies is shown in figure 1-2. The assemblies are designed to be installed in only one direction.

1.9.1 Module Removal Procedure

Perform the following procedure to replace a faulted assembly identified by self test. Figure 1-2 shows the location of all radio assemblies.

a. Remove power from the radio by turning the FUNCTION control to the OFF position and disconnecting the battery case from the radio.

b. Detach the handset, antenna, and any other cables from the radio.

c. Loosen the four front panel hex screws (captive) securing the case of the radio.

d. Remove the outer case.

NOTE

The A8 and A9 assemblies are now exposed and either of them can be removed without further disassembly of the radio.

e. The A8 Power Amplifier/Harmonic Filter Assembly (10372-1400-01) is located at the back of the chassis.

1. Disconnect the ribbon cable and carefully remove the RF connector with needle-nose pliers (both cable and connector are found on the bottom of the chassis).
2. Loosen the four captive screws in the corners of the A8A1 Power Amplifier Assembly and remove the RF cable from the A8A2 Assembly before lifting it all the way out.
3. To remove the Harmonic Filter Assembly, A8A2, loosen the four captive screws that attach it to the A8A1 Assembly, and remove.

f. The A9 Antenna Coupler Assembly (10372-1450-01) is located on the right hand side of the chassis.

1. Remove the brass screw that connects the RF connector to the A9 Coupler Assembly.
2. Disconnect the ribbon cable and carefully remove the RF connector with needle-nose pliers (both cable and connector are found on the bottom of the chassis).
3. To remove the A9 Coupler Assembly, loosen the four captive screws that attach the A9 to the chassis and remove.
4. To separate the A9A1 from the A9A2, remove the brass screw on the A9A1 Coupler Input Assembly and pull apart.

NOTE

To access all other assemblies, the shielded top cover has to be removed by loosening the eight captive screws.

g. Remove faulty assemblies as follows:

1. A1 Assembly – use needle-nose pliers to carefully lift out the assembly by its green cord. To separate the A1A1 from the A1A2, remove the four screws on the A1A1 Interface Assembly and pull apart.
2. A3 Assembly – use needle-nose pliers to carefully lift out the assembly by its green cord.

3. A4 Assembly – use needle-nose pliers to carefully lift out the assembly by its green cord.
4. A5 Assembly – disconnect cables and use needle-nose pliers to carefully lift out the assembly by its green cord.
5. A6 Assembly – disconnect cable and use needle-nose pliers to carefully lift out the assembly by its green cord.
6. A7 Assembly – This is located in the left-hand, rear corner of the chassis. To remove this assembly, loosen the three screws on the bottom of the case and lift up from the top.
7. A10 Assembly – loosen the four captive hex screws attaching the front panel to the outer case.
   (a.) Remove the outer case.
   (b.) Remove the two ribbon cables and the RF connector to the A9 Antenna Coupler Assembly.
   (c.) Remove the two counter sunk screws on each side of the Assembly and lift off.

h. The A11 Motherboard (Interconnect) Assembly is removed after all the other assemblies are removed. Four screws hold the motherboard to the chassis. Once they are removed, the motherboard lifts out.

1.9.2 Assembly Installation Procedure

Perform the following procedure to install the replacement assembly:

a. To install an assembly, firmly press the assembly into its chassis slot. DO NOT FORCE. The correct assembly slides easily into place.

b. For assemblies A7, A8, A9, A10, and the A11 motherboard, replace screws.

c. Carefully re-attach any assembly cables.

d. Replace the shielded cover and carefully tighten all eight screws.

e. Replace the case of the radio, and fasten the four front panel hex screws (captive).

f. Re-attach the handset, antenna, and any other necessary cables to the receiver-transmitter.

g. Re-attach power to the radio by connecting the battery case. Turn the FUNCTION control to the SSB position.

1.10 GENERAL TROUBLESHOOTING TECHNIQUES

Before proceeding to any specific bite fault troubleshooting procedure, perform the following general steps.

NOTE

Do not run self test in FM mode.

a. Zeroize the radio and reprogram the settings.

CAUTION

To avoid damage to the radio, always remove power from the radio before replacing an assembly by disconnecting and removing the battery case and (or) any external power.

b. Replace the assembly identified by the self test fault code with a known good assembly, reconnect power, and rerun self test. If self test still identifies the fault code error, the problem may not be the fault identified in the self test. If self test does not return the fault code error, remove the known good assembly and replace it with the suspected assembly. Rerun self test and verify that the fault code error is produced.

NOTE

If no error occurred on the second self test, the assembly may have simply been seated incorrectly on the motherboard. If the error cannot be reproduced, rerun self test several times to verify that the assembly no longer produces an error.

c. Proceed to the bite faults and troubleshooting procedures found in the individual assembly sections of this manual.

1.11 CHECKING RECEIVER SENSITIVITY

Perform the following procedure to test the sensitivity of the RT-1694:

a. Set up the RT-1694 as shown in figure 1-3.

CAUTION

The transceiver should never be keyed when a signal generator is connected to the Antenna (RF) connector. Serious damage can result.

b. Set the transceiver to the following settings:

Function Switch:	SSB
Mode:	USB
Digital Voice:	OFF
Modem:	OFF
Squelch:	OFF
Encryption:	OFF
RX Frequency:	1.6000 MHz
TX Frequency:	1.6000 MHz
RF GAIN:	100%
AGC:	MED
IF BW:	2.7 kHz

c. With the signal generator set to 1.6010 MHz, the measured SINAD (signal + noise + distortion/noise + distortion) should be greater than 10 dB.

d. Repeat this measurement with the following frequency settings:

Signal Generator	**Transceiver**
15.001 MHz	15.0000 MHz
29.001 MHz	29.0000 MHz
30.101 MHz	30.1000 MHz
46.601 MHz	46.6000 MHz
59.701 MHz	59.7000 MHz

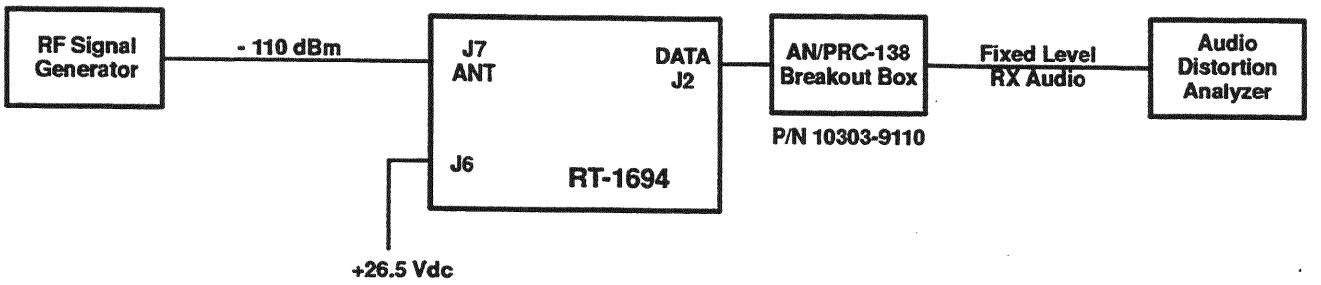


Figure 1-3. Receiver Sensitivity Test Set Up

1.12 POWER OUTPUT MEASUREMENT

Perform the following test to measure the power output of the RT-1694:

a. Set up the RT-1694 as shown in figure 1-4.

b. Set the transceiver to the following settings:

Function Switch:	SSB
Mode:	CW
Digital Voice:	OFF
Internal Coupler:	BYPASS
Receiver Preamplifier:	BYPASS
Modem:	OFF
Squelch:	OFF
Encryption:	OFF
RX Frequency:	1.6000 MHz
TX Frequency:	1.6000 MHz
RF GAIN:	100%
AGC:	FAST
IF BW:	0.35 kHz

c. Using the handset, key the transceiver and verify that the output level is:

TX POWER:	HIGH	32.0 V (28-40 V) +43 dBm (+2/–1) 20 W (16-32 W)
TX POWER:	MED	16.0 V (14.1-20 V) +37 dBm (+2/–1) 5 W (4-8 W)
TX POWER:	LOW	7.1 V (6.4-9 V) +30 dBm (+2/–1) 1 W (0.8-1.6 W)
EXCITER MODE (WITH EXT. PA FEEDBACK)		:2.25 V (2.0-2.8 V) +20 dBm (+2/–1) 100 mW (80-160 mW)

EXCITER MODE (OPEN-LOOP CW) :3.2 V (2.8-3.55 V)
+23 dBm (+1/–1)
200 mW (160-250 mW)

d. Repeat this measurement with the transceiver set to the following transmit frequencies:

15.0000 MHz
29.0000 MHz
31.1000 MHz
46.6000 MHz
59.7 MHz

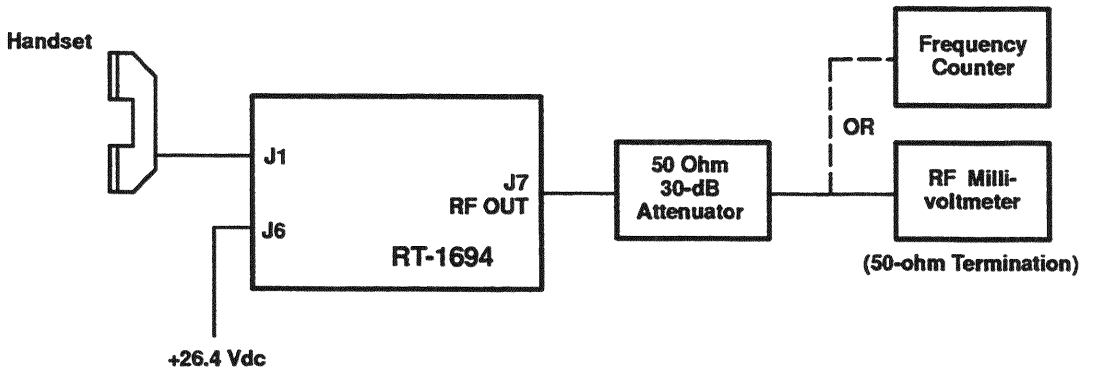


Figure 1-4. Power Output Measurement Test Set Up

1.13 TRANSMIT FREQUENCY MEASUREMENT

Perform the following test to measure the RT-1694 transmit frequency:

a. Set up the RT-1694 as shown in figure 1-4.

b. Set the transceiver to the following settings:

Mode:	CW
Digital Voice:	OFF
Internal Coupler:	BYPASS
Modem:	OFF
Squelch:	OFF
Encryption:	OFF
RX Frequency:	59.999 MHz
TX Frequency:	59.999 MHz
TX Power;	HIGH
RF GAIN:	100%
AGC:	FAST
IF BW:	1.0 kHz

c. The output frequency should be 59.999 MHz, ±60 Hz, as noted on the frequency counter.

1.14 PARTS LIST, INTERCONNECT AND BLOCK DIAGRAMS

Table 1-13 is the RT-1694 main chassis parts list. Figure 1-5 is the system interconnect diagram.

Table 1-13. RT-1694 Main Chassis Parts List (10372-1000-01 Rev. S)

Ref. Desig.	Part Number	Description
	DWG-10372-8900	FIRMWARE, SYSTEM CONFIGUR
1	10372-1005-01	CHASSIS
2	10372-1014-01	RADIO CASE & GASKET ASSY
3	10372-1010-01	COVER ASSY, PWB COMPT
4	10372-1028-01	INSULATOR
5	10372-1029-01	INSULATOR
6	10372-1030-01	SUPPORT, PWB
7	10372-1031-01	SUPPORT, PWB
9	10372-1033-01	SUPPORT, PWB
10	10372-1043-01	INSULATOR
11	10372-1043-02	INSULATOR
13	10372-1043-04	INSULATOR
14	MS24693-C24	FHS SS 6-32X1/4 100DE
15	MS24693-C17	FHS SS 2-56X5/32 100DE
16	H50-1006-404	SPCR 3/16HEX SS 4-40X.250
17	MS51957-3	PHS SS 2-56X1/4
19	MS35338-134	LW SPLT SS #2
20	MS15795-803	FW SS .125X.250X.022
21	10372-1077-01	ID/SERIAL # LABEL PLATE
22	MS51957-2B	PHS BL SS 2-56X3/16
23	10372-1206-01	O-RING, CONDUCTIVE
26	10372-1061-01	PAD, RUBBER
27	10372-1064-01	INSULATOR
29	10303-2280	PWB ASSY, INTERFACE
30	10372-1209-01	SPRING FINGER STRIP
31	P15-3145-001	SEALER RTV 3145 CLEAR
32	10303-3024	WASHER, FLAT #2 SM
33	MS93076-12R	DUST CAP
34	10303-1206-01	INSULATOR, PWB
A1A1	10303-2280	PWB ASSEMBLY, INTERFACE
A1A2*	10303-2240	PWB ASSEMBLY, ENCRYPTION
A3**	10372-3440-01	PWB ASSEMBLY, LPC/FILL
A4	10303-2500	PWB ASSY,SIGNAL PRCSR
A5	10303-2600	RCVR/EXCITER

NOTES:

* RF-5170 OPTION

**RF-5161-01 OPTION

Table 1-13. RT-1694 Main Chassis Parts List (10372-1000-01 Rev. S) (Cont.)

Ref. Desig.	Part Number	Description
A6	10303-2700	SYNTHESIZER ASSY
A7	10303-2200	POWER SUPPLY ASSY
A8	10372-1400-01	PWR AMP/BATT CHG ASSY
A9	10372-1450-01	ANTENNA CPLR ASSY
A10	10372-1500-01	FRONT PANEL ASSY
A11	10303-2170	MOTHER BOARD
W1	10372-1037-01	CABLE ASSY, RF (PA-CPLR)
W2	10372-1053-01	CABLE ASSY, RF (PA-R/E)

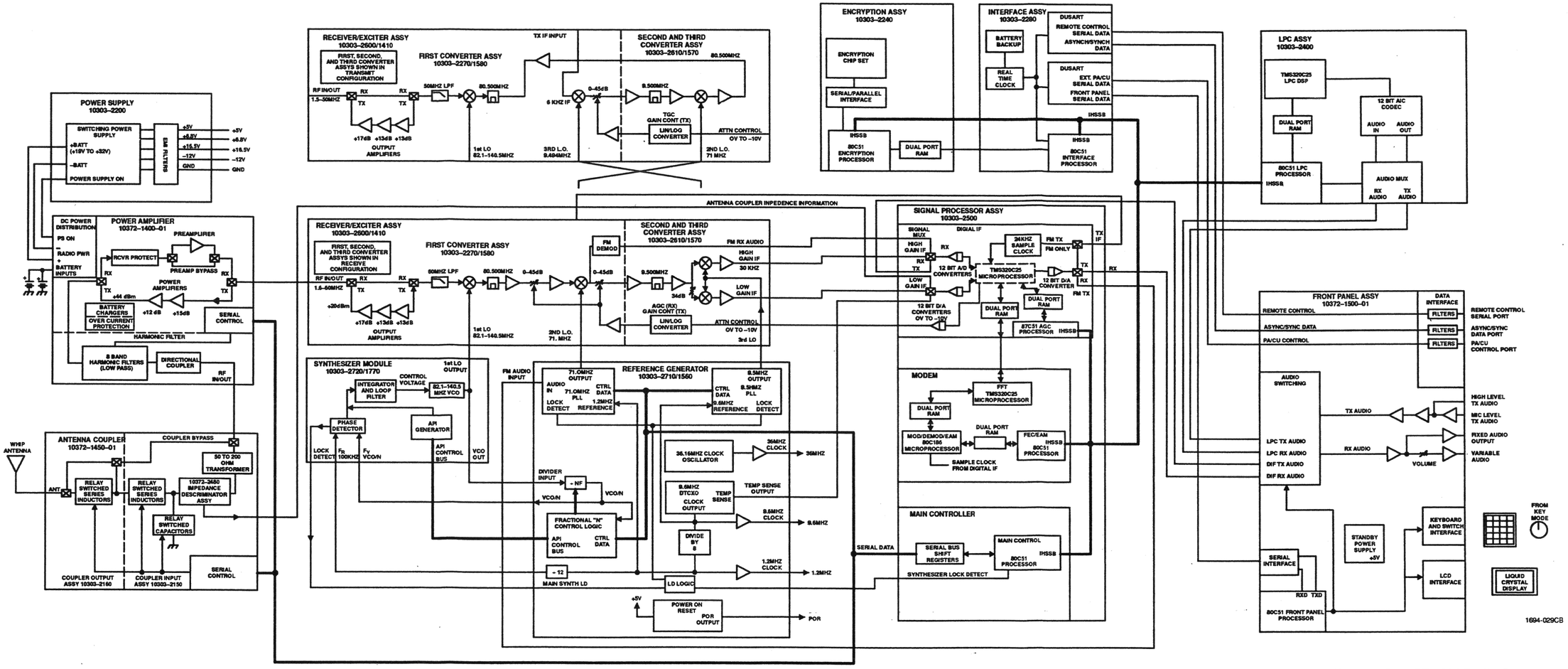
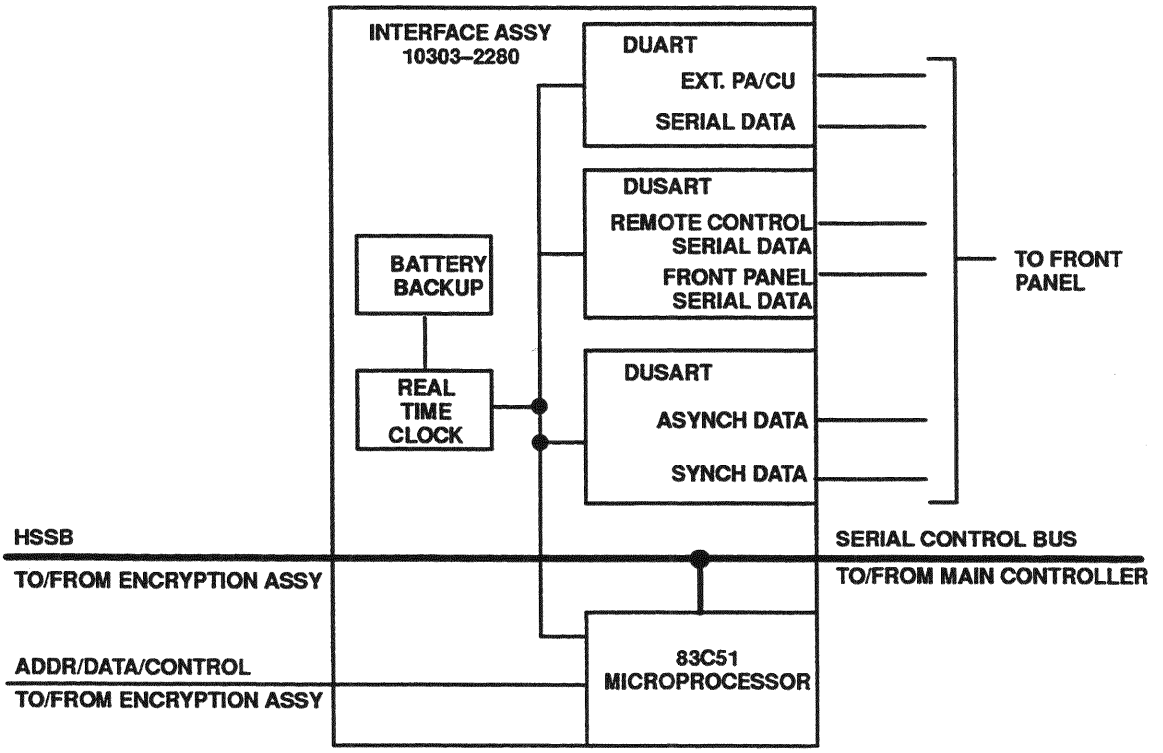


Figure 1-5. RT-1694 Radio System Interconnect Diagram (10372-1001)

A1A1
INTERFACE



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A1A1 INTERFACE

1. GENERAL DESCRIPTION

The A1A1 Interface Assembly (10303-2280) provides the data interface between the RT-1694(P)/PRC-138 and various types of external devices.

For devices requiring a data interface, the A1A1 Assembly provides two RS-232 ports and the external, RF-device port. One of the RS-232 ports, the remote port, is always configured for asynchronous communications. The remote port is primarily used to remotely control the R/T, although asynchronous data from this port can be sent over the air. The other RS-232 port, the data port, is software configurable for either synchronous or asynchronous communications. The data port cannot be used to remotely control the radio. It can only be used to send or receive modem data. The external, RF-device port can only be used to control external PAs, couplers, and pre-postselectors.

The A1A1 Interface Assembly consists of the A1A1 10303-2280 printed wiring board. If the A1A2 RF-5170 Data Encryption Assembly (10303-2240) is installed, it is connected to the Interface Assembly via connector J2. For information on the A1A2 RF-5170 Data Encryption Option, refer to its tab section in this manual.

2. INTERFACE CONNECTIONS

The signals sent to and received by the A1A1 Interface Assembly are listed in tables 1 and 2. Figure 1 is the A1A1 Interface Assembly interconnect diagram.

Table 1. Interface Control Assembly – Encryption/Interface Assembly Connections

Connector and Pin	Signal	Comments
J2-1	+5 V	5-volt logic supply to board
J2-2	+5 V	5-volt logic supply to board
J2-3	/IWR	Interface write strobe, active low
J2-4	Internal HSSB	300 kbaud communications bus
J2-5	IA8	Interface address line 8
J2-6	/IRD	Interface read strobe, active low
J2-7	IA10	Interface address line 10
J2-8	IA9	Interface address line 9
J2-9	Spare	N/C
J2-10	IA11	Interface address line 11
J2-11	Spare	N/C
J2-12	ENCFRCLK	Frame clock (not used)
J2-13	ID7	Interface data bit 7
J2-14	IA7	Interface address line 7
J2-15	ID6	Interface data bit 6
J2-16	IA6	Interface address line 6
J2-17	ID5	Interface data bit 5

Table 1. Interface Control Assembly – Encryption/Interface Assembly Connections (Cont.)

Connector and Pin	Signal	Comments
J2-18	IA5	Interface address line 5
J2-19	ID4	Interface data bit 4
J2-20	IA4	Interface address line 4
J2-21	ID3	Interface data bit 3
J2-22	IA3	Interface address line 3
J2-23	ID2	Interface data bit 2
J2-24	IA2	Interface address line 2
J2-25	ID1	Interface data bit 1
J2-26	IA1	Interface address line 1
J2-27	ID0	Interface data bit 0
J2-28	IA0	Interface address line 0
J2-29	TSTRES_ENC	Test line to hold encryption in reset, active high
J2-30	DP_INT	Message interrupt to encryption
J2-31	AUX2	Auxiliary control strobe 2
J2-32	AUX3	Auxiliary control strobe 3
J2-33	9.6 MHz	9.6-MHz system clock
J2-34	/PGM	Disables Peripheral I/O Select, active low
J2-35	+16 V UNREG	Unused
J2-36	VPP	Flash Programming Voltage (12.5V maximum)
J2-37	VBATT	Unused
J2-38	Reset	System reset, active high
J2-39	GND	System GROUND
J2-40	GND	System GROUND

Table 2. Interface Control Assembly – Motherboard Assembly Connections

Connector and Pin	Signal	Comments
J1-1	9.6 MHz clock	+5/0 V, CMOS square wave
J1-2	3.9 V BATTERY BACKUP	+2.8 - +3.9 V
J1-3	Digital GND	Motherboard GROUND
J1-4	Digital GND	Motherboard GROUND
J1-5	+16 V	+16.5V +/- 10%, unreg
J1-6	+16 V	+16.5V +/- 10%, unreg
J1-7	-12 V	-12.0V +/- 5%, reg
J1-8	-12 V	-12.0V +/- 5%, reg
J1-9	+5 V	+5.0V +/- 2%, reg
J1-10	+5 V	+5.0V +/- 2%, reg
J1-11	PA Control Data –	0/+5 V, async 12.5-150 kbaud
J1-12	PA Control Data +	+5/0 V, async 12.5-150 kbaud
J1-13	TX Data IN	RS-232/MIL-188, async/sync
J1-14	Spare	N/C
J1-15	Spare	N/C
J1-16	RX Data OUT	RS-232/MIL-188, async/sync
J1-17	Data to FP	+5/0 V, async, 9600 baud
J1-18	RTC Interrupt	+VBATT/0 V, active high
J1-19	Spare	N/C
J1-20	Spare	N/C
J1-21	TX Remote Data IN	RS-232/MIL-188, async up to 9600 baud
J1-22	Sync Clock OUT	RS-232/MIL-188
J1-23	Spare	N/C
J1-24	Frame Clock	+5/0 V, 22.5ms period
J1-25	RTS Data	RS-232/MIL-188
J1-26	/PA Power ON	+5/0 V, active low
J1-27	Spare	N/C
J1-28	CTS Data	RS-232/MIL-188
J1-29	Sync Clock IN	RS-232/MIL-188
J1-30	Spare	N/C
J1-31	Spare	N/C

Table 2. Interface Control Assembly – Motherboard Assembly Connections (Cont.)

Connector and Pin	Signal	Comments
J1-32	RLSD	RS-232/MIL-188
J1-33	/RESET	+5/0 V, active low
J1-34	Spare	N/C
J1-35	Spare	N/C
J1-36	MFO from RTC	+5/0 V, 32.768 kHz
J1-37	HSSB	+5/0 V, 300 kbaud
J1-38	Spare	N/C
J1-39	TSTRES_INT	Test line to hold interface in RESET, active high
J1-40	RX Remote	RS-232/MIL-188, async up to 9600 baud
J1-41	/PGM	+5/0 V, active low
J1-42	Spare	N/C
J1-43	1.2 MHz	+5/0 V, CMOS square wave
J1-44	Data from FP	+5/0 V, async, 9600 baud
J1-45	VPP	+12V +/- 5%
J1-46	Spare	N/C
J1-47	Spare	N/C
J1-48	Spare	N/C
J1-49	Batt GND	Motherboard GROUND
J1-50	Test pin	Interface board GROUND (used to detect board on test fixture)

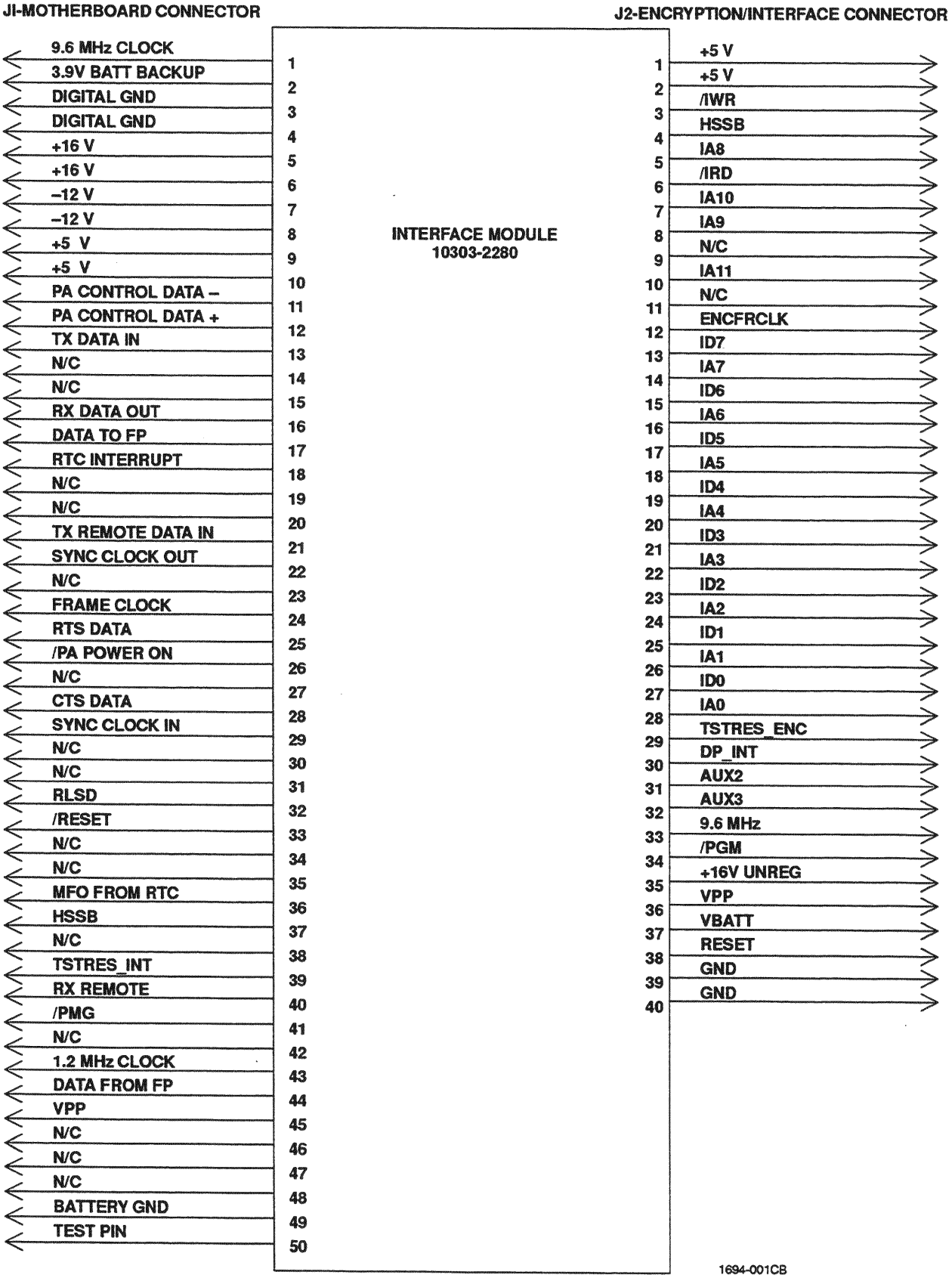


Figure 1. Interface Assembly Interconnect Diagram

3. TECHNICAL DESCRIPTION

3.1 TX Digital Path

Figure 2 contains a block diagram of the control communication paths of the A1A1 Interface Assembly. There are two possible sources of control data coming into the A1A1 Interface Assembly; the auxiliary remote port at the auxiliary data connector and the front panel. Remote control data usually comes from a RS-232 or MIL-188 terminal, or a personal computer running terminal emulation software. This data is translated by U14 from the external data voltage levels to +0 or +5 V digital levels. The serial data is then optionally inverted in the case of MIL-188 by IC U10, and fed into DUSART2 U16, where it is formatted into bytes and passed to the microprocessor U1. U1 then passes this remote control data to the A4A1 Main Controller Module via the internal high-speed serial bus. Front panel control data is handled in a similar way, except that it is already at digital voltage levels and it is not inverted for MIL-188 operation.

The auxiliary remote port is also used to provide asynchronous data for over-the-air transmission by the embedded modem or the RF-5161 Automatic Link Establishment (ALE) option. The data communications path is shown in figure 3. The flow of this data is the same as for the above described control data, except that its final destination is not the A4A1 Main Controller Module. This data is routed by microprocessor U1 to one of the above-mentioned modules (depending upon how the radio is configured). In both cases, the data transmission from the remote port is initiated only by typing a Control-B (^B) (ASCII 02, STX). The remote port cannot be keyed by hardware means, nor can it be used for transmitting synchronous data.

The second source of TX digital data is the auxiliary data port. This port is software configurable for either asynchronous or synchronous operation. This port is only used to provide data for over-the-air transmission by the embedded modem. It cannot be used to provide a remote control function or over-the-air data for the RF-5161 ALE option. The serial transmit data stream is converted from external transmission levels (either RS-232 or MIL-188) to digital levels by IC U14. After this, the data is optionally inverted in the case of MIL-188, and is input to DUSART1 U9, where it is formatted into bytes and given to the microprocessor U1. U1 then transfers the data via the internal high-speed data bus to the embedded modem (specifically module A4A4, the FEC module of the embedded modem), where it is modulated for over-the-air transmission. When the data port is configured for synchronous operation, there are two clocking options for transmit. The data clock can be configured to be sourced by the A1A1 Interface Assembly, or it can be sourced by an external device. Furthermore, when the port is synchronous, it can only be keyed (data transmission initiated) by raising the DATA RTS line, and unkeyed by lowering the line. When configured for asynchronous operation, this port can be keyed either by raising RTS or by typing Control-B (^B) (ASCII 02, STX). If the port is keyed with Control-B (^B), it can be unkeyed by typing Control-C (^C) (ASCII 03, ETX) or, if nothing is typed for a period of 30 seconds, a timeout unkey occurs. If the port is keyed with RTS, the only way to unkey is by dropping RTS.

3.2 RX Digital Path

The auxiliary remote port outputs both remote control/status information and received asynchronous over-the-air data. In either case, the flow is the same. The information is received by the microprocessor U1 and given to DUSART2 U16, where it is converted into a serial stream, optionally inverted for MIL-188 by U10, then converted to transmission voltage levels by U12 or U13. DUSART2 U16 also passes information from the main controller to the front panel. In this case, there is no inversion.

In receive, the auxiliary data port is only used to output received over-the-air modem data. The flow of this data stream is similar to the above, except that the microprocessor gives the data to DUSART1 U9. DUSART1 U9 converts the data into a serial stream which is optionally inverted by U10 and converted to transmission voltage levels by U12 or U13. If the port is configured for synchronous operation, U9 also provides a data clock that is used by an external device to clock in the receive data. Note that in receive, the A1A1 Interface Assembly does not accept an external clock.

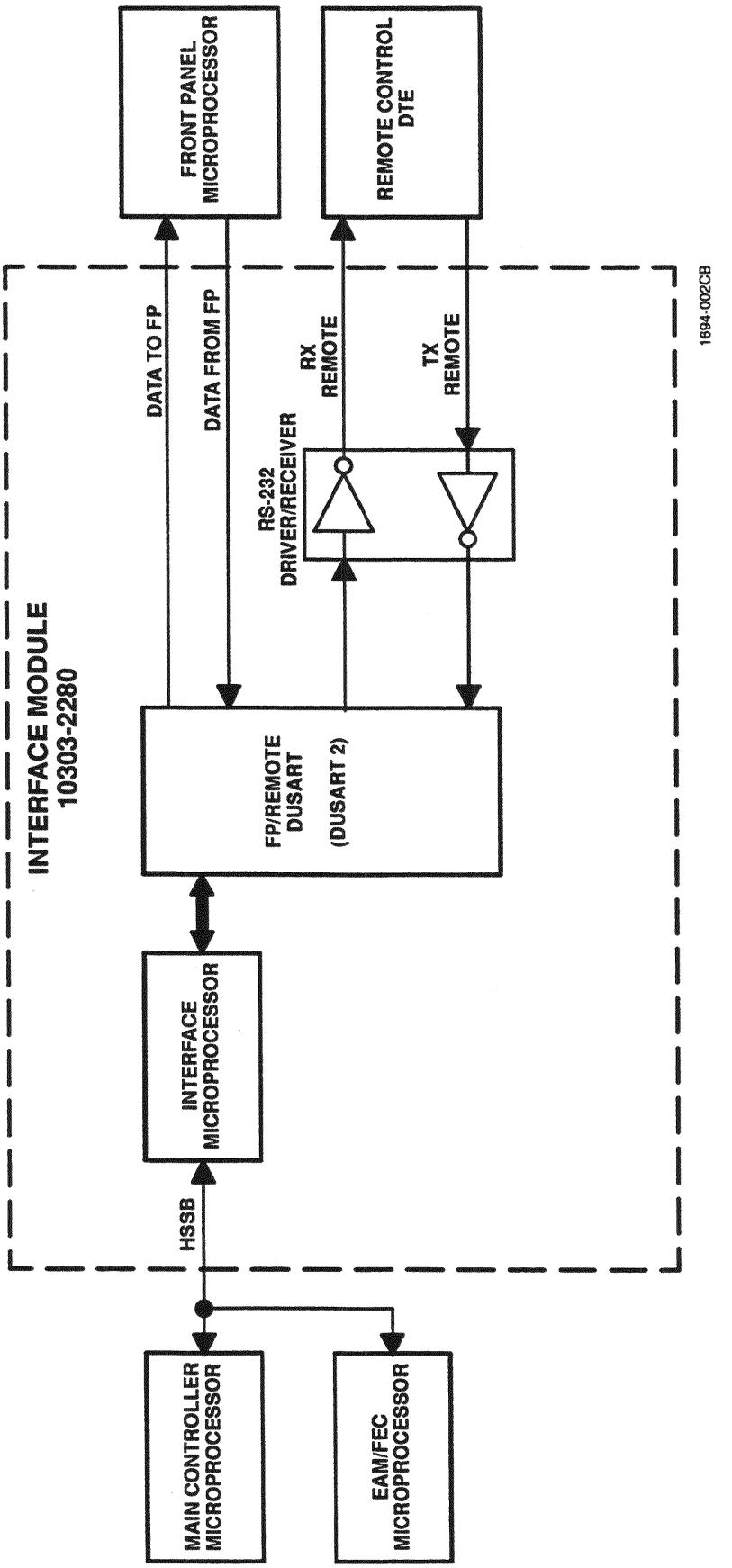


Figure 2. Front Panel and Remote Control Communication Paths

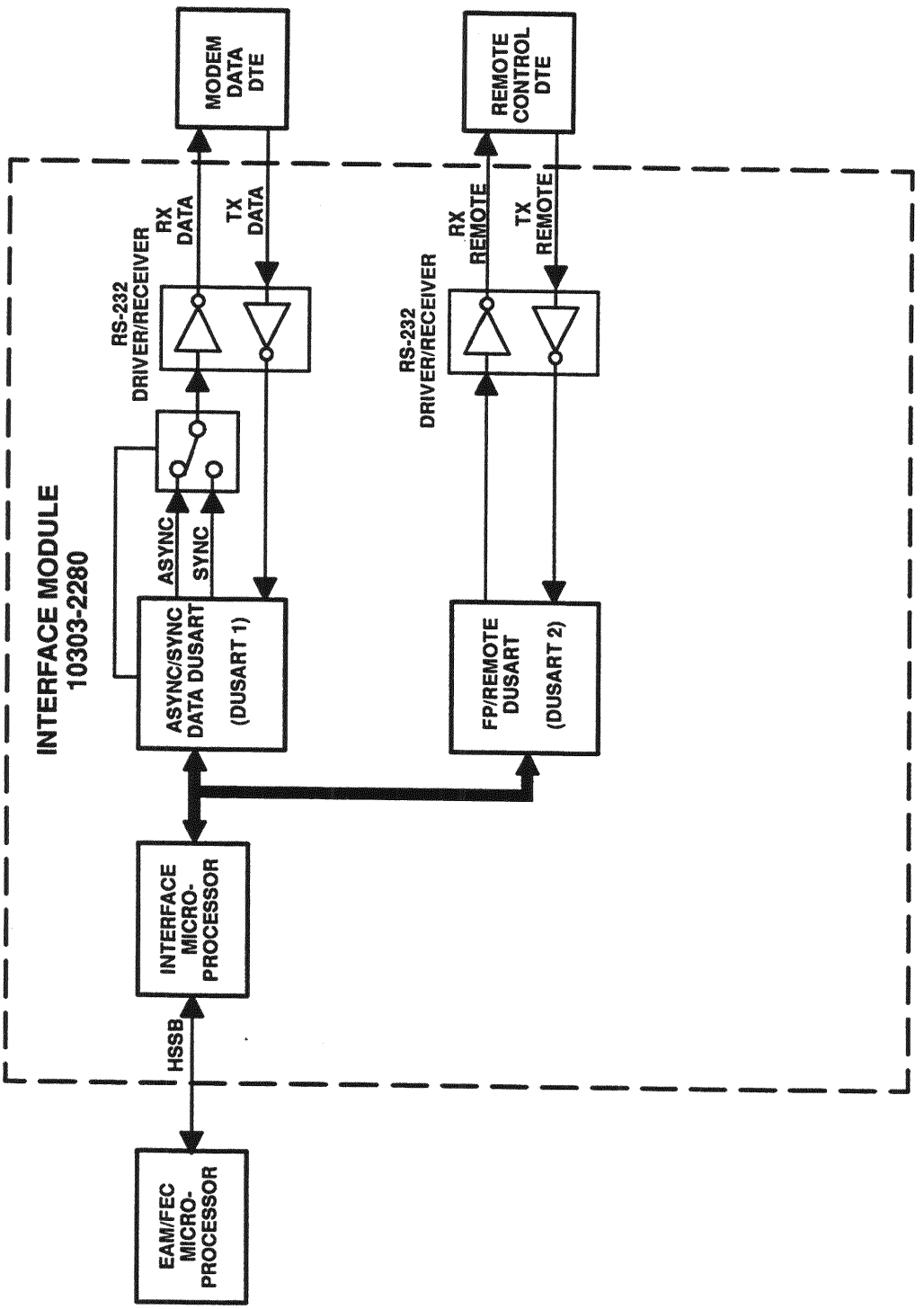


Figure 3. Data Communication Paths

3.3 Encryption

Figure 4 contains a block diagram of the encryption communications flow. In general, data packets are passed back and forth via the DP RAM (A1A2 Encryption Assembly U5). For details of operation, see section of this manual concerning the RF-5170 Encryption Assembly option.

3.4 Real-Time Clock (RTC) Operation

Figure 5 contains a block diagram of the microprocessor's communication link with the real-time clock IC. The RTC U19 maintains the time while the radio is powered off. Since the A4A1 Main Controller Module's clock is more accurate, the RTC on the Interface Assembly is continually updated with the correct time while the radio is powered on.

3.5 External RF-Device Communications

Figure 6 contains a block diagram of the external RF-device communication path. Control information is received from the A4A1 Main Controller Module and then passed through the DUART U25 and the balanced line drivers to the external RF-device at a rate of 150 kbaud.

Responses (if necessary) from the external RF-device are received through the balanced line drivers at a rate of 12.5 kbaud and formatted into bytes by the DUART U25. These bytes are then passed to the A4A1 Main Controller Module.

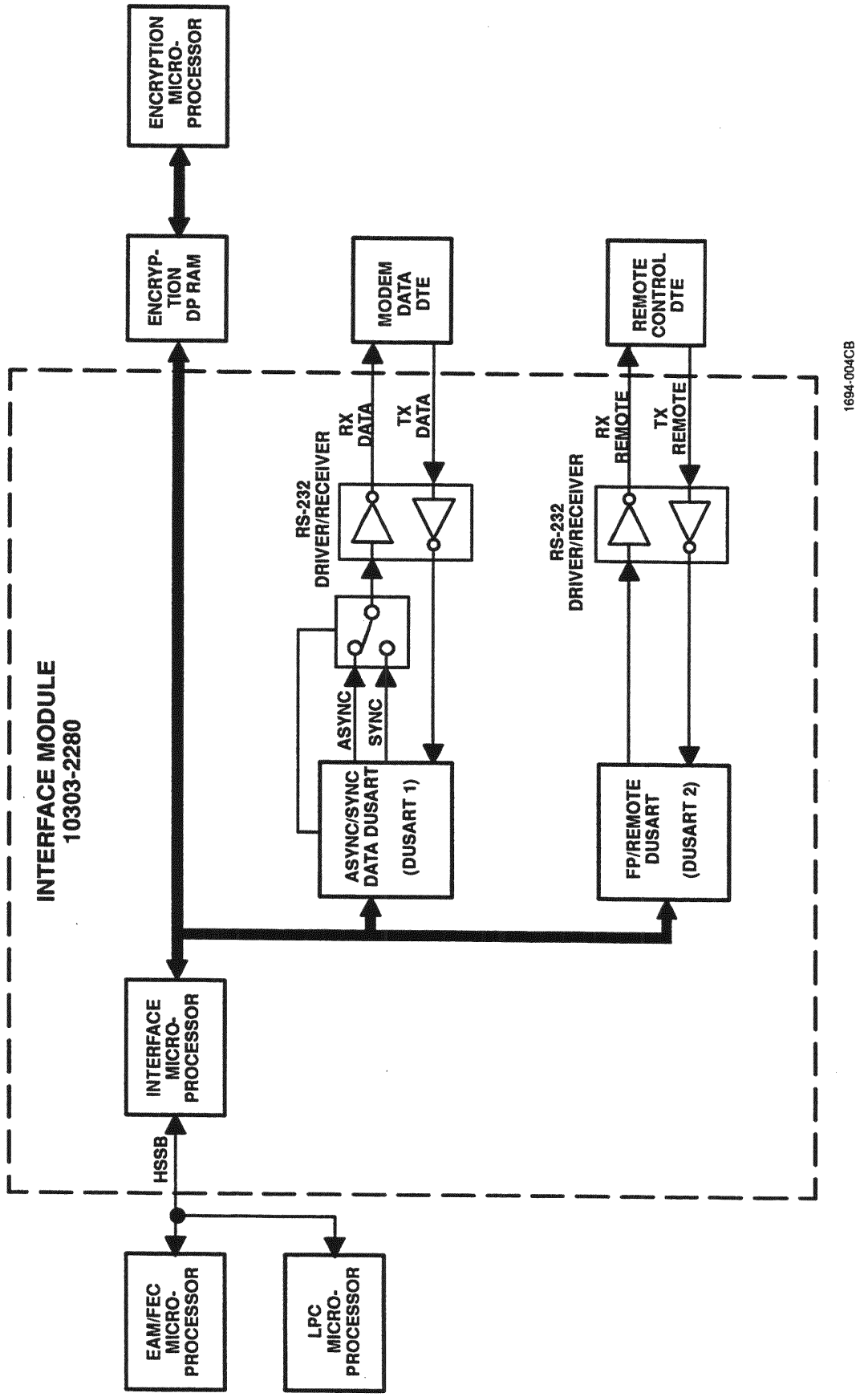


Figure 4. Data/Digital Voice Communication Paths

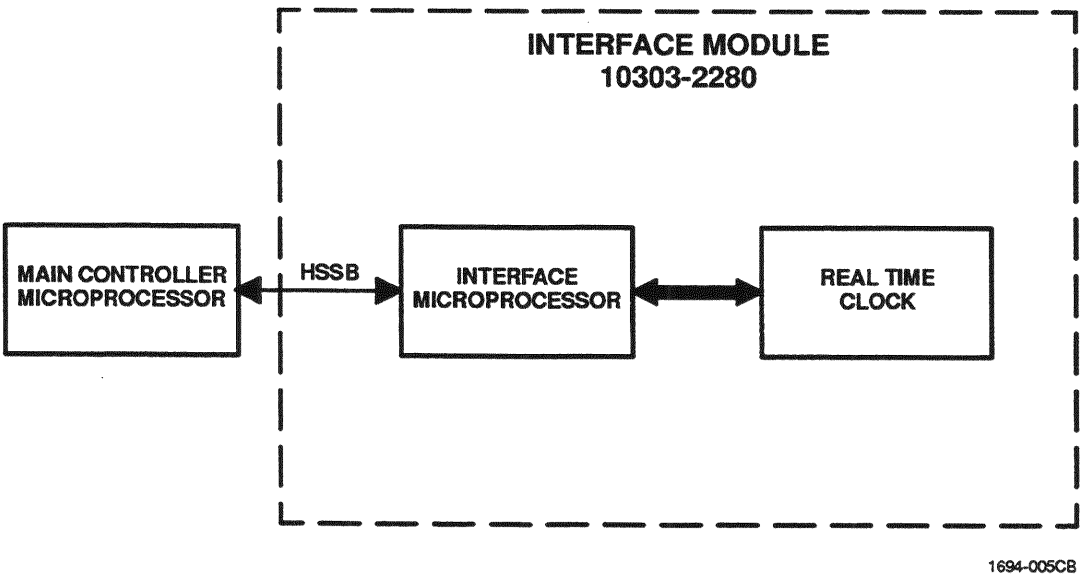


Figure 5. Real-Time Clock Communication Path

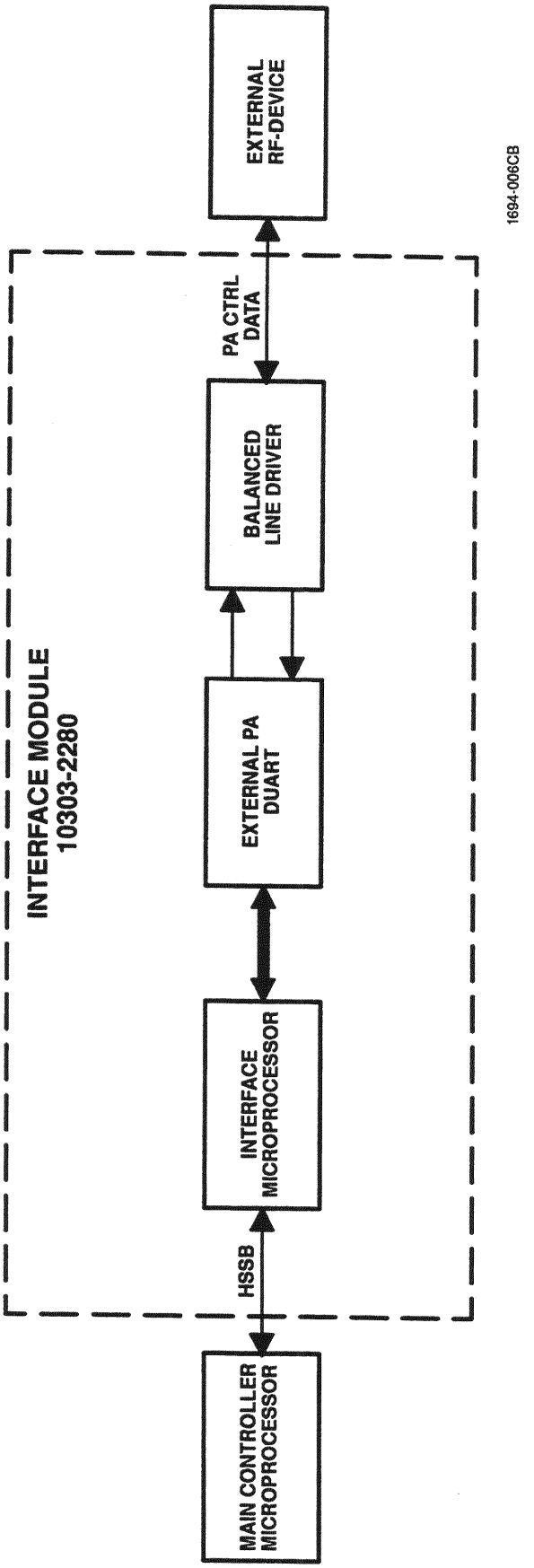


Figure 6. RF-Device Communication Path

4. TESTING AND ALIGNMENT

The A1A1 Interface Assembly requires no regular maintenance, adjustments, or alignments.

5. BITE FAULTS AND TROUBLESHOOTING

Table 3 is a list of self-test fault codes for the A1A1 Interface Assembly. The tests and faults are described in greater detail in the following paragraphs.

The following test equipment is required for troubleshooting:

- Digital multimeter
- Oscilloscope (Tektronix 465m or equivalent)

A basic troubleshooting checklist for the A1A1 Interface Assembly includes checking the following:

- Supply voltages at ICs (+5 V, +12 V, -12V)
- Clocks at ICs (9.6 MHz, 9.216 MHz, 1.2 MHz)
- Correct parts
- Orientation of parts on printed wiring board
- Mistaken placement of capacitors in resistor locations or vice versa
- Cold solder joints or unsoldered pins

WARNING

DO NOT insert the Interface Assembly into the R/T with power supplied to rear panel connectors or the front panel PA connector (this includes batteries). Insert the card first, then attach the supply voltage.

In the uninitialized state, the RTC can generate a signal which enables the power supply. Once the RTC is initialized, this signal should be in its proper state. In addition, if the board has a problem, the RTC may not initialize properly. Consequently, the radio will not turn off until power is removed or the Interface Assembly is removed.

The act of inserting the Interface Assembly into a radio with power supplied is also suspected of damaging the RTC IC.

Table 3. A1A1 Interface Assembly Fault Codes

Code	Fault
01	Communications fault
02	Microprocessor internal RAM fault
03	ROM fault
04	RAM fault
05	Asynchronous Data Channel fault
06	Synchronous Data Channel fault
09	Remote communications channel fault
0A	External PA DUART internal counter fault
0B	External PA communications channel fault
0F	Frame clock fault
10	DP RAM Semaphore Register fault
11	DP RAM fault
51	RTC not installed
52	RTC Internal RAM fault
55	RTC rollover registers fault
56	RTC crystal oscillator failure
81	Encryption communications fault

5.1 Fault 01 – Communications Fault

The communications fault indicates that the A4A1 Main Controller Module cannot communicate with the A1A1 Interface Assembly. It implies a fault that prevents the 87C51 microprocessor from running. In reality, this fault should not be able to occur because the Interface Assembly must be communicating in order for the operator to start the BITE test. A failure might indicate a problem with the BITE test internal timing.

5.2 Fault 02 – Microprocessor Internal RAM Fault

The microprocessor (internal RAM) fault indicates that the RAM internal to U1, the 83C51 microprocessor, is faulty. Replace U1.

5.3 Fault 03 – ROM Fault

The ROM fault test verifies the proper operation of the program memory by performing an additive checksum test on the PROM. Every memory location in the PROM is added together and compared with a value stored in the PROM. Failing this test indicates either a faulty PROM or some other failure that prevents the microprocessor from correctly accessing program memory.

This fault indicates that U5 has failed the ROM checksum test. Replace U5.

5.4 Fault 04 – RAM Fault

The RAM fault verifies the proper operation of the CMOS RAM U4. It performs a nondestructive test of all memory locations, first saving the data, then writing and reading a pattern from each address location.

This fault indicates that U4 has failed the RAM test. Replace U4.

5.5 Fault 05 – Asynchronous Data Channel Fault

This test verifies the internal operation of DUSART1 U9. It performs an internal loop-back test. The DUSART provides communication between the data port serial lines and the microprocessor.

Perform the following test to indicate an asynchronous data channel fault:

a. Verify 9.6 MHz input on pin 13 of U9.

b. If 9.6 MHz is present, verify 9.216 MHz on pin 23 of U9.

c. If 9.216 MHz is not present, check oscillator and replace crystal Y1, if necessary.

d. If both 9.6 MHz and 9.216 MHz are present, replace U9.

5.6 Fault 06 – Synchronous Data Channel Fault

This test verifies the internal operation of DUSART1 U9. It performs an internal loop-back test. The DUSART provides communication between the data port serial lines and the microprocessor.

Perform the following test to indicate a synchronous data channel fault:

a. Verify 9.6 MHz input on pin 13 of U9.

b. If 9.6 MHz is present, verify 9.216 MHz on pin 23 of U9.

c. If 9.216 MHz is not present, check oscillator and replace crystal Y1, if necessary.

d. If both 9.6 MHz and 9.216 MHz are present, replace U9.

5.7 Fault 09 – Remote Communications Channel Fault

This test verifies the operation of DUSART2 U16. It performs an internal loop-back test. DUSART2 is used to communicate with the front panel and the auxiliary remote port.

Perform the following test to indicate a remote communications channel fault:

a. Verify 9.6 MHz input on pin 13 of U16.

b. If 9.6 MHz is present, verify 9.216 MHz on pin 23 of U16.

c. If 9.216 MHz is not present, check oscillator and replace crystal Y1, if necessary.

d. If both 9.6 MHz and 9.216 MHz are present, replace U16.

5.8 Fault 0A – EXTERNAL PA DUART Counter Fault

Perform the following DUART counter fault test to verify the operation of the baud rate generator internal to the DUART U25:

a. Verify 1.2 MHz at U25-40 and U25-36. Trace back to J1-43.

b. Verify 150 kHz at U25-3, U25-15, and U25-43 while self-test is performed. U25-15 is the output of the baud rate generator.

c. If 150 KHz is not present, replace U25.

5.9 Fault 0B – External PA Communications Channel Fault

The DUART serial data fault test verifies operation of the DUART U25. It performs internal testing of the integrated circuit as well as a loop-back test on board. The DUART is used to communicate with the power amplifiers and antenna couplers in the system. This communication is performed via high-speed serial data using a proprietary Harris protocol. The serial data is differentially buffered using U22 and U23. U15 is a differential receiver. The data is sent using a bidirectional link; therefore, any data sent is also received.

Since it is possible for a faulty power amplifier to cause this fault indication, it is important that the following test be performed while the radio is connected to a known good power amplifier.

a. While changing the frequency of the radio, verify activity on U25-33, TX data to the power amplifier. If no activity occurs, replace U25.

b. Verify inverted activity at U22-4 and U23-8.

c. Verify non-inverted activity at U23-3 and U23-6.

d. Verify U23 output enabled by U23-4 and U23-10. U25-32 should be low during data activity.

e. If there is no enable, replace U25.

f. If there is no data at the outputs of U23, replace U23.

g. Verify data while changing frequency at J1-11, J1-12, U15-2, and U15-3.

h. If U15-1 output does not match U15-3 input, replace U15.

i. Otherwise, replace U25.

5.10 Fault 10 – Semaphore Register Fault

Perform the following procedure to test the Interface Assembly's half of the A1A2 Data Encryption Assembly's (10303-2240) dual port RAM semaphore registers:

a. Verify that the A1A2 Data Encryption Assembly is installed.

b. If the assembly is installed, replace A1A2 U5 on the Data Encryption Assembly.

5.11 Fault 11 – Dual Port RAM Fault

Perform the following procedure to do a non-destructive RAM test of the dual port RAM on the A1A2 Data Encryption Assembly:

a. Verify that the A1A2 Data Encryption Assembly is installed.

b. If the assembly is installed, replace A1A2 U5 on the Data Encryption Module.

5.12 Faults 0F - Frame Clock Fault

The frame clock fault test verifies the ability of the Interface Assembly microprocessor U1 to detect activity on the frame clock line J1-24. The frame clock is used to synchronize data transfers between the A1A1 Interface Assembly and the A4A(4-6) Modem Module. This line pulses at a regular rate whenever the modem is enabled.

Perform the following test to indicate a frame clock fault:

a. With the radio in SSB mode and the modem on, observe U1-14. There should be a narrow (< 10 usec) pulse every 22.5 milliseconds.

b. If the frame clock cannot be detected, it must be traced back to the A4A(4-6) Modem Module.

c. If the frame clock is detected and the radio fails this test, replace U1.

5.13 Fault 51 - Real-Time Clock (RTC) Fault

This failure indicates that the RTC chip does not respond to any signals that are sent to it. Perform the following procedure to indicate a RTC fault:

a. Verify the crystal oscillator circuit (chip and crystal) by observing a 32.768 kHz square wave at U19-12.

b. Verify the presence of +5 V on U19-28 and 3 V on U19-11.

c. If supply voltages are present, replace U19.

5.14 Fault 52 - RTC Internal RAM Fault

A non-destructive RAM test is done during BITE on two blocks of RAM within U19. If this fault occurs, replace U19.

5.15 Fault 55 - RTC Rollover Registers Fault Fault

This fault indicates that the internal time of U19 is not functioning correctly. Replace U19.

5.16 Fault 56 - RTC Crystal Oscillator Fault

Check for the presence of a 32.768 kHz square wave at U19-12. If the signal is present, replace U19. If the waveform is not present, replace Y2.

5.17 Fault 81 - Encryption No Communication Fault

Perform the following test to verify that the A1A1 Interface Assembly can communicate with the A1A2 Encryption Assembly during self-test:

a. If the Fault 81 fault code appears, swap the A1A2 Encryption Assembly with one that is known to be working.

b. If the problem clears up, then replace the dual port RAM U5 on the original A1A2 Encryption Assembly and run self-test again.

6. PARTS LIST, COMPONENT LOCATION DIAGRAM, AND SCHEMATIC DIAGRAM

Table 4 is the parts list, figure 7 is the component location diagram, and figure 8 is the schematic diagram for the A1A1 Interface Assembly.

Table 4. A1A1 Interface Assembly Parts List (10303-2280 Rev. F)

Ref. Desig.	Part Number	Description
1	10303-2289	PWB
2	10303-1089	RIVET
3	P15-3145-001	SEALER RTV 3145 CLEAR
4	10372-1524-03	CORD ASSY
BT1	B41-0013-002	BAT LITHIUM 3.5V
C1	C13-0103-333	CAP .033UF 10% 100V SMD
C2	C13-0103-333	CAP .033UF 10% 100V SMD
C3	C13-0103-333	CAP .033UF 10% 100V SMD
C4	C13-0103-333	CAP .033UF 10% 100V SMD
C5	C13-0101-220	CAP 22PF 10% 100V SMD
C6	C13-0103-333	CAP .033UF 10% 100V SMD
C7	C36-0016-685	CAP 6.8UF 10% 16V TANT
C8	C13-0105-102	CAP CER 1000PF 5% 100V
C9	C13-0105-102	CAP CER 1000PF 5% 100V
C10	C13-0105-102	CAP CER 1000PF 5% 100V
C11	C36-0035-106	CAP TANT 10UF 10% 35V
C12	C36-0035-106	CAP TANT 10UF 10% 35V
C13	C13-0101-220	CAP 22PF 10% 100V SMD
C14	C13-0103-103	CAP .01UF 10% 100V SMD
C15	C36-0035-335	CAP 3.3UF 10% 35V TANT
C16	C36-0035-106	CAP TANT 10UF 10% 35V
C17	C36-0035-335	CAP 3.3UF 10% 35V TANT
C18	C13-0101-470	CAP 47PF 10% 50V CER
C19	C13-0101-470	CAP 47PF 10% 50V CER
C20	C13-0103-333	CAP .033UF 10% 100V SMD
C21	C13-0105-102	CAP CER 1000PF 5% 100V
C22	C13-0103-333	CAP .033UF 10% 100V SMD
C23	C13-0103-103	CAP .01UF 10% 100V SMD
C24	C13-0103-103	CAP .01UF 10% 100V SMD
C25	C13-0105-102	CAP CER 1000PF 5% 100V
C26	C13-0105-471	CAP 470PF 5% 100V SMD
C27	C13-0105-471	CAP 470PF 5% 100V SMD
C28	C13-0103-333	CAP .033UF 10% 100V SMD
C29	C13-0103-333	CAP .033UF 10% 100V SMD
C30	C13-0103-333	CAP .033UF 10% 100V SMD
C31	C13-0103-333	CAP .033UF 10% 100V SMD
C32	C13-0103-333	CAP .033UF 10% 100V SMD
C33	C13-0103-333	CAP .033UF 10% 100V SMD
C34	C13-0103-333	CAP .033UF 10% 100V SMD

Table 4. A1A1 Interface Assembly Parts List (10303-2280 Rev. F) (Cont.)

Ref. Desig.	Part Number	Description
C35	C13-0103-333	CAP .033UF 10% 100V SMD
C36	C13-0103-333	CAP .033UF 10% 100V SMD
C37	C13-0103-333	CAP .033UF 10% 100V SMD
C38	C13-0105-471	CAP 470PF 5% 100V SMD
C39	C13-0105-471	CAP 470PF 5% 100V SMD
C40	C13-0105-471	CAP 470PF 5% 100V SMD
C41	C13-0105-471	CAP 470PF 5% 100V SMD
C42	C13-0105-471	CAP 470PF 5% 100V SMD
C43	C13-0105-471	CAP 470PF 5% 100V SMD
C44	C13-0103-333	CAP .033UF 10% 100V SMD
C45	C13-0103-333	CAP .033UF 10% 100V SMD
C46	C13-0103-333	CAP .033UF 10% 100V SMD
C47	C13-0103-333	CAP .033UF 10% 100V SMD
C49	C13-0103-333	CAP .033UF 10% 100V SMD
CR1	D15-0002-001	DIODE, DUAL (MMBD2835L)
CR3	D15-0914-101	DIODE HI-SPD SWITCHING
J1	J46-0117-050	CONN, 50 PIN MALE
J2	J46-0116-040	40 PIN, FEMALE, SMD CONN
L1	10303-3113-01	TOROID, 130UH
L2	L45-0007-033	INDUCTOR SMD 5.6UH
L3	L45-0007-033	INDUCTOR SMD 5.6UH
Q1	Q02-2907-101	XSTR SS/GP PNP MMBT2907A
Q2	Q12-2222-101	XSTR NPN SWG SM SS/GP
Q3	Q02-2907-101	XSTR SS/GP PNP MMBT2907A
Q4	Q12-2222-101	XSTR NPN SWG SM SS/GP
Q5	Q12-2222-101	XSTR NPN SWG SM SS/GP
Q6	Q12-2222-101	XSTR NPN SWG SM SS/GP
Q7	Q02-2907-101	XSTR SS/GP PNP MMBT2907A
R1	R85-0004-334	RES 22.1K 1% 1/8W FLM
R2	R85-0004-201	RES 1000 1% 1/8W FLM
R3	R85-0004-401	RES 100K 1% 1/8W FLM
R4	R85-0004-266	RES,4.75K 1% 1/8W CHIP
R5	R85-0004-101	RES 100 1% 1/8W FLM
R6	R85-0004-266	RES,4.75K 1% 1/8W CHIP
R7	R85-0004-301	RES 10K 1% 1/8W FLM
R8	R85-0004-101	RES 100 1% 1/8W FLM
R9	R85-0004-334	RES 22.1K 1% 1/8W FLM
R10	R85-0004-101	RES 100 1% 1/8W FLM
R12	R85-0004-201	RES 1000 1% 1/8W FLM

Table 4. A1A1 Interface Assembly Parts List (10303-2280 Rev. F) (Cont.)

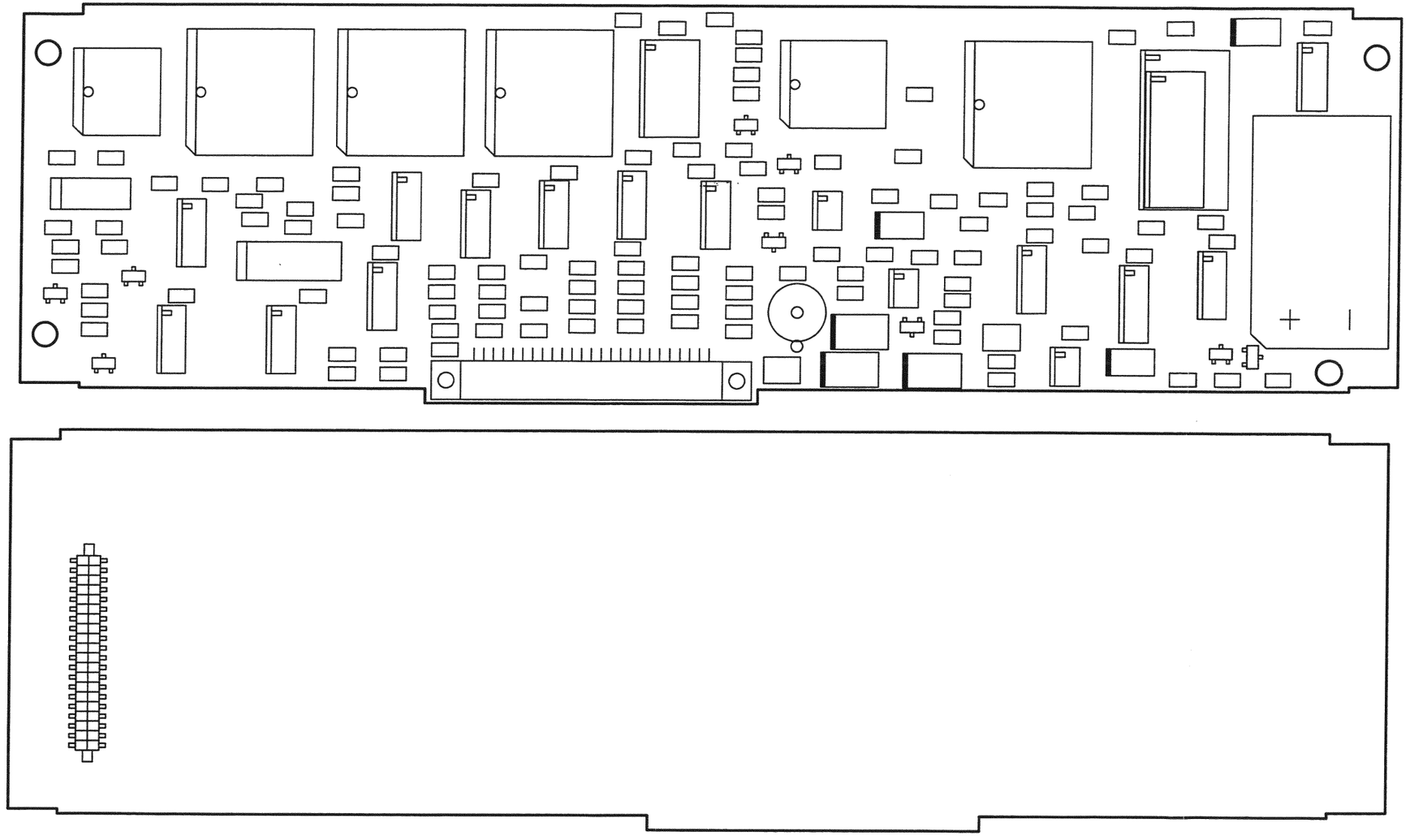
Ref. Desig.	Part Number	Description
R13	R85-0004-266	RES,4.75K 1% 1/8W CHIP
R14	R85-0004-334	RES 22.1K 1% 1/8W FLM
R15	R85-0004-301	RES 10K 1% 1/8W FLM
R16	R85-0004-101	RES 100 1% 1/8W FLM
R17	R85-0004-101	RES 100 1% 1/8W FLM
R18	R85-0004-334	RES 22.1K 1% 1/8W FLM
R19	R85-0004-000	RES ZERO OHM 1/8W FILM
R21	R85-0004-101	RES 100 1% 1/8W FLM
R22	R85-0004-334	RES 22.1K 1% 1/8W FLM
R23	R85-0004-334	RES 22.1K 1% 1/8W FLM
R24	R85-0004-101	RES 100 1% 1/8W FLM
R25	R85-0004-101	RES 100 1% 1/8W FLM
R26	R85-0004-101	RES 100 1% 1/8W FLM
R27	R85-0004-101	RES 100 1% 1/8W FLM
R28	R85-0004-101	RES 100 1% 1/8W FLM
R29	R85-0004-101	RES 100 1% 1/8W FLM
R30	R85-0004-101	RES 100 1% 1/8W FLM
R31	R85-0004-101	RES 100 1% 1/8W FLM
R32	R85-0004-101	RES 100 1% 1/8W FLM
R33	R85-0004-101	RES 100 1% 1/8W FLM
R34	R85-0004-334	RES 22.1K 1% 1/8W FLM
R35	R85-0004-101	RES 100 1% 1/8W FLM
R36	R85-0004-101	RES 100 1% 1/8W FLM
R37	R85-0004-101	RES 100 1% 1/8W FLM
R38	R85-0004-101	RES 100 1% 1/8W FLM
R39	R85-0004-401	RES 100K 1% 1/8W FLM
R40	R85-0004-334	RES 22.1K 1% 1/8W FLM
R41	R85-0004-334	RES 22.1K 1% 1/8W FLM
R42	R85-0004-401	RES 100K 1% 1/8W FLM
R43	R85-0004-301	RES 10K 1% 1/8W FLM
R44	R85-0004-143	RES 274 1% 1/8W FLM
R45	R85-0004-238	RES 2.43K 1%
R46	R85-0004-201	RES 1000 1% 1/8W FLM
R47	R85-0004-334	RES 22.1K 1% 1/8W FLM
R49	R85-0004-266	RES,4.75K 1% 1/8W CHIP
R50	R85-0004-266	RES,4.75K 1% 1/8W CHIP
R51	R85-0004-173	RES 562 1% 1/8W FLM
R52	R85-0004-266	RES,4.75K 1% 1/8W CHIP
R53	R85-0004-216	RES 1430 1% 1/8W FLM

Table 4. A1A1 Interface Assembly Parts List (10303-2280 Rev. F) (Cont.)

Ref. Desig.	Part Number	Description
R54	R85-0004-301	RES 10K 1% 1/8W FLM
R55	R85-0004-451	RES 332K 1% 1/8W SMD
R56	R85-0004-266	RES,4.75K 1% 1/8W CHIP
R57	R85-0004-266	RES,4.75K 1% 1/8W CHIP
R58	R85-0004-301	RES 10K 1% 1/8W FLM
R59	R85-0004-401	RES 100K 1% 1/8W FLM
R60	R85-0004-334	RES 22.1K 1% 1/8W FLM
R61	R85-0004-000	RES ZERO OHM 1/8W FILM
R62	R85-0004-334	RES 22.1K 1% 1/8W FLM
R63	R85-0004-334	RES 22.1K 1% 1/8W FLM
R64	R85-0004-334	RES 22.1K 1% 1/8W FLM
R65	R85-0004-334	RES 22.1K 1% 1/8W FLM
R66	R85-0004-334	RES 22.1K 1% 1/8W FLM
R67	R85-0004-301	RES 10K 1% 1/8W FLM
U1	10181-8017	PROG. TN 83C51FA PLCC MIC
U2	I01-5000-138	3 TO 8 DECODER (74HC138D)
U3	I01-5000-573	8-BIT LATCH (74HC573DW)
U4	I26-0021-012	IC RAM HM62256LFPI-15T
U5	I25-0033-006	128K X 8 FLASH EPROM, IC
U6	I01-5000-008	IC 74HC08AD PLSTC CMOS
U7	I02-0021-005	IC, MC74HCU04D HEX INV
U8	I01-5000-008	IC 74HC08AD PLSTC CMOS
U9	I61-0011-010	Z8523010VEC
U10	I01-5000-086	IC 74HC86 CMOS SMD
U11	I01-5000-125	QUAD TRI-STATE (74HC125D)
U12	I17-0018-001	SN75C188D
U13	I17-0018-001	SN75C188D
U14	I17-0017-001	75C189
U15	I20-0010-004	IC LM2903D COMPARATORD
U16	I61-0011-010	Z8523010VEC
U17	I01-5000-086	IC 74HC86 CMOS SMD
U18	I01-5000-125	QUAD TRI-STATE (74HC125D)
U19	I35-0015-002	IC REAL TIME CLOCK PLCC
U20	I11-0015-008	REGULATOR, SM
U21	I11-0012-009	LM337LM ADJ NEG REG
U22	I02-0021-005	IC, MC74HCU04D HEX INV
U23	I01-5000-125	QUAD TRI-STATE (74HC125D)
U25	I61-0006-006	88C681J/44 DUART

Table 4. A1A1 Interface Assembly Parts List (10303-2280 Rev. F) (Cont.)

Ref. Desig.	Part Number	Description
Y1	Y15-0004-946	XTAL, 9.216 MHZ,MA-506
Y2	Y15-0004-005	XTL RTC 32.768 KHZ SMD

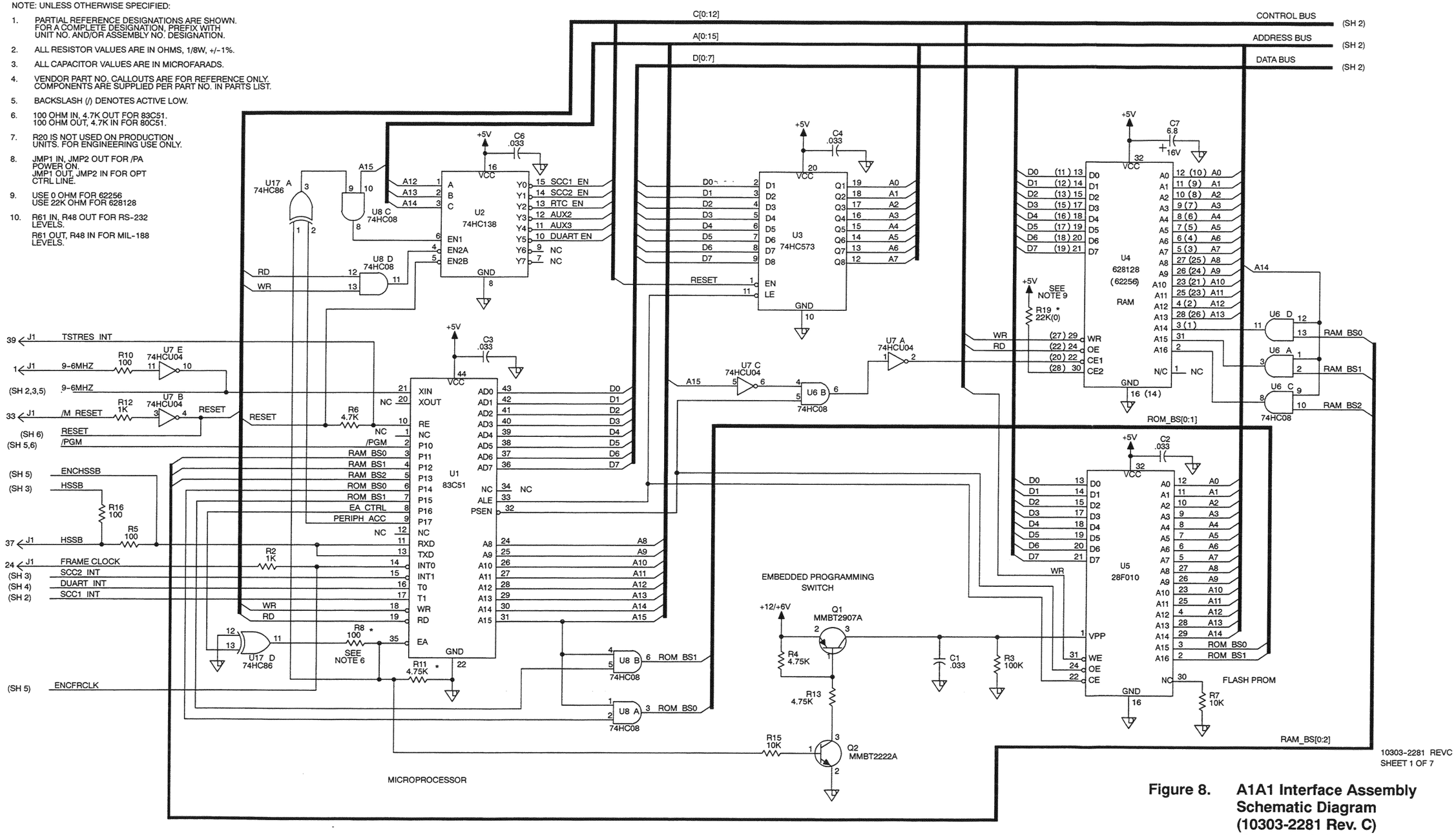


10303-2280

Figure 7. **A1A1 Interface Assembly Component Location Diagram (10303-2280 Rev. A)**

NOTE: UNLESS OTHERWISE SPECIFIED:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR A COMPLETE DESIGNATION, PREFIX WITH UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.
2. ALL RESISTOR VALUES ARE IN OHMS, 1/8W, +/-1%.
3. ALL CAPACITOR VALUES ARE IN MICROFARADS.
4. VENDOR PART NO. CALLOUTS ARE FOR REFERENCE ONLY. COMPONENTS ARE SUPPLIED PER PART NO. IN PARTS LIST.
5. BACKSLASH (/) DENOTES ACTIVE LOW.
6. 100 OHM IN, 4.7K OUT FOR 83C51. 100 OHM OUT, 4.7K IN FOR 80C51.
7. R20 IS NOT USED ON PRODUCTION UNITS. FOR ENGINEERING USE ONLY.
8. JMP1 IN, JMP2 OUT FOR /PA POWER ON. JMP1 OUT, JMP2 IN FOR OPT CTRL LINE.
9. USE 0 OHM FOR 62256 USE 22K OHM FOR 628128
10. R61 IN, R48 OUT FOR RS-232 LEVELS. R61 OUT, R48 IN FOR MIL-188 LEVELS.



10303-2281 REVC
SHEET 1 OF 7

Figure 8. A1A1 Interface Assembly Schematic Diagram (10303-2281 Rev. C) (Sheet 1 of 7)

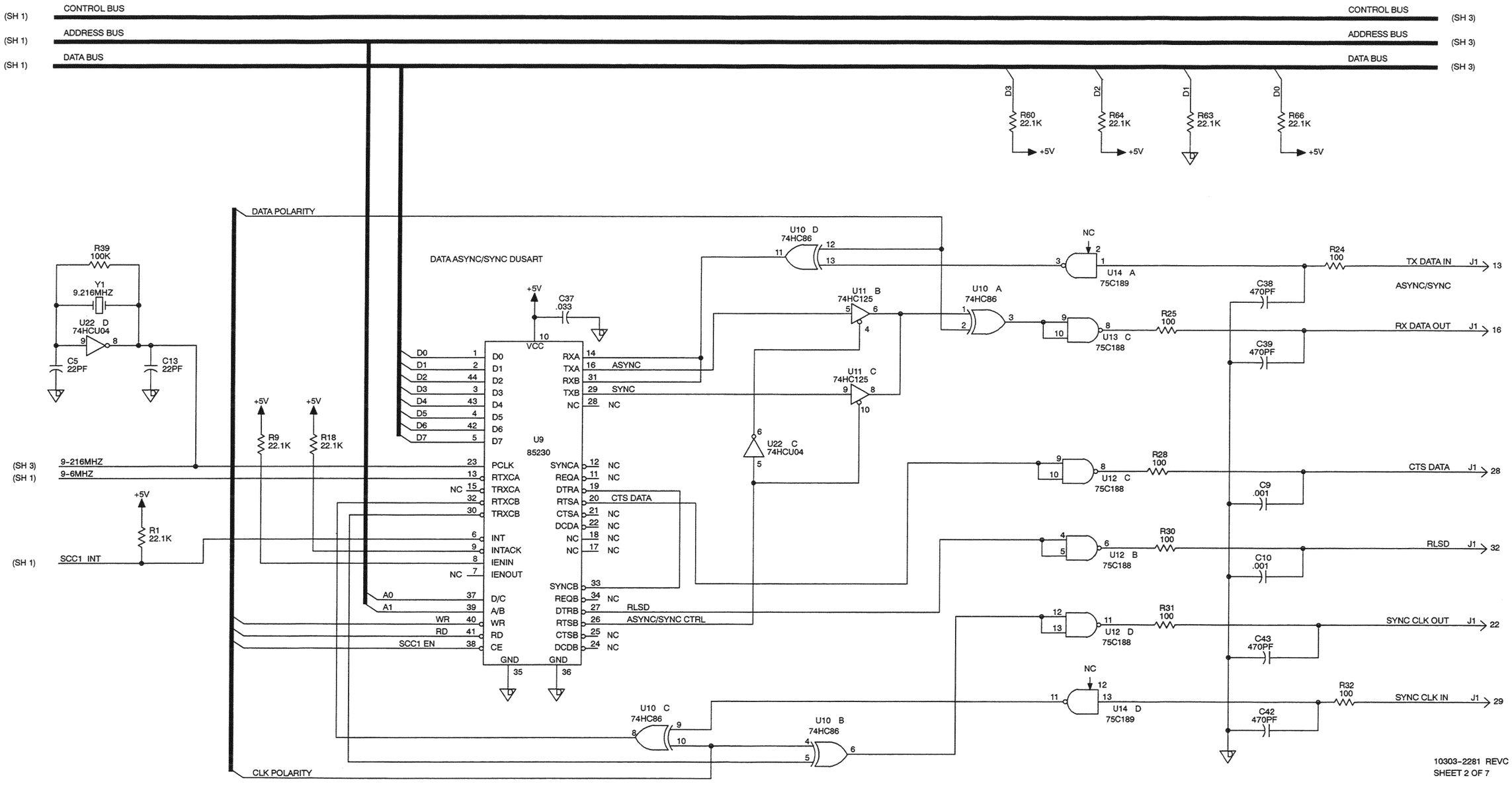


Figure 8. A1A1 Interface Assembly Schematic Diagram (10303-2281 Rev. C) (Sheet 2 of 7)

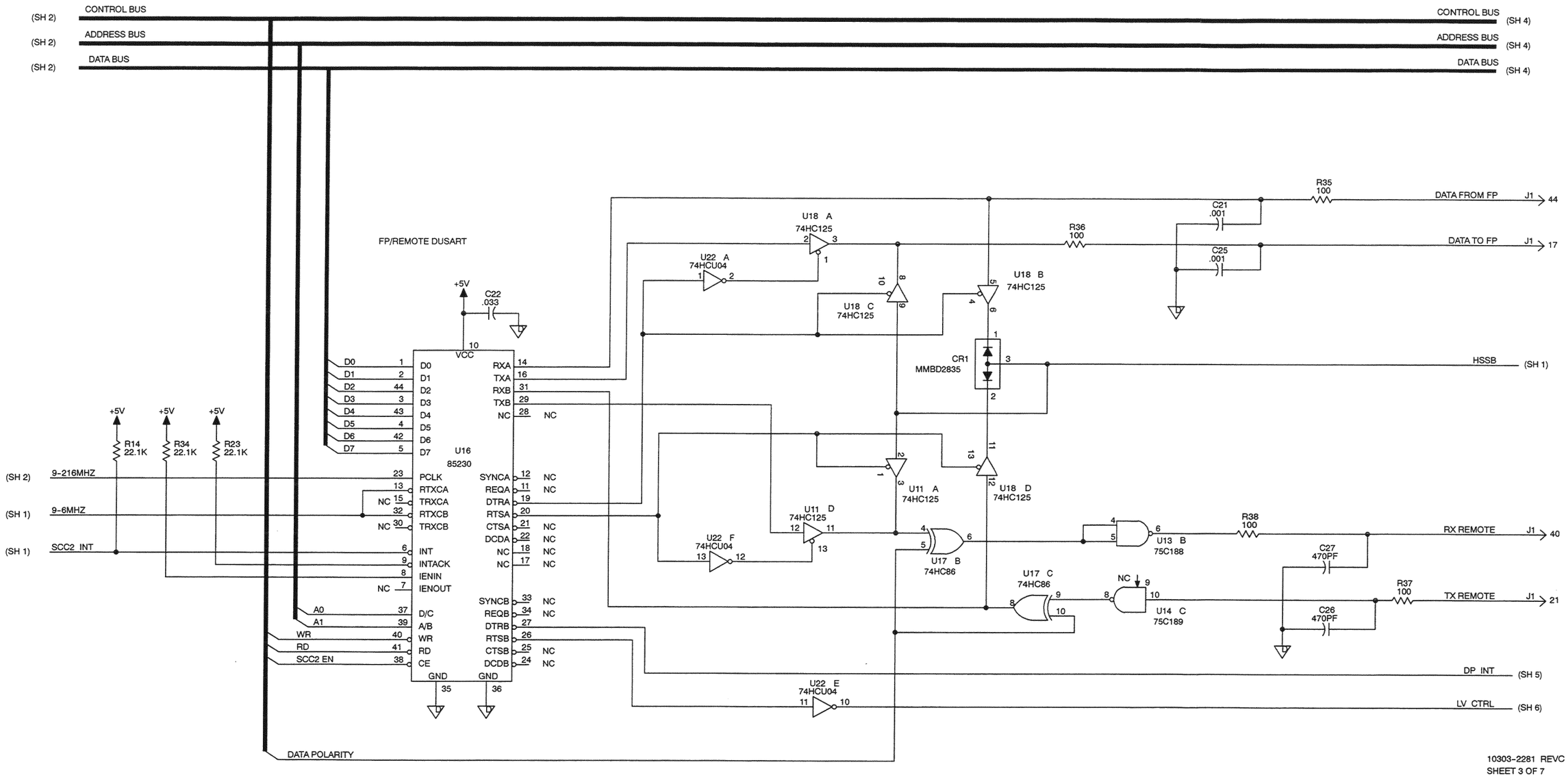
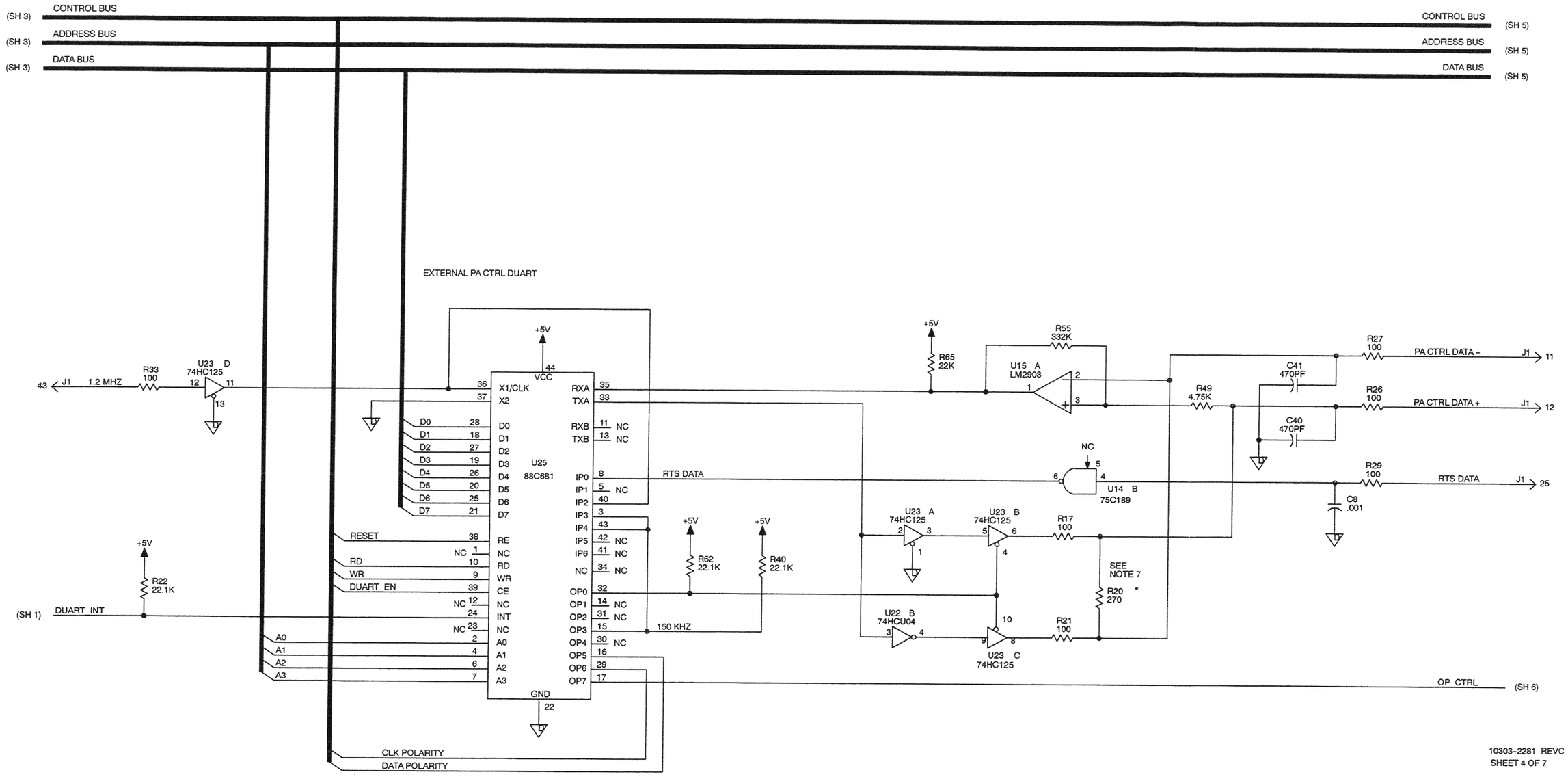
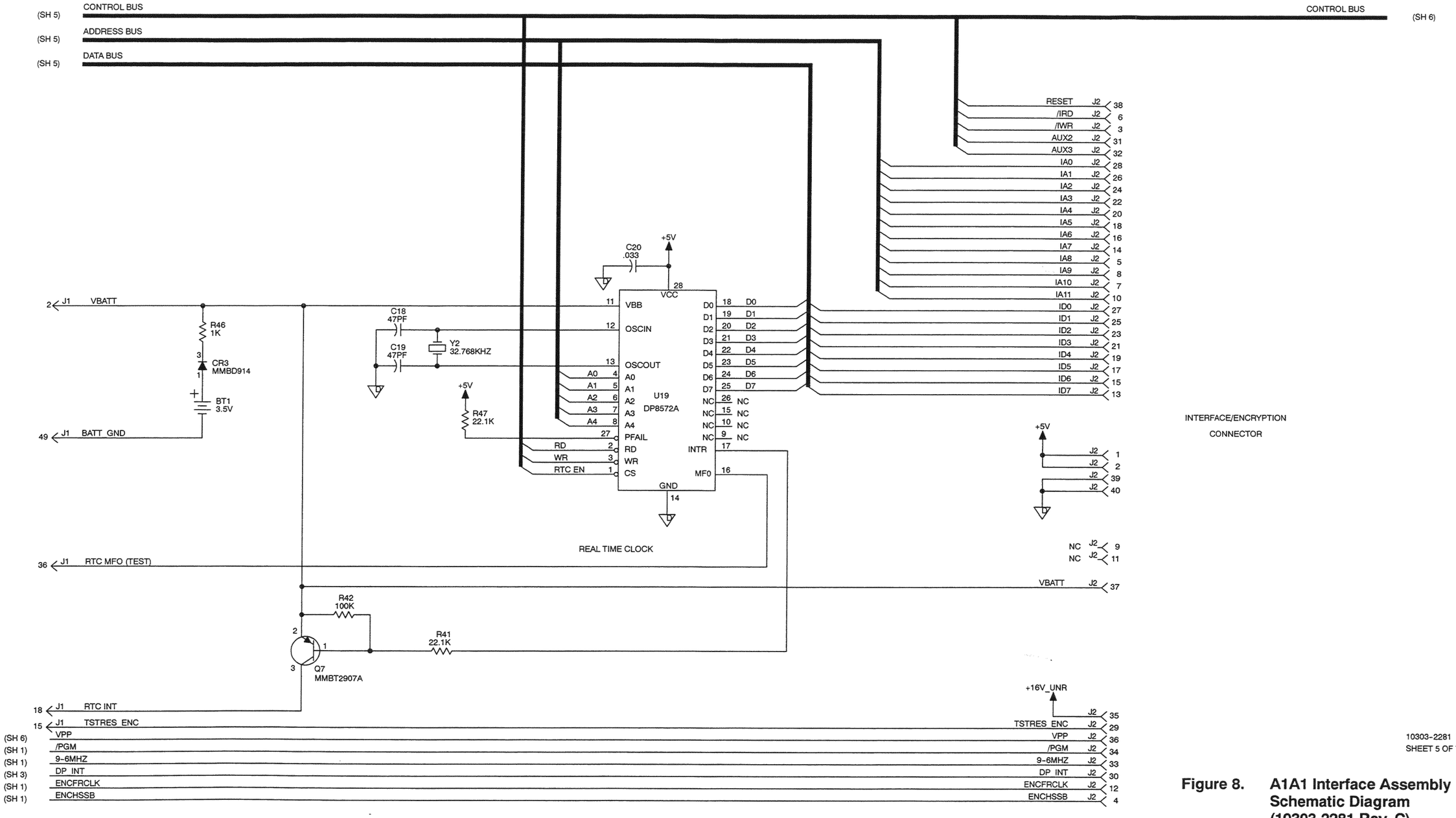


Figure 8. A1A1 Interface Assembly Schematic Diagram (10303-2281 Rev. C) (Sheet 3 of 7)



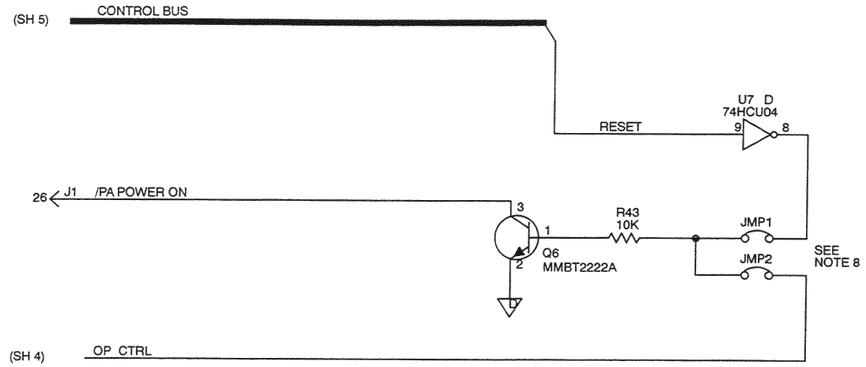
10303-2281 REVC
SHEET 4 OF 7

Figure 8. A1A1 Interface Assembly Schematic Diagram (10303-2281 Rev. C) (Sheet 4 of 7)

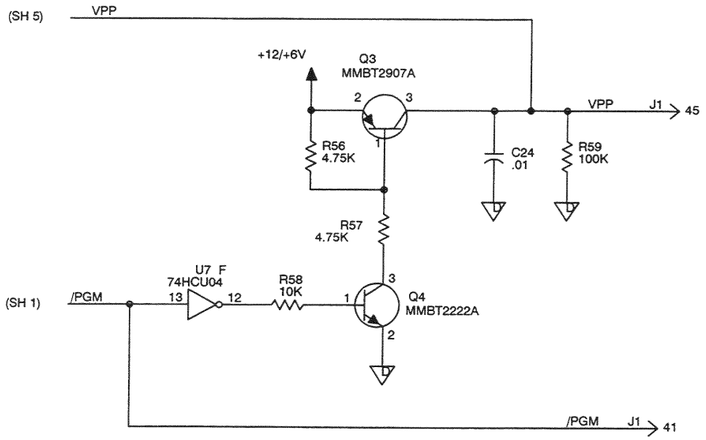


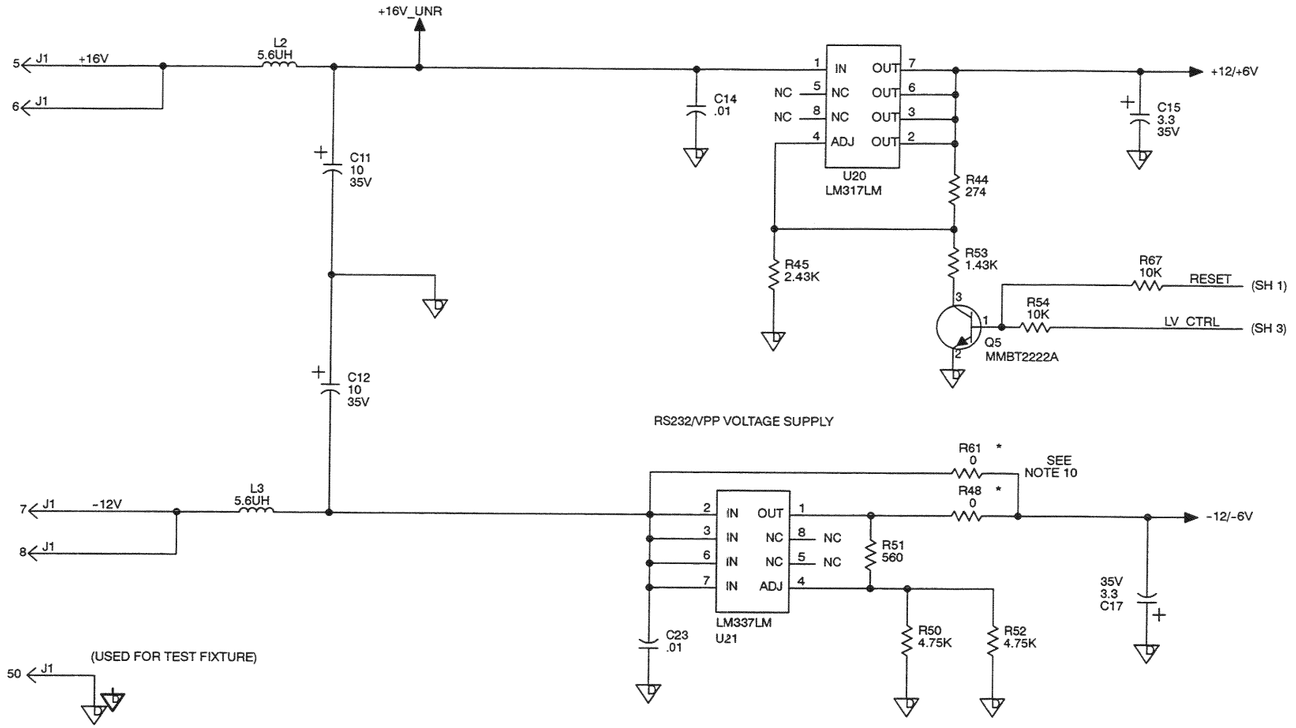
10303-2281 REVC
SHEET 5 OF 7

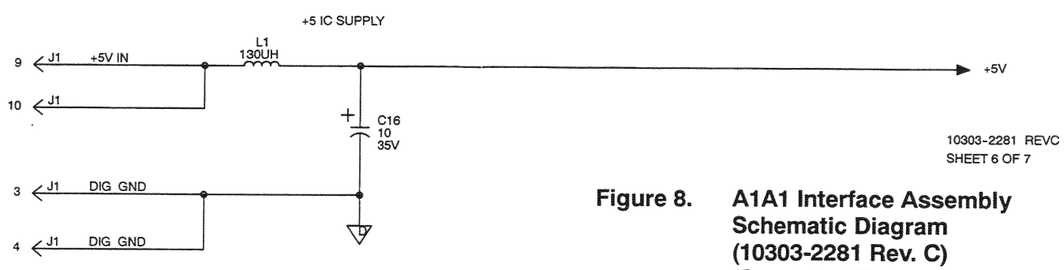
Figure 8. A1A1 Interface Assembly Schematic Diagram (10303-2281 Rev. C) (Sheet 5 of 7)



EMBEDDED PROGRAMMING
CONTROL AND VOLTAGE







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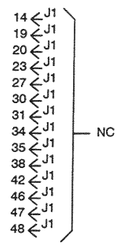
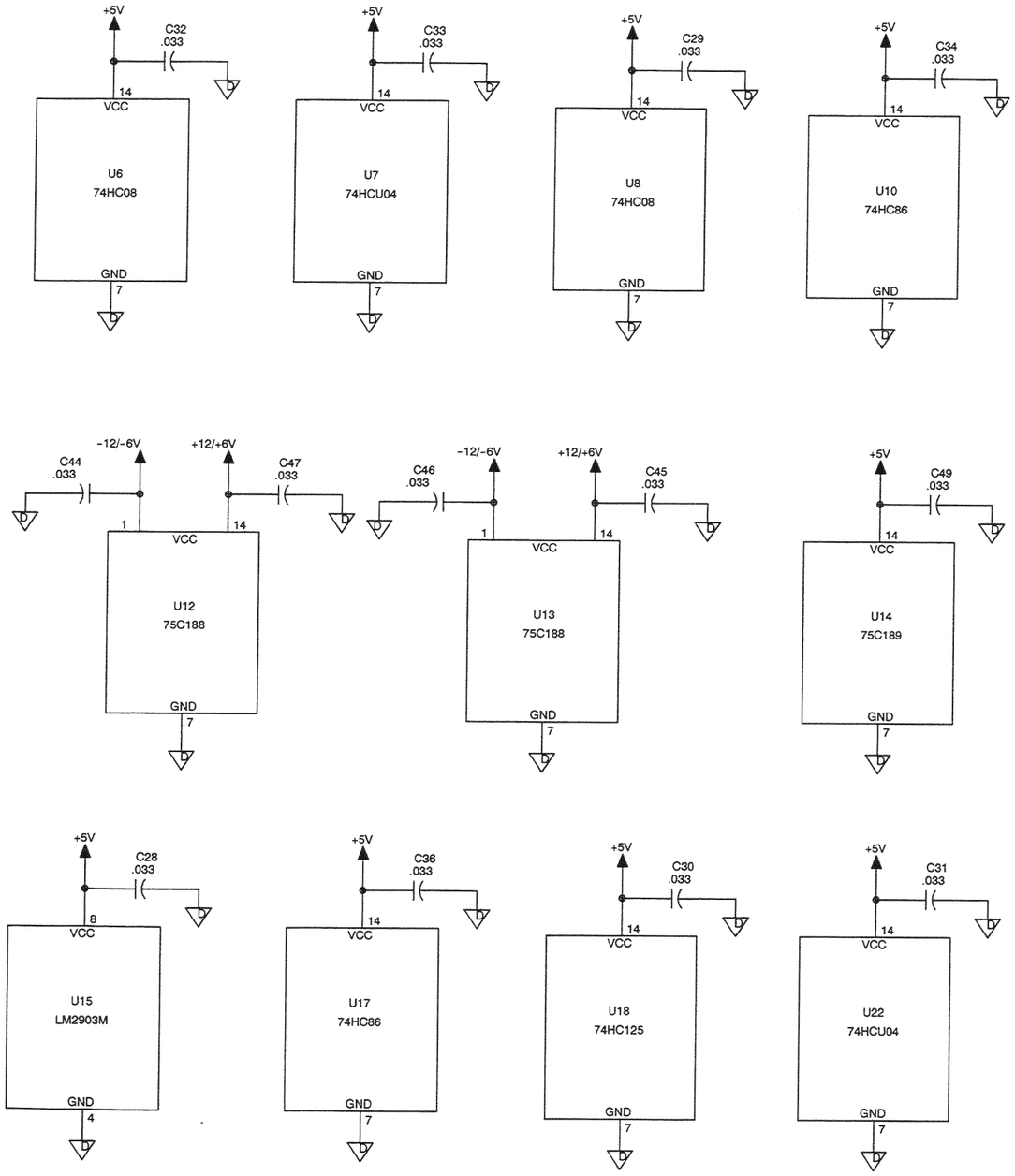
SHEET 6 OF 7

Figure 8. A1A1 Interface Assembly Schematic Diagram (10303-2281 Rev. C) (Sheet 6 of 7)

UNUSED PINS/UNUSED GATES/POWER AND GROUND CONNECTIONS

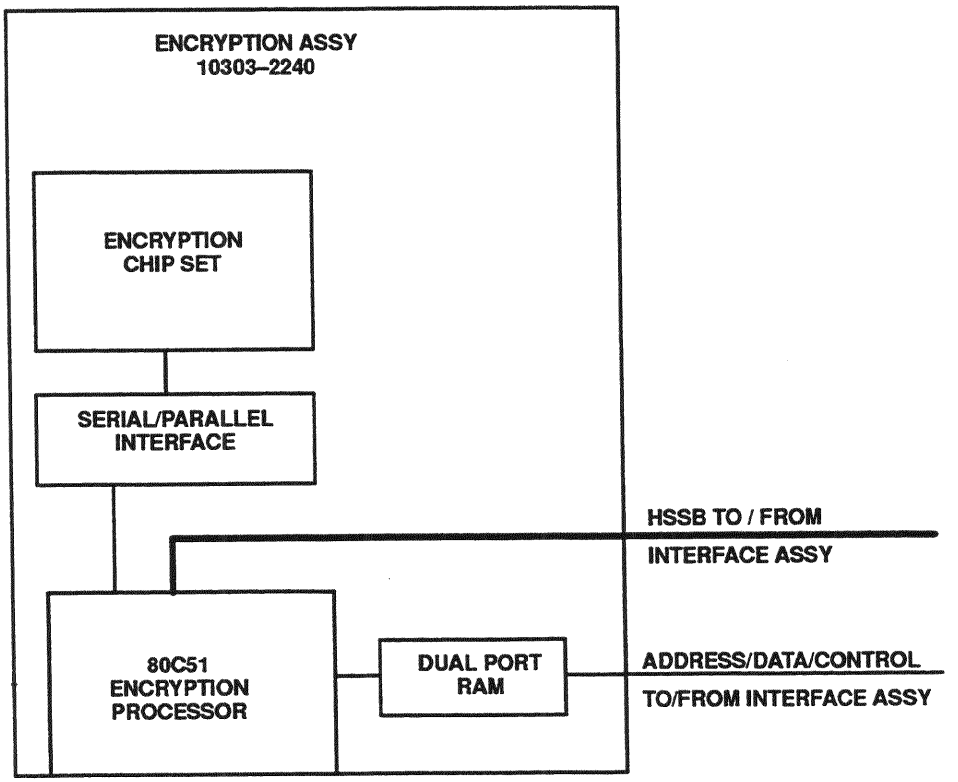




10303-2281 REVC
SHEET 7 OF 7

Figure 8. A1A1 Interface Assembly Schematic Diagram (10303-2281 Rev. C) (Sheet 7 of 7)

A1A2
RF-5170 ENCRYPTION OPTION



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A1A2 RF-5170 ENCRYPTION OPTION

1. GENERAL DESCRIPTION

The A1A2 RF-5170 Encryption Assembly, when installed, provides the receiver-transmitter with the ability to encrypt and decrypt digital data. This is accomplished through the use of a proprietary, exportable, non-linear, non-error propagating, pseudorandom key generator that is initialized by a multi-level key architecture. If the RF-5161 A3 LPC Assembly is also installed, the A1A2 RF-5170 Encryption Assembly also provides the following:

- Encrypted single-channel digital voice (LPC) traffic
- Encrypted hopping (ECCM) DTE and 800 bps voice traffic
- Analog voice security

The A1A2 Encryption Assembly cannot encrypt MIL-STD-148-141A data text messages (DTMs), also known as engineering order wires (EOWs). ALE's automatic message displays (AMDs) are also not encrypted.

The A1A2 RF-5170 Encryption Assembly is implemented in hardware as a piggy-back module that mounts to the A1A1 Interface Assembly. There is an A1A2 connector on the back of the A11 Motherboard Assembly, but it is not used in the current encryption configuration.

2. INTERFACE CONNECTIONS

The signals sent to and received by the RF-5170 Encryption Assembly are listed in table 1.

Table 1. RF-5170 Encryption Assembly Interface Connections

Connector and Pin	Signal	Comments
P2-1	+5 V	5-volt logic supply to board
P2-2	+5 V	5-volt logic supply to board
P2-3	/IWR	Interface Assembly write strobe, active low
P2-4	HSSB	Serial Data
P2-5	IA8	Interface Assembly address line 8
P2-6	/IRD	Interface Assembly read strobe, active low
P2-7	IA10	Interface Assembly address line 10
P2-8	IA9	Interface Assembly address line 9
P2-9	No Connect	
P2-10	IA11	Interface Assembly address line 11
P2-11	No Connect	
P2-12	Frame Clock	Not Used
P2-13	ID7	Interface Assembly data bit 7
P2-14	IA7	Interface Assembly address line 7
P2-15	ID6	Interface Assembly data bit 6
P2-16	IA6	Interface Assembly address line 6
P2-17	ID5	Interface Assembly data bit 5
P2-18	IA5	Interface Assembly address line 5

Table 1. RF-5170 Encryption Assembly Interface Connections (Cont.)

Connector and Pin	Signal	Comments
P2-19	ID4	Interface Assembly data bit 4
P2-20	IA4	Interface Assembly address line 4
P2-21	ID3	Interface Assembly data bit 3
P2-22	IA3	Interface Assembly address line 3
P2-23	ID2	Interface Assembly data bit 2
P2-24	IA2	Interface Assembly address line 2
P2-25	ID1	Interface Assembly data bit 1
P2-26	IA1	Interface Assembly address line 1
P2-27	ID0	Interface Assembly data bit 0
P2-28	IA0	Interface Assembly address line 0
P2-29	Test Fixture Reset	Used by test fixture to hold micro in reset
P2-30	DPRAM INT	Dual Port Ram interrupt from Interface Assembly
P2-31	AUX2	DPRAM Semaphore select from Interface Assembly
P2-32	AUX3	DPRAM chip select from Interface Assembly
P2-33	9.6 MHz	9.6-MHz system clock
P2-34	/PGM	Disables Peripheral I/O selection, Active low
P2-35	+16 V UNREG	Not used
P2-36	VPP	Flash programming voltage (12.5 V max.)
P2-37	VBATT	Not used
P2-38	Power On Reset	System reset, active high
P2-39	DGND	Supply ground return
P2-40	DGND	Supply ground return

3. TECHNICAL DESCRIPTION

Figure 1 is a functional block diagram of the A1A2 Encryption Assembly. Use this figure for reference during the following description of operation. A parts list, component location diagram, and schematic diagram for the A1A2 Encryption Assembly are included at the end of this section.

The A1A2 RF-5170 Encryption Assembly can be viewed as being composed of three separate, although not independent, functional blocks:

- Circuitry to perform the encryption and decryption process.
- Circuitry to control the encryption/decryption process and to communicate with the A1A1 Interface Assembly and the rest of the transceiver through a dual-port RAM (DPRAM), which consists of microcontroller U1, its local EPROM U10, its local RAM U11, and DPRAM U5.
- Miscellaneous logic provides address latching (U6) and I/O decoding (U7).

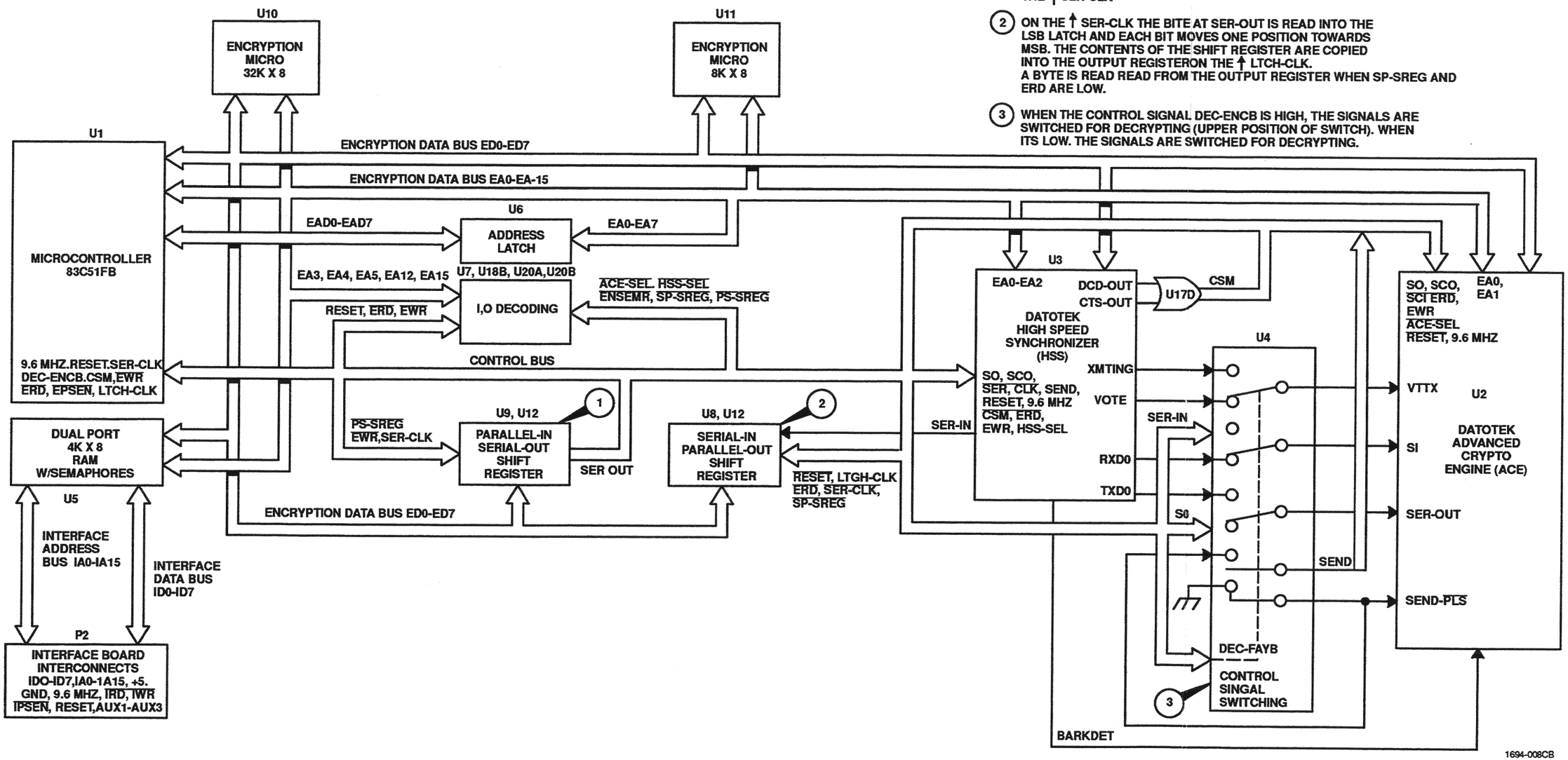

Figure 1. Digital Encryption Assembly Block Diagram

3.1 Data/Voice Encryption and Decryption Logic

Data and voice (LPC) encryption are performed by the advanced crypto engine (ACE) U2 and the high-speed synchronizer (HSS) U3. These chips, in conjunction with the parallel-in/serial-out shift register logic U9, the serial-in/parallel-out U8, and the signal routing switch U4, combine to form the encryption/decryption logic block.

When the RT-1694 is in the single-channel mode of operation (SSB), the HSS and ACE encryption chips work together as a pair. Information is transferred between the two encryption chips in serial fashion. The 83C51FB encryption microcontroller communicates with the A1A1 Interface Assembly through DPRAM U5 in 8-bit bytes. For the encryption microcontroller to send 8-bit information to the encryption chips, it must first convert each 8-bit byte into serial form before clocking it into the encryption chips. When information is received from the encryption chips, it must be converted from serial form back into 8-bit bytes. These serial-to-parallel and parallel-to-serial operations are performed by the shift registers.

In the hopping mode of operation (HOP), the HSS is not used, and the ACE is used in the parallel mode of operation. That is, 8-bit bytes are sent directly to the ACE to be encrypted or decrypted, and the resulting information is read back from the ACE as 8-bit bytes.

The signal routing switch U4 is used only in SSB operation. This switch configures some external HSS and ACE signal pins for the encryption or decryption mode of operation.

In single channel operation, there is a start-of-message crypto-sync-message of approximately 800 bits inserted before the actual encrypted data is transmitted. This translates into a single-ended throughput delay of 800 bits ÷ modem baud rate (bps). There is also an 800 bit long end-of-message crypto-sync-message transmitted at the end of every transmission. Therefore, total on-air transmission time will be increased by 1600 bits ÷ modem baud rate (bps). In hopping (ECCM) mode, encryption does not alter any timing parameters and does not increase the length of the transmission.

3.2 Serial-to-Parallel and Parallel-to-Serial Data Conversion

This section deals with the conversion of the 8-bit information format used by the Interface and Encryption microcontrollers to and from their serial information format used by the HSS and ACE encryption chips.

The parallel-in/serial-out shift register logic U9 performs two functions in SSB mode: converting parallel 8-bit data to serial data for transfer to the ACE for encryption, and converting received, parallel information to serial form for transfer to the HSS for decryption. The data to be encrypted can be digitized voice from the A3 LPC Assembly or DTE from the data port, and comes from the Interface Assembly through the DPRAM U5. Encrypted data from the HSS is sent to the Interface Assembly through the DPRAM for transmission.

The serial-in/parallel-out shift register logic U8 also performs two functions in SSB mode: converting decrypted, serial information from the ACE to parallel form for transfer to the rest of the transceiver, and converting encrypted, serial information from the HSS to parallel form for transfer to the rest of the transceiver. Decrypted data packets are sent by the Encryption Assembly's microprocessor U1 to the A1A1 Interface Assembly's microcontroller through DPRAM U5. The Interface Assembly's microcontroller then sends the decrypted data packet to the A3 LPC Assembly for conversion, or out the selected data port.

The HSS generates and recovers the crypto-synch message (CSM). The ACE performs the actual encrypting and decrypting of information. The CSM generated and recovered by the HSS is used to establish encryptor/decryptor synchronization. Synchronization is done entirely within the HSS. Encryptor/decryptor synchronization is established by means of a random seed which is generated by the transmit unit's ACE, and is sent to the receive unit's ACE as part of the CSM. The recovered random seed is combined with the master key variable, which is entered into the transceivers by the user. When the same master key and random seed are entered in both the transmitting and receiving units, the receiving unit's ACE can properly decrypt the transmitting unit's data or voice message.

4. TESTING AND ALIGNMENT

The A1A2 Encryption Assembly has no testing or alignment procedures.

5. BITE FAULTS AND TROUBLESHOOTING

Before proceeding to any specific bite fault troubleshooting procedure, perform the following steps:

a. Replace the questionable Encryption Assembly with a known good Encryption Assembly and rerun the self test. If the self test still returns an error, the problem is not the Encryption Assembly. If the self test does not return the error, remove the known good Encryption Assembly and replace it with the questionable Encryption Assembly. Rerun the self test and verify that a bite error is produced.

NOTE

If no error occurred on the second self test, the Encryption/Interface Assembly may have simply been seated incorrectly on the motherboard. If the error cannot be reproduced, rerun the self test several times to verify that the Encryption card no longer produces an error.

b. If the error is confirmed, check the reference designators listed in table 2 in the sequence that is listed.

If signals are not correct, check for shorts/opens and components that seem excessively hot. If all of the initial checks pass, proceed to subsection 5.1, Troubleshooting BITE Faults.

Table 3 is a list of self-test fault codes for the A1A2 Encryption Assembly. The tests and faults are described in greater detail in the following paragraphs.

Table 2. A1A2 Encryption Assembly Checks

Ref. Desig.	Function	What to Look For	To Correct, Check
U1-21	Clock input	9.6 MHz clock	Clock traces
U1-20	Clock output	9.6 MHz clock	U1 bad if no signal
U1-10	Reset (active high)	Pulse on power up, then logic low	U13. R17, P2-38
U1-33	ALE	Approx. 1.6 MHz clock	R1, U6, CR4, U1 may be defective
U1-35	/EA (external add)	Logic low	U10 defective or U10 bad checksum
U1-44	Vcc	+5 Vdc	Power traces
U6-1	Reset enable; address demux	Pulse on power up, then logic low	U13. R17, P2-38
U10-1	Vpp	+5 Vdc	CR1, Q1, Q2, U12, U1
U10-32	Vcc	+5 Vdc	Power traces

Table 3. A1A2 Encryption Assembly Fault Codes

Code	Fault
81	Communications fault
82	ROM fault
83	Internal RAM fault
84	External RAM fault
85	Dual-port RAM fault (Encryption side)
86	Semaphore register fault (Encryption side)
87	ACE fault
88	HSS register fault
89	Encryption loop back fault

5.1 Troubleshooting BITE Faults

5.1.1 Fault 81 – Communications Fault

This fault indicates the Interface microprocessor cannot communicate with the Encryption microprocessor U1 via U5 Dual Port RAM. Perform the following:

a. Ensure that all checks in section 5 have been performed.

b. While BITE is active, check the components listed in table 4.

c. If fault persists, replace U5.

d. If fault persists, replace U10 (flash EPROM).

e. If fault persists, replace U6 (HC573 address latch).

Table 4. Fault 81 Communications Fault Checks

Ref. Desig.	Function	What to Look For	To Correct, Check
U6-11	Latch enable add	Approximately 1.2 MHz digital signal	Open/shorted trace or defective U6
U6-12 through -19	Address 0–7	Active high and low	Traces on U6 pins 2 through 9 to U1. Check same for shorts and opens. Traces on U6 pins 12–19 to U5
U5-51	DPRAM enable right	Active pulses	U16-C and U1 pins 31 and 28
U5-50	Read/write enable	Active pulses	Trace to U1-18. Possible bad U1-19
U5-46	Output enable	Active pulses	Trace to U1-19. Possible bad U1-18
P2. All address/ data/control pins to U5.		Check for opens/shorts	

5.1.2 Fault 82 – ROM Fault

This fault indicates that the internal additive checksum test for U10 has failed. Perform the following:

a. Ensure that all checks in subsection 5 have been performed.

b. While BITE is active, check the components listed in table 5.

NOTE

Verify 0 to +5 V activity on every address and data line at U10 (A0 to A15, D0 to D7). If any of these lines do not toggle, trace it back to its source and verify that a line is connected to its source and is not shorted to anything nearby.

c. If there is no activity on any of A0 through A7, replace U6.

d. If fault continues, replace U10.

Table 5. Fault 82 – ROM Fault Checks

Ref. Desig.	Function	What to Look For	To Correct, Check
U10-22	Flash chip enable	1.6 MHz clock	R1, CR4
U10-31	Write enable	Activity high and low	Trace to U1
U10-24	Output enable	Activity high and low	CR3, trace to U1
U10-13 through -21	Data lines	Activity high and low	Traces to U1
U10-5 through -12	Address 0 through 7	Activity high and low	Traces to U6
U6-11	Latch enable add	Approximately 1.2 MHz digital signal	Open/shorted trace or defective U6
U6-12 through -19	Address 0 through 7	Activity high and low	Traces on U6 pins 2 through 9 to U1. Check same for shorts and opens.
U10-23, -25 through -29, -4	Address 8 – 14	Activity high and low	Continuity to U1
U10-2, -3	Address 15, 16	Activity high and low	U15, U15 to U1

5.1.3 Fault 83 – Internal RAM Fault

This fault indicates a problem within the U1 microprocessor. Perform the following:

a. Replace U1.

5.1.4 Fault 84 – External RAM Fault

This fault indicates a problem with external RAM U11. Perform the following:

a. Ensure that all checks in subsection 5 have been performed.

b. While BITE is active, check the components listed in table 6.

c. If there is no activity on any of A0 through A7, replace U6.

d. If fault continues, replace U11.

Table 6. Fault 84 EXTERNAL RAM Fault Checks

Ref. Desig.	Function	What to Look For	To Correct, Check
U11-29 (27)	Write enable	Activity high and low	Trace to U1-18
U11-24 (22)	Output enable	Activity high and low	Trace to U1-19
U11-22 (20)	RAM enable 1	Activity high and low	Trace to U1-31
U11-30 (28)	RAM enable 2	+5 Vdc	R34, R34 to +5 Vdc
U11-13 (11) through -15 (13) , -17 (15) through -21 (19)	RAM data lines	Activity high and low	Trace back to U1
U11 -3 (5) through -10 (11)	RAM address 0 through 7	Activity high and low	Trace back to U6
U6-11	Latch enable add	Approximately 1.2 MHz digital signal	Open/shorted trace or defective U6
U6-12 through -19	Address 0 through 7	Activity high and low	Traces on U6 pins 2 through 9 to U1. Check same for shorts and opens
U11-3 (1)	Address 14	Activity high and low	Trace back to U15-11. U15-13 to U1-7. U15-12 to U1-30.

NOTE: Pins in () for RAM P/N HM628128

5.1.5 Fault 85 – Dual-Port RAM Fault (Encryption Side)

This fault indicates a problem with dual-port RAM U5. Perform the following:

a. Ensure that all checks in section 5 have been performed.

b. While BITE is active, check the components listed in table 7. If there is no activity on any of the lines, trace that line back to its source and check for opens or shorts.

c. If fault continues, replace U5.

Table 7. Fault 85 – Dual-Port RAM Fault (Encryption Side) Checks

Ref. Desig.	Function	What to Look For	To Correct, Check
U5-52	Vcc	+ 5 Vdc	Trace to +5 source
U5-51	Enable right side	Activity high and low	Trace back to U8. Possible defective U16. Check U16 pins 8, 9, and 10
U5-46	Output enable	Activity high and low	Trace to U1-19
U5-50	Read/Write	Activity high and low	Trace to U1-18
U5-27 through -34	Data lines 0 through 7	Activity high and low	Trace to U1
U5-38 through -45	Address 0 through 7	Activity high and low	Trace to U6
U6-11	Latch enable add	9.6 MHz clock	Open/shorted trace or defective U6
U6-12 through -19	Address 0 through 7	Activity high and low	Traces on U6 pins 2 through 9 to U1. Check same for shorts and opens
U5-37, -36, -48, -47	Address 8 through 11	Activity high and low	Trace to U1

5.1.6 Fault 86 – Semaphore Register Fault (Encryption Side)

The semaphore registers are also part of the dual-port RAM U5, however, if this test fails, it means that the test for Fault 85 passed. This limits the possible causes of this fault. Perform the following:

a. Ensure that all checks in section 5 have been performed.

b. While BITE is active, check the components listed in table 8.

c. If the test is still failing, replace U5.

Table 8. Fault 86 – Semaphore Register Fault (Encryption Side) Checks

Ref. Desig.	Function	What to Look For	To Correct, Check
U5-51	Enable right side	Activity high and low	Trace back to U8. Possible defective U16. Check U16 pins 8, 9 and 10.
U5-49	Enable semaphore right	0V during BITE	Replace U7
U5-1	Enable left side	Activity high and low	Trace to P2-32
U5-3	Enable semaphore left	Activity high and low	Trace to P2-31

5.1.7 Fault 87 – ACE Fault

This fault indicates that U1 is unable to communicate with the ACE (U2), or that U2 is defective. Perform the following:

a. Ensure that all checks in subsection 5 have been performed.

b. While BITE is active, check the components listed in table 9.

c. If the fault persists, the problem is with U2. Replace U2.

d. If the fault persists, examine all pins for good solder wetting. If possible, have a trained and certified technician resolder U2. Otherwise, replace the A1A2 Encryption Assembly.

Table 9. Fault 87 – ACE Fault Checks

Ref. Desig.	Function	What to Look For	To Correct, Check
U7-15	ACE select	100 pulses during BITE	Replace U7

5.1.8 Fault 88 – HSS Register Fault

This fault indicates that U1 is unable to communicate with the HSS (U3), or that U3 is defective. Perform the following:

a. Ensure that all checks in subsection 5 have been performed.

b. While BITE is active, check the components listed in table 10.

c. If these pulses do not occur, replace U7.

d. If the pulses do occur, it indicates that HSS (U3) is not working. Replace U3.

e. If the fault persists, examine all pins for good solder wetting. If possible, have a trained and certified technician resolder U2. Otherwise, replace the A1A2 Encryption Assembly.

Table 10. Fault 88 – HSS Register Fault Checks

Ref. Desig.	Function	What to Look For	To Correct, Check
U7-14	HSS chip select	Approximately 10 high to low pulses	U7 decoder

5.1.9 Fault 89 – Encryption Loop Back Fault

This test encrypts and then decrypts an internally generated bit stream. A fault indicates a possible problem in any of the following ICs: U2, U3, U4, U8, or U9. Perform the following:

a. Look for four low to high transitions on CSM (U12-11). If there are at least two transitions, then the HSS (U3) is working properly, but not decrypting properly. This indicates a possible problem with U4 (replace). If there were two transitions on U12-11 and replacing U4 did not solve the problem, replace U3 (HSS).

b. If there are no transitions on U12-11, check for clock activity on U2 (ACE) pin 63. If there is no clock activity, replace U13. If there are transitions on this pin, check for data transitions on U2 pin 60. If there is no activity on this line, replace the ACE (U2).

c. If there are four transitions on U12-11, but the test still fails, verify that all Encryption Microprocessor's (U1) data bus lines are correctly connected to U8 pins Q1 → Q8. If they are, verify data activity on U8 pin 14. If there is no activity, replace U8.

d. If the test is still failing, replace U4, U8, and U9.

e. If the test is still failing, replace U2 and U3.

5.2 Troubleshooting Operational Faults

The following describe problems and solutions for operational faults that occur during troubleshooting.

Problem: Receive radio outputs no decrypted data, or random data, or in the case of LPC traffic, normal radio noise is not muted.

Solution: Make sure that the following are set up the same way for both transmitter and receiver:

- The selected encryption key
- The value of that encryption key
- Settings of currently selected data preset (that is, baud rate, interleaving, modem type, and so on). The only mismatch possible would be one radio selecting the async data port and the other selecting the async remote port.
- The port settings of the ports selected in the data preset. If the selected ports are asynchronous, their baud rates may differ, but number of bits, number of stop bits, and parity must be identical.

Problem: On a perfect channel Receive radio outputs mostly decrypted data, but with some bit errors.

Solution: This problem may not be due to the Encryption Option. Instead, the problem lies in the Signal Processor. Refer to the A4 Signal Processor Assembly's troubleshooting section.

Problem: Hopping will not achieve initial synchronization.

Solution: Hopping initial synchronization uses no encrypted data. therefore, the problem lies elsewhere. Refer to the A4 Signal Processor Assembly's troubleshooting section under hopping.

Problem: Analog Voice Security (AVS) is unintelligible.

Solution: Make sure the same encryption keys are selected and that their values are identical. If they are, refer to the A3 LPC Assembly's troubleshooting section.

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6. PARTS LIST, COMPONENT LOCATION DIAGRAM, AND SCHEMATIC DIAGRAM

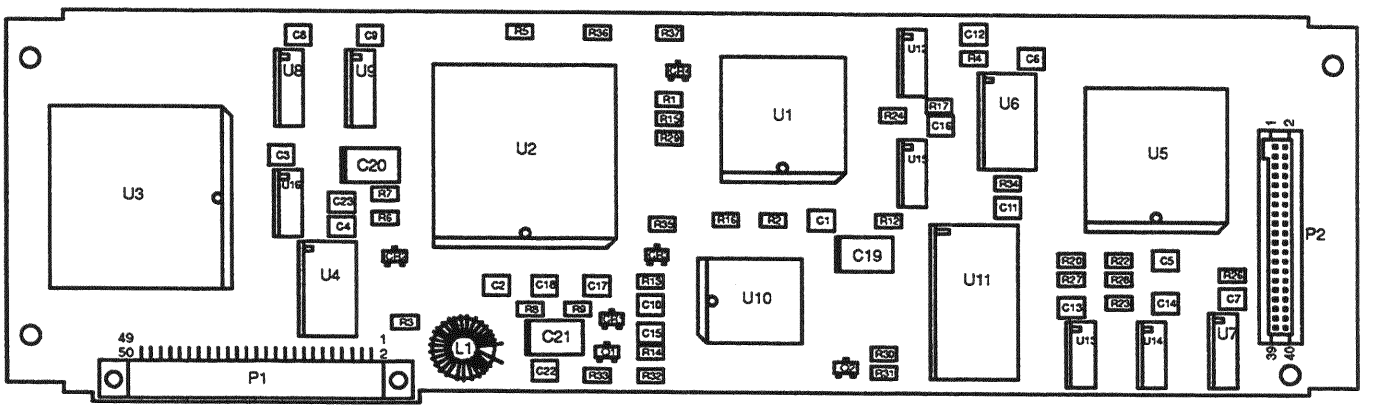
Table 11 is the parts list, figure 2 is the component location diagram, and figure 3 is the schematic diagram for the A1A2 Encryption Assembly.

Table 11. Encryption Assembly Parts List (10303-2240 Rev. F)

Ref. Desig.	Part Number	Description
C1	C13-0107-473	CAP .047 UF 250V CER SMC
C2	C13-0107-473	CAP .047 UF 250V CER SMC
C3	C13-0107-473	CAP .047 UF 250V CER SMC
C4	C13-0107-473	CAP .047 UF 250V CER SMC
C5	C13-0107-473	CAP .047 UF 250V CER SMC
C6	C13-0107-473	CAP .047 UF 250V CER SMC
C7	C13-0107-473	CAP .047 UF 250V CER SMC
C8	C13-0107-473	CAP .047 UF 250V CER SMC
C9	C13-0107-473	CAP .047 UF 250V CER SMC
C10	C13-0107-473	CAP .047 UF 250V CER SMC
C11	C13-0107-473	CAP .047 UF 250V CER SMC
C12	C13-0107-473	CAP .047 UF 250V CER SMC
C13	C13-0107-473	CAP .047 UF 250V CER SMC
C14	C13-0107-473	CAP .047 UF 250V CER SMC
C15	C13-0107-473	CAP .047 UF 250V CER SMC
C16	C13-0107-473	CAP .047 UF 250V CER SMC
C19	C36-0016-336	CAP, 33UF 16V TANT
C20	C36-0016-336	CAP, 33UF 16V TANT
C23	C13-0107-473	CAP .047 UF 250V CER SMC
CR1	D20-0005-001	DIODE, SOT-23
CR2	D20-0005-001	DIODE, SOT-23
CR3	D20-0005-001	DIODE, SOT-23
CR4	D20-0005-001	DIODE, SOT-23
P2	J46-0115-040	CONN, 40 PIN MALE
Q1	Q02-2907-101	XSTR SS/GP PNP MMBT2907A
Q2	Q12-2222-101	XSTR NPN SWG SM SS/GP
R1	R85-0004-334	RES 22.1K 1% 1/8W FLM
R2	R85-0004-251	RES 3320 1% 1/8W
R3	R85-0004-401	RES 100K 1% 1/8W FLM
R4	R85-0004-001	RES, 10 1% 1/8W CHIP
R5	R85-0004-301	RES 10K 1% 1/8W FLM
R6	R85-0004-251	RES 3320 1% 1/8W
R7	R85-0004-334	RES 22.1K 1% 1/8W FLM
R10	R85-0004-000	RES ZERO OHM 1/8W FILM
R11	R85-0004-000	RES ZERO OHM 1/8W FILM
R12	R85-0004-001	RES, 10 1% 1/8W CHIP
R13	R85-0004-001	RES, 10 1% 1/8W CHIP
R14	R85-0004-401	RES 100K 1% 1/8W FLM
R15	R85-0004-266	RES,4.75K 1% 1/8W CHIP

Table 11. Encryption Assembly Parts List (10303-2240 Rev. F) (Cont.)

Ref. Desig.	Part Number	Description
R16	R85-0004-251	RES 3320 1% 1/8W
R17	R85-0004-201	RES 1000 1% 1/8W FLM
R24	R85-0004-101	RES 100 1% 1/8W FLM
R27	R85-0004-101	RES 100 1% 1/8W FLM
R28	R85-0004-101	RES 100 1% 1/8W FLM
R29	R85-0004-001	RES, 10 1% 1/8W CHIP
R30	R85-0004-251	RES 3320 1% 1/8W
R31	R85-0004-301	RES 10K 1% 1/8W FLM
R32	R85-0004-266	RES,4.75K 1% 1/8W CHIP
R33	R85-0004-158	RES 392 1% 1/8W FLM
R34	R85-0004-000	RES ZERO OHM 1/8W FILM
R35	R85-0004-401	RES 100K 1% 1/8W FLM
R36	R85-0004-401	RES 100K 1% 1/8W FLM
R37	R85-0004-401	RES 100K 1% 1/8W FLM
U1	10181-8017	PROG. TN 83C51FA PLCC MIC
U2	10075-1207	ADVANCED CRYPTO ENGINE
U3	10075-1206	HIGH SPEED SYNCHRONIZER
U4	I01-5000-241	IC, OCTAL BUFFER, 74HC241
U5	I26-0032-001	IC,IDT1342
U6	I01-5000-573	8-BIT LATCH (74HC573DW)
U7	I01-5000-138	3 TO 8 DECODER (74HC138D)
U8	I01-5000-595	IC, 8-BIT SHIFT REG.
U9	I01-5000-165	IC 74HC165 SHIFT REG SOIC
U10	I25-0033-006	IC, 128K X 8 FLASH EPROM
U11	I26-0021-012	IC RAM HM62256LFPI-15T
U12	I01-5000-032	IC 74HC32AD PLSTC CMOS
U13	I01-5000-004	HEX INVERTER (74HC04D)
U14	I01-5000-008	IC 74HC08AD PLSTC CMOS
U15	I01-5000-008	IC 74HC08AD PLSTC CMOS
U16	I01-5000-000	QUAD NAND-GATE (74HC00D)



NOTE: The following parts are not used. They are for future expansion: P1, C21, C22, L1, R8, R9, R20, R22, R23, and R26.

Figure 2. A1A2 Encryption Assembly Component Location Diagram (10303-2240 Rev. A)

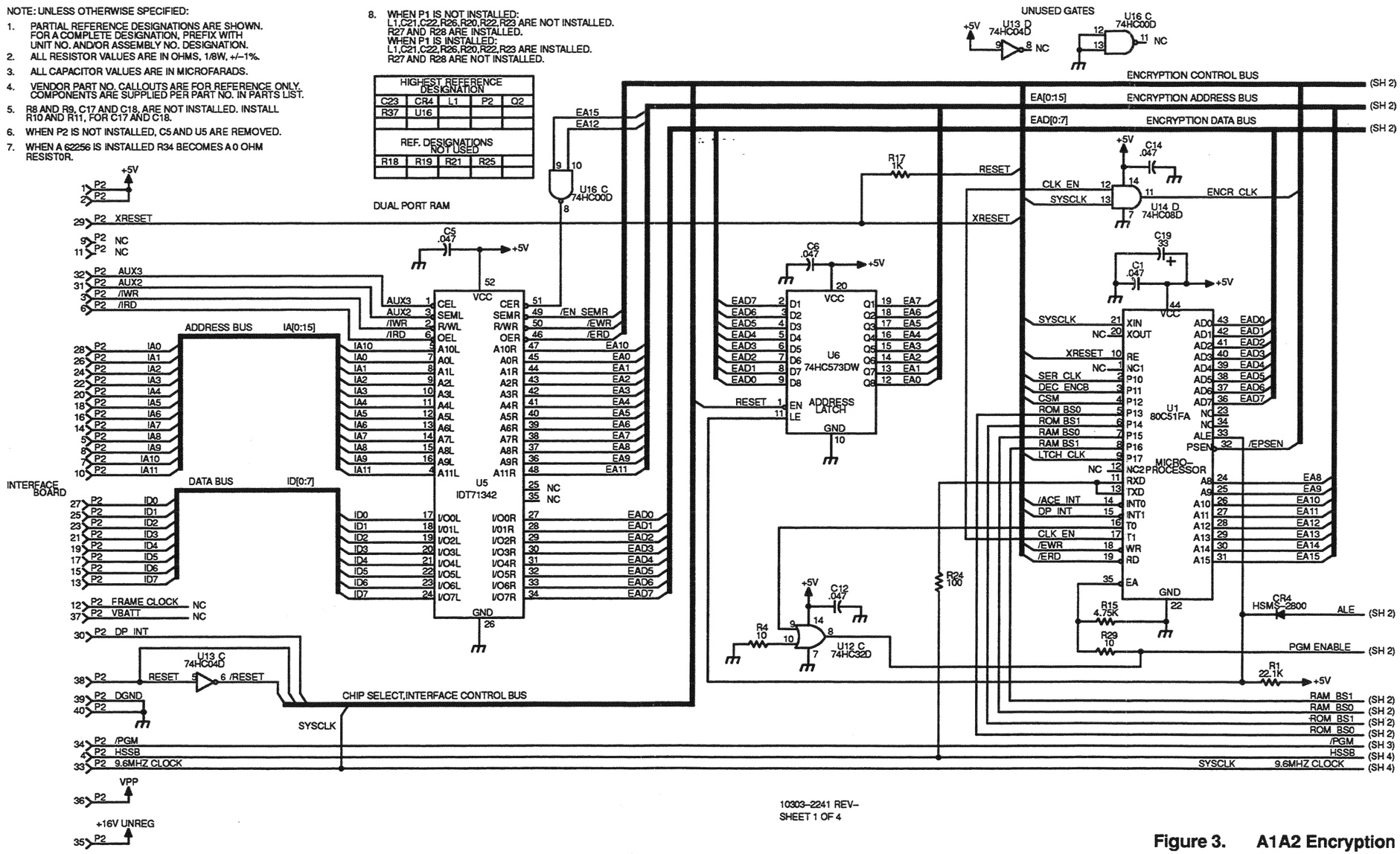
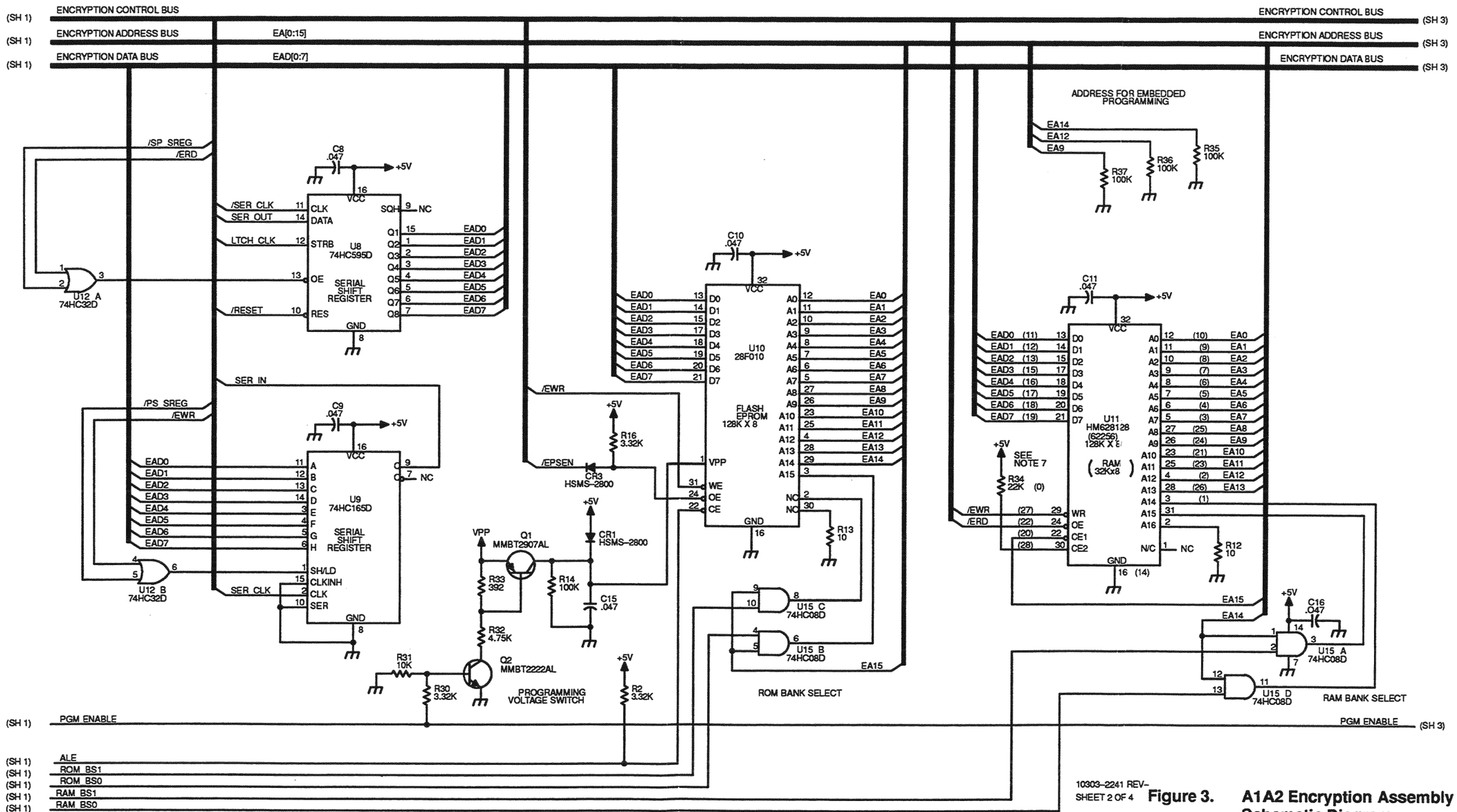
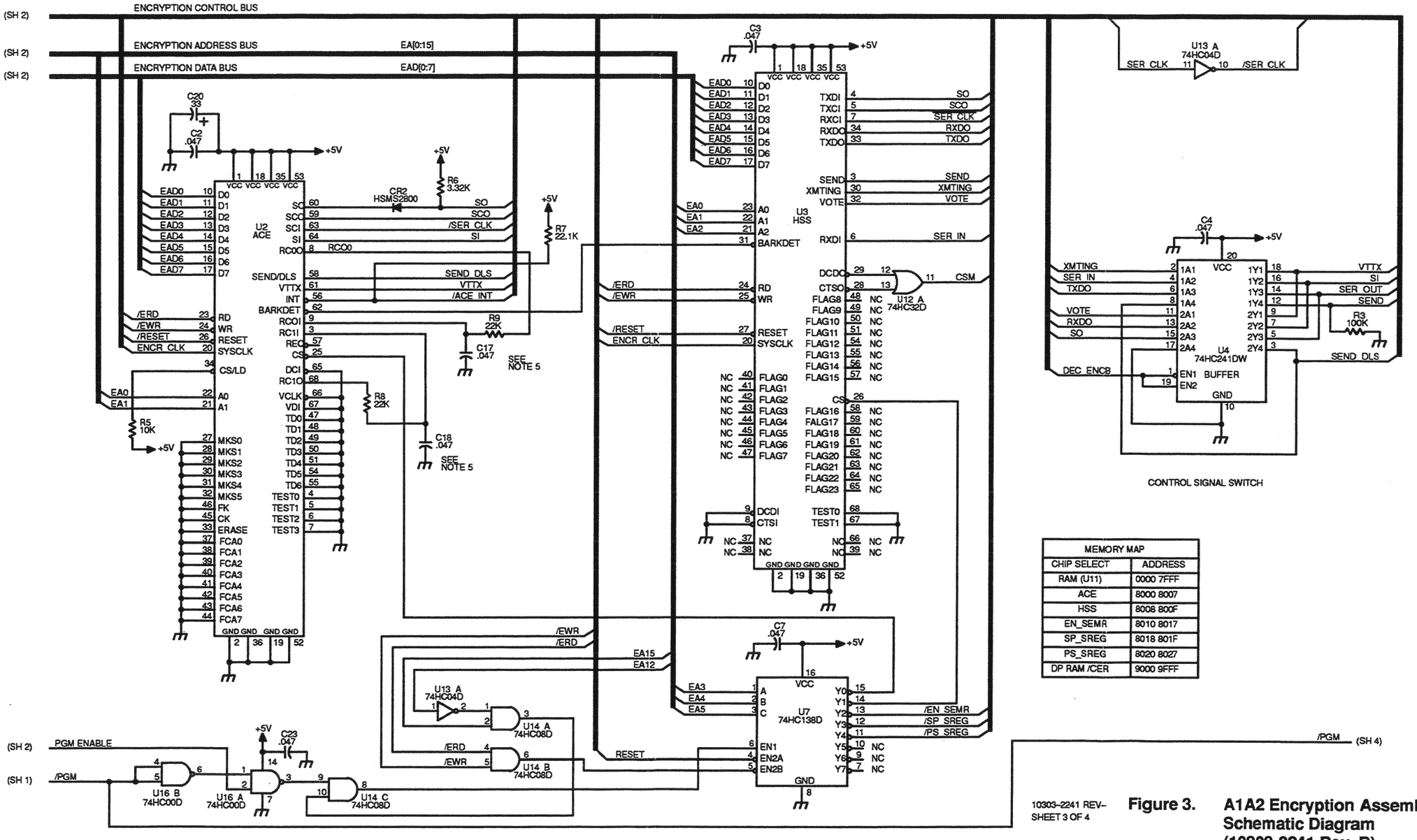


Figure 3. A1A2 Encryption Assembly Schematic Diagram (10303-2241 Rev. B) (Sheet 1 of 4)



10303-2241 REV–
SHEET 2 OF 4

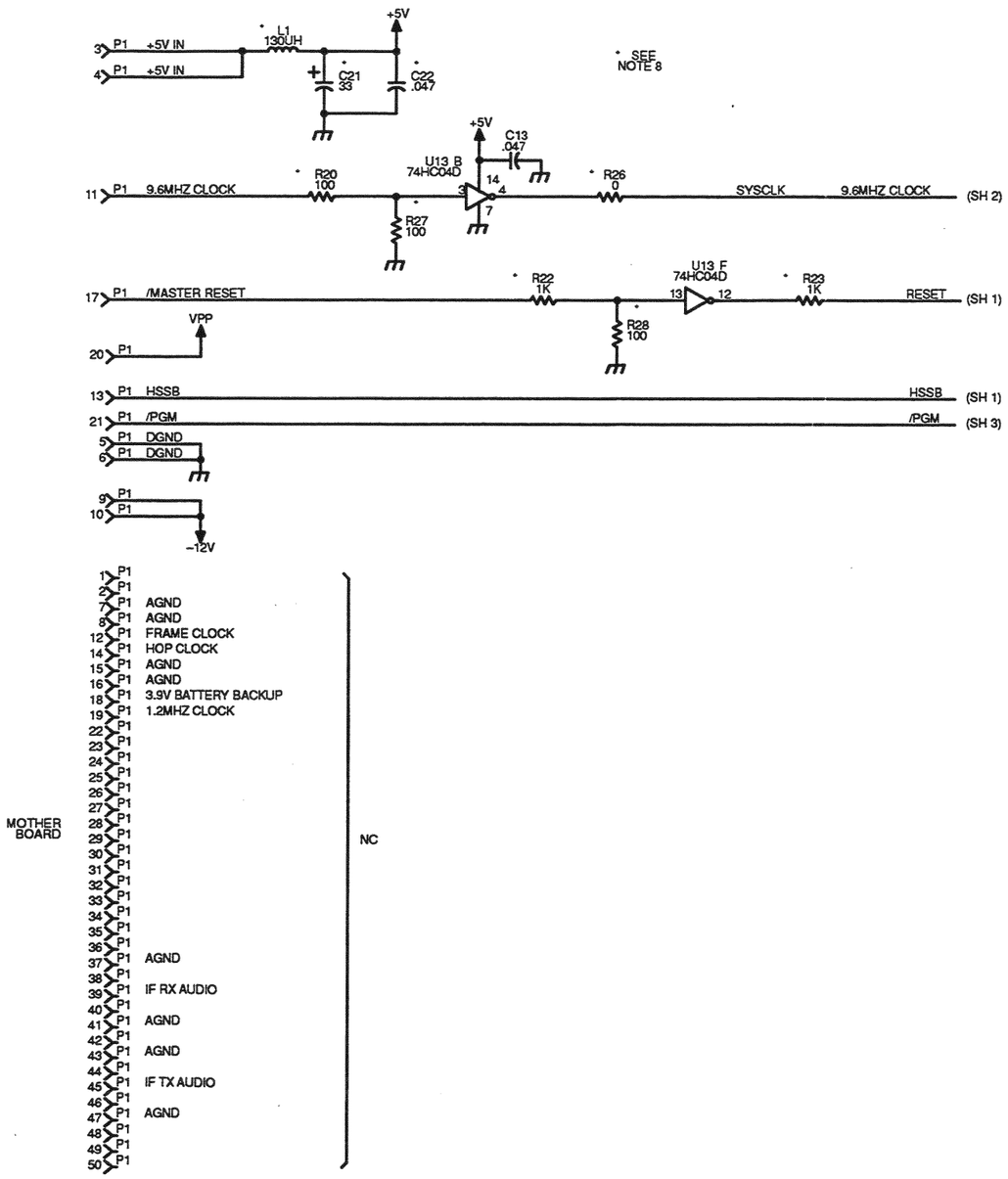
Figure 3. A1A2 Encryption Assembly Schematic Diagram (10303-2241 Rev. B) (Sheet 2 of 4)



MEMORY MAP	
CHIP SELECT	ADDRESS
RAM (U11)	0000 7FFF
ACE	8000 8007
HSS	8008 800F
EN_SEMR	8010 8017
SP_SREG	8018 801F
PS_SREG	8020 8027
DP RAM /CER	9000 9FFF

10303-2241 REV-
SHEET 3 OF 4

Figure 3. A1A2 Encryption Assembly Schematic Diagram (10303-2241 Rev. B) (Sheet 3 of 4)



EPROM MEMORY BANKS			
EA0–EA15	ROM BS1	ROM BS0	EPROM ADDRESS
0–7FFF	X	X	0–7FFF
8000–FFFF	0	0	0–7FFF
8000–FFFF	0	1	8000–FFFF
8000–FFFF	1	0	10000–17FFF
8000–FFFF	1	1	18000–1FFFF

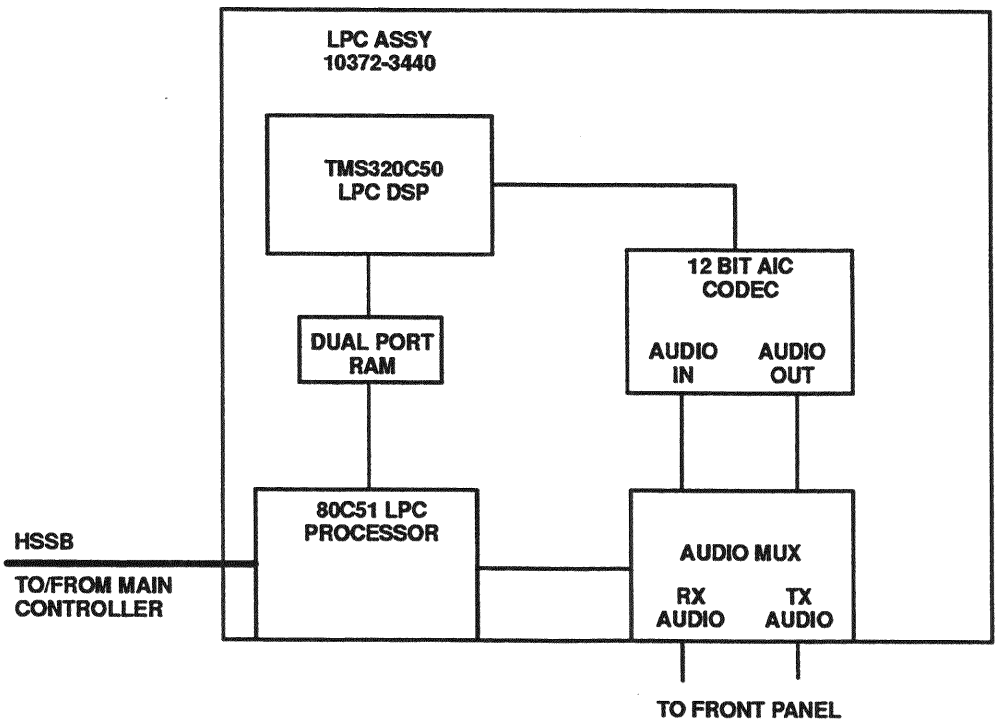
RAM MEMORY BANKS			
EA0–EA15	RAM BS1	RAM BS0	RAM ADDRESS
0–7FFF	X	X	0–3FFF
8000–FFFF	0	0	0–3FFF
8000–FFFF	0	1	4000–7FFF
8000–FFFF	1	0	8000–BFFF
8000–FFFF	1	1	C000–FFFF

10303-2241 REV–
SHEET 4 OF 4

Figure 3. A1A2 Encryption Assembly Schematic Diagram (10303-2241 Rev. B) (Sheet 4 of 4)

A3
LPC OPTION

RF-5161-01 DIGITAL VOICE OPTION OR RF-5170 ANALOG VOICE SECURITY OPTION



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A3 LPC OPTION
(RF-5161-01 DIGITAL VOICE OPTION OR RF-5170 ANALOG VOICE SECURITY OPTION)

1. GENERAL DESCRIPTION

The A3 LPC Assembly (10372-3440) option is factory configured as either the RF-5161-01 Digital Voice (DV), and/or the RF-5170 Analog Voice Security (AVS) options, per customer requirement. The RF-5161-01 DV Option enables a user to send secure-voice transmissions using forward error correction (FEC) to another AN/PRC-138 System with similar equipment. The RF-5161-01 DV Option requires the internal 39-Tone High-Speed Modem. With the addition of the RF-5170 Analog Voice Security, a higher level of security can be added.

The RF-5170 AVS option provides secure-voice scrambling to the TX audio in both the frequency domain and time domain. AVS mode provides secure voice transmission over a longer distance than Digital Voice, but is less resistant to channel interference.

2. INTERFACE CONNECTIONS

Table 1 describes the signals A3 LPC Assembly input/output signals.

Table 1. A3 LPC Assembly Interface Connections

Connector and Pin	Signal	Comments
P1-1	+16V	System +16 volt signal (+16 Vdc)
P1-2	–12V	System –15 volt signal (–12 Vdc)
P1-3	NC	No connection
P1-4	NC	No connection
P1-5	NC	No connection
P1-6	NC	No connection
P1-7	+5V	System +5 volt signal (+5 Vdc)
P1-8	+5V	System +5 volt signal (+5 Vdc)
P1-9	/PGM	System FLASH EPROM Program Enable
P1-10	NC	No connection
P1-11	NC	No connection
P1-12	NC	No connection
P1-13	NC	No connection
P1-14	NC	No connection
P1-15	NC	No connection
P1-16	NC	No connection
P1-17	NC	No connection
P1-18	NC	No connection
P1-19	NC	No connection
P1-20	NC	No connection

Table 1. A3 LPC Assembly Interface Connections (Cont.)

Connector and Pin	Signal	Comments
P1-21	AGND	System analog ground (0 Vdc)
P1-22	AGND	System analog ground (0 Vdc)
P1-23	DGND	System digital ground (0 Vdc)
P1-24	DGND	System digital ground (0 Vdc)
P1-25	TX AUDIO	LPC Audio In
P1-26	FRAME CLOCK	5/0 V, 22.5 ms clock
P1-27	HOP CLOCK	5/0 V, 50 ms clock
P1-28	NC	No connection
P1-29	9.6 MHZ	5/0 V, CMOS Square Wave
P1-30	NC	No connection
P1-31	1.2 MHZ	5/0 V, CMOS Square Wave
P1-32	POR	5/0 V, active high
P1-33	NC	No connection
P1-34	HSSB	5/0 V, Serial Data
P1-35	NC	No connection
P1-36	NC	No connection
P1-37	NC	No connection
P1-38	NC	No connection
P1-39	NC	No connection
P1-40	NC	No connection
P1-41	NC	No connection
P1-42	NC	No connection
P1-43	NC	No connection
P1-44	NC	No connection
P1-45	NC	No connection
P1-46	NC	No connection
P1-47	RX AUDIO	LPC Audio Out
P1-48	NC	No connection
P1-49	AGND	System analog ground (0 Vdc)
P1-50	NC	No connection
J1-1	TMS	JTAG test mode select
J1-2	–TRST	JTAG test reset

Table 1. A3 LPC Assembly Interface Connections (Cont.)

Connector and Pin	Signal	Comments
J1-3	TDI	JTAG test data input
J1-4	DGND	System digital ground (0 Vdc)
J1-5	+5V	System +5 volt signal (+5 Vdc)
J1-6	NC	No connection (used to key connector)
J1-7	TDO	JTAG test data output
J1-8	DGND	System digital ground (0 Vdc)
J1-9	TCK	JTAG test clock (CMOS input)
J1-10	DGND	System digital ground (0 Vdc)
J1-11	TCK	JTAG test clock (CMOS input)
J1-12	DGND	System digital ground (0 Vdc)
J1-13	EMU0	Emulation pin 0
J1-14	EMU1	Emulation pin 1

3. TECHNICAL DESCRIPTION

This subsection provides component-level theory of operation for the A3 LPC Assembly. This option is designed to provide both digital and analog voice security over an HF communication link. Figure 1 shows the data/voice path for LPC mode, and figure 2 shows the data/voice for AVS mode.

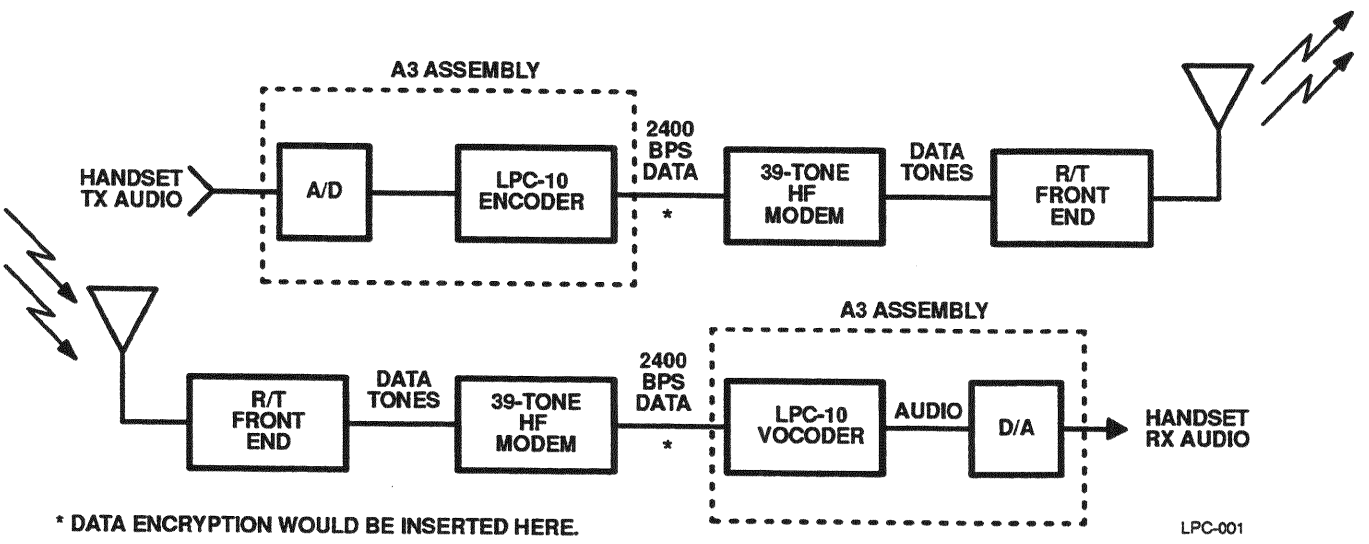


Figure 1. LPC Mode Data/Voice Path Block Diagram

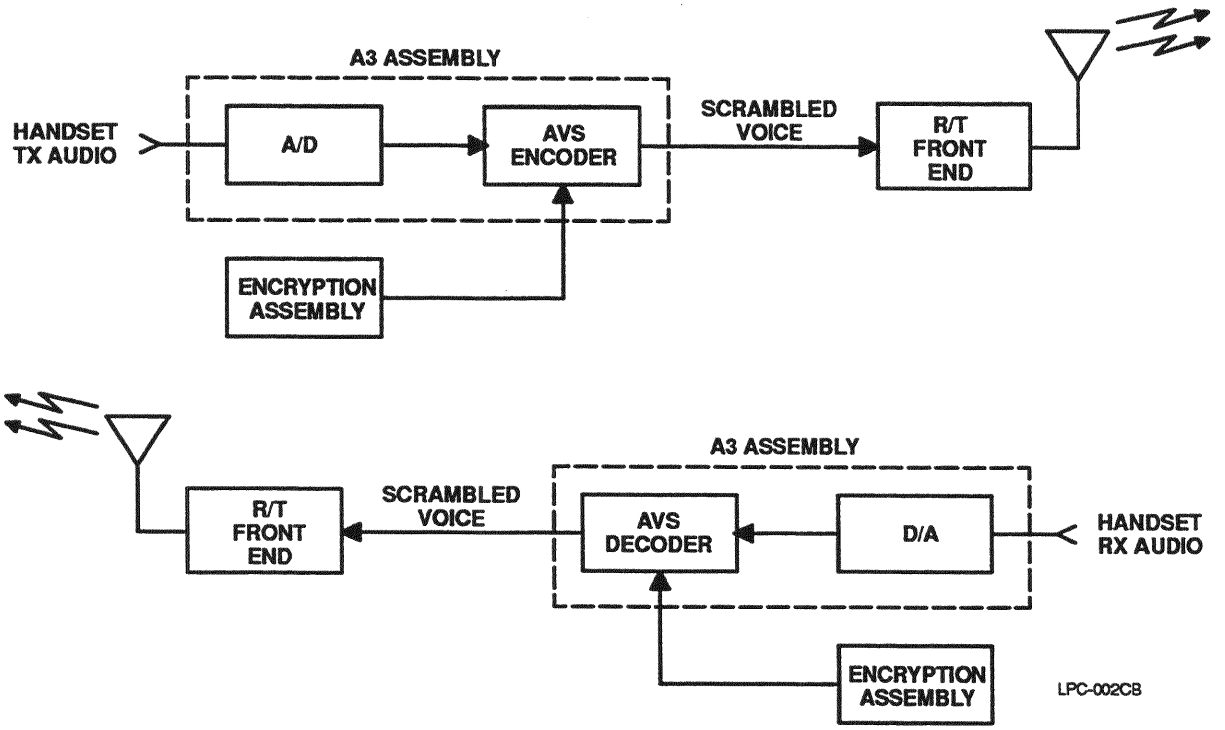


Figure 2. AVS Mode Data/Voice Path Block Diagram

3.1 Modes of Operation

The following subsections describe the four modes of operation supported by the A3 LPC Assembly.

3.1.1 DV Mode

Digital Voice (DV) mode uses the United States government's LPC-10 version 52 vocoder (voice coder) algorithm. This algorithm reduces the amount of information transmitted. For example, if speech is sampled at an 8 kHz rate and contains 12 bits of resolution, a data rate of 96,000 bits per second (bps) would result. DV is used to encode (digitally reduce the effective data rate) of speech for narrow-band communications (3 kHz). The model encodes pitch, energy gain, voicing decisions, and the 10 filter coefficients of an all-pole filter into a 54 bit data frame. The LPC-10 model generates output comparable to an all-pole filter being excited by a gain-controlled periodic pulse train signal source (if voiced), or by a gain-controlled white noise source (if un-voiced). The process of converting a speech sample into 2400 bps model parameter data bits is called *analysis*. The reverse process of converting 2400 bps model parameter data bits into speech samples is called *synthesis*.

3.1.2 Encrypted DV Mode

Encrypted DV also operates using the LPC-10 vocoder algorithm. The LPC-10 data is sent to the encryption module where it is encrypted before being sent to or received from the modem module. Each encryption key allows the user to communicate with radios also using encryption and the same encryption key.

3.1.3 AVS Mode

Analog Voice Security (AVS) does not provide the same level of voice security as Digital Voice. However, AVS has greater range over HF than DV because AVS does not require the use of an HF modem. AVS uses digital signal processing to scramble both the frequency and timing of the speech signal without using a modem preamble for synchronization. The input encryption key is used to scramble 24 frequency bits with a fixed delay through each filter. Operational range of AVS is limited only by radio signal propagation conditions, and is much less sensitive to propagation phase distortion, amplitude distortion, and channel interference.

3.1.4 RWAS Mode

In this mode, the LPC Module performs Robust Wakeup/Active Squelch (RWAS) waveform detection and generation. The RWAS waveform is used to provide the RT-1694/ PRC-138 with a reliable HF squelch capability, a reliable retransmit capability and a power-saving standby mode of operation. Based on the 75 bps Serial Tone modem waveform, the RWAS waveform can provide these capabilities in negative signal-to-noise ratio conditions. In addition, the RWAS waveform is user-addressable via the RWAS Key input which allows selection of 100 currently supported RWAS waveform variations for both security and networking considerations.

3.2 LPC Circuit Description

The following subsections provide an A3 LPC Assembly circuit description. While following this description, see figure 3 and figure 5.

3.2.1 83C51 Microcontroller

The 83C51 microcontroller (U1) is an eight bit processor with the following characteristics:

- 8-bit internal and external data bus
- 16-bit address bus
- Multiplexed address and data bus
- Configurable input and output port pins
- High speed serial port
- Two external interrupts
- Internal mask ROM

Because the lower eight address bus lines serve a dual purpose with the eight data bus lines, an external address latch (U2) is required. The 83C51 runs its application code from FLASH EPROM U3. The 83C51 also requires a portion of external dual-port RAM U4. Additionally, the 83C51 controls the TMS320C50 reset and hold by using latch U9. This reset control downloads code into the TMS320C50 for BITE and 16 bit FLASH re-programming operation. Finally, the 83C51 controls audio switch U23 to disable audio I/O and DV squelch. Software on the 83C51 uses the FRMCLK interrupt from interface connector P9. This clock is used in DV modes to interface data to the modem/encryption card at a 22.5 msec data rate, which is the frame rate for the 39-tone transmission for the LPC Digital Voice format. The high speed serial bus (HSSB) is used for inter-processor communication and data traffic with other modules in the radio.

3.2.2 83C51 FLASH Circuitry

The 83C51 processor U1 contains a Harris-proprietary FLASH reprogramming algorithm inside its internal mask. On power-up and by command from the HSSB, the 83C51 uses this internal code to reprogram external FLASH EPROM U3. U1 pin 35 at a logic 1 indicates that the 83C51 is running this code. Also, -PRGMEN must be at logic 0 and the VPP circuit must be on (Q1 ON and Q2 ON) for FLASH reprogramming.

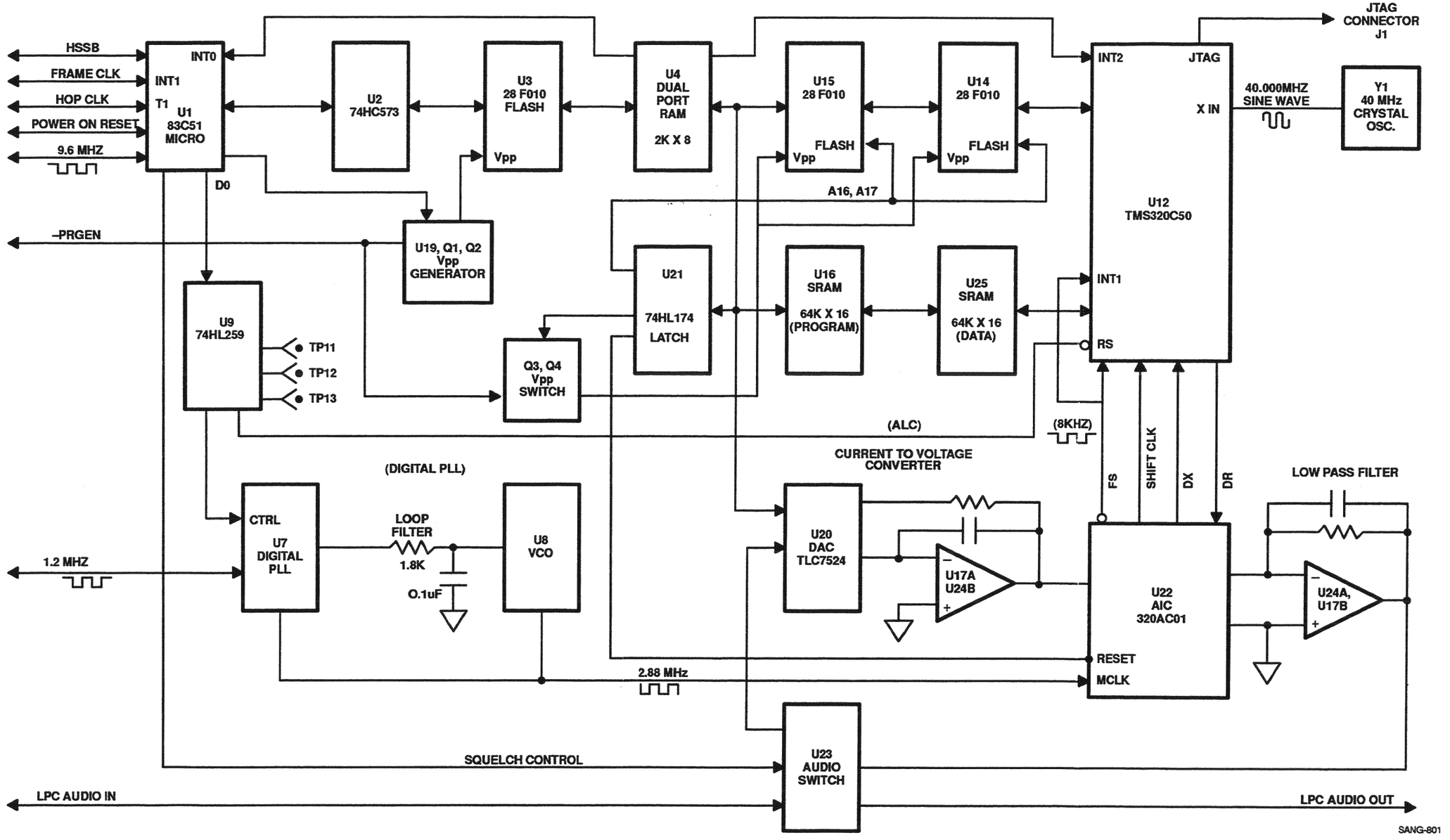


Figure 3. RF-5161-01 Digital Voice Option Functional Block Diagram

3.2.3 Sample Clock PLL

The 83C51 processor programs the digital Phase Locked Loop (PLL) to 2.88 MHz, locking the analog-to-digital (A/D) and digital-to-analog (D/A) sample clocks to the system's 1.2 MHz clock. This allows the sample clock to be as precise as the radio's internal reference. The interface to the digital PLL (U7) is a serial interface and is programmed using the serial port pins of the 83C51 processor.

3.2.4 83C51/320 Communication

Communication between 83C51 (U1) and TMS320C50 (U12) is accomplished using a 2k x 8 bit static dual-port RAM. The processors communicate using hardware interrupts. The 83C51 is interrupted through U1 pin 14, while the TMS320C50 is interrupted through U12 pin 39. The dual-port RAM (U4) identifies that the TMS320C50 is busy by checking U4 pin 49. The 83C51, however, does not have an external ready line, so latch U6B is used along with some 83C51 port pins to accomplish dual-port arbitration on the 83C51 side. If a collision occurs while the 83C51 is trying to access dual port, a busy signal is generated by U6B. The 83C51 then detects the busy signal in software (8031DPBUSY logic 1), clears (-8031DPBUSYCLR logic 0), and retries the access until successful.

3.2.5 TMS320C50 DSP

The TMS320C50 is a digital signal processor with the following features:

- 16-bit non-multiplexed address and data bus
- Four external hardware interrupts
- Two synchronous serial ports
- On-board program/data RAM
- On-board boot code ROM

The TMS320C50 is a general purpose digital signal processor that is used to implement LPC-10, AVS, and RWAS through the use of software. This processor executes code at a 50 nS cycle time from an external program 64k x 16, 15 nS stored in static RAM (U16). Code is downloaded from slow FLASH (U14 and U15) into this high speed static RAM to execute at the 50 nS cycle rate. Also, there is an external 64k x 16 static RAM in data space for additional data storage. The multiplying DAC (U20) is in the I/O space of the TMS320C50 for scaling the transmit microphone audio before sampling by the Analog Interface Chip (AIC U22). The address mapping latch (U21) is in I/O space and is used for bank selecting FLASH banks during code downloading, local FLASH Vpp program enabling, TMS320C50 boot select, and AIC reset control.

3.2.6 TMS320C50 FLASH Circuitry

The TMS320C50 DSP processor contains an internal boot loader that allows the TMS320C50 to boot from dual-port RAM (U4). On command from the main controller, the 83C51 resets the TMS320C50 and loads a 16 bit monitor from the 83C51 FLASH (U3). After reset is removed, the TMS320C50 can erase and reprogram U14 and U15 through the high speed serial bus to the external remote terminal. Data packets are transferred from the interface, main controller, and LPC 83C51 through the High-Speed Serial Bus (HSSB). The 83C51 passes FLASH data through dual port RAM (U4) to the TMS320C50 using dual-port interrupt acknowledgments. For FLASH erasure and reprogramming to be functional, the signal 320VPPCTL on inverter U10 pin 10 must be at a logic 1. This implies that Q3 and Q4 are both ON, applying +12.5 V to U14 and U15.

3.2.7 Audio Circuitry

Analog-to-digital and digital-to-analog conversion is accomplished by the AIC (U22). This device contains a serial 14 bit A/D converter and frequency controllable bandpass anti-alias filters. Transmit speech samples are transferred from the AIC to the internal serial port of the TMS320C50. Also, the AIC contains a serial 14 bit D/A and a frequency controllable reconstruction low pass filter. The sample rates for the A/D and D/A are a function of the PLL's 2.88 MHz clock (U7 and U8). The 2.88 MHz clock is divided down by an internal programmable counter inside the AIC to generate the sample clock signal (U22 pin 12). The sample rate on this pin is 8 kHz in DV mode and 7.2 kHz in AVS mode.

3.2.7.1 Transmit Audio Path

Transmit audio enters the receiver-transmitter's handset mic and is converted from a nominal level of 1.4mV (3.95 mV_{p-p}) to approximately +0.32 V (0.91V_{p-p}) on the A10 Motherboard Assembly. This audio enters the A3 LPC Vocoder Assembly through interface connector J9. Transmit audio enters the LPC Vocoder Assembly through the 83C51-controlled audio switch if DV is enabled and is not squelched. Audio is then scaled by the multiplying DAC (U20 and U17). Transmit audio is then level shifted by U24 to be biased at +2.5 volts before being sampled by U22. Note that the transmit audio signal must not exceed +3 Vpp at U22 pin 26 or the signal will be clipped. In DV mode only, the multiplying DAC (U20) is used to perform continuous Automatic Level Control (ALC) to ensure that DV does not clip. Clipping severely degrades DV voice quality.

3.2.7.2 Receive Audio Path

Receive audio is generated by the AIC (U22). Audio is biased at approximately +2.5 volts after leaving U24 pin 1. Capacitor C58 is used to bias the receive signal about ground. The output signal output level is controlled in software by the TMS320C50. The audio switch (U23) is used for receive squelch. In DV, this switch is closed during a transmission, as well as when actively receiving an LPC signal. In AVS mode this switch is always closed. The audio switch is open while not actively receiving a DV message, or if AVS and DV are disabled.

3.2.8 Voltage Generation

The A3 LPC Vocoder Assembly generates several signals and sends them to the interface connector. Refer to table 2.

Table 2. Signals Generated by the A3 LPC Vocoder Assembly

Signal	Purpose
+5 V_REF	This signal is generated from +5 V signal. The L5/C38/L6/C39 filter isolates the signal. This signal is used as the LPC analog +5 V supply.
+12_5VREF	This signal is generated from the variable voltage regulator's (U19) +16 V supply. This signal is used as the local positive analog voltage supply.
+12_5V	This signal is the low pass filter version of +12_5VREF. This signal is used for the local +12.5 V Vpp used in FLASH reprogramming.

4. TESTING AND ALIGNMENT

This assembly requires no alignment.

5. BITE FAULTS AND TROUBLESHOOTING

Table 3 is a list of the self-test fault codes for the A3 LPC Assembly. The faults are described in greater detail in this subsection.

Table 3. A3 LPC Assembly Fault Codes

Code	Fault
01	8751 communications fault
02	8751 ROM fault
03	8751 microprocessor internal RAM fault
05	8751 dual port RAM fault
06	8751 dual port RAM busy fault
07	8751 dual port RAM interrupt fault
14	Hop clock fault
15	Frame clock fault
81	TMS320 internal RAM fault
82	TMS320 external program RAM fault
83	TMS320 external data RAM fault
84	TMS320 ROM fault
85	TMS320 dual port RAM fault
86	Sample clock fault
87	TMS320 AIC fault
88	TMS320 DAC fault
F5	8751 not finished fault
FA	TMS320 not finished fault

5.1 Required Test Equipment

The following test equipment is required:

- Digital multimeter
- Oscilloscope (Tektronix 465m or equivalent)

5.2 Fault 01 – 8751 Communications Fault

Perform the following procedure:

a. With the A3 LPC Assembly removed and power applied to the radio, verify +5 V supply voltage (P1-7 and P1-8) at the LPC Assembly motherboard connector. If absent, take corrective action.

b. With the A3 LPC Assembly removed and power applied to the radio, verify 0 to 5 V activity on the High Speed Serial Bus signal (P1-34) at the LPC Assembly motherboard connector. If no activity exists, take corrective action.

c. With the A3 LPC Assembly removed and power applied to the radio, verify 0 to 5 V activity on the 9.6 MHz clock signal (P1-29) at the LPC Assembly motherboard connector. If no activity exists, take corrective action.

d. Otherwise, replace the A3 LPC Assembly.

5.3 Fault 02 – 8751 ROM Fault

Replace the A3 LPC Assembly.

5.4 Fault 03 – 8751 Microprocessor Internal RAM Fault

Replace the A3 LPC Assembly.

5.5 Fault 05 – 8751 Dual Port RAM Fault

Replace the A3 LPC Assembly.

5.6 Fault 06 – 8751 Dual Port RAM Busy Fault

Replace the A3 LPC Assembly.

5.7 Fault 07 – 8751 Dual Port RAM Interrupt Fault

Replace the A3 LPC Assembly.

5.8 Fault 14 – Hop Clock Fault

Perform the following procedure:

a. Verify 0 to 5 V activity on hop clock signal (P1-27) during BITE. If there is no activity, take corrective action.

b. Otherwise, replace the A3 LPC Assembly.

5.9 Fault 15 – Frame Clock Fault

Perform the following procedure:

a. Verify 0 to 5 V activity on frame clock signal (P1-26) during BITE. If no activity exists, take corrective action.

b. Otherwise, replace the A3 LPC Assembly.

5.10 Fault 81 – TMS320 Internal RAM Fault

Perform the following procedure:

a. Replace the A3 LPC Assembly. If problem persists, the A4 Assembly is not waiting long enough for LPC BITE tests to conclude and may be faulty.

5.11 Fault 82 – TMS320 External Program RAM Fault

Perform the following procedure:

a. Replace the A3 LPC Assembly.

b. If problem persists, the A4 Assembly is not waiting long enough for LPC BITE tests to conclude and may be faulty.

5.12 Fault 83 – TMS320 External Data RAM Fault

Perform the following procedure:

a. Replace the A3 LPC Assembly.

b. If problem persists, the A4 Assembly is not waiting long enough for LPC BITE tests to conclude and may be faulty.

5.13 Fault 84 – TMS320 ROM Fault

Perform the following procedure:

a. Replace the A3 LPC Assembly.

b. If problem persists, the A4 Assembly is not waiting long enough for LPC BITE tests to conclude and may be faulty.

5.14 Fault 85 – TMS320 Dual Port RAM Fault

Perform the following procedure:

a. Replace the A3 LPC Assembly.

b. If problem persists, the A4 Assembly is not waiting long enough for LPC BITE tests to conclude and may be faulty.

5.15 Fault 86 – Sample Clock Fault

Perform the following procedure:

a. Replace the A3 LPC Assembly.

b. If problem persists, the A4 Assembly is not waiting long enough for LPC BITE tests to conclude and may be faulty.

5.16 Fault 87 – TMS320 AIC Fault

Perform the following procedure:

a. Replace the A3 LPC Assembly.

b. If problem persists, the A4 Assembly is not waiting long enough for LPC BITE tests to conclude and may be faulty.

5.17 Fault 88 – TMS320 DAC Fault

Perform the following procedure:

a. Replace the A3 LPC Assembly.

b. If problem persists, the A4 Assembly is not waiting long enough for LPC BITE tests to conclude and may be faulty.

5.18 Fault F5 – 8751 Not Finished Fault

Perform the following procedure:

a. Replace the A3 LPC Assembly.

b. If problem persists, the A4 Assembly is not waiting long enough for LPC BITE tests to conclude and may be faulty.

5.19 Fault FA – TMS320 Not Finished Fault

Perform the following procedure:

a. Replace the A3 LPC Assembly.

b. If problem persists, the A4 Assembly is not waiting long enough for LPC BITE tests to conclude and may be faulty.

5.20 Troubleshooting Operational Faults

The following describe problems and solutions for operational faults that occur during troubleshooting.

Problem: No audio after hearing 39-tone modem waveform sign in DV.

Solution(s): Ensure that the following are set up EXACTLY the same for both transmitter and receiver.

- The Selected Encryption Key.
- The Value of that Encryption Key.

Problem: On a perfect channel, receive radio output speech sounds broken up, or pauses in speech.

Solution(s): This problem may not be due to the A3 LPC Assembly Option. Instead the problem lies in the A4 Signal Processor Assembly. Refer to the A4 Signal Processor Assembly's troubleshooting section.

Problem: Analog Voice Security is unintelligible.

Solution(s): Ensure the same encryption keys are selected and their values are the same.

Problem: DV and AVS are not working.

Solution(s): Configure the transmit and receive radios the same.

- USB or LSB
- Same Frequency
- Encryption On or OFF
- Same Key and Key Value

6. PARTS LIST, COMPONENT LOCATION DIAGRAM, AND SCHEMATIC DIAGRAM

Table 4 is the parts list, figure 4 is the component location diagram, and figure 5 is the schematic diagram for the A3 LPC Assembly.

Table 4. A3 LPC Assembly Parts List (10372-3440-01 Rev. A)

Ref. Desig.	Part Number	Description
C1	C13-0107-104	CAP, .1UF 10% 100V CER
C2	C13-0107-104	CAP, .1UF 10% 100V CER
C3	C13-0107-104	CAP, .1UF 10% 100V CER
C4	C36-0010-476	CAP, 47UF 10V TANT SMD
C5	C13-0107-104	CAP, .1UF 10% 100V CER
C6	C13-0107-104	CAP, .1UF 10% 100V CER
C7	C36-0010-476	CAP, 47UF 10V TANT SMD
C8	C13-0101-101	CAP 100PF 10% 100V SMD
C9	C13-0107-104	CAP, .1UF 10% 100V CER
C10	C13-0107-104	CAP, .1UF 10% 100V CER
C11	C13-0107-104	CAP, .1UF 10% 100V CER
C12	C36-0035-105	CAP 1UF 35V SMT
C13	C13-0107-104	CAP, .1UF 10% 100V CER
C14	C13-0107-104	CAP, .1UF 10% 100V CER
C15	C13-0107-104	CAP, .1UF 10% 100V CER
C16	C13-0107-104	CAP, .1UF 10% 100V CER
C17	C13-0107-104	CAP, .1UF 10% 100V CER
C18	C13-0107-104	CAP, .1UF 10% 100V CER
C19	C13-0107-104	CAP, .1UF 10% 100V CER
C20	C13-0107-104	CAP, .1UF 10% 100V CER
C21	C36-0010-476	CAP, 47UF 10V TANT SMD
C22	C13-0107-104	CAP, .1UF 10% 100V CER
C23	C13-0107-104	CAP, .1UF 10% 100V CER
C24	C13-0107-104	CAP, .1UF 10% 100V CER
C25	C13-0107-104	CAP, .1UF 10% 100V CER
C26	C13-0101-221	CAP 220PF 10% 100V SMD
C27	C13-0107-104	CAP, .1UF 10% 100V CER
C28	C13-0101-100	CAP 10PF 10% 100V SMD
C29	C36-0035-105	CAP 1UF 35V SMT
C30	C13-0107-104	CAP, .1UF 10% 100V CER
C31	C13-0101-221	CAP 220PF 10% 100V SMD
C32	C13-0107-104	CAP, .1UF 10% 100V CER
C33	C13-0107-104	CAP, .1UF 10% 100V CER
C34	C13-0107-104	CAP, .1UF 10% 100V CER
C35	C36-0035-105	CAP 1UF 35V SMT
C36	C13-0107-104	CAP, .1UF 10% 100V CER

Table 4. A3 LPC Assembly Parts List (10372-3440-01 Rev. A) (Cont.)

Ref. Desig.	Part Number	Description
C37	C36-0035-105	CAP 1UF 35V SMT
C38	C36-0010-476	CAP, 47UF 10V TANT SMD
C39	C36-0035-105	CAP 1UF 35V SMT
C40	C13-0107-104	CAP, .1UF 10% 100V CER
C41	C36-0010-476	CAP, 47UF 10V TANT SMD
C42	C13-0105-102	CAP CER 1000PF 5% 50V NPO
C43	C13-0107-104	CAP, .1UF 10% 100V CER
C44	C13-0105-102	CAP CER 1000PF 5% 50V NPO
C45	C36-0035-105	CAP 1UF 35V SMT
C46	C13-0107-104	CAP, .1UF 10% 100V CER
C47	C13-0107-104	CAP, .1UF 10% 100V CER
C48	C36-0035-105	CAP 1UF 35V SMT
C49	C36-0035-105	CAP 1UF 35V SMT
C50	C36-0035-105	CAP 1UF 35V SMT
C51	C36-0010-476	CAP, 47UF 10V TANT SMD
C52	C13-0107-104	CAP, .1UF 10% 100V CER
C53	C13-0107-104	CAP, .1UF 10% 100V CER
C54	C13-0107-104	CAP, .1UF 10% 100V CER
C55	C36-0010-476	CAP, 47UF 10V TANT SMD
C56	C13-0101-221	CAP 220PF 10% 100V SMD
C57	C36-0035-105	CAP 1UF 35V SMT
C58	C13-0107-104	CAP, .1UF 10% 100V CER
C60	C13-0107-104	CAP, .1UF 10% 100V CER
CR1	D20-0005-001	DIODE, SOT-23
J1	J46-0129-014	14 PIN FEM RT ANGLE CONN
L1	10303-3113-01	TOROID, 130UH
L2	L45-0005-152	COIL 1.5UH 10% SMD
L3	L45-0005-152	COIL 1.5UH 10% SMD
L4	L45-0005-152	COIL 1.5UH 10% SMD
L5	10303-3113-01	TOROID, 130UH
L6	L45-0005-152	COIL 1.5UH 10% SMD
P1	J46-0117-050	CONN, 50 PIN MALE
Q1	2N7002	TRANSISTOR, FET (SOT-23)
Q2	Q26-0025-001	MOSFET,P-CHAN
Q3	2N7002	TRANSISTOR, FET (SOT-23)
Q4	Q26-0025-001	MOSFET,P-CHAN
R1	R85-0004-301	RES 10K 1% 1/8W FLM
R2	R85-0004-301	RES 10K 1% 1/8W FLM
R3	R85-0004-101	RES 100 1% 1/8W FLM

Table 4. A3 LPC Assembly Parts List (10372-3440-01 Rev. A) (Cont.)

Ref. Desig.	Part Number	Description
R4	R85-0004-226	RES 1.82K 1% 1/8W CHIP
R5	R85-0004-301	RES 10K 1% 1/8W FLM
R6	R85-0004-301	RES 10K 1% 1/8W FLM
R7	R85-0004-266	RES,4.75K 1% 1/8W CHIP
R8	R85-0004-000	RES ZERO OHM 1/8W FILM
R9	R85-0004-266	RES,4.75K 1% 1/8W CHIP
R10	R85-0004-301	RES 10K 1% 1/8W FLM
R13	R85-0004-051	RES 33.2 1% 1/8W CHIP
R14	R41-0005-223	RES NET SMD 22K 2%
R15	R85-0004-334	RES 22.1K 1% 1/8W FLM
R16	R85-0004-051	RES 33.2 1% 1/8W CHIP
R17	R85-0004-051	RES 33.2 1% 1/8W CHIP
R18	R85-0004-051	RES 33.2 1% 1/8W CHIP
R20	R85-0004-051	RES 33.2 1% 1/8W CHIP
R21	R85-0004-301	RES 10K 1% 1/8W FLM
R22	R85-0004-201	RES 1000 1% 1/8W FLM
R23	R85-0004-000	RES ZERO OHM 1/8W FILM
R24	R85-0004-401	RES 100K 1% 1/8W FLM
R25	R85-0004-401	RES 100K 1% 1/8W FLM
R26	R85-0004-000	RES ZERO OHM 1/8W FILM
R30	R85-0004-381	RES 68.1K 1% 1/8W FLM
R31	R85-0004-401	RES 100K 1% 1/8W FLM
R32	R85-0004-401	RES 100K 1% 1/8W FLM
R33	R85-0004-401	RES 100K 1% 1/8W FLM
R34	R85-0004-401	RES 100K 1% 1/8W FLM
R35	R85-0004-401	RES 100K 1% 1/8W FLM
R36	R85-0004-401	RES 100K 1% 1/8W FLM
R38	R85-0004-401	RES 100K 1% 1/8W FLM
R39	R85-0004-151	RES 332 1% 1/8W FLM
R40	R85-0004-266	RES,4.75K 1% 1/8W CHIP
R41	R85-0004-266	RES,4.75K 1% 1/8W CHIP
R42	R85-0004-000	RES ZERO OHM 1/8W FILM
R43	R85-0004-401	RES 100K 1% 1/8W FLM
R45	R85-0004-101	RES 100 1% 1/8W FLM
R46	R85-0004-101	RES 100 1% 1/8W FLM
R48	R85-0004-101	RES 100 1% 1/8W FLM
R49	R85-0004-401	RES 100K 1% 1/8W FLM
R50	R85-0004-101	RES 100 1% 1/8W FLM
R51	R85-0004-101	RES 100 1% 1/8W FLM

Table 4. A3 LPC Assembly Parts List (10372-3440-01 Rev. A) (Cont.)

Ref. Desig.	Part Number	Description
R52	R85-0004-101	RES 100 1% 1/8W FLM
R53	R85-0004-401	RES 100K 1% 1/8W FLM
R54	R85-0004-101	RES 100 1% 1/8W FLM
R55	R85-0004-401	RES 100K 1% 1/8W FLM
R56	R85-0004-245	RES 2.87K 1% 1/8W SMD
R58	R85-0004-000	RES ZERO OHM 1/8W FILM
R59	R85-0004-000	RES ZERO OHM 1/8W FILM
R60	R85-0004-301	RES 10K 1% 1/8W FLM
R61	R85-0004-051	RES 33.2 1% 1/8W CHIP
R63	R85-0004-301	RES 10K 1% 1/8W FLM
R64	R85-0004-266	RES,4.75K 1% 1/8W CHIP
U1	10181-8015	FIRMWARE KIT, EMBD MON
U2	I01-5000-573	8-BIT LATCH (74HC573DW)
U3	I25-0033-006	IC, 128K X 8 FLASH EPROM
U4	I26-0034-005	IDT71321LA45J
U5	I01-6000-032	IC QUAD 2-IN OR SMT
U6	I01-5000-074	IC,CMOS D-FF,SOIC
U7	I70-0005-003	PROG FREQ SYNTH (MC145158
U8	I01-5000-406	PLL WITH VCO (74HC4046AD)
U9	I01-5000-259	IC 74HC259D PLSTC CMOS
U10	I01-5000-004	HEX INVERTER (74HC04D)
U11	I02-0021-005	IC, MC74HCU04D HEX INV
U12	I87-0007-001	TMS320C50PQ
U13	I01-6000-032	IC QUAD 2-IN OR SMT
U14	I25-0033-006	IC, 128K X 8 FLASH EPROM
U15	I25-0033-006	IC, 128K X 8 FLASH EPROM
U16	10284-2443	IC, 64K X 16 STATIC RAM
U17	I30-0067-001	TL032AID(R)
U19	I11-0015-008	REGULATOR, SM
U20	I03-0032-001	IC CMOS D/A CONVERTER
U21	I01-5000-174	HEX D-FF (74HC174D)
U22	I59-0014-001	TLC320AC01CFN, AIC
U23	I06-0013-101	DUAL SPDT SWITCH DG403AB
U24	I30-0049-005	MC33172D
U25	10284-2443	IC, 64K X 16 STATIC RAM
U27	I01-5000-008	IC 74HC08AD PLSTC CMOS
U28	I01-5000-032	IC 74HC32AD PLSTC CMOS
Y1	Y01-0017-001	OSC 40 MHZ SMD

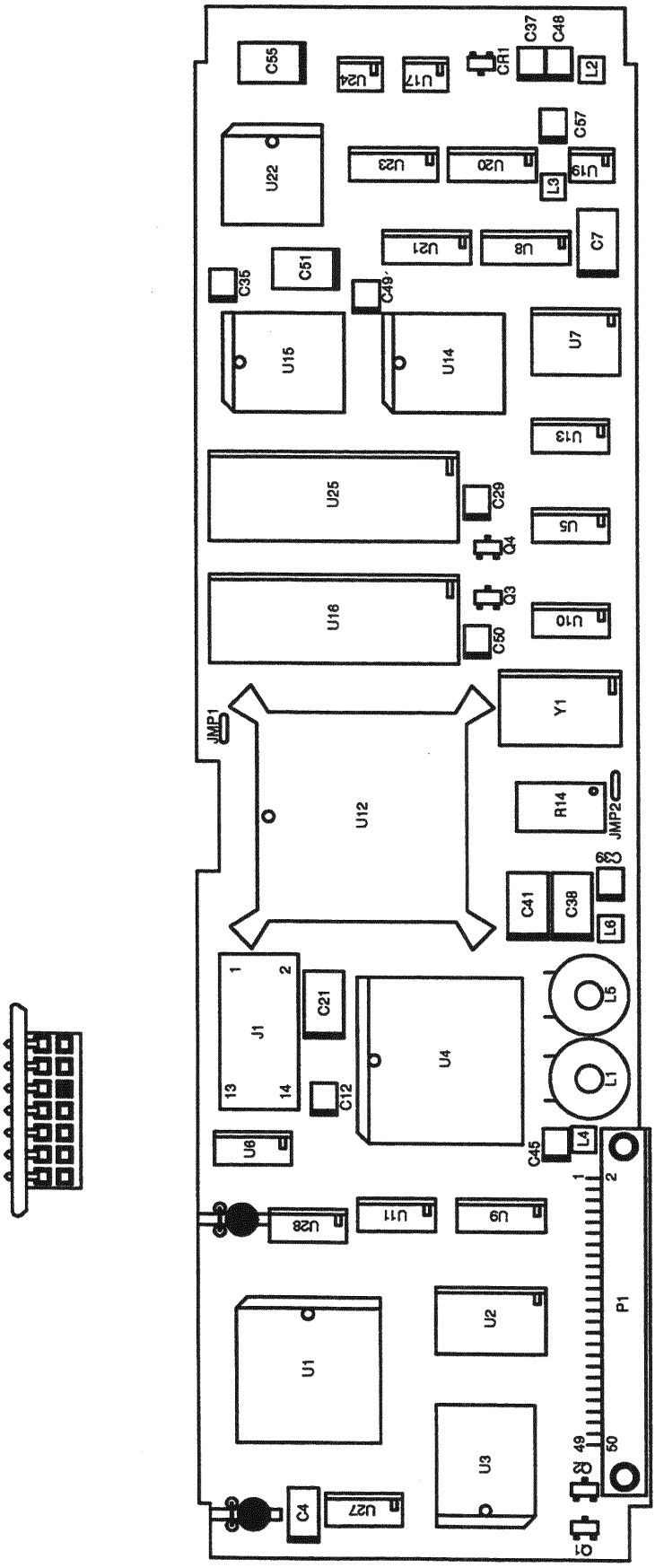


Figure 4. A3 LPC PWB Assembly Component Location Diagram (10372-3440 Rev. A) (Sheet 1 of 2)

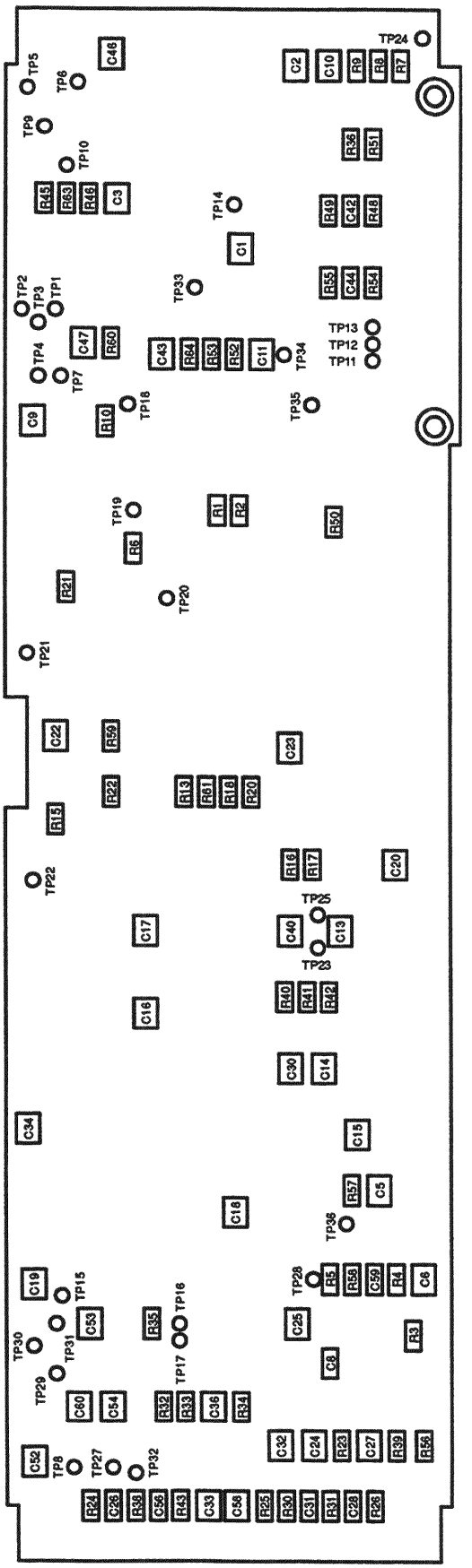
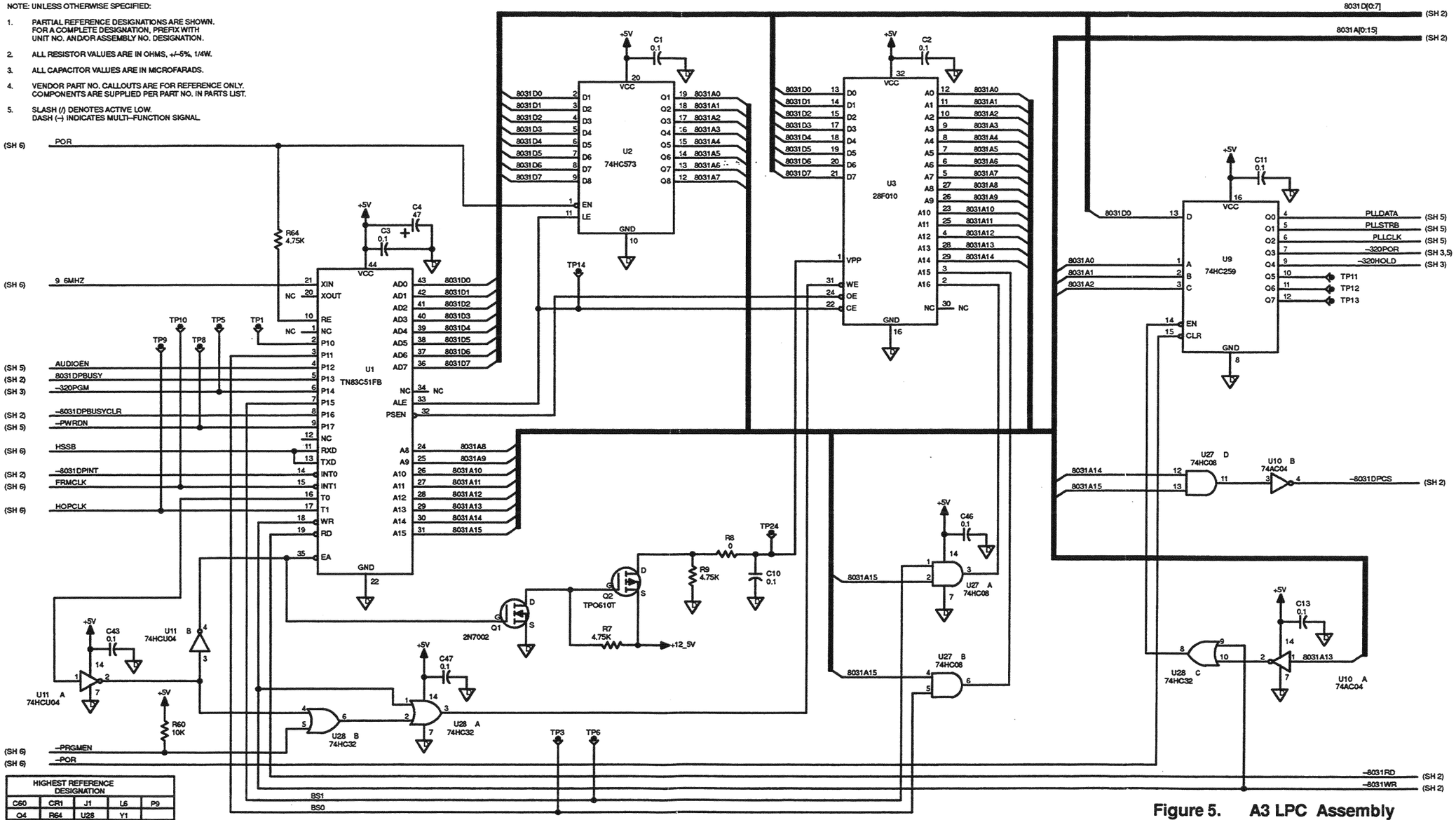


Figure 4. A3 LPC PWB Assembly Component Location Diagram (10372-3440 Rev. A) (Sheet 2 of 2)

NOTE: UNLESS OTHERWISE SPECIFIED:

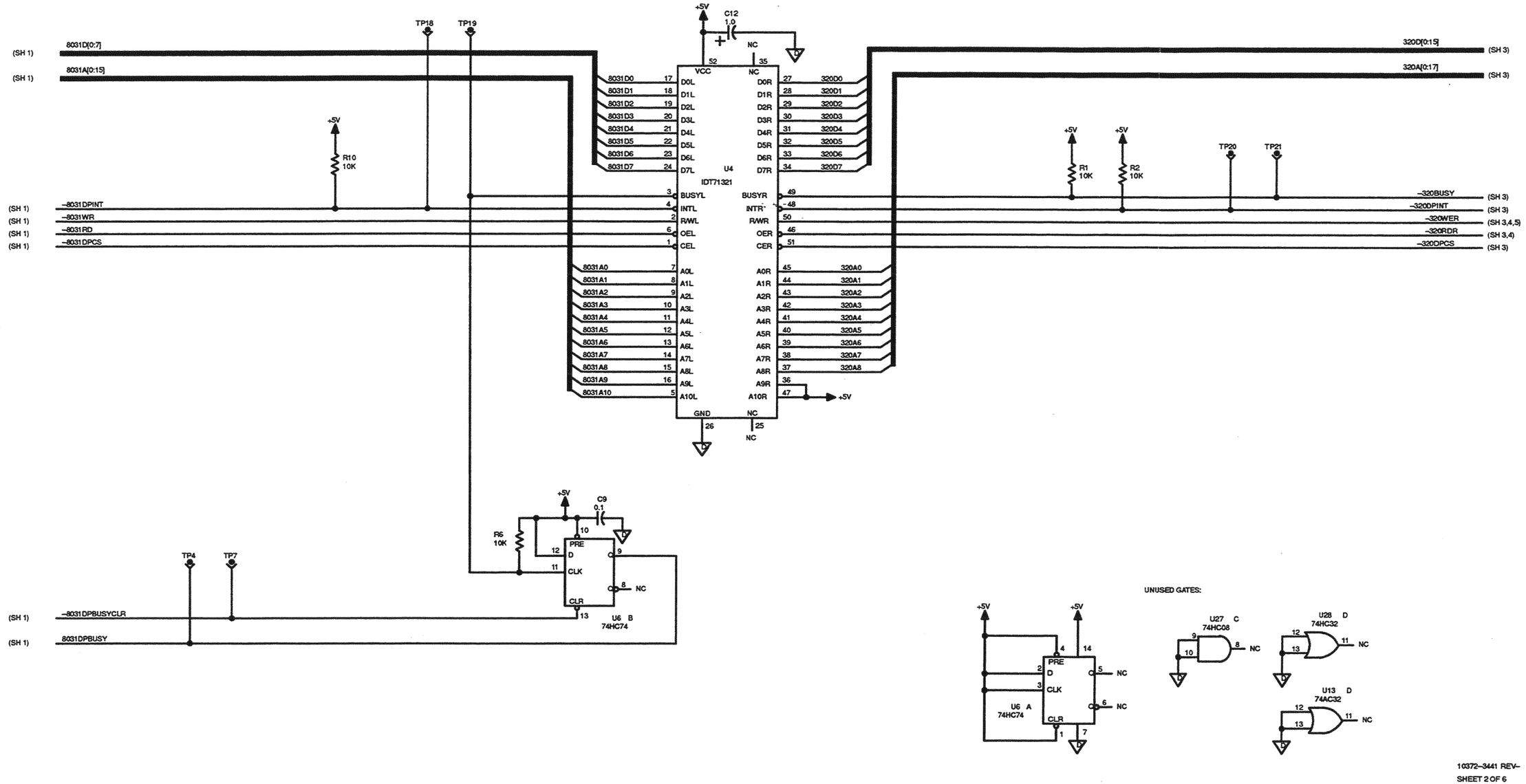
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR A COMPLETE DESIGNATION, PREFIX WITH UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.
2. ALL RESISTOR VALUES ARE IN OHMS, +/-5%, 1/4W.
3. ALL CAPACITOR VALUES ARE IN MICROFARADS.
4. VENDOR PART NO. CALLOUTS ARE FOR REFERENCE ONLY. COMPONENTS ARE SUPPLIED PER PART NO. IN PARTS LIST.
5. SLASH (/) DENOTES ACTIVE LOW. DASH (–) INDICATES MULTI-FUNCTION SIGNAL.



HIGHEST REFERENCE DESIGNATION				
C60	CR1	J1	L6	P9
Q4	R64	U28	Y1	

REF. DESIGNATIONS NOT USED				
P1–P8		R11	R12	R19
R27	R28	R29	R37	R44
R47	R52	U18	U26	

Figure 5. A3 LPC Assembly Schematic Diagram (10372-3441 Rev. –) (Sheet 1 of 6)



UNUSED GATES:

10372-3441 REV–
SHEET 2 OF 6

Figure 5. A3 LPC Assembly Schematic Diagram (10372-3441 Rev. –) (Sheet 2 of 6)

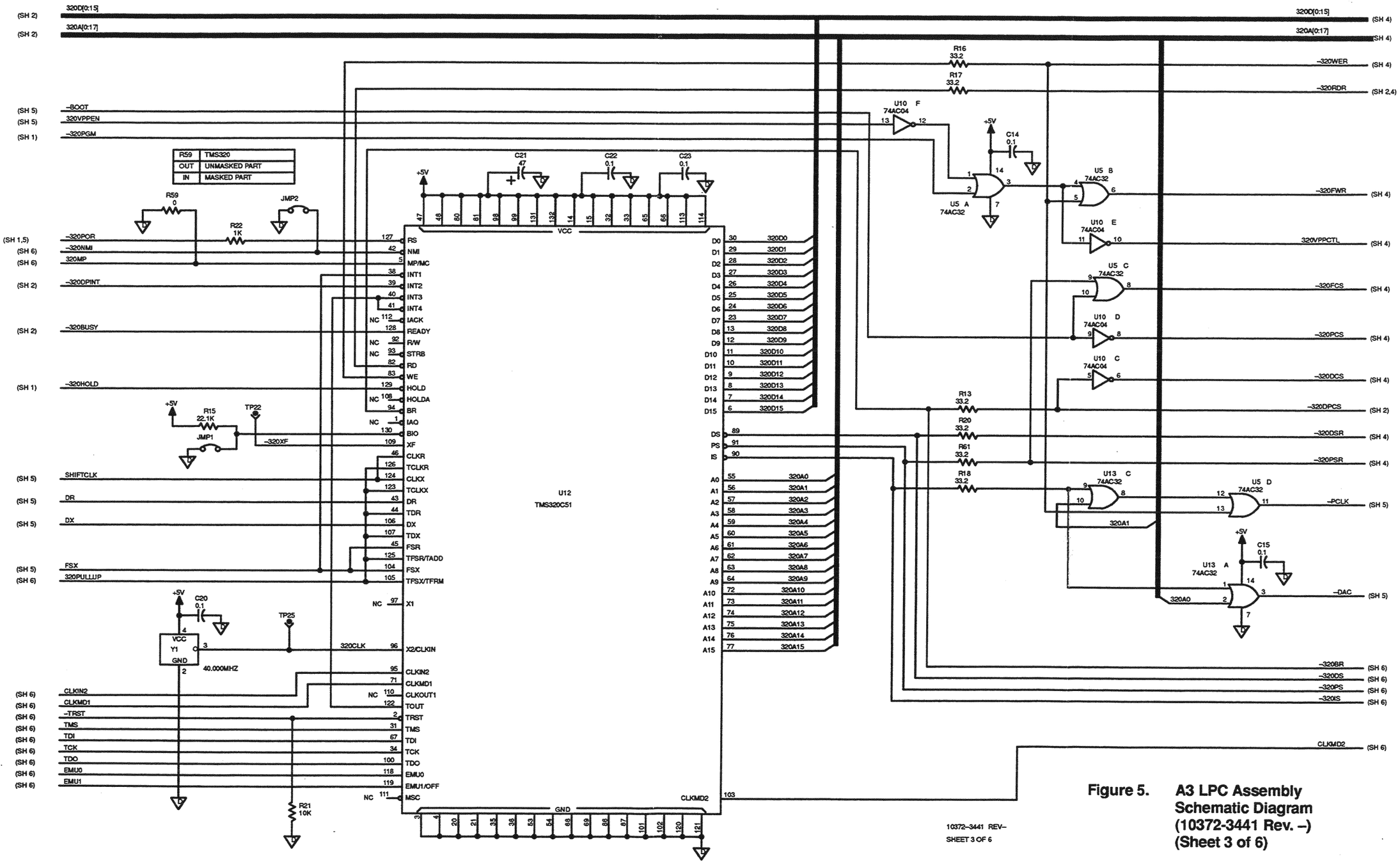


Figure 5. A3 LPC Assembly Schematic Diagram (10372-3441 Rev. –) (Sheet 3 of 6)

10372-3441 REV–
SHEET 3 OF 6

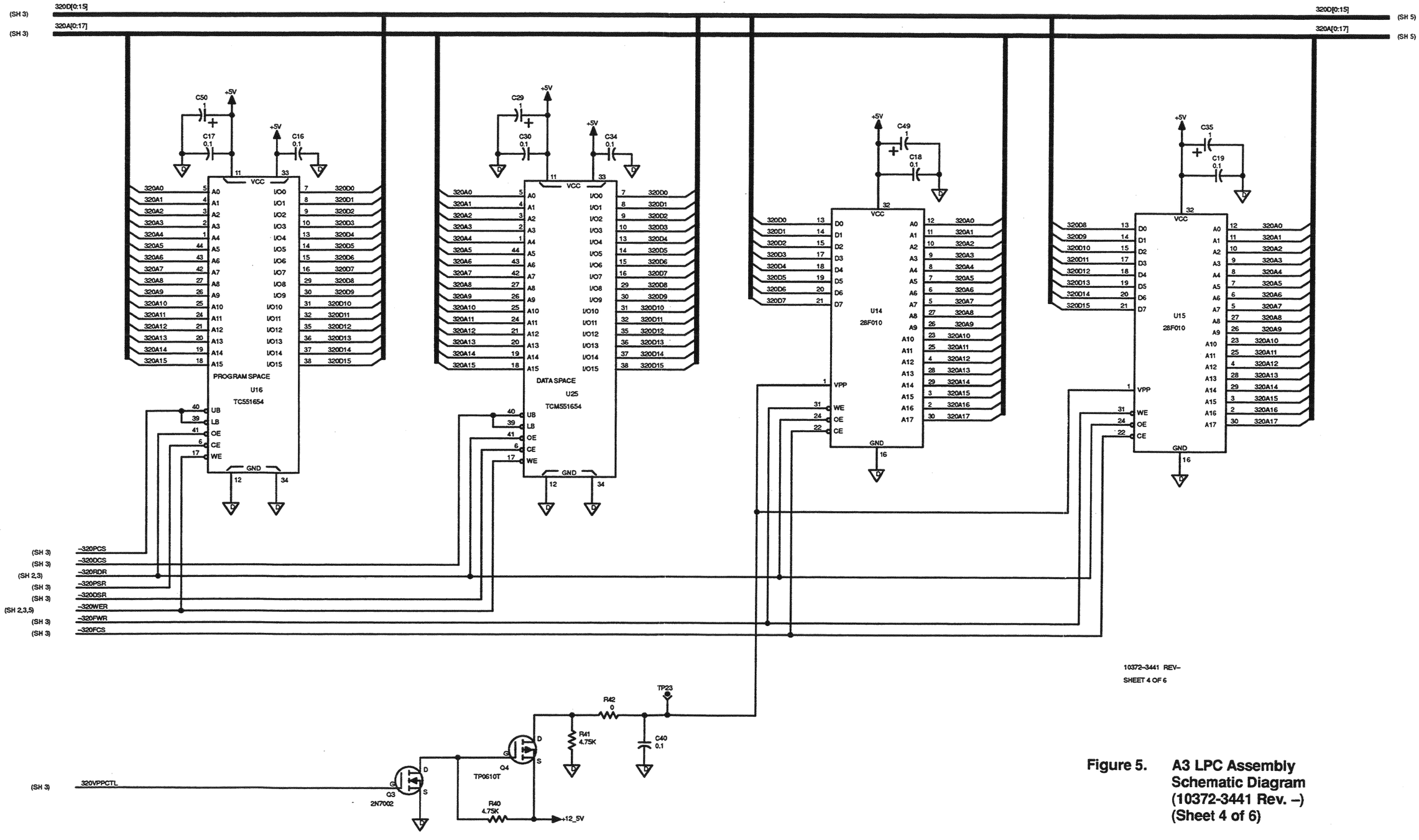


Figure 5. A3 LPC Assembly Schematic Diagram (10372-3441 Rev. –) (Sheet 4 of 6)

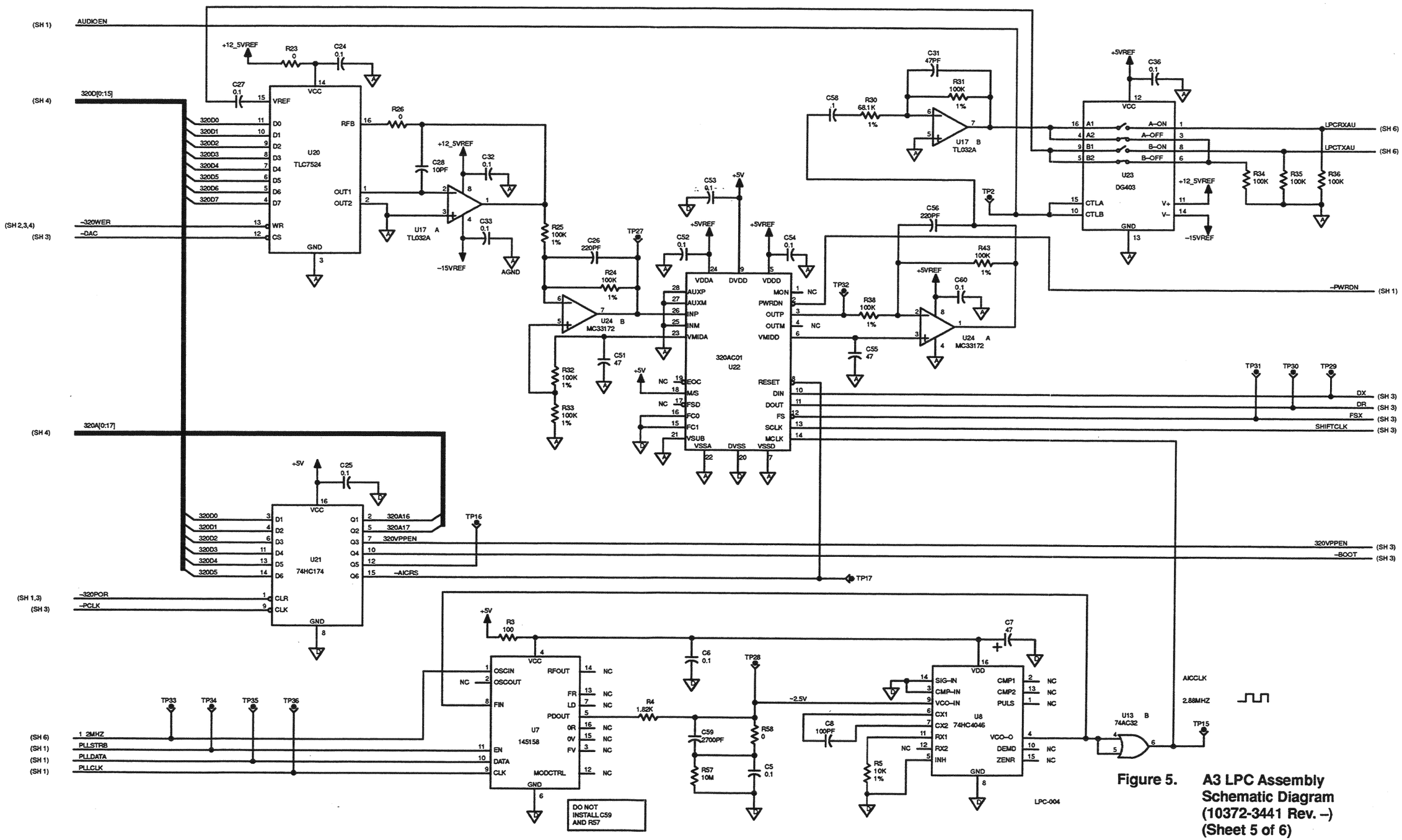


Figure 5. A3 LPC Assembly Schematic Diagram (10372-3441 Rev. –) (Sheet 5 of 6)

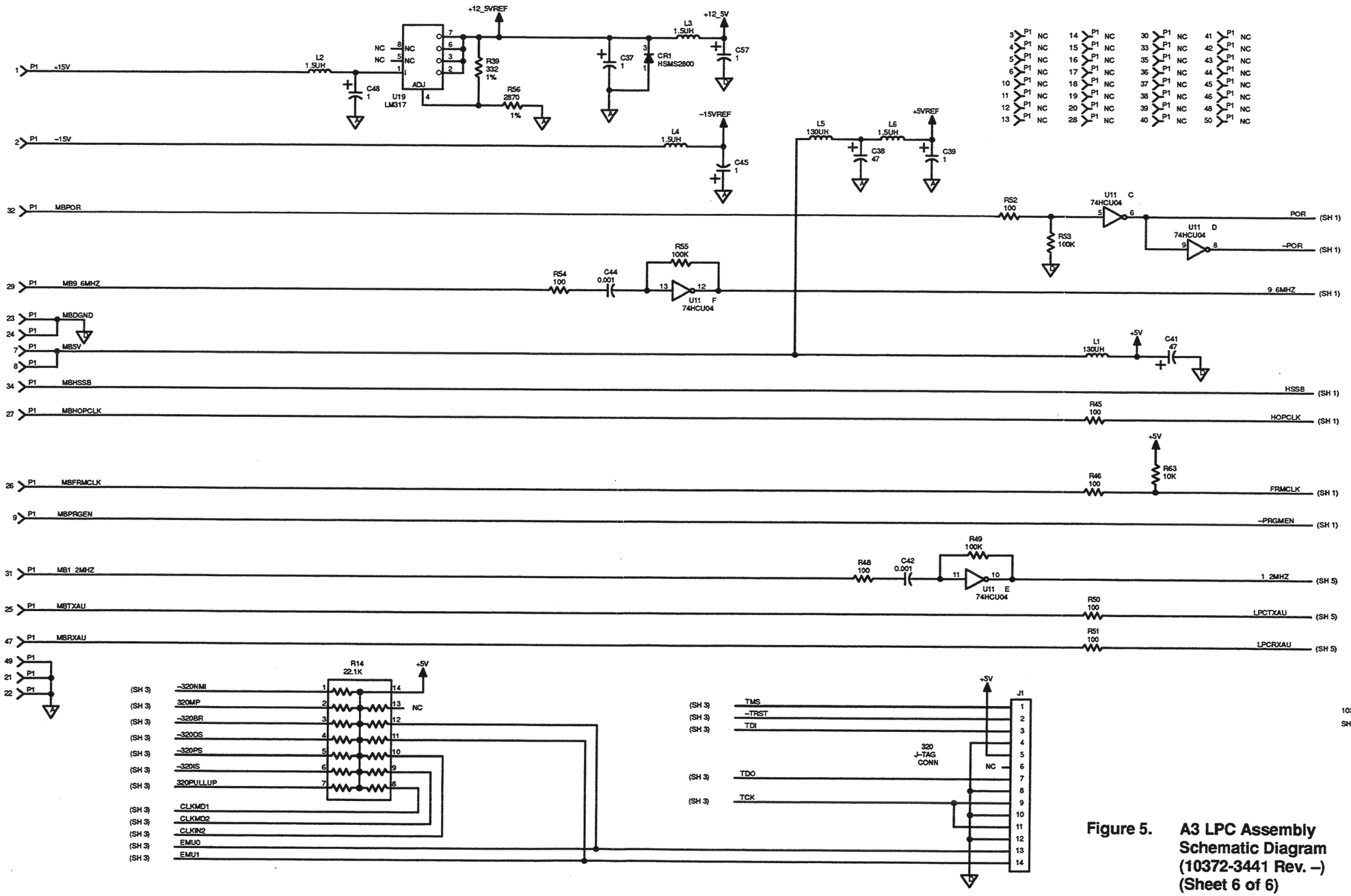
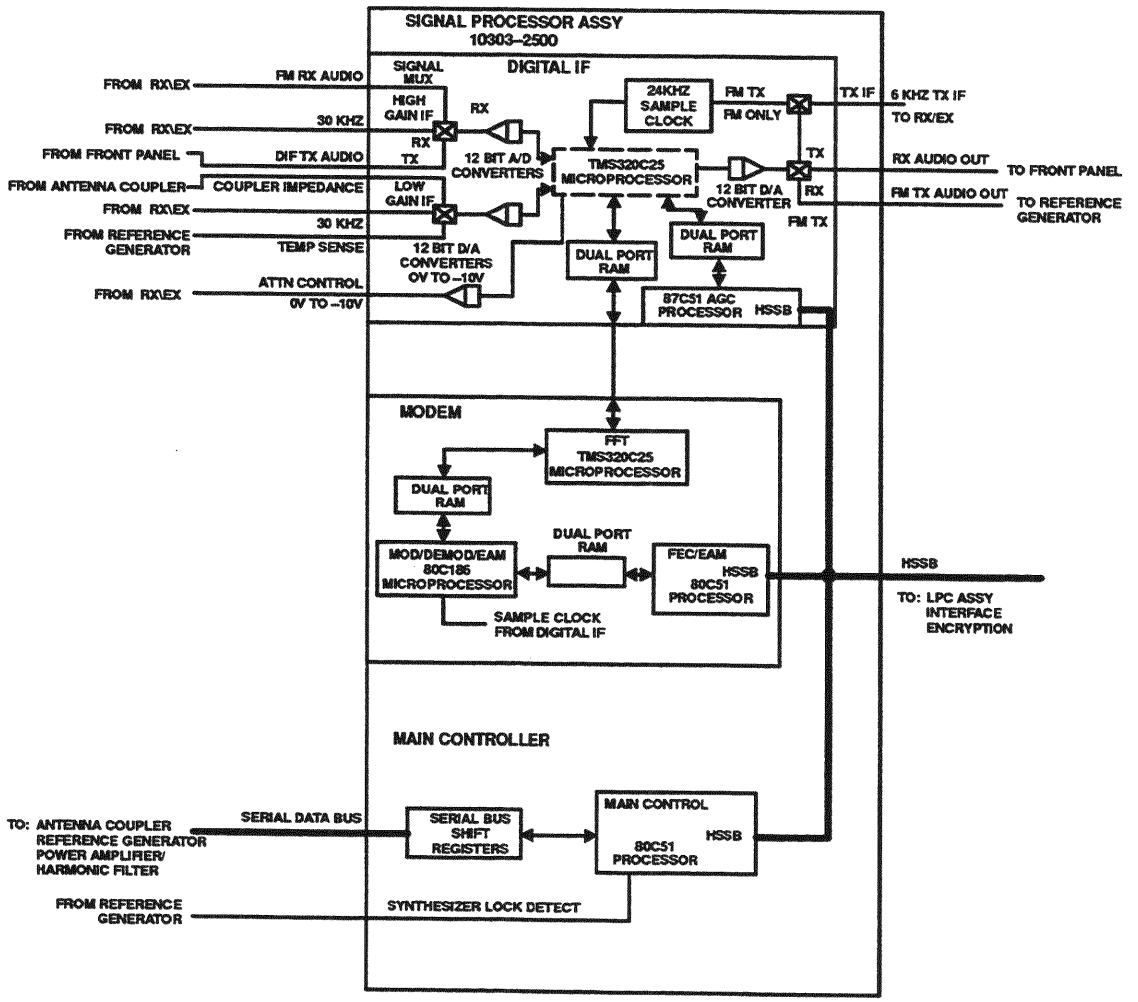


Figure 5. A3 LPC Assembly Schematic Diagram (10372-3441 Rev. –) (Sheet 6 of 6)

A4
SIGNAL PROCESSOR



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A4 SIGNAL PROCESSOR

1. GENERAL DESCRIPTION

The Signal Processor Assembly (10303-2500), though physically divided into three sections, is functionally divided into five major subsets. These subsets are the Main Controller, Digital IF/AGC, Modem, Frequency Hopping, and Automatic Link Establishment sections. These operations are not confined to any particular physical area on the A4 Assembly. All five of these functions utilize the entire PWB and, to some extent, do share hardware. The user must realize, when reading the functional explanations of this assembly, that any given hardware component may be used in any given function, and is likely to be mentioned in more than one section. The operation of the A4 Signal Processor Assembly is explained in five separate and complete subsections, broken down by the five major functions of the assembly.

The A4 Assembly, as a whole, is responsible for the control and coordination of all other functional parts of the RT-1694 during operation, and their evaluation during self test. Communications internal to the A4 Signal Processor Assembly are handled largely by the internal high speed serial bus (HSSB). It is through this bus that the Main Controller processor sends commands to the other microprocessors on the assembly. The other major component of internal communications is dual-port RAM, used as a message passing common memory area by the Modem and Digital IF functions.

2. INTERFACE CONNECTIONS

The A4 Signal Processor Assembly distributes data and commands to other assemblies in the R/T through the A11 Motherboard Assembly. The signals sent to and received by the A4 Signal Processor Assembly are listed in table 1.

Table 1. A4 Signal Processor Assembly Interface Connections

Connector and Pin	Signal	Connector and Pin	Signal
P3-1	Main Synth Strobe	P3-26	Vpp
P3-2	Serial Data	P3-27	+16V Unregulated
P3-3	Aux Synth Strobe	P3-28	/PGM
P3-4	Serial Clock	P3-29	–12V
P3-5	Rcvr IF 1	P3-30	N.C.
P3-6	Lock Detect	P3-31	9.6 MHz clock
P3-7	Rcvr IF 2	P3-32	3.9V Battery Backup
P3-8	FM Tx Audio	P3-33	36 MHz clock
P3-9	6 kHz TX IF	P3-34	N.C.
P3-10	FM Rx Audio	P3-35	/Master Reset
P3-11	EEPROM Data Strobe	P3-36	N.C.
P3-12	RF Atten Ctl	P3-37	OK to Tx
P3-13	TCXO Temp Sense	P3-38	IF Rx Audio
P3-14	EEPROM Serial Data	P3-39	+5V
P3-15	1.2 MHz clock	P3-40	+5V
P3-16	/Tx Keyline	P3-41	Hop Clock
P3-17	PA/Cplr Strobe	P3-42	Aux Key
P3-18	N.C.	P3-43	+5V
P3-19	Cplr Mux Control #2	P3-44	IF Tx Audio
P3-20	Tx Keyline	P3-45	Frame Clock

Table 1. A4 Signal Processor Assembly Interface Connections (Cont.)

Connector and Pin	Signal	Connector and Pin	Signal
P3-21	Cplr Feedback B	P3-46	Analog GND
P3-22	Cplr Mux Control #1	P3-47	Analog GND
P3-23	PA Feedback	P3-48	N.C.
P3-24	Cplr Feedback A	P3-49	Analog GND
P3-25	HSSB	P3-50	Analog GND

3. TECHNICAL DESCRIPTION

The technical descriptions for each part of the A4 Signal Processor Assembly are found in their individual subsections.

4. TESTING AND ALIGNMENT

There are no testing and alignment procedures for the A4 Signal Processor Assembly.

5. BITE FAULTS AND TROUBLESHOOTING

The self-test fault codes for the A4 Signal Processor Assembly are shown in table 2.

The tests and faults for the various parts of the Signal Processor Assembly are described in greater detail in their individual subsections.

Table 2. A4 Signal Processor Assembly Fault Codes

Code	Fault
01	Communication fault
14	Hop clock error
15	Frame Clock error
1F	FEC ROM checksum fault
20	FEC External RAM fault
21	FEC dual port RAM fault
22	MDM not running
23	FFT handshake fault
24	FFT to MDM dual port RAM fault
25	MDM to FFT dual port RAM fault
26	MDM to FEC dual port RAM fault
27	MDM ROM checksum fault
28	MDM RAM fault
29	Sample Clock error
2A	FFT ROM checksum fault
2B	FFT internal RAM fault
2C	FFT external RAM fault
2D	FFT to DIF dual port RAM fault
2E	Hop Clock error
2F	FFT self test not complete

Table 2. A4 Signal Processor Assembly Fault Codes (Cont.)

Code	Fault
30	FFT self test not complete
31	Reserved
32	Time Sample transfer
33	MDM self test not complete
34	FEC self test not complete
42	Non-destructive internal RAM fault
43	ROM checksum fault
44	Non-destructive external RAM fault
61	Communication fault
62	Internal RAM fault
63	ROM checksum fault
64	External RAM fault
67	Digital IF handshake fault (Dual Port RAM)
6B	Digital IF did not complete BITE
6C	Anti-Alias filter fault
6D	28.8-kHz Sampler clock fault
6E	24.0-kHz Sampler clock fault
74	Frame Clock not detected
75	Hop Clock not detected
80	ROM checksum fault
82	External RAM fault
83	Dual port RAM to AGC fault
84	Dual port RAM to FFT fault
85	Filter fault – Below lower limit
86	Filter fault – Above Upper Limit
87	Bad fault code returned from filter test
88	External Sample clock fault – staying high
89	External Sample clock fault – staying low
8A	External Sample clock fault – low too long
8B	External Sample clock fault –low too short
8C	External Sample clock fault – high too long
8D	External Sample clock fault – high too short
8E	External Sample clock fault – low too long
8F	External Sample clock fault – low too short
90	External Sample clock fault – timer ran out
91	External Sample clock fault – timer ran out

Table 2. A4 Signal Processor Assembly Fault Codes (Cont.)

Code	Fault
92	External Sample clock fault – timer ran out
93	Hop clock not detected
9D	Fault
9E	Bad tone detected, amplitude too low
9F	Bad tone detected, amplitude too high

6. PARTS LISTS, COMPONENT LOCATION DIAGRAMS, AND SCHEMATIC DIAGRAMS

Table 3 is the parts list for the A4 Signal Processor Assembly. Figure 1 is the component location diagram and figure 2 is the schematic diagram.

Table 3. A4 Signal Processor Assembly Parts List (10303-2500 Rev. K)

Ref. Desig.	Part Number	Description
—	10372-1524-02	CORD ASSY
C1	C36-0010-476	CAP, 47UF 10V TANT SMD
C2	C13-0103-473	CAP .047UF 10% 100V SMD
C3	C13-0103-473	CAP .047UF 10% 100V SMD
C4	C13-0103-473	CAP .047UF 10% 100V SMD
C5	C13-0103-473	CAP .047UF 10% 100V SMD
C6	C13-0103-473	CAP .047UF 10% 100V SMD
C7	C13-0103-473	CAP .047UF 10% 100V SMD
C8	C13-0103-473	CAP .047UF 10% 100V SMD
C9	C13-0103-473	CAP .047UF 10% 100V SMD
C10	C13-0103-473	CAP .047UF 10% 100V SMD
C11	C13-0103-473	CAP .047UF 10% 100V SMD
C12	C13-0103-473	CAP .047UF 10% 100V SMD
C13	C13-0103-473	CAP .047UF 10% 100V SMD
C14	C13-0103-473	CAP .047UF 10% 100V SMD
C15	C13-0103-473	CAP .047UF 10% 100V SMD
C16	C36-0035-334	CAP .33UF 35V TANT SMD
C17	C13-0103-473	CAP .047UF 10% 100V SMD
C18	C36-0010-476	CAP, 47UF 10V TANT SMD
C19	C13-0103-473	CAP .047UF 10% 100V SMD
C20	C13-0103-473	CAP .047UF 10% 100V SMD
C21	C13-0103-473	CAP .047UF 10% 100V SMD
C22	C13-0103-473	CAP .047UF 10% 100V SMD
C23	C13-0103-473	CAP .047UF 10% 100V SMD
C24	C13-0103-473	CAP .047UF 10% 100V SMD
C25	C13-0103-473	CAP .047UF 10% 100V SMD
C26	C13-0103-473	CAP .047UF 10% 100V SMD
C27	C13-0103-473	CAP .047UF 10% 100V SMD

Table 3. A4 Signal Processor Assembly Parts List (10303-2500 Rev. N) (Cont.)

Ref. Desig.	Part Number	Description
C17	C13-0103-473	CAP .047UF 10% 100V SMD
C18	C36-0010-476	CAP, 47UF 10V TANT SMD
C19	C13-0103-473	CAP .047UF 10% 100V SMD
C20	C13-0103-473	CAP .047UF 10% 100V SMD
C21	C13-0103-473	CAP .047UF 10% 100V SMD
C22	C13-0103-473	CAP .047UF 10% 100V SMD
C23	C13-0103-473	CAP .047UF 10% 100V SMD
C24	C13-0103-473	CAP .047UF 10% 100V SMD
C25	C13-0103-473	CAP .047UF 10% 100V SMD
C26	C13-0103-473	CAP .047UF 10% 100V SMD
C27	C13-0103-473	CAP .047UF 10% 100V SMD
C28	C13-0103-473	CAP .047UF 10% 100V SMD
C29	C13-0103-473	CAP .047UF 10% 100V SMD
C30	C13-0105-102	CAP CER 1000PF 5% 100V
C31	C13-0103-473	CAP .047UF 10% 100V SMD
C32	C36-0035-105	CAP 1UF 35V SMT
C33	C13-0105-151	CAP 150PF 5% 100V
C34	C13-0101-150	CAP 15PF 10% 100V SMD
C35	C13-0101-181	CAP 180PF 10% 100E
C36	C13-0105-271	CAP 270PF 5% 100V SMD
C37	C13-0103-473	CAP .047UF 10% 100V SMD
C38	C13-0101-181	CAP 180PF 10% 100E
C39	C13-0105-151	CAP 150PF 5% 100V
C40	C13-0101-150	CAP 15PF 10% 100V SMD
C41	C13-0105-271	CAP 270PF 5% 100V SMD
C42	C13-0105-102	CAP CER 1000PF 5% 100V
C43	C13-0105-102	CAP CER 1000PF 5% 100V
C44	C13-0103-473	CAP .047UF 10% 100V SMD
C46	C13-0103-473	CAP .047UF 10% 100V SMD
C48	C13-0105-102	CAP CER 1000PF 5% 100V
C49	C13-0105-102	CAP CER 1000PF 5% 100V
C50	C13-0103-473	CAP .047UF 10% 100V SMD
C51	C13-0103-473	CAP .047UF 10% 100V SMD
C52	C13-0103-473	CAP .047UF 10% 100V SMD
C53	C13-0103-473	CAP .047UF 10% 100V SMD
C54	C13-0103-473	CAP .047UF 10% 100V SMD
C55	C36-0016-106	CAP 10UF 16V SMT
C56	C13-0103-473	CAP .047UF 10% 100V SMD
C57	C13-0103-473	CAP .047UF 10% 100V SMD

Table 3. A4 Signal Processor Assembly Parts List (10303-2500 Rev. N) (Cont.)

Ref. Desig.	Part Number	Description
C58	C13-0103-473	CAP .047UF 10% 100V SMD
C59	C13-0103-473	CAP .047UF 10% 100V SMD
C60	C36-0035-334	CAP .33UF 35V TANT SMD
C61	C36-0010-476	CAP, 47UF 10V TANT SMD
C62	C36-0035-334	CAP .33UF 35V TANT SMD
C63	C36-0016-106	CAP 10UF 16V SMT
C64	C36-0035-334	CAP .33UF 35V TANT SMD
C65	C36-0035-334	CAP .33UF 35V TANT SMD
C66	C13-0105-102	CAP CER 1000PF 5% 100V
C67	C13-0103-103	CAP .01UF 10% 100V SMD
C68	C13-0103-103	CAP .01UF 10% 100V SMD
C69	C13-0103-473	CAP .047UF 10% 100V SMD
C70	C13-0103-473	CAP .047UF 10% 100V SMD
C73	C13-0103-473	CAP .047UF 10% 100V SMD
C74	C13-0103-473	CAP .047UF 10% 100V SMD
C75	C13-0103-473	CAP .047UF 10% 100V SMD
C76	C13-0103-473	CAP .047UF 10% 100V SMD
C77	C13-0103-473	CAP .047UF 10% 100V SMD
C78	C36-0016-106	CAP 10UF 16V SMT
C79	C13-0103-473	CAP .047UF 10% 100V SMD
C80	C13-0103-473	CAP .047UF 10% 100V SMD
C81	C13-0103-473	CAP .047UF 10% 100V SMD
C82	C36-0010-476	CAP, 47UF 10V TANT SMD
C83	C13-0105-151	CAP 150PF 5% 100V
C84	C13-0103-473	CAP .047UF 10% 100V SMD
C85	C36-0010-476	CAP, 47UF 10V TANT SMD
C86	C13-0103-473	CAP .047UF 10% 100V SMD
C87	C13-0103-473	CAP .047UF 10% 100V SMD
C88	C13-0103-473	CAP .047UF 10% 100V SMD
C89	C13-0103-473	CAP .047UF 10% 100V SMD
C90	C13-0103-473	CAP .047UF 10% 100V SMD
C91	C13-0103-473	CAP .047UF 10% 100V SMD
C92	C13-0103-473	CAP .047UF 10% 100V SMD
C93	C13-0103-473	CAP .047UF 10% 100V SMD
C94	C13-0103-473	CAP .047UF 10% 100V SMD
C95	C13-0103-473	CAP .047UF 10% 100V SMD
C96	C13-0103-473	CAP .047UF 10% 100V SMD
C97	C36-0010-476	CAP, 47UF 10V TANT SMD
C98	C13-0103-473	CAP .047UF 10% 100V SMD

Table 3. A4 Signal Processor Assembly Parts List (10303-2500 Rev. N) (Cont.)

Ref. Desig.	Part Number	Description
C99	C13-0103-473	CAP .047UF 10% 100V SMD
C100	C13-0103-473	CAP .047UF 10% 100V SMD
C101	C13-0103-473	CAP .047UF 10% 100V SMD
C102	C13-0103-473	CAP .047UF 10% 100V SMD
C103	C36-0016-335	CAP 3.3UF 16V TANT SMD
C104	C13-0103-473	CAP .047UF 10% 100V SMD
C105	C13-0105-270	CAP 27PF 10% 100V SMD
C106	C13-0103-473	CAP .047UF 10% 100V SMD
C107	C13-0105-270	CAP 27PF 10% 100V SMD
C108	C36-0016-106	CAP 10UF 16V SMT
C109	C36-0016-106	CAP 10UF 16V SMT
C110	C13-0103-473	CAP .047UF 10% 100V SMD
C111	C36-0016-106	CAP 10UF 16V SMT
C112	C36-0016-106	CAP 10UF 16V SMT
C113	C36-0016-106	CAP 10UF 16V SMT
C114	C36-0010-476	CAP, 47UF 10V TANT SMD
C115	C36-0016-106	CAP 10UF 16V SMT
C116	C36-0016-106	CAP 10UF 16V SMT
C119	C13-0103-473	CAP .047UF 10% 100V SMD
C120	C13-0105-102	CAP CER 1000PF 5% 100V
C123	C36-0016-106	CAP 10UF 16V SMT
C124	C13-0103-473	CAP .047UF 10% 100V SMD
C125	C36-0010-476	CAP, 47UF 10V TANT SMD
C126	C36-0016-106	CAP 10UF 16V SMT
C127	C36-0010-476	CAP, 47UF 10V TANT SMD
C129	C36-0016-106	CAP 10UF 16V SMT
C130	C13-0103-473	CAP .047UF 10% 100V SMD
C131	C13-0103-473	CAP .047UF 10% 100V SMD
C132	C13-0103-473	CAP .047UF 10% 100V SMD
C133	C13-0103-473	CAP .047UF 10% 100V SMD
C134	C13-0103-473	CAP .047UF 10% 100V SMD
C135	C13-0103-473	CAP .047UF 10% 100V SMD
C136	C13-0103-473	CAP .047UF 10% 100V SMD
C137	C13-0103-473	CAP .047UF 10% 100V SMD
C138	C13-0103-473	CAP .047UF 10% 100V SMD
C141	C13-0105-102	CAP CER 1000PF 5% 100V
C142	C13-0105-102	CAP CER 1000PF 5% 100V
C150	C13-0101-272	CAP 2700PF 10% 100V SMD
CR1	D15-0914-101	DIODE HI-SPD SWITCHING

Table 3. A4 Signal Processor Assembly Parts List (10303-2500 Rev. N) (Cont.)

Ref. Desig.	Part Number	Description
CR2	D15-0914-101	DIODE HI-SPD SWITCHING
CR3	D15-0914-101	DIODE HI-SPD SWITCHING
CR4	D15-0914-101	DIODE HI-SPD SWITCHING
CR5	D15-0914-101	DIODE HI-SPD SWITCHING
CR6	D15-0914-101	DIODE HI-SPD SWITCHING
CR7	D15-0914-101	DIODE HI-SPD SWITCHING
CR8	D15-0914-101	DIODE HI-SPD SWITCHING
CR9	D15-0914-101	DIODE HI-SPD SWITCHING
CR10	D15-0914-101	DIODE HI-SPD SWITCHING
CR11	D15-0914-101	DIODE HI-SPD SWITCHING
CR12	D15-0914-101	DIODE HI-SPD SWITCHING
CR13	D15-0914-101	DIODE HI-SPD SWITCHING
CR14	D15-0914-101	DIODE HI-SPD SWITCHING
CR15	D15-0914-101	DIODE HI-SPD SWITCHING
CR16	D15-0914-101	DIODE HI-SPD SWITCHING
CR17	D15-0914-101	DIODE HI-SPD SWITCHING
CR18	D15-0914-101	DIODE HI-SPD SWITCHING
CR19	D15-0914-101	DIODE HI-SPD SWITCHING
CR20	D15-0914-101	DIODE HI-SPD SWITCHING
CR21	D15-0914-101	DIODE HI-SPD SWITCHING
CR22	D15-0914-101	DIODE HI-SPD SWITCHING
L1	MS75084-2	COIL 1.5UH 10% FXD RF
L2	MS75084-2	COIL 1.5UH 10% FXD RF
L3	10303-3113-01	TOROID, 130UH
L4	10303-3113-01	TOROID, 130UH
L5	10303-3113-01	TOROID, 130UH
P3	J46-0117-050	CONN, 50 PIN MALE
Q1	Q12-2222-101	XSTR NPN SWG SM SS/GP
Q2	Q12-2222-101	XSTR NPN SWG SM SS/GP
Q3	Q12-2222-101	XSTR NPN SWG SM SS/GP
Q4	2N7002	TRANSISTOR, FET (SOT-23)
Q5	2N7002	TRANSISTOR, FET (SOT-23)
Q6	2N7002	TRANSISTOR, FET (SOT-23)
R1	R85-0004-266	RES,4.75K 1% 1/8W CHIP
R2	R85-0004-251	RES 3320 1% 1/8W
R3	R85-0004-266	RES,4.75K 1% 1/8W CHIP
R6	R85-0125-104	RES 100K 5% 1/8W FILM
R7	R85-0125-101	RES 100 5% 1/8W FILM
R8	R85-0004-251	RES 3320 1% 1/8W

Table 3. A4 Signal Processor Assembly Parts List (10303-2500 Rev. N) (Cont.)

Ref. Desig.	Part Number	Description
R9	R85-0004-266	RES,4.75K 1% 1/8W CHIP
R11	R85-0004-251	RES 3320 1% 1/8W
R12	R85-0125-101	RES 100 5% 1/8W FILM
R13	R85-0125-101	RES 100 5% 1/8W FILM
R14	R85-0125-101	RES 100 5% 1/8W FILM
R15	R85-0125-101	RES 100 5% 1/8W FILM
R16	R85-0125-101	RES 100 5% 1/8W FILM
R17	R85-0125-104	RES 100K 5% 1/8W FILM
R18	R85-0125-103	RES 10K 5% 1/8W FILM
R19	R85-0125-103	RES 10K 5% 1/8W FILM
R20	R85-0125-101	RES 100 5% 1/8W FILM
R21	R85-0125-101	RES 100 5% 1/8W FILM
R22	R85-0125-101	RES 100 5% 1/8W FILM
R23	R85-0004-251	RES 3320 1% 1/8W
R24	R85-0004-251	RES 3320 1% 1/8W
R25	R85-0004-266	RES,4.75K 1% 1/8W CHIP
R27	R85-0125-104	RES 100K 5% 1/8W FILM
R28	R85-0004-266	RES,4.75K 1% 1/8W CHIP
R29	R85-0125-101	RES 100 5% 1/8W FILM
R30	R85-0125-104	RES 100K 5% 1/8W FILM
R31	R85-0004-434	RES 221K 1% 1/8W SMD
R32	R85-0125-101	RES 100 5% 1/8W FILM
R33	R85-0125-104	RES 100K 5% 1/8W FILM
R34	R85-0004-434	RES 221K 1% 1/8W SMD
R35	R85-0004-434	RES 221K 1% 1/8W SMD
R36	R85-0004-434	RES 221K 1% 1/8W SMD
R37	R85-0004-434	RES 221K 1% 1/8W SMD
R38	R85-0004-434	RES 221K 1% 1/8W SMD
R39	R85-0125-101	RES 100 5% 1/8W FILM
R40	R85-0125-101	RES 100 5% 1/8W FILM
R41	R85-0004-130	RES 200 1% 1/8W FLM
R42	R85-0004-290	RES 8450 1% 1/8W FLM
R43	R85-0004-255	RES 3650 1% 1/8W FLM
R44	R85-0125-101	RES 100 5% 1/8W FILM
R45	R85-0125-101	RES 100 5% 1/8W FILM
R46	R85-0125-100	RES 10 5% 1/8W FILM
R47	R85-0125-101	RES 100 5% 1/8W FILM
R48	R85-0004-363	RES,44.2K 1% 1/8W CHIP
R49	R85-0125-223	RES 22K 5% 1/8W FILM

Table 3. A4 Signal Processor Assembly Parts List (10303-2500 Rev. N) (Cont.)

Ref. Desig.	Part Number	Description
R50	R85-0004-366	RES 47.5K 1% 1/8W FLM
R51	R85-0004-381	RES 68.1K 1% 1/8W FLM
R52	R85-0125-223	RES 22K 5% 1/8W FILM
R53	R85-0004-201	RES 1000 1% 1/8W FLM
R54	R85-0004-201	RES 1000 1% 1/8W FLM
R55	R85-0125-223	RES 22K 5% 1/8W FILM
R56	R85-0125-103	RES 10K 5% 1/8W FILM
R57	R85-0125-104	RES 100K 5% 1/8W FILM
R58	R85-0004-401	RES 100K 1% 1/8W FLM
R59	R85-0125-103	RES 10K 5% 1/8W FILM
R60	R85-0125-103	RES 10K 5% 1/8W FILM
R61	R85-0004-201	RES 1000 1% 1/8W FLM
R62	R85-0125-101	RES 100 5% 1/8W FILM
R63	R85-0004-346	RES,29.4K 1% 1/8W CHIP
R64	R85-0125-101	RES 100 5% 1/8W FILM
R65	R85-0125-151	RES 150 5% 1/8W FILM
R66	R85-0125-101	RES 100 5% 1/8W FILM
R67	R85-0125-103	RES 10K 5% 1/8W FILM
R68	R85-0125-101	RES 100 5% 1/8W FILM
R69	R85-0125-103	RES 10K 5% 1/8W FILM
R71	R85-0125-244	RES 240K 5% 1/8W FILM
R72	R85-0125-103	RES 10K 5% 1/8W FILM
R73	R85-0125-103	RES 10K 5% 1/8W FILM
R74	R85-0125-100	RES 10 5% 1/8W FILM
R75	R85-0004-230	RES 2.0K 1% 1/8W SMD
R76	R85-0125-103	RES 10K 5% 1/8W FILM
R77	R85-0125-101	RES 100 5% 1/8W FILM
R78	R85-0125-101	RES 100 5% 1/8W FILM
R79	R85-0004-201	RES 1000 1% 1/8W FLM
R80	R85-0004-277	RES 6190 1% 1/8W FLM
R81	R85-0004-366	RES 47.5K 1% 1/8W FLM
R82	R85-0125-101	RES 100 5% 1/8W FILM
R83	R85-0125-101	RES 100 5% 1/8W FILM
R84	R85-0125-101	RES 100 5% 1/8W FILM
R85	R85-0125-101	RES 100 5% 1/8W FILM
R86	R85-0004-266	RES,4.75K 1% 1/8W CHIP
R88	R85-0125-101	RES 100 5% 1/8W FILM
R89	R85-0125-101	RES 100 5% 1/8W FILM
R90	R85-0125-101	RES 100 5% 1/8W FILM

Table 3. A4 Signal Processor Assembly Parts List (10303-2500 Rev. N) (Cont.)

Ref. Desig.	Part Number	Description
R91	R85-0125-150	RES 15 5% 1/8W, SMT
R92	R85-0125-150	RES 15 5% 1/8W, SMT
R93	R85-0125-150	RES 15 5% 1/8W, SMT
R94	R85-0125-150	RES 15 5% 1/8W, SMT
R95	R85-0125-103	RES 10K 5% 1/8W FILM
R96	R85-0004-266	RES,4.75K 1% 1/8W CHIP
R97	R85-0004-201	RES 1000 1% 1/8W FLM
R98	R85-0125-103	RES 10K 5% 1/8W FILM
R99	R85-0004-081	RES 68.1 1% 1/8W FLM
R100	R85-0125-101	RES 100 5% 1/8W FILM
R101	R85-0125-101	RES 100 5% 1/8W FILM
R102	R85-0125-101	RES 100 5% 1/8W FILM
R103	R85-0004-230	RES 2.0K 1% 1/8W SMD
R104	R85-0125-103	RES 10K 5% 1/8W FILM
R105	R85-0125-103	RES 10K 5% 1/8W FILM
R106	R85-0004-230	RES 2.0K 1% 1/8W SMD
R107	R85-0004-230	RES 2.0K 1% 1/8W SMD
R108	R85-0125-101	RES 100 5% 1/8W FILM
R109	R85-0125-101	RES 100 5% 1/8W FILM
R110	R85-0004-230	RES 2.0K 1% 1/8W SMD
R111	R85-0125-104	RES 100K 5% 1/8W FILM
R112	R85-0125-104	RES 100K 5% 1/8W FILM
R114	R85-0004-201	RES 1000 1% 1/8W FLM
R115	R85-0004-201	RES 1000 1% 1/8W FLM
R120	R85-0125-163	RES 16K 5% 1/8W FILM
R121	R85-0125-106	RES 10M 5% 1/8W FILM
R122	R85-0125-100	RES 10 5% 1/8W FILM
R123	R85-0125-100	RES 10 5% 1/8W FILM
R124	R85-0125-100	RES 10 5% 1/8W FILM
R125	R85-0004-230	RES 2.0K 1% 1/8W SMD
R127	R85-0004-230	RES 2.0K 1% 1/8W SMD
R128	R85-0004-000	RES ZERO OHM 1/8W FILM
R129	R85-0004-000	RES ZERO OHM 1/8W FILM
R130	R85-0004-000	RES ZERO OHM 1/8W FILM
R131	R85-0125-223	RES 22K 5% 1/8W FILM
U1	I26-0034-004	IC 2KX8 DPRAM W/INT PLCC
U2	I26-0021-101	32K X 8 RAM SMT
U4	I01-5000-074	IC,CMOS D-FF,SOIC
U5	10181-8017	PROG. TN 83C51FA PLCC MIC

Table 3. A4 Signal Processor Assembly Parts List (10303-2500 Rev. N) (Cont.)

Ref. Desig.	Part Number	Description
U6	I01-5000-573	8-BIT LATCH (74HC573DW)
U7	I25-0033-006	128K X 8 FLASH EPROM, IC
U8	I01-5000-368	IC,CMOS HEX INV,SOIC
U10	I01-5000-138	3 TO 8 DECODER (74HC138D)
U11	I01-5000-000	QUAD NAND-GATE (74HC00D)
U12	I01-5000-174	HEX D-FF (74HC174D)
U13	I26-0029-002	2KX16 DP RAM IDT7133L90J
U14	I01-5000-032	IC 74HC32AD PLSTC CMOS
U15	I25-0042-005	IC, 256K X 8 FLASH MEMORY
U16	I01-5000-002	QUAD N0R-GATE (74HC02)
U17	I01-5000-000	QUAD NAND-GATE (74HC00D)
U18	I01-5000-368	IC,CMOS HEX INV,SOIC
U19	10181-8017	PROG. TN 83C51FA PLCC MIC
U20	I01-5000-573	8-BIT LATCH (74HC573DW)
U21	I26-0021-101	32K X 8 RAM SMT
U23	I01-5000-299	8-BIT SHIFT REG (74HC299D
U24	I01-6000-032	IC QUAD 2-IN OR SMT
U25	I25-0032-002	64KX16 UV EPROM
U26	I27-0019-003	DSP (TMS320C25FNA)
U27	I01-6000-008	QUAD AND-GATE (74AC08D)
U29	I01-6000-240	OCTAL INV/BUFFER 74AC240
U30	I26-0017-007	8K X 8 SRAM (MCM6264NJ35)
U31	I26-0017-007	8K X 8 SRAM (MCM6264NJ35)
U32	I01-5000-139	DUAL 2-4 DECODER (74HC139
U34	10181-8017	PROG. TN 83C51FA PLCC MIC
U35	I26-0034-004	IC 2KX8 DPRAM W/INT PLCC
U36	I01-5000-573	8-BIT LATCH (74HC573DW)
U37	I25-0033-006	128K X 8 FLASH EPROM, IC
U38	I01-5000-000	QUAD NAND-GATE (74HC00D)
U41	I30-0048-003	IC, LP DUAL OP AMP (MC331
U42	I03-0028-001	DUAL 12-BIT DAC DAC8222E
U43	I06-0009-301	DUAL SPDT SWITCH DG303AB
U44	I01-5000-574	8-BIT D-FF (74HC574DW)
U45	I30-0048-003	IC, LP DUAL OP AMP (MC331
U46	I03-0027-001	12-BIT ADC (AD7870LP)
U47	I03-0027-001	12-BIT ADC (AD7870LP)
U48	I30-0048-005	IC, LP QUAD OP AMP (MC331
U49	I09-0011-101	DUAL 4 CH MUX (DG509ACWE)
U50	I06-0009-301	DUAL SPDT SWITCH DG303AB

Table 3. A4 Signal Processor Assembly Parts List (10303-2500 Rev. N) (Cont.)

Ref. Desig.	Part Number	Description
U51	I12-0016-001	REG, LOW PWR 12V
U52	I12-0010-205	REG, LOW POWER -5V
U53	I01-5000-574	8-BIT D-FF (74HC574DW)
U54	I09-0011-101	DUAL 4 CH MUX (DG509ACWE)
U55	I30-0048-005	IC, LP QUAD OP AMP (MC331
U56	I03-0020-101	8-BIT SERIAL ADC TLC548I
U57	I03-0020-101	8-BIT SERIAL ADC TLC548I
U58	I01-5000-406	PLL WITH VCO (74HC4046AD)
U59	I70-0005-003	PROG FREQ SYNTH (MC145158
U60	I01-5000-390	DUAL 4STG CNTR (2/5)(74HC
U61	I01-5000-161	ASYNC BIN PRST CNTR(74HC1
U63	I01-6000-032	IC QUAD 2-IN OR SMT
U64	I25-0032-002	64KX16 UV EPROM
U65	I27-0019-003	DSP (TMS320C25FNA)
U66	I01-6000-240	OCTAL INV/BUFFER 74AC240
U67	I01-5000-139	DUAL 2-4 DECODER (74HC139
U68	I01-6000-000	QUAD NAND-GATE (74AC00D)
U69	I26-0021-102	32K X 8 SRAM (HM62832JP-3
U70	I26-0021-102	32K X 8 SRAM (HM62832JP-3
U71	I25-0047-001	IC,256K X 16 UV EPROM 150
U72	I01-5000-573	8-BIT LATCH (74HC573DW)
U73	I01-6000-074	DUAL D-FF (74AC74D)
U74	I01-5000-004	HEX INVERTER (74HC04D)
U75	I27-0030-001	16-BIT MICRO TN80C186EA-1
U76	I01-5000-573	8-BIT LATCH (74HC573DW)
U77	I01-5000-573	8-BIT LATCH (74HC573DW)
U78	I26-0037-004	IC 128KX8 SRAM 628128 SMD
U79	I26-0037-004	IC 128KX8 SRAM 628128 SMD
U80	I26-0029-002	2KX16 DP RAM IDT7133L90J
U81	I01-6000-074	DUAL D-FF (74AC74D)

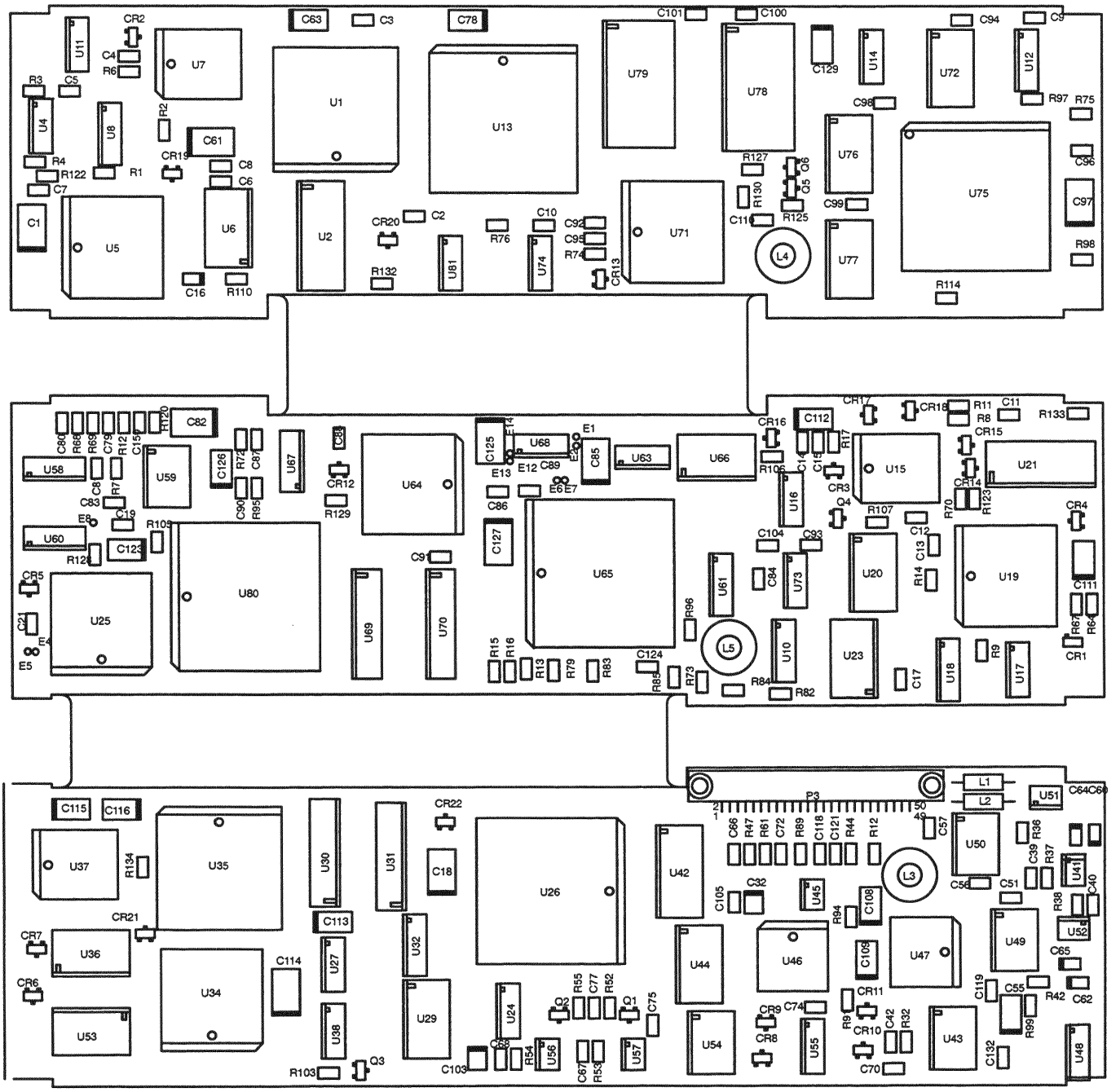


Figure 1. A4 Signal Processor Assembly Component Location Diagram (10303-2500 Rev. C) (Sheet 1 of 2)

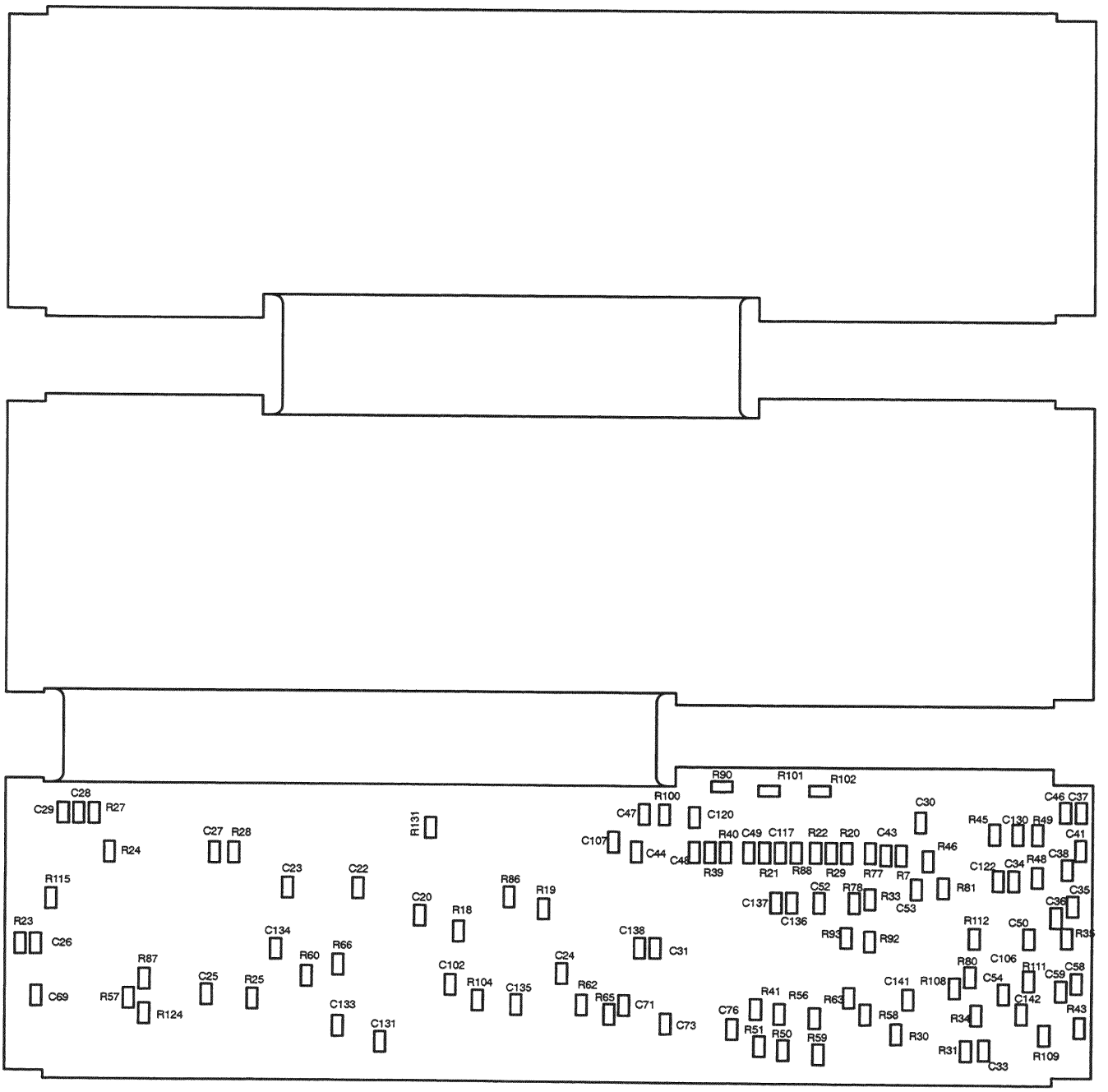
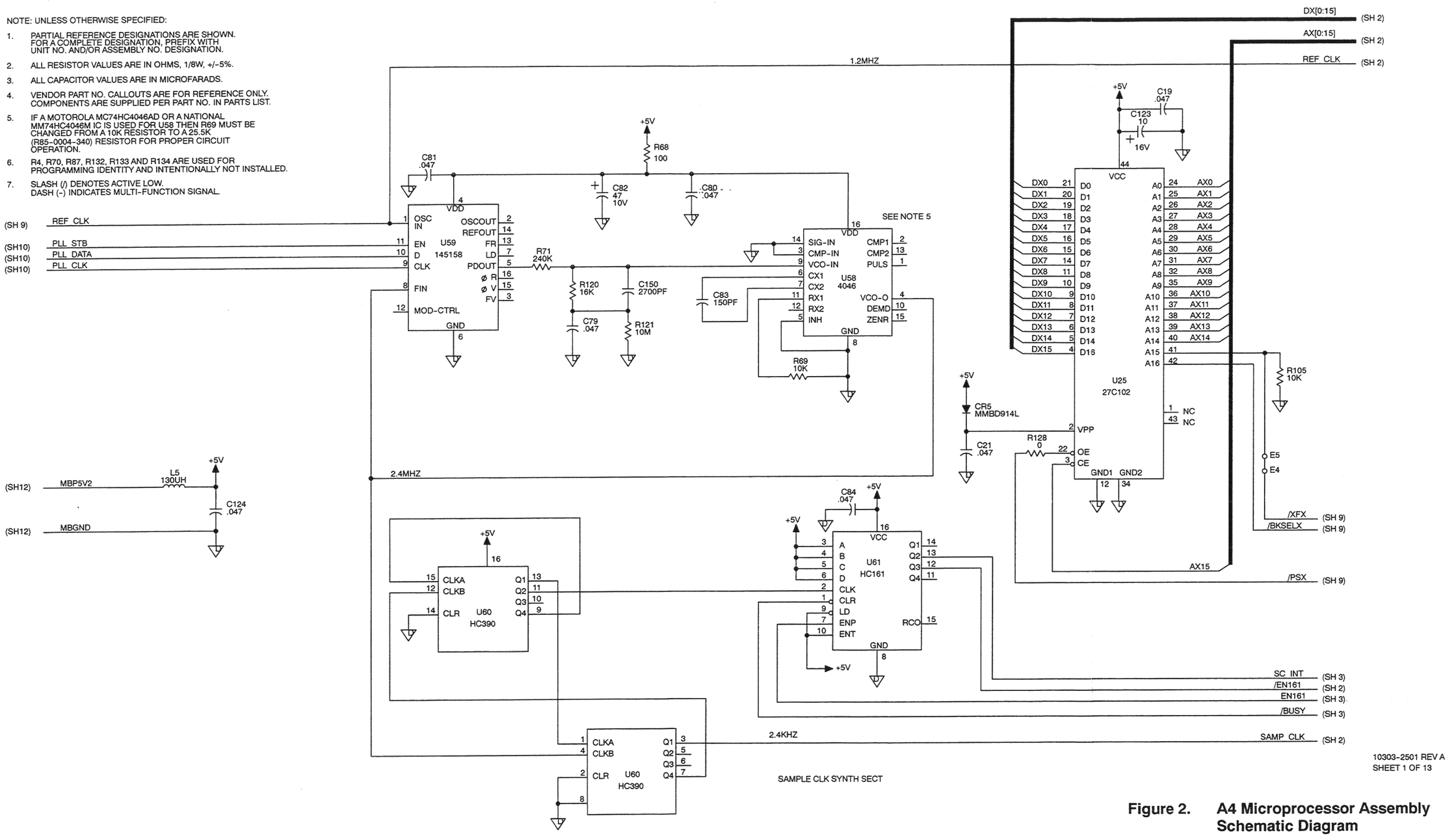


Figure 1. A4 Signal Processor Assembly Component Location Diagram (10303-2500 Rev. C) (Sheet 2 of 2)

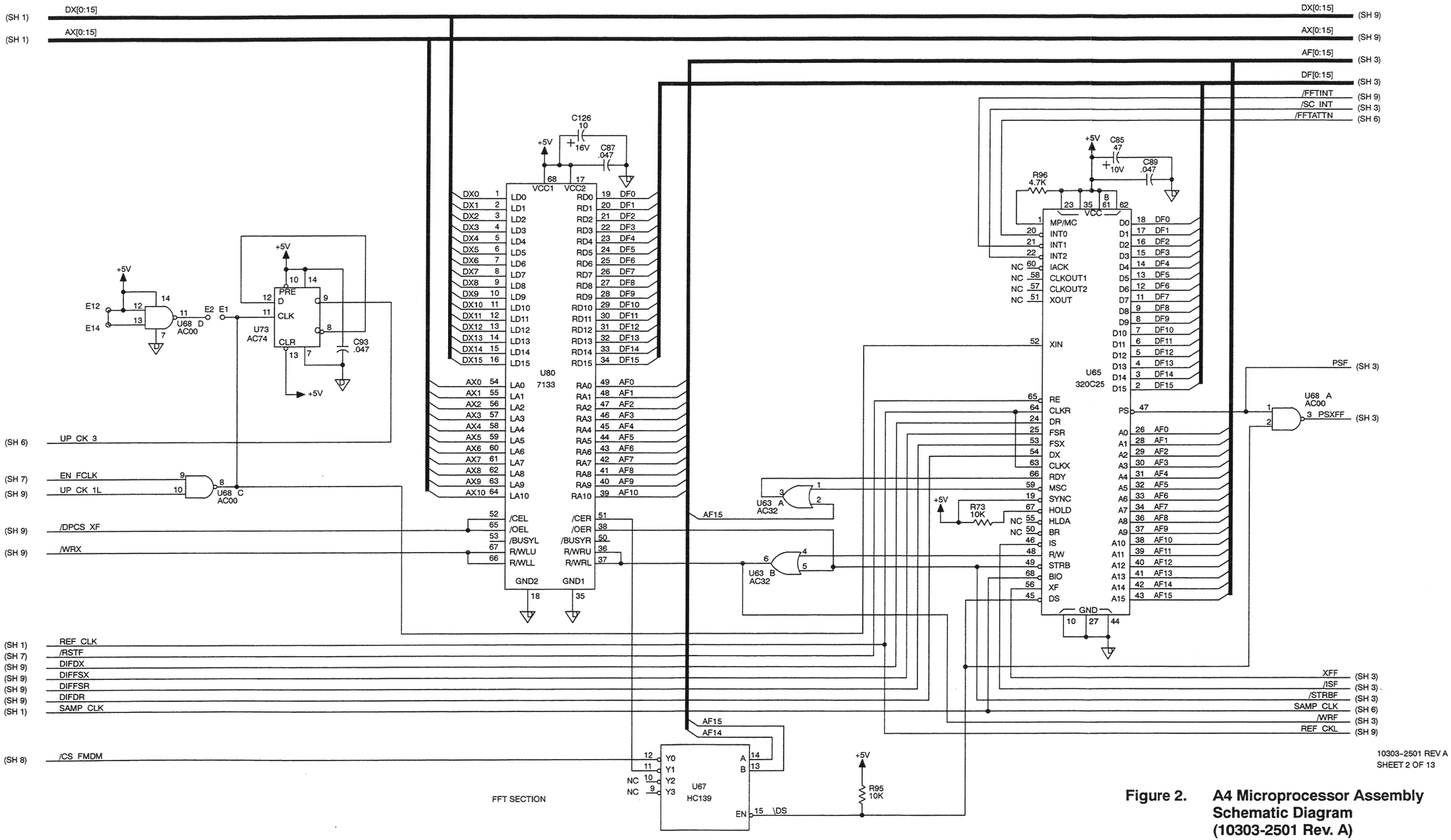
NOTE: UNLESS OTHERWISE SPECIFIED:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR A COMPLETE DESIGNATION, PREFIX WITH UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.
2. ALL RESISTOR VALUES ARE IN OHMS, 1/8W, +/-5%.
3. ALL CAPACITOR VALUES ARE IN MICROFARADS.
4. VENDOR PART NO. CALLOUTS ARE FOR REFERENCE ONLY. COMPONENTS ARE SUPPLIED PER PART NO. IN PARTS LIST.
5. IF A MOTOROLA MC74HC4046AD OR A NATIONAL MM74HC4046M IC IS USED FOR U58 THEN R69 MUST BE CHANGED FROM A 10K RESISTOR TO A 25.5K (R85-0004-340) RESISTOR FOR PROPER CIRCUIT OPERATION.
6. R4, R70, R87, R132, R133 AND R134 ARE USED FOR PROGRAMMING IDENTITY AND INTENTIONALLY NOT INSTALLED.
7. SLASH (/) DENOTES ACTIVE LOW. DASH (-) INDICATES MULTI-FUNCTION SIGNAL.



10303-2501 REV A
SHEET 1 OF 13

Figure 2. A4 Microprocessor Assembly Schematic Diagram (10303-2501 Rev. A) (Sheet 1 of 13)



10303-2501 REV A
SHEET 2 OF 13

Figure 2. A4 Microprocessor Assembly Schematic Diagram (10303-2501 Rev. A) (Sheet 2 of 13)

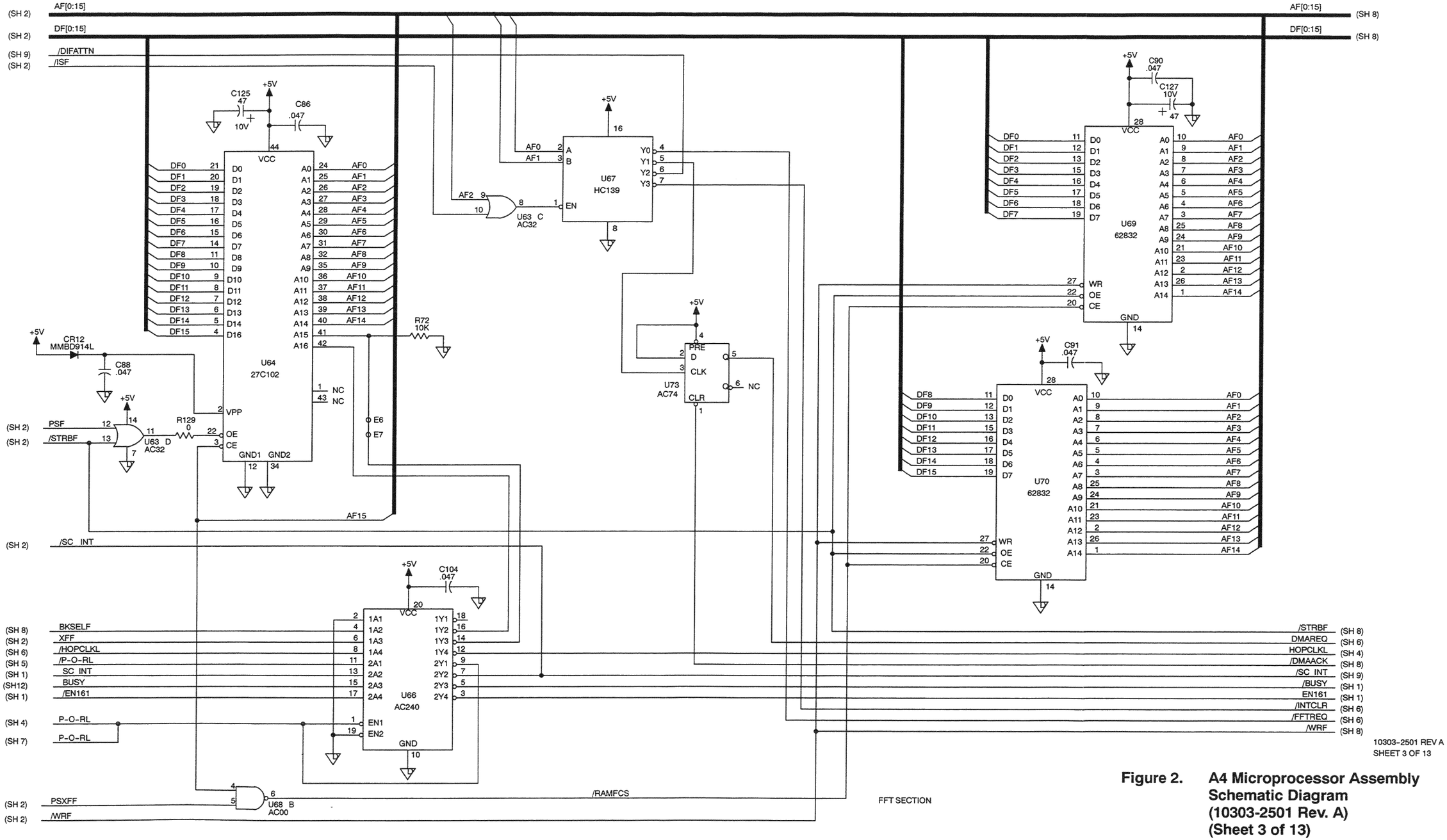


Figure 2. A4 Microprocessor Assembly Schematic Diagram (10303-2501 Rev. A) (Sheet 3 of 13)

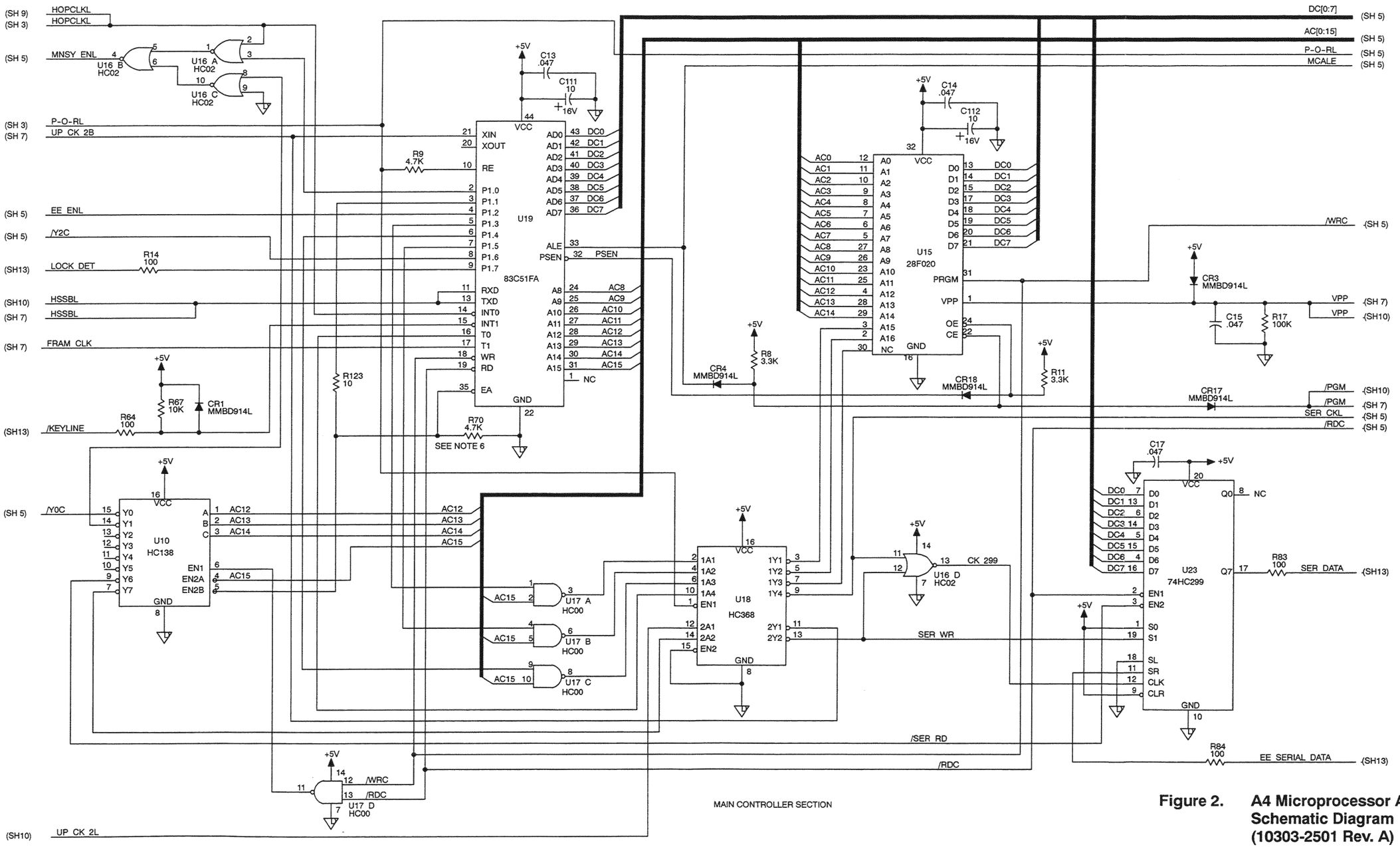
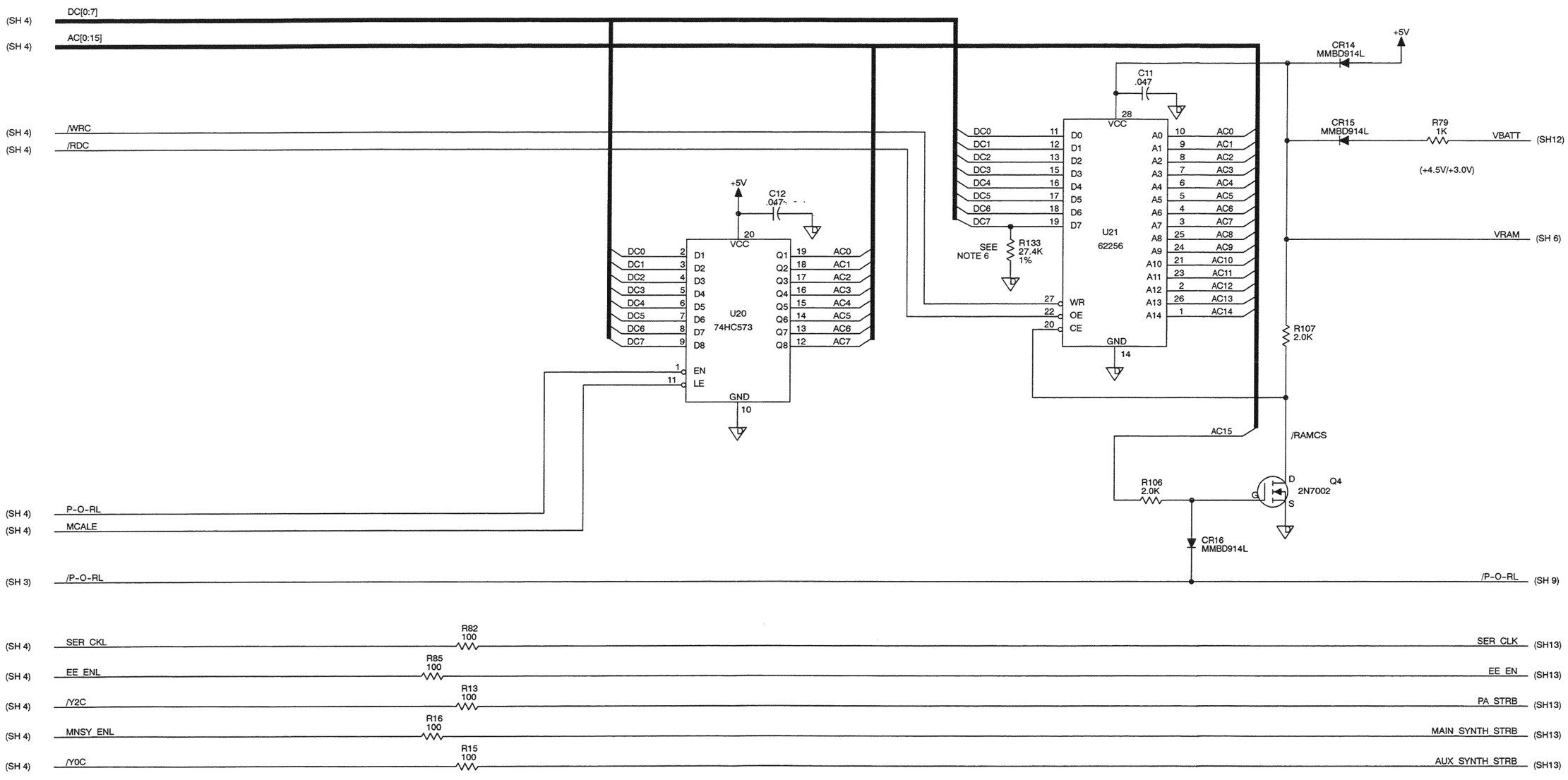


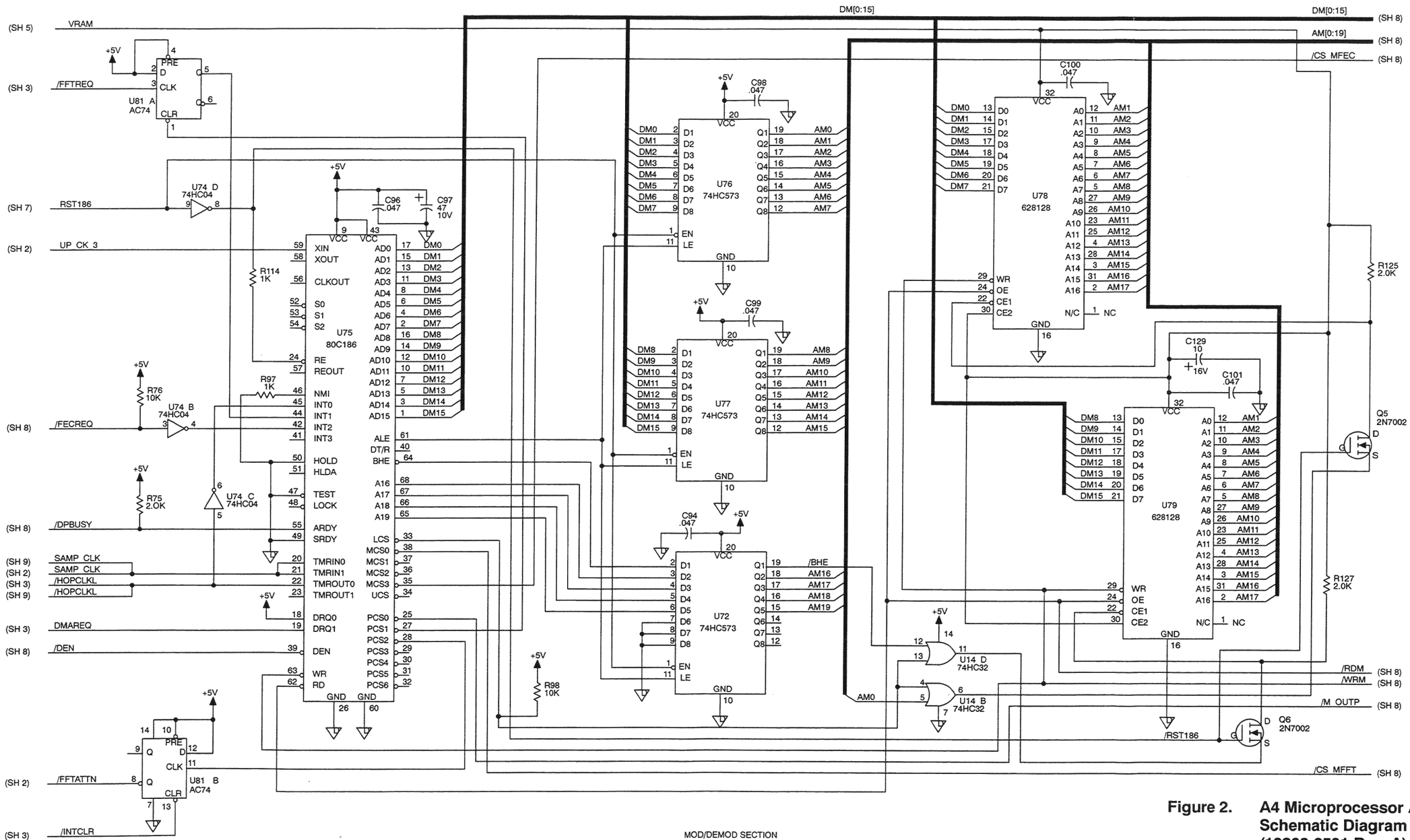
Figure 2. A4 Microprocessor Assembly Schematic Diagram (10303-2501 Rev. A) (Sheet 4 of 13)



10303-2501 REV A
SHEET 5 OF 13

Figure 2. A4 Microprocessor Assembly Schematic Diagram (10303-2501 Rev. A) (Sheet 5 of 13)

MAIN CONTROLLER SECTION



10303-2501 REV A
SHEET 6 OF 13

Figure 2. A4 Microprocessor Assembly Schematic Diagram (10303-2501 Rev. A) (Sheet 6 of 13)

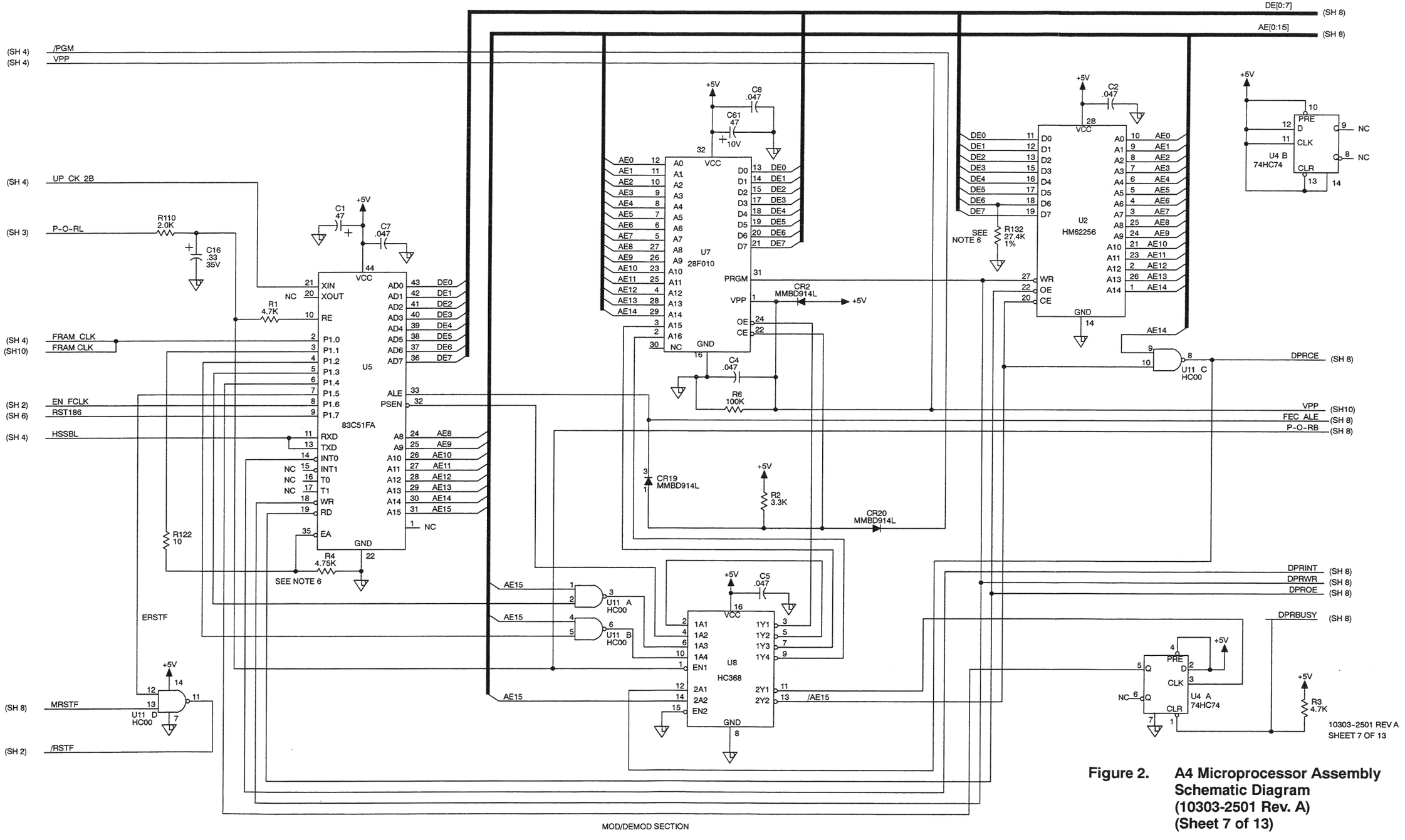


Figure 2. A4 Microprocessor Assembly Schematic Diagram (10303-2501 Rev. A) (Sheet 7 of 13)

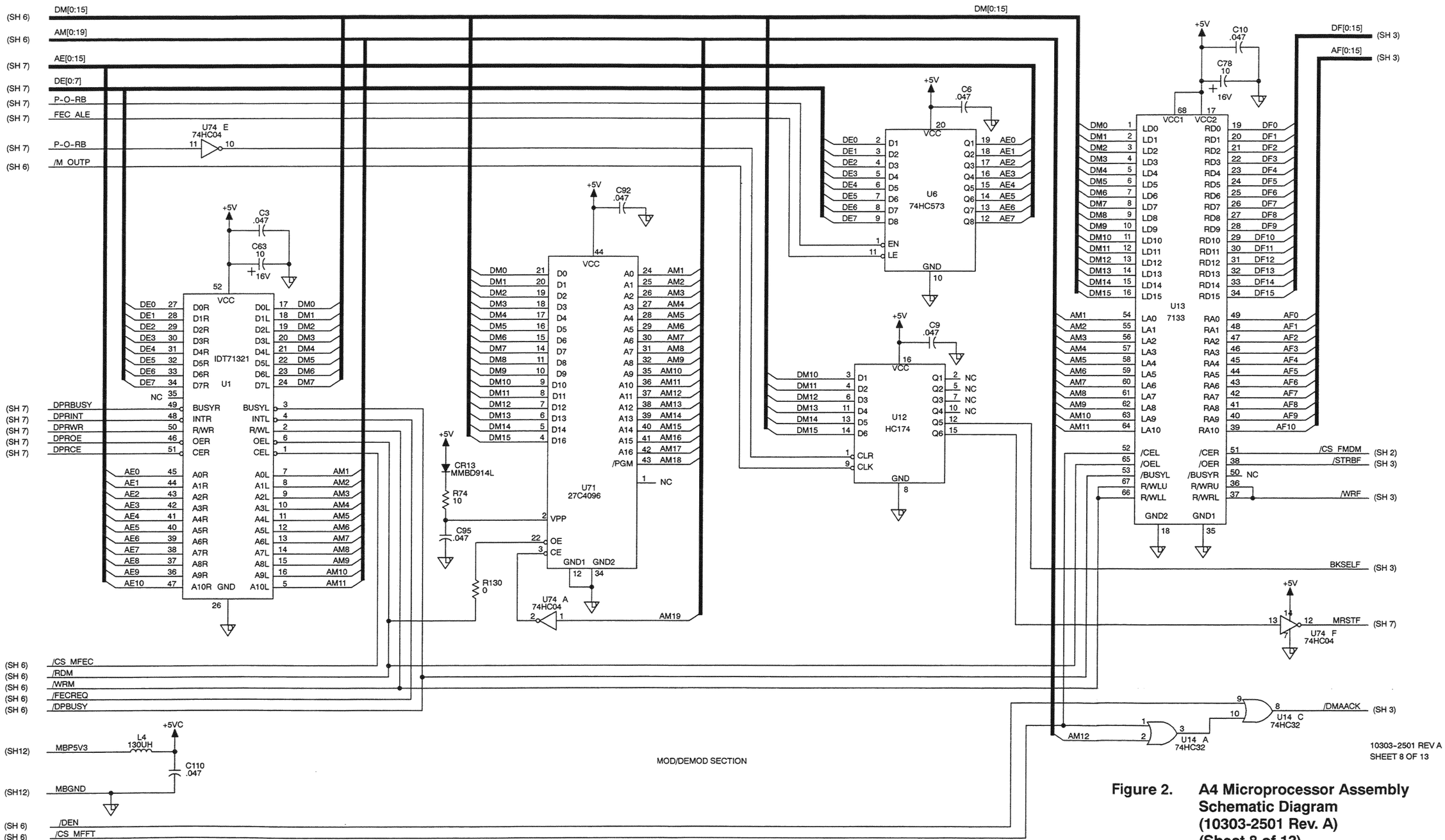


Figure 2. A4 Microprocessor Assembly Schematic Diagram (10303-2501 Rev. A) (Sheet 8 of 13)

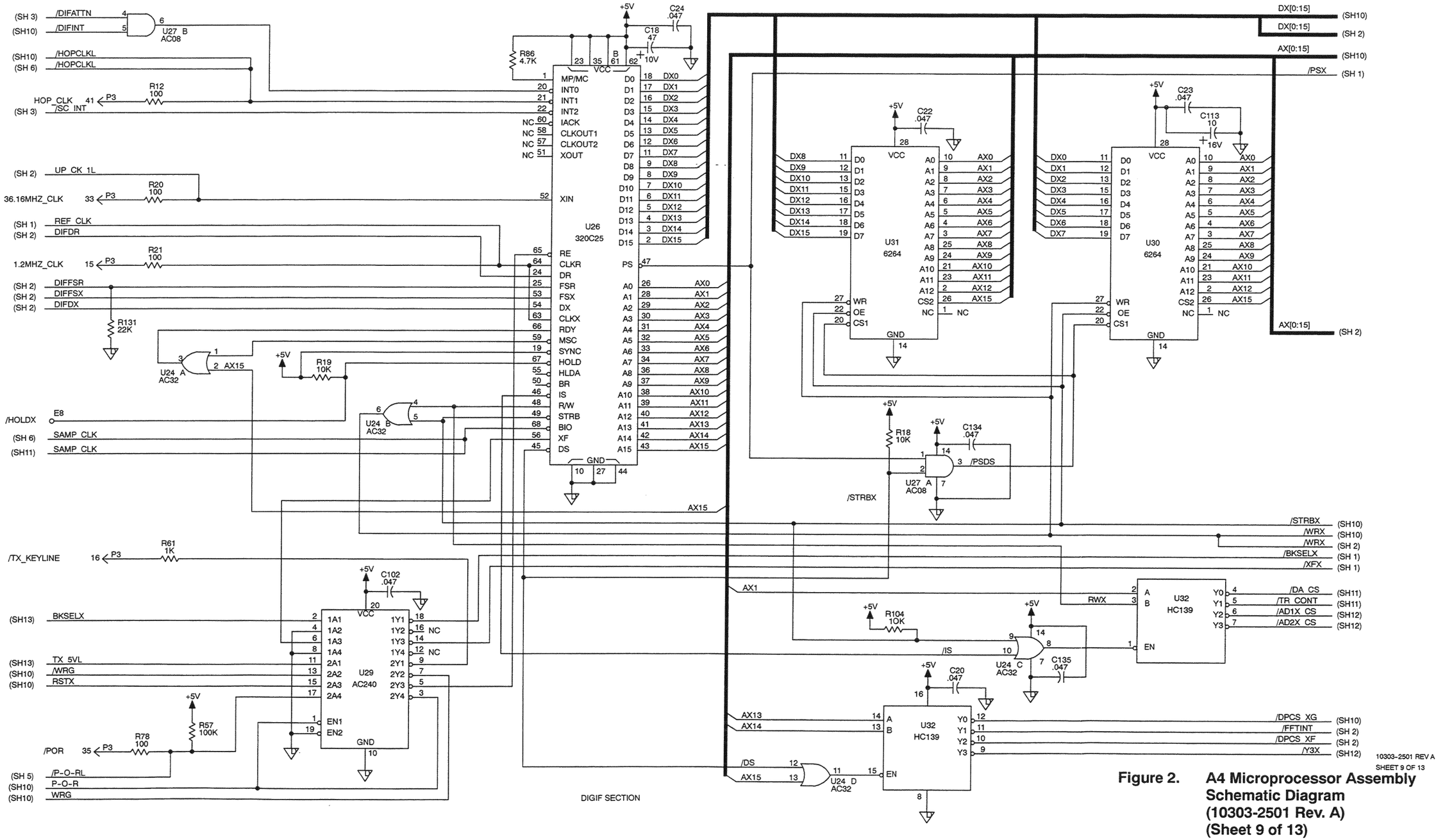
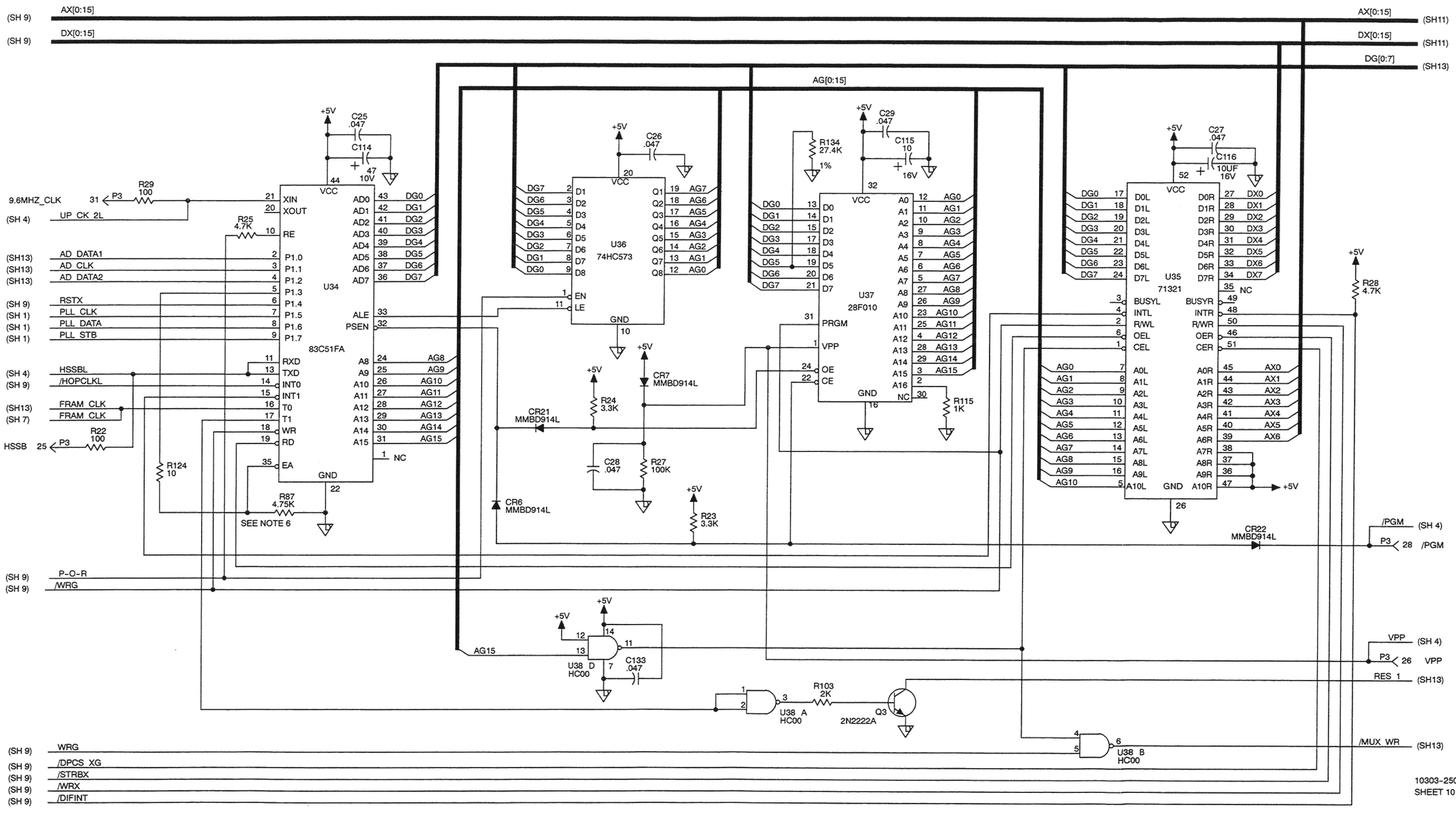


Figure 2. A4 Microprocessor Assembly Schematic Diagram (10303-2501 Rev. A) (Sheet 9 of 13)



DIGIF SECTION

Figure 2. A4 Microprocessor Assembly Schematic Diagram (10303-2501 Rev. A) (Sheet 10 of 13)

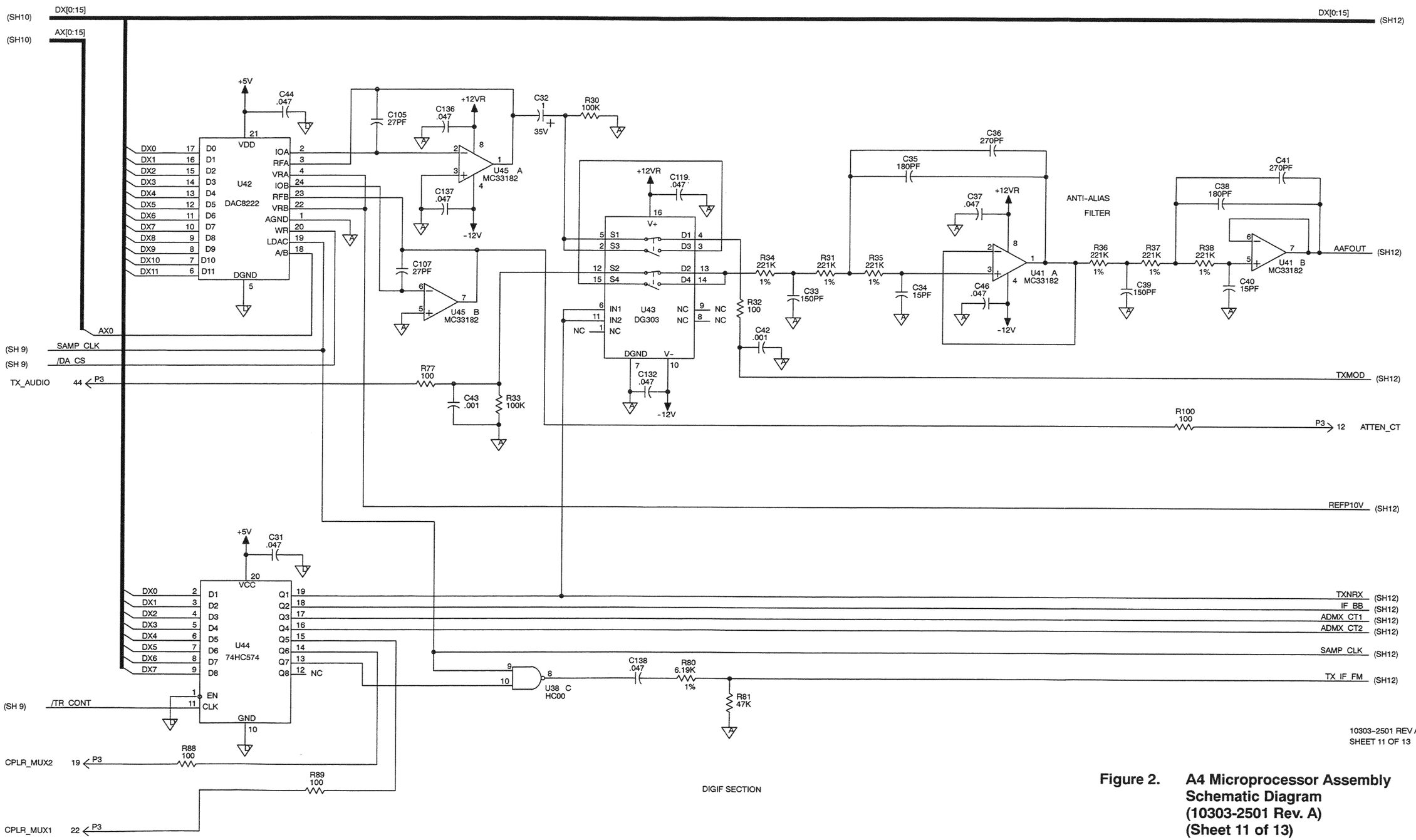


Figure 2. A4 Microprocessor Assembly Schematic Diagram (10303-2501 Rev. A) (Sheet 11 of 13)

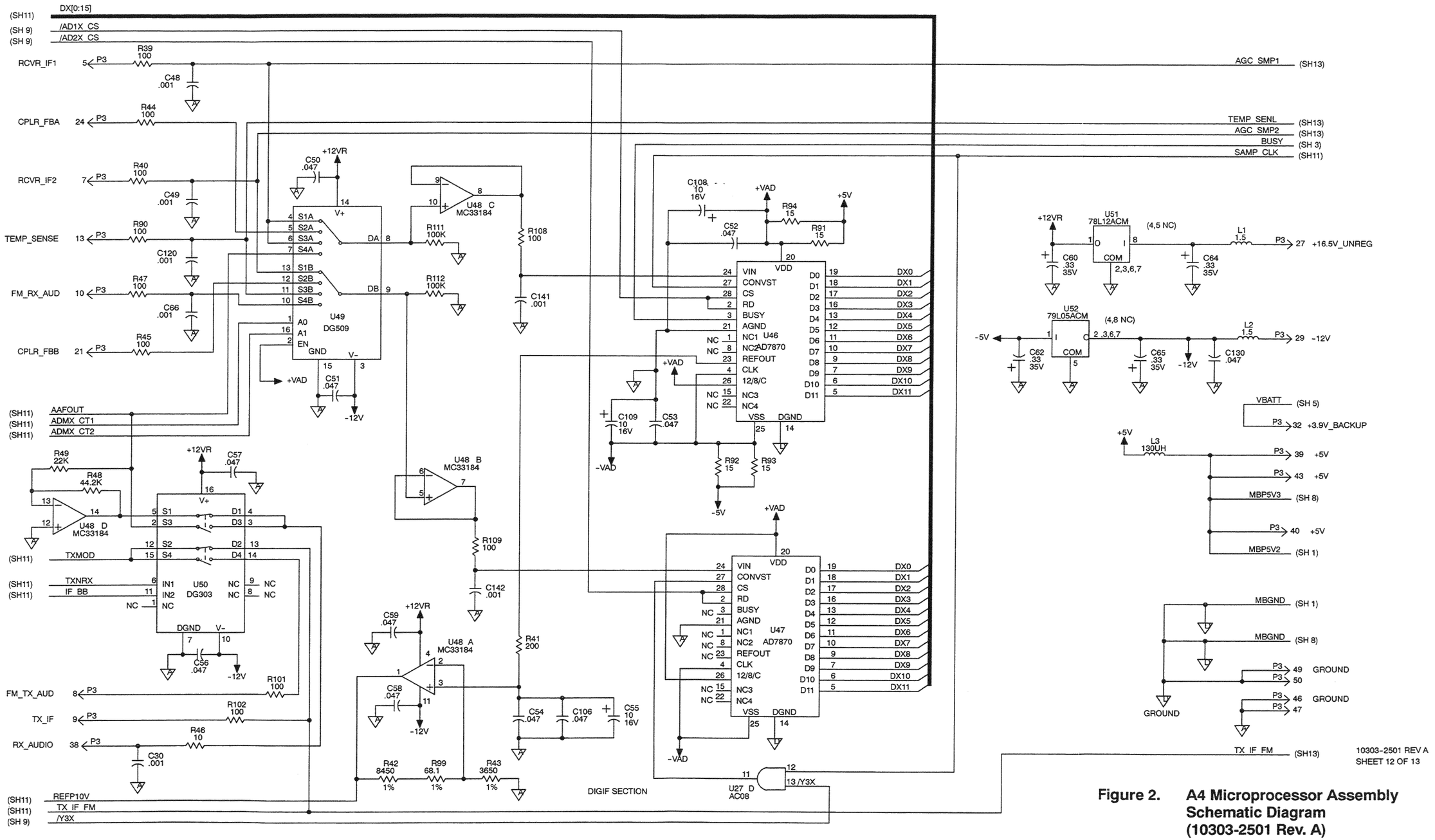
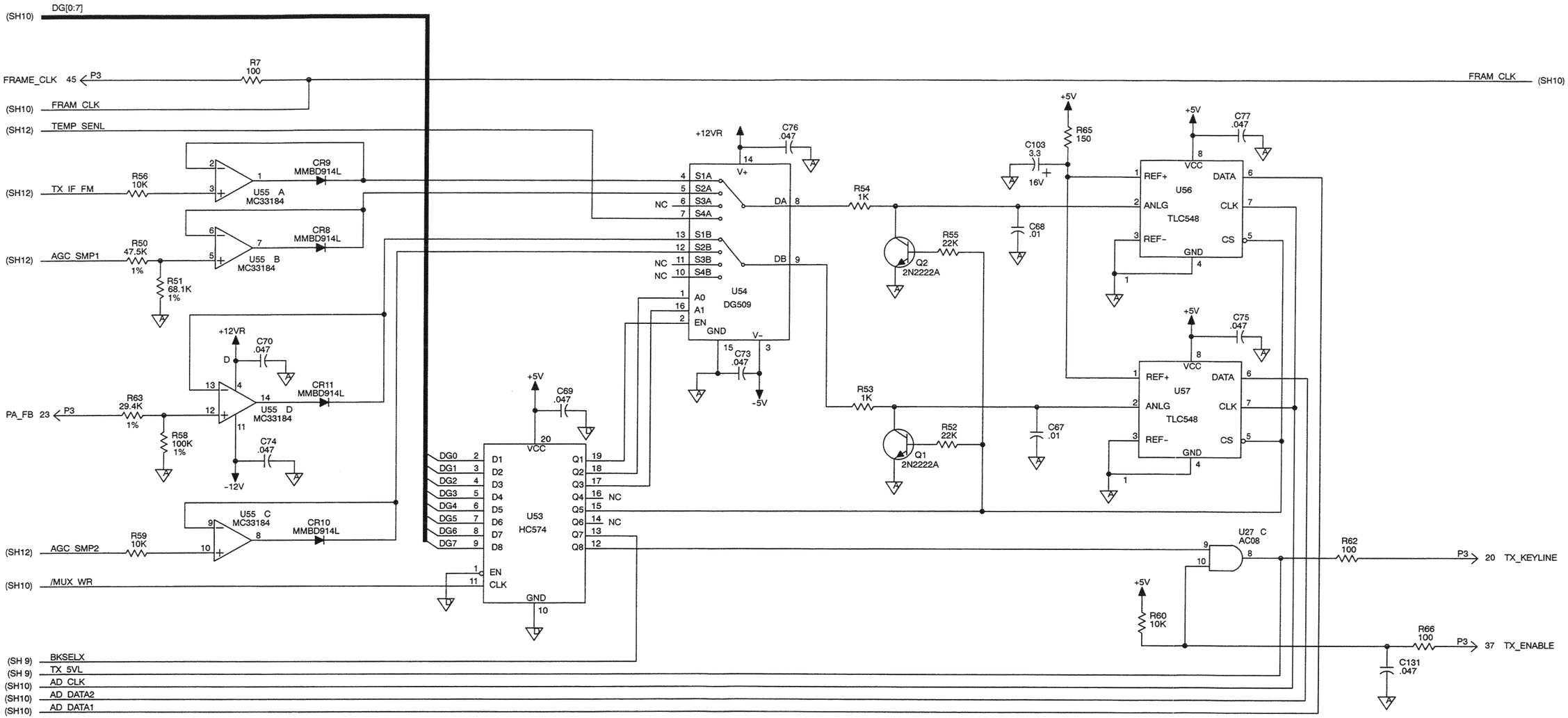


Figure 2. A4 Microprocessor Assembly Schematic Diagram (10303-2501 Rev. A) (Sheet 12 of 13)



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DIGIF SECTION

Figure 2. A4 Microprocessor Assembly Schematic Diagram (10303-2501 Rev. A) (Sheet 13 of 13)

MAIN CONTROLLER

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LIST OF FIGURES

LIST OF TABLES

A4 SIGNAL PROCESSOR ASSEMBLY MAIN CONTROLLER SUBSECTION

1. GENERAL DESCRIPTION

The Main Controller portion of the A4 Signal Processor Assembly is the source of all control and command signals in the AN/PRC-138. The Main Controller performs the following functions:

- Initializes each module in the R/T. Current revisions of each module present and reporting are stored.
- Analyzes front panel and remote commands using an ASCII protocol. In ALE, only commands not applicable to the ALE function are analyzed.
- Keeps the time of day.
- Controls the internal power amplifier and internal antenna coupler over a serial bus.
- Loads the synthesizer data over the same serial bus.
- Reads the temperature correction data for the DCXO from the serial EEPROM on the Reference Generator Assembly.
- Stores the data for 100 SSB/ALE channels.
- Stores the data for 10 hop nets.
- Regulates temporary channel parameters. These are valid for either the current channel or the current mode of operation (that is, modem, DV, AVS, CW, etc.). Temporary parameters include frequency, mode, and bandwidth.
- Stores and monitors the selected mode of operation, and temporarily disables conflicting modes.
- Regulates keyline (MIC, AUX, DATA, ALE, CW).
- Stores the states of various parameters (i.e., power, data/remote async, modem presets, encryption keys) and other functions that are restored upon power-up.
- Coordinates the complete R/T self-test.

2. INTERFACE CONNECTIONS

See the A4 Signal Processor Assembly section for interface connections.

3. TECHNICAL DESCRIPTION

Figure 1 is a simplified block diagram of the Main Controller portion of the A4 Signal Processor Assembly. A parts list, component location diagram, and schematic diagram are included at the end of this section.

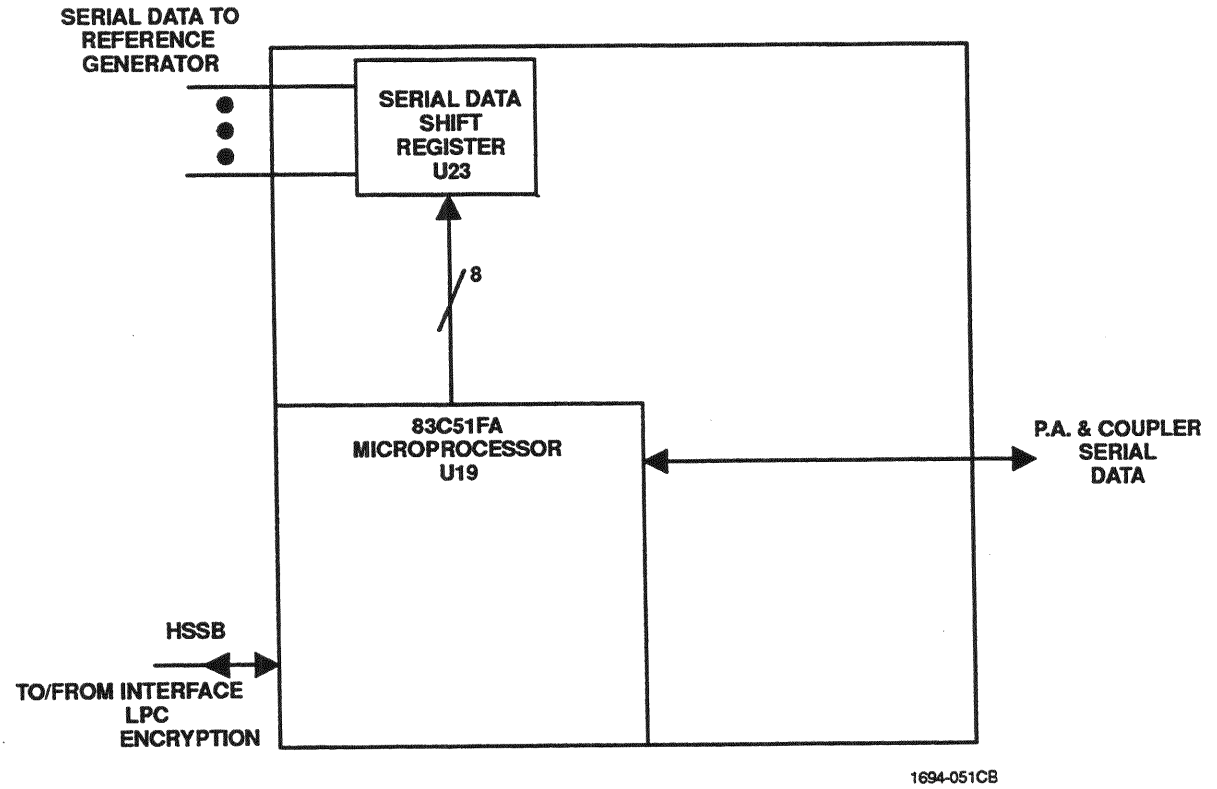

Figure 1. Main Controller Module Block Diagram

3.1 High-Speed Serial Bus

All control signals within the AN/PRC-138, with the exception of synthesizer data, power amplifier, and antenna coupler commands, are sent by the 83C51FA microprocessor U19 over the internal high-speed serial bus. This half-duplex, 300-kbps data bus connects all of the 83C51FA microprocessors within the R/T. A proprietary Harris protocol is used on this bus.

3.2 Synthesizer and PA/Coupler Serial Data

The 83C51FA microprocessor U19 loads frequency data for the synthesizer and relay settings for the internal power amplifer and antenna coupler assemblies into the HC299 shift register (U23) by writing to the address 7XXXH. This data is clocked onto the serial data line (P3-2) to both the synthesizer and power amplifier and antenna coupler assemblies. The power amplifer and antenna coupler assemblies read the data and strobes it on the rising edge of port pin P1-6 (U19-8). Writing to an address of 1XXXH strobes the data into the synthesizer. The port pin T0 (U19-16) is used to clock the shift register.

This shift register also reads in temperature correction data from the serial EEPROM on the A6 Synthesizer/Reference Generator Assembly to the serial input of the shift register (U23-11). This data represents the frequency error in the 9.6 MHz DXCO for a given temperature. The Main Controller uses a measure of the temperature from the A/D and this correction data to calculate an LO offset to correct for the error in the standard. Port pin P1-2 (U19-4) enables the EEPROM. Reading an address in the 6XXXH range reads the data from the shift register.

3.3 Bank Switching

U15 is a 256Kx8 FLASH ROM. U17 and U18 gate three of the microprocessor port pins to control the A15, A16, and A17 address lines of EPROM U15. The lower 32 Kbytes of the ROM are always accessible to the microprocessor in the 0000 to 7FFF address space. The microprocessor may map any 32-Kbyte section of FLASH ROM into the 8000 to FFFF address space. This mapping is defined in table 1.

Table 1. Address Space Mapping for FLASH EPROM U15

Bank No.	U1-7 BS3	U1-6 BS2	U1-5 BS1	Microprocessor Address Space	FLASH ROM Address Space
LOW	X	X	X	0000 to 7FFF	0000 to 7FFF
0	0	0	0	8000 to FFFF	0000 to 7FFF
1	0	0	1	8000 to FFFF	8000 to FFFF
2	0	1	0	8000 to FFFF	10000 to 7FFFF
3	0	1	1	8000 to FFFF	18000 to 1FFFF
4	1	0	0	8000 to FFFF	20000 to 27FFF
5	1	0	1	8000 to FFFF	28000 to 2FFFF
6	1	1	0	8000 to FFFF	30000 to 37FFF
7	1	1	1	8000 to FFFF	38000 to 3FFFF

4. TESTING AND ALIGNMENT

This module requires no regular adjustments or alignments.

5. BITE FAULTS AND TROUBLESHOOTING

The self-test fault codes for the Main Controller portion of the A4 Signal Processor Assembly are shown in table 2.

The tests and faults for the Main Controller subsection of the Signal Processor Assembly are described in greater detail in the subsections that follow.

Table 2. A4 Signal Processor Assembly Fault Codes

Code	Fault
42	Non-destructive internal RAM fault
43	ROM checksum fault
44	Non-destructive external RAM fault

5.1 Fault 42 – Non-destructive Internal RAM Fault

This fault indicates that the internal RAM of U19 is faulty. Replace U19.

5.2 Fault 43 – ROM Checksum Fault

The 83C51 microprocessor detects a checksum error in its flash EPROM. Check the following on the A4 Signal Processor (10303-2500) Assembly:

a. Check address lines and bank-switching circuitry U17 and U18. It is unlikely that this part of the module would function if problems existed on these lines.

b. Check for short and open circuits on all address and data lines.

c. There should be +5 Vdc on U15-1 during normal operation, and +12.5 Vdc on U15-1 during EPROM programming.

d. If no problems are found in the previous steps, replace U15.

5.3 Fault 44 – Non-destructive External RAM Fault

Perform the following non-destructive RAM test to indicate a faulty RAM:

a. Check chip-enable pin U21-20; observe whether it pulses low during BITE.

b. Check activity on all address and data lines during BITE.

c. If no problems are found in the previous steps, replace U21.

DIGITAL IF/AGC

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A4 SIGNAL PROCESSOR ASSEMBLY DIGITAL IF/AGC SUBSECTION

1. GENERAL DESCRIPTION

The Digital IF Assembly contains a Texas Instruments TMS320 digital signal processor, an Intel 80C51FA microcontroller, and assorted ICs (A/D converters, D/A converter, analog switches, latches, etc.). The Digital IF processor (TMS320 U26) is responsible for transmit IF generation and receive audio reconstruction, and, in cooperation with the U34 AGC Processor, power amplifier monitoring and radio reference temperature monitoring.

The AGC processor (80C51FA U34) is responsible for receive automatic gain control (AGC), transmit gain control (TGC) and audio level control (ALC). It also interfaces the Digital IF processor with the other processors in the radio.

2. INTERFACE CONNECTIONS

See the A4 Signal Processor Assembly section for the Digital IF/AGC interface connections.

3. TECHNICAL DESCRIPTION

3.1 Digital IF Assembly

3.1.1 Digital IF – Receive Mode

Figure 1 is a block diagram of the Digital IF SSB/CW receive mode. The received RF signal, after being mixed down to the 30 kHz (36 kHz modem) third IF by the A5 Assembly, is passed to the A4 Signal Processor Assembly at P3-5. The IF signal passes through switch U49 and buffer amp U48C. From U48C the IF is sent to A/D converter U46 where the 12 bit digital IF is placed on the data bus. The IF signal at this point is a 6 kHz digital representation which is then subject to the following software processing by U26. The high-gain, 6 kHz, IF is sent through an operator-selected bandpass filter and undergoes AGC processing with the 80C31 microprocessor serving as part of the control loop. The signal is then mixed down to bandbase audio frequency using a digitally-generated local oscillator. It is then low pass filtered and limited. From the data bus the digital representation of the audio is input to the D/A converter U42. Now an analog signal, the audio is buffered (U45A) and switched through U43 to the anti-alias filter U41 for reconstruction. The RX audio is then switched through U50 to the front panel via P3-38.

In FM mode, the received RF signal is mixed down to audio by the A5 Assembly, and passed directly to the A4 Signal Processor Assembly. Figure 2 is a block diagram of the Digital IF FM receive mode. The unfiltered FM audio is first presented to the 12 bit analog-to-digital converter U46. From this point on, the signal undergoes only digital processing. The signal is then attenuated by 24 dB and AGC is applied. As shown in the block diagram, both Tone Squelch and Noise Squelch modes use the signal at this point to determine squelch activity on the signal after the signal has been bandpass filtered (cascaded low and high pass) to between 288 Hz and 2.9 kHz. Both squelch modes consist of a bandpass filter, an integrator, and a threshold circuit to activate/deactivate squelch. After squelch has been applied, the signal is converted back to analog by U42, filtered by a 7 kHz anti-aliasing filter U41 and the result is processed FM audio.

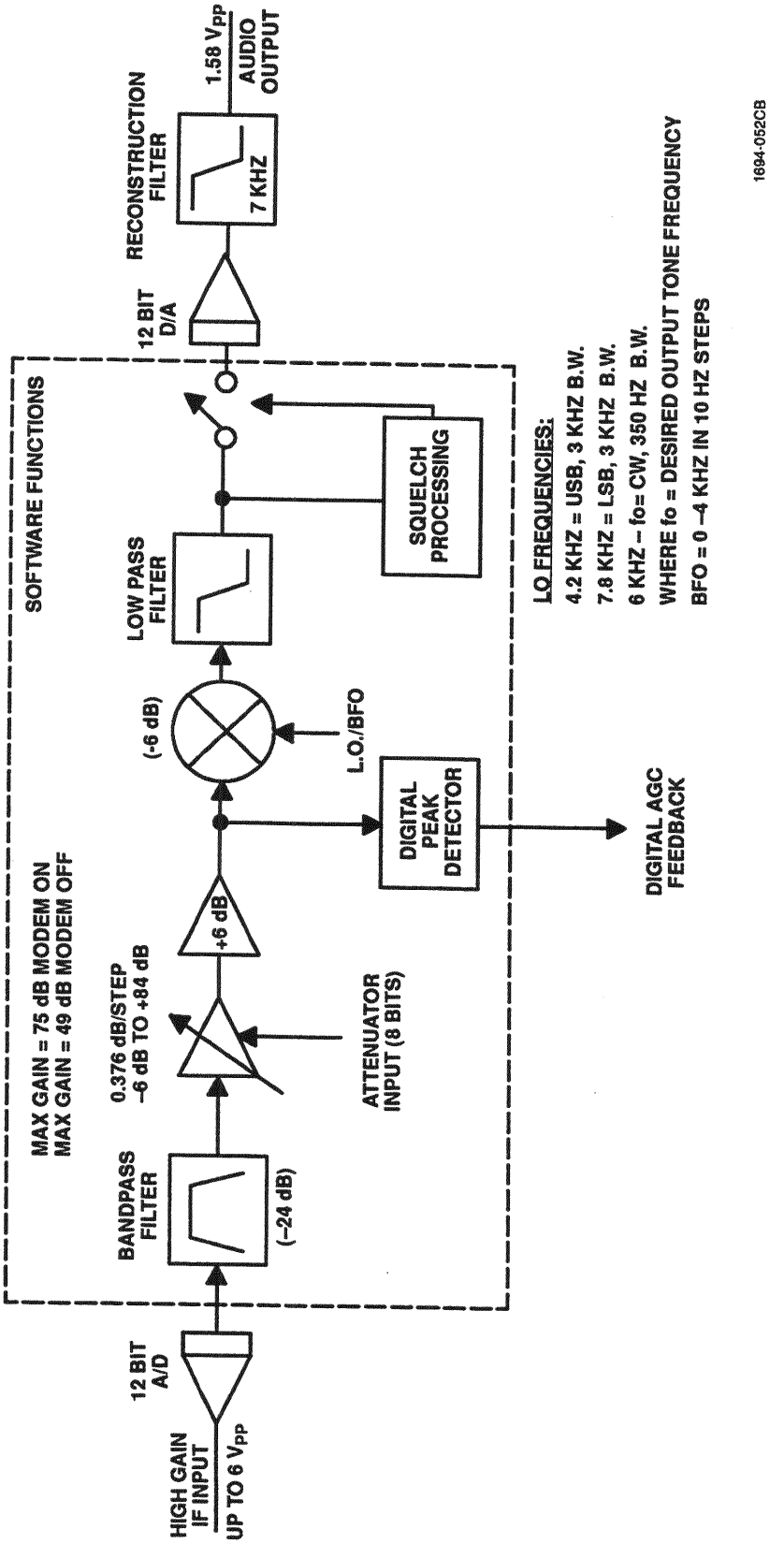


Figure 1. Digital IF – SSB/CW Receive Mode Block Diagram

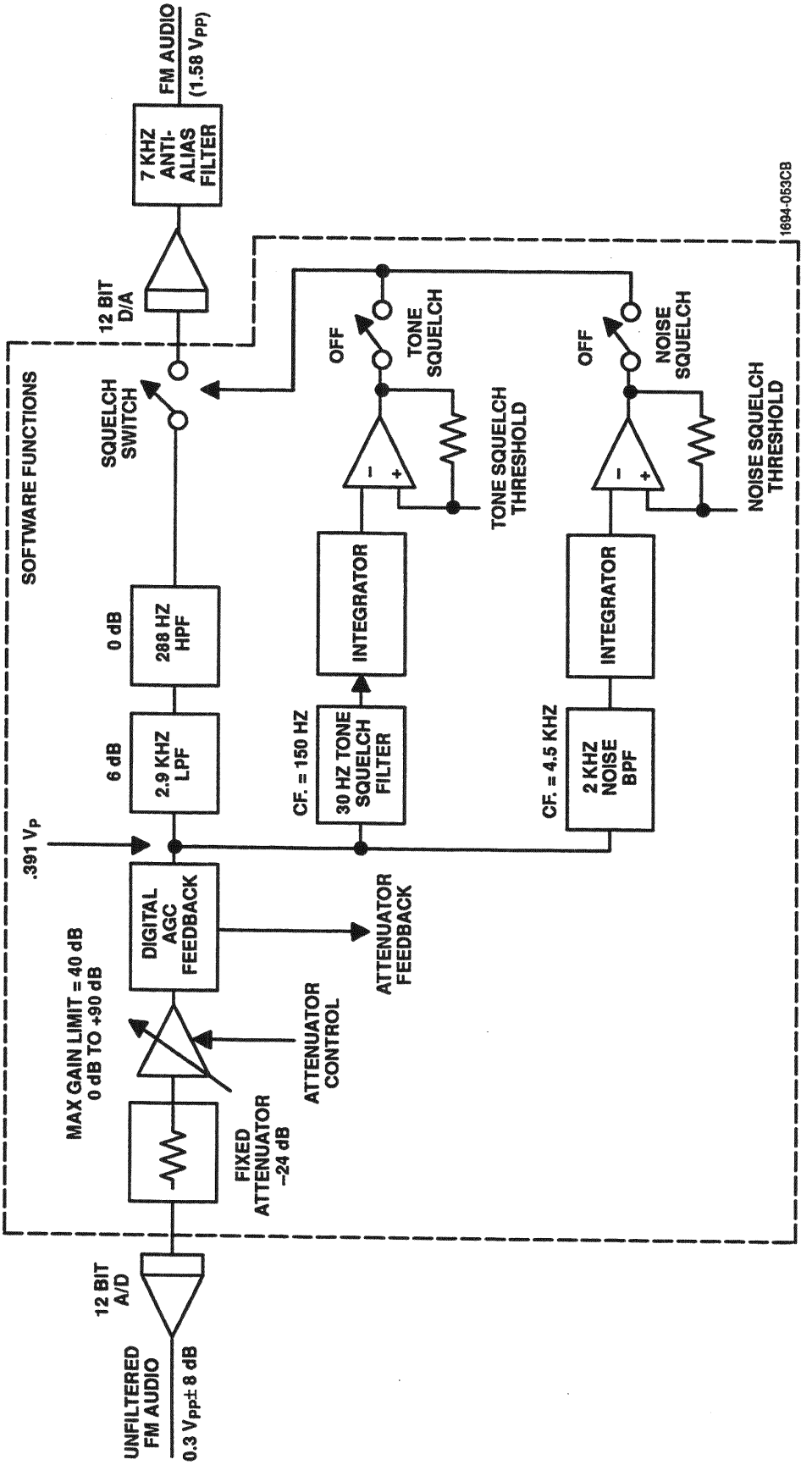


Figure 2. Digital IF – FM Receive Mode Block Diagram

3.1.2 Digital IF – Transmit Mode

The Digital IF transmit functions are very similar to the receive process. The assembly relies on A/D and D/A converters with the majority of processing done through software. The following paragraphs explain each transmit mode of operation.

3.1.2.1 Single Sideband and AME

Figure 3 is a block diagram of the transmit path for USB, LSB, and AME modes. Audio from the front panel comes into the A4 Assembly at P3-44, The audio is switched through U43 to a low pass, anti-alias filter U41. Filtered audio then passes through the A/D converter, goes through a high pass digital filter, and is level-controlled to a constant level. It is then either passed directly to a low pass filter, or is sent through a 2:1 compressor before going to the low pass filter. The compressor can be selected only from a remote control terminal.

The low pass filter output is modulated up to 6 kHz by a digitally-synthesized local oscillator. The output of the mixer is bandpass filtered to strip off the desired sideband. In AME, the carrier is reinjected at this point. In single-sideband mode, the carrier suppression is set to zero. The output is multiplied by a number set by the peak power control (PPC). This normally has no effect on the output and only comes into effect if the output of the transmitter exceeds rated power by 1 dB. The output goes to a D/A converter which produces a 6-kHz single-sideband signal. The processed digital IF is placed on the data bus to D/A converter U42. From U42, the now analog IF is buffered (U45A), switched by U43 and U50, and sent to the A5 Receiver/Exciter Assembly via P3-9.

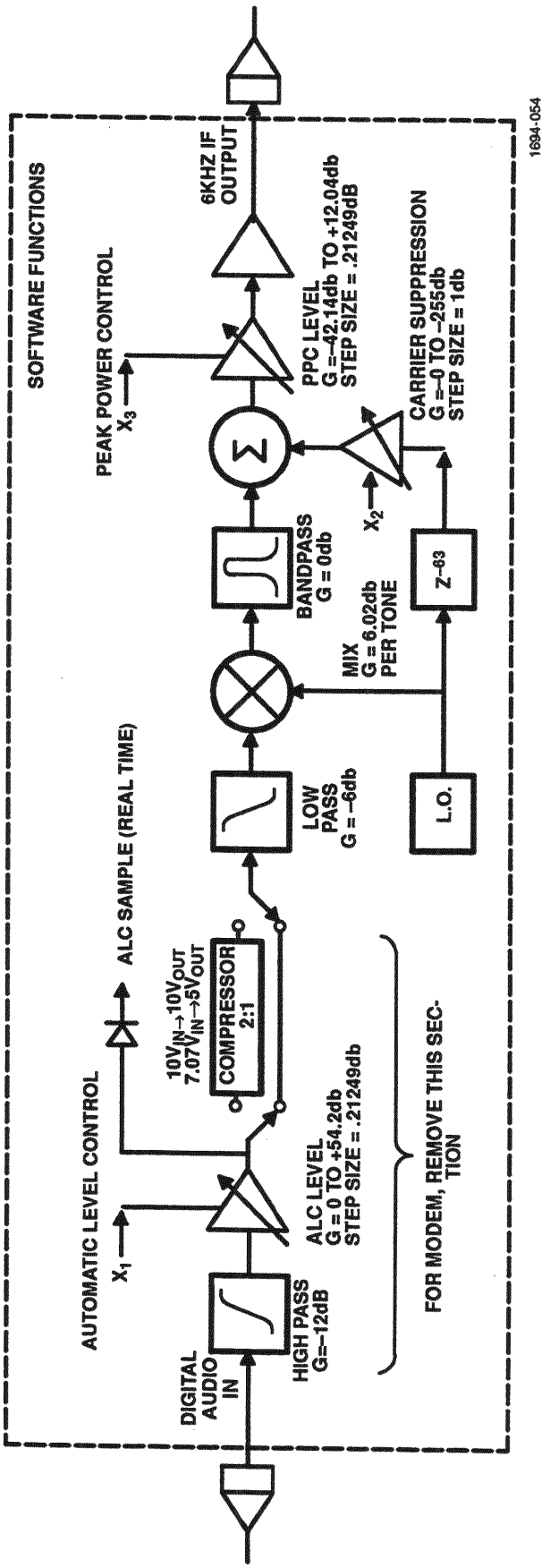


Figure 3. Digital IF – USB, LSB, and AME Transmit Mode Block Diagram

3.1.2.2 CW

Figure 4 is a functional block diagram showing operation of digital IF in CW transmit mode. This uses a 6-kHz look-up table to digitally synthesize a sinewave. CW keying closes a switch at the input of a bandpass filter. The bandpass filter provides CW shaping to reduce spectral splatter. The output of the filter is fed to a multiplier which provides peak-power control. PPC reduces output whenever the output of the transmitter exceeds rated power by 1 dB.

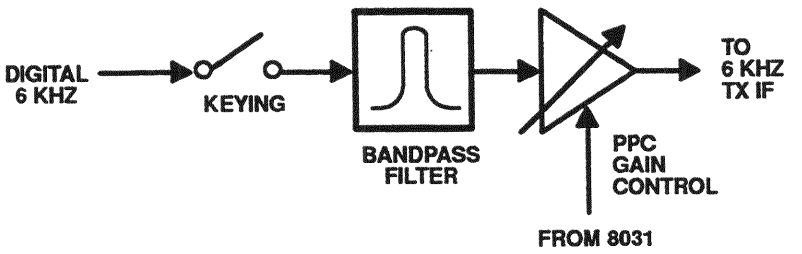


Figure 4. CW Transmit Mode Block Diagram

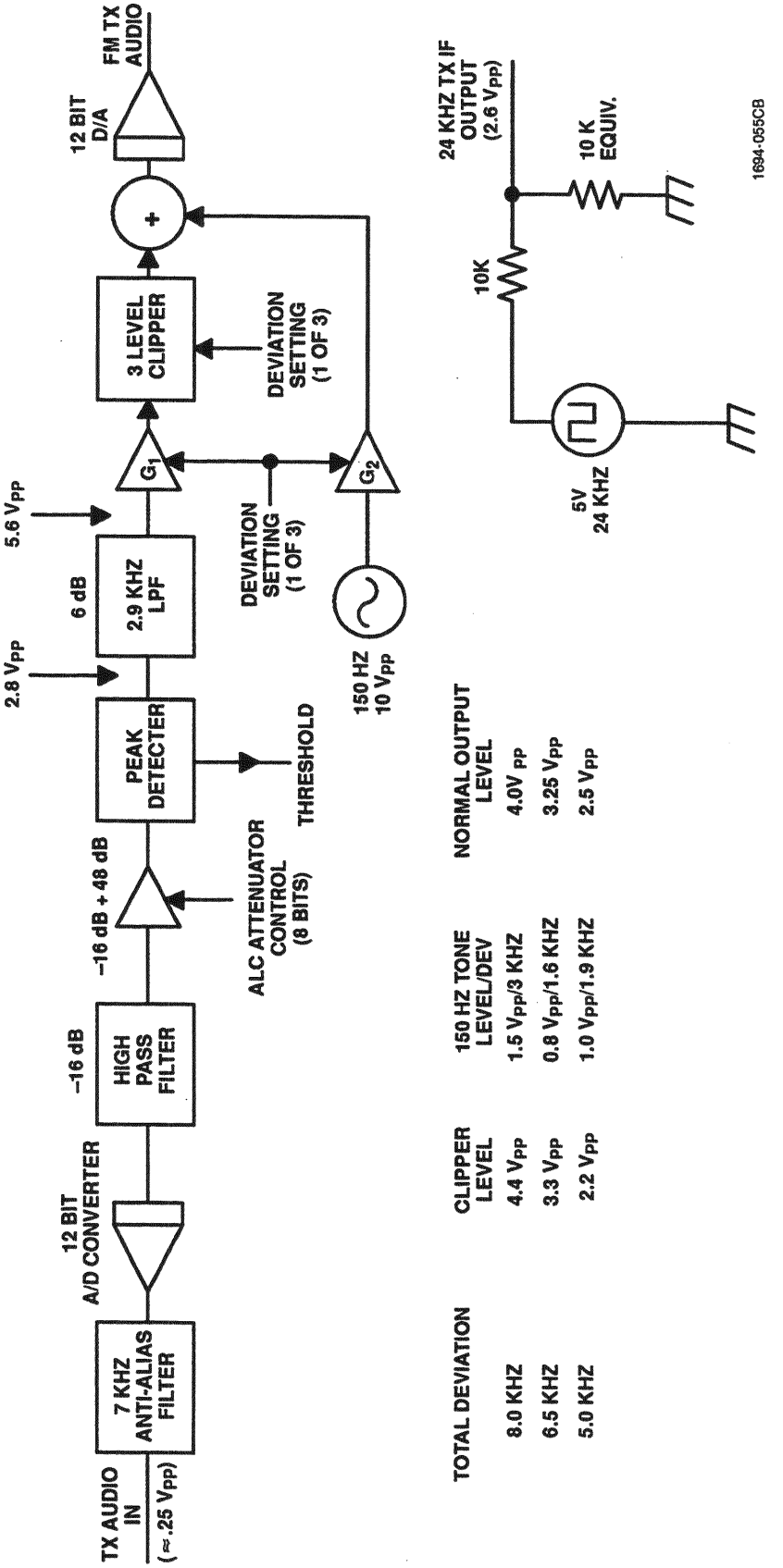
3.1.2.3 FM

Figure 5 is a block diagram of the transmit path of the Digital IF in FM mode. Audio is again brought into the module through the A/D converter U46 and digitally highpass filtered. The signal is limited to a constant level by the Automatic Level Control (ALC) circuit and lowpass filtered to 2.9 kHz. A variable gain amplifier is employed at this point to set signal level corresponding to any of three selected FM deviation levels. A variable clipper follows the amplifier, with clipping level also determined by the FM deviation level. Finally, a 150 Hz tone is added to the signal for use in receiver Tone Squelch. The level of this 150 Hz tone is also varied by the selectable FM deviation. The 12-bit D/A converter U42 produces the analog FM TX audio that is used to modulate the 71 MHz LO on the A6 assembly. The TX IF that is passed to the A5 exciter to form the signal carrier is a digitally generated 24 kHz square wave.

3.2 AGC Operation

Figure 6 is a functional block diagram of the automatic gain control. Receiver gain control is accomplished in two fashions. There is a digital gain control loop that simply attenuates the recovered audio signal internal to the digital IF processor. The AGC uses data gathered from the digital IF on signal level. The AGC processor determines the correct amount of attenuation (or gain) to be applied, and this value is given to the IF processor.

If the signal is very large at the receiver, the A/D converters may run out of range. In this case, the AGC processor uses readings from its own A/D converters to determine the appropriate amount of attenuation to cut in directly at the receiver. This attenuation control voltage may be observed on the second channel of the DAC (the first channel is an audio output).



TOTAL DEVIATION	CLIPPER LEVEL	150 HZ TONE LEVEL/DEV	NORMAL OUTPUT LEVEL
8.0 KHZ	4.4 V_{PP}	1.5 V_{PP}/3 KHZ	4.0V $_{PP}$
6.5 KHZ	3.3 V_{PP}	0.8 V_{PP}/1.6 KHZ	3.25 V_{PP}
5.0 KHZ	2.2 V_{PP}	1.0 V_{PP}/1.9 KHZ	2.5 V_{PP}

Figure 5. Digital IF – FM Transmit Mode Block Diagram

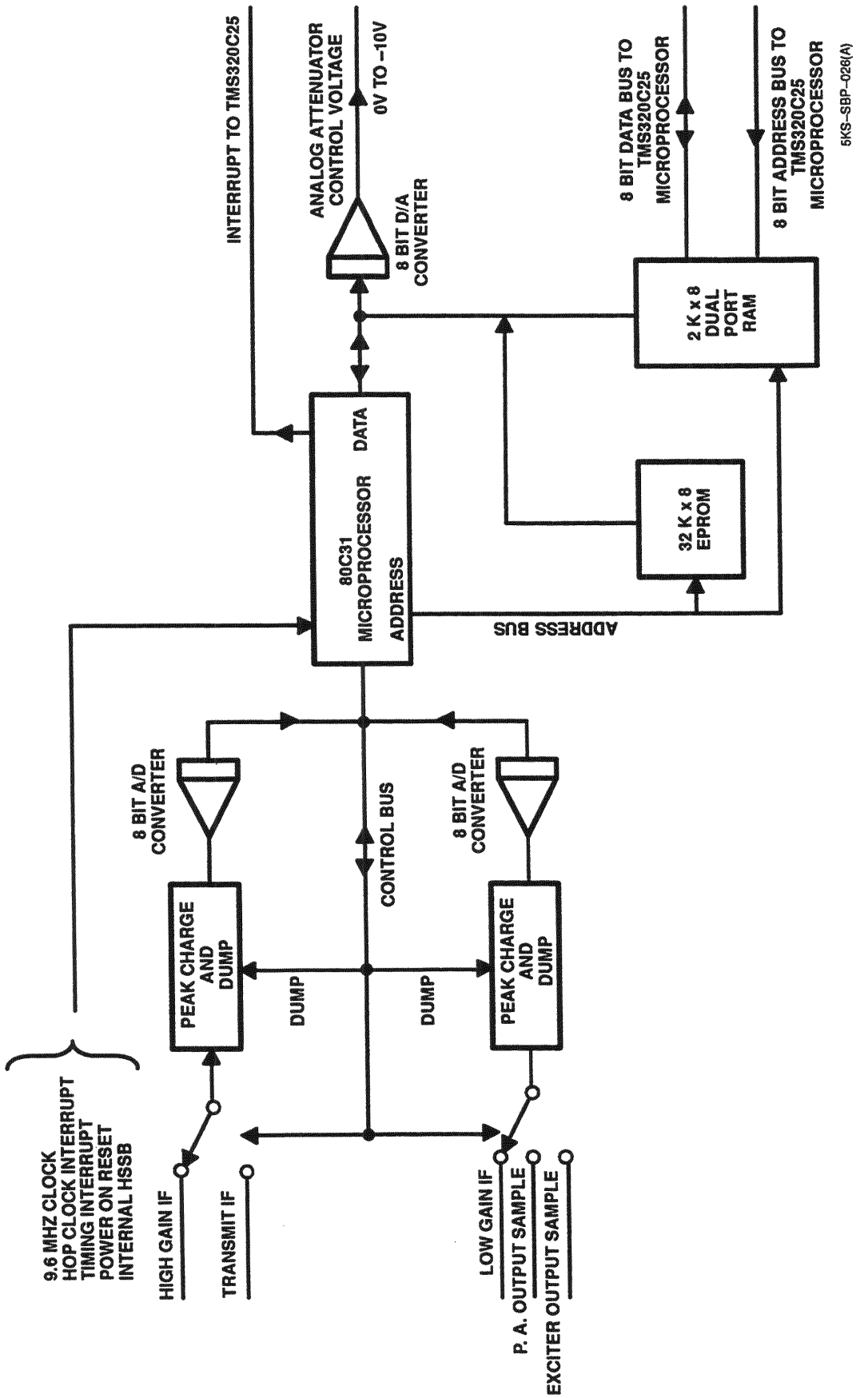


Figure 6. Gain Control Functional Block Diagram

3.3 TGC Operation

Transmit gain control (TGC) works in a similar way. There are actually three control loops that run in transmit. TGC is the main loop that controls transmitter power. This uses the analog attenuator control line to control exciter drive level. This is typically a slow responding loop, as to not modulate the signal.

Peak power control (PPC) is a very fast attacking digital loop that will attenuate the output of the IF processor if the RF power feedback line suddenly indicates an excess of power at the antenna. This loop typically takes control if an operator were transmitting and his antenna suddenly became disconnected.

Finally, the audio level control (ALC) loop normalizes the audio signal from the handset or other source. This gives the operator the maximum talk power for a wide range of voice volume levels. It is an all digital loop that has fast attack and slow decay times.

The TGC loop only operates if there is an IF signal present. Upon tuning to a new frequency, the TGC loop must acquire a power setting, and this should be done as quickly as possible. The AGC processor in this case is in "acquisition mode", where the TGC loop will very quickly try to acquire a gain setting. Once acquired, the processor shifts into "track" mode, where it very slowly responds to loop gain requirements. This slowness is necessary so the RF signal is not modulated with gain changes determined by the AGC processor.

3.4 Antenna Coupler/Power Amplifier Monitoring

During both transmit and receive, the IF processor occasionally samples the power amplifier and antenna coupler feedback lines. This data is given to the AGC processor, where it is stored until requested by the main control processor. VSWR is also calculated by the IF processor in transmit.

Sample rate is dependent on mode. CW mode does not require any audio sampling, therefore the power amplifier is sampled more often. The same is true of modem modes. Audio transmit modes are sampled less frequently, since an audio sample must be omitted to sample the power amplifier. Antenna tune mode is simply a CW mode that exclusively samples the coupler feedback lines.

3.5 Reference Temperature Monitoring

Also during transmit and receive, the temperature of the 9.6 MHz reference must also be measured by the IF processor. This measurement is necessary for the radio to maintain frequency accuracy. Occasionally, in the same manner that the PA is monitored, the temperature is monitored and the voltage read is given to the AGC processor, where it remains until the Main Controller requests it.

3.6 Support Sub Circuits

3.6.1 Sample Clock Synthesizer – U58, U59, U60, Associated resistors and capacitors

This circuit actually resides on the center board of the A4 three board set, although it is loaded by the AGC processor. This clock is phase locked to the 1.2 MHz clock generated by the reference board and drives the sampling of the audio signal and modem system timing. Most modes operate with a 24-kHz sample clock, but modem modes operate with a 28.8 sample clock. If there is no sample clock, the IF processing will not occur. If the sample clock has jitter, this will usually be seen as a high SNR in test.

3.6.2 Digital IF Interrupt Generator – U61

This chip generates a narrow pulse to the TMS320 that causes a "sample ready" interrupt. The TMS320 reads the A/D converters at this time.

3.6.3 Anti–Alias Filter – U41, Many Resistors and Capacitors

This circuit is an active lowpass filter that greatly attenuates signals above 7 kHz. This is necessary since signals with signals above 12-kHz "alias" (show up as) signals in the desired audio range. Our audio sample rate is 24 kHz, s/2 = 12 kHz. In receive this is used as a "reconstruction" (smoothing) filter.

3.6.4 Signal A/D Converters – U46, U47, U48, U49, and Associated Resistors and Capacitors

These A/D converters are used by the IF processor. The analog multiplexor (U49) is used to select the source sampled. The buffer amplifiers (U48B, U48C) provide additional drive to the A/D converters. U48A provides a 10-volt reference used by the D/A converter. It uses the stable 3-volt reference that is generated by the A/D converters. U48D is an output amplifier for receive audio.

3.6.5 AGC Peak Detect/Sample and Hold/Control Circuitry – U53, U54, U55, U56, U57, Q1, Q2, Resistors, Capacitors, and Diodes

These A/D converters are used for AGC and TGC sampling purposes. The peak detector is necessary because of the slow sample rate of the AGC processor. U55 are "active diodes" used to rectify and buffer the input signal. U54 is the input multiplexor for the peak detectors. U53 controls the peak detectors, A/D converters, mux, and keyline to the receiver/exciter module. Rectified audio/IF signals charge up C67 and C68. After the peak detectors are sampled by A/D converters U56 and U57, the capacitors' charges are dumped to ground by Q1 and Q2. After the detectors are dumped, the analog mux is turned on and the capacitors are allowed to charge once again. This occurs at a 1 kHz to 2 kHz rate.

3.6.6 Dual Port RAMs – U35, U80

These are used for communication between the IF processor and AGC processor (U35) and the IF processor and FFT processor (U80) RAM. The IF/AGC interrupts pass through the RAM (U35) while the IF/FFT processors use decoders (U67, U32) to interrupt each other. The 16-bit wide dual port RAMs have no internal interrupt generation mechanism.

3.6.7 Analog Switch Control – U44

This latch is used by the IF processor to direct the flow of audio on the analog portion of the board. Other lines on the latch are used to control multiplexors on the antenna coupler, and to gate the sample clock to the exciter (for FM mode).

4. TESTING AND ALIGNMENT

There are no testing or alignment procedures for this module.

5. BITE FAULTS AND TROUBLESHOOTING

Table 1 is a list of self-test fault codes for the Digital IF/AGC section of the A4 Signal Processor Assembly. The tests and faults are described in greater detail in the following subsections.

Table 1. Digital IF/AGC Fault Codes

Code	Fault
61	Communications fault
62	Internal RAM fault
63	ROM checksum fault
64	External RAM fault
67	Digital IF handshake fault (Dual Port RAM)
6B	Digital IF did not complete BITE
6C	Anti-alias filter fault
6D	28.8-kHz Sample clock fault
6E	24.0-kHz Sample clock fault
74	Frame clock not detected
75	Hop clock not detected
80	ROM checksum fault
81	Internal RAM fault
82	External RAM fault
83	Dual port RAM to AGC fault
84	Dual port RAM to FFT fault

5.1 Fault 61 – AGC Communication Fault

This indicates the Main Controller cannot communicate with the AGC processor over the internal high speed serial bus (HSSB). If this occurs, do the following:

a. Verify that the correct code version has been programmed in the flash ROM.

b. Verify that the AGC processor is running. Verify that +5 V, clock, and a valid reset pulse has been given to the processor.

c. Verify continuity of the HSSB.

5.2 Fault 62 – AGC Processor Internal RAM

This is a non-destructive test of the on-chip RAM of the microcontroller. If this test fails, the processor must be replaced.

5.3 Fault 63 – AGC Checksum Fault

This test performs an additive checksum test on all bytes in the program storage ROM. If any locations are bad or incorrectly programmed, this fault will occur. If this test fails, but the processor is running, the IC may simply have to be erased and reprogrammed. If this does not fix the problem, the ROM will have to be changed.

5.4 Fault 64 – AGC External RAM Fault

This is a nondestructive test that tests all of the external RAM on the microcontroller's bus. If this fault code occurs, it is likely that the external RAM device being tested is bad. A faulty address or data line to the part may also be the problem. Perform the following:

a. Check all data and address lines to the RAM for continuity. A simple probe of each line to check for activity may be sufficient, with a continuity check for a suspect bad line.

b. Check the "glue" logic to be sure that the RAM is being enabled.

c. The RAM may be faulty.

5.5 Fault 67 – Digital IF Handshake Fault (Dual Port RAM)

This tests the interrupt generation of the AGC and IF processors. If this test fails, the IF processor is probably not running. Check to see that the IF processor reported with a "TEST 3" command. If this test fails, do the following:

a. Verify that the TMS320 processor is receiving a valid clock signal, +5 volts, and a valid reset pulse was given to the processor.

b. Verify that the interrupt lines from the dual port RAM (U35) are high and generate narrow low pulses during the test. A digital storage scope will be required to see the narrow pulse. If the line(s) are low, the processor is not able to respond to the interrupt request. Be sure the interrupt request to the processor is high, pulsing low.

c. A faulty sample clock or interrupt generation circuit may also cause this problem. If an external interrupt line is held low, the processor will report its firmware revisions, then enter an interrupt service routine without ever exiting.

5.6 Fault 6B – Digital IF did not complete BITE

The digital IF is a much faster processor than the 80C51FA, and should have completed its test well before the AGC processor. If this fault code is encountered, do the following:

a. Verify the code in the TMS320 ROM. The processor may be getting lost in the test and not reporting.

b. Check for a strong clock and valid reset pulse. If everything seems okay, the processor may be faulty.

5.7 Fault 6C – Anti-alias Filter Test

This test checks the response of the active low pass filter. The IF processor generates a series of tones starting at 100 Hz and finishing at 16 kHz. The A/D converters perform a peak detect on the signal at the output of the filter, and this is compared to a table of acceptable limits. During a self test, this sweep generator can be heard in the handset. Failures in this test are most likely incorrect passive elements in the active filter circuit. Perform the following to troubleshoot the circuit:

a. Observe the output at the DAC (pin 1 of U45). Shortly after initiating self test, a series of tones from 100 Hz to 16 kHz of the same amplitude should be observed. This signal can be traced through the board, where the high frequencies should show attenuation after the anti-alias filter. By tracing this signal the faulty segment of the board may be identified.

5.8 Fault 6D – 28.8-kHz Sample Clock Fault and Fault 6E – 24.0-kHz Sample Clock Fault

During this test, the IF processor simply measures the duty cycle and period of the sample clock using the 36-MHz processor clock as a reference. This is a crude test, but it functions as desired. It will not, however, detect a noisy sample clock that is the correct frequency. Both 24-kHz and 28.8-kHz clocks are checked.

a. Check for a 24-kHz sample clock with the modem off and 28.8-kHz sample clock with the modem on. Observe that this signal is present at the 80C186 and the TMS320s.

b. If this is not present, observe a 1.2-MHz reference frequency at the input of the phase locked loop IC (U59 pin 1).

c. If the 1.2-MHz clock is present, observe that the serial data, clock, and strobe lines are free to toggle. Turning the modem on and off will generate activity on these three lines. PLL_DATA and PLL_CLOCK should have many transitions, while PLL_STB will only have two pulses per load.

5.9 Fault 74 – Frame Clock Not Detected

The Main Controller generates a frame clock pulse, and the AGC processor reports if the clock pulse was detected or not.

a. Verify the frame clock has continuity between the main control 80C51FA and the AGC 80C51FA.

b. Verify the frame clock line is not in a "stuck" condition (shorted to +5v or GND).

5.10 Fault 75 – Hop Clock Not Detected

This test is identical to the frame clock test, but a different hardware line is tested. Troubleshooting is identical to frame clock troubleshooting.

5.11 Fault 80 – Digital IF ROM Checksum Fault

This test is identical to the one the 80C51FA performs. The same solution applies.

5.12 Fault 81 – Digital IF Internal RAM Fault

This test is identical to the one the 80C51FA performs. The same solution applies.

5.13 Fault 82 – Digital IF External RAM Fault

This test is identical to the one the 80C51FA performs, but it is performed on the digital IF's dedicated external RAM. The same solution applies.

5.14 Fault 83 – Dual Port RAM to AGC Fault

These tests are the same tests that are performed on external RAMs. Dual port RAMs are also external and are accessed in the same manner. Faults here may occur because the part is bad or a faulty address or data line to the part may exist. Also any glue logic that is used to address or enable the part may by at fault. Check the same things as above.

5.15 Fault 84 – Dual Port RAM to FFT Fault

This test is identical to the dual port RAM to AGC processor test, but it is performed on the 16-bit wide part that interfaces the IF processor to the FFT processor. The same solution applies.

MODEM

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A4 SIGNAL PROCESSOR ASSEMBLY MODEM SUBSECTION

1. GENERAL DESCRIPTION

The internal High-Speed Data Modem included with the AN/PRC-138 is designed to overcome the problems that limit the rates at which data may be passed over a HF radio link. HF radio data links have been typically confined to low data rates and are subject to high error rates. The internal modem overcomes the problems presented by fading, multipath propagation, and interference on HF channels. The internal modem allows asynchronous or synchronous data to be passed at up to 2400 bps using 39-tone modulation, and up to 300 bps using FSK modulation.

2. INTERFACE CONNECTIONS

See the A4 Signal Processor Assembly section for interface connections.

3. TECHNICAL DESCRIPTION

The internal modem has two primary modes of operation: 39 tone and FSK. (The hopping mode with 16 tones will not be discussed here.) The 39-tone mode uses time-differential QPSK modulation of 39 tones for a resultant 3466-bps channel rate. The FSK mode is compatible with binary FSK modulators/demodulators. Mark and space frequencies over a 350-Hz to 3250-Hz range (at 5-Hz resolution) are selectable by the user. The FSK mode supports 75, 150, and 300 bps data rates.

Figure 1 is a simplified block diagram of the internal modem.

3.1 39-Tone Mode

Figure 2 illustrates the 39-tone mode modulation and demodulation functions. Modulation begins with the reception of a serial data stream from the data terminal equipment (DTE). The DTE can be a teletypewriter, voice digitizer, facsimile unit, or any other device compatible with an EIA RS-232 or MIL-STD-188-141A interface format.

Forward error correction (FEC) codes are calculated and added to the incoming data stream. The data and FEC bits are organized in a matrix. The matrix configuration allows adjacent groups of data bits to be redistributed in time to reduce burst errors. This process is called interleaving and is described in paragraph 3.1.5.

Modulation is performed by high-speed microprocessors. The digital signal processing produces a string of 12-bit words that are converted to an audio signal. The audio signal is then transmitted to the receive site and demodulated.

Demodulation recovers the transmitted data from the received audio signal. Demodulation is a digital process. The received audio signal is sampled at a rate of 7200 samples per second to generate a string of 12-bit words that digitally represent the audio signal. The digital signal processing includes frequency correction calculations and the actual demodulation. A major portion of the demodulation is a lengthy, continuous calculation called a Fast-Fourier Transform. This calculation recovers phase-shift information that yields the received data. The interleaving matrix created during the modulation process is reconstructed to put the data bits in their original order. The FEC code is evaluated and data errors are corrected before the data is sent to the receiving DTE in a serial stream.

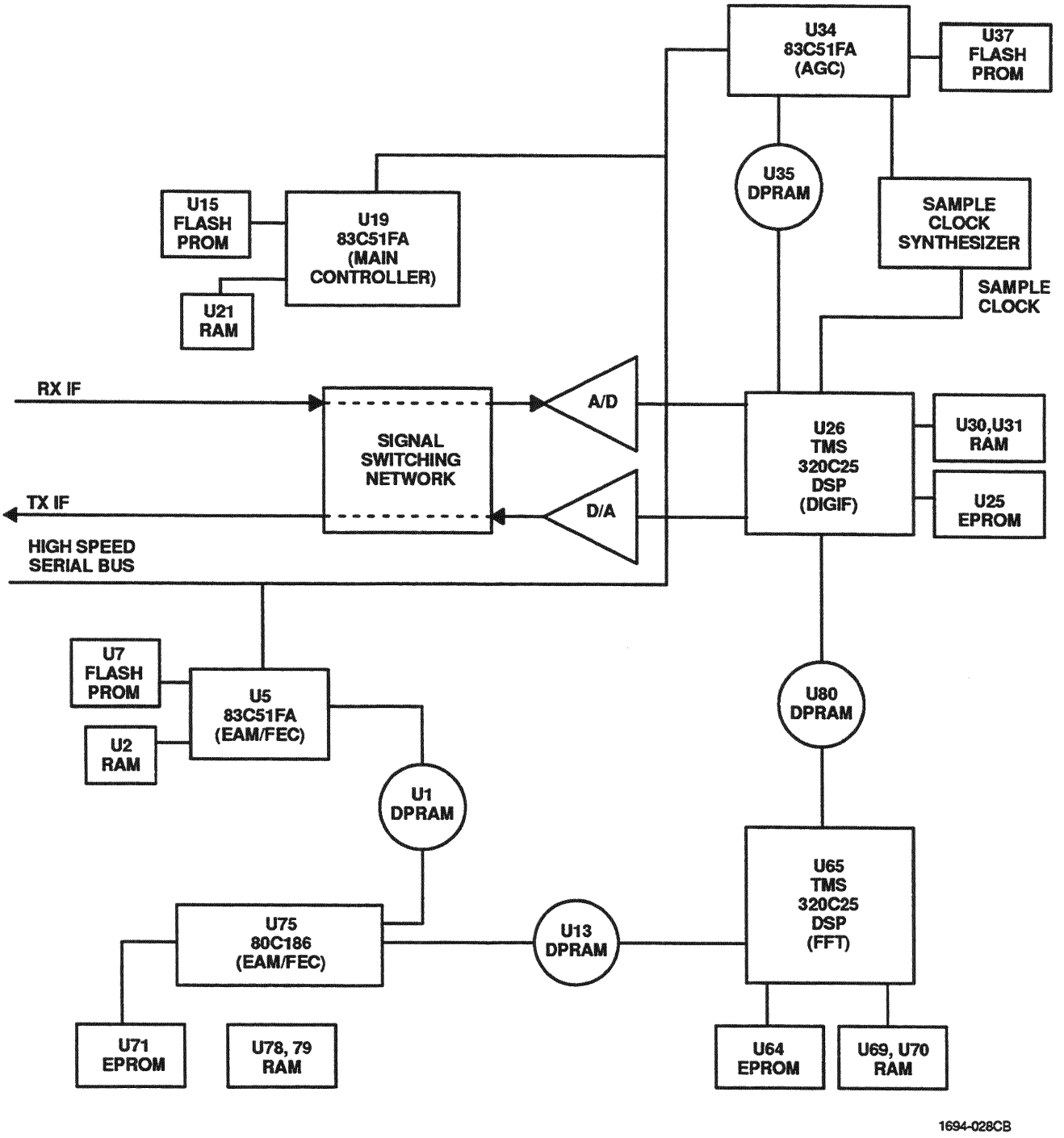


Figure 1. Signal Processor Module Block Diagram

3.1.1 39-Tone Modulation

The modulation method used in 39-tone mode is a form of phase shift keying (PSK). PSK shifts a sinusoidal wave in time to represent a binary data bit. The shift is measured in degrees. The internal 39-tone modem uses a type of PSK called time differential quaternary phase shift keying (TDQPSK). With this form of PSK, an individual wave can be shifted by 45, 135, 225, or 315 degrees. With four possibilities, each phase shift can be used to represent one of the four unique two-bit combinations shown in table 1.

A phase shift must be measured against some reference. In the modem, the phases of individual tones are changed at regular intervals. The time segments between phase changes are called frames. The phase shift of a signal in a frame is measured against the position of the signal in the previous frame. The fundamentals of TDQPSK are shown in figure 3.

The modulated tones in the 39-tone mode are in the audible range. The modem generates, modulates, and broadcasts 39 data tones simultaneously, along with an unmodulated doppler tone. The 39 tones are whole-integer harmonics of the 56.25-Hz fundamental. This separates the tones adequately to minimize interference while limiting the total bandwidth to 3 kHz.

TDQPSK allows each tone to carry two data bits per frame. A total of 78 data bits can be included in each frame. Notice that neighboring phases have few dissimilar bits (Hamming distance) so that minor signal impairments will produce the least bits in error. With a frame length of 22.5 milliseconds, the modem achieves an over-the-air baud rate of 3466 bits per seconds. FEC reduces the effective data rate to 2400 bits per second.

Table 1. TDQPSK Phase Shift Data

Phase Shift	Data
45	10
135	00
225	01
315	11

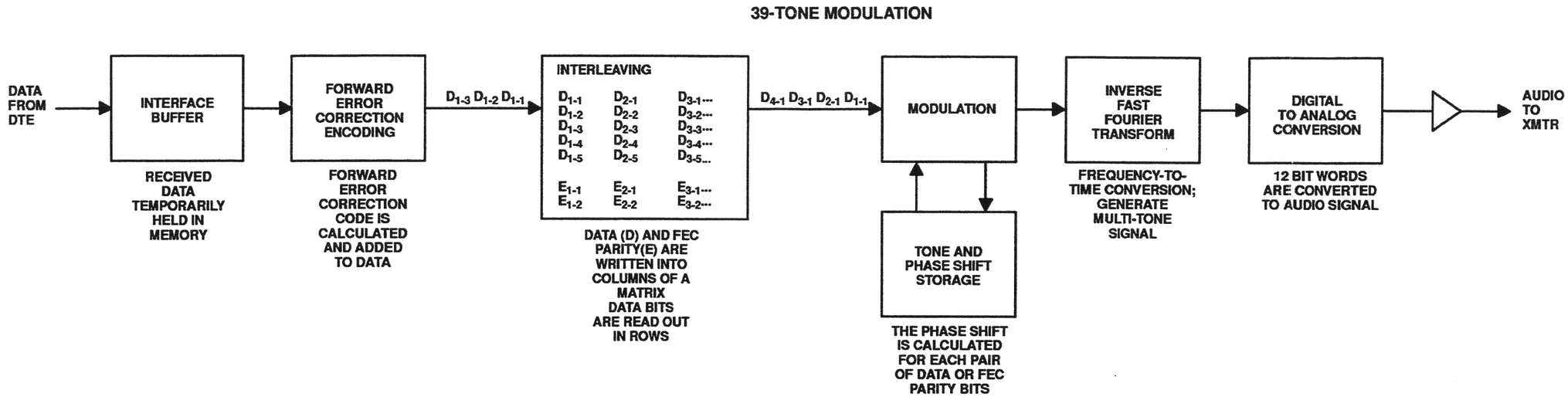
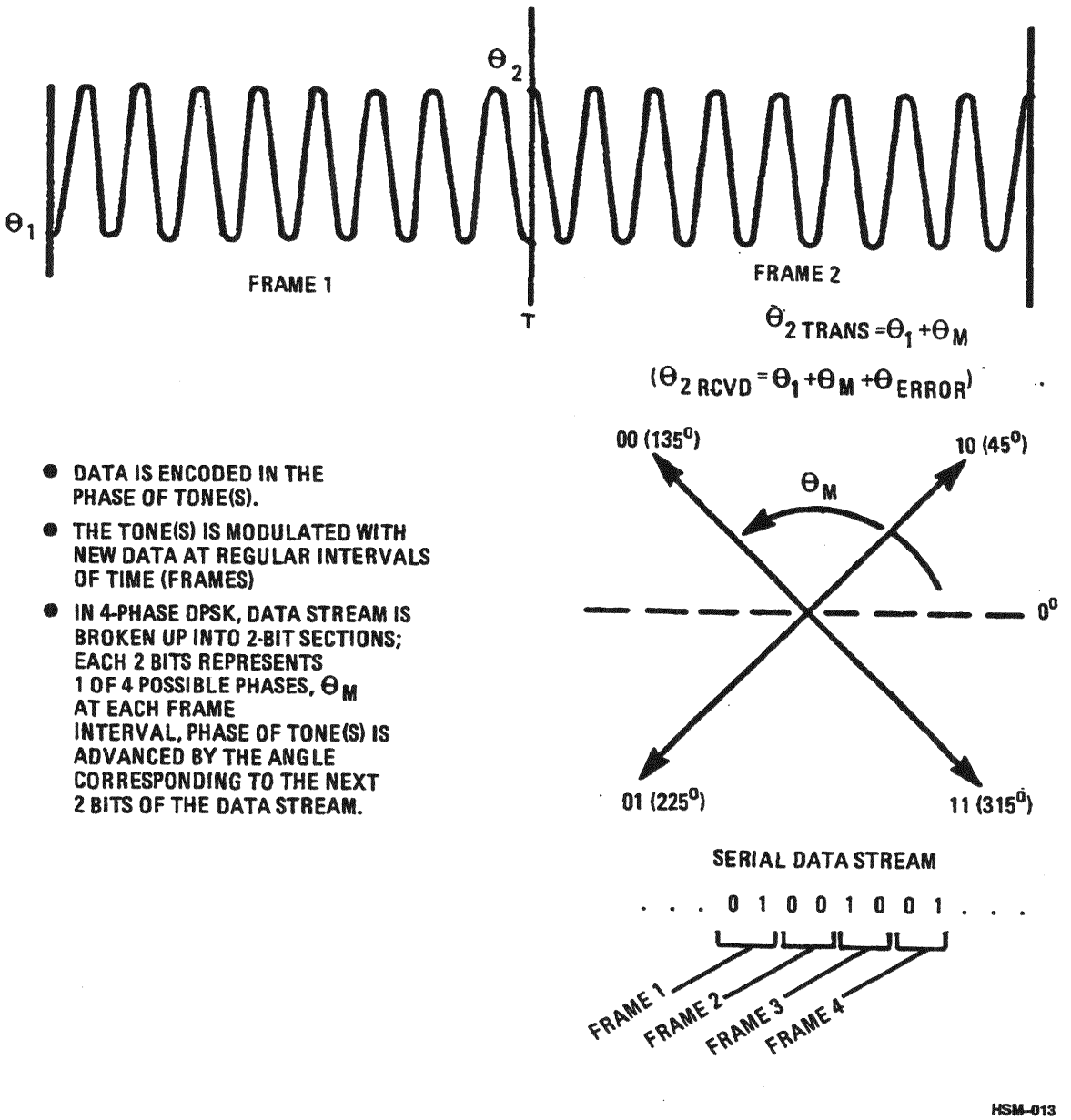


Figure 2. 39-Tone Modulation and Demodulation



- DATA IS ENCODED IN THE PHASE OF TONE(S).
- THE TONE(S) IS MODULATED WITH NEW DATA AT REGULAR INTERVALS OF TIME (FRAMES)
- IN 4-PHASE DPSK, DATA STREAM IS BROKEN UP INTO 2-BIT SECTIONS; EACH 2 BITS REPRESENTS 1 OF 4 POSSIBLE PHASES, Θ_M AT EACH FRAME INTERVAL, PHASE OF TONE(S) IS ADVANCED BY THE ANGLE CORRESPONDING TO THE NEXT 2 BITS OF THE DATA STREAM.

Figure 3. TDQPSK Fundamentals

3.1.2 Demodulation

Demodulation is the process of recovering data from the received audio signal. This is done digitally in the internal 39-tone modem The demodulation is preceded by a frequency-correction routine to eliminate any errors introduced during transmission. An algorithm based on the Fast-Fourier Transform is used to separate the 39 tones and determine their phase shifts.

The Fast-Fourier Transform is a mathematical tool used in digital signal processing to convert a variable of time into a variable of the frequency spectrum. The relative phase of each tone is expressed as the position of a vector on a coordinate system where the axes are I (in-phase) and Q (quadrature). The modulation process uses four phase shifts, each separated by 90 degrees. The demodulation process needs only to determine the quadrant of the phase-shift vector to retrieve the data (see figure 4). Confidence values are computed for each bit and are a function of amplitude and angle. For fixed amplitude, the I data bit confidence value reaches its maximum for vector positions of 90 degrees and 270 degrees (see figure 3). The Q data bit reaches its minimum values at these angles. At 0 degrees and 180 degrees, the Q data bit reaches its maximum value and the I data bit reaches its minimum value.

The received data is de-interleaved to reposition the bits in their original order, and is run through an FEC decoding routine before being sent to the receiving DTE.

3.1.3 Frequency and Frame Synchronization

A two-part preamble is used to synchronize the sending and receiving units at the beginning of each transmission. The first part of the preamble is used by the receiving unit to correct for frequency errors. Frequency errors can be introduced by vehicle motion, shift of the ionosphere, or by the radio equipment. Because the modulated tones are only 56.25 Hz apart, small frequency shifts can cause data errors. Part two of the preamble establishes frame synchronization.

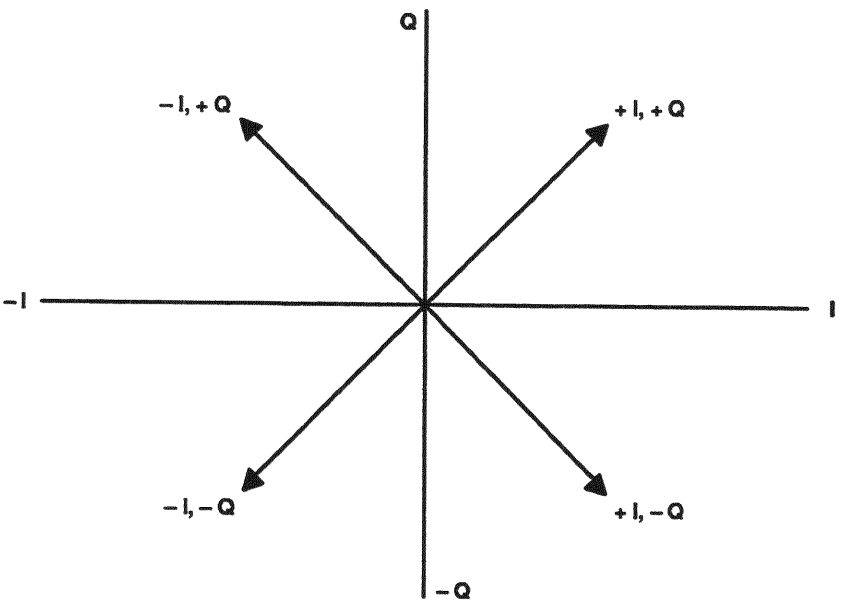
Part one of the preamble has four unmodulated tones at 787.5, 1462.5, 2137.5, and 2812.5 Hz. This part of the preamble lasts for the equivalent of 14 frames or 315 milliseconds. Upon recognizing this pattern, the receiving unit initiates an algorithm that can correct for frequency errors of up to 75 Hz. The same process is performed continuously during data transmission using the 393.75-Hz doppler tracking tone as a reference. The modem can correct for shifts of up to 3 Hz per second.

The second part of the preamble establishes the frame boundaries. Part two of the preamble has three bi-phase modulated tones at 1125.0, 1800.0, and 2475.0 Hz. The phase of each tone alternates between two angles. The receiving unit looks for this phase shift and uses it to locate the frame boundary.

The signal at the frame boundaries is unstable because of multipath distortion. The receiving modem splits the received signal into periods based on the frame boundaries. A guard time of 4.7 milliseconds separates the integration time periods of two adjacent frames, as shown in figure 5. Frequency and phase shift calculations are performed on the signal received during the integration time. In summary:

TX frame = 22.50 ms
RX integration = 17.77 ms
Guard time = 4.73 ms.

The preamble is followed by a single frame containing all 39 tones. This frame is used by the receiving modem to establish an initial phase reference for each tone and has initial phases chosen simply to create a nicely shaped envelope with no peaks.



I	Q	ANGLE	DATA
+	+	45°	1 0
–	+	135°	0 0
–	–	225°	0 1
+	–	315°	1 1

HSM–014–mp

Figure 4. Vector Representation of Phase Shift

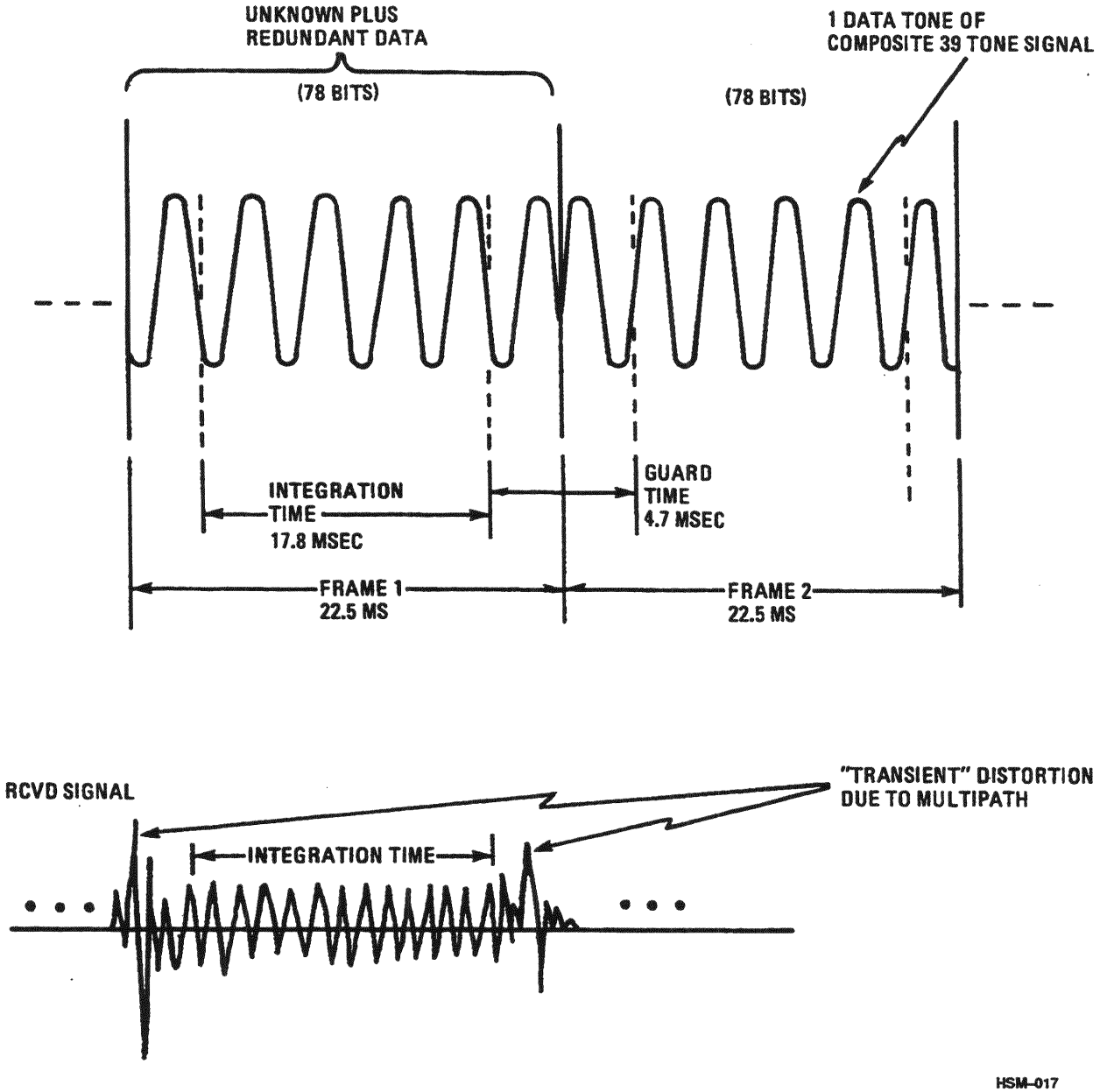


Figure 5. Frame Boundaries

3.1.4 Forward Error Correction (FEC) Code

FEC involves encoding data at the sending station so that the receiving station can correct errors introduced during transmission. The FEC code is derived from, and so reflects, the bit pattern of the data stream. Once computed, this code is inserted into the data by the sending unit. The receiving unit computes code bits for the received data and compares them to those computed by the sending unit. Differences in the codes calculated at the sending and receiving ends of the link are used to locate and correct data errors.

The internal 39-tone modem employs a Reed-Solomon code. To implement this, the data stream is divided into four-bit segments called symbols. At the 2400-bit-per-second rate, the Reed-Solomon (14, 10, 2) code is used. This means that at this data rate, the data is organized into code words 14 symbols long. Each code word has ten data symbols and four code symbols. Two symbol errors in each word can be corrected.

At data rates of 1200-bits-per-second and below, the Reed-Solomon (7, 3, 2) code is used. In this version, the code words are seven symbols long, with three data symbols and four code symbols. Two symbol errors in each word can be corrected.

The Reed-Solomon code is a systematic block code, meaning that the data bits and check bits are not interspersed. The code words are always the same length and the code symbols follow the data symbols in each word. The code is non-binary with symbols of fixed length to help guard against burst errors. A synchronizing sequence is inserted into the data stream so the receiving unit can detect word boundaries.

3.1.5 Interleaving

Between the encoding and the modulation operations, the binary signals undergo an interleaving process in which adjacent symbols are intermixed and distributed in time in a systematic way. This produces no net change in the transmission rate, although it may introduce a substantial delay, depending on the interleaving factor. Interleaving enhances the ability of the decoder to correct errors arising from localized channel disturbances, such as short fades or lightning activity. Between the demodulation and decoder, a deinterleaving process restores the received data signal to its original order, thereby breaking up error clusters and distributing the damaged symbols over several code words. The power of the decoding process is then sufficient to correct many of the errors because the number of errors in each code word is small.

3.1.6 Diversity

Diversity in the modem refers to sending and receiving data by more than one path. Inband diversity is used in the internal 39-tone modem. Inband diversity is the process of modulating more than one tone with the same data.

For Inband diversity, each bit of data is modulated onto two of 16 different tones, depending upon the baud rate. The diversity factors are listed in table 2. Two forms of Inband diversity are available: frequency, and time/frequency diversity. In frequency diversity, the tones which carry the same data are all transmitted within the same symbol interval. In time/frequency diversity, the redundant tones are transmitted over successive symbol intervals. This achieves a time spread for added protection during fades. For most types of HF channel conditions, time/frequency diversity yields improved performance over frequency diversity, although some additional delay is introduced as shown in table 2.

Table 2. Diversity Factors

Baud Rate	Diversity Factor	Additional Delay in Time/Frequency Mode
2400	1	0
1200	1	0
600	2	180 msec
300	4	293 msec
150	8	338 msec
75	16	360 msec

3.1.7 Signal Clipping Average

The baseband output of the internal 39-tone modem is clipped internally to improve system performance by limiting the peak-to-average ratio of the signal. The output signal is made up of 39 tones with equal amplitudes. The signal resembles band-limited white noise. Periodic high peaks of this signal can be clipped without affecting the performance of the modem. The amount of clipping is predetermined, not user-selectable.

Limiting the peak-to-average ratio of the baseband signal allows the power output of the RT-1694 Transmitter to be increased. The added RF signal strength improves system performance.

3.2 Binary FSK Theory of Operation

In FSK mode, the internal modem can interoperate with existing binary modulators/demodulators. Mark and space frequencies over a 350-Hz to 3250-Hz range (at 5-Hz resolution) are selectable by the user.

3.2.1 FSK Modulation

As shown in figure 6, external data enters the modem through the A1A1 Interface Assembly. The interface UART then strips the start and stop bits from the incoming data and sends data-only packets through the EAM/Modem processor. For an asynchronous signal, the start, stop, and optional parity bits are inserted on the EAM/Modem processor software USART for transmission. In synchronous mode, the EAM/Modem processor takes data from the FEC processor and, based on its transmit clock, feeds the data into the FFT processor.

In FSK mode, the FFT processor sends mark or space tones based on data from the EAM/Modem processor. A transmit clock is generated by counting samples at the 14.4-kHz FSK sampling rate. This clock is used to drive the software USART on the EAM/Modem processor.

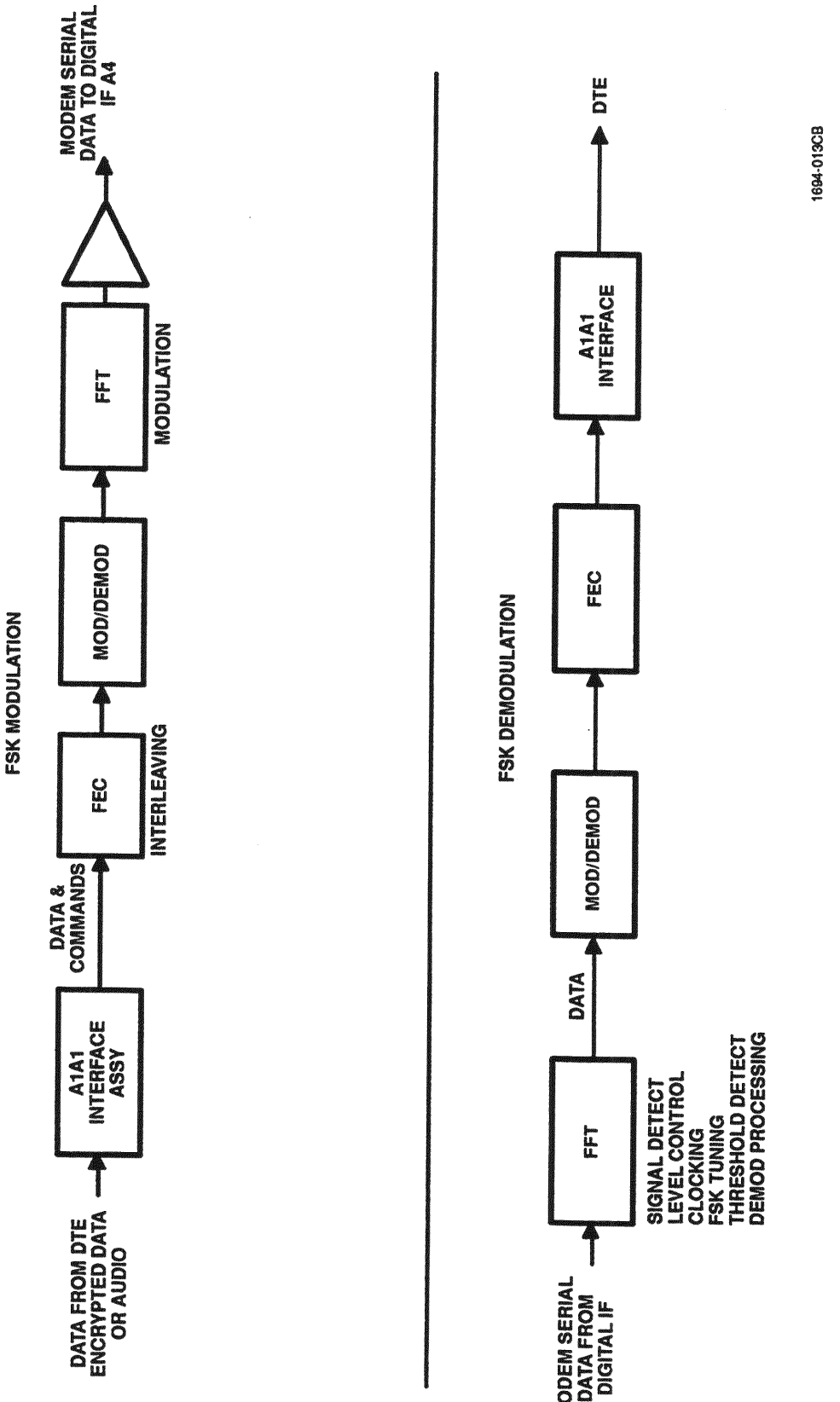


Figure 6. FSK Modulation and Demodulation

3.2.2 FSK Demodulation

Receive data is reconstructed in the FFT processor 320C25 by the processing shown in figure 6. The method of waveform depends upon the data port, sync or async. In asynchronous mode, a free-running oscillator follows the incoming signal. At the point of data transition, 1-to-0 or 0-to-1, samples are taken at exactly one-half of the baud period or at the center of integration where the data stability is the greatest. This sampling technique continually resynchs upon each transition to provide sampling at the peak stability point on the waveform.

To ensure that an FSK synchronous signal is sampled properly, a more complex sample locater is used. In the sync mode, another free-running oscillator compares its counter with the transition of the signal. It corrects itself by adding one to the counter value if the receive clock is behind the signal, and subtracts one from the counter value if the clock is ahead of the signal. This approach reduces clock drift that could cause operating problems when providing a clock to a synchronous data device.

3.3 39-Tone Mode Versus FSK Mode

FSK mode performs well at high signal-to-noise ratios and low baud rates. The FSK signal characteristics are such that signals outside the mark and space frequencies are not considered and, therefore, do not interfere. FSK mode is offered to make the AN/PRC-138 compatible with devices which are only capable of FSK TX/RX.

The 39-tone mode is preferred for sending HF signals at higher bit rates or in more severe HF channel conditions. Since the 39-tone waveform is QPSK processed, each bit of information is at a different phase angle.

4. TESTING AND ALIGNMENT

This module requires no testing or alignment procedures.

5. BITE FAULTS AND TROUBLESHOOTING

The self-test fault codes for the Modem Module are shown in table 3. The tests and faults are described in greater detail in the following subsections. The test equipment required for troubleshooting includes:

- Digital multimeter
- Oscilloscope (Tektronix 465m or equivalent)

Table 3. Modem Module Fault Codes

Code	Fault
01	Communications fault
14	Hop clock error
15	Frame clock error
1F	FEC ROM checksum fault
20	FEC external RAM fault
21	FEC dual-port RAM fault
22	MDM not running
23	FFT handshake fault
24	FFT to MDM dual-port RAM fault
25	MDM to FFT dual port RAM fault
26	MDM to FEC dual port ram fault
27	MDM ROM checksum fault
28	MDM RAM fault
29	Sample clock error
2A	FFT ROM checksum fault
2B	FFT internal RAM fault
2C	FFT external RAM fault
2D	FFT to DIF dual port RAM fault
2E	Hop clock error
2F	FFT self test (not complete)
30	FFT self test (not complete)
31	Reserved
32	Time sample transfer fault
33	MDM self test (not complete)
34	FEC self test (not complete)

NOTE: FEC refers to Forward Error Correction Processor A04 U5 (83C51FB) MDM refers to Modulate/Demodulate Processor A04 U75 (80C186) FFT refers to Fast Fourier Transform Processor A04 U65(TMS320C25) DIF refers to the Digital Intermediate Frequency Processor A04 U26 (TMS320C25).

5.1 Fault 01 – Communications Fault

This fault occurs when the FEC processor does not respond to the Main Controller via the internal high-speed serial bus (HSSB). Do the following:

a. Verify +5 V on U5-44, U6-20, U7-32, U2-28, U8-16 and U11-14.

b. Verify 9.6 MHz on U5-21.

c. Verify at power-up a high (+5 V) then a low (GND) on U5-10.

d. Verify U5-11,13 (Internal Serial Bus) toggling from power-up.

e. Verify U5-32 (PSEN) and U5-33 (ALE) toggling from power-up.

5.2 Fault 14 – Hop Clock Error

The Main Controller is unable to detect a hop clock signal sourced from U75 (the 80C186). Check the following nodes and signals.

NOTE

It is possible that the LPC Module (A3) or the Motherboard could be holding the Hop Clock Signal. If the following trouble shooting does not identify the source of the fault on the Signal Processor, refer to the LPC Module's trouble shooting section.

a. During BITE check U19-14 for activity. If there is none, put radio in 39-tone mode and check for logic level activity on this pin. If there is none, it is possible that the MDM 80C186 (U75) or the FEC 83C51FB (U5) are not running correctly.

b. If U75 and U5 appear to be operating correctly, check to see if the Motherboard or the LPC Module are holding the /HOPCLKL line.

5.3 Fault 15 – Frame Clock Fault

This fault occurs when the Main Controller micro (U19) is unable to detect a pulse on FRAM_CKL line, generated by the FEC micro (U5). Do the following:

NOTE

It is possible that the Interface Module (A1A1) or the LPC module (A3) is holding this line, thereby causing this fault.

a. Verify activity on U19-17 during BITE. If there is no activity on this pin, put the radio in 39-tone mode and check for activity on this line. If there is none, it is possible that the FEC micro (U5) or the MDM micro (U75) are not running correctly.

b. If U5 and U75 appear to be running correctly, verify that the LPC module or the Interface module are not holding FRAM_CKL line.

5.4 Fault 1F – FEC ROM Checksum Fault

This fault indicates that the FEC micro U5 has detected a checksum error in its FLASH PROM U15. Do the following:

a. Verify logic level activity on U15–22, 24 (ALE , PSEN).

b. Verify activity on all address and data lines on during test.

c. Check for short or open circuits on all address and data lines on U15.

5.5 Fault 20 – FEC External RAM Fault

The FEC micro cannot write to and read back from all locations in its external RAM U2. Do the following:

a. Verify logic level activity on all address and data lines on U2 during BITE test.

b. Check for short or open circuits on all address and data lines on U2.

c. Check for activity on U2-20, 22, 27.

d. Replace U2.

5.6 Fault 21 – FEC Dual-Port RAM Fault

The 83C51FA microprocessor U5 cannot read to and read back from all locations of MDM/FEC Dual Port RAM U1. Do the following:

a. Check for logic level activity on U1-46, 50, 51 during BITE.

b. Check for logic level activity on all address and data lines on the FEC side of U1 during BITE.

c. Replace U1.

5.7 Fault 22 – 80C186 (U75) MDM Not Running

The MDM 80C186 microprocessor (U75) is unable to respond to commands from the 83C51FA microprocessor through the MDM/FEC Dual Port RAM U1. Do the following:

a. Verify +5 V on U75-9, 43, U71-44, U78-32, U79-32, U72-20, U77-20, U76-20.

b. Verify 36.16 MHz activity (including logic levels) on U75-59.

c. Verify that U75-24 goes low then high at least once from power-up, and then remains high.

d. From power-up if U75-42 drops and then never goes high, then U75 is not responding to interrupts correctly. If U75-42 never drops, verify inverter U74 is working correctly. If it is, then replace U1.

e. Verify that U72, U76, U77 (HC573s) are latching addresses correctly. If one or more are not, replace.

f. Verify logic level activity on all data and address lines on U71.

g. Replace U71.

h. If test still fails, replace U75.

5.8 Fault 23 – FFT Handshake Fault

This fault indicates that the MDM 80C186 (U75) cannot communicate with the FFT TMS320C25 (U65) via MDM/FFT Dual Port Ram U13. Do the following:

a. Verify +5 V on U13-17, 68; U65-23, 35, 61, 62; and U64-4

b. Verify 36.16 MHz on U65-52.

c. Verify that U65-65 goes low then remains high at least once during BITE.

d. Verify logic level activity on all data and address lines on U64, and then U13. Verify that U63 is operating correctly and providing low going pulses to U64-22.

e. If test is still failing, replace U64.

f. If test is still failing, replace U13.

g. If test is still failing, replace U65.

5.9 Fault 24 – FFT to MDM Dual-Port RAM Fault

This fault indicates that the FFT micro (U65) cannot write to and read back from dual port ram U13. Do the following:

a. Verify +5 V on U13-17, 68; U65-23, 35, 61, 62, and U64-4.

b. Verify logic level activity on all data and address lines on U13.

c. Replace U13.

5.10 Fault 25 – MDM to FFT Dual-Port RAM Fault

This fault indicates that the MDM micro (U75) cannot write to and read back from MDM/FFT Dual Port RAM U13. Do the following:

a. Verify +5 V on U13-17, 68,;U65-23, 35, 61, 62, and U64-4

b. Verify logic level activity on all data and address lines on U13.

c. Replace U13.

5.11 Fault 26 – MDM to FEC Dual Port RAM Fault

This fault indicates that the MDM micro (U75) cannot write to and read from its side of MDM/FEC Dual Port Ram (U). Do the following:

a. Check for logic level activity on U1-1, 2, 6 during BITE.

b. Check for logic level activity on all address and data lines on the MDM side of U1 during BITE.

c. Replace U1.

5.12 Fault 27 – MDM ROM Checksum Fault

This fault indicates that the MDM 80C816 (U75) has detected checksum fault in its UV eprom U71. Do the following:

a. Verify +5 V on U71-44, U72-20, U77-20, U76-20.

b. Verify logic level activity on all address and data lines on U71 during BITE.

c. Verify that there are no short or open circuits on all data and address lines on U71.

d. Verify logic level activity on pins U71-3, 22.

e. Reprogram U71.

5.13 Fault 28 – MDM RAM Fault

This fault indicates that the MDM 80C186 processor U75 cannot read and write to every location in its RAMs U78 and U79. Do the following:

a. Verify +5 V on U78-32, U79-32.

b. Verify logic level activity on all data and address lines on U78, U79 during BITE.

c. Verify logic level activity on U78-22, 24, 29, 30.

d. Verify that there are no short or open circuits on all data and address lines on U78 and U79.

e. Verify that U72, U76, U77 are working correctly.

f. Replace U78, U79.

5.14 Fault 29 – Sample Clock Fault

This fault indicates that the MDM 80C186 (U75) detected an incorrect sample clock rate at U75-20, 21. Do the following:

a. Verify logic levels toggling at 28.8 kHz or 24 kHz on pins U75-20, 21.

b. If there is no (or incorrect) signal, verify 2.4 or 2.8 MHz at U58-4,. If this signal is correct, replace U6

c. If signal at U58-4 is incorrect, verify 1.2 MHz at logic levels on U59-1.

d. If 1.2 MHz is correct on U59-1, verify that R71, R120, R121, C79, C150 are the correct values.

e. Verify that U59-5 is at +5 V with short-duration pulses to ground. If this is not seen, replace U59.

f. If the signal at U59-5 is as described above, then replace U58.

5.15 Fault 2A – FFT ROM Checksum Test

This failure indicates that the FFT TMS320C25 micro (U65) has detected a checksum error in its UV EPROM U64. Do the following:

a. Verify +5 V on U64–44.

b. Verify logic level activity on all address and data lines of U64 during BITE.

c. Verify that there are no short or open circuits on any of the address or data lines of U64.

d. Reprogram U64.

e. If the test still fails, replace U64.

5.16 Fault 2B – FFT Internal RAM Fault

This test indicates that the FFT TMS320C25 microprocessor (U65) is unable to read and write to all its internal RAM locations. Do the following:

a. Replace U65

5.17 Fault 2C – FFT External RAM Fault

This fault indicates that the FFT TMS320C25 is unable to write and read to every location in its external RAM space. Do the following:

a. Verify +5 V on U69-28 and U70-28.

b. Verify logic level activity on all data and address lines on U69, U70 during BITE.

c. Verify logic level activity on U69-20, 22, 27; U70-20, 22, 27.

d. Verify that there are no short or open circuits on all data and address lines on U69 and U70.

e. Replace U69. If fault still occurs, replace U70.

5.18 Fault 2D – FFT to DIF Dual Port RAM Fault

This fault indicates that the FFT micro (U65) cannot write to and read from its side of FFT/DIF Dual Port Ram (U80). Do the following:

a. Verify +5 V on U80-17, 68.

b. Verify logic level activity on all data and address lines on FFT side of U80 during BITE.

c. Verify logic level activity on U80–36, 37, 38, 51.

d. Verify that there are no short or open circuits on all data and address lines on U80.

5.19 Fault 2E – Hop Clock Error

See fault 14.

5.20 Fault 2F – FFT Self Test (Not Complete)

This fault indicates that the FFT micro (U65) did not reply after it was commanded to test its side of the FFT/MDM Dual Port RAM.

Follow troubleshooting recommendations for faults 22, 24, 2A, 2C.

5.21 Fault 30 – FFT Self Test (Not Complete)

This fault indicates that the FFT microprocessor (U65) did not reply after it was commanded to test its internal and external RAMs and its ROM.

Follow troubleshooting recommendations for faults 22, 24, 2A, 2C.

5.22 Fault 32 – Digital IF Time Sample Transfer Test

This test transfers known data to the DIF processor via the FFT processor and the MDM/FFT and FFT/DIF Dual Port Rams. Do the following:

a. Follow troubleshooting procedures for faults 24 and 25.

b. If test still fails, refer to the Digital IF fault code 84 troubleshooting section.

5.23 Fault 33 – MDM Self Test (Not Complete)

This fault indicates that the MDM 80C186 microprocessor (U75) did not return from performing its self test after being commanded to perform its test by the FEC processor.

Follow the same troubleshooting techniques for faults 27 and 28.

5.24 Fault 34 – FEC Self Test (Not Complete)

This fault indicates that the FEC 83C51FB microprocessor (U5) had not finished its self test when the Main Controller micro polled it for its test results.

Follow the same troubleshooting techniques as for faults 01, 1F, and 20.

FREQUENCY HOPPING

TABLE OF CONTENTS

LIST OF FIGURES

A4 SIGNAL PROCESSOR ASSEMBLY FREQUENCY HOPPING SUBSECTION

1. GENERAL DESCRIPTION

The AN/PRC-138 Harris proprietary frequency-hopping option is embedded in the A4 Signal Processor Assembly (10303-2500). The hopping mode of operation provides LPI/LPD (Low probability of intercept/Low probability of detection) communication of 75/150/300 baud modem data and 800 bit per second digitized LPC voice. In addition, the hopping mode is designed to provide reliable communication in a jamming/high interference environment. For additional security hopping modem data and digital voice data may be encrypted using the A1A2 Encryption Assembly option.

2. INTERFACE CONNECTIONS

See the A4 Signal Processor Assembly section for interface connections.

3. TECHNICAL DESCRIPTION

The hopping mode of operation is based on a 20 hop/sec, 16 parallel-tone modem waveform. Time differential quadrature phase shift keying (TDQPSK) is used to modulate each of the 16 tones for the transmission of data/digitized voice. In TDQPSK, each tone can carry two bits of information which are coded as one of four possible phase shifts in the tone at a frame boundary. In addition to the TDQPSK signalling used for most data transmission, there also exists "id frames" which are used for waveform synchronization. These frames use 3 of 16 FSK signalling where only 3 tones of the possible 16 possible tones are modulated. The three tones chosen are unique to the programmed network identification (NETID). Radio TX/RX frequencies are picked from a programmed set of frequencies (HOPSET) based on a pseudorandom number (PN) generator that is seeded by the NETID.

3.1 Hopset Types

Three different types of hopsets may be programmed into the RT-1694:

- Wideband (WB)
- Narrowband (NB)
- List (LI)

When using the antenna coupler, only narrowband hopsets are allowed. When the antenna coupler is bypassed for broadband antenna use, all three types of hopsets are available.

3.1.1 Wideband Hopsets

A wideband hopset is defined by a start frequency and a stop frequency. The hopset consists of all frequencies between the start and stop subject to the following constraints:

- Minimum Bandwidth 70 kHz
- Maximum Bandwidth 2 MHz
- Frequency Spacing 5 kHz

3.1.2 Narrowband Hopsets

A narrowband hopset is defined by a center frequency (Fc). The hopset consists of all frequencies within a defined bandwidth centered about Fc. The bandwidth available and the frequency spacing is dependent on the center frequency as follows:

- 2.0 MHz <= Fc < 3.5 MHz
  Frequency Spacing 2.5 kHz
  Hopset Bandwidth 17.5 kHz

- 3.5 MHz <= Fc < 5.0 MHz
  Frequency Spacing 2.5 kHz
  Hopset Bandwidth 50 kHz

- 5.0 MHz <= Fc < 15.0 MHz
  Frequency Spacing 2.5 kHz
  Hopset Bandwidth 100 kHz

- 15.0 MHz <= Fc
  Frequency Spacing 5 kHz
  Hopset Bandwidth 300 kHz

3.1.3 List Hopsets

A list hopset allows the user to program specific hopset frequencies. The following restrictions apply:

- Minimum Bandwidth 140 kHz
  Maximum Bandwidth 2.0 MHz
  Minimum Number of Frequencies 15
  Frequency Spacing 10.0 kHz

3.2 Exclusion Bands

Up to ten exclusion bands may be programmed. These bands, defined by a start frequency and a stop frequency, are excluded from any wideband hopset. For example, if a wideband hopset is programmed with a start frequency of 2.0 MHz and a stop frequency of 2.8 MHz, it would normally transmit on frequencies throughout this entire range; however, if an exclusion band is programmed for 2.4 to 2.5 MHz, the unit will not use any frequencies in the excluded band. Exclusion bands are used only for wideband nets, and have no effect on narrowband or list hopsets.

3.3 Initial Synchronization

For two or more AN/PRC-138s to communicate in hopping mode, a hopping net must first be established to synchronize the unit's PN generators and hop clocks. This processes is termed "initial synchronization." For units to achieve synchronization they must be programmed with identical NETIDs and HOPSETs. This programming provides each unit with a set of five distinct frequencies which are only used for the initial synchronization procedure. These five frequencies are referred to as the "initial sync frequencies". In addition, a known pattern of hopset frequencies which are used during for the "sync response" transmission is selected. This sequence of frequencies is called the "sync response dwell pattern". Prior to initial synchronization, a unit displays a "NO SYNC" status, and cannot communicate with any other units.

The protocol for initial synchronization is shown in figure 1.

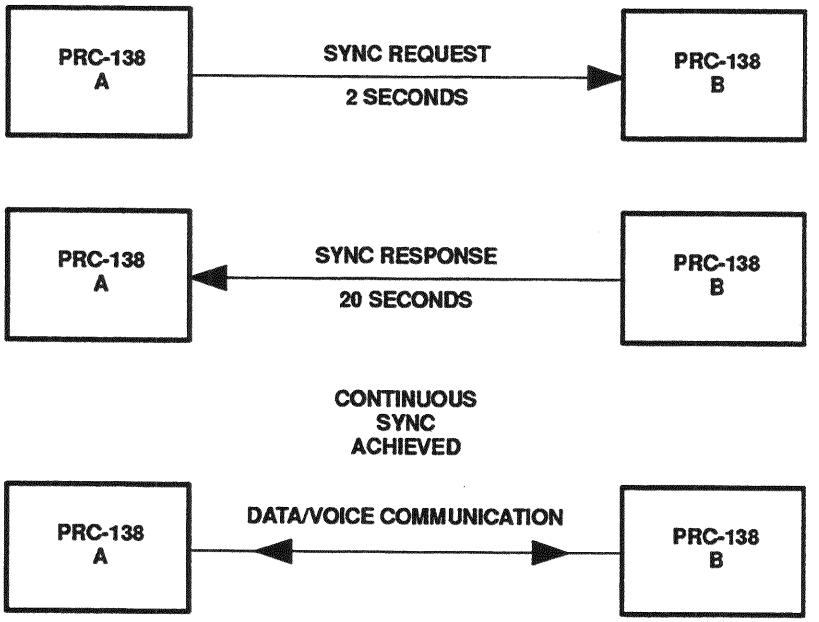


Figure 1. Initial Synchronization

3.3.1 Sync Request

Synchronization is initiated when one unit transmits a 2 second "SYNC REQUEST" burst to another unit. This burst conveys NETID information using Frequency Shift Keying (FSK) modulation. Based on the NETID, 3 of the 16 parallel modem tones are FSK modulated. This information is sent out 10 times on each of the five initial sync frequencies at a rate of 50 hops/sec (see figure 2). An unsynchronized receiving unit will scan it's initial sync frequencies to look for the SYNC REQUEST burst. When the receiver detects this burst, it notifies the operator. If the operator wishes to synchronize with the requesting radio, he/she replies with a SYNC RESPONSE transmission.

3.3.2 Sync Response

The SYNC RESPONSE transmission is 20 seconds long and is sent on the "sync response dwell pattern" frequencies at 20 hops/second. The waveform used for this transmission is the same as the one used for all data transmissions, and is shown in figure 3. The unit receiving the SYNC RESPONSE synchronizes its hop timing to follow the transmitter's hop pattern. During the SYNC RESPONSE transmission, 75 baud data is sent to the receiver. This data contains the transmitter's PN generator state, and it is sent out redundantly for robustness. If the receiver is successful in obtaining the transmitters PN data, then it will load it into it's own PN generator and update the generator appropriately. Both units are now hopping on the same random frequencies at the same time. The two units are now said to be in CONTINUOUS SYNC, and display a status of "IN SYNC".

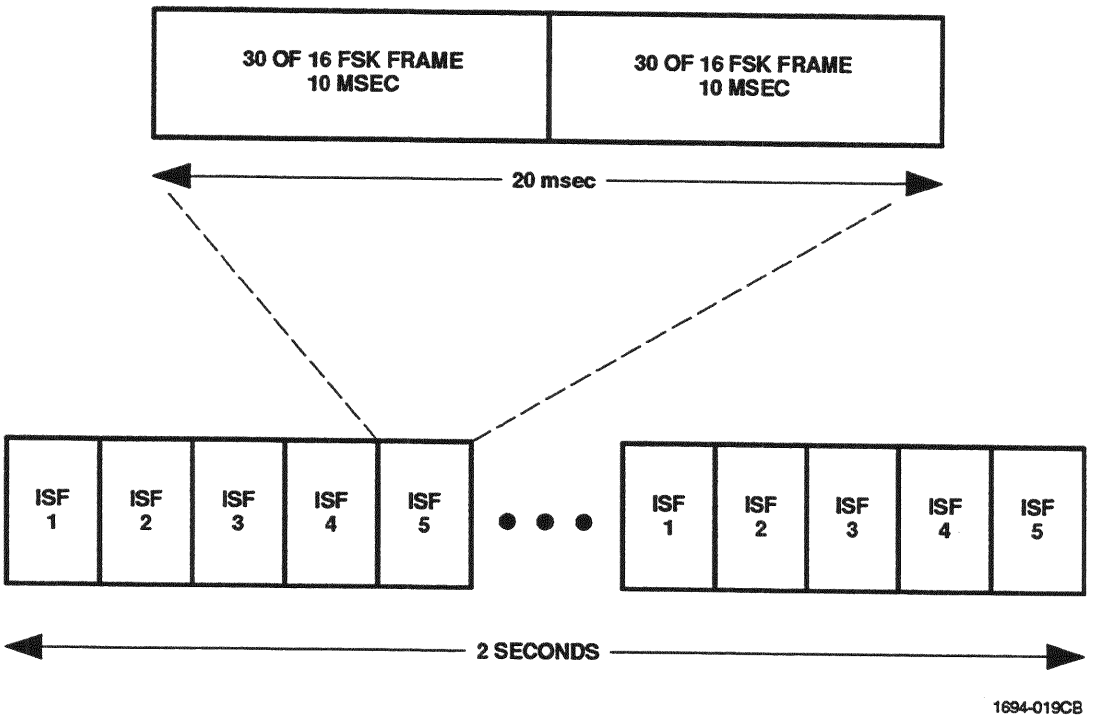


Figure 2. Sync Request Burst

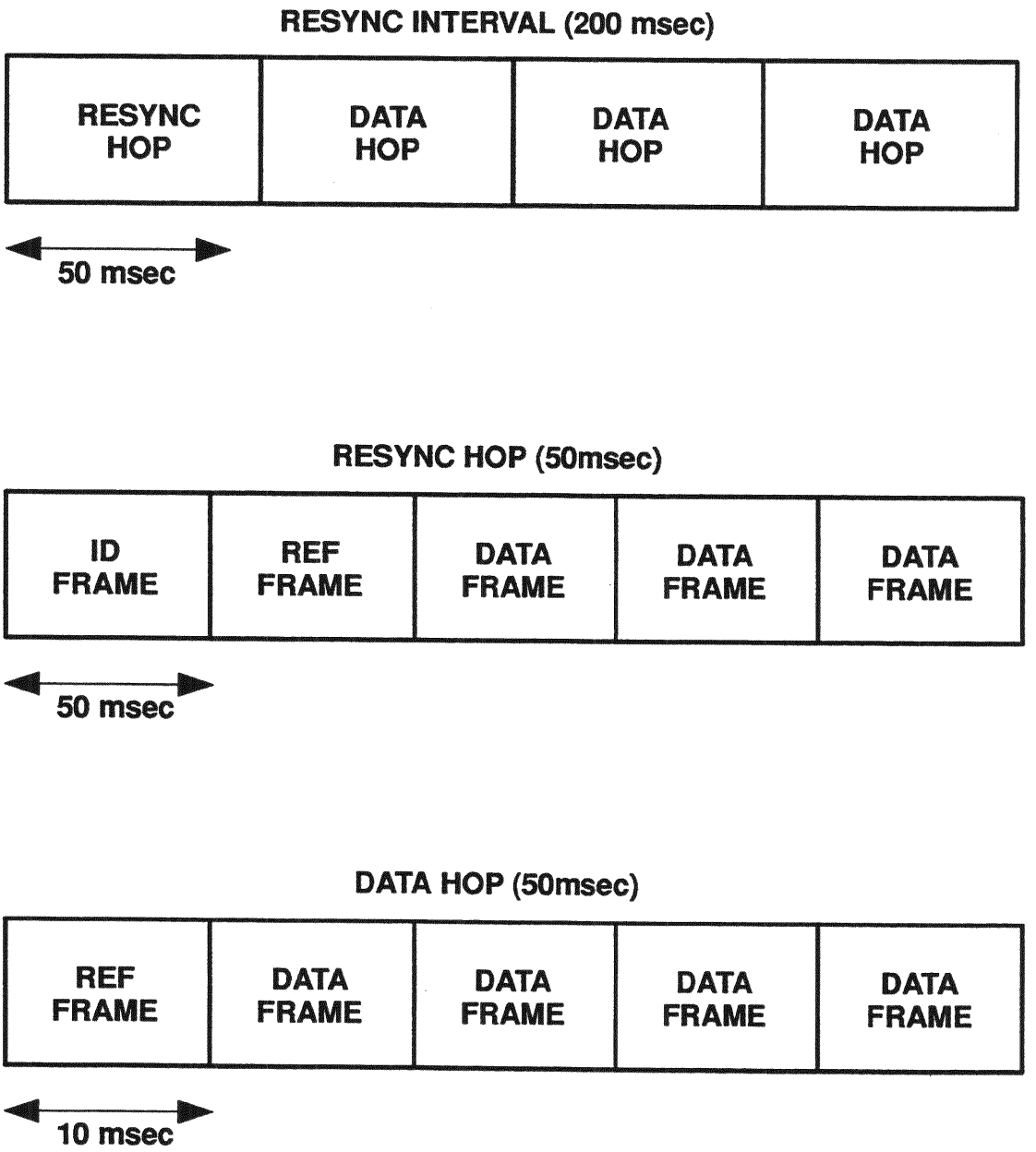


Figure 3. Data Transmission Waveform

3.4 Continuous Synchronization

When two or more units are in CONTINUOUS SYNC, they can communicate by sending 75/150/300 baud modem data, or LPC digital voice. Communication occurs on frequencies selected randomly from the hopset at a rate of 20 hops/second. The transmission waveform is shown in figure 3. CONTINUOUS SYNC lasts for a period of eight hours, at which time the unit drops back to the "NO SYNC" state and the Initial Synchronization procedure must be repeated before any further communication can take place.

3.5 Passive Initial Synchronization

A procedure called passive initial synchronization allows a unit to enter a hopping network without actively sending a SYNC REQUEST. This process occurs when the unsynchronized unit detects a SYNC REQUEST, but does not reply with a SYNC RESPONSE transmission. Instead the unit listens for a SYNC RESPONSE which may be transmitted by a third unit in the network. The procedure then follows a "normal" initial synchronization, and the unit enters the CONTINUOUS SYNC mode.

3.6 Late Net Entry

Once a hopping network is established between two or more units (by passive or active initial synchronization), another unit may enter this network at a later time. This is called a late net entry. Units which are in CONTINUOUS SYNC mode, but are not actively transmitting or receiving data, periodically scan the initial sync frequencies looking for SYNC REQUEST bursts. If a sync request burst is heard at this time, the unit may respond with a SYNC RESPONSE and the requesting unit will enter the network as in "normal" initial synchronization.

3.7 Modem Operation

The modem used in hopping is capable of sending data at rates of 75, 150, or 300 baud. There is auto-baud capability built in, that is, that the receiver automatically detects the baud rate being used by the transmitter and adjusts its baud rate to correspond. The modem is capable of synchronous or asynchronous data operation, and may be interfaced to many external data terminal devices (DTEs). Modem data may be sent in clear or encrypted mode.

3.8 LPC Voice Operation

In the hopping mode, no analog voice transmission is allowed. Whenever the handset is keyed, a digital voice transmission begins. The LPC voice algorithm used is a low baud rate (800 bps) adaptation of the LPC-10 standard (2400 bps). LPC voice data may be clear or encrypted.

4. TESTING AND ALIGNMENT

This module requires no testing and alignment procedures.

5. BITE FAULTS AND TROUBLESHOOTING

Their are no self-test fault codes for the frequency hopping option. Troubleshooting techniques are included in the following subsections.

5.1 General Hardware Check

Perform the following checks when troubleshooting the frequency-hopping option.

a. Check for Vcc, GND, clocks on all processors U19, U34, U26, U5, U75, U65.

b. Verify hop clock at pin 22 of EAM/MOD/DEMOD processor (U75). In hopping mode, this should be a 50 % duty cycle clock with a period of 50 msec. During a SYNC REQUEST TX, this period should change to 20 msec.

c. Verify frame clock at pin 2 of the EAM/FEC processor (U5) . You should see narrow pulses every 20 msec.

d. Verify 24-kHz sample clock at pin 68 of DIGIF processor (U26). A sample clock of 28.8 kHz is used for single-channel modem modes.

e. Verify radio power output in CW mode.

f. Verify modem/LPC operation in single channel mode.

5.2 Troubleshooting Operational Faults

The following are possible troubleshooting problems and solutions:

Problem: Two units will not achieve initial synchronization.

Solution(s):

a. Check that both units have same HOPSET.

b. Check that both units have same NETID.

c. If wideband operation, verify that exclusion bands are programmed the same, as they apply to the current hopset.

d. Verify transmission of SYNC REQUEST on scope.

e. Verify transmission of SYNC RESPONSE on scope.

Problem: Two units say they are "IN SYNC", but cannot pass modem/voice data.

Solution(s):

a. Verify that both units have encryption on, or both have it off.

b. Verify that units have same encryption key, if encryption is on.

c. Check to see if the two units hop clocks are in alignment during active TX/RX. The hop clocks can be found at pin 22 of U75 on each respective unit's 10303-2500 module. The rising edges of the two should be within 1–2 msec of each other.

Problem: Units seem to pass modem data, but it looks like "garbage" on DTE terminal.

Solution(s):

a. Verify that both modems are operating in the same DTE mode Sync/Async.

b. If in Async mode, verify that DTE baud, parity, and stop bit settings are the same.

AUTOMATIC LINK ESTABLISHMENT

TABLE OF CONTENTS

LIST OF FIGURES

A4 SIGNAL PROCESSOR ASSEMBLY
AUTOMATIC LINK ESTABLISHMENT SUBSECTION

1. GENERAL DESCRIPTION

The MIL-STD-188-141A compatible (also RF-7210 compatible) Automatic Link Establishment (ALE) option is embedded in the A4 Signal Processor Assembly (10303-2500). This option is included as part of the RF-5161 Performance Option. It is enabled in the RT-1694 through the presence of the LPC Assembly (10303-1540).

There are two distinct modes of ALE operation in the RT-1694:

- Remote Operation
- Standby Operation

The remote operation mode maintains the RT-1694 remote port as ALE control. During standby operation, the user controls the ALE functions through the front panel. Local standby mode is a feature of the manpack which allows the radio to reduce its power consumption significantly during receive scanning operation. This is accomplished by quickly powering up, performing a quick scan of the complete scan channel set, and (if no signal is present) powering down the radio for a predetermined amount of time before repeating the process.

2. INTERFACE CONNECTIONS

See the A4 Signal Processor Assembly section for interface connections.

3. TECHNICAL DESCRIPTION

When the radio is in ALE mode, all of the individual hardware and microprocessors in the A4 Signal Processor Assembly are configured to implement this function. The majority of the ALE functions are implemented on U75 (an 80C186 microcontroller known as the EAM/Modem), U65 (a TMS320C25 microprocessor known as the FFT), and U5 (known as the EAM/FEC processor). The EAM portion is responsible for implementing the bulk of the MIL-STD-188-141A protocol. The EAM/FEC Processor, an 80C31 microcontroller, is responsible for interfacing the EAM portion of the Signal Processor Assembly to the rest of the radio. The U26 TMS320C25 DIGIF processor and its supporting circuitry serve as the IF signal conversion interface to the EAM section of the module.

The EAM/FEC processor U5 controls the audio conversion circuitry through commands sent via the High Speed Serial Bus (HSSB) to the Main Controller U19. The Main Controller in turn, configures the rest of the radio including the signal switching circuitry and the DIGIF processor through commands sent to the AGC processor (U34) via the HSSB. During modulation, the transmit data is formatted by the 16-bit embedded controller U75 and the IF signalling is accomplished by the digital signal processors (DSP) U65, U26, and the digital to analog conversion chip U42. During demodulation, the data is processed by analog to digital converter, the two digital signal processors, and the 80C186 microcontroller. The received information is then sent to the 8-bit EAM/FEC processor to be routed to the rest of the radio.

3.1 EAM/FEC Processor (U5)

The EAM/FEC Processor (U5), shown in figure 1, is responsible for communications between the EAM/Modem Processor (U75) and the rest of the RT-1694. In many cases, the EAM/FEC Processor acts as a protocol converter, translating commands and statuses to and from the RT-1694 to commands and status understandable by the EAM Protocol Processor. The EAM section of the Signal Processor Assembly serves two functions; ALE functions and modem functions. Consequently, the EAM/FEC Processor is also responsible for coordinating ALE/MODEM switching for the EAM/Modem processors.

The 9.6 MHZ clock for the 83C51FA microcontroller is derived from the RT-1694 motherboard. It is buffered by U18 and fed to the XIN clock input pin on the microcontroller.

The reset to the 83C51FA microcontroller is derived from the POR (power on reset) signal from the RT-1694 motherboard. Buffer U66 inverts this signal and applies it to the microcontroller every time the RT-1694 is turned on, including the standby power-up.

The EAM/FEC Processor has the capability of resetting the 80186 processor at any time through the port pin P1-7 (RST186). This is primarily done when the radio switches modes between ALE and modem operation and the EAM/Modem Processor needs to start running from the beginning in a different mode, thereby requiring a reset.

The FFT reset is controlled both by the EAM/FEC Processor and the EAM/Modem Processor. This is implemented through the NAND gate U11. The FFT processor is reset whenever both control lines to the NAND gate are logic high.

The 83C51FA microcontroller has a built-in, full duplex, serial communications port (TXD and RXD). The EAM/FEC Processor communicates with other sections of the RT-1694 through these port pins at a data rate of 200 K baud. The RXD and TXD pins are tied together to the HSSB line.

U6, along with the ALE (Address Latch Enable) signal from the 83C51FA microcontroller, is used to demultiplex the combined address/data lines, A8 to A15 (latched internally to the 83C51FA microcontroller) are used to address program code in the ROM U7, general RAM U2, and dual-port RAM (DPRAM) U1.

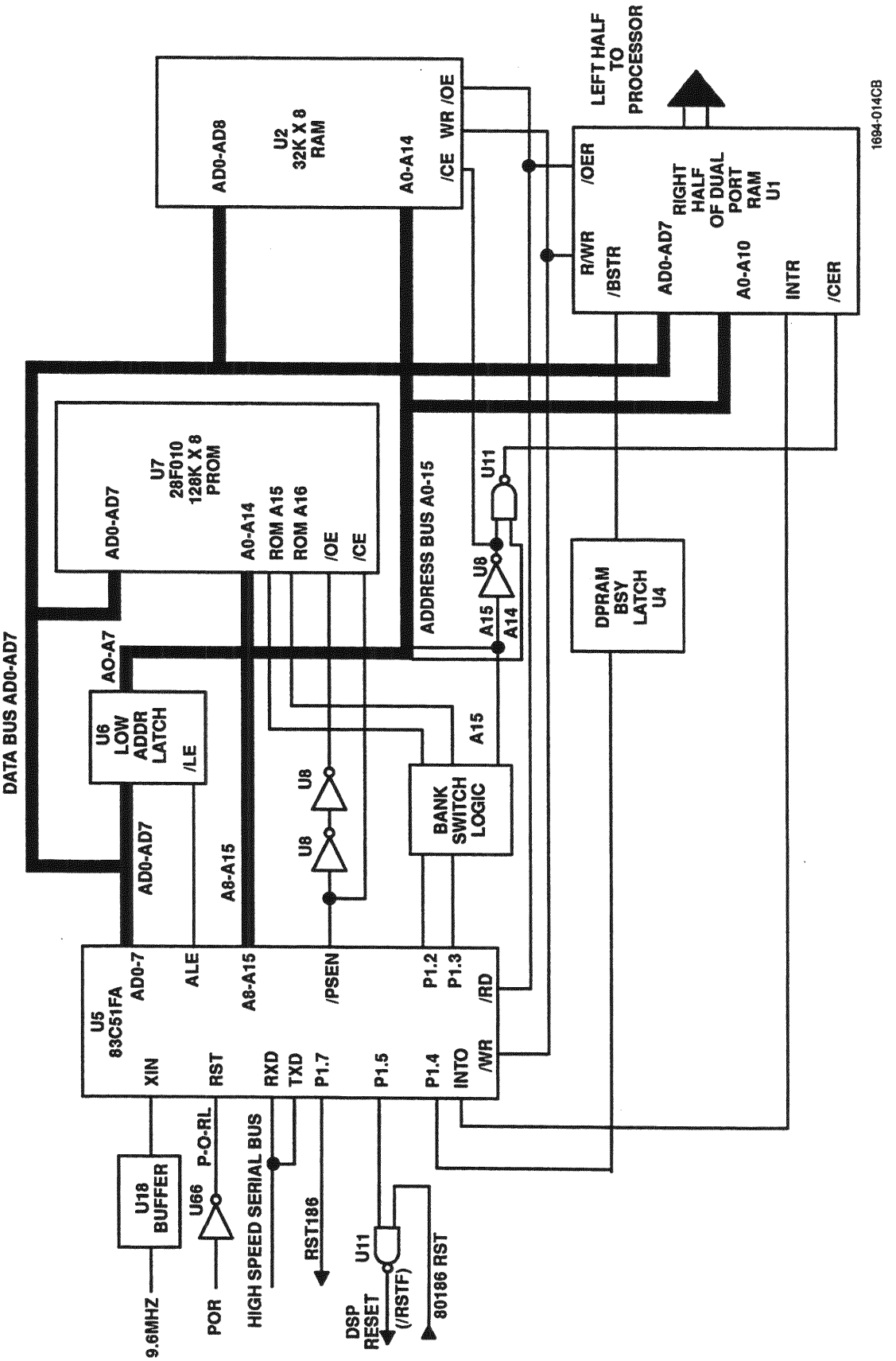


Figure 1. EAM/FEC Processor Block Diagram

3.1.1 Memory Access

During an instruction fetch by the 83C51FA microcontroller, program code is placed on the data bus, AD0 to AD7, when the PSEN strobe from the 83C51FA microcontroller U5 is low. PSEN is active low only when instruction fetches are being made by the 83C51FA.

General purpose RAM U2 is written to when address A15 is high and WR is low from the 83C51FA microcontroller. Data is read from the general purpose RAM U16 when microcontroller line A15 is high and RD from the 83C51FA microcontroller is low. WR and RD are only active when accessing data space (RAM). When accessing code space (ROM), PSEN acts as the read line, and the RD and WR signal lines remain inactive (high) preventing RAM data from being placed on the data bus at the same time as ROM instructions.

Communication between the EAM/FEC processor and the protocol processor takes place through dual-port RAM (DPRAM) U1. The EAM/FEC processor uses the right half of the DPRAM, and the protocol processor uses the left half. Access to the left half of the DPRAM U1 by the EAM/FEC processor is also governed by the RD and WR control signal lines. However, placement of data onto the data bus or writing of data from the data bus to the DPRAM is permitted only when address lines A15 is logic high and A14 is logic low. This prevents access of the DPRAM when the general RAM is desired (A15 is always a logic high when general purpose RAM is being addressed).

DPRAM U1 has two other status lines in addition to the normal read, write, and chip-enable lines. These lines are used to alert the EAM/FEC processor that the protocol processor has written something to it, or to prevent simultaneous access of the same memory location. Similar lines exist on the protocol processor's side of the DPRAM and serve the same purpose.

The U1, /INTL signal line alerts the EAM/FEC processor that the protocol processor has something for it to read. This signal line is asserted any time the protocol processor writes to a certain "mail-box" location in the RAM. This line is connected to the INT0 pin of the EAM/FEC processor and, when asserted, causes it to read what the protocol processor wrote from the DPRAM.

It is possible for the protocol processor and the EAM/FEC processor to both access the same memory location in the DPRAM at the same time. To arbitrate such a simultaneous access, the DPRAM determines which processor can have access to the disputed location. If it is determined the protocol processor had attempted an access first, the /BSTR signal pin on the DPRAM is asserted. This signal is latched by the DPRAM BSY LTCH circuit U4 and is read by the EAM/FEC processor on port 1, pin 4 (P1–4). Any access to the DPRAM by the EAM/FEC processor after latching occurs clears the DPRAM BSY LTCH U4 logic, arming it for detection of future simultaneous accesses.

3.2 EAM/Modem Processor (U75)

The EAM/Modem protocol processor U75, shown in figure 2, has a multiplexed address and data bus (DM0 – DM15). Therefore, the falling edge of the ALE (Address Latch Enable) signal is used to latch addressing information for the protocol resident address bus. Address Latch Enable is used as the latch enable for 8-bit resident bus address latches U3, U4, and U5

Resident RAM sites U78 and U79 are enabled onto the data bus by a combination of integrated chip select (LCS), protocol resident address bus (AMO), and bus high enable (BHE). That is, these inputs are applied to the high/low RAM byte chip select generation circuit. Protocol processor U2 accesses 16-bit words as even addresses only, and bytes as both even and odd addresses. All even byte accesses enable resident RAM site U79. All odd byte accesses enable resident RAM site U78. All word addresses enable both resident RAM sites.

Read and write signals (RD and WR) are active-low signals that are generated by EAM protocol processor U75 during the read and write cycles.

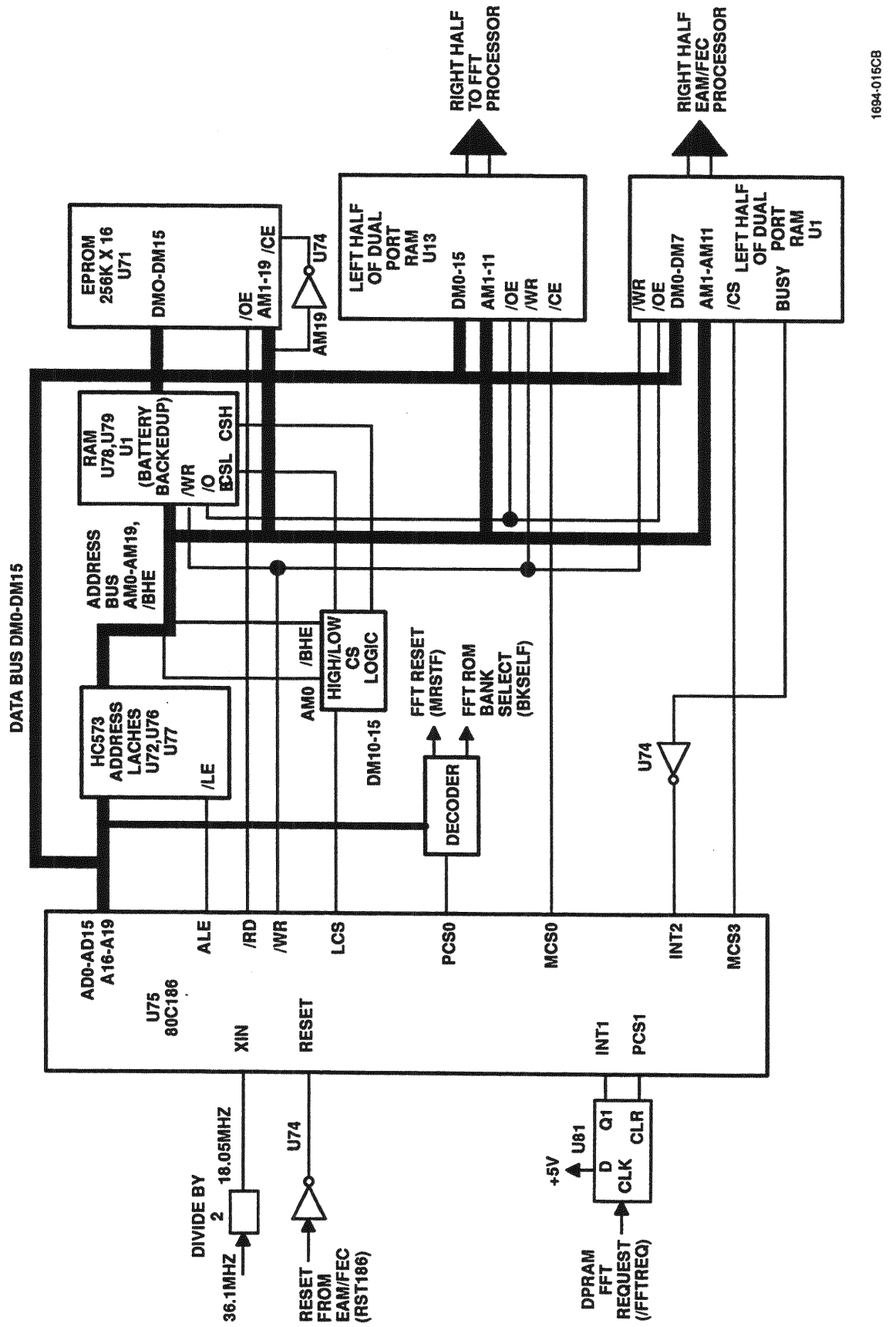


Figure 2. EAM/Modem Protocol Processor Block Diagram

3.3 FFT Digital Signal Processor (U65)

Refer to figure 3 for a detailed block diagram of this circuit.

3.3.1 General Operation

The FFT digital signal processor U65 operates at a frequency of 36.16 MHz. This frequency is internally divided by four into a two-phase clock. FFT digital signal processor U65 is reset by the active low signal/RSTF. This signal is generated by the EAM/Modem protocol processor U75 and EAM/FEC processor U5 through the NAND gate U11. The instruction cycle time is 111 nanoseconds.

3.3.2 Memory Access

The high-speed nature of the instruction cycle time of digital signal processor U6 makes high-speed memory a necessity. The access time of all memory must be less than 40 nanoseconds. This includes static memory and dual-port RAMS (that is, U69, U70, U13, and U80, respectively) which have access times of 35 nanoseconds.

Digital signal processor (U65) has 16 bits of address (AF0 – AF15) and 16 bits of data (DF0 – DF15). External data and program space overlap. This is achieved by having separate chip selects for program space (PS) and data space (DS).

The program space (PS) select signal is active low and is ORed with the FA15 address line to enable the UVEPROM (U64) onto the data bus. The UVEPROM is mapped in the lower 32 K of the address space, consequently the /XF line is used as the UVEPROM A15 address selection. The switching between 64K blocks on the UVEPROM is implemented through the BKSELF line from the EAM/Modem protocol processor. This switching is done primarily to toggle the FFT processor state between ALE and modem execution. When the Processor is executing ALE, this pin on the UVEPROM (pin 42) should be logic high.

The FFT digital signal processor high-speed static memory is accessed at address 8000-FFFFH. FFT digital signal processor U65 signals R/W and STRB are used to determine if the processor is executing a read or a write cycle when accessing the dual-port RAM. The Chip select for both of the dual port RAM devices U80 and U13 are provided through a 1:4 decoder U67, which is accessed through address line AF14 and AF15 and the data strobe line DS. The Address of the DIGIF DPRAM (U80) is 4000-47FFH, while the EAM/Modem DPRAM address is 1000-17FFH.

3.3.3 Interrupt Structure

Dual-port RAMS U80 and U13 do not have built-in interrupts, so the FFT processor must manually alert the DIGIF and EAM/Modem processors whenever data is written/read into the respective DPRAM. The Address line AF0 in combination with the ISF signal are used to service these interrupts. The FFTREQ signal generates an interrupt on the EAM/Modem processor. It is generated by writing to the Signal Processor I/O location 0. The DIFATN signal is used to interrupt the DIGIF processor. This interrupt is generated by writing to the signal processor I/O location 2.

FFT digital signal processor interrupt 0 is generated by the EAM/Modem protocol processor. It is used to alert the digital signal processor that there is valid data in the dual-port RAM (U13). This interrupt is latched in on the flip flop U81, consequently the FFT processor writes to I/O space address 3 to clear the interrupt.

FFT digital signal processor interrupt 1 is generated by the DIGIF at a 24 kHz rate. This interrupt signals the FFT processor that there is valid audio data in the dual-port RAM (U80).

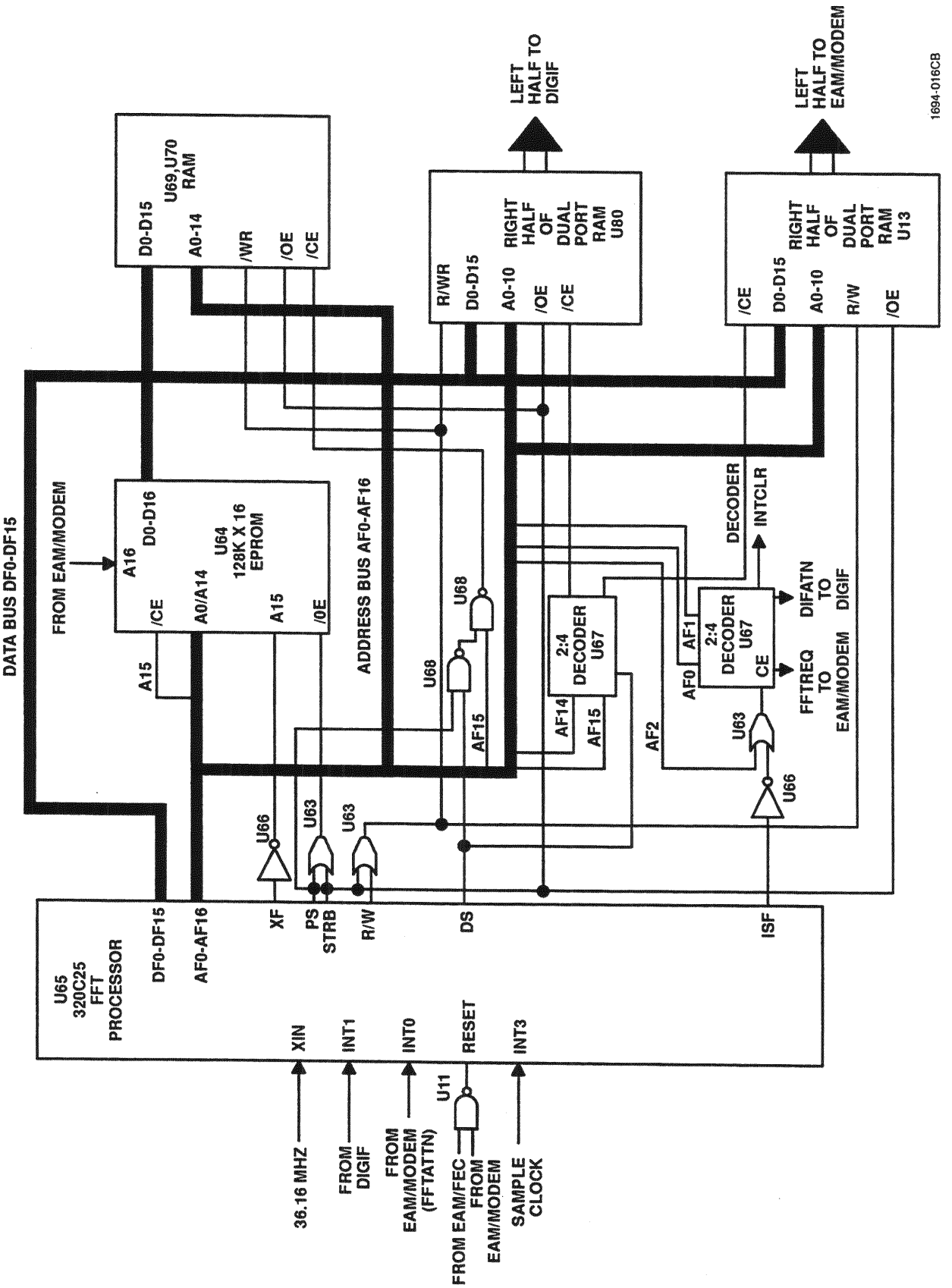


Figure 3. FFT Block Diagram

4. ALE REMOTE OPERATION

4.1 Link Quality Analysis (LQA) Data

The ALE Module automatically selects the optimal frequency to be used for a communications link with one or more remotely-located stations (outstations). The optimal frequency choice depends upon a number of factors which include the:

- Distance between the local station and outstation
- Time of day
- Noise or radio interference on one or more of the frequencies being evaluated

The ALE Module selects the best frequency for communication using a process called Link Quality Analysis (LQA). During an LQA sequence, signal quality is measured at a number of frequencies between pairs of HF radio stations. The measurements are stored, ranked according to link quality, then used to select the optimum channel for link establishment.

Each channel score is a weighted average of signal + noise + plus distortion to noise + distortion ratio (SINAD) and bit error rate (BER) accumulated over the entire signalling interval. The scores range from 0 to 100, where 100 is the best attainable score.

The controller is capable of passing the measured signal quality to one or more of the outstations. The station at each end of the path stores the LQA score.

The ALE Module uses two LQA methods: the sounding LQA method and the bidirectional or exchange LQA method.

4.1.1 Sounding LQAs

A sounding LQA is a sequence of short, unidirectional messages sent at regular intervals by the calling unit on all the channels programmed for one of its self addresses. The calling unit uses the self address to identify itself to the receiving units. The receiving unit (or units) detects the sound, temporarily stops scanning, measures and stores the received signal quality as a score, and resumes scanning.

Figure 4 shows an example of the sounding LQA process. An initiating station with the self address of UT1 starts the process. Initiating station UT1 is assigned three channels: 0, 1, and 2. The three target stations UT2, UT3, and UT4 have channels 0, 1, and 2 included in their scan set.

Initiating station UT1 begins the sounding LQA process on the highest-frequency channel (channel 2 in figure 4). When the sounding message is received, the three target stations (UT2, UT3, and UT4) stop scanning on channel 2, measure the received signal quality, compute the score, and store the score for the UT1/channel 2 combination in memory. The target stations then return to scan mode.

Once initiating station UT1 has completed the sounding LQA process on the highest-frequency channel, it repeats the process on the next highest-frequency channel. This continues until all channels have been sounded by the initiating station, from highest frequency to lowest frequency.

Upon completion of the sounding LQA process, stations UT2, UT3, and UT4 have measured the signal quality from UT1 on channels 0, 1, and 2. Initiating station UT1 returns to scan mode. The initiating station does not know how well the receiving stations detected its sounding message. If a target station fails to detect the sounding message, the UT1 channel score is not updated in its memory.

4.1.2 Bidirectional LQA Method Description

A bidirectional LQA uses a three-way message exchange, during which two or more stations measure and exchange received signal-quality information. This differs from a sounding LQA in that the initiating and target station exchange link-quality information during the LQA. A bidirectional LQA may be performed between individual stations, a net member station and other members of the same net, or a group member and other members of the group.

4.1.2.1 Individual LQA

Figure 5 shows the exchange of signals in an individual bidirectional LQA. An initiating station with the self address of UT1 begins a bidirectional LQA with a target station with self address UT2. Initiating station UT1 is assigned four channels: 3, 2, 1, and 0. Target station UT2 has channels 0, 1, 2, and 3 included in its scan set.

Station UT1 initiates the bidirectional LQA process by transmitting a call message (step 1) on the highest-frequency channel (channel 3). When the signal is received, target station UT2 stops scanning on channel 3, continues to receive the call message, and measures the received signal quality. The received signal quality value is stored by target station UT2 as a RX score.

Upon reception of the call message, target station UT2 sends a response message (step 2) to initiating station UT1. The response message includes the score measured by target station UT2 while receiving the call message. When initiating station UT1 receives the response message, it stores the score as a TX score and measures the received signal quality. The resulting value is stored in UT1's memory as a RX score.

Initiating station UT1 then sends an acknowledgement message (step 3) to target station UT2. This message contains the score measured by UT1 while receiving the response message. Target station UT2 stores the score sent by UT1 (sent as a TX score), and measures the received signal quality. The score computed during reception of the acknowledgement message is used to update target station UT2's RX score.

At the completion of the message exchange, both initiating station UT1 and target station UT2 have stored TX and RX. These scores are combined to produce a bidirectional score for the channel. The concluding portion of the acknowledgement message commands target station UT2 to return to scan mode.

Initiating station UT1 continues the bidirectional LQA process by transmitting a call message (step 4) on channel 2, the second highest-frequency channel. This is followed by response and acknowledgement messages (steps 5 and 6). When this process is complete, both systems contain channel-quality information as bidirectional scores for channel 2.

The bidirectional LQA process continues until all channels assigned to target station UT2 have been called (steps 7 through 14). The possibility exists that one or more of the channels has degraded to a point where target station UT2 cannot detect the incoming ALE signalling. In that case, no signal-quality information is available and the scores are not updated.

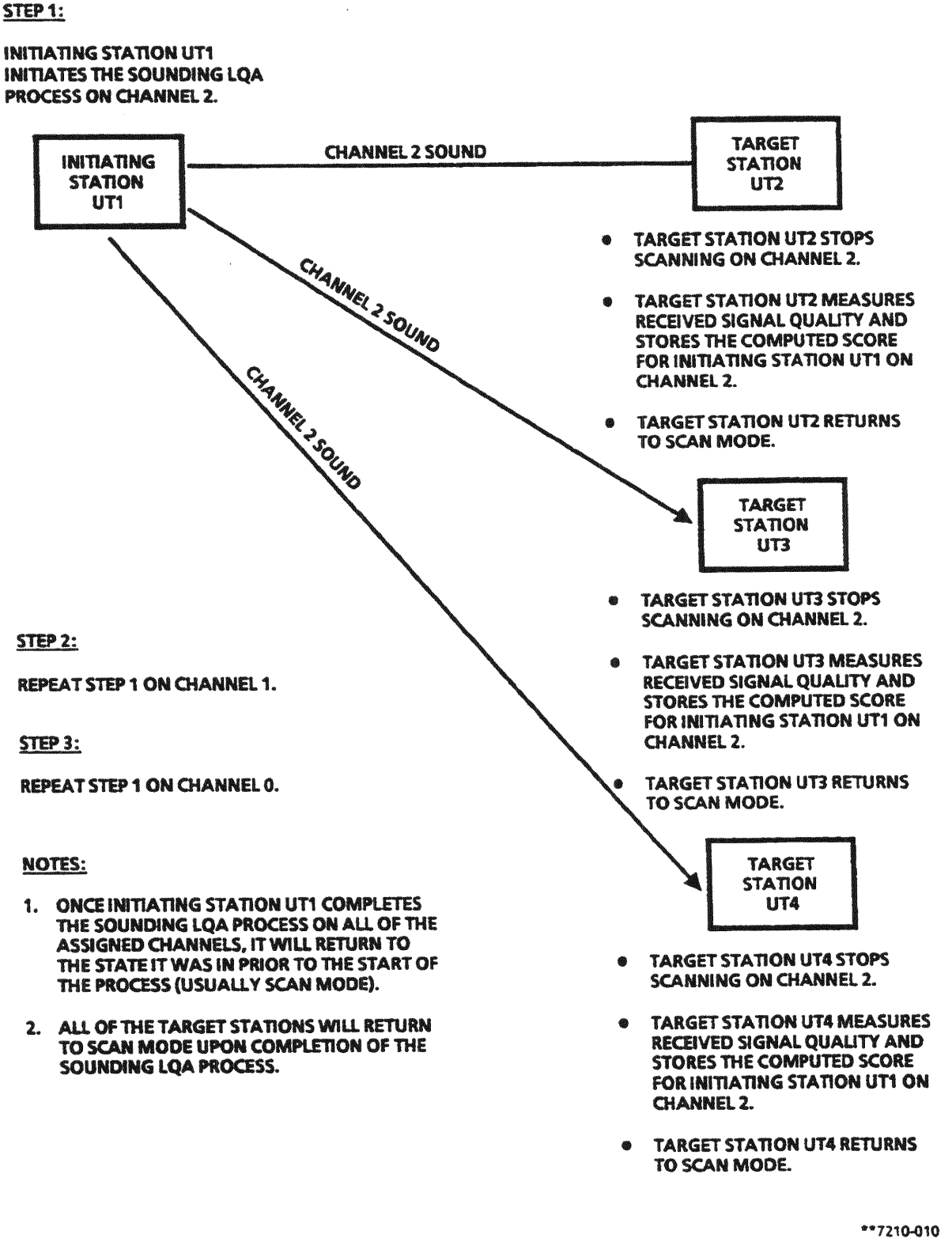


Figure 4. Sounding LQA Process Signal Exchange

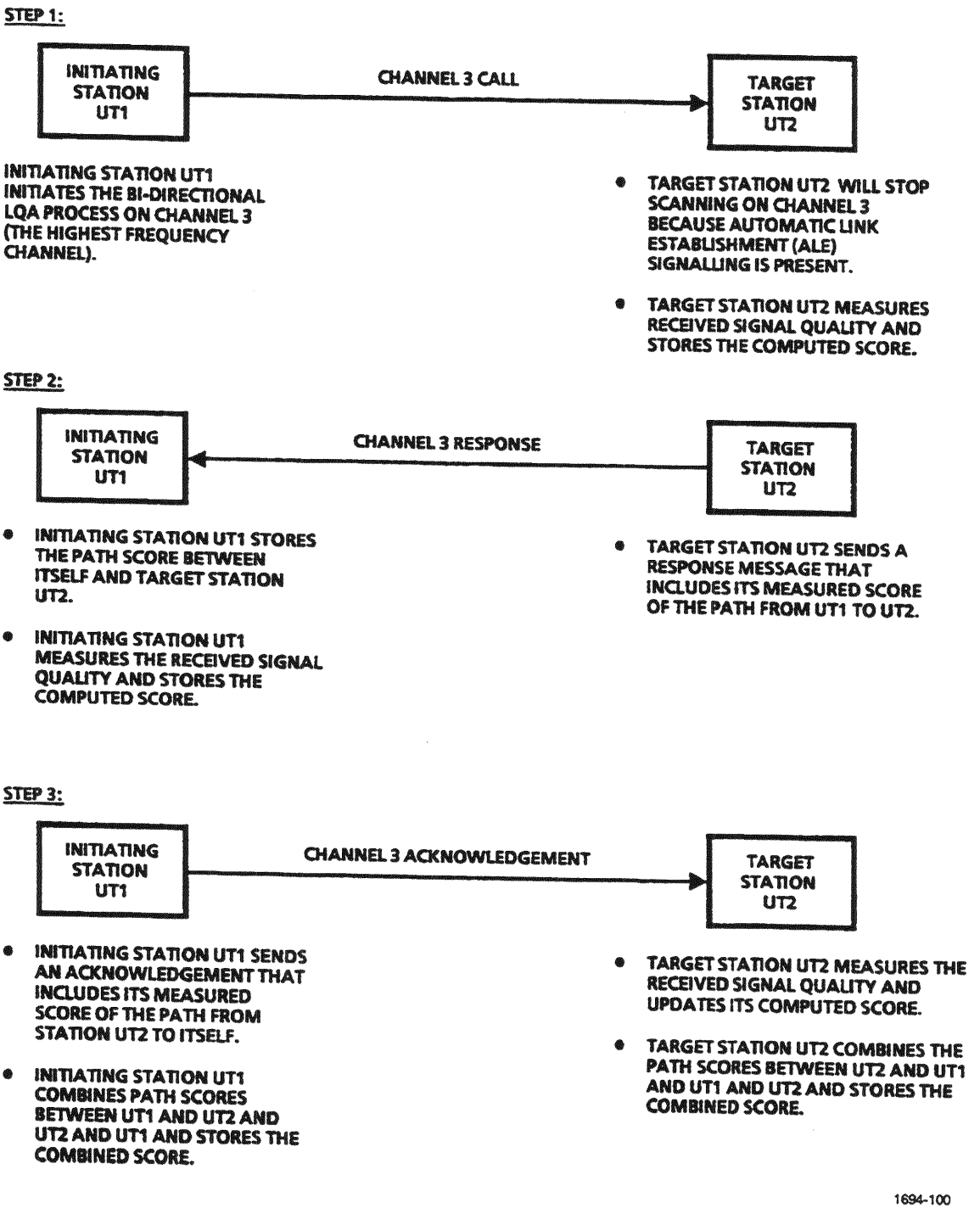


Figure 5. Bidirectional LQA Process Signal Exchange (Sheet 1 of 4)

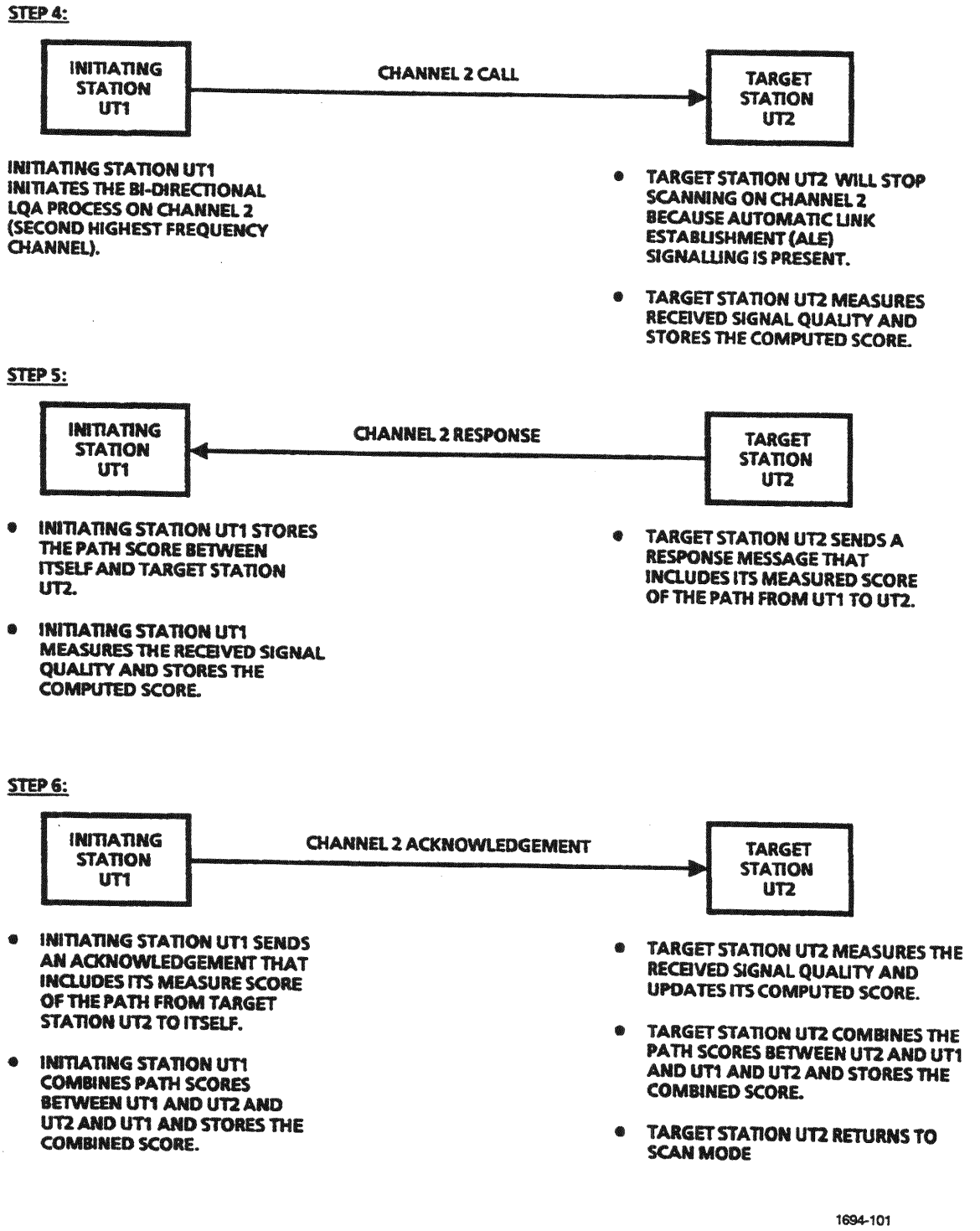


Figure 5. Bidirectional LQA Process Signal Exchange (Sheet 2 of 4)

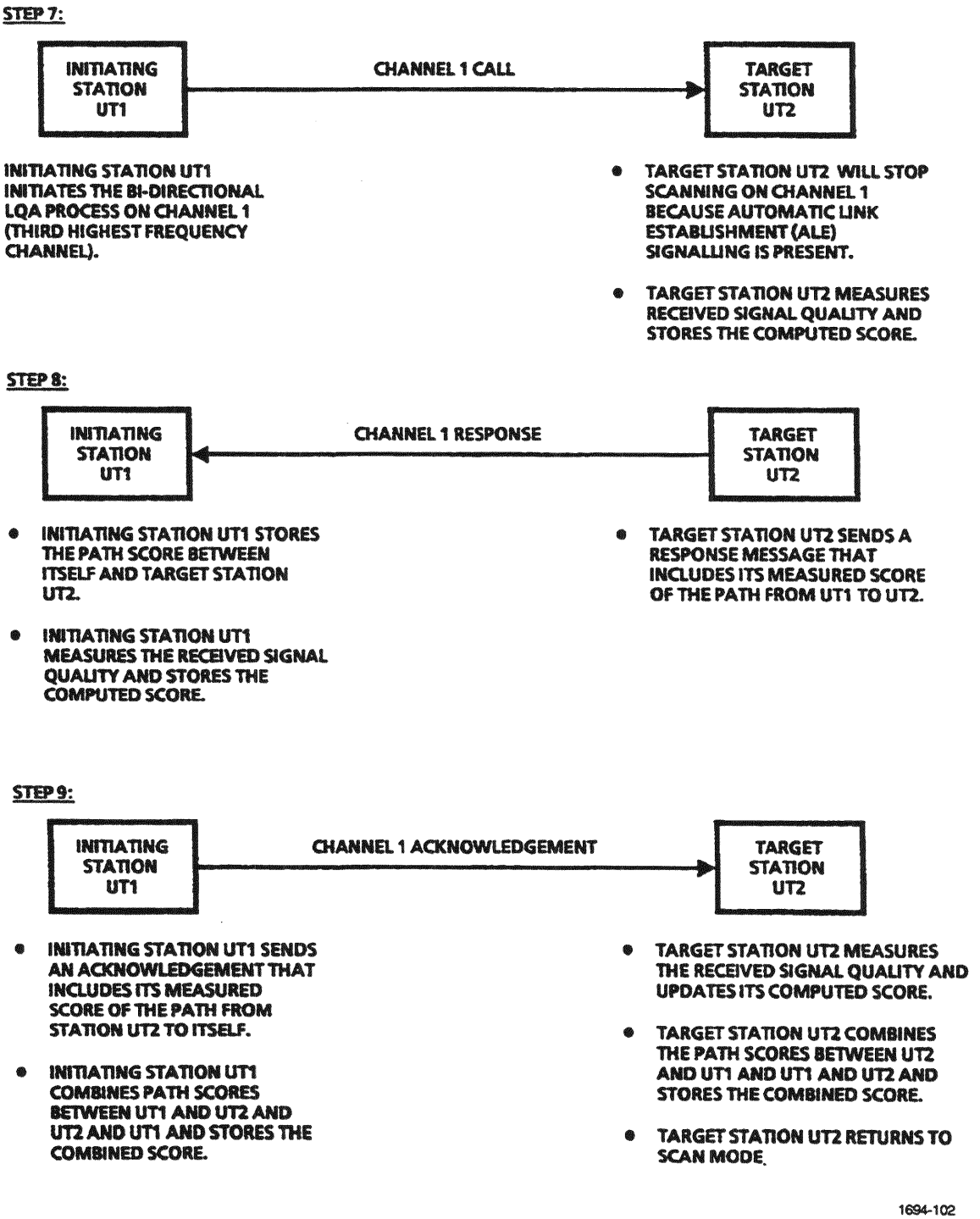


Figure 5. Bidirectional LQA Process Signal Exchange (Sheet 3 of 4)

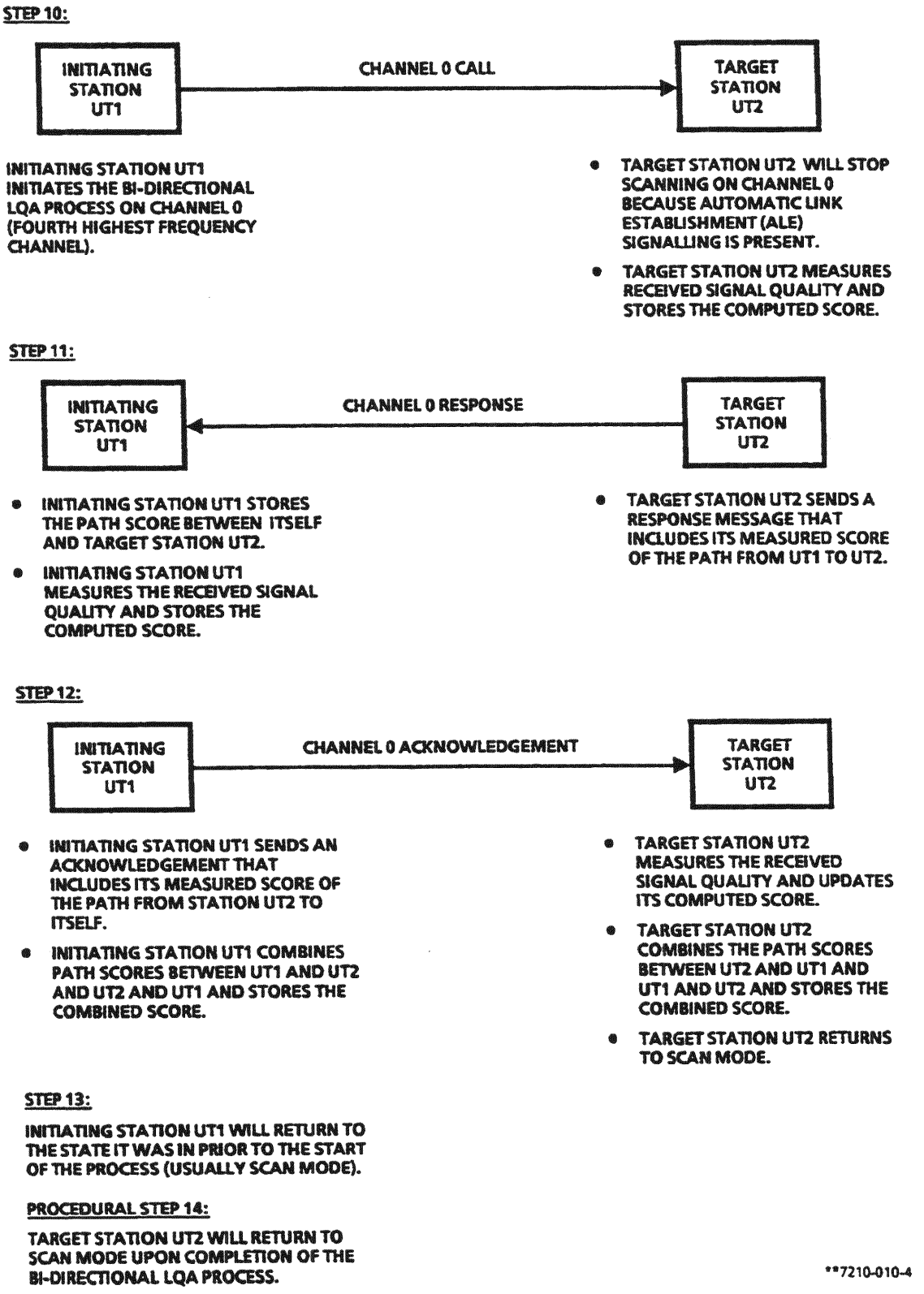


Figure 5. Bidirectional LQA Process Signal Exchange (Sheet 4 of 4)

4.1.2.2 Net and Group LQAs

In net and group bidirectional LQAs, the receiving units transmit response messages in time-slotted order. The response messages contain the scores measured by the net members during reception of the initial call message. The net or group call initiator measures signal quality during reception of the slotted responses and updates each individual member's score accordingly. No scores are sent in the acknowledgement message portion of a net or group call.

The individual, net, and group LQA signal exchanges are virtually identical to the corresponding call signal exchanges. The only difference is in the concluding portion of the acknowledgement message. In a bidirectional LQA, this commands the receiving units to return to scan mode. In an individual, net, or group call, the concluding portion of the acknowledgement message commands the receiving units to link on the current frequency.

Upon completion of the bidirectional LQA process, the scores in the transmit and receive units represent the quality of the transmit and receive paths for all channels on which the procedure was performed.

NOTE

The AN/PRC-138 System which is equipped with the ALE Module can only receive group LQAs. It cannot initiate group LQAs.

4.2 Call Setup to Outstations

4.2.1 General Information

The ALE Module can communicate and establish a link with a single outstation, a set of outstations, or all outstations that can receive its transmissions. The following is a list of all of the types of calls that can be placed or received by the ALE Module:

- Manual and auto individual calls (transmit and receive)
- Manual and auto net calls (transmit and receive)
- Manual and auto group calls (receive only)
- Special calls (transmit and receive):
  - Manual and auto allcalls (including selective allcall [only via remote control])
- Special calls (receive only):
  - Manual and auto anycalls (including selective and double selective anycalls [only via remote control])
  - Wildcard calls

In the case of a manual call, the operator explicitly specifies the channel on which the call is to be placed. In the case of an auto call, the controller selects the best channel on which the call is to be placed, based on the latest corresponding LQA information.

4.2.2 Individual Calls – Descriptive Information

An individual call is used to establish communication (connection) between two stations. An individual call may be placed to any programmed individual address.

4.2.2.1 Manual Individual Call Protocol

Figure 6 shows the exchange of signals during a manual individual call. Initiating station UT1 begins the process by transmitting a call message (step 1) to target station UT2 on a manually-selected channel. The length of the call message is determined by the MAX SCAN CHANNELS system parameter. Target station UT2 stops scanning on a channel when ALE signalling is present. If target station UT2 determines that the call is addressed to it and that it is on a valid channel (that is, on its channel list), it stays on the channel and continues to receive the call message.

Once the call message has been received, target station UT2 sends a response message (step 2) to initiating station UT1. Upon receipt of this response message, initiating station UT1 sends an acknowledgement message (step 3) confirming receipt of the response message. Once the acknowledgement message transmission is completed, initiating station UT1 changes to the linked state and updates the front-panel display. When target station UT2 completes reception of the acknowledgement message, it changes to the linked state, updates the display, and enables its call alert beeper. Both systems are now ready to exchange voice or data information. For the two systems to link, it is necessary that all three portions of the message exchange (call, response, and acknowledgement) are received correctly.

4.2.2.2 Automatic Individual Call Protocol

To place an automatic individual call to a specified target, the controller selects the best channel on which to link. This selection is based on the current score data stored in the LQA matrix. The score data is the result of the most recent sounding or bidirectional LQA process with the specified station. If communications cannot be established on the best channel, initiating station UT1 attempts a call on the next best channel. If the channel scores are the same or there are no scores present, the higher-frequency channels have precedence while placing an automatic call. An attempt is made on all channels assigned to an individual address until a link is established. If a link cannot be established with any of the channels attempted, the initiating station's controller displays a NO RESPONSE message.

4.2.3 Net Calls – Descriptive Information

A net (or star net), as defined in the MIL-STD-188-141A specification, is a prearranged collection of stations. Typically, one of the stations in the net initiates a call, and becomes (for that call) the net control station. A net call is a very efficient method to link with many stations. It is more organized than a group call. Unless specifically excluded, every station programmed in the net can initiate a call to that net.

The exchange of signals for a net call protocol is shown in figure 7. Net ABC consists of initiating station UT1 and target stations UT2, UT3, and UT4. Initiating station UT1 begins the net call (step 1) by sending a call message to net ABC. The stations in the net stop scanning on the calling channel and receive the call.

After the call message has been received; target stations UT2, UT3, and UT4 respond (step 2) in their predetermined time slots 1, 2, and 3, respectively. Initiating station UT1 collects the slotted responses and the front-panel display of UT1 indicates the reception of each response.

After the last response is received, initiating station UT1 sends an acknowledgement message (step 3) to the net ABC members. After the members receive the acknowledgement message, they change to linked state, update their displays, and enable their call alert beepers. Initiating station UT1 also goes into the linked state.

If, after the call message has been sent, initiating station UT1 receives no responses, no acknowledgement message is sent. If any members respond, the acknowledgement message is sent.

To place an automatic net call, the controller selects the best channel on which to link. This selection is based on the current score data stored in the LQA matrix. The score data is the result of the most recent sounding or bidirectional LQA process.

If communications cannot be established on the best channel, initiating station UT1 attempts a call on the next best channel. If the channel scores are the same or there are no scores present, the higher-frequency channels have precedence. While placing an automatic call, attempts are made on all channels assigned to a net address and continue until a link is established. If a link cannot be established on any of the channels attempted, the initiating station's controller displays a NO RESPONSE message.

NOTE

In order for the NET to operate properly, all stations must be properly programmed. Exercise care when time slots are programmed so each NET member will have the same time slot.

4.2.3.1 Assignment Of Time Slots – Programming Considerations

When placing net calls, slot width is computed automatically, based on the address length of the net members and the turn-around/propagation time. The assignment of time slot widths by the operator is not supported by the AN/PRC-138 System when equipped with an ALE Module.

4.2.4 Group Calls

A group (or star group) is an informal collection of stations which, like a star net, can link and interoperate. The initiating station functions as the group control station. A group differs from a net in that target members of a group do not to have to be preprogrammed.

A group call rapidly and efficiently establishes connection or contact with a small number of stations. In most cases, little or nothing is known about the stations, except their individual addresses and scanned frequencies. Unlike a net call, a group call cannot have preset slots. The responses made by group members is based on the structure of calls which are actually received. The exchange of signals during a group call is shown in figure 8.

NOTE

An AN/PRC-138 System that is equipped with the ALE Module can only receive group calls. It cannot initiate group calls.

STEP 1:

- STATION UT1 INITIATES THE CALL BY ENTERING TARGET STATION UT2'S ADDRESS AND CHANNEL NUMBER.
- INITIATING STATION UT1 SENDS THE CALL MESSAGE.
- TARGET STATION UT2 WILL STOP SCANNING BECAUSE AUTOMATIC LINK ESTABLISHMENT (ALE) SIGNALLING WAS DETECTED.
- TARGET STATION UT2 WILL STAY ON THE CHANNEL AND CONTINUE RECEIVING THE CALL MESSAGE.

STEP 2:

- INITIATING STATION UT1 RECEIVES THE RESPONSE MESSAGE.

WHEN TARGET STATION UT2 HAS DETERMINED THAT THE CALL IS ADDRESSED TO IT, IT SENDS A RESPONSE MESSAGE.

STEP 3:

- WHEN INITIATING UT1 RECEIVES A RESPONSE AND DETERMINES THAT THE RESPONDER'S ADDRESS IS VALID, IT SENDS AN ACKNOWLEDGEMENT MESSAGE.
- INITIATING STATION UT1 CHANGES TO A LINKED STATE, AND UPDATES ITS DISPLAY.
- ONCE TARGET STATION UT2 RECEIVES THE ACKNOWLEDGEMENT MESSAGE, IT CHANGES TO A LINKED STATE, UPDATES ITS DISPLAY, AND ENERGIZES THE AUDIO BEEPER.

INITIATING STATION UT1 AND TARGET STATION UT2 ARE NOW READY FOR DATA/VOICE TRAFFIC.

**7210-011

Figure 6. Manual Individual Call Signal Exchange

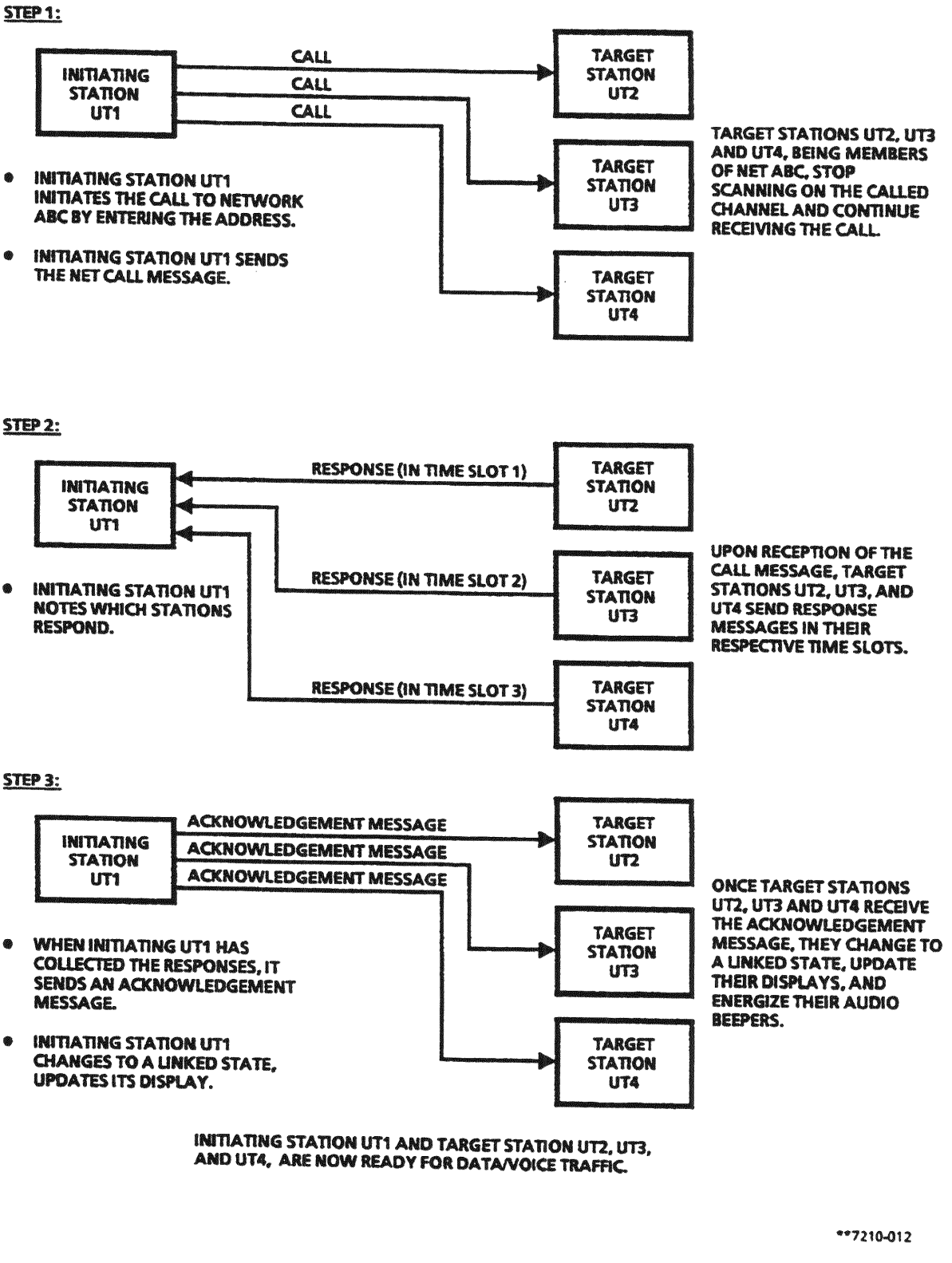


Figure 7. Net Call Protocol Signal Exchange

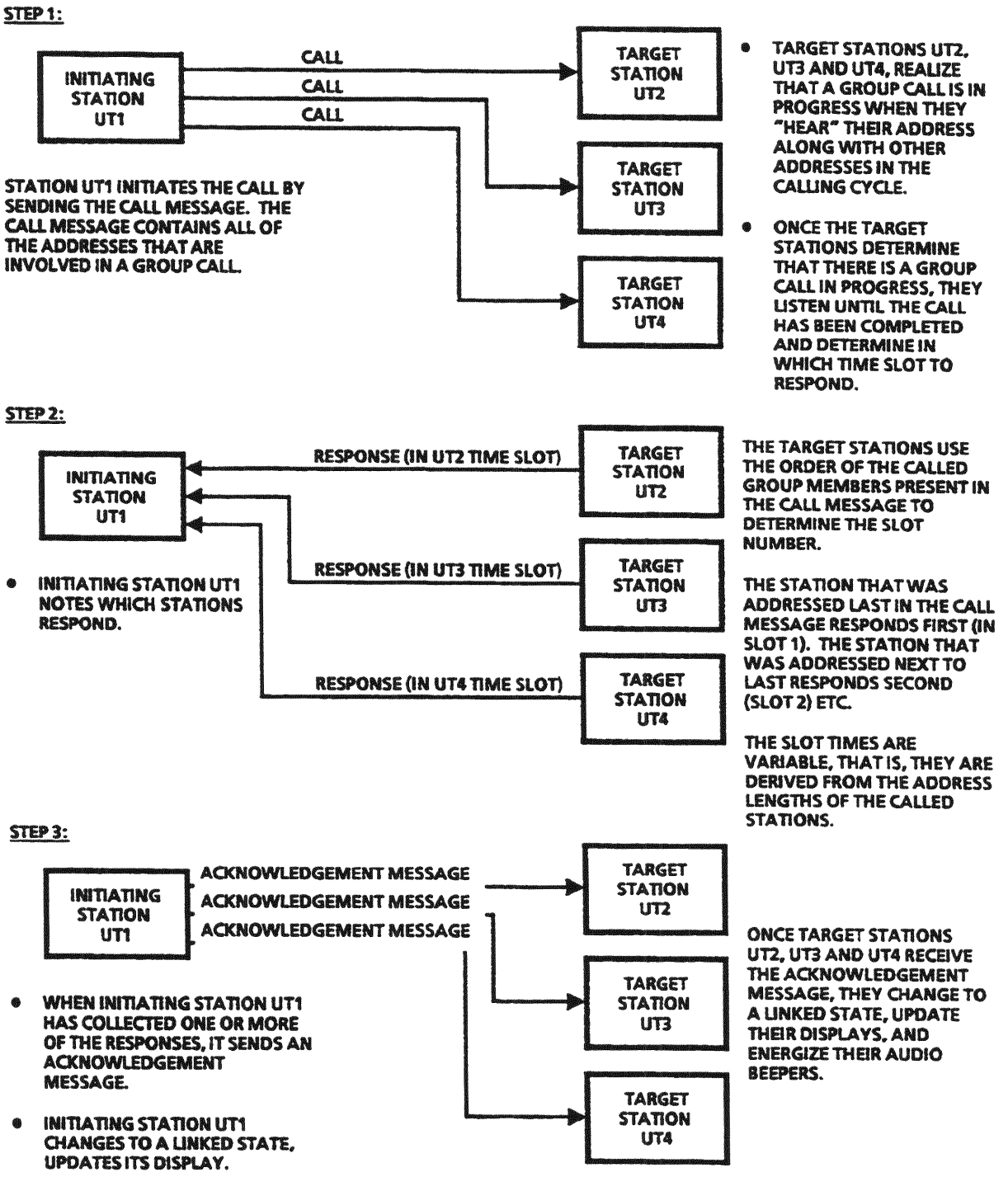


Figure 8. Group Call Protocol Signal Exchange

4.2.5 Special Calls

4.2.5.1 Allcalls

An allcall is a general broadcast which does not designate a specific address and does not request a response. An allcall message is unidirectional and contains an allcall identifier and the initiating (calling) station's address. When an allcall message has been successfully received, the receiving stations change to the linked state and are ready for voice or data communication.

The initiating station is able to organize the available receiving stations using selective allcall. Selective allcall is identical in structure and function to allcall, except that it specifies the last character in the address of the desired subgroup of receiving stations.

4.2.5.2 Anycalls

An anycall is a general broadcast that requests responses without designating specific addresses. An anycall provides the adaptive system the ability to identify new stations. This protocol is used for emergencies, reconstitution of systems, and creation of new networks.

The call message contains the anycall identifier and the address of the initiating (calling) station. Upon receiving the call, the target station or stations stop scanning, receive the rest of the message, and prepare to respond in randomly-selected time slots.

Each target station randomly selects a time slot and uses it to send its response message. Collisions (two or more target stations selecting the same time slot) are possible and are tolerated. After the maximum wait for response time (44 seconds) has elapsed, the initiating station sends an acknowledgement message to those stations which have responded. If no stations respond, no acknowledgement message is sent.

The initiating station is able to organize the available, but unspecified, receiving stations into subsets using selective and double-selective anycall. Selective and double-selective anycall are identical in structure, and function like global anycall except that they specify the last character in the addresses of the desired subset of receiving stations (selective anycall) or the last two characters in the addresses of the desired subset of receiving stations (double-selective anycall).

NOTE

An AN/PRC-138 System that is equipped with the ALE Module can only initiate selective and double selective anycalls from remote.

4.2.5.3 Null Address Calls

A null address call is used for test and maintenance purposes. When the null address is received, the receiving stations suspend scanning (due to the presence of ALE signalling on the channel), but almost immediately return to scan mode once the null address call has been identified.

If a null address appears in a group call, no station is designated to respond in the associated slot.

NOTE

An AN/PRC-138 System which is equipped with the ALE Module can only receive null calls. It cannot initiate null calls.

4.2.5.4 Use of Wildcards In Addresses

A wildcard is a special character used by the calling station to address multiple station addresses with a single call address. The initiating station uses a question mark (?) as the wildcard character. The target station accepts the wildcard character as a substitute for any alphanumeric character in the same position. For example, if a call is made to the address ???, all stations having at least one three-character self address accept the call. An address may not be programmed with a wildcard character, but it may be entered when placing a call to an individual, net, or group.

Upon reception of a wildcard call, the target station or stations randomly determine a slot number (between 1 and 16) and respond in that slot. The initiating station sends an acknowledgement message to all stations that responded. A wildcard call is similar to an anycall.

NOTE

An AN/PRC-138 System which is equipped with the ALE Module can only receive wildcard calls. It cannot initiate wildcard calls.

4.3 Link Termination

Link termination is used to cause resumption of scanning by one or more outstations. Link termination commands are sent by the initiating station of any call (individual, net, group, allcall, anycall, etc.). A link termination command is sent automatically by the target station in an individual call. The link termination command is sent when the CLR button is pressed while the system is in linked state. A link termination command is not sent by the target station for a call that involves more than two stations. (For example, net calls.)

5. ALE STANDBY OPERATION

Standby operation is a key feature to the AN/PRC-138 Manpack radio. This mode enables the radio to reduce its power consumption significantly during receive scanning operation by quickly powering up, performing a quick scan of all channels being scanned by ALE, and (if no signal is present) powering down the radio for a pre-determined amount of time before repeating the process. This power-down time (idle time) is dependant on the timing of the MIL-STD-188-141A ALE signal, so the receiver is guaranteed to scan over a valid call at least once.

5.1 Overview

Whenever one ALE station places a call to an addressee that is assumed to be scanning multiple channels, a scanning call (Tsc) is appended to the beginning of the call to capture the receiver. This call is transmitted only on the channel currently being called. The standard length of the preamble is (2 x N x .392) seconds long, where N is the maximum number of channels to scan. It is during this interval that the receiver must recognize that a call is being made so that it may stop scanning to listen for further information. Therefore, as a minimum requirement, the receiver must evaluate every potential channel at least once during the Tsc interval.

The following is the overall approach to attain this fast scan/sleep mode of operation:

- To initiate a Fast Scan, all essential parts of the radio (Interface, ALE, Main Controller, AGC) are brought up and working.
- ALE is told to scan through its scan list one time.
- If a signal is detected, ALE processes the call normally. The radio continues in traffic mode until either a link termination is received, a link timeout occurs, or the user forces scan. After any of these events, the radio returns to standby.

- ALE informs the front panel if no ALE signal is received. ALE is then suspended until further notified.
- The front panel powers down the radio and waits for the idle time (dependant on number of channels scanned), after which the process is repeated.
- During standby operation, any front panel operations that access ALE are processed in the normal way.

6. TESTING AND ALIGNMENT

This module requires no testing or alignment procedures.

7. BITE FAULTS AND TROUBLESHOOTING LIST

There are no bite faults for this module. This subsection contains the most common problems that can occur and offers solutions.

Problem: Front Panel/Remote displays ALE NOT INSTALLED

Solution(s):

a. Check if LPC Assembly is installed (needed to enable ALE option).

b. Check for presence of EAM processors using Revision Report feature.

c. Check for Vcc, Clocks, and reset on EAM processors U5, U75, and U65.

d. Check for bus activity (ALE, Address Line PSEN, WR, RD, etc.) on EAM processors U5, U75, and U65.

e. Check for dual port RAM (U1 and U13) activity (interrupts, bus activity, etc.).

f. Check DIGIF Sample Clock (U65) – should be 24 kHz square wave.

g. Check for HSSB activity.

Problem: ALE powers up, but does not scan

Solution(s):

a. Make sure ALE is programmed with necessary parameters (Self Address, Individual Address, and channels).

b. Check EAM TMS processor (U65) is running (bus activity, etc.).

c. Check EAM TMS UV EPROM U64 pin 42 for logic High.

d. Check EAM TMS processor (U65) reset line (should be low).

e. Check for dual port RAM (U1 and U13) activity (interrupts, bus activity, etc.).

f. Check DIGIF Sample Clock (U65) – should be 24 kHz square wave.

g. Dual Port Interrupt (Int1 on U65) should be at a 24 kHz rate.

Problem: ALE scans, but does not transmit.

Solution(s):

a. Check EAM TMS processor (U65) is running (bus activity, etc.).

b. Check EAM TMS UV EPROM U64 pin 42 for logic High.

c. Check EAM TMS processor (U65) reset line (should be low).

d. Check for dual port Ram (U1 and U13) activity (interrupts, bus activity, etc.).

e. Check DIGIF Sample Clock (U65) – should be 24 kHz square wave.

f. Dual Port Interrupt (Int1 on U65) should be at a 24 kHz rate.

g. Check transmit path.

h. Check for proper PA/Coupler operation – do VSWR test.

Problem: ALE works, but does not go into Standby.

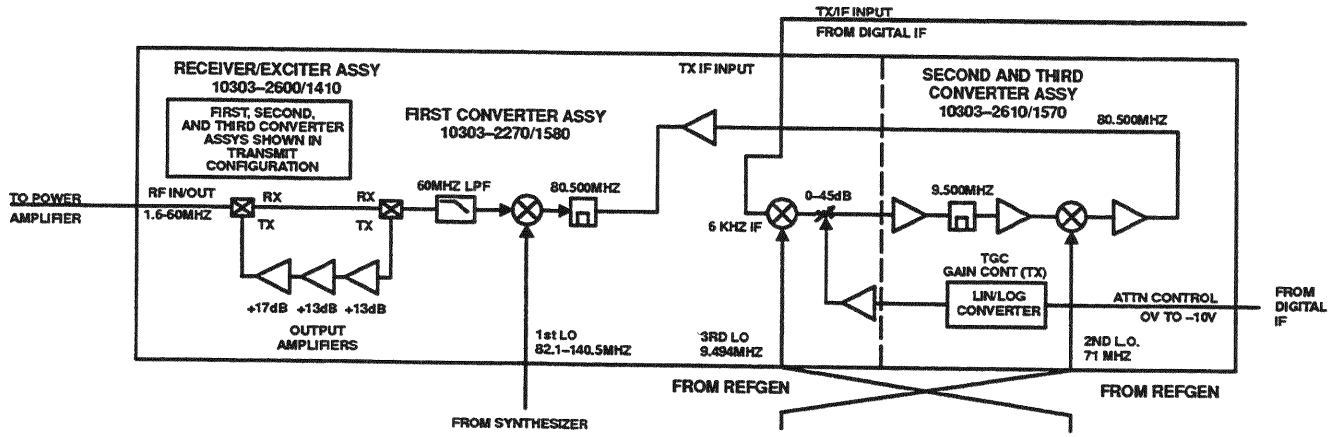
Solution(s):

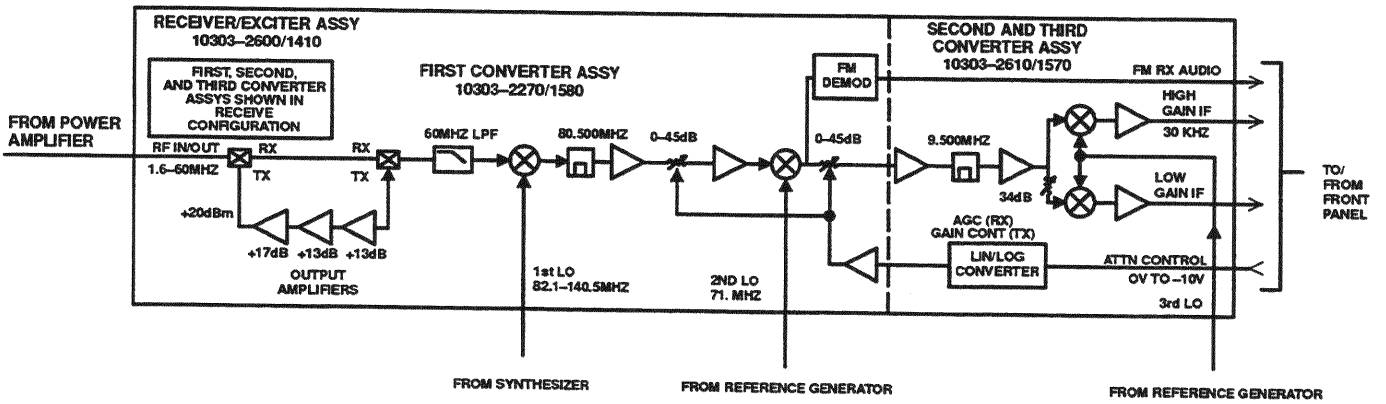
a. Make sure ALE is in local scan operation – standby does not take effect while in Remote, Linked, Manual Channel, and External Power operation.

b. Check that Debug Standby response (in Remote) is Standby Enabled.

c. Make sure ALE MAX SCANNED CHANNELS programming parameter is correct (large value will effect standby timing).

A5
RECEIVER/EXCITER





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A5 RECEIVER/EXCITER

1. GENERAL DESCRIPTION

The A5 Receiver/Exciter Assembly (10303-2600) consists of two separate subassemblies:

- First Converter Assembly (10303-2270)
- Second and Third Converter Assembly (10303-2610)

In receive mode, the A5 Receiver/Exciter Assembly converts HF and VHF signals in the 1.6 to 60 MHz range to a 30 or 36 kHz intermediate frequency, depending on the mode, for further processing in the Signal Processor Assembly (10303-2500). In transmit mode, the A5 Receiver/Exciter Assembly converts a 6 kHz intermediate frequency from the Signal Processor to a RF output at 100 milliwatts.

1.1 Receive Signal Path

Refer to figure 1, a block diagram of the A5 Receiver/Exciter Assembly receive path, during the following description.

The receive function of this assembly is carried out by a triple-conversion, super-heterodyne receiver. Modulated RF signals in the 1.6 to 60 MHz range, present at the First Converter Assembly, are lowpass filtered, converted up to the 80.5 MHz first IF, filtered to 22 kHz bandwidth, and amplified before being processed by the Second and Third Converters.

The Second Converter mixes the first IF down to the 9.5 MHz second IF. In FM receive mode, the second IF is demodulated and lowpass filtered to provide an audio output to the signal processor. In any other mode, the second IF is amplified, filtered to 8 kHz bandwidth, and amplified again before entering the Third Converter.

At this point the signal is split into two paths, with one path attenuated by 34 dB with respect to the other. The lower level IF is used in frequency hoping mode to avoid AGC processing and response time and allow a faster hop. Both 9.5 MHz second IF signals are independently converted down to a 30 or 36 kHz third IF, amplified, and sent to the Digital IF portion of the Signal Processor Assembly. The third IF is 36 kHz only when the radio's modem is active, and 30 kHz at all other times.

1.2 Transmit Signal Path

Refer to figure 1, a block diagram of the A5 Receiver/Exciter Assembly transmit path, during the following description.

The transmit frequency scheme is identical to the one used in receive, except that the third IF frequency is 6 kHz in transmit. The third IF is converted up to the second IF frequency of 9.5 MHz, amplified, and filtered to 8 kHz bandwidth before moving on to the transmit Second Converter. The Second Converter amplifies the signal and converts it up to the first IF frequency of 80.5 MHz.

The first IF is then amplified again, filtered to 22 kHz bandwidth, and converted up to a RF output frequency in the 1.6 to 60 MHz range. This output is then lowpass filtered to 60 MHz and amplified to 100 milliwatts. This signal is sent to the Power Amplifier Assembly (10303-2130) before actual transmission.

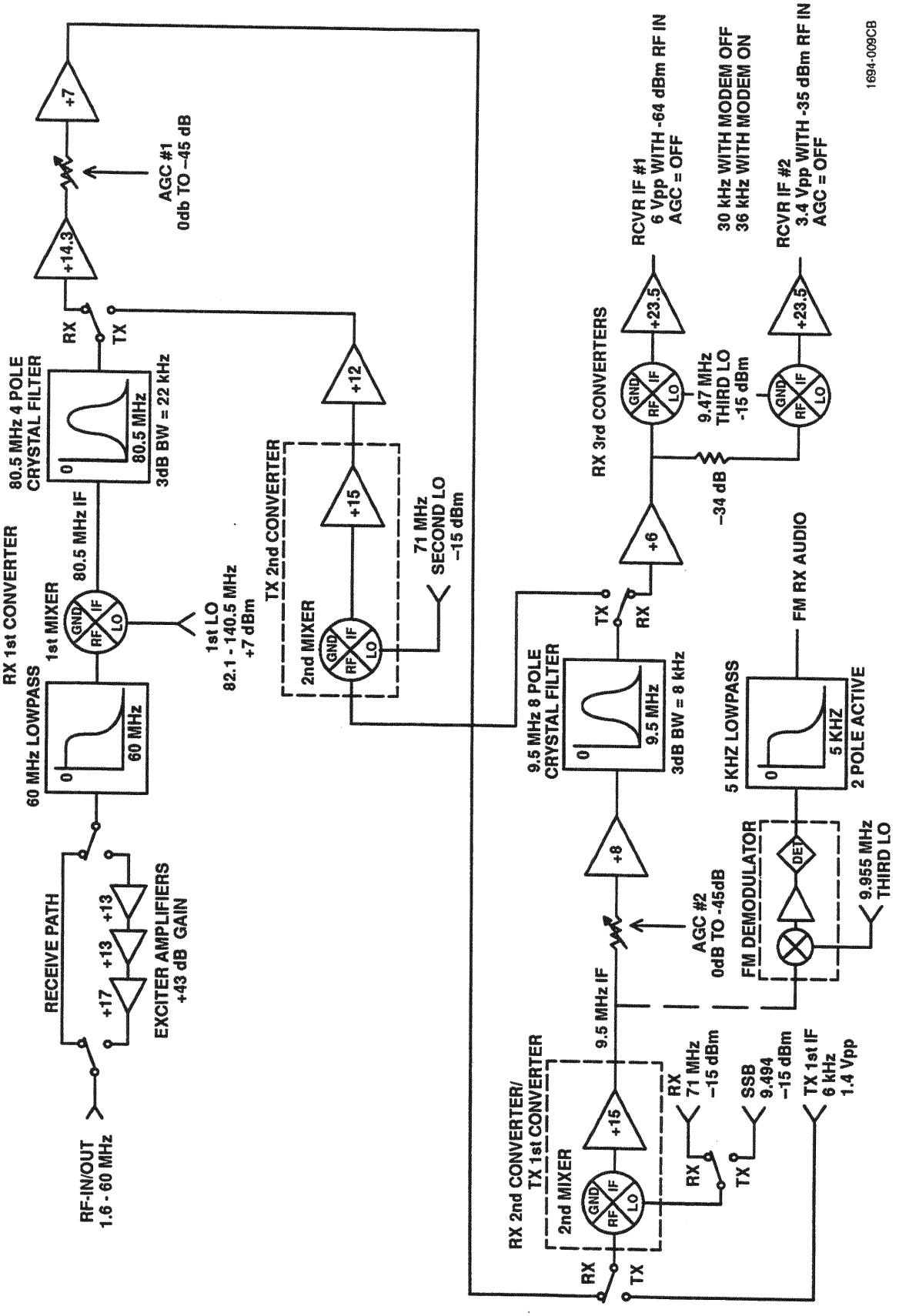


Figure 1. A5 Receiver/Exciter Assembly Block Diagram

2. INTERFACE CONNECTIONS

Table 1 shows the signals sent to and received by the First Converter Assembly. Table 2 shows the signals sent to and received by the Second and Third Converter Assembly.

Table 1. First Converter Interface Connections

Connector and Pin	Signal	Comments
P8	RF Input/Output	1.6 - 59.9999 MHz in/out Z = 50 ohms
J2	First local oscillator input	82.5 - 140.4999 MHz, +7 dBm, Zin = 50 ohms
P1-1	+12 Volts DC	Power input, 12.0 V ±8%
P1-2	+12 Volts DC	Power input, 12.0 V ±8%
P1-3	+5 Volts DC	Power input, 5.0 V ±2%
P1-4	-12 Volts DC	Power input, -12.0 V ±5%
P1-5	TX keyline	+5.0 V transmit, 0 V receive, Zin = 1.4 K ohms
P1-6	+5 Volts DC	Power input, 5.0 V ±2%
P1-7	Second LO input	71.0 MHz, 100 mVpp sine wave, Zin = 50 ohms
P1-8	/TX keyline	0 V transmit, +5 V receive, Zin = 10 K ohms, active low
P1-9	AGC control input	25 mV - 10 V produces 0 to 90 dB gain reduction
P1-10	6 kHz transmit IF input	2.8 Vpp in CW transmit mode, Zin = 13 K ohms
P1-11	Ground	
P1-12	FM RX audio output	0 - 5 kHz recover FM audio, 0.5 Vpp
P1-13	Ground	
P1-14	Third LO input	9.5 MHz - 9.6 MHz, 100 mVpp, Zin = 100 ohms
P1-15	Ground	
P1-16	Ground	
P1-17	Ground	
P1-18	Ground	
P1-19	80.5 MHz TX IF input	Low level, Zin = 5 K ohms
P1-20	9.5 MHz IF output	9.5 MHz IF, BW = 22 kHz, Zout = 2 K ohms

Table 2. Second and Third Converter Interface Connections

Connector and Pin	Signal	Comments
P5-1	RX IF #2	30/36 kHz low gain IF, BW = 8 kHz, Zout = 200
P5-2	TX keyline	+5 V - transmit, 0 V - receive, Zin = 1.4 K ohms
P5-3	RX IF #1	30/36 kHz high gain IF, BW = 8 kHz, Zout = 200
P5-4	FM RX audio output	0 - 5 kHz recovered FM audio, 0.5 Vpp
P5-5	/Aux 5 V enable input	0 V - U6 enabled, +5 V - U6 disabled, Zin = 82 K, active low
P5-6	RF attenuator control	0 V to -10 V produces 90 dB gain reduction
P5-7	Power supply ON (output)	+4.3 V = power supply ON, 0 V = power supply OFF
P5-8	6/7.2 kHz TX IF input	BW = 8 kHz, 2.8 Vpp in CW mode, Zin = 13 K ohms

Table 2. Second and Third Converter Interface Connections (Cont.)

Connector and Pin	Signal	Comments
P5-9	+24 V battery input	20 - 35 Vdc power input, Imax = 5 mA
P5-10	Ground	
P5-11	Main power supply trigger	Rising or falling edge causes P5-7 on for 200 mS
P5-12	Second LO input	71.0 MHz, 100 mVpp, Zin = 50 ohms
P5-13	-12 Vdc input	Power input, -12.0 V ± 5%, I_{typ} = 6 ma
P5-14	/TX keyline	0 V - transmit, +5 V - receive, Zin = 20 K ohms, active low
P5-15	+16.5 Vdc input	Power input, 16.5 V ± 10%, I_{typ} = 50/175 ma RX/TX
P5-16	24 V battery return	Power return
P5-17	+3.9 V memory backup out	+3.9 V ± 10%, Zout = 400 ohms, Imax = 1 mA
P5-18	+ 5 Vdc input	Power input, 5.0 V ± 25, I_{typ} = 60/125 ma RX/TX
P5-19	Third LO input	9.5 MHz, 100 mVpp, Zin = 100 ohms
P5-20	Ground	
J1-1	+12 Vdc	Power output, 12.0 V ± 8%
J1-2	+12 Vdc	Power output, 12.0 V ± 8%
J1-3	+5 Vdc	Power output, 5.0 V ± 2%
J1-4	-12 Vdc	Power output, -12.0 V ± 5%
J1-5	TX keyline	+5 V TX, 0 V RX
J1-6	+5 Vdc	Power output, 5.0 V ± 2%
J1-7	Second LO output	71.0 MHz, 100 mVpp sine wave
J1-8	/TX keyline	0 V TX, +5 V RX, active low
J1-9	AGC control output	25 mV - 10 V produces 0 to 90 dB gain reduction
J1-10	6 kHz TX IF output	2.8 Vpp in CW TX mode
J1-11	Ground	
J1-12	FM RX audio input	0 - 5 kHz recovered FM audio, 0.5 Vpp
J1-13	Ground	
J1-14	Third LO output	9.5 MHz - 9.6 MHz, 100 mVpp
J1-15	Ground	
J1-16	Ground	
J1-17	Ground	
J1-18	Ground	
J1-19	80.5 MHz TX IF output	Low level, Zout = 180 ohms
J1-20	9.5 MHz IF input	9.5 MHz IF > 10 K ohms

3. TECHNICAL DESCRIPTION

3.1 Receive Mode

3.1.1 First Converter Assembly

The First Converter Assembly provides the first level of RF signal processing in the receiver/exciter chain. Figure 2 is a block diagram of the First Converter Assembly. A parts list, component location diagram, and schematic diagram for the First Converter Assembly are provided at the end of this section. Refer to these diagrams during the following descriptions.

3.1.1.1 60 MHz 7th-Order Lowpass Filter

The lowpass filter is designed to pass signals in the 1.6 to 60 MHz input range with a maximum insertion loss of 0.3 dB. It is intended to provide at least 40 dB of attenuation to signals in the image frequency band of 162.6 to 221 MHz. The first null of the filter is placed at 80.5 MHz to assist in achieving the 80 dB IF Rejection spec for the receiver. Additional IF rejection filtering is provided in the Power Amplifier Assembly. A plot of attenuation vs. frequency for the input lowpass filter is shown in figure 3.

3.1.1.2 Double-Balanced Diode Ring Mixer

RF input signals from 1.6 to 60 MHz are applied at the input of mixer U4. A high level local oscillator in the 82.1 to 140.5 MHz range is used to drive the mixer LO port at +7 dBm. The frequency of the LO drive is used to select the desired receive frequency from the RF input band and convert the signal to an 80.5 MHz first IF. This IF signal is attenuated by the conversion loss of the mixer (usually 5 dB).

3.1.1.3 80.5 MHz 4-Pole Crystal Filter

The 80.5 MHz IF signal generated by U4 is filtered by four-pole crystal filter FL1. This filter has a -3 dB bandwidth of f_c+/-11 kHz, a -60 dB bandwidth of f_c+/-85 kHz, 5.0 dB maximum insertion loss, and less than 1 dB passband ripple over f_c+/-8 kHz. Input impedance matching at the 80.5 MHz IF frequency is provided internal to the filter to provide a match to the normally 50 ohm output impedance of mixer U4. External components R66, C73, C74, and L19 are transparent to the IF, but provide a 50 ohm termination at all other frequencies. The filter's output impedance is 300 ohms and is matched to the 75 ohm input of amplifier Q10 by C68 and T2.

3.1.1.4 Low-Noise Receive Amplifier with AGC

Transistor Q10 is a grounded-gate, low-noise, FET amplifier which has a gain of +14.3 dB and a 75 ohm input impedance. The output of the amplifier is resonated with L9 and C31 at 80.5 MHz. The output impedance of the amplifier is varied by changing the DC current through attenuator diode CR3. This varies the voltage gain of the amplifier over a 45 dB range and allows the automatic gain control (AGC) to control the receiver gain. The amplifier is biased by constant-current sink Q11 which holds the amplifier bias current to about 8 mA.

3.1.1.5 Second Converter with AGC

The 80.5 MHz RX IF passes through a cascode amplifier formed by transistors Q12 and Q13 before reaching the second mixer. This stage has a gain of +7 dB.

The second conversion process is accomplished by analog mixer U5. The 80.5 MHz input is mixed with a 71 MHz local oscillator to produce a 9.5 MHz second IF. This mixer IC incorporates an amplifier and has a conversion gain of +15 dB.

Varying the DC current through attenuator diode CR7 varies the input impedance of the second IF amplifier which controls overall receiver gain. This allows another AGC control and can provide up to 45 dB of attenuation.

The 9.5 MHz second IF is then passed on to the Second and Third Converter Assembly. Notice the inaccuracy of the assembly names. The Second Converter is actually located on the First Converter Assembly.

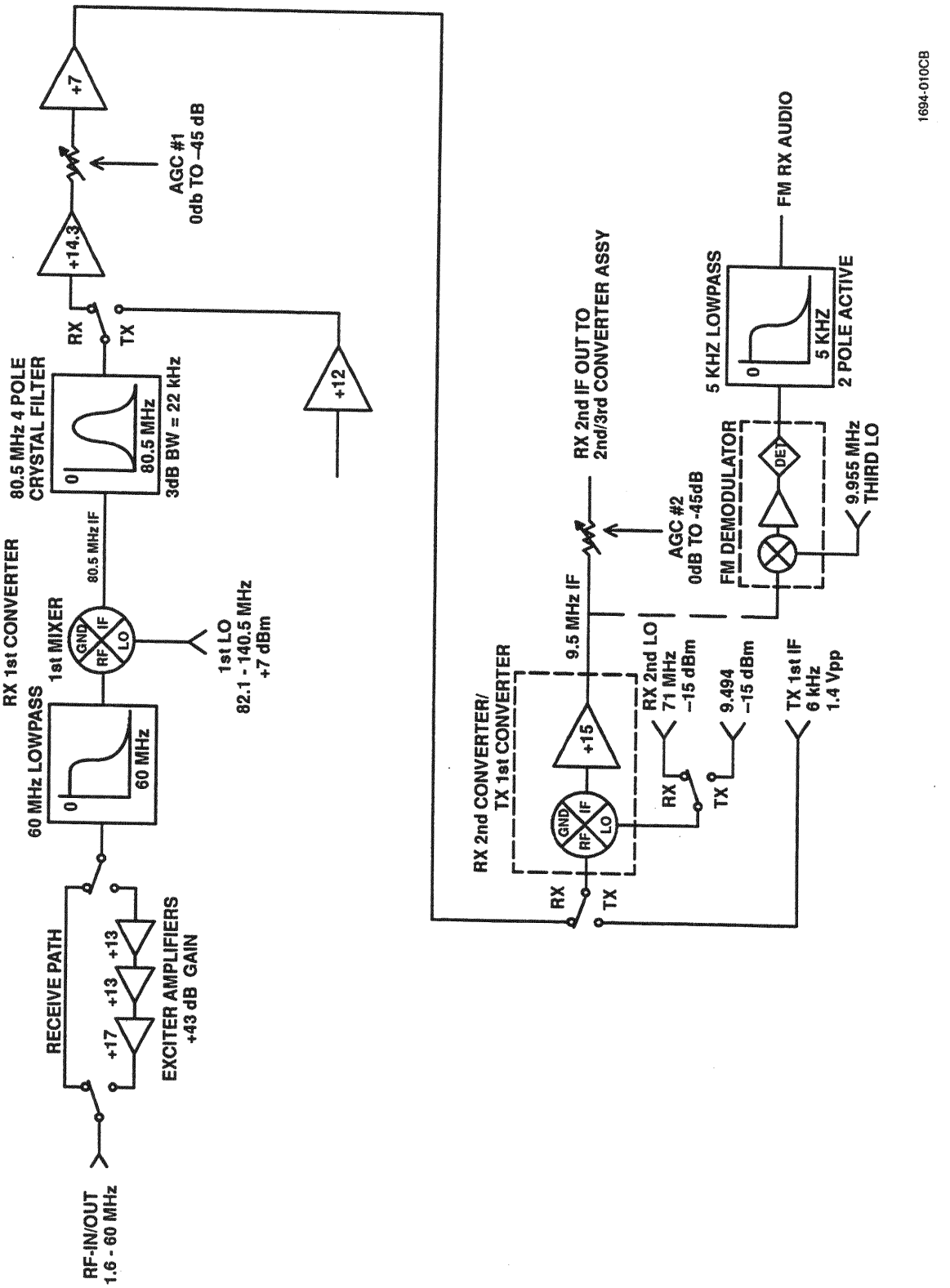


Figure 2. First Converter Assembly Block Diagram

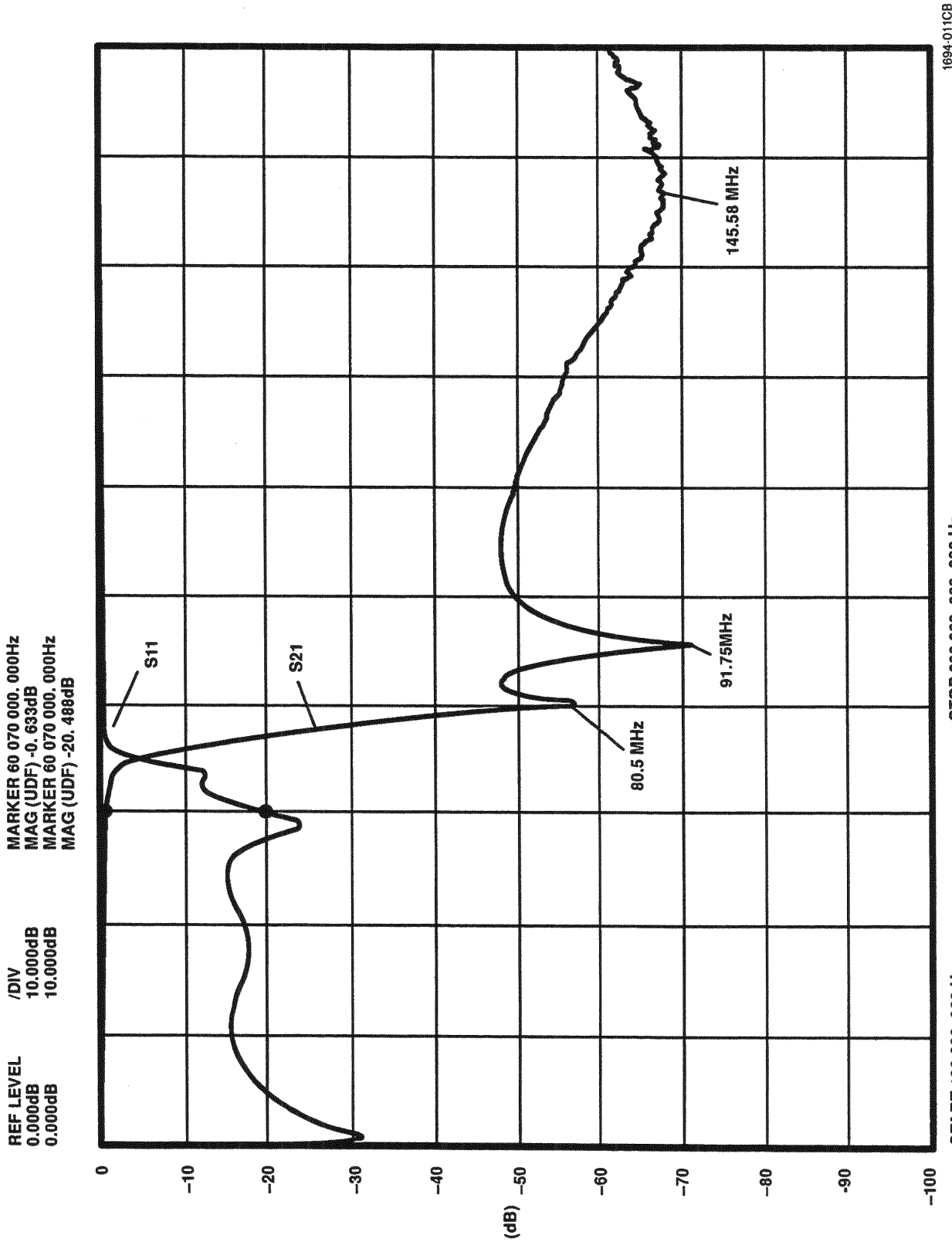


Figure 3. 60-MHz Low Pass Filter Response

3.1.2 Second and Third Converter Assembly

The Second and Third Converter Assembly interfaces the 9.5 MHz second IF signal produced by the First Converter Assembly with the Digital IF Assembly. Figure 4 is a block diagram of the Second and Third Converter Assembly.

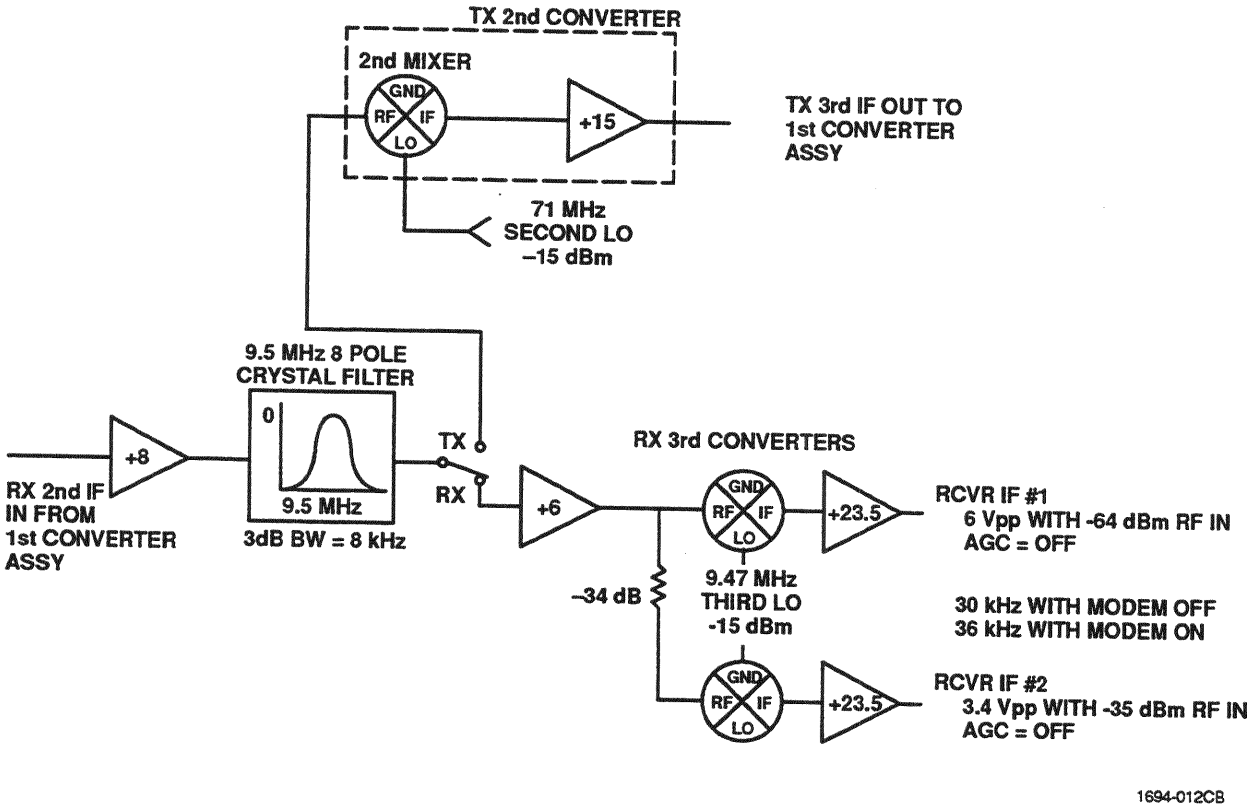


Figure 4. Second and Third Converter Assembly Block Diagram

3.1.2.1 Second IF Amplifier with AGC

The 9.5 MHz second IF is amplified by a cascode amplifier formed by transistors Q1 and Q2. This amplifier has an 8 dB power gain and a 2 K ohm output impedance. As mentioned above, AGC capability is provided by attenuator diode CR7 on the 10303-2270 assembly.

3.1.2.2 9.5 MHz Crystal Filter

The 9.5 MHz output signal of Q2 passes through 8-pole crystal filter FL1. This filter has a -3 dB bandwidth of f_c+/-4 kHz, a -60 dB bandwidth of f_c+/-9.5 kHz, 3.5 dB maximum insertion loss, and less than 0.5 dB passband ripple over f_c+/-3 kHz. The filter's 2 kOhm output is matched by L2 and C6.

The 9.5 MHz signal at the output of FL1 is amplified by emitter follower Q3 which drives IF amplifier Q4 and transmit mixer U1. This stage provides +6 dB of gain. IF amplifier Q9 splits the IF signal into two paths, generating the high-gain balanced drive required by third mixer U2 and the attenuated drive for mixer U3. The 34 dB of attenuation for the drive to mixer U3 is accomplished by resistors R16-R19.

3.1.2.3 Third Receive IF Mixers

Mixers U2 and U3 independently transform the two 9.5 MHz IF signals to a third IF frequency of 30 kHz or 36 kHz. The local oscillator is set to 9.47 MHz for a 30 kHz output or to 9.464 MHz to produce a 36 kHz output. The outputs of mixers U2 and U3 are buffered by the transistors in U9 before driving op amp sections U4A and U4B. Receive IF1 and IF2 are then fed to the digital IF section of the Signal Processor Assembly (10303-2500).

3.2 Transmit Mode

3.2.1 First Converter Assembly

The 6 kHz transmit IF created by the Signal Processor Assembly is routed to the First Converter Assembly for the first up-conversion by mixer U5. Resistive divider R41-R42 determines the drive level to the mixer. This 6 kHz IF is mixed with the 9.494 MHz third LO to produce a 9.5 MHz second IF. Notice that the same components (mixer, etc.) make up the Second Converter in receive mode. Similarly to receive mode, the second IF is amplified within the mixer and is subject to TGC control by attenuator diode CR7. The 9.5 MHz second IF is then passed on to the Second and Third Converter Assembly.

3.2.2 Second and Third Converter Assembly

3.2.2.1 Second IF Amplifier and Crystal Filter

The next few steps in the transmit path are exactly the same as in the receive path. The 9.5 MHz second IF is amplified by the cascode amplifier formed by Q1 and Q2, with TGC provided by attenuator diode CR7 on the First Converter Assembly. Crystal Filter FL1 filters the IF signal to an 8 kHz bandwidth.

3.2.2.2 Transmit Second Converter

The output of emitter follower Q3 is routed to the transmit second converter U1. The 9.5 MHz input is mixed with the 71 MHz second LO to produce an 80.5 MHz third IF. This third IF signal is resonated with L3 and C9 on this assembly and C72 on the First Converter Assembly.

3.2.3 Third IF Signal (First Converter Assembly)

The third IF signal is fed back to the First Converter Assembly for the conversion down to its RF transmission frequency.

3.2.3.1 Transmit IF Amplifier

The 80.5 MHz third IF is fed to a cascode amplifier formed by transistors Q6 and Q7. This amplifier stage has a 22 K ohm input impedance, 300 ohm output impedance, and 12 dB of gain. Transistor Q8 serves either as a bias current sink in transmit or to turn the bias off in receive. In transmit, the amplifier bias current is about 13 mA.

3.2.3.2 Crystal Filter and Front-End Mixer

This part of the transmit path is the receive path in reverse. The third IF signal is filtered to 22 kHz bandwidth by crystal filter FL1. U4 then mixes the 80.5 MHz IF with a +7 dBm LO in the 82.1 to 140.5 MHz range. The difference frequency then is placed within the 1.6 to 60 MHz output range.

3.2.3.3 60 MHz Lowpass Filter

The output of mixer U4 consists of our desired output frequency along with other parasitic frequencies such as harmonics, intermodulation products, and mixer sum frequencies (also known as image frequencies from 162.6 to 221 MHz). This output, then, must be lowpass filtered to allow only our 1.6 to 60 MHz RF frequencies to pass. This is the same filter whose response is shown in figure 3.

3.2.3.4 Exciter Amplifiers

The exciter's RF output must be amplified to the correct level before leaving the A5 Receiver/Exciter Assembly for transmission. The radio's Power Amplifier Assembly requires 100 mW of exciter drive to produce the 20 Watt radio output. To produce this 100 mW the First Converter Assembly incorporates three amplifiers, U3, U1, and Q5, with a 43 dB cascaded gain. They should require approximately -23 dBm drive to reach the exciter output level of 100 mW. U1 and U3 are class A, broadband, integrated-circuit amplifiers. They both have 50 ohm input and output impedances and approximately +13 dB of power gain. These are followed by a discrete, broadband,

class A, feedback amplifier consisting of Q5, U2, and T1. This amplifier has 50 ohm input impedance, 200 ohm output Impedance, and +17 dB of power gain. The output impedance of the amplifier stage is reduced to 50 ohms by transformer T1. Op amp U2 holds the DC emitter voltage of Q5 to 900 mV when in transmit. In receive, the whole amplifier chain is bypassed, so transistor Q4 biases U1 and U3 off to reduce power consumption.

3.3 RX/TX Switching

All RX/EX switching is controlled by the two lines called TX Keyline (+5 V TX, 0 V RX) and /TX Keyline (0 V TX, +5 V RX).

3.3.1 First Converter Assembly

As mentioned above, the exciter amplifier chain is bypassed in receive mode. Relays K1 and K2, in their "normally closed" or de-energized state, present a short from exciter input P8 to the input lowpass filter. In transmit, transistors Q1 and Q2 energize the relays and switch in the exciter amplifiers. The DC bias to amplifiers U1 and U3 gets switched on in transmit by transistors Q3 and Q4.

At the first IF stage, RX/TX switching is done by transistors Q8 and Q9. In receive, the DC bias to TX amplifier Q6-Q7 is turned off and the attenuator control to the low-noise amplifier is allowed to operate normally. In transmit, the TX amplifier is biased to 13 mA and the AGC attenuator becomes fully biased to disable the RX amplifiers and attenuate all signals on the RX path.

Mixer U5 is incorporated as both a second converter in receive and a first converter in transmit. Transistors Q14, Q15, and Q16, along with diodes CR4, CR5, and CR6 control whether the 71 MHz second LO or 9.47 MHz third LO is used to drive the mixer.

3.3.2 Second and Third Converter Assembly

The +5 V TX line is used to bias diode CR1 and thereby activate or deactivate the TX second converter U1.

4. TESTING AND ALIGNMENT

The A5 Receiver/Exciter Assembly (10303-2600) is made up of two separate subassemblies:

- First Converter Assembly (10303-2270)
- Second and Third Converter Assembly (10303-2610)

The following paragraphs cover test and alignment of these assemblies:

Table 3 is a list of test equipment required to test and align the A5 Receiver/Exciter Assembly In addition to this required test equipment, refer to the General Information section of this manual for recommended tools, equipment, and procedures necessary to access and test the A5 Receiver/Exciter Assembly.

The testing and alignment procedures outlined below assume that the following preliminary steps have been performed:

- The outside case of the radio has been removed.
- The chassis cover has been removed allowing access to the individual modules.
- The A5 Receiver/Exciter Assembly has been installed on an extender card with the First Converter Assembly (10303-2270) facing upward and the LO input from the synthesizer connected.
- The RF shield over the First Converter Assembly (10303-2270) has been unsoldered and removed.

The extender card should be included in an MRK kit and is necessary for any test or adjustment of the A5 Receiver/Exciter Assembly.

NOTE

In order to ensure accuracy in the test and alignment procedures, perform each procedure in the order in which it is listed in the following paragraphs.

The transceiver should be connected to a remote terminal and configured as follows:

- MODE USB
- RX FREQ 3.1 MHz
- TX FREQ 3.1 MHz
- AGC OFF
- RF GAIN 100
- PREAMP BYPASSED
- INTCOUP BYPASSED

Table 3. Required Test Equipment

Test Equipment	Model/Manufacturer
Digital Multimeter	Fluke 8012 or equivalent
Oscilloscope	Tektronix 475. or equivalent
RF Signal Generators (2)	HP-8657A or equivalent HP-8640B or equivalent
RF Millivoltmeter	Boonton 9200B or equivalent
Spectrum Analyzer	Marconi 2380/2382 or equivalent
Audio Analyzer	HP-8903B or equivalent
Function Generator	EXACT 507 or equivalent
DC Voltage Supply	

4.1 Power Supply Checks

Using a DVM, verify at P5 of the Second and Third Converter Assembly (10303-2610):

- P5-17 +3.9 VDC ±10% (3.51 to 4.29)

Using a DVM, also verify at P1 of the First Converter Assembly (10303-2270):

- P1-1 +12 VDC ±8% (11.04 to 12.96)
- P1-2 +12 VDC ±8% (11.04 to 12.96)
- P1-4 -12 VDC ±5% (-12.6 to -11.4)
- P1-3 +5 VDC ±2% (4.9 to 5.1)
- P1-6 +5 VDC ±2% (4.9 to 5.1)

4.2 PIN Attenuator

Perform the following procedure to set the PIN attenuator:

a. Verify 0.018 VDC ± 0.001 (0.017 to 0.019) at TP-1 of the First Converter Assembly (10303-2270). R33 on the Second and Third Converter Assembly (10303-2610) will adjust this.

b. This measurement assumes that AGC is OFF and RF GAIN is 100.

4.3 Initial Receiver Alignment

Perform the following procedure to align the receiver:

a. With the RX frequency at 3.1 MHz, connect an external RF Signal Generator to the RF input coax P8 of the First Converter Assembly (10303-2270) and inject a 3.101 MHz signal at -64 dBm.

b. With an oscilloscope, monitor the output of P5 pin 3 of the Second and Third Converter Assembly (10303-2610).

c. Adjust capacitors C31, C66, and C46 on the First Converter Assembly (10303-2270) for maximum peak to peak amplitude. Also, peak C74 on revision F PWBs and later.

d. Insure that each capacitor can peak the signal at two different adjustment positions.

4.4 First Converter Crystal Filter Check

Perform the following procedure to align the First Converter crystal filter:

a. With the same setup as above, change the MODE Control on the front panel of the RT-1694 Transceiver back to USB.

b. Increase the RF input level to -45 dBm.

c. Set the function generator to produce a 5 Hz triangle wave that drives the external FM modulation input to the signal generator and the X input (horizontal) of the scope.

d. On the RF signal generator press [SHIFT] [FM] and set FM deviation for 40 kHz.

e. Set the level of the function generator so that both the HIGH EXT and LO EXT lights on the signal generator are extinguished.

f. Place the oscilloscope in the X-Y mode.

g. Set the horizontal gain of the scope so the trace sweeps across the entire face of the display.

h. Probe U6 pin 16 on the First Converter Assembly (10303-2270) with CH2 of the oscilloscope.

i. Verify that the First Converter Crystal Filter FL1 has a flat passband response between Fc ± 11 kHz (-3 dB skirts).

4.5 Second Converter Crystal Filter Check

Perform the following procedure to align the Second Converter crystal filter:

a. Decrease the RF input level to -64 dBm and probe P5-3 of the Second and Third Converter Assembly (10303-2610).

b. On the RF signal generator press [SHIFT] [FM] and set FM deviation for 10 kHz.

c. Verify a flat passband response between ± 4 kHz.

4.6 Receiver Gain Adjustment & IF #2 Check

Perform the following procedure to adjust receiver gain and check receiver IF #2:

a. Insure that the RF generator's MODULATION is OFF and that the oscilloscope is set up to monitor CH2.

b. Adjust R4 on the Second and Third Converter Assembly (10303-2610) for 6.0 ± 0.35 V P-P at P5-3 of 10303-2610 as measured on the oscilloscope.

c. Increase the RF input level to -35 dBm.

d. RCVR IF #2 should measure 3.60 ±0.60 V P-P at P5 pin 1 on the Second and Third Converter Assembly (10303-2610).

4.7 Receiver Input Lowpass Filter Adjustment

Perform the following procedure to adjust the receiver input lowpass filter:

a. Disconnect the radio's first LO from J2 of the First Converter Assembly (10303-2270) and connect an external signal generator (HP-8640 or equivalent).

b. Monitor P5-3 of the 10303-2310 Assembly with an oscilloscope. Perform the following adjustments:

RF Input Frequency	LO Frequency	Adjustment on First Converter Assy*
80.500 MHz	161.000 MHz	L2
91.750 MHz	172.250 MHz	L3
145.580 MHz	226.080 MHz	L1
80.500 MHz	161.000 MHz	L2

*Adjust for minimum level on oscilloscope.

4.8 FM Demodulator Check

Perform the following procedure to check the FM demodulator:

a. Reconnect radio's first LO to J2 of the First Converter Assembly (10303-2270).

b. Set radio frequency to 20.850 MHz FM mode.

c. Set RF input signal to 20.850 MHz at -107 dBm.

d. Frequency modulate the RF input signal generator at 8 kHz deviation with a 1 kHz tone.

e. Connect an oscilloscope probe to the input high BNC connector and monitor P5-3 of the A5A1 Assembly (10303-2610). Press [FREQ.], [1], [KHz], and [SINAD].

f. Place the audio analyzer in the SLOW AVG DETECTOR mode by pressing [CLEAR], [5.3], and [SPCL],

g. Adjust C45 of the First Converter Assembly (10303-2270) for maximum SINAD. The output SINAD must be greater than 10 dB.

h. Increase the amplitude of the RF signal generator to -80 dBm,. Measure the P-P amplitude of the FM RX audio at P1-12 of the First Converter Assembly (10303-2270) with the oscilloscope. The recovered audio level should be 0.15 ± 0.05 VP-P (0.10 to 0.20).

i. Press DISTN on the audio analyzer. Measure and record the distortion of the 1 kHz signal measured by the audio analyzer. Verify that the distortion is less than 10%.

j. Remove the probe from the oscilloscope CH2 and place it on the INPUT HIGH BNC of the audio analyzer. Continue to monitor P1-12. Select ac measurement (dB) on the audio analyzer and then set to a reference zero by pressing the ratio button. Increase the modulating tone frequency to 4 kHz, measure and record the dB difference (must be -3 dB or greater).

k. Increase the modulating tone frequency to 10 kHz, measure and record the dB difference (must be -9 dB or less). Return FM modulation frequency to 1 kHz.

l. Disconnect the probe from the audio analyzer and reconnect it to CH2 of the oscilloscope. Disable the RF output from the RF generator and verify that the P-P noise amplitude equals the 1 kHz signal amplitude (± 50 mv).

4.9 Receiver Sensitivity Check

Perform the following procedure to check receiver sensitivity:

a. Change radio MODE control to USB at the RF Input Frequencies listed in step b. Connect the signal generator to the RF input connector on the radio, and connect the audio analyzer to the radio Audio output.

b. RF input at -110 dBm at the frequencies listed below plus 1 kHz (i.e., 2.05 MHz + 1 kHz = 2.051 MHz):

RF Input Frequency	First LO Frequency (Reference Only)
2.05 MHz	82.550 MHz
5.10 MHz	85.600 MHz
10.10 MHz	90.600 MHz
15.10 MHz	95.600 MHz
20.10 MHz	100.600 MHz
25.10 MHz	105.600 MHz
30.10 MHz	110.600 MHz
40.10 MHz	120.600 MHz
46.10 MHz	126.600 MHz
59.70 MHz	140.200 MHz

c. With the radio's first LO connected to J2 of the First Converter Assembly (10303-2270), set radio RX frequency to the same as that listed as RF input frequency in step a.

d. Measure signal plus noise to noise ratio of radio's audio output with the audio analyzer. The resultant Signal+Noise/Noise should be ≥ 10 dB at each frequency.

4.10 Attenuator Linearity Check

Perform the following procedure to check the attenuator linearity:

a. Return signal generator frequency to 3.1 MHz at -38 dBm.

b. Monitor P5-3 with oscilloscope.

c. Connect external dc supply set at 0 volts output to P5-6 of Second and Third Converter Assembly (10303-2610) in such a manner as to provide negative voltage to the pin

d. Very slowly increase the negative voltage until 6 Vpp appears on the scope.

e. Verify that the dc voltage is -2.99 ± 0.33 Vdc (-2.66 to -3.32 volts).

4.11 Transmitter Carrier Null Adjustment

Perform the following procedure to adjust the transmitter carrier null:

a. Connect a signal generator into the First LO connector J2 [First Converter Assembly (10303-2270)].

b. Set the generator to 83.6 MHz @ +7 dBm.

c. Have the dc supply on P5-6 of Second and Third Converter Assembly (10303-2610) set at 0 volts.

d. Connect RF connector P8 [First Converter Assembly (10303-2270)] to 50 ohm input of RF millivoltmeter.

e. Key transmitter and adjust negative dc supply until the RF output measures +17 dBm.

f. Adjust C72 [First Converter Assembly (10303-2270)] for maximum transmitter output.

g. Verify that the trimmer can peak the output at two different positions.

h. Readjust the negative dc supply for +20 dBm RF output.

i. Set up the spectrum analyzer as follows:

- SPAN 2 kHz/Div
- Center Frequency 3.1 MHz
- Reference Level +22 dBm

j. Disconnect the RF voltmeter from P8 and connect P8 to the spectrum analyzer.

k. Adjust R44 on the First Converter Assembly (10303-2270) to dip the signal that is 6 kHz above the desired signal at 3.10 MHz. (The undesired output, 6 kHz above 3.1 MHz, should be a minimum of 50 dB below the desired carrier).

4.12 Exciter Spurious Output Check

Perform the following procedure to check the exciter spurious output:

a. Leaving the setup and adjustments the same as from subsection 4.11, set up the spectrum analyzer as follows:

- FULL SPAN
- Center Frequency 3.1 MHz
- Reference Level +22 dBm

b. Connect the unit under test's First LO (J2) to the radio's First LO connector.

c. Verify that no spurious signals (> -50 dBc) above 100 MHz are present that are attributable to the UUT.

4.13 Exciter Output Level Check

Perform the following procedure to check the exciter output level:

a. Connect P8 (First Converter Assembly [10303-2270]) RF output to the 50 ohm input of the RF millivoltmeter.

b. With the radio's First LO connected to J2 (First Converter Assembly [10303-2270]), set the TX FREQ for each one listed below: (CW MODE)

RF Output Frequency	First LO Frequency (Reference Only)
2.05 MHz	82.550 MHz
5.10 MHz	85.600 MHz
10.10 MHz	90.600 MHz
15.10 MHz	95.600 MHz
20.10 MHz	100.600 MHz
25.10 MHz	105.600 MHz
30.10 MHz	110.600 MHz
40.10 MHz	120.600 MHz
50.10 MHz	130.600 MHz
59.80 MHz	140.300 MHz

c. Adjust the negative dc voltage on P5 pin 6 (Second and Third Converter Assembly [10303-2610]) so that the exciter outputs +20 dBm when keyed at each of the above transmit frequencies. The dc voltage required for + 20 dBm output should be –2.80 to –4.80 Vdc.

4.14 End of Test

Perform the following:

a. Make sure the toroids L1 – L3 are cemented in place.

b. Remove the test equipment from the module and the radio.

c. Remove the extender card.

d. Replace the RF shield over the First Converter Assembly (10303-2270).

e. Solder in place.

f. Reassemble the radio.

5. BITE FAULTS AND TROUBLESHOOTING

The self-test fault codes for the A5 Receiver/Exciter Assembly are shown in table 4. The faults are described in greater detail in the paragraphs that follow.

Table 4. A5 Receiver/Exciter Assembly Fault Codes

Code	Fault
01	Receiver in band analog attenuation too low
02	Receiver in band digital attenuation too low
03	Receiver out of band analog attenuation too high
04	Receiver out of band digital attenuation too high
0F	Exciter gain too low
10	Exciter gain too high
11	Exciter output too low
12	Exciter output too high

5.1 Receiver Faults 01 through 04

Receiver BITE faults are determined by the digital and analog AGC control outputs. When the test is run from a remote terminal, the terminal display shows the following:

S: Axx Dxx <-- Out of Band

S: Axx Dxx <-- In Band

where A and D are the analog and digital controller values, respectively.

Fault		Fault Value
01	In band analog attenuation low	<05 H
02	In band digital attenuation low	>30 H
03	Out of band analog attenuation high	<>00 H
04	Out of band digital attenuation high	<60 H (usually 82 H)

5.2 Exciter Faults 0F through 12

Exciter Gain faults are determined by the ATTEN CTRL line value measured by the software. Exciter Output faults are determined by the level detectors placed on the Power Amplifier Assembly, after the A5 Receiver/Exciter Assembly output. I. When the test is run from a remote terminal, the terminal display shows the following:

O:xx G:xxxx

where O and G are the output and gain, respectively.

Fault	Displayed Value	Corr. Value	Problem:
0F EX gain low	<3851 H	–2.2 V	Less attenuation
10 EX gain high	>91E2 H	–5.7 V	More attenuation
11 EX output low	<77 H	2.35 V	
12 EX output high	>F0 H	4.70 V	

Exciter output fault values correspond to –3 dB and +3 dB from the full power output reading of 3.32 V after AGC attenuation.

6. PARTS LISTS, COMPONENT LOCATION DIAGRAMS, AND SCHEMATIC DIAGRAMS

Table 5 is the parts list for the A5 Receiver/Exciter Assembly. The parts lists, component location diagrams, and schematics for the individual circuit assemblies that comprise A5 follow.

Table 6 is the parts list, and figure 5 is the component location diagram, for the A5A1 Second and Third Converter Assembly. Figure 7 is the schematic diagram for all revisions of the A5A1 Second and Third Converter Assembly.

Table 8 is the parts list and figure 8 is the component location diagram for the A5A2 First Converter Assembly. Figure 9 is the schematic for all revisions of the First Converter.

Table 5. A5 Receiver/Exciter Assembly Parts List (10303-2600 Rev. G)

Ref. Desig.	Part Number	Description
—	10303-1054	INSULATOR
—	10303-1107	COVER
16	10303-1122-01	INSULATOR
17	10303-1036	INSULATOR, PS BOARDS
18	10303-1124	INSULATOR
20	10372-1115-01	SHIELD ASSEMBLY
A1	10303-2610	PWB ASSY,RCVR-EXCTR/2ND,3
A2	10303-2270	PWB ASSY,RCVR-EXCTR 1ST C

Table 6. A5A1 Second & Third Converter Assembly Parts List (10303-2610 Rev. F)

Ref. Desig.	Part Number	Description
—	E70-0002-005	PAD MNT XSTR TO-18
—	E70-0002-004	PAD MNT XSTR TO-5
—	10303-1055	CONTACT,SPRING FINGER
—	10372-1524-04	CORD
C1	C13-0103-103	CAP .01UF 10% 100V SMD
C2	C13-0103-103	CAP .01UF 10% 100V SMD
C3	C13-0103-103	CAP .01UF 10% 100V SMD
C4	C13-0103-103	CAP .01UF 10% 100V SMD
C5	C85-0009-001	CAP VAR 2.5-10PF CER
C6	C85-0009-001	CAP VAR 2.5-10PF CER
C7	C13-0103-103	CAP .01UF 10% 100V SMD
C8	C13-0103-103	CAP .01UF 10% 100V SMD
C9	C13-0105-689	CAP 6.8PF +-.5PF 100V SMD
C10	C13-0103-103	CAP .01UF 10% 100V SMD
C11	C13-0103-103	CAP .01UF 10% 100V SMD
C12	C13-0103-103	CAP .01UF 10% 100V SMD
C13	C13-0103-103	CAP .01UF 10% 100V SMD
C14	C13-0103-103	CAP .01UF 10% 100V SMD
C15	C13-0103-103	CAP .01UF 10% 100V SMD
C16	C13-0103-103	CAP .01UF 10% 100V SMD
C17	C13-0103-103	CAP .01UF 10% 100V SMD
C18	C13-0103-103	CAP .01UF 10% 100V SMD
C19	C13-0103-473	CAP .047UF 10% 100V SMD
C20	C13-0103-473	CAP .047UF 10% 100V SMD
C21	C13-0103-473	CAP .047UF 10% 100V SMD
C22	C13-0103-103	CAP .01UF 10% 100V SMD
C23	C13-0103-103	CAP .01UF 10% 100V SMD
C24	C13-0105-680	CAP 68PF 10% 100V SMD

Table 6. A5A1 Second & Third Converter Assembly Parts List (10303-2610 Rev. F) (Cont.)

Ref. Desig.	Part Number	Description
C25	C13-0105-680	CAP 68PF 10% 100V SMD
C26	C13-0103-473	CAP .047UF 10% 100V SMD
C27	C13-0103-473	CAP .047UF 10% 100V SMD
C28	C13-0105-680	CAP 68PF 10% 100V SMD
C29	C13-0105-680	CAP 68PF 10% 100V SMD
C30	C13-0103-103	CAP .01UF 10% 100V SMD
C31	C13-0103-103	CAP .01UF 10% 100V SMD
C32	C13-0103-473	CAP .047UF 10% 100V SMD
C33	C13-0103-473	CAP .047UF 10% 100V SMD
C34	C13-0103-473	CAP .047UF 10% 100V SMD
C35	C13-0103-103	CAP .01UF 10% 100V SMD
C36	C13-0103-103	CAP .01UF 10% 100V SMD
C37	C13-0103-103	CAP .01UF 10% 100V SMD
C38	C13-0103-102	CAP 1000PF 10% 100V SMD
C39	C22-0020-105	CAP 1.0UF 10% 20V TANT
C40	C22-0020-105	CAP 1.0UF 10% 20V TANT
C41	C22-0010-106	CAP, 10UF 10V 10% TANT
C42	C13-0103-473	CAP .047UF 10% 100V SMD
C43	C13-0103-473	CAP .047UF 10% 100V SMD
C44	C22-0025-106	CAP, 10UF 25V 10% TANT
C45	C13-0103-473	CAP .047UF 10% 100V SMD
C46	C13-0103-473	CAP .047UF 10% 100V SMD
C47	C13-0103-473	CAP .047UF 10% 100V SMD
C48	C22-0025-106	CAP, 10UF 25V 10% TANT
C49	C13-0103-473	CAP .047UF 10% 100V SMD
C50	C13-0103-473	CAP .047UF 10% 100V SMD
C51	C13-0103-473	CAP .047UF 10% 100V SMD
C52	C22-0010-226	CAP 22UF 10% 10V TANT
C53	C13-0103-473	CAP .047UF 10% 100V SMD
C54	C13-0103-473	CAP .047UF 10% 100V SMD
C55	C13-0103-473	CAP .047UF 10% 100V SMD
C56	C22-0010-106	CAP, 10UF 10V 10% TANT
C57	C22-0010-106	CAP, 10UF 10V 10% TANT
C58	C13-0103-103	CAP .01UF 10% 100V SMD
C59	C13-0103-102	CAP 1000PF 10% 100V SMD
C60	C13-0103-473	CAP .047UF 10% 100V SMD
C62	C13-0103-103	CAP .01UF 10% 100V SMD
C63	C13-0105-829	CAP 8.2PF +-.5PF 100V SMD
C64	C13-0103-473	CAP .047UF 10% 100V SMD

Table 6. A5A1 Second & Third Converter Assembly Parts List (10303-2610 Rev. F) (Cont.)

Ref. Desig.	Part Number	Description
C65	C22-0050-225	CAP, 2.2UF 50V TANT
C67	C97-0004-473	CAP, 47000 UF 5.5V
CR1	1N4454	DIODE 200MA 75V SW
CR2	1N4454	DIODE 200MA 75V SW
CR3	1N4454	DIODE 200MA 75V SW
CR4	1N4454	DIODE 200MA 75V SW
CR5	1N4454	DIODE 200MA 75V SW
FL1	10303-3104	FILTER, 8 POLE XTAL 9.5 M
J1	J46-0115-020	CONN, 20 PIN MALE
JMP1	MP-1142	RES ZERO OHM (CKT JMPR)
L1	MS21426-27	COIL 15UH 10% FIXED RF
L2	MS21426-27	COIL 15UH 10% FIXED RF
L3	10303-3182	INDUCTOR, .056UH
L4	MS14046-4	COIL 10UH 10% FXD RF
L5	MS14046-4	COIL 10UH 10% FXD RF
L6	MS90538-12	COIL 100UH 5% FXD RF
L7	MS14046-4	COIL 10UH 10% FXD RF
L8	MS14046-4	COIL 10UH 10% FXD RF
L10	MS21426-9	COIL .47UH 10% FIXED RF
P5	J46-0117-020	CONN, 20 PIN MALE RT ANG
Q1	Q35-0003-000	XSTR N-CH JFET U310
Q2	2N5179	XSTR SS/RF NPN TO-72
Q3	2N5179	XSTR SS/RF NPN TO-72
Q4	2N2222A	XSTR SS/GP NPN TO-18
Q9	I90-0011-001	XSTR, DUAL MATCHED PR(LM1
Q10	2N2907A	XSTR SS/GP PNP TO-18
R1	R85-0125-104	RES 100K 5% 1/8W FILM
R2	R85-0125-104	RES 100K 5% 1/8W FILM
R3	R85-0004-177	RES 619 1% 1/8W FLM
R4	R30-0018-202	RES VARIABLE 2K
R5	R85-0125-101	RES 100 5% 1/8W FILM
R6	R85-0125-102	RES 1.0K 5% 1/8W FILM
R7	R85-0125-100	RES 10 5% 1/8W FILM
R8	R85-0004-230	RES 2.0K 1% 1/8W SMD
R9	R85-0125-100	RES 10 5% 1/8W FILM
R10	R85-0125-682	RES 6.8K 5% 1/8W FILM
R11	R85-0125-272	RES 2.7K 5% 1/8W FILM
R12	R85-0125-100	RES 10 5% 1/8W FILM
R13	R85-0125-471	RES 470 5% 1/8W FILM

Table 6. A5A1 Second & Third Converter Assembly Parts List (10303-2610 Rev. F) (Cont.)

Ref. Desig.	Part Number	Description
R15	R85-0004-158	RES 392 1% 1/8W FLM
R16	R85-0004-151	RES 332 1% 1/8W FLM
R17	R85-0004-081	RES 68.1 1% 1/8W FLM
R18	R85-0004-130	RES 200 1% 1/8W FLM
R19	R85-0004-145	RES 287 1% 1/8W SMD
R20	R85-0125-102	RES 1.0K 5% 1/8W FILM
R21	R85-0004-230	RES 2.0K 1% 1/8W SMD
R22	R85-0125-101	RES 100 5% 1/8W FILM
R23	R85-0125-101	RES 100 5% 1/8W FILM
R24	R85-0004-230	RES 2.0K 1% 1/8W SMD
R25	R85-0125-102	RES 1.0K 5% 1/8W FILM
R26	R85-0125-101	RES 100 5% 1/8W FILM
R27	R85-0125-153	RES 15K 5% 1/8W FILM
R28	R85-0004-410	RES 124K 1% 1/8W SMD
R29	R85-0125-102	RES 1.0K 5% 1/8W FILM
R30	R85-0004-210	RES 1.24K 1% 1/8W SMD
R31	R85-0125-102	RES 1.0K 5% 1/8W FILM
R32	R85-0125-104	RES 100K 5% 1/8W FILM
R33	R40-0016-503	RES VAR 50K OHM PCB
R34	R85-0004-326	RES,18.2K 1% 1/8W CHIP
R35	R85-0004-381	RES 68.1K 1% 1/8W FLM
R36	R85-0004-201	RES 1000 1% 1/8W FLM
R37	R85-0004-350	RES 32.4K 1% 1/8W SMD
R38	R85-0125-104	RES 100K 5% 1/8W FILM
R39	R85-0004-434	RES 221K 1% 1/8W SMD
R40	R85-0004-434	RES 221K 1% 1/8W SMD
R41	R85-0125-273	RES 27K 5% 1/8W FILM
R42	R85-0125-823	RES 82K 5% 1/8W FILM
R43	R85-0004-145	RES 287 1% 1/8W SMD
R45	R85-0004-177	RES 619 1% 1/8W FLM
R46	R85-0004-269	RES 5110 1% 1/8W FLM
R47	R85-0125-100	RES 10 5% 1/8W FILM
R48	R85-0125-100	RES 10 5% 1/8W FILM
R49	R85-0125-100	RES 10 5% 1/8W FILM
R50	R85-0125-100	RES 10 5% 1/8W FILM
R51	R85-0125-100	RES 10 5% 1/8W FILM
R52	R85-0125-100	RES 10 5% 1/8W FILM
R53	R85-0125-330	RES 33 5% 1/8W FILM
R54	R85-0125-101	RES 100 5% 1/8W FILM

Table 6. A5A1 Second & Third Converter Assembly Parts List (10303-2610 Rev. F) (Cont.)

Ref. Desig.	Part Number	Description
R55	R85-0125-103	RES 10K 5% 1/8W FILM
R56	R85-0125-101	RES 100 5% 1/8W FILM
R57	R85-0125-101	RES 100 5% 1/8W FILM
R58	R85-0125-101	RES 100 5% 1/8W FILM
R59	R85-0125-101	RES 100 5% 1/8W FILM
R60	R85-0004-151	RES 332 1% 1/8W FLM
R68	R85-0125-181	RES 180 5% 1/8W FILM
R70	R85-0004-366	RES 47.5K 1% 1/8W FLM
R71	R85-0004-230	RES 2.0K 1% 1/8W SMD
R72	R85-0004-366	RES 47.5K 1% 1/8W FLM
R73	R85-0004-366	RES 47.5K 1% 1/8W FLM
R74	R85-0004-366	RES 47.5K 1% 1/8W FLM
R75	R85-0004-230	RES 2.0K 1% 1/8W SMD
R77	R85-0125-100	RES 10 5% 1/8W FILM
R78	R85-0004-301	RES 10K 1% 1/8W FLM
R79	R85-0004-301	RES 10K 1% 1/8W FLM
R80	R85-0004-330	RES 20.0K 1% 1/8W FLM
R81	R85-0004-330	RES 20.0K 1% 1/8W FLM
RT1	D40-0004-003	THERM 1K 5% @ 25DEG
U1	I51-0007-001	IC MIXER ANALOG 12002
U2	I51-0007-001	IC MIXER ANALOG 12002
U3	I51-0007-001	IC MIXER ANALOG 12002
U4	I30-0048-002	IC, LP DUAL OP-AMP (MC331
U5	I30-0048-002	IC, LP DUAL OP-AMP (MC331
U6	I01-0000-353	IC 4538B PLASTIC CMOS
U7	I11-0020-001	VOLTAGE REG 5V (LM2936Z-5
U8	I11-0015-002	IC, VOLT REG,VAR (LM117H)
U9	I90-0012-001	IC,QUAD XSTR (MPQ2222A)
VR1	I14-0015-007	REG, PREC 2.5V (LM285BXZ-
VR2	1N4735A	DIODE 6.2V 5% 1W ZENER
Z1	L50-0001-004	FERRITE BEAD

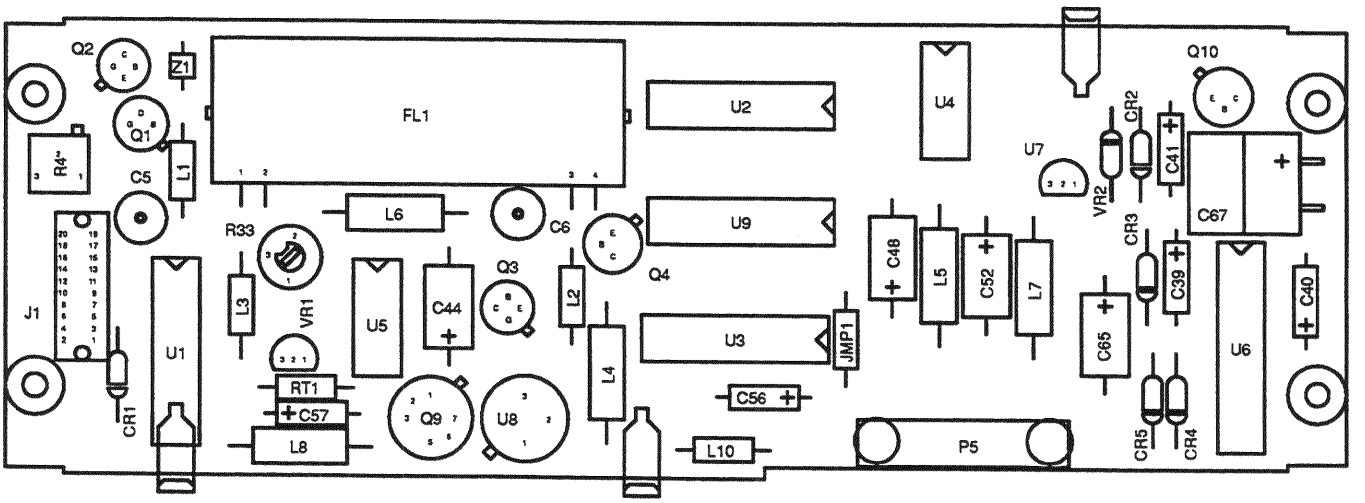


Figure 5. Second and Third Converter Assembly Component Location Diagram (10303-2610 Rev. B) (Sheet 1 of 2)

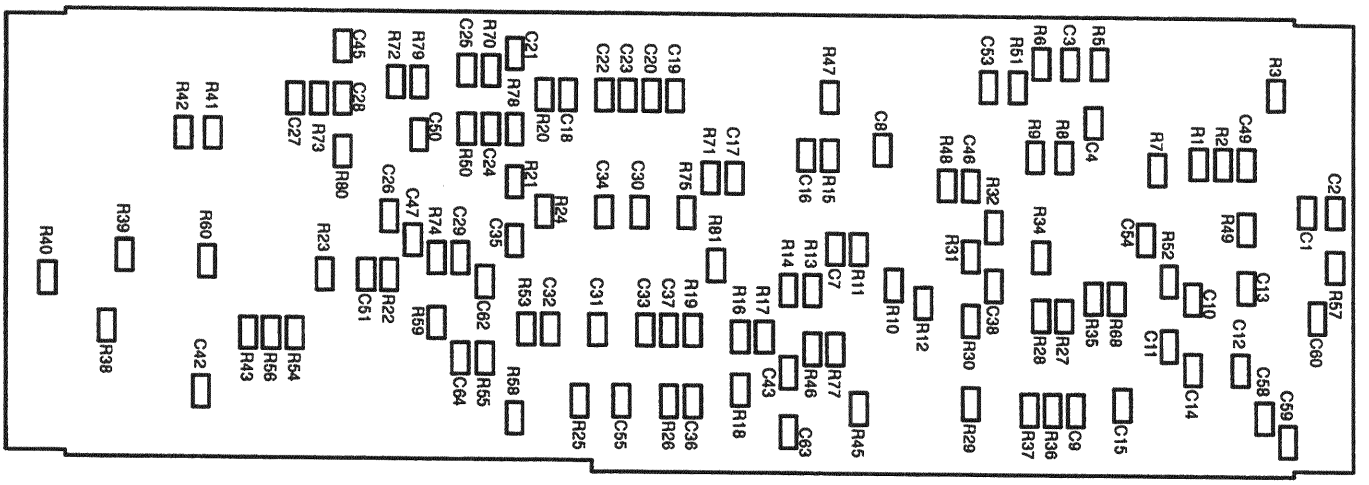


Figure 5. Second and Third Converter Assembly Component Location Diagram (10303-2610 Rev. B) (Sheet 2 of 2)

Table 7. A5A1 Second & Third Converter Assembly Parts List (10303-2610 Rev. B and Earlier)

Ref. Desig.	Part Number	Description
1	10303-1571	SCHEM, SECOND/THIRD CONVE
3	E70-0002-005	PAD MNT XSTR TO–18
4	E70-0002-004	PAD MNT XSTR TO–5
5	10303-1055	CONTACT, SPRING FINGER
6	10303-1045	STANDOFF, SWAGE
7	H70-0008-001	EYELET
10	10303-2619	PWB, SECOND/THIRD
C1	C13-0103-103	CAP .01UF 10% 100V SMD
C2	C13-0103-103	CAP .01UF 10% 100V SMD
C3	C13-0103-103	CAP .01UF 10% 100V SMD
C4	C13-0103-103	CAP .01UF 10% 100V SMD
C5	C85-0009-101	CAP VAR 2.5–10PF AIR
C6	C85-0009-101	CAP VAR 2.5–10PF AIR
C7	C13-0103-103	CAP .01UF 10% 100V SMD
C8	C13-0103-103	CAP .01UF 10% 100V SMD
C9	C13-0105-689	CAP 6.8PF +-.5PF 100V SMD
C10	C13-0103-103	CAP .01UF 10% 100V SMD
C11	C13-0103-103	CAP .01UF 10% 100V SMD
C12	C13-0103-103	CAP .01UF 10% 100V SMD
C13	C13-0103-103	CAP .01UF 10% 100V SMD
C14	C13-0103-103	CAP .01UF 10% 100V SMD
C15	C13-0103-103	CAP .01UF 10% 100V SMD
C16	C13-0103-103	CAP .01UF 10% 100V SMD
C17	C13-0103-103	CAP .01UF 10% 100V SMD
C18	C13-0103-103	CAP .01UF 10% 100V SMD
C19	C13-0103-473	CAP .047UF 10% 100V SMD
C20	C13-0103-473	CAP .047UF 10% 100V SMD
C21	C13-0103-473	CAP .047UF 10% 100V SMD
C22	C13-0103-103	CAP .01UF 10% 100V SMD
C23	C13-0103-103	CAP .01UF 10% 100V SMD
C24	C13-0105-680	CAP 68PF 10% 100V SMD
C25	C13-0105-680	CAP 68PF 10% 100V SMD
C26	C13-0103-473	CAP .047UF 10% 100V SMD
C27	C13-0103-473	CAP .047UF 10% 100V SMD
C28	C13-0105-680	CAP 68PF 10% 100V SMD
C29	C13-0105-680	CAP 68PF 10% 100V SMD
C30	C13-0103-103	CAP .01UF 10% 100V SMD
C31	C13-0103-103	CAP .01UF 10% 100V SMD
C32	C13-0103-473	CAP .047UF 10% 100V SMD

Table 7. A5A1 Second & Third Converter Assembly Parts List (10303-2610 Rev. B and Earlier) (Cont.)

Ref. Desig.	Part Number	Description
C33	C13-0103-473	CAP .047UF 10% 100V SMD
C34	C13-0103-473	CAP .047UF 10% 100V SMD
C35	C13-0103-103	CAP .01UF 10% 100V SMD
C36	C13-0103-103	CAP .01UF 10% 100V SMD
C37	C13-0103-103	CAP .01UF 10% 100V SMD
C38	C13-0103-102	CAP 1000PF 10% 100V SMD
C39	C22-0020-105	CAP 1.0UF 10% 20V TANT
C40	C22-0020-105	CAP 1.0UF 10% 20V TANT
C41	C22-0010-106	CAP, 10UF 10V 10% TANT
C42	C13-0103-473	CAP .047UF 10% 100V SMD
C43	C13-0103-473	CAP .047UF 10% 100V SMD
C44	C22-0025-106	CAP, 10UF 25V 10% TANT
C45	C13-0103-473	CAP .047UF 10% 100V SMD
C46	C13-0103-473	CAP .047UF 10% 100V SMD
C47	C13-0103-473	CAP .047UF 10% 100V SMD
C48	C22-0025-106	CAP, 10UF 25V 10% TANT
C49	C13-0103-473	CAP .047UF 10% 100V SMD
C50	C13-0103-473	CAP .047UF 10% 100V SMD
C51	C13-0103-473	CAP .047UF 10% 100V SMD
C52	C22-0010-226	CAP 22UF 10% 10V TANT
C53	C13-0103-473	CAP .047UF 10% 100V SMD
C54	C13-0103-473	CAP .047UF 10% 100V SMD
C55	C13-0103-473	CAP .047UF 10% 100V SMD
C56	C22-0010-106	CAP, 10UF 10V 10% TANT
C57	C22-0010-106	CAP, 10UF 10V 10% TANT
C58	C13-0103-103	CAP .01UF 10% 100V SMD
C59	C13-0103-102	CAP 1000PF 10% 100V SMD
C60	C13-0103-473	CAP .047UF 10% 100V SMD
C62	C13-0103-103	CAP .01UF 10% 100V SMD
C63	C13-0105-829	CAP 8.2PF +-.5PF 100V SMD
C64	C13-0103-473	CAP .047UF 10% 100V SMD
C65	C22-0050-225	CAP, 2.2UF 50V TANT
C67	C97-0002-473	CAP, 47000 UF 5.5V
CR1	1N4454	DIODE 200MA 75V SW
CR2	1N4454	DIODE 200MA 75V SW
CR3	1N4454	DIODE 200MA 75V SW
CR4	1N4454	DIODE 200MA 75V SW
CR5	1N4454	DIODE 200MA 75V SW

Table 7. A5A1 Second & Third Converter Assembly Parts List (10303-2610 Rev. B and Earlier) (Cont.)

Ref. Desig.	Part Number	Description
FL1	10303-3104	FILTER, 8 POLE XTAL 9.5 M
J1	J46-0115-020	CONN, 20 PIN MALE
JMP1	MP-1142	RES ZERO OHM (CKT JMPR)
L1	MS21426-27	COIL 15UH 10% FIXED RF
L2	MS21426-27	COIL 15UH 10% FIXED RF
L3	10303-3182	INDUCTOR, .056UH
L4	MS14046-4	COIL 10UH 10% FXD RF
L5	MS14046-4	COIL 10UH 10% FXD RF
L6	MS90538-12	COIL 100UH 5% FXD RF
L7	MS14046-4	COIL 10UH 10% FXD RF
L8	MS14046-4	COIL 10UH 10% FXD RF
L10	MS21426-9	COIL .47UH 10% FIXED RF
P5	J46-0117-020	CONN, 20 PIN MALE RT ANG
Q1	Q35-0003-000	XSTR N-CH JFET U310
Q2	2N5179	XSTR SS/RF NPN TO-72
Q3	2N5179	XSTR SS/RF NPN TO-72
Q4	2N2222A	XSTR SS/GP NPN TO-18
Q9	I90-0011-001	XSTR, DUAL MATCHED PR(LM1)
Q10	2N2907A	XSTR SS/GP PNP TO-18
R1	R85-0125-104	RES 100K 5% 1/8W FILM
R2	R85-0125-104	RES 100K 5% 1/8W FILM
R3	R85-0004-177	RES 619 1% 1/8W FLM
R4	R40-0016-202	RES VARIABLE 2K OHM PCB
R5	R85-0125-101	RES 100 5% 1/8W FILM
R6	R85-0125-102	RES 1.0K 5% 1/8W FILM
R7	R85-0125-100	RES 10 5% 1/8W FILM
R8	R85-0004-230	RES 2.0K 1% 1/8W SMD
R9	R85-0125-100	RES 10 5% 1/8W FILM
R10	R85-0125-682	RES 6.8K 5% 1/8W FILM
R11	R85-0125-272	RES 2.7K 5% 1/8W FILM
R12	R85-0125-100	RES 10 5% 1/8W FILM
R13	R85-0125-471	RES 470 5% 1/8W FILM
R14	R85-0125-100	RES 10 5% 1/8W FILM
R15	R85-0004-158	RES 392 1% 1/8W FLM
R16	R85-0004-151	RES 332 1% 1/8W FLM
R17	R85-0004-081	RES 68.1 1% 1/8W FLM
R18	R85-0004-130	RES 200 1% 1/8W FLM
R19	R85-0004-145	RES 287 1% 1/8W SMD

Table 7. A5A1 Second & Third Converter Assembly Parts List (10303-2610 Rev. B and Earlier) (Cont.)

Ref. Desig.	Part Number	Description
R20	R85-0125-102	RES 1.0K 5% 1/8W FILM
R21	R85-0004-230	RES 2.0K 1% 1/8W SMD
R22	R85-0125-101	RES 100 5% 1/8W FILM
R23	R85-0125-101	RES 100 5% 1/8W FILM
R24	R85-0004-230	RES 2.0K 1% 1/8W SMD
R25	R85-0125-102	RES 1.0K 5% 1/8W FILM
R26	R85-0125-101	RES 100 5% 1/8W FILM
R27	R85-0125-153	RES 15K 5% 1/8W FILM
R28	R85-0004-410	RES 124K 1% 1/8W SMD
R29	R85-0125-102	RES 1.0K 5% 1/8W FILM
R30	R85-0004-210	RES 1.24K 1% 1/8W SMD
R31	R85-0125-102	RES 1.0K 5% 1/8W FILM
R32	R85-0125-104	RES 100K 5% 1/8W FILM
R33	R40-0016-503	RES VAR 50K OHM PCB
R34	R85-0004-326	RES,18.2K 1% 1/8W CHIP
R35	R85-0004-381	RES 68.1K 1% 1/8W FLM
R36	R85-0004-201	RES 1000 1% 1/8W FLM
R37	R85-0004-350	RES 32.4K 1% 1/8W SMD
R38	R85-0125-104	RES 100K 5% 1/8W FILM
R39	R85-0004-434	RES 221K 1% 1/8W SMD
R40	R85-0004-434	RES 221K 1% 1/8W SMD
R41	R85-0125-273	RES 27K 5% 1/8W FILM
R42	R85-0125-823	RES 82K 5% 1/8W FILM
R43	R85-0004-145	RES 287 1% 1/8W SMD
R45	R85-0004-177	RES 619 1% 1/8W FLM
R46	R85-0004-269	RES 5110 1% 1/8W FLM
R47	R85-0125-100	RES 10 5% 1/8W FILM
R48	R85-0125-100	RES 10 5% 1/8W FILM
R49	R85-0125-100	RES 10 5% 1/8W FILM
R50	R85-0125-100	RES 10 5% 1/8W FILM
R51	R85-0125-100	RES 10 5% 1/8W FILM
R52	R85-0125-100	RES 10 5% 1/8W FILM
R53	R85-0125-330	RES 33 5% 1/8W FILM
R54	R85-0125-101	RES 100 5% 1/8W FILM
R55	R85-0125-103	RES 10K 5% 1/8W FILM
R56	R85-0125-101	RES 100 5% 1/8W FILM
R57	R85-0125-101	RES 100 5% 1/8W FILM
R58	R85-0125-101	RES 100 5% 1/8W FILM

Table 7. A5A1 Second & Third Converter Assembly Parts List (10303-2610 Rev. B and Earlier) (Cont.)

Ref. Desig.	Part Number	Description
R59	R85-0125-101	RES 100 5% 1/8W FILM
R60	R85-0004-151	RES 332 1% 1/8W FLM
R68	R85-0125-181	RES 180 5% 1/8W FILM
R70	R85-0004-366	RES 47.5K 1% 1/8W FLM
R71	R85-0004-230	RES 2.0K 1% 1/8W SMD
R72	R85-0004-366	RES 47.5K 1% 1/8W FLM
R73	R85-0004-366	RES 47.5K 1% 1/8W FLM
R74	R85-0004-366	RES 47.5K 1% 1/8W FLM
R75	R85-0004-230	RES 2.0K 1% 1/8W SMD
R77	R85-0125-100	RES 10 5% 1/8W FILM
R78	R85-0004-301	RES 10K 1% 1/8W FLM
R79	R85-0004-301	RES 10K 1% 1/8W FLM
R80	R85-0004-330	RES 20.0K 1% 1/8W FLM
R81	R85-0004-330	RES 20.0K 1% 1/8W FLM
RT1	D40-0004-003	THERM 1K 5% @ 25DEG
U2	I51-0007-001	IC MIXER ANALOG 12002
U3	I51-0007-001	IC MIXER ANALOG 12002
U4	I30-0048-002	IC, LP DUAL OP-AMP (MC331
U5	I30-0048-002	IC, LP DUAL OP-AMP (MC331
U6	I01-0000-353	IC 4538B PLASTIC CMOS
U7	I11-0020-001	VOLTAGE REG 5V (LM2936Z-5
U8	I11-0015-002	IC, VOLT REG, VAR (LM117H)
U9	I90-0012-001	IC,QUAD XSTR (MPQ2222A)
VR1	I14-0015-007	REG, PREC 2.5V (LM285BXZ-
VR2	1N4735	DIODE 6.2V 10% 1W ZENER
Z1	L50-0001-004	FERRITE BEAD

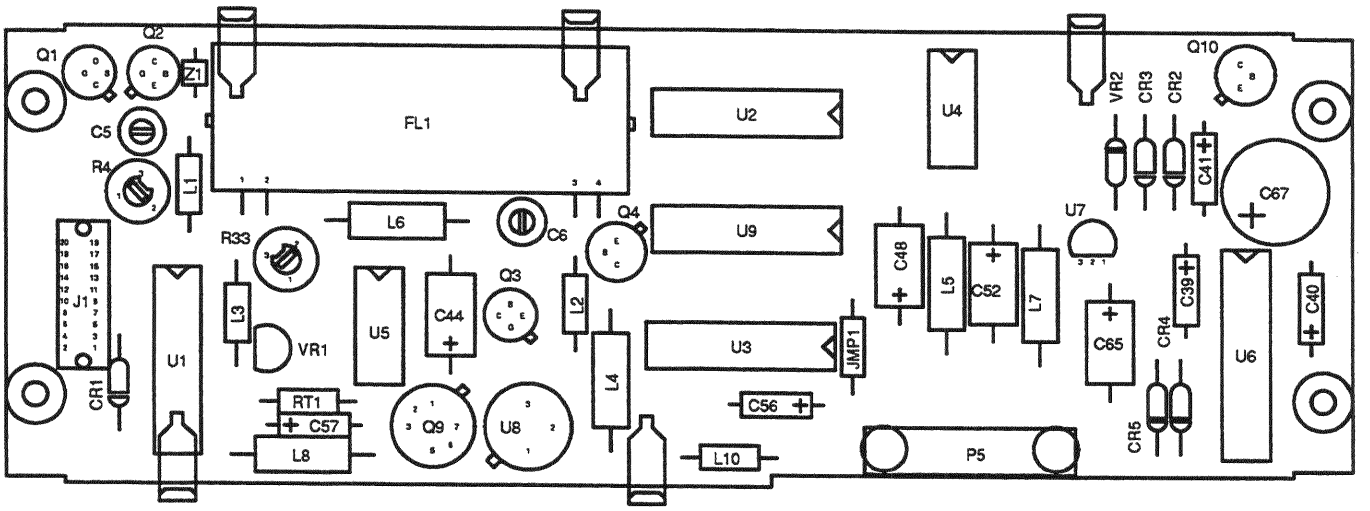


Figure 6. Second and Third Converter Assembly Component Location Diagram (10303-2610 Rev. A) (Sheet 1 of 2)

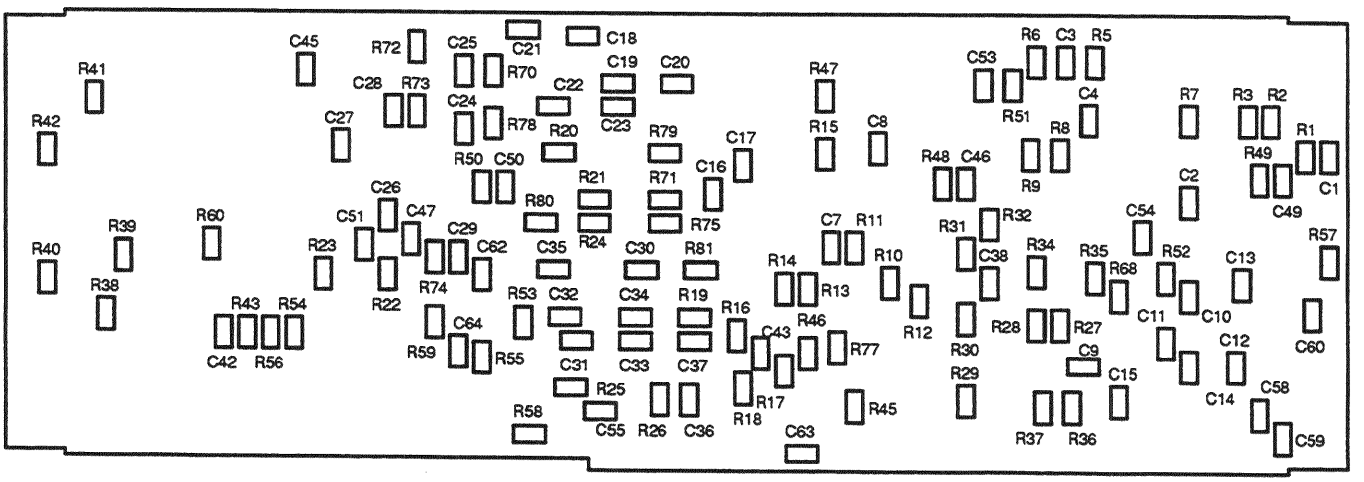
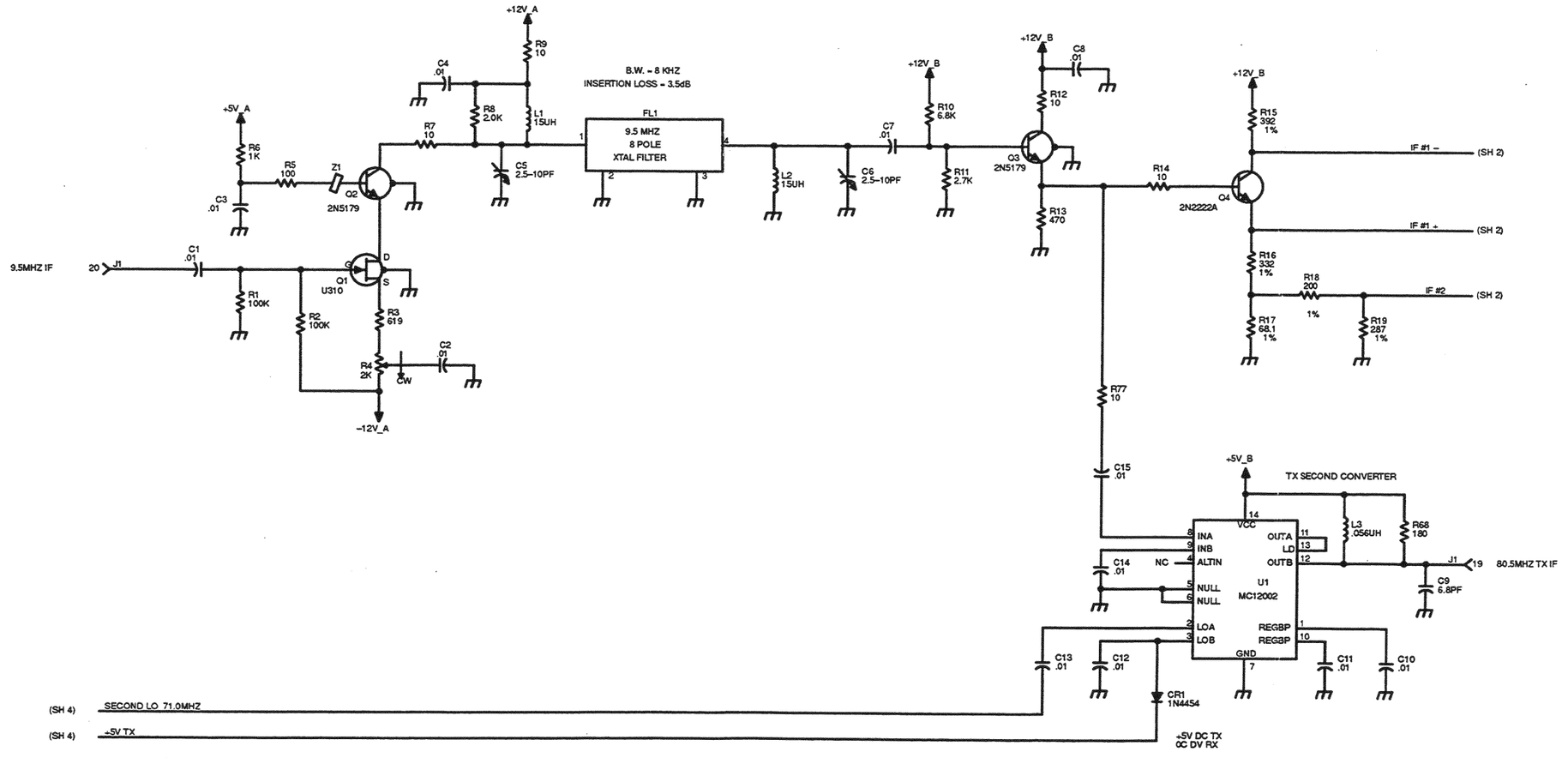


Figure 6. Second and Third Converter Assembly Component Location Diagram (10303-2610 Rev. A) (Sheet 2 of 2)

NOTE: UNLESS OTHERWISE SPECIFIED:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR A COMPLETE DESIGNATION, PREFIX WITH UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.
2. ALL RESISTOR VALUES ARE IN OHMS, 1/8W +/-5%.
3. ALL CAPACITOR VALUES ARE IN MICROFARADS.
4. VENDOR PART NO. CALLOUTS ARE FOR REFERENCE ONLY. COMPONENTS ARE SUPPLIED PER PART NO. IN PARTS LIST.



10303-2611 REV A
SHEET 1 OF 4

Figure 7. Second and Third Converter Assembly Schematic Diagram (10303-2611 Rev. A) (Sheet 1 of 4)

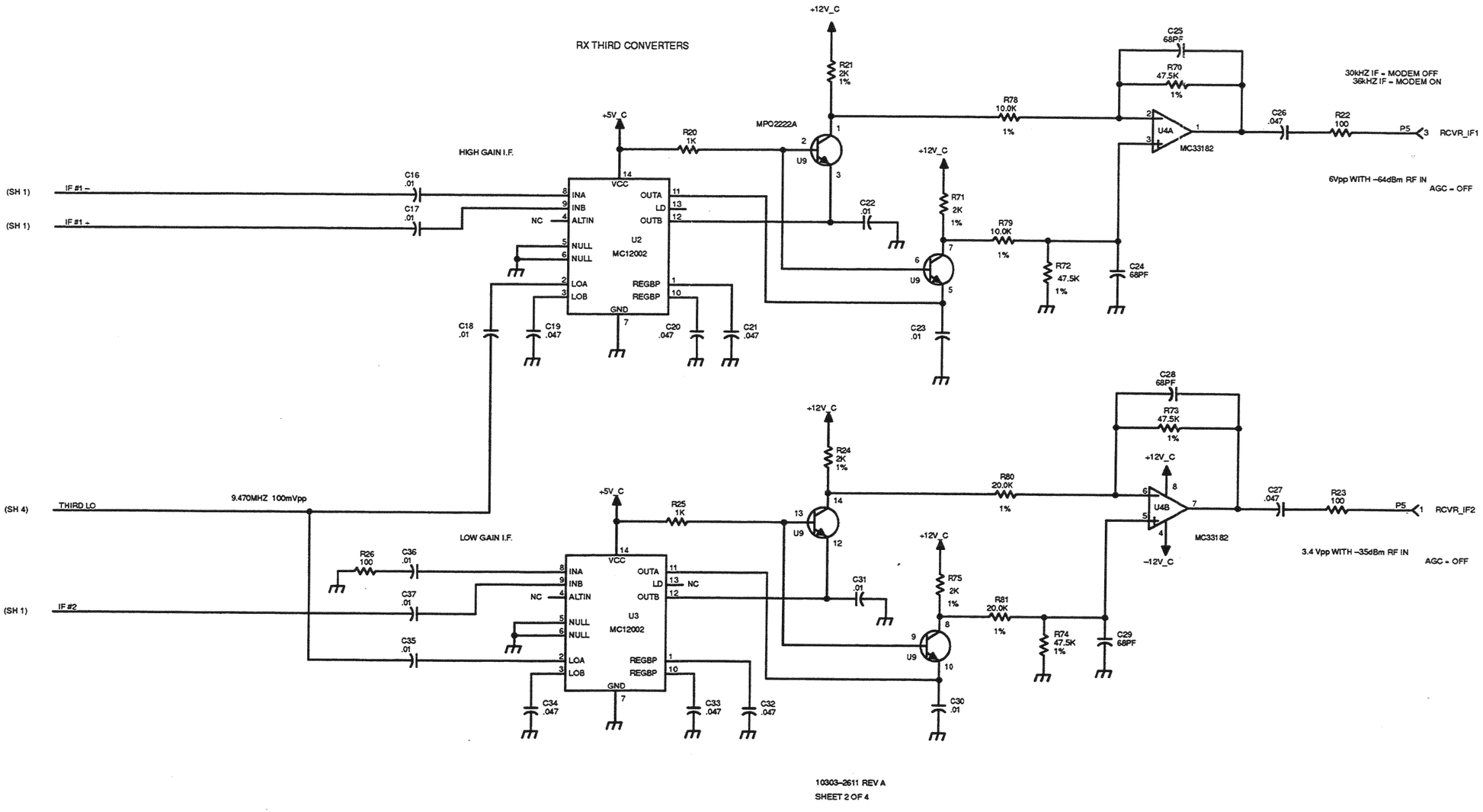


Figure 7. Second and Third Converter Assembly Schematic Diagram (10303-2611 Rev. A) (Sheet 2 of 4)

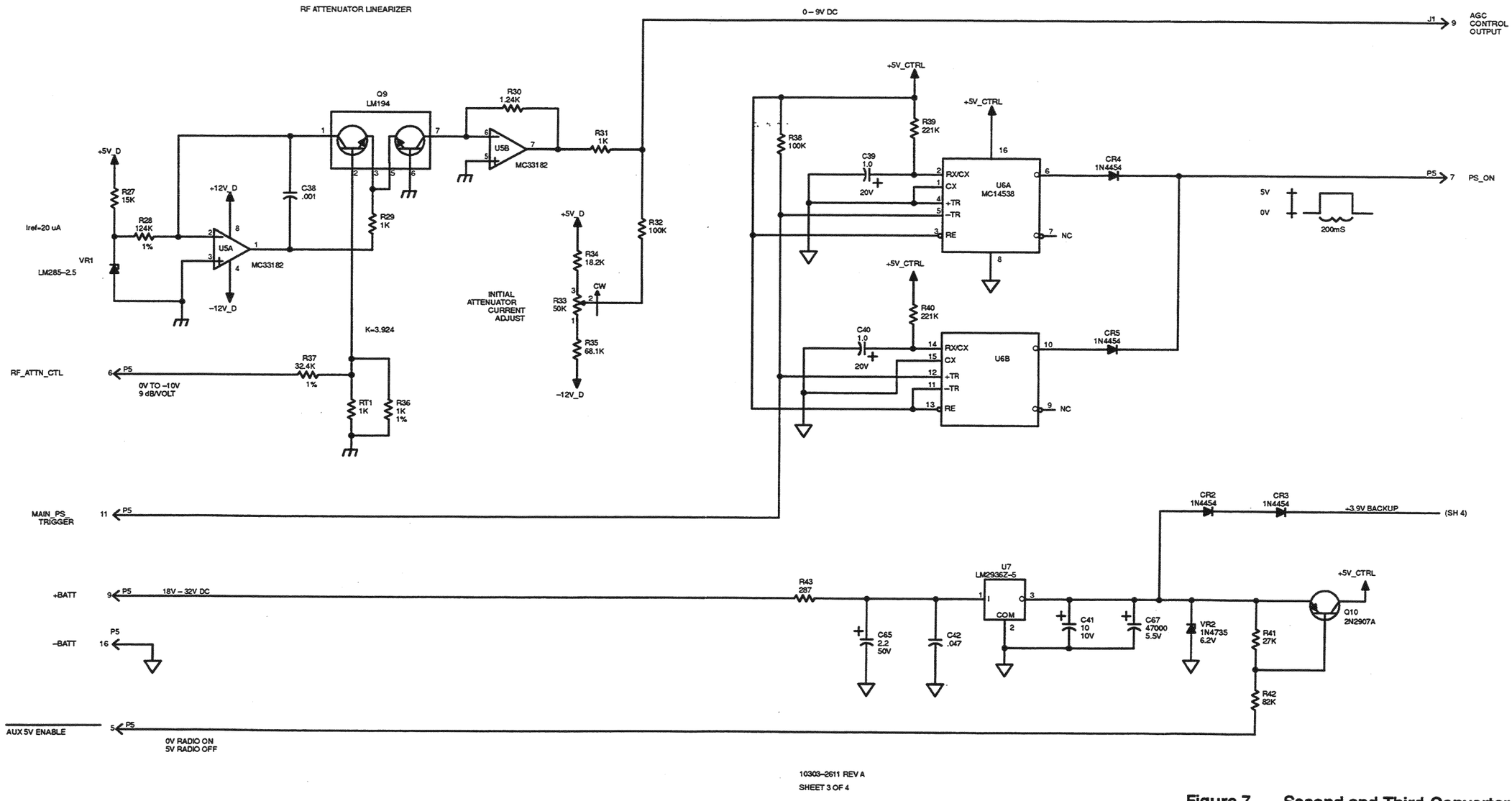
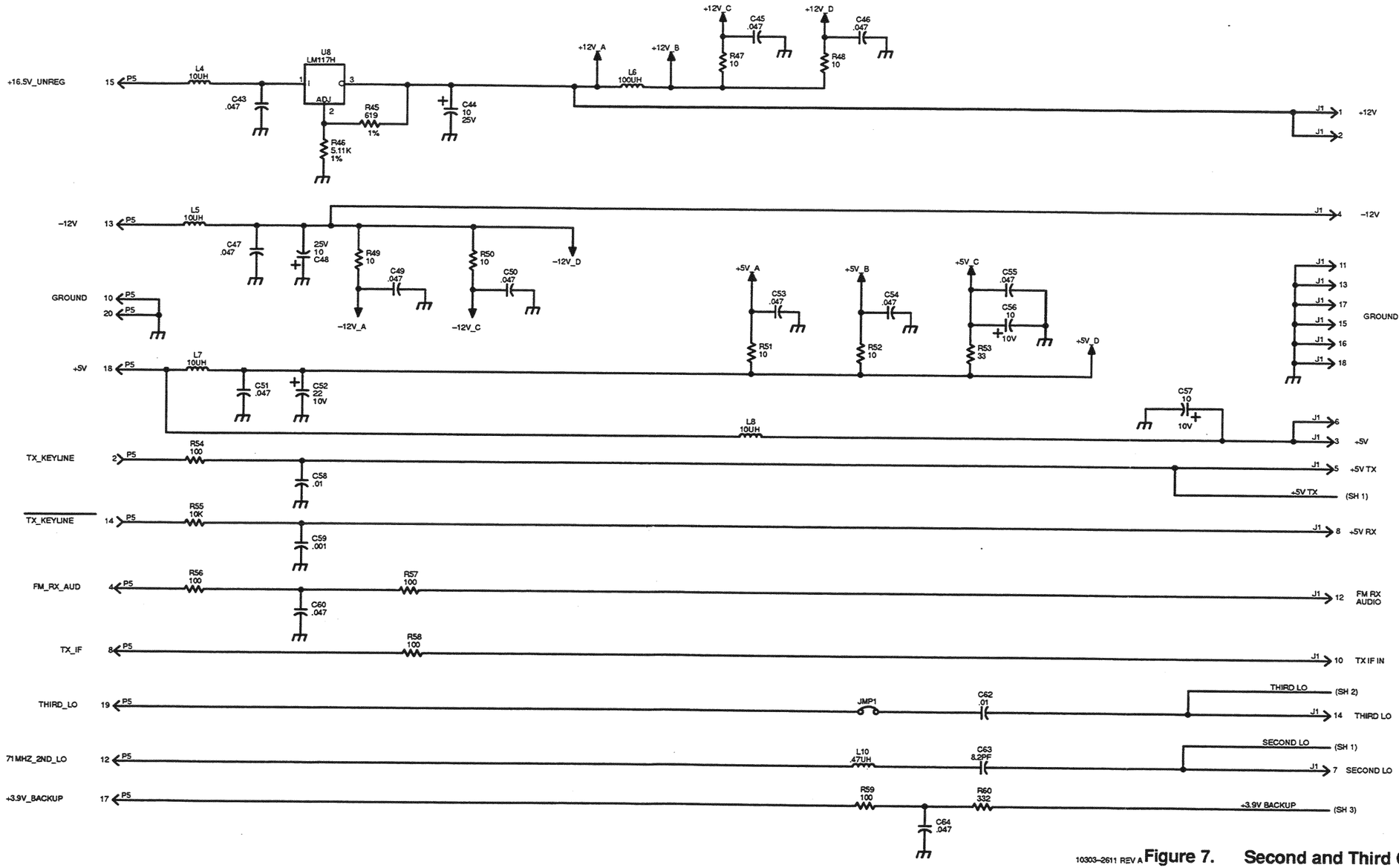


Figure 7. Second and Third Converter Assembly Schematic Diagram (10303-2611 Rev. A) (Sheet 3 of 4)



10303-2611 REV A
SHEET 4 OF 4

Figure 7. Second and Third Converter Assembly Schematic Diagram (10303-2611 Rev. A) (Sheet 4 of 4)

Table 8. A5A2 First Converter Assembly Parts List (10303-2270 Rev. P)

Ref. Desig.	Part Number	Description
1	10303-2271	SCHEM, FIRST CONVERTER
2	10303-2279	PWB, FIRST CONVERTER
3	E70-0002-004	PAD MNT XSTR TO-5
4	E70-0002-005	PAD MNT XSTR TO-18
5	10303-1040	SHIELD, FIRST CONVERTER
6	10372-3160	PWB ASSY, FILTER TANK
7	W20-0001-010	WIRE BUSS #22AWG TIN'D CU
8	10303-3023	GASKET, CONDUCTIVE
9	W20-0001-011	WIRE BUSS #20AWG TIN'D CU
11	10303-1046	SPACER
12	W20-0001-009	WIRE BUSS #24AWG TIN'D CU
13	P15-3140-000	SEALER RTV 3140
C2	C13-0105-330	CAP 33PF 10% 100V SMD
C4	C13-0105-620	CAP 62PF 5% 100V SMD
C6	C13-0105-560	CAP 56PF 10% 100V SMD
C7	C13-0105-330	CAP 33PF 10% 100V SMD
C8	C13-0105-390	CAP 39PF 5% 100V SMD
C9	C13-0103-103	CAP .01UF 10% 100V SMD
C10	C13-0103-473	CAP .047UF 10% 100V SMD
C11	C13-0103-473	CAP .047UF 10% 100V SMD
C12	C13-0103-473	CAP .047UF 10% 100V SMD
C13	C13-0103-473	CAP .047UF 10% 100V SMD
C14	C13-0103-473	CAP .047UF 10% 100V SMD
C15	C13-0103-103	CAP .01UF 10% 100V SMD
C16	C13-0103-473	CAP .047UF 10% 100V SMD
C17	C13-0103-473	CAP .047UF 10% 100V SMD
C18	C13-0103-473	CAP .047UF 10% 100V SMD
C19	C13-0103-473	CAP .047UF 10% 100V SMD
C20	C13-0103-103	CAP .01UF 10% 100V SMD
C23	C13-0103-103	CAP .01UF 10% 100V SMD
C24	C13-0103-103	CAP .01UF 10% 100V SMD
C26	C13-0103-103	CAP .01UF 10% 100V SMD
C27	C13-0103-103	CAP .01UF 10% 100V SMD
C28	C13-0103-103	CAP .01UF 10% 100V SMD
C29	C22-0025-106	CAP, 10UF 25V 10% TANT
C30	C13-0103-103	CAP .01UF 10% 100V SMD
C31	C85-0009-001	CAP VAR 2.5-10PF CER
C32	C13-0103-103	CAP .01UF 10% 100V SMD
C33	C13-0103-103	CAP .01UF 10% 100V SMD

Table 8. A5A2 First Converter Assembly Parts List (10303-2270 Rev. P) (Cont.)

Ref. Desig.	Part Number	Description
C34	C13-0103-103	CAP .01UF 10% 100V SMD
C35	C13-0103-103	CAP .01UF 10% 100V SMD
C36	C13-0103-103	CAP .01UF 10% 100V SMD
C37	C13-0105-100	CAP, CERAMIC CHIP, 10 PF
C38	C13-0105-102	CAP CER 1000PF 5% 100V
C40	C13-0103-103	CAP .01UF 10% 100V SMD
C41	C13-0103-103	CAP .01UF 10% 100V SMD
C42	C13-0103-473	CAP .047UF 10% 100V SMD
C43	C13-0103-473	CAP .047UF 10% 100V SMD
C44	C13-0103-103	CAP .01UF 10% 100V SMD
C45	C85-0009-001	CAP VAR 2.5-10PF CER
C46	C85-0009-001	CAP VAR 2.5-10PF CER
C47	C13-0103-103	CAP .01UF 10% 100V SMD
C48	C13-0103-103	CAP .01UF 10% 100V SMD
C49	C13-0103-103	CAP .01UF 10% 100V SMD
C50	C13-0103-103	CAP .01UF 10% 100V SMD
C51	C13-0105-820	CAP 82PF 10% 100V SMD
C52	C13-0103-473	CAP .047UF 10% 100V SMD
C53	C13-0103-473	CAP .047UF 10% 100V SMD
C54	C13-0103-473	CAP .047UF 10% 100V SMD
C55	C13-0105-102	CAP CER 1000PF 5% 100V
C56	C13-0103-103	CAP .01UF 10% 100V SMD
C57	C13-0103-222	CAP 2200PF 10% 100V SMD
C58	C13-0105-102	CAP CER 1000PF 5% 100V
C60	C13-0103-473	CAP .047UF 10% 100V SMD
C61	C13-0105-102	CAP CER 1000PF 5% 100V
C62	C13-0103-473	CAP .047UF 10% 100V SMD
C63	C13-0103-473	CAP .047UF 10% 100V SMD
C64	C13-0103-473	CAP .047UF 10% 100V SMD
C65	C13-0105-102	CAP CER 1000PF 5% 100V
C66	C85-0009-001	CAP VAR 2.5-10PF CER
C67	C13-0103-103	CAP .01UF 10% 100V SMD
C68	C13-0105-189	CAP 1.8PF +-.5PF 100V SMD
C69	C13-0103-104	CAP .1UF 10% 50V SMD
C71	C22-0050-224	CAP, 0.22UF 50V TANT
C72	C85-0009-001	CAP VAR 2.5-10PF CER
C73	C13-0105-181	CAP CER. 180PF 5% 50V
C74	C84-0009-001	CAP VAR 6-50PF CER
CR1	1N4454	DIODE 200MA 75V SW

Table 8. A5A2 First Converter Assembly Parts List (10303-2270 Rev. P) (Cont.)

Ref. Desig.	Part Number	Description
CR2	1N4454	DIODE 200MA 75V SW
CR3	D12-0007-001	DIODE PIN ATTN 1W 9301
CR4	D10-3500-000	DIODE .25W 35V PIN BSW
CR5	D10-3500-000	DIODE .25W 35V PIN BSW
CR6	D10-3500-000	DIODE .25W 35V PIN BSW
CR7	D12-0007-001	DIODE PIN ATTN 1W 9301
CR8	1N4454	DIODE 200MA 75V SW
FL1	10303-3140	FILTER
FL2	G25-0005-002	FILTER 455KHZ CER
J2	J92-0003-001	CONN SSMB RTANG PCB M
K1	K16-0009-001	RELAY SPOT TO-5 12V
K2	K16-0009-001	RELAY SPOT TO-5 12V
L4	MS75084-17	COIL 27.0UH 10% FXD RF
L5	MS75084-17	COIL 27.0UH 10% FXD RF
L6	L10-0009-278	COIL .27UH 10% FXD RF
L7	MS75084-8	COIL 4.7UH 10% FXD RF
L9	MS75087-5	COIL .22UH 10% FXD RF
L10	MS21426-3	COIL .15UH 10% FIXED RF
L11	MS21426-27	COIL 15UH 10% FIXED RF
L12	MS21426-24	COIL, 8.2UH 10% FXD RF SH
L13	MS75085-7	COIL 100UH 10% FXD RF
L14	MS18130-12	COIL 2.2UH 20% FXD RF
L15	MS14046-4	COIL 10UH 10% FXD RF
L16	MS75084-17	COIL 27.0UH 10% FXD RF
L17	MS18130-12	COIL 2.2UH 20% FXD RF
L18	MS75084-7	COIL 3.9UH 10% FXD RF
L19	10303-3106-32	TORID, 0.019 UH 5%
P1	J46-0113-020	CONN, 20 POS VERT MOUNT
P8	10303-1091	CABLE ASSY, RF
Q1	2N2907A	XSTR SS/GP PNP TO-18
Q2	2N2222A	XSTR SS/GP NPN TO-18
Q3	2N2222A	XSTR SS/GP NPN TO-18
Q4	2N2907A	XSTR SS/GP PNP TO-18
Q5	Q25-0015-000	XSTR RF VHF 2.5W MRF525
Q6	2N5179	XSTR SS/RF NPN TO-72
Q7	Q35-0003-000	XSTR N-CH JFET U310
Q8	2N2222A	XSTR SS/GP NPN TO-18
Q9	2N2222A	XSTR SS/GP NPN TO-18
Q10	Q35-0003-000	XSTR N-CH JFET U310

Table 8. A5A2 First Converter Assembly Parts List (10303-2270 Rev. P) (Cont.)

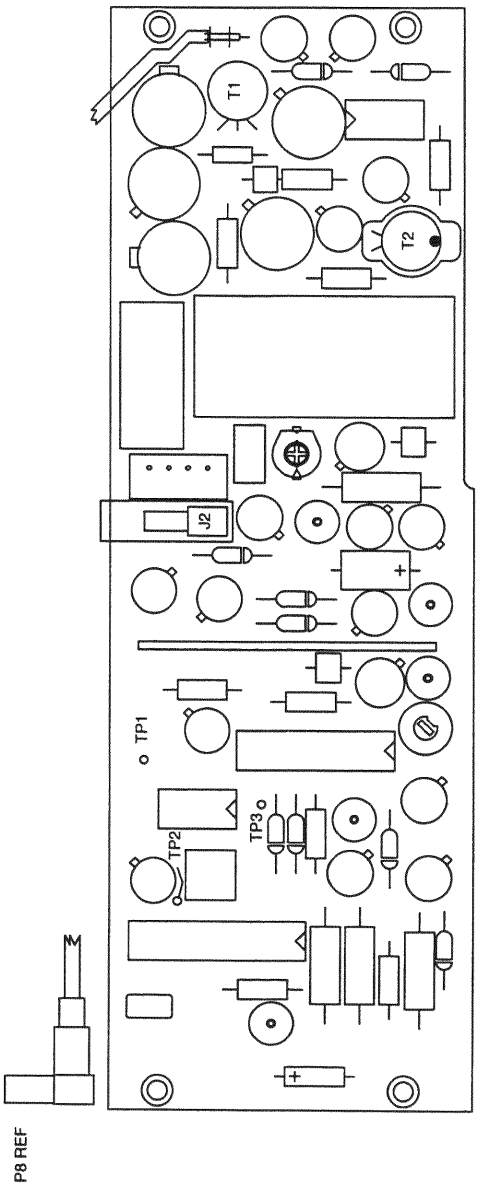
Ref. Desig.	Part Number	Description
Q11	2N2222A	XSTR SS/GP NPN TO-18
Q12	Q35-0003-000	XSTR N-CH JFET U310
Q13	2N5179	XSTR SS/RF NPN TO-72
Q14	2N2484	XSTR
Q15	2N2484	XSTR
Q16	2N2484	XSTR
Q17	2N2222A	XSTR SS/GP NPN TO-18
Q18	2N2222A	XSTR SS/GP NPN TO-18
R1	R85-0125-153	RES 15K 5% 1/8W FILM
R2	R85-0125-103	RES 10K 5% 1/8W FILM
R3	R85-0125-103	RES 10K 5% 1/8W FILM
R4	R85-0125-220	RES 22 5% 1/8W FILM
R5	R85-0125-103	RES 10K 5% 1/8W FILM
R6	R85-0125-100	RES 10 5% 1/8W FILM
R7	R85-0125-104	RES 100K 5% 1/8W FILM
R8	R85-0004-266	RES,4.75K 1% 1/8W CHIP
R9	R85-0125-100	RES 10 5% 1/8W FILM
R10	R85-0125-102	RES 1.0K 5% 1/8W FILM
R11	R85-0004-234	RES 2.21K 1% 1/8W FLM
R12	R85-0125-103	RES 10K 5% 1/8W FILM
R13	R85-0125-103	RES 10K 5% 1/8W FILM
R14	R85-0125-102	RES 1.0K 5% 1/8W FILM
R15	R85-0125-103	RES 10K 5% 1/8W FILM
R16	R85-0125-220	RES 22 5% 1/8W FILM
R17	R85-0125-100	RES 10 5% 1/8W FILM
R18	R85-0004-288	RES,8.06K 1% 1/8W CHIP
R19	R85-0125-100	RES 10 5% 1/8W FILM
R20	R85-0004-330	RES 20.0K 1% 1/8W FLM
R21	R85-0125-100	RES 10 5% 1/8W FILM
R22	R85-0125-223	RES 22K 5% 1/8W FILM
R23	R85-0125-302	RES 3.0K 5% 1/8W FILM
R24	R85-0125-102	RES 1.0K 5% 1/8W FILM
R25	R85-0004-081	RES 68.1 1% 1/8W FLM
R26	R85-0004-251	RES 3320 1% 1/8W
R27	R85-0125-103	RES 10K 5% 1/8W FILM
R28	R85-0004-166	RES 475 1% 1/8W SMD
R29	R85-0004-283	RES 7.15K 1% 1/8W SMD
R30	R85-0004-177	RES 619 1% 1/8W FLM
R31	R85-0125-101	RES 100 5% 1/8W FILM

Table 8. A5A2 First Converter Assembly Parts List (10303-2270 Rev. P) (Cont.)

Ref. Desig.	Part Number	Description
R32	R85-0125-104	RES 100K 5% 1/8W FILM
R33	R85-0004-134	RES 221 1% 1/8W FLM
R34	R85-0125-100	RES 10 5% 1/8W FILM
R35	R85-0125-100	RES 10 5% 1/8W FILM
R36	R85-0125-100	RES 10 5% 1/8W FILM
R37	R85-0004-330	RES 20.0K 1% 1/8W FLM
R38	R85-0004-288	RES,8.06K 1% 1/8W CHIP
R39	R85-0125-100	RES 10 5% 1/8W FILM
R40	R85-0125-100	RES 10 5% 1/8W FILM
R41	R85-0004-289	RES 8250 1% 1/8W FLM
R42	R85-0004-230	RES 2.0K 1% 1/8W SMD
R43	R85-0125-560	RES 56 5% 1/8W FILM
R44	R40-0016-103	RES VAR 10K OHM PCB
R45	R85-0125-560	RES 56 5% 1/8W FILM
R46	R85-0125-103	RES 10K 5% 1/8W FILM
R47	R85-0125-103	RES 10K 5% 1/8W FILM
R48	R85-0004-251	RES 3320 1% 1/8W
R49	R85-0125-101	RES 100 5% 1/8W FILM
R50	R85-0125-560	RES 56 5% 1/8W FILM
R51	R85-0004-239	RES 2490 1% 1/8W FLM
R52	R85-0004-218	RES 1500 1% 1/8W FLM
R53	R85-0004-334	RES 22.1K 1% 1/8W FLM
R54	R85-0125-104	RES 100K 5% 1/8W FILM
R55	R85-0125-103	RES 10K 5% 1/8W FILM
R56	R85-0004-366	RES 47.5K 1% 1/8W FLM
R57	R85-0004-201	RES 1000 1% 1/8W FLM
R58	R85-0004-271	RES,5.36K 1% 1/8W CHIP
R59	R85-0125-102	RES 1.0K 5% 1/8W FILM
R60	R85-0125-103	RES 10K 5% 1/8W FILM
R61	R85-0004-334	RES 22.1K 1% 1/8W FLM
R62	R85-0125-100	RES 10 5% 1/8W FILM
R63	R85-0125-100	RES 10 5% 1/8W FILM
R64	R85-0125-101	RES 100 5% 1/8W FILM
R65	R85-0125-221	RES 220 5% 1/8W FILM
R66	R85-0125-470	RES 47 5% 1/8W FILM
T1	10303-3115	XFMR, 4:1 BROADBAND
T2	10303-3116	XFMR,200-300 OHM RF
U1	I69-0002-003	IC MWA130 RF AMP WBW TO39
U2	I30-0043-101	IC, OP AMP SING SUP (MC33

Table 8. A5A2 First Converter Assembly Parts List (10303-2270 Rev. P) (Cont.)

Ref. Desig.	Part Number	Description
U3	I69-0002-003	IC MWA130 RF AMP WBW TO39
U4	I51-0008-001	MIXER, RF +7DBM
U5	I51-0007-001	IC MIXER ANALOG 12002
U6	I60-0006-003	IC, LOW PWR NB FM
U7	I30-0048-002	IC, LP DUAL OP-AMP (MC331
VR1	1N5248B	DIODE 18V 5% .5W ZENER
Y1	A01-0003-001	DISCRIMINATOR 455 KHZ CER
Z1	L50-0001-004	FERRITE BEAD
Z2	L50-0001-004	FERRITE BEAD
Z3	L50-0001-004	FERRITE BEAD



TOP SIDE SHOWN

Figure 8. First Converter Assembly Component Location Diagram (10303-2270 Rev. H) (Sheet 1 of 2)

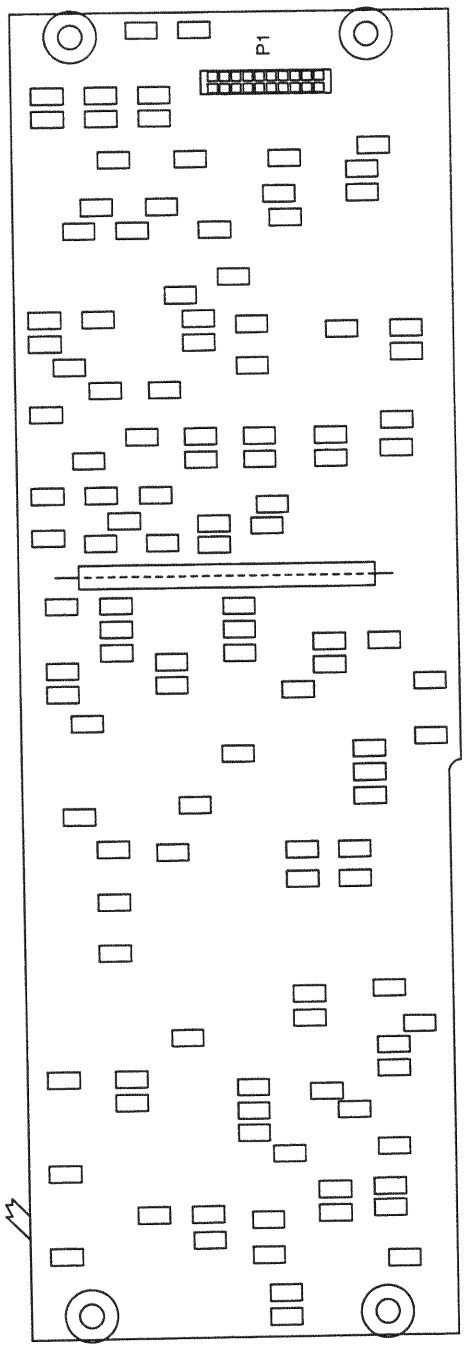


Figure 8. First Converter Assembly Component Location Diagram (10303-2270 Rev. H) (Sheet 2 of 2)

NOTE: UNLESS OTHERWISE SPECIFIED:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR A COMPLETE DESIGNATION, PREFIX WITH UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.
2. ALL RESISTOR VALUES ARE IN OHMS, 1/8W +/-5%.
3. ALL CAPACITOR VALUES ARE IN MICROFARADS.
4. VENDOR PART NO. CALLOUTS ARE FOR REFERENCE ONLY. COMPONENTS ARE SUPPLIED PER PART NO. IN PARTS LIST.
5. RELAYS SHOWN IN THE DE-ENERGIZED STATE.
6. L1,L2,L3,C3,C5, AND C7 SHOWN FOR REFERENCE ONLY. COMPONENTS INSTALLED ON ASSY 10372-3160 (ITEM 6).
7. FOR ASSY 10303-2270-02:
   U3,Z3, AND L4 REMOVED.
   C19 REPLACED BY ZERO OHM RESISTOR.
   U3 BYPASSED BY BUSS WIRE. (ITEM 7)
   R41 IS 6810 OHMS AND R42 IS 3320 OHMS.

TUNED ELEMENT	RF FREQUENCY	LO FREQUENCY
L1	f1 = 145.58 Mhz	L.O. = 226.08 MHZ
L2	f2 = 80.5 Mhz	L.O. = 161.0 MHZ
L3	f3 = 91.75 Mhz	L.O. = 172.25 MHZ

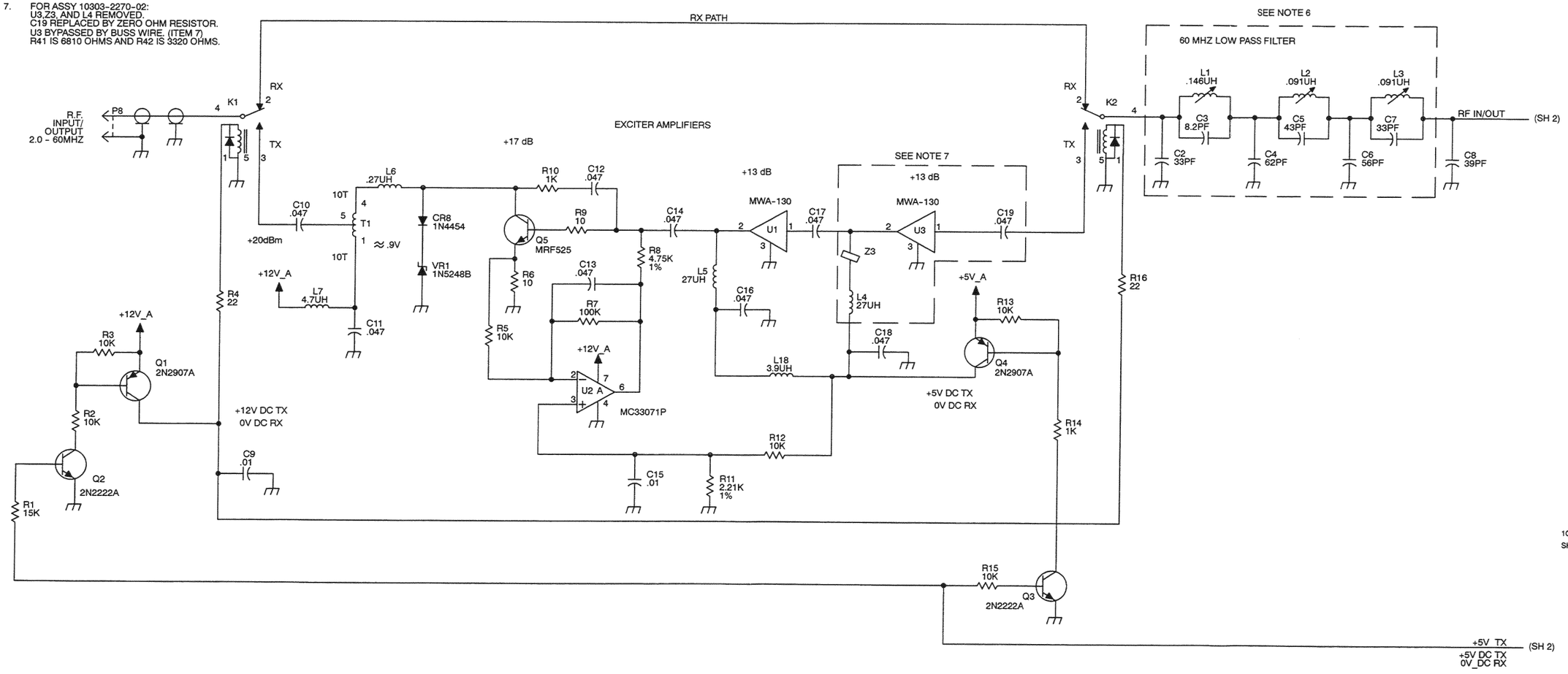


Figure 9. First Converter Assembly Schematic Diagram (10303-2271 Rev. B) (Sheet 1 of 4)

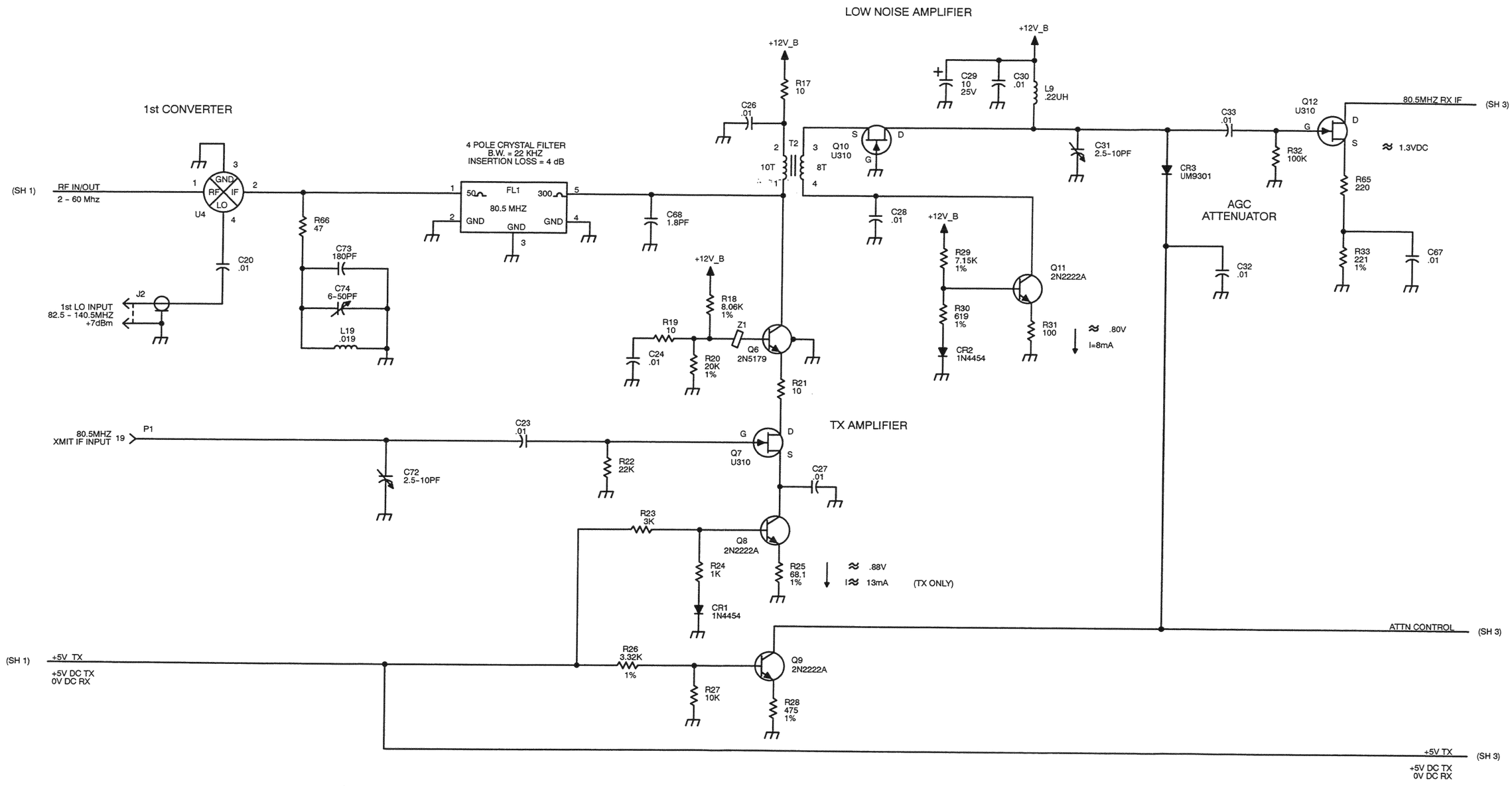


Figure 9. First Converter Assembly Schematic Diagram (10303-2271 Rev. B) (Sheet 2 of 4)

10303-2271 REV B
SHEET 2 OF 4

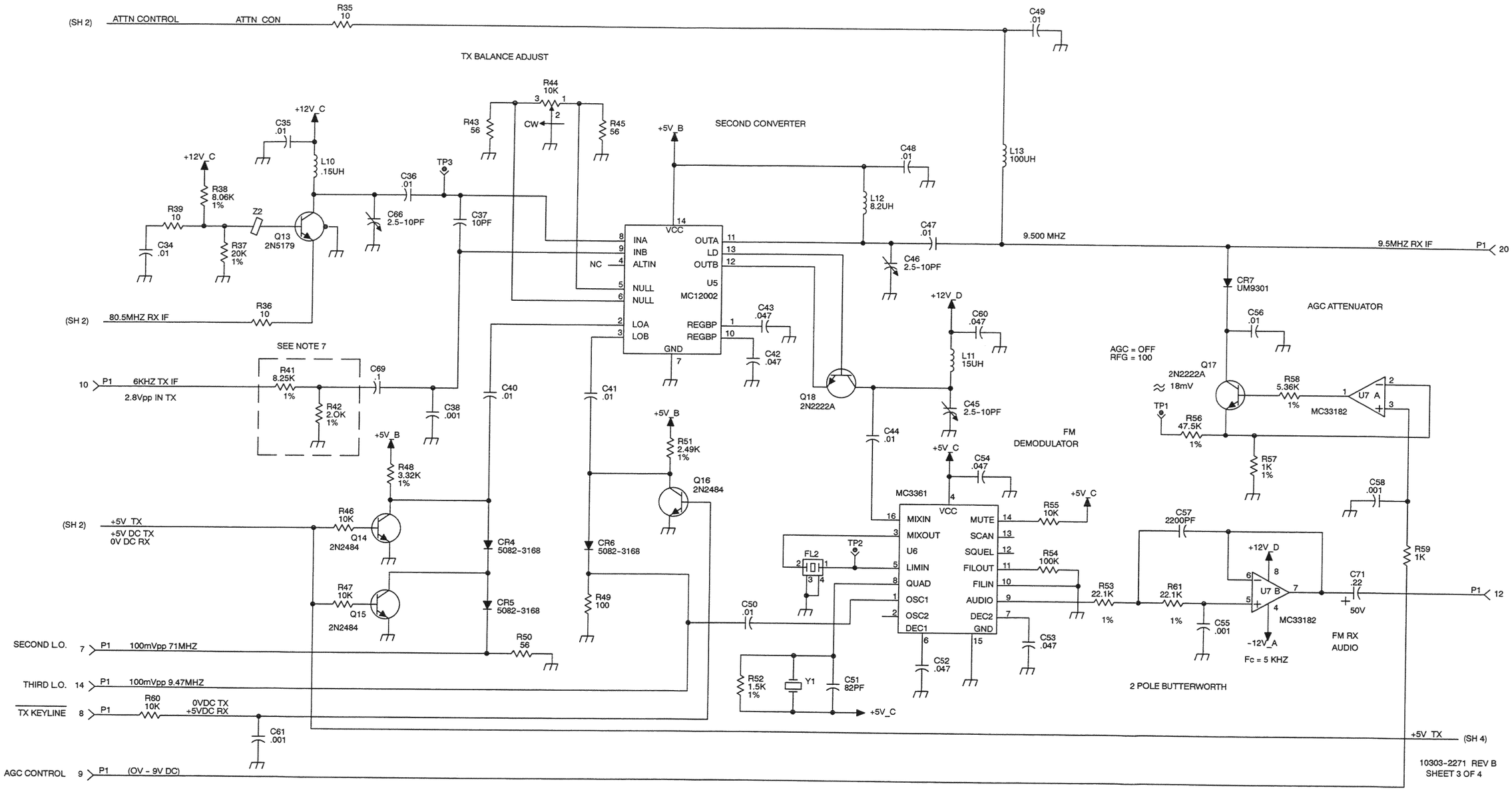
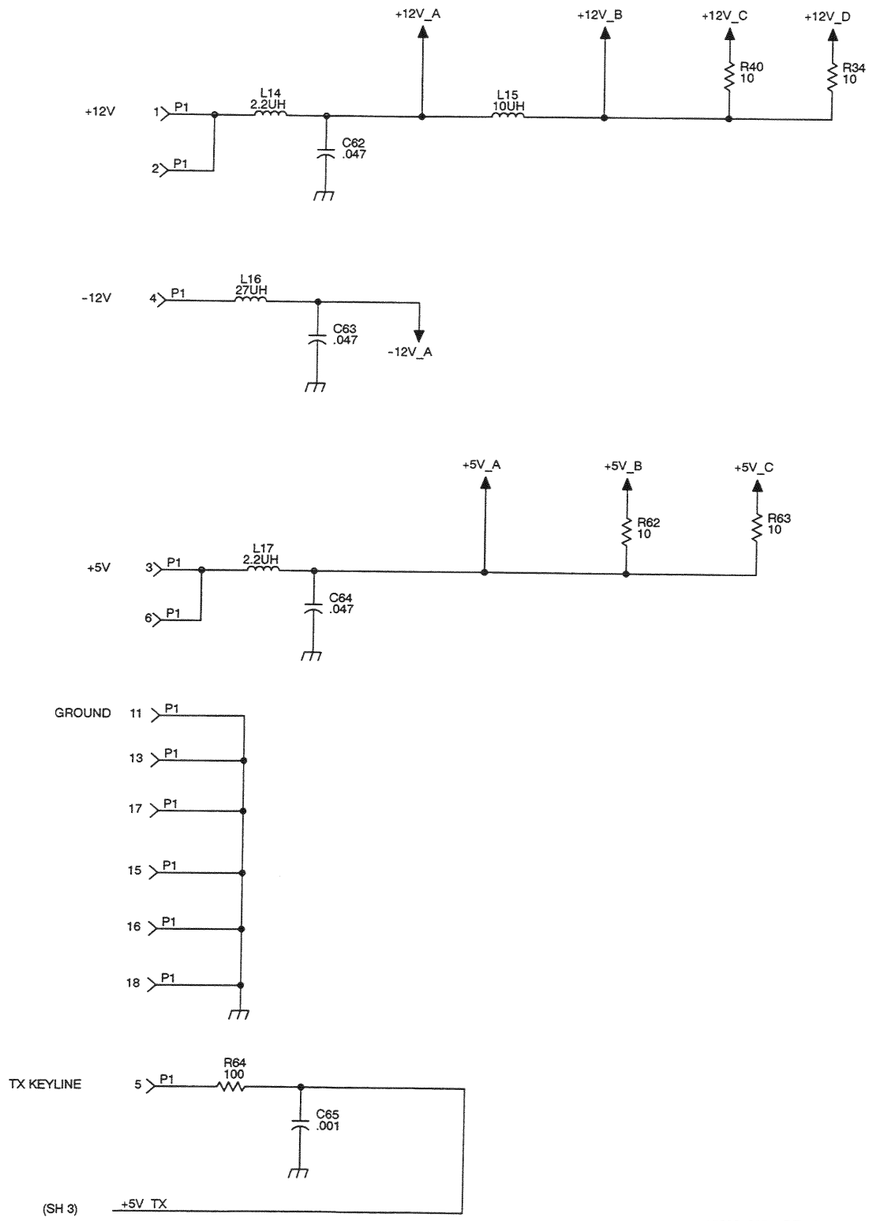


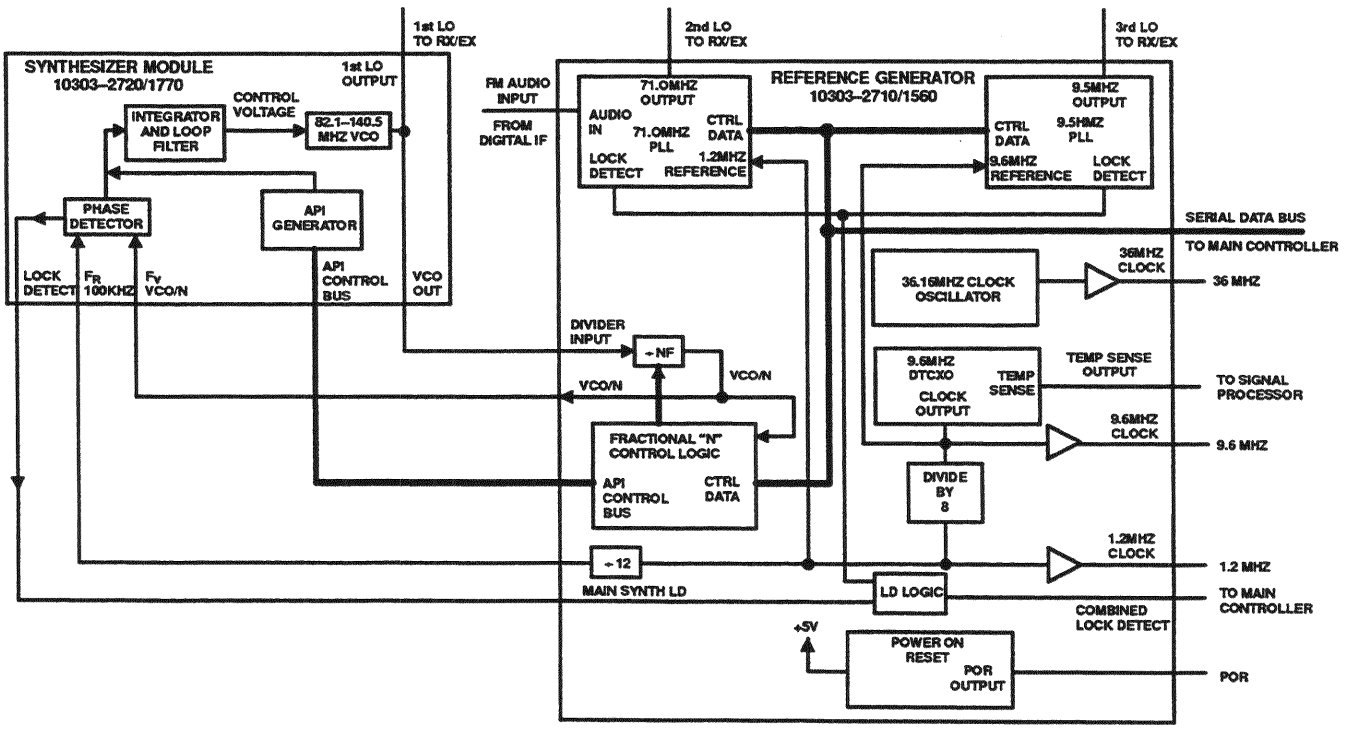
Figure 9. First Converter Assembly Schematic Diagram (10303-2271 Rev. B) (Sheet 3 of 4)



10303-2271 REV B
SHEET 4 OF 4

Figure 9. First Converter Assembly Schematic Diagram (10303-2271 Rev. B) (Sheet 4 of 4)

A6
REFERENCE GENERATOR/SYNTHESIZER



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A6 REFERENCE GENERATOR/SYNTHESIZER

1. GENERAL DESCRIPTION

The A6 Reference Generator/Synthesizer Assembly (10303-2700) consists of two separate assemblies, the A6A1 Reference Generator Assembly (10303-2710) and the A6A2 Synthesizer Assembly (10303-2720), as shown in figure 1. The A6A1 Reference Generator Assembly (10303-2710) contains a digitally temperature compensated crystal oscillator at 9.6 MHz that provides a high stability frequency reference for the radio. This assembly also generates nine other signals that are listed below.

- VCO/N frequency
- 100 kHz reference frequency
- 9.5 MHz third local oscillator
- 71 MHz second local oscillator
- Combined lock detect
- 1.2 MHz clock
- 9.6 MHz microprocessor clock
- 36.16 MHz microprocessor clock
- Power on reset

The A6A2 Synthesizer Assembly (10303-2720) contains the phase detector, loop filter, analog phase interpolator, and voltage controlled oscillator for a single loop Fractional N type synthesizer that is phase-locked to a 100 kHz reference, generated by the Reference Generator Assembly. The output frequency range of the synthesizer is 82.1000 MHz to 140.4999 MHz with a frequency resolution of 0.1 Hz. This fine resolution is possible due to the fractional N technique used in the Synthesizer, which allows finer resolution than the reference frequency of 100 kHz. Control of the Synthesizer is accomplished by the A4 Signal Processor Assembly via the synchronous serial control bus. The digital control logic for the synthesizer is located on the A6A1 Reference Generator Assembly.

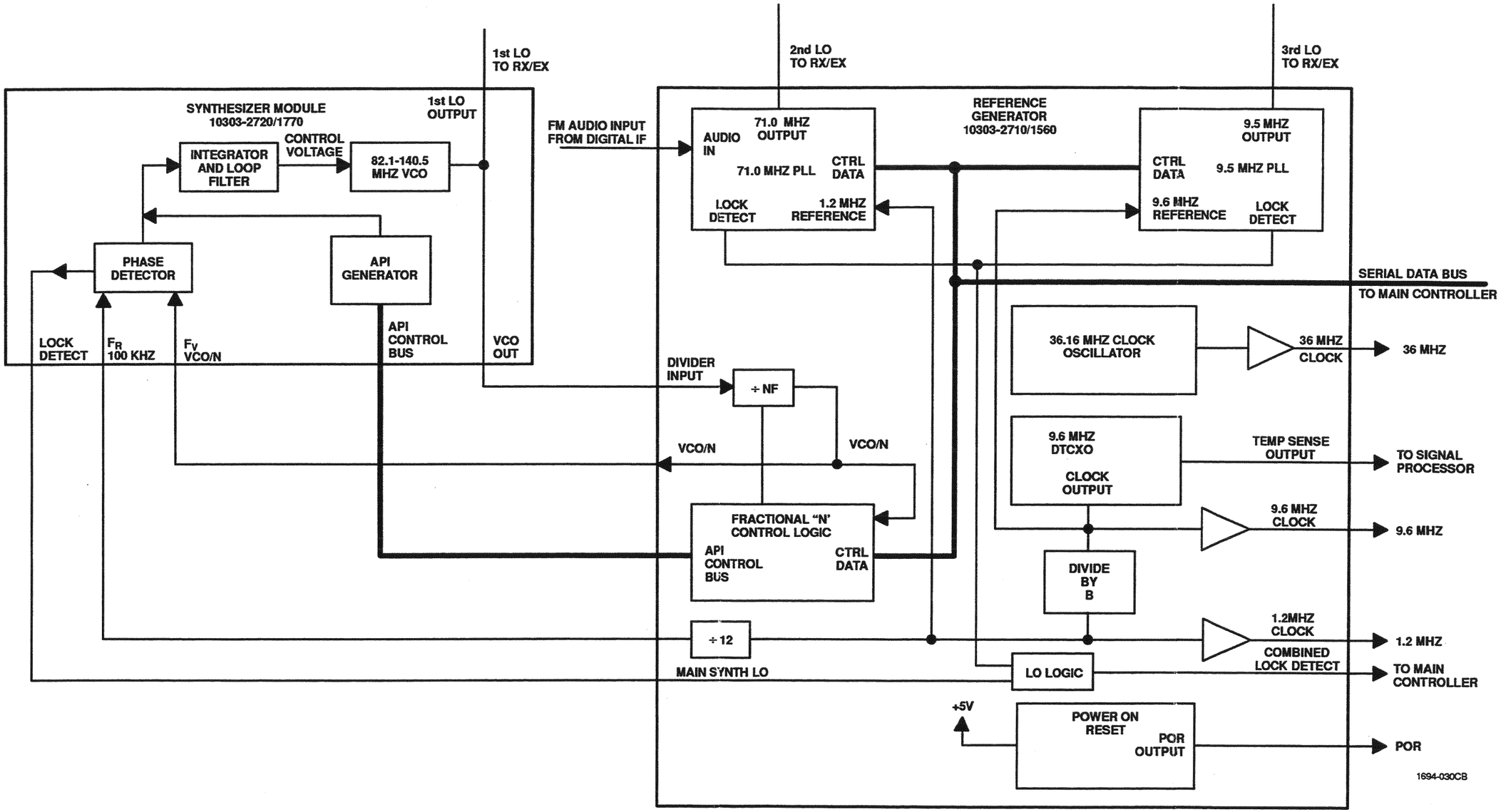


Figure 1. **A6 Reference Generator/ Synthesizer Assembly Block Diagram**

2. INTERFACE CONNECTIONS

Tables 1 and 2 list the signals sent to and received by the A6 Reference Generator/Synthesizer Assembly.

Table 1. Reference Generator Interconnect Connections

Connector and Pin	Signal	Comments
P4-1	36.16 MHz uP clock output	5 V CMOS logic 36.16 MHz ±100 ppm, 3 Vpp minimum
P4-2	PS Sync	Unused
P4-3	/POR	Power on reset, 0 V = reset when +5V line ≤4.5 V
P4-4	EEPROM strobe input	5 V CMOS logic 0 V = disabled, +5 V = enabled
P4-5	EEPROM data output	5 V CMOS logic
P4-6	9.6 MHz uP clock output	5 V CMOS logic, 9.6 MHz ±20 ppm, 50% duty cycle
P4-7	TCXO temp sense output	0 V TO 3 V output = –40C TO +80C
P4-8	1.2 MHz clock output	5 V CMOS logic, 1.2 MHz ± 20 ppm, 50% duty cycle
P4-9	FM TX audio input	10 Hz TO 10 kHz TX audio input, 4 Vpp nominal
P4-10	Main synth strobe input	5 V CMOS logic rising edge triggered
P4-11	Aux synth strobe input	5 V CMOS logic, logic 0 level triggered
P4-12	/Lock detect output	+5 V = unlocked, 0 V = locked, all synthesizers
P4-13	Serial clock input	5 V CMOS logic, 250 kHz, 50% duty cycle
P4-14	N.C.	
P4-15	Serial data input	5 V CMOS logic, 0 V = logic 0, +5 V = logic 1
P4-16	N.C.	
P4-17	N.C.	
P4-18	Third LO output	9.5 MHz to 9.6 MHz sinewave, 100 mVpp, Zo = 30 ohms
P4-19	EEPROM program enable	5 V CMOS logic, +5 V = pgrm, 0 V = read
P4-20	Second LO output	71 MHz sinewave, 100 mVpp, Zout = 7 ohms
P4-21	N.C.	
P4-22	+6.8 volts dc	Power input, 6.5 V ± 10%, I_{typ} = 40 mA
P4-23	–12 volts dc	Power input, –12 V ± 5%, I_{typ} = 26 mA
P4-24	–12 volts dc	Power input, –12 V ± 5%
P4-25	+16.5 volts dc	Power input, +16.5 V ± 10%, I_{typ} = 75 mA
P4-26	+16.5 volts dc	Power input, +16.5 V ± 10%
P4-27	+5 volts dc	Power input, +5 V ± 2%, I_{typ} = 130 mA
P4-28	+5 volts dc	Power input, +5 V ± 2%

Table 1. Reference Generator Interconnect Connections (Cont.)

Connector and Pin	Signal	Comments
P4-29	Ground	
P4-30	Ground	
J1-1	API control 5 output	5 V CMOS logic output
J1-2	API control 4 output	5 V CMOS logic output
J1-3	API control 1 output	5 V CMOS logic output
J1-4	Sample control input	5 V CMOS logic output
J1-5	Ground	
J1-6	API control 2 output	5 V CMOS logic output
J1-7	Ground	
J1-8	API control 3 output	5 V CMOS logic output
J1-9	Delayed bias output	5 V CMOS logic output
J1-10	+12 volts dc output	Power output, +12.0 V ± 8%
J1-11	Ground	
J1-12	Ground	
J1-13	+6.8 volts output	Power output, +6.5 V ± 10%
J1-14	Ground	
J1-15	Ground	
J1-16	–12 volts output	Power output, –12.0 V ± 5%
J1-17	/Main synth lock detect	Input, +5 V = unlocked, 0 V = locked
J1-18	VCO bandswitch output	Low ban = –12 V (82.1 – 109.9999 MHz), High band = 5 V (110.0 – 140.4999 MHz)
J1-19	Ground	
J1-20	Ground	
J1-21	Ground	
J1-22	Ground	
J1-23	100 kHz reference clock	5 V CMOS logic output, 50% duty cycle
J1-24	Ground	
J1-25	VCO/N output	5 V CMOS logic output, 3.9 MHz – 7.1 MHz
J1-26	Ground	
J1-27	Ground	
J1-28	Ground	
J1-29	Ground	
J1-30	VCO sample input	82.1 MHz – 140.49999 MHz, Z_{in} = 100 ohms

Table 2. Synthesizer Interconnect Connections

Connector and Pin	Signal	Comments
P2	First LO output	82.1 – 140.4999 MHz, +7 dBm, Zout = 50 ohms
J1-1	API control 5 input	
J1-2	API control 4 input	
J1-3	API control 1 input	
J1-4	Sample control input	
J1-5	Ground	
J1-6	API control 2 input	
J1-7	Ground	
J1-8	API control 3 input	
J1-9	Delayed bias input	
J1-10	+12 volts dc input	Power input, +12.0 V ± 8%
J1-11	Ground	
J1-12	Ground	
J1-13	+6.8 volts input	Power input, +6.5 V ±10%
J1-14	Ground	
J1-15	Ground	
J1-16	–12 volts input	Power input, –12.0 V ± 5%
J1-17	/Main synth lock detect	Output, + 5 V = unlocked, 0 V = locked
J1-18	VCO bandswitch input	
J1-19	Ground	
J1-20	Ground	
J1-21	Ground	
J1-22	Ground	
J1-23	100 kHz reference clock	100 kHz phase detecter input
J1-24	Ground	
J1-25	VCO/N input	VCO/N phase detector input
J1-26	Ground	
J1-27	Ground	
J1-28	Ground	
J1-29	Ground	
J1-30	VCO sample input	

3. SYNTHESIZER TECHNICAL DESCRIPTION

The technical description of the Synthesizer Assembly is presented in two parts: a functional description and a detailed circuit description. The functional description outlines the overall function of the synthesizer and the operational theory of a fractional, divide-by-N, phase-locked loop. The detailed circuit description describes the operation of the synthesizer circuit, including observable waveforms and signals.

3.1 Functional Description

The A6 Reference Generator/Synthesizer Assembly generates the first local oscillator (first LO) signal of 82.1 to 140.4999 MHz. The first LO is used to convert a received or transmitted signal between 1.600000 and 59.999999 MHz to an IF frequency of 80.5 MHz. The first LO is generated in a single phase-locked loop circuit using a fractional divide-by-N technique. Translation of the receive frequency shown on the front-panel display into the frequency that the First LO synthesizer is set to is done on the A4 Signal Processor Assembly. Synthesizer frequency resolution is possible to the 0.1-Hz level (for example, first LO=85,479,341.7 Hz); however, 1-Hz resolution is used in most transceiver modes.

3.1.1 Description of Fractional Divide-by-N Phase-Locked Loop

A simplified block diagram of synthesizer operation is shown in figure 2. The major elements in the phase-locked loop (PLL) are the phase detector, voltage controlled oscillator (VCO), and the divide-by-N circuit. As in all conventional indirect synthesizers, a divided sample of the VCO output is compared to a reference to yield a control voltage. The control voltage is adjusted by the phase detector and loop filter so that the output frequency of the VCO is equal to the divide-by-N value, times the reference frequency. For example, if the reference frequency is 100 kHz and the divide-by-N value is 919, the VCO frequency is 91.9 MHz. The frequency resolution of the PLL is 100 kHz since the divide-by-N value can only be an integer. A fractional divide-by-N PLL can generate a frequency with a resolution much greater than that of the PLL phase detector reference frequency. As in a standard PLL, the VCO output frequency is equal to the reference frequency, times the divide-by-N.F. (number fraction). A digital phase accumulator is used in conjunction with an analog compensation circuit to enable the synthesizer to resolve step sizes that are a fraction of the reference frequency. For example, a reference frequency of 100 kHz and a N.F. of 919.3754 results in a VCO frequency of 91.93754 MHz.

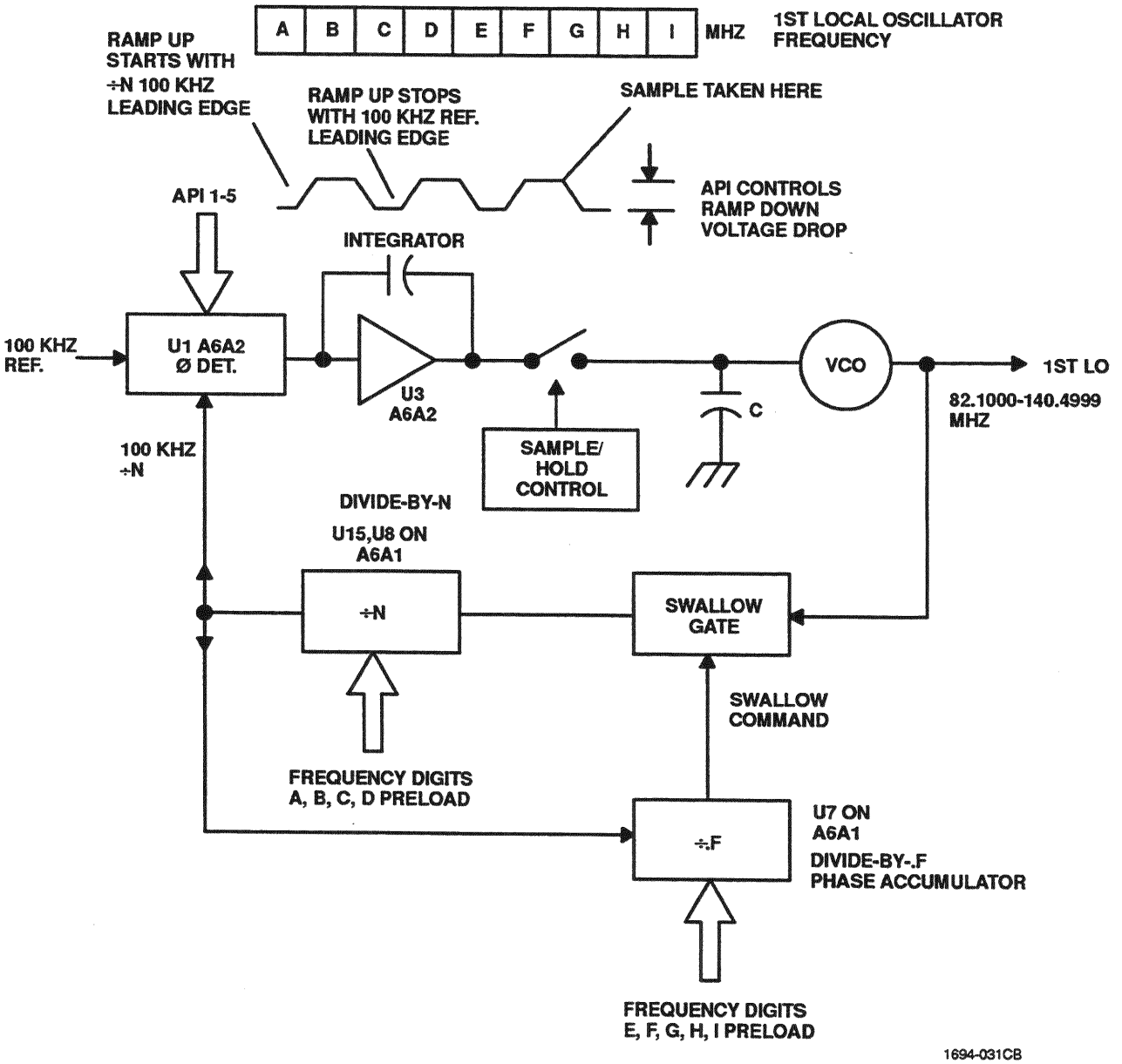


Figure 2. Synthesizer Simplified Block Diagram

3.1.2 Example of Divide-by-N.F.

The following example is given to clarify the operation of a fractional divide-by-N PLL. The following are operating characteristics for the example:

- Reference Frequency: 100 kHz
- N.F. Value: 919.375
- VCO Output Frequency: 91.9375 MHz (VCO = Ref. Freq. x N.F.)
- Fractional Characteristic: 375 (0.375 x 360 degrees = 135 degrees)

NOTES

The fractional characteristic should be considered in fractions of a VCO cycle, rather than in degrees of a VCO cycle; that is, 0.375 of phase accumulation, rather than 135 degrees of accumulation.

For all modes of operation, the first LO is equal to the operating frequency, plus 80.500 MHz. Therefore, for this example, the transceiver operating frequency is 11.4375 MHz.

Table 3 summarizes the activity of the fractional divide-by-N circuit through ten divide cycles. The individual steps are described in the paragraphs following the table.

Table 3. Fractional Divide-by-N Example

Divide Out	VCO Pulses In	Swallow?	Phase Accumulation
First	919	No	0.375 (0.00 + 0.375)
Second	919	No	0.750 (0.375 +0.375)
Third	920	Yes	0.125 (0.750 + 0.375 – 1.0 = 0.125)
Fourth	919	No	0.500 (0.125 + 0.375)
Fifth	919	No	0.875 (0.500 + 0.375)
Sixth	920	Yes	0.250 (0.875 + 0.375 – 1.0 = 0.250)
Seventh	919	No	0.625 (0.250 + 0.375)
Eighth	920	Yes	0.000 (0.625 + 0.375 – 1.0 = 0.00)
Ninth	919	No	0.375 (0.00 + 0.375)
Tenth	919	No	0.750 (0.375 + 0.375)

3.1.2.1 Step 1

The first 919 input VCO sample pulses are divided by 919, causing one output pulse from the divide-by-N circuit. The divide-by-N output pulse loads 0.375 (representing the .F fraction of a VCO cycle) into the phase accumulator that was empty when the process began.

3.1.2.2 Step 2

The next 919 input VCO sample pulses are divided by 919, causing a second output pulse from the divide-by-N circuit. A second 0.375 VCO cycle is loaded into the phase accumulator, which has now accumulated a total of 0.750 VCO cycle.

3.1.2.3 Step 3

The next 919 input VCO sample pulses are divided by 919, causing a third output pulse from the divide-by-N circuit. A third 0.375 VCO cycle is loaded into the phase accumulator, which now overflows with a total of 1.125 VCO cycle. The phase accumulator has now acquired a complete VCO cycle plus a remainder. To reduce this phase accumulation total by 1.00 VCO cycle, a VCO pulse is subtracted from the divide-by-N input. A VCO pulse is said to be swallowed. This reduces the phase accumulation total to 0.125 VCO cycle. Including the deleted (swallowed) pulse, 920 input VCO sample pulses are received during the third cycle.

3.1.2.4 Step 4

The next 919 input VCO sample pulses are divided by 919, causing a fourth output pulse from the divide-by-N circuit. A fourth 0.375 VCO cycle is loaded into the phase accumulator, which now has a total of 0.500 VCO cycle.

3.1.2.5 Step 5

The next 919 input VCO sample pulses are divided by 919, causing a fifth output pulse from the divide-by-N circuit. A fifth 0.375 VCO cycle is loaded into the phase accumulator, which now has a total of 0.875 VCO cycle.

3.1.2.6 Step 6

The next 919 input VCO sample pulses are divided by 919, causing a sixth output pulse from the divide-by-N circuit. A sixth 0.375 VCO cycle is loaded into the phase accumulator, which now overflows with a total of 1.25 VCO cycle. This overflow causes the accumulator to subtract 1.00 VCO cycle by swallowing the next VCO pulse, leaving a remainder of 0.250 VCO cycle. Including the deleted pulse, 920 input VCO sample pulses are received during this cycle.

3.1.2.7 Step 7

The next 919 input VCO sample pulses are divided by 919, causing a seventh output pulse from the divide-by-N circuit. A seventh 0.375 VCO cycle is loaded into the phase accumulator, which now has a total of 0.625 VCO cycle.

3.1.2.8 Step 8

The next 919 input VCO sample pulses are divided by 919, causing an eighth output pulse from the divide-by-N circuit. An eighth 0.375 VCO cycle is loaded into the phase accumulator, which now overflows with a total of 1.00 VCO cycle. This overflow causes the accumulator to subtract 1.00 VCO cycle by swallowing the next VCO pulse, leaving a remainder of 0.00 VCO cycle. Including the deleted (swallowed) pulse, 920 input VCO sample pulses are received during this cycle.

3.1.2.9 Step 9

With the accumulator now empty, the cycle repeats each eight divide-by-N output pulses. To calculate the average divide number for this example:

- Total VCO pulses: 919 + 919 + 920 + 919 + 919 + 920 + 919 + 920 = 7355
- Divider output pulses: 8
- Average divider characteristic: 7355/8 = 919.375
- VCO frequency: = Reference frequency x divider characteristic
  = 100 kHz x 919.375
  = 91.9375 MHz (the desired VCO frequency)

3.1.3 Analog Phase Interpolation (API) and VCO Control Voltage

The divide-by-N technique requires some refinement, since the VCO must operate at an exact frequency, not an average frequency. The accumulating phase error and VCO pulse swallowing cause spurious VCO frequency outputs because of changes in the VCO control voltage. To overcome this effect, an Analog Phase Interpolator (API) circuit is used in the phase detector. This is described in detail in subsection 3.2.2.

The API anticipates a pulse swallow and makes corrections to the integrator so that large error signals are not transmitted to the VCO. When the divide-by-N circuit produces an output pulse, the phase detector ramp up current is turned on, causing the integrator (essentially a capacitor) to charge, which causes its output voltage to ramp up. The current sink charging the capacitor is turned off by the leading edge of a 100-kHz reference pulse and the ramp voltage levels off. The level of the integrator output voltage is proportional to the phase difference between the 100-kHz signal from the divide-by-N circuit and the 100-kHz reference signal. The integrator output voltage is sampled on each reference cycle, retained by the sample-and-hold circuit, and passed on to the VCO. Following the sampling, a "delayed bias" signal turns on a ramp down current source, which causes the integrator output voltage to slope down as the integrator capacitor is discharged.

When the N.F. includes a fractional element, the VCO operates at a frequency somewhat higher than the frequency indicated by the divide-by-N circuit. In the example, the divide-by-N is 919, indicating a VCO frequency of 91.9 MHz, where the actual VCO frequency (as a result of the .F fraction) is 91.9375 MHz. The fractional part of the VCO frequency results in an advancing phase error that would cause the integrator voltage to ramp up to a higher output level on each succeeding output cycle as the phase difference accumulates. The API circuit prevents this by controlling the discharge of the integrator so that the integrator output voltage drops below the previous starting level for each succeeding cycle, in anticipation of the advancing phase error. In this way, the integrator always ramps up to the same voltage. The voltage sample taken by the sample and hold is then taken at the same voltage each time to obtain the correct VCO frequency.

The ramp-down current is controlled by five API switches which are, in turn, controlled by the phase accumulator. Each time the divide-by-N circuit produces an output pulse, the phase accumulator increments with the phase characteristic (0.375 VCO cycle in the example). The number stored in the phase accumulator at any time corresponds to the accumulated phase difference. The 100-kHz, divide-by-N sample pulses occur sooner and sooner with reference to the 100-kHz reference pulse. The correction is obtained by converting the number held in the phase accumulator into five data bits, each of which controls an API current switch. The API switches are turned on in combinations that correspond to the numerical value of the phase accumulation, with API1 representing the most-significant digit and API5 representing the least-significant digit. Each API switch represents a current that alters the discharge rate of the integrator capacitor. The API1 current sink has a magnitude of 25 uA, and the API2 current sink has a magnitude of 2.5 uA. Each successive API current sink decreases by a factor of ten.

3.2 Detailed Circuit Operation

Figure 3 is a block diagram of the First LO, and the A6 Reference Generator/Synthesizer Assembly schematic is shown at the end of this section. The synthesizer is described in the following subsections:

- Serial Data Control
- Phase Detector/Integrator/Analog Phase Interpolator
- Sample and Hold
- Loop Filter
- Voltage Controlled Oscillator (VCO)
- Divide by N.F. (Number Fractional)

3.2.1 Serial Data Control

Frequency information is provided by the Signal Processor Assembly A4 as a serial data stream consisting of data, clock, and main synthesizer strobe. Serial data is clocked into fractional-N logic array U7 and programmable logic array U8. The data bits are latched into shift registers on the rising edge of the main synthesizer strobe pulse. The data consists of six decades of BCD information, two control bits, and seventeen binary bits. The six BCD decades, corresponding to the fractional steps 0.1 Hz, 1 Hz, 10 Hz, 100 Hz, 1 kHz, and 10 kHz, are shifted into the fractional-N logic array U7. The control bits, shifted into U8, are used for VCO band control. The seventeen binary bits contain the information for the integer divider contained in programmable logic array U8.

3.2.2 Phase Detector and Analog Phase Interpolator (API) – General Description

A simplified block diagram of the dual-slope, sample-and-hold phase detector is shown in figure 4. The phase detector circuit U1 converts a phase difference between the 100-kHz reference signal and the 100-kHz feedback signal into a control voltage for the VCO. The VCO control voltage is developed by sinking or sourcing a precision current through integrator capacitor A6A2C8. This voltage can range between –6 volts and +6 volts, and has a typical waveform shape, as shown in figure 4. The phase detector output voltage waveform can be broken into three phases, the ramp up phase, the sample phase, and the ramp-down phase.

3.2.2.1 Phase Detector Ramp Up Phase

A sequential phase/frequency comparator, A6A2U1 is used to gate the up ramp current sink into the integrator. The comparator is configured to behave like a single flip flop that is set, LOGIC 0, by the leading edge of the VCO/N.F. signal, and is reset, LOGIC 1, by the leading edge of the 100-kHz reference signal. The 100-kHz reference signal for the phase detector is divided down from the 9.600 MHz reference oscillator A6A1U1. The VCO sample signal is divided down to 100 kHz by the divide-by-N.F. circuit consisting of A6A1U7, A6A1U8, and A6A1U15. The positive-going edge of the VCO/N.F. signal sets the flip flop which biases transistor A6A2Q1 on and turns off transistor A6A2Q2. With Q2 off, a voltage of about –1.3 volts is developed on the anode of A6A2CR3 causing it to be reverse biased. When A6A2CR3 is reverse biased, a current path from A6A2C8 through A6A2CR4 and A6A2Q12 is established, allowing a precision current of 4.3 mA to charge the integrator capacitor. The leading edge of the 100 kHz reference signal resets the phase detector flip-flop, which biases on transistor A6A2Q2 and turns off transistor Q1. This causes a voltage of about +0.8 volts to appear at the anode of diode A6A2CR3 which forward biases CR3 and reverse biases diode A6A2CR4. The ramp up current is diverted away from the integrator causing the integrator output voltage to level off until the voltage is stored in the sample and hold circuit. The voltage on the integrator capacitor can be monitored at A6A2U3-6.

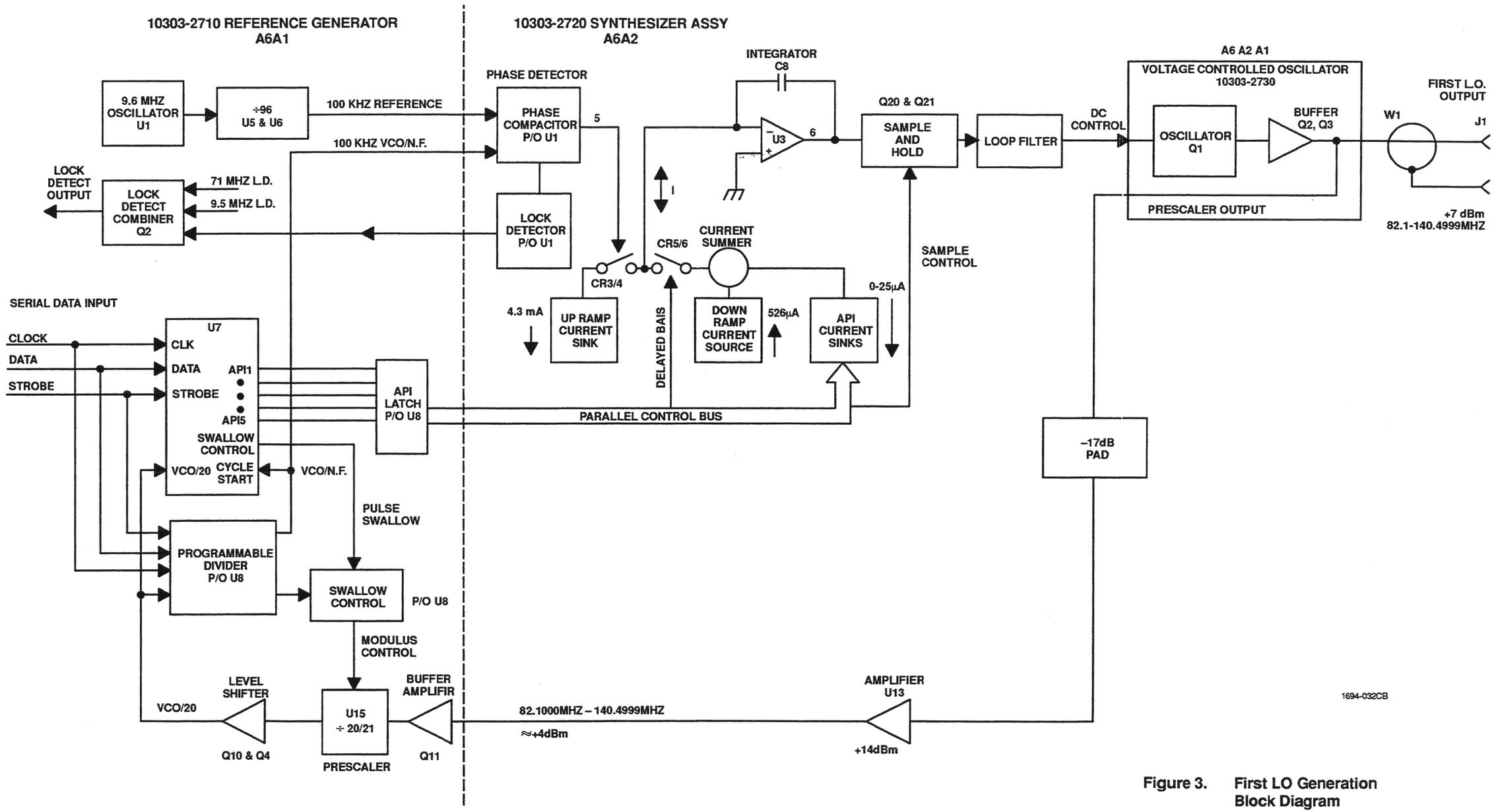
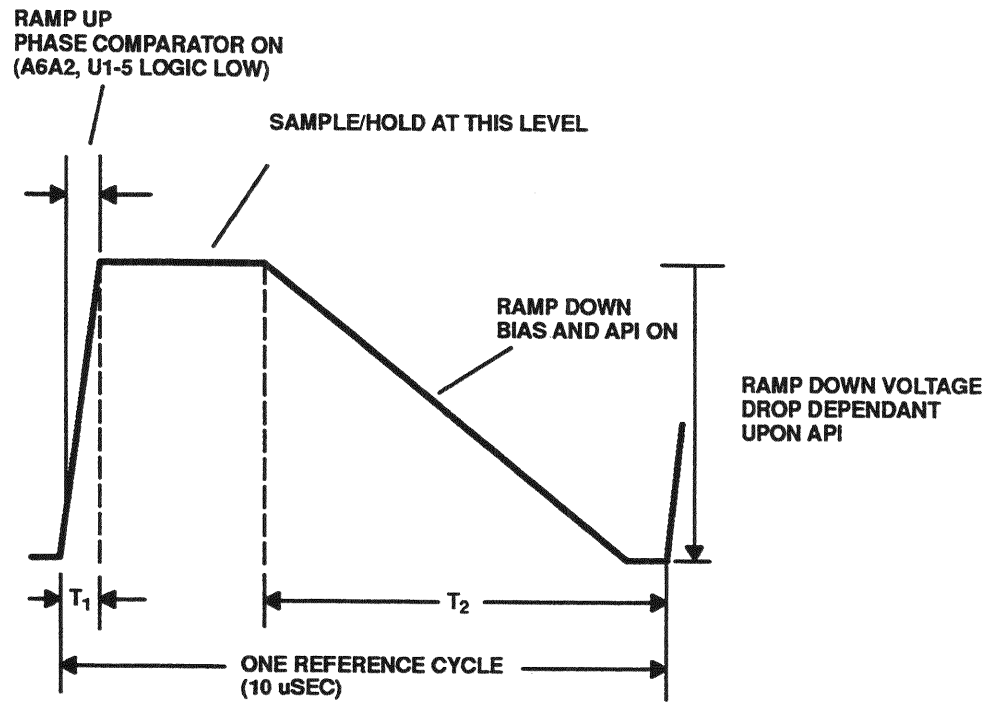


Figure 3. First LO Generation Block Diagram



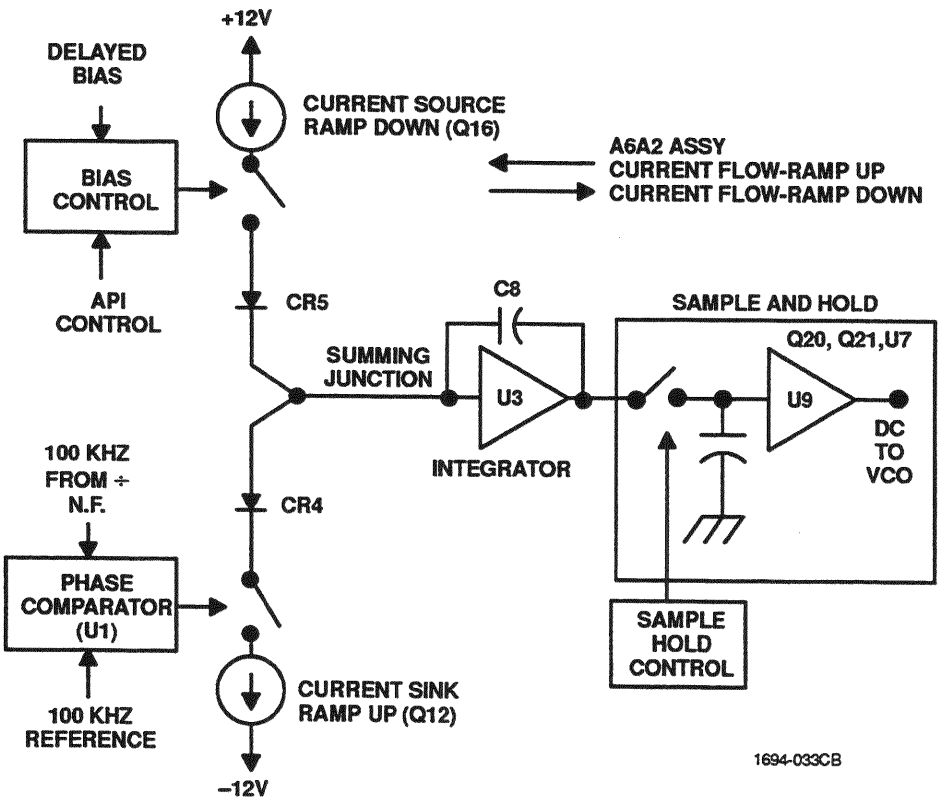


Figure 4. Simplified Phase Detector and Integrator Waveform

3.2.2.2 Phase Detector Sample and Ramp Down Phases

Refer to figure 4. During the hold period, CR4 and CR5 are biased off so the integrator capacitor C8 cannot charge or discharge. The sample and hold circuit at the output of the phase detector is commanded to sample and then hold the voltage at the output of the integrator. At the end of the sample period, A6A1U7 puts a LOGIC 1 on the bias line and latches it into A6A1U8. The active-high delayed-bias signal from the A6A1U8 is applied to the emitter of transistor Q5 via a resistor network to bias the transistor on. When A6A2Q5 is on, Q6 is biased off causing the voltage at the cathode of CR6 to be raised from approximately –1.2 volts to approximately +1.9 volts. This also causes the gate bias on transistor A6A2Q11 to change from –6 volts to +1.5 volts which turns Q11 on allowing the same current sink used in the ramp up phase to be used for the API1 current sink. The voltage change at CR6 biases the diode off and CR5 conducts current, which causes integrator capacitor C8 to discharge. The ramp down current source is the sum of the currents presented to the current summer made up of transistors A6A2Q16, A6A2Q17, and A6A2Q28. Transistors A6A2Q13 and A6A2Q14 form a 526 uA current source that provides a positive input to the current summing circuit. The API circuits provide the negative current inputs to the summer. The magnitude of the API currents are listed in table 4.

The integrator discharge rate is adjusted by the API circuit to maintain a constant sampled voltage from one reference cycle to the next. This is accomplished by subtracting the pulse-width modulated API currents from the fixed 526 uA current source, thereby creating a current source that can vary from about 500 uAmps to 526 uAmps. Without this, the integrator output voltage begins to rise in response to the accumulating phase error. Part of the API circuit is illustrated in figure 4. The API current sinks are turned on and off by the API control signals coming from A6A1U8. API control signals API1 through API5 yield a binary-coded decimal representation of the accumulated phase error.

The API currents are subtracted from the fixed current source when the corresponding API signals generated by A6A1U8 are logic 0. The rate of discharge of the integrator decreases as more of the API current sinks are enabled. As the content of the phase accumulator increases, the rate of discharge is increased by selectively turning off API current sinks. API1, API2, and API3 currents are generated by precision current sinks that consist of transistor array A6A2U4 and resistor network A6A2U5. The API4 and API5 current sinks are derived from the logic levels at the output of A6A1U8 and resistor network U5.

The current summing circuit comprised of Q16, Q17, and Q28 sums the fixed bias current (526 uA) with the five API current sinks to form the ramp-down current. Transistors Q28 and Q17 adjust the gate bias on Q17 to maintain a constant 5 volts between the source of Q17 and ground independent of the current flowing into the source. Transistor Q8 is a level shifter used to convert the CMOS logic level of API1 to a voltage which can be used to forward and reverse bias diode CR10. When API1 is a logic 1, the voltage at the cathode of CR10 is about 2.5 volts, causing CR10 to be forward biased, which turns on the API1 current sink. When API1 is a logic 0, the voltage at the cathode of CR10 is about 6.2 volts, causing CR10 to be reversed bias, which turns off the API1 current sink. Transistors Q9 and Q10 perform a similar function for API2 and API3.

Table 4. API Currents

API Designator	API Current
API1	25 uA
API2	2.5 uA
API3	250 nA
API4	25 nA
API5	2.5 nA

3.2.3 Sample and Hold

The sample and hold circuit consists of three differential amplifiers (Q18, Q19, and U7), two series switches (Q20, Q21), and a dual op amp. The three differential amplifiers provide the level shifting required to bias the series switches that actually perform the sample and hold function. The sample and hold function is controlled by the sample control line, which is described in table 5.

When the HOLD function is selected, transistor Q18 biases transistors U7A and U7D on, which causes a voltage of at least –4 volts to appear from the gate to source on JFET Q20 and Q21. The negative gate to source bias turns the JFET switches off so that any further voltage changes out of the integrator do not get stored on the hold capacitors C24 and C26. Op amp U9A is a high impedance unity gain buffer amplifier that is used to drive the loop filter without discharging hold capacitor C24 during the hold period. When the SAMPLE function is selected, transistor Q19 is biased on, causing transistor U7B and U7C to be biased on. Transistors U7D and U7A are biased off, causing the gate-to-source voltage on JFET switches Q20 and Q21 to be zero volts, which turns the switches on. Any voltage change on the integrator output since the last sample command are now stored in hold capacitors C24 and C26. The output of the sample and hold circuit drives the loop filter, and can be monitored at U9-1. The 100 kHz sideband null adjustment comprises C25, R72, and L1. The sample and hold circuit is sampled at a 100 kHz rate, which causes current to flow through the gate-to-source capacitance of JFET Q21 every time the FET is turned on and off. Capacitor C25 is driven from a voltage source, U7B that is equal and opposite to the JFET gate drive voltage source, U7A. When C25 is adjusted until its value is equal to the gate to source capacitance of Q21, the voltage that is introduced at the output of the sample and hold from the gate of Q21 is canceled by the voltage introduced through C25. Integrated circuit U8 is a precision 2.5 volt voltage reference that generates the bias supply for the differential amplifiers made from transistor array U7. The voltage at the cathode of U8 should be –9.5 volts.

Table 5. Sample Control Line Functions

Function	Sample Control	Q18 Base Voltage	Q18 State	Q19 State
HOLD	LOGIC 0	-.4 VOLTS	ON	OFF
SAMPLE	LOGIC 1	+2 VOLTS	OFF	ON

3.2.4 Loop Filter

The output of the sample and hold drives a roofing filter and loop filter, which low pass filters the VCO control voltage and provides the proper loop compensation so that the phase lock loop, PLL, has a second order response. Inductors L8 and L9, with capacitors C52 through C56, form a fifth order elliptic low pass roofing filter with a cutoff frequency of 155 kHz. The actual compensating loop filter consists of R86, R87, C49, R85, CR14, CR15, C48, and R83. During large voltage changes, greater than ±0.4 volts, diodes CR14 and CR15 conduct allowing the VCO control voltage to change faster, causing the synthesizer to change frequency faster. Transistor Q23 is used to limit the maximum VCO control voltage to about +6.5 volts. This ensures that the varactor diodes in the VCO are never forward biased.

3.2.5 Voltage Controlled Oscillator (VCO)

The VCO is a varactor-tuned Colpitts oscillator that uses JFET Q1 as the oscillator transistor (as shown in figure 5). Varactors CR3 through CR10 form the variable capacitor portion of the oscillator's tank, while T1 provides the inductive element. The cathodes of varactor diodes CR3 through CR10 are referenced to a 10-volt supply to keep them reversed biased over the normal range of the VCO control voltage, approximately (–1 volt to +5 volts). The oscillator covers the frequency range of 82.1000 MHz to 140.4999 MHz in two different bands. The low band is 82.1000 MHz to 110.4999 MHz, and the high band is 110.5000 MHz to 140.4999 MHz. The VCO BANDSWITCH signal is used to select the operating band for the VCO. The low band is selected when –12 volts is present on the VCO BANDSWITCH line, and the high band is selected when +5 volts is present on the VCO

BANDSWITCH line. The +5 volts on the control line forward biases diode CR1 to effectively parallel the primary and secondary inductances of transformer T1. The inductance of the tank circuit is decreased by a factor of two and the oscillator's output frequency is increased by a factor of two. A typical VCO control voltage verses output frequency curve is shown in figure 5. The output of the VCO is buffered by a cascode amplifier consisting of JFETs Q2 and Q3. The cascode amplifier provides isolation between the VCO and it's load so that changing load conditions do not influence the VCO's operating frequency. The VCO output level is +7 dBm +4dB/-2dB at connector W1J1 and is attenuated by 17 dB by R113 and R112 for use as a prescaler output. The attenuated signal is amplified by hybrid amplifier U13, which has a power gain of +14 dB. This yields a prescaler output drive level of +4 dBm.

3.2.6 Divide-by-N.F. Circuit

The elements of the divide-by-N.F. circuit which reside on the A6A1 Reference Assembly include dual-modulus prescaler U15 (divide by 20/21), programmable divider U8, and LSI fractional N logic array U7 (see figure 6). The divide-by-N.F. circuit can be separated into the divide-by-N. and the divide-by-.F sections of the circuit. The divide-by-.F output is processed in the U7 fractional N logic array to keep track of the fractional component in the phase accumulator, and to generate the timing for the VCO pulse-swallow command. The N programmable dividers are loaded with a 17-bit binary word corresponding to the numeric information from the first four significant digits of the first LO frequency. The .F dividers are loaded with numeric information from the last six significant digits of the first LO frequency. The first LO frequency is equal to the displayed radio operating frequency, plus the first IF frequency (80.5 MHz). The transceiver operates over the RF frequency range of 1.6 MHz to 59.9999999 MHz. This makes the range of the first LO from 82.1000000 to 140.4999999 MHz. The first four significant digits of the first LO range from 082.1 to 140.4 for the divide-by-N. The remaining digits of 000000 to 999999 are used for the divide-by-.F.

3.2.6.1 Divide-by-N

Figure 6 shows the essential components of the divide-by-N circuit. Timing relations of the individual events are illustrated in figure 7. In the following paragraphs, the first LO digits will be referred to as follows:

Digit Designator	A	B	C	D	E	F	G	H	I	J	
Minimum First LO frequency	0	8	2	1	0	0	0	0	0	0	MHz
Maximum First LO frequency	1	4	0	4	9	9	9	9	9	9	MHz

The first four digits of the LO frequency ABCD are numerically manipulated and used in the divide-by-N circuit and the remaining digits EFGHIJ are used in the fractional divide-by-.F circuit. Operation of the divide-by-N circuit is the same with or without a fractional component of the LO frequency present (.F).

The programmable divide-by-N circuit uses a dual-modulus counter scheme that utilizes two programmable counters, divide-by-A counter and divide-by-N counter, and a dual-modulus prescaler, U15, that can divide by 20 or 21, depending on the state of the modulus control line. The divide-by-A counter can be loaded with any number between 0 and 19, and the divide-by-N counter can be loaded with any number between 41 and 70. During the division cycle, the preloaded counters both count down to 0. When this occurs, the input VCO frequency sample is divided by a number that yields a divider output frequency of 100 kHz.

At the start of the division cycle, the modulus control line is logic 0 and the dual-modulus prescaler U15 divides by 21. So, for every 21 VCO input pulses, there is one dual-modulus output pulse. Each dual-modulus output pulse decrements the preloaded numbers in the N and A programmable counters by one. This continues until the A counter reaches zero, which causes the modulus control line to the dual-modulus prescaler to change state from logic 0 to logic 1. This causes the dual-modulus prescaler to divide by 20 instead of 21. The VCO division continues with each group of 20 VCO input pulses yielding one prescaler output pulse which decrements the programmable N counter. When the programmable divide-by-N counter reaches zero, the preloaded division of the VCO input has occurred. Before a new cycle begins, the A and N counters are preloaded with the stored A and N register contents. A new cycle is started and the entire process is repeated.

This following example is included to clarify the operation of the divide-by-N circuit. The following are parameters for this example:

- First LO frequency: 90.9000000 MHz

	Reference									
A	B	C	D	E	F	G	H	I	J	
0	9	0	9	0	0	0	0	0	0	MHz

ABCD is the divide-by-N portion, that is, divide-by-0909. The divide-by-.F portion, EFGHIJ is 000000, so no fractional division is required to yield the desired 100 kHz output. The divide by A and N registers must be loaded with the proper numbers to produce the desired divide by 909. The main controller microprocessor on the A4 Signal Processor Assembly divides the first four digits, ABCD, of the first LO frequency, 0909, by 20; yielding a quotient of 45 and a remainder of 9. The divide-by-N register will be loaded with the binary representation of the quotient, 45, and the divide by A register will be loaded with the binary representation of the remainder, 9, via the serial control bus for the main synthesizer. The serial control data is clocked into serial to parallel registers and is latched into the divide by A and N registers within U8 on the rising edge of the main synthesizer strobe.

The programmable divide by A and N counters U7 are preloaded from the A and N registers, between the last divide-by-N output pulse, divide-by-N counter equal to 0, and the next VCO pulse. The remainder 9 is loaded into the A counter, and the quotient 45 is loaded into the N counter.

The dual-modulus prescaler U15 is commanded to divide by 21 because the A counter is not zero. After the first 21 input VCO pulses, an output pulse from the prescaler decrements the A counter from 9 to 8, and the N counter from 45 to 44. After another 168 input VCO pulses, the A counter reaches zero and the N counter reaches 36. There are a total of 189 input VCO pulses up to this point in the cycle.

When the A divider reaches zero, the modulus control line changes from a logic 0 to logic 1, causing the dual-modulus prescaler to divide by 20, instead of 21.

After another 20 input VCO pulses, the prescaler produces another output pulse and the N counter decrements from 36 to 35. The N counter continues to decrement by one for each 20 input VCO pulses until the N counter is decremented to zero, which requires an additional 700 VCO pulses.

When the U8 N counter reaches zero, a CYCLE START pulse is produced at the "cycle_st_out" line of U8, and is sent to U7. This pulse is used to preload the divide-by-N counter. The next rising edge from the prescaler loads the U8 divide by A counter. The count sequence then repeats, producing a CYCLE START pulse for every 909 input VCO pulses (189 for the A counter countdown, plus 720 for the rest of the N counter countdown).

Although the CYCLE START output operates at 100 kHz, it is not used as the 100-kHz VCO/N signal used to drive the phase detector. The CYCLE START pulse initiates sequencing in fractional N logic array U7 to generate the API, bias, swallow, sample, and API Latch Clock signals. The 100-kHz VCO divide-by-N signal is derived by processing the bias output of U7. It is converted into a fast-rising pulse by a latch contained inside programmable gate array U8. This signal is called VCO/N.

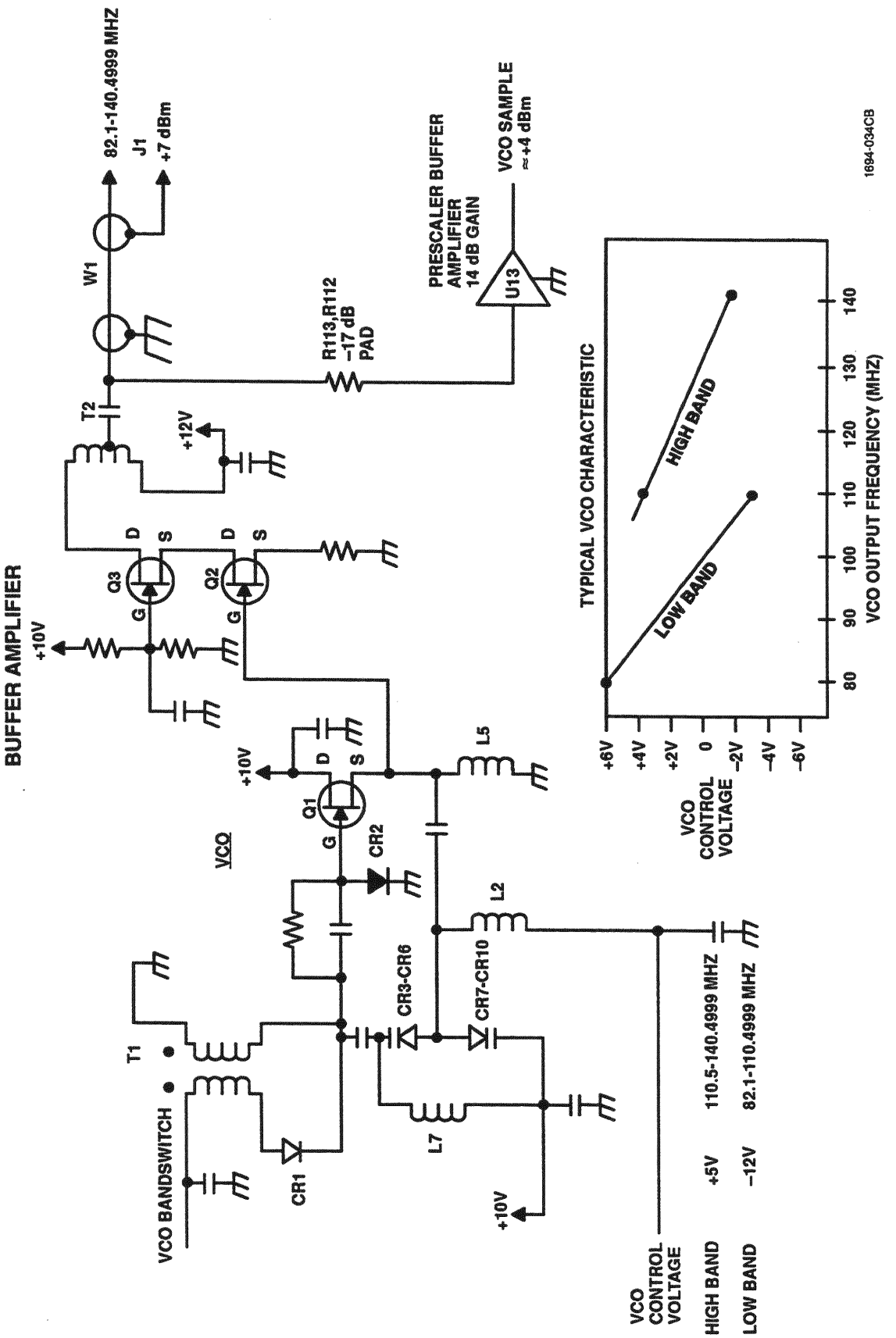


Figure 5. VCO Simplified Schematic Diagram

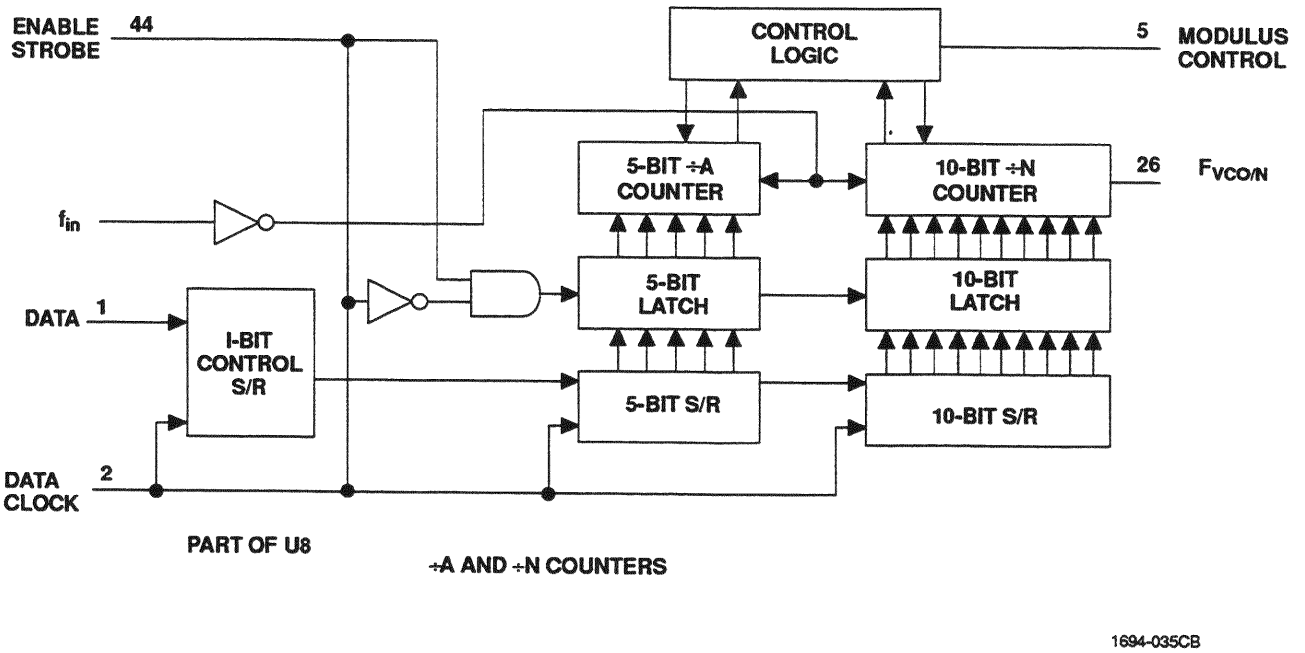


Figure 6. Divide-by-N Circuit

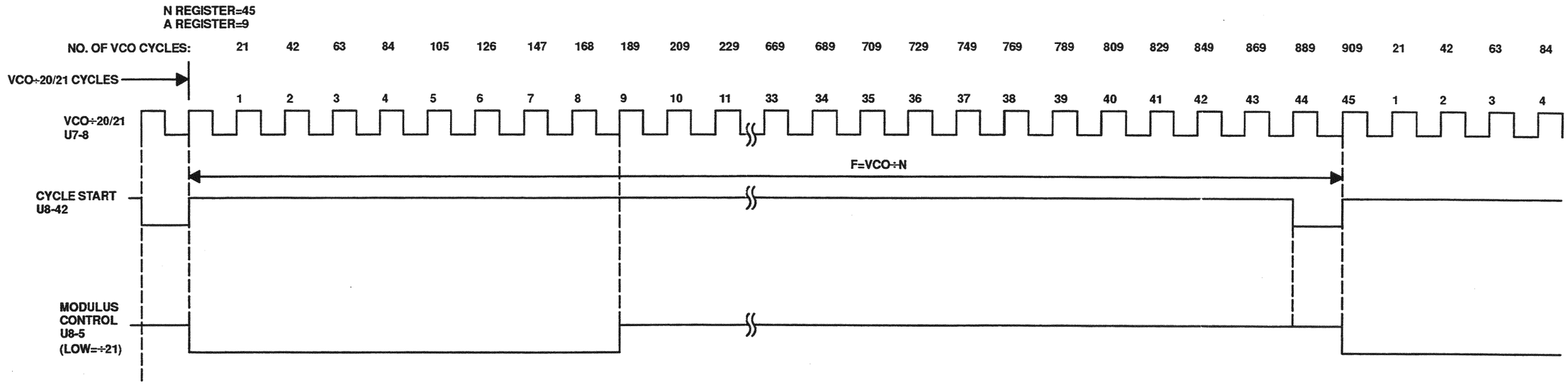


Figure 7. Divide-by-N Timing Sequence

3.2.6.2 Divide-by-.F (Fractional) Counter Operation

The fractional portion of the divide-by-N.F. circuit deletes (swallows) input VCO pulses. This has the effect of removing one cycle (360 degrees) of phase accumulation, as described in paragraph A6 3.1.2. The timing of the events in a typical divide-by-N.F. cycle is illustrated in figure 8. The divide-by-N circuit is not affected by the action of the divide-by-N.F. circuit. The circuits operate independently, except when a pulse is swallowed and the count is increased by one. LSI integrated circuit U7 internally processes almost all divide-by-N.F. functions. Since a discussion of the inner workings of U7 is beyond the scope of this manual, only the divide-by-.F outputs are considered: API control, bias, and swallow control.

The operation of API control lines and delayed bias control are described in subsection 3.2.2. Swallow control is interactive with the dual-modulus divider used with the divide-by-N circuit. The dual-modulus divider operates in the divide-by-21 mode until the preloaded A divider underflows by counting down to zero. The dual-modulus divider is then programmed to divide by 20 for the rest of the divide-by-N cycle. The divide-by-.F pulse swallow is made to occur by changing the dual-modulus divider from the divide-by-20 mode back to the divide-by-21 mode for one VCO pulse, then back again to the divide-by-20 mode. This results in a prescaler output pulse to decrement the N divider after 21 VCO pulses instead of 20 VCO pulses. This causes one VCO pulse to be swallowed.

The swallow command is generated during the first ten cycles of the VCO divide by 20 or 21 output. This means that a swallow command may occur during the period that the divide by A counter is counting down from its preload and the prescaler is dividing by 21. If a swallow command occurs during this period or occurs at the same time that the divide by A counter decrements to 0, the swallow command must be stored until it can be used, any time the prescaler is in the divide by 20 mode. This is accomplished by storing the swallow command in the swallow-control flip flop that is part of U8.

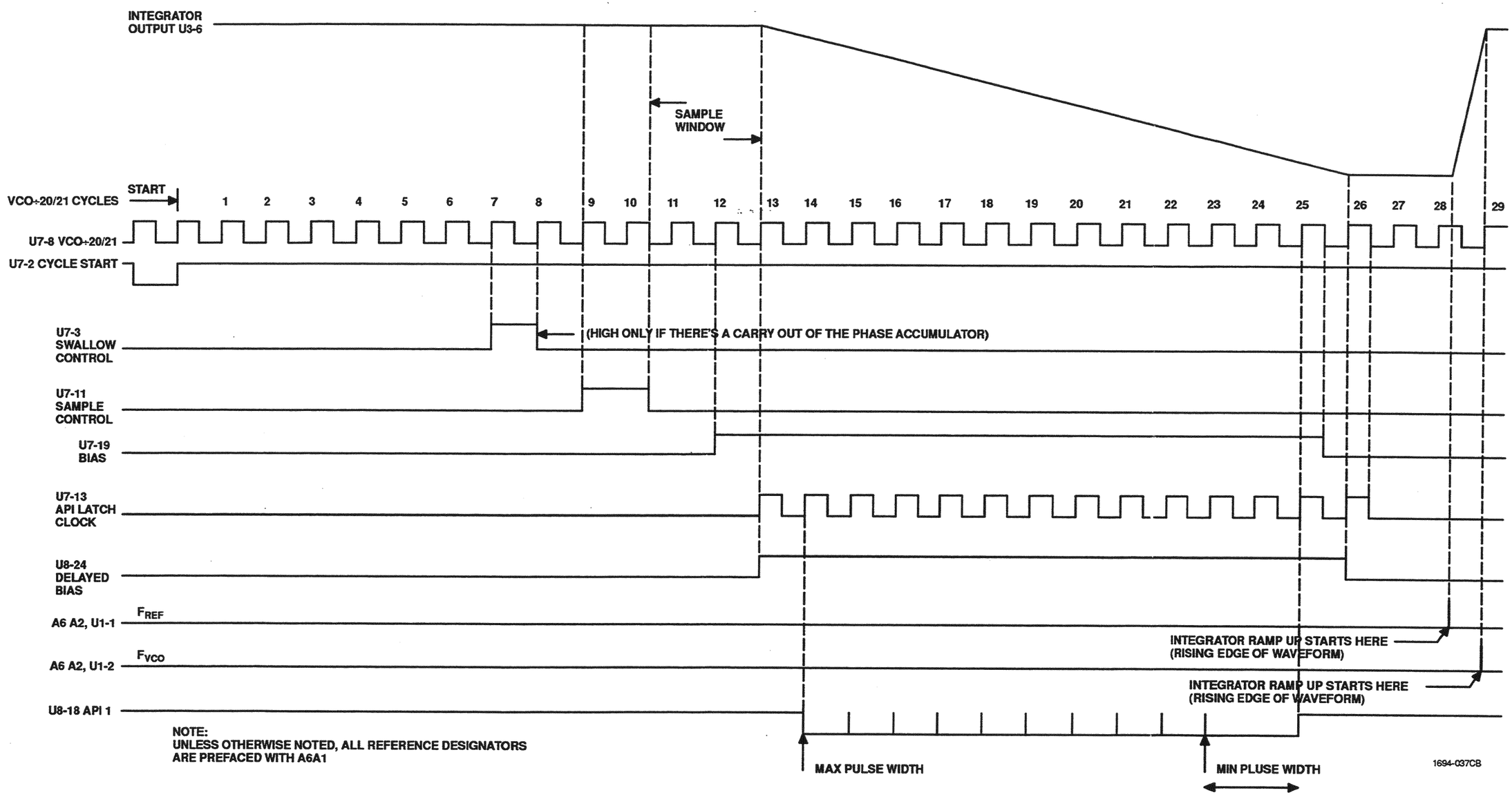


Figure 8. Typical Fractional Divide-by-N.F. Timing Sequence

4. REFERENCE GENERATOR TECHNICAL DESCRIPTION

Figure 1 is a block diagram of the Reference Generator Assembly. In addition to generating many of the signals required for the first LO synthesizer, the assembly also generates the following signals that are needed by the transceiver:

- DTCXO Digital Temperature-Characterized Crystal Oscillator
- 9.5 MHz third local oscillator
- 71 MHz second local oscillator
- Combined Synthesizer Lock Detect
- 100 kHz Reference Clock for Main Synthesizer
- 1.2 MHz clock
- 9.6 MHz microprocessor clock
- 36.16 MHz microprocessor clock
- /Power on reset

4.1 9.6-MHz Digitally Temperature-Characterized Crystal Oscillator

The 9.6-MHz Digitally Temperature-Characterized Crystal Oscillator, (DTCXO U1), is a self-contained crystal oscillator and temperature sensor. The temperature sensor produces a voltage that is proportional to the oscillator temperature, as shown in figure 9. The output frequency of the oscillator changes slightly with respect to temperature. A typical oscillator's frequency vs. temperature voltage curve is shown in figure 10. This frequency change is not desirable, as this oscillator is used as the frequency reference in the transceiver. Each oscillator has a unique frequency vs. temperature characteristic, which is measured and stored in EEPROM U2. The oscillator frequency error is subtracted from the main synthesizer frequency by the main control microprocessor on the Signal Processor Assembly A4. After the DTCXO frequency has been corrected by the main control processor, the frequency accuracy of the transceiver is less than or equal to ±1 PPM over the temperature range of –40°C to +70°C. The oscillator frequency output is a CMOS compatible squarewave. Initial frequency calibration of the DTCXO is accomplished by adjusting variable resistor R5.

4.2 9.5-MHz Third Local Oscillator

The 9.5 MHz local oscillator is a phase locked loop (PLL) that is phase locked to the 9.6 MHz DTCXO. The PLL consists of a MC145157 PLL integrated circuit U13, charge pump phase detector/loop filter, and voltage controlled oscillator (VCO) as shown in figure 11. The 9.5 MHz VCO is a FET Colpitts oscillator stage (Q5) and buffer amplifier (Q6) whose frequency changes as the capacitance of the varactor diodes changes in response to changes in VCO control voltage. A VCO control voltage shift from 3.0 V to 11.0 V produces a change in VCO frequency from 8.6 MHz to 10.6 MHz, see figure 12. Under normal receive operation, when the third LO is set to 9.470 MHz (SSB and Hopping RX), the VCO control voltage is approximately 6.5 volts.

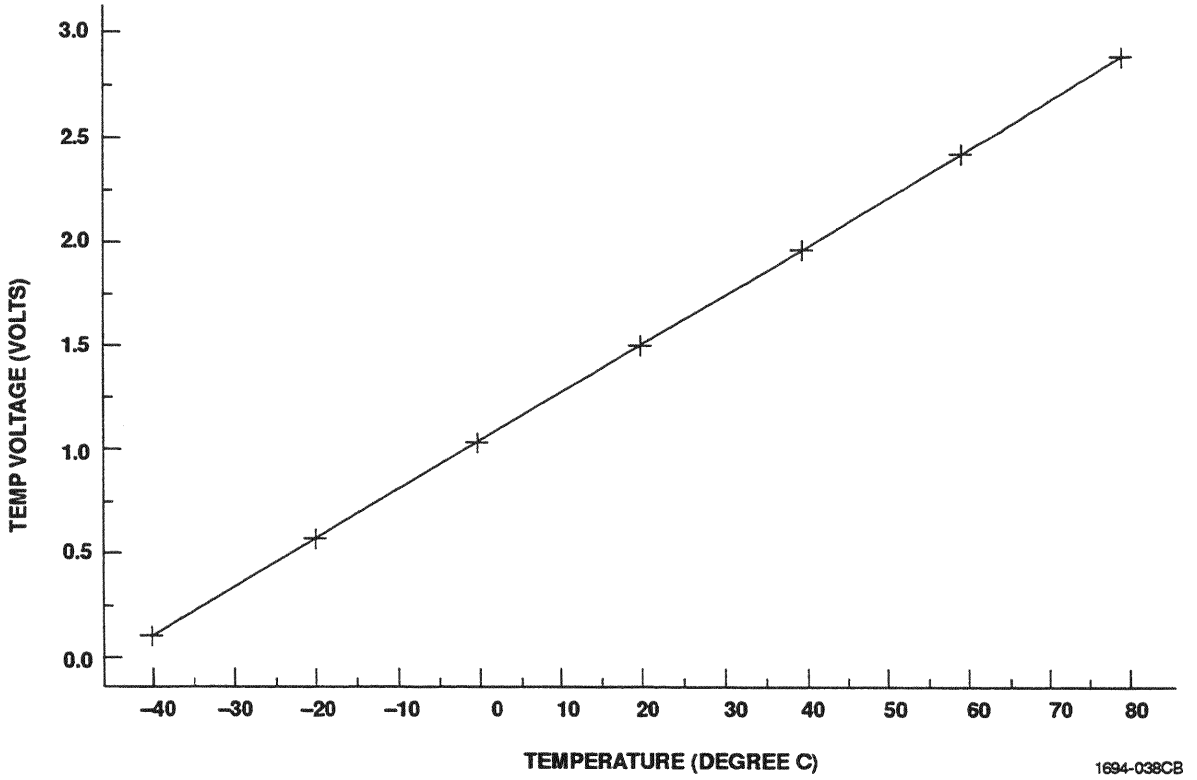


Figure 9. DTCXO Temperature vs. Temperature Voltage

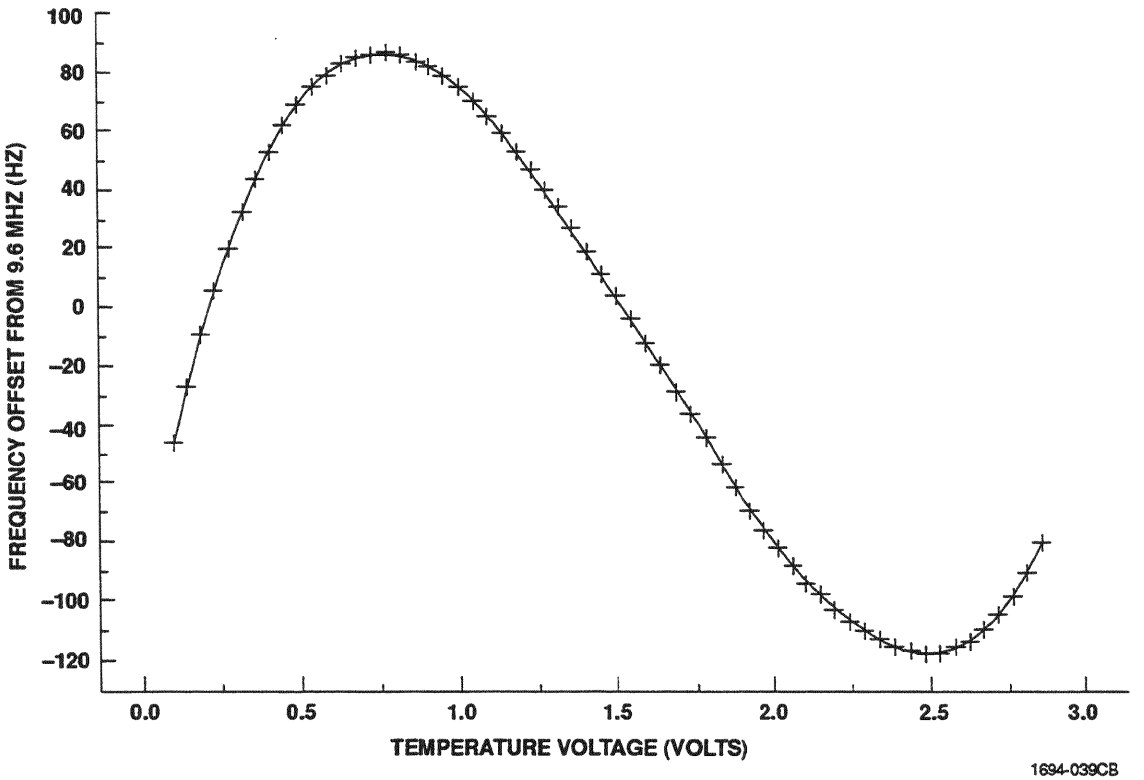
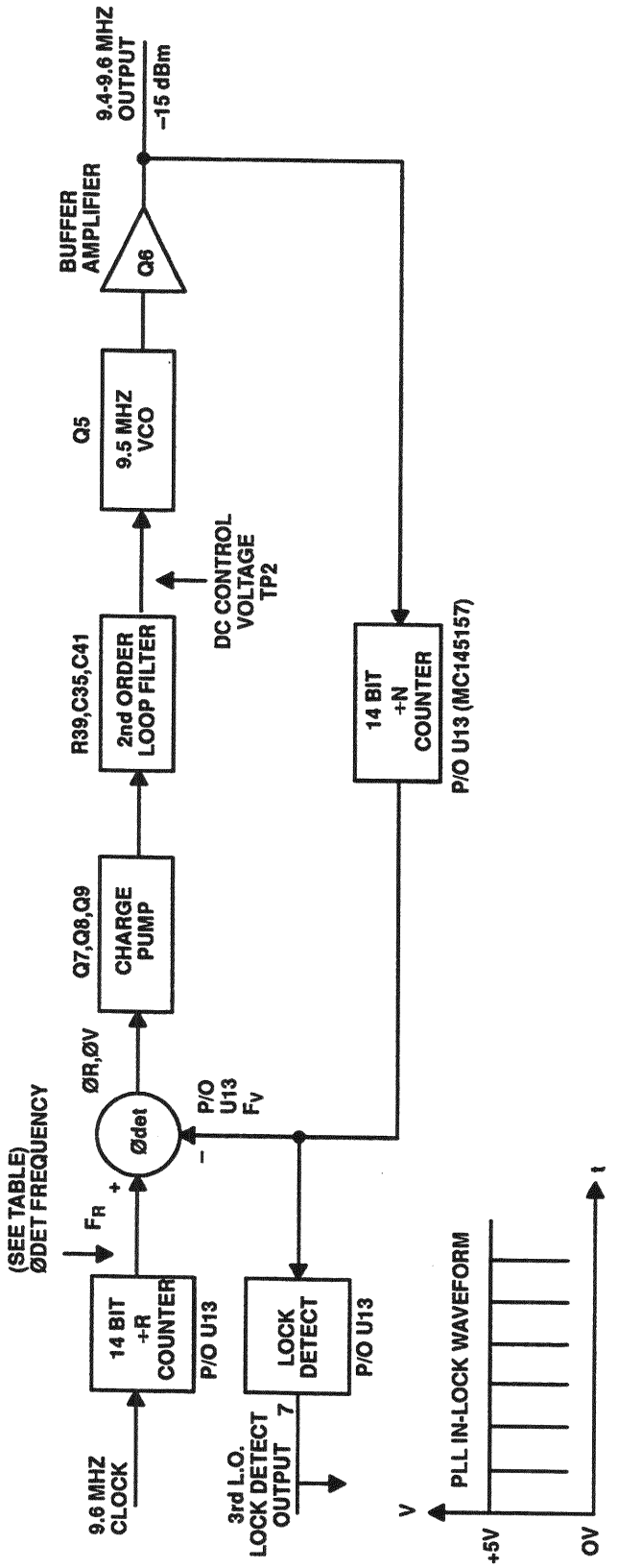


Figure 10. DTCXO Temperature Voltage vs. Frequency



OUTPUT FREQUENCY	+N	+R	Ødet FREQUENCY	TRANSCEIVER STATE
9.46520 MHZ	351	356	26.96 KHZ	MODEM ON RX
9.4700 MHZ	510	517	18.50 KHZ	SSB/HOPPING RX
9.5060 MHZ	708	715	13.40 KHZ	SSB/HOPPING TX
9.4928 MHZ	797	806	11.91 KHZ	MODEM ON TX
9.9550 MHZ	561	541	17.75 KHZ	FM RX
9.4760 MHZ	376	379	25.33 KHZ	FM TX

Figure 11. 9.5 MHz Third LO PLL Block Diagram

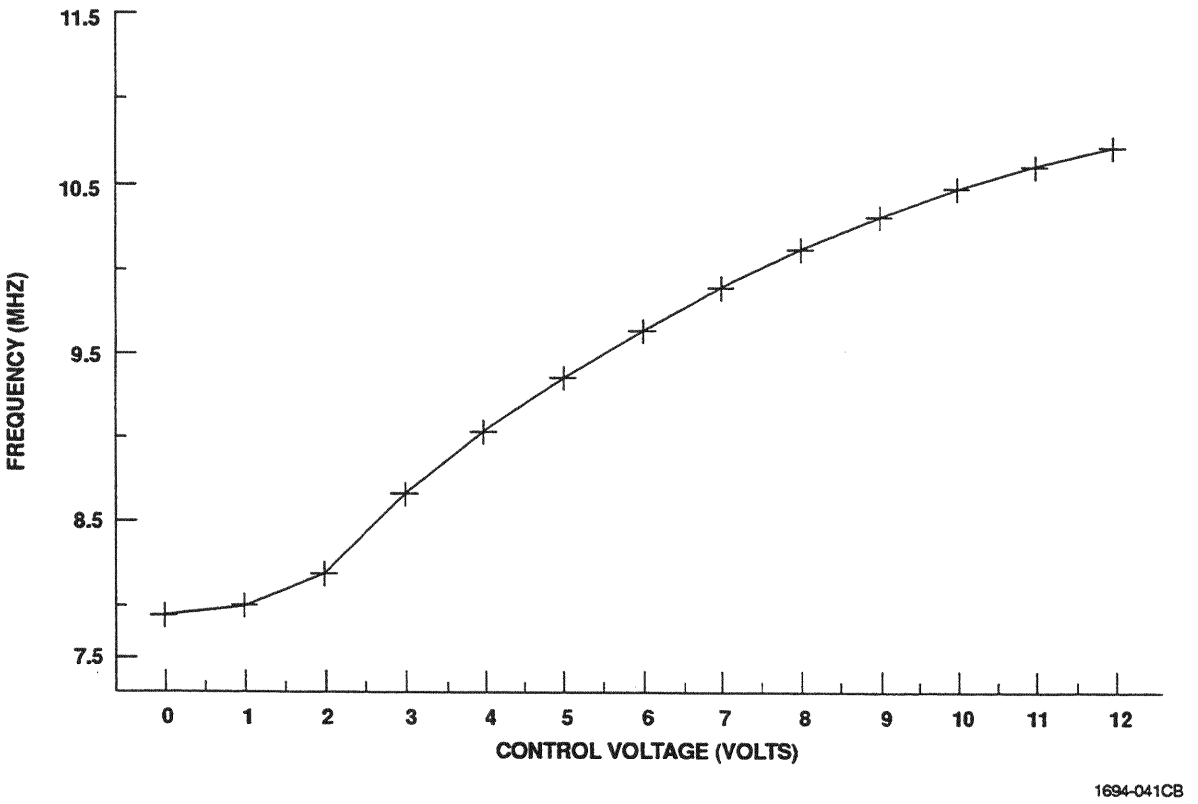


Figure 12. 9.5 MHz VCO Frequency vs. Control Voltage

4.2.1 Phase-Locked Loop (PLL) Operation

The PLL is based on a Motorola MC145157P phase-locked loop IC. This contains the following sub-circuits:

- Reference divider (R)
- VCO divider (N)
- Lock detector
- Phase/Frequency detector

The PLL IC is loaded with serial data (clock, data, and enable) from the main control microprocessor on the signal processor Assembly that sets up the internal divider registers to one of the values shown in figure 11. When the VCO output is 9.4700 MHz, the divide-by-N counter is dividing by 510, which produces a 18.50 kHz signal at the F_V input to the phase/frequency detector. This signal can be measured on the F_V output, pin 3 of U13. The 9.6 MHz clock signal is divided by the number contained in the R counter (517 in this example) to produce a 18.50 kHz phase/frequency detector reference signal, F_T. This signal can be measured on the F_T output, pin 13 of U13. These two signals are compared for equal phase and frequency. When this condition is met, the two phase-detector output signals (ΦR and ΦV) are held high, causing the charge pump circuit (Q7, Q8, and Q9) to stop charging or discharging the loop filter. The voltage at the output of the loop filter is consequently held constant.

If the VCO output frequency falls below 9.4700 MHz, the VCO feedback signal after the divide-by-N counter, F_V, becomes lower than the desired phase detector reference frequency of 18.50 kHz. When F_V is is less than F_T, the ΦR output of the phase detector goes low and the ΦV output remains high, causing the charge pump to inject current into the loop filter which ramps the VCO control voltage up to a higher level. This causes the VCO frequency to increase until it again reaches 9.4700 MHz.

If the VCO output frequency rises above 9.4700 MHz, the VCO feedback signal F_V is higher than the reference frequency F_T, which is at 18.5 kHz. The phase/frequency detector responds to this condition setting the ΦV output low and the ΦR output high which causes the charge pump to take current out of the loop filter. The VCO control voltage ramps down to a lower level and the VCO frequency decreases until it again reaches 9.4700 MHz.

The PLL IC U13 produces a lock-detect signal which is used during Built-In Test (BIT) to determine if the third LO PLL is in lock. The IN-Lock condition is indicated by a logic high (+5 V) on the lock-detect signal line (U13-7), see waveform shown in figure 11. If this signal toggles low for more than an instant, the third LO synthesizer is out-of-lock.

4.2.2 Loop Filter

The second-order loop filter consists of a charge pump circuit and phase shift network/integrator. The charge pump, Q7, Q8, and Q9, either sinks or sources a precision current into the phase shift network, R39, C35, and C41. When the ΦR input to the charge pump is logic low and the ΦV input is logic high, transistor Q7 and Q9 are turned on causing a precision current of 360 uAmps to be sourced into the integrator network which causes the voltage across the integrator to ramp up. When the ΦR input to the charge pump is logic high and the ΦV input is logic low, transistor Q7 and Q9 are turned off and transistor Q8 is turned on causing a precision current of 360 uAmps to be sinked out of the integrator network, which causes the voltage across the integrator to ramp down. When both the ΦR and ΦV control lines are logic high, transistors Q7, Q8, and Q9 are turned off and no current is sinked or sourced into the integrator network, which causes the integrator voltage to remain constant.

4.3 71 MHz Second Local Oscillator

The 71 MHz second local oscillator is a phase locked loop (PLL) that is phase locked to the 9.6 MHz DTCXO. The PLL consists of a MC145158 PLL integrated circuit U9, phase detector/loop filter, and voltage controlled

crystal oscillator (VCXO), as shown in figure 12. The 71 MHz VCXO is a bipolar Colpitts oscillator stage (Q1) whose frequency changes as the capacitance of the varactor diodes changes in response to changes in VCO control voltage. A VCO control voltage shift from 3.0 V to 11.0 V produces a change in VCO frequency from 70.988 MHz to 71.022 MHz (see figure 13). Under normal operation when the second LO is set to 71.0 MHz, the VCO control voltage is approximately 6.5 volts. This synthesizer is phase modulated with processed audio to produce FM modulation during FM transmit.

4.3.1 Phase-Locked Loop (PLL) Operation

The PLL is based on a Motorola MC145158P phase-locked loop IC and MC12019 divide by 20/21 prescaler. The MC145158 contains the following sub-circuits:

- Reference divider (R)
- VCO divider (N) and (A) with prescaler modulus control
- Lock detector
- Phase/Frequency detector

The PLL IC is loaded with serial data (clock, data, and enable) from the main control microprocessor on the Signal Processor Assembly via the third LO PLL integrated circuit. This data sets up the internal divider registers to the values shown in figure 13.

When the desired VCO output is 71.0 MHz, the divide-by-N counter is set to 17 and the divide by A counter is set to 15, which produces a 200 kHz signal at the F_V input to the phase/frequency detector. This signal can be measured on the F_V output, pin 3 of U9. The reference input to the phase/frequency detector F_T is derived by dividing the 9.6 MHz DTCXO clock by 8 with integrated circuits U5A and U6 to yield a 1.2 MHz clock that is further divided by 6 with the divide by R counter contained in U9, which produces a 200 kHz reference signal. This signal can be measured on the F_T output, pin 13 of U9. These two signals are compared for equal phase and frequency by the phase/frequency detector. When this condition is met, the two phase-detector output signals (ΦR and ΦV) are held high, causing the output voltage of the loop filter to remain constant.

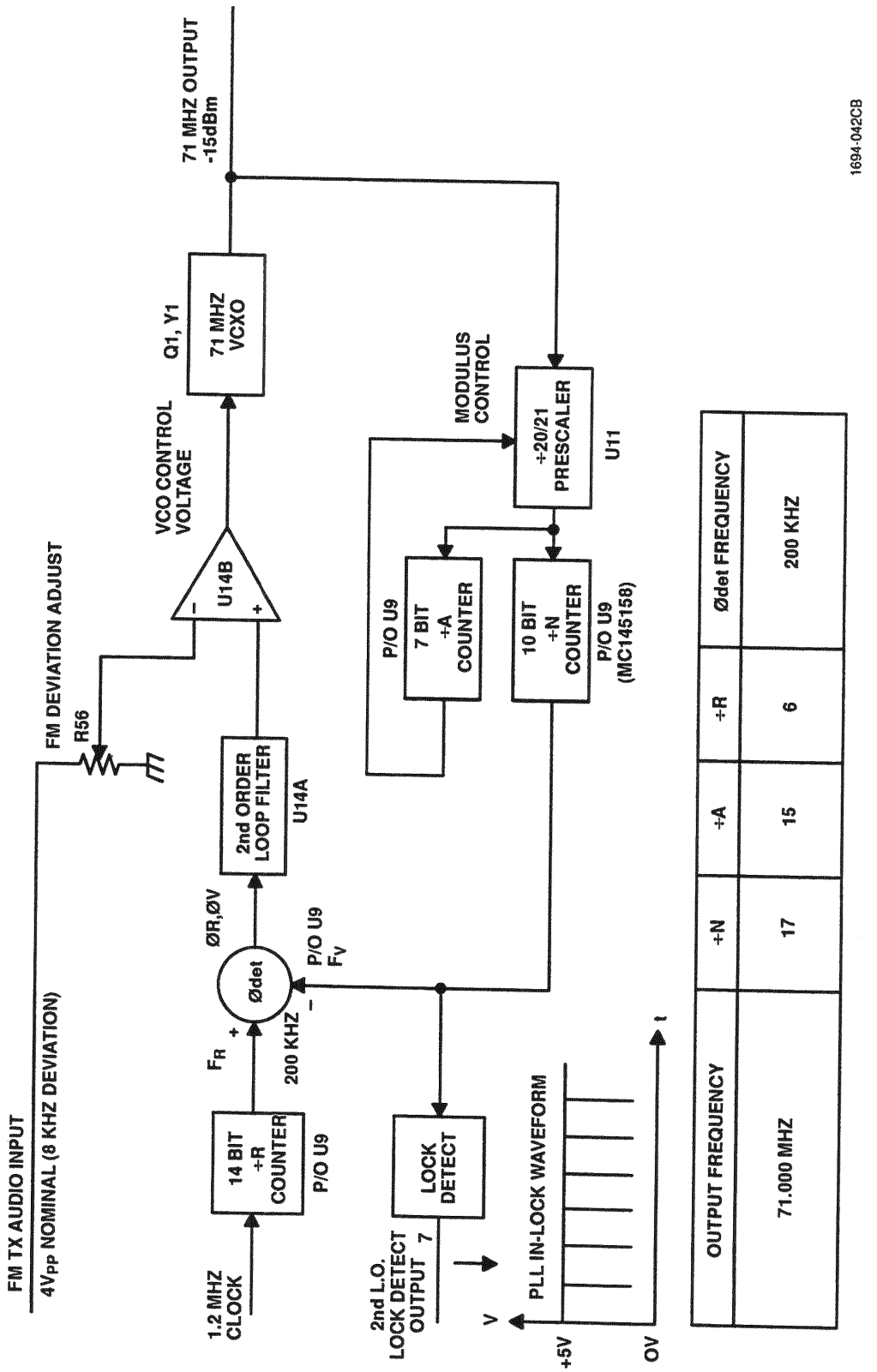
If the VCO output frequency falls below 71.0 MHz, the VCO feedback signal, F_V, becomes lower than the phase detector reference frequency of 200 kHz. When F_V is is less than F_T, the ΦR output of the phase detector goes low and the ΦV output remains high, causing the loop filter voltage to increase and the VCO frequency to increase until it again reaches 71.0 MHz.

If the VCO output frequency rises above 71.0 MHz, the VCO feedback signal F_V is higher than the reference frequency F_T, which is at 200 kHz. The phase/frequency detector responds to this condition setting the ΦV output low and the ΦR output high, which causes the loop filter output voltage to decrease and the VCO frequency decreases until it again reaches 71.0 MHz.

The PLL IC U9 produces a lock-detect signal which is used during Built-In Test (BIT) to determine if the second LO PLL is in lock. The IN-Lock condition is indicated by a logic high (+5 V) on the lock-detect signal line (U9-7), (see waveform shown in figure 14). If this signal toggles low for more than an instant, the second LO synthesizer is out-of-lock.

4.3.2 Loop Filter

Second-order loop filter U9 is made from an op amp connected as a difference amplifier/integrator. Phase frequency detector outputs ΦR and ΦV charge or discharge capacitors C49 and C51, based on the amount of phase or frequency error in the control loop. The output of the loop filter drives a summing amplifier, U14B, that sums processed FM TX audio into the PLL. The processed audio modulates the PLL outside the loop's bandwidth so that the FM modulation on the VCO is not removed by the PLL. Resistor R56 is used to adjust the FM deviation of the modulator. The processed audio is only present when the transceiver is in FM mode.



OUTPUT FREQUENCY	+N	+A	+R	Ødet FREQUENCY
71.000 MHZ	17	15	6	200 KHZ

Figure 13. 71 MHz Second LO PLL Block Diagram

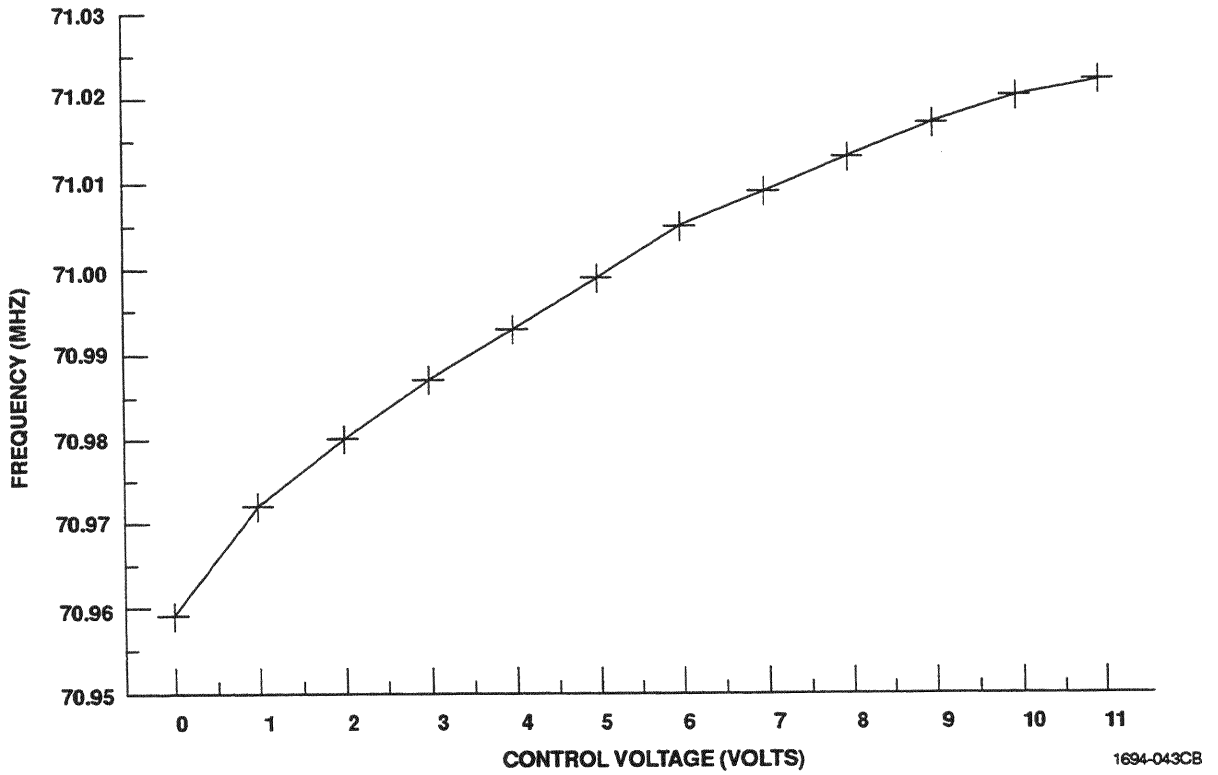


Figure 14. Typical 71 MHz VCXO Frequency vs. Control Voltage

4.4 Combined Synthesizer Lock Detect

The individual synthesizer lock detect signals are combined into a single lock detect line that is used by Built-In-Test, BIT, to determine if all three synthesizers are in lock. Transistor Q2 combines the individual lock detect signal so that when all the synthesizers are in lock, the combined lock detect signal on connector P4-12 is a logic low. If any one of the three synthesizers is unlocked, the combined lock detect signal is a logic high.

4.5 100-kHz Reference Clock for Main Synthesizer

The 100-kHz reference clock for the main synthesizer is generated from the DTCXO 9.6-MHz clock that is divided by 4 with binary counter U5A ,which produces a 2.4-MHz clock. This clock is divided by 12 to yield a 200-kHz clock by programmable binary counter U6. The 200-kHz clock is divided by 2 with binary counter U5B to achieve the desired 100-kHz clock.

4.6 1.2-MHz Clock

The 1.2-MHz clock at connector P4, pin 8 is created by dividing the 9.6-MHz output of the DTCXO by eight in U5A.

4.7 9.6-MHz Microprocessor Clock

The 9.6-MHz microprocessor clock is generated by buffering the DTCXO output with a HCMOS inverter U12.

4.8 36.16-MHz Microprocessor Clock

The 36.16 MHz microprocessor clock is generated by a third overtone crystal oscillator, U12A and Y2, that is, buffered by an inverter gate U12B, The clock has a 50 percent duty cycle.

4.9 Power On Reset (POR)

The power on reset for most of the microprocessors in the transceiver is generated with reset IC U4. When the +5V line first reaches 4.6 volts, the /POR output P4-3 remains at logic 0 for an additional 50 milliseconds before switching to logic high. This allows all the microprocessor clocks to start and gives the +5V line time to stabilize before the microprocessors are permitted to execute their program

5. TESTING AND ALIGNMENT

In order to accurately produce a VCO output with a resolution of 0.1 Hz, the A6 Reference Generator/Synthesizer Assembly contains precision circuits. Some of these circuits have extremely small currents and voltages. Due to the sensitive nature of these circuits, the A6 Reference Generator/Synthesizer Assembly will not perform correctly on an extender card and requires a special test fixture for depot level alignment. Thus, a test and alignment procedure is beyond the scope of this manual.

6. BITE FAULTS AND TROUBLESHOOTING

Table 6 is a list of the self-test faults reported by the A6 Reference Generator/Synthesizer Assembly. The tests and faults are described in the following paragraphs.

Table 6. Reference Generator/Synthesizer Assembly Self-Test Faults

Code	Fault
12	Combined lock detect fault
20	Serial EEPROM data read fault

6.1 Fault 12 – Combined Lock Detect Fault

This test verifies that the A6 Reference Generator/Synthesizer Assembly locks on the frequencies at each extreme of its operating range. This test is performed after the serial data fault test and assumes that the EEPROM data is correct. Refer to the troubleshooting flowchart in figure 15 and follow the procedure outlined in the following subsection.

6.1.1 Isolate Fault to Assembly Level

Replace the A6 Assembly with a known good assembly to locate this fault, as outlined in subsection 1. If the fault still occurs with the known good A6 assembly, the fault is most likely on the A4 or A11 assembly. Perform the same module replacement technique described above with a known good A4 Assembly. Trace the /Lock Detect line from the A6 Assembly, through the A11 Interconnect Assembly, to the A4 Signal Processor Assembly. Check the lines for shorts and opens. If the fault does exist on the A4 Assembly, verify the value and correct operation of resistor A4R14, and verify power to, and correct input/output activity of A4U19.

If the fault is located on the A6 Assembly, the following procedure will further isolate the problem.

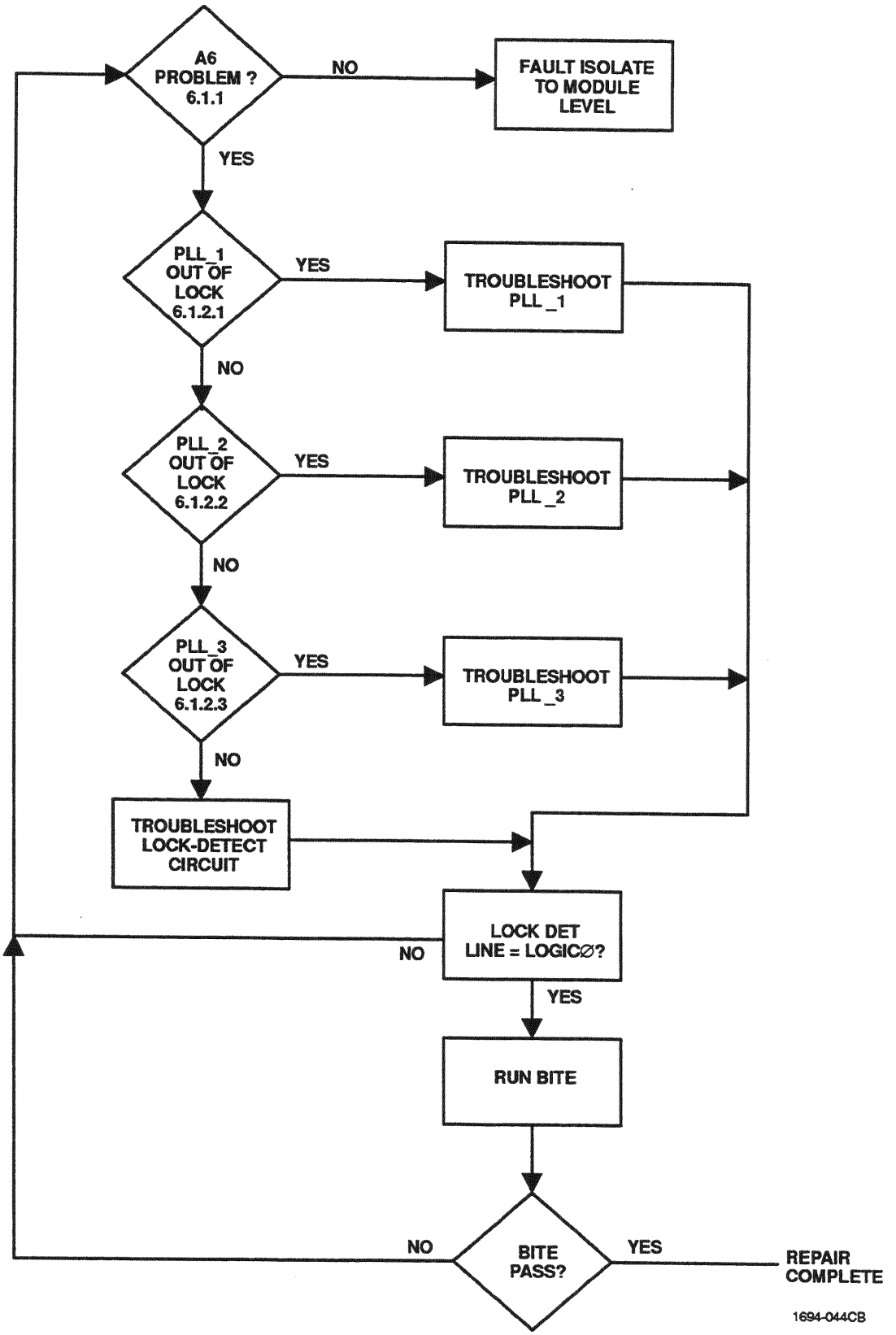


Figure 15. Fault 12 – Troubleshooting Flowchart

6.1.2 A6 Assembly is Out of Lock

Use an oscilloscope probe to verify overall lock status (logic 0) at pin 12 of connector P4, or at the test point on the extender card. Verify lock status with the R/T set at the frequency extremes of 1.6 MHz and 59.9 MHz. The assembly will only be locked if all three of the local oscillators and their appropriate PLLs are locked. If overall lock status is not achieved, verify the lock status of the individual PLL lines, as listed in the subsections below. Follow the provided troubleshooting guidelines for any of the PLLs that are unlocked.

6.1.2.1 First LO – Out of Lock

Verify that the first LO (PLL1_LD) is locked, as indicated by a logic 0 at pin 17 of connector A6A2J1 and a logic 1 at pin 3 of A6A2U1. If the lock status at these two locations are not of opposite logic state, there is a problem with inverter Q22 or its supporting circuitry. If PLL1_LD is unlocked, there is a problem either with the VCO or the support/control circuitry.

a. With an oscilloscope probe, verify the presence of the 100 kHz frequency reference at pin 1 of A6A2U1. If the reference signal is not present, verify the voltage supplies to, and proper input/output activity of, A6A1U1, U5, U6, and U12.

b. Monitor pin 2 of A6A2U1 for a similar 100 kHz signal. If this signal is not present, check the voltage supplied to pins 3, 14, 25, and 35 of A6A1U8. Also verify regular high/low logic activity at the inputs of U8. If the +5V supply and the inputs and clocks are good, replace U8.

c. With the R/T frequency set to 40.1 MHz, the VCO output should be at a frequency 80.5 MHz above the R/T frequency. Verify that the output of the VCO at A6A2P2 is at 120.6 MHz at a level of +7 dBm (+4 /-2 dBm). If the frequency is less than 110 MHz, measure the voltage at pin E3 of the A6A2A1 VCO Assembly. A measurement of +5V indicates a problem within the VCO. A measurement of –12V indicates a problem with the VCO bandswitch. If pin 18 of connector A6A2P1 is at +5V, there is a problem with A6A2R105, R106, C34, or C30. If P1–18 is also at –12V, check the values and operation of A6A1Q3 and the associated VCO bandswitch circuitry.

d. Verify that the VCO Sample signal is reaching pin 5 of A6A1U15 (prescaler). If the signal is not present, use the oscilloscope probe to monitor intermediate points along the path from pin E1 of the A6A2A1 VCO Assembly, through amplifier U13 and coax W2, to pin 30 of connector A6A2P1. Verify proper component values in the bias circuitry of U13. Verify the presence of the +6.8V bias supply. The signal should measure 0.355 Vrms (+4 dBm) at pin 30 of P1. Check for passage of the signal through amplifier A6A1Q11 and check the supporting bias circuitry.

e. If the inputs to A6A2U1 (pins 1 and 2) are correct and equal, the output at pin 5 (ramp up bias) shows proper high/low activity, and the Lock Detect output at pin 3 is still low (unlocked), replace U1.

f. If the unlocked condition persists, the A6A2 Synthesizer Assembly will require specialized alignment after any problem is corrected. For the reasons stated in subsection 5, the A6 Assembly should be replaced.

6.1.2.2 Second LO – Out of Lock

Verify that the 71.0 MHz second LO (PLL2_LD) is locked, as indicated by a logic 1 at pin 7 of A6A1U9. If PLL2_LD is unlocked (logic 0), the following procedure should help to isolate the fault.

a. Using the oscilloscope probe, verify the presence of the 1.2 MHz reference signal at pin 1 of A6A1U9. If this signal is not present, verify the voltage supplies to, and the proper input/output activity of A6A1U1, U5, and U6.

b. Verify that both pins 3 and 13 of U9 show a 200 kHz signal. If this signal is not present on pin 13, but the 1.2 MHz reference in step a is present on pin 1, verify the presence of serial clock, data, and enable strobe signals on pins 9, 10, and 11 of U9. If these signals are present and pin 13 does not exhibit 200 kHz, replace U9. If the 200 kHz is not present at pin 3, there may be a problem in the VCO feedback path through U11. Check U11 for proper +5V supply and input/output operation. If a 3.55 MHz signal is observed at pin 8 of U9, but the 200 kHz signal is not present on pin 3, replace U9.

c. If pins 3 and 13 of U9 are correct and equal, pins 15 and 16 should be held high (+5V), the VCO control voltage should be constant, and the second LO output should be a constant 71.0 MHz. Verify a VCO control voltage of about +6.5V at pins 1 and 7 of A6A1U14. Verify that the supporting components are of the correct values, and that there are no shorted or open signal lines.

d. If the 71.0 MHz output is not present at either pin 5 of A6A1U11 or pin 20 of A6A1P4, check components C1, CR4, CR5, L4, R13, R14, and R22 for proper values and shorted or open traces. Otherwise, the oscillator Y1–Q1 is probably not working. Verify that the +5V bias is present and that the supporting components are of the correct value and are not shorted/open. If the oscillator still does not function, replace Q1. As a last resort, replace Y1.

6.1.2.3 Third LO – Out of Lock

Verify that the 9.5 MHz third LO (PLL3_LD) is locked, as indicated by a logic 1 at pin 7 of A6A1U13. If PLL3_LD is unlocked (logic 0), use the following procedure to isolate the fault.

a. Using the oscilloscope probe, verify the presence of the 9.6 MHz reference signal at pin 1 of A6A1U13. If this signal is not present, verify the voltage supply to, and the proper 9.6 MHz output of A6A1U1. Also verify the value of A6A1R38 and that there are no shorts or opens on the 9.6 MHz line.

b. Verify that both pins 3 and 13 of U13 show an 18.5 kHz signal. If this signal is not present on pin 13, but the 9.6 MHz reference in step a is present on pin 1, verify the presence of serial clock, data, and enable strobe on pins 9, 10, and 11 of U13. If these signals are present and pin 13 does not exhibit 18.5 kHz, replace U13. If the 18.5 kHz signal is not present on pin 3, there may be a problem with the feedback capacitor C31, or there may be a problem in the oscillator itself. If a 9.47 MHz signal is present on pin 8 of U13, but the 18.5 kHz signal is not observed on pin 3, replace U13.

c. If pins 3 and 13 of U13 are correct and equal, pins 15 and 16 should be held high (+5V), the VCO control voltage should be constant, and the third LO output should be a constant 9.47 MHz. Verify a VCO control voltage of approximately +6.5V at test point A6A1TP2. Verify that the supporting components are of the correct values and that there are no shorted or open signal lines.

d. If the 9.47 MHz output is not present at pin 18 of connector A6A1P4, check components A6A1R35, R36, and C32 for proper values and shorted or open traces. Otherwise, the oscillator Q5–Q6 is probably not working. Verify that the +5V bias is present to both Q5 and Q6, and that supporting components are of the correct value and are not shorted/open. If the problem persists, replace Q5 and Q6.

6.1.2.4 All Local Oscillators In Lock

If all three of the PLL lock detect lines indicate locked status, but the assembly is still out of lock (at pin 12 of A6A1P4), there is a problem with the lock detect combining circuit based on A6A1Q2. Verify that the supporting components are of the correct value and are operating properly, and that there are no shorts/opens on the lines. Verify the presence of the +5V supply to the emitter of Q2. Replace Q2.

At this point, the lock detect function should be working properly. Reinstall the assembly and run BITE (self test) to verify that the problem no longer exists. If the system is still out of lock, begin the troubleshooting cycle again from subsection 6.1.1.

6.2 Fault 20 – Serial EEPROM Data Read Fault

This test verifies that the Main Controller section of the A4 Signal Processor Assembly was able to verify the checksum of the Reference Generator Assembly's EEPROM A6A1U2. If the fault occurs, replace the A6 Assembly with a known good assembly.

If the fault is located on the A6 Assembly, trace the serial clock, serial data, and EEPROM serial data lines on the A6 Assembly from the pins of A6U2 to the pins of connector A6P4. Check for opens and shorts on the lines. Also verify the values and correct operation of resistors A6A1R74, R75 and capacitors A6A1C69, C70. Otherwise, the data in the EEPROM A6A1U2 is corrupt. Since the EEPROM data is specific to TCXO (A6A1U1), and they must be used as a matched pair, it is recommended that the A6 Assembly be replaced.

If the fault still occurs with the known good A6 Assembly, the fault is most likely on the A4 Signal Processor Assembly or the A11 Interconnect Assembly. Perform the same module replacement technique as above with a known good A4 Assembly. Trace the serial clock, serial data, and EEPROM serial data lines from the A6 Assembly, through the A11 Interconnect Assembly, and to the A4 Signal Processor Assembly, as shown on their respective schematics. Check for opens or shorts on the lines. If the fault is located on the A4 Assembly, verify the values and correct operation of resistors A4R85, R84, R83, and R82. Verify power to, and correct input/output activity of A4U23.

7. PARTS LISTS, COMPONENT LOCATION DIAGRAMS, AND SCHEMATIC DIAGRAMS

Table 7 is the parts list for the A6 Reference Generator/Synthesizer Assembly. Table 8 is the parts list for the A6A1 Reference Generator PWB Assembly. Figure 16 is the component location diagram and figure 17 is the schematic diagram. Table 9 is the parts list for the A6A2 Synthesizer Assembly, figure 18 is the component location diagram, and figure 19 is the schematic diagram. Table 10 is the parts list for the A6A2A1 VCO PWB Assembly and figure 20 is the component location diagram.

Table 7. A6 Reference Generator/Synthesizer Assembly Parts List (10303-2700 Rev. D)

Ref. Desig.	Part Number	Description
—	10303-1108	SUPPORT, RUBBER
—	10303-1061	INSULATOR, PWB/SHIELD
—	10372-1524-01	CORD ASSY
—	10303-1124	INSULATOR
—	10372-1110-01	SHIELD ASSEMBLY
A1	10303-2710	PWB ASSY, REF GENERATOR
A2	10303-2720	PWB ASSY, SYNTHESIZER

Table 8. A6A1 Reference Generator Assembly Parts List (10303-2710 Rev. K)

Ref. Desig.	Part Number	Description
C1	C13-0103-102	CAP 1000PF 10% 100V SMD
C2	C13-0103-473	CAP .047UF 10% 100V SMD
C3	C13-0103-473	CAP .047UF 10% 100V SMD
C4	C13-0103-473	CAP .047UF 10% 100V SMD
C5	C13-0103-473	CAP .047UF 10% 100V SMD
C6	C13-0103-473	CAP .047UF 10% 100V SMD
C7	C13-0103-103	CAP .01UF 10% 100V SMD
C8	C13-0103-473	CAP .047UF 10% 100V SMD
C9	C13-0103-473	CAP .047UF 10% 100V SMD
C10	C13-0103-473	CAP .047UF 10% 100V SMD
C11	C13-0103-473	CAP .047UF 10% 100V SMD
C12	C13-0103-103	CAP .01UF 10% 100V SMD
C13	C13-0103-102	CAP 1000PF 10% 100V SMD
C15	C13-0105-820	CAP 82PF 10% 100V SMD
C16	C13-0105-100	CAP, CERAMIC CHIP, 10 PF
C17	C13-0103-473	CAP .047UF 10% 100V SMD
C18	C13-0103-102	CAP 1000PF 10% 100V SMD
C19	C13-0103-103	CAP .01UF 10% 100V SMD
C20	C13-0105-330	CAP 33PF 10% 100V SMD
C21	C13-0103-473	CAP .047UF 10% 100V SMD
C22	C13-0103-103	CAP .01UF 10% 100V SMD
C24	C13-0105-180	CAP 18PF 10% 100V SMD
C25	C13-0103-102	CAP 1000PF 10% 100V SMD
C26	C13-0103-103	CAP .01UF 10% 100V SMD
C27	C13-0105-120	CAP, 12PF 5% 100V SMD
C28	C13-0103-103	CAP .01UF 10% 100V SMD
C29	C13-0105-101	CAP, NPO, 100PF 5%
C30	C13-0103-102	CAP 1000PF 10% 100V SMD
C31	C13-0103-103	CAP .01UF 10% 100V SMD
C32	C13-0103-103	CAP .01UF 10% 100V SMD
C33	C13-0105-270	CAP 27PF 10% 100V SMD
C34	C13-0103-103	CAP .01UF 10% 100V SMD
C35	C13-0103-473	CAP .047UF 10% 100V SMD
C36	C13-0103-102	CAP 1000PF 10% 100V SMD
C37	C13-0105-270	CAP 27PF 10% 100V SMD
C39	C13-0105-101	CAP, NPO, 100PF 5%
C40	C13-0103-473	CAP .047UF 10% 100V SMD
C41	C13-0103-473	CAP .047UF 10% 100V SMD
C42	C13-0103-473	CAP .047UF 10% 100V SMD

Table 8. A6A1 Reference Generator Assembly Parts List (10303-2710 Rev. K) (Cont.)

Ref. Desig.	Part Number	Description
C43	C22-0015-685	CAP 6.8UF 10% 15V TANT
C45	C22-0025-335	CAP 3.3UF 10% 25V TANT
C46	C13-0103-102	CAP 1000PF 10% 100V SMD
C47	C22-0015-685	CAP 6.8UF 10% 15V TANT
C48	C13-0103-102	CAP 1000PF 10% 100V SMD
C49	C13-0103-473	CAP .047UF 10% 100V SMD
C50	C13-0103-102	CAP 1000PF 10% 100V SMD
C51	C13-0103-473	CAP .047UF 10% 100V SMD
C52	C13-0103-473	CAP .047UF 10% 100V SMD
C53	C13-0103-473	CAP .047UF 10% 100V SMD
C54	C13-0103-103	CAP .01UF 10% 100V SMD
C55	C13-0103-473	CAP .047UF 10% 100V SMD
C56	C13-0103-102	CAP 1000PF 10% 100V SMD
C57	C13-0103-102	CAP 1000PF 10% 100V SMD
C58	C13-0103-103	CAP .01UF 10% 100V SMD
C59	C13-0103-102	CAP 1000PF 10% 100V SMD
C60	C13-0103-473	CAP .047UF 10% 100V SMD
C61	C22-0010-226	CAP 22UF 10% 10V TANT
C61	C22-0010-226	CAP 22UF 10% 10V TANT
C62	C13-0103-473	CAP .047UF 10% 100V SMD
C65	C22-0025-335	CAP 3.3UF 10% 25V TANT
C66	C13-0103-103	CAP .01UF 10% 100V SMD
C67	C22-0010-226	CAP 22UF 10% 10V TANT
C68	C22-0010-106	CAP, 10UF 10V 10% TANT
C69	C13-0101-101	CAP 100PF 10% 100V SMD
C70	C13-0101-101	CAP 100PF 10% 100V SMD
C71	C13-0101-101	CAP 100PF 10% 100V SMD
C72	C22-0010-106	CAP, 10UF 10V 10% TANT
C73	C13-0103-473	CAP .047UF 10% 100V SMD
C74	C22-0025-335	CAP 3.3UF 10% 25V TANT
C75	C13-0103-103	CAP .01UF 10% 100V SMD
C76	C13-0103-103	CAP .01UF 10% 100V SMD
C77	C13-0103-473	CAP .047UF 10% 100V SMD
C79	C13-0103-473	CAP .047UF 10% 100V SMD
CR4	10075-1353	TUNING DIODE
CR5	10075-1353	TUNING DIODE
CR7	10075-1353	TUNING DIODE
CR8	1N5711	DIODE SCHOTTKY 70V .25W
CR9	10075-1353	TUNING DIODE

Table 8. A6A1 Reference Generator Assembly Parts List (10303-2710 Rev. K) (Cont.)

Ref. Desig.	Part Number	Description
CR10	1N4454	DIODE 200MA 75V SW
CR11	10075-1353	TUNING DIODE
CR12	10075-1353	TUNING DIODE
J1	J46-0115-030	CONN, 30 PIN MALE
L1	MS75084-12	COIL 10UH 10% FXD RF
L2	MS75084-1	COIL 1.2UH 10% FXD RF
L3	MS75083-1	COIL .10UH 10% FXD RF
L4	MS75083-12	COIL .82UH 10% FXD RF
L5	MS75084-1	COIL 1.2UH 10% FXD RF
L6	MS21422-23	COIL 6.8UH 5% FIXED
L7	MS75085-9	COIL 150UH 10% FXD RF
L8	MS75084-1	COIL 1.2UH 10% FXD RF
L9	MS75085-11	COIL 220UH 10% FXD RF
L10	MS75084-1	COIL 1.2UH 10% FXD RF
L11	MS75084-1	COIL 1.2UH 10% FXD RF
L12	MS75084-8	COIL 4.7UH 10% FXD RF
L13	MS75084-12	COIL 10UH 10% FXD RF
L14	MS75084-7	COIL 3.9UH 10% FXD RF
L15	MS75083-13	COIL 1.0UH 10% FXD RF
P4	J46-0117-030	CONN, 30 PIN MALE
Q1	2N5179	XSTR SS/RF NPN TO-72
Q2	Q02-4917-000	XSTR PN4917 SS/GP PNP 30V
Q3	Q02-4917-000	XSTR PN4917 SS/GP PNP 30V
Q4	Q02-4917-000	XSTR PN4917 SS/GP PNP 30V
Q5	Q35-0003-000	XSTR N-CH JFET U310
Q6	Q35-0003-000	XSTR N-CH JFET U310
Q7	Q50-0009-000	XSTR MPSH34 NPN 45V .35W
Q8	Q50-0009-000	XSTR MPSH34 NPN 45V .35W
Q9	Q02-4917-000	XSTR PN4917 SS/GP PNP 30V
Q10	Q02-4917-000	XSTR PN4917 SS/GP PNP 30V
Q11	Q35-0003-000	XSTR N-CH JFET U310
R1	R85-0125-100	RES 10 5% 1/8W FILM
R2	R85-0004-177	RES 619 1% 1/8W FLM
R3	R85-0004-269	RES 5110 1% 1/8W FLM
R4	R85-0004-181	RES 681 1% 1/8W FLM
R5	R30-0018-203	RES, VARIABLE 20K
R6	R85-0125-152	RES 1.5K 5% 1/8W FILM
R7	R85-0125-100	RES 10 5% 1/8W FILM
R8	R85-0125-100	RES 10 5% 1/8W FILM

Table 8. A6A1 Reference Generator Assembly Parts List (10303-2710 Rev. K) (Cont.)

Ref. Desig.	Part Number	Description
R9	R85-0125-330	RES 33 5% 1/8W FILM
R10	R85-0125-100	RES 10 5% 1/8W FILM
R11	R85-0004-034	RES 22.1 1% 1/8W FLM
R12	R85-0125-223	RES 22K 5% 1/8W FILM
R13	R85-0004-026	RES 18.2 1% 1/8W FLM
R14	R85-0004-334	RES 22.1K 1% 1/8W FLM
R15	R85-0004-151	RES 332 1% 1/8W FLM
R16	R85-0004-209	RES FILM 1.21K 1% 1/8 SMD
R17	R85-0004-118	RES 150 1% 1/8 WATT
R18	R85-0004-201	RES 1000 1% 1/8W FLM
R19	R85-0004-366	RES 47.5K 1% 1/8W FLM
R20	R85-0004-366	RES 47.5K 1% 1/8W FLM
R21	R85-0004-430	RES 200K 1% 1/8W FILM
R22	R85-0004-018	RES 15.0 1% 1/8W FLM
R23	R85-0125-184	RES 180K 5% 1/8W FLM
R24	R85-0004-158	RES 392 1% 1/8W FLM
R25	R85-0004-366	RES 47.5K 1% 1/8W FLM
R26	R85-0004-366	RES 47.5K 1% 1/8W FLM
R27	R85-0004-430	RES 200K 1% 1/8W FILM
R28	R85-0125-184	RES 180K 5% 1/8W FILM
R29	R85-0125-104	RES 100K 5% 1/8W FILM
R30	R85-0125-100	RES 10 5% 1/8W FILM
R31	R85-0004-151	RES 332 1% 1/8W FLM
R32	R85-0125-100	RES 10 5% 1/8W FILM
R33	R85-0125-101	RES 100 5% 1/8W FILM
R34	R85-0125-223	RES 22K 5% 1/8W FILM
R35	R85-0125-561	RES 560 5% 1/8W FILM
R36	R85-0125-330	RES 33 5% 1/8W FILM
R37	R85-0125-101	RES 100 5% 1/8W FILM
R38	R85-0125-100	RES 10 5% 1/8W FILM
R39	R85-0004-307	RES,11.5K 1% 1/8W CHIP
R40	R85-0004-034	RES 22.1 1% 1/8W FLM
R41	R85-0004-283	RES 7.15K 1% 1/8W SMD
R42	R85-0004-283	RES 7.15K 1% 1/8W SMD
R43	R85-0004-283	RES 7.15K 1% 1/8W SMD
R44	R85-0004-366	RES 47.5K 1% 1/8W FLM
R45	R85-0004-401	RES 100K 1% 1/8W FLM
R46	R85-0004-283	RES 7.15K 1% 1/8W SMD
R47	R85-0125-223	RES 22K 5% 1/8W FILM

Table 8. A6A1 Reference Generator Assembly Parts List (10303-2710 Rev. K) (Cont.)

Ref. Desig.	Part Number	Description
R48	R85-0125-330	RES 33 5% 1/8W FILM
R50	R85-0125-330	RES 33 5% 1/8W FILM
R51	R85-0004-266	RES,4.75K 1% 1/8W CHIP
R52	R85-0125-103	RES 10K 5% 1/8W FILM
R53	R85-0125-100	RES 10 5% 1/8W FILM
R54	R85-0125-103	RES 10K 5% 1/8W FILM
R55	R85-0125-103	RES 10K 5% 1/8W FILM
R56	R40-0016-203	RES VAR 20K OHM PCB
R57	R85-0125-473	RES 47K 5% 1/8W FILM
R58	R85-0004-266	RES,4.75K 1% 1/8W CHIP
R59	R85-0004-266	RES,4.75K 1% 1/8W CHIP
R60	R85-0004-151	RES 332 1% 1/8W FLM
R61	R85-0004-158	RES 392 1% 1/8W FLM
R62	R85-0004-151	RES 332 1% 1/8W FLM
R63	R85-0004-130	RES 200 1% 1/8W FLM
R64	R85-0125-330	RES 33 5% 1/8W FILM
R65	R85-0004-266	RES,4.75K 1% 1/8W CHIP
R66	R85-0004-266	RES,4.75K 1% 1/8W CHIP
R67	R85-0125-100	RES 10 5% 1/8W FILM
R68	R85-0125-101	RES 100 5% 1/8W FILM
R69	R85-0004-225	RES 1780 1% 1/8W FLM
R71	R85-0125-100	RES 10 5% 1/8W FILM
R72	R85-0125-101	RES 100 5% 1/8W FILM
R74	R85-0125-101	RES 100 5% 1/8W FILM
R75	R85-0125-101	RES 100 5% 1/8W FILM
R76	R85-0125-223	RES 22K 5% 1/8W FILM
R77	R85-0125-101	RES 100 5% 1/8W FILM
R78	R85-0125-027	RES 2.7 5% 1/8W SMD
R79	R85-0125-027	RES 2.7 5% 1/8W SMD
R80	R85-0125-101	RES 100 5% 1/8W FILM
R83	R85-0125-102	RES 1.0K 5% 1/8W FILM
U1	10303-3126	CRYSTAL, TCXO
U2	I25-0031-001	IC, EEPROM (NMC93CS66EN)
U3	I11-0014-001	IC VR 317 ADJ V .10A
U4	I14-0013-010	IC RESET MAX690EPA
U5	I15-0000-393	IC 74HC393 PLASTIC CMOS
U6	I15-0000-163	IC 74HC163 PLASTIC CMOS
U7	10085-5620	IC FRACTIONAL N
U8	10303-8010	FIRMWARE KIT(SYNTH ACTEL)

Table 8. A6A1 Reference Generator Assembly Parts List (10303-2710 Rev. K) (Cont.)

Ref. Desig.	Part Number	Description
U9	I70-0005-001	IC FREQ SYNTH 145158
U11	I70-0012-001	IC PRESCALER 20/21 12019
U12	I15-0000-004	IC 74HC04 PLASTIC CMOS
U13	I70-0013-003	IC,PLL,FREQ SYNTHESIZER
U14	I30-0049-001	IC, OP AMP DUAL (MC33172P
U15	I70-0012-001	IC PRESCALER 20/21 12019
Y1	10303-3105	CRYSTAL, 71MHZ
Y2	10303-3112	CRYSTAL, 36.16 MHZ

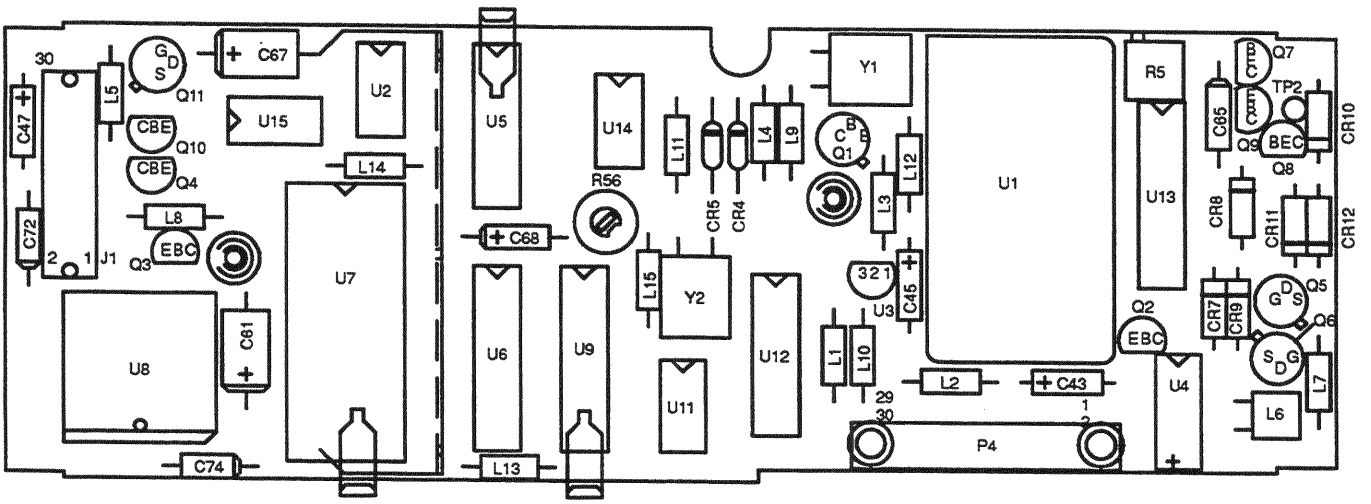


Figure 16. A6A1 Reference Generator Assembly Component Location Diagram (10303-2710 Rev. A) (Sheet 1 of 2)

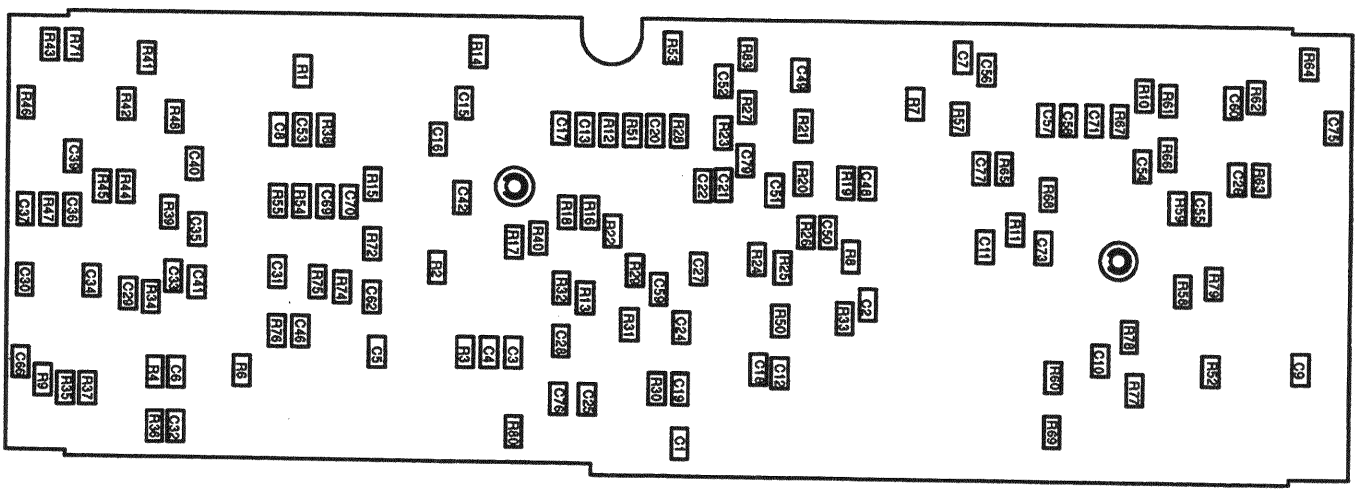


Figure 16. A6A1 Reference Generator Assembly Component Location Diagram
(10303-2710 Rev. A) (Sheet 2 of 2)

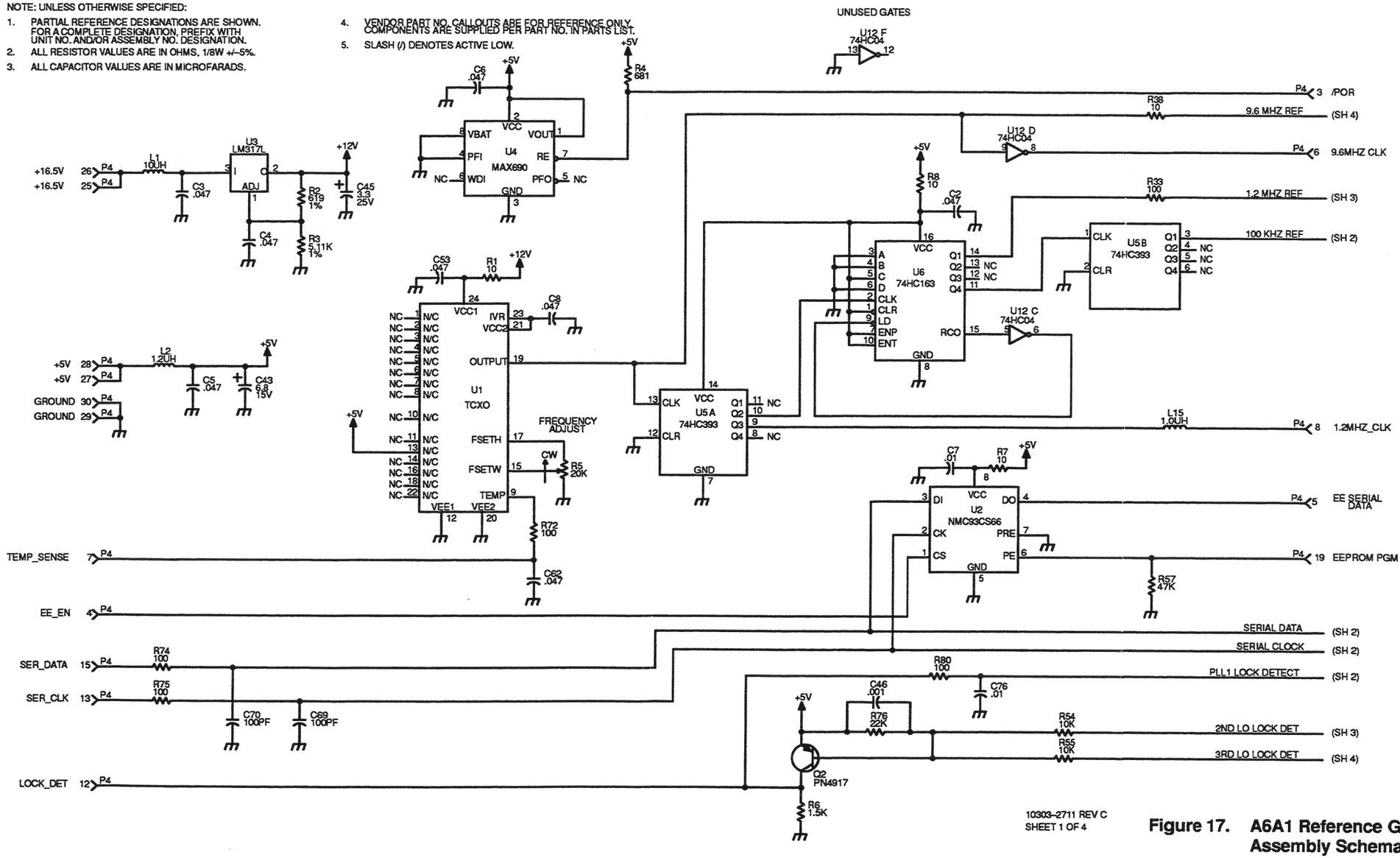
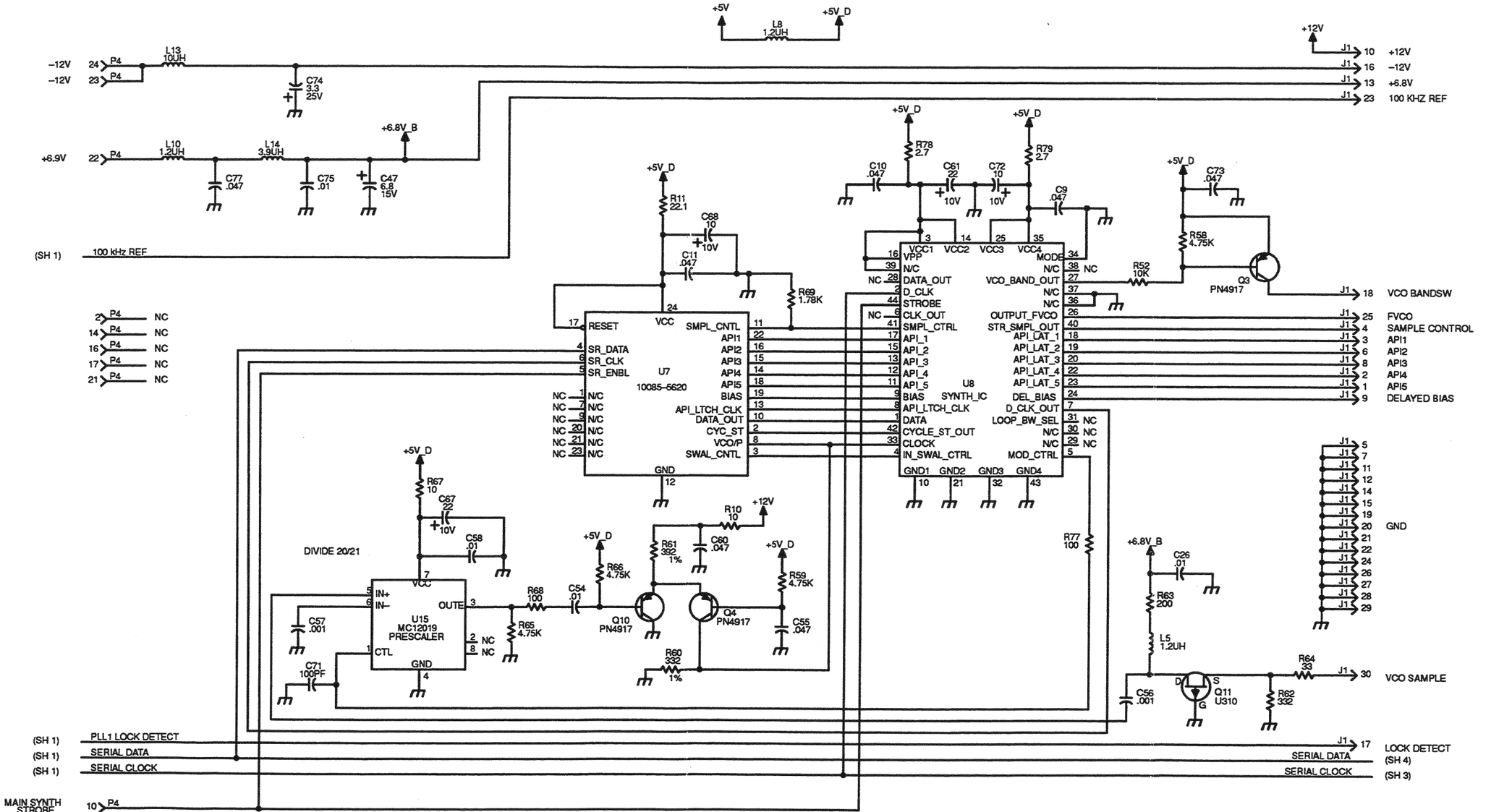
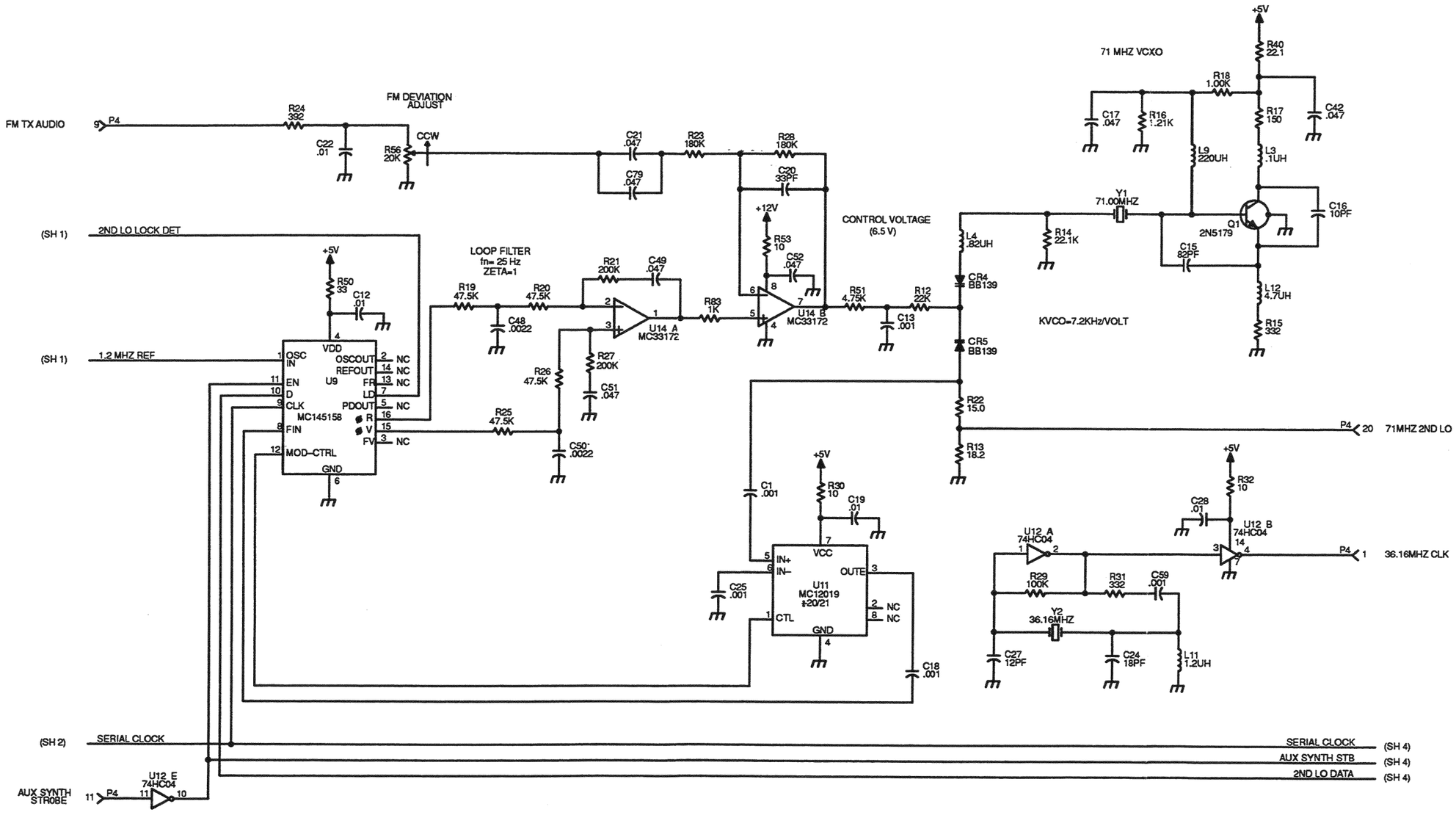


Figure 17. A6A1 Reference Generator Assembly Schematic Diagram (10303-2711 Rev. C) (Sheet 1 of 4)



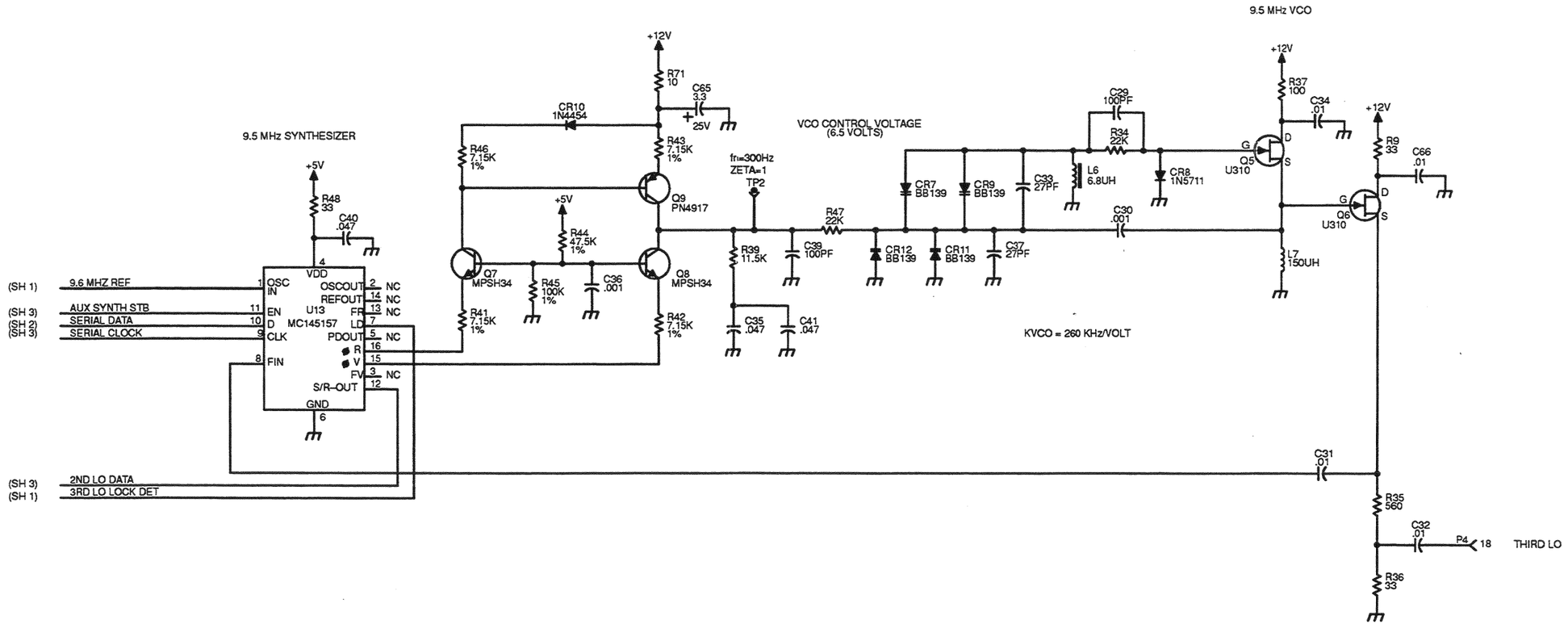
10303-2711 REV C
SHEET 2 OF 4

Figure 17. A6A1 Reference Generator Assembly Schematic Diagram (10303-2711 Rev. C) (Sheet 2 of 4)



10303-2711 REV C
SHEET 3 OF 4

Figure 17. A6A1 Reference Generator Assembly Schematic Diagram (10303-2711 Rev. C) (Sheet 3 of 4)



10303-2711 REV C
SHEET 4 OF 4

Figure 17. A6A1 Reference Generator Assembly Schematic Diagram (10303-2711 Rev. C) (Sheet 4 of 4)

Table 9. A6A2 Synthesizer Assembly Parts List (10303-2720 Rev. –)

Ref. Desig.	Part Number	Description
—	Z25-0071-015	TOROID
A1	10303-2730	PWB ASSY, VCO
C1	C13-0103-473	CAP .047UF 10% 100V SMD
C2	C22-0020-155	CAP, 1.5UF, 20V
C3	C13-0103-473	CAP .047UF 10% 100V SMD
C4	C22-0020-335	CAP 3.3UF 20V TANT
C5	C13-0103-473	CAP .047UF 10% 100V SMD
C6	C13-0103-473	CAP .047UF 10% 100V SMD
C7	C22-0010-106	CAP, 10UF 10V 10% TANT
C8	C40-0005-301	CAP, MICA, 300PF, 50V
C9	C22-0020-475	CAP 4.7UF 10% 20V TANT
C10	C13-0105-829	CAP 8.2PF +-.5PF 100V SMD
C11	C13-0103-103	CAP .01UF 10% 100V SMD
C12	C22-0020-475	CAP 4.7UF 10% 20V TANT
C13	C13-0103-103	CAP .01UF 10% 100V SMD
C14	C13-0103-273	CAP, CERAMIC CHIP, .027UF
C15	C22-0020-475	CAP 4.7UF 10% 20V TANT
C16	C13-0103-473	CAP .047UF 10% 100V SMD
C17	C22-0020-155	CAP, 1.5UF, 20V
C18	C22-0010-106	CAP, 10UF 10V 10% TANT
C19	C13-0105-100	CAP, CERAMIC CHIP, 10 PF
C20	C22-0020-155	CAP, 1.5UF, 20V
C21	C22-0020-155	CAP, 1.5UF, 20V
C22	C13-0103-473	CAP .047UF 10% 100V SMD
C23	C13-0103-473	CAP .047UF 10% 100V SMD
C24	C40-0005-391	CAP, MICA, 390PF, 50V
C25	C85-0009-101	CAP VAR 2.5-10PF AIR
C26	C40-0005-331	CAP, MICA, 330PF, 50V
C27	C13-0103-102	CAP 1000PF 10% 100V SMD
C28	M39003/01-2280	CAP 1.5UF 10% 20V TANT-M
C29	C13-0103-103	CAP .01UF 10% 100V SMD
C30	C13-0103-103	CAP .01UF 10% 100V SMD
C31	C22-0020-475	CAP 4.7UF 10% 20V TANT
C32	C22-0020-106	CAP 10UF 20V TANT
C33	C36-0016-336	CAP, 33UF 16V TANT
C34	C13-0103-103	CAP .01UF 10% 100V SMD
C35	C36-0016-106	CAP 10UF 16V SMT
C36	C22-0010-106	CAP, 10UF 10V 10% TANT
C37	C22-0025-335	CAP 3.3UF 10% 25V TANT

Table 9. A6A2 Synthesizer Assembly Parts List (10303-2720 Rev. –) (Cont.)

Ref. Desig.	Part Number	Description
C38	C36-0010-476	CAP, 47UF 10V TANT SMD
C39	C36-0120-106	CAP, KEMET, 10 UF, 20V
C40	C36-0120-106	CAP, KEMET, 10 UF, 20V
C41	C22-0025-335	CAP 3.3UF 10% 25V TANT
C42	C13-0103-103	CAP .01UF 10% 100V SMD
C43	C13-0103-103	CAP .01UF 10% 100V SMD
C47	C22-0020-475	CAP 4.7UF 10% 20V TANT
C48	C80-0008-184	CAP POLYCARB .18UF 50V
C49	C13-0103-682	CAP 6800PF 10% 100V SMD
C50	C13-0103-473	CAP .047UF 10% 100V SMD
C51	C13-0103-473	CAP .047UF 10% 100V SMD
C52	C13-0103-392	CAP 3900PF, 10% 100V
C53	C13-0101-911	CAP, 910PF 10% 100V SMD
C54	C13-0103-392	CAP 3900PF, 10% 100V
C55	C13-0101-621	CAP, 620PF CERAMIC CHIP
C56	C13-0101-102	CAP 1000PF 10% 100V SMD
C57	C13-0103-103	CAP .01UF 10% 100V SMD
C77	C13-0103-103	CAP .01UF 10% 100V SMD
C78	C13-0103-103	CAP .01UF 10% 100V SMD
C79	C13-0103-103	CAP .01UF 10% 100V SMD
C83	C13-0103-103	CAP .01UF 10% 100V SMD
CR1	1N4454	DIODE 200MA 75V SW
CR2	1N4454	DIODE 200MA 75V SW
CR3	1N5711	DIODE SCHOTTKY 70V .25W
CR4	1N5711	DIODE SCHOTTKY 70V .25W
CR5	1N5711	DIODE SCHOTTKY 70V .25W
CR6	1N5711	DIODE SCHOTTKY 70V .25W
CR7	1N4454	DIODE 200MA 75V SW
CR8	1N4454	DIODE 200MA 75V SW
CR9	1N4454	DIODE 200MA 75V SW
CR10	1N4454	DIODE 200MA 75V SW
CR12	1N5297	DIODE 1.00MA CURRENT REG
CR13	1N4454	DIODE 200MA 75V SW
CR14	1N5711	DIODE SCHOTTKY 70V .25W
CR15	1N5711	DIODE SCHOTTKY 70V .25W
CR16	1N5711	DIODE SCHOTTKY 70V .25W
L1	MS75085-11	COIL 220UH 10% FXD RF
L2	MS75084-16	COIL 22.0UH 10% FXD RF
L5	MS75084-16	COIL 22.0UH 10% FXD RF

Table 9. A6A2 Synthesizer Assembly Parts List (10303-2720 Rev. –) (Cont.)

Ref. Desig.	Part Number	Description
L7	MS75084-16	COIL 22.0UH 10% FXD RF
L8	MS75085-15	COIL 470UH 10% FXD RF
L9	MS75085-13	COIL 330UH 10% FXD RF
P1	J46-0113-030	CONN, 30 POS FEMALE
Q1	Q02-4917-000	XSTR PN4917 SS/GP PNP 30V
Q2	Q02-4917-000	XSTR PN4917 SS/GP PNP 30V
Q3	Q50-0009-000	XSTR MPSH34 NPN 45V .35W
Q4	Q02-4917-000	XSTR PN4917 SS/GP PNP 30V
Q5	Q02-4917-000	XSTR PN4917 SS/GP PNP 30V
Q6	Q02-4917-000	XSTR PN4917 SS/GP PNP 30V
Q7	Q02-4917-000	XSTR PN4917 SS/GP PNP 30V
Q8	Q50-0009-000	XSTR MPSH34 NPN 45V .35W
Q9	Q50-0009-000	XSTR MPSH34 NPN 45V .35W
Q10	Q50-0009-000	XSTR MPSH34 NPN 45V .35W
Q11	Q30-0006-000	XSTR JFET
Q12	Q30-0006-000	XSTR JFET
Q13	Q02-4917-000	XSTR PN4917 SS/GP PNP 30V
Q14	Q02-4917-000	XSTR PN4917 SS/GP PNP 30V
Q15	Q02-4917-000	XSTR PN4917 SS/GP PNP 30V
Q16	JAN2N5116	XSTR SW P-CH JFET 30V
Q17	Q02-4917-000	XSTR PN4917 SS/GP PNP 30V
Q18	Q02-4917-000	XSTR PN4917 SS/GP PNP 30V
Q19	Q02-4917-000	XSTR PN4917 SS/GP PNP 30V
Q20	Q05-0003-001	XSTR, N-CH JFET (PN4393)
Q21	Q05-0003-001	XSTR, N-CH JFET (PN4393)
Q22	Q02-4917-000	XSTR PN4917 SS/GP PNP 30V
Q23	Q02-4917-000	XSTR PN4917 SS/GP PNP 30V
Q28	Q50-0011-000	XSTR DUAL AMP MD918A
R1	R85-0125-103	RES 10K 5% 1/8W FILM
R2	R85-0004-201	RES 1000 1% 1/8W FLM
R3	R85-0004-201	RES 1000 1% 1/8W FLM
R4	R85-0125-223	RES 22K 5% 1/8W FILM
R5	R85-0004-234	RES 2.21K 1% 1/8W FLM
R6	R85-0004-179	RES, 649 1% 1/8W CHIP
R7	R85-0004-168	RES 499 1% 1/8W FLM
R8	R85-0004-301	RES 10K 1% 1/8W FLM
R9	R85-0125-220	RES 22 5% 1/8W FILM
R10	R85-0004-225	RES 1780 1% 1/8W FLM
R11	R85-0004-225	RES 1780 1% 1/8W FLM

Table 9. A6A2 Synthesizer Assembly Parts List (10303-2720 Rev. –) (Cont.)

Ref. Desig.	Part Number	Description
R12	R85-0004-081	RES 68.1 1% 1/8W FLM
R13	R85-0125-100	RES 10 5% 1/8W FILM
R14	R85-0125-101	RES 100 5% 1/8W FILM
R15	R85-0125-100	RES 10 5% 1/8W FILM
R16	R85-0125-470	RES 47 5% 1/8W FILM
R17	R85-0004-363	RES,44.2K 1% 1/8W CHIP
R18	R85-0004-251	RES 3320 1% 1/8W
R19	R85-0004-221	RES,1.62K 1% 1/8W CHIP
R20	R85-0125-470	RES 47 5% 1/8W FILM
R21	R85-0004-239	RES 2490 1% 1/8W FLM
R22	R85-0004-326	RES,18.2K 1% 1/8W CHIP
R23	R85-0004-253	RES 3480 1% 1/8W FLM
R24	R85-0004-288	RES,8.06K 1% 1/8W CHIP
R25	R85-0004-271	RES,5.36K 1% 1/8W CHIP
R26	R85-0004-307	RES,11.5K 1% 1/8W CHIP
R27	R85-0004-288	RES,8.06K 1% 1/8W CHIP
R28	R85-0004-269	RES 5110 1% 1/8W FLM
R29	R85-0004-225	RES 1780 1% 1/8W FLM
R30	R85-0004-266	RES,4.75K 1% 1/8W CHIP
R31	R85-0004-269	RES 5110 1% 1/8W FLM
R32	R85-0004-225	RES 1780 1% 1/8W FLM
R33	R85-0004-266	RES,4.75K 1% 1/8W CHIP
R34	R85-0004-269	RES 5110 1% 1/8W FLM
R35	R85-0004-225	RES 1780 1% 1/8W FLM
R36	R85-0004-266	RES,4.75K 1% 1/8W CHIP
R37	R85-0004-229	RES 1960 1% 1/8W FLM
R38	R85-0125-101	RES 100 5% 1/8W FILM
R39	R85-0125-470	RES 47 5% 1/8W FILM
R40	R85-0004-218	RES 1500 1% 1/8W FLM
R41	R30-0016-503	RES, VAR 50K
R42	R40-0016-102	RES VAR 1K OHM PCB
R43	R85-0004-330	RES 20.0K 1% 1/8W FLM
R44	R85-0004-101	RES 100 1% 1/8W FLM
R46	R40-0016-201	RES VAR 200 OHM PCB
R47	R85-0004-258	RES 3920 1% 1/8W FLM
R48	R85-0125-106	RES 10M 5% 1/8W FILM
R49	R85-0004-493	RES 909K 1% 1/8W FLM
R50	R85-0004-234	RES 2.21K 1% 1/8W FLM
R51	R85-0004-234	RES 2.21K 1% 1/8W FLM

Table 9. A6A2 Synthesizer Assembly Parts List (10303-2720 Rev. –) (Cont.)

Ref. Desig.	Part Number	Description
R52	R85-0125-470	RES 47 5% 1/8W FILM
R53	R85-0125-470	RES 47 5% 1/8W FILM
R54	R85-0004-261	RES 4220 1% 1/8W FLM
R55	R85-0004-266	RES,4.75K 1% 1/8W CHIP
R56	R85-0125-223	RES 22K 5% 1/8W FILM
R57	R85-0004-301	RES 10K 1% 1/8W FLM
R58	R85-0004-210	RES 1.24K 1% 1/8W SMD
R59	R85-0004-234	RES 2.21K 1% 1/8W FLM
R60	R85-0004-351	RES 33.2K 1% 1/8W FLM
R61	R85-0004-234	RES 2.21K 1% 1/8W FLM
R62	R85-0125-470	RES 47 5% 1/8W FILM
R63	R85-0125-101	RES 100 5% 1/8W FILM
R64	R85-0004-201	RES 1000 1% 1/8W FLM
R65	R85-0004-229	RES 1960 1% 1/8W FLM
R66	R85-0125-101	RES 100 5% 1/8W FILM
R67	R85-0004-201	RES 1000 1% 1/8W FLM
R68	R85-0004-201	RES 1000 1% 1/8W FLM
R69	R85-0125-101	RES 100 5% 1/8W FILM
R70	R85-0004-229	RES 1960 1% 1/8W FLM
R71	R85-0004-229	RES 1960 1% 1/8W FLM
R72	R85-0004-189	RES 825 1% 1/8W FLM
R73	R85-0004-189	RES 825 1% 1/8W FLM
R74	R85-0004-189	RES 825 1% 1/8W FLM
R76	R85-0125-102	RES 1.0K 5% 1/8W FILM
R77	R85-0125-102	RES 1.0K 5% 1/8W FILM
R78	R85-0125-470	RES 47 5% 1/8W FILM
R79	R85-0004-189	RES 825 1% 1/8W FLM
R80	R85-0125-101	RES 100 5% 1/8W FILM
R81	R85-0004-189	RES 825 1% 1/8W FLM
R82	R85-0004-301	RES 10K 1% 1/8W FLM
R83	R85-0125-560	RES 56 5% 1/8W FILM
R84	R85-0125-152	RES 1.5K 5% 1/8W FILM
R85	R85-0004-289	RES 8250 1% 1/8W FLM
R86	R85-0004-301	RES 10K 1% 1/8W FLM
R87	R85-0125-102	RES 1.0K 5% 1/8W FILM
R88	R85-0125-101	RES 100 5% 1/8W FILM
R89	R85-0125-103	RES 10K 5% 1/8W FILM
R90	R85-0125-331	RES 330 5% 1/8W FILM
R103	R65-0003-820	RES 82 5% 1/4W CAR FILM

Table 9. A6A2 Synthesizer Assembly Parts List (10303-2720 Rev. –) (Cont.)

Ref. Desig.	Part Number	Description
R104	R65-0003-100	RES 10 5% 1/4W CAR FILM
R105	R85-0125-223	RES 22K 5% 1/8W FILM
R106	R85-0125-121	RES 120 5% 1/8W FILM
R107	R85-0125-100	RES 10 5% 1/8W FILM
R108	R85-0125-475	RES 4.7M 5% 1/8W
R110	R85-0125-101	RES 100 5% 1/8W FILM
R111	R85-0125-271	RES 270 5% 1/8W FILM
R112	R85-0125-560	RES 56 5% 1/8W FILM
R113	R85-0125-331	RES 330 5% 1/8W FILM
U1	I60-0007-001	IC,PHASE DET (IMI4345008P
U3	I30-0047-001	IC, BIFET OP AMP (AD744BN
U4	I90-0008-001	IC XSTR ARRAY 3045
U5	10303-3110	RESISTOR NETWORK
U6	I11-0020-001	VOLTAGE REG 5V (LM2936Z-5
U7	I90-0008-001	IC XSTR ARRAY 3045
U8	I12-0012-001	IC TL431 VOLT REF TO92
U9	I30-0048-002	IC, LP DUAL OP-AMP (MC331
U10	I11-0020-001	VOLTAGE REG 5V (LM2936Z-5
U11	I11-0020-001	VOLTAGE REG 5V (LM2936Z-5
U13	I69-0002-001	IC MWA110 RF AMP WBW TO39
VR1	I14-0010-002	REF DIODE, 5 VOLT
VR2	I14-0010-002	REF DIODE, 5 VOLT
VR3	I14-0015-007	REG, PREC 2.5V (LM285BXZ-
W1	10303-1090	CABLE ASSY, RF

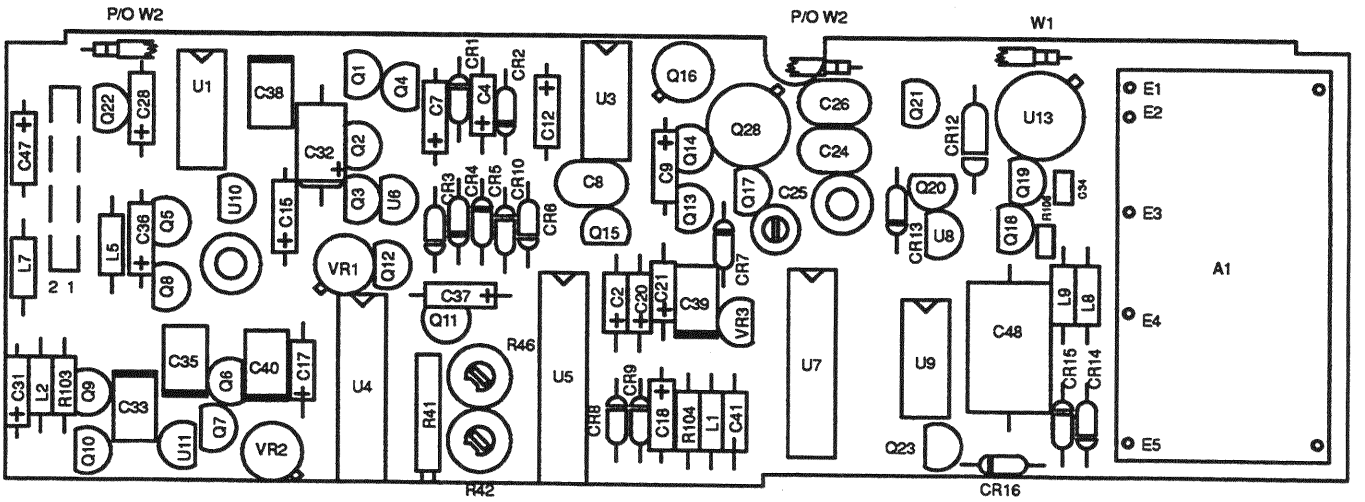


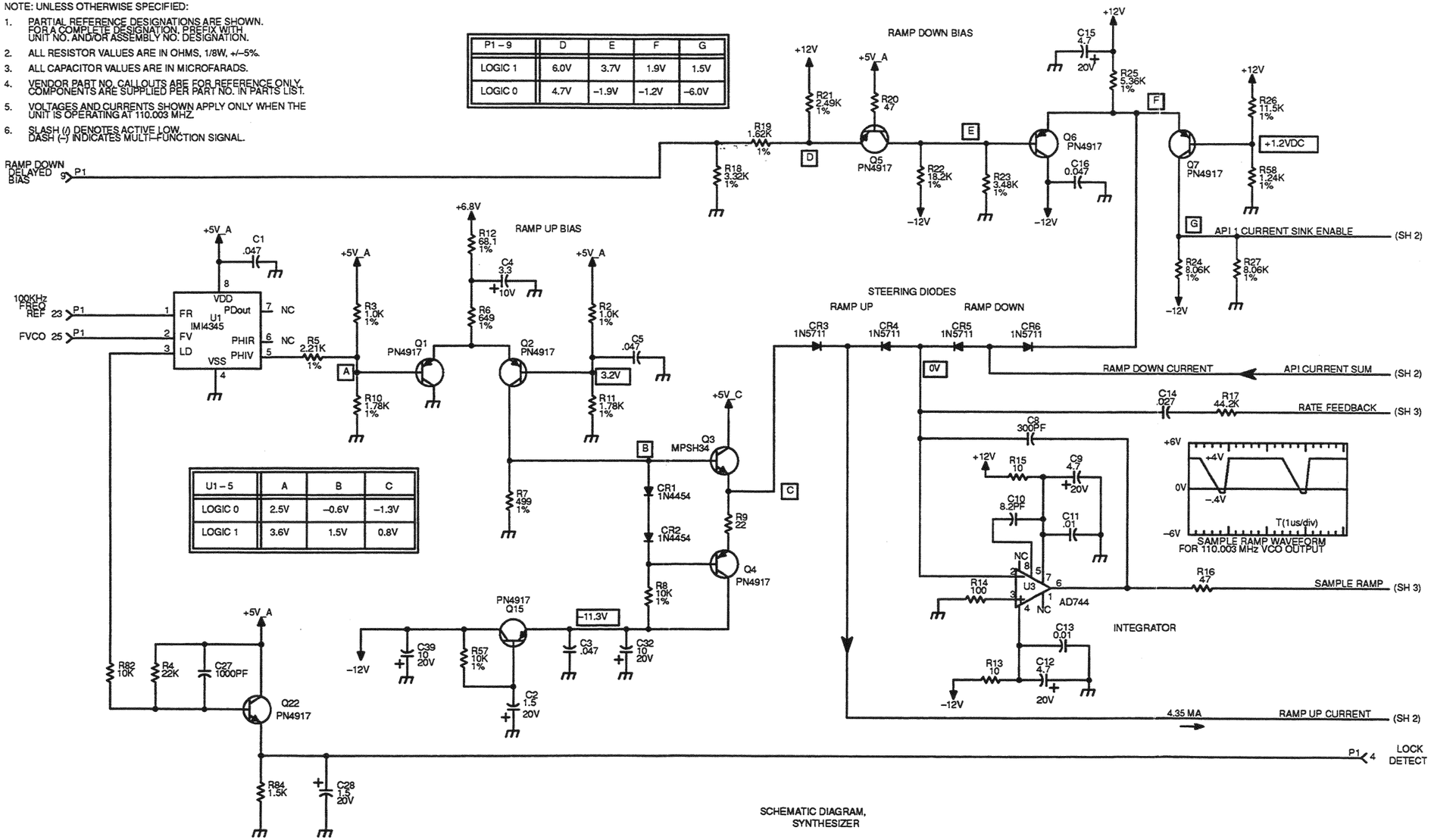
Figure 18. A6A2 Synthesizer Assembly Component Location Diagram (10303-2720 Rev. A)

NOTE: UNLESS OTHERWISE SPECIFIED:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR A COMPLETE DESIGNATION, PREFIX WITH UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.
2. ALL RESISTOR VALUES ARE IN OHMS, 1/8W, +/–5%.
3. ALL CAPACITOR VALUES ARE IN MICROFARADS.
4. VENDOR PART NO. CALLOUTS ARE FOR REFERENCE ONLY. COMPONENTS ARE SUPPLIED PER PART NO. IN PARTS LIST.
5. VOLTAGES AND CURRENTS SHOWN APPLY ONLY WHEN THE UNIT IS OPERATING AT 110.003 MHZ.
6. SLASH (/) DENOTES ACTIVE LOW. DASH (–) INDICATES MULTI-FUNCTION SIGNAL.

P1 – 9	D	E	F	G
LOGIC 1	6.0V	3.7V	1.9V	1.5V
LOGIC 0	4.7V	–1.9V	–1.2V	–6.0V

U1 – 5	A	B	C
LOGIC 0	2.5V	–0.6V	–1.3V
LOGIC 1	3.6V	1.5V	0.8V



SCHEMATIC DIAGRAM, SYNTHESIZER

10303–2721 –
1 OF 5

Figure 19. A6A2 SynthesizerAssembly Schematic Diagram (10303-2721 Rev. –) (Sheet 1 of 5)

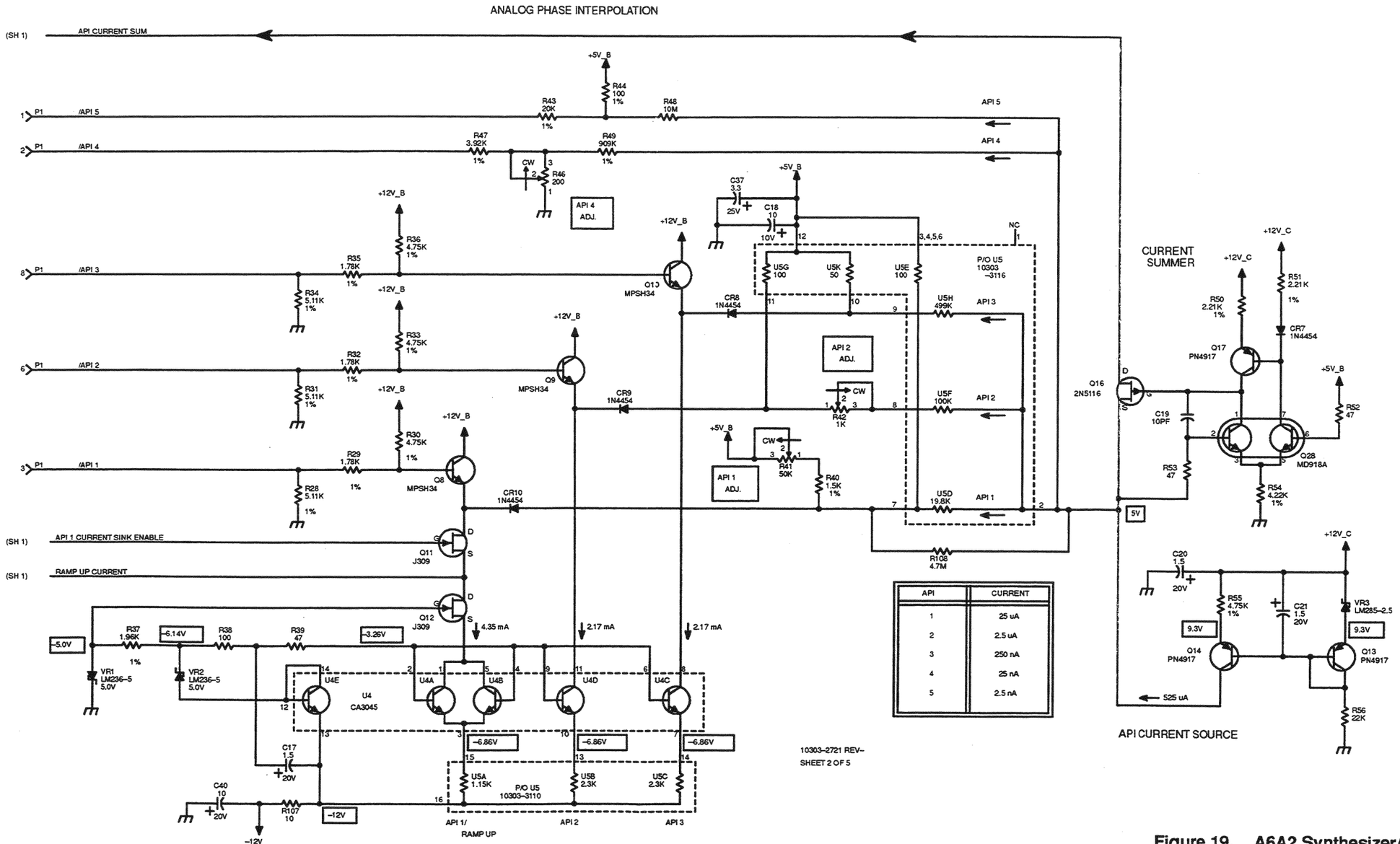
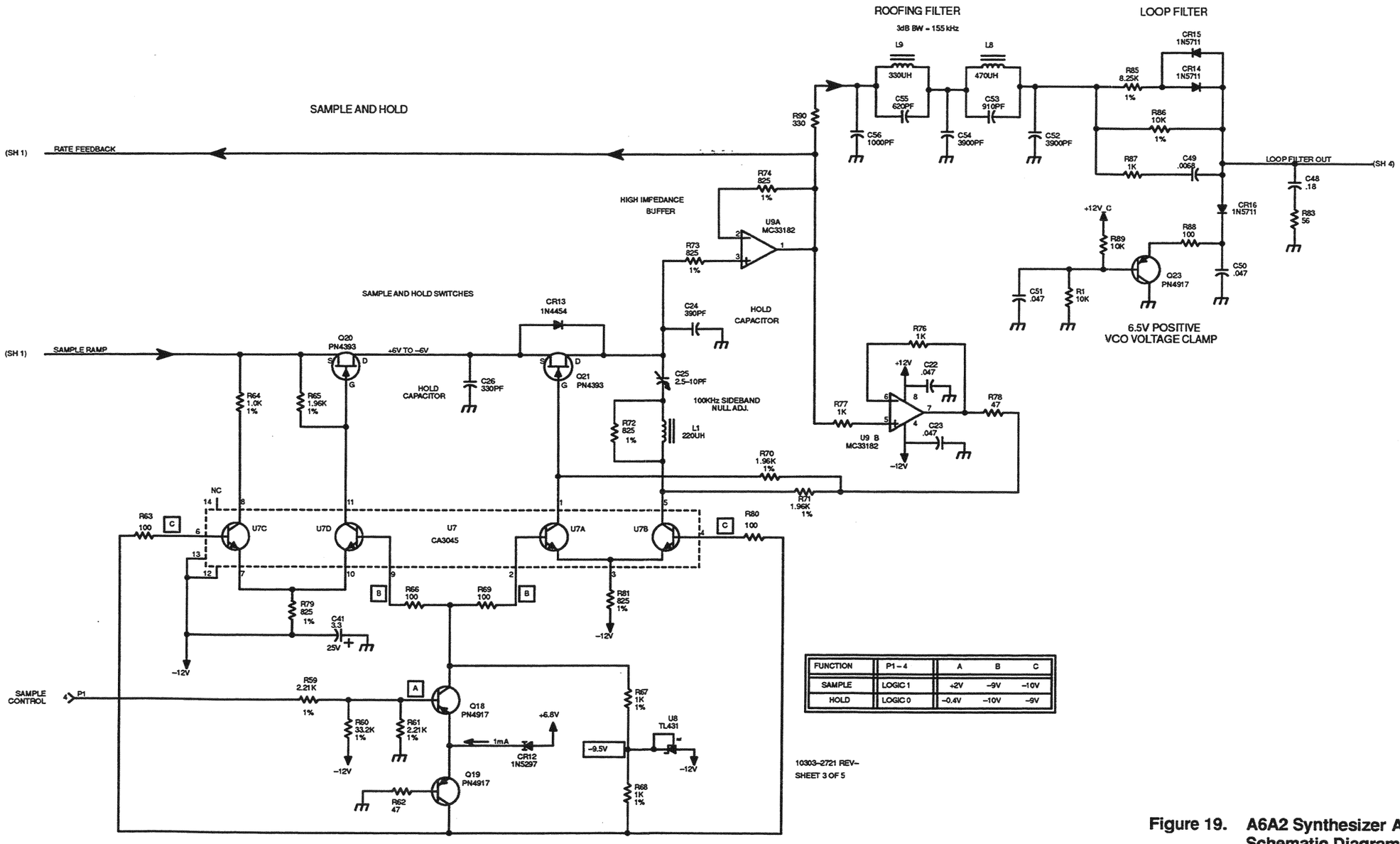


Figure 19. A6A2 SynthesizerAssembly Schematic Diagram (10303-2721 Rev. –) (Sheet 2 of 5)



FUNCTION	P1 – 4	A	B	C
SAMPLE	LOGIC 1	+2V	–9V	–10V
HOLD	LOGIC 0	–0.4V	–10V	–9V

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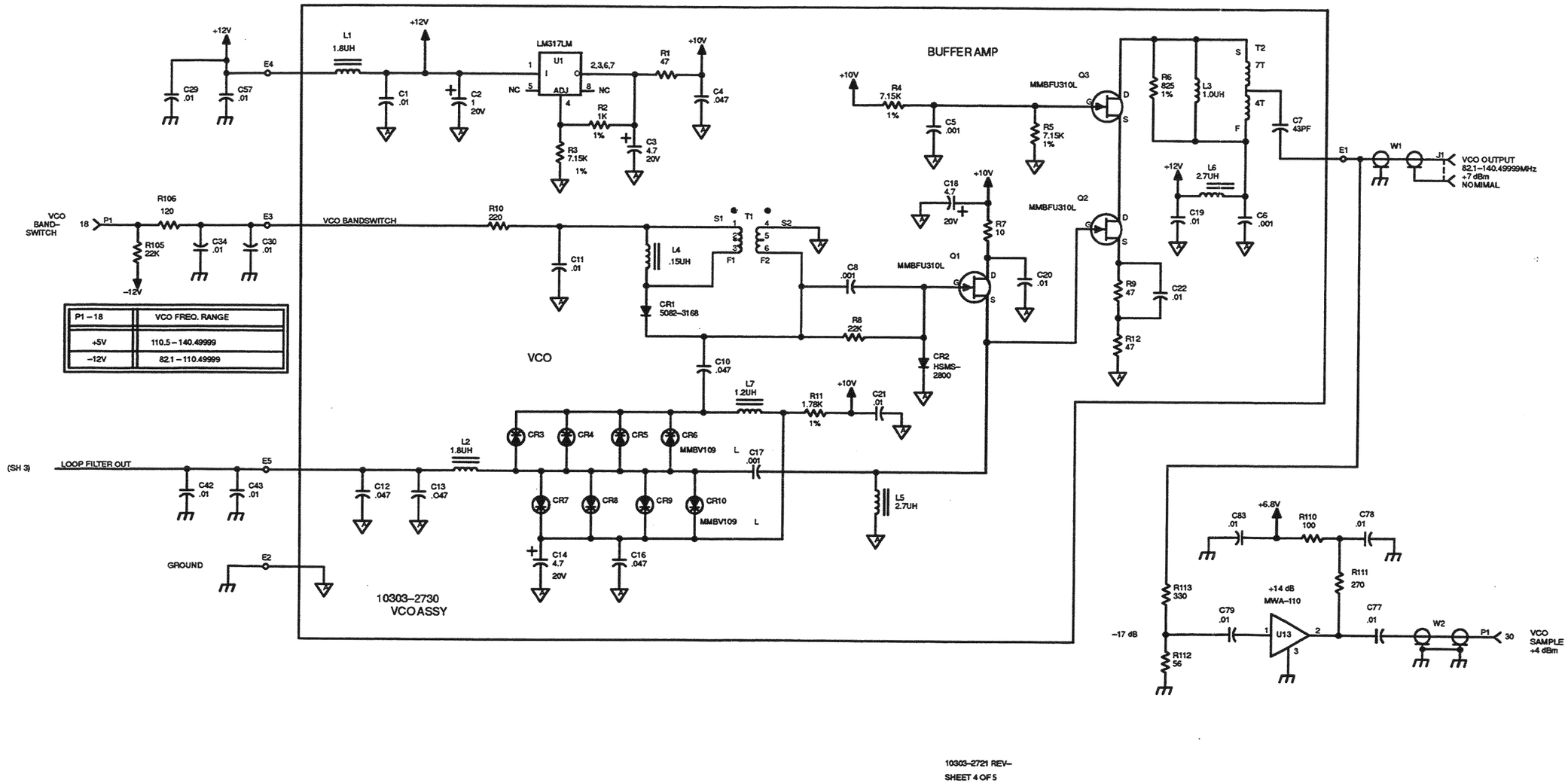
SHEET 3 OF 5

Figure 19. A6A2 Synthesizer Assembly Schematic Diagram (10303-2721 Rev. –) (Sheet 3 of 5)



P1 – 18	VCO FREQ. RANGE
+5V	110.5 – 140.49999
–12V	82.1 – 110.49999

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SHEET 4 OF 5

Figure 19. A6A2 Synthesizer Assembly Schematic Diagram (10303-2721 Rev. –) (Sheet 4 of 5)

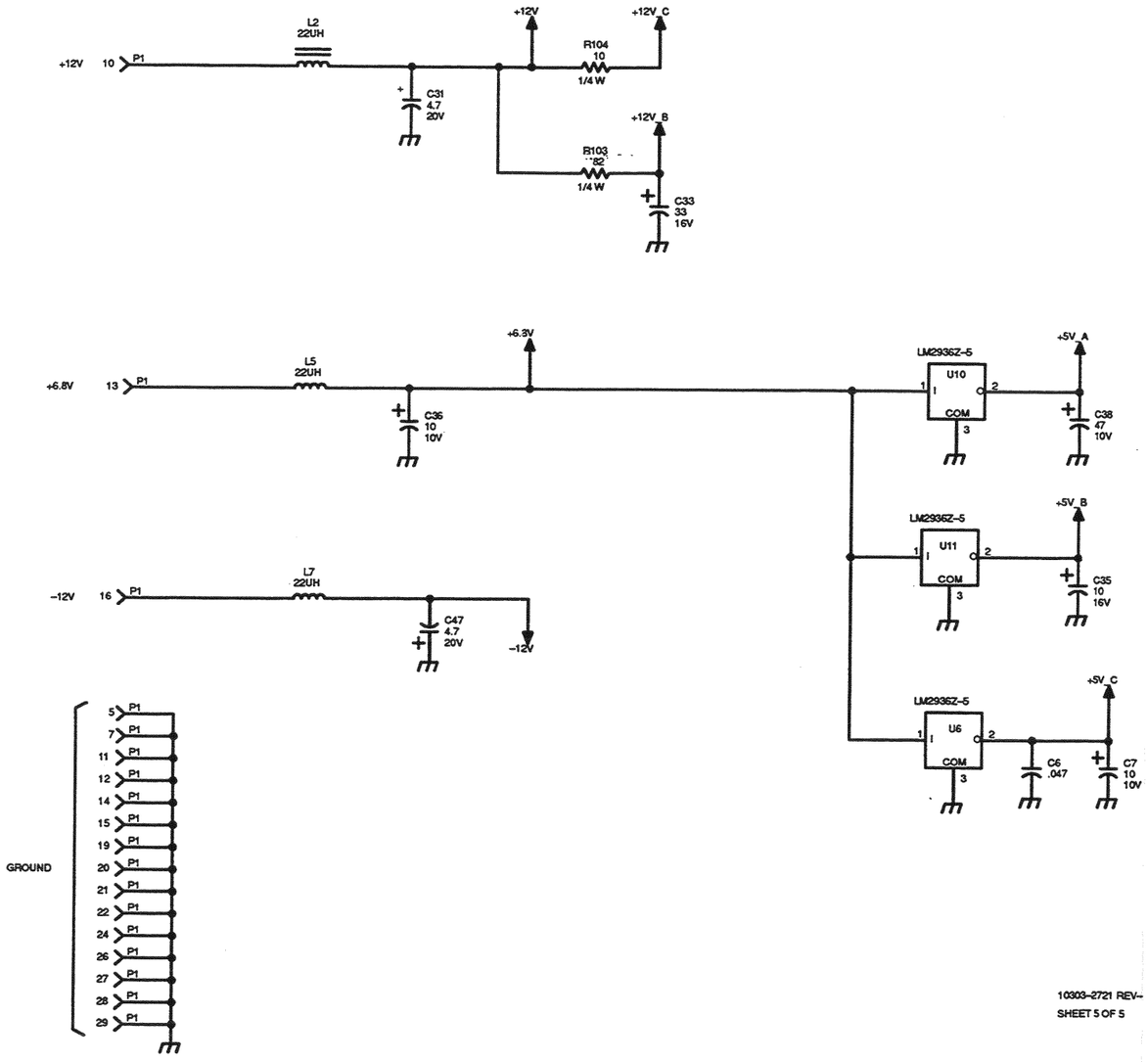


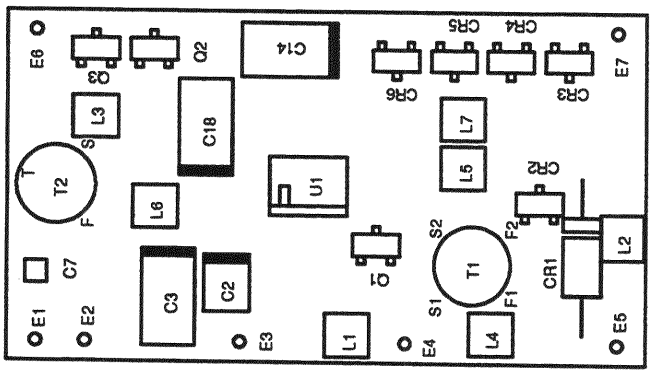
Figure 19. A6A2 Synthesizer Assembly Schematic Diagram (10303-2721 Rev. –) (Sheet 5 of 5)

Table 10. A6A2A1 VCO PWB Assembly Parts List (10303-2730 Rev. A)

Ref. Desig.	Part Number	Description
C1	C13-0103-103	CAP .01UF 10% 100V SMD
C2	C36-0120-105	CAP, KEMET, 1 UF, 20V
C3	C36-0120-475	CAP, KEMET, 4.7UF, 20V
C4	C13-0103-473	CAP .047UF 10% 100V SMD
C5	C13-0103-102	CAP 1000PF 10% 100V SMD
C6	C13-0103-102	CAP 1000PF 10% 100V SMD
C7	C11-0062-430	CAP 43PF 150V CER SMC
C8	C13-0103-102	CAP 1000PF 10% 100V SMD
C10	C13-0107-473	CAP .047 UF 250V CER SMC
C11	C13-0103-103	CAP .01UF 10% 100V SMD
C12	C13-0103-473	CAP .047UF 10% 100V SMD
C13	C13-0103-473	CAP .047UF 10% 100V SMD
C14	C36-0120-475	CAP, KEMET, 4.7UF, 20V
C16	C13-0107-473	CAP .047 UF 250V CER SMC
C17	C13-0101-102	CAP 1000PF 10% 100V SMD
C18	C36-0120-475	CAP, KEMET, 4.7UF, 20V
C19	C13-0103-103	CAP .01UF 10% 100V SMD
C20	C13-0103-103	CAP .01UF 10% 100V SMD
C21	C13-0103-103	CAP .01UF 10% 100V SMD
C22	C13-0103-103	CAP .01UF 10% 100V SMD
CR1	D10-3500-000	DIODE .25W 35V PIN BSW
CR2	D20-0005-001	DIODE, SOT-23
CR3	D25-0003-000	DIODE TUNING
CR4	D25-0003-000	DIODE TUNING
CR5	D25-0003-000	DIODE TUNING
CR6	D25-0003-000	DIODE TUNING
CR7	D25-0003-000	DIODE TUNING
CR8	D25-0003-000	DIODE TUNING
CR9	D25-0003-000	DIODE TUNING
CR10	D25-0003-000	DIODE TUNING
E1	E37-0002-005	TERMINAL
E2	E37-0002-005	TERMINAL
E3	E37-0002-005	TERMINAL
E4	E37-0002-005	TERMINAL
E5	E37-0002-005	TERMINAL
E6	E37-0002-005	TERMINAL
E7	E37-0002-005	TERMINAL
L1	L45-0005-182	COIL, 1.8UH,10%
L2	L45-0005-182	COIL, 1.8UH,10%

Table 10. A6A2A1 VCO PWB Assembly Parts List (10303-2730 Rev. A) (Cont.)

Ref. Desig.	Part Number	Description
L3	L45-0005-102	COIL, 1.0UH,10%
L4	L45-0005-151	COIL, .15U, 10%
L5	L45-0005-272	COIL, 2.7UH, 10%
L6	L45-0005-272	COIL, 2.7UH, 10%
L7	L45-0005-122	COIL, 1.2UH, 10%
Q1	Q35-0003-100	XSTR N-CH JFET U310 SOT
Q2	Q35-0003-100	XSTR N-CH JFET U310 SOT
Q3	Q35-0003-100	XSTR N-CH JFET U310 SOT
R1	R85-0125-470	RES 47 5% 1/8W FILM
R2	R85-0004-201	RES 1000 1% 1/8W FLM
R3	R85-0004-283	RES 7.15K 1% 1/8W SMD
R4	R85-0004-283	RES 7.15K 1% 1/8W SMD
R5	R85-0004-283	RES 7.15K 1% 1/8W SMD
R6	R85-0004-189	RES 825 1% 1/8W FLM
R7	R85-0125-100	RES 10 5% 1/8W FILM
R8	R85-0125-223	RES 22K 5% 1/8W FILM
R9	R85-0125-470	RES 47 5% 1/8W FILM
R10	R85-0125-221	RES 220 5% 1/8W FILM
R11	R85-0004-225	RES 1780 1% 1/8W FLM
R12	R85-0125-470	RES 47 5% 1/8W FILM
T1	10303-3107	OSCILLATOR TRANSFORMER
T2	10303-3124	OUTPUT TRANSFORMER
U1	I11-0015-008	REGULATOR, SM



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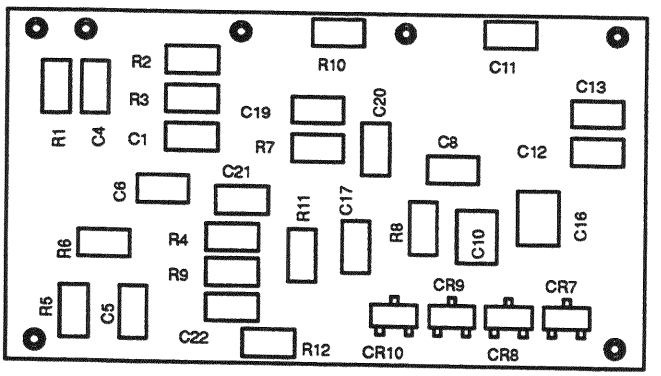
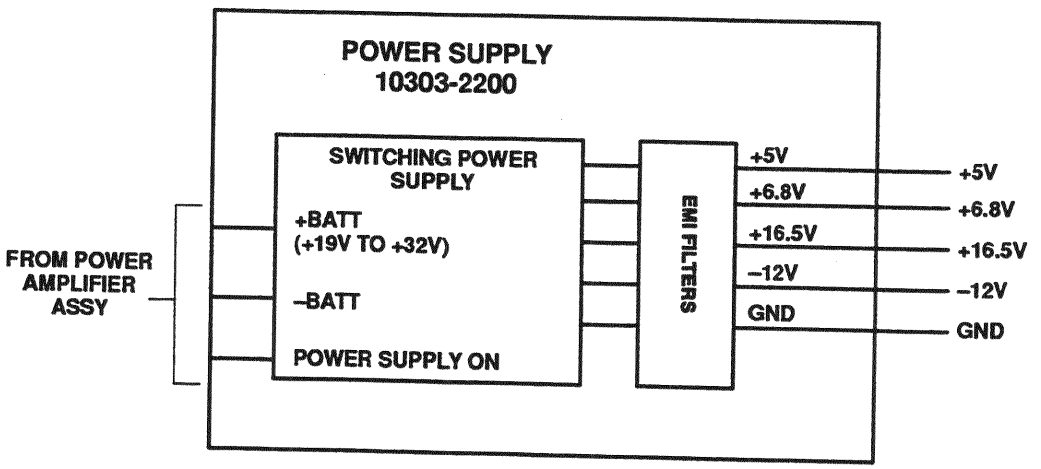


BOTTOM

Figure 20. A6A2A1 VCO Assembly Component Location Diagram (10303-2730 Rev. A)

A7
POWER SUPPLY



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A7 POWER SUPPLY

1. GENERAL DESCRIPTION

The A7 Power Supply Assembly generates the fixed-voltage supplies used throughout the RT-1694. A parts list, component location diagram, and schematic diagram can be found at the end of this section.

2. INTERFACE CONNECTIONS

The signals sent to and received by the A7 Power Supply Assembly are listed in table 1.

Table 1. A7 Power Supply Interface Connector Assignments

Connector and Pin	Signal	Comments
P1-1	+ Battery	
P1-2	+ Battery	
P1-3	Battery return	
P1-4	Battery return	
P1-5	Not Used	
P1-6	Ground	
P1-7	-12 V	
P1-8	Ground	
P1-9	+16.5 V	Unregulated
P1-10	Ground	
P1-11	Power supply On	Connected to + Battery to turn power supply on
P1-12	+6.8 V	Unregulated
P1-13	+5 V	
P1-14	+5 V	

3. TECHNICAL DESCRIPTION

3.1 Switching Power Supply

The supply voltages required by the transceiver are developed by a switching regulator, using pulse width modulation to provide the regulation. The circuit is a push-pull forward convertor using a center-tapped transformer with a MOSFET switch connected to each end of the primary, and the center tap connected to the positive supply (battery) voltage. The MOSFET switches (Q1 and Q2) are driven alternately by the complimentary outputs from pulse width modulator U1. This results in a symmetrical voltage across the primary of power transformer T1.

The main secondary winding of T1 is rectified and LC filtered to produce a dc voltage of +5 V. Synchronous rectifiers Q3 and Q4 are used instead of conventional diode rectifiers to reduce diode voltage drop losses, thereby increasing supply efficiency.

Voltage regulation is accomplished by feeding back the dc voltage from the LC filter output to regulator U1, where the feedback voltage is lowered to a stable voltage reference. The feedback voltage, –err is compared with a very stable, internally generated reference, 5V. The 5V is then lowered and input back as +err. The two voltages, –err and +err, are compared in U1 by a high gain error amplifier. The error amplifier output voltage is used as a reference in the pulse width modulator. The error voltage is compared to the oscillator ramp to produce an output

pulse proportional to the value of the error voltage. This produces a pulse train with the correct duty cycle to maintain a proper voltage at the output of the power supply. These pulses are then gated with the output of a steering flip-flop to produce two bi-phase signals that drive the power MOSFETS on the transformer primary, as well as the synchronous rectifiers on the transformer secondary. As line voltage or load is varied, the voltage feedback loop causes the duty cycle of the pulses to vary to maintain the correct output voltage.

Additional secondaries on T1 produce output voltages of +6.8 V and ±16.5 V. The +6.8 V supply has its own full wave rectifier (CR9 and CR10) and LC filter. The ±16.5 V supplies uses a full wave bridge rectifier (CR5 – 8) and separate LC filters. The –16.5 V supply feeds a –12 V linear regulator (U2). The unregulated output voltages are not within the voltage feedback loop; therefore, these outputs will vary with load, as well as with variations on the +5 V supply.

When the transceiver is powered on, the pulse width modulator IC initially receives its power from the PS ON line via Q5. The PS ON line also turns transistor switch Q6 on, so when the modulator is running, U1's power voltage comes from the +16.5 V output. This also causes the emitter-base junction of Q5 to be reversed biased, thus turning it off. Capacitor C7, connected to the soft start pin of U1, protects the power devices from power-on surge currents by limiting the duty cycle of the output pulses. The frequency of oscillation, which is determined by timing components C5 and R7, is 100 kHz.

3.2 Over-Current Protection

Current transformer T2 senses the current in the primary of power transformer T1. This produces a current sense voltage across R8, which is applied to the non-inverting input of the current sense comparator in U1. When this voltage reaches 100 mV, the outputs of the modulator are disabled.

4. TESTING AND ALIGNMENT

The A7 Power Supply Assembly is a non-repairable assembly. There are no testing and alignment procedures.

5. BITE FAULTS AND TROUBLESHOOTING

There are no bite faults or troubleshooting techniques associated with the A7 Power Supply Assembly.

6. PARTS LIST, COMPONENT LOCATION DIAGRAM, AND SCHEMATIC DIAGRAM

Tables 2 through 6 are the parts lists, and figures 1 and 2 are the component location diagrams for the A7A1 and A7A2 Power Supply Control PWB assemblies. Figure 3 is the schematic diagram for the A7 Power Supply Assembly.

Table 2. A7 Power Supply Assembly Parts List (10303-2200 Rev. E)

Ref. Desig.	Part Number	Description
—	10303-1025	CAN, POWER SUPPLY
—	10303-1205	COVER, POWER SUPPLY
—	10303-1036	INSULATOR, PS BOARDS
—	10303-1037	SUPPORT, PS BOARDS
—	10303-1077	FLEX CIRCUIT PS INTRCNCT
A1	10303-2450	PWN ASSY,POWER SUPPLY CTL
A2	10303-2460	PWB ASSY,POWER SUPPLY FLT
A3	10303-2470	PWB ASSY,PWR SUPPLY INTER
A4	10303-2210	PWB ASSY,PS INTERFACE
A5	10372-1220	FILTER ASSY, 6.8V
Z1	L50-0003-006	FERRITE BEAD
Z2	L50-0003-006	FERRITE BEAD
Z3	L50-0003-006	FERRITE BEAD
Z4	L50-0003-006	FERRITE BEAD
Z5	L50-0003-006	FERRITE BEAD
Z6	L50-0003-006	FERRITE BEAD
Z7	L50-0003-006	FERRITE BEAD

Table 3. A7A1 Power Supply Control PWB Assembly Parts List (10303-2450 Rev. C)

Ref. Desig.	Part Number	Description
—	P15-3145-001	SEALER RTV 3145 CLEAR
—	10303-2459	PWB, POWER SUPPLY
C1	M39014/02-1316V	CAP .22UF 10% 50V CER-R
C2	C13-0103-102	CAP 1000PF 10% 100V SMD
C3	C13-0103-473	CAP .047UF 10% 100V SMD
C4	C13-0103-103	CAP .01UF 10% 100V SMD
C5	C13-0105-122	CAP, 1200PF 5% 100V CHIP
C6	C13-0103-102	CAP 1000PF 10% 100V SMD
C7	C25-0133-684	CAP ELECT .68UF 35V
C8	C25-0132-155	CAP 1.5UF, 10% 25V
C9	C25-0132-155	CAP 1.5UF, 10% 25V
C11	C13-0103-471	CAP 470PF 10% 100V SMD
C12	C14-0001-106	CAP 10UF 50V MLC

Table 3. A7A1 Power Supply Control PWB Assembly Parts List (10303-2450 Rev. C) (Cont.)

Ref. Desig.	Part Number	Description
C14	C14-0001-106	CAP 10UF 50V MLC
C15	C13-0103-471	CAP 470PF 10% 100V SMD
C16	C13-0103-103	CAP .01UF 10% 100V SMD
CR2	1N4454	DIODE 200MA 75V SW
CR3	1N5804	DIODE, RECT UNITROD
CR4	1N5804	DIODE, RECT UNITROD
CR9	1N5804	DIODE, RECT UNITROD
CR10	1N5804	DIODE, RECT UNITROD
CR11	1N4454	DIODE 200MA 75V SW
CR12	1N4454	DIODE 200MA 75V SW
Q1	Q26-0040-002	XSTR MOSFET (IRFU120)
Q2	Q26-0040-002	XSTR MOSFET (IRFU120)
Q3	Q26-0022-001	XSTR, MOSFET (MTD10N05E-1)
Q4	Q26-0022-001	XSTR, MOSFET (MTD10N05E-1)
Q5	Q50-0017-001	XSTR, DARLINGTON (MJD122-1)
R1	R40-0016-202	RES VAR 2K OHM PCB
R2	R85-0004-201	RES 1000 1% 1/8W FLM
R3	R85-0004-266	RES, 4.75K 1% 1/8W CHIP
R4	R85-0004-366	RES 47.5K 1% 1/8W FLM
R5	R85-0004-330	RES 20.0K 1% 1/8W FLM
R6	R85-0004-234	RES 2.21K 1% 1/8W FLM
R7	R85-0004-271	RES, 5.36K 1% 1/8W CHIP
R8	R85-0125-027	RES 2.7 5% 1/8W SMD
R9	R85-0125-101	RES 100 5% 1/8W FILM
R10	R85-0125-223	RES 22K 5% 1/8W FILM
R11	R85-0125-220	RES 22 5% 1/8W FILM
R12	R85-0125-270	RES 27 5% 1/8W FILM
R13	R85-0125-102	RES 1.0K 5% 1/8W FILM
R14	R85-0004-166	RES 475 1% 1/8W SMD
R15	R85-0125-100	RES 10 5% 1/8W FILM
R16	R85-0125-270	RES 27 5% 1/8W FILM
R17	R85-0125-102	RES 1.0K 5% 1/8W FILM
R18	R85-0004-166	RES 475 1% 1/8W SMD
R19	R85-0125-100	RES 10 5% 1/8W FILM
R20	R12-0010-001	RES, .33 1/2W 1%
R21	R85-0125-470	RES 47 5% 1/8W FILM
R22	R85-0125-102	RES 1.0K 5% 1/8W FILM
R23	R85-0125-470	RES 47 5% 1/8W FILM
R24	R85-0125-102	RES 1.0K 5% 1/8W FILM

Table 3. A7A1 Power Supply Control PWB Assembly Parts List (10303-2450 Rev. C) (Cont.)

Ref. Desig.	Part Number	Description
R26	R85-0004-268	RES 4990 1% 1/8W FLM
R27	R85-0004-330	RES 20.0K 1% 1/8W FLM
R29	R85-0004-266	RES, 4.75K 1% 1/8W CHIP
T1	10303-3109	TRANSFORMER, POWER
T2	10303-3108	XFMR, CURRENT SENSOR
U1	I62-0012-002	IC, PWM CONTROL SG2526N
VR1	1N5242B	DIODE 12V 5% .5W ZENER
Z1	L50-0003-006	FERRITE BEAD

Table 4. A7A2 Power Supply Filter PWB Assembly Parts List (10303-2460 Rev. B)

Ref. Desig.	Part Number	Description
—	W10-0005-111	WIRE #24 BROWN PVC
—	W10-0005-333	WIRE #24 ORANGE PVC
—	W10-0005-444	WIRE #24 YELLOW PVC
—	W10-0005-555	WIRE #24 GREEN PVC
—	W10-0005-666	WIRE #24 BLUE PVC
—	W10-0005-777	WIRE #24 VIOLET PVC
—	W10-0005-888	WIRE #24 GRAY PVC
—	W10-0005-999	WIRE #24 WHITE PVC
—	W10-0005-000	WIRE #24 BLACK PVC
—	W10-0005-919	WIRE #24 WHITE/BROWN PVC
—	W10-0005-929	WIRE #24 WHITE/RED PVC
C13	C78-0040-107	CAP 100UF 20% 40V ELEC.
C17	C13-0103-103	CAP .01UF 10% 100V SMD
C18	C78-0016-391	CAP, ELECT 390UF 16V
C19	C78-0016-391	CAP, ELECT 390UF 16V
C21	C78-0016-391	CAP, ELECT 390UF 16V
C23	C78-0020-227	CAP 220UF 20% 20V ELEC.
C25	C78-0020-227	CAP 220UF 20% 20V ELEC.
C26	C25-0132-156	CAP ELECT 15UF 25V
CR1	D22-0030-001	DIODE,SCHOTTKY RECT 3A 40
CR5	D22-0026-004	DIODE, 1A 90V SCHOTTKY
CR6	D22-0026-004	DIODE, 1A 90V SCHOTTKY
CR7	D22-0026-004	DIODE, 1A 90V SCHOTTKY
CR8	D22-0026-004	DIODE, 1A 90V SCHOTTKY
CR13	1N5804	DIODE, RECT UNITROD
L2	10303-3106-01	TOROID 100UH
L3	10303-3106-04	TOROID 1MH
L4	10303-3106-02	TOROID 500UH

Table 4. A7A2 Power Supply Filter PWB Assembly Parts List (10303-2460 Rev. B) (Cont.)

Ref. Desig.	Part Number	Description
L5	10303-3106-03	TOROID 500UH
Q6	Q12-2222-101	XSTR NPN SWG SM SS/GP
R25	R85-0125-027	RES 2.7 5% 1/8W SMD
R28	R85-0125-223	RES 22K 5% 1/8W FILM
T3	10303-3125	CHOKE, COMMON-MODE
U2	I10-0003-212	REG,-12V (MC79M12CDT-1)

Table 5. A7A3 Power Supply Interface PWB Assembly Parts List (10303-2470 Rev. A)

Ref. Desig.	Part Number	Description
—	10303-2479	PWB, P.S. INTERFACE
—	10303-1043	PIN, SOLDER

Table 6. A7A4 Power Supply Interface PWB Assembly Parts List (10303-2210 Rev. B)

Ref. Desig.	Part Number	Description
—	10303-2219	PWB DETAIL
C1	C14-0001-185	CAP 1.8UF 50V
C2	C14-0001-185	CAP 1.8UF 50V
C3	C14-0000-225	CAP 2.2UF MLC
C4	C14-0000-225	CAP 2.2UF MLC
C5	C14-0000-225	CAP 2.2UF MLC
C6	C14-0000-225	CAP 2.2UF MLC
C8	C13-0103-473	CAP .047UF 10% 100V SMD
P1	J46-0084-314	HEADER 14 POS DUAL ROW

Table 7. A7A5 6.8 V Filter Assembly Parts List (10372-1220 Rev. B)

Ref. Desig.	Part Number	Description
—	10372-1229	PWB
—	W10-0005-222	WIRE #24 RED PVC
—	W60-0005-002	WIRE TFE 22GA 200 DEG
—	W20-0001-0140	14 BUSS WIRE
—	C78-0053-122	CAPACITOR, 1200UF, 16V

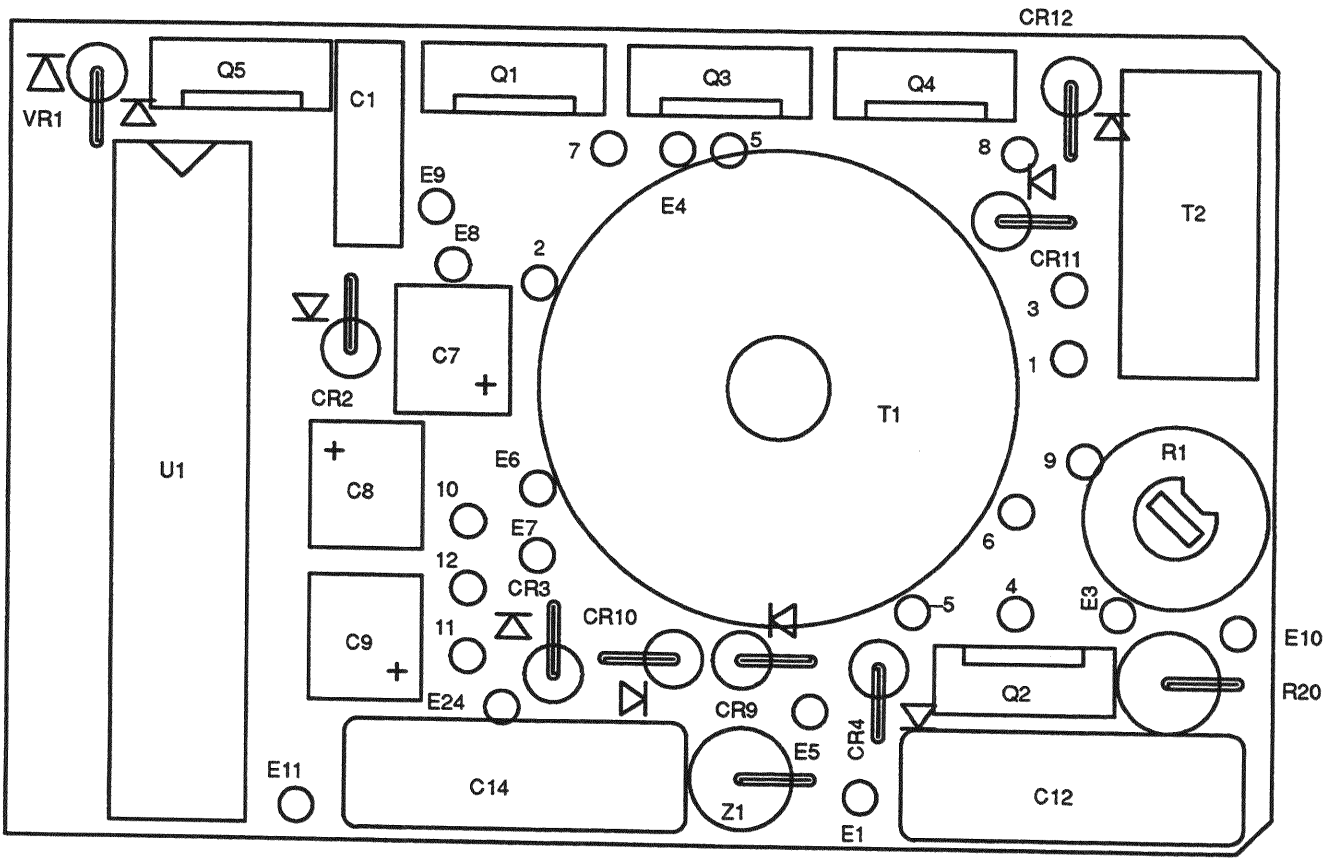


Figure 1. A7A1 Power Supply Control PWB Assembly Component Location Diagram (10303-2450 Rev. A) (Sheet 1 of 2)

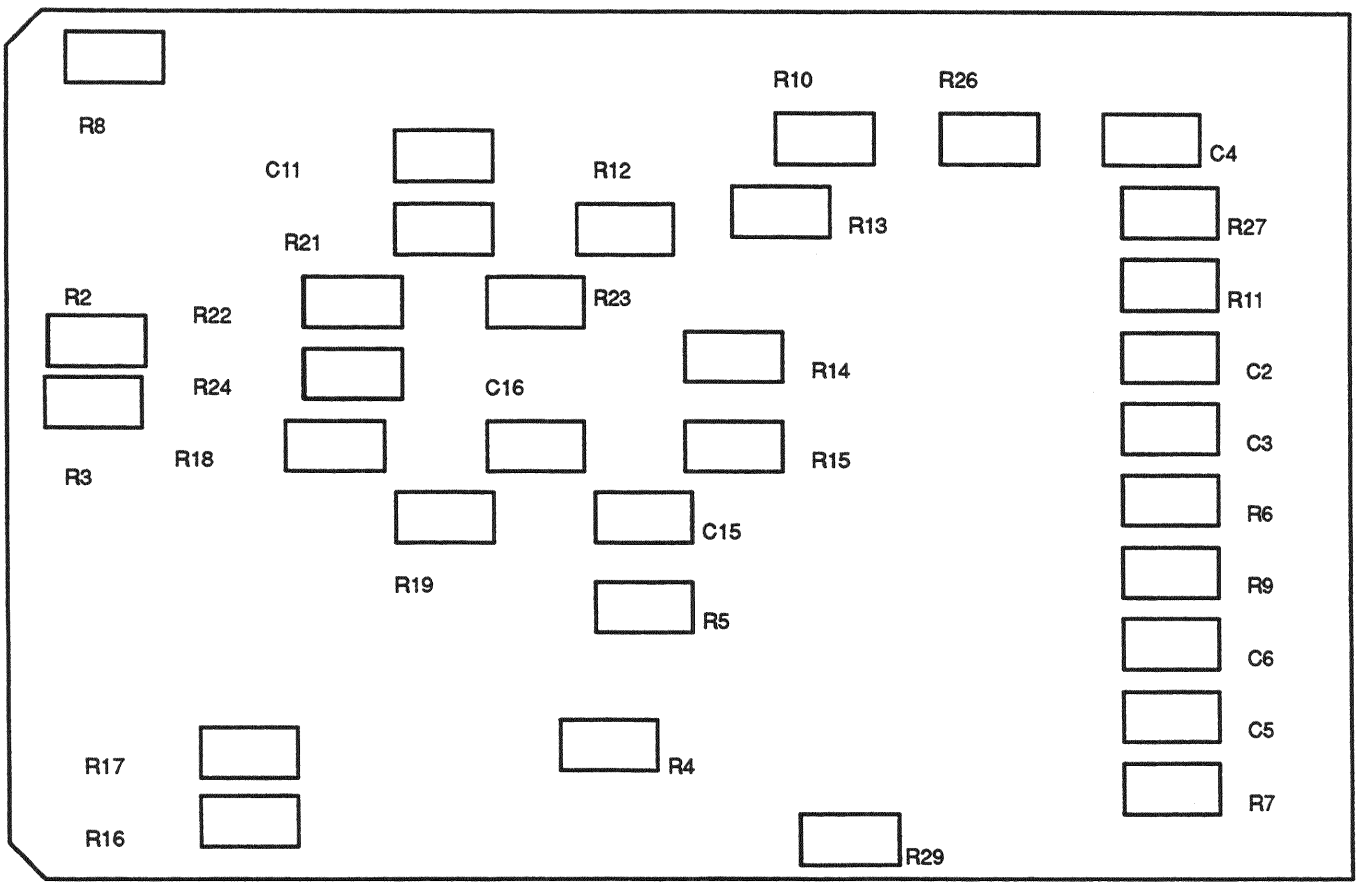


Figure 1. A7A1 Power Supply Control PWB Assembly Component Location Diagram (10303-2450 Rev. A) (Sheet 2 of 2)

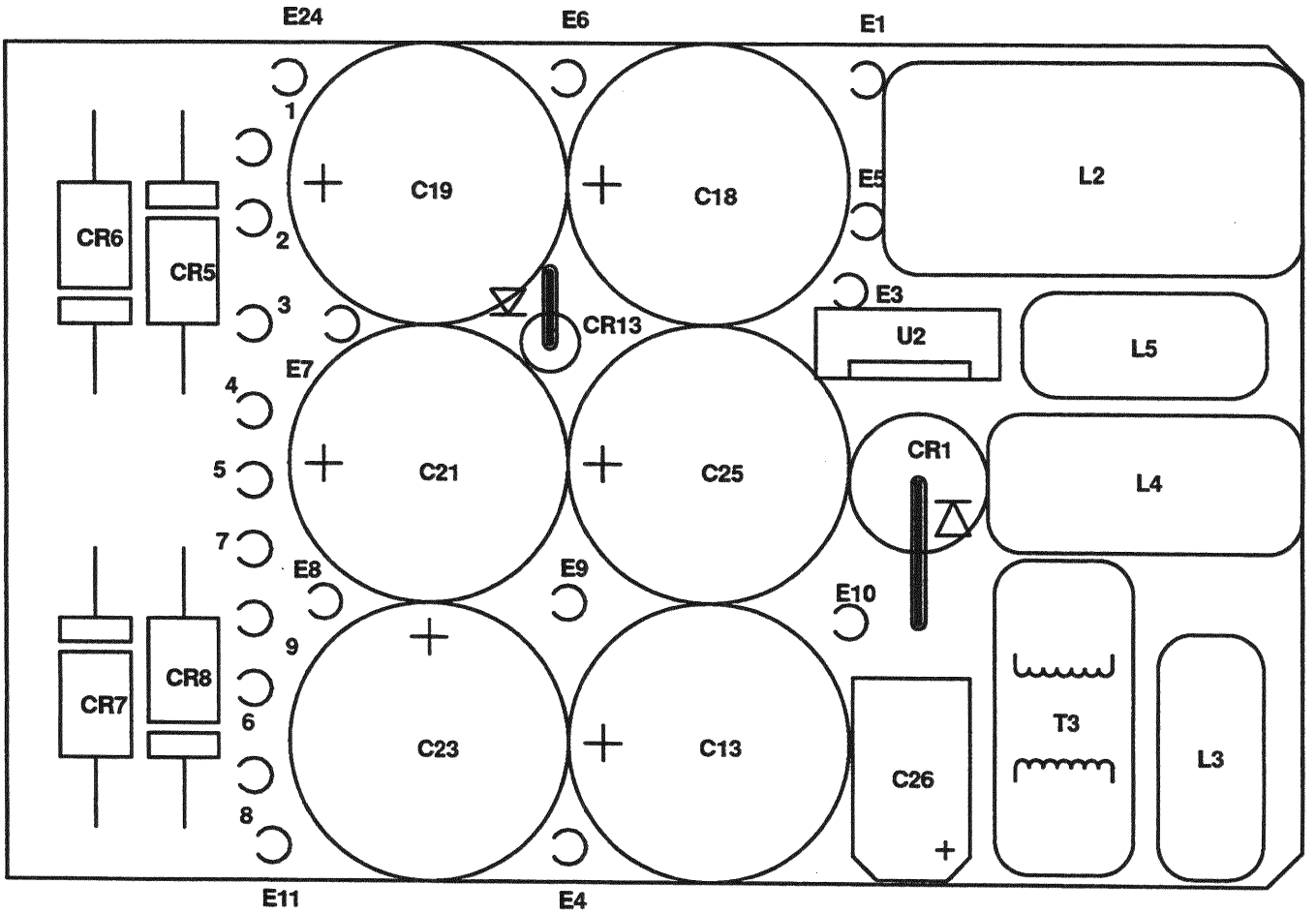


Figure 2. A7A2 Power Supply Filter PWB Assembly Component Location Diagram (10303-2460 Rev. B) (Sheet 1 of 2)

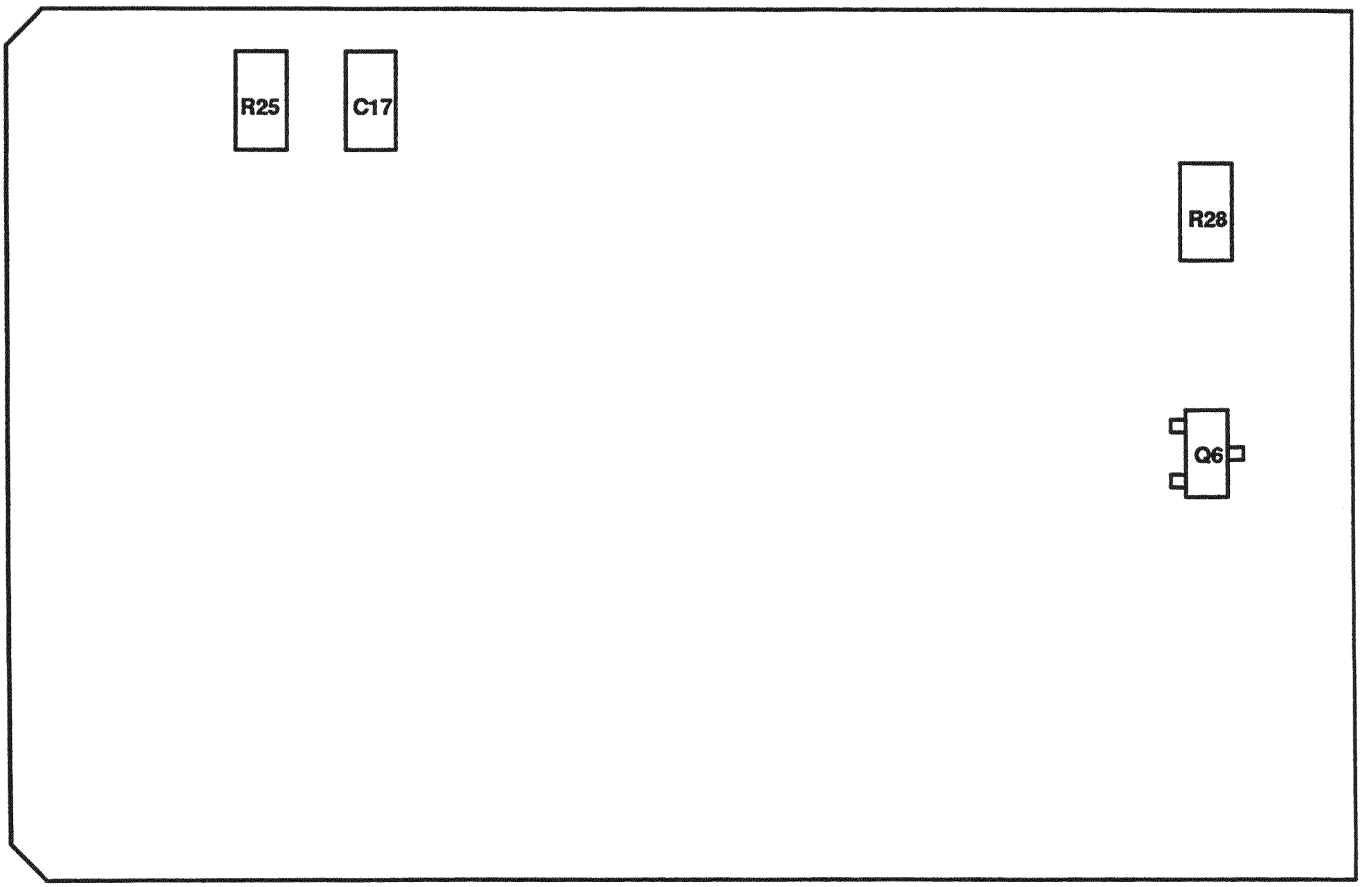
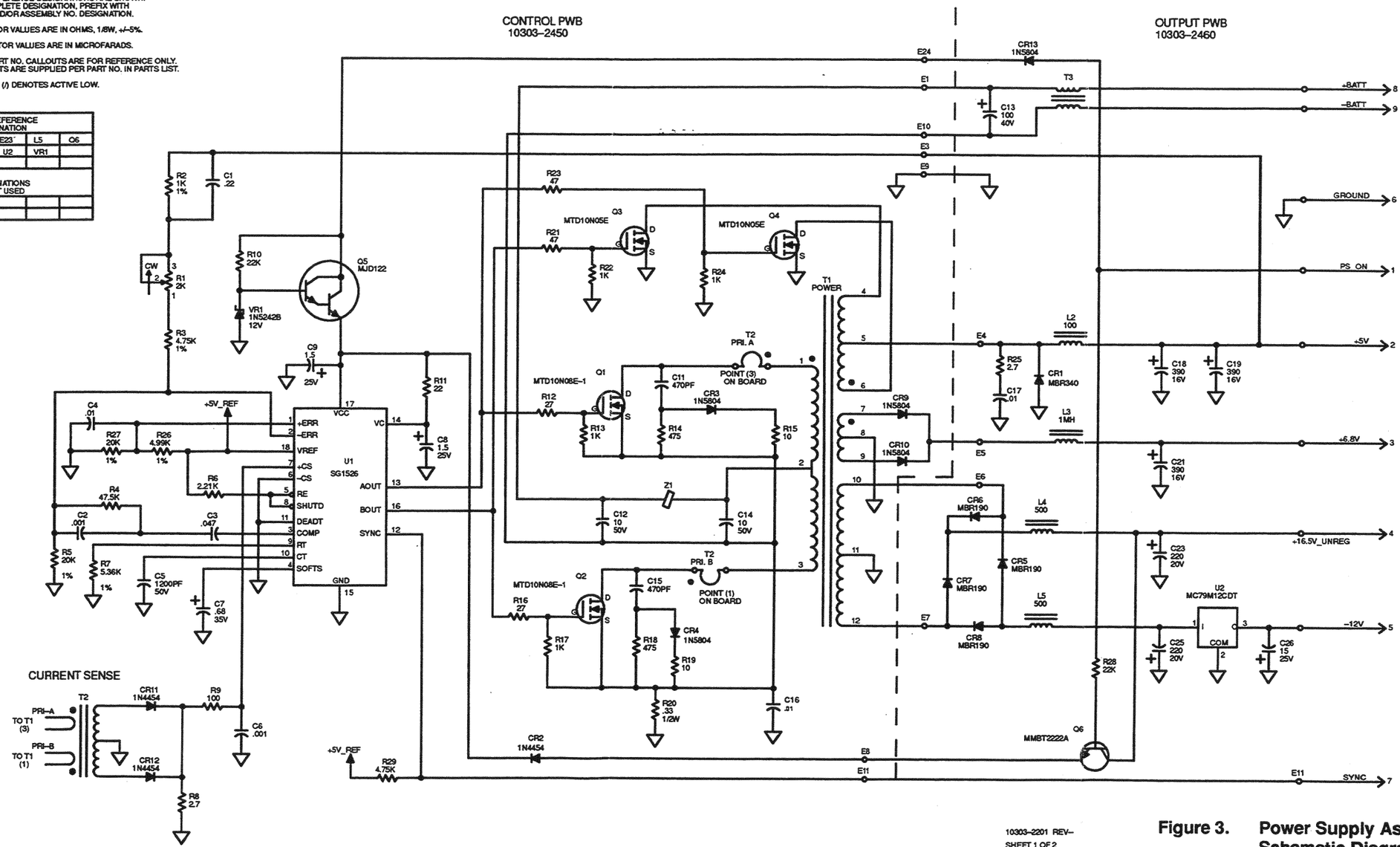


Figure 2. A7A2 Power Supply Filter PWB Assembly Component Location Diagram (10303-2460 Rev. B) (Sheet 2 of 2)

NOTE: UNLESS OTHERWISE SPECIFIED:

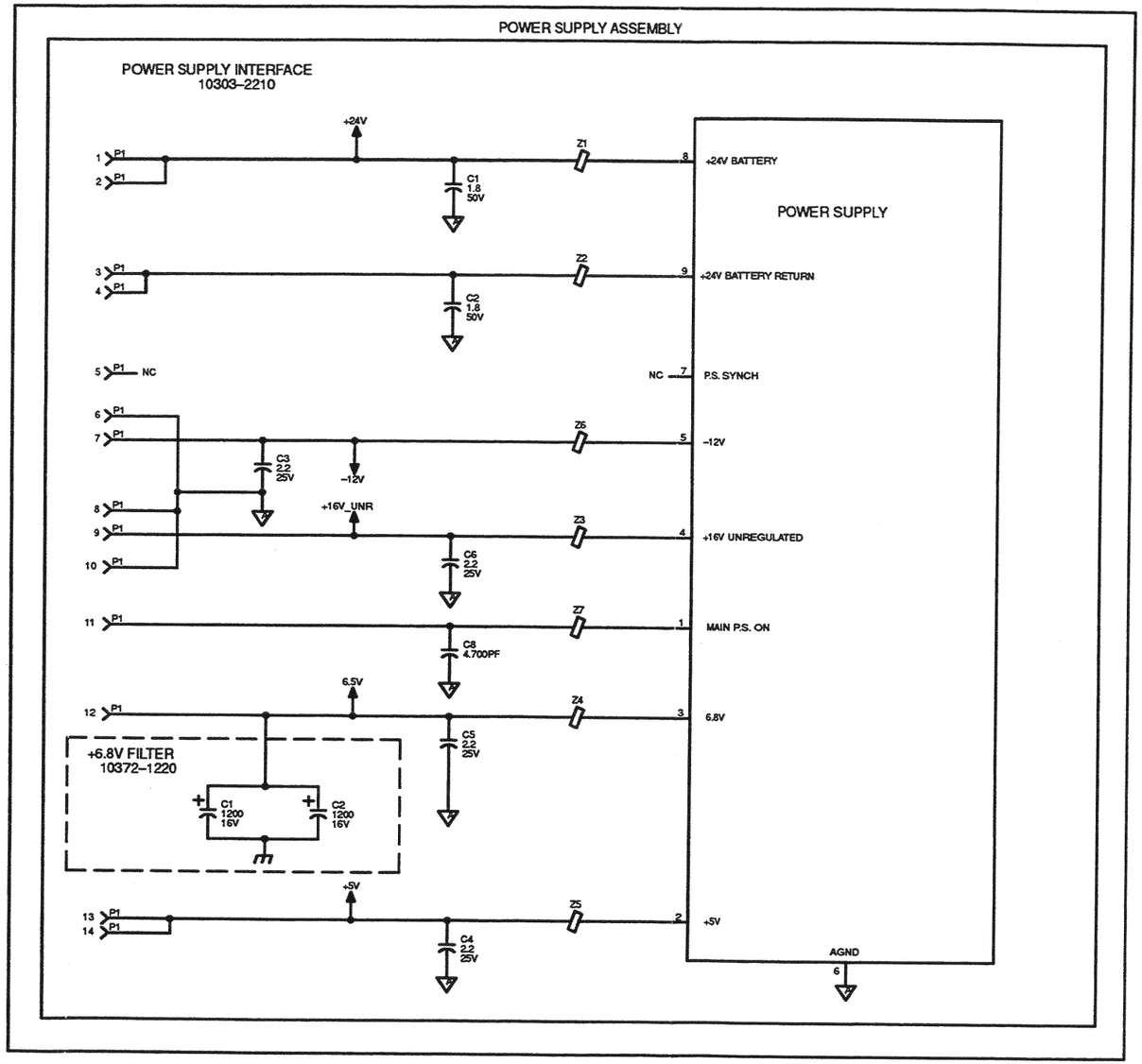
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR A COMPLETE DESIGNATION, PREFIX WITH UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.
2. ALL RESISTOR VALUES ARE IN OHMS, 1/8W, +/-5%.
3. ALL CAPACITOR VALUES ARE IN MICROFARADS.
4. VENDOR PART NO. CALLOUTS ARE FOR REFERENCE ONLY. COMPONENTS ARE SUPPLIED PER PART NO. IN PARTS LIST.
5. BACKSLASH (/) DENOTES ACTIVE LOW.

HIGHEST REFERENCE DESIGNATION				
C27	CR13	E23	L5	Q6
R29	T3	U2	VR1	
REF. DESIGNATIONS NOT USED				



10303-2201 REV-
SHEET 1 OF 2

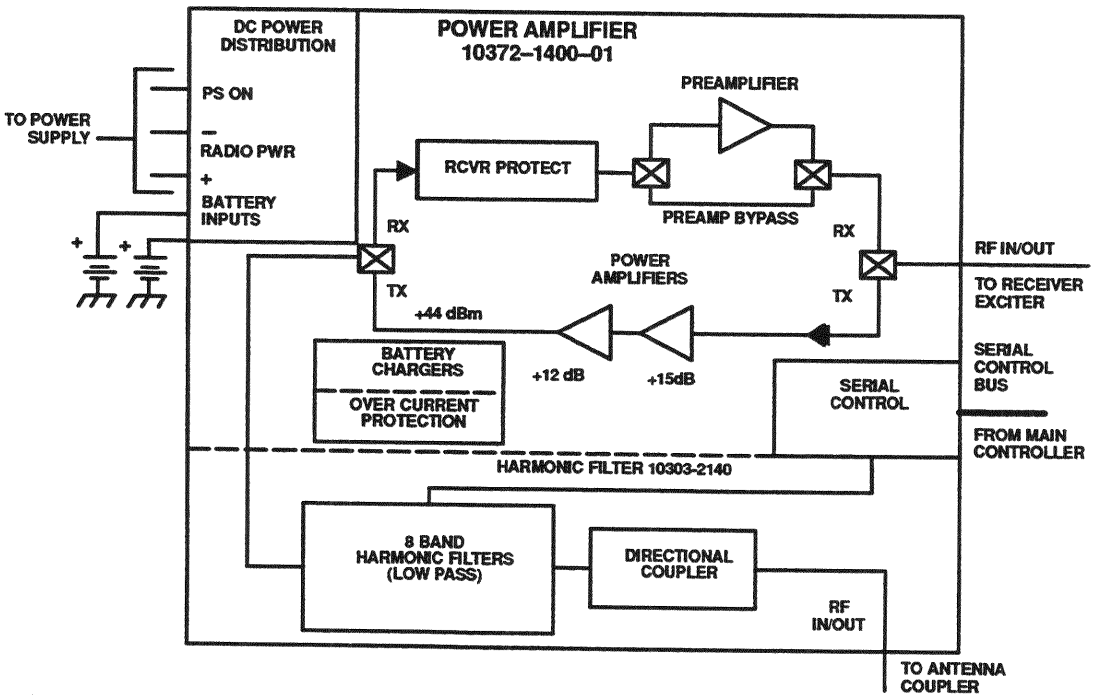
Figure 3. Power Supply Assembly Schematic Diagram (10303-2201 Rev. –) (Sheet 1 of 2)



10303–2201 REV–
SHEET 2 OF 2

Figure 3. Power Supply Assembly Schematic Diagram (10303-2201 Rev. –) (Sheet 2 of 2)

A8
POWER AMPLIFIER/BATTERY CHARGER



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A8 POWER AMPLIFIER/BATTERY CHARGER ASSEMBLY

1. GENERAL DESCRIPTION

The A8 Power Amplifier/Battery Charger Assembly (10372-1400) consists of the following subassemblies:

- A8A1 RF Power Amplifier/Battery Charger PWB Assembly (10303-2130)
- A8A2 Harmonic Filter PWB Assembly (10303-2140)

The RF Power Amplifier takes a nominal 50 mW RF signal from the A5 Receiver/Exciter Assembly and amplifies the signal up to 25 W in the transmit mode. In the receive mode, the RF Power Amplifier Assembly performs the receiver protection function as well as a selectable RF preamplifier function. The RF Power Amplifier also performs the functions of DC input power distribution and charging batteries attached to the radio. The A8 Assembly is digitally controlled by the A4 Signal Processor Assembly. Additionally, the A4 Signal Processor is provided with status information about the RF Power Amplifier. Figure 1 is a block diagram of the A8 Power Amplifier/Battery Charger Assembly.

1.1 Transmit Signal Path

Transmit RF signals in the 1.6 MHz to 60 MHz frequency range from the A5 Receiver/Exciter Assembly are routed through the RF Power Amplifier. The RF Power Amplifier consists of two stages that amplify the exciter RF from 50 mW to the 25 W power level. Transmit RF signals then pass through one of eight harmonic filters to reduce the level of the unwanted harmonics. Finally, the transmit RF passes through a directional coupler which provides a sample of the RF level to the A4 Signal Processor Assembly to control the transmit output power level. The transmit RF signals then leave the RF Power Amplifier Assembly and go to the A9 Antenna Coupler Assembly.

1.2 Receive Signal Path

Receive RF signals in the 1.6 MHz to 60 MHz frequency range come from the A9 Antenna Coupler Assembly. The receive signals first pass through the harmonic filters in the reverse order from the transmit signal path. Next, the receive signal passes through a receiver protection circuit that limits the receive signals that are greater than +7dBm to a level that is safe for the A5 Receiver/Exciter. A user-selectable RF preamplifier with a gain of 13 dB is the final function performed on the receive signal before leaving the RF Power Amplifier Assembly and going to the A5 Receiver/Exciter Assembly.

1.3 Input Power Distribution

The A8 Power Amplifier/Battery Charger Assembly also performs input power distribution from all possible input power sources to the assemblies that require +24 V. The sources are the two batteries that connect to the A8 Power Amplifier/Battery Charger Assembly as well as the external R/T power and battery charger power that come from the A10 Front Panel Assembly external PA I/O connector. These various sources are combined/routed appropriately to the various assemblies which require the use of +24 V by diode ORing the batteries and external R/T power. The assemblies that require +24 V are the A5 Receiver/Exciter, A7 Power Supply, A9 Antenna Coupler, and A10 Front Panel. The battery charger power is used solely by the internal battery chargers of the A8 Power Amplifier/Battery Charger Assembly.

1.4 Battery Chargers

The A8 Power Amplifier/Battery Charger Assembly has two internal battery chargers designed to charge the BB-590 Nickel-Cadmium batteries that are used with the radio. The battery chargers trickle charge the batteries at 180 mA in 14 to 16 hours. These chargers are independent of each other and attempt to charge only if a BB-590 is attached to the respective battery connector.

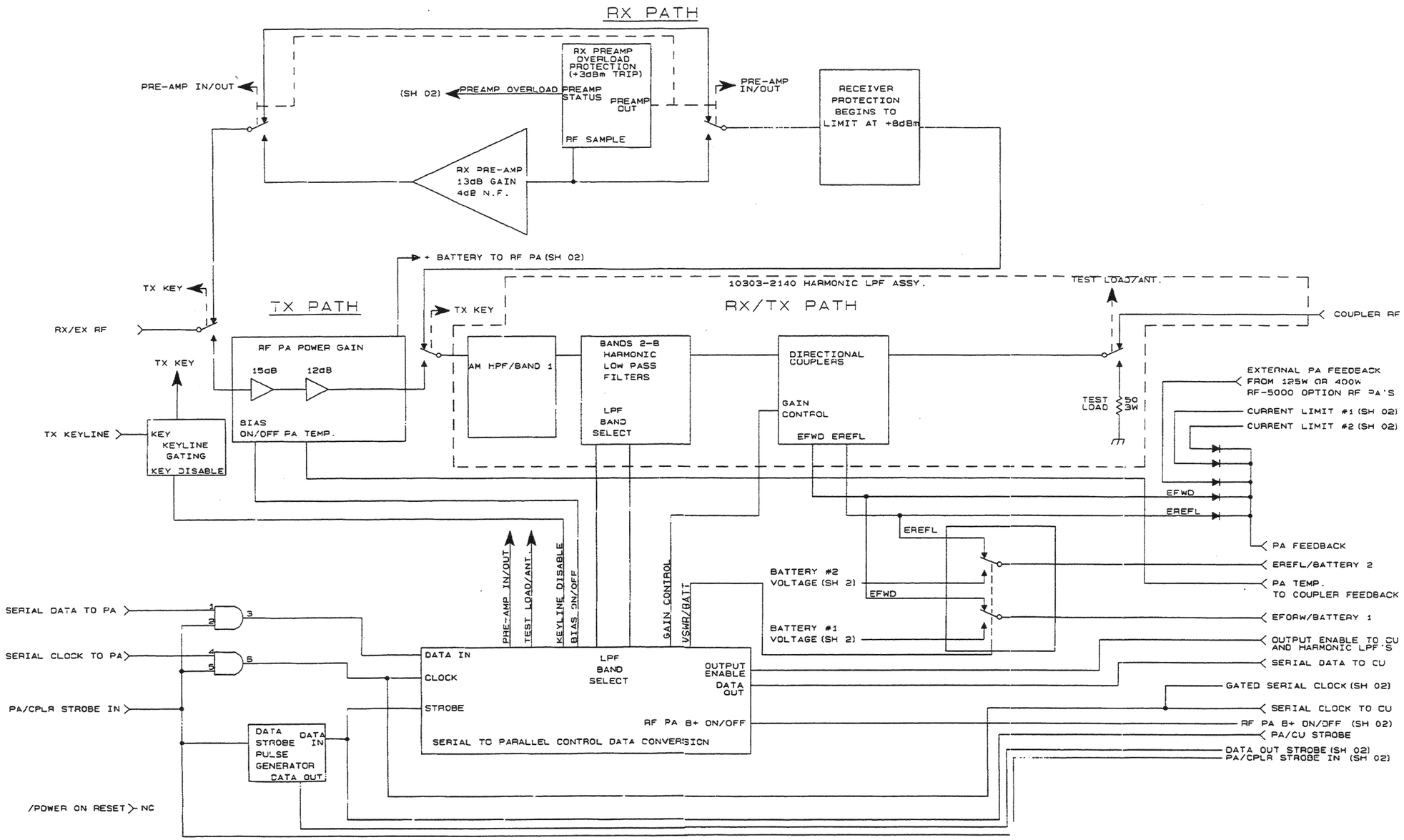


Figure 1. A8 Power Amplifier/Battery Charger Assembly Block Diagram (Sheet 1 of 2)

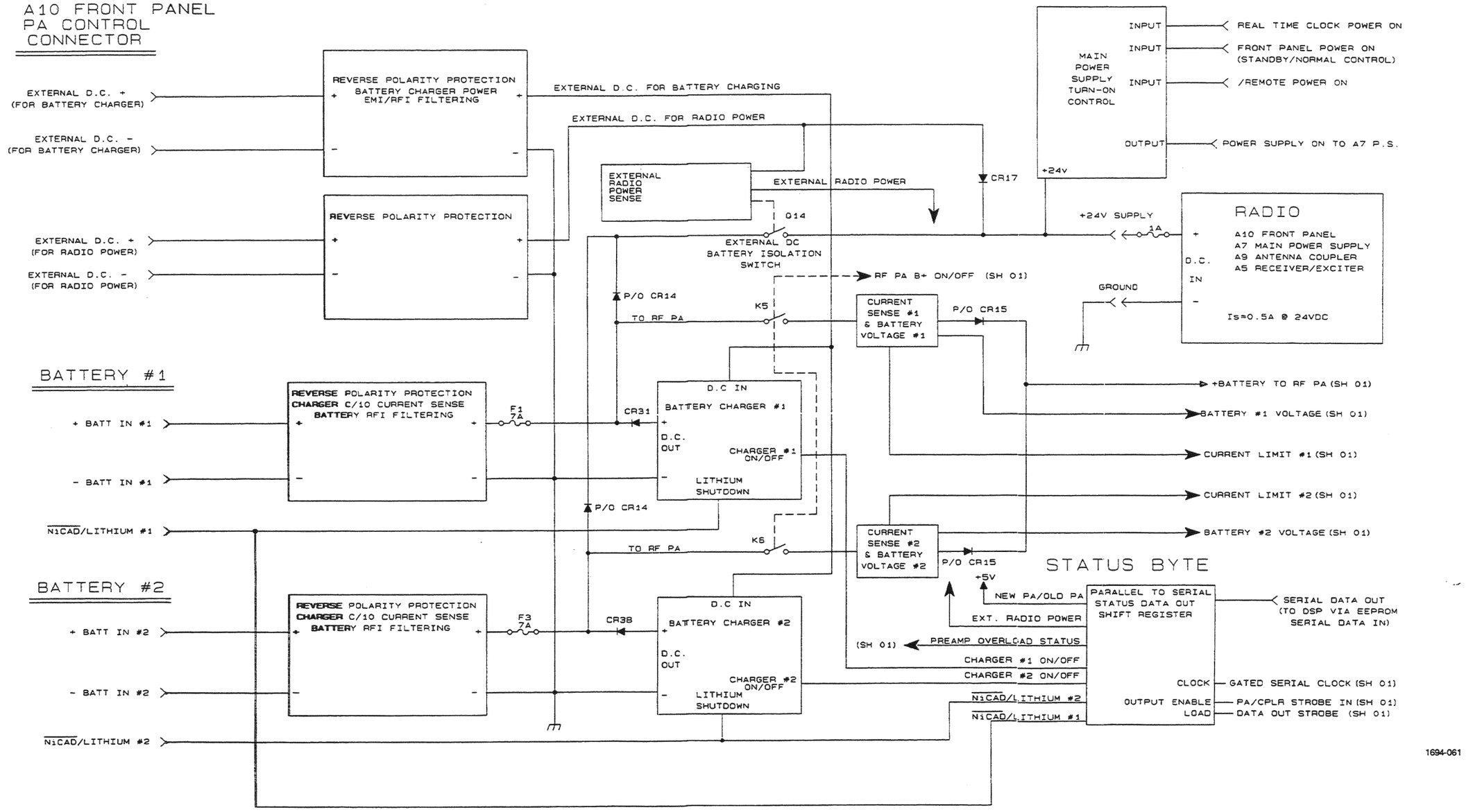


Figure 1. A8 Power Amplifier/Battery Charger Assembly Block Diagram (Sheet 2 of 2)

2. INTERFACE CONNECTIONS

Tables 1 and 2 list the signals sent to and received by the A8 Power Amplifier/Battery Charger Assembly.

Table 1. A8A1 RF Power Amplifier/Battery Charger Assembly Interface Connector Assignments

Connector and Pin	Signal	Comments
P1-1	Charger DC +	10–32 Vdc, dc power in to operate battery chargers.
P1-2	Charger DC +	10–32 Vdc, dc power in to operate battery chargers.
P1-3	Charger DC Return	0 V, dc return for battery charger power.
P1-4	Charger DC Return	0 V, dc return for battery charger power.
P1-5	Radio DC +	18–32 Vdc, dc power in to operate radio as Receiver/Exciter.
P1-6	Radio DC Return	0 V, dc return for radio power.
P1-7	Radio DC Return	0 V, dc return for radio power.
P1-8	/RMT Power On	0 V-32 Vdc 1.5 mA maximum, Zin = 22 K, ground closure to turn on radio main power supply, pulled up to battery voltage.
P1-9	Main/Standby	0 V/5 V, Rin = 22.1 K, 5 V will cause main power supply to turn on, 0 V will turn off main power supply.
P1-10	RTC Power On	0 V/5 V, Rin = 22.1 K, 5 V will cause main power supply to turn on, 0 V will turn off main power supply.
P1-11	Main PS On	0 V–32 Vdc, 0.2 amps maximum, open collector, + battery voltage is applied to turn on main power supply.
P1-12	B+ to Radio	18 V–32 Vdc, dc to run radio except for RF PA Assembly.
P1-13	B+ to Radio	8 V–32 Vdc,dc to run radio except for RF PA Assembly.
P1-14	+5 V	+5 Vdc, 50 mA maximum, +5 V from power supply to run logic and diode bias.
P1-15	–12 V	–12 Vdc, 50 mA maximum, –12 V from power supply to run analog circuits.
P1-16	+16 V	+16 Vdc, 50 mA maximum, +16 V from power supply to run analog circuits.
P1-17	HSSB/Power on Reset	0 V/5 V, 350 Kbaud asynch, not used at this time.
P1-18	Ground	0 V, ground for all circuits in radio (along with chassis ground).

Table 1. A8A1 RF Power Amplifier/Battery Charger Assembly Interface Connector Assignments (Cont.)

Connector and Pin	Signal	Comments
P1-19	Ground	0 V, ground for all circuits in radio (along with chassis ground).
P1-20	External PA Feedback	0 V–7 VDC, Rin = 100K, analog feedback from external RF PA for TGC loop, nominal of 4.3 V.
P1-21	Power Off Protect	0 V/5 V, Rin = 57 K, active high signal used to throw test load relay on Filter Assembly when MODE control is off.
P1-22	PA Temperature	0 V–5 V, Rout = 6 K, dc analog level to indicate RF output transistor temperature.
P1-23	PA Feedback	0 V–7 Vdc, Zout = Op-amp output, analog signal to provide feedback to TGC loop for transmitter power control.
P1-24	EREFL/Battery #2	0 V–6 Vdc, Zout = 100 (EREFL) Zout = 2 K (battery #2 voltage) analog signal that is either a sample of reflected RF power or battery #2 voltage.
P1-25	EFWD/Battery #1	0 V–6 VDC, Zout = 100 (EREFL Zout = 2 K (battery #1 voltage) analog signal that is either a sample of forward RF power or battery #1 voltage.
P1-26	TX Keyline	0 V/5 V, 5 V active, switches PA RF from RX path to TX path.
P1-27	Serial Data Out	0 V/5 V Zout = 100, 100 pF CMOS gate, gated serial control data to coupler.
P1-28	Output Enable	0 V/5 V Zout = 100, 100 pF CMOS gate, active low pulse to enable relay driver ICs outputs.
P1-29	Serial Clock Out	0 V/5 V Zout = CMOS gate output, gated serial control data clock.
P1-30	Data Strobe Out	0 V/5 V Zout = CMOS gate output, active high pulse to latch serial control data.
P1-31	Status Data Out	0 V/5 V Zout = 100, 100 pF CMOS gate serial data to provide RF PA/charger status.
P1-32	PA/CPLR Strobe	0 V/5 V Zin = 2 K CMOS gate, 100 pf, active low strobe, to be held low during entire transfer of serial control data.
P1-33	Serial Data In	0 V/5 V Zin = 100, 100 pf CMOS gate serial control data in, must be inverted by DSP Assembly before sending.
P1-34	Serial Clock	0 V/5 V Zin = 100, 100 pf, CMOS gate, clock for serial control data.
J4-1	Serial Clock	+5/0 V, 2 CMOS gate inputs, gated serial clock for control data.

Table 1. A8A1 RF Power Amplifier/Battery Charger Assembly Interface Connector Assignments (Cont.)

Connector and Pin	Signal	Comments
J4-2	Serial Data Out	+5/0 V, 2 CMOS gate inputs, gated serial control data.
J4-3	LPF Data Strobe	+5/0 V, 2 CMOS gate inputs, strobe to latch serial control data, 5 V active.
J4-4	Serial Data Out	+5/0 V, CMOS gate output, gated serial control data to coupler.
J4-5	Output Enable	+5/0 V, 2 CMOS gate inputs, strobe to enable relay driver outputs, 0 V active.
J4-6	Spare	No connect.
J4-7	+24 V	+24 Vdc, power to run relay drivers.
J4-8	+12 V	+12 Vdc, power to run analog circuits.
J4-9	–12 V	–12 Vdc, power to run analog circuits.
J4-10	Ground	0 V, ground for control and filters.
J4-11	PA Feedback	0.5 V – 7 V, analog feedback for PA power control.
J4-12	Ground	0 V, ground for control and filters.
J4-13	E Forward	0.5 V – 7 V, Zout = 100 ohm, analog level indicating RF forward power to load.
J4-14	E Reflected	0.5 V – 7 V, Zout = 100 ohm, analog level indicating RF reflected power from load.
J4-15	Ground	0 V, ground for control and filters.
J4-16	Gain Control	5 V/float, control for 100 mw/20 W mode, 5 V for 100 mW mode.
J4-17	Preamp In	0 V/24 V, relay control for RF preamp, 24 V active.
J4-18	Preamp Out	0 V/24 V, relay control for RF preamp, 24 V active.
J4-19	Power Off Protect	0 V/5 V, Rin = 57 Kohms, active high from front panel to set test load relay to protect receiver when mode is set to off.
J4-20	+5 V	+ 5 V, power for digital circuits.
J4-21	Spare	No connect.
J4-22	Spare	No connect.
J5-1	Battery #1 Return	0 V – 1 V, 5 amps maximum, negative return for Battery #1.
J5-2	Lithium/Ni-Cd #1	0 V/5 V, 2 mA maximum, control signal to sense battery type, 0 V = Ni-Cd.
J5-3	Mechanical Key	This pin is used with a mechanical dummy plug to avoid misconnection.

Table 1. A8A1 RF Power Amplifier/Battery Charger Assembly Interface Connector Assignments (Cont.)

Connector and Pin	Signal	Comments
J5-4	Battery #1	18 – 32 Vdc, 5 amps maximum, Battery #1 output voltage to power entire radio.
J6-1	Battery #2 Return	0 V – 1 V, 5 amps maximum, negative return for Battery #2.
J6-2	Lithium/Ni-Cd #2	0 V/5 V, 2 mA maximum, control signal to sense battery type, 0 V = Ni-Cd.
J6-3	Mechanical Key	This pin is used with a mechanical dummy plug to avoid misconnection.
J6-4	Battery #2	18 – 32 Vdc, 5 amps maximum, Battery #2 output voltage to power entire radio.

Table 2. A8A2 Harmonic Filter Assembly Interface Connector Assignments

Connector and Pin	Signal	Comments
P1-1	Serial Clock	+5/0 V, 2 CMOS gate inputs, gated serial clock for control data.
P1-2	Serial Data Out	+5/0 V, 2 CMOS gate inputs, gated serial control data.
P1-3	LPF Data Strobe	+5/0 V, 2 CMOS gate inputs, strobe to latch serial control data, 5 V active.
P1-4	Serial Data Out	+5/0 V, CMOS gate output, gated serial control data to coupler.
P1-5	Output Enable	+5/0 V, 2 CMOS gate inputs, strobe to enable relay driver outputs, 0 V active.
P1-6	Spare	No connect.
P1-7	+24 V	+ 24 Vdc, power to run relay drivers.
P1-8	+12 V	+12 Vdc, power to run analog circuits.
P1-9	–12 V	–12 Vdc, power to run analog circuits.
P1-10	Ground	0 V, ground for control and filters.
P1-11	PA Feedback	0.5 V – 7 V, analog feedback for PA power control.
P1-12	Ground	0 V, ground for control and filters.
P1-13	E Forward	0.5 V – 7 V, Zout = 100 ohm, analog level indicating RF forward power to load.
P1-14	E Reflected	0.5 V – 7 V, Zout = 100 ohm, analog level indicating RF reflected power from load.
P1-15	Ground	0 V, ground for control and filters.

Table 2. A8A2 Harmonic Filter Assembly Interface Connector Assignments (Cont.)

Connector and Pin	Signal	Comments
P1-16	Gain Control	5 V/float, control for 100 mW/20 W mode, 5 V for 100 mW mode.
P1-17	Preamp In	0 V/24 V, relay control for RF preamp, 24 V active.
P1-18	Preamp Out	0 V/24 V, relay control for RF preamp, 24 V active.
P1-19	Power Off Protect	0 V/5 V, Rin = 57 Kohms, active high from front panel to set test load relay to protect receiver when mode is set to off.
P1-20	+5 V	+5 V, power for digital circuits.
P1-21	Spare	No connect.
P1-22	Spare	No connect.

3. TECHNICAL DESCRIPTION

This subsection gives a detailed circuit description for the A8 Power Amplifier/Battery Charger Assembly. The subsections that are covered include the following assemblies:

- A8A1 RF POWER AMPLIFIER/BATTERY CHARGER PWB ASSEMBLY (10303-2130)

  RF PA/Harmonic Filter/Antenna Coupler Serial Digital Control

  RF PA Digital Status Monitor

  RF Transmit Signal Path

  RF Receive Signal Path

  DC Power Distribution

  RF PA Analog Signals

  Internal Battery Chargers

- A8A2 HARMONIC FILTER ASSEMBLY (10303-2140)

  Harmonic Filter Control

  Harmonic Filter RF Signal Flow

  Harmonic Filter topology

  Directional Coupler and PA TX Power Control

3.1 A8A1 RF Power Amplifier/Battery Charger PWB Assembly (10303-2130)

3.1.1 RF PA/Harmonic Filter/Antenna Coupler Serial Digital Control

A synchronous serial data stream is used to control the RF PA, Harmonic Filters, and Antenna Tuner simultaneously. Figure 2 is a detailed block diagram of the RF PA/Harmonic Filter/Antenna Coupler serial data stream structure and flow. Figure 3 is a PA/Coupler Synchronous Serial Control Bus Timing Diagram and figure 4 is a PA/Coupler Control Data Word Diagram.

The serial data from the A4 Signal Processor Assembly goes directly to the A8A1 RF Power Amplifier/Battery Charger PWB Assembly. The A8A1 RF Power Amplifier/Battery Charger PWB Assembly uses one byte of data for its control. The serial data then passes to the A8A2 Harmonic Filter Assembly which uses 20 bits to control its selection of filter bands. Finally, the serial data goes to the A9 Antenna Coupler Assembly which requires 52 bits of data to control the selection of tuning elements. In order to get to the A9 Antenna Coupler from the Harmonic Filter Assembly, the data must pass back through the A8A1 RF Power Amplifier/Battery Charger Assembly, because the A8A2 Harmonic Filter Assembly is not connected directly to the A11 Motherboard.

The serial data stream and clock are common to the A6 Reference Generator/Synthesizer Assembly which uses it to load frequency data information in its various PLLs and main Synthesizer. The A4 Signal Processor Assembly controls where the serial data goes (A6 Reference Generator/Synthesizer Assembly or A8 RF Power Amplifier Assembly/A9 Antenna Coupler Assembly) by the use of single line address strobe signals which are unique to each assembly. Serial data and clock from the A4 Signal Processor Assembly are present and active at the A8 RF Power Amplifier Assembly when the A4 Signal Processor Assembly is sending data intended for the A6 Reference Generator/Synthesizer Assembly; however, the strobe is high. The A8A1 RF Power Amplifier/Battery Charger Assembly uses U1 to stop the data and clock intended for the A6 Reference Generator/Synthesizer Assembly from propagating through the A8 RF Power Amplifier/A9 Antenna Coupler Assemblies. This helps prevent digital noise from interfering with RF transmit and receive signals which pass through these assemblies. To load the Power Amplifier and Antenna Coupler assemblies, the A4 Signal Processor Assembly brings the RF PA/Coupler strobe signal from high to low to enable the data to pass through U1. The RF PA/Coupler strobe is held low during the entire 10 byte stream of serial data to allow it to propagate through the A8 RF Power Amplifier/A9 Antenna Coupler assemblies. After the last bit is shifted, the RF PA/Coupler strobe is brought from low back to high. The circuit with C9, R9, R16 is used as a differentiator to form the control data strobe pulse on the low to high transition of the RF PA/Coupler strobe to latch the serial data into the A8 and A9 assemblies.

Byte #10 of the RF PA/Coupler control word is latched into U2 by the Control Data Strobe Pulse. U2 converts the serial data stream to control signals for the A8A1 RF Power Amplifier/Battery Charger Assembly. There are eight control signals for the RF PA that come from the serial control data. Relay driver output enable is U2 pin 15. This signal is pulsed low to activate the +24 V outputs of all the Relay Driver ICs in the A8A2 Harmonic Filter Assembly and the A9 Antenna Coupler Assembly. This means that all the relays change states simultaneously once the serial data is latched.

On the A8A1 RF Power Amplifier/Battery Charger Assembly, U2 pin 1 is used to control the state of an analog multiplexer U5 which is monitored by the A4 Signal Processor Assembly via analog antenna coupler feedback. Internal battery charger operation is controlled by U2 pin 2. Transistors Q1 and Q2 are used to shut down the internal battery chargers when necessary during radio operation by grounding the output of the constant current diodes CR29 and CR36 for battery chargers #1 and #2, respectively. Battery power for the RF power amplifier transistors Q4 and Q5 is controlled by U2 pin 3. The rising and falling edges of U2 pin 3 are used to actuate relays K5 and K6 which apply battery power to the drains of Q4 and Q5. The differentiator circuits consisting of C50, C112, R59, R65, R67, and R151 form pulses to drive level shifting transistors Q10 and Q11. U2 also controls analog switch U3, a section of which is used as an open drain level shifter for the DC bias control to actuate Q6 which actually switches the +12 V DC bias supply to the gates of Q4 and Q5. U2 also uses analog switch U3 as an open drain buffer to control the following three functions:

- Turn the receive RF preamplifier +5 V power on and off.
- Change harmonic filter directional coupler forward power gain for 100mW TX mode.
- Disable the TX keyline from the A4 Signal Processor Assembly for 100mW TX mode.

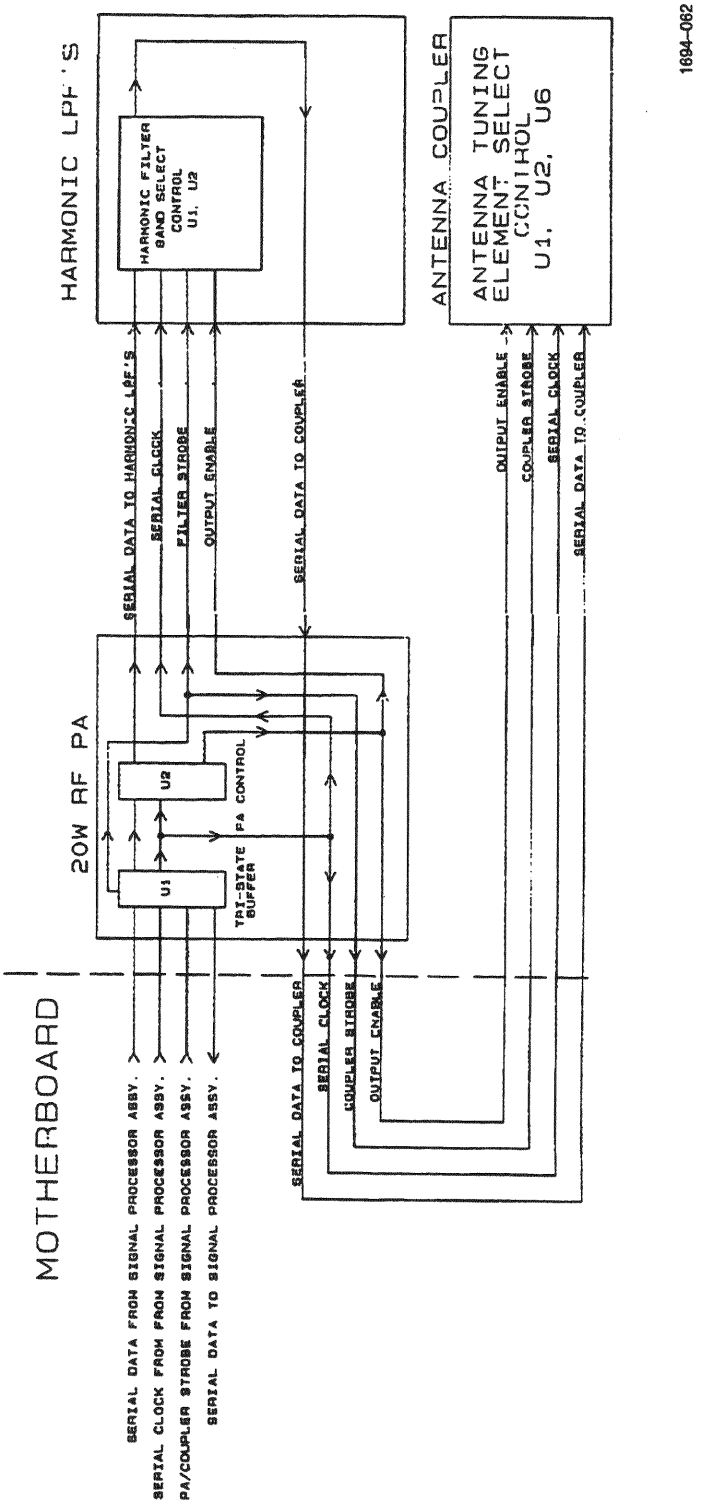


Figure 2. PA/Coupler Serial Data Control Block Diagram

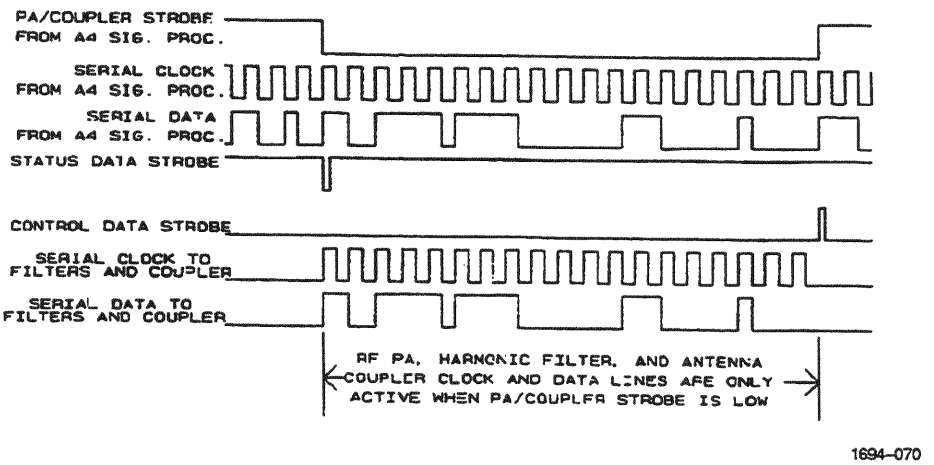
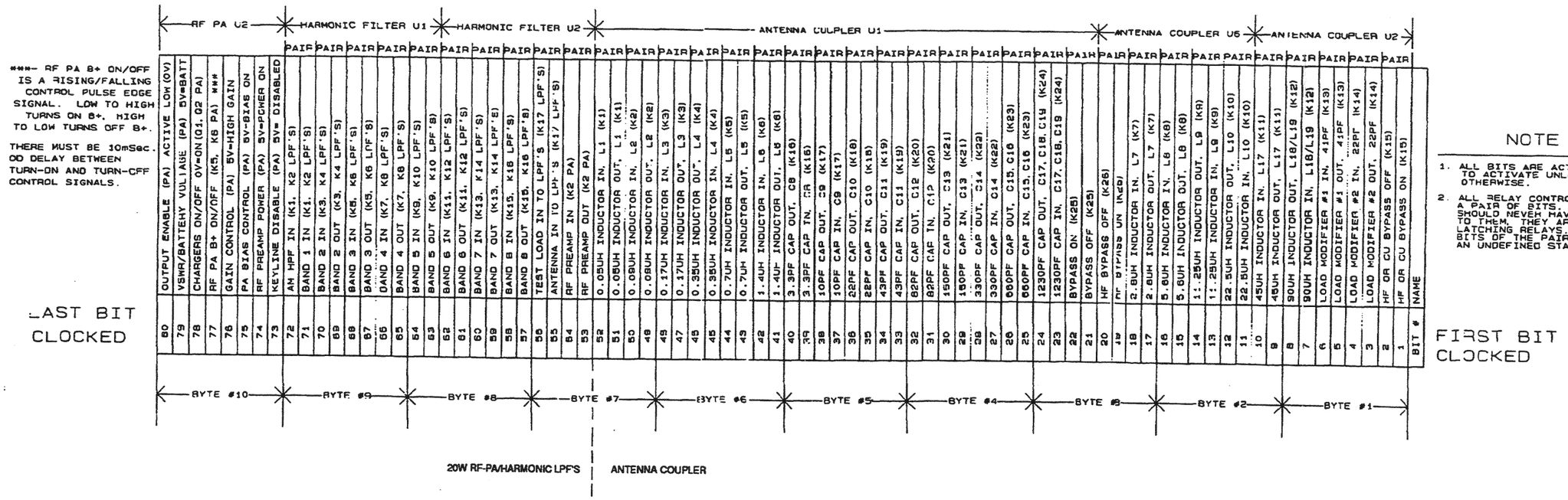


Figure 3. PA/Coupler Synchronous Control Bus Timing Diagram



NOTE

1. ALL BITS ARE ACTIVE HIGH TO ACTIVATE UNLESS STATED OTHERWISE.
2. ALL RELAY CONTROL BITS ARE A PAIR OF BITS. THE PAIR SHOULD NEVER HAVE A 1 1 WRITTEN TO THEM. THEY ARE 2 COIL LATCHING RELAYS. SETTING BOTH BITS OF THE PAIR WILL CAUSE AN UNDEFINED STATE IN THE RELAY.

****- RF PA B+ ON/OFF IS A RISING/FALLING CONTROL PULSE EDGE SIGNAL. LOW TO HIGH TURNS ON B+, HIGH TO LOW TURNS OFF B+.

THERE MUST BE 10mSec. OD DELAY BETWEEN TURN-ON AND TURN-OFF CONTROL SIGNALS.

1694-071

Figure 4. PA/Coupler Control Data Word Diagram

3.1.2 RF PA Digital Status Monitor

The A8A1 RF Power Amplifier/Battery Charger Assembly provides a byte of digital information that allows the A4 Signal Processor to monitor the activity of certain analog conditions within the assembly. The analog functions that are monitored are Ni-Cd/$LiSO_2$ battery type for each battery, external DC power for radio power, RX preamplifier overload status, and internal battery charger outputs on/off.

These status signals are read by the A4 Signal Processor on the same serial data line that is used for reading DTCXO temperature data from the A6 Reference Generator/Synthesizer Assembly. U4 of the A8A1 RF Power Amplifier/Battery Charger Assembly is used to shift the status data to the A4 Signal Processor Assembly. The status data shifts out simultaneously as the control data for the A8 RF PA/A9 Antenna Coupler is shifted in. U1 serves as a tri-state output buffer that only allows the data from U4 onto the serial bus to the A4 Signal Processor when the RF/PA Coupler strobe is active (low). The status data is latched into U4 by a load pulse that is created by the high to low transition of the RF PA/Coupler strobe being differentiated into a short pulse by the network of C7, R5, and R6.

3.1.3 RF Transmit Signal Path (25 Watt)

The internal 25W RF PA accepts TX RF of 1.6 MHz to 60 MHz directly from the A5 Receiver/Exciter Assembly at a nominal level of 50 mW to J2 of the A8A1 RF Power Amplifier/Battery Charger Assembly. The TX path is routed through K1 and K4 which normally have the RX path selected. The TX keyline signal from the A4 Signal Processor Assembly supplies an active high (5 V) signal to K1 and K4 to select the TX path. Additionally, the A4 Signal Processor Assembly uses two control lines from U2 and U3 to control the applicators of battery power to the drains of RF power MOSFETS Q4 and Q5, and DC bias voltage to the gates of Q4 and Q5 in order for the amplifiers to function. DC bias is applied to the gates of Q4 and Q5 by an active low signal turning on Q6. The parallel combination of R39 and RT1 (positive temperature coefficient thermistor) is used to reduce the DC bias to both Q4 and Q5 as the temperature of the transistors increases. The first of two stages of the RF power amplifier consists of Q5, a class A driver stage which is set to 400mA of drain bias current by adjusting R36. Q5 is followed by Q4, a class A–B output stage which has each side of Q4 set to 50 mA of drain bias current by adjusting R48 and R49. The Q5 class A driver stage is a 1.6 MHz to 60 MHz broadband feedback design with R29 and R31 providing the feedback to yield 15 dB of power gain, which is 1.6W out for 50 mW in. Q5 drives the balanced output stage through T1, which is a 50 ohm BALUN (unbalanced to balanced converter). The output from T1 are two signals that are half the amplitude of the input signal and 180 degrees out of phase with each other. These signals are used to drive the Q4 class A–B output stage. The Q4 class A–B output stage is also broadband, 1.6 MHz to 60 MHz. Components R40, L5, R42, and C28 form an impedance matching network to match the low gate impedance of Q4A to 25 ohms. Similarly, components R50, L6, R52, and C31 form an impedance matching network to match the low gate impedance of Q4B to 25 ohms. Components R45 and R55 feed the DC bias voltage to the gates of Q4A and Q4B, respectively while their high impedance deters the RF signal from going back down the DC bias path. The outputs of Q4A and Q4B are combined and matched from the 35 ohm impedance level to 50 ohms by T2. T2 also functions as a balun to convert from the balanced output stage to single unbalanced output. The class A–B output has 12 dB power gain to produce 25W output for 1.6W input. The high level RF then passes through K4 T/R relay, out the J3 coax, and on to the A8A2 Harmonic Filter Assembly.

3.1.3.1 RF Transmit Signal Path (100 mW)

The 10303-2130 also has a 100 mW transmit mode of operation for antenna tuning and exciter operation with 125W or 400W external RF Power Amplifiers. 100 mW transmit RF is generated by the A5 Receiver/Exciter Assembly. The same TX keyline that is used to select the 25W transmit path on the A8A1 RF Power Amplifier/Battery Charger Assembly is used to key the A5 Receiver/Exciter Assembly. In 100 mW transmit mode, the A8A1 RF Power Amplifier/Battery Charger Assembly merely allows the transmit RF to pass through the RF receive path and not through the 25W transmit path. The keyline disable control from U2/U3 is used to ground the gate of keyline level shifter Q3, which disables the TX keyline to the PA. Resistor R25 is used to

provide a high impedance for the TX keyline signal which is used to key the A5 Receiver/Exciter Assembly. If the user selectable RF preamplifier is enabled, the A4 Signal Processor Assembly bypasses the RF preamplifier when in 100 mW transmit mode so that 100 mW is not transmitted into the output of the preamplifier. The 100mW transmit RF then passes through the A8A2 Harmonic Filter Assembly and on to the A9 Antenna Coupler Assembly.

3.1.4 RF Receive Signal Path

The RF receive path in the A8A1 RF Power Amplifier/Battery Charger Assembly consists of a receiver protection circuit followed by a user selectable receive preamplifier. The RX path is also used for 100 mW transmit when antenna tuning is done or when the radio is acting as an exciter for an external 125W or 400W RF power amplifier. T/R relays K1 and K4 default to the receive path unless the TX keyline from the A4 Signal Processor Assembly is asserted with an active high 5 V.

3.1.4.1 Receiver Protection

Receive RF enters the A8A1 RF Power Amplifier/Battery Charger Assembly at J3. It then passes through K4 and the first thing encountered is the receiver protection circuit. Receiver protection is accomplished by using diodes CR1 and CR4 as RF peak limiters. CR1 and CR4 begin to limit when the peak of the receive signal is approximately 1.4 Vp-p or about +7 dBm. In order for these diodes to act as limiters they must have a DC path to ground. Inductors L12 and L9 provide these DC paths to ground. Inductor L9 actually gets its DC path to ground through the first RF mixer in the A5 Receiver/Exciter Assembly. Both of these DC ground paths must be present in order for the peak limiter to function properly. When the RX path is used for 100 mW transmit, the DC blocking capacitor in the output of the last stage exciter amplifier in the A5 Receiver/Exciter Assembly interrupts the DC path to ground and the limiter no longer limits for the 100 mW (+20 dBm) transmit RF.

3.1.4.2 Receiver Preamplifier

The next function in the receive path on the A8A1 RF Power Amplifier Assembly is the user selectable RX RF preamplifier. U7 is a low noise 1.6 MHz to 60 MHz broadband amplifier that has 4 dB noise figure and 13 dB gain. When the RF preamplifier is selected, the A4 Signal Processor Assembly activates it by pulsing pin 10 of relay K2 to put the RF preamplifier into the receive path. The RF preamplifier power on/off control from U2/U3 turns on Q8 and applies power to U7 and U8. Resistor R54 sets the supply current for U7 to 10mA and inductor L8 allows the DC current to pass while presenting a high impedance to the RF signal. U7 is a low level amplifier and cannot take signals larger than +3 dBm without degradation in noise figure and gain. Also, signals of this level will cause the RF preamplifier to badly distort any AM or USB modulation. In order to cope with these problems the DC bias voltage of the RF preamplifier (U7 pin 1) is sampled by the network of R68, C52, and R73.

U7 is a single-stage, bipolar, transistor amplifier and normally has a DC bias of about 0.7 V. As the signal level at the input to U7 increases toward the +3 dBm level, the DC bias voltage will begin to drop. When the RF receive signal is about +3 dBm, the DC bias will drop to about 0.55 V. U8 is a comparator which has a reference voltage of 0.55 V. When the DC bias of the RF Preamplifier U7 drops below the reference voltage, comparator U8 fires and through the open collector level shifting network of Q13 and Q9, a +24 V pulse is applied to relay K2 pin 1 to remove U7 from the RF receive path. The RF preamplifier will then be out of the receive path, but preamplifier power will still be applied. A preamplifier overload status signal is derived from this condition.

When the RF preamplifier is selected, R77 is DC grounded through the first mixer in the A5 Receiver/Exciter Assembly. R76 feeds this low voltage into U4 pin 3. When the RF preamplifier overload comparator U8 fires and relay K2 removes the RF preamplifier from the receive signal path, R77 loses the DC ground from the A5 Receiver/Exciter Assembly and the voltage sampled by R76 rises to 5 V to indicate that an input signal overload has occurred. This preamplifier status can be read by the A4 Signal Processor in the RF PA status byte as described in subsection 3.1.2. When the preamplifier is bypassed by user selection, the A4 Signal Processor Assembly pulses relay K2 pin 1 and uses the U2/U3 preamplifier power on/off line to remove the 5 V from U7 by turning off Q8. After the selectable RF preamplifier, the receive RF passes through relay K1 and out through J2 to the A5 Receiver/Exciter Assembly.

3.1.5 DC Power Distribution

The A8A1 RF Power Amplifier/Charger Assembly accepts and distributes all sources of DC input power for the radio which come from the A10 Front Panel and the two batteries that connect directly to the A8 RF Power Amplifier. DC input power should be from 20 to 32 VDC and must be conditioned, which means that no voltage surges or spikes above 32 VDC should be present on these sources. Refer to figure 1 and the A8A1 schematic for the following description.

The A10 Front Panel Assembly external RF power amplifier interface connector (A10, J6) accepts DC power on two sets of pins that are routed directly from the A10 Front Panel to the A8 RF Power Amplifier. One set of pins is used as external DC power for the radio and the other set is used as DC input power for the internal Ni-Cd battery chargers located on the A8A1 RF Power Amplifier/Battery Charger Assembly. The external DC power is fused at 1 ampere and the battery charger power is fused at 7 amperes on the A11 Motherboard. Two BB-590/U Ni-Cd or BA-5590/U $LiSO_2$ batteries may be used with the radio and connected directly to the A8A1 RF Power Amplifier/Chargers PWB Assembly.

The DC sources of power have one of two destinations, the 25W RF power amplifier or the rest of the radio that requires +24 V. (The assemblies that require +24 V are the A5 Receiver/Exciter, A7 Power Supply, A8 RF Power Amplifier and Harmonic Filter relays, A9 Antenna Coupler, and A10 Front Panel.) The batteries are the only source of DC power that can power the 25W RF Power Amplifier. The external radio power can only power the rest of the radio that requires +24 V. The batteries also power the rest of the radio when there is no external radio power from the A10 Front Panel.

Battery #1 enters the radio through A8A1 RF Power Amplifier/Battery Charger Assembly J5 and battery #2 enters through J6. C57, C59, and T3 provide EMI/RFI filtering for battery #1, while C66, C68, and T4 perform the same function for battery t#2. F1 and F3 provide catastrophic over current protection for battery #1 and #2. Additionally, CR14 and CR15 provide series reverse polarity protection for each battery.

Battery #1 provides power to the 25W RF PA through relay K5 and battery #2 provides power to the 25W RF PA through relay K6. The relays are necessary to ensure that no current is drawn from the batteries when the 25W RF PA is not in use. If the RF power transistors Q4 and Q5 were directly on the batteries, they would draw up to 10mA from the batteries all the time (even when they are biased off). After passing through the relays K5 and K6, the current from each battery is sampled by resistors R150 and R106 for the purpose of transmit current limiting and then the two batteries are diode ORed together via CR15 to provide power for the 25W RF PA.

A parallel path for each battery to power the rest of the assemblies exists where the batteries connect to K5 and K6. At these points the batteries are diode ORed together via CR14 and the ORed voltage passes through Q14 to provide power to all the assemblies listed above, except the 25W RF Power Amplifier. Q14 is a battery isolation solid-state switch that prevents the CR14 ORed battery voltage from powering the radio (except for the 25W RF power amplifier when external radio power is present), so that if the external radio power is lower in voltage than the batteries, the batteries will not be drained when external radio power is present.

External radio power enters the A8A1 RF Power Amplifier/Battery Charger Assembly from the A11 Motherboard at P1 pin 5, passes through reverse polarity protection diode CR17, and then goes directly to power the assemblies that require +24 V. External radio power is sensed at P1 pin 5 by the circuit of VR2, R89, R90, and Q15. When the external radio voltage at P1 pin 5 is greater than 16 VDC, Q15 turns on and opens the battery isolation switch Q14 by turning on Q16. Q16 shorts the gate to source voltage of Q14 and turns Q14 off to isolate the batteries from the external radio power and all assemblies except the 25W RF PA. An external radio power sense status bit is monitored by U4 pin 12 which is pulled up to 5 V unless Q15 is on.

When there is external radio power and Q15 is on, this bit becomes a zero and the A4 Signal Processor can discern that external radio power is present and that an external 125W or 400W RF power amplifier is connected to the radio. The presence of an external RF PA causes the A4 Signal Processor to disallow the use of the internal 25W RF power amplifier and to disallow any transmit frequency above 30 MHz. The 125W and 400W external

RF power amplifiers do not operate at frequencies higher than 30 MHz, and 25W of input drive power to these external RF PAs would damage them. They are designed to operate from 100 mW of drive power.

3.1.5.1 Batteries

The two types of batteries that connect to the radio are BB-590/U Ni-Cd or BA-5590/U $LiSO_2$ batteries. Both types of batteries can be configured as two 12 V sources to be operated in parallel, or as one 24 V cell when used in a series. The two 12 V sources are pins 4 (+) and 1 (–), and pins 5 (+) and 2 (–). The RT-1694 uses the sources in series with pin 5 as the positive terminal, pin 1 as the negative terminal, and pins 2 and 4 tied together to form a 24 V source of DC power.

The BB-590/U Nickel-Cadmium Battery is rechargeable and the RT-1694 has internal battery chargers to recharge it.

The BA-5590/U $LiSO_2$ is not rechargeable and has a peak current limitation of 2 amperes. It is fused internally so that if more than 2 amperes is drawn, the fuse opens to protect the battery. The BA-5590/U can fail in a violent manner, which in the worst case is an explosion, if it experiences a cell reversal. This is usually caused by high discharge currents or attempted recharging.

WARNING

Do not charge the BA-5590/U Lithium-Sulfide Battery. The battery may rupture, releasing toxic material.

If a $LiSO_2$ battery accidentally ruptures, ventilate the area well and wash away any spilled residue with water.

WARNING

Do not use a Halon-type fire extinguisher on a lithium-sulfur dioxide battery fire. In the event of a fire near a $LiSO_2$ battery, rapid cooling is important. Use a carbon dioxide (CO_2) extinguisher. Control of the equipment fire and cooling may prevent the battery from venting and potentially exposing lithium metal. In the event that lithium metal becomes involved in the fire, the use of a graphite-based, Class-D fire extinguisher is recommended.

NOTE

Be sure to follow all of the battery manufacturer's safety precautions.

Proper disposal of a lithium-sulfur dioxide battery is of utmost importance. Completely discharged batteries are not considered hazardous or reactive. The BA-5590/U Lithium-Sulfur Dioxide Battery includes an internal discharge switch. To discharge the battery, activate this switch per the battery manufacturer's instructions.

WARNING

A partially discharged lithium-sulfur dioxide battery is considered to be hazardous waste and it should not be disposed of with ordinary trash/refuse.

The two batteries are identified electrically by using pin 3 of the battery. The BB-590/U has pin 3 tied to pin 1, the BA-5590/U has no pin 3 and it is, therefore, floating electrically. Pin 3 of J5 is pulled up to 5 V by R78 and pin 3 of J6 is pulled up to 5 V by R99. If a BB-590/U is connected to either battery input, pin 3 will be pulled down low. Each battery has a circuit that uses Q26 and Q27 to inhibit internal battery charger operation if pin 3 is floating, which would be the case if a BA-5590/U or no battery was connected to either battery input. Q26 and Q27 inhibit internal charger operation when they are turned on. Note that the bias for these transistors is obtained from the internal charger DC input power, so no current is drawn from the batteries to bias these devices on. They only operate when external power is present at the front panel. Pin 3 of each battery is monitored by U4 pins 4 and 5, which then can be read by the A4 Signal Processor in the digital status bite to allow battery type identification. Analog switch U15 has its control inputs tied to pin 3 of each battery. When pin 3 is floating, the analog switch sets the amount of current that the 25W RF PA can draw from a battery to 1.4 amperes so that the BA-5590/U is not damaged. Diodes CR14 and CR15 that OR the two batteries together also provide battery to battery isolation, so if one battery is higher in voltage than the other, it cannot charge the lower voltage battery.

3.1.6 RF PA Analog Signals

The following are other analog functions/signals in the A8A1 RF Power Amplifier/Battery Charger Assembly which are described in this subsection:

- A7 power supply turn-on circuit
- 25W RF PA temperature sense
- 25W RF PA battery current limit
- RF PA Feedback for TX power control
- Individual battery voltage/VSWR measurement

3.1.6.1 A7 Power Supply Turn-on

The A7 Power Supply requires a +24 V level to its turn-on input to become active and generate the +5 V, +6.8 V, +16.5 V, and –12 V power necessary to run the radio, including the op-amps and logic on the A8A1 RF Power Amplifier/Battery Charger Assembly. The A8A1 RF Power Amplifier/Battery Charger Assembly accepts inputs from the A10 Front Panel and A1A1 Interface real time clock to turn on the A7 Power Supply. The A10 Front Panel supplies a 5 V active level standby/normal control to P1 pin 9 which is the usual method for turning on the radio. The A10 Front Panel data connector (J2 pin E) also has an active low remote power on signal which enters at P1 pin 8 to turn on the A7 Power Supply. The A1A1 Interface real time clock can provide a 5 V active level which enters at P1 pin 10 to turn on the A7 Power Supply. The circuit consisting of Q17 and Q18 performs the turn-on function. This circuit is an OR function; therefore, any one or all of the three possible inputs listed above may turn on the A7 Power Supply.

3.1.6.2 25 W RF PA Temperature Sense

Temperature of the 25W RF PA output stage transistor Q4 is monitored by the voltage divider consisting of R56 and RT2. RT2 is a negative temperature coefficient thermistor that is attached to the mounting flange of Q4. As the temperature of the output transistor increases, the divider voltage decreases from 5 V. At a room temperature of approximately 25°C, this voltage is about 4.55 V. When Q4 reaches a temperature of 85°C, the A4 Signal Processor cuts back transmit power from 25W to 5W to allow Q4 to cool. This temperature signal is fed to the A9 Antenna Coupler and is monitored by the A4 Signal Processor via coupler feedback.

3.1.6.3 RF PA TX Battery Current Limit

Transmit current drawn from each battery is monitored by current sampling resistors R150 and R106 for battery #1 and #2, respectively. SIP resistor R83 forms a differential amplifier with U9A, which then feeds the two-level gain amplifier U9B to produce 4.3 V when 1.4A is drawn from a BA-5590/U, or when 3.4A is drawn from a BB-590/U by the 25W RF PA. The two-level gain change is accomplished by U15. When a BB-590/U is present, the gain of U9B is determined by R87 and R88. When a BA-5590/U is present, U15 switches R157 in parallel with R88 to increase the gain of U9B, which means that less current through the sample resistor R150 is required to drive the output of U9B to 4.3 V. An identical circuit is present for battery #2 with SIP R102 and U10A forming the differential amplifier and R105, R109, R162, and U10B forming the two-level gain stage. U15 switches in R162 to increase the gain of U10B when a BA-5590/U is present at battery #2.

3.1.6.4 RF PA Feedback for TX Power Control

RF PA feedback to the transmitter gain control loop is comprised of a diode ORing of the two current limit signals described earlier, forward TX power level, reflected power level, and external 125W or 400W RF PA feedback. The A4 Signal Processor adjusts the A5 Receiver/Exciter RF drive level to the 25W RF PA to get 4.3 V on the PA feedback signal that is monitored from P1 pin 23 when the radio is set to high power. The OR function works on the principal that whichever signal reaches 4.3 V with the lowest amount of exciter drive will control transmit power output level. Normally, 25W of forward transmit power will be the first signal to be driven to 4.3 V from the A5 Receiver/Exciter drive. If there is a VSWR of greater than 2.5:1 then the reflected power signal will be the first signal to reach 4.3 V and it will control the TX output power level, which will be less than 25W. Both of these signals are generated by the directional coupler circuits on the A8A2 Harmonic Filter Assembly and are diode ORed there and then fed to the A8A1 Assembly at J4 pin 11 where they are joined by the two current limit and external RF PA signals. If there is some fault condition in the output load or if only one BA-5590/U is present, the battery TX current limit signals will be driven to 4.3 V with the least amount of exciter drive. Finally, when there is an external 125W or 400W RF PA present, the internal 25W PA is not used. This eliminates the current limit inputs and only 100mW of exciter drive will pass through the directional coupler, which will produce little forward and reflected power for feedback and the external RF PA feedback should control the transmit power output.

3.1.6.5 Individual Battery Voltage/VSWR Measurement

Battery voltage is measured individually by U9C for battery #1 and by U10C for battery #2. U9C samples battery #1's voltage at SIP R83 pin 2, which is the battery voltage divided by 3. The output of U9C is then divided by 5.52 by the voltage divider formed by R85 and R86 to produce a battery #1 voltage sample that is approximately divided by 17.

Similarly, U10C samples battery #2 voltage at SIP R102 pin 2, which is the battery voltage divided by 3 and the output of U10C is further divided by R103 and R104 to also provide a battery #2 voltage sample divided by 17. These battery voltage samples are fed to analog switch U5. Additionally, the A8A2 Harmonic Filter Assembly provides voltages representing forward and reflected power to analog switch U5 to allow the A4 Signal Processor to calculate the VSWR that is present at the output of the harmonic filters. The VSWR/battery voltage control from U2 is set by the A4 Signal Processor to select which analog signals are to be monitored. These signals are sent to the A9 Antenna Coupler and are monitored by A4 via the coupler feedback.

3.1.7 Internal Battery Chargers

There are two identical internal battery chargers on the A8A1 RF PA/Charger Assembly. These chargers operate independently for each battery. They are flyback type DC to DC converters that operate as constant current sources of 180mA with a maximum output voltage of 34.5 V. DC input voltage from 10 V to 32 V is sourced from the A10 Front Panel external RF PA connector(A10, J6), enters the A8A1 RF Power Amplifier/Battery Charger Assembly at P1 pins 1 and 2(+), and pins 3 and 4(–), and is supplied to the two charger circuits.

Battery charger #1 DC input first passes through series reverse polarity protection diode CR28. Next, the input voltage passes through EMI/RFI filtering formed from the network of C13, C74, C75, C77, T5, and E7. The input voltage is then fed to the flyback power transformer T6 and to the current mode control pulse width modulator (PWM) IC U11 through voltage regulator circuit Q20, CR29, and VR3. The voltage regulator produces about 10.7 V at the emitter of Q20 when the input voltage is above 12 V due to the 12 V zener diode in the base of Q20. CR29 is a constant current diode that sources 2mA of current (no matter what voltage is applied across it) and serves to bias the Q20 voltage regulator circuit. The output of this circuit sources power for the current mode control PWM IC U11, the feedback amplifier U12, and the lithium battery charger shutdown circuit of Q27, R71, and R72.

PWM control IC U11 is a current mode controller which changes the width of drive pulses that are applied to the gates of power MOSFETS Q21 and Q22 to maintain the output voltage of the charger at whatever voltage is necessary to obtain the constant charge current of 180mA. The MOSFET gate drive output at U11 pin 10 is a train of pulses at a constant frequency determined by R112, C82, and C83 of about 70KHz whose width is determined by both feedback amplifier U12 and peak MOSFET current that is sampled by R116, which is fed into the sense input pin 5 of U11. When the drive pulses are high, power MOSFETS Q21 and Q22 turn on and pull pin 2 of flyback power transformer T6 near to ground. Current flows through the primary of T6 which stores energy, while Q21 and Q22 are on. T6 is wound so that pin 3 has the same polarity as pin 2, therefore when pin 2 is near ground so is pin 3 and the output rectifier CR31 is reverse biased. All the load current then is supplied from output filter capacitor C81. When the gate drive pulses to Q21 and Q22 go back low, Q21 and Q22 turn off. The voltage across the primary of T6 pin 2 flies back to the input voltage plus the output voltage divided by the turns ratio of primary to secondary which is 1:3.8. This is due to the property of inductors that the primary of T6 wants to keep the current flowing in the same direction and magnitude that it was when Q21 and Q22 were on. The polarity of the voltage instantly reverses which forward biases output rectifier CR31, and the peak current that was flowing in the primary of T6 during the on time of Q21 and Q22 transfers to the secondary, once again divided by the turns ratio of T6. This current goes to both the output load and filter capacitor C81.

The output voltage level of the charger is determined mainly by feedback amplifier U12. U12 is a diode ORed feedback amplifier which is intended to provide feedback to the compensation input (pin 1) of U11 to maintain constant charge current of 180 mA, but also limits the maximum output voltage of the charger to 34.5 V if no current is being drawn. A 5 V reference voltage is available at U11 pin 14 which is used to set reference levels for the feedback amplifier U12 for constant current and maximum output voltage. R117 and R125 form a voltage divider to create a reference voltage of 0.87 V at the constant current control portion of the feedback amplifier, U12 pin 5. R116 and C85 form a filter that uses the 5 V reference directly to the reference for the maximum output voltage feedback at U12 pin 3. The voltage across R94 is sampled to represent the charge current flowing in the battery and fed back to the constant current portion of U12 at R127. CR13 is in parallel with R94 to allow normal operating current through the battery to flow around R94 and clamps the voltage to about 0.5 V, when charging CR13 is reverse biased and R94 has all the charging current flow through it to provide the current sample mentioned earlier.

When the charger control loop is operating normally, the feedback voltage input from R94 (Ichg*4.3) at R127 will be equal to the reference voltage at U12 pin 5 of 0.87 V, and 0.87 V divided by 4.3 ohms yields the desired charge current 180 mA. Similarly, CR32 and C89 provide a sample of the output voltage of the charger that is fed to the maximum output voltage portion of U12 at R120. R120 and R119 form a voltage divider such that when the output voltage is 34 V there will be 5 V at U12 pin 2.

Because the maximum output voltage reference is higher than the constant current reference voltage, the constant current should control the charger output voltage, but if not enough charge current is flowing, the output voltage will rise in an attempt to get the feedback through R94 to be 0.87 V. When the voltage reaches 34 V, the maximum output voltage control loop reference voltage will be satisfied by feedback to R120 of U12 pin 2 and the charger will be under constant voltage control. Lastly, when there is no battery present, VR5 and R11 provide a minimum output current load when the output voltage rises above 33 V. This is necessary to keep the output

capacitor C91 from charging to the peak voltage of the secondary waveform which is nearly 200 V with 36 VDC of charger input power.

The charger is turned on and off by firmware control through Q1 or from the lithium battery sensing hardware circuit of Q27. Q1 or Q27 can turn off the charger by grounding the base of the 10.7 V regulator pass transistor Q20 which removes Vcc from the switcher control IC U11, which causes the charger to stop operating. Firmware does not allow the charger to run when the radio is on so that EMI/RFI does not degrade the sensitivity of the receiver. The lithium battery sensing hardware does not allow the charger to run when a lithium battery (or no battery) is connected to the radio. Charger output voltage is sampled by the voltage divider of R100 and R101 and is fed back as charger output voltage on/off status to the A4 Signal Processor to evaluate/verify the charger operation.

Battery charger #2 is identical to battery charger #1 in its circuitry and electrical functionality. When troubleshooting, refer to the schematic for battery charger #1 and then locate the similar component on the schematic for battery charger #2.

3.2 A8A2 Harmonic Filter PWB Assembly (10303-2140)

The A8A2 Harmonic Filter PWB Assembly is a physical piggyback assembly to the A8A1 RF Power Amplifier/Battery Charger Assembly. It consists of eight low pass filters that are relay selectable along with a relay selectable RF transmit BITE test load. Transmit power control feedback and VSWR measurement are present on this assembly. The selection of the filters, etc. is accomplished through the synchronous serial control from the A4 Signal Processor described in subsection 3.1.1.

3.2.1 Harmonic Filter Control

The A8A2 Harmonic Filter Assembly selects filter bands, RF test load, and A8A1 RX Preamplifier via relays whose states are digitally controlled by the A4 Signal Processor synchronous serial control. U1 and U2 are relay driver level shifting buffer ICs that appear as 5 V shift registers with data latches on their outputs to the A4 Signal Processor. The data that is stored in the latches is level shifted to +24 V to drive the coils of the relays on the A8A2 Harmonic Filter Assembly. Serial data enters U1 at pin 15 is shifted through 10 bits of control and exits U1 at pin 18. The data out of U1 enters U2 at pin 15 and is shifted through an additional 10 bits of control and exits U2 at pin 18. This data is then passed back through the A8A1 RF PA/Chargers through the A11 Motherboard and on to the A9 Antenna Coupler. Control data is latched into U1 and U2 simultaneously by the data strobe signal generated on the A8A1 RF Power Amplifier/Battery Charger Assembly, which enters the A8A2 Harmonic Filter at P1 pin 3. The blank input of U1 and U2 at pin 14 of the ICs actually applies the +24 V level shifted output of the relay driver ICs when brought low. This signal must be held low (at least 5 msec) to allow the relays enough time to switch.

When the relays have switched, the +24 V is removed by the act of bringing the blank input of U1 and U2 back high. All the relays driven by U1 and U2 are latching relays that remain in whatever position they are switched to after the relay coil drive is removed. The gain of the directional coupler PA feedback forward power amplifier is also digitally controlled by the A4 Signal Processor from the A8A1 gain control bit which enters the A8A2 Harmonic Filter at P1 pin 16. When this signal is switched to high gain, 100 mW of forward RF power will drive the PA feedback to 4.3 V for antenna tuning power control. There is a control signal that comes from the A10 Front Panel, which is the Power Off Protect that enters the A8A2 Harmonic Filter at P1 pin 19. This signal is generated when the MODE control on the A10 Front Panel is switched to the OFF position.

It is a 5 V pulse that switches the Harmonic Filters into the RF Test Load rather than the A9 Antenna Coupler to protect the filters, RF PA, and Receiver from ESD and High power RF from the Antenna when the radio is off.

3.2.2 Harmonic Filter RF Signal Flow

Refer to figure 5, a block diagram of the Harmonic Filter RF signal flow, and the A8A2 schematic diagram for the following discussion.

Transmit signal flow through the A8A2 Harmonic Filter Assembly starts with A8A1 RF Power Amplifier/Battery Charger transmit signal entering at J2. There are eight possible harmonic filters that RF can pass through which are referred to as filter bands. The transmit signal must pass through either Band 1 low pass filter or an AM broadcast interference (BCI) high pass filter, and then pass through one of the remaining seven filter bands, through the directional coupler, and out J3 to the A9 Antenna Coupler. Note that any unused filter band from band 2 through band 8 is grounded at both ends when not in use to prevent RF coupling to the unused bands. When using frequencies in band 1 from 1.6 MHz to 2 MHz, these signals are routed through band 2, as the additional filtering of band 2 helps with harmonic attenuation of band 1 signals from 1.8 MHz to 2 MHz. The AM BCI HPF is used in series with bands 2 through eight to provide 20dB of attenuation for unwanted AM broadcast signals from 550 kHz to 1.65 MHz. The filtered RF then passes through a directional coupler that takes a sample of both forward and reflected RF power at the output of the harmonic filters. At this point, the transmit signal is routed either to the BITE test load or out J3 to the A9 Antenna Coupler.

3.2.3 Harmonic Filter Topology

All the harmonic low pass filters (LPFs) and the AM BCI high pass filter (HPF) are of the elliptical topology. These type of filters provide the steepest possible slope in transition from passband to stopband for a filter of a given order. The order of the filter is how many reactive branches there are in the filter. As the order of the filter increases, the filter transition from passband to stopband becomes steeper and also the ultimate stopband attenuation will be greater. Filter band 1 is a third order elliptical LPF that provides 15 dB of attenuation to harmonics of fundamental signals in frequencies from 1.6 MHz to 2 MHz. The AM BCI HPF is a fifth order elliptical HPF that provides 20 dB of attenuation for signals from 550 kHz to 1.65 MHz. Bands 2 through 7 are seventh order elliptical LPFs of identical design to provide 50dB of attenuation for harmonics of fundamental frequencies from 2 MHz to 30 MHz. Band 8 is a fifth order elliptical LPF that provides 30 dB of attenuation for harmonics of fundamental frequencies from 30 MHz to 60 MHz.

Figure 6 is a representation of band 2 filter attenuation and return loss, and is the typical shape of the LPFs. Return loss is a measure of reflected power (relative to forward power) in dB. Table 3 lists the specifications for all the filters.

HARMONIC FILTER RF SIGNAL FLOW

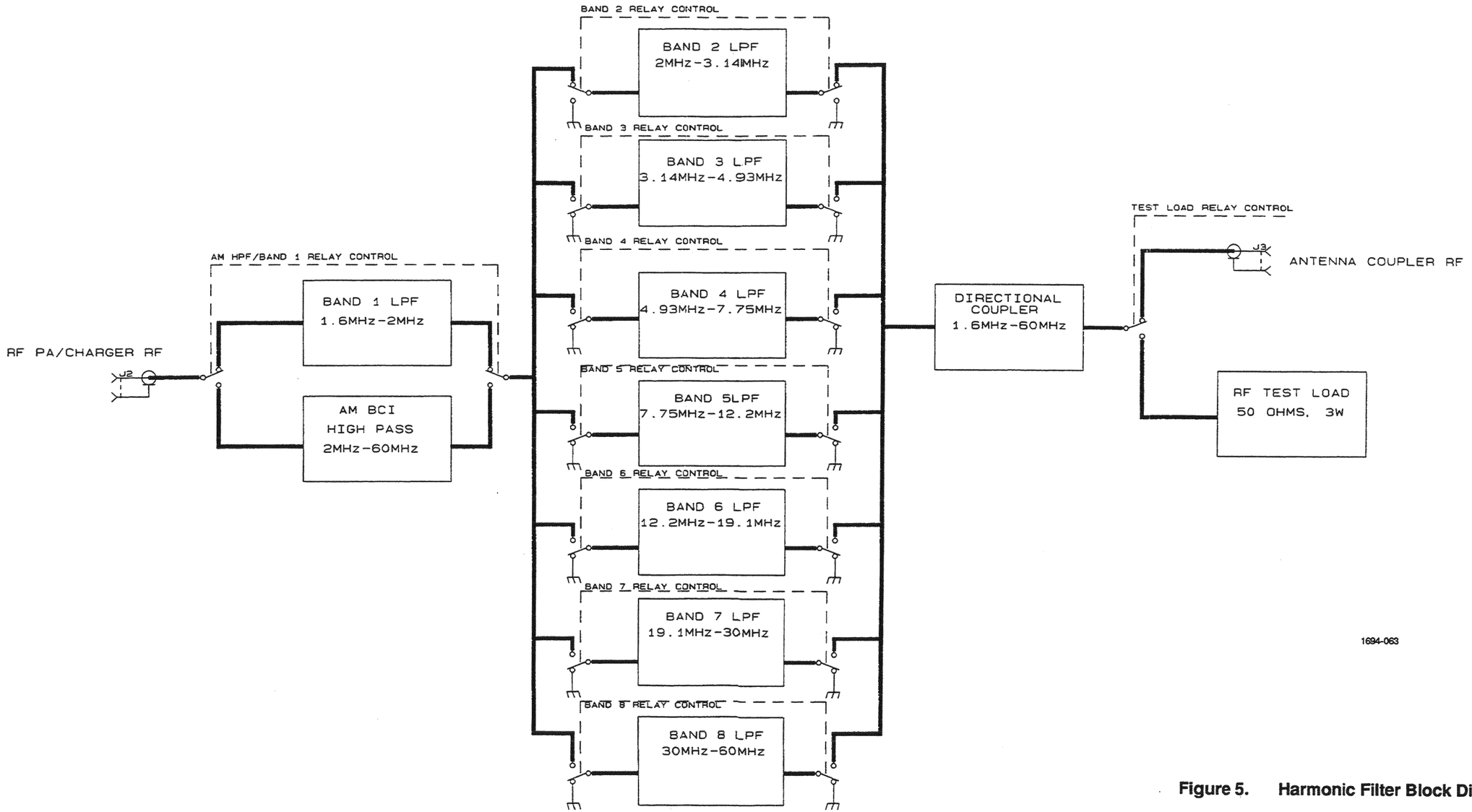


Figure 5. Harmonic Filter Block Diagram

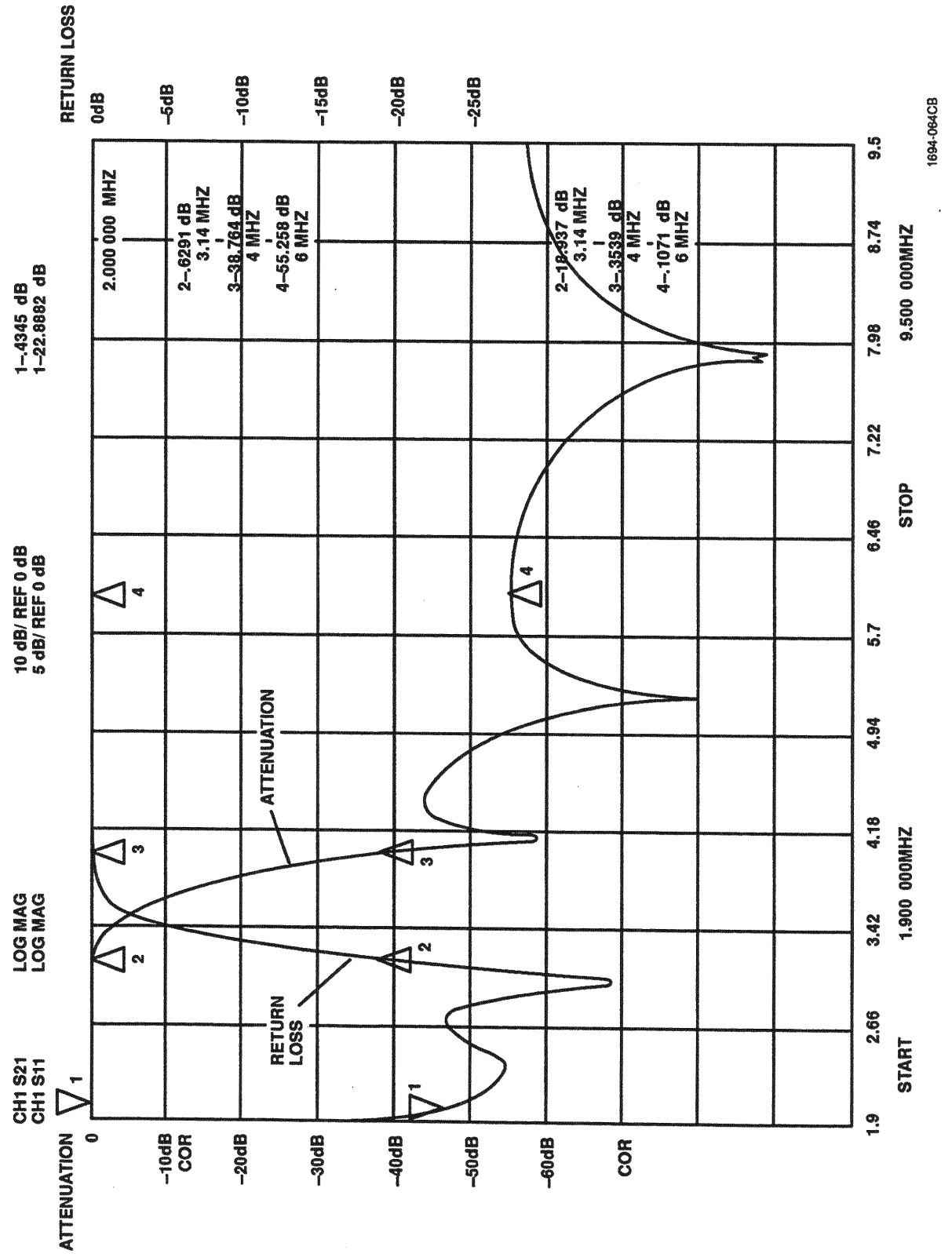


Figure 6. Band 2 Filter Attenuation and Return Loss

Table 3. Harmonic Filter Specifications

Filter Band	Pass Band			Transition Band		Stop Band	
	Freq (MHz)	Atten (dB) (max.)	Return loss (dB) (max.)	Freq (MHz)	Atten (dB) (min.)	Freq (MHz)	Atten (dB) (min.)
AM HPF	2 – 60	–0.25	–17			0.55 – 1.65	–20
1	1.6 – 2	–0.7	–17			3.2 – 3.6 3.6 – 6.0	–15 –50
2	2 – 3.14	–0.7	–17	4 – 4.9	–35	4.9 – 9.42	–50
3	3.14 – 4.93	–0.7	–17	6.28 – 7.75	–35	7.75 – 14.79	–50
4	4.93 – 7.75	–0.7	–17	9.86 – 12.2	–35	12.2 – 23.25	–50
5	7.75 – 12.16	–0.7	–17	15.5 – 19.1	–35	19.1 – 36.5	–50
6	12.16 – 19.1	–0.7	–17	24.3 – 30	–35	30 – 57.3	–50
7	19.1 – 30	–0.7	–17	38.2 – 47	–35	47 – 90	–50
8	30 – 60	–0.7	–17	80 – 110	–30	110 – 180	–40

3.2.4 Directional Coupler and PA TX Power Control

Transformers T1 and T2 are connected together to form a directional coupler with a 13:1 turns ratio, which gives a sample of forward and reflected power coupled at –22.3 dB less than the actual RF power level that passes through the primary of T1 and is across the secondary of T2. The forward power sample is peak detected by CR6 and C138, while the reflected power sample is peak detected by CR3 and C133. Each of these samples is buffered by U3 and sent to the A4 Signal Processor, which uses them to calculate load VSWR, via the A8A1 RF Power Amplifier/Battery Charger VSWR/Battery voltage analog multiplexer and A9 Antenna Coupler feedback described above.

The EFWD voltage at P1 pin 13 should be 3.8 VDC for a continuous 25W of forward power. Additionally, the forward and reflected power samples are amplified and diode ORed together to provide input for RF PA Feedback.

The gain of the forward power amplifier U3B has a voltage gain of 1.09 which requires 25W of forward power to produce the 4.3 V that the PA feedback voltage needs to be when the TGC loop is steady state. There is a high gain mode in which the voltage gain of U3B is increased to 11.82 by Q1 switching R30 in parallel to R31. In the high gain mode only 100 mW of forward power is required to produce 4.3 V of PA feedback which is used for power control when tuning antennae. The reflected power amplifier has a voltage gain of 2.69, which requires 4.3W of reflected power to produce 4.3 V of PA Feedback. With a load VSWR of 2.4:1, 25W of forward power will cause 4.3W of reflected power and any VSWR greater than 2.4:1 will require less than 25W of forward power to produce 4.3W of reflected power. The diode ORing nature of the PA feedback signal works under the principle that whichever feedback signal is driven to 4.3 V by the least amount of exciter drive will control the transmitter power out, and with a load VSWR of greater than 2.4:1 the reflected power portion of the diode OR will reach 4.3 V before the forward power reaches 25W and the transmitter will be under reflected power control. These diode ORed signals are sent to the A8A1 RF Power Amplifier/Battery Charger at P1 pin 11 where they are additionally ORed with battery current limit and external RF PA feedback signals.

4. TESTING AND ALIGNMENT

The A8 Power Amplifier/Battery Charger Assembly has no regular test or alignment necessary. If RF PA transistors are replaced, the DC bias adjustment should be performed as follows:

a. Remove the outer case from the radio.

b. Disconnect and remove the A8 Power Amplifier/Battery Charger Assembly from the rear of the radio as described in the General Information section of this manual (section 1.9.1).

c. Remove the A8A2 Harmonic Filter Assembly and reconnect the A8A1 RF Power Amplifier/Battery Charger Assembly to the A11 Motherboard. Leave the RF cables from the A5 Receiver/Exciter and the A9 Antenna Coupler disconnected.

d. Adjust R36, R48, and R49 fully CCW.

e. Power the radio through one battery connector and insert DVM current meter capable of 1.5A in battery input.

f. Turn on radio in CW and assert PTT keyline; note current draw from +24 V battery input.

g. Adjust R36 CW until the battery current draw increases by 300 mA.

h. Adjust R48 CW for an additional 50 mA of battery current.

i. Adjust R49 CW for an additional 50 mA of battery current to give a total bias of 400 mA greater than the reading taken in step f.

j. Reconnect the A8A2 Harmonic Filter Assembly and both RF cables and reinstall the A8 Power Amplifier/Battery Charger Assembly into the radio.

k. Connect a known good BB-590/U Battery (or be sure battery pin 1 is connected to battery pin 3). Run self test and verify that the A8 Power Amplifer/Battery Charger Assembly is properly functioning. The VSWR test can also be used to verify full power output at any desired frequency.

5. BITE FAULTS AND TROUBLESHOOTING

The A8 Power Amplifier/Battery Charger Assembly has a single bite test, which is to attempt to transmit 5W of RF power into the bite test load on the A8A2 Harmonic Filter Assembly through each of the eight possible filter bands in the A8A2 Harmonic Filter Assembly. There are 256 possible fault codes so, the fault code structure along with a couple of examples are given below. The fault codes are bit mapped in a hex byte so that each of the eight filter bands is a bit as shown below:

A08 FAULT Fx1x2

x1	x2	HEX Byte
B8 B7 B6 B5	B4 B3 B2 B1	Binary Filter Band Conversion

TX Power Successful, Binary Bit = 0
TX Power Failure, Binary Bit = 1

EXAMPLE: A08 Fault F08

x1=0, x2=8 Hexidecimal
0 0 0 0, 1 0 0 0 Binary
B8 B7 B6 B5, B4 B3 B2 B1 Filters

There is a failure in Band 4 of the Harmonic Filters, all other bands are OK. Swap A8A2 Harmonic Filter PWB of A8 Assembly and repeat BITE. If BITE passes, troubleshoot Band 4 of original 10303-2140 PWB Assembly.

EXAMPLE: A08 Fault FFF

x1=F, x2=F Hexidecimal
1 1 1 1, 1 1 1 1 Binary
B8 B7 B6 B5, B4 B3 B2 B1 Filters

There is no power in any filter band. Swap with a known good A8A1 Assembly and repeat the BITE. If the BITE passes, troubleshoot the original A8A1 Assembly. If the BITE still fails, check for powering from A10 Front Panel external P/A power. Power from this source will cause the radio to inhibit internal 25W RF PA operation and the BITE will fail. Check for good battery power level from BB-590/U. Low battery voltage will inhibit TX keying. If using BA-5590/U Lithium batteries, be sure both batteries are present. TX current limit will cut back TX power with only one lithium Battery and the BITE may fail.

5.1 Troubleshooting the A8 Assembly using VSWR BITE

When an A08 BITE fault is encountered, try the VSWR test at a frequency within the failed filter band to verify the filter band is bad. If a good VSWR is measured, but power out is low, the problem is probably in the A8A1 RF Power Amplifier/Battery Charger Assembly. If a bad VSWR is measured, check your load and try retuning the A9 Antenna Coupler to get a good VSWR. If this is not possible, there is an A9 Antenna Coupler problem at that frequency. If little or no power out is measured on the VSWR test in the bad filter band, try another frequency in a different band and if the new frequency works, then the original band is bad. Replace the A8A2 Harmonic Filter Assembly.

6. PARTS LISTS, COMPONENT LOCATION DIAGRAMS, AND SCHEMATIC DIAGRAMS

Tables 4 and 5 are the parts lists, figure 7 and 8 are the component location and schematic diagrams for the A8A1 Power Amplifier/Battery Charger PWB Assembly. Tables 6 is the parts list and figures 9 and 11 are the component location and schematic diagrams for the A8A2 Power Amplifier/Battery Charger PWB Assembly.

Table 4. A8 Power Amplifier/Battery Charger Assembly Parts List (10372-1400-01 Rev. D)

Ref. Desig.	Part Number	Description
A1	10372-1400-01	PWB ASSY PWR AMP/BATT CH
A2	10372-1400-01	PWB ASSY, HARMONIC FILTER
J7	10012-0347	CONNECTOR
J8	10012-0347	CONNECTOR

Table 5. A8A1 Power Amplifier/Battery Charger PWB Assembly (10303-2130 Rev. T)

Ref. Desig.	Part Number	Description
1	10303-2131	SCHEMATIC, RF PA/CHARGER
2	10303-1202-01	SUPPORT, RECEPTACLE
3	W20-0001-010	WIRE BUSS #22AWG TIN'D CU
4	H65-0005-003	STDOFF PRESS-FIT .093 L
5	E70-0002-002	PAD MNT XSTR TO-5
6	E50-0003-005	SLVG TFL .042 ID 18GA NAT
7	J60-0012-001	SOCKET, FUSE, HDWR SP.INC
8	P15-3140-000	SEALER RTV 3140
9	10303-2139	PWB, RFPA/CHARGER
11	P05-0003-013	TAPE,FM,CL CELL,3/16X1/2
C1	C13-0101-101	CAP 100PF 10% 100V SMD
C2	C13-0101-101	CAP 100PF 10% 100V SMD
C3	C13-0103-333	CAP .033UF 10% 100V SMD
C4	C13-0103-333	CAP .033UF 10% 100V SMD
C5	C13-0101-101	CAP 100PF 10% 100V SMD
C6	C13-0101-101	CAP 100PF 10% 100V SMD
C7	C13-0101-101	CAP 100PF 10% 100V SMD
C8	C13-0101-101	CAP 100PF 10% 100V SMD
C9	C13-0101-101	CAP 100PF 10% 100V SMD
C10	C13-0101-101	CAP 100PF 10% 100V SMD
C11	C13-0103-333	CAP .033UF 10% 100V SMD
C13	C14-0001-185	CAP 1.8UF 50V
C14	C36-0035-105	CAP 1UF 35V SMT
C15	C36-0035-105	CAP 1UF 35V SMT
C16	C36-0035-105	CAP 1UF 35V SMT
C17	C36-0035-105	CAP 1UF 35V SMT
C18	C13-0103-333	CAP .033UF 10% 100V SMD
C19	C13-0103-103	CAP .01UF 10% 100V SMD
C21	C13-0107-104	CAP, .1UF 10% 100V CER
C22	C13-0107-104	CAP, .1UF 10% 100V CER
C23	C13-0107-104	CAP, .1UF 10% 100V CER
C24	C13-0107-104	CAP, .1UF 10% 100V CER
C25	C13-0107-104	CAP, .1UF 10% 100V CER
C26	C13-0105-102	CAP CER 1000PF 5% 100V
C27	C13-0103-333	CAP .033UF 10% 100V SMD
C28	C11-0062-221	CAP 220PF 5% 150V
C29	C13-0107-104	CAP, .1UF 10% 100V CER
C30	C13-0107-104	CAP, .1UF 10% 100V CER
C31	C11-0062-221	CAP 220PF 5% 150V

Table 5. A8A1 Power Amplifier/Battery Charger PWB Assembly (10303-2130 Rev. T) (Cont.)

Ref. Desig.	Part Number	Description
C32	C18-0052-107	CAP 100UF 20% 50V ELEC
C35	C13-0107-104	CAP, .1UF 10% 100V CER
C36	C13-0107-104	CAP, .1UF 10% 100V CER
C38	C13-0107-104	CAP, .1UF 10% 100V CER
C39	C13-0107-104	CAP, .1UF 10% 100V CER
C40	C13-0107-104	CAP, .1UF 10% 100V CER
C48	C13-0103-103	CAP .01UF 10% 100V SMD
C49	C13-0107-104	CAP, .1UF 10% 100V CER
C50	C13-0107-104	CAP, .1UF 10% 100V CER
C51	C13-0107-104	CAP, .1UF 10% 100V CER
C52	C36-0006-106	CAP, 10UF, 10% 6V SMD
C53	C13-0107-104	CAP, .1UF 10% 100V CER
C54	C36-0006-106	CAP, 10UF, 10% 6V SMD
C55	C13-0107-104	CAP, .1UF 10% 100V CER
C56	C13-0105-360	CAP, CERAMIC CHIP, 36PF
C57	C13-0107-104	CAP, .1UF 10% 100V CER
C58	C36-0035-105	CAP 1UF 35V SMT
C59	C13-0107-104	CAP, .1UF 10% 100V CER
C61	C13-0105-102	CAP CER 1000PF 5% 100V
C62	C13-0105-102	CAP CER 1000PF 5% 100V
C63	C13-0103-333	CAP .033UF 10% 100V SMD
C64	C13-0103-103	CAP .01UF 10% 100V SMD
C65	C13-0103-103	CAP .01UF 10% 100V SMD
C66	C13-0107-104	CAP, .1UF 10% 100V CER
C68	C13-0107-104	CAP, .1UF 10% 100V CER
C70	C13-0105-102	CAP CER 1000PF 5% 100V
C71	C13-0105-102	CAP CER 1000PF 5% 100V
C72	C13-0103-103	CAP .01UF 10% 100V SMD
C73	C13-0103-103	CAP .01UF 10% 100V SMD
C74	C14-0001-185	CAP 1.8UF 50V
C75	C14-0001-185	CAP 1.8UF 50V
C77	C14-0001-185	CAP 1.8UF 50V
C78	M39006/25-0051	CAP,ELECT 120UF 50V
C79	C36-0025-475	CAP, TANT, 4.7UF 25V SMD
C80	C13-0103-103	CAP .01UF 10% 100V SMD
C81	M39006/25-0050	CAP,ELECT 33UF 50V
C82	C13-0101-101	CAP 100PF 10% 100V SMD
C83	C13-0103-152	CAP 1500PF 10% 100V SMD
C84	C13-0101-471	CAP 470PF 10% 100V SMD

Table 5. A8A1 Power Amplifier/Battery Charger PWB Assembly (10303-2130 Rev. T) (Cont.)

Ref. Desig.	Part Number	Description
C85	C13-0103-103	CAP .01UF 10% 100V SMD
C86	C13-0103-153	CAP,CERAMIC CHIP .015UF
C87	C13-0107-104	CAP, .1UF 10% 100V CER
C89	C13-0103-103	CAP .01UF 10% 100V SMD
C90	C14-0001-185	CAP 1.8UF 50V
C91	C14-0001-185	CAP 1.8UF 50V
C92	C14-0001-185	CAP 1.8UF 50V
C93	C14-0001-185	CAP 1.8UF 50V
C94	M39006/25-0051	CAP,ELECT 120UF 50V
C95	C36-0025-475	CAP, TANT, 4.7UF 25V SMD
C96	C13-0103-103	CAP .01UF 10% 100V SMD
C97	M39006/25-0050	CAP,ELECT 33UF 50V
C98	C13-0101-101	CAP 100PF 10% 100V SMD
C99	C13-0103-152	CAP 1500PF 10% 100V SMD
C100	C13-0101-471	CAP 470PF 10% 100V SMD
C101	C13-0103-103	CAP .01UF 10% 100V SMD
C102	C13-0103-153	CAP,CERAMIC CHIP .015UF
C103	C13-0107-104	CAP, .1UF 10% 100V CER
C105	C13-0103-103	CAP .01UF 10% 100V SMD
C106	C13-0103-103	CAP .01UF 10% 100V SMD
C107	C13-0103-103	CAP .01UF 10% 100V SMD
C108	C13-0103-103	CAP .01UF 10% 100V SMD
C109	C13-0103-103	CAP .01UF 10% 100V SMD
C110	C13-0103-333	CAP .033UF 10% 100V SMD
C111	C13-0103-333	CAP .033UF 10% 100V SMD
C112	C13-0107-104	CAP, .1UF 10% 100V CER
C113	C13-0103-333	CAP .033UF 10% 100V SMD
C114	C13-0105-102	CAP CER 1000PF 5% 100V
C115	C13-0105-102	CAP CER 1000PF 5% 100V
C116	C13-0105-102	CAP CER 1000PF 5% 100V
C117	C13-0105-102	CAP CER 1000PF 5% 100V
C118	C36-0050-154	CAP 0.15UF 10% 50V TANT
C121	C13-0105-102	CAP CER 1000PF 5% 100V
C123	C13-0103-103	CAP .01UF 10% 100V SMD
C124	C13-0103-103	CAP .01UF 10% 100V SMD
C126	C13-0105-102	CAP CER 1000PF 5% 100V
C127	C13-0107-104	CAP, .1UF 10% 100V CER
CR1	D22-0033-005	MURS140T3
CR4	D22-0033-005	MURS140T3

Table 5. A8A1 Power Amplifier/Battery Charger PWB Assembly (10303-2130 Rev. T) (Cont.)

Ref. Desig.	Part Number	Description
CR7	D15-0914-101	DIODE HI-SPD SWITCHING
CR13	D22-0034-004	MBRD660CT DUAL CR
CR14	D22-0034-004	MBRD660CT DUAL CR
CR15	D22-0034-004	MBRD660CT DUAL CR
CR16	D15-0914-101	DIODE HI-SPD SWITCHING
CR17	D22-0033-005	MURS140T3
CR18	D15-0914-101	DIODE HI-SPD SWITCHING
CR19	D15-0914-101	DIODE HI-SPD SWITCHING
CR20	D15-0914-101	DIODE HI-SPD SWITCHING
CR21	D15-0914-101	DIODE HI-SPD SWITCHING
CR23	D22-0034-004	MBRD660CT DUAL CR
CR26	D15-0914-101	DIODE HI-SPD SWITCHING
CR27	D15-0914-101	DIODE HI-SPD SWITCHING
CR28	D22-0034-004	MBRD660CT DUAL CR
CR29	1N5305	DIODE CURRENT REGULATING
CR30	D22-0033-005	MURS140T3
CR31	D22-0033-005	MURS140T3
CR32	D22-0033-005	MURS140T3
CR33	D20-0005-001	DIODE, SOT-23
CR34	D20-0005-001	DIODE, SOT-23
CR35	D22-0034-004	MBRD660CT DUAL CR
CR36	1N5305	DIODE CURRENT REGULATING
CR37	D22-0033-005	MURS140T3
CR38	D22-0033-005	MURS140T3
CR39	D22-0033-005	MURS140T3
CR40	D20-0005-001	DIODE, SOT-23
CR41	D20-0005-001	DIODE, SOT-23
CR44	D15-0914-101	DIODE HI-SPD SWITCHING
CR45	D15-0914-101	DIODE HI-SPD SWITCHING
CR46	D15-0914-101	DIODE HI-SPD SWITCHING
CR47	D15-0914-101	DIODE HI-SPD SWITCHING
CR48	D15-0914-101	DIODE HI-SPD SWITCHING
CR49	D15-0914-101	DIODE HI-SPD SWITCHING
CR50	D15-0914-101	DIODE HI-SPD SWITCHING
CR51	D15-7000-001	DIODE GP/SW SMD MMBD7000
E7	L50-0003-006	FERRITE BEAD
E8	L50-0003-006	FERRITE BEAD
F1	F15-0001-015	FUSE 7A, 125V
F3	F15-0001-015	FUSE 7A, 125V

Table 5. A8A1 Power Amplifier/Battery Charger PWB Assembly (10303-2130 Rev. T) (Cont.)

Ref. Desig.	Part Number	Description
J2	J92-0003-001	CONN SSMB RTANG PCB M
J3	J92-0020-001	RECEPTACLE, RF
J4	J46-0087-122	CONN PC.1 TOP ENTR 22 PIN
J5	J46-0022-004	HDR 4 PIN 0.100" SR LKG
J6	J46-0022-004	HDR 4 PIN 0.100" SR LKG
K1	K16-0007-024	DPDT RELAY DPDT1L
K2	K16-0007-224	DPDT RELAY DPDT
K4	K28-0008-524	RELAY, SPDT 24V, LOW PWR
K5	K10-0004-124	RELAY DPDT 24V LATCHING
K6	K10-0004-124	RELAY DPDT 24V LATCHING
L1	L45-0008-012	INDUCTOR, 100 UH SMT
L2	L45-0008-012	INDUCTOR, 100 UH SMT
L3	L45-0008-012	INDUCTOR, 100 UH SMT
L4	10303-3106-17	TOROID ASSY, 19UH
L5	10303-3142-01	INDUCTOR, .17UH
L6	10303-3142-01	INDUCTOR, .17UH
L7	10303-3106-18	TOROID ASSY, 2:1UH
L8	L45-0008-012	INDUCTOR, 100 UH SMT
L9	10303-3178-01	IN,1041CT060-3E2A,18T#30
L11	10303-3177-01	INDUCT,T25-17,9 TURNS,#24
L12	10303-3178-01	IN,1041CT060-3E2A,18T#30
P1	J46-0055-034	HEADER RT ANGLE 34 PIN
Q1	Q12-2222-101	XSTR NPN SWG SM SS/GP
Q2	Q12-2222-101	XSTR NPN SWG SM SS/GP
Q3	2N7002	TRANSISTOR, FET (SOT-23)
Q4	10303-3132	XSTR FFT POWER
Q5	10303-3131	XSTR FFT POWER
Q6	Q02-2907-101	XSTR SS/GP PNP MMBT2907A
Q8	Q02-2907-101	XSTR SS/GP PNP MMBT2907A
Q9	Q02-2907-101	XSTR SS/GP PNP MMBT2907A
Q10	2N7002	TRANSISTOR, FET (SOT-23)
Q11	2N7002	TRANSISTOR, FET (SOT-23)
Q12	2N7002	TRANSISTOR, FET (SOT-23)
Q13	Q12-2222-101	XSTR NPN SWG SM SS/GP
Q14	Q26-0034-003	MOSFET, 60V 9.6A DPAK
Q15	Q12-2222-101	XSTR NPN SWG SM SS/GP
Q16	Q02-2907-101	XSTR SS/GP PNP MMBT2907A
Q17	Q12-2222-101	XSTR NPN SWG SM SS/GP
Q18	Q02-2907-101	XSTR SS/GP PNP MMBT2907A

Table 5. A8A1 Power Amplifier/Battery Charger PWB Assembly (10303-2130 Rev. T) (Cont.)

Ref. Desig.	Part Number	Description
Q20	Q50-0019-001	XSTR, DARLINGTON
Q21	Q26-0036-001	TRANSISTOR,TMOS (MTD6N15)
Q22	Q26-0036-001	TRANSISTOR,TMOS (MTD6N15)
Q23	Q50-0019-001	XSTR, DARLINGTON
Q24	Q26-0036-001	TRANSISTOR,TMOS (MTD6N15)
Q25	Q26-0036-001	TRANSISTOR,TMOS (MTD6N15)
Q26	2N7002	TRANSISTOR, FET (SOT-23)
Q27	2N7002	TRANSISTOR, FET (SOT-23)
Q28	2N7002	TRANSISTOR, FET (SOT-23)
R1	R85-0004-101	RES 100 1% 1/8W FLM
R2	R85-0004-101	RES 100 1% 1/8W FLM
R3	R85-0004-101	RES 100 1% 1/8W FLM
R4	R85-0004-101	RES 100 1% 1/8W FLM
R5	R85-0004-301	RES 10K 1% 1/8W FLM
R6	R85-0004-301	RES 10K 1% 1/8W FLM
R8	R85-0004-101	RES 100 1% 1/8W FLM
R9	R85-0004-301	RES 10K 1% 1/8W FLM
R10	R85-0004-101	RES 100 1% 1/8W FLM
R11	R85-0004-366	RES 47.5K 1% 1/8W FLM
R16	R85-0004-301	RES 10K 1% 1/8W FLM
R17	R85-0004-366	RES 47.5K 1% 1/8W FLM
R18	R85-0004-366	RES 47.5K 1% 1/8W FLM
R19	R85-0004-101	RES 100 1% 1/8W FLM
R20	R85-0004-301	RES 10K 1% 1/8W FLM
R22	R85-0004-301	RES 10K 1% 1/8W FLM
R24	R85-0004-466	RES 475K 1% 1/8W CHIP
R25	R85-0004-401	RES 100K 1% 1/8W FLM
R26	R85-0004-172	549 R
R27	R85-0004-266	RES,4.75K 1% 1/8W CHIP
R28	R85-0004-018	RES 15.0 1% 1/8W FLM
R29	R85-0006-162	RES 432 1%
R30	R85-0004-226	RES 1.82K 1% 1/8W CHIP
R31	R85-0015-011	RES. 1.1, 1/2W SORT
R35	R85-0004-255	RES 3650 1% 1/8W FLM
R36	R30-0015-103	TRIMMER 10K
R37	R85-0004-366	RES 47.5K 1% 1/8W FLM
R38	R85-0004-301	RES 10K 1% 1/8W FLM
R39	R85-0004-226	RES 1.82K 1% 1/8W CHIP
R40	R85-0013-051	RES. 33.2, 1W SORT

Table 5. A8A1 Power Amplifier/Battery Charger PWB Assembly (10303-2130 Rev. T) (Cont.)

Ref. Desig.	Part Number	Description
R42	R85-0015-051	RES. 5.1, 1/2W SORT
R45	R85-0004-209	RES FILM 1.21K 1% 1/8 SMD
R46	R85-0004-289	RES 8250 1% 1/8W FLM
R47	R85-0004-289	RES 8250 1% 1/8W FLM
R48	R30-0015-103	TRIMMER 10K
R49	R30-0015-103	TRIMMER 10K
R50	R85-0013-051	RES. 33.2, 1W SORT
R52	R85-0015-051	RES. 5.1, 1/2W SORT
R54	R85-0004-134	RES 221 1% 1/8W FLM
R55	R85-0004-209	RES FILM 1.21K 1% 1/8 SMD
R56	R85-0004-301	RES 10K 1% 1/8W FLM
R57	R85-0004-224	RES 1.74K 1% 1/8W SMD
R58	R85-0004-266	RES,4.75K 1% 1/8W CHIP
R59	R85-0004-301	RES 10K 1% 1/8W FLM
R60	R85-0004-301	RES 10K 1% 1/8W FLM
R61	R85-0004-301	RES 10K 1% 1/8W FLM
R62	R85-0004-301	RES 10K 1% 1/8W FLM
R63	R85-0004-301	RES 10K 1% 1/8W FLM
R64	R85-0004-466	RES 475K 1% 1/8W CHIP
R65	R85-0004-301	RES 10K 1% 1/8W FLM
R66	R85-0004-466	RES 475K 1% 1/8W CHIP
R67	R85-0004-401	RES 100K 1% 1/8W FLM
R68	R85-0004-301	RES 10K 1% 1/8W FLM
R70	R85-0004-301	RES 10K 1% 1/8W FLM
R71	R85-0004-466	RES 475K 1% 1/8W CHIP
R72	R85-0004-466	RES 475K 1% 1/8W CHIP
R73	R85-0004-273	RES 5.62K 1% 1/8W FLM
R74	R85-0004-418	RES 150K 1% 1/8W FLM
R75	R85-0004-326	RES,18.2K 1% 1/8W CHIP
R76	R85-0004-334	RES 22.1K 1% 1/8W FLM
R77	R85-0004-334	RES 22.1K 1% 1/8W FLM
R78	R85-0004-366	RES 47.5K 1% 1/8W FLM
R80	R85-0004-466	RES 475K 1% 1/8W CHIP
R81	R85-0004-466	RES 475K 1% 1/8W CHIP
R83	10303-3134	RESISTOR NETWORK
R85	R85-0004-466	RES 475K 1% 1/8W CHIP
R86	R85-0004-347	RES 30.1K 1% 1/8W FLM
R87	R85-0004-377	RES 61.9K 1% 1/8W FLM
R88	R85-0004-240	RES 2.55K 1% 1/8W SMD

Table 5. A8A1 Power Amplifier/Battery Charger PWB Assembly (10303-2130 Rev. T) (Cont.)

Ref. Desig.	Part Number	Description
R89	R85-0004-334	RES 22.1K 1% 1/8W FLM
R90	R85-0004-334	RES 22.1K 1% 1/8W FLM
R91	R85-0004-334	RES 22.1K 1% 1/8W FLM
R92	R85-0004-301	RES 10K 1% 1/8W FLM
R93	R85-0004-366	RES 47.5K 1% 1/8W FLM
R94	R85-0007-004	RES. 4.3OHM 1/4W 5% SMT
R95	R85-0004-334	RES 22.1K 1% 1/8W FLM
R96	R85-0004-334	RES 22.1K 1% 1/8W FLM
R97	R85-0004-334	RES 22.1K 1% 1/8W FLM
R98	R85-0004-255	RES 3650 1% 1/8W FLM
R99	R85-0004-366	RES 47.5K 1% 1/8W FLM
R100	R85-0004-366	RES 47.5K 1% 1/8W FLM
R101	R85-0004-301	RES 10K 1% 1/8W FLM
R102	10303-3134	RESISTOR NETWORK
R103	R85-0004-466	RES 475K 1% 1/8W CHIP
R104	R85-0004-347	RES 30.1K 1% 1/8W FLM
R105	R85-0004-377	RES 61.9K 1% 1/8W FLM
R106	R12-0011-001	RES, .1 1%, 1.5W WW
R107	R85-0007-004	RES. 4.3OHM 1/4W 5% SMT
R108	R85-0004-401	RES 100K 1% 1/8W FLM
R109	R85-0004-240	RES 2.55K 1% 1/8W SMD
R110	R85-0004-001	RES, 10 1% 1/8W CHIP
R111	R85-0004-173	RES 562 1% 1/8W FLM
R112	R85-0004-301	RES 10K 1% 1/8W FLM
R113	R85-0004-001	RES, 10 1% 1/8W CHIP
R114	R85-0004-001	RES, 10 1% 1/8W CHIP
R115	R85-0004-201	RES 1000 1% 1/8W FLM
R116	R12-0010-001	RES, .33 1/2W 1%
R117	R85-0004-366	RES 47.5K 1% 1/8W FLM
R118	R85-0004-366	RES 47.5K 1% 1/8W FLM
R119	R85-0004-366	RES 47.5K 1% 1/8W FLM
R120	R85-0004-443	RES, 274K 1% 1/8W CHIP
R121	R85-0004-234	RES 2.21K 1% 1/8W FLM
R122	R85-0004-501	RES 1M 1% 1/8W CHIP
R123	R85-0004-301	RES 10K 1% 1/8W FLM
R124	R85-0004-234	RES 2.21K 1% 1/8W FLM
R125	R85-0004-501	RES 1M 1% 1/8W CHIP
R126	R85-0004-301	RES 10K 1% 1/8W FLM
R127	R85-0004-389	RES 82.5K 1% 1/8W FLM

Table 5. A8A1 Power Amplifier/Battery Charger PWB Assembly (10303-2130 Rev. T) (Cont.)

Ref. Desig.	Part Number	Description
R128	R85-0004-001	RES, 10 1% 1/8W CHIP
R129	R85-0004-173	RES 562 1% 1/8W FLM
R130	R85-0004-301	RES 10K 1% 1/8W FLM
R131	R85-0004-001	RES, 10 1% 1/8W CHIP
R132	R85-0004-001	RES, 10 1% 1/8W CHIP
R133	R85-0004-201	RES 1000 1% 1/8W FLM
R134	R85-0004-366	RES 47.5K 1% 1/8W FLM
R135	R12-0010-001	RES, .33 1/2W 1%
R136	R85-0004-366	RES 47.5K 1% 1/8W FLM
R137	R85-0004-366	RES 47.5K 1% 1/8W FLM
R138	R85-0004-443	RES, 274K 1% 1/8W CHIP
R139	R85-0004-234	RES 2.21K 1% 1/8W FLM
R140	R85-0004-501	RES 1M 1% 1/8W CHIP
R141	R85-0004-301	RES 10K 1% 1/8W FLM
R142	R85-0004-501	RES 1M 1% 1/8W CHIP
R143	R85-0004-234	RES 2.21K 1% 1/8W FLM
R144	R85-0004-301	RES 10K 1% 1/8W FLM
R145	R85-0004-389	RES 82.5K 1% 1/8W FLM
R146	R85-0004-366	RES 47.5K 1% 1/8W FLM
R147	R85-0004-301	RES 10K 1% 1/8W FLM
R150	R12-0011-001	RES, .1 1%, 1.5W WW
R151	R85-0004-401	RES 100K 1% 1/8W FLM
R152	R85-0004-301	RES 10K 1% 1/8W FLM
R157	R85-0004-224	RES 1.74K 1% 1/8W SMD
R162	R85-0004-224	RES 1.74K 1% 1/8W SMD
R163	R85-0004-401	RES 100K 1% 1/8W FLM
R164	R85-0004-466	RES 475K 1% 1/8W CHIP
R165	R85-0004-366	RES 47.5K 1% 1/8W FLM
R166	R85-0004-234	RES 2.21K 1% 1/8W FLM
R167	R85-0004-234	RES 2.21K 1% 1/8W FLM
R168	R85-0004-234	RES 2.21K 1% 1/8W FLM
RT1	D40-0014-001	THERMISTOR ASSY
RT2	10372-9400	THERMISTOR ASSY
T1	10303-3179-01	RF DRIVER XFMR
T2	10303-3180-01	ASSY, BROADBAND RF XFMR
T3	10385-1127	CHOKE,COMMON-MODE
T4	10385-1127	CHOKE,COMMON-MODE
T5	10385-1127	CHOKE,COMMON-MODE
T6	10385-1126	TRANSFORMER

Table 5. A8A1 Power Amplifier/Battery Charger PWB Assembly (10303-2130 Rev. T) (Cont.)

Ref. Desig.	Part Number	Description
T7	10385-1127	CHOKE,COMMON-MODE
T8	10385-1126	TRANSFORMER
U1	I01-5000-367	BUS DRIVER, HEX (74HC367)
U2	I01-5000-595	IC, 8-BIT SHIFT REG.
U3	I06-0015-003	IC, QUAD CMOS SW DG412DY
U4	I01-5000-165	IC 74HC165 SHIFT REG SOIC
U5	I06-0013-101	DUAL SPDT SWITCH DG403AB
U6	I11-0015-008	REGULATOR, SM
U7	I69-0002-001	IC MWA110 RF AMP WBW TO39
U8	I20-0010-004	IC LM2903D COMPARATORD
U9	I30-0041-005	IC, QUAD OP AMP, TL034AID
U10	I30-0041-005	IC, QUAD OP AMP, TL034AID
U11	I62-0016-101	PWM CONTROL UC2843AD
U12	I30-0049-005	MC33172D
U13	I62-0016-101	PWM CONTROL UC2843AD
U14	I30-0049-005	MC33172D
U15	I06-0015-003	IC, QUAD CMOS SW DG412DY
VR2	D05-0005-020	DIODE, ZENER 15V SOT-23
VR3	D05-0005-017	DIODE, 12V ZENER SMT
VR4	D05-0005-025	DIODE 20V .25W SMD
VR5	D05-0005-032	33V ZENER _VRSOT23
VR6	D05-0005-017	DIODE, 12V ZENER SMT
VR7	D05-0005-025	DIODE 20V .25W SMD
VR8	D05-0005-032	33V ZENER _VRSOT23
VR9	D05-0005-007	DIODE 5.1V 5% SOT ZENER
VR10	D05-0005-007	DIODE 5.1V 5% SOT ZENER

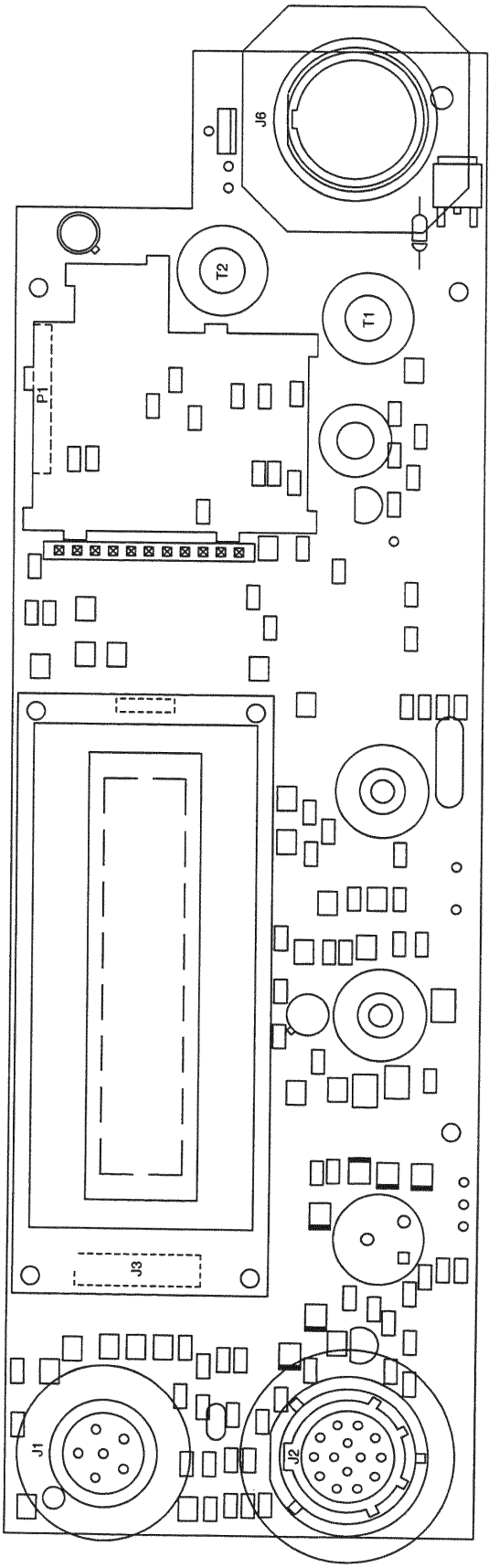


Figure 7. A8A1 Power Amplifier/Battery Charger PWB Assembly Component Location Diagram
(10303-2130 Rev. D) (Sheet 1 of 2)

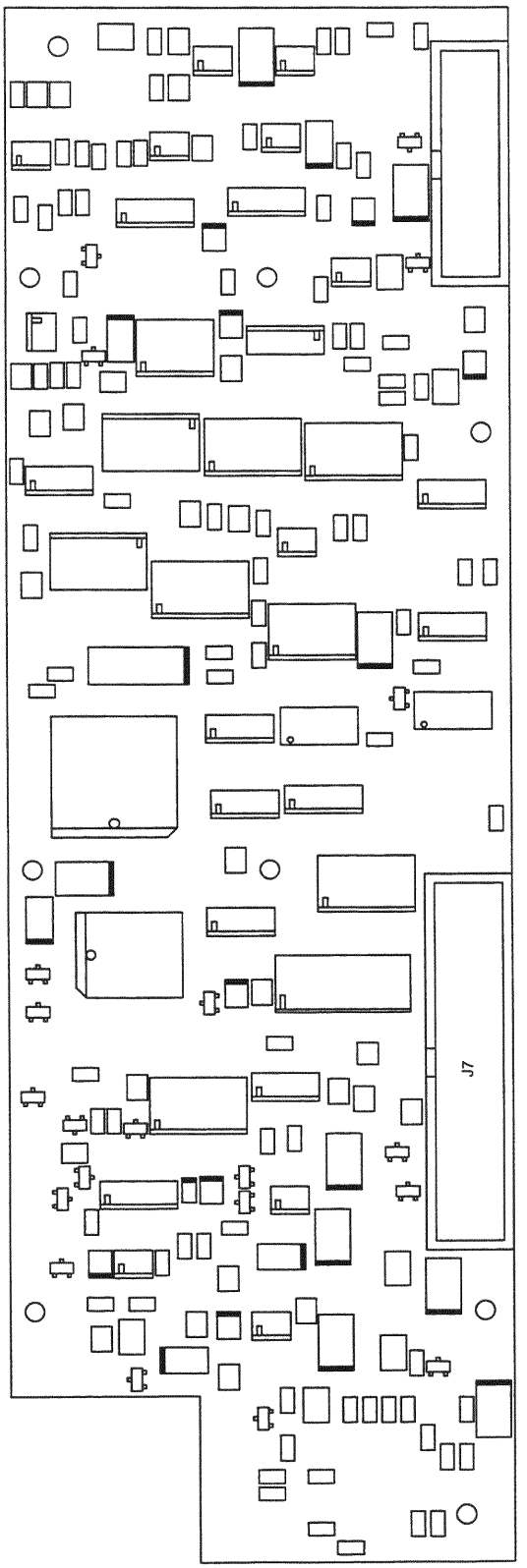


Figure 7. A8A1 Power Amplifier/Battery Charger PWB Assembly Component Location Diagram
(10303-2130 Rev. D) (Sheet 2 of 2)

NOTE: UNLESS OTHERWISE SPECIFIED:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR A COMPLETE DESIGNATION, PREFIX WITH UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.
2. ALL RESISTOR VALUES ARE IN OHMS, 1/8W, +/-1%.
3. ALL CAPACITOR VALUES ARE IN MICROFARADS.
4. VENDOR PART NO. CALLOUTS ARE FOR REFERENCE ONLY. COMPONENTS ARE SUPPLIED PER PART NO. IN PARTS LIST.
5. BACKSLASH (/) DENOTES ACTIVE LOW.

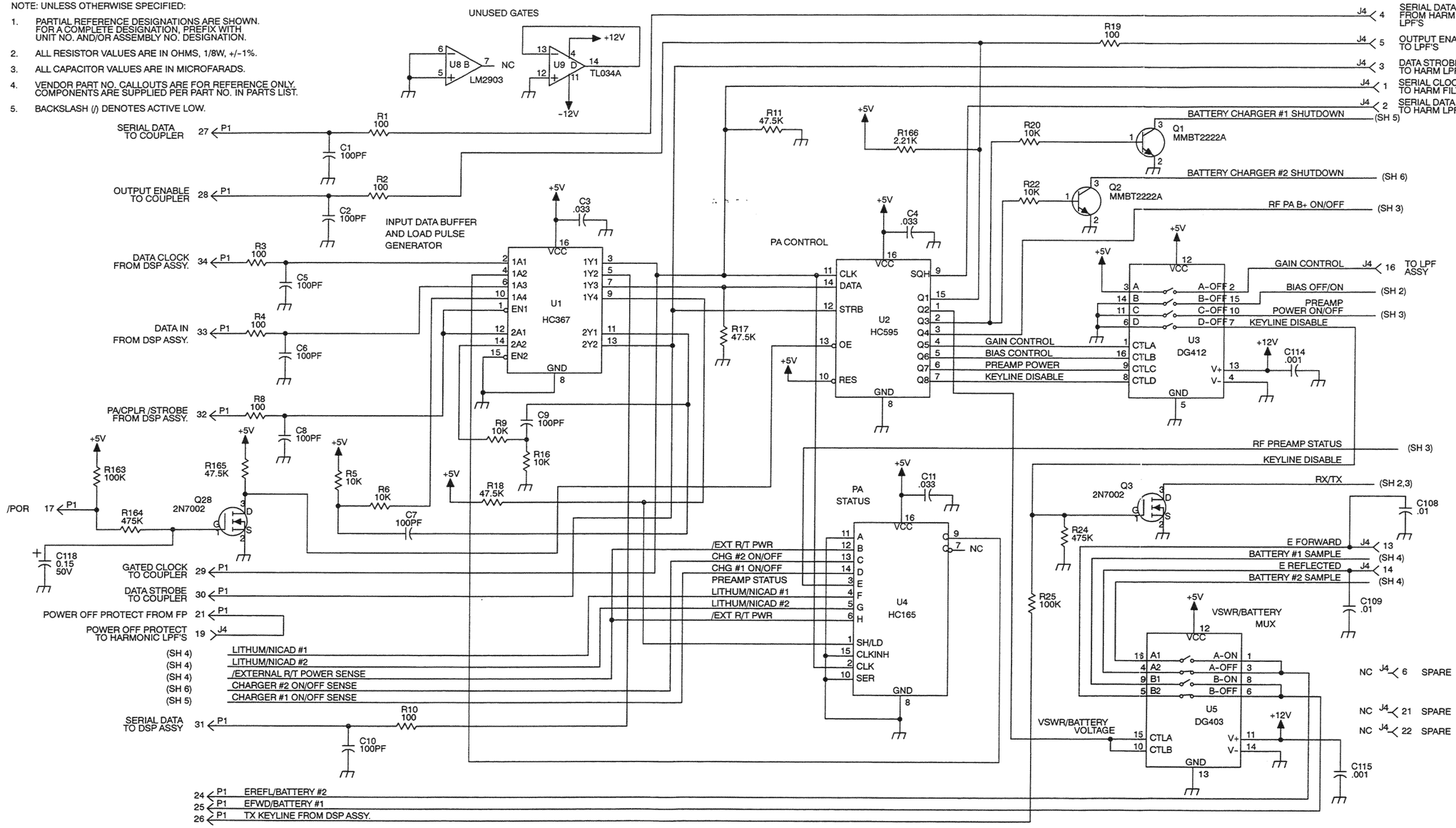


Figure 8. A8A1 Power Amplifier/Battery Charger PWB Assembly Schematic Diagram (10303-2131 Rev. L) (Sheet 1 of 6)

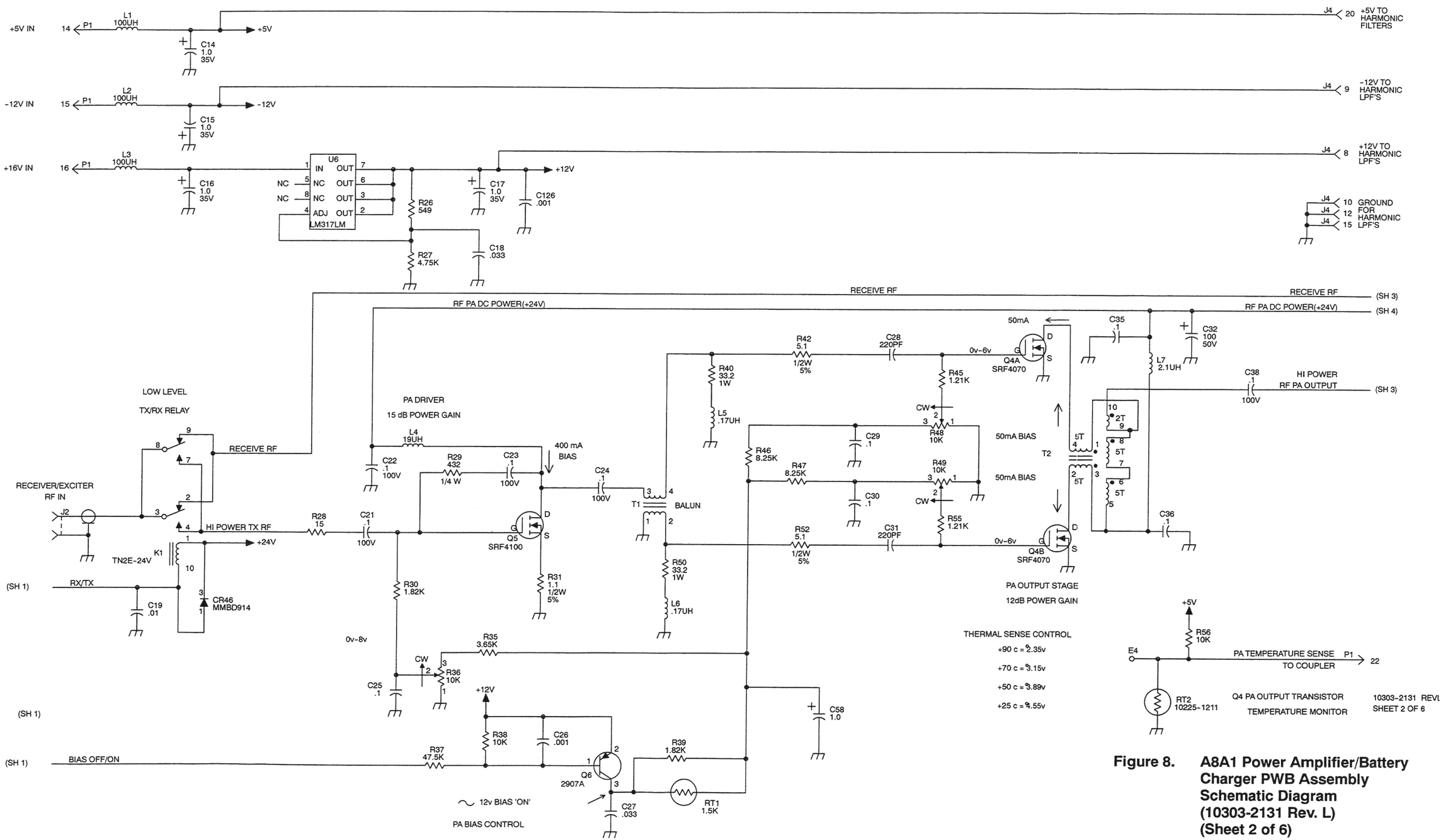


Figure 8. A8A1 Power Amplifier/Battery Charger PWB Assembly Schematic Diagram (10303-2131 Rev. L) (Sheet 2 of 6)

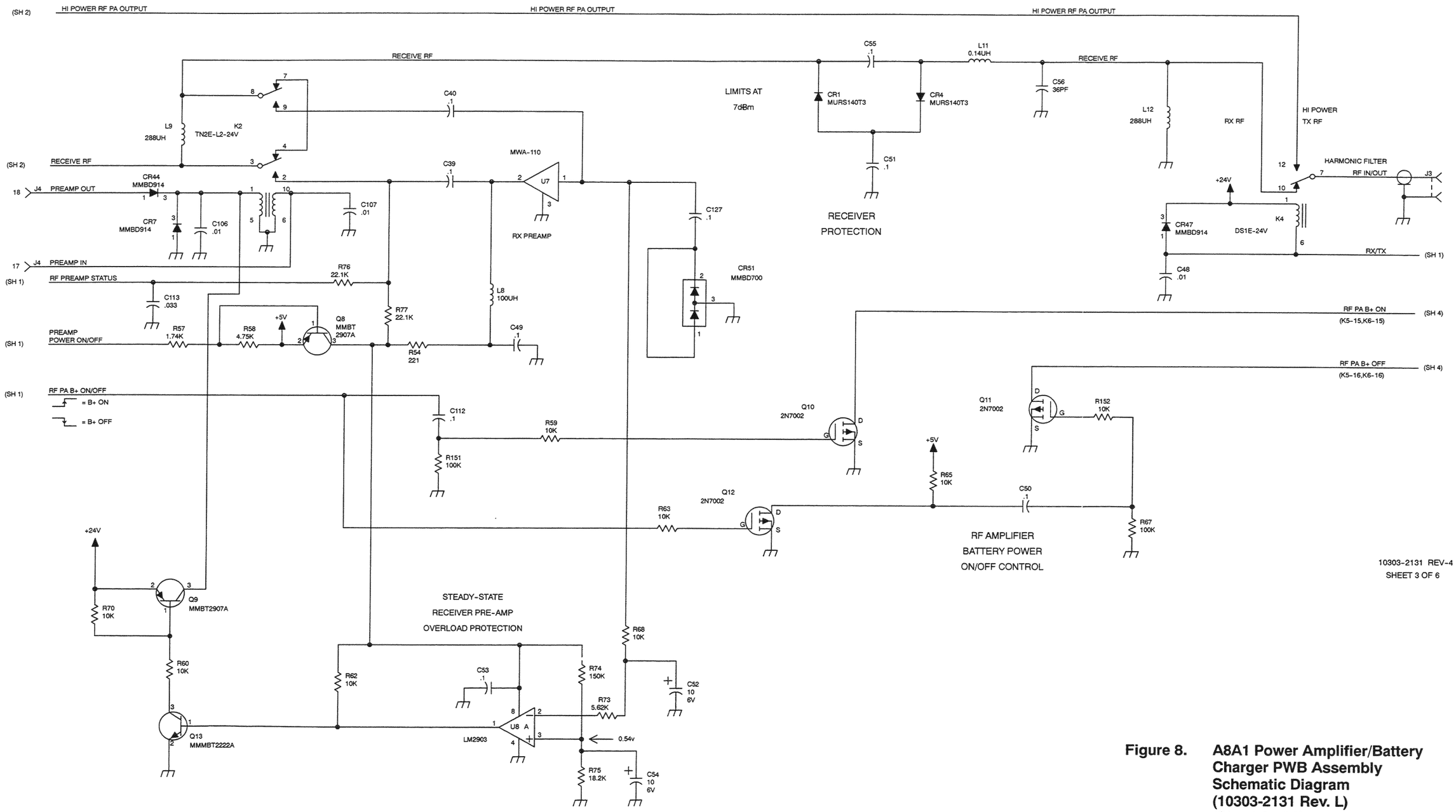


Figure 8. A8A1 Power Amplifier/Battery Charger PWB Assembly Schematic Diagram (10303-2131 Rev. L) (Sheet 3 of 6)

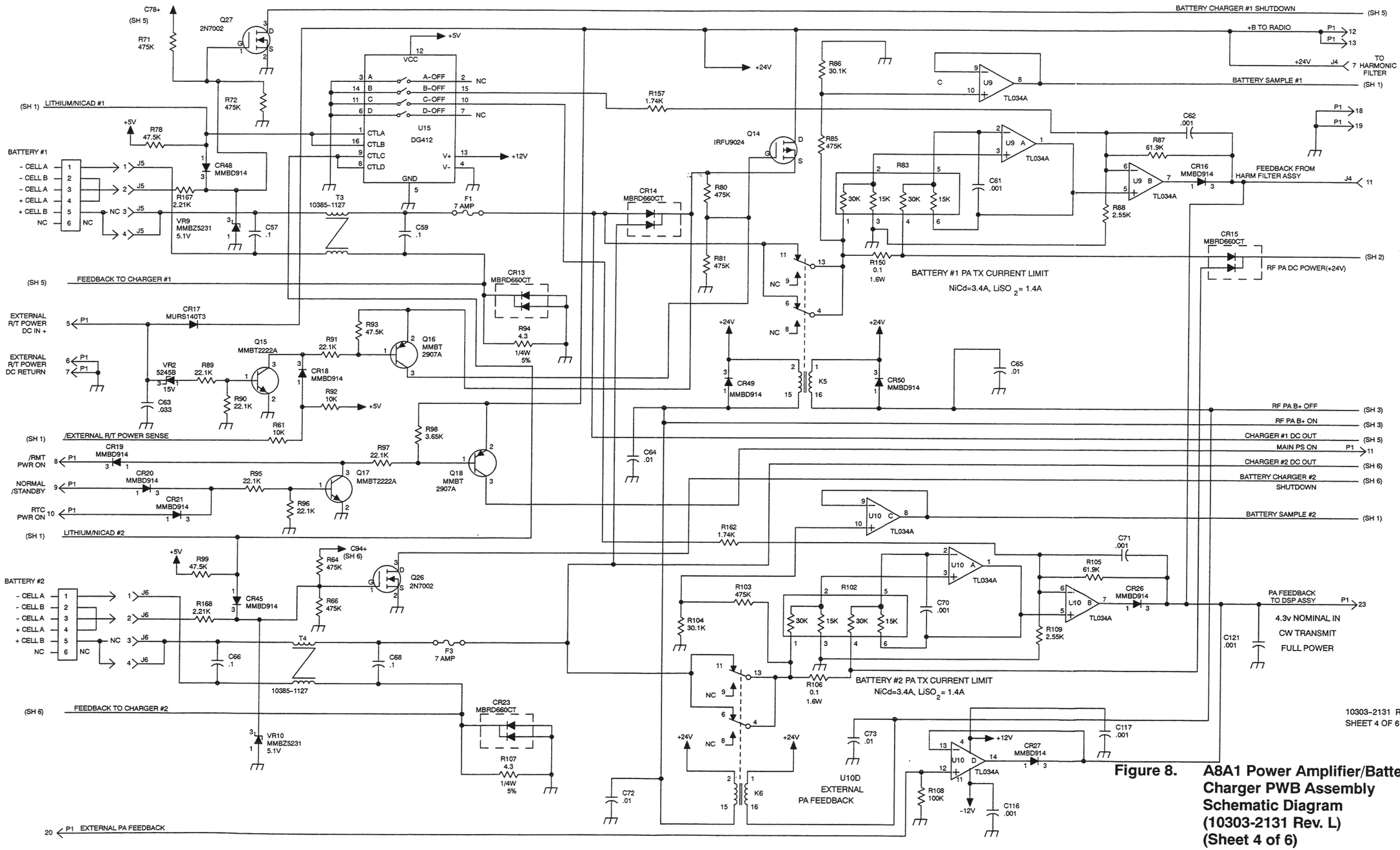


Figure 8. A8A1 Power Amplifier/Battery Charger PWB Assembly Schematic Diagram (10303-2131 Rev. L) (Sheet 4 of 6)

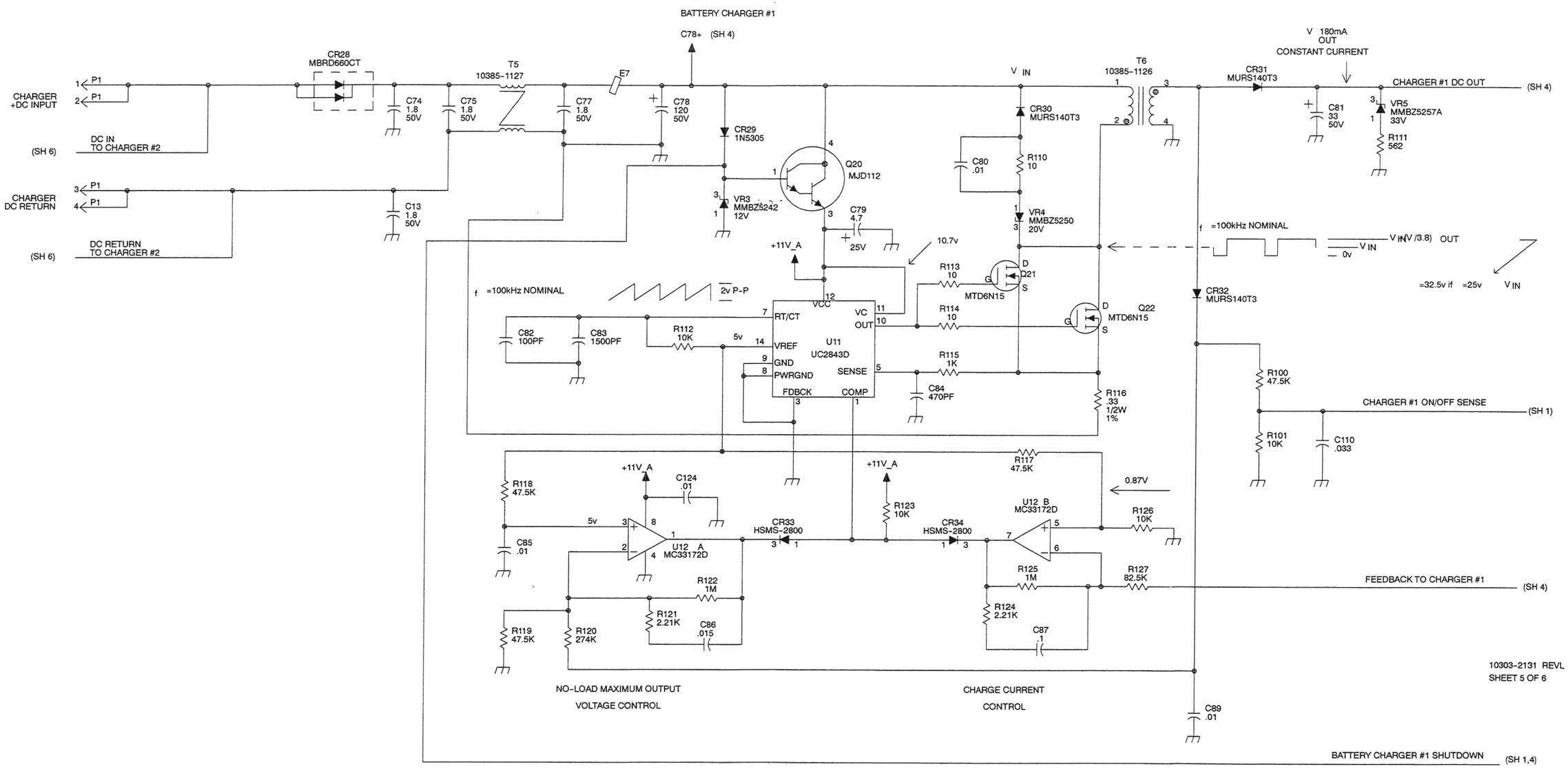


Figure 8. A8A1 Power Amplifier/Battery Charger PWB Assembly Schematic Diagram (10303-2131 Rev. L) (Sheet 5 of 6)

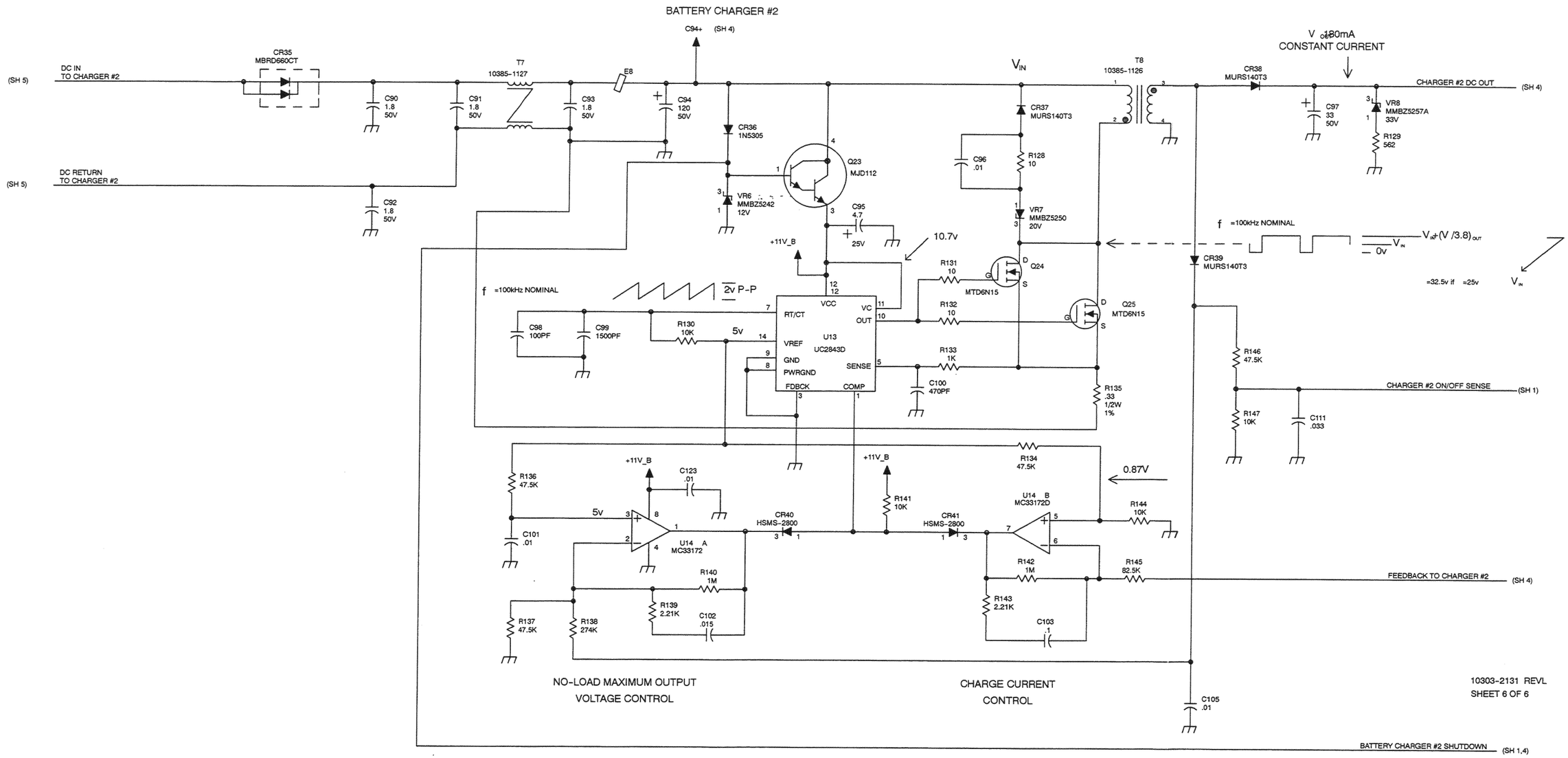


Figure 8. A8A1 Power Amplifier/Battery Charger PWB Assembly Schematic Diagram (10303-2131 Rev. L) (Sheet 6 of 6)

Table 6. A8A2 Harmonic Filter PWB Assembly Parts List (10303-2140 Rev. J)

Ref. Desig.	Part Number	Description
—	R85-0004-001	RES, 10 1% 1/8W CHIP
A1	10303-2310	BAND 1/HPF FILTER CKT.ASS
A2	10303-2320-02	BAND 2 TANK CKT. ASSY
A3	10303-2320-03	BAND 3 TANK CKT. ASSY
A4	10303-2320-04	BAND 4 TANK CKT. ASSY
A5	10303-2320-05	BAND 5 TANK CKT. ASSY
A6	10303-2320-06	BAND 6 TANK CKT. ASSY
A7	10303-2320-07	BAND 7 TANK CKT. ASSY
C2	C13-0103-333	CAP .033UF 10% 100V SMD
C3	C13-0103-103	CAP .01UF 10% 100V SMD
C4	C13-0103-103	CAP .01UF 10% 100V SMD
C5	C13-0103-103	CAP .01UF 10% 100V SMD
C6	C13-0103-103	CAP .01UF 10% 100V SMD
C7	C13-0103-103	CAP .01UF 10% 100V SMD
C8	C13-0103-103	CAP .01UF 10% 100V SMD
C9	C13-0103-103	CAP .01UF 10% 100V SMD
C10	C13-0103-103	CAP .01UF 10% 100V SMD
C11	C13-0103-103	CAP .01UF 10% 100V SMD
C12	C13-0103-103	CAP .01UF 10% 100V SMD
C13	C13-0103-333	CAP .033UF 10% 100V SMD
C14	C13-0103-333	CAP .033UF 10% 100V SMD
C15	C13-0103-103	CAP .01UF 10% 100V SMD
C16	C13-0103-103	CAP .01UF 10% 100V SMD
C17	C13-0103-103	CAP .01UF 10% 100V SMD
C18	C13-0103-103	CAP .01UF 10% 100V SMD
C19	C13-0103-103	CAP .01UF 10% 100V SMD
C20	C13-0103-103	CAP .01UF 10% 100V SMD
C21	C13-0103-103	CAP .01UF 10% 100V SMD
C22	C13-0103-103	CAP .01UF 10% 100V SMD
C24	C13-0103-103	CAP .01UF 10% 100V SMD
C37	C13-0103-103	CAP .01UF 10% 100V SMD
C39	C13-0103-103	CAP .01UF 10% 100V SMD
C40	C13-0103-103	CAP .01UF 10% 100V SMD
C41	C11-0063-621	CAP, 620PF 2% 150V
C42	C13-0103-103	CAP .01UF 10% 100V SMD
C43	C11-0063-201	CAP, 200PF 2% 150V
C45	C11-0063-621	CAP, 620PF 2% 150V
C46	C11-0063-201	CAP, 200PF 2% 150V
C48	C11-0063-621	CAP, 620PF 2% 150V

Table 6. A8A2 Harmonic Filter PWB Assembly Parts List (10303-2140 Rev. J) (Cont.)

Ref. Desig.	Part Number	Description
C49	C11-0063-621	CAP, 620PF 2% 150V
C51	C13-0103-103	CAP .01UF 10% 100V SMD
C52	C11-0063-561	CAP, 560PF 2% 150V
C53	C13-0103-103	CAP .01UF 10% 100V SMD
C54	C13-0103-103	CAP .01UF 10% 100V SMD
C55	C13-0103-103	CAP .01UF 10% 100V SMD
C56	C11-0063-471	CAP, 470PF 2% 150V
C58	C11-0063-331	CAP, 330PF 2% 150V
C60	C11-0063-561	CAP, 560PF 2% 150V
C62	C13-0103-103	CAP .01UF 10% 100V SMD
C63	C11-0063-331	CAP, 330PF 2% 150V
C64	C13-0103-103	CAP .01UF 10% 100V SMD
C65	C13-0103-103	CAP .01UF 10% 100V SMD
C66	C13-0103-103	CAP .01UF 10% 100V SMD
C67	C11-0063-221	CAP, 220PF 2% 150V
C69	C11-0063-561	CAP, 560PF 2% 150V
C71	C11-0063-561	CAP, 560PF 2% 150V
C73	C13-0103-103	CAP .01UF 10% 100V SMD
C74	C11-0063-301	CAP, 300PF 2% 150V
C75	C13-0103-103	CAP .01UF 10% 100V SMD
C76	C13-0103-103	CAP .01UF 10% 100V SMD
C77	C13-0103-103	CAP .01UF 10% 100V SMD
C78	C11-0063-111	CAP, 110PF 2% 150V
C80	C11-0063-331	CAP, 330PF 2% 150V
C82	C11-0063-331	CAP, 330PF 2% 150V
C84	C13-0103-103	CAP .01UF 10% 100V SMD
C85	C11-0063-161	CAP, 160PF 2% 150V
C86	C13-0103-103	CAP .01UF 10% 100V SMD
C87	C13-0103-103	CAP .01UF 10% 100V SMD
C88	C13-0103-103	CAP .01UF 10% 100V SMD
C89	C11-0063-820	CAP, 82PF 2% 150V
C91	C11-0063-221	CAP, 220PF 2% 150V
C93	C11-0063-201	CAP, 200PF 2% 150V
C95	C13-0103-103	CAP .01UF 10% 100V SMD
C96	C11-0063-820	CAP, 82PF 2% 150V
C97	C13-0103-103	CAP .01UF 10% 100V SMD
C98	C13-0103-103	CAP .01UF 10% 100V SMD
C99	C13-0103-103	CAP .01UF 10% 100V SMD
C100	C11-0063-820	CAP, 82PF 2% 150V

Table 6. A8A2 Harmonic Filter PWB Assembly Parts List (10303-2140 Rev. J) (Cont.)

Ref. Desig.	Part Number	Description
C102	C11-0063-151	CAP, 150PF 2% 150V
C104	C11-0063-131	CAP, 130PF 2% 150V
C106	C13-0103-103	CAP .01UF 10% 100V SMD
C107	C11-0063-560	CAP, 56PF 2% 150V
C108	C13-0103-103	CAP .01UF 10% 100V SMD
C109	C13-0103-103	CAP .01UF 10% 100V SMD
C110	C13-0103-103	CAP .01UF 10% 100V SMD
C111	C11-0063-300	CAP, 30PF 2% 150V
C112	C11-0063-150	CAP, 15PF 2% 150V
C113	C11-0063-560	CAP, 56PF 2% 150V
C114	C11-0063-560	CAP, 56PF 2% 150V
C115	C11-0063-150	CAP, 15PF 2% 150V
C116	C11-0063-240	CAP, 24PF 2% 150V
C117	C13-0103-103	CAP .01UF 10% 100V SMD
C118	C11-0063-120	CAP, 12PF 2% 150V
C119	C13-0103-103	CAP .01UF 10% 100V SMD
C120	C11-0063-561	CAP, 560PF 2% 150V
C121	C11-0063-221	CAP, 220PF 2% 150V
C125	C11-0063-240	CAP, 24PF 2% 150V
C131	C13-0107-104	CAP, .1UF 10% 100V CER
C132	C13-0107-104	CAP, .1UF 10% 100V CER
C133	C13-0105-101	CAP, NPO, 100PF 5%
C134	C13-0103-333	CAP .033UF 10% 100V SMD
C135	C13-0103-333	CAP .033UF 10% 100V SMD
C136	C13-0103-102	CAP 1000PF 10% 100V SMD
C137	C13-0107-104	CAP, .1UF 10% 100V CER
C138	C13-0105-101	CAP, NPO, 100PF 5%
C139	C13-0103-471	CAP 470PF 10% 100V SMD
C140	C13-0103-471	CAP 470PF 10% 100V SMD
C142	C13-0103-102	CAP 1000PF 10% 100V SMD
C143	C13-0103-103	CAP .01UF 10% 100V SMD
C144	C11-0063-561	CAP, 560PF 2% 150V
C145	C13-0103-103	CAP .01UF 10% 100V SMD
C146	C13-0103-103	CAP .01UF 10% 100V SMD
C147	C13-0103-103	CAP .01UF 10% 100V SMD
C148	C13-0103-103	CAP .01UF 10% 100V SMD
CR3	D20-0005-001	DIODE, SOT-23
CR4	D15-0914-101	DIODE HI-SPD SWITCHING
CR5	D20-0005-001	DIODE, SOT-23

Table 6. A8A2 Harmonic Filter PWB Assembly Parts List (10303-2140 Rev. J) (Cont.)

Ref. Desig.	Part Number	Description
CR6	D20-0005-001	DIODE, SOT-23
CR7	D15-0914-101	DIODE HI-SPD SWITCHING
CR8	D15-0914-101	DIODE HI-SPD SWITCHING
CR9	D15-0914-101	DIODE HI-SPD SWITCHING
CR10	D15-0914-101	DIODE HI-SPD SWITCHING
CR11	D15-0914-101	DIODE HI-SPD SWITCHING
J2	J92-0023-001	CONN COAX 50 OHM PWB
J3	J92-0020-001	RECEPTACLE, RF
K1	K28-0008-724	RELAY, SPDT LATCH 24V
K2	K28-0008-724	RELAY, SPDT LATCH 24V
K3	K28-0008-724	RELAY, SPDT LATCH 24V
K4	K28-0008-724	RELAY, SPDT LATCH 24V
K5	K28-0008-724	RELAY, SPDT LATCH 24V
K6	K28-0008-724	RELAY, SPDT LATCH 24V
K7	K28-0008-724	RELAY, SPDT LATCH 24V
K8	K28-0008-724	RELAY, SPDT LATCH 24V
K9	K28-0008-724	RELAY, SPDT LATCH 24V
K10	K28-0008-724	RELAY, SPDT LATCH 24V
K11	K28-0008-724	RELAY, SPDT LATCH 24V
K12	K28-0008-724	RELAY, SPDT LATCH 24V
K13	K28-0008-724	RELAY, SPDT LATCH 24V
K14	K28-0008-724	RELAY, SPDT LATCH 24V
K15	K28-0008-724	RELAY, SPDT LATCH 24V
K16	K28-0008-724	RELAY, SPDT LATCH 24V
K17	K28-0008-724	RELAY, SPDT LATCH 24V
L22	10303-3154-01	TOROID 11T #24 ON T30-0
L23	10303-3155-01	TOROID 7T #24 ON T30-0
L24	10303-3156-01	TOROID, 7T #24 ON T25-17
P1	J46-0084-322	HDR 2ROW .400/.120 22 PIN
Q1	2N7002	TRANSISTOR, FET (SOT-23)
Q2	2N7002	TRANSISTOR, FET (SOT-23)
Q3	Q02-2907-101	XSTR SS/GP PNP MMBT2907A
R21	R70-0010-500	RES,50 10% 2.5W NON-INDV.
R22	R85-0004-069	RES 51.1 1% 1/8W
R23	R85-0004-466	RES 475K 1% 1/8W CHIP
R24	R85-0004-201	RES 1000 1% 1/8W FLM
R25	R85-0004-101	RES 100 1% 1/8W FLM
R26	R85-0004-334	RES 22.1K 1% 1/8W FLM
R27	R85-0004-069	RES 51.1 1% 1/8W

Table 6. A8A2 Harmonic Filter PWB Assembly Parts List (10303-2140 Rev. J) (Cont.)

Ref. Desig.	Part Number	Description
R28	R85-0004-466	RES 475K 1% 1/8W CHIP
R29	R85-0004-201	RES 1000 1% 1/8W FLM
R30	R85-0004-260	RES FILM 4120 1% 1/8W SMD
R31	R85-0004-467	RES 487K 1% 1/8W SMT
R32	R85-0004-341	RES 26.1K 1% 1/8W SMT
R33	R85-0004-363	RES,44.2K 1% 1/8W CHIP
R34	R85-0004-363	RES,44.2K 1% 1/8W CHIP
R35	R85-0004-101	RES 100 1% 1/8W FLM
R36	R85-0004-101	RES 100 1% 1/8W FLM
R37	R85-0004-466	RES 475K 1% 1/8W CHIP
R38	R85-0004-301	RES 10K 1% 1/8W FLM
R39	R85-0004-366	RES 47.5K 1% 1/8W FLM
R40	R85-0004-301	RES 10K 1% 1/8W FLM
R41	R85-0004-301	RES 10K 1% 1/8W FLM
T1	10225-2218	ASSY,DIRECT CPLR XFMR
T2	10225-2218	ASSY,DIRECT CPLR XFMR
U1	I08-0016-001	DRIVER (UCN5810EP)
U2	I08-0016-001	DRIVER (UCN5810EP)
U3	I30-0048-005	IC, LP QUAD OP AMP (MC331

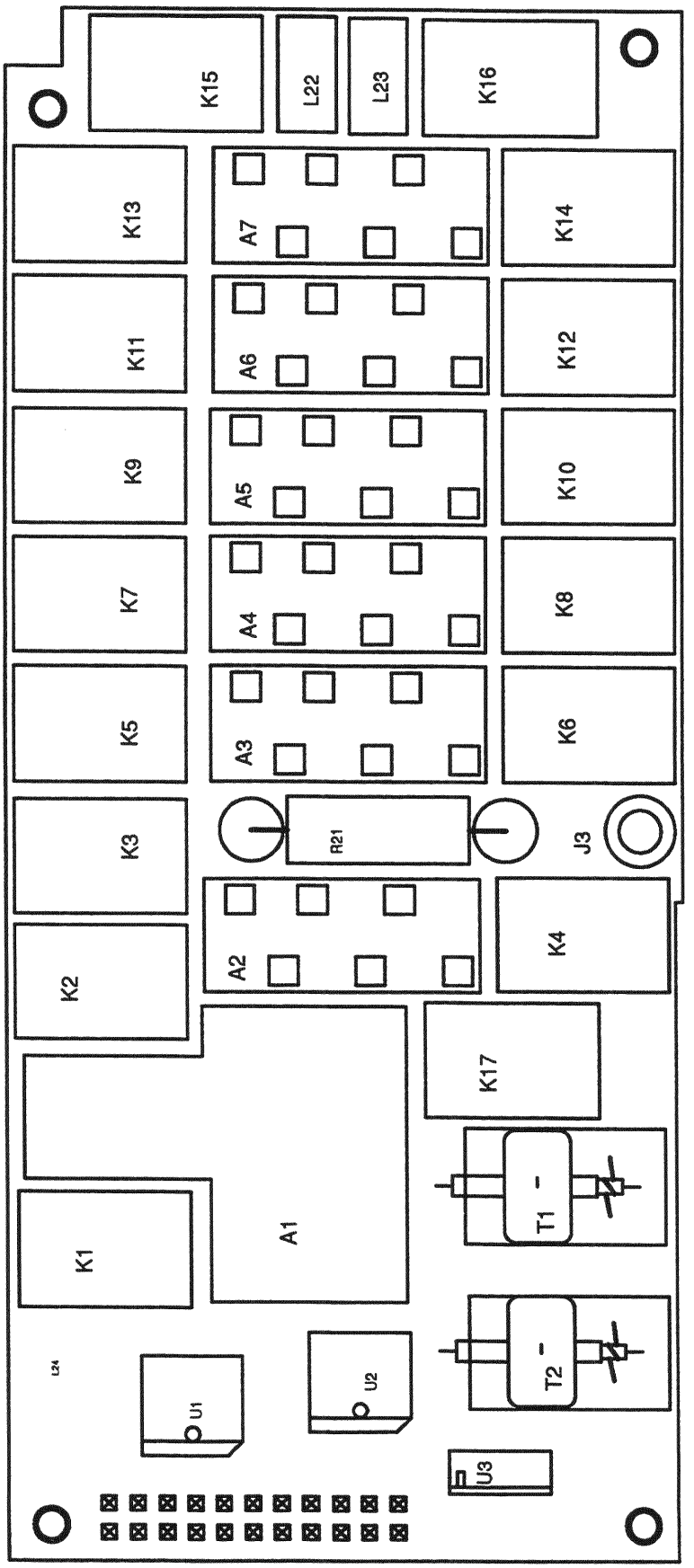


Figure 9. A8A2 Harmonic Filter PWB Assembly Component Location Diagram (10303-2140 Rev. C) (Sheet 1 of 2)

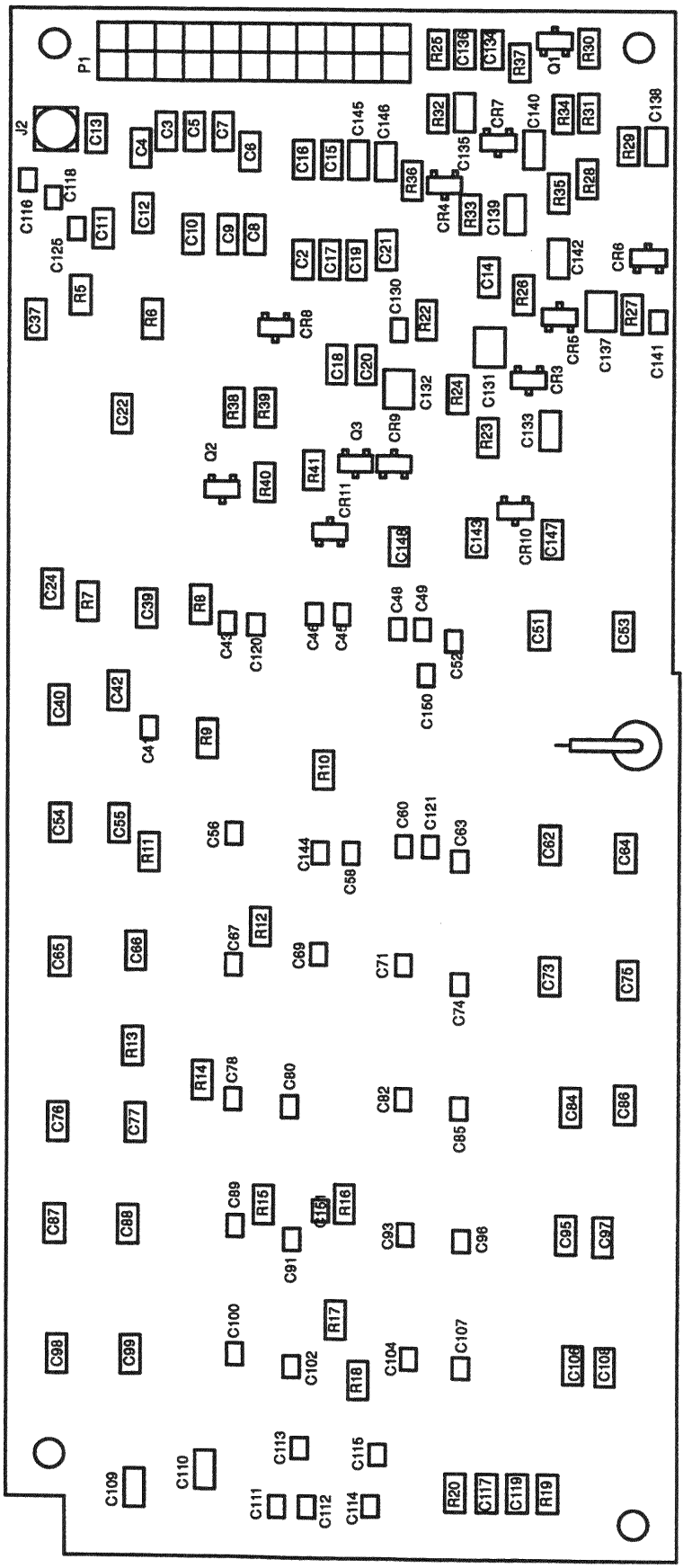
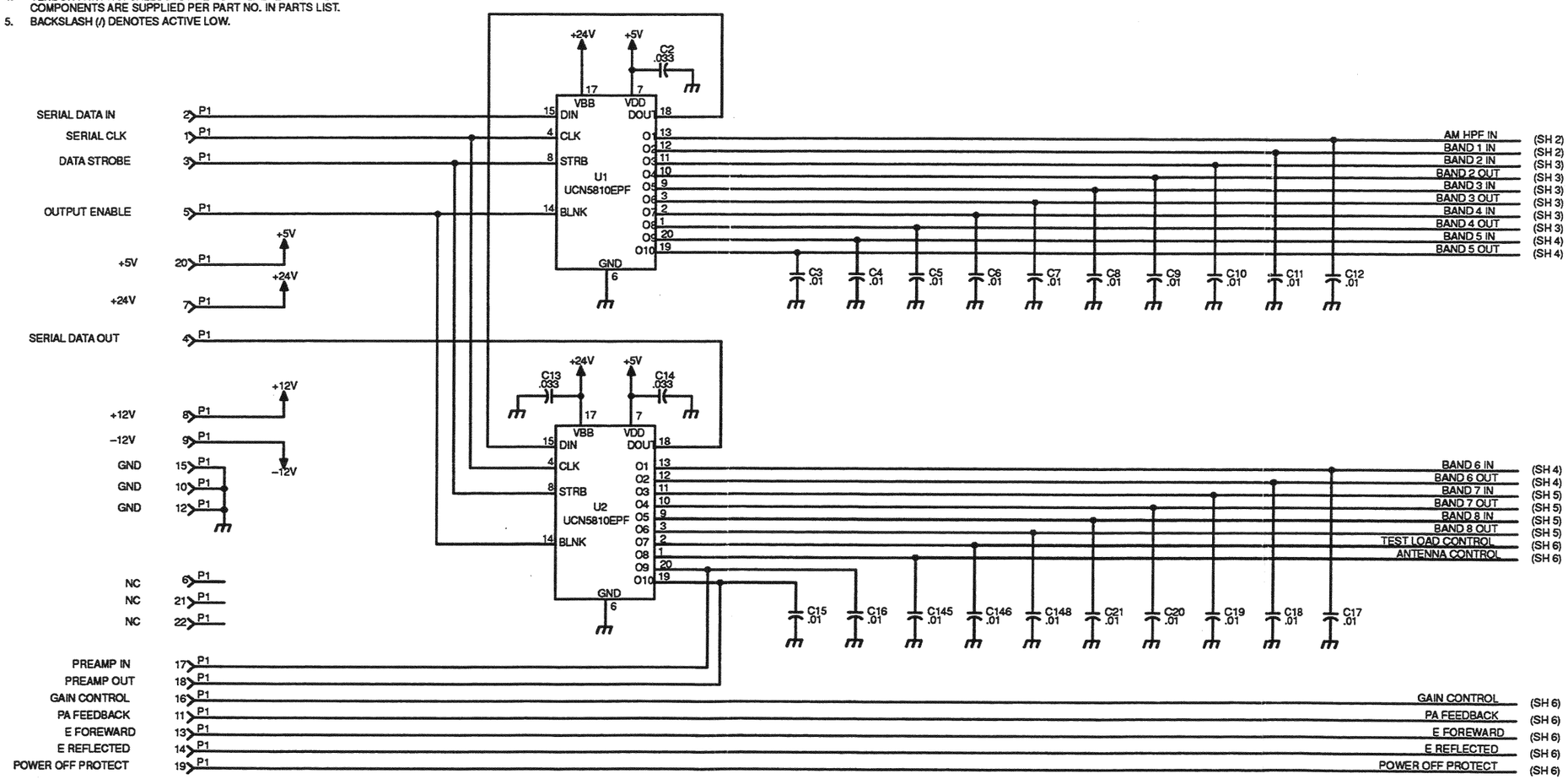


Figure 9. A8A2 Harmonic Filter PWB Assembly Component Location Diagram (10303-2140 Rev. C) (Sheet 2 of 2)

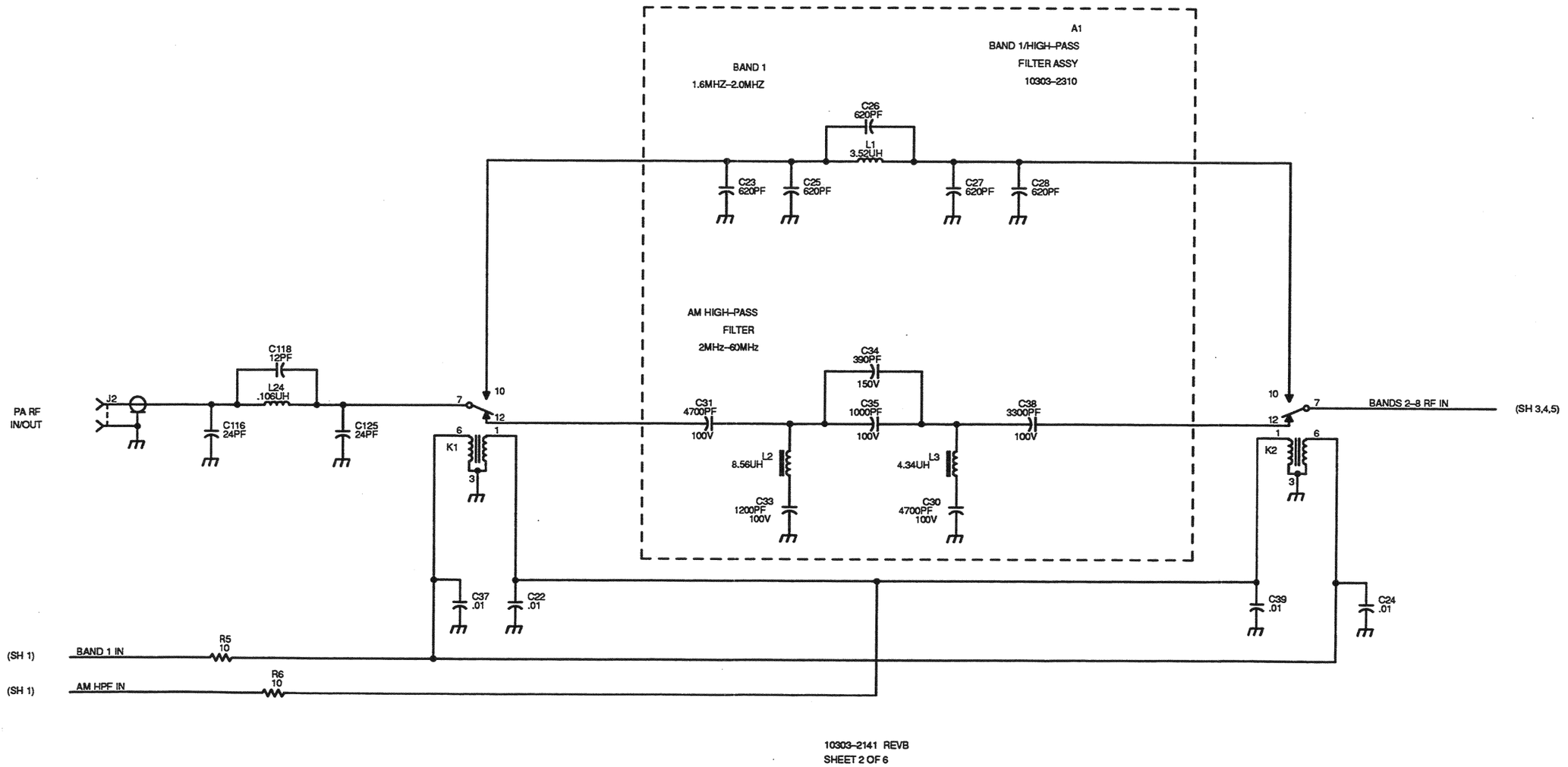
NOTE: UNLESS OTHERWISE SPECIFIED:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR A COMPLETE DESIGNATION, PREFIX WITH UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.
2. ALL RESISTOR VALUES ARE IN OHMS, 1/8W, +/–1%.
3. ALL CAPACITOR VALUES ARE IN MICROFARADS.
4. VENDOR PART NO. CALLOUTS ARE FOR REFERENCE ONLY. COMPONENTS ARE SUPPLIED PER PART NO. IN PARTS LIST.
5. BACKSLASH (/) DENOTES ACTIVE LOW.



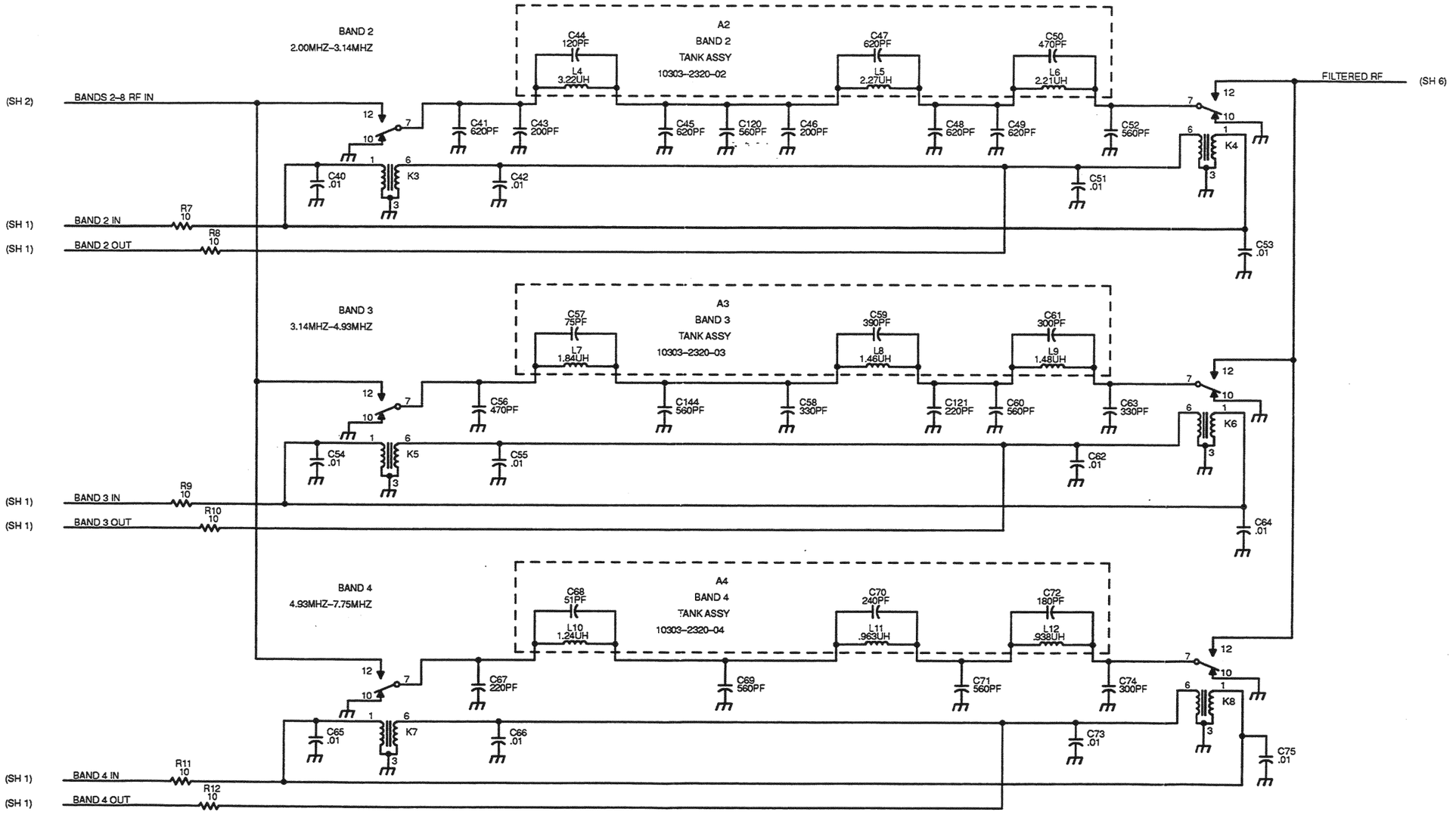
10303–2141 REVB
SHEET 1 OF 6

Figure 10. A8A2 Harmonic Filter PWB Assembly Schematic Diagram (10303-2141 Rev. B) (Sheet 1 of 6)



10303-2141 REVB
SHEET 2 OF 6

Figure 10. A8A2 Harmonic Filter PWB Assembly Schematic Diagram (10303-2141 Rev. B) (Sheet 2 of 6)



10303–2141 REVB
SHEET 3 OF 6

Figure 10. A8A2 Harmonic Filter PWB Assembly Schematic Diagram (10303-2141 Rev. B) (Sheet 3 of 6)

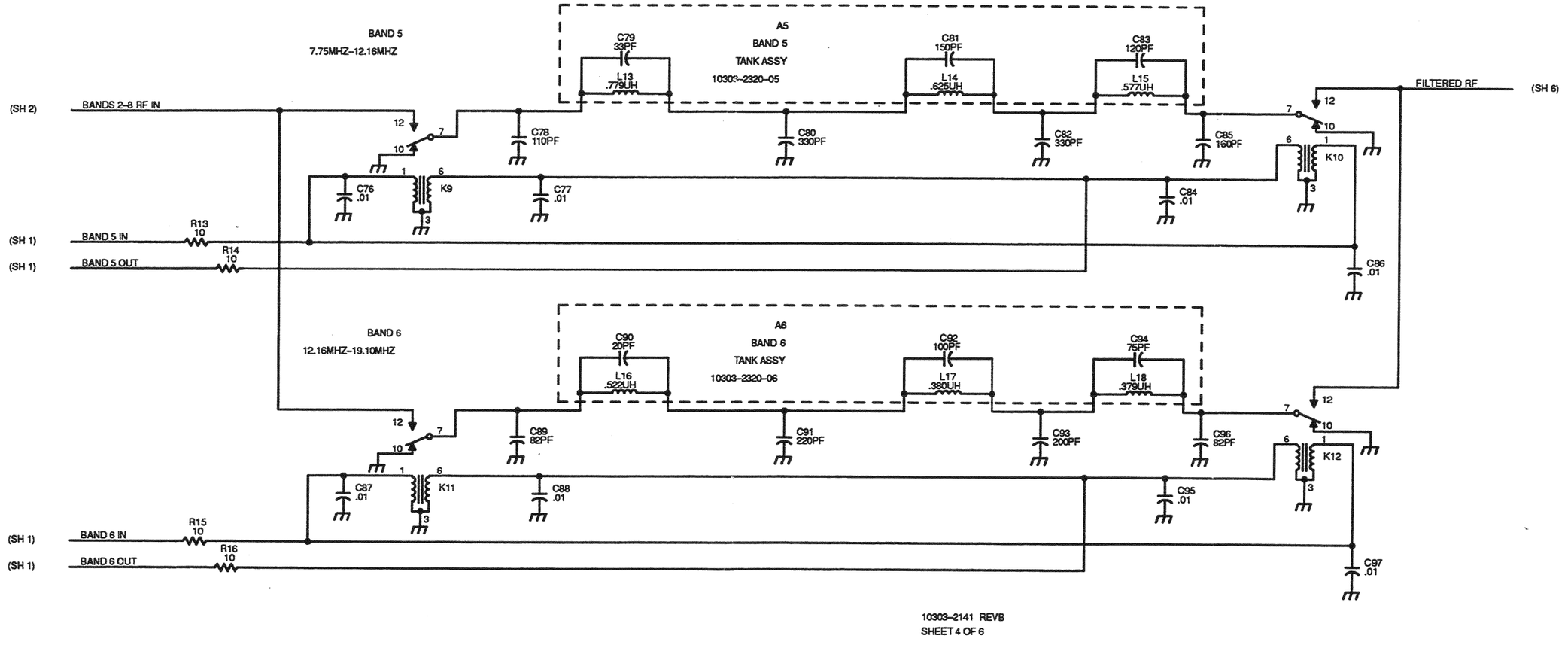


Figure 10. A8A2 Harmonic Filter PWB Assembly Schematic Diagram (10303-2141 Rev. B) (Sheet 4 of 6)

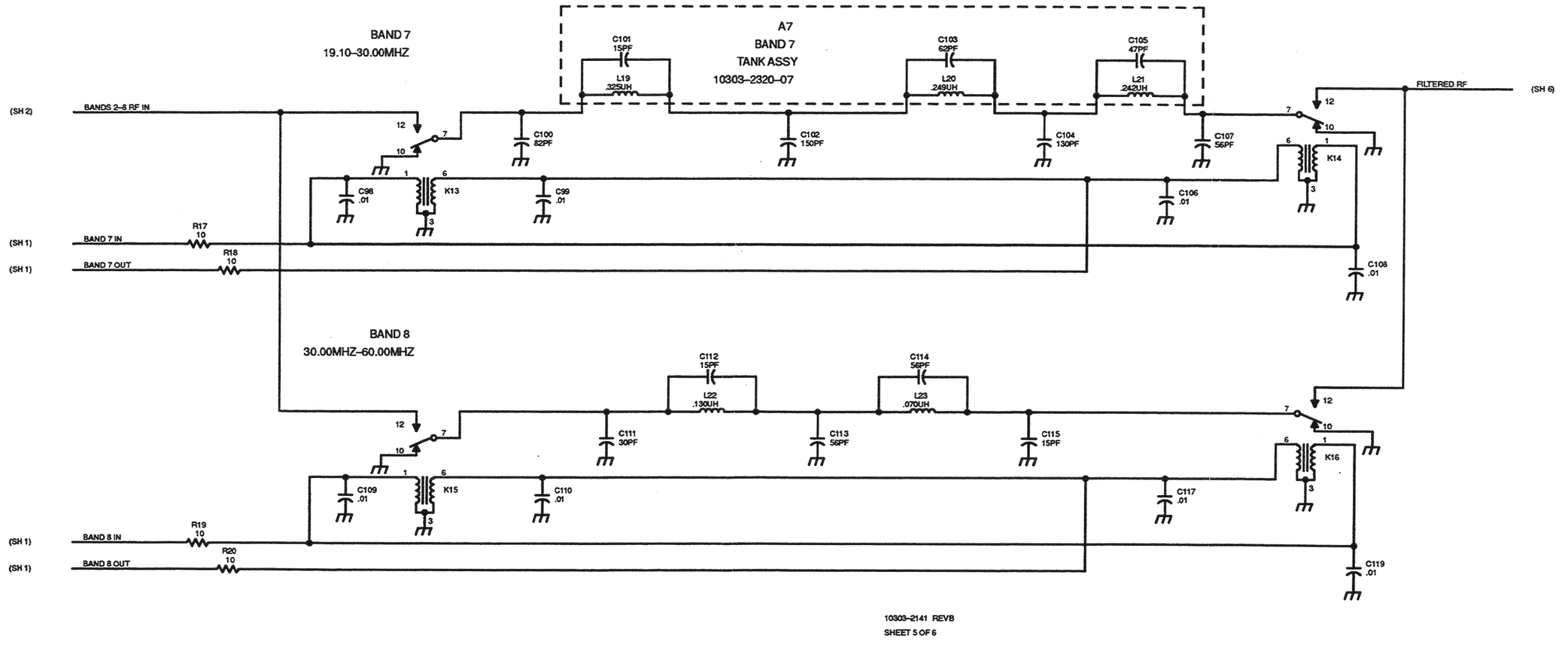
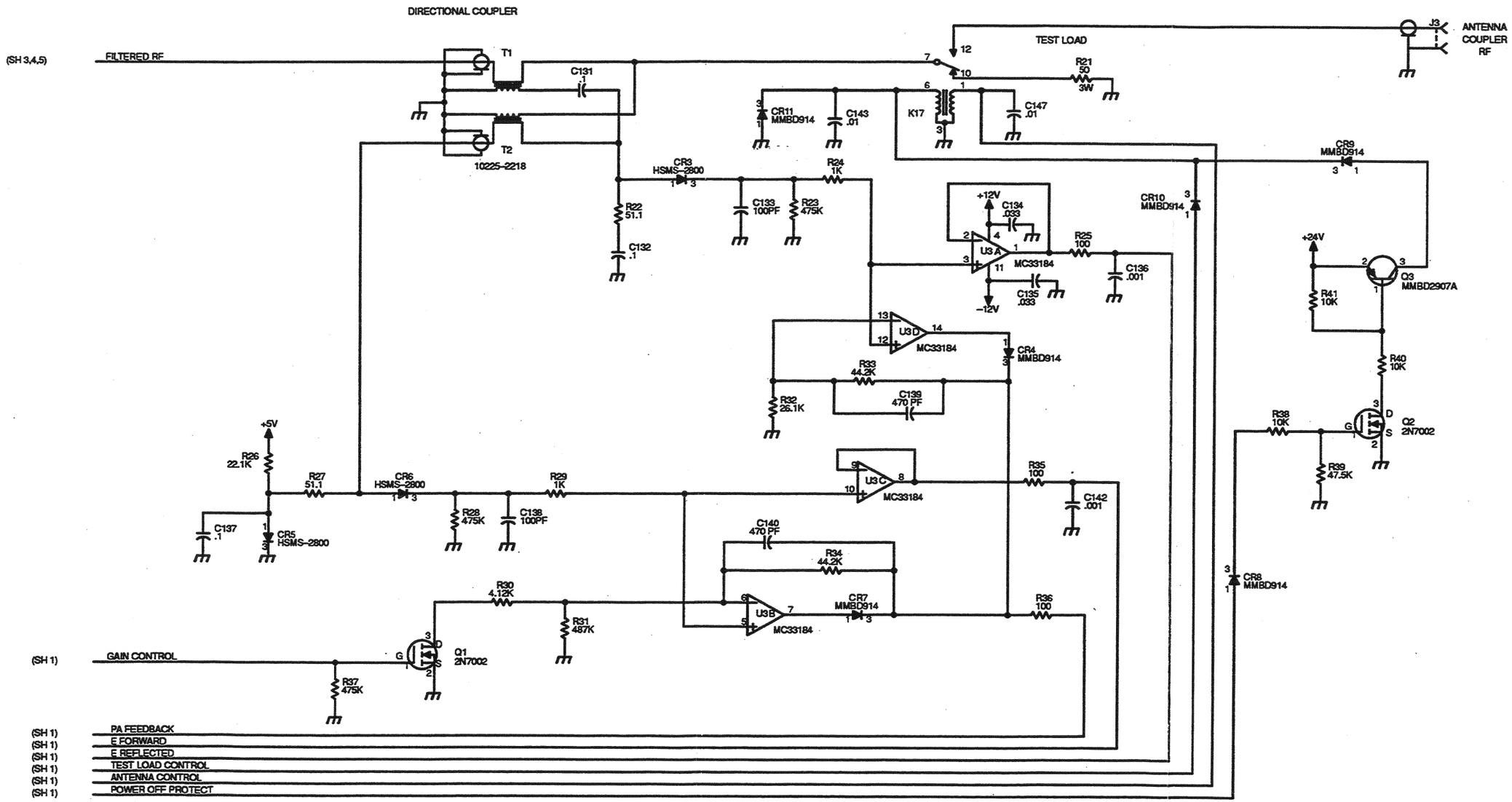


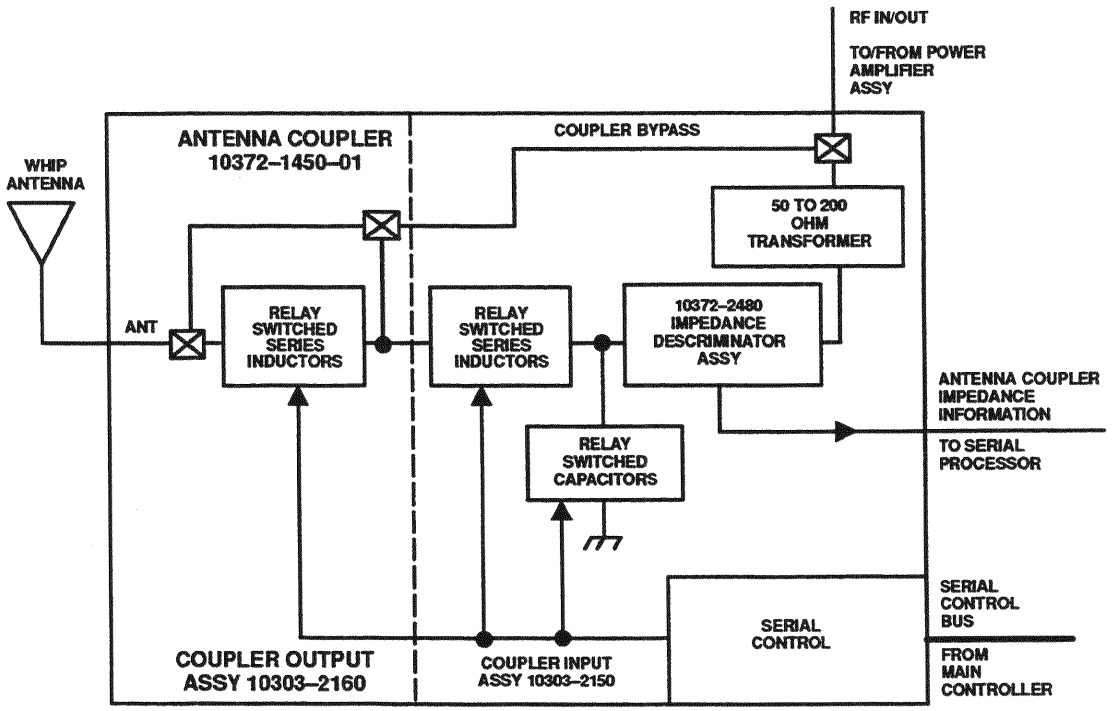
Figure 10. A8A2 Harmonic Filter PWB Assembly Schematic Diagram (10303-2141 Rev. B) (Sheet 5 of 6)



10303-2141 REV8
SHEET 6 OF 6

Figure 10. A8A2 Harmonic Filter PWB Assembly Schematic Diagram (10303-2141 Rev. B) (Sheet 6 of 6)

A9
ANTENNA COUPLER



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A9 ANTENNA COUPLER

1. GENERAL DESCRIPTION

The antenna impedance and tuning conditions change constantly in the RT-1694 Manpack. To provide for every possibility, the RT-1694 checks the VSWR of the stored memory tune before each radio transmission. If the VSWR is greater than 2:1, then the radio attempts to improve the VSWR by retuning before the transmission. If the observed VSWR is less than 2:1, then the transmission is initiated without a retune. After a radio zeroize, the tune table is initialized to a coupler bypass setting.

The RT-1694 is equipped with an internal A9 Antenna Coupler Assembly. Coupler tuning is controlled by radio software contained in the A4 Signal Processor Assembly. The Antenna Coupler Assembly is an L-C matching network placed between the power amplifier output and the antenna. The goal of the coupler is to tune the attached antenna load so it appears as a 50-ohm, purely-resistive load to the power amplifier. This maximizes power transmitted through the antenna and minimizes power reflected back to the power amplifier.

The A9 Antenna Coupler Assembly (10372-1450-01) is composed of the following PWB assemblies:

- A9A1 Coupler #1 PWB Assembly (10303-2150)
- A9A1A1 Discriminator PWB Assembly (10303-2480)
- A9A2 Coupler #2 PWB Assembly (10303-2160)

2. INTERFACE CONNECTIONS

The signals sent to and received by the A9 Antenna Coupler Assembly are listed in table 1.

Table 1. Antenna Coupler Interface Connector Assignments

Connector and Pin	Signal	Comments
P1-1	+16 Vdc	+16 Vdc input from power supply
P1-2	-12 Vdc	-12 Vdc input from power supply
P1-3	+24 Vdc	+24 Vdc input from PA
P1-4	+5 Vdc	+5 Vdc input from power supply
P1-5	Ground	System ground
P1-6	Ground	System ground
P1-7	Eforw/Battery 1	Multiplexed analog sense input from PA, 0 to 3 V
P1-8	Erefl/Battery 2	Multiplexed analog sense input from PA, 0 to 3 V
P1-9	PA Temp	Analog sense input from PA, 0 to 3 V
P1-10	MUX Control 1	Multiplexer control input from DSP assembly, 5 V CMOS logic
P1-11	MUX Control 2	Multiplexer control input from DSP assembly, 5 V CMOS logic
P1-12	CU Feedback A	Multiplexed PA/CU status analog output to DSP assembly, 0 to 3 V
P1-13	CU Feedback B	Multiplexed PA/CU status analog output to DSP assembly, 0 to 3 V

Table 1. Antenna Coupler Interface Connector Assignments (Cont.)

Connector and Pin	Signal	Comments
P1-14	Serial Data	Gated serial data input from PA, 5 V CMOS logic
P1-15	Serial Clock	Gated serial clock input from PA, 5 V CMOS logic (data clocked on rising edge)
P1-15	Serial Clock	Gated serial clock input from PA, 5 V CMOS logic (data clocked on rising edge)
P1-16	PA/CU Strobe	Strobe input from PA, 5 V CMOS logic (relays latched on rising edge)
P1-17	Output Enable	Relay enable input from PA, 5 V CMOS logic (active low)
P1-18	Not used	
P1-19	Not used	
P1-20	Not used	
J1-1	K10-B	Reset K10, L10 in, 24 V pulse
J1-2	K26-A	Set K26, HF bypass on, 24 V pulse
J1-3	K10-A	Set K10, L10 out, 24 V pulse
J1-4	K26-B	Reset K26, HF bypass off, 24 V pulse
J1-5	K9-B	Reset K9, L9 in, 24 V pulse
J1-6	K7-B	Reset K7, L7 in, 24 V pulse
J1-7	K9-A	Set K9, L9 out, 24 V pulse
J1-8	K7-A	Set K7, L7 out, 24 V pulse
J1-9	K8-A	Set K8, L8 out, 24 V pulse
J1-10	K8-B	Reset K8, L8 in, 24 V pulse
J1-11	K13-B	Reset K13, C6/C7 out, 24 V pulse
J1-12	K14-A	Set K14, C66/C67 in, 24 V pulse
J1-13	K13-A	Set K13, C6/C7 in, 24 V pulse
J1-14	K12-B	Reset K12, L18/L19 in, 24 V pulse
J1-15	K12-A	Set K12, L18/L19 out, 24 V pulse
J1-16	K14-B	Reset K14, C66/C67 out, 24 V pulse
J1-17	K11-B	Reset K11, L17 out, 24 V pulse
J1-18	K15-A	Set K15, bypass off, 24 V pulse
J1-19	K11-A	Set K11, L17 in, 24 V pulse
J1-20	K15-B	Reset K15, bypass on, 24 V pulse
J1-21	High Voltage Sense	1 Vdc = 140 Vp at E14
J1-22	Ground	System ground

Table 1. Antenna Coupler Interface Connector Assignments (Cont.)

Connector and Pin	Signal	Comments
J2	RF In from PA	Receive RF to PA assembly; transmit RF from PA (25 watts maximum)
P2/J3	Bypass RF	RF bypass between coupler input and output assemblies
E14	RF Out	High voltage connection to front panel antenna connector
E15	RF	High voltage connection between coupler input and output assemblies

3. TECHNICAL DESCRIPTION

3.1 General Theory – Coupler Tuning Hardware

The major functional blocks of the A9A1 Antenna Coupler #1 Assembly are shown in its block diagram, figure 1. The functional blocks consist of the following:

- T1, a 50 ohm:200 ohm transformer
- A9A1A1 Discriminator Assembly
- The matching network, which includes inductors L1 – L10 and L17 – L19, and capacitors C8 – C19
- Load modifiers C6/C7 and C66/C67
- PA/Coupler status multiplexer U3
- Relay drivers U1, U2, and U6.

Tuning the antenna to the 50 ohm impedance of the transceiver is accomplished by the matching network. This network includes 9 relay-selected steps of input shunt capacitance (3.3 pF to 1300 pF; Cmax = 2600 pF), 12 relay-selected steps of series inductance (.05 to 90 uH; Lmax = 180 uH), and a 50 ohm to 200 ohm broadband matching transformer. Load modifiers C6/C7 and C66/C67 are used to increase the tuning potential of the matching network. The load modifiers are selected as required for certain frequencies and antennas.

Selection of the matching network components is controlled by the A4 Signal Processor Assembly in response to inputs from the A9A1A1 Discriminator Assembly. The Signal Processor reads the discriminator outputs via the PA/Coupler status multiplexer; other signals from the A8 Power Amplifier Assembly are read via the multiplexer. A successive approximation method is used to determine the correct matching network components. The A4 Signal Processor sets the appropriate relays by sending serial data to relay drivers U1, U2, and U6. When 52 bits of data have been clocked to the drivers, the strobe line, which is normally low, pulses high to latch the data, and then the output enable line, which is normally high, pulses low to set the relays. The coupler uses dual-coil latching relays.

Relays K25, K26, and K15 provide two different bypassing capabilities within the coupler. K26 and K15 permit bypassing around the seven largest inductive elements; this mode is selected as required, particularly when tuning high frequencies. All three relays are used to provide a 50-ohm bypass around the tuning elements.

High voltage protection is provided by capacitive divider C62/C63/C64 and detector diode CR5; this signal is monitored by the signal processor via the status multiplexer.

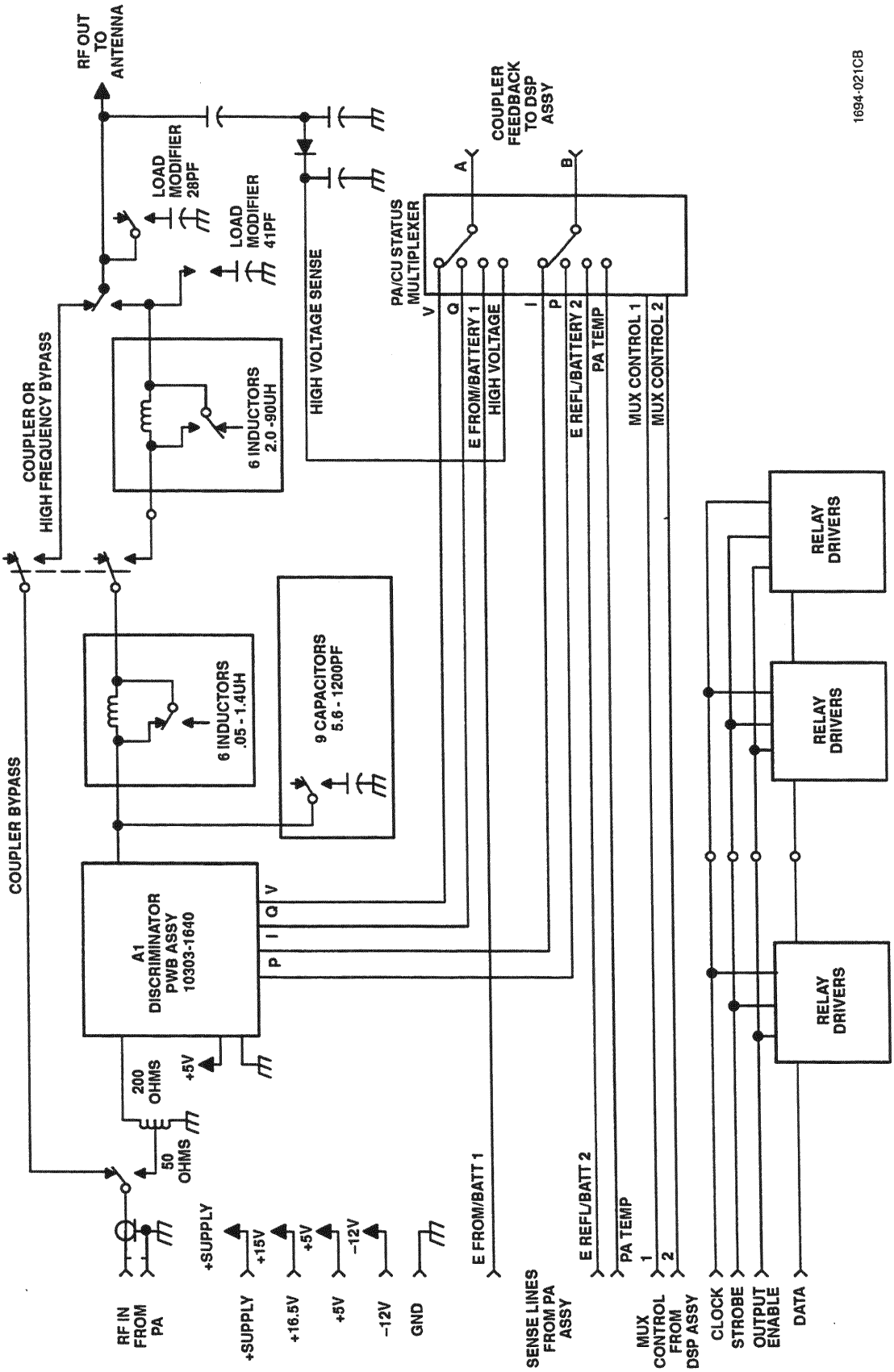


Figure 1. A9A1 Antenna Coupler #1 Block Diagram

3.2 General Theory – Coupler Tuning Software

The coupler tuning process has four primary inputs. These are the V, I, P, and Q voltages which are read from the discriminator hardware. These voltages provide a measure of the magnitude and phase of the antenna load, as seen by the power amplifier.

Based on the discriminator readings, the software will attempt to tune the load by switching combinations of L and C elements into the matching network via mechanical relays.

3.2.1 Series L Elements

In the RT-1694 the total amount of series L available in the matching network is 179.91 uH. This total L is divided into 4095 increments of 0.044 uH, each which may be switched in or out in a binary fashion under software control. These increments will be referred to as steps of L.

3.2.2 Parallel C Elements

The total amount of parallel C available in the matching network is 2602.6 pF. This total C is divided into 511 increments of 5.093 pF, each which may be switched in or out in a binary fashion under software control. These increments will be referred to as steps of C.

3.2.3 Load Modifiers

In the event that the load cannot be tuned using the available L and C coupler elements, the coupler software also has the ability to switch in shunt C elements called load modifiers. There are two load modifiers available (22 pF and 41 pF). Either or both of these may be switched in at any time, thus resulting in three binary increments of load modifier C.

3.2.4 Switching Elements

Individual coupler elements (Ls, Cs, and load modifiers) are switched in by setting the appropriate data bits in the PA/Coupler serial data stream. The data stream is clocked out to the mechanical relays on the A9 Antenna Coupler Assembly and then strobed in to set the state of the relays. Two bits are used for each element. A total of 52 bits are used.

3.3 Tune Algorithm

Refer to figures 2 and 3 for the following description.

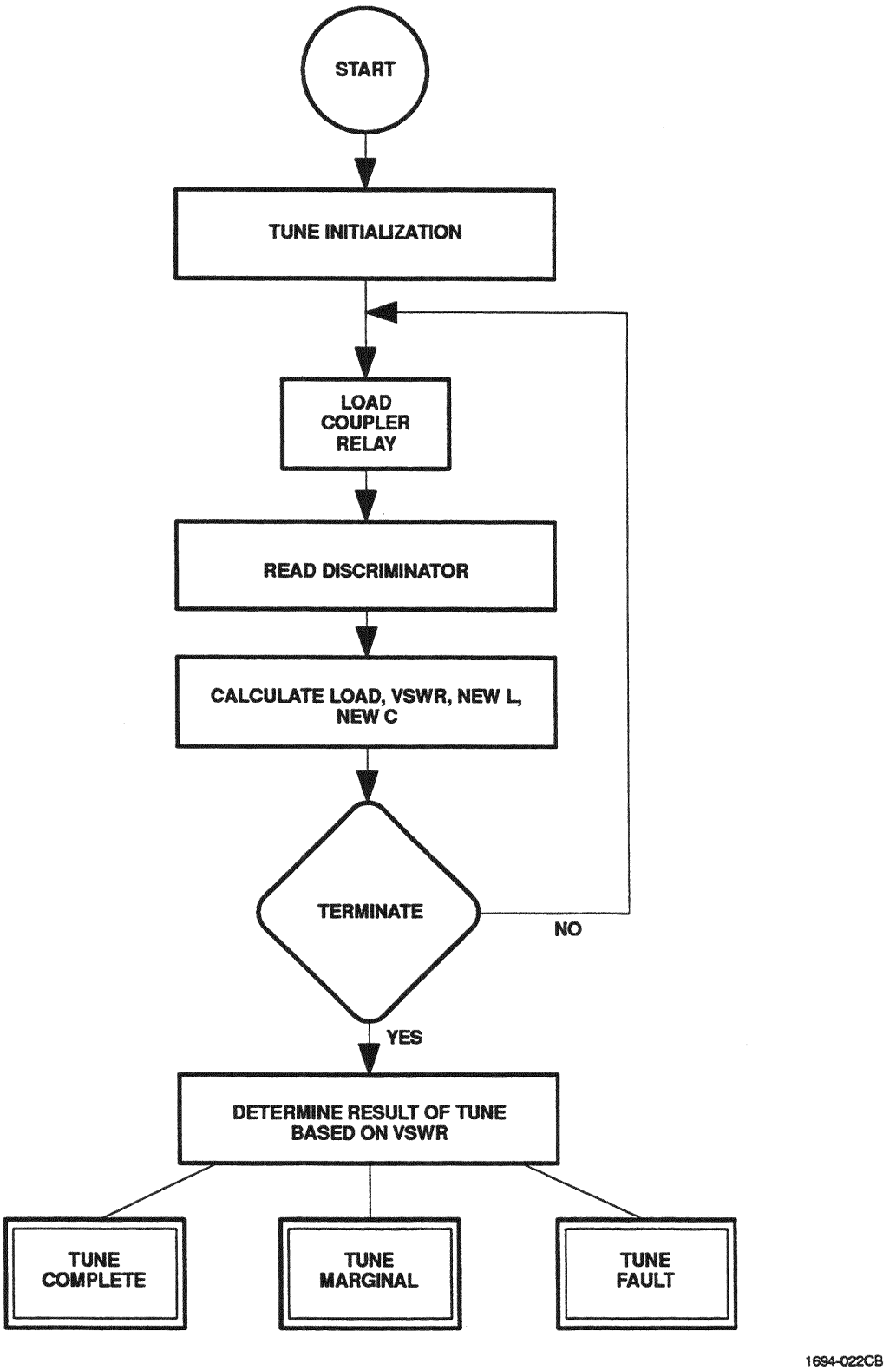


Figure 2. Tune Algorithm Flow Chart

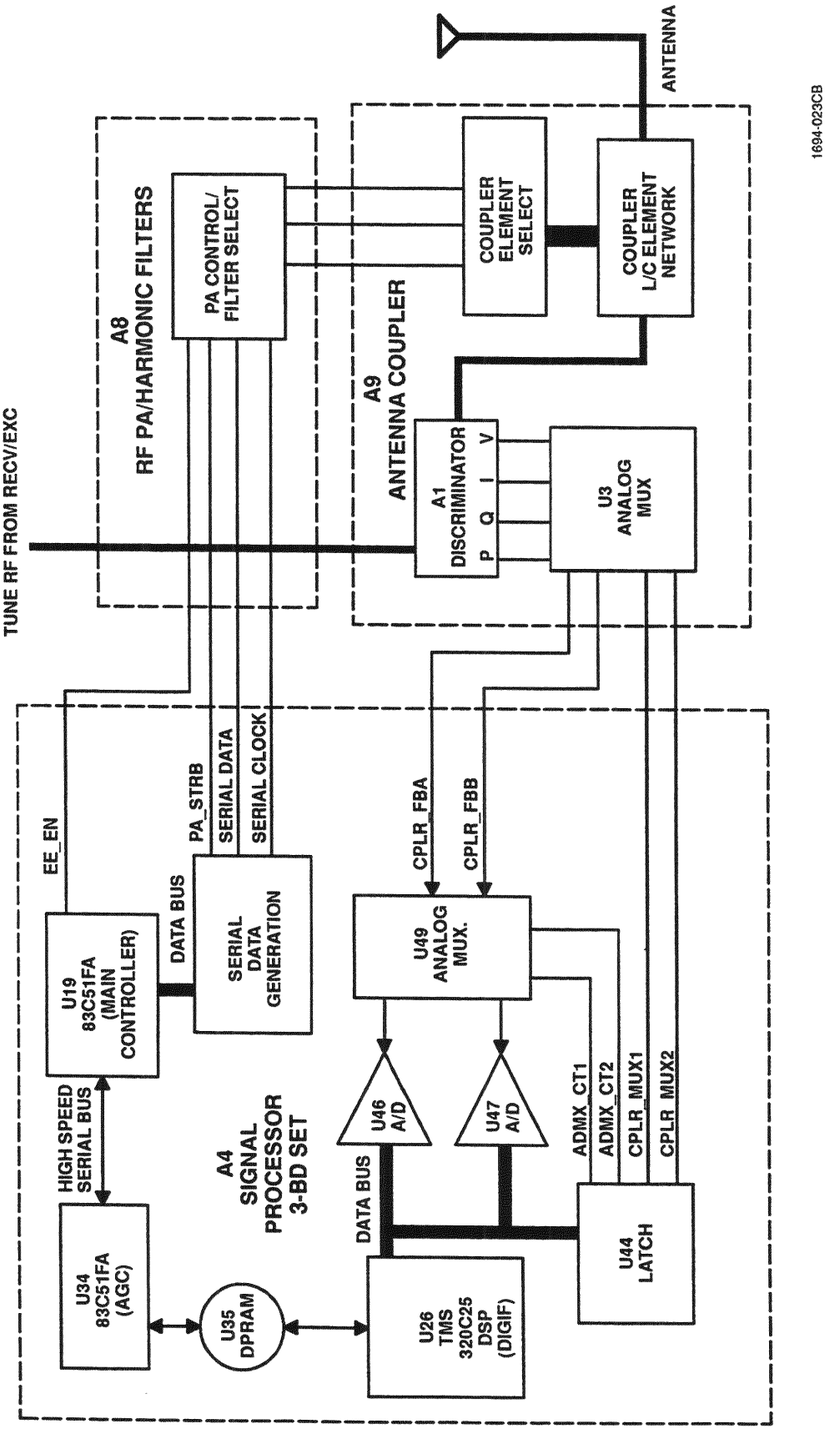


Figure 3. Tuning Hardware System Block Diagram

3.3.1 Overview

The coupler tuning algorithm is an iterative procedure driven by feedback from the discriminator hardware outputs (V, I, P, and Q). Based on the V, I, P, and Q readings, the software calculates the load impedance seen by the discriminator. From this impedance the software then calculates what series L and parallel C are needed to match the load to 50 +j0 ohms. The calculated L and C are then switched in and a new discriminator reading is taken. This procedure repeats until an acceptable tune is achieved or the algorithm fails. Each iteration of this procedure is referred to as a tune step.

The Antenna Coupler tuning software is primarily split between two processors on the A4 Signal Processor Assembly. They are the Main Controller 8051 processor and the Digital IF TMS320 processor.

The Main Controller processor governs the tuning process and controls the switching of the tune elements via a serial data stream. It also keeps track of the following status information:

- Current # L steps in
- Current # C steps in
- Current # modifiers in
- Current tune state
- Tune frequency
- # tune steps (iterations) performed

This status information is sent to the Digital IF processor at the start of each tune step.

In tune mode, the Digital IF processor continually outputs a 100 mw CW signal to the PA/Coupler hardware. It uses two A/D converters to periodically sample readings from the discriminator outputs. These readings, as well as the information fed back from the Main Controller, drive a series of calculations on the Digital IF. The following are outputs of these calculations:

- Current load magnitude
- Current load phase angle
- Current VSWR
- Current tune status
- Desired # L steps for tune
- Desired # C steps for tune

3.3.2 Tune Mode Initialization

The Main Controller performs several steps before coupler tuning takes place on a given frequency. First, it resets all the coupler settings so that all Ls, Cs, and load modifiers are switched out. Then it initializes all status variables to their starting values and sets the tune step counter to 0. Then it commands the Digital IF processor to begin tune mode operation. Now the Main Controller sends the Digital IF processor all initial status information (see subsection 3.3.1). Tuning operation can now begin.

3.3.3 Tune Steps (Iterations)

One tune step performs the following tasks in order:

1. Main Controller loads relays to switch in current # L steps, current # C steps, and current # load modifiers.
2. Main Controller sends current status information to Digital IF processor.
3. Digital IF processor samples discriminator outputs.
4. Digital IF calculates current load impedance and VSWR.
5. Digital IF determines tune status based on above results and calculates new desired values for # L steps, # C steps.
6. Main Controller polls Digital IF for results.
7. Based on Digital IF results, the Main Controller does one or more of the following:
   (a.) Sets new current # L steps and current # C steps
   (b.) Sets new current # load modifiers
   (c.) Changes tune state
   (d.) Terminates tuning (see subsection 3.3.4)
8. If tune has not been terminated, increment step counter and return to step 1.

3.3.4 Tune Termination

Tuning operation can terminate with one of three results:

- TUNE COMPLETE - For tune frequencies below 30.0 MHz, a tune complete occurs when the tune algorithm has successfully achieved a VSWR of 1:5:1 or better. For tune frequencies above 30.0 MHz the VSWR requirement is relaxed slightly based linearly on frequency so a VSWR of 2.0:1 is acceptable at 60.0 MHz. The L, C, and load modifier settings are stored for this frequency.
- TUNE MARGINAL - A marginal tune is declared if the tune algorithm has exhausted all attempts to achieve a TUNE COMPLETE, but a VSWR better than 3.0:1 has been achieved. The L, C, and load modifier settings are stored for this frequency.
- TUNE FAULT - A tune fault is declared if the tune algorithm has exhausted all attempts to achieve a TUNE COMPLETE and the best obtainable VSWR is worse than 3.0:1. The element settings are not saved in this case.

3.3.5 High Frequency Bypass Mode

Due to stray capacitances associated with the coupler hardware (relays, PCB traces, etc.), it may be difficult to tune some loads at higher frequencies. To minimize this problem, the coupler may be switched to HIGH FREQUENCY BYPASS mode. This essentially bypasses the larger L elements which most likely are not used for a high frequency tune. The result is a reduction in stray C and a greater likelihood of achieving a tune. The software will automatically attempt a tune in HIGH FREQUENCY BYPASS mode, when necessary.

4. TESTING AND ALIGNMENT

There are no routine test or alignment procedures for the A9 Antenna Coupler Assembly.

4.1 A9A1A1 Discriminator Assembly Alignment

If the A9A1A1 Discriminator Assembly is damaged or defective, it is recommended that the entire A9A1 Coupler #1 PWB Assembly be replaced. If it is necessary, however, to replace or repair only the A9A1A1 Discriminator Assembly, then the A9A1A1 Discriminator Assembly must be aligned before it is placed onto the A9 Antenna Coupler Assembly.

The following test equipment is required for this alignment:

- Discriminator Alignment Test Fixture, 10303-9120
- Digital Multimeter, Fluke Model 8012 or equivalent (quantity 2)
- RF Signal Generator, HP-8640B or equivalent

NOTE

The signal generator must be capable of delivering a +20 dBm signal with all harmonics < 35 dBc.

4.1.1 Alignment Setup and Preparation

Perform the following:

a. Connect all equipment to bench 115 V, 60 Hz power.

b. Connect the RED lead from voltmeter 1 to the V jack and the BLACK lead to the I jack on the text fixture. This will measure Vz.

c. Connect the RED lead from the voltmeter 2 to the P jack and the BLACK lead to the Q jack of the text fixture. This will measure VΘ.

d. Attach the signal generator to the RF IN connector J1 on the test fixture. Set the generator to 1.875 MHz, +20 dBm. Turn the RF output switch off.

4.1.2 Discriminator Alignment Procedure

Perform the following:

a. Place the A9A1A1 Discriminator Assembly on the test fixture.

b. Adjust R1 until Vz = 0 Volts ±3 mV. Adjust R2 until VΘ = 0 Volts ± 3 mV.

c. Turn on the signal generator. Adjust R4 on the A9A1A1 Discriminator Assembly until Vz = 0 Volts ±3 mV.

d. Change the frequency of the signal generator to 30 MHz and leave the level at +20 dBm. Adjust C24 on the Discriminator Assembly until Vz = 0 Volts ±3 mV.

e. Repeat steps c. and d. until Vz = 0 Volts ±3 mV at both 1.875 MHz and 30 MHz.

f. Check the bandwidth discrimination by setting the signal generator to each of the frequencies shown in table 2 and measuring both Vz and VΘ. Verify that both voltages are within the limits shown in table 2.

g. The alignment is complete and the A9A1A1 Discriminator Assembly may be installed on the A9 Antenna Coupler Assembly.

Table 2. Bandwidth Discrimination Limits

Frequency (MHz)	Vz Limit	VΘ Limit
1.875	0 ± 5 mv	0 ± 50 mV
3.750	0 ± 50 mV	0 ± 50 mV
7.500	0 ± 50 mV	0 ± 50 mV
15.000	0 ± 50 mV	0 ± 50 mV
30.000	0 ± 5 mV	0 ± 50 mV
60.000	0 ± 50 mV	0 ± 50 mV

5. BITE FAULTS AND TROUBLESHOOTING

The A9 Antenna Coupler Assembly has one fault code:

- Fault 01 - Coupler operational fault

5.1 Troubleshooting BITE Faults

5.1.1 Fault 01 – Coupler Operational Fault

This fault occurs when the manpack attempts to transmit 100 mW CW and fails to detect the presence of any modulated RF at the antenna coupler discriminator. To isolate the fault, perform the following steps.

a. Check the PA/Antenna Coupler connection for damaged, disconnected, or missing coaxial cables.

b. Verify that the antenna coupler relays are configured correctly for tune power transmission.

5.2 Troubleshooting Operational Faults

The following describe problems and solutions for operational faults that occur during troubleshooting.

Problem: TUNE COMPLETE cannot be achieved.

Solution(s): Replace A9A1A1 Discriminator Assembly.

Problem: Relays will not actuate.

Solution(s): Check L13 and L14 for an open.

Replace U1, U2, U6.

Problem: RF is present at output (E14) only when coupler is in RF BYPASS mode.

Solution(s): Check T1, L15, A1 for possible defect.

Check K25, K26, K15 for proper operation.

Problem: High voltage signal was not received at A4 Signal Processor.

Solution(s): Check U7A, CR5 for proper operation.

6. PARTS LIST, COMPONENT LOCATION DIAGRAM, AND SCHEMATIC DIAGRAM

Tables 3 through 6 are the parts lists, and figures 4 through 9 are the component location diagrams and schematic diagrams for the Antenna Coupler Assembly.

Table 3. A9 Antenna Coupler Assembly Parts List (10372-1450-01 Rev. B)

Ref. Desig.	Part Number	Description
1	10303-1200-01	STANDOFF, CAPTIVE
2	MS15795-803	FW SS .125X.250X.022
3	MS35338-135	LW SPLT SS #4
4	H33-0002-416	SCREW CPTV 4-40X1
5	H12-0002-103	SCREW BRASS
6	10303-1213-01	STANDOFF
7	H40-0003-002	FW BRASS .119X.28X.025
8	H41-0002-002	LW PLN BVGZ SPLT #4X.025
A1	10303-2150	PWB ASSY, COUPLER INPUT
A2	10303-2160	PWB ASSY, COUPLER OUTPUT

Table 4. A9A1 Coupler Input PWB Assembly Parts List (10303-2150 Rev. F)

Ref. Desig.	Part Number	Description
A1	10303-2480	PWB ASSY,DISCRIMINATOR
C5	C13-0107-103	CAP CER .01UF 20% 100V
C8	C11-0053-033	CAP 3.3PF 5% 500V SMD
C9	C11-0053-100	CAP 10PF 5% 500V SMD
C10	C11-0053-220	CAP 22PF 5% 500V SMD
C11	C11-0053-430	CAP 43PF 5% 500V SMD
C12	C11-0053-820	CAP 82PF 5% 500V SMD
C13	C11-0053-161	CAP 160PF 5% 300V SMD
C14	C11-0053-331	CAP 330PF 5% 200V SMD
C15	C11-0053-331	CAP 330PF 5% 200V SMD
C16	C11-0053-331	CAP 330PF 5% 200V SMD
C17	C11-0053-431	CAP 430PF 5% 200V SMD
C18	C11-0053-431	CAP 430PF 5% 200V SMD
C19	C11-0053-431	CAP 430PF 5% 200V SMD
C30	C13-0103-102	CAP 1000PF 10% 100V SMD
C31	C13-0103-102	CAP 1000PF 10% 100V SMD
C32	C13-0103-102	CAP 1000PF 10% 100V SMD
C33	C13-0103-102	CAP 1000PF 10% 100V SMD
C34	C13-0103-102	CAP 1000PF 10% 100V SMD
C35	C13-0103-102	CAP 1000PF 10% 100V SMD
C36	C13-0103-102	CAP 1000PF 10% 100V SMD
C37	C13-0103-102	CAP 1000PF 10% 100V SMD
C38	C13-0103-102	CAP 1000PF 10% 100V SMD

Table 4. A9A1 Coupler Input PWB Assembly Parts List (10303-2150 Rev. F) (Cont.)

Ref. Desig.	Part Number	Description
C39	C13-0103-102	CAP 1000PF 10% 100V SMD
C40	C13-0103-102	CAP 1000PF 10% 100V SMD
C41	C13-0103-102	CAP 1000PF 10% 100V SMD
C42	C13-0103-102	CAP 1000PF 10% 100V SMD
C43	C13-0107-104	CAP, .1UF 10% 100V CER
C44	C13-0107-104	CAP, .1UF 10% 100V CER
C45	C13-0107-104	CAP, .1UF 10% 100V CER
C46	C13-0107-104	CAP, .1UF 10% 100V CER
C47	C13-0105-101	CAP, NPO, 100PF 5%
C48	C13-0105-101	CAP, NPO, 100PF 5%
C49	C13-0105-101	CAP, NPO, 100PF 5%
C50	C13-0107-104	CAP, .1UF 10% 100V CER
C51	C13-0107-104	CAP, .1UF 10% 100V CER
C52	C13-0103-102	CAP 1000PF 10% 100V SMD
C53	C13-0103-102	CAP 1000PF 10% 100V SMD
C54	C13-0103-102	CAP 1000PF 10% 100V SMD
C55	C13-0103-102	CAP 1000PF 10% 100V SMD
C56	C13-0103-102	CAP 1000PF 10% 100V SMD
C57	C13-0103-102	CAP 1000PF 10% 100V SMD
C58	C13-0103-102	CAP 1000PF 10% 100V SMD
C59	C13-0103-102	CAP 1000PF 10% 100V SMD
C60	C13-0107-104	CAP, .1UF 10% 100V CER
C61	C13-0107-104	CAP, .1UF 10% 100V CER
C68	C13-0105-101	CAP, NPO, 100PF 5%
C70	C13-0103-102	CAP 1000PF 10% 100V SMD
C71	C13-0103-102	CAP 1000PF 10% 100V SMD
C72	C07-0007-102	CAP NTWRK 1000PF 10% 100V
C75	C13-0103-102	CAP 1000PF 10% 100V SMD
C77	C13-0103-102	CAP 1000PF 10% 100V SMD
C79	C13-0103-102	CAP 1000PF 10% 100V SMD
C84	C13-0103-102	CAP 1000PF 10% 100V SMD
C85	C13-0103-102	CAP 1000PF 10% 100V SMD
C106	C13-0107-104	CAP, .1UF 10% 100V CER
C107	C13-0107-104	CAP, .1UF 10% 100V CER
C108	C13-0107-104	CAP, .1UF 10% 100V CER
C109	C13-0107-104	CAP, .1UF 10% 100V CER
J1	J46-0087-122	CONN PC.1 TOP ENTR 22 PIN
J2	J92-0006-000	CONN SMB VERT PNL MT F
K1	K28-0008-724	RELAY, SPDT LATCH 24V

Table 4. A9A1 Coupler Input PWB Assembly Parts List (10303-2150 Rev. F) (Cont.)

Ref. Desig.	Part Number	Description
K2	K28-0008-724	RELAY, SPDT LATCH 24V
K3	K28-0008-724	RELAY, SPDT LATCH 24V
K4	K28-0008-724	RELAY, SPDT LATCH 24V
K5	K28-0008-724	RELAY, SPDT LATCH 24V
K6	K28-0008-724	RELAY, SPDT LATCH 24V
K16	K28-0008-724	RELAY, SPDT LATCH 24V
K17	K28-0008-724	RELAY, SPDT LATCH 24V
K18	K28-0008-724	RELAY, SPDT LATCH 24V
K19	K28-0008-724	RELAY, SPDT LATCH 24V
K20	K28-0008-724	RELAY, SPDT LATCH 24V
K21	K28-0008-724	RELAY, SPDT LATCH 24V
K22	K28-0008-724	RELAY, SPDT LATCH 24V
K23	K28-0008-724	RELAY, SPDT LATCH 24V
K24	K28-0008-724	RELAY, SPDT LATCH 24V
K25	K28-0008-724	RELAY, SPDT LATCH 24V
L1	10303-3138-01	INDUCTOR, .05UH
L2	10303-3141-01	INDUCTOR, .09UH
L3	10303-3142-01	INDUCTOR, .17UH
L4	10303-3143-01	INDUCTOR, .35UH
L5	10303-3144-01	INDUCTOR, .7UH
L6	10303-3145-01	INDUCTOR, 1.4UH
L13	L45-0007-042	INDCTR 33 UH CHIP UN-SH
L14	L45-0007-042	INDCTR 33 UH CHIP UN-SH
L15	10303-3151-01	TOROID ASSY .47UH
P1	J46-0054-020	HEADER 20 PIN
P2	J92-0020-001	RECEPTACLE, RF
R13	R85-0004-166	RES 475 1% 1/8W SMD
R14	R85-0004-166	RES 475 1% 1/8W SMD
R15	R85-0004-166	RES 475 1% 1/8W SMD
R16	R85-0004-166	RES 475 1% 1/8W SMD
R17	R85-0004-101	RES 100 1% 1/8W FLM
R18	R85-0004-101	RES 100 1% 1/8W FLM
R19	R85-0004-101	RES 100 1% 1/8W FLM
R20	R85-0004-101	RES 100 1% 1/8W FLM
R23	R85-0004-401	RES 100K 1% 1/8W FLM
R25	R85-0004-101	RES 100 1% 1/8W FLM
R26	R85-0004-101	RES 100 1% 1/8W FLM
R30	R85-0004-201	RES 1000 1% 1/8W FLM
T1	10303-3139-01	XFMR, 1:4

Table 4. A9A1 Coupler Input PWB Assembly Parts List (10303-2150 Rev. F) (Cont.)

Ref. Desig.	Part Number	Description
U1	I08-0017-001	DRIVER (UCN5818EP)
U2	I08-0016-001	DRIVER (UCN5810EP)
U3	I06-0017-001	DUAL 4 CH MUX (DG409DY)
U4	I30-0048-005	IC, LP QUAD OP AMP (MC331
U6	I08-0016-001	DRIVER (UCN5810EP)
U7	I30-0048-003	IC, LP DUAL OP AMP (MC331
VR1	D05-0005-012	DIODE 8.2V 5% SOT ZENER
VR2	D05-0005-012	DIODE 8.2V 5% SOT ZENER
VR3	D05-0005-012	DIODE 8.2V 5% SOT ZENER
VR4	D05-0005-012	DIODE 8.2V 5% SOT ZENER

Table 5. A9A1A1 Discriminator PWB Assembly Parts List (10303-2480 Rev. H)

Ref. Desig.	Part Number	Description
C1	C11-0062-027	CAP 2.7PF 150V CER SMC
C2	C11-0063-151	CAP, 150PF 2% 150V
C4	C11-0063-151	CAP, 150PF 2% 150V
C20	C13-0103-103	CAP .01UF 10% 100V SMD
C21	C11-0062-027	CAP 2.7PF 150V CER SMC
C22	C13-0103-102	CAP 1000PF 10% 100V SMD
C23	C13-0103-102	CAP 1000PF 10% 100V SMD
C24	C85-0009-101	CAP VAR 2.5-10PF AIR
C25	C13-0101-101	CAP 100PF 10% 100V SMD
C26	C13-0101-101	CAP 100PF 10% 100V SMD
C27	C13-0101-101	CAP 100PF 10% 100V SMD
C28	C13-0101-101	CAP 100PF 10% 100V SMD
C29	C11-0062-390	CAP 39PF
C69	C13-0103-122	CAP 1200PF 10% 100V SMD
CR1	1N4454	DIODE 200MA 75V SW
CR2	1N4454	DIODE 200MA 75V SW
CR3	1N4454	DIODE 200MA 75V SW
CR4	1N4454	DIODE 200MA 75V SW
E1	J46-0114-001	HEADER, 1 POS
E2	J46-0114-001	HEADER, 1 POS
E3	J46-0114-001	HEADER, 1 POS
E4	J46-0114-001	HEADER, 1 POS
E5	J46-0114-001	HEADER, 1 POS
E6	J46-0114-001	HEADER, 1 POS
E7	J46-0114-001	HEADER, 1 POS
E8	J46-0114-001	HEADER, 1 POS

Table 5. A9A1A1 Discriminator PWB Assembly Parts List (10303-2480 Rev. H) (Cont.)

Ref. Desig.	Part Number	Description
L11	L10-0009-568	COIL .56UH 10% FXD RF
L12	L10-0009-568	COIL .56UH 10% FXD RF
L16	L45-0005-561	INDUCTOR CHIP 560NH
R1	R85-0125-222	RES 2.2K 5% 1/8W FILM
R2	R85-0004-147	RES 301 1% 1/8W FLM
R3	R16-0002-103	RES, 10K 1/2W
R4	R41-0004-202	RES VAR SMD 2K 20% .20W
R5	R85-0004-218	RES 1500 1% 1/8W FLM
R6	R85-0004-262	RES 4320 1% 1/8W FLM
R7	R85-0004-373	RES 56.2K 1% 1/8W SMD
R8	R85-0004-373	RES 56.2K 1% 1/8W SMD
R9	R85-0004-451	RES 332K 1% 1/8W SMD
R10	R85-0004-451	RES 332K 1% 1/8W SMD
R11	R85-0004-458	RES 392K 1% 1/8W SMD
R12	R85-0004-458	RES 392K 1% 1/8W SMD
R21	R85-0004-262	RES 4320 1% 1/8W FLM
R22	R85-0125-103	RES 10K 5% 1/8W FILM
T2	10303-3106-14	TRANSFORMER ASSY
T3	10303-3135	TRANSFORMER ASSY
T4	10303-3106-14	TRANSFORMER ASSY
T5	10303-3102-04	TRANSFORMER ASSY

Table 6. A9A2 Coupler Output PWB Assembly Parts List (10303-2160 Rev. L)

Ref. Desig.	Part Number	Description
2	10303-2161	SCHEM, COUPLER OUTPUT
3	10303-2169	PWB, COUPLER OUTPUT
4	10303-1220-01	CAP, TOROID
5	10303-1215-01	DIVIDER
6	MS18211-25C	FHS,NYLON,4-40 X .875,82D
7	MS51858-2	NUT NYLON 4-40
8	W20-0001-009	WIRE BUSS #24AWG TIN'D CU
9	P15-3140-001	RTV
10	P30-0013-000	THD SLNT (RED)
11	10303-1215-02	DIVIDER
12	E50-0003-013	SLVG TFL .106 ID 10GA NAT
C6	C11-0054-820	CAP,82PF, 1000V, CER
C7	C11-0054-820	CAP,82PF, 1000V, CER
C62	C11-0054-039	CAP, 3.9 PF 1000V, CER

Table 6. A9A2 Coupler Output PWB Assembly Parts List (10303-2160 Rev. L) (Cont.)

Ref. Desig.	Part Number	Description
C63	C11-0054-039	CAP, 3.9 PF 1000V, CER
C64	C13-0105-820	CAP 82PF 10% 100V SMD
C65	C13-0105-221	CAP CER 220PF 5% 50V NPO
C66	C11-0054-430	CAP, 43PF, 1000V, CER
C67	C11-0054-430	CAP, 43PF, 1000V, CER
C73	C13-0107-104	CAP, .1UF 10% 100V CER
C86	C13-0105-102	CAP CER 1000PF 5% 100V
C87	C13-0105-102	CAP CER 1000PF 5% 100V
C88	C07-0007-102	CAP NTWRK 1000PF 10% 100V
C89	C07-0007-102	CAP NTWRK 1000PF 10% 100V
C111	C13-0107-104	CAP, .1UF 10% 100V CER
C112	C13-0107-104	CAP, .1UF 10% 100V CER
CR5	1N4454	DIODE 200MA 75V SW
E14	10303-1210-01	TERMINAL, HIGH VOLTAGE
J3	J92-0023-001	CONN COAX 50 OHM PWB
K7	K28-0008-724	RELAY, SPDT LATCH 24V
K8	K28-0008-724	RELAY, SPDT LATCH 24V
K9	K28-0008-724	RELAY, SPDT LATCH 24V
K10	K28-0008-724	RELAY, SPDT LATCH 24V
K11	K28-0001-224	RLY DPST 24V LATCHING
K12	K28-0001-324	RLY DPST 24V LATCHING
K13	K28-0001-324	RLY DPST 24V LATCHING
K14	K28-0001-224	RLY DPST 24V LATCHING
K15	K28-0001-224	RLY DPST 24V LATCHING
K26	10303-1274	RELAY, DC, DPDT, LATCHING
L7	10303-3146-01	INDUCTOR, 2.8UH
L8	10303-3147-01	INDUCTOR, 5.6 UH
L9	10303-3148-01	INDUCTOR, 11.25UH
L10	10303-3149-01	INDUCTOR, 22.5 UH
L17	10303-3150-01	INDUCTOR, 45UH
L18	10303-3150-01	INDUCTOR, 45UH
L19	10303-3150-01	INDUCTOR, 45UH
P3	J46-0084-322	HDR 2ROW .400/.120 22 PIN
R24	R85-0004-301	RES 10K 1% 1/8W FLM
R27	R85-0004-381	RES 68.1K 1% 1/8W FLM
R28	R85-0004-366	RES 47.5K 1% 1/8W FLM
R29	R85-0004-301	RES 10K 1% 1/8W FLM
U5	I14-0003-004	LM136H-2.5 VOLTAGE REF.

Table 6. A9A2 Coupler Output PWB Assembly Parts List (10303-2160 Rev. L) (Cont.)

Ref. Desig.	Part Number	Description
W1	W-0944	COAX CABLE 50 OHM DBLSHLD
Z1	Z25-0073-002	BEAD FERRITE SMD

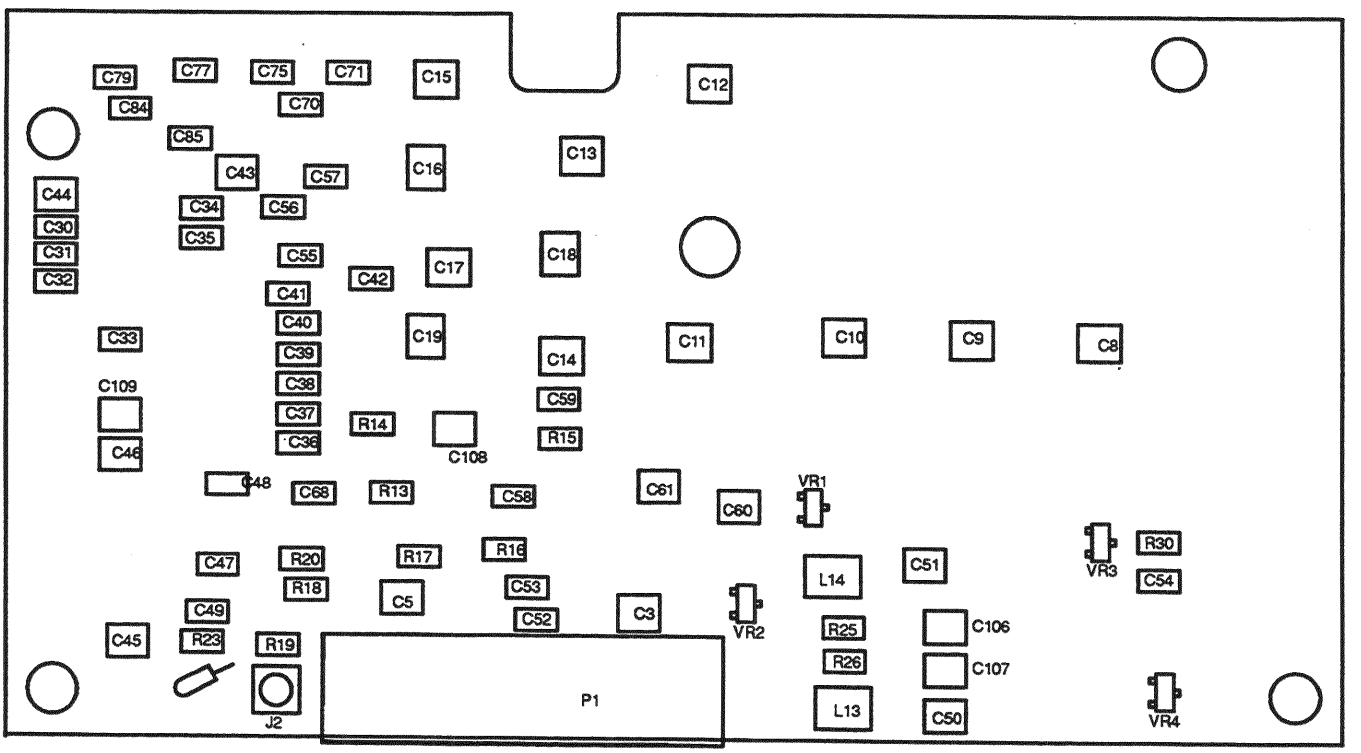


Figure 4. A9A1 Coupler Input PWB Assembly Component Location Diagram (10303-2150 Rev. D) (Sheet 2 of 2)

NOTE: UNLESS OTHERWISE SPECIFIED:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR A COMPLETE DESIGNATION, PREFIX WITH UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.
2. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, +/–5%.
3. ALL CAPACITOR VALUES ARE IN MICROFARADS.
4. VENDOR PART NO. CALLOUTS ARE FOR REFERENCE ONLY. COMPONENTS ARE SUPPLIED PER PART NO. IN PARTS LIST.
5. BACKSLASH (/) DENOTES ACTIVE LOW.
6. ALL INDUCTOR VALUES ARE IN MICROHENRIES.
7. ALL RELAYS SHOWN WITH COIL 'B' LAST ENERGIZED.

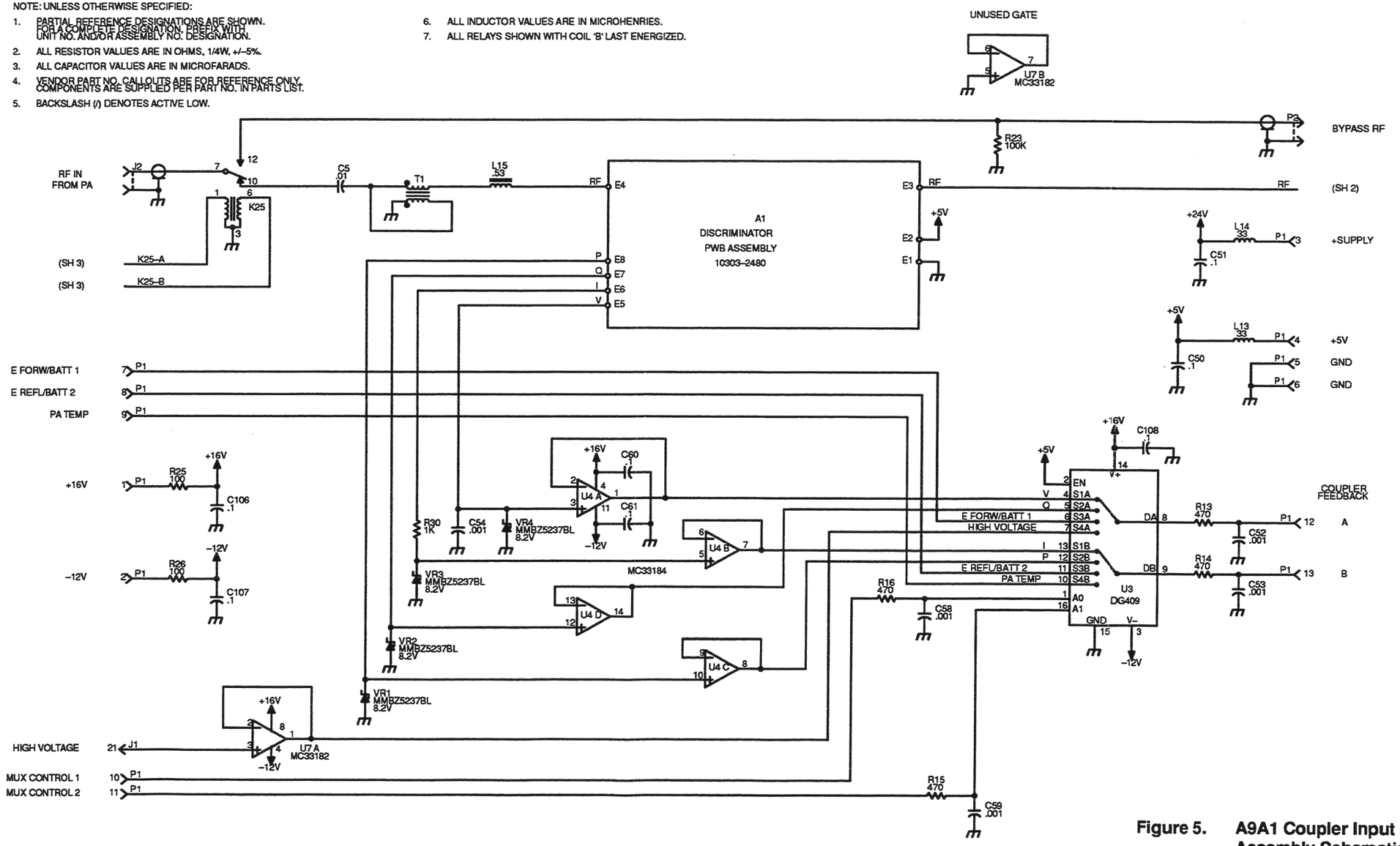
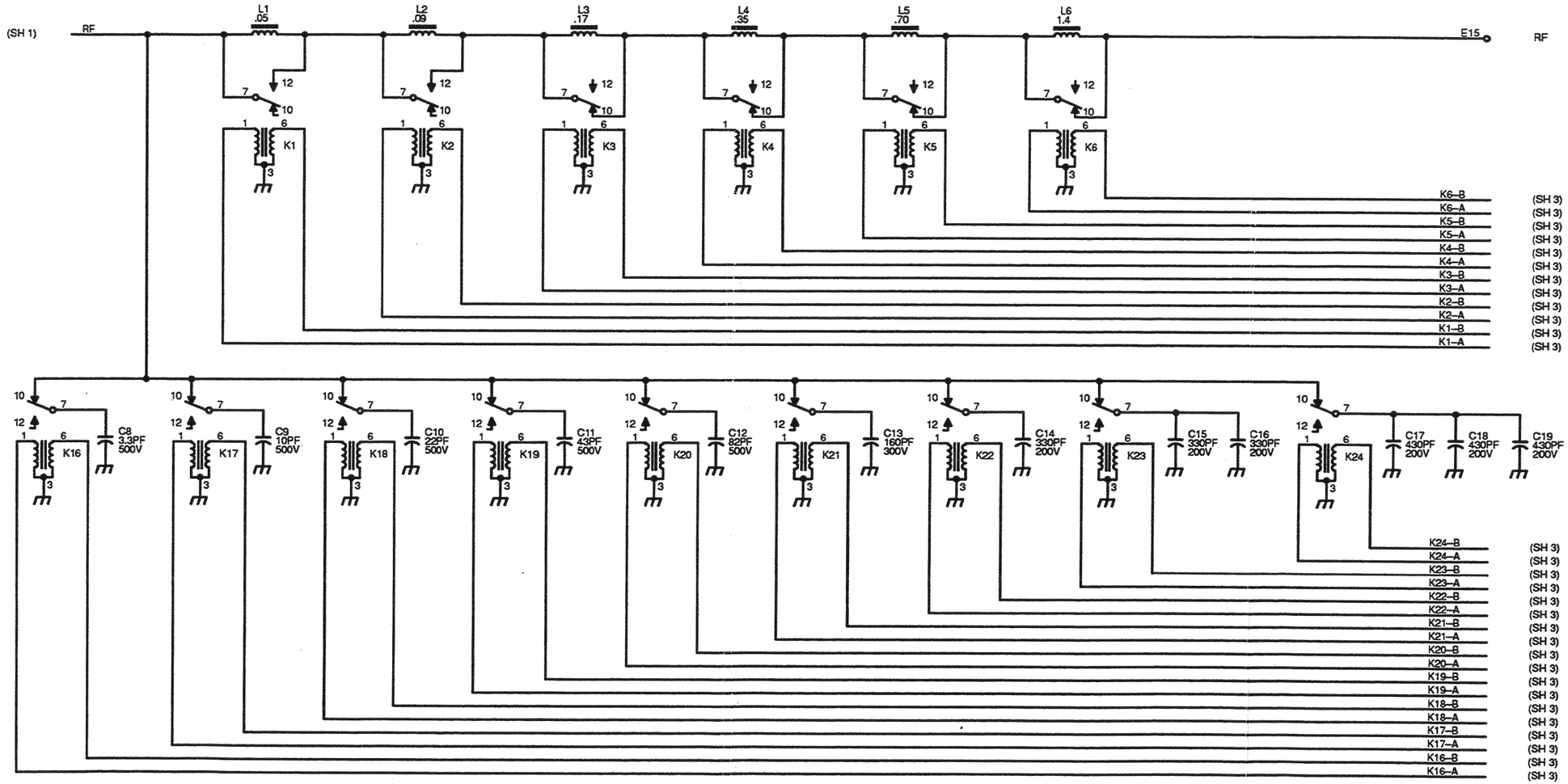
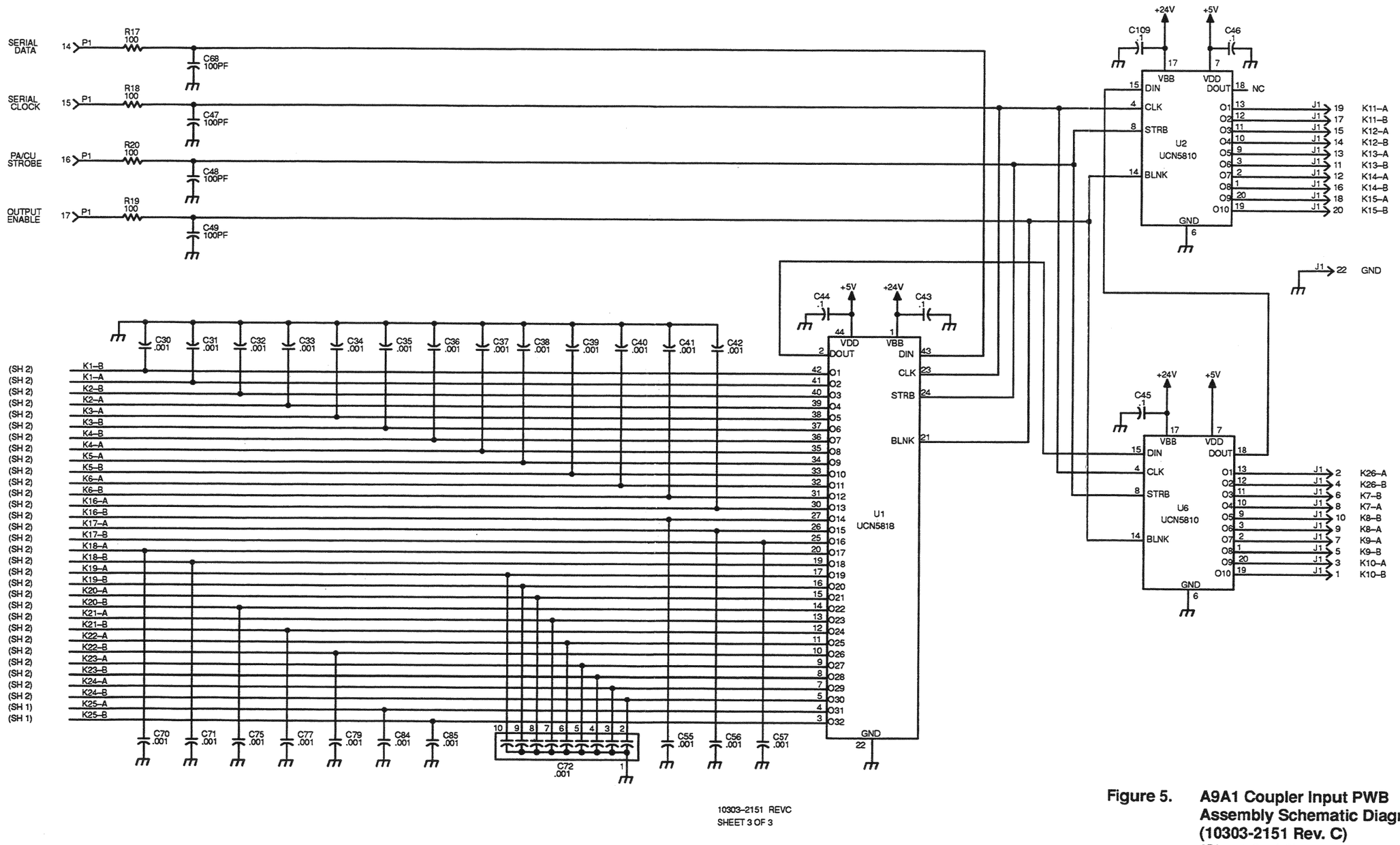


Figure 5. A9A1 Coupler Input PWB Assembly Schematic Diagram (10303-2151 Rev. C) (Sheet 1 of 3)



10303-2151 REVC
SHEET 2 OF 3

Figure 5. A9A1 Coupler Input PWB Assembly Schematic Diagram (10303-2151 Rev. C) (Sheet 2 of 3)



10303-2151 REVC
SHEET 3 OF 3

Figure 5. A9A1 Coupler Input PWB Assembly Schematic Diagram (10303-2151 Rev. C) (Sheet 3 of 3)

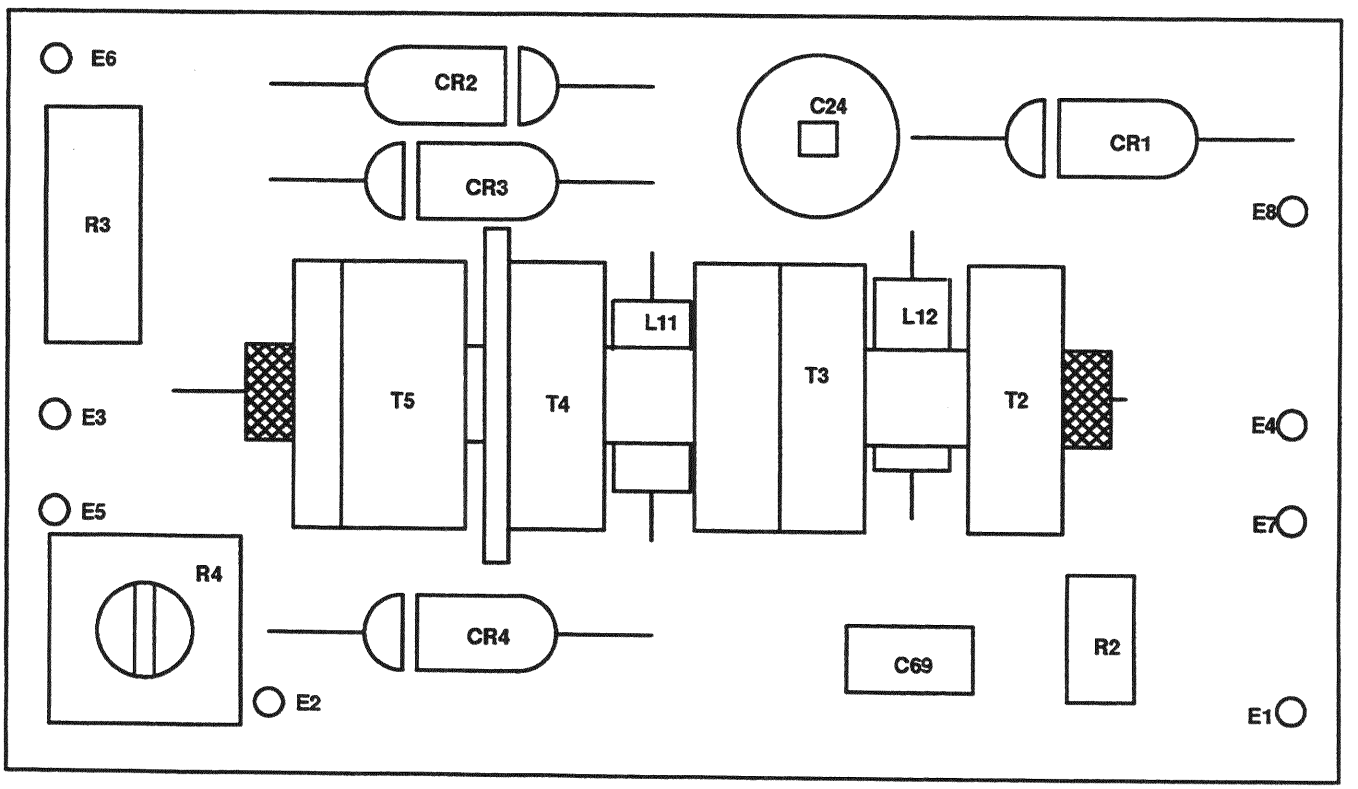


Figure 6. A9A1A1 Discriminator PWB Assembly Component Diagram (10303-2480 Rev. A) (Sheet 1 of 2)

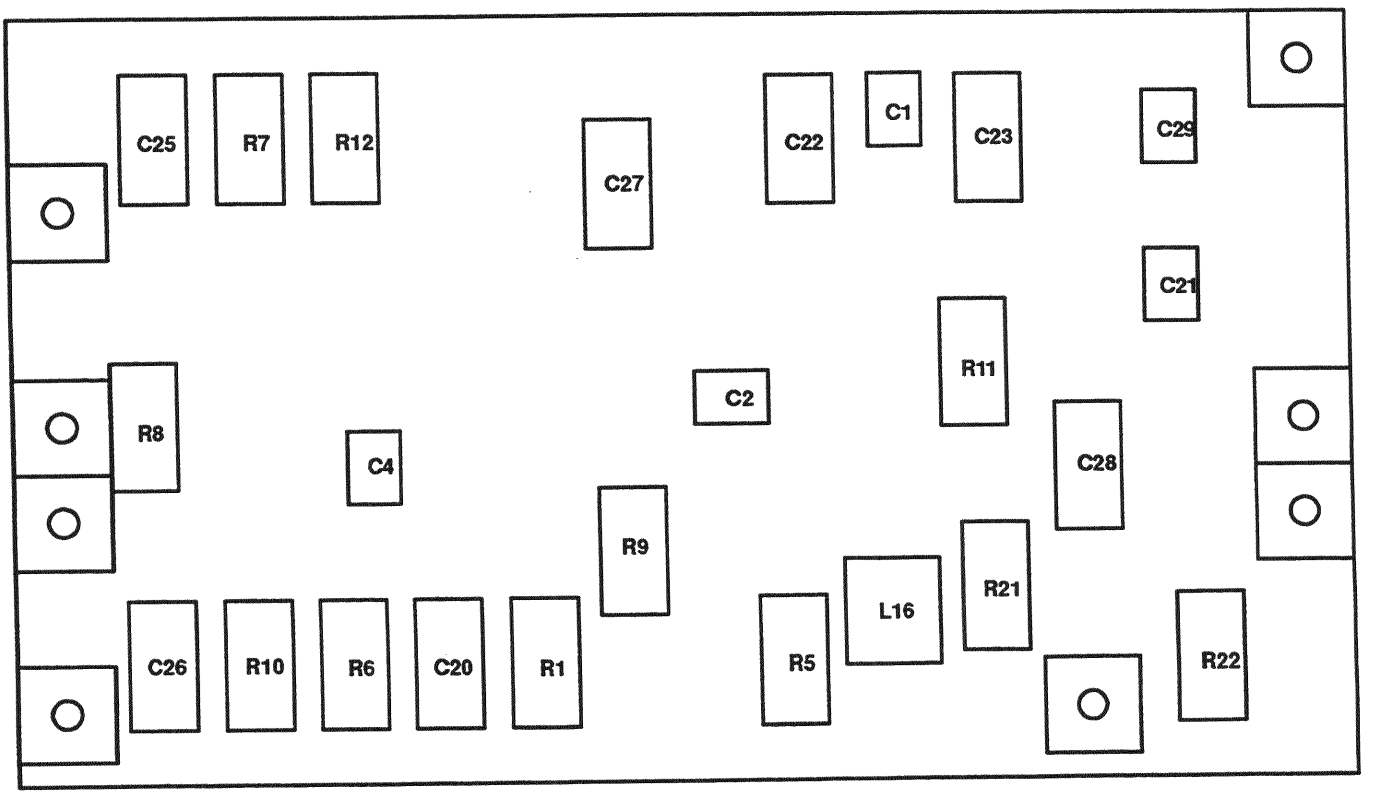
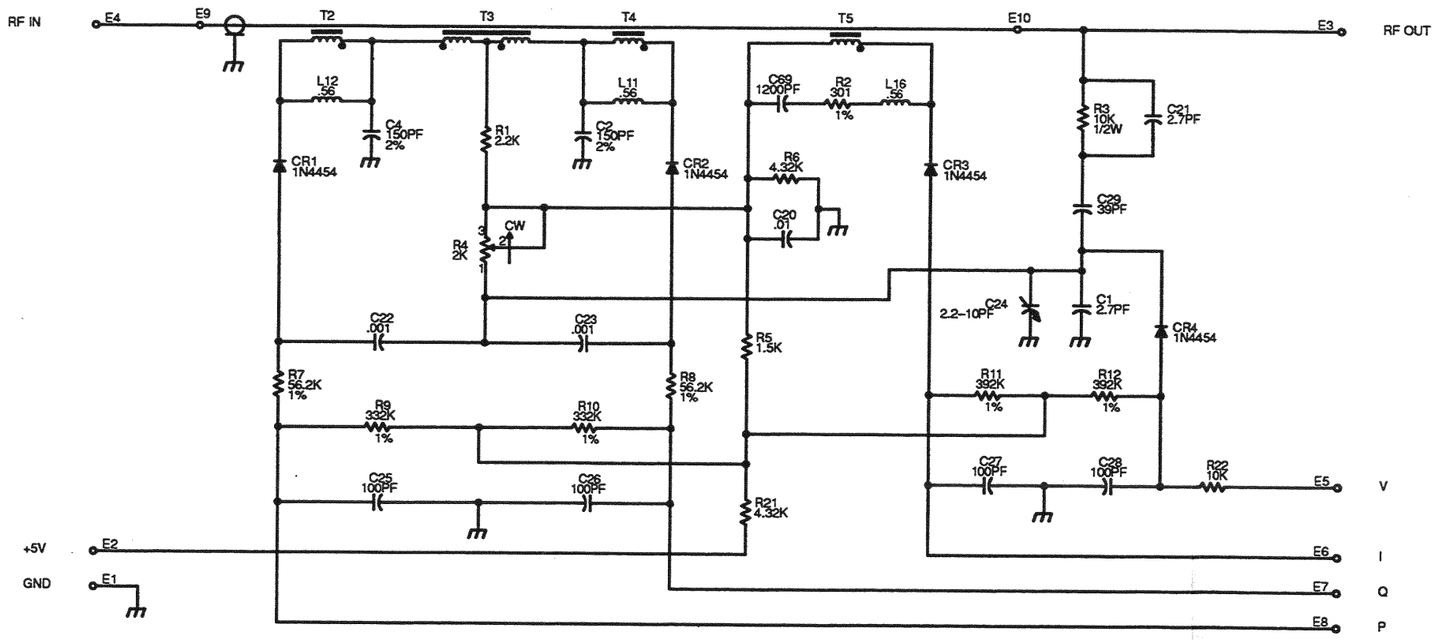


Figure 6. A9A1A1 Discriminator PWB Assembly Component Diagram (10303-2480 Rev. A) (Sheet 2 of 2)

NOTE: UNLESS OTHERWISE SPECIFIED:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR A COMPLETE DESIGNATION, PREFIX WITH UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.
2. ALL RESISTOR VALUES ARE IN OHMS, 1/8W, +/–5%.
3. ALL CAPACITOR VALUES ARE IN MICROFARADS.
4. VENDOR PART NO. CALLOUTS ARE FOR REFERENCE ONLY. COMPONENTS ARE SUPPLIED PER PART NO. IN PARTS LIST.
5. BACKSLASH (/) DENOTES ACTIVE LOW.
5. ALL INDUCTOR VALUES ARE IN MICROHENRIES.



HIGHEST REFERENCE DESIGNATION				
C69	CR4	E10	L16	R22
T5				
REF. DESIGNATIONS NOT USED				
C3	C5–C19		C30–C68	
L1–L10		L13–L15		
R13–R20	T1			

10303–2481 REVA
SHEET 1 OF 1

Figure 7. A9A1A1 Discriminator PWB Assembly (10303-2481 Rev. A)

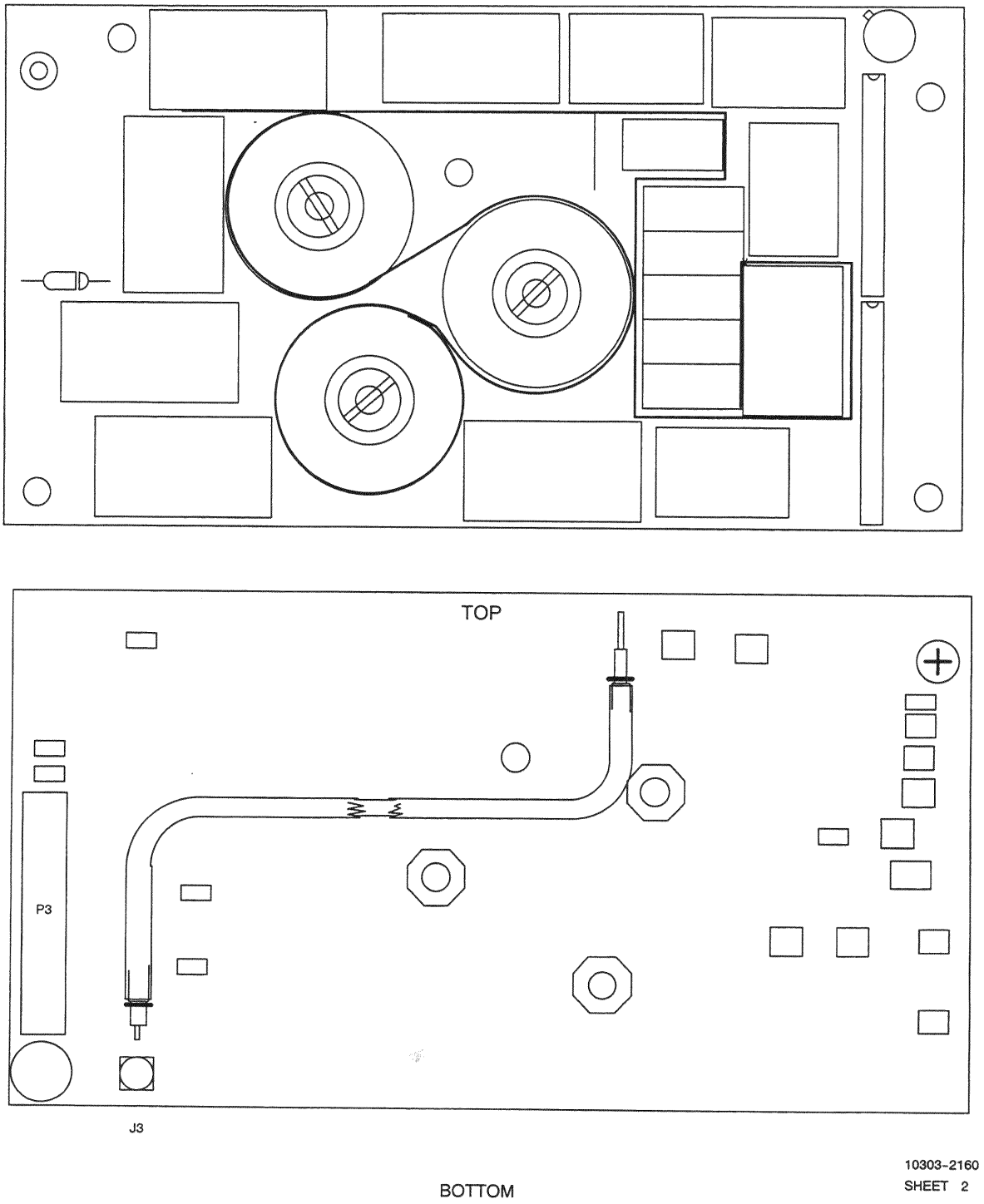
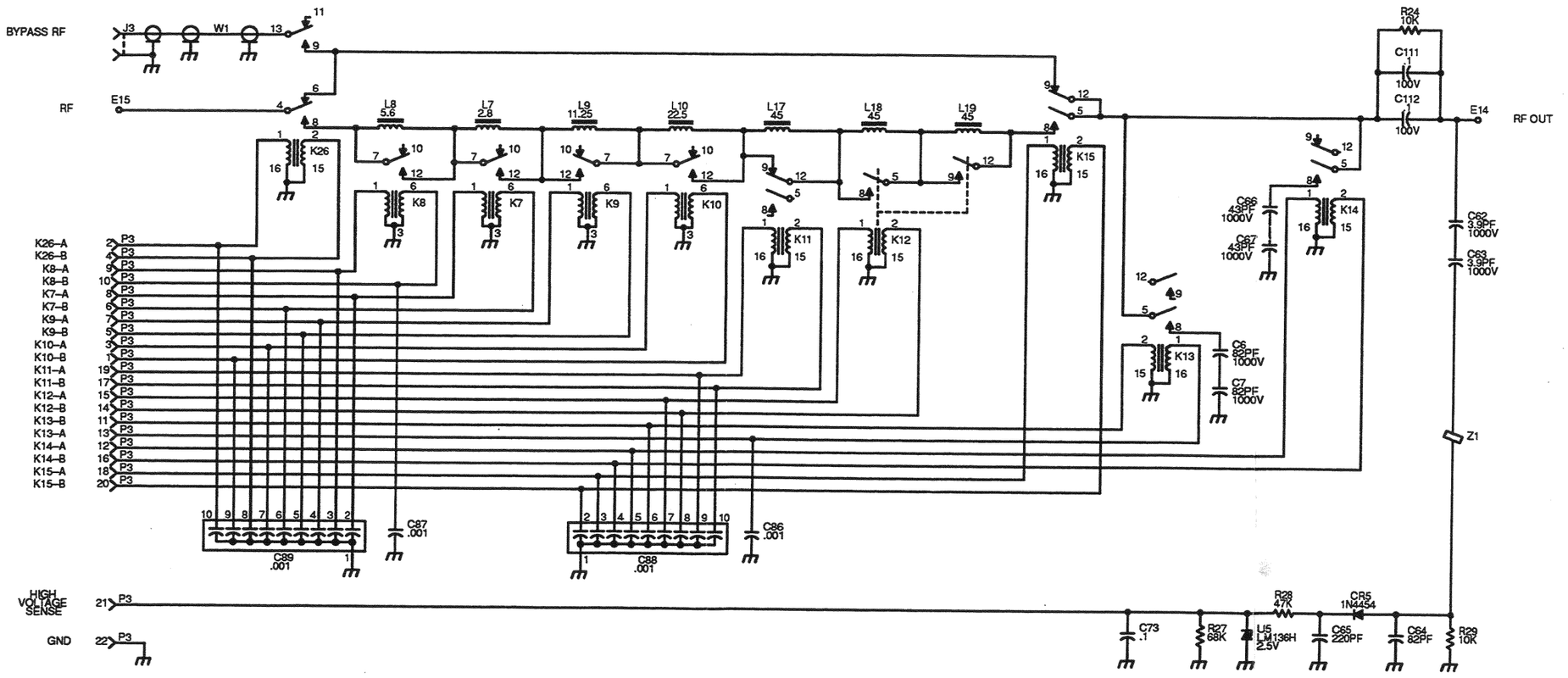


Figure 8. A9A2 Coupler Output PWB Assembly (10303-2160 Rev. G)

NOTE: UNLESS OTHERWISE SPECIFIED:

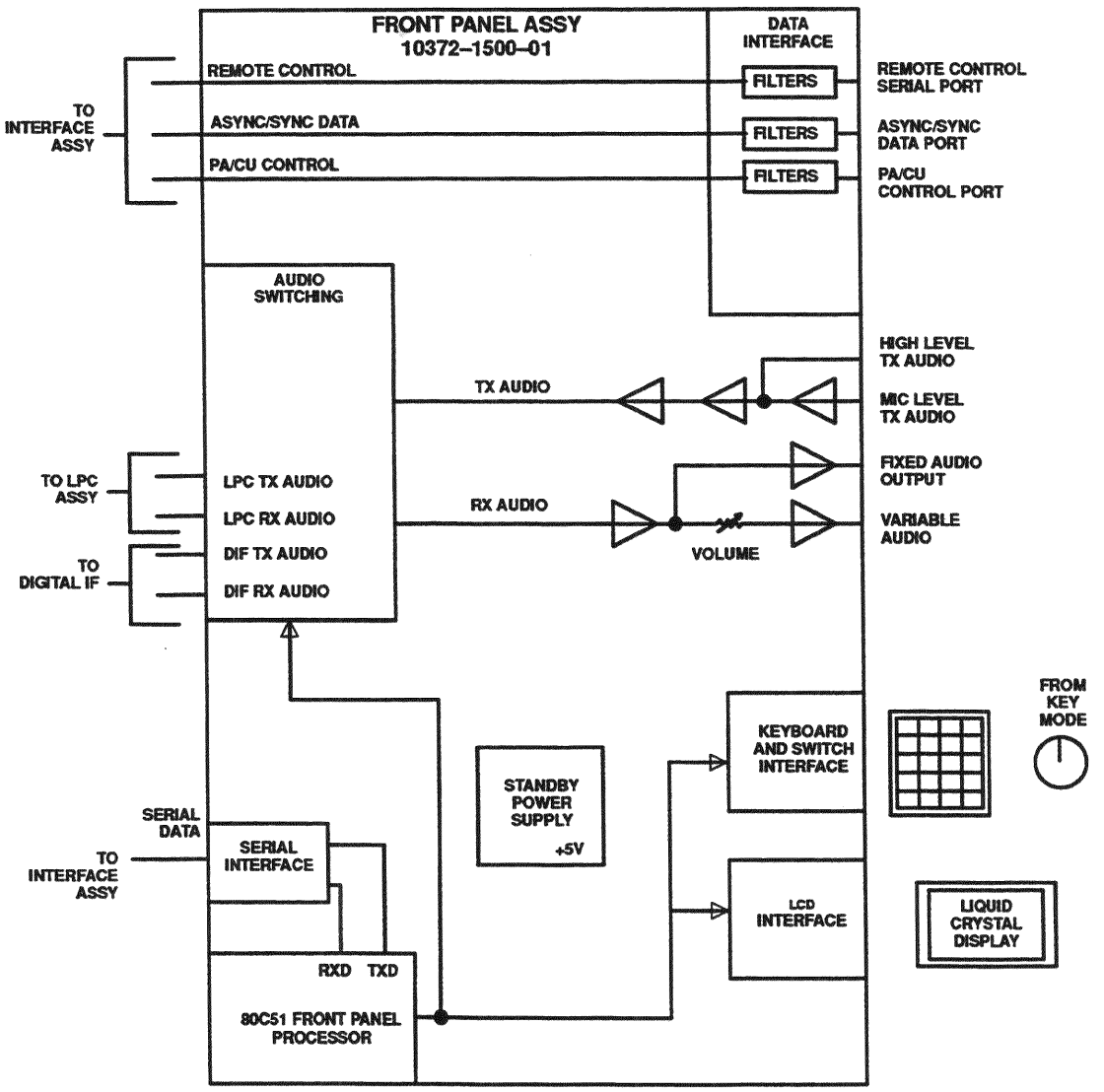
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR A COMPLETE DESIGNATION, PREFIX WITH UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.
2. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, +/–5%.
3. ALL CAPACITOR VALUES ARE IN MICROFARADS.
4. VENDOR PART NO. CALLOUTS ARE FOR REFERENCE ONLY. COMPONENTS ARE SUPPLIED PER PART NO. IN PARTS LIST.
5. BACKSLASH (/) DENOTES ACTIVE LOW.



10303-2161 REVC
SHEET 1 OF 1

Figure 9. A9A1 Coupler Input PWB Assembly Schematic Diagram (10303-2161 Rev. C)

A10
FRONT PANEL



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A10 FRONT PANEL

1. GENERAL DESCRIPTION

The A10 Front Panel Assembly interfaces to all connections/functions of the radio, except the batteries. These interfaces include handsets, data devices, remote control devices, external RF power amplifiers, user input from the keypad, FUNCTION and CHANNEL controls, user status information via the LCD display, and the antenna for RF communications. The A10 Front Panel routes, buffers, and does analog processing on all audio, in and out of the radio.

The A10 Front Panel also has a microcomputer that processes inputs from the keypad, FUNCTION, and CHANNEL controls. It communicates the processed information to the radio and to the LCD display on the Front Panel. The A10 Front Panel microcomputer also receives information from the radio to display on the LCD display, and to set audio routing.

ALE standby battery power saving operation also depends on the A10 Front Panel. The Front Panel operates from its own power supply when the radio is turned on and periodically turns the main radio on and off to save power in ALE standby.

2. INTERFACE CONNECTIONS

Tables 1 through 5 list the A10 Front Panel Assembly input and output signals.

Table 1. J1* AUDIO Input/Output Signals

Connector and Pin	Signal	Comments
J1-A	Ground	Not filtered
J1-B	RX Handset Audio Output	10 Vp-p maximum into 1 Kohm
J1-C	PTT Key/Fill RTS	PTT active low, pulled up to +5 V
J1-D	Mic TX Audio	1.4 mVrms, Zin = 150 ohm
J1-E	Retrans Key/Fill Clock	5 V CMOS levels
J1-F	Fill Data	5 V CMOS levels

*J1 is a filtered connector providing 50 dB attenuation above 100 MHz.

Table 2. J2* Input/Output Signals

Connector and Pin	Signal	Comments
J2-A	Fixed Level WB RX Audio Out	2.2 Vp-p, 10 Hz-10 kHz, Rout = 600 ohm
J2-B	Fixed Level WB TX Audio In	2.2 Vp-p, 10 Hz-10 kHz, Rin = 100 K
J2-C	Data Out	RS-232/MIL-188 Sync/Async
J2-D	Data In	RS-232/MIL-188 Sync/Async
**J2-E	+24V Out (E1 to E3) or Remote Power On (E1 to E2)	+24 V out – Battery Voltage 20-32 V, 100 mA max., Remote power on – Active low pulled up to 24 V

*Filtered connector, maximum data rate = 9600 baud

**Normal Jumper E1 to E2

Table 2. J2* Input/Output Signals (Cont.)

Connector and Pin	Signal	Comments
J2-F	TX Keyline	Active low, 5 V levels
J2-H	RLSD	RS-232/MIL-188 levels
J2-J	Ground	Not filtered
J2-K	Remote Async Data In	RS-232/MIL-188 Async only
J2-L	CTS	RS-232/MIL-188 levels
J2-M	Sync Clock In	RS-232/MIL-188 levels
J2-N	Remote Async Data Out	RS-232/MIL-188 Async only
J2-P	RTS	RS-232/MIL-188 levels
J2-R	Sync Clock Out	RS-232/MIL-188 levels

Table 3. J6 EXTERNAL PA CONTROL Input/Output Signals

Connector and Pin	Signal	Comments
J6-A	Hop Clock Out	5 V CMOS levels
J6-B	PA Control Data –	+5 V balanced PA control data
J6-C	PA Control Data +	+5 V balanced PA control data
J6-D	PA ON/OFF	ON is bw, OFF is open collector 60 V maximum
J6-E	Ground Return Battery Charger	Ground return for charger power
J6-F	R/T Ground Return	Ground return for R/T power
J6-G	PA Feedback –	Ground of analog PA
J6-H	PA Feedback +	0.5 - 7 V analog signal
J6-J	Ext DC + for Battery Charger	10 -32 Vdc power for internal charger
J6-K	R/T Ext DC +	20 - 32 Vdc, 1 amp maximum power from PA for R/T

Table 4. J5 Input/Output Signals

Connector and Pin	Signal	Comments
J5-1	Sync Clock In	RS-232 levels ±12 V or MIL-188 ±6 V
J5-2	Ground	0.0 Vdc
J5-3	Data Out	RS-232/MIL-188 levels, async/sync, up to 9600 baud
J5-4	Ground	0.0 Vdc
J5-5	Data In	RS-232/MIL-188 levels, async/sync, up to 9600 baud
J5-6	RTS	RS-232 levels ±12 V or MIL-188 ±6 V
J5-7	Remote Async Data Out	RS-232/MIL-188 levels, sync, up to 9600 baud

Table 4. J5 Input/Output Signals (Cont.)

Connector and Pin	Signal	Comments
J5-8	Sync Clock Out	RS-232 levels ±12 V or MIL-188 ±6 V
J5-9	Remote Async Data In	RS-232/MIL-188 levels, sync, up to 9600 baud
J5-10	/Remote Power On	Active low input, 0.0 Vdc, pulled up to battery voltage
J5-11	RLSD	RS-232 levels ±12 V or MIL-188 ±6 V
J5-12	CTS	RS-232 levels ±12 V or MIL-188 ±6 V
J5-13	/TX Keyline	Active low input, 0.0 Vdc, 30 mA maximum
J5-14	LPC RX Audio	2.2 Vp-p, 10 – 10 kHz audio BW
J5-15	Ground	0.0 Vdc
J5-16	Dig IF RX Audio	2.2 Vp-p, 10 – 10 kHz audio BW
J5-17	Ground	0.0 Vdc
J5-18	LPC TX Audio	2.2 Vp-p, 10 – 10 kHz audio BW
J5-19	Ground	0.0 Vdc
J5-20	Dig IF TX Audio	2.2 Vp-p, 10 – 10 kHz audio BW

Table 5. Front Panel Connector J7 Input/Output Signals

Connector and Pin	Signal	Comments
J7-1	Front Panel Data from Interface	+5 V, 0.0 V CMOS levels, async, 9600 baud
J7-2	Ground	0.0 Vdc
J7-3	Front Panel Data to Interface	+5 V, 0.0 V CMOS levels, async, 9600 baud
J7-4	Remote Masked ROM Enable	Not used
J7-5	/PA On/Off	+5 V, 0.0 V CMOS, Active Low signal
J7-6	PA control Data +	+5 V, 0.0 V, Async, 150 k baud
J7-7	Ground	0.0 Vdc
J7-8	PA Control Data –	+5 V, 0.0 V, Async, 150 k baud
J7-9	PA Feedback +	Sensed analog feedback, 0.5 Vdc – 7 Vdc maximum, 4.3 Vdc nominal
J7-10	Ground	0.0 Vdc
J7-11	Ground	0.0 Vdc
J7-12	Ground	0.0 Vdc
J7-13	+24 Vdc	18 – 32 Vdc battery input voltage
J7-14	Zeroize	Active log signal, 0.0 Vdc
J7-15	–12 V Main	–12 Vdc from main power supply, 70 mA maximum
J7-16	Test ControlPort Enable	Not used

Table 5. Front Panel Connector J7 Input/Output Signals (Cont.)

Connector and Pin	Signal	Comments
J7-17	Ground	0.0 Vdc
J7-18	Ground	0.0 Vdc
J7-19	Ground	0.0 Vdc
J7-20	Ground	0.0 Vdc
J7-21	Ground	0.0 Vdc
J7-22	Standby/Normal	+5 V, 0.0 V CMOS, 0.0 V = Standby supply, +5 V = Main supply
J7-23	Ground	0.0 Vdc
J7-24	Power On Protect	+5 V CMOS, active high
J7-25	Battery Backup	+2.8 V to +3.9 Vdc battery backup voltage
J7-26	+5 V Main	+5 Vdc from main supply, 20 mA maximum
J7-27	Ground Return	0.0 Vdc, 1 amp maximum, DC return for radio
J7-28	External DC +	18 – 32 Vdc, 1 amp maximum, DC power to operate radio
J7-29	+15 V Main	+15 Vdc from main supply, 70 mA maximum
J7-30	Hop Clock Out	+5 V, 0.0 V CMOS level, active high signal
J7-31	Ground Return for Battery Chargers	0.0 Vdc, 3.4 amps maximum, DC return for battery chargers
J7-32	Ground Return for Battery Chargers	0.0 Vdc, 3.4 amps maximum, DC return for battery chargers
J7-33	External DC + for Battery Chargers	10 – 32 Vdc, 3.4 amps maximum, DC power to operate battery charger
J7-34	External DC + for Battery Chargers	10 – 32 Vdc, 3.4 amps maximum, DC power to operate battery charger

3. TECHNICAL DESCRIPTION

All operator interface is performed within the A10 Front Panel Assembly (10372-1500-01), which consists of the following subassemblies:

- A10A1 Audio/Control PWB Assembly (10303-2100)
- A10A1A1 LCD Assembly (10372-1210)
- A10A1A2 Standby Power Supply Assembly (10303-2250)
- A10A2 Keypad PWB Assembly (10303-2110-01)

The A10A1 Audio/Control Assembly (10303-2100) contains the microcomputer, audio processing, FUNCTION control, CHANNEL control, volume control, handset connector, data connector, and external RF PA connector. The A10A1A1 LCD Assembly (10372-1210) and A10A1A2 Standby Power Supply Assembly (10303-2250) are subassemblies to the A10A1 Audio/Control PWB Assembly. The A10A1 Audio/Control PWB Assembly and the A10A2 Keypad Assembly mount to the Front Panel metal casting to make up the A10 Front Panel Assembly.

Parts lists, component location diagrams, and schematic diagrams for the various assemblies that make up the A10 Front Panel Assembly are located at the end of this section.

3.1 A10A1 Audio/Control PWB Assembly Architecture and Operation

The A10A1 Audio/Control PWB Assembly uses an 83C51FA Microcontroller with external EEPROM, SRAM, and I/O ports to form a microcomputer to perform the functions outlined above. Figure 1 is a detailed block diagram of the A10A1 architecture. The A10A1 schematic is located at the end of this section.

The Front Panel needs power when the rest of the radio is off for standby, so it contains its own 5V power supply and operates independently from the rest of the radio, which receives its power from the A7 Power Supply Assembly. To accomplish this, the 83C51FA Microcontroller U1 has its own 9.216 MHz crystal for a clock, rather than using the main radio 9.6 MHz clock. It also has its own power supply supervisory (IC U17).

U17 provides a 50 msec power on reset/power off reset when the 5 V power supply drops below 4.65 V. It also provides a watchdog timer and automatic switchover to the battery backup for the SRAM U9, with RAM chip select lockout while on battery backup. The battery backup is provided from the A11 motherboard at J7 pin 25 and originates from the A1A1 Interface Assembly lithium backup battery. The watchdog timer function of U17 may be disabled by floating U17 pin 17. This is accomplished by removing R10 from the A10A1 Audio/Control PWB Assembly. U1 is designed to run with or without external memory and has the following four integrated eight-bit I/O ports:

- Port 0 is used as the multiplexed address/data lines AD0–AD7.
- Port 1 is used as an I/O port in either mode of memory use.
- Port 2 is used as the high order address lines A8–A15 when U1 is used with external memory.
- Port 3 makes up control I/Os such as /WR, /RD, that are necessary for use with external memory.

The A10A1 Audio/Control PWB Assembly uses U1 in both modes of operation. The /EA line of U1 (U1–35) is used to determine which mode to use. /EA low will cause U1 to use external program memory (U8) and /EA high will use internal ROM for the lower 32K of address space. The internal ROM is used only during the power up sequence; therefore, the /EA line should always be low in normal operation.

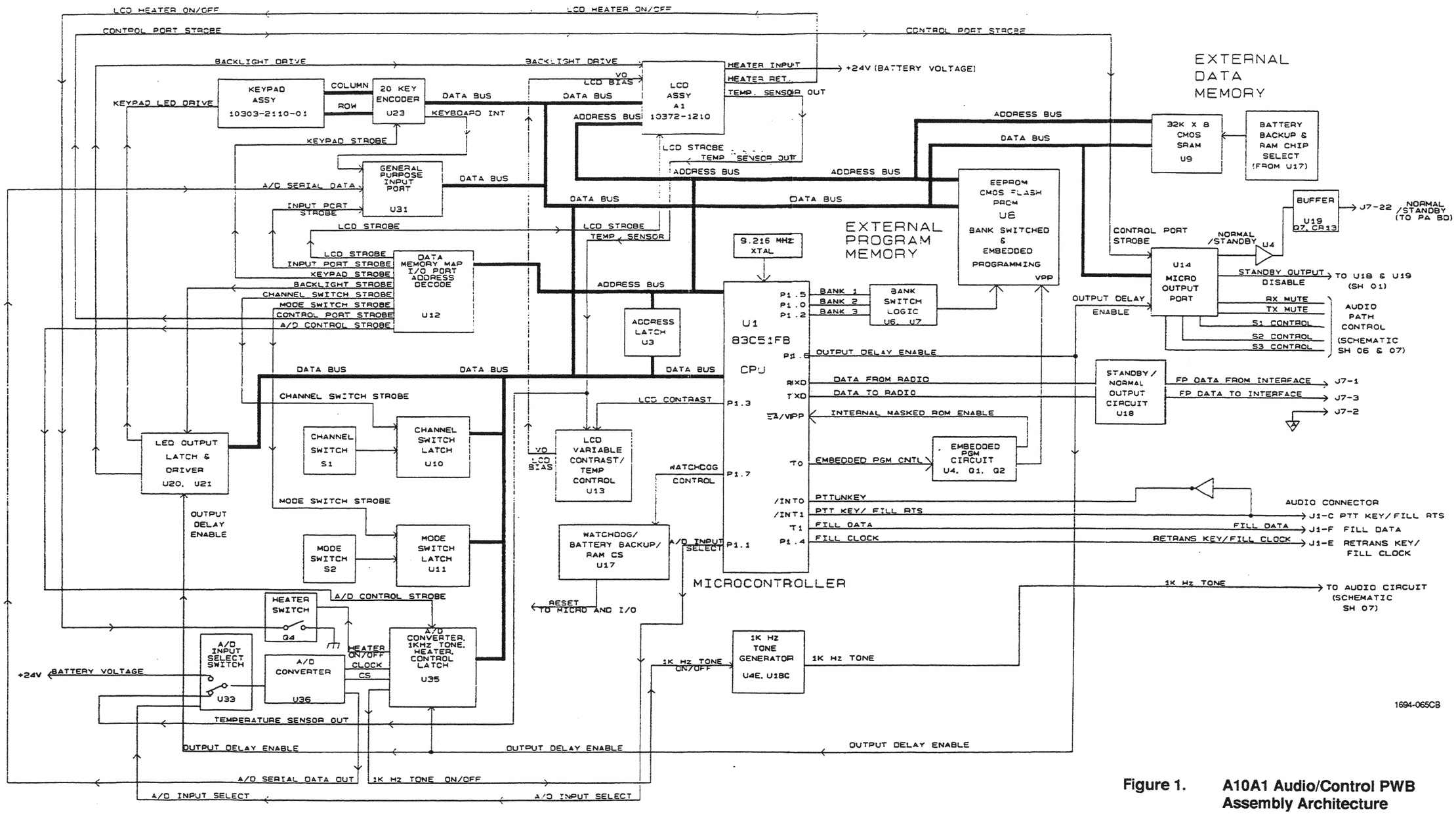


Figure 1. A10A1 Audio/Control PWB Assembly Architecture

3.1.1 Microcontroller U1 Direct I/O and Control

U1, the 83C51FA Microcontroller of the A10A1 Audio/Control PWB Assembly, performs many I/O functions from the integral I/O Port 1. U1 uses P15, P10, and P12 as the extra address lines for the bank switching of the flash EEPROM U8. P11 is an output used to control SPDT analog switch U33, to select the analog input for A/D converter U36. P13 is used as an output to set user selected contrast levels for the front panel A10A1A1 LCD Assembly. P14 is used for a fill clock output, which is used to operate a fill device through the handset connector J1. P16 is used as an output that controls the tri-state output enable lines for all external data memory mapped output ports.

After the firmware has initialized the external data memory mapped output ports to a known state, this line is sent low to activate all outputs. P17 is used to toggle the built-in watchdog timer of U17 (MAX691). This line must change states at least once per second or the watchdog timer of U17 will fire and apply a reset to U1. The internal UART of U1, located at Port 3 (U1–11,U1–13), is used to communicate to the radio at 9600 baud when the front panel is in normal operation. Port 3 also provides hardware interrupt inputs INT0 (U1–14) and INT1 (U1–15), which are used by the front panel firmware to detect handset PTT keys (INT1) and PTT unkeys (INT0). Port 3 also provides two timer I/Os. The front panel firmware uses timer T0 as an output to control data mapped I/O disable and set U1's /EA line high. Timer T1 is used as a bi-directional I/O for fill data, either from or to a fill device connected at the handset connector J1.

The fill device interface is intended to work with a RF-5961 fill gun. The fill device is a slave type device that is controlled by the equipment it is connected to, and can load/read encryption information. The RF-5961 interfaces at the handset connector J1. The fill device is activated by an RTS signal at J1-C, which is generated by the INT1 line of U1. Fill data is synchronous. U1 provides the clock from P14 to J1-E, and reads/sends fill data from T1 timer U1-17 to J1-F. The fill interface is accessed by the user through front panel menu selections.

3.1.2 Microcontroller U1 Memory and I/O Ports

Figure 2 is a memory map diagram of the A10A1 Audio/Control Assembly microcomputer U1. U1 is capable of running with no external memory because it has 256 bytes of internal RAM and 8K bytes of internal ROM. This ROM; however, is insufficient for the tasks necessary for the front panel, so flash EEPROM U8 provides 256K bytes of program memory. U9 is a SRAM that provides 32K bytes of battery-backed data memory. Figure 2 shows how the internal/external memory and other I/O ports of the front panel microcomputer are memory mapped. U1 has only 16 address lines which allow it to interface directly with 64K bytes of both program and data memory. U1 uses /PSEN from pin 32 to access program memory, and /RD and /WR from pins 19 and 18 respectively to access data memory. Since U8 has 256K bytes of memory and U1 has only 64K bytes of addressing capability, a technique of bank switching the program memory using the internal port 1 pins of U1 as additional address lines is used. There are eight 32K banks in the 256K bytes of U8 and the lower 32K bytes are always mapped to U1 external program address space 0000H to 7FFFH, while the upper 32K bytes are the other seven banks of U8, which are moved into the U1 external program address space from 8000H to FFFFH as necessary. The data memory appears as a separate 64K bytes of memory to U1. Figure 2 shows how the 32K byte SRAM and outside world I/O ports are address-mapped to the data memory space. The I/O ports are partially decoded to the most significant nibble of the hex address by decoder IC U12, and the resultant address overlap of the ports causes the eight I/O ports to fill the entire 32K of upper data memory.

Table 6 summarizes the use of the eight I/O ports.

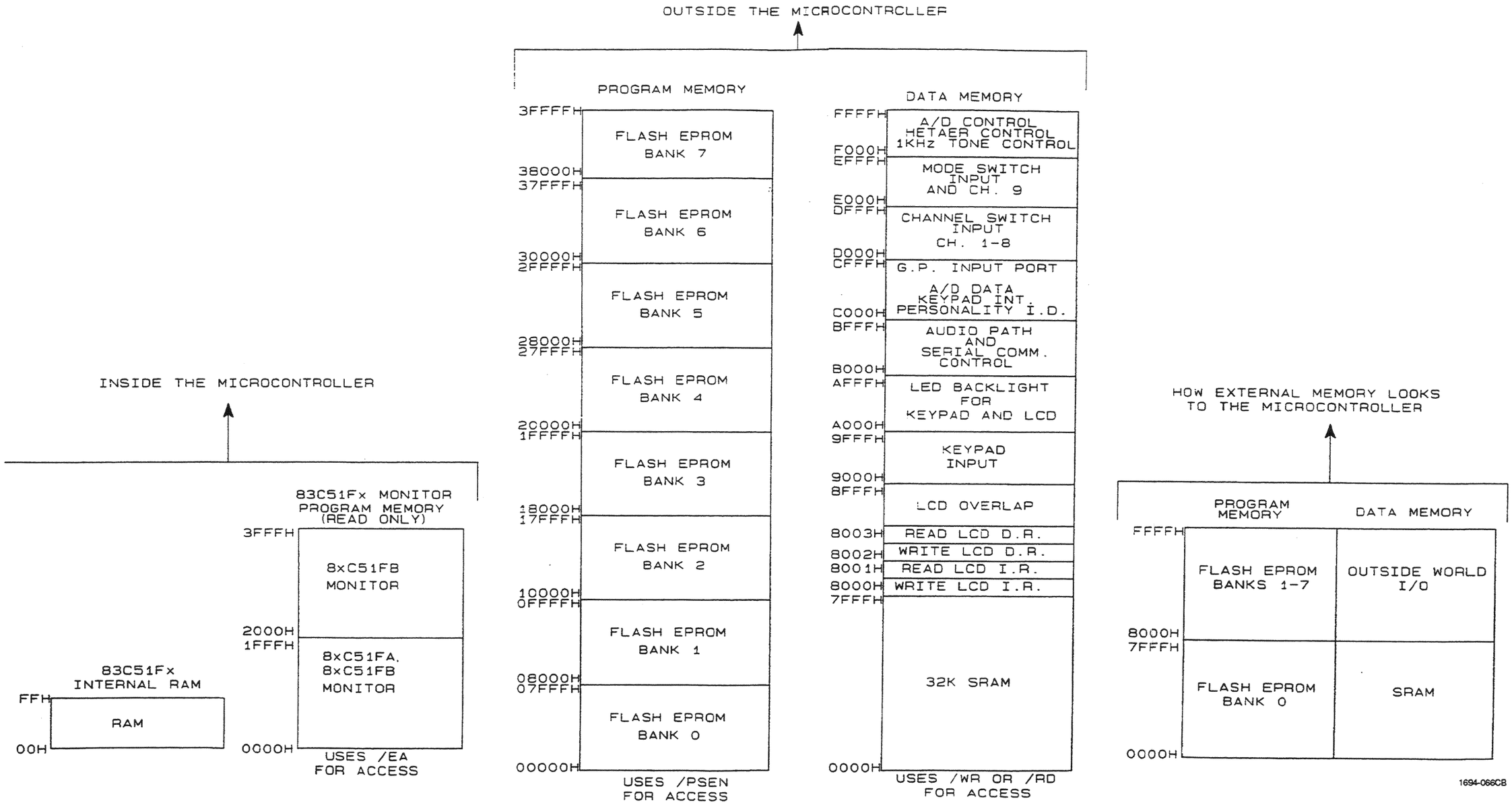


Figure 2. Memory Map Diagram

Table 6. I/O Port Usage

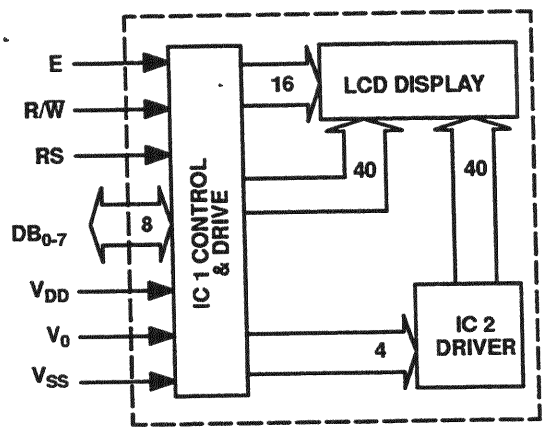
I/O Port	Address	Function
Port 1	8xx0H 8xx1H 8xx2H 8xx3H	LCD write instruction register LCD read instruction register LCD write data register LCD read data register
Port 2	Á9xxxH	Keypad data input port
Port 3	AxxxH	LED Backlight control output port
Port 4	BxxxH	Audio Path control output port
Port 5	CxxxH	General purpose input port
Port 6	DxxxH	CHANNEL control switch input port
Port 7	ExxxH	FUNCTION Control switch input port
Port 8	FxxxH	A/D, heater, and 1 kHz tone control output port

3.1.2.1 Port 1 – LCD Read/Write Register

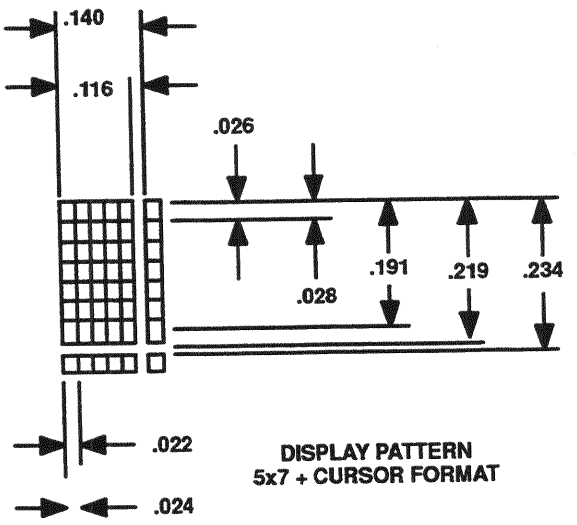
Figure 3 is a LCD block diagram and interface definition. The A10A1A1 LCD Assembly connects to the A10A1 Audio/Control PWB Assembly at J3, E6, E7, E8, and E9. The A10A1A1 LCD Assembly consists of a 5 x 7 dot matrix alphanumeric liquid crystal display of 2 lines of 16 characters with IC controller, LED backlight, and heater/temperature sensor. The LCD controller is a stand-alone dedicated microcontroller with its own clock. It is a bi-directional parallel, interfaced directly to the data bus of the A10A1 Audio/Control PWB Assembly at J3.

The A10A1Audio Control PWB Assembly provides 5 V power, LCD contrast voltage, and a direct interface to the data and address of the U1 microcontroller. The partially decoded address of U1 is further decoded for instruction and data register read and write access by using A0 (RD/WR) and A1 (INST/DATA REG) of the microcontroller address bus directly at J3, along with the LCD strobe generated by U12–15, to have complete access to the LCD controller IC. The LED backlight is driven at J3–15 by the output of U21 which provides 9 levels of intensity adjustment. The LED backlight draws 30 mA maximum. The LCD heater/sensor has flying leads that interface directly to the A10A1 Audio/Control PWB Assembly at E6 and E7 for the temperature sensor, E8 and E9 for the heater. The temperature sensor provides temperature information to U13 for analog contrast compensation and to the A/D converter for heater control data to the A10A1 Front Panel firmware. LCD contrast voltage is set by U13 and can range over 1V to –7V over temperature and user-set contrast levels. Variable contrast is derived from a variable duty cycle 9KHz, 5 V pulse train from U1–5. The contrast setting is held constant over temperature from the analog compensation of the temperature sensor. The 2W heater is turned on and off by the A10A1 front panel firmware when the LCD temperature is below –20C and above 0C, respectively.

PIN NO.	LABEL	DESCRIPTION
1	VSS	POWER SUPPLY GROUND
2	VDD	LOGIC POWER SUPPLY + VDC
3	VO	CONTRAST VIEWING ANGLE ADJUSTMENT VOLTAGE
4	RS	REGISTER SELECT: HIGH = DATA INPUT LOW =INSTRUCTION INPUT
5	R/W	READ/WRITE: HIGH = READ LOW = WRITE
6	E	ENABLE STROBE
7	DBO	BIT 0 OF BI-DIRECTIONAL DATA BUSS
8	DB1	BIT 0 OF BI-DIRECTIONAL DATA BUSS
9	DB2	BIT 0 OF BI-DIRECTIONAL DATA BUSS
10	DB3	BIT 0 OF BI-DIRECTIONAL DATA BUSS
11	DB4	BIT 0 OF BI-DIRECTIONAL DATA BUSS
12	DB5	BIT 0 OF BI-DIRECTIONAL DATA BUSS
13	DB6	BIT 0 OF BI-DIRECTIONAL DATA BUSS
14	DB7	BIT 0 OF BI-DIRECTIONAL DATA BUSS
15	ANODE	LED BACKLIGHT POSITIVE (+5V @ 30mA)
16	CATHODE	LED BACKLIGHT NEGATIVE (CONNECT TO GROUND)



FUCTIONAL BLOCK DIAGRAM



CHARACTER DISPLAY PATTERN

1694-069

Figure 3. LCD Block Diagram and Interface Definition

3.1.2.2 Port 2 – Keypad Data Input

The A10A2 Keypad PWB Assembly is a 20-key LED backlit keypad that interfaces to the A10A1 Audio/Control Assembly at P4. The 20 keys are organized into a matrix of four columns by five rows. The A10A1 Audio/Control Assembly uses U23, a 74C923 keypad scan IC, to monitor the A10A2 keypad. The keypad scan IC scans the rows and columns at a 100 Hz rate set by C24. When a key press is sensed, U23 waits a debounce time of 50 msec set by C23. If the key press is still present after the debounce, U23 sets the data available line U23–13 high, which is monitored by U1 through general purpose input Port U31. U1 then reads the five-bit, parallel keypad data from U23 directly onto the data bus from address 9xxxH, which returns the data available line back to low. The LED backlighting of the A10A2 Keypad Assembly is driven by U21 with nine user-selectable levels of intensity, drawing 30mA at the maximum intensity.

3.1.2.3 Port 3 – LED Backlight Control Output

The A10A1 Microcontroller U1 uses U20 as a dedicated eight-bit parallel output port at address AxxxH for intensity control of both the A10A1A1 LCD Assembly and the A10A2 Keypad Assembly LED backlights. U21 is an eight-bit, high side driver that has binarily weighted resistors in its outputs to be summed to give nine levels of backlight intensity for both the LCD and the keypad, with approximately 30mA maximum LED current. The eight bits of U20/U21 are split to four bits of control for the LCD and Keypad.

3.1.2.4 Port 4 – Audio Path Control Output

The A10A1 Microcontroller U1 uses U14 as a dedicated eight-bit, parallel output port at address BxxxH with U34 as a tri-state impedance buffer, to control the audio routing of the A10A1 Audio/Control PWB Assembly. The audio for both TX and RX must be routed in different ways for Single-channel voice, Digital voice, and Analog Voice scrambler modes of operation. U14/U34 control analog switch ICs U25, U26, U27, and U30 route/mute the audio, as necessary for each mode of operation mentioned earlier. The U34 tri-state buffer is used when in standby, so the audio circuits that are not powered do not load down U14. The routing is defined in the analog switch control matrix diagram on the A10A1 Audio/Control schematic (figure 7, sheet 6).

3.1.2.5 Port 5 – General Purpose Input

The A10A1 Microcontroller U1 uses U31 as a general purpose eight-bit, parallel input port at address CxxxH. The lower 4 (D0–D3) bits of U31 provide a personality code for the A10A1 firmware that is unique to the A10A1 Assembly. The fifth bit (D4) is not used. The upper three bits are used to read A/D converter U36 serial data (D5), to read the external RF PA hop clock pin J6-A with E4 jumpered to E5 (D6), and to monitor the U23 keypad scan the IC data available signal. U36 is a serial eight-bit, A/D converter that is used to monitor both LCD temperature and battery voltage to the main radio. Its serial data is clocked out by output port U35 and read in at U31–7. The monitor of the external RF PA hop clock E4 to E5 is not normally jumpered into U31–8, which is pulled up to 5 V, and has no current use in the front panel firmware. Lastly, the A10A1 firmware periodically reads U31–9 to check for user input activity from the U23 74C923 keypad scan IC.

3.1.2.6 Port 6 – CHANNEL Control Switch Input

The A10A1 Microcontroller U1 uses U10 as an eight-bit parallel input port at address DxxxH. The CHANNEL control switch S1, which is a 10-position rotary switch, has all of its channel outputs (except for the manual channel which floats) pulled to 5 V by SIP resistor R32. U10 monitors the first eight channels from the S1 CHANNEL control switch. If one of these channels is selected, the common of the CHANNEL control switch will ground that input of U10 to produce a low input on that channel. The A10A1 firmware periodically reads the CHANNEL control switch state from U10 to check for channel changes. Channel 9 is read by the FUNCTION control input port discussed below. The manual channel (M), which is the tenth channel on the CHANNEL control switch, is left floating. If the A10A1 Microcontroller reads a high (channel not active) for all nine channels that are connected to the input ports, then by process of elimination, the A10A1 firmware knows that the manual (tenth) channel must be selected.

3.1.2.7 Port 7 – FUNCTION Control Switch Input

The A10A1 Microcontroller U1 uses U11 as an eight-bit, parallel input port at address ExxxH. The FUNCTION control switch S2 is a seven-position rotary switch with a spring-loaded pull to turn in the seventh position (for zeroize). The FUNCTION control switch is dual function; it inputs user function selection for the radio and also provides a hardware power on/off control to the front panel standby power supply. U11 has its input pins pulled up to 5 V by R34, R35, R40, R42, R44, R45, R75, and R32–13 on the anode side of diode array U15. The cathode side of the U15 diode array is pulled up to 24 V by the power on/off signal through diode array U16 on all the FUNCTION positions except the OFF position at S2–1. Any FUNCTION selection other than OFF will ground the power on/off line by the common of the FUNCTION control switch S2–9 through diode array U16, which turns on the front panel standby power supply to provide the 5 V supply for the A10A1 microcomputer. Diode array U15 protects U11 from being driven by +24 V from the hardware on/off function of S2. Simultaneously, whatever function is selected will pull that pin of U11 low through diode array U15. U11 is read periodically by the A10A1 firmware for function changes, also channel 9 from CHANNEL control switch S1 is read by U11.

3.1.2.8 Port 8 – A/D Converter, LCD Heater, 1 kHz Tone Control Output

The A10A1 Microprocessor U1 uses U35 as a four-bit parallel output port at address FxxxH. This output is used to control the U36 TLC548 serial A/D converter, LCD heater, and 1kHz tone generator. U35 provides a clock (U35–4) and chip select (U35–3) to the U36 TLC548 serial A/D converter. The TLC548 has all the circuitry necessary to do A/D conversions internally and when a chip select is brought low, a conversion is initiated. After waiting the conversion time, U35 clocks out the eight-bit A/D converter data. The data out of U36 is read by the general purpose input port U31 described in subsection 3.1.2.5. The A/D converter monitors both the battery voltage and the LCD temperature sensor which are selected by analog switch U33. The battery voltage information is sent to the radio for use in battery status determination, while the LCD temperature sensor is used by the A10A1 firmware to determine when to turn on the LCD heater. U35 is used to turn the LCD heater on and off by Q4. Q4 is an N-channel power MOSFET, which switches the +24 V battery voltage for the LCD heater in the low side of the heater at E9, the high side of the 68 ohm, 2W LCD heater gets +24V at E8. U35 also provides an on/off control for the 1 kHz tone generator at U18C pin 10. U4E, which is a Schmitt trigger input inverter, is used as a gate oscillator with R29 and C32 setting the 1 kHz frequency. U18C can inhibit oscillator operation by pulling U4–11 solidly to 5 V. U35–6 controls the enable of U18 on pin 10. When U18C is enabled, the output is 5 V, which is applied to the input of U4E at pin 11 to set its output to DC value 0 V. When U18C's output is disabled by U35–6, the high impedance of the U18 tri-state output allows the U4E gate oscillator to run. The 1 kHz tone is used as a warning tone if an illegal front panel keypad entry is attempted, and as end of message tones in the digital voice receive mode of operation.

3.2 Front Panel Audio

Figure 4 is the front panel audio flow/control diagram. All audio for the RT-1694 interfaces through the A10A1 Audio/Control PWB Assembly. There are two outside audio interfaces; a handset interface at J1 and line level interface at data connector J2. These two audio interfaces are routed to and from both the A4 Signal Processor and A3 LPC Assembly. Analog switches are used to route the audio for SSB, digital voice, and analog voice security modes of operation. Additionally, a 1 kHz tone, generated on the A10A1 Audio/Control PWB Assembly, is summed into the TX path and gets to the RX path as a TX sidetone (as a warning tone).

3.2.1 Transmit Path

Transmit audio at the line level of 2.2 Vp-p is expected at the data connector J2-B. This input is high impedance at 100K ohms and is wideband with a 10Hz to 10 kHz minimum bandwidth. Transmit audio at a handset level of 3.95 mVp-p is expected at handset connector J1-D. This input has 150 ohm input impedance and has a voice bandwidth of 300Hz to 3 kHz minimum. Line level and handset audio are summed and scaled to a level of 0.91 Vp-p by U32. A 1 kHz tone, generated by U14E, is also summed into the transmit path and scaled to 0.91Vp-p by U32. The transmit audio then simultaneously goes to a firmware-controlled TX audio mute function at U27 and clear transmit sidetone generation at R87. After passing through the transmit mute function of U27, the transmit audio is ready to be delivered to either the A4 Signal Processor Assembly for clear voice transmit or to the A3 LPC Assembly for digital voice and analog voice security transmit. Transmit sidetone is generated by analog switch U26 to switch a transmit audio sample taken by R87 into the receive audio path. Transmit sidetone is designed to be –6dB from the nominal receive audio level of 1.48Vp-p. U26 actually mutes the normal receive audio sources while in the transmit sidetone position.

3.2.2 Receive Path

Receive audio is sourced by either the A4 Signal Processor or the A3 LPC Assembly to the A10A1 Audio/Control Assembly where it is buffered and routed as necessary for clear voice, digital voice, and analog voice security modes of operation. The final destination of the receive audio is to the the handset J1–B and data connector J2–A. The handset output is variable level from 10mVp-p to 10Vp-p into a 1K ohm load with a voice bandwidth of 300Hz to 3 kHz. The data connector output is line level of 2Vp-p and can drive a 600 ohm load at that level with a bandwidth of 10Hz to 10 kHz. Receive audio is expected at a level of 0.77Vp-p from the A3 LPC and 1.48Vp-p from the A4 Signal Processor. Both sources of receive audio are first applied to analog switch U25. For digital voice and clear voice modes, the receive audio passes through U25 and is applied to U28B, which sums both sources and scales them to be 1.48Vp-p.

In analog voice security (AVS), the receive audio is re-routed by analog switch U25. In AVS transmit, transmit audio is routed to the A3 LPC Assembly to be scrambled. Scrambled receive audio from the A3 LPC Assembly is routed by U25 to transmit audio into the A4 Signal Processor. In AVS receive, A4 Signal Processor audio is re-routed to the A3 LPC Assembly, which unscrambles the audio and sends it back to the A10 Front Panel Assembly to be treated as normal LPC receive audio. The analog switch control matrix in figure 4 and the 1A10A1 Audio/Control schematic show the settings necessary to produce this routing.

After the audio passes through U28B of the A10A1 Audio/Control PWB Assembly, it goes to analog switch U26, which is used for receive audio mute when necessary. U26 mutes the receive audio by switching to transmit sidetone audio input for the receive, which should not be present in receive mode of operation. After U26, the receive audio splits to its two destinations; the handset and data connectors. The handset path then passes through the front panel volume control and handset driver op-amp U29B. Before being applied to the handset at pin B, the audio passes through the handset-only mute switch U30. This mute is used to block objectionable transient noise in the handset only in standby mode when the radio is continually turning on and off. The line level output is buffered by U29B and goes directly to the data connector at pin A.

3.3 Power Distribution

Figure 5 is a block diagram of front panel power distribution. The A10 Front Panel Assembly gets 24 V battery power directly from the A7 Power Supply Assembly, but also has its own power supply that always produces the 5 V, +15 V, and –8.5 V to power the A10A1 Audio/Control PWB and A10A1A1 LCD assemblies.

The A10A1 Audio/Control PWB also receives +16.5 V and –12 V from the A7 Power Supply Assembly when it is on. This is necessary for the ALE standby power saving mode of operation. The A10 Front Panel Assembly operates continuously from the A10A1A2 Standby Power Supply which is enabled by the FUNCTION control switch when the radio is turned on by selecting any mode other than OFF. The A10 Front Panel turns the A7 Power Supply Assembly on and off by using the standby/normal control line from the A10A1 Microcomputer U1.

When the front panel power is turned on, it turns on the A7 Power Supply Assembly and, in normal operation, keeps it on. When in ALE standby, however, the front panel turns on the radio periodically to check for valid receive signals.

The A4 Signal Processor Assembly decides whether or not the main radio should stay on. The A4 Signal Processor commands the front panel to either keep the radio on due to valid signals or to turn the radio off and start another standby time period.

The A10A1A1 Standby Power Supply powers only the A10A1 Audio/Control PWB microcomputer U1 and the A10A1A1 LCD Assembly. The LED backlights for both the A10A1A1 LCD and A10A2 Keypad assemblies receive their power from the A7 Power Supply Assembly and do not function while the main radio is off during ALE standby. The audio circuits in the A10A1 Audio/Control PWB Assembly also receives their power form the A7 Power Supply Assembly. The A7 Power Supply 16.5 V and –12 V are diode Ored into the 15 V and –8.5 V outputs of the A10A1A1 Standby Power Supply, so the A7 Power Supply will power the entire A10A1 Audio/Control Assembly for normal radio operation except for 5 V.

3.3.1 A10A1A2 Standby Power Supply Assembly

The A10A1A2 Standby Power Supply receives 24 V from the A10A1 Audio/Control PWB Assembly and provides regulated DC outputs of 5 V, 15 V, and –8.7 V. The 24 V can be anywhere from 18–28 V and is pre-regulated to that level by the A10A1 regulator circuit of Q8, CR15, CR12, and C70 before entering the A10A1A2 Standby Power Supply at J1-3. Diode CR3 provides input polarity protection for the A10A1A2 Standby Power Supply. U1, an LP2951, is a low power, linear-adjustable regulator that puts out +15 VDC at up to 160 mA. U1 output is additionally regulated down to 8.7 VDC by R3 and CR4. U3, an LTC1044, is an inverting charge pump that will produce the negative of whatever voltage is supplied at the V+ input U3–8. U3 receives its power from the 8.7V output from CR4 and produces a –8.7 V at up to 40 mA. The LTC1044 operates at a frequency of 10 kHz and this waveform can be observed at U3–2 or U3–4. U2, a LTC1111, is an integrated, low power buck regulator that produces a regulated DC output of 5 V at up to 50mA. The LTC1111 operates at a frequency of 71.4 kHz and the switch waveform may be observed at U2–4.

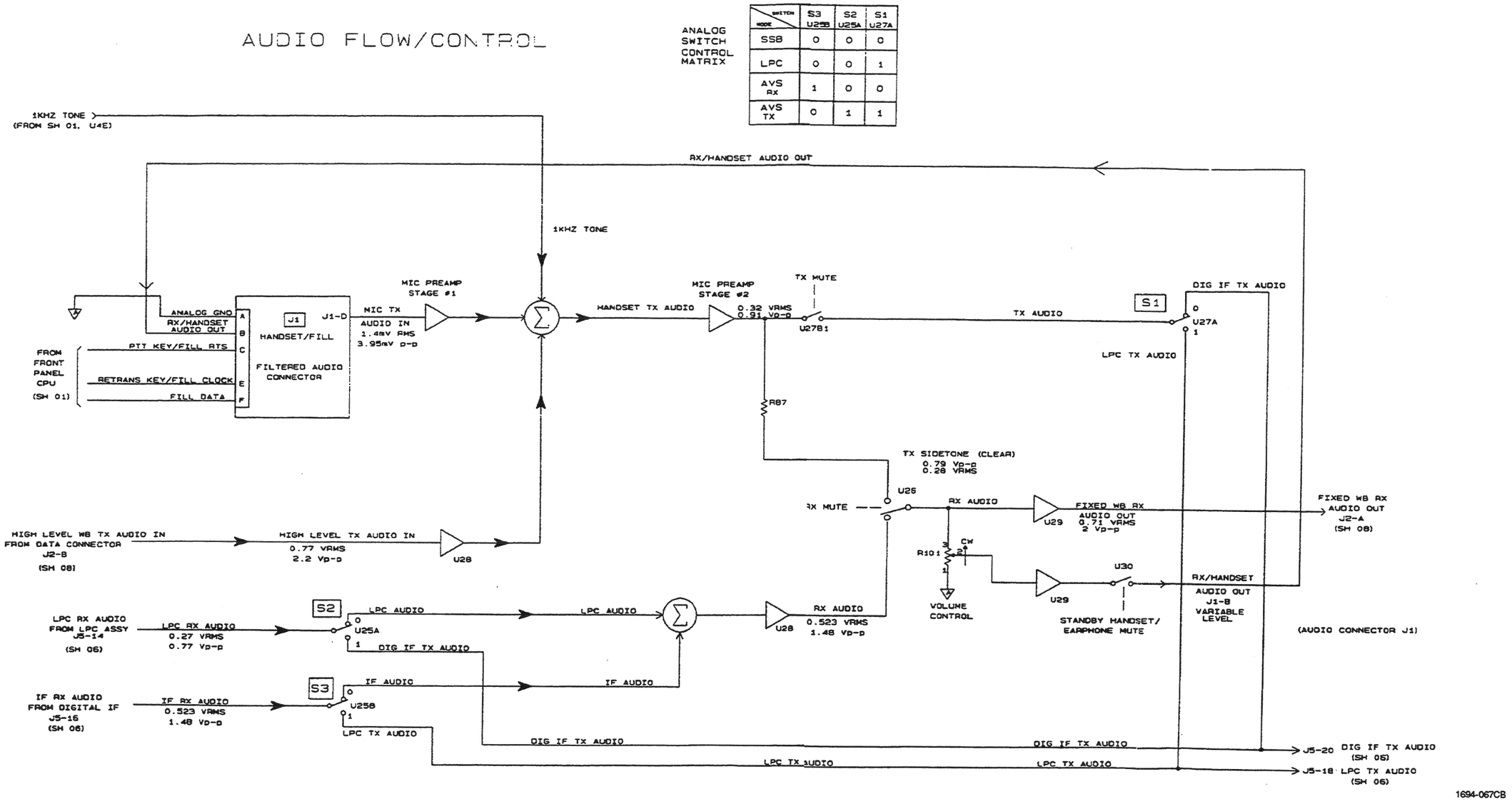


Figure 4. Front Panel Audio Flow/Control Diagram

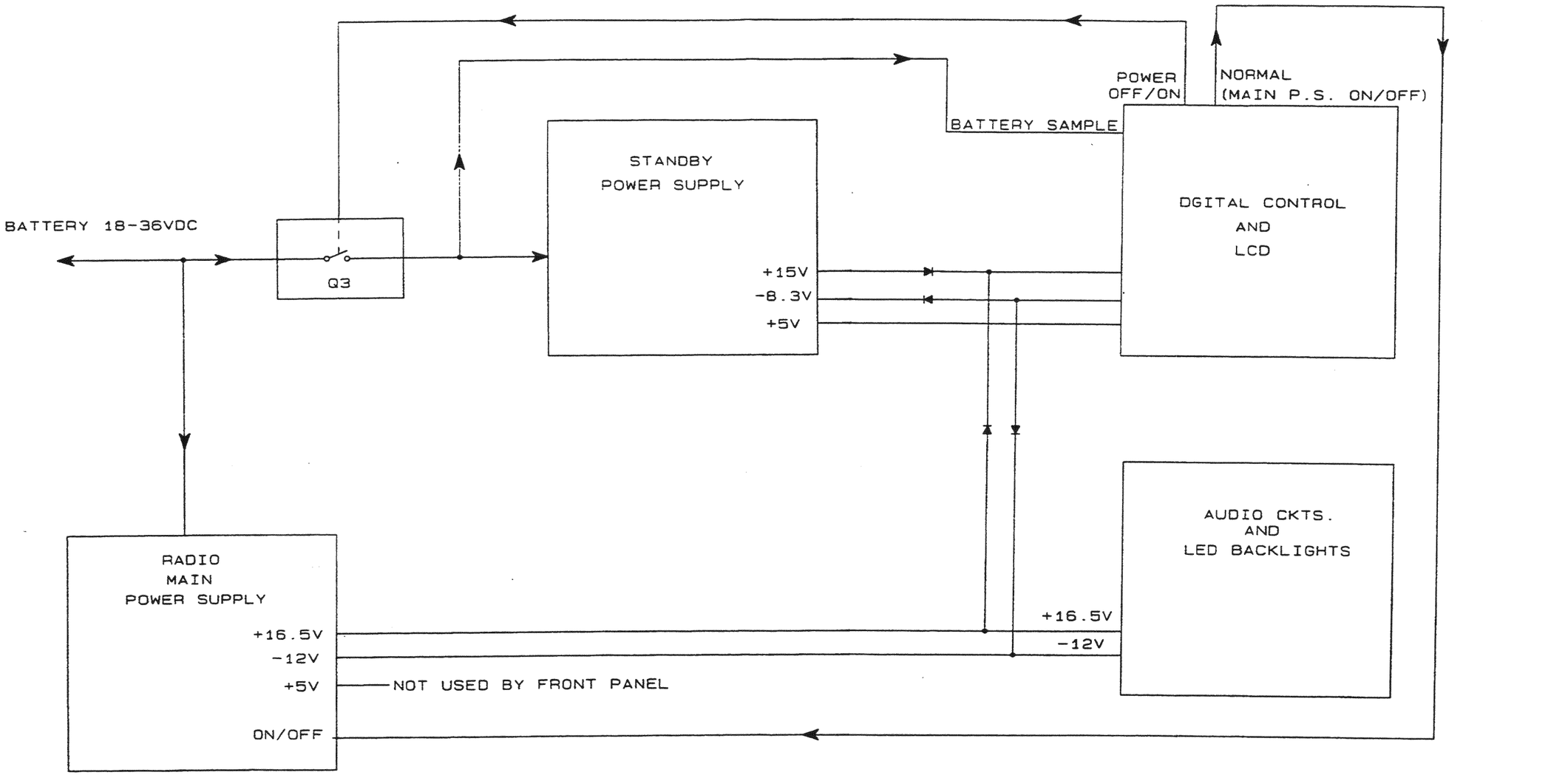


Figure 5. Front Panel Power Distribution Block Diagram

4. TESTING AND ALIGNMENT

There are no test or alignment procedures necessary for the A10 Front Panel Assembly.

5. BITE FAULTS AND TROUBLESHOOTING

Table 7 lists the self-test codes for the A10 Front Panel Assembly. The faults are described in greater detail in the following paragraphs.

Table 7. A10 Front Panel Assembly Self-Test Codes

Code	Fault
02	Internal RAM fault
03	ROM fault
04	External RAM fault
05	The display driver's busy flag is not functional

5.1 Fault 02 – Microprocessor Internal RAM Fault

This fault occurs if the 83C51FA Microprocessor determines that its internal RAM is defective. Replace U1.

5.2 Fault 03 – ROM Fault

This fault occurs if the checksum calculated and recorded in the program ROM during factory programming does not match the checksum calculated by the 83C51FA microprocessor during self-test.

Perform the following test to indicate a ROM fault:

a. Verify that address lines A0 through A7 are properly latched by U3; if not, replace U3.

b. Verify that there are no shorts or opens on address lines A0–A15 to U8.

c. Verify that there are no shorts or opens on AD0–AD7 to U8.

d. Verify logic activity at U8–22 chip select and U8–24 output enable; if not, replace U1.

e. Verify logic activity on bank select logic U7 and U6, also verify activity on U8–3 (A15), U8–2 (A16), and U8-30 (A17).

f. Replace flash EEPROM U8.

5.3 Fault 04 – External RAM Fault

During a check of external RAM U9, one or more bits are detected as being stuck as logic 0s or logic 1s. This may also be the result of open or shorted address, data, or control lines.

Perform the following test to indicate an external RAM fault:

a. Verify that address lines A0 through A7 are properly latched by U3; if not, replace U3.

b. Verify that there are no shorts or opens on address lines A0 through A14.

c. Verify that the U9–20 chip enable is active whenever there is a /RD from U1–18 or a /WR from U1–19. If not, check or replace U1, U17, U2, and U6.

d. Verify activity on the U9 /RD and /WR lines simultaneous with U1 activity on the same lines. If not, check for shorts or opens on the /RD and /WR lines to U9.

e. Replace U9.

5.4 Fault 05 – LCD Fault

An LCD fault indicates that the microprocessor cannot communicate with the Liquid Crystal Display board. Replace the Liquid Crystal Display Assembly (10303-1210).

5.5 Internal Communication Fault

When the message ** Internal Comm Fault ** is displayed on the Front Panel LCD, there are no communications with the radio from the front panel. Perform the following procedure:

a. Verify that the power to the radio is at least 20.5 Vdc. If not, raise the input voltage or change batteries.

b. Cycle power to the radio by turning the FUNCTION control switch to OFF, and then back to SSB.

c. Verify that the normal line at J7–22 is high. If not, troubleshoot that section of front panel circuitry.

d. Verify that the main PS on line on the motherboard at the A7 Power Supply interface at J12–11 is at the battery voltage. If so, then verify that voltages out of the A7 Power Supply are present. Otherwise troubleshoot the A7 Power Supply.

e. Verify activity on the data to and from the front panel for U1 UART. Verify at U1 and U18B, U18C. If not, replace U1 or U18.

f. Troubleshoot the J7 motherboard cable for opens or shorts on the front panel data lines. If not, troubleshoot the A1A1 Interface or A4 Signal Processor Assembly.

6. PARTS LISTS, COMPONENT LOCATION DIAGRAMS, AND SCHEMATIC DIAGRAMS

Table 8 is the parts list for the A10 Front Panel Assembly.

Table 9 is the parts list, figure 6 is the component location diagram, and figure 7 is the schematic diagram for the A10A1 Audio/Control PWB Assembly.

Table 10 is the parts list, figure 8 is the component location diagram, and figure 9 is the schematic diagram for the A10A1A2 Standby Power Supply Assembly.

Table 11 is the parts list, figure 10 is the component location diagram, and figure 11 is the schematic diagram for the A10A2 Keypad Assembly.

Table 8. A10 Front Panel Assembly Parts List (10372-1500-01 Rev. H)

Ref. Desig.	Part Number	Description
--	10372-1505-01	FRONT PANEL
--	10372-1027-01	WINDOW, DISPLAY
--	10181-2017	BEZEL, KEYPAD
--	10243-2021	CASTING, CONTROL KNOB
--	MS16995-9B	SCREW, HSH, 4-40X1/4,BLK
--	10372-1036-01	OVE- AY (CHANNEL)
--	10372-1036-02	OVE- AY (MODE)
--	10372-1058-01	SHIELD, FRONT PANEL
--	P30-0008-000	THD SLNT #262 GRADE O
A1	10303-2100	FRONT PANEL AUDIO/CONTROL
A2	10303-2110-01	PWB ASSY, KEYPAD

Table 9. A10A1 Audio/Control PWB Assembly Parts List (10303-2100 Rev. W)

Ref. Desig.	Part Number	Description
1	10303-2109	PWB, FRONT PANEL REV-A
2	10303-2101	SCHEM, FRONT PANEL AUDIO
3	J46-0114-003	HEADER, 3 PIN
4	J46-0084-314	HEADER 14 POS DUAL ROW
6	10303-1204-207	SCREW, CAPTIVE #2-56X7/16
7	10303-3024	WASHER, FLAT #2 SM
8	MS35338-134	LW SPLT SS #2
9	10303-1203-01	SPACER, CAPTIVE
10	10303-1207-01	INSULATOR, AUDIO CONN
11	10303-1208-01	INSULATOR, DATA CONN
12	E70-0002-005	PAD MNT XSTR TO-18
13	10303-1216-01	STANDOFF, #2-56
14	10303-1219-01	STANDOFF, MF #2-56
16	W20-0001-010	WIRE BUSS #22AWG TIN'D CU
17	H40-0019-001	.010 "THK FIBER WASHER
18	P15-3145-001	SEALER RTV 3145 CLEAR
A1	10372-1210	LCD ASSEMBLY
A2	10303-2250	STANDBY POWER SUPPLY
C1	C36-0016-336	CAP, 33UF 16V TANT
C2	C13-0103-103	CAP .01UF 10% 100V SMD
C3	C13-0105-102	CAP CER 1000PF 5% 100V
C4	C36-0016-106	CAP 10UF 16V SMT
C5	C36-0035-106	CAP TANT 10UF 10% 35V

Table 9. A10A1 Audio/Control PWB Assembly Parts List (10303-2100 Rev. W) (Cont.)

Ref. Desig.	Part Number	Description
C6	C13-0103-103	CAP .01UF 10% 100V SMD
C7	C13-0101-220	CAP 22PF 10% 100V SMD
C8	C13-0101-220	CAP 22PF 10% 100V SMD
C9	C13-0105-102	CAP CER 1000PF 5% 100V
C10	C13-0107-473	CAP .047 UF 250V CER SMC
C11	C13-0107-473	CAP .047 UF 250V CER SMC
C12	C13-0107-473	CAP .047 UF 250V CER SMC
C13	C13-0107-473	CAP .047 UF 250V CER SMC
C14	C36-0016-106	CAP 10UF 16V SMT
C15	C13-0107-473	CAP .047 UF 250V CER SMC
C16	C36-0035-105	CAP 1UF 35V SMT
C17	C13-0107-473	CAP .047 UF 250V CER SMC
C18	C36-0016-475	CAP 4.7UF 10% 16V TANT SM
C19	C13-0107-473	CAP .047 UF 250V CER SMC
C20	C13-0107-473	CAP .047 UF 250V CER SMC
C21	C13-0107-473	CAP .047 UF 250V CER SMC
C22	C13-0107-473	CAP .047 UF 250V CER SMC
C23	C36-0016-475	CAP 4.7UF 10% 16V TANT SM
C24	C36-0025-474	CAP .47UF 10% 25V TANT
C25	C13-0107-473	CAP .047 UF 250V CER SMC
C26	C13-0105-102	CAP CER 1000PF 5% 100V
C27	C13-0107-473	CAP .047 UF 250V CER SMC
C28	C13-0103-103	CAP .01UF 10% 100V SMD
C29	C13-0107-473	CAP .047 UF 250V CER SMC
C30	C13-0107-473	CAP .047 UF 250V CER SMC
C31	C36-0016-475	CAP 4.7UF 10% 16V TANT SM
C32	C13-0107-473	CAP .047 UF 250V CER SMC
C33	C13-0107-473	CAP .047 UF 250V CER SMC
C34	C13-0107-473	CAP .047 UF 250V CER SMC
C35	C13-0107-473	CAP .047 UF 250V CER SMC
C36	C13-0107-473	CAP .047 UF 250V CER SMC
C37	C36-0050-475	CAP 4.7UF 10% 50V TANT SM
C38	C13-0107-473	CAP .047 UF 250V CER SMC
C39	C13-0107-104	CAP, .1UF 10% 100V CER
C40	C36-0016-106	CAP 10UF 16V SMT
C41	C13-0107-473	CAP .047 UF 250V CER SMC
C42	C13-0107-104	CAP, .1UF 10% 100V CER
C43	C13-0107-104	CAP, .1UF 10% 100V CER
C44	C36-0016-336	CAP, 33UF 16V TANT

Table 9. A10A1 Audio/Control PWB Assembly Parts List (10303-2100 Rev. W) (Cont.)

Ref. Desig.	Part Number	Description
C45	C36-0035-106	CAP TANT 10UF 10% 35V
C46	C36-0035-106	CAP TANT 10UF 10% 35V
C47	C36-0035-106	CAP TANT 10UF 10% 35V
C48	C36-0035-106	CAP TANT 10UF 10% 35V
C49	C36-0016-106	CAP 10UF 16V SMT
C50	C13-0107-104	CAP, .1UF 10% 100V CER
C51	C13-0103-103	CAP .01UF 10% 100V SMD
C52	C13-0103-103	CAP .01UF 10% 100V SMD
C53	C13-0107-473	CAP .047 UF 250V CER SMC
C54	C36-0035-105	CAP 1UF 35V SMT
C55	C13-0107-473	CAP .047 UF 250V CER SMC
C56	C13-0103-103	CAP .01UF 10% 100V SMD
C57	C13-0107-473	CAP .047 UF 250V CER SMC
C58	C13-0105-102	CAP CER 1000PF 5% 100V
C59	C13-0103-333	CAP .033UF 10% 100V SMD
C60	C13-0105-102	CAP CER 1000PF 5% 100V
C61	C13-0105-102	CAP CER 1000PF 5% 100V
C62	C13-0103-103	CAP .01UF 10% 100V SMD
C63	C13-0107-473	CAP .047 UF 250V CER SMC
C64	C13-0107-473	CAP .047 UF 250V CER SMC
C65	C13-0107-473	CAP .047 UF 250V CER SMC
C66	C36-0035-105	CAP 1UF 35V SMT
C67	C36-0035-105	CAP 1UF 35V SMT
C68	C36-0035-105	CAP 1UF 35V SMT
C69	C13-0103-103	CAP .01UF 10% 100V SMD
C70	C36-0050-475	CAP 4.7UF 10% 50V TANT SM
C72	C13-0103-333	CAP .033UF 10% 100V SMD
C73	C13-0103-333	CAP .033UF 10% 100V SMD
C76	C13-0107-473	CAP .047 UF 250V CER SMC
C77	C13-0107-473	CAP .047 UF 250V CER SMC
C78	C13-0101-470	CAP 47PF 10% 50V CER
C81	C13-0107-473	CAP .047 UF 250V CER SMC
C82	C13-0107-473	CAP .047 UF 250V CER SMC
C83	C36-0035-105	CAP 1UF 35V SMT
C84	C36-0035-105	CAP 1UF 35V SMT
C85	C36-0035-105	CAP 1UF 35V SMT
C86	C36-0035-105	CAP 1UF 35V SMT
C87	C13-0107-473	CAP .047 UF 250V CER SMC
C88	C36-0020-226	CAP, 22UF, 20V

Table 9. A10A1 Audio/Control PWB Assembly Parts List (10303-2100 Rev. W) (Cont.)

Ref. Desig.	Part Number	Description
C91	C13-0101-100	CAP 10PF 10% 100V SMD
C92	C13-0107-473	CAP .047 UF 250V CER SMC
C93	C13-0107-473	CAP .047 UF 250V CER SMC
C94	C13-0107-473	CAP .047 UF 250V CER SMC
C96	C13-0107-473	CAP .047 UF 250V CER SMC
C97	C13-0105-102	CAP CER 1000PF 5% 100V
C98	C13-0107-473	CAP .047 UF 250V CER SMC
C100	C14-0000-225	CAP 2.2UF MLC
C101	C13-0103-103	CAP .01UF 10% 100V SMD
C103	C13-0105-102	CAP CER 1000PF 5% 100V
C104	C36-0016-335	CAP 3.3UF 16V TANT SMD
C105	C13-0105-102	CAP CER 1000PF 5% 100V
C106	C13-0107-473	CAP .047 UF 250V CER SMC
C107	C13-0107-473	CAP .047 UF 250V CER SMC
C108	C13-0107-473	CAP .047 UF 250V CER SMC
C109	C13-0101-150	CAP 15PF 10% 100V SMD
C110	C13-0101-121	CAP 120PF 10% 100V SMD
C111	C13-0107-473	CAP .047 UF 250V CER SMC
C112	C36-0020-225	CAP, 2.2UF, 20V
C113	C13-0107-473	CAP .047 UF 250V CER SMC
C114	C13-0107-473	CAP .047 UF 250V CER SMC
C115	C13-0105-102	CAP CER 1000PF 5% 100V
C116	C13-0105-102	CAP CER 1000PF 5% 100V
C117	C13-0107-473	CAP .047 UF 250V CER SMC
C118	C13-0107-473	CAP .047 UF 250V CER SMC
C119	C13-0107-473	CAP .047 UF 250V CER SMC
C120	C13-0105-102	CAP CER 1000PF 5% 100V
C121	C13-0105-102	CAP CER 1000PF 5% 100V
C122	C13-0105-102	CAP CER 1000PF 5% 100V
C123	C13-0105-102	CAP CER 1000PF 5% 100V
CR1	D20-0005-001	DIODE, SOT-23
CR2	D20-0005-001	DIODE, SOT-23
CR3	D15-0914-101	DIODE HI-SPD SWITCHING
CR4	D15-0914-101	DIODE HI-SPD SWITCHING
CR5	D20-0005-004	DIODE, DUAL HSMS-2803
CR6	D15-0914-101	DIODE HI-SPD SWITCHING
CR7	D20-0005-003	DIODE SCHOTTKY HSMS2802
CR8	D20-0005-001	DIODE, SOT-23
CR9	D15-0914-101	DIODE HI-SPD SWITCHING

Table 9. A10A1 Audio/Control PWB Assembly Parts List (10303-2100 Rev. W) (Cont.)

Ref. Desig.	Part Number	Description
CR10	D15-0914-101	DIODE HI-SPD SWITCHING
CR11	D20-0005-005	DIODE, SOT-23, HSMS-2804
CR12	1N5290	DIODE, CURRENT
CR13	D15-0914-101	DIODE HI-SPD SWITCHING
CR14	D15-0914-101	DIODE HI-SPD SWITCHING
CR15	D05-0005-030	DIODE, MMBZ5255,ZENER
J1	J69-0005-002	6 PIN AUDIO CONNECTOR
J2	10372-1200-01	CONNECTOR, DATA, 14 PIN
J5	J46-0054-020	HEADER 20 PIN
J6	J09-0016-001	CONNECTOR, PA, 10 PIN
J7	J46-0054-034	HEADER 34 PIN
L1	L45-0008-012	INDUCTOR, 100 UH SMT
L2	L45-0008-012	INDUCTOR, 100 UH SMT
L4	10303-3113-01	TOROID, 130UH
L5	L45-0005-472	INDUCTOR CHIP 4.7 UH
L6	L45-0008-001	INDUCTOR, 12UH, SMT
L7	L45-0008-001	INDUCTOR, 12UH, SMT
L10	L45-0008-012	INDUCTOR, 100 UH SMT
L11	L45-0008-012	INDUCTOR, 100 UH SMT
L12	L45-0008-012	INDUCTOR, 100 UH SMT
L13	L45-0008-012	INDUCTOR, 100 UH SMT
L14	L45-0008-012	INDUCTOR, 100 UH SMT
L15	L45-0008-001	INDUCTOR, 12UH, SMT
P4	J46-0088-111	CONNECTOR, 68685-311
Q1	Q02-2907-101	XSTR SS/GP PNP MMBT2907A
Q2	Q12-2222-101	XSTR NPN SWG SM SS/GP
Q3	Q02-2907-101	XSTR SS/GP PNP MMBT2907A
Q4	Q26-0021-001	FET, MTD6N10-1
Q5	Q02-2907-101	XSTR SS/GP PNP MMBT2907A
Q6	Q12-2222-101	XSTR NPN SWG SM SS/GP
Q7	Q02-2907-101	XSTR SS/GP PNP MMBT2907A
Q8	Q50-0019-001	XSTR, DARLINGTON
Q9	Q12-2222-101	XSTR NPN SWG SM SS/GP
R1	R85-0004-334	RES 22.1K 1% 1/8W FLM
R2	R85-0004-201	RES 1000 1% 1/8W FLM
R3	R85-0004-334	RES 22.1K 1% 1/8W FLM
R4	R85-0004-334	RES 22.1K 1% 1/8W FLM
R5	R85-0004-266	RES,4.75K 1% 1/8W CHIP
R6	R85-0004-201	RES 1000 1% 1/8W FLM

Table 9. A10A1 Audio/Control PWB Assembly Parts List (10303-2100 Rev. W) (Cont.)

Ref. Desig.	Part Number	Description
R7	R85-0004-201	RES 1000 1% 1/8W FLM
R8	R85-0004-334	RES 22.1K 1% 1/8W FLM
R9	R85-0004-101	RES 100 1% 1/8W FLM
R10	R85-0004-000	RES ZERO OHM 1/8W FILM
R11	R85-0004-334	RES 22.1K 1% 1/8W FLM
R12	R85-0004-101	RES 100 1% 1/8W FLM
R13	R85-0004-334	RES 22.1K 1% 1/8W FLM
R14	R85-0004-334	RES 22.1K 1% 1/8W FLM
R15	R85-0004-009	RES, CHIP 12.1 1/8 W 1%
R16	R85-0004-334	RES 22.1K 1% 1/8W FLM
R17	R85-0004-401	RES 100K 1% 1/8W FLM
R18	R85-0004-251	RES 3320 1% 1/8W
R19	R85-0004-301	RES 10K 1% 1/8W FLM
R20	R85-0004-201	RES 1000 1% 1/8W FLM
R21	R85-0004-301	RES 10K 1% 1/8W FLM
R22	R85-0004-366	RES 47.5K 1% 1/8W FLM
R23	R85-0004-366	RES 47.5K 1% 1/8W FLM
R24	R85-0004-201	RES 1000 1% 1/8W FLM
R25	R85-0004-301	RES 10K 1% 1/8W FLM
R26	R85-0004-101	RES 100 1% 1/8W FLM
R27	R85-0004-251	RES 3320 1% 1/8W
R28	R85-0004-401	RES 100K 1% 1/8W FLM
R29	R85-0004-343	RES 27.4K 1% 1/8W FLM
R31	R85-0004-366	RES 47.5K 1% 1/8W FLM
R32	R41-0005-473	RES, SIP, SMT, 47K BOURNS
R33	R85-0004-101	RES 100 1% 1/8W FLM
R34	R85-0004-366	RES 47.5K 1% 1/8W FLM
R35	R85-0004-366	RES 47.5K 1% 1/8W FLM
R36	R85-0004-401	RES 100K 1% 1/8W FLM
R37	R85-0004-366	RES 47.5K 1% 1/8W FLM
R38	R85-0004-334	RES 22.1K 1% 1/8W FLM
R39	R85-0004-266	RES,4.75K 1% 1/8W CHIP
R40	R85-0004-366	RES 47.5K 1% 1/8W FLM
R41	R85-0004-334	RES 22.1K 1% 1/8W FLM
R42	R85-0004-366	RES 47.5K 1% 1/8W FLM
R43	R85-0004-201	RES 1000 1% 1/8W FLM
R44	R85-0004-366	RES 47.5K 1% 1/8W FLM
R45	R85-0004-366	RES 47.5K 1% 1/8W FLM
R46	R85-0004-343	RES 27.4K 1% 1/8W FLM

Table 9. A10A1 Audio/Control PWB Assembly Parts List (10303-2100 Rev. W) (Cont.)

Ref. Desig.	Part Number	Description
R47	R85-0004-301	RES 10K 1% 1/8W FLM
R48	R41-0005-473	RES, SIP, SMT, 47K BOURNS
R49	R85-0004-166	RES 475 1% 1/8W SMD
R50	R85-0004-222	RES, CHIP 1650 1/8 W 1%
R51	R85-0004-447	RES 301K 1% 1/8W FILM
R52	R85-0004-447	RES 301K 1% 1/8W FILM
R53	R85-0004-447	RES 301K 1% 1/8W FILM
R54	R85-0004-447	RES 301K 1% 1/8W FILM
R55	R85-0004-293	RES 9090 1% 1/8W FLM
R56	R85-0004-324	RES 17.4K 1% 1/8W
R57	R85-0004-189	RES 825 1% 1/8W FLM
R58	R85-0004-401	RES 100K 1% 1/8W FLM
R59	R85-0004-322	RES 16.5K 1% 1/8W FILM
R60	R85-0004-366	RES 47.5K 1% 1/8W FLM
R61	R85-0004-330	RES 20.0K 1% 1/8W FLM
R62	R85-0004-330	RES 20.0K 1% 1/8W FLM
R63	R85-0004-189	RES 825 1% 1/8W FLM
R64	R85-0004-160	RES, CHIP 412 1/8 W 1%
R65	R85-0004-249	RES 3160 1% 1/8W FLM
R66	R85-0004-220	RES 1580 1% 1/8W FLM
R67	R85-0004-187	RES, CHIP 787 1/8 W 1%
R68	R85-0004-146	RES, CHIP 294 1/8 W 1%
R69	R85-0004-201	RES 1000 1% 1/8W FLM
R70	R85-0004-101	RES 100 1% 1/8W FLM
R71	R85-0004-166	RES 475 1% 1/8W SMD
R72	R85-0004-166	RES 475 1% 1/8W SMD
R73	R85-0004-466	RES 475K 1% 1/8W CHIP
R74	R85-0004-466	RES 475K 1% 1/8W CHIP
R75	R85-0004-366	RES 47.5K 1% 1/8W FLM
R76	R85-0004-251	RES 3320 1% 1/8W
R77	R85-0004-301	RES 10K 1% 1/8W FLM
R78	R85-0004-366	RES 47.5K 1% 1/8W FLM
R79	R85-0004-166	RES 475 1% 1/8W SMD
R80	R85-0004-301	RES 10K 1% 1/8W FLM
R81	R85-0004-466	RES 475K 1% 1/8W CHIP
R82	R85-0004-466	RES 475K 1% 1/8W CHIP
R83	R85-0004-466	RES 475K 1% 1/8W CHIP
R84	R85-0004-369	RES 51.1K 1% 1/8W FLM
R85	R85-0004-401	RES 100K 1% 1/8W FLM

Table 9. A10A1 Audio/Control PWB Assembly Parts List (10303-2100 Rev. W) (Cont.)

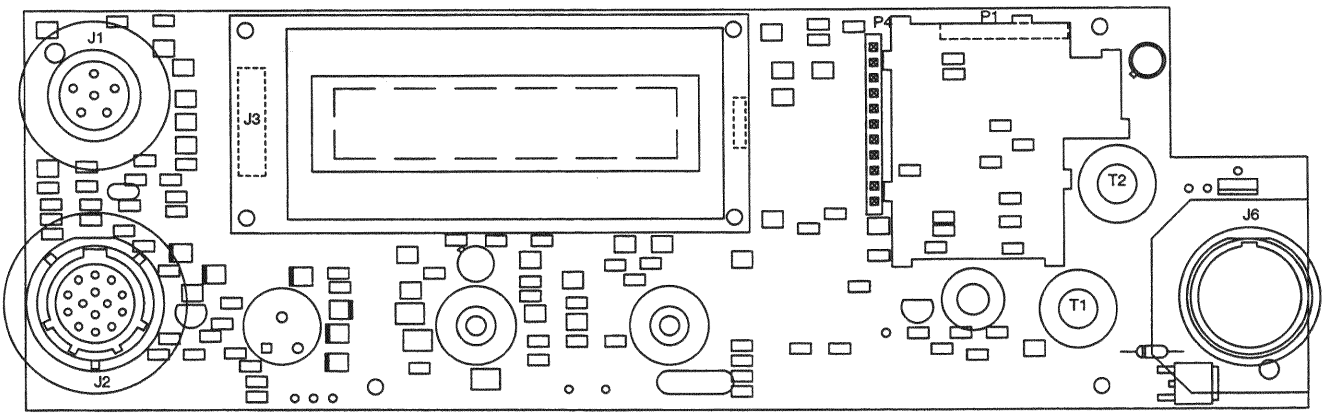
Ref. Desig.	Part Number	Description
R86	R85-0004-401	RES 100K 1% 1/8W FLM
R87	R85-0004-218	RES 1500 1% 1/8W FLM
R88	R85-0004-101	RES 100 1% 1/8W FLM
R89	R85-0004-251	RES 3320 1% 1/8W
R90	R85-0004-334	RES 22.1K 1% 1/8W FLM
R91	R85-0004-258	RES 3920 1% 1/8W FLM
R92	R85-0004-101	RES 100 1% 1/8W FLM
R93	R85-0004-101	RES 100 1% 1/8W FLM
R94	R85-0004-251	RES 3320 1% 1/8W
R95	R85-0004-401	RES 100K 1% 1/8W FLM
R96	R85-0004-384	RES FILM 73.2K 1% 1/8 SMD
R97	R85-0004-401	RES 100K 1% 1/8W FLM
R98	R85-0004-366	RES 47.5K 1% 1/8W FLM
R99	R85-0004-366	RES 47.5K 1% 1/8W FLM
R100	R85-0004-251	RES 3320 1% 1/8W
R101	R21-0009-103	RES, POT, 10K
R102	R85-0004-358	RES 39.2K 1% 1/8W FLM
R103	R85-0004-466	RES 475K 1% 1/8W CHIP
R104	R85-0004-134	RES 221 1% 1/8W FLM
R106	R85-0004-366	RES 47.5K 1% 1/8W FLM
R107	R85-0004-101	RES 100 1% 1/8W FLM
R109	R85-0004-066	RES 47.5 1% 1/8W FLM
R110	R85-0004-101	RES 100 1% 1/8W FLM
R111	R85-0004-101	RES 100 1% 1/8W FLM
R112	R85-0004-366	RES 47.5K 1% 1/8W FLM
R113	R85-0004-366	RES 47.5K 1% 1/8W FLM
R114	R85-0004-401	RES 100K 1% 1/8W FLM
R115	R85-0004-066	RES 47.5 1% 1/8W FLM
R116	R85-0004-101	RES 100 1% 1/8W FLM
R119	R85-0004-101	RES 100 1% 1/8W FLM
R125	R85-0004-101	RES 100 1% 1/8W FLM
R126	R85-0004-201	RES 1000 1% 1/8W FLM
R127	R85-0004-401	RES 100K 1% 1/8W FLM
R128	R85-0004-359	RES 40.2K 1% 1/8W FLM
R129	R85-0004-001	RES, 10 1% 1/8W CHIP

Table 9. A10A1 Audio/Control PWB Assembly Parts List (10303-2100 Rev. W) (Cont.)

Ref. Desig.	Part Number	Description
R130	R85-0004-266	RES,4.75K 1% 1/8W CHIP
R131	R85-0004-118	RES 150 1% 1/8 WATT
R132	R85-0004-366	RES 47.5K 1% 1/8W FLM
R133	R85-0004-466	RES 475K 1% 1/8W CHIP
R134	R85-0004-262	RES 4320 1% 1/8W FLM
R135	R85-0004-443	RES, 274K 1% 1/8W CHIP
R136	R85-0004-401	RES 100K 1% 1/8W FLM
R137	R85-0004-401	RES 100K 1% 1/8W FLM
R138	R85-0004-101	RES 100 1% 1/8W FLM
R139	R85-0004-101	RES 100 1% 1/8W FLM
R141	R85-0004-366	RES 47.5K 1% 1/8W FLM
R142	R85-0004-366	RES 47.5K 1% 1/8W FLM
R143	R85-0004-101	RES 100 1% 1/8W FLM
R144	R85-0004-301	RES 10K 1% 1/8W FLM
S1	S27-0014-010	SWITCH, 10 POS ROTARY
S2	10243-7602	SW RTRY 7 POS
T1	10385-1127	CHOKE,COMMON-MODE
T2	10385-1127	CHOKE,COMMON-MODE
U1	10181-8017	PROG. TN 83C51FA PLCC MIC
U2	10372-7414	IC, 74HC14 SMT
U3	I01-5000-573	8-BIT LATCH (74HC573DW)
U4	10372-7414	IC, 74HC14 SMT
U5	I12-0016-001	REG, LOW PWR 12V
U6	I01-5000-000	QUAD NAND-GATE (74HC00D)
U7	I01-5000-000	QUAD NAND-GATE (74HC00D)
U8	I25-0042-005	IC, 256K X 8 FLASH MEMORY
U9	I26-0021-012	IC RAM HM62256LFPI-15T
U10	I01-5000-573	8-BIT LATCH (74HC573DW)
U11	I01-5000-573	8-BIT LATCH (74HC573DW)
U12	I01-5000-138	3 TO 8 DECODER (74HC138D)
U13	I30-0048-003	IC, LP DUAL OP AMP (MC331
U14	I01-5000-574	8-BIT D-FF (74HC574DW)
U15	I91-0003-001	IC, DIODE ARRAY, MMAD1109
U16	I91-0003-001	IC, DIODE ARRAY, MMAD1109
U17	I14-0013-116	IC, SUPERVISORY IC, SO-1
U18	I01-5000-125	QUAD TRI-STATE (74HC125D)
U19	I10-0018-001	MICRO REG LP2950ACZ-5.0
U20	I01-5000-574	8-BIT D-FF (74HC574DW)
U21	I08-0011-005	IC, HIGH SIDE DRIVER SMT

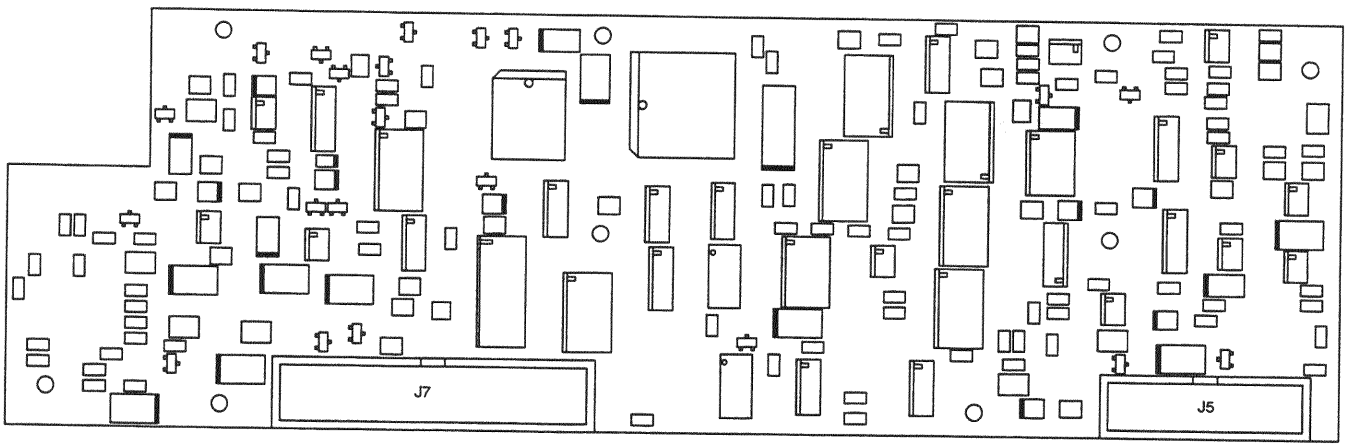
Table 9. A10A1 Audio/Control PWB Assembly Parts List (10303-2100 Rev. W) (Cont.)

Ref. Desig.	Part Number	Description
U22	I10-0018-001	MICRO REG LP2950ACZ-5.0
U23	I36-0005-003	IC, ENCODER,MM74C923WM
U24	I12-0016-001	REG, LOW PWR 12V
U25	I06-0013-101	DUAL SPDT SWITCH DG403AB
U26	I06-0014-101	IC, SPDT SWITCH DG419ABW
U27	I06-0013-101	DUAL SPDT SWITCH DG403AB
U28	I30-0048-003	IC, LP DUAL OP AMP (MC331
U29	I30-0048-003	IC, LP DUAL OP AMP (MC331
U30	I06-0014-002	IC, ANALOG SW, DG418DY
U31	I01-5000-573	8-BIT LATCH (74HC573DW)
U32	I30-0048-003	IC, LP DUAL OP AMP (MC331
U33	I06-0014-101	IC, SPDT SWITCH DG419ABW
U34	I01-5000-367	BUS DRIVER, HEX (74HC367)
U35	I01-5000-173	IC,QUAD TRI-STATE FF
U36	I03-0020-101	8-BIT SERIAL ADC TLC548I
U37	Q34-0000-001	XSTR DUAL MOSFET 9953
VR2	I14-0003-004	LM136H-2.5 VOLTAGE REF.
Y1	Y15-0004-946	XTAL, 9.216 MHZ,MA-506
Z1	D41-0002-025	PTC CIRCUIT PROT .25A 60V



TOP SIDE SHOWN

Figure 6. A10A1 Audio/Control Assembly Component Location Diagram (10303-2100 Rev. H) (Sheet 1 of 2)



BOTTOM SIDE SHOWN

10303-2100
SHEET2 OF 2

Figure 6. A10A1 Audio/Control Assembly Component Location Diagram (10303-2100 Rev. H) (Sheet 2 of 2)

NOTE: UNLESS OTHERWISE SPECIFIED:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR A COMPLETE DESIGNATION, PREFIX WITH UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.
2. ALL RESISTOR VALUES ARE IN OHMS, 1/8W, +/-1%.
3. ALL CAPACITOR VALUES ARE IN MICROFARADS.
4. VENDOR PART NO. CALLOUTS ARE FOR REFERENCE ONLY. COMPONENTS ARE SUPPLIED PER PART NO. IN PARTS LIST.
5. BACKSLASH (/) DENOTES ACTIVE LOW.

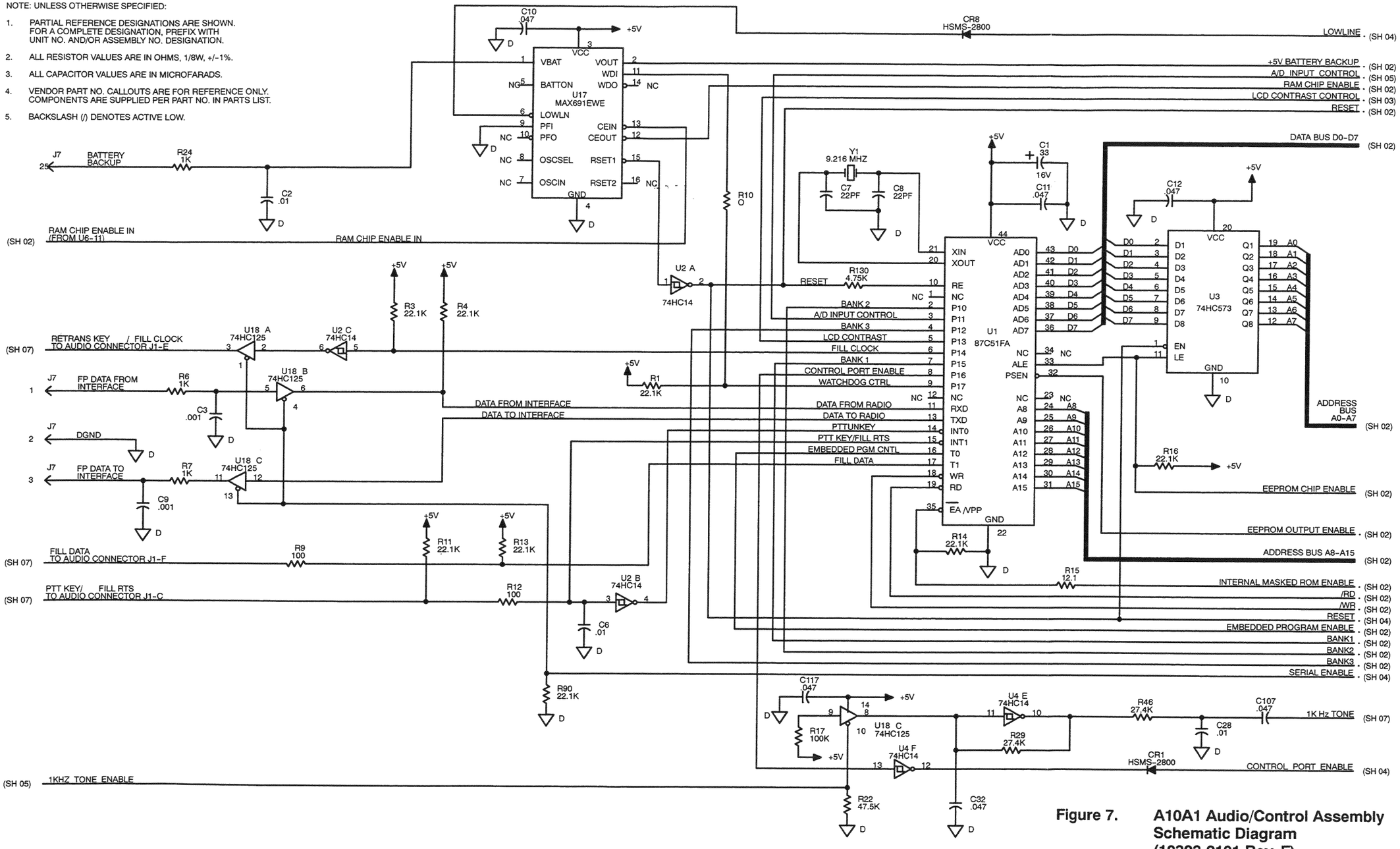


Figure 7. A10A1 Audio/Control Assembly Schematic Diagram (10303-2101 Rev. F) (Sheet 1 of 9)

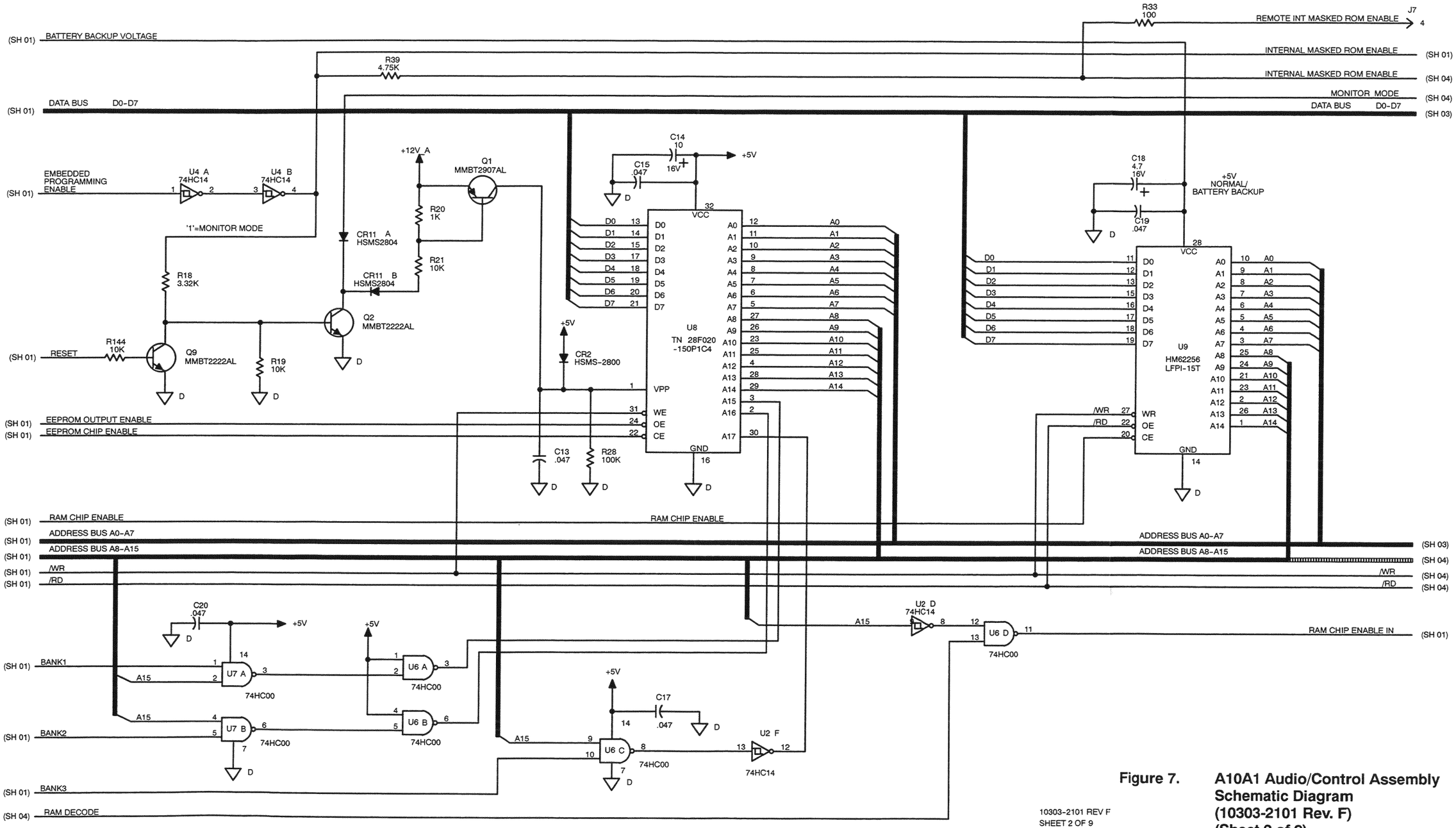
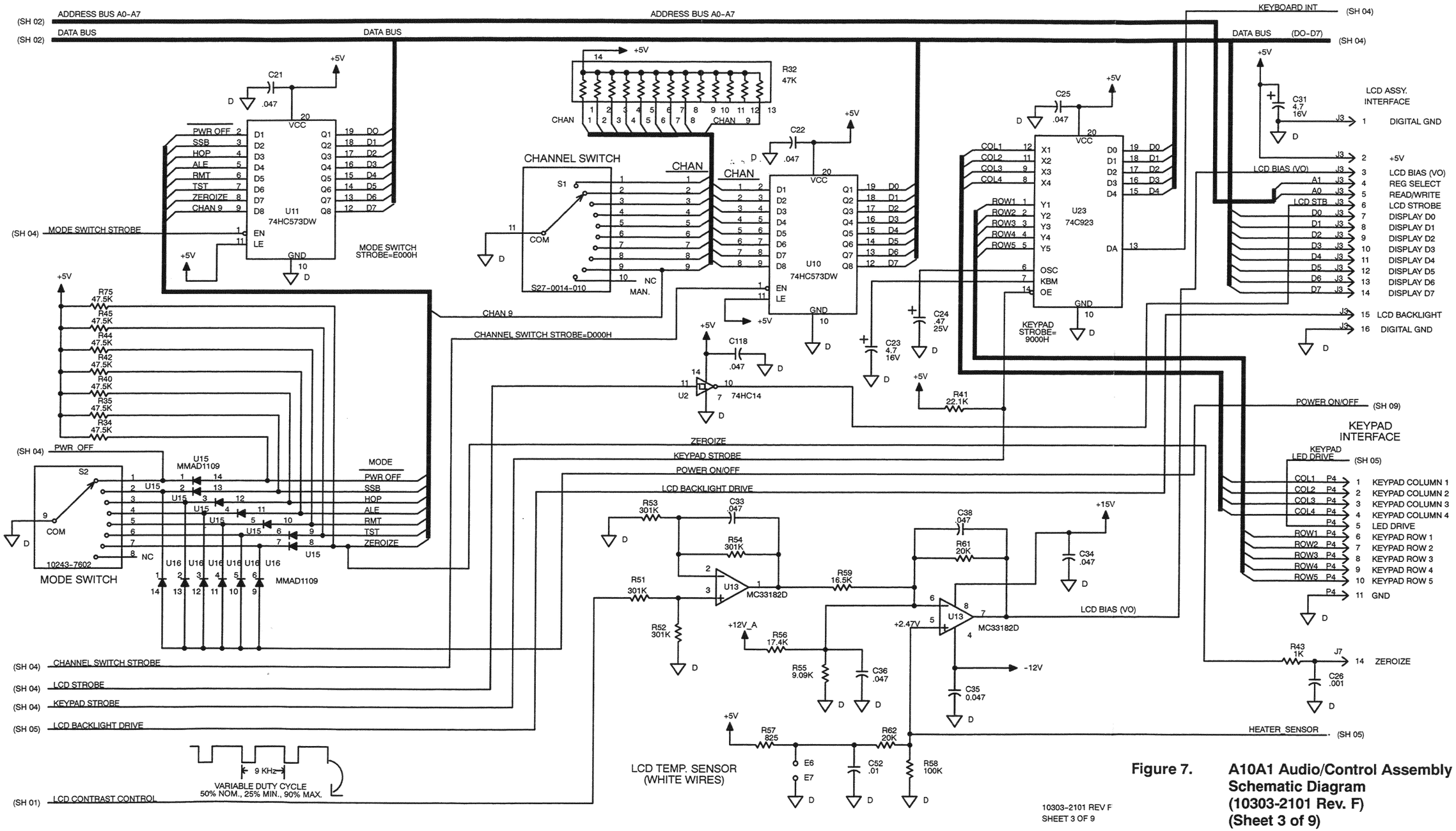


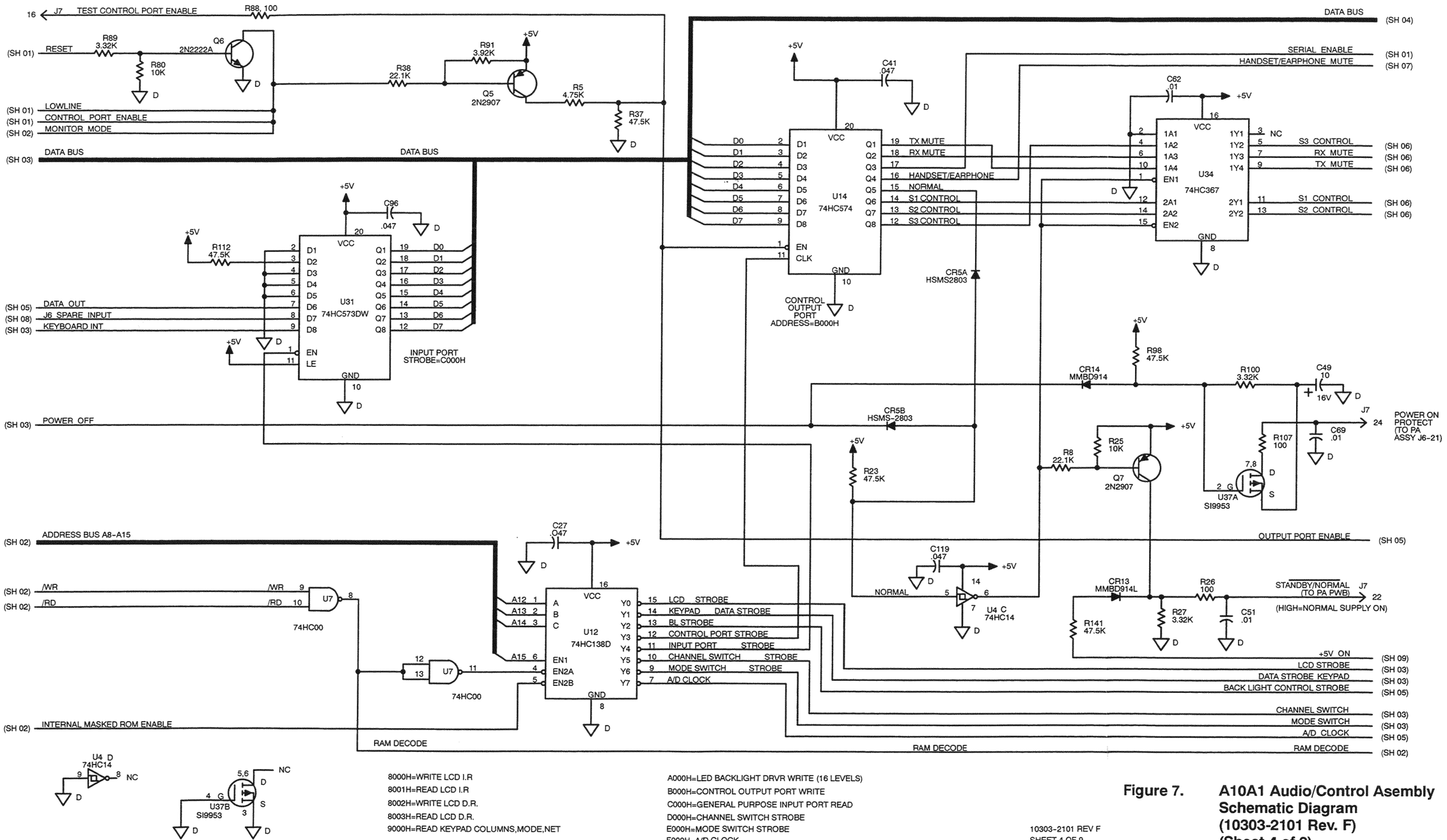
Figure 7. **A10A1 Audio/Control Assembly Schematic Diagram (10303-2101 Rev. F) (Sheet 2 of 9)**

10303-2101 REV F
SHEET 2 OF 9



10303-2101 REV F
SHEET 3 OF 9

Figure 7. A10A1 Audio/Control Assembly Schematic Diagram (10303-2101 Rev. F) (Sheet 3 of 9)



10303-2101 REV F
SHEET 4 OF 9

Figure 7. A10A1 Audio/Control Asembly Schematic Diagram (10303-2101 Rev. F) (Sheet 4 of 9)

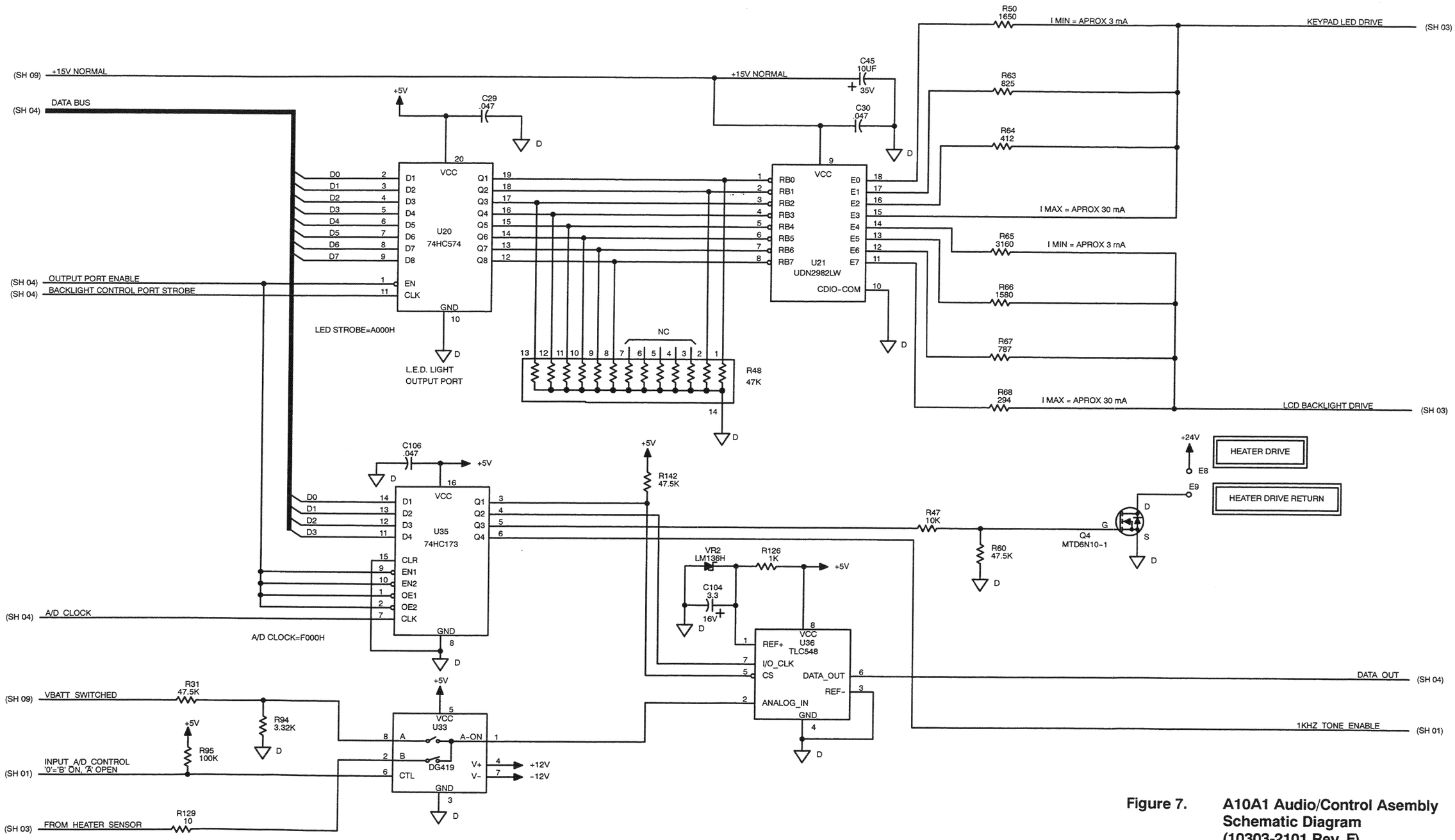
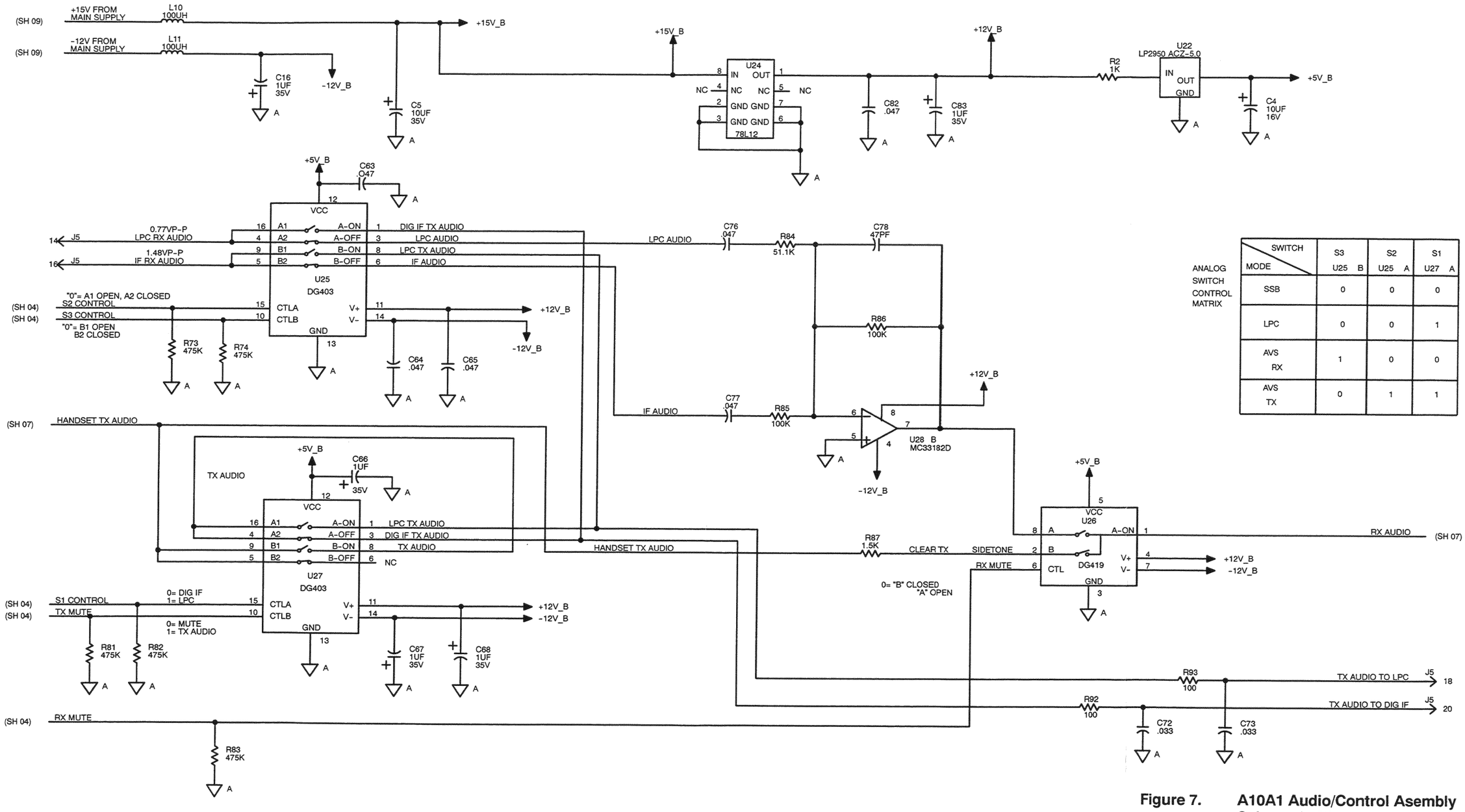


Figure 7. **A10A1 Audio/Control Asembly Schematic Diagram (10303-2101 Rev. F) (Sheet 5 of 9)**

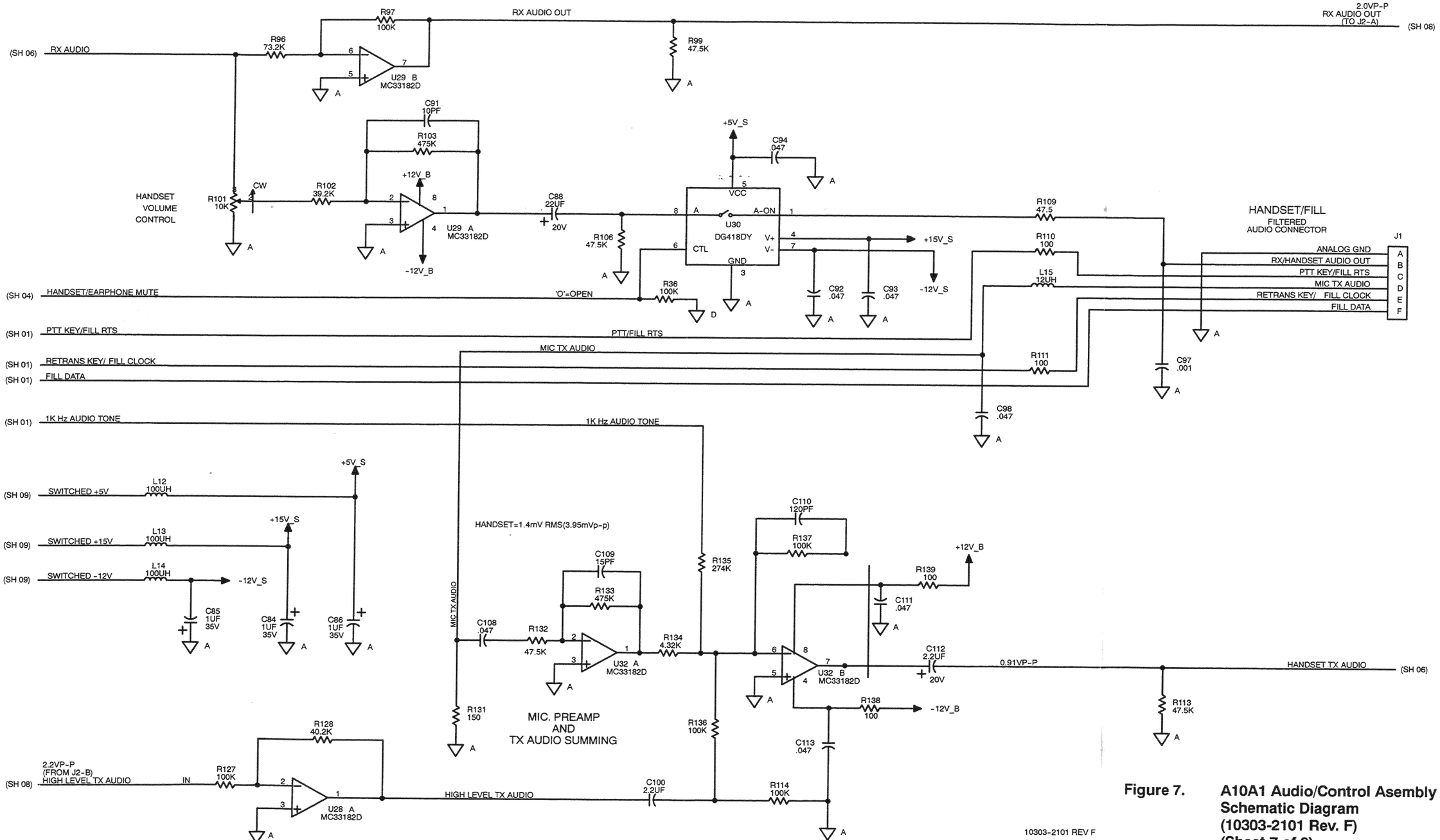
10303-2101 REV F
SHEET 5 OF 9



ANALOG SWITCH CONTROL MATRIX	SWITCH / MODE	S3 U25 B	S2 U25 A	S1 U27 A
	SSB	0	0	0
	LPC	0	0	1
	AVS RX	1	0	0
	AVS TX	0	1	1

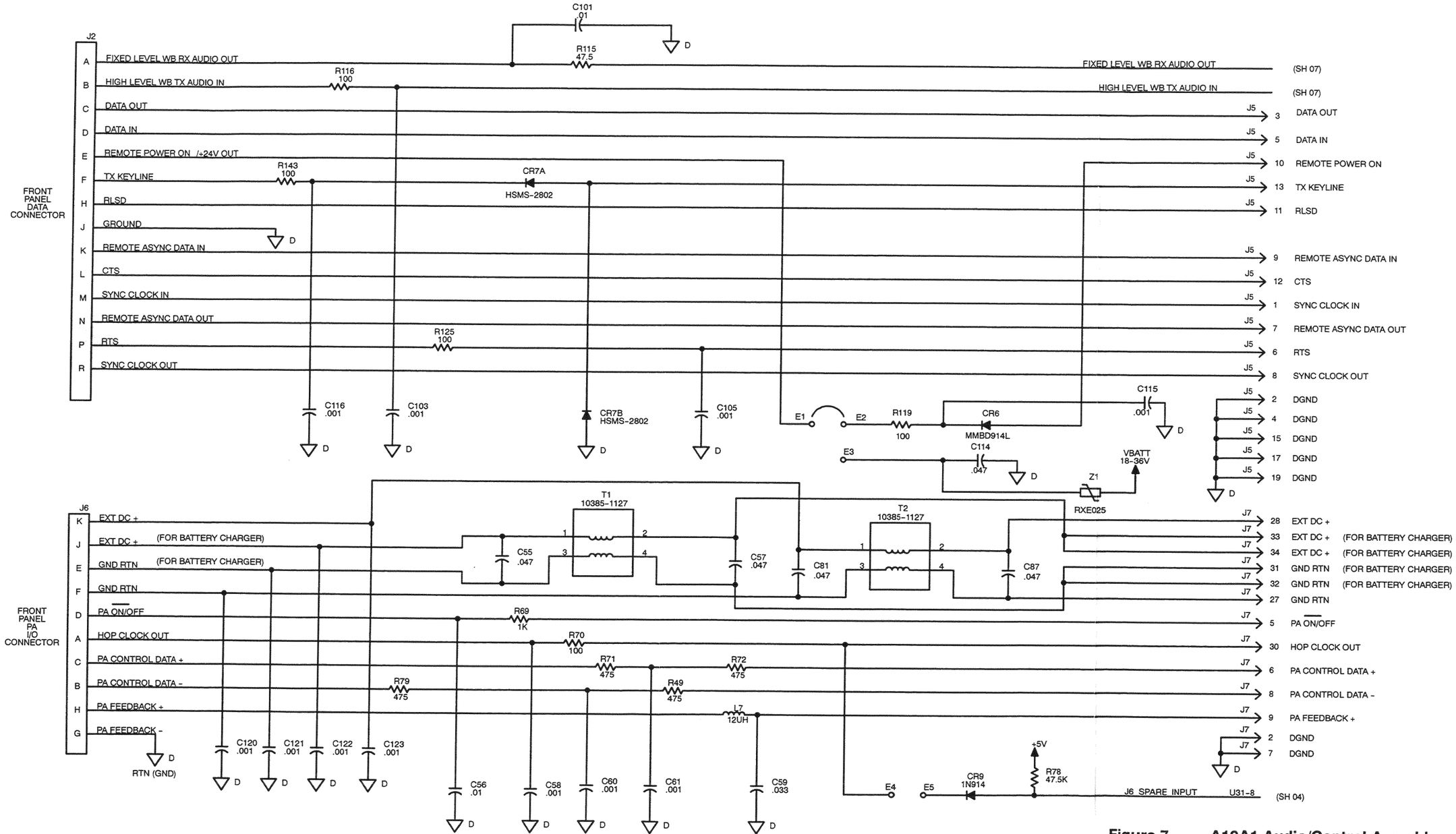
Figure 7. A10A1 Audio/Control Asembly Schematic Diagram (10303-2101 Rev. F) (Sheet 6 of 9)

10303-2101 REV F
SHEET 6 OF 9



10303-2101 REV F
SHEET 7 OF 9

Figure 7. A10A1 Audio/Control Asembly Schematic Diagram (10303-2101 Rev. F) (Sheet 7 of 9)



10303-2101 REV F
SHEET 8 OF 9

Figure 7. **A10A1 Audio/Control Asembly Schematic Diagram (10303-2101 Rev. F) (Sheet 8 of 9)**

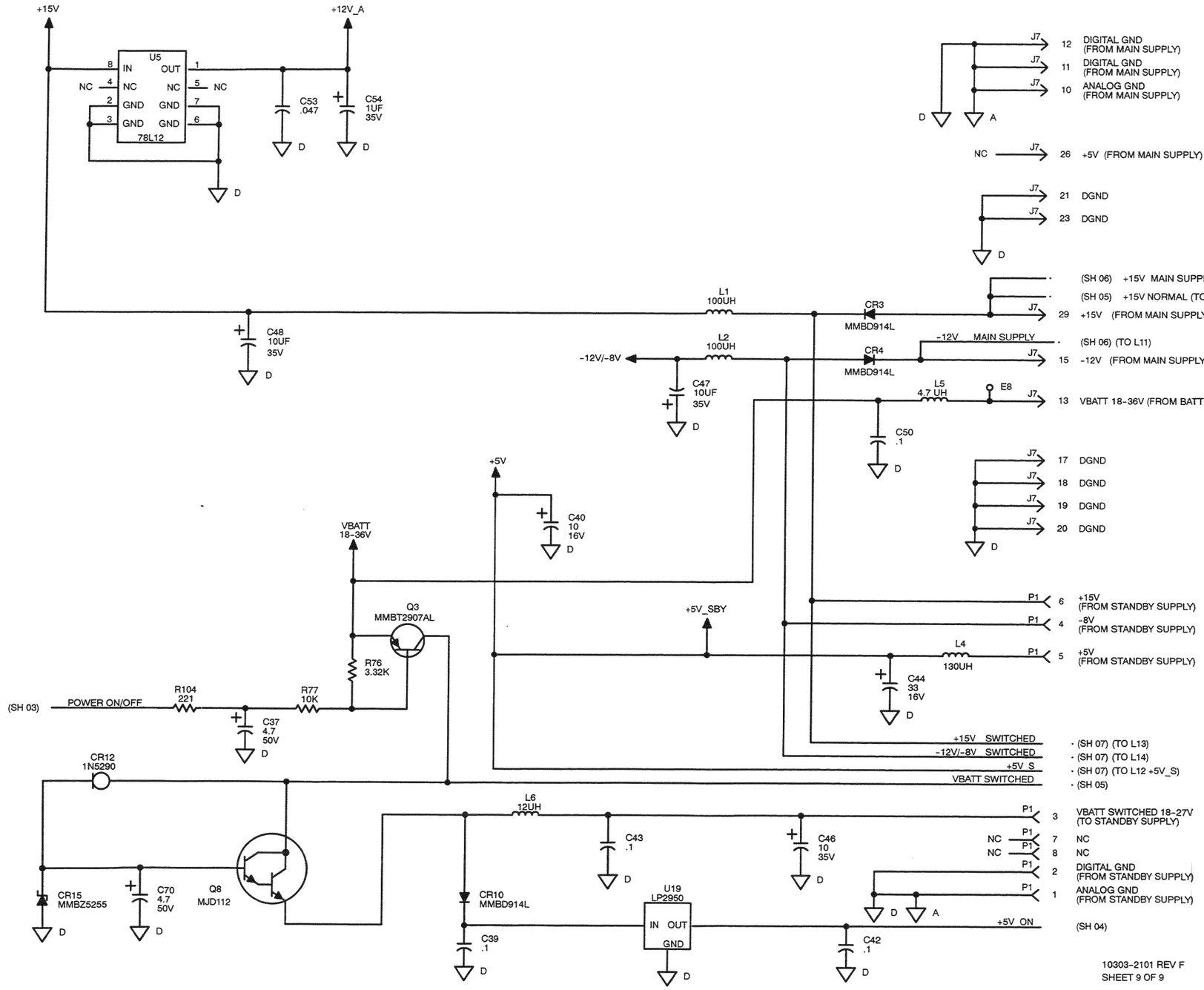


Figure 7. A10A1 Audio/Control Assembly Schematic Diagram (10303-2101 Rev. F) (Sheet 9 of 9)

Table 10. A10A1A2 Standby Power Supply Assembly Parts List (10303-2250 Rev. G)

Ref. Desig.	Part Number	Description
C1	C13-0107-104	CAP, .1UF 10% 100V CER
C2	C36-0050-475	CAP 4.7UF 10% 50V TANT SM
C3	C13-0103-103	CAP .01UF 10% 100V SMD
C4	C36-0035-106	CAP TANT 10UF 10% 35V
C6	M39006/25-0051	CAP,ELECT 120UF 50V
C7	C13-0107-104	CAP, .1UF 10% 100V CER
C8	C36-0016-475	CAP 4.7UF 10% 16V TANT SM
C9	C36-0020-106	CAP 10UF 20V SMT
C10	C36-0016-106	CAP 10UF 16V SMT
C12	C36-0016-475	CAP 4.7UF 10% 16V TANT SM
CR1	D15-0914-101	DIODE HI-SPD SWITCHING
CR2	D20-0005-001	DIODE, SOT-23
CR3	D15-0914-101	DIODE HI-SPD SWITCHING
CR4	D05-0005-013	DIODE, MMBZ5238BL
CR5	D22-0038-001	DIODE, RECTIFIER
J1	J46-0074-008	HEADER, 8 PIN, 65516-108
R1	R85-0004-401	RES 100K 1% 1/8W FLM
R2	R85-0004-291	RES 8.66K 1% 1/8W FILM
R3	R85-0004-210	RES 1.24K 1% 1/8W SMD
R4	R85-0004-409	RES 121K 1% 1/8W FLM
R5	R85-0004-166	RES 475 1% 1/8W SMD
R6	R85-0004-358	RES 39.2K 1% 1/8W FLM
T1	10303-3181-01	TRANSFORMER
U1	I10-0019-001	IC,MICRO PWRREG LP2951ACM
U2	I10-0020-001	IC,MICRO PWRCON LT1111CS8
U3	I10-0022-001	IC, LTC1044CS8

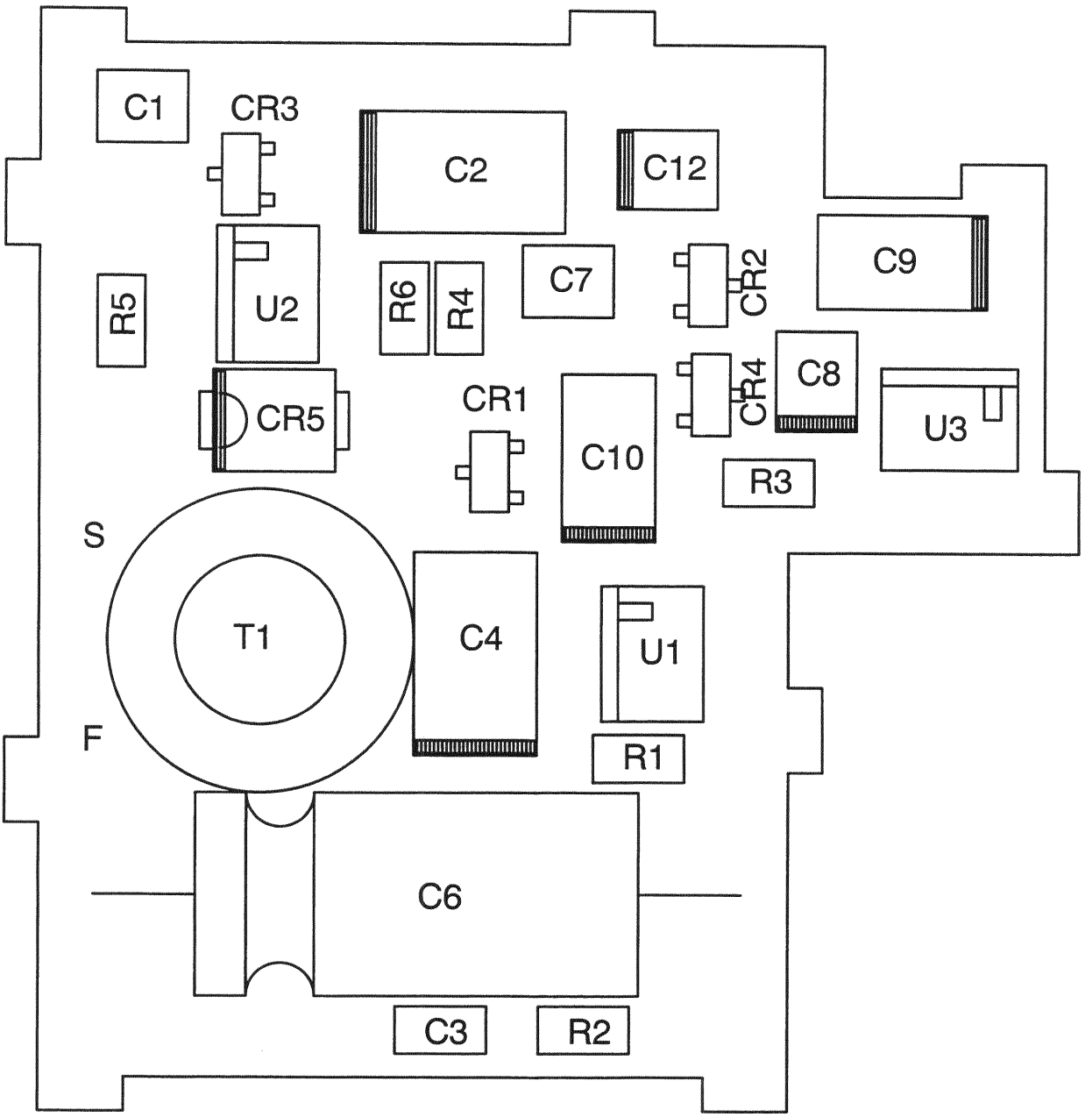


Figure 8. A10A1A2 Standby Power Supply Assembly Component Location Diagram (10303-2250 Rev. C) (Sheet 1 of 2)

Table 10. A10A1A2 Standby Power Supply Assembly Parts List (10303-2250 Rev. G)

Ref. Desig.	Part Number	Description
C1	C13-0107-104	CAP, .1UF 10% 100V CER
C2	C36-0050-475	CAP 4.7UF 10% 50V TANT SM
C3	C13-0103-103	CAP .01UF 10% 100V SMD
C4	C36-0035-106	CAP TANT 10UF 10% 35V
C6	M39006/25-0051	CAP,ELECT 120UF 50V
C7	C13-0107-104	CAP, .1UF 10% 100V CER
C8	C36-0016-475	CAP 4.7UF 10% 16V TANT SM
C9	C36-0020-106	CAP 10UF 20V SMT
C10	C36-0016-106	CAP 10UF 16V SMT
C12	C36-0016-475	CAP 4.7UF 10% 16V TANT SM
CR1	D15-0914-101	DIODE HI-SPD SWITCHING
CR2	D20-0005-001	DIODE, SOT-23
CR3	D15-0914-101	DIODE HI-SPD SWITCHING
CR4	D05-0005-013	DIODE, MMBZ5238BL
CR5	D22-0038-001	DIODE, RECTIFIER
J1	J46-0074-008	HEADER, 8 PIN, 65516-108
R1	R85-0004-401	RES 100K 1% 1/8W FLM
R2	R85-0004-291	RES 8.66K 1% 1/8W FILM
R3	R85-0004-210	RES 1.24K 1% 1/8W SMD
R4	R85-0004-409	RES 121K 1% 1/8W FLM
R5	R85-0004-166	RES 475 1% 1/8W SMD
R6	R85-0004-358	RES 39.2K 1% 1/8W FLM
T1	10303-3181-01	TRANSFORMER
U1	I10-0019-001	IC,MICRO PWRREG LP2951ACM
U2	I10-0020-001	IC,MICRO PWRCON LT1111CS8
U3	I10-0022-001	IC, LTC1044CS8

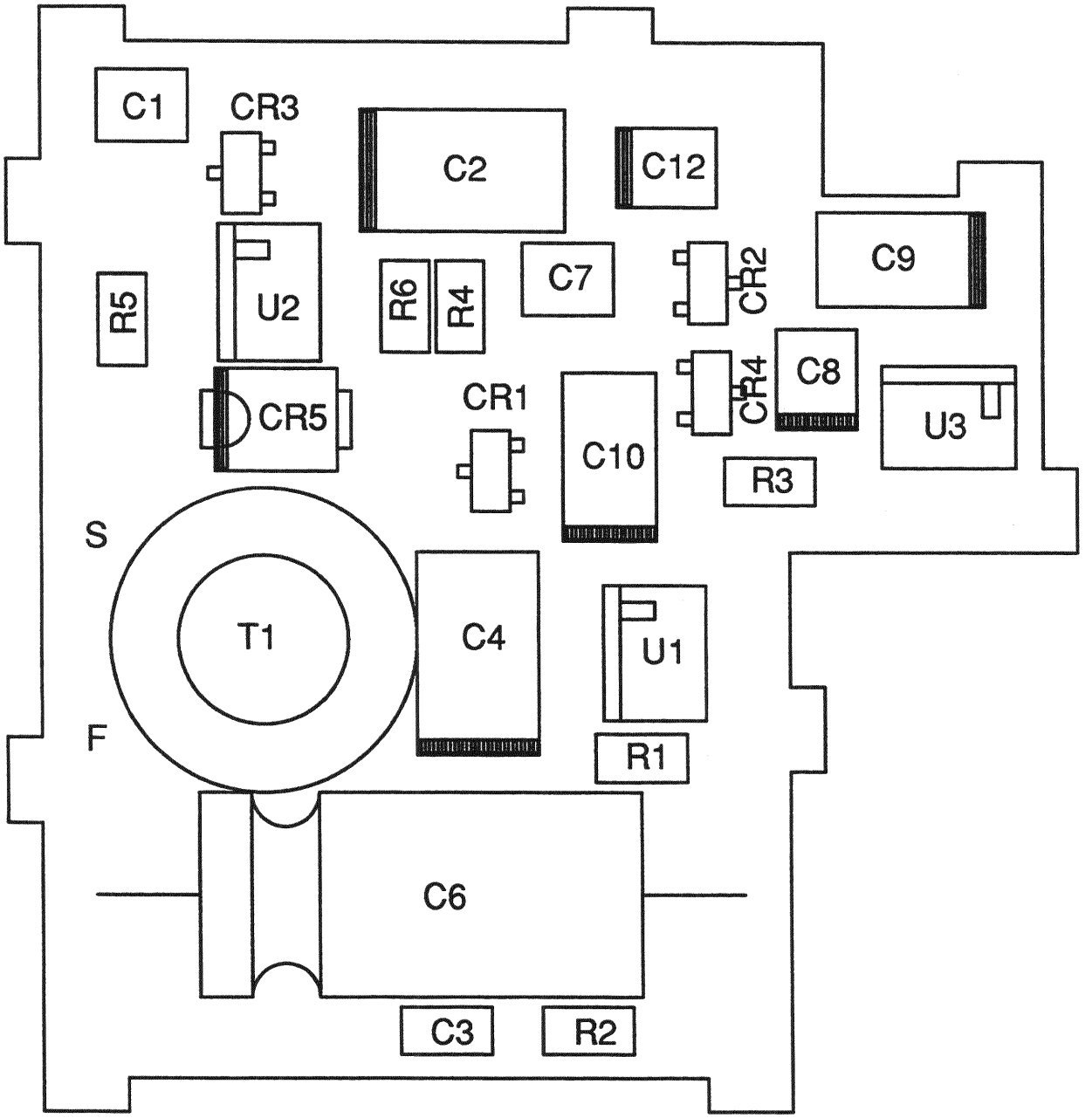


Figure 8. A10A1A2 Standby Power Supply Assembly Component Location Diagram (10303-2250 Rev. C) (Sheet 1 of 2)

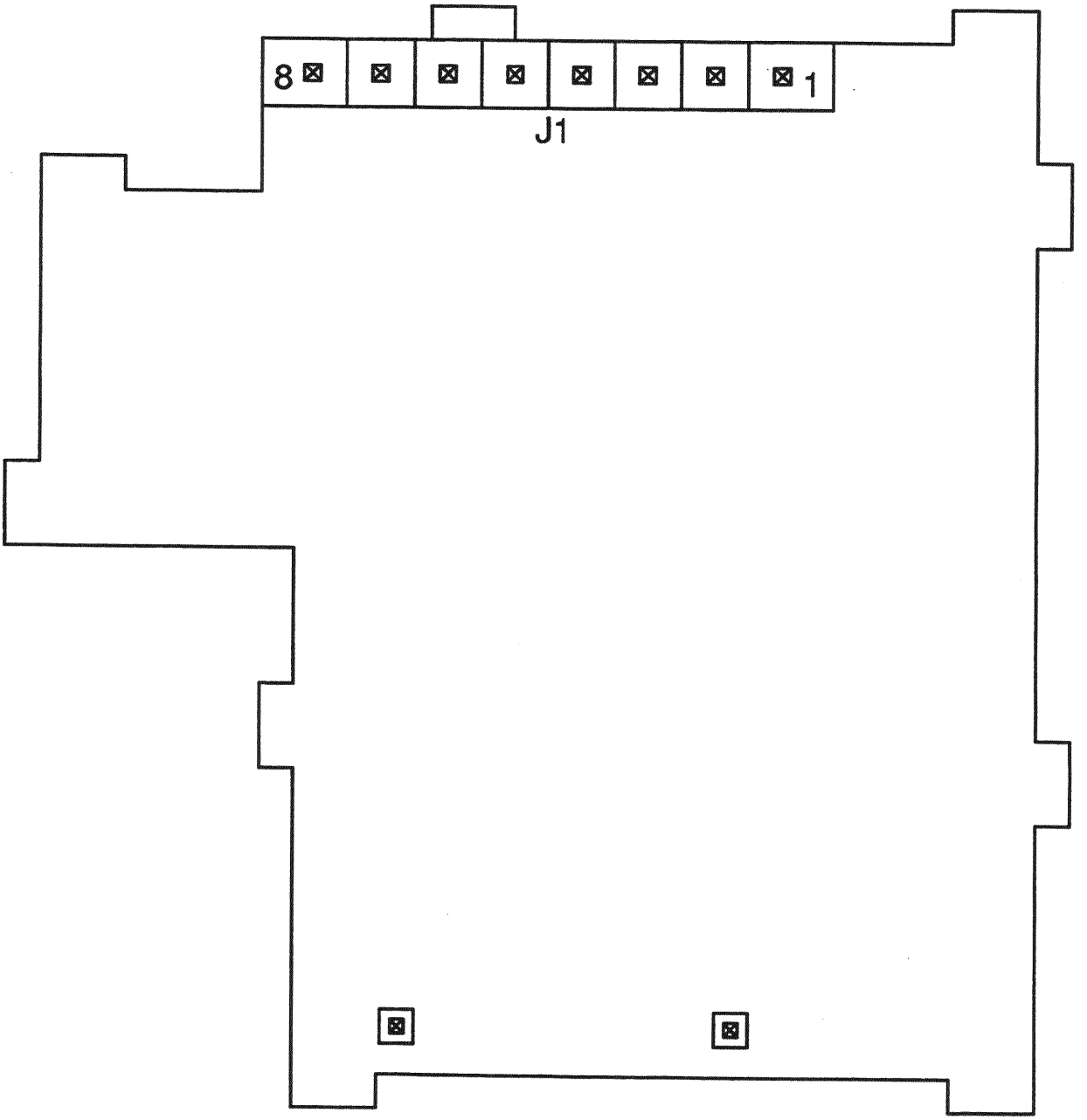


Figure 8. A10A1A2 Standby Power Supply Assembly Component Location Diagram (10303-2250, Rev. C) (Sheet 2 of 2)

NOTE: UNLESS OTHERWISE SPECIFIED:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR A COMPLETE DESIGNATION, PREFIX WITH UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.
2. ALL RESISTOR VALUES ARE IN OHMS, 1/8W, +/-1%.
3. ALL CAPACITOR VALUES ARE IN MICROFARADS.
4. VENDOR PART NO. CALLOUTS ARE FOR REFERENCE ONLY. COMPONENTS ARE SUPPLIED PER PART NO. IN PARTS LIST.

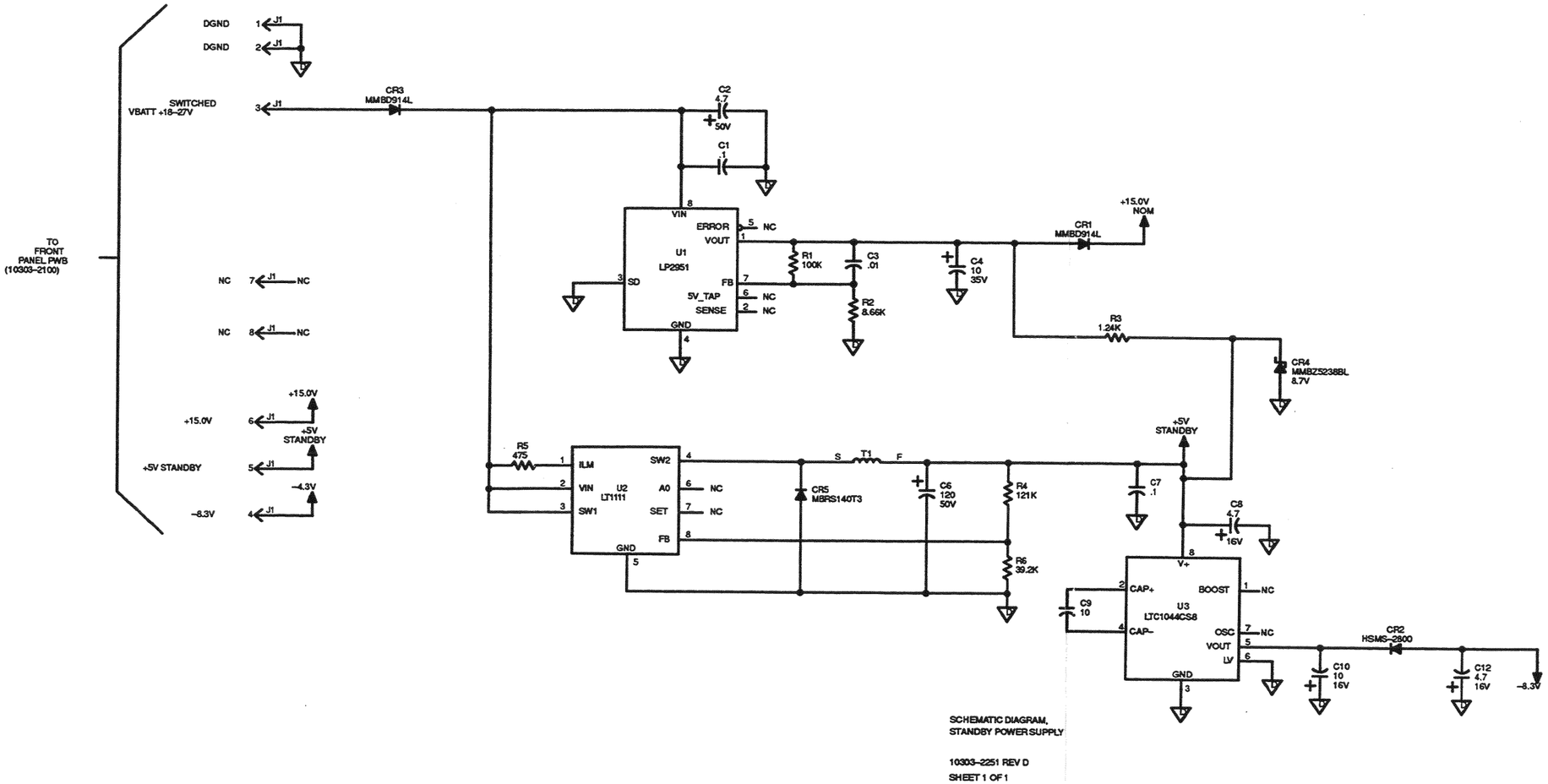


Figure 9. A10A1A2 Standby Power Supply Assembly Schematic Diagram (10303-2251 Rev. D)

Table 11. A10A2 Keypad PWB Assembly Parts List (10303-2110-01 Rev. A)

Ref. Desig.	Part Number	Description
CR1	N21-0028-001	LED, GREEN, SMD
CR2	N21-0028-001	LED, GREEN, SMD
CR3	N21-0028-001	LED, GREEN, SMD
CR4	N21-0028-001	LED, GREEN, SMD
CR5	N21-0028-001	LED, GREEN, SMD
CR6	N21-0028-001	LED, GREEN, SMD
CR7	N21-0028-001	LED, GREEN, SMD
CR8	N21-0028-001	LED, GREEN, SMD
CR9	N21-0028-001	LED, GREEN, SMD
CR10	N21-0028-001	LED, GREEN, SMD
CR11	N21-0028-001	LED, GREEN, SMD
CR12	N21-0028-001	LED, GREEN, SMD
J4	J46-0074-511	HEADER, 11 PIN, DUPONT
R1	R85-0004-176	RES 604 1% 1/8W FLM
R2	R85-0004-176	RES 604 1% 1/8W FLM
R3	R85-0004-176	RES 604 1% 1/8W FLM

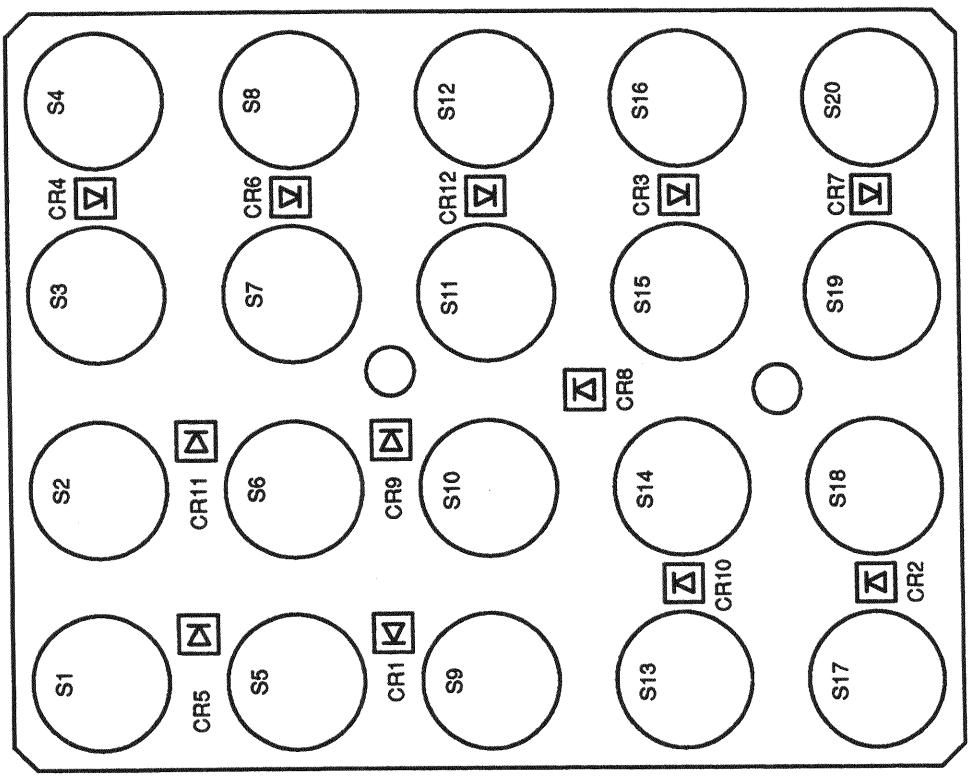


Figure 10. A10A2 Keypad Assembly Component Location Diagram (10303-2110 Rev. A) (Sheet 1 of 2)

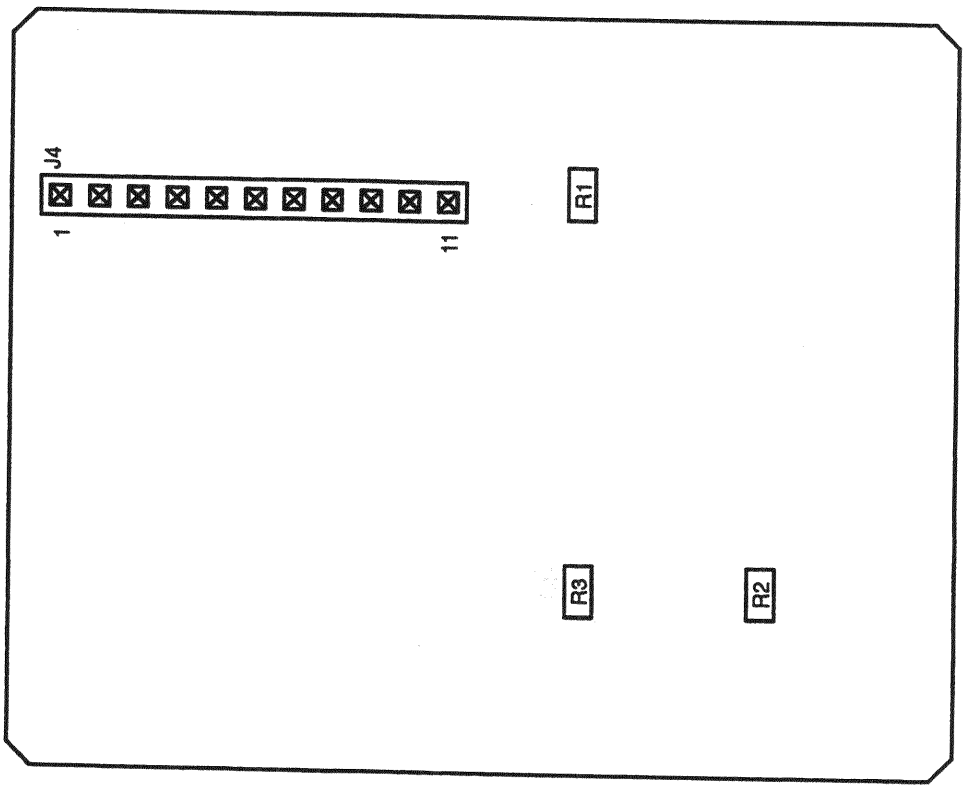
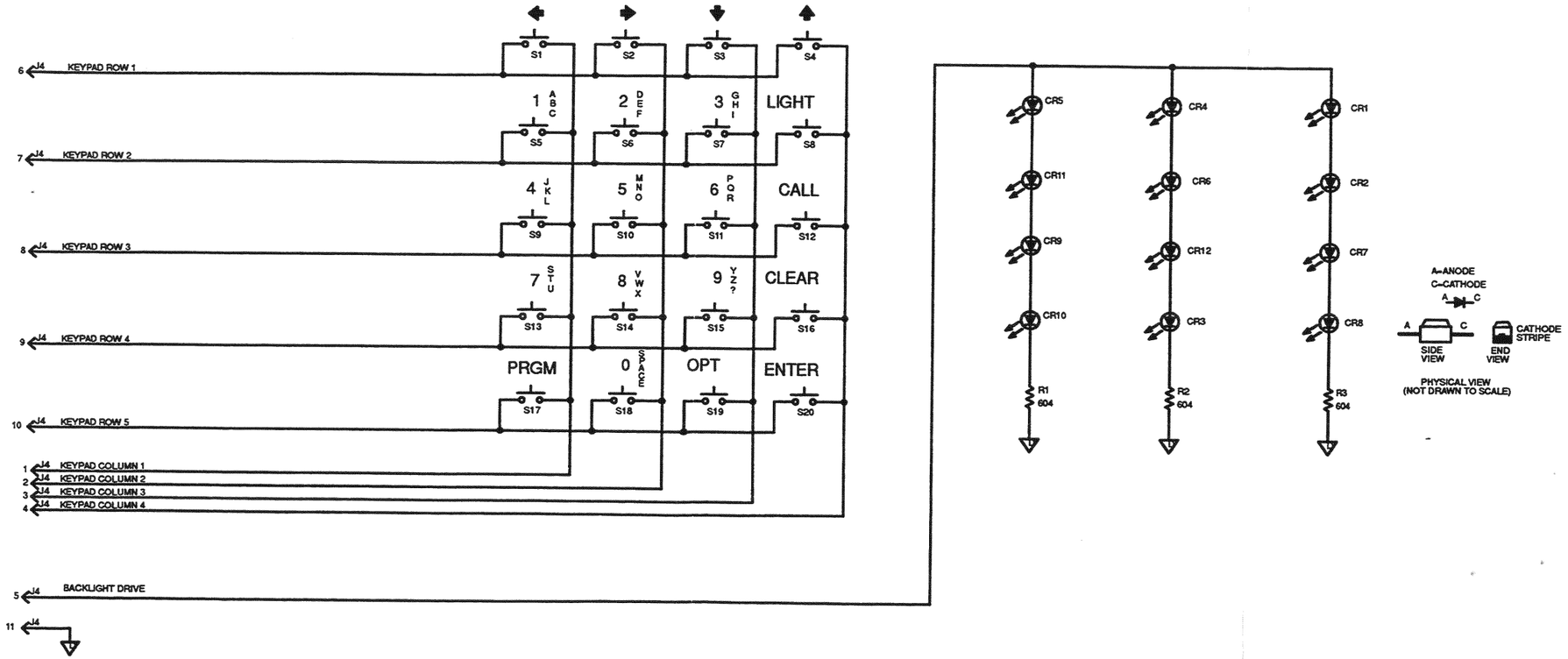


Figure 10. A10A2 Keypad Assembly Component Location Diagram (10303-2110 Rev. A) (Sheet 2 of 2)

NOTE: UNLESS OTHERWISE SPECIFIED:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR A COMPLETE DESIGNATION, PREFIX WITH UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.
2. ALL RESISTOR VALUES ARE IN OHMS, 1/8W, +/-1%.
3. ALL CAPACITOR VALUES ARE IN MICROFARADS.
4. VENDOR PART NO. CALLOUTS ARE FOR REFERENCE ONLY. COMPONENTS ARE SUPPLIED PER PART NO. IN PARTS LIST.
5. BACKSLASH (/) DENOTES ACTIVE LOW.



SCHEMATIC DIAGRAM,
BACKLIT KEYPAD

10303-2111 –

1 OF 1

Figure 11. A10A2 Keypad PWB Assembly Schematic Diagram (10303-2111 Rev. –)

A11
MOTHERBOARD

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LIST OF FIGURES

LIST OF TABLES

A11 MOTHERBOARD

1. GENERAL DESCRIPTION

The A11 Motherboard Assembly provides interconnection of plug-in modules A1 through A10, including signal routing, control, and power distribution. The A11A1 Daughterboard Assembly serves as intermediate interconnection for the A5 and A6 assemblies.

2. INTERFACE CONNECTIONS

Interface connection information is provided in the individual module sections and on the A11 Motherboard and the A11A1 Daughterboard schematic diagrams at the end of this section.

3. TECHNICAL DESCRIPTION

There is no technical description for the A11 Motherboard Assembly.

4. TESTING AND ALIGNMENT

There are no test or alignment procedures required for the A11 Motherboard Assembly.

5. BITE FAULTS AND TROUBLESHOOTING

There are no bite faults or troubleshooting provided for the A11 Motherboard Assembly; however, the following is a list of possible defects:

- Blown fuse (F1 or F2)
- Broken or loose connector
- Intermittent connection in ribbon cable
- Solder bridge on connector
- Ensure proper amperage fuses are in their proper place on motherboard

6. PARTS LIST, COMPONENT LOCATION DIAGRAM, AND SCHEMATIC DIAGRAM

Table 1 is the parts list, figure 1 is the component location diagram, and figure 2 is the schematic diagram for the A11 Motherboard Assembly. Table 2 is the parts list, figure 3 is the component location diagram, and figure 4 is the schematic diagram for the Daughterboard Interconnect PWB Assembly.

Table 1. A11 Motherboard Assembly Parts List (10303-2170 Rev. F)

Ref. Desig.	Part Number	Description
–	10303-2179	PCB MOTHER BOARD
–	10303-1206-01	INSULATOR, PWB
–	J60-0012-001	SOCKET, FUSE, HDWR SP.INC
–	10372-1032-01	SUPPORT, PWB
–	10303-1218-01	SPACER, PWB SUPPORT
–	MS51957-4	PHS SS 2-56X5/16
–	10303-3024	WASHER, FLAT #2 SM
–	MS35338-134	LW SPLT SS #2
A1	10303-2190	PWB ASSY, INTERCONNECT
C1	C13-0101-101	CAP 100PF 10% 100V SMD

Table 1. A11 Motherboard Assembly Parts List (10303-2170 Rev. F) (Cont.)

Ref. Desig.	Part Number	Description
C2	C13-0101-101	CAP 100PF 10% 100V SMD
C3	C13-0101-101	CAP 100PF 10% 100V SMD
C4	C13-0101-101	CAP 100PF 10% 100V SMD
C5	C13-0101-101	CAP 100PF 10% 100V SMD
C6	C13-0101-101	CAP 100PF 10% 100V SMD
C7	C13-0101-101	CAP 100PF 10% 100V SMD
C8	C13-0101-101	CAP 100PF 10% 100V SMD
C9	C13-0101-101	CAP 100PF 10% 100V SMD
C10	C13-0101-101	CAP 100PF 10% 100V SMD
C11	C13-0101-101	CAP 100PF 10% 100V SMD
C12	C13-0101-101	CAP 100PF 10% 100V SMD
C13	C13-0101-101	CAP 100PF 10% 100V SMD
C14	C13-0101-101	CAP 100PF 10% 100V SMD
C15	C13-0101-101	CAP 100PF 10% 100V SMD
C16	C13-0101-101	CAP 100PF 10% 100V SMD
C17	C13-0101-101	CAP 100PF 10% 100V SMD
C18	C13-0101-101	CAP 100PF 10% 100V SMD
C19	C13-0101-101	CAP 100PF 10% 100V SMD
C20	C13-0101-101	CAP 100PF 10% 100V SMD
C21	C13-0101-101	CAP 100PF 10% 100V SMD
F1	F15-0001-015	FUSE 7A, 125V
F2	F15-0001-009	FUSE 2A 125V
J1	J46-0116-050	CONN, 50 PIN FEMALE SMD
J2	J46-0116-050	CONN, 50 PIN FEMALE SMD
J3	J46-0116-050	CONN, 50 PIN FEMALE SMD
J9	J46-0125-130	CONN, 30 PIN
J10	J46-0116-050	CONN, 50 PIN FEMALE SMD
J12	J46-0087-414	CONN, 2 X 7
JMP1	R85-0004-000	RES ZERO OHM 1/8W FILM
P1	10303-1271-01	CABLE ASSY, 34 POS (PA)
P2	10303-1270-01	CABLE ASSY, 20 POS (CPLR)
P5	10303-1272-01	CABLE ASSY, 20 POS (FP)
P7	10303-1273-01	CABLE ASSY, 34 POS (FP)
R1	R85-0004-101	RES 100 1% 1/8W FLM
R2	R85-0004-101	RES 100 1% 1/8W FLM
R3	R85-0004-201	RES 1000 1% 1/8W FLM
R4	R85-0004-101	RES 100 1% 1/8W FLM
R5	R85-0004-101	RES 100 1% 1/8W FLM
R6	R85-0004-101	RES 100 1% 1/8W FLM

Table 1. A11 Motherboard Assembly Parts List (10303-2170 Rev. F) (Cont.)

Ref. Desig.	Part Number	Description
R7	R85-0004-101	RES 100 1% 1/8W FLM
R8	R85-0004-101	RES 100 1% 1/8W FLM
R9	R85-0004-101	RES 100 1% 1/8W FLM
R10	R85-0004-101	RES 100 1% 1/8W FLM
R11	R85-0004-101	RES 100 1% 1/8W FLM
R12	R85-0004-101	RES 100 1% 1/8W FLM
R13	R85-0004-101	RES 100 1% 1/8W FLM
R14	R85-0004-101	RES 100 1% 1/8W FLM
R15	R85-0004-101	RES 100 1% 1/8W FLM
R16	R85-0004-101	RES 100 1% 1/8W FLM
R17	R85-0004-101	RES 100 1% 1/8W FLM
R18	R85-0004-101	RES 100 1% 1/8W FLM
R19	R85-0004-101	RES 100 1% 1/8W FLM
R20	R85-0004-101	RES 100 1% 1/8W FLM
R21	R85-0004-101	RES 100 1% 1/8W FLM
R22	R85-0004-101	RES 100 1% 1/8W FLM
R23	R85-0004-101	RES 100 1% 1/8W FLM
R24	R85-0004-101	RES 100 1% 1/8W FLM
R25	R85-0004-101	RES 100 1% 1/8W FLM
R26	R85-0004-101	RES 100 1% 1/8W FLM
R27	R85-0004-101	RES 100 1% 1/8W FLM
R28	R85-0004-101	RES 100 1% 1/8W FLM
R29	R85-0004-101	RES 100 1% 1/8W FLM
R30	R85-0004-101	RES 100 1% 1/8W FLM

Table 2. A11A1 Interconnect PWB Assembly Parts List (10303-2190 Rev. A)

Ref. Desig.	Part Number	Description
–	10303-2199	PWB
–	J46-0122-120	HEADER, 2 X 10
–	J46-0122-108	HEADER, 2 X 4
–	10303-1211-01	INSULATOR
–	J46-0122-106	HEADER, 2 X 3
J4	J46-0116-030	CONN, 30 PIN FEMALE SMD
J5	J46-0116-020	CONN, 20 PIN FEMALE SMD

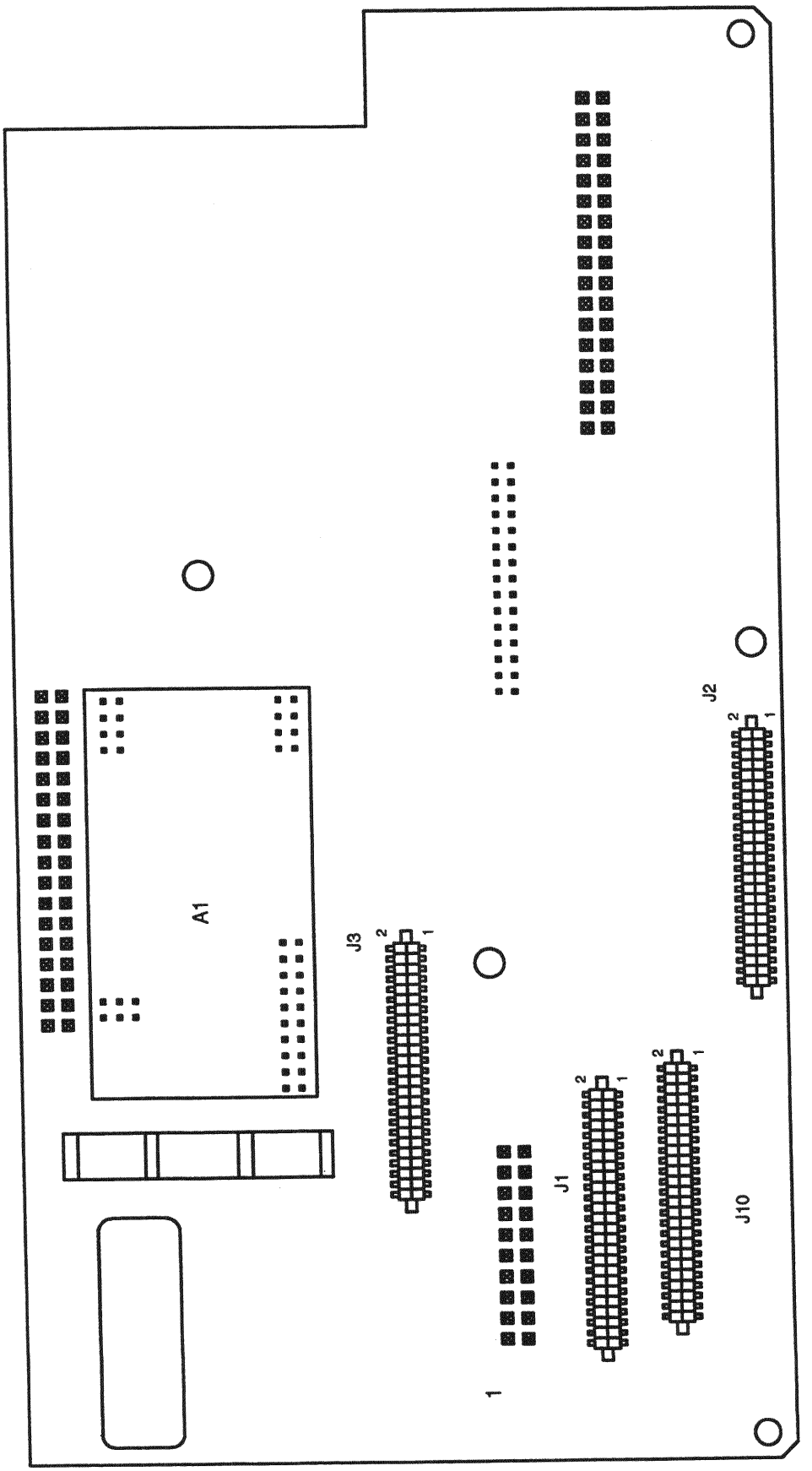


Figure 1. A11 Motherboard PWB Assembly Component Location Diagram
(10303-2170 Rev. E) (Sheet 1 of 2)

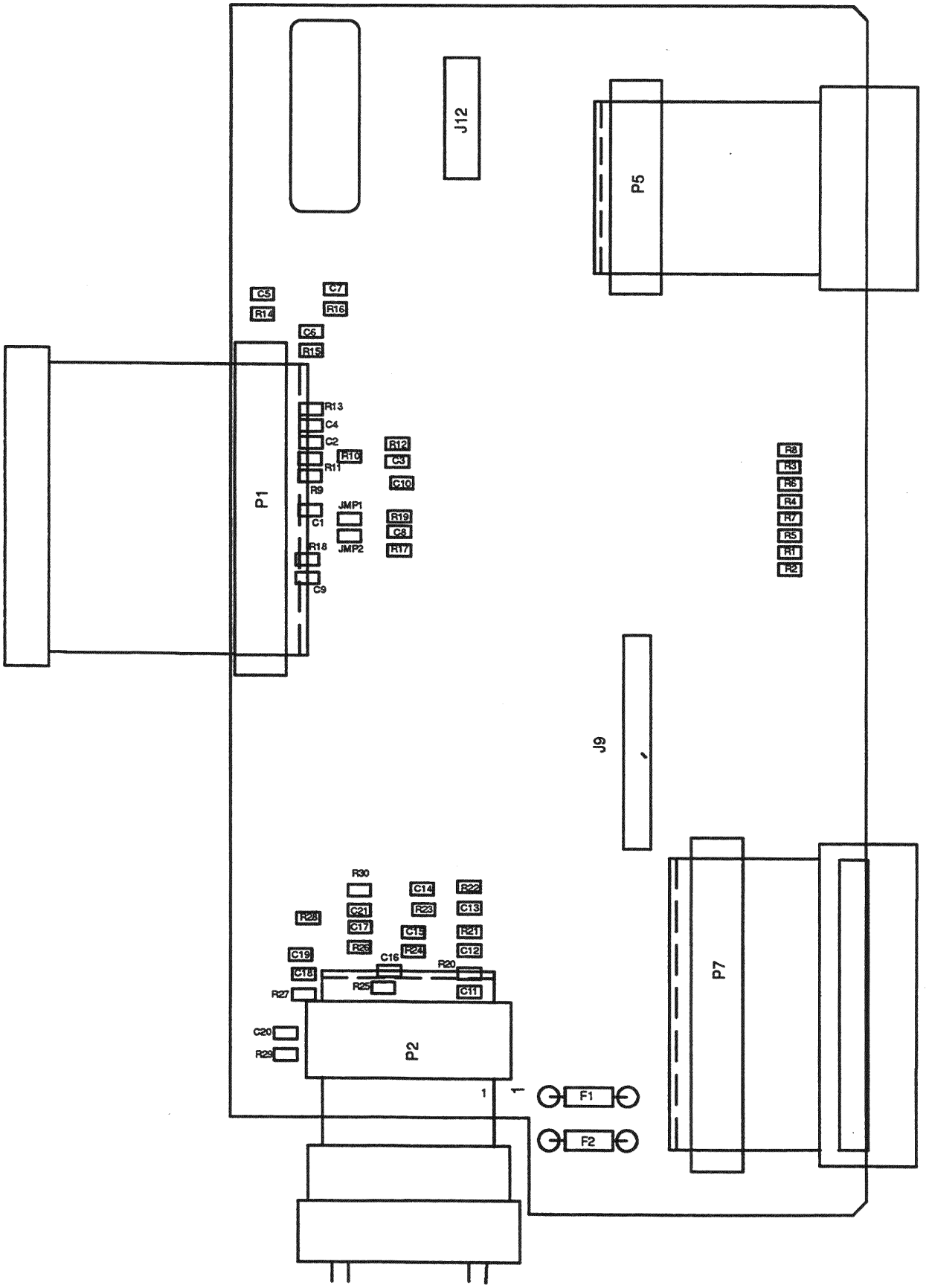


Figure 1. A11 Motherboard PWB Assembly Component Location Diagram
(10303-2170 Rev. E) (Sheet 2 of 2)

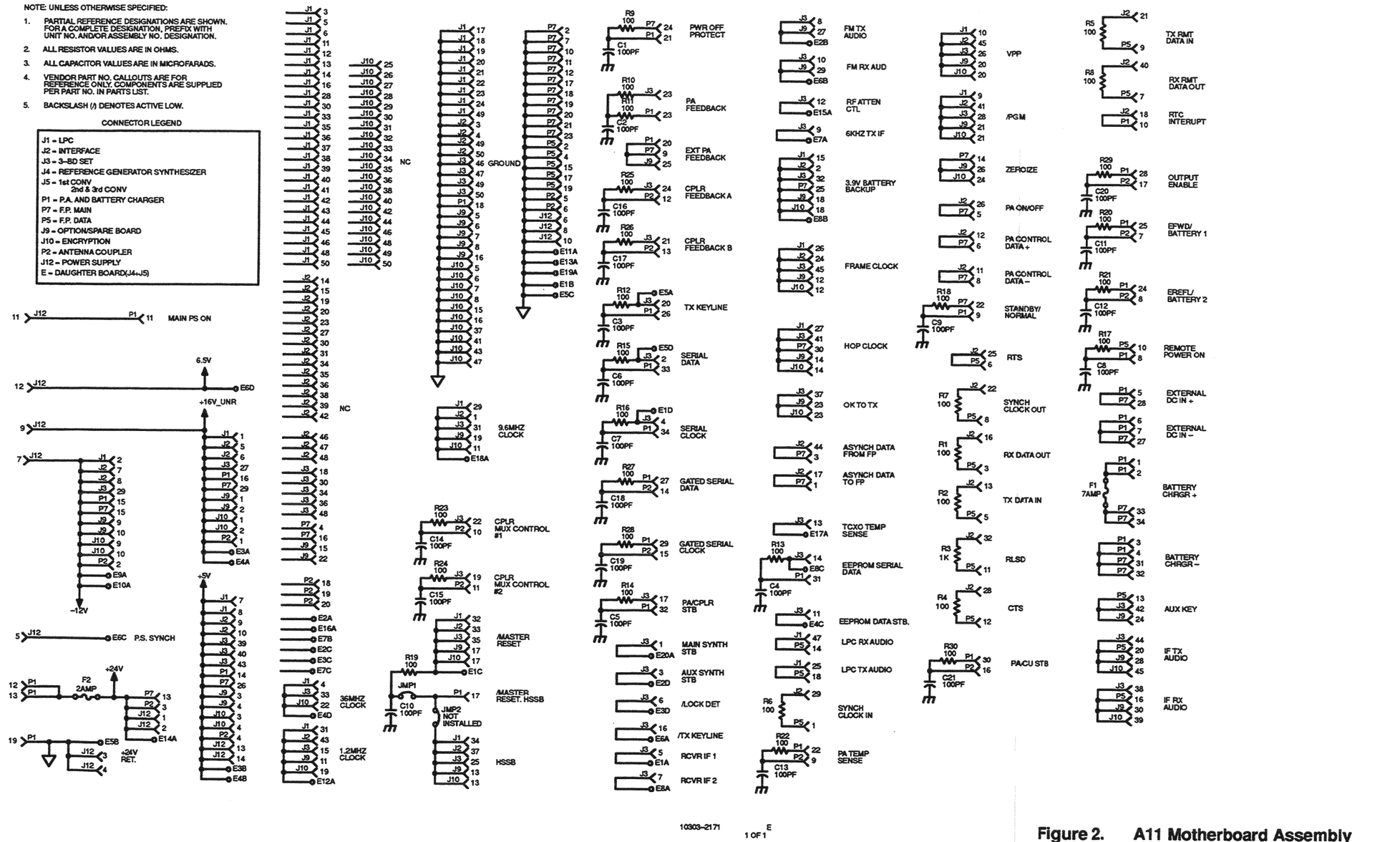


Figure 2. A11 Motherboard Assembly Schematic Diagram (10303-2171 Rev. E)

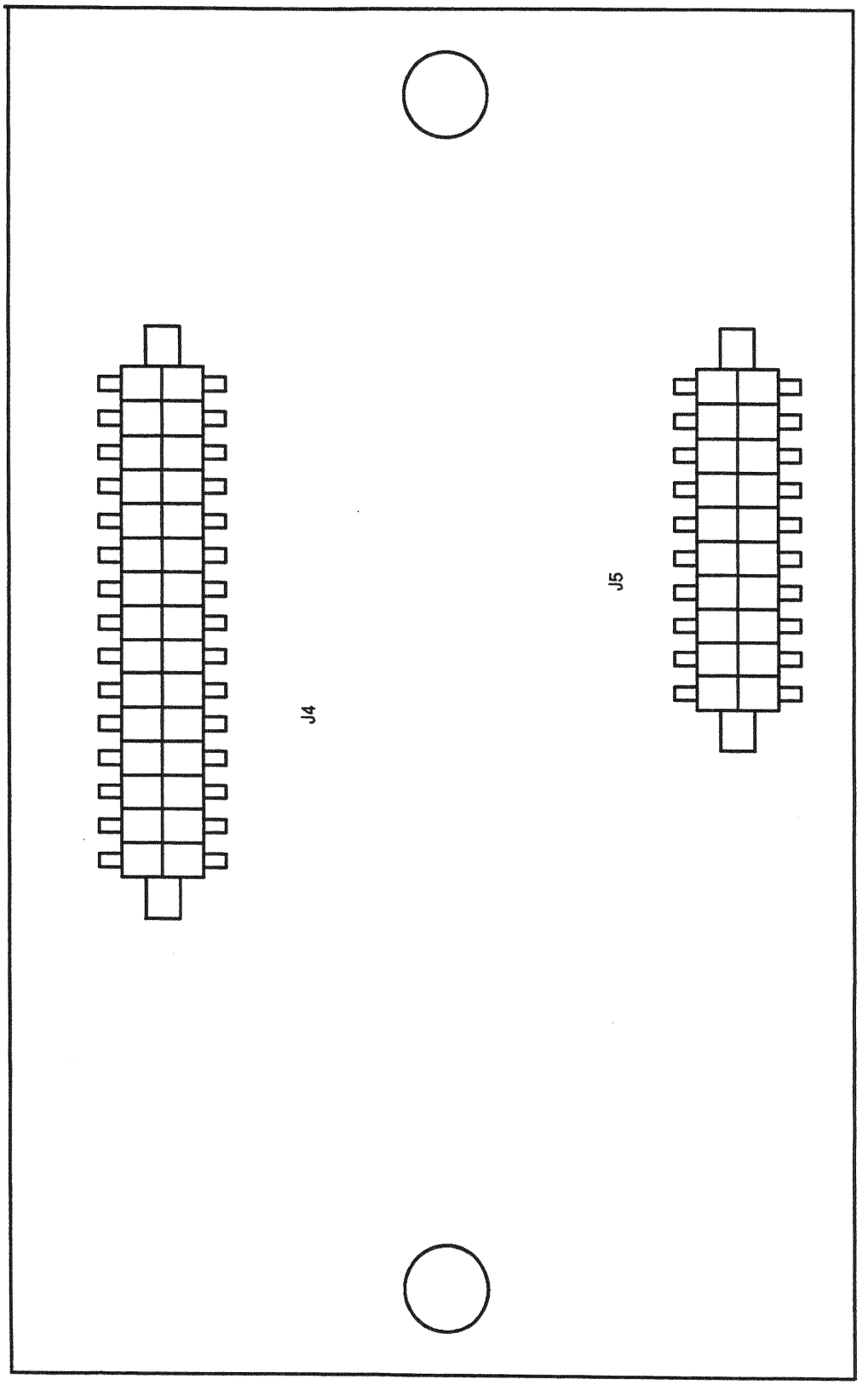


Figure 3. A11A1 Daughterboard PWB Assembly Component Location Diagram
(10303-2190 Rev. A) (Sheet 1 of 2)

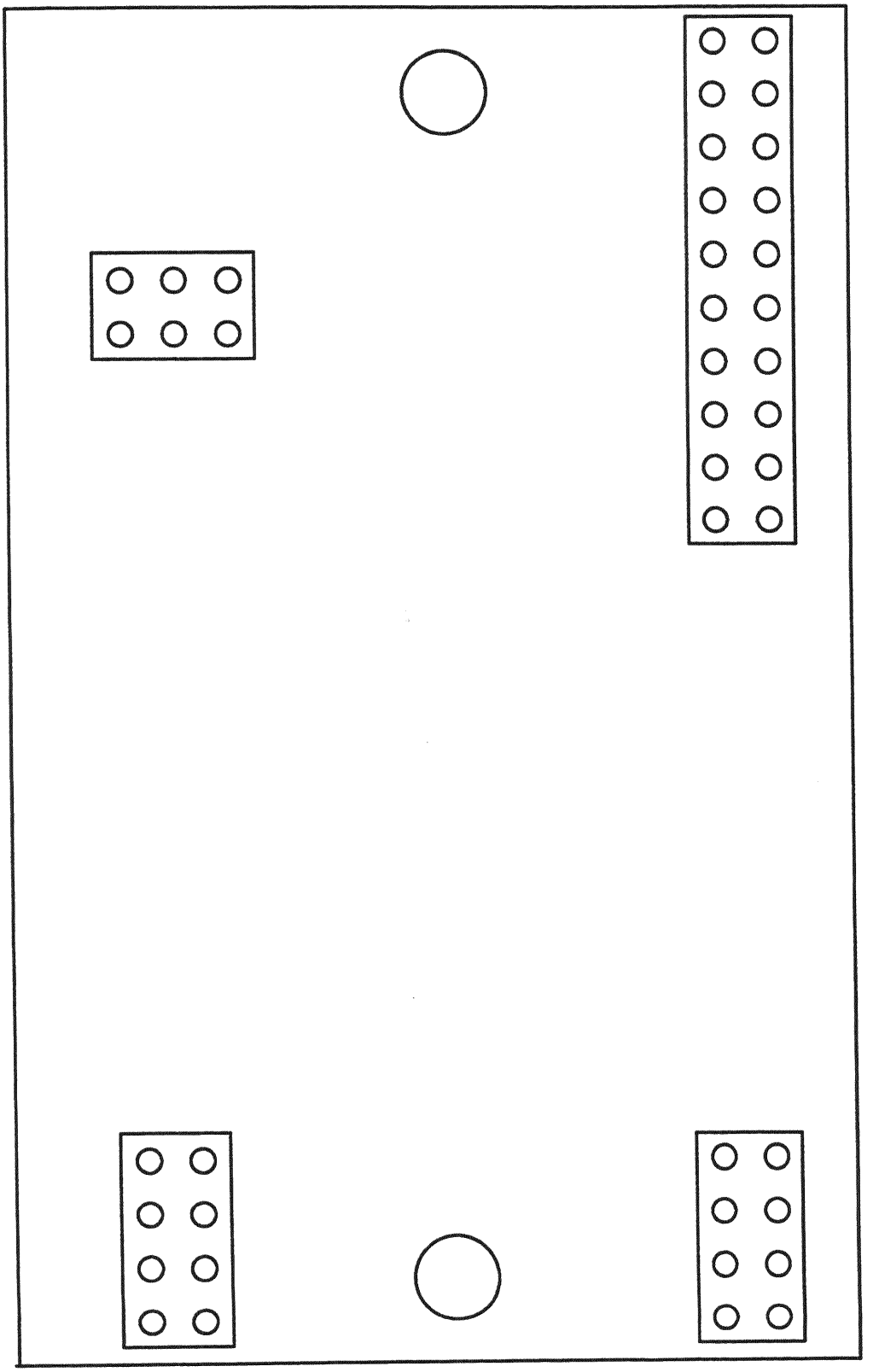


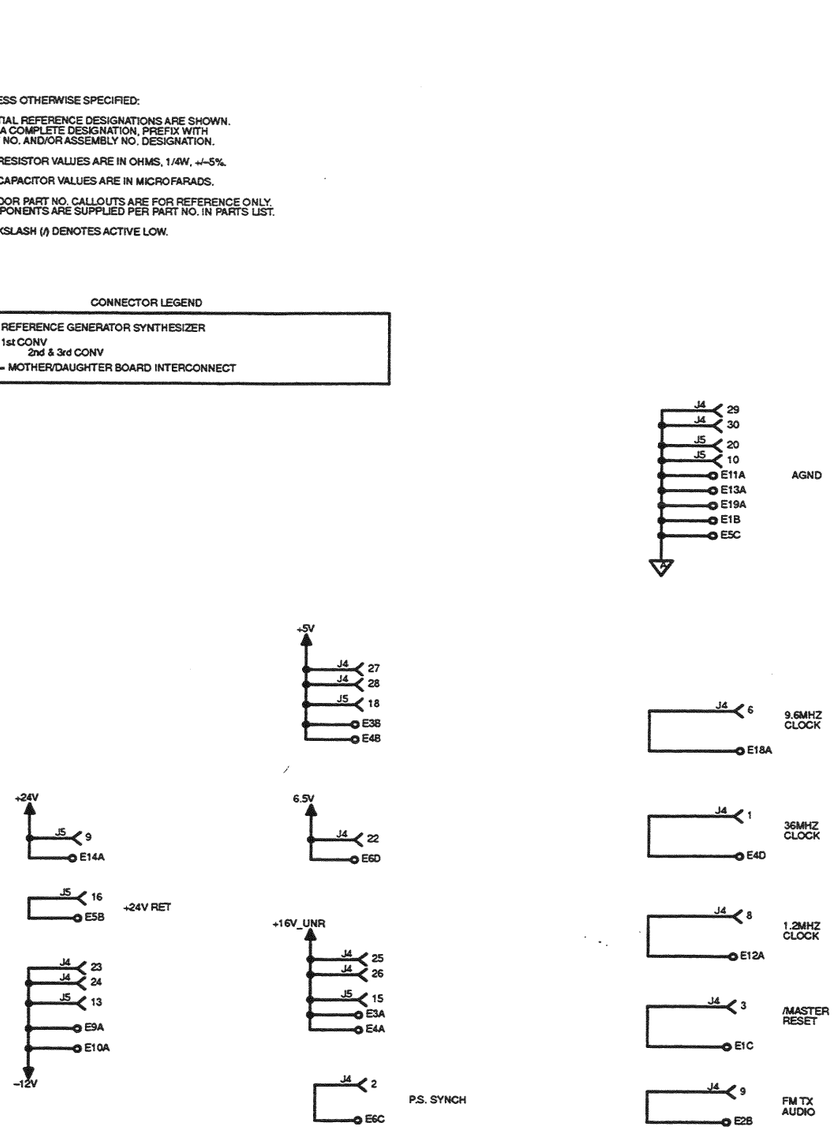
Figure 3. A11A1 Daughterboard PWB Assembly Component Location Diagram
(10303-2190 Rev. A) (Sheet 2 of 2)

NOTE: UNLESS OTHERWISE SPECIFIED:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR A COMPLETE DESIGNATION, PREFIX WITH UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.
2. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, +/-5%.
3. ALL CAPACITOR VALUES ARE IN MICROFARADS.
4. VENDOR PART NO. CALLOUTS ARE FOR REFERENCE ONLY. COMPONENTS ARE SUPPLIED PER PART NO. IN PARTS LIST.
5. BACKSLASH (/) DENOTES ACTIVE LOW.

CONNECTOR LEGEND

J4 = REFERENCE GENERATOR SYNTHESIZER
J5 = 1st CONV
2nd & 3rd CONV
E = MOTHER/DAUGHTER BOARD INTERCONNECT



INTERCONNECT DIAGRAM, DAUGHTER BOARD

10303-2191 A

Figure 4. A11A1 Daughterboard Assembly Schematic Diagram (10303-2191 Rev. A)

APPENDIX

APPENDIX
MATERIAL SAFETY DATA SHEET
FOR
LITHIUM METAL, BATTERY QUALITY
INGOTS, FOIL, PARTS
EFFECTIVE: 11/01/85
REPLACES: (ALL PRIOR)

1. PRODUCT IDENTIFICATION

Manufacturer: Lithium Corporation

Address: P.O. Box 795, Bessemer City, NC 28016-0795

Trade Name: Lithium Metal Battery Quality Ingots, Foil, Parts

Synonym: None

Formula: LI

C.A.S. No.: 7439-93-2

Regular Telephone: 704-867-8371

EMERGENCY TELEPHONE NUMBERS

Medical (Collect): 303-595-9048

Chemtrec: 800-424-9300

Lithco: 704-629-5361

Chemical Family: Alkail Metals

2. PRECAUTIONARY STATEMENTS

2.1 Health Hazards

Corrosive to eyes and skin.

2.2 Physical Hazards

Flammable solid. Reacts violently with water to give off corrosive dust and hydrogen gas, which can explode or catch fire spontaneously at room temperature.

Elevated temperatures can result in spontaneous ignition in air.

3. INGREDIENTS

Material or Component	C.A.S. No.	%	TLV Hazard Data				Other
			PEL (OSHA)	TWA (ACGIH)	STEL (ACGIH)	Ceiling	
Lithium Metal	7439-93-2	100	No applicable information was found.				

4. PHYSICAL DATA

Boiling Point (760 Hg): 1317°C (2400°F)

Melting Point: 180.5 °C (357 °F)

Density: 0.53 g/cc

Vapor Density: Not applicable.

Vapor Pressure: Not applicable.

Evaporation Rate: Not applicable.

Solubility in Water: Reacts.

Volatiles: Not applicable.

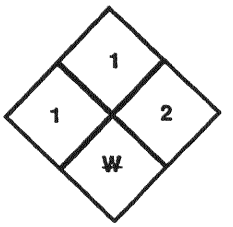
Appearance and Odor: Silvery-white, soft, metallic solid with no odor.

5. FIRE, EXPLOSION, AND REACTIVITY DATA

5.1 Physical Hazard

Flammable solid.

National Fire Prevention Code



5.2 Flash Point

Not applicable.

5.3 Autoignition Temperature

No applicable information was found.

5.4 Flammable Limits in Air

Not applicable.

5.5 Extinguishing Media

DO NOT use water, sand, or carbon dioxide. Use graphite, Lith-X (Ansul). If not available, use dry sodium chloride, dry (anhydrous) calcium oxide, or dry lithium chloride.

5.6 Special Fire Fighting Procedures

Wear self-contained breathing apparatus and full fire fighting protective clothing when fighting significant-sized fires.

Lithium fires can throw off molten lithium metal particles. Burning lithium releases corrosive lithium oxide dust and fumes.

Lithium metal can re-ignite after fire is initially extinguished. Never leave extinguished fire unattended. After all material has apparently burned and cooled, carefully turn over remaining residue and be prepared to re-extinguish should this re-ignition occur. Carefully place residue in a steel drum using a long-handled shovel, and cover with extinguishing media.

5.7 Unusual Fire and Explosion Hazards

Corrosive lithium oxide and/or lithium hydroxide fumes are released during combustion.

5.8 Stability

Stable.

5.9 Conditions Contributing to Instability

None.

5.10 Incompatibility

Moisture, acids, oxidizers, oxygen, nitrogen, carbon dioxide, elevated temperatures.

5.11 Hazardous Decomposition Products

Lithium is an element and does not decompose. However, it is highly reactive in contact with many other substances, releasing large quantities of heat and/or hazardous products. It can react violently with water, the humidity in moist air, and the moisture in other substances, releasing hydrogen gas, which may catch fire explosively. Corrosive fumes of lithium oxide and/or lithium hydroxide are also released. The reactivity of the lithium increases as the exposed surface area increases.

5.12 Conditions Contributing to Hazardous Polymerization

Does not polymerize.

6. HEALTH HAZARD INFORMATION

6.1 Health Hazard

Corrosive.

6.2 Product TLV

No applicable information was found.

6.3 Primary Route(s) of Entry

Eye Contact: No toxicology data available. Corrosive.

Skin Contact: No toxicology data available. Corrosive.

6.4 Symptoms of Exposure

Acute Overexposure: Severe chemical burns to eyes and skin.

Chronic Overexposure: Not applicable.

6.5 Emergency and First Aid Procedures

Eyes: Remove particles, then flush with plenty of water, occasionally lifting the lower and upper lids, for at least fifteen minutes. Obtain immediate medical attention.

Skin: Quickly brush off excess. Flush with plenty of water. If particles are embedded and cannot be removed, cover with mineral oil and do not flush with water. Obtain immediate medical attention.

7. SPILL OR LEAK PROCEDURES

7.1 Steps to be Taken if Material is Released or Spilled

To prevent ignition, coat with mineral oil (or kerosene), soaking thoroughly, and place in oiled steel drums, closing them securely and tightly. Keep away from water, rain, snow, etc.

Waste Disposal Method: Dispose of waste according to federal EPA, state, and local regulations.

8. SPECIAL PROTECTION INFORMATION

8.1 Ventilation Requirements

None.

8.2 Specific Personal Protection Equipment

Eyes: Safety glasses or goggles

Gloves: Rubber

8.3 Other Clothing and Equipment

Quick-drench eyewash and safety shower.

9. HANDLING AND STORAGE

Keep away from water, humid air, acids, and oxidizing materials.

Can be handled in open atmosphere at room temperature, either coated with mineral oil or where relative humidity is maintained below 2%.

Wear safety glasses or goggles, and dry rubber gloves.

Store in original, unopened shipping container. Once opened, store in argon atmosphere or mineral oil.

Protect shipping container from physical damage.

Store in a cool place.

Keep away from sparks, heat, and flame.

10. LITHCO PRODUCTS TO WHICH THIS MSDS APPLIES

This material safety data sheet applies to the following Lithco product code Nos.: 452, 460, 459, 463, 491, 508, 541, 543, 563, 583, 732, 733, 734, 735, 736, 737, 738, and 740.

11. CONTACT PERSON

Manager, Technical Services
Lithium Corporation of America
449 North Cox Road
P.O. Box 3925
Gastonia, North Carolina 28053-3925

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GLOSSARY

GLOSSARY

-A-

A, AMP	Ampere(s)
ac, AC	Alternating Current
ACE	Advanced Crypto Engine
ADC	Analog-to-Digital Converter
Address (ADDR)	Any alphanumeric string (except ALL or ANY) from 1 to 15 characters in length
AF	Audio Frequency
AFSK	Audio Frequency Shift Keying
AGC	Automatic Gain Control
AIC	Analog Interface Chip
ALC	Audio Level Control
ALE	Automatic Link Establishment
All Call	A unidirectional broadcast, made to all stations scanning on a given channel, in which no response signals are required from the Target Stations
AME	Amplitude Modulation Equivalent
AND gate	A circuit with two or more inputs and one output in which the output signal is high if and only if (sometimes written *iff*) all the inputs are high simultaneously.
ANDVT	Advanced Narrowband Digital Voice Terminal
ANT	Antenna
ANTIVOX	Voice-Operated Transmitter Key Inhibitor
Any Call	A call made to all stations scanning on a given channel in which responses are required from the Target Stations.
API	Analog Phase Interpolation
ARQ	Automatic Repeat on Request
ASI	Analog Signal Interface
ASK	Amplitude Shift Keying

GLOSSARY (Cont.)

-A- (Cont.)

Associated Self	A Self Address used in programming a Net
ATE	Automatic Test Equipment
AUD	Audio
Automatic Call	A call in which the best available channel is selected by the ALE
Automatic Link Establishment (ALE)	A technique that uses MIL-STD-188-141-specified octal FSK signalling (or similar) to automatically establish communications on the best available channel among two or more stations
Automatic Message Display (AMD)	An engineering orderwire message, up to 87 ASCII characters in length, sent to an Individual, Net, or Group
AUX	Auxiliary
AVS	Analog Voice Security
AWG	American Wire Gauge

-B-

BC	Broadcast, Binary Counter
BCD	Binary-Coded Decimal
BD	Baud, Binary Decoder
BER	Bit Error Rate
BFO	Beat frequency oscillator
BHE	Bus High Enable
Bidirectional LQA	An LQA technique which involves two-way messages sent between two stations on all common channels – channel rankings are established based on received signal quality
BIT	Built-In-Test; acronym from **bi**nary digi**t**. It is the basic unit of information in a computer or data processing system.
BITE	Built-In Test Equipment
Bit Error Rate (BER)	An evaluation of the ability of a channel to pass error-free data information
BNC	Baby N Connector (bayonet type)

GLOSSARY (Cont.)

-B- (Cont.)

BPI	Bits Per Inch
bps	Bits Per Second
BPSK	Binary Phase Shift Keying
Btu	British Thermal Unit
BW	Bandwidth
BYTE	A group of bits taken together and treated as a word in a digital computer.

-C-

Calling Station	The station initiating a call to a Target Station
CB	Circuit Breaker
CCW	Counterclockwise
Channel (CH., CHAN)	A programmed combination of frequency and mode of transmission
Channel Group	A programmed collection of channels – up to ten Channel Groups can be programmed, each containing up to 100 channels
Channel List	A list of channels a station is programmed to scan
Channel Score	A rating of overall channel quality
CKT	Circuit
cm	Centimeter
CMOS	Complimentary Metal-Oxide-Semiconductor
CSM	Crypto-sync message
CNTL	Control
CTRL	Control
CTS	Clear to Send
CW	Continuous Wave, Clockwise

GLOSSARY (Cont.)

-D-

Data Text Message (DTM)	An engineering orderwire text message sent to a Target Station using an automatic repeat (ARQ) protocol to ensure error-free reception of the message
dB	Decibel(s)
dBi	Decibels referenced to Isotropic Radiator
dBm	Decibels referenced to 1 milliwatt
dc, DC	Direct Current
DE	Data Encryption
DGC	Digital Gain Control
DIF	Digital Intermediate Frequency
DIP	Dual in-line package
DMA	Direct Memory Access
Demod	Demodulated
Double Selective Any Call	An Any Call made to all stations whose addresses end in the same two characters
DPRAM	Dual port RAM
DS	Data Space
DSP	Digital Signal Processor
DTE	Data Terminal Equipment
DTMF	Dual Tone Multi-Frequency
DTR	Data Terminal Ready
DV	Digitized Voice
DVM	Digital Voltmeter
DVOM	Digital Volt-Ohm Meter

-E-

EAM	Embedded Adaptive Module
EAROM	Electronically Alterable Read-Only Memory

GLOSSARY (Cont.)

-E- (Cont.)

ECM	Electronic Countermeasure
ECCM	Electronic Counter-Countermeasure
EIA	Electronic Industries Association
EMI	Electromagnetic Interference
EOM	End of Message
EPROM	Erasable Programmable Read-Only Memory
Exchange	An LQA technique which involves two-way messages sent between two stations on all common channels – channel rankings are established based on received signal quality
Exclusive OR gate	A circuit with two or more inputs and one output whose output is high if one input is high.

-F-

FAX	Facsimile transmission
Fc	Center frequency
FCC	Federal Communications Commission
FEC	Forward Error Correction
FET	Field-effect transistor
FFT	Fast Fourier Transform
FH	Frequency Hopping
FM	Frequency Modulation
FSK	Frequency Shift Keying

-G-

G, Giga	A prefix to a unit denoting a multiple of 10^9 of that unit.
Gnd, GND	Ground
Ground Wave	Follows the surface of the earth and provides reliable signals over short ranges
Group	A programmed collection of station – the programming of the Group is done only at the calling station. It is not necessary for Target Stations to know they are members of a Group.

GLOSSARY (Cont.)

-G- (Cont.)

Group Address — An address used to refer to a Group

Group Call — A call from an individual station to members of a Group – Group members respond in the order in which they are called by the initiating station

Group LQA — A Group Call in which the originating and Target Stations exchange link quality information – the originating station obtains bidirectional LQA information. Target Stations get information only on their receive paths.

-H-

HD — Half Duplex

HDCP — Harris Data Communications Protocol

HF — High Frequency

HSS — High Speed Synchronizer

HSSB — High Speed Serial Bus

Hz — Hertz

-I-

IC — Integrated Circuit

ID — Identification

IF — Intermediate Frequency

I/O — Input/Output

Inverter (NOT gate) — A circuit with one input whose output is high if the input is low, and vice versa.

Ionosphere — An electrically charged (ionized) region of the atmosphere that extends from about 60 km (37 miles) to 1000 km (620 miles) above the earth's surface

Individual Address — An address used to identify a single Target Station – the same character string is used as the Self Address when acting as a Calling Station

Individual Call — A call placed to a single Target Station using an Individual Address – each station must be programmed with the Address and Channel List of the other station before initiating the call

GLOSSARY (Cont.)

-I- (Cont.)

INT	Interrupt
INTLK	Interlock
INTR	Interrupt
I/O	Input/Output
ISB	Independent Sideband
ISF	Initial synchronization frequency

-J-

J	Joules
JFET, JUGFET	Junction field-effect transistor

-K-

K	Thousand
Kbyte	Kilobyte
kHz	Kilohertz
Km	Kilometer(s)
kV	Kilovolt(s)
KVA	Kilovolt Ampere(s)
kW	Kilowatt(s)

-L-

LCD	Liquid Crystal Display
LED	Light-Emitting Diode
LF	Low Frequency
Link Quality Analysis (LQA)	A measurement of the quality of signals between two or more HF radio stations
Listen Before Transmit (LBT)	A feature which samples the incoming signal before transmitting – if ALE traffic is detected, the unit steps to the next logged channel without transmitting

GLOSSARY (Cont.)

-L- (Cont.)

LLSB	Lower Lower Sideband
LO	Local Oscillator
LOS	Line of Sight
LP	Low Pass
LPC	Linear Predictive Coding
LPD	Low probability of detection
LPI	Low probability of intercept
LRU	Line Replaceable Unit
LSB	Lower Sideband
LSD	Least Significant Digit

-M-

m	Milli. A prefix to a unit denoting a submultiple of 10^{-3} of that unit.
M	Meter or mega. A prefix to a unit denoting a multiple of 10^{6} of that unit; a prefix used in computing to denote a multiple of 2^{20}.
mA	Milliampere(s)
Manual Call	A call in which the channel is selected by the user
Mbyte	Megabyte
MDM	Modem; Modulate/Demodulate
MF	Medium frequency
MHz	Megahertz
MIC	Microphone
Micro	Symbol υ. A prefix to a unit denoting a submultiple of 10^{-6} of that unit.
mili	U.S. syn. for thousand
MIL-STD	Military Standard
mm	Millimeter(s)
Mod	Modification, Modulated

GLOSSARY (Cont.)

-M-(Cont.)

MOS	Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
ms, msec	Millisecond
MSDS	Material Safety Data Sheet
MTBF	Mean Time Between Failure
MTBR	Mean Time Between Replacement
Mux	Multiplex, Multiplexer

-N-

n	Nano; a prefix to a unit denoting a submultiple of 10^{-9} of that unit.
NAND gate	A circuit with two or more inputs and one output, whose output is high if any one or more of the inputs is low, and low if all the inputs are high.
NB	Narrowband
NC, N.C.	Normally Closed
N/C	Not Connected
Net	A programmed collection of stations – the Net must be similarly programmed in all Net members
Net Address	An address used to identify members of a Net
Net Call	A call from an individual station to members of a Net – each Net member is assigned a response slot. All stations in the Net must be programmed with Network information.
Net LQA	A Net Call in which the originating and Target Stations exchange link quality information – the originating station obtains bidirectional LQA information. Target Stations get information only on their receive paths.
Ni-Cd	Nickel cadmium
NO, N.O.	Normally Open
NOR gate	A circuit with two or more inputs and one output, whose output is high if and only if all the inputs are low.
NPN	Negative-Positive-Negative (transistor)

GLOSSARY (Cont.)

-O-

O&M	Operation and Maintenance
O&R	Operation and Repair
O.C.	Open Circuit or Open Collector
OEM	Original Equipment Manufacturer
Op Amp	Operational Amplifier
OR gate	A circuit with two or more inputs and one output whose output is high if any one or more of the inputs are high.

-P-

PA	Power Amplifier
PC	Printed Circuit
PCM	Pulse Code Modulation
PEP	Peak Envelope Power
pF	Picofarad
PIV	Peak Inverse Voltage
PLL	Phase-Locked Loop
PN	Pseudorandom number
PNP	Positive-Negative-Positive (terminal)
POR	Power-On Reset
P-P	Peak-to-Peak
PPC	Peak Power Control
PROM	Programmable Read Only Memory
PS	Power Supply; Program Space
PSK	Phase Shift Keying
Pt Pt, Pt-Pt	Point-to-Point
PTT	Push to Talk
PWB	Printed Wiring Board

GLOSSARY (Cont.)

-Q-

QTY	Quantity
Queued LQA	An Individual, Net, or Group LQA that is repeated at operator-specified intervals

-R-

R, RG	Receiver Circuit: Receive, Receive Ground (from teletype)
RAD	Random Access Data
Radio Silence	A feature which prevents response to incoming calls or LQA requests
RAM	Random Access Memory
RCU	Remote Control Unit
RCV/RX	Receive
RCVR	Receiver
RD	Read
RDY	Ready
REC	Receptacle
RF	Radio Frequency
RFI	Radio-Frequency Interference
RLPA	Rotatable Log Periodic Antenna
RMM	Read-Mostly Memory
RMS	Root Mean Square
ROM	Read-Only Memory
RTC	Real-Time Clock
RTN	Return
RTS	Request to Send
RTTY	Radio Teletype
RTU	Remote Terminal Unit

GLOSSARY (Cont.)

-S-

S, SG	Send Circuit, Send Ground (to teletype)
SA	Spectrum Analyzer
SB	Sideband
Score	A rating of overall channel quality
Selective All call	An All Call made to all stations whose addresses end in the same character
Selective Any call	An Any Call made to all stations whose addresses end in the same character
Selective Calling	Calls made to a subset of the stations in a system. See Selective All Call, Selective Any Call, Double Selective Any Call, and Wildcard Call
Self Address	An address used to identify a Calling Station – a station may have more than one Self Address. The same character string is used as the Individual Address when receiving calls as a Target Station
SINAD	A ratio of (signal + noise + distortion) to (noise + distortion) used to measure the signal quality of a communication channel – SINAD is commonly used to evaluate the ability of a channel to pass voice traffic
Skywave	Signals are refracted by the reflection layer of the ionosphere
SMD	Surface Mount Device
SNR	Signal-to-Noise Ratio
SOM	Start of Message
Sounding	An LQA technique which involves sending a one-way message on all channels programmed for a Self Address – target Stations establish channel rankings based on received signal quality
SSB	Single Sideband
SWR	Standing Wave Ratio
SYNC	Synchronous

-T-

Target Station	A station called by a Calling Station
TDQPSK	Time Differential Quaternary Phase Shift Keying
TGC	Transmitter Gain Control

GLOSSARY (Cont.)

-T- (Cont.)

T/R	Transmit/Receive
TT	Teletype
TTL	Transistor-Transistor Logic
TT VFT	Teletype Voice Frequency Tone
TTY	Teletype
TX	Transmit

-U-

u	Micro
uF	Microfarad
UHF	Ultra High Frequency
USART	Universal Synchronous/Asynchronous Receiver Transmitter
USB	Upper Sideband
UUSB	Upper Upper Sideband
UUT	Unit Under Test
uW	Microwave

-V-

V	Volt
VA	Volt-ampere
Vac	Volts, Alternating Current
VCA	Voltage Controlled Attenuator
VCO	Voltage Controlled Oscillator
VCXO	Voltage Controlled Crystal Oscillator
VDC, Vdc	Volts, Direct Current
VDU	Video Display Unit
VECT	Vector
VF	Voice Frequency

GLOSSARY (Cont.)

-V- (Cont.)

VFO	Variable Frequency Oscillator
VFR	Voice Frequency Repeater
VHF	Very High Frequency
VLF	Very Low Frequency
VOM	Volt-Ohm-Meter
VOX	Voice Operated Transmitter Key
VSWR	Voltage Standing Wave Ratio

-W-

W	Watt(s)
Wildcard Call	A feature which allows substitution of a wildcard character (?) for alphanumeric characters in Addresses used in making Selective Any Calls – Wildcard Calls permit Selective Calling based on Address similarities other than the last two characters
WRL	Wire Run List

-X-

XCVR	Transceiver
XMT	Transmit
XMTR	Transmitter

-Z-

Zeroize	A command sequence which erases all programmed channel parameter and option settings

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