DATONG ELECTRONICS LIMITED

Spence Mills, Mill Lane, Bramley,
Leeds LS13 3HE. England.
Telephone: 0532 552461

SERVICE INFORMATION - MODEL ANF

THE CIRCUIT AND SERVICE INFORMATION SUPPLIED IS CONFIDENTIAL AND FOR USE BY DATONG AGENTS ONLY

To be read in conjunction with the product data sheet and the user instructions.

General Description

Model ANF uses the MF10 switched capacitor filter chip as its basic filtering unit. This chip contains two identical 2-pole state-variable filter sections, both of which have a centre frequency which is determined by an external clock signal (at CMOS logic levels). In Model ANF the clock frequency is 100 times the filter centre frequency.

Each of the two filter sections simultaneously provides the following output signals: low-pass, band-pass, and notch. In the CW mode the two sections are used in cascade to give a filter with variable centre frequency but fixed bandwidth; that is, the audio output signal passes through both sections.

In the notch mode the two sections are used differently. The first provides the notch output signal directly. Its low-pass output is then used to feed the input of the second filter. It is the second filter which provides the AFC.

Comparison of the low-pass and notch outputs of the second filter in a phase-sensitive detector gives a DC control voltage which is then used to vary the clock frequency of the filter chip. The result is that the filter tracks any signal which is within the notch. The system relies on the excellent match between the filter sections. Since these are clocked by the same signal their centre frequencies are precisely the same under all tuning conditions.

Because the second filter sees only the signal passed by the first the control system sees only a relatively noise-free signal and this makes the filter able to lock well even in the presence of strong other signals.

A second phase sensitive detector is used to compare the phase of the input signal to the first filter with that of the low-pass output of the second filter. The result is a voltage proportional to the level of the signal (if any) within the filter pass-band. This output drives a comparator whose output is used as a logic level to indicate the "locked" condition.

When the filter is not locked the loop integrator is converted to a linear sawtooth sweep generator which sweeps the filter frequency back and forth over its full range. When lock is signalled, the sweep stops and the sweep circuit reverts to being the loop

integrator.

The signal-to-noise ratio of switched capacitor filter chips is poorer than ordinary op. amp.-type filters. This tends to make the sweep audible as a slight whistle at low input volume levels. A special feature of Model ANF is that this effect is avoided by placing the complete filter circuit within a compandor circuit (NE571). This is used in a configuration which gives a constant signal level into the filter. The result is that no matter what the input level applied to the filter, the filter and its control circuitry always see the same signal, therefore the results with the filter are always equally good.

Circuit Description

Refer now to the circuit diagram. Signal input goes via C34 into pin 5 of the NE571 (this is a virtual earth point). The compressor output is from pin 7 and this goes to the input of the MF10 chip (pin17, also a virtual earth point).

Clock signal for the MF10 comes from the voltage controlled oscillator (VCO) in a CD4046 phase lock loop chip (IC1). VR1 and VR2 set the upper and lower tuning limit for the VCO. The phase sensitive detector which controls the tuning is within the 4046 and is fed with logic signals via the limiting amplifiers made from IC7a, IC7b, and IC6a. The control loop for the frequency control is completed via an integrator whose time constant components are R7/C7/R8. The actual op. amp. used in the integrator is half the LF353 together with IC6e and IC6f.

When the system is locked IC2c (one gate of a CD4066) is open circuit and R11 effectively disconnected. When lock occurs however,R11 is connected and the Schmidt trigger formed by IC6c and d closes a positive feedback loop which converts the loop integrator into a sweep voltage generator with the important property that its output ramps right up to Vcc and down to ground potential.

IC7c (an exclusive OR gate) is used as a full wave phase sensitive detector to detect the presence of lock. IC2d is used to raise the time constant for the post detection smoothing circuit when lock has been achieved. This reduces the lock time of the system considerably.

Frequency indication is via the LM3914 chip (IC10) and this is fed with a direct voltage proportional to the filter's centre frequency. This comes from a frequency-to-voltage convertor based on IC2a and IC2b.

Special Points

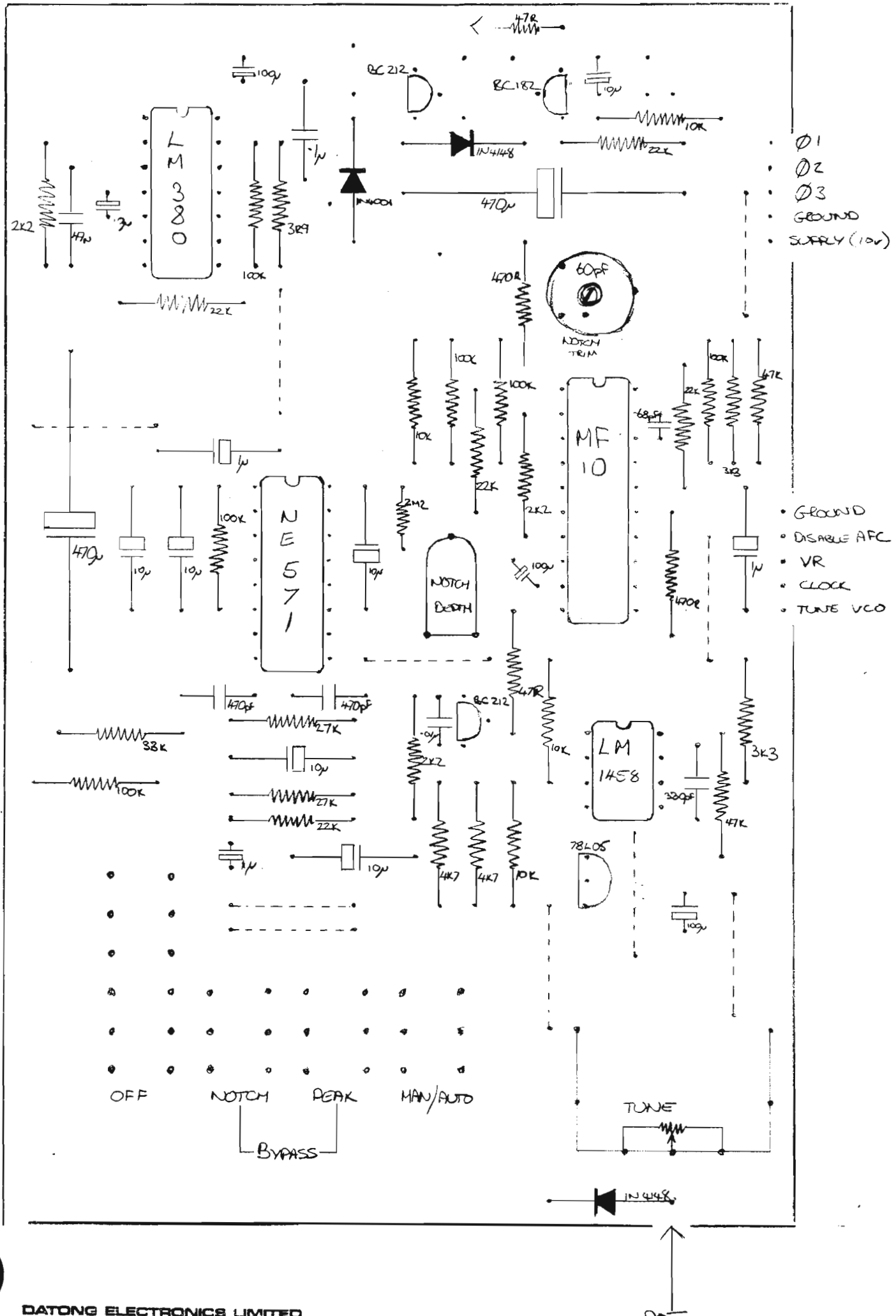
Although the two filter sections are very well matched in the MF10 a slight trim adjustment is still needed in order to get the

best possible notch depth. This is provided by VR5.

When the filter is used for CW it is best not to use the compandor because it is difficult to optimise its time constant for fast pulses. The compandor is therefore disabled in the manual peaking mode (ie CW) by diode D4.

When the notch is tuned manually the automatic tuning system is still connected but only to a very much reduced extent. This gives a small pull-in range to aid in fine tuning, but not so much that the filter might tune itself to the wrong tone. The amount of pull-in is determined by the relative size of VR6 and R13. All trace of auto-tuning is disabled (via D1) when using the manual peaking mode (CW).

The righthand LED in the display is used both for the frequency display and to indicate the "locked" condition.



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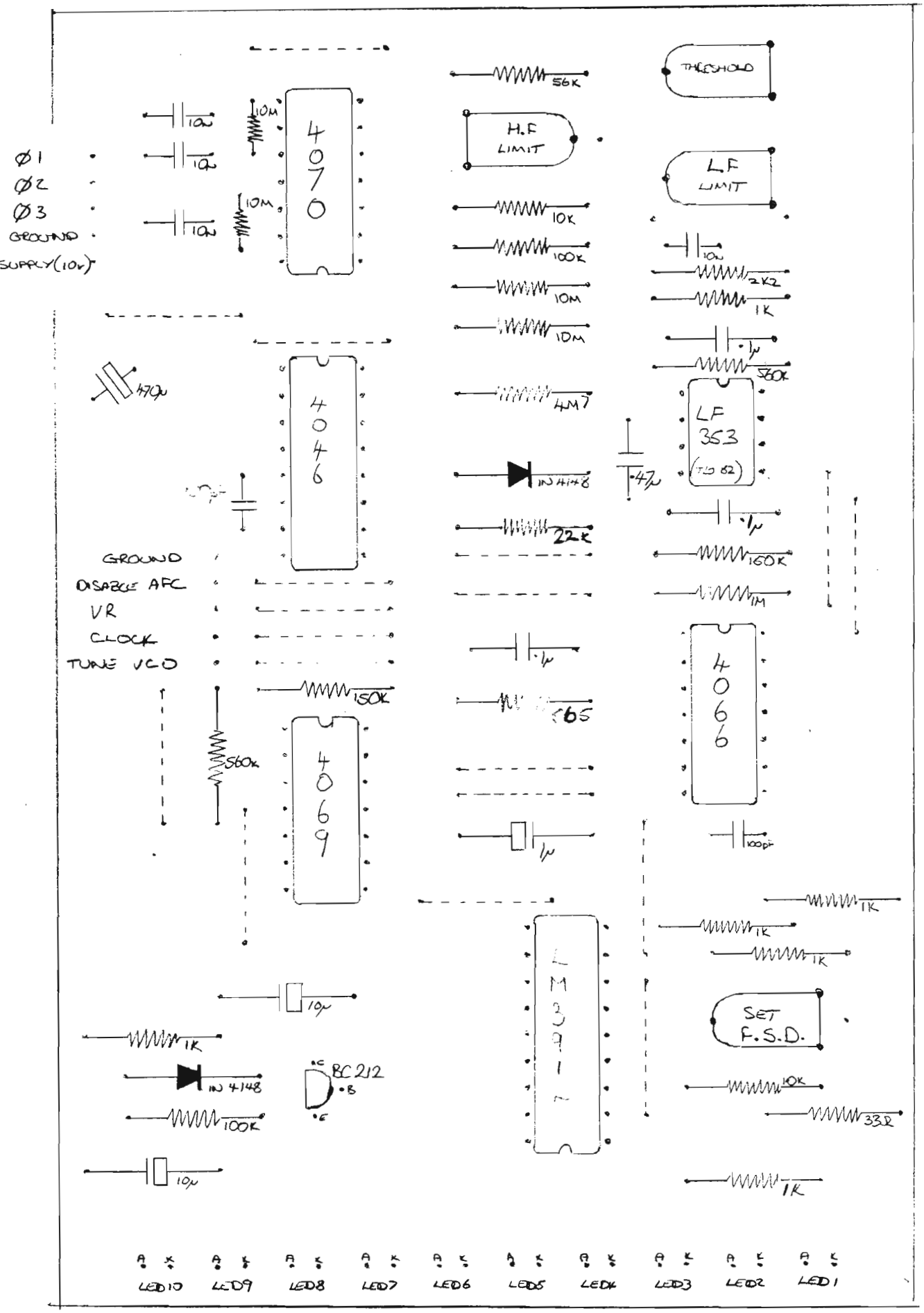

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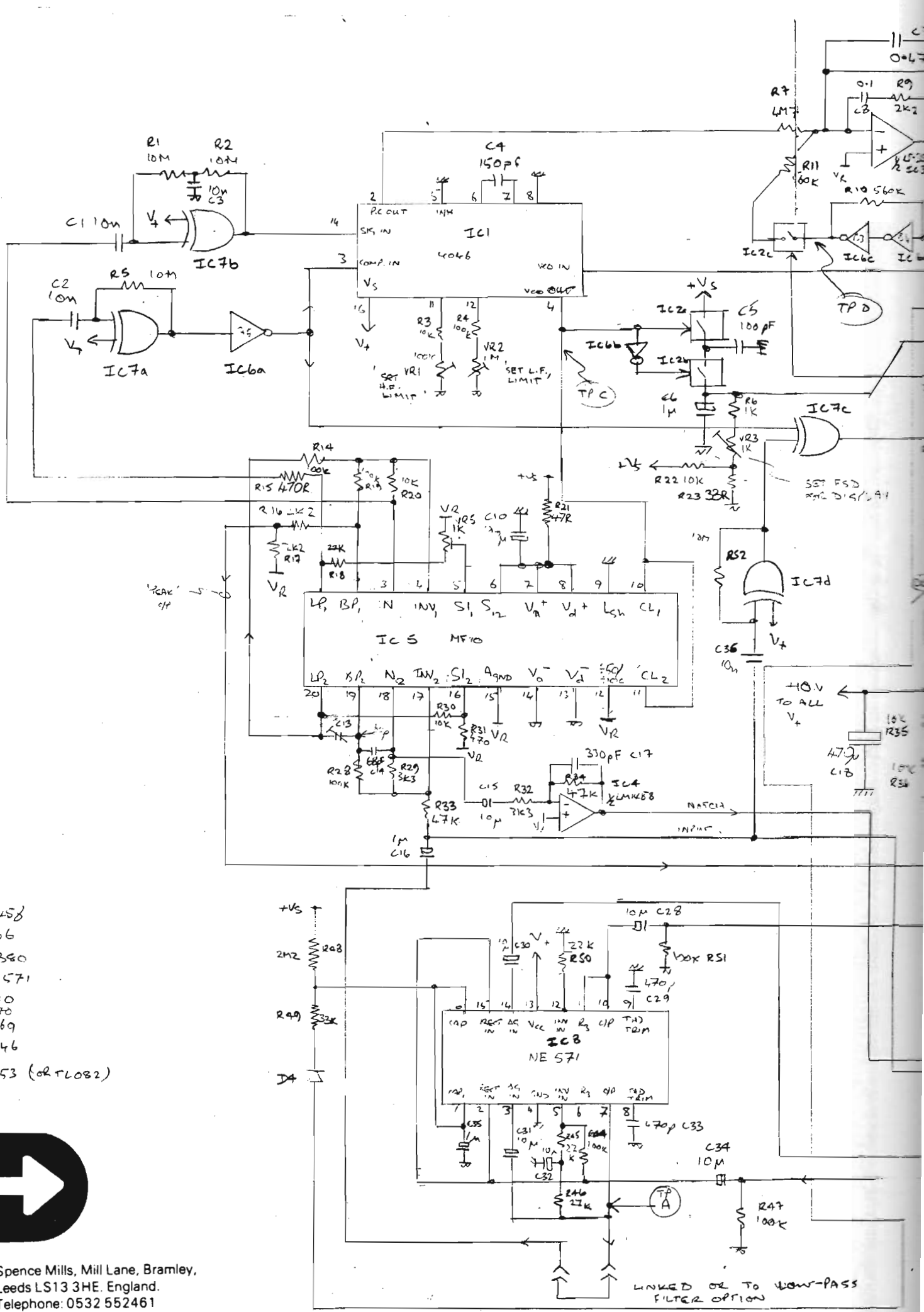

1 LM1458
1 4066
LM360
NE571
MF10
4070
4069
4046
1 LF353 (OR TL082)

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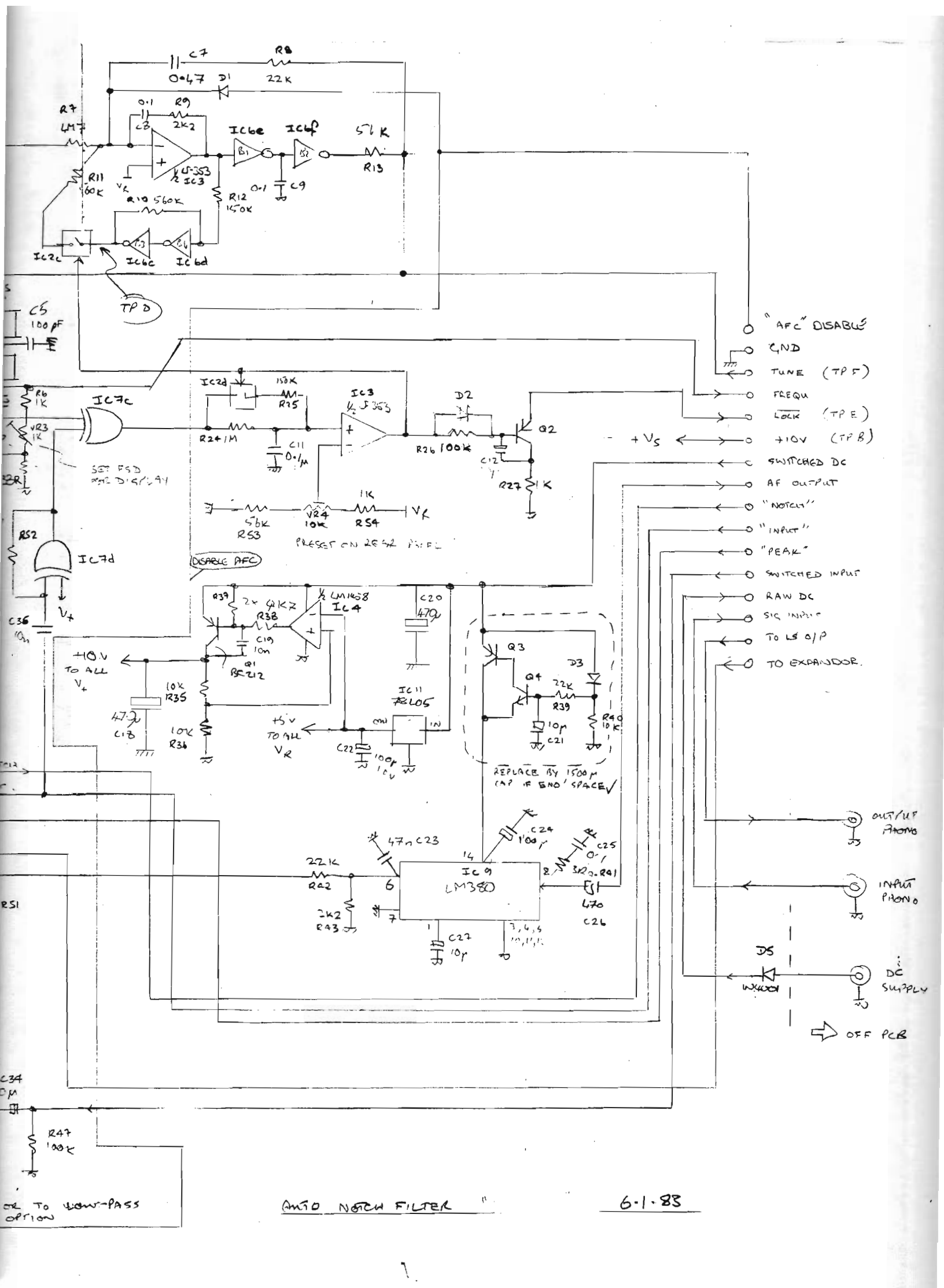
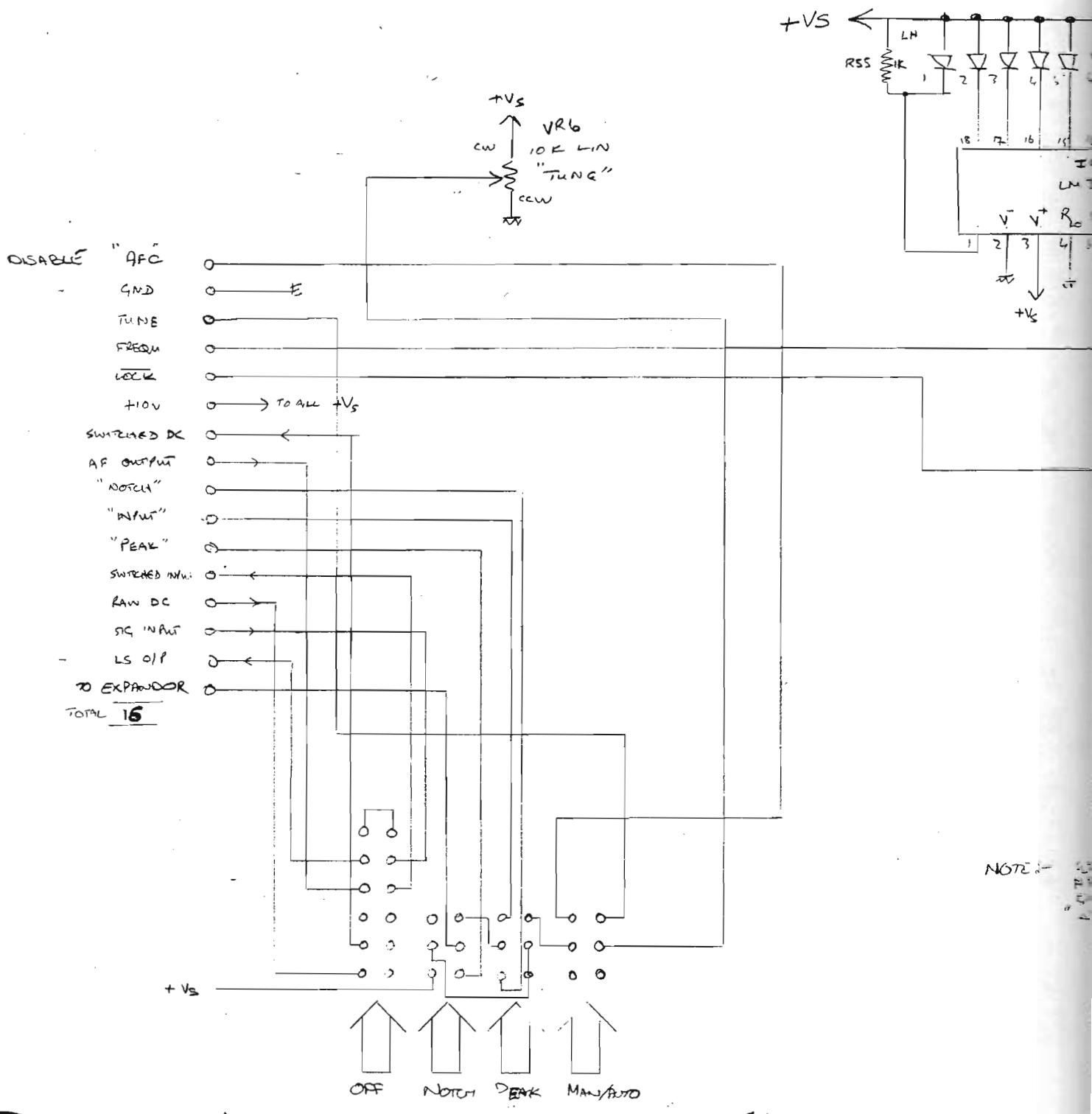

C7
0·47
D1
R8
22K
0·1
C8
R9
2K2
R7
4M7
IC6e
IC6f
57K
R13
R11
560K
R10 560K
R12
150K
0·1
C9
IC2c
IC6c
IC6d
TP D
C5
100pF
IC2d
150K
R25
IC3
½ LF353
D2
Q2
R6
1K
IC7c
VR3
1K
R24 1M
C11
0·1µ
R26 100K
C12
R27 1K
SET FSD AND DISPLAY
1K
R53
56K
VR4
10K
R54
VR
PRESET ON REAR PANEL
R52
IC7d
DISABLE AFC
C36
10µ
V+
R39
2x 64K2
R38
IC4
½ LM1458
C19
10n
C20
470µ
Q1
BC212
+10V TO ALL V+
10K
R35
47µ
C18
10K
R36
+5V TO ALL VR
IC11
4066
C22
100µ 10V
Q3
Q4
D3
22K
R39
10µ
C21
R40
10K
REPLACE BY 1500µ CAP IF END SPACE
47n C23
C24
100µ
C25
0·1
22K
R42
2K2
R43
IC9
LM380
5Ω3 R41
470
C26
C27
10µ
3,4,5
10,11,12
"AFC" DISABLE
GND
TUNE (TP F)
FREQU
LOCK (TP E)
+10V (TP B)
+VS
SWITCHED DC
AF OUTPUT
"NOTCH"
"INPUT"
"PEAK"
SWITCHED INPUT
RAW DC
SIG INPUT
TO LS O/P
TO EXPANDOR
OUTPUT PHONO
INPUT PHONO
DS
IN4001
DC SUPPLY
OFF PCB
C34
10µ
R47
100K
OR TO LOW-PASS OPTION
ANTI NOTCH FILTER
6·1·83



AUTO NOTCH FILTER

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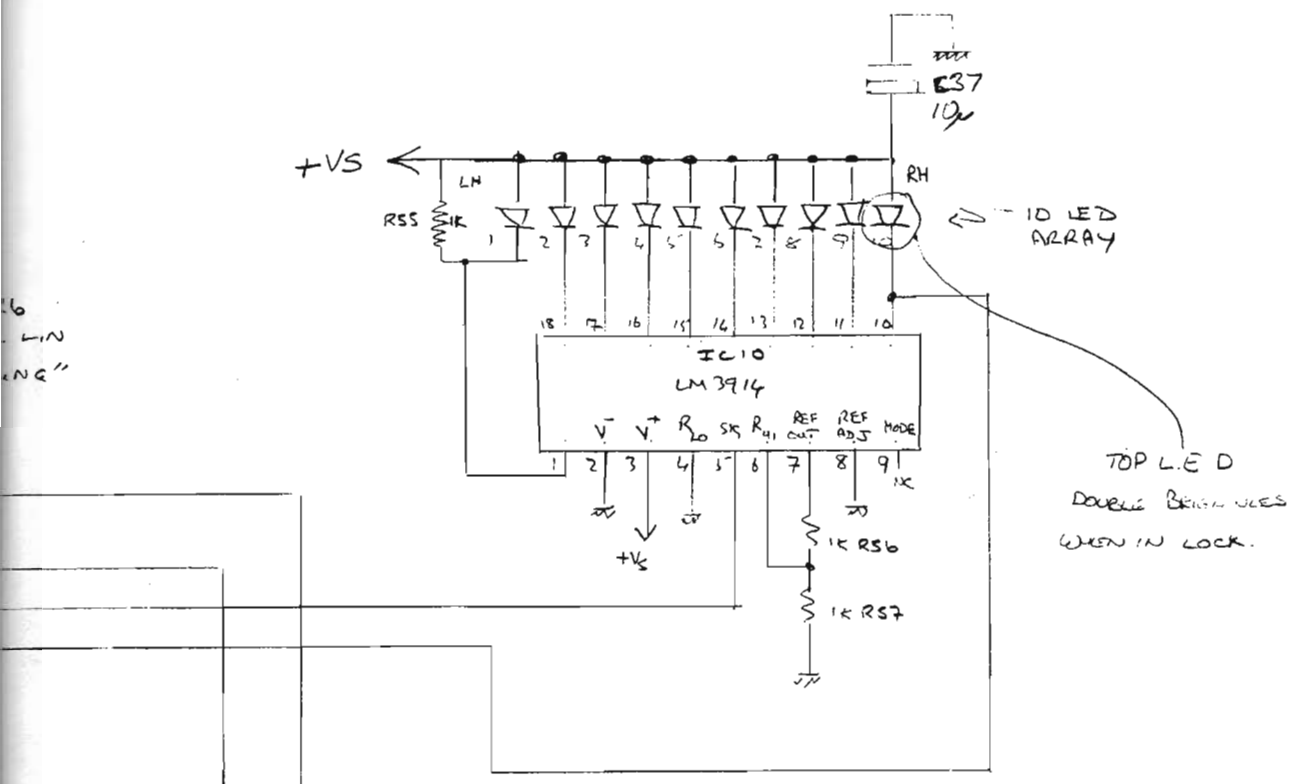

NOTE:- WHEN IN MAN MODE A.F.C. TO PEAK IS DISCONNECTED TO STOP "WARBLING".

MAN/AUTO

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