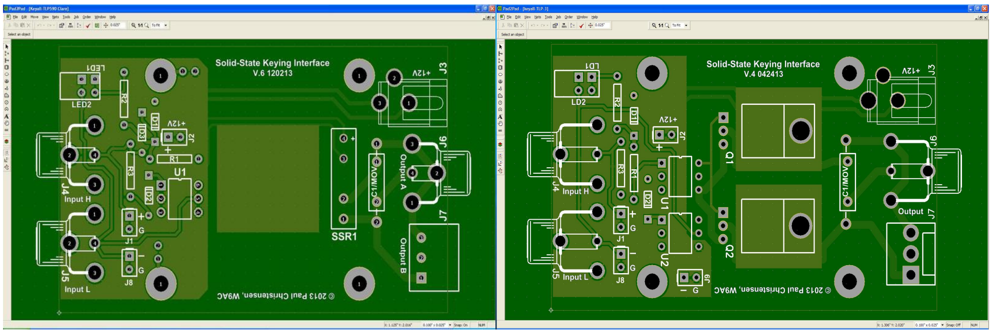
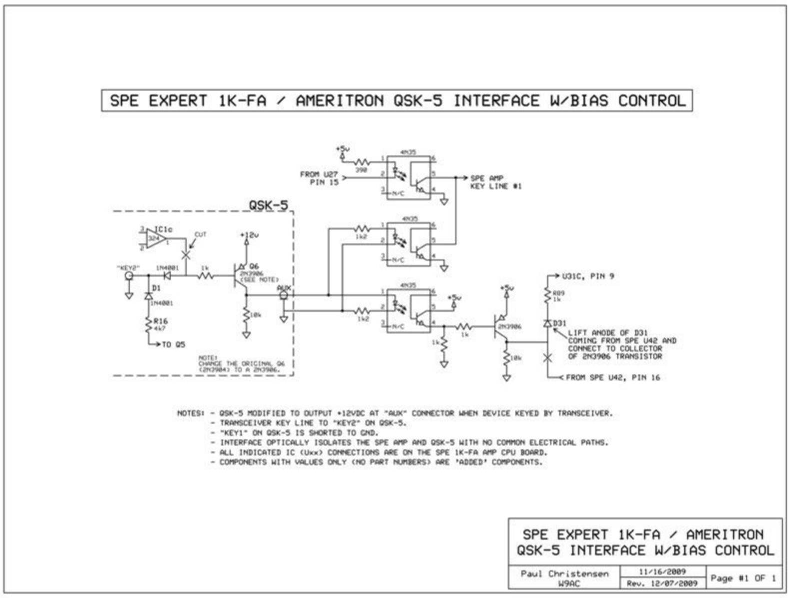


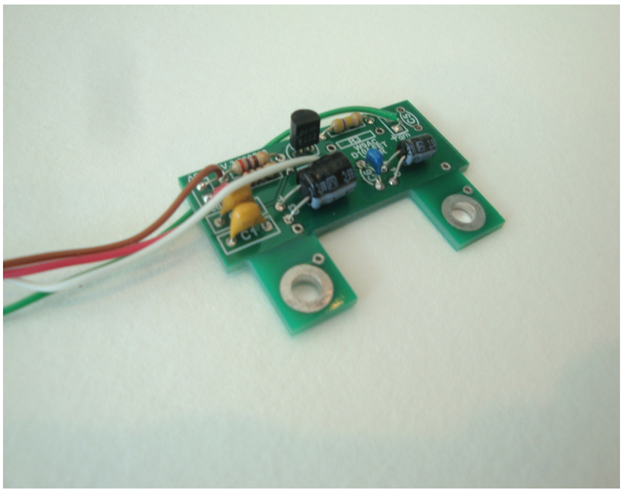
SPE 1K-FA QSK MODIFICATION

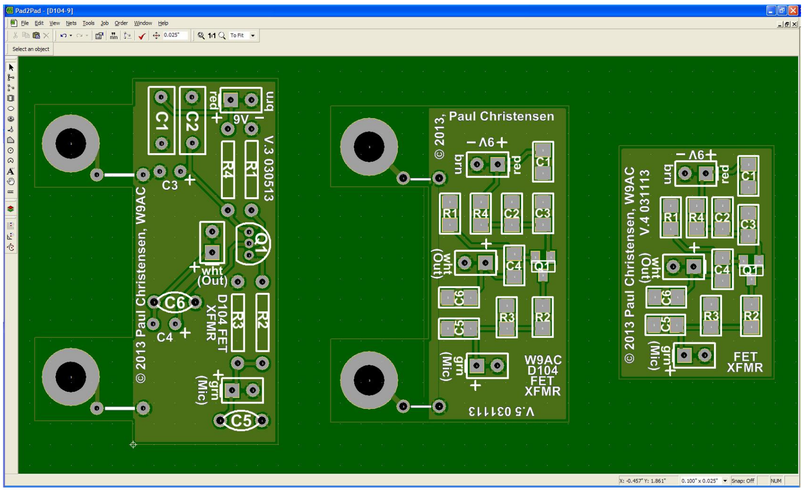
After measuring the SPE amp's T/R time, it is not QSK compatible, although SPE appears to have addressed the problem with newer production amplifiers. A modified Ameritron QSK-5 PIN diode switching unit now controls the amp's T/R and MOSFET bias functions. Control logic between the SPE and QSK-5 is optically isolated. Switch time was reduced from 16ms to under 4ms and hot-switching is eliminated. A schematic of the QSK-5 and SPE bias modification is shown here:



ASTATIC D104 MODIFICATIONS - D104 PREAMP - D104 BUFFER CIRCUITS

HIGH PERFORMANCE ASTATIC D104 FET TRANSFORMER CIRCUIT





Three versions of the Astatic D104 FET Transformer Circuit appear above (with schematic below) and all are designed to work with a 9V battery -- or any transceiver where +8V is available at the mic connector. The circuit board to the left measures 1.75" x 0.70" and is slightly smaller than the original 2-transistor board. The two extended mounting tabs make it a direct drop-in replacement into the D104 microphone. The board in the middle is a SMD/SMT version that also uses Astatic mounting tabs. The board to the right uses surface-mount (SMD/SMT) components and is about the size of a postage stamp. This is a universal FET Transformer Circuit that can be dropped into any crystal microphone base including those made by Astatic, Turner, and Shure. In all three board versions, a ground plane pour is used to assist with RFI mitigation.

Like all crystal mic elements, the D104 performs best when the load impedance is significantly higher than its source impedance - especailly when the load impedance is mostly resistive. A typical crystal cartridge's source impedance is highly dependant on its internal capacitive reactance with equivalent series capacitance values being in the range of 1000pF - 2400pF. By lightly loading the crystal element with the extremely high input impedance of the JFET's gate, the D104 can attain reasonably good low-frequency response to approximately 80 Hz -- approaching the quality of a dynamic broadcast microphone.

If the stock D104 base contains a 2-transistor "power mic" circuit, it should be completely removed with substitution of the FET transformer circuit. In computing the input impedance of the old "power mic" pre-amp, I found that it is approximately 470K -- still too low for the attributes of the crystal cartridge if one desires a low-end response down to 100 Hz..

The SMD boards were designed after trying to source J201 and MPF-102 FETs in the traditional thru-hole style case. The major semiconductor manufacturers who once mass-produced these transistors in TO-92 style cases have now "obsoleted" these two components. In fact, even the SMD versions are now in danger of going obsolete. Presently, only **InterFET Corporation** and **Linear Systems** appear to be manufacturing both through-hole and SMD versions of high-performance JFETs.

Be careful when sourcing any semiconductor. The components stated here are widely available on the Asian market but when making a purchase through many on-line retailers, it's not possible to trace the supply chain of the component to its origin. For example, some Toshiba low-noise bipolar transistors are in fact re-labled 2N3904 devices. Unless the purchaser has access to a curve tracer and a means to perform critical noise and frequency response testing, one is left to trust the seller for a clean "chain of custody" between the time of manufacture and point of sale. Because of this, I only purchase semiconductors direct from the OEM or through well-established distributors including Newark, Mouser, Digi-Key, Arrow, AvNet, and Allied. For an interesting perspective concerning the severity of the counterfeit semiconductor market, see the following **report** issued by the Semiconductor Industry Association (SIA).

The FET Transformer is configured as a classic source-follower (common drain) where gain is less than unity. It uses either a J310, MPF-102, or equivalent n-channel JFET transistor. Note that the JFET as a source-follower is self-biased and *does not require* a "leak" resistor (R3) between the gate and circuit ground. However, notice that R3 is shown as an option in the diagram below. R3 can be set to 10 meg in low humidity areas to prevent JFET gate damage from static electricity. Moreover, R3 can be reduced in vaue to deliberately form a simple 6 dB/octave high-pass filter. An R3 value of 100K will result in a -3dB turnover point close to 250 Hz.

Self-bias stabilizes the quiesecent operating point against changes in JFET parameters (e.g.,Idss, gfs, etc.). Here's the idea: Suppose we substitute a JFET with a forward transconductance (gm or gfs) value that's twice as large. Then, the drain current will try to double. But since the drain current flows through R(s), the gate-source voltage V(gs) becomes more negative and reduces the original increase in drain current. A gate voltage equal to 1/4 of V(gs-off) results in drain current equal to approximately 1/2 of Idss. To set-up the mid-point bias "Q point," R(s) is computed simply by taking the *reciprocal of the JFET's forward transconductance value*. This value creates a drain current equal to 1/2 of Idss.

With some difficulty, transconductance can be measured. In the alternative, simply research the range of gm or gfs values from the manufacturer's data sheet and compute the geometric mean. For the Motorola MPF-102, the computed R(s) value is approximately 270 ohms. This becomes the driving source impedance to the transceiver. And so, the input impedance of the FET transformer circuit is greater than 10-megohm while the output impedance is less than 300 ohms. Within limits, R1 can change in value based on the JFET's gfs value. As the value is lowered, one benefit is the source Z decreases, but at the expense of greater current and a shift of the Q point along the FET Transformer's bias curve. Keep this in mind when powering the circuit from a 9V battery.

Output coupling capacitor C4 is 4.7 uF and is adaquately large enough to pass a low-end response below 100 Hz as the typical mic input impedance of most modern transceivers is > 1K-ohm. Click **here** for a display of the LTSPICE simulator output.

The FET Transformer Circuit is an excellent choice when using a crystal mic element on a long mic cable run into the grid of an audio triode, for example. Many owners of older vacuum tube-based transmitters incorrectly assume that the extremely high input impedance of the control grid is enough to offset the crystal element's Hi-Z source impedance. However, a recipe for disaster is set up any time a high parallel capacitance exists across a Hi-Z source impedance. Since the source Z of the crystal element is mostly a capacitive reactance, the cable capacitance creates a uniform voltage divider across all audio frequencies. To mitigate the effect of distributed cable capacitance from the D104's Hi-Z mic element, the FET Transformer Circuit will convert the Hi-Z mic output to a Lo-Z source at a point where it matters most: *the input end of the mic cable*. In doing so, the low output impedance from the FET Transformer is set up by R(s) and swamps out the detrimental attenuation caused by a combination of cable capacitance in parallel with a series capacitive source. A low driving source Z also minimizes noise pick-up on the mic line.

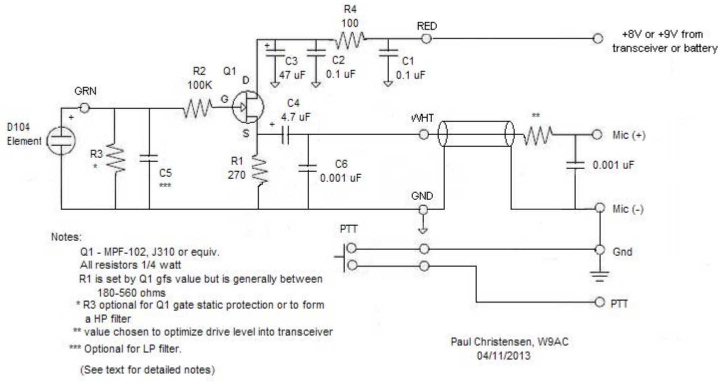
The D104's crystal element and mechanics have evolved little since its first introduction in the 1930s. However, during its 70+ year manufacturing history, the "grip-to-key" arm was added in the 1950s, and the 2-transistor amplifier in the TUG8/TUG9 base style was added in the late '60s. Finally, the Silver Eagle version included an additional PTT arm in the mic base. Below, I show several D104 wiring diagrams for use with the FET Transformer circuit. This is not an all-inclusive set of diagrams. For example, I do not yet have a wiring diagram of the non-amplified D104 with the grip-to-key arm. Also, very early D104s have no PTT switching whatsoever: the mic cable is connected to the mic element, runs through the stem and out the base to the transmitter. So, some brain power will be required when using the FET Transfomer in these D104 variations.

When considering cost, circuit simplicity and performance, it's difficult to beat the FET transformer circuit. However, for those interested in obtaining gain from the circuit, see the MOSFET and Op-Amp variations of the FET transformer circuit shown further down the page. In each of these configurations, the existing Astatic 5K pot may be used for level control.

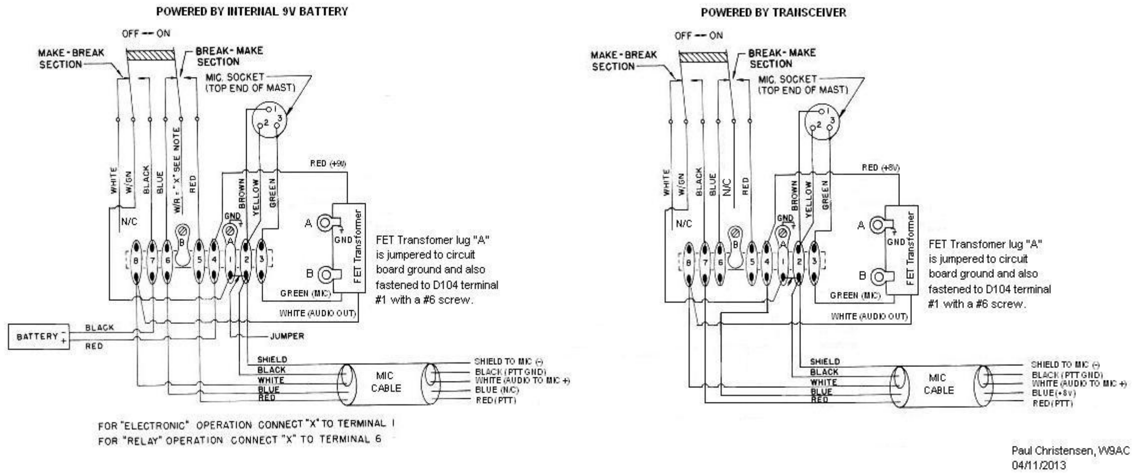
Specifications:

Input impedance: Greater than 10 megohm.
Frequency response: +/- 0.5 dB, 50 Hz - 10 kHz (incl. crystal element equivalent source Z of 1000pF in series with 10K resistance);
Audio filtering: On-board provision for optional 6dB/octave HP filter by adding two components;
Output impedance: Less than 300 ohms and will drive both Lo-Z and Hi-Z terminations;
THD, ref. 1 kHz at 0 dBu input level: 0.1%;
IMD (SMPTE): 0.15% at 0 dBu input level;
SNR, no weighting, > -80 dB ref. 0 dBu;
Gain: Less than unity as a source-follower. Generally, no amplification required as the high-output-voltage crystal element is completely unloaded;
Output level: Adjustable with external control as shown on our schematic and circuit description. The existing Astatic 5K potentiometer may be used to control output level;
Powered from +5V to +15V and only 2 mA of idle current with the J310 and MPF-103; approx. 1 mA with the J201.

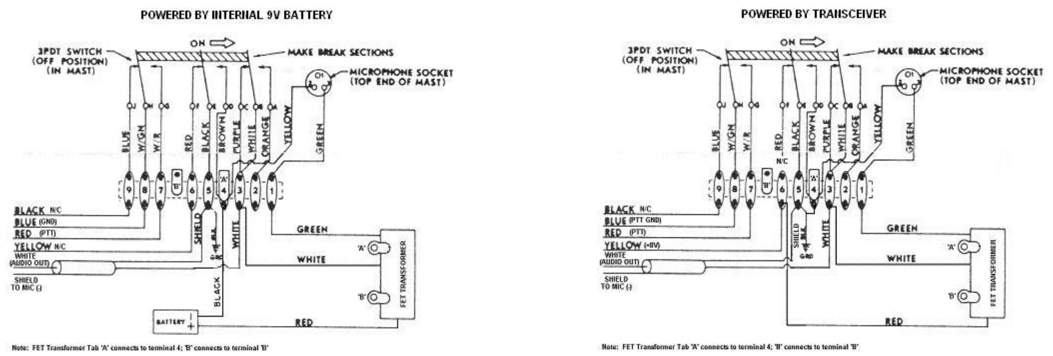
D104 FET TRANSFORMER SCHEMATIC DIAGRAM



D104 FET TRANSFORMER WIRING DIAGRAM
(EARLY AMPLIFIED VERSION)



D104 FET TRANSFORMER WIRING DIAGRAM
(LATE AMPLIFIED VERSION)



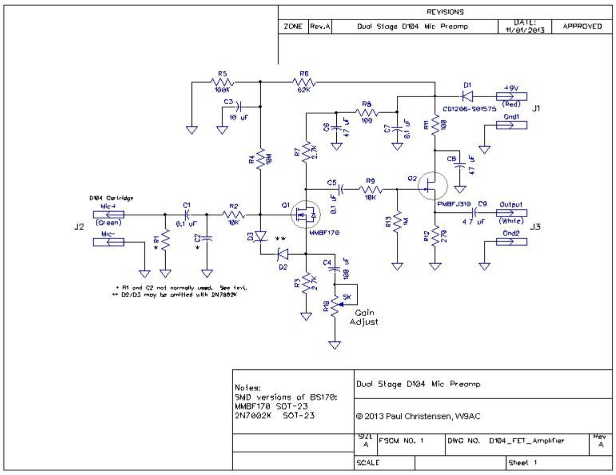
2-STAGE D104 MOSFET TRANSFORMER/AMPLIFIER

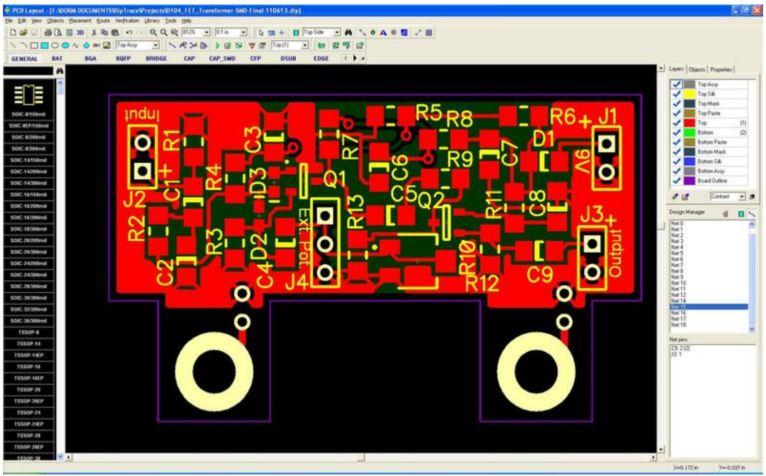
The circuit shown below is a 2-stage MOSFET preamp for the Astatic D104 and makes use of the existing 5K base-mounted level control - or an on-board Bourns sub-minitaure potentiometer. The first stage sets circuit gain and utilizes a BS170 MOSFET (Q1) in a common-source configuration, followed by a J310 JFET (Q2) as a source-follower for driving Lo-Z terminations. As the component count is increased over the simpler, one-stage source-follower, this board uses SMD/SMT surface-mount components.

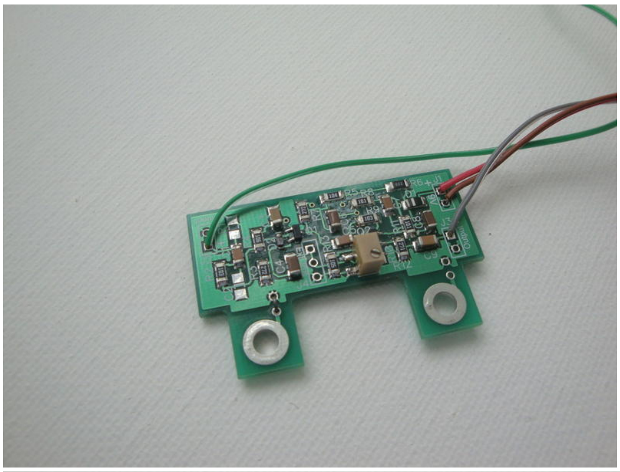
By using fixed bias on the gate of the BS170 MOSFET, the circuit maintains a constant Q point on the FET's load line, regardless of R10's gain setting. Moreover, the noise figure of the amp is not fixed; it will vary only to the extent of needed gain. Although a voltage source is used on the MOSFET gate rather than being self-biased, the input Z is still 10-megohm. Zeners D2 and D3 are used to protect the MOSFET gate from static discharges when using the D104 in low humidity conditions. These diodes may be omitted when using a MOSFET with internal ESD protection -- like the 2N7002K.

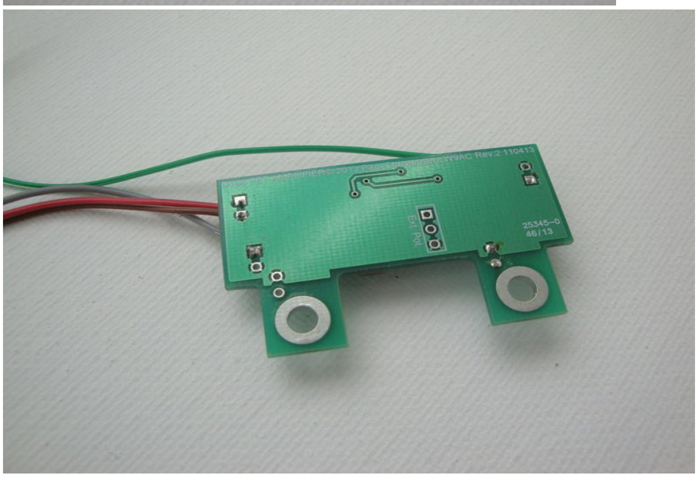
The circuit output Z is set by R12's low value of 270 ohms. As in my previous D104 circuit designs, the power bus is completely decoupled and seperately filtered at the bias voltage divider as well as the drain lead of each stage.

This circuit design taught me a valuable lesson concerning the use of multilayer chip capacitors (MLCC). Note the use of several high-value MLCC caps in both the audio and power supply filtering paths. When using Class II & III (X7R, X5R & Y5V) MLCC types, the voltage coefficient de-rates the effective capacitance value and this can have a disastrous effect on the operation of a circuit. For example, what you think is a 100 uF cap, may be derated down to 10 uF or less as the voltage nears the MLCC's maximum voltage rating. NP0/C0G MLCC caps do not exhibit this behavior but beyond about 0.5 uF, this class of MLCC capacitors don't exist. When a high value capacitor is needed, use an electrolytic type or use it in parallel with the MLCC. Miniature electrolytic SMD versions are plentiful and can be seen in the improved op-amp design of the equivalent circuit shown further down this page. For a detailed look at the effect of capacitor voltage coefficent, see this **document** from NIC Components Corp. In particular, look at the graphs displayed on pp. 6-7.









D104 PRECISION OP-AMP TRANSFORMER/AMPLIFIER

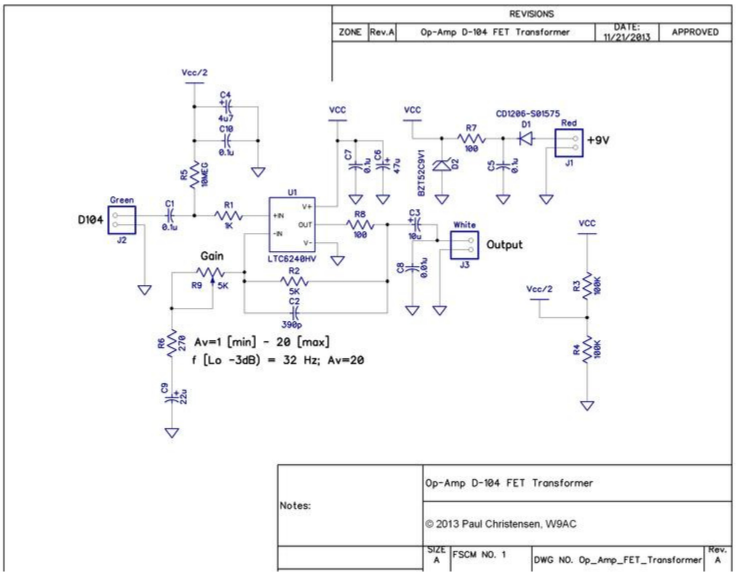
At the suggestion of Jack Smith, K8ZOA, I designed a D104 transformer circuit built around a low input bias op-amp to perform the gain and Z transformation function. It wasn't long ago that when a designer wanted to optimize a circuit based on a given op-amp performance parameter that the performance of other op-amp attributes was sacrificed. Today, there's little sacrifice in audio applications and several manufacturers offer op-amps with superlative noise, distortion, transient, input bias current, and offset voltage characteristics.

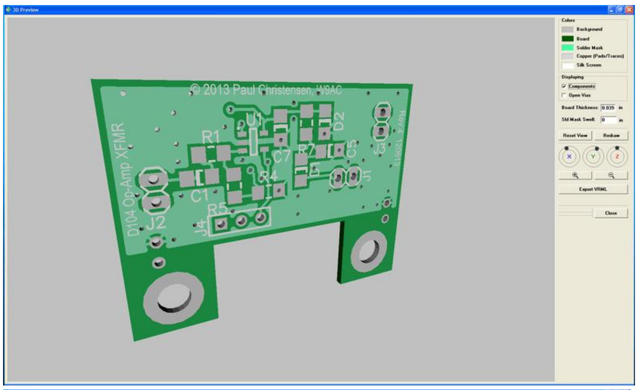
In the circuit shown below, a high performance LTC6240HV op-amp is used. Both the top and bottom PCB layers are evenly populated with SMD components. Because this op-amp has an exceptionally low input bias current of 0.2 pA, a high-value bias injection resistor (R5=10 megohm) can be inserted onto the non-inverting input to bias and stabilize the op-amp at 1/2 of Vcc. The resulting input Z is commensurate with that of the self-biased JFET circuit. Perhaps a decade ago, it would have been a difficult challenge to create a biased Hi-Z op-amp input while trying to preserve some semblance of good low-frequency audio response from the D104's highly reactive crystal element.

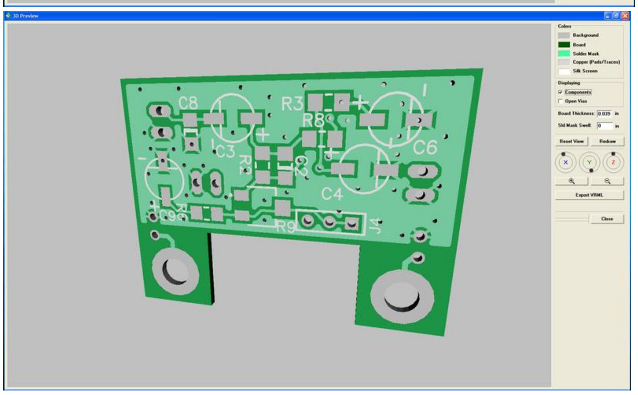
The upper frequency response is mostly limited by the 390 pF feedback capacitor, but only under conditions of gain since the non-inverting input is used. No matter the gain control of a non-inverting input, the output level is not less than unity since the gain equation is Vout = Vin[1+(Rf/Rg)]; where Rf represents the feedback resistance and Rg is the inverting input resistance.

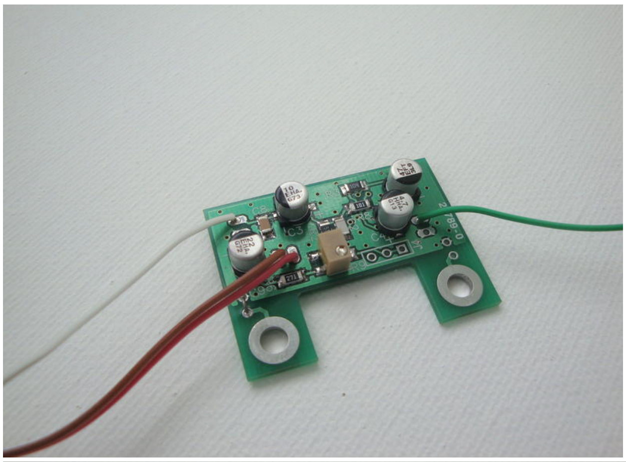
Click **here** for a display of the LTSPICE simulator output. The graph shows worst-case low-end frequency response when the gain pot is set to zero ohms, resulting in maximum gain. The circuit board photos below show a virtual reality image from the PCB software as well as the top and bottom layers of the completed board.

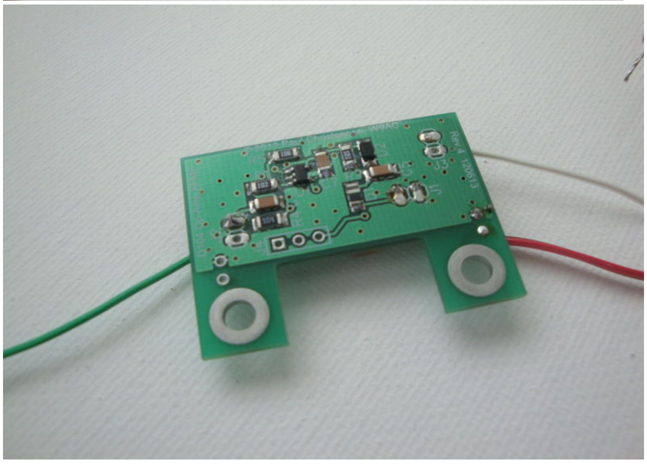
Beginning with the op-amp version of the D104 transformer/amplifier, I am now using extensive "**via stitching**" between top and bottom copper ground plane pours of my new PCB designs. Via stiching generally becomes effective with an increase in frequency relative to board size. Multilayer PCBs, especially when designed for RF, may have many layers of ground; even the signal layers typically have ground flooded on them. These grounds need to be all tied together to keep them from acting like stubs or transmission line segments themselves. Or put another way, they need to be a low impedance at all the operating frequencies of the PCB, otherwise they don't look like ground anymore - they start looking reactive to the signals on them. Rule of thumb: If you space ground vias at 1/8 of a wavelength or less, your ground plane will look and behave like a solid ground.





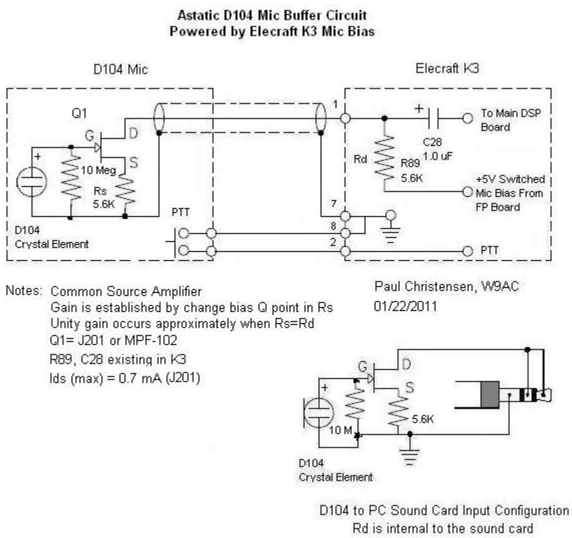






ASTATIC D104 MODIFICATION FOR ELECRAFT K3

Those interested in powering their Astatic D-104 mics from the Elecraft K3 transceiver may be interested in the following common-source buffer circuit. It uses any common n-channel JFET transistor (e.g., MPF-102, J310, J201 or equiv.). The K3 supplies power to the interface through +5V bias injected onto the mic lead. The input impedance of the circuit is 5 Megohm. The output impedance is approximately 5K-ohm and is equal to the JFET's drain resistance. The drain resistor is internal to the K3 as shown. An alternate diagram is shown for interfacing the D-104 microphone into a PC sound card where the card supplies a mic bias voltage.



AMPLIFIER RELOCATABLE POWER TAP (RPT)

I've been thinking about ways to best manage AC power distribution for my desktop amps. Until recently, I've been manually switching power plugs under the operating table. One branch circuit is used, and consisted of a 30A OCPD (breaker) and a run of #10/4 electrical cable to a 30A Twist-Lock wall-mounted receptacle. 4-wire cabling is used since the older Alphas make use of a neutral for the blower.

To simultaneously feed AC power into three amps, I had several choices: (1) add more branch circuits; (2) add a J-box in the wall and split one branch circuit to feed more than one receptacle; or (3) construct a relocatable power tap (i.e., a 240/120V version of a multiple outlet strip). I decided against options 1 & 2 since the house will one day go to a new owner and I didn't want to add even more wall trauma. Further, UL and NEC limits option #2 to 20A circuits. My amps are all legal-limit and 20A service is adequate as the maximum current demand is less than 15A. The #10 cabling to my shack helps to reduce voltage drop losses over an 80 ft run.

Option #3 became the plan but what does UL have to say about 240/120V RPTs? UL 1363 sets the RPT product standard although another UL provision addresses portable power distribution of the type generally found at construction sites. Even though I will not mass-produce these RPTs , I wanted to know how close I could come to making one that is 100% UL 1363 compliant. I got pretty close. In fact, it complies but for the fact that the PVC enclosure has permanent mounting tabs. UL 1363 states that any physical mounting must be effectuated without the use of tools. Typically, we see home RPTs with mounting blocks designed to slip over screw heads so that the RPT is easily attached and removed without the use of hand tools.