Heathkit®

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PACKKIT®

Model HKA-232-3

Technical 595-3999

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Welcome to the Heath family. We believe you will enjoy assembling your kit and will be pleased with its performance. Please read this Consumer Protection Plan carefully. It is a "LIMITED WARRANTY" as defined in the U.S. Consumer Product Warranty and Federal Trade Commission Improvement Act. This warranty gives you specific legal rights, and you may also have other rights which vary from state to state.

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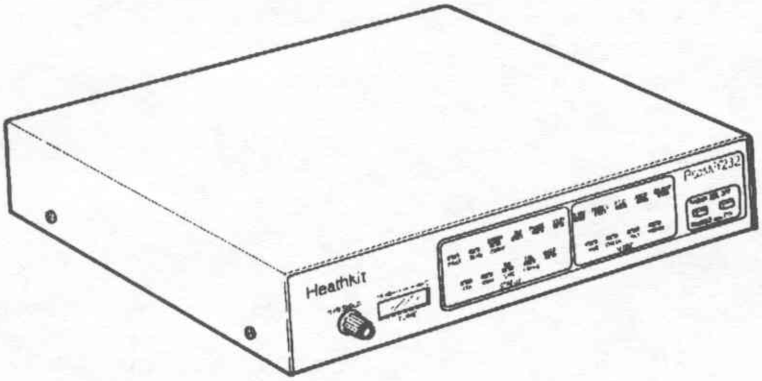
Phillip Lewey

PACKKIT®

Model HKA-232-3

Technical 595-3999



HEATH COMPANY
BENTON HARBOR, MICHIGAN 49022

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INTRODUCTION

The Heathkit PackKit® Model HK-232 is a multimode protocol converter and data controller that interfaces a computer or terminal to an HF or VHF amateur transceiver. On the radio side of the interface, the HK-232 sends and receives Morse, Baudot and ASCII RTTY, black and white facsimile, AMTOR/SITOR and AX.25 packet. An AFSK modem handles most data transfers, while a CW keyer circuit permits on-off transmission. On the terminal side, the HK-232 converts these signals to and from ASCII and transfers the data via an EIA standard RS-232C (CCITT V.24/V.28) serial port. In addition, it can send facsimile data to a printer through a Centronics-compatible parallel interface.

The HK-232 is an "intelligent" device containing a CPU, RAM, and ROM. These circuits control the data flow inside the unit and provide timing and key control to the station transmitter. Also, the computer circuits provide special editing and debugging utilities, along with several programmable options. These options can be stored in battery-backed CMOS RAM, which will retain its contents when the HK-232 is turned off. This permits customizing the unit to the user's terminal configuration, station call sign, and operating characteristics. These characteristics include using the controller for personal communications, or as an unattended repeater, a beacon, or, with the appropriate computer and software, as an electronic bulletin board.

The HK-232 also has a number of hardware features. This includes internal jumpers to configure the unit to transmitters with positive or negative PTT lines, select between the internal modem and an external modem, and enable the optional battery backup. Rear-panel connectors permit interfacing the unit to two transceivers, which can have either a positive or a negative CW keyer circuit. There is also a scope/FSK connector that allows monitoring the received mark/space signals with an oscilloscope and for directly driving an external FSK modulator with the digital signal. On the front panel are LEDs to indicate the operating mode and status of the unit. A bar graph LED indicates relative frequency of the incoming signal. Controls include the power switch, a threshold control, and a switch to select one of two radios.

There are other features that make the HK-232 easy to service. You can access the top of the circuit board by removing six screws and lifting off the top cover. You can quickly signal-trace most analog problems simply by connecting the transmitter output back to the receiver input. The digital circuits are based on a common Z80 design consisting of processor, memory, I/O, and decoders. Static RAMs further simplify the design. In addition, the firmware contains a checksum routine to test the integrity of the ROMs. Plus, it has routines that let you quickly and accurately calibrate the modem frequencies without test equipment. You will only need an oscilloscope or AC voltmeter to adjust the modem output amplitude. You will find this information in the "Disassembly," "Troubleshooting," and "Alignment" sections of this Blue Book.

In addition to disassembly, troubleshooting, and alignment information, this book also contains IC data, circuit board layout, and a circuit description. A visual checks section helps you quickly locate and verify the correct installation of components. The operation section provides enough information for you to effectively bench-test the unit. The specifications and normal operating characteristics sections describe what to expect from the HK-232 and point out some of its idiosyncrasies. The schematic diagram has detailed voltages, pulse measurements, and other useful information.

While this book provides sufficient information to successfully troubleshoot the HK-232 you may want to study the "HK-232 PackKit User Manual," part number 595-3902. This manual provides a complete description of all the commands, detailed operating procedures, and definitions of the protocols associated with facsimile, AMTOR, and packet operation.

SPECIFICATIONS

Modem Characteristics

Operating Modes	Morse, Baudot, ASCII, AMTOR/SITOR, Packet Radio per AX.25, half or full duplex, and WEFAX (Weather Facsimile) with suitable printer.
Demodulator	Limiter-discriminator type, preceded by an eight-pole Chebyshev 0.5-dB ripple bandpass filter.
Receive Bandpass	Automatically switched by operating mode. VHF Packet: Center frequency 1700 Hz, bandwidth 2600 Hz. HF (except CW): Center frequency 2210 Hz, bandwidth 450 Hz. CW: Center frequency 800 Hz, bandwidth 200 Hz.
Modulator	Low-distortion AFSK sine wave function generator, phase-continuous AFSK.
Output Level	5 to 100 millivolts RMS, adjustable by a rear-panel control.

Processor System

CPU	Z-80 microprocessor.
RAM	16 kilobytes CMOS static RAM.
ROM	**48 kilobytes.**
HDLC	**Zilog 8530 SCC.**

Input/Output Connections

Radio Interface	Two five-pin right-angle connectors, two 3.5-mm phone jacks, selectable from the front panel.
Input/Output Lines	Receive audio. Transmit audio. Push-To-Talk (PTT). External squelch input. Ground.
External Modem Connector	Five-pin right-angle connector: TXD, RXD, DCD, PTT, and Ground.
Direct FSK Outputs	Normal and reverse.
Oscilloscope Outputs	Mark (Stop) and space (Start).
CW Keying Outputs	Positive: +100 VDC max, at up to 100 mA. Negative: -30 VDC max, at up to 20 mA.
Terminal Interface	RS-232C 25-pin DB-25 connector.
Serial Input/Output	RS-232C with full handshake (hardware and software). Must use only wires 1 through 8 and 20.
Parallel Input/Output	Eight data lines and three handshake lines available in nonstandard configuration of DB-25 Serial Port.
Terminal Data Rates	Autobaud selection of 300, 1200, 2400, 4800 and 9600 BPS. In addition, the TBAUD command adds 110, 150, 200 and 600 BPS.

Controls and Indicators

Front Panel Controls	Power Switch. Radio Selector Switch. Threshold Adjust.
Indicators	Ten-segment discriminator-type bar-graph indicator for HF tuning. DCD LED (Data Carrier Detect).

Status and Mode Indicators ....

Mode Group	Status Group
BAUDOT	STBY
ASCII	PHASE
PKT	IDLE
MORSE	ERROR/CONV
CHECK	OVER
FEC	TFC/TRANS
ARQ	RQ/CMD
MODE L	CON
STBY	STA
	MULT
	SEND

General

Power Requirements	+13 VDC (12 to 16 VDC) at 700 mA.
Dimensions (overall)	2-1/2"H x 8-1/4"W x 11"D. (6.4 cm x 21 cm x 27.9 cm).
Weight	3 pounds (1.36 kg).

The Heath Company reserves the right to discontinue products and to change specifications at any time without incurring any obligation to incorporate new features in products previously sold.

OPERATION

INTRODUCTION

This part of your PackKit Technical Manual is divided into two sections: "Hardware" and Software". The Hardware section information on how to connect the unit to a terminal and a variety of transceivers. The software section covers operating modes and provides a summary of commands. Due to space limitations, this book only covers the basics. For detailed information, see the "Packet Model HK-232 User Manual", part number 595-3902.

HARDWARE
Controls, Connectors and Indicators

FRONT PANEL

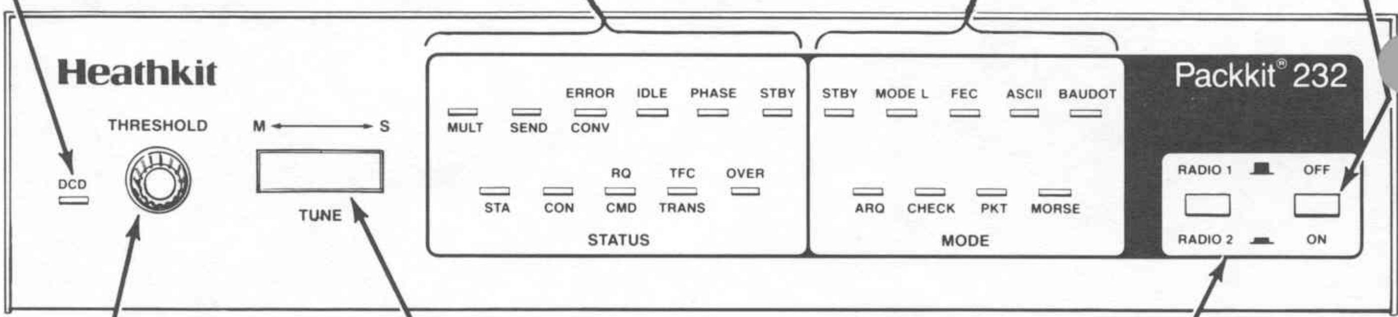
Controls and Indicators

DCD: Data Carrier Detect LED. Lights when the received signal level exceeds the setting of the THRESHOLD control.

OFF/ON: Switches external DC power to the HK-232 on or off.

STATUS: These LEDs indicate the status of the system, signal, and protocols. See "Status Indicator LEDs" for more information.

MODE: These LEDs indicate the operating mode of the HK-232. See "Mode Indicator LEDs" for more information.



TUNE: Indicates the frequency of the incoming AFSK signal. Mark (logic 1) is the lower frequency. Space (loigc 0) is the upper frequency.

RADIO 1/RADIO 2: Selects between one of two transceivers. These radios can both be HF, VHF, or one each.

THRESHOLD: Sets the operating level of the threshold detector circuits. If the received signal exceeds this level, the threshold detector informs the HK-232 that data is present.

Status Indicator LEDs

Note that all markings below the LEDs refer to packet operation, while markings above the LEDs refer to all other modes. The following table describes these indicators from left to right and from top to bottom.

Status LED	Operating Mode	Description
MULT	Packet	Lights when multiple packet connections exist.
SEND	Packet	Lights when the HK-232 is transmitting a packet. (PTT is active.)
ERROR	ARQ	Lights when the AMTOR (AMateur Teleprinting Over Radio) system receives errors from another system.
CONV	Packet	Lights when the system is in the conversation mode.
IDLE	ARQ/FEC	Lights when the AMTOR system sends synchronizing or idle characters.
PHASE	ARQ	Lights when the AMTOR system sends its SELCAL (Selective Call) or phasing signals to another station.
STBY	ARQ	Lights when the AMTOR system is available to answer an ARQ SELCAL from another station.
STA	Packet	The STAtus LED lights when the unit sends a packet but doesn't get an acknowledgement.
CON	Packet	Lights when the HK-232 is connected to another packet radio station.
RQ	ARQ	Lights when another AMTOR station requests a repeat of previous information blocks.
CMD	Packet	Lights when the system is in the command mode.
TFC	ARQ/FEC	Lights when the AMTOR system sends information.
TRANS	Packet	Lights when the the system is in the transparent mode.
OVER	ARQ	Lights when the AMTOR system sends a change-over command to another station.

Mode Indicator LEDs

The following table describes the mode indicators from left to right and from top to bottom.

Mode LED	Operating Mode	Description
STBY	ARQ/FEC	Lights when the system is in the AMTOR ARC or FEC mode.
MODE L	ARQ	Lights when the system is in the AMTOR listen mode.
FEC	FEC	Lights when the AMTOR system is in the Forward Error Correction mode.
ASCII	RTTY	Lights when the system is in the ASCII RTTY mode.
BAUDOT	RTTY	Lights when the system is in the Baudot RTTY mode.
ARQ	ARQ	Lights when the AMTOR system is in the Automatic ReQuest for repetition mode.
CHECK	Undefined	Reserved for future applications.
PKT	Packet	Lights when the system is in the packet mode.
MORSE	Morse Code	Lights when the system is in the Morse code mode.

REAR PANEL

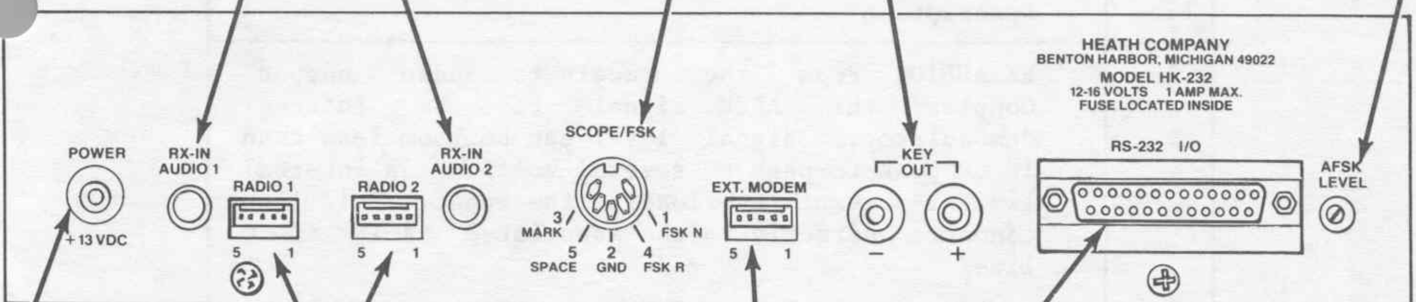
Connectors and Control Descriptions

SCOPE/FSK: Round 5-pin DIN socket. The SCOPE outputs permit monitoring the outputs of the mark/space resonators with an oscilloscope. The open-collector FSK outputs monitor the digital signal going to the input of the AFSK modulator. You can use this signal to drive transceivers that have their own AFSK modulator.

AFSK LEVEL: Adjusts the voltage level of the AFSK signal to the transmitter. The exact level depends on the user's radio (see "Configuration and Alignment"). Clockwise rotation increases the level.

RX-IN AUDIO 1 and 2: Miniature phone socket. Directly wired to the receive audio line on the RADIO 1/2 connector. This is an alternate input for the RADIO 1/RADIO 2 connectors when only a receiver is being used.

KEY OUT: RCA phono socket. CW keyer output lines. Use the minus output for transmitters that have negative keying lines (common with vacuum tube sets). Use the plus output for positive lines.



RADIO 1 and 2: Five-pin right-angle male connector. Interfaces the HK-232 to an HF or VHF transceiver. Provides receive audio, transmit audio, squelch, PTT, and ground-return lines.

RS-232 I/O: 25-pin female D connector (DCE). Provides an RS-232C interface to a computer or terminal. Only pins 1-8 and 20 are standard. The remaining pins are a parallel interface to a printer.

POWER: Standard power socket. Connects to an external power supply, +12 to +16 VDC. Draws 700 mA at +13 VDC nominal.

EXT. MODEM: Five-pin right-angle male connector. Permits connecting the HK-232 to an external modem. The internal modem will have to be disconnected, though. See "Configuration and Alignment" for details.

Pin-out Tables

POWER

Connector	**Description**
Center	+13 VDC, 700 mA from external power supply.
Sleeve	Ground return.

RX-IN AUDIO 1 and 2

Connector	**Description**
Tip	Receiver audio signal. May be used as output or an input.
Sleeve	Ground return.

RADIO 1 and 2

Pin	**Description**
1	**RX AUDIO:** From the receivers audio output. Couples the AFSK signal to the internal demodulator. Signal level can be from less than 10 mV peak-to-peak to several volts. An internal limiter prevents overloading the input. This line connects directly to the associated RX-IN AUDIO line.
2	**TX AUDIO:** AFSK output from the HK-232 to the microphone input of the transmitter. Signal level adjusted by the AFSK LEVEL control. This can vary from one transmitter to another, but is typically 10 to 20 mV peak-to-peak.

RADIO 1 and 2 (continued)

Pin	Description
3	**SQUELCH:** From the squelch circuits in the receiver. The HK-232 monitors this line in the packet mode to prevent transmitting if the channel is already active. This is only necessary if the channel is also used for other forms of communication, such as voice. That is, voice will break squelch, but not trigger the threshold and mark/space detectors. Thus, without the squelch input, the HK-232 may think the channel is empty and begin transmitting and cause interference. Pin 3 isn't monitored in other modes. Also, it doesn't need to be connected for the packet mode as long as the HK-232 is used on packet-only channels. If the receiver doesn't have a squelch output, you might be able to connect pin 3 to the radio's "busy" light or other carrier-detect indicators. The signal must be positive, but may be active-high or active-low. Use the HK-232 "SQ ON/OFF" command to select the appropriate level. There is no specified upper voltage limit, but it should be kept near TTL levels. Pin 3 connects through a 20-kilohm resistor to the base of a 2N2904 NPN transistor.
4	**GROUND:** Signal return path.
5	**PTT:** Push-to-talk output control line to the transmitter PTT input. Jumpers inside the HK-232 can program the unit for positive or negative PTT lines. Though the voltage and current ratings aren't specified, the PTT circuitry is similar to the CW keyer lines. That is, the positive PTT circuits should handle up to +100 VDC and sink about 100 mA. The negative circuits should handle up to -30 VDC and sink about 20 mA.

SCOPE/FSK

Pin	Description
1	**FSK N:** Frequency-shift Keying Normal output. This is the signal that drives the internal AFSK modulator. It's an open-collector output that can handle up to +30 volts and sink 40 mA. There aren't any industry standards for signal polarity, so the "Normal" output uses a logic one to represent a space and a logic zero for a mark.
2	**GND:** Ground.
3	**MARK:** Output from the mark resonator isolated by a 4.7-kilohm resistor. Typically, the signal is about 5 V peak-to-peak. To get a vertical mark, connect this pin to the Y input of the oscilloscope.
4	**FSK R:** Frequency-shift Keying Reversed output. This is the signal that drives the internal AFSK modulator. It's an open-collector output that can handle up to +30 volts and sink 40 mA. There aren't any industry standards for signal polarity, so the "Reversed" output uses a logic zero to represent a space and a logic one for a mark.
3	**SPACE:** Output from the space resonator isolated by a 4.7-kilohm resistor. Typically, the signal is about 5 V peak-to-peak. To get a horizontal space, connect this pin to the X input of the oscilloscope.

EXT. MODEM

Pin	Description
1	**RX DATA:** TTL-level receive data from the external modem.
2	**TX DATA:** TTL-level transmit data to the external modem.
3	**DCD:** TTL-level data carrier detect signal from the external modem. A logic zero represents a detected signal.
4	**GND:** Ground.
5	**PTT:** Active-low, TTL-level push-to-talk signal to the external modem. This line can be used to inhibit the modem output in custom applications.

KEY OUT

Connector	Description
Center	Negative and positive control lines to the transmitter keyer. The negative line will sink up to 20 mA at -30 VDC and the positive line will sink up to 100 mA at +100 VDC.
Sleeve	Ground.

RS-232 I/O

Pin	Description
1	**CHASSIS GROUND:** This line also connects to the circuit board ground through the left and right rear spacers holding the circuit board to the chassis. If either spacer or associated mounting hardware is missing, pin 1 will float.
2	**TXD:** RS-232C signal from computer transmit data output. ±18 volts, minimum ±3 volts. Idles at MARK (negative voltage).
3	**RXD:** RS-232C signal to the computer receive data input. ±10 volts. Idles at mark (negative voltage).
4	**RTS:** RS-232C handshake from the computer request-to-send output. Active high (+3 to +18 volts).
5	**CTS:** RS-232C handshake to the computer clear-to-send input. Active high (+10 volts).
6	**DSR:** RS-232C handshake to the computer data-set-ready input. Permanently tied high (+10 volts) inside the HK-232.
7	**SIGNAL GROUND:** This line connects directly to the circuit board ground. It also connects to the chassis ground through the right rear spacer holding the circuit board to the chassis.
8	**RLSD (DCD):** RS-232C handshake to the computer received line signal detector input. The EIA specifies pin 8 as RLSD, but it's referred to as the data-carrier-detect in the HK-232. Active high (+10 volts). If the DCDCONN command is set to ON, this line responds to the front panel CON LED when in the packet or AMTOR mode. When CON is lit, DCD is high; otherwise, it's low. This signal is used by some packet communications programs to monitor connect status.
9	Not connected.
10	Not connected.
11	Not connected.
12	Not connected.
13	**DATA1:** Parallel port data line to printer. TTL active-high.
14	**DATA2:** Parallel port data line to printer. TTL active-high.
15	**DATA3:** Parallel port data line to printer. TTL active-high.

RS-232 I/O (continued)

Pin	Description
16	**DATA4:** Parallel port data line to printer. TTL active-high.
17	**DATA5:** Parallel port data line to printer. TTL active-high.
18	**DATA6:** Parallel port data line to printer. TTL active-high.
19	**DATA7:** Parallel port data line to printer. TTL active-high.
20	**DTR:** RS-232C handshake from the computer data terminal ready output. Active high (+3 to +10 volts).
21	**DATA8:** Parallel port data line to printer. TTL active-high.
22	**$\overline{\text{STROBE}}$:** Parallel port handshake line to the printer. TTL active-low. After the HK-232 places data on DATA1-DATA8, it brings pin 22 low to tell the printer that a new byte is present at the printer input.
23	**$\overline{\text{ACK}}$:** Parallel port handshake line from the printer. TTL active-low. The printer asserts this line to acknowledge that it processed the byte on DATA1-DATA8 and is ready to receive another character. To reduce ringing, the $\overline{\text{ACK}}$ line should have a 200-ohm series resistor in the cable.
24	**BUSY:** Parallel port handshake line from the printer. TTL active-high. The printer asserts this line if it can't accept a data byte from the HK-232 at the time $\overline{\text{STROBE}}$ asserts. To reduce ringing, the cable should contain a 200-ohm series resistor in the BUSY line.
25	**+5V:** From the HK-232 +5 VDC regulator (non-battery backup). Not used by the RS-232C or parallel port.

Equipment Hookup

COMPUTER INTERFACE

Here is the RS-232C cable wiring for the Heath/Zenith series H/Z-89, H/Z-100, PC, lap top, and Advanced PC computers. Older systems use a 25-pin DTE or DCE connector while newer systems use a 9-pin DTE. For other manufacturers, refer to the HK-232 PackKit User Manual, #595-3902. Note that most general communications programs don't require that all the handshaking pins be connected. In most cases, all you need is TXD, RXD, and signal ground.

In the following tables, the arrows show the direction of signal flow.

25-Pin DTE Connector

Computer Connector (DTE)		Signal		HK-232 Connector (DCE)
1*	———	Chassis Ground	———	1*
2	>———>	TXD	>———>	2
3	<———<	RXD	<———<	3
4	>———>	RTS	>———>	4
5	<———<	CTS	<———<	5
6	<———<	DSR	<———<	6
7	———	Signal Ground	———	7
8	<———<	DCD	<———<	8
20	>———>	DTR	>———>	20

*Also connect this wire to the plug shields.

25-Pin DCE Connector

If using one of the DCE serial connectors on the H/Z-89 or H/Z-100, wire the cable as follows:

```
Computer                                          HK-232
Connector                                         Connector
 (DCE)                                             (DCE)
_________                                         _________

   1* ────────── Chassis Ground ──────────── 1*
   3 >──────────────> TXD >──────────────> 2
   2 <──────────────< RXD <──────────────< 3
   5 >──────────────> RTS >──────────────> 4
   4 <──────────────< CTS <──────────────< 5
  20 <──────────────< DSR <──────────────< 6
   7 ──────────── Signal Ground ──────────── 7
 N.C. <─────────────< DCD <──────────────< 8
   6 >──────────────> DTR >──────────────> 20
```

Since the EIA references the signal names to the DTE connector, the above mnemonics are meaningless, since a DCE-to-DCE connection is nonstandard. At best, they refer to the functions assigned to the ACE or EPCI inside the computer. Also, the RLSD/DCD line isn't connected in the H/Z-89 and H/Z-100, which prevents using some specialized packet communications programs.

9-Pin DTE Connector

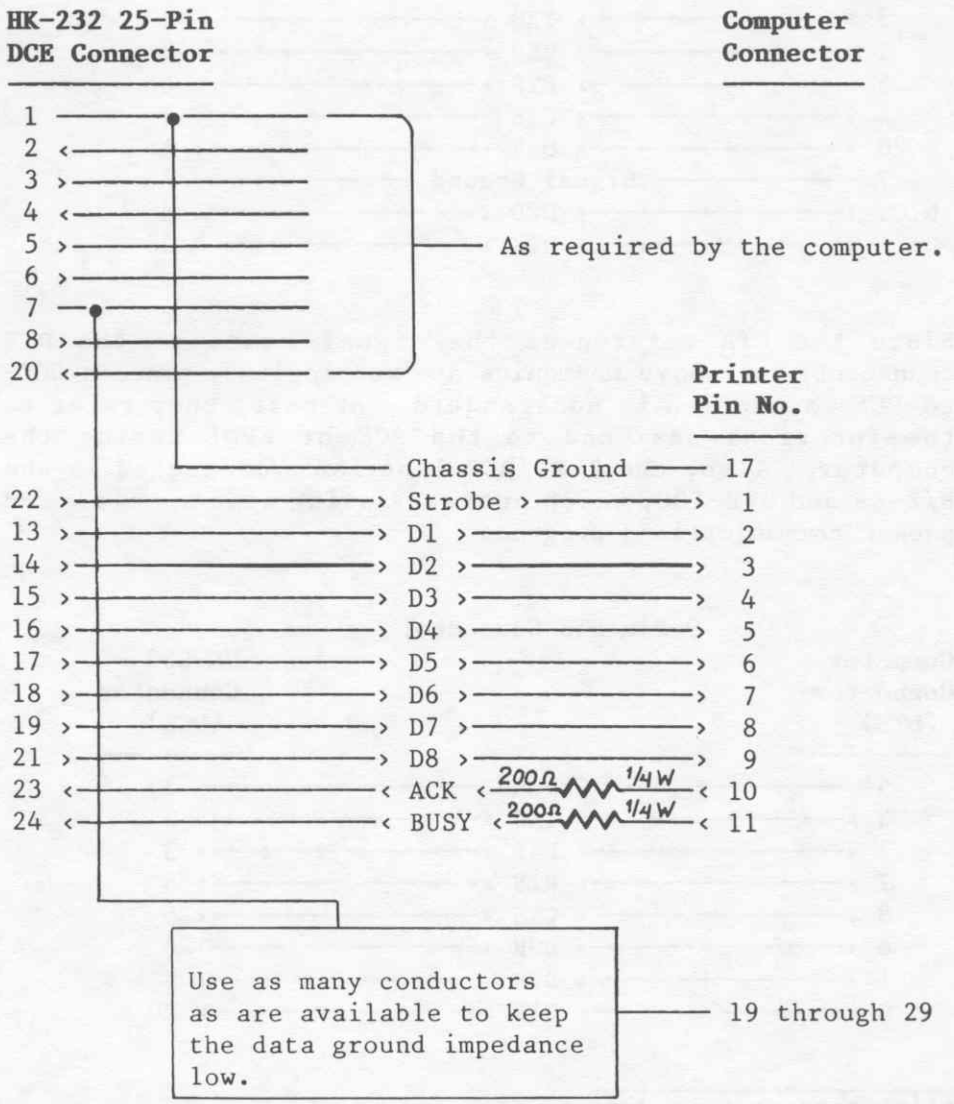
```
Computer                                          HK-232
Connector                                         Connector
 (DTE)                                             (DCE)
_________                                         _________

   5* ─────────────── Ground ─────────────── 1, 7*
   3 >──────────────> TXD >──────────────> 2
   2 <──────────────< RXD <──────────────< 3
   7 >──────────────> RTS >──────────────> 4
   8 <──────────────< CTS <──────────────< 5
   6 <──────────────< DSR <──────────────< 6
   1 <──────────────< DCD <──────────────< 8
   4 >──────────────> DTR >──────────────> 20
```

---

*Also connect this wire to the plug shields.

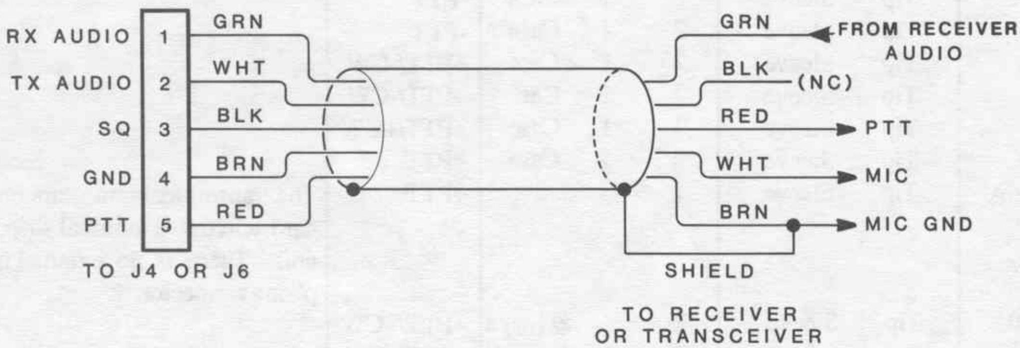
PRINTER INTERFACE

Here is the printer interface wiring for EPSON-type dot matrix graphics printers. The table also shows a partial schematic of the RS-232 leads for reference. See "Computer Interface" for detailed wiring information. For other printer manufacturers, refer to their technical literature. This cable is available wired as #230-8157.



RADIO INTERFACE

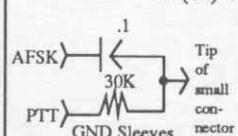
The following schematic shows the wiring of the interface cable (#230-8155) for the RADIO 1/RADIO 2 connectors. The side that connects to the HK-232 is preassembled, while the other side is left open so it can be adapted to a variety of radios. The "Heath Transceiver Wiring" table shows the wiring for most Heathkit HF and VHF radios.

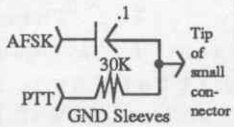
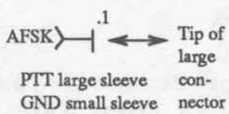
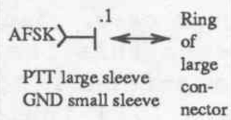


Note that the squelch wire at pin 5 isn't connected unless the HK-232 is going to be used as a packet controller on a shared channel. (See the "RADIO 1 and 2" pinout table for more information.)

HEATH TRANSCEIVER WIRING

Though not part of the RADIO 1/RADIO 2 wiring, the table also shows CW keyer polarity information for the HF radios. If not indicated, the radio doesn't have a CW line.

Model	Receiver Audio	Receiver Ground	Transmitter PTT	Transmitter MIC	Transmitter GND	PTT/CW Polarity	Remarks
HEATH							
HW-12	Tip	Sleeve	2	1	Case	-PTT	
HW-22	Tip	Sleeve	2	1	Case	-PTT	
HW-32	Tip	Sleeve	2	1	Case	-PTT	
HW-100	Tip	Sleeve	2	1	Case	+PTT/-CW	
HW-101	Tip	Sleeve	2	1	Case	+PTT/-CW	
HW-104	Tip	Sleeve	2	1	Case	+PTT/+CW	
HW-202	Tip	Sleeve	2	1	Case	+PTT	
HW-2036A	Tip	Sleeve	1	3	2	+PTT	The transmitter connectors must be hard-wired to a terminal strip in the unit. There is no external microphone connector.
HW-5400	Tip	Sleeve	3	1	2 (or) 4	+PTT/+CW	
SB-100	Tip	Sleeve	2	1	Case	+PTT/-CW	
SB-101	Tip	Sleeve	2	1	Case	+PTT/-CW	
SB-102	Tip	Sleeve	2	1	Case	+PTT/-CW	
SB-104	Tip	Sleeve	2	1	Case	+PTT/+CW	
SB-104A	Tip	Sleeve	2	1	Case	+PTT/+CW	
SB-110	Tip	Sleeve	2	1	Case	+PTT/-CW	
SS-9000	Tip	Sleeve	3	1	2 (or) 4	+PTT/+CW	
VF-7401	Tip	Sleeve	1	2	4	+PTT	
ICOM							
4-pin			2	1	3		
8-pin	Pin 8 on some radios.		5	1	6 (or) 7		
HT	Tip	Sleeve					
YAESU							
4-pin			3	2	3		
8-pin			6	8	6 (or) 7		FT-270 / 2700 require DC mike blocking connector and a diode in series with PTT line.

Model	Receiver Audio	Receiver Ground	Transmitter PTT	Transmitter MIC	Transmitter GND	PTT/CW Polarity	Remarks
YAESU (continued)							
FT-x03 x09 727	Tip	Sleeve					
FT-208	Pin 2		3	1	4		
KENWOOD							
4-pin			2	1	3 (or) 4		
5-pin			2	1	4 (or) 5		
6-pin			2	1	6		
8-pin			2	1	7 (or) 8		
TR-2500	Tip	Sleeve					
TR-x600 TH-x1	Tip	Sleeve					
TEN-TEC							
12-pin			3	1	2		
8-pin			Tip	Ring	Sleeve		
AZDEN							
12-pin			9	12	2 (or) 11		
8-pin			7	1	2		
DRAKE							
4-pin			2	1	3		
1/4" stereo			Tip	Ring	Sleeve		

SOFTWARE
Operating Modes

CAUTION: The Baudot, ASCII, and AMTOR FEC transmit signals have a 100% duty cycle. This can damage some HF transmitters operating at full power. Refer to the manufacturer's transmitter specifications for information on reducing the power output to safe levels.

This section of "Operation" provides you with information to allow you to become familiar with the major operating modes of the HK-232. Due to the large number of commands, it only covers the ones you need to know when bench-testing the unit. For complete information, refer to the PackKit Model HK-232 User Manual, #595-3902.

In the following sections, the commands you are to enter and the HK-232 responses are shown in **BOLD FACE.** Display values may be in either upper- or lower case. Sentences that state "...the HK-232 displays..." means that the HK-232 sent the data to the display on the external computer. A word surrounded by angle brackets (<>) indicates a control character such as <CTRL-C> and <RETURN>. Numbers prefixed with a dollar sign are in hexadecimal.

COMMAND

The command mode is the first mode the HK-232 enters once it's powered up. At turn-on, if there's no configuration in battery backed RAM, the HK-232 will send the following message to the computer.

Please type a star (*) for auto-baud routine.

If the computer is operating at 1200 buad, the message will appear asshown; otherwise, it will be garbled characters. The fornt panel DCD will be on or off, depending on the setting of the THRESHOLD control and the TUNE indicator will be lit and cnetered. Of the status and mode indicators, only the MODE BAUDOT LED will be lit.

Press the * (asterisk) key a few times to set the baud rate. The HK-232 will display a message similar to the following.

HK-232 is using default values.

Heathkit HK-232 Multi-Mode TNC
Copyright (C) 1986, 1987 by
Heath Company and AEA, Inc.
Release 04 March 1987
Checksum $xx*
cmd:

The checksum is a hexadecimal number that is the sum of the bytes in system ROM modulo 256. Note that the release number and checksum may be different for the unit your're servicing.

The HK-232 is now in the command mode and packet radio mode. The status and mode LEDs will light as follows.

STATUS: CMD
MODE: PKT

From the command prompt (cmd:), the HK-232 can be programmed to enter any of several other modes. The following sections describe the major ones in alphabetical order.

*

ROM #	CHECKSUMXX
444-580 444-581	$ C7
444-580-1 444-581-1	$ DA
444-580-2 444-581-2	$ 82

AMTOR

AMTOR (Amateur Teleprinting Over Radio), an adaptation of the SITOR system used in high-seas ship telex, uses a unique seven-bit synchronous code for error detection and error correction. There are two operating modes, ARQ (Mode A) and FEC (Mode B). ARQ (Automatic ReQuest for repetition) provides a synchronous, interactive link with error detection and correction. Many amateurs consider ARQ to be the most error-free method of HF message transmission available in the amateur radio service. FEC (Forward Error Correction) permits transmitting information to more than one station at the same time. With forward error correction, the FEC station transmits enough information for the receiving station to detect and sometimes correct a garbled character. However, if it can't correct the character, the receiving station won't notify the transmitter of the fact (as does ARQ). Instead, it doesn't print anything, but waits for the next character.

To enter the AMTOR mode, first install a SELCAL (Selective Sequential Calling) code. You only need to do this once (assuming battery backup). The SELCAL consists of exactly four alphabetic characters deriving from amateur's call sign; for bench testing, enter any four letters you desire. For example, if you type **MYS XYZY**, the HK-232 will respond with the following:

MYSELCAL was
MYSELCAL now XYZY

Next enter the AMTOR mode by typing **AM <RETURN>.** Assuming that packet was the previous mode, the HK-232 display will show the following:

OPMODE was PACKET
OPMODE now AMTOR

The DCD and tuning LEDs will continue to operate normally and the following status and mode LEDs will light.

STATUS: **STDBY**
MODE: **STDBY**

Mode A (ARQ)

To enter AMTOR mode A, type **ARQ XYZY <RETURN>**. (If on the air, substitute the SELCAL of the receiving station for XYZY.) The HK-232 will display the following.

OPMODE was AMTOR
OPMODE now ARQ

The DCD and tuning LEDs will continue to operate normally and the following status and mode LEDs will light.

STATUS: SEND, TFC, CON, IDLE
MODE: ARQ

Note that TFC, CON, and IDLE will alternately turn on and off with the data flow. To return to the command mode, type **<CTRL-C> <RETURN>**. If the HK-232 is connected to a transmitter, type **R <RETURN>** to unkey it.

Mode B (FEC)

To enter AMTOR mode B, type **FEC <RETURN>**. The HK-232 will display the following.

OPMODE was ARQ
OPMODE now FEC

The TUNE display will turn off, but the DCD LED will continue to operate normally. The following status and mode LEDs will light.

STATUS: SEND, IDLE, TFC (briefly)
MODE: FEC

The HK-232 keys the transmitter and sends FEC "idle" signals. When sending data, the IDLE LED will turn off and TFC will light. To exit FEC, type **<CTRL-C> <RETURN>** followed by **R <RETURN>** to unkey the transmitter.

ASCII RTTY

The ASCII (American Standard Code for Information Interchange) code is also known as International Alphabet Number 5. It is a seven-bit code that represents 128 different letters, numbers, punctuation marks, symbols, and control codes. In RTTY, it's transmitted asynchronously with an eighth bit added to permit sending binary files.

To enter the ASCII RTTY mode, type **AS <RETURN>**; the HK-232 will respond with a display similar to the following.

OPMODE was AMTOR
OPMODE now ASCII

The DCD and TUNE LEDs will function normally, while the following status and mode LEDs will light.

STATUS: CMD
MODE: ASCII

Though the display shows the "cmd:" prompt, the HK-232 is in the receive mode and will reproduce any ASCII RTTY characters it gets from the receiver. To enter the transmit mode, type **X <RETURN>**. The following status and mode LEDs will light.

STATUS: SEND, CONV
MODE: ASCII

To verify operation of the unit, jumper pin 1 of the active RADIO connector to pin 2. The lit bar on the TUNE display will move to the Mark position on the left, indicating the idle state. Typing on the keyboard will cause the TUNE bar to jump between the Mark and Space positions. At the same time, the HK-232 will echo the typed characters to the screen.

To exit the transmit mode, enter **<CTRL-C>**. The CONV LED will turn off and the screen will display the "cmd:" prompt. The STATUS SEND LED will still be lit because the transmitter is still keyed. To unkey the transmitter, enter **R <RETURN>**.

BAUDOT RTTY

The Baudot code (developed by Donald Murray and Emile Baudot) is also known as International Telegraph Alphabet Number 2. It is a five-bit code that represents 55 characters, numbers, punctuation, symbols, and control codes. To get around the 32-character limitation of five-bit code, two control characters--FIGS and LTRS--act as shift commands. When the receiving station gets the LTRS character, it interprets the incoming code as alphabetic characters. When it receives FIGS, it interprets the code as numbers, punctuation, and symbols. In RTTY, the code is sent asynchronously, but, since the length is limited to five bits, it's not practical to send binary data.

Though Baudot code has limitations, it's been in use for over a century and so it is firmly entrenched as a communications protocol. Not only is it popular among amateurs, it's still used by the International Telex Network, making Baudot one of the most widely used data transmission codes in the world.

To enter the Baudot mode, type **BA <RETURN>**. The HK-232 will display the following message.

OPMODE was ASCII
OPMODE now BAUDOT

The DCD and TUNE LEDs will function normally, while the following status and mode LEDs will light.

STATUS: **CMD**
MODE: **BAUDOT**

Though the display shows the "cmd:" prompt, the HK-232 is in the receive mode and will reproduce any Baudot RTTY characters it gets from the receiver. To enter the transmit mode, type **X <RETURN>**. The following status and mode LEDs will light.

STATUS: **SEND, CONV**
MODE: **BAUDOT**

To verify operation of the unit, jumper pin 1 of the active RADIO connector to pin 2. The lit bar on the TUNE display will move to the Mark position on the left, indicating the idle state. Typing on the keyboard will cause the TUNE bar to jump between the Mark and Space positions. At the same time the HK-232 will echo the typed characters to the screen.

To exit the transmit mode, enter **<CTRL-C>**. The CONV LED will turn off and the screen will display the "cmd:" prompt. The STATUS SEND LED will remain lit because the transmitter is still keyed. To unkey the transmitter, enter **R <RETURN>**.

CALIBRATE

The calibrate mode provides an accurate built-in method of aligning the AFSK generator. Using the internal clock as a reference, the Z80 CPU in the HK-232 monitors the output of the generator, converts the reading to frequency, and displays the results. It also displays the control you must adjust to get the correct frequency.

To enter the calibrate mode, type **CAL <RETURN>**. The front panel LEDs will remain in their previous settings, but the display will show something similar to the following:

```
1200    R167
1200    R167
1200    R167
1200    R167
....    ....
```

and continuously repeat.

While in the calibrate mode the following keys are active.

Key	Function
Space	Toggles between mark and space.
D	Toggles between the mark and space tones at a rate determined by the radio baud (HB) rate.
H	Toggles between wide and narrow band-pass.
K	Toggles the PTT line on and off.
Q	Exits the calibrate routine.

For an example on using the calibration mode, refer to "Configuration and Alignment."

FACSIMILE

Facsimile, or FAX, is used to transmit maps, drawings, photographs, and other fixed images to another station. The image is scanned at the originating station and converted into an electrical signal before it's transmitted. A receiving station then reconstructs the electrical signal into a likeness of the original. The HK-232 converts this signal to a two-level monochrome signal--black and white--before sending it to the printer. Though printers such as the EPSON can be programmed to produce shades of gray, the HK-232 can only detect a mark or a space. However, this is adequate for copying weather maps.

To enter the facsimile mode, connect an Epson-compatible printer to the HK-232 and type **PRCON ON** on the terminal. The HK-232 will display the following.

PRCON was OFF
PRCON now ON

The PRCON ON command reconfigures the HK-232 parallel port from a front panel display interface to a printer interface. The following status and mode LEDs will light.

STATUS: **STA, CON, MULT**
MODE: **PKT**

Since the mode and status LEDs are connected in parallel to the printer lines, they will flash randomly when the HK-232 sends data to the printer.

Now type **FAX <RETURN>**. The HK-232 will display the following.

OPMODE was BAUDOT
OPMODE now FAX

Adjust the **THRESHOLD** control FCW. This control acts as a printer-enable control in FAX. To disable the printer, turn the control FCCW. The HK-232 is now in the facsimile standby-receive mode, which means that it is waiting for a synchronization signal from a facsimile transmitter to begin a new picture.

To route the facsimile picture to the RS-232C port rather than the parallel port, type **PRFAX OFF**. The HK-232 will display the following.

PRFAX was ON
PRFAX now OFF

Before turning on the terminal emulator file capture routine, be sure to set AWLEN to 8, 8BITCONV to ON, PARity to 0, and ACRDISP to 0. Note that the terminal emulator must be able to process binary files and not add carriage returns or line feeds to the captured file.

To transmit a picture, tune the HK-232 AFSK generator as described in "Configuration and Alignment" and type **X <RETURN>**. The HK-232 will first send a black tone (mark) for five seconds, then a 300 Hz alteration of black and white tones for another five seconds. Next, it sends 30 seconds of synchronizing pulses at a rate determined by FSPEED (default: 2 lines/second). As soon as the sync pulses start, the HK-232 can accept dot graphics from the computer. Type **<CTRL-C>** to return to the command mode and then type **TRANS <RETURN>**. This ensures that the transmission won't abort if the HK-232 senses a byte such as a control-C or a control-D inside an escape sequence. Now transmit the picture using the disk file transfer procedures for your terminal emulator.

When done transmitting, enter **<CTRL-D>**. Since this character is outside of an Epson escape sequence, the HK-232 responds by sending 5 seconds of a 450 Hz alternation between black and white tones to indicate end of transmission. It then returns to the command mode.

During transmission, if PRCON is ON, the following status and mode LEDs will be lit.

STATUS: MULT, PHASE, STA, CON
MODE: PKT

They will remain on when the HK-232 returns to the receive mode. If PRCON is OFF during transmission, only the STATUS SENT and CONV LEDs will light. In receive, all LEDs but TUNE and DCD will be off. Before exiting the FAX mode, type **PRCON OFF <RETURN>** to disable the printer and **RESTART <RETURN>** to restore the RS-232C port settings.

MORSE CODE

Morse code continues to be the foundation of amateur radio operation. The traditional Morse code QSO is greatly improved by computer-based operation. There are some differences, however, between manual and automatic Morse operation. As a rule, computer-based Morse needs stronger signals to achieve the lowest number of errors in decoding the received text. Computers aren't forgiving or tolerant of a bad fist. If the HK-232 receives characters with improperly spaced dots and dashes, it will send garbled characters to the screen.

To enter the Morse mode, type **MO <RETURN>**. The HK-232 will display a message similar to the following.

OPMODE was FAX
OPMODE now MORSE

The following front panel LEDs will light.

STATUS: CMD
MODE: MORSE

The HK-232 is now in the receive mode and will reproduce any Morse code character it gets from the receiver. To enter the transmit mode, type **X <RETURN>**. The HK-232 will key the transmitter and light the following status and mode LEDs.

STATUS: SEND, CONV
MODE: MORSE

To exit the transmit mode, type **<CTRL-C>** to return to the command mode, followed by **R <RETURN>** to unkey the transmitter. Alternately, you can type **<CTRL-D>** to return to the command mode and unkey the transmitter at the same time. However, the HK-232 will first finish sending any remaining characters in its buffer.

PACKET

Packet radio, one of the newest forms of communication, offers a major improvement in the reliability of text and data transmission. The HK-232 uses the AX.25 protocol. This is a modification of the X.25 which is used by various telephone networks. The protocol involves adding control and checksum information to the data to ensure that it will arrive at the correct receiver. In addition, the protocol requires that the equipment check the channel to make sure it's not active before sending the packet. This lets several operators use the same channel without interfering with each other.

To see what each bit field does, read the following as you refer to the "Packet Construction" pictorial.

FLAG	ADDRESS	CONTROL	DATA	FCS	FLAG

Packet Construction

FLAG: This is a unique bit sequence that marks the beginning and end of each packet. It's unique because it contains six consecutive binary ones with a zero at each end (01111110). To prevent a false flag from appearing in other places in the bit stream, the HK-232 performs a function known as "bit-stuffing". This involves inserting a zero after every five consecutive ones that may appear anywhere outside the flag fields. The receiving controller removes these zeroes to recover the data.

ADDRESS: This field contains the packet routing information. It includes the destination station and, optionally, the originating station and any networks the packet is routed through.

CONTROL: This field describes the purpose of the packet to the recipient. It includes initializing or terminating communications, packet acknowledgement, or request for retransmission.

DATA: The information typed at the terminal or loaded from mass storage, such as a floppy disk. It can be from 1 to 128 bytes long, depending on how many characters were sent from the terminal before <RETURN> was pressed. If more than 128 bytes are entered before <RETURN>, the HK-232 will automatically send the packet. However, further incoming data will not be lost.

FCS: Frame Check Sequence. The FCS logic in the HK-232 counts the number of bits in a packet using a cyclic redundancy check algorithm (see the #230-8121 IC data sheet) and places the 16-bit result between the data field and final flag field. When the receiving controller gets the packet, it computes a CRC on the data and compares the result to the value stored in the FCS field. If the values match, the receiving station sends an acknowledgement to the originating station. If the values don't match, then an error occurred in transmission and the receiving station ignores the packet. When the sending station doesn't get an acknowledgement, it resends the packet.

To enter the packet mode, type **PA <RETURN>**. The HK-232 will display a message similar to the following:

OPMODE was MORSE
OPMODE now PACKET

and the following front panel LEDs will light.

STATUS: CMD
MODE: PKT

To check the HK-232 on the bench, connect it back-to-back with a jumper from pin 1 to pin 2 of the active RADIO connector. Next, type **MYCALL XYZZY <RETURN>**. The HK-232 will display a message similar to the following.

MYCALL was HK232
MYCALL now XYZZY

Now, type **CON XYZZY <RETURN>**. The HK-232 will respond with the following display.

***** CONNECTED to XYZZY**

The TUNE LED will flicker rapidly between the mark and space positions and the following status and mode LEDs will light.

STATUS: SEND, STA, CONV, CON
MODE: PKT

After roughly a 1/2-second pause, the TUNE LED will again flicker and then stop at the center. The SEND and STA LEDs will then turn off.

When you type something on the keyboard, the HK-232 will echo the characters to the screen, but no other activity will take place until you hit <RETURN> (or exceed 128 characters). At that time, you'll get the two sets of TUNE LED activity, SEND and STA will light for the duration, and the HK-232 will again echo the line to the screen.

To return to the command mode, enter **<CTRL-C>**. This will restore the "cmd:" prompt and light the following LEDs.

STATUS: CON, CMD
MODE: PKT

Now type **DISC <RETURN>**. After the displays flicker as previously described, the CON LED will turn off and the TUNE display will return to center. The HK-232 will send the following message to the computer.

***** DISCONNECTED: XYZZY**
XYZZY*>XYZZY (UA)

SIAM™

The HK-232 uses the Signal Identification and Acquisition Mode (SIAM) to analyze the incoming teleprinter signal. This includes the baud rate and the mode (Baudot, ASCII, AMTOR, or packet). If in AMTOR ARQ mode, SIAM will enable the ALIST command and, if it detects a reversed signal in AMTOR, Baudot, or ASCII, it will display RXREV ON. Where applicable, the HK-232 will indicate if the signal is synchronous or if it's using six-bit code. The six-bit code may be encountered when monitoring some military transmitters. It usually indicates that the data is encrypted and can't be processed by the HK-232. Finally, if the HK-232 cannot analyze the signal, it will display "noise."

To enter SIAM, tune the receiver to an RTTY station and type **SIGNAL <RETURN>**. The screen will display a message similar to the following.

OPMODE was PACKET
OPMODE now SIGNAL

All the mode indicators will turn off and only the STATUS CMD LED will remain lit. The tuning and DCD indicators will continue to operate normally. After about 10 seconds, the screen will display something similar to the following.

0.47: 50 baud

The number on the left is a confidence factor that ranges from 0.10 and 0.99, while the one on the right is an estimate of the baud rate. After another 10 seconds, the HK-232 will add the signal class to the display.

0.47: 50 baud, Baudot, RXREV OFF

This display will repeat once every 20 seconds.

Though SIAM is active, the HK-232 can still process command-mode commands. If you now type **OK <RETURN>**, the HK-232 will enter the operating mode using the parameters it analyzed. For the above example, it would print the following.

OPMODE was SIGNAL
OPMODE now BAUDOT

If, while in SIAM, the display was similar to one of the following:

0.47: 50 baud, 6 bits
0.47: 50 baud, synchronous
noise

the HK-232 will respond to the OK command with:

?bad

and remain in the analysis mode. In this case, exit SIAM by entering one of the other mode commands, such as PA.

Command Summary

The following table lists the commands available to the HK-232. The first column shows the complete command, while the mnemonic column lists the minimum number of letters that you must type. The default column shows the parameter for that command when the unit is powered up and no values have previously been saved in battery-backed RAM. The function column briefly describes what the command does. Hexadecimal numbers are preceeded by a dollar sign ($). This is to maintain consistency with the display.

COMMAND	MNEMONIC	DEFAULT	FUNCTION
8BITCONV	8B	OFF	Strip bit 7 in CONVERSE.
AAB	AA	HK-232	0-17 character answerback (WRU?).
ABAUD	AB	110 baud	ASCII baud rate.
ACHG	AC	Immediate command	Force AMTOR ARQ Changeover.
ACRDISP	ACRD	80	Screen width.
ACRPACK	ACRP	ON	Add <CR> to packet.
ACRRTTY	ACRR	71	Auto <CR> column in RTTY.
ADELAY	AD	4 (40 mS)	AMTOR transmit delay (X10 mS).
ADDRESS	ADD	Enter hex address	For MEMORY & I/O commands.
ALFDISP	ALFD	ON	Send LF after <CR> to terminal.
ALFPACK	ALFP	OFF	Send LF after <CR>, packet.
ALFRTTY	ALFR	ON	Send LF after <CR>, RTTY.
ALIST	AL	Immediate command	Start AMTOR ARQ "Listen" mode.
AMTOR	AM	Immediate command	Start AMTOR mode in ARQ standby.
ARQ	AR	Empty; enter SELCAL	Start AMTOR ARQ call with SELCAL.
ARQTMO	ARQT	90	Sets time of ARQ SELCAL.
ASCII	AS	Immediate command	Start ASCII RTTY mode.
ASPECT	ASP	2	Sets aspect ratio.
AWLEN	AW	7	Data bits per word, to terminal.
AX25L2V2	A	ON	Operate as AX.25 Version 1.0.
ASDELAY	AXD	0 (00 mS)	Repeater key-up delay (X10 mS).
AXHANG	AXH	0 (000 mS)	Repeater hang time (X100 mS).

COMMAND	MNEMONIC	DEFAULT	FUNCTION
BAUDOT	BA	Immediate command	Start Baudot RTTY mode.
BEACON	B	EVERY 0 (00 sec)	Set beacon timing (X10 seconds).
BITINV	BI	$00	Set bit pattern.
BKONDEL	BK	ON	Send BS SP BS for DELETE char..
BTEXT	BT	(Empty)	120-byte BEACON message text.
CALIBRAT	CAL	Immediate command	Start calibrate mode.
CANLINE	CAN	$18 <CTRL-X>	LINE DELETE character.
CANPAC	CANP	$19 <CTRL-Y>	Packet DELETE character.
CASEDISP	CAS	0 (as is)	Sets upper or lower case.
CBELL	CB	OFF	Enable "Connect" bell.
CCITT	CC	ON	Select CCITT ITA #2 or US Baudot.
CFROM	CF	All	Connect request/accept list.
CHCALL	CHC	OFF	Show call sign after channel ID.
CHDOUBLE	CHD	OFF	Show CHSWITCH character twice.
CHECK	CH	30 (300 mS)	Idle link timeout (X10 seconds).
CHSWITCH	CHS	$00	Channel-select (Link) character.
CMDTIME	CM	10 (1000 mS)	Transparent Mode escape timer.
CMSG	CMS	OFF	Send CTEXT message to caller.
CODE	COD	0 (International)	Set alphabet code.
COMMAND	COM	$03 <CTRL-C>	Character escape to COMMAND Mode.
CONMODE	CONM	CONVERSE	Mode to enter when link starts.
CONNECT	C	Immediate command	Send connect request to <call>.
CONPERM	CONP	OFF	Never disconnect this link.
CONSTAMP	CONS	OFF	Mark connections with time/date.
CONVERSE	CONV (or K)	Immediate command	Start Converse Mode from Command.
CPACTIME	CP	OFF	Use packet timeout in Converse.
CRADD	CRA	OFF	Send <CR><CR><LF> in RTTY Modes.
CSTATUS	CS	Immediate command	Show status of channels (links).
CTEXT	CT	(Sample text)	120-byte CONNECT message text.
CWID	CW	$06 <CTRL-F>	Command to send CWID (in text).

COMMAND	MNEMONIC	DEFAULT	FUNCTION
DAYSTAMP	DAYS	OFF	Include DATE in time-stamp.
DAYTIME	DA	Not set	Set/read HK-232 internal clock.
DCDCONN	DC	OFF	Sets state of RS-232C cable pin 8.
DELETE	DEL	OFF	Use BS ($08), not DEL ($7F).
DFROM	DF	All	Digipeat call sign list.
DISCONNE	D	Immediate command	Send DISC to distant station.
DISPLAY	DISP	Immediate command	Show HK-232 parameters/classes.
DWAIT	DW	16 (160 mS)	Delay for digi repeat (X10 mS).
EAS	EAS	OFF	Echo as sent, non-packet modes.
ECHO	E	ON	Echo typed keyboard characters.
ESCAPE	ES	OFF	Send ESC character $1B as $24.
FAX	FA	Immediate command	Start FAX Mode.
FAXNEG	FAXN	OFF	Set white and black senses.
FEC	FE	Immediate command	Start AMTOR FEC transmission.
FLOW	F	ON	Stop echo to screen while typing.
FRACK	FR	3 (3 sec.)	Time (X1 sec) to wait for ACK.
FSPEED	FS	2	Set FAX scan rate.
FULLDUP	FU	OFF	Full-Duplex terminal operation.
GRAPHICS	GR	1 (fast 960)	Set horizontal print density.
HBAUD	HB	1200 baud	Packet link (radio) baud rate.
HEADERLN	HEA	ON	Insert <CR> after headers.
HELP	H	Immediate command	Show brief HELP text on screen.
HID	HI	OFF	Send ID UI packet every 9.5 mins.
HOST	HOST	OFF	Host/terminal interface.
HPOLL	HP	ON	Host/poll, packet mode.
ID	I	Immediate command	Force ID packet via Unproto path.
ILFPACK	IL	OFF	Sets line feed action.
IO	IO	Varies	Read/write IO register.
JUSTIFY	JU	0 (zero)	Move image closer to left edge of paper.
K	K	Immediate command	Same as CONVERSE.
KISS	KI	OFF	Selects TNC action.
LEFTRITE	LE	ON	Set direction of scan.
LOCK	L	Immediate command	Measures speed of incoming Morse signal.

COMMAND	MNEMONIC	DEFAULT	FUNCTION
MAXFRAME	MAX	4	Maximum un-ACK'd frames allowed.
MBX	MB	None, (enter calls)	Monitor channel without headers.
MCON	MC	0 (none)	Monitor while connected (0-6).
MDIGI	MD	OFF	Monitor digipeated frames.
MEMORY	ME	Varies	Read/write memory location.
MFILTER	MFI	$07, $13	Filter received characters.
MFROM	MF	All	Monitor MFROM call signs.
MHEARD	MH	Immediate command	Display call signs heard.
MONITOR	M	4 (UA DM C D I UI)	Monitor mode level select (0-6).
MORSE	MO	Immediate command	Start Morse mode, unlock speed.
MRPT	MR	ON	Show digipeaters in headers.
MSPEED	MSP	20	Set Morse speed in WPM (5-99).
MSTAMP	MS	OFF	Time-stamp monitored frames.
MTO	MT	None	Monitor MTO call signs.
MYALIAS	MYA	None; enter yours	Alternate MYCALL.
MYALTCAL	MYALT	Empty; enter yours	Alternate AMTOR SELCAL.
MYCALL	MY	HK-232; enter yours	Your call sign for packet address.
MYSELCAL	MYS	Empty; enter yours	Your AMTOR SELCAL, 4 letters.
NEWMODE	NE	ON	Return to Command mode at DISC.
NOMODE	NO	OFF	Never switch modes.
NUCR	NU	OFF	Nulls to terminal after <CR>.
NULF	NUL	OFF	Nulls to terminal after <LF>.
NULLS	NULL	0 (zero)	Number of nulls for NUCR & NULF.
OK	OK	Immediate command	Accept parameters determined by SIGNAL command.
OPMODE	O	Immediate command	Display current operating mode.

COMMAND	MNEMONIC	DEFAULT	FUNCTION
PACKET	PA	Immediate command	Start Packet Mode.
PACLEN	PACL	128	Number of user-typed bytes in packet.
PACTIME	PACT	AFTER 10 (1000 mS)	Packet transmit timer (X100 mS).
PARITY	PAR	3 (even)	Terminal program parity (0-3).
PASS	PAS	$16 <CTRL-V>	Pass input editing character.
PASSALL	PASSA	OFF	Ignore CRC in HDLC ("Junk Mode").
PERSIST	PE	127	Sets threshold value for random transmit attempt.
PPERSIST	PP	OFF	Selects PERSIST and SLOTTIME or DWAIT.
PRCON	PRC	ON	Set printer or no printer.
PRFAX	PRF	OFF	Send FAX bit graphics to printer or terminal.
PROUT	PRO	OFF	Send text data to printer or terminal.
RBAUD	RB	45 baud (60 WPM)	Baudot RTTY baud rate.
RCVE	R	Immediate command	Go to receive, Morse/RTTY/AMTOR.
RECEIVE	REC	$04 <CTRL-D>	Receive-mode character in text.
REDISPLA	RED	$12 <CTRL-R>	Redisplay current input buffer.
RESET	RESET	Immediate command	RESET RAM system configuration to factory defaults.
RESPTIME	RES	10 (1000 mS)	Minimum delay before sending ACK.
RESTART	RESTART	Immediate command	Same as power-on/off reset.
RETRY	RE	10	Maximum number of frame repeats.
RFEC	RF	ON	Determines whether Mode B (FEC) signals are displayed.
RXREV	RXR	OFF	Reverse received data sense.
SELFEC	SEL	?CALLSIGN	Start Selective FEC with SELCAL.
SENDPAC	SE	$0D <CTRL-M>	Character that "sends" a packet.
SIGNAL	SI	Immediate command	Start signal analysis.
SLOTTIME	SL	1 (10 mS)	Sets transmit random wait time.
SQUELCH	SQ	OFF	Select receiver squelch polarity.
SRXALL	SRX	OFF	SELFEC Receive SELECTIVE or ALL.
START	STA	$11 <CTRL-Q>	Resume sending data to terminal.
STOP	STO	$13 <CTRL-S>	Stop sending data to terminal.

COMMAND	MNEMONIC	DEFAULT	FUNCTION
TBAUD	TB	1200 baud	Set terminal data rate.
TCLEAR	TC	Immediate command	Non-packet clear Transmit Buffer.
TIME	TI	$14 <CTRL-T>	Insert "send time" in text.
TRACE	TRAC	OFF	Hex dump of packet frame.
TRANS	T	Immediate command	Start Transparent Data Mode.
TRFLOW	TRF	OFF	Terminal flow ctrl-Transparent.
TRIES	TRI	0 (zero)	Show or force retry count.
TXDELAY	TXD	30 (300 mS)	PTT key-to-data delay (X10 mS).
TXFLOW	TXF	OFF	HK-232 flow control-Transparent.
TXREV	TXR	OFF	Reverse transmitted data sense.
UNPROTO	U	CQ	Path/address to send UI frames.
USERS	US	1	Number of multi-connections that are allowed.
USOS	USO	OFF	RTTY "unshift on space."
VHF	V	ON	Packet-wide or narrow shift.
WIDESHFT	WI	OFF	RTTY-wide or narrow shift.
WORDOUT	WO	OFF	RTTY-word or character output.
WRU	WR	OFF	Turn on auto-answerback (AAB).
XFLOW	XF	ON	Software flow control.
XMIT	X	Immediate command	Start transmission-key PTT.
XMITOK	XMITO	ON	PTT line can be keyed.
XOFF	XO	$13 <CTRL-S>	Stop sending data to terminal.
XON	XON	$11 <CTRL-Q>	Resume sending data to terminal.

New Commands

Starting with the second production run, the following commands have been added or changed.

COMMAND	MNEMONIC	DEFAULT	FUNCTION
BITINV	BI	0	Now also accepts UP and DOWN as arguments.
CALIBRATE	CAL	Immediate command	No longer starts with 1000 Hz shift, but starts with shift in effect at the time.
DIGIPEAT	DIG	OFF	Digipeat command for BBS use.
ILFPACK	IL	ON	Force ID packet via Unproto path.
MARSDISP	MAR	OFF	When ON, converts LTRS into CTRL-O and FIGS into CTRL-N when in Baudot and AMTOR modes.
MBELL	MBE	OFF	If ON, the HK-232 sends three BELL characters if the callsigns in the monitored packet headers match the MFROM or MTO lists.
MFILTER	MFI	$80	Filter received characters. Range expanded to $00-$80. Special character $80 filters all characters but CR and LF.
MPROTO	MP	OFF	Monitors all packet I-frames (OFF), or only I-frames with a PID byte of $F0 (ON).
PRTYPE	PRT	2 (Epson)	Selects the printer type used in the facsimile mode. This includes Epson, IBM, Radio Shack, Apple, Okidata, Gemini, Star Micronics, Gorilla, Texas Instruments, Genicom, BMC BMX-80, Blue Chip 120/10, and Mannesmann Tally Spirit 80.
WIDESHIFT	WI	OFF	Now works in AMTOR.

PRINTER INFORMATION

Abbreviations used:

1. cps = characters per second
2. col = columns, characters per line
3. dpi = dots per inch
4. LPM = lines per minutes
5. LQ = letter quality
6. NLQ = near letter quality

Printer	Features	Type
AMT 2002	250 cps, 16-pin	
Addmaster 170	matrix, 50 cps, 18/21 col	
Addmaster 180	matrix, 48 cps, 34/40 col	
Adeus CP/2000		daisy
Alphacom 81	thermal, 80 cps, 80 dpi, 80 col	
Alphacom 1842	thermal, 80 cps, 80 dpi, 80 col	
Alphacom Sprinter 20	matrix, 20 col	
Alphacom Sprinter 40	matrix, 40 col	
Alps ALQ-218	200 cps, 18-pin	
Alps ALQ-324	240 cps, 24-pin	
Alps P2000	250 cps, 9-pin	
Alps P2100	400 cps, 18-pin	stylus
Amdek 5025	25 cps, LQ	
Amdek 5040	40 cps, LQ	daisy
Amperex GP300	matrix, 300/80 cps, 122/144 col	
Anacom 150	matrix, 150 cps, 136 col	
Anacom 150Z	matrix, 180 cps, 40/220 col	
Anacom 160	matrix, 150 cps, 80 col	
Anacom 160Z	matrix, 150 cps, 80 col	
Anadex WP-6000	230 cps, 18-pin	
Anadex DP-6500	500 cps, 18-pin	
Anadex DP-8000	matrix, 112 cps, 80 col	
Anadex DP-8000 AP	matrix, 134 cps, 96 col	

Printer	Features	Type
Anadex DP-9000	150 cps, 80 col	PRTYPE 12, 14
Anadex DP-9001	120 cps, 80 col	
Anadex DP-9500	150 cps, 15"	PRTYPE 12-15
Anadex DP-9501	120 cps, 15"	
Anadex DP-9510		
Anadex DP-9620	200 cps	
Anadex DP-9625	240 cps, 9-pin	
Antex ADS-2000		PRTYPE 0, 2
Apple Dot Matrix	predecessor to Imagewriter	PRTYPE 12, 14
Apple Imagewriter I		PRTYPE 12, 14
Apple Imagewriter II		
Apple Prowriter		PRTYPE 12, 14
Axiom AT-100		
Axiom AT-550		
Axiom EX-401	192 cps, 8-pin, 5"	
Axiom EX-801 Micro Printer	matrix, 20/80 col	
Axiom EX-1620	960 cps, 144 dpi	
Axiom GP-80M	matrix, 30 cps, 80 col	
Axiom GP-100	50 cps, 60 dpi, 80 col	
Axiom GP-550	50 cps	
Axiom GP-700	color	
Axiom IMP-1	matrix, 100 cps, 80/96/132 col	
Axiom IMP-2	matrix, 100 cps, 80/96/132 col	
Axiom IMP-3	matrix, 100 cps, 80 col	
Axiom IMP-4	matrix, 100 cps, 80 col	
BMC 401	LQ	daisy
BMC BX-80		PRTYPE 48, 50
BMC BX-100		PRTYPE 48-51?
Base 2 800MST	matrix, 100 cps, 80/132 col	
Base 2 850MST	matrix, 100 cps, 80/132 col	
Blue Chip M120/10		PRTYPE 48, 50
Blue Chip M120/15		PRTYPE 48-51
Brother HR-1	16 cps	
Brother HR-11		daisy
Brother HR-15	13 cps, LQ	daisy
Brother HR-25	23 cps	daisy
Brother HR-20		daisy
Brother HR-35		daisy
Brother M-1009		PRTYPE 4, 6
Brother M-1109 (Mode I)		PRTYPE 0, 2
Brother M-1109 (Mode II)		PRTYPE 4, 6
Brother M-1409	matrix	
Brother M-1509	matrix	PRTYPE 0, 2
Brother M-1709	200 cps, 9-pin	PRTYPE 0, 2
Brother M-2024	160 cps, 24-pin	
Brother Twinwriter 5		PRTYPE 0, 2
Cal-Abco Legend 800		PRTYPE 0, 2
Canon A-50	180 cps, 9-pin	
Canon A-60	200 cps, 18-pin	
Canon A1200		PRTYPE 12, 14
Canon LBP-8A-1P		laser
Canon LBP-8A-2P		laser

Printer	Features	Type
Canon PW-1156A		PRTYPE 0-3
Centronics GLP		PRTYPE 0, 2
Centronics H-80	140 cps, 60-240 dpi	PRTYPE 0, 2
Centronics H136A		PRTYPE 0, 2
Centronics 122G	120 cps	
Centronics 122-1		
Centronics 150	matrix, 150 cps, 80 col	
Centronics 152	matrix, 150 cps, 80 col, wide	
Centronics 351	200 cps, 132 col, 66 dpi	PRTYPE 0-3
Centronics 352	200 cps, 132 col	PRTYPE 0-3
Centronics 353	200 cps, 132 col, 66 dpi	PRTYPE 0-3
Centronics 357	400 cps, 66.7 dpi	
Centronics 358	400 cps, 66.7 dpi	no graphics
Centronics 700	matrix, 69 cps, 132 col	
Centronics 701	matrix, 60 cps, 132 col	
Centronics 702	matrix, 120 cps, 132 col	no graphics
Centronics 703	matrix, 180 cps, 132 col	no graphics
Centronics 704	matrix, 180 cps, 132 col, serial	no graphics
Centronics 730	matrix, 100 cps, 80 col	
Centronics 737	matrix, 100 cps, 80 col	no graphics
Centronics 739	matrix, 100 cps, 80/132 col, serial	
Centronics 753	matrix, 150 cps, 80 col	
Centronics 761	matrix, 30 cps, 132 col	
Centronics 779	matrix, 60 cps, 80 col	
CIE 3500	350 cps	
Citizen MSP-10 (IBM mode)	160 cps, 80 col	PRTYPE 4, 6
Citizen MSP-15 (IBM mode)	160 cps, 132 col	PRTYPE 4-7
Citizen MSP-20 (IBM mode)	200 cps, 80 col	PRTYPE 4, 6
Citizen MSP-25 (IBM mode)	200 cps, 132 col	PRTYPE 4-7
Citizen Premiere 35		daisy
Citizen 120-D	120 cps, 9-pin	PRTYPE 0,2,4,6
Citizen Tribute 224	200 cps, 24-pin	
Commodore MPS 801	same as 1525	
Commodore 1525	30 cps, 60 dpi, 7-pin	PRTYPE 36
Commodore 1526	50 cps, 8-pin	
Commodore 4022	matrix, 30 cps, 40 col	
Comrex ComRiter1		daisy
Comrex ComRiter2		daisy
Comrex ComRiter3		daisy
Comrex 420 IBM		
Coosol 101B-48E	matrix, 100 cps, 48 col	
Coosol 101B-80E	matrix, 160 cps, 80 col	
Coosol 102B-132E	matrix, 160 cps, 132 col	
Copal SC-1200		PRTYPE 0, 2
Copal SC-1500		PRTYPE 0, 2
Copal SC-5500		PRTYPE 0, 2
Cordata LP-300		laser
DTC 380 Z		daisy
Daisywriter 2000	40 cps	daisy
Dana/Abati LQ-20P	18 cps, 15", LQ	
Data ED DE-80SG	matrix, 80 col, serial	
Dataproducts M-100	matrix, 130 cps, 132 col	

Printer	Features	Type
Dataproducts B-600-3	600 LPM	
Dataproducts 8010	180 cps	
Dataproducts 8012	180 cps, 9-pin	
Dataproducts Prism 8050	200 cps, 132 col	PRTYPE 20?
Dataproducts 8051		
Dataproducts 8070	400 cps, 18-pin	PRTYPE 20?
Datasouth DS-180	180 cps, 15", serial, 75 dpi, 9-pin no graphics	
Datasouth DS-220	220 cps, 60/120 dpi no graphics	
Datasouth Personal Printer I		PRTYPE 0, 2
Datasouth Personal Printer II		PRTYPE 0, 2
DECwriter LA34	matrix, 30 cps, 132 col, serial	
DECwriter LA35	matrix, 30 cps, 132 (Graphics II)	
DECwriter LA36	matrix, 30 cps, 132 col (Graphics II)	
DECwriter LA120	matrix, 120 cps, 132 col, serial	PRTYPE 4-7
DECwriter Letterprint 100	matrix, 240 cps, 132 col, serial	
Diablo Hytype II		
Diablo D25		
Diablo P-11	100 cps	
Diablo P-31	wide	
Diablo P-32 CQ1		
Diablo 620	20 cps, serial	daisy
Diablo 630	40 cps, serial	daisy
Diablo 635		daisy
Diablo D-80 1F		
Diablo 34LQ		PRTYPE 4, 6
Diablo RO-630	25 cps, 132 col	daisy
Diablo KSR-1640	45 cps, 132 col, serial	daisy
Diablo KSR-1650	45 cps, 132 col, serial	daisy
Dip-81	matrix, 100 cps, 40/80 col	
Dip-82	matrix, 100 cps, 80 col, serial	
Dip-84	matrix, 100 cps, 40/80 col	
Dip-85	matrix, 100 cps, 80/132 col	
Dynax DM-40	dot matrix	
Dynax DX-5	thermal, 30 cps, 60 dpi	
Dynax DX-15	same as Brother HR-15	daisy
Dynax DX-25		daisy
Dynas HR-25	18 cps	daisy
Dynax HR-35	33 cps	daisy
Eaton 7000+40	matrix, 125 cps, 40 col	
Eaton 7000+64	matrix, 125 cps, 64 col	
Epson DX-10		daisy
Epson DX-35	35 cps, LQ	daisy
Epson EX-800	300/60 cps, 80 col	PRTYPE 0, 2
Epson EX-1000	250 cps, 132 col, 9-pin	PRTYPE 0-3
Epson FX-70		PRTYPE 0, 2
Epson FX-80	160 cps	PRTYPE 0, 2
Epson FX-85	160 cps	PRTYPE 0, 2
Epson FX-100	160 cps, 15"	PRTYPE 0-3
Epson FX-185	160 cps, 15"	PRTYPE 0-3
Epson FX-286	160 cps, 132 col	PRTYPE 0-3

Printer	Features	Type
Epson HS-80		
Epson HW-100	100 cps	
Epson JX-80 color		PRTYPE 0, 2
Epson LQ-400		
Epson LQ-800	180/60 cps, 80 col, 24 pins	PRTYPE 0, 2
Epson LQ-1000	180/60 cps, NLQ, 24 pins	
Epson LQ-1500	200 cps, 24 pins, 60-240 dpi	PRTYPE 0, 2
Epson LQ-2500	270 cps, 24-pin	
Epson LX-80 (Homewriter 10)	120 cps, 10"	PRTYPE 0, 2
Epson LX-86	120 cps	PRTYPE 0, 2
Epson MX-70	80 cps, 80 col	PRTYPE 0, 2
Epson MX-80 III		PRTYPE 0, 2
Epson MX-80 with Graftrax 80	80 cps, 80 col	PRTYPE 40, 42
Epson MX-85		PRTYPE 0, 2
Epson MX-100	80 cps, 15"	PRTYPE 0-3
Epson MX-185		PRTYPE 0, 2
Epson P-80		PRTYPE 0, 2
Epson RX-70		PRTYPE 0, 2
Epson RX-80	100 cps	PRTYPE 0, 2
Epson RX-85		PRTYPE 0, 2
Epson RX-100		PRTYPE 0-3
Epson RX-185		PRTYPE 0, 2
Facit 4510	matrix, 120 cps	
Facit 4511	matrix, 158 cps	
Facit 4525	matrix, 150 cps, 80 col	
Facit 4526	matrix, 150 cps, 132 col	
Florida Data OSP-120	matrix, 600 cps, 198 col, serial	
Florida Data OSP-300		
Fujitsu DPMG9	18 cps, 60/120/240 dpi	
Fujitsu DPL-24	240 cps, 90/180 dpi, 24-pin	daisy?
Fujitsu SP-320	40 cps	daisy
Fujitsu SP-830	80 cps, 163 col, serial	daisy
Fujitsu DX-2100		
Fujitsu DX-2200	220 cps, 9-pin	
Fujitsu DL-2400		
Fujitsu DL-2600	288 cps, 24-pin	
Fujitsu DM-2400		
Genicom 1020	200 cps, 18-pin	
Genicom 3014		PRTYPE 0, 2
Genicom 3024		PRTYPE 0, 2
Genicom 3210	240 cps, 8-pin	
Genicom 3310 (IBM-GP mode)		PRTYPE 44-47
Genicom 3320 (IBM-GP mode)		PRYTPE 44-47
Genicom 3410	400 cps, 18-pin	
Heath H-14	matrix, 40 cps, 80 col, serial	
Heath H-25	matrix, 150 cps, 132 col, serial	
Hewlett-Packard HP-2225	150 cps, 90/180 dpi	no graphics
Hewlett-Packard HP-2671	120 cps, 90 dpi	no graphics
Hewlett-Packard HP-2673	120 cps, 90 dpi, 80 col	no graphics
Hewlett-Packard HP-82905	80 cps, 60/120 dpi, 9-pin	no graphics
Hewlett-Packard HP-2932	200 cps, 90 dpi	no graphics

Printer	Features	Type
Hewlett-Packard HP-2933	200 cps, 90 dpi	no graphics
Hewlett-Packard HP-2934	200 cps, 90 dpi	no graphics
Hewlett-Packard HP-2601	40 cps	daisy
Hi-G 9/80	matrix, 150 cps, 80 col	
Hi-G 9/132	matrix, 150 cps, 132 col	
Howard Typrinter 221	20 cps, 132 col, serial	daisy
IBM Color		PRTYPE 4, 6
IBM Graphics		PRTYPE 4, 6
IBM Proprinter		PRTYPE 4, 6
IBM Proprinter XL	200 cps, 9-pin	
IBM Prowriter		
IBM Prowriter XL		
IBM Quietwriter		daisy
IDS Microprism 480	110 cps, 80 col	
IDS Paper Tiger 445	198 cps, 80/132 col	6-pin
IDS Paper Tiger 460	matrix, 150 cps, 80 col	
IDS Paper Tiger 560	matrix, 198 cps, 132 col	
IDS Prism 80	200 cps, 80 col	PRTYPE 8?
IDS Prism 132	200 cps, 132 col	PRTYPE 8?
Inforunner Riteman		PRTYPE 0, 2
Infoscribe 500	matrix, 150 cps, 136 col	
Infoscribe 1000	matrix, 200 cps, 136 col	
Infoscribe 1100	200 cps, 9-pin	
Infoscribe 1500	matrix, 360 cps, 136 col	
Infoscribe 1400	400 cps, 18-pin	
C. Itoh Comet I	matrix, 125 col, 80 col	
C. Itoh Comet II	matrix, 125 col, 136 col	
C. Itoh Gorilla GX-100		PRTYPE 36
C. Itoh Starwriter A10-20		daisy
C. Itoh Starwriter A10-30SP	18 cps	
C. Itoh C10		
C. Itoh D10-40		
C. Itoh Starwriter F10-40PU	40 cps, LQ	daisy
C. Itoh Printmaster F10-55PU	55 cps	
C. Itoh Riteman II		PRTYPE 0, 2
C. Itoh LQ24		
C. Itoh 620		
C. Itoh 630		
C. Itoh Prowriter 1550	120 cps, 15"	PRTYPE 16-19
C. Itoh 7500		PRTYPE 12-15
C. Itoh Prowriter 8510 A	120 cps, 136 col	PRTYPE 16-19
C. Itoh Prowriter 8510 B	120 cps	PRTYPE 16, 18
C. Itoh Prowriter 8510 S	180 cps	PRTYPE 16, 18
C. Itoh Prowriter 8510 SC		PRTYPE 16, 18
C. Itoh Prowriter 8510 SEP		PRTYPE 4, 6
C. Itoh 8600		
Juki 5500		
Juki 5510		
Juki 6000		daisy
Juki 6100	18 cps	daisy
Juki 6300		daisy

Printer	Features	Type
Leading Edge Gorilla Banana		PRTYPE 36
Legend 880	80 cps, 80/160 dpi	PRTYPE 0, 2?
Legend 1000		PRTYPE 0, 2?
Legend 1080		PRTYPE 0, 2?
Legend 1081		PRTYPE 0, 2?
Legend 1200		PRTYPE 0, 2?
Legend 1500		PRTYPE 0, 2?
Legend 1380		PRTYPE 0, 2?
Legend 1385		PRTYPE 0, 2?
MPI 88G	matrix, 100 cps, 80/132 col	
Mannesmann Tally 85 (Epson mode)		PRTYPE 0, 2
Mannesmann Tally 85 (IBM mode)		PRTYPE 4, 6
Mannesmann Tally 86 (Epson mode)		PRTYPE 0, 2
Mannesmann Tally 86 (IBM mode)		PRTYPE 4, 6
Mannesmann Tally 160L	160 cps, 80 col	PRTYPE 0, 2
Mannesmann Tally 180L	180 cps, 132 col	PRTYPE 0, 2?
Mannesmann Tally MT-290 (Epson)	200 cps, 9-pin	PRTYPE 0, 2
Mannesmann Tally MT-290 (IBM)	200 cps, 9-pin	PRTYPE 4, 6
Mannesmann Tally MT-490	400 cps, 18-pin	PRTYPE 0,1,4,5
Mannesmann Tally 420L-112		
Mannesmann Tally Spirit 80	80 cps, 80/160 dpi	PRTYPE 48, 50
Mannesmann Tally 1602		PRTYPE 0, 2?
Mannesmann Tally 1605		PRTYPE 0, 2?
Mannesmann Tally 1800	matrix, 200 cps, 132 col	PRTYPE 0, 2?
Mannesmann Tally 1802		PRTYPE 0, 2?
Mannesmann Tally 1805	200 cps, serial	PRTYPE 0, 2?
Mannesmann Tally 8024L		
Matra SCANSET		PRTYPE 4-7
Micro Peripherals Printmate 99	100 cps, 50/60/75/85 dpi	
Micro Peripherals Printmate 150	150 cps, 50-85 dpi, wide	
Micro Peripherals Sprinter	160 cps, 50-85 dpi	
Microtek Tekwriter-1	matrix, 80 cps, 80 col	
Microtek Bytewriter 1	same as Tekwriter-1	
Microtek Tekwriter-2	matrix, 80 cps, 132 col	
Microtek MT-80	matrix, 125 cps, 80 col	
NEC ELF		daisy
NEC Pinwriter P1 18 pins		
NEC Pinwriter P2-2	180 cps, 18 pins, 10"	
NEC Pinwriter P2-3	180 cps, 18 pins, 10"	
NEC Pinwriter P2-7	180 cps, 18 pins, 10"	
NEC Pinwriter P3-2	180 cps, 15"	
NEC Pinwriter P3-3	180 cps, 15"	
NEC Pinwriter P3-7	180 cps, 15"	
NEC Pinwriter P5	290 cps	
NEC Pinwriter XL	290 cps, 24-pin	
NEC Pinwriter P6	216 cps	PRTYPE 0, 2
NEC CP6		
NEC Pinwriter P7	216 cps, 132 col	PRTYPE 0-3
NEC CP7		
NEC P560		
NEC P760		

Printer	Features	Type
NEC 2000		daisy
NEC 2010	20 cps	
NEC 2015		
NEC 2030	20 cps, LQ	
NEC 2050	20 cps, LQ	daisy
NEC 2525	daisy	
NEC Spinwriter 3500		daisy
NEC Spinwriter 3510	33 cps, serial, 15"	daisy
NEC 3515		daisy
NEC 3520		daisy
NEC Spinwriter 3530	33 cps, LQ	daisy
NEC Spinwriter 3550	35 cps, LQ	daisy
NEC 5510	55 cps, 132 col, serial	thimble
NEC 5520	55 cps, 132 col, serial	thimble
NEC 5530	55 cps, 132 col, serial	thimble
NEC Spinwriter 7700		daisy
NEC Spinwriter 7710	55 cps, serial	
NEC 7715		
NEC Spinwriter 7720		
NEC 7725		
NEC Spinwriter 7730	55 cps	
NE 8023	100 cps	PRTYPE 12, 14
NEC 8025		
NEC 8027		
NEC 8810		daisy
NEC 8830		daisy
NEC 8850		55 cps, LQ daisy
Newbury OSP-3	22 cps, 18-pin	
Nissho NP-910	350 cps, 9-pin	
Nissho NP-2410	300 cps, 24-pin	
Okidata Okimate 20 (IBM mode)		PRTYPE 4-7
Okidata 80	80 cps, 80 col	
Okidata ML82A with Okigraph I	120 cps, 80 col	PRTYPE 20
Okidata ML83A with Okigraph I	120 cps, 132 col (15")	PRTYPE 20-21
Okidata ML84 (IBM mode)	200 cps, 136 col (15")	PRTYPE 4-7
Okidata ML92 (IBM mode)	160 cps, 80 col	PRTYPE 4
Okidata ML92 (Oki mode) 1	60 cps, 80 col	PRTYPE 20
Okidata ML93 (IBM mode)	160 cps, 136 col (15")	PRTYPE 4-7
Okidata ML93 (Oki mode)	160 cps, 136 col (15")	PRTYPE 20, 21
Okidata 94		
Okidata 120 NLQ		
Okidata ML182 (IBM mode)	120 cps, 80 col	PRTYPE 4, 6
Okidata ML183 (IBM mode)		PRTYPE 4-7
Okidata 192	160 cps	PRTYPE 24, 26
Okidata 192+	216 cps	
Okidata 193		PRTYPE 24-27
Okidata 193+	200 cps, 9-pin	
Okidata 292	200 cps, NLQ	
Okidata 293	200 cps, 15"	
Okidata 294	400 cps, 18-pin	
Okidata 801		

Printer	Features	Type
Okidata 2350 Pacemark	350 cps	
Okidata 2410 Pacemark	350 cps	
Olivetti DY-211	20 cps, 132 col, serial	daisy
Olivetti DY-311	32 cps, 150 col, serial	daisy
Olivetti DY-811	65 cps, 150 col, serial	daisy
Olivetti DM-80/180	matrix, 80 cps, 150 col	
Olivetti DM-280		PRTYPE 0, 2
Olivetti DM-290		PRTYPE 0-3
Olympia Compact 2		
Olympia Compact RO		
Olympia ES100		daisy
Olympia ESW 3000		daisy
Olympia Needlepoint	matrix	
Olympia NP-136	200 cps, 9-pin	
Orange Micro		
OTC OT-700	700 cps, 9-pin	
Panasonic KX-P1080i	120 cps, 9-pin	PRTYPE 0, 2
Panasonic KX-P1090		PRTYPE 0, 2
Panasonic KX-P1090i		
Panasonic KX-P1091	120 cps	PRTYPE 0, 2
Panasonic KX-P1091i	160 cps, 9-pin	
Panasonic KX-P1092	180 cps	PRTYPE 0, 2
Panasonic KX-P1092i	240 cps, 9-pin	
Panasonic KX-P1093		
Panasonic KX-P1592	240 cps, 15"	PRTYPE 0-3
Panasonic KX-P1595	240 cps, 15"	
Panasonic KX-P3131		daisy
Panasonic KX-P3151		daisy
Personal Micro DMP-85		PRTYPE 12, 14
Pertec Stylist 360	17 cps, 198 col	daisy
Printek 910	matrix, 170 cps, 80 col	
Printek 920	matrix, 340 cps, 80 col	
Printers Plus NLQ		PRTYPE 0, 2
Printronix P300	300 LPM	no graphics
Printronix P600	600 LPM	no graphics
Printronix P1013	178 cps, 24-pin	
Prism see IDS Prism		
Qantex 7020		
Qantex 7030		
Qantex 7040		
Qantex 7065		
Qume Letterpro	20 cps	daisy
Qume Sprint 5/45	45 cps, 132 col	daisy
Qume Sprint 5/55	55 cps, 132 col	daisy
Qume Sprint 9/35	35 cps, 132 col	daisy
Qume Sprint 9/45	45 cps, 132 col	daisy
Qume Sprint 9/55	55 cps, 132 col	daisy
Qume Sprint 11/40+	40 cps, 132 col	daisy
Qume Sprint 11/45	45 cps	daisy
Qume Sprint 11/55	55 cps	daisy
Qume Sprint 11/90	90 cps	daisy

Printer	Features	Type
Qume Sprint Widetrack	55 cps, 240 col	daisy
Radio Shack Daisywheel II	43 cps, 136 col	daisy
Radio Shack Lineprinter IV	50 cps, 80 col	
Radio Shack Lineprinter V	120 cps, 132 col	
Radio Shack Lineprinter VI	100 cps, 132 col	
Radio Shack Lineprinter VII	30 cps, 40 col	PRTYPE 8
Radio Shack Lineprinter VIII	80 cps, 80 col	PRTYPE 8
Radio Shack Quick Printer II	matrix, 32 cps, 16 col	
Radio Shack DMP-100	60 dpi	PRTYPE 8
Radio Shack DMP-105		PRTYPE 8
Radio Shack DMP-110	120 dpi	PRTYPE 8
Radio Shack DMP-120	120/200 dpi	PRTYPE 8
Radio Shack DMP-130	100 cps, 9-pin	PRTYPE 8, 4, 6
Radio Shack DMP-200	120/144/200 dpi	PRTYPE 8
Radio Shack DMP-400 (DMP emul.)	60/72/100 dpi	PRTYPE 8
Radio Shack DMP-420 (DMP emul.)	60/72/100 dpi	PRTYPE 8
Radio Shack DMP-430	180 cps, 18 pins	PRTYPE 4, 6
Radio Shack DMP-500 (DMP emul.)	60/72/100 dpi	PRTYPE 8
Radio Shack DMP-2100		PRTYPE 4, 6
Radio Shack DMP-2110	240 cps, 24-pin	PRTYPE 8
Radio Shack DMP-2200	380 cps	PRTYPE 4-9
Radio Shack CGP-220	80 dpi	PRTYPE 8
Ricoh RP1200		daisy
Ricoh RP1300		daisy
Ricoh RP1500		daisy
Ricoh RP1600		daisy
Ricoh RP2200		daisy
Ricoh RP3400		daisy
Sakata SP-1000		PRTYPE 0, 2
Sakata SP-1500		PRTYPE 0, 2
Seikosha GP-100		PRTYPE 36
Seikosha GX-100		PRTYPE 36
Seikosha SL-80	135 cps, 24-pin	
Seikosha SP-1000 A		PRTYPE 0, 2
Seikosha SP-1000 VC (E-64)		PRTYPE 36
Seikosha SP-1000 IBM		PRTYPE 4, 6
Seikosha SP-1000 AS		PRTYPE 0, 2
Seikosha SP-1000 AP, AP IIc		
Seikosha BP-1300		
Seikosha BP-5200		
Seikosha BP-5420	420 cps, 8-pin	
Seikosha MP-1300	300 cps, 9-pin	
Silver Reed EXP-400		daisy
Silver Reed EXP-420		
Silver Reed EXP-500	16 cps	daisy
Silver Reed EXP-550	20 cps, 132 cols	daisy
Silver Reed EXP-600		daisy
Silver Reed EXP-770	36 cps	daisy
Silver Reed EXP-800		daisy
Smith Corona TP-1	12 cps, 105/125 col	daisy
Smith Corona D-100		PRTYPE 0, 2

Printer	Features	Type
Smith Corona D-200 (standard)	120 cps	PRTYPE 0, 2
Smith Corona D-200 (IBM)	120 cps	PRTYPE 4, 6
Smith Corona D-300 (standard)	140 cps	PRTYPE 0, 2
Smith Corona D-300 (IBM)	140 cps	PRTYPE 4, 6
Smith Corona Fastext 80		PRTYPE 0, 2
Smith Corona TP-1000		PRTYPE 0,2,4,6
Star COEX 80-FT	9 pins	
Star LV12-10		
Star Gemini 10		PRTYPE 28
Star Gemini 15		PRTYPE 28-29
Star Gemini 10X		PRTYPE 32, 34
Star Gemini 15		PRTYPE 32-35
Star Gemini 10XPC		PRTYPE 4, 6
Star Gemini 15XPC		PRTYPE 4-7
Star Gemini 10X Plus		PRTYPE 0, 2
Star Gemini 15X Plus		PRTYPE 0-3
Star Micronics SG-10 (Star mode)		PRTYPE 32, 34
Star Micronics SG-15 (Star mode)		PRTYPE 32-35
Star Micronics SG-10 (IBM mode)		PRTYPE 4, 6
Star Micronics SG-15 (IBM mode)		PRTYPE 4-7
Star Delta 10		PRTYPE 32, 34
Star Delta 15		PRTYPE 32-35
Star Delta 10 PC		PRTYPE 4, 6
Star Delta 15 PC		PRTYPE 4-7
Star Delta 10 Plus		PRTYPE 0, 2
Star Delta 15 Plus		PRTYPE 0-3
Star Micronics SD-10 (Star mode)	160 cps	PRTYPE 32, 34
Star Micronics SD-15 (Star mode)	160 cps	PRTYPE 32-35
Star Micronics SD-10 (IBM mode)	160 cps	PRTYPE 4, 6
Star Micronics SD-15 (IBM mode)	160 cps	PRTYPE 4-7
Star Radix 10		PRTYPE 32, 34
Star Radix 15		PRTYPE 32-35
Star Radix 10 PC		PRTYPE 4, 6
Star Radix 15 PC		PRTYPE 4-7
Star Radix 10 Plus		PRTYPE 0, 2
Star Radix 15 Plus		PRTYPE 0-3
Star Micronics SR-10 (Star mode)	200 cps	PRTYPE 32, 34
Star Micronics SR-15 (Star mode)	200 cps	PRTYPE 32-35
Star Micronics SR-10 (IBM mode)	200 cps	PRTYPE 4, 6
Star Micronics SR-15 (IBM mode)	200 cps	PRTYPE 4-7
Star Micronics SB-10		
Star Micronics NB-15, 9-wire emulation	300 cps, 24-pin	PRTYPE 4-7
Star Micronics NX-10		
Star Micronics NX-15		
Star Micronics NL-10 (std. cartridge)	120 cps	PRTYPE 0, 2
Star Micronics NL-10 (IBM cartridge)	120 cps	PRTYPE 4, 6
Star Micronics NL-15 (std. cartridge)		PRTYPE 0-3
Star Micronics NL-15 (IBM cartridge)		PRTYPE 4-7
Star Micronics DP-8480	matrix, 80 cps, 132 col	
Star Power Type	18 cps, LQ	daisy

Printer	Features	Type
Tally see Mannesmann Tally		
Tandy see Radio Shack		
Teletex T1014		daisy
Televideo TPC 11		
Televideo 186 PS		
Televideo 1605		
Texas Instruments 743	matrix, 30 cps, 80 col, serial	
Texas Instruments 765	matrix, 30 cps, 80 col, serial	
Texas Instruments 810	matrix, 150 cps, 132 col, serial	
Texas Instruments 820	matrix, 150 cps, 132 col, serial	
Texas Instruments 825	matrix, 75 cps, 132 col, serial	
Texas Instruments 850 (DP mode)		PRTYPE 40-43
Texas Instruments 855 (DP mode)		PRTYPE 40-43
Texas Instruments Omni 880	300 cps, 9-pin	
Toshiba P321	216 cps	
Toshiba P341	180 cps, 24-pin, 132 col	
Toshiba P-1340	120 cps, 80 col, 24-pin	
Toshiba P-1350	24-pin	
Toshiba P-1351	160 cps, 24-pin	
TRS-80 see Radio Shack		
Transtar 120	14 cps	daisy
Transtar 130	18 cps	daisy
Transtar 140	serial	daisy
Transtar T315		PRTYPE 12, 14
Williams Bytewriter	12 cps, 100 col	daisy
Xerox 1730	40 cps, 132 col, serial	daisy
Xerox 1740	45 cps, 132 col, serial	daisy
Xerox 1750	45 cps, 132 col, serial	daisy
Xymec HY-Q 1000	20 cps, 198 col	daisy

NORMAL OPERATING CHARACTERISTICS

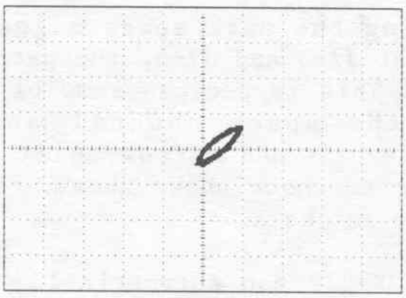
The following characteristics of the HK-232 PackKit® controller are considered normal. Become familiar with these characteristics before servicing the unit. By doing so, you'll save troubleshooting time.

- When in the calibrate mode, the date and time functions are disabled. After calibrating the unit, use the DAYTIME command to set the clock.

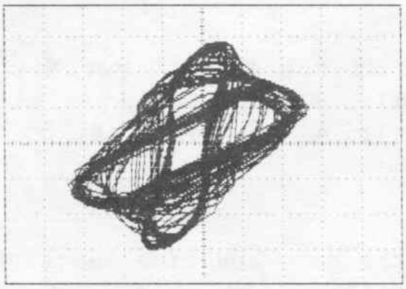
- The battery backup saves only the contents of RAM. Since the timer that is used to update the clock and calendar functions is in the parallel port, the time and date are lost whenever the HK-232 is turned off.

- When entering the date with the DAYTIME command, the program does not check to see if the day of the month is legal (e.g. February 30th).

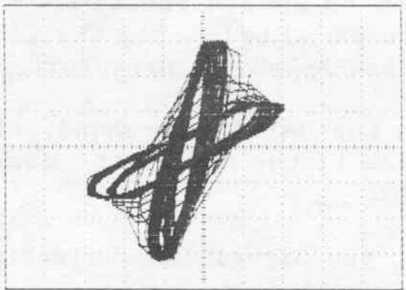
- In the second production run, the Signal Identification and Aquisition mode has been speeded up.



- Due to internal noise, an X-Y oscilloscope connected to the mark/space resonators at J7-3 and J7-5 show a waveform similar to the one above.



Typical wideshift X-Y display (packet, VHF ON).



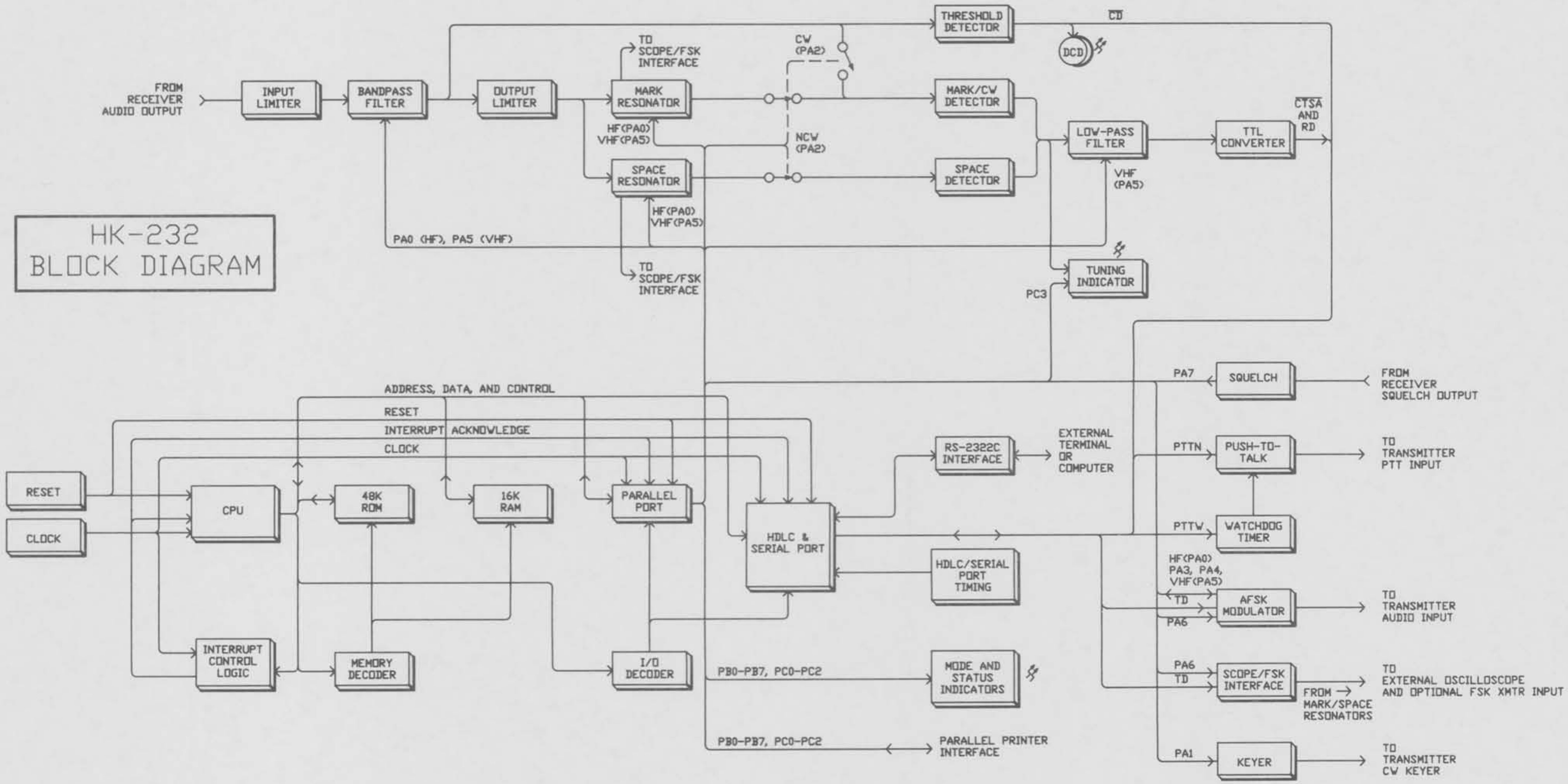
Typical narrow-shift X-Y display (Baudot, WI OFF).

- When monitoring the mark/space signals with an X-Y oscilloscope at J7-3 and J7-5, the pattern will appear as an elipse. This is because some of the mark signal appears in the space channel and vice versa. Typically, wideshift and narrow-shift RTTY will have shapes similar to those shown above. Mark is on the Y axis and space on the X.

- Although the HK-232 can automatically track different CW code-sending speeds in the Morse code mode, it cannot decode a "bad fist." If the dot-dash lengths, intervals and ratios, and intercharacter and interword spacing are outside of normal specifications, the unit will send garbled characters to the display.

- When the HK-232 is sending data through the parallel port to the printer, the MODE and STATUS LEDs will reflect the states of the data and handshake lines. To get the unit's mode and status, use the OPMODE command at the "cmd:" prompt.

CIRCUIT DESCRIPTION


HK-232
BLOCK DIAGRAM
FROM RECEIVER AUDIO OUTPUT
INPUT LIMITER
BANDPASS FILTER
OUTPUT LIMITER
MARK RESONATOR
SPACE RESONATOR
TO SCOPE/FSK INTERFACE
HF(PA0) VHF(PA5)
CW (PA2)
NCW (PA2)
THRESHOLD DETECTOR
DCD
CD
MARK/CW DETECTOR
SPACE DETECTOR
LOW-PASS FILTER
VHF (PA5)
TTL CONVERTER
CTSA AND RD
TUNING INDICATOR
PC3
PA0 (HF), PA5 (VHF)
ADDRESS, DATA, AND CONTROL
RESET
INTERRUPT ACKNOWLEDGE
CLOCK
CPU
48K ROM
16K RAM
PARALLEL PORT
HDLC & SERIAL PORT
HDLC/SERIAL PORT TIMING
RS-2322C INTERFACE
EXTERNAL TERMINAL OR COMPUTER
INTERRUPT CONTROL LOGIC
MEMORY DECODER
I/O DECODER
PB0-PB7, PC0-PC2
MODE AND STATUS INDICATORS
PARALLEL PRINTER INTERFACE
PA7
SQUELCH
FROM RECEIVER SQUELCH OUTPUT
PTTN
PUSH-TO-TALK
TO TRANSMITTER PTT INPUT
PTTW
WATCHDOG TIMER
HF(PA0) PA3, PA4, VHF(PA5)
TD
PA6
AFSK MODULATOR
TO TRANSMITTER AUDIO INPUT
SCOPE/FSK INTERFACE
FROM MARK/SPACE RESONATORS
TO EXTERNAL OSCILLOSCOPE AND OPTIONAL FSK XMTR INPUT
PA1
KEYER
TO TRANSMITTER CW KEYER

BLOCK DIAGRAM DESCRIPTION

Overview

The HK-232 Pack-Kit Multi-Mode TNC consists of circuitry that interfaces an HF/VHF transceiver to a computer or terminal. It also provides outputs to drive an Epson-type parallel printer, monitor the received signal with an oscilloscope, and directly drive transmitters equipped with an FSK input. Refer to the block diagram as you read the following.

Receiver Circuits Block Diagram

The receiver circuits are represented by the blocks along the top of the diagram. They start with the input limiter on the left and end with the TTL converter on the right. Note that while the squelch circuit (below the TTL converter) is connected to the external receiver, it's used by the transmitter circuits. (See "Transmitter Circuits Block Diagram" for more information.)

Audio signals from the user's receiver enter the TNC at the input limiter, which prevents overloading of the bandpass filter. Two control lines from the parallel port, VHF and HF, select the filter center frequency and bandwidth. These two mnemonics are somewhat misleading, as they have no relationship to the transmitter frequency. They probably got their names during the early design phase of the HK-232 at Advanced Electronics Applications, Inc., since most packet communications are on VHF and the others on HF. More accurately, the VHF line is the wide-shift enable and the HF line is the narrow-shift enable. The following table shows how they affect the bandpass filter.

	Line		**Frequency Response (Hz)**		
Mode	**HF**	**VHF**	**Fl**	**Fo**	**Fh**
----	--	---	--	--	--
Packet	Off	On	400	1700	3000
Morse	Off	Off	700	800	900
RTTY (wide)	Off	On	400	1700	3000
RTTY (narrow)	On	Off	1895	2210	2435
AMTOR	On	Off	1895	2210	2435
Facsimile	Off	On	400	1700	3000

The output of the bandpass filter connects to the threshold detector and the output limiter. The threshold detector compares the signal to the setting of the front panel threshold control. If the signal is large enough, it lights the DCD LED and places a logic zero on the $\overline{CD}$ line to indicate that a carrier has been detected. This lets the CPU know that there is data present that must be processed.

The output limiter removes any remaining amplitude variations from the signal and sends it to the mark and space resonators. The resonators are active filters that separate the mark (logic one) and space (logic zero) frequencies. In the AFSK modes, the mark resonator responds to the lower frequencies; 1100 Hz for VHF, and 2080 Hz for HF. Similarly, the space resonator passes the higher frequencies; 2100 Hz for VHF, and 2310 Hz for HF. Two taps off of these blocks send the mark and space tones to the scope/FSK interface in the lower right corner of the diagram. This permits driving the X and Y inputs of an oscilloscope to aid in tuning the receiver. (See "Transmitter Circuits Block Diagram" for the FSK interface description.)

The resonator outputs couple through two electronic switches to the mark/CW and space detectors. In the CW mode, these switches open the circuits from the resonators and connect the bandpass filter directly to the mark/cw filter. In this case, the space detector is disabled.

When receiving a CW or mark signal, the mark/CW detector generates a positive DC voltage at its output. Similarly, a space signal will cause the space detector to generate a negative voltage. These are summed by a resistor network and sent to the tuning indicator and the low-pass filter. The tuning indicator is a simple A/D converter that drives a ten-element bar display. It lights the bar on the left for a mark and the one on the right for a space. Intermediate frequencies will light one or more bars in between these two. Under a no-signal condition, the center bar will light. PC3 is a display-enable control line.

The active low-pass filter removes any residual pulses caused by the modulating tones. The VHF control line selects the appropriate cutoff frequency: about 1500 Hz for the packet, RTTY wide, and facsimile modes; and 400 Hz for the Morse, RTTY narrow, and AMTOR modes. The filter output connects to a TTL converter, which squares up the signal and inverts it so that a logic one corresponds to a mark. It then couples the signal on the RD signal line to the HDLC/serial port (High-level Data Link Controller).

Transmitter Circuits Block Diagram

The tranmitter circuits consist of the column of blocks on the right side of the diagram, starting with the squelch block and ending with the keyer.

The squelch circuit couples the external receiver squelch status through PA7 to the parallel port. The HK-232 monitors the squelch to prevent transmitting if the channel is already active. Simply checking the status of the threshold circuits and mark/space detectors isn't enough. These circuits will inform the CPU that FSK information is present, but not if some other form of communication, such as voice, is taking place. Note that the HK-232 only uses the squelch circuit in the packet mode. In other modes, the operator must decide when to transmit.

The push-to-talk circuits connect to the microphone PTT line on the external transmitter. The HK-232 controls this line though the $\overline{\text{PTTN}}$ line from the serial port. Jumper plugs in the TNC allow selecting an active high or low to key the transmitter. As discussed in the previous two paragraphs, the HK-232 won't key PTT if the channel is active in the packet mode.

The watchdog timer circuit disables the PTT circuits if a failure occurs in the HK-232. The HK-232 pulses the serial port PTTW line roughly once every 5 mS to keep the timer inactive. The exact period will jitter by about 2 mS because the CPU must constantly process interrupt requests from the parallel port timer. (See "Digital Circuits Block Diagram" for more information.) If a failure occurred and PTTW stopped pulsing, the watchdog timer would time out after about 60 mS and shut down the push-to-talk switch.

Note that when the HK-232 has been placed in the calibrate mode and the transmitter keyed ("K" pressed), the CPU will deliberately stop pulsing the PTTW line after about 60 seconds. Also, the pulses will be about 200 uS apart since the program is in a tighter loop.

The AFSK modulator provides the audio-frequency tones for all the transmitting modes. The TD line, from the HDLC, is the modulating signal for the packet mode and ASCII RTTY mode for data rates above 600 baud. PA6, from the parallel port, provides modulation for the other modes. Note that when switching from a higher ASCII baud rate to a lower rate, such as from 1200 baud to 300, the TD line will still be the active data path. To force the data path back to PA6, return to the "cmd:" prompt and enter **R <RETURN>** to put the HK-232 back in the receive mode. Change the baud rate then re-enter the transmit mode (see "Operation").

Four other lines from the parallel port monitor and control the modulator: HF, VHF, PA3, and PA4. The HF line sets the mark/space frequencies to 2110 Hz/2310 Hz for narrow-shift RTTY and AMTOR. The VHF line sets these frequencies to 1200 Hz/2200 Hz for the packet and wide-shift RTTY modes. VHF is also high for facsimile transmission, but the modulator must be recalibrated to 1300 Hz/2100 Hz before using it. (See "Configuration and Alignment.") The line at PA3 sends the output of the modulator oscillator to the parallel port. The CPU monitors this signal during alignment to determine if the oscillator is at the correct frequency. The remaining line, PA5, disables the modulator output when not transmitting.

The TD and PA6 lines also connect to the scope/FSK interface. The scope mark/space lines are actually independent of this circuit, but share the same rear-panel connector. (See "Receiver Circuits Block Diagram.") The FSK interface permits the TD and PA6 lines to directly drive an external FSK modulator.

The remaining circuit, the keyer, interfaces the PA1 line from the parallel port to the external transmitter key input. When a keyboard key is pressed, and the HK-232 is in the transmit Morse code mode, the PA1 line pulses with the Morse code sequence representing the keyboard key. At the same time, the push-to-talk circuit is activated and the AFSK modulator is sending the equivalent dots and dashes as a 1200-Hz tone to the microphone input. This gives the operator the choice of using either straight CW or tone-modulated CW.

Digital Circuits Block Diagram

The digital circuits consist of a microprocessor, ROM, RAM, serial and parallel I/O, and support logic to provide timing and control. These circuits are located on the lower left and lower center of the block diagram.

The reset block resets the CPU, the parallel port, and the serial port at powerup. There's no external control line connected to it, so the reset circuit is only active at turn-on.

The clock circuit generates a 4-MHz crystal-controlled square wave to provide timing to the CPU, I/O ports, and interrupt control logic.

The CPU is a Z80A 8-bit microprocessor that performs all the data processing in the HK-232. It fetches instructions from the ROM, stores and fetches data in the RAM, and transfers data between it and the I/O ports. The ROM consists of a 32K EPROM and a 16K EPROM located between addresses 0000H and BFFFH. The RAM is two 8K CMOS static read/write memories located between addresses C000H and FFFFH. The memory decoder monitors the CPU address bus and selects the appropriate IC when the CPU performs a memory access. Similarly, the I/O decoder selects the serial or parallel I/O port.

The parallel port, at addresses BCH-BFH, provides several timing and control functions. In addition to those described in "Receiver Circuits Block Diagram" and "Transmitter Circuits Block Diagram," it also has three programmable internal timers, a printer port interface, and control lines to the front panel mode and status indicators (see "Operation"). The internal timer generates an interrupt request once each millisecond which the CPU uses for various timing functions, such as updating the time-of-day clock. The printer port interface permits connecting the TNC to a Centronics-compatible parallel printer for printing facsimile pictures. Currently, the only graphics software supported is the Epson MX/LX standard.

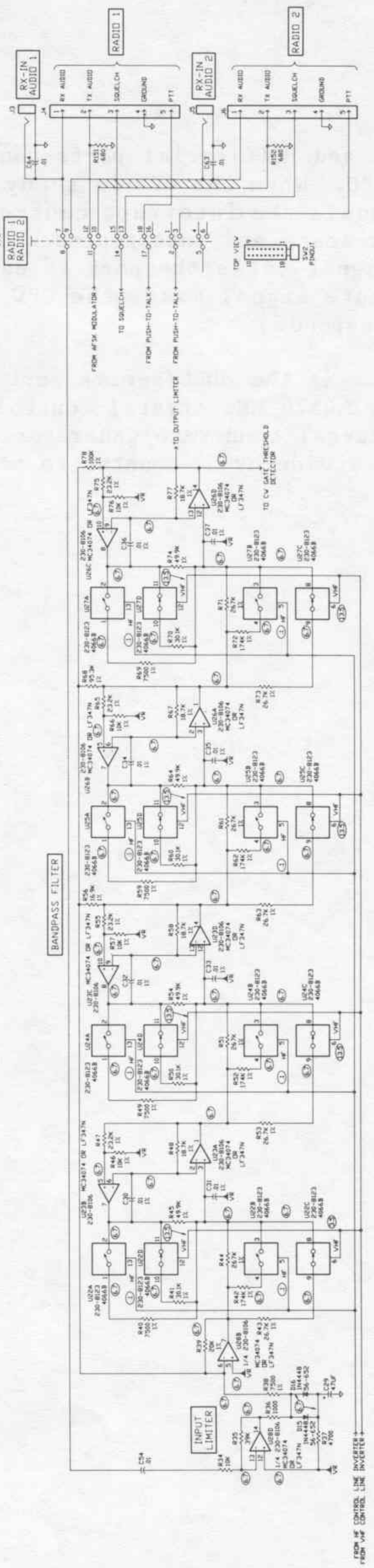
The serial I/O circuits consist of an RS-232C port at addresses 7CH-7DH and an HDLC port at 7EH-7FH. The RS-232C connects to the RS-232C interface which converts the output signals from TTL to ±10 volts, and the input data from ±10 volts to TTL. A standard terminal or computer can be connected to this interface. Data rates in the TNC are software-adjustable from 110 baud to 9600 baud.

The HDLC port performs most of the work for the CPU in converting the data to and from the AX.25 protocol. This includes frame-level control, automatic zero insertion and deletion, I-field residue handling, abort generation and detection, and CRC generation and checking. (See the #230-8121 IC data sheet for more details.)

In other modes, the HK-232 sends serial data through PA6 in the parallel port and receives data at $\overline{\text{CTSA}}$ of the HDLC port. In either case, it's the CPU's job to correctly translate the protocols. This includes the on/off keying of Morse and facsimile, ASCII and Baudot codes in RTTY, and the ARQ and FEC protocols in AMTOR.

Both the parallel and HDLC/serial ports can send interrupt requests to the CPU. When the CPU is ready to process the interrupt, it signals the interrupt control logic, which generates the wait-state and interrupt-acknowledge signals. The acknowledge signal tells the port it can send the data while the wait-state signal makes the CPU wait until the port has time to respond.

The remaining block is the HDLC/serial port timing circuit. This consists of a 2.4576 MHz crystal-controlled oscillator that times the internal baud-rate generator. Also included in this block is a divide-by-32 counter to provide baud rate timing to the HDLC.


RX-IN AUDIO 1
RADIO 1
RX-IN AUDIO 2
RADIO 2
RX AUDIO
TX AUDIO
SQUELCH
GROUND
PTT
RADIO 1 RADIO 2
TOP VIEW
FROM AFSK MODULATOR
TO SQUELCH
FROM PUSH-TO-TALK
TO OUTPUT LIMITER
TO CV GATE THRESHOLD DETECTOR
BANDPASS FILTER
INPUT LIMITER
FROM HF CONTROL LINE INVERTER
FROM VHF CONTROL LINE INVERTER

DETAILED CIRCUIT DESCRIPTION
Receiver Circuits

Refer to the Analog Circuits schematic diagram as you read the following.

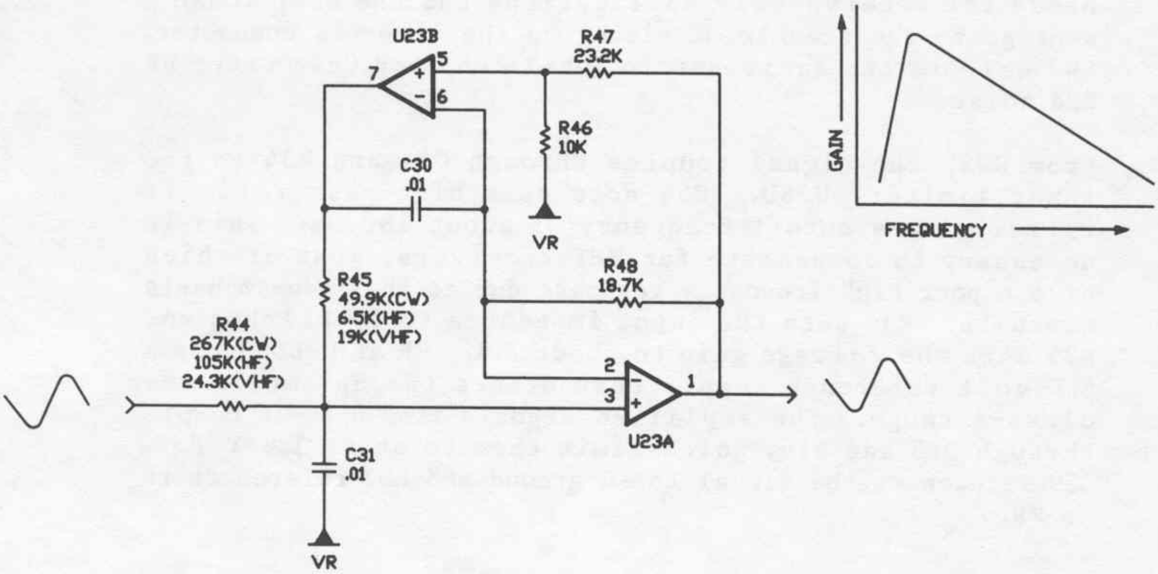
INPUT CIRCUITS

Audio signals from the external radio receiver enter the Data Controller through pin 1 of J4 (RADIO 1) or J6 (RADIO 2). J3 and J5 are two miniature phone connectors that provide an alternate audio input path. This comes in handy for receive-only applications and the user doesn't want go to the trouble of wiring up the five-pin connector. SW2 selects the active radio, while C63 and C64 filter RF and noise.

From SW2, the signal couples through C54 and R34 to the input limiter, U28D. C54 acts as a high-pass roll-off filter with a cutoff frequency of about 180 Hz. This is necessary to compensate for VHF receivers, most of which have a poor high-frequency response due to their de-emphasis circuits. R34 sets the input impedance to 10 kilohms and R35 sets the voltage gain to about 3.9. VR at U28D-12 is a 6.7-volt reference supply that biases the op amp in the class-A range. The amplified signals from U28D-14 couple through D15 and D16, which limit them to about 1.4 V P-P. C29 references the signal to AC ground and R37 references it to VR.

BANDPASS FILTER

The signals then pass through R38 to the bandpass filter. This filter consists of an input op amp at U28B, four Dual-Amplifier Bandpass Filters (DABP) at U23 and U26, and eight sets of eletronic switches at U22, U24, U25, and U27. Since all four stages are alike, only the first one will be described. Refer to the DABP schematic diagram on the next page as you read the following.



DABP Schematic Diagram

At low frequencies, C30 has a high capacitive reactance, so the negative feedback from U23B-7 to U23B-6 is relatively small. Thus, the signal coupled from U23A-1 through R48 to pin 6 will be larger than the one on pin 5. This results in U23B inverting the signal and providing negative feedback through R45, cancelling the signal from R44. In addition, since X_{C30} is greater than R48, U23A will attenuate the signal, resulting in a steep roll-off on the lower stop band.

As the frequency increases, the reactance of C30 decreases, which reduces the gain of U23B due to increased negative feedback. Since X_{C30} is decreasing, the ratio of R48 to X_{C30} is increasing, so the gain of U23A is increasing. The signal at U23B-5 will become larger than pin 6, so the output at pin 7 will become in phase with the input at R44. At the center frequency, the filter has a voltage gain of about 2. At higher frequencies, X_{C30} further decreases so that U23B becomes a unity-gain amplifier. The low-pass filter at R44 and C31 have the major effect on the signal at this time, resulting in a 6 dB/octave roll-off.

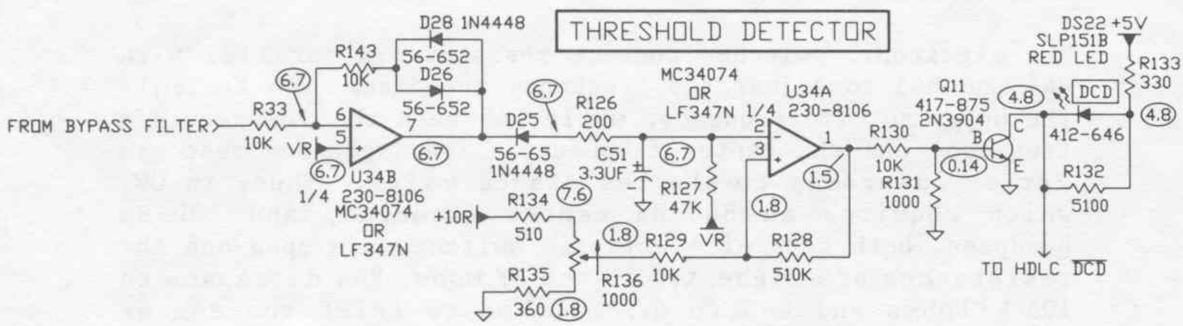
The electronic switches connect resistors in parallel with R44 and R45 to adjust the frequency response. R44 controls the upper cutoff frequency, while R45 sets the lower cutoff frequency and the center frequency. The frequency response varies inversely to the resistance value. Thus, in CW, which requires an 800-Hz center frequency and 200-Hz bandpass, both sets of electronic switches are open and the resistances are highest. In the HF mode, R44 decreases to 105 kilohms and R45 to 6.5 kilohms to shift the center frequency up to 2210 Hz, ±225 Hz. In the VHF mode, R44 decreases to 24.3 kilohms and R45 increases to 19 kilohms, thus reducing the center frequency to 1700 Hz and spreading the bandpass to 2600 Hz.

By itself, a single DABP filter won't meet the required response characteristics. The maximum gain will be toward the low end of the response curve as shown in the DABP schematic diagram. To get a steeper roll-off in the stop bands and to flatten the response, four DABP filters are cascaded and three of them are fed back to the inverting input of U28B. The feedback resistors are at R56, R68, and R78 on the Analog Circuits schematic diagram.

Without feedback, R38 and R39 set the gain of U28B to about 2.6. However, the feedback resistors will modify the gain according to the frequency of the signal. When the input signal frequency is beyond the upper or lower cutoff frequencies, the negative feedback is minimal so U28Bs gain is maximum. In the passband, the negative feedback is maximum and U23B will attenuate the incoming signal. This results in flattening the response curve while the number of DABP stages provide the gain for steep roll-off.

The output of the bandpass filter connects to the output limiter, the CW gate, and the threshold detector.

THRESHOLD DETECTOR

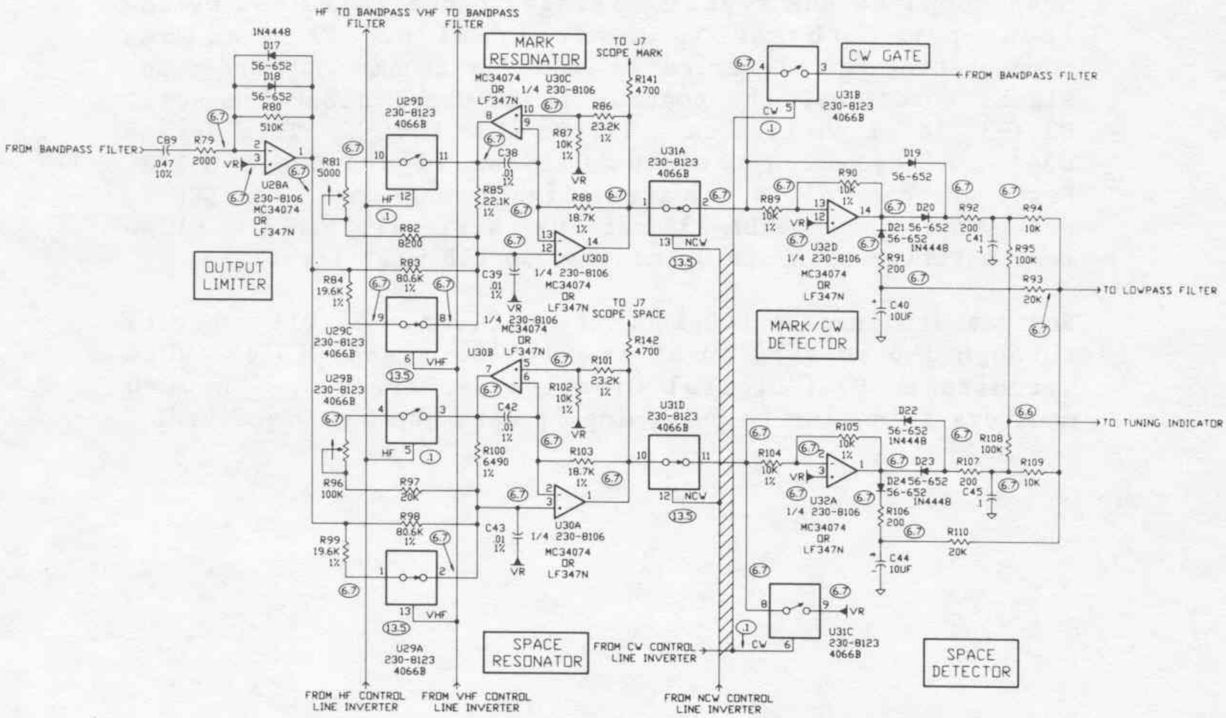


The threshold detector consists of U34B, U34A, Q11, and support components. The input stage, U34B, has a high gain when receiving weak signals and a low gain on strong signals. This is due to the logarithmic voltage/current characteristics of D26 and D28. A weak signal will generate very little feedback current, so the stage gain will be about 12.5. As the signal strength increases, the effective resistance of D26 and D28 decreases in such as fashion that the stage gain decreases logarithmically. Finally, when the diodes saturate, R33 and R143 will set the gain to unity. The result is that the threshold detector is sensitive to weak signals but won't overload on strong ones.

D25 rectifies the output of U34B-7 and couples it to R126 and C51, a low-pass filter with a cutoff frequency of about 240 Hz. The filter reduces the likelihood of the threshold detector triggering on short bursts of static. R127 references the signal to VR, so a no-signal condition is +6.7 volts and a received signal is some less-positive value.

U34A compares the signal voltage to the value set by the front-panel threshold control, R136. This allows compensating for electrically noisy environments. Under no-signal condtions, the control is adjusted clockwise until U34A-3 is slightly more positive than U34A-2. This drives U34A-1 high, which turns on Q11 and lights the DCD LED. Next, the control is adjusted slightly CCW until the LED is off. Now, when the HK-232 receives a signal, pin 2 will go less positive than pin 3 and the DCD LED will light.

Besides driving the DCD LED, the collector of Q11 connects through JP6 to send an active-low $\overline{CD}$ signal to the HDLC circuits in U7 ("Digital Circuits" schematic). The CPU monitors this line to determine if data has been received.


FROM BANDPASS FILTER
HF TO BANDPASS FILTER
VHF TO BANDPASS FILTER
MARK RESONATOR
TO J7 SCOPE MARK
CW GATE
FROM BANDPASS FILTER
OUTPUT LIMITER
MARK/CW DETECTOR
TO LOWPASS FILTER
TO J7 SCOPE SPACE
TO TUNING INDICATOR
SPACE RESONATOR
FROM CW CONTROL LINE INVERTER
SPACE DETECTOR
FROM HF CONTROL LINE INVERTER
FROM VHF CONTROL LINE INVERTER
FROM NCW CONTROL LINE INVERTER

OUTPUT LIMITER, CW GATE, AND MARK/SPACE CIRCUITS

The output limiter, U28A, consists of a high-gain op amp and clipper to remove variations in the amplitude of the mark and space signals. R79 and R80 set the voltage gain to 255 while D17 and D18 provide the clipping action. If the output goes above ±0.7 volts (referenced to VR at U28A-3) the appropriate silicon diode will conduct to cancel the signal at U28A-2.

From the output limiter, the signal connects to the mark and space resonators, which consist sections of U29 and U30. Both circuits are DABP filters and function in the same manner as the ones in the bandpass filter. The only difference is that the resonators need to be tuned to a specific set of frequencies, so there's no negative feedback to flatten the response curve. The mark resonator consists of U29C, U29D, U30C, and U30D. In the VHF mode, the U29D-12 is low to open U29D while U29C-6 is at +13 volts to close it. The space resonator at U29A, U29B, U30A, and U30B functions in the same manner, except that its resistors are slightly smaller since it's operating at the higher frequency. The result is that the mark frequency is about 1100 Hz and the space frequency is about 2100 Hz.

In the HF mode, the two sets of electronic switches toggle to their opposite states. As mentioned in the DABP filter description, the input resistors (in this case R83 and R98) set the upper cutoff frequency while the feedback resistors (R85 and R100) control the center frequency and lower cutoff frequency. Thus, the input switches are open to reduce the upper cutoff frequency and the feedback switches are closed to raise the lower cutoff and center frequencies. This narrower response is necessary because the mark and space tones are only 230 Hz apart (2080/2310 Hz) instead of the 1000 Hz difference of VHF.

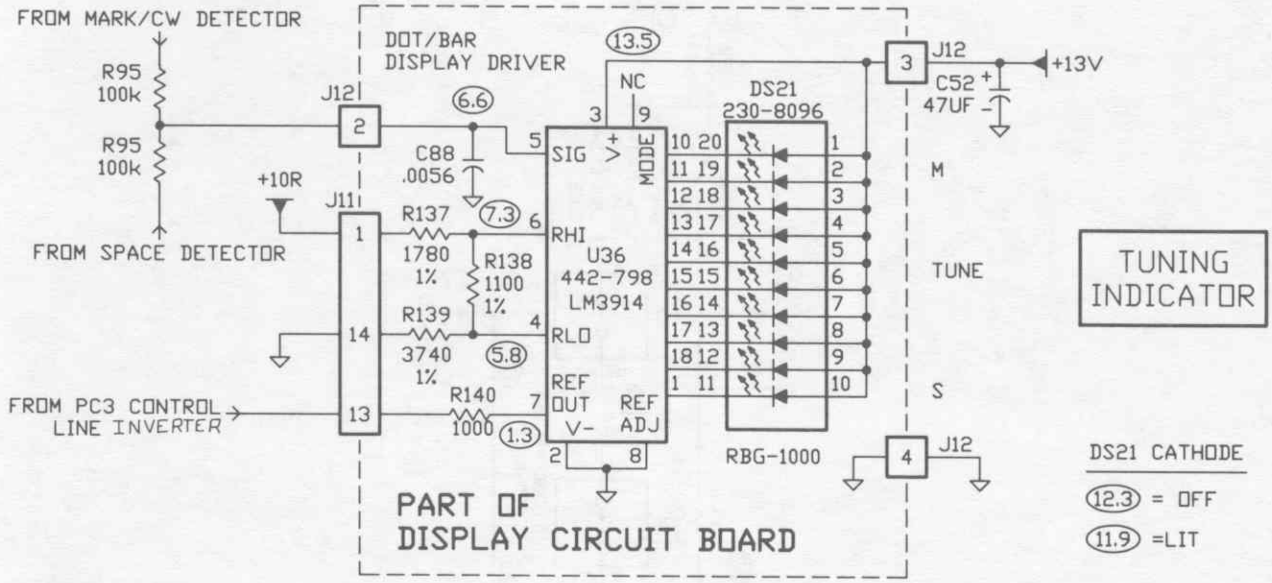
The outputs of the mark/space resonators connect through R141 and R142 to the scope interface at J7 (right side of the "Analog Circuits" schematic). The main signal path, however, is through the electronic switches at U31A and U31D to the inputs of the mark/CW and space detectors. The NCW control line keeps the switches closed in all modes but Morse Code. In that mode, NCW goes low to open the switches and CW goes to +13 volts to close the CW gate, U31B. This couples the output of the bandpass filter directly to the input of the mark/CW detector. CW also connects to U31C-6 to connect VR to the input of the space detector, disabling it.

The mark/CW detector is a precision full-wave rectifier with a gain of unity, set by R89 and R90. VR, at U32D-12 provides class-A bias. This voltage is also the reference for the detector signals. Note that when the following description refers to a positive or negative voltage, the polarity is relative to VR. That is, positive is greater than +6.7 volts and negative is some value between 0 volts and +6.7 volts.

D19 and D20 provide rectification. On positive-input signals, D19 conducts to couple the signal directly to the filter. D20 is reverse biased to isolate the output of U32D-14. When the signal goes negative (with respect to VR at U32D-12), U32D-14 goes high, D20 conducts, and D19 turns off. The low-pass filter at R92 and C41 restores the original signal from the pulsating DC. The cutoff frequency is about 8 kHz to ensure capturing data at 9600 baud. D21, R91, and C40 also rectify and filter the mark/CW signal. The filter has a longer duty cycle to generate a negative DC voltage to maintain the correct bias levels to the following stage.

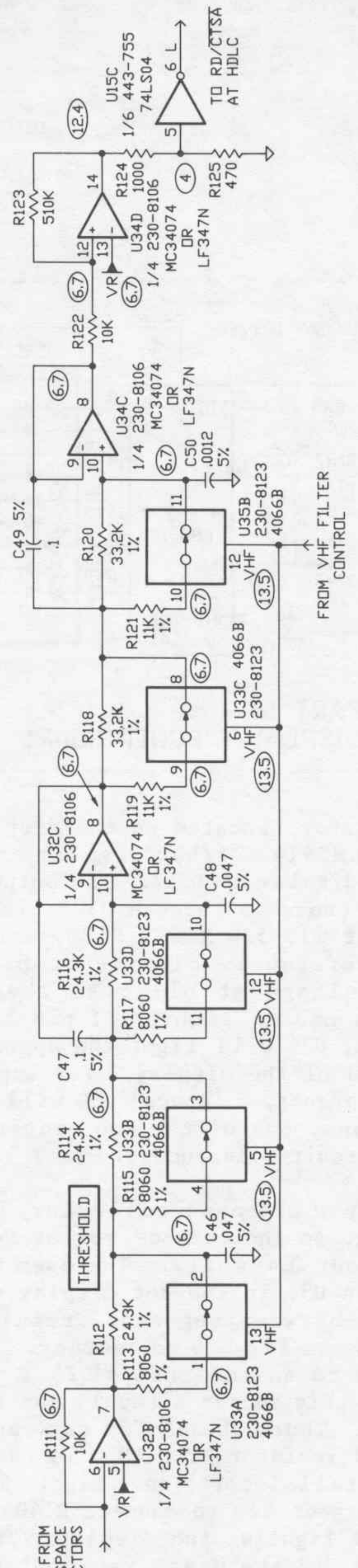
The space detector at U32A functions in the same manner as the mark detector, except that the voltage polarities are reversed. The outputs of both detectors connect through a summing network consisting of R93, R94, R109, and R110 to the input of the low-pass filter driver, U32B. Another summing network R95 and R108 couples the demodulated signal outputs to the tuning indicator.

TUNING INDICATOR



The tuning indicator, located on the display circuit board, consists of an LM3914 dot/bar display driver at U36 and a RBG-1000 10-LED display at DS21. The output of the R95/R108 summing network connects through J12-2 to the signal input of the driver at U36-5. R137, R138, and R139 set up the low and high reference voltages at pins 4 and 6. U36 compares the voltage at pin 5 to these references to determine which LED to light. If pin 5 is closer to the voltage at pin 6, U36 will light the appropriate LED closer to the "mark" end of the display. For input voltages close to the pin 4 reference, a "space" LED will light. Under no-signal conditions, one of the two center LEDs will light (depending on circuit tolerances).

The driver outputs are open-collector, but have built-in current limiting, so the cathode voltage of a lit LED will only drop by about 0.4 volts. The open connection at the MODE, U36-9, puts U36 in the dot display mode. This causes a 1 mV overlap between segments, resulting in a smooth transition from one lit LED to another. The REF OUT line, pin 7, connects to an internal +1.25 V reference source. The current from this source directly controls the intensity of the lit LEDs. Thus, the HK-232 can control the display through the load resistor at R140. To turn on the display, PC3 (from the parallel port) goes high. The open-collector output at U18D-8 goes low to connect R140 to ground, causing current flow and lighting the display. The remaining line, REF ADJ at pin 8, is the negative input to REF OUT and is grounded to complete the circuit.

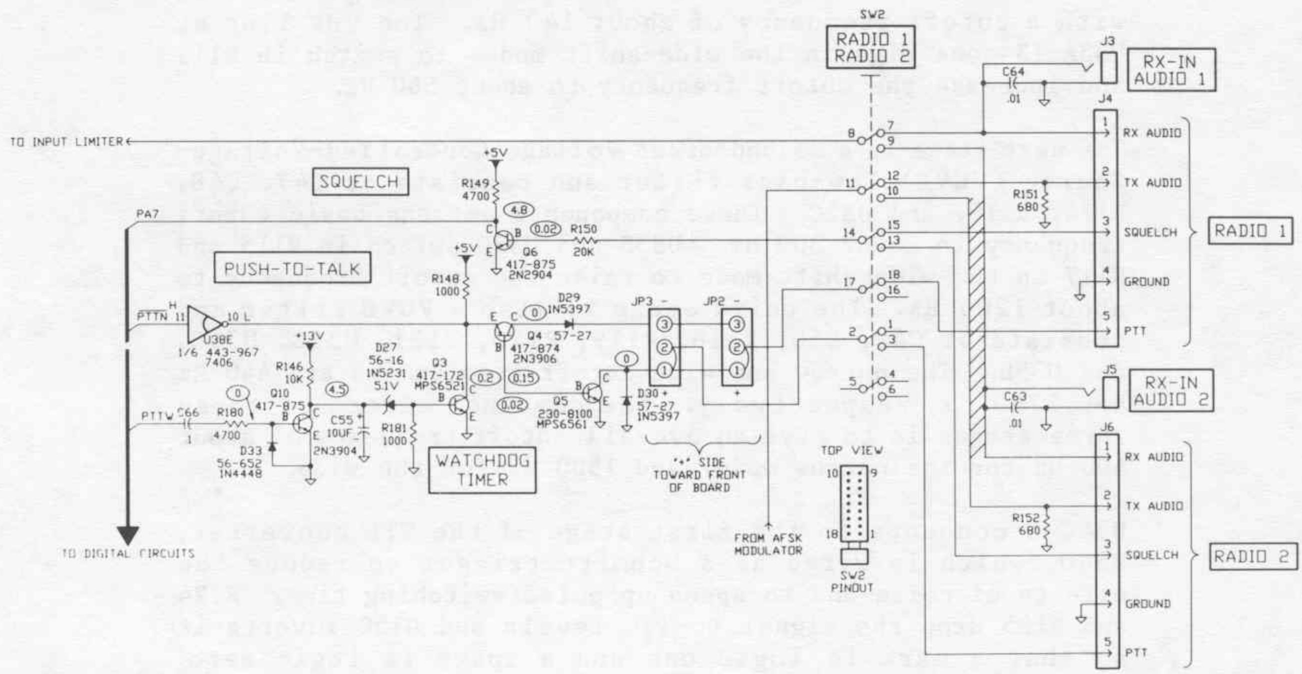

FROM MARK/CW/SPACE DETECTORS
R111 10K
U32B 1/4 230-8106 MC34074 OR LF347N
R113 8060 1%
R112 24.3K 1%
U33A 230-8123 4066B
C46 .047 5%
THRESHOLD
R115 8060 1%
R114 24.3K 1%
U33B 230-8123 4066B
C47 .1 5%
R117 8060 1%
R116 24.3K 1%
U33D 230-8123 4066B
C48 .0047 5%
U32C 1/4 230-8106 MC34074 OR LF347N
R119 11K 1%
R118 33.2K 1%
U33C 4066B 230-8123
R121 11K 1%
R120 33.2K 1%
C49 5% .1
U35B 230-8123 4066B
C50 .0012 5%
FROM VHF FILTER CONTROL
U34C 1/4 230-8106 MC34074 OR LF347N
R122 10K
R123 510K
U34D 1/4 230-8106 MC34074 OR LF347N
R124 1000
R125 470
U15C 1/6 443-755 74LS04
TO RD/CTSA AT HDLC

LOW-PASS FILTER AND TTL CONVERTER

The low-pass filter consists of sections of U32, U33, U34, and U35. U32C is a unity-gain inverter that isolates the outputs of the detectors from the filter. The output will go low for a mark and high for a space. C46 and R112 form the first filter stage. This is a passive low-pass filter with a cutoff frequency of about 140 Hz. The VHF line at U33A-13 goes high in the wide-shift modes to switch in R113 and increase the cutoff frequency to about 560 Hz.

The next stage is a second-order Voltage-Controlled-Voltage-Source (VCVS) low-pass filter and consists of C47, C48, R114, R116, and U32C. These components set the basic cutoff frequency to about 300 Hz. U33B and U33D switch in R115 and R117 in the wide-shift mode to raise the cutoff frequency to about 1200 Hz. The third stage is also a VCVS filter and consists of C49, C50, R118, R119, R120, R121, U33C, U34C, and U35B. The narrow and wide cutoff frequencies are 440 Hz and 1760 Hz, respectively. The combined effect of these three stages is to give an overall cutoff frequency of about 400 Hz for the narrow mode, and 1500 Hz for the wide.

U34C-8 connects to the first stage of the TTL converter, U34D, which is wired as a Schmitt trigger to reduce the effects of noise and to speed up pulse switching time. R124 and R125 drop the signal to TTL levels and U15C inverts it so that a mark is logic one and a space is logic zero. U15C-6 couples the recovered serial data through JP4 to the RD input of the HDLC (U7-13 on the "Digital Circuits" schematic) in the packet radio mode and into the $\overline{\text{CTSA}}$ input (U7-18) for all other modes.


TO INPUT LIMITER
SQUELCH
PUSH-TO-TALK
PA7
PTTN
PTTW
TO DIGITAL CIRCUITS
U38E
1/6 443-967
7406
R149
4700
Q6
417-875
2N2904
R150
20K
R148
1000
D29
1N5397
Q4
57-27
417-874
2N3906
D27
56-16
1N5231
5.1V
Q3
417-172
MPS6521
R146
10K
Q10
417-875
R180
4700
C66
C55
10UF
2N3904
D33
56-652
1N4448
R181
1000
WATCHDOG
TIMER
Q5
230-8100
MPS6561
D30
57-27
1N5397
JP3
JP2
"+" SIDE
TOWARD FRONT
OF BOARD
SW2
RADIO 1
RADIO 2
TOP VIEW
SW2
PINOUT
FROM AFSK
MODULATOR
C64
.01
J3
RX-IN
AUDIO 1
J4
RX AUDIO
TX AUDIO
SQUELCH
GROUND
PTT
R151
680
RADIO 1
C63
.01
J5
RX-IN
AUDIO 2
J6
RX AUDIO
TX AUDIO
SQUELCH
GROUND
PTT
R152
680
RADIO 2

Transmitter Circuits

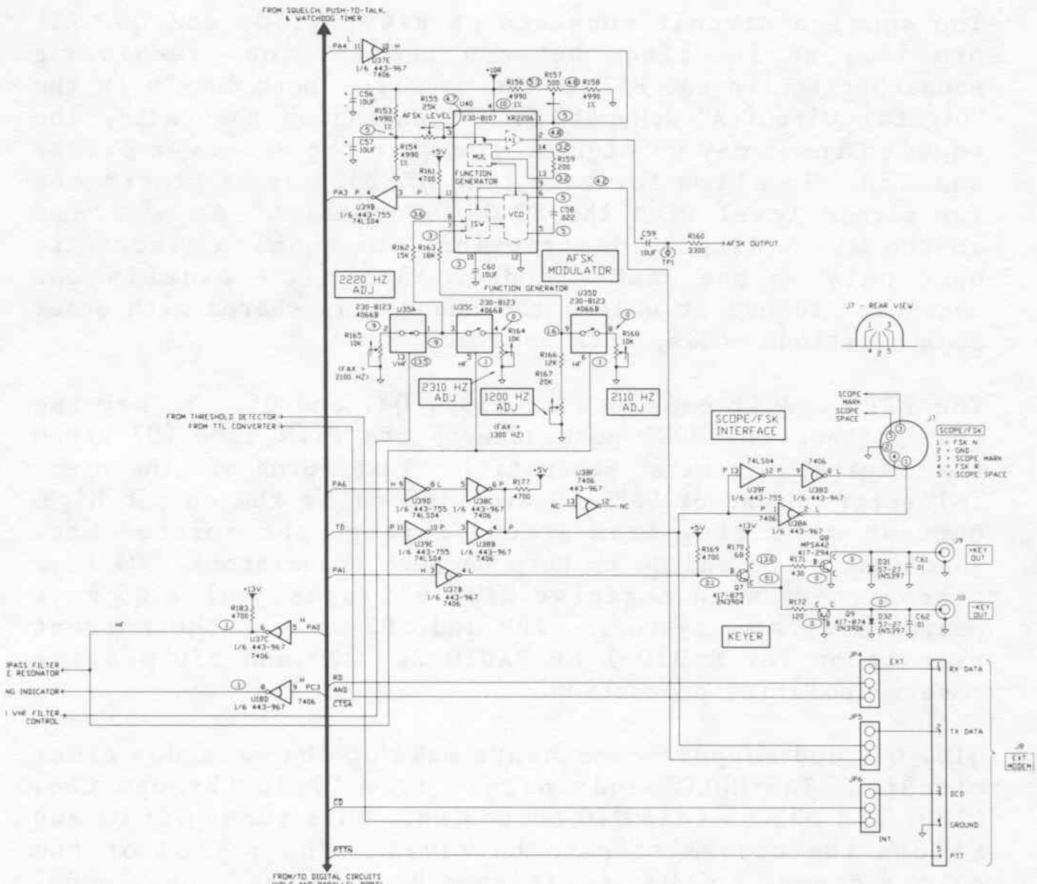
Refer to the right side of the Analog Circuits schematic as you read the following.

SQUELCH, PUSH-TO-TALK, AND WATCHDOG TIMER

The squelch circuit consists of R149, R150, and Q6. It provides an interface between the external receiver's squelch circuits and PA7 of the parallel port (U6-26 on the "Digital Circuits" schematic). Depending on the radio, the squelch input may go high or low when the receiver breaks squelch. To allow for this, the HK-232 may be programmed for either level with the SQ ON/OFF command. As mentioned in the block diagram description, the squelch circuit is used only in the packet mode. Also, it's usually not necessary to use it unless the channel is shared with other communications modes, such as voice.

The PTT circuit consists of U38E, Q4, and Q5. To key the transmitter, the HDLC port asserts the $\overline{\text{PTTN}}$ line (U7-17 on the "Digital Circuits" schematic). This turns off the open-collector output of U38E-10 and R148 pulls the output high. Current will flow from ground through the emitter-base junctions of Q5 and Q4 to turn on both transistors. Q4 keys transmitters with negative bias voltages, while Q5 keys positive-voltage systems. JP2 and JP3 select the correct transistor for RADIO 1 or RADIO 2. D29 and D30 provide reverse polarity protection.

Q10, Q3, and support components make up the watchdog timer circuit. The HDLC sends pulses from U7-16 through C66, R180, and D33 to keep Q10 turned on. This turns off Q3 and allows the transmitter to be keyed. The period of the pulses depend on the operating mode. In the packet mode, it's about 5 mS. In other modes, it will vary from 2 mS to 4 mS. In all modes, the duty cycle is 50%. On a scope, the signal display will jitter since the CPU is handling interrupts and other functions.


FROM SQUELCH, PUSH-TO-TALK, & WATCHDOG TIMER
AFSK LEVEL
FUNCTION GENERATOR
AFSK OUTPUT
AFSK MODULATOR
2220 HZ ADJ
2310 HZ ADJ
1200 HZ ADJ
2110 HZ ADJ
(FAX = 2100 HZ)
(FAX = 1300 HZ)
J7 - REAR VIEW
SCOPE/FSK INTERFACE
SCOPE MARK
SCOPE SPACE
SCOPE/FSK
1 = FSK N
2 = GND
3 = SCOPE MARK
4 = FSK R
5 = SCOPE SPACE
FROM THRESHOLD DETECTOR
FROM TTL CONVERTER
KEYER
+KEY OUT
-KEY OUT
RX DATA
TX DATA
DCD
GROUND
PTT
EXT MODEM
FROM/TO DIGITAL CIRCUITS (HDLC AND PARALLEL PORT)

If a major component fails, such as the CPU or HDLC, it's likely that PTTW would stop pulsing. If so, Q10 would turn off and C55 would start charging through R146. After about 60 mS, the 5.1 V zener diode at D27 would conduct and turn on Q3. In turn, Q3 would turn off Q4 and Q5 to shut down the transmitter.

AFSK MODULATOR

The Audio-Frequency-Shift-Keying (AFSK) modulator is an XR2206 function generator at U40. Electronic switches at U35A, U35C, and U35D select the operating frequency while various inverters in U37, U38, and U39 interface U40 to the parallel and HDLC ports (U6 and U7 on the "Digital Circuits" schematic).

Depending on the operating mode, the modulating signal can arrive through one of two paths. In the packet radio mode, the TD line (from U7-15) sends the serial data through U39E to the open-collector inverter at U38B. At this time, PA6 (from U6-27) is high to prevent blocking the signal. In other operating modes, TD goes high and PA6 generates the serial data.

The outputs of the inverters couple through JP5 to the modulating input at U40-9. Internally, the signal connects to a current switch labeled ISW. This section controls the frequency of the VCO by selecting the resistor networks at pins 8 and 9. Pin 8 generates the space tones when pin 9 is low. In the wideshift mode, U35A closes and R165 sets the frequency to 2220 Hz. For narrow modes, U35A opens and U35C closes to shift the space frequency to 2310 Hz. In the Morse code mode, both switches are open so that no tone is generated. When pin 9 is high, pin 7 sets the mark frequency; this is 1200 Hz for wideshift/CW and 2110 Hz for narrow shift. Optionally, R168 and R167 can be adjusted to a 2100/1300-Hz shift for facsimile transmission. Adjusting any of these controls CCW will lower the frequency, while CW raises it.

U40-11 is an open-collector output from the VCO and is used during transmitter alignment. It couples through U39B to PA3 of the parallel port, U6-30. The CPU can compare the frequency of the signal with its clock and determine if the VCO is at the correct frequency. The other VCO output connects internally to a multiplier stage that functions as a wave shaper and tone null circuit. R159 at pins 13 and 14 is part of the waveshaping circuit that feeds back to the VCO to force it to generate a sine wave.

U40-1 is the tone null input. The bias voltage from R156, R157, and R158 controls the amplitude of the AFSK signal. The null voltage is about +5 VDC. When R157 is adjusted through this value the signal amplitude will decrease, go through zero, reverse phase, and then increase. When R157 is properly adjusted, the signal will be either completely nulled or at maximum amplitude, depending on the output of U37E, an open-collector inverter. During any mode but transmit, U37E-10 is open, so the signal is nulled. During transmit, pin 10 goes low and the multiplier will pass the AFSK signal to the AFSK level control and the output buffer. C57, R153, R154, and R155 control the signal level by a combination of shunting the signal and biasing the final stage. The lower the resistance of R155, the smaller the signal.

The output buffer couples the AFSK signal from U40-2, through C59 and R160 to the RADIO 1/RADIO 2 switch. R151 and R152 provide impedance matching to the transmitter microphone input and, in conjunction with R160, drops the signal level from about 1.4 V P-P to about 200 mV P-P to prevent overloading the transmitter.

At U40-10, C60 ensures VCO frequency stability and C56 at U40-4 decouples power supply noise.

FSK INTERFACE

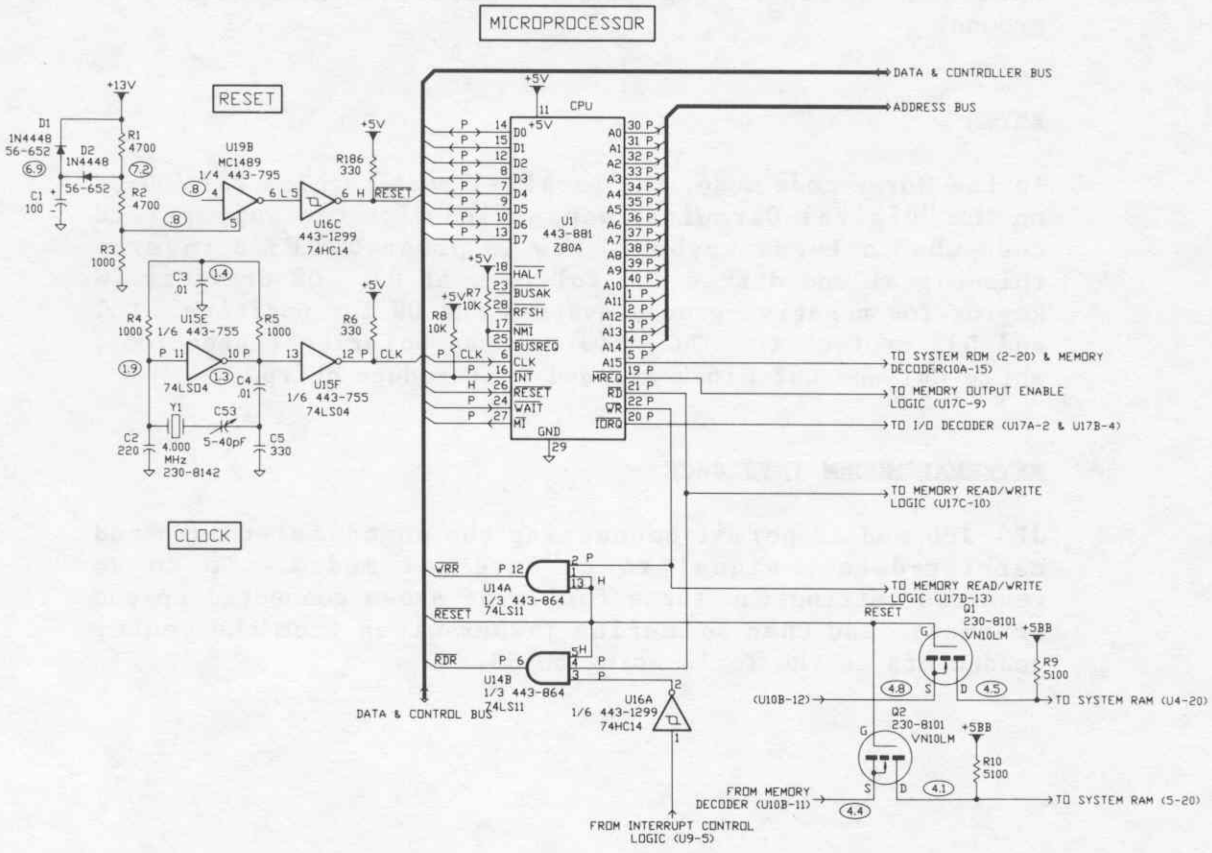
Besides driving the AFSK generator, the serial data from U38B and U38C also connect to the FSK interface. U39F and U38D provide a noninverted output and U38A an inverted output. Both outputs are open-collector to allow connecting a variety of external FSK modulators to J7. Although the external pullup voltage must be positive with respect to ground.

KEYER

In the Morse code mode, the parallel port toggles PA1 (U6-32 on the "Digital Circuits" schematic) with the appropriate code when a legal keyboard key is pressed. U37B inverts this signal and drives the follower at Q7. Q8 provides CW keying for negative-ground systems and Q9 for positive. D31 and D32 protect the TNC from reverse-polarity connections, while C61 and C62 block RFI and help reduce chirp.

EXTERNAL MODEM INTERFACE

JP4-JP6 and J8 permit connecting the unmodulated data and carrier-detect signal to an external modem. To do so requires cutting the three foil runs shown connected on the schematic and then soldering jumper wires from the center conductors to the foils going to J8.


MICROPROCESSOR
RESET
CLOCK
+13V
D1
1N4448
56-652
D2
1N4448
56-652
C1
100
R1
4700
R2
4700
R3
1000
U19B
MC1489
1/4 443-795
U16C
443-1299
74HC14
R186
330
+5V
RESET
C3
.01
R4
1000
U15E
1/6 443-755
74LS04
R5
1000
U15F
1/6 443-755
74LS04
R6
330
CLK
C4
.01
C2
220
Y1
4.000
MHz
230-8142
C53
5-40pF
C5
330
CPU
U1
443-881
Z80A
HALT
BUSAK
RFSH
NMI
BUSREQ
CLK
INT
RESET
WAIT
M1
GND
R7
10K
R8
10K
MREQ
RD
WR
IORQ
DATA & CONTROLLER BUS
ADDRESS BUS
TO SYSTEM ROM (2-20) & MEMORY DECODER(10A-15)
TO MEMORY OUTPUT ENABLE LOGIC (U17C-9)
TO I/O DECODER (U17A-2 & U17B-4)
TO MEMORY READ/WRITE LOGIC (U17C-10)
TO MEMORY READ/WRITE LOGIC (U17D-13)
VRR
U14A
1/3 443-864
74LS11
RDR
U14B
1/3 443-864
74LS11
DATA & CONTROL BUS
U16A
1/6 443-1299
74HC14
FROM INTERRUPT CONTROL LOGIC (U9-5)
Q1
230-8101
VN10LM
+5BB
R9
5100
(U10B-12)
TO SYSTEM RAM (U4-20)
Q2
230-8101
VN10LM
R10
5100
FROM MEMORY DECODER (U10B-11)
TO SYSTEM RAM (5-20)

Digital Circuits

RESET CIRCUITS

The reset circuits consist of C1, D1, D2, R1-R3, R186, U16C, and U19B. At powerup, C1 begins to charge through D2 and R1. The output of D2 couples through R2 to the response control line at U19B-5. Internally, this line connects directly to the base of a common-emitter NPN transistor, so the output at U19B-5 remains high until the input rises to about +0.6 volts.

The CMOS Schmitt trigger at U16C inverts the high to generate the active-low $\overline{\text{RESET}}$ signal at pin 6. Due to the time constant of R1/C1, $\overline{\text{RESET}}$ remains low for about 250 mS. This gives time for the two crystal oscillators to stabilize and for the LSI chips to initialize their internal registers. Once C1 charges, U16C-6 goes high and releases the HK-232 from the reset state. The pullup resistor at R186 ensures a fast rise time by overcoming the relatively high input capacitance of Q1 and Q2 (about 48 pF each).

Q1 and Q2 are VN10LM n-channel enhancement-mode VMOS power FETs. The $\overline{\text{RESET}}$ line turns off these transistors during reset to protect the battery-backed RAM. R9 and R10 will pull the chip select lines high and prevent glitches on the data bus from being written into memory. At the end of reset, both FETs saturate and conduct the chip-select signals from U10B to U4-20 and U5-20.

U16C-6 resets the Z80 by connecting directly to U1-26. (See "Central Processing Unit" for more information.) U16C indirectly resets the serial and parallel ports by simultaneously asserting $\overline{\text{WRR}}$ at U14A-12 and $\overline{\text{RDR}}$ at U14B-6. Normally, these two lines will not go low at the same time, so U6 and U7 are designed to recognize this condition as a hard reset. (See "Parallel Ports and Timers" and "RS-232C and HDLC Ports.")

The remaining reset component, D1, serves to rapidly discharge C1 when the HK-232 is turned off. This ensures the 250 mS reset time if the unit is immediately turned on again.

SYSTEM CLOCK

The system clock, CLK, provides timing to the Z80 at U1-6, the parallel port at U6-16, and the interrupt control logic at U9-8. These circuits generate secondary timing signals that are synchronized to CLK. The clock circuitry consists of C2-C5, C53, R4-R6, U15E, U15F, and Y1. These components generate a 4 MHz TTL-level square wave with a 50% duty cycle.

At powerup, the voltage surge through C4 shocks the crystal at Y1 into oscillation. The crystal, along with C2, C5, and C53, provide positive feedback to U15E-11 to maintain oscillation. R4 and R5 bias U15E into its linear range. Since these are relatively low-value resistors (necessary for TTL), C3 shunts the signal to ground to prevent negative feedback. C53 sets the resonant frequency to exactly 4 MHz. Trimming the frequency is necessary because the system clock provides the basic timing for the time-of-day and date functions. In addition, the CPU uses it as a reference when the HK-232 is in the calibrate mode.

U15F provides load isolation for the oscillator output. R6 is a pullup resistor to ensure that the system clock meets specifications for the CPU clock input line (high = Vcc - .6 volts).

CENTRAL PROCESSING UNIT

The CPU is a Z80A at U1 operating at 4 MHz. This processor executes the programs stored in memory to control all the functions in the HK-232. The Z80A was selected for its versatile instruction set (158 different types) and large number of internal registers. These include two 8-bit accumulators and flag registers, twelve 8-bit general-purpose registers, two 8-bit special-purpose registers, and four 16-bit special-purpose registers.

The Z80 registers communicate with other circuits in the HK-232 through the bidirectional data bus at D0-D7 and the address bus at A0-A15. The CPU also has several lines for controlling and monitoring the status of the circuits it's communicating with. Basically, these lines function as follows. (See the **Z80 CPU/Z80A CPU** Blue Book for detailed information.)

Pins 1-5 and 30-40, A0-A15: Address bus. The Z80 uses these output lines to select a specific I/O port or memory location. A0-A7 are used to select I/O, thus allowing up to 256 I/O ports. In certain types of I/O instructions, the contents of the B register is placed on the upper eight address bits, A8-A15. All sixteen lines are used to address a byte in memory. This permits the Z80 to directly address up 65536 bytes of RAM or ROM. The address lines are active high. That is, at address zero all lines are low, while at address FFFFH all lines are high.

The address bus also provides a refresh function for systems using dynamic RAMs. It does this at the end of each instruction fetch cycle by placing the contents of the refresh register onto A0-A7. It then increments the refresh register so a different refresh address will be placed on the bus during the next instruction fetch. During refresh, only A0-A6 are incremented, A7 is held at logic zero, and the contents of the interrupt page address register are placed on A8-A15.

Pin 6, CLK: Clock. The signal on this input line provides all the internal timing to the Z80. In the HK-232, this signal is a 4-MHz TTL square wave with a 50% duty cycle.

Pins 7-10 and 12-15, D0-D7: Data bus. These eight bi-directional bus lines permit the Z80 to communicate with memory and I/O. During a read operation, these are input lines, so data travels from the addressed device to the CPU. During a write, they're output lines, so the CPU can transfer data to the addressed device.

Pin 16, INT: Interrupt request. This active-low input line allows I/O devices to request processor time. When the Z80 senses the low, it completes its current instruction and sends an interrupt-acknowledge signal (INTACK--see "Interrupt Control Logic") to the device. The HK-232 uses Mode 2 interrupts, so the interrupting device sends an 8-bit vector address to the Z80. In turn, the CPU combines this byte with the contents of its **I** register, forming a 16-bit vector address. This address holds the location of the appropriate interrupt-handling program which the Z80 calls in the same way it would a subroutine. Once the Z80 has processed the interrupt, it returns to the previous program and continues with it.

Only two devices use the interrupt request line, the parallel port at U6-24 and the serial port at U7-5. Both lines are open-drain, hence the 10-kilohm pullup resistor at R8 (near U1-16).

Note that the interrupt request line at pin 16 can be disabled (masked) through software control. When masked, a logic zero at INT won't affect Z80 operation.

Pin 17, NMI: Nonmaskable Interrupt. This input control line is similar to the INT line at pin 16, except that it can't be disabled through software control. Also, it's triggered on the negative-going edge of the input rather than on a logic zero. The NMI line isn't used in the Z80, so it's tied high through R7. In case a voltage spike in the power supply should generate an NMI, the Z80 will perform a restart instruction to address 0066H. In Release 3.0 of the HK-232 system ROM, this location contains a jump instruction to address zero, so the system will merely re-initialize itself.

Pin 18, HALT: Halt. This output line goes low to indicate that the Z80 has executed a HALT instruction. While halted, the Z80 will execute NOPs to maintain memory refresh activity. The only way to restart the processor is to generate an interrupt or a hard reset. The HALT line isn't used in the HK-232, so it's not connected.

Pin 19, $\overline{\text{MREQ}}$: Memory Request. The CPU pulls this output control line low when it needs to read or write memory. The low indicates that the address bus holds a valid address.

Pin 20, $\overline{\text{IORQ}}$: Input/Output Request. The CPU pulls this output control line low when it needs to read or write a port. The low indicates that the lower 8 bits of the address bus holds a valid I/O port address.

Pin 21, $\overline{\text{RD}}$: Read. When low, this output control line indicates that the Z80 is ready to read data from the addressed memory or I/O device. The addressed device uses this signal to gate the data onto the data bus.

Pin 22, $\overline{\text{WR}}$: Write. When low, this output control line indicates that the Z80 data bus holds valid data to be stored in the addressed or I/O device.

Pin 23, $\overline{\text{BUSACK}}$: Bus Acknowledge. When low, this output control line indicates to the requesting device that the CPU has given up control of the system address, data, and control busses. (See **Pin 25, $\overline{\text{BUSREQ}}$** for more details.) This circuit isn't used in the HK-232, so it's not connected.

Pin 24, $\overline{\text{WAIT}}$: Wait. When low, this input control line puts the Z80 into a wait state. Data, address, and control lines will remain in their current logic state until pin 24 goes high. In the HK-232, the wait line is used to give the serial and parallel ports time to respond to an interrupt-acknowledge signal. (See "Interrupt Control Logic.")

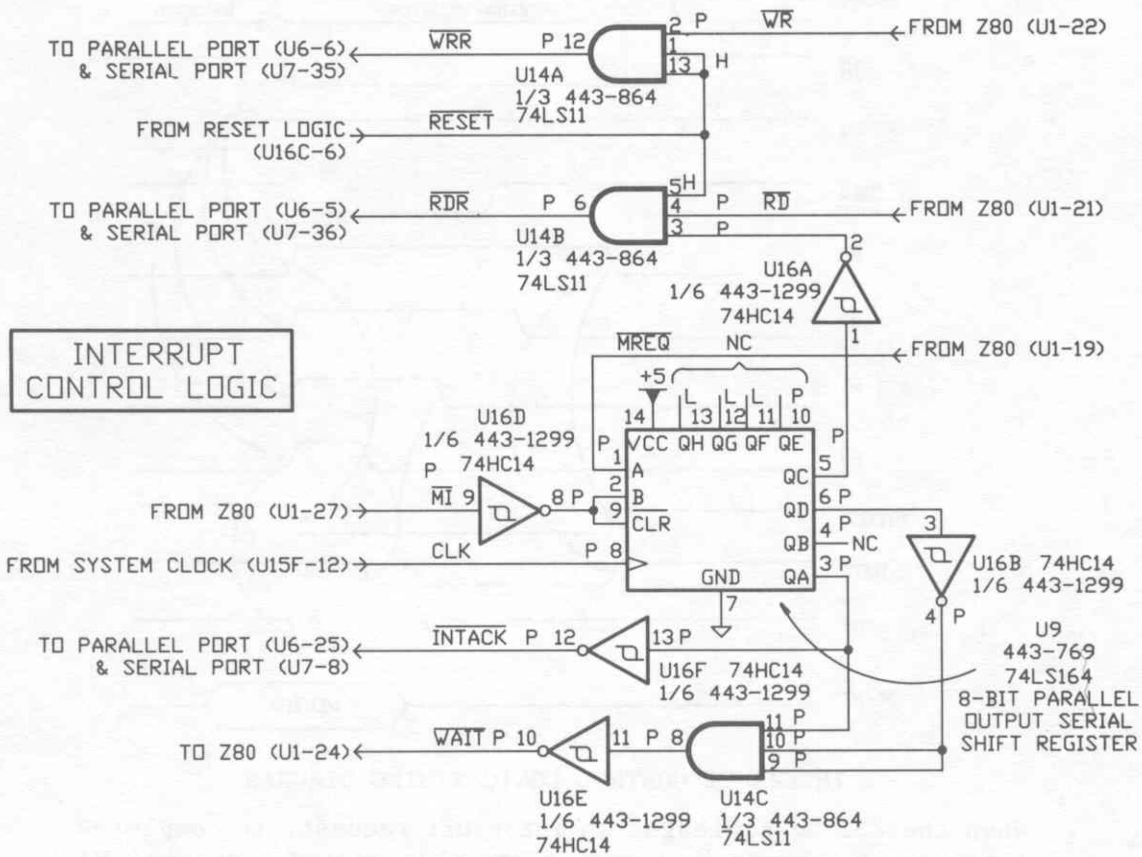
Pin 25, $\overline{\text{BUSREQ}}$: Bus Request. This input is a control line that's used by DMA circuits to gain access to the system bus. When low, the Z80 halts operation and its address, data, and output control lines enter a high-impedance state. DMA isn't used in the HK-232, so this line is tied high through R7.

Pin 26, $\overline{\textbf{RESET}}$: Reset. When brought low, this input control line halts all CPU operation. It disables interrupts and sets the interrupt mode to zero. The program counter, interrupt vector register, and refresh registers are cleared. During reset time, the address and data bus go to a high-impedance state, and all control output signals go high. No memory refresh occurs.

Pin 27, $\overline{\textbf{M1}}$: Machine cycle one. This output line pulses low when when the Z80 is fetching an instruction from memory. The pulse occurs during the first half of the M1 cycle when the instruction is fetched. During the second half of the M1 cycle, the Z80 is internally processing the instruction and doesn't need to access the bus. It's during this time that a memory refresh takes place.

Pin 28, $\overline{\textbf{RFSH}}$: Refresh. This output control line goes low during the second half of an M1 cycle to inform external circuits that a dynamic RAM refresh is taking place. During this time, the rest of the Z80 is internally processing an instruction and does not need to access the busses. Instead, the Z80 places the contents of the refresh register on A0-A6 and pulses $\overline{\text{MREQ}}$. External circuits decode these lines to perform a memory read to refresh the RAM. (Note that there's no data transfer, however.) This results in a transparent refresh and eliminates the need for arbitration logic, which would otherwise slow down system operation. Since the HK-232 uses static RAMs, pin 28 isn't connected.

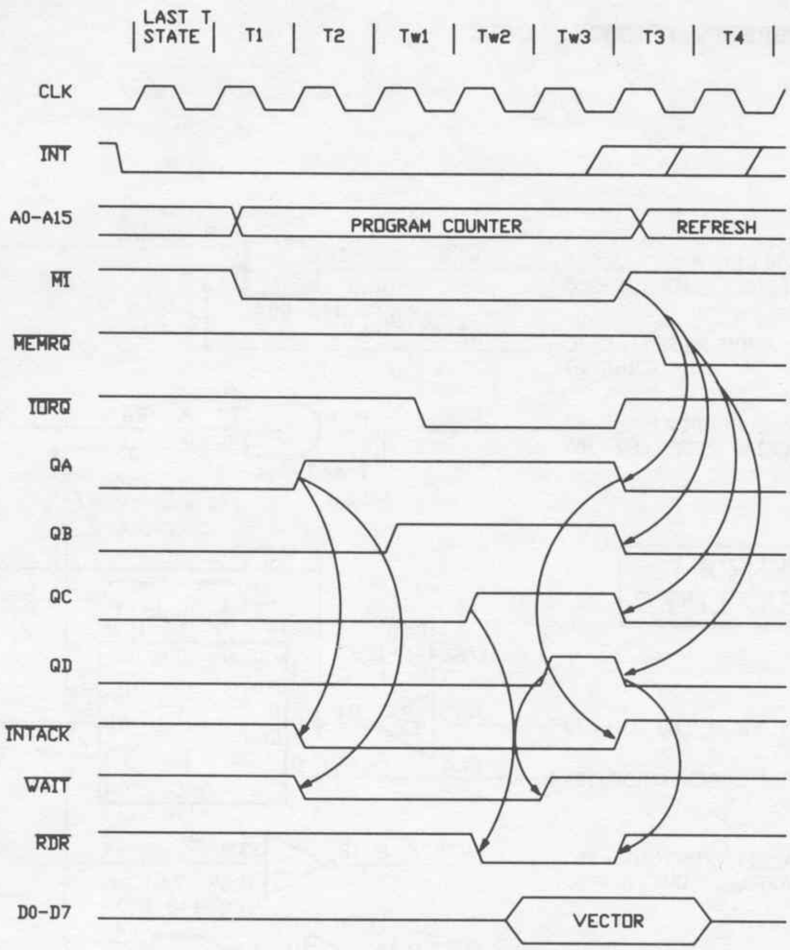
INTERRUPT CONTROL LOGIC



INTERRUPT CONTROL LOGIC

During an interrupt-acknowledge sequence, the interrupt control logic provides the correct timing and control signals to the Z80 and the serial and parallel ports. The circuitry consists of a 74LS164 8-bit parallel output shift register at U9 plus some gates and inverters in U14 and U16. These circuits monitor the $\overline{\text{MREQ}}$ and $\overline{\text{M1}}$ lines from the Z80, and the CLK line from the 4-MHz clock circuits. The outputs are $\overline{\text{RDR}}$ and $\overline{\text{INTACK}}$ to the serial and parallel ports, and $\overline{\text{WAIT}}$ to the Z80.

Refer to the Interrupt Control Logic timing diagram as you read the following.



INTERRUPT CONTROL LOGIC TIMING DIAGRAM

When the Z80 acknowledges an interrupt request, it completes the current program instruction and then begins a special M1 cycle. This is similar to a standard instruction-fetch cycle, except that the CPU inserts two wait states at Tw1 and Tw2. U9 adds a third wait state at Tw3 to allow the interrupting device time to respond to the acknowledge signal.

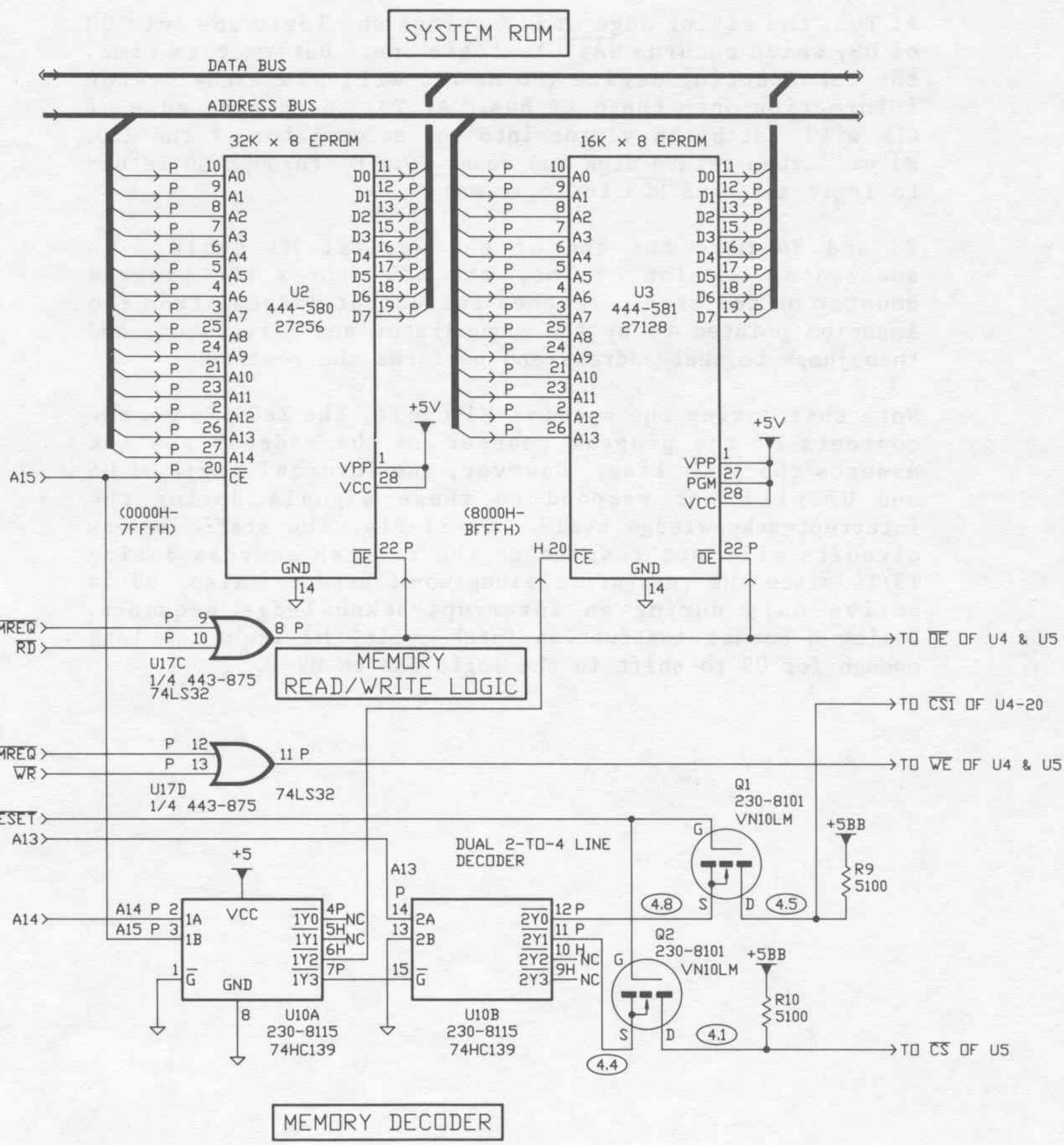
At T1, $\overline{\text{M1}}$ goes low to remove the clear signal at U9-9 and to place a logic one on the B serial input, U9-2. The MREQ signal from the Z80 connects to the A serial input at U9-1 and is also high. At T2, the CLK pulse at U9-8 shifts this high into QA, U9-3. This in turn asserts $\overline{\text{INTACK}}$ through U16F and $\overline{\text{WAIT}}$ through U14C and U16E. The $\overline{\text{INTACK}}$ line connects to the parallel and serial ports, U6-25 and U7-8, respectively, to inform the interrupting device that it can place the vector on the data bus. The logic zero at U16E-10 connects to the Z80 $\overline{\text{WAIT}}$ input at U1-24. The Z80 will ignore this signal at this time as it inserts its own two wait states first.

At Tw1, U9 shifts the logic one into QB, which is unconnected. At Tw2, U9 shifts the high to QC, which drives $\overline{RDR}$ low through U16A and U14B. Half way through Tw2, the falling edge of CLK and the low on $\overline{WAIT}$ causes the Z80 to generate one more wait state, Tw3.

At Tw3, the rising edge of CLK shifts the logic one into QD of U9, which returns $\overline{WAIT}$ to logic one. During this time, the interrupting device (U6 or U7) will place the vector information onto the data bus. At T3, the rising edge of CLK will latch the vector into the accumulator of the Z80. $\overline{M1}$ will then return high and reset U9. QA through QD return to logic zero and $\overline{RDR}$ to logic one.

T3 and T4 mark the end of the special M1 cycle. In succeeding machine cycles, the Z80 stores the program counter on the stack, fetches the vector address from the location pointed to by the accumulator and I register, and then jumps to that address and performs the routine.

Note that during the special M1 cycle, the Z80 places the contents of the program counter on the address bus and asserts the $\overline{IORQ}$ line. However, the internal logic of U6 and U7 will not respond to these signals during the interrupt-acknowledge cycle. Similarly, the static memory circuits will not respond to the refresh address during T3/T4 since the read/write lines won't assert. Also, U9 is active only during an interrupt-acknowledge sequence. During a normal instruction fetch cycle, $\overline{M1}$ isn't low long enough for U9 to shift in the logic one on U9-1.


SYSTEM ROM
DATA BUS
ADDRESS BUS
32K x 8 EPROM
U2
444-580
27256
(0000H-7FFFH)
16K x 8 EPROM
U3
444-581
27128
(8000H-BFFFH)
+5V
VPP
VCC
PGM
GND
CE
OE
A15
MREQ
RD
U17C
1/4 443-875
74LS32
MEMORY READ/WRITE LOGIC
TO OE OF U4 & U5
TO CSI OF U4-20
MREQ
WR
U17D
1/4 443-875
74LS32
TO WE OF U4 & U5
RESET
A13
A14
Q1
230-8101
VN10LM
+5BB
R9
5100
DUAL 2-TO-4 LINE DECODER
+5
U10A
230-8115
74HC139
U10B
230-8115
74HC139
Q2
230-8101
VN10LM
R10
5100
TO CS OF U5
MEMORY DECODER

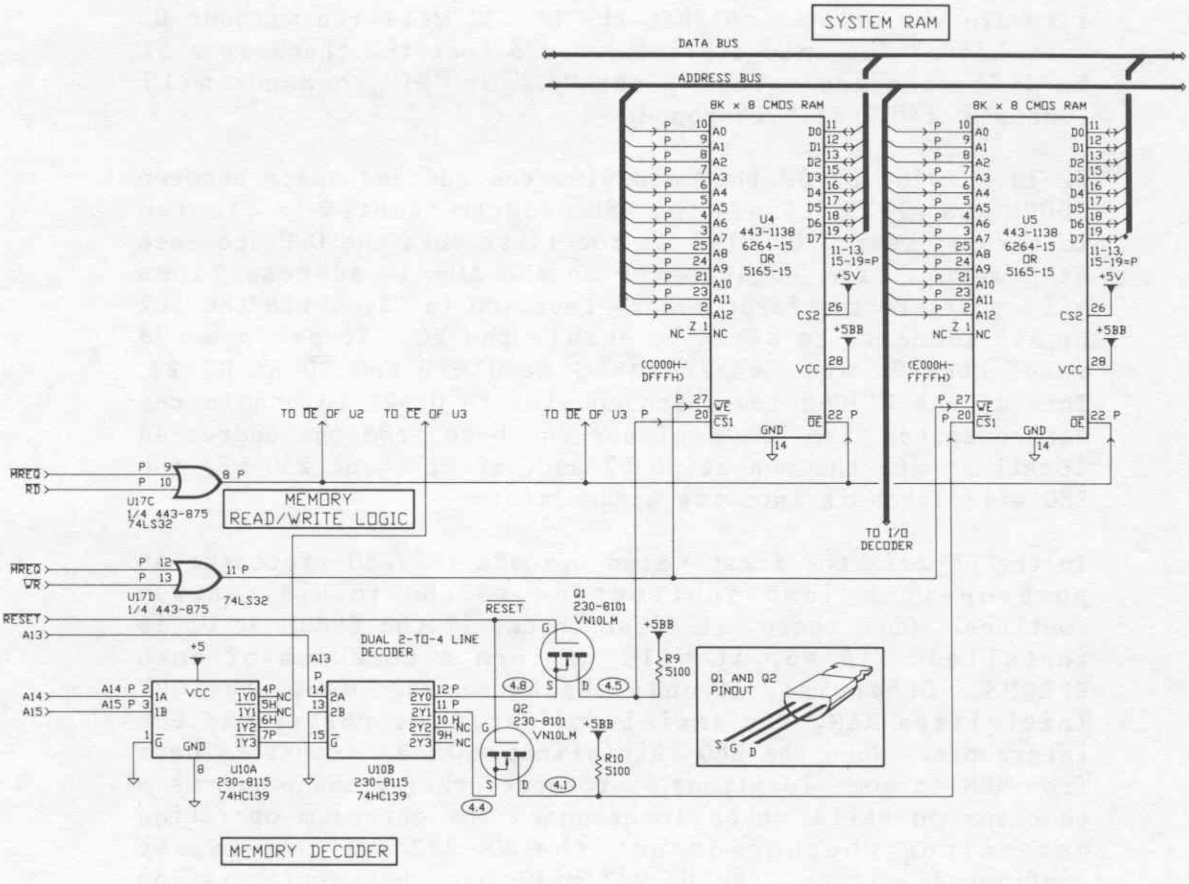
MEMORY

System ROM

The system ROM consists of a 32K x 8 EPROM at U2 and a 16K x 8 EPROM at U3. U2 performs the system initialization, I/O processing, command parsing, and data processing for the packet, Morse, RTTY, and AMTOR modes. U3 processes data for the facsimile and signal analysis modes. Note that the firmware was written so that the HK-232 will run without U3 installed. The only differences are that the checksum will be different and entering the "FA" or "SI" commands will generate a "?What?" response.

U2 is a 27256 EPROM that occupies the address space between 0000H and 7FFFH. Since the Z80 program counter is cleared to zero at reset, U2 will be the first chip the CPU accesses at powerup. The logic zeros on the A0-A14 address lines will point to the first memory location in U2, while the low on A15 connects to U2-20 to enable the IC. To perform the read, the Z80 will assert $\overline{MREQ}$ at U1-19 and $\overline{RD}$ at U1-21. This drives U17C-8 low which couples to U2-22 to enable the data outputs. The EPROM places the byte from the addressed location onto the bus at D0-D7 and, after about 250 nS, the Z80 will latch it into its accumulator.

In the HK-232, the first valid op-code the Z80 processes at powerup is a jump instruction to the initialization routines. Once there, it first checks if the EPROM at U3 is installed. If so, it will perform a checksum of both EPROMS. Otherwise, it only checksums U2. Next, the CPU initializes RAM, the serial and parallel ports, and the interrupts. When the Z80 initializes RAM, it transfers data from ROM to some locations, zeros-out others, and performs a checksum on still other locations. The checksum operation determines whether or not the HK-232 was previously configured. If so, the HK-232 will use that configuration instead of the default values. Finally, the HK-232 displays the sign-on message and enters a loop while waiting for an input from the serial port.



SYSTEM RAM
DATA BUS
ADDRESS BUS
8K x 8 CMOS RAM
U4
443-1138
6264-15
OR
5165-15
(C000H-
DFFFH)
U5
443-1138
6264-15
OR
5165-15
(E000H-
FFFFH)
TO DE OF U2
TO CE OF U3
TO DE OF U3
TO I/O
DECODER
MEMORY
READ/WRITE LOGIC
U17C
1/4 443-875
74LS32
U17D
1/4 443-875
74LS32
MREQ
RD
WR
RESET
A13
A14
A15
DUAL 2-TO-4 LINE
DECODER
U10A
230-8115
74HC139
U10B
230-8115
74HC139
MEMORY DECODER
Q1
230-8101
VN10LM
Q2
230-8101
VN10LM
R9
5100
R10
5100
+5BB
Q1 AND Q2
PINOUT

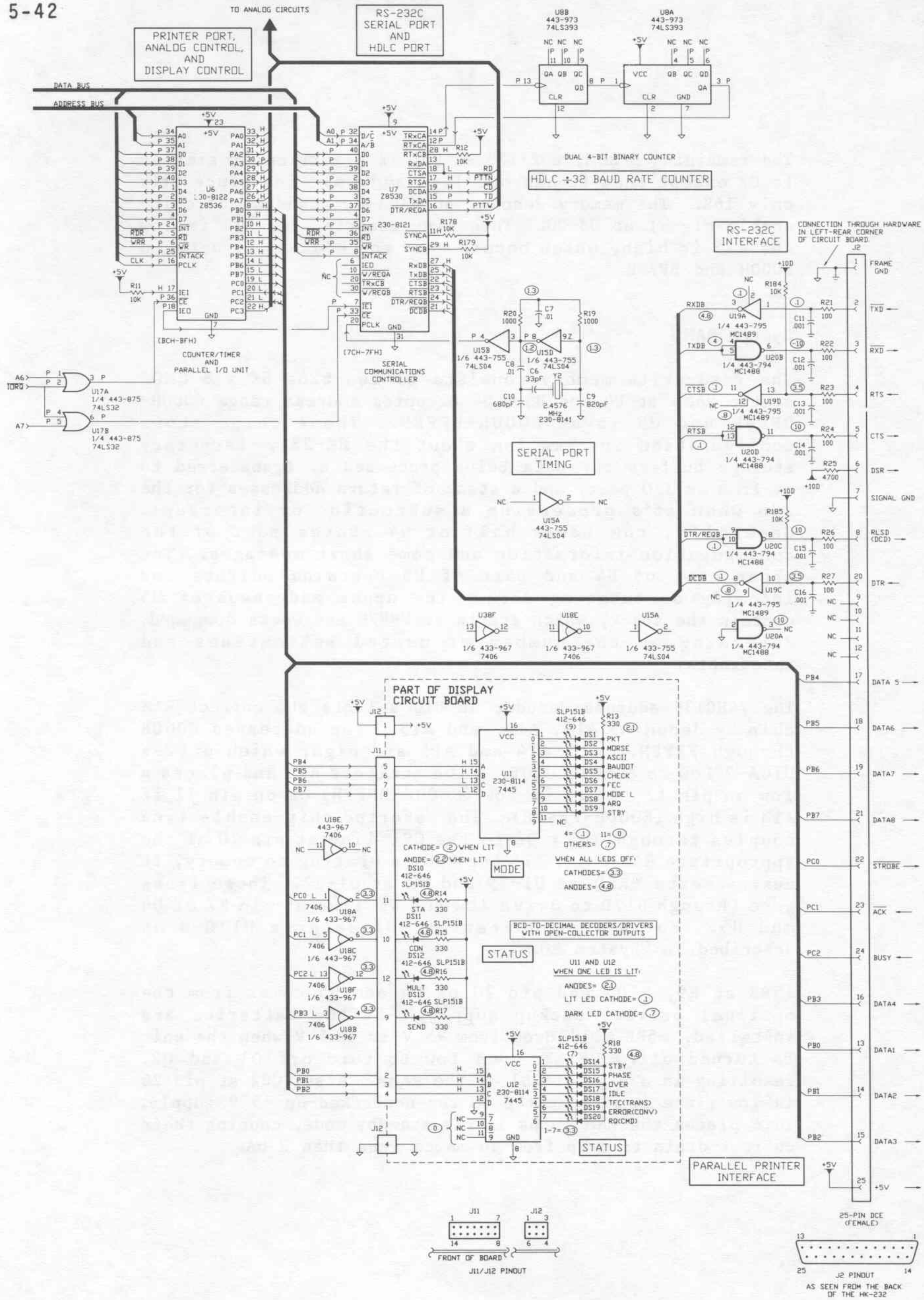
The remaining EPROM, a 27128 at U3, is electrically similar to U2 except that it has one less address line since it's only 16K. The memory decoder at U10A-6 provides the chip-enable signal at U3-20. This line asserts when A14 is low and A15 is high, which occurs when the address is between 8000H and BFFFH.

System RAM

The read-write memory consists of two 6264 8K x 8 CMOS static RAMs at U4 and U5. U4 occupies address range C000H-DFFFH and U5 is at E000H-FFFFH. These chips store configuration information about the HK-232, temporary storage buffers for data being processed or transferred to or from an I/O port, and a stack of return addresses for the Z80 when it's processing a subroutine or interrupt. Generally, the lower half of U4 stores most of the configuration information and some short messages. The upper half of U4 and part of U5 contains buffers for incoming or outgoing data. The upper addresses of U5 contain the stack, which starts at FFFFH and works downward, depending on the number of nested subroutines and interrupts.

The 74HC139 address decoder at U10 selects the correct RAM chip by decoding A13, A14, and A15. For addresses C000H through FFFFH, both A14 and A15 are high, which drives U10A-7 low to enable U10B. U10B monitors A13 and places a low on pin 12 if A13 is low (C000H-DFFFH) or on pin 11 if A13 is high (E000H-FFFFH). The asserted chip-enable line couples through Q1 or Q2 to the $\overline{CS1}$ line at pin 20 of the appropriate RAM chip. If the Z80 is writing to memory, it next asserts $\overline{MREQ}$ at U1-19 and $\overline{WR}$ at U1-22. These lines gate through U17D to drive low the $\overline{WE}$ line at pin 27 of U4 and U5. For a read operation, U1 asserts U17C-8 as described in "System ROM."

+5BB at R9, R10, and pin 20 of U4 and U5 comes from the optional battery backup supply. If the batteries are installed, +5BB will drop from +5 V to +4.5 V when the unit is turned off. $\overline{RESET}$ goes low to turn off Q1 and Q2, resulting in a high at $\overline{CS1}$ of the RAMs. Also, CS2 at pin 26 is low since it's connected to the nonbacked-up +5 V supply. This places the RAM chips in the standby mode, causing their current drain to drop from 40 mA to less than 2 uA.



TO ANALOG CIRCUITS
PRINTER PORT, ANALOG CONTROL, AND DISPLAY CONTROL
RS-232C SERIAL PORT AND HDLC PORT
DATA BUS
ADDRESS BUS
U6 230-8122 Z8536
COUNTER/TIMER AND PARALLEL I/O UNIT
U7 Z8530 230-8121
SERIAL COMMUNICATIONS CONTROLLER
U8B 443-973 74LS393
U8A 443-973 74LS393
DUAL 4-BIT BINARY COUNTER
HDLC ÷32 BAUD RATE COUNTER
RS-232C INTERFACE
CONNECTION THROUGH HARDWARE IN LEFT-REAR CORNER OF CIRCUIT BOARD.
U17A 1/4 443-875 74LS32
U17B 1/4 443-875 74LS32
SERIAL PORT TIMING
Y2 2.4576 MHz 230-8141
U15B 1/6 443-755 74LS04
U15D 1/6 443-755 74LS04
U15A 443-755 74LS04
U19A 1/4 443-795 MC1489
U20B 1/4 443-794 MC1488
U19D 1/4 443-795 MC1489
U20D 1/4 443-794 MC1488
U20C 1/4 443-794 MC1488
U19C 1/4 443-795 MC1489
U20A 1/4 443-794 MC1488
U38F 1/6 433-967 7406
U18E 1/6 433-967 7406
PART OF DISPLAY CIRCUIT BOARD
U11 230-8114 7445
U12 230-8114 7445
PKT
MORSE
ASCII
BAUDOT
CHECK
FEC
MODE L
ARQ
STBY
MODE
STATUS
STA
CON
MULT
SEND
PHASE
OVER
IDLE
TFC(TRANS)
ERROR(CONV)
RQ(CMD)
BCD-TO-DECIMAL DECODERS/DRIVERS WITH OPEN-COLLECTOR OUTPUTS
WHEN ALL LEDS OFF:
U11 AND U12 WHEN ONE LED IS LIT:
LIT LED CATHODE=
DARK LED CATHODE=
PARALLEL PRINTER INTERFACE
J2
FRAME GND
TXD
RXD
RTS
CTS
DSR
SIGNAL GND
RLSD (DCD)
DTR
DATA 5
DATA6
DATA7
DATA8
STROBE
ACK
BUSY
DATA4
DATA1
DATA2
DATA3
+5V
25-PIN DCE (FEMALE)
J2 PINOUT AS SEEN FROM THE BACK OF THE HK-232
FRONT OF BOARD
J11/J12 PINOUT

PARALLEL PORTS AND TIMERS

General

The parallel ports and timers are located in a Z8536 IC at U6. This IC contains two independent 8-bit I/O ports, a 4-bit I/O port, and three 16-bit counter/timers. The I/O ports can be programmed as inputs or outputs on a line-by-line basis. If used as inputs, the lines can be programmed to monitor logic states or operate as latches to catch pulses. As outputs, the lines can be programmed to generate active highs and lows, or operate as open-collector devices. Each timer has four access modes: write to timer, read timer, gate timer on or off, and trigger the timer on. There are three output duty cycles: pulsed, one-shot, and square-wave. In addition, the output of one timer can drive the input of another, thus providing longer counts.

The Z80 communicates with U6 through D0-D7. U17A ORs A6 and the $\overline{\text{IORQ}}$ line from U1-20 to chip-enable the parallel port at U6-36. The Z80 will assert either $\overline{\text{WRR}}$ at U6-6 for a write operation or $\overline{\text{RDR}}$ at U6-5 for a read. Address lines A0 and A1 select the specific port inside the chip. The HK-232's firmware forces all other address bits high, yielding these addresses:

Address	Description
0BCH	Parallel port A data
0BDH	Parallel port B data
0BEH	Parallel port C data
0BFH	Control port

The Z80 writes to the control port to set up the timers, configure the parallel ports, and program the interrupt circuits. It can read the control port to determine handshake status, timer status, and which port generated an interrupt.

Parallel Port Interrupt Operation

The following table shows the interrupts available in order from highest priority to lowest.

1. Timer 3
2. Radio Interface (PA0-PA7)
3. Timer 2
4. Printer Data & Mode/Status LEDs (PB0-PB7)
5. Timer 1

During powerup, the HK-232 programs only timer 1 to generate interrupts. This occurs at 1 mS intervals and is based on the 4.0 MHz clock entering U6-16. To begin the interrupt, U6 places a logic zero on the interrupt request line, pin 24. When the Z80 is ready to process the interrupt, it asserts the interrupt-acknowledge line at U6-25. U6 will then place the interrupt vector on D0-D7, which the Z80 uses to determine the location of the interrupt program.

U6-17 is a hardware interrupt-enable input. If this line is low, the IC can't generate an interrupt request. R11 permanently ties this line high. U6-18 is the interrupt-enable output and connects to U7-7, the serial port interrupt enable input. If U6 is performing an interrupt request and acknowledge cycle, pin 18 goes low and disables the interrupt circuits in U7. This gives the timer highest priority, which is necessary for the Z80 to maintain its various timekeeping functions--such as time-of-day and determining Morse code speed.

Radio Interface (PA0-PA7)

Parallel port A controls and monitors most of the functions that interface the HK-232 to a radio. These are shown in the following table.

Bit	Pin	Function	Active Level	Direction
PA7	26	Squelch		In
PA6	27	RTTY transmit data		Out
PA5	28	Wide shift enable (VHF)	High	Out
PA4	29	Tone enable	High	Out
PA3	30	Calibration		In
PA2	31	FSK enable (CW/NCW)	High	Out
PA1	32	CW keyer	Low	Out
PA0	33	Narrow shift enable (HF)	Low	Out

PA7 may be programmed with the SQ ON/OFF command to be either active-high or active-low . PA6 doesn't have a defined active state, but rather pulses when the HK-232 transmits data in any of the non-packet modes. PA3 counts the transitions on the digital output of U40, the XR2206 tone generator.

PA2 switches the HK-232 between the CW and FSK modes. When high, it enables FSK for Packet and RTTY; when low, PA2 enables CW. PA5, PA2 and PA0 work together to determine the amount of frequency shift.

PA5	PA2	PA0	Function
0	1	0	Narrow shift FSK
1	1	1	Wide shift FSK
0	0	1	CW

On the Analog Circuits schematic, U39C and U37D double-invert PA5 to generate the VHF control line. The open-collector inverter at U37D and the pullup resistor at R182 convert the signal from TTL to the +13 V signal required by the 4066B FET switches. U37A inverts PA2 to form the CW line, while U39A and U37F form the NCW line. U37C converts PA0 to the HF control line.

Mode and Status Display Control (PB0-PB7, PC0-PC3)

Parallel ports B and C work together for printer I/O and controlling the mode and status LEDs. Most of the time, these lines drive the front panel LEDs through decoder chips. If PRCON is ON, they interface with the parallel printer.

Parallel port B pins PB4, PB5, PB6 and PB7 drive the Mode LEDs through the 7445 decade decoder at U11. Refer to the following table.

PB7	PB6	PB5	PB4	LED	
0	0	0	0	PKT	
0	0	0	1	MORSE	
0	0	1	0	ASCII	
0	0	1	1	BAUDOT	
0	1	0	0	CHECK	
0	1	0	1	FEC	
0	1	1	0	MODE L	
0	1	1	1	ARQ	
1	0	0	0	STBY	
1	0	0	1	(FAX)	} Not used on the
1	0	1	0	(SIGNAL or SIAM)	} front panel

PB3 also drives the SEND LED through U18B, while U12 decodes PB0-PB2 to drive the status LEDs shown in the following table.

PB2	PB1	PB0	LED	
0	0	0	STBY	
0	0	1	PHASE	
0	1	0	OVER	
0	1	1	IDLE	
1	0	0	TFC	TRANS
1	0	1	ERROR	CONV
1	1	0	RQ	CMD

Parallel port C drives the remaining status LEDs through the 7406 inverter at U18.

Bit	IC	Description
PC0	U18A	STA LED
PC1	U18C	CON LED
PC2	U18F	MULT LED

In addition, PC3 connects through U18D on the Analog Circuits schematic to enable the bar graph display.

Printer I/O (PB0-PB7, PC0-PC3)

Ports B and C also provide an interface to printers with Centronics-type parallel connectors. This includes eight data lines and three handshake lines. Refer to the following table. Note that in the first production run, only Epson-compatible printers were supported. Several other printers were added in later runs.

Bit	U6 pin	J2 pin	Function	Active State	Direction
PB7	15	21	DATA 8	High	Out
PB6	14	19	DATA 7	High	Out
PB5	13	18	DATA 6	High	Out
PB4	12	17	DATA 5	High	Out
PB3	11	16	DATA 4	High	Out
PB2	10	15	DATA 3	High	Out
PB1	9	14	DATA 2	High	Out
PB0	8	13	DATA 1	High	Out
PC2	21	24	BUSY	High	In
PC1	20	23	$\overline{\text{ACK}}$	Low	In
PC0	19	22	$\overline{\text{STROBE}}$	Low	Out

The three handshake lines function as follows.

$\overline{\text{STROBE}}$: After the CPU latches data on PB0-PB7, it asserts the strobe line to tell the printer that a new byte is present at the printer input.

$\overline{\text{ACK}}$: The printer asserts this line to acknowledge that it processed the byte on PB0-PB7 and is ready to receive another character.

BUSY: This line asserts if the printer is busy and cannot accept a data byte at the time STROBE occurs. This can happen if the print head is moving (as during a carriage return) or if the printer is in the off-line mode. The CPU stops sending characters until the BUSY line goes to its inactive state.

To reduce ringing, the BUSY and ACK signals should each contain a 200-ohm series resistor in the cable to the parallel printer.

RS-232C AND HDLC SERIAL PORTS

General

The serial ports are located in a Z8530 IC at U7. This IC contains two independent asynchronous serial ports that can be programmed to operate as a standard RS-232C serial port or as a High-Level Data Link controller (HDLC). As a serial port, it features software control of the baud rate, number of stop bits, parity control, and full hand shaking. In the HDLC mode, it has comprehensive frame-level control, automatic zero insertion and deletion, I-field residue handling, abort processing, and CRC processing.

The Z80 communicates with U7 through D0-D7. U17B ORs A7 and the IORQ line to chip-enable the serial ports at U7-33. The Z80 will assert either WRR at U7-35 for a write operation or RDR at U7-36 for a read. Address line A0 selects the data or control register, while A1 selects port A or port B. Except for A0, A1, and A7, the HK-232's firmware forces all other address bits high, yielding these addresses:

Address	Description
07CH	Port B Control (RS-232C)
07DH	Port B Data (RS-232C)
07EH	Port A Control (HDLC)
07FH	Port A Data (HDLC)

The Z80 writes to the control register of each port to set up the type of operation, and the default data rates, and to program the interrupt circuits. It can read the control port to determine handshake status, configuration status, error status, and which port generated an interrupt.

Serial Port Interrupt Operation

The HK-232 uses interrupts in the two serial ports to permit it to perform other functions instead of continuously polling the ports for incoming data. U7-5 and U7-8 perform the interrupt request/acknowledge cycle in the same manner as the $\overline{\text{INT}}/\overline{\text{INTACK}}$ lines on U6. Once the CPU responds to the interrupt, it will process the one with the higher priority (if more than one occurs). The following table shows the interrupts available in order from highest priority to lowest.

1. HDLC Receive Data
2. HDLC Transmit Data
3. HDLC Handshake/Status registers
4. RS-232C Receive Data
5. RS-232C Transmit Data
6. RS-232C Handshake/Status registers

During powerup, the Z80 disables the HDLC interrupts until the HDLC enters the packet mode. In the packet mode, the CPU enables all three HDLC interrupts. The transmit data interrupt will let the Z80 know that the HDLC's transmit buffer is ready to accept more data, while the receive interrupt signals that it's got incoming data in its buffer for the CPU. The handshake/status interrupt occurs if one of the handshake lines pulses (such as $\overline{\text{CTSA}}$), or an error occurs when sending or receiving data. The three RS-232C interrupts are also initialized and function in the same manner as the HDLC interrupts.

The interrupt priorities were chosen by the amount of data each port was expected to handle. For most operations, the RS-232C receive data will be typed in by a human, which allows the Z80 plenty of time to process it. The HDLC port, however, must transfer high-speed bursts of information, thus requiring the CPU to process it immediately in order to prevent data loss. Note that this applies mostly to the modes that don't perform error detection, such as Baudot or Morse. If the HK-232 detects an error in AMTOR or packet, it merely requests that the data be sent again.

The only higher interrupt is the timer 1 interrupt from the parallel port at U6. While U6 is performing an interrupt operation, it places a logic zero on U7-7, the interrupt enable input. As long as this line is low, U7 can't generate an interrupt request. (See "Parallel Port Interrupt Operation.") Since there are no other circuits in the HK-232 that generate interrupts, the interrupt-enable output at U7-6 isn't connected.

Serial Port Timing

The serial port clock is a 2.4576 MHz crystal oscillator at U15D and Y2. Its design is similar to the 4 MHz clock at U15E and Y1. (See "System Clock.") That is, C7, R19, and R20 bias and decouple the IC. C6, C9, and C10 trim the frequency, while C8 starts oscillation at powerup. U15B provides load isolation and couples the clock to U7-20, PCLK.

The 2.4576 MHz frequency is an even multiple of the standard baud rates used in serial communication, thus making it easy for U7 to generate the proper timing. Inside U7, PCLK provides the basic timing for both the HDLC port and the RS-232C port. However, the HDLC uses synchronous timing while the RS-232C port uses asynchronous.

In the HDLC section, PCLK connects to a baud rate generator that divides the frequency down to 32 times the desired serial baud rate. That is, it will generate a 38.4 kHz square wave for a 1200-baud packet signal. Internally, the HDLC couples this signal to a digital phase-locked loop that compares it to the received serial data at U7-13. By monitoring the time difference between the X32 clock and the rising and falling edges of the incoming NRZI data, the DPLL can generate a clock signal that is synchronous to the incoming data. Other circuits in U7 use this clock to extract the received data for further processing before it's sent to the Z80. In addition, U7 uses this clock to generate a 1 mS negative-going pulse at the $\overline{\text{SYNCA}}$ output, U7-11. The pulse repetition rate is 1/8 the baud rate and occurs only when receiving data. Though it's not used in the HK-232, it permits you to quickly verify the HDLC when troubleshooting.

The baud rate generator also sends the X32 square wave to the $\overline{\text{TRxCA}}$ line at pin 14. This is a bidirectional line that the CPU programmed as an output at powerup. U8B and U8A form a divide-by-32 counter to reduce the square-wave frequency to the data baud rate. U8A-3 couples the resulting X1 clock to $\overline{\text{RTxCA}}$ (U7-12), which is always an input. Inside U7, this is used as the HDLC transmit clock.

In the RS-232C section, PCLK connects to another baud rate generator that the Z80 programmed to operate at 16 times the data baud rate. The generator output connects directly to the internal receive and transmit clocks. Since the NRZ serial data is asynchronous, it contains start and stop bits that allow the receiver to extract the data bits. So the DPLL isn't needed. The baud rate generator also connects to the TRxCB output at U7-26. Though not connected, it provides an indication of proper operation. At powerup, if there's no battery-backed data in RAM, U7-26 will generate a 19.2 kHz square wave as the HK-232 sends the "Please type a star..." message to the computer at 1200 baud. U7-26 then shifts to 153.6 kHz (9600 baud) while it waits for an input from the keyboard. When U7 starts receiving data from the computer, it lowers the baud rate generator frequency until the incoming data matches the ASCII code for an asterisk (02AH).

RTxCB, U7-28, is a clock input, but isn't used, so it's tied high. W/REQA at U7-10 and W/REQB at pin 30 are wait/request lines used in some designs to synchronize the CPU to the serial ports. They're not required in the HK-232, so they're not connected.

HDLC Data and Control

There are two modem receive data paths: RxDA at U7-13 and CTSA at U7-18. When the HK-232 is in the packet mode, it uses the RxDA path. This permits the HDLC to check the packet for errors and, if okay, extract the data from the packet and send it to the Z80 through D0-D7. If the packet is not okay, U7 signals the distant station to resend it using the AX.25 protocol. The CTSA input handles the AMTOR, Baudot, ASCII, FAX, and Morse modes. The Z80 monitors this handshake line by reading the CTS bit (D5) of the transmit/receive/external status register in U7. The CPU then assembles the required number of bits appropriate for the operating mode to form readable data.

To transmit packets, the Z80 couples the binary data through D0-D7 to U7, which adds the AX.25 flags, addresses, control codes, and checksum information. U7 then converts this data to serial and transmits it through the TxDA output at pin 15 to the AFSK modulator. To transmit data in nonpacket modes, the CPU transmits it through U6-27 as described in "Radio Interface (PA0-PA7)."

The RTSA output at U7-17 is the push-to-talk signal, PTTN. For PTTN to be effective, the Z80 toggles the DTR/REQA output at U7-16 once every 4 to 6 mS. This signal, PTTW, keeps the watchdog timer from disabling the transmitter (see "Squelch, Push-to-Talk, and Watchdog Timer"). Note that if the HK-232 doesn't have battery backup, or isn't configured, PTTN won't start pulsing until after the asterisks have been entered at powerup. The DCDA input at U7-19 is the carrier-detect signal from the threshold detector. This line goes low when the HK-232 receives an audio signal from the external receiver (see "Threshold Detector").

RS-232C Data and Control

The RS-232C circuits consist of U7, U19, U20, and J2. U20, a standard 1488 EIA line driver, converts the TTL inputs to the ±10 V levels required by the RS-232C standard. The output impedance is 300 ohms and the signal is current-limited to ±10 mA. U19 is a standard 1489 EIA line receiver that converts the RS-232C signals to TTL levels. It has built-in hysteresis to improve noise rejection and has a 3- to 7-kilohm input resistance. J2 is a DCE DB-25 female connector. Only pins 1-8 and 20 are standard, however. The rest are used by the parallel port. R21-R27 protect the circuits from excessive voltages. C11-C16 limit the signal slew rate to 30 volts per microsecond as specified by the RS-232C standard. Note that these capacitors connect to chassis ground. The current path is through the left rear spacer holding the circuit board to the chassis. If this spacer or its associated hardware is missing, the capacitors will float. Also, the circuit board ground connects to the chassis through the right rear spacer. This hardware must be installed to a good ground.

If the HK-232 isn't initialized, or doesn't have battery backup, the Z80 will program the RS-232C section of U7 for 1200 baud, 8 data bits, no parity, and one stop bit. Note that the serial port used two stop bits in the first production run. Also, two stop bits are used at 110 baud and below.

U7-25, TxDB, sends serial data through U20B and J2-3 to the external terminal or computer. Data from the terminal couples through J2-2 and U19A to U7-27. The two handshake inputs, $\overline{\text{CTSB}}$ at U7-22 and $\overline{\text{DCDB}}$ at pin 21, must be low before U7-25 will transmit a signal. U19D and U19C interface these signals to the external terminal. If the terminal doesn't use these lines, R184 and R185 will pull up the input voltage to enable the transmitter. Note that the voltage at the input of the inverters will be fairly low. This is due to their low input resistance (3- to 7-kilohms).

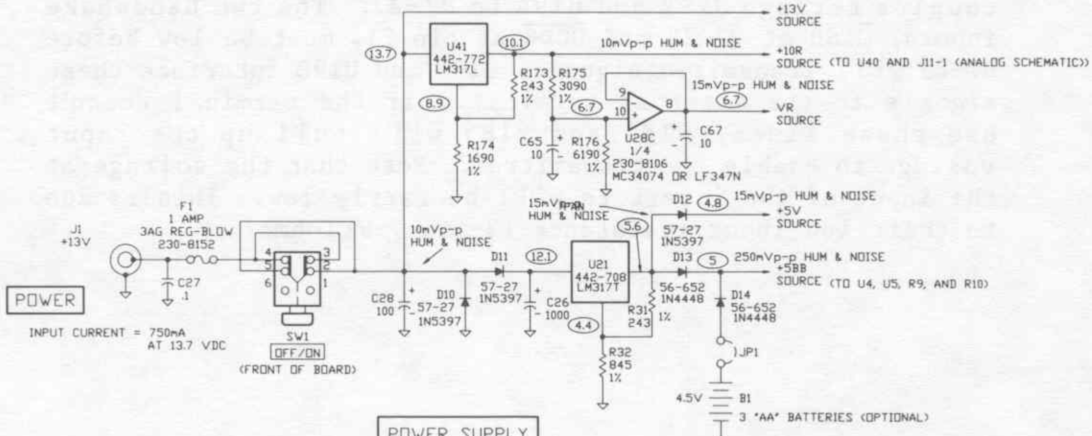
When the HK-232 isn't sending data to the console, it holds $\overline{\text{RXD}}$ at J2-3 at -10 V. This corresponds to a logic one, or mark. A space is +10 V. As specified by the EIA, the mnemonics of the signals at J2 are referenced to the remote DTE connector, which is why they appear incorrect when compared to those on serial port A.

One output handshake line, $\overline{\text{RTSB}}$ at U7-23, couples through U20D and J2-5 to the CTS input of the external terminal.

The $\overline{\text{DTR/REQB}}$ line, U7-24, is always low if the HK-232 is in the DCDCONN OFF mode (default). When DCDCONN is ON, U7-24 responds to the state of the front panel CON LED when in the packet or AMTOR mode. When communicating with a distant station, the CON LED is lit and pin 24 is low. After disconnecting, the LED turns off and pin 24 goes high. U20C inverts this handshake signal and sends it as RLSD to the terminal. It's used by some packet communications programs to monitor connect status.

J2-6, DSR, is permanently pulled high by R25. J2-1 is frame ground and J2-7 is signal ground. All other J2 pins are reserved for use with a parallel printer.

The $\overline{\text{SYNCB}}$ input, U7-29, is pulled high by R179. Grounding this line forces the HK-232 into the echo-as-sent mode. That is, when the Z80 transmits data to the HDLC, it will also send it to the RS-232C port. It has the same effect as entering the EAS ON command.



POWER SUPPLY

Power Supply

The HK-232 draws about 700 mA from an external DC supply that can range from +12 VDC to +16 VDC. Ripple can be as much as 1 V P-P. This wide range permits powering the unit from the optional #150-333 power cube, a car battery, or other supply operating at a nominal +13 volts.

Refer to the "Power Supply" schematic at the left as you read the following.

DC power from the external source couples through J1, F1, and SW1 to the +13V supply and the regulators. C27 and C28 filter noise and ripple. D10 provides reverse-voltage protection.

The +13V line supplies power directly to the op amps, electronic switches, and tuning indicator on the "Analog Circuits" schematic. This line doesn't need to be regulated due to the high common mode rejection ratio and power supply rejection ratio of the op amps.

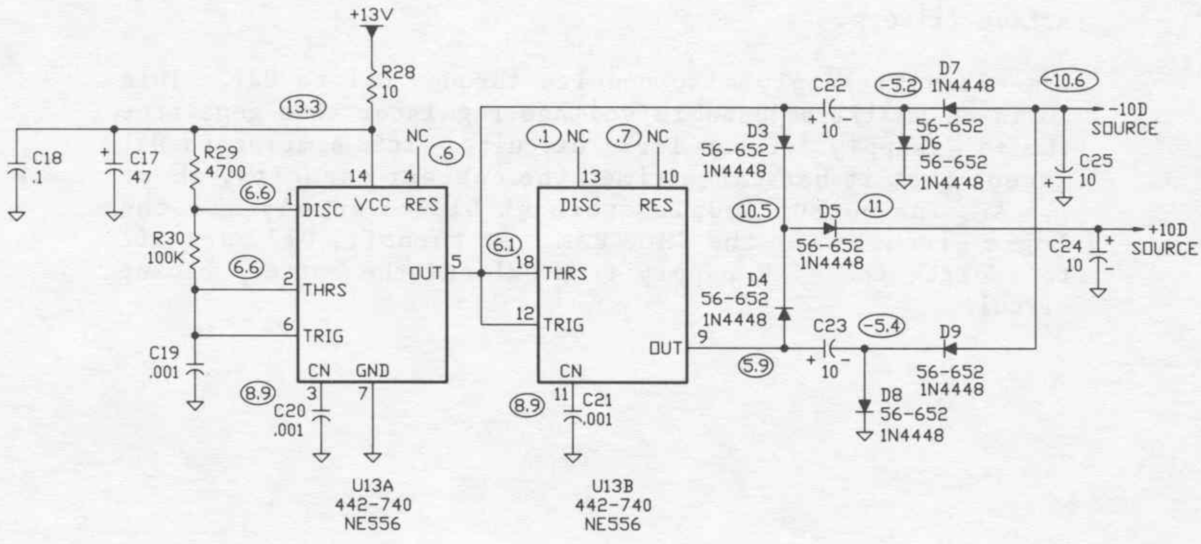
U41 is an LM317L adjustable voltage regulator that generates the +10R supply. R173 and R174 set the output voltage to +10 V. This circuit provides power to the AFSK modulator and acts as a reference voltage for the tuning indicator, both on the Analog Circuits schematic. +10R also couples through R175 to U28C-10, a unity gain follower. This circuit provides the +6.7 V reference voltage, VR, for the active filters.

The +13-volt supply also couples through D11 to U21. This IC is an LM317T adjustable voltage regulator that generates the +5 V supply for the logic circuits. It's similar to U41 except that it has three times the current capacity, about 1.5 A. The output couples through D12 to supply all the logic circuits but the CMOS RAM. At turnoff, D12 cuts off to isolate the +5 V supply from U21 and the battery backup circuit.

B1 and JP1 are the optional battery backup supply for the system RAM. B1 consists of three series-connected AA cells that generate the +4.5 V supply, +5BB. When the HK-232 is turned on, U21 supplies +5BB through D13. When the unit is turned off, B1 supplies power through D14. D13 will be reverse biased to prevent B1 from discharging into U21 and the +5 V supply. Depending on the manufacturer of the CMOS RAMs, B1 will supply from 2 to 20 uA when in the standby mode.

RS-232C Power Supply

As shown in the "RS-232C Power Supply" schematic below, the RS-232C power supply consists of U13A, U13B, D5-D9, and their associated resistors and capacitors. U13A is one half of an NE556 timer wired as an astable multivibrator. C19, R29, and R30 set the frequency to about 7 kHz; R29 and R30 set the duty cycle to about 50%. C20 filters noise from U13A-3, the other input to the threshold and trigger comparators. C17, C18, and R28 decouple any oscillator noise that may be present at pin 14.



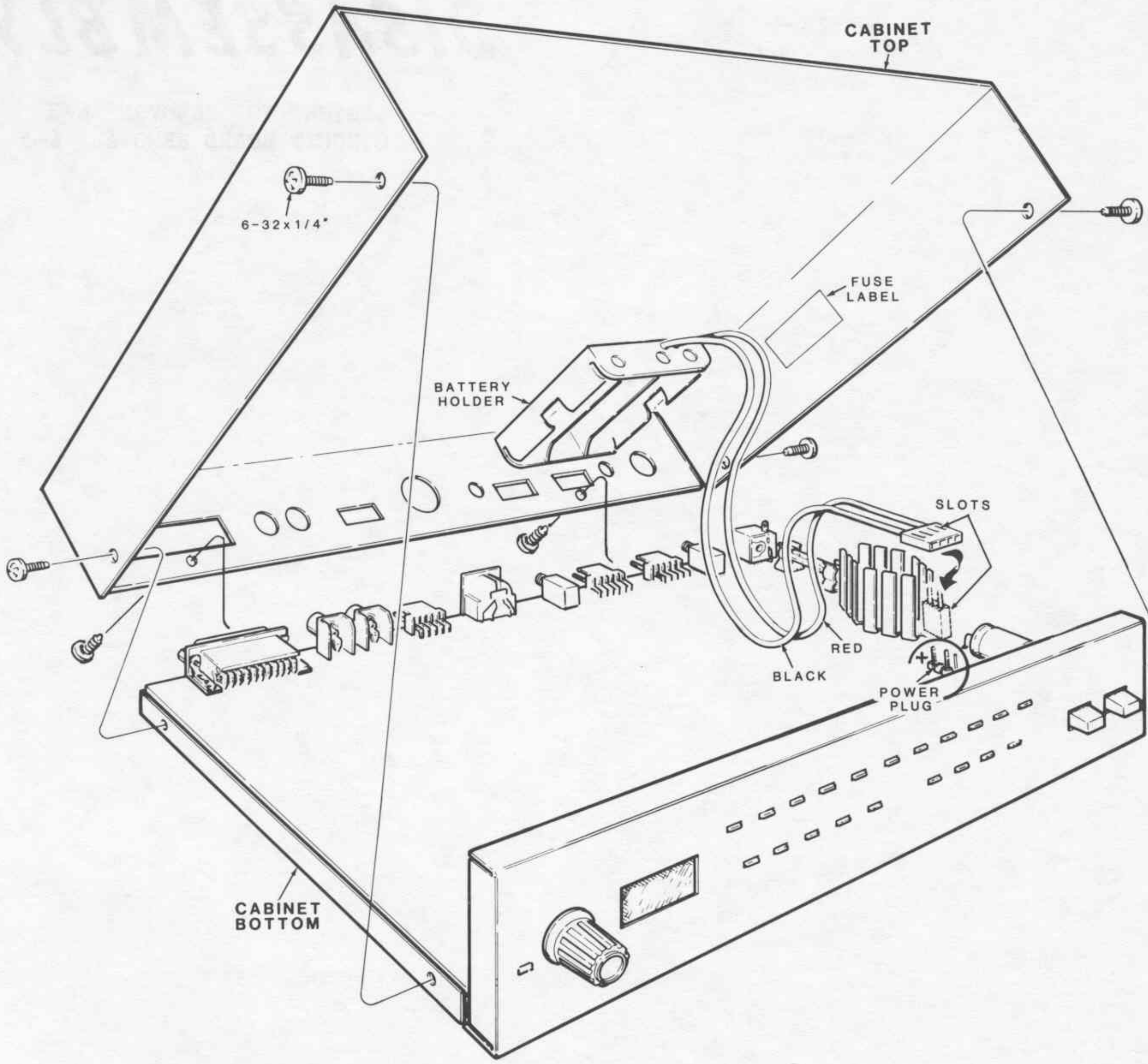
RS-232C POWER SUPPLY

At powerup, the voltage across C19 is low, so U13A-6 triggers U13A-5 high. At the same time, DISC at pin 1 goes high and C19 begins to charge through R29 and R30. When the voltage gets to about +9 VDC, it will exceed the internal reference of the threshold comparator and cause pins 1 and 5 to go low. Pin 1 will discharge C19 and the cycle will repeat. The result is a square wave at pin 5 ranging from zero to positive twelve volts.

U13A-5 connects to pins 8 and 12 of U13B, which is wired as an inverter. When the output of 10A swings below or above U13B's threshold voltage (present at U13B-11), the output at U13B-9 switches in the opposite direction (+12 V to 0 V).

These opposite-phase square waves alternately turn on D3 and D4 to supply a continuous current through D5. C24 filters voltages spikes caused by the switching action. The square waves also couple through C22 and C23 to D6-D9, a full-wave bridge rectifier. Effectively, the signal across the negative sides of the two capacitors is a 20 VAC peak-to-peak square wave, resulting in a -10 VDC at the anodes of D7 and D9. C25 filters any switching noise present.

DISASSEMBLY


CABINET TOP
6-32 x 1/4"
FUSE LABEL
BATTERY HOLDER
SLOTS
RED
BLACK
POWER PLUG
CABINET BOTTOM

CABINET TOP REMOVAL

-- Unplug all connectors from the rear of the HK-232.

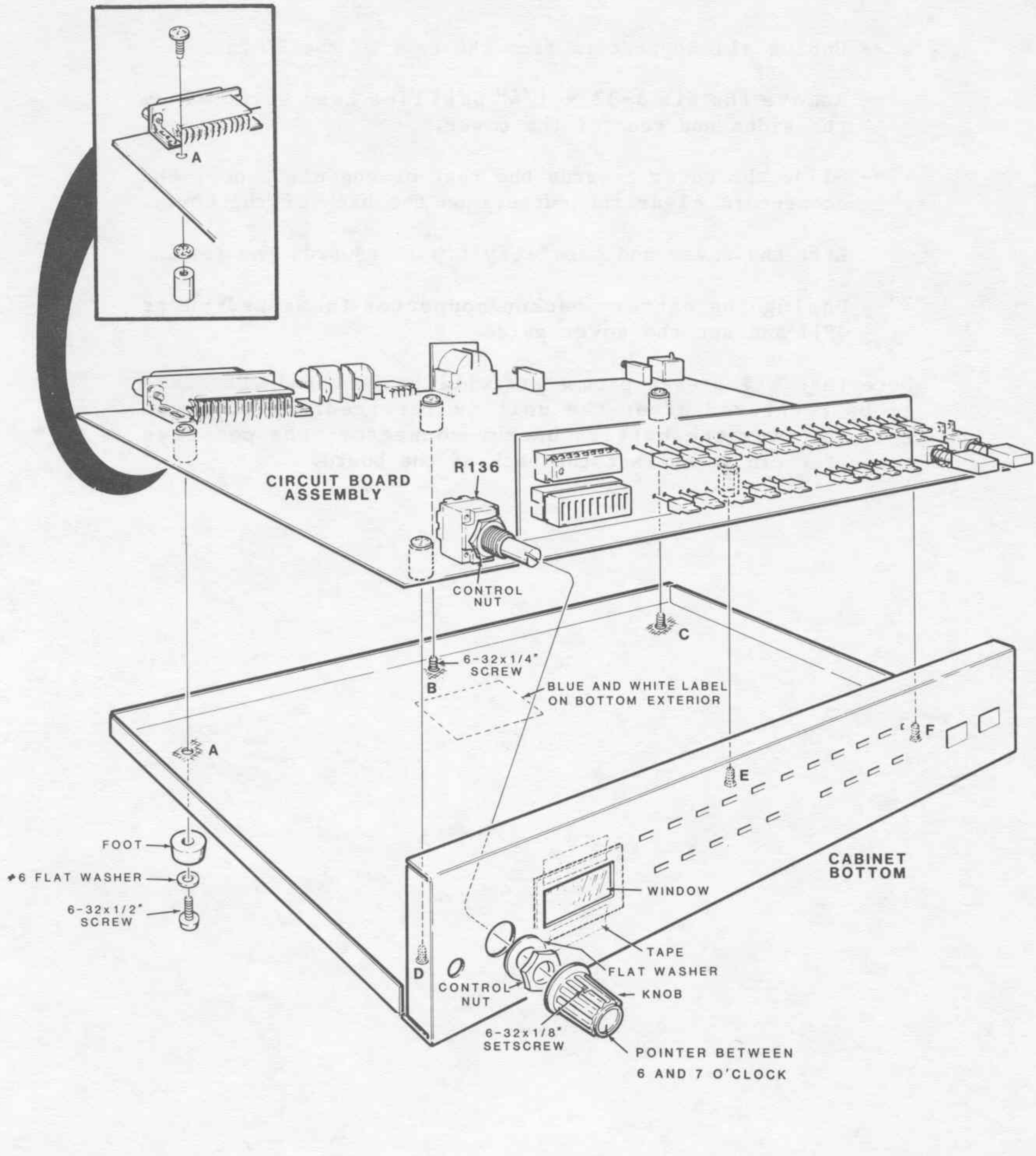
-- Remove the six 6-32 x 1/4" phillips head screws from the sides and rear of the cover.

-- Slide the cover towards the rear of the unit until the connectors clear the cutouts on the back of the cover.

-- Lift the cover and carefully tip it towards the rear.

-- Unplug the battery backup connector (unmarked--near JP1) and set the cover aside.

Note that all preset parameters will be lost and will have to be reentered after the unit is repaired. Also, when reinstalling the battery backup connector, the positive connector pin is nearest the back of the board.


A
CIRCUIT BOARD ASSEMBLY
R136
CONTROL NUT
C
6-32x1/4" SCREW
B
BLUE AND WHITE LABEL ON BOTTOM EXTERIOR
A
F
E
FOOT
#6 FLAT WASHER
6-32x1/2" SCREW
CABINET BOTTOM
WINDOW
TAPE
D
FLAT WASHER
CONTROL NUT
KNOB
6-32x1/8" SETSCREW
POINTER BETWEEN 6 AND 7 O'CLOCK

CIRCUIT BOARD REMOVAL

-- With a 0.062 allen wrench (#490-14), loosen the 6-32 x 1/8" setscrew in the Threshold control and remove the knob.

-- Remove the control nut and control washer.

NOTE: As shown in the inset, there are #6 lockwashers between the circuit board and the spacers. For quicker reassembly, the following steps will instruct you to remove the hardware from the bottom of the chassis.

-- Turn the unit over and remove the two 6-32 x 1/4" phillips head screws at locations B and E.

-- Remove the four 6-32 x 1/4" screws from the rubber feet at each corner.

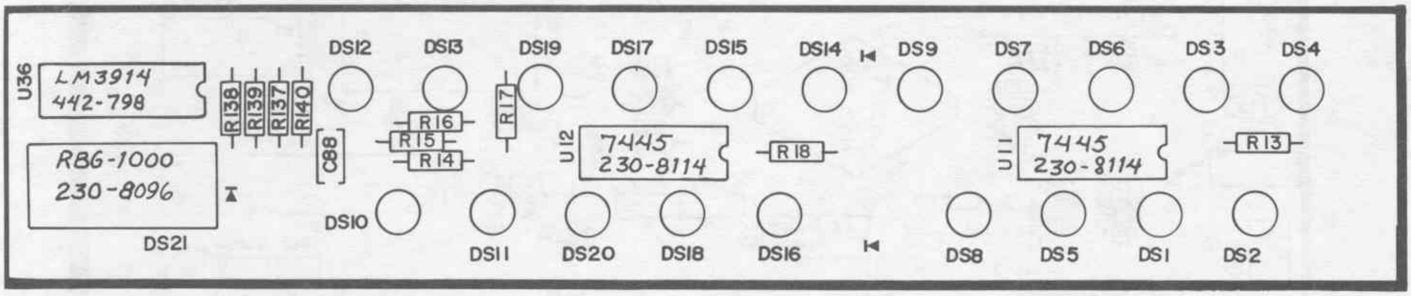
-- Position the unit circuit-board side up with the front panel facing you.

-- Slide the circuit board towards the rear of the chassis until the control shaft clears the front panel hole and lift the circuit board clear of the chassis.

Disassembly complete. To reassemble, perform the previous steps in the opposite order. Before installing the circuit board, make sure that the front panel indicator lights are properly aligned and not bent. When reinstalling the Threshold control knob, adjust the control FCCW and position the pointer on the knob between 6 and 7 o'clock.

VISUAL CHECKS

DISPLAY CIRCUIT BOARD
Component Locations and Values



CAPACITOR

C88	.0056 uF (562K) Mylar®	27-147

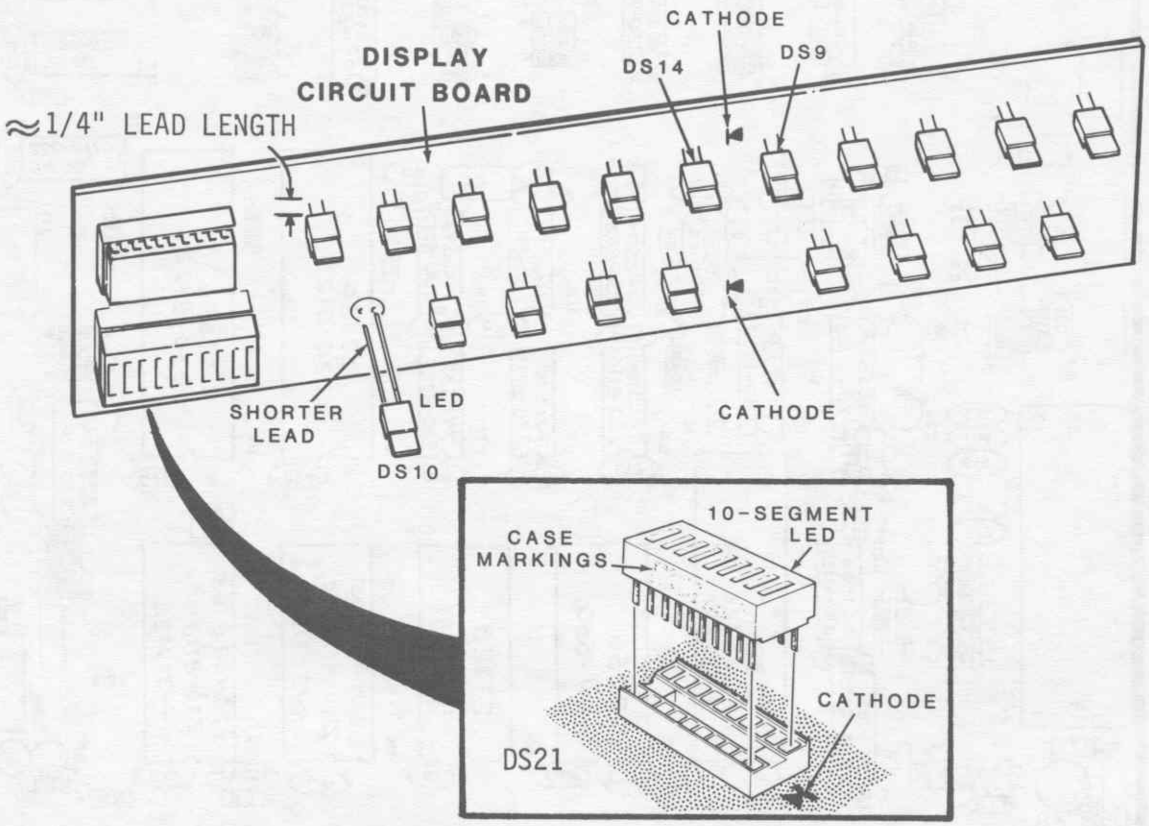
LEDS

DS1-DS20	SLP151B, red	412-646
DS21	RBG-1000, 10-segment bar graph	230-8096

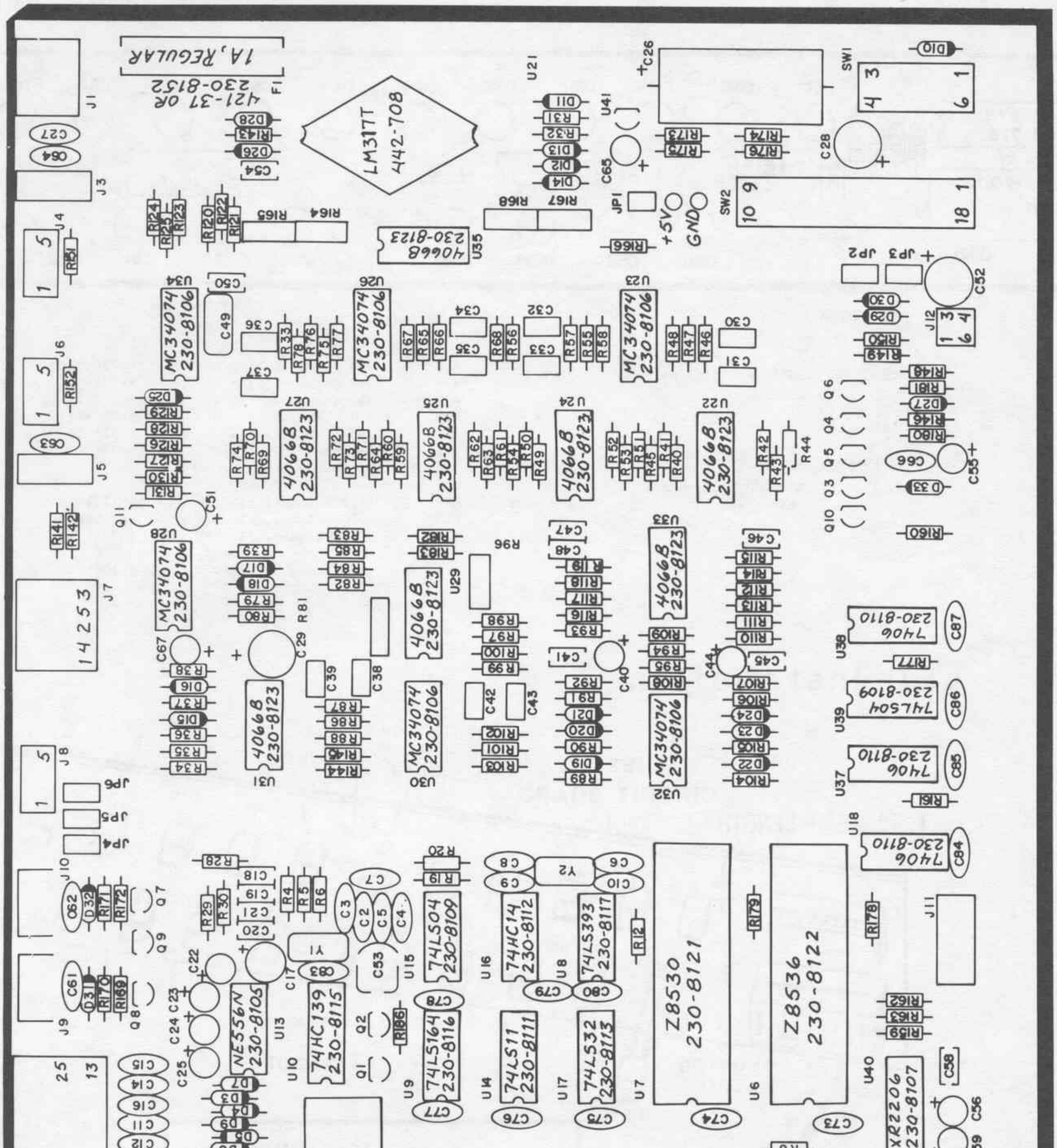
RESISTORS

R13	330 ohms, 5%, 1/4 W	6-331-12
R14	330 ohms, 5%, 1/4 W	6-331-12
R15	330 ohms, 5%, 1/4 W	6-331-12
R16	330 ohms, 5%, 1/4 W	6-331-12
R17	330 ohms, 5%, 1/4 W	6-331-12
R18	330 ohms, 5%, 1/4 W	6-331-12
R19-R136	On main board.	
R137	1.78 kilohms, 1%, 1/4 W	6-1781-12
R138	1.10 kilohms, 1%, 1/4 W	6-1101-12
R139	3.74 kilohms, 1%, 1/4 W	6-3741-12
R140	1.0 kilohm, 5%, 1/4 W	6-102-12

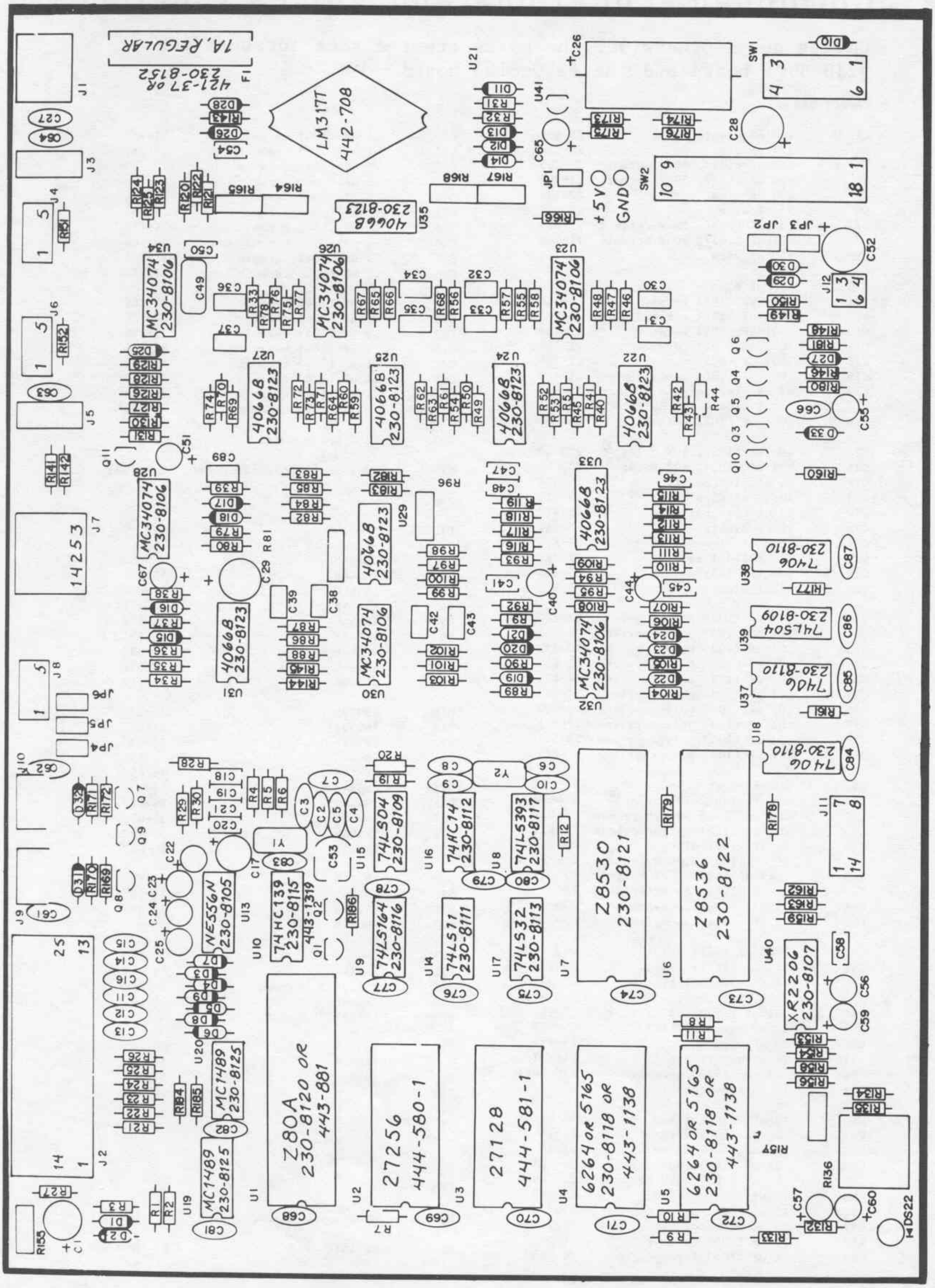
LED Installation



MAIN CIRCUIT BOARD (#230-8001)
Component Locations and Values



MAIN CIRCUIT BOARD (#230-8163)
Component Locations and Values (continued)



MAIN CIRCUIT BOARD
Component Locations and Values (continued)

Unless noted otherwise, the parts are the same for both the #230-8001 board and the #230-8163 board.

CAPACITORS

C1	100 uF electrolytic	25-885
C2	220 pF mica	20-120
C3	.01 uF (103), 50 V ceramic	21-769
C4	.01 uF (103), 50 V ceramic	21-769
C5	330 pF mica	20-139
C6	33 pF mica	230-8024
C7	.01 uF (103), 50 V ceramic	21-769
C8	.01 uF (103), 50 V ceramic	21-769
C9	820 pF mica	20-171
C10	680 pF mica	20-107
C11	.001 uF (102) ceramic	21-784
C12	.001 uF (102) ceramic	21-784
C13	.001 uF (102) ceramic	21-784
C14	.001 uF (102) ceramic	21-784
C15	.001 uF (102) ceramic	21-784
C16	.001 uF (102) ceramic	21-784
C17	47 uF electrolytic	25-915
C18	.1 uF (104), 10% Mylar®	230-8004
C19	.001 uF (102) ceramic	21-784
C20	.01 uF (103), 10% Mylar®	230-8003
C21	.01 uF (103), 10% Mylar®	230-8003
C22	10 uF electrolytic	25-917
C23	10 uF electrolytic	25-917
C24	10 uF electrolytic	25-917
C25	10 uF electrolytic	25-917
C26	1000 uF electrolytic	27-876
C27	.1 uF (104) ceramic	21-786
C28	100 uF electrolytic	25-885
C29	47 uF electrolytic	25-915
C30	.01 uF (103) polypropylene	27-822
C31	.01 uF (103) polypropylene	27-822
C32	.01 uF (103) polypropylene	27-822
C33	.01 uF (103) polypropylene	27-822
C34	.01 uF (103) polypropylene	27-822
C35	.01 uF (103) polypropylene	27-822
C36	.01 uF (103) polypropylene	27-822
C37	.01 uF (103) polypropylene	27-822
C38	.01 uF (103) polypropylene	27-822
C39	.01 uF (103) polypropylene	27-822
C40	10 uF electrolytic	25-917
C41	.1 uF (104), 10% Mylar®	230-8004
C42	.01 uF (103) polypropylene	27-822
C43	.01 uF (103) polypropylene	27-822
C44	10 uF electrolytic	25-917
C45	.1 uF (104), 10% Mylar®	230-8004
C46	.047 uF (473J), 2% Mylar®	27-129
C47	.1 uF (104), 5% Mylar®	27-77
C48	.0047 uF polypropylene	230-8021
C49	.1 uF (104), 5% Mylar®	27-77
C50	1200 pF (122) Mylar®	230-8009
C51	3.3 uF electrolytic	25-912
C52	47 uF electrolytic	25-915
C53	5-40 pF trimmer	230-8015
C54	.01 uF (103), 5% Mylar®	27-161
C55	10 uF electrolytic	25-917
C56	10 uF electrolytic	25-917
C57	10 uF electrolytic	25-917
C58	.022 uF (233) ceramic	230-8011
C59	10 uF electrolytic	25-917
C60	10 uF electrolytic	25-917
C61	.01 uF, 500V ceramic	21-16
C62	.01 uF, 500V ceramic	21-16
C63	.01 uF (103), 50V ceramic	21-769
C64	.01 uF (103), 50V ceramic	21-769
C65	10 uF electrolytic	25-917
C66	.1 uF (104) ceramic	21-786
C67	10 uF electrolytic	25-917
C68	.1 uF (104) ceramic	21-786
C69	.1 uF (104) ceramic	21-786
C70	.1 uF (104) ceramic	21-786
C71	.1 uF (104) ceramic	21-786
C72	.1 uF (104) ceramic	21-786
C73	.1 uF (104) ceramic	21-786
C74	.1 uF (104) ceramic	21-786
C75	.1 uF (104) ceramic	21-786
C76	.1 uF (104) ceramic	21-786
C77	.1 uF (104) ceramic	21-786
C78	.1 uF (104) ceramic	21-786
C79	.1 uF (104) ceramic	21-786
C80	.1 uF (104) ceramic	21-786
C81	.1 uF (104) ceramic	21-786
C82	.1 uF (104) ceramic	21-786
C83	.1 uF (104) ceramic	21-786
C84	.1 uF (104) ceramic	21-786
C85	.1 uF (104) ceramic	21-786
C86	.1 uF (104) ceramic	21-786
C87	.1 uF (104) ceramic	21-786
C88	On display board.	
C89	.047 uF (473K), 10% Mylar R	230-8005

DIODES

D1	1N4448	56-652
D2	1N4448	56-652
D3	1N4448	56-652
D4	1N4448	56-652
D5	1N4448	56-652
D6	1N4448	56-652
D7	1N4448	56-652
D8	1N4448	56-652
D9	1N4448	56-652
D10	1N5397	57-27
D11	1N5397	57-27
D12	1N5397	57-27
D13	1N4448	56-652
D14	1N4448	56-652
D15	1N4448	56-652
D16	1N4448	56-652
D17	1N4448	56-652
D18	1N4448	56-652
D19	1N4448	56-652
D20	1N4448	56-652
D21	1N4448	56-652
D22	1N4448	56-652
D23	1N4448	56-652
D24	1N4448	56-652
D25	1N4448	56-652
D26	1N4448	56-652
D27	1N5231 5.1V zener	56-16
D28	1N4448	56-652
D29	1N5397	57-27
D30	1N5397	57-27
D31	1N5397	57-27
D32	1N5397	57-27
D33	1N4448	56-652

LED

DS1-DS21	On display board.	
DS22	SLP151B, red	412-646

MAIN CIRCUIT BOARD
Component Locations and Values (continued)

TRANSISTORS

Q1	VN10LM	230-8101
Q2	VN10LM	230-8101
Q3	MPS6521	417-172
Q4	2N3906	417-874
Q5	MPS6561	230-8100
Q6	2N3904	417-875
Q7	2N3904	417-875
Q8	MPSA42	417-294
Q9	2N3906	417-874
Q10	2N3904	417-875
Q11	2N3904	417-875

RESISTORS

R1	4.7 kilohms, 5%, 1/4 W	6-472-12
R2	4.7 kilohms, 5%, 1/4 W	6-472-12
R3	1.0 kilohm, 5%, 1/4 W	6-102-12
R4	1.0 kilohm, 5%, 1/4 W	6-102-12
R5	1.0 kilohm, 5%, 1/4 W	6-102-12
R6	330 ohms, 5%, 1/4 W	6-331-12
R7	10 kilohms, 5%, 1/4 W	6-103-12
R8	10 kilohms, 5%, 1/4 W	6-103-12
R9	5.1 kilohms, 5%, 1/4 W	6-512-12
R10	5.1 kilohms, 5%, 1/4 W	6-512-12
R11	10 kilohms, 5%, 1/4 W	6-103-12
R12	10 kilohms, 5%, 1/4 W	6-103-12
R13-R18	On display board.	
R19	1.0 kilohm, 5%, 1/4 W	6-102-12
R20	1.0 kilohm, 5%, 1/4 W	6-102-12
R21	100 ohms, 5%, 1/4 W	6-101-12
R22	100 ohms, 5%, 1/4 W	6-101-12
R23	100 ohms, 5%, 1/4 W	6-101-12
R24	100 ohms, 5%, 1/4 W	6-101-12
R25	4.7 kilohms, 5%, 1/4 W	6-472-12
R26	100 ohms, 5%, 1/4 W	6-101-12
R27	100 ohms, 5%, 1/4 W	6-101-12
R28	10 ohms, 5%, 1/4 W	6-100-12
R29	4.7 kilohms, 5%, 1/4 W	6-472-12
R30	100 kilohms, 5%, 1/4 W	6-104-12
R31	243 ohms, 1%, 1/4 W	6-2430-12
R32	845 ohms, 1%, 1/4 W	6-8450-12
R33	10 kilohms, 5%, 1/4 W	6-103-12
R34	10 kilohms, 5%, 1/4 W	6-103-12
R35	39 kilohms, 5%, 1/4 W	6-393-12
R36	1.0 kilohm, 5%, 1/4 W	6-102-12
R37	4.7 kilohms, 5%, 1/4 W	6-472-12
R38	7.50 kilohms, 1%, 1/4 W	6-7501-12
R39	20.0 kilohms, 1%, 1/4 W	6-2002-12
R40	7.50 kilohms, 1%, 1/4 W	6-7501-12
R41	30.1 kilohms, 1%, 1/4 W	6-3012-12
R42	174 kilohms, 1%, 1/4 W	6-1743-12
R43	26.7 kilohms, 1%, 1/4 W	6-2672-12
R44	267 kilohms, 1%, 1/4 W	6-2673-12
R45	49.9 kilohms, 1%, 1/4 W	6-4992-12
R46	10.0 kilohms, 1%, 1/4 W	6-1002-12
R47	23.2 kilohms, 1%, 1/4 W	6-2322-12
R48	18.7 kilohms, 1%, 1/4 W	6-1872-12
R49	7.50 kilohms, 1%, 1/4 W	6-7501-12
R50	30.1 kilohms, 1%, 1/4 W	6-3012-12
R51	267 kilohms, 1%, 1/4 W	6-2673-12
R52	174 kilohms, 1%, 1/4 W	6-1743-12
R53	26.7 kilohms, 1%, 1/4 W	6-2672-12
R54	49.9 kilohms, 1%, 1/4 W	6-4992-12
R55	23.2 kilohms, 1%, 1/4 W	6-2322-12
R56	16.9 kilohms, 1%, 1/4 W	6-1692-12
R57	10.0 kilohms, 1%, 1/4 W	6-1002-12
R58	18.7 kilohms, 1%, 1/4 W	6-1872-12
R59	7.50 kilohms, 1%, 1/4 W	6-7501-12
R60	30.1 kilohms, 1%, 1/4 W	6-3012-12
R61	267 kilohms, 1%, 1/4 W	6-2673-12
R62	174 kilohms, 1%, 1/4 W	6-1743-12
R63	26.7 kilohms, 1%, 1/4 W	6-2672-12
R64	49.9 kilohms, 1%, 1/4 W	6-4992-12
R65	23.2 kilohms, 1%, 1/4 W	6-2322-12
R66	10.0 kilohms, 1%, 1/4 W	6-1002-12
R67	18.7 kilohms, 1%, 1/4 W	6-1872-12
R68	95.3 kilohms, 1%, 1/4 W	6-9532-12
R69	7.50 kilohms, 1%, 1/4 W	6-7501-12
R70	30.1 kilohms, 1%, 1/4 W	6-3012-12
R71	267 kilohms, 1%, 1/4 W	6-2673-12
R72	174 kilohms, 1%, 1/4 W	6-1743-12
R73	26.7 kilohms, 1%, 1/4 W	6-2672-12
R74	49.9 kilohms, 1%, 1/4 W	6-4992-12
R75	23.2 kilohms, 1%, 1/4 W	6-2322-12
R76	10.0 kilohms, 1%, 1/4 W	6-1002-12
R77	18.7 kilohms, 1%, 1/4 W	6-1872-12
R78	100 kilohms, 1%, 1/4 W	6-1003-12
R79	2.0 kilohms, 5%, 1/4 W	6-202-12
R80	510 kilohms, 5%, 1/4 W	6-514-12
R81	5000-ohm control	230-8090
R82	8.2 kilohms, 5%, 1/4 W	6-822-12
R83	80.6 kilohms, 1%, 1/4 W	6-8062-12
R84	19.6 kilohms, 1%, 1/4 W	6-1962-12
R85	22.1 kilohms, 1%, 1/4 W	6-2212-12
R86	23.2 kilohms, 1%, 1/4 W	6-2322-12
R87	10.0 kilohms, 1%, 1/4 W	6-1002-12
R88	18.7 kilohms, 1%, 1/4 W	6-1872-12
R89	10.0 kilohms, 1%, 1/4 W	6-1002-12
R90	10.0 kilohms, 1%, 1/4 W	6-1002-12
R91	200 ohms, 5%, 1/4 W	6-201-12
R92	200 ohms, 5%, 1/4 W	6-201-12
R93	20 kilohms, 5%, 1/4 W	6-203-12
R94	10 kilohms, 5%, 1/4 W	6-103-12
R95	100 kilohms, 5%, 1/4 W	6-104-12
R96	100-kilohm control	230-8086
R97	20 kilohms, 5%, 1/4 W	6-203-12
R98	80.6 kilohms, 1%, 1/4 W	6-8062-12
R99	19.6 kilohms, 1%, 1/4 W	6-1962-12
R100	6.49 kilohms, 1%, 1/4 W	6-6491-12
R101	23.2 kilohms, 1%, 1/4 W	6-2322-12
R102	10.0 kilohms, 1%, 1/4 W	6-1002-12
R103	18.7 kilohms, 1%, 1/4 W	6-1872-12
R104	10.0 kilohms, 1%, 1/4 W	6-1002-12
R105	10.0 kilohms, 1%, 1/4 W	6-1002-12
R106	200 ohms, 5%, 1/4 W	6-201-12
R107	200 ohms, 5%, 1/4 W	6-201-12
R108	100 kilohms, 5%, 1/4 W	6-104-12
R109	10 kilohms, 5%, 1/4 W	6-103-12
R110	20 kilohms, 5%, 1/4 W	6-203-12
R111	10 kilohms, 5%, 1/4 W	6-103-12
R112	24.3 kilohms, 1%, 1/4 W	6-2432-12
R113	8.06 kilohms, 1%, 1/4 W	6-8061-12
R114	24.3 kilohms, 1%, 1/4 W	6-2432-12
R115	8.06 kilohms, 1%, 1/4 W	6-8061-12
R116	24.3 kilohms, 1%, 1/4 W	6-2432-12
R117	8.06 kilohms, 1%, 1/4 W	6-8061-12
R118	33.2 kilohms, 1%, 1/4 W	6-3322-12
R119	11.0 kilohms, 1%, 1/4 W	6-1102-12
R120	33.2 kilohms, 1%, 1/4 W	6-3322-12
R121	11.0 kilohms, 1%, 1/4 W	6-1102-12
R122	10 kilohms, 5%, 1/4 W	6-103-12
R123	510 kilohms, 5%, 1/4 W	6-514-12
R124	1.0 kilohm, 5%, 1/4 W	6-102-12
R125	470 ohms, 5%, 1/4 W	6-471-12
R126	200 ohms, 5%, 1/4 W	6-201-12
R127	47 kilohms, 5%, 1/4 W	6-473-12
R128	510 kilohms, 5%, 1/4 W	6-514-12
R129	10 kilohms, 5%, 1/4 W	6-103-12

MAIN CIRCUIT BOARD
Component Locations and Values (continued)

Resistors (continued)

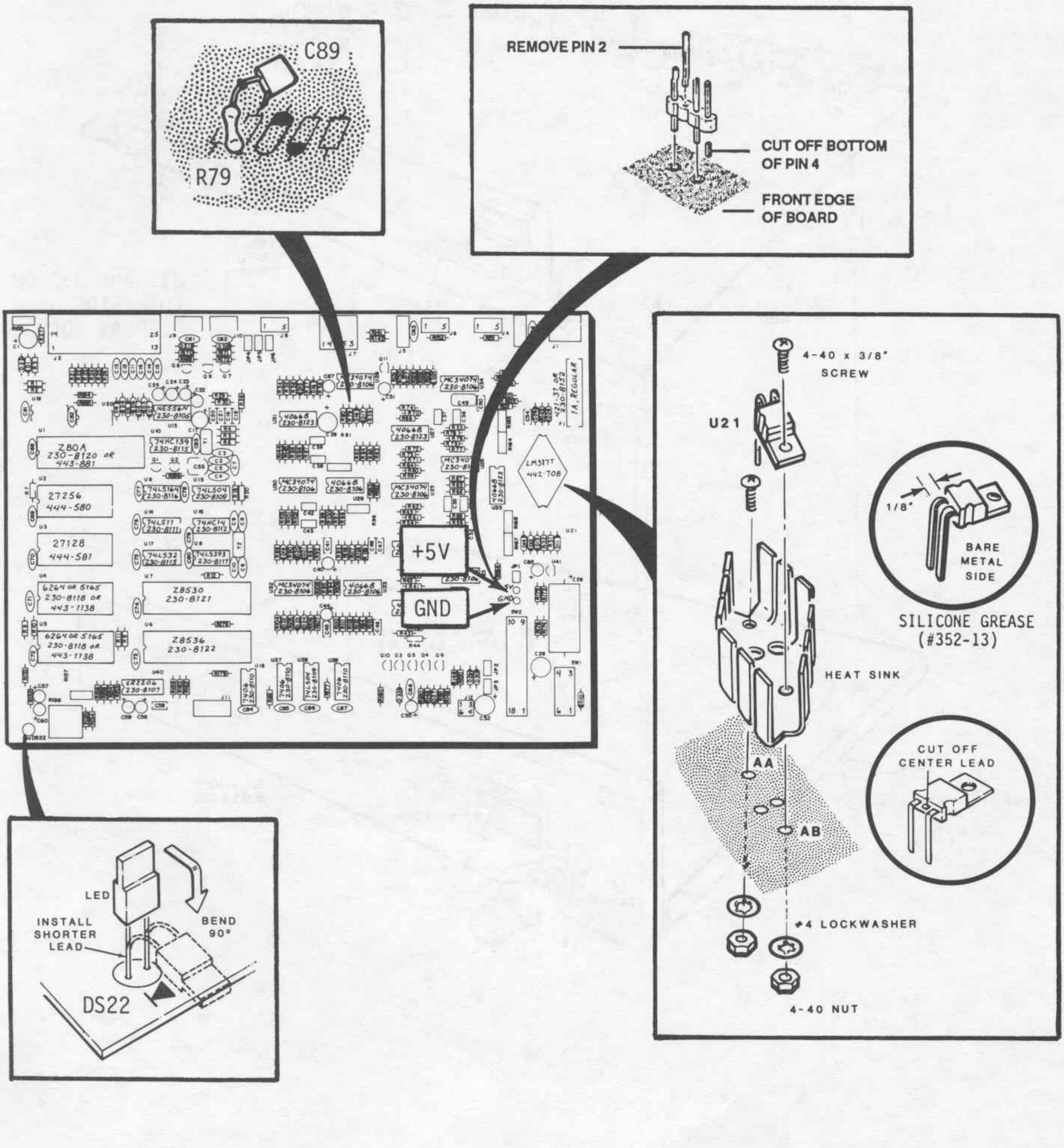
R130	10 kilohms, 5%, 1/4 W	6-103-12
R131	1.0 kilohm, 5%, 1/4 W	6-102-12
R132	5.1 kilohms, 5%, 1/4 W	6-512-12
R133	330 ohms, 5%, 1/4 W	6-331-12
R134	510 ohms, 5%, 1/4 W	6-511-12
R135	360 ohms, 5%, 1/4 W	6-361-12
R136	1000-ohm control (on #230-8001 main board)	230-8084
R136	1000-ohm control (on #230-8163 main board)	230-8161
R137-R140	On display board.	
R141	4.7 kilohms, 5%, 1/4 W	6-472-12
R142	4.7 kilohms, 5%, 1/4 W	6-472-12
R143	10 kilohms, 5%, 1/4 W	6-103-12
R144	4.7 kilohms, 5%, 1/4 W	6-472-12
R145	4.7 kilohms, 5%, 1/4 W	6-472-12
R146	10 kilohms, 5%, 1/4 W	6-103-12
R148	1.0 kilohm, 5%, 1/4 W	6-102-12
R149	4.7 kilohms, 5%, 1/4 W	6-472-12
R150	20 kilohms, 5%, 1/4 W	6-203-12
R151	680 ohms, 5%, 1/4 W	6-681-12
R152	680 ohms, 5%, 1/4 W	6-681-12
R153	4.99 kilohms, 1%, 1/4 W	6-4991-12
R154	4.99 kilohms, 1%, 1/4 W	6-4991-12
R155	25-kilohm control	230-8088
R156	4.99 kilohms, 1%, 1/4 W	6-4991-12
R157	500-ohm control	230-8089
R158	4.99 kilohms, 1%, 1/4 W	6-4991-12
R159	200 ohms, 5%, 1/4 W	6-201-12
R160	3.3 kilohms, 5%, 1/4 W	6-332-12
R161	4.7 kilohms, 5%, 1/4 W	6-472-12
R162	15 kilohms, 5%, 1/4 W	6-153-12
R163	18 kilohms, 5%, 1/4 W	6-183-12
R164	10-kilohm control	230-8085
R165	10-kilohm control	230-8085
R166	12 kilohms, 5%, 1/4 W	6-123-12
R167	20-kilohm control	230-8087
R168	10-kilohm control	230-8085
R169	4.7 kilohms, 5%, 1/4 W	6-472-12
R170	68 ohms, 5%, 1/4 W	6-680-12
R171	430 ohms, 5%, 1/4 W	6-431-12
R172	120 ohms, 5%, 1/4 W	6-121-12
R173	243 ohms, 1%, 1/4 W	6-2430-12
R174	1.69 kilohms, 1%, 1/4 W	6-1691-12
R175	3.09 kilohms, 1%, 1/4 W	6-3091-12
R176	6.19 kilohms, 1%, 1/4 W	6-6191-12
R177	4.7 kilohms, 5%, 1/4 W	6-472-12
R178	10 kilohms, 5%, 1/4 W	6-103-12
R179	10 kilohms, 5%, 1/4 W	6-103-12
R180	4.7 kilohms, 5%, 1/4 W	6-472-12
R181	1.0 kilohm, 5%, 1/4 W	6-102-12
R182	4.7 kilohms, 5%, 1/4 W	6-472-12
R183	4.7 kilohms, 5%, 1/4 W	6-472-12
R184	10 kilohms, 5%, 1/4 W	6-103-12
R185	10 kilohms, 5%, 1/4 W	6-103-12
R186	330 ohms, 5%, 1/4 W	6-331-12

CRYSTALS

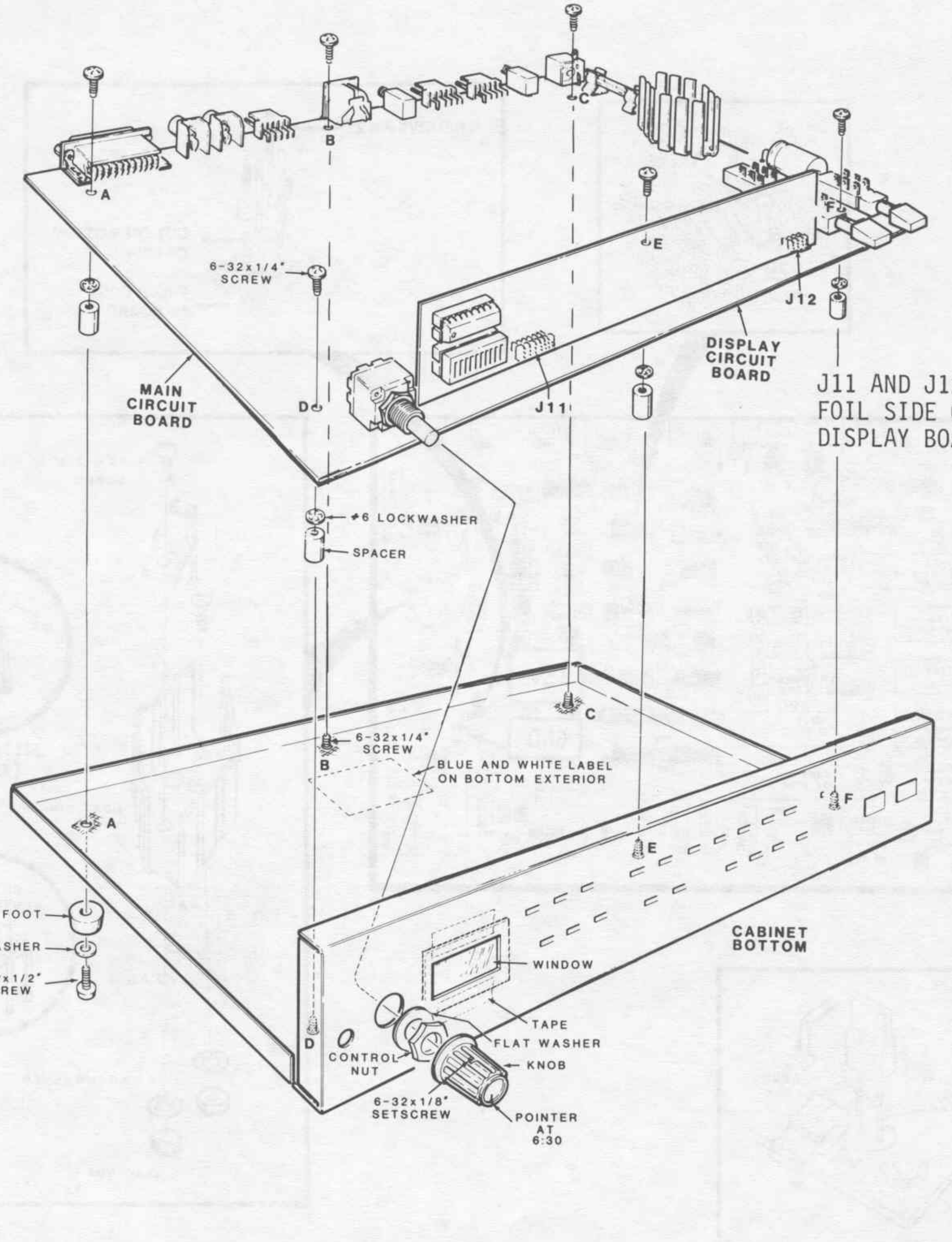
Y1	4.0000 MHz	230-8142
Y2	2.4576 MHz	230-8141

MAIN CIRCUIT BOARD (continued)
Special Component Locations

NOTE: C89 is installed as shown in the inset only on the first production run (#230-8001 board). In later production runs, it's mounted on the circuit board.

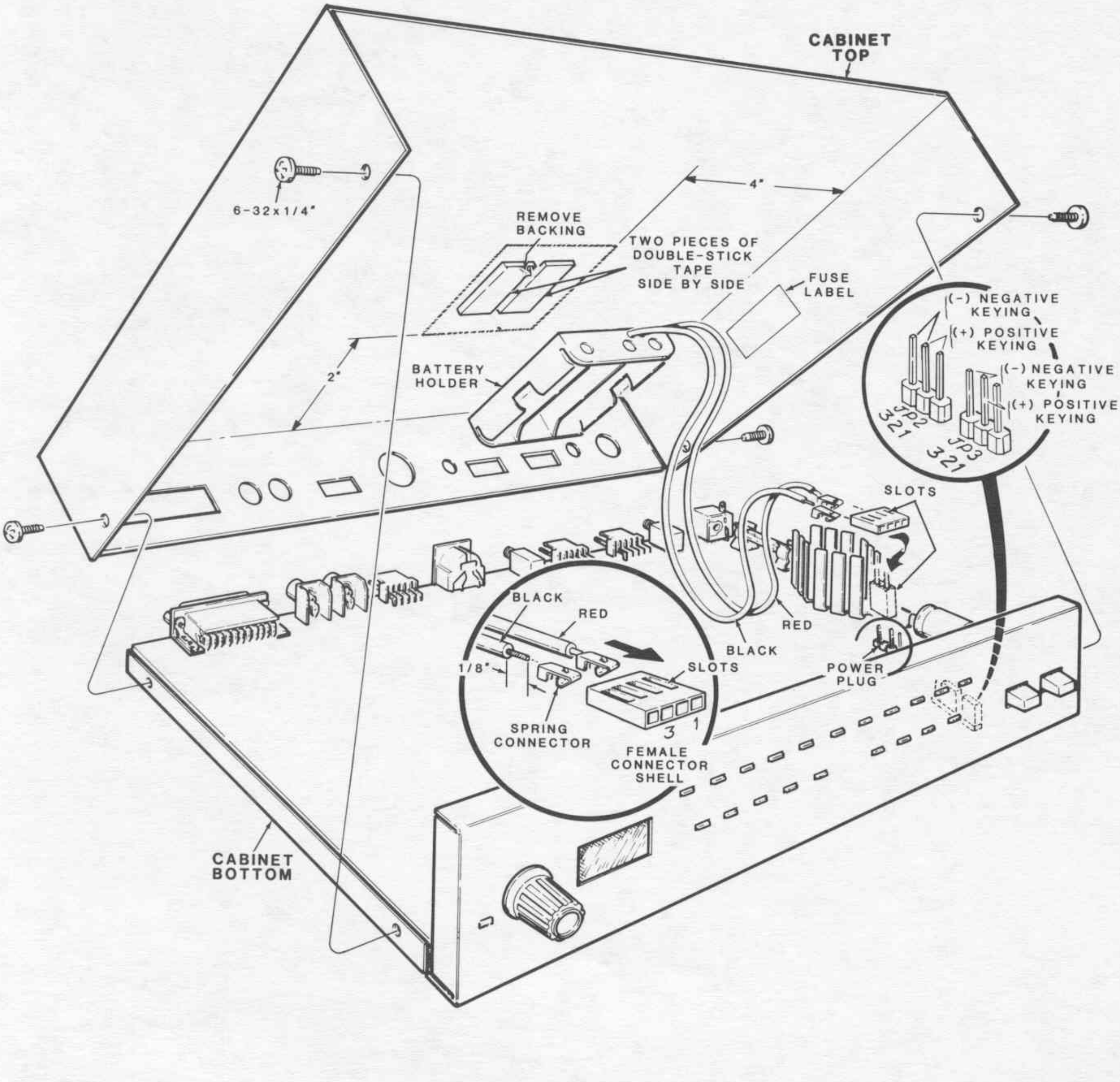


CHASSIS
Exploded View

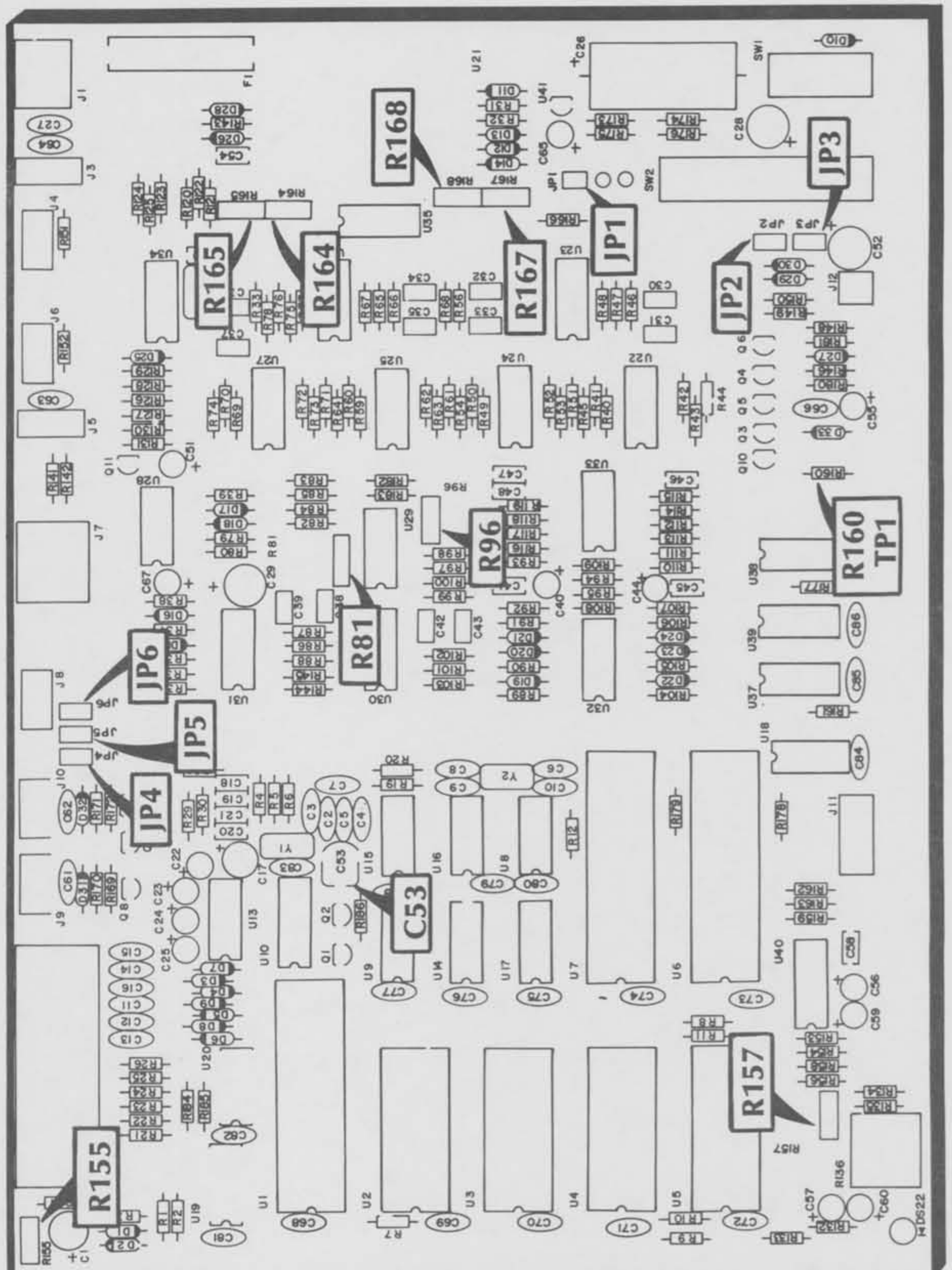


J11 AND J12 ON FOIL SIDE OF DISPLAY BOARD

CHASSIS (continued)
Battery Backup Wiring



CONFIGURATION AND ALIGNMENT


R168
JP3
JP1
R165
R164
R167
JP2
R96
R160
TP1
R81
JP6
JP5
JP4
C53
R157
R155

EQUIPMENT NEEDED

To align the HK-232, you will need the following test equipment. The test equipment specifications should meet or exceed those listed after each item. The suggested model numbers at the end of each item will fulfill these requirements.

Oscilloscope: DC to 25 MHz, dual trace, triggered sweep. IO-4225 or equivalent.

Low-Capacitance Oscilloscope Probe: Input capacitance adjustable between 15-50 pF, 4-nS rise time. Heath PKW-105 or equivalent.

Digital Multimeter: High-impedance input. Measures ohms, AC/DC voltage, and AC/DC current. Heath SM-77 or equivalent.

Frequency Counter: Able to measure from 5 Hz to 512 MHz with a resolution from 0.1 Hz to 1000 Hz. Heath IM-2420 or equivalent.

13 VDC, 700 mA Power Supply: Heath power cube (#150-333) or equivalent.

Computer Terminal: RS-232C and ASCII compatible. Data rate adjustable to 600 or 9600 baud. Heath H-19 or equivalent. Alternately, you can use a computer and terminal emulation software, such as the Heath HS-158 and HUGMCP (#885-3033-37 from Heath Users' Group).

CONFIGURATION

There are six jumpers on the main board which configure the HK-232, JP1-JP6. JP1 through JP3 are set using Berg jumpers, while JP4-JP6 are foil runs on the foil-side of the board. The following table defines each jumper setting and their default values.

Jumper	Description
JP1	Open: No battery backup (default). Closed: Battery backup selected.
JP2	+ (front pin): RADIO 1 PTT is positive (default). - (back pin): RADIO 1 PTT is negative.
JP3	+ (front pin): RADIO 2 PTT is positive (default). - (back pin): RADIO 2 PTT is negative.
JP4	INT (front hole): Internal modem RX data (default). EXT (back hole): External modem RX data.
JP5	INT (front hole): Internal modem TX data (default). EXT (back hole): External modem TX data.
JP6	INT (front hole): Internal modem DCD handshake (default). EXT (back hole): External modem DCD handshake.

The external modem option permits using the HK-232 in custom applications that require data rates higher than 1200 baud. To modify the unit, remove the circuit board and cut the foil runs bridging the center hole to the front (see "X-Ray Views"). Next, on the component-side of the board, solder jumper wires from the center holes to the ones closest to the back.

ALIGNMENT

NOTE: Some of the following adjustments, along with any repairs you may have made to the AFSK modulator, will change the amplitude of the AFSK output signal. The AFSK LEVEL control, R155, sets this amplitude, but must be adjusted to the specifications of the customer's radio. Refer the customer to chapter four in the "HK-232 PackKit User's Manual" (#595-3902) for final adjustments.

Preliminary Setup

-- Remove the cabinet top as described in "Disassembly."

-- Connect the HK-232 to a 13 VDC, 700 mA power supply, such as the optional #150-333 power cube.

-- Connect a terminal or computer to the HK-232's serial port. If using a computer, boot up a terminal emulation program such as HUGMCP.

-- Set the terminal for 1200 baud, 7 or 8 data bits, no parity, and 1 stop bit.

-- Adjust the HK-232 THRESHOLD control FCCW.

-- Turn on the HK-232. You should get the following message on the terminal's screen.

Please type a star (*) for auto-baud routine.

-- Type three or four asterisks, at one-second intervals, until you see the sign-on message.

Heathkit HK-232 Multi-Mode TNC
Copyright (C) 1986, 1987 by
Heath Company and AEA, Inc.
Release DD-MMM-YY
Checksum $nn
cmd:

Calibration Procedure

The AFSK generator frequencies will be adjusted using the HK-232's internal calibration routine and built-in frequency meter. Refer to the control and jumper locations pictorial at the beginning of this section as you perform the following steps.

-- Allow the HK-232 to warm up for at least 20 minutes.

-- Connect the frequency counter to U15-12 and adjust C53 as close as possible to 4.000 MHz.

NOTE: The following steps direct you to adjust several controls using an indication on the computer's display. If you wish to use the frequency counter instead, connect it to TP1 (the indicated lead of R160).

-- Type **CAL <RETURN>** to start the calibration procedure.

-- Adjust R167 for a reading of 1200 Hz, ±10 Hz.

If adjusting R167 has no effect, press the space bar to toggle between the mark and space frequencies.

-- Press the space bar.

-- Adjust R165 for a reading of 2200 Hz, ±10 Hz.

-- Press the **H** key to change to narrow-shift operation. Note that the H key toggles between wide-shift and narrow shift.

-- Adjust R164 for a reading of 2310 Hz, ±5 Hz.

If adjusting R164 has no effect, press the space bar once and try again.

-- Press the space bar.

-- Adjust R168 for a reading of 2110 Hz, ±5 Hz.

-- Connect an oscilloscope or AC voltmeter to TP1 (R160).

-- Press the **Q** key to exit the calibration procedure.

-- Adjust R157 for minimum signal (typically less than 3 mVAC RMS). This is the AFSK null adjustment.

-- Connect a jumper wire from J4-2 to J4-1 and release the RADIO 1 pushbutton (out position).

-- Type **CAL <RETURN>**.

-- Press the **H** key.

The frequency counter should read 2110 Hz, $\pm$5 Hz. If not, press the space bar.

-- Connect the oscilloscope or AC voltmeter to U30-14.

-- Adjust R81 for maximum signal amplitude (typically greater than 1 VAC RMS).

-- Press the space bar. The on-screen frequency counter should read 2310 Hz, +5 Hz.

-- Connect the oscilloscope or AC voltmeter to U30-1.

-- Adjust R96 for maximum signal amplitude (typically greater than 1 VAC RMS).

-- Connect the oscilloscope or AC voltmeter to TP1.

-- Note the current setting of R155.

-- Rotate R155 from FCCW to FCW. The signal should rise from about 3 mVAC RMS to about 1 VAC RMS.

-- Restore R155 to its original setting.

If the unit hasn't been calibrated before, set R155 for a signal of about 2 mVAC RMS at TP1.

-- Press the **Q** key to exit the calibration routine.

Alignment complete.

Facsimile Transmit Tone Recalibration

Perform the following if you want to transmit facsimile instead of VHF packet. The two are exclusive because packet uses 1000-Hz shift while facsimile uses 800 Hz.

-- At the "cmd:" prompt, type **CAL <RETURN>.**

The monitor should display:

1200 R167

If the resistor is R165, press the space bar.

-- Adjust R167 for a 1300-Hz tone.

-- Press the space bar.

-- Adjust R165 for a 2100-Hz tone.

Alignment complete. To restore packet operation, perform the above procedure, but substitute 1200 Hz for R167 and 2200 Hz for R165.

TROUBLESHOOTING

EQUIPMENT NEEDED

To troubleshoot the HK-232, you will need the following test equipment. The test equipment specifications should meet or exceed those listed after each item. The suggested model numbers at the end of each item will fulfill these requirements.

Oscilloscope: DC to 25 MHz, dual trace, triggered sweep, IO-4225 or equivalent.

Low-Capacitance Oscilloscope Probe: Input capacitance adjustable between 15-50 pF, 4-nS rise time. Heath PKW-105 or equivalent.

Logic Probe: DC to 20 MHz, capable of detecting 10 nS single pulses. Indicates logic one, logic zero, and high-impedance states. Heath IT-7410, or Hewlett-Packard HP-545A, or equivalent.

Digital Multimeter: High-impedance input. Measures ohms, AC/DC voltage, and AC/DC current. Heath SM-77 or equivalent.

Frequency Counter: Able to measure from 5 Hz to 512 MHz with a resolution from 0.1 Hz to 1000 Hz. Heath IM-2420 or equivalent.

Audio Signal Generator: Able to generate sine waves from 1 Hz to 100 kHz. Amplitude adjustable from 1 mV to 10 V RMS. Heath IG-18 or equivalent.

DC Power Supply: 12 VDC, 1 A. Heath #150-333 or equivalent.

Computer Terminal: RS-232C and ASCII compatible. Data rate adjustable to 1200 baud. Heath H-19 or equivalent. Alternately, you can use a computer and terminal emulation software, such as the Heath HS-158 and HUGMCP (885-3033-37 from Heath Users' Group).

SERVICE HINTS

NOTE: To get consistent results, unplug the RAM backup batteries while you perform these tests.

Digital Circuits

UNIT DEAD OR LOCKED UP

Unless noted otherwise, the components mentioned in the following steps are located on the "Digital Circuits" schematic.

No LEDS Lit

-- Check the circuitry for damaged or improperly-installed components (see "Visual Checks").

-- Check the temperature of the components. Except for the following, they should be near room temperature.

Component	Temperature
D11	47.8°C (118.0°F)
D12	43.2°C (109.8°F)
U1	37.5°C (99.5°F)
U6	34.7°C (94.5°F)
U7	33.0°C (91.4°F)
U21	72.0°C (161.6°F)

-- Check the power supply voltages. Make sure the outputs are properly filtered.

MODE and STATUS LED Symptoms

Observe the MODE and STATUS LEDs and perform the appropriate checks. These checks assume that the DCD and TUNE LEDs are okay.

All MODE and STATUS LEDs Off

If some flash briefly at powerup:

-- Check for a 2.4576 TTL square wave at U7-20.

If missing, check U15B, U15D, and Y2.

-- Check for pulses on U7-33.

If missing, check U17B, the continuity from U17B-5 to U1-37, and the continuity of U17B-4 to U1-20.

-- Check for pulses on U7-7.

If missing, check for an open R11 or a short to ground at U6-17. Check U6.

-- Replace U7.

If the LEDs don't flash at all:

-- Check the continuity of the +5 volt supply through J12-1 to the display board.

MULT, STA, SEND, and CON LEDs Lit; Others Off

-- Check for 4 MHz clock pulses at U1-6, U6-16, and U9-8. If any are missing, trace back to U15F and U15E.

-- Monitor the $\overline{\text{RESET}}$ line at U1-26 as you turn on the unit.

The line should remain low for about 1/4 second, then jump to logic one. This delay is necessary because the Z80 requires at least three clock pulses while reset is low to initialize itself. If the delay isn't present, the reset line will go high before the 4 MHz crystal clock can start oscillating. The result is that the Z80 locks up. All the address bus lines will be high and the data bus will usually be low (depending on the memory contents of U5).

If there's no 1/4-second delay, or the line remains low, check U16C, U19B, C1, and the associated components.

-- Remove U3.

If the unit now powers up properly, replace U3.

NOTE: This test works properly in the first production run, but may not in the future. If in doubt, check the Technical Exchange or with the Tech Consultants for up-to-date information.

-- Check for pulses at U1-24.

If missing, check U16E, U14C, U16B, U9, and U16D.

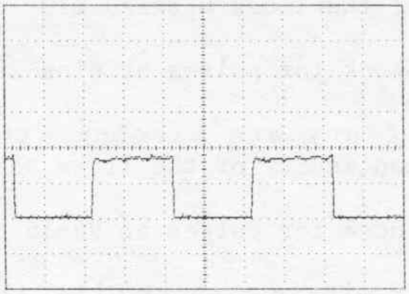
-- Check the data, address, and control bus lines for short circuits.

Signals on the address and control lines will typically have steep rise and fall times. Data line signals will have steep trailing edges, but the leading edges are slightly rounded near the top. If these conditions aren't present, suspect a leaky component on the bus.

The signals should switch from less than +0.8 volts (logic zero) to greater than +2.4 volts (logic one). If the pulse on one or more lines doesn't reach either of these limits, or appears to "step" when switching, suspect a short circuit to an adjacent bus line.

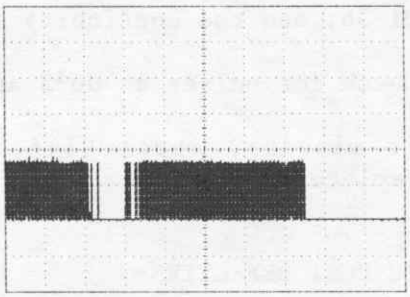
A0 U1-30
(Synchronizing Signal)
V = 2.0 V/div
H = 500 nS/div

Baseline at division 2



A10 U1-40
(Synchronizing Signal)
V = 2.0 V/div
H = 20 uS/div

Baseline at division 2



You can quickly check the address bus by removing all the RAM and remaining ROM chip. A properly-working Z80 will begin generating square waves on all address lines similar to the above. A0 will generate a 2 uS signal, while each succeeding line has a frequency that is lower by a factor of two. From A7 to A15 the square waves will be modulated by 1 uS square waves. All this takes place because the Z80 is attempting to read memory (you will also see pulses on U1-19, U1-21, and U1-27). Since there is no memory, the data bus lines are all logic zero, which is the Z80 NOP (No OPeration) instruction. Use the guidelines from the previous two paragraphs to check the address bus. If the rise and fall times look good, but the signal is irregular, make sure none of the data bus lines are being pulled high. If any are, suspect U6 and U7. Otherwise, check the Z80 and the memory chips that you removed.

-- Reinstall the ICs.

-- Check for pulses at U4-20 and U5-20.

If either are missing, check the appropriate FET at Q1 and Q2, the memory decoder at U10, and the continuity of the lines between U10 and U1.

-- Check for pulses at pins 22 and 27 of U4 and U5.

If any are missing, check U17C, U17D, and the continuity of the lines between U17 and U1.

-- Check for pulses at U6-36.

If missing, check U17A, the continuity from U17A-1 to U1-36, and the continuity from U17A-2 to U1-20.

-- Check for pulses at U6-5 and U6-6.

If missing, check U14A, U14B, and U16A. If okay, replace U6.

RS-232C PORT DEFECTIVE

The LEDs respond properly at powerup, but the HK-232 can't communicate with the computer terminal.

-- Make sure the terminal is set to 1200 baud, 8 data bits, 1 stop bit, and no parity.

-- Check the RS-232C power supply at U13.

-- Check U7, U19, and U20.

-- Verify that the DTR line on Pin 2 of J2, or the RTS line on Pin 4 of J2 (the RS232C I/O connector) are not being held low.

If the controller software flow control is disabled by setting START, STOP, XON and XOFF to 00 (hex) and XFLOW to OFF, the controller will not send data to the terminal unless DTR and RTS are asserted.

If the computer or terminal does not provide the DTR/CTS protocol or "handshake", the DTR/CTS lines (pins 20 and 5 on J2) should not be connected.

PARALLEL PORT DEFECTIVE

General

-- Check the continuity of the interconnect cable.

-- Check for short circuits on the inputs of the display drivers, U11, U12, and U18

-- Check U6.

FAX Mode

Appears to Print Two Pictures Side by Side

-- Reduce the FSPEED setting.

You are probably trying to print a facsimile transmission that is being sent at 240 lines per minute with the FSPEED set to 120 lines per minute. Similarly, the transmission may be at 120 lines per minute with the FSPEED set to 60 lines per minute.

Printer Never Prints

-- Make sure PRCON is ON, the THRESHOLD control is FCW, and the DCD LED is lit.

If the DCD LED is off, check U34A, U34B, and Q11.

-- Check the OPMODE to make sure it is FAX SYNC RECEIVE.

If not, type **FAX <RETURN>** to enter the facsimile mode. Next, type **LOCK <RETURN>** to force a synchronization lock. If the printer doesn't begin printing in about a minute, type **PROUT ON <RETURN>** to reroute the HK-232 serial output to the printer. If the printer now starts to print, its graphics commands probably aren't supported by the firmware. In the first production run, the HK-232 supported only Epson-compatible printers. In later runs, twelve other manufacturers were added. Refer to the PRTYPE command under "New Commands" in "Operation" for more details.

Picture Edges Veer Towards Left or Right

-- Check the frequency of the 4 MHz oscillator.

Monitor U1-6 with a frequency counter and adjust C53 for a reading of 4 MHz ±10 Hz.

Analog Circuits

MODEM CANNOT BE CALIBRATED

If the calibration signal is present, but you cannot successfully calibrate the frequency, the value of a frequency-determining component may have changed.

-- Verify that the proper signals are present at TP1 (see "Waveforms").

If not, check U40 and the values of its passive components.

-- Check for pulses at U6-30.

If present, substitute a known-good IC at U6. Otherwise, trace back through U39B to U40.

-- Make sure that the proper switching voltages are at pins 5, 6, and 13 of U35.

If not, check U6, U37C, U37D, and U39C. Otherwise, check U35.

TRANSMITTER CANNOT BE KEYED

If the transmitter cannot be keyed, but the DCD Threshold control functions normally:

-- Check the watchdog timer circuit at Q10 and Q3.

-- Check the PTT driver transistors Q4 and Q5.

-- Check the timing capacitor C55.

If the DCD Threshold control has no effect on the DCD LED and the LED is permanently lit:

-- Check U34A and U34B.

-- Check for an open circuit at R136.

TRANSMITTED SIGNALS NOT COPYABLE BY OTHER STATIONS

If the problem is only on FM:

-- Verify the associated transmitter's modulation index.

The peak deviation for any tone should not exceed 4 kHz.

-- Adjust the AFSK output level with R155 to produce the correct transmitter deviation.

If the problem is only on SSB:

-- Make sure the customer is using the lower sideband or the sideband called for by the customer's regional agreements.

-- Verify that the transmitter's audio input stage and ALC systems are not being overdriven.

-- Adjust the transmitter's microphone gain in accordance with the radio manuafacturer's duty cycle, plate current and power dissipation specifications.

-- If reducing the radio's gain control does not solve the problem, adjust the AFSK output level with R155 to produce the correct transmitter operating conditions.

If the HK-232 won't transmit in any mode, connect J4-1 to J4-2 and trace the signal from output to input (see "Analog Circuits Waveforms").

TRANSMITS PACKETS OKAY, BUT NOTHING ELSE

-- Check U6, U39D, and U38C.

WILL NOT TRANSMIT PACKETS, OTHER MODES OKAY

-- Check U7, U8, U39E, and U38B.

RECEIVED SIGNALS NOT COPYABLE

If unable to correctly decode signals from other stations:

-- Verify that the HK-232 is set for the proper mode.

-- Verify the correct settings of R81 and R96.

-- Verify that the DCD Threshold control is operating correctly.

Connect J4-1 to J4-2 and trace the signal from output to input (see "Analog Circuits Waveforms").

RECEIVES PACKETS OKAY, BUT NOTHING ELSE

-- Check for an open circuit between U7-18 and U15C-6.

-- Replace U7.

CANNOT DETECT PACKETS, OTHER MODES OKAY

-- Check for open circuit between U7-13 and U15C-6.

-- Replace U7.

RECEIVER FILTER CHECKS

Perform the following checks if you need to test the stage gain and frequency response of the receiver filters. If you need to signal trace a dead receiver, refer to "Logic Circuits Waveforms."

Filter Control Line Checks

Before performing extended tests on the receiver filter circuits, make sure the control lines to the 4066B electronic switches are functioning properly. The following table shows the voltage level for each mode. Zero volts opens the switch and +13 volts closes it. Note that the exact value of the switch-closing voltage depends on the external DC power supply.

The switch settings in the schematic correspond to the RTTY (WI ON) mode. They were measured when the unit was just turned on, battery backup was disconnected, and nothing was connected to the serial, parallel, or radio ports.

Mode	HF	VHF	CW	NCW
Packet (VHF ON)	0 V	+13 V	0 V	+13 V
Packet (VHF OFF)	+13 V	0 V	0 V	+13 V
Morse	0 V	0 V	+13 V	0 V
RTTY (WI ON)	0 V	+13 V	0 V	+13 V
RTTY (WI OFF)	+13 V	0 V	0 V	+13 V
AMTOR	+13 V	0 V	0 V	+13 V
Facsimile	0 V	+13 V	0 V	+13 V

If any of these voltages are incorrect, trace back though the appropriate inverter at U37 and U39 to U6 on the "Digital Circuits" schematic.

Set Up

-- Release SW2 to put the HK-232 in the RADIO 1 mode.

-- Disconnect the internal battery backup cable and any external cables (other than the power supply).

-- Connect an audio sine wave generator to J4-1.

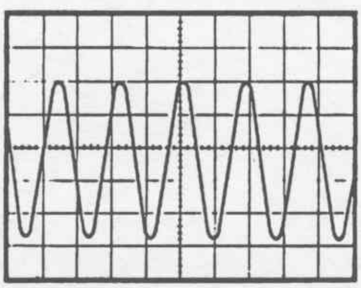
-- Turn on the generator and the HK-232.

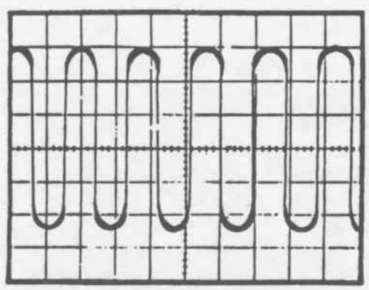
If there's a problem in only the VHF ON/WIDESHIFT ON modes, such as packet, perform the steps under "Bandpass Filter; VHF On." If there's a problem with the narrow-shift modes, such as Baudot, perform the steps under "Bandpass Filter; VHF Off."

Bandpass Filter; VHF ON

-- Refer to the following normalized waveforms and voltage tables and check the signal at U28A-1 and U26D-14. Check both frequencies and keep the generator amplitude at 400 mV P-P. Adjust the scope horizontal sweep and vertical gain as necessary.

If the signals are okay, skip the following steps and proceed to "Mark and Space Filters; VHF On." Otherwise, signal trace through the filter to find the faulty stage. The table lists the stages from input to output, but if you'd prefer to move from back to front, or starting in the middle, use the technique you're comfortable with.





Test Point	Amplitude (V P-P) 1100 Hz	2100 Hz	Waveform
U28D-14	0.800	1.000	A
U28B-7	0.100	1.300	A
U23A-1	0.250	2.000	A
U23D-14	0.600	3.000	A
U26A-1	1.800	4.500	A
U26D-14	5.000	6.500	A
U28A-1	1.100	1.200	B

-- If the waveforms are correct, skip the following checks and proceed to "Mark and Space Filters; VHF On."

-- Check the bias voltages at the suspected faulty stage. They should be close to those shown on the schematic diagram. If so, check the 4066B electronic switch and the capacitors at that stage. Otherwise, perform the following.

NOTE: Because the bandpass filter is direct-coupled and has a lot of feedback loops, a stage with faulty DC bias will affect stages in front of it and behind it. (You do not need to perform the following steps if only U28A is faulty. It's isolated from the bandpass filter by C89.)

-- Lift U23A-1 to break the loop.

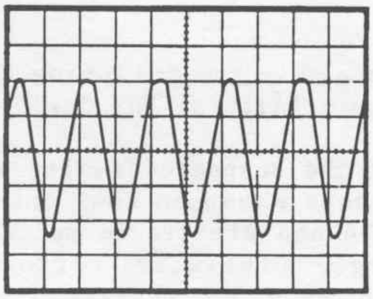
-- Check U23C/U23D, U23A/U23B, and U26C/U26D in that order.

Their voltages should be the values shown on the schematic. The first stage to exhibit incorrect bias voltages is the area to troubleshoot. However, if these stages are okay, check U28D and U28A. If these are okay, the problem is in the U23A/U23B stage.

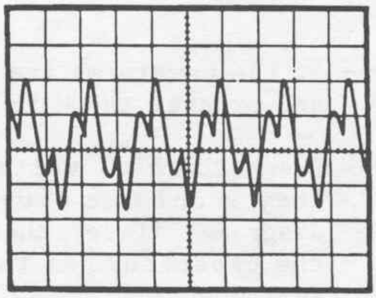
Mark and Space Filters; VHF ON

-- Adjust the signal generator to 1100 Hz, 400 mV P-P.

-- Refer to the following normalized waveforms and voltage table and check the signals U30 and U32. Adjust the scope horizontal sweep and vertical gain as necessary.



Waveform A

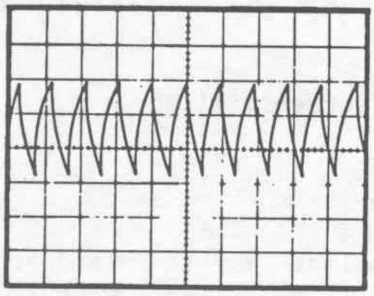


Waveform B

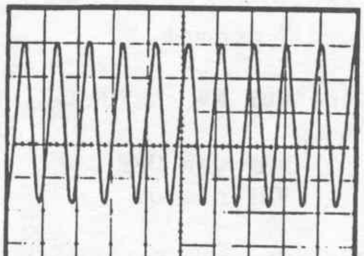
Test Point	Amplitude (V P-P) 1100 Hz	Waveform
U30D-14	5.000	A
U32D-14	5.000	A
U30A-1	1.800	B
U32A-1	1.800	B

-- Adjust the signal generator to 2100 Hz, 400 mV P-P.

-- Refer to the following normalized waveforms and voltage table and check the signals at U30 and U32. Adjust the scope horizontal sweep and vertical gain as necessary.



Waveform A



Waveform B

Test Point	Amplitude (V P-P) 2100 Hz	Waveform
U30D-14	2.800	A
U32D-14	2.800	A
U30A-1	4.800	B
U32A-1	4.800	B

-- If the waveforms are correct, skip the following checks and proceed to "Bandpass Filters; VHF Off."

-- Check the bias voltages at the suspected faulty stage. They should be close to those shown on the schematic diagram. If so, check the 4066B electronic switch and the capacitors at that stage. Otherwise, trace the stages with incorrect bias voltages back towards U28A.

Bandpass Filters; VHF OFF

-- Turn the THRESHOLD control FCCW.

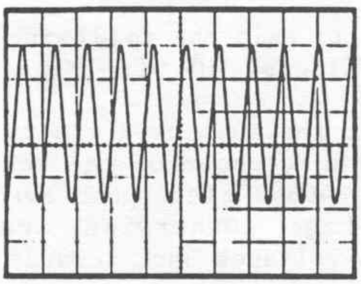
-- Connect a computer to the HK-232 and enter * (asterisks) until you get the sign-on message and the "cmd:" prompt.

-- Type **VHF FF <RETURN>**. The screen will show:

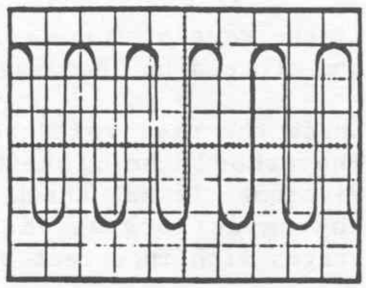
VHF was OFF
VHF now ON

-- Refer to the following normalized waveforms and voltage tables and check the signal at U28A-1 and U26D-14. Check both frequencies and keep the generator amplitude at 400 mV P-P. Adjust the scope's horizontal sweep and vertical gain as necessary.

If the signals are okay, skip the following steps and proceed to "Mark and Space Filters; VHF Off." Otherwise, signal trace through the filter to find the faulty stage. The table lists the stages from input to output, but if you'd prefer to move from back to front, or starting in the middle, use the technique you're comfortable with.



Waveform A



Waveform B

Test Point	Amplitude (V P-P) 2080 Hz	2310 Hz	Waveform
U28D-14	1.000	1.600	A
U28B-7	0.340	1.100	A
U23A-1	0.700	1.600	A
U23D-14	1.400	2.800	A
U26A-1	3.000	4.500	A
U26D-14	6.800	6.500	A
U28A-1	1.200	1.200	B

-- If the waveforms are correct, skip the following checks and proceed to "Mark and Space Filters; VHF Off."

-- Check the bias voltages at the suspected faulty stage. They should be close to those shown on the schematic diagram. If so, check the 4066B electronic switch and the capacitors at that stage. Otherwise, perform the following.

NOTE: Because the bandpass filter is direct-coupled and has a lot of feedback loops, a stage with faulty DC bias will affect stages in front of it and behind it. (You do not need to perform the following steps if only U28A is faulty. It's isolated from the bandpass filter by C89.)

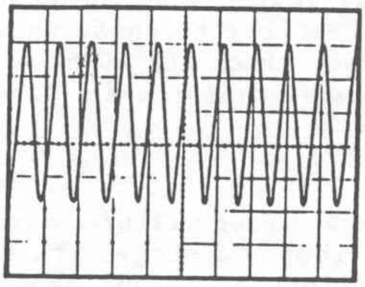
-- Lift U23A-1 to break the loop.

-- Check U23C/U23D, U23A/U23B, and U26C/U26D in that order.

Their voltages should be the values shown on the schematic. The first stage to exhibit incorrect bias voltages is the area to troubleshoot. However, if these stages are okay, check U28D and U28A. If these are okay, the problem is in the U23A/U23B stage.

Mark and Space Filters; VHF OFF

-- Refer to the following normalized waveform and voltage tables and check the indicated test points. Check both frequencies and keep the generator amplitude at 400 mV P-P. Adjust the scope's horizontal sweep and vertical gain as necessary.



Waveform A

Test Point	**Amplitude (V P-P) 2080 Hz**	**2310 Hz**	**Waveform**
U30D-14	5.000	2.400	A
U32D-14	4.800	2.400	A
U30A-1	1.800	5.100	A
U32A-1	1.800	5.100	A

-- If the waveforms are correct, skip the following check and proceed to "Low-Pass Filter."

-- Check the bias voltages at the suspected faulty stage. They should be close to those shown on the schematic diagram. If so, check the 4066B electronic switch and the capacitors at that stage. Otherwise, trace the stages with incorrect bias voltages back towards U28A.

Low-Pass Filter

Since the low-pass filter is designed to work with pulses rather than a steady signal, it's more practical to test this circuit with an actual RTTY signal. A convenient way to do this is to use the ASCII RTTY signal generated by the AFSK modulator. To do this, refer to "Analog Circuits Waveforms" in the next section.

WAVEFORMS

Overview

The following waveforms were measured with an ID-4850 Computer Oscilloscope under the noted conditions. Due to the random nature of some of the pulses and the sampling technique of the ID-4850, some of these waveforms will look different on a cathode ray tube oscilloscope. However, such things as general timing and rise/fall times should be the same.

Unless noted otherwise, the waveforms are usually shown with the synchronizing signal on top. They are grouped alphanumerically by the nonsynchronized signals (shown in bold face). To find a waveform, look up the bold face letter, then sync your scope to the one listed above it (if it's a dual-trace illustration).

Analog Circuits Waveforms

To get the following waveforms, perform the following:

-- Connect a jumper from J4-1 to J4-2.

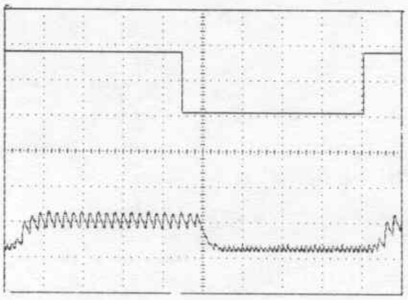
-- Put SW2 in the RADIO 1 position.

-- Turn on the HK-232 and enter * (asterisks) until you get the sign-on message.

-- Enter the following commands:

AS <RETURN>
WI ON <RETURN>
X <RETURN>

Repeatedly press **<RETURN>** to generate the signal.



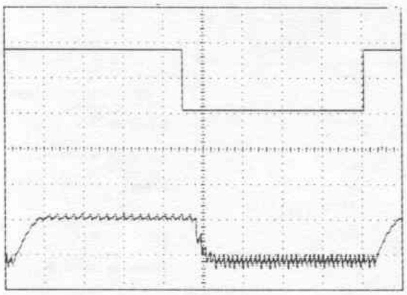
U6-27
(Synchronizing Signal)
V = 2.0 V/div
H = 2 mS/div

Baseline at division 5

D20 Cathode

V = 1.0 V/div
H = 2 mS/div

Baseline at division 2



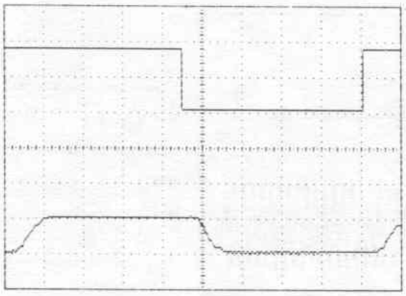
U6-27
(Synchronizing Signal)
V = 2.0 V/div
H = 2 mS/div

Baseline at division 5

D23 Anode

V = 1.0 V/div
H = 2 mS/div

Baseline at division 2



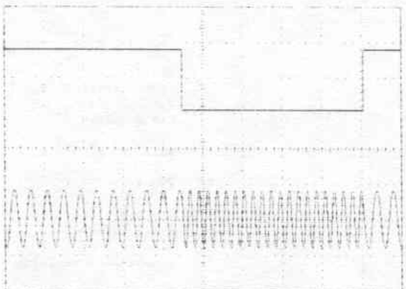
U6-27
(Synchronizing Signal)
V = 2.0 V/div
H = 2 mS/div

Baseline at division 5

J12-2

V = 1.0 V/div
H = 2 mS/div

Baseline at division 2



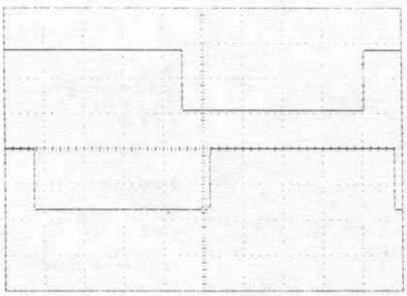
U6-27
(Synchronizing Signal)
V = 2.0 V/div
H = 2 mS/div

Baseline at division 5

TP-1

V = 1.0 V/div
H = 2 mS/div

Baseline at division 2



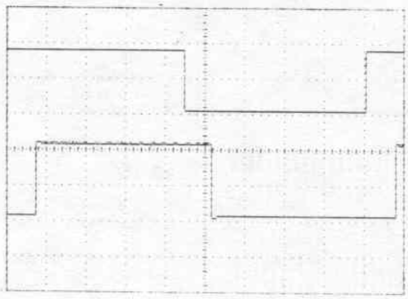
U6-27
(Synchronizing Signal)
V = 2.0 V/div
H = 2 mS/div

Baseline at division 5

U15-5

V = 2.0 V/div
H = 2 mS/div

Baseline at division 2



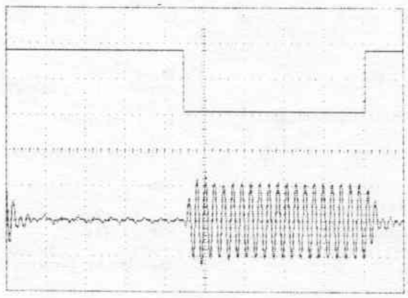
U6-27
(Synchronizing Signal)
V = 2.0 V/div
H = 2 mS/div

Baseline at division 5

U15-6

V = 2.0 V/div
H = 2 mS/div

Baseline at division 2



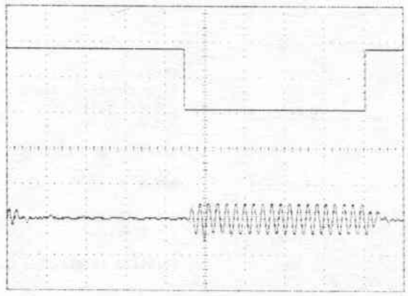
U6-27
(Synchronizing Signal)
V = 2.0 V/div
H = 2 mS/div

Baseline at division 5

U23-1

V = 1.0 V/div
H = 2 mS/div

Baseline at division 2



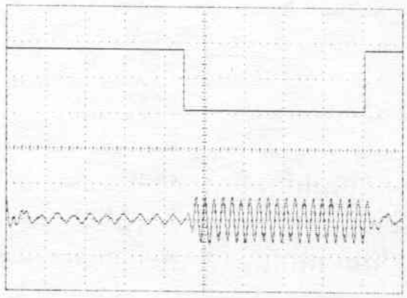
U6-27
(Synchronizing Signal)
V = 2.0 V/div
H = 2 mS/div

Baseline at division 5

U23-7

V = 1.0 V/div
H = 2 mS/div

Baseline at division 2



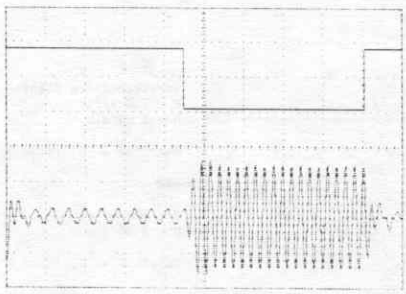
U6-27
(Synchronizing Signal)
V = 2.0 V/div
H = 2 mS/div

Baseline at division 5

U23-8

V = 1.0 V/div
H = 2 mS/div

Baseline at division 2



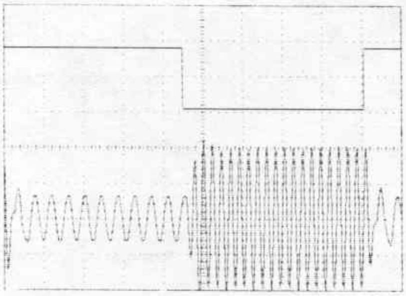
U6-27
(Synchronizing Signal)
V = 2.0 V/div
H = 2 mS/div

Baseline at division 5

U23-14

V = 1.0 V/div
H = 2 mS/div

Baseline at division 2



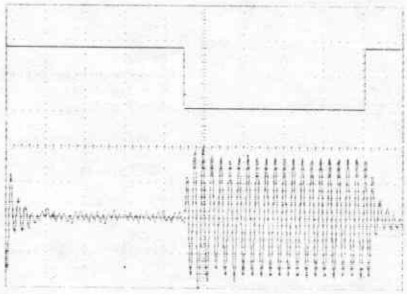
U6-27
(Synchronizing Signal)
V = 2.0 V/div
H = 2 mS/div

Baseline at division 5

U26-1

V = 1.0 V/div
H = 2 mS/div

Baseline at division 2



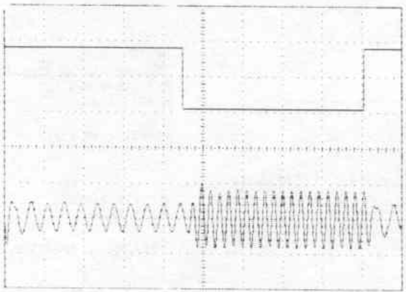
U6-27
(Synchronizing Signal)
V = 2.0 V/div
H = 2 mS/div

Baseline at division 5

U28-7

V = 500 mV/div
H = 2 mS/div

Baseline at division 2



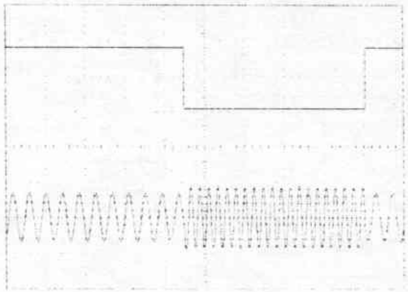
U6-27
(Synchronizing Signal)
V = 2.0 V/div
H = 2 mS/div

Baseline at division 5

U26-7

V = 1.0 V/div
H = 2 mS/div

Baseline at division 2



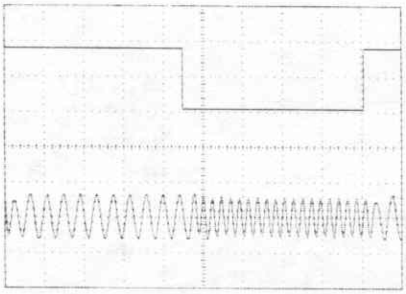
U6-27
(Synchronizing Signal)
V = 2.0 V/div
H = 2 mS/div

Baseline at division 5

U28-14

V = 500 mV/div
H = 2 mS/div

Baseline at division 2



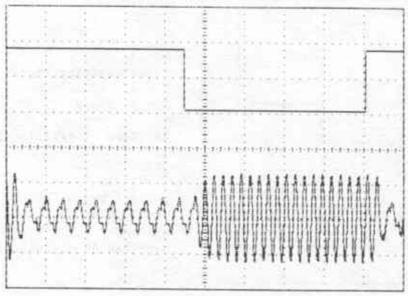
U6-27
(Synchronizing Signal)
V = 2.0 V/div
H = 2 mS/div

Baseline at division 5

U26-8

V = 2.0 V/div
H = 2 mS/div

Baseline at division 2



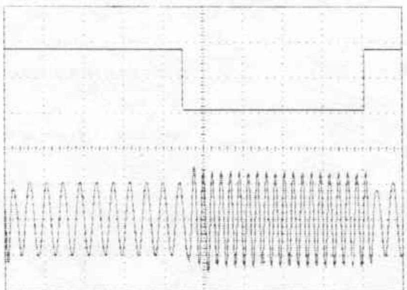
U6-27
(Synchronizing Signal)
V = 2.0 V/div
H = 2 mS/div

Baseline at division 5

U30-1

V = 2.0 V/div
H = 2 mS/div

Baseline at division 2



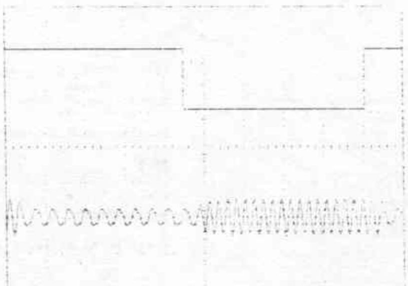
U6-27
(Synchronizing Signal)
V = 2.0 V/div
H = 2 mS/div

Baseline at division 5

U26-14

V = 2.0 V/div
H = 2 mS/div

Baseline at division 2



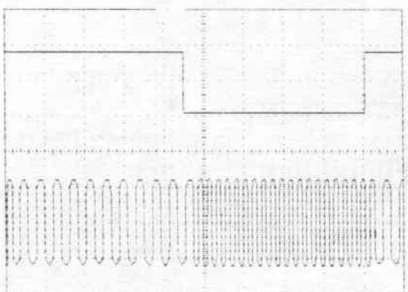
U6-27
(Synchronizing Signal)
V = 2.0 V/div
H = 2 mS/div

Baseline at division 5

U30-7

V = 2.0 V/div
H = 2 mS/div

Baseline at division 2



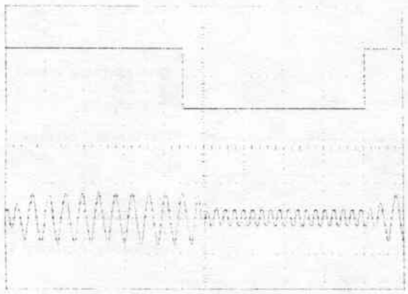
U6-27
(Synchronizing Signal)
V = 2.0 V/div
H = 2 mS/div

Baseline at division 5

U28-1

V = 500 mV/div
H = 2 mS/div

Baseline at division 2



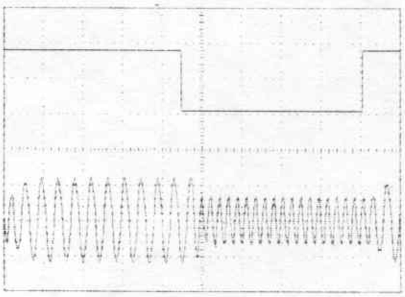
U6-27
(Synchronizing Signal)
V = 2.0 V/div
H = 2 mS/div

Baseline at division 5

U30-8

V = 2.0 V/div
H = 2 mS/div

Baseline at division 2



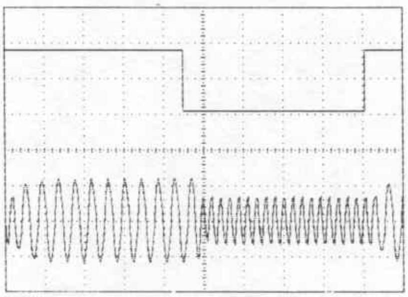
U6-27
(Synchronizing Signal)
V = 2.0 V/div
H = 2 mS/div

Baseline at division 5

U30-14

V = 2.0 V/div
H = 2 mS/div

Baseline at division 2



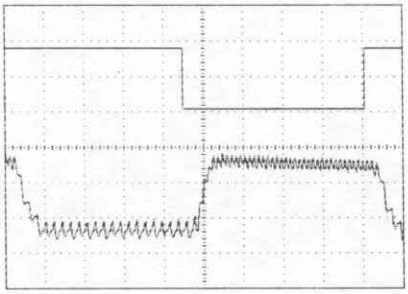
U6-27
(Synchronizing Signal)
V = 2.0 V/div
H = 2 mS/div

Baseline at division 5

U32-1

V = 2.0 V/div
H = 2 mS/div

Baseline at division 2



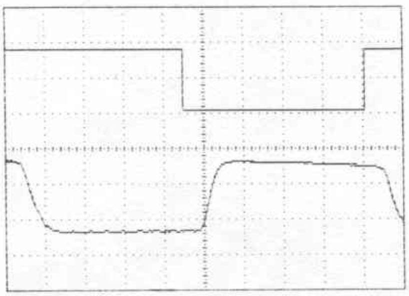
U6-27
(Synchronizing Signal)
V = 2.0 V/div
H = 2 mS/div

Baseline at division 5

U32-7

V = 1.0 V/div
H = 2 mS/div

Baseline at division 2



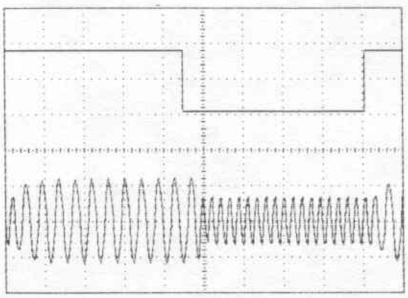
U6-27
(Synchronizing Signal)
V = 2.0 V/div
H = 2 mS/div

Baseline at division 5

U32-8

V = 1.0 V/div
H = 2 mS/div

Baseline at division 2



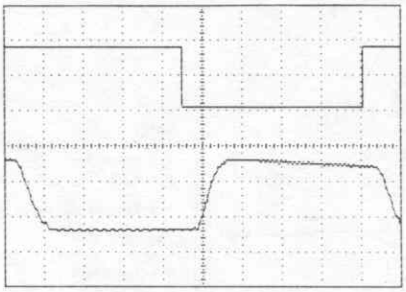
U6-27
(Synchronizing Signal)
V = 2.0 V/div
H = 2 mS/div

Baseline at division 5

U32-14

V = 2.0 V/div
H = 2 mS/div

Baseline at division 2



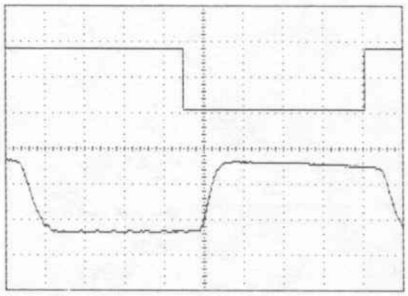
U6-27
(Synchronizing Signal)
V = 2.0 V/div
H = 2 mS/div

Baseline at division 5

U33-2

V = 1.0 V/div
H = 2 mS/div

Baseline at division 2



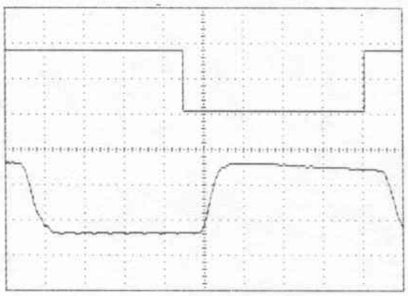
U6-27
(Synchronizing Signal)
V = 2.0 V/div
H = 2 mS/div

Baseline at division 5

U33-3

V = 1.0 V/div
H = 2 mS/div

Baseline at division 2



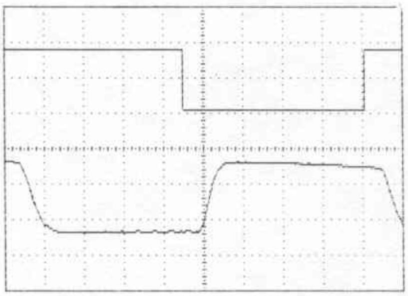
U6-27
(Synchronizing Signal)
V = 2.0 V/div
H = 2 mS/div

Baseline at division 5

U33-8

V = 1.0 V/div
H = 2 mS/div

Baseline at division 2



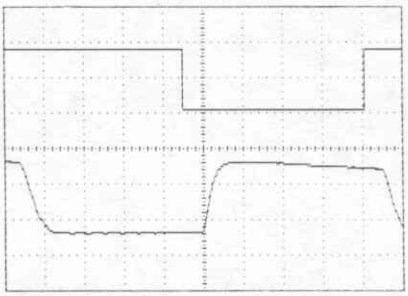
U6-27
(Synchronizing Signal)
V = 2.0 V/div
H = 2 mS/div

Baseline at division 5

U33-10

V = 1.0 V/div
H = 2 mS/div

Baseline at division 2



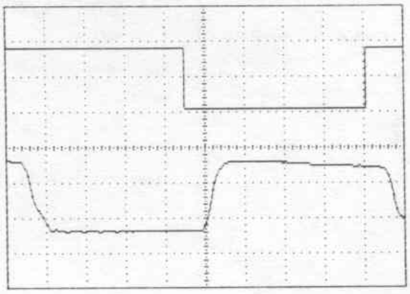
U6-27
(Synchronizing Signal)
V = 2.0 V/div
H = 2 mS/div

Baseline at division 5

U34-8

V = 1.0 V/div
H = 2 mS/div

Baseline at division 2



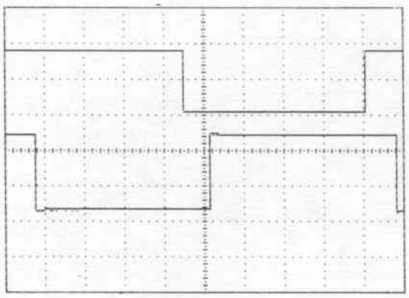
U6-27
(Synchronizing Signal)
V = 2.0 V/div
H = 2 mS/div

Baseline at division 5

U34-10

V = 1.0 V/div
H = 2 mS/div

Baseline at division 2



U6-27
(Synchronizing Signal)
V = 2.0 V/div
H = 2 mS/div

Baseline at division 5

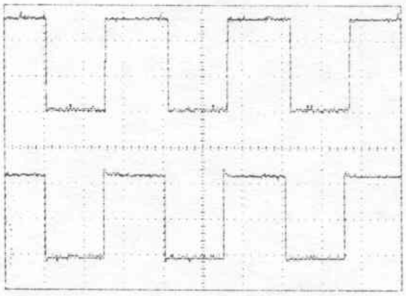
U34-14

V = 5 V/div
H = 2 mS/div

Baseline at division 2

Clock and Power Supply Waveforms

The following waveforms were measured with the battery backup and all peripherals disconnected.



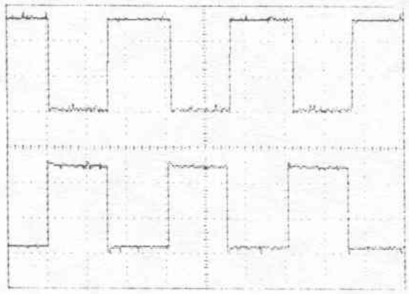
U13-1
(Synchronizing Signal)
V = 5 V/div
H = 50 uS/div

Baseline at division 5

D6 Anode

V = 5 V/div
H = 50 uS/div

Baseline at division 3



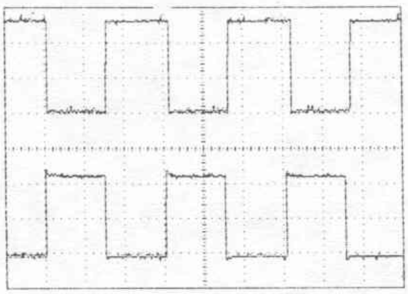
U13-1
(Synchronizing Signal)
V = 5 V/div
H = 50 uS/div

Baseline at division 5

U13-9

V = 5 V/div
H = 50 uS/div

Baseline at division 1



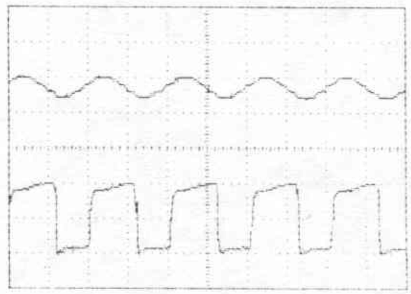
U13-1
(Synchronizing Signal)
V = 5 V/div
H = 50 uS/div

Baseline at division 5

D8 Anode

V = 5 V/div
H = 50 uS/div

Baseline at division 3



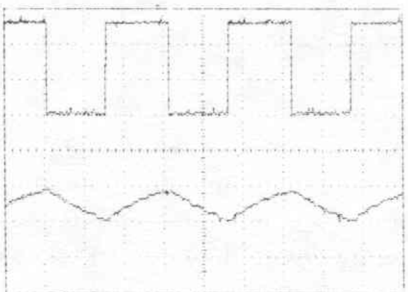
U15-9
(Synchronizing Signal)
V = 2.0 V/div
H = 200 nS/div

Baseline at division 5

U15-4

V = 2.0 V/div
H = 200 nS/div

Baseline at division 1



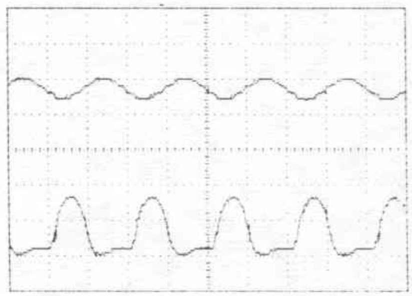
U13-1
(Synchronizing Signal)
V = 5 V/div
H = 50 uS/div

Baseline at division 5

U13-2

V = 5 V/div
H = 50 uS/div

Baseline at division 1



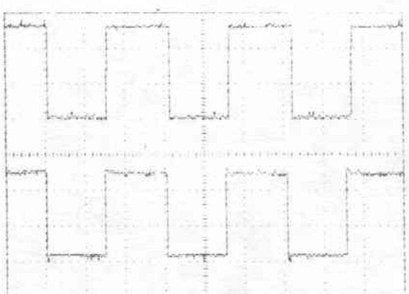
U15-9
(Synchronizing Signal)
V = 2.0 V/div
H = 200 nS/div

Baseline at division 5

U15-8

V = 2.0 V/div
H = 200 nS/div

Baseline at division 1



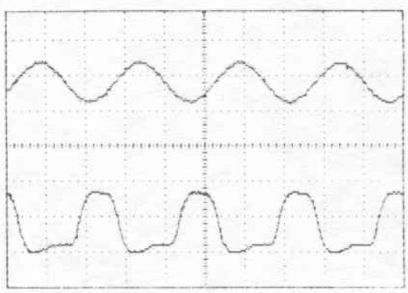
U13-1
(Synchronizing Signal)
V = 5 V/div
H = 50 uS/div

Baseline at division 5

U13-5

V = 5 V/div
H = 50 uS/div

Baseline at division 1



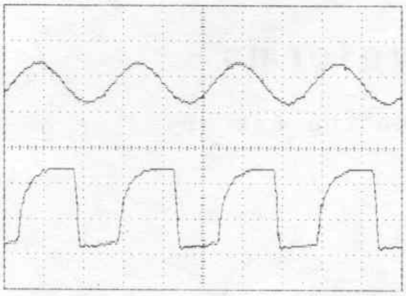
U15-11
(Synchronizing Signal)
V = 2.0 V/div
H = 100 nS/div

Baseline at division 5

U15-10

V = 2.0 V/div
H = 100 nS/div

Baseline at division 1



U15-11
(Synchronizing Signal)
V = 2.0 V/div
H = 100 nS/div

Baseline at division 5

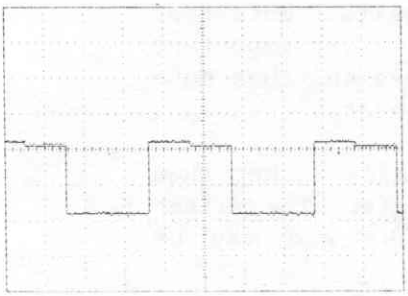
U15-12

V = 2.0 V/div
H = 100 nS/div

Baseline at division 1

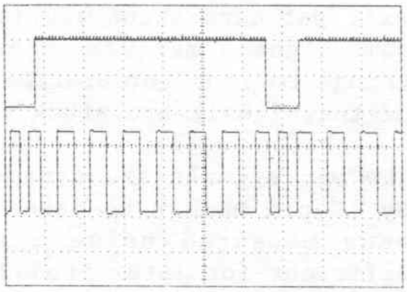
HDLC Waveforms

The following waveforms were measured with the battery backup and all peripherals disconnected.



U7-12
(Synchronizing Signal)
V = 2.0 V/div
H = 200 uS/div

Baseline at division 2



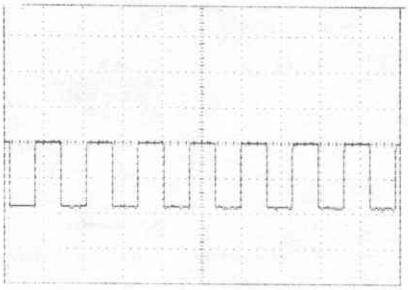
U7-15
(Synchronizing Signal)
V = 2.0 V/div
H = 1 mS/div

Baseline at division 5

U40-11

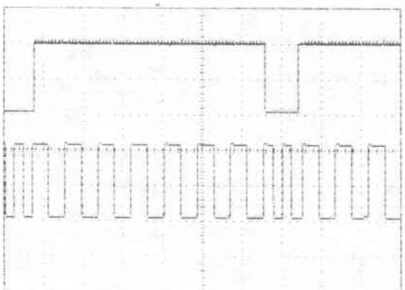
V = 2.0 V/div
H = 1 mS/div

Baseline at division 2



U7-14
(Synchronizing Signal)
V = 2.0 V/div
H = 20 uS/div

Baseline at division 2



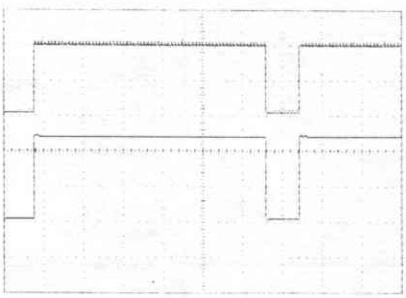
U7-15
(Synchronizing Signal)
V = 2.0 V/div
H = 1 mS/div

Baseline at division 5

U39-4

V = 2.0 V/div
H = 1 mS/div

Baseline at division 2



U7-15
(Synchronizing Signal)
V = 2.0 V/div
H = 1 mS/div

Baseline at division 5

U40-9

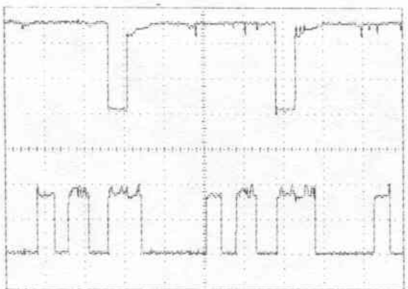
V = 2.0 V/div
H = 1 mS/div

Baseline at division 2

Logic Circuits Waveforms

The following waveforms were measured with the battery backup and all peripherals disconnected. The CPU is in a loop that constantly polls a location in U4 while it's waiting for asterisks from the RS-232C port. By synchronizing the oscilloscope to U4's chip-select line, you will get consistent waveforms when U4-20 asserts. Note that some signals may vary when this line is high. The important things to look for are the rise and fall times and that none of the signals are stuck in an intermediate state.

The bus signals are arranged by their mnemonics rather than by IC pin number to make them easier to locate. The pulses were measured using first-production ROMs and may be different for later productions.



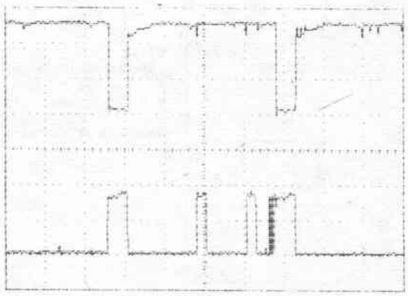
$\overline{\text{CS1}}$ U4-20
(Synchronizing Signal)
V = 2.0 V/div
H = 2 uS/div

Baseline at division 5

A0 U4-10

V = 2.0 V/div
H = 2 uS/div

Baseline at division 1



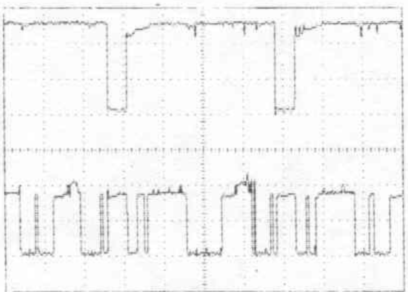
$\overline{\text{CS1}}$ U4-20
(Synchronizing Signal)
V = 2.0 V/div
H = 2 uS/div

Baseline at division 5

A3 U4-7

V = 2.0 V/div
H = 2 uS/div

Baseline at division 1



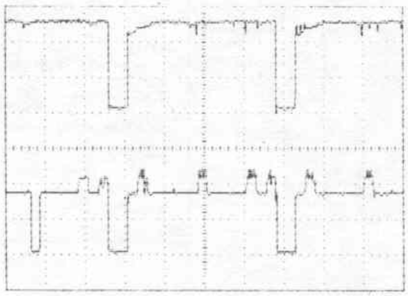
$\overline{\text{CS1}}$ U4-20
(Synchronizing Signal)
V = 2.0 V/div
H = 2 uS/div

Baseline at division 5

A1 U4-9

V = 2.0 V/div
H = 2 uS/div

Baseline at division 1



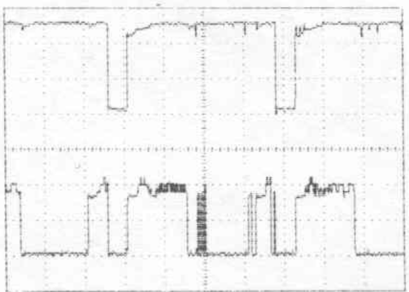
$\overline{\text{CS1}}$ U4-20
(Synchronizing Signal)
V = 2.0 V/div
H = 2 uS/div

Baseline at division 5

A4 U4-6

V = 2.0 V/div
H = 2 uS/div

Baseline at division 1



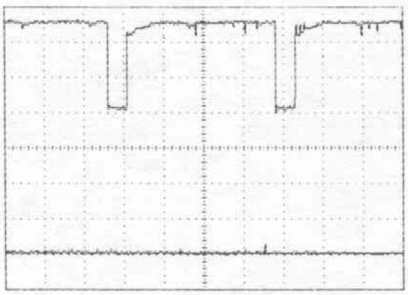
$\overline{\text{CS1}}$ U4-20
(Synchronizing Signal)
V = 2.0 V/div
H = 2 uS/div

Baseline at division 5

A2 U4-8

V = 2.0 V/div
H = 2 uS/div

Baseline at division 1



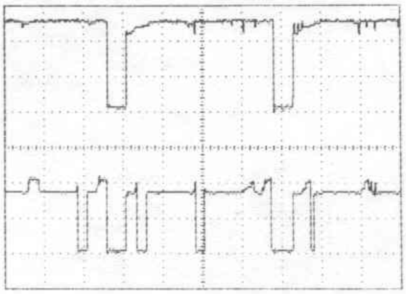
$\overline{\text{CS1}}$ U4-20
(Synchronizing Signal)
V = 2.0 V/div
H = 2 uS/div

Baseline at division 5

A5 U4-5

V = 2.0 V/div
H = 2 uS/div

Baseline at division 1



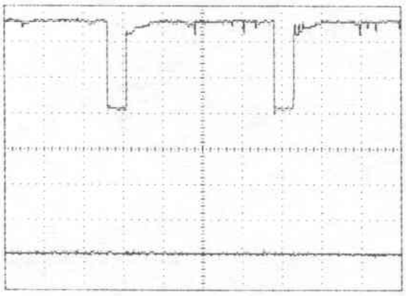
$\overline{CS1}$ U4-20
(Synchronizing Signal)
V = 2.0 V/div
H = 2 uS/div

Baseline at division 5

A6 U4-4

V = 2.0 V/div
H = 2 uS/div

Baseline at division 1



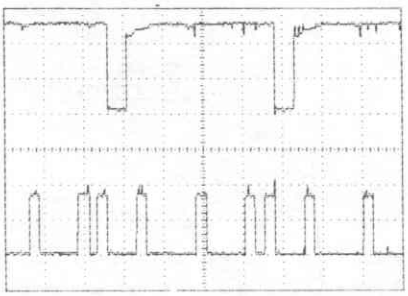
$\overline{CS1}$ U4-20
(Synchronizing Signal)
V = 2.0 V/div
H = 2 uS/div

Baseline at division 5

A7 U4-3

V = 2.0 V/div
H = 2 uS/div

Baseline at division 1



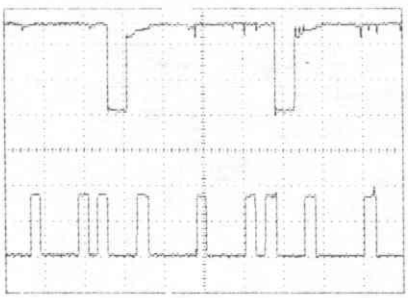
$\overline{CS1}$ U4-20
(Synchronizing Signal)
V = 2.0 V/div
H = 2 uS/div

Baseline at division 5

A8 U4-25

V = 2.0 V/div
H = 2 uS/div

Baseline at division 1



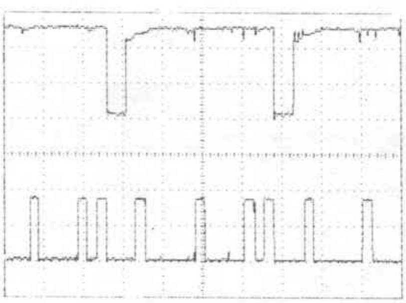
$\overline{CS1}$ U4-20
(Synchronizing Signal)
V = 2.0 V/div
H = 2 uS/div

Baseline at division 5

A9 U4-24

V = 2.0 V/div
H = 2 uS/div

Baseline at division 1



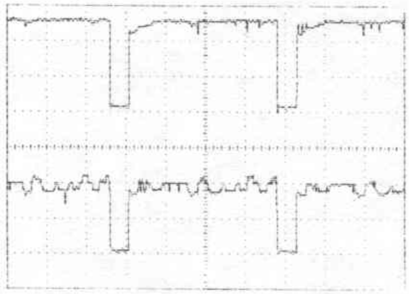
$\overline{CS1}$ U4-20
(Synchronizing Signal)
V = 2.0 V/div
H = 2 uS/div

Baseline at division 5

A10 U4-21

V = 2.0 V/div
H = 2 uS/div

Baseline at division 1



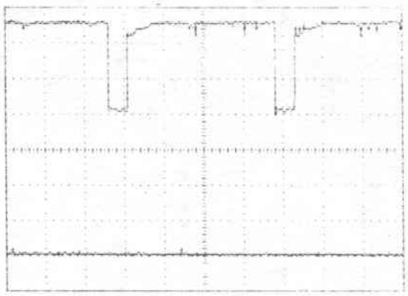
$\overline{CS1}$ U4-20
(Synchronizing Signal)
V = 2.0 V/div
H = 2 uS/div

Baseline at division 5

A11 U4-23

V = 2.0 V/div
H = 2 uS/div

Baseline at division 1



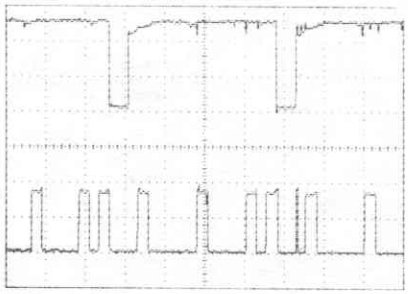
$\overline{CS1}$ U4-20
(Synchronizing Signal)
V = 2.0 V/div
H = 2 uS/div

Baseline at division 5

A12 U4-2

V = 2.0 V/div
H = 2 uS/div

Baseline at division 1



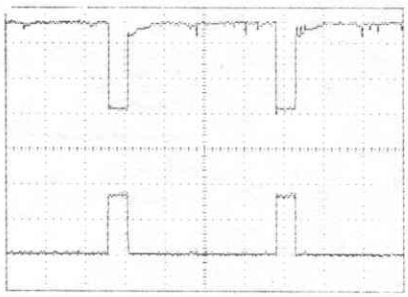
$\overline{CS1}$ U4-20
(Synchronizing Signal)
V = 2.0 V/div
H = 2 uS/div

Baseline at division 5

A13 U1-3

V = 2.0 V/div
H = 2 uS/div

Baseline at division 1



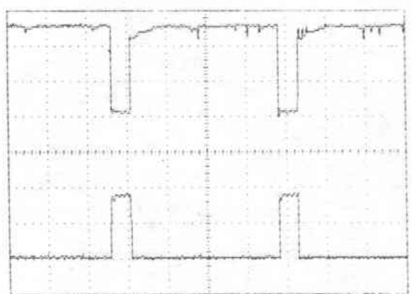
$\overline{CS1}$ U4-20
(Synchronizing Signal)
V = 2.0 V/div
H = 2 uS/div

Baseline at division 5

A14 U1-4

V = 2.0 V/div
H = 2 uS/div

Baseline at division 1



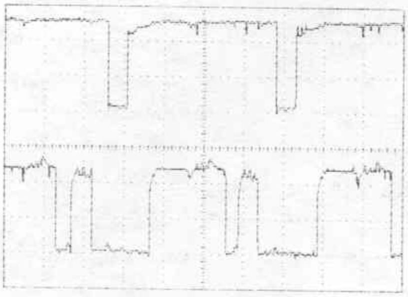
$\overline{CS1}$ U4-20
(Synchronizing Signal)
V = 2.0 V/div
H = 2 uS/div

Baseline at division 5

A15 U1-5

V = 2.0 V/div
H = 2 uS/div

Baseline at division 1



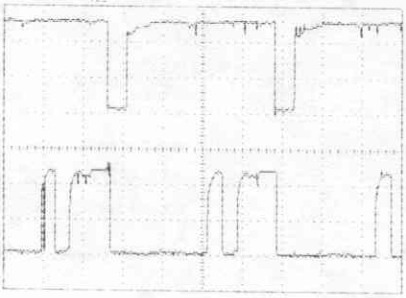
$\overline{\text{CST}}$ U4-20
(Synchronizing Signal)
V = 2.0 V/div
H = 2 uS/div

Baseline at division 5

D0 U4-11

V = 2.0 V/div
H = 2 uS/div

Baseline at division 1



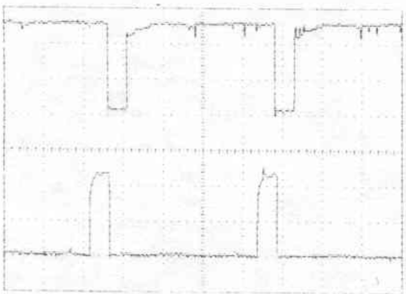
$\overline{\text{CST}}$ U4-20
(Synchronizing Signal)
V = 2.0 V/div
H = 2 uS/div

Baseline at division 5

D1 U4-12

V = 2.0 V/div
H = 2 uS/div

Baseline at division 1



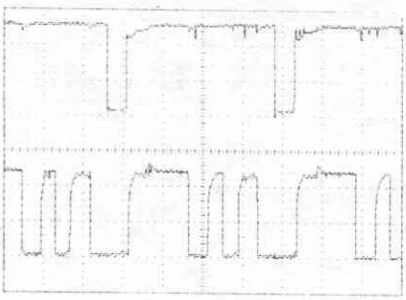
$\overline{\text{CST}}$ U4-20
(Synchronizing Signal)
V = 2.0 V/div
H = 2 uS/div

Baseline at division 5

D2 U4-13

V = 2.0 V/div
H = 2 uS/div

Baseline at division 1



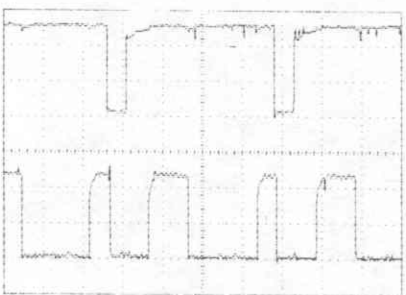
$\overline{\text{CST}}$ U4-20
(Synchronizing Signal)
V = 2.0 V/div
H = 2 uS/div

Baseline at division 5

D3 U4-15

V = 2.0 V/div
H = 2 uS/div

Baseline at division 1



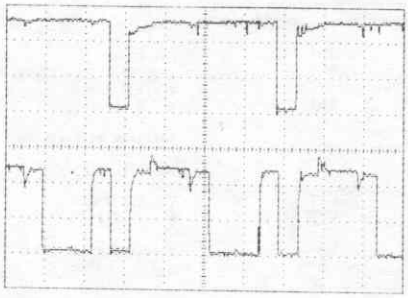
$\overline{\text{CST}}$ U4-20
(Synchronizing Signal)
V = 2.0 V/div
H = 2 uS/div

Baseline at division 5

D4 U4-16

V = 2.0 V/div
H = 2 uS/div

Baseline at division 1



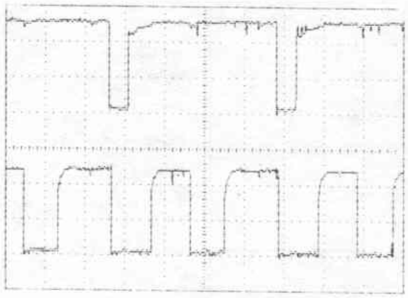
$\overline{\text{CST}}$ U4-20
(Synchronizing Signal)
V = 2.0 V/div
H = 2 uS/div

Baseline at division 5

D5 U4-17

V = 2.0 V/div
H = 2 uS/div

Baseline at division 1



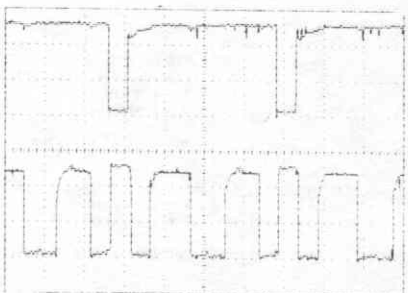
$\overline{\text{CST}}$ U4-20
(Synchronizing Signal)
V = 2.0 V/div
H = 2 uS/div

Baseline at division 5

D6 U4-18

V = 2.0 V/div
H = 2 uS/div

Baseline at division 1



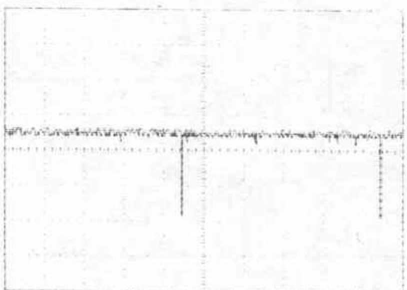
$\overline{\text{CST}}$ U4-20
(Synchronizing Signal)
V = 2.0 V/div
H = 2 uS/div

Baseline at division 5

D7 U4-19

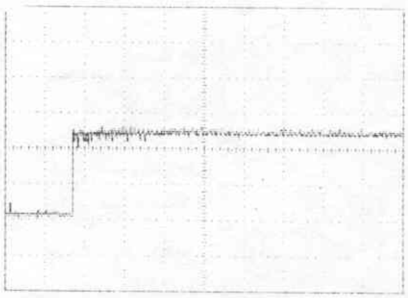
V = 2.0 V/div
H = 2 uS/div

Baseline at division 1



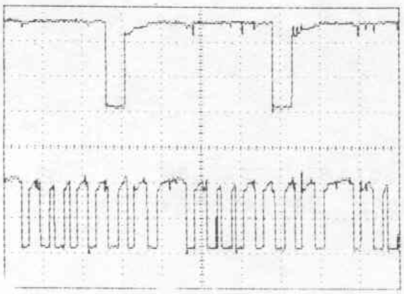
INT U1-16
(Synchronizing Signal)
V = 2.0 V/div
H = 200 uS/div

Baseline at division 2



INT U1-16
(Synchronizing Signal)
V = 2.0 V/div
H = 1 uS/div

Baseline at division 2



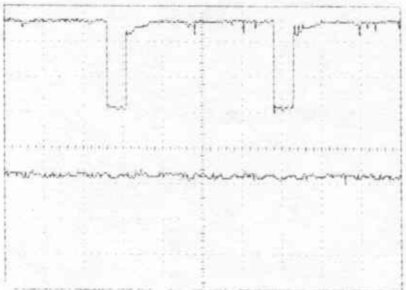
$\overline{\text{CS1}}$ U4-20
(Synchronizing Signal)
V = 2.0 V/div
H = 2 uS/div

Baseline at division 5

$\overline{\text{OE}}$ U4-22

V = 2.0 V/div
H = 2 uS/div

Baseline at division 1



$\overline{\text{CS1}}$ U4-20
(Synchronizing Signal)
V = 2.0 V/div
H = 2 uS/div

Baseline at division 5

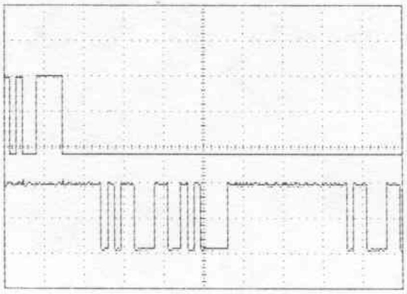
$\overline{\text{WE}}$ U4-27

V = 2.0 V/div
H = 2 uS/div

Baseline at division 1

RS-232C Waveforms

Connect a computer or terminal to the HK-232 serial port and enter asterisks until you get the "cmd:" prompt. Repeatedly press **<RETURN>** to get the following waveforms.



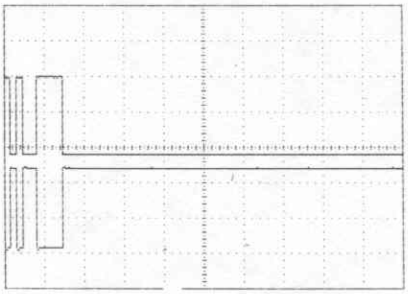
U19-1
(Synchronizing Signal)
V = 10 V/div
H = 5 mS/div

Baseline at division 5

U7-25

V = 2.0 V/div
H = 5 mS/div

Baseline at division 1



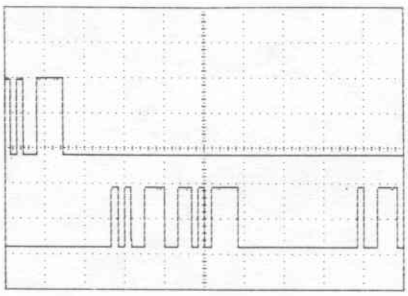
U19-1
(Synchronizing Signal)
V = 10 V/div
H = 5 mS/div

Baseline at division 5

U7-27

V = 2.0 V/div
H = 5 mS/div

Baseline at division 1



U19-1
(Synchronizing Signal)
V = 10 V/div
H = 5 mS/div

Baseline at division 5

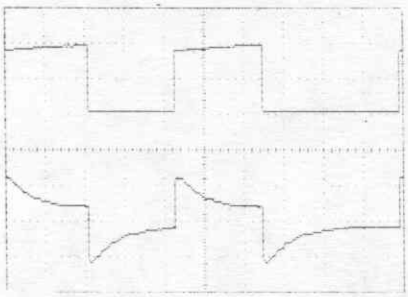
U20-6

V = 10 V/div
H = 5 mS/div

Baseline at division 2

Watchdog Timer Waveforms

To get the following waveforms, enter * (asterisks) until you get the "cmd:" prompt.



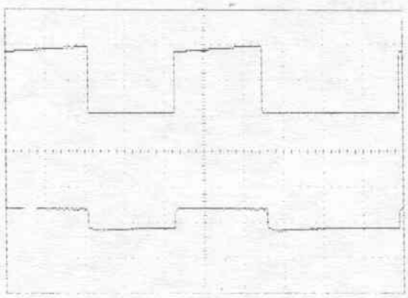
U7-16
(Synchronizing Signal)
V = 2.0 V/div
H = 1 mS/div

Baseline at division 5

C66/R180 Junction

V = 2.0 V/div
H = 1 mS/div

Baseline at division 2



U7-16
(Synchronizing Signal)
V = 2.0 V/div
H = 1 mS/div

Baseline at division 5

D33 Cathode

V = 2.0 V/div
H = 1 mS/div

Baseline at division 2

FINAL CHECKS

Before you start to use the HK-232 again, perform the following checks to be sure it's working properly. Be sure that:

-- All the hardware is installed and tightened.

-- The circuit boards are securly installed.

-- The unit is properly configured and aligned.

-- The unit powers up properly.

-- The power supply voltages are correct.

-- The RS-232C serial port and printer port function properly.

To test, type **PRO ON <RETURN> PRC ON <RETURN>** at the "cmd:" prompt. At the first command, the CRT will display:

PROUT was OFF
PROUT now ON

At the second command, the printer will print:

PRCON was OFF
PRCON now ON

As you type characters on the keyboard, the CRT will remain inactive and the front panel LEDs will flash as U6 sends the data to the printer. Some printers, such as the Epson LX-80, won't print the line until you hit the Return key (or until its buffer fills).

Exit the print mode by typing **PRC OFF <RETURN>.**

-- All LEDs function properly.

-- The unit sends and receives properly.

To test, turn the THRESHOLD knob CW until the DCD LED lights, then adjust it CCW until the light just goes out. Next, connect a jumper from J4-1 to J4-2 and enter the following commands:

MY XYZZY <RETURN>
CON XYZZY <RETURN>

When you type a line and press the Return key, the TUNE indicator should show marks and spaces, the DCD LED should light, and the data that you entered should be echoed to the display.

-- When sending packets, you should see sinusoidal waveforms at pins 3 and 5 of J7 and pulses at pins 1 and 4 of J7.

-- The squelch circuit functions properly.

While still in the packet conversation mode, test the squelch circuit by connecting a positive voltage (5 to 13 volts) to pin 3 of the RADIO 1 connector. Type a line of text and press **<RETURN>**. The HK-232 should respond by lighting the STA LED. The TUNE LED will remain centered, indicating that the packet wasn't sent. When you remove the positive voltage from pin 3, the STA LED will turn off, the HK-232 will send the packet, the TUNE LED will indicate marks and spaces, and the computer will echo the line you typed.

Exit the packet mode by typing **CTRL-C DISC <RETURN>**.

-- The PTT and CW keyer circuits function properly.

To test, type the following commands:

MO <RETURN>
X <RETURN>

The PTT line should go to ground if jumpered for positive, or to +1.6 V if jumpered for negative. When you press a keyboard key, the +KEY output will pulse to gound and the -KEY output to +0.6 V. Exit the Morse code mode by typing **CTRL-D**.

-- The unit runs for an hour without thermal or intermittent problems.

If the unit has had a thermal or intermittent problem (or you suspect one), let the unit run overnight. Perform the final checks again in the morning.

PARTS LISTS

PARTS LISTS

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CIRCUIT Comp. No.	DESCRIPTION	HEATH Part No.
CABLES		
	Power	230-8154
	RS-232C/FAX	230-8157
	RX-IN, 2-wire with miniature phone plugs	230-8156
	Radio interface	230-8155
HARDWARE		
	Lockwasher, control	254-5
	Nut, control	252-773
	Screw, 6-32 x 1/2"	250-1425
	Screw, 6-32 x 1/4"	250-1325
	Setscrew, 6-32 x 1/8"	250-1282
	Washer, #6 flat	253-60
	Washer, control flat	253-10
SOCKETS-CONNECTORS		
	DIN, 5-pin	230-8157
	Shell, 4-hole	432-1151
	Spring contact, Molex	432-866

POWER CUBE

This component is not supplied with the HK-232 kit. It must be purchased separately.

CIRCUIT Comp. No.	DESCRIPTION	HEATH Part No.
	120 VAC input; 12 VDC, 1 A output	150-333

CIRCUIT Comp. No.	DESCRIPTION	HEATH Part No.
MISCELLANEOUS		
	Battery holder	230-8158
	Cabinet bottom	200-1554-1
	Cabinet top	90-1394-1
	Fuse label	390-1255
	Knob	462-1248
	Plug, phono	438-4
	Tape, double-stick foam, battery holder mounting	73-92
	Tape, double-stick insulator, TUNE window mounting	73-151
	Window	446-761

DISPLAY CIRCUIT BOARD

CIRCUIT Comp. No.	DESCRIPTION	HEATH Part No.
CAPACITOR		
C1-C87	On main board.	
C88	.0056 uF (562K) Mylar®	27-147
LEDS		
DS1	SLP151B, red	412-646
DS2	SLP151B, red	412-646
DS3	SLP151B, red	412-646
DS4	SLP151B, red	412-646
DS5	SLP151B, red	412-646
DS6	SLP151B, red	412-646
DS7	SLP151B, red	412-646
DS8	SLP151B, red	412-646
DS9	SLP151B, red	412-646
DS10	SLP151B, red	412-646
DS11	SLP151B, red	412-646
DS12	SLP151B, red	412-646
DS13	SLP151B, red	412-646
DS14	SLP151B, red	412-646
DS15	SLP151B, red	412-646
DS16	SLP151B, red	412-646
DS17	SLP151B, red	412-646
DS18	SLP151B, red	412-646
DS19	SLP151B, red	412-646
DS20	SLP151B, red	412-646
DS21	RBG-1000, 10-segment bar graph	230-8096
PLUGS		
J1-J10	On main board.	
J11	14-pin right-angle	230-8131
J12	6-pin right-angle	230-8129
RESISTORS		
R1-R12	On main board.	
R13	330 ohms, 5%, 1/4 W	6-331-12
R14	330 ohms, 5%, 1/4 W	6-331-12
R15	330 ohms, 5%, 1/4 W	6-331-12
R16	330 ohms, 5%, 1/4 W	6-331-12
R17	330 ohms, 5%, 1/4 W	6-331-12
R18	330 ohms, 5%, 1/4 W	6-331-12
R19-R136	On main board.	
R137	1.78 kilohms, 1%, 1/4 W	6-1781-12
R138	1.10 kilohms, 1%, 1/4 W	6-1101-12
R139	3.74 kilohms, 1%, 1/4 W	6-3741-12
R140	1.0 kilohm, 5%, 1/4 W	6-102-12

CIRCUIT Comp. No.	DESCRIPTION	HEATH Part No.
INTEGRATED CIRCUITS		
U1-U10	On main board.	
U11	7445	230-8114
U12	7445	230-8114
U13-U35	On main board.	
U36	LM3914	442-798
MANUALS AND BINDERS		
	3-ring assembly, 1/2"	701-233
	3-ring assembly, 1"	701-234
	Binder cover for 1/2" ring assembly	597-4460
	Binder cover for 1" ring assembly	597-4464
	Manual, Assembly	595-3901
	Manual, User	595-3902
	Nut, 6-32 X 1/4"	252-3
	Parts order form	597-260
	Screw, 3/8" nylon	250-357
	Washer, #8 flat	253-14
SOCKETS		
	16-pin IC	434-299
	18-pin IC	434-310
	20-pin IC	434-311
MISCELLANEOUS		
	Circuit board, display	230-8002
	Desoldering braid	490-185

MAIN CIRCUIT BOARD

CIRCUIT Comp. No.	DESCRIPTION	HEATH Part No.
CAPACITORS		
C1	100 uF electrolytic	25-885
C2	220 pF mica	20-120
C3	.01 uF (103), 50 V ceramic	21-769
C4	.01 uF (103), 50 V ceramic	21-769
C5	330 pF mica	20-139
C6	33 pF mica	230-8024
C7	.01 uF (103), 50 V ceramic	21-769
C8	.01 uF (103), 50 V ceramic	21-769
C9	820 pF mica	20-171
C10	680 pF mica	20-107
C11	.001 uF (102) ceramic	21-784
C12	.001 uF (102) ceramic	21-784
C13	.001 uF (102) ceramic	21-784
C14	.001 uF (102) ceramic	21-784
C15	.001 uF (102) ceramic	21-784
C16	.001 uF (102) ceramic	21-784
C17	47 uF electrolytic	25-915
C18	.1 uF (104), 10% Mylar R	230-8004
C19	.001 uF (102) ceramic	21-784
C20	.01 uF (103), 10% Mylar R	230-8003
C21	.01 uF (103), 10% Mylar R	230-8003
C22	10 uF electrolytic	25-917
C23	10 uF electrolytic	25-917
C24	10 uF electrolytic	25-917
C25	10 uF electrolytic	25-917
C26	1000 uF electrolytic	27-876
C27	.1 uF (104) ceramic	21-786
C28	100 uF electrolytic	25-885
C29	47 uF electrolytic	25-915
C30	.01 uF (103) polypropylene	27-822
C31	.01 uF (103) polypropylene	27-822
C32	.01 uF (103) polypropylene	27-822
C33	.01 uF (103) polypropylene	27-822
C34	.01 uF (103) polypropylene	27-822
C35	.01 uF (103) polypropylene	27-822
C36	.01 uF (103) polypropylene	27-822
C37	.01 uF (103) polypropylene	27-822
C38	.01 uF (103) polypropylene	27-822
C39	.01 uF (103) polypropylene	27-822
C40	10 uF electrolytic	25-917
C41	.1 uF (104), 10% Mylar R	230-8004
C42	.01 uF (103) polypropylene	27-822
C43	.01 uF (103) polypropylene	27-822
C44	10 uF electrolytic	25-917
C45	.1 uF (104), 10% Mylar R	230-8004
C46	.047 uF (473J), 2% Mylar R	27-129
C47	.1 uF (104), 5% Mylar R	27-77
C48	.0047 uF polypropylene	230-8021
C49	.1 uF (104), 5% Mylar R	27-77
Capacitors (continued)		
C50	1200 pF (122) Mylar R	230-8009
C51	3.3 uF electrolytic	25-912
C52	47 uF electrolytic	25-915
C53	5-40 pF trimmer	230-8015
C54	.01 uF (103), 5% Mylar R	27-161
C55	10 uF electrolytic	25-917
C56	10 uF electrolytic	25-917
C57	10 uF electrolytic	25-917
C58	.022 uF (233) ceramic	230-8011
C59	10 uF electrolytic	25-917
C60	10 uF electrolytic	25-917
C61	.01 uF, 500V ceramic	21-16
C62	.01 uF, 500V ceramic	21-16
C63	.01 uF (103), 50V ceramic	21-769
C64	.01 uF (103), 50V ceramic	21-769
C65	10 uF electrolytic	25-917
C66	.1 uF (104) ceramic	21-786
C67	10 uF electrolytic	25-917
C68	.1 uF (104) ceramic	21-786
C69	.1 uF (104) ceramic	21-786
C70	.1 uF (104) ceramic	21-786
C71	.1 uF (104) ceramic	21-786
C72	.1 uF (104) ceramic	21-786
C73	.1 uF (104) ceramic	21-786
C74	.1 uF (104) ceramic	21-786
C75	.1 uF (104) ceramic	21-786
C76	.1 uF (104) ceramic	21-786
C77	.1 uF (104) ceramic	21-786
C78	.1 uF (104) ceramic	21-786
C79	.1 uF (104) ceramic	21-786
C80	.1 uF (104) ceramic	21-786
C81	.1 uF (104) ceramic	21-786
C82	.1 uF (104) ceramic	21-786
C83	.1 uF (104) ceramic	21-786
C84	.1 uF (104) ceramic	21-786
C85	.1 uF (104) ceramic	21-786
C86	.1 uF (104) ceramic	21-786
C87	.1 uF (104) ceramic	21-786
C88	On display board.	
C89	.047 uF (473K), 10% Mylar R	230-8005

CIRCUIT Comp. No.	DESCRIPTION	HEATH Part No.
DIODES		
D1	1N4448	56-652
D2	1N4448	56-652
D3	1N4448	56-652
D4	1N4448	56-652
D5	1N4448	56-652
D6	1N4448	56-652
D7	1N4448	56-652
D8	1N4448	56-652
D9	1N4448	56-652
D10	1N5397	57-27
D11	1N5397	57-27
D12	1N5397	57-27
D13	1N4448	56-652
D14	1N4448	56-652
D15	1N4448	56-652
D16	1N4448	56-652
D17	1N4448	56-652
D18	1N4448	56-652
D19	1N4448	56-652
D20	1N4448	56-652
D21	1N4448	56-652
D22	1N4448	56-652
D23	1N4448	56-652
D24	1N4448	56-652
D25	1N4448	56-652
D26	1N4448	56-652
D27	1N5231 5.1V zener	56-16
D28	1N4448	56-652
D29	1N5397	57-27
D30	1N5397	57-27
D31	1N5397	57-27
D32	1N5397	57-27
D33	1N4448	56-652
LED		
DS1-DS21	On display board.	
DS22	SLP151B, red	412-646
FUSE		
F1	1-ampere, regular blow	230-8152 or 421-37

CIRCUIT Comp. No.	DESCRIPTION	HEATH Part No.
CONNECTORS		
	4-pin, battery backup	432-1129
J1	DC Power	230-8135
J2	25-pin DCE, RS-232C	432-1382
J3	Miniature phone, AUDIO 1	230-8136
J4	5-pin right-angle, RADIO 1	432-1106
J5	Miniature phone, AUDIO 2	230-8136
J6	5-pin right-angle, RADIO 2	432-1106
J7	5-pin DIN, SCOPE/FSK	432-1495
J8	5-pin right-angle, EXT MODEM	432-1106
J9	Phono, +KEY OUT (on #230-8001 main board)	230-8137
J9	Phono, +KEY OUT (on #230-8163 main board)	230-8162
J10	Phono, -KEY OUT (on #230-8001 main board)	230-8137
J10	Phono, -KEY OUT (on #230-8163 main board)	230-8162
JUMPER SOCKET AND PLUGS		
	Socket, jumper, 2F, Berg	432-1041
JP1	Plug, 2-pin	432-1309
JP2	Plug, 3-pin	432-1310
JP3	Plug, 3-pin	432-1310
TRANSISTORS		
Q1	VN10LM	230-8101
Q2	VN10LM	230-8101
Q3	MPS6521	417-172
Q4	2N3906	417-874
Q5	MPS6561	230-8100
Q6	2N3904	417-875
Q7	2N3904	417-875
Q8	MPSA42	417-294
Q9	2N3906	417-874
Q10	2N3904	417-875
Q11	2N3904	417-875

CIRCUIT Comp. No.	DESCRIPTION	HEATH Part No.
RESISTORS		
R1	4.7 kilohms, 5%, 1/4 W	6-472-12
R2	4.7 kilohms, 5%, 1/4 W	6-472-12
R3	1.0 kilohm, 5%, 1/4 W	6-102-12
R4	1.0 kilohm, 5%, 1/4 W	6-102-12
R5	1.0 kilohm, 5%, 1/4 W	6-102-12
R6	330 ohms, 5%, 1/4 W	6-331-12
R7	10 kilohms, 5%, 1/4 W	6-103-12
R8	10 kilohms, 5%, 1/4 W	6-103-12
R9	5.1 kilohms, 5%, 1/4 W	6-512-12
R10	5.1 kilohms, 5%, 1/4 W	6-512-12
R11	10 kilohms, 5%, 1/4 W	6-103-12
R12	10 kilohms, 5%, 1/4 W	6-103-12
R13-R18	On display board.	
R19	1.0 kilohm, 5%, 1/4 W	6-102-12
R20	1.0 kilohm, 5%, 1/4 W	6-102-12
R21	100 ohms, 5%, 1/4 W	6-101-12
R22	100 ohms, 5%, 1/4 W	6-101-12
R23	100 ohms, 5%, 1/4 W	6-101-12
R24	100 ohms, 5%, 1/4 W	6-101-12
R25	4.7 kilohms, 5%, 1/4 W	6-472-12
R26	100 ohms, 5%, 1/4 W	6-101-12
R27	100 ohms, 5%, 1/4 W	6-101-12
R28	10 ohms, 5%, 1/4 W	6-100-12
R29	4.7 kilohms, 5%, 1/4 W	6-472-12
R30	100 kilohms, 5%, 1/4 W	6-104-12
R31	243 ohms, 1%, 1/4 W	6-2430-12
R32	845 ohms, 1%, 1/4 W	6-8450-12
R33	10 kilohms, 5%, 1/4 W	6-103-12
R34	10 kilohms, 5%, 1/4 W	6-103-12
R35	39 kilohms, 5%, 1/4 W	6-393-12
R36	1.0 kilohm, 5%, 1/4 W	6-102-12
R37	4.7 kilohms, 5%, 1/4 W	6-472-12
R38	7.50 kilohms, 1%, 1/4 W	6-7501-12
R39	20.0 kilohms, 1%, 1/4 W	6-2002-12
R40	7.50 kilohms, 1%, 1/4 W	6-7501-12
R41	30.1 kilohms, 1%, 1/4 W	6-3012-12
R42	174 kilohms, 1%, 1/4 W	6-1743-12
R43	26.7 kilohms, 1%, 1/4 W	6-2672-12
R44	267 kilohms, 1%, 1/4 W	6-2673-12
R45	49.9 kilohms, 1%, 1/4 W	6-4992-12
R46	10.0 kilohms, 1%, 1/4 W	6-1002-12
R47	23.2 kilohms, 1%, 1/4 W	6-2322-12
R48	18.7 kilohms, 1%, 1/4 W	6-1872-12
R49	7.50 kilohms, 1%, 1/4 W	6-7501-12
R50	30.1 kilohms, 1%, 1/4 W	6-3012-12
R51	267 kilohms, 1%, 1/4 W	6-2673-12
R52	174 kilohms, 1%, 1/4 W	6-1743-12
R53	26.7 kilohms, 1%, 1/4 W	6-2672-12
R54	49.9 kilohms, 1%, 1/4 W	6-4992-12
R55	23.2 kilohms, 1%, 1/4 W	6-2322-12
R56	16.9 kilohms, 1%, 1/4 W	6-1692-12
R57	10.0 kilohms, 1%, 1/4 W	6-1002-12
R58	18.7 kilohms, 1%, 1/4 W	6-1872-12
R59	7.50 kilohms, 1%, 1/4 W	6-7501-12

CIRCUIT Comp. No.	DESCRIPTION	HEATH Part No.
Resistors (continued)		
R60	30.1 kilohms, 1%, 1/4 W	6-3012-12
R61	267 kilohms, 1%, 1/4 W	6-2673-12
R62	174 kilohms, 1%, 1/4 W	6-1743-12
R63	26.7 kilohms, 1%, 1/4 W	6-2672-12
R64	49.9 kilohms, 1%, 1/4 W	6-4992-12
R65	23.2 kilohms, 1%, 1/4 W	6-2322-12
R66	10.0 kilohms, 1%, 1/4 W	6-1002-12
R67	18.7 kilohms, 1%, 1/4 W	6-1872-12
R68	95.3 kilohms, 1%, 1/4 W	6-9532-12
R69	7.50 kilohms, 1%, 1/4 W	6-7501-12
R70	30.1 kilohms, 1%, 1/4 W	6-3012-12
R71	267 kilohms, 1%, 1/4 W	6-2673-12
R72	174 kilohms, 1%, 1/4 W	6-1743-12
R73	26.7 kilohms, 1%, 1/4 W	6-2672-12
R74	49.9 kilohms, 1%, 1/4 W	6-4992-12
R75	23.2 kilohms, 1%, 1/4 W	6-2322-12
R76	10.0 kilohms, 1%, 1/4 W	6-1002-12
R77	18.7 kilohms, 1%, 1/4 W	6-1872-12
R78	100 kilohms, 1%, 1/4 W	6-1003-12
R79	2.0 kilohms, 5%, 1/4 W	6-202-12
R80	510 kilohms, 5%, 1/4 W	6-514-12
R81	5000-ohm control	230-8090
R82	8.2 kilohms, 5%, 1/4 W	6-822-12
R83	80.6 kilohms, 1%, 1/4 W	6-8062-12
R84	19.6 kilohms, 1%, 1/4 W	6-1962-12
R85	22.1 kilohms, 1%, 1/4 W	6-2212-12
R86	23.2 kilohms, 1%, 1/4 W	6-2322-12
R87	10.0 kilohms, 1%, 1/4 W	6-1002-12
R88	18.7 kilohms, 1%, 1/4 W	6-1872-12
R89	10.0 kilohms, 1%, 1/4 W	6-1002-12
R90	10.0 kilohms, 1%, 1/4 W	6-1002-12
R91	200 ohms, 5%, 1/4 W	6-201-12
R92	200 ohms, 5%, 1/4 W	6-201-12
R93	20 kilohms, 5%, 1/4 W	6-203-12
R94	10 kilohms, 5%, 1/4 W	6-103-12
R95	100 kilohms, 5%, 1/4 W	6-104-12
R96	100-kilohm control	230-8086
R97	20 kilohms, 5%, 1/4 W	6-203-12
R98	80.6 kilohms, 1%, 1/4 W	6-8062-12
R99	19.6 kilohms, 1%, 1/4 W	6-1962-12
R100	6.49 kilohms, 1%, 1/4 W	6-6491-12
R101	23.2 kilohms, 1%, 1/4 W	6-2322-12
R102	10.0 kilohms, 1%, 1/4 W	6-1002-12
R103	18.7 kilohms, 1%, 1/4 W	6-1872-12
R104	10.0 kilohms, 1%, 1/4 W	6-1002-12
R105	10.0 kilohms, 1%, 1/4 W	6-1002-12
R106	200 ohms, 5%, 1/4 W	6-201-12
R107	200 ohms, 5%, 1/4 W	6-201-12
R108	100 kilohms, 5%, 1/4 W	6-104-12
R109	10 kilohms, 5%, 1/4 W	6-103-12

CIRCUIT Comp. No.	DESCRIPTION	HEATH Part No.
Resistors (continued)		
R110	20 kilohms, 5%, 1/4 W	6-203-12
R111	10 kilohms, 5%, 1/4 W	6-103-12
R112	24.3 kilohms, 1%, 1/4 W	6-2432-12
R113	8.06 kilohms, 1%, 1/4 W	6-8061-12
R114	24.3 kilohms, 1%, 1/4 W	6-2432-12
R115	8.06 kilohms, 1%, 1/4 W	6-8061-12
R116	24.3 kilohms, 1%, 1/4 W	6-2432-12
R117	8.06 kilohms, 1%, 1/4 W	6-8061-12
R118	33.2 kilohms, 1%, 1/4 W	6-3322-12
R119	11.0 kilohms, 1%, 1/4 W	6-1102-12
R120	33.2 kilohms, 1%, 1/4 W	6-3322-12
R121	11.0 kilohms, 1%, 1/4 W	6-1102-12
R122	10 kilohms, 5%, 1/4 W	6-103-12
R123	510 kilohms, 5%, 1/4 W	6-514-12
R124	1.0 kilohm, 5%, 1/4 W	6-102-12
R125	470 ohms, 5%, 1/4 W	6-471-12
R126	200 ohms, 5%, 1/4 W	6-201-12
R127	47 kilohms, 5%, 1/4 W	6-473-12
R128	510 kilohms, 5%, 1/4 W	6-514-12
R129	10 kilohms, 5%, 1/4 W	6-103-12
R130	10 kilohms, 5%, 1/4 W	6-103-12
R131	1.0 kilohm, 5%, 1/4 W	6-102-12
R132	5.1 kilohms, 5%, 1/4 W	6-512-12
R133	330 ohms, 5%, 1/4 W	6-331-12
R134	510 ohms, 5%, 1/4 W	6-511-12
R135	360 ohms, 5%, 1/4 W	6-361-12
R136	1000-ohm control (on #230-8001 main board)	230-8084
R136	1000-ohm control (on #230-8163 main board)	230-8161
R137-R140	On display board.	
R141	4.7 kilohms, 5%, 1/4 W	6-472-12
R142	4.7 kilohms, 5%, 1/4 W	6-472-12
R143	10 kilohms, 5%, 1/4 W	6-103-12
R144	4.7 kilohms, 5%, 1/4 W	6-472-12
R145	4.7 kilohms, 5%, 1/4 W	6-472-12
R146	10 kilohms, 5%, 1/4 W	6-103-12
R148	1.0 kilohm, 5%, 1/4 W	6-102-12
R149	4.7 kilohms, 5%, 1/4 W	6-472-12
R150	20 kilohms, 5%, 1/4 W	6-203-12
R151	680 ohms, 5%, 1/4 W	6-681-12
R152	680 ohms, 5%, 1/4 W	6-681-12
R153	4.99 kilohms, 1%, 1/4 W	6-4991-12
R154	4.99 kilohms, 1%, 1/4 W	6-4991-12
R155	25-kilohm control	230-8088
R156	4.99 kilohms, 1%, 1/4 W	6-4991-12
R157	500-ohm control	230-8089
R158	4.99 kilohms, 1%, 1/4 W	6-4991-12
R159	200 ohms, 5%, 1/4 W	6-201-12

CIRCUIT Comp. No.	DESCRIPTION	HEATH Part No.
Resistors (continued)		
R160	3.3 kilohms, 5%, 1/4 W	6-332-12
R161	4.7 kilohms, 5%, 1/4 W	6-472-12
R162	15 kilohms, 5%, 1/4 W	6-153-12
R163	18 kilohms, 5%, 1/4 W	6-183-12
R164	10-kilohm control	230-8085
R165	10-kilohm control	230-8085
R166	12 kilohms, 5%, 1/4 W	6-123-12
R167	20-kilohm control	230-8087
R168	10-kilohm control	230-8085
R169	4.7 kilohms, 5%, 1/4 W	6-472-12
R170	68 ohms, 5%, 1/4 W	6-680-12
R171	430 ohms, 5%, 1/4 W	6-431-12
R172	120 ohms, 5%, 1/4 W	6-121-12
R173	243 ohms, 1%, 1/4 W	6-2430-12
R174	1.69 kilohms, 1%, 1/4 W	6-1691-12
R175	3.09 kilohms, 1%, 1/4 W	6-3091-12
R176	6.19 kilohms, 1%, 1/4 W	6-6191-12
R177	4.7 kilohms, 5%, 1/4 W	6-472-12
R178	10 kilohms, 5%, 1/4 W	6-103-12
R179	10 kilohms, 5%, 1/4 W	6-103-12
R180	4.7 kilohms, 5%, 1/4 W	6-472-12
R181	1.0 kilohm, 5%, 1/4 W	6-102-12
R182	4.7 kilohms, 5%, 1/4 W	6-472-12
R183	4.7 kilohms, 5%, 1/4 W	6-472-1[illegible]
R184	10 kilohms, 5%, 1/4 W	6-103-[illegible]
R185	10 kilohms, 5%, 1/4 W	6-103-12
R186	330 ohms, 5%, 1/4 W	6-331-12
SWITCHES		
SW1	OFF/ON, 2P2T	230-8139
SW2	RADIO, 6P2T	230-8140

CIRCUIT Comp. No.	DESCRIPTION	HEATH Part No.
INTEGRATED CIRCUITS		
U1	Z80A	230-8120 or 443-881
U2	27256 (on #230-8001 board)	444-580
U2	27256 (on #230-8163 board)	444-580-1
U3	27128 (on #230-8001 board)	444-581
U3	27128 (on #230-8163 board)	444-581-1
U4	6264 or 5165	230-8118 or 443-1138
U5	6264 or 5165	230-8118 or 443-1138
U6	Z8536	230-8122
U7	Z8530	230-8121
U8	74LS393	230-8117 or 443-973
U9	74LS164	230-8116 or 443-769
U10	74HC139	230-8115 or 443-1319
U11	On display board.	
U12	On display board.	
U13	NE556N	230-8105 or 442-740
U14	74LS11	230-8111 or 443-864
U15	74LS04	230-8109 or 443-755
U16	74HC14	230-8112 or 443-1299
U17	74LS32	230-8113 or 443-875
U18	7406	230-8110 or 443-967
U19	MC1489	230-8125 or 443-795
U20	MC1488	230-8124 or 443-794
U21	LM317T	442-708
U22	4066B	230-8123 or 442-744
U23	MC34074 or LF347N	230-8106 or 442-756
U24	4066B	230-8123 or 442-744
U25	4066B	230-8123 or 442-744
U26	MC34074 or LF347N	230-8106 or 442-756
U27	4066B	230-8123 or 442-744
U28	MC34074 or LF347N	230-8106 or 442-756
U29	4066B	230-8123 or 442-744
U30	MC34074 or LF347N	230-8106 or 442-756
U31	4066B	230-8123 or 442-744
U32	MC34074 or LF347N	230-8106 or 442-756
U33	4066B	230-8123 or 442-744
U34	MC34074 or LF347N	230-8106 or 442-756
U35	4066B	230-8123 or 442-744
U36	On display board.	
U37	7406	230-8110 or 443-967
U38	7406	230-8110 or 443-967
U39	74LS04	230-8109 or 443-755
U40	XR2206	230-8107 or 442-710
U41	LM317L	442-772

CIRCUIT Comp. No.	DESCRIPTION	HEATH Part No.
CRYSTALS		
Y1	4.0000 MHz	230-8142
Y2	2.4576 MHz	230-8141
HARDWARE		
	Lockwasher, #4	254-9
	Lockwasher, #6	254-1
	Nut, 4-40	252-2
	Screw, 4-40 x 3/8"	250-1412
	Screw, 6-32 x 1/4"	250-1325
	Spacer, round, 6-32 x 15/32"	255-23
IC SOCKETS		
	14-pin	434-298
	16-pin	434-299
	28-pin	434-312
	40-pin	434-253
MISCELLANEOUS		
	Allen wrench, 1/16"	490-14
	Circuit board, main, first production run	230-8001
	Circuit board, main, second production run	230-8163
	Foot	261-9
	Fuse clip	230-8151
	Heat sink	230-8149
	Pushbutton	230-8150
	Silicone grease	352-13

SEMICONDUCTOR ID CHARTS AND IC DATA

IC DATA

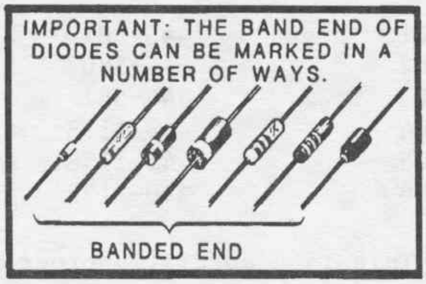
#230-8096	RBG-1000
#230-8106	MC34074, LF347 (N), JRC6002, or JRC7005
#230-8107	KR2206
#230-8114	7445
#230-8115	74HC139
#230-8121	Z8530
#230-8122	Z8536
#230-8123	4066B
#442-708	LM317T
#442-740	NE556
#442-772	LM317L
#442-798	LM3914
#443-755	74LS04
#443-769	74LS164
#443-794	MC1488
#443-795	MC1489
#443-864	74LS11
#443-875	74LS32
#443-881	Z80A
#443-967	7406
#443-973	74LS393
#443-1138	6264, 5165, or 3664
#443-1299	74HC14
#444-580	27256
#444-581	27128

SEMICONDUCTOR IDENTIFICATION CHARTS

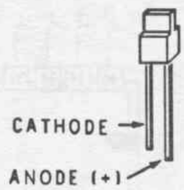
DIODES

COMPONENT NUMBER	HEATH PART NUMBER	MAY BE REPLACED WITH	KEY NUMBER
D1-D9	56-652	1N4448	A1
D10	57-27	1N5397	A1
D11	57-27	1N5397	A1
D12	57-27	1N5397	A1
D13-D26	56-652	1N4448	A1
D27	56-16	1N5231	A1
D28	56-652	1N4448	A1
D29	57-27	1N5397	A1
D30	57-27	1N5397	A1
D31	57-27	1N5397	A1
D32	57-27	1N5397	A1
D33	56-652	1N4448	A1
DS1-DS20	412-646	SLP151B	A2
DS21	230-8096	10-segment bar graph	A3
DS22	412-646	SLP151B	A2

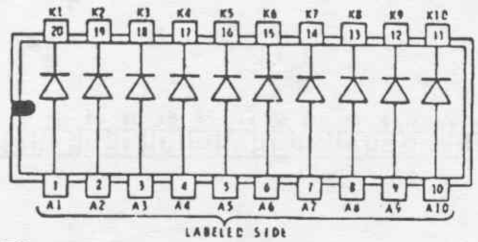
A1



A2



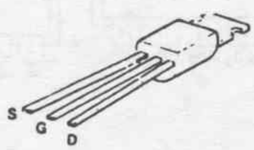
A3



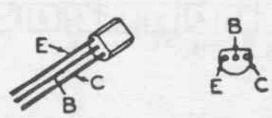
TRANSISTORS

COMPONENT NUMBER	HEATH PART NUMBER	MAY BE REPLACED WITH	KEY NUMBER
Q1	230-8101	VN10LM	B1
Q2	230-8101	VN10LM	B1
Q3	417-172	MPS6521	B2
Q4	417-874	2N3906	B2
Q5	230-8100	MPS6561	B2
Q6	417-875	2N3904	B2
Q7	417-875	2N3904	B2
Q8	417-294	MPSA42	B2
Q9	417-874	2N3906	B2
Q10	417-875	2N3904	B2
Q11	417-875	2N3904	B2

B1



B2

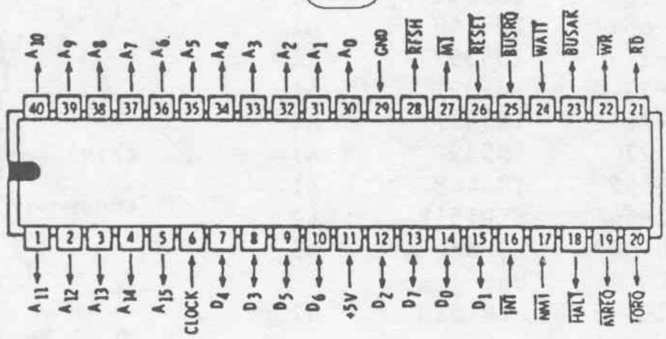


INTEGRATED CIRCUITS

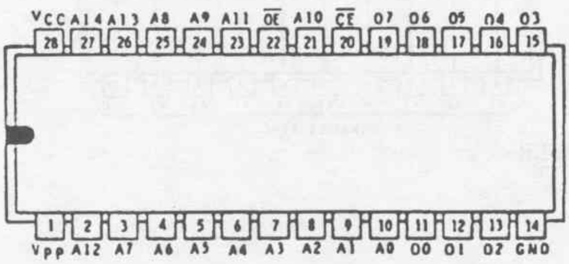
COMPONENT NUMBER	HEATH PART NUMBER	MAY BE REPLACED WITH	KEY NUMBER
U1	443-881	Z80A	C1
U2	444-580	27256*	C2
U3	444-581	27128*	C3
U4	443-1138	6264 or 5165	C4
U5	443-1138	6264 or 5165	C4
U6	230-8122	Z8536	C5

*This is a specially-programmed IC available only from the Heath Company.

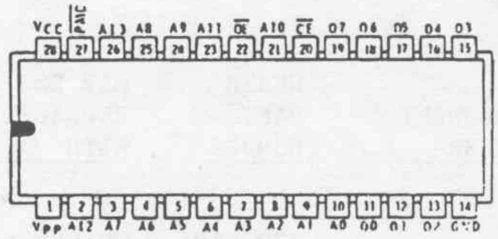
C1



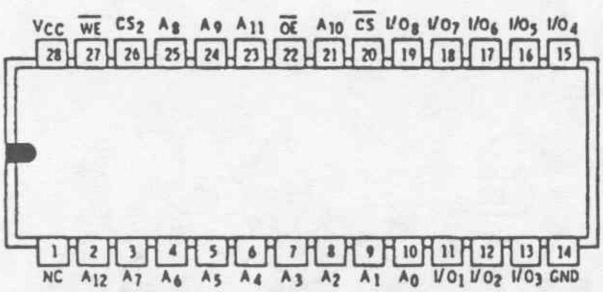
C2



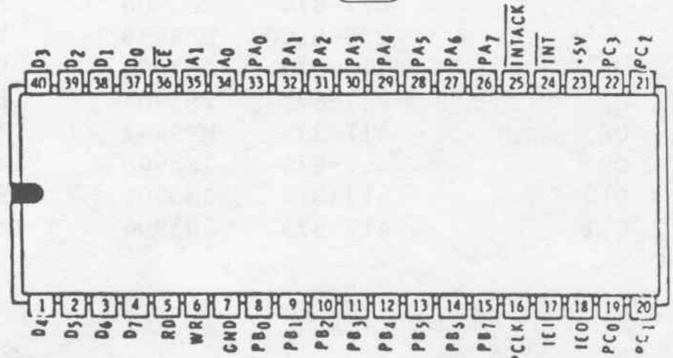
C3



C4



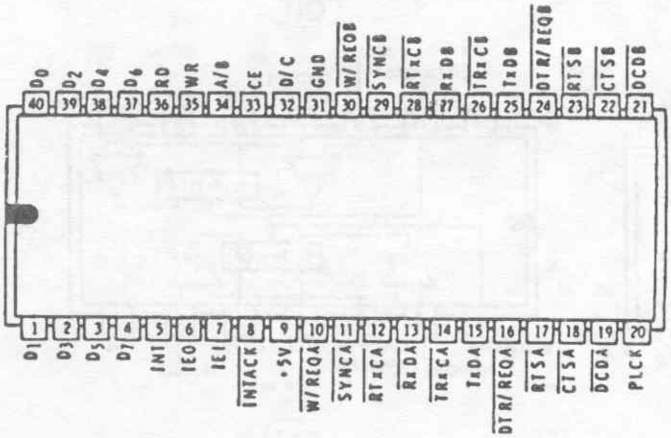
C5



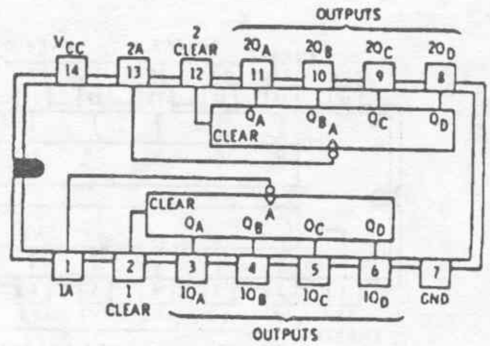
INTEGRATED CIRCUITS (Cont'd)

COMPONENT NUMBER	HEATH PART NUMBER	MAY BE REPLACED WITH	KEY NUMBER
U7	230-8121	Z8530	C6
U8	443-973	74LS393	C7
U9	443-769	74LS164	C8
U10	230-8115	74HCT139	C9

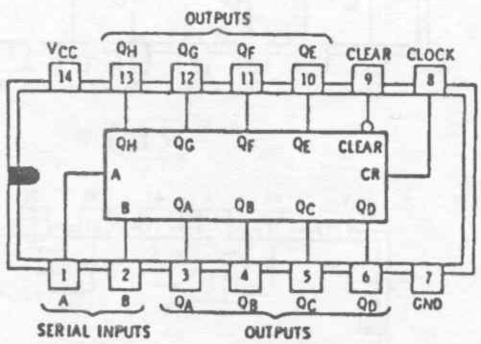
C6



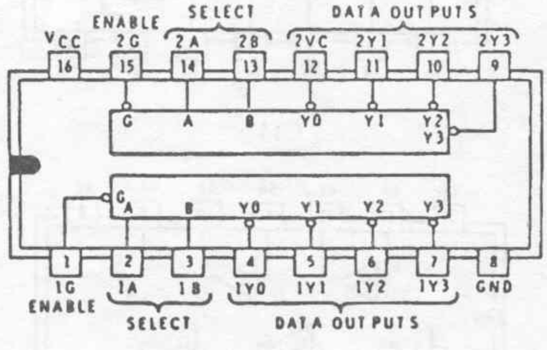
C7



C8



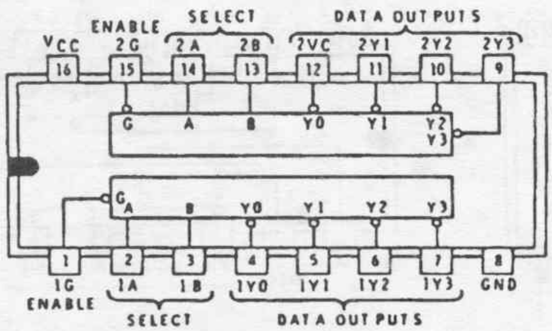
C9



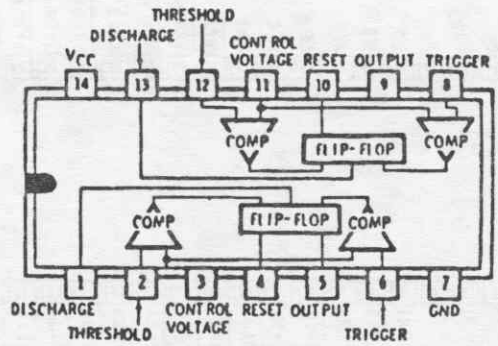
INTEGRATED CIRCUITS (Cont'd)

COMPONENT NUMBER	HEATH PART NUMBER	MAY BE REPLACED WITH	KEY NUMBER
U11	230-8114	7445	C10
U12	230-8114	7445	C10
U13	442-740	NE566N	C11
U14	443-864	74LS11	C12
U15	443-755	74LS04	C13
U16	443-1299	74HC14	C14
U17	443-875	74LS32	C15
U18	443-967	7406	C14

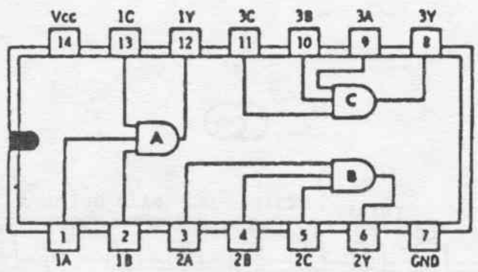
C10



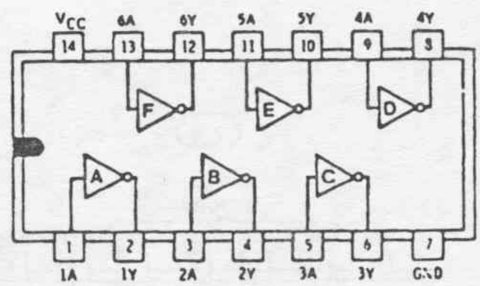
C11



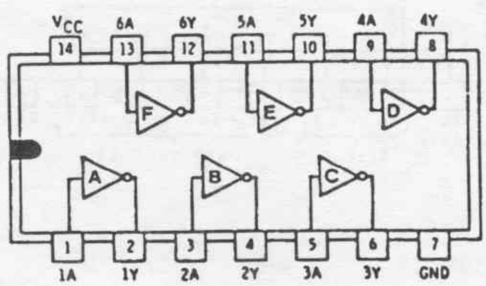
C12



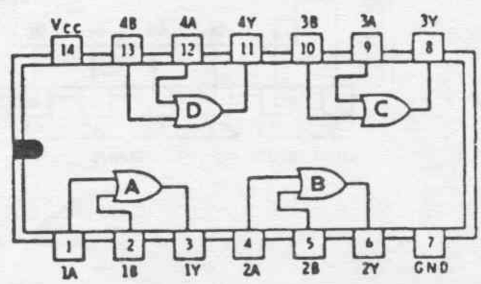
C13



C14



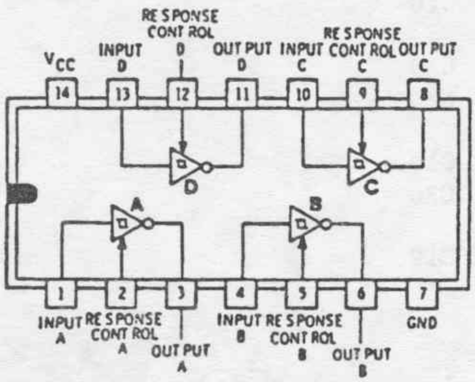
C15



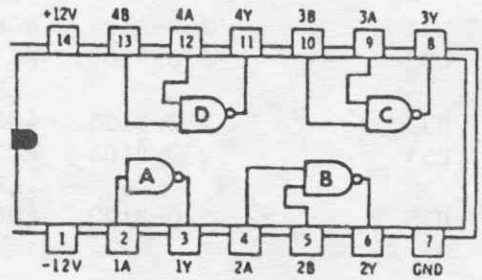
INTEGRATED CIRCUITS (Cont'd)

COMPONENT NUMBER	HEATH PART NUMBER	MAY BE REPLACED WITH	KEY NUMBER
U19	443-795	MC1489	C16
U20	443-794	MC1488	C17
U21	442-708	LM317T	C18
U22	230-8123	4066B	C19

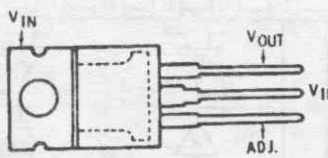
C16



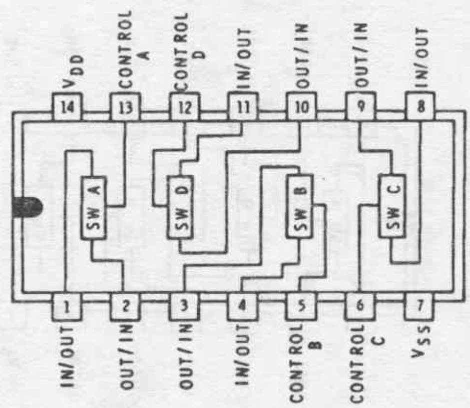
C17



C18



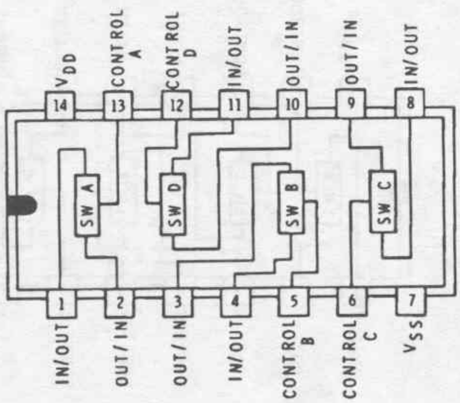
C19



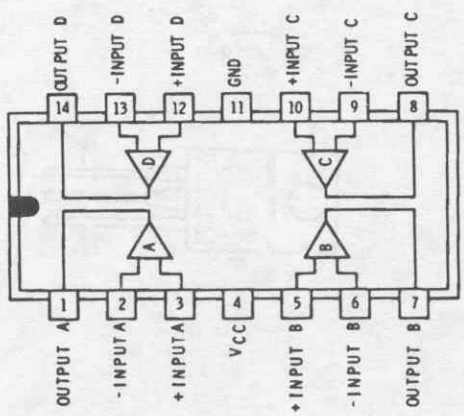
INTEGRATED CIRCUITS (Cont'd)

COMPONENT NUMBER	HEATH PART NUMBER	MAY BE REPLACED WITH	KEY NUMBER
U23	230-8106	MC34074 or LF374	C20
U24	230-8123	4066B	C19
U25	230-8123	4066B	C19
U26	230-8106	MC34074 or LF374	C20
U27	230-8123	4066B	C19
U28	230-8106	MC34074 or LF374	C20
U29	230-8123	4066B	C19
U30	230-8106	MC34074 or LF374	C20
U31	230-8123	4066B	C19
U32	230-8106	MC34074 or LF374	C20
U33	230-8123	4066B	C19
U34	230-8106	MC34074 or LF374	C20
U35	230-8123	4066B	C19

C19



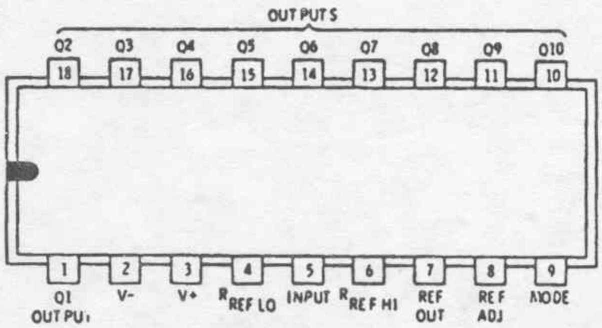
C20



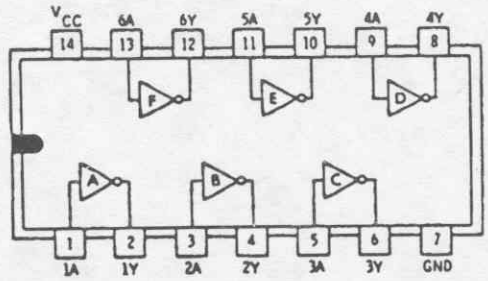
INTEGRATED CIRCUITS (Cont'd)

COMPONENT NUMBER	HEATH PART NUMBER	MAY BE REPLACED WITH	KEY NUMBER
U36	442-798	LM3914	C21
U37	443-967	7406	C22
U38	443-967	7406	C22
U39	443-755	74LS04	C23
U40	230-8107	XR2206	C24
U41	442-772	LM317L	C25

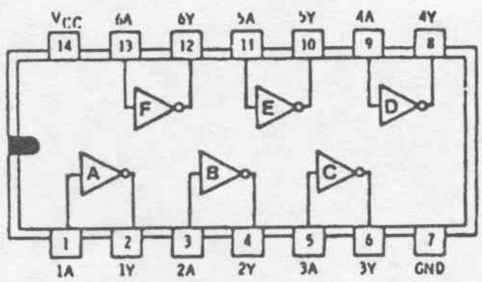
C21



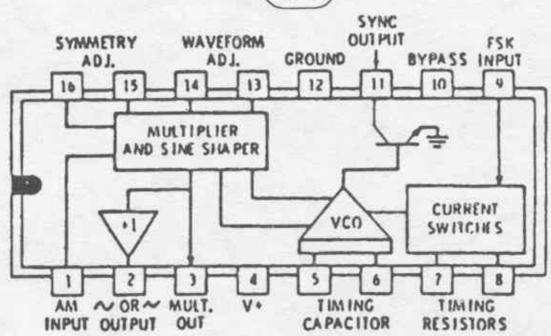
C22

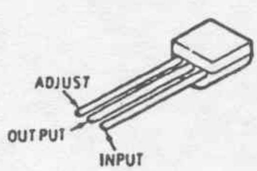


C23



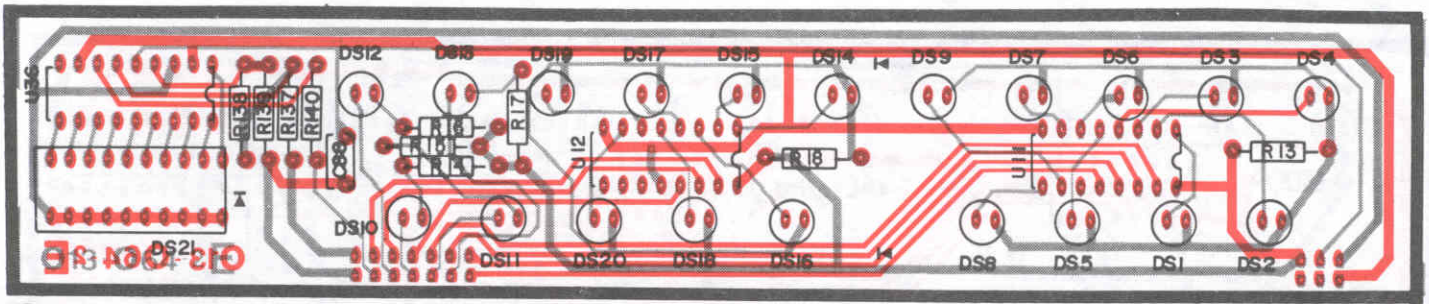
C24





C25

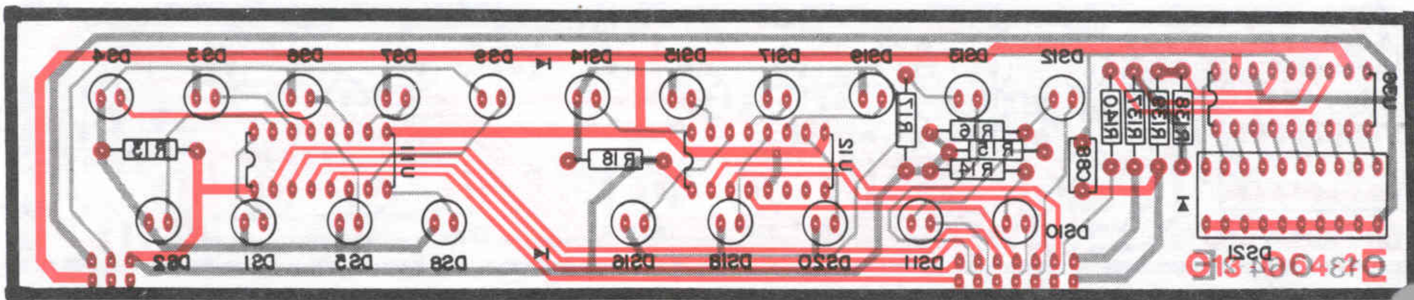
CIRCUIT BOARD
X-RAY VIEWS



DISPLAY BOARD

#230-8002

Top Side View
(Bottom Side Foils Shown in Red)

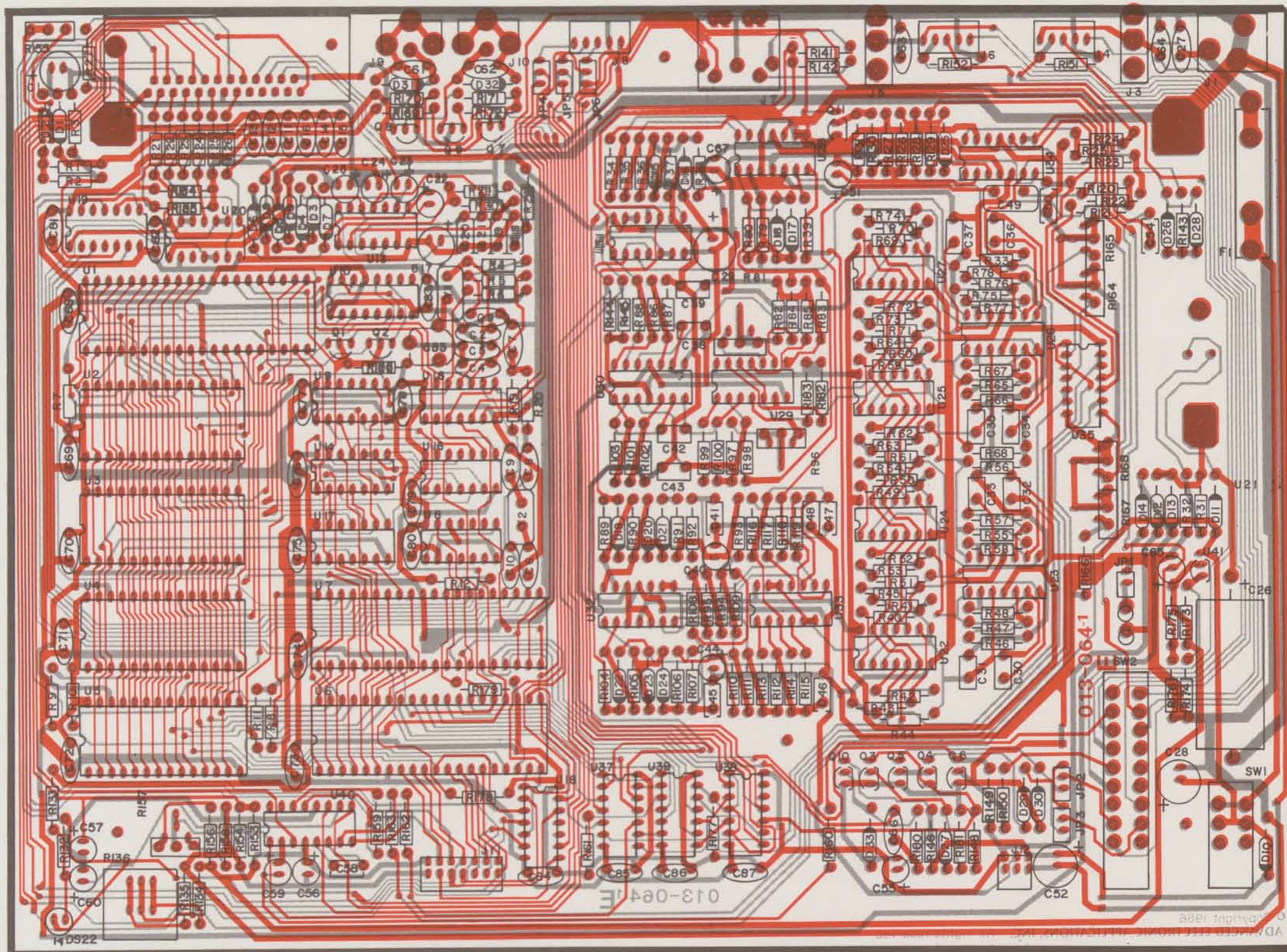


DISPLAY BOARD

#230-8002

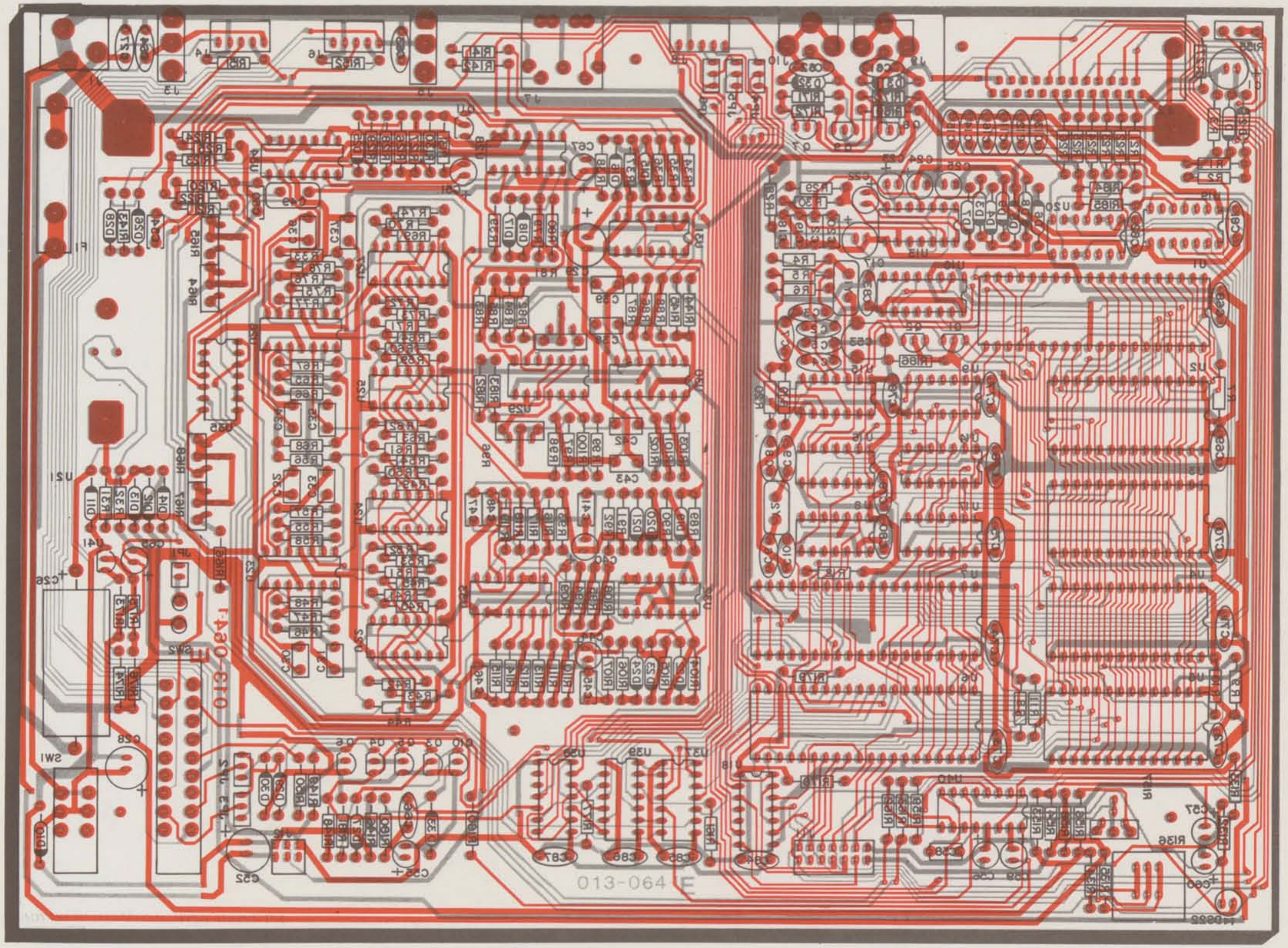
Bottom Side View

(Bottom Side Foils Shown in Red)

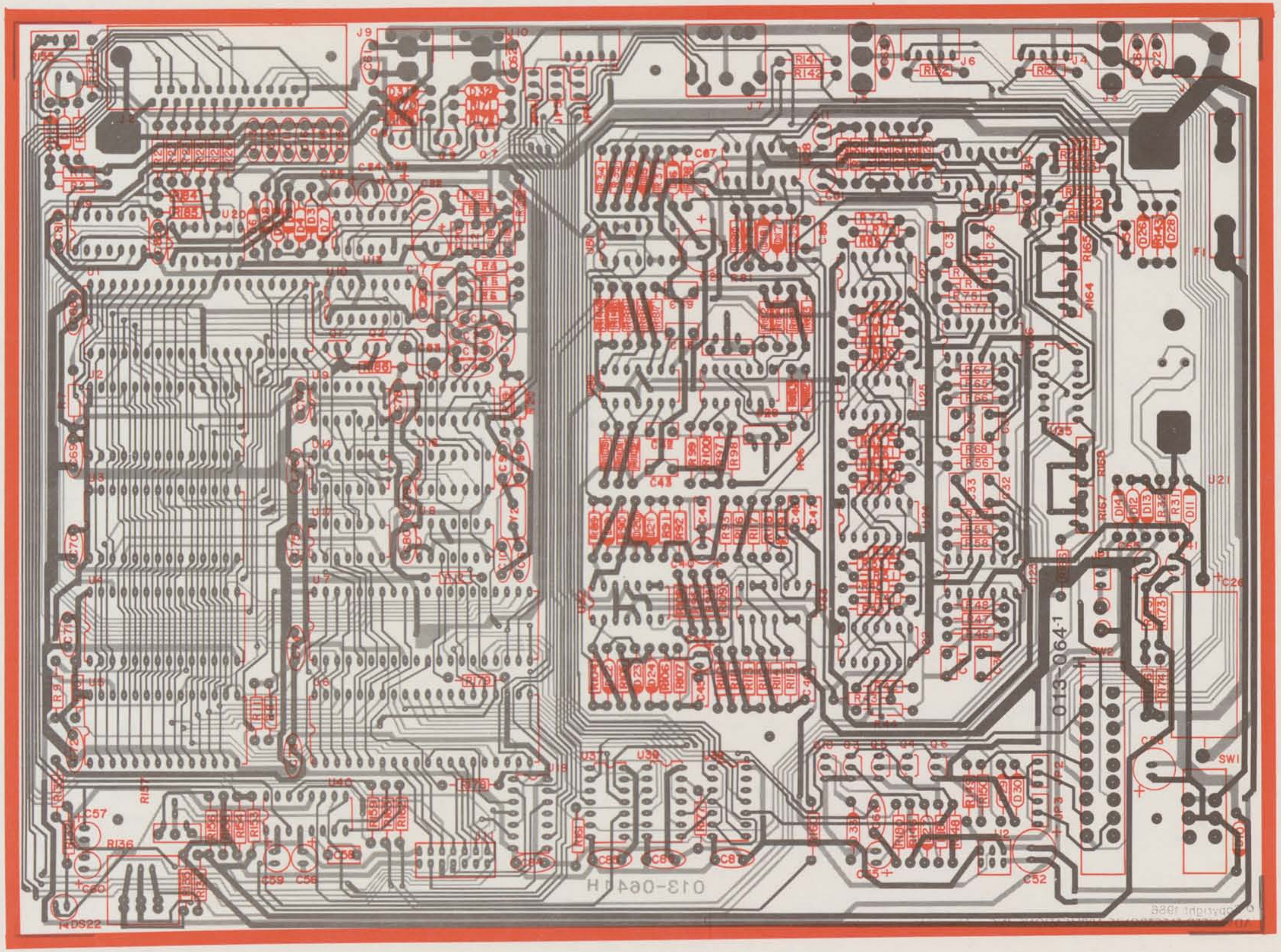


MAIN BOARD
#230-8001

Top Side View
(Top Side Foils Shown in Red)

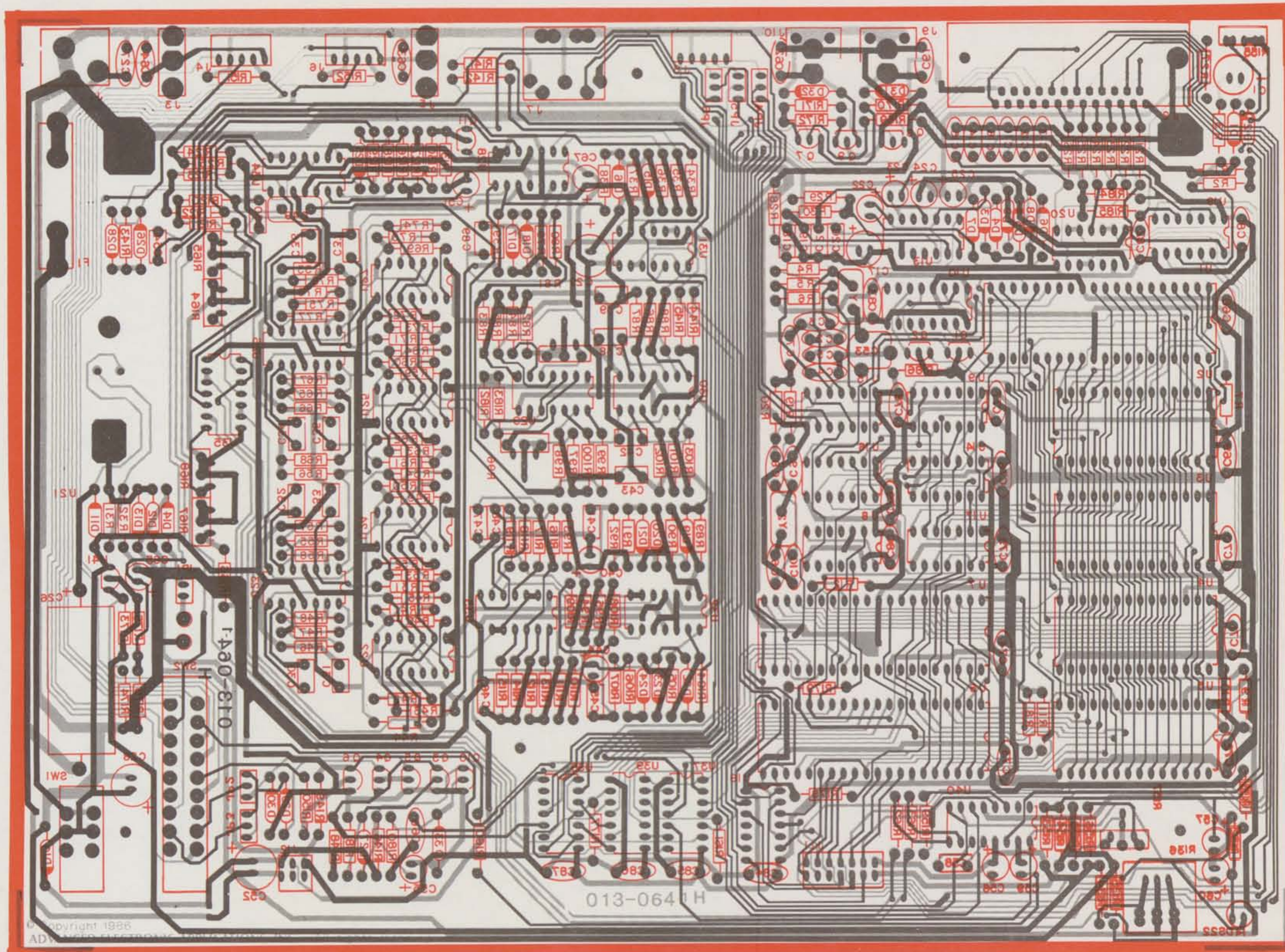


MAIN BOARD
#230-8001
Bottom Side View
(Top Side Foils Shown in Red)



MAIN BOARD
#230-8163

Top Side View
(Top Side Foils Shown in Red)



MAIN BOARD
#230-8163

Bottom Side View
(Top Side Foils Shown in Red)

CUSTOMER SERVICE

REPLACEMENT PARTS

Please provide complete information when you request replacements from either the factory or Heath/Zenith Computers and Electronics centers. Be certain to include the **HEATH** part number exactly as it appears in the parts list.

ORDERING FROM THE FACTORY

Print all of the information requested on the parts order form furnished with this product and mail it to Heath. For telephone orders (parts only) dial 616 982-3571. If you are unable to locate an order form, write us a letter or card including:

- Heath part number.
- Model number.
- Date of purchase.
- Location purchased or invoice number.
- Nature of the defect.
- Your payment or authorization for COD shipment of parts not covered by warranty.

Mail letters to: Heath Company
Benton Harbor
MI 49022
Attn: Parts Replacement

Retain original parts until you receive replacements. Parts that should be returned to the factory will be listed on your packing slip.

OBTAINING REPLACEMENTS FROM HEATH/ZENITH COMPUTER AND ELECTRONICS CENTERS

For your convenience, "over the counter" replacement parts are available from the Heath/Zenith Computer and Electronics centers listed in your catalog. Be sure to bring in the original part and purchase invoice when you request a warranty replacement from a Heath/Zenith Computer and Electronics center.

TECHNICAL CONSULTATION

Need help with your kit? — Self-Service? — Construction? – Operation? — Call or write for assistance. You'll find our Technical Consultants eager to help with just about any technical problem except "customizing" for unique applications.

The effectiveness of our consultation service depends on the information you furnish. Be sure to tell us:

- The Model number and Series number from the blue and white label.
- The date of purchase.
- An exact description of the difficulty.
- Everything you have done in attempting to correct the problem.

Also include switch positions, connections to other units, operating procedures, voltage readings, and any other information you think might be helpful.

Please do not send parts for testing, unless this is specifically requested by our Consultants.

Hints: Telephone traffic is lightest at midweek — please be sure your Manual and notes are on hand when you call.

Heath/Zenith Computer and Electronics center facilities are also available for telephone or "walk-in" personal assistance.

REPAIR SERVICE

Service facilities are available, if they are needed, to repair your completed kit. (Kits that have been modified, soldered with paste flux or acid core solder, cannot be accepted for repair.)

If it is convenient, personally deliver your kit to a Heath/Zenith Computers and Electronics center. For warranty parts replacement, supply a copy of the invoice or sales slip.

If you prefer to ship your kit to the factory, attach a letter containing the following information directly to the unit:

- Your name and address.
- Date of purchase and invoice number.
- Copies of all correspondence relevant to the service of the kit.
- A brief description of the difficulty.
- Authorization to return your kit COD for the service and shipping charges. (This will reduce the possibility of delay.)

Check the equipment to see that all screws and parts are secured. (Do not include any wooden cabinets or color television picture tubes, as these are easily damaged in shipment. Do not include the kit Manual.) Place the equipment in a strong carton with at least THREE INCHES of *resilient* packing material (shredded paper, excelsior, etc.) on all sides. Use additional packing material where there are protrusions (control sticks, large knobs, etc.). If the unit weighs over 15 lbs., place this carton in another one with 3/4" of packing material between the two.

Seal the carton with reinforced gummed tape, tie it with a strong cord, and mark it "Fragile" on at least two sides. Remember, the carrier will not accept liability for shipping damage if the unit is insufficiently packed. Ship by prepaid express, United Parcel Service, or insured Parcel Post to:

Heath Company
Service Department
Benton Harbor, Michigan 49022

Heath Company
Benton Harbor, Michigan