AZDEN PCS-4000

2-METER FM TRANSCEIVER

ADJUSTMENT AND SERVICE MANUAL

AZDEN

PCS-4000 ADJUSTMENT AND SERVICE MANUAL

1. TESTING EQUIPMENT

In order to fully adjust and service the Azden PCS-4000, the following test equipment will be required:

(a) Frequency counter
(b) Spectrum Analyzer
(c) Tracking generator
(d) Wattmeter (50 ohms impedance)
(e) Directional Coupler
(f) Linear Detector
(g) Standard Signal Generator
(h) SINAD Meter
(i) Audio Oscillator (600 ohms output impedance)
(j) Oscilloscope
(k) RF Voltmeter (input impedance above 100K ohms)

2. DISASSEMBLY PROCEDURE

Refer to the operating manual. Remove top and bottom cabinets first. Be sure to use screwdrivers of the correct size.

3. TOOLS FOR ADJUSTMENT

Do not use metal tools for adjusting ferrite cores. This will cause changes in inductance while adjustments are being made. It also increases the risk of damage to the cores. An adjustment driver made of plastic or bakelite is recommended.

4. CIRCUIT OPERATION

4-1. Outline

The PCS-4000 is a 2-meter (142.000 to 149.995 MHz) FM amateur-band transceiver, developed primarily for automobile installations. It employs a four-bit CMOS microcomputer for all frequency-control functions. Fig. 1 is a block diagram illustrating the functional operation of the PCS-4000.

4-2. Display Section

The display section is functionally illustrated in Fig. 2. The layout of components is shown in Fig. 3.

Note 1: The SW in Fig. 2 and D119 in Fig. 3 serve to prevent current flow from the microcomputer output ports (R and 0) during memory back-up periods (power switch OFF).

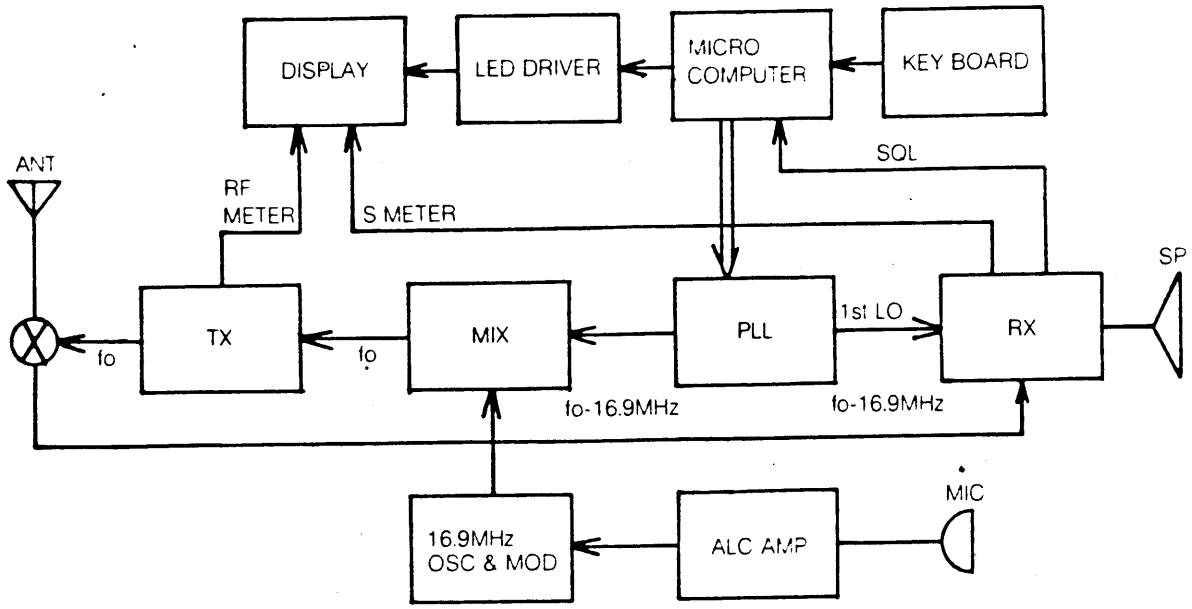

DISPLAY
LED DRIVER
MICRO COMPUTER
KEY BOARD
ANT
RF METER
S METER
SQL
SP
TX
MIX
PLL
1st LO
RX
fo
fo
fo-16.9MHz
fo-16.9MHz
MIC
16.9MHz OSC & MOD
ALC AMP

Fig. 1

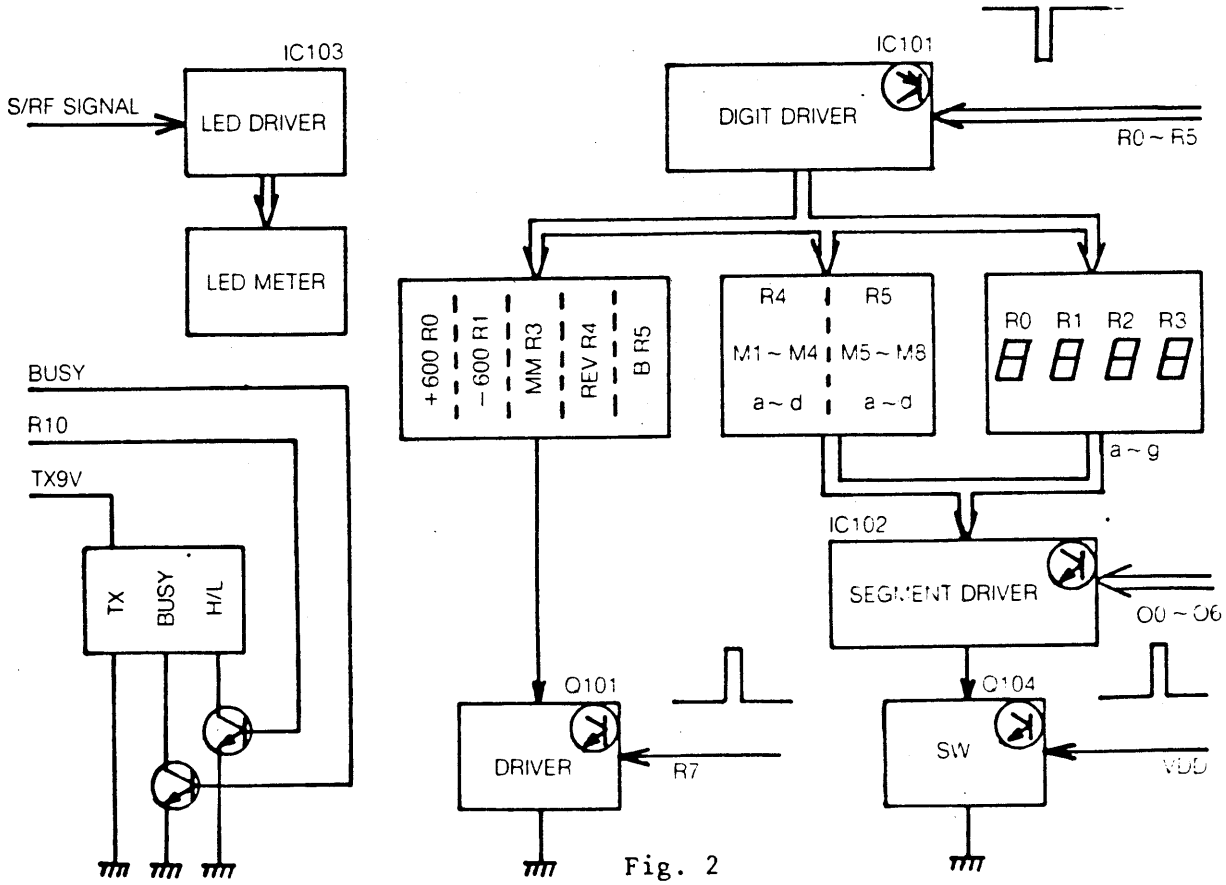

IC103
S/RF SIGNAL
LED DRIVER
LED METER
BUSY
R10
TX9V
TX
BUSY
H/L
IC101
DIGIT DRIVER
R0 ~ R5
+600 R0
−600 R1
MM R3
REV R4
B R5
R4
R5
M1 ~ M4
M5 ~ M8
a ~ d
a ~ d
R0 R1 R2 R3
a ~ g
IC102
SEGMENT DRIVER
O0 ~ O6
Q101
DRIVER
R7
Q104
SW
VDD

Fig. 2

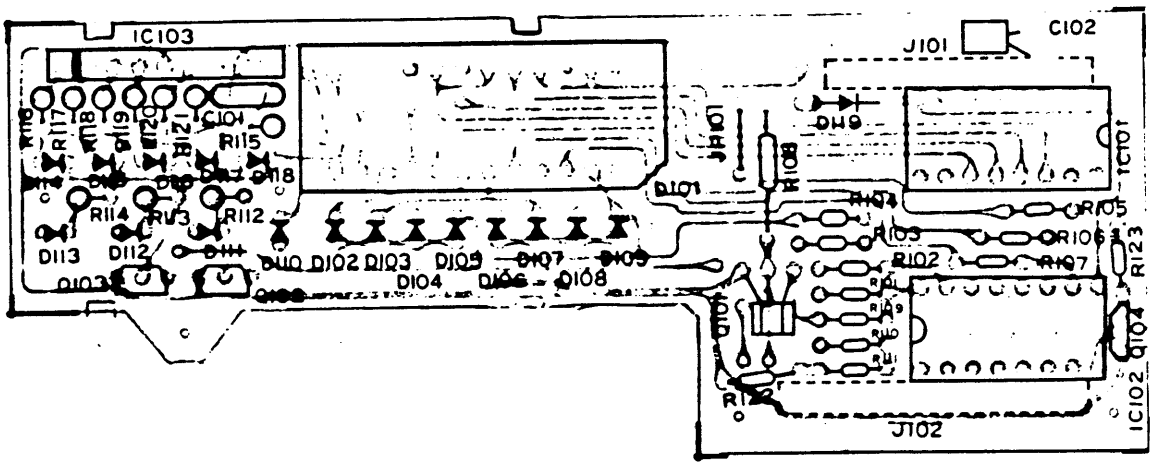


Fig. 3

Note 2: The external appearance of the frequency display LEDs is bright green, which is the same as in the PCS-3000 2-meter FM transceiver. However, the PCS-4000 uses common-anode type diodes, while the PCS-3000 employs common-cathode types. This is important when replacing diodes.

Note 3: In the mounted position, the longer wire leads of diodes D102 through D118 are the anode leads.

4-3. Control Section

The control-section component layout is shown in Fig. 4, and a functional block diagram is given by Fig. 5.

4-3-1. Operating Precautions for Key Matrix

As can be seen from Fig. 4, the control section is built around the four-bit CMOS microcomputer MB8855. The operation of the MB8855 is determined by shorting of the output ports R and the key input ports K. The combinations are listed in Tables 1 through 4.

As we can see from Table 5, the division frequency of the PLL programmable divider for the 144-MHz band in the EU (European) mode is 12.5 kHz, and in the JP (Japanese) and US (United States) modes it is 5 kHz. Therefore, Table 2 should not be used in an attempt to perform conversion between the EU mode and the JP or US modes. To convert the unit, it is necessary to change the frequency of the

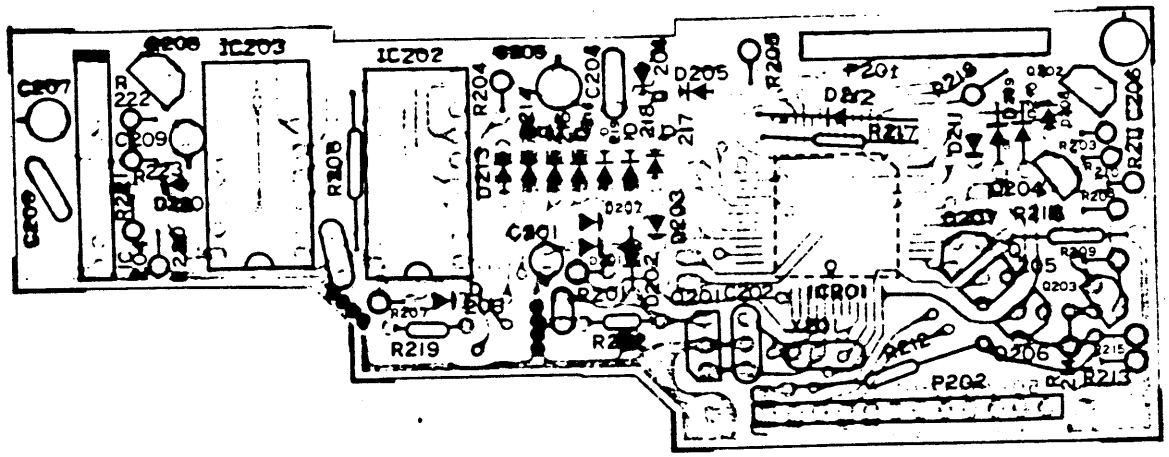

IC203
IC202
D205
R205
R219
P202

Fig. 4

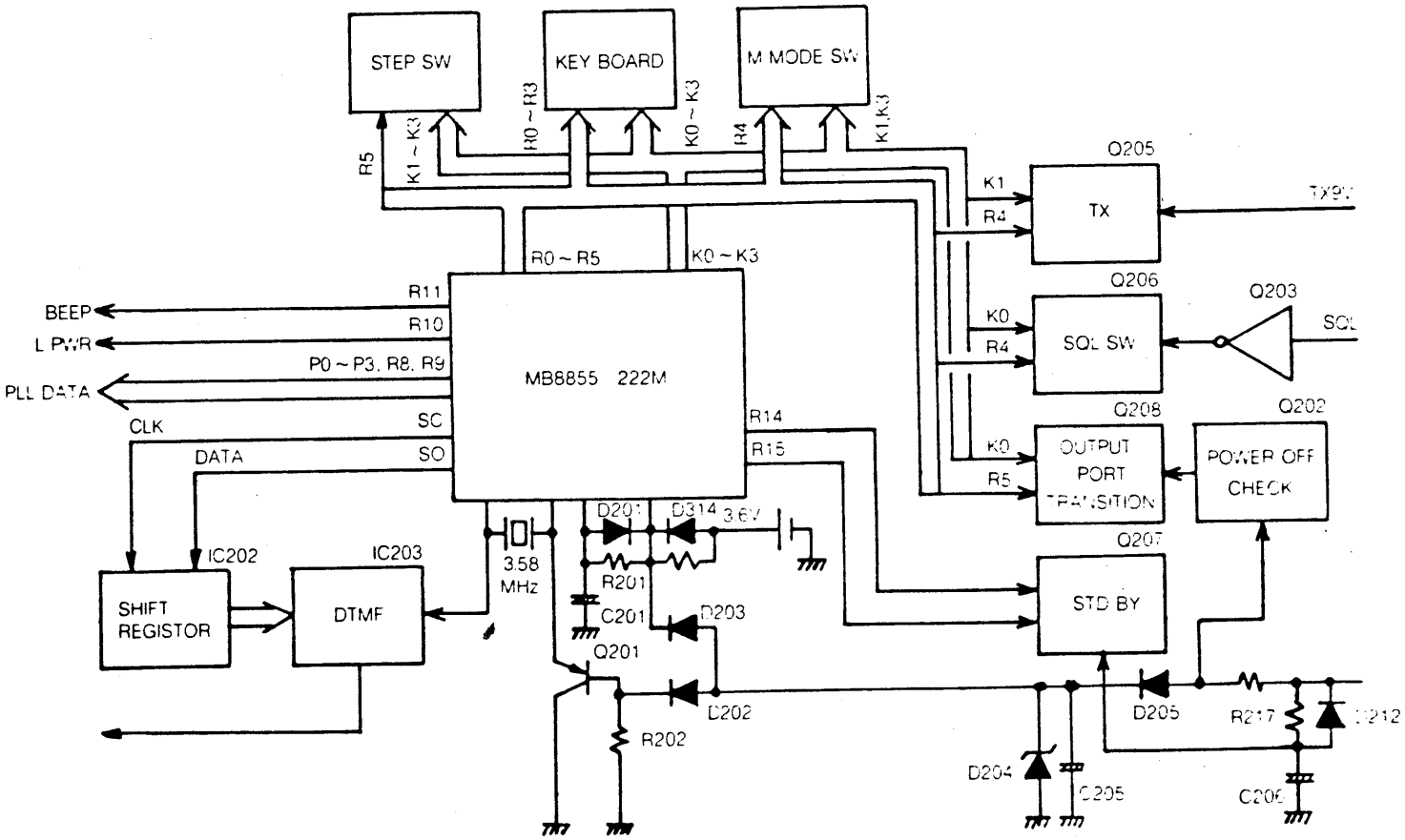

STEP SW
KEY BOARD
M MODE SW
R0 ~ R3
K0 ~ K3
R4
K1,K3
R5
K1 ~ K3
Q205
TX
K1
R4
R0 ~ R5
K0 ~ K3
Q206
SQL SW
Q203
SQL
K0
R4
BEEP
L PWR
PLL DATA
CLK
DATA
R11
R10
P0 ~ P3, R8, R9
SC
SO
MB8855 222M
R14
R15
Q208
OUTPUT PORT TRANSITION
Q202
POWER OFF CHECK
K0
R5
D201
D314
3.6V
3.58 MHz
IC202
IC203
SHIFT REGISTOR
DTMF
R201
C201
Q201
D203
D202
R202
Q207
STD BY
D205
R217
D212
D204
C205
C206

Fig. 5

222M KEY MATRIX

Table 1: STEP

	R5							
	5K	10K	12.5K	15K	20K	25K	40K	50K
K₀	0	0	0	0	S	S	S	S
K₁	0	0	S	S	0	0	S	S
K₂	0	S	0	S	0	S	0	S

Table 2: BAND

Freq BAND	R6						
	144/US	144/JP	144/EU	430	28	50	
K₃	0	0	0	0	S(D_{214})	S(D_{215})	
K₂	0	0	S(D_{216})	S(D_{218})	0	0	
K₁	0	S(D_{217})	0	S(D_{217})	0	S(D_{217})	

Table 3: M MODE

	R4			
	A	B	A−B	A×B
K₃	0	S(D_4)	0	S(D_4)
K₂	0	0	S(D_5)	S(D_5)

Table 4: KEY

	R0	R1	R2	R3
K₀	MHZ UP	100K UP	STEP UP	REV
K₁	MHZ DN	100K DN	STEP DN	H/L
K₂	M SCAN	M ADRS	MIA CALL	SHIFT
K₃	P SCAN	M CALL	MIB CALL	M WRITE

Table 5

Freq BAND	DISP/N	SHIFT
144/US	2.000 ~ 9.995	±0.600
	1700 ~ 3299	
144/JP	4.000 ~ 5.995	±0.600
	2100 ~ 2499	
144/EU	4.000 ~ 5.995	±0.600
	680 ~ 839	
430	0.000 ~ 9.995	±5.000
	1100 ~ 2099 × 2	
28	8.000 ~ 9.995	±0.100
	1700 ~ 2099	
50	0.000 ~ 3.995	±1.000
	1700 ~ 2499	

crystal in the PLL section. For the steps in Table 1, a combination of multiples of 5 for the JP and US modes, and multiples of 12.5 for the EU mode, is possible. But a combination where the multiples will not match is impossible using the steps in Table 1. For example, a combination of 10 kHz and 12.5 kHz is not possible, but 12.5 kHz / 25 kHz is possible, and 5 kHz / 25 kHz is also possible.

4-3-2. Microcomputer Initialization

This unit incorporates an initialization circuit that operates automatically whenever the power is switched ON. If the display shows an irregular or random indication, the initialization circuit is probably at fault. Disconnect P308 on the RX circuit board to interrupt the backup power supply, and set the power switch from OFF to ON. Automatic initialization is performed by C201, R201, and D201. For memory backup, leave the power switch in the ON position after re-initialization, and re-connect P308. The backup power-supply voltage should, at this time, be at least 3.6 volts. If it is below 3.6 volts, the memory backup battery must be charged.

4-3-3. TX Processing (K1 - R4)

When the transmitting voltage TX 9V causes Q205 to conduct, K1 - R4 is shortened. Thus the input operation to the microcomputer (Table 4) is stopped, and a serial signal is produced for operation of the DTMF IC. Then, depending on the selected split mode, the transmit offset processing is performed. IC202 is a shift register, which changes the DTMF serial signal from the microcomputer into an 8-bit parallel signal, to be supplied to IC203.

4-3-4. SQL Processing (K0 - R4)

When Q206 becomes conductive because of the SQL signal, K0 - R4 is shorted. When the scan operation (either the memory or programmable scan) is performed, scanning is interrupted while K0 - R4 is shorted. When K0 - R4 opens again, scanning is resumed.

4-3-5. Memory Backup Processing

When the STDBY terminal becomes low, the unit enters the standby mode. Then, it is necessary that Vcc be maintained for 13 command cycles (approximately 45 uS). Then, the backup power supply is used.

In order to carry out this operation, Q202 detects the

power OFF condition, making Q208 conduct and K0 - R5 become short-circuited. At this time, the microcomputer Vcc voltage is maintained by C205, allowing continued operation. When K0 - R5 is shorted, all output ports of the microcomputer are set to their determined condition, and R14 becomes low. As Q207 conducts while the power is OFF, R15 also becomes low and standby operation is initiated. When C205 is discharged and Vcc becomes smaller than the backup battery voltage, D203 switches OFF and power is supplied from the battery. Because Q201 also conducts in this situation, the clock pulse oscillation ceases. The re-setting of all output ports to their determined condition serves to prevent current from flowing from the output ports to peripheral circuits; this would lead to excessive backup current. However, because the output ports may not enter their determined settings under certain software conditions, a diode is inserted on the PLL board to prevent current from flowing from the PLL code output port.

The standby mode is released when Q207 becomes OFF (due to re-application of power to the unit). If the standby mode is discontinued too early, the microcomputer sends out the PLL code before the PLL IC has reached stable operation; this would create an unlocked condition of the PLL, but it is kept in lock by an automatic delay of the backup release time, effected by R217 and C206.

4-3-6. PLL Data

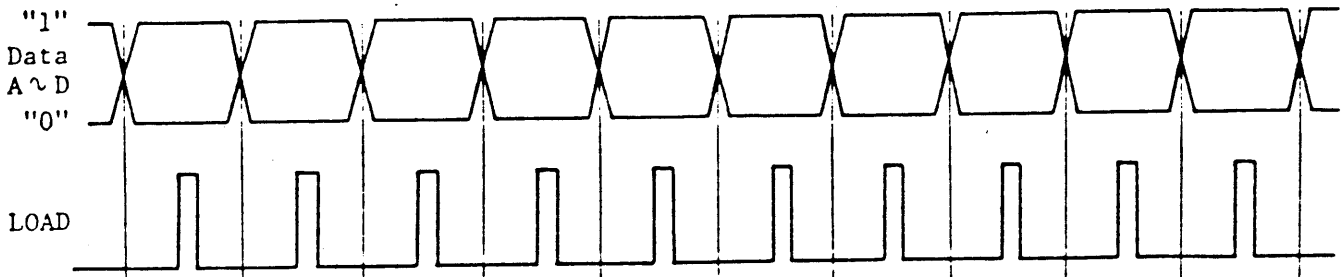
PLL data are supplied in Fig. 6. The ZNH signal is high, except for frequencies of 144.000 to 145.995 (in the 144/US mode).

4-4. PLL Section

The PLL IC is diagrammed in Fig. 7, and the entire PLL section is diagrammed in Fig. 8.

4-4-1. IC401 (TC9125BP)

As shown in Fig. 7, this IC incorporates a four-digit programmable counter which operates up to approximately 16 MHz. It also contains a reference frequency divider, a phase comparator, and related circuitry for PLL operation. The selection of the programmable divider division frequency and the IC operation mode (generally 5 kHz in the 144/US mode and 12.5 kHz in the 144/EU mode) are performed by a four-bit, parallel, five-digit serial input. Details of this input signal are shown in Fig. 6. The LD terminal carries the output signal in the unlocked condition.



		Address designation of unit's	Data set of unit's	Address designation of ten's	Data set of ten's	Address disignation of hundred's	Data set of hundred's	Address disignation of thousand's	Data set of thousand's	Address designation of mode setting	Data set of mode setting
Data Input	A	1	A_1	0	A_2	1	A_3	0	A_4	1	A_5
	B	1	B_1	0	B_2	0	B_3	1	B_4	1	B_5
	C	0	C_1	1	C_2	1	C_3	1	C_4	1	C_5
	D	1	D_1	1	D_2	1	D_3	1	D_4	1	0
		F=11	F=0∿9	F=12	F=0∿9	F=13	F=0∿9	F=14	F=0∿9	F=15	F=0∿7

Fig. 6

4-4-2. Voltage-controlled Oscillator (VCO)

The low-pass filter made up of Q401, Q402 and related circuitry extracts the DC component of the signal fed from the phase comparator in IC401. This DC voltage serves to control the VCO. The oscillation frequency range is 125.1 to 133.095 MHz (127.1 to 128.9875 MHz for the 144/EU mode). The oscillating frequency is obtained by mixing the first receiving IF, 16.9 MHz, with the operating frequency. This output is fed to the receiver mixer stage and the transmitter first local oscillator and PLL mixer stage by separate buffers.

4-4-3. PLL Local Oscillator and Mixer

The local oscillator serves to convert the output from the VCO into a frequency that can drive the programmable counter. The input frequency to the programmable counter is

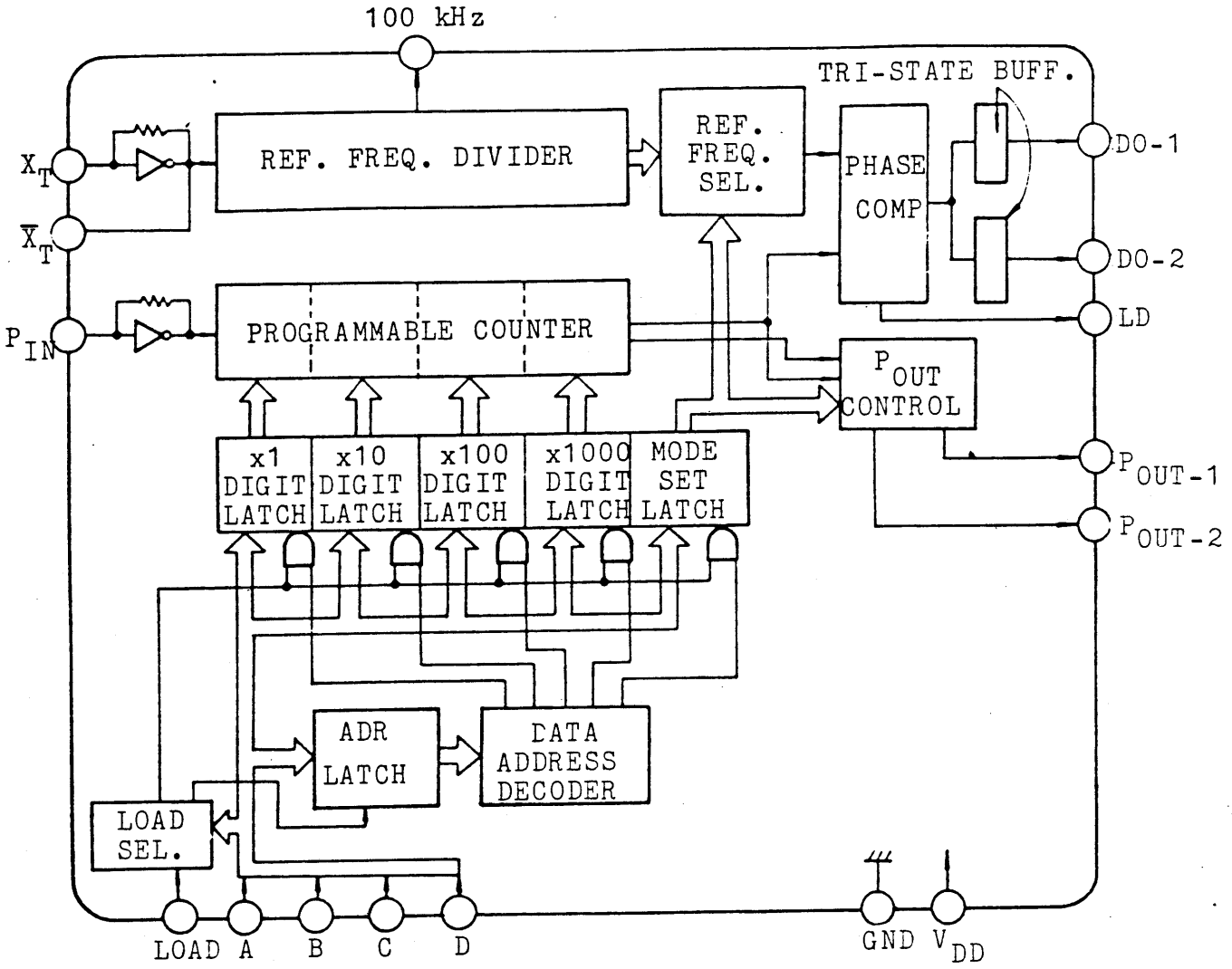

100 kHz
TRI-STATE BUFF.
X_T
$\overline{X}_T$
P_{IN}
REF. FREQ. DIVIDER
REF. FREQ. SEL.
PHASE COMP
DO-1
DO-2
LD
PROGRAMMABLE COUNTER
P_{OUT} CONTROL
x1 DIGIT LATCH
x10 DIGIT LATCH
x100 DIGIT LATCH
x1000 DIGIT LATCH
MODE SET LATCH
P_{OUT}-1
P_{OUT}-2
ADR LATCH
DATA ADDRESS DECODER
LOAD SEL.
LOAD
A
B
C
D
GND
V_{DD}

Fig. 7

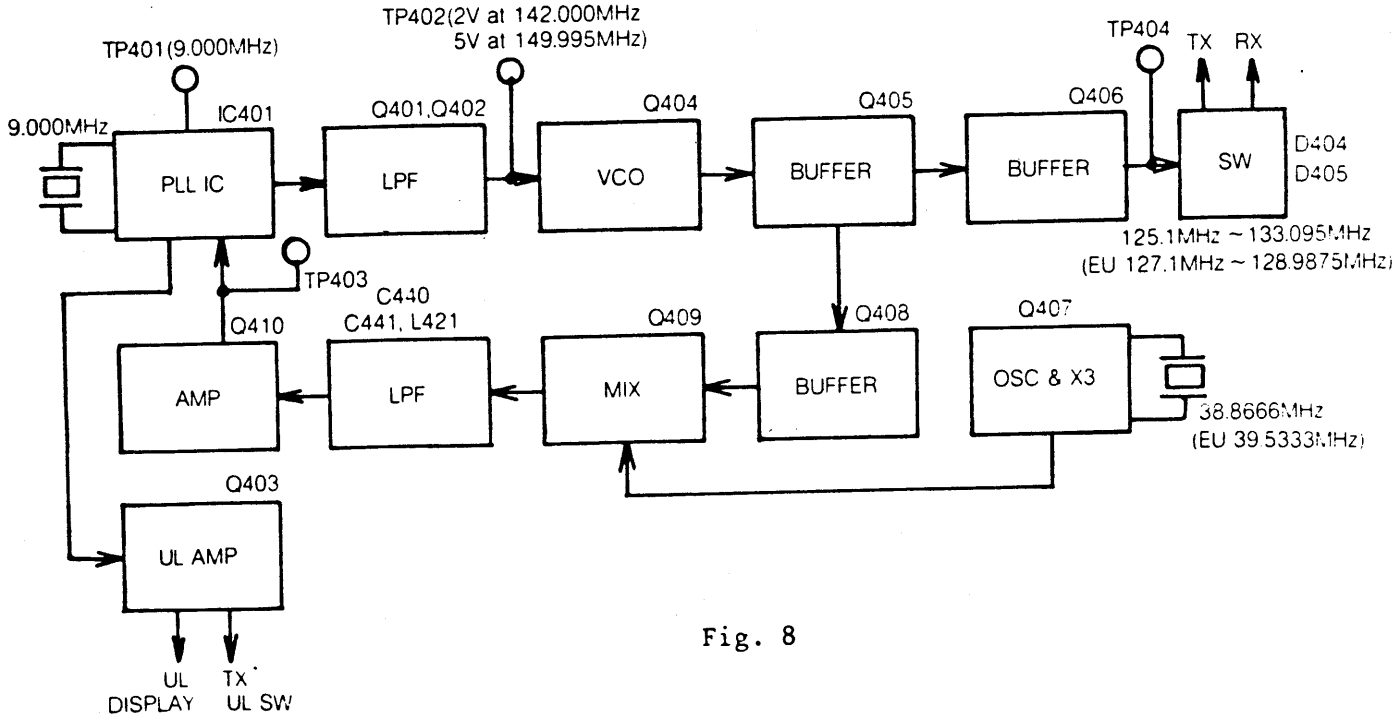

TP401(9.000MHz)
TP402(2V at 142.000MHz
5V at 149.995MHz)
TP404
TX
RX
9.000MHz
IC401
PLL IC
Q401,Q402
LPF
Q404
VCO
Q405
BUFFER
Q406
BUFFER
SW
D404
D405
125.1MHz ~ 133.095MHz
(EU 127.1MHz ~ 128.9875MHz)
TP403
C440
C441, L421
Q410
AMP
LPF
Q409
MIX
Q408
BUFFER
Q407
OSC & X3
38.8666MHz
(EU 39.5333MHz)
Q403
UL AMP
UL DISPLAY
TX UL SW

Fig. 8

set at 16.9/2 MHz to 16.9 MHz, with 8.5 MHz at the lowest receiving frequency of 142.000 MHz (144.000 MHz for EU mode). Therefore, the necessary local-oscillator frequency becomes

142.000 - 16.9 - 8.5 = 116.6 MHz (US mode)
144.000 - 16.9 - 8.5 = 118.6 MHz (EU mode)

The crystal frequency is thus

116.6/3 = 38.8666 MHz (US mode)
118.6/3 = 39.5333 MHz (EU mode)

This local oscillator signal is combined with the VCO output at Q409, and the low-pass filter (LPF) extracts the signal below 16.5 MHz, which is amplified by Q410 and fed to the programmable counter of IC401. The divisor N of the programmable counter at the lowest receiving frequency is therefore

N = 8.5 MHz / 5 kHz = 1700 (US mode)
N = 8.5 MHz / 12.5 kHz = 680 (EU mode)

4-5. Transmitter and Modulator Sections

A block diagram of the transmitter and modulator sections is shown by Fig. 9.

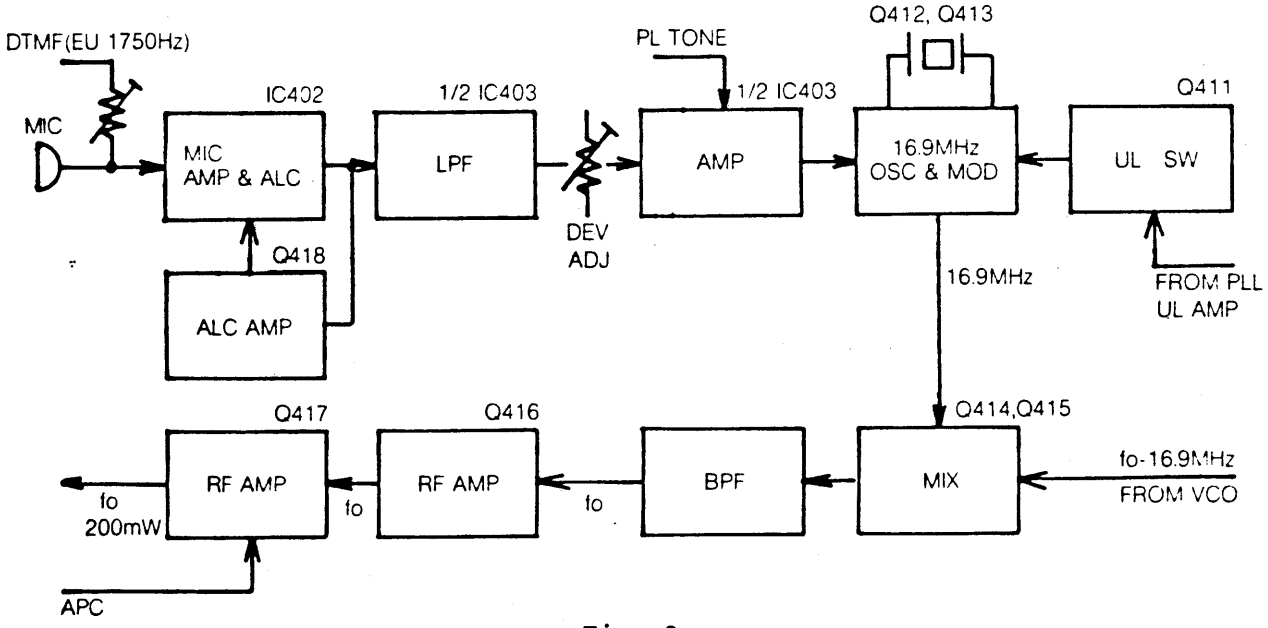


Fig. 9

4-5-1. Modulator Section

The TA7137P integrated circuit, IC402, is an audio amplifier with built-in ALC. When the microphone input exceeds a certain level, the ALC prevents further increase in amplitude. The output is fed to a tertiary active low-pass filter, which operates as a splatter filter. Then the signal is amplified at the adder circuit together with the PL tone. The output is used to directly frequency modulate the 16.9-MHz crystal oscillator circuit. Because the audio signal and the PL tone signal are added at the op-amp adder, there is no mutual interaction between them and their levels can be adjusted independently. As the crystal is directly frequency modulated, there is a minimum of distortion, even when a low audio frequency such as the PL tone is injected.

When the PLL becomes unlocked, the UL (unlock) signal from the PLL activates Q411 to stop the 16.9-MHz oscillator.

4-5-2. Transmitter Section

The signal from the VCO and the modulated 16.9-MHz signal are combined at the balanced mixer, consisting of Q414 and Q415. Then the desired frequency, f_o, is extracted at the bandpass filter and amplified by Q416 and Q417 to a level of approximately 200 mW.

4-6. RF Power Amplifier Section

The equivalent circuit of the Hybrid IC, S-AV7, for the PCS-4000 power amplifier is shown in Fig. 10.

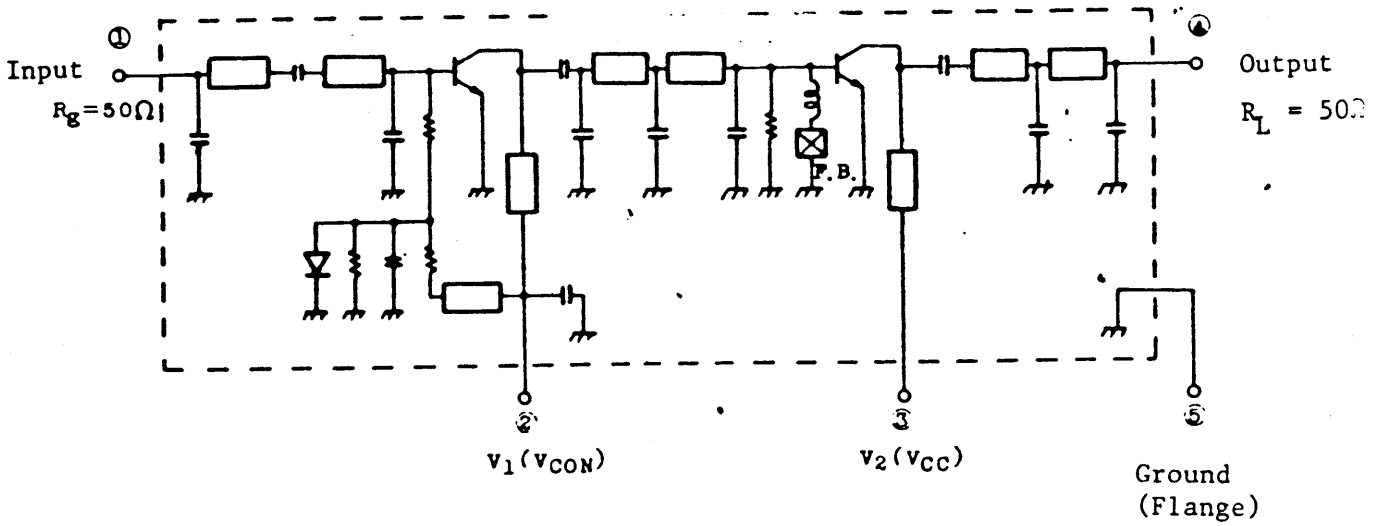


Fig. 10

This IC is designed to produce an output of more than 25 W with an input of approximately 100 mW. The output is supplied to the antenna via a four-stage low-pass filter which suppresses high-frequency harmonics. Switching between transmit and receive is performed by a relay, designed to withstand more than 150,000 ON/OFF operations with 30-W current.

4-7. Receiver Section

A block diagram of the receiver section is shown in Fig. 11. As can be seen from this diagram, the receiver section

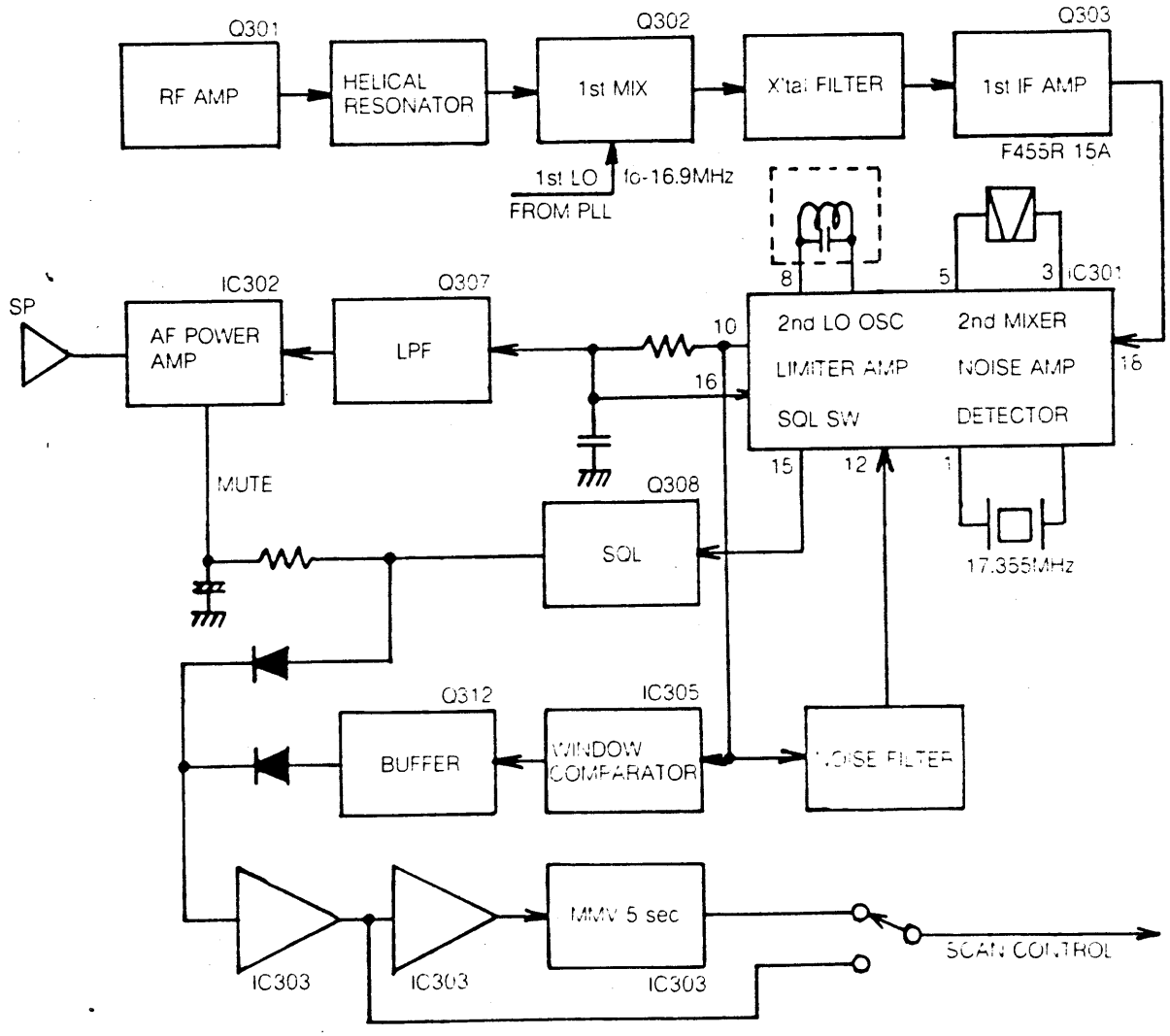


Fig. 11

employs an ordinary double-conversion type superheterodyne system. The first IF is 16.9 MHz and the second IF is 455 kHz. For RF amplification, and in the first mixer stage, MOSFETs (3SK77BL) are used. In the second mixer stage, second local oscillator, limiter amplifier, discriminator, noise amplifier, squelch, and others, the one-chip IC, MC3359 is used. This IC has good limiter characteristics and provides excellent noise-quieting sensitivity. The 5-kHz-step scanning control circuit, which operates with the discriminator to sense the center of the channel as well as the presence of carrier, assures that the PCS-4000 will stop on the correct frequency when band scanning. (This is the same circuit as that employed in the PCS-3000.)

4-8. Discriminator Scan Control

The approximate characteristics of the quadrature detector, employing the MC3359P, are shown in Fig. 12.

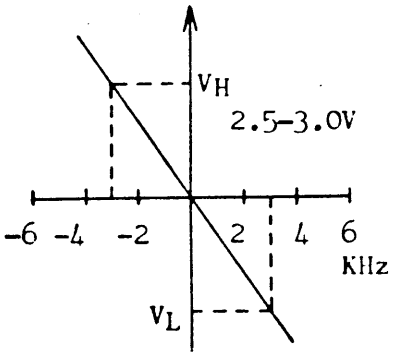


Fig. 12

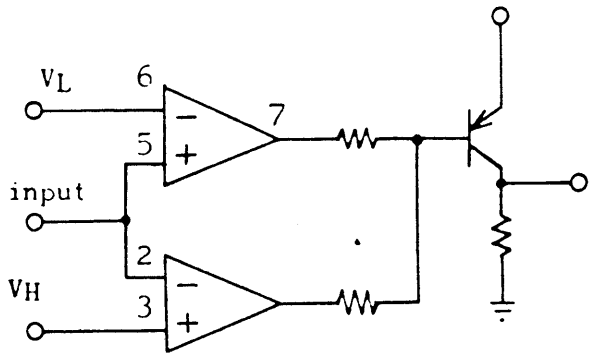


Fig. 13

By setting up a window comparator as shown in Fig. 13, with V_L and V_H (from Fig. 12) as reference voltages, a low output is obtained for frequencies within 3 kHz of the center frequency, and a high voltage is obtained for frequencies farther away than ±3 kHz. The logical AND of this output voltage and the scanning control output of the MC3359P will open the squelch when f_o is within ±3 kHz. Without this circuit, the scanning would stop prematurely.

5. ADJUSTMENT

5-1. PLL Section (Fig. 14)

5-1-1. Adjustment of Reference Frequency

* Connect a frequency counter to TP401.
* Adjust VC401 for a frequency counter reading of 9.0000 MHz, to within 100 Hz.

5-1-2. Adjustment of Mixer Stage

* Set the PCS-4000 frequency display to 6.000 (5.000 for European model).
* Connect an oscilloscope to TP402.
* Adjust L411, L412, and L413 until the amplitude of the waveform, displayed on the oscilliscope, is maximum. This amplitude should be 4 to 6 volts, and the cycle is 0.08 uS or approximately 12.5 MHz.
* If the VCO frequency is incorrect by a large amount, the PLL will fall out of lock and the above adjustment cannot be performed. In this case, first adjust L415 until the PLL becomes locked. Then perform the above procedure.

5-1-3. Output Adjustment

* Set the PCS-4000 frequency display to 6.000 (5.000 for European model).
* Connect an oscilloscope (bandwidth above 200 MHz) or an RF voltmeter (bandwidth above 200 MHz) and a frequency counter to TP404.
* Adjust L411 for a maximum indication on the oscilloscope or RF voltmeter. The indication should be between 0.5 and 1.5 volts peak-to-peak.
* Adjust VC402 for a frequency counter reading of 129.1000 MHz, to within 100 Hz.

5-1-4. Adjustment of VCO Control Voltage

* Set the PCS-4000 frequency display to 2.000 (4.000 for European model).
* Connect a DC voltmeter with an internal resistance of at least 20,000 ohms per volt.
* Adjust L415 for a voltmeter reading of 2.0 volts plus or minus 0.1 volt. (For the European model, this should be 2.8 volts plus or minus 0.1 volt.)
* VCO control voltage should be observed to increase as the PCS-4000 frequency is increased.

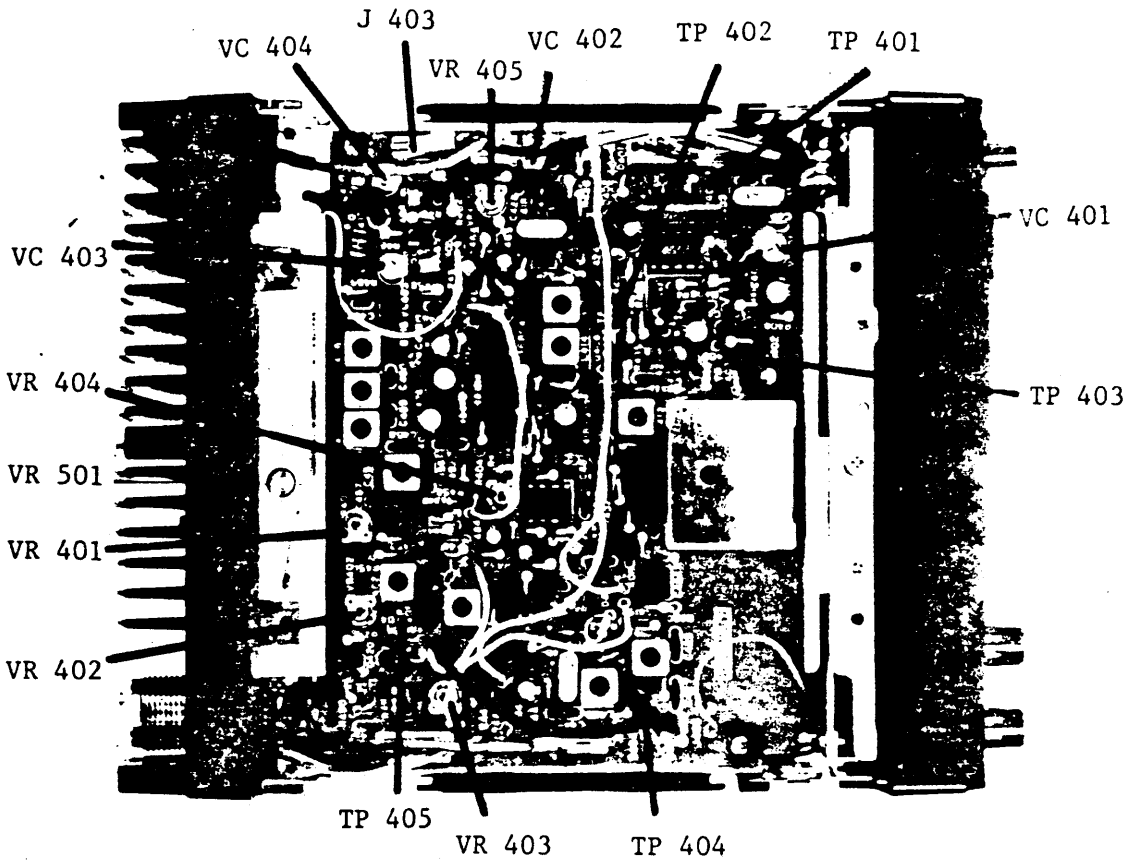

J 403
VC 404
VC 402
TP 402
TP 401
VR 405
VC 401
VC 403
VR 404
TP 403
VR 501
VR 401
VR 402
TP 405
VR 403
TP 404

Fig. 14

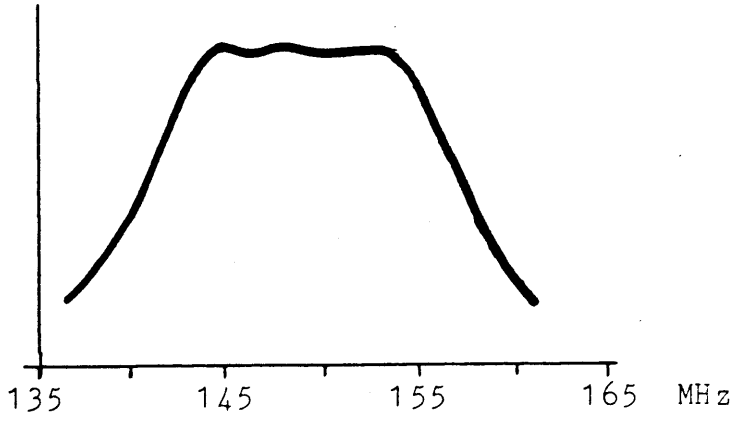

135
145
155
165
MHz

Fig. 15

5-2. Transmitter Section (Fig. 14)

5-2-1. Bandpass Filter Adjustment

* Connect a spectrum analyzer, of 50 ohms input impedance, to J403. Use an attenuator if needed. The maximum output from J403 is 26 dBm.
* Apply the output from a tracking generator to TP403.
* Turn VR401 fully counterclockwise.
* Ground the front-panel side of R415 with a clip lead. This will prevent the VCO from oscillating.
* Push the PTT lever on the microphone to put the unit in the transmit mode. Adjust L403, L404, L405, L406, VC403, and VC404 to obtain a spectrum-analyzer waveform as nearly identical to the waveform in Fig. 15 as possible.
* Adjust VR401 for minimum size of the waveform display on the spectrum analyzer.

5-2-2. Adjustment of Transmitting Frequency, Driver Output

* Connect an oscilloscope and frequency counter to TP405.
* Connect a spectrum analyzer, of 50 ohms input impedance, to J403. Use an attenuator if needed.
* Set the frequency display to 6.000.
* Push the PTT lever to put the PCS-4000 in the transmit mode. Adjust L401 for maximum size of the waveform display on the oscilloscope.
* Adjust L420 for a frequency counter reading of 16.9000 MHz, to within 100 Hz.
* Adjust L402 for maximum size of the display on the spectrum analyzer.
* Adjust VC403 and VC404 for maximum size of the display on the spectrum analyzer; this will be a critical adjustment.
* Adjust L401 and VR401 for minimum spurious output on neighboring frequencies, as shown on the spectrum analyzer. This will be a critical adjustment.
* Check to be sure that the spurious outputs are down at least 60 dB in the range 142.000-149.995 MHz, and that the output is above 200 mW.
* If the above values are not achieved, change the frequency and repeat the above steps until these requirements are met.

5-2-3. Output Adjustment

* Be sure there is a reliable connection between the driver output and the RF power-amplifier input.

* Connect a wattmeter, spectrum analyzer and counter to the output connector via an attenuator, if needed.
* Set the frequency display to 6.000 (5.000 for European model).
* Push the PTT lever to put the PCS-4000 in the transmit mode. Adjust VR403 for a wattmeter reading of 27 watts.
* Check that the output, spurious suppression, and frequency are within specifications at several points in the range 142.000 to 149.995 MHz. (For the European model, check between 144.000 and 145.987 MHz.) Since an M-coupled APC (automatic power control) is employed, a somewhat higher power output is to be expected with the US model at the lower end of its frequency range.
* Set the frequency display to 6.000 and push the H/L button to set the PCS-4000 to the low-power mode.
* Push the PTT lever, and adjust VR402 for a wattmeter reading of 5 watts.
* Adjust VR501 so that two LEDs of the RF bar-graph LED meter are illuminated in the low-power mode at 5 watts.
* Push the H/L button to return the unit to the high-power mode. Be sure that all five LEDs of the RF bar-graph LED meter light up when transmitting.

5-2-4. Modulation Adjustment

* Connect a dummy load and linear detector to the output connector using a directional coupler.
* Apply a signal of 30 mV RMS at 1.8 kHz, with 600 ohms impedance, to the microphone input terminal.
* Push the PTT switch to set the PCS-4000 to the transmit mode. Adjust VR404 so that the indication on the linear detector becomes ±5 kHz.
* Set the input at the microphone input to zero.
* Press the respective keys on the front panel, and adjust VR404 so that the linear detector indication becomes ±3 kHz.
* For the Eurpoean model, press the TONE switch and adjust for a linear detector reading of ±5 kHz.

5-3. Receiver Section (Fig. 16)

5-3-1. RF amplification Stage

* Connect a tracking generator to the antenna connector.
* Connect a spectrum analyzer to TP301.
* Disconnect the cable supplying the local oscillator signal from J301.
* Adjust L301, L302, HR301 so that the waveform display on the spectrum analyzer closely resembles that in Fig. 17,

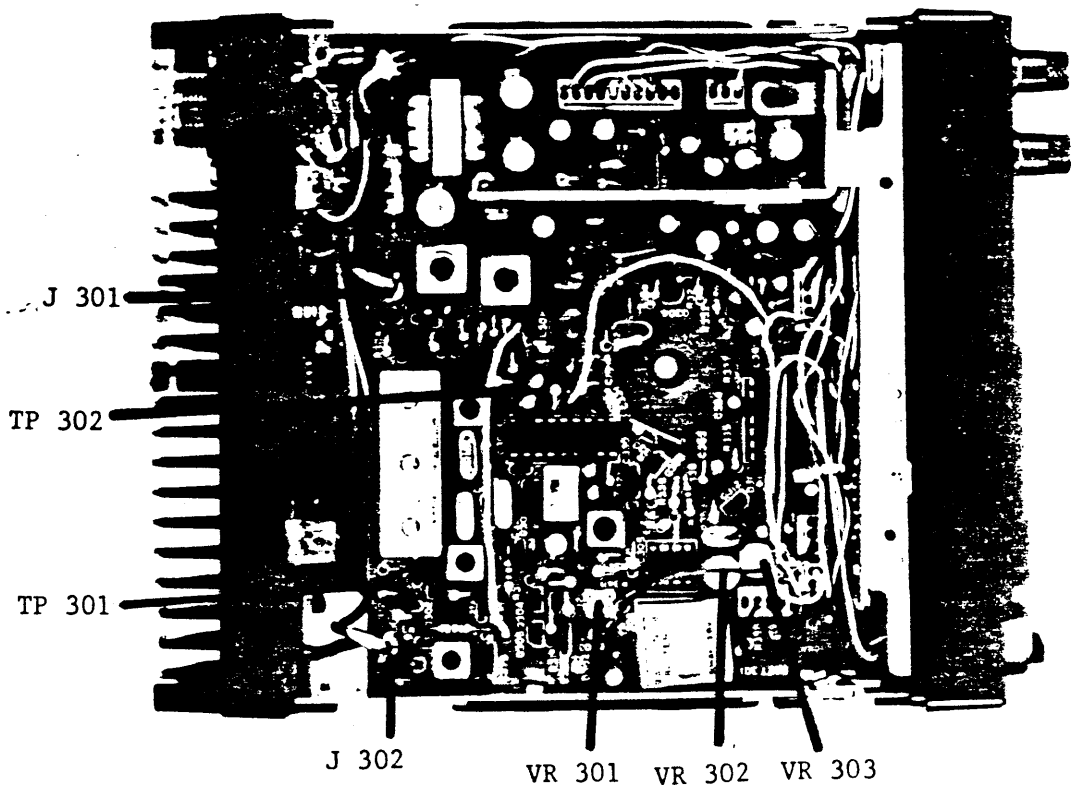


Fig. 16

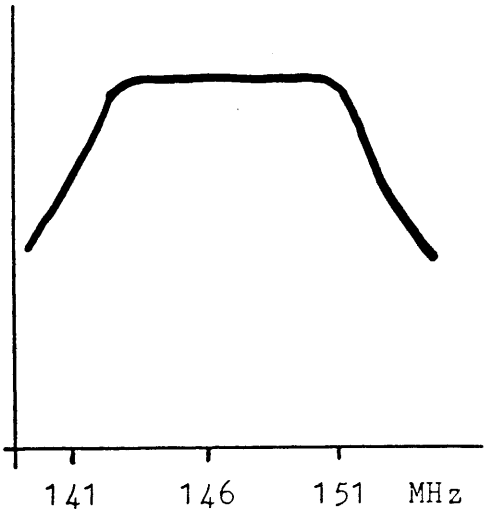


Fig. 17

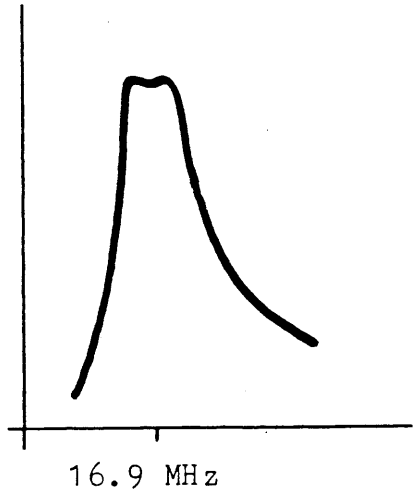


Fig. 18

and the amplitude becomes maximum.

5-3-2. IF Amplification Stage

* Connect a tracking generator to TP301.
* Connect a spectrum analyzer to TP302 via a high-impedance probe.
* Adjust L304 and L305 so that the waveform display on the spectrum analyzer becomes maximum, and closely resembles the display shown in Fig. 18.

5-3-3. Signal-strength Meter, Discriminator Adjustment

* Connect a local-oscillator signal of constant amplitude to J302.
* Connect a SSG to the antenna connector.
* Connect a dummy load of 8 ohms to the speaker jack, and connect an AC voltmeter across this dummy load. Set the volume control to the 12 o'clock position.
* Set the frequency to 6.000 (5.000 for European model).
* Set the SSG output to 146.000 MHz (145.000 for European model), 10 dBf, modulation frequency 1 kHz, and deviation ±3.5 kHz.
* Adjust VR301 so that four LEDs of the signal-strength meter are illuminated.
* Adjust L306 for maximum indication on the voltmeter.

5-3-4. Adjustment of Scan Control Circuit

* Connect a SSG to the antenna connector.
* Set the SSG output to 146.003 MHz (145.005 MHz for the European model), 20 dBf, modulation frequency 1 kHz, and frequency deviation ±3.5 kHz.
* Set the frequency of the PCS-4000 to 6.000 (5.000 for European model).
* First turn VR303 fully counterclockwise, and then turn it slowly clockwise until the BUSY LED on the front panel illuminates. Turn VR303 just a bit further clockwise after this point is reached.
* Change the SSG frequency to 145.997 MHz (144.995 MHz for European model).
* First turn VR302 fully counterclockwise. When it is then turned slowly clockwise, the BUSY LED will come on for a moment and then go out again. Turn VR302 further clockwise until the BUSY LED comes on a second time. Then turn it slightly further.
* The above procedure provides a scanning window of about ±3 kHz for the US model, and about ±5 kHz for the European model.

6. TROUBLESHOOTING

6-1. Display Malfunction

Refer to the flow chart, Fig. 19.

6-2. Insufficient Receiver Sensitivity

The second local oscillator of the PCS-4000 receiver is set to oscillate at a low level, in order to improve the suppression of spurious signals. Often, a lack of receiver sensitivity is the result of an interruption in the oscillation. Check the level of the second local oscillator first. Using a high-impedance probe at pin 2 of IC301, a voltage of 100 to 150 mV should be seen.

If this oscillator is functioning properly, localize the problem by inserting signals at various points along the receiver chain until the defective stage is found.

6-3. Hum During Reception

The dynamic signal for the display may cause hum in the receive mode if the screw near R340, on the receiver board, is loose. Tightening this screw will eliminate this problem.

6-4. Hum During Transmission

The same loose screw mentioned above may cause hum on the transmitted signal. If objectionable hum still occurs after this screw is tightened, insert a disk ceramic capacitor of 0.01 uF between the heat-dissipating fin of IC 304 (uA7805) and L302. Also, be certain that all screws holding down the circuit boards are tight.

6-5. Modulation of Transmitted Signal

With early models, serial numbers 200001 to 201000, a tone may occur on the modulated signal. To correct this, perform the modification shown in Fig. 20.

6-6. Modulation Interruption with High-level Audio Input

This condition may occur with early models, serial numbers 200001 to 201600. It may be eliminated by changing R472 from 100K to 51K. Also, solder a ceramic capacitor of 0.001 uF between pins 2 and 5 of IC402. Do not use too much capacitance or the high-range modulation characteristics may be adversely affected.

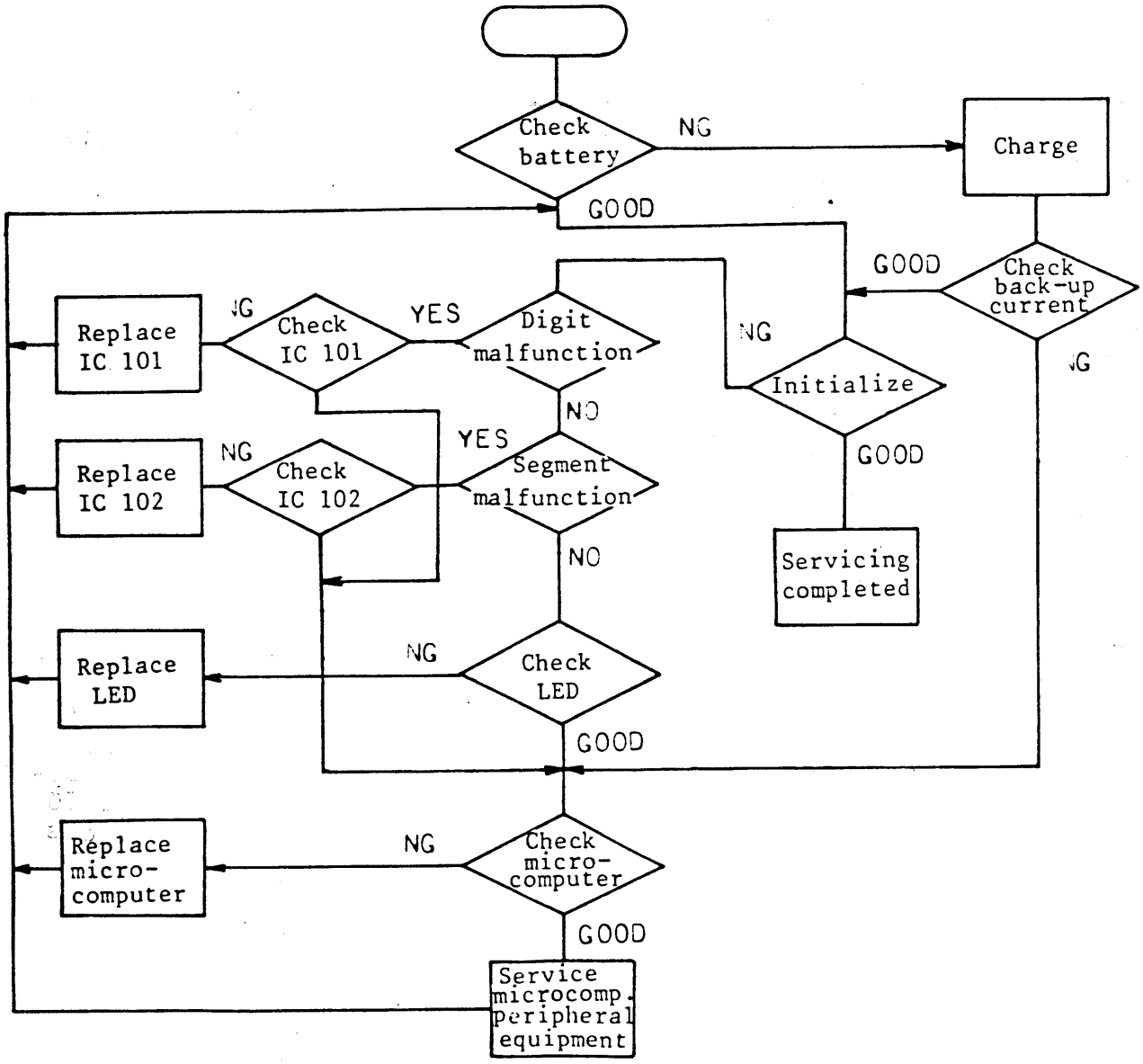

Check battery
NG
Charge
GOOD
GOOD
Check back-up current
NG
Replace IC 101
NG
Check IC 101
YES
Digit malfunction
NG
Initialize
NO
YES
Replace IC 102
NG
Check IC 102
Segment malfunction
GOOD
Servicing completed
NO
Replace LED
NG
Check LED
GOOD
Replace micro-computer
NG
Check micro-computer
GOOD
Service microcomp. peripheral equipment

Fig. 19

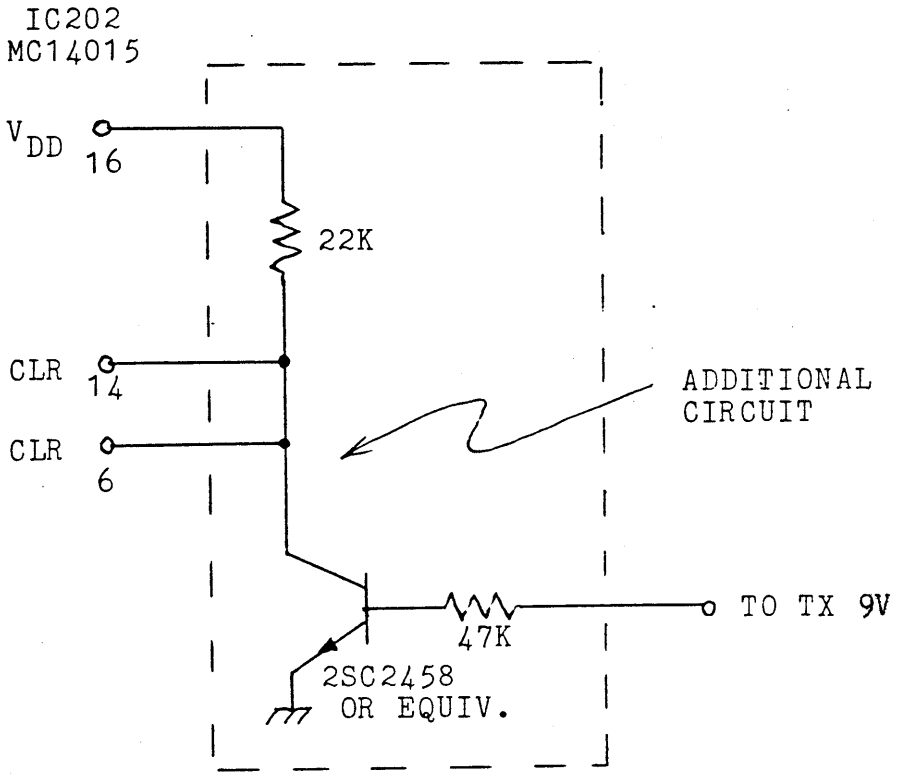


Fig. 20