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(Collins PRC-515)
Техничко Упутство

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Instruction Book

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Rockwell
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instruction book

COLLINS AN/PRC-515 RADIO SET

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Rockwell International
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INTRODUCTION

This manual contains second and third line maintenance instructions for Radio Set AN/PRC-515. It includes a description of the equipment, maintenance procedures, illustrated parts list, and schematics. Throughout the manual, common names are used for nonmenclatured items of Radio Set AN/PRC-515 and several nomenclatured accessory items. The common names are:

NOMENCLATURE	COMMON NAME
Receiver-Transmitter Group OR-5007/URC	receiver-transmitter group
Radio Receiver-Transmitter RT-5047/URC	receiver-transmitter
Receiver-Transmitter Control C-5310/URC	control
Amplifier-Coupler AM-5280/URC	amplifier-coupler
Storage Battery BB-706/U	battery
Radio Set Harness MT-5167/PRC-515	pack frame
Antenna AS-5093/PRC-515	whip antenna
Handset H-5017/GR	handset
Headset-Microphone H-5016/PRC-515	headset
Electrical Power Cable Assembly CX-5229/PRC-515	battery cable
Battery Charger PP-5267/U	battery charger
Direct Current Generator G-5002/PRC-515	generator
Telegraph Key KY-5033/PRC-515	telegraph key
Antenna AS-5094/PRC-515	dipole antenna
Antenna Counterpoise AS-5095/PRC-515	antenna counterpoise

Additional manuals that support Radio Set AN/PRC-515 include:

Radio Set AN/PRC-515 Operator's Manual

Radio Test Set AN/PRM-501

Radio Test Set AN/PRM-502

Battery Charger PP-5267/U Maintenance Manual

SECTION I

DESCRIPTION

1.1 PURPOSE

Radio Set AN/PRC-515 (figure 1-1) is a backpack, single-sideband, high-frequency receiver-transmitter that provides tactical voice and CW communications in the 2.0000- to 29.9999-MHz frequency range with a channel spacing of 100 Hz.

1.2 EQUIPMENT SUPPLIED

Equipment supplied as part of Radio Set AN/PRC-515, is shown in figure 1-2, and is listed in table 1-1.

1.3 ACCESSORY EQUIPMENT

Accessory equipment available for use with Radio Set AN/PRC-515 is shown in figure 1-3 and is listed in table 1-2.

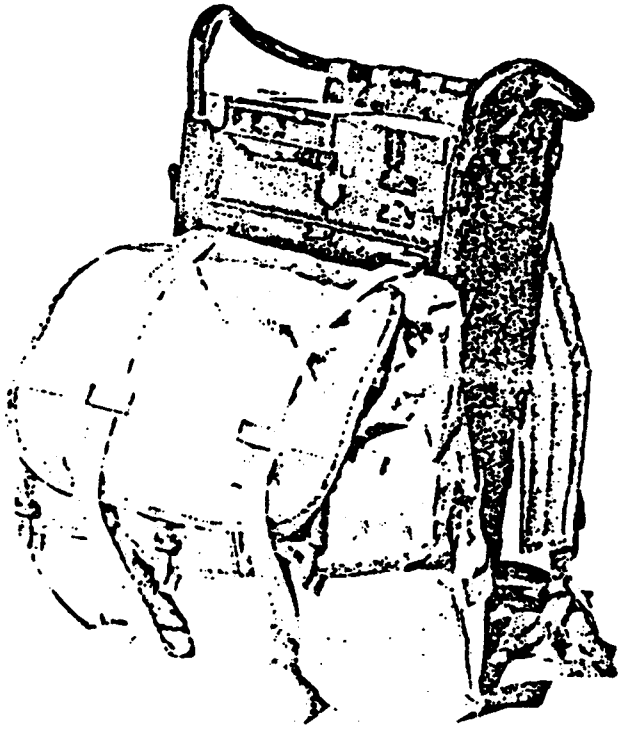
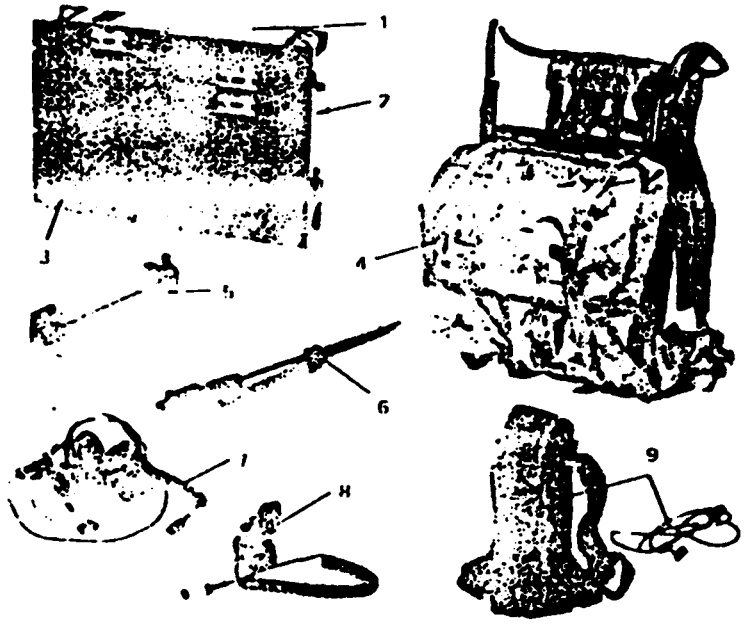


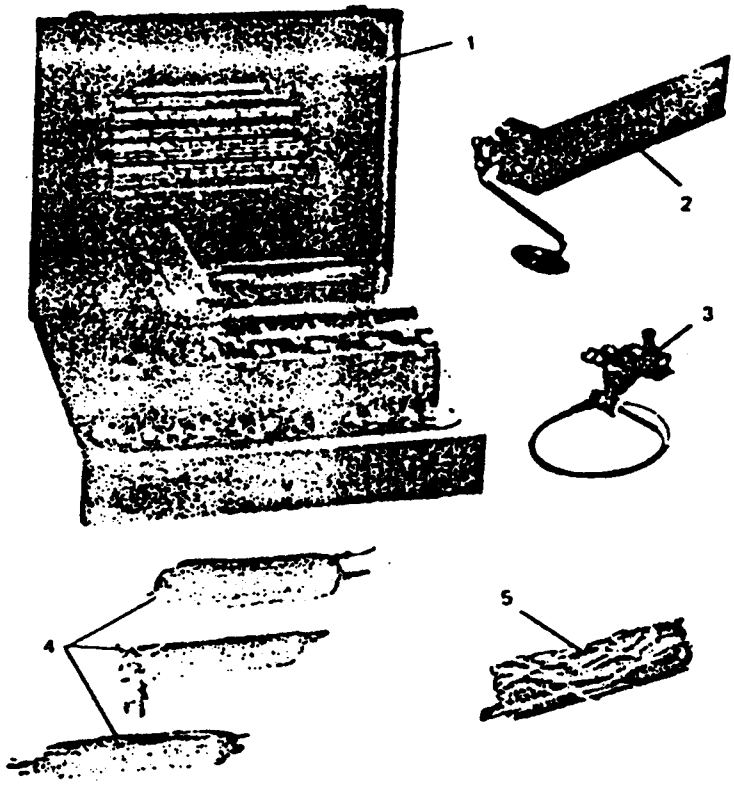
Figure 1-1. Radio Set AN/PRC-515



1. RECEIVER-TRANSMITTER CONTROL C-5310/URC
2. RADIO RECEIVER-TRANSMITTER RT-5047/URC
3. AMPLIFIER-COUPLER AM-5280/URC
4. RADIO SET HARNESS MT-5167/PRC-515
5. STORAGE BATTERY BB-706/U
6. ANTENNA AS-5093/PRC-515
7. HEADSET-MICROPHONE H-5016/PRC-515
8. HANDSET H-5017/GR
9. ELECTRICAL POWER CABLE ASSEMBLY CX-5229/PRC-515

TPA-0797-017

Figure 1-2. Equipment Supplied



1. BATTERY CHARGER PP-5267/U
2. DIRECT CURRENT GENERATOR G-5002/PRC-515
3. TELEGRAPH KEY KY-5033/PRC-515
4. ANTENNA AS-5094/PRC-515
5. ANTENNA COUNTERPOISE AS-5095/PRC-515

TPA-0298-017

Figure 1-3. Accessory Equipment

QTY	NOMENCLATURE	COLLINS PART NUMBER
*1	Radio Receiver-Transmitter RT-5047/URC	622-2148-002
*1	Receiver-Transmitter Control C-5310/URC	622-2553-003
*1	Amplifier-Coupler AM-5280/URC	622-2149-001
2	Storage Battery BB-706/U	629-5703-001
1	Radio Set Harness MT-5167/PRC-515	629-3425-002
1	Antenna AS-5093/PRC-515	629-5702-001
1	Handset H-5017/GR	637-1952-001
1	Headset-Microphone H-5016/PRC-515	635-5148-001
1	Electrical Power Cable Assembly CX-5229/PRC-515	629-3428-001

*These items make up Receiver-Transmitter Group OR-5007/URC (Collins part number 622-1407-002).

Table 1-1. Equipment Supplied

NOMENCLATURE	COLLINS PART NUMBER
Battery Charger PP-5267/U	629-3416-003
Direct Current Generator G-5002/PRC-515	629-3415-001
Telegraph Key KY-5033/PRC-515	637-1949-001
Antenna AS-5094/PRC-515	622-3073-001
Antenna Counterpoise AS-5095/PRC-515	629-5896-001

Table 1-2. Accessory Equipment

1.4 EQUIPMENT SPECIFICATIONS

Frequency range	2 to 29.9999 MHz in 0.1-kHz increments.
Modes	Upper sideband (USB), amplitude modulation equivalent (AM), and continuous wave (CW).
Power output	20 watts (high power) or 2 watts (low power) nominal peak envelope or average power into 50 ohms with 1.3:1 vswr.
Duty cycle	Continuous for 12-hour period at 1:9 transmit voice/receive ratio using one Storage Battery BB-706/U
Tuning time	4 seconds nominal and 7 seconds maximum (after frequency selection is made).
Receiver sensitivity	
USB	-113 dB mW, 50-ohm rf input for a signal + noise/noise ratio of not less than 10 dB.
AM	-102 dB mW, 30% modulated, 50-ohm rf input for a signal + noise/noise ratio of not less than 10 dB.
Audio input	-56 to -26 dB mW into 600 ohms to develop rated rf output.
Audio output	10 mW into 600 ohms, adjustable with volume control.
Primary power	22 to 30 V dc (25.2 V dc nominal), 60 watts nominal on transmit CW and 1.5 watts nominal on receive (provided by Storage Battery BB-706/U).
Total weight	12.7 kg (28 lb).
Temperature range	
Operating	-54 to +65°C (-65.2 to +149°F).
Storage	-60 to +75°C (-76 to +167°F).
Operating altitude	3,048 metres (10,000 feet).
Operating humidity	95 percent relative humidity.

1.5 EQUIPMENT DESCRIPTION

1.5.1 Receiver-Transmitter Group OR-5007/URC

Receiver-Transmitter Group OR-5007/URC is a compact lightweight receiver-transmitter consisting of three units: Radio Receiver-Transmitter RT-5047/URC, Receiver-Transmitter Control C-5310/URC, and Amplifier-Coupler AM-5280/URC. When mechanically latched together, these units are electrically connected through mating connectors. All operating controls are located under a hinged cover on the control.

1.5.2 Storage Battery BB-706/U

Storage Battery BB-706/U is a rechargeable nickel-cadmium 1.8-Ah battery that latches beneath the receiver-transmitter group. It supplies dc power for 12 hours of operation at a 1:9 transmit voice/receive duty cycle.

1.5.3 Radio Set Harness MT-5167/PRC-515

Radio Set Harness MT-5167/PRC-515 is a lightweight, rugged pack frame with adjustable straps. It can hold, simultaneously, a receiver-transmitter group, a battery, and either a Direct Current Generator G-5002/PRC-515 or a spare battery. The field pack, part of the pack frame, has compartments to store all the accessory items except the battery charger.

1.5.4 Antenna AS-5093/PRC-515

Antenna AS-5093/PRC-515 is a 2.4-metre (8-foot) whip antenna that can be easily folded for storage. It has a shock absorbing mount and detent positioning device capable of ±90° front-to-back movement in 45° increments.

1.5.5 Handset H-5017/GR

Handset H-5017/GR has an earpiece, a microphone, a push-to-talk (ptt) switch, and connects to the control by means of a coiled cord.

1.5.6 Headset-Microphone H-5016/PRC-515

Headset-Microphone H-5016/PRC-515 has two earpieces, a boom microphone, a ptt switch, a headband, and connects to the control by means of a coiled cord.

1.5.7 Electrical Power Cable Assembly CX-5229/PRC-515

The CX-5229/PRC-515 is a 1.5-metre (5-foot) cable and a canvas bag with an adjustable shoulder strap. It allows the battery to be carried under the operator's outer clothing during very cold weather.

1.5.8 Battery Charger PP-5267/U

Battery Charger PP-5267/U is a portable battery charger that will discharge and charge six batteries simultaneously. It operates from either 28-V dc or 110-V ac power source.

1.5.9 Direct Current Generator G-5002/PRC-515

Direct Current Generator G-5002/PRC-515 is a hand-operated generator that can be latched between the receiver-transmitter group and the battery to extend operating time indefinitely.

charging rates are indicated by lamps; green for normal operation and red for high charging rate.

1.5.10 Telegraph Key KY-5033/PRC-515

Telegraph Key KY-5033/PRC-515 is adjustable in tension and gap and connects to the control by means of a 0.9-metre (3-foot) flexible cord and connector. The telegraph key can be attached to the operator's thigh with a strap.

1.5.11 Antenna AS-5094/PRC-515

Antenna AS-5094/PRC-515 is a dipole antenna that consists of two 35.67-metre (117-foot) braided wires, wrapped on individual plastic bobbins, and allows long-range communications. Each wire has a 30.48-metre (100-foot) throwing line attached. The two wires are connected to a center junction, which is connected to the receiver-transmitter with a 15.25-metre (50-foot) coaxial feeder line.

1.5.12 Antenna Counterpoise AS-5095/PRC-515

The AS-5095/PRC-515 provides a ground plane in low electrical conductivity areas. It consists of four 10-metre (32.8-foot) braided wires and a 1.8-metre (6-foot) feeder cable connected to a center junction. The wires and feeder cable are wrapped on a plastic bobbin for storage.

1.6 OPERATING CONFIGURATIONS AND OPTIONS

1.6.1 Standard Configuration

The standard configuration consists of the receiver-transmitter group and the battery installed in the pack frame. The whip antenna is connected to the antenna connector on the amplifier-coupler, and the handset or the headset is connected to one of the audio connectors on the control. For CW operation, the telegraph key is connected to one of the audio connectors. This configuration is used for missions of up to 12 hours operating time and communications distances up to 25 kilometres (15.5 miles).

1.6.2 Spare Battery Option

When missions of up to 24 hours operating time are required, a spare battery is latched to the bottom of the operational battery. The spare battery is not electrically connected to the system. When the operating battery is discharged, it is interchanged with the spare.

1.6.3 Generator Option

For cases of isolated or extended missions, a generator can be used to maintain battery charge. The generator connects between the receiver-transmitter group and the battery. A clip on the pack frame secures the generator crank.

1.6.4 Cold Weather Configuration

During cold weather of 0°C (32°F) and colder, the battery must be kept warm to obtain sufficient mission time. The battery cable allows the battery to be removed from the receiver-transmitter group and to be carried in a battery bag under the operator's outer clothing.

1.6.5 Antenna Options

In dry or rocky terrain of low electrical conductivity, the antenna counterpoise provides a ground plane for the whip antenna. The four braided wires of the antenna counterpoise are laid out on the ground, and the feedline connector is plugged into the coaxial BNC connector on the amplifier-coupler.

For extended communications ranges, the whip antenna is replaced with the dipole antenna. The dipole antenna can be erected using available structures such as buildings or trees. Each end of the dipole terminates in a bobbin that allows adjustment of the length. Marking on the braided wire facilitates selection of the proper length for the desired operating frequency. The antenna feedline is plugged into the coaxial BNC connector on the amplifier-coupler.

1.7 PRINCIPLES OF OPERATION

Figure 1-4 is a block diagram of Radio Set AN/PRC-515, including optional accessory items and figure 1-5 is a block diagram of the receiver-transmitter group.

1.7.1 Receive Functional Theory

The receiver-transmitter group is in the receive mode whenever the push-to-talk (ptt) or CW key line is open. In the receive mode, the receive-transmit relays in power amplifier A3A4 and broadband amplifier A1A3 bypass these amplifiers and connect the antenna rf signal to mixer A1A2 where it is converted to a 5-MHz if signal.

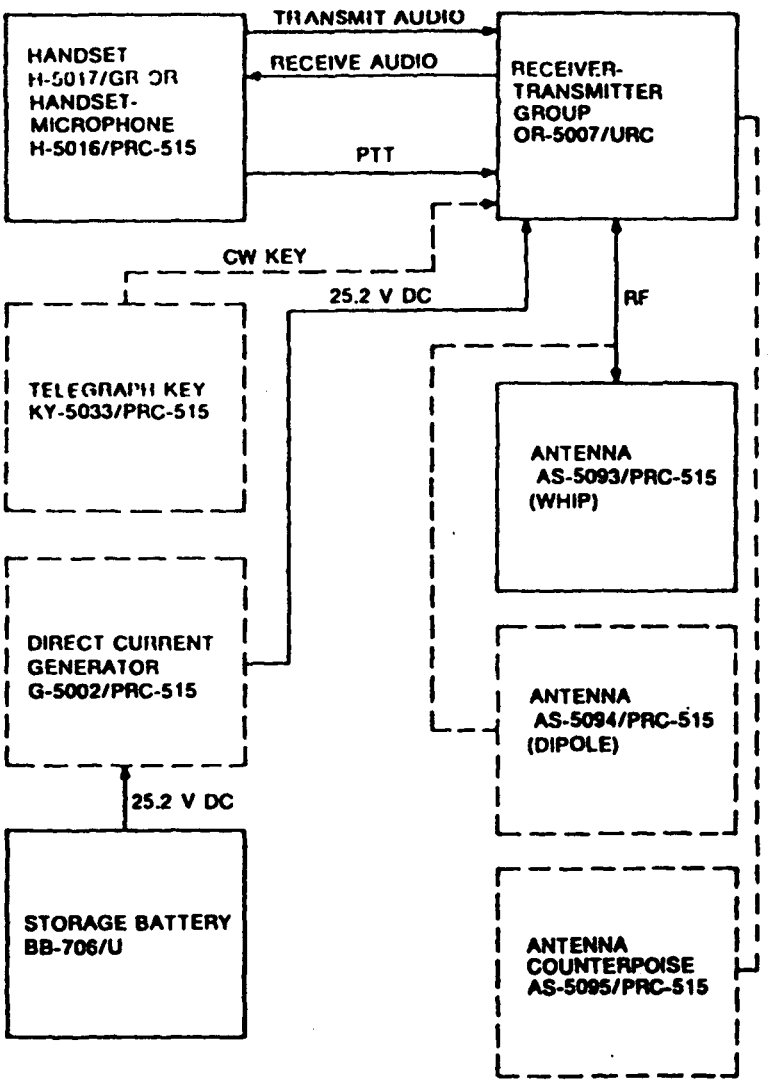
Mixer A1A2 consists of two mixer circuits and a 115-MHz filter. The first mixer circuit mixes the rf signal with a variable injection signal (117 to 145 MHz) from frequency synthesizer A1A6. The variable injection frequency is controlled by frequency selectors on the control. The output of the first mixer is passed through a 115-MHz bandpass filter to the second mixer. In the second mixer the 115-MHz if signal is mixed with a 110-MHz injection signal to produce a 5-MHz if signal. The 5-MHz if signal is fed to if/af amplifier A1A5 where it is converted to an audio signal.

If/af amplifier A1A5 performs USB or AM detection depending on the position of the MODE selector on the control. The detection circuits receive a 5-MHz injection signal from frequency synthesizer A1A6. The volume control on the control sets the audio input level of A1A5. The receive audio A1A5 is coupled through a filter in the control and is parallel connected to the two audio connectors on the control.

1.7.2 Transmit Functional Theory

The receiver-transmitter group is in the transmit mode whenever the ptt or CW key line is closed. During CW operation, a delay circuit in A1A5 maintains the transmit mode during normal CW key open periods (1 second maximum).

On voice operation, the transmit audio signal is passed through a filter in the control to if/af amplifier A1A5 in the radio receiver-transmitter. In A1A5, the voice signal is amplified and applied to a balanced modulator. The balanced modulator uses a 5-MHz injection signal from frequency synthesizer A1A6 to produce a 5-MHz double-sideband signal, which is passed through a SSB filter to produce a single-sideband (SSB) signal. In AM, the 5-MHz carrier is reinserted after the SSB filter to produce an equivalent AM signal consisting of the SSB signal and a 5-MHz carrier.



NOTE:
BROKEN LINES INDICATE OPTIONAL ACCESSORY ITEMS.

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Figure 1-4. Radio Set AN/PRC-515, Block Diagram

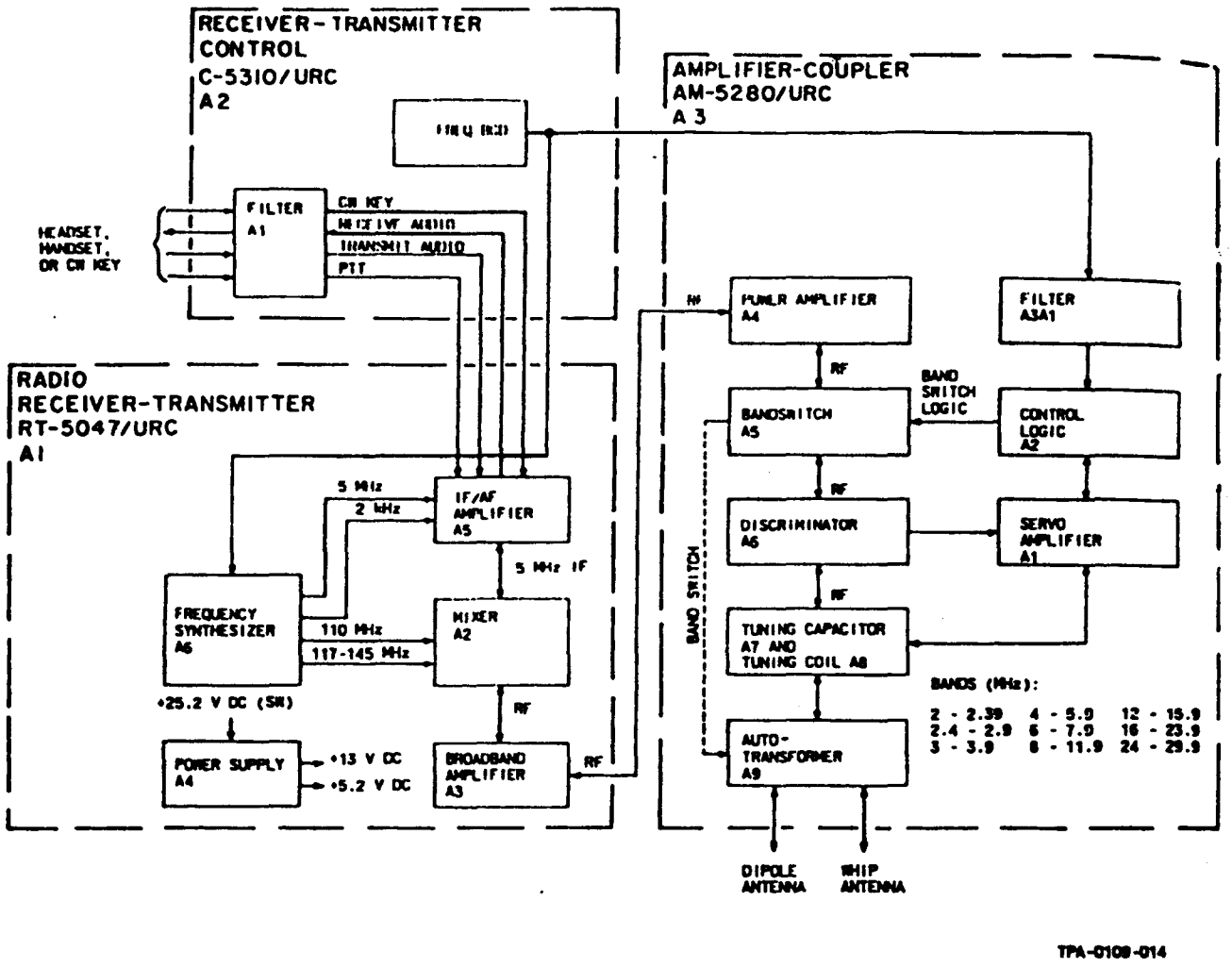

Figure 1-5. Receiver-Transmitter Group or OR -5007/URC, Block Diagram

On CW operation, the CW key line is filtered in the control and applied to if/af amplifier A1A5 in the radio receiver-transmitter. A CW keying circuit in A1A5 applies a keyed 2-kHz signal to the input of the balanced modulator. The 2-kHz signal is obtained from frequency synthesizer A1A6.

Mixer A1A2 converts the 5-MHz voice or CW if signal to an rf signal of the desired frequency. Mixer A1A2 consists of two mixers and a 115-MHz bandpass filter. In the first mixer circuit, the 5-MHz if signal is mixed with a 110-MHz injection signal from frequency synthesizer A1A6. The output of this mixer is fed through a 115-MHz bandpass filter to the second mixer. In the second mixer, the 115-MHz if signal is mixed with a variable injection frequency (117 to 145 MHz) from frequency synthesizer A1A6 to produce the desired rf signal frequency. The variable injection frequency is controlled by frequency selectors on the control.

The output of mixer A1A2 is amplified to approximately 250 mW by broadband amplifier A1A3 and applied to power amplifier A3A4. Power amplifier A3A4 amplifies the output to 2 watts or 20 watts depending upon the setting of the POWER/PUISSANCE switch on the control. The output of power amplifier A3A4 is fed through bandswitch A3A5, discriminator A3A6, tuning capacitor A3A7, tuning coil A3A8, and autotransformer A3A9 to the antenna. When connected, the whip antenna is used. When the whip antenna is disconnected, a switch in the amplifier-coupler selects the dipole antenna.

1.7.3 Tuning Functional Theory

Whenever power is turned on or a new frequency is selected, the control applies a rechannel pulse to if/af amplifier A1A5. If/af amplifier A1A5 processes the rechannel pulse and applies it to frequency synthesizer A1A6 and control logic A3A2. Frequency synthesizer A1A6 generates a new variable injection frequency based on binary coded decimal (bcd) information received from the frequency selectors on the control. Control logic A3A2 also receives bcd frequency information from the selector switches and provides band-switching information to bandswitch A3A5. During synthesizer frequency changing and band switching, the transmit circuit is disabled. When band switching is complete, control logic A3A2 advances to a standby condition. In this condition, frequency synthesizer A1A6 and bandswitch A3A5 are tuned to the new frequency, but tuning capacitor A3A7 and tuning coil A3A8 are tuned to the old frequency. The receive circuits are operational, but the transmit circuits are disabled.

Final tuning is initiated by momentarily pressing the ptt switch or the CW key. Control logic A3A2 now advances to the tune state and (1) a 2-kHz audio tone is applied to the operator's headset; (2) a transmit signal at the selected frequency is supplied to the amplifier-coupler for tuning; (3) the transmitter is keyed; and (4) tuning capacitor A3A7 and tuning coil A3A8 are servo tuned to the new frequency using the output of discriminator A3A6. When vswr remains below approximately 1.3:1 for 300 milliseconds, control logic A3A2 advances to the operate state and the transmitter is unkeyed. Tuning is now complete.

During transmit operation, the vswr is continuously monitored and if it goes above 1.3:1 for more than 2 seconds, a retune cycle is initiated. In retune, the servo amplifiers are enabled and the servo motors are driven by discriminator phasing and loading inputs, derived from the transmitter voice envelope, until the vswr is below 1.3:1 for more than 300 milliseconds.

Transmit operation is checked by a tune incomplete monitor circuit in control logic A3A2. A fault condition occurs if (1) the tune or retune cycle is not completed or (2) the rf voltage at the junction of the tuning coil and tuning capacitor exceeds 850 volts peak. When a fault condition occurs, tuning stops, the transmit circuit is disabled, and an interrupted 2-kHz tone (beeping) is applied to the operator's headset. A tune incomplete condition is reset by rechanneling the frequency selectors on the control.

1.7.4 Receiver-Transmitter Group OR-5007/URC Detailed Theory

1.7.4.1 Receiver-Transmitter Control A2, C-5310/URC

Refer to figure 4-14, schematics section of this manual. When Receiver-Transmitter Control C-5310/URC (control) is mechanically latched to Radio Receiver-Transmitter RT-5047/URC (receiver-transmitter), connector A2P1 is mated with A1A1J1 (as shown on figure 4-1, schematics section). Connectors J1 and J2 of A2 are connected in parallel to simultaneously accommodate any two of three audio I/O devices: Handset H-5017/GR, Headset-Microphone H-5016/PRC-515, and Telegraph Key KY-5033/PRC-515. The signals of the audio I/O device(s), CW KEY, PTT, RCV/XMT AUDIO, are filtered by the LC filter

network connected to each of the signal lines. The control provides OFF control for the receiver-transmitter group through mechanical linkage of a switch contact to the wiper arm of potentiometer A2R1. When A2R1 is rotated to the maximum counterclockwise (ccw) position, detent occurs (switch contact opens) and the +25.2-V dc (SW) voltage is removed from A2P1-36 and -49. Rotating A2R1 clockwise (cw) from the detent, closes the switch and applies +25.2 V dc from A2P1-24 and -30 to A2P1-36 and -49. Further rotation of A2R1 toward maximum cw increases the audio gain (AF GAIN HIGH) of the af amplifier stage of the receiver-transmitter. Rotating A2R1 ccw decreases af gain. When +25.2 V dc is switched to A2P1-36 and -49, the voltage is also applied to the lamp circuits of frequency selector switches A2S1 through A2S6. The switches are then illuminated when lamp test switch A2S7 is depressed and ground is applied. This illuminates switches A2S1 through A2S6 when the operator needs light to read the frequency or wants to make a lamp check. Frequency selection is made by actuating the appropriate switches until the desired frequency is read in the window adjacent to each switch. The frequency switches provide binary coded decimal (bcd) signals, representing the selected frequency, to which the receiver-transmitter and Amplifier-Coupler AM-5280/URC (amplifier-coupler) automatically tune. Operating modes, USB or AM, are selected by switch A2S8. An open circuit at A2P1-23 selects the AM (USB) function, whereas, a ground at A2P1-23 selects AM. Operating power level, HI PWR or LO PWR, is selected by switch A2S9. A ground at A2P1-27 places the radio in LOW POWER (2 watts) operation. An open at A2P1-27 selects LOW POWER (22 watts) operation. A rechannel signal (ground) is applied to A2P1-38 (RCP) whenever one or more of switches A2S1 through A2S6 are actuated.

1.7.4.2 Radio Receiver-Transmitter A1, RT-5047/URC

Refer to figure 1-6. The radio receiver-transmitter performs frequency translation and amplification of af to rf (transmit function) and rf to af (receive function) with five subassemblies: if/af amplifier (A1A5), mixer (A1A2), broadband amplifier (A1A3), frequency synthesizer (A1A6), and power supply (A1A4). If/af amplifier A1A5 provides af/if amplification, modulation/demodulation, if selectivity, and logic processing of control functions. Mixer A1A2 provides up and down conversion for the received or transmitted signals. Broadband amplifier A1A3 amplifies the transmit rf to approximately 250 mW to drive the power amplifier circuits of amplifier-coupler A3. Frequency synthesizer A1A6 generates and supplies injection frequencies to the mixer for up and down conversion, and carrier injection frequency and tone frequency to the if/af amplifier. Power supply A1A4 converts +25.2 volts dc (SW) into regulated +13-volt and -5.2-volt dc outputs for distribution to the other subassemblies.

1.7.4.2.1 Receiver Theory

Refer to figure 4-14, schematics section. At control A2 the operator selects either the USB or AM mode and the operating frequency. When A2 is turned on, tuning is complete, the radio is unkeyed, and receive operation of Radio Set AN/PRC-515 is in effect.

1.7.4.2.1.1 Broadband Amplifier A1A3

Refer to figure 1-7 in this section and figure 4-3 of the schematic section. The received signal is coupled from amplifier-coupler A3 through chassis A1A1 to connector A1A1J3/A1A1P1-12 and on to relay A1A3K1-A2. With the radio unkeyed, relay A1A3K1 is de-energized and relay contacts A2/A3 and B2/B3 are closed. This routes the received rf from P1-12 through the limiter and LC filter network to A1A1J3/A1A3P1-2.

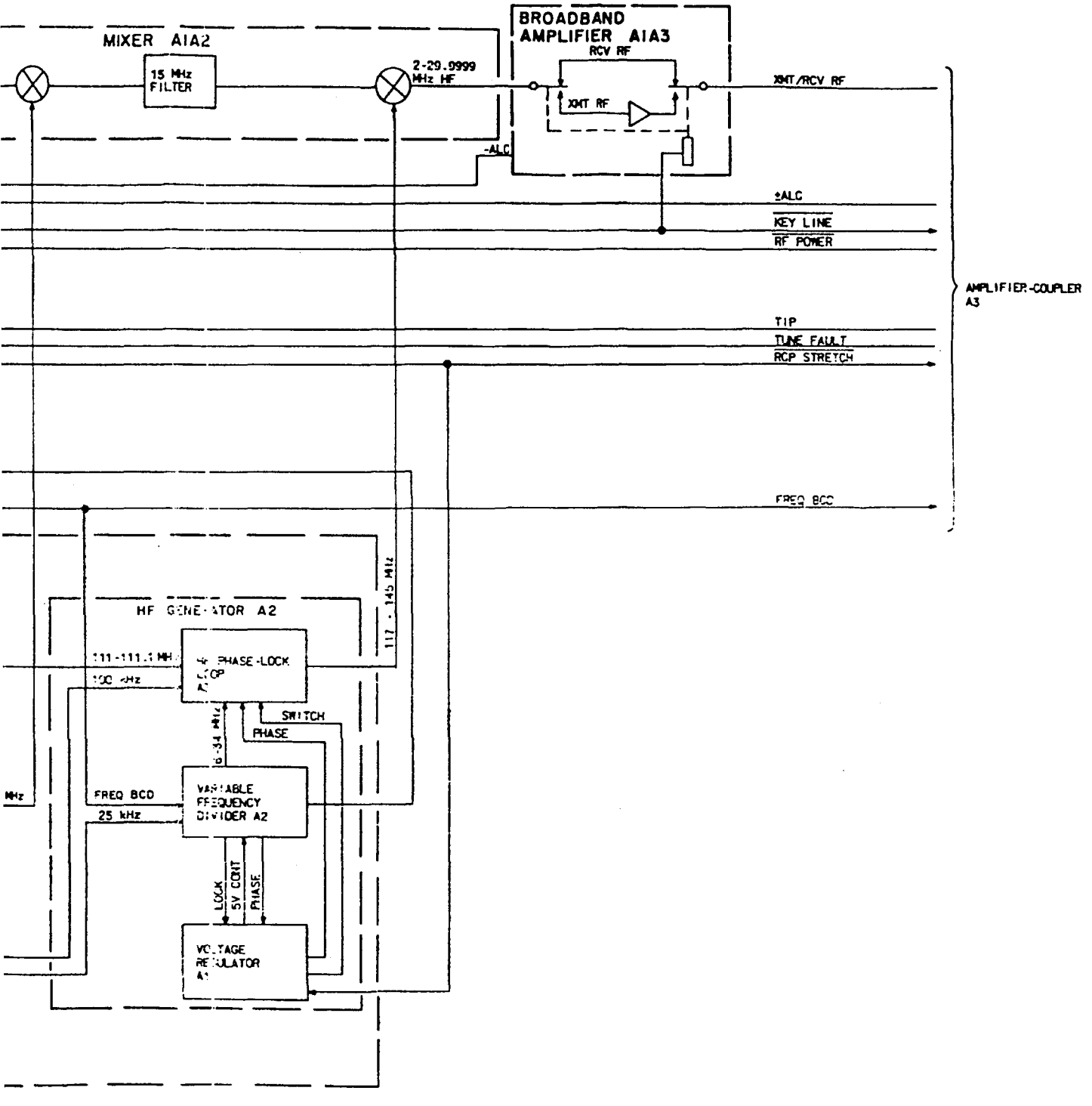

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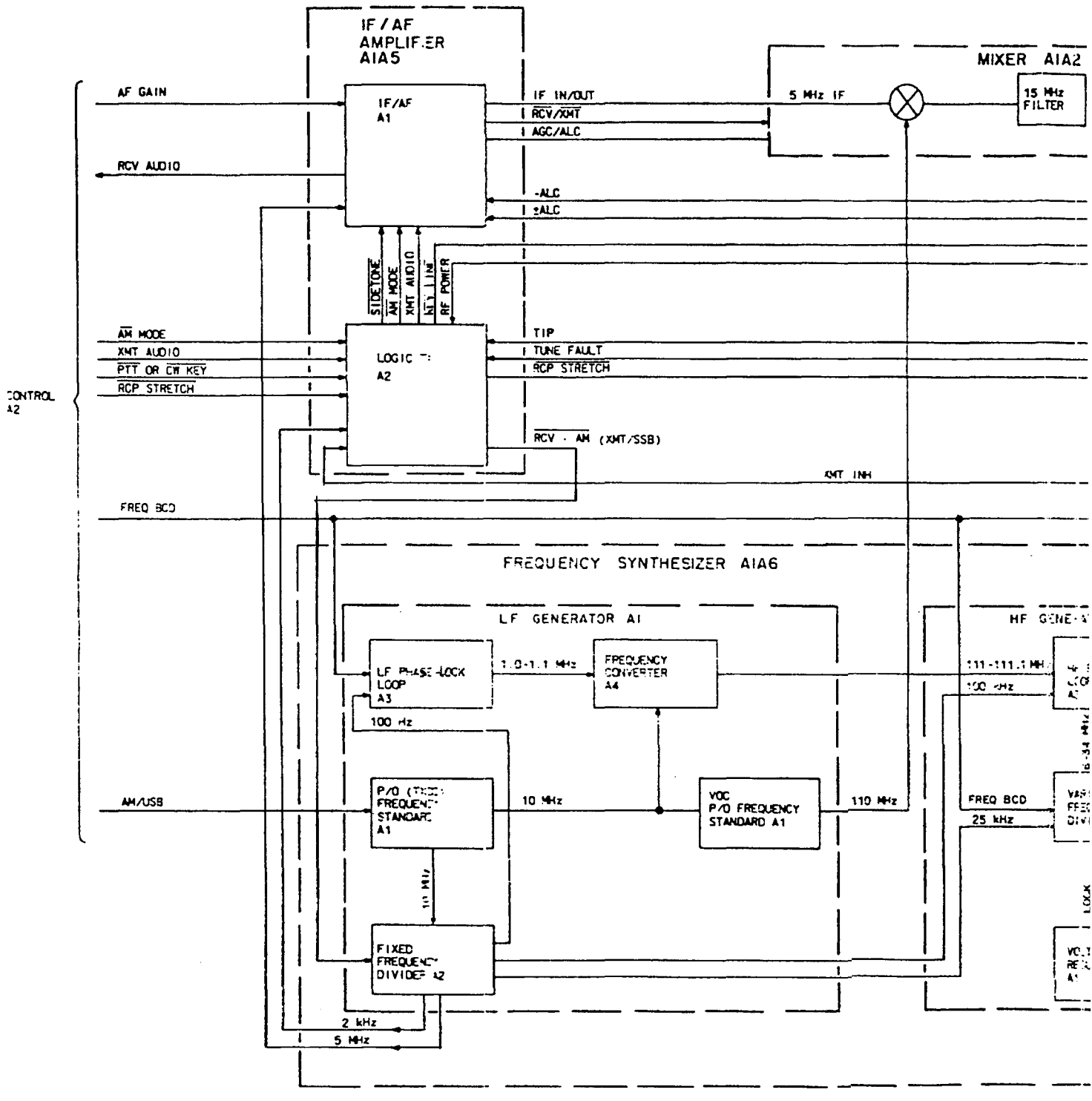
Figure 1-6. Radio Receiver-Transmitter RT-5047/URC, Block Diagram


IF / AF
AMPLIFIER
A1A5
MIXER A1A2
AF GAIN
IF/AF
A1
IF IN/OUT
RCV/XMT
AGC/ALC
5 MHz IF
15 MHz
FILTER
RCV AUDIO
-ALC
±ALC
SIDETONE
AM MODE
XMT AUDIO
RF POWER
AM MODE
XMT AUDIO
PTT OR CW KEY
RCP STRETCH
LOGIC
A2
TIP
TUNE FAULT
RCP STRETCH
RCV - AM (XMT/SSB)
XMT INH
CONTROL
A2
FREQ BCD
FREQUENCY SYNTHESIZER A1A6
LF GENERATOR A1
LF PHASE-LOCK
LOOP
A3
1.0-1.1 MHz
FREQUENCY
CONVERTER
A4
100 Hz
AM/USB
10 MHz
VOC
P/O FREQUENCY
STANDARD A1
110 MHz
FREQ BCD
25 kHz
FIXED
DIVIDER A2
2 kHz
5 MHz

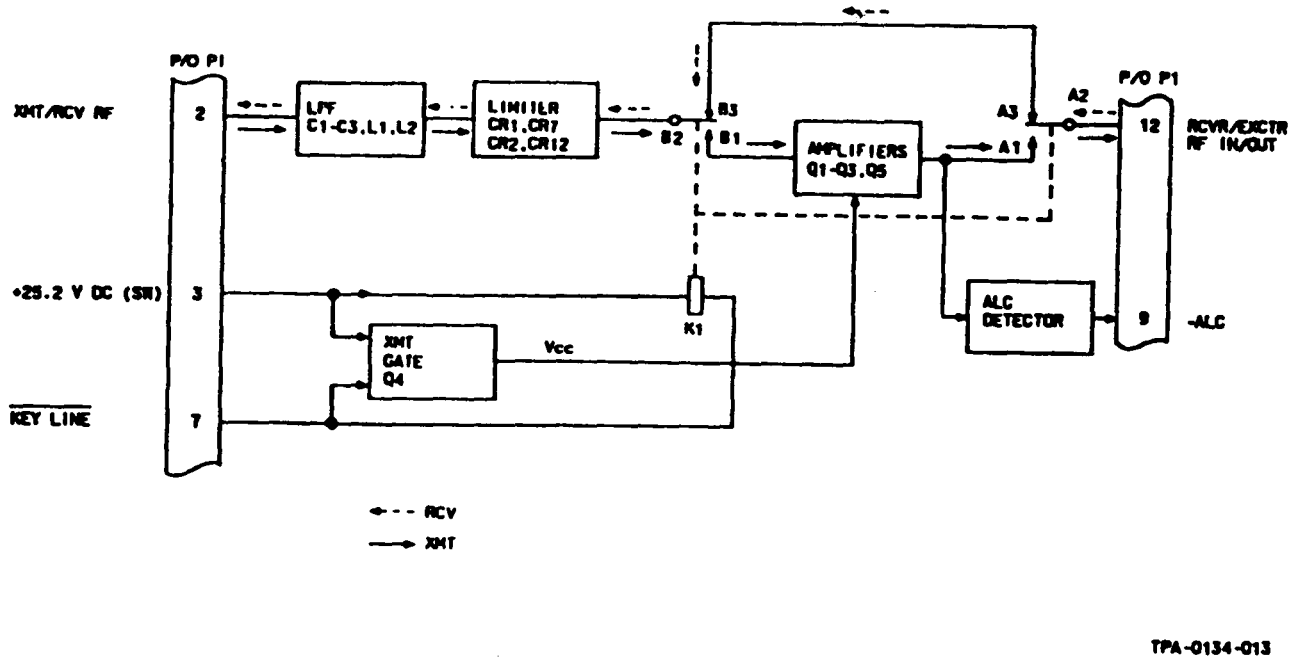


Figure 1-7. Broadband Amplifier (Receive or Transmit), Simplified Schematic Diagram

1.7.4.2.1.2 Mixer A1A2

Refer to figure 1-8 of this section and figures 4-1 and 4-2 of the schematic section. The receive rf (AM or USB) is routed by chassis wiring from broadband amplifier A1A3 to A1A1J2/A1A2P1-14. The control inputs supplied to A1A2 are $\overline{\text{XMT}}$ and $\overline{\text{RCV}}$ logic, and the AGC/ALC DRIVE from A1A5. During receive mode, RCV ($\overline{\text{XMT}}$) logic at A1A2P1-5 is high and the XMT ($\overline{\text{RCV}}$) logic at A1A2P1-6 is low. The RCV logic is applied to injection amplifier transistors Q9 and Q13, which in turn switches on diodes CR2, CR3, CR6, and CR8. The fixed and variable injection frequencies are now applied to the receive up conversion mixer Q1 and Q2 and the receive down conversion mixer Q11 and Q12. The XMT logic switches Q10 and Q14 are off, which disables both transmit mixers.

The receive rf (2-29.9999 MHz) from P1-14 passes through the low-pass LC filter, switching diode CR2, transformer T1, and on to the gates of the up conversion mixer FET's Q1 and Q2. FET's Q3 and Q4 neutralize the gate-to-drain capacity of Q1 and Q2. The receive rf is mixed with the variable injection frequency (117-144.9999 MHz) to obtain 115-MHz if, which is applied to the 115-MHz filter through diode CR3. The 115-MHz if out of the filter passes through diode CR6 and transformer T5 to the bases of down conversion mixer transistors Q11 and Q12. The 115-MHz if is mixed with fixed injection (110-MHz) to produce a 5-MHz if. The 5-MHz if (with upper and lower sidebands reversed) is coupled by transformer T6 through diode CR8 to P1-2 (IF OUT).

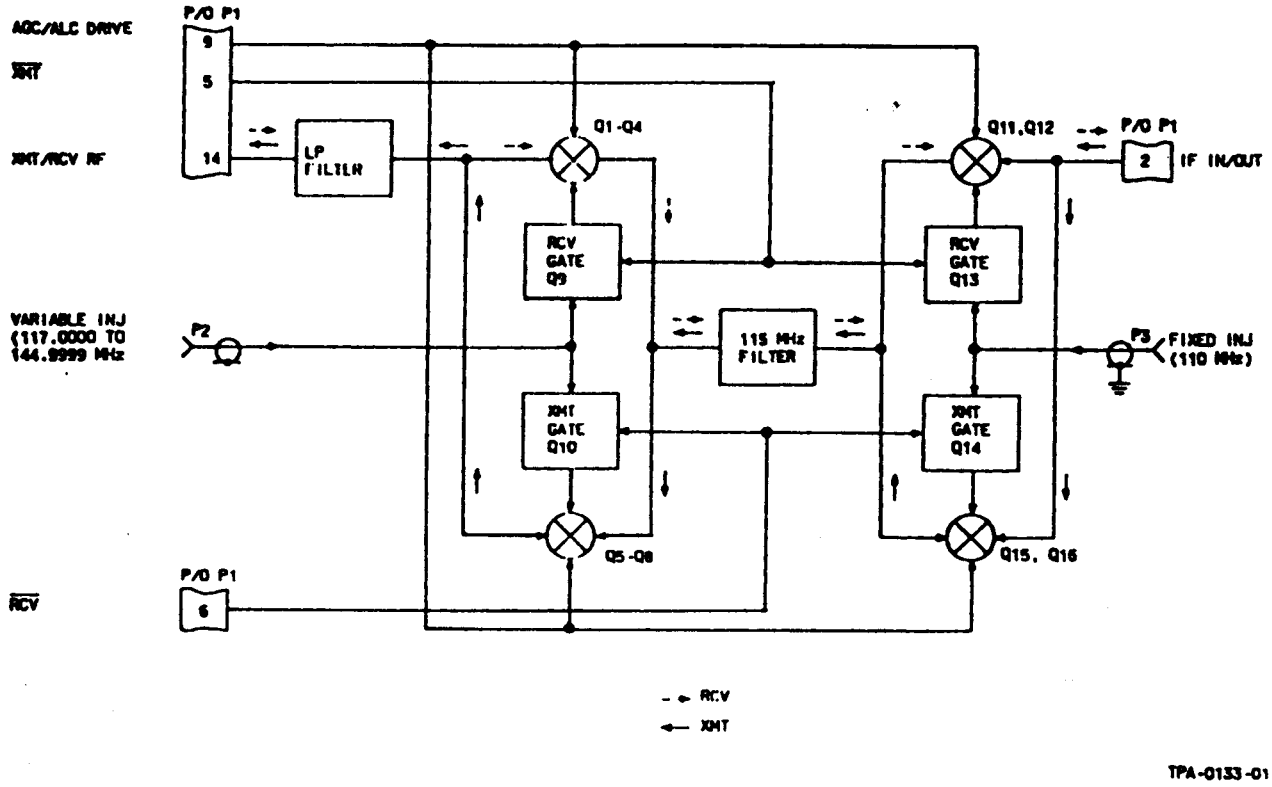


Figure 1-8. Mixer (Receive or Transmit), Simplified Schematic Diagram

When the receive rf input signals are below AGC threshold, the electron flow is through i ductors L3 and L16, bypassing diodes CR1 and CR7. As the rf input signal increases, th AGC/ALC DRIVE voltage at P1-9 decreases, permitting conduction by diodes CR1 and CI As the current of diodes CR1 and CR7 increases, the rf and if signals are shunted to ground, reducing the signal gain.

1.7.4.2.1.3 If/Af A1A5A1

a. AM Receive. Refer to figure 1-9 of this section and figures 4-1 and 4-5 of the schematic section. The IF IN signal is applied from A1A2P1/A1A1J2-2 to A1A1J5/ A1A5A1P1-2. When in AM mode, the 5-MHz if signal is coupled from A1A5A1P1-2 (IF IN), to the base of amplifier switch transistor Q2. With the radio in AM mode, $\overline{\text{RCV}}\cdot\text{AM}$ logic (ground) at P2-30 is applied to the base of transistor Q2, biasing it o and allowing the AM receive if to be applied to filter AM filter FL1 and then on to a plifier switch transistor Q19, which is also biased on by +5.2-volt logic (RCV.AM) P2-13. Transistors Q1 and Q20 are biased off during AM mode.

The receive if output of transistor Q19 passes through if amplifier transistors Q21 through Q24 on to AGC/AM audio detector transistor Q25. The detected af output o transistor Q25 is applied to the input of AM switch U3B and to the AGC hang circuit transistors Q29 through Q32. As the collector current of transistor Q32 increases transistor Q8 of the ALC/AGC DRIVE circuit, the output voltage of transistor Q6 d creases. This decrease in voltage to inductors L1, L2, and L3 permits diodes CR CR7, and CR8 to conduct, which maintains the gain of transistors Q19, Q21, and Q

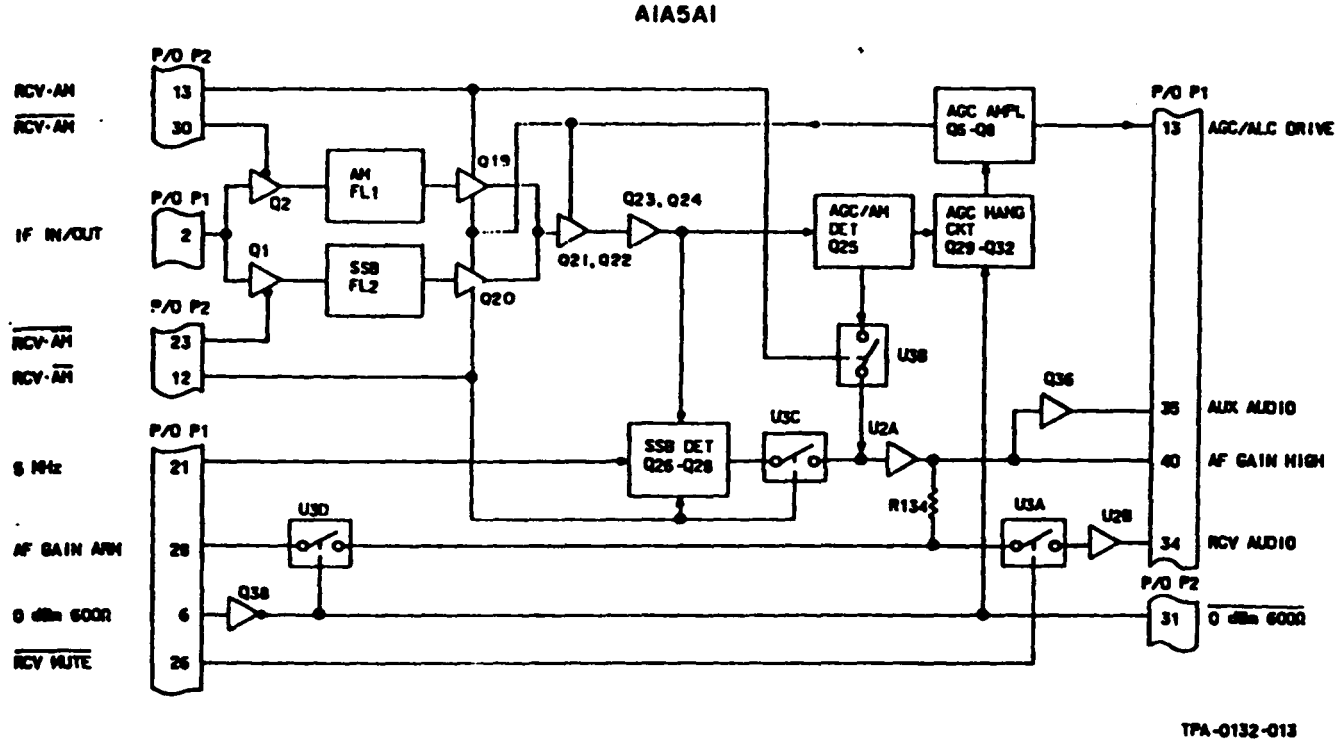


Figure 1-9. If/Af (A1A5A1) Receive, Functional Block Diagram

proportionate to the received signal level. The dc voltage output of transistor Q6 is also supplied to A1A2 from P1-13 (AGC DRIVE).

The presence of RCV·AM logic at the control element of switch U3B switches the AM receive audio to the output element of the switch. This audio is then coupled by capacitor C55 to the first audio amplifier U2A. The output of audio amplifier U2A is applied to R134, and to P1-40 (AF GAIN HIGH), which connects to variable resistor R1 (af gain) of control A2. The audio level at the input to audio mute gate, switch U3A, is controlled by A2R1 and voice/data gate, switch U3D. Switch U3A is gated by $\overline{\text{RCV MUTE}}$ logic. With the radio in normal receive operation, no tuning occurring, the $\overline{\text{RCV MUTE}}$ logic enables switch U3A and the audio is coupled by capacitor C61 to the second af amplifier U2B. The receive audio is amplified and coupled to A1A5P1/A1A1J5-34 on to A1A1J1/A2P1-43 (RCV AUDIO) for routing to the audio I/O device(s) connected to the control.

b. USB Receive. Refer to figures 4-1 and 4-5, schematics section, and figure 1-9 of this section. The 5-MHz USB receive if is applied to A1A5A1 on the same signal line that AM receive if is applied. The USB receive if is coupled to switch transistors Q1 and Q2. With Q1 gated on by $\overline{\text{RCV·AM}}$ logic (P2-23), when the radio is in USB mode, the receive if output of Q1 is direct coupled to lower sideband filter FL2 (the sidebands are inverted in A1A2 so lower sideband is the upper sideband). Then the receive if passes through transistor Q20 when $\overline{\text{RCV·AM}}$ gating logic is present. This couples the 5-MHz if to if amplifiers, transistors Q21 through Q24. The gain of transistors Q20 through Q22 is controlled by AGC/ALC DRIVE in the same manner as noted in AM receive mode of

operation. The if output of transistor Q24 is sent to AGC/AM audio detector, transistor Q25. Also, the if signal at the emitter of Q24 is coupled to transistor Q28 of the SSB detector, which is comprised of transistors Q26, Q27, and Q28. The SSB detector is switched on during USB mode by RCV·$\overline{AM}$ logic (P2-12) which is applied to the base of transistor Q27. The 5-MHz injection signal from P1-21 is coupled to the base of Q26. Mixing the injection frequency with the receive if produces the resultant USB af output from Q27 which is then coupled by capacitor C54 to switch U3C. During USB receive mode, switch U3C is closed by RCV·$\overline{AM}$ logic and the audio output of U3C is coupled to the audio amplifiers by capacitor C55. The USB audio amplifiers are the same ones that are used for AM operation.

1.7.4.2.2 Transmitter Theory

The receiver-transmitter group is ready to transmit after power is turned on, frequency and mode are selected at control A2, and tuning is complete. To transmit, enable the receiver-transmitter group keyline by (1) pressing the ptt switch on the headset or handset, or (2) by keying the telegraph key.

Refer to figures 4-1, 4-6, and 4-14 schematic section. For voice operation, the PTT signal is supplied to A1A5A2 from control A2 through the following route; A2P1/A1A1J1-39, through chassis A1A1 wiring to A1A1J5/A1A5A1P1-23, and through A1A5A1 board wiring to A1A5A1P2/A1A5A2P1-26.

For CW keying operation, the CW KEY signal is supplied to A1A5A2 from control A2 through the following route; A2P1/A1A1J1-19, through A1A1 chassis wiring to A1A1J5/A1A5A1P1-17 and through A1A5A1 board wiring to A1A5A1P2/A1A5A2P1-20.

For xmit audio (voice), the xmit audio signal is supplied to A1A5A2 from control A2 through the following route; A2P1/A1A1J1-20, through chassis A1A1 wiring to A1A1J5/A1A5A1P1-15, and through A1A5A1 board wiring to A1A5A1P2/A1A5A2P1-29.

1.7.4.2.2.1 Logic/Tx A1A5A2

Refer to figure 1-12 of this section and figure 4-6, schematics section. XMT AUDIO from P1-29 is coupled through FET Q12 to af amplifier U8B. Transistor Q14 and FET Q13 serve as a voice/data gain change stage (data is not used). The af output from amplifier U8B is applied to P1-9 and to af amplifier U8A. The audio to U8A is amplified and applied to AGC detector, transistor Q11. The AGC detector output voltage is applied to attenuators (FET's Q12 and Q15) to maintain the audio output at P1-9 at a constant level.

Figure 1-10 of this section provides a logic table for the various transmit-receive functions. In CW mode, the 2-kHz audio from P1-10 passes through gate/filter stage, FET's Q5, Q6, and Q16, and through af amplifier U8B with attenuators Q12 and Q15 at full attenuation. RC network C1 and R4 provides a delay to hold the radio in transmit mode for approximately one second after CW key is released.

The rechannel pulse signal at P1-24, which is momentary ground, causes capacitors C4 and C24 to be discharged by transistors Q3 and Q4, respectively. The output pulse at P1-33 ($\overline{RCP\ STRETCH}$) is delayed by the time constand of C4 and R18 and the pulse width is determined by C24 and R69.

1.7.4.2.2.2 If/Af A1A5A1

Refer to figure 1-10 and 1-11 in this section. The logic in transmit turns on balanced modulator U1 and transistor Q3, while biasing off transistor Q39. The XMT AUDIO from P2-9 is applied to balanced modulator U1 where it is mixed with 5-MHz from P1-21 to produce a double sideband, suppressed carrier output signal. This output signal from U1 is sent through transistor Q5, diode CR2 and SSB filter FL2.

PI PIN	INPUTS						OUTPUTS	
	PTT 26	TIP 28	CW KEY 20	RCV ONLY 15	XMT INH 22	TUNE FAULT 17	RCV 6	XMT 32
	X	X	X	X	X	0	X	0
	0	X	X	X	X	0	0	X
	X	0	X	X	X	0	0	X
	0	X	X	0	X	0	X	0
	0	X	X	X	0	0	X	0
	0	X	X	X	X	X	X	0
	X	X	0	X	X	0	0	X
	X	X	0 TO X	X	X	0	NOTE	NOTE

NOTE: WHEN CW KEY IS DISABLED THE OUTPUT STAYS AT ZERO AT PI-6 FOR APPROX. 1 SECOND.

X = MORE THAN +4.5 V
0 = LESS THAN +0.5 V

PI PIN	INPUTS			OUTPUTS				
	PTT 26	AM 19	TIP 28	13	30	27	12	23
	X	X	X	0	X	0	X	0
	0	X	X	0	X	0	0	X
	X	0	X	X	0	0	0	X
	0	0	X	0	X	X	0	X
	X	0	0	X	0	0	0	X

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Figure 1-10. Logic/Tx A1A5A2, Logic Tables

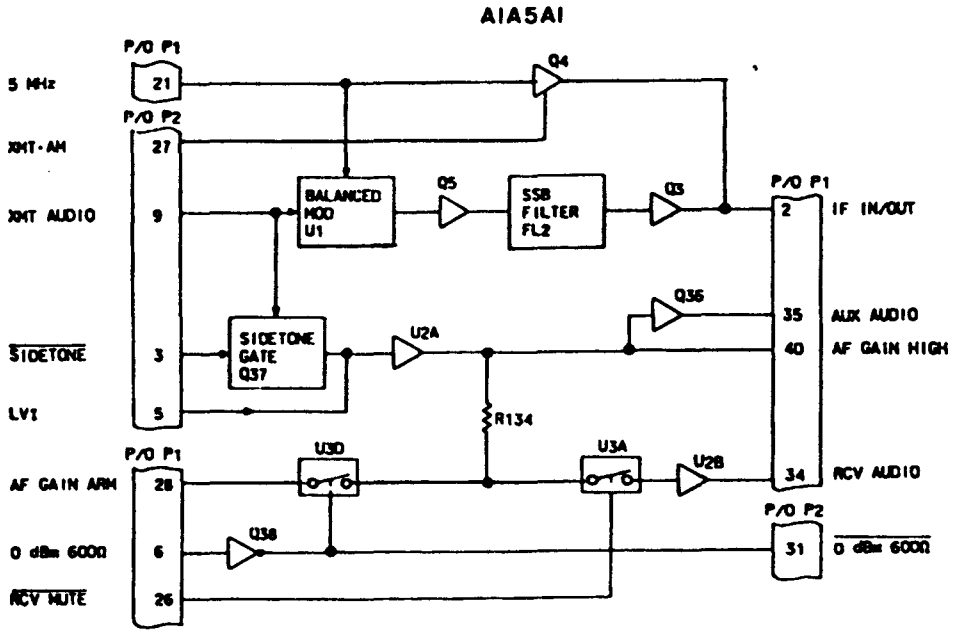


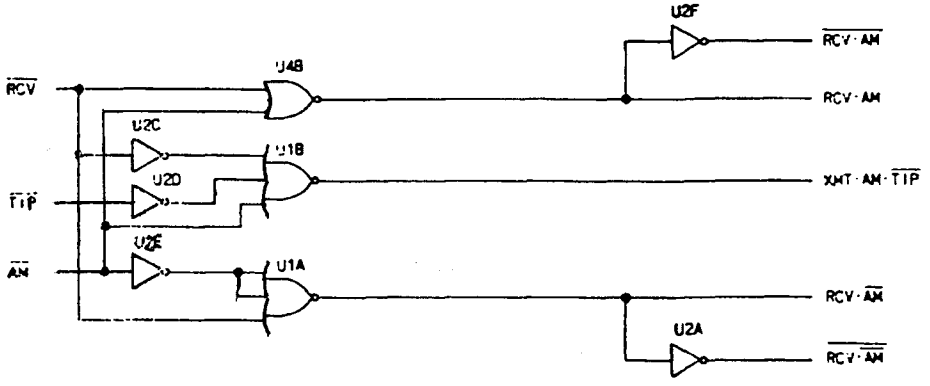
Figure 1-11. If/Af A1A5A1 (Transmit), Simplified Schematic Diagram

The if output from FL2 is amplified by transistor Q3 and coupled to P1-2 (IF OUT). If AM is selected at control A2, carrier reinsert gate, transistor Q4 and diode CR1, are gated on by logic from P2-27. This allows the 5-MHz carrier to be added to the SSB output of if amplifier Q3, producing an AM equivalent (AM) signal to P1-2.

a. Sidetone and Low Voltage Input. During transmit, the sidetone transmit audio is supplied to the headset or the handset via the receive audio circuits previously discussed. Refer to figures 1-12 and 1-13 of this section and figures 4-5 and 4-6, schematics section.

There are three conditions when the sidetone gate (FET A1A5A1Q37) is biased on: When (1) tuning is in progress (TIP) a 2-kHz tone is heard; when (2) a coupler fault occurs, a pulsating 2-kHz tone is heard; or, when (3) there is forward power output from amplifier-coupler (A3), audio is heard. In USB mode FET A1A5A1Q37 remains on for the time constant of capacitor A1A5A2C3 and resistor A1A5A2R14 (approximately 1 second) after the absence of voice audio.

The low voltage input (LVI) indication occurs when +25.2 V dc (SW) at A1A5A2P1-25 becomes less than +22.5 volts, allowing transistor A1A5A2Q1 to conduct. This causes square-wave generator A1A5A2U4A and A1A5A2U5A to oscillate. This square-wave output is coupled through R37 to A1A5A2P1/A1A5A1P2-5 and on to the audio circuits of A1A5A1 to produce a low frequency clicking sound. If a coupler fault occurs during this time, a pulsating 2-kHz tone is heard.



INPUTS		
AM	TIP	RCV
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1

OUTPUTS				
RCV·AM	RCV·AM	XMT·AM·TIP	RCV·AM	RCV·AM
0	1	0	1	0
1	0	0	1	0
0	1	0	1	0
1	0	1	1	0
1	0	0	0	1
1	0	0	1	0
1	0	0	0	1
1	0	0	1	0

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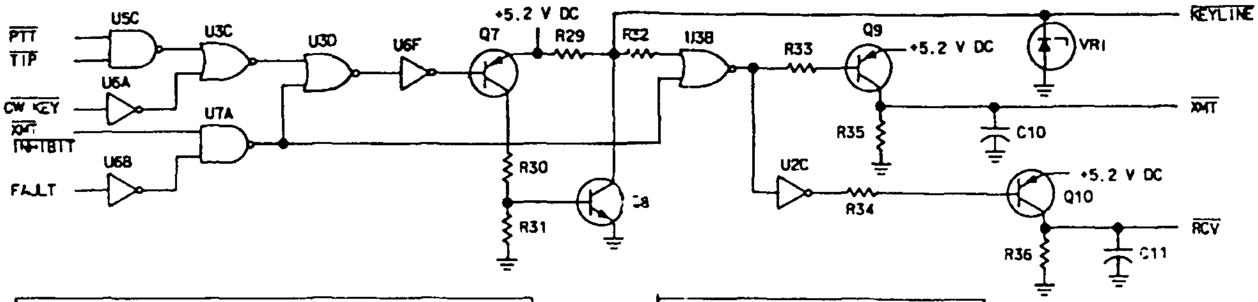
Figure 1-12. Logic/Tx A1A5A2, Simplified Schematic Diagram and Logic Tables



INPUTS				
PTT	TIP	CW KEY	XMT INHIBIT	FAULT
0	0	0	0	0
0	0	0	0	1
0	0	0	1	0
0	0	0	1	1
0	0	1	0	0
0	0	1	0	1
0	0	1	1	0
0	0	1	1	1
0	1	0	0	0
0	1	0	0	1
0	1	0	1	0
0	1	0	1	1
0	1	1	0	0
0	1	1	0	1
0	1	1	1	0
0	1	1	1	1
1	0	0	0	0
1	0	0	0	1
1	0	0	1	0
1	0	0	1	1
1	0	1	0	0
1	0	1	0	1
1	0	1	1	0
1	0	1	1	1
1	1	0	0	0
1	1	0	0	1
1	1	0	1	0
1	1	0	1	1
1	1	1	0	0
1	1	1	0	1
1	1	1	1	0
1	1	1	1	1

OUTPUTS		
KEYLINE	XMT	RCV
1	1	0
1	1	0
0	0	1
1	1	0
1	1	0
1	1	0
0	0	1
1	1	0
1	1	0
1	1	0
0	0	1
1	1	0
1	1	0
1	1	0
0	0	1
1	1	0
1	1	0
1	1	0
0	0	1
1	1	0
1	1	0
1	1	0
0	0	1
1	1	0
1	1	0
1	1	0
0	0	1
1	1	0
1	1	0
1	1	0
1	1	0
1	1	0

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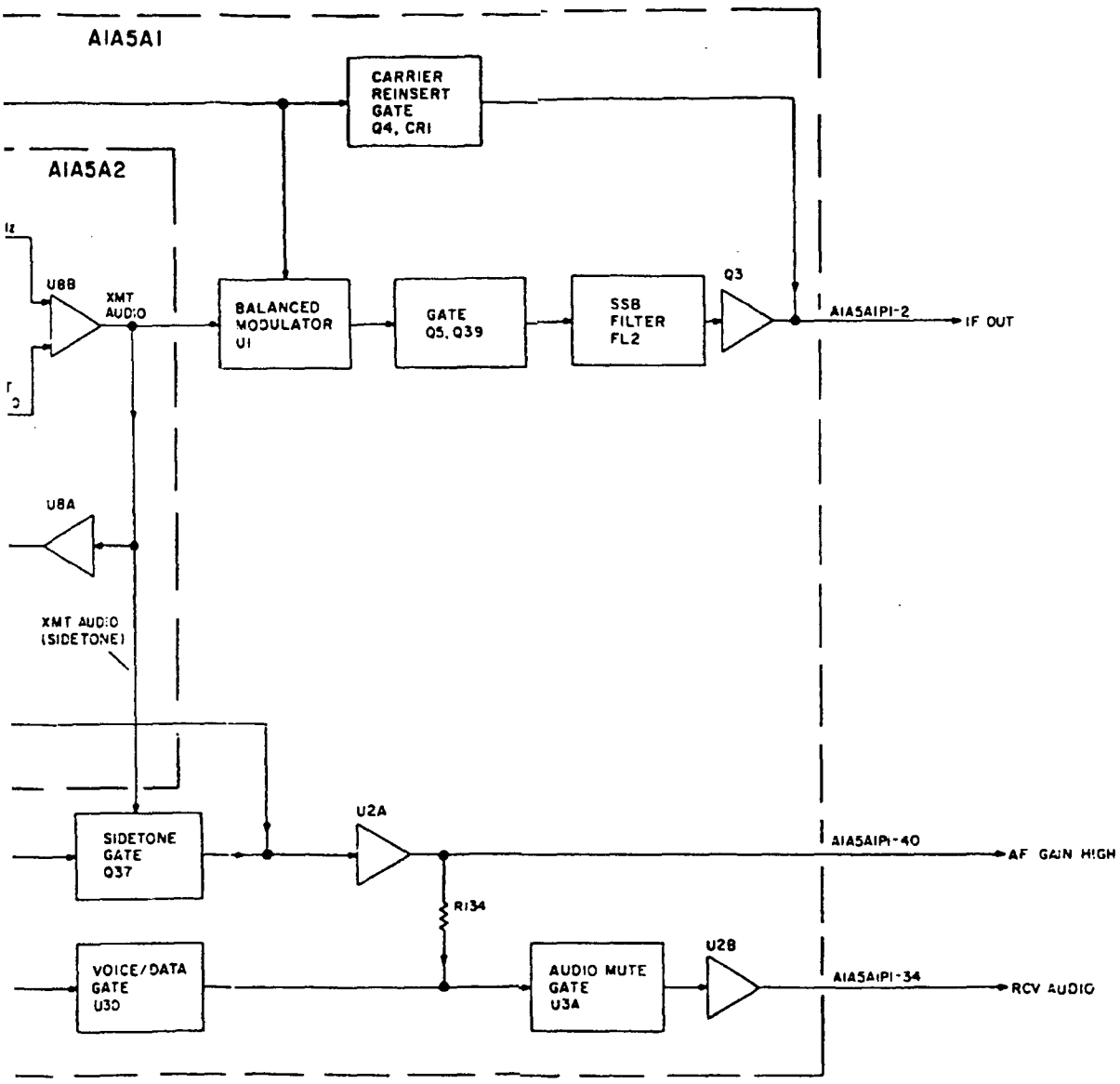

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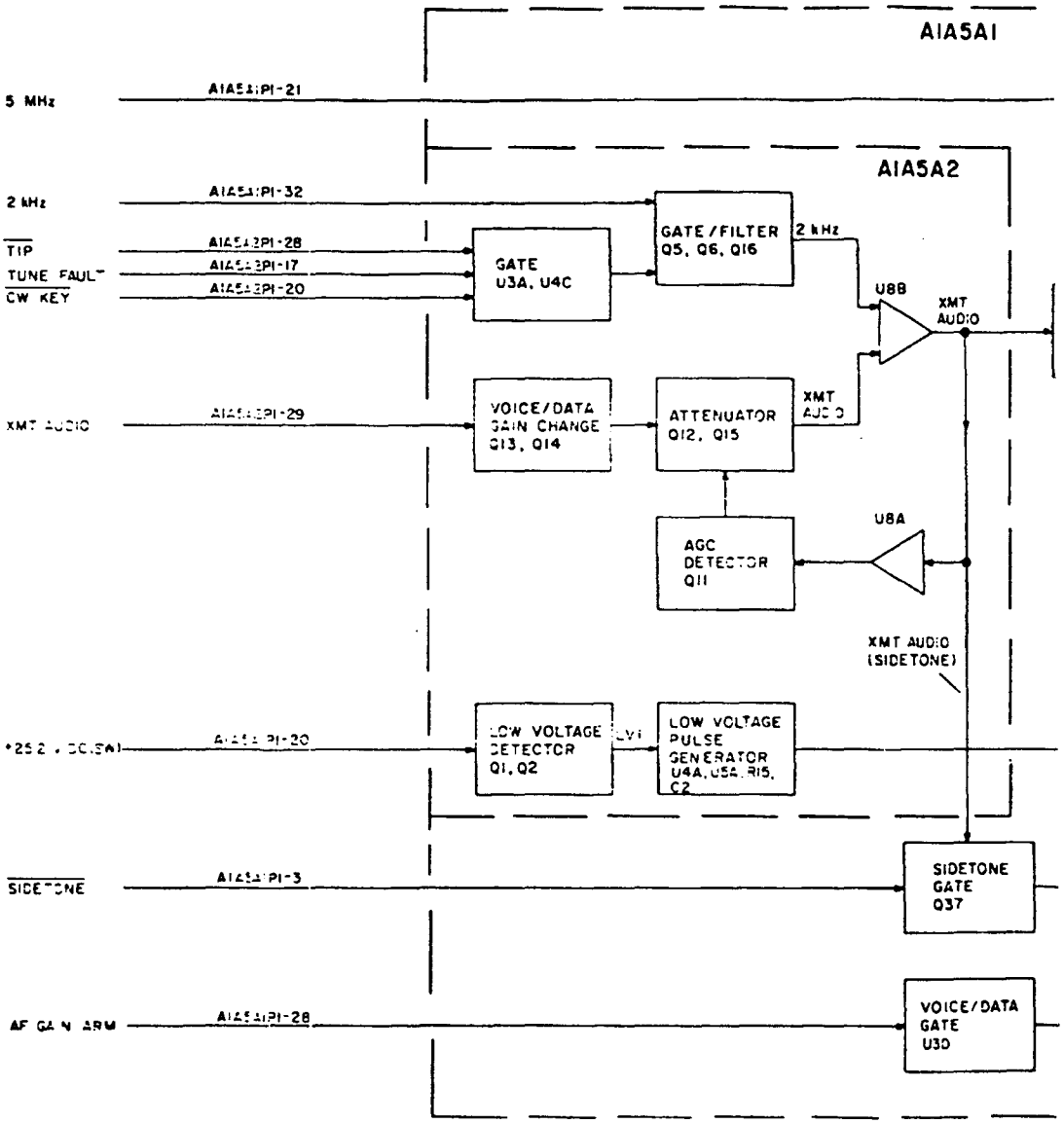
Figure 1-13. If/Af Amplifier A1A5 (Transmit) Functional Block Diagram


A1A5A1
5 MHz
A1A5A1P1-21
A1A5A2
2 kHz
A1A5A1P1-32
TIP
TUNE FAULT
CW KEY
A1A5A2P1-28
A1A5A2P1-17
A1A5A2P1-20
GATE
U3A, U4C
GATE/FILTER
Q5, Q6, Q16
2 kHz
U8B
XMT
AUDIO
XMT AUDIO
A1A5A2P1-29
VOICE/DATA
GAIN CHANGE
Q13, Q14
ATTENUATOR
Q12, Q15
XMT
AUDIO
U8A
AGC
DETECTOR
Q11
XMT AUDIO
(SIDETONE)
+25.2 ± 20.5VDC
A1A5A1P1-20
LOW VOLTAGE
DETECTOR
Q1, Q2
LVI
LOW VOLTAGE
PULSE
GENERATOR
U4A, U5A, R15,
C2
SIDETONE
A1A5A1P1-3
SIDETONE
GATE
Q37
AF GAIN ARM
A1A5A1P1-28
VOICE/DATA
GATE
U3D

b. ALC. Refer to figure 1-14 of this section and figure 4-5 of the schematic section. During transmit operation, the ALC stages of A1A5A1 are enabled by XMT logic from P2-32 to switch transistor Q11. When transmitting, negative ALC voltage from amplifier-coupler A3 is applied from P1-31 to the emitter of transistor Q17. If broadband amplifier A1A3 exceeds approximately 300 mW, it develops a negative ALC voltage which is applied to the emitter of transistor Q16 through P1-36. The output of Q16 or Q17 causes transistor Q13 to start discharging capacitor C22, which causes transistor Q9 to begin conduction. As the conduction of Q9 increases, the output of transistor Q6 (ALC/AGC DRIVE to mixer A1A2) decreases, permitting diodes A1A2CR1 and A1A2CR7 to conduct. This decreases the rf output from A1A2 to amplifier-coupler A3 until A3 has the proper output level and is not overdriven.

1.7.4.2.2.3 Mixer A1A2

Refer to figure 1-8 of this section and figure 4-2 of the schematic section. During transmit, the switching logic at P1-5 and P1-6 switches the transmit mixers on and the receive mixers off. The IF IN (5-MHz AME or SSB) signal is coupled by diode CR10 and transformer T8 to the up conversion mixer, transistors Q15 and Q16. The sum of 110- and 5-MHz frequencies (115 MHz) is coupled through transformer T7 and diode CR9 to the 115-MHz filter. The filtered output is coupled to the down conversion mixer, FET's Q5 and Q8, by diode CR5 and transformer T4. Here the 115-MHz signal is mixed with 117- to 144.9999-MHz variable injection signal from P2 to obtain the 2- to 29.9999-MHz output. FET's Q7 and Q8 neutralize

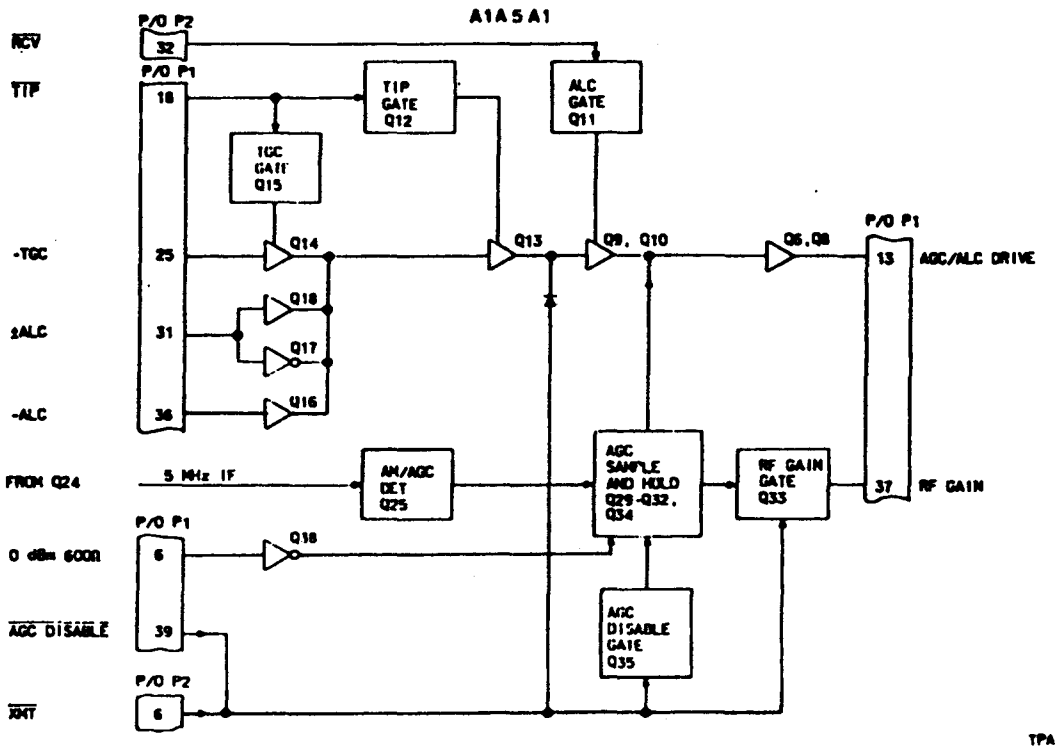


Figure 1-14. AGC/ALC, Simplified Schematic Diagram

the gate-to-drain capacity of FET's Q5 and Q6. The rf output of the down conversion mixer is coupled through low-pass filter inductors L1 and L2 and capacitors C1 and C2, to P1-14 (XMT RF) by transformer T3, diode CR4, and capacitor C4. If the rf output is too high (as noted in ALC discussion), the ALC/ AGC DRIVE at P1-9 decreases, permitting diodes CR1 and CR7 to conduct, reducing the rf output.

1.7.4.2.2.4 Broadband Amplifier A1A3

Refer to figure 1-7 of this section and figures 4-1 and 4-3 of the schematic section. The transmit rf output of A1A2 is applied to A1A3 via A1A2P1/A1A1J2-14 and A1A1J3/A1A3P1-2. With the radio turned on at the control, +25.2 V dc (SW) is applied to A1A3, and with the key line enabled by the ptt switch, keying relay K1 is energized and the +25.2 V dc (SW) is switched to the amplifier circuits by Q4. The incoming rf at P1-2 is passed through the LC filter network, a limiter circuit and on to the emitter follower stage, Q1, through the closed relay contacts, B1 and B2. The emitter follower couples the rf to rf amplifiers Q2, Q3, and Q5. The 250-mW rf output of Q5 is transformer coupled by T1 through the closed relay contacts A1 and A2 to P1-12. The ALC detector, VR2 and CR8, provide a protective ALC bias to A1A5 ALC circuits that limits the rf output to approximately 300 mW if amplifier-coupler A3 ALC should fail. This ALC OUT signal at P1-9 is routed through A1A1J3-9 to A1A1J5/A1A5A1P1-36. The transmit rf output from A1A3 is supplied to amplifier-coupler A3 through A1A3P1/A1A1J3-12 of A1A3 and A1A1P1/A3J1-36.

1.7.4.2.2.5 Frequency Synthesizer A1A6

Refer to figure 1-6. Frequency synthesizer A1A6 provides a variable injection frequency and a fixed injection frequency to A1A2 plus two fixed frequencies to A1A5 during both receive and transmit periods of operation. The variable injection frequency is a frequency in the 117 MHz to 144.9999-MHz range, variable in 100-Hz increments, the specific frequency being proportionate to the operating frequency selected at the control. The fixed injection frequency to the mixer module is 110 MHz. Two fixed frequencies are supplied to A1A5. One is the 5-MHz fixed injection frequency and the other one is the 2-kHz tone signal. A1A6 also supplies the transmit inhibit logic output (XMT INH) in response to the power on or frequency change logic (RECHANNEL) from control A2. Control A2 also provides the bcd frequency selection logic and the USB logic inputs to A1A6.

To process the above logic inputs and to generate the above output signals, the frequency synthesizer uses the seven subassemblies shown on figure 1-6. For frequency generation functions, four phase-lock loops are used. Refer to figure 1-15. One phase-lock loop is used to generate the fixed injection frequency (110 MHz). The remaining phase-lock loops, the low frequency, the converter, and the high frequency phase-lock loops, are used to generate the 117-144.9999-MHz variable injection frequency. The low frequency phase-lock loop (LFPLL) uses the bcd logic from the control and provides the bcd selected frequency within the 1.0 to 1.0999-MHz range to the converter for translation to a higher frequency within the 111 to 111.0999-MHz range.

This translated output from the converter is applied to the high frequency phase-lock loop (HFPLL) for translation to a higher frequency. During locked conditions, the HFPLL is controlled by the sample and hold phase detector stage. The output frequency of the HFPLL mixer (variable from 6-33.9 MHz), the resultant frequency of mixing the output frequency of the converter (111-111.0999 MHz) with the HFPLL vco frequency (117-144.9999 MHz), is sampled by the sample and hold phase detector to maintain the correct vco frequency. But, when a new frequency acquisition by the HFPLL is required (initiated by frequency change at control A2), control of the HFPLL vco is switched to the frequency/phase discriminator of the variable divider to acquire digital phase lock on the new frequency. As shown in figure 1-15, the variable divider is controlled by bcd logic from the control, thus, a frequency

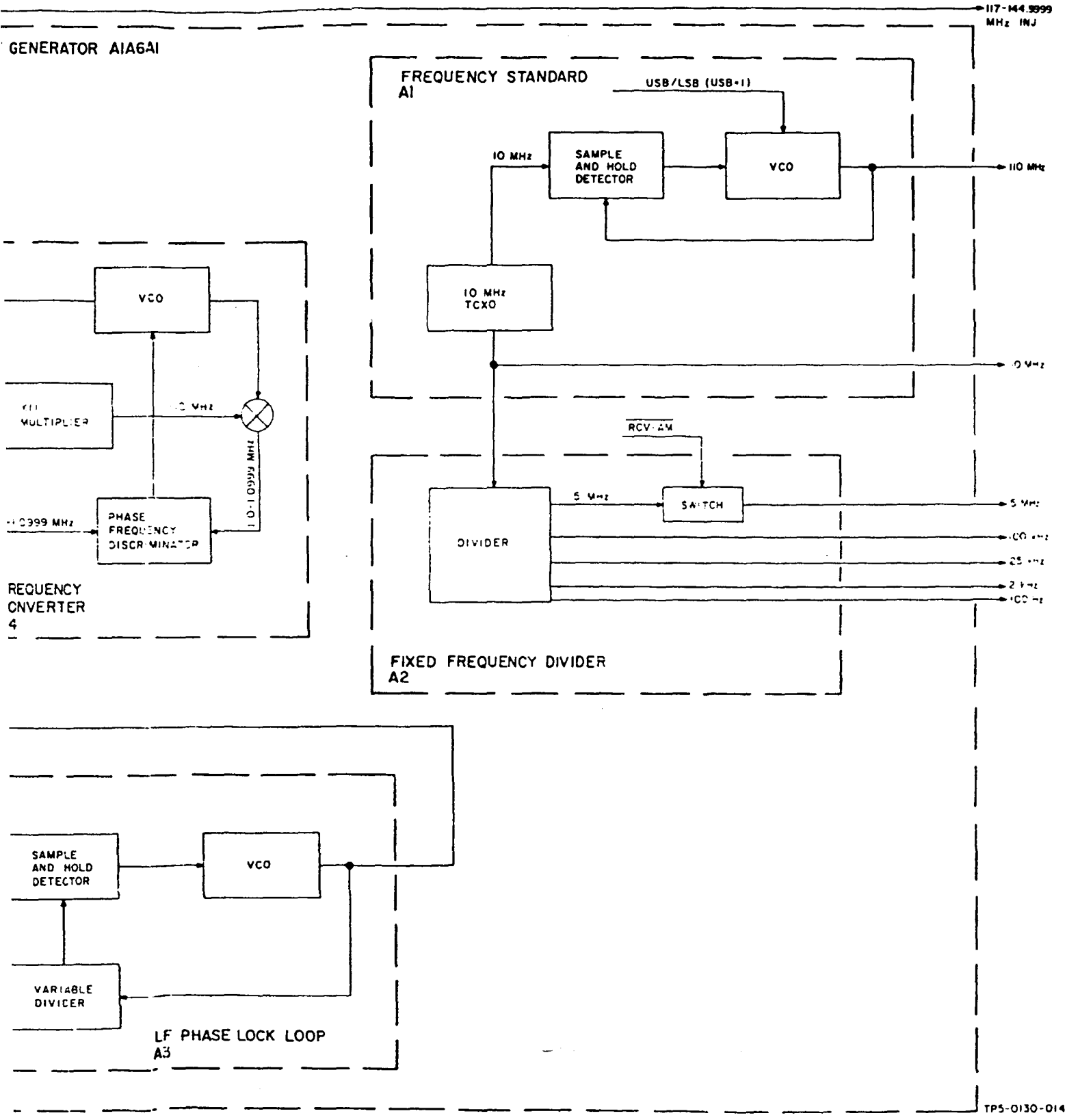
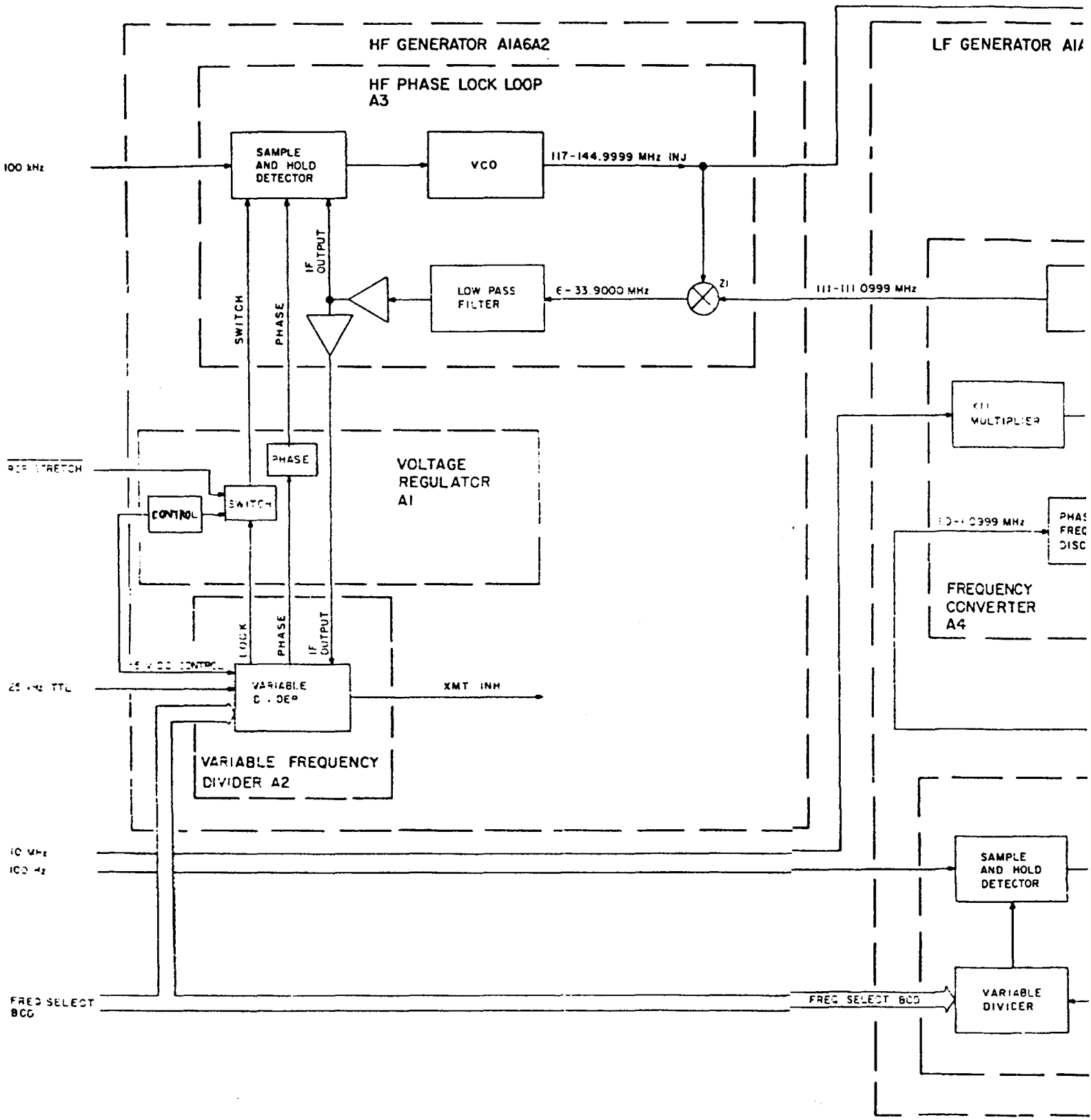


Figure 1-15. Frequency Synthesizer A1A6, Block Diagram


HF GENERATOR AIA6A2
HF PHASE LOCK LOOP
A3
LF GENERATOR AIA
100 kHz
SAMPLE
AND HOLD
DETECTOR
VCO
117-144.9999 MHz INJ
IF
OUTPUT
SWITCH
PHASE
LOW PASS
FILTER
6-33.9000 MHz
ZI
111-111.0999 MHz
MULTIPLIER
PHASE
VOLTAGE
REGULATOR
A1
CONTROL
SWITCH
LOCK
PHASE
IF
OUTPUT
FREQUENCY
CONVERTER
A4
VARIABLE
DIVIDER
XMT INH
VARIABLE FREQUENCY
DIVIDER A2
SAMPLE
AND HOLD
DETECTOR
VARIABLE
DIVIDER
FREQ SELECT
BCD
FREQ SELECT BCD

change at the control causes the bcd logic change to switch on the variable divider. This initiates the loop action necessary to achieve digital phase lock on the new frequency by the frequency/phase discriminator and inhibit the transmit (XMT INH) functions during frequency acquisition (rechannel cycle). When digital phase-lock occurs, vco control is transferred back to the sample and hold phase detector and the variable divider is switched off. This puts the hf phase-lock loop back in a locked (normal) condition.

The fixed divider operates in conjunction with the frequency standard and supplies the following frequencies to the radio receiver-transmitter. The 5-MHz is supplied to A1A5 during all modes of operation except AM receive when the 5-MHz signal is switched off. The 2-kHz tone signal is supplied to A1A5 during all modes of operation. The 100-kHz frequency is supplied to the HFPLL. The 25-kHz frequency is applied to the variable divider, and the 100-Hz frequency is supplied to the LFPLL.

a. Frequency Standard A1A6A1A1. Refer to figures 1-6 and 1-15 of this section, and figure 4-7, schematics section. The frequency standard subassembly circuits are comprised of the frequency standard generator (10 MHz), which is a temperature-compensated, crystal controlled oscillator (texo), and a fixed injection frequency generator, which is a vco with a sample and hold stage. The texo consists of crystal Y1, transistors Q1 and Q2, varactor CR2 and temperature compensating networks RT1, RT2, and RT3. The trimmer capacitor is provided to compensate for the aging of the crystal and the selectable components (as noted by schematic note 3) are to be selected at final test. When the radio power is turned on, the texo is energized and supplies a stable reference frequency of 10 MHz from the impedance matching output network of Q1 and Q2 through the buffer-driver stage Q3 and Q4 to the sample and hold reference pulse shaper Q5. The 10-MHz reference frequency output from the impedance matching network is supplied to frequency converter A1A6A1A4 and the 10-MHz output from the buffer-driver is applied to A1A6A1A2. The vco circuit consists of the oscillator, FET Q9, varactor CR1, and switch transistor Q8. With the radio power on, the USB logic input from A1A5 switches transistor Q8 on to provide the correct dc voltage level for the oscillator to operate at 110 MHz. The 110-MHz output of the vco is applied to the sample and hold circuit, CR7 and CR8, through buffer Q6 and Q7. The rectifier diodes CR7 and CR8, provide a negative dc voltage feedback to the vco that corrects the frequency compared to the 10-MHz reference frequency at the primary of T1. The 110-MHz output from the vco, 110 MHz INJ, is applied to A1A2 as an output from buffer-driver Q10 and connector A1A6A1A1P1.

The +5.2 V dc is supplied to frequency standard A1A6A1A1 from power supply A1A4 via A1A1 and A1A6A1A2. The +11.5 V dc is supplied by voltage regulator A1A6A2A1 via A1A6A1A2. (Refer to figure 4-11, schematics section.)

b. Fixed Frequency Divider A1A6A1A2. Refer to figures 1-6 and 1-15 of this section and figure 4-8, schematics section. The fixed frequency divider consists of a network of frequency dividers and a gated transistor emitter-follower circuit that applies the 5-MHz injection frequency output to A1A5. The 10-MHz reference frequency is supplied by A1A6A1A1 to transistor driver Q2. The output of the driver is a 10-MHz square-wave clocking signal that is applied to the 2:1 frequency divider, U1A. The outputs of the divider are two 5-MHz signals. One is used to clock the 5:1 divider stage, U1B and U2, and the other is coupled to emitter-follower Q1, which is controlled by the $\overline{\text{RCV}\cdot\text{AM}}$ logic from P1-6. Q1 is turned on by the $\overline{\text{RCV}\cdot\text{AM}}$ logic during all modes of operation except the AM receive mode at which time Q1 is turned off and the 5-MHz output is cut off. The 5-MHz input to the dividers, U1B, U2A and U2B, is divided by 5, to 1 MHz, and further divided by 10, to 100-kHz, by U3A. One 100-kHz output is applied to divider U3B and one output is supplied to HFPLL A1A6A2A3. The divider U3B is configured to divide the 100-kHz signal by 2 and 5, providing a 50-kHz output and a 20-kHz

output. The 50-kHz output is divided by 2 by U4A to provide a 25-kHz frequency to the variable divider subassembly. The 20-kHz output is applied to divider U5B and divided by 10 to produce a 2-kHz output. This is coupled by capacitor C2 to P1-5.

The 2-kHz output from divider U5B is also applied to 2:1 divider U4B and to 10:1 divider U5A, and converted to 100 Hz for application to LFPLL A1A6A1A3.

The +5.2 V dc is supplied by A1A4 and the +11.5 V dc is provided by A1A6A2A1 (figure 4-11, schematics section).

c. LF Phase-Lock Loop A1A6A1A3. Refer to figures 1-6 and 1-15 of this section and figure 4-9, schematics section. The LFPLL supplies to the frequency converter A1A6A1A4 a frequency that can be varied from 1.0 MHz to 1.0999 MHz in 100-Hz increments. The specific frequency within the 1.0- to 1.0999-MHz range is determined by the bcd logic input to connector P1 from control A2. To generate the 1.0- to 1.09999 MHz frequency, A1A6A1A3 employs a vco stage, a frequency/phase detector stage, and a sample and hold phase detector stage referenced to 100-Hz from the fixed frequency divider. The output frequency of the vco is controlled over the above range by the dc voltage applied to varactor CR2. Therefore, when a frequency is selected at control A2, the bcd logic is applied to the frequency discriminator variable dividers U6-U9. They establish the proper logic input to the sample and hold switch, U1, to adjust the dc voltage to CR2 for an oscillator output frequency equivalent to the binary coding from control A2. To maintain vco frequency stability, the output of the vco is looped back to the phase detector, U4A, through feedback driver Q7. The output of the frequency discriminator is applied from NOR gate U5A to the phase detector U4A. The output of U4A is a logic output with a variable duty cycle that controls the duty cycle of the output from U6 to the sample and hold phase detector, U1. Also applied to U1 is the ramp voltage supplied by the ramp generator, transistors Q1 and Q2. The ramp generator is driven by the 100-Hz reference signal from A1A6A1A2. When Q2 is on (the input is high), capacitors C1 and C2 are held at zero. When the input is low Q1 is turned off, allowing C1 and C2 to charge toward 14 V dc at a constant rate until Q2 is turned on by the 100-Hz input. The ramp voltage is sampled by the ϕ1 and ϕ2 signals at the duty cycle rate which is a function of the phase difference between the compared frequencies applied to the phase detector, U4A. The ϕ1 signal gates (samples) the ramp voltage through the first part of switch U1. The ϕ2 signal follows and gates the sampled ramp voltage through the second section of switch U1 for filtering. The sampled ramp voltage, after filtering, becomes the vco control voltage and is coupled to varactor CR2 by source followers Q3 and Q4. Increasing the vco control voltage, increases the vco frequency; decreasing the control voltage, decreases the vco frequency. Therefore, the vco control voltage, being a function of the frequency difference between the compared frequencies, increases or decreases the oscillator frequency to correct the output frequency.

The +13 V dc voltage is supplied by A1A4 and the +11.5 and +14 V dc voltage is provided by A1A6A2A1 (figure 4-11, schematics section).

d. Frequency Converter A1A6A1A4. Refer to figures 1-6 and 1-15 of this section and figure 4-10, schematics section. The frequency converter generates a frequency within the 111.0 to 111.0999-MHz range. The frequency is supplied to A1A6A2A3 for generation of the variable injection frequency that is supplied to A1A2. The specific output frequency of the converter is controlled by the output of frequency/phase detector (F/ϕ DET) U1 and U2. An output frequency between 111.0-111.0999 MHz is generated by the vco, Q2. The vco control voltage to CR1 from the F/ϕ detector is a function of the phase difference between the output frequency of the oscillator and the input frequency from A1A6A1A3, both of which are applied to the F/ϕ detector, U1. The input frequency to the F/ϕ detector from A1A6A1A3, as previously noted, is determined by the bcd logic from the control. The other input frequency to the F/ϕ detector

(1.0-1.0999 MHz), representing the vco frequency, is developed in the following manner. The 111.0-111.0999-MHz vco output is applied to buffer Q6 and coupled by C36 to gate G2 of mixer Q5. The 10-MHz input from the frequency standard is applied to amplifier-buffer Q3 and coupled by C26 to X11 multiplier Q4 which provides the 110-MHz input to gate G1 of mixer Q5. The resultant output frequency, 1.0-1.0999 MHz, is supplied to squaring amplifier Q1. The 1.0-1.0999-MHz square-wave output of Q1 is applied to the input of F/ϕ detector U1A. The two frequencies are compared by the F/ϕ detector to develop a square wave pulse train at the output of U2 with a duty cycle that is a function of the phase difference between the compared frequencies. The output of U2C is applied to the low-pass filter network where the ac component is filtered out and the dc voltage becomes the vco control voltage. This is applied to varactor CR1 to vary the vco frequency as necessary to decrease the phase difference to achieve lock-on.

The +13 and +5.2 volts dc voltage is supplied by A1A4 and the +11.5 volts dc comes from A1A6A2A1 (figure 4-11, schematics section).

e. Hf Phase-Lock Loop A1A6A2A3, Variable Frequency Divider A1A6A2A2, and Voltage Regulator A1A6A2A1. Refer to figures 1-6 and 1-15 of this section, and figures 4-11, 4-12, and 4-13, schematics section. The purpose of the HFPLL is to generate a variable injection frequency within the 117 to 144.9999-MHz range for application to mixer A1A2 (figure 1-6). To accomplish this, A1A6A2A3 requires the 111.0 to 111.0999-MHz input from A1A6A1A4, the 100-kHz signal from A1A6A1A2, and the phase/lock control signals from A1A6A2A2. During locked operations (normal operating conditions with power on and all tuning complete), the frequency generating circuits of A1A6A2A3 operate independently of A1A6A2A2 and A1A6A2A1. The HFPLL (figure 4-13, schematics section) consists of the vco, Q104 and varactors CR101 and CR102; the sample and hold detector, Q3; the mixer, Z1; and the associated buffer stages for the vco and mixer output signals. The output frequency of the vco is actively controlled by the dc control voltage applied by the sample and hold phase detector to the varactors. This detector dc output is a result of the sampled output frequency of mixer Z1. Two frequencies are applied to Z1, the 111-111.0999-MHz reference frequency from A1A6A1A4 and the 117-144.9999 MHz output frequency of vco Q104, to develop an if within the 6-33.9 MHz range (4-MHz above the 2-29.9999-MHz operating frequency selected at control A2). The output of the mixer is passed through the low-pass LC filter network to the squaring amplifier circuits of Q6 and Q7 for application to the sample and hold detector stage. The 6-33.9-MHz signal is mixed with the 100-kHz input from A1A6A1A2 in the secondary of transformer T1. The resultant 6-33.9-MHz signal is rectified and filtered by the circuits of CR3 and CR4 and Q3 of A1A6A2A3. This becomes the vco dc negative feedback voltage that is applied to varactors CR101 and CR102 of A1A6A2A3. The dc voltage varies the capacitance of the varactors, raising or lowering the vco frequency as necessary to keep the phase error in the hold-in range.

The if output from Z1 is also applied from if amplifier Q7 to squaring amplifier Q5, the output of which is routed to A1A6A2A2P2-2 (figure 4-12, schematics section). During the locked condition described above, the variable divider is inoperative, therefore, the if input has no effect. However, when the radio is first turned on or a new frequency is selected at the control a reechannel logic signal is initiated by control A2. This starts a tuning cycle within the radio that includes switching (on or off) of logic 1 and +5 V dc to various circuits of A1A6A2A2. The reechannel logic ($\overline{\text{RCP STRETCH}}$) is supplied from A1A5A2P1-33 to A1A6A2A1P1-3 via A1A5A1 and chassis A1A1. When the reechannel signal is enabled at A1A6A2A1P1-3, a ground is applied to pulse stretcher circuit U2 of A1A6A2A1 resulting in conduction of squaring amplifier Q7. Conduction of Q7 establishes the following events; (1) Q4 to conduct, (2) Q5 to conduct, (3) +14V dc potential felt at switch function of A1A6A2A3, (4) Q8 ceases conduction, (5) Q9 to conduct, and (6) Q6 to conduct. The conduction of Q6 applies a ground potential on connector pin A1A6A2A1P2/A1A6A2A2P2-5 (5 V dc CONTROL line). A ground

on this pin forward biases series control switch Q2 of A1A6A2A2 thereby enabling the logic 1 and +5 V dc function. These two functions are enabled as long as control transistor Q2 is held on by the 5 Vdc CONTROL signal from A1A6A2A1. When a LOCK (LOCK=O) pulse occurs on connector pin A1A6A2A1P2-3, the 5 V dc CONTROL line is disabled and Q2 ceases conduction. This disables logic 1 and +5 V dc on A1A6A2A2.

Refer to figure 4-12, schematics section. A1A6A2A2 performs the frequency/phase discrimination and vco control functions for the hf phase-lock loop in a manner similar to those functions previously covered for A1A6A1A4. When logic 1 and +5 V dc is enabled as a result of a rechannel pulse, the variable dividers, U2-U5 of A1A6A2A2, receive the bcd logic signals from the control. The bcd logic, representing the selected frequency, is processed for comparison with the logic output of divider U1 (6-33.9 MHz), representing the HFPLL vco output frequency, to determine the frequency and phase difference with reference to the 25-kHz signal from A1A6A1A2 via A1A6A2A1. The phase difference output from the frequency/phase discriminator, U10 through U12 of A1A6A2A2, is applied to the PHASE signal line, A1A6A2A2P2-4, the duty cycle of which is a function of the phase difference between the compared frequencies.

Refer to figures 4-11, 4-12, and 4-13, schematics section. The PHASE signal at A1A6A2A2P2/A1A6A2A1P2-4 is applied to the pulse shaper transistor, A1A6A2A1Q3. The output of A1A6A2A1Q3 is applied to FET A1A6A2A3Q8 for filtering and conversion to a dc vco control voltage. The dc level, proportionate to the phase difference, is applied to the varactors to retune the vco to reduce the phase difference until lock-in is achieved. When lock-in occurs, the frequency phase discriminator of the variable divider (figure 4-12, schematics section) provides a LOCK signal at A1A6A2A2P2-3 from NOR gate A1A6A2A2U6B, which is routed to inverter A1A6A2A1U2A and coupled to the pulse shaper amplifier stage, Q7, Q4, Q8, and Q9, of voltage regulator A1A6A2A1. One output from A1A6A2A1Q4 is supplied to A1A6A2A3 (SWITCH signal) to turn off FET A1A6A2A3Q8. This transfers the control of vco A1A6A2A3Q104 from A1A6A2A2 to the sample and hold circuits of A1A6A2A3. The other output from A1A6A2A1Q4 is amplified by A1A6A2A1Q9 and applied as a cut off signal to switch transistor A1A6A2A1Q6 as previously discussed in this subsection (e).

When a frequency change is initiated at the control, the bcd logic is processed by A1A6A2A2 to provide a transmit inhibit signal (XMT INHIBIT to A1A5A2P1-22 to prevent transmission during the tune cycle of the radio. The +5.2 volts dc at A1A6A2A2-11 is supplied by A1A4.

Refer to figure 4-11, schematics section. In addition to the circuits already discussed, A1A6A2A1 provides regulating circuits for the +11.5 and +14 volts dc voltages as well as signal interface between the various synthesizer subassemblies as shown on figure 4-11. The +14-volt dc regulator consists of series regulator transistor Q1, reference voltage regulator VR1, and comparator U1B, which is connected to the output voltage divider R3, R4, and R12, and the reference voltage divider, VR1, R10, and R11. The collector of series regulator Q1 is connected to +25.2 V dc (sw and fltr). A change in the +14-volt dc output appears as a voltage change across voltage divider R3, R4, and R12. This change is compared with the reference voltage by the comparator U1B and reflected as a bias change at the base of series regulator Q1. An increase in bias reflects an increase in the output voltage. Consequently, the increased bias reduces conduction of Q1 which reduces the output voltage until +14 V dc is reached. In like manner, a decrease in bias reflects a decrease in the output voltage. This increases Q1 conduction to increase the output voltage until the +14-volt output level is reached. The +11.5-volt voltage regulator, Q2, VR3, and U1A, are connected to the reference voltage divider VR1, R10, and R11, and +11.5-volts dc divider R7, R8, and R9. The series regulator Q2, connected to +13 volts dc, and the control circuits operate in the same manner as Q1 to provide a regulated +11.5 volts dc output.

The +14- and +11.5-volt dc outputs are distributed to the various frequency synthesizer subassemblies as shown on the voltage regulator schematic diagram, figure 4-11.

1.7.4.2.2.6 Power Supply A1A4

Refer to figure 1-16 and 1-33 of this section and figure 4-4, schematics section. Power supply A1A4 provides regulated +13 volts and +5.2 volts dc outputs from a +25.2-volt dc source (battery). The routing of source voltage is shown on the power distribution diagram, figure 1-33 of this section. The +13 V dc switching regulator circuits consist of series switch transistor Q1, fly-back diode CR1, control transistors Q3, Q4, Q5, comparator transistors Q6 and Q7, and reference voltage regulator VR4. Transistor Q1 conducts in 14- to 35-usec intervals in response to bias changes effected by the comparator, Q6 and Q7. If the sampled output voltage applied to Q6 is high compared to the reference voltage applied to Q6, the series switch transistor is saturated for reduced periods of time during its operating interval by the reduced on-time of the control transistor Q3. The on-time of Q3 is reduced by the increased bias voltage from the Darlington pair of transistors, Q4 and Q5, which reflects the voltage error (high voltage) determined by the comparator Q6. During the conduction cycle of series switch Q1, the reduced current flow causes the output voltage to decrease toward the reference level until the correct output (+13 V dc) is reached. Conversely, if the output voltage decreases, the effective bias reverses to increase the conduction time of Q1 and raise the output voltage to the normal level. Transistor Q2 provides overcurrent protection for the +13 V dc regulator network.

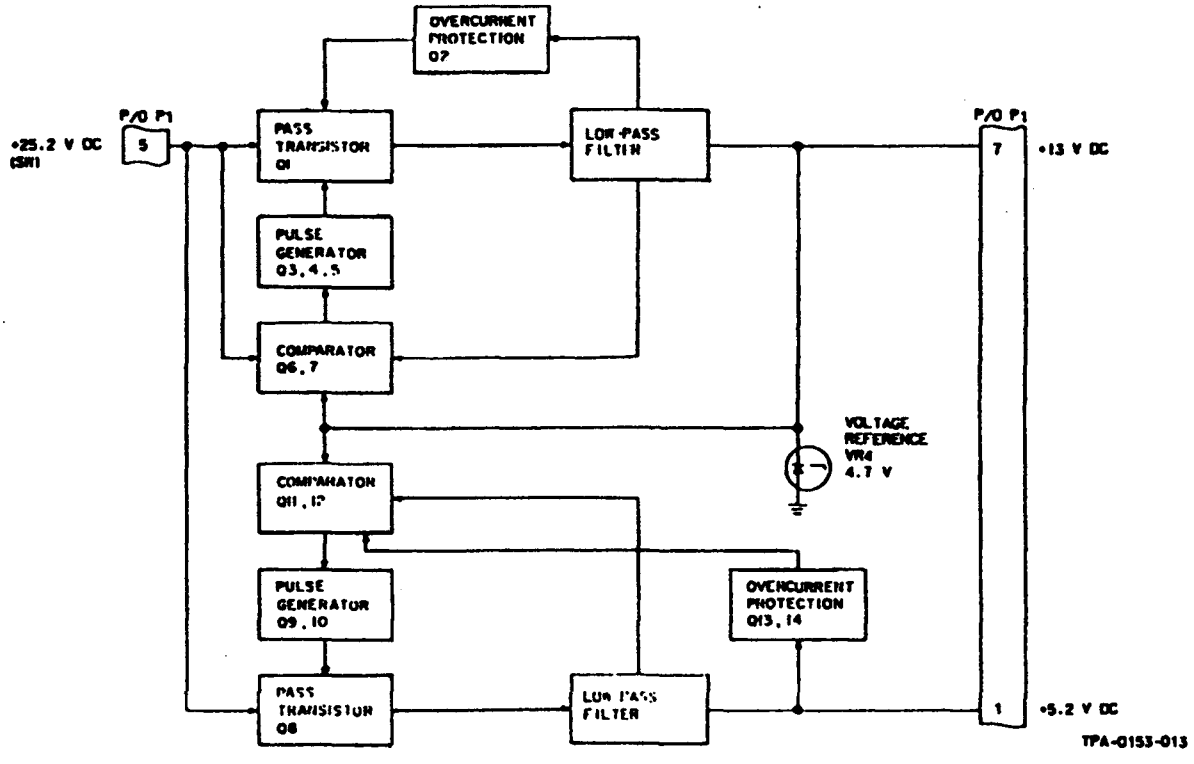


Figure 1-16. Power Supply A1A4 Simplified Schematic Diagram

The +5.2-volt dc regulator network is comprised of series switch Q8, control circuits Q9 and Q10, comparator Q11 and Q12, and reference voltage regulator VR4. The operation of the +5.2 V dc regulator is similar to the operation of the +13 V dc regulator. Transistors Q13 and Q14 provide overcurrent protection for the regulator.

1.7.4.2.2.7 Receiver-Transmitter Chassis A1A1

Refer to figure 4-1, schematics section. The receiver-transmitter chassis has eight connectors, J1 through J7 and P1, and a number of filtering capacitors. The eight connectors provide interconnection between modules A1A2 through A1A6, control A2 and amplifier-coupler A3. A dc filter circuit for +25.2 V dc (SW) is also provided. The filter circuit, Q1, capacitors C1 and C2, and resistors R1 through R3 are energized when +25.2 V dc (SW) is switched on at control A2. The +25.2 V dc (SW) turns on Q1. This results in a +25.2 V dc (SW and FLTR) output from the filter network, C1, C2, and R1 through R3, to connector J6 of A1A1. When the +25.2 V dc (SW) is switched off at control A2, transistor Q1 is turned off, cutting off the +25.2 V dc (SW and FLTR) to J6.

1.7.4.3 Amplifier-Coupler A3, AM-5280/URC

1.7.4.3.1 Transmit Theory

Refer to figure 1-17. Power amplifier A3A4 of the amplifier-coupler is a three stage push-pull class AB broadband amplifier with a minimum power gain of 23.5 dB. The amplifier is designed for a maximum required drive of 100 milliwatts, and 22-watts output. An output of 22 watts allows for antenna coupler losses, and guarantees full 20-watts output when the antenna coupler is tuned to a 50-ohm load. The power amplifier can be operated at either 20- or 2-watts output. The output level is selected by a switch on control A2.

A thermal switch in the power amplifier monitors the temperature of a heat sink. In the event a safe operating temperature is exceeded, such as by over extending the duty cycle, the ALC circuit automatically limits the output at 2 watts.

The fully automatic antenna coupler is capable of tuning an 8-foot whip and 50-ohm antennas over the 2- to 30-MHz frequency range. The coupler will also tune long wire and other whip antennas at selected frequencies. Tuning time is 4 seconds typical and 7 seconds maximum. Tuning elements include servo-driven elements (A3A7 and A3A8) that provide fine tuning and frequency band switched elements (A3A9). Elements within A3A9 are used to translate antenna impedances to within the tuning range of the servo-driven elements, A3A7 and A3A8.

1.7.4.3.1.1 Power Amplifier A3A4

Refer to figures 4-18 and 4-19, schematics section, and figure 1-17 of this section. In transmit mode, rf is applied from radio receiver-transmitter A1 to rf subassembly A3A4A1. Since the PA KEY is low and +25.2 V dc (KEYED) is enabled in transmit mode, rf is passed through contacts B2/B1 of relay A3A4A1K1 to transformer A3A4A1T1. The rf is amplified by a three stage amplifier and applied to output coax A3A4A1P1. Each of the three amplifier stages of A3A4A1 is transformer coupled to the next stage. The predriver stage consists of transistor pair Q1 and Q2, the driver stage consists of Q3 and Q4, and the final amplifier consists of Q5 and Q6. The rf is amplified to about 22 watts and coupled through transformer T6 to bias/control A3A4A2, connector J1. A bias regulator circuit on A3A4A2 provides the proper dc bias levels to coupling transformers A3A4A1T1, T2, and T3 to ensure class AB amplifier operation. The amplified rf is then passed by relay A3A4A2K1 to bandswitch A3A5.

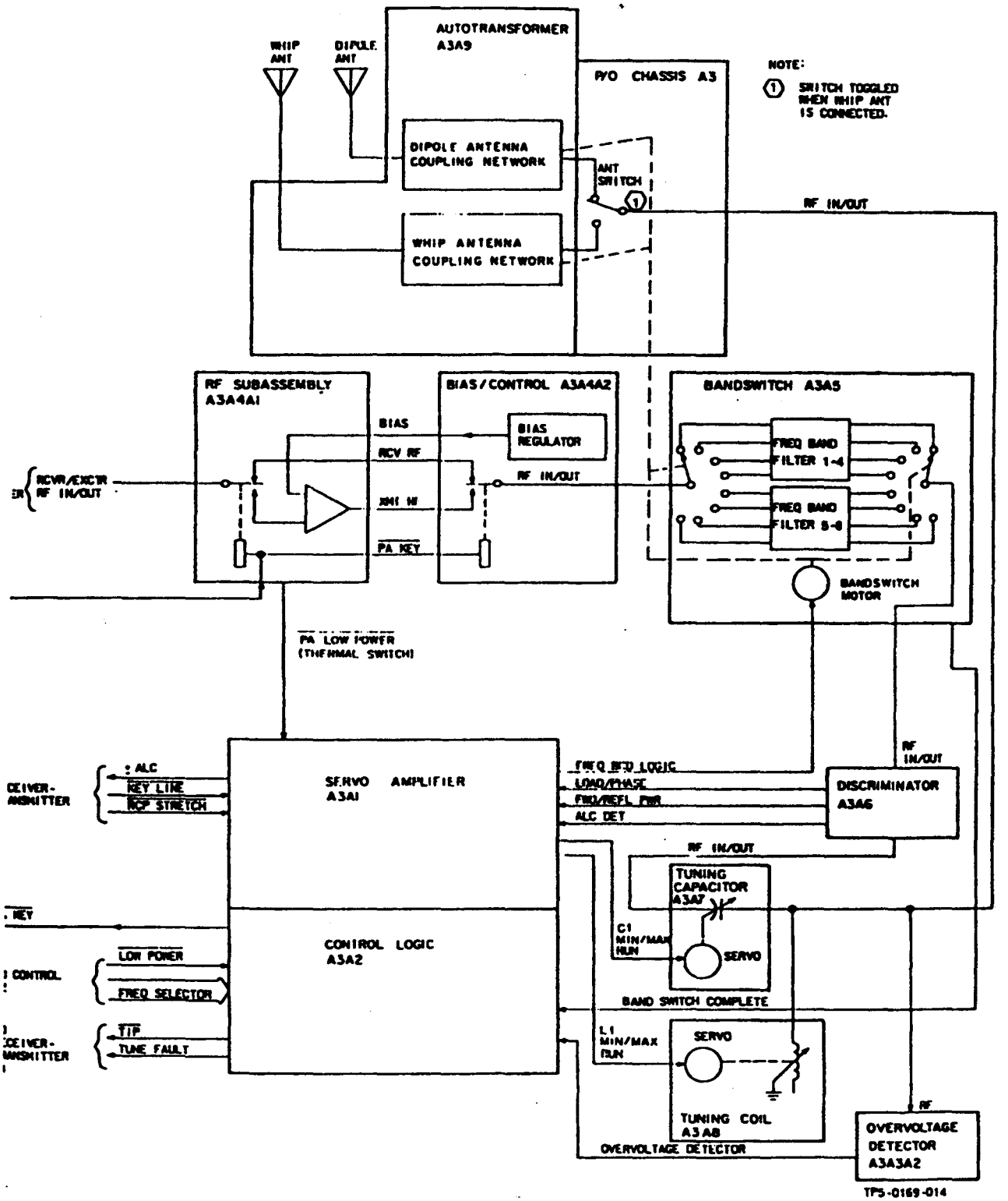


Figure 1-17. Amplifier-Coupler A3, AM-5280/URC, Block Diagram

Power amplifier ALC (automatic level control) is derived by sampling the rf drive supplied to discriminator A3A6. The resulting dc signal from the alc detector on the discriminator is fed to an op-amp on servo amplifier A3A1. The op-amp produces 0 VDC when the output of the rf amplifier is 1/2 dB or less below 20 watts and approximately -8 V dc with an rf output +1/2 dB above 20 watts.

1.7.4.3.1.2 Bandswitch A3A5

Refer to figure 1-17 this section and figure 4-20, schematics section. The bandswitch automatically selects the proper frequency band filter upon receipt of information from control logic A3A2. The band switched filters are used to provide harmonic rejection in the transmit mode. The filters are low pass filters and are selected approximately every 1/2 octave for each of the eight bands. The filter element values for each band are selected to give the best possible harmonic suppression for that band. The number of filter elements in some bands is higher than actually needed for harmonic suppression, this reduces the bandpass ripple to keep the vswr low at the higher frequencies and maintains optimum efficiency. Frequency band logic from control logic A3A2 applies a logic high to the appropriate servo band contact of switch S1. This logic high enables transistor switch A1Q2 which actuates relay A1K1 and applies +25.2 V dc to bandswitch motor B1. The motor runs and rotates switches S1, S2A, and S3 until S1 switches off of the logic high contact and opens the motor circuit. This deenergizes A1K1 and stops the motor. Simultaneously, S2A and S3 have rotated to contact positions corresponding with the activated frequency band. This connects the appropriate bandpass filter (1 of 8) to the rf signal path. The amplified rf from the power amplifier is now able to pass through S3 to the proper bandpass filter and through S2A to discriminator A3A6.

The bandswitch also drives switch S2B which applies a ground to the center tap of the variable tuning coil (A3A8) if the frequency is greater than 12 MHz. Bandswitch motor B1 is mechanically coupled to the wafer switch in autotransformer A3A9. While the motor is running the band logic selects the correct output network in A3A9. When the motor stops running (relay A1K1 deenergizes), ground is removed from the band switch complete output (A3A5P1-14). This logic output tells control logic card A3A2 that the band switching process is completed.

During the amplifier-coupler tune cycle, a logic low from the tune in progress (TIP) circuit actuates relay A1K2. This places the TIP resistor across the output (rf line) until all tuning is completed. The TIP resistor is located on A3.

1.7.4.3.1.3 Discriminator A3A6

Refer to figure 4-21, schematics section. The discriminator is a device that samples input rf power, voltage and current to the amplifier-coupler and develops dc error signals that are related to the impedance of the load and the power to the load. The loading discriminator develops a dc error voltage that is proportional to the magnitude of the impedance with respect to the normal 50-ohm impedance. The phasing discriminator develops a dc error signal that is proportional to the phase angle between the reactive and resistive portions of the load impedance. The forward and reflected power detectors are used to determine the start and completion respectively of the tuning sequence.

a. Loading Discriminator, Part of A3A6A1 and A3A6A2. Refer to figure 1-18. The loading discriminator compares the magnitude of the rf current with the rf voltage. This comparison creates an error signal output that is proportional to the difference between the impedance of the rf circuit and 50 ohms.

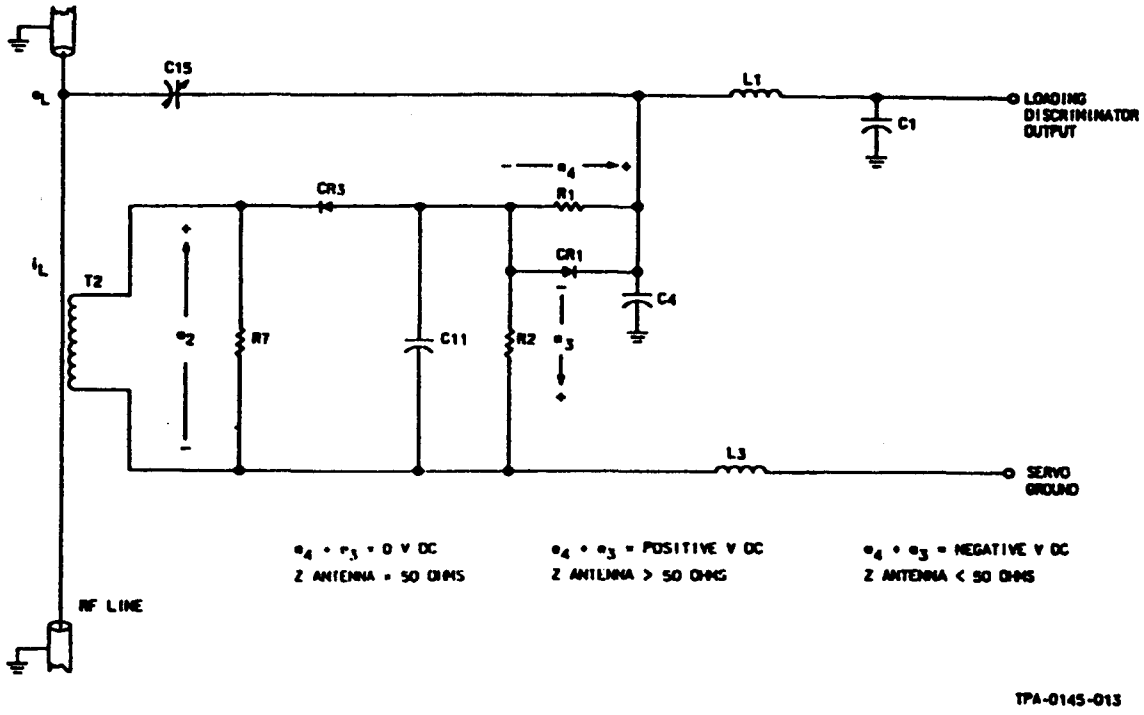


Figure 1-18. Loading Discriminator, Part of A3A6A1 and A3A6A2, Simplified Schematic Diagram

When the impedance of the rf circuit is 50 ohms, there is no error signal developed. When the rf circuit impedance is greater than 50 ohms, the error signal is positive. When the rf circuit impedance is less than 50 ohms, the error signal is negative.

Rf line current (i_1) induces a voltage (e_2) across transformer T2. When diode CR3 is forward biased, the current through resistor R2, diode CR3, and transformer T2 develops a voltage (e_3) across R2 that is proportional to the rf line current.

Line voltage is sampled by a voltage divider consisting of C15 and C4. When diode CR1 is reverse biased, the current through R1 develops a voltage (e_4) across R1 that is proportional to the rf line voltage.

C15 is factory adjusted so that the voltage across R2 is equal to the voltage across R1 when the impedance of the rf circuit is 50 ohms.

When the rf circuit impedance is less than 50 ohms, the line current increases and the line voltage tends to decrease. This causes the voltage across R2 to increase due to the increased current flow through T2. The voltage across R1 tends to decrease since it is proportional to the line voltage. The voltage difference across R2 and R1 develops

a negative error signal output. When the rf circuit impedance is greater than 50 ohms, the inverse is true, and a positive error signal is developed.

b. Phasing Discriminator, A3A6A3 and part of A3A6A1. Refer to figure 1-19. The phasing discriminator in amplifier-coupler A3 develops a dc error signal that is proportional to the phase shift between the rf voltage and the rf current. When the antenna is resistive, the line current and the line voltage are in phase, and the error signal is zero. When the antenna is capacitive, the line current leads the line voltage, and the error signal is negative. When the antenna is inductive, the line current lags the line voltage, and the error signal is positive.

The phasing discriminator is divided into two circuits. Potentiometer R5 is adjusted to balance the impedance of circuit number 1 (B, C, E, and F) and circuit number 2 (A, D, E, and F). The line voltage e_L is sampled, with no phase shift, by voltage divider C12 and C13. The induced voltage in the secondary of the transformer is 90 degrees out of phase with line current i_L. The vector addition of the induced voltage e_2 and the sampled voltage e_6 in circuit number 1 creates a resultant voltage e_4. The vector addition of induced voltage e_3 and the sampled voltage e_6 in circuit number 2 creates a resultant voltage e_5. Voltages e_4 and e_5 are rectified by CR6 and CR5 and filtered by C10 and C9. The algebraic sum of Vcc and Ved is the error output.

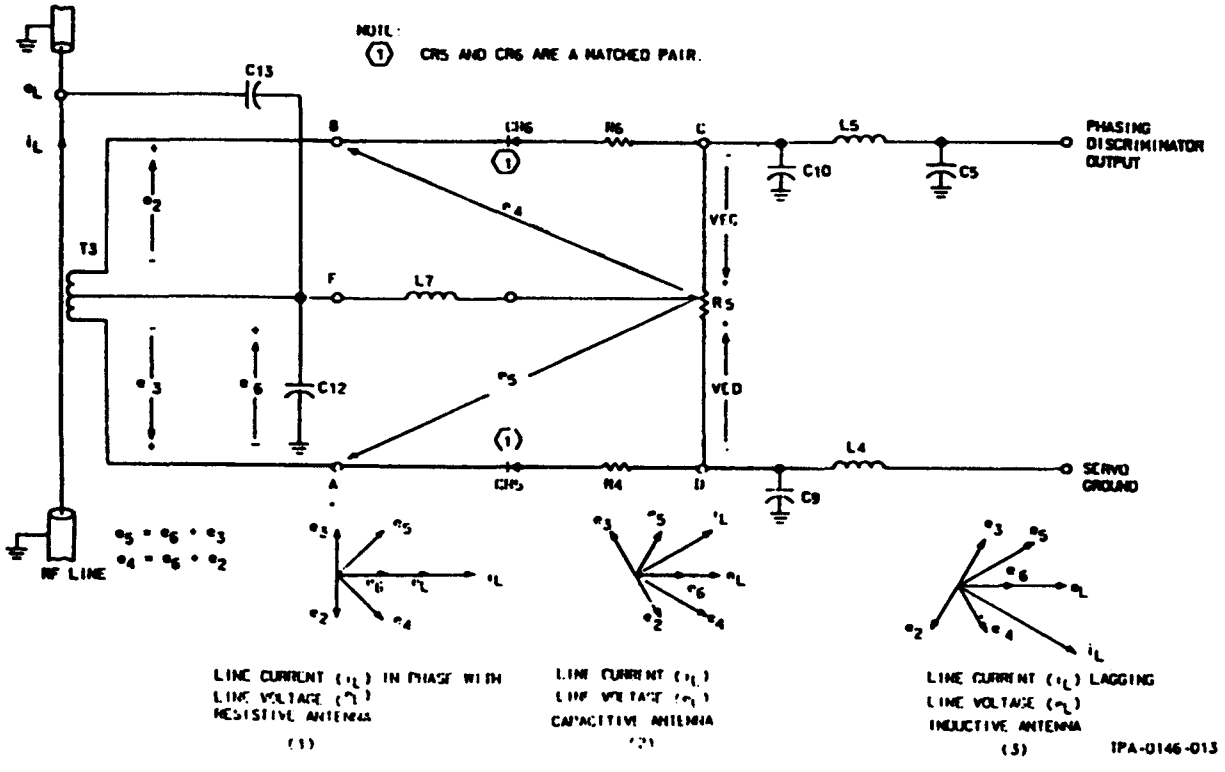


Figure 1-19. Phasing Discriminator, A3A6A3 and part of A3A6A1, Simplified Schematic Diagram

When the antenna is resistive, line current i_L and line voltage e_L are in phase. The magnitude of the resultant voltage across circuit number 1 (e_4) is equal to the magnitude of the resultant voltage across circuit number 2 (e_5); therefore, the error signal is zero (vector diagram (1) of figure 1-19).

When the antenna is capacitive, the vector addition of induced voltage e_2 and sampled voltage e_6 causes resultant voltage e_4 to increase in magnitude. The vector addition of induced voltage e_3 and sampled voltage e_6 causes resultant voltage e_5 to decrease in magnitude. The algebraic sum of resultant voltages e_4 and e_5 creates a negative error signal output (vector diagram (2) of figure 1-19).

When the antenna is inductive, the vector addition of induced voltage e_2 and sampled voltage e_6 causes resultant voltage e_4 to decrease in magnitude. The vector addition of induced voltage e_3 and sampled voltage e_6 causes resultant voltage e_5 to increase in magnitude. The algebraic sum of resultant voltages e_4 and e_5 creates a positive error signal output (vector diagram (3) of figure 1-19).

Resultant voltage e_4 is rectified by diode CR6 and then filtered by C5, L5, and C10. Resultant voltage e_5 is rectified by diode CR5 and then filtered by L4, and C9. The algebraic differences of the resultant voltages create a dc error signal output proportional to the phase difference between the rf voltage and the rf current.

Forward Power Discriminator, Part of A3A6A1 and A3A6A2. Refer to figure 1-20. The forward power discriminator generates a dc output proportional to the rf power traveling toward the antenna.

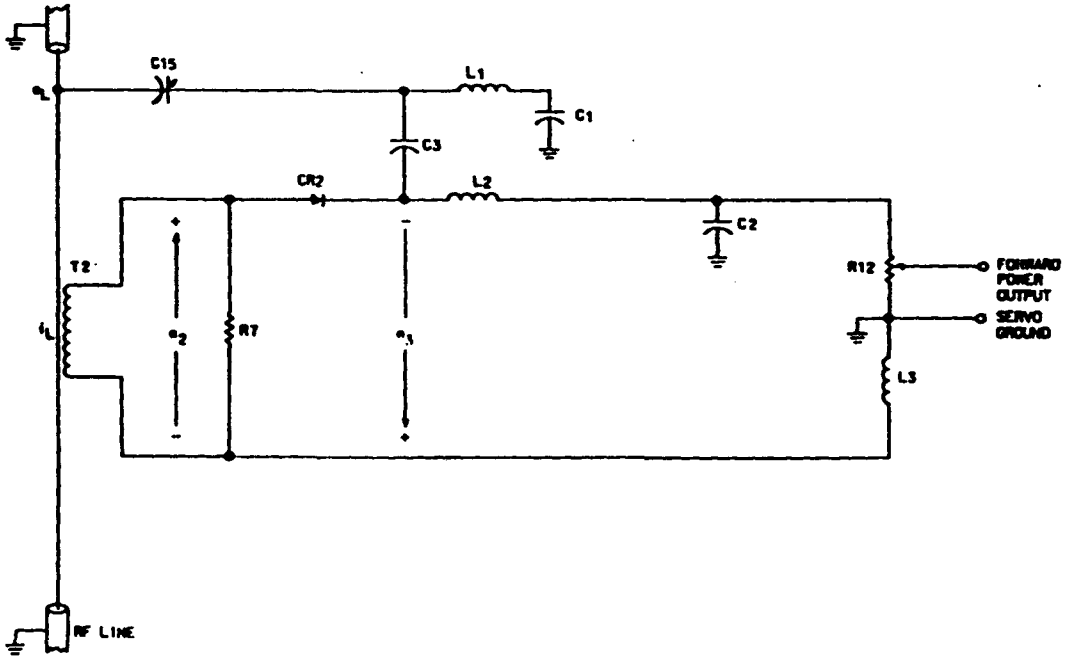


Figure 1-20. Forward Power Discriminator, Part of A3A6A1 and A3A6A2, Simplified Schematic Diagram

The secondary of transformer T2 is loaded with a low value of resistance, R7, to result in a secondary voltage (e_2) 180° out of phase with primary current. The line voltage is sampled by the voltage divider C15 and C1 and appears at the junction of CR2 and L2. The sampled portion of the line voltage is 180° out of phase with the secondary voltage across T2. On one-half of the rf cycle the induced voltage is greater in magnitude than the sampled voltage; therefore, diode CR2 is forward biased to produce a positive output when forward power is present.

d. Reflected Power Discriminator, Part of A3A6A1 and A3A6A2. Refer to figure 1-21. The reflected power discriminator develops a dc output proportional to the deviation of the vswr from 1.0 to 1. The vswr deviates from 1.0 to 1 when the antenna impedance is not 50 ohms and resistive; therefore, a reflected power output is developed when the antenna circuit is not resonant with a resistance of 50 ohms.

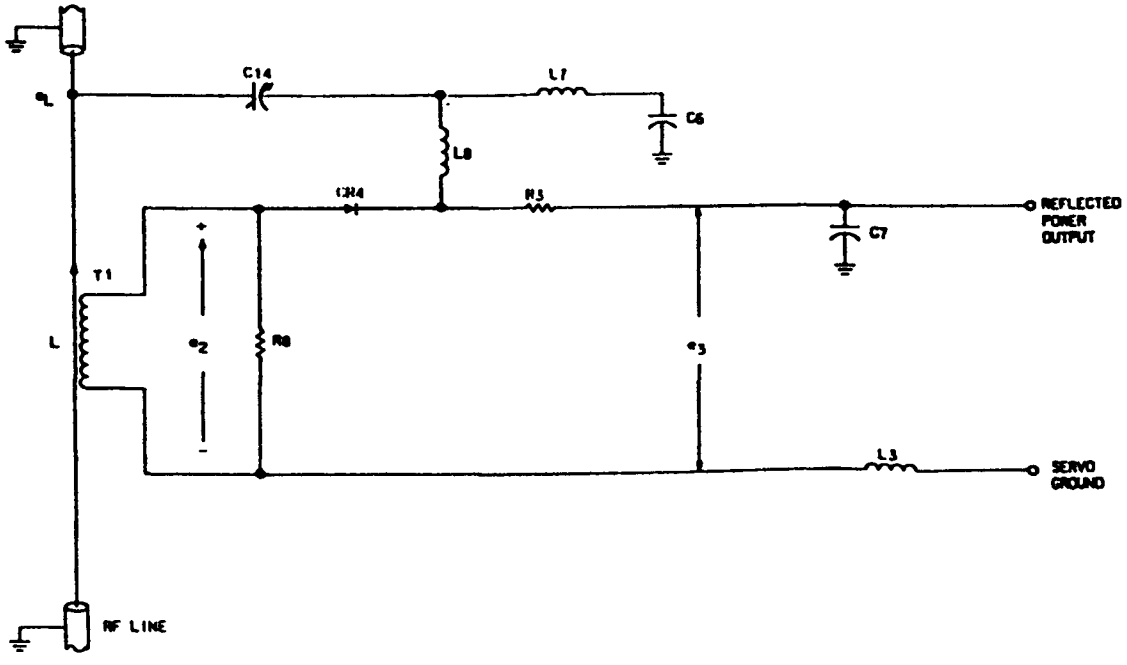


Figure 1-21. Reflected Power Discriminator, Part of A3A6A1 and A3A6A2, Simplified Schematic Diagram

The secondary of transformer T1 is loaded with a low value resistor, R8, to result in a secondary voltage (e_2) in phase with the line current i_1. The line voltage is sampled, with no phase shift, by voltage divider C14 and C6. C14 is factory adjusted to create a sampled voltage (at junction of CR4 and R3) equal to the induced voltage on T1 when the vswr is 1.0 to 1; therefore, CR4 is cut off, and there is no output.

When the antenna circuit is resonant with a resistance less than 50 ohms, the rf current increases and the rf voltage tends to decrease. The induced voltage in the secondary of T1 is greater in magnitude than the sampled voltage. Therefore, on the positive half of the rf cycle, diode CR4 is forward biased. The conduction of CR4 develops a positive output proportional to the reflected power.

When the antenna circuit is resonant with a resistance more than 50 ohms, the rf current decreases and the rf voltage tends to increase. The induced voltage e_2 is less than sampled voltage e_3. Therefore, on the negative half of the rf cycle, diode CR4 is forward biased. The conduction of CR4 develops a positive output proportional to the reflected power.

When the antenna circuit is reactive (nonresonant), the rf line voltage is out of phase with the rf line current. During a portion of each cycle, the induced voltage is more positive than the sampled voltage, and diode CR4 is forward biased. The conduction of CR4 develops a positive output proportional to the reflected power.

e. ALC Detector. The ALC detector develops a dc output proportional to the rf voltage. The rf is rectified by CR7 and referenced by zener diode VR1. The ALC detector voltage controls the output of the power amplifier during tune and low power (2 watts) modes.

1.7.4.3.1.4 Rf Tuning Network

Refer to figure 1-22 Tuning capacitor A3A7(C1) and tuning coil A3A8(L1) are servo driven elements that provide exact impedance matching to the 50-ohm output of the solid-state power amplifier. Autotransformer A3A9 contains capacitive and inductive components which are frequency bandswitched elements that translate antenna impedances to within the tuning range of C1 and L1. The inductive component, autotransformer (A3A9T1), is used exclusively for tuning the 8-foot whip antenna from 2 to 8 MHz. The antenna switch located on A3 is a mechanically interlocked switch that selects the proper tuning element in autotransformer A3A9. The switch is activated by the whip antenna. When the whip antenna is not connected, the capacitive components (A3A9C1 through C5 and C7) are automatically connected to the dipole antenna BNC connector.

a. Autotransformer A3A9. Refer to figure 1-22 in this section and to figures 4-16 and 4-24, schematics section. The autotransformer provides two frequency selective networks, one for use with a dipole antenna (capacitors C1 through C5 and C7) and one for use with a whip antenna (autotransformer T1 and capacitor C6).

The required value of capacitance (C1 through C5 and C7) is selected by bandswitch A3A5. The capacitance translates the dipole antenna impedances to within the tuning range of variable elements L1 and C1. The same is true for selecting autotransformer taps when using the whip antenna. Once antenna impedances are inside the tuning range, loading and phasing error signals run L1 and C1 to obtain the 50-ohm input impedance to the antenna.

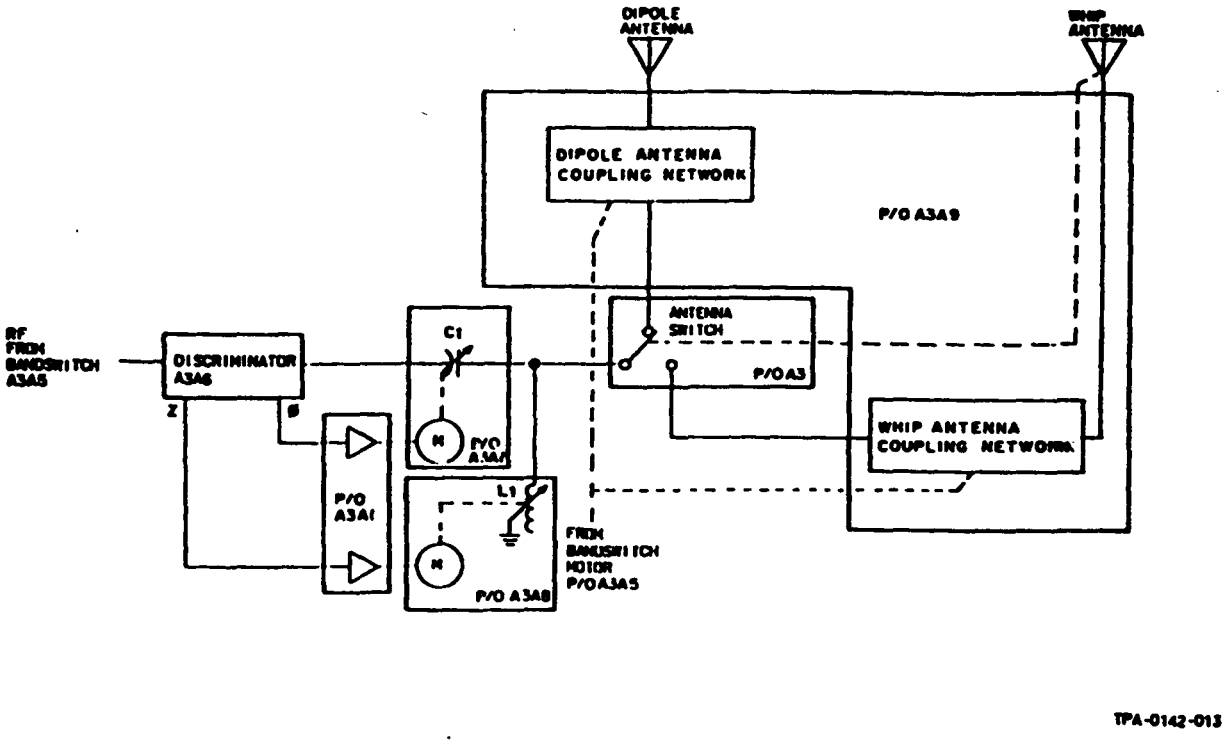


Figure 1-22. Rf Tuning Network, Simplified Schematic Diagram

Figure 1-23 shows how L1, C1, and capacitance (A3A9C1 through C5 and C7) are used to tune the antenna at one example frequency. Figure 1-24 shows the tuning procedure using the 8-foot whip antenna below 8.0 MHz. The auto transformer is switched out above 8.0 MHz.

When a whip antenna is connected, the amplifier-coupler antenna switch is mechanically switched to the normally open position. The rf is applied to switch wafers S1A and S1B of A3A9. Switch S1 is driven by bandswitch motor A3A5B1. At tuned frequencies from 2 to 7.9999 MHz, the rf is coupled through S1B to autotransformer T1. The autotransformer passes the rf through S1A to the whip antenna connector. From 8 to 23.9999 MHz, the rf is applied directly to S1A. From 24 to 29.9999 MHz, capacitor C6 provides capacitance for tuning the whip antenna.

When using the dipole antenna, the antenna switch remains in the normally closed position. The rf is applied to a contact on switch wafer S1C. Capacitors A3A9 C1 through C5 and C7 translate the antenna impedance within the tuning range of C1 and L1. The wiper arm of S1C applies the rf to the dipole antenna BNC connector.

b. Tuning Capacitor A3A7. Refer to figure 4-22, schematics section. The tuning capacitor is controlled by voltages (C1 max run and C1 min run) from servo amplifier A3A1. When a positive voltage is applied to A3A7P1-9 (C1 max run) and a ground to A3A7P1-10, current flows through the wiper arm of S1A to motor B1. Under this condition when B1 runs, the capacitance of C1 is mechanically adjusted toward maximum capacitance.

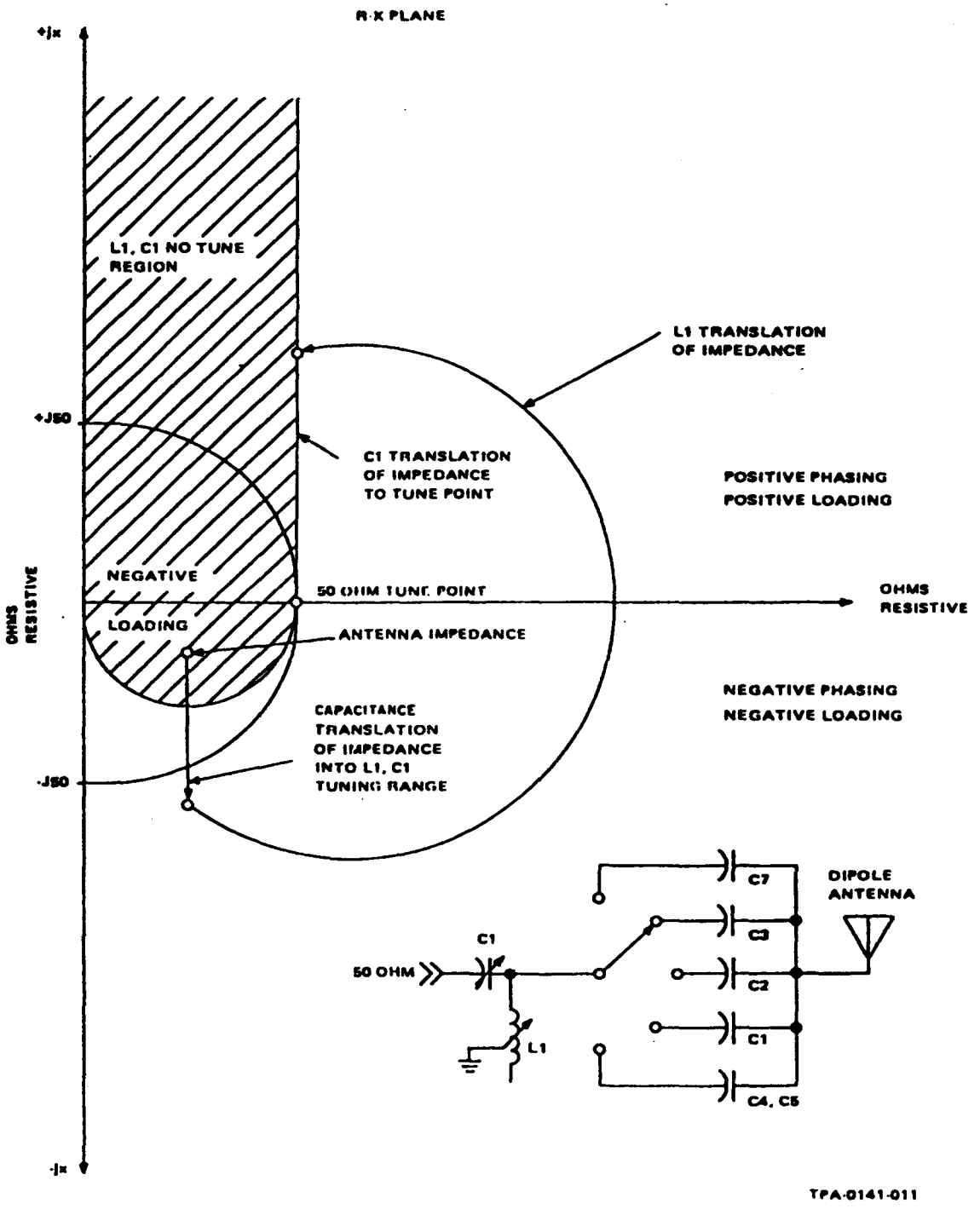


Figure 1-23. Tuning Procedure when C2 is required

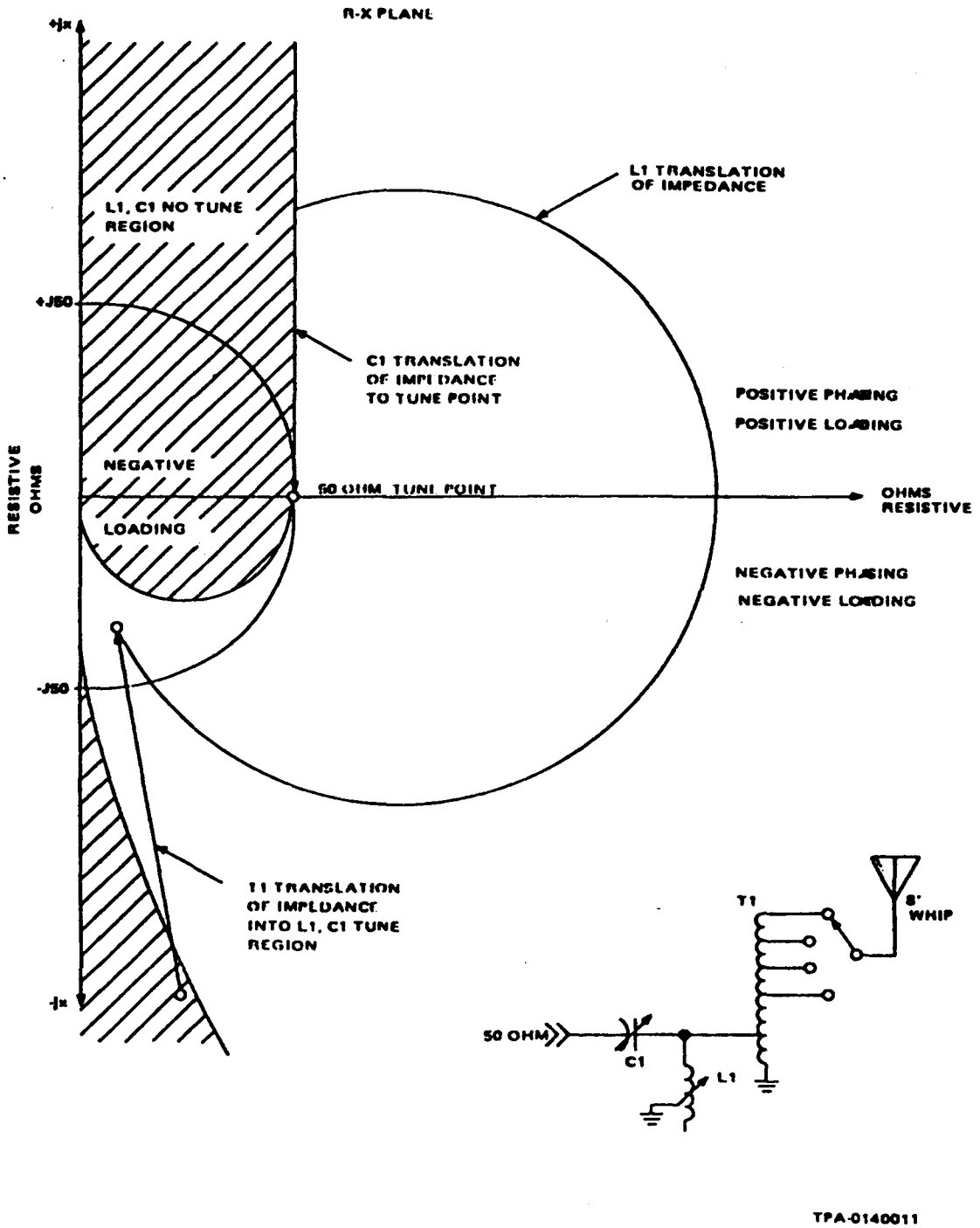


Figure 1-24. Tuning Procedure when T1 is used

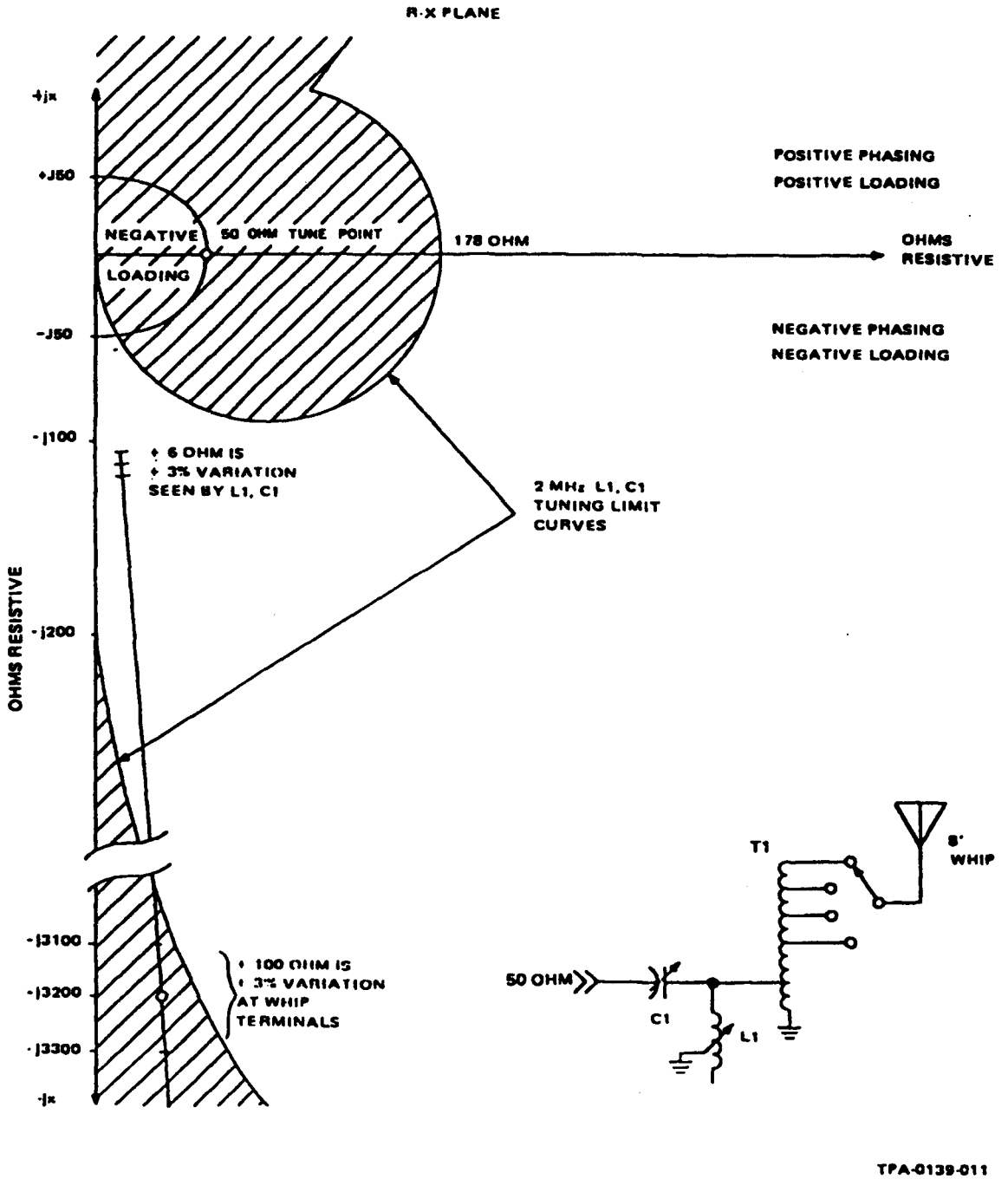


Figure 1-25. Whip Antenna Reactance Variation Reduction

S1A is mechanically connected to B1. S1A may rotate until the contact going to CR4 becomes open at maximum capacitance. When the contact opens, the voltage to B1 is removed and B1 stops. Switch S1B rotates while B1 is running. A ground established through S1B from A3A7P1-2, applies a ground at A3A7P1-5 to tell control logic A3A2 when C1 is maximum.

When a positive voltage is applied to A3A7P1-10 (C1 min run); current flows through B1 (red dot side) to the wiper arm of S1A and out through CR3. C1 max run (A3A7P1-9) is ground. B1 now runs to force C1 towards minimum and also rotates switches S1A and S1B. Switch S1A may continue to rotate until the contact going to CR3 becomes open, disabling B1. Switch S1B applies a ground to A3A7P1-6 to tell control logic A3A2 when C1 reaches a capacitance of 145 to 275 pf or less.

When logic conditions on control logic A3A2 are such that there is no forcing of the capacitor to max or min positions, the phasing voltage sample from the discriminator controls C1 position. Operation of the tuning capacitor is as discussed above, except that C1 is adjusted (toward max or min) only when a phasing voltage exists.

c. Tuning Coil A3A8. Refer to figure 4-23, schematics section. The tuning coil is positioned by L1 max run and L1 min run control voltages from servo amplifier A3A1. When a positive voltage is applied to A3A8P1-10 (L1 max run) current flows through CR1 and S1 to motor B1. L1 min run (A3A8P1-4) is ground. This condition forces B1 to run to maximum. At max inductance, the follower arm places a ground on A3A8P1-2 ($\overline{\text{L1 MAX}}$) and pulls switch S1 down to CR2. The ground at A3A8P1-2 tells control logic A3A2 that L1 is at maximum. When S1 is actuated, the current path is broken and the motor stops running. When a positive voltage is applied to A3A8P1-4 (L1 min run), current flows through servo B1, switch S2, and diode CR3. L1 max run (A3A8P1-10) is ground. This forces servo B1 to run to minimum. At minimum inductance, the follower arm places a ground on A3A8P1-9 ($\overline{\text{L1 MIN}}$) and pulls switch S2 down to CR4. The ground at A3A8P1-9 tells control A3A2 that L1 is at minimum. When S2 is actuated, the current path is broken and the motor stops running.

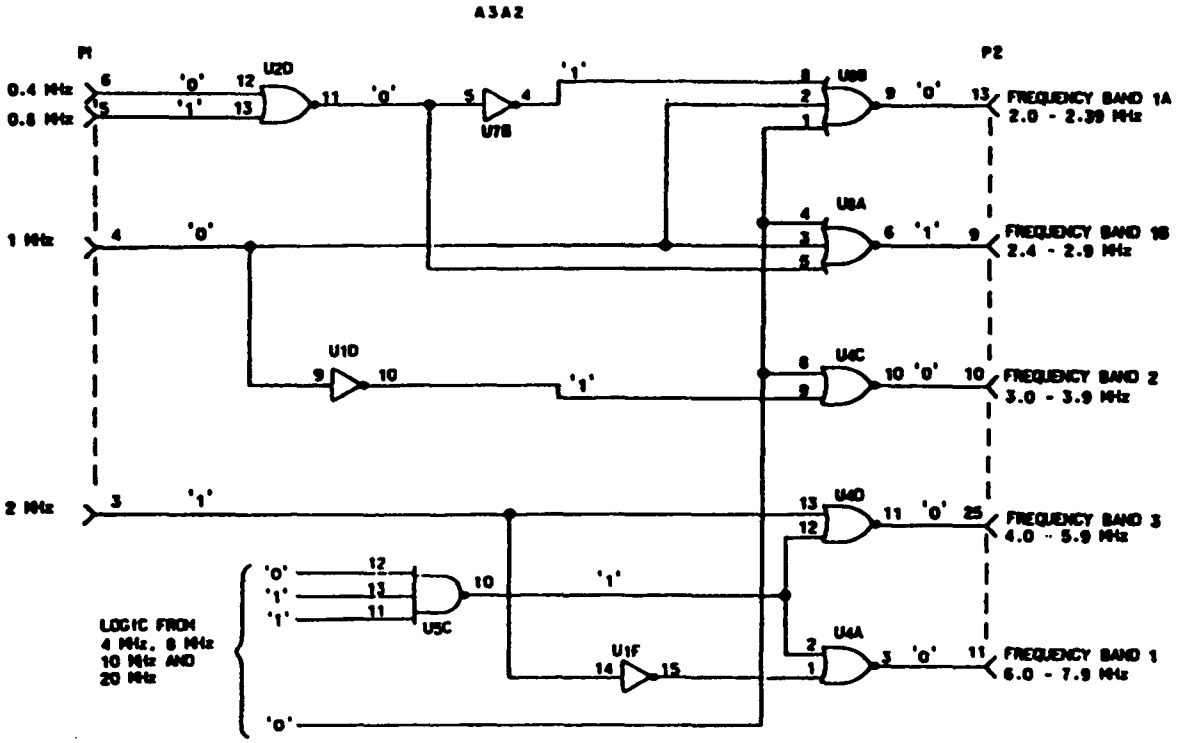
When logic conditions on control logic A3A2 are such that there is no forcing of the inductor to max or min positions, the loading voltage sample from discriminator A3A6 controls the tuning of L1. Operation of the tuning coil is as discussed above, except that L1 is adjusted (toward max or min) only when a loading voltage exists. The positive or negative voltage sample will cause L1 to run only until proper loading occurs (rf circuit impedance returns to 50 ohms).

A tab above the tuning coil is connected to the $\overline{\text{L1 Position}}$ output of A3A8. When a frequency 12 MHz or greater is selected a ground is applied by bandswitch A3A5 to the center-tap on the tuning coil L1. Should the roller make contact with the tab above 12 MHz, the ground is transferred to the $\overline{\text{L1 Position}}$ output and applied to control logic A3A2. Logic from A3A2 then disables the loading servo amplifier and the coil stops.

1.7.4.3.1.5 Control Logic A3A2

Refer to figure 4-17 schematics section. Control logic A3A2 receives binary coded decimal (bcd) frequency information, rechannel pulse (RCP STRETCH) and key line control from radio receiver-transmitter A1, servo enable from servo amplifier A3A1, and tuning coil/capacitor position logic from A3A7 and A3A8. The logic control supplies control logic signals for the amplifier-coupler, such as frequency band logic and servo command logic.

a. Frequency Decoding. Refer to figure 1-26. The bcd input from control A2 is decoded into frequency band information, see table 1-3. Band logic controls B1 on bandswitch module A3A5. High level logic is applied to the appropriate frequency line/lines on connector P1 of control logic A3A2. This logic is applied to various logic gates where



NOTE:

BCD FREQ INFORMATION FROM CONTROL = 2.8 MHz

TRUTH TABLE

NAND			NOR			INV	
A	B	C	A	B	C	A	B
0	0	1	0	0	1	0	1
1	0	1	1	0	0	1	0
0	1	1	0	1	0		
1	1	0	1	1	0		

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Figure 1-26. Frequency Band Logic, Simplified Schematic Diagram

FREQ BAND	FREQ RANGE	CONN PIN
1A	2.0 to 2.39 MHz	P2-13
1B	2.4 to 2.9 MHz	P2-9
2	3.0 to 3.9 MHz	P2-10
3	4.0 to 5.9 MHz	P2-25
4	6.0 to 7.9 MHz	P2-11
5	8.0 to 11.9 MHz	P2-28
6	12.0 to 15.9 MHz	P2-26
7	16.0 to 23.9 MHz	P2-20
8	24.0 to 29.9 MHz	P2-27

Table 1-3. Frequency Bands

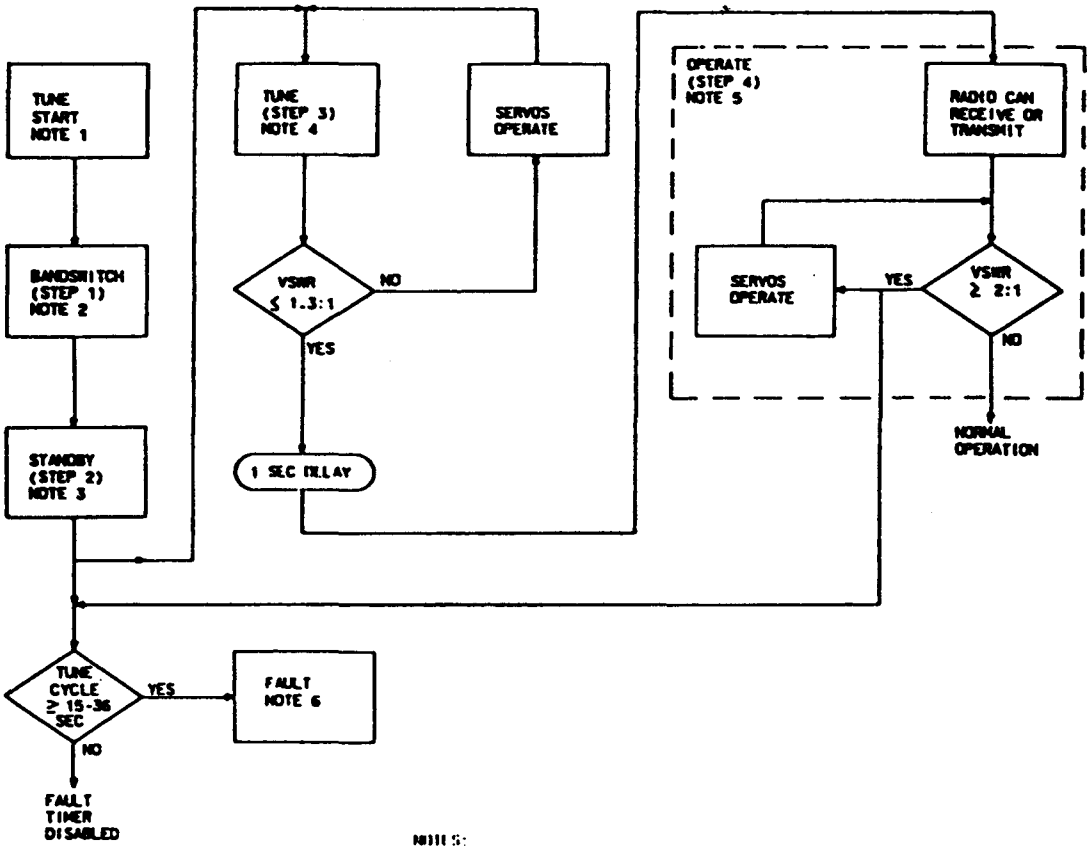
it is decoded and a logic 1 is applied to the proper connector pin on P2. This in turn enables B1 on bandswitch module A3A5. For example; assume an operating frequency of 2.8 MHz. Refer to figure 1-26. A logic 1 is applied to the 2.0 MHz and 0.8 MHz input (P1-3/5), all other frequency inputs are logic 0.

The bcd frequency logic, as shown in figure 1-26 is applied directly or indirectly through logic gates to the output gates for each frequency band. Note that output gate U8A, figure 1-26, is the only output gate with all logic 0 inputs to connector P1. Refer to the truth table in figure 1-26. A logic 1 output from U8A enables the 2.4 to 2.9 MHz frequency band (1B). All other outputs are logic 0 and the frequency bands (1A and 2 through 8) are disabled. Operation for decoding any frequency (2 to 29.9 MHz) is similar to the above example except the logic flow will change and the proper band for the selected frequency will be enabled.

At frequencies above 12 MHz, a high level logic is applied to the forcing circuits of the variable tuning elements (C1/L1) where it is used under certain conditions. This is covered in later paragraphs.

b. Tune Logic. Refer to figure 1-27. Coupler tuning is accomplished by four tuning steps (bandswitch, standby, tune, and operate) that control the logic to the servo amplifiers and ALC circuits.

Initial turn-on of primary power or the selection of a different frequency generates a rechannel pulse. The rechannel pulse sets the amplifier-coupler to tune step 1, bandswitch. The tuning sequence is illustrated in figure 1-27. A bandswitch complete signal plus coil (L1) position signal allows the logic to advance to step 2, standby. The sequence logic waits in standby for a key (key interlock) from the operator. The tuning elements are still positioned in the tuned condition for the last frequency. Upon receipt of a key (key interlock) the logic sequence goes to step 3, tune. When the tuning sequence is not in bandswitch and all bandswitching is complete, and a key interlock is



NOTES:

1. TUNE START — RECHANNEL PULSE RECEIVED WHEN POWER IS TURNED ON OR A NEW FREQUENCY IS SELECTED.
2. BANDSWITCH (STEP 1) — SWITCHED +25.2 V DC TURNED ON AND SYSTEM HELD IN UNKEYED CONDITION. BANDSWITCH COMPLETE PLUS COIL POSITION LOGIC, AMPLIFIER-COUPLER ADVANCES TO STANDBY.
3. STANDBY (STEP 2) — AMPLIFIER-COUPLER DORMANT AWAITING KEY (KEY INTERLOCK) TO ALLOW AMPLIFIER-COUPLER TO ADVANCE TO TUNE.
4. TUNE (STEP 3) — AMPLIFIER-COUPLER ELEMENTS TUNE, LEAVES TUNE AND ADVANCES TO OPERATE WHEN FWD PWR IS PRESENT AND VSWR IS LOW.
5. OPERATE (STEP 4) — KEYED OR UNKEYED, RECEIVE THROUGH A TUNED AMPLIFIFR-COUPLER IN RECEIVE, TRANSMIT WITH KEY. IF IN TRANSMIT AND SYSTEM DETECTS HIGH VSWR (2:1 FOR 1.5 SECONDS OR MORE) ELEMENTS ARE ALLOWED TO TUNE TO RESTORE LOW VSWR.
6. FAULT — TUNE FAULT IF SYSTEM DOES NOT TUNE IN ALLOTED TIME, REQUIRES NEW RECHANNEL PULSE TO RESET.

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Figure 1-27. Tune Sequence Flow Diagram

present, transistor switch Q2 applies a ground to A3A2P1-11. This ground actuates keyline relays in power amplifier A3A4 to pass the rf to bandswitch A3A5.

In tune, the following signals are used to control the tune cycle:

Servo amplifier enable	enables servos and allows elements C1 and L1 to tune
Tune-in-progress (TIP) signal to power amplifier	places power amplifier in a tune mode
TIP to radio receiver-transmitter A1	places radio receiver-transmitter A1 in a tune mode, which supplies a CW tone for tuning
Sidetone control to radio receiver-transmitter A1	rf present in receiver-transmitter A1 sidetone control circuits, which in turn generates a sidetone in the operators headset.

Forward rf power and low vswr ($\overline{\text{VSWR}}$) logic from servo amplifier A3A1 indicates that rf is present and the transmission line to the power amplifier is tuned to 50+ JO ohms to within 1.3:1 vswr. Approximately 1 second after the amplifier-coupler is tuned to 1.3:1 vswr with forward power present, the tuning sequence advances to step 4, operate. In operate, anytime the vswr indicates a mismatch of greater than approximately 2:1 for more than the allotted time delay, the servo amplifiers are enabled. The amplifier-coupler retunes until the vswr is low and the fixed delay expires, then it returns to normal operate. The vswr logic to enable the servos is delayed each time the vswr increases or decreases to provide noise immunity and allow the servos to pull-in as accurately as possible.

The tune cycle is timed by a fault circuit, see figure 1-27. If the tune cycle exceeds 15 to 36 seconds the system will fault. If a fault occurs, the tuning sequence must be reset with a tune start (rechannel) pulse.

1. Bandswitch Step. Refer to figure 1-28. The rechannel pulse ($\overline{\text{RCP STRETCH}}$) applies a 50 ms ground (logic 0) to U20D. This sets the bandswitch flip-flop (U20D and U21C). This same low level pulse is applied to U20B and resets the fault flip-flop (U20A and U20B). Simultaneously a logic 0 is gated through U14D and U15E and resets the standby, tune, and operate flip-flops. When the bandswitch flip-flop is set, the logic 1 output of U20D is applied to servo enable U9B. The output of U9B drives the circuit to energize relay A3A3A1K1. This enables +25.2 V dc (KEYED). Gate U20D also supplies a logic 1 to U21A. The logic 0 output of U21C is applied to the input of U11D. If the frequency is higher than 12 MHz and the roller on the tuning coil is contacting the L1 position tab, a logic 0 from U13D is applied to the other input of U11D. The logic 1 out of U11D enables the servo and forces the roller toward MIN until it breaks contact with the tab, at approximately mid-coil. The output of U13D changes to a logic 1 and is applied to the input of U21A. The logic 0 output of U21C is also applied to U18C to hold the power amplifier in an unkeyed condition.

   When bandswitch motor B1 on A3A5 stops running, ground is removed from the bandswitch complete circuit and a logic 1 is applied to the input of U21A. When the bandswitch flip-flop is set, bandswitch is complete, and the roller on the tuning coil is not making contact with the L1 position tab (if over 12 MHz) all inputs to U21A are logic 1. When all inputs to U21A are at logic 1, the tuning sequence advances to standby.
2. Standby Step. The logic 0 output of U21A sets standby flip-flop (U20C and U21B). The logic 0 output of U20C is applied to the input of U17C. The logic 0 output of

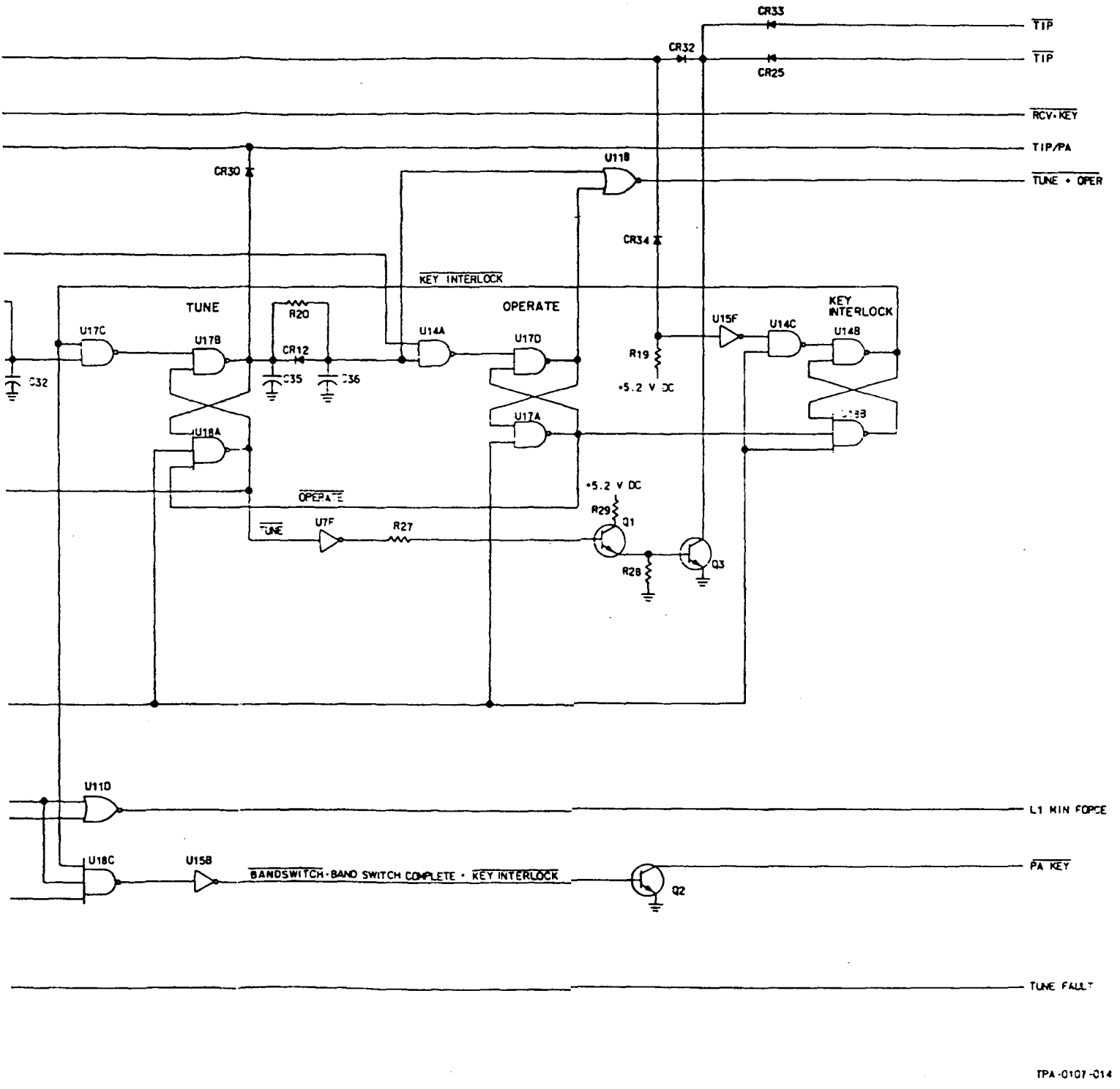

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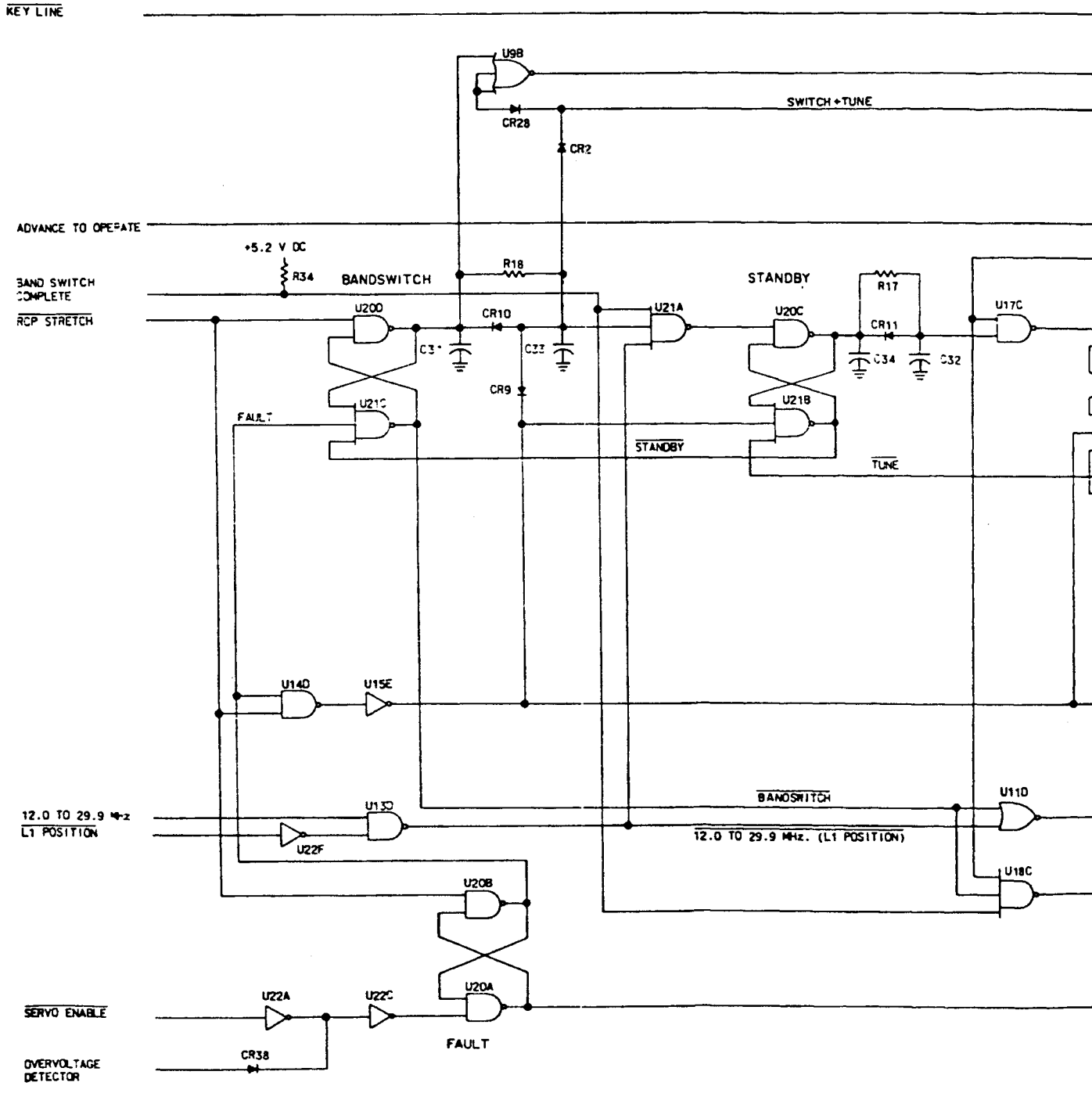
Figure 1-28. Control Logic A3A2, Simplified Schematic Diagram


KEY LINE
U9B
SWITCH+TUNE
CR28
CR2
ADVANCE TO OPERATE
+5.2 V DC
R34
BAND SWITCH COMPLETE
BANDSWITCH
R18
STANDBY
R17
RCP STRETCH
U20D
CR10
U21A
U20C
CR11
U17C
C31
C33
C34
C32
CR9
U21C
U21B
FAULT
STANDBY
TUNE
U14D
U15E
12.0 TO 29.9 MHz
L1 POSITION
U13D
U22F
BANDSWITCH
U11D
12.0 TO 29.9 MHz. (L1 POSITION)
U18C
U20B
U20A
U22A
U22C
SERVO ENABLE
FAULT
OVERVOLTAGE DETECTOR
CR38

U21B is fed back to U21C to reset the bandswitch flip-flop. In standby the radio may receive but transmission is inhibited. The tuning elements are still in their previously tuned positions unless the radio is in the RCV only mode. In the RCV only mode the tuning coil and capacitor are homed to maximum, however, the RCV only mode is used only during testing with Radio Test Set AN/PRM-501.

When the standby flip-flop is set and the radio keyed (key interlock) both inputs to U17C are logic 1. When both inputs to U17C are at logic 1 the tuning sequence advances to tune.

When a ground is applied to the keyline, a logic 0 is gated through U15F and U14C to set key interlock flip-flop U14B and U18B. The logic 1 output of U14B is applied back to the input of U17C and also to U18C to remove the power amplifier key inhibit.

3. Tune Step. When both inputs to U17C are at logic 1, the logic 0 output sets tune flip-flop U17B and U18A. The logic 1 output of U17B is applied through CR30 to enable the servos and applied through R20 to the input of U14A. The logic 0 output of U18A supplies the feedback to reset the standby flip-flop and also applies a logic 0 to U7F. The logic is inverted by U7F, amplified by Q1, and switched by Q3, placing a ground on the keyline and applying TIP logic low to radio receiver-transmitter A1. The radio receiver-transmitter turns on the rf and allows the amplifier-coupler tuning elements to tune. Discriminator A3A6 samples the rf and provides phasing and loading information to servo amplifier A3A1. A3A1 determines when the vswr is 1.3:1. When the vswr is correct and forward power is present, an advance to operate signal (logic 1) is applied to the input of U14A.

   When the tune flip-flop is set and an advance to operate logic 1 is supplied by A3A1 both inputs to U14A are at logic 1. When both inputs to U14A are at logic 1 the tuning sequence advances to step 4, operate.

4. Operate Step. The logic 0 output of U14A sets the operate flip-flop, U17D and U17A. The logic 1 output of U17D ($\overline{\text{operate}}$ or $\overline{\text{tune}}$) is applied through U11B to the L1/C1 forcing circuits. The logic 0 output from U17A is fed back to U18A to reset the tune flip-flop. This reset condition releases the hold on the keyline and TIP line applied by transistor switch Q3. In operate step, the amplifier-coupler is tuned and ready to transmit or receive as long as the vswr remains 1.3:1. Should the vswr vary, and forward power is present, the servos will be enabled until the amplifier-coupler is retuned to the correct vswr.

5. Tuning Coil/Capacitor Forcing Logic. Logic gating on control logic A3A2 determine the conditions under which the tuning elements (C1/L1) are forced to run toward maximum or minimum position. The developed forcing logic is applied to servo amplifier A3A1.

   Refer to figure 1-29. When the following logic conditions are set, C1 max forcing logic is applied to the servo amplifier forcing C1 to maximum: L1-Min, C1-Min, ($\overline{\text{12 to 29.9 MHz}}$) and (operate or tune) step. With these conditions, logic 0's are applied to the inputs of U11A and U10A. The logic 1 outputs of U11A and U10A are applied to U19B. The logic 0 output of U19B sets flip-flop U19C and U16A. The logic 1 output of U19C is applied through A3A2P3-15 to servo amplifier A3A1 which forces C1 to maximum position. If L1 runs off minimum or C1 hits maximum, the force flip-flop will reset disabling the forcing functions.

   Refer to figure 1-30. When the following logic conditions are set, L1 Max forcing logic is applied to the servo amplifier forcing L1 to maximum: L1 at Min, C1 at Max while in operate or tune. With these conditions, logic 0's are applied to the inputs of U10B and U22E. The logic 1 outputs of U10B and U22E are applied to U19A. The logic 0 output of U19A sets flip-flop U19D and U16B. The logic 1 output of U19D is applied through A3A2P3-8 to servo amplifier A3A1 which forces L1 to maximum position.

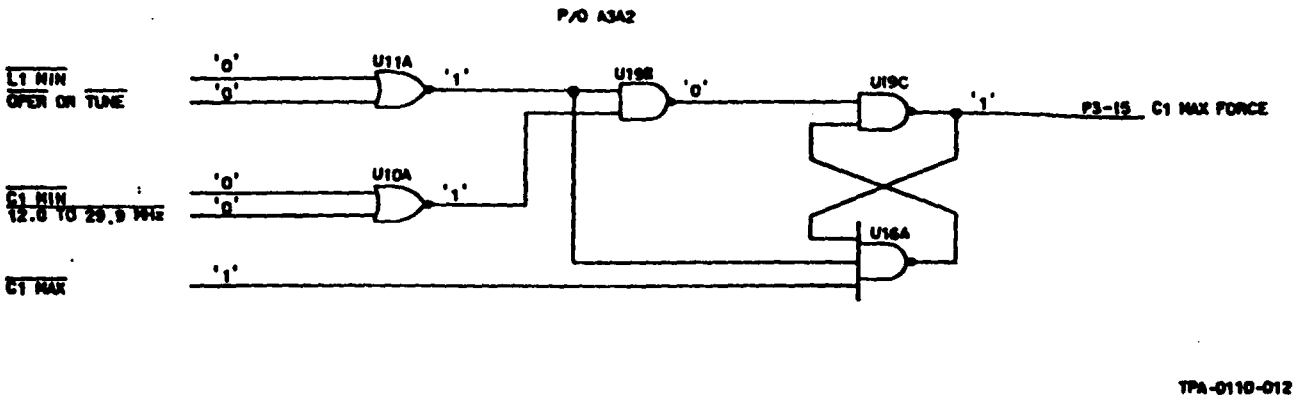


Figure 1-29. C1 Max Forcing Logic, Simplified Schematic Diagram

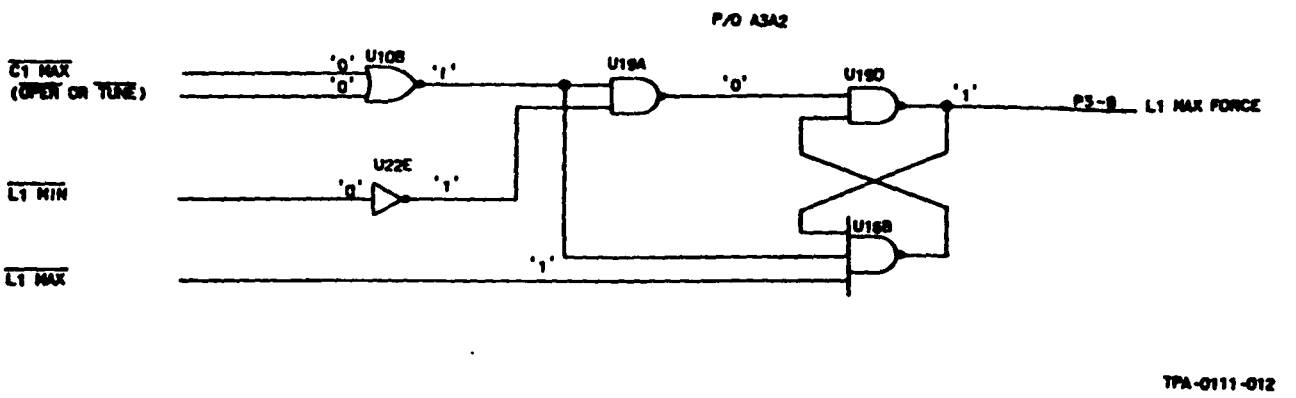


Figure 1-30. L1 Max Forcing Logic, Simplified Schematic Diagram

Refer to figure 1-31. When the following logic conditions are appropriately set, L1 Min forcing logic is applied to the servo amplifier forcing L1 toward minimum position: frequency below 12 MHz (12 to 29.9 MHz), L1 Position, L1 Max, C1 Max and (operate or tune). With these conditions, a logic 1 is inverted through U22F and applied, along with a logic 0 from the 12 to 29.9 MHz logic, to the input of U13D. The logic 1 output of U13D and a logic 0 from L1 Max are applied to U13C. Logic 0's from C1 Max and (operate or tune) are applied to the inputs of U10B. The logic 1 output of U10B and the logic 1 output of U13C are applied to the input of U13B. The logic 0 out of U13B sets flip-flop U13A and U16C. The logic 1 output of U13A is applied through A3A2P3-9 to servo amplifier A3A1 which forces L1 toward minimum position. If the frequency is above 12 MHz and L1 roller is making contact with the tab and in bandswitch tuning step, logic 0's are applied to U11D. The logic 1 output of U11D is applied through A3A2P3-9 to the servo amplifier which forces L1 toward minimum position until the roller breaks contact with the tab. Above 29 MHz the coil will force to min if C1 hits max while in the tune or operate step. The flip-flop will reset if L1 hits min or C1 comes off max or phasing sense becomes positive.

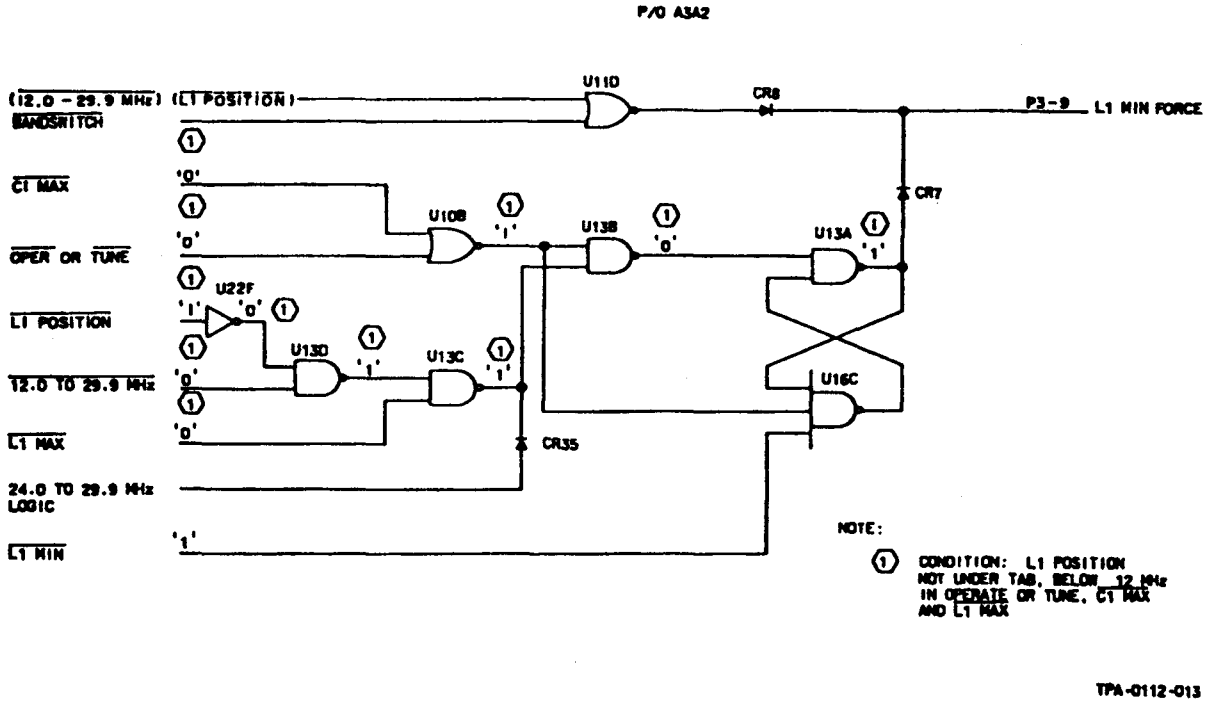


Figure 1-31. L1 Min Forcing Logic, Simplified Schematic Diagram

Positive phasing sense logic from servo amplifier A3A1 applies a logic 1 to U10B. The logic 0 output of U10B is inverted by U13B (L1 Min Force) and U19A (L1 Max Force) and resets the L1 forcing flip-flops, disabling the forcing logic and allowing the servos to control the tuning.

c. Fault Logic. Refer to figure 1-28. When the servos are enabled a logic 0 is applied by the servo amplifier to U22A in the fault circuit. The logic 0 is inverted by U22A and applied to the fault timing network. If the radio fails to tune within 15 to 36 seconds, the logic 1 is inverted by U22C and applied to the fault flip-flop, U20A and U20B. The logic 1 output of U20A (tune fault) is applied to the system. If a tune fault occurs, a logic 0 from U20B resets all the tune step flip-flops to 0 status and tuning stops. A new tune start pulse must be initiated to start a new tuning sequence. At any time the rf signal level becomes too high, overvoltage detector A3A3A2 applies a logic high through CR38 to U22C. This will also fault the tuning sequence.

Overvoltage detector A3A3A2, refer to figure 4-15 in diagrams section, provides rf sampling to protect amplifier-coupler A3 from damage due to abnormally high signal levels. The rf (approximately 850 volts peak) is sampled at the junction of the tuning coil and the tuning capacitor, and applied to A3A3A2. The rf is then filtered, rectified by CR5, and integrated by C4 to provide a normalized dc voltage to the noninverting input of U1A. A filtered 5.1 V dc is developed across zener VR1 and the inverting input of U1A. When the rectified dc voltage exceeds 5.1 volts, comparator U1A develops a positive output voltage. This positive voltage is applied to the control logic card as a fault initiate command, indicating an abnormally high level of rf.

1.7.4.3.1.6 Servo Amplifier A3A1

Refer to figure 4-17, schematics section. The servo amplifier is a dc amplifier capable of operation from a battery supply voltage of 22 to 30 V dc. The servo amplifier receives loading and phasing error voltages, forward and reflected power logic from discriminator A3A6 and forcing logic from logic control A3A2. The servo amplifier converts forcing logi and error voltages into servo drive signals to cause the tuning coil and capacitor to run towards maximum or minimum position. The servo amplifier also develops phasing sense, vswr comparison, servo controls, ALC, and sidetone voltages.

a. Tuning Coil/Capacitor Run Control. When the tuning coil forcing logic is low (both L1 max force and L1 min force), the loading sample from the discriminator A3A6 controls op amp U1A. When the loading voltage is positive (rf impedance more than 50 ohms), the output of U1A decreases, causing the output of U2B to increase, which supplies a positive voltage output at A3A1J4-4. Since U2A is now low, a ground is applied to A3A1J4-10. This forces L1 to run toward minimum. When the rf circuit impedance adjusts to 50 ohms, the loading voltage becomes zero and L1 stops running. When the loading is negative (rf impedance less than 50 ohms), the output of U1A increases, causing the output voltage of U2A to increase which supplies a positive voltage output at A3A1J4-10 to force L1 to run toward maximum. Again, when the rf circuit impedance adjusts to 50 ohms, L1 stops running. When forcing logic from A3A2 activates L1 min force or L1 max force, the forcing logic levels override the loading input. A logic '1' on the L1 min force input (A3A1J1-9) will cause a positive voltage output at A3A1J4-4 as described above. A logic 1 on the L1 max force input (A3A1J1-8) will cause a positive voltage output at A3A1J4-10, as described above. However, should the tuning coil-tab contact the roller while tuned to a frequency greater than or equal to 12 MHz, transistor Q12 is cut off. This condition back biases FET Q16 and removes Q5 and Q22 from the circuit. An open circuit appears at A3A1J4-4 which stops the tuning coil from running toward minimum.

   The phasing input from the discriminator controls op amp U1B. Logic from A3A2 applies C1 max force and C1 min force logic commands. Circuit operation is the same as that discussed above for the loading and tuning coil forcing logic.

b. Phasing Sense. The phasing input from the discriminator is applied to the noninverting input of U5B. When there is positive phasing the output of U5A develops a logic high voltage across VR8 which is applied to control logic card A3A2.

c. Vswr and Forward Power. Refer to figure 1-32. Both the forward power and the reflected power samples from discriminator A3A6 are applied to U4B. The input networks to U4B allow the forward and reflected power to be compared and a vswr check to be made. When the vswr is 1.3 to 1 a logic 1 is applied to NOR gate U6A. The logic is inverted by U6A and applied, along with logic from the forward power circuit, to U6B. (When forward power is present a logic 0 is applied to U6B.) The logic 1 output of U6B (advance to operate) is applied to control logic A3A2. Simultaneously a logic 1 is applied through a time delay network to U6D. When forward power is present, U4A applies a logic 0 to U6D. The logic 0 output of U6D, along with a logic 0 (servo enable) from A3A2 is applied to U6C. If the vswr is 1.3 to 1 and forward power is present, the output of U6C is a logic 1. The logic 1 enables transistor Q13 which in turn disables transistor Q9, removing +25.2 V dc (Keyed, filtered and enabled) thereby disabling the servo amplifiers. U6C also provides the servo enable logic to the fault circuit on A3A2. When the vswr is not 1.3 to 1 and forward power is present, a logic 0 is applied through the time delay network to U6D. The output of U6D changes to a logic 1, the output of U6C goes to a logic 0 and cuts off Q13 and allows Q9 to conduct applying +25.2 V dc (Keyed and Fltr) to servo op amps as +25 V dc (Keyed, fltr and enabled). The servos are enabled and the amplifier coupler retunes until the vswr is at the proper ratio then the tuning sequence goes back into the operate step.

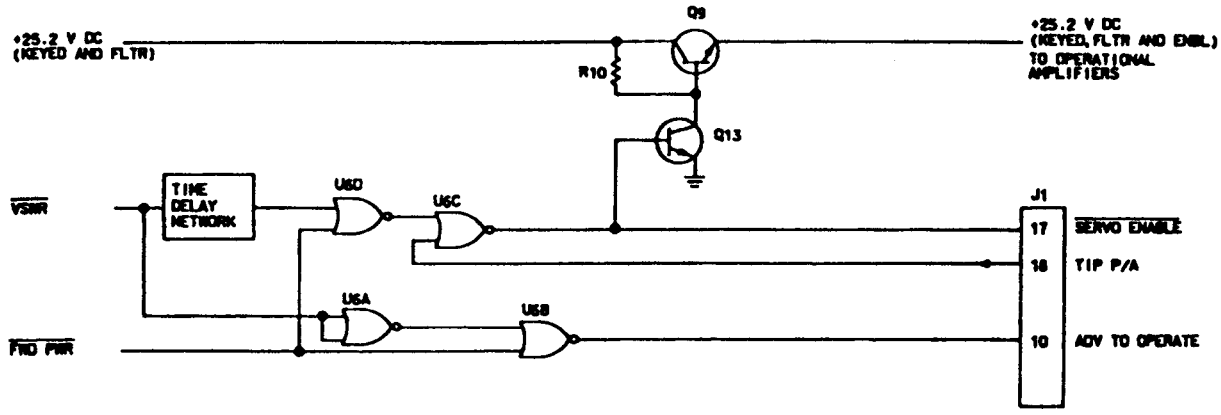


Figure 1-32. Forward Power to Vswr Comparison and Servo Enable, Simplified Schematic Diagram

d. ALC and Sidetone. In the tune mode (tune step 3) the detected ALC voltage from the discriminator controls the ALC output voltage from U5B. The cathodes of CR3 and CR1 are grounded by TIP. This disables the bias supplied through R37 and enables Q17. The ALC detector voltage from the Q17 is much higher than the forward power voltage supplied from the discriminator. As a result the ALC detector controls U5B. However, if the reflected power is too high, resistor R82 will feed bias to U5B and the forward power will be decreased.

In operate, Q17 is biased off and the output of U5B is controlled by forward power. The cathodes of CR1 and CR3 are no longer grounded. If low power is requested (P1-19 grounded) Q17 will turn on and the ALC detector will control the output of U5B.

Sidetone enabling is controlled by current summing op amp U5B. The sidetone (A3A1P1-25) is applied during tune and operate when rf is present. Five current sources feed the inverting input. When the current through R82 (reflected power) plus the current through R6 (forward power plus the current through Q17 (ALC)) is equal to the current through R33 (reference) plus the current through R36 (drive), the output of U5B goes negative. This condition turns Q10 on and applies a logic 0 to A3A1P1-25 (RF POWER) to activate the sidetone.

The servo amplifier also contains an internal -12 V dc supply circuit. Inverters U7A and U7B are tuned by R70 and C39 to develop a 20 kHz square wave. The square wave switches Q11, Q26, and Q14 on and off and controls the biasing of CR11. Zener diodes VR4 and VR5 then develop -12.4 V dc at the base of Q15, causing Q15 to conduct and -12 V dc to develop at the emitter lead.

1.7.4.3.2 Receive Theory

The following paragraphs contain a description of the rf signal path from the antenna to radio receiver-transmitter A1. For more detail on any particular module, card, or sub-assembly refer to the description of the transmit path, paragraph 1.7.4.3.1.

When using a dipole antenna, the received rf is coupled through autotransformer A3A9 wafer switch section S1C, and through its associated capacitive network to the antenna switch. When using a whip antenna, the received rf is coupled through autotransformer A3A9 wafer switch section S1A and either capacitor C6, autotransformer T1 and S1B, or directly to the antenna switch. Autotransformer T1 is used for frequencies from 2 to 7.9999 MHz only and capacitor C6 is used for frequencies from 16 to 23.9999 MHz only. The antenna switch is toggled when the whip antenna is connected.

The rf signal from the antenna switch is applied to tuning coil A3A8L1, tuning capacitor A3A7C1, and overvoltage detector A3A3A2. The tuning coil and tuning capacitor are tuned to optimum receive conditions by logic applied by servo amplifier A3A1 and control logic A3A2. Optimum receive conditions occur when the control logic is in the standby step of the tuning sequence. The overvoltage detector provides a fault initiate signal to A3A2 should the rf signal get too high.

The rf is then coupled through the discriminator to bandswitch A3A5. The bandswitch module contains two filter boards, each having four bandpass filters. The appropriate filter is selected by the bandswitch step of the tuning sequence. The band filtered rf is then applied to the power amplifier.

Relay A3A4A2K2 is deenergized when receiving. The received rf is passed to rf assembly A3A4A1. Relay A3A4A1K1 is also deenergized when receiving. The received rf is then passed through the relay to receiver-transmitter A1.

1.7.4.4 DC Power Distribution

Refer to figure 1-33. The receiver-transmitter group operates from a 25.2-volt (+5, -3 V dc) battery connected to A3J2. Four terms are used to functionally label the 25.2 volts dc shown on figure 1-33.

+25.2 V dc	voltage applied to the receiver-transmitter group when the battery is connected.
+25.2 V dc (keyed)	voltage applied when the receiver-transmitter group is keyed.
+25.2 V dc (SW)	voltage applied when switched on at the control.
+25.2 V dc (SW and filtered)	switched voltage filtered by the circuits discussed in paragraph 1.7.4.2.5.

The +25.2 volt dc battery voltage is applied from connector A3J2-1 to fuse A3A3A1F1. From the fuse, the +25.2 V dc voltage is routed to relay A3A3A1K1, A3J1-24 and -30, and A3A3A1J1-21 for distribution. When A3A3A1K1 is energized by keying the equipment, +25.2 V dc (KEYED) voltage is supplied to A3A1P1-13, A3A2P1-13, A3A4A1J1-3 and A3A4A2P1-3.

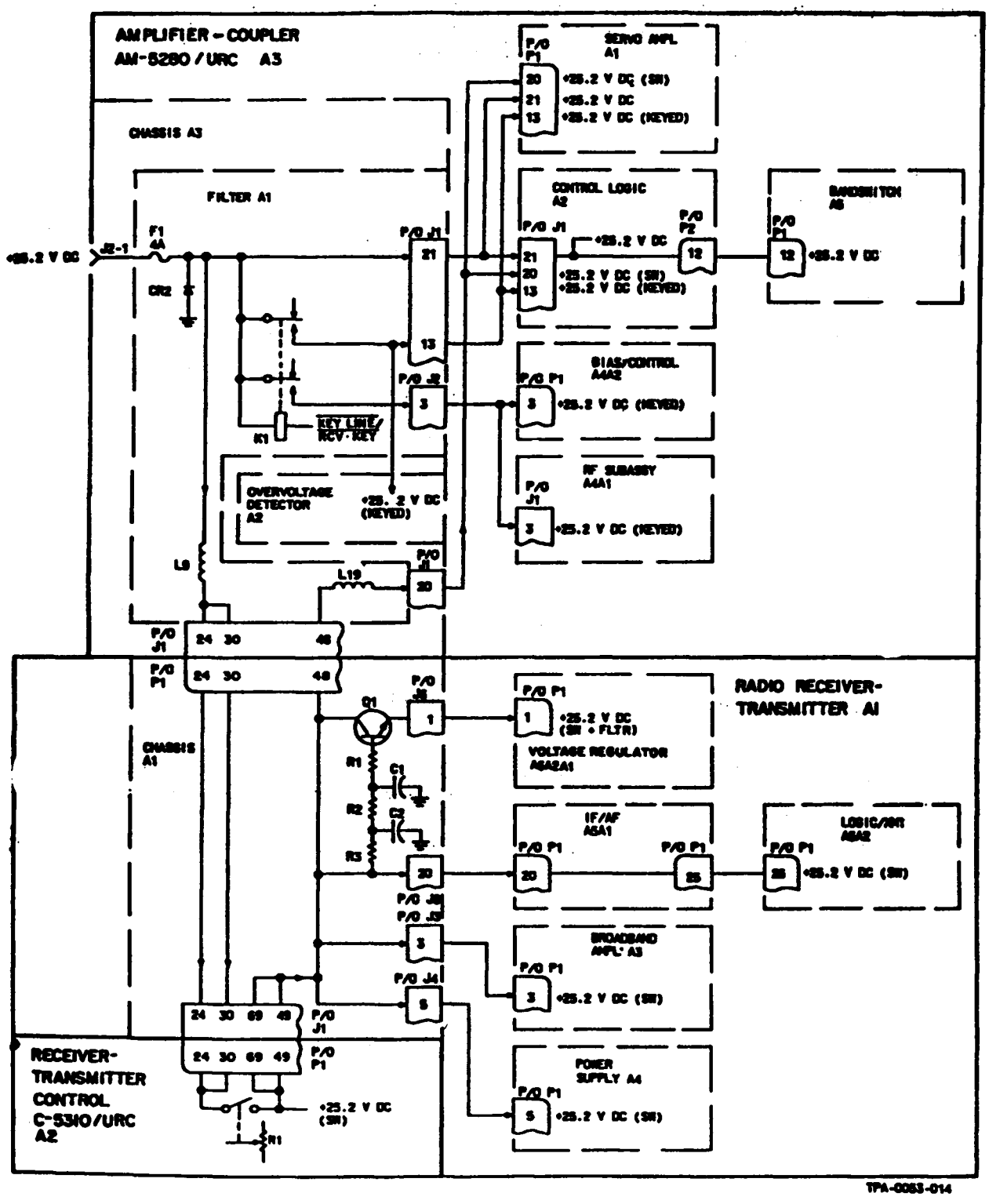


Figure 1-33. Receiver-Transmitter Group OR-5007/URC, DC Power Distribution Diagram

The +25-volt voltage is distributed to A3A1, A3A2 and A3A5, and is connected to the O section of A2R1 through connectors A3J1/A1A1P1-24, -30 and A1A1J1/A2P1-24, 30. W the receiver-transmitter group is turned on at the control, the +25.2 volts dc becomes +25.2 V DC (SW) which is applied to A2P1/A1A1J1-36, -49 for distribution (figure 1-33 The switched dc output of A1A1Q1 becomes +25.2 V DC (SW AND FLTR) and is applied to A1A6.

The +25.2 DC (SW) is applied to A1A4P1-5 and converted to regulated +5.2 and +13 volt +5.2 V DC is applied to A1A4P1 -1 and +13 V DC to A1A4P1-7 for distribution.

1.7.5 Direct Current Generator G-5002/PRC-515 Detailed Theory

Refer to figure 4-28, schematics section. The generator consists of a crank generator, a voltage regulator circuit, and a current output indicator circuit. The dc output of the hand crank generator is applied through the CR1-CR4 bridge circuit to a series voltage regulator, Q1, Q2, and Q4. Primary current flow is through series transistor Q1, curr sensing resistor R1, and diode CR5. Diode CR5 prevents battery discharge back throug the generator when it is not being operated.

For low input voltage levels (slow cranking speeds), drive transistor Q2 and series tran tor Q1 are on (control transistor Q4 is in cutoff) and the output voltage follows the input voltage. Output voltage is fed back through the voltage divider R7 and R8 to the base of control transistor Q4. VR2 is the threshold reference diode that allows Q4 to turn on wh the voltage across R9 is equal to Q4 emitter-base drop plus 5.1 volts.

When the output voltage reaches approximately +30 V dc, base drive supplied by voltage divider R7 and R9 is sufficient to turn on Q4. The conduction by Q4 diverts base drive away from Q2. Q2 and Q1 conduct less, Q1 collector to emitter voltage increases, and the output voltage is maintained at approximately 30 V dc.

The green (DS1) and red (DS2) crank speed indicator lamps are controlled by a current sensing circuit made up of R1, Q3, Q5, Q6, and VR1 and VR3. As output current increas the voltage drop across current sensing resistor R1 also increases. The voltage drop across R1, which is in the Q3 base to emitter path, controls current flow through Q3. Wi an output current flow of between 40 and 150 mA, there is sufficient current flow through Q3 to cause Q5 to turn on and light lamp DS1. With an output current of between 150 and 300 mA, there is sufficient current flow through Q3 to cause Q6 to turn on and light lamp DS2.

Missing pages:

SECTION II: Maintenance

SECTION III: Parts List

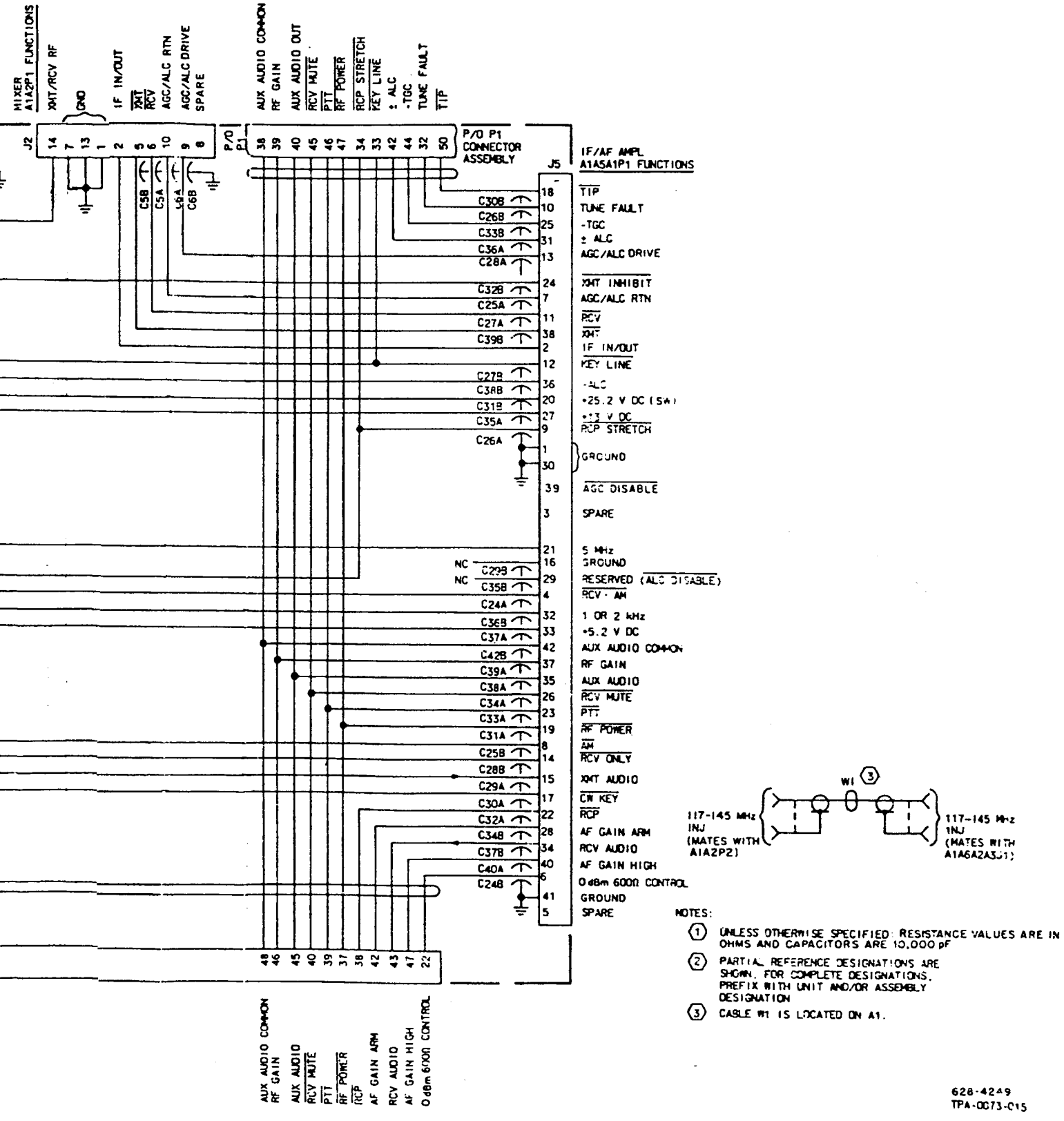
SECTION IV

SCHEMATICS

4.1 GENERAL

Schematic diagrams are included for Receiver-Transmitter Group OR-5007/URC, Handset H-5017/PRC-515, Handset-Microphone H-5016/PRC-515, Electrical Power Cable Assembly CX-5229/PRC-515, and Direct Current Generator G-5002/PRC-515. The schematic diagram titles and figure numbers are:

FIGURE	TITLE
4-1	Chassis A1A1, Schematic Diagram
4-2	Mixer A1A2, Schematic Diagram
4-3	Broadband Amplifier A1A3, Schematic Diagram
4-4	Power Supply A1A4, Schematic Diagram
4-5	If/Af A1A5A1, Schematic Diagram
4-6	Logic/Tx A1A5A2, Schematic Diagram
4-7	Frequency Standard A1A6A1A1, Schematic Diagram
4-8	Fixed Frequency Divider A1A6A1A2, Schematic Diagram
4-9	Lf Phase-Lock Loop A1A6A1A3, Schematic Diagram
4-10	Frequency Converter A1A6A1A4, Schematic Diagram
4-11	Voltage Regulator A1A6A2A1, Schematic Diagram
4-12	Variable Frequency Divider A1A6A2A2, Schematic Diagram
4-13	Hf Phase-Lock Loop A1A6A2A3, Schematic Diagram
4-14	Receiver-Transmitter Control A2, C-5310/URC, Schematic Diagram
4-15	Amplifier-Coupler A3, AM-5280/URC, Schematic Diagram
4-16	Servo Amplifier A3A1, Schematic Diagram
4-17	Control Logic A3A2, Schematic Diagram
4-18	RF Subassembly A3A4A1, Schematic Diagram
4-19	Bias/Control A3A4A2, Schematic Diagram



NOTES:

1. UNLESS OTHERWISE SPECIFIED: RESISTANCE VALUES ARE IN OHMS AND CAPACITORS ARE 10,000 pF
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATIONS, PREFIX WITH UNIT AND/OR ASSEMBLY DESIGNATION
3. CABLE W1 IS LOCATED ON A1.

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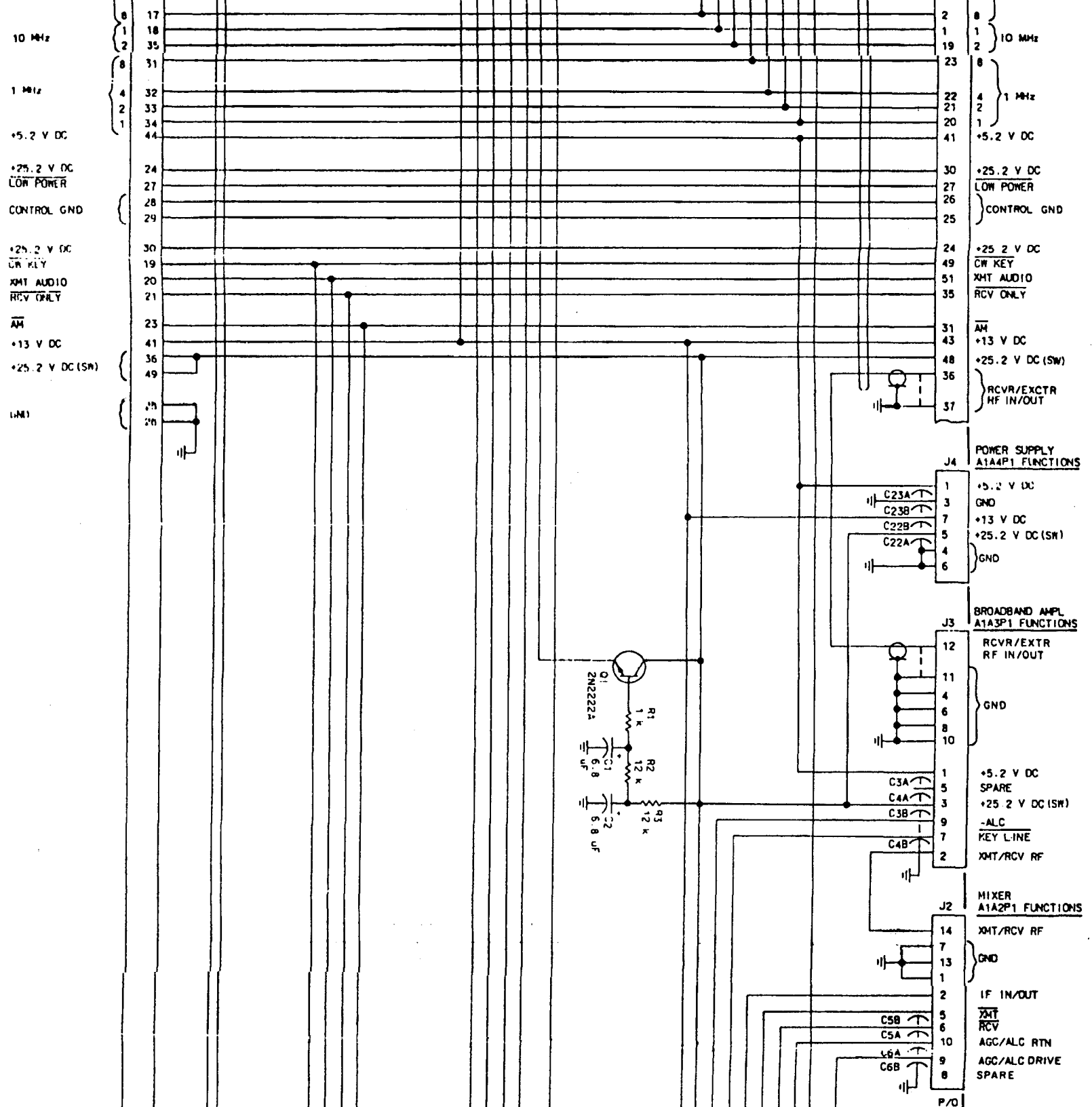
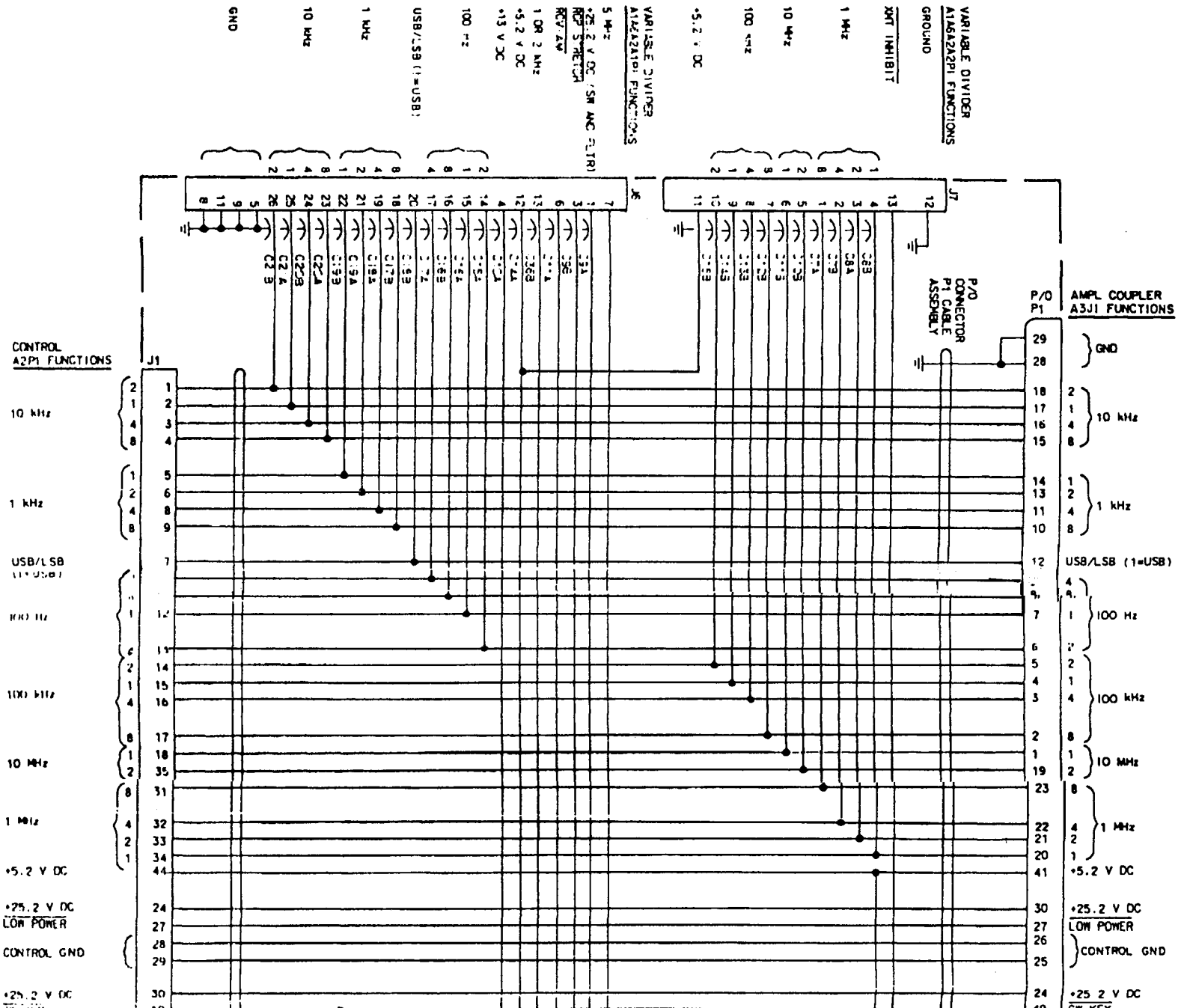
TPA-0073-015

Figure 4-1. Chassis A1A1, Schematic Diagram


10 MHz
1 MHz
+5.2 V DC
+25.2 V DC
LOW POWER
CONTROL GND
+25.2 V DC
CW KEY
XMT AUDIO
RCV ONLY
AM
+13 V DC
+25.2 V DC (SW)
GND
17
18
35
31
32
33
34
44
24
27
28
29
30
19
20
21
23
41
36
49
10 MHz
1 MHz
+5.2 V DC
+25.2 V DC
LOW POWER
CONTROL GND
+25.2 V DC
CW KEY
XMT AUDIO
RCV ONLY
AM
+13 V DC
+25.2 V DC (SW)
RCVR/EXCTR
RF IN/OUT
POWER SUPPLY
A1A4P1 FUNCTIONS
J4
+5.2 V DC
GND
+13 V DC
+25.2 V DC (SW)
GND
C23A
C23B
C22B
C22A
BROADBAND AMPL
A1A3P1 FUNCTIONS
J3
RCVR/EXTR
RF IN/OUT
GND
+5.2 V DC
SPARE
+25.2 V DC (SW)
-ALC
KEY LINE
XMT/RCV RF
C3A
C4A
C3B
C4B
Q1
2N2222A
R1
1 k
R2
12 k
R3
12 k
C1
6.8 uF
C2
6.8 uF
MIXER
A1A2P1 FUNCTIONS
J2
XMT/RCV RF
GND
IF IN/OUT
XMT
RCV
AGC/ALC RTN
AGC/ALC DRIVE
SPARE
C5B
C5A
C6A
C6B
P/O


CONTROL
A2P1 FUNCTIONS
J1
10 kHz
1 kHz
USB/LSB
100 Hz
100 kHz
10 MHz
1 MHz
+5.2 V DC
+25.2 V DC
LOW POWER
CONTROL GND
+25.2 V DC
GND
10 MHz
1 kHz
USB/LSB (1=USB)
100 Hz
+13 V DC
+5.2 V DC
1 OR 2 kHz
5 MHz
VARIABLE DIVIDER
A1A6A2A1P1 FUNCTIONS
+5.2 V DC
100 kHz
10 MHz
1 MHz
XMT INHIBIT
GROUND
VARIABLE DIVIDER
A1A6A2A2P1 FUNCTIONS
J7
P/O
CONNECTOR
P1 CABLE
ASSEMBLY
P/O
P1
AMPL COUPLER
A3J1 FUNCTIONS
GND
10 kHz
1 kHz
USB/LSB (1=USB)
100 Hz
100 kHz
10 MHz
1 MHz
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+25.2 V DC
LOW POWER
CONTROL GND
+25.2 V DC

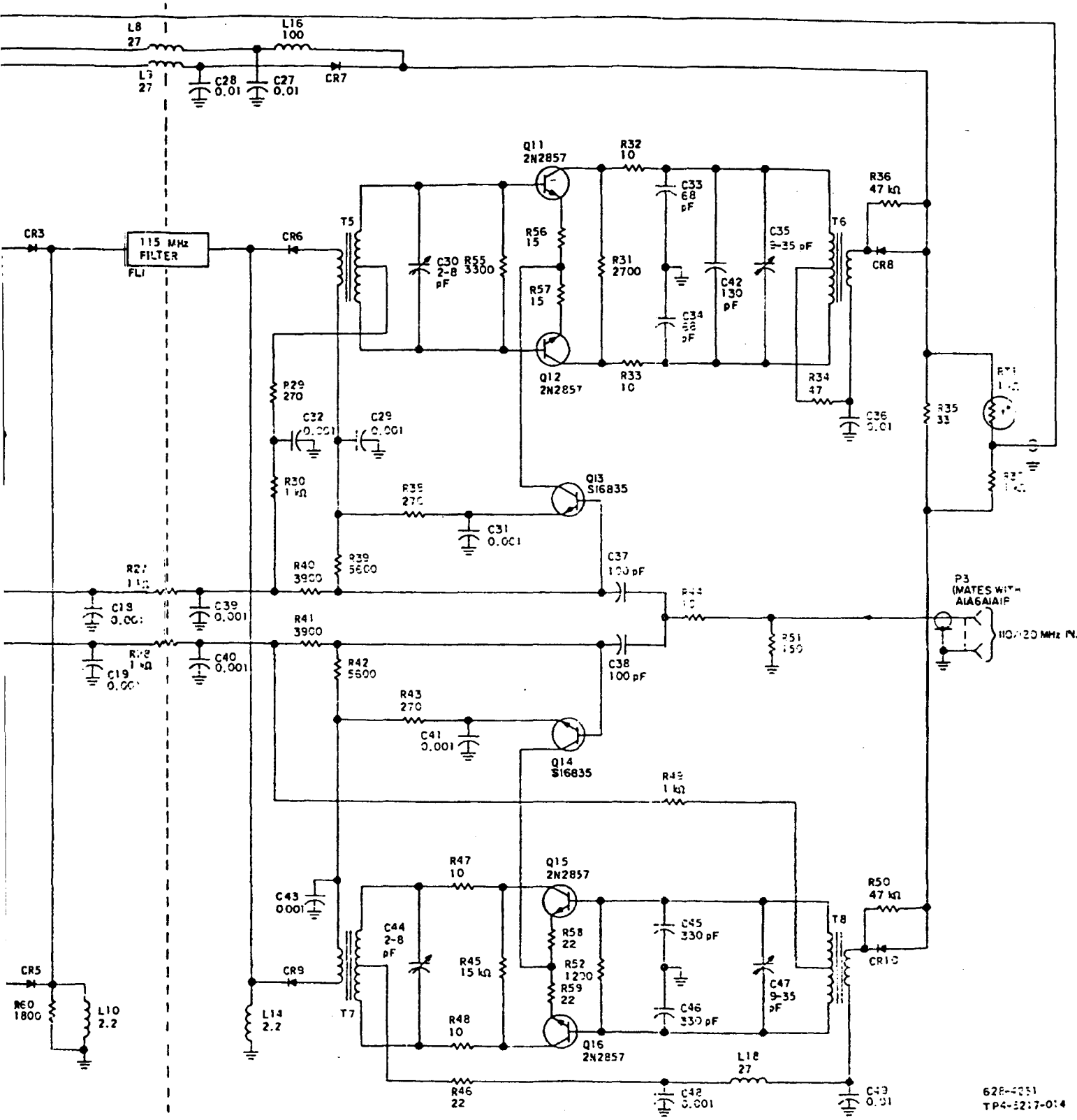
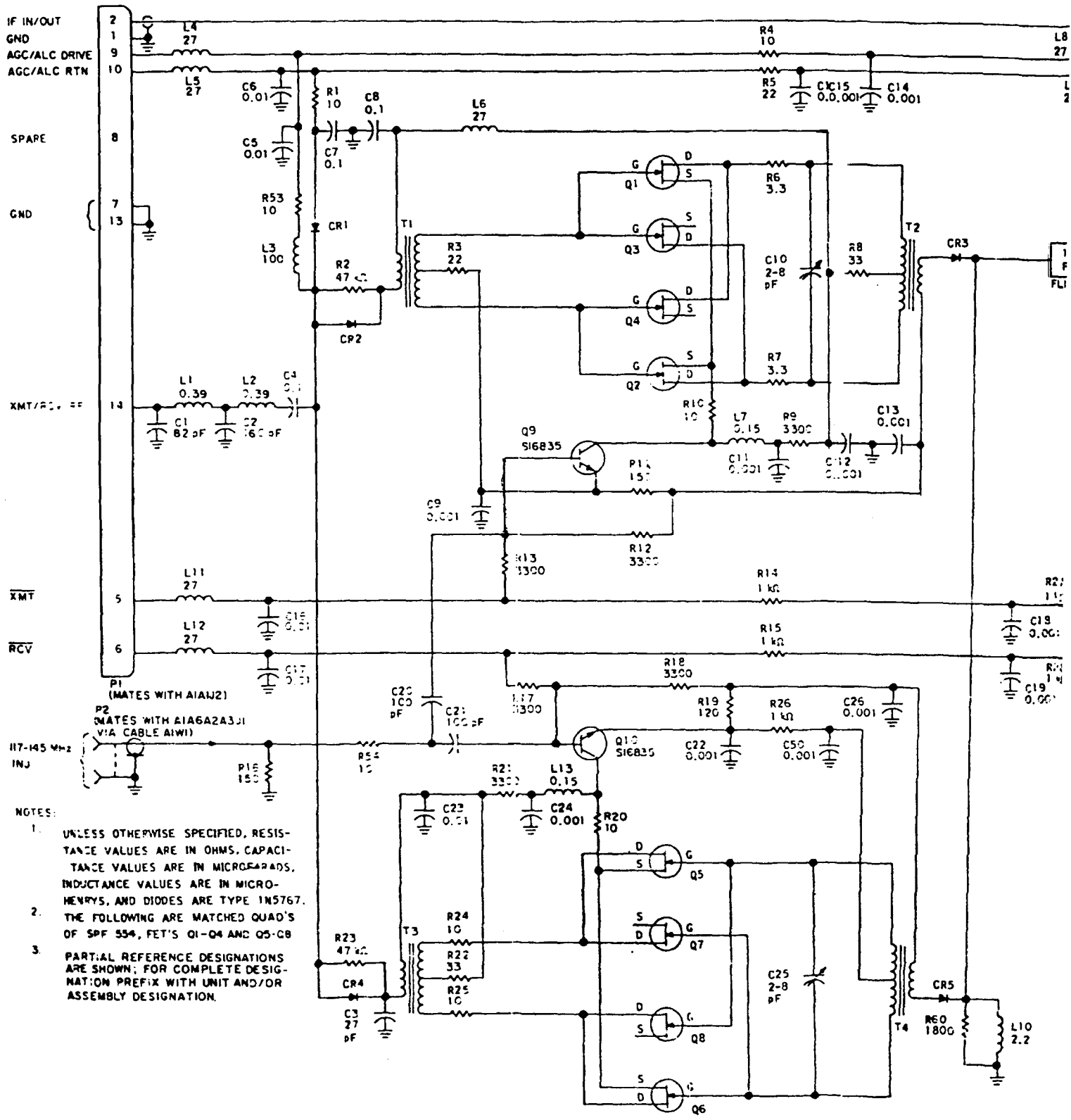
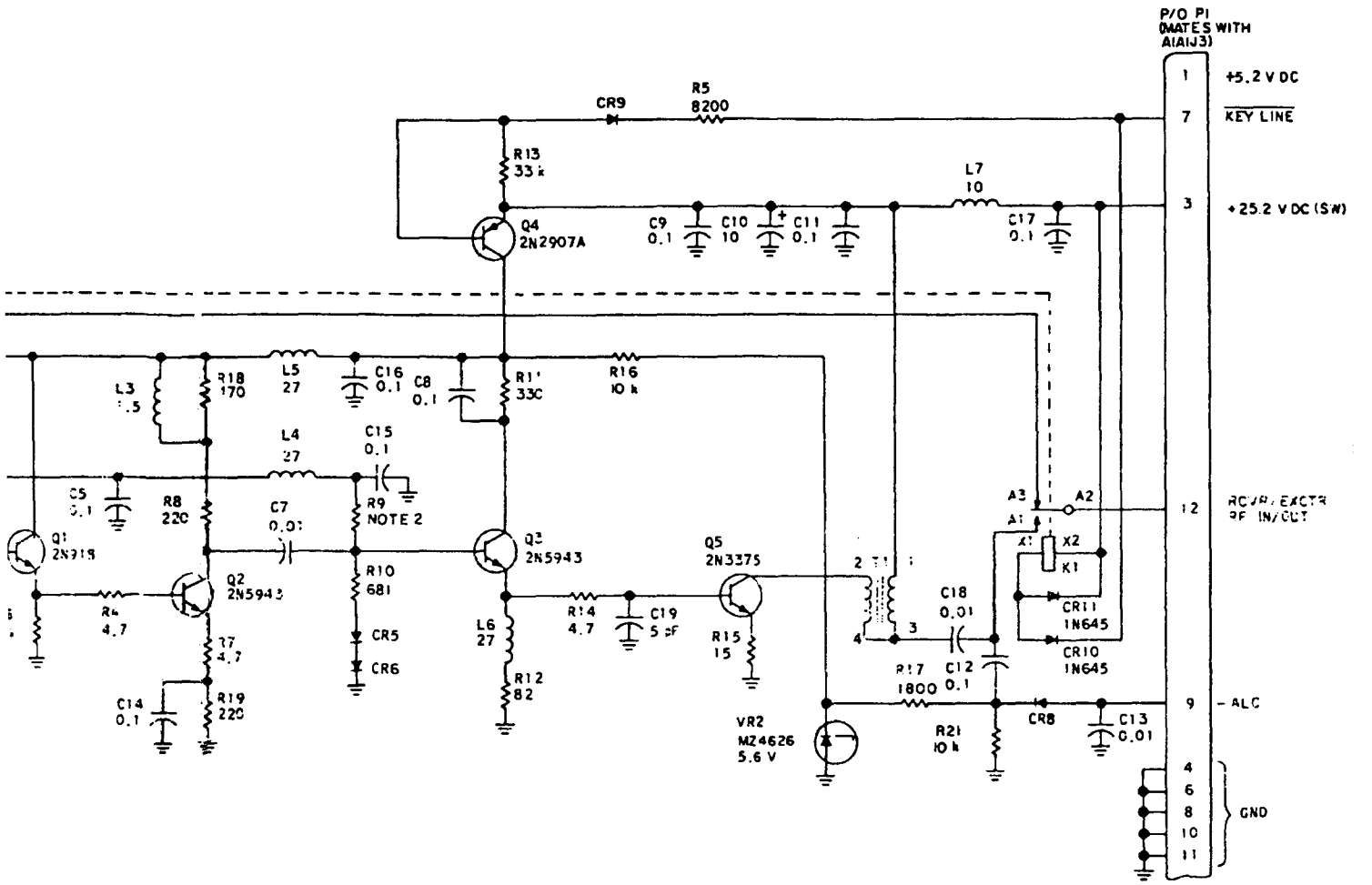


Figure 4-2. Mixer A1A2, Schematic Diagram



NOTES:

1. UNLESS OTHERWISE SPECIFIED, RESISTANCE VALUES ARE IN OHMS, CAPACITANCE VALUES ARE IN MICROFARADS, INDUCTANCE VALUES ARE IN MICROHENRYS, AND DIODES ARE TYPE 1N5767.
2. THE FOLLOWING ARE MATCHED QUAD'S OF SPF 554, FET'S Q1-Q4 AND Q5-Q8
3. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION PREFIX WITH UNIT AND/OR ASSEMBLY DESIGNATION.



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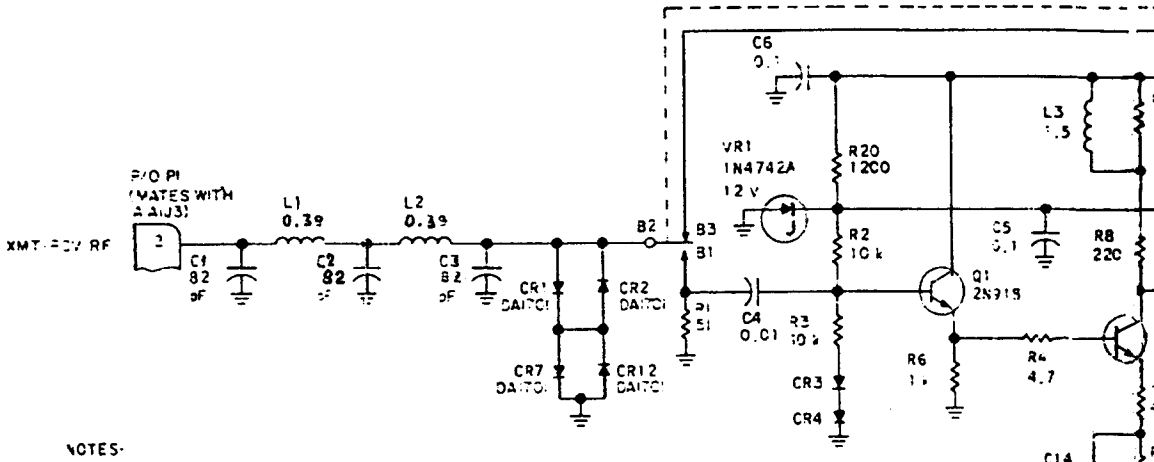
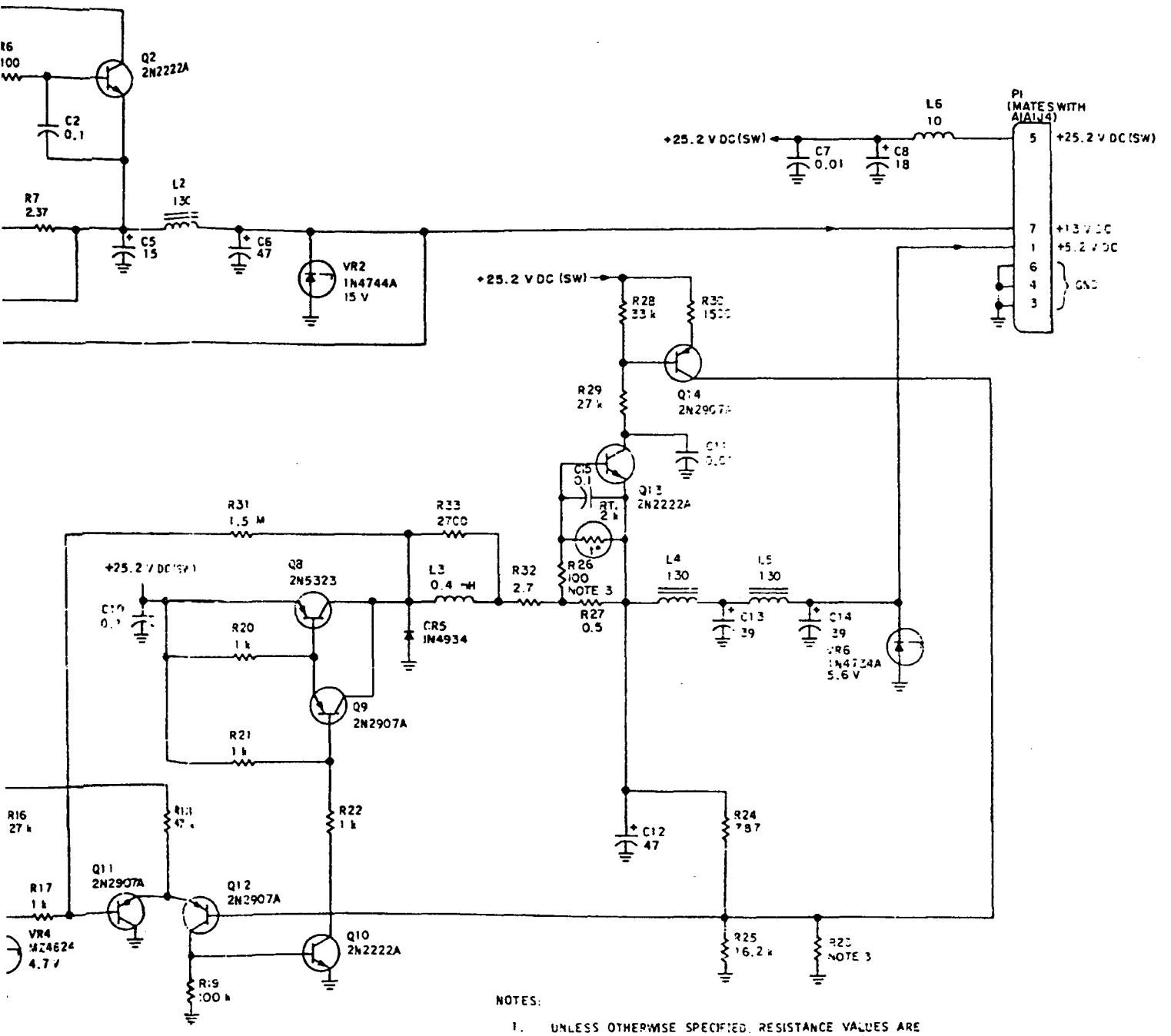
TP4-4661-014

Figure 4-3. Broadband Amplifier A1A3, Schematic Diagram



NOTES:

1. UNLESS OTHERWISE SPECIFIED, RESISTANCE VALUES ARE IN OHMS, CAPACITANCE VALUES ARE IN MICROFARADS, INDUCTANCE VALUES ARE IN MICROHENRYS AND DIODES ARE TYPE 1N4454.
2. FINAL VALUE OF R9 SELECTED IN TEST, NOMINAL VALUE 3320.

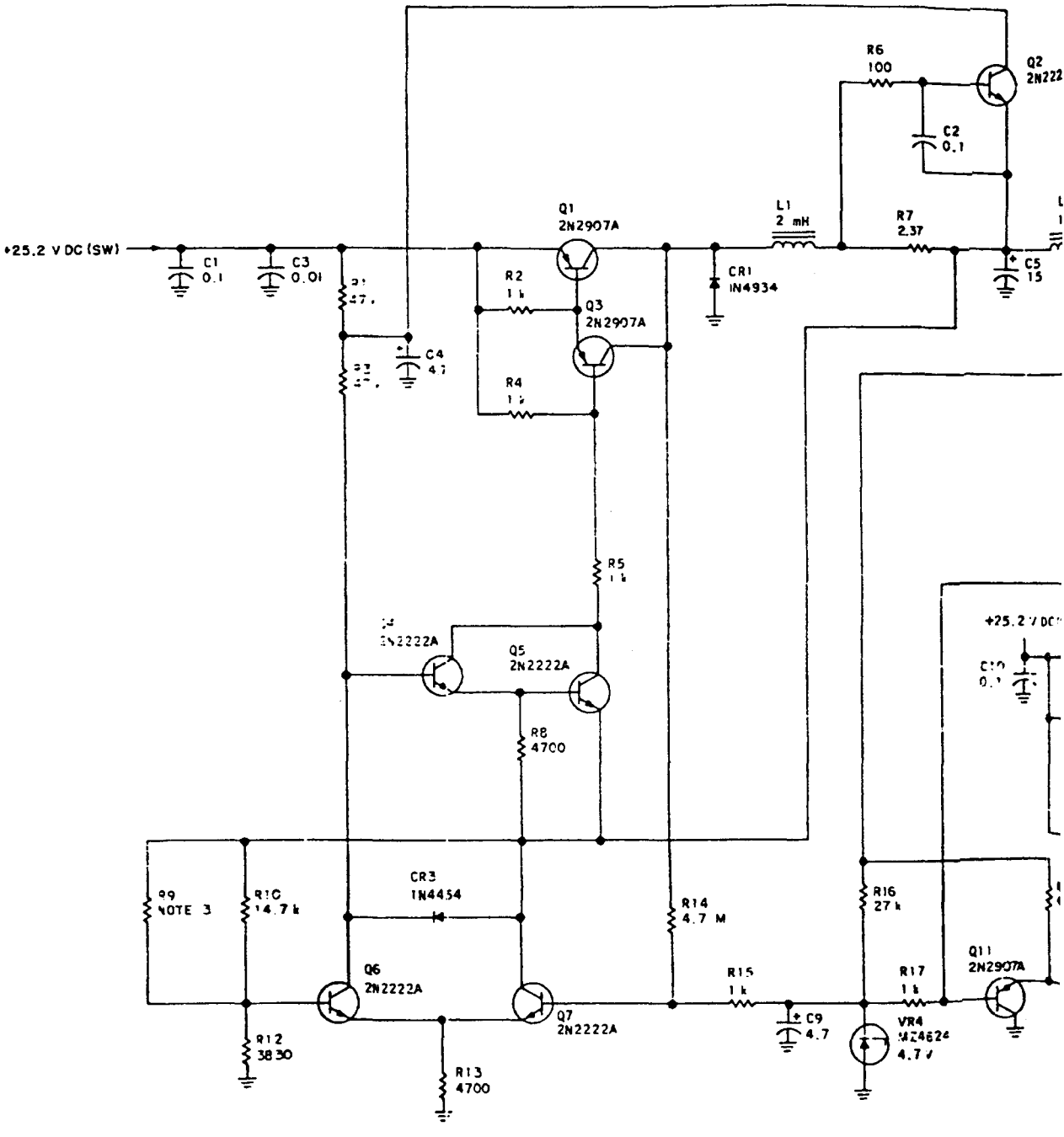


NOTES:

1. UNLESS OTHERWISE SPECIFIED, RESISTANCE VALUES ARE IN OHMS, CAPACITANCE VALUES ARE IN MICROFARADS, AND INDUCTANCE VALUES ARE IN MICROHENRYS.
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION, PREFIX UNIT AND/OR ASSEMBLY DESIGNATION.
3. VALUES ARE SELECTED IN TEST.

6294-4750
TP4 4554-014

Figure 4-4. Power Supply A1A4, Schematic Diagram


+25.2 V DC (SW)
C1
0.1
C3
0.01
Q1
2N2907A
L1
2 mH
R6
100
Q2
2N222
C2
0.1
R7
2.37
C5
15
CR1
IN4934
R2
1 k
Q3
2N2907A
C4
4.7
R4
1 k
R5
1 k
Q5
2N2222A
R8
4700
+25.2 V DC
R9
NOTE 3
R10
14.7 k
CR3
IN4454
R14
4.7 M
R16
27 k
Q11
2N2907A
Q6
2N2222A
Q7
2N2222A
R15
1 k
R17
1 k
C9
4.7
VR4
MZ4624
4.7 V
R12
3830
R13
4700

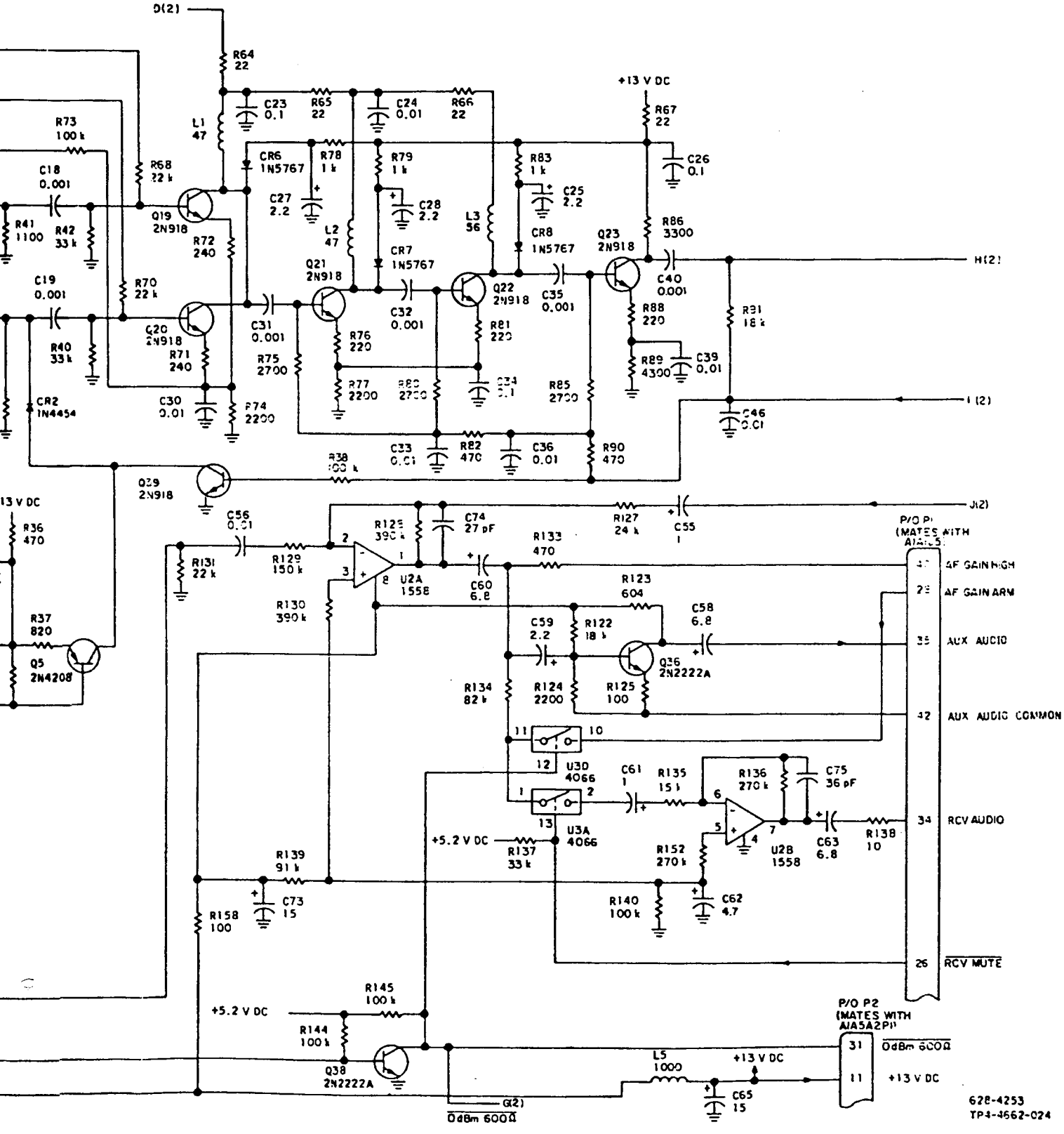
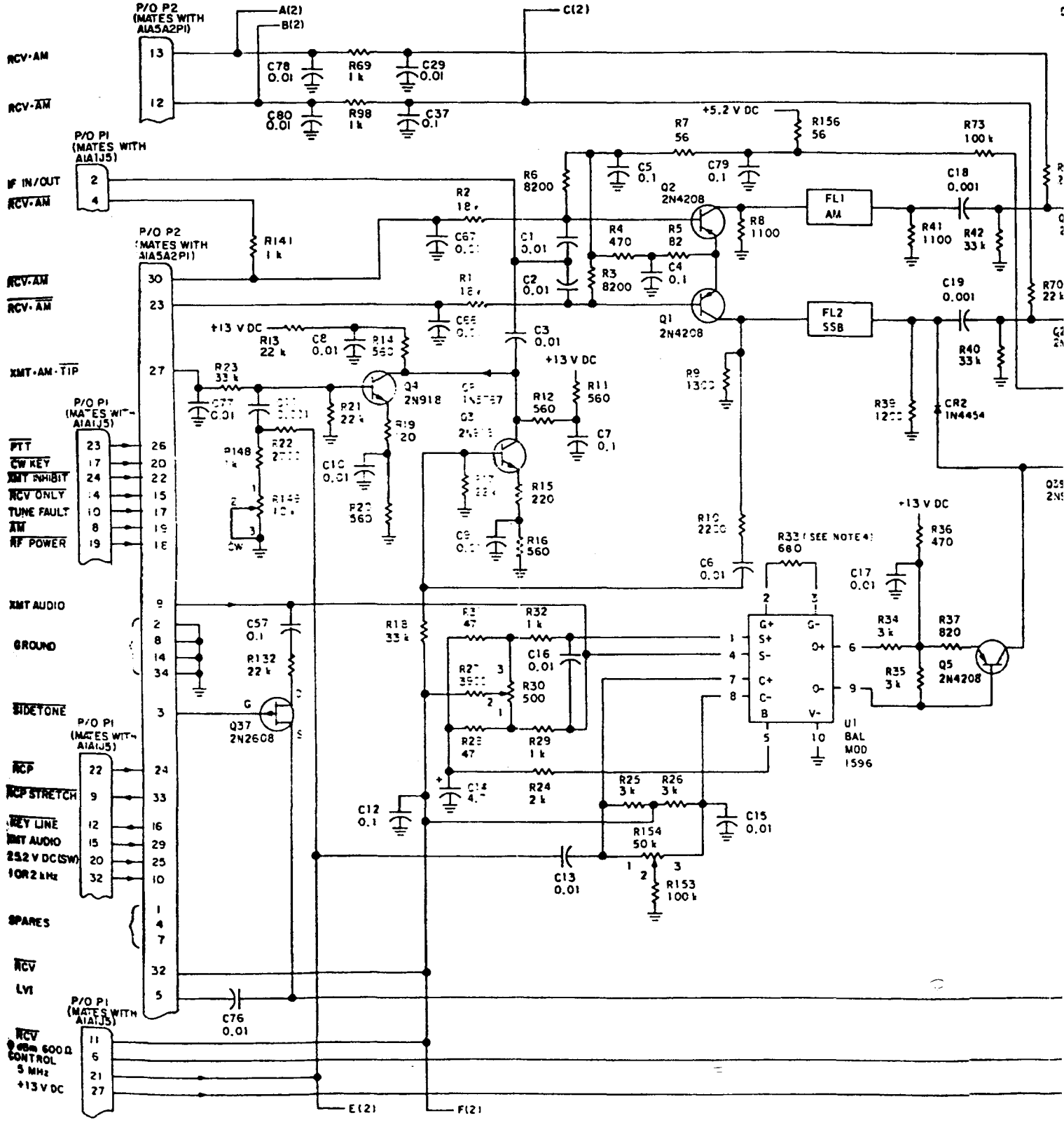
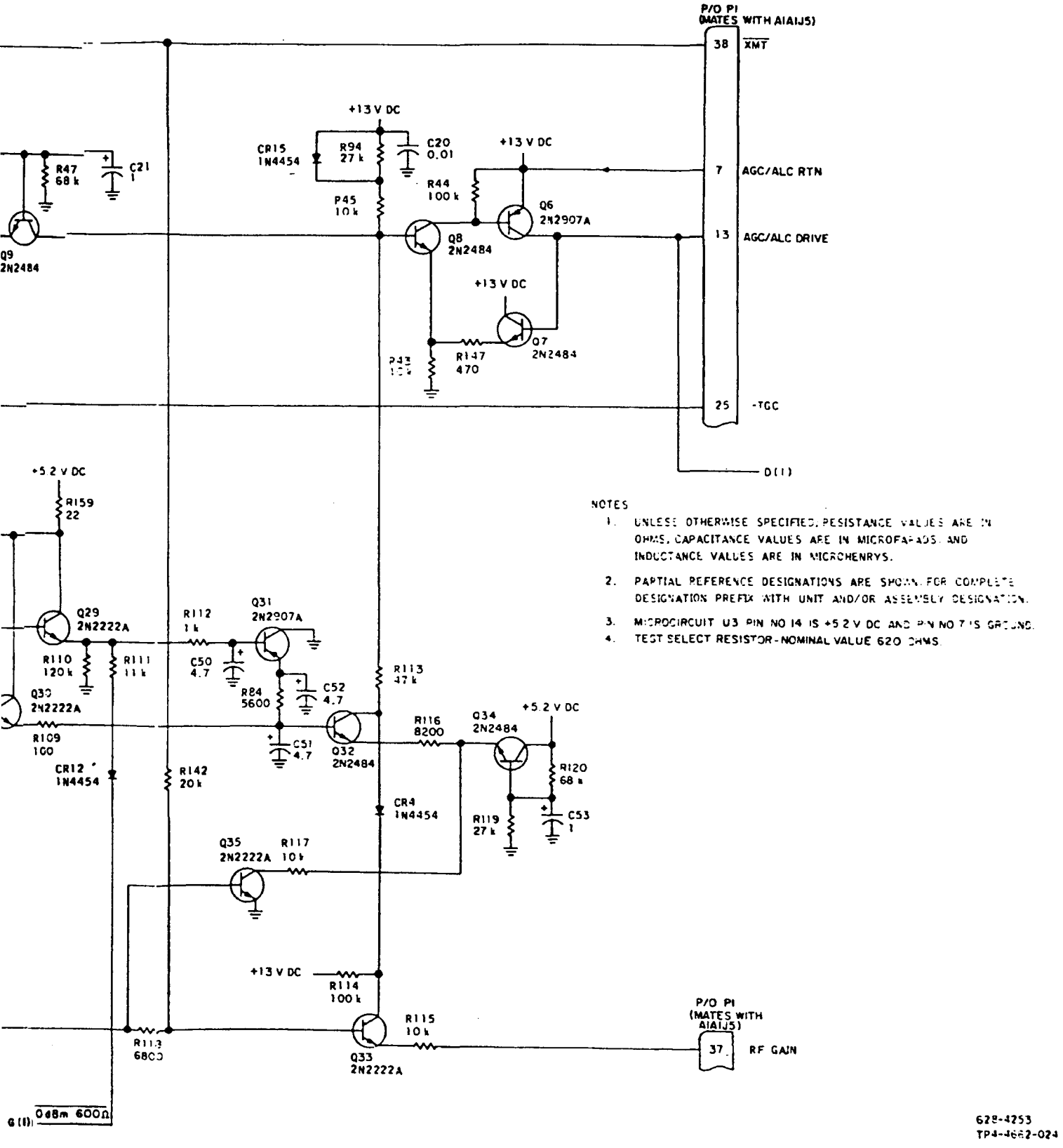


Figure 4-5. If/Af A1A5A1, Schematic Diagram (Sheet 1 of 2)


P/O P2 (MATES WITH A1A5A2P1)
A(2)
B(2)
C(2)
RCV-AM
RCV-AM
C78 0.01
R69 1 k
C29 0.01
C80 0.01
R98 1 k
C37 0.1
P/O P1 (MATES WITH A1A1J5)
IF IN/OUT
RCV-AM
R141 1 k
P/O P2 (MATES WITH A1A5A2P1)
RCV-AM
RCV-AM
XMT-AM-TIP
+13 V DC
R13 22 k
C8 0.01
R14 560
R23 33 k
C77 0.01
P/O P1 (MATES WITH A1A1J5)
PTT
CW KEY
XMT INHIBIT
RCV ONLY
TUNE FAULT
AM
RF POWER
R22
R19 20
C10 0.01
R20 560
Q4 2N918
R21 22 k
R15 220
R16 560
R12 560
R11 560
C7 0.1
+13 V DC
C3 0.01
R2 18
R1 18
C1 0.01
C2 0.01
R6 8200
R3 8200
R4 470
R5 82
C4 0.1
Q2 2N4208
Q1 2N4208
+5.2 V DC
R7 56
R156 56
C5 0.1
C79 0.1
R8 1100
FL1 AM
FL2 SSB
R73 100 k
C18 0.001
R41 1100
R42 33 k
C19 0.001
R40 33 k
R70 22 k
R9 1300
R39 1200
CR2 1N4454
R10 2200
C6 0.01
R33 (SEE NOTE 4) 680
+13 V DC
R36 470
C17 0.01
R34 3 k
R37 820
R35 3 k
Q5 2N4208
U1 BAL MOD 1596
G+
S+
S-
C+
C-
B
G-
O+
O-
V-
XMT AUDIO
GROUND
SIDETONE
C57 0.1
R132 22 k
Q37 2N2608
R18 33 k
R32 1 k
C16 0.01
R30 500
R29 1 k
R24 2 k
C14 4.7
C12 0.1
R25 3 k
R26 3 k
C15 0.01
R154 50 k
R153 100 k
C13 0.01
P/O P1 (MATES WITH A1A1J5)
RCP
RCP STRETCH
KEY LINE
XMT AUDIO
25.2 V DC(SW)
10 OR 2 kHz
SPARES
RCV
LVI
C76 0.01
P/O P1 (MATES WITH A1A1J5)
RCV
0 dBm 600 Ω CONTROL
5 MHz
+13 V DC
E(2)
F(2)



NOTES

1. UNLESS OTHERWISE SPECIFIED, RESISTANCE VALUES ARE IN OHMS, CAPACITANCE VALUES ARE IN MICROFARADS, AND INDUCTANCE VALUES ARE IN MICROHENRYS.
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION PREFIX WITH UNIT AND/OR ASSEMBLY DESIGNATION.
3. MICROCIRCUIT U3 PIN NO 14 IS +5.2 V DC AND PIN NO 7 IS GROUND.
4. TEST SELECT RESISTOR - NOMINAL VALUE 620 OHMS.

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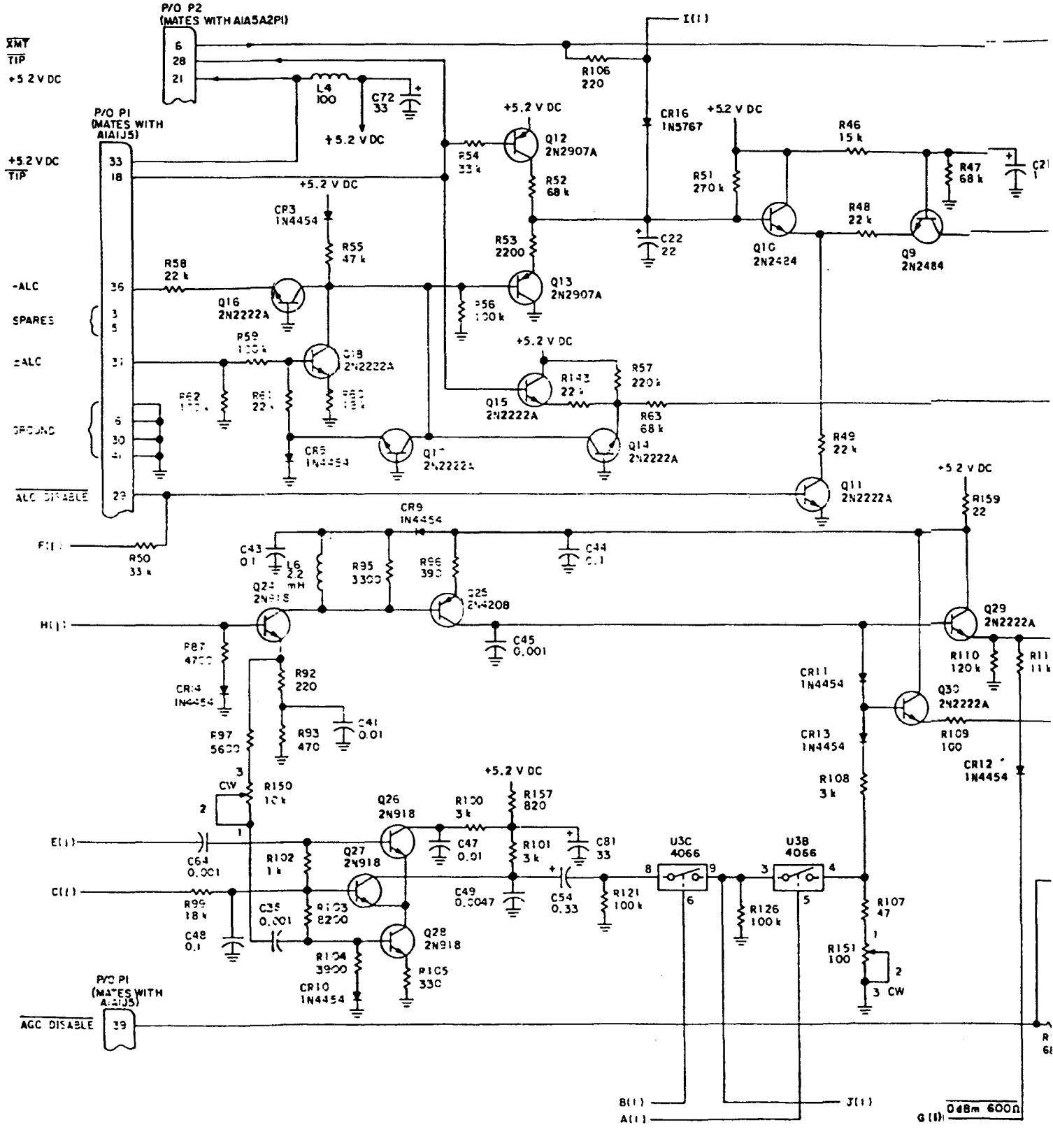
Figure 4-5. If/Af A1A5A1, Schematic Diagram (Sheet 2)


P/O P2
(MATES WITH A1A5A2P1)
XMT
TIP
+5.2 V DC
6
28
21
L4
100
C72
33
+5.2 V DC
I(1)
R106
220
P/O P1
(MATES WITH
A1A1J5)
+5.2 V DC
TIP
33
18
+5.2 V DC
Q12
2N2907A
R54
33 k
R52
68 k
CR16
1N5767
+5.2 V DC
R46
15 k
R51
270 k
R47
68 k
CR3
1N4454
R55
47 k
R53
2200
C22
22
Q10
2N2484
R48
22 k
Q9
2N2484
R58
22 k
-ALC
36
Q16
2N2222A
Q13
2N2907A
R56
100 k
SPARES
3
5
+5.2 V DC
R59
100 k
+ALC
31
Q18
2N2222A
R62
100 k
R61
22 k
R60
100 k
+5.2 V DC
R57
220 k
R143
22 k
Q15
2N2222A
R63
68 k
GROUND
6
30
41
CR5
1N4454
Q17
2N2222A
Q14
2N2222A
R49
22 k
ALC DISABLE
29
Q11
2N2222A
+5.2 V DC
R159
22
CR9
1N4454
R50
33 k
C43
0.1
L6
2.2 mH
R95
3300
R96
390
C44
0.1
Q24
2N918
Q25
2N4208
H(1)
C45
0.001
Q29
2N2222A
R87
4700
R110
120 k
CR11
1N4454
CR14
1N4454
R92
220
Q30
2N2222A
R97
5600
R93
470
C41
0.01
R109
100
CR13
1N4454
CR12
1N4454
R108
3 k
3
CW
R150
10 k
2
1
+5.2 V DC
Q26
2N918
R100
3 k
R157
820
E(1)
C64
0.001
R102
1 k
Q27
2N918
C47
0.01
R101
3 k
C81
33
U3C
4066
U3B
4066
C(1)
R99
18 k
C35
0.001
R103
8250
C49
0.0047
C54
0.33
R121
100 k
R126
100 k
R107
47
C48
0.1
Q28
2N918
R104
3900
R105
330
R151
100
1
2
3 CW
CR10
1N4454
P/O P1
(MATES WITH
A1A1J5)
AGC DISABLE
39
B(1)
A(1)
J(1)
0dBm 600Ω
G(1)

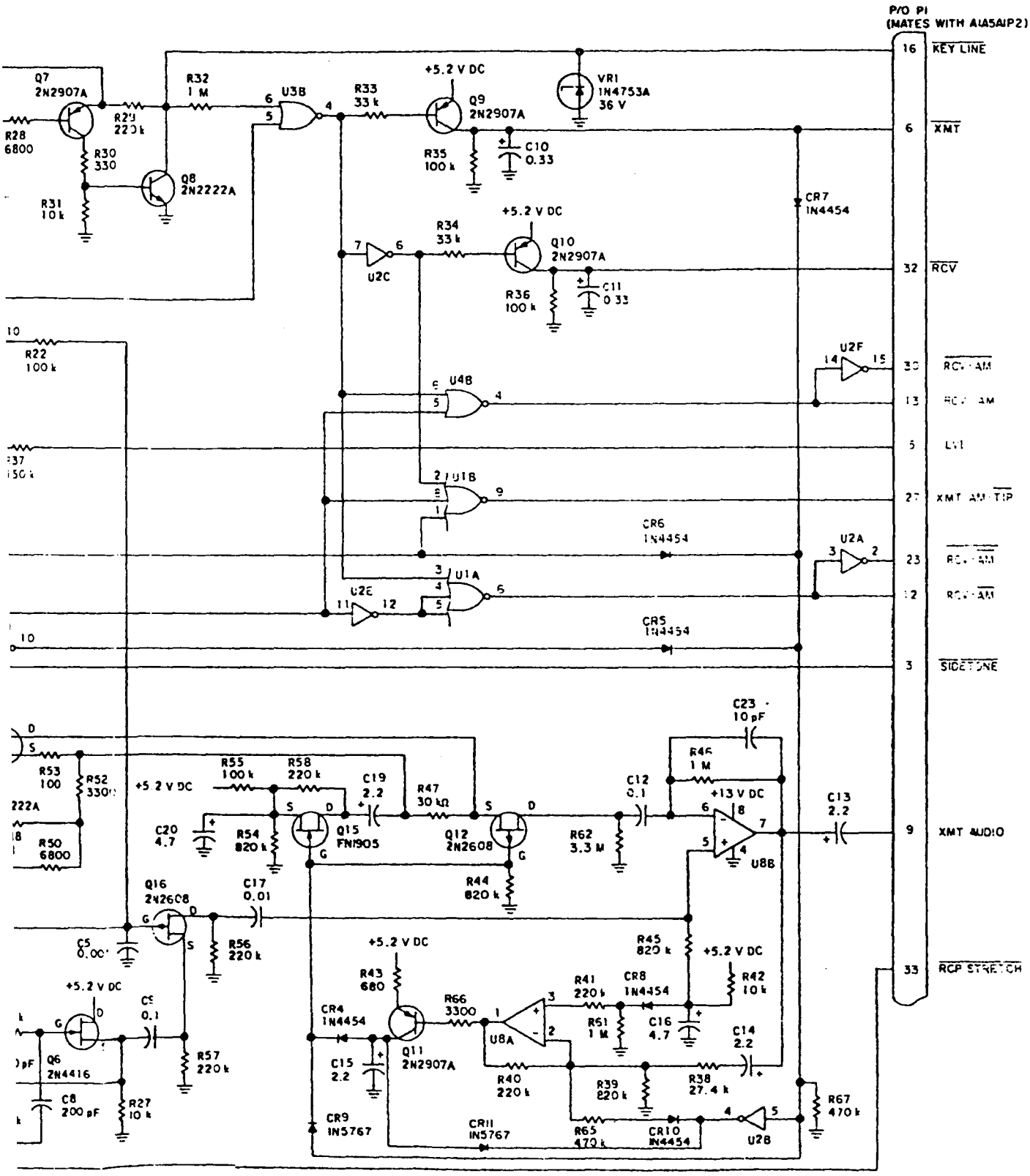
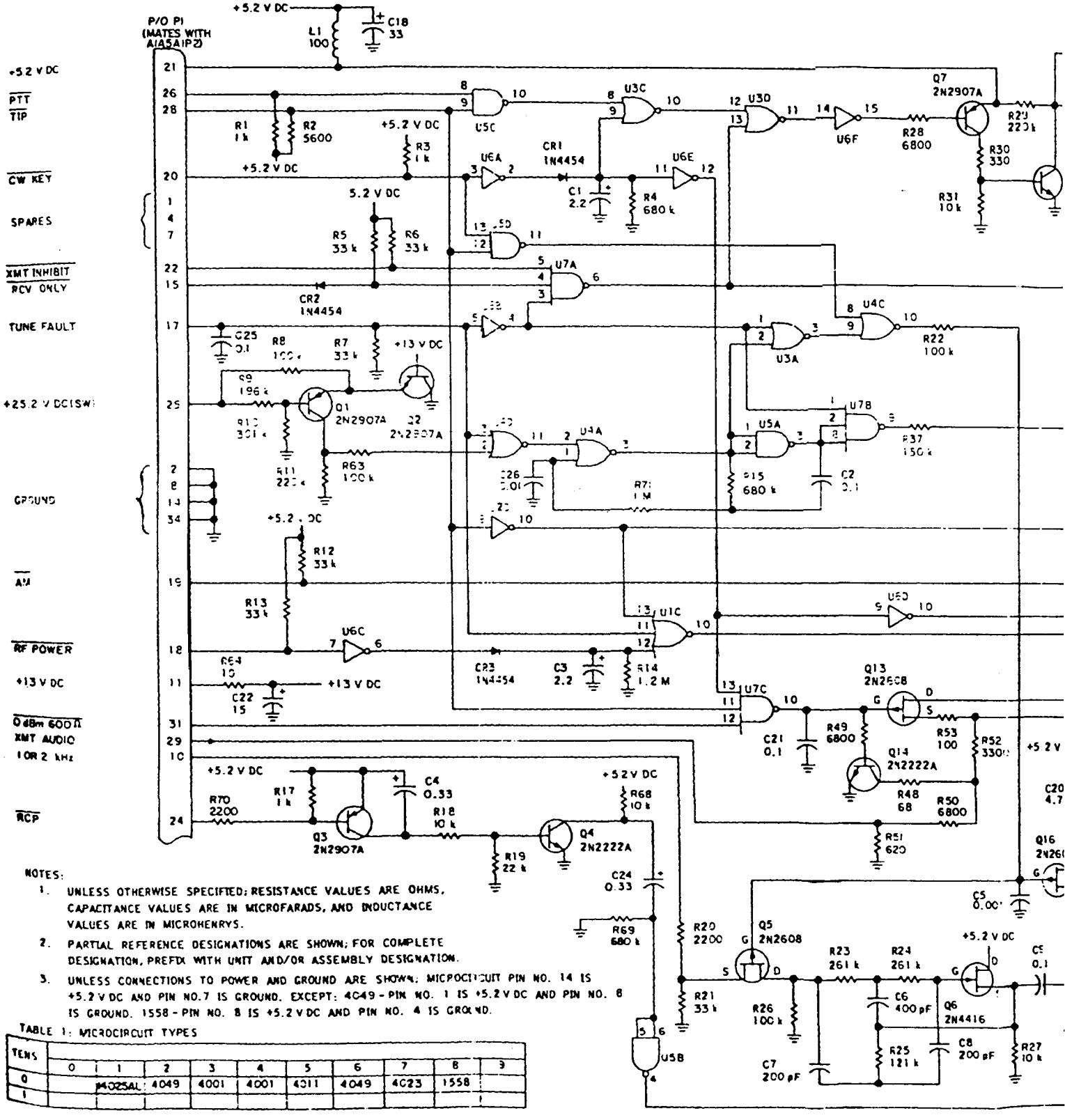


Figure 4-6. Logic/Tx A1A5A2, Schematic Diagram



NOTES:

1. UNLESS OTHERWISE SPECIFIED: RESISTANCE VALUES ARE OHMS, CAPACITANCE VALUES ARE IN MICROFARADS, AND INDUCTANCE VALUES ARE IN MICROHENRYS.
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION, PREFIX WITH UNIT AND/OR ASSEMBLY DESIGNATION.
3. UNLESS CONNECTIONS TO POWER AND GROUND ARE SHOWN, MICROCIRCUIT PIN NO. 14 IS +5.2 V DC AND PIN NO.7 IS GROUND. EXCEPT: 4049 - PIN NO. 1 IS +5.2 V DC AND PIN NO. 8 IS GROUND. 1558 - PIN NO. 8 IS +5.2 V DC AND PIN NO. 4 IS GROUND.

TABLE 1: MICROCIRCUIT TYPES

TENS	0	1	2	3	4	5	6	7	8	9
0		μ4025AL	4049	4001	4001	4011	4049	4023	1558	
1										

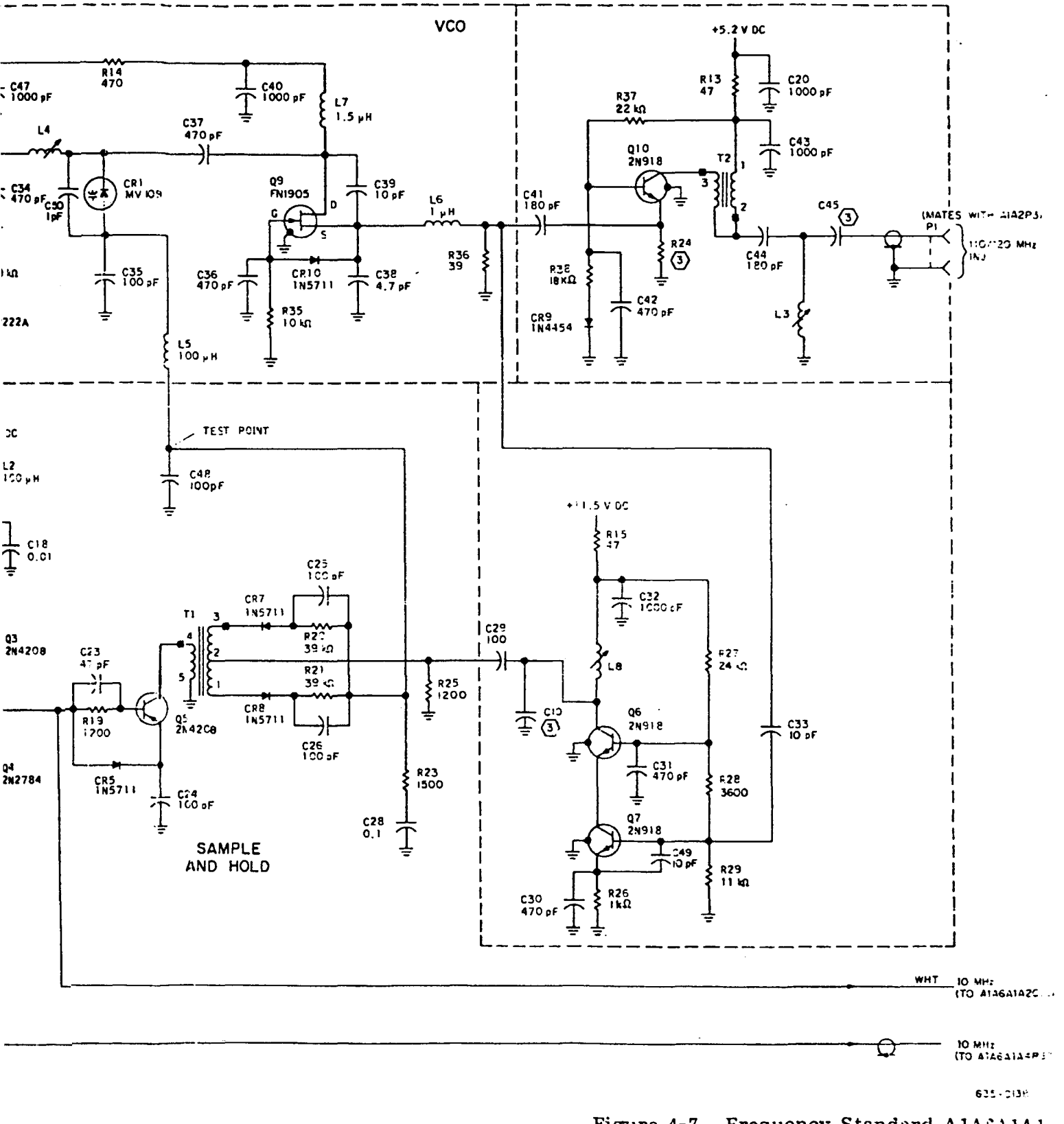
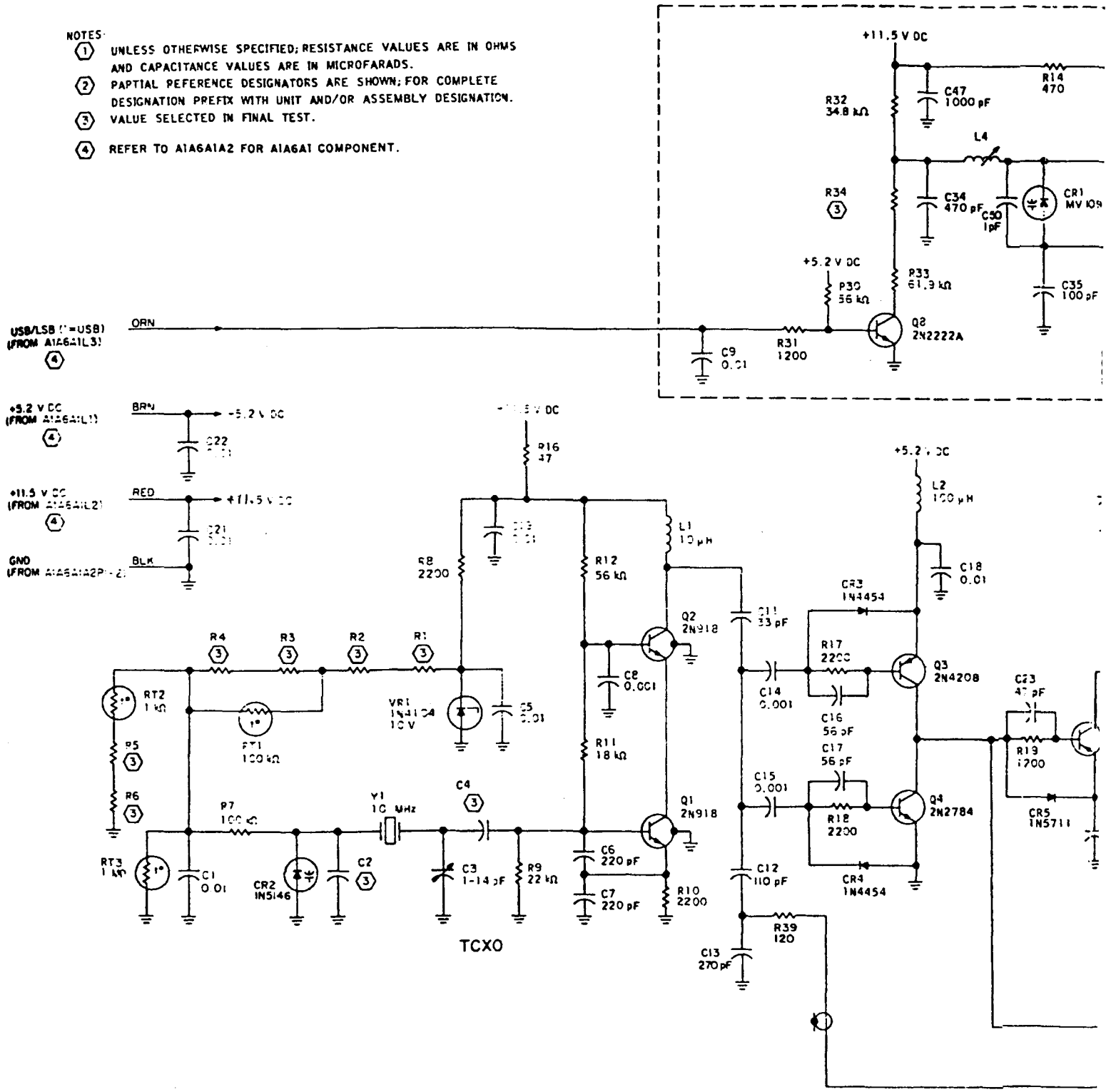


Figure 4-7. Frequency Standard A1A6A1A1, Schematic Diagram

NOTES:

1. UNLESS OTHERWISE SPECIFIED; RESISTANCE VALUES ARE IN OHMS AND CAPACITANCE VALUES ARE IN MICROFARADS.
2. PAPTIAL PEFERENCE DESIGNATORS ARE SHOWN; FOR COMPLETE DESIGNATION PREFIX WITH UNIT AND/OR ASSEMBLY DESIGNATION.
3. VALUE SELECTED IN FINAL TEST.
4. REFER TO A1A6A1A2 FOR A1A6A1 COMPONENT.



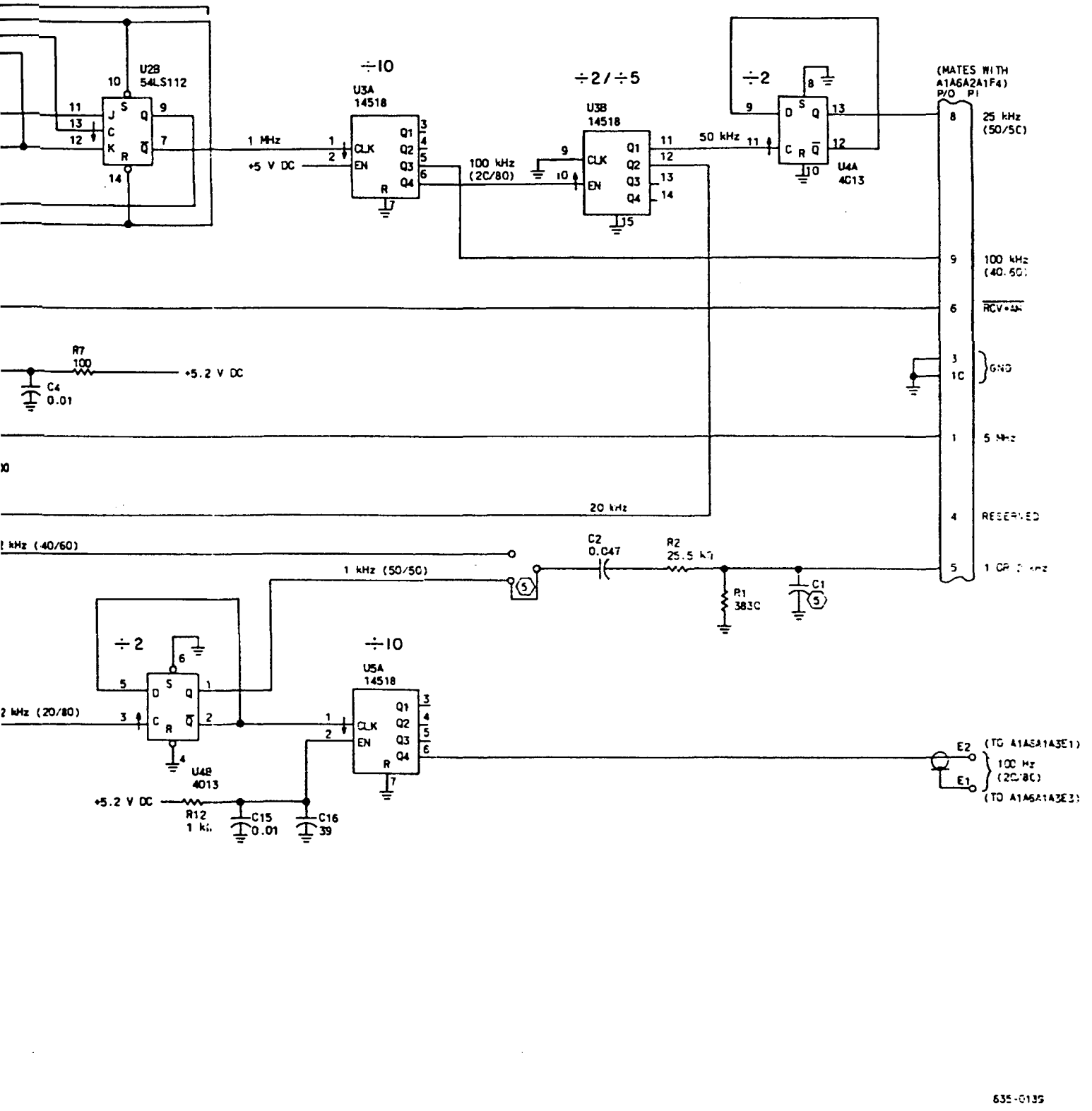
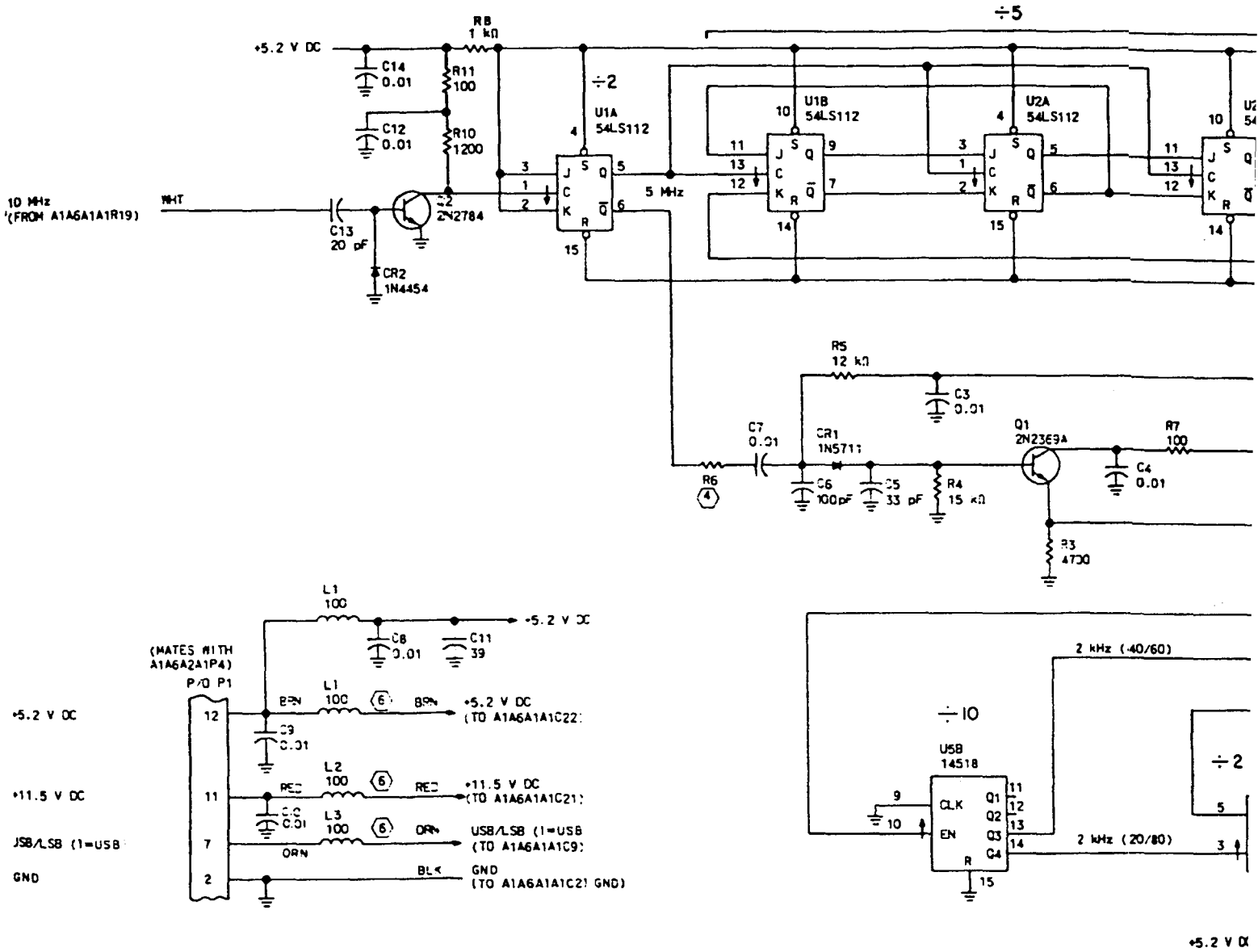


Figure 4-8. Fixed Frequency Divider A1A6A1A2 Schematic Diagram



NOTES:

(1) UNLESS OTHERWISE SPECIFIED, RESISTANCE VALUES ARE IN OHMS, CAPACITANCE VALUES ARE IN MICROFARADS AND INDUCTANCE VALUES ARE IN MICROHENRYS

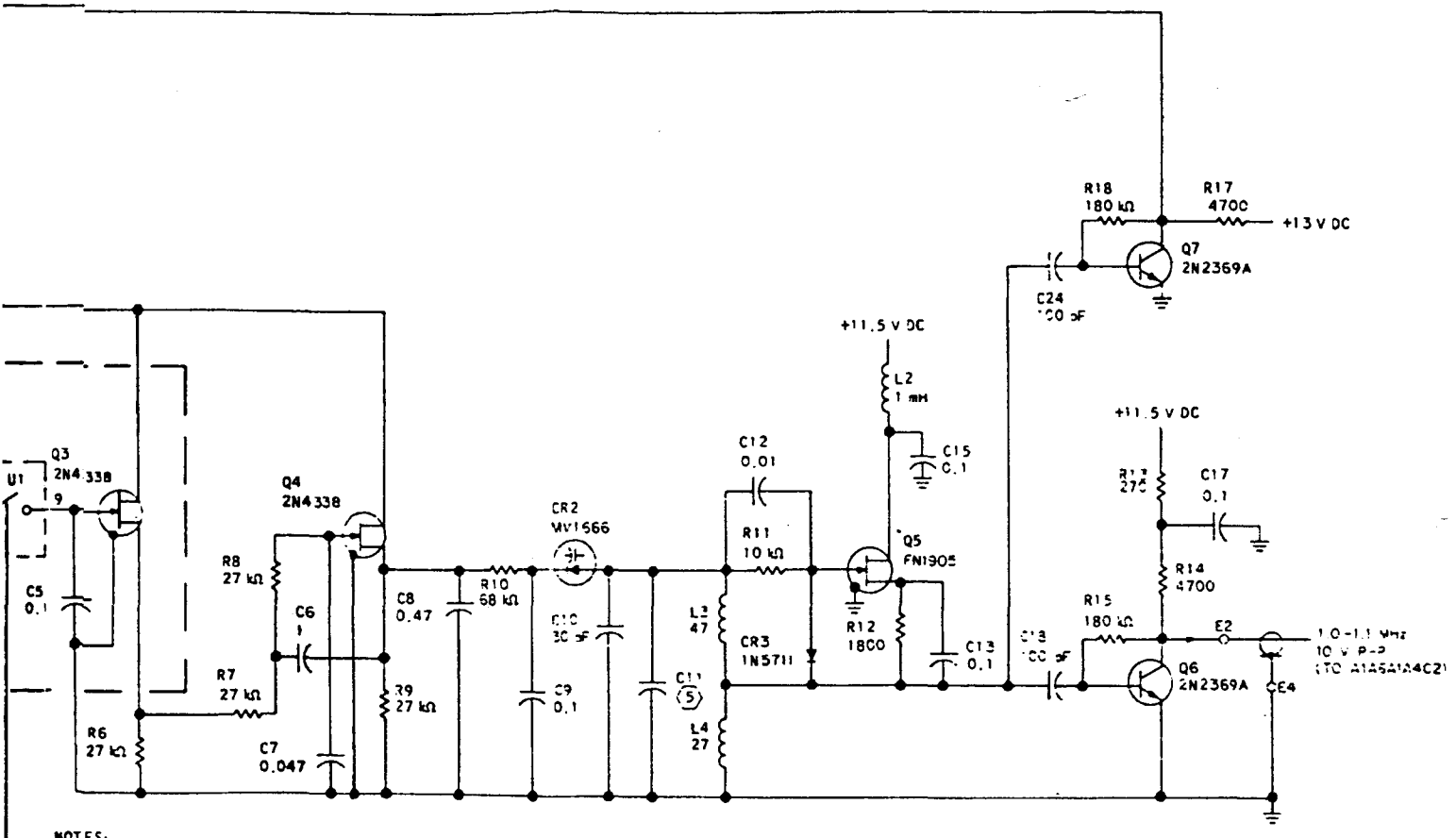
(2) PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION, PREFIX WITH UNIT AND/OR ASSEMBLY DESIGNATION.

(3) MICROCIRCUIT POWER AND GROUND INFORMATION:
U1,U2 -- PIN 14 IS +5.2 V DC PIN 7 IS GROUND
U3 -- PIN 16 IS +5 V DC PIN 8 IS GROUND
U4 -- PIN 14 CONNECTS TO +5.2 V DC THRU R12 PIN 7 IS GROUND
U5 -- PIN 16 CONNECTS TO +5.2 V DC THRU R12 PIN 8 IS GROUND

(4) FINAL VALUE IS SELECTED IN TEST.

(5) 1 OR 2 kHz STRAPPING OPTION.
-001: 1 kHz, C1 = 0.1 uF
-002: 2 kHz, C1 = 0.047 uF

(6) LOCATED ON A1A6A1.



NOTES:

(1) UNLESS OTHERWISE SPECIFIED ALL RESISTANCE VALUES ARE IN OHMS, ALL CAPACITANCE VALUES ARE IN MICROFARADS, AND ALL INDUCTANCE VALLES ARE IN MICROHENRYS.

(2) PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE DESIGNATION PREFIX WITH UNIT AND/OR ASSEMBLY DESIGNATION.

(3) UNLESS CONNECTION TO POWER AND GROUND ARE SHOWN PIN 14 IS +13 V AND PIN 7 IS GROUND EXCEPT

TYPE	POWER		GROUND
	PIN	VOLT	
4029	16	+13	8
4049	1	+13	8
4066			7

(4) MICROCIRCUIT TYPES

TENS	UNITS									
	0	1	2	3	4	5	6	7	8	9
0		4066	4002	4049	4013	4002	4029	4029	4029	4029

(5) VALUE SELECTED IN TEST.

(6) LOCATED ON A1A6A1.

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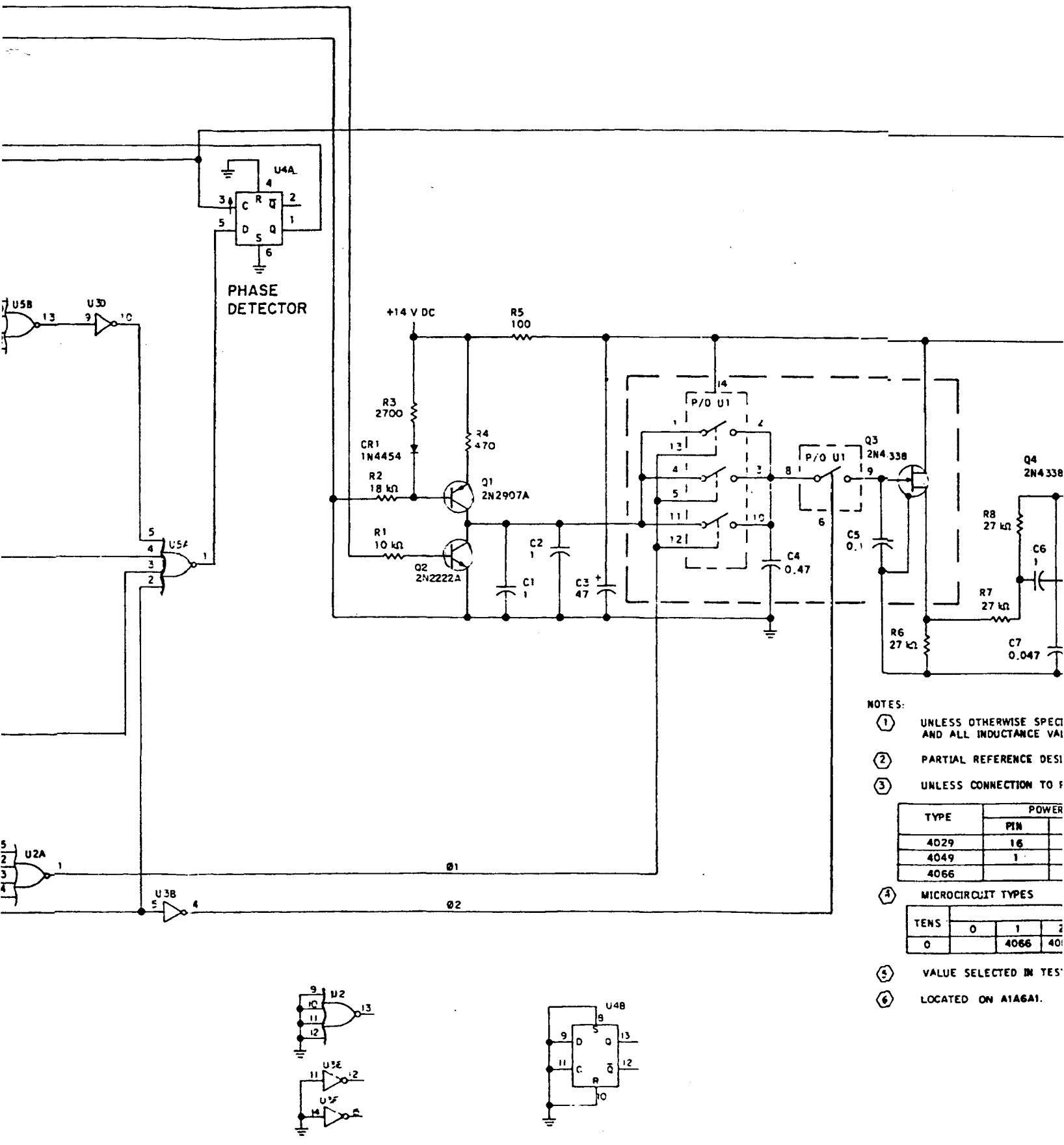
Figure 4-9. Lf Phase-Lock Loop A1A6A1A3 Schematic Diagram



NOTES:

(1) UNLESS OTHERWISE SPECI
AND ALL INDUCTANCE VA

(2) PARTIAL REFERENCE DESI

(3) UNLESS CONNECTION TO F

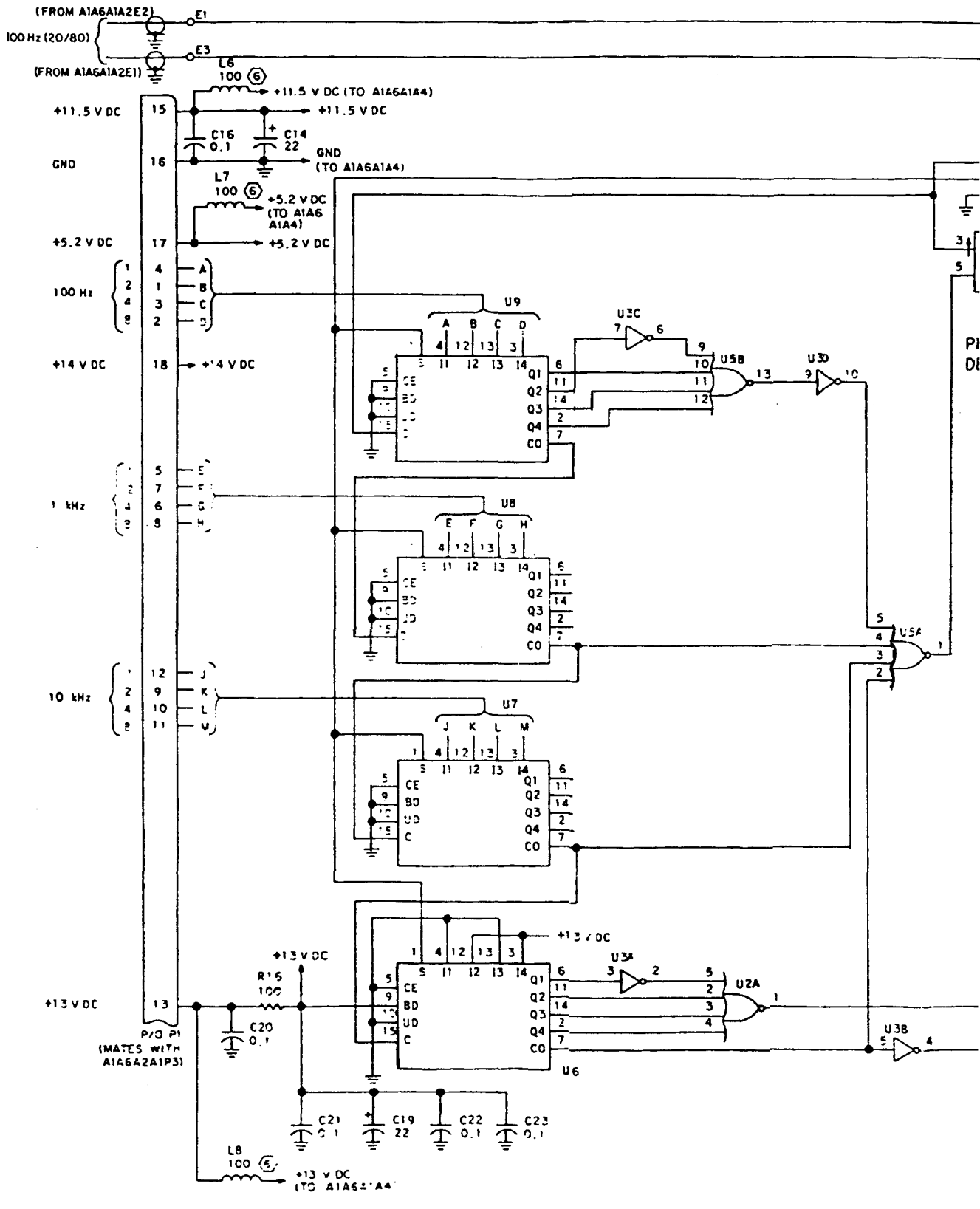
TYPE	POWER
	PIN
4029	16
4049	1
4066	

(4) MICROCIRCUIT TYPES

TENS			
	0	1	2
0		4066	40

(5) VALUE SELECTED IN TES

(6) LOCATED ON A1A6A1.


(FROM A1A6A1A2E2)
100 Hz (20/80)
(FROM A1A6A1A2E1)
E1
E3
L6
100
+11.5 V DC (TO A1A6A1A4)
+11.5 V DC
+11.5 V DC
C16
0.1
C14
22
GND
GND
(TO A1A6A1A4)
L7
100
+5.2 V DC
(TO A1A6
A1A4)
+5.2 V DC
+5.2 V DC
100 Hz
+14 V DC
+14 V DC
1 kHz
10 kHz
+13 V DC
+13 V DC
R15
100
C20
0.1
P/O P1
(MATES WITH
A1A6A2A1P3)
L8
100
+13 V DC
(TO A1A6A1A4)
U9
U8
U7
U6
U3C
U5B
U3D
U5A
U3A
U2A
U3B
C21
0.1
C19
22
C22
0.1
C23
0.1

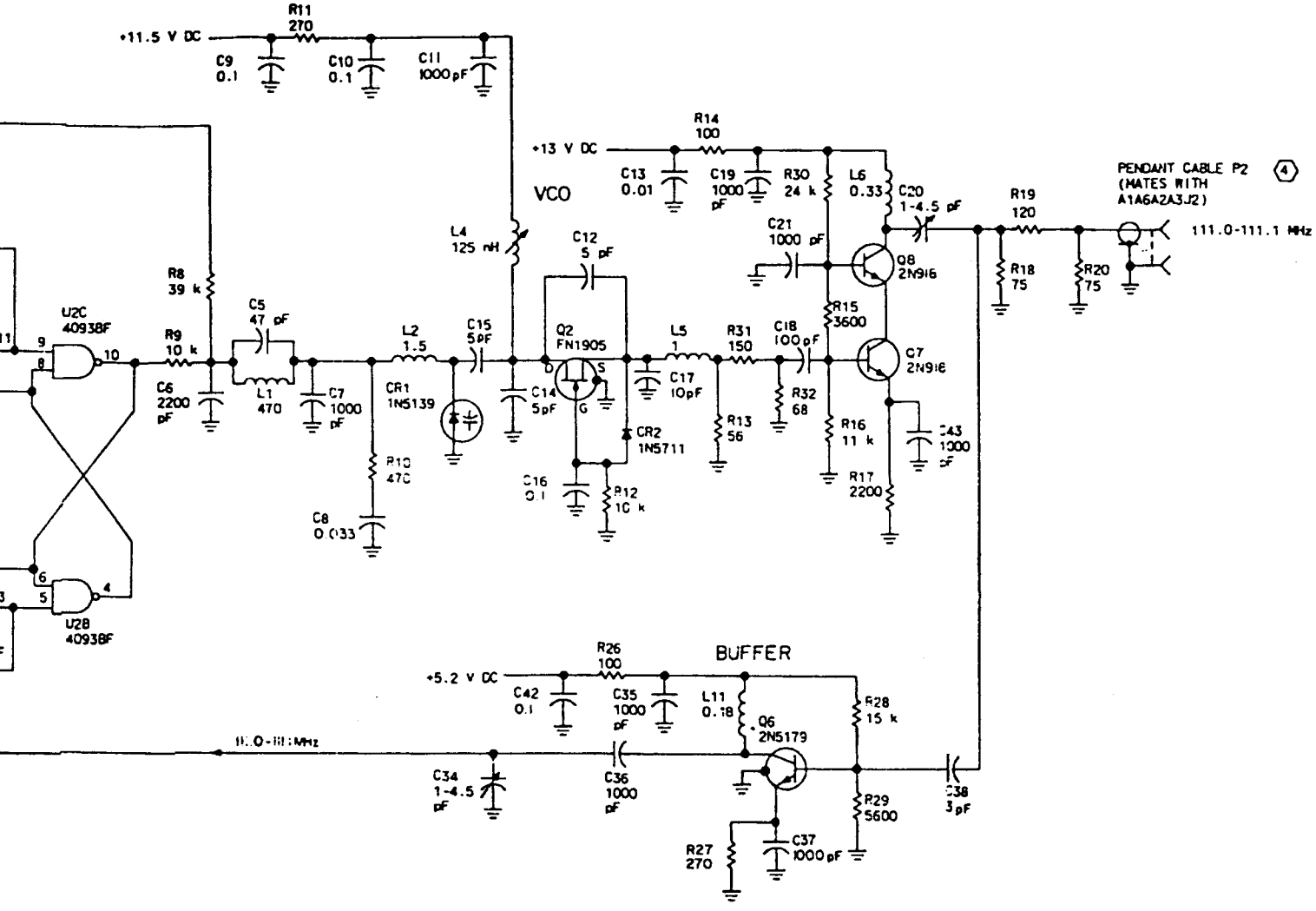


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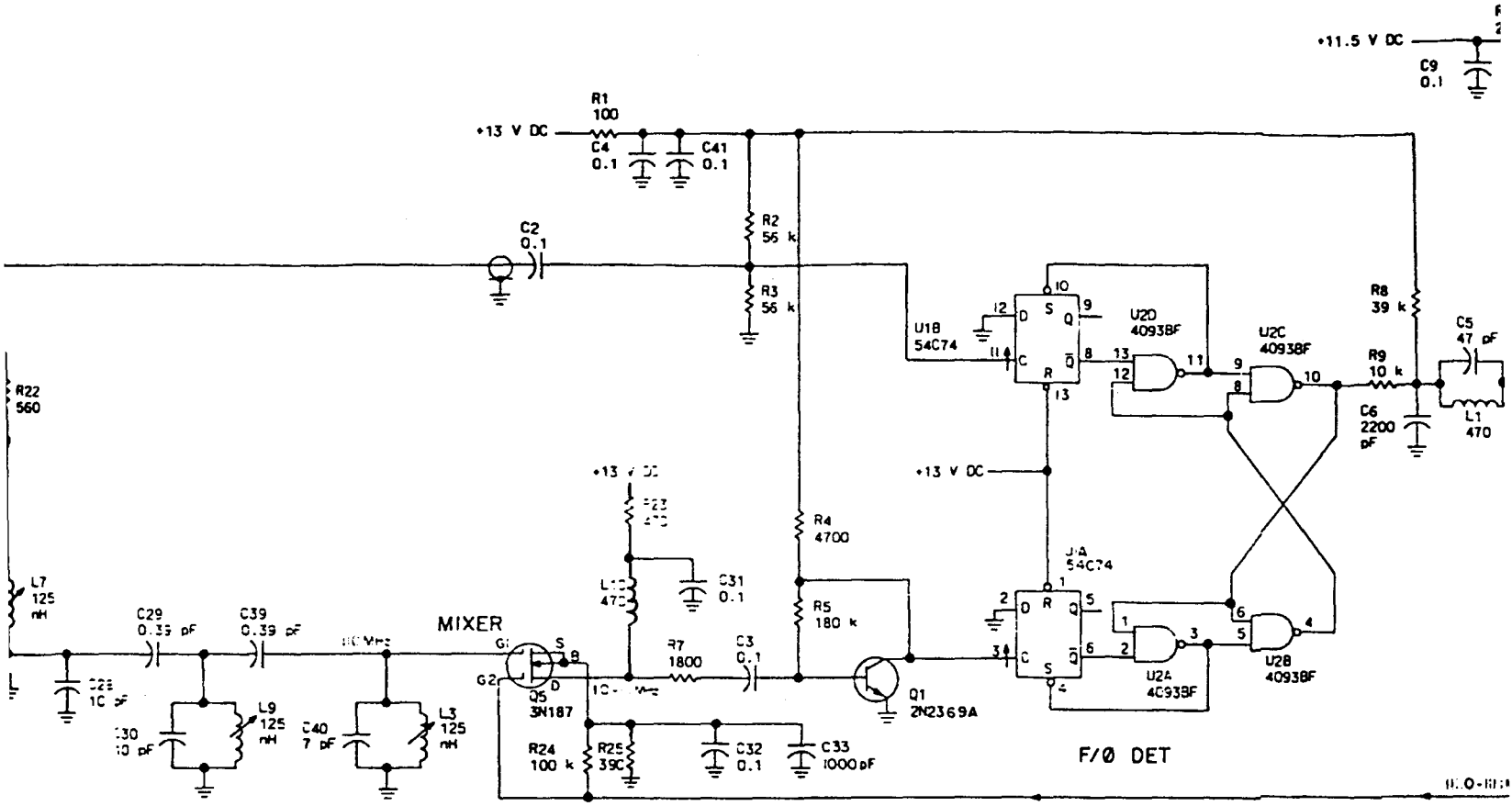
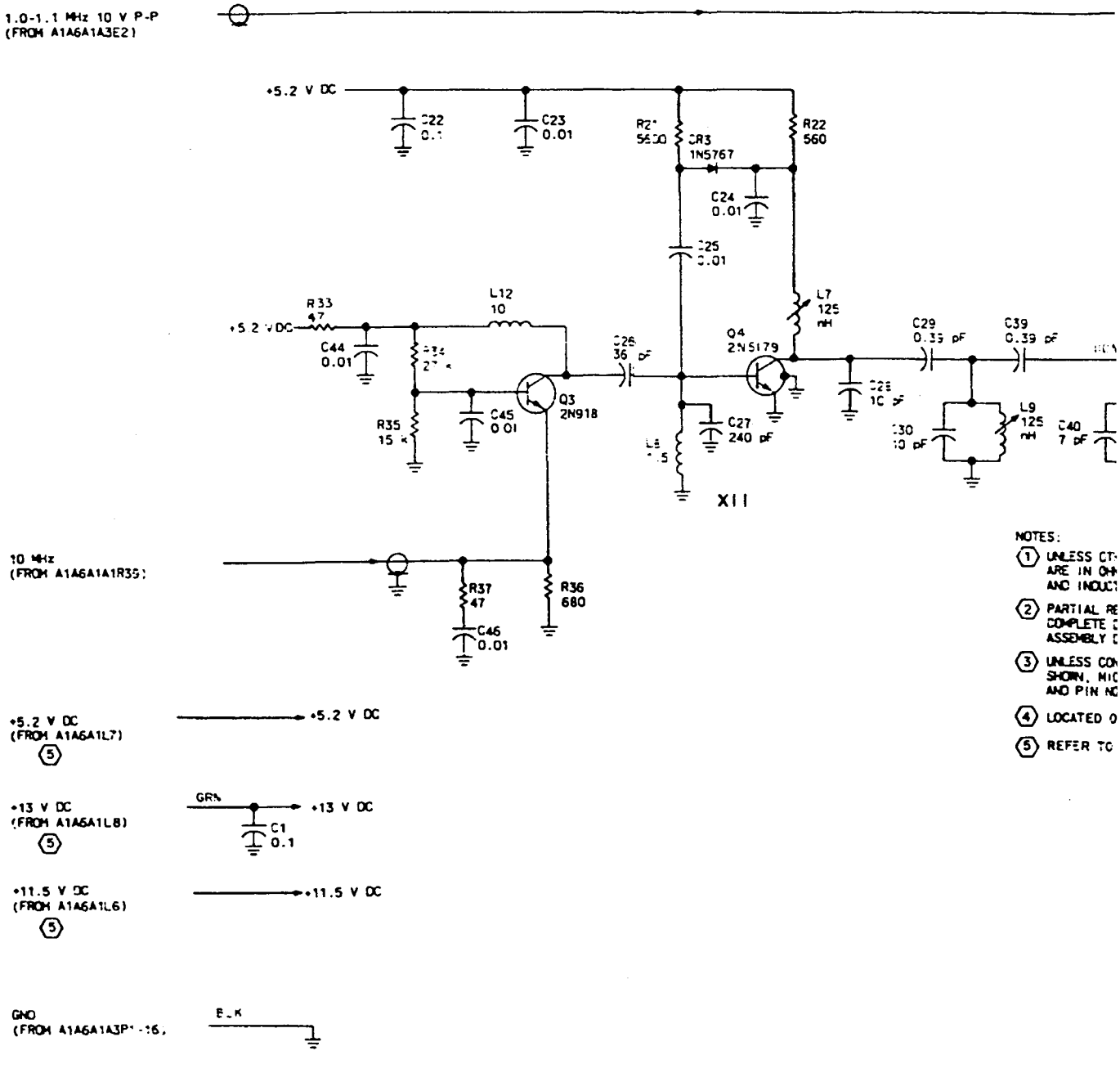
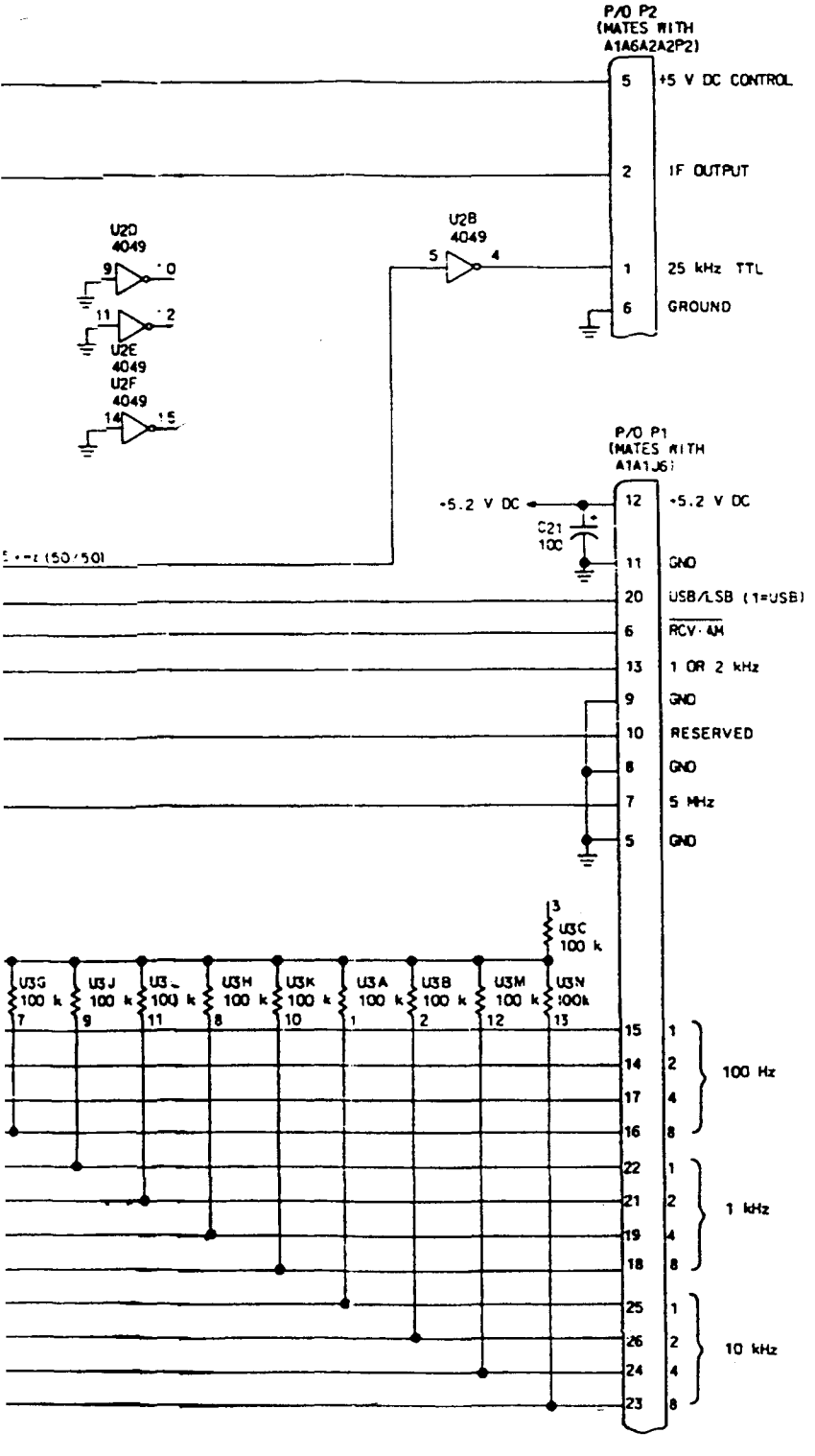
Figure 4-10. Frequency Converter A1A6A1A4, Schematic Diagram



NOTES:

1. UNLESS OTHERWISE SPECIFIED, RESISTANCE VALUES ARE IN OHMS, CAPACITANCE VALUES ARE IN MICROFARADS AND INDUCTANCE VALUES ARE IN MICROHENRYS.
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION, PREFIX WITH UNIT AND/OR ASSEMBLY DESIGNATION.
3. UNLESS CONNECTIONS TO POWER AND GROUND ARE SHOWN, MICROCIRCUIT PIN NO. 14 IS +13 V DC AND PIN NO. 7 IS GROUND.
4. LOCATED ON A1A6A1.
5. REFER TO A1A6A1A3 FOR A1A6A1 COMPONENT.


1.0-1.1 MHz 10 V P-P
(FROM A1A6A1A3E21)
+5.2 V DC
C22
0.1
C23
0.01
R22
560
CR3
1N5767
C24
0.01
C25
0.01
L7
125
nH
R33
47
+5.2 V DC
L12
10
C44
0.01
C45
0.01
Q3
2N918
R35
15
R37
47
C46
0.01
R36
680
Q4
2N5179
C27
240 pF
C29
0.39 pF
C39
0.39 pF
L9
125
nH
C40
7 pF
XII
10 MHz
(FROM A1A6A1A1R35)
NOTES:
1 UNLESS OT
ARE IN OH
AND INDUC
2 PARTIAL RE
COMPLETE
ASSEMBLY
3 UNLESS CO
SHOWN, MI
AND PIN NO
4 LOCATED O
5 REFER TO
+5.2 V DC
(FROM A1A6A1L7)
5
+5.2 V DC
+13 V DC
(FROM A1A6A1L8)
5
GRN
C1
0.1
+13 V DC
+11.5 V DC
(FROM A1A6A1L6)
5
+11.5 V DC
GND
(FROM A1A6A1A3P1-16,
BLK



NOTES:

1. UNLESS OTHERWISE SPECIFIED RESISTANCE VALUES ARE IN OHMS, CAPACITANCE VALUES ARE IN MICROFARADE, AND INDUCTANCE VALUES ARE IN MICROHENRYS.
2. UNLESS OTHERWISE NOTED, DIODES ARE TYPE 1N4454 AND TRANSISTORS ARE TYPE 2N2222A.
3. UNLESS CONNECTION TO POWER AND GROUND ARE SHOWN, MICROCIRCUIT PIN NO. 1 IS +5.2 V DC AND PIN NO. 8 IS GROUND, EXCEPT 1558 WHERE MICROCIRCUIT PIN NO. 8 IS +13 V DC AND PIN NO. 4 IS GROUND.
4. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION, PREFIX WITH UNIT AND/OR ASSEMBLY DESIGNATION.
5. VALUE SELECTED DURING FINAL TEST

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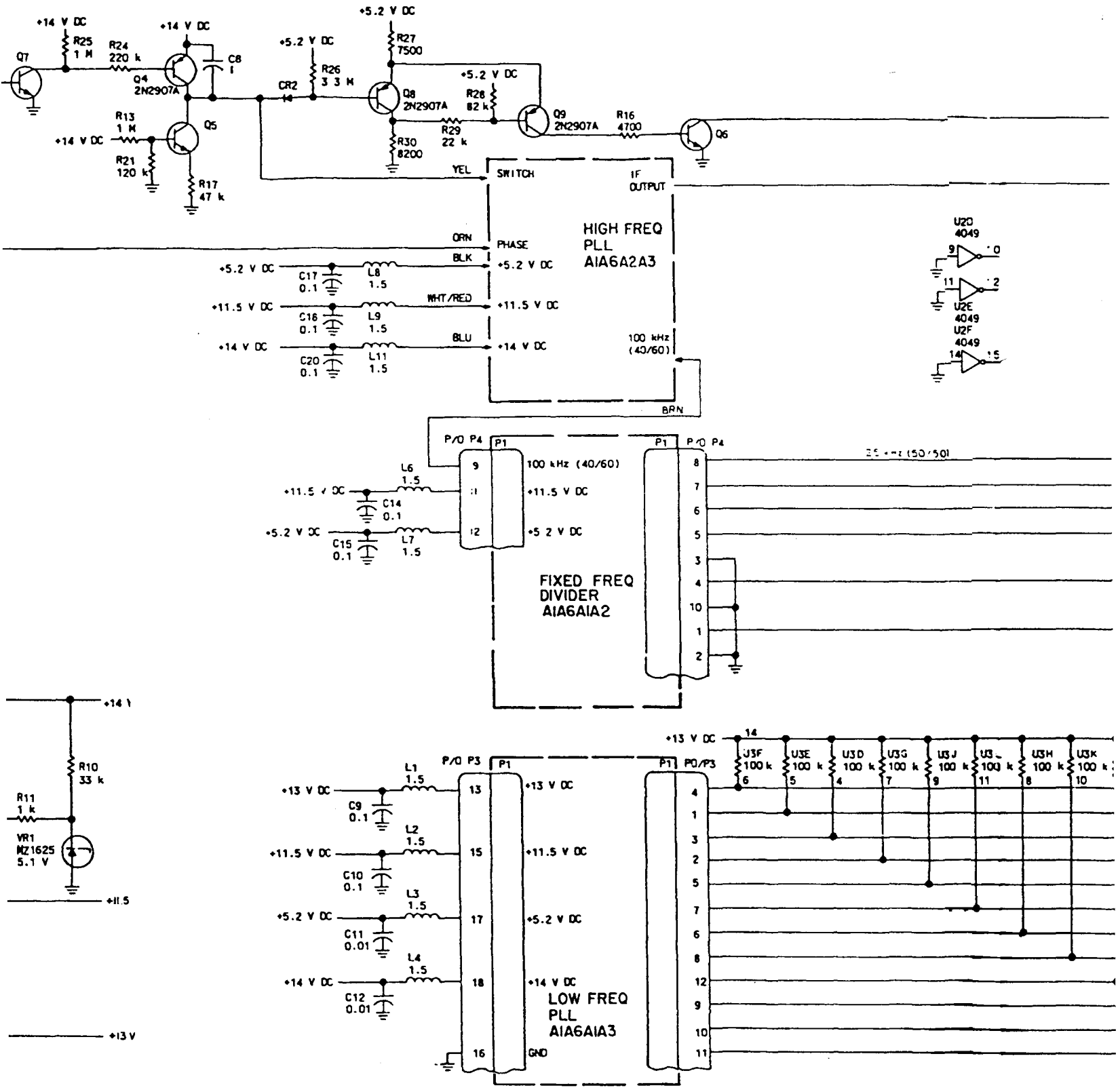
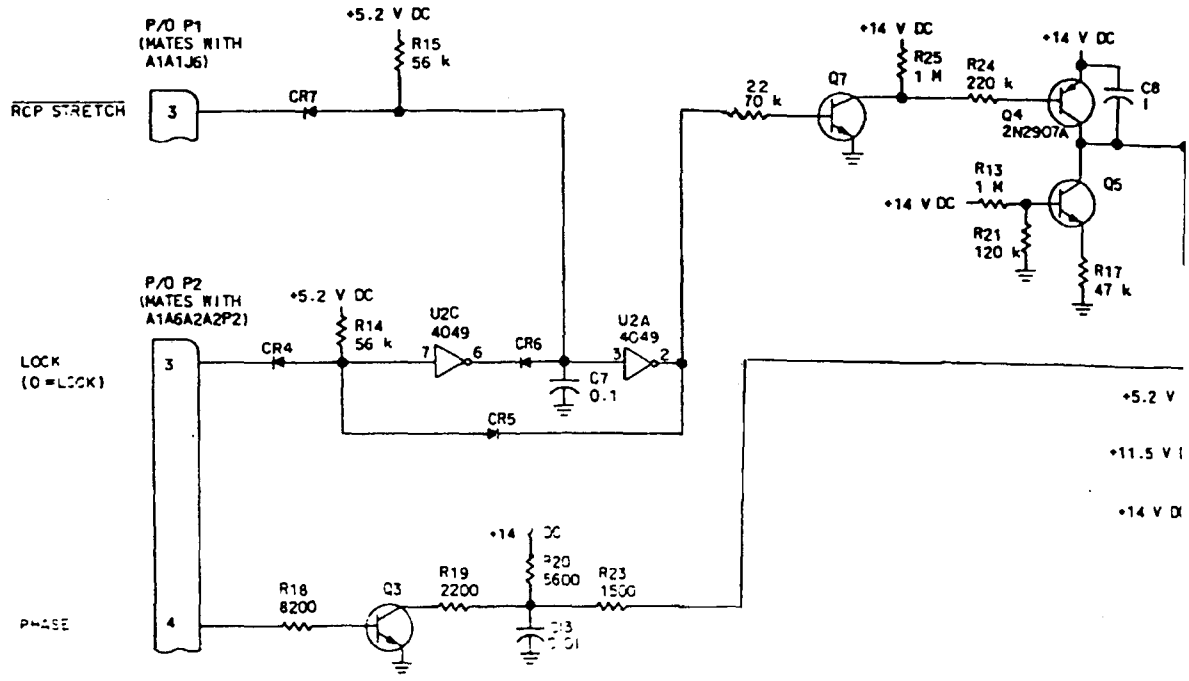
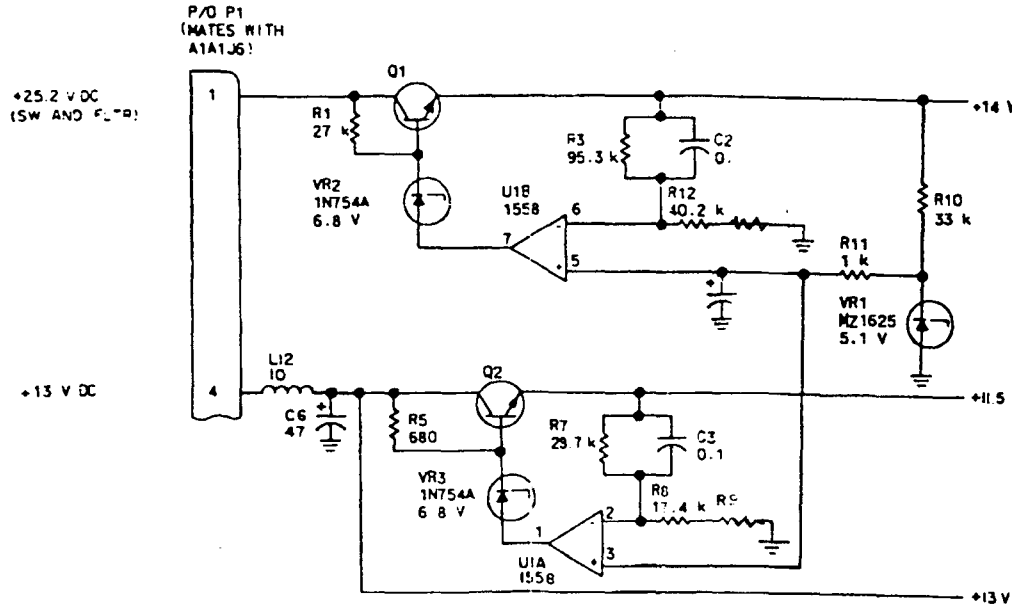
TPA-0071-015

Figure 4-11. Voltage Regulator A1A6A2A1 Schematic Diagram


+14 V DC
R25 1 M
R24 220 k
Q7
Q4 2N2907A
C8 1
+14 V DC
R13 1 M
+14 V DC
R21 120 k
Q5
R17 47 k
+5.2 V DC
R26 3 3 M
CR2
+5.2 V DC
R27 7500
Q8 2N2907A
R30 8200
+5.2 V DC
R28 82 k
R29 22 k
Q9 2N2907A
R16 4700
Q6
YEL
SWITCH
IF OUTPUT
HIGH FREQ PLL AIA6A2A3
ORN
PHASE
BLK
+5.2 V DC
+5.2 V DC
C17 0.1
L8 1.5
WHT/RED
+11.5 V DC
+11.5 V DC
C16 0.1
L9 1.5
BLU
+14 V DC
+14 V DC
C20 0.1
L11 1.5
100 kHz (40/60)
BRN
U2D 4049
U2E 4049
U2F 4049
P/O P4
P1
100 kHz (40/60)
+11.5 V DC
L6 1.5
C14 0.1
+5.2 V DC
+5 2 V DC
C15 0.1
L7 1.5
FIXED FREQ DIVIDER AIA6AIA2
P/O P4
P1
+14 V
R10 33 k
R11 1 k
VR1 MZ1625 5.1 V
+11.5
+13 V
+13 V DC
P/O P3
P1
L1 1.5
C9 0.1
+11.5 V DC
L2 1.5
C10 0.1
+5.2 V DC
L3 1.5
C11 0.01
+14 V DC
L4 1.5
C12 0.01
+13 V DC
+11.5 V DC
+5.2 V DC
+14 V DC
GND
LOW FREQ PLL AIA6AIA3
P1
P0/P3
+13 V DC
U3F 100 k
U3E 100 k
U3D 100 k
U3G 100 k
U3J 100 k
U3H 100 k
U3K 100 k


P/O P1
(MATES WITH
A1A1J6)
+5.2 V DC
R15
56 k
RCP STRETCH
3
CR7
22
70 k
+14 V DC
R25
1 M
Q7
R24
220 k
+14 V DC
C8
1
Q4
2N2907A
R13
1 K
Q5
+14 V DC
R21
120 k
R17
47 k
P/O P2
(MATES WITH
A1A6A2A2P2)
+5.2 V DC
R14
56 k
U2C
4049
U2A
4049
LOCK
(0 = LOCK)
3
CR4
CR6
C7
0.1
CR5
+5.2 V
+11.5 V
+14 V DC
+14 V DC
R20
5600
R19
2200
R23
1500
R18
8200
Q3
PHASE
4


P/O P1
(MATES WITH
A1A1J6)
+25.2 V DC
(SW AND FLTR)
1
Q1
R1
27 k
+14 V
R3
95.3 k
C2
0.
VR2
1N754A
6.8 V
U1B
1558
6
7
R12
40.2 k
R10
33 k
R11
1 k
5
VR1
MZ1625
5.1 V
+13 V DC
4
L12
10
C6
47
Q2
+11.5
R5
680
R7
29.7 k
C3
0.1
VR3
1N754A
6.8 V
R8
17.4 k
R9
2
1
3
U1A
1558
+13 V

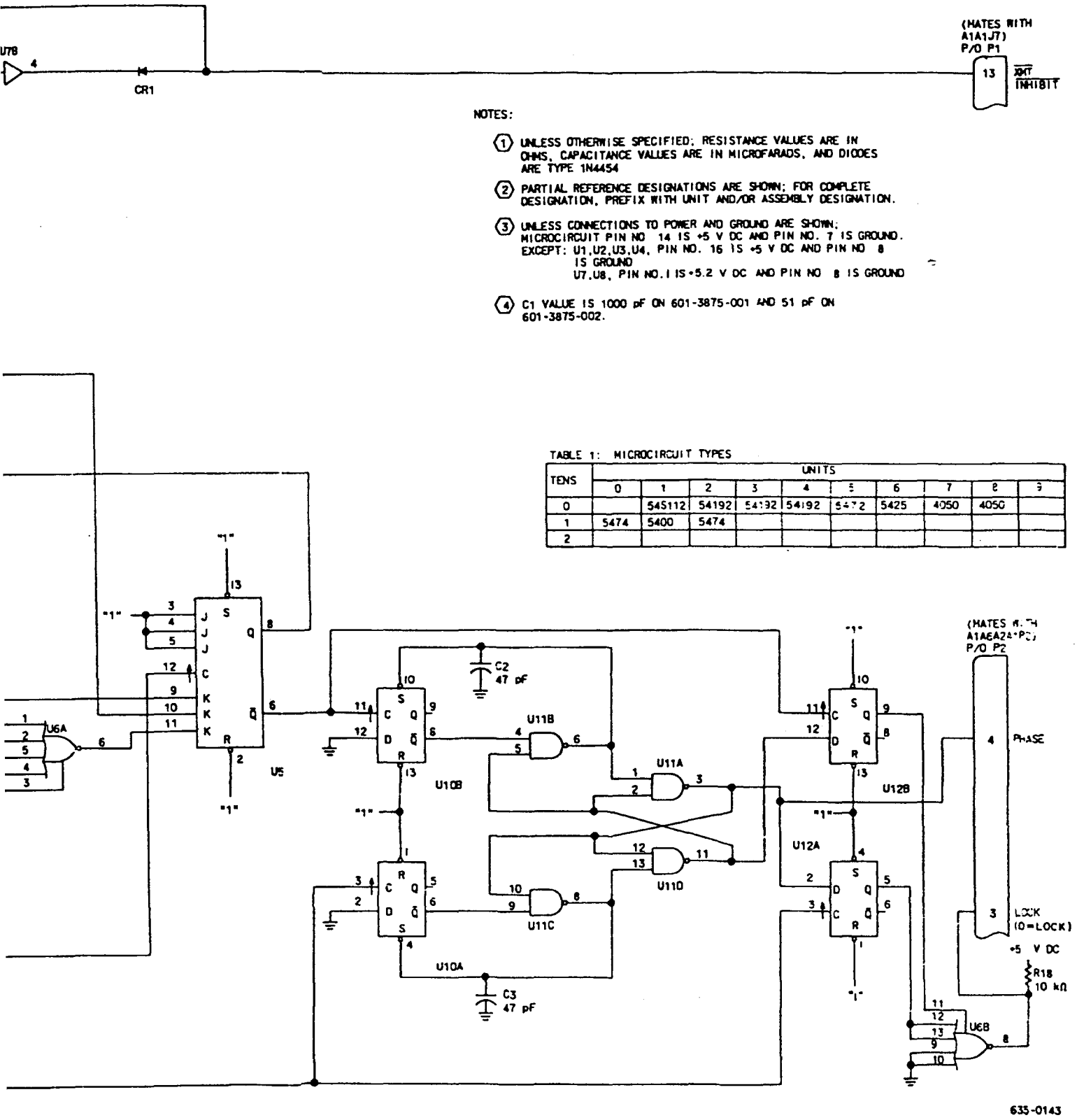
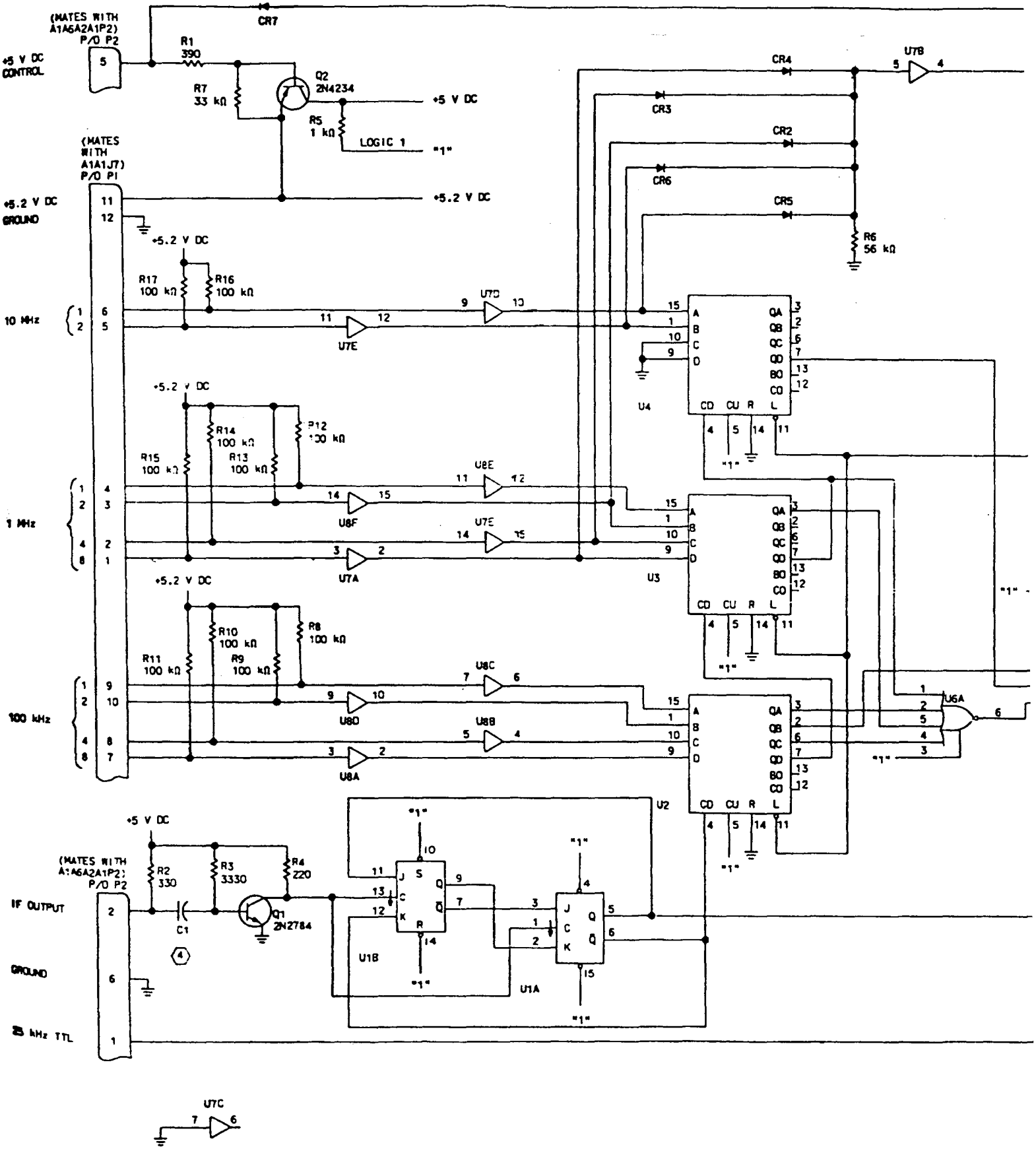
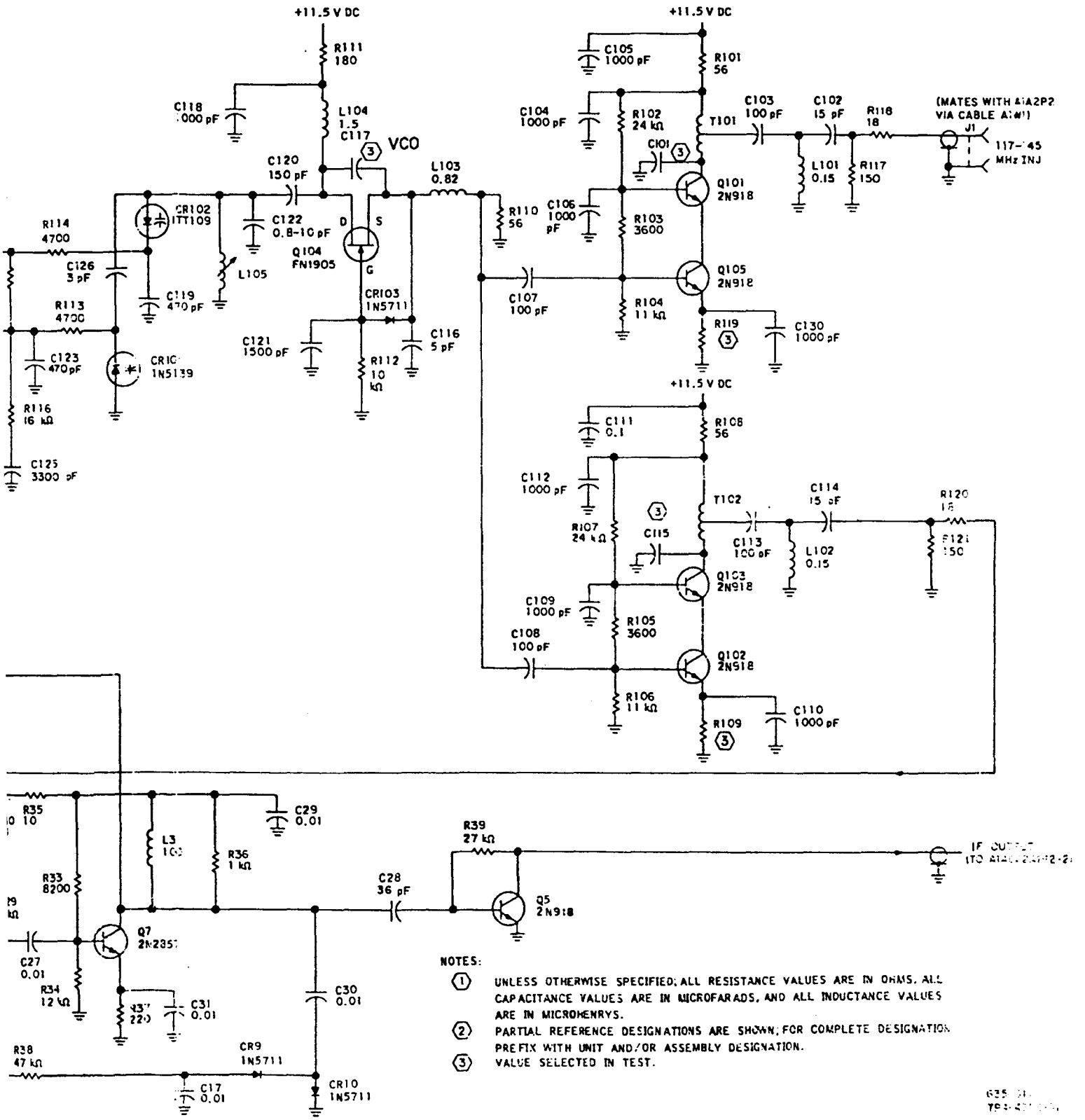


Figure 4-12. Variable Frequency Divider A1A6A2A2, Schematic Diagram

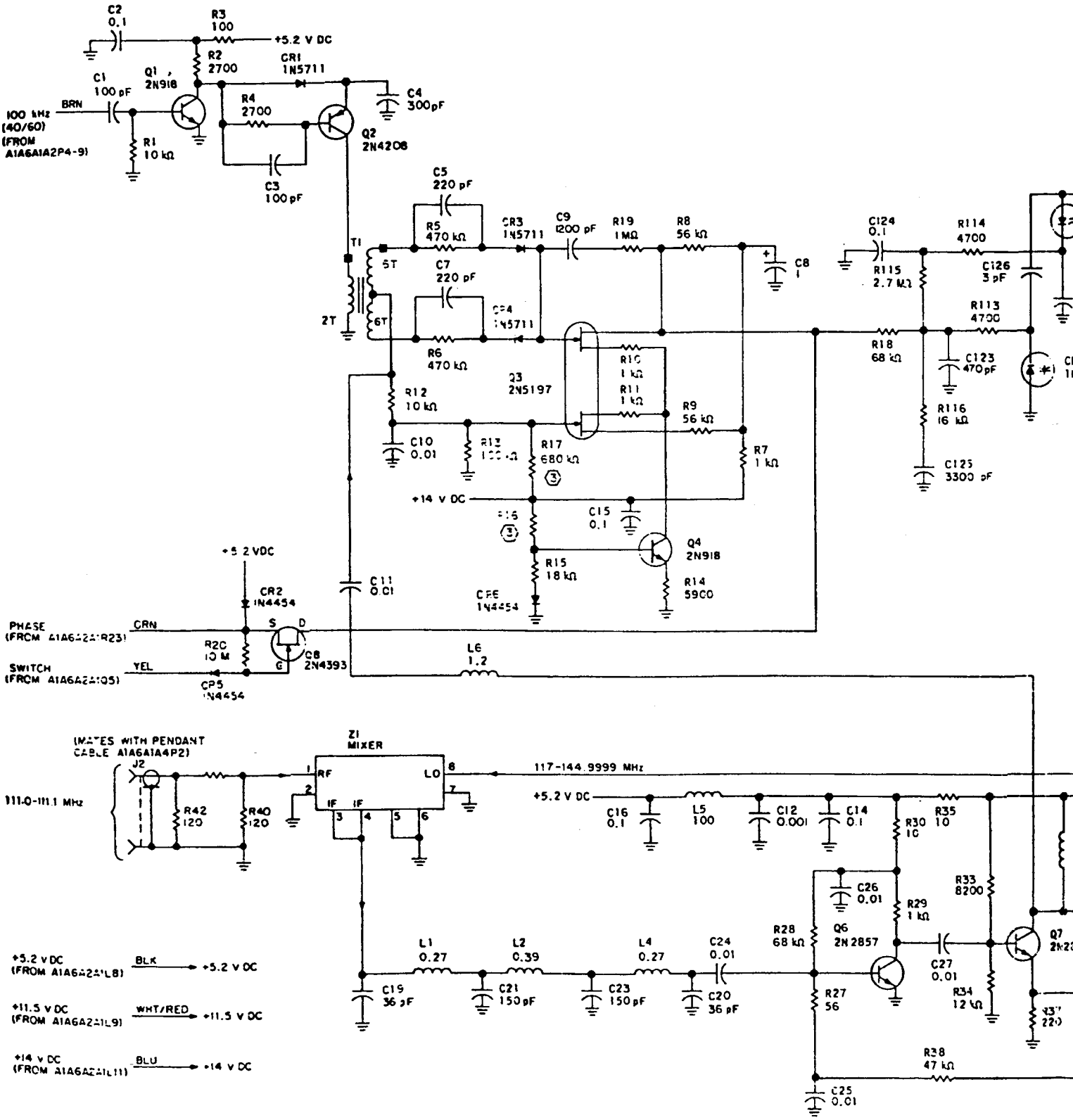

(MATES WITH A1A6A2A1P2) P/O P2
+5 V DC CONTROL
CR7
R1 390
R7 33 kΩ
Q2 2N4234
+5 V DC
R5 1 kΩ
LOGIC 1
"1"
(MATES WITH A1A1J7) P/O P1
+5.2 V DC
GROUND
+5.2 V DC
CR4
CR3
CR2
CR6
CR5
U7B
R6 56 kΩ
10 MHz
1 MHz
100 kHz
R17 100 kΩ
R16 100 kΩ
R14 100 kΩ
R12 100 kΩ
R15 100 kΩ
R13 100 kΩ
R10 100 kΩ
R8 100 kΩ
R11 100 kΩ
R9 100 kΩ
U7D
U7E
U8E
U8F
U7E
U7A
U8C
U8D
U8B
U8A
U4
U3
U6A
U2
U1B
U1A
IF OUTPUT
GROUND
25 kHz TTL
(MATES WITH A1A6A2A1P2) P/O P2
R2 330
R3 3330
R4 220
C1
Q1 2N2784
U7C



NOTES:

1. UNLESS OTHERWISE SPECIFIED; ALL RESISTANCE VALUES ARE IN OHMS. ALL CAPACITANCE VALUES ARE IN MICROFARADS, AND ALL INDUCTANCE VALUES ARE IN MICROHENRYS.
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION PREFIX WITH UNIT AND/OR ASSEMBLY DESIGNATION.
3. VALUE SELECTED IN TEST.

Figure 4-13. Hf Phase-Lock Loop A1A6A1A3, Schematic Diagram


C2 0.1
R3 100
+5.2 V DC
R2 2700
CR1 1N5711
C1 100 pF
Q1 2N918
C4 300pF
100 kHz (40/60) (FROM A1A6A1A2P4-9)
BRN
R4 2700
Q2 2N4208
R1 10 kΩ
C3 100 pF
C5 220 pF
R5 470 kΩ
CR3 1N5711
C9 1200 pF
R19 1 MΩ
R8 56 kΩ
C8 1
T1
5T
C7 220 pF
2T
6T
CR4 1N5711
R6 470 kΩ
Q3 2N5197
R10 1 kΩ
R11 1 kΩ
R12 10 kΩ
R9 56 kΩ
C10 0.01
R13 100 Ω
R17 680 kΩ
R7 1 kΩ
+14 V DC
C15 0.1
Q4 2N918
R15 18 kΩ
R14 5900
CR5 1N4454
C11 0.01
+5.2 VDC
CR2 1N4454
PHASE (FROM A1A6A2A1R23)
GRN
SWITCH (FROM A1A6A2A1Q5)
YEL
R20 10 M
Q8 2N4393
CR5 1N4454
L6 1.2
C124 0.1
R114 4700
R115 2.7 MΩ
C126 3 pF
R113 4700
R18 68 kΩ
C123 470 pF
R116 16 kΩ
C125 3300 pF
(MATES WITH PENDANT CABLE A1A6A1A4P2)
J2
A1
A2
A3
A4
111.0-111.1 MHz
R42 120
R40 120
Z1 MIXER
RF
LO
IF
IF
117-144.9999 MHz
+5.2 V DC
C16 0.1
L5 100
C12 0.001
C14 0.1
R30 10
R35 10
C26 0.01
R29 1 kΩ
R33 8200
R28 68 kΩ
Q6 2N2857
L1 0.27
L2 0.39
L4 0.27
C24 0.01
C19 36 pF
C21 150 pF
C23 150 pF
C20 36 pF
C27 0.01
R27 56
R34 12 kΩ
R38 47 kΩ
C25 0.01
+5.2 VDC (FROM A1A6A2A1L8)
BLK
+5.2 V DC
+11.5 V DC (FROM A1A6A2A1L9)
WHT/RED
+11.5 V DC
+14 V DC (FROM A1A6A2A1L11)
BLU
+14 V DC

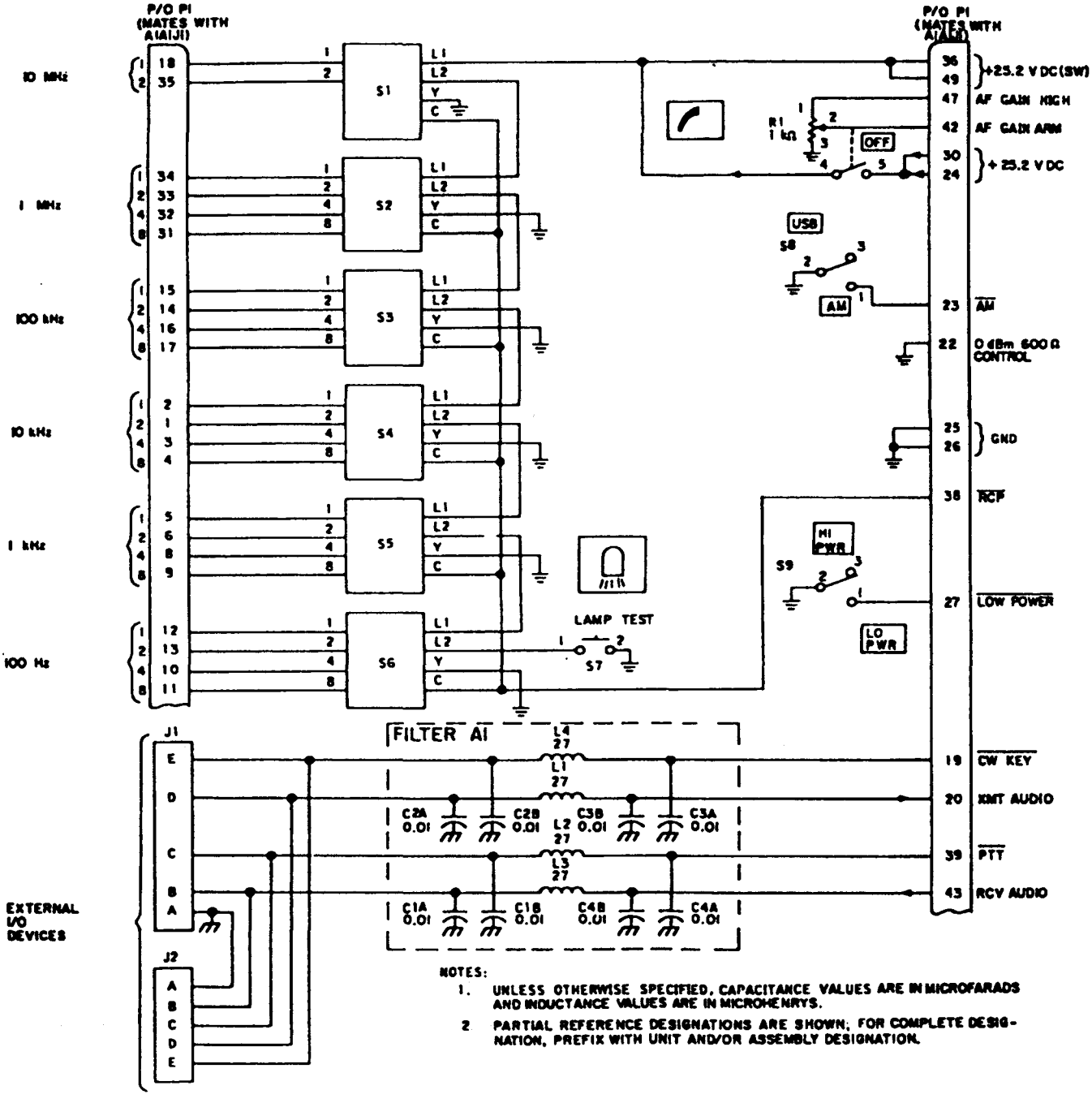
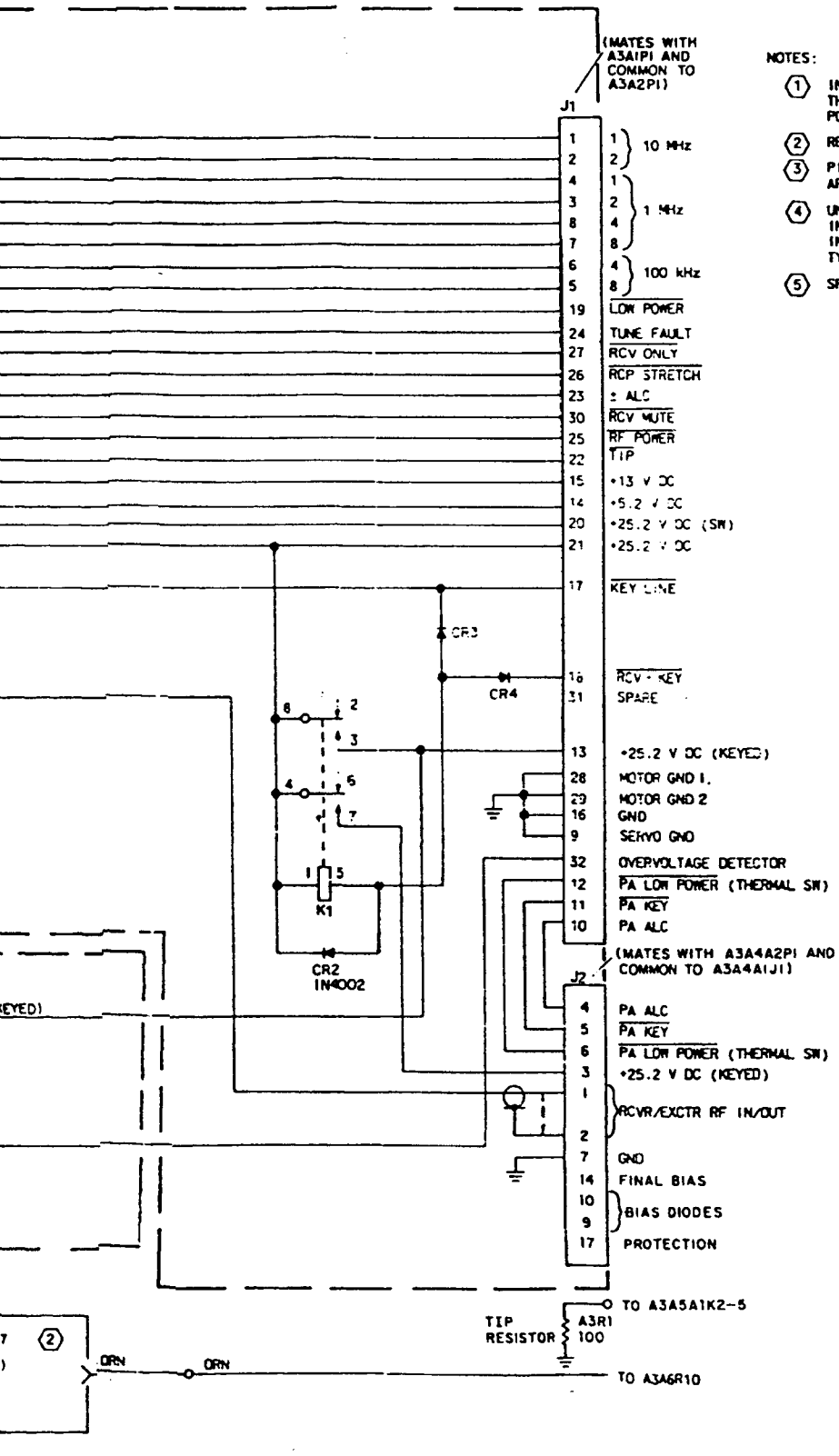


Figure 4-14. Receiver-Transmitter Control Az C-5310/URC, Schematic Diagram



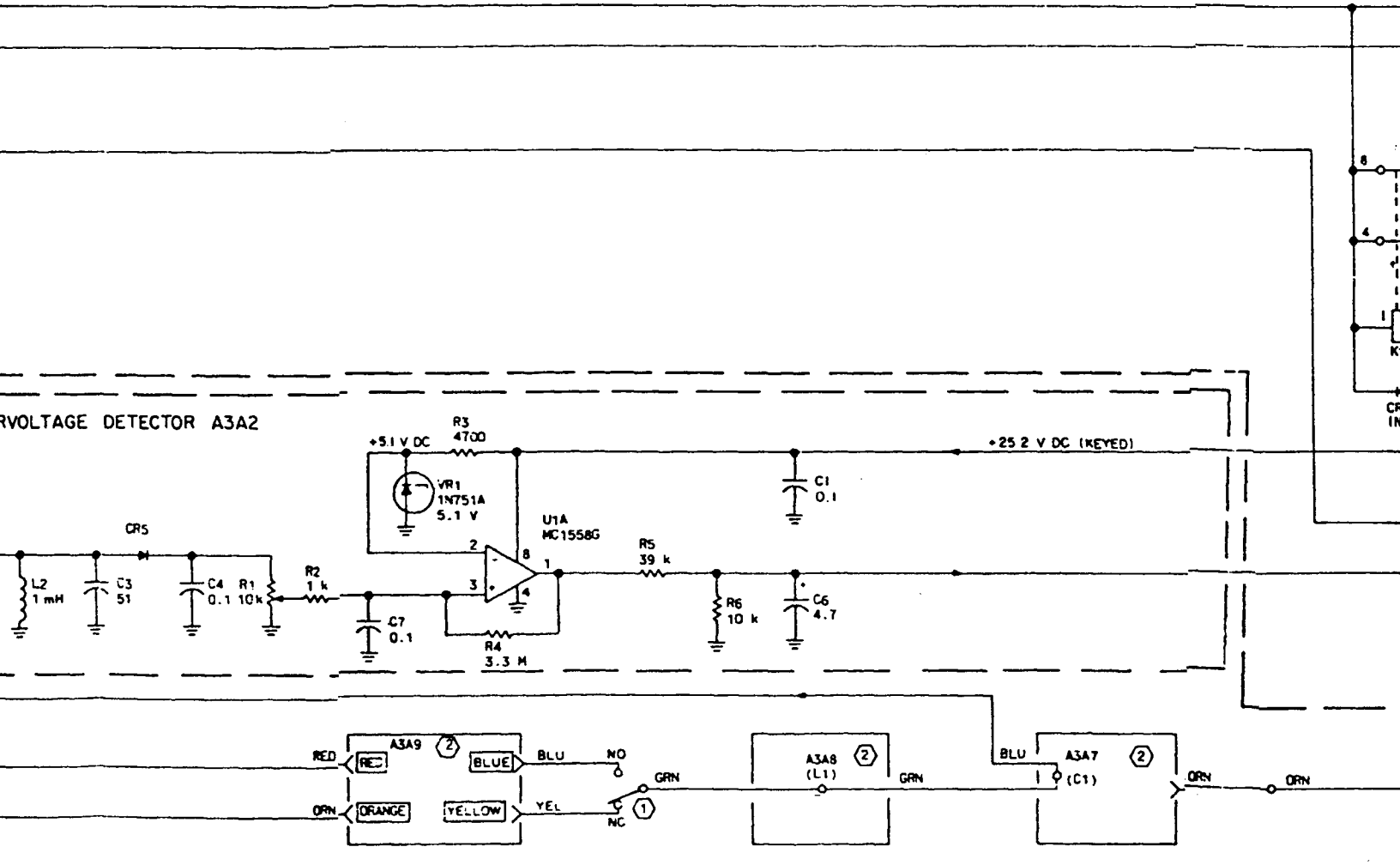
NOTES:

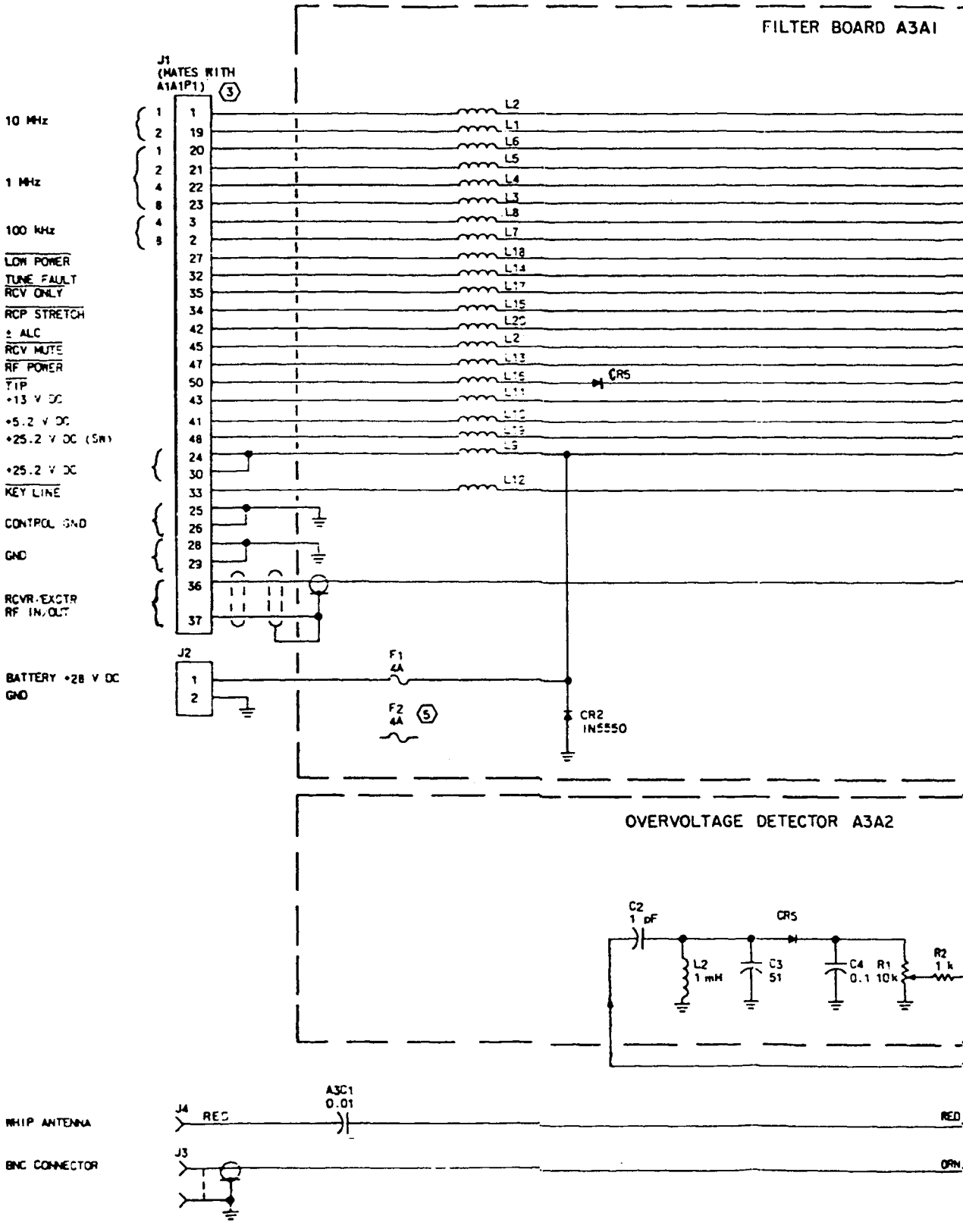
1. INSERTION OF THE WHIP ANTENNA MECHANICALLY CHANGES THE CIRCUIT FROM NORMALLY CLOSED TO NORMALLY OPEN POSITION.
2. REFER TO SCHEMATIC OF THIS ASSEMBLY.
3. PINS 4 THRU 18, 31, 38, 39, 40, 44, 46, 49 AND 51 ON A3J1 ARE SPARES.
4. UNLESS OTHERWISE SPECIFIED RESISTANCE VALUES ARE IN OHMS, CAPACITANCE VALUES ARE IN MICROFARADS, AND INDUCTANCE VALUES ARE 100 uH, AND DIODES ARE TYPE 1N4454.
5. SPARE FUSE

6A[illegible]225
TPA 3072-015

Figure 4-15. Amplifier-Coupler A3, AM-5280/URC, Schematic Diagram

FILTER BOARD A3A1




FILTER BOARD A3A1
J1
(MATES WITH
A1A1P1)
3
10 MHz
1 MHz
100 kHz
LOW POWER
TUNE FAULT
RCV ONLY
RCP STRETCH
± ALC
RCV MUTE
RF POWER
TIP
+13 V DC
+5.2 V DC
+25.2 V DC (SW)
+25.2 V DC
KEY LINE
CONTROL GND
GND
RCVR-EXCTR
RF IN/OUT
L2
L1
L6
L5
L4
L3
L8
L7
L18
L14
L17
L15
L20
L2
L13
L16
L11
L19
L9
L12
CR5
J2
BATTERY +28 V DC
GND
F1
4A
F2
4A
5
CR2
IN5550
OVERVOLTAGE DETECTOR A3A2
C2
1 pF
CR5
L2
1 mH
C3
51
C4
0.1
R1
10k
R2
1 k
WHIP ANTENNA
BNC CONNECTOR
J4
RED
A3C1
0.01
J3
RED
ORN

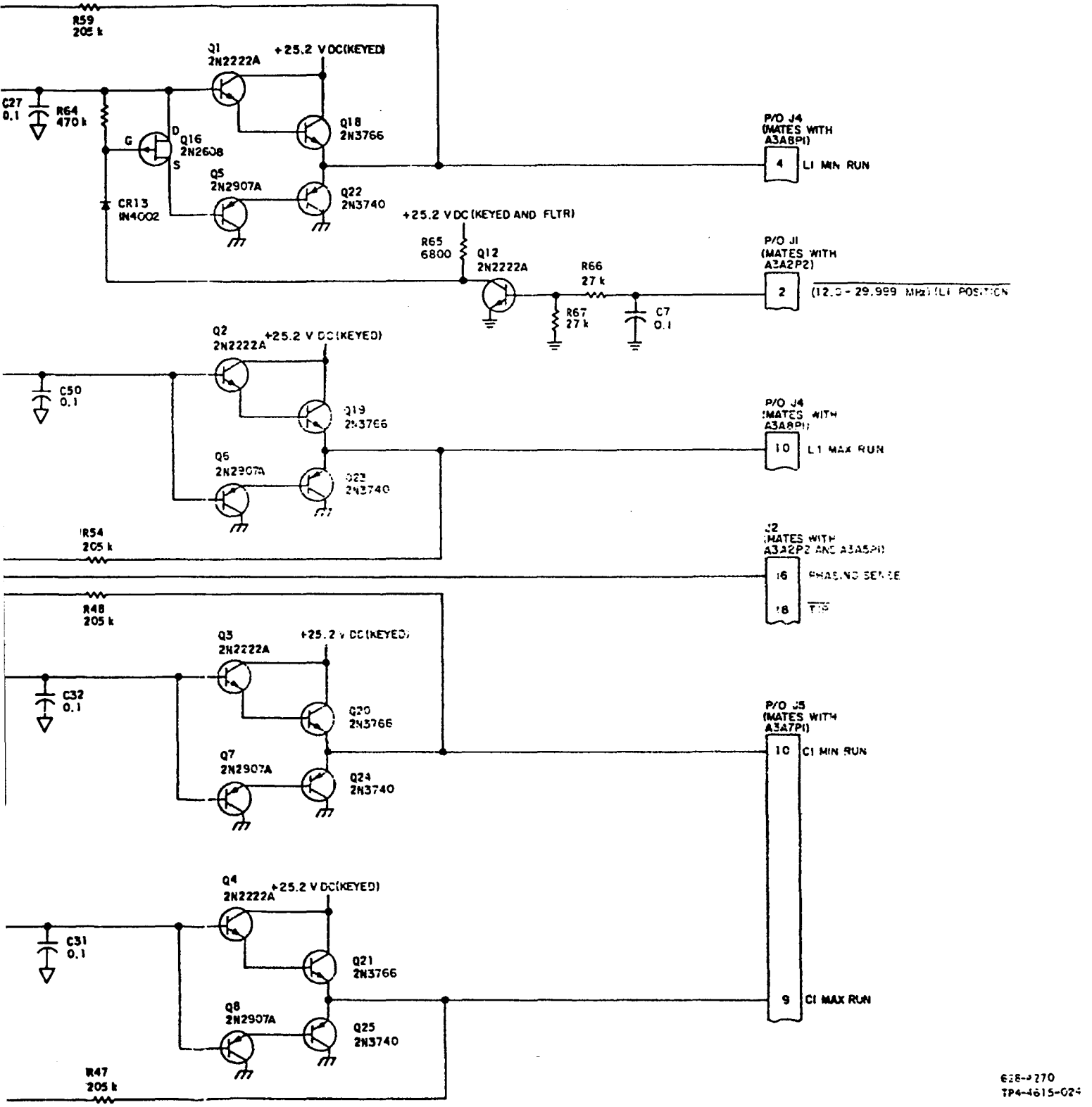
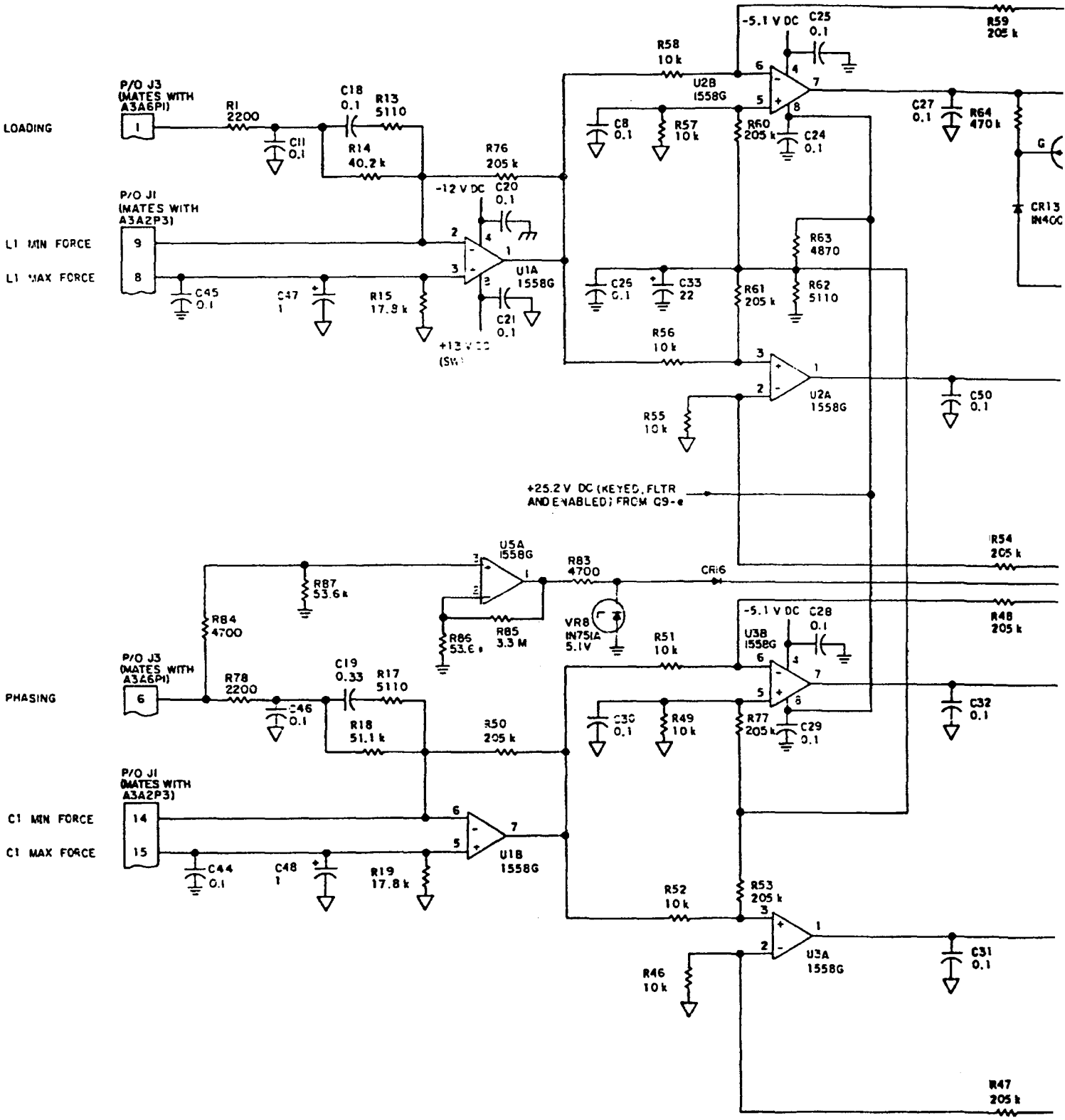
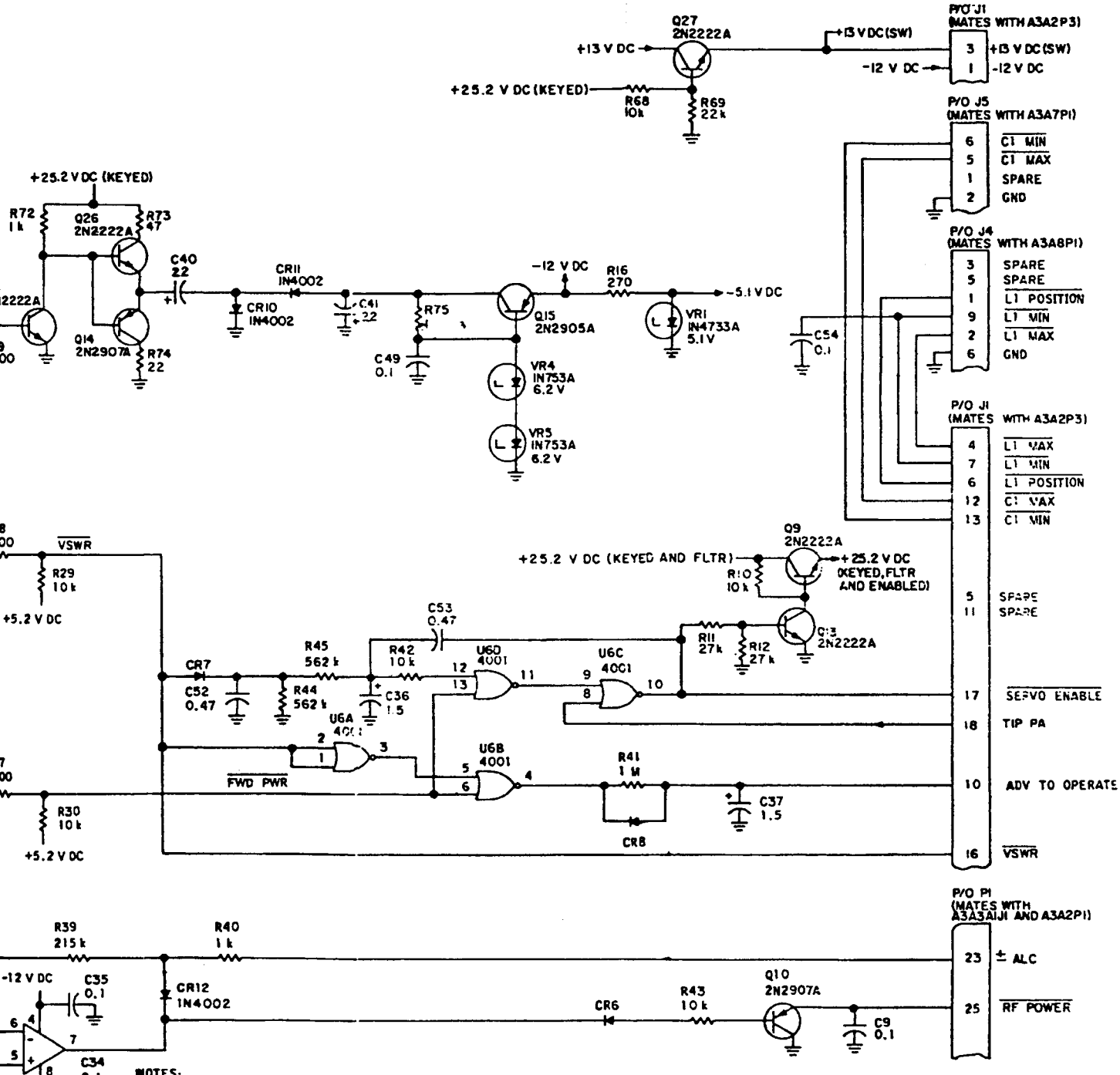


Figure 4-16. Servo Amplifier A3A1. Schematic Diagram (Sheet 1 of 2)


LOADING
P/O J3 (MATES WITH A3A6P1)
1
R1 2200
C11 0.1
C18 0.1
R13 5110
R14 40.2 k
R76 205 k
P/O J1 (MATES WITH A3A2P3)
L1 MIN FORCE
9
L1 MAX FORCE
8
C45 0.1
C47 1
R15 17.8 k
-12 V DC
C20 0.1
U1A 1558G
C21 0.1
+13 V DC (SW)
-5.1 V DC
C25 0.1
R58 10 k
U2B 1558G
C8 0.1
R57 10 k
R60 205 k
C24 0.1
R59 205 k
C27 0.1
R64 470 k
CR13 IN400
R63 4870
C26 0.1
C33 22
R61 205 k
R62 5110
R56 10 k
U2A 1558G
C50 0.1
R55 10 k
+25.2 V DC (KEYED, FLTR AND ENABLED) FROM G9-e
PHASING
P/O J3 (MATES WITH A3A6P1)
6
R78 2200
C46 0.1
C19 0.33
R17 5110
R18 51.1 k
R50 205 k
R84 4700
R87 53.6 k
U5A 1558G
R83 4700
CR16
R86 53.6 k
R85 3.3 M
VR8 IN751A 5.1V
R54 205 k
R48 205 k
-5.1 V DC
C28 0.1
U3B 1558G
R51 10 k
C30 0.1
R49 10 k
R77 205 k
C29 0.1
C32 0.1
P/O J1 (MATES WITH A3A2P3)
C1 MIN FORCE
14
C1 MAX FORCE
15
C44 0.1
C48 1
R19 17.8 k
U1B 1558G
R52 10 k
R53 205 k
U3A 1558G
C31 0.1
R46 10 k
R47 205 k



NOTES:

1. UNLESS OTHERWISE SPECIFIED; RESISTANCE VALUES ARE IN OHMS, CAPACITANCE VALUES ARE IN MICROFARADS, INDUCTANCE VALUES ARE IN MILLIHENRYS, AND DIODES ARE TYPE 1N4454.
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION, PREFIX WITH UNIT AND/OR ASSEMBLY DESIGNATION.
3. UNLESS CONNECTION TO POWER AND GROUND ARE SHOWN; MICROCIRCUIT PIN NO. 14 IS +5 V DC AND PIN NO. 7 IS GROUND.
4. C55 USED ON MCN 1 THRU 16 ONLY.

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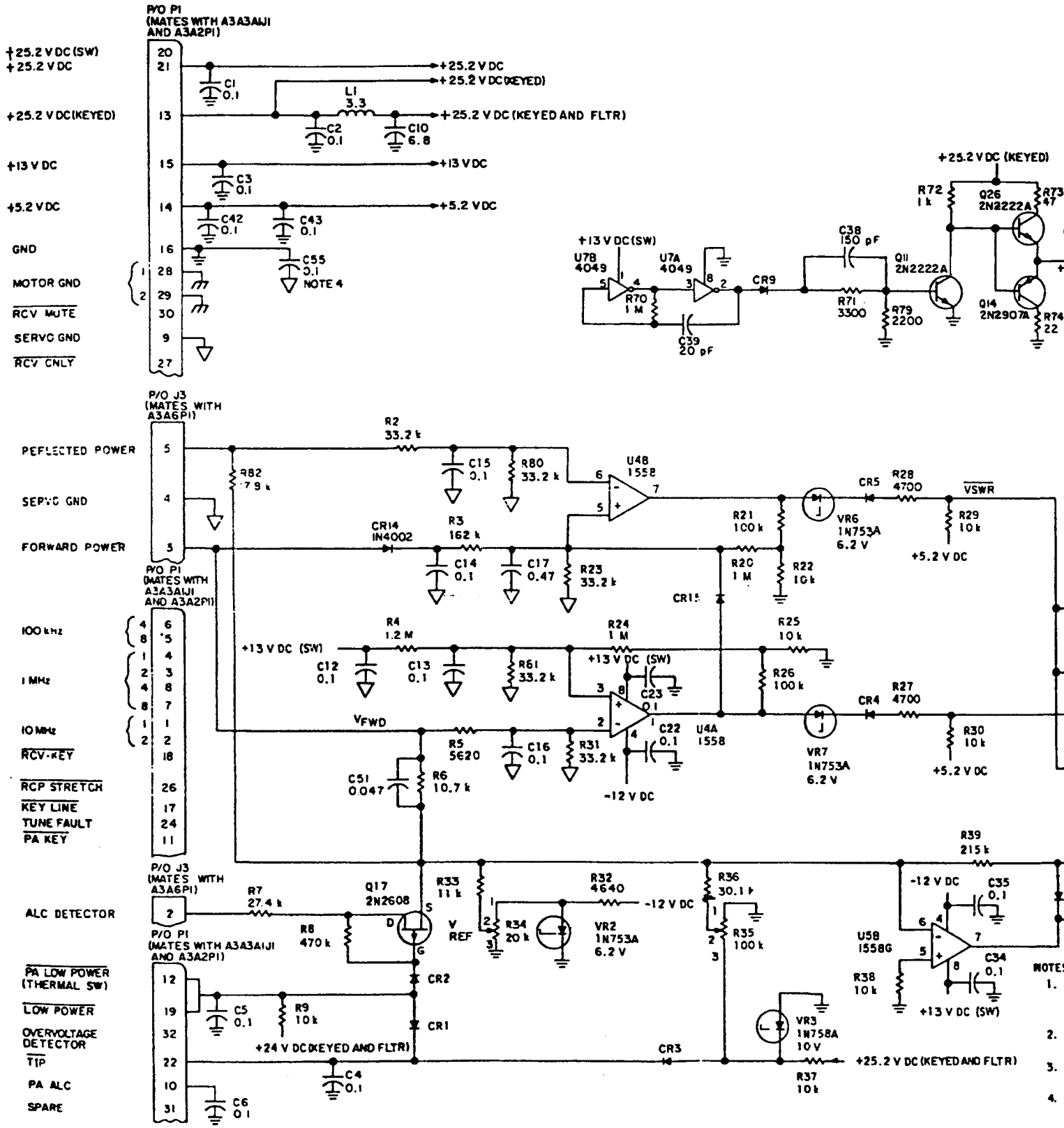
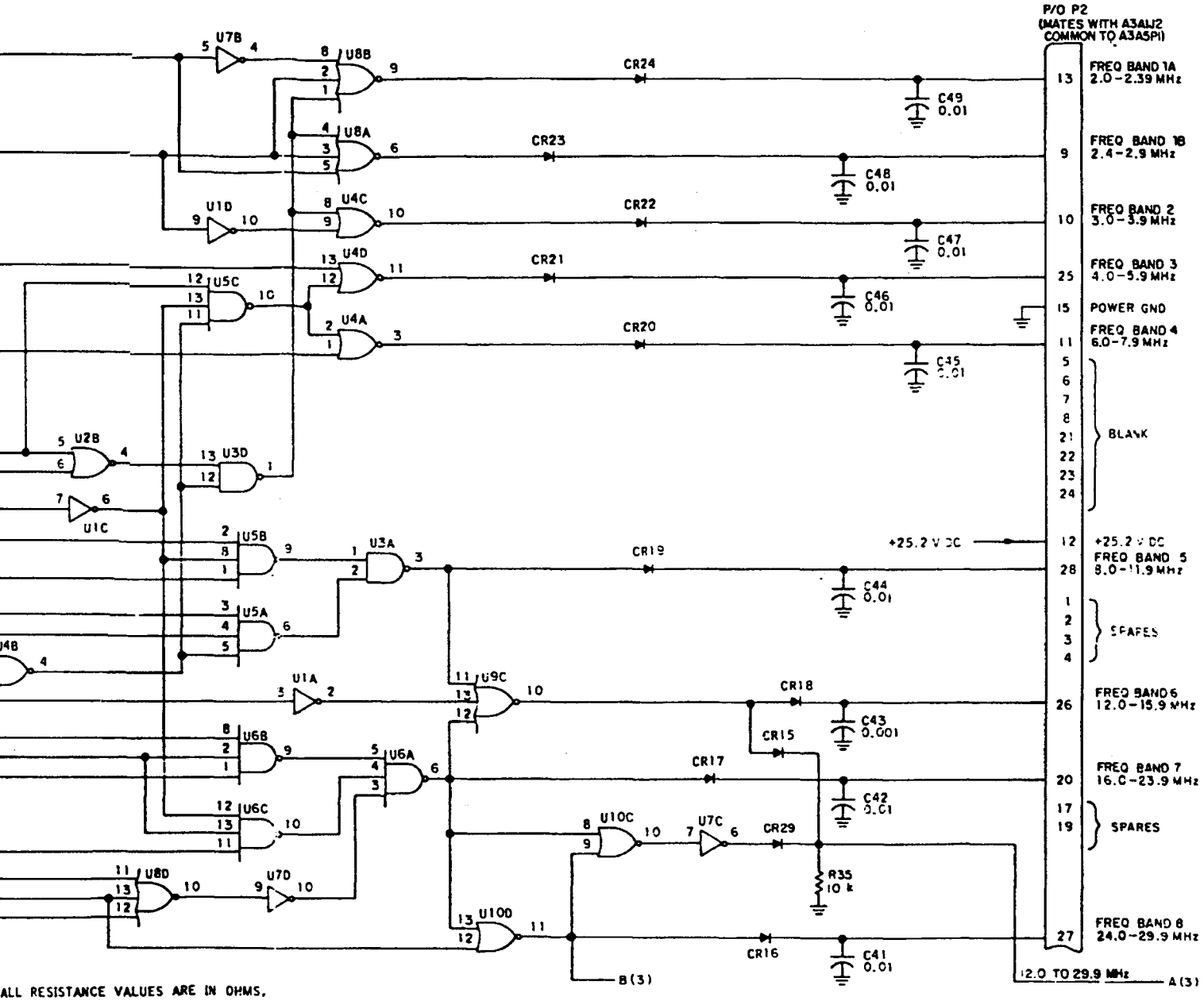
Figure 4-16. Servo Amplifier A3A1, Schematic Diagram (Sheet 2)



NOTE

HIGHEST REFERENCE DESIGNATORS USED CR16, VR8, L1, R87, C55, Q27, U7



ALL RESISTANCE VALUES ARE IN OHMS,
IN MICROFARADS, AND ALL DIODES ARE

ONS ARE SHOWN; FOR COMPLETE DESIGNATION
EMBLY DESIGNATION.
AND GROUND ARE SHOWN PIN 14 IS +5 V DC
PE 4049 WHERE PIN 1 IS +5 V DC AND PIN 8 IS GND.

	UNITS					
4	5	6	7	8	9	
4001	4023	4023	4049	4023	4025	
4011	4049	4023	4011	4023	4011	

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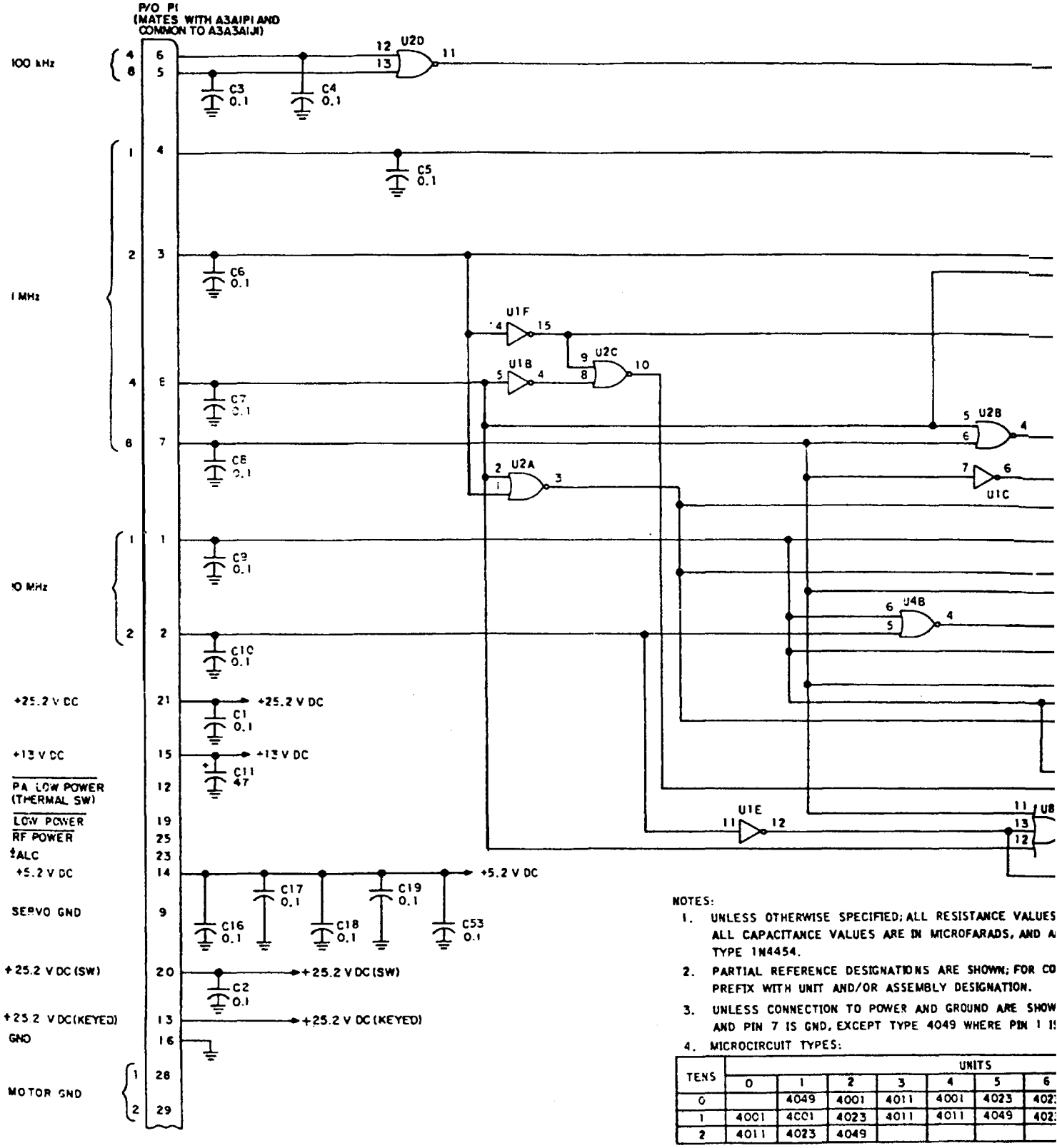
Figure 4-17. Control Logic A3A2, Schematic Diagram (Sheet 1 of 3)



NOTES:

1. UNLESS OTHERWISE SPECIFIED; ALL RESISTANCE VALUES
   ALL CAPACITANCE VALUES ARE IN MICROFARADS, AND A
   TYPE 1N4454.
2. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR CO
   PREFIX WITH UNIT AND/OR ASSEMBLY DESIGNATION.
3. UNLESS CONNECTION TO POWER AND GROUND ARE SHOW
   AND PIN 7 IS GND, EXCEPT TYPE 4049 WHERE PIN 1 IS
4. MICROCIRCUIT TYPES:

TENS	UNITS						
	0	1	2	3	4	5	6
0		4049	4001	4011	4001	4023	402
1	4001	4001	4023	4011	4011	4049	402
2	4011	4023	4049				

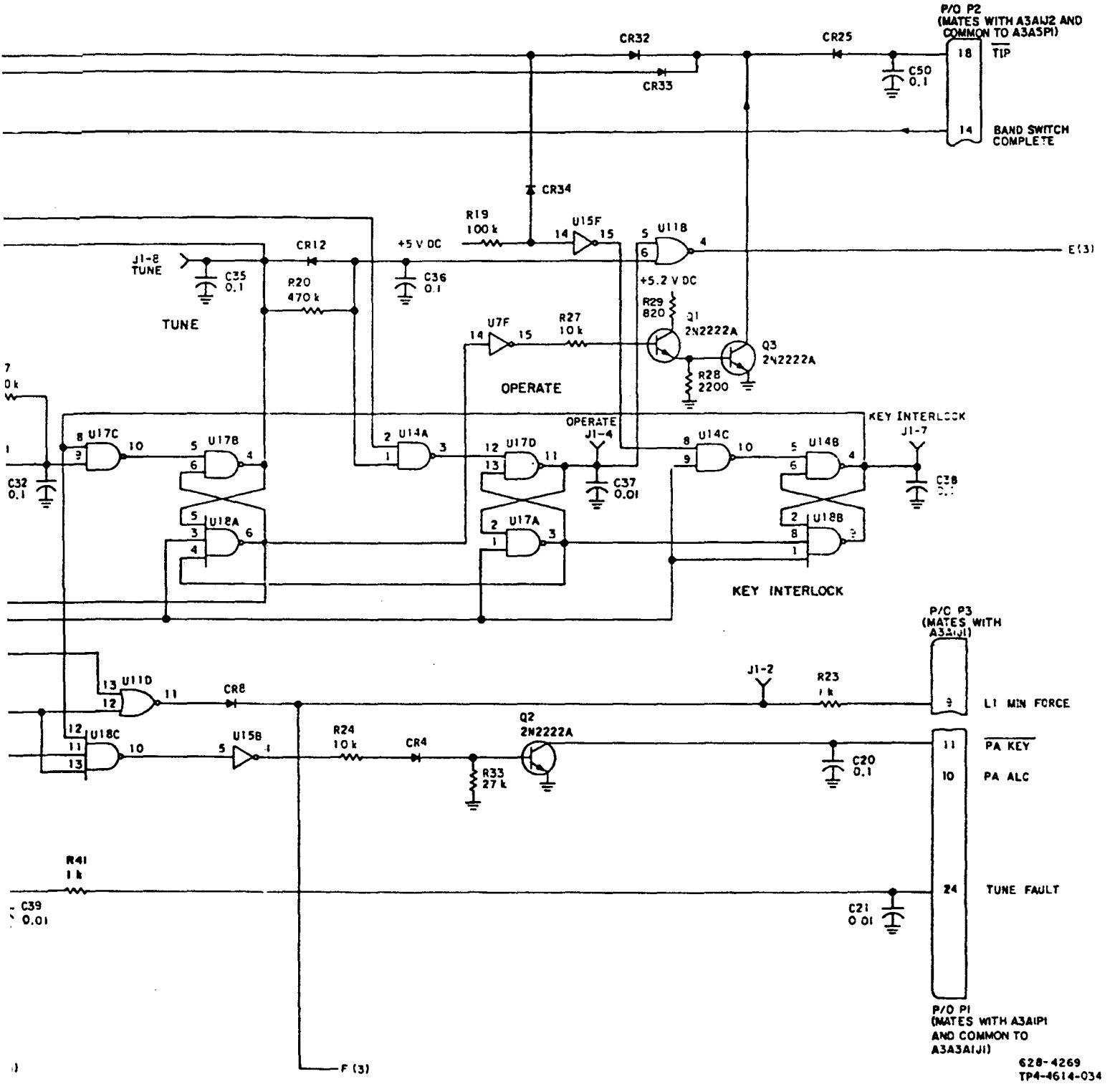
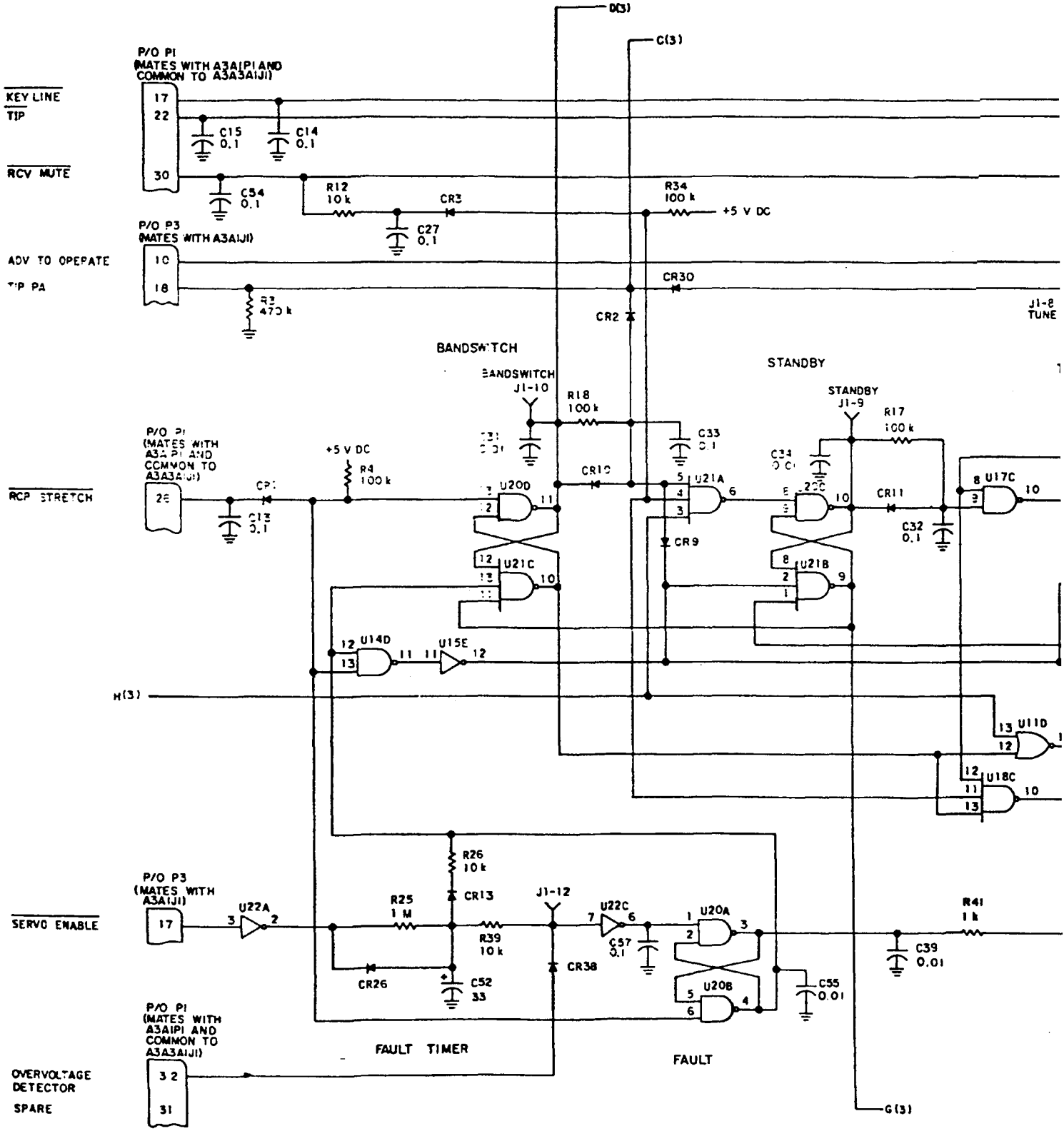


Figure 4-17. Control Logic A3A2, Schematic Diagram (Sheet 2)


D(3)
C(3)
P/O P1
(MATES WITH A3A1P1 AND
COMMON TO A3A3A1J1)
KEY LINE
TIP
17
22
30
C15
0.1
C14
0.1
RCV MUTE
C54
0.1
R12
10 k
CR3
C27
0.1
R34
100 k
+5 V DC
P/O P3
(MATES WITH A3A1J1)
ADV TO OPERATE
TIP PA
10
18
R3
470 k
CR30
CR2
J1-8
TUNE
BANDSWITCH
BANDSWITCH
J1-10
R18
100 k
C31
0.01
C33
0.1
STANDBY
STANDBY
J1-9
R17
100 k
C34
0.01
P/O P1
(MATES WITH
A3A1P1 AND
COMMON TO
A3A3A1J1)
RCP STRETCH
28
CR1
C13
0.1
+5 V DC
R4
100 k
CR10
U20D
U21A
CR11
U17C
C32
0.1
CR9
U21C
U21B
U14D
U15E
H(3)
U11D
U18C
R26
10 k
P/O P3
(MATES WITH
A3A1J1)
SERVO ENABLE
17
U22A
R25
1 M
CR13
J1-12
U22C
U20A
R41
1 k
R39
10 k
C57
0.1
C39
0.01
CR26
C52
33
CR38
U20B
C55
0.01
P/O P1
(MATES WITH
A3A1P1 AND
COMMON TO
A3A3A1J1)
FAULT TIMER
FAULT
OVERVOLTAGE
DETECTOR
SPARE
32
31
G(3)

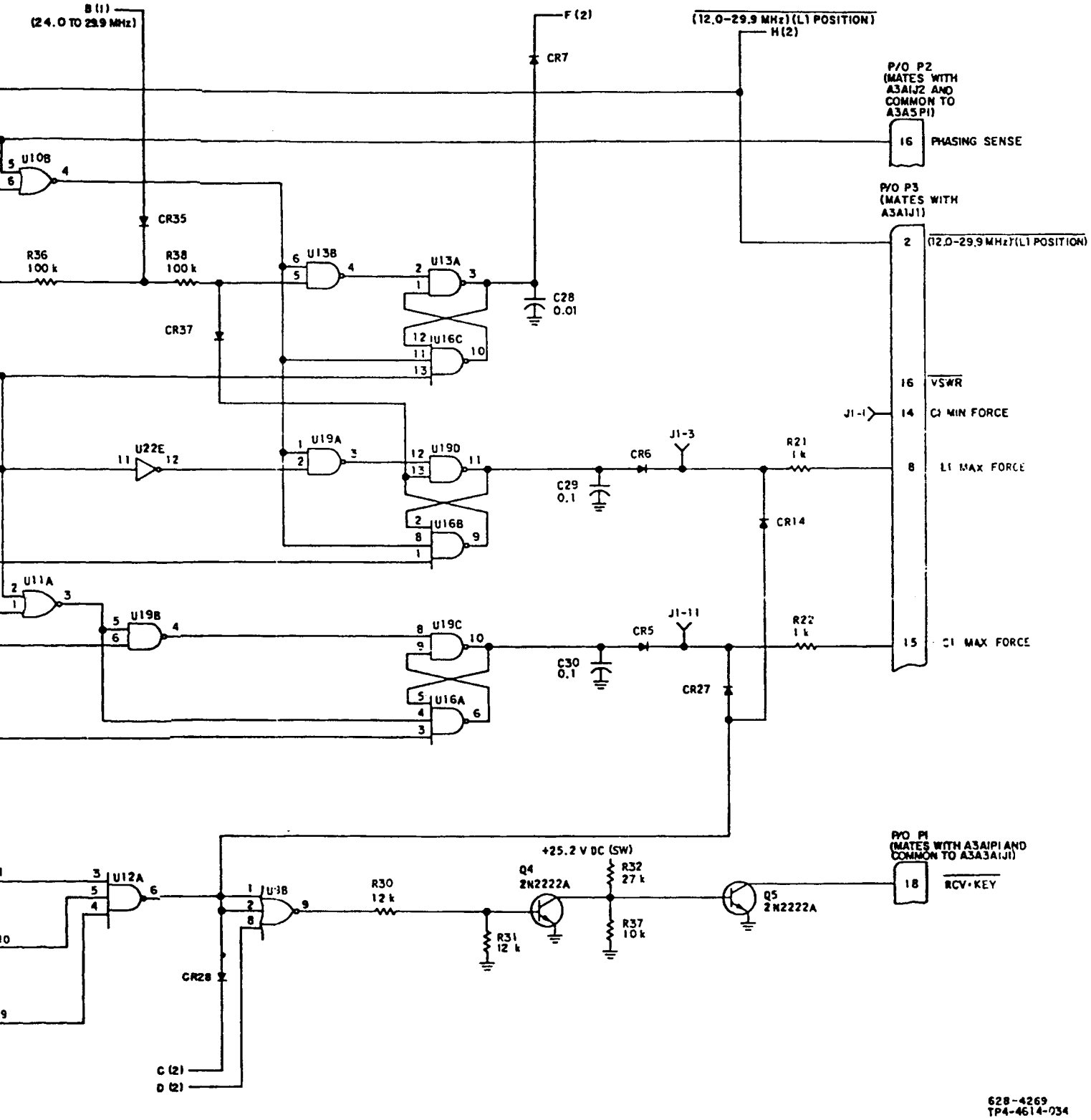


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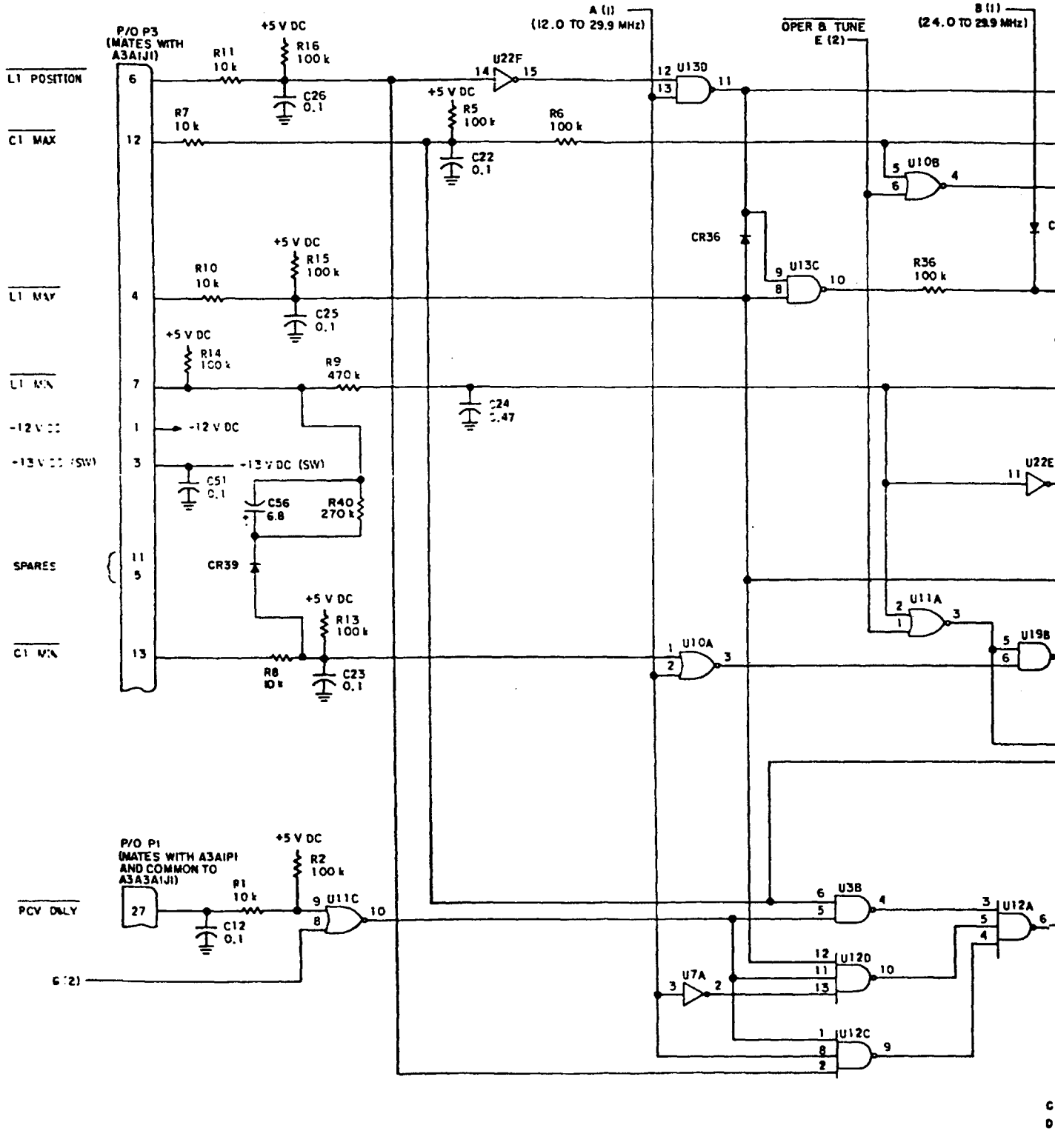
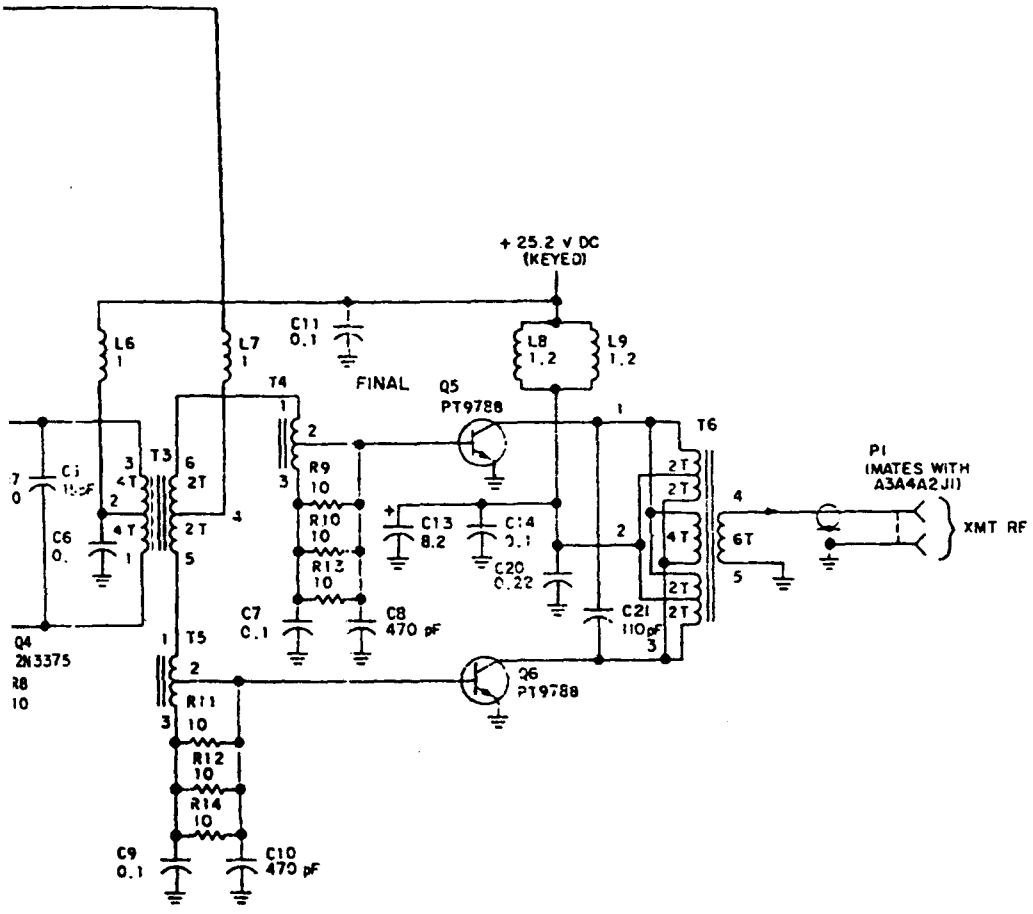
Figure 4-17. Control Logic A3A2 Schematic Diagram (Sheet 3)


P/O P3
(MATES WITH
A3A1J1)
+5 V DC
R11
10 k
R16
100 k
C26
0.1
U22F
14
15
A (1)
(12.0 TO 29.9 MHz)
12 U13D
13
11
OPER B TUNE
E (2)
B (1)
(24.0 TO 29.9 MHz)
L1 POSITION
6
R7
10 k
C1 MAX
12
+5 V DC
R5
100 k
R6
100 k
C22
0.1
5 U10B
6
4
CR36
+5 V DC
R10
10 k
R15
100 k
9 U13C
8
10
R36
100 k
L1 MAX
4
C25
0.1
+5 V DC
R14
100 k
R9
470 k
L1 MIN
7
C24
0.47
-12 V DC
1
-12 V DC
-13 V DC (SW)
3
-13 V DC (SW)
C51
0.1
C56
6.8
R40
270 k
U22E
11
SPARES
11
5
CR39
+5 V DC
R13
100 k
2 U11A
1
3
C1 MIN
13
R8
10 k
C23
0.1
1 U10A
2
3
5 U19B
6
P/O P1
(MATES WITH A3A1P1
AND COMMON TO
A3A3A1J1)
+5 V DC
R2
100 k
R1
10 k
PCV DLY
27
C12
0.1
9 U11C
8
10
6 U3B
5
4
3 U12A
5
4
6
12
11
U12D
10
13
G (2)
3 U7A 2
1
U12C
8
9
2



NOTES:

(1) UNLESS OTHERWISE SPECIFIED, RESISTANCE VALUES ARE IN OHMS, CAPACITANCE VALUES ARE IN MICROFARADS, AND INDUCTANCE VALUES ARE IN MICROHENRYS.

(2) PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION, PREFIX WITH UNIT AND/OR ASSEMBLY DESIGNATION.

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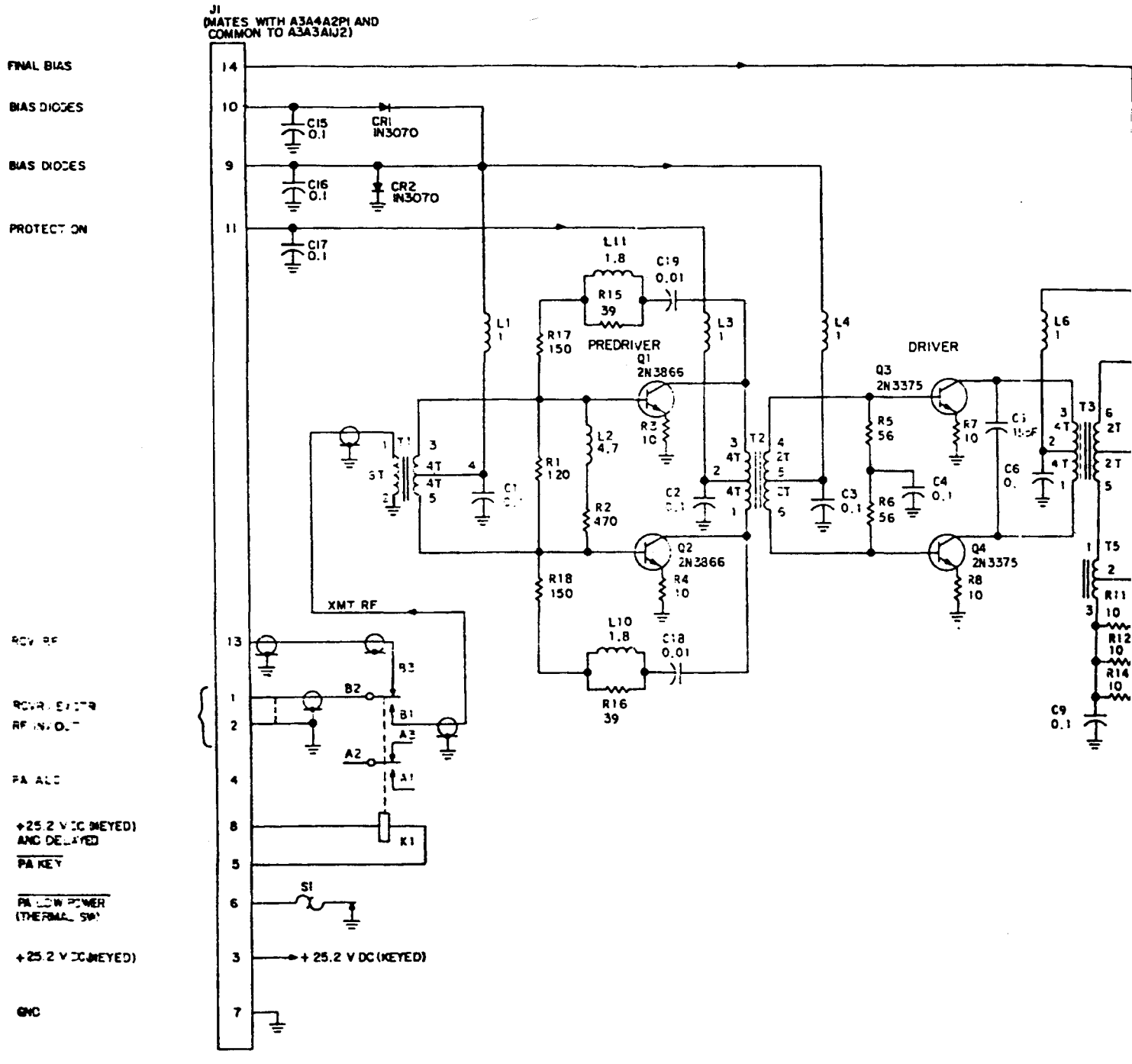
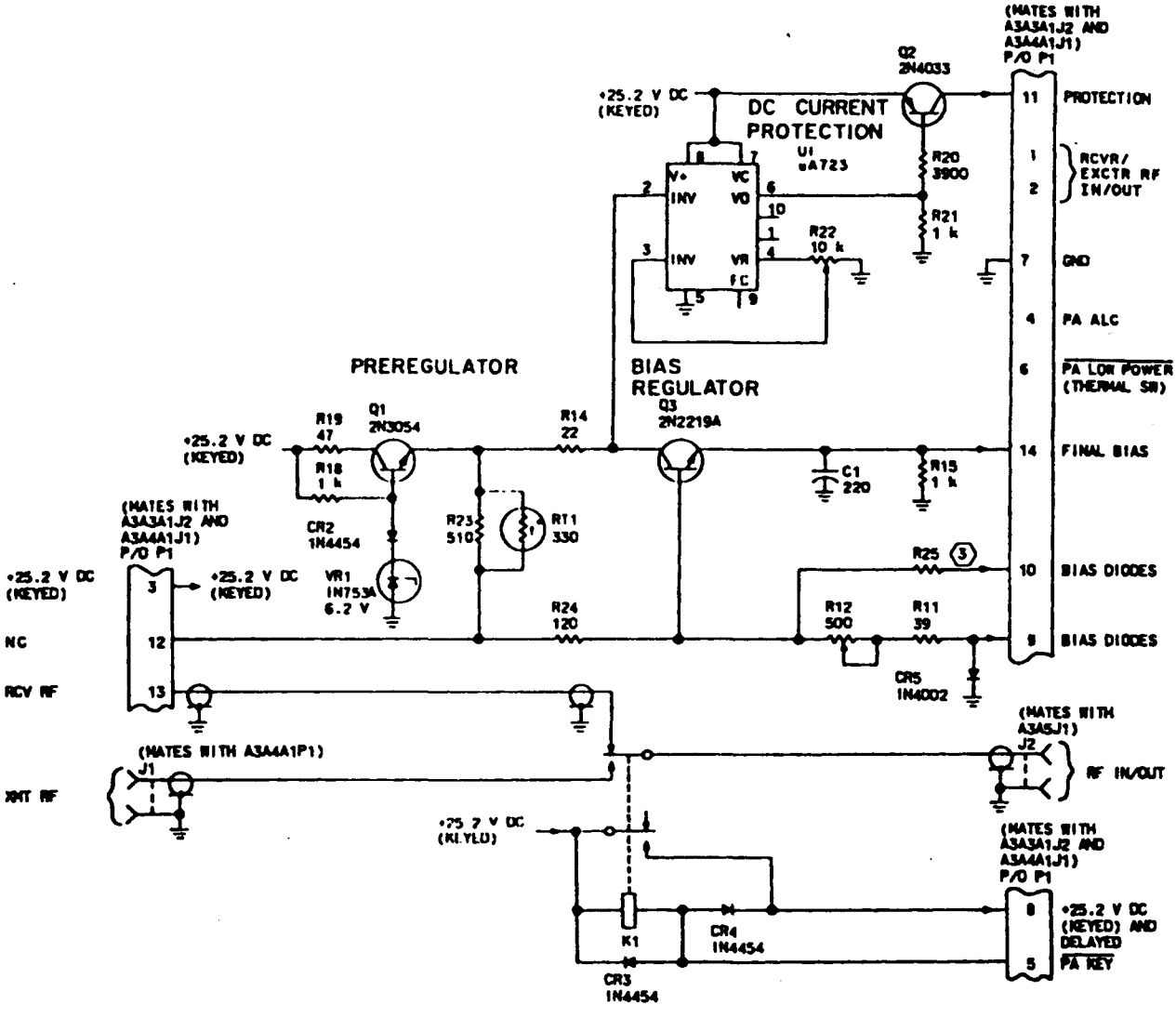
Figure 4-18. RF Subassembly A3A4A1, Schematic Diagram



HIGHEST REFERENCE DESIGNATION			
R17	C16	CR4	L12
Q6	T6	K1	S1

REFERENCE DESIGNATION NOT USED			
R13, R14	CR3		
R15, R16			



NOTES:

(1) UNLESS OTHERWISE SPECIFIED: RESISTANCE VALUES ARE IN OHMS AND CAPACITANCE VALUES ARE IN MICROFARADS.

(2) PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION, PREFIX WITH UNIT AND/OR ASSEMBLY DESIGNATION.

(3) R25 IS A TEST SELECT, MAY BE 0, 3.3 OR 4.7 OHMS.

Figure 4-19. Bias/Control A3A4A2, Schematic Diagram

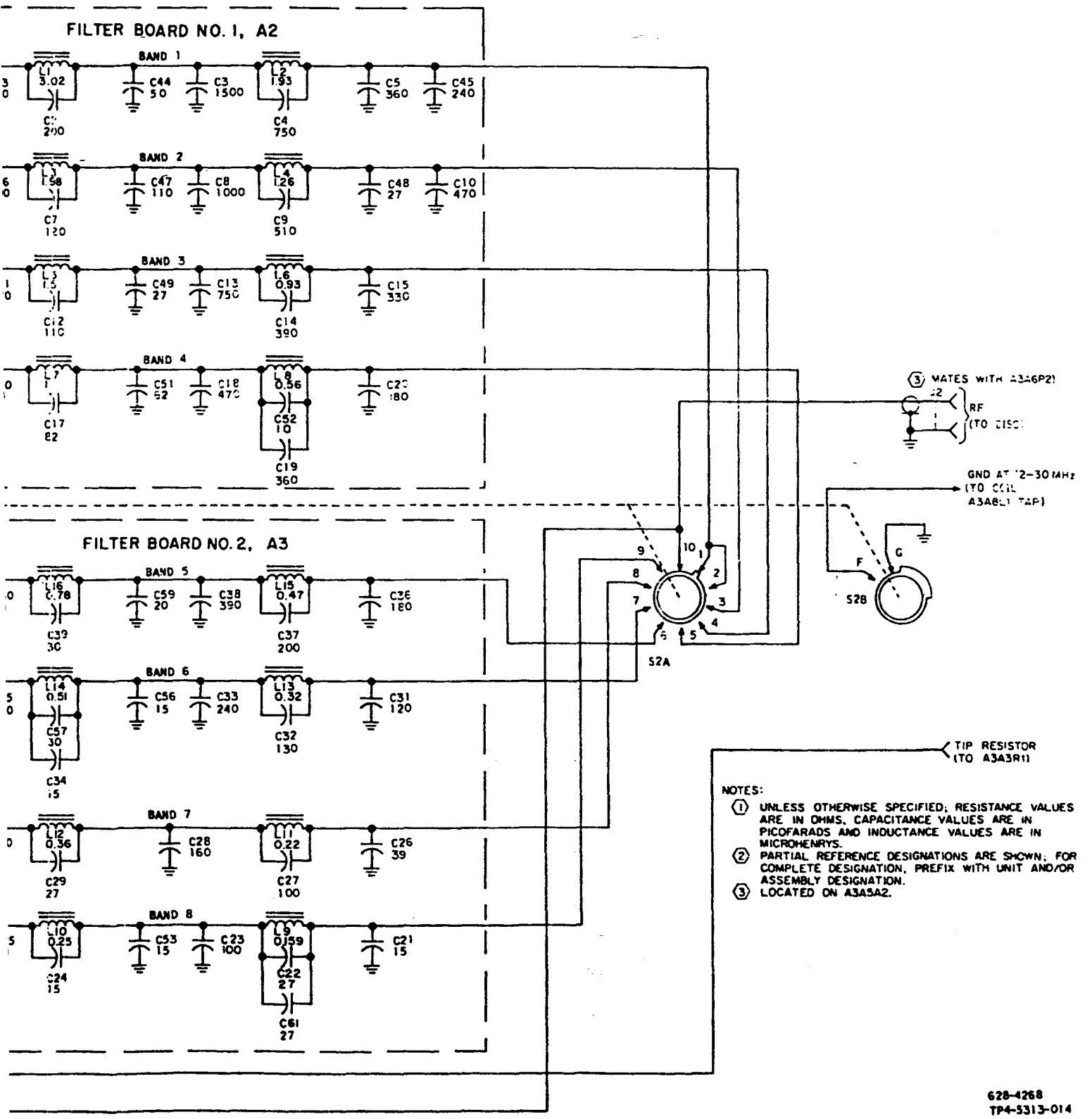
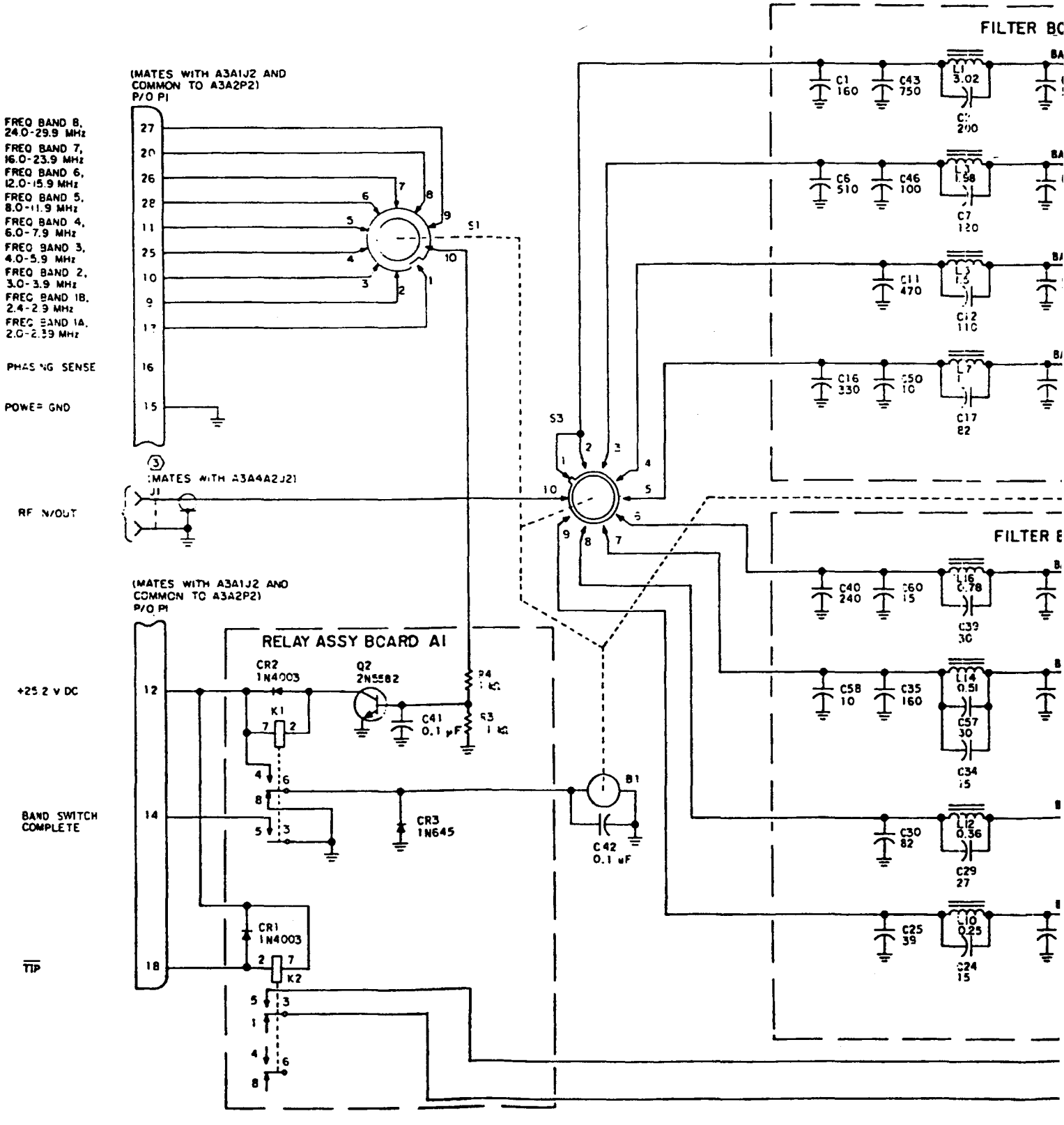
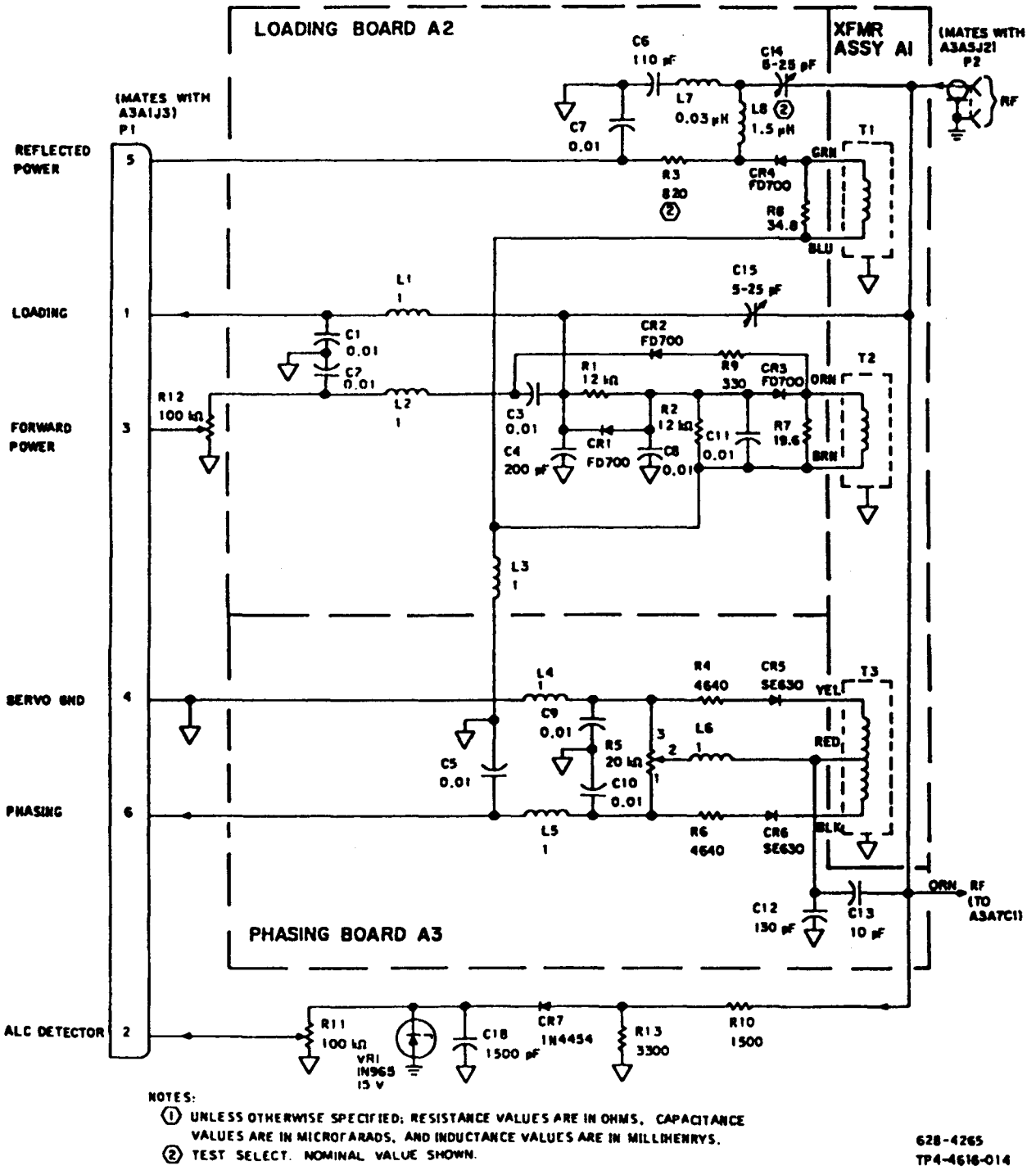


Figure 4-20. Bandswitch A3A5, Schematic Diagram


FILTER BC
(MATES WITH A3A1J2 AND COMMON TO A3A2P2) P/O P1
FREQ BAND 8, 24.0-29.9 MHz
FREQ BAND 7, 16.0-23.9 MHz
FREQ BAND 6, 12.0-15.9 MHz
FREQ BAND 5, 8.0-11.9 MHz
FREQ BAND 4, 6.0-7.9 MHz
FREQ BAND 3, 4.0-5.9 MHz
FREQ BAND 2, 3.0-3.9 MHz
FREQ BAND 1B, 2.4-2.9 MHz
FREQ BAND 1A, 2.0-2.39 MHz
PHASING SENSE
POWER GND
27
20
26
28
11
25
10
9
17
16
15
S1
S3
C1 160
C43 750
L1 3.02
C2 290
C6 510
C46 100
L3 1.98
C7 120
C11 470
L5
C12 110
C16 330
C50 10
L7
C17 82
(3)
(MATES WITH A3A4A2J21)
J1
RF IN/OUT
FILTER E
C40 240
C60 15
L16 0.78
C39 30
C58 10
C35 160
L14 0.51
C57 30
C34 15
C30 82
L12 0.36
C29 27
C25 39
L10 0.25
C24 15
(MATES WITH A3A1J2 AND COMMON TO A3A2P2) P/O P1
RELAY ASSY BOARD A1
+25.2 V DC
BAND SWITCH COMPLETE
TIP
12
14
18
CR2 1N4003
Q2 2N5582
K1
C41 0.1 μF
R3 1 KΩ
CR3 1N645
B1
C42 0.1 μF
CR1 1N4003
K2



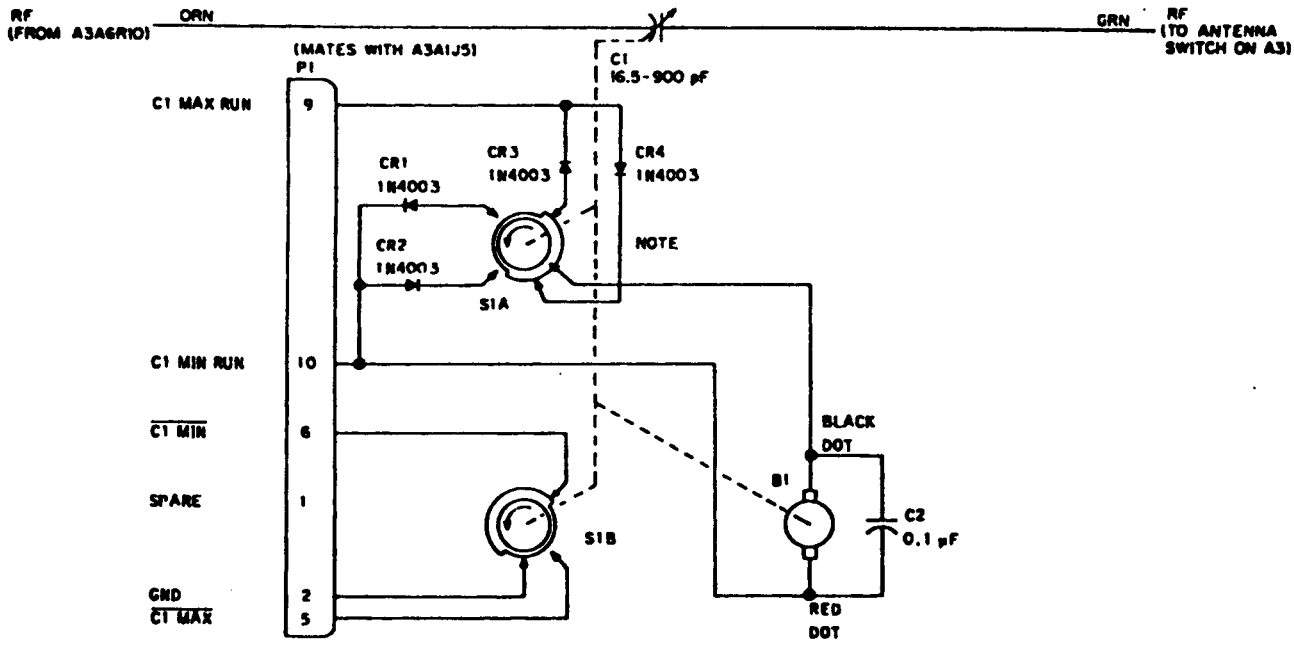
NOTES:

① UNLESS OTHERWISE SPECIFIED; RESISTANCE VALUES ARE IN OHMS, CAPACITANCE VALUES ARE IN MICROFARADS, AND INDUCTANCE VALUES ARE IN MILLIHENRYS.

② TEST SELECT. NOMINAL VALUE SHOWN.

628-4265
TP4-4616-014

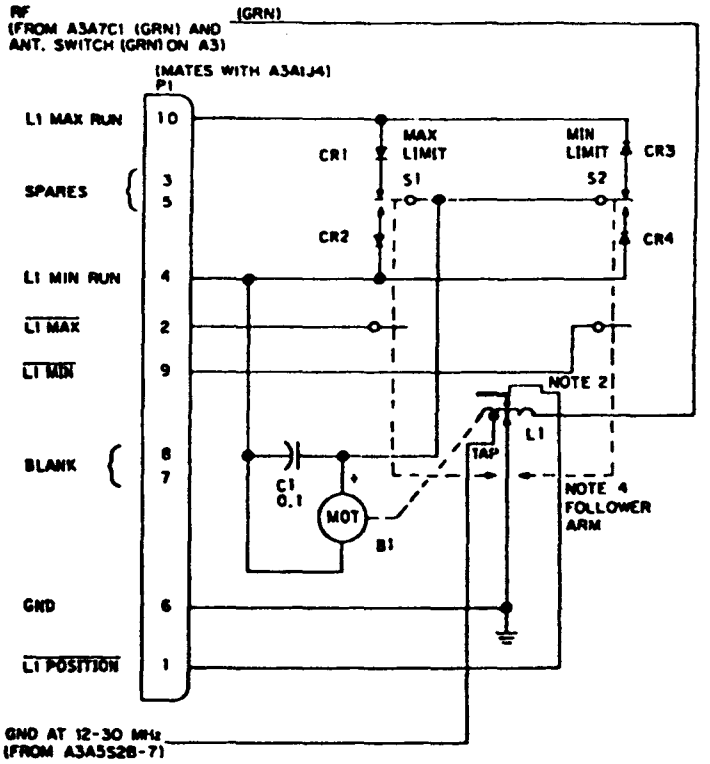
Figure 4-21. Discriminator A3A6, Schematic Diagram



NOTE:
S1A CONTACT GOING TO CR3 IS OPEN AT MINIMUM. S1A CONTACT GOING TO CR4 IS OPEN AT MAXIMUM. ARROW IN SWITCH INDICATES DIRECTION TO MAXIMUM.

628-4256
TP4-4617-013

Figure 4-22. Tuning Capacitor A3A7, Schematic Diagram



NOTES:

1. UNLESS OTHERWISE NOTED, DIODES ARE IN4003.
2. THE FOLLOWER ARM MAKES CONTACT AND GROUNDS THE POSITIONING CONTACT OVER PART OF THE COIL L1.
3. UNLESS OTHERWISE SPECIFIED, RESISTANCE VALUES ARE IN OHMS, CAPACITANCE VALUES ARE IN MICROFARADS, AND INDUCTANCE VALUES ARE IN MICROHENRYS.
4. FOLLOWER ARM ACTUATES S1 AND S2 AND PLACES A GROUND ON ACTUATOR (PIN 2 OR 9).

628-4267
TP4-4682-014

Figure 4-23. Tuning Coil A3A8, Schematic Diagram

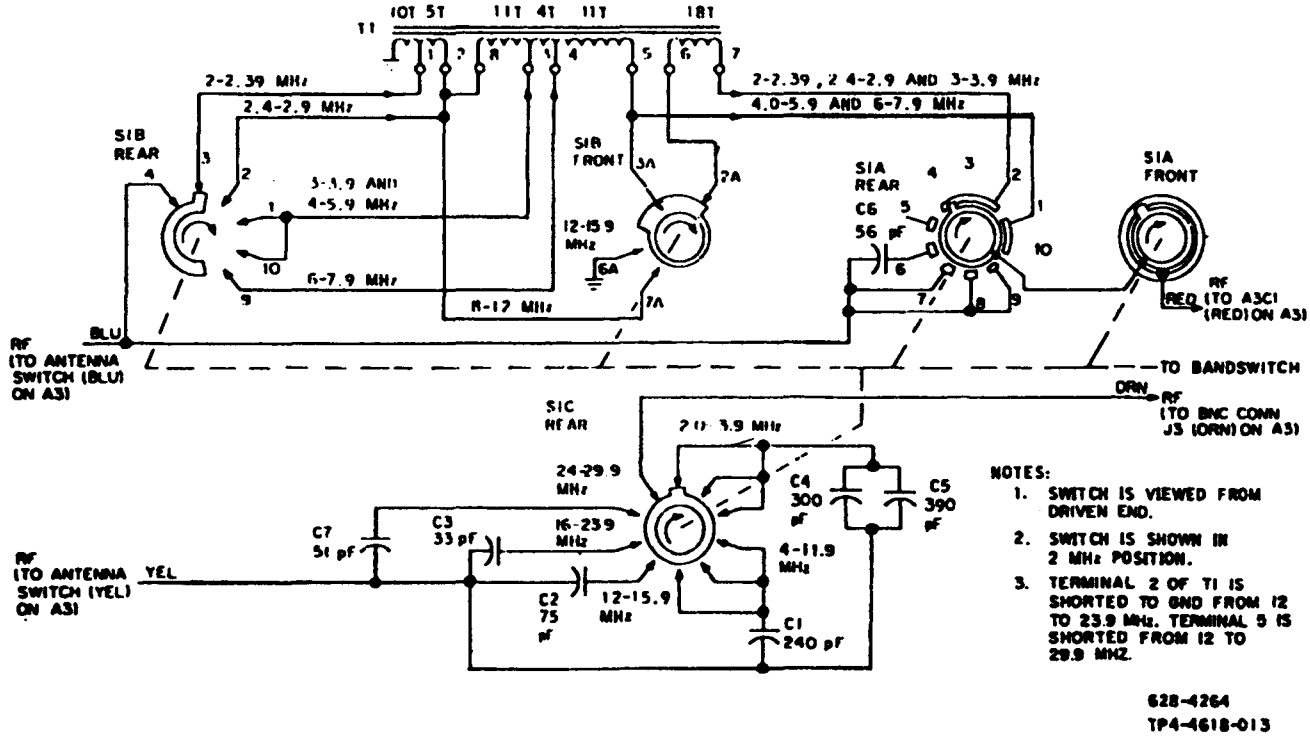


Figure 4-24. Autotransformer A3A9, Schematic Diagram

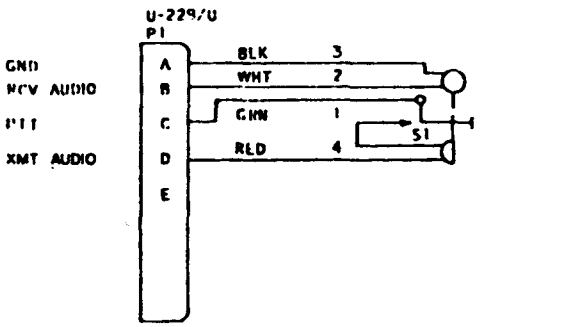


Figure 4-25. Handset H-5017/PRC-515, Schematic Diagram

Missing figures:

4-26

4-27

4-28