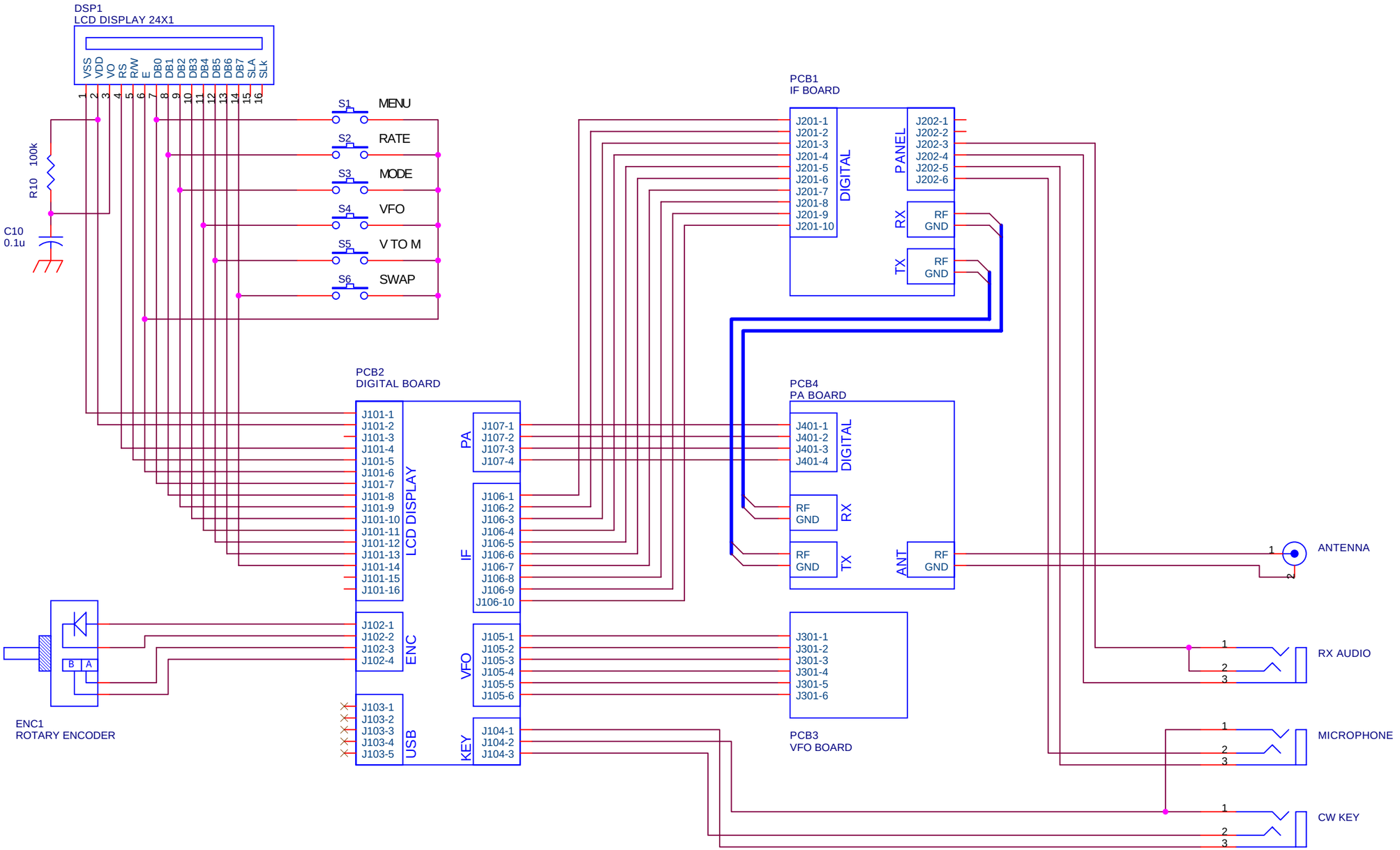


FIGURE 6

Title

**CHASSIS SCHEMATIC DIAGRAM**

| Size | Document Number | Rev |
|---|---|---|
| B | WA2EUJ 40M XCVR - TAK-40 VERSION 1.0 | 1.0 |

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IF BOARD

PA BOARD

12V U108 LM317LZ VIN VOUT ADJ C103 1u R119 560 C106 0.1u VR102 5k R118 100K C104 100p D101 MV209 Y101 4.0MHz R113 100k C102 39p

U104B CD4011B U104D CD4011B U104A CD4011B R120 2.2K L101 10 uH C112 150p C111 0.1u R123 10k R130 10k VCC

J106 10 PIN HEADER 12V GND MIXER1 GND MIXER2 RX/TX* TX/RX* AGC IN TX POWER CW KEY

J107 4 PIN HEADER GND TX POWER RX/TX* TX/RX*

C109 0.1u C115 0.1u R127 1k R126 1k R128 1k R125 1k

74HC125 U107 74HC125 U106

2.2K R131 2.2K R124 C108 0.1u C114 0.1u

J103 5 PIN HEADER USB ADAPTER

R122 10k U102C 74HC14

C105 1u R121 10k R129 10k C110 0.1u

J105 6 PIN HEADER 12V GND LO TUNE LO RANGE LO OUT GND LOCAL OSCILLATOR

MCP4922 U103 Vdd N/C /CS SCK SDI N/C N/C VoutA VrefA Vss VrefB VoutB /SHDN /LDAC R116 130 R117 910

U105 PIC16F871 RC0/T1OSO/T1CKI RC1/T1OSI/CCP2 RC2/CCP1 RC3/SCK/SCL RC4/SDI/SDA RC5/SDO RC6/TX/CK RC7/RX/DT RE2/CS/AN7 RE1/WR/AN6 RE0/RD/AN5 RD0/PSP0 RD1/PSP1 RD2/PSP2 RD3/PSP3 RD4/PSP4 RD5/PSP5 RD6/PSP6 RD7/PSP7 GND GND RA0/AN0 RA1/AN1 RA2/AN2/VREF- RA3/AN3/VREF+ RA4/T0CKI RA5/AN4/SS RB0/INT RB1 RB2 RB3/PGM RB4 RB5 RB6/PGC RB7/PGD OSC1/CLKIN OSC2/CLKOUT MCLR/VPP/THV VDD VDD

J101 16 PIN HEADER LCD DISPLAY AND FP SWITCHES VR101 1k R109 22 R101 10k R102 10k R103 10k R104 10k R105 10k R106 10k R107 10k R108 10k

OSC101 ACH-20.000MHZ-EK OUT VCC GND C113 0.1u C107 0.1u

U101 LM7805C IN GND OUT C101 1u

U102A 74HC14 U102B 74HC14

J102 4 PIN HEADER VCC LED A B OPTICAL ENCODER

J104 3 PIN HEADER DIT DAH/PTT GND MIC/CW KEY

R115 1k R114 1k R110 22k R111 22k R112 1k

FIGURE 2

Title

**DIGITAL BOARD SCHEMATIC DIAGRAM**

| Size | Document Number | Rev |
|---|---|---|
| B | WA2EUJ 40M XCVR - TAK-40 VERSION 1.0 | 1.0 |

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PRIMARY - 12 Turns #30 enameled wire bifilar wound
SECONDARY - 8 trums #30 enameled wire

USE SHIELDED WIRE

DIGITAL BOARD

FRONT PANEL

# FIGURE 3

**DIGITAL BOARD SCHEMATIC DIAGRAM**

| Size | Document Number | Rev |
|---|---|---|
| C | WA2EUJ 40M XCVR - TAK-40 VERSION 1.0 | 1.0 |

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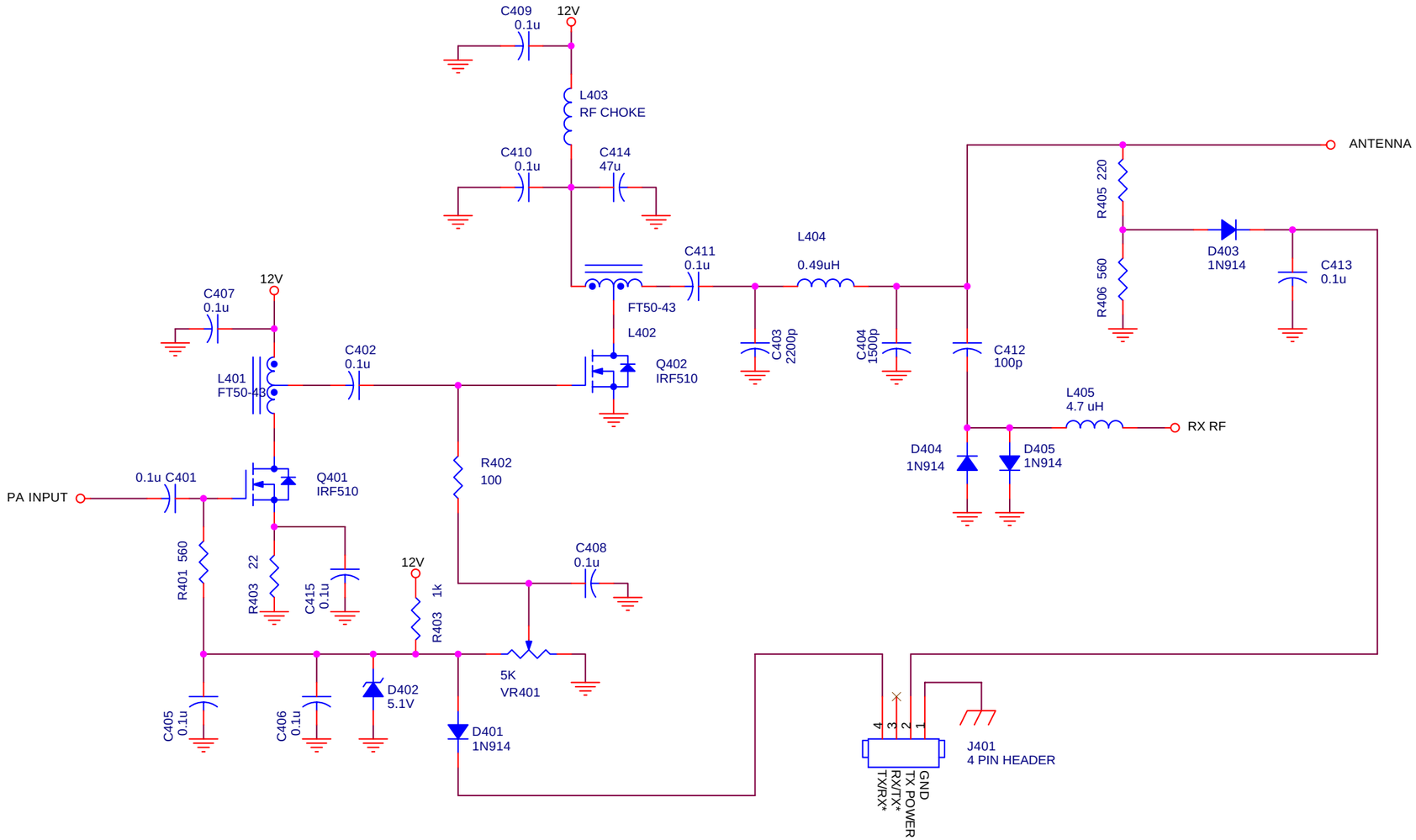


NOTES -

L401, L402 - 16 Turns #26 Bifilar Enameled wire on a FT50-43 core.
Twist bifilar wire 8~10 turns per inch

L403 - As many turns as possible #26 Enameled wire on a FT50-43 core.
Single layer.

L404 - 10 Turns #22 Enameled wire on a T50-2 core.

FIGURE 5

Title
**POWER AMP BOARD SCHEMATIC DIAGRAM**

| Size | Document Number | Rev |
|---|---|---|
| B | WA2EUJ 40M XCVR - TAK-40 VERSION 1.0 | 1.0 |

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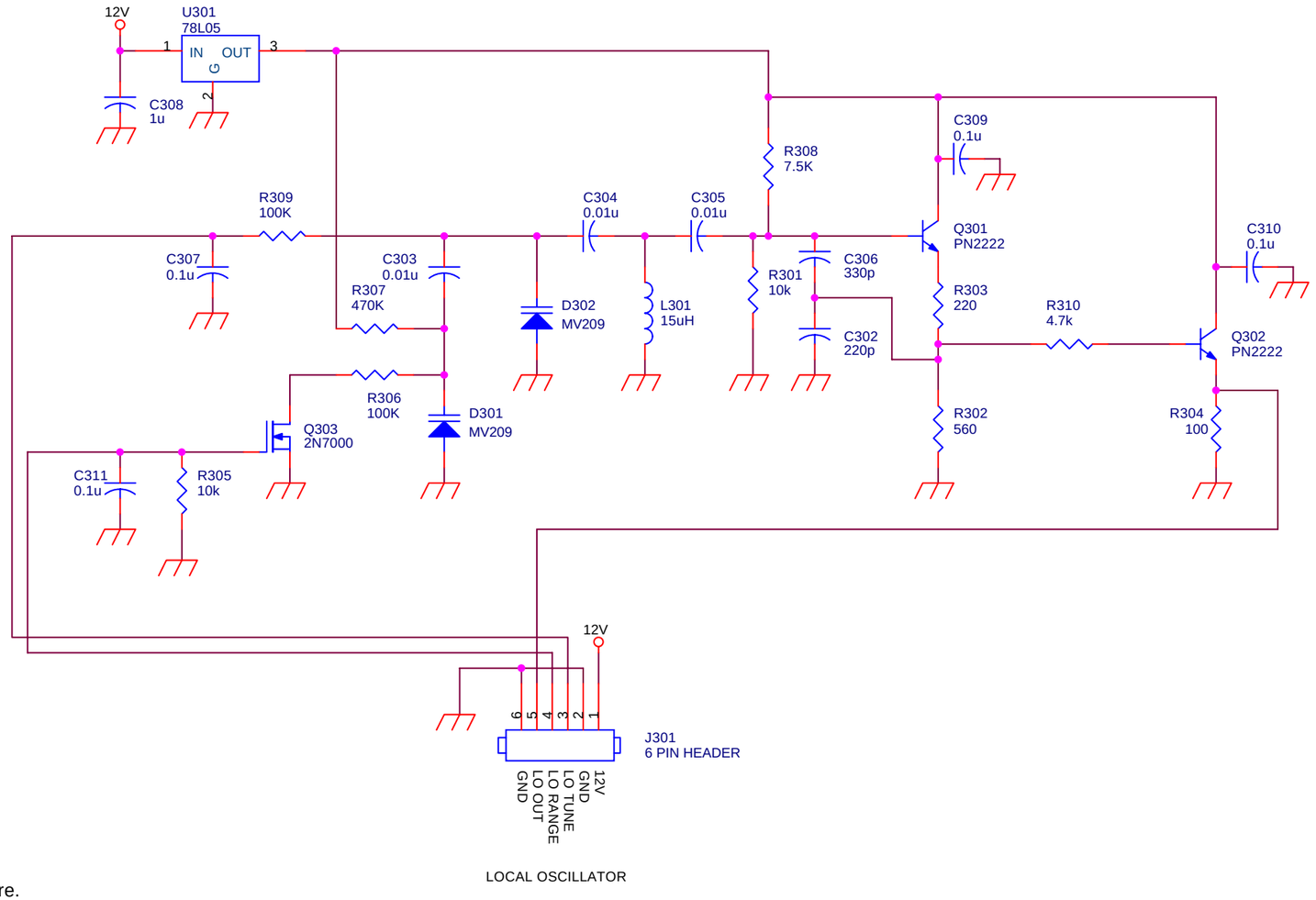


LOCAL OSCILLATOR

NOTES -

L1 - 52 Turns #26 Enameled wire on a T50-2 core. Set Vtune to 1 volt and remove turns until output frequency is between 3.08 and 3.14 MHz.

Use NPO capacitors for C7, C9 and C16.

Assemble the circuit so that the components are rigid with good mechanical stability.

FIGURE 4

Title
**VFO BOARD SCHEMATIC DIAGRAM**

| Size | Document Number | Rev |
|---|---|---|
| B | WA2EUJ 40M XCVR - TAK-40 VERSION 1.0 | 1.0 |

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