PUBLICATION NUMBER: 10215-0022B
JULY 1989

HARRIS

RF COMMUNICATIONS

R-2368/URR
RADIO RECEIVER

INSTRUCTION MANUAL

PUBLICATION NUMBER: 10215-0022B
JULY 1989

R-2368/URR
RADIO RECEIVER

INSTRUCTION MANUAL

HARRIS

HARRIS CORPORATION RF COMMUNICATIONS GROUP
1680 University Avenue Rochester, New York 14610 USA
Tel.: 716-244-5830 Fax.: 716-244-2917, 716-325-1572 • TELEX: 240313 RFCOM UR

Equipment manufactured by Harris Corporation, RF Communications Group meets stringent quality and safety standards. However, high voltages are present in many radio products, and only a skilled technician should attempt to remove outer covers and make adjustments or repairs. All personnel who operate and maintain the equipment should be familiar with this page as a safety preparedness measure. Although this procedure is reproduced as a service to the personnel involved with this equipment, Harris Corporation assumes no liability regarding any injuries incurred during the operation and repair of such equipment, or the administration of this suggested procedure.

ELECTRICAL SHOCK: EMERGENCY PROCEDURE

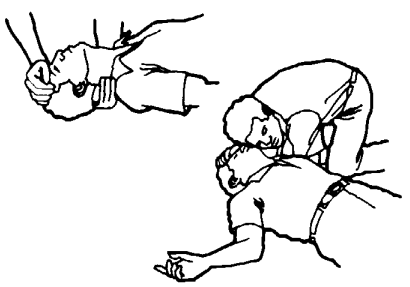
The victim will appear unconscious and may not be breathing. If the victim is still in contact with the voltage source, disconnect the power source in a manner safe to you, or remove the victim from the source with an insulated aid (wooden pole or rope). Next, determine if the victim is breathing and has a pulse. If there is a pulse but no breathing, administer artificial respiration. If there is no pulse and no breathing, perform CPR (if you have been trained to do so). If you have not been trained to perform CPR, administer artificial respiration anyway. Never give fluids to an unconscious person.

WHEN BREATHING STOPS

FIRST, send someone to get a **DOCTOR**.
THEN, administer first aid to restore breathing (artificial respiration):

1 IF A VICTIM APPEARS TO BE UNCONSCIOUS

TAP VICTIM ON THE SHOULDER AND SHOUT, "ARE YOU OKAY?"

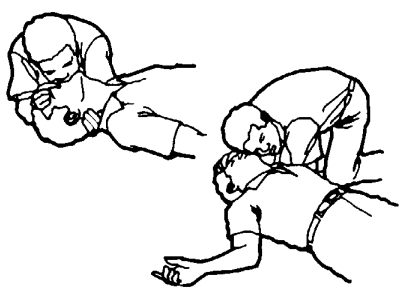


2 IF THERE IS NO RESPONSE

TILT THE VICTIM'S HEAD, CHIN POINTING UP. Place one hand under the victim's neck and gently lift. At the same time, push with the other hand on the victim's forehead. This will move the tongue away from the back of the throat to open the airway.

IMMEDIATELY LOOK, LISTEN, AND FEEL FOR AIR.

While maintaining the backward head tilt position, place your cheek and ear close to the victim's mouth and nose. Look for the chest to rise and fall while you listen and feel for the return of air. Check for about five seconds.



3 IF THE VICTIM IS NOT BREATHING

GIVE FOUR QUICK BREATHS.

Maintain the backward head tilt, pinch the victim's nose with the hand that is on the victim's forehead to prevent leakage of air, open your mouth wide, take a deep breath, seal your mouth around the victim's mouth, and blow into the victim's mouth with four quick but full breaths just as fast as you can. When blowing, use only enough time between breaths to lift your head slightly for better inhalation.

If you do not get an air exchange when you blow, it may help to reposition the head and try again.

AGAIN, LOOK, LISTEN, AND FEEL FOR AIR EXCHANGE.

4 IF THERE IS STILL NO BREATHING

CHANGE RATE TO ONE BREATH EVERY FIVE SECONDS.

For more information about these and other life-saving techniques, contact your Red Cross chapter for training.
"When Breathing Stops" reproduced with permission from an American Red Cross Poster

TABLE OF CONTENTS

Paragraph		Page
	Specifications	viii
	About This Manual	xi
	SECTION 1 - INTRODUCTION	
1.1	Introduction	1-1
1.2	General Description	1-1
1.3	Receiver Features	1-3
1.4	Compatibility	1-3
1.5	Customer Options	1-4
1.6	Specialized Requirements	1-5
	SECTION 2 - INSTALLATION	
2.1	Introduction	2-1
2.2	Unpacking and Inspection	2-1
2.3	Ancillary Kit	2-1
2.4	Site Selection	2-1
2.4.1	Antennas	2-2
2.5	Mechanical Installation	2-2
2.6	Power Requirements	2-2
2.7	Input/Output Connections	2-4
2.8	Initial Setup and Adjustments	2-4
2.8.1	Memory Backup Battery	2-8
2.8.2	Remote Control Interface Setup	2-8
2.8.3	USB, LSB and ISB Line Audio Output Level Adjust	2-10
2.8.4	Adjusting Front Panel Display Brightness	2-11
2.9	Functional Checkout Procedure	2-11
2.9.1	Receive Mode Test	2-11
2.9.1.1	Frequency Entry	2-11
2.9.1.2	Tune Rate	2-12
2.9.1.3	Mode Selection	2-12
2.9.1.4	Bandwidth Selection	2-12
2.9.1.5	AGC Selection	2-12
2.9.1.6	BFO Selection	2-12
2.9.1.7	RF Gain	2-13
2.9.1.8	AF Gain	2-13
2.9.1.9	Load Memory Function	2-13
2.9.1.10	Channelized Reception	2-14
2.9.1.11	Local/Remote Switch	2-14
2.9.1.12	Meter Switch	2-14
2.9.1.13	COR Control	2-15
2.9.2	Program Mode	2-15
2.9.2.1	Recall Memory Function	2-15
2.9.2.2	Program Group Function	2-15
2.9.3	Scan Mode Test	2-15
2.9.3.1	Channel Scan	2-16

TABLE OF CONTENTS (Cont.)

Paragraph		Page
	SECTION 2 - INSTALLATION (Cont.)	
2.9.3.2	Group Scan	2-16
2.9.4	Self-Test (BITE)	2-16
2.9.5	Reconnection	2-16
	SECTION 3 - OPERATION	
3.1	Introduction	3-1
3.2	Controls and Indicators	3-1
3.2.1	Power, AF Gain, RF Gain, and COR	3-1
3.2.2	Tuning Wheel and Keypad Entries for Channel, Frequency, BFO, and Group	3-1
3.2.3	AGC, Mode, BW, and Dwell	3-4
3.2.4	TEST, RECALL, LOCAL, PROG, SCAN, and RCV Controls	3-6
3.2.5	Front Panel Meter	3-7
3.2.6	Remote, Fault, and NB (Noise Blanker)	3-8
3.3	Power Up	3-9
3.4	Receiver (Non-Channelized) Operation	3-9
3.4.1	Operating Procedure	3-9
3.5	Programming the Receiver for Channelized Operation	3-10
3.5.1	Channel Programming Procedure	3-10
3.5.2	Group Programming Procedure	3-12
3.5.3	Entering Auxiliary Channel Procedure	3-12
3.6	Programmed Receiver Operation	3-14
3.6.1	Standard (Non-scanning) Channelized Operation	3-14
3.6.2	Automatic Scanning	3-14
3.6.2.1	Channel Scanning Procedure	3-14
3.6.2.2	Group Scanning Setup Procedure	3-15
3.6.2.3	Terminating the Scan Function	3-15
3.7	Remote Operation	3-15
	SECTION 4 - TECHNICAL DESCRIPTION	
4.1	Introduction	4-1
4.2	Receiver Operation	4-1
4.2.1	Receiver Signal Path	4-1
4.2.1.1	Preselector Assembly A19 and Input Filter Assembly A1	4-2
4.2.1.2	First Converter Assembly A2	4-2
4.2.1.3	Second Converter Assembly A3	4-2
4.2.1.4	IF Filter Assembly A4	4-2
4.2.1.5	IF/Audio Assembly A5	4-6
4.2.1.6	ISB IF/Audio Assembly A18	4-6
4.2.1.7	Meter Board A13A3	4-6
4.2.2	Synthesizer BFO, Front Panel, and Control Assemblies	4-7
4.2.3	Frequency Synthesizer Assembly A10	4-7
4.2.4	BFO Assembly A12	4-7
4.2.5	Control PWB Assembly A14	4-7
4.3	Conversion Between dBm and Vrms	4-7

TABLE OF CONTENTS (Cont.)

Paragraph		Page
	SECTION 5 - MAINTENANCE	
5.1	Introduction	5-1
5.2	PWB Repairs	5-1
5.3	MOSFET Replacement	5-1
5.4	CMOS Handling and Replacement	5-2
5.5	Built-In Test Equipment (BITE) Self-Diagnostics	5-2
5.5.1	Continuous Self-Test Monitoring	5-5
5.5.2	Self-Diagnostic Operation	5-5
5.5.2.1	Lamp Test	5-5
5.5.2.2	ROM Test (Assembly A14)	5-5
5.5.2.3	RAM Test (Assembly A14)	5-5
5.5.2.4	I/O Port Tests	5-5
5.5.2.5	Serial Data Test	5-6
5.5.2.6	Reference Generator Test (Assembly A12)	5-6
5.5.2.7	A/D Converter Tests	5-6
5.5.2.8	Phase Locked Loop (PLL) Tests	5-6
5.5.2.9	Input Filter Test (Assembly A1)	5-6
5.5.2.10	First Converter Test (Assembly A2)	5-7
5.5.2.11	Second Converter Test (Assembly A3)	5-7
5.5.2.12	IF Filter Test (Assembly A4)	5-7
5.5.2.13	IF Audio Test (Assembly A5)	5-8
5.5.2.14	ISB IF/Audio Test (Assembly A18)	5-9
5.5.2.15	LCU Test (Optional Assembly A17, If Installed)	5-9
5.5.3	Self-Diagnostics Sequence Summary	5-10
5.6	Supplement to Built-In Test Capabilities	5-13
5.6.1	Abnormal Front Panel Displays	5-13
5.6.2	Abnormal Operation, But With No Built-In Test Failure	5-13
5.6.3	Fault Indications With Multiple Causes	5-14
5.7	Receiver Performance Test Procedures	5-15
5.7.1	Sensitivity Test	5-16
5.7.2	Audio Output Level and Distortion Test	5-17
5.7.2.1	Line Output Check	5-18
5.7.2.2	Headphone Output Check	5-19
5.7.3	AGC Range	5-19
5.7.4	IF Filter Selectivity	5-20
	MAIN CHASSIS INTERCONNECTION	
	A1 INPUT FILTER ASSEMBLY	
	A2 FIRST CONVERTER ASSEMBLY	
	A3 SECOND CONVERTER ASSEMBLY	
	A4 IF FILTER ASSEMBLY	
	A5 IF/AUDIO PWB ASSEMBLY	

TABLE OF CONTENTS (Cont.)

Paragraph — Page

A10 SYNTHESIZER ASSEMBLY

A11 BFO ASSEMBLY

A12/A21 REFERENCE GENERATOR ASSEMBLY

A13 FRONT PANEL ASSEMBLY

A14 CONTROL BOARD ASSEMBLY

A15 POWER SUPPLY ASSEMBLY

A16 POWER DISTRIBUTION ASSEMBLIES

A18 ISB IF/AUDIO ASSEMBLY

A19 PRESELECTOR ASSEMBLY

A25 EMP/EMI SUPPRESSION ASSEMBLY

APPENDIX

LIST OF FIGURES

Figure		Page
Frontispiece	Receiver	
1-1	Typical Receiver Applications	1-2
2-1	Typical Doublet Antenna Installation	2-3
2-2	Desk Mount Dimensions	2-5
2-3	Rack Mounting Details	2-6
2-4	Rear Panel	2-7
2-5	Functional Test Setup	2-11
3-1	Power ON/OFF, AF Gain, RF Gain, and COR	3-2
3-2	Channel, Frequency, BFO, and Group Display Entries	3-3
3-3	AGC, Mode, BW, and Dwell Displays and Controls	3-5
3-4	Speaker, Test, Recall, Load, Program, Scan and Receive Control	3-6
3-5	Front Panel Meter and Controls	3-7
3-6	Remote, Fault and Noise blanker (NB) Controls and Indicators	3-8
4-1	Receiver Signal Path Block Diagram	4-3
4-2	Receiver Gain Distribution	4-5
5-1	Sensitivity Test Setup	5-16
5-2	Line Audio Test Setup	5-18
5-3	Phone Audio Test Setup	5-19
5-4	AGC Range Test Setup	5-20
5-5	IF Filter Selectivity Test Setup	5-20

LIST OF TABLES

Table		Page
1-1	Optional Equipment	1-4
2-1	Ancillary Kit (P/N 10215-0021)	2-1
2-2	Calculation of Doublet Antenna Element Lengths	2-4
2-3	Rear Panel Connector J7	2-8
2-4	Remote Control Interface Configuration Switch Setting	2-9
2-5	Serial Interface Baud Rate Switch Settings	2-10
2-6	ID Number Switch Weights	2-10
2-7	Typical Filter Complement	2-12
2-8	Programmed Channels	2-13
4-1	Conversion of dBm to Vrms across 50 ohms (0 dBm = 1 mWatt)	4-8
5-1	Fault Code Listing	5-3
5-2	BFO Tuning Range	5-6
5-3	AM and SSB Test Results and Fault Locations	5-9
5-4	Self-Diagnostics Sequence Summary	5-10
5-5	Test Procedures	5-16
5-6	Sensitivity Test Reports	5-17
5-7	Audio Output Level and Distortion Test Report	5-18
5-8	IF Filter Response Test Report	5-21

SPECIFICATIONS FOR LF/MF/HF SYNTHESIZED RECEIVER

Frequency Range:	14 kHz to 29.999999 MHz
Frequency Resolution:	1 Hz increments standard
Tuning:	Continuous via tuning wheel in seven selectable rates or direct entry via keypad.
Tuning Time:	Tuning time between any two frequencies is less than 20 msec.
Frequency Stability - Internal:	± 0.5 part in 10^7-Standard
FREQUENCY STANDARD I/O	
Input:	1 MHz, 0 dBm minimum
Output:	1 MHz, 0 dBm minimum
Channel Memory:	100-channel capacity capable of being loaded locally or remotely with complete receiver parameters.
Scanning:	Scan any set of consecutive channel numbers (channel scan) or one of the ten preprogrammed sets of random channel numbers (group scan).
Readout/Display:	Receiver frequency, BFO frequency offset, channel assignment, mode, IF BW/filters, AGC, BITE, dwell, scan group.
BFO:	10 Hz synthesized tuning, ± 9.99 kHz.
Remote Control:	A microprocessor-based system capable of accepting asynchronous serial data in accordance with MIL-STD-188C.
Remote Control Functions:	Frequency, Channel Select, IF BW, Mode, AGC-TC, BFO, Fault-BITE Status, Scan Select, RF/IF Gain, and Channel Load.
Internal Preselector:	Digital Preselector - standard
Maximum Signal Input:	Receiver protected at 25 watts available power input.
Modes of Operation:	CW, 2-ISB, AM, FM, LSB, USB, FSK with external demodulator.
COR:	Carrier Operated Relay

SPECIFICATIONS FOR LF/MF/HF SYNTHESIZED RECEIVER (Cont.)

Sensitivity:	For 10 dB (S + N) ÷ N ratio CW: 0.2 μV (300 Hz) AM: 2.5 μV (6 kHz) SSB: 0.6 μV Note: Below 200 kHz, sensitivity may degrade 14 dB.
IF Bandwidths:	IF Filter: 3 dB BW (kHz) CW: 0.3 AM: 6.0 FM: 16 USB: 2.7 LSB: 2.7
INTERMODULATION	
In-Band:	-40 dB or better for (2) 50 mV (-13 dBm) signals within the IF passband.
Out-of-Band:	-90 dB or better for (2) -20 dBm signals separated 100 kHz or more.
Cross Modulation:	10% or better for a 900 mV (+ 12 dBm) 30% modulated interfering signal removed 100 kHz or greater from the desired signal of 30 uV (-77 dBm).
Reciprocal Mixing:	The apparent noise appearing at the Receiver input when in a 3 kHz bandwidth, caused by a -17 dBm signal 100 kHz off tune, is less than 0.3 uV (-117 dBm).
Quieting Ultimate (S + N) ÷ N:	35 dB.
SPURIOUS RESPONSES	
Image and IF:	-80 dB
Spurious:	Internal -101 dBm equivalent or less, external -80 dB.
AGC	
Range:	≤ 3 dB audio output variation for 2 μV to 200 mV signal range. (Threshold internally adjustable from 1.0 to 5.0 μV).
Time Constants:	3 ranges
Attack Time:	< 20 msec
Decay + Hang Times:	Fast: < 35 msec Medium: 200 ± 50 msec Slow: 2.5 ± .5 sec Manual: 100 dB range

SPECIFICATIONS FOR LF/MF/HF SYNTHESIZED RECEIVER (Cont.)

AUDIO OUTPUTS:	
Phone:	+ 15 dBm/600 ohms/5% distortion
Line Output:	+ 15 dBm/600 ohms/5% distortion
Hum and Noise:	Less than 35 dB
Pass Band Ripple:	3 dB max.
IF Outputs:	455 kHz.
Built-In Test Diagnostics:	Fault isolation to module with front panel alphanumeric indication.
Power Requirements:	115 Vac, 60 Hz, 90 watts
Temperature:	Operating: 0°C to + 50°C Non-Operating: -62°C to + 71°C
Humidity:	0 to 95%
Size:	Rack mount and desk mount capability 5.25 H x 19 W x 19.5 D (behind front panel) in. max. (13.3 H x 48.3 W x 49.5 D cm).
Weight:	40 lbs. (18 kg)

ABOUT THIS MANUAL

This instruction manual is divided into five general information sections (blue tabs), and 16 unit instruction sections (white tabs). Installation, operation, and maintenance procedures as well as a comprehensive technical description are included in the general information tab sections. The 16 unit instruction sections include detailed circuit descriptions, parts lists, component location drawings and schematic diagrams for the sub-assemblies of the Receiver. Data sheets for the integrated circuits used in this Receiver are included in the appendix for the user's convenience.

R-2368/URR
RADIO RECEIVER

INSTRUCTION MANUAL

URR-100P

R-2368/URR Receiver

SECTION 1

INTRODUCTION

1.1 INTRODUCTION

This manual contains information necessary to install, operate, maintain, and repair the Receiver. This manual is subdivided into the following sections.

- Section 1: Introduction. Includes basic description, feature highlights, optional auxiliary equipment, etc.
- Section 2: Installation. Includes site selection, power requirements, mechanical installation, interconnect requirements, initial setup and power on, and functional checkout.
- Section 3: Operation. Includes general operating instructions, control, and indicator descriptions.
- Section 4: Technical Description. Contains general receiver characteristics, receiver block diagram, AGC-gain distribution chart, and signal path and synthesizer functional descriptions.
- Section 5: Maintenance: Contains general repair techniques, component handling techniques, self-test (BITE) descriptions and error code listings, receiver performance test procedures, and component data sheets.
- Unit Instruction: Main Chassis thru A25: These sections include detailed circuit descriptions, component location diagrams, parts lists and schematic diagrams for all subassemblies in the Receiver.

1.2 GENERAL DESCRIPTION

The Receiver is designed to deliver high performance synthesized reception operating in the AM, CW, FM, USB, LSB, and ISB modes tuning to signals from 14 kHz to 29.99999 MHz (in 1 Hz increments) utilizing digital tuning techniques. Up to 100 channels can be programmed for frequency, detection mode, filter bandwidth, AGC mode, and BFO offset, and recalled individually, or scanned sequentially or in groups. The Receiver contains a comprehensive built-in test equipment (BITE) network which allows extensive microprocessor controlled self-testing to isolate faults at the modular level. Typical Receiver applications are illustrated in figure 1-1.

Manual tuning and channel selection is activated via a front panel touch pad or tuning wheel. Operating parameters such as detection mode and filter bandwidth (CW -.3 kHz; AM, 6 kHz; USB/LSB - 2.7 kHz; FM - 16 kHz) and AGC mode (slow, medium, fast, off) are pushbutton selectable. Receiver operating parameters and self-testing results are displayed on two front panel numeric and alphanumeric displays. Full remote control is built-in as a standard feature and is compatible with MIL-STD-188C.

Rear panel connectors include an N type coaxial connector for the RF antenna input and BNC 50-ohm connectors for the following inputs/outputs: filtered 455 kHz IF output, unfiltered 455 kHz DSB output, ISB output, 1 MHz frequency standard input, and frequency standard output. Additionally, other connectors allow access to 600-ohm line audio outputs, remote control inputs and outputs, and other functions (see table 2-3).

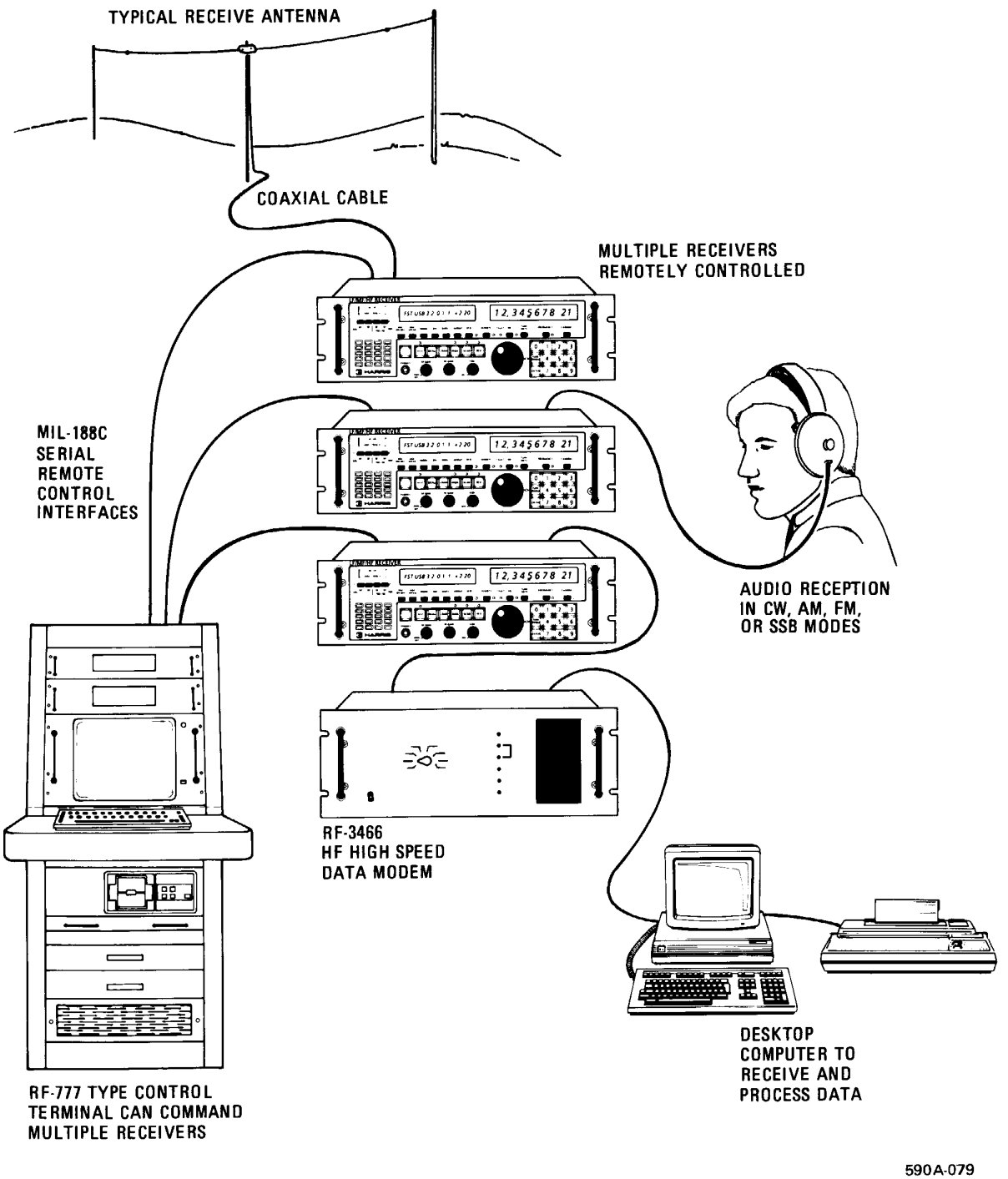


Figure 1-1. Typical Receiver Applications

The Receiver is entirely modular in design to facilitate maintenance. The unit may be rack mounted with the following considerations.

- Dimension - 5.25 H x 19.0 W x 19.5 D (less front panel projections) inches maximum (13.3 H x 48.3 W x 49.5 D cm)
- Weight - 40 pounds (18.1 kg)
- Power requirements - 115 Vac, 60 Hz, 90 watts

Note that a complete listing of all Receiver specifications is included at the front of this manual.

1.3 RECEIVER FEATURES

This high performance Receiver utilizes the latest device technology and circuit design. The microprocessor based architecture allows for a cost effective design with the following versatile features.

- Synthesized digital tuning and readout in 1 Hz steps from 14 kHz to 29.99999 MHz.
- Keyboard control
- Continuous single knob tuning
- Full remote control by digital asynchronous commands with a wide variety of standards and rates.
- Built-in test equipment (BITE) fault isolation to replaceable module level.
- Preset channel memory - Up to 100 front panel programmable channels can be stored in a nonvolatile memory. Frequency and mode are stored in memory for instant recall.
- Channel scanning - Automatically searches programmed channels, with a selectable dwell time.
- Synthesized variable BFO offset - ± 9.99 kHz in 10 Hz steps.
- Diversity capability - With external RF-575 Diversity Combiner.
- Multimode operation - Including USB, LSB, ISB, CW, AM, and FM. (FSK optional.)
- COR (Carrier Operated Relay) - Operated from a front panel control.
- Plug in subassemblies - All subassemblies can be replaced using common hand tools.

1.4 COMPATIBILITY

This Receiver is compatible with the following RF products:

- RF-551A Preselector
- RF-575 Quad Diversity Combiner

- RF-130, RF-1130, RF-755 and RF-765 Transmitters
- RF-7110 Adaptive Controller
- RF-7405 Remote Control
- RF-777 Remote Control

1.5 CUSTOMER OPTIONS

Table 1-1 is a list of optional equipment.

Table 1-1. Optional Equipment

Number	Name	Part No.	Description	Publication No.
RF-518	Earphones	724-0075	For reduction of ambient noise levels or to utilize private listening.	None
RF-567	High Impedance RF Input Transformer	1920-1450	Improves reception when untuned antennas are used.	1920-1452 (Instruction Sheet)
RF-575	Diversity Combiner	7634-0000	Selects audio from the receiver with the strongest signal.	7634-1030
RF-593	High Stability Frequency Option	759-3906	1 MHz frequency standard with proportional temperature control. 1 part in 10^8 stability.	10215-0022 A12/A21 section
RF-594-01	Rack Mount	10073-0055	Includes slides and related hardware for rack mounting applications	10215-0020 (installation section)
RF-594-02	Desk Top Case	10073-0045	Enclosed case for desk top installation.	10215-0020 (installation section)
RF-594-03	Stack Mount	10073-0035	Includes hardware for standard stack mounting applications.	10215-0020 (installation section)
RF-595A-02	Delay Compensated ISB Option	10215-6360	Delay compensated filtering for critical data communications. Provides less than 500 u/sec. differential time delay from 400 Hz to 2900 Hz. Offers less than 2 dB ripple in the 300 Hz to 3 kHz passband.	10215-0018 (supplement)

Table 1-1. Optional Equipment (Cont.)

Number	Name	Part No.	Description	Publication No.
RF-596-01	Half Octave Filter	10073-6410	Offers filtering protection from 2 to 30 MHz in 8 half-octave band filters. Also, for frequencies below 2 MHz, Low Pass filtering is provided	SU-10073-0019-1 (supplement)
RF-597A	Noise Blanker	10215-6800	The Noise Blanker removes impulse type noise from received signals. Adjusts automatically to received signal level changes.	10215-0019 (supplement)
RF-598A	4ISB Option	N/A	Provides simultaneous operation on four independent sidebands.	N/A
RF-651-02	Receiver Multicoupler (2 port)	RF-651-002	Permits operation of two receivers from a common antenna. At the same time, it provides isolation between receivers.	7733-000
RF-651-04	Receiver Multicoupler (4 port)	RF-651-004	Same as RF-651-002, but with 4 ports.	7733-000
RF-651-08	Receiver Multicoupler (8 port)	RF-651-008	Same as RF-651-002, but with 8 ports.	7733-000

1.6 SPECIALIZED REQUIREMENTS

Harris/RF Communications Group Systems Division specializes in translating exacting customer needs into complete systems packages. Contact the following for specialized requirements.

Harris Corporation/RF Communications Group
1680 University Avenue
Rochester, New York 14610 U.S.A.
Phone: (716) 244-5830
Cable: RFCOM; Rochester, New York
Telex: 978464

SECTION 2

INSTALLATION

2.1 INTRODUCTION

This section provides unpacking and inspection information, equipment installation and mounting instructions, site selection, interconnection data, initial setup, and receiver functional test procedures.

2.2 UNPACKING AND INSPECTION

Carefully open the shipping carton and check the contents against the packing list secured to the outside of the container. Inspect all items for signs of damage. Immediately notify the carrier if any damage is discovered. Save all packing material for possible reshipment.

2.3 ANCILLARY KIT

Items that are supplied in the Receiver Ancillary Kit, (Part No. 10215-0021) are listed in table 2-1.

Table 2-1. Ancillary Kit (P/N 10215-0021)

Quantity	Part No.	Description
1	J22-0001-001	Connector, Type D, 25 pin
1	J55-0015-025	Hood, D-Connector, 25 pin
1	W-0023	Cord, Line, 6 feet

2.4 SITE SELECTION

The Receiver provides specified performance in any environment within the temperature range of 0°C to + 50°C and up to 95 percent humidity. Consider the following factors when determining the operating location for the Receiver.

- Avoid sites which will subject the receiver to conditions exceeding those mentioned above. If this is not possible, provide an environmentally controlled site (adequate ventilation, temperature control, etc.) to maintain the stated operating limits.
- Avoid nearby obstructions such as hills, trees, buildings, and power lines which absorb and reflect radio signals. In particular, avoid obstructions that are in a direct line with the desired directions of reception.
- Some antennas, especially the doublet, are directional and should be oriented for maximum signal gain. Therefore allow enough land area around the site to orient the antenna as necessary.
- Reception is generally best at the top of a hill, over level ground, or over water.

Once the operating site has been chosen, consider the following factors when positioning the Receiver at the site.

- Ease of operation and visibility of controls
- Relation to other units
- Power, control, and output interfaces
- Environmental considerations for unit and operator (temperature control, adequate ventilation, etc.).

WARNING

Always operate the Receiver with a heavy gauge ground strap connected from a solid earth ground to the rear panel ground. Failure to do so could result in serious injury or death to the operator if the receiver should ever fail in such a manner as to make the chassis electrically hot.

2.4.1 Antennas

Maximum receiver sensitivity is achieved when the antenna impedance presented at antenna input connector, J1, is 50 ohms. The use of coaxial cables, such as type RG-58/U terminated with an N type connector, prevents feed-line noise pickup and provides the proper impedance match.

Doublet antenna kits, such as the RF-334 and SB-AD, are available from Harris Corporation/RF Communications. Three basic types of antennas, the horizontal doublet, the inverted V, and the slant wire can be constructed with these kits. Figure 2-1 shows these three antenna types used in typical installations. Each type of doublet antenna has two legs of equal length, one connected to the center conductor of the coaxial cable and the other connected to the shield. The two legs have a combined electrical length of one-half wavelength (one-quarter wavelength for each leg).

The inverted V and slant wire doublets are useful if the antenna site prohibits the use of the two supports required for a horizontal doublet, or if the supports cannot be located so that the doublet is perpendicular to the direction of the desired transmitted signal. All doublet antennas are directional and provide best response to signals received from directions perpendicular to their lengths. The length of each element of a doublet can be determined from one of the formulas given in table 2-2.

2.5 MECHANICAL INSTALLATION

The Receiver may be desk mounted (RF-594-02 option), see figure 2-2, stack mounted (RF-594-03 option) or rack mounted (RF-594-01 option) into a standard 19-inch equipment rack. See figure 2-3 for rack mounting information. Note that two different mounting brackets are supplied for rack mounting. PN 10073-1010 fits the left side of the Receiver and PN 10073-1014 fits the right side. The detail drawing in figure 2-3 shows the left side bracket.

2.6 POWER REQUIREMENTS

The Receiver requires 115 Vac, 60 Hz single-phase power at 90 watts, nominally. Ac power selection is factory set to 115 Vac. The receiver can be configured for other line voltages including 100, 220, or 240 Vac. To select a different range, first turn the front panel power switch off, then remove the ac power cord at the rear panel. Slide the plastic cover out of the way to expose the fuseholder and remove the fuse by pulling on the lever labeled FUSE PULL. Grasp the small PC card (located to the left of the fuseholder) with needlenose pliers

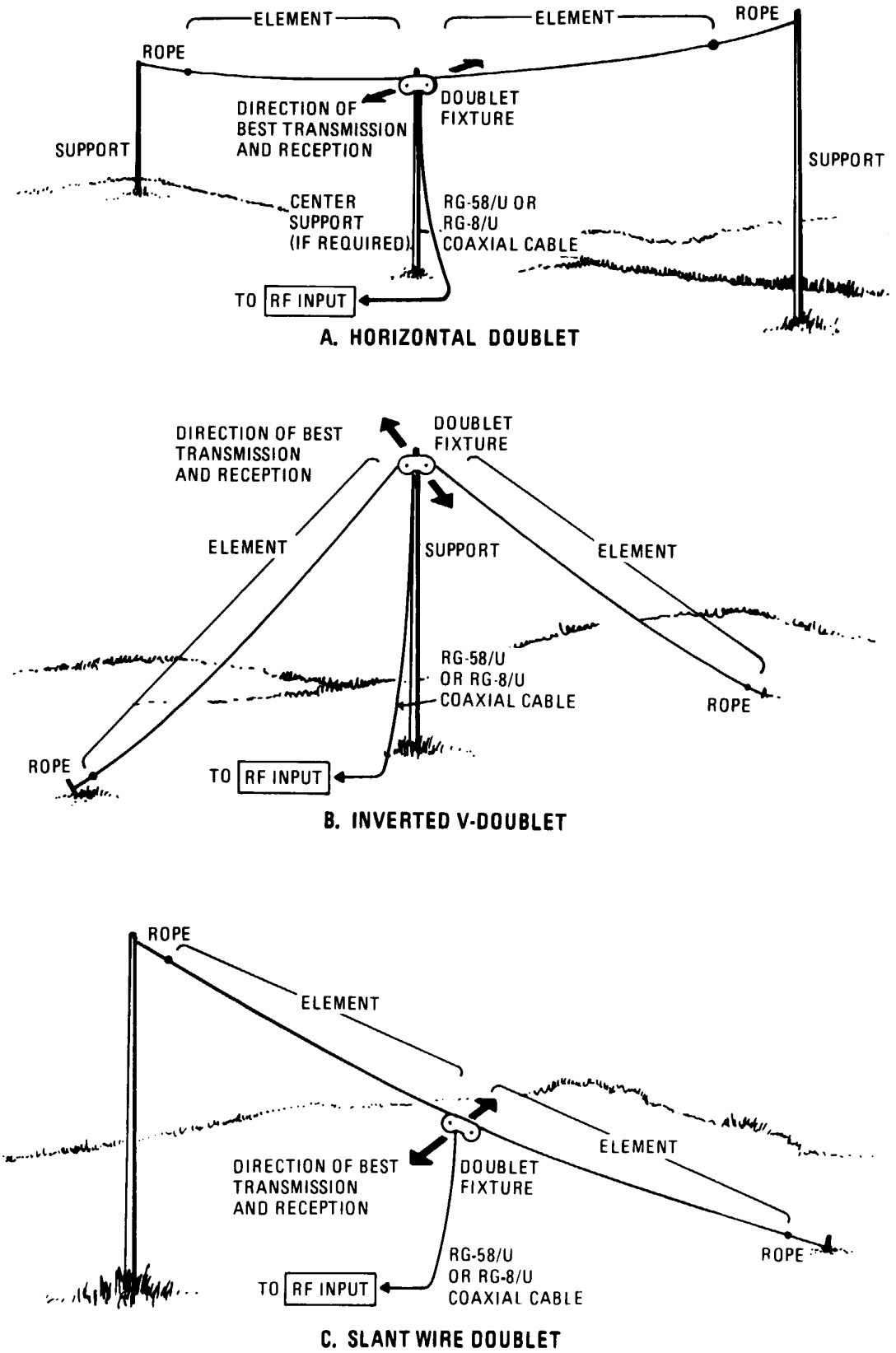


Figure 2-1. Typical Doublet Antenna Installation

Table 2-2. Calculation of Doublet Antenna Element Lengths

Antenna Type	Length of Each Element (Feet)	Length of Each Element (Meters)
Doublet, horizontal, or slanted	$\frac{234}{f\ (MHz)}$	$\frac{71.3}{f\ (MHz)}$
Inverted V doublet	$\frac{245}{f\ (MHz)}$	$\frac{74.5}{F\ (MHz)}$

and pull the card straight out. This card will be labeled with the numbers 100, 120, 220, and 240 Vac. Orient this card so that the desired range faces the fuseholder, and is the only number visible once the card has been reinserted. Insert the fuse for the selected voltage and reconnect the power cord to the radio and the ac source. Turn the power on.

2.7 INPUT/OUTPUT CONNECTIONS

The Receiver is complete and can be operated without other equipment. It requires only the appropriate power, antenna connections, and a headset. All other input/output connectors are used to expand and integrate features of the receiver or the system. Input and output connectors are shown and their uses explained in figure 2-4.

All RF type connectors are standard BNC, 50-ohm connections except the antenna connector which is an N type coaxial connector. Table 2-3 details the signal functions available at J7.

2.8 INITIAL SETUP AND ADJUSTMENTS

To set up the remote control interface, the Control Assembly A14 must be accessed. The A14 assembly is located behind the front panel. To access the assembly, remove the top and bottom covers, then the four phillips head screws on the front panel and tilt the panel forward. The front panel is hinged at the bottom. After the Control Assembly is configured, the front panel can be returned to its original position and power can be applied to the unit. Brightness of the displays can be adjusted at this point, if desired, by turning A13A2R29.

WARNING

High voltages are present inside the front panel when the receiver is turned on.

After the brightness has been adjusted, the top and bottom covers can be replaced. The line audio adjustments can be made when an appropriate signal is present using the adjustment screws adjacent to the front panel meter.

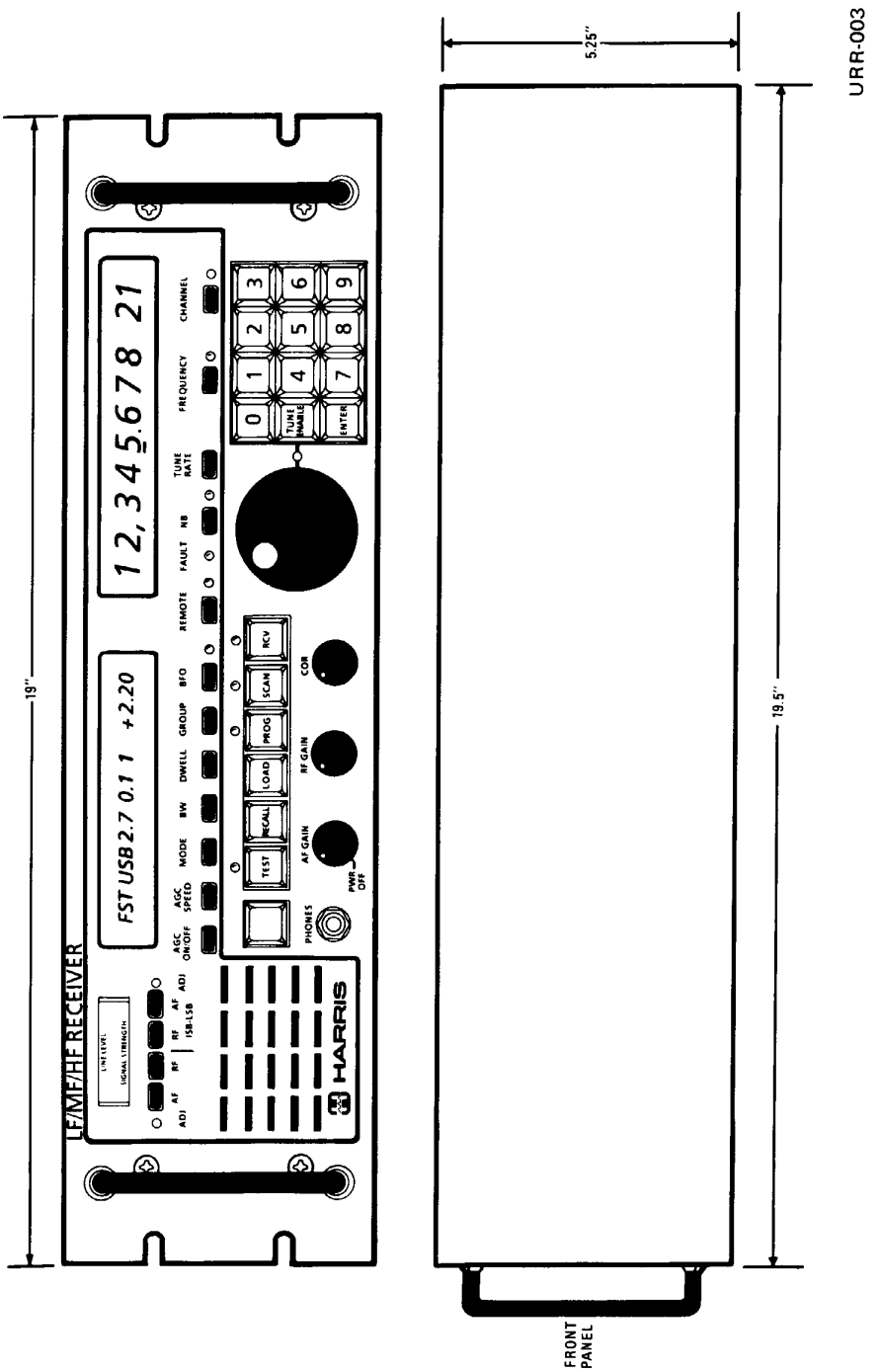


Figure 2-2. Desk Mount Dimensions

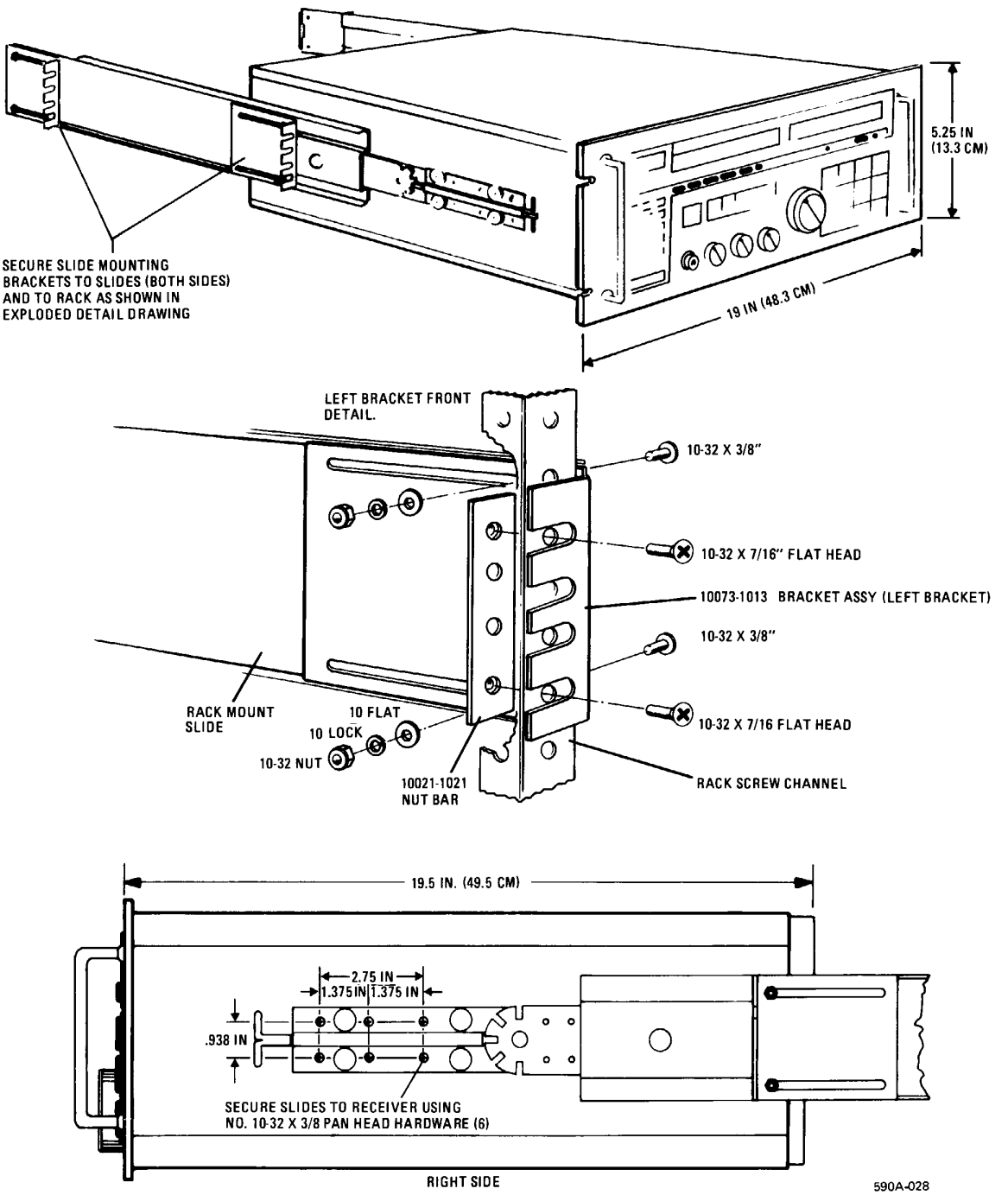


Figure 2-3. Rack Mounting Details

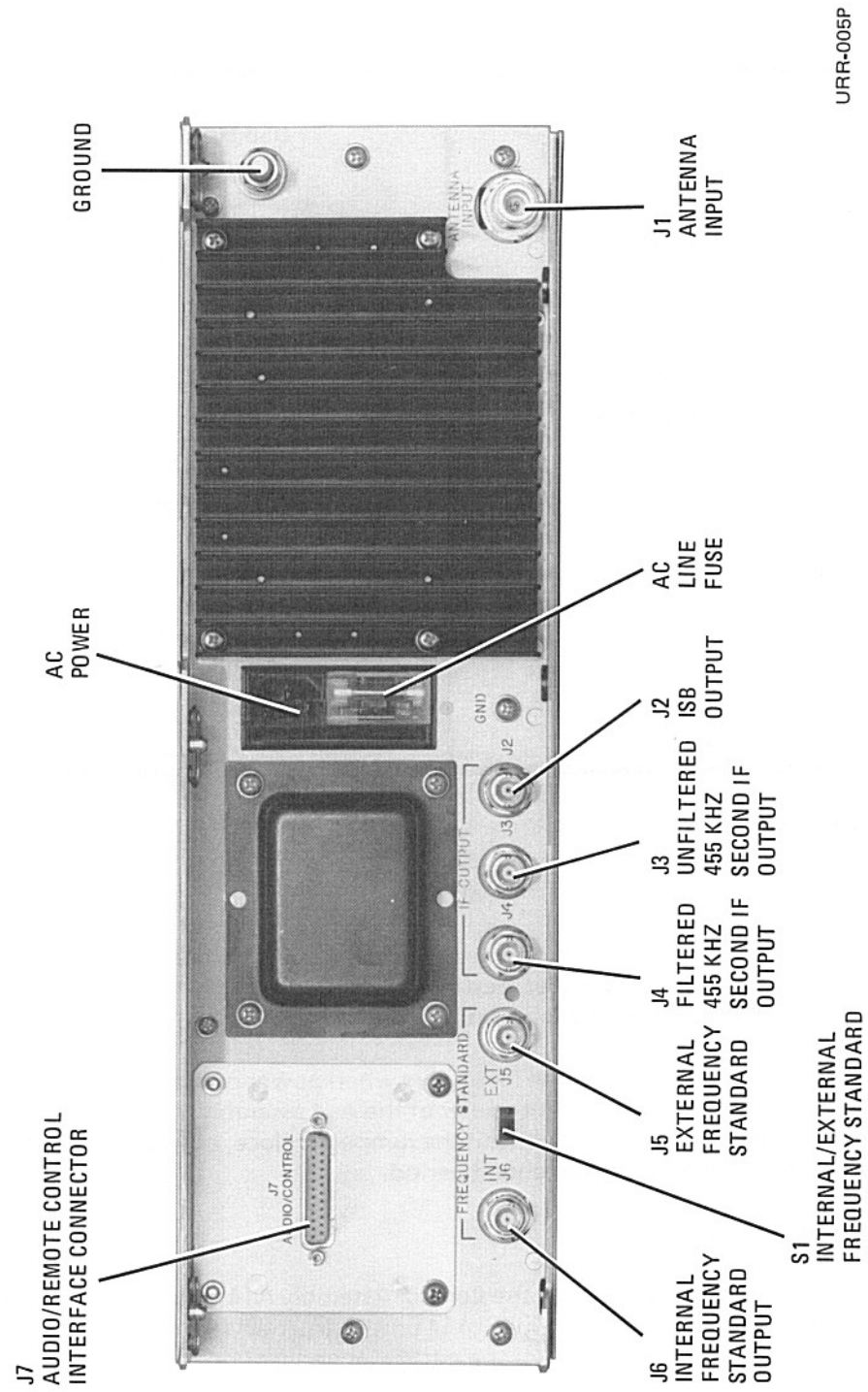


Figure 2-4. Rear Panel

Table 2-3. Rear Panel Connector J7

Pin	Function
J7-1	USB Line Out
J7-2	USB Line Ret
J7-3	GND
J7-4 thru J7-9	Spare
J7-10	COR (Contact)
J7-11	RS-232 Out/RS-422 Out -
J7-12	GND
J7-13	MIL-188C Out/RS-422 Out +
J7-14 thru J7-16	Spare
J7-17	ISB Line Out
J7-18	ISB Line Ret.
J7-19	GND
J7-20, J7-21	Spare
J7-22	COR (N.C.)
J7-23	COR (N.O.)
J7-24	RS-232 In/RS-422 In -
J7-25	MIL-188C In/RS-422 In +

2.8.1 Memory Backup Battery

CAUTION

DO NOT short backup battery terminals. A shorted battery can overheat, destroying the battery and damaging the PWB assembly.

A rechargeable Ni-Cad battery is used to keep the RAM alive when power is interrupted or the receiver is turned off. Jumper J17, located in the upper right corner of the A14 assembly, must be in place to activate the keep alive circuit. Receivers are normally shipped with the jumper in place, however, the jumper should be removed if the receiver is to be stored for an extended period.

2.8.2 Remote Control Interface Setup

The remote control interface circuit is located on the Control Assembly A14 and can be accessed when the front panel is folded down. See the Control Assembly A14 unit instruction section for locations of switches and jumpers. The interface must be configured for the particular application of the Receiver. The setup procedure includes:

- Enabling or disabling the interface
- Setting the baud rate

- Setting the unit ID
- Selecting the serial interface type

The control assembly has one serial interface that can be configured for a variety of standard interface types. For this application the interface must be configured for MIL-188. DIP switch S5 is used to enable the interface and configure the serial port. To enable or disable the remote control interface set switch S5-1 as follows:

- Remote Control Enabled: S5-1 Closed
- Remote Control Disabled: S5-1 Open

Note that when the remote control interface is disabled the REMOTE switch on the front panel will be disabled.

The serial interface is configured for MIL-188 using switches S5-2, and S5-4 thru S5-8, and jumper J19 on the A14 assembly. Switch S5-3 is not used for Remote Control configuration and should be closed. Switch settings and jumper positions for selecting the interface type are listed in table 2-4.

Table 2-4. Remote Control Interface Configuration Switch Setting

Switch or Jumper	S5-2	S5-4	S5-5	S5-6	S5-7	S5-8	A14J19
Setting or Position	Open	Open	Closed	Closed	Open	Open	2 to 3

The serial interface baud rate is selected by a 16-position rotary switch, S4. Most popular baud rates between 50 and 19200 are selectable. All selectable baud rates and their corresponding switch settings are listed in table 2-5.

For systems that use multiple, remotely controlled receivers, each receiver must have its own ID number. The ID number is selected as an 8 bit binary number by setting the switches of DIP switch S3 Table 2-6 lists the eight switches and their weights.

The bit is high when the corresponding switch is open. A bit is low when the switch is closed. Decimal numbers between 0 and 255 are selectable. The decimal equivalent of the switch settings can be calculated by adding the weights assigned to each closed switch. Note that the ID and the baud rate are read into the memory only at power up or when the microprocessor is reset.

The unit ID and the baud rate can be displayed on the front panel when the receiver is in the remote mode. To display them on the alphanumeric display, simply press and hold the ENTER pushbutton for about 10 seconds.

2.8.3 USB, LSB and ISB Line Audio Output Level Adjust

USB and LSB line audio output levels are adjustable from the front panel. Multiturn adjustment potentiometers are accessed through holes located next to the USB and LSB meter select pushbutton switches on the front panel.

Table 2-5. Serial Interface Baud Rate Switch Settings

S4 Position	Baud Rate
0	50
1	75
2	110
3	134.5
4	150
5	300
6	600
7	1200
8	1800
9	2000
A	2400
B	Not Used
C	4800
D	7200
E	9600
F	19200

Table 2-6. ID Number Switch Weights

Switch	Weight
S3-1	1
S3-2	2
S3-3	4
S3-4	8
S3-5	16
S3-6	32
S3-7	64
S3-8	128

2.8.4 Adjusting Front Panel Display Brightness

Potentiometer R29 on Front Panel Driver Board Assembly A13A2 is used to adjust the brightness of the vacuum fluorescent displays. R29 can be accessed by removing the top chassis cover. R29 can be adjusted with a small screwdriver and is identified in subsection A13.

2.9 FUNCTIONAL CHECKOUT PROCEDURE

The following is a local control functional test to determine the satisfactory operation of the Receiver. The following equipment (or equivalent) is required.

- HP-8640B Signal Generator
- HP-5383A Frequency Counter

The following paragraphs briefly describe and test Receiver operation. The operator may find it useful to read section 3, Operation, prior to or concurrently with this procedure. Connect the signal generator and frequency counter shown in figure 2-5.

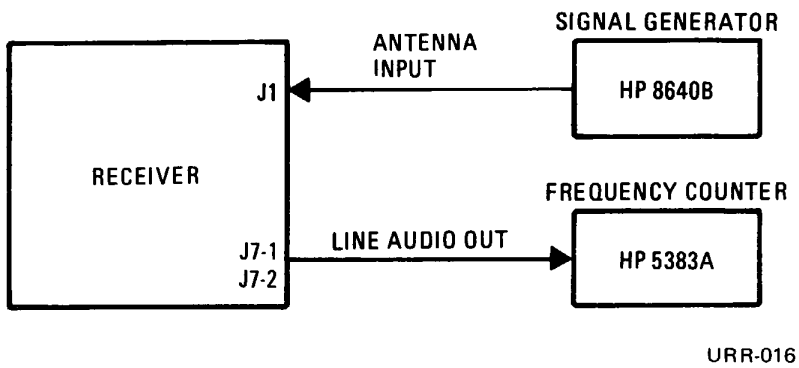


Figure 2-5. Functional Test Setup

2.9.1 Receive Mode Test

Apply the ac power and check that the receiver powers up with RCV (Receive), FREQUENCY, and TUNE LEDs lit. The receiver will run a self-test routine when turned on. The fault indicator will be lit during the test cycle but should go out shortly after that. If the unit fails, the fault indicator will remain lit and a fault code will be displayed. See the maintenance section for fault code definitions.

Set the receiver to the following initial conditions:

- Mode: USB
- RF Gain: Fully clockwise (cw)
- AGC: MED

Connect the signal generator to the receiver's antenna input and set the generator for a level of -24 dBm (14.1 mV_{rms}) at any frequency.

2.9.1.1 Frequency Entry

Press the FREQUENCY button and enter a frequency of 12.345678 MHz via the keypad. Press ENTER. Set the signal generator to a frequency 1 kHz above the receiver tuned frequency (12.346678) and note the 1-kHz

audible output tone. Connect the frequency counter to the line audio output and verify the audio frequency is 1 kHz.

2.9.1.2 Tune Rate

Press TUNE RATE successively until the cursor is beneath the 1-kHz digit. Rotate the tuning wheel and use the signal generator to verify tuning in 1 kHz steps.

Press TUNE RATE to place the cursor beneath the 100-Hz digit and use the signal generator to verify tuning in 100 Hz steps.

Press TUNE RATE to place the cursor beneath the 10-Hz digit and use the signal generator to verify tuning in the 1 Hz steps.

2.9.1.3 Mode Selection

Press the MODE button under the alphanumeric display and check that USB, LSB, ISB, FM, CW, and AM, are selectables as modes. Keeping the button pressed causes the display to scroll through the valid modes. Release the button and the receiver is placed into the selected mode.

2.9.1.4 Bandwidth Selection

Press the BW button under the alphanumeric display and check that the bandwidth display scrolls through the filter selections that are valid for the selected mode. (Note that filter bandwidths are customer specified, and will vary depending on the requirements. A typical filter complement for different modes is shown in table 2-7.

Table 2-7. Typical Filter Complement

Mode	Bandwidth
USB	2.7 kHz
LSB	2.7 kHz
CW	0.3 kHz
AM	6.0 kHz, 16.0 kHz
FM	16.0 kHz

2.9.1.5 AGC Selection

With the Receiver in the CW mode, press the AGC speed button beneath the alphanumeric display and check that the AGC speed selection scrolls from SLOW to FAST to MEDIUM until released.

2.9.1.6 BFO Selection

Select the USB mode, and press the BFO button to enable BFO entries. Check that the BFO LED Lights and that keypad selections (followed by pressing ENTER) cause the BFO offset frequency to appear in the BFO display field.

Check that the tuning wheel varies the BFO selection when the TUNE LED is lit.

With the signal generator set for a frequency of 12.346678 and the receiver set at 12.345678, USB mode, tune the BFO via the tuning wheel to + 1 kHz and check that a zero beat is obtained.

Return the BFO frequency to 0.00 kHz.

2.9.1.7 RF Gain

Set the front panel meter pushbuttons to measure USB RF level. Press the AGC ON/OFF button under the alphanumeric display to select AGC OFF. Verify that the AGC display changes to OFF and that the meter reading increases. Adjust the RF GAIN control and verify that the meter reading changes.

2.9.1.8 AF Gain

Rotate the AF GAIN knob and check that the volume is adjustable.

2.9.1.9 Load Memory Function

The channel programming memory allows up to 100 channels to be stored. Press the PROGRAM button to place the receiver in the Program mode, and check that the PROGRAM and CHANNEL LEDs light. Perform the following steps:

a. Enter 01 via the keyboard.

b. Press FREQUENCY and enter 01.111111 MHz via the keyboard. Press ENTER.

c. Select AGC-SLO, MODE-USB.

d. Press LOAD.

e. Press CHANNEL and enter 02 via the keyboard.

f. Press FREQUENCY and enter 02.222222 MHz via the keyboard. Press ENTER.

g. Select AGC MED, MODE-LSB.

h. Press LOAD.

i. Press CHANNEL and enter 03.

j. Push FREQUENCY and enter 03.333333 MHz. Press ENTER.

k. Select AGC-FAST, MODE-CW, BW-0.3 kHz.

l. Press LOAD.

m. Press CHANNEL and enter 04.

n. Press FREQUENCY and enter 04.444444 MHz. Press ENTER.

o. Select AGC-MED, MODE-CW, BW-0.3 kHz.

p. Press LOAD.

q. Press RECEIVE to leave the Program mode.

2.9.1.10 Channelized Reception

With the Receiver in the Receive Mode (RCV LED lit), press the CHANNEL button. (CHANNEL LED should light.) Select each channel number (followed by ENTER) listed in table 2-8. Check that the receiver front panel updates to number listed. Using the signal generator, check that the receiver has in fact tuned to the frequency listed.

Table 2-8. Programmed Channels

Channel	Frequency MHz	AGC	Mode	Bandwidth kHz
01	01.111111	SLO	USB	2.7
02	02.222222	MED	LSB	2.7
03	03.333333	FST	CW	0.3
04	04.444444	MED	CW	0.3

With the TUNE and CHANNEL LEDs lit, rotate the tuning wheel. Check that channels 1-4 are selected.

2.9.1.11 Local/Remote Switch

The following test applies only if the remote control interface is enabled. If not, the REMOTE button will have no effect. With the Receiver under local control, press the REMOTE button and check that the REMOTE LED lights and that it is no longer possible to change Receiver parameters via the front panel. Make sure that by pressing the REMOTE button a second time, the Receiver is placed back under local control.

2.9.1.12 Meter Switch

Set the Receiver in the following conditions:

- Frequency: 12.345678
- Mode: USB
- AGC: MED
- RF Gain: Fully clockwise (cw)
- AF Gain: As desired

Set the signal generator to a frequency of 12.346678 MHz and a level of -24 dBm (14.1 mV_{rms}).

Press the USB/RF pushbutton under the meter. The meter indication should be approximately 14 mV_{rms}.

Press the USB/AF pushbutton under the meter. The meter indication should be approximately 0 dBm unless the meter has been set to indicate some other level.

Note that the USB positions select USB information and the ISB-LSB positions select LSB information.

2.9.1.13 COR Control

Set receiver as in paragraph 2.9.1.11. Verify COR operation as the COR control is varied. The COR should be energized and deenergized as the COR threshold is adjusted above and below the carrier levels. Check for continuity between J7-10 and J7-22, J7-23.

2.9.2 Program Mode

NOTE

Channels 1 through 4 were previously programmed in step 2.9.1.9 of this procedure.

2.9.2.1 Recall Memory Function

Place the receiver in the Program mode. Enter 02 via the keyboard and press RECALL. The display should update to 02.222222 MHz, CHANNEL-02, AGC-MED, MODE-LSB.

2.9.2.2 Program Group Function

Group programming of channels allows the preprogramming of up to 10 channel groups (20 channels per group maximum). Channels may be programmed in any order and any channel can appear in more than one group.

To program a group, place the receiver in the Program mode and perform the following steps:

a. Press GROUP.

b. Enter the number 1 via the keyboard in response to the prompt GROUP NUMBER?. Press ENTER.

c. Enter 03 via the keyboard in response to the prompt CHANNEL NUMBER?, and press ENTER and LOAD. The display will respond with 03 OK.

d. Enter 02, followed by ENTER and LOAD.

e. Enter 01, followed by ENTER and LOAD.

f. Exit programming by pushing RECEIVE.

g. Proceed to 2.9.3. Verification of Group programming will be done during the Group scan test.

2.9.3 Scan Mode Test

The following two scan modes are available on the Receiver:

- Channel scan
- Group scan

Channel scan allows the automatic sequential scanning of up to 100 programmed channels. Group scan allows scanning of up to ten groups (20 channels per group, maximum). Follow the steps in paragraph 2.9.3.1 to perform a Channel scan and the steps in 2.9.3.2 to perform a Group scan.

2.9.3.1 Channel Scan

a. With the Receiver in RECEIVE MODE, press SCAN. SCAN LED should light.

b. Press CHANNEL in response to GROUP or CHANNEL SCAN?.

c. Enter 01 followed by ENTER in response to FIRST CHANNEL?.

d. Enter 04 followed by ENTER in response to LAST CHANNEL?. The Receiver should commence to automatically scan channels 1-4. Press SCAN; verify that the scanning stops. Verify that pressing SCAN again restarts scanning. Verify that pushing the DWELL button affects the dwell speed accordingly.

2.9.3.2 Group Scan

a. Push the RECEIVE button, then SCAN.

b. Press GROUP In response to the GROUP or CHANNEL SCAN? prompt.

c. Enter 1 via the keyboard, followed by ENTER. The Receiver should now scan channels 3, 2, 1 in that order.

2.9.4 Self-Test (BITE)

Press the TEST button to begin the Receiver's self-diagnostics. The Receiver will perform an automatic self-test, approximately 5 seconds in length. During this time, all front panel display segments and LEDs should light, and stay lit until the message --- TEST PASSED --- appears in the left-hand display.

In the event of a failure, a Receiver fault code will be displayed. If this occurs, consult the maintenance section of this manual, table 5-1, which lists the fault codes by assembly number.

2.9.5 Reconnection

After the checkout is complete, disconnect the signal generator and the frequency counter. Reconnect the antenna and audio output lines, if used.

SECTION 3

OPERATION

3.1 INTRODUCTION

The following paragraphs describe the function of the front panel controls and indicators and the basic operational modes of the Receiver. Operation of the Receiver is not difficult but should not be attempted before reading this section. This section begins with descriptions of the front panel controls and indicators. The controls and indicators have been broken up into functional groups for the purpose of discussion. Normal (non-programmed) operation is discussed immediately following the control and indicator descriptions. That discussion is followed by programming instructions and channelized operating procedures for a programmed receiver. Programmed operation includes channel and group scanning.

3.2 CONTROLS AND INDICATORS

3.2.1 Power, AF Gain, RF Gain, and COR

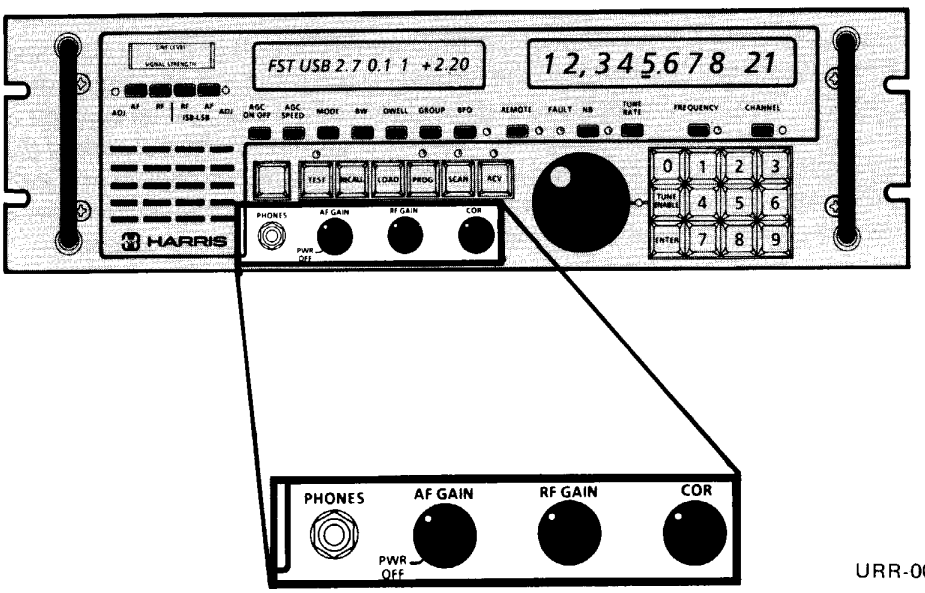
The power on/off, AF Gain, RF Gain, and COR controls are shown and described in figure 3-1. The receiver power control is combined with the audio gain (AF GAIN) control. The receiver is off when the knob is rotated fully counterclockwise. Rotate the knob clockwise past the click stop to turn the Receiver on. Rotate the knob clockwise to increase the audio amplifier gain and the volume level at the headphones. The RF GAIN control knob is used to manually control the radio frequency amplifier. The COR control sets the threshold at which the carrier operated relay is energized. Rotate the knob clockwise to raise the threshold.

3.2.2 Tuning Wheel and Keypad Entries for Channel, Frequency, BFO, and Group

The operating frequency, channel, BFO, and group are displayed on the front panel as shown and described in figure 3-2. These displays can be changed using the keypad, or, except for the GROUP display, the tuning wheel. The keypad or tuning wheel is dedicated to one display at a time as selected by the switches under the displays. LEDs located next to the switches light to identify the active display. To use the tuning wheel, press and release the TUNE ENABLE button located in the keypad matrix. An LED located between the tuning wheel and the TUNE ENABLE button will be lit when the wheel is active.

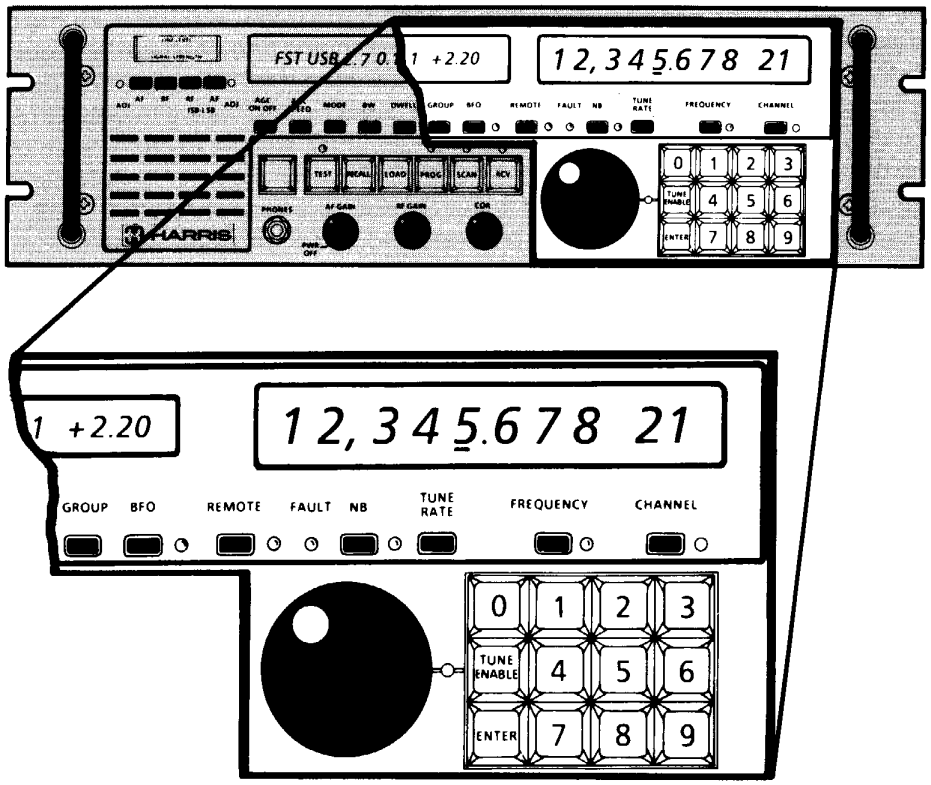
When using the tuning wheel to scan or select frequencies, the operator can change the sensitivity of the wheel. The resolution is defined as total frequency change per turn of the wheel and is selected by using the TUNE RATE pushbutton located below the frequency display. This pushbutton changes the position of a cursor located below the digits in the frequency display. The cursor position selects the associated digit as the tuning unit. If the cursor is in the 1-kHz position, the tuning wheel will raise or lower the frequency in 1-kHz increments. With the cursor in the 10-kHz position, the wheel will raise or lower the frequency in 10-kHz increments. The 10-MHz cursor position is not allowed and will effectively disable the tuning wheel when selected.

Channel groups are used only in the Scan mode. Groups do not have to be entered for other modes of operation. See the operating procedures for proper entry of group numbers.



CONTROL/ INDICATOR	FUNCTION	CONTROL/ INDICATOR	FUNCTION
PWR OFF/ AF GAIN	Receiver On/Off, Loudspeaker and Headphone Audio Level	COR	Sets threshold to energize the carrier operated relay. Turn knob fully clockwise for maximum threshold.
RF GAIN	Controls Radio Frequency (RF) Gain. Turn fully clockwise for maximum gain. Gain Control Gain Range is over 100 dB.	PHONE	Headphone Jack. Accepts PL-55 type plug.

Figure 3-1. Power ON/OFF, AF Gain, RF Gain, and COR



URR-008

CONTROL/ INDICATOR	FUNCTION	CONTROL/ INDICATOR	FUNCTION
TUNING WHEEL	Used to select or scan frequencies and select BFO when operating in normal mode, or select channels in the programmed mode. Enabled by TUNE ENABLE.	CHANNEL	Enables the channel display to receive entries from the keypad or to be changed by the tuning knob. The LED adjacent to the pushbutton switch is lit when the display is enabled.
TUNE ENABLE	Enables tune wheel to scan frequencies, channels, or set BFO offset. LED indicates Tuning Wheel is enabled.	BFO	Enables Beat Frequency Oscillator offset display to receive entries from the keypad, or to be changed by the tuning knob. The pushbutton switch is also used to change the direction of offset + or -.
TUNE RATE	Selects tune rate for tuning wheel by positioning cursor under desired digit in frequency display. Digit selected becomes tuning increment. Cursor position also locates starting place for keypad frequency entries.	GROUP	Enables the group display to receive entries from the keypad. Allowed entries are from 0 to 9. See section 3.5 for group programming instructions.
FREQUENCY	Enables frequency display to receive entries from the keypad or to be changed by the tuning knob. The LED adjacent to the pushbutton switch is lit when the display is enabled.	ENTER	Enters displayed data. In remote mode will display unit ID and baud rate.

Figure 3-2. Channel, Frequency, BFO, and Group Display Entries

3.2.3 AGC, Mode, BW, and Dwell

The automatic gain control (AGC), demodulation mode, bandwidth (BW), and the scanning dwell interval are selected using the pushbutton switches and associated displays shown and described in figure 3-3. The AGC speed constant, demodulation mode, filter bandwidth and scanning dwell time are displayed during normal operation of the receiver. The AGC SPEED, MODE, BW, and DWELL switches are located directly below, and are used to change their respective displays. The operator can single step or scroll through the available options for each of the operating parameters. The AGC ON/OFF switch toggles the AGC circuit on and off. The AGC circuit adjusts the Receiver's gain to limit audio output variations to less than 3 dB. The AGC attack is fixed at less than 20 milliseconds except when DATA is selected, it is then less than 10 milliseconds. The AGC hang and decay time constants (AGC speed) are front panel selectable as follows:

- SLO (slow, 2.5 ± .5 second)
- MED (medium, 200 ± 50 milliseconds)
- FST (fast, less than 35 milliseconds)
- DAT (Data, less than 20 milliseconds, available in USB, LSB, and ISB only)

Slower decay constants are usually desirable for voice applications while the faster decay time constant is used for data applications.

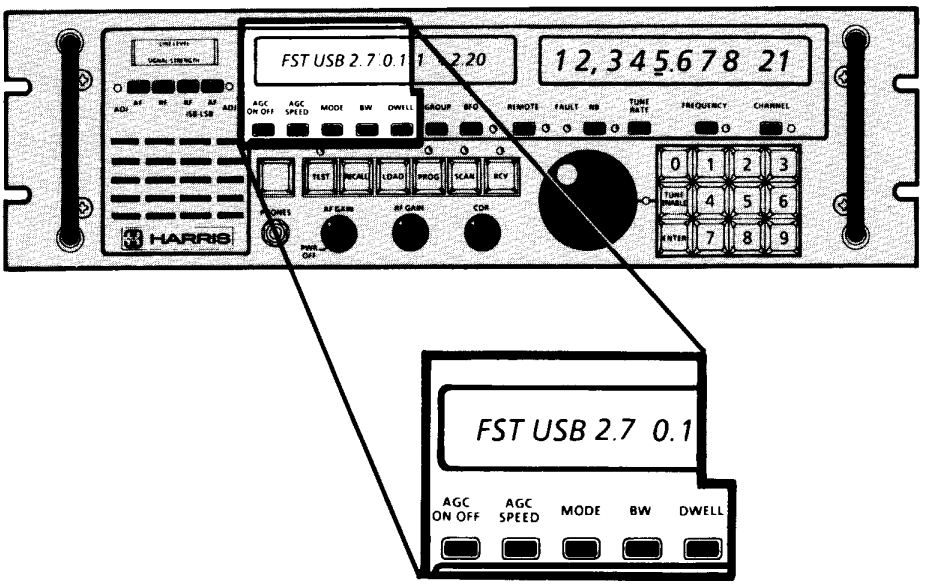
The standard available demodulation modes are:

- USB (upper sideband)
- LSB (lower sideband)
- AM (amplitude modulation)
- FM (frequency modulation)
- CW (continuous wave)
- ISB (Independent sideband)

An optional demodulation mode is FSK (frequency shift keying).

The available filter bandwidths will vary with the demodulation mode and are displayed in kHz.

The dwell is the time the Receiver will monitor each channel when scanning operation is selected. The dwell is displayed in seconds and can be set between 0.1 and 8.



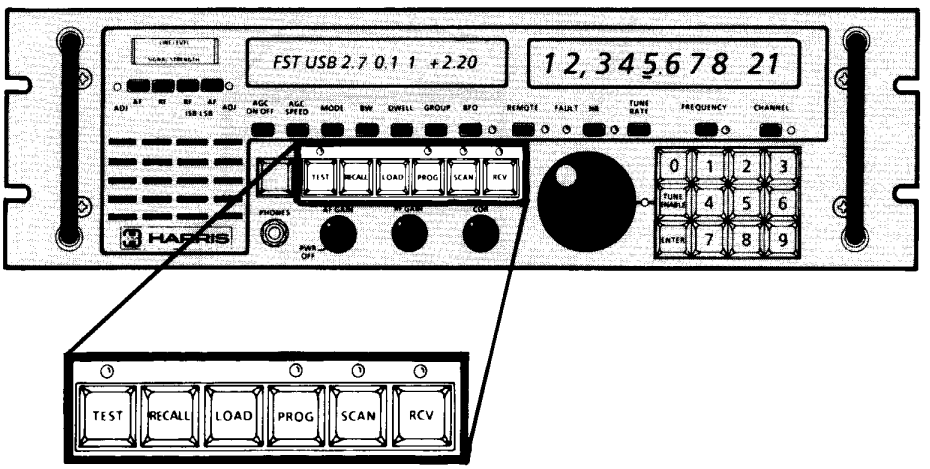
URR-009

CONTROL/ INDICATOR	FUNCTION	CONTROL/ INDICATOR	FUNCTION
AGC ON/OFF	Toggles Automatic Gain Control on and off.	BW	Single steps or scrolls through bandwidths available for selected mode. Selected bandwidths are displayed above the switch.
AGC SPEED	Selects AGC speed slow, medium, fast, or data. Selections are displayed above the switch. Hold switch to scroll, or press and release to single step selections.	DWELL	Single steps or scrolls through available dwell times for scanning operation. Selected dwell time is displayed in seconds above the switch (0.1 to 8 seconds)
MODE	Pushbutton switch used to select demodulation mode for the receiver, USB, LSB, CW, AM, FM, or ISB standard 4-ISB, or FSK optionally. Single steps or scrolls choices. Selections are displayed above switch.		

Figure 3-3. AGC, Mode, BW, and Dwell Displays and Controls

3.2.4 TEST, RECALL, LOCAL, PROG, SCAN, and RCV Controls

The large pushbutton switches in the center of the front panel are used to select the Receiver's operating mode, call up the auxiliary channel and load channel parameters or channel groups into memory. The switches are shown and described in figure 3-4.



URR-010

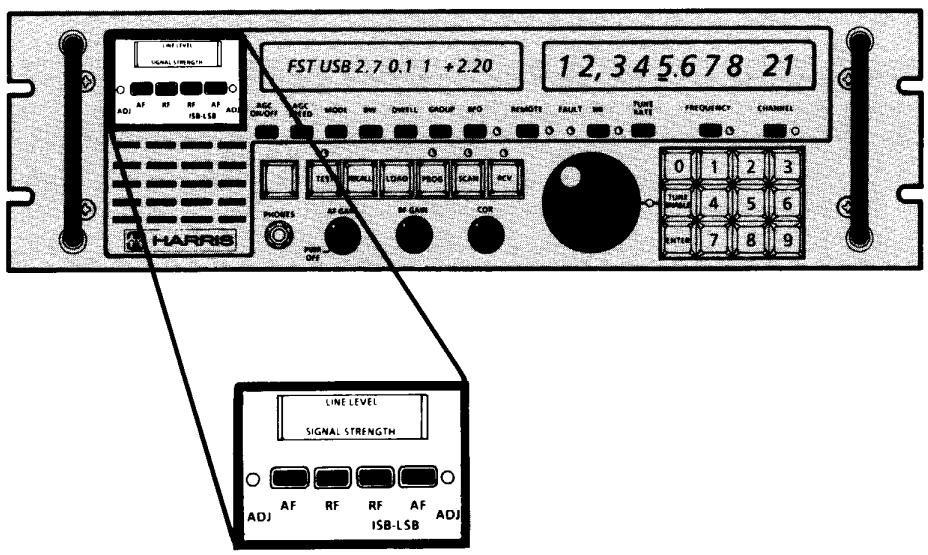
CONTROL/ INDICATOR	FUNCTION	CONTROL/ INDICATOR	FUNCTION
TEST	Puts the receiver in the test mode and initiates the BITE sequence. The LED above the switch is lit while the test is in progress.	PROG	Selects the programming mode. The LED above the switch is lit when the receiver is in the programming mode.
RECALL	Recalls the programmed auxiliary channel in RCV mode. Recalls last channel entered in PROG mode.	SCAN	Selects the scan mode of operation. The LED above the switch is lit when the receiver is in the scan mode.
LOAD	Loads channel parameters or channel groups into memory in program mode.	RCV	Returns the receiver to the receive mode from the test, programming or scan mode.

Figure 3-4. Speaker, Test, Recall, Load, Program, Scan and Receive Control

3.2.5 Front Panel Meter

The front panel meter can be used to measure the signal strength of the incoming RF signal or the line output level of the audio signal. The meter and its associated switches are shown and described in figure 3-5. The logarithmic scale on the meter measures RF signal strength between 1 microvolt and 100 millivolts. Audio output levels can be measured between -15 dBm and + 15 dBm with the center of the scale marked at + 4 dBm.

For ISB operation, the USB AF and ISB-LSB AF switches serve double duty. In addition to selecting the meter function, they also select USB or LSB audio for the headphones.



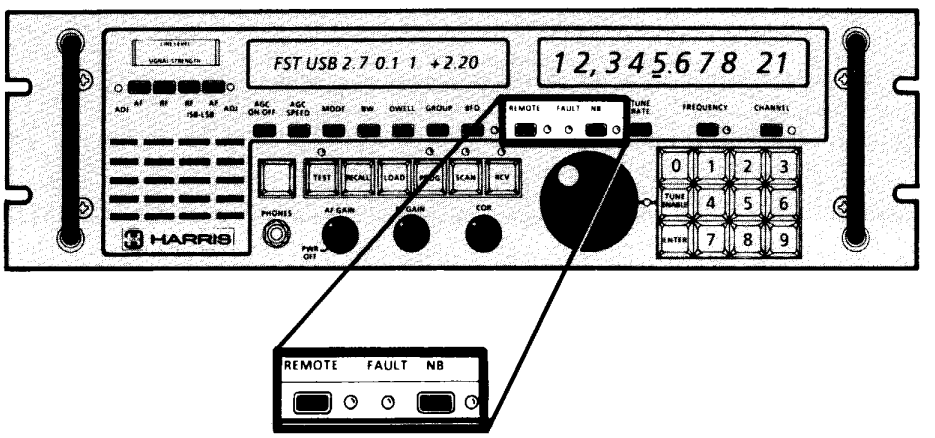
URR-011

CONTROL/ INDICATOR	FUNCTION	CONTROL/ INDICATOR	FUNCTION
METER	Displays RF signal strength or line audio output level.	ISB-LSB AF	Selects LSB audio output signal level for meter display. Selects LSB audio in 2-ISB mode.
USB-AF	Selects USB line audio output level for meter display. Selects USB audio in 2-ISB mode.	ISB-LSB RF	Selects LSB radio frequency signal strength for meter display.
USB-RF	Selects USB radio frequency signal strength for meter display.		

Figure 3-5. Front Panel Meter and Controls

3.2.6 Remote, Fault, and NB (Noise Blanker)

The FAULT indicator, REMOTE switch and indicator, and the NB (noise blanker) switch and indicator are located below the numeric display as shown in figure 3-6. When the Receiver is in the remote mode all switches except the ENTER key are locked out. In the remote mode, the ENTER key is used to display the unit ID and the remote interface baud rate. These are displayed on the alphanumeric display when the ENTER key is pushed and held for 10 seconds.



URR-012

CONTROL/ INDICATOR	FUNCTION	CONTROL/ INDICATOR	FUNCTION
REMOTE	Toggles the receiver between local and remote modes. LED adjacent to the pushbutton switch is lit when the unit is under remote control.	NB	Enables and disables optional Noise Blanker. The LED adjacent to the pushbutton switch is lit when the noise blanker is enabled.
FAULT	Red LED Lights to indicate a fault condition.		

Figure 3-6. Remote, Fault and Noise blanker (NB) Controls and Indicators

3.3 POWER UP

The AF GAIN-ON/OFF control/switch is used to turn the Receiver on and off. The Receiver is off when the knob is turned fully counterclockwise. To turn the Receiver on, turn the knob clockwise past the click stop. At power up the Receiver will automatically run the BITE routine. The LED above the TEST switch will be on while the test is in progress. At the end of the test cycle the TEST indicator will go out and the Receiver will enter either the local or remote mode depending upon the mode selected at power off. The front panel will display the frequency, AGC speed, bandwidth, etc. selected when the Receiver was turned off.

3.4 RECEIVER (NON-CHANNELIZED) OPERATION

Nonchannelized operation may be used before channels are programmed or when the operator wishes to receive on an unprogrammed frequency. The Receiver will revert to the nonchannelized mode if any of the parameters of a selected channel are changed during channelized operation. The following general procedure describes nonchannelized operation.

3.4.1 Operating Procedure

STEP	ACTION
a.	If the REMOTE indicator is lit, push and release the REMOTE pushbutton switch. The REMOTE indicator should not be illuminated.
b.	Push and release the RCV pushbutton switch. The LED above the switch will light to indicate that the Receiver is in the receive mode.
c.	To select the demodulation mode, push and hold the MODE pushbutton switch while watching the MODE display. Release the pushbutton when the desired mode is displayed.
d.	Push and release the FREQUENCY pushbutton switch. The LED adjacent to the switch will light to indicate that digits can be entered into the frequency display.

NOTE

The frequency can be entered directly from the keypad or can be selected by using the tuning wheel. When using the keypad, digits will be entered from left to right (10 MHz to 1Hz). Digits will dim to half brightness as they are entered. To use the tuning wheel, press and release the TUNE ENABLE push- button switch. Use the TUNE RATE pushbutton switch to position the cursor and select the tuning rate unit. Turn the wheel until the desired frequency is displayed.

e.	Enter or select the desired frequency.
f.	Push and release the ENTER pushbutton switch. The frequency display will increase to full brightness and the receiver will tune to the selected frequency.

STEP	ACTION (Cont.)

NOTE

At this point the receiver should be operational. You may turn the AGC on or off, select a bandwidth filter, adjust the beat frequency oscillator (BFO) offset. The following steps set these operating parameters.

g. Turn the AGC on or off using the AGC ON/OFF pushbutton switch. The AGC display will light when the AGC is on. To select the AGC delay time constant (AGC speed), push and hold the AGC SPEED pushbutton switch until the desired speed is displayed and release the switch. For manual RF gain control, turn the AGC to OFF and adjust the RF GAIN knob until the desired signal strength is obtained.

h. Push and hold the BW (Bandwidth) pushbutton switch until the desired filter bandwidth is displayed, then release the switch.

i. To set the BFO offset, press and release the BFO pushbutton switch. Change the offset using the keypad or the tuning wheel. The direction of the offset (+ or -) can be changed by pushing and releasing the BFO pushbutton switch when the adjacent LED is lit. (Invalid on AM and FM mode.)

j. Frequency and other operating parameters can be changed as required.

3.5 PROGRAMMING THE RECEIVER FOR CHANNELIZED OPERATION

The Receiver must be programmed before it can be used for channelized operations including scanning. The procedure in 3.5.1 can be used to program up to 100 channels into the receiver. The procedure in 3.5.2 is used to create up to 10 groups of up to 20 channels each for group scanning operation.

3.5.1 Channel Programming Procedure

STEP	ACTION

a. Push and release the PROG pushbutton switch. The LED above the switch will light to indicate that the receiver is in the programming mode.

b. Push and release the CHANNEL push button switch, the LED adjacent to the switch will light to indicate that digits can be entered into the CHANNEL display from the keypad.

c. Enter the channel number from the keypad (two digits must be entered).

d. Push and release the ENTER pushbutton.

e. Push and release the FREQUENCY pushbutton switch. The LED adjacent to the switch will light to indicate that digits can be entered into the frequency display.

f. Select the frequency for the displayed channel using the keypad or tuning wheel.

STEP	ACTION (Cont.)

NOTE

Normally frequency digit entries begin with the 10 MHz digit. For entry of multiple channels with similar frequencies entries, it is not always necessary to change the most significant digits in the display. To save time, the TUNE RATE pushbutton can be used to position the cursor below the most significant digit that will be changed repeatedly.

g. Once the frequency is entered, press and release the ENTER pushbutton switch.

NOTE

Steps h through m adjust the BFO offset, demodulation mode, bandwidth, and AGC speed and may not have to be performed depending upon the status of the displayed parameters.

h. Push and release the BFO pushbutton switch. The LED adjacent to the switch will light to indicate that entries can be made into the BFO display from the keypad.

i. Adjust the BFO offset frequency using the keypad or the tuning wheel. Change the sign of the offset by pressing and releasing the BFO pushbutton switch.

j. Push and release the ENTER pushbutton switch.

k. Select AGC on or off using the AGC ON/OFF pushbutton. If its turned on, use the AGC SPEED pushbutton to select the desired speed.

l. Push and hold the MODE pushbutton switch. The demodulation modes will be scrolled on the display above the switch. Release the MODE switch when the desired mode is displayed.

m. Push and hold the BW (bandwidth) pushbutton switch. The available filters for the selected mode will be scrolled on the display above the switch. Release the switch when the desired bandwidth is displayed.

n. Push and release the LOAD pushbutton switch.

NOTE

This concludes the programming for the first channel. To program additional channels repeat steps a through m. The RECALL Pushbutton switch can be used at any time while the Receiver is in the program mode to display the parameters of the channel entered prior to the currently displayed channel.

o. When programming is complete, push RCV or SCAN, as desired, to exit the program mode.

3.5.2 Group Programming Procedure

Channels can be arranged in groups for scanning. Up to 10 groups can be entered, each with up to 20 channels. Channels can be entered in any order and will be scanned in the sequence that they are entered.

STEP	ACTION
a.	Push and release the PROG pushbutton switch. The LED above the switch will light to indicate that the Receiver is in the program mode.
b.	Push and release the GROUP pushbutton switch. The prompt GROUP NUMBER? will appear on the alpha numeric display above the switch.
	NOTE Entry of a group number will automatically erase any previous entries for that group.
c.	Using the keypad, enter the single-digit group number (0 thru 9) and push and release the ENTER key. The Receiver will respond by displaying the prompt CHANNEL NUMBER?.
d.	Using the keypad, enter the first two digit channel number in the group.
e.	Push and release the LOAD pushbutton.
f.	Repeat steps d thru f for additional channel entries for this group. Up to 20 channels can be entered.
g.	Repeat steps b through g for up to 10 groups.
h.	To exit the program mode, press and release the RCV or SCAN pushbutton as desired.

3.5.3 Entering Auxiliary Channel Procedure

A frequently used or special application channel can be entered into the Receiver's memory as the auxiliary channel. The auxiliary channel can be recalled using the RECALL pushbutton. The parameters for the auxiliary channel may be entered using the following procedure.

STEP	ACTION
a.	Push and release the RCV pushbutton switch. The LED above the switch will be lit to indicate that the Receiver is in the receiver mode.
b.	Push and release the FREQUENCY pushbutton switch. The LED adjacent to the switch will light to indicate that digits can be entered into the frequency display.
c.	Select the frequency for the auxiliary channel using the keypad or tuning wheel.

STEP	ACTION (Cont.)

NOTE

Normally frequency digit entries begin with the 10-MHz digit. To save time, the TUNE RATE pushbutton can be used to position the cursor below the most significant digit that will be changed.

d. When the desired frequency is displayed, push and release the ENTER pushbutton switch.

NOTE

Steps e through h set the BFO offset, demodulation mode, bandwidth, and AGC speed, and may not have to be performed depending upon the status of the displayed parameters.

e. Push and release the BFO pushbutton switch. The LED adjacent to the switch will light to indicate that entries can be made into the BFO display from the keypad.

f. Set the BFO offset frequency using the keypad or the tuning wheel. Change the sign of the offset by pressing and releasing the BFO pushbutton switch.

g. Push and release the ENTER pushbutton switch.

h. Turn the AGC on or off using the AGC ON/OFF pushbutton. If its turned on, use the AGC SPEED pushbutton to select the desired speed.

i. Push and hold the MODE pushbutton switch. The demodulation modes will be scrolled on the display above the switch. Release the MODE switch when the desired mode is displayed.

j. Push and hold the BW (bandwidth) pushbutton switch. The available filters for the selected mode will be scrolled on the display above the switch. Release the switch when the desired bandwidth is displayed.

k. Push and release the LOAD pushbutton switch.

NOTE

This concludes the entry procedure for the auxiliary channel. To use the channel, press and release the RECALL pushbutton switch when the receiver is in the receive mode.

3.6 PROGRAMMED RECEIVER OPERATION

The programmed Receiver can be used for channelized operation, channel scanning, or group scanning. Scanning and other channelized operations are described in the following procedures.

3.6.1 Standard (Non-scanning) Channelized Operation

When the Receiver is in the receive mode, channels can be called up individually or manually scanned. To call up a channel:

- Push and release the CHANNEL pushbutton switch.
- Using the keypad, enter the desired channel number.
- Press and release the ENTER pushbutton switch.

The display will update to the parameters for the desired channel and the receiver will tune to the selected frequency.

To manually scan channels:

- Push and release the CHANNEL pushbutton switch.
- Push and release the TUNE ENABLE pushbutton switch. The LED adjacent to the key will be lit.
- Use the tuning wheel to scan all programmed channels.

3.6.2 Automatic Scanning

The programmed Receiver will scan all or a selected group of programmed channels automatically. The first procedure below sets up the Receiver to incrementally scan a block of channels and the second procedure puts the Receiver in the group scanning mode. For all scanning operations, the dwell time should be preset. The dwell selects the length of time the Receiver will monitor each channel before proceeding to the next. See figure 3-3 for dwell time selection.

3.6.2.1 Channel Scanning Procedure

STEP	ACTION
a.	Push and release the SCAN pushbutton switch. The LED above the switch will light and prompt GROUP OR CHANNEL SCAN? will appear in the alphanumeric display.
b.	Push and release the CHANNEL pushbutton switch. The LED adjacent to the switch will light, the prompt FIRST CHANNEL? will appear on the alphanumeric display and first channel of a previously scanned group will be displayed.
c.	Using the keypad, enter the lowest channel number in the block to be scanned.
d.	Push and release the ENTER pushbutton switch. The prompt LAST CHANNEL? will appear on the alphanumeric display.
e.	Use the keypad to enter the highest channel number in the group of channels to be scanned.

f. Push and release the ENTER pushbutton switch.

3.6.2.2 Group Scanning Setup Procedure

STEP	ACTION
a.	Press and release the SCAN pushbutton switch. The LED above the switch will light and the prompt GROUP OR CHANNEL SCAN? will appear on the alphanumeric display.
b.	Push and release the GROUP pushbutton switch. The prompt GROUP NUMBER? will appear on the alphanumeric display.
c.	Use the keypad to enter the single digit group number (0 - 9) in the group display.
d.	Push and release the ENTER key. The Receiver will start to scan the channels in the selected group in the order that they were originally entered. If the selected group was not programmed the prompt ANOTHER GROUP? will appear on the alphanumeric display.

3.6.2.3 Terminating the Scan Function

Group or channel scanning can be stopped by:

- Pressing and releasing the SCAN button. Press and release the button a second time to restart the scan.
- Pressing and releasing the TUNE ENABLE pushbutton switch

3.7 REMOTE OPERATION

The Receiver can be used in remote applications. Remote or local control is front panel selectable. The remote pushbutton switch is located above and just to the left of the tuning knob. The switch toggles the receiver between remote and local control. When the Receiver is in the remote mode, the LED adjacent to the switch is lit and all other front panel controls are locked out. To take the Receiver out of the remote mode, push and release the REMOTE pushbutton switch.

SECTION 4

TECHNICAL DESCRIPTION

4.1 INTRODUCTION

This section includes a general overview of Receiver operation and a comprehensive circuit description.

Included in the general Receiver overview are the following items:

- A Receiver signal path simplified block diagram
- A Receiver gain distribution chart

More extensive block diagrams, circuit descriptions, schematics, parts lists, and test procedures for each subassembly are contained in the unit instruction sections.

4.2 RECEIVER OPERATION

4.2.1 Receiver Signal Path

The information presented in this section details the signal processing in the receiver signal path from antenna RF input to audio output. The RF input range is from 14 kHz to 29.99999 MHz. A dual conversion scheme is employed, with a first intermediate frequency (IF) of 40.455 MHz and a second intermediate frequency (IF) of 455 kHz.

A variable first local oscillator (LO No. 1) of 40.469 to 70.455 MHz is employed for the first conversion to 40.455 MHz while a fixed second local oscillator (LO No. 2) at 40.000 MHz is employed for the second conversion to 455 kHz.

The primary RF signal path crosses the following assemblies:

- Preselector Assembly A19
- Input Filter Assembly A1
- First Converter Assembly A2
- Second Converter Assembly A3
- IF Filter Assembly A4
- IF/Audio Assembly A5

Additionally, Meter Board Assembly A13A3 provides monitoring capabilities, and the ISB IF/Audio Assembly, A18, provides ISB operation capabilities.

The following brief circuit descriptions follow figure 4-1, Simplified Receiver Block Diagram. A Receiver Gain Distribution Chart, figure 4-2, has also been included.

4.2.1.1 Preselector Assembly A19 and Input Filter Assembly A1

The RF signal picked up by the antenna and injected into the Receiver via J1 is introduced to the Preselector Assembly A19. The assembly offers filtering and overload protection. Automatically tuned bandpass filtering is used for signals between 2 and 29.99999 megahertz, and lowpass filters are switched into the circuit for signals below 2 megahertz. The bandpass filters provide attenuation for signals 10% above or below the tuned frequency. The filter networks are bypassed when the receiver is operating in the scan mode.

The signal from the preselector is applied to Input Filter Assembly A1. This assembly contains low pass filtering to provide more than 100 dB of rejection to undesired signals at input frequencies greater than 30 MHz.

Insertion loss is less than 1/2 dB, with a VSWR less than 2:1. Receiver input overload protection circuitry (up to 70 Vrms overload), muting, Built-In Test Equipment (BITE) detection, and BITE signal generation functions are also included.

4.2.1.2 First Converter Assembly A2

First Converter Assembly A2 accepts the 14 kHz to 29.99999 MHz output from the A1 assembly and subtractively mixes with the first LO (40.469 to 70.455 MHz) to produce a first IF of 40.455 MHz. (Note that sideband inversion occurs during the mixing process.) Filtering is utilized at 40.455 MHz before the first IF is directed to the Second Converter Assembly A3. Input signal levels of typically -120 to + 10 dBm are gain controlled by an AGC signal which provides up to 20 dB of gain reduction. Typical conversion loss through the assembly is 0 dB.

A BITE detector operating at 40.455 MHz monitors the operation of the assembly.

4.2.1.3 Second Converter Assembly A3

Second Converter Assembly A3 converts the first IF of 40.455 MHz to a second IF of 455 kHz through subtractive mixing with the second LO frequency of 40.000000 MHz.

Filtering occurs at both IF frequencies. Overall module gain is approximately 13 dB and gain reduction of up to 20 dB is controlled by an AGC voltage.

A BITE detector operating at 455 kHz monitors the operation of the assembly.

4.2.1.4 IF Filter Assembly A4

IF Filter Assembly A4 accepts the second IF from the A3 assembly and provides the selection of one of up to eight filters for signal processing. (ISB operation requires selection of two filters.) The main signal frequency selectivity is determined by these filters. Module gain is + 10 dB. An unfiltered 455 kHz signal output is tapped off and applied to a rear panel connector for external demodulation or monitoring purposes. The two main signal outputs from the A4 assembly are:

- The normal 455 kHz second IF to the A5 IF/Audio assembly, (for AM, CW, FM, USB, or LSB operation).
- ISB (LSB) output to the A18 ISB IF/Audio assembly (for ISB operation).

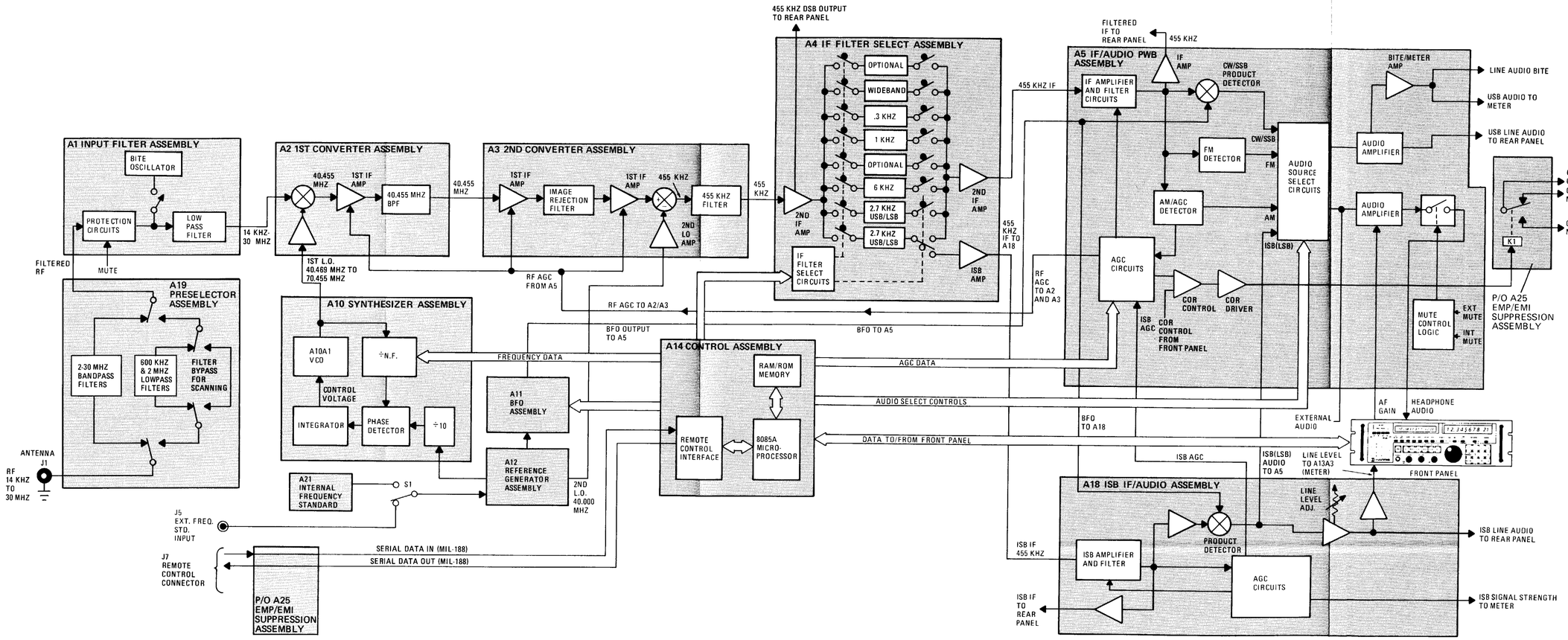


Figure 4-1. Receiver Signal Path Block Diagram

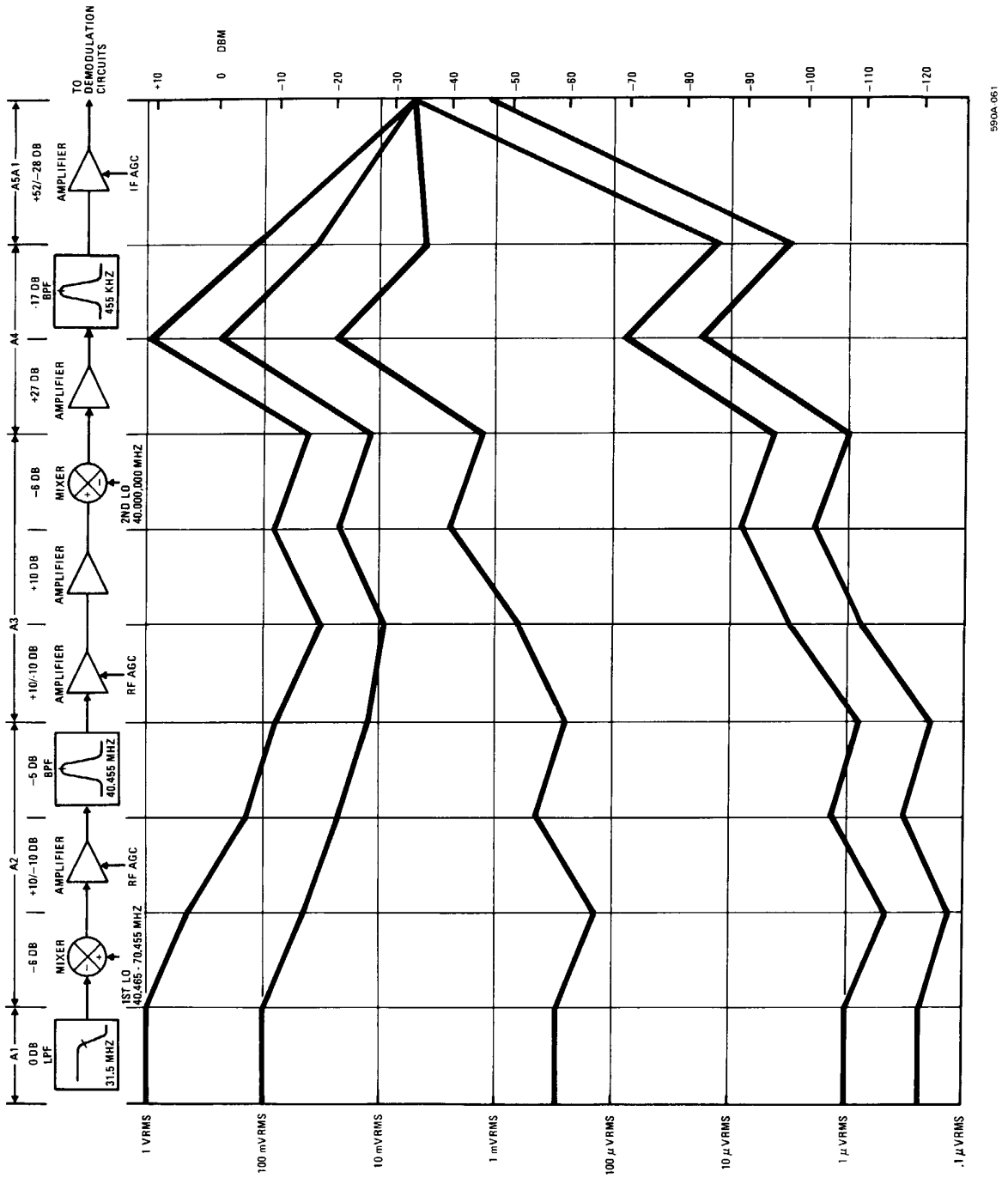


Figure 4-2. Receiver Gain Distribution

4.2.1.5 IF/Audio Assembly A5

The primary functions of the IF/Audio Assembly A5 are to:

- Amplify and filter the 455 kHz IF signal
- Detect the audio signal
- Select the audio signal
- Develop and Integrate IF and RF AGC signals

The gain of the IF amplifier section is controlled over a 90 dB dynamic range by the AGC circuit. The amplified and filtered IF signal is applied to the SSB/CW, FM, and AM detectors to recover the audio components of the signals. The outputs of these detectors is applied to the audio select switch along with the ISB audio signal. The audio select switch is controlled by signals sent from the A14 assembly and closes the signal path for between one of the audio inputs and the audio amplifiers. The selected audio is amplified, filtered, and sent to the Carrier Operated Relay (COR) on the A25 assembly, headphones and audio outputs on the rear panel. An external audio signal can be injected into the audio path via the rear panel. Gain of the headphone audio amplifiers is controlled directly by the AF GAIN knob on the front panel.

The AGC circuit integrates inputs from the ISB audio AGC, external AGC, and RF GAIN control to develop outputs for the dual loop control system that adjusts the RF and IF gains to maximize receiver performance. The attack time of the AGC is set (less than 20 ms for slow, medium, and fast; less than 10 ms for data), but the decay characteristic is front panel selectable for slow, medium, fast or special data operation.

4.2.1.6 ISB IF/Audio Assembly A18

ISB IF/Audio Assembly A18 is used when simultaneous LSB and USB is required. A18 operation is virtually identical to A5 operation, except that the A18 assembly contains only one demodulator circuit (the ISB product detector). A 455 kHz ISB IF output and an ISB line audio output are provided on the rear panel.

4.2.1.7 Meter Board A13A3

Meter Board A13A3 contains the circuitry and switches required to monitor selected RF and AF signals. The following signals may be monitored on the front panel meter via front panel switch controls:

- USB-RF
- USB-AF
- LSB-RF
- LSB-AF

(Note that in ISB operation, the ISB channel is monitored in the LSB switch mode.)

Meter drive signals originate on IF/Audio Assembly A5. (ISB signals originate on ISB IF/Audio Assembly A18). The meter itself is calibrated in microvolts rms or mVrms for RF signal strength and dBm/600 ohms for AF line level.

4.2.2 Synthesizer, BFO, Front Panel, and Control Assemblies

The Front Panel Assembly is the interface between the operator and the Receiver. It is the point of entry for operating instructions, such as frequency, bandwidth, mode, etc. and it is where operating parameters and fault codes are displayed. The front panel entries are read by the Control Assembly A14. The Control Assembly in turn calculates the first local oscillator (L.O.) and the beat frequency oscillator (BFO) frequencies and writes the data to the Synthesizer and BFO assemblies respectively. The Synthesizer assembly generates the first L.O. signal and the BFO assembly generates the signal that is mixed with the second IF to detect the audio when receiving in the SSB mode. It should be noted that the first L.O. frequency can be calculated by adding the receive frequency to the first intermediate frequency of 40.455 MHz. When the receiver is tuned to 2000.000 kHz, the first L.O. frequency will be 42.455 MHz.

4.2.3 Frequency Synthesizer Assembly A10

The Frequency Synthesizer Assembly, A10, generates the first local oscillator (L.O.) signal used to tune the Receiver to the desired operating frequency with a 1 Hz resolution. The 40.469 MHz to 70.455 MHz signal is mixed with the incoming RF signal to produce the first IF. The first L.O. signal is generated by a voltage-controlled oscillator that is part of a fractional divide-by-N.F phase-locked loop (PLL). The VCO and the other parts of the PLL are discussed in depth in the A10 unit instruction section.

4.2.4 BFO Assembly A12

The BFO assembly is a frequency synthesizer that operates around 455.000 kHz. The output is injected into the SSB/CW product detector on the A5 assembly. The BFO can be offset ± 10 kHz via front panel per front panel entries.

4.2.5 Control PWB Assembly A14

The Control Assembly A14, is the functional control center of the Receiver. All logical decisions are made on this assembly. The assembly features:

- An 8085A microprocessor
- An EPROM to store the program
- A RAM used as a scratch pad and for semi-permanent storage of operating parameters
- A remote control interface
- Serial and parallel ports to interface the microprocessor with other assemblies in the receiver

The Control Assembly monitors, controls, and tests most functions of the Receiver in response to inputs from the front panel, or a remote source, and instructions resident in the EPROM. The remote control interface will support RS-232 and MIL-188 serial data formats operating at most common baud rates between 50 and 19,200 bps. Built-in fault protection guards against power transients and losses. A backup battery keeps the RAM alive when power to the unit is interrupted. The circuits of the Control assembly are described in detail in the A14 unit instruction section.

4.3 CONVERSION BETWEEN dBm AND Vrms

Power levels in this manual are stated in dBm, or decibels with respect to 1 milliwatt. For example, + 6 dBm means 6 dB more than (above) 1 mW, or 4 mW. Similarly, -6 dBm is 6 dB less than (below) 1 mW, or 0.25 mW (250 uW). Notice that every value of dBm corresponds to a particular amount of power. If the impedance in

which this power is dissipated is known, the corresponding voltage and current can be determined. Table 4-1 lists 50 ohm voltage equivalents for many dBm power levels. Note that for negative values of dBm, voltages are read in either of the two left-hand columns. For positive values of dBm, voltages are read in the right-hand column. For instance, -6 dBm is 0.112 V (112 mV), across 50 ohms, while + 6 dBm is 0.446 V. Similarly, -20 dBm equals 22.4 mV, while + 20 dBm equals 2.24 volts (across 50 ohms).

Table 4-1. Conversion of dBm to Vrms across 50 ohms (0 dBm = 1 mWatt)

(Negative dBm)		dBm	(Positive dBm)
Volts	Millivolts		Volts
.224	224	0	.224
.199	199	1	.251
.178	178	2	.282
.158	158	3	.316
.141	141	4	.354
.126	126	5	.398
.112	112	6	.446
	99.9	7	.501
	89.0	8	.562
	79.3	9	.630
	70.7	10	.707
	63.0	11	.793
	56.2	12	.890
	50.1	13	.999
	44.6	14	1.12
	39.8	15	1.26
	35.4	16	1.41
	31.6	17	1.58
	28.2	18	1.78
	25.1	19	1.99
	22.4	20	2.24
	19.9	21	2.51
	17.8	22	2.82
	15.8	23	3.16
	14.1	24	3.54
	12.6	25	3.98

Table 4-1. Conversion of dBm to Vrms across 50 ohms (Cont.)
(0 dBm = 1 mWatt)

(Negative dBm)		dBm	(Positive dBm)
Volts	Millivolts		Volts
	12.0	25.41	4.17
	11.2	26	4.46
	10.0	27	5.01
	8.90	28	5.62
	7.93	29	6.30
	7.07	30	7.07
	3.98	35	12.6
	2.24	40	22.4
	1.26	45	39.8
	0.707	50	70.7

SECTION 5

MAINTENANCE

5.1 INTRODUCTION

Section 5 contains information concerning general repair, Built-In Test Equipment (BITE) description and fault code chart, overall receiver performance tests, and component data.

5.2 PWB REPAIRS

The following general rules and techniques are useful in servicing printed circuit boards.

- When replacing components on printed wiring boards (PWB), clip the mounting leads with a suitable pair of diagonal cutters and remove the component. This is especially helpful on multilead components such as the dual in-line and circular type integrated circuits. The individual leads are then removed from the PWB with a low wattage iron.
- Before removing an integrated circuit from a PWB, note orientation of the pin locating tab and make sure the replacement component is reinstalled in exactly the same way.
- Because of the double sided construction used on many of the PWBs in the Receiver, a component lead may be soldered to printed circuit areas on the top and bottom of the PWB. Consequently, when a component lead is removed, the replacement component should be resoldered top and bottom as applicable.
- Overheating a printed circuit conductor may cause it to pull loose from the board material. Apply only the minimum amount of heat necessary for component removal or replacement. The use of a soldering iron in the 25- to 35-watt range is recommended.
- A desoldering tool (solder-sucker) is very convenient (and minimizes board damage) when removing multilead components which cannot be cut loose with diagonal cutters. Components of this type include special PWB transformers mounted on solderable leads and double balanced mixers, both used extensively in the various assemblies.
- A convenient device to use in place of a solder-sucker is a roll of Solder-Wick, manufactured by Solder Removal Co., Covina, California. This flux-saturated copper braid is often more effective than a solder-sucker for removing solder from PWBs.

5.3 MOSFET REPLACEMENT

When handling and replacing Metal-Oxide Semiconductor Field-Effect Transistor (MOSFET) devices, the following three (3) steps should be performed.

a. Remove new MOSFET from package. The four leads will be connected together with a small ferrule or wire to prevent static voltage differences from developing between the gate and substrate terminals. If the ferrule is present, wrap several turns of small solid wire around the leads and then remove the ferrule.

b. Position the four leads and carefully install the MOSFET on the PWB.

c. Remove the jumper(s) only after the leads have been soldered.

5.4 CMOS HANDLING AND REPLACEMENT

All Complementary Offset Symmetry Metal-Oxide Semiconductor (CMOS) devices have diode input protection against adverse electrical environments such as static electricity.

Although the devices contain circuitry to protect inputs against damage due to high voltages or electrical fields, precautions should be taken to avoid application of any voltage higher than maximum rated voltages.

Unfortunately, severe electrical conditions can develop during the process of handling. For example, static voltages generated by a person walking across a common waxed floor have been measured in the 4 to 15 kV range. This depends to a great extent upon the humidity, surface conditions, friction, and other factors. These static voltages are potentially disastrous when discharged into a CMOS input, considering the energy stored in the human body at these voltage levels.

Present CMOS gate protection structures can generally protect against overvoltages. However, these same structures will break down under severe conditions such as described above. The following are some suggested handling procedures for CMOS devices, many of which apply to most semiconductors.

- All CMOS devices should be stored or transported in materials that are conductive. CMOS devices must never be inserted into conventional plastic packing material or plastic trays.
- Avoid contact with the leads of the device. The component should always be handled very carefully by the ends or the side opposite the leads.
- Avoid contact between printed wiring board circuits or component leads and synthetic clothing while handling static sensitive devices or assemblies containing them.
- Do not insert or remove CMOS devices when power is applied. Check all power supplies to be used for testing CMOS devices to be certain that the voltage and polarity are correct, and that no transients are present.
- Use only soldering irons and tools that are properly grounded. Ungrounded soldering tips will destroy these devices. Never use soldering guns.

NOTE

When replacing CMOS devices in a PWB, it is recommended that the same procedures for replacing MOSFET devices be followed.

5.5 BUILT-IN TEST EQUIPMENT (BITE) SELF-DIAGNOSTICS

The Receiver has the capability of extensive self-testing in the event of a failure. The general types of tests and the assemblies affected are as follows:

a. Control circuit tests
   - Control Assembly A14
   - Driver Assembly A13A2
   - Display Assembly A13A4 and A13A5

b. Frequency Synthesizer tests
   - Reference Generator A12 and Frequency Standard A21
   - BFO Assembly A11

- Synthesizer Assembly A10

c. Signal Path tests

- Input Filter Assembly A1
- First Converter Assembly A2
- Second Converter Assembly A3
- IF Filter Assembly A4
- IF Audio Assembly A5

d. Power Supply tests

- Power Supply Assembly A15

Most of these tests can be automatically performed by momentarily pressing the TEST button located on the Receiver's front panel. Once the TEST button has been pressed, all receiver front panel controls (except AF GAIN, SPEAKER, and AUDIO LINE LEVEL) become inoperative, and the signal overload relay located on the A1 assembly deenergizes to prevent any possible spurious radiation of test signals during BITE diagnostics.

The normal length of the self-test is approximately 5 seconds. All tests are performed sequentially.

If it is determined that a fault exists in a particular assembly, that assembly number and the corresponding fault code number defining the type of failure will be displayed on the Receiver's front panel alphanumeric display. (See table 5-1 for a listing of assembly numbers and fault codes.) For example if the reception of LSB signals became difficult (due to unknown reasons), initiate self-test by pressing TEST. The display, Assy 04 FAULT "02", would probably be shown. Table 5-1 indicates that this would be a fault due to IF Filter Assembly A4 LSB Filter.

NOTE

Section 5.6 is a listing of faults which may not be directly identified by Receiver BITE Diagnostics. These symptoms should be checked before undertaking any module level repair operation.

Table 5-1. Fault Code Listing

Assembly Number	Fault Code	Description
A1	1	Antenna Overload
	2	Relay Fault (Closed)
	3	BITE Oscillator or A1 RF Det.
	4	Front End Filter
	5	Relay (Open) or dc Det. (TP5)
A2	1	A2 Detector

Table 5-1. Fault Code Listing (Cont.)

Assembly Number	Fault Code	Description
A3	1	A3 Detector
A4	1	Bypass Signal Path Fault
	2	LSB Filter
	3	USB Filter
	4	CW Filter
	5	CW Filter
	6	Special Filter - Slot 5
	7	Special Filter - Slot 6
	8	Special Filter - Slot 7
	9	A5 IF Input peak Detector or A4 IF Amplifier and Output Circuitry
A5 *See Note	1	A5 Gain
	2	AM Detector
	3	Line Audio
	4	Product Detector
	5	FM Detector
A10	1	Serial Data
	2	Synthesizer Out-of-Lock
A11	1	Serial Data
	2	BFO PLL Out-of-Lock
A12	1	1 MHz Reference
	2	800 kHz Reference
	3	40 MHz PLL Out-of-Lock
A13	--	No Fault Codes (Converter Module)
A14	1	PROM Failure
	2	8155 RAM Failure
	3	CMOS RAM Failure
	4	Serial Data
	5	8155 Output Port Failure
	6	8255 Output Port Failure
	7	A/D Conversion Timing Test
	8, 9	A/D Converter Result Test
A15	--	No Fault Codes (Linear Power Supply)
A17 (Optional)	1	LCU PROM
	2	LCU Communication
	3	LCU Interface
A18 *See Note	1	A18 Peak Detector or A4 Output Failure
	2	A18 AGC Level Test
	3	A18 Line Audio Detector

*Note: Certain faults may be indicated if the associated audio line level is set too low. If a fault level is indicated, adjust the appropriate front panel line level control for 0 dBm output and repeat the test.

If initiating the self-test function results in no faults (radio completely functional), the following front panel message would be displayed, --- TEST PASSED ---.

5.5.1 Continuous Self-Test Monitoring

Certain critical circuits that may adversely affect receiver operation, or even cause physical damage if they malfunction, are continuously monitored by the self-diagnostics. These circuits are as follows:

a. Power Supply A15. All power lines distributed to the receiver are continuously monitored for acceptable voltage limits.

b. RF Input or Antenna Overload. The signal presented to the Receiver from the antenna is constantly monitored so that signal path shut down circuits will protect the Receiver from an input signal greater than approximately 1.5 V_{rms}.

c. The Synthesizer Phase Lock Loop (PLL). The PLL is continually monitored for a locked condition, ensuring that the receive frequency's stable and correct.

Any of the above mentioned items will cause a front panel FAULT LED to illuminate. Additionally, the RF signal overload would result in a front panel display of ANTENNA OVERLOAD.

5.5.2 Self-Diagnostic Operation

The self-diagnostic tests are a series of sequential tests and measurements used to verify the proper operation of the Receiver. They are described in the following paragraphs. It may be necessary to consult the specific circuit schematics under discussion. These schematics are in the assembly subsections.

5.5.2.1 Lamp Test

The first test performed is a lamp test. All LEDs and segments of the 10-character and 20-character displays located on the front panel are lit. This condition is maintained for approximately 4 seconds for the operator to examine all front panel indicators and while the remainder of the receiver testing is being accomplished.

5.5.2.2 ROM Test (Assembly A14)

ROM test of Control Assembly A14 is the next test performed. U5 contains all the firmware used to control the main Receiver functions and is tested to determine that the information contained is correct. If it is found to have a problem, the corresponding fault message will be displayed on the front panel. If this fault is displayed, a factory replacement should be obtained. This device is factory programmed and cannot be repaired in the field.

5.5.2.3 RAM Test (Assembly A14)

The next test to be performed is the RAM test. This test will determine the read/write capability of the CMOS RAM (U8) and RAM of the 8155 (U7) located on Control Assembly A14. If it is determined that a fault exists, then the appropriate fault message will be displayed on the front panel.

5.5.2.4 I/O Port Tests

Parallel output ports of the A14 assembly are tested next. Output bit patterns are written to U7 and U9 ports, and then read back by the microprocessor to check the data bus path to these devices. If the bit pattern readback is not the same as written, a fault is noted.

5.5.2.5 Serial Data Test

The operation of the parallel-in/serial out shift registers (U17, U18) on the Control Assembly and the capability of the synthesizer and BFO to accept serial data from the Control Board will now be tested. If the synthesizer or BFO fails to receive data correctly, then that assembly will be identified as having failed. If both fail, then it will be assumed that the Control Board is the faulty assembly.

The synthesizer is loaded with all zeros and tested. It's then loaded with 00000000 00000000 001 binary. The one (1) bit will set the serial check line (SW1) of the synthesizer to logic 1. This bit is then tested. If a fault occurs, the appropriate fault message will be displayed on the front panel.

5.5.2.6 Reference Generator Test (Assembly A12)

Reference Generator Assembly A12 will be tested next. The 40 MHz lock bit is read and tested for a lock condition (0 = lock). If detected as being out-of-lock, the proper fault code and assembly number will be displayed on the front panel.

The 1 MHz and 800 kHz detect lines are now read and if a logic 1 is read (indicating a fault), the appropriate fault code and the appropriate assembly number are displayed on the front panel.

5.5.2.7 A/D Converter Tests

The analog-to-digital converter used in the remaining BITE tests is now tested. A conversion is made to confirm that a result is available in approximately 100 microseconds (as indicated by the end-of-conversion output line). Readings are also obtained from two A/D channels tied to the + 5 V and ground reference points, respectively. The conversion result bounds are checked. Failure of any of these three tests causes an A14 fault to be indicated.

5.5.2.8 Phase Locked Loop (PLL) Tests

The BFO PLL and the synthesizer are now tested to ensure that they can be tuned over their entire range. This testing is done in three steps. These three steps are shown in table 5-2.

Table 5-2. BFO Tuning Range

Range	Receiver Frequency	BFO Frequency
LOW	00,000.000 kHz	9.99 kHz
MID	15,050.500 kHz	0.00 kHz
HIGH	29,999.999 kHz	-9.99 kHz

At each frequency, the BFO and synthesizer PLLs are tested to determine the status of their respective lock lines. If a fault occurs as a result of these tests, the appropriate fault code and assembly number are displayed on the front panel.

5.5.2.9 Input Filter Test (Assembly A1)

Input Filter Assembly A1 will be tested next. This is done by testing the relay, the BITE oscillator, and front end filter.

First the input is tested for an overload condition. If an overload exists, then the test is terminated and an antenna overload message is displayed. If no overload exists, testing is continued.

The antenna relay is tested by energizing the relay, passing dc through it, and sampling the A1 dc detector to ensure that the signal path is complete. Sampling the A1 detector output (as well as the A2, A3, and A5 detector outputs) is done by an analog to digital converter (A/D) located on Control Board Assembly A14.

If this test fails, there will not be an immediate fault. The result is saved for future use during this test. The relay is then turned off using the relay control line and the BITE detector level is again tested. If a signal is still present, then the problem is in the relay or its associated control circuitry. If this is the case, a fault is reported indicating a relay failure.

If a fault condition is not detected, an RF test of the A1 assembly is performed by removing the dc relay test signal and activating the 100 kHz BITE Oscillator. The BITE oscillator signal level at the output of the A1 assembly is -20 dBm. The A1 RF detector level is measured. If it is found that the output level is too low then the results of the relay test are checked. If the relay test also failed, then the fault is in the front end filter or the detector line to the A14 assembly. If the relay test passed, then the fault is in either the BITE oscillator or the RF detector. If the RF test is passed and the relay test failed, then the fault is either the relay or the dc detector.

5.5.2.10 First Converter Test (Assembly A2)

After the A1 assembly has been found to be operating correctly, First Converter Assembly A2 is tested. It should be pointed out that the BITE oscillator was left activated from the previous test and will be used as a signal source during the testing of this assembly. The AGC is set to OFF, the RF GAIN is set to maximum and the receiver is tuned to 100 kHz. The A2 DET line is now read by the A/D converter and the results tested to ensure the level is correct. If a fault occurs as a result of this test, the A2 assembly will be flagged as the faulty module and the appropriate fault code will be displayed.

5.5.2.11 Second Converter Test (Assembly A3)

If the First Converter is operating correctly then the Second Converter module is tested. AGC, RF GAIN, and BITE Oscillator are in the same state as used in the testing of the First Converter. Since all conditions are set up, it is only necessary to measure the A3 detector level using the A/D converter and to verify the correct level. If the level is incorrect, the appropriate fault information will be displayed.

5.5.2.12 IF Filter Test (Assembly A4)

After it has been determined that the Second Converter is operating satisfactorily, IF Filter Assembly A4 can be tested. FSK filters will not be tested because of the wide variety of center frequencies and shifts available. The BITE test oscillator located on the A1 assembly will be disabled at this time. A signal generated by the first LO (via signal leakage through the First Converter A2 mixer) will be used. (The first LO signal is used to obtain better frequency accuracy for some of the narrow bandwidth filters that may be present in IF Filter Assembly A4.)

First the 16 kHz bypass path is tested to verify that a signal can be passed through the filter assembly amplifiers to the peak detector located on the input of IF/Audio Assembly A5. The 16 kHz bypass is selected and the level of the peak detector is read by the A/D converter. The results of this test are stored until after the USB filter is tested since, at this time, there could be a problem in either the A4 bypass circuitry or a problem in the A5 input peak detector.

To pinpoint any possible problem, the Receiver will now be tuned to set the first LO to 40.454 MHz. This will generate a 1 kHz USB tone. USB filter (BW2) will be selected and the peak detector output read using the A/D

converter. If a fault exists, then the results of the 16-kHz bypass test will be examined to pinpoint the fault. If the USB filter test passed but the bypass test indicated a fault, then the bypass path is flagged as the faulty circuit. If the USB filter test failed and the bypass path test passed, then the USB filter is identified as the faulty circuit. If both of these tests failed, then the fault is identified as being either the A5 peak detector or the A4 filter amplifiers and their associated circuitry. If the test results indicate that both are operating correctly, then testing the remaining filters installed in the A4 assembly continues.

The LSB filter (BW1) is tested by tuning the first LO to a frequency of 40.456 MHz and enabling the A4 LSB filter slot. A 1 kHz LSB tone is generated, detected by the A5 input peak detector, and measured by the A14 A/D converter. If a fault exists, the LSB filter is identified as the faulty circuit.

Next the CW filter (BW3) is tested. The first LO is tuned to 40.455 MHz and the CW filter is enabled. The level of the peak detector is read by the A/D converter. If the level monitored indicates that a problem exists, then the CW filter (BW3) is identified as being the faulty circuit.

The second CW filter (BW4) is now tested. The same procedure is used to test this filter as was used to test BW3 CW filter. If a problem exists, then this CW filter (BW4) is identified as being the faulty circuit.

Filter slots 5, 6, and 7 may have a variety of filters installed. The only types of filters allowed in these slots are AM, FM, CW, or FSK. Since FSK filters will not be tested and AM, FM, and CW can all be tested at the same frequency, we only need to determine if a filter is present and whether or not it is an FSK type. Testing is identical to that of the CW filters, BW3, and BW4. If a problem exists in any of these filters, the appropriate fault message is displayed.

NOTE

The eight pole dip switch (S2) located on the A14 assembly must be set correctly for the above test to be performed correctly. This switch is set at the factory (based on the filter configuration of the A4 assembly) and should not be altered.

5.5.2.13 IF/Audio Test (Assembly A5)

IF/Audio Assembly A5 is now tested to determine that the SSB, AM, and FM detectors are operating correctly. The A4 filter is set to select the 16 kHz bypass path. The AGC speed Is set to MEDIUM, the mode is set to USB, and the A1 assembly BITE test oscillator is enabled.

The receiver is first tuned to 104.000 kHz. Since the BITE oscillator has a frequency of 100 kHz, a 4 kHz USB tone will result. The second IF AMP GAIN is tested by measuring the AGC voltage through the A/D converter. If the level is incorrect, an AGC fault is displayed on the front panel of the receiver. If this level is satisfactory, then the product detector is tested. The BITE test oscillator is disabled and the receiver is tuned to 4 kHz. The results of this test are stored since there could be a problem in either the line audio circuits or the USB product detector (if a fault indication is detected).

The AM test is now performed. With the Receiver tuned to 4 kHz, the Receiver mode is set to AM. The 16-kHz bypass is again used for this test. To simulate an AM signal, the Receiver will be tuned repetitively from 4 kHz to 100 kHz using LO leakage as a signal source. The line audio level is measured to verify that the AM detector is operational. The results of this test and those of the SSB test are compared to determine where possible faults may have occurred. Table 5-3 shows the results of this test and that of the SSB test.

The next test concerned with the A5 assembly is the FM detector test. The Receiver is set to FM mode and tuned to a frequency of 5 kHz. The Receiver will then be tuned from + 5 kHz to -5 kHz repetitively to simulate

a FM signal using LO leakage as a signal source. The line audio will be read through the A/D converter. If a problem exists, the appropriate fault message is displayed on the front panel of the Receiver.

Table 5-3. AM and SSB Test Results and Fault Locations

AM and SSB Test Results	Fault Location
If AM Passed and SSB passed	No fault
If AM passed and SSB failed	Product detector fault
If AM failed and SSB passed	AM detector fault
If AM failed and SSB failed	Line audio fault

5.5.2.14 ISB IF/Audio Test (Assembly A18)

ISB IF/Audio Assembly A18 is now tested to determine that the IF Peak Detector, ISB AGC, and ISB Line Audio Detector are operating correctly.

Filter Assembly A4 is first set to select the LSB filter. Next, the receiver mode is set to ISB and the RF GAIN is set to maximum. The 100-kHz bite oscillator located on Input Filter Assembly A1 is now activated and the receiver is tuned to 95 kHz (resulting in a LSB frequency of 5 kHz).

Now the ISB Peak Detector level is sampled to determine whether an inband ISB signal has been found (level greater than 1 volt dc). If this level is not found, the frequency of the Receiver is increased 200 Hz and the detector level is checked again. This process is repeated until the correct level is found or until the Receiver frequency is greater than 115 kHz.

If the frequency is greater than 115 kHz, the no inband tone was found so it is assumed that the input peak detector has failed or the signal path between Filter Assembly A4 and the A18 ISB IF/Audio Assembly has been interrupted. If this is true, the fault code for the A18 Peak Detector will be displayed on the Receiver front panel and no further testing of the assembly will take place.

If the inband tone was found, the frequency is increased by 1.5 kHz, placing the tone in the center of the LSB filter.

Once the Receiver is tuned, the peak detector, AGC detector, and line audio detector levels are measured to verify their operation. If any of these are found to be at an improper level, the appropriate fault code will be displayed on the Receiver front panel and all further receiver testing is aborted.

If the three levels are found to be correct, then the assembly is considered to be functioning correctly.

5.5.2.15 LCU Test (Optional Assembly A17, If Installed)

The last thing to be tested during self-test is the Optional FSK Remote Control Assembly A17, if it is used. The information used to control these tests is contained with the FSK remote control assembly firmware. If it is determined that the FSK remote control assembly is installed, the remote control assembly will test the UART, the LCU ROM (U7), and the RS-422 interface. If any of these are found to be at fault, then the corresponding fault information is displayed on the front panel. The LCU also reports, to the remote site, any self-test pass/fail conditions that may occur as a result of the TEST function being performed.

Upon completion of the self-test, if no fault has occurred, a --- TEST PASSED --- message is displayed indicating to the operator that the radio is operating satisfactorily.

5.5.3 Self-Diagnostics Sequence Summary

The self-diagnostics are done in the order of assembly importance. If a fault is discovered during testing, this failure must be corrected before the remaining tests are attempted.

The order of testing from the first to last test is shown in table 5-4.

Table 5-4. Self-Diagnostics Sequence Summary

1.	ROM Test - Assembly A14
2.	RAM Test - Assembly A14
3.	Output Port Test - Assembly A14
	3.1 8155 Ports B, C
	3.2 8255 port A
4.	Serial Data Tests
	4.1 Assembly A14
	4.2 Assembly A11
	4.3 Assembly A10
5.	Reference Generator Tests - Assembly A12
	5.1 40 MHz Phase locked loop
	5.2 1 MHz Reference
	5.3 800 kHz Reference
6.	Phase Locked loops
	6.1 Assembly A10
	6.2 Assembly A11 - BFO PLL
7.	A/D Converter Test - Assembly A14
	7.1 Conversion Timing Test
	7.2 + 5 Reference Measurement
	7.3 Gnd Reference Measurement

Table 5-4. Self-Diagnostics Sequence Summary (Cont.)

8. Input Filter Test - Assembly A1 8.1 Antenna overload test 8.2 Dc Signal test 8.2.1 Relay closed 8.2.2 Relay open 8.3 RF signal test **NOTE** If both tests 8.2.1 and 8.3 fail then it is assumed that the filter is faulty.
9. First Converter Test - Assembly A2
10. Second converter Test - Assembly A3
11. IF Filter Tests - Assembly A4 11.1 16 kHz Bypass Test 11.2 USB Filter Test **NOTE** If both tests 11.1 and 11.2 fail then it is assumed that either the IF amplifier or the A5 assembly peak detector is faulty. 11.3 LSB Filter Test 11.4 CW Filter Test 11.5 CW Filter Test 11.6 Special Filter 5 Test 11.7 Special Filter 6 Test 11.8 Special Filter 7 Test **NOTE** Tests 11.6, 11.7, and 11.8 are done only if filters are installed and if they are not FSK filters.

Table 5-4. Self-Diagnostics Sequence Summary (Cont.)

12.	IF/Audio Test - Assembly A5 12.1 AGC Test 12.2 SSB Noise Test 12.3 SSB Signal Test 12.4 AM Noise Test 12.5 AM Signal Test **NOTE** If both test 12.3 and 12.5 fail then it is assumed that the line audio detector is faulty. 12.6 FM Noise Test 12.7 FM Signal Test
13.	ISB IF/Audio Test - Assembly A18 13.1 Peak Detector 13.2 AGC Test 13.3 Line Audio Detector
14.	FSK Remote Test - Optional FSK Remote Control Interface Assembly A17 (If installed) 14.1 PROM Test 14.2 Communications Test 14.3 Interface Test

5.6 SUPPLEMENT TO BUILT-IN TEST CAPABILITIES

The following are failure modes that may not be directly pinpointed by the receiver self diagnostics sequence. Included are fault indications that may have multiple causes due to module interaction in the radio

5.6.1 Abnormal Front Panel Displays

a. Symptom:
One front panel display is blank, the other display operates normally.

Fault:
A13 Front Panel Assembly.

b. Symptom:
Both front panel displays are blank, with no FAULT LED.

Perform check:
Test for correct power supply voltages at power supply test points.

Fault:
If power supply voltage(s) is bad - A15 Power Supply Assembly.
If power supply voltages are OK - A13 Front Panel Assembly

c. Symptom:
Both front panel displays are blank, with FAULT LED lit.

Perform check:
Pull connector J8 on A14 Control PWB.

Fault:
If FAULT LED goes out - A15 Power Supply Assembly.
If FAULT LED is still on - A13 Front Panel Assembly.

d. Symptom:
Front Panel displays are random, all segments on, and/or locked up with no front panel control.

Fault:
A14 Control PWB

5.6.2 Abnormal Operation, But With No Built-In Test Failure

a. Symptom:
Cannot establish link with Remote Control Unit, but no built-in test failure indicated.

Perform check:
Check A14J19 and A14S3-S5 settings for proper Remote Control Interface configuration.

Fault:
If settings are correct, A14 Control PWB.

b. Symptom:
Severely degraded sensitivity, but no built-in test failure indicated.

Verify Symptom:
Tune receiver to 3.000 MHz, USB mode, AGC off, AF meter function and apply an RF signal of 3.001 MHz at 0.6 uV. If signal is not heard and no meter deflection, perform following check.

Perform check:
Disconnect J1 and J2 from A19 Preselector Assembly and connect together using a male/male type SMB barrel connector.

Fault:
If signal is heard when bypassing preselector - A19 Preselector Assembly.
If signal is still not present - A1 Input Filter Assembly or input coaxes.

c. Symptom:
Unit loses channel memory when turned off for a long period of time, but no built-in test failure indicated.

Fault:
A14 Control PWB

d. Symptom:
No front panel meter functions, but no built-in test failure indicated.

Fault:
A13 Front Panel Assembly.

e. Symptom:
Unit operates normally on internal frequency standard, but faults when on external standard.

Fault:
A12 Reference Generator PWB

5.6.3 Fault Indications With Multiple Causes

NOTE

Verify the presence of correct dc supply voltages on any module which is suspected of having failed.

a. Symptom:
ANTENNA OVERLOAD fault is indicated with no input signal applied.

Perform check:
Disconnect power cable J10 to A19 Preselector Assembly.

Fault:
If fault goes away - A19 Preselector Assembly
If fault still present - A1 Input Filter PWB

b. Symptom:
A12 Reference Generator fault code.

Perform check:
With oscilloscope, test for presence of 1 MHz sinewave with a minimum amplitude of 1.5 $V_{pk\text{-}pk}$ at J9-1 on A12 Reference Generator PWB.

Fault:
If 1 MHz signal not present - A21 Frequency Standard Module
If 1 MHz signal OK - A12 Reference Generator PWB.

c. Symptom:
A2 First Converter fault code.

Perform check:
With no RF input signal and AGC FAST, measure dc voltage on A2J4 pin 1.

Fault:
If A2J4-1 is more negative than -1 Vdc - A5 IF/Audio PWB

Perform check:
With oscilloscope, measure LO input signal level at A2TP3.

Fault:
If no signal at A2TP3 - A10 Synthesizer PWB or coaxial cables between A10 Assembly and A2 Assembly.
If level is approximately 0.5 V_{pk-pk} sinewave - A2 First Converter

d. Symptom:
A4 Fault 09 IF Filter Assembly

Perform check:
Set receiver for USB mode, AGC OFF. Monitor A4TP4 with an oscilloscope and apply a 454 kHz signal at -20 dBm into A4J1 from an external RF generator.

Fault:
If no 454 kHz signal observed at A4TP4 - A4 IF Filter PWB.
If 454 kHz signal at a level of about 0.4 V_{pk-pk} is observed at A4TP4 - A5 IF/Audio PWB.

e. Symptom:
A5 Fault 04 IF/Audio Assembly.

Perform check:
If ISB option (A18) is installed, check for audio output in LSB mode.

Fault:
If LSB Audio is present - A5 IF/Audio Assembly
If LSB Audio is not present - A11 BFO PWB

Perform check:
If ISB option (A18) is not installed, set receiver for USB mode, BFO 0.00 Hz. With oscilloscope, check 455 kHz signal level at A11TP6.

Fault:
If no signal observed at A11TP6 - A11 BFO PWB.
If 455 kHz sinewave of about 0.6 V_{pk-pk} is present at A11TP6 - A5 IF/Audio PWB

5.7 RECEIVER PERFORMANCE TEST PROCEDURES

Table 5-5 shows tests used to verify Receiver operation.

Table 5-5. Test Procedures

Test	Paragraph
Local Control Function Test	2.7
Sensitivity	5.7.1
Audio Output Level and Distortion	5.7.2
AGC Range	5.7.3
IF Filter Selectivity	5.7.4

5.7.1 Sensitivity Test

The following test equipment is required to perform this test.

- HP-8640B Signal Generator
- HP-331A Audio Distortion Analyzer
- 600 Ohm Feedthrough Termination

The following steps describe the sensitivity test procedure.

a. Connect equipment as shown in figure 5-1. Note that when making measurements in the LSB mode, connect the distortion analyzer to J7-17 and J7-18.

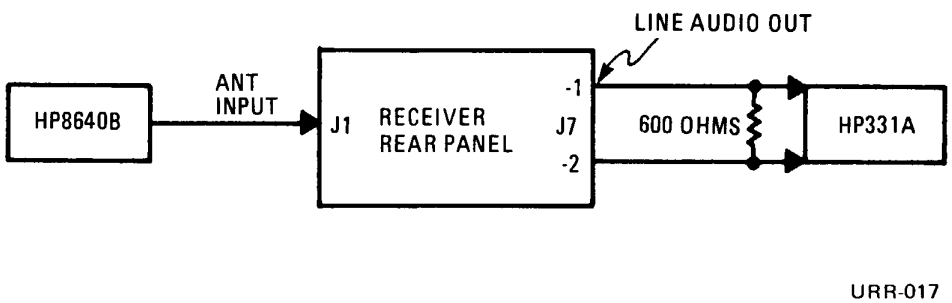


Figure 5-1. Sensitivity Test Setup

b. Initially set Receiver's AGC to OFF and RF GAIN to maximum.

c. Perform steps d through f for each of the modes and bandwidths listed in table 5-6.

d. Set generator for a minimum RF output.

e. Adjust audio distortion analyzer sensitivity for a convenient reference indication.

f. Adjust generator output until the audio output rises 10 dB above the reference noted in step e. Record the signal generator output level in table 5-6. Note that this value must be no greater than the maximum allowable 10 dB S + N/N sensitivity listed.

NOTE

Generator frequencies may be varied within the passband range to obtain a peak audio output in the channel being tested.

NOTE

In AM mode, it will be necessary to set the signal generator for 50 percent modulation at the modulation frequency indicated. Increase carrier power until a 10 dB difference above the reference level is obtained between modulation OFF and modulation ON.

Table 5-6. Sensitivity Test Reports

Mode	BW kHz	Radio Frequency MHz	Generator Frequency MHz	Modulation Frequency kHz	Maximum 10* dB $\frac{S+N}{N}$ Sensitivity uV_{rms}	Measured 10 dB $\frac{S+N}{N}$ Sensitivity uV_{rms}
LSB	2.7	2.100000	2.099000	---	.60	_____
		16.000000	15.999000	---	.60	_____
		29.900000	29.899000	---	.60	_____
USB	2.7	2.100000	2.101000	---	.60	_____
		16.000000	16.001000	---	.60	_____
		29.900000	29.901000	---	.60	_____
CW	.3	2.100000	2.100000	---	.40	_____
		16.000000	16.000000	---	.40	_____
		29.900000	29.900000	---	.40	_____
AM	6.0	2.100000	2.100000	1.0	2.5	_____
		16.000000	16.000000	1.0	2.5	_____
		29.900000	29.900000	1.0	2.5	_____

* 16 dB S + N/N Sensitivity in CW mode only.

5.7.2 Audio Output Level and Distortion Test

The following test equipment is required to perform this test.

- HP-8640B Signal Generator
- HP-331A Distortion Analyzer
- 600-Ohm Feedthrough Termination

Use the following procedures to check line output, headphone output, and speaker output.

5.7.2.1 Line Output Check

To check the line output proceed as follows:

a. Set signal generator to -20 dBm, 2.001500 MHz. Set Receiver to 2.000000 MHz, AGC to MED (medium), MODE to USB, and RF GAIN to maximum.

b. Connect equipment as shown in figure 5-2.

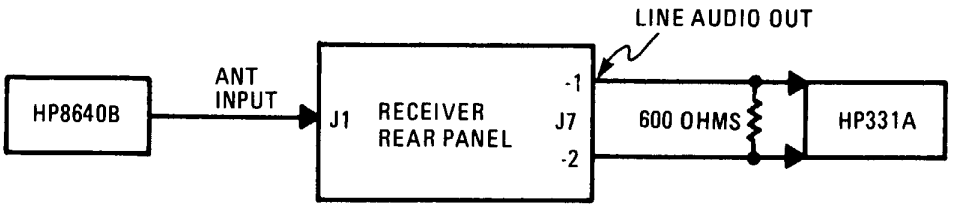


Figure 5-2. Line Audio Test Setup

c. Measure line audio output level. Level must be adjustable line audio control from -16 dBm (.123 V_{rms}) to + 15 dBm (4.24 V_{rms}) (0.25 mW to 30 mW). Record range in table 5-7.

Table 5-7. Audio Output Level and Distortion Test Report

Test	Output Level Measured V_{rms}	Output Level Limits V_{rms}	Percent Distortion Measured	Distortion Limits %
Line Audio		.123 to 4.24 Minimum		5
Headphone Audio		4.24 Minimum		5

d. Set the line audio level to 4.24 V_{rms}.

e. Use the SET LEVEL control on the distortion analyzer to set its reading to 100%.

f. Select its distortion analyzer function, and null out the audio tone using the BALANCE and frequency adjustments.

g. Adjust the meter scale, and read the total harmonic distortion (THD) in percent. The THD must be less than 5%. Record the value in table 5-7.

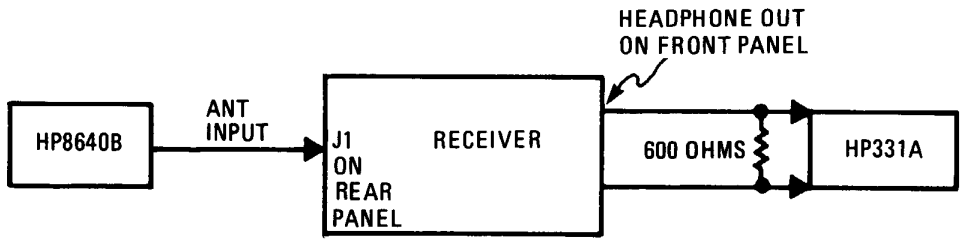
h. Reset the line audio level to 0.775 V_{rms} (0 dBm). Check that the receiver's front panel meter indicates 0 dBm ± 2 dB.

5.7.2.2 Headphone Output Check

To check the headphone output proceed as follows:

a. Set signal generator to -20 dBm, 2.001500 MHz. Set Receiver to 2.000000 MHz, AGC to MEDIUM, Mode to USB, and RF GAIN to maximum.

b. Connect equipment as shown in figure 5-3. Use a jack with a 600-ohm load to plug into the headphone output.



590A-057

Figure 5-3. Phone Audio Test Setup

c. Adjust AF GAIN control for maximum output. Headphone output level must be 4.24 V_{rms} (30 mW) minimum. Record in table 5-7.

d. Measure Total Harmonic Distortion at 4.24 V_{rms} output. THD must be less than 5%. Record in table 5-7.

e. Readjust AF GAIN to minimum.

5.7.3 AGC Range

The following test equipment is required to perform this test.

- HP-8640B Signal Generator
- HP-331A Audio Distortion Meter
- 600 Ohm Feedthrough Termination

Use the following procedures to perform the AGC range test.

a. Connect equipment as shown in figure 5-4.

b. Set signal generator to 10.001500 MHz and RF output level at 2 uV_{rms}.

c. Set AGC to OFF, Mode to USB, Receive Frequency to 10.000000 MHz, BFO to 0.00 kHz, and MED (medium) adjust Line Audio Output to 0 dBm.

d. Set a convenient reference level on the distortion analyzer, and then increase signal generator output to 0.2 V_{rms}. The audio output level should not increase by more than 3 dB. Record level change below.

Total Audio Output Level Change: _____ dB (3 dB maximum)
(RF input level 2 uV_{rms} to 0.2 V_{rms})

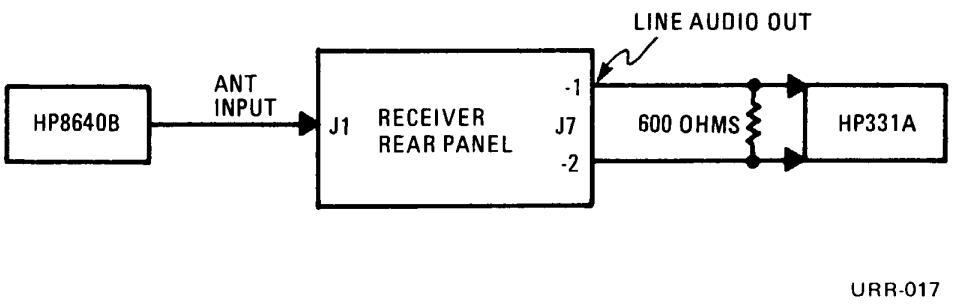


Figure 5-4. AGC Range Test Setup

5.7.4 IF Filter Selectivity

The following test equipment is required for this test:

- HP-8640B Signal Generator
- Boonton Model 91-H RF Millivoltmeter with 50-ohm adapter.
- HP-5383A Frequency Counter

Use the following procedures to verify filter IF response.

a. Initially set Receiver to 10.000,000 MHz, AGC to OFF, BFO to 0.00 kHz, and MODE to USB. Connect equipment as shown in figure 5-5. Note that when measuring the LSB filter the ISB IF output J2 should be monitored instead of J4.

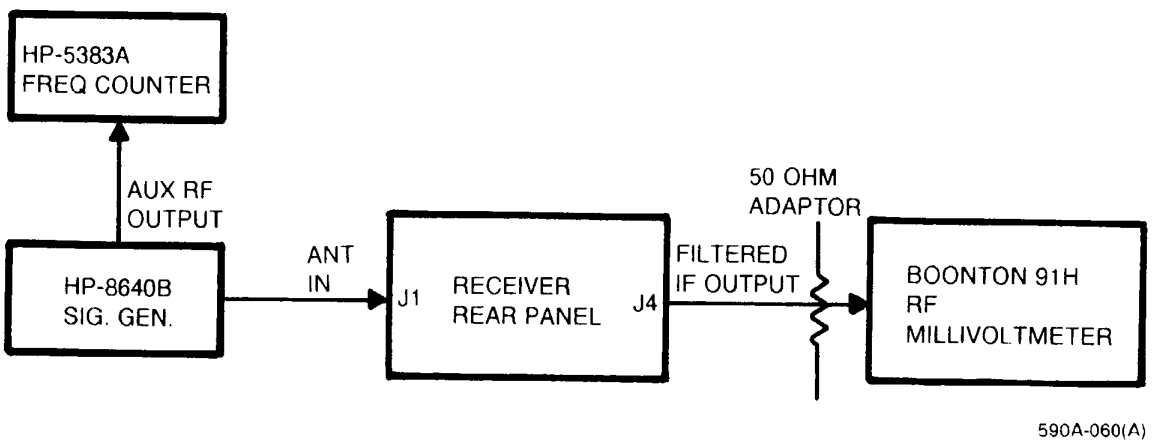


Figure 5-5. IF Filter Selectivity Test Setup

b. Set signal generator frequency f_o to 10.0015 MHz. Adjust generator output to set a convenient millivoltmeter reference level in the generator's -110 dB range (i.e., below the Receiver's AGC threshold).

c. Vary the generator frequency to determine the peak level in the passband.

d. Adjust the generator frequency to determine the values (approximately ± 10 kHz) at which the output level is 3 dB below the level recorded in step (c). Calculate the 3 dB bandwidth as the difference between these frequencies, and record it in table 5-8.

e. Vary the generator frequencies through the range between the -3 dB values determined in step (d). Disregarding the levels at the end points, determine the maximum and minimum levels within this range. Calculate the difference between the maximum and minimum in dB, and record the value in table 5-8.

f. Repeat steps (b) through (e) for the LSB, CW, and AM modes at the generator frequencies given in table 5-8.

Table 5-8. IF Filter Response Test Report

Generator Reference Level Frequency f_o MHz	Mode	Filter Bandwidth, kHz		Passband Ripple	
		(Minimum)	Measured	Maximum dB	Measured dB
10.00150	USB	2.6		3	
9.99850	LSB	2.6		3	
10.0000	CW	.30		3	
10.0000	AM	6		3	

MAIN CHASSIS INTERCONNECTION

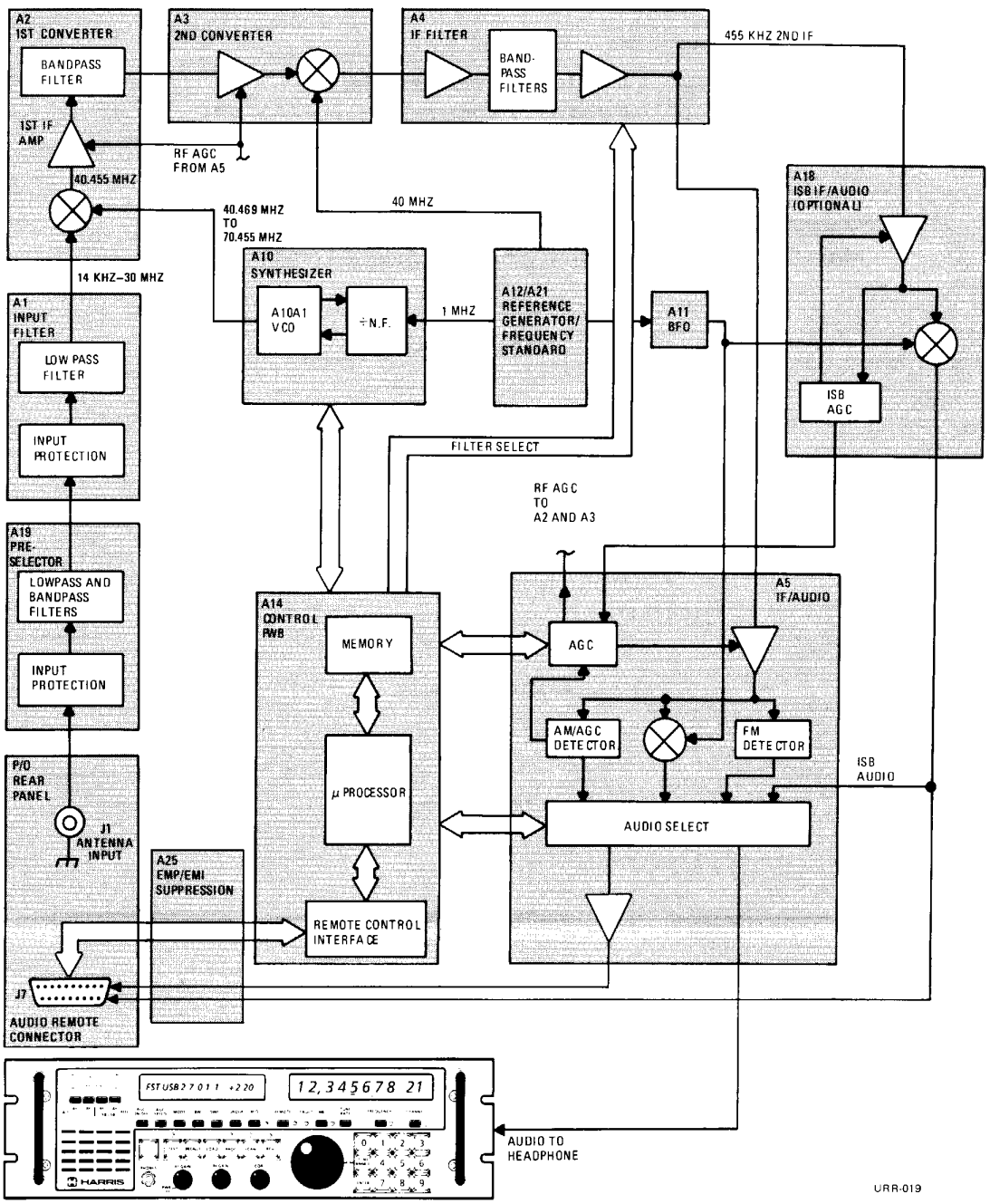


TABLE OF CONTENTS

Paragraph		Page
1.	Introduction	1

LIST OF FIGURES

Figure		Page
1	Main Chassis Top View with A19 and A18 In Place	3
2	Main Chassis Top View with A19 Removed to Expose A2, A3, and A16A2	4
3	Main Chassis Bottom View	5
4	Main Chassis Front View.	6
5	Main Chassis Rear View	7
6	Main Chassis Interconnection Schematic Diagram (10215-1011)	9

LIST OF TABLES

Table		Page
1	Main Chassis, (PL 10215-1010)	1

MAIN CHASSIS INTERCONNECTION

1. INTRODUCTION

This section contains main chassis level information including parts lists, illustrations identifying and locating major assemblies, and an interconnection diagram. All major subassemblies of the main chassis are listed in table 1 and identified in figures 1 through 5. Figure 6 is the main chassis interconnection schematic diagram.

Table 1. Main Chassis, (PL 10215-1010, Rev. K)

Ref. Desig.	Part Number	Description
A1	10073-5100	INPUT FILTER PWB ASSY
A2	10073-5200-02	1ST CONVERTER
A3	10215-5300	PWB ASSY,2ND CON
A4	10073-5500-06	IF FILTER ASSY
A5	10215-5410-02	PWB ASSY,IF/AUDI
A10	10215-4100	PWB ASSY,SYNTHES
A11	10073-4600	BFO PWB ASSY
A12	10073-4700	REF-GEN PWB ASSY
A13	10215-2010	PANEL ASSEMBLY
A14	10215-2800-02	ASSY,CONTROL BD
A15	10073-3000	POWER SUPPLY ASSY
A16A1	10215-1200	PWB ASSY,FRONT P
A16A2	10073-1400	CHASIS POWER DISTRIBUTION
A16A3	10215-1350	REAR PWR DIST ASSY
A18	10215-6300-02	PWB,ISB IF/AUDIO
A19	10215-6600	ASSY,PRESELECTOR
A21	10073-7321	FREQ STD 1X10 7 NAVY
A25	10215-6850	EMP/EMI SUPPR. A
J10	J90-0012-001	COAX ADAPTOR SELECTRO
S1	10073-7245	FREQ. STAND. SWITCH ASSY
W1	10073-7160	CABLE,ASSY,COAX
W2	10073-7161	CABLE,ASSY,COAX
W3	10073-7158	CABLE,ASSY,COAX
W4	10073-7186	CABLE ASSY COAX
W5	10073-7184	CABLE ASSY COAX
W6	10073-7157	CABLE ASSY COAX
W7	10073-7183	CABLE, COAX ASSY
W8	10073-7156	CABLE ASSY COAX
W9	10073-7054	CABLE,RIBBON
W10	10073-7182	CABLE, COAX ASSY
W11	10073-7246	CABLE, AC POWER
W13	10215-7004	CBL ASSY SYN-REF
W14	10215-7005	CBL ASSY SYN-CNT
W17	10073-7069	CABLE ASSEMBLY
W19	10073-7152	CABLE ASSY
W20	10073-7070	RIB CABLE CONT-PAN
W23	10073-7247	SPEAKER CABLE
W24	10073-7055	RIBBON CABLE (MTR CONT)
W26	10073-7056	CABLE,RIBBON

Table 1. Main Chassis, (PL 10215-1010, Rev. K) (Cont.)

Ref. Desig.	Part Number	Description
W30	10073-7191	COAX CABLE ASSY
W31	10073-7192	CABLE ASSY
W34	10073-7066	CABLE, RIBBON
W35	10073-6654	CABLE, RIBBON
W36	10073-7068	CABLE, RIBBON
W37	10073-7187	CABLE COAX
W38	10073-7248	CABLE ASSY
W39	10215-7006	CABLE, COAX, RF IN
W40	10073-7162	COAX CABLE ASSY

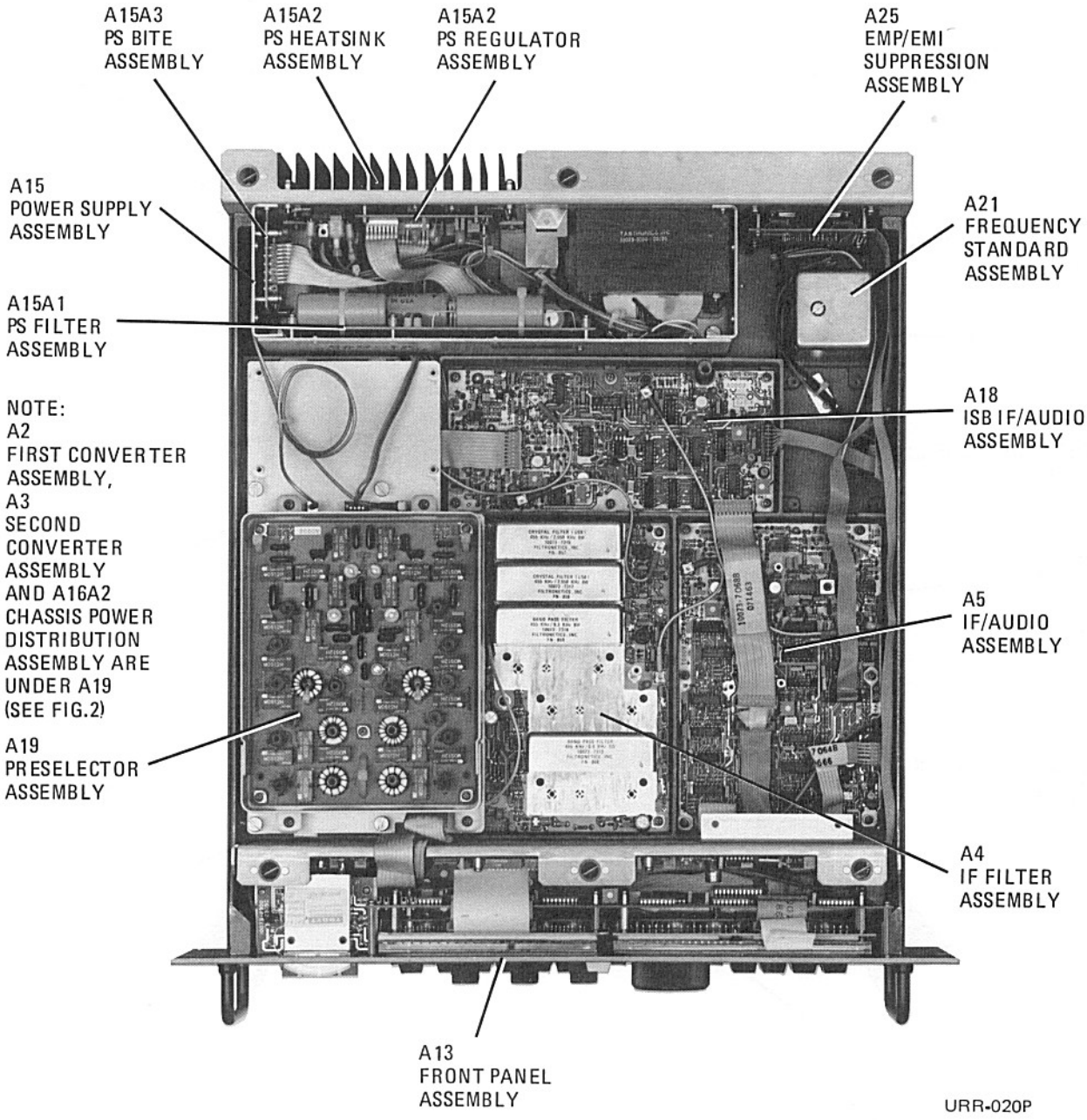


Figure 1. Main Chassis Top View with A19 and A18 In Place

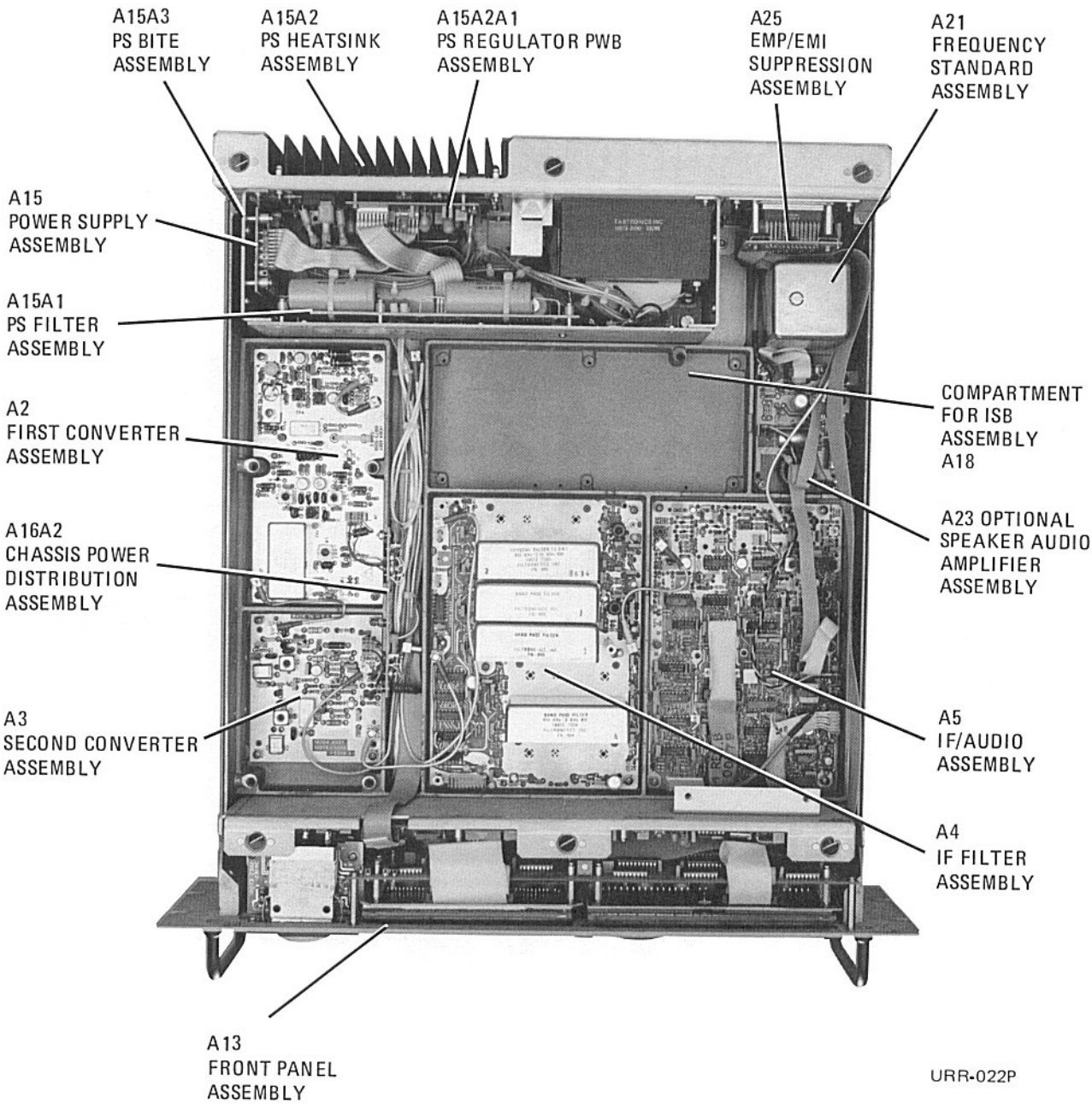


Figure 2. Main Chassis Top View with A19 Removed to Expose A2, A3, and A16A2

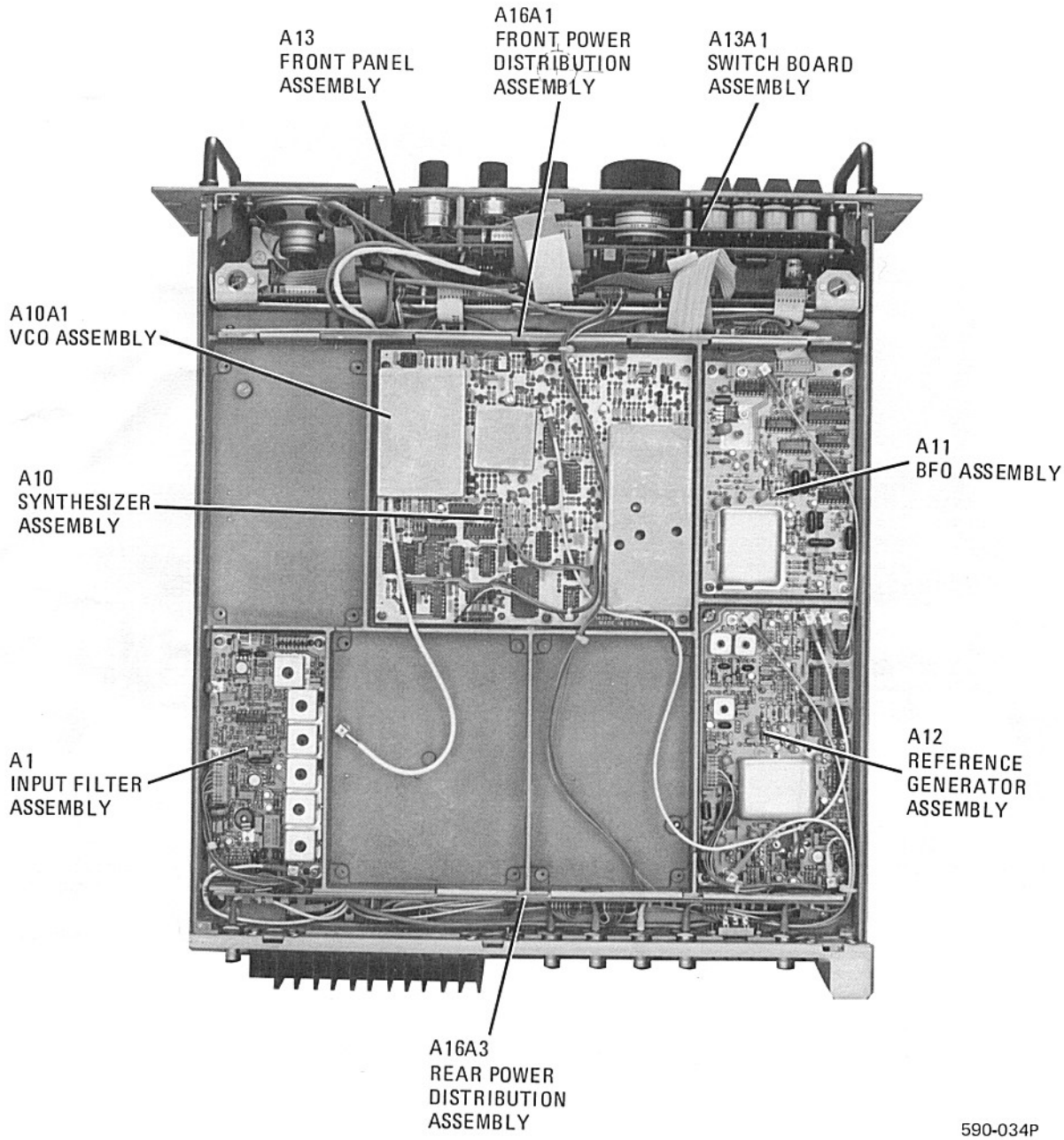


Figure 3. Main Chassis Bottom View

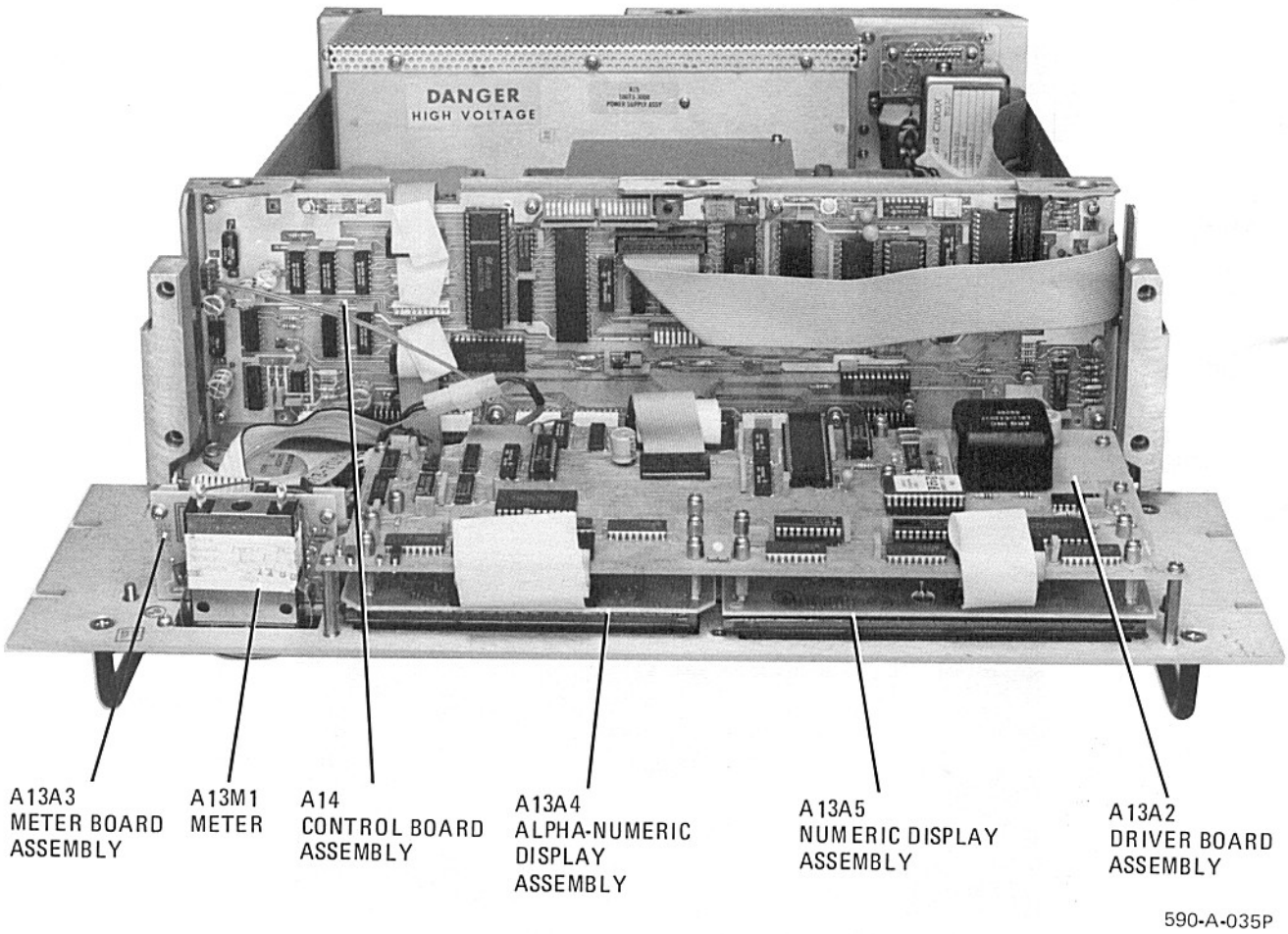


Figure 4. Main Chassis Front View

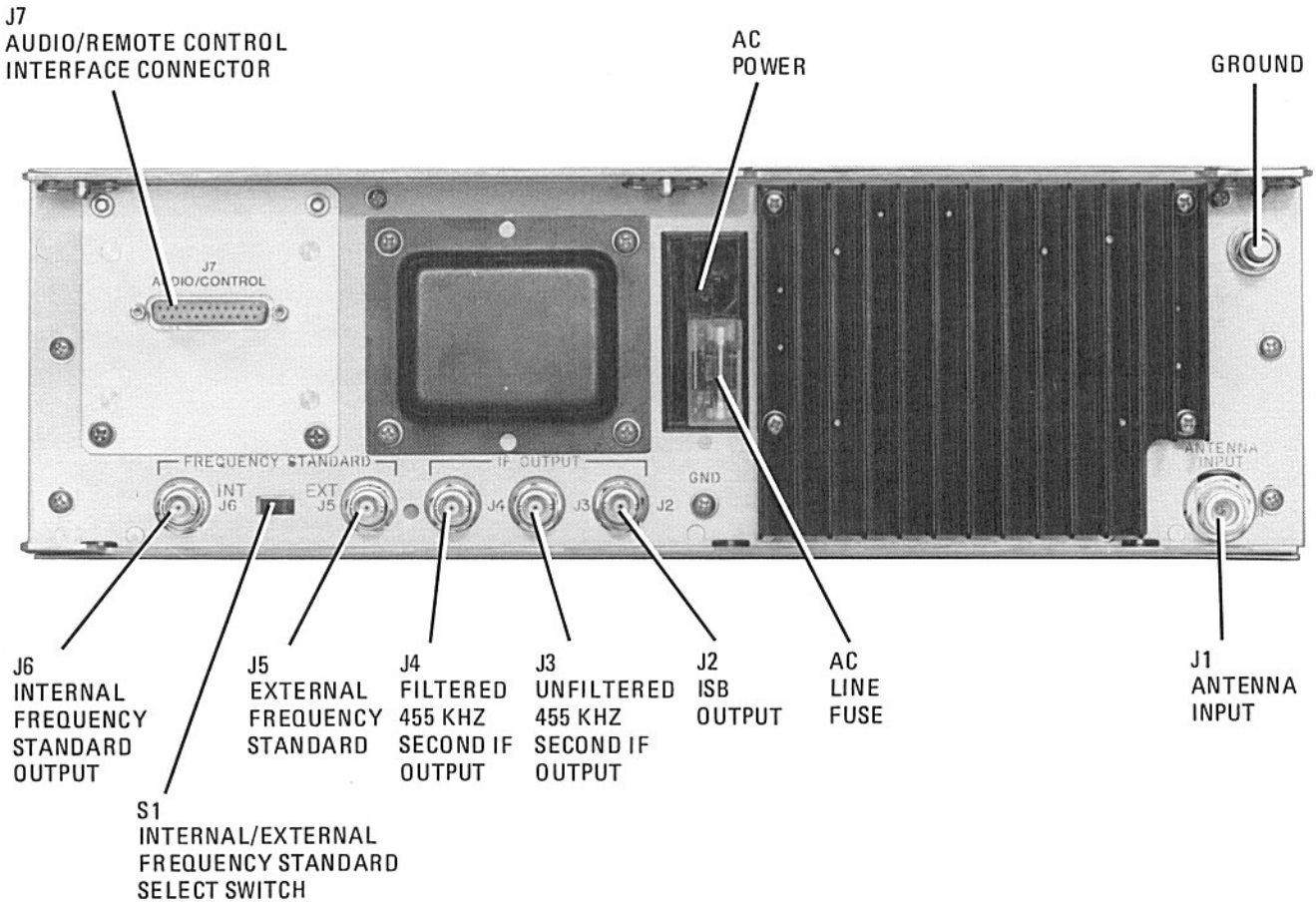


Figure 5. Main Chassis Rear View

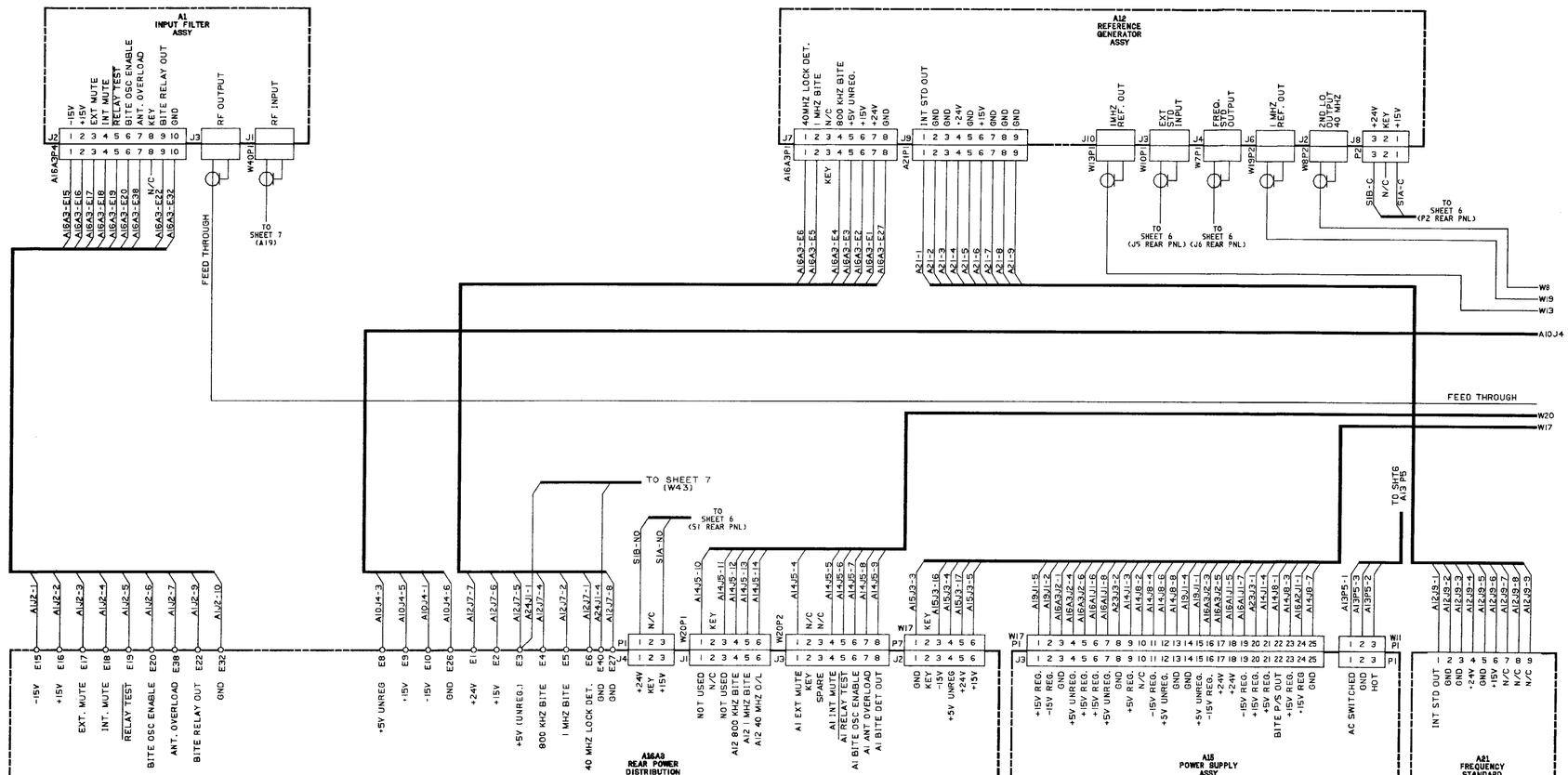


Figure 6. Main Chassis Interconnection Schematic Diagram (10215-1011, Rev.C) (Sheet 1 of 7)

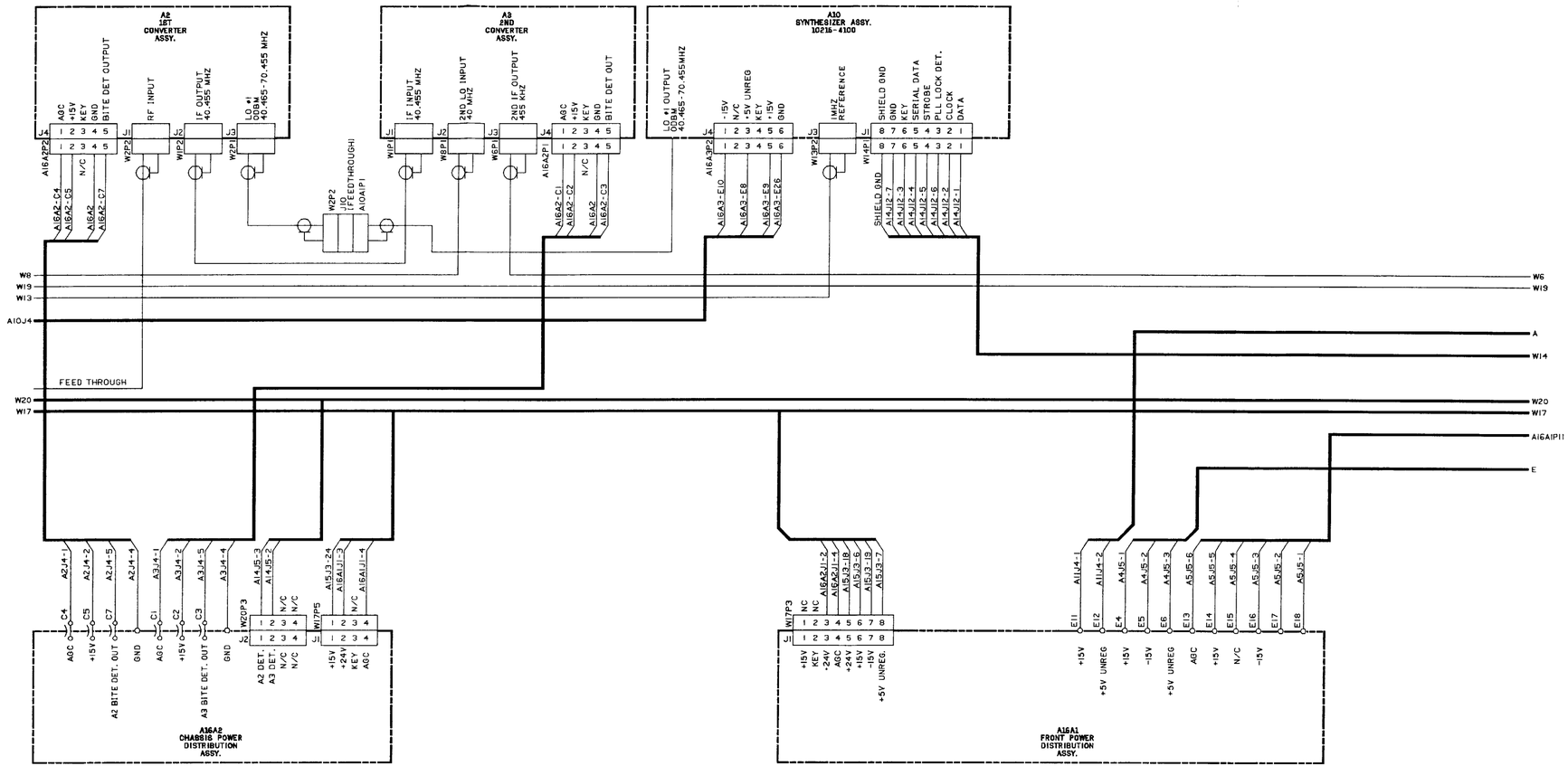


Figure 6. Main Chassis Interconnection Schematic Diagram (10215-1011, Rev.C) (Sheet 2 of 7)

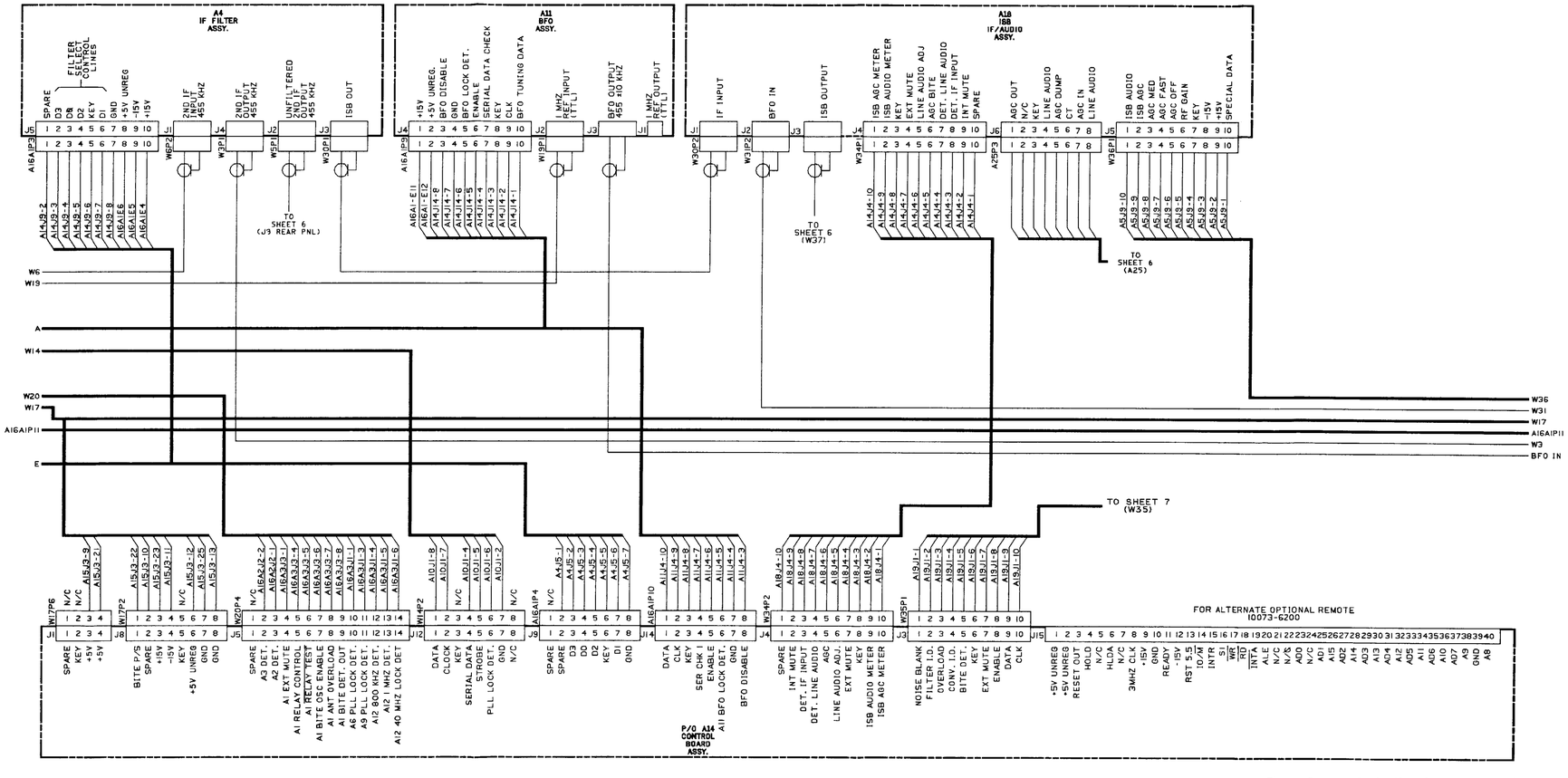


Figure 6. Main Chassis Interconnection Schematic Diagram (10215-1011, Rev.C) (Sheet 3 of 7)

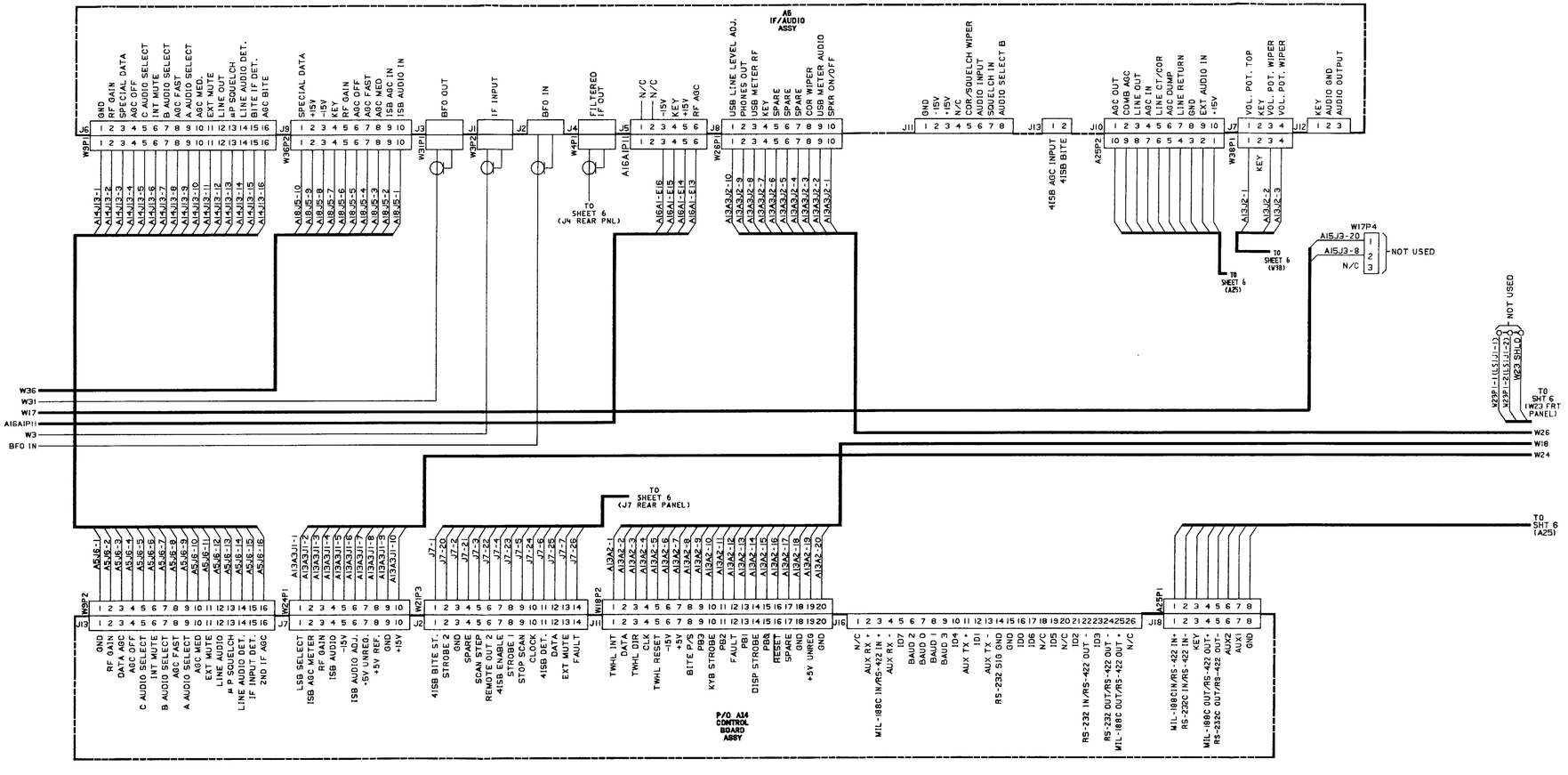


Figure 6. Main Chassis Interconnection Schematic Diagram (10215-1011, Rev.C) (Sheet 4 of 7)

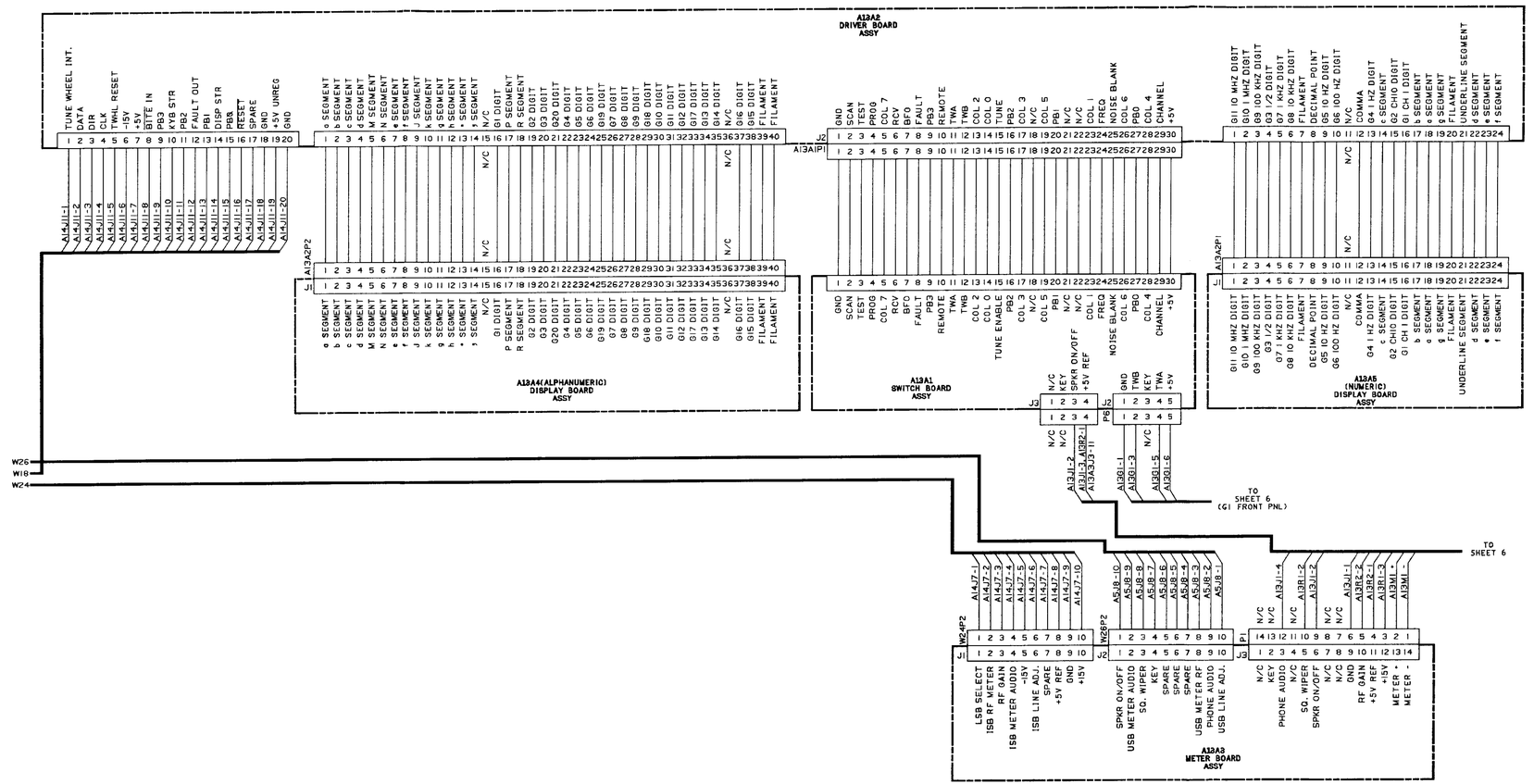


Figure 6. Main Chassis Interconnection Schematic Diagram (10215-1011, Rev. C) (Sheet 5 of 7)

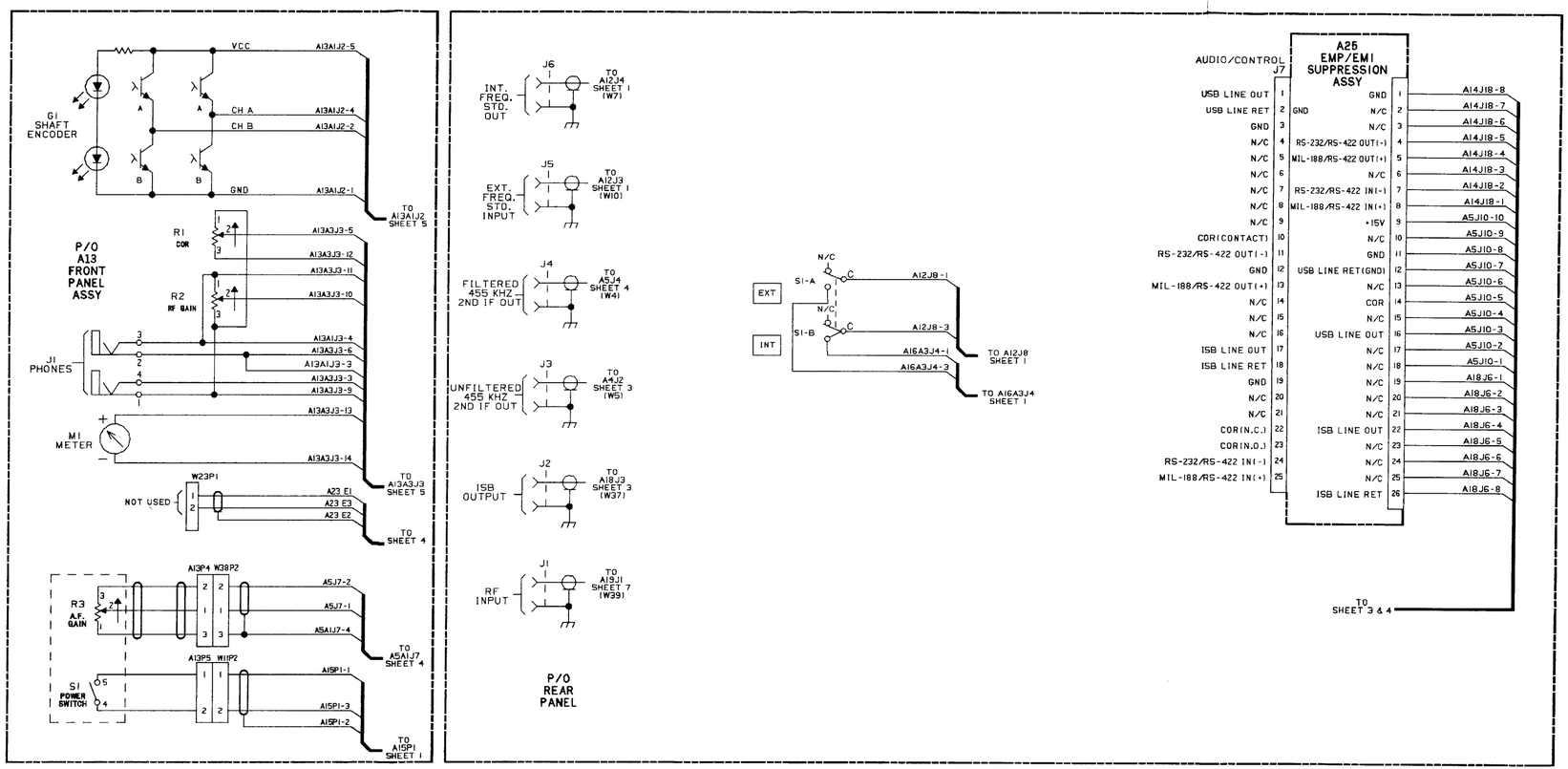
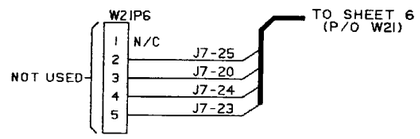


Figure 6. Main Chassis Interconnection Schematic Diagram (10215-1011, Rev. C) (Sheet 6 of 7)



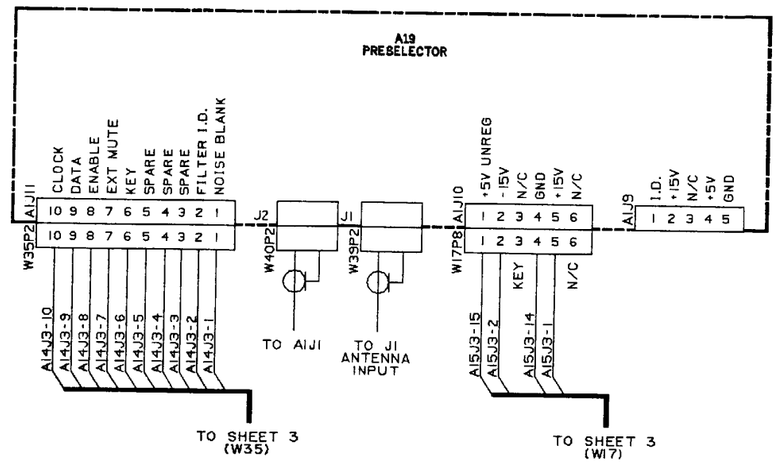


Figure 6. Main Chassis Interconnection Schematic Diagram (10215-1011, Rev.C) (Sheet 7 of 7)

A1
INPUT FILTER ASSEMBLY

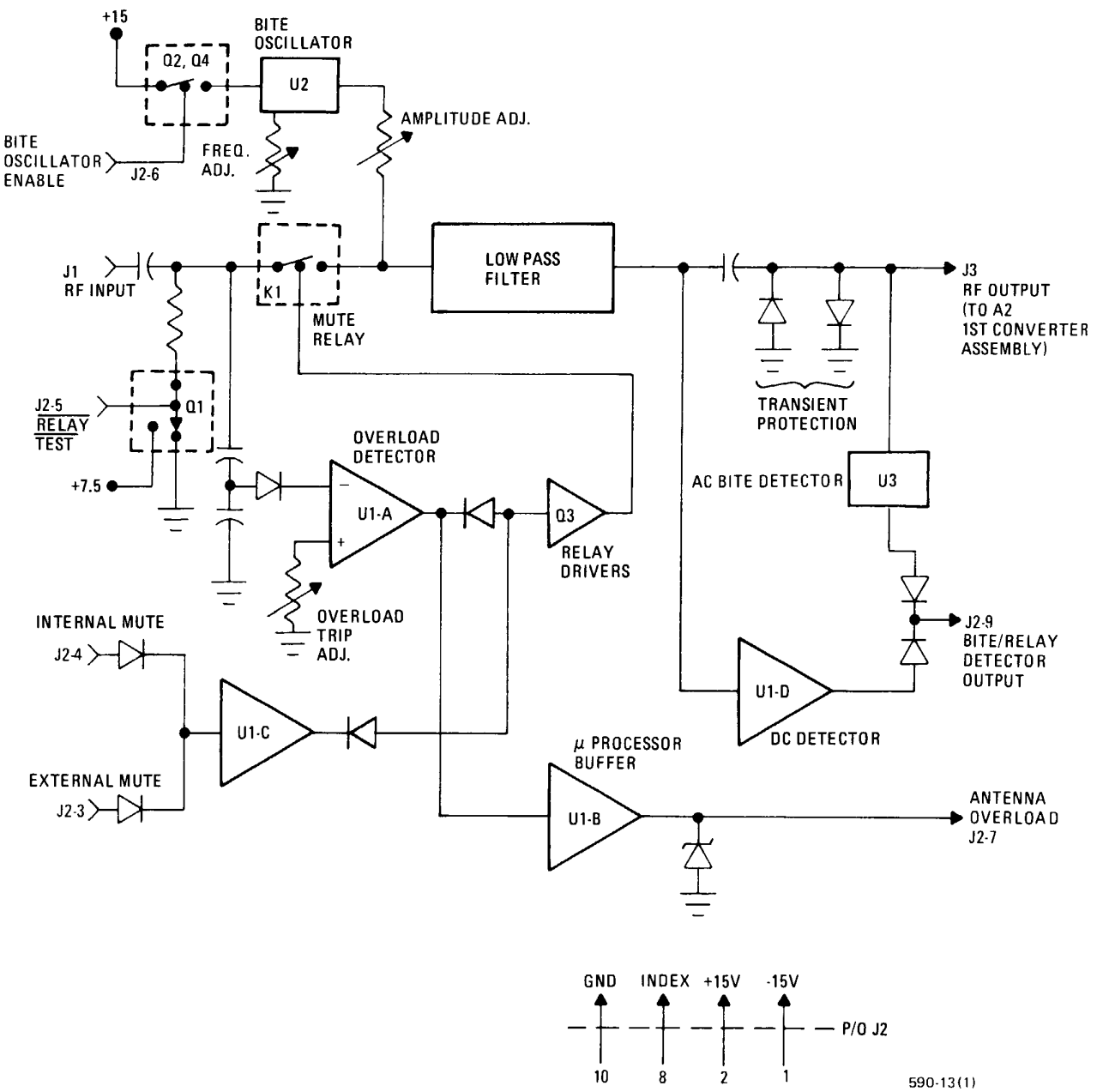


TABLE OF CONTENTS

Paragraph		Page
1.	General Description	1
2.	Interface Connections	1
3.	Circuit Description	2
3.1	Low Pass Filter (LPF) Circuit	2
3.2	Protection Circuits	2
3.2.1	Transient Protection	2
3.2.2	Steady State Protection	2A
3.3	Mute Circuitry	2A
3.4	BITE Circuitry	2A
3.4.1	BITE Signal Generation	2B
3.4.2	BITE Detection	2B
3.4.2.1	Relay K1 Test Circuits	2B
3.4.2.2	A1 Signal Path Test Circuits	2B
4.	Maintenance	3
4.1	BITE Oscillator Adjustments/Test	3
4.2	Overload Adjustments/Test	4
5.	Parts List	4
6.	Schematic Diagram	4

LIST OF FIGURES

Figure		Page
1	Typical A1 LPF Characteristics	2
2	A1 BITE Oscillator Test Setup	3
3	A1 Overload Adjustment Test Setup	4
4	Input Filter Assembly A1 Component Location Diagram (10073-5100)	9
5	Input Filter Assembly A1 Schematic Diagram (10073-5101)	11

LIST OF TABLES

Table		Page
1	A1 Input Filter Assembly Interface Connections	1
2	Input Filter Assembly A1 Parts List (PL 10073-5100)	5

A1 INPUT FILTER ASSEMBLY

1. GENERAL DESCRIPTION

Input Filter Assembly A1 performs two primary functions:

a. RF signal filtering above the desired receiver input range of 14 kHz to 30 MHz. Specifically, the first IF signal at 40.455 MHz, and the image band at 80.920 to 110.910 MHz.

b. Protection from high level input signals (1.5 to 70 V_{rms}) which could damage receiver front end circuits.

Additionally, BITE signal generation, A1 BITE detection, and receiver muting also occur on the A1 Assembly.

RF input signals arrive at J1 from the Preselector Assembly A19, or rear panel connector J1, Antenna Input, if the preselector is not used. RF output signals feed from J3 to First Converter Assembly A2. Total module gain from input to output is nominally 0 dB.

2. INTERFACE CONNECTIONS

Table 1 details the various input/output connections and any relevant data.

Table 1. A1 Input Filter Assembly Interface Connections

Connector	Function	Characteristics
J1	RF INPUT	14 kHz - 30 MHz, Zo = 50 ohms
J2-1	Power	-15 Vdc at 20 mA
J2-2	Power	+ 15 Vdc at 200 mA
J2-3	External Mute	Same as Internal Mute
J2-4	Internal Mute	+ 5 Vdc = relay contacts open, 0 Vdc = relay contacts closed
J2-5	Relay Test	Relay Test Line, 0 Vdc = + 7.5 Vdc applied to K1 contacts + 5 Vdc = 0 Vdc applied to K1 contacts
J2-6	Bite Oscillator Enable	Bite Oscillator Enable Line, + 5 Vdc = oscillator on 0 Vdc = oscillator off
J2-7	Antenna Overload Output	3.5 Vdc output for 1.5 - 70 V_{rms} input
J2-8	Index	
J2-9	BITE Detector Output	BITE signal test: 2.5 Vdc nominally for ac or dc BITE tests
J2-10	GND	
J3	RF Output	14 kHz - 30 MHz, Zo = 50 ohms

3. CIRCUIT DESCRIPTION

3.1 Low Pass Filter (LPF) Circuit

The LPF was designed for a passband of 10 kHz to 30 MHz, a total insertion loss of less than 1/2 dB (nominally), and an VSWR of 1.1:1.

The LPF image rejection desired of >100 dB is required since the Receiver image band of 80.920 MHz to 110.910 MHz encompasses U.S. TV channels 5,6, and the FM band. To accomplish this, a ninth order Elliptic function filter is cascaded with a fifth order Chebishev function filter. The first null of the Elliptic filter was chosen at the first IF (40.455 MHz), and the Chebishev filter is used to flatten out the stop band characteristics of the Elliptic filter. See figure 1 for a typical A1 LPF characteristic. The -3 dB cutoff frequency is approximately 31.5 MHz.

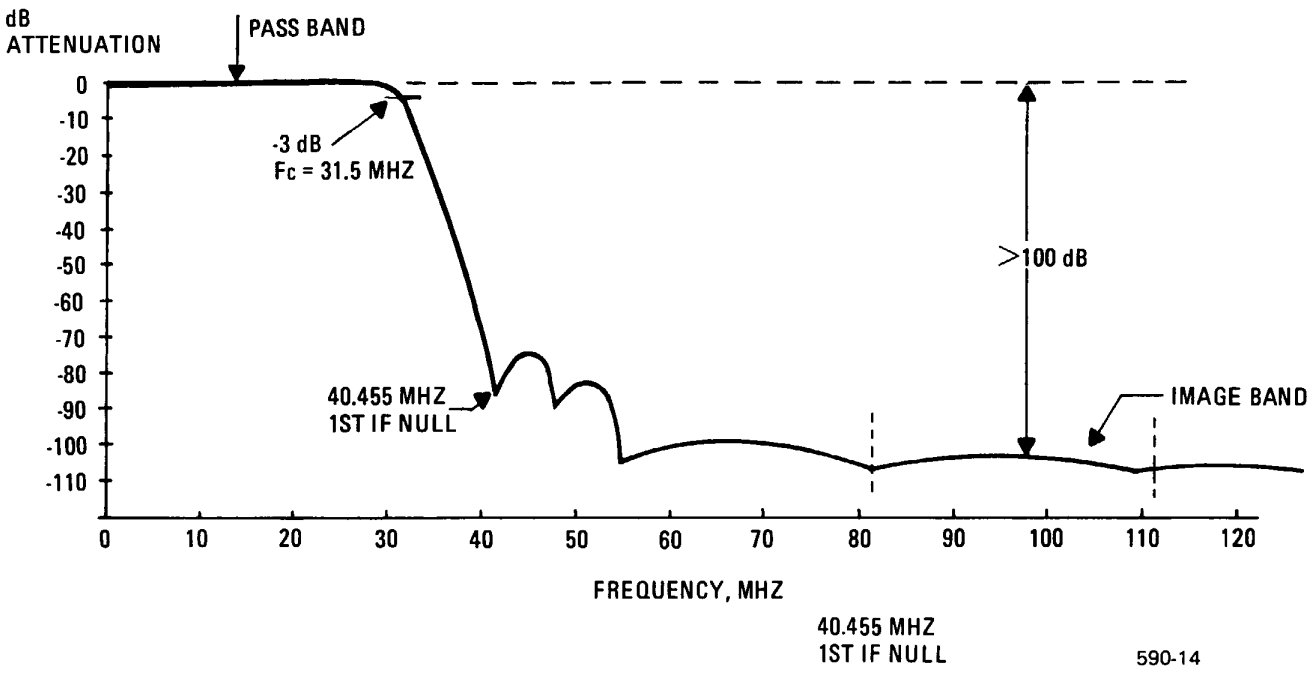


Figure 1. Typical A1 LPF Characteristics

3.2 Protection Circuits

Two protection circuits are employed on the A1 assembly and respond to the two possible types of overload conditions: transient and steady state.

3.2.1 Transient Protection

Upon initial application of an overload condition, a transient signal may pass through the LPF before relay K1 can deenergize. This transient is clamped at a maximum level of 8 V_{PP} by CR1-CR4 and CR24-CR27 before leaving the assembly. This allows temporary protection until the relay control circuits can activate in the presence of a steady state signal. Also, certain types of overloads are basically transient in nature, and it may not be desirable to disturb the signal path by deenergizing K1.

3.2.2 Steady State Protection

Under no RF input conditions at J1, CR5-CR8, R40, and CR9-CR12, R5 bias U1A (-) input to nominally 0 Vdc. This value is less than the positive potential set by R7, Overload Adjust, at U1A (+), so U1A output at pin 8 will be high (+ 15 Vdc). Consequently, CR14 is reverse biased, and R10 supplies base current to Q3, turning Q3 and relay K1 on.

When an RF signal is received at J1, a portion is tapped off by voltage divider network C3-C9 and detected by the diode string CR5-CR12. This raises the potential at U1A (-). When this level exceeds the trip point set by R7 (corresponding to approximately 1.5 Vrms ac at J1), U1A output swings low (-15 Vdc) and forward biases CR14. This removes base drive to Q3. Q3 turns off and the relay deenergizes, breaking the RF signal path into the receiver. Hysteresis around U1A holds the relay deenergized until the RF input drops at least 10 dB.

Under overload conditions, the low output at U1A causes U1B output to swing high (+ 15 Vdc). This forward biases CR29. Voltage divider/clamp network R18, R21, R37, and CR22 provide a TTL logic high signal (≈ 4 Vdc) to detection circuitry on Control Board A14. This in turn causes the front panel display to read out the message ANTENNA OVERLOAD. This disables all front panel controls until the overload condition is removed, at which time the overload message is removed and normal operation is resumed.

3.3 Mute Circuitry

Two receiver mute inputs are provided on the A1 board; Internal Mute and External Mute. Both cause RF signal path muting when a high TTL level (≈ 5 Vdc) signal is present at their inputs. This causes U1C output to swing low (-15 Vdc), which forward biases CR20 and removes base drive to Q3. Q3 turns off, deenergizing K1 and disrupting the RF signal path into the receiver. This + 5 Vdc is generated on the control board (A14) whenever the external Mute line on J7-7 (rear panel) is grounded.

Internal Muting occurs as part of the receiver BITE routine. External Muting is accessed via the rear panel terminal strip TB1, pin 16, and/or connector J7, pin 7. External Muting is an option to be exercised by the operator, depending upon system requirements.

3.4 BITE Circuitry

BITE test signal generation occurs on the A1 assembly. This test signal is adjusted to -20 dBm, 100 kHz at J3. It is fed through the A1 assembly and on to assemblies A2-A5 for testing purposes. Various amplitude sample and detection circuits throughout the signal path monitor critical signal stages to check for proper operation. BITE testing is completely under software control and is initiated by pressing the front panel TEST switch (see the Maintenance section of this manual).

3.4.1 BITE Signal Generation

The BITE test signal is generated by 100 kHz oscillator U2 and its associated components. U2 output is applied to the LPF side of relay K1 only when K1 is deenergized via software control. This prevents U2 output signals from reaching the antenna. The 100 kHz injection at U2, pin 3, is a 15 Vpp square wave. The BITE test signal is set while monitoring J3. R25 sets the operating frequency to 100 kHz and R28 sets the output amplitude to -20 dBm.

Oscillator U2 is enabled by Q2 and Q4, which in turn are controlled via system software. A + 5 Vdc level at J2-6 enables U2.

3.4.2 BITE Detection

Two BITE tests are enacted on the A1 assembly.

- K1 relay check
- A1 signal path level check

Both tests are under BITE software control and commence upon initiating front panel TEST control. The tests are done sequentially, and the resulting output signal at J2-9 is ultimately applied to Control Board Assembly A14. An error code will be displayed on the RF-590 front panel display if either test fails.

3.4.2.1 Relay K1 Test Circuits

During normal operating conditions, K1 will be energized, Internal Mute line will be low, and Relay Test line will be high (consequently, holding Q1 on, and applying 0 Vdc to TP1 and relay K1). When the BITE routine begins, $\overline{\text{Relay Test}}$ goes low, turning off Q1 and applying ≈ 7.5 Vdc to TP1 and the relay contacts. This signal is passed through the relay and the low pass filter (LPF), and is detected by Dc BITE Detector U1D. U1D output, which had previously been low (-15 Vdc) will now swing high (+ 15 Vdc) and forward bias CR21. This provides a nominal 2.5 Vdc level at J2, pin 9, BITE/Relay Out. This signal is fed to an A/D converter on the A14 Control Board, which then feeds other A14 circuits that determine if this signal has sufficient amplitude to ensure that no dc losses are present in relay K1 or the LPF.

Next, Internal Mute goes high, which turns Q3 and K1 off. Since the 7.5 Vdc signal at TP1 can no longer pass through the relay, U1D output will swing low and present ≈ 0 Vdc at BITE/Relay Out. Control Board A14 circuitry will interpret this as an indication that the relay did deenergize, and will proceed to the next test, A1 Signal Path.

3.4.2.2 A1 Signal Path Test Circuits

Upon successful completion of relay K1 testing, the A1 signal path is checked using a 100 kHz test signal generated by BITE Oscillator U2. The oscillator is enabled when the BITE Oscillator Enable line is pulled high (under software control) turning on Q4 and Q2. This applies + 15 Vdc to oscillator U2. U2 output is applied to the input of the LPF (relay K1 is deenergized during this test) and is detected by Ac BITE Detector U3. If no faults occur in the signal path, U3 will produce a nominal output voltage of 2.5 Vdc at J2, pin 9, BITE/RELAY OUT. This is sampled by the A/D Converter on Control Board A14, and if the level is sufficient (indicating no ac

losses on the A1 assembly), BITE testing would continue throughout the RF chain of the receiver. (Note that it is this same 100 kHz signal which is used to test circuits on the A2-A5 assemblies.)

4. MAINTENANCE

The following adjustments should not be performed as routine maintenance procedures, but should be used only when a failure indicates a definite requirement. All tests should be performed with all assembly connections in normal contact, unless otherwise specified.

NOTE

J3 plugs directly into the A2 assembly through the chassis. Therefore it will be necessary to remove the A1 assembly from the chassis to gain access to J3.

4.1 BITE Oscillator Adjustments/Test

a. Connect equipment as shown in figure 2.

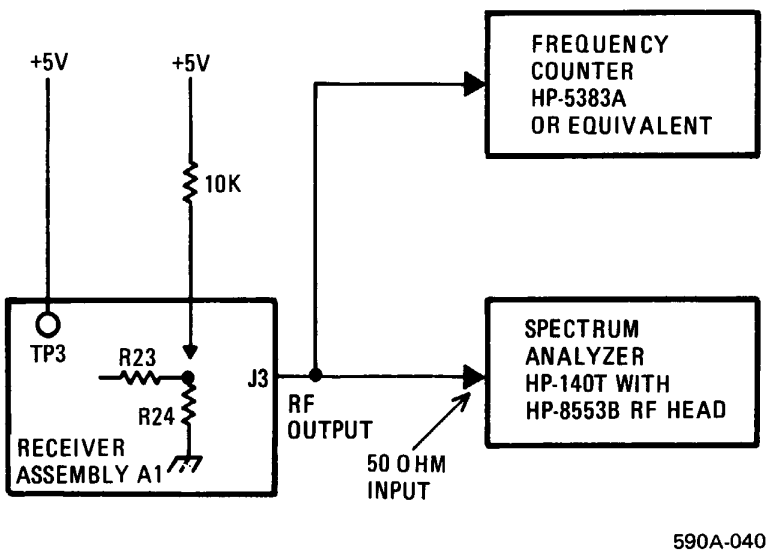


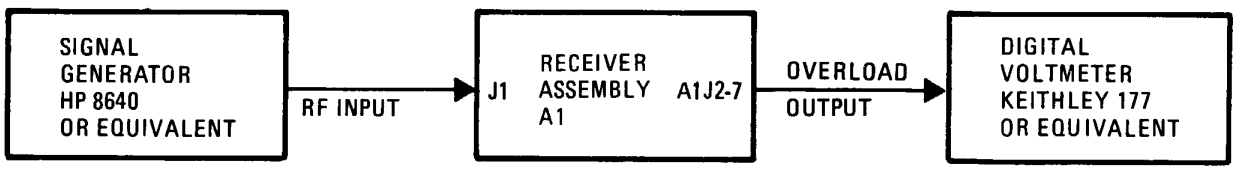
Figure 2. A1 BITE Oscillator Test Setup

b. Adjust R25 for 100.0 kHz and R28 for -20 dBm at J3 RF output.

c. Disconnect all equipment and fully reconnect the A1 module to the Receiver. Initiate the BITE Test. The receiver must pass 01 testing.

4.2 Overload Adjustments/Test

a. Connect equipment as shown in figure 3.



590A-041

Figure 3. A1 Overload Adjustment Test Setup

b. Set Front Panel controls as follows:

Frequency: 10.000000 MHz

Mode: USB

AGC: Medium

RF Gain: Fully clockwise (cw)

c. Set signal generator to 10.000 MHz, 1.5 V_{rms}.

d. Adjust R7 until J2-7 Antenna Overload switches to approximately 5 Vdc.

e. Disconnect all equipment.

5. PARTS LIST

Table 2 is a comprehensive parts list of all replaceable components in Input Filter Assembly A1. When ordering parts from the factory, include a full description of the part. Use figure 4, the Input Filter Assembly A1 component location diagram to identify parts.

6. SCHEMATIC DIAGRAM

Figure 5 is the Input Filter Assembly A1 schematic diagram.

Table 2. Input Filter Assembly A1 Parts List (PL 10073-5100, Rev. T)

Ref. Desig.	Part Number	Description
C1	M39014/02-1320	CAP, CER, ,47UF,
C2	M39014/02-1320	CAP, CER, ,47UF,
C3	CM04ED300J03	CAP 30PF 5% 500V MICA
C4	CM04ED300J03	CAP 30PF 5% 500V MICA
C5	CM04ED300J03	CAP 30PF 5% 500V MICA
C6	CM04ED300J03	CAP 30PF 5% 500V MICA
C7	CM04ED750J03	CAP 75PF 5% 500V MICA
C8	CM04ED750J03	CAP 75PF 5% 500V MICA
C9	CM04ED750J03	CAP 75PF 5% 500V MICA
C10	CM04CD120J03	CAP 12PF 5% 500V MICA
C11	CM04CD050D03	CAP 5PF +-.5PF 500V MICA
C12	CM04FD151J03	CAP 150PF 5% 500V MICA
C13	CM04ED430J03	CAP 43PF 5% 500V MICA
C14	CM04ED510J03	CAP 51PF 5% 500V MICA
C15	CM04ED750J03	CAP 75PF 5% 500V MICA
C16	CM04ED470J03	CAP 47PF 5% 500V MICA
C17	CM04FD131J03	CAP 130PF 5% 500V MICA
C18	CM04ED300J03	CAP 30PF 5% 500V MICA
C19	CM04ED620J03	CAP 62PF 5% 500V MICA
C20	CM04ED680J03	CAP 68PF 5% 500V MICA
C21	CM04FD151J03	CAP 150PF 5% 500V MICA
C22	CM04ED680J03	CAP 68PF 5% 500V MICA
C23	M39014/02-1310	CAP .1 UF
C25	M39014/02-1320	CAP, CER, ,47UF,
C26	M39014/02-1320	CAP, CER, ,47UF,
C27	CK05BX472M	CAP 4700PF 20% 100V CER
C27	CK05BX472K	CAP 4700PF 10% 100V CER
C28	CM04FD151J03	CAP 150PF 5% 500V MICA
C29	M39014/02-1320	CAP, CER, ,47UF,
C30	M39014/02-1320	CAP, CER, ,47UF,
C31	M39014/02-1320	CAP, CER, ,47UF,
C32	M39014/02-1310	CAP .1 UF
C33	CM06FD122J03	CAP 1200PF 5% 500V MICA
C35	M39014/02-1320	CAP, CER, ,47UF,
C36	M39014/01-1535	CAP .01UF
C37	M39014/02-1310	CAP .1 UF
C38	M39014/02-1310	CAP .1 UF
C39	M39014/02-1310	CAP .1 UF
C40	M39014/02-1310	CAP .1 UF
C41	M39014/02-1310	CAP .1 UF
C43	M39014/02-1310	CAP .1 UF
C44	C26-0025-339	CAP,FXD,ELCTLT,3.3 UF,25
C45	C26-0025-339	CAP,FXD,ELCTLT,3.3 UF,25
C46	M39014/01-1535	CAP .01UF

Table 2. Input Filter Assembly A1 Parts List (PL 10073-5100, Rev. T) (Cont.)

Ref. Desig.	Part Number	Description
C47	M39014/01-1535	CAP .01UF
C48	M39014/02-1310	CAP .1 UF
C50	CM04FD151J03	CAP 150PF 5% 500V MICA
CR1	D02-0003-001	DIODE,RECT,RF
CR2	D02-0003-001	DIODE,RECT,RF
CR3	D02-0003-001	DIODE,RECT,RF
CR4	D02-0003-001	DIODE,RECT,RF
CR5	1N4454	DIODE, SS SILICON
CR6	1N4454	DIODE, SS SILICON
CR7	1N4454	DIODE, SS SILICON
CR8	1N4454	DIODE, SS SILICON
CR9	1N4454	DIODE, SS SILICON
CR10	1N4454	DIODE, SS SILICON
CR11	1N4454	DIODE, SS SILICON
CR12	1N4454	DIODE, SS SILICON
CR13	1N5245B	DIODE 15V 5% 0.5W ZENER
CR14	1N4454	DIODE, SS SILICON
CR15	1N4007	DIODE, RECT. 1000V 1A
CR16	1N4454	DIODE, SS SILICON
CR17	1N4454	DIODE, SS SILICON
CR18	1N4454	DIODE, SS SILICON
CR19	1N4454	DIODE, SS SILICON
CR20	1N4454	DIODE, SS SILICON
CR21	1N4454	DIODE, SS SILICON
CR22	1N5230A	DIODE 4.7V 10% 0.5W ZENER
CR23	1N5230A	DIODE 4.7V 10% 0.5W ZENER
CR24	D02-0003-001	DIODE,RECT,RF
CR25	D02-0003-001	DIODE,RECT,RF
CR26	D02-0003-001	DIODE,RECT,RF
CR27	D02-0003-001	DIODE,RECT,RF
CR28	1N4454	DIODE, SS SILICON
CR29	1N4454	DIODE, SS SILICON
J1	J-0031	CONNECTOR, COAX, SNAP-ON
J2	J46-0032-010	HEADER, 10 PIN DISCRETE
J3	J90-0014-001	CONNECTOR, COAX
K1	K-0118	RLY,12VDC,DPDT,ENC,PC MNT
L1	10073-5111	INDUCTOR
L2	10073-5112	INDUCTOR
L3	10073-5113	INDUCTOR
L4	10073-5114	INDUCTOR
L5	10073-5114	INDUCTOR
L6	10073-5114	INDUCTOR
L7	10073-7029	INDUCTOR
L9	MS75085-13	COIL, RF 330 UH 10%
L10	MS75085-13	COIL, RF 330 UH 10%

Table 2. Input Filter Assembly A1 Parts List (PL 10073-5100, Rev. T) (Cont.)

Ref. Desig.	Part Number	Description
L11	MS75085-13	COIL, RF 330 UH 10%
L12	MS75085-13	COIL, RF 330 UH 10%
L13	MS75085-13	COIL, RF 330 UH 10%
L14	MS75085-13	COIL, RF 330 UH 10%
Q1	2N2222	XSTR, SS/GP, NPN
Q2	2N2907	XSTR, SS/GP, PNP
Q3	2N2222	XSTR, SS/GP, NPN
Q4	2N2222	XSTR, SS/GP, NPN
R1	R65-0003-103	RES,10K 5% 1/4W CAR FILM
R2	R65-0003-104	RES,100K 5% 1/4W CAR FILM
R3	R65-0003-103	RES,10K 5% 1/4W CAR FILM
R4	R65-0003-104	RES,100K 5% 1/4W CAR FILM
R5	RN55D1053F	RES,105K 1% 1/8W MET FLM
R6	R65-0003-472	RES,4.7K 5% 1/4W CAR FILM
R7	R30-0008-501	RES,VAR,PCB,500,20% 1/2W
R8	R65-0003-103	RES,10K 5% 1/4W CAR FILM
R9	R65-0003-103	RES,10K 5% 1/4W CAR FILM
R10	R65-0003-512	RES,5.1K 5% 1/4W CAR FILM
R11	R65-0003-302	RES,3.0K 5% 1/4W CAR FILM
R12	R65-0003-330	RES,33 5% 1/4W CAR FILM
R13	RN55D1002F	RES,10.0K 1% 1/8W MET FLM
R14	RN55D1002F	RES,10.0K 1% 1/8W MET FLM
R15	R65-0003-472	RES,4.7K 5% 1/4W CAR FILM
R16	R65-0003-512	RES,5.1K 5% 1/4W CAR FILM
R17	R65-0003-472	RES,4.7K 5% 1/4W CAR FILM
R18	R65-0003-103	RES,10K 5% 1/4W CAR FILM
R19	R65-0003-133	RES,13K 5% 1/4W CAR FILM
R20	R65-0003-122	RES,1.2K 5% 1/4W CAR FILM
R21	R65-0003-472	RES,4.7K 5% 1/4W CAR FILM
R22	R65-0003-104	RES,100K 5% 1/4W CAR FILM
R23	R65-0003-103	RES,10K 5% 1/4W CAR FILM
R24	R65-0003-513	RES,51K 5% 1/4W CAR FILM
R25	R-2228	RES,VAR,PCB 10K .5 20%
R26	R65-0003-102	RES,1.0K 5% 1/4W CAR FILM
R27	R65-0003-203	RES,20K 5% 1/4W CAR FILM
R28	R-2229	RES,VAR,PCB 20K .5 20%
R29	R65-0003-103	RES,10K 5% 1/4W CAR FILM
R30	R65-0003-103	RES,10K 5% 1/4W CAR FILM
R31	R65-0003-102	RES,1.0K 5% 1/4W CAR FILM
R32	R65-0003-472	RES,4.7K 5% 1/4W CAR FILM
R33	RN55D1740F	RES,174.0 1% 1/8W MET FLM
R34	R65-0003-104	RES,100K 5% 1/4W CAR FILM
R35	R65-0003-103	RES,10K 5% 1/4W CAR FILM
R36	R65-0003-103	RES,10K 5% 1/4W CAR FILM
R37	R65-0003-102	RES,1.0K 5% 1/4W CAR FILM

Table 2. Input Filter Assembly A1 Parts List (PL 10073-5100, Rev. T) (Cont.)

Ref. Desig.	Part Number	Description
R38	R65-0003-102	RES,1.0K 5% 1/4W CAR FILM
R39	R65-0003-394	RES,390K 5% 1/4W CAR FILM
R40	RN55D8062F	RES,80.6K 1% 1/8W MET FLM
R41	R65-0004-472	RES,4.7K 5% 1/2W CAR FILM
R42	R65-0003-104	RES,100K 5% 1/4W CAR FILM
R43	R65-0003-513	RES,51K 5% 1/4W CAR FILM
R44	R65-0003-302	RES,3.0K 5% 1/4W CAR FILM
R45	R65-0003-104	RES,100K 5% 1/4W CAR FILM
R46	RN55D1003F	RES,100K 1% 1/8W MET FLM
R47	R65-0003-472	RES,4.7K 5% 1/4W CAR FILM
R50	R65-0003-203	RES,20K 5% 1/4W CAR FILM
R51	R65-0003-203	RES,20K 5% 1/4W CAR FILM
R52	R65-0003-124	RES,120K 5% 1/4W CAR FILM
TP1	J-0071	TIP JACK, BROWN
TP2	J-0066	TIP JACK, RED
TP3	J-0069	TIP JACK, ORANGE
TP4	J-0070	TIP JACK, YELLOW
TP5	J-0068	TIP JACK, GREEN
U1	I30-0003-000	IC 324 OP AMP PLASTIC
U2	I20-0005-001	IC LM211H COMPARATOR
U3	I20-0005-001	IC LM211H COMPARATOR

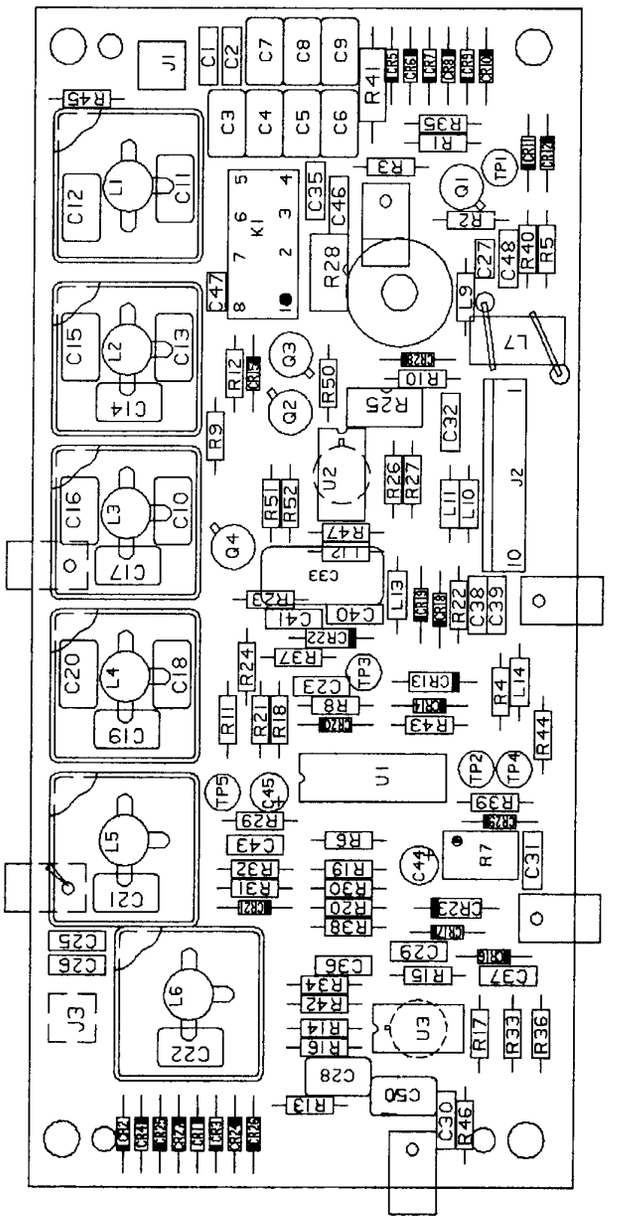


Figure 4. Input Filter Assembly A1 Component Location Diagram (10073-5100)

NOTE: UNLESS OTHERWISE SPECIFIED:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR A COMPLETE DESIGNATION, PREFIX WITH UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.
2. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, ±5%.
3. ALL CAPACITOR VALUES ARE IN MICROFARADS.
4. ALL INDUCTOR VALUES ARE IN MICROHENRIES.
5. VENDOR PART NO. CALLOUTS ARE FOR REFERENCE ONLY. COMPONENTS ARE SUPPLIED PER PART NO. IN PARTS LIST.
6. RELAY K1 IS SHOWN ENERGIZED.
7. VOLTAGE LEVEL SPECIFIED FOR NO RF INPUT.
8. VOLTAGE LEVEL SPECIFIED DURING AI BITE TEST.

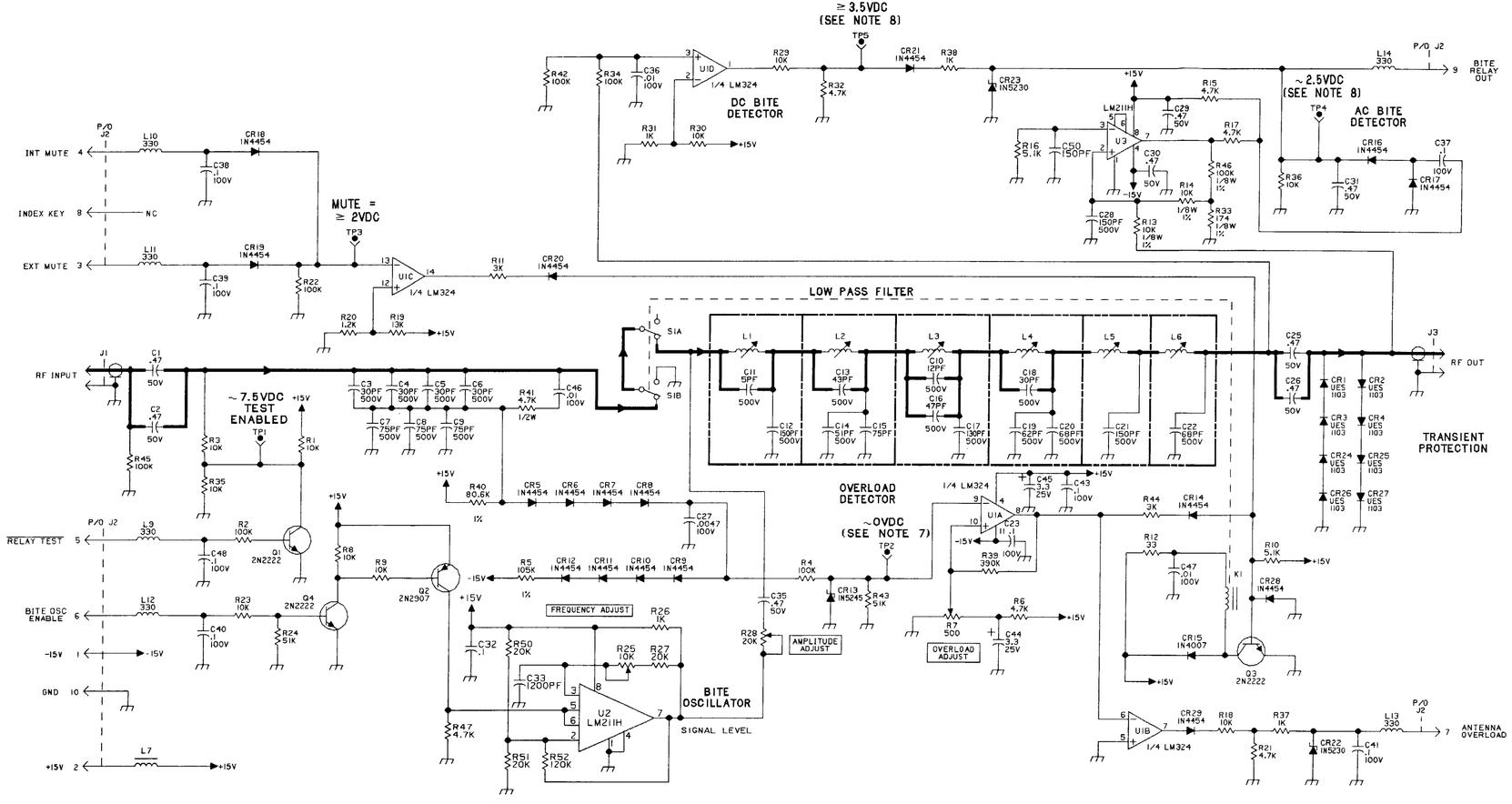
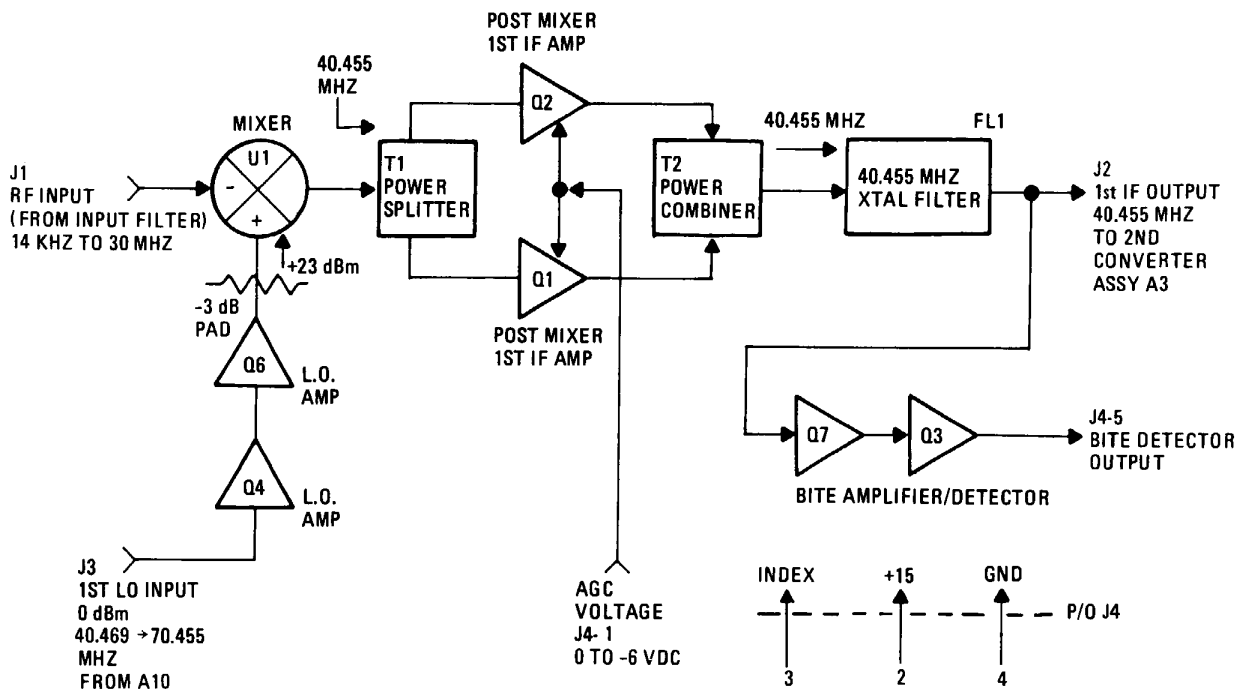


Figure 5. Input Filter Assembly A1 Schematic Diagram (10073-5101, Rev. F)

A2
FIRST CONVERTER ASSEMBLY



URR-030

TABLE OF CONTENTS

Paragraph		Page
1.	General Description	1
2.	Interface Connections	1
3.	Circuit Description	1
3.1	Mixer/Postmixer IF Amplifiers	1
3.2	BITE Detection Circuit	2
3.3	LO No. 1 Amplifier	2
4.	Maintenance	2
4.1	LO No. 1 Amplifier Test	2
4.2	Postmixer IF Amplifier Adjustments/Test	3
4.3	AGC Test	3
4.4	BITE Test/Alignment	5
5.	Parts List	5
6.	Schematic Diagram	5

LIST OF FIGURES

Figure		Page
1	A2 Postmixer IF Amplifier Test Setup	3
2	A2 AGC Test Setup	4
3	A2 BITE Test Setup	5
4	First Converter Assembly A2 Component Location Diagram (10073-5200-02)	9
5	First Converter Assembly A2 Schematic Diagram (10073-5201)	11

LIST OF TABLES

Table		Page
1	First Converter A2 Interface Connections	1
2	A2 AGC - Gain Reduction Data	4
3	First Converter Assembly A2 Parts List (PL 10073-5200/-5200-02)	6

A2 FIRST CONVERTER ASSEMBLY

1. GENERAL DESCRIPTION

First Converter Assembly A2 converts the Input Radio Frequency (RF) range of 14 kHz to 30 MHz to an Intermediate Frequency (IF) of 40.455 MHz at mixer U1. (Sideband inversion occurs during the mixing process.) This IF signal is then split in power and fed to two identical automatic gain controlled (AGC) First IF Amplifier (postmixer) stages. After the amplified signals are recombined, they are filtered through a 16 kHz wide, 40.455 MHz crystal filter and directed to Second Converter Assembly A3. Typical RF input to IF output gain is 0 dB. The IF signal is also monitored by the Built-In Test Equipment (BITE) detection circuit which monitors the operation of the First Converter Assembly.

2. INTERFACE CONNECTIONS

Table 1 details the various input/output connections and other relevant data.

Table 1. First Converter A2 Interface Connections

Connector	Function	Characteristics
J1	RF INPUT	14 kHz - 30 MHz, -120/ + 10 dBm Zo = 50 ohms
J2	IF Output	40.455 MHz ± 8 kHz, -120/9 dBm (under AGC control), Zo = 50 ohms
J3	LO No. 1 Injection	40.469 - 70.455 MHz, 0 dBm
J4-1	AGC Input	0 Vdc → -6 Vdc produces 0 → -20 dB gain reduction
J4-2	Power	+ 15 Vdc at 400 mA
J4-3	Index Pin	
J4-4	Ground	
J4-5	Bite Output	Approximately .75 Vdc for -20 dBm J1 input at 100 kHz

3. CIRCUIT DESCRIPTION

3.1 Mixer/Postmixer IF Amplifiers

RF input signals from 14 kHz to 30 MHz are applied to doubly balanced, diode - ring type mixer U1 at pin 1, through a 2 dB pad. U1 is a very high level mixer requiring + 23 dBm at its LO port, pin 8, from the LO No. 1 Amplifier (paragraph 3.3). Conversion loss is typically 6 dB.

IF output from U1 (pins 3, 4) is applied to a broadband 50-ohm power splitter comprised of T1, C1, C2, C45, and R4.

Q1 and Q2 are identical grounded-gate FET amplifier stages, so only one stage (Q1) shall be discussed. Q1 is biased by R5 to typically 1-2 volts at its source. The drain load impedance is set at 1400 ohms by C46, C16, and L6 (L6 is adjusted for resonance at 40.455 MHz). Nominal stage power gain is + 12 dB.

CR1 provides gain reduction by reducing the drain load on Q1 upon application of a negative AGC voltage at R7. Typically, -20 dB of gain reduction is possible.

Q1 and Q2 outputs are recombined in a broadband 50 ohm combiner consisting of T2, C19, C20, and R9. The 40.455 MHz IF output is then filtered in crystal filter FL-1, whose -6 dB bandwidth is ± 8 kHz and whose loss is approximately -4 dB.

The filtered IF output is directed to Second Converter Assembly A3 via J2, and to the BITE detection circuit (paragraph 3.2).

3.2 BITE Detection Circuit

The 40.455 MHz IF output is applied to buffer stage Q7, a source follower. Q7 output feeds tuned amplifier Q3, which amplifies the signal to the required detection level. This signal is then rectified and filtered by CR3, CR4, and C25. CR6 limits the detection voltage to approximately 5 Vdc to protect the following A/D converter inputs. An RF input level of -20 dBm at J1 results in approximately .5 Vdc at BITE Output, J4, pin 5.

3.3 LO No. 1 Amplifier

LO No. 1 injection of 0 dBm (nominally) is supplied by Synthesizer Assembly A10 to LO No. 1 input, J3, and then to common base amplifier driver Q4. The LO frequency range is 40.469 - 70.455 MHz. Q4 is biased to approximately 50 mA of emitter current via R14 - R16, and provides approximately 10 dB of voltage gain from TP3 to TP4.

T3 and T4 provide an impedance stepdown to the base of power amplifier Q6. R29 - C40 - R26 stabilize Q6 and provide a flat output (± 1 dB) from Q6 over the LO frequency range. T5 supplies nominally + 26 dBm and impedance matching to a 50 ohm, -3 dB pad consisting of R1, R2, and R3. This pad then supplies a 50 ohm termination and + 23 dBm level to the LO port of mixer U1.

Q5 and associated circuitry provides base current to Q6, resulting in a Q6 collector current of approximately 300 mA. Diode CR5 provides thermal stabilization to Q5 base current. Resistor pair R23 and R24 form a sense circuit for Q6 collector current. As Q6 collector current increases, the voltage at the emitter of Q5 decreases, thereby reducing the base-emitter voltage of Q5. This in turn reduces Q5 base and emitter current, and also Q6 base and collector current.

4. MAINTENANCE

The following adjustments should not be performed as routine maintenance procedures, but only when a failure indicates a definite need. All tests are performed with all assembly connections in normal contact except those specified.

NOTE

J1 plugs directly into the A1 assembly through the chassis. Therefore it will be necessary to remove the A1 assembly from the chassis to gain access to J1. Leave all other connections to A2 connected unless otherwise specified.

4.1 LO No. 1 Amplifier Test

a. Set the front panel controls as follows:

Frequency: 10.000000 MHz

Mode: USB

AGC: OFF

RF Gain: Fully clockwise (cw)

b. Monitor A2 TP1 with an oscilloscope and frequency counter (each capable of measuring signals to 100 MHz). Signal at TP1 should be approximately 7.5 V_{pp} at 50.455000 MHz.

4.2 Postmixer IF Amplifier Adjustments/Test

a. Set the front panel controls as follows:

Frequency: 10.000000 MHz

Mode: USB

AGC: OFF

RF Gain: Fully clockwise (cw)

b. Connect equipment as shown in figure 1.

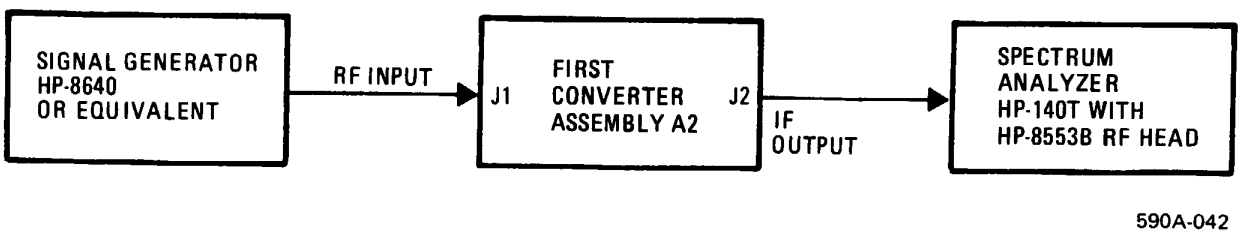


Figure 1. A2 Postmixer IF Amplifier Test Setup

c. Apply a -20 dBm, 10.000000 MHz test signal to RF input J1. Monitoring IF output J2 with a spectrum analyzer at 40.455 MHz, adjust L6 and L7 for maximum output. Output must be -20 dBm ± 2 dB, indicating an overall module gain of 0 dB.

4.3 AGC Test

a. Set the front panel controls as follows:

Frequency: 10.000000 MHz

Mode: USB

AGC: OFF

RF Gain: Fully clockwise (cw)

b. Connect equipment as shown in figure 2.

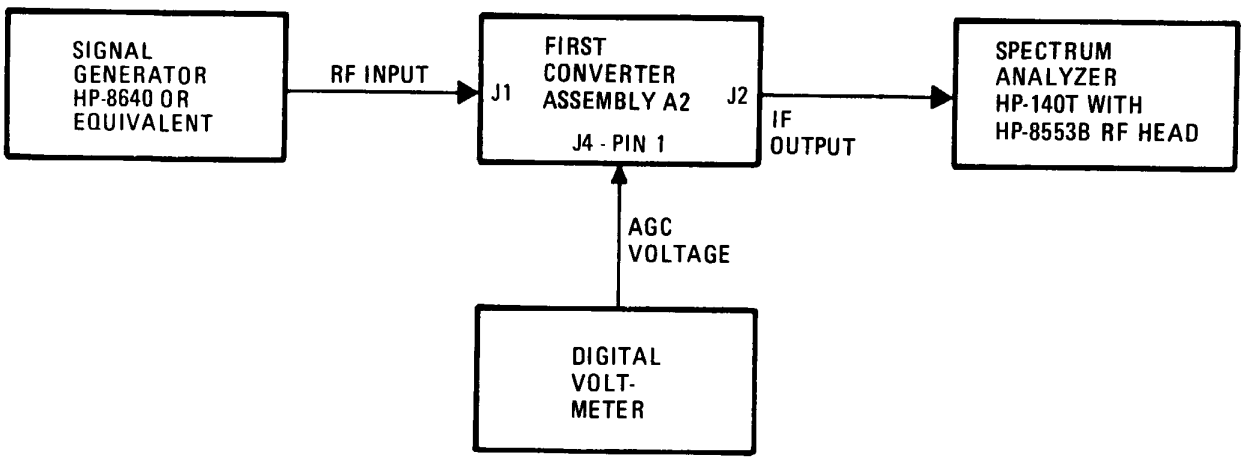


Figure 2. A2 AGC Test Setup

c. Adjust signal generator to approximately -20 dBm at 10.000000 MHz. Monitor IF output J2 on spectrum analyzer. IF output must be -20 dBm ± 2 dB.

d. Slowly turn the front panel RF Gain Control counterclockwise (ccw). An AGC voltage range of 0 to -6 Vdc should result in an IF output gain reduction range of approximately 0 to -20 dB. Intermediate levels are given in table 2.

Table 2. A2 AGC - Gain Reduction Data

AGC Voltage, Volts	Gain Reduction, - dB
0	0
-1	-7.5, ± 2
-2	-14.0, ± 2
-3	-18.0, ± 2
-4	-21.0, ± 2
-5	-23.0, ± 2
-6	-25.0, ± 2

4.4 BITE Test/Alignment

a. Set the front panel controls as follows:

Frequency: 10.000000 MHz

Mode: USB

AGC: OFF

RF Gain: Fully clockwise (cw)

b. Connect equipment as shown in figure 3.

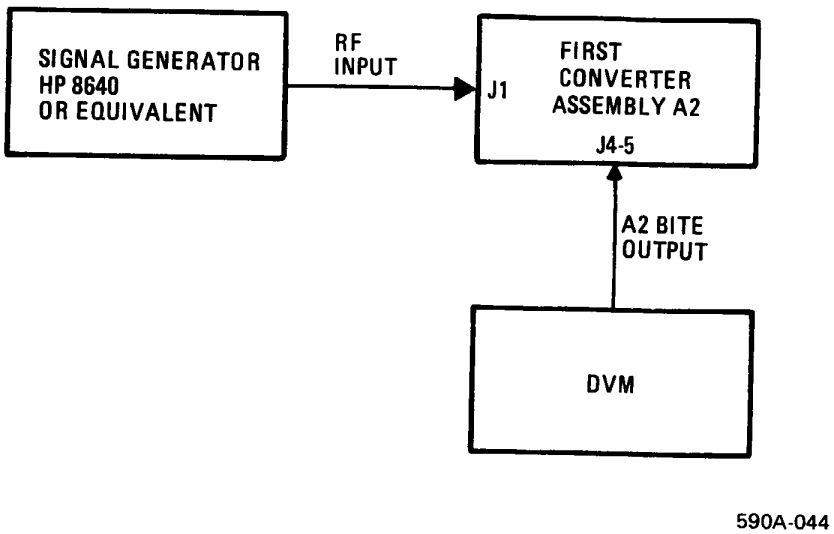


Figure 3. A2 BITE Test Setup

c. Set signal generator to 10.000000 MHz, -20 dBm. Adjust L8 for a peak indication on the DVM. DVM should indicate approximately .75 Vdc.

d. Disconnect all equipment and reconnect A2 to the Receiver. Initiate Receiver BITE test. The Receiver must pass A2 BITE testing.

5. PARTS LIST

Table 3 is a comprehensive parts list of all replaceable components in First Converter Assembly A2. When ordering parts from the factory, include a full description of the part. Use figure 4, First Converter Assembly A2 component location diagram to identify parts.

6. SCHEMATIC DIAGRAM

Figure 5 is the First Converter Assembly A2 schematic diagram.

Table 3. First Converter Assembly A2 Parts List (PL 10073-5200, Rev. U/-5200-02, Rev. C)

Ref. Desig.	Part Number	Description
C1	CM04ED330J03	CAP 33PF 5% 500V MICA
C2	CM04ED330J03	CAP 33PF 5% 500V MICA
C3	M39014/01-1535	CAP .01UF 10% 100V CER-R
C4	M39014/01-1535	CAP .01UF 10% 100V CER-R
C5	M39014/01-1535	CAP .01UF 10% 100V CER-R
C6	M39014/01-1535	CAP .01UF 10% 100V CER-R
C7	C26-0025-100	CAP 10UF 20% 25V TANT
C8	C26-0025-100	CAP 10UF 20% 25V TANT
C9	M39014/01-1535	CAP .01UF 10% 100V CER-R
C10	M39014/01-1535	CAP .01UF 10% 100V CER-R
C11	M39014/01-1535	CAP .01UF 10% 100V CER-R
C12	M39014/01-1535	CAP .01UF 10% 100V CER-R
C13	M39014/01-1535	CAP .01UF 10% 100V CER-R
C14	M39014/01-1535	CAP .01UF 10% 100V CER-R
C15	M39014/01-1535	CAP .01UF 10% 100V CER-R
C16	CM04CD150J03	CAP 15PF 5% 500V MICA
C17	CM04CD150J03	CAP 15PF 5% 500V MICA
C18	M39014/01-1535	CAP .01UF 10% 100V CER-R
C19	CM04ED330J03	CAP 33PF 5% 500V MICA
C20	CM04ED330J03	CAP 33PF 5% 500V MICA
C21	M39014/01-1535	CAP .01UF 10% 100V CER-R
C22	M39014/01-1535	CAP .01UF 10% 100V CER-R
C23	M39014/01-1535	CAP .01UF 10% 100V CER-R
C24	M39014/01-1535	CAP .01UF 10% 100V CER-R
C25	M39014/01-1535	CAP .01UF 10% 100V CER-R
C26	CM04CD050D03	CAP 5PF + -.5PF 500V MICA
C27	M39014/02-1310	CAP .1UF 10% 100V CER-R
C28	C26-0025-339	CAP 3.3UF 20% 25V TANT
C29	M39014/01-1535	CAP .01UF 10% 100V CER-R
C30	M39014/01-1535	CAP .01UF 10% 100V CER-R
C31	M39014/02-1310	CAP .1UF 10% 100V CER-R
C32	M39014/01-1535	CAP .01UF 10% 100V CER-R
C33	CM04ED390J03	CAP 39PF 5% 500V MICA
C34	M39014/01-1535	CAP .01UF 10% 100V CER-R
C35	M39014/01-1535	CAP .01UF 10% 100V CER-R
C36	M39014/01-1535	CAP .01UF 10% 100V CER-R
C37	M39014/02-1310	CAP .1UF 10% 100V CER-R
C38	M39014/01-1535	CAP .01UF 10% 100V CER-R
C39	C26-0025-339	CAP 3.3UF 20% 25V TANT
C40	M39014/02-1310	CAP .1UF 10% 100V CER-R
C41	M39014/01-1535	CAP .01UF 10% 100V CER-R
C42	M39014/02-1310	CAP .1UF 10% 100V CER-R
C43	C26-0025-339	CAP 3.3UF 20% 25V TANT

Table 3. First Converter Assembly A2 Parts List (PL 10073-5200, Rev. U/-5200-02, Rev. C) (Cont.)

Ref. Desig.	Part Number	Description
C44	M39014/01-1535	CAP .01UF 10% 100V CER-R
C45	CM04CD050D03	CAP 5PF +-.5PF 500V MICA
C46	CM04ED510J03	CAP 51PF 5% 500V MICA
C47	CM04ED510J03	CAP 51PF 5% 500V MICA
C48	C26-0025-339	CAP 3.3UF 20% 25V TANT
C49	M39014/01-1535	CAP .01UF 10% 100V CER-R
C50	M39014/01-1535	CAP .01UF 10% 100V CER-R
C51	M39014/01-1535	CAP .01UF 10% 100V CER-R
C52	M39014/01-1535	CAP .01UF 10% 100V CER-R
CR1	D12-0007-001	DIODE PIN ATTN 1W 9301
CR2	D12-0007-001	DIODE PIN ATTN 1W 9301
CR3	1N4454	DIODE 200MA 75V SW
CR4	1N4454	DIODE 200MA 75V SW
CR5	1N3064	DIODE 75mA 75V SW
CR6	1N5231B	DIODE 5.1V 5% .5W ZENER
FL1	10073-7000	FILTER,40.455 MHZ
J1	J-0031	CONN SMB VERT PCB F
J2	J-0031	CONN SMB VERT PCB F
J3	J-0031	CONN SMB VERT PCB F
J4	J46-0022-005	HDR 5 PIN 0.100" SR LKG
L1	MS14046-4	COIL 10UH 10% FXD RF
L2	MS14046-4	COIL 10UH 10% FXD RF
L3	MS14046-4	COIL 10UH 10% FXD RF
L4	MS14046-4	COIL 10UH 10% FXD RF
L5	L08-0001-001	CHOKE W B 50 MHZ
L6	L11-0004-005	INDUCT SH VAR .198-.242UH
L7	L11-0004-005	INDUCT SH VAR .198-.242UH
L8	L11-0004-013	INDUCT SH VAR .900-1.1 UH
L9	MS90538-12	COIL 100UH 5% FXD RF
L10	MS75084-12	COIL 10UH 10% FXD RF
Q1	Q35-0004-001	XSTR JFET U431
Q2	Q35-0004-001	XSTR JFET U431
Q3	Q35-0001-001	XSTR JFET J310
Q4	2N3866	XSTR SS/RF NPN TO-39
Q5	2N4037	XSTR SS/RF NPN TO-39
Q6	Q25-0014-000	XSTR RF VHF 4W MRF237
Q7	Q35-0001-001	XSTR JFET J310
R1	R65-0003-301	RES 300 5% 1/4W CAR FILM
R2	R65-0003-301	RES 300 5% 1/4W CAR FILM
R3	RCR20G180JM	RES 18 5% 1/2W CAR COMP
R4	R65-0003-510	RES 51 5% 1/4W CAR FILM
R5	R65-0003-910	RES 91 5% 1/4W CAR FILM
R6	R65-0003-910	RES 91 5% 1/4W CAR FILM
R7	R65-0003-222	RES 2.2K 5% 1/4W CAR FILM
R8	R65-0003-222	RES 2.2K 5% 1/4W CAR FILM

Table 3. First Converter Assembly A2 Parts List (PL 10073-5200, Rev. U/-5200-02, Rev. C) (Cont.)

Ref. Desig.	Part Number	Description
R9	R65-0003-510	RES 51 5% 1/4W CAR FILM
R10	R65-0003-104	RES 100K 5% 1/4W CAR FILM
R11	R65-0003-181	RES 180 5% 1/4W CAR FILM
R12	R65-0003-224	RES 220K 5% 1/4W CAR FILM
R13	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R14	R65-0003-100	RES 10 5% 1/4W CAR FILM
R15	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R16	R65-0003-272	RES 2.7K 5% 1/4W CAR FILM
R17	R65-0003-270	RES 27 5% 1/4W CAR FILM
R18	R65-0003-221	RES 220 5% 1/4W CAR FILM
R19	R65-0003-680	RES 68 5% 1/4W CAR FILM
R20	R65-0003-101	RES 100 5% 1/4W CAR FILM
R21	R65-0003-681	RES 680 5% 1/4W CAR FILM
R22	R65-0003-272	RES 2.7K 5% 1/4W CAR FILM
R23	RCR32G100JM	RES 10 5% 1W CAR COMP
R24	RCR32G100JM	RES 10 5% 1W CAR COMP
R25	R65-0003-301	RES 300 5% 1/4W CAR FILM
R26	R65-0003-101	RES 100 5% 1/4W CAR FILM
R27	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R28	R65-0003-181	RES 180 5% 1/4W CAR FILM
R29	R65-0003-101	RES 100 5% 1/4W CAR FILM
R30	R65-0003-431	RES 430 5% 1/4W CAR FILM
R31	R65-0003-120	RES 12 5% 1/4W CAR FILM
R32	R65-0003-431	RES 430 5% 1/4W CAR FILM
T1	10073-7013	TRANSFORMER ASSY
T2	10073-7013	TRANSFORMER ASSY
T3	10073-7005	TRANSFORMER, RF, FIXED
T4	10073-7005	TRANSFORMER, RF, FIXED
T5	10073-7010	TRANSFORMER, RF, FIXED
TP1	J-0071	TP PWB BRN TOP ACCS .080"
TP2	J-0066	TP PWB RED TOP ACCS .080"
TP3	J-0069	TP PWB ORN TOP ACCS .080"
TP4	J-0070	TP PWB YEL TOP ACCS .080"
U1	I51-0003-002	MIXER DB SAY-1

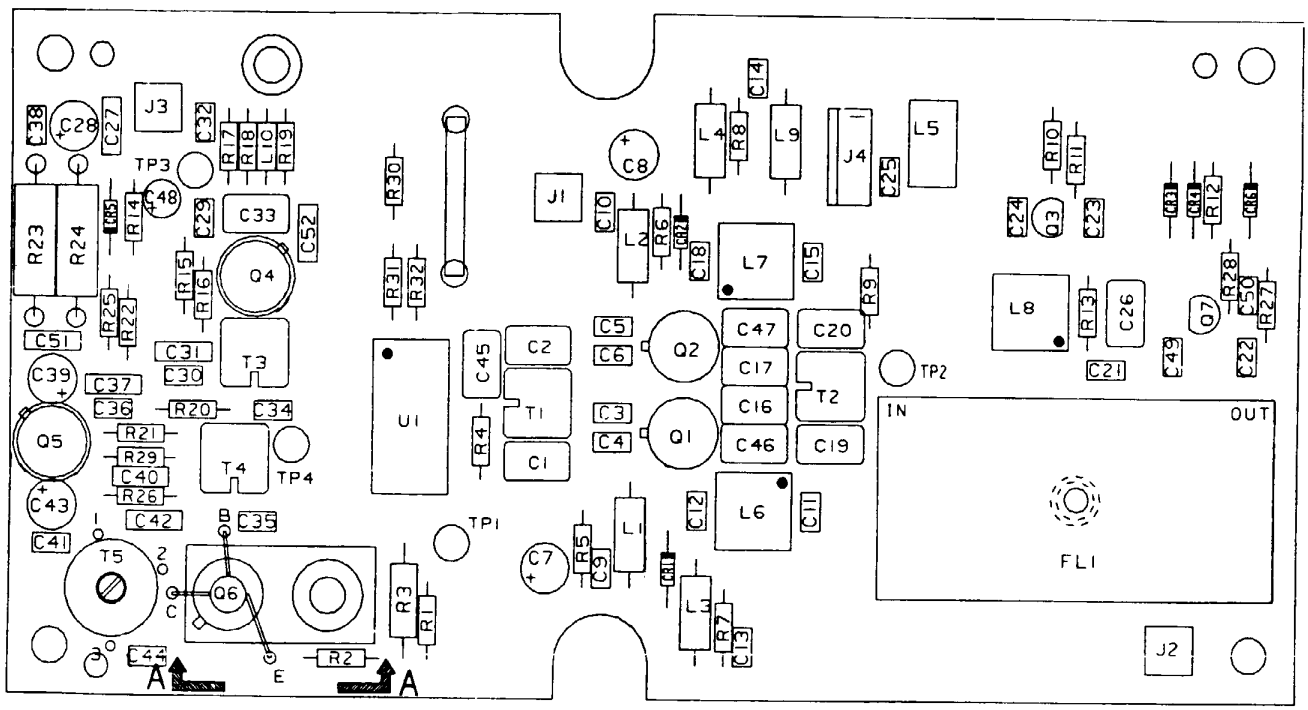


Figure 4. First Converter Assembly A2 Component Location Diagram (10073-5200, Rev. G)

NOTE: UNLESS OTHERWISE SPECIFIED:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR A COMPLETE DESIGNATION, PREFIX WITH UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.
2. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, ±5%.
3. ALL CAPACITOR VALUES ARE IN MICROFARADS.
4. ALL INDUCTOR VALUES ARE IN MICROHENRIES.
5. LEVELS SPECIFIED CORRESPOND TO A 0 DBM, 10KHZ-30 MHZ SIGNAL INJECTED AT J1.
6. LEVELS SPECIFIED CORRESPOND TO A -20 DBM, 10KHZ-30 MHZ SIGNAL INJECTED AT J1.
7. DC VOLTAGES AT TRANSISTORS ARE SPECIFIED FOR NO RF INPUTS.
8. VENDOR PART NO. CALLOUTS ARE FOR REFERENCE ONLY. COMPONENTS ARE SUPPLIED PER PART NO. IN PARTS LIST.

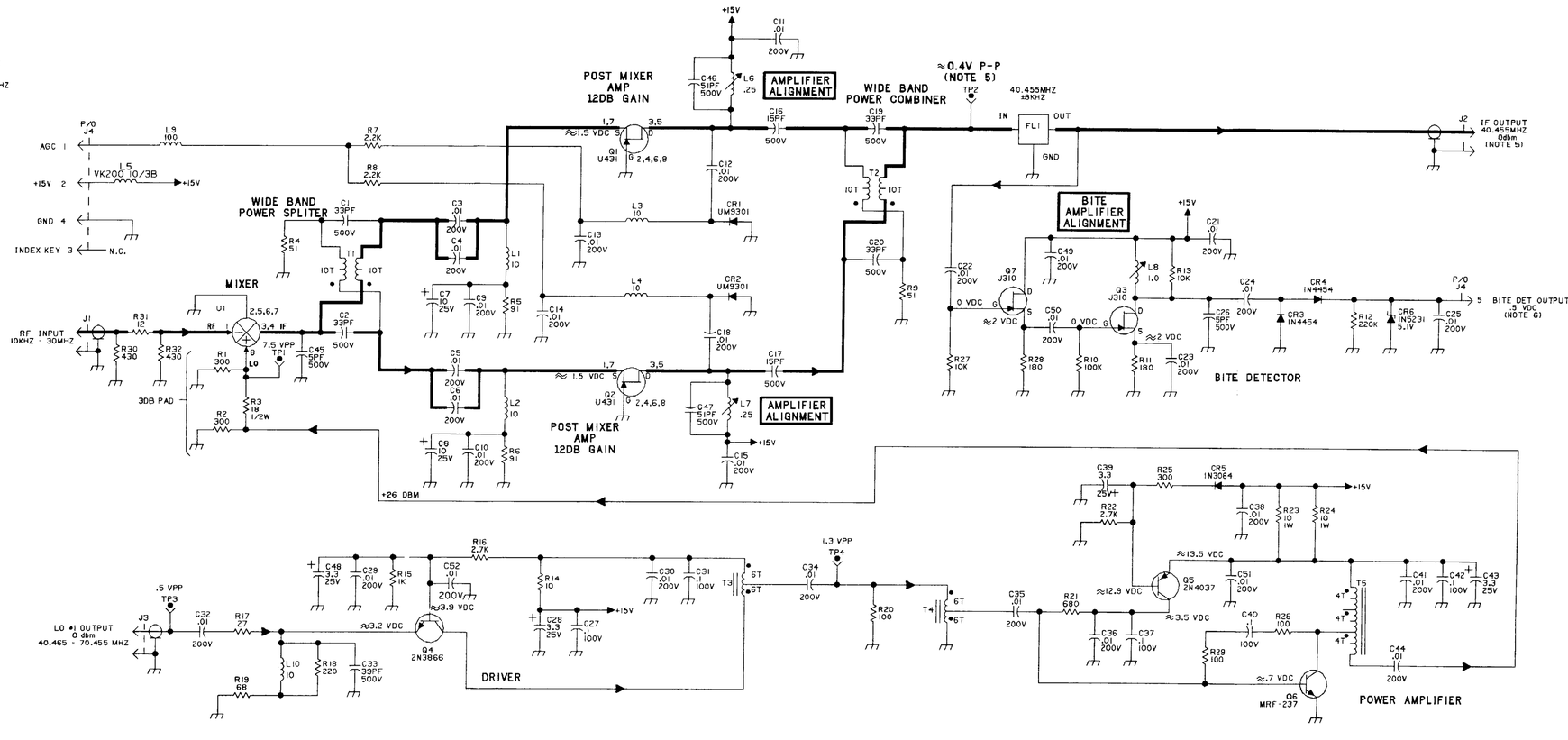
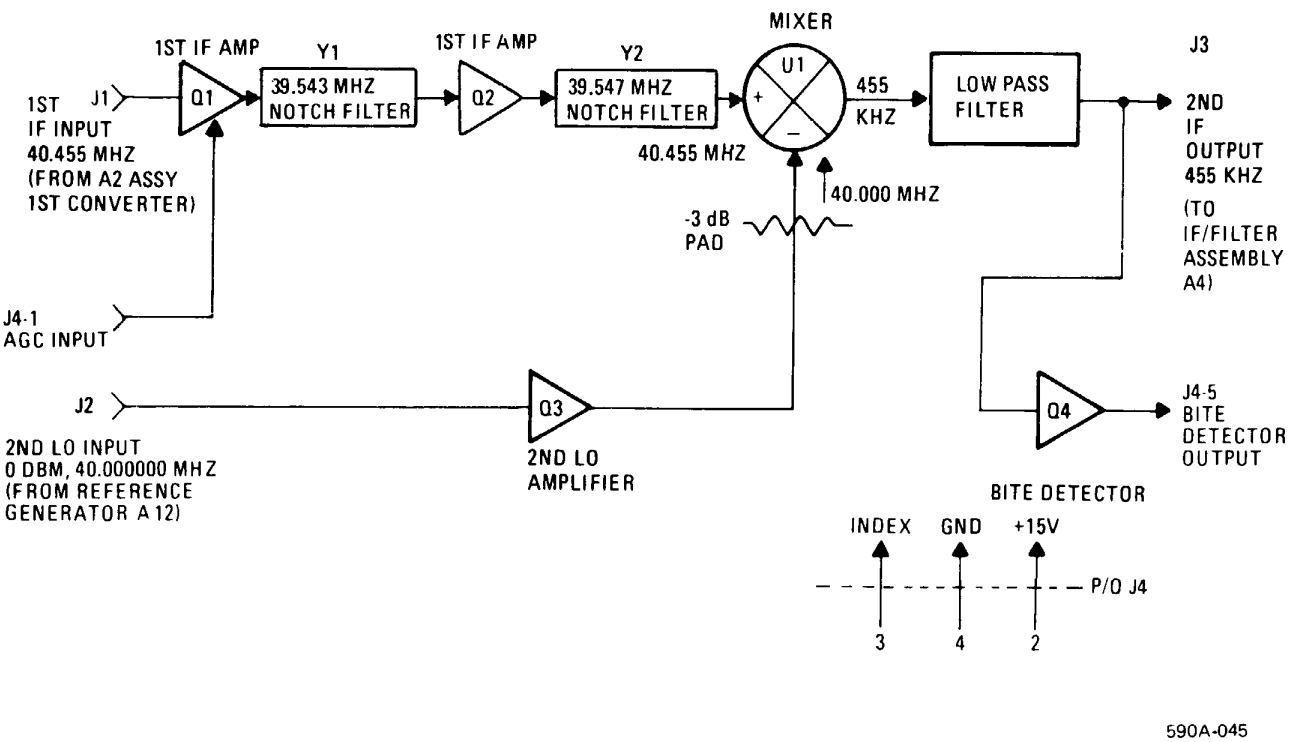


Figure 5. First Converter Assembly A2 Schematic Diagram (10073-5201, Rev. G)

A3
SECOND CONVERTER ASSEMBLY



590A-045

TABLE OF CONTENTS

Paragraph		Page
1.	General Description	1
2.	Interface Connections	1
3.	Circuit Description	1
3.1	IF Amplifiers and Mixer	1
3.2	BITE Detection Circuit	2
3.3	LO No. 1 Amplifier	2
4.	Maintenance	2
4.1	LO No. 1 Amplifier Test	2
4.2	IF Amplifiers and Mixer Adjustments/Test	2
4.3	AGC Test	3
4.4	BITE Test	4
5.	Parts List	5
6.	Schematic Diagram	5

LIST OF FIGURES

Figure		Page
1	A3 IF Amplifier Test Setup	3
2	A3 AGC Test Setup	4
3	A3 BITE Test Setup	5
4	Second Converter Assembly A3 Component location Diagram (10215-5300)	8
5	Second Converter Assembly A3 Schematic Diagram (10215-5301)	9

LIST OF TABLES

Table		Page
1	Second Converter A3 Interface Connections	1
2	A3 AGC - Gain Reduction Data	4
3	Second Converter Assembly A3 Parts List (PL 10215-5300)	6

A3 SECOND CONVERTER ASSEMBLY

1. GENERAL DESCRIPTION

Second Converter Assembly A3 converts the first IF of 40.455 (from First Converter Assembly A2) to a second IF of 455 kHz. Overall module gain from J1 to J3 is approximately 14 ± 2 dB.

Input 40.455 MHz first IF signals are applied through an automatic gain controlled amplifier and passed on to a fixed gain stage. Each amplifier incorporates a crystal notch filter. At this point the signal is down converted to 455 kHz, filtered, and fed out to IF Filter Assembly A4. The second IF signal is also monitored by the BITE detection circuit which monitors the operation of the Second Converter Assembly.

2. INTERFACE CONNECTIONS

Table 1 details the various input/output connections and any relevant data.

Table 1. Second Converter A3 Interface Connections

Connector	Function	Characteristics
J1	First IF Input	40.455 MHz, -120/-9 dBm (under AGC control), Zo = 50 ohms
J2	Second LO Input	40.000 MHz, 0 dBm, Zo = 50 ohms
J3	Second IF Output	455 kHz, -107/-15 dBm (under AGC control), Zo = 50 ohms
J4-1	AGC Input	0 to -6 Vdc produces a 0 to -20 dB gain reduction
J4-2	Power	+ 15 Vdc at 60 mA
J4-3	Index pin	
J4-4	Ground	
J4-5	BITE Output	2.25 - 3 Vdc for -20 dBm input at J1

3. CIRCUIT DESCRIPTION

3.1 IF Amplifiers and Mixer

First IF input signals from First Converter Assembly A2 are received at J1 and fed to grounded gate FET amplifier Q1. C1 and L4 perform an impedance transformation of 50 ohms to Q1's source impedance for optimum power gain. C2 and R1 form a bypassed bias resistor network. L1, C25, and C5 provide impedance transformation for Q1's drain load of 2200 ohms to 50 ohms. This yields an overall stage gain of 13 dB. Crystal Y1 is series resonant at 39.543 MHz and produces a notch filter at this frequency.

CR1 provides gain reduction by reducing Q1's drain load upon application of a negative AGC voltage at R2 (AGC input). Typically -20 dB of gain reduction is possible.

Q2 and its associated components perform identically to amplifier Q1, except that no AGC is applied. This fixed gain stage also has an overall gain of 13 dB. Crystal Y2 produces a notch at 39.547 MHz.

The combined effects of crystals Y1 and Y2 create a notch filter to reject the second IF image frequency, which is an undesired response.

U1 is a low LO level diode ring mixer that converts the 40.455 MHz first IF to the 455 kHz second IF. A LO drive level of + 7 dBm (50 ohm) at 40.000000 MHz is supplied by Q3 (paragraph 3.3). U1 typically has 6 dB of conversion loss.

Components C10, C12 and L7 form a low-pass filter to reject all undesired mixer products (especially LO leakage). This allows only 455 kHz to pass out of J3 to IF Filter Assembly A4 and ultimately to the high gain second IF amplifiers on IF/Audio Assembly A5.

3.2 BITE Detection Circuit

The 455 kHz second IF signal is also applied to common emitter amplifier Q4. Bias circuitry R7, R8, and R11 bias Q4 to 10 mA of collector current. R9, R10, and C16 set the voltage gain to allow BITE to operate when the signal at J1 is at -20 dBm. The dc detection voltage produced by detector network CR2, CR4, and C17 under these conditions is approximately 2.25 to 3 Vdc at J4-5, BITE Detector output.

3.3 LO No. 1 Amplifier

Common emitter amplifier Q3 receives a 40.000000 MHz, 0 dBm drive signal from Reference Generator Assembly A12 at J2. R14, R15, CR3, and R17 bias Q3 to 23 mA of collector current. R16-C21 and R18 comprise emitter and collector to base feedback networks. These networks simultaneously set the stage gain to + 10 dB and the input and output impedances to 50 ohms. A + 10 dBm signal is fed to -3 dB, 50 ohm pad R19-R21. This applies a + 7 dBm LO level to mixer U1.

4. MAINTENANCE

The following adjustments should not be performed as routine maintenance procedures, but only when a failure indicates a definite need. All tests should be performed with all assembly connections in normal contact unless otherwise specified.

4.1 LO No. 1 Amplifier Test

a. Set the front panel controls as follows:

Frequency: 10.000000 MHz

Mode: USB

AGC: OFF

RF Gain: Fully clockwise (cw)

b. Monitor TP4 with an oscilloscope and frequency counter. Signal at TP4 would be 40.000000 MHz at approximately 1.5 V_{pp}.

4.2 IF Amplifiers and Mixer Adjustments/Test

a. Set the front panel controls as follows:

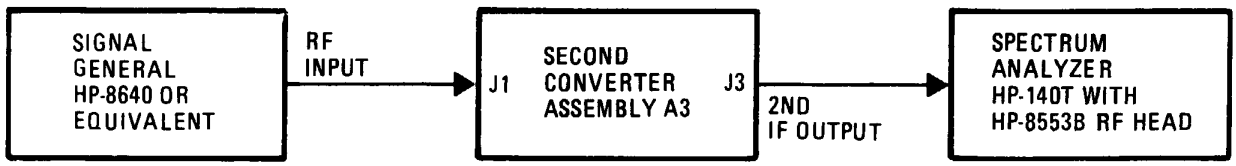
Frequency: 10.000000 MHz

Mode: USB

AGC: OFF

RF Gain: Fully clockwise (cw)

b. Connect equipment as shown in figure 1.



590A-046

Figure 1. A3 IF Amplifier Test Setup

c. Apply a -30 dBm, 40.455 MHz signal at J1. Monitor second IF output J3 at 455 kHz on the spectrum analyzer. Adjust L1 and L2 for maximum output. Output must be -15 dBm ± 2 dB, indicating approximately 15 dB of module gain.

4.3 AGC Test

a. Set the front panel controls as follows:

Frequency: 10.000000 MHz

Mode: USB

AGC: OFF

RF Gain: Fully clockwise (cw)

b. Connect equipment as shown in figure 2.

c. Adjust Signal Generator to -30 dBm, 40.455 MHz. Monitor second IF output J3 on spectrum analyzer. IF Output must be -15 dBm ± 3 dB.

d. Slowly adjust the front panel RF gain control counterclockwise (ccw). An AGC voltage range of 0 to -6 Vdc should result in an IF output gain reduction of approximately 0 to -24 dB. Intermediate levels are given in table 2. Reset RF gain control fully clockwise (cw).

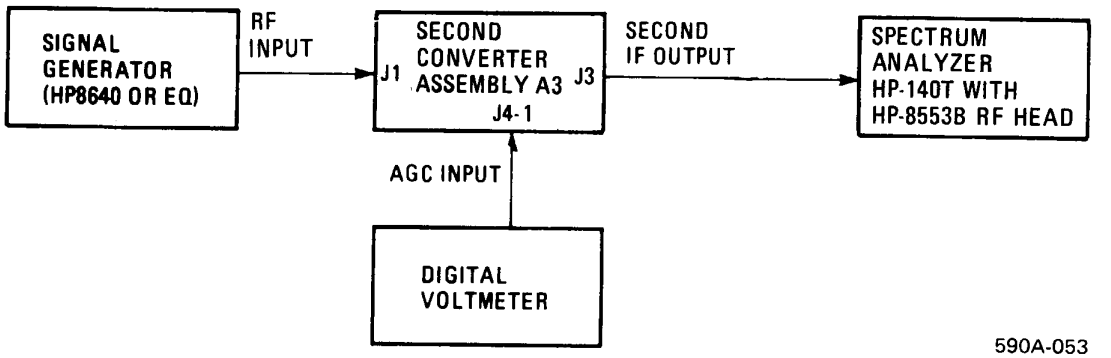


Figure 2. A3 AGC Test Setup

Table 2. A3 AGC - Gain Reduction Data

AGC Voltage, Volts	Gain Reduction, - dB
0	0
-1	-8, ± 2
-2	-14, ± 2
-3	-17, ± 2
-4	-20, ± 2
-5	-22, ± 2
-6	-24, ± 2

4.4 BITE Test

a. Set the front panel controls as follows:

Frequency: 10.000000 MHz

Mode: USB

AGC: OFF

RF Gain: Fully clockwise (cw)

b. Connect equipment as shown in figure 3.

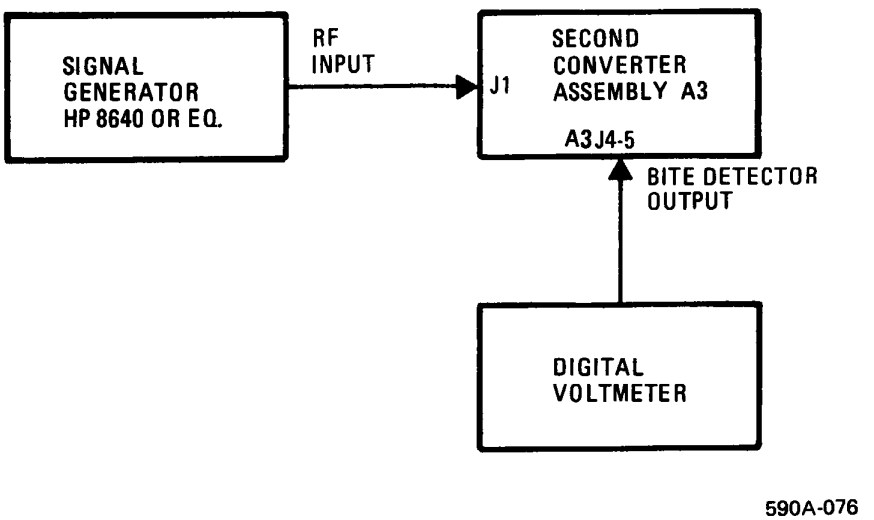


Figure 3. A3 BITE Test Setup

c. Set signal generator to -20 dBm at 40.455 MHz. BITE output voltage must be approximately 2.25 to 3 Vdc.

d. Disconnect all equipment and reconnect the A3 assembly. Initiate the BITE test. The receiver must pass A3 BITE testing.

5. PARTS LIST

Table 3 is a comprehensive parts list of all replaceable components in Second Converter Assembly A3. When ordering parts from the factory, include a full description of the part. Use figure 4, the Second Converter Assembly component location diagram to identify parts.

6. SCHEMATIC DIAGRAM

Figure 5 is the Second Converter Assembly schematic diagram.

Table 3. Second Converter Assembly A3 Parts List (PL 10215-5300)

Ref. Desig.	Part Number	Description
C1	CM04FD131J03	CAP 130PF 5% 500V MICA
C2	M39014/01-1535	CAP .01UF
C3	M39014/01-1535	CAP .01UF
C4	M39014/01-1535	CAP .01UF
C5	CM04CD120J03	CAP 12PF 5% 500V MICA
C6	M39014/01-1535	CAP .01UF
C8	M39014/01-1535	CAP .01UF
C9	CM04CD120J03	CAP 12PF 5% 500V MICA
C10	M39014/02-1298	CAP 01UF
C12	M39014/02-1298	CAP 01UF
C13	M39014/02-1320	CAP, CER, ,47UF,
C14	M39014/02-1310	CAP .1 UF
C15	M39014/02-1320	CAP, CER, ,47UF,
C16	M39014/02-1320	CAP, CER, ,47UF,
C17	M39014/02-1310	CAP .1 UF
C18	M39014/01-1535	CAP .01UF
C19	M39014/01-1535	CAP .01UF
C20	M39014/01-1535	CAP .01UF
C21	M39014/01-1535	CAP .01UF
C22	M39014/01-1535	CAP .01UF
C23	M39014/02-1320	CAP, CER, ,47UF,
C24	CM04CD150J03	CAP 15PF 5% 500V MICA
C25	CM04CD150J03	CAP 15PF 5% 500V MICA
C26	M39014/01-1535	CAP .01UF
CR1	D12-0007-001	DIODE UM9301
CR2	1N4454	DIODE, SS SILICON
CR3	1N4454	DIODE, SS SILICON
CR4	1N4454	DIODE, SS SILICON
J1	J-0031	CONNECTOR, COAX, SNAP-ON
J2	J-0031	CONNECTOR, COAX, SNAP-ON
J3	J-0031	CONNECTOR, COAX, SNAP-ON
J4	J46-0022-005	CONN HEADER 5 PIN
L1	L11-0004-008	COIL, VARIABLE
L2	L11-0004-008	COIL, VARIABLE
L3	MS14046-6	COIL, RF 15 UH 10%
L4	MS75083-9	COIL, RF 0.47 UH 10%
L7	MS14046-7	COIL, RF 18 UH 10%
L9	MS14046-6	COIL, RF 15 UH 10%
L10	MS90539-15	COIL, RF 1000 UH 5%
Q1	Q35-0001-001	XSTR, JFET, J310
Q2	Q35-0001-001	XSTR, JFET, J310
Q3	2N5109	XSTR, RF PWR
Q4	2N2222A	XSTR, SS/GP, NPN
R1	RN55D1820F	RES,182.0 1% 1/8W MET FLM
R2	R65-0003-392	RES,3.9K 5% 1/4W CAR FILM
R3	RN55D1820F	RES,182.0 1% 1/8W MET FLM

Table 3. Second Converter Assembly A3 Parts List (PL 10215-5300) (Cont.)

Ref. Desig.	Part Number	Description
R4	R65-0003-101	RES,100 5% 1/4W CAR FILM
R6	R65-0003-101	RES,100 5% 1/4W CAR FILM
R7	R65-0003-103	RES,10K 5% 1/4W CAR FILM
R8	R65-0003-512	RES,5.1K 5% 1/4W CAR FILM
R9	R65-0003-561	RES,560 5% 1/4W CAR FILM
R10	R65-0003-270	RES,27 5% 1/4W CAR FILM
R11	R65-0003-431	RES,430 5% 1/4W CAR FILM
R12	R65-0003-103	RES,10K 5% 1/4W CAR FILM
R13	R65-0003-101	RES,100 5% 1/4W CAR FILM
R14	R65-0003-242	RES,2.4K 5% 1/4W CAR FILM
R15	R65-0003-471	RES,470 5% 1/4W CAR FILM
R16	R65-0003-399	RES,3.9 5% 1/4W CAR FILM
R17	R65-0003-101	RES,100 5% 1/4W CAR FILM
R18	R65-0003-681	RES,680 5% 1/4W CAR FILM
R19	R65-0003-301	RES,300 5% 1/4W CAR FILM
R20	R65-0003-180	RES,18 5% 1/4W CAR FILM
R21	R65-0003-301	RES,300 5% 1/4W CAR FILM
TP1	J-0071	TIP JACK, BROWN
TP3	J-0069	TIP JACK, ORANGE
TP4	J-0070	TIP JACK, YELLOW
U1	I51-0003-001	MIXER
Y1	10215-5315	CRYSTAL, 39.543 MHZ
Y2	10215-5325	CRYSTAL, 39.547 MHZ

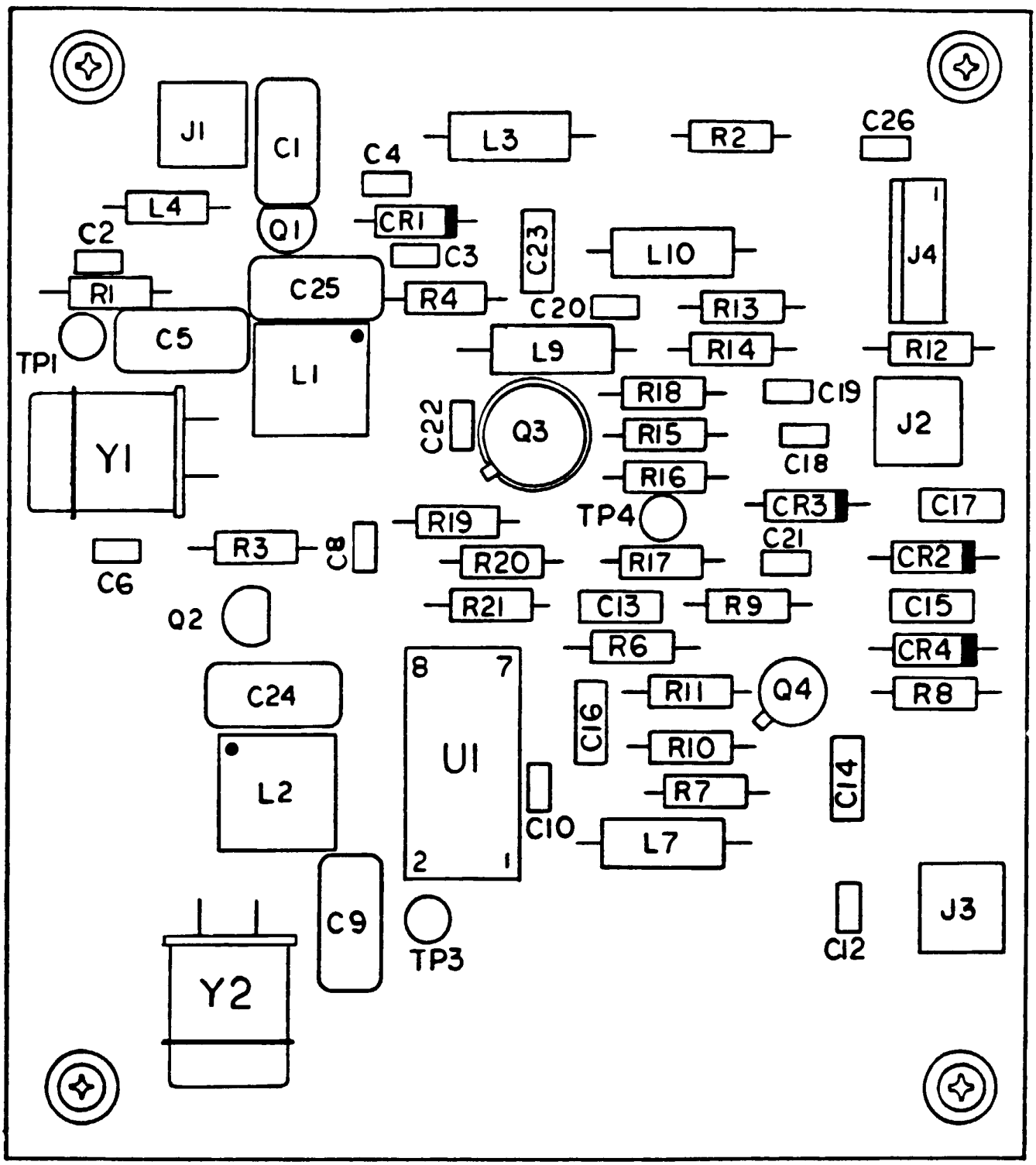


Figure 4. Second Converter Assembly A3 Component Location Diagram (10215-5300)

NOTE: UNLESS OTHERWISE SPECIFIED:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR A COMPLETE DESIGNATION, PREFIX WITH UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.
2. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, ±5%.
3. ALL CAPACITOR VALUES ARE IN MICROFARADS, 200VDC.
4. VENDOR PART NO. CALLOUTS ARE FOR REFERENCE ONLY. COMPONENTS ARE SUPPLIED PER PART NO. IN PARTS LIST.
5. LEVELS SPECIFIED ARE FOR A -30 DBM, 40.455 MHZ SIGNAL INJECTION AT J1.
6. LEVELS SPECIFIED ARE FOR A -20 DBM, 40.455 MHZ SIGNAL INJECTION AT J1.
7. DC VOLTAGES AT TRANSISTORS ARE SPECIFIED FOR NO RF INPUT.

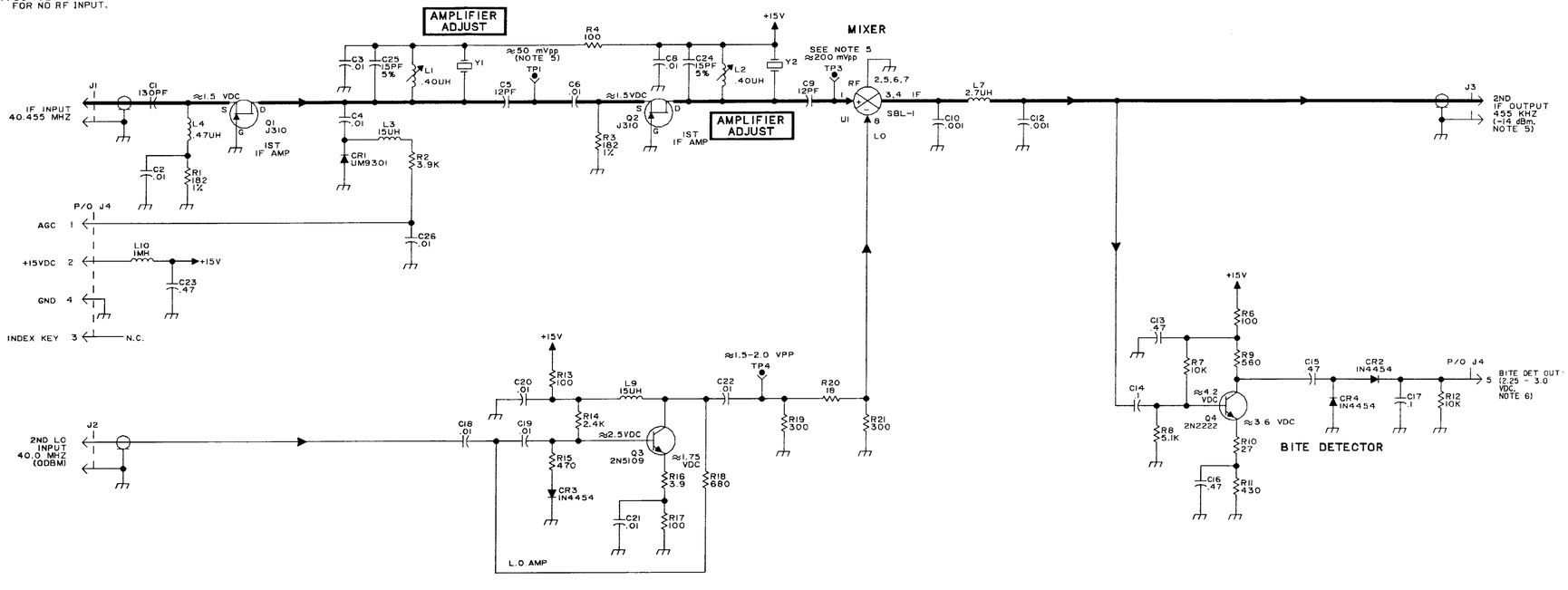
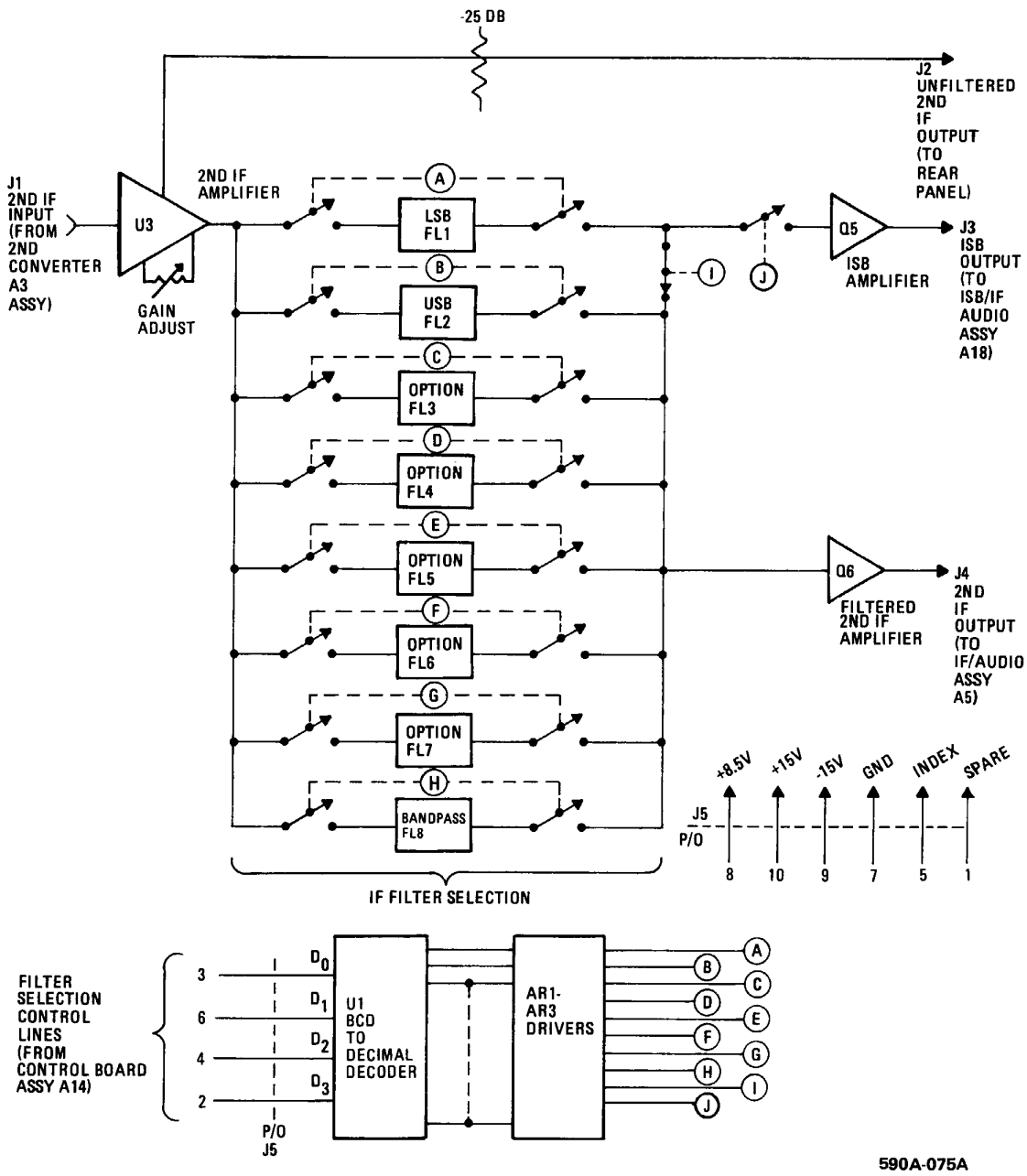


Figure 5. Second Converter Assembly A3 Schematic Diagram (10215-5301, Rev. C)

A4
IF FILTER ASSEMBLY



590A-075A

TABLE OF CONTENTS

Paragraph		Page
1.	General Description	1
2.	Interface Connections	2
3.	Circuit Description	2
3.1	Input/Output Amplifiers	2
3.2	Filter Selection	3
3.2.1	LSB Operation	3
3.2.2	ISB Operation	4
4.	Maintenance	4
4.1	Input/Output Amplifier Test/Adjustment	4
4.2	Filter Selection Test	5
5.	Parts List	5
6.	Schematic Diagrams	5

LIST OF FIGURES

Figure		Page
1	A4 I/O Amplifiers Test Setup	4
2	IF Filter Assembly A4 Component Location Diagram (10073-5500)	10
3	IF Filter Assembly A4 Schematic Diagram (10073-5501)	11

LIST OF TABLES

Table		Page
1	Typical Filter Complement	1
2	IF Filter Assembly A4 Interface Connections	2
3	A4 Filter Selection	3
4	IF Filter Assembly A4 Parts List (PL 10073-5500-06)	5

A4 IF FILTER ASSEMBLY

1. GENERAL DESCRIPTION

IF Filter Assembly A4 contains provisions for automatically selecting one of eight bandpass filters. The main signal frequency selectivity is determined by these filters. Actual filter bandwidths which may be employed are customer specified and depend upon operational modes desired (see note below). Table 1 shows a typical filter complement in the Receiver. Automatic filter selection is accomplished via flexible programmable logic circuitry on Control Assembly A14.

NOTE

Filter positions FL1 and FL2 must be reserved for LSB and USB (respectively) if ISB operation is desired. (ISB operation requires the simultaneous selection of two filters.) Filter position FL8 is for wideband operation.

Table 1. Typical Filter Complement

Mode of Operation	Filter Selected	Specified Bandwidth
LSB-ISB	FL1	2.7 kHz
USB	FL2	2.7 kHz
CW	FL3	.3 kHz
Optional	FL4	---
Optional	FL5	---
AM	FL6	6.0 kHz
Optional	FL7	---
FM or AM	FL8	16 kHz

Input signals at 455 kHz (nominally) arrive at J2 from Second Converter Assembly A3. Three A4 signal outputs are derived.

- Filtered Second IF output at J4. This output is fed to IF/Audio Assembly A5, and is chosen whenever SSB, AM, or FM detection is required.
- ISB output at J3. This output is fed to ISB IF/Audio Assembly A18 and is used whenever reception of LSB signals is required. For ISB operation, J3 carries the LSB signal to the A18 Assembly while J4 routes the USB signal to the A5 Assembly.
- Unfiltered second IF output at J2. This output is fed to rear panel connector J3, and is provided as a convenience whenever external signal processing of the wideband signal (present at J1) is required.

Overall assembly gain is set by R10 to nominally be 10 dB at J4 in the USB mode of operation. This also sets the ISB output gain (when used) to 10 dB, and the unfiltered second IF output to approximately 4 dB.

2. INTERFACE CONNECTIONS

Table 2 details the various input/output connections and other relevant data.

Table 2. IF Filter Assembly A4 Interface Connections

Connector	Function	Characteristics
J1	Unfiltered second IF Input	455 kHz, -107/-15 dBm, Zo = 50 ohms
J2	Unfiltered second IF output	455 kHz, -111/-19 dBm, Zo = 50 ohms
J3	LSB output to A18	455 kHz, -97/-5 dBm, Zo = 50 ohms
J4	Filtered second IF output	455 kHz, -97/-5 dBm, Zo = 50 ohms
J5-1	Spare	
J5-2	D3	Filter Select Line 3, TTL
J5-3	D0	Filter Select Line 0, TTL
J5-4	D2	Filter Select Line 2, TTL
J5-5	Index Pin	
J5-6	D1	Filter Select Line 1, TTL
J5-7	Ground	
J5-8	Power	+ 8.5 V at 8 mA
J5-9	Power	-15 V at 30 mA
J5-10	Power	+ 15 V at 100 mA

3. CIRCUIT DESCRIPTION

3.1 Input/Output Amplifiers

Unfiltered second IF signals at J1 are applied to second IF amplifier U3. U3 provides + 27 dB (nominal) of gain at each of two outputs, adjustable by R10. The output at pin 8 drives the selected filter input, and is adjusted by R10 for a nominal assembly gain of 10 dB with the USB filter selected.

The second U3 output at pin 7 is applied through 50 ohm matching network R75 and R77 to J2. This unfiltered 455 kHz IF output is then routed to rear panel connector J3. Output level under AGC action at this port is typically, -111/-19 dBm into 50 ohms.

Output source follower FET amplifier Q6 matches the high impedance filter outputs (5K ohms) to the low impedance IF/Audio Assembly A5 input (50 ohms). Q6 may normally receive signals from any of the filters, depending upon the filter selected. However, when the ISB operation is selected, diode logic steers only USB informaiton to Q6, while LSB information is steered to Q5 (see paragraph 3.2).

Output amplifier Q5 is essentially identical to Q6, except that it is used only when the ISB operation is selected, and then will only carry LSB information. LSB signals would then pass through J3 ISB output to ISB IF/Audio Assembly A18.

3.2 Filter Selection

Automatic filter selection control originates on Control Assembly A14 in response to operator entries via the front panel controls. Control line inputs D0-D3 carry BCD control signals to BCD to decimal decoder U1. It should be noted that some filters can be used for more than one demodulation mode. Table 3 lists the standard filters along with the control signals that select them.

Table 3. A4 Filter Selection

Filter Position Chosen	Mode	Control Line Inputs				Selected Output Pin No.	Output Amplifier Used
		U1-10 D0	U1-13 D1	U1-12 D2	U1-11 D3		
FL1	LSB	1	0	0	1	5	Q5
FL2	USB	0	0	0	0	3	Q6
FL1, FL2	ISB	1	0	0	0	14	Q5 and Q6
FL3	CW (300 Hz)	1	1	0	0	15	Q6
FL4	Optional	0	0	1	0	1	Q6
FL5	Optional	1	0	1	0	6	Q6
FL6	AM (6.0 kHz)	0	1	1	0	7	Q6
FL7	Optional	1	1	1	0	4	Q6
FL8	Wideband	0	0	0	1	9	Q6

U1 outputs, in turn, selectively drive switches AR1-AR3. These switches then select the appropriate filter by putting -15 Vdc on the associated filter control line, while holding all other lines at + 15 Vdc.

As an example, consider the selection of FL3. U1 filter select control lines would be D0 = 1, D1 = 1, D2 = 0, and D3 = 0. This would cause only U1, pin 15, to switch high (+ 5 Vdc); all other outputs would remain low. This 5 volt level causes switch AR1-A, pin 13, (-) input to exceed the 2 volt level at AR1-A, pin 12 (+), which forces the output, pin 14, to swing to -15 Vdc. Note that at this time, all other switch outputs would be at + 15 Vdc.

The -15 Vdc potential at AR1-A, pin 14, now forward biases CR12 and CR15, while reverse biasing CR13 and CR14. Any signal present at amplifier U3 output would now be allowed to only pass through FL3 to buffer amplifier Q6. Diodes associated with all other filters would prevent any signal from passing through these filters.

If some other filter is selected, U1, pin 14, is pulled to + 15 Vdc. This level reverse biases CR12 and CR15 (preventing any signal from passing through FL3), while forward biasing CR13 and CR14 (which would short out any signal that did appear there).

3.2.1 LSB Operation

Filter selection for LSB operation is the same as all other modes except that the output of FL1 is steered to Q5 instead of Q6.

3.2.2 ISB Operation

During ISB operation, U1, pin 14, is selected, allowing AR2-A and AR3-A to switch to -15 Vdc via OR Gates P/O U2. Control lines for FL1 and FL2 are then -15 Vdc, enabling FL1 and FL2. This places both USB and LSB filters in the circuit. The control line to R59 and R60 goes to + 15 Vdc, which reverse biases CR5 and CR7, effectively steering FL1 (LSB) signals to Q5 (ISB output) and FL2 (USB) signals to Q6. Also, Q4 is selected via AR1-D which activates Q5 by applying + 15 Vdc on Q5's drain.

4. MAINTENANCE

The following adjustment should not be performed as a routine maintenance procedure. It should be performed under the following two conditions:

- A failure indicating a definite problem
- Installation of new or different sideband filters. If the new filters have a loss which is different than the loss of the filters supplied with the Receiver, then R10 should be readjusted according to paragraph 4.1.

All tests are performed with all assembly connections in normal contact unless otherwise specified.

4.1 Input/Output Amplifier Test/Adjustment

a. Verify that the proper filters are installed in the A4 Assembly.

b. Set the front panel controls as follows:

Frequency: 15.000000 MHz

Mode: USB

AGC: OFF

RF Gain: Fully clockwise (cw)

c. Connect equipment as shown in figure 1.

590A-030A

Figure 1. A4 I/O Amplifiers Test Setup

d. Apply a 15.001 MHz, -50 dBm, signal to J1 Antenna input. Monitoring A4J4, adjust R10 for a -25 dBm signal level.

e. Monitor J2 (unfiltered IF output) with a spectrum analyzer. Signal level should be approximately -54 dBm.

f. Disconnect test equipment and reconnect A4 to Receiver.

4.2 Filter Selection Test

a. Selection of filters via the front panel consists of verifying that only the proper filter control line goes to -15 Vdc when the desired filter is selected. All other lines must stay at + 15 Vdc (except in the case of ISB mode, where both control lines FL1 and FL2 go to -15 Vdc).

b. Initiate BITE test. The receiver must pass 04 testing.

5. PARTS LIST

Table 4 is a comprehensive parts list of all replaceable components in IF Filter Assembly A4. When ordering parts from the factory, include a full description of the part. Use figure 2, the IF Filter Assembly component locaiton diagram to identify parts.

6. SCHEMATIC DIAGRAMS

Figure 3 is the IF Filter Assembly schematic diagram.

Table 4. IF Filter Assembly A4 Parts List (PL 10073-5500-06)

Ref. Desig.	Part Number	Description
AR1	I30-0003-000	IC 324 OP AMP PLASTIC
AR2	I30-0003-000	IC 324 OP AMP PLASTIC
AR3	I30-0003-000	IC 324 OP AMP PLASTIC
C6	M39014/01-1535	CAP .01UF
C9	M39014/02-1310	CAP .1 UF
C10	M39014/01-1535	CAP .01UF
C11	M39014/01-1535	CAP .01UF
C12	M39014/02-1320	CAP, CER, ,47UF,
C15	M39014/02-1320	CAP, CER, ,47UF,
C16	M39014/01-1535	CAP .01UF
C17	M39014/01-1535	CAP .01UF
C20	M39014/02-1320	CAP, CER, ,47UF,
C21	M39014/02-1298	CAP 01UF
C22	M39014/02-1298	CAP 01UF
C25	M39014/02-1320	CAP, CER, ,47UF,
C26	M39014/01-1535	CAP .01UF
C27	M39014/01-1535	CAP .01UF
C30	M39014/02-1320	CAP, CER, ,47UF,
C31	M39014/01-1535	CAP .01UF
C32	M39014/02-1298	CAP 01UF
C35	M39014/02-1320	CAP, CER, ,47UF,
C36	M39014/01-1535	CAP .01UF

Table 4. IF Filter Assembly A4 Parts List (PL 10073-5500-06) (Cont.)

Ref. Desig.	Part Number	Description
C37	M39014/01-1535	CAP .01UF
C40	M39014/02-1320	CAP, CER, ,47UF,
C41	M39014/01-1535	CAP .01UF
C42	M39014/01-1535	CAP .01UF
C45	M39014/02-1320	CAP, CER, ,47UF,
C46	CK05BX102K	CAP 1000PF 10% 200V CER
C47	M39014/01-1535	CAP .01UF
C48	M39014/01-1535	CAP .01UF
C49	M39014/01-1535	CAP .01UF
C50	M39014/01-1535	CAP .01UF
C51	M39014/02-1310	CAP .1 UF
C52	M39014/02-1310	CAP .1 UF
C53	M39014/02-1310	CAP .1 UF
C54	M39014/02-1310	CAP .1 UF
C55	C26-0016-330	CAP,TANT,33UF,16V
C56	M39014/02-1320	CAP, CER, ,47UF,
C57	M39014/02-1320	CAP, CER, ,47UF,
C58	M39014/02-1310	CAP .1 UF
C60	M39014/02-1320	CAP, CER, ,47UF,
C61	M39014/02-1320	CAP, CER, ,47UF,
C62	C18-0125-470	CAPACITOR
C63	C18-0125-470	CAPACITOR
C66	M39014/02-1320	CAP, CER, ,47UF,
C67	M39014/02-1320	CAP, CER, ,47UF,
C68	M39014/02-1320	CAP, CER, ,47UF,
C69	M39014/02-1320	CAP, CER, ,47UF,
C70	M39014/02-1320	CAP, CER, ,47UF,
C71	M39014/02-1320	CAP, CER, ,47UF,
C72	M39014/02-1320	CAP, CER, ,47UF,
CR1	1N4454	DIODE, SS SILICON
CR2	1N4454	DIODE, SS SILICON
CR3	1N4454	DIODE, SS SILICON
CR4	1N4454	DIODE, SS SILICON
CR5	1N4454	DIODE, SS SILICON
CR6	1N4454	DIODE, SS SILICON
CR7	1N4454	DIODE, SS SILICON
CR8	1N4454	DIODE, SS SILICON
CR9	1N4454	DIODE, SS SILICON
CR10	1N4454	DIODE, SS SILICON
CR11	1N4454	DIODE, SS SILICON
CR12	1N4454	DIODE, SS SILICON
CR13	1N4454	DIODE, SS SILICON
CR14	1N4454	DIODE, SS SILICON
CR15	1N4454	DIODE, SS SILICON
CR16	1N4454	DIODE, SS SILICON
CR17	1N4454	DIODE, SS SILICON
CR18	1N4454	DIODE, SS SILICON
CR19	1N4454	DIODE, SS SILICON
CR20	1N4454	DIODE, SS SILICON

Table 4. IF Filter Assembly A4 Parts List (PL 10073-5500-06) (Cont.)

Ref. Desig.	Part Number	Description
CR21	1N4454	DIODE, SS SILICON
CR22	1N4454	DIODE, SS SILICON
CR23	1N4454	DIODE, SS SILICON
CR24	1N4454	DIODE, SS SILICON
CR25	1N4454	DIODE, SS SILICON
CR26	1N4454	DIODE, SS SILICON
CR27	1N4454	DIODE, SS SILICON
CR28	1N4454	DIODE, SS SILICON
CR29	1N4454	DIODE, SS SILICON
CR30	1N4454	DIODE, SS SILICON
CR31	1N4454	DIODE, SS SILICON
CR32	1N4454	DIODE, SS SILICON
CR33	1N4454	DIODE, SS SILICON
CR34	1N4454	DIODE, SS SILICON
CR35	1N4454	DIODE, SS SILICON
CR39	1N4454	DIODE, SS SILICON
FL1	10073-7316	FILTER, USB
FL2	10073-7317	FILTER, LSB
FL3	10073-7318	FILTER, CW, 300 HZ
FL6	10073-7319	FILER, AM, 6KHZ
FL8	G25-0003-001	CERMAIC FILTER,30KHZ
J1	J-0031	CONNECTOR, COAX, SNAP-ON
J2	J-0031	CONNECTOR, COAX, SNAP-ON
J3	J-0031	CONNECTOR, COAX, SNAP-ON
J4	J-0031	CONNECTOR, COAX, SNAP-ON
J5	J46-0032-010	HEADER, 10 PIN DISCRETE
L4	MS75085-13	COIL, RF 330 UH 10%
L5	MS75085-13	COIL, RF 330 UH 10%
L6	10073-7033	INDUCTOR 10MH
L7	10073-7033	INDUCTOR 10MH
L8	MS75085-13	COIL, RF 330 UH 10%
L9	MS75085-13	COIL, RF 330 UH 10%
Q4	2N2222A	XSTR, SS/GP, NPN
Q5	Q35-0001-001	XSTR, JFET, J310
Q6	Q35-0001-001	XSTR, JFET, J310
R5	R65-0003-333	RES,33K 5% 1/4W CAR FILM
R6	R65-0003-333	RES,33K 5% 1/4W CAR FILM
R7	R65-0003-333	RES,33K 5% 1/4W CAR FILM
R8	R65-0003-333	RES,33K 5% 1/4W CAR FILM
R10	R-2205	RES,VAR,PCB 500 .5 20%
R17	R65-0003-102	RES,1.0K 5% 1/4W CAR FILM
R21	R65-0003-512	RES,5.1K 5% 1/4W CAR FILM
R22	R65-0003-512	RES,5.1K 5% 1/4W CAR FILM
R23	RN55D5111F	RES,5110 1% 1/8W MET FLM
R24	R65-0003-512	RES,5.1K 5% 1/4W CAR FILM
R25	R65-0003-512	RES,5.1K 5% 1/4W CAR FILM
R26	RN55D5111F	RES,5110 1% 1/8W MET FLM
R27	R65-0003-512	RES,5.1K 5% 1/4W CAR FILM
R28	R65-0003-512	RES,5.1K 5% 1/4W CAR FILM

Table 4. IF Filter Assembly A4 Parts List (PL 10073-5500-06) (Cont.)

Ref. Desig.	Part Number	Description
R29	RN55D5111F	RES,5110 1% 1/8W MET FLM
R30	R65-0003-512	RES,5.1K 5% 1/4W CAR FILM
R31	R65-0003-512	RES,5.1K 5% 1/4W CAR FILM
R32	RN55D5111F	RES,5110 1% 1/8W MET FLM
R33	R65-0003-512	RES,5.1K 5% 1/4W CAR FILM
R34	R65-0003-512	RES,5.1K 5% 1/4W CAR FILM
R35	RN55D5111F	RES,5110 1% 1/8W MET FLM
R36	R65-0003-512	RES,5.1K 5% 1/4W CAR FILM
R37	R65-0003-512	RES,5.1K 5% 1/4W CAR FILM
R38	RN55D5111F	RES,5110 1% 1/8W MET FLM
R39	R65-0003-512	RES,5.1K 5% 1/4W CAR FILM
R40	R65-0003-512	RES,5.1K 5% 1/4W CAR FILM
R41	RN55D5111F	RES,5110 1% 1/8W MET FLM
R42	R65-0003-512	RES,5.1K 5% 1/4W CAR FILM
R43	R65-0003-152	RES,1.5K 5% 1/4W CAR FILM
R44	RN55D5111F	RES,5110 1% 1/8W MET FLM
R45	R65-0003-822	RES,8.2K 5% 1/4W CAR FILM
R46	R65-0003-182	RES,1.8K 5% 1/4W CAR FILM
R48	R65-0003-101	RES,100 5% 1/4W CAR FILM
R49	R65-0003-101	RES,100 5% 1/4W CAR FILM
R50	R65-0003-101	RES,100 5% 1/4W CAR FILM
R51	R65-0003-101	RES,100 5% 1/4W CAR FILM
R52	R65-0003-101	RES,100 5% 1/4W CAR FILM
R53	R65-0003-101	RES,100 5% 1/4W CAR FILM
R54	R65-0003-101	RES,100 5% 1/4W CAR FILM
R55	R65-0003-101	RES,100 5% 1/4W CAR FILM
R56	R65-0003-101	RES,100 5% 1/4W CAR FILM
R57	R65-0003-153	RES,15K 5% 1/4W CAR FILM
R58	R65-0003-102	RES,1.0K 5% 1/4W CAR FILM
R59	R65-0003-333	RES,33K 5% 1/4W CAR FILM
R60	R65-0003-333	RES,33K 5% 1/4W CAR FILM
R61	R65-0003-102	RES,1.0K 5% 1/4W CAR FILM
R62	R65-0003-153	RES,15K 5% 1/4W CAR FILM
R63	R65-0003-103	RES,10K 5% 1/4W CAR FILM
R64	R65-0003-101	RES,100 5% 1/4W CAR FILM
R65	R65-0003-104	RES,100K 5% 1/4W CAR FILM
R66	R65-0003-101	RES,100 5% 1/4W CAR FILM
R67	R65-0003-101	RES,100 5% 1/4W CAR FILM
R68	R65-0003-104	RES,100K 5% 1/4W CAR FILM
R69	R65-0003-101	RES,100 5% 1/4W CAR FILM
R70	R65-0003-272	RES,2.7K 5% 1/4W CAR FILM
R71	R65-0003-510	RES,51 5% 1/4W CAR FILM
R72	R65-0003-510	RES,51 5% 1/4W CAR FILM
R73	R65-0003-511	RES,510 5% 1/4W CAR FILM
R74	R65-0003-511	RES,510 5% 1/4W CAR FILM
R75	R65-0003-102	RES,1.0K 5% 1/4W CAR FILM
R76	R65-0003-681	RES,680 5% 1/4W CAR FILM
R77	R65-0003-510	RES,51 5% 1/4W CAR FILM
R78	R65-0003-101	RES,100 5% 1/4W CAR FILM

Table 4. IF Filter Assembly A4 Parts List (PL 10073-5500-06) (Cont.)

Ref. Desig.	Part Number	Description
R79	R65-0003-101	RES,100 5% 1/4W CAR FILM
R80	R65-0003-101	RES,100 5% 1/4W CAR FILM
R81	R65-0003-101	RES,100 5% 1/4W CAR FILM
R82	R65-0003-101	RES,100 5% 1/4W CAR FILM
R83	R65-0003-101	RES,100 5% 1/4W CAR FILM
R84	R65-0003-101	RES,100 5% 1/4W CAR FILM
TP1	J-0071	TIP JACK, BROWN
TP2	J-0066	TIP JACK, RED
TP3	J-0069	TIP JACK, ORANGE
TP4	J-0070	TIP JACK, YELLOW
TP5	J-0068	TIP JACK, GREEN
TP6	J-0072	TIP JACK, BLUE
TP7	J-0073	TIP JACK, VIOLET
TP8	J-0074	TIP JACK, GRAY
U1	I01-0000-200	IC 4028B PLASTIC CMOS
U2	I01-0000-023	IC 4071B PLASTIC CMOS
U3	I50-0002-000	IC 733 VIDEO AMP PLASTIC
VR1	1N5231B	DIODE 5.1V 5% 0.5W ZENER

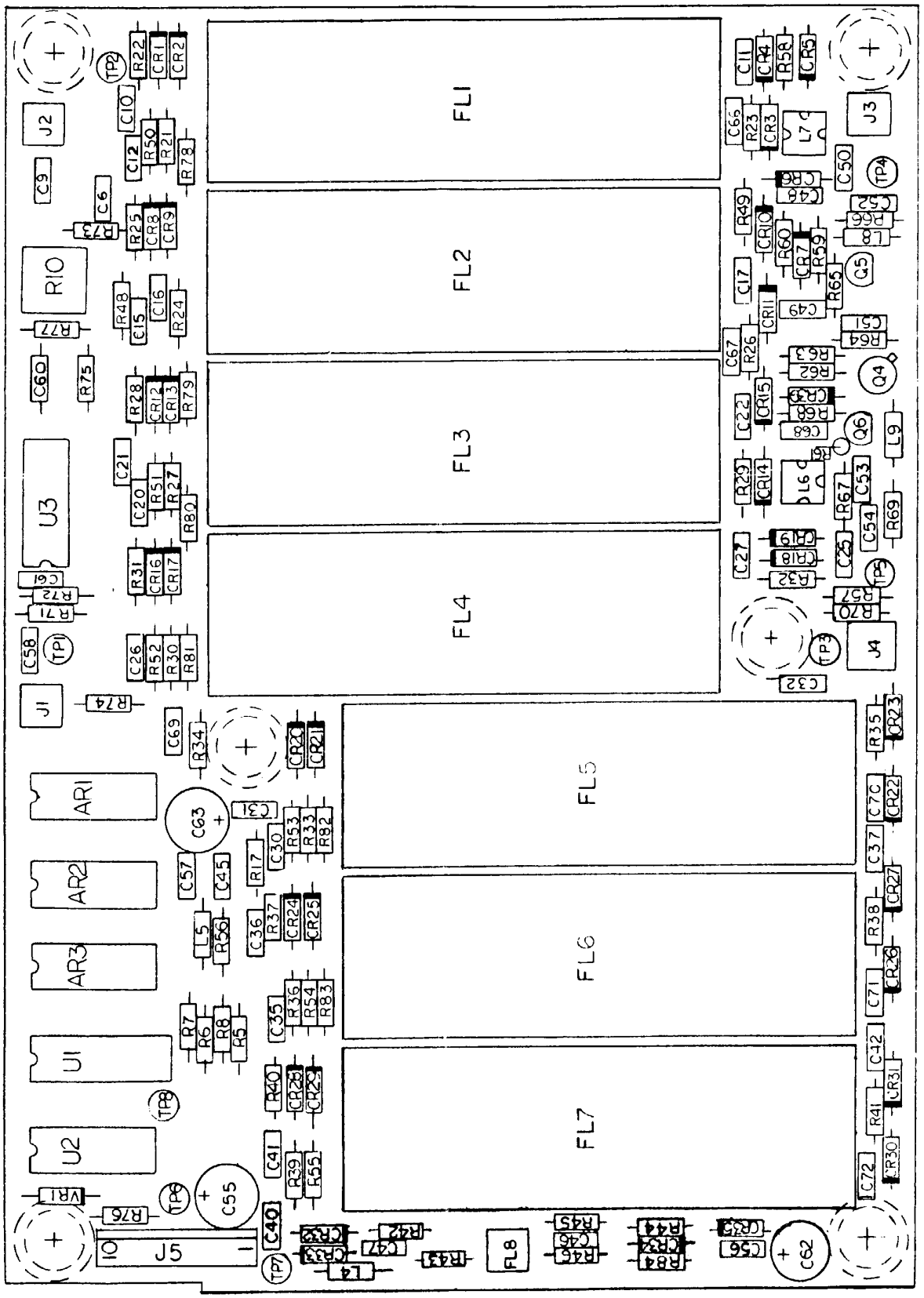


Figure 2. IF Filter Assembly A4 Component Location Diagram (10073-5500, Rev. F)

NOTE: UNLESS OTHERWISE SPECIFIED:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR A COMPLETE DESIGNATION, PREFIX WITH UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.
2. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, ±5%.
3. ALL CAPACITOR VALUES ARE IN MICROFARADS.
4. ALL UNLABLED DIODES ARE D10-4454-000.
5. VENDOR PART NO. CALLOUTS ARE FOR REFERENCE ONLY. COMPONENTS ARE SUPPLIED PER PART NO. IN PARTS LIST.
7. SIGNAL LEVELS SPECIFIED CORRESPOND TO A -20 dBm, 455KHZ INJECTION AT J1.
8. FILTERS FL1 THROUGH FL7 ARE OPTIONAL AND MAY VARY IN USE AND TYPE.

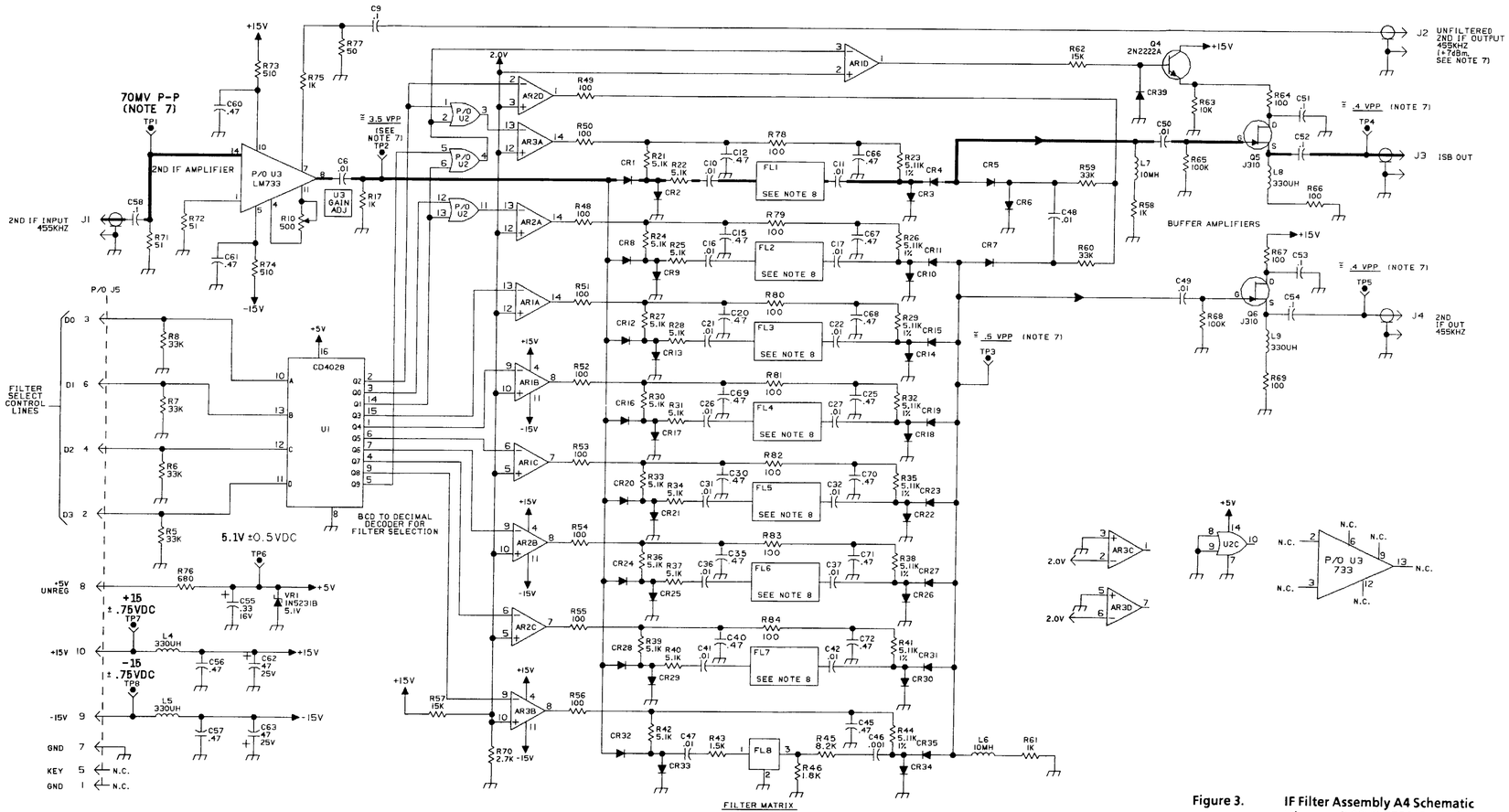


Figure 3. IF Filter Assembly A4 Schematic Diagram (10073-5501, Rev. H)

A5
IF/AUDIO PWB ASSEMBLY

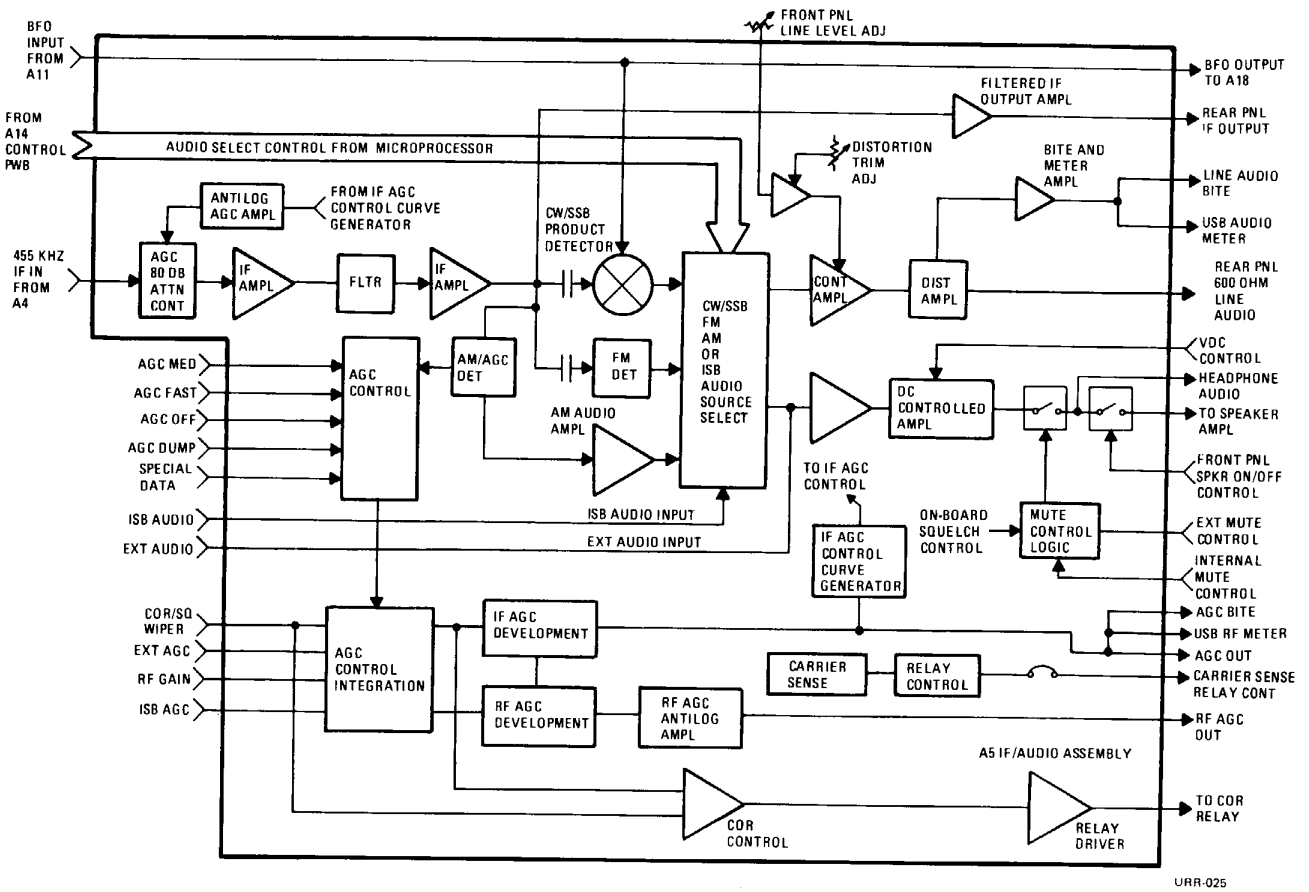


TABLE OF CONTENTS

Paragraph		Page
1.	Introduction	1
2.	General Description	1
3.	Circuit Descriptions.	1
3.1	IF Amplification and Control	1
3.2	AM/SSB/CW, and FM Detectors	2
3.3	Audio Source Select	2
3.4	Line Audio Outputs	2
3.5	Speaker and Headphone Audio	5
3.6	Squelch, Mute, and Speaker Control	5
3.7	AGC Development	5
3.7.1	Comparator With Hysteresis	5
3.7.2	One Shot Timer Control	6
3.7.3	AGC Charge Pump	6
3.7.4	AGC Off/Dump Control	6
3.7.5	AGC Source Selection	7
3.7.6	IF/RF AGC Integration	7
3.7.7	Combined and RF AGC Output	7
4.	Maintenance	7
4.1	R44 Adjustment, IF Level Set	7
4.2	R78 Adjustment, IF AGC Gain Set	7
4.3	R79 Adjustment, RF Level Set	8
4.4	R74 Adjustment, AGC 1 dB Compression Point	8
4.5	R180 Adjustment, Line Amplifier Distortion Trim Adjustment	8
4.6	L7 Adjustment, FM Demodulator Fidelity Adjustment	8
4.7	R194 Adjust, Dead Zone	9
5.	Parts List, Component Location, and Schematic Diagrams	9

LIST OF FIGURES

Figure		Page
1	IF/Audio Assembly Functional Block Diagram	3
2	Dead Zone Adjustment Waveform	9
3	IF/Audio Assembly A5 Component Locations (10215-5410)	21
4	IF/Audio Assembly A5 Schematic Diagram (10215-5411)	23

LIST OF TABLES

Table		Page
1	Audio Select Truth Table	2
2	AGC Charge Pump Control Truth Table	6
3	IF/Audio Assembly A5 Parts List (10215-5410-02)	10

A5 IF/AUDIO ASSEMBLY

1. INTRODUCTION

This section provides detailed assembly level information for the A5 IF/Audio Assembly. The schematic diagram, parts list, and component location diagram are organized together at the back of this section for ready reference. A general description, and detailed circuit descriptions, test/setup adjustments, and maintenance information are also included in this section. For unit level interconnect information, refer to the Main Chassis Interconnect Tab Section. The Main Chassis Tab Section also contains a diagram that locates the A5 Assembly in the Receiver.

2. GENERAL DESCRIPTION

The cover diagram identifies all major functions resident on the A5 Assembly. Figure 4-1 in the Technical Description Tab Section shows these same functions in a unit-level context. Significant signal and control inputs and/or outputs are also shown on this diagram. This assembly amplifies the 455 kHz IF input from the A4 Filter PWB, detects the SSB, CW, FM, or AM audio components, and executes the audio selection switching commands from the A14 Control Assembly. Both the RF and the IF AGC control voltages are developed on this assembly. The IF hang AGC system has an approximate 90 dB dynamic control range on this assembly; the RF AGC output works with the IF AGC in a two control loop system that is integrated and shaped to optimize receiver performance.

Slow, medium, fast, and special data AGC decay characteristic control logic circuits are also incorporated on this assembly. This logic is integrated to work with ISB audio/AGC, external audio, mute, COR, and optional squelch control circuits as subsequently described.

3. CIRCUIT DESCRIPTIONS

The cover diagram is largely self-explanatory, especially when used in its unit level context as shown in figure 4-1 in the Unit Level Technical Description Tab Section. Refer to these diagrams briefly before reading this section. The circuit descriptions in this section will refer primarily to the detailed functional diagram for this assembly, shown in figure 1. This detailed functional diagram, together with the related descriptions, should permit the user to use the schematic information at the end of this section to maintain the equipment.

3.1 IF Amplification and Control

The IF input to the A5 Assembly is from the A4 IF Filter Assembly. The A5 Assembly incorporates sufficient gain to raise the IF output level by 75 dB. PIN diode attenuation control in the IF amplifier circuit provides a dynamic control range of approximately 90 dB through the IF Amplifier circuit. As will be subsequently discussed, two AGC voltages are developed on this assembly; IF and RF. The control curves of these two AGC voltages are combined so that the primary control range of the IF AGC system is operative first, and with the RF AGC system becoming dominant above -50 dBm.

IF Amplifiers Q8, Q9, and Q16 provide approximately 60 dB gain. FL1 is a ceramic 455 kHz IF Filter that limits the bandwidth of the IF amplifier. The FL1 output is amplified approximately 20 dB by Q3 and Q4. Considering the 5 dB insertion loss of FL1, the overall gain of the IF system is approximately 75 dB. Q5 is a buffer amplifier for the rear panel IF outlet. A rear-panel BNC connector provides a convenient test output and can be used for system applications as necessary.

3.2 AM, SSB/CW, and FM Detectors

Q6 and Q7 detect the Q4 IF Amplifier output. The output of this circuit is a voltage that tracks the IF envelope power and can thus be used as an AM detector and as a source voltage for AGC development. The output level to the AGC system and to U12B, the AM Audio buffer amplifier, is approximately 1 volt (peak). The voltage divider at the U12B output attenuates the signal by about 2.5 dB so that the level at TP3 will be 350 to 400 millivolts rms (assuming operation in the AGC range and that the AM signal is modulated 50%).

The IF output is used in a product detector (U11) circuit (heterodyned with the BFO input signal) to detect the single sideband or CW output signal. R104 and R173 at the U11 input introduce 26 dB attenuation to the IF signal to produce the same audio output in these two modes as in all other modes. The output level at TP3 or TP4 should be 350 to 400 millivolts rms assuming operation in the AGC range.

FM Detector U18 is driven in parallel with U11, the SSB/CW Detector. R174 and R112 attenuate the FM IF signal input 13 dB. The detected output at TP3 or TP4 will be 350 to 400 millivolts, assuming modulation sufficient to produce 4.5 kHz deviation. This detector also incorporates a quadrature trim inductor, L7. L7 is adjusted for minimum distortion in the receiver audio output in FM mode of operation.

3.3 Audio Source Select

U19 is controlled by audio select logic lines A, B, and C (microprocessor control from the Control Assembly). The simplified drawing of U19 in figure 1 is an accurate functional representation of this device. Table 1 is a truth table that shows the A, B, and C control line conditions for each of the audio select options.

Table 1. Audio Select Truth Table

Mode	Line C	Line B	Line A
AM	0	0	0
SSB or CW	0	0	1
FM	0	1	0
ISB-LSB	1	0	1

NOTE

An internal or external MUTE signal activates a high impedance state that opens all audio lines.

3.4 Line Audio Outputs

Line audio outputs are independent of the front-panel volume control. Line audio output levels are adjusted with the front panel screwdriver control potentiometers. In non-ISB operation there is only one output. The circuitry shown here is controlled by the USB level adjust potentiometer (the one on the left). The line level for LSB is controlled on the A18 Assembly. Adjusting this potentiometer produces a wiper voltage of from 0 Vdc to -15 Vdc (-15 Vdc correlates with maximum line level). U23 is a dc controlled amplifier that can be distortion compensated by R180. This output level is normally set to produce + 10 dBm in 600 ohms, but can be changed from this level to accommodate other system application requirements. Full power output from the line amplifier is + 15 dBm into an unbalanced 600-ohm load. The meter on the front panel is calibrated to measure the line audio in dBm, assuming a 600-ohm load. Full scale on the meter is + 15 dBm.

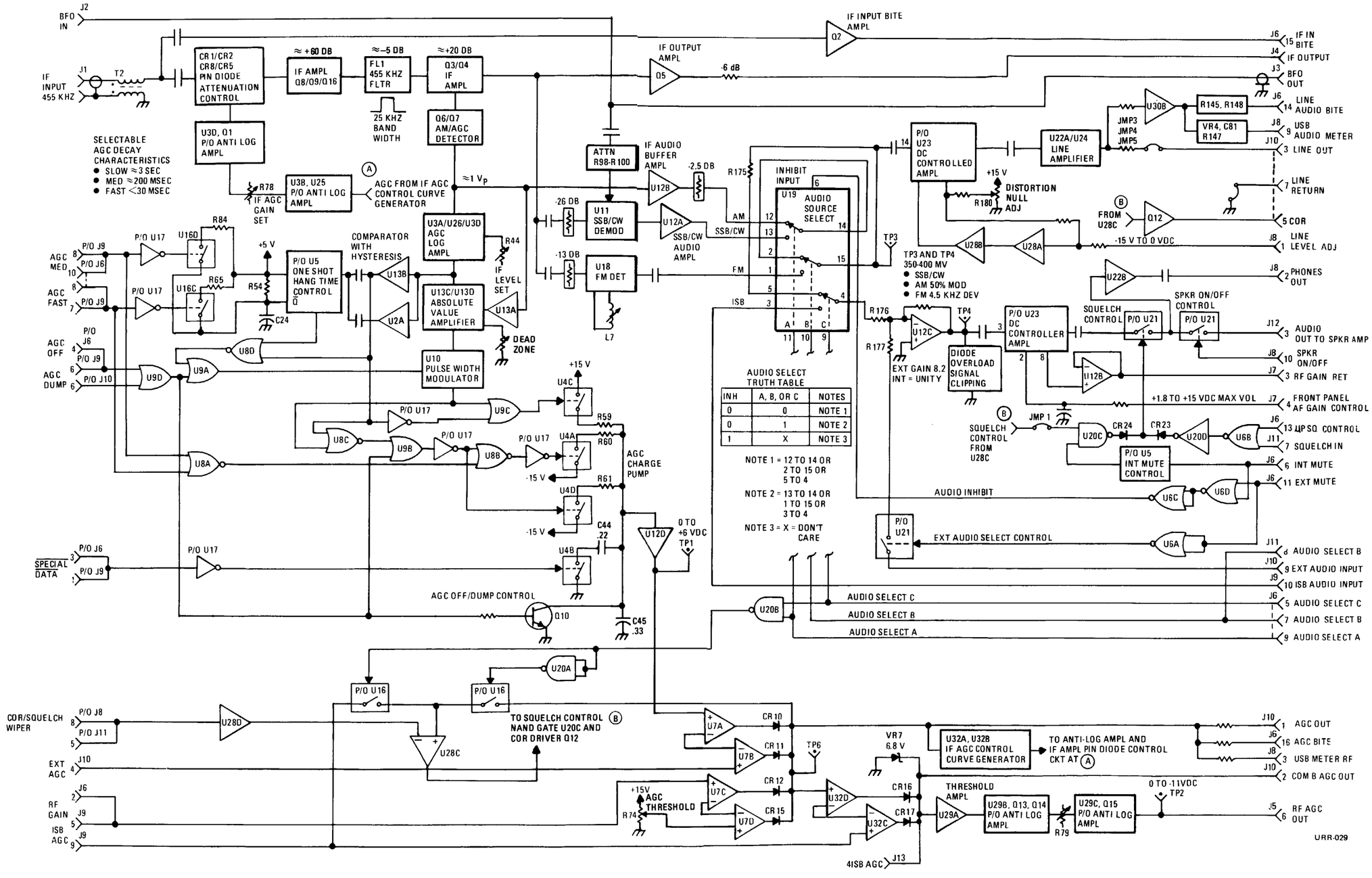


Figure 1. IF/Audio Assembly Functional Block Diagram

3.5 Speaker and Headphone Audio

The operational amplifier at the U19 pin 4 output is set for unity gain ratio of R178/(R175 + R176) in AM, SSB/CW, and FM modes. The ISB (LSB)and external audio inputs, however, are amplified 8.19 times as the ratio of R178/R176. These differences work to produce constant outputs for given inputs. Diode clipping (CR25 through CR30) limits audio peaks during periods when unusually strong signals are present. The front panel AF Gain Control establishes the desired output level at either the speaker (if installed) or the headset audio outputs. This is also a dc controlled amplifier with the wiper voltage varying from + 1.8 to + 15 Vdc. + 15 Vdc correlates with maximum volume. The speaker audio outputs are squelch and mute controlled; the line audio output is not.

3.6 Squelch, Mute, and Carrier Operated Relay Control

Squelch and mute circuits can be exercised by signals from the Control Assembly. When active, these signals will effectively open the audio path to the headphones and disable analog switch U19. This feature is used primarily to prevent unwanted noise from going to the audio output during BITE operation.

3.6.1 Carrier Operated Relay Control (COR)

The Carrier Operated Relay (COR) is controlled by the front panel COR control through U28D, U28C, and Q12. U28D feeds the offset and buffered voltage of the front panel COR control to comparator U28C. U28C compares the voltage from U28D against either the normal IF AGC or the ISB AGC, as selected by the front panel switches and U20A, U20B, U16A, and U16B. Positive feedback is applied to U28C via R76 to give the comparator hysteresis so undesired circuit switching does not occur around the COR set point. The output from U28C goes to the COR relay driver Q12, with CR19 and CR22 providing protection to Q12.

3.7 AGC Development

The AGC control loop detects any change in the IF input level and reacts to amplify or attenuate the signal in order to maintain the desired output level. The attack time for the AGC is built into the system but the decay time is front panel selectable. Slow or medium AGC characteristics are desirable for CW or voice operation to prevent pumping of the AGC system and possible loss of continuity in the intelligence during pauses in modulation or transmission. Other forms of communication, such as data transmission, require fast AGC decay characteristics.

With the receiver operating within the AGC dynamic range, and with a constant RF input level, the detected IF envelope power will produce approximately 1 volt (peak) at the input to log amplifier U3A, U26, U3D (the output is a negative logarithmic function of the input). The output of this circuit to comparator U13B and to the absolute value amplifier will be approximately 0 volts with a 1 volt input. The output level of the absolute value amplifier (U13C, U13D) to the pulse width modulator U10 is level shifted and temperature compensated to be approximately 1.4 volts. For larger signal excursions (in excess of + 14 dB), U13A bypasses the log amplifier to directly drive the absolute value amplifier to maximum. These devices, and the associated logic circuits control the AGC level through a charge pump circuit. Assuming no input level change, the AGC value at TP6 will remain constant.

3.7.1 Comparator With Hysteresis

U13B functions as a comparator with hysteresis. This means that the AGC level being compared must change by a predetermined amount before the output state switching conditions of U13B are met. If the input signal conditions increase, the AGC system reacts immediately through the Absolute Value Amplifier. If the input signal conditions decrease beyond the hysteresis level of U13B, the output of this device goes low and the One Shot AGC hang timer U5 is activated. The output of U13B is also an input to the AGC charge pump control

logic circuit. When the U13B output is positive the charge pump will charge. When the output is negative the charge pump will discharge.

U2A functions as a comparator, similarly to U13B but with a different switching threshold. While U13B monitors the input for an increase or decrease from the equilibrium level, U2A monitors the input only for a decrease from this level by more than 6 dB. This comparator is required so that two or more rapid consecutive drops in the RF input signal will be detected. The outputs of U13B and U2A are differentiated by C104 and C105 and summed together to provide a trigger pulse for U5.

3.7.2 One Shot Timer Control

When U5 is activated by U13B or U2A, signaling a reduction in AGC requirement, the timer starts to run. The period of this timer can be set at 3 seconds (slow AGC), 170 milliseconds (medium AGC), or 13 milliseconds (fast AGC). The period is set by the C24 time constant, which is in turn controlled by the resistance placed in series with it and its + 5 Vdc charging source. Slow AGC is a default condition when neither the medium or fast AGC conditions are commanded. In this condition both the U16C and the U16D analog switch elements are open and the C24 charge path is through R54. When medium AGC is commanded, R84 is placed in parallel with R54 to reduce the time constant. In fast AGC R65 is placed in parallel with R54 to reduce the time constant to about 15 milliseconds. This hang time inhibits immediate AGC discharge when the signal starts to fall.

3.7.3 AGC Charge Pump

Quad Monolithic SPST CMOS Analog Switches U4A, U4B, U4C, and U4D operate to control charge pump operation. Pulse Width Modulator U10 produces an output pulse width that varies at a rate determined by the voltage at its input (pin 4). When it is calling for increased AGC, it activates U4C to place R59 in the C44 and C45 charge path to + 15 Vdc. When U4D and or U4A are activated, C44 and C45 are discharged through R61 and R60 to reduce AGC. Table 2 is a truth table that shows the state of these switches for all operating conditions. Notice that U4B is active in all modes except the data mode. In the data mode C44 is removed from the circuit to achieve the desired AGC time characteristics. U5 works with the AGC OFF and DUMP inputs to control U10 and the decay rate.

Table 2. AGC Charge Pump Control Truth Table

Mode	U4A	U4B	U4C	U4D
Slow	0	1	X	X
Med	X	1	X	X
Fast	X	1	X	X
Data	X	0	X	X

0 = Disabled (off)
1 = Enabled (on)
X = Switched in and out by Pulse Width Modulator

3.7.4 AGC Off/Dump Control

Q10 can be activated to provide a low impedance AGC Dump path to ground. When AGC OFF or AGC DUMP is commanded, Q10 is held on to prevent any AGC voltage buildup on C44 and C45 if it is selected. With Q10 off, the AGC voltage on C44 and C45 will be controlled by the charge pump and the AGC system. In normal operation, the AGC voltage at TP1 will typically vary between 0 and + 6 Vdc.

3.7.5 AGC Source Selection

The TP1 AGC voltage (from the charge pump) is only one source of level control; there are three other sources as shown of figure 1: EXT AGC, RF GAIN, and AGC THRESHOLD (R74). Source selection is made by an ideal diode OR circuit. U7A, U7B, U7C, and U7D work with diodes CR10, CR11, CR12, and CR15 to form this AGC source selection circuit. In this circuit, the AGC source with the highest voltage will dominate and shut the other sources off. In normal operation the source is the internal AGC system, and as a consequence the TP1 AGC level and the TP6 level should agree.

3.7.6 IF/RF AGC Control Shaping

The TP6 AGC level is fed to IF AGC Control Curve Shaper, U32A and U32B, and to the RF AGC System. The output of the IF AGC Control Curve Generator is fed to antilog amplifier U25, U3B, U3C, and Q1. This voltage can exercise approximately a 90 dB dynamic control range on the IF amplifier on this assembly. The control curve generator sets a fixed break point so that the IF AGC exercises primary control from the threshold of sensitivity to the approximately -50 dBm of RF input. At this point the control curves for RF AGC (via U29A) and IF AGC are joined to ensure a linear slope. The RF AGC becomes dominant above this point.

3.7.7 Combined and RF AGC Output

U32C and U32D also work in an ideal diode circuit to select either the internal or the ISB AGC as the drive source for the RF and the combined AGC outputs. U29A acts as a threshold amplifier configured to drive the RF AGC Control Curve shapes U29B and U29C, when above the crossover threshold. R79 can be adjusted for a 10 millivolt indication on the front panel RF meter with a calibrated 10 millivolt RF input at the antenna. The TP2 output level will vary between 0 and -11 Vdc in normal operation.

4. MAINTENANCE

There are no routine maintenance adjustments for this assembly. All boards are made for direct replacement without adjustment. If components are replaced or if the operation of the assembly is in question, proceed with the following setup adjustments in the order shown.

4.1 R44 Adjustment, IF Level Set

a. Connect an RF Signal Generator to the receiver RF Input.

b. Make sure that the AGC is operating in the FAST mode. Set mode to USB.

c. Set the Signal Generator output to 10 millivolts at 1 kHz above the receiver operating frequency.

d. Connect an RF Voltmeter to the receiver IF Output and adjust R44 on the A5 Assembly for -6 dBm (112 mV rms in 50 ohms) at this calibration setup point.

4.2 R78 Adjustment, IF AGC Gain Set

a. Tune the Receiver to 10.000 MHz, select the USB mode, and set the AGC to FAST.

b. Set the front panel meter to read the USB RF signal level.

c. Set the signal generator to output a 10.001 MHz, 10 microvolt signal.

d. Turn A5R74 fully counterclockwise.

e. Measure the Dc voltage at A5TP6.

f. Adjust A5R78 until 1.375 V ± 25 mV is measured at TP6.

g. Use the front panel meter zero adjust to set the meter to read 10 microvolts.

4.3 R79 Adjustment, RF Level Set

a. Set the signal generator output level to 10 millivolts.

b. Adjust A5R79 until 4.15 ± 50 mV is measured at A5TP6.

c. The front panel meter should read 10 mV (± a needle width).

d. Repeat the R78 and R79 adjustment procedures as required to minimize the effect of the interaction between the potentiometers.

4.4 R74 Adjustment, AGC 1 dB Compression Point

a. Set the signal generator output level to 1 microvolt.

b. Use the front panel or external meter to monitor the USB line audio.

c. Note the USB line audio level with the AGC on.

d. Turn the AGC off and turn the RF GAIN control fully clockwise.

e. Adjust A5R74 until the USB audio level is 1 dB greater than it was when the AGC was on.

f. Turn the AGC back on.

g. To check the AGC flatness, note the USB line audio level and increase the signal generator output level by 100 dB. The line level should increase by no more than 3 dB.

4.5 R180 Adjustment, Line Amplifier Distortion Trim Adjustment

a. With a signal generator connected as in paragraph 4.1, setup for single tone operation.

b. Verify line level adjustment + 10 dBm on the front panel meter.

c. Connect a distortion analyzer to the line audio output and adjust R180 for minimum distortion.

4.6 L7 Adjustment, FM Demodulator Fidelity Adjustment

a. Connect an FM Signal Generator to the receiver RF Input and adjust the output for 4.5 kHz deviation at the receiver operating frequency.

b. With the Receiver in FM mode, observe the audio output and adjust L7 for minimum distortion.

4.7 R194 Adjust, Dead Zone

Test Equipment required:

- RF Signal Generator Hewlett Packard HP8640 or equivalent
- Square wave source (1 to 5 V_{p-p}, 5 to 10 Hz output).
- Tektronix 465B oscilloscope or equivalent.

a. Connect the square wave source to the RF generator's external AM input using the DC mode if possible. Adjust the levels as required to produce modulation depth of 30 to 40 dB. Adjust the RF generator so that the peak output is -10 dBm ± 5 dB.

b. Tune the receiver to 10.000 MHz, select the USB mode, and set the AGC to FAST.

c. Set the signal generator to deliver a 10.001 MHz signal.

d. Monitor A5U3 pin 1 with the oscilloscope.

e. Adjust A5R194 so that the separation between the attack and decay waveforms is 60 mV ± 5 mV, see figure 2.

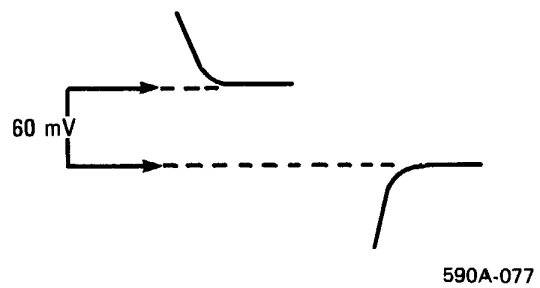


Figure 2. Dead Zone Adjustment Waveform

f. Disconnect the test equipment, return all cables to their original positions and replace all covers. Perform BITE testing from the front panel.

5. PARTS LIST, COMPONENT LOCATION, AND SCHEMATIC DIAGRAMS

The parts list, component location drawing and schematic diagram for the A5 Audio/IF Assembly are shown in table 3 and figures 3 and 4, respectively.

Table 3. IF/Audio Assembly A5 Parts List (10215-5410, Rev. N/-5410-02, Rev. D)

Ref. Desig.	Part Number	Description
C1	M39014/02-1310	CAP .1UF 10% 100V CER-R
C2	M39014/02-1310	CAP .1UF 10% 100V CER-R
C3	M39014/02-1310	CAP .1UF 10% 100V CER-R
C4	M39014/02-1310	CAP .1UF 10% 100V CER-R
C5	M39014/02-1310	CAP .1UF 10% 100V CER-R
C6	M39014/02-1310	CAP .1UF 10% 100V CER-R
C7	M39014/02-1310	CAP .1UF 10% 100V CER-R
C8	C26-0025-100	CAP 10UF 20% 25V TANT
C9	C26-0025-100	CAP 10UF 20% 25V TANT
C10	M39014/02-1310	CAP .1UF 10% 100V CER-R
C11	CK05BX101K	CAP 100PF 10% 200V CER
C12	M39014/02-1298	CAP .01UF 10% 200V CER-R
C13	M39014/02-1310	CAP .1UF 10% 100V CER-R
C14	M39014/02-1310	CAP .1UF 10% 100V CER-R
C15	M39014/02-1310	CAP .1UF 10% 100V CER-R
C16	M39014/02-1310	CAP .1UF 10% 100V CER-R
C17	M39014/02-1310	CAP .1UF 10% 100V CER-R
C18	M39014/02-1310	CAP .1UF 10% 100V CER-R
C19	M39014/02-1310	CAP .1UF 10% 100V CER-R
C20	M39014/02-1310	CAP .1UF 10% 100V CER-R
C21	CK05BX102K	CAP 1000PF 10% 200V CER
C22	C26-0050-109	CAP 1.0UF 20% 50V TANT
C23	CK05BX102K	CAP 1000PF 10% 200V CER
C24	C26-0025-339	CAP 3.3UF 20% 25V TANT
C25	CK05BX221K	CAP 220PF 10% 200V CER
C26	M39014/02-1310	CAP .1UF 10% 100V CER-R
C27	M39014/02-1298	CAP .01UF 10% 200V CER-R
C28	M39014/02-1298	CAP .01UF 10% 200V CER-R
C29	M39014/02-1298	CAP .01UF 10% 200V CER-R
C30	M39014/02-1298	CAP .01UF 10% 200V CER-R
C31	M39014/02-1298	CAP .01UF 10% 200V CER-R
C32	M39014/02-1298	CAP .01UF 10% 200V CER-R
C33	CK05BX221K	CAP 220PF 10% 200V CER
C34	M39014/02-1310	CAP .1UF 10% 100V CER-R
C35	M39014/02-1310	CAP .1UF 10% 100V CER-R
C36	M39014/02-1310	CAP .1UF 10% 100V CER-R
C37	M39014/02-1310	CAP .1UF 10% 100V CER-R
C38	C26-0050-109	CAP 1.0UF 20% 50V TANT
C39	C26-0050-109	CAP 1.0UF 20% 50V TANT
C40	C26-0050-109	CAP 1.0UF 20% 50V TANT
C41	C26-0050-109	CAP 1.0UF 20% 50V TANT
C42	C26-0050-109	CAP 1.0UF 20% 50V TANT
C43	CK06BX222K	CAP 2200PF 10% 200V CER
C44	C61-0001-004	CAP .22UF 5% 100V POLYE
C45	C61-0001-005	CAP .33UF 5% 100V POLYE
C46	CK05BX102K	CAP 1000PF 10% 200V CER
C47	CK05BX101K	CAP 100PF 10% 200V CER

Table 3. IF/Audio Assembly A5 Parts List (10215-5410, Rev. N/-5410-02, Rev. D) (Cont.)

Ref. Desig.	Part Number	Description
C48	M39014/02-1310	CAP .1UF 10% 100V CER-R
C49	CK06BX472K	CAP 4700PF 10% 200V CER
C50	CK06BX472K	CAP 4700PF 10% 200V CER
C51	CK05BX470K	CAP 47PF 10% 200V CER
C52	M39014/02-1320	CAP .47UF 10% 50V CER-R
C53	M39014/02-1310	CAP .1UF 10% 100V CER-R
C54	CK06BX472K	CAP 4700PF 10% 200V CER
C55	M39014/02-1310	CAP .1UF 10% 100V CER-R
C56	CK05BX680K	CAP 68PF 10% 200V CER
C57	C26-0025-339	CAP 3.3UF 20% 25V TANT
C58	CK06BX332K	CAP 3300PF 10% 200V CER
C59	M39014/02-1310	CAP .1UF 10% 100V CER-R
C60	M39014/02-1298	CAP .01UF 10% 200V CER-R
C61	M39014/02-1310	CAP .1UF 10% 100V CER-R
C62	M39014/02-1310	CAP .1UF 10% 100V CER-R
C63	C26-0025-339	CAP 3.3UF 20% 25V TANT
C64	C26-0025-339	CAP 3.3UF 20% 25V TANT
C65	M39014/02-1310	CAP .1UF 10% 100V CER-R
C66	C26-0025-100	CAP 10UF 20% 25V TANT
C67	C26-0025-339	CAP 3.3UF 20% 25V TANT
C68	M39014/02-1310	CAP .1UF 10% 100V CER-R
C69	C26-0025-339	CAP 3.3UF 20% 25V TANT
C70	M39014/02-1310	CAP .1UF 10% 100V CER-R
C71	C26-0025-339	CAP 3.3UF 20% 25V TANT
C72	C26-0025-339	CAP 3.3UF 20% 25V TANT
C73	M39014/02-1298	CAP .01UF 10% 200V CER-R
C74	M39014/02-1310	CAP .1UF 10% 100V CER-R
C75	C26-0025-100	CAP 10UF 20% 25V TANT
C76	C26-0025-100	CAP 10UF 20% 25V TANT
C77	CK05BX471K	CAP 470PF 10% 200V CER
C78	CK05BX220K	CAP 22PF 10% 200V CER
C79	M39014/02-1310	CAP .1UF 10% 100V CER-R
C80	C26-0025-339	CAP 3.3UF 20% 25V TANT
C81	C26-0025-339	CAP 3.3UF 20% 25V TANT
C82	M39014/02-1310	CAP .1UF 10% 100V CER-R
C83	M39014/02-1310	CAP .1UF 10% 100V CER-R
C84	M39014/02-1310	CAP .1UF 10% 100V CER-R
C85	M39014/02-1310	CAP .1UF 10% 100V CER-R
C86	M39014/02-1310	CAP .1UF 10% 100V CER-R
C87	M39014/02-1310	CAP .1UF 10% 100V CER-R
C88	M39014/02-1310	CAP .1UF 10% 100V CER-R
C89	M39014/02-1310	CAP .1UF 10% 100V CER-R
C90	M39014/02-1310	CAP .1UF 10% 100V CER-R
C91	M39014/02-1310	CAP .1UF 10% 100V CER-R
C92	M39014/02-1310	CAP .1UF 10% 100V CER-R
C93	M39014/02-1310	CAP .1UF 10% 100V CER-R
C94	M39014/02-1310	CAP .1UF 10% 100V CER-R
C95	M39014/02-1310	CAP .1UF 10% 100V CER-R

Table 3. IF/Audio Assembly A5 Parts List (10215-5410, Rev. N/-5410-02, Rev. D) (Cont.)

Ref. Desig.	Part Number	Description
C96	CK05BX101K	CAP 100PF 10% 200V CER
C97	M39014/02-1310	CAP .1UF 10% 100V CER-R
C98	CK05BX470K	CAP 47PF 10% 200V CER
C99	CK05BX221K	CAP 220PF 10% 200V CER
C100	CK05BX471K	CAP 470PF 10% 200V CER
C101	CK05BX471K	CAP 470PF 10% 200V CER
C102	M39014/02-1310	CAP .1UF 10% 100V CER-R
C103	M39014/02-1310	CAP .1UF 10% 100V CER-R
C104	M39014/02-1298	CAP .01UF 10% 200V CER-R
C105	M39014/02-1298	CAP .01UF 10% 200V CER-R
C106	M39014/02-1310	CAP .1UF 10% 100V CER-R
C107	M39014/02-1310	CAP .1UF 10% 100V CER-R
C108	M39014/02-1310	CAP .1UF 10% 100V CER-R
C109	CK05BX471K	CAP 470PF 10% 200V CER
CR1	D12-0007-001	DIODE PIN ATTN 1W 9301
CR2	D12-0007-001	DIODE PIN ATTN 1W 9301
CR3	1N4454	DIODE 200MA 75V SW
CR4	1N4454	DIODE 200MA 75V SW
CR5	D12-0007-001	DIODE PIN ATTN 1W 9301
CR6	1N4454	DIODE 200MA 75V SW
CR7	1N4454	DIODE 200MA 75V SW
CR8	D12-0007-001	DIODE PIN ATTN 1W 9301
CR9	1N4454	DIODE 200MA 75V SW
CR10	1N4454	DIODE 200MA 75V SW
CR11	1N4454	DIODE 200MA 75V SW
CR12	1N4454	DIODE 200MA 75V SW
CR13	1N4454	DIODE 200MA 75V SW
CR15	1N4454	DIODE 200MA 75V SW
CR16	1N4454	DIODE 200MA 75V SW
CR17	1N4454	DIODE 200MA 75V SW
CR19	1N4454	DIODE 200MA 75V SW
CR20	1N4454	DIODE 200MA 75V SW
CR21	1N4454	DIODE 200MA 75V SW
CR22	1N4454	DIODE 200MA 75V SW
CR23	1N4454	DIODE 200MA 75V SW
CR24	1N4454	DIODE 200MA 75V SW
CR25	1N4454	DIODE 200MA 75V SW
CR26	1N4454	DIODE 200MA 75V SW
CR27	1N4454	DIODE 200MA 75V SW
CR28	1N4454	DIODE 200MA 75V SW
CR29	1N4454	DIODE 200MA 75V SW
CR30	1N4454	DIODE 200MA 75V SW
CR31	1N4454	DIODE 200MA 75V SW
CR32	1N4454	DIODE 200MA 75V SW
CR33	1N4454	DIODE 200MA 75V SW
CR34	1N4454	DIODE 200MA 75V SW
CR35	1N4454	DIODE 200MA 75V SW
CR36	1N4454	DIODE 200MA 75V SW

Table 3. IF/Audio Assembly A5 Parts List (10215-5410, Rev. N/-5410-02, Rev. D) (Cont.)

Ref. Desig.	Part Number	Description
CR37	1N4454	DIODE 200MA 75V SW
CR38	1N4454	DIODE 200MA 75V SW
CR39	1N4454	DIODE 200MA 75V SW
CR40	1N4454	DIODE 200MA 75V SW
CR41	1N4454	DIODE 200MA 75V SW
CR42	1N4454	DIODE 200MA 75V SW
FL1	G25-0003-003	CER FILTER 455KHZ 10KHZBW
J1	J-0031	CONN SMB VERT PCB F
J2	J90-0014-001	CONN SMB VERT PCB MT M
J3	J-0031	CONN SMB VERT PCB F
J4	J-0031	CONN SMB VERT PCB F
J5	J46-0022-006	HDR 6 PIN 0.100" SR LKG
J6	J46-0013-016	HDR 16 PIN 0.100" DR SHRD
J7	J46-0022-004	HDR 4 PIN 0.100" SR LKG
J8	J46-0022-010	HDR 10 PIN 0.100" SR LKG
J9	J46-0022-010	HDR 10 PIN 0.100" SR LKG
J10	J46-0013-010	HDR 10 PIN 0.100 DR SHRD
J11	J43-0006-008	CONN 8 SKT SINGLE.100
J12	J46-0022-003	HDR 3 PIN 0.100" SR LKG
J13	J46-0022-002	HDR 2 PIN 0.100" SR LKG
JMP3	MP-1142	RES ZERO OHM (CKT JMPR)
JMP7	MP-1142	RES ZERO OHM (CKT JMPR)
L1	MS75085-15	COIL 470UH 10% FXD RF
L2	MS75085-15	COIL 470UH 10% FXD RF
L3	MS75085-15	COIL 470UH 10% FXD RF
L4	MS75085-15	COIL 470UH 10% FXD RF
L5	MS75085-15	COIL 470UH 10% FXD RF
L6	MS75089-21	COIL 680UH 10% FXD RF
L7	L11-0004-032	INDUCT SH VAR 35.1-42.9UH
Q1	2N4403	XSTR SS/GP PNP TO-92
Q2	2N4401	XSTR SS/GP NPN TO-92
Q3	2N4401	XSTR SS/GP NPN TO-92
Q4	2N4403	XSTR SS/GP PNP TO-92
Q5	2N4401	XSTR SS/GP NPN TO-92
Q6	2N4401	XSTR SS/GP NPN TO-92
Q7	2N4401	XSTR SS/GP NPN TO-92
Q8	Q35-0003-000	XSTR N-CH JFET U310
Q9	2N4403	XSTR SS/GP PNP TO-92
Q10	2N4401	XSTR SS/GP NPN TO-92
Q12	2N4401	XSTR SS/GP NPN TO-92
Q13	2N4403	XSTR SS/GP PNP TO-92
Q14	2N4403	XSTR SS/GP PNP TO-92
Q15	2N4401	XSTR SS/GP NPN TO-92
Q16	2N4401	XSTR SS/GP NPN TO-92
Q17	2N4403	XSTR SS/GP PNP TO-92
R1	R65-0003-151	RES 150 5% 1/4W CAR FILM
R2	R65-0003-151	RES 150 5% 1/4W CAR FILM
R3	R65-0003-151	RES 150 5% 1/4W CAR FILM
R4	R65-0003-751	RES 750 5% 1/4W CAR FILM

Table 3. IF/Audio Assembly A5 Parts List (10215-5410, Rev. N/-5410-02, Rev. D) (Cont.)

Ref. Desig.	Part Number	Description
R5	R65-0003-301	RES 300 5% 1/4W CAR FILM
R6	R65-0003-182	RES 1.8K 5% 1/4W CAR FILM
R7	R65-0002-181	RES 180 5% 1/8W CAR FILM
R8	R65-0003-223	RES 22K 5% 1/4W CAR FILM
R9	R65-0003-101	RES 100 5% 1/4W CAR FILM
R10	RN55D3922F	RES 39.2K 1% 1/8W MET FLM
R11	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R12	R65-0003-561	RES 560 5% 1/4W CAR FILM
R13	R65-0003-562	RES 5.6K 5% 1/4W CAR FILM
R14	R65-0003-270	RES 27 5% 1/4W CAR FILM
R15	R65-0003-391	RES 390 5% 1/4W CAR FILM
R16	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R17	R65-0003-242	RES 2.4K 5% 1/4W CAR FILM
R18	R65-0003-561	RES 560 5% 1/4W CAR FILM
R19	R65-0003-561	RES 560 5% 1/4W CAR FILM
R20	R65-0003-561	RES 560 5% 1/4W CAR FILM
R21	R65-0003-152	RES 1.5K 5% 1/4W CAR FILM
R22	R65-0003-152	RES 1.5K 5% 1/4W CAR FILM
R23	R65-0003-182	RES 1.8K 5% 1/4W CAR FILM
R24	RN55D1003F	RES 100K 1% 1/8W MET FLM
R25	R65-0003-202	RES 2.0K 5% 1/4W CAR FILM
R26	RN55D3162F	RES 31.6K 1% 1/8W MET FLM
R27	RN55D1001F	RES 1000 1% 1/8W MET FLM
R28	R65-0003-152	RES 1.5K 5% 1/4W CAR FILM
R29	RN55D2002F	RES 20.0K 1% 1/8W MET FLM
R30	R65-0003-203	RES 20K 5% 1/4W CAR FILM
R31	R65-0003-152	RES 1.5K 5% 1/4W CAR FILM
R32	R65-0003-821	RES 820 5% 1/4W CAR FILM
R33	R65-0003-470	RES 47 5% 1/4W CAR FILM
R34	R65-0003-223	RES 22K 5% 1/4W CAR FILM
R35	R65-0003-562	RES 5.6K 5% 1/4W CAR FILM
R36	R65-0003-222	RES 2.2K 5% 1/4W CAR FILM
R37	R65-0003-332	RES 3.3K 5% 1/4W CAR FILM
R38	R65-0003-821	RES 820 5% 1/4W CAR FILM
R39	R65-0003-752	RES 7.5K 5% 1/4W CAR FILM
R40	R65-0003-154	RES 150K 5% 1/4W CAR FILM
R41	RN55D3162F	RES 31.6K 1% 1/8W MET FLM
R42	RN55D1001F	RES 1000 1% 1/8W MET FLM
R43	R65-0003-202	RES 2.0K 5% 1/4W CAR FILM
R44	R30-0008-104	RES VAR PCB 100K 1/2W 10%
R45	R65-0003-104	RES 100K 5% 1/4W CAR FILM
R46	RN55D8062F	RES 80.6K 1% 1/8W MET FLM
R47	RN55D2002F	RES 20.0K 1% 1/8W MET FLM
R48	RN55D8062F	RES 80.6K 1% 1/8W MET FLM
R49	RN55D2002F	RES 20.0K 1% 1/8W MET FLM
R50	RN55D2002F	RES 20.0K 1% 1/8W MET FLM
R51	RN55D1002F	RES 10.0K 1% 1/8W MET FLM
R52	R65-0003-473	RES 47K 5% 1/4W CAR FILM

Table 3. IF/Audio Assembly A5 Parts List (10215-5410, Rev. N/-5410-02, Rev. D) (Cont.)

Ref. Desig.	Part Number	Description
R53	R65-0003-394	RES 390K 5% 1/4W CAR FILM
R54	R65-0003-824	RES 820K 5% 1/4W CAR FILM
R55	R65-0003-562	RES 5.6K 5% 1/4W CAR FILM
R56	R65-0003-470	RES 47 5% 1/4W CAR FILM
R57	R65-0003-203	RES 20K 5% 1/4W CAR FILM
R58	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R59	RN55D8062F	RES 80.6K 1% 1/8W MET FLM
R60	R65-0003-104	RES 100K 5% 1/4W CAR FILM
R61	R65-0003-515	RES 5.1M 5% 1/4W CAR FILM
R62	R65-0003-333	RES 33K 5% 1/4W CAR FILM
R63	R65-0003-242	RES 2.4K 5% 1/4W CAR FILM
R64	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R65	R65-0003-392	RES 3.9K 5% 1/4W CAR FILM
R66	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R67	R65-0003-513	RES 51K 5% 1/4W CAR FILM
R68	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R69	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R70	R65-0003-104	RES 100K 5% 1/4W CAR FILM
R71	R65-0003-563	RES 56K 5% 1/4W CAR FILM
R72	R65-0003-512	RES 5.1K 5% 1/4W CAR FILM
R73	R65-0002-153	RES 15K 5% 1/8W CAR FILM
R74	R-2207	RES VAR 2K 10% .5W HOR.
R75	R65-0003-392	RES 3.9K 5% 1/4W CAR FILM
R76	R65-0003-564	RES 560K 5% 1/4W CAR FILM
R77	R65-0003-183	RES 18K 5% 1/4W CAR FILM
R78	R-2204	RES VAR 200 10% .5W HOR.
R79	R-2205	RES VAR 500 10% .5W HOR.
R80	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R81	R65-0003-333	RES 33K 5% 1/4W CAR FILM
R82	R65-0003-201	RES 200 5% 1/4W CAR FILM
R83	R65-0003-431	RES 430 5% 1/4W CAR FILM
R84	R65-0003-563	RES 56K 5% 1/4W CAR FILM
R85	R65-0003-104	RES 100K 5% 1/4W CAR FILM
R86	R65-0003-104	RES 100K 5% 1/4W CAR FILM
R87	R65-0003-123	RES 12K 5% 1/4W CAR FILM
R88	RN55D3162F	RES 31.6K 1% 1/8W MET FLM
R89	R65-0003-333	RES 33K 5% 1/4W CAR FILM
R90	RN55D1001F	RES 1000 1% 1/8W MET FLM
R91	D40-0004-003	THERM 1K 5% @ 25DEG
R92	D40-0004-003	THERM 1K 5% @ 25DEG
R93	D40-0004-003	THERM 1K 5% @ 25DEG
R94	RN55D1823F	RES 182K 1% 1/8W MET FLM
R95	R65-0003-202	RES 2.0K 5% 1/4W CAR FILM
R96	RN55D3012F	RES 30.1K 1% 1/8W MET FLM
R97	R65-0003-470	RES 47 5% 1/4W CAR FILM
R98	R65-0003-100	RES 10 5% 1/4W CAR FILM
R99	R65-0003-222	RES 2.2K 5% 1/4W CAR FILM
R100	R65-0003-680	RES 68 5% 1/4W CAR FILM

Table 3. IF/Audio Assembly A5 Parts List (10215-5410, Rev. N/-5410-02, Rev. D) (Cont.)

Ref. Desig.	Part Number	Description
R101	R65-0003-680	RES 68 5% 1/4W CAR FILM
R102	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R103	R65-0003-682	RES 6.8K 5% 1/4W CAR FILM
R104	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R105	R50-0010-473	RES 47K 2% 10SIP 9RES
R106	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R107	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R108	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R109	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R110	R65-0003-101	RES 100 5% 1/4W CAR FILM
R111	R50-0010-473	RES 47K 2% 10SIP 9RES
R112	R65-0003-271	RES 270 5% 1/4W CAR FILM
R113	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R114	R65-0003-821	RES 820 5% 1/4W CAR FILM
R115	R65-0003-392	RES 3.9K 5% 1/4W CAR FILM
R116	R65-0003-392	RES 3.9K 5% 1/4W CAR FILM
R117	R65-0003-273	RES 27K 5% 1/4W CAR FILM
R118	R65-0003-273	RES 27K 5% 1/4W CAR FILM
R119	R65-0003-154	RES 150K 5% 1/4W CAR FILM
R120	R65-0003-154	RES 150K 5% 1/4W CAR FILM
R121	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R122	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R123	R65-0003-302	RES 3.0K 5% 1/4W CAR FILM
R124	R65-0003-511	RES 510 5% 1/4W CAR FILM
R125	R65-0003-153	RES 15K 5% 1/4W CAR FILM
R126	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R127	R65-0003-471	RES 470 5% 1/4W CAR FILM
R128	R65-0003-244	RES 240K 5% 1/4W CAR FILM
R130	R65-0003-622	RES 6.2K 5% 1/4W CAR FILM
R131	R65-0003-223	RES 22K 5% 1/4W CAR FILM
R132	R65-0003-104	RES 100K 5% 1/4W CAR FILM
R133	R65-0003-104	RES 100K 5% 1/4W CAR FILM
R134	R65-0003-104	RES 100K 5% 1/4W CAR FILM
R135	R65-0003-104	RES 100K 5% 1/4W CAR FILM
R136	R65-0003-104	RES 100K 5% 1/4W CAR FILM
R137	R65-0003-104	RES 100K 5% 1/4W CAR FILM
R138	R65-0003-104	RES 100K 5% 1/4W CAR FILM
R139	R65-0004-330	RES 33 5% 1/2W CAR FILM
R140	R65-0002-223	RES 22K 5% 1/8W CAR FILM
R141	R65-0002-821	RES 820 5% 1/8W CAR FILM
R142	R65-0003-104	RES 100K 5% 1/4W CAR FILM
R143	R65-0003-114	RES 110K 5% 1/4W CAR FILM
R144	R65-0003-333	RES 33K 5% 1/4W CAR FILM
R145	R65-0003-153	RES 15K 5% 1/4W CAR FILM
R146	R65-0003-152	RES 1.5K 5% 1/4W CAR FILM
R147	R65-0003-333	RES 33K 5% 1/4W CAR FILM
R148	R65-0003-184	RES 180K 5% 1/4W CAR FILM

Table 3. IF/Audio Assembly A5 Parts List (10215-5410, Rev. N/-5410-02, Rev. D) (Cont.)

Ref. Desig.	Part Number	Description
R149	R65-0003-221	RES 220 5% 1/4W CAR FILM
R153	R65-0003-563	RES 56K 5% 1/4W CAR FILM
R154	R65-0003-822	RES 8.2K 5% 1/4W CAR FILM
R155	R65-0003-473	RES 47K 5% 1/4W CAR FILM
R156	R65-0003-473	RES 47K 5% 1/4W CAR FILM
R157	R65-0003-154	RES 150K 5% 1/4W CAR FILM
R158	R65-0003-822	RES 8.2K 5% 1/4W CAR FILM
R159	R65-0003-203	RES 20K 5% 1/4W CAR FILM
R160	R65-0003-104	RES 100K 5% 1/4W CAR FILM
R161	R65-0003-114	RES 110K 5% 1/4W CAR FILM
R162	R65-0003-101	RES 100 5% 1/4W CAR FILM
R163	R65-0003-754	RES 750K 5% 1/4W CAR FILM
R164	R65-0003-473	RES 47K 5% 1/4W CAR FILM
R167	R65-0003-183	RES 18K 5% 1/4W CAR FILM
R169	R65-0003-473	RES 47K 5% 1/4W CAR FILM
R171	R65-0003-473	RES 47K 5% 1/4W CAR FILM
R172	R65-0003-473	RES 47K 5% 1/4W CAR FILM
R173	R65-0003-560	RES 56 5% 1/4W CAR FILM
R174	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R175	R65-0003-164	RES 160K 5% 1/4W CAR FILM
R176	R65-0003-223	RES 22K 5% 1/4W CAR FILM
R177	R65-0003-223	RES 22K 5% 1/4W CAR FILM
R178	R65-0003-184	RES 180K 5% 1/4W CAR FILM
R179	R65-0003-683	RES 68K 5% 1/4W CAR FILM
R180	R-2211	RES VAR 25K 10% .5W HOR.
R181	R65-0003-682	RES 6.8K 5% 1/4W CAR FILM
R182	R65-0003-473	RES 47K 5% 1/4W CAR FILM
R183	R65-0004-151	RES 150 5% 1/2W CAR FILM
R184	R65-0004-151	RES 150 5% 1/2W CAR FILM
R185	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R186	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R187	R65-0003-473	RES 47K 5% 1/4W CAR FILM
R188	R65-0003-473	RES 47K 5% 1/4W CAR FILM
R189	R65-0003-101	RES 100 5% 1/4W CAR FILM
R190	R65-0003-473	RES 47K 5% 1/4W CAR FILM
R191	R65-0003-473	RES 47K 5% 1/4W CAR FILM
R192	R65-0003-331	RES 330 5% 1/4W CAR FILM
R193	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R194	R30-0008-501	RES VAR PCB 500 1/2W 10%
R195	R65-0003-184	RES 180K 5% 1/4W CAR FILM
R196	R65-0003-392	RES 3.9K 5% 1/4W CAR FILM
R197	R65-0003-474	RES 470K 5% 1/4W CAR FILM
R198	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R199	R65-0003-153	RES 15K 5% 1/4W CAR FILM
R200	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R201	R65-0003-223	RES 22K 5% 1/4W CAR FILM
R202	R65-0003-123	RES 12K 5% 1/4W CAR FILM
R203	R65-0003-104	RES 100K 5% 1/4W CAR FILM

Table 3. IF/Audio Assembly A5 Parts List (10215-5410, Rev. N/-5410-02, Rev. D) (Cont.)

Ref. Desig.	Part Number	Description
R204	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R205	R65-0003-333	RES 33K 5% 1/4W CAR FILM
R206	R65-0003-333	RES 33K 5% 1/4W CAR FILM
R207	R65-0003-101	RES 100 5% 1/4W CAR FILM
R208	R65-0002-103	RES 10K 5% 1/8W CAR FILM
R209	R65-0003-560	RES 56 5% 1/4W CAR FILM
R210	R65-0003-332	RES 3.3K 5% 1/4W CAR FILM
R210	R65-0003-512	RES 5.1K 5% 1/4W CAR FILM
R211	R65-0003-223	RES 22K 5% 1/4W CAR FILM
T2	10085-5012	BALUN RF/IF
T3	10085-5012	BALUN RF/IF
TP0	J-0067	TP PWB BLK TOP ACCS .080"
TP1	J-0071	TP PWB BRN TOP ACCS .080"
TP2	J-0066	TP PWB RED TOP ACCS .080"
TP3	J46-0047-001	HDR 1 POSITION
TP4	J46-0047-001	HDR 1 POSITION
TP5	J46-0047-001	HDR 1 POSITION
TP6	J46-0047-001	HDR 1 POSITION
TP8	J-0074	TP PWB GRA TOP ACCS .080"
TP9	J46-0047-001	HDR 1 POSITION
U2	I30-0035-000	IC OP AMP QUAD 072
U3	I30-0038-001	IC OP AMP QUAD 347
U4	I06-0002-001	IC DG211 ANALOG SW QUAD
U5	I01-0000-353	IC 4538B PLASTIC CMOS
U6	I01-0000-003	IC 4001B PLASTIC CMOS
U7	I30-0003-000	IC OP AMP QUAD 324
U8	I01-0000-003	IC 4001B PLASTIC CMOS
U9	I01-0000-023	IC 4071B PLASTIC CMOS
U10	I14-0001-001	IC PS CONTROLLER 5561
U11	I62-0001-000	IC 1496 BAL MODULATOR
U12	I30-0038-001	IC OP AMP QUAD 347
U13	I30-0038-002	IC OP AMP QUAD 347
U16	I06-0002-001	IC DG211 ANALOG SW QUAD
U17	I01-0000-021	IC 4069UB PLASTIC CMOS
U18	I60-0003-001	IC 1357/2111 FM/IF AMP
U19	I01-0000-252	IC 4053B PLASTIC CMOS
U20	I01-0000-008	IC 4011B PLASTIC CMOS
U21	I06-0002-001	IC DG211 ANALOG SW QUAD
U22	I30-0035-000	IC OP AMP QUAD 072
U23	I24-0001-000	IC COMPANDOR NE571 PLAS
U24	I33-0001-101	IC CURRENT AMP LH0002
U25	I90-0011-002	IC XSTR ARRAY NPN PR 394
U26	I90-0011-002	IC XSTR ARRAY NPN PR 394
U28	I30-0003-000	IC OP AMP QUAD 324
U29	I30-0003-000	IC OP AMP QUAD 324
U30	I30-0020-103	IC OP AMP DUAL 358
U32	I30-0003-000	IC OP AMP QUAD 324
VR1	I12-0006-005	IC VR 78L05A +5V .10A 4%
VR2	I12-0006-008	IC VR 78L08A +8V .10A 4%

Table 3. IF/Audio Assembly A5 Parts List (10215-5410, Rev. N/-5410-02, Rev. D) (Cont.)

Ref. Desig.	Part Number	Description
VR3	I12-0010-005	IC VR 79L05A -5V .10A 4%
VR4	1N5231B	DIODE 5.1V 5% .5W ZENER
VR5	1N5231B	DIODE 5.1V 5% .5W ZENER
VR6	1N5235B	DIODE 6.8V 5% .5W ZENER
VR7	1N5235B	DIODE 6.8V 5% .5W ZENER

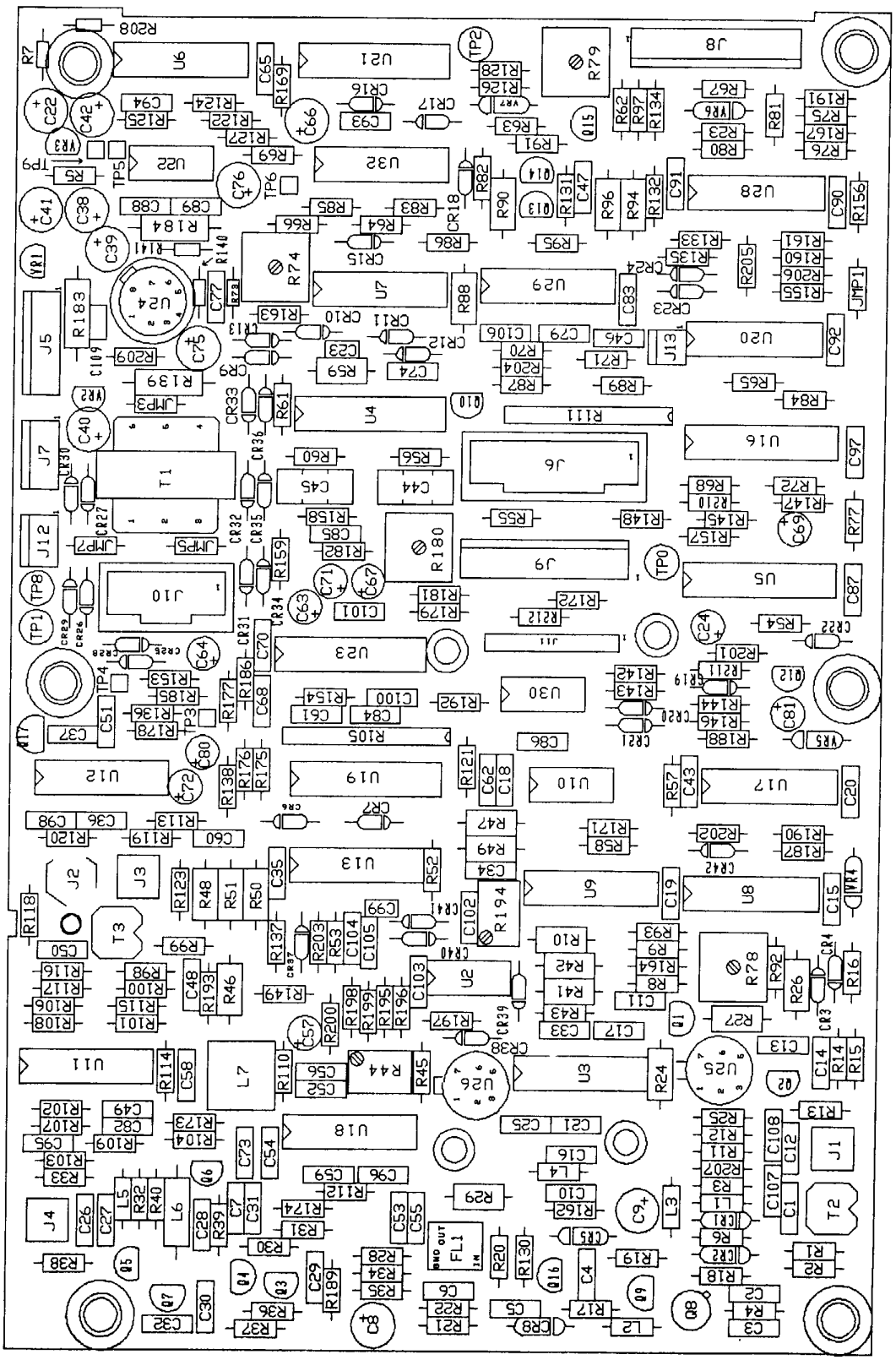


Figure 3. IF/Audio Assembly A5 Component Locations (10215-5410, Rev. H)

NOTE: UNLESS OTHERWISE SPECIFIED:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR A COMPLETE DESIGNATION, PREFIX WITH UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.
2. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, ±5%.
3. ALL CAPACITOR VALUES ARE IN MICROFARADS.
4. VENDOR PART NO. CALLOUTS ARE FOR REFERENCE ONLY. COMPONENTS ARE SUPPLIED PER PART NO. IN PARTS LIST.
5. SEE SHEET 6 FOR UNUSED GATES, UNUSED SECTIONS OF SIP'S, AND IC SUPPLY CONNECTIONS.
6. ALL DIODE PART NUMBERS ARE IN4454.
7. THIS IS A TABULATED DRAWING SEE SHT 5 FOR -01 AND -02 APPLICATIONS.
8. 454MHZ @ -80dBm INPUT AT J1 fc=10.000MHZ AGC: FST RF GAIN MAX.

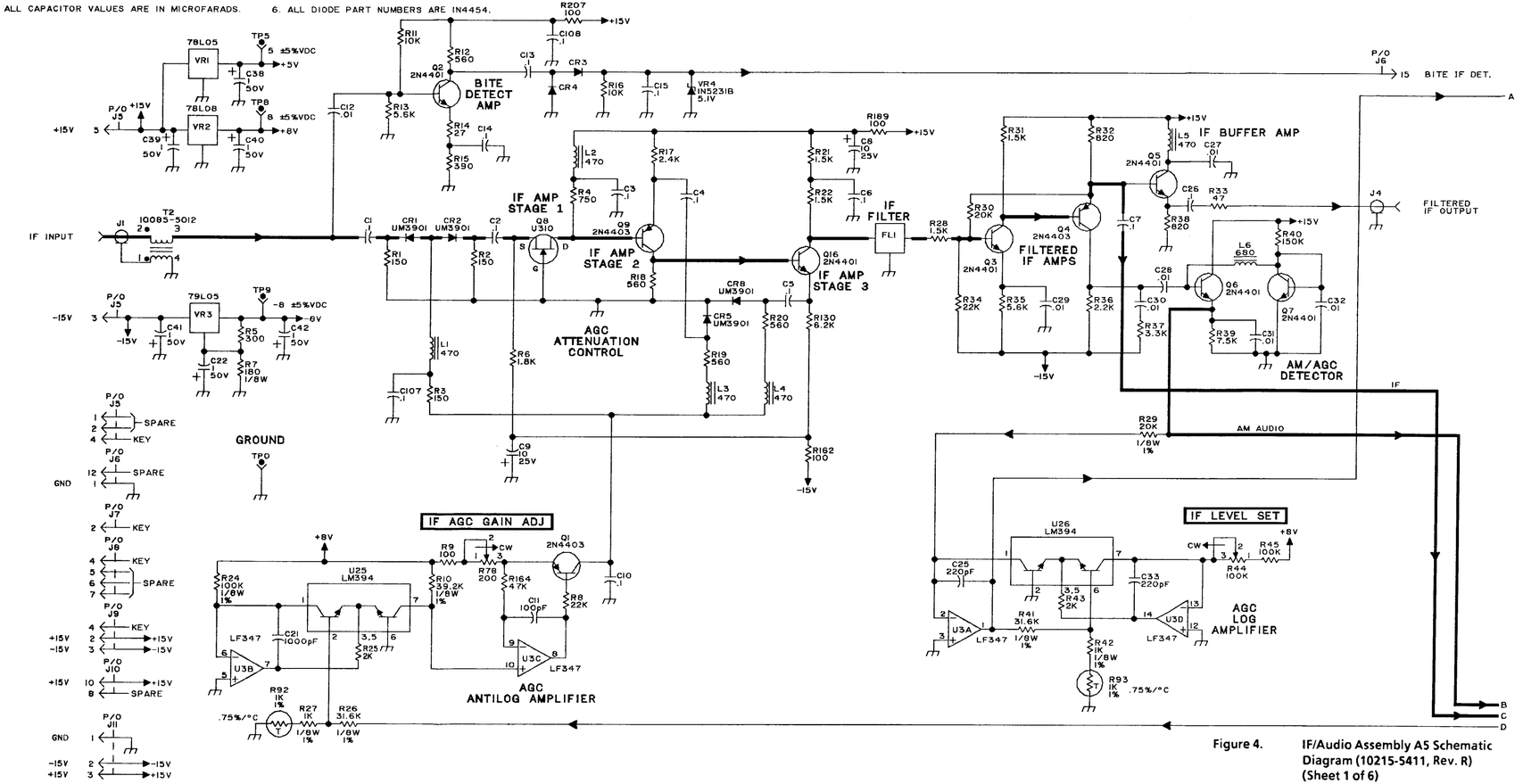


Figure 4. IF/Audio Assembly A5 Schematic Diagram (10215-5411, Rev. R) (Sheet 1 of 6)

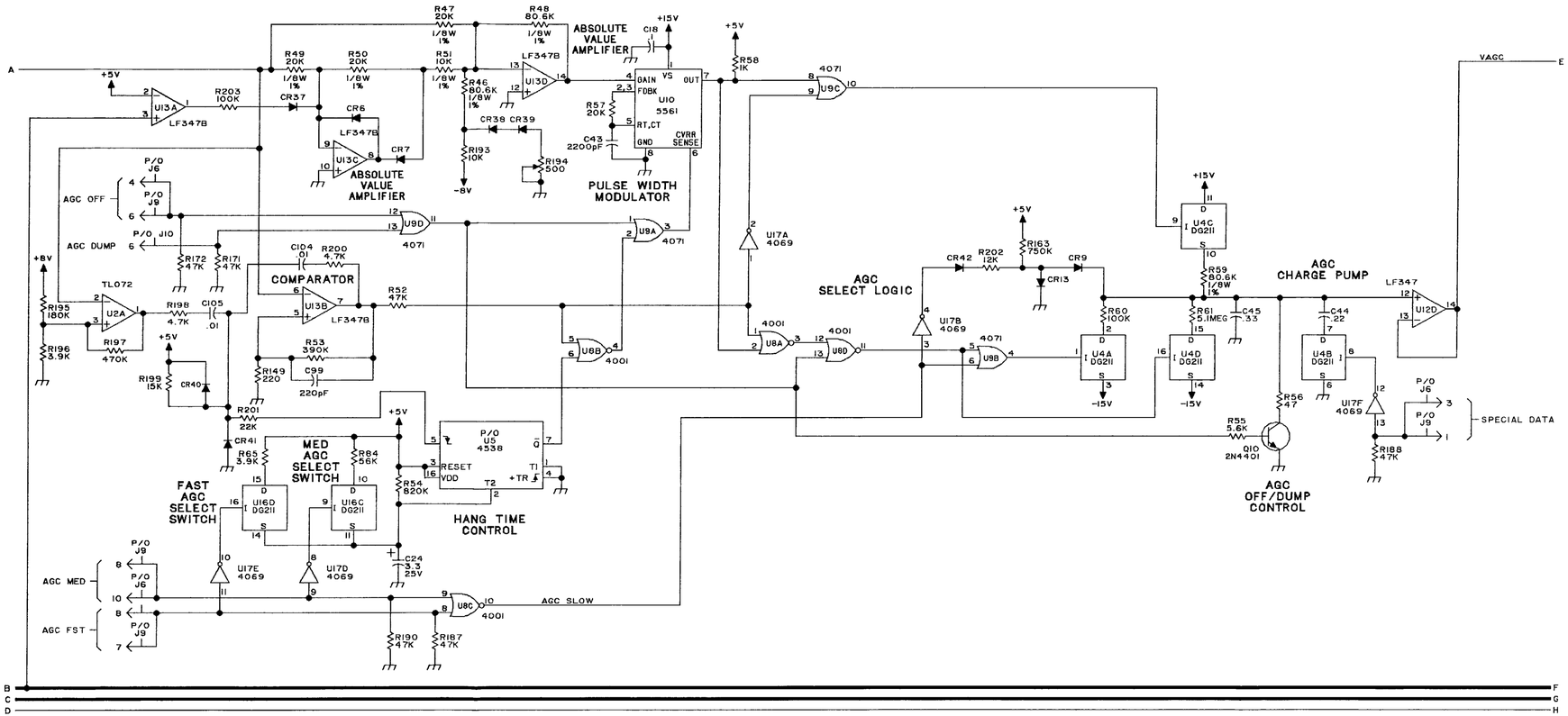


Figure 4. IF/Audio Assembly A5 Schematic Diagram (10215-5411, Rev. R) (Sheet 2 of 6)

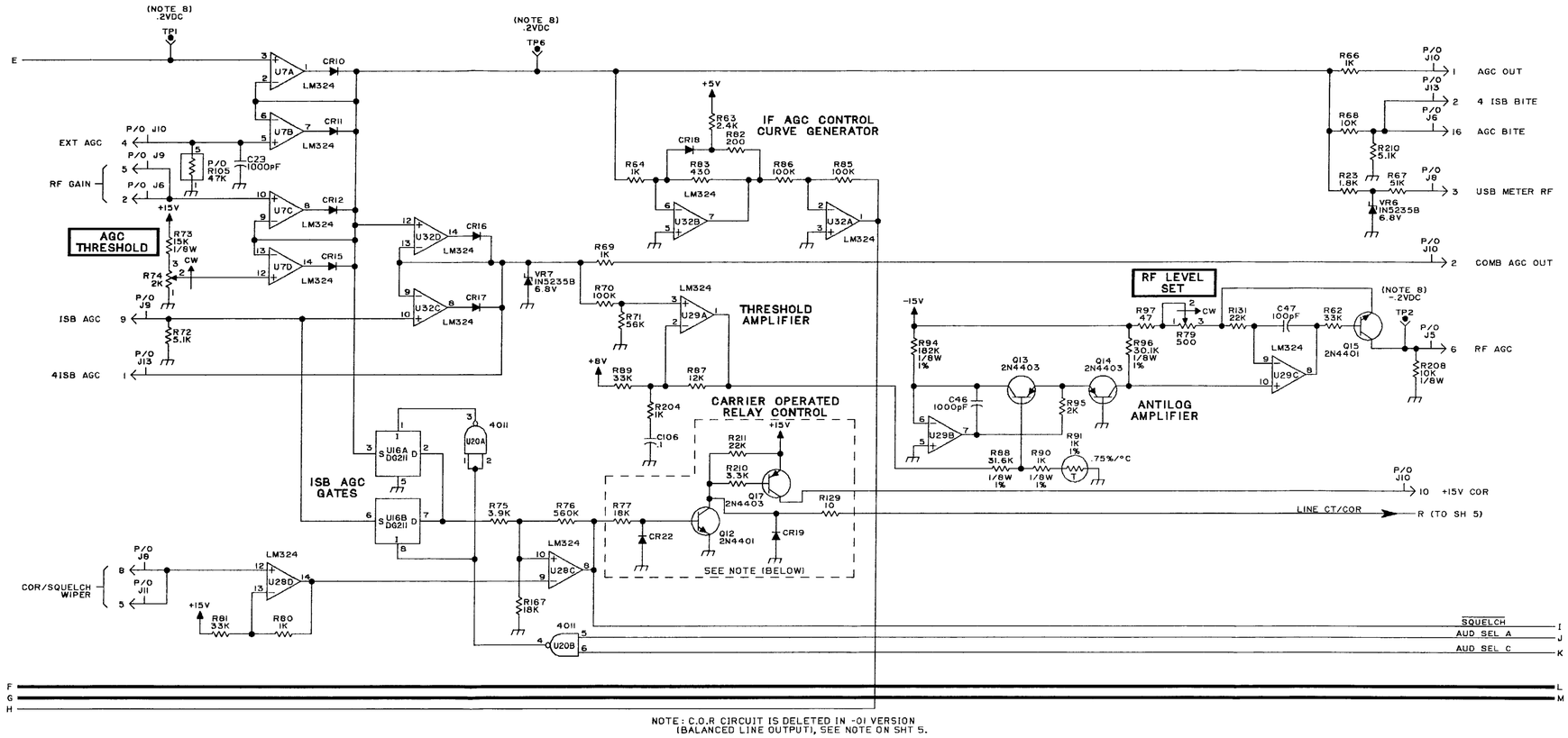


Figure 4. IF/Audio Assembly A5 Schematic Diagram (10215-5411, Rev. R) (Sheet 3 of 6)

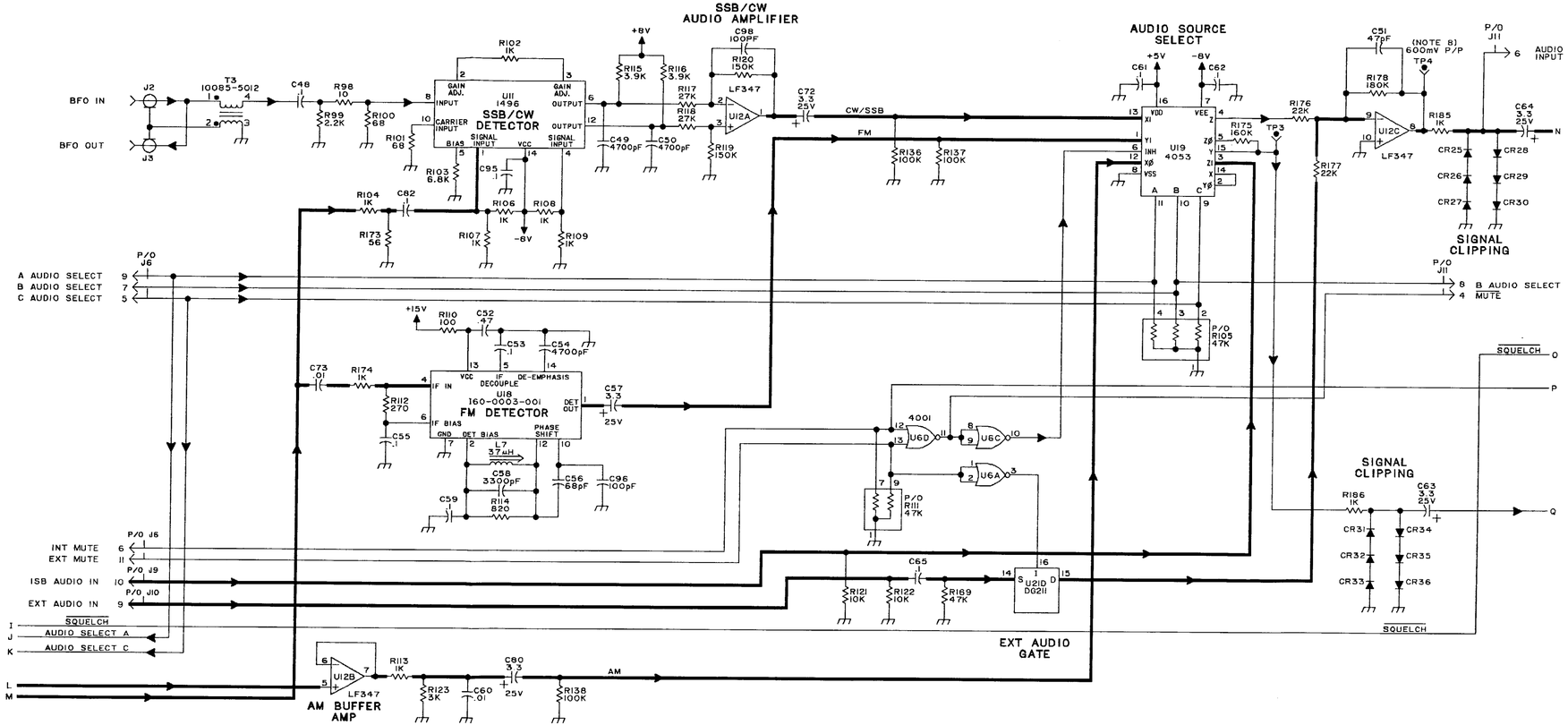


Figure 4. IF/Audio Assembly A5 Schematic Diagram (10215-5411, Rev. R) (Sheet 4 of 6)

NOTE:
USE THE APPROPRIATE TABLE FOR -01, -02 AND -04 APPLICATIONS

REF DES	-01 ASSY (+10dBm BALANCED LINE)	-02 ASSY (+15dBm UNBALANCED LINE)	-04 ASSY (10215-6930 OPTION)
CR19	DELETED	INSTALLED	DELETED
CR22	DELETED	INSTALLED	DELETED
Q12	DELETED	INSTALLED	DELETED
R77	DELETED	INSTALLED	DELETED
R129	DELETED	INSTALLED	DELETED
R139	180 1/2W	33 1/2W	180 1/2W
R143	300K	110K	110K
T1	INSTALLED	DELETED	INSTALLED
JMP 1	INSTALLED	DELETED	DELETED
JMP 2	NOT USED	NOT USED	NOT USED
JMP 3	DELETED	INSTALLED	DELETED
JMP 4	INSTALLED	DELETED	INSTALLED
JMP 5	INSTALLED	DELETED	INSTALLED
JMP 6	INSTALLED	DELETED	INSTALLED
JMP 7	DELETED	INSTALLED	DELETED

FROM SHT 3

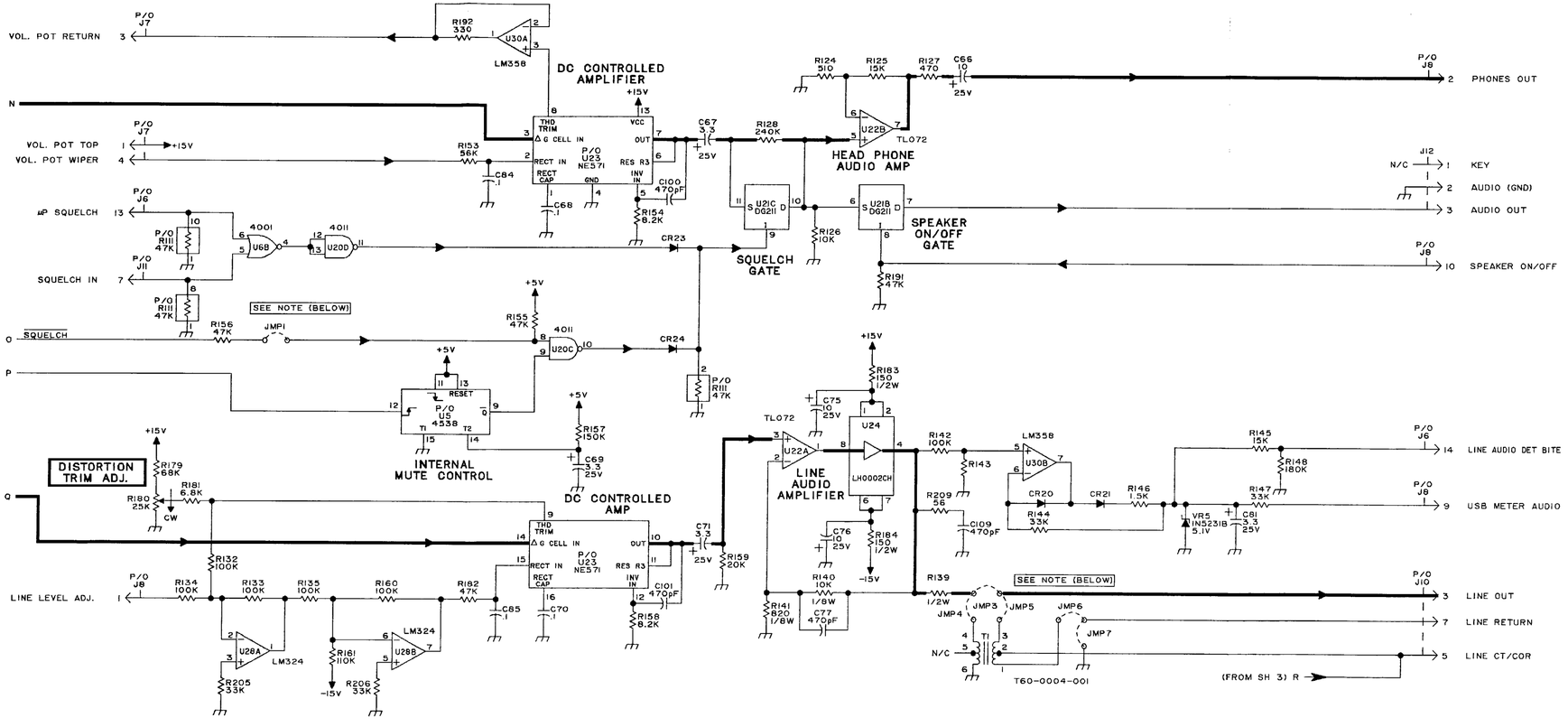


Figure 4. IF/Audio Assembly A5 Schematic Diagram (10215-5411, Rev. R) (Sheet 5 of 6)

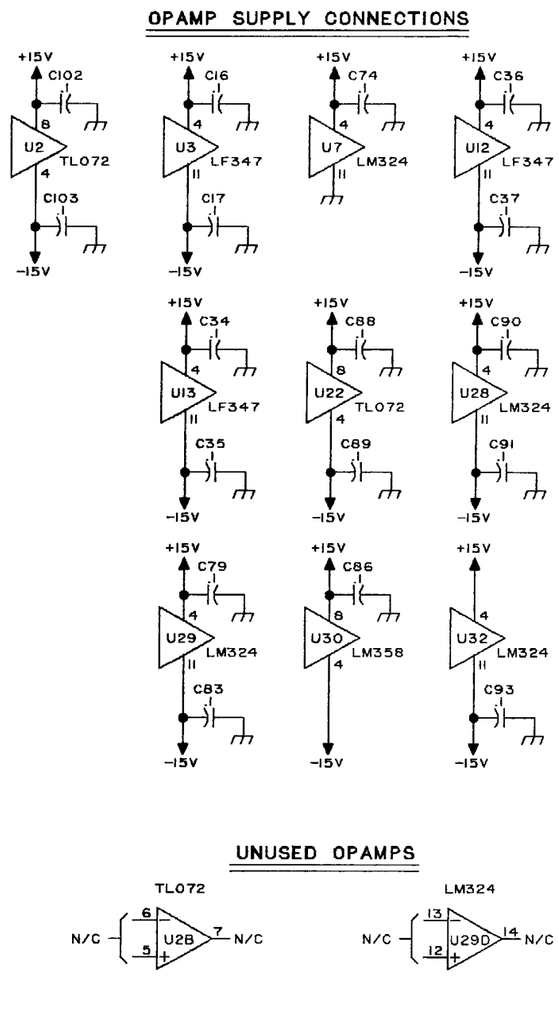


Figure 4. IF/Audio Assembly A5 Schematic Diagram (10215-5411, Rev. R) (Sheet 6 of 6)

A10
SYNTHESIZER ASSEMBLY

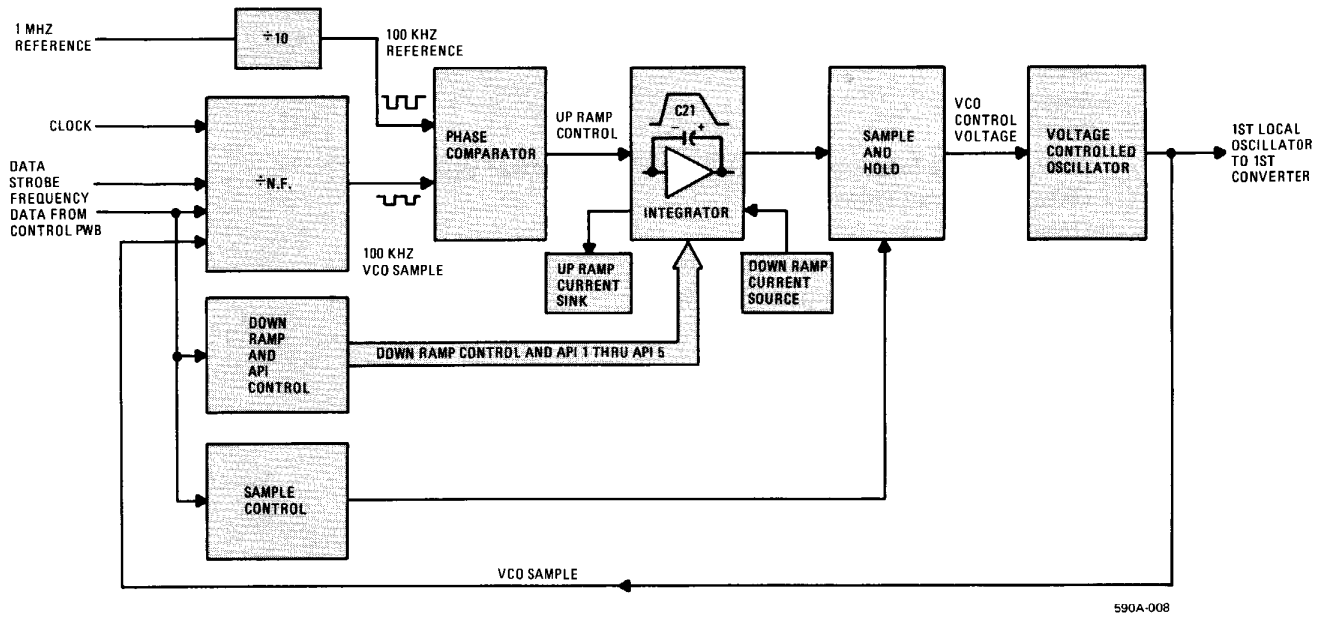


TABLE OF CONTENTS

Paragraph		Page
1.	Introduction	1
2.	Interface Connections	1
3.	Technical Description	1
3.1	Functional Description	2
3.1.1	General Information	2
3.1.2	Description of Fractional Divide-by-N Phase Lock Loop	4
3.1.2.2	Example of Divide-By-N.F.	2
3.1.2.2.1	Step 1	5
3.1.2.2.2	Step 2	5
3.1.2.2.3	Step 3	5
3.1.2.2.4	Step 4	5
3.1.2.2.5	Step 5	5
3.1.2.2.6	Step 6	5
3.1.2.2.7	Step 7	5
3.1.2.2.8	Step 8	5
3.1.2.2.9	Step 9	6
3.1.2.3	Analog Phase Interpolation (API) and VCO Control Voltage	6
3.2	Detailed Circuit Operation	7
3.2.1	Data Inputs.	7
3.2.2	Phase Detector - General Description	7
3.2.3	Phase Detector Up Ramp and Sample	7
3.2.4	Down Ramp and API	7
3.2.5	Sample and Hold	13
3.3	VCO	13
3.4	Divide-By-N.F Circuit	13
3.4.1	Divide-By-N	14
3.4.2	Divide-By-519 Cycle Step One	19
3.4.3	Divide-by-519 Cycle Step Two	19
3.4.4	Divide-by-519 Cycle Step Three.	19
3.4.5	Divide-by-519 Cycle Step Four	19
3.4.6	Divide-by-519 Cycle Step Five	19
3.4.7	Divide-by-519 Cycle Step Six	19
3.4.8	Divide-by-519 Cycle Step Seven.	19
3.4.9	Divide-by-519 Cycle Step Eight	19
3.4.10	Divide-by-519 Cycle Step Nine.	20
3.5	Divide-By-F (Fractional)	20
4.	Maintenance	20
4.1	Test Procedure	20
4.1.1	Required Test Equipment	20
4.1.2	Preliminary Procedure	23
4.1.3	Out-Of-Lock Condition.	23
4.1.4	Preliminary Sample and Hold Circuit Checkout Procedure	24
4.1.5	Detailed VCO Oscillator and Amplifier Checkout	25
4.1.6	Divide-By-N Checkout Procedure	26
4.1.7	Integrator Checkout Procedure	26
4.1.8	Integrator Troubleshooting Procedure	27
4.2	Synthesizer Alignment Procedure	29

TABLE OF CONTENTS (Cont.)

Paragraph		Page
4.2.1	Required Test Equipment	29
4.2.2	API Alignment Procedure	29
4.2.3	100 kHz Sideband Null Adjustment	31
5.	Parts Lists, Component Locations, and Schematic Diagrams	31

LIST OF FIGURES

Figure		Page
1	Synthesizer Simplified Block Diagram	3
2	Synthesizer PWB Assembly Block Diagram	9
3	Simplified Phase Detector and Integrator Waveform	11
4	Down Ramp and API Circuit Simplified Schematic	12
5	VCO Simplified Schematic	15
6	Synthesizer Simplified Divide-By-N Diagram	16
7	Divide-By-N Timing Sequence	17
8	Typical Fractional Divide-By-N.F Timing Sequence	21
9	Integrator Output and Sample Control Waveform Relative Position	25
10	Normal Synthesizer Waveforms	28
11	Synthesizer PWB Assembly Component Locations (10215-4100)	41
12	Synthesizer Assembly A10, Schematic Diagram (10215-4101)	43
13	VCO PWB Assembly A10A1 Component Locations (10215-4120)	55

LIST OF TABLES

Table		Page
1	Typical L.O. and BFO Frequencies	1
2	Synthesizer Interface PWB Connector Assignments	1
3	Fractional Divide-by-N Example	4
4	Synthesizer PWB Assembly A10 Parts List (10215-4100)	32
5	Synthesizer VCO PWB Assembly A10A1 Parts List (10215-4120)	53

A10 SYNTHESIZER ASSEMBLY

1. INTRODUCTION

The Synthesizer Assembly A10 along with the VCO Assembly A10A1, generates the first local oscillator signal. This signal is mixed with the received RF signal on the First Converter Assembly A2 to create the first IF signal. A fractional divide-by-N phase-lock-loop is used to control a VCO that generates the first LO signals between 40.465 MHz and 70.455 MHz. The VCO Assembly A10A1 mounts on A10.

The first L.O. is usually set to generate an IF of 40.455 MHz when subtractively mixed with the received RF signal. In Receivers not equipped for ISB operation or with the A18 Assembly disconnected and equipped with the standard filter configuration, the 1st L.O. is offset slightly when operating in the LSB or AM modes. This is done to position the IF to pass through a filter tuned for the upper sideband. For LSB operation, the BFO is offset by the same amount as the 1st L.O. so the audio can be detected. Table 1 lists the 1st L.O. frequencies for same receive frequency in the USB, LSB, and AM modes to illustrate the offset. The frequency offset scheme is not used when the ISB IF/Audio Assembly A18 is installed.

Table 1. Typical L.O. and BFO Frequencies with A18 Disconnected

Receive Frequency	Mode	Band-width	1st L.O.	BFO Center Frequency
2000.000 kHz	USB	2.7	42.455000 MHz	455.000 kHz
2000.000 kHz	LSB	2.7	42.4516000 MHz	451.600 kHz
2000.000 kHz	AM	3.2	42.453450 MHz	------

The Synthesizer Assembly is mounted on the bottom side of the chassis. LO frequencies are calculated by Control Assembly A14 and sent to the synthesizer in serial data streams. Details of the synthesizer circuit, and technical documentation for the assembly are included in this unit instruction section.

2. INTERFACE CONNECTIONS

All signals sent and received by the Synthesizer Assembly are listed in table 2.

Table 2. Synthesizer Interface PWB Connector Assignments

Connector And Pin	Signal	To/From	Comments
J1-1	DATA	A14J12-1	TTL
J1-2	CLOCK	A14J12-2	TTL
J1-3	PLL LOCK DET	A14J12-6	TTL
J1-4	STROBE	A14J12-5	TTL
J1-5	SERIAL DATA	A14J12-4	TTL
J1-6	KEY	A14J12-3	
J1-7	GND	A14J12-7	

Table 2. Synthesizer Interface PWB Connector Assignments (Cont.)

Connector And Pin	Signal	To/From	Comments
J1-8	SHIELD GND	GND	
J3	1 MHZ REFERENCE	A12	
J4-1	-15 V	A16A3-E10	
J4-2	N/C		
J4-3	+ 5 V REG UNREG	A16A3-E8	
J4-4	KEY		
J4-5	+ 15 V	A16A3-E9	
A1P1	L.O. #1 OUTPUT	A2	40.469 to 70.455 MHz

3. TECHNICAL DESCRIPTION

The technical description of the synthesizer is presented in two parts, a functional description and a detailed circuit description. The functional description describes the overall function of the synthesizer and the theory behind a fractional divide-by-N phase locked loop. The second section describes the actual operation of the synthesizer circuit including observable waveforms and signals.

3.1 Functional Description

3.1.1 General Information

Synthesizer Assembly A10 generates the first local oscillator (1st LO) signal of 40.469,000 to 70.454,999 MHz. The 1st LO is used to convert a received signal between 14 kHz and 29.999,999 MHz to an IF frequency of 40.455 MHz. The 1st LO is generated in a single phase-lock-loop circuit using a fractional divide-by-N technique. Translation of the receive frequency displayed on the front panel into synthesizer frequency information is accomplished on the Control PWB A14. Synthesizer frequency resolution is possible to the 0.1 Hz level (example, 1st LO = 56,469,341.7 Hz), however, 1 Hz resolution is used in all demodulation modes of the receiver.

3.1.2 Description of Fractional Divide-by-N Phase Lock Loop

A simplified block diagram of synthesizer operation is shown in figure 1. The major elements of the phase lock loop (PLL) are the phase detector, voltage controlled oscillator (VCO), and the divide-by-N.F circuit. As in all conventional indirect synthesizers, a divided sample of the VCO output is compared to a reference to yield a control voltage. The control voltage is adjusted by the circuit so that the frequency of the VCO signal is equal to the divide ratio times the reference frequency. For example, if the reference is 100 kHz and the divide-by-N is 519, the VCO frequency is 51.9 MHz. The frequency resolution of the PLL is 100 kHz since the divide-by-N can only be an integer. A fractional divide-by-N PLL can generate a frequency with a resolution much greater than the PLL phase detector reference frequency. As in a standard PLL, the VCO output frequency is R_{ref} x divide-by-N.F (number fraction). A digital phase accumulator in conjunction with an analog compensation circuit enable the synthesizer to resolve step sizes that are a fraction of the reference frequency. For example, a reference of 100 kHz and a N.F of 519.3754 results in a VCO frequency of 51.93754 MHz.

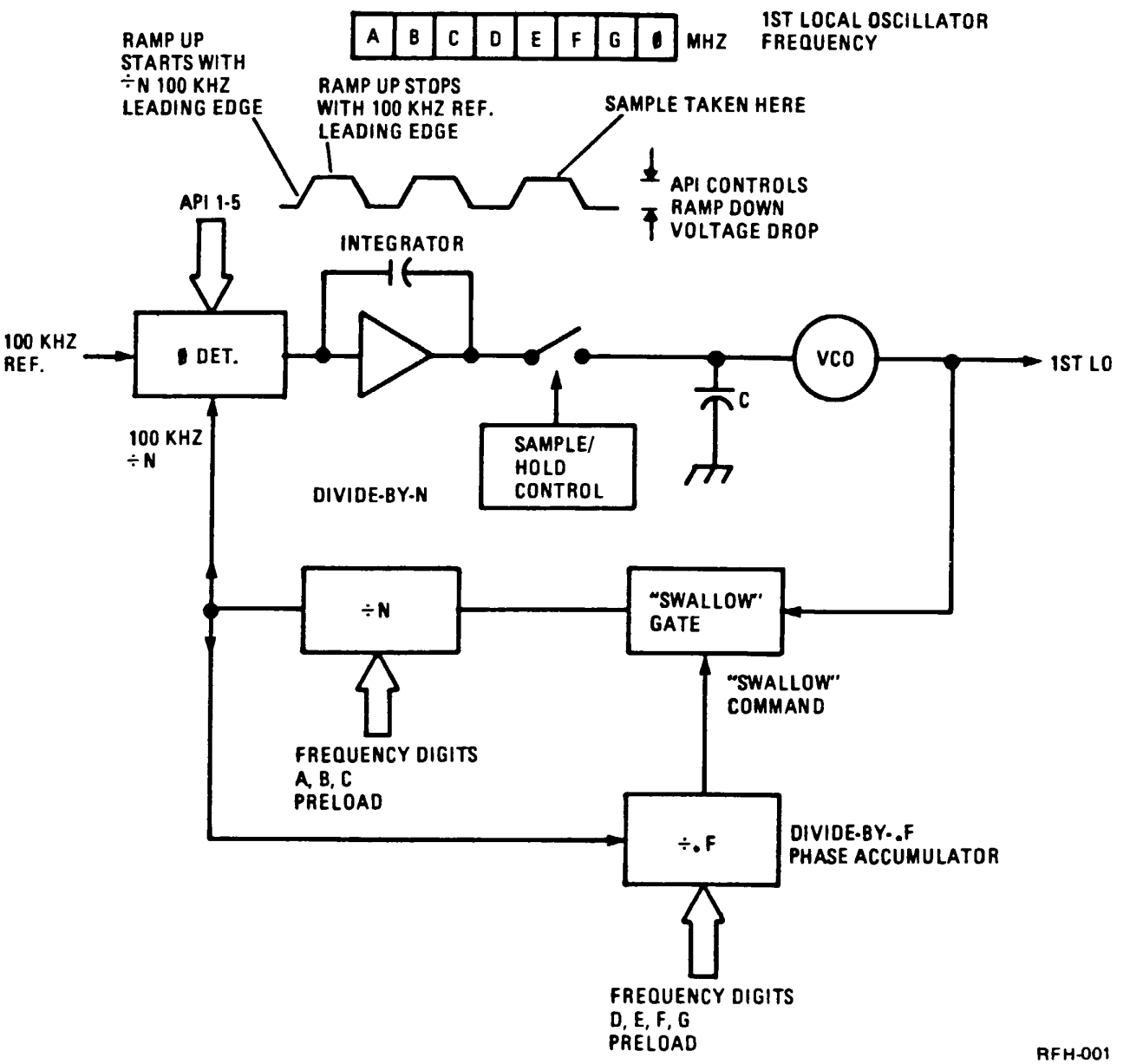


Figure 1. Synthesizer Simplified Block Diagram

3.1.2.2 Example of Divide-By-N.F.

The following will clarify the operation of a fractional divide-by-N PLL. The example operating characteristics are:

- Reference Frequency 100 kHz
- N.F. Characteristic 519.375
- VCO Output frequency 51.9375 MHz (Ref. Freq. x N.F. = VCO)
- Fractional Characteristic 375 (.375 x 360 degrees = 135 degrees)

NOTES

The fractional characteristic should be considered in fractions of a VCO cycle rather than in degrees of a VCO cycle, i.e., .375 of phase accumulation rate rather than 135 degrees of accumulation.

For all modes of operation, the 1st LO is equal to the operating frequency plus 40.455 MHz. Therefore, for this example, the receiver would be operating at a frequency of 11.4825 MHz.

Table 3 summarizes the activity of the fractional divide-by-N circuit through ten divide cycles. The individual steps are described in the paragraphs following the table.

Table 3. Fractional Divide-by-N Example

Divide Out	VCO Pulses In	Swallow?	Phase Accumulation
1st	519	No	.375 (0.00 + .375)
2nd	519	No	.750 (.375 + .375)
3rd	520	Yes	1.125 (.750 + .375-1.0 = .125)
4th	519	No	.500 (.125 + .375)
5th	519	No	.875 (.500 + .375)
6th	520	Yes	1.250 (.875 + .375-1.0 = .250)
7th	519	No	.625 (.250 + .375)
8th	520	Yes	1.000 (.625 + .375-1.0 = 0.00)
9th	519	No	.375 (0.00 + .375)
10th	519	No	.750 (.375 + .375)

3.1.2.2.1 Step 1

The first 519 input VCO sample pulses are divided by 519, resulting in one output pulse from the divide-by-N. The divide-by-N output pulse loads .375 (representing the .F fraction of a VCO cycle) into the phase accumulator, which was empty when the process began.

3.1.2.2.2 Step 2

The next 519 input VCO sample pulses are divided by 519, resulting in a second output pulse from the divide-by-N. A second .375 VCO cycle is loaded into the phase accumulator, which now has accumulated a total of .750 VCO cycle.

3.1.2.2.3 Step 3

The next 519 input VCO sample pulses are divided by 519, resulting in a third output pulse from the divide-by-N. A third .375 is loaded into the phase accumulator, which now overflows with a total of 1.125 VCO cycle. This means the phase accumulator has accumulated a complete VCO cycle plus a remainder. To reduce this phase accumulation by 1.00 VCO cycle, a VCO pulse is subtracted from the divide-by-N input, i.e., a VCO pulse is "swallowed", and the phase accumulation drops to .125. Including the deleted pulse, 520 input VCO sample pulses were received during this divide cycle.

3.1.2.2.4 Step 4

The next 519 input VCO sample pulses are divided by 519, resulting in a fourth output pulse from the divide-by-N. A fourth .375 VCO cycle is loaded into the phase accumulator, which now has a total of .500 VCO cycle.

3.1.2.2.5 Step 5

The next 519 input VCO sample pulses are divided by 519, resulting in a fifth output pulse from the divide-by-N. A fifth .375 VCO cycle is loaded into the phase accumulator which now has a total of .875 VCO cycle.

3.1.2.2.6 Step 6

The next 519 input VCO sample pulses are divided by 519, resulting in a sixth output pulse from the divide-by-N. A sixth .375 VCO cycle is loaded into the phase accumulator which now overflows with a total of 1.25 VCO cycle. The overflow causes the accumulator to subtract 1.00 VCO cycle by swallowing the next VCO pulse, leaving a remainder of .250 VCO cycle. Including the deleted pulse, 520 input VCO sample pulses were received during this divide cycle.

3.1.2.2.7 Step 7

The next 519 input VCO sample pulses are divided by 519, resulting in a seventh output pulse from the divide-by-N. A seventh .375 VCO cycle is loaded into the phase accumulator which now has a total of .625 VCO cycle.

3.1.2.2.8 Step 8

The next 519 input VCO sample pulses are divided by 519, resulting in an eighth output pulse from the divide-by-N. An eighth .375 VCO cycle is loaded into the phase accumulator which overflows with a total of 1.00 VCO cycle. The overflow causes the next VCO pulse to be swallowed and the phase accumulator is empty with 0.00 VCO cycle. Including the deleted pulse, a total of 520 input VCO sample pulses were received during this divide cycle.

3.1.2.2.9 Step 9

With the accumulator empty, the cycle now repeats for each eight divide-by-N output pulses. To calculate the average divide number for this example:

Total VCO pulses: 519 + 519 + 520 + 519 + 519 + 520 + 519 + 520 = 4155

Divider output pulses: 8

Average divider characteristic 4155/8 = 519.375

VCO Frequency = Reference Frequency x divider characteristic
= 100 kHz x 519.375
= 51.9375 MHz, the desired VCO frequency

3.1.2.3 Analog Phase Interpolation (API) and VCO Control Voltage

The divide-by-N.F technique just described requires some refinement since the VCO must operate at an exact frequency, not an average frequency. This requires a steady control voltage.

The primary refinement is made in the VCO control circuitry. Without correction, the accumulating phase error and VCO pulse swallowing would cause spurious VCO frequency outputs due to changes in the control voltage. The correction is provided by the Analog Phase Interpolation (API) circuit.

The API anticipates a pulse deletion and makes corrections to the integrator output so that large error signals are not transmitted to the VCO. When the divide-by-N produces an output pulse, the phase detector current is turned on, causing the integrator, essentially a capacitor, to charge and its output to ramp up. The current source to the capacitor is turned off by the leading edge of a 100-kHz reference pulse and the ramp levels off. Therefore, the level of the integrator output is proportional to the phase difference between the 100-kHz from the divide-by-N and the 100-kHz reference. The ramp voltage level is sampled on each reference cycle, retained by the sample-and-hold circuit, and passed on to the VCO. Following the sampling, a fixed bias signal turns on a bias current, which causes the integrator output to slope down as the capacitor is discharged.

When the N.F includes a fractional element, the VCO operates at a frequency somewhat higher than the frequency indicated by the divide-by-N indicates. In the example, the divide-by-N is 519, indicating a VCO frequency of 51.9 MHz, where the actual VCO frequency due to the .F fraction is 51.9375 MHz. The fractional part of the VCO frequency results in an advancing phase error that causes the integrator to ramp up to a higher output level on each succeeding reference cycle, as the phase difference accumulates. The API prevents this by controlling the discharge of the integrator so the signal drops below the previous starting level for each succeeding cycle in anticipation of the advancing phase error. In this way, the integrator always ramps up to the same level. The sample is taken at the same level each time, and the VCO control voltage is steady at the exact level required to obtain the correct VCO frequency.

The ramp-down current is controlled by five API switches, which are in turn controlled by the phase accumulator. Each time the divide-by-N produces an output pulse, the phase accumulator is incremented with the phase characteristic (.375 VCO cycle in the example above). The number stored in the phase accumulator at any time corresponds to the accumulated phase difference. The 100-kHz divide-by-N sample pulses occur sooner and sooner with reference to the 100-kHz reference pulse. The correction is obtained by converting the number held in the phase accumulator into five data bits, each of which controls an API current switch. The switches are turned on in combinations that correspond to the numerical value of the phase accumulation, with API1 representing the most significant digit and API5 the least significant digit. Each API switch represents a current. API1 represents ten times as much current as API2, and API2 represents ten times as much as API3, etc.

3.2 Detailed Circuit Operation

Figure 2 is a block diagram of the synthesizer circuit. The circuit has been broken into sections for the purpose of discussion. The following paragraphs describe data reception and processing, phase comparator operation, the fractional Divide-by-N circuit, the VCO, and the Analog Phase Interpolator (API) process.

3.2.1 Data Inputs

Frequency information is received from the Control Assembly A14 as a serial data stream. The data is buffered by U3 and clocked into the logic array U5 and shift registers U6 and U13. The 40 bits of data are latched into the shift registers on the falling edge of the strobe pulse received from the Control PWB. The data consists of nine decades of BCD data, and four control bits. The six BCD decades corresponding to the fractional steps, .1 Hz, 1 Hz, 10 Hz, 100 Hz, 1 kHz, and 10 kHz are shifted into the fractional N logic array U5. The remaining three BCD digits and the four control bits are shifted into U6 and U13. This portion of the data word makes up the load for the integer divider (100 kHz, 1 MHz, and 10 MHz steps) as well as the VCO band and the loop filter bandwidth controls.

3.2.2 Phase Detector - General Description

The phase detector is a dual slope, sample-and-hold type as illustrated in figure 3. The major function of the phase detector is to convert a phase difference between the 100 kilohertz reference signal and the 100 kilohertz feedback signal into a control voltage for the VCO. The phase difference is detected by U1A and U1B. The control voltage is developed at integrator capacitor C21 as the maximum voltage of a 100 kHz ramp waveform and can be between -6 and + 6 volts (see figure 3). The control voltage is captured by C24 and C25 in the sample and hold circuit after passing through the loop filter. A steady control voltage is then sent to the VCO.

3.2.3 Phase Detector Up Ramp and Sample

A sequential phase comparator, made up of dual flip-flop U1 and quad NAND gate U2, is used to start and stop the up ramp portion of the sample and hold waveform. The comparator is configured to behave like a single flip-flop that is set by the leading edge of the VCO/N.F sample signal and reset by the leading edge of the 100 kilohertz reference signal. The 100 kilohertz reference signal is divided down from a 1 megahertz input by U18. The VCO sample signal is divided to 100 kilohertz by the divide-by-N.F. network. The sample signal is applied to the clock input of flip-flop U1A. The high going edge of the sample signal sets the flip-flop which turns transistor Q1 off. With Q1 off, Q3 is turned off and Q4 is turned on to bias CR6 off. When CR6 is off a current path from C21 through CR5 and Q29 to a current sink is closed allowing the capacitor to charge. The leading edge of the reference signal clocks U1B and sets it. When U1A and U1B are set, the output of U2A is driven low to reset both flip-flops. This turns Q1 on, which turns Q3 on and Q4 off. This biases CR6 on to turn CR5 off and open the current path for the ramp up. C21 is charged to its maximum value at this point. The capacitor holds the charge until the ramp down portion of the cycle starts. Charge on the capacitor can be monitored at TP2.

3.2.4 Down Ramp and API

During the hold period CR4 and CR5 are biased off so C21 cannot charge or discharge. At the end of the sample period U5 will send out the bias control signal and latch it into U9. The active high signal from the latch is applied to the emitter of Q5 via a resistor network to bias the transistor on. When Q5 is on, Q6 will be biased off. With Q6 off, the potential at the cathode of CR3 is raised from approximately -1 volt to approximately + 1 volt to bias the diode off. With CR3 off, CR4 will conduct current and C21 will start to discharge. The current source for the down ramp is the output of the summing amplifier made up of Q30, Q31 and Q32.

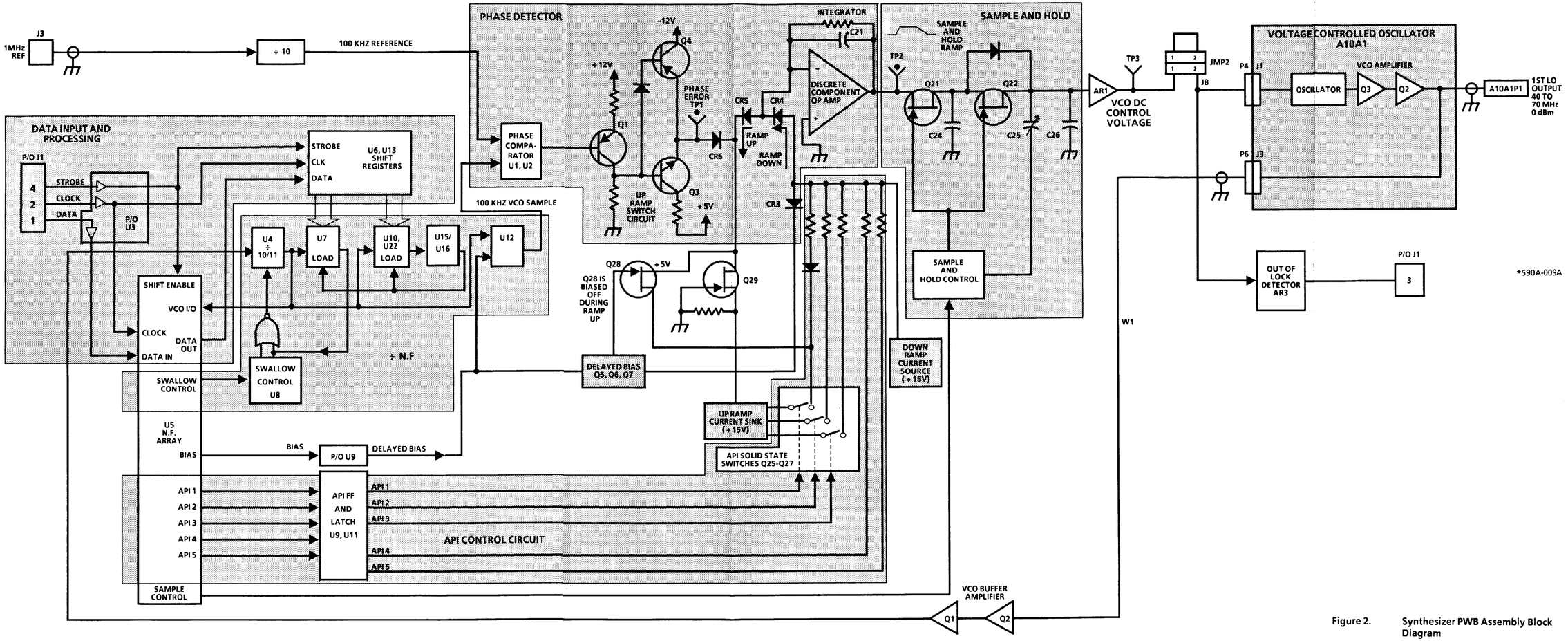
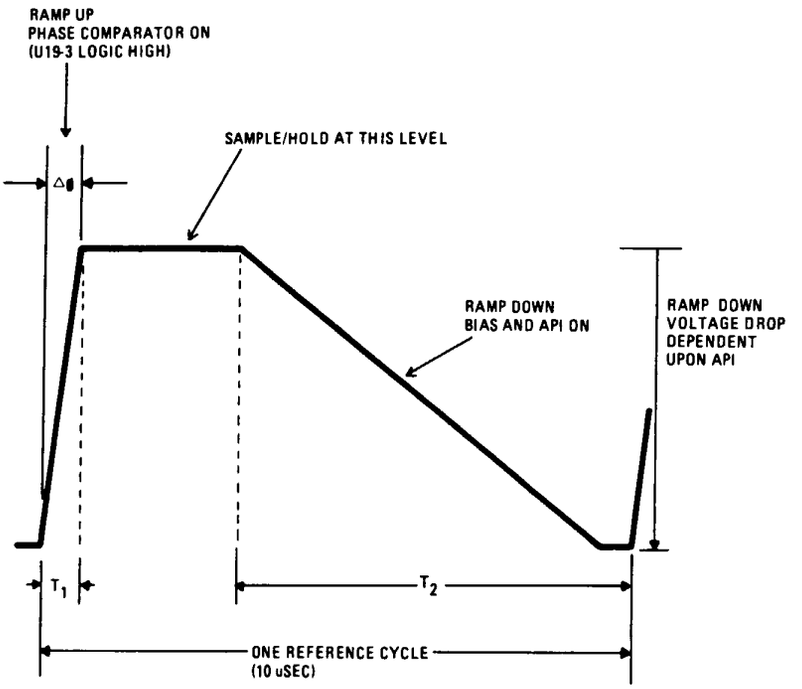
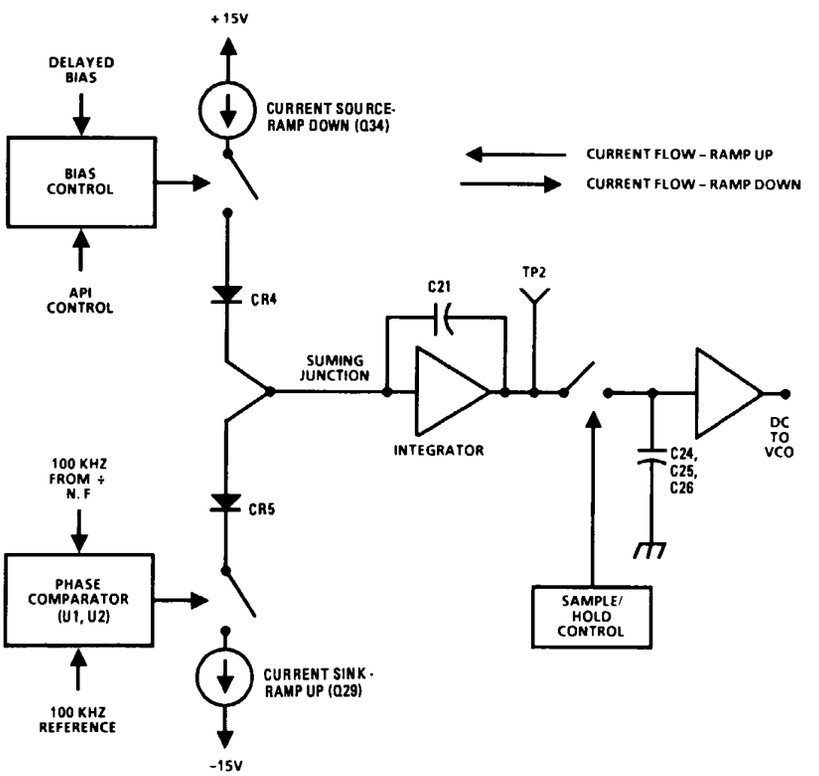


Figure 2. Synthesizer PWB Assembly Block Diagram



T_1 = DEPENDENT UPON Δϕ

T_2 = 13/10 VCO CYCLE TIME



590A-066A

Figure 3. Simplified Phase Detector and Integrator Waveform

The rate of discharge is adjusted by the API circuit to maintain the plateau of the waveform at a constant amplitude. Without it the control voltage would start to rise in response to the accumulating phase error. The API is a set of five decade weighted current sinks that are summed with the down ramp current source to adjust the discharge rate of C21. Part of the API circuit is illustrated in figure 4. The paths to the current sinks are opened and closed by the API control signals. API control signals API 1 through API 5 yield a binary coded decimal representation of the accumulated phase error. The API current paths are graduated by powers of 10 (decade weighted). The current path controlled by API 1 conduct approximately 50 milliamperes which is ten times the current that the API 2 current path can conduct. The API 2 path can conduct ten times the current that the API 3 path can, etc.

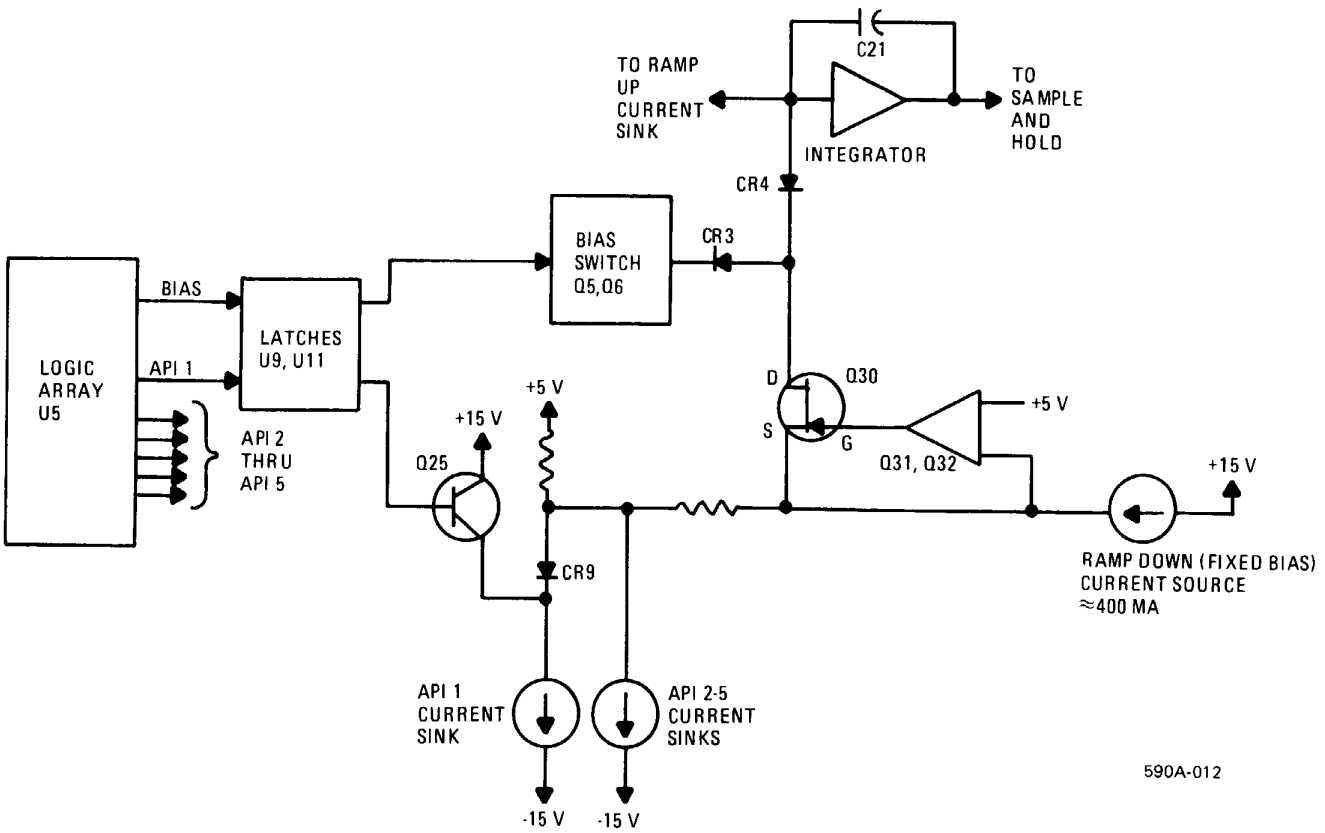


Figure 4. Down Ramp and API Circuit Simplified Schematic

The rate of discharge for C21 decreases as more of the API current sinks are enabled. The rate of discharge is the slowest when all API current paths are closed. As the content of the phase accumulator increases the rate of discharge is increased by selectively opening the API current paths. The API current paths are closed when the corresponding API commands are low. API 1, API 2, and API 3 open and close current paths between the

current source and a common current sink. The API 4 and API 5 current sinks are derived from the logic levels at the output of U9.

The summing amplifier made up of Q30, Q31, and Q32 sums the fixed bias current (400 mA) with the five API current sinks to the ramp down current. Q32 is a differential amplifier that responds to changes in the current level at the junction of the down ramp current source and the API current sinks. The amplifier biases the gate of Q30 so the current supplied to C21 is same as the sum of the current at the drain of Q34 and the API current sinks.

3.2.5 Sample and Hold

Sample and hold FET switches Q21 and Q22 operate simultaneously and are enabled by the control signal SAMPLE/HOLD CONTROL. The integrator plateau is sampled directly by Q21 with the voltage held on capacitor C24. At the same time, the voltage on C24 is sampled by Q22 and stored on capacitor C26. The two-stage sample circuit isolates the integrator from the VCO and reduces ripple in the control voltage. Unity gain buffer amplifier AR1 presents a very high impedance to C26 to prevent discharge during the hold period. The output of the sample and hold circuit is the VCO control voltage and can be monitored at TP3.

3.3 VCO

The VCO is essentially a varactor tuned Colpitts oscillator that uses JFET Q1 as the active element as shown in figure 5. The varactors CR4 through CR11 form the capacitive portion of the oscillator's tank while T1 provides the major portion of the inductive element. The cathodes of varactor diodes CR4 thru CR11 are referenced to a + 8 volt supply to keep them reversed biased over the normal range of the control voltage (approx. -1 to + 5 volts). The oscillator operates in two different bands. The lower band is 40.455 MHz to 55 MHz and the upper band is 55 MHz to 70.455 MHz. The VCO BANDSWITCH signal is used to select the operating band for the VCO. The signal is at a logic low for the lower band and at a logic high level for the upper band. The high logic level turns on Q35 and Q36 to effectively parallel the inductance of the secondary winding of T1 to the tank circuit of the oscillator.

The LOOP FILTER signal is used to switch in additional control voltage filtering at the lower end of the oscillators operating range. The LOOP FILTER signal will be low when the oscillator is operating below 40.500 MHz and high at all other times. When the signal is active, Q4 is turned on to effectively add the network of C19, R14 and C20 to the loop filter circuit.

The oscillator output is picked off the T1 tap and is applied to the gate of Q3. Q3 together with Q2 form casode buffer providing substantial isolation for the VCO output which is sent to the First Converter assembly A2 and is fed back to the divide-by-N.F circuit.

3.4 Divide-By-N.F Circuit

The elements of the divide-by-N circuit are dual modulus prescaler U4 (divide by 10/11); two blocks of programmable dividers, U7, U10 and U22; and LSI fractional N logic array U5. The divide-by.F is processed in the U5 Fractional N Logic Array to keep track of the fractional component in the phase accumulator, and generate the timing for the VCO pulse swallow command. The N programmable dividers are loaded with numeric information from the first three significant digits of the 1st LO frequency, and the .F dividers are loaded with numeric information from the last five significant digits. The 1st LO frequency = RF + 1st IF (40.455 MHz). The receiver operates over an RF frequency range of 14 kHz to 29.999,990 MHz, so that the range of the 1st LO is 40.469 to 70.455 MHz. Therefore, the first three significant digits of the 1st LO range from 404 to 704 for the divide-by-N, and the remaining digits 00000 to 99999 are used for the divide-by-.F.

3.4.1 Divide-By-N

The essential components of the divide-by-N circuit are shown in figure 6. Timing relations of the individual events is illustrated in figure 7. In figure 6, and the following paragraphs the 1st LO digits are in the order ABCDEFG. For example:

	A	B	C	D	E	F	G	H	
1st LO	4	2.	0	5	5	0	0	0	MHz
1st LO	7	0.	4	5	4	9	9	9	MHz

The divide ABC are used int he divide-by-N circuit, and the remaining digits DEFGH are used in the fractional divide-by.F circuit. Operation of the divide-by-N circuit is the same with or without a .F component. The divide-by-N simply considers the ABC digit information and divides accordingly with the dual modulus prescaler and two blocks of programmable dividers.

The U7 divide-by-N programmable block is the "A" counter and is preloaded with the "C" digit and U22 and U10 are the "N" counter and are preloaded with digits A and B respectively. The A counter can be loaded with any number between 0-9, and the "N" divider can be loaded with any number between 40 to 70. During the division cycle, the preloaded dividers (both) count down to "0". When this occurs, the input VCO frequency sample is divided exactly by a number that yields a divider output frequency of 100 kHz. The dual modulus prescaler U4 prescales the VCO frequency and supplies a programmable division characteristic of divide-by-10 or divide-by-11.

At the start of a division cycle, dual modulus prescaler U4 divides by 11. Therefore, for every 11 VCO input pulses, there is 1 dual modulus output pulse. Each dual modulus output pulse counts down the preloaded number in both the "N" and "A" programmable dividers by one. This continues until the "A" counter has counted down to zero, and sends a RIPPLE CARRY OUT (RCO) pulse to the dual modulus prescaler. The RCO pulse disables the "A" divider from further counting, and programs the dual modulus prescaler to now divide by 10, instead of 11. The VCO division continues with each group of 10 VCO input pulses, yielding 1 prescaler output pulse, which counts the "N" programmable divider down one more step toward zero. When the programmable divider "N" reaches zero, a new cycle is started and the entire process is repeated.

An example will clarify the operation of the divide-by-N circuit. The parameters for this example are:

Receiver Mode of Operation: USB
Receiver Frequency of Operation: 11.4450000 MHz

NOTE

A voice mode of operation is selected because the 1st LO is offset in the CW and AFSK modes.

1st LO frequency = RF + 1st IF (40.455 MHz)
= 11.445000 MHz + 40.455 MHz
= 51.90000 MHz

Reference							
A	B.	C	D	E	F	G	H
5	1.	9	0	0	0	0	0 MHz

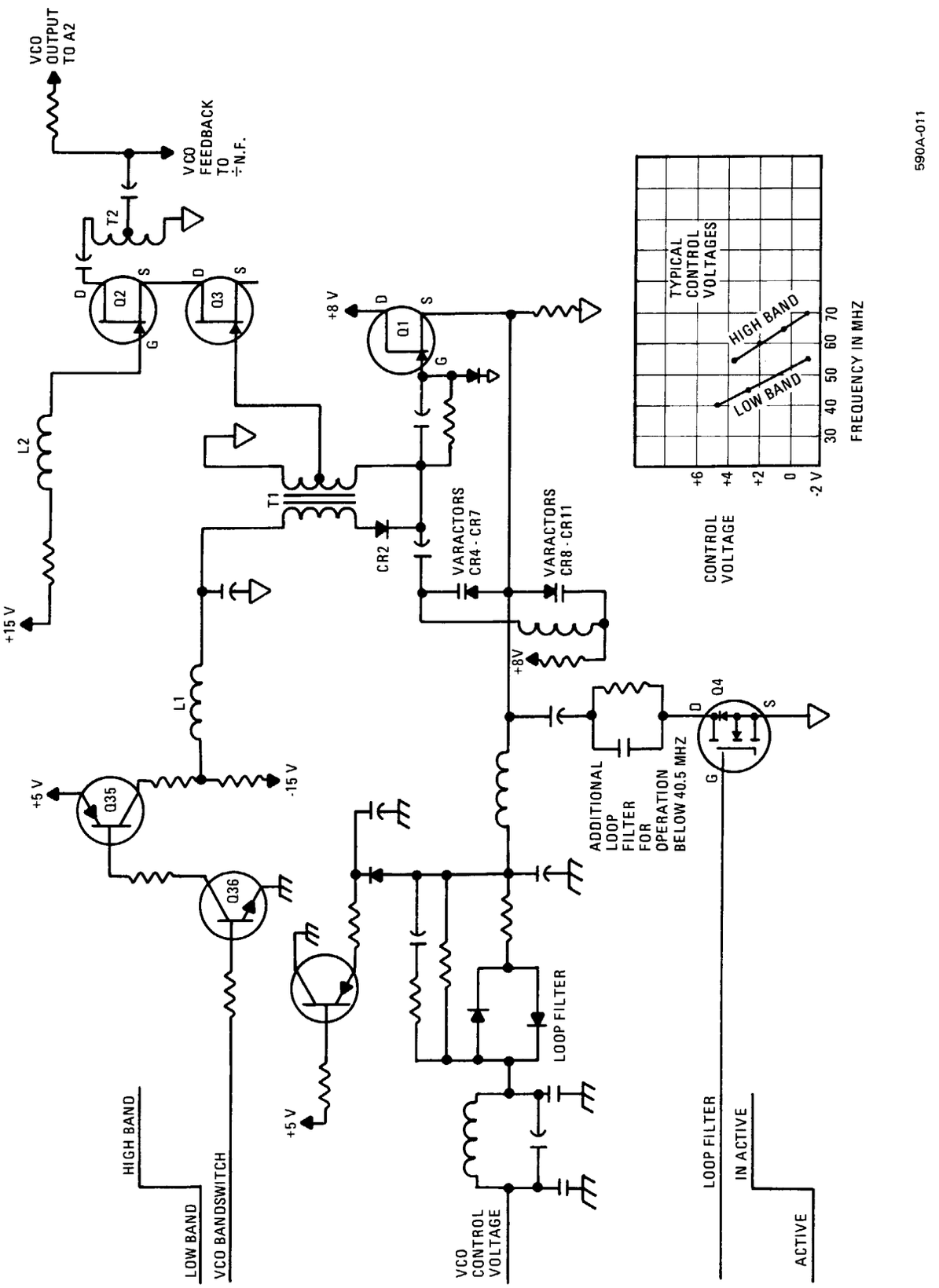


Figure 5. VCO Simplified Schematic

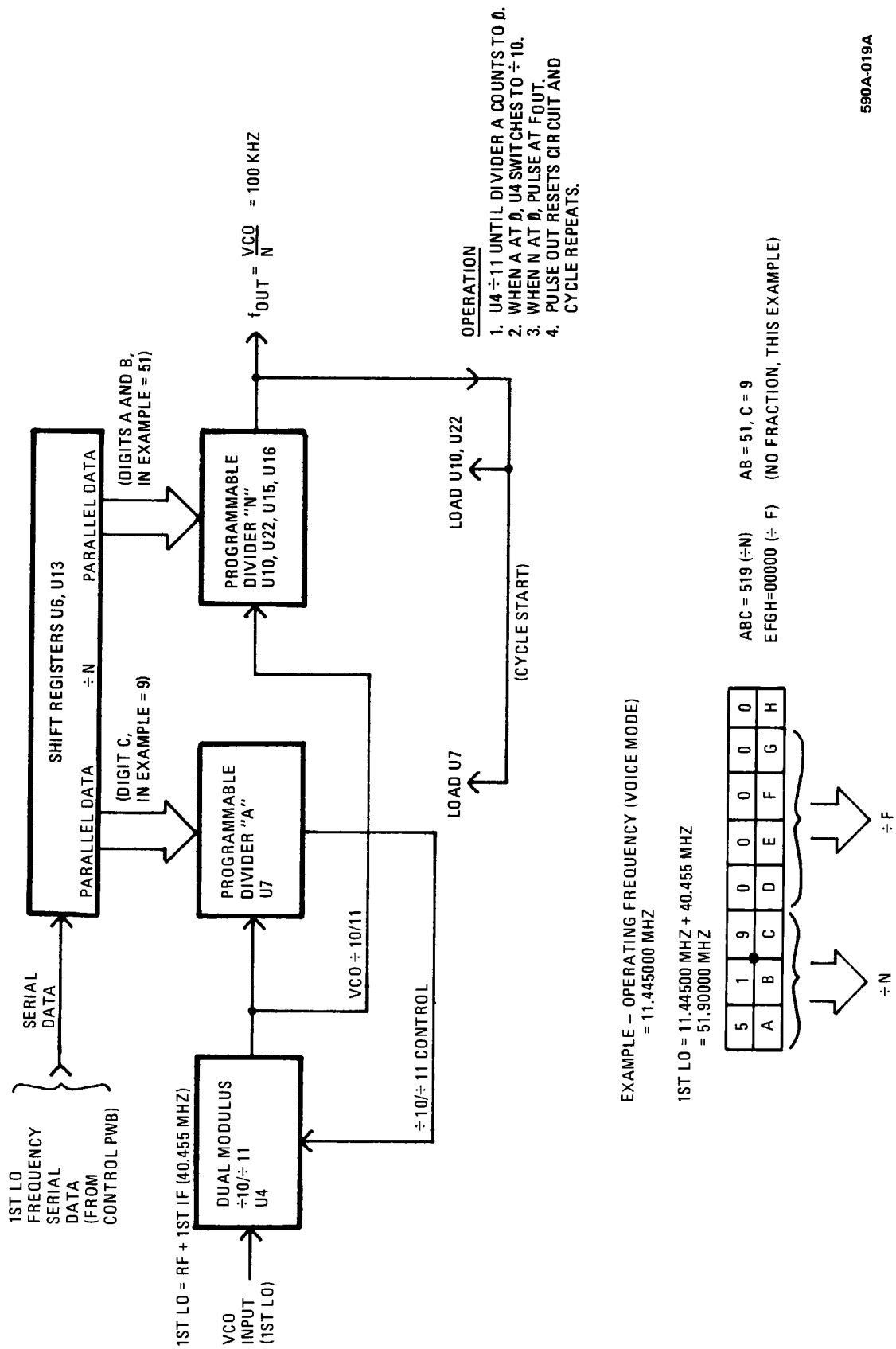


Figure 6. Synthesizer Simplified Divide-By-N Diagram

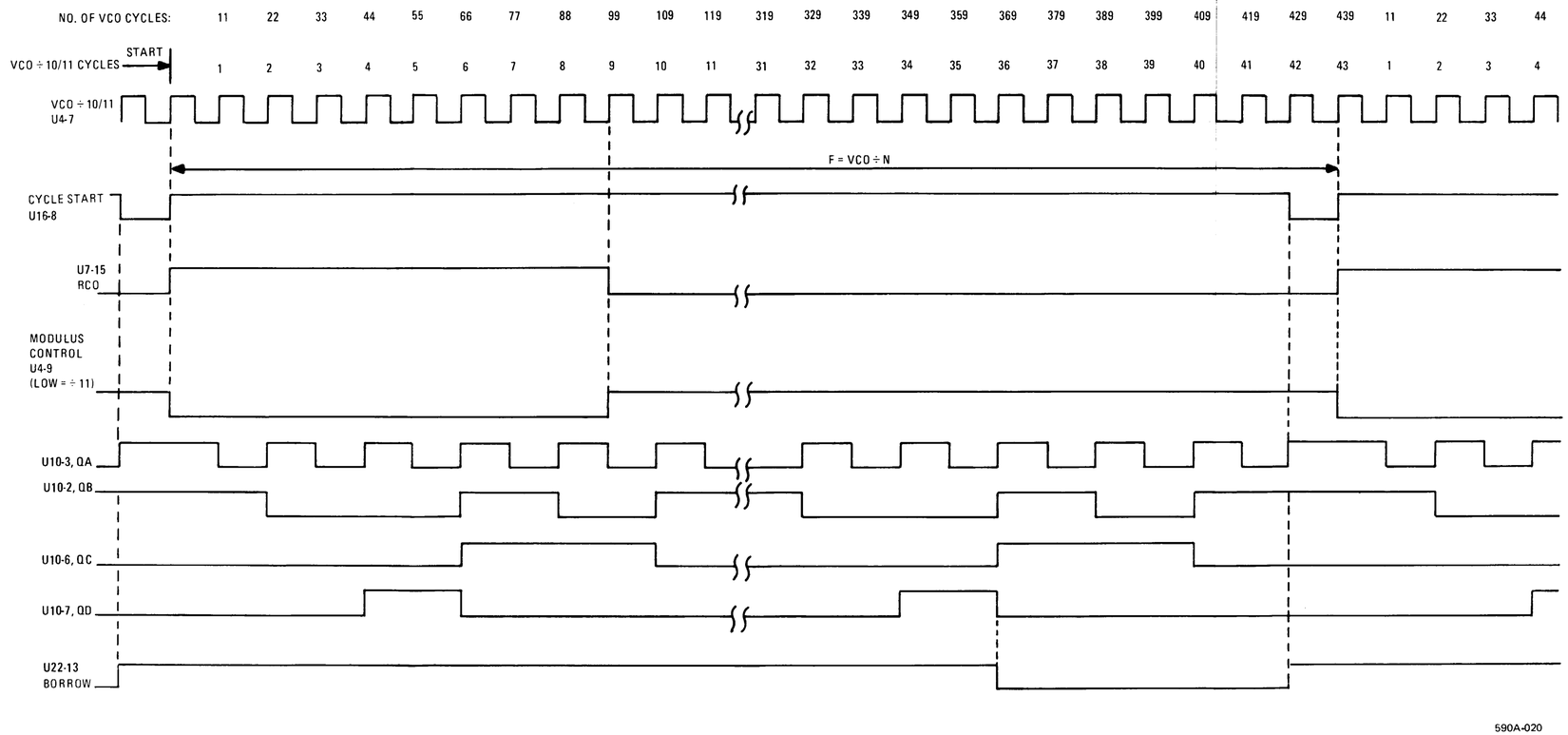


Figure 7. Divide-By-N Timing Sequence

ABC is the divide-by-N portion, i.e., divide-by-519. The divide-by-.F portion, DEFG, is 0000; therefore, there is no fractional (1st LO) of 51.90000 MHz to yield the desired 100-kHz output.

3.4.2 Divide-by-519 Cycle Step One

The receiver operating frequency is 11.445000 MHz. The A14 Control PWB processes this information and writes the corresponding 1st LO frequency of 51.9 MHz into the Synthesizer PWB. The data reception circuits are enabled by a low going strobe.

3.4.3 Divide-by-519 Cycle Step Two

The serial digital data, coded with the 1st LO 51.9 MHz frequency information, is clocked into serial-to-parallel registers U6 and U13 after shifting through by U5. U6 and U13 are strobed and the data appears at the parallel outputs.

3.4.4 Divide-by-519 Cycle Step Three

Between the last divider output pulse and the next VCO pulse, the programmable dividers U7, U10, and U22 are preloaded by a CYCLE START command. The "9" of the divide-by-519 is loaded in the U7 "A" divider, and the "51" of the Divide-by-519 is loaded in the U22, U10 "N" divider.

3.4.5 Divide-by-519 Cycle Step Four

At the start of this (and every) divider cycle, the dual modulus prescaler U4 is programmed for divide by 11. Therefore, after the first 11 input VCO pulses, a prescaler output pulse steps down the A divider from 9 to 8, and the N divider from 51 to 50. In this same manner, after another 88 input VCO pulses, the A divider has stepped to 0, and the N divider has stepped to 42. Overall, 99 input VCO pulses occur in this part of the cycle.

3.4.6 Divide-by-519 Cycle Step Five

When the A divider reaches 0, a U7 RIPPLE CARRY OUT (RCO) pulse from the A divider stops further A divider counting, and causes the dual modulus prescaler to be commanded to divide-by-10 (instead of 11).

3.4.7 Divide-by-519 Cycle Step Six

After another 10 input VCO pulses, the prescaler produces an output pulse, and the N divider steps from 42 to 41. After another 10 input VCO pulses, the A13 divider steps from 41 to 40, and so forth. Overall, the prescaler requires 420 input VCO pulses to step the N divider from 42 to 0.

3.4.8 Divide-by-519 Cycle Step Seven

When the U10/U22 N counter reaches a count of two the "J" input, U16-7, of the flip-flop is taken high so that it changes state with the next clock pulse and a logic low occurs at U16-8. This pulse is used to preload the N dividers and is named CYCLE START. The next rising clock edge from the prescaler loads the A divider (U7), and the divide-by-519 cycle repeats.

3.4.9 Divide-by-519 Cycle Step Eight

The total VCO pulses required for 1 divider output including 99 for the A divider count down, plus 420 for the rest of the N divider count down (total 519). Thus, the circuit operates at the desired divide-by-519.

3.4.10 Divide-by-519 Cycle Step Nine

Although the CYCLE START output operates at 100 kHz, it is not used as the 100-kHz divide-by-N sample. Instead, CYCLE START initiates sequencing in Fractional N Logic Array U5 to generate the API, bias, swallow, sample, and API Latch Clock signals. The 100-kHz sample is derived from processing the bias output of U5, which is converted into a fast-rising pulse by latch U9 and dual flip-flop U12.

3.5 Divide-By-F (Fractional)

The fractional portion of the divide-by-N.F. functions in relation to the divider circuit by deleting or "swallowing" an input VCO pulse. This has the effect of removing 1 cycle, or 360 degrees, of phase accumulation as described in paragraph 3.1.2.2. Timing of the events in a typical divide-by-N.F cycle are illustrated in figure 8. The divide-by-N is unaffected by the action of the divide-by-.F, and the circuits essentially operate independently (except when a pulse is swallowed, then the count is increased by one). Virtually all of the divide-by-.F functions are processed internally to LSI integrated circuit U5. Since a discussion of the internal workings of U5 is beyond the scope of this manual, only the divide-by-.F outputs are considered: API control, bias, and swallow control.

The operation of the API control is discussed in the phase detector circuit description, as is the bias control. The swallow control is interactive with the dual modulus divider used with the Divide-by-N circuit. The dual modulus divider U4 (divide-by-10 or 11) is operating as a divide-by-11 until the preloaded "A" divider under flows by counting down to zero. At that time, the dual modulus is programmed to divide by 10 for the remainder of the divide-by-N cycle. The divide-by-.F VCO pulse swallow occurs by changing the dual modulus divider from divide-by-10, back to divide-by-11 for one VCO pulse, and then back to divide-by-10 again. In this manner, a prescaler output counts down the N divider one step with 11 VCO pulses, instead of 10 VCO pulses, and a VCO pulse is thereby swallowed.

The swallow command is generated during the first 10 cycles of the VCO/10 or 11 output. This means that the A divider counts down from its preload during the same time a swallow command may occur. If the swallow command occurs when the dual modulus divider is already dividing by 11, or if a swallow command occurs at the same time the A divider under flows, the swallow command must be "stored" until the proper time. This is accomplished by using the swallow control flip-flop U8.

4. MAINTENANCE

The Synthesizer Assembly does not require any regular maintenance or adjustments. Paragraph 4.2 outlines a method for testing and troubleshooting a faulty synthesizer assembly.

NOTE

VCO Assembly A10A1 with its attached shieldcan is to be replaced as a unit. Removal of the PWB from the shieldcan is difficult and is not recommended.

4.1 Test Procedure

4.1.1 Required Test Equipment

Equipment required to complete the following test procedure is listed below.

- Digital multimeter
- Spectrum analyzer - HP-8568A or equivalent

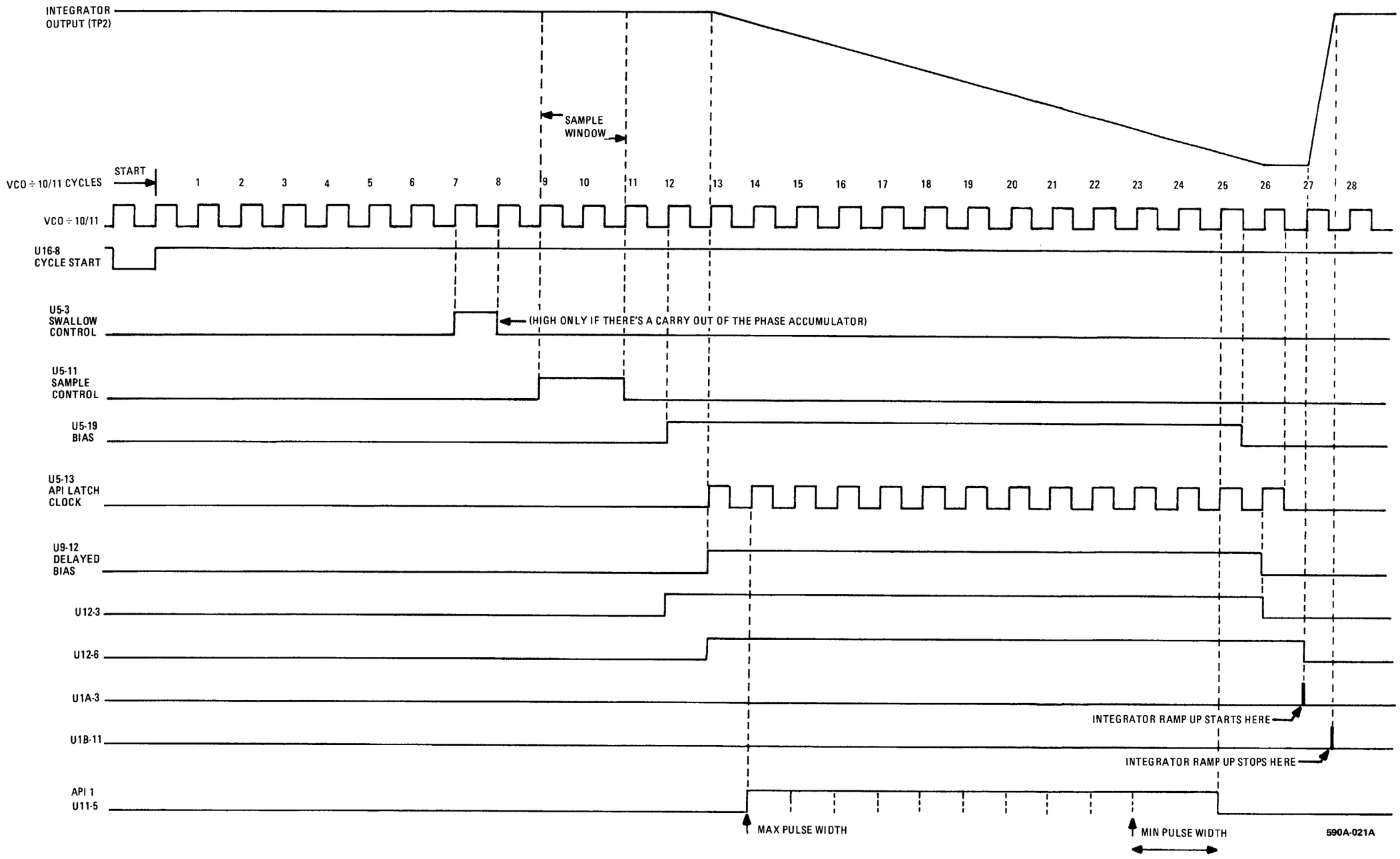


Figure 8. Typical Fractional Divide-By-N.F Timing Sequence

- Oscilloscope - Tektronix 465m or equivalent
- Adjustable dc power supply
- Frequency counter
- SMB to BNC adapter

4.1.2 Preliminary Procedure

a. Position receiver so the synthesizer is exposed and accessible, then power up the receiver.

b. Check the following power supply inputs.

Voltage	Test Point
+ 15 Vdc	L8, L9, or L12
-15 Vdc	L10
+ 5 V Unreg. (9 Vdc)	L11

c. If voltages are not present or are incorrect trace the signals back to the power supply, then correct the problem as required.

d. If the voltages are present and within specified tolerances, place the unit in the TEST mode and run the BITE test.

e. A display of ASSY 10 FAULT 02 indicates that the synthesizer is out-of-lock and the out-of-lock signal on J1-3 is low.

NOTE

The BITE test checks the synthesizer for the out-of-lock condition at 70.455 MHz and 42.455 MHz.

f. Set the receiver to the RCV mode and check the FAULT Indicator. If it is lit, check J1-3 for a logic low that indicates the out-of-lock condition.

4.1.3 Out-Of-Lock Condition

a. Disconnect the coax cable (A10A1P1) from J10 on the chassis. This is the cable that carries the VCO output from A10A1P1. Connect the cable to the input of a spectrum analyzer (HP-8568A or equivalent).

b. Set up the spectrum analyzer so that it will scan from 0 to 110 MHz, and a full vertical display will equal + 10 dBm.

c. On the front panel of the receiver, select the USB demodulation mode, and set the frequency to 1.64500 MHz. This sets the synthesizer to 42.10000 MHz.

d. Monitor TP3 on the Synthesizer Assembly A10 with the oscilloscope (Tektronix 465 or equivalent). If the synthesizer is operating properly the voltage at TP3 should be + 3.7 ± 0.4 Vdc with no ac component.

e. Use the oscilloscope and the spectrum analyzer to check for the following conditions:

1. VCO output less than 35 MHz and a dc voltage greater than + 5 volts at TP3.

   Probable Fault: Reference frequency signal path malfunction.

   Check: for presence of 100 kHz signal at pin 11 of U1. Trace signal back to U18 and correct problem as required.

2. VCO output greater than 42 MHz and a dc voltage greater than + 5 volts at TP3.

   Probable Fault: Bandswitch malfunction.

   Check: Voltage at Q35C, If it measures -15 volts then the VCO is the probable failure, If it measures + 14 volts then Q35, Q36 or U13 maybe the cause.

3. VCO output is greater than 60 MHz and a dc voltage less than -4 volts at TP3.

   Probable Fault: VCO, Sample and Hold circuit, divide-by-N circuit, integrator, or bandswitch malfunction.

   Check: If the out of lock condition only occurs when the front panel frequency is greater than 55 to 60 MHz and the VCO output is less than 70 MHz and the control voltage at TP3 is less than -4 volts then check the voltage at Q35C. If it is -15 volts then Q35, Q36 or U13 may be bad. If this is not the cause, check the other circuits using the following procedures.

4.1.4 Preliminary Sample and Hold Circuit Checkout Procedure

a. Use the dual channel oscilloscope to check the signal at TP2 of the synthesizer assembly and the SAMPLE CONTROL signal at the Q23 collector. The signals will resemble the waveforms shown in figure 9 when the synthesizer is operating properly.

b. The amplitude of the integrator waveform during the high active period of the SAMPLE CONTROL signal should be the same as the voltage measured at TP3.

c. If no sample pulse is present, monitor pin 11 of U5 with the oscilloscope. The SAMPLE CONTROL signal at this pin should be a series of positive-going pulses 280 to 500 nanoseconds wide, with a frequency of 100 kHz, when the synthesizer is in lock.

d. If the SAMPLE CONTROL signal monitored in step c is good, one or more of transistors Q17 thru Q24 or AR1 may be defective.

e. If the voltage at TP2 and TP3 measures 11.5 volts or greater or less than -6 volts, the sample and hold circuit is probably operating properly.

f. Under some circumstances the signal at TP3 may be an ac waveform. If this is the case, slow the sweep on the oscilloscope and compare the waveforms on TP2 and TP3. If the two correspond this is an indication that the sample and hold circuit is working.

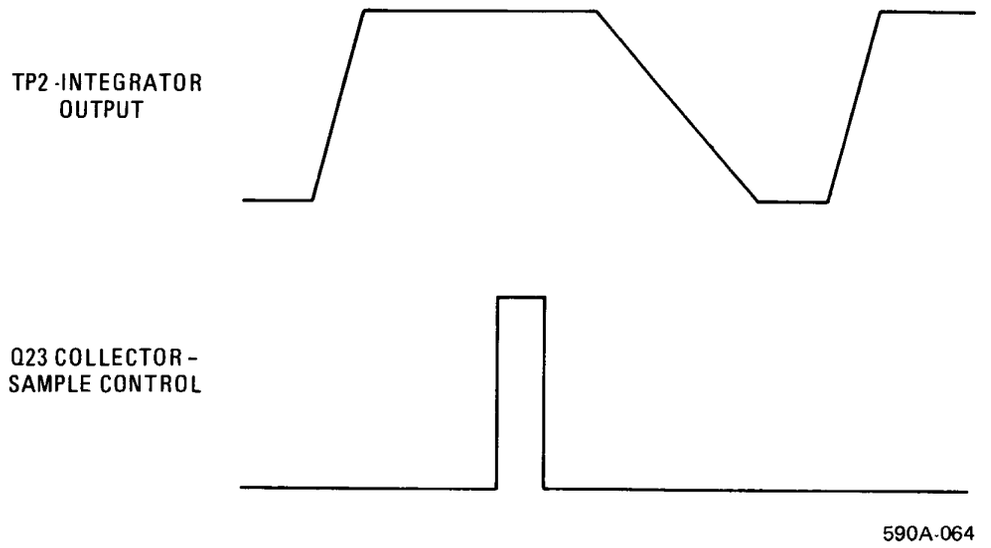


Figure 9. Integrator Output and Sample Control Waveform Relative Position

g. Check the voltage at pin 3 of AR1. It should be the same as the voltage measured at pin 6 of AR1 and TP3.

h. Check the voltage at pin 2 of AR1. It should be the same as the readings taken in step e.

4.1.5 Detailed VCO Oscillator and Amplifier Checkout

a. Remove jumper plug JMP2 on the synthesizer assembly.

b. Disconnect VCO output cable P1 from J5 on the First Converter Assembly A2. Use an SMB-to-BNC adapter and connect the cable to the input of a frequency counter.

c. Connect the positive (+) lead of a dc power supply to JMP2-2, and the negative (-) lead to ground.

d. Adjust the power supply to 4.5 (3.6 V) High band) Vdc. The frequency of the VCO outputs should measure 40 ± 1 Low Band (55 ± 1) High Band MHz, and the signal at J5 should measure 0 ± 2 dBm.

e. Reverse the polarity of the power supply leads.

f. Adjust the power supply for an output of -1.4 Vdc. The frequency of the VCO output should now measure 55 (73 MHz) High Band) MHz, and the signal at J5 should be 50 mV_{rms} or greater.

g. Disconnect the RF Voltmeter.

h. Disconnect the VCO output cable from the frequency counter and connect it to the Spectrum Analyzer.

j. Vary the dc supply voltage from -2 to + 5 Vdc and observe the RF voltmeter. The VCO output signal should measure between 0 dBm ± 2 dB as the supply voltage is varied.

4.1.6 Divide-By-N Checkout Procedure

a. Remove jumper plug JMP2 on the Synthesizer Assembly.

b. Connect Dc supply to pin 2.

c. Connect Frequency Counter to VCO output cable.

d. Adjust Dc supply for 0 frequency of 42.1 MHz ± .1 MHz.

e. Connect a 14-pin DIP to U1.

f. Connect a X10 oscilloscope probe to the 1-megohm input of a frequency counter.

g. Measure the frequency at U1 pin 3.

- U1-3
- U11-5
- U9-2
- U9-7
- U9-10
- U9-12

The frequency at this point should measure 100.0 kHz.

h. Use the oscilloscope to monitor the U1 pin 3. This should should be a series of pulses, with a frequency of 100 kHz.

4.1.7 Integrator Checkout Procedure

a. Set up a Tektronix 465 m oscilloscope (or equivalent for two channel operation.

b. On the oscilloscope, monitor TP2 with channel 1.

c. Monitor the DELAYED BIAS signal at the cathode of CR3 with channel 2 of the oscilloscope. (Refer to figure 10)

d. Compare the signals. The start of the ramp down of the signal on channel one should coincide with the high-going edge of the DELAYED BIAS pulse on channel 2.

4.1.8 Integrator Troubleshooting Procedure

a. If the integrator output measured at TP2 is a steady dc voltage greater than 11.5 volts indicating that the integrator does not ramp down proceed with step b. If the signal at TP2 is a steady dc voltage less than -11.5 volts, go to step g.

b. If the DELAYED BIAS signal at the cathode of CR12 does not go high as shown in figure 10, the delayed bias circuit is suspect. Check the following points to isolate the faulty signal:

Pin	Signal
U9-12	DELAYED BIAS
U9-13	BIAS (one clock pulse ahead of DELAYED BIAS)
U5-91	BIAS
U5-2	CYCLE START (100 kHz)
U5-8	VCO FREQUENCY/10

c. If the signals at U5-2 and U5-8 are good, but the BIAS signal at U5-9 is bad, check the following pins for proper supply voltages:

Pin	Voltage
U5-24	+ 5 Vdc
U5-12	0 Vdc

d. Check that the RESET at U5-17 is high.

e. If the voltages and the reset are good while U5-19 is bad, replace U5.

f. Check the ramp down current source at the following points;

Monitor Point	Normal Signal
Q30-Drain	See Figure 10
Q30-Source	+ 5.0 ± 0.25 Vdc
Q34-Source	+ 8.8 ± 0.2 Vdc

If the signals at the three points listed above are good, then the discrete component op amp may be faulty.

NOTE

Follow steps g through p only if the signal at TP2 is a steady dc voltage less than 11.5 volts.

g. Set up the oscilloscope for two channel operation. Monitor TP2 with channel 1, and TP1 with channel 2. Observe the relationship between the negative-going pulse at TP1 (the pulse should drop to -1.2 volts) and the rising edge of the pulse at TP2 (ramp up). The ramp-up should start when the pulse at TP1 goes low, as shown in figure 10.

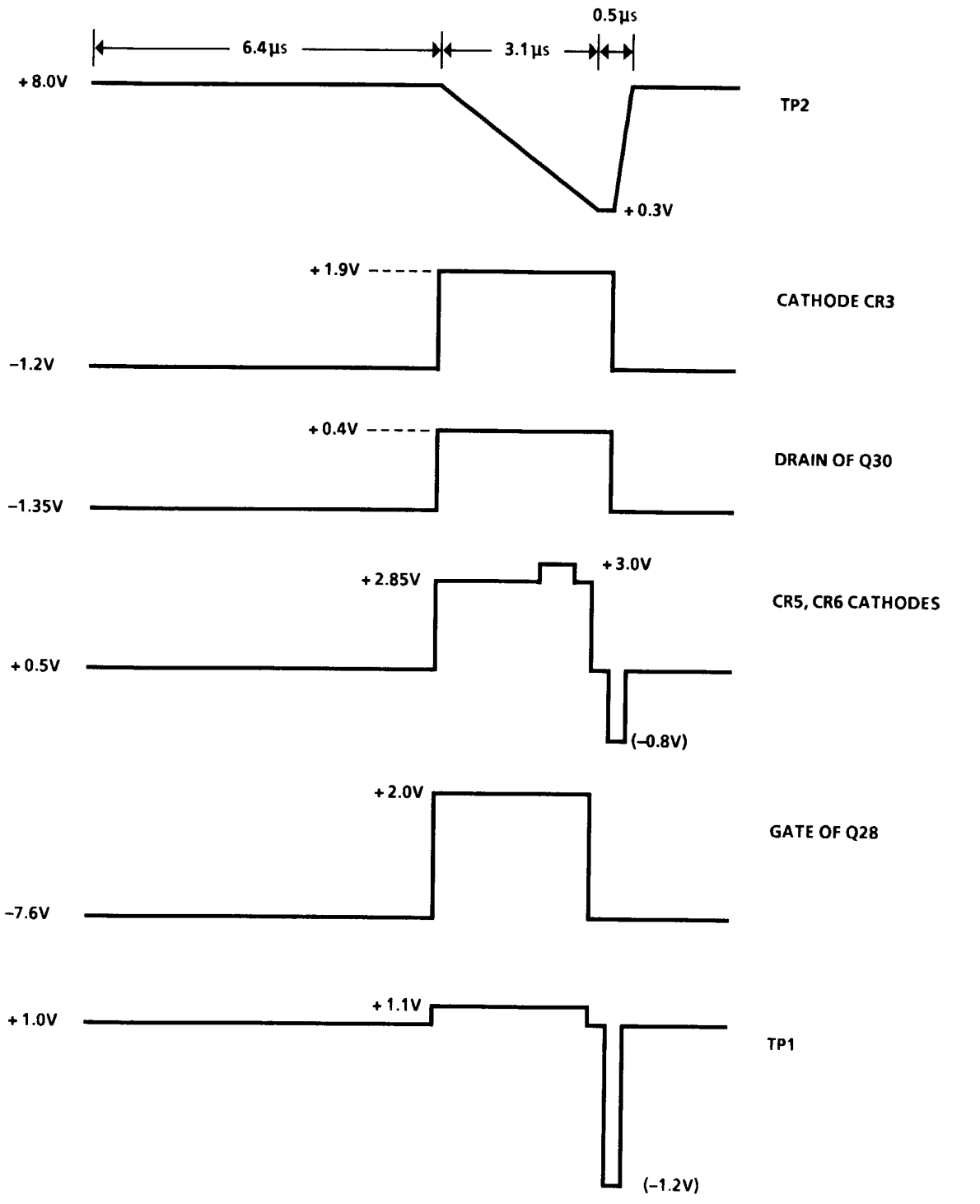


Figure 10. Normal Synthesizer Waveforms

h. If the negative-going pulse on TP1 is absent or does not drop to -1.2 Vdc, then the phase comparator U19, or the components between U19 and CR3 may be causing the fault. Verify the following inputs and outputs of U19.

Pin	Normal Signal
U1-5	100 kHz (output)
U1-6	100 kHz (output)
U1-3	100 kHz (input)
U1-11	100 kHz (input)
U1-14	+ 5 Vdc (supply input)
U1-7	0 Vdc (supply ground)
U2-3	100 kHz Narrow pulser

i. If the outputs of U1 are bad, but the inputs are good, replace U1 or U2. If all inputs and outputs of U1 are good proceed with step j.

j. If the signal at TP1 appears to be good but the signal at TP3 does not rise as shown in figure 10, then continue to monitor TP2 with channel 1 of the oscilloscope, and monitor the junction of the cathodes of CR5 and CR6 with the other channel. The normal waveforms are shown in figure 10.

k. If the signal at the cathodes of CR5 and CR6 is good (appears as illustrated in figure 10) then the ramp up current sink circuit may be faulty.

l. Monitor the gate of Q28 (case). This is the DELAYED BIAS signal and it must be low to bias Q28 off during ramp up.

m. If the gate of Q28 is high, trace the DELAYED BIAS signal back from the collector of Q7 to U9-19 to isolate the faulty component.

n. If the signal at the gate of Q28 is good, check the gate of Q29 (case) for the presence of a steady 6.2 Vdc signal, with no ac component.

o. If the signal at the gate of Q29 is good, check U24-15 for the presence of a -8.8 V signal with no ac component.

p. If the ramp-up current sink circuit checks out, the discrete component op amp is probably faulty.

4.2 Synthesizer Alignment Procedure

4.2.1 Required Test Equipment

- SMB to BNC adapter
- Spectrum analyzer HP-8568A or equivalent

4.2.2 API Alignment Procedure

a. On the Receivers front panel select the USB mode and set the frequency to 19.54800 MHz.

b. Disconnect the synthesizer output cable from the chassis bulk head in the adjoining compartment, and use the SMB to BNC adapter to connect it to the RF input of the spectrum analyzer.

c. Set the spectrum analyzer for the following parameters.

- Input Attenuation: 10 dB
- Center Frequency: 60 MHz
- Scan Width: 1.0 kHz per division
- Resolution Bandwidth: 300 Hz
- Scan Time Per Division: 2 milliseconds
- Log Reference Level: + 10 dBm
- Scan Trigger: Auto
- Scan Mode: Int
- Video Filter: 100 Hz
- Log/Linear: 10 dB log

d. With the spectrum analyzer set to a center frequency of 60 MHz the API sidebands will appear on the display for the following 4 adjustment steps, the sideband to be adjusted will always be 3 kHz from the desired output.

e. The spectrum analyzer display should now be centered on the API sideband, 3kHz below the synthesizer output. Adjust the trim pot R90 on A10 to reduce the API sideband level to a minimum. The signal level should be at least 65 dB below the level of the synthesizer output signal. Normally the sideband level can be adjusted to 70 to 75 dB below the synthesizer output.

f. On the front panel of the receiver change the frequency to 19.54530 MHz. Adjust trim pot R92 on A10 to reduce the sideband signal level to a minimum. The signal level should be at least 65 dB below the level of the synthesizer output signal. Normally the sideband signal level can be adjusted so that it is at least 75 dB below the output signal level.

g. Set the front panel frequency to 19.54503 MHz. Adjust R159 on A10 to reduce the sideband level to a minimum. The sideband level should be at least 65 dB below the output and can usually be adjusted so that it is at least 75 dB below the output level.

h. Set the front panel frequency to 19.545003 MHz. Adjust R93 to reduce the sideband level to a minimum. The signal level should be at least 65 dB below the synthesizer output and can typically be adjusted to be at least 75 dB below the output signal level.

4.2.3 100 kHz Sideband Null Adjustment

a. Select the following parameters on the receivers front panel.

- Frequency: 00.099 MHz (99 kHz)
- Mode: USB
- AGC: OFF
- BFO: 000

b. Adjust the RF Gain to produce a signal 30 dB above the noise floor or as close to 30 dB above the floor as possible.

c. Connect the spectrum analyzer to the IF monitor output and set it up as follows.

- Center Frequency: 453.5 kHz
- Resolution Bandwidth: 100 Hz
- Video Bandwidth: 30 Hz
- Span: 5 kHz
- Reference Level + 20 dBm (TBV)

d. While observing the output level and listening to the tone in the speaker, adjust C25 on the synthesizer for minimum amplitude. Increase the RF GAIN as needed to resolve the null. The tone should be no more than 10 dB above the noise floor and typically can be reduced to the noise level so that the tone becomes inaudible.

5. PARTS LISTS, COMPONENT LOCATIONS, AND SCHEMATIC DIAGRAMS

All replaceable components of Synthesizer Assembly A10 are listed in table 4, and their locations are shown in figure 11. The circuits of the synthesizer and VCO assemblies are shown schematically in figure 12. Components of VCO Assembly, A10A1 are listed in table 5, and their locations are shown in figure 13.

Table 4. Synthesizer PWB Assembly A10 Parts List (10215-4100, Rev. G)

Ref. Desig.	Part Number	Description
--	10215-4120	ASSY VCO PWB
AR1	I30-0035-000	IC OP AMP QUAD 072
AR2	I30-0035-000	IC OP AMP QUAD 072
AR3	I20-0010-000	IC LM2903 COMPARATOR PL
C1	M39014/02-1310	CAP .1UF 10% 100V CER-R
C2	M39014/02-1310	CAP .1UF 10% 100V CER-R
C3	M39014/02-1310	CAP .1UF 10% 100V CER-R
C4	M39014/02-1310	CAP .1UF 10% 100V CER-R
C6	M39014/02-1310	CAP .1UF 10% 100V CER-R
C8	C26-0025-220	CAP 22UF 20% 25V TANT
C9	C26-0050-109	CAP 1.0UF 20% 50V TANT
C10	M39014/02-1310	CAP .1UF 10% 100V CER-R
C11	C26-0025-339	CAP 3.3UF 20% 25V TANT
C12	M39014/02-1310	CAP .1UF 10% 100V CER-R
C13	M39014/02-1320	CAP .47UF 10% 50V CER-R
C14	M39014/02-1320	CAP .47UF 10% 50V CER-R
C15	M39014/02-1298	CAP .01UF 10% 200V CER-R
C16	M39014/02-1310	CAP .1UF 10% 100V CER-R
C17	M39014/02-1320	CAP .47UF 10% 50V CER-R
C18	CK06BX152K	CAP 1500PF 10% 200V CER
C19	CM05CD180J03	CAP 18PF 5% 500V MICA
C20	M39014/02-1298	CAP .01UF 10% 200V CER-R
C21	CM05FD301J03	CAP 300PF 5% 500V MICA
C22	M39014/02-1303	CAP .033UF 10% 100V CER-R
C23	C80-0001-273	CAP .027UF 5% 50V POLYC
C24	CM05FD331J03	CAP 330PF 5% 500V MICA
C25	C85-0001-002	CAP VAR 1-10PF PIST
C26	C-2496	CAP 470PF 2% 500V MICA
C27	C26-0025-220	CAP 22UF 20% 25V TANT
C28	C26-0050-109	CAP 1.0UF 20% 50V TANT
C29	CK05BX100K	CAP 10PF 10% 200V CER
C30	M39014/02-1310	CAP .1UF 10% 100V CER-R
C31	M39014/02-1310	CAP .1UF 10% 100V CER-R
C32	M39014/02-1310	CAP .1UF 10% 100V CER-R
C33	M39014/02-1310	CAP .1UF 10% 100V CER-R
C34	M39014/02-1298	CAP .01UF 10% 200V CER-R
C35	C26-0025-220	CAP 22UF 20% 25V TANT
C36	C80-0001-273	CAP .027UF 5% 50V POLYC
C37	C61-0003-003	CAP 1.0UF 5% 100V POLYE
C38	C80-0008-332	CAP POLYCARB 3300PF 50V
C39	C80-0008-122	CAP POLYCARB 1200PF 50V
C40	C80-0008-123	CAP POLYCARB .012UF 50V
C41	C80-0008-332	CAP POLYCARB 3300PF 50V
C42	C80-0008-123	CAP POLYCARB .012UF 50V
C43	M39014/02-1298	CAP .01UF 10% 200V CER-R
C45	M39014/02-1310	CAP .1UF 10% 100V CER-R
C46	M39014/02-1310	CAP .1UF 10% 100V CER-R
C47	M39014/02-1310	CAP .1UF 10% 100V CER-R

Table 4. Synthesizer PWB Assembly A10 Parts List (10215-4100, Rev. G) (Cont.)

Ref. Desig.	Part Number	Description
C48	M39014/02-1310	CAP .1UF 10% 100V CER-R
C49	CK05BX102K	CAP 1000PF 10% 200V CER
C50	M39014/02-1310	CAP .1UF 10% 100V CER-R
C51	M39014/02-1310	CAP .1UF 10% 100V CER-R
C52	M39014/02-1310	CAP .1UF 10% 100V CER-R
C53	M39014/02-1310	CAP .1UF 10% 100V CER-R
C54	M39014/02-1310	CAP .1UF 10% 100V CER-R
C56	M39014/02-1310	CAP .1UF 10% 100V CER-R
C57	M39014/02-1310	CAP .1UF 10% 100V CER-R
C58	M39014/02-1320	CAP .47UF 10% 50V CER-R
C59	M39014/02-1320	CAP .47UF 10% 50V CER-R
C60	C26-0025-220	CAP 22UF 20% 25V TANT
C61	M39014/02-1320	CAP .47UF 10% 50V CER-R
C62	M39014/02-1310	CAP .1UF 10% 100V CER-R
C63	M39014/02-1310	CAP .1UF 10% 100V CER-R
C64	M39014/02-1310	CAP .1UF 10% 100V CER-R
C65	C26-0025-220	CAP 22UF 20% 25V TANT
C67	M39014/02-1310	CAP .1UF 10% 100V CER-R
C72	M39014/02-1310	CAP .1UF 10% 100V CER-R
C73	M39014/02-1298	CAP .01UF 10% 200V CER-R
C74	C26-0025-220	CAP 22UF 20% 25V TANT
C75	M39014/02-1298	CAP .01UF 10% 200V CER-R
C76	C26-0025-220	CAP 22UF 20% 25V TANT
C77	M39014/02-1310	CAP .1UF 10% 100V CER-R
C78	M39014/02-1298	CAP .01UF 10% 200V CER-R
C79	C26-0025-220	CAP 22UF 20% 25V TANT
C80	M39014/02-1310	CAP .1UF 10% 100V CER-R
C81	M39014/02-1298	CAP .01UF 10% 200V CER-R
C82	C26-0025-220	CAP 22UF 20% 25V TANT
C83	C26-0025-220	CAP 22UF 20% 25V TANT
C84	M39014/02-1310	CAP .1UF 10% 100V CER-R
C85	M39014/02-1310	CAP .1UF 10% 100V CER-R
C87	C26-0025-220	CAP 22UF 20% 25V TANT
C88	M39014/02-1310	CAP .1UF 10% 100V CER-R
C89	M39014/02-1310	CAP .1UF 10% 100V CER-R
C90	M39014/02-1310	CAP .1UF 10% 100V CER-R
C91	M39014/02-1310	CAP .1UF 10% 100V CER-R
C92	M39014/02-1298	CAP .01UF 10% 200V CER-R
C93	M39014/02-1310	CAP .1UF 10% 100V CER-R
C94	M39014/02-1310	CAP .1UF 10% 100V CER-R
C95	M39014/02-1298	CAP .01UF 10% 200V CER-R
C96	M39014/02-1310	CAP .1UF 10% 100V CER-R
C97	M39014/02-1310	CAP .1UF 10% 100V CER-R
C98	M39014/02-1302	CAP .022UF 10% 100V CER-R
C100	M39014/02-1310	CAP .1UF 10% 100V CER-R
C101	M39014/02-1310	CAP .1UF 10% 100V CER-R
C102	M39014/02-1298	CAP .01UF 10% 200V CER-R
C103	M39014/02-1298	CAP .01UF 10% 200V CER-R

Table 4. Synthesizer PWB Assembly A10 Parts List (10215-4100, Rev. G) (Cont.)

Ref. Desig.	Part Number	Description
C104	M39014/02-1298	CAP .01UF 10% 200V CER-R
C105	CK05BX102K	CAP 1000PF 10% 200V CER
C106	M39014/02-1298	CAP .01UF 10% 200V CER-R
C110	C11-0015-047	CAP 4.7PF 5% 63V CER
CR1	1N4454	DIODE 200MA 75V SW
CR2	1N4454	DIODE 200MA 75V SW
CR3	1N5711	DIODE SCHOTTKY 70V .25W
CR4	1N5711	DIODE SCHOTTKY 70V .25W
CR5	1N5711	DIODE SCHOTTKY 70V .25W
CR6	1N5711	DIODE SCHOTTKY 70V .25W
CR7	1N4454	DIODE 200MA 75V SW
CR8	JAN1N748A	DIODE 3.9V 5% .5W ZENER
CR9	1N4454	DIODE 200MA 75V SW
CR10	JAN1N825	DIODE 6.2V .002%TC ZENER
CR11	JAN1N825	DIODE 6.2V .002%TC ZENER
CR12	1N4454	DIODE 200MA 75V SW
CR13	1N4454	DIODE 200MA 75V SW
CR14	1N4454	DIODE 200MA 75V SW
CR15	1N4454	DIODE 200MA 75V SW
CR16	1N6263	DIODE .40W 60V HOT CARR
CR17	1N6263	DIODE .40W 60V HOT CARR
CR18	1N6263	DIODE .40W 60V HOT CARR
J1	J46-0022-008	HDR 8 PIN 0.100" SR LKG
J3	J-0031	CONN SMB VERT PCB F
J4	J46-0022-006	HDR 6 PIN 0.100" SR LKG
JMP1	J41-0002-002	CONN 2 PIN
JMP2	J41-0002-002	CONN 2 PIN
JMP3	J41-0002-002	CONN 2 PIN
JMP4	J41-0002-002	CONN 2 PIN
L1	MS75085-11	COIL 220UH 10% FXD RF
L2	MS75084-2	COIL 1.5UH 10% FXD RF
L3	MS90539-15	COIL 1000UH 5% FXD RF
L4	MS90540-2	COIL 1200UH 5% FXD RF
L5	MS75084-3	COIL 1.8UH 10% FXD RF
L6	MS75084-9	COIL 5.6UH 10% FXD RF
L8	MS14046-8	COIL 22UH 10% FXD RF
L9	MS14046-8	COIL 22UH 10% FXD RF
L10	MS75084-16	COIL 22.0UH 10% FXD RF
L11	L-0185	CHOKE W B 180 MHZ
L12	MS75084-16	COIL 22.0UH 10% FXD RF
P2	J65-0008-103	JMPR 2P FEM .10CNTR
Q1	2N4917	XSTR SS/GP PNP
Q2	2N4917	XSTR SS/GP PNP
Q3	Q50-0009-000	XSTR MPSH34 NPN 45V .35W
Q4	2N4917	XSTR SS/GP PNP
Q5	2N4917	XSTR SS/GP PNP
Q6	2N4917	XSTR SS/GP PNP
Q7	2N4917	XSTR SS/GP PNP

Table 4. Synthesizer PWB Assembly A10 Parts List (10215-4100, Rev. G) (Cont.)

Ref. Desig.	Part Number	Description
Q8	2N5566	XSTR DUAL N-CH JFET
Q9	Q50-0009-000	XSTR MPSH34 NPN 45V .35W
Q10	Q50-0009-000	XSTR MPSH34 NPN 45V .35W
Q11	2N4917	XSTR SS/GP PNP
Q12	Q50-0009-000	XSTR MPSH34 NPN 45V .35W
Q13	2N4917	XSTR SS/GP PNP
Q14	Q50-0009-000	XSTR MPSH34 NPN 45V .35W
Q15	Q50-0009-000	XSTR MPSH34 NPN 45V .35W
Q16	2N4917	XSTR SS/GP PNP
Q17	2N4917	XSTR SS/GP PNP
Q18	2N4917	XSTR SS/GP PNP
Q19	Q50-0009-000	XSTR MPSH34 NPN 45V .35W
Q20	Q50-0009-000	XSTR MPSH34 NPN 45V .35W
Q21	2N4393	XSTR JFET N-CH TO-18
Q22	2N4393	XSTR JFET N-CH TO-18
Q23	Q50-0009-000	XSTR MPSH34 NPN 45V .35W
Q24	Q50-0009-000	XSTR MPSH34 NPN 45V .35W
Q25	2N3904	XSTR SS/GP NPN TO-92
Q26	2N3904	XSTR SS/GP NPN TO-92
Q27	2N3904	XSTR SS/GP NPN TO-92
Q28	Q35-0003-002	XSTR N-CH JFET U309
Q29	Q35-0003-002	XSTR N-CH JFET U309
Q30	JAN2N5116	XSTR SW P-CH JFET 30V
Q31	2N4917	XSTR SS/GP PNP
Q32	Q50-0011-000	XSTR DUAL AMP MD918A
Q33	Q50-0009-000	XSTR MPSH34 NPN 45V .35W
Q34	JAN2N5116	XSTR SW P-CH JFET 30V
Q35	2N4917	XSTR SS/GP PNP
Q36	Q50-0009-000	XSTR MPSH34 NPN 45V .35W
Q37	Q35-0003-000	XSTR N-CH JFET U310
Q38	2N4917	XSTR SS/GP PNP
Q39	Q50-0009-000	XSTR MPSH34 NPN 45V .35W
Q40	Q50-0009-000	XSTR MPSH34 NPN 45V .35W
R1	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R2	R65-0003-331	RES 330 5% 1/4W CAR FILM
R3	R65-0003-331	RES 330 5% 1/4W CAR FILM
R4	R65-0003-471	RES 470 5% 1/4W CAR FILM
R5	R65-0003-471	RES 470 5% 1/4W CAR FILM
R6	RN55D6490F	RES 649 1% 1/8W MET FLM
R7	RN55D1960F	RES 196 1% 1/8W MET FLM
R8	RN55D5111F	RES 5110 1% 1/8W MET FLM
R9	R65-0003-220	RES 22 5% 1/4W CAR FILM
R10	R65-0003-152	RES 1.5K 5% 1/4W CAR FILM
R11	R65-0003-152	RES 1.5K 5% 1/4W CAR FILM
R18	RN55D1212F	RES 12.1K 1% 1/8W MET FLM
R19	RN55D1501F	RES 1500 1% 1/8W MET FLM
R20	RN55D6810F	RES 681 1% 1/8W MET FLM
R21	R65-0003-182	RES 1.8K 5% 1/4W CAR FILM
R22	R65-0003-470	RES 47 5% 1/4W CAR FILM

Table 4. Synthesizer PWB Assembly A10 Parts List (10215-4100, Rev. G) (Cont.)

Ref. Desig.	Part Number	Description
R24	RN55D1781F	RES 1780 1% 1/8W MET FLM
R25	RN55D3481F	RES 3480 1% 1/8W MET FLM
R26	RN55D7501F	RES 7500 1% 1/8W MET FLM
R27	RN55D6190F	RES 619 1% 1/8W MET FLM
R28	RN55D5111F	RES 5110 1% 1/8W MET FLM
R29	RN55D5111F	RES 5110 1% 1/8W MET FLM
R30	R65-0003-820	RES 82 5% 1/4W CAR FILM
R31	R65-0003-101	RES 100 5% 1/4W CAR FILM
R32	R65-0003-100	RES 10 5% 1/4W CAR FILM
R33	R65-0003-100	RES 10 5% 1/4W CAR FILM
R34	RN55D1472F	RES 14.7K 1% 1/8W MET FLM
R35	RN55D1961F	RES 1960 1% 1/8W MET FLM
R36	RN55D1472F	RES 14.7K 1% 1/8W MET FLM
R37	RN55D1000F	RES 100 1% 1/8W MET FLM
R38	RN55D1000F	RES 100 1% 1/8W MET FLM
R39	RN55D6190F	RES 619 1% 1/8W MET FLM
R40	R65-0003-470	RES 47 5% 1/4W CAR FILM
R41	RN55D2151F	RES 2150 1% 1/8W MET FLM
R42	RN55D1212F	RES 12.1K 1% 1/8W MET FLM
R43	RN55D2870F	RES 287 1% 1/8W MET FLM
R44	R65-0003-101	RES 100 5% 1/4W CAR FILM
R45	R65-0003-101	RES 100 5% 1/4W CAR FILM
R46	RN55D6810F	RES 681 1% 1/8W MET FLM
R47	R65-0003-332	RES 3.3K 5% 1/4W CAR FILM
R48	R65-0003-101	RES 100 5% 1/4W CAR FILM
R49	R65-0003-560	RES 56 5% 1/4W CAR FILM
R50	R65-0003-101	RES 100 5% 1/4W CAR FILM
R51	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R52	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R53	R65-0003-183	RES 18K 5% 1/4W CAR FILM
R54	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R55	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R56	RN55D4422F	RES 44.2K 1% 1/8W MET FLM
R57	RN55D6811F	RES 6810 1% 1/8W MET FLM
R58	R65-0003-470	RES 47 5% 1/4W CAR FILM
R59	R65-0003-101	RES 100 5% 1/4W CAR FILM
R60	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R61	RN55D1961F	RES 1960 1% 1/8W MET FLM
R62	RN55D8250F	RES 825 1% 1/8W MET FLM
R63	R65-0003-101	RES 100 5% 1/4W CAR FILM
R64	RN55D5110F	RES 511 1% 1/8W MET FLM
R65	RN55D5110F	RES 511 1% 1/8W MET FLM
R66	R65-0003-101	RES 100 5% 1/4W CAR FILM
R67	RN55D1961F	RES 1960 1% 1/8W MET FLM
R68	RN55D1961F	RES 1960 1% 1/8W MET FLM
R69	RN55D8250F	RES 825 1% 1/8W MET FLM
R70	R65-0003-101	RES 100 5% 1/4W CAR FILM

Table 4. Synthesizer PWB Assembly A10 Parts List (10215-4100, Rev. G) (Cont.)

Ref. Desig.	Part Number	Description
R71	R65-0003-821	RES 820 5% 1/4W CAR FILM
R72	R65-0003-821	RES 820 5% 1/4W CAR FILM
R73	R65-0003-821	RES 820 5% 1/4W CAR FILM
R74	R65-0003-470	RES 47 5% 1/4W CAR FILM
R75	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R76	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R77	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R78	RN55D3831F	RES 3830 1% 1/8W MET FLM
R79	RN55D1001F	RES 1000 1% 1/8W MET FLM
R80	RN55D1961F	RES 1960 1% 1/8W MET FLM
R81	RN55D3831F	RES 3830 1% 1/8W MET FLM
R82	RN55D1001F	RES 1000 1% 1/8W MET FLM
R83	RN55D1961F	RES 1960 1% 1/8W MET FLM
R84	RN55D3831F	RES 3830 1% 1/8W MET FLM
R85	RN55D1001F	RES 1000 1% 1/8W MET FLM
R86	RN55D1961F	RES 1960 1% 1/8W MET FLM
R87	R65-0003-681	RES 680 5% 1/4W CAR FILM
R88	R65-0003-101	RES 100 5% 1/4W CAR FILM
R89	R65-0003-470	RES 47 5% 1/4W CAR FILM
R90	R30-0008-503	RES VAR PCB 50K 1/2W 10%
R91	RN55D1002F	RES 10.0K 1% 1/8W MET FLM
R92	R-2206	RES VAR 1K 10% .5W HOR.
R93	R-2202	RES VAR 50 10% .5W HOR.
R94	RN55D5621F	RES 5620 1% 1/8W MET FLM
R95	RN55D2001F	RES 2000 1% 1/8W MET FLM
R96	RN55D9093F	RES 909K 1% 1/8W MET FLM
R97	RN55D1000F	RES 100 1% 1/8W MET FLM
R98	RN55D1002F	RES 10.0K 1% 1/8W MET FLM
R99	RCR07G106JM	RES 10M 5% 1/4W CAR COMP
R100	R65-0003-470	RES 47 5% 1/4W CAR FILM
R101	R65-0003-222	RES 2.2K 5% 1/4W CAR FILM
R102	R65-0003-222	RES 2.2K 5% 1/4W CAR FILM
R103	R65-0003-470	RES 47 5% 1/4W CAR FILM
R104	RN55D4221F	RES 4220 1% 1/8W MET FLM
R105	RN55D6811F	RES 6810 1% 1/8W MET FLM
R106	RN55D6811F	RES 6810 1% 1/8W MET FLM
R107	RN55D1332F	RES 13.3K 1% 1/8W MET FLM
R108	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R109	R65-0003-153	RES 15K 5% 1/4W CAR FILM
R110	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R111	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R112	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R113	R65-0003-223	RES 22K 5% 1/4W CAR FILM
R114	RN55D4022F	RES 40.2K 1% 1/8W MET FLM
R115	RN55D3321F	RES 3320 1% 1/8W MET FLM
R116	R65-0003-100	RES 10 5% 1/4W CAR FILM
R117	R65-0003-470	RES 47 5% 1/4W CAR FILM
R118	R65-0003-221	RES 220 5% 1/4W CAR FILM

Table 4. Synthesizer PWB Assembly A10 Parts List (10215-4100, Rev. G) (Cont.)

Ref. Desig.	Part Number	Description
R119	R65-0003-270	RES 27 5% 1/4W CAR FILM
R121	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R122	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R123	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R124	R65-0003-470	RES 47 5% 1/4W CAR FILM
R125	R65-0003-470	RES 47 5% 1/4W CAR FILM
R126	R65-0003-470	RES 47 5% 1/4W CAR FILM
R127	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R129	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R130	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R131	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R132	R65-0003-470	RES 47 5% 1/4W CAR FILM
R133	R65-0003-470	RES 47 5% 1/4W CAR FILM
R134	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R135	R65-0003-470	RES 47 5% 1/4W CAR FILM
R136	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R137	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R138	R65-0003-470	RES 47 5% 1/4W CAR FILM
R140	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R141	R65-0003-222	RES 2.2K 5% 1/4W CAR FILM
R145	RN55D6191F	RES 6190 1% 1/8W MET FLM
R146	RN55D6491F	RES 6490 1% 1/8W MET FLM
R147	RN55D7151F	RES 7150 1% 1/8W MET FLM
R148	RN55D1002F	RES 10.0K 1% 1/8W MET FLM
R149	RN55D1002F	RES 10.0K 1% 1/8W MET FLM
R150	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R151	R65-0003-331	RES 330 5% 1/4W CAR FILM
R157	R65-0003-101	RES 100 5% 1/4W CAR FILM
R158	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R159	R-2209	RES VAR 10K 10% .5W HOR.
R160	RN55D1003F	RES 100K 1% 1/8W MET FLM
R161	R65-0003-104	RES 100K 5% 1/4W CAR FILM
R162	R65-0002-104	RES 100K 5% 1/8W CAR FILM
R163	R65-0003-221	RES 220 5% 1/4W CAR FILM
R164	R65-0003-100	RES 10 5% 1/4W CAR FILM
R165	R65-0003-151	RES 150 5% 1/4W CAR FILM
R166	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R167	R65-0003-152	RES 1.5K 5% 1/4W CAR FILM
R168	R65-0003-471	RES 470 5% 1/4W CAR FILM
R169	R65-0003-560	RES 56 5% 1/4W CAR FILM
R170	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R171	R65-0003-223	RES 22K 5% 1/4W CAR FILM
R172	R65-0003-473	RES 47K 5% 1/4W CAR FILM
R173	R65-0003-223	RES 22K 5% 1/4W CAR FILM
TP1	J46-0047-001	HDR 1 POSITION
TP2	J46-0047-001	HDR 1 POSITION
TP3	J46-0047-001	HDR 1 POSITION
TP4	J46-0047-001	HDR 1 POSITION

Table 4. Synthesizer PWB Assembly A10 Parts List (10215-4100, Rev. G) (Cont.)

Ref. Desig.	Part Number	Description
U1	115-0000-074	IC 74HC74 PLASTIC CMOS
U2	115-0000-000	IC 74HC00 PLASTIC CMOS
U3	115-0000-014	IC 74HC14 PLASTIC CMOS
U4	165-0004-001	IC PRESCALER 10/11 12013
U5	10085-5620	IC FRACTIONAL N
U6	101-0000-156	IC 4094B PLASTIC CMOS
U7	105-0000-168	IC 74LS168A PLASTIC TTL
U8	115-0000-109	IC 74HC109 PLASTIC CMOS
U9	115-0000-174	IC 74HC174 PLASTIC CMOS
U10	115-0000-192	IC 74HC192 PLASTIC CMOS
U11	115-0000-074	IC 74HC74 PLASTIC CMOS
U12	115-0000-074	IC 74HC74 PLASTIC CMOS
U13	101-0000-156	IC 4094B PLASTIC CMOS
U14	115-0000-002	IC 74HC02 PLASTIC CMOS
U15	115-0000-027	IC 74HC27 PLASTIC CMOS
U16	115-0000-073	IC 74HC73 PLASTIC CMOS
U18	115-0000-192	IC 74HC192 PLASTIC CMOS
U22	115-0000-192	IC 74HC192 PLASTIC CMOS
U23	190-0008-001	IC XSTR ARRAY 3045
U24	10085-5610	RES NETWORK SPECIAL 16PIN
VR1	112-0006-012	IC VR 78L12A + 12V .10A 4%
VR2	112-0010-012	IC VR 79L12A -12V .10A 4%
VR3	112-0006-005	IC VR 78L05A + 5V .10A 4%
VR4	112-0006-005	IC VR 78L05A + 5V .10A 4%
VR5	112-0006-005	IC VR 78L05A + 5V .10A 4%
VR7	111-0001-001	IC VR 7805 + 5V 1.5A 4%
VR8	112-0006-005	IC VR 78L05A + 5V .10A 4%

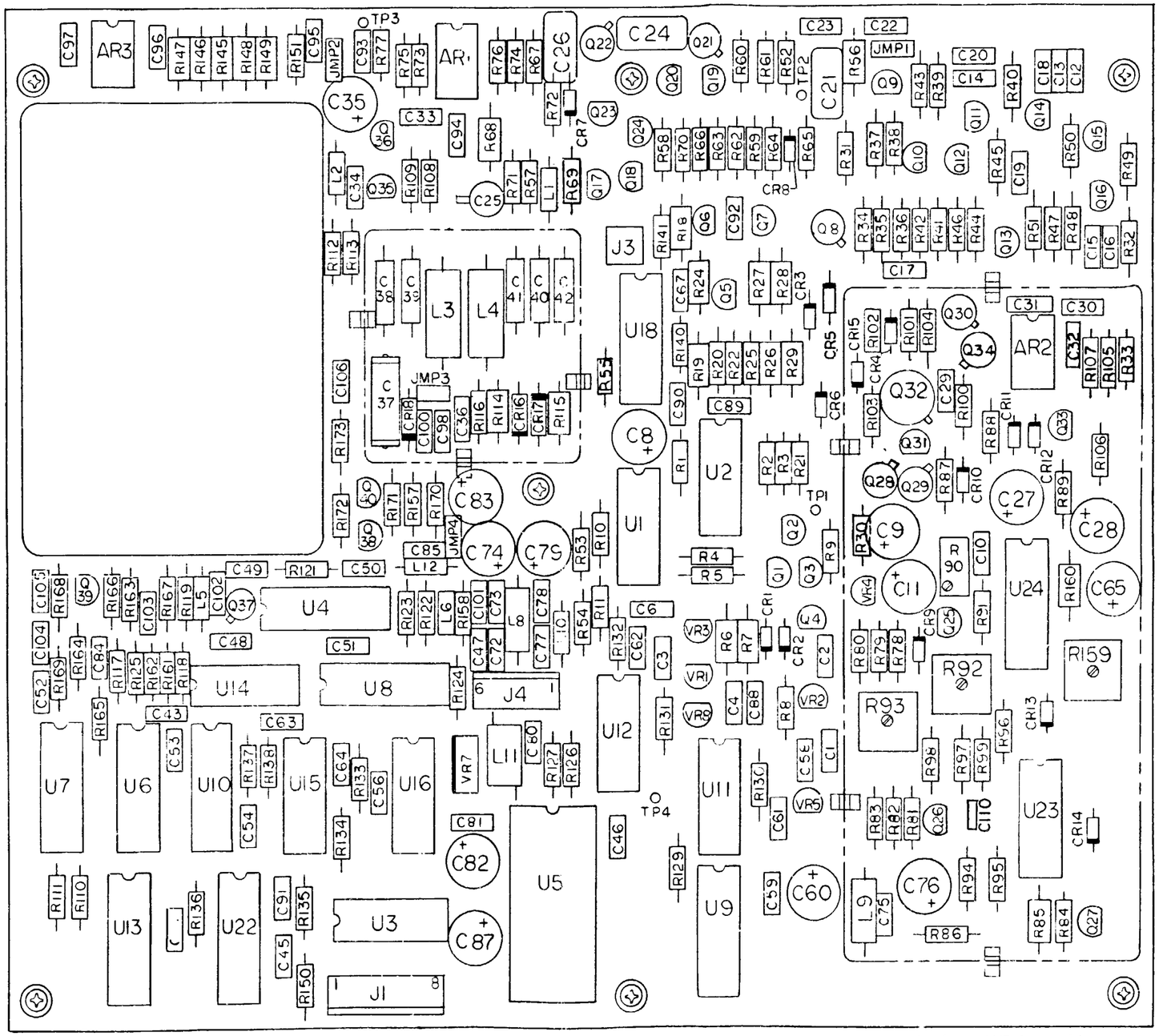


Figure 11. Synthesizer PWB Assembly Component Locations (10215-4100, Rev. D)

NOTE: UNLESS OTHERWISE SPECIFIED:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR A COMPLETE DESIGNATION, PREFIX WITH UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.
2. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, ±5%.
3. ALL CAPACITOR VALUES ARE IN MICROFARADS.
4. VENDOR PART NO. CALLOUTS ARE FOR REFERENCE ONLY. COMPONENTS ARE SUPPLIED PER PART NO. IN PARTS LIST.
5. ALL RESISTORS ON VCO ASSY 10215-4120 ARE 1/8W, ±5% UNLESS OTHERWISE SPECIFIED.
6. LEVEL SPECIFIED IS WITH RECEIVER TUNED TO 1.64500 MHZ. (L.O. OUTPUT AT PI=42.10000 MHZ)

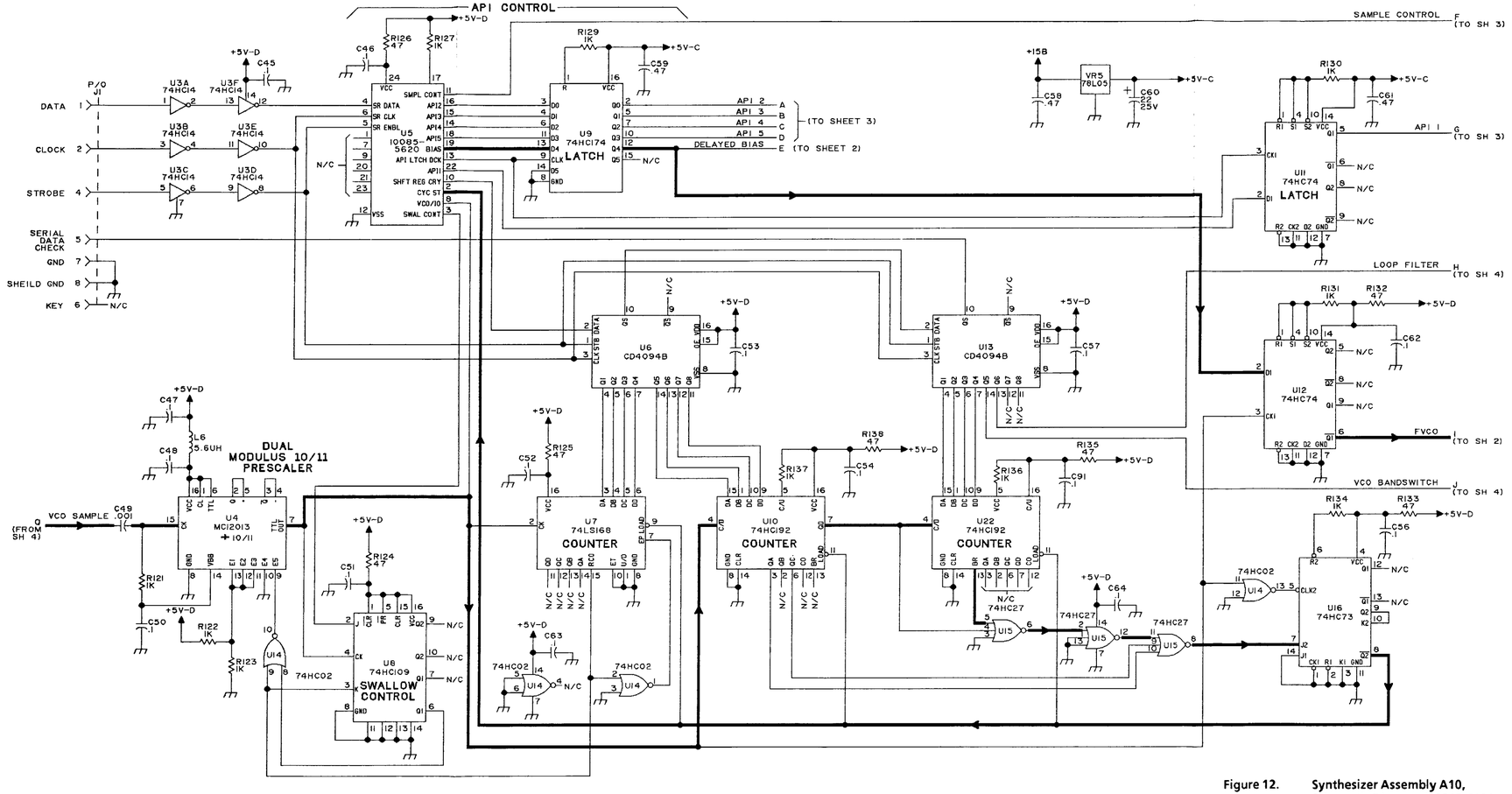


Figure 12. Synthesizer Assembly A10, Schematic Diagram (10215-4101, Rev. K) (Sheet 1 of 5)

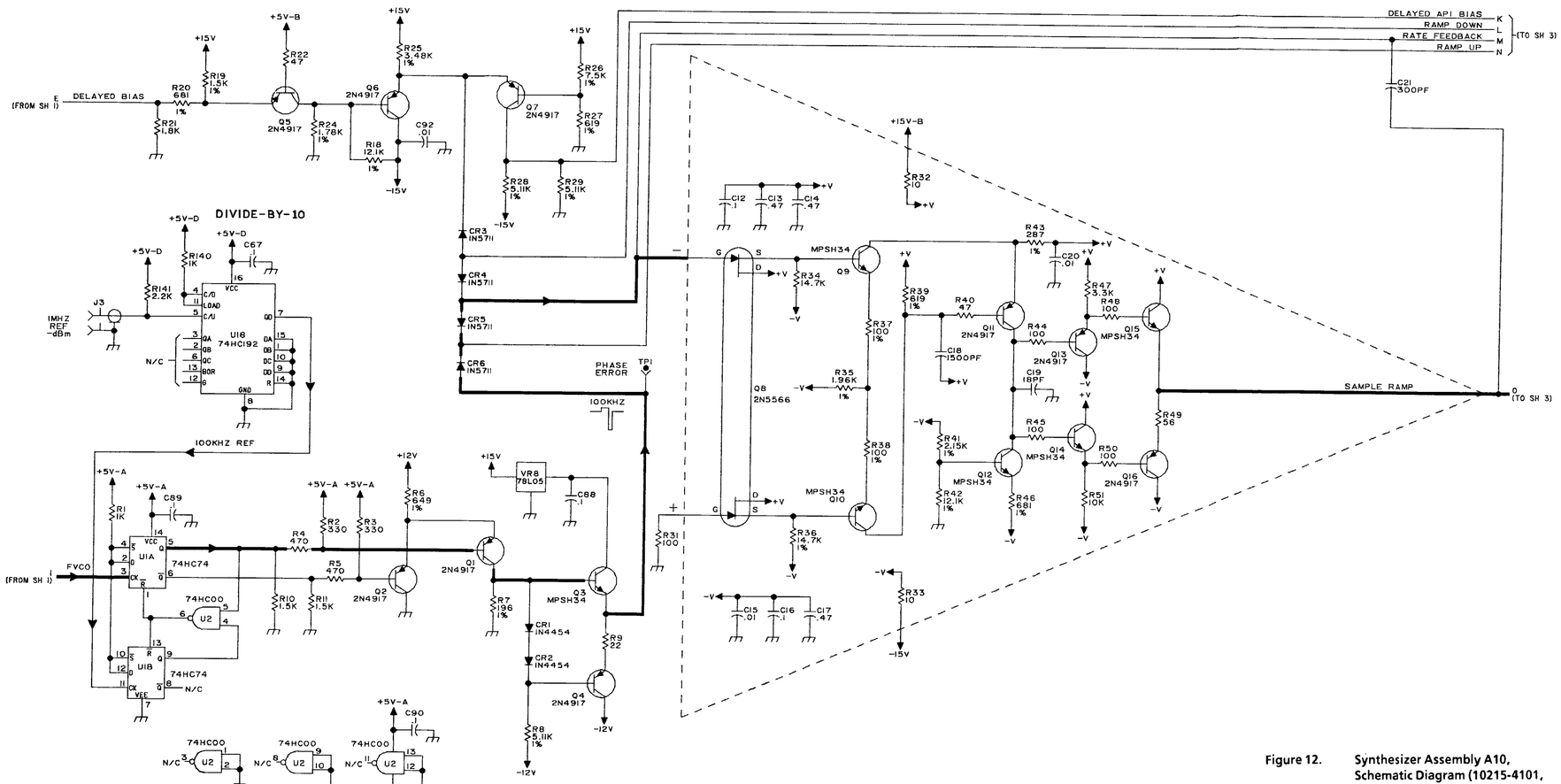


Figure 12. Synthesizer Assembly A10, Schematic Diagram (10215-4101, Rev. K) (Sheet 2 of 5)

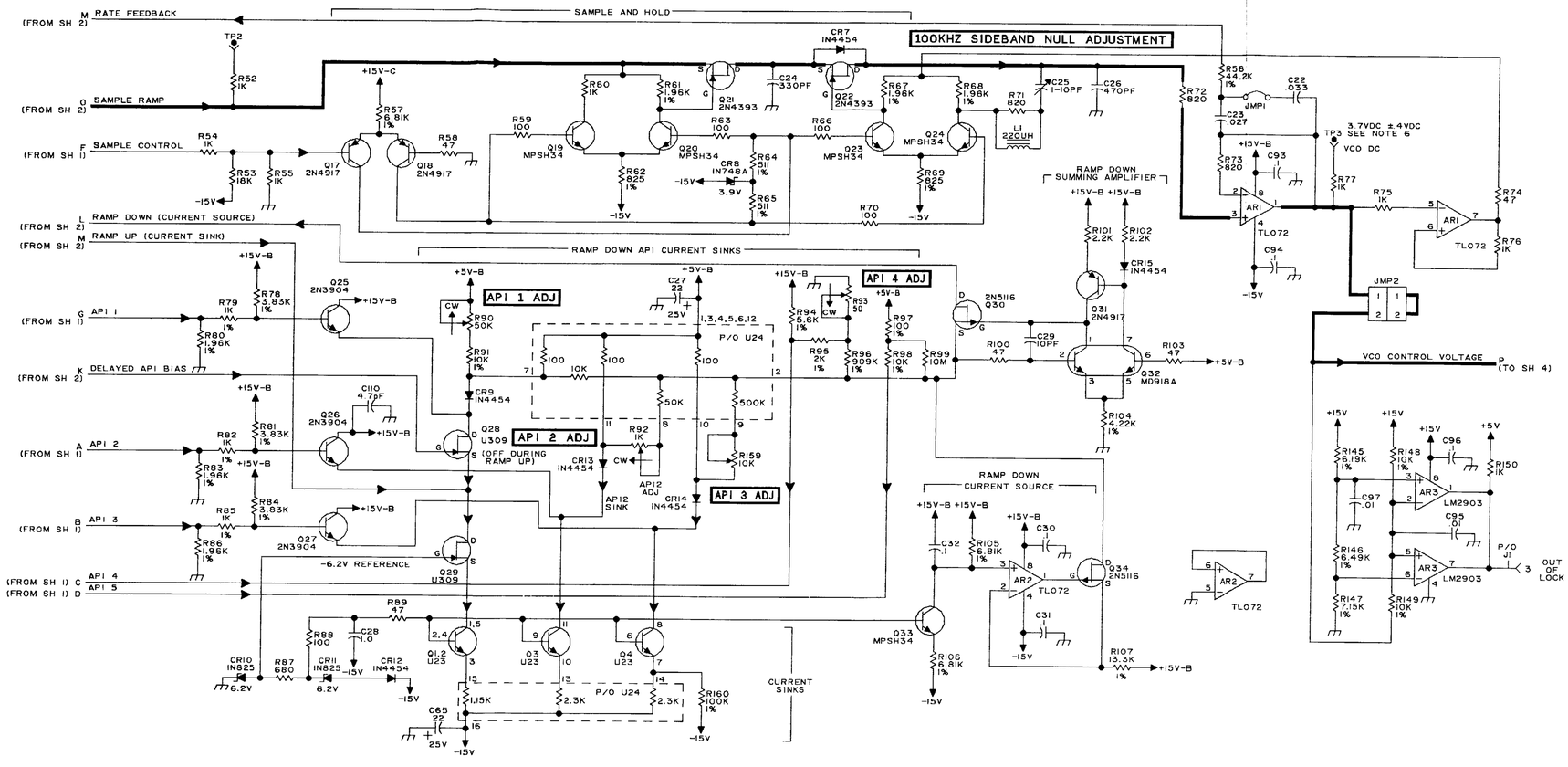


Figure 12. Synthesizer Assembly A10, Schematic Diagram (10215-4101, Rev. K) (Sheet 3 of 5)

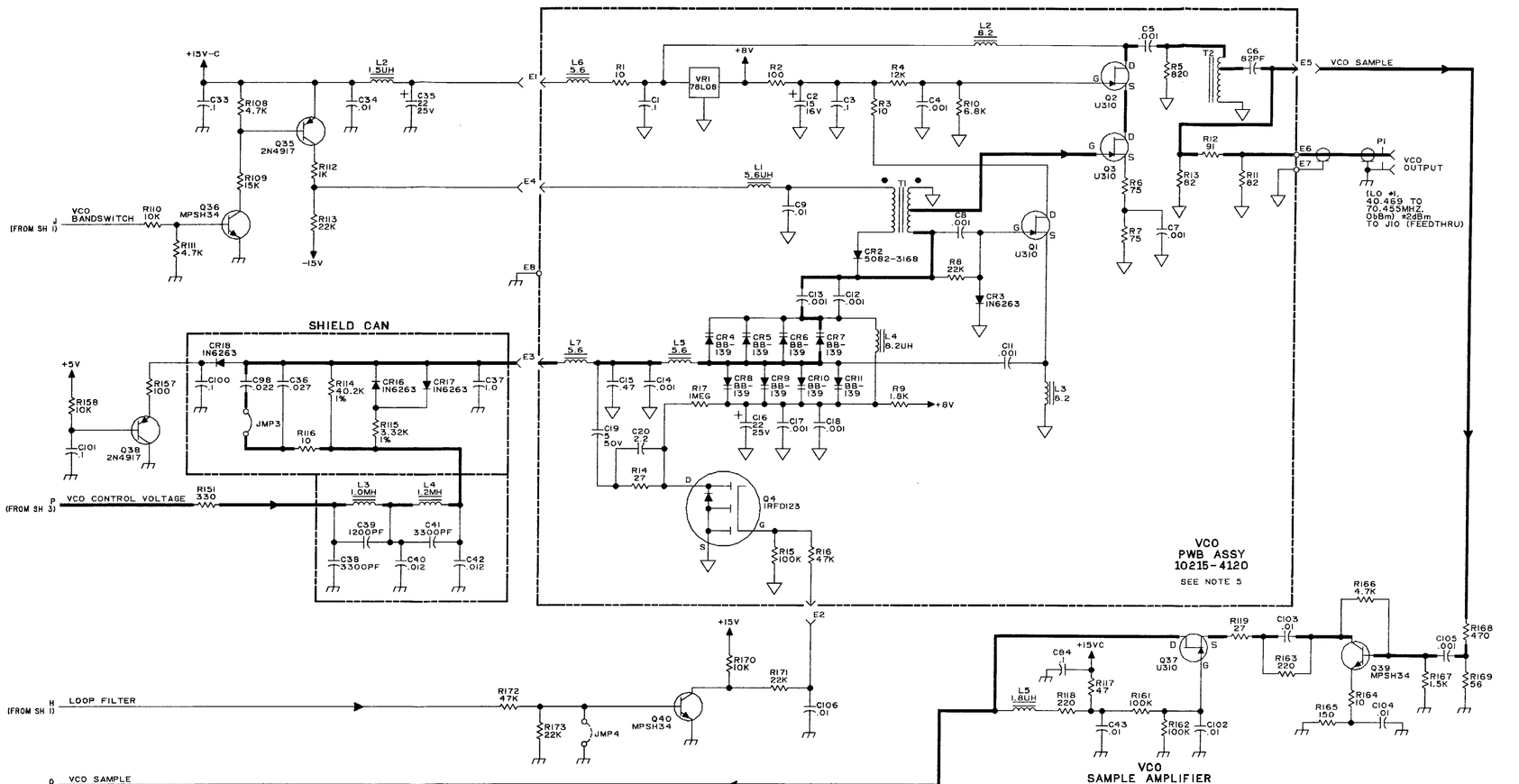


Figure 12. Synthesizer Assembly A10, Schematic Diagram (10215-4101, Rev. K) (Sheet 4 of 5)

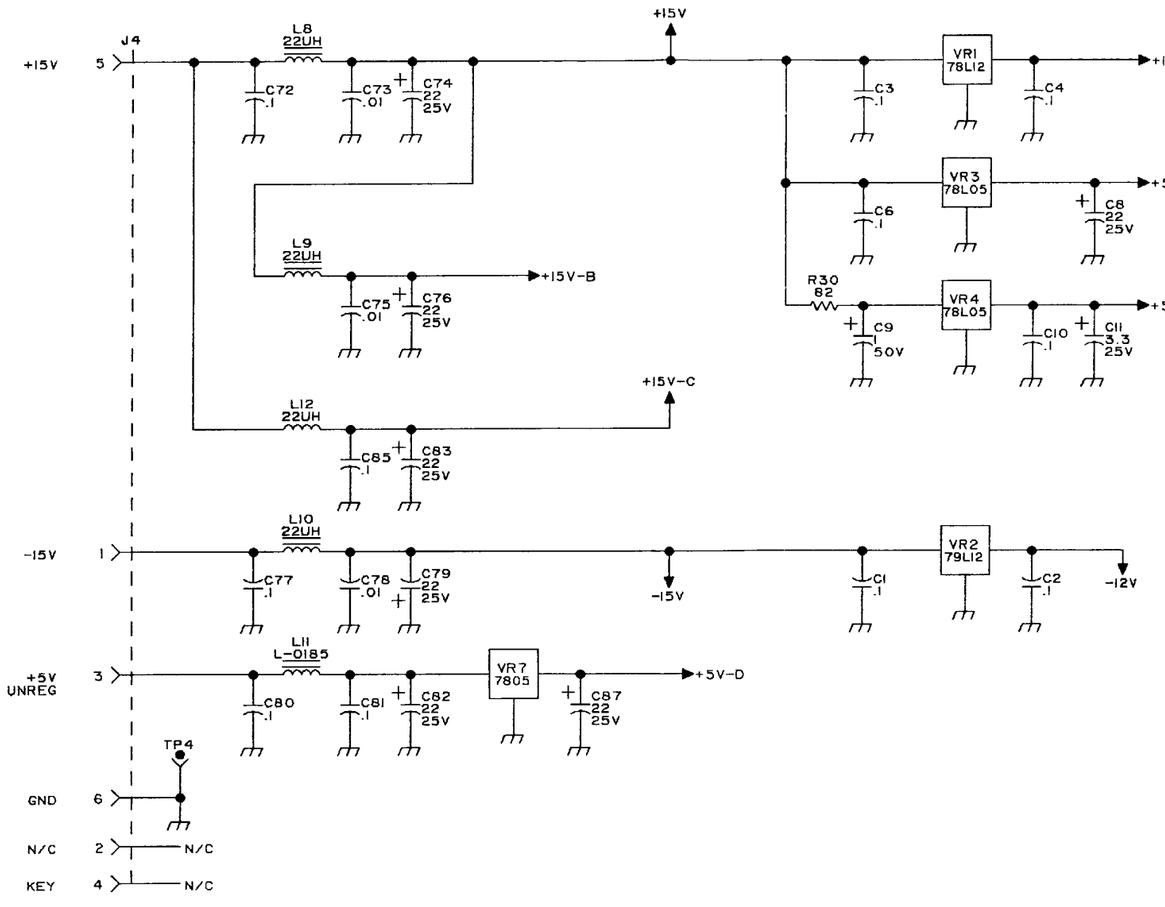


Figure 12. Synthesizer Assembly A10, Schematic Diagram (10215-4101, Rev. K) (Sheet 5 of 5)

Table 5. Synthesizer VCO PWB Assembly A10A1 Parts List (10215-4120, Rev. C)

Ref. Desig.	Part Number	Description
C1	M39014/02-1310	CAP .1 UF
C2	C26-0016-150	CAP, TANT 15MFD 16V
C3	M39014/02-1310	CAP .1 UF
C4	CK05BX102K	CAP 1000PF 10% 200V CER
C5	CK05BX102K	CAP 1000PF 10% 200V CER
C6	CM05ED820G03	CAP 82PF 2% 500V MICA
C7	CK05BX102K	CAP 1000PF 10% 200V CER
C8	CK05BX102K	CAP 1000PF 10% 200V CER
C9	M39014/02-1298	CAP 01UF
C11	CK05BX102K	CAP 1000PF 10% 200V CER
C12	CK05BX102K	CAP 1000PF 10% 200V CER
C13	CK05BX102K	CAP 1000PF 10% 200V CER
C14	CK05BX102K	CAP 1000PF 10% 200V CER
C15	C61-0002-003	CAP, MYLAR .47 100V
C16	C26-0025-220	CAP TANT 22 UF 25V
C17	CK05BX102K	CAP 1000PF 10% 200V CER
C18	CK05BX102K	CAP 1000PF 10% 200V CER
C19	C80-0004-505	CAP 5UF,50V METAL PO
C20	C61-0003-005	CAPACITOR
CR2	D10-3500-000	DIODE,PIN SWITCHING
CR3	1N6263	DIODE,HOT CARRIER
CR4	D25-0002-001	DIODE, VARICAP
CR5	D25-0002-001	DIODE, VARICAP
CR6	D25-0002-001	DIODE, VARICAP
CR7	D25-0002-001	DIODE, VARICAP
CR8	D25-0002-001	DIODE, VARICAP
CR9	D25-0002-001	DIODE, VARICAP
CR10	D25-0002-001	DIODE, VARICAP
CR11	D25-0002-001	DIODE, VARICAP
L1	MS14046-1	COIL, RF 5.6 UH 10%
L2	MS75084-11	COIL, RF 8.2 UH 10%
L3	MS75084-11	COIL, RF 8.2 UH 10%
L4	MS75084-11	COIL, RF 8.2 UH 10%
L5	MS14046-1	COIL, RF 5.6 UH 10%
L6	MS14046-1	COIL, RF 5.6 UH 10%
L7	MS14046-1	COIL, RF 5.6 UH 10%
P1	J92-0005-003	CONN,COAX,SUBMIN PLUG
Q1	Q35-0003-000	XSTR, JFET, HIGH GM
Q2	Q35-0003-000	XSTR, JFET, HIGH GM
Q3	Q35-0003-000	XSTR, JFET, HIGH GM
Q4	Q65-0003-001	XSTR, IRD 123 MOS FET
R1	R65-0002-100	RES,10 5% 1/8W CAR FILM
R2	R65-0002-101	RES,100 5% 1/8W CAR FILM
R3	R65-0002-100	RES,10 5% 1/8W CAR FILM
R4	R65-0002-122	RES,1.2K 5% 1/8W CAR FILM
R5	R65-0002-821	RES,820 5% 1/8W CAR FILM
R6	R65-0002-750	RES,75 5% 1/8W CAR FILM

Table 5. Synthesizer VCO PWB Assembly A10A1 Parts List (10215-4120, Rev. C) (Cont.)

Ref. Desig.	Part Number	Description
R7	R65-0002-750	RES,75 5% 1/8W CAR FILM
R8	R65-0002-223	RES,22K 5% 1/8W CAR FILM
R9	R65-0002-182	RES,1.8K 5% 1/8W CAR FILM
R10	R65-0002-682	RES,6.8K 5% 1/8W CAR FILM
R11	RCR05G820JM	RES,82 5% 1/8W CAR COMP
R12	RCR05G910JM	RES,1/8W 5% 910HM
R13	RCR05G820JM	RES,82 5% 1/8W CAR COMP
R14	R65-0002-270	RES,27 5% 1/8W CAR FILM
R15	R65-0002-104	RES,100K 5% 1/8W CAR FILM
R16	R65-0002-473	RES,47K 5% 1/8W CAR FILM
R17	R65-0002-105	RES,1.0M 5% 1/8W CAR FILM
T1	10215-4122	TRANSFORMER, OSC
T2	10215-4123	TRANSFORMER, OUTPUT
VR1	I12-0006-008	IC VR 78L08A +8V .10A 4%

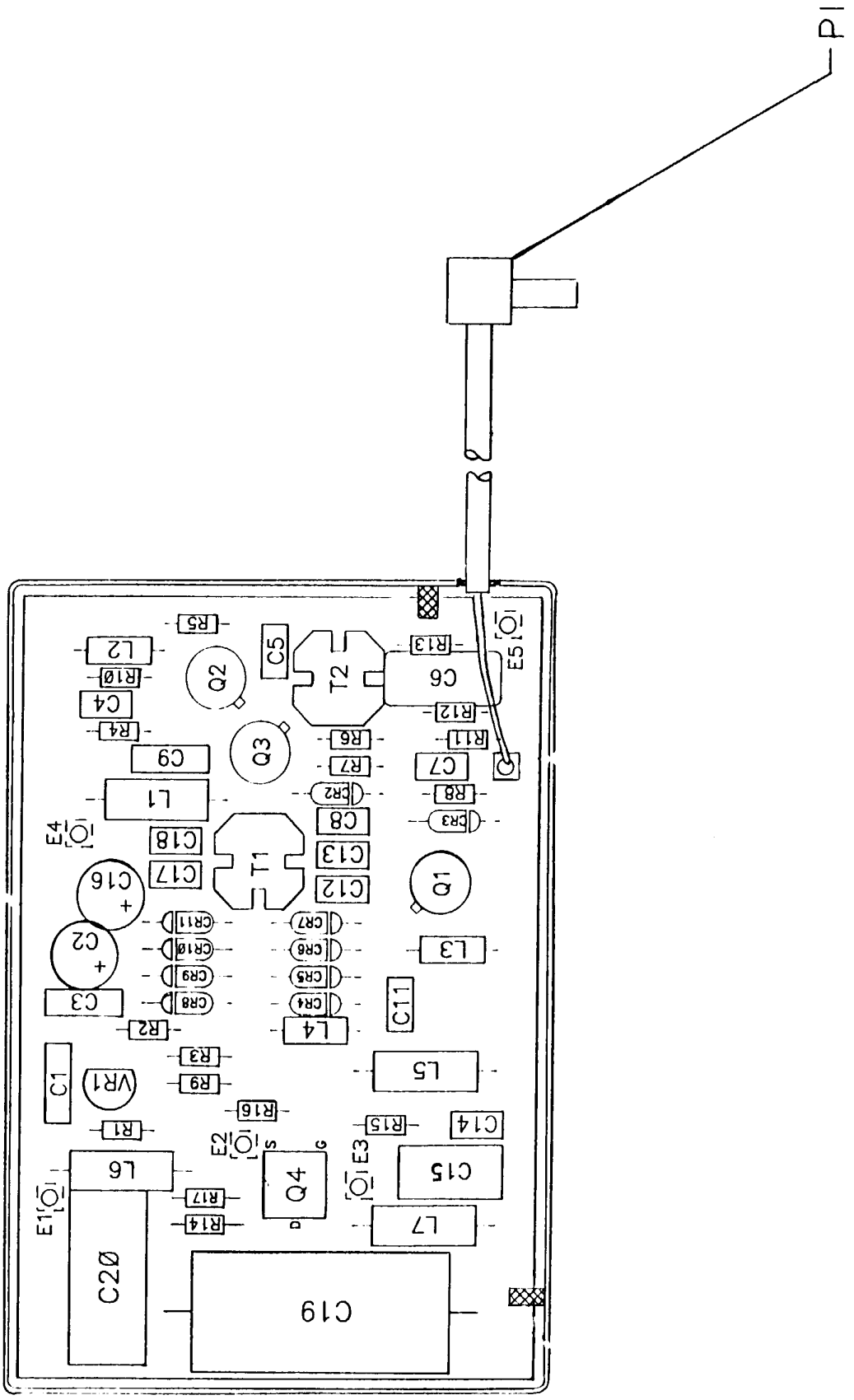
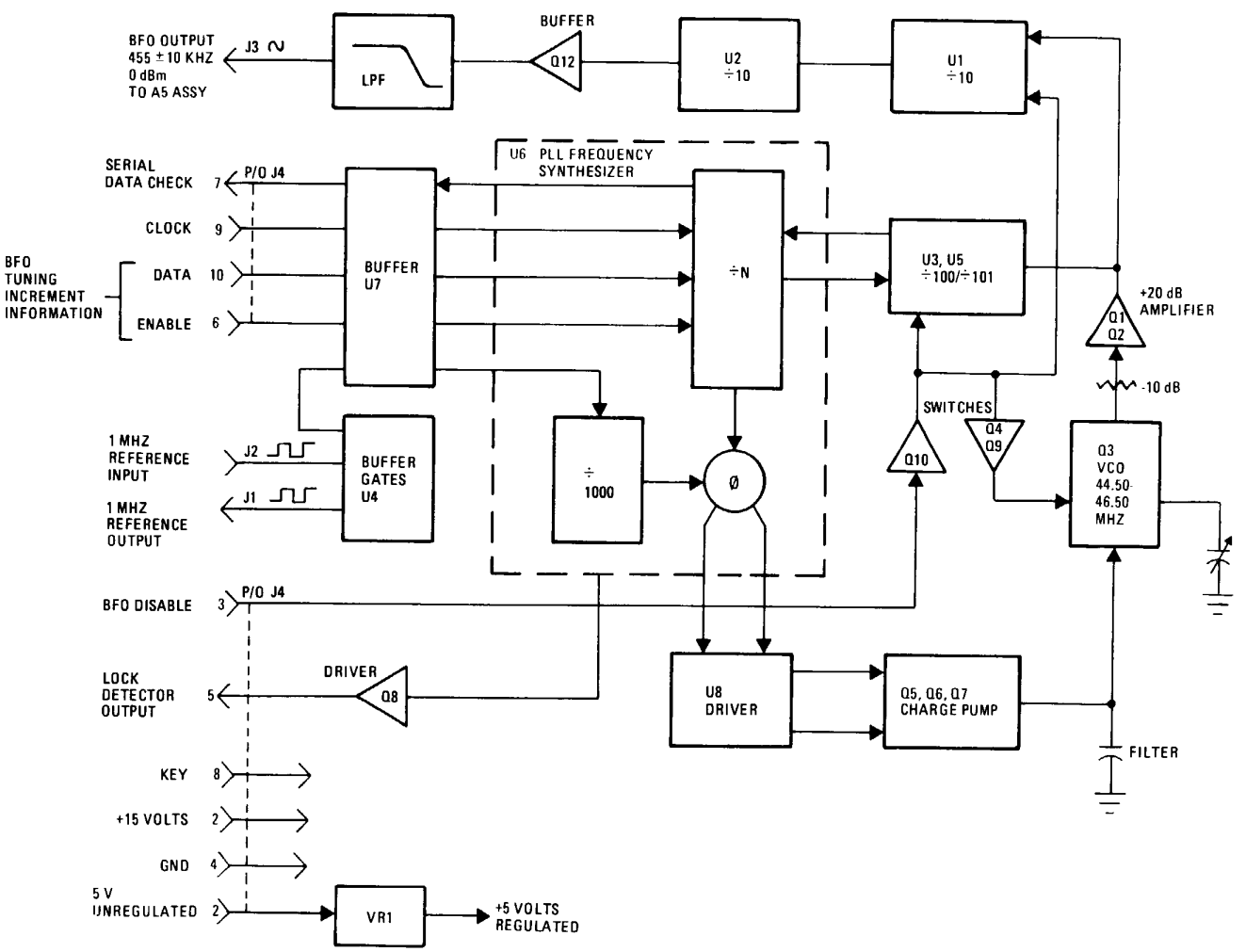


Figure 13. VCO PWB Assembly A10A1 Component Locations (10215-4120)

A11
BFO ASSEMBLY



590-28(1)

TABLE OF CONTENTS

Paragraph		Page
1.	General Description	1
2.	Interface Connections	1
3.	Circuit Description	1
3.1	Reference Generation	1
3.2	Divide by N Counter	2
3.3	Phase Comparator and Charge Pump Operation	2
3.4	VCO Operation and Control	3
3.5	BITE Circuits	3
4.	Maintenance	3
4.1	VCO Adjustment	3
5.	Parts List	5
6.	Schematic Diagram	5

LIST OF FIGURES

Figure		Page
1	BFO VCO Alignment	4
2	BFO Assembly A11 Component Location Diagram (10073-4600)	10
3	BFO Assembly A11 Schematic Diagram (10073-4601)	11

LIST OF TABLES

Table		Page
1	A11 BFO Interface Connections	1
2	BFO Frequency Offset	4
3	BFO Assembly A11 Parts List (PL 10073-4600)	6

A11 BFO ASSEMBLY

1. GENERAL DESCRIPTION

The A11 BFO Assembly is a single phase locked loop synthesizer that provides the BFO offset injection required for proper CW or SSB reception. The BFO range is ± 10 kHz around 455 kHz. It is selected via BFO selection controls in 10 Hz increments.

Frequency select input data is applied to the A11 assembly in serial data form from the Control Assembly A14. A11 output is applied to IF/Audio Assembly A5 where it mixes with the second IF of 455 kHz to permit proper CW and SSB demodulation.

2. INTERFACE CONNECTIONS

Table 1 lists the various input/output connections and other relevant data.

Table 1. A11 BFO Synthesizer Interface Connections

Connector	Function	Characteristics
J1	1 MHz Reference Output	TTL
J2	1 MHz Reference Input	TTL
J3	BFO Output	455 kHz ± 10 kHz, 0 dBm
J4-1	+ 15 V	Approximately 20 mA
J4-2	+ 5.0 V Unregulated	Approximately 200 mA
J4-3	BFO Disable	+ 5 V = BFO Disabled
J4-4	GND	
J4-5	Lock Detector Output	P/O BITE, + 5 V = Unlocked, 0 V = Locked
J4-6	Enable	+ going pulse = Enabled
J4-7	Serial Data Check	P/O BITE Testing, + 5 Vdc = ok
J4-8	Key	
J4-9	Clock	TTL, 750 kHz
J4-10	Data	TTL

3. CIRCUIT DESCRIPTION

3.1 Reference Generation

A 1 MHz signal from Reference Generator Assembly A12 enters the A11 BFO at J2. This signal is buffered by TTL NAND gates in U4 and directed to J1, a spare 1 MHz output. It is also routed to a divide by 1000 counter (internal to U6) via buffer stage U7 to produce a 1 kHz reference signal. Since this has been ultimately derived from the crystal frequency standard via the A12 assembly, stable and accurate A11 operation is assured.

3.2 Divide by N Counter

Since the A11 assembly requires a variable output frequency (455 kHz ± 10 kHz), a programmable counter has been incorporated into the VCO feedback path to the phase comparator. This counter consists of dual modulus ÷ 100/÷ 101 prescaler network U5 and U3 and a programmable counter internal to U6. Together this circuit creates a total division range of N = 44,500 to N = 46,500 where N is a function of the receiver BFO offset tune positions.

The output of the divide by N counter will always attempt to equal the 1 kHz reference frequency at the phase comparator inputs (despite changes in the divide by N factor due to changing the 1 kHz, 100 Hz, and/or 10 Hz BFO offset tuning positions). To accomplish this, VCO frequency will change in response to command signals generated by the phase comparator output. The VCO frequency will always equal (N) (reference frequency) or (N) (1000 Hz) = 44.50 MHz to 46.50 MHz.

Selection of a BFO offset frequency from the front panel causes Control Assembly A14 to generate a serial data code containing information about the frequency chosen. This code is applied synchronously with the 750 kHz system clock to U6 whenever the U6 enable line is gated open by A14.

The value of N may be found from the formula, N = (45,500 - XXX), where XXX is the ± value of the 1 kHz, 100 Hz, and 10 Hz BFO offset tuning positions. For example, tuning the BFO offset to + 5.00 kHz would make N = 45,500 - (+ 500) = 45,000. The VCO frequency would be (N) (reference) = (45,000) (1000) = 45.00 MHz. There is a divide by 100 counter at the VCO output, so the BFO output at J3 would be 450 kHz. Note that as the selected BFO offset frequency increases the BFO output frequency must decrease.

In summary, the BFO output frequency may be calculated from the following formula, F = 10 (45,500 - XXX) Hz, where ± XXX represents the value of the 1 kHz, 100 Hz, and 10 Hz BFO offset tune frequency.

3.3 Phase Comparator and Charge Pump Operation

Phase comparison of the 1 kHz reference and the 1 kHz VCO derived signal at the divide by N counter output is accomplished by a phase comparator internal to U6.

When these two signals are equal in frequency and phase, the phase comparator outputs at TP4 and TP5 are essentially 5 Vdc. U8 buffers this level to the charge pump circuit where + 5 Vdc on the Q6 and Q7 emitters holds both transistors off. Q5 is also off, and the voltage at TP1 (across C24) is constant. This level holds the VCO frequency constant between 44.5 MHz and 46.5 MHz.

Assume that the division ratio of U3, U5, and U6 is changed so that the VCO derived feedback signal is less than the 1 kHz reference. (This will happen if the divide by N factor increases.) The phase comparator will output a series of negative going pulses at TP4 whose pulse widths are a function of the difference in frequency. Q7 will turn on during these negative periods, and its collector voltage drops. This permits Q5 to turn on and pump charge into C24. This causes the C24 voltage to increase, which in turn causes an increase in the VCO frequency. The VCO frequency increases until the signals at the U6 phase comparator inputs are equal. At this time, the phase comparator output error pulse width will have decreased to an extremely small value. TP4 is essentially at 5 Vdc, Q5 and Q7 turn off, and no further increase in the voltage across C24 will occur. The VCO will therefore rest at a new higher frequency.

Assume that the division ratio changes so the VCO derived feedback signal is greater than the 1 kHz reference. U6 will pulse low at TP5, causing Q6 to turn on. C24 will start to discharge through Q6 to ground, and its voltage drops. This causes the VCO to decrease in frequency until the inputs at the phase comparator are equal. Again, the output error pulse width will have decreased to an extremely small value. TP5 will be at essentially 5 Vdc, Q6 will turn off, the C24 voltage will no longer decrease, and the VCO frequency will rest at this new lower value.

3.4 VCO Operation and Control

Buffer stage U8 applies the phase comparator outputs to a charge pump circuit consisting of Q5, Q6, Q7, and associated components followed by filters C24 and C25. This stage converts the two phase comparator pulse outputs into an analog dc control voltage. This control voltage is then applied to the varactor diode string in the VCO. It controls the operating frequency of JFET Hartley oscillator stage Q3. A new control voltage change of 6.5 Vdc to 8.5 Vdc produces a VCO frequency range of 44.500 MHz to 46.500 MHz.

The VCO output is fed through a 10 dB attenuator network, R10-R11, and to 20 dB gain amplifier stage, Q1 and Q2. The signal is then split and sent to the divide by N circuit U3, U5, and U6 (to complete the feedback loop) and to divide by 100 chain U1 and U2. U2 TTL output at 455 to 465 kHz is applied through buffer stage Q12 to a low pass filter (LPF) network. LPF output is a 455 kHz ± 10 kHz, 0 dBm sine wave and is fed through J3 to IF/Audio Assembly A5 to become the BFO injection frequency.

BFO disabling occurs whenever the receiver is in any mode other than LSB, USB, ISB, or CW modes. This occurs in response to a + 5 Vdc command by the A14 assembly at J4, pin 3. This signal disables the VCO by turning Q10 on. This turns Q4 on. Q4 then removes base drive to Q9. Q9 turns off and removes the supply voltage from oscillator stage Q3. Also, Q10's on state forward biases diodes CR14 and CR15, which shorts out the signals at the U1 and U5 inputs.

3.5 BITE Circuits

The A11 assembly contains two circuits for self-test evaluation.

- Lock detector Q8 whose output is 0 Vdc whenever the PLL is tracking properly. This line is constantly monitored by Control Assembly A14. A front panel fault light will appear if the loop ever unlocks.

- Serial data check that verifies that the tuning data from the A14 assembly has been received and properly translated into the correct divide by N factor. A serial data word is sent by the A14 assembly on the BFO tuning data line (J4 pin 10) and the U6 SW1 output is read at J4, pin 7. If the word has been received and properly decoded, this line will pulse to + 5 Vdc. The serial data check test occurs automatically, but only when the receiver BITE self-test is actuated.

4. MAINTENANCE

The following adjustments should not be performed as a routine maintenance procedure, but only when a failure indicates a definite need. A11 tests should be performed with all connections in normal contact, unless otherwise specified.

4.1 VCO Adjustment

Perform this procedure to align the VCO.

a. Connect equipment as shown in figure 1.

NOTE

A11J3 mates with A5J2 through a hole in the chassis. It will be necessary to remove the A5 assembly to gain access to A11J3.

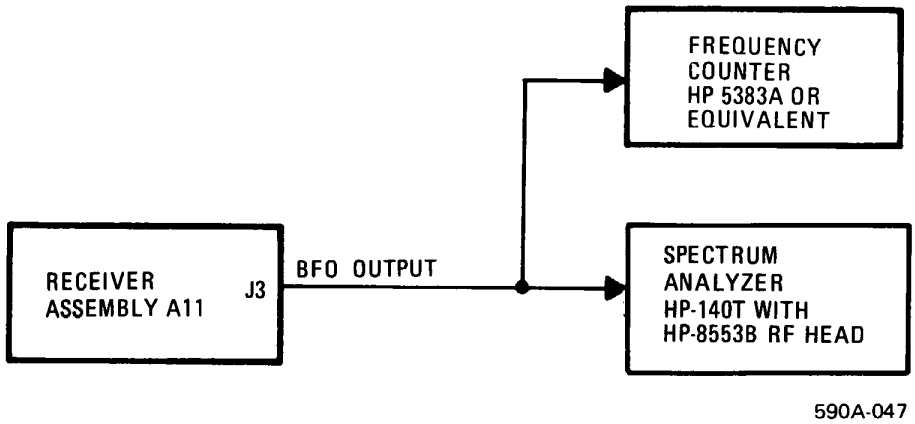


Figure 1. BFO VCO Alignment

b. Set the front panel controls as follows:

- Frequency to 10.000000 MHz
- MODE to USB
- BFO to 0.00 kHz

c. Monitor TP1 with a digital voltmeter. Adjust C20 for 7.0 Vdc.

d. Check that the BFO output frequency (as a function of the front panel BFO settings) agrees with table 2. (BFO output amplitude should always be 0 dBm ± 2 dB.)

Table 2. BFO Frequency Offset

BFO Offset Frequency Selected	BFO Output Frequency	Approximate Voltage at TP1
0.00 kHz	455.00 kHz	7.0
+ 9.99 kHz	445.01 kHz	6.0
-9.99 kHz	464.99 kHz	8.0

e. Fully reconnect the A11 assembly to the Receiver. Initiate BITE self-test. Receiver must pass all tests associated with the A11 assembly. Test is complete.

5. PARTS LIST

Table 3 is a comprehensive parts list of all replaceable components in BFO Assembly A11. When ordering parts from the factory, include a full description of the part. Use figure 2, BFO Assembly A11 component location diagram to identify parts.

6. SCHEMATIC DIAGRAM

Figure 3 is the BFO Assembly A11 schematic diagram.

Table 3. BFO Assembly A11 Parts List (PL 10073-4600, Rev. R)

Ref. Desig.	Part Number	Description
C1	M39014/02-1310	CAP .1 UF
C2	C26-0025-470	CAP,TANT,47UF,25V
C3	M39014/02-1310	CAP .1 UF
C4	M39014/01-1535	CAP .01UF
C5	CK05BX102K	CAP 1000PF 10% 200V CER
C6	M39014/02-1310	CAP .1 UF
C7	M39014/02-1310	CAP .1 UF
C8	M39014/02-1310	CAP .1 UF
C9	M39014/01-1535	CAP .01UF
C10	M39014/01-1535	CAP .01UF
C11	M39014/01-1535	CAP .01UF
C12	M39014/01-1535	CAP .01UF
C13	CK05BX102K	CAP 1000PF 10% 200V CER
C14	M39014/02-1310	CAP .1 UF
C15	M39014/02-1310	CAP .1 UF
C16	M39014/02-1310	CAP .1 UF
C17	C26-0025-680	CAP,FXD,ELCTLT,68UF
C18	M39014/02-1310	CAP .1 UF
C19	M39014/01-1535	CAP .01UF
C20	C84-0003-004	CAP,VAR,CER,9-35 PF
C21	CK05BX102K	CAP 1000PF 10% 200V CER
C22	CK05BX102K	CAP 1000PF 10% 200V CER
C23	C26-0025-680	CAP,FXD,ELCTLT,68UF
C24	C25-0003-107	35V 1MFD TANT
C25	C25-0003-004	CAP FXD ELECT 33UF
C26	C26-0025-100	CAP, TANT, 10UF, 25V
C27	M39014/02-1310	CAP .1 UF
C28	C25-0001-301	TANT CAP 1UF 20V
C29	C26-0016-151	CAP,150UF,16V
C30	M39014/02-1310	CAP .1 UF
C31	C26-0025-100	CAP, TANT, 10UF, 25V
C32	M39014/02-1310	CAP .1 UF
C33	M39014/02-1310	CAP .1 UF
C34	M39014/02-1310	CAP .1 UF
C35	C25-0001-301	TANT CAP 1UF 20V
C36	M39014/02-1310	CAP .1 UF
C37	M39014/02-1310	CAP .1 UF
C38	M39014/02-1310	CAP .1 UF
C40	M39014/02-1310	CAP .1 UF
C41	M39014/02-1310	CAP .1 UF
C42	M39014/02-1310	CAP .1 UF
C43	M39014/02-1310	CAP .1 UF
C44	6628-0660	CAP 5600PF 5% 300V MICA
C45	CM06FD272J03	CAP 2700PF 5% 500V MICA

Table 3. BFO Assembly A11 Parts List (PL 10073-4600, Rev. R) (Cont.)

Ref. Desig.	Part Number	Description
C46	CM06FD751J03	CAP 750PF 5% 500V MICA
C47	C-2503	CAP 820PF 2% 300V MICA
C48	6628-0660	CAP 5600PF 5% 300V MICA
C49	CM06FD272J03	CAP 2700PF 5% 500V MICA
C50	M39014/02-1310	CAP .1 UF
C51	M39014/01-1535	CAP .01UF
C52	M39014/01-1535	CAP .01UF
CR1	10073-7118	DIODE HYPERABRUPT SILICON
CR2	10073-7118	DIODE HYPERABRUPT SILICON
CR3	10073-7118	DIODE HYPERABRUPT SILICON
CR4	10073-7118	DIODE HYPERABRUPT SILICON
CR5	10073-7118	DIODE HYPERABRUPT SILICON
CR6	10073-7118	DIODE HYPERABRUPT SILICON
CR7	10073-7118	DIODE HYPERABRUPT SILICON
CR8	10073-7118	DIODE HYPERABRUPT SILICON
CR9	10073-7118	DIODE HYPERABRUPT SILICON
CR10	10073-7118	DIODE HYPERABRUPT SILICON
CR11	1N6263	DIODE,HOT CARRIER
CR12	1N3064	DIODE
CR13	1N3064	DIODE
CR14	1N3064	DIODE
J1	J-0031	CONNECTOR, COAX, SNAP-ON
J2	J-0031	CONNECTOR, COAX, SNAP-ON
J3	J-0031	CONNECTOR, COAX, SNAP-ON
J4	J46-0032-010	HEADER, 10 PIN DISCRETE
L1	MS14046-9	COIL, RF 27 UH 10%
L2	MS75084-3	COIL, RF 1.8 UH 10%
L3	MS75084-10	COIL, RF 6.8 UH 10%
L4	L08-0001-001	CHOKE,WIDEBAND
L5	MS14046-7	COIL, RF 18 UH 10%
Q1	Q35-0003-000	XSTR, JFET, HIGH GM
Q2	2N2369	XSTR, SS/RF, NPN
Q3	Q35-0003-000	XSTR, JFET, HIGH GM
Q4	2N2907	XSTR, SS/GP, PNP
Q5	2N2907	XSTR, SS/GP, PNP
Q6	2N2222	XSTR, SS/GP, NPN
Q7	2N2222	XSTR, SS/GP, NPN
Q8	2N2907	XSTR, SS/GP, PNP
Q9	2N2907	XSTR, SS/GP, PNP
Q10	2N2222	XSTR, SS/GP, NPN
Q11	2N5088	XSTR, SS/GP
Q12	2N2222	XSTR, SS/GP, NPN
R1	R65-0003-201	RES,200 5% 1/4W CAR FILM
R2	R65-0003-102	RES,1.0K 5% 1/4W CAR FILM
R3	R65-0003-513	RES,51K 5% 1/4W CAR FILM

Table 3. BFO Assembly A11 Parts List (PL 10073-4600, Rev. R) (Cont.)

Ref. Desig.	Part Number	Description
R4	R65-0003-270	RES,27 5% 1/4W CAR FILM
R5	R65-0003-201	RES,200 5% 1/4W CAR FILM
R6	R65-0003-472	RES,4.7K 5% 1/4W CAR FILM
R7	R65-0003-152	RES,1.5K 5% 1/4W CAR FILM
R8	R65-0003-100	RES,10 5% 1/4W CAR FILM
R9	R65-0003-151	RES,150 5% 1/4W CAR FILM
R10	R65-0003-101	RES,100 5% 1/4W CAR FILM
R11	R65-0003-201	RES,200 5% 1/4W CAR FILM
R12	R65-0003-101	RES,100 5% 1/4W CAR FILM
R13	R65-0003-270	RES,27 5% 1/4W CAR FILM
R14	R65-0003-513	RES,51K 5% 1/4W CAR FILM
R15	R65-0003-102	RES,1.0K 5% 1/4W CAR FILM
R16	R65-0003-562	RES,5.6K 5% 1/4W CAR FILM
R17	RN55D5621F	RES,5620 1% 1/8W MET FLM
R18	R65-0003-562	RES,5.6K 5% 1/4W CAR FILM
R19	R65-0003-561	RES,560 5% 1/4W CAR FILM
R20	RN55D6810F	RES,681.0 1% 1/8W MET FLM
R21	RN55D6810F	RES,681.0 1% 1/8W MET FLM
R22	RN55D9091F	RES,9090 1% 1/8W MET FLM
R23	RN55D3321F	RES,3320 1% 1/8W MET FLM
R24	RN55D6810F	RES,681.0 1% 1/8W MET FLM
R25	RN55D6810F	RES,681.0 1% 1/8W MET FLM
R26	R65-0003-472	RES,4.7K 5% 1/4W CAR FILM
R27	R65-0003-472	RES,4.7K 5% 1/4W CAR FILM
R28	R65-0003-103	RES,10K 5% 1/4W CAR FILM
R29	R65-0003-472	RES,4.7K 5% 1/4W CAR FILM
R30	R65-0003-102	RES,1.0K 5% 1/4W CAR FILM
R31	R65-0003-103	RES,10K 5% 1/4W CAR FILM
R32	R65-0003-103	RES,10K 5% 1/4W CAR FILM
R33	R65-0003-222	RES,2.2K 5% 1/4W CAR FILM
R34	R65-0003-472	RES,4.7K 5% 1/4W CAR FILM
R35	R65-0003-273	RES,27K 5% 1/4W CAR FILM
R36	R65-0003-103	RES,10K 5% 1/4W CAR FILM
R37	R65-0003-472	RES,4.7K 5% 1/4W CAR FILM
R38	R65-0003-102	RES,1.0K 5% 1/4W CAR FILM
R39	R65-0003-151	RES,150 5% 1/4W CAR FILM
R40	R65-0003-750	RES,75 5% 1/4W CAR FILM
R41	R65-0003-103	RES,10K 5% 1/4W CAR FILM
T1	10073-7003	TRANSFORMER
TP1	J-0071	TIP JACK, BROWN
TP2	J-0066	TIP JACK, RED
TP3	J-0069	TIP JACK, ORANGE
TP4	J-0070	TIP JACK, YELLOW
TP5	J-0068	TIP JACK, GREEN
TP6	J-0072	TIP JACK, BLUE

Table 3. BFO Assembly A11 Parts List (PL 10073-4600, Rev. R) (Cont.)

Ref. Desig.	Part Number	Description
U1	I65-0004-001	IC 12013 PLASTIC ECL
U2	I05-0000-090	IC 74LS90 PLASTIC TTL
U3	I05-0000-168	IC 74LS168 PLASTIC TTL
U4	I05-0000-000	IC 74LS00 PLASTIC TTL
U5	I65-0004-001	IC 12013 PLASTIC ECL
U6	I70-0002-001	IC MC145156 PLASTIC CMOS
U7	I01-0000-019	IC 4050B PLASTIC CMOS
U8	I05-0000-000	IC 74LS00 PLASTIC TTL
VR1	I11-0001-001	IC VR 7805 + 5V 1.5A 4%

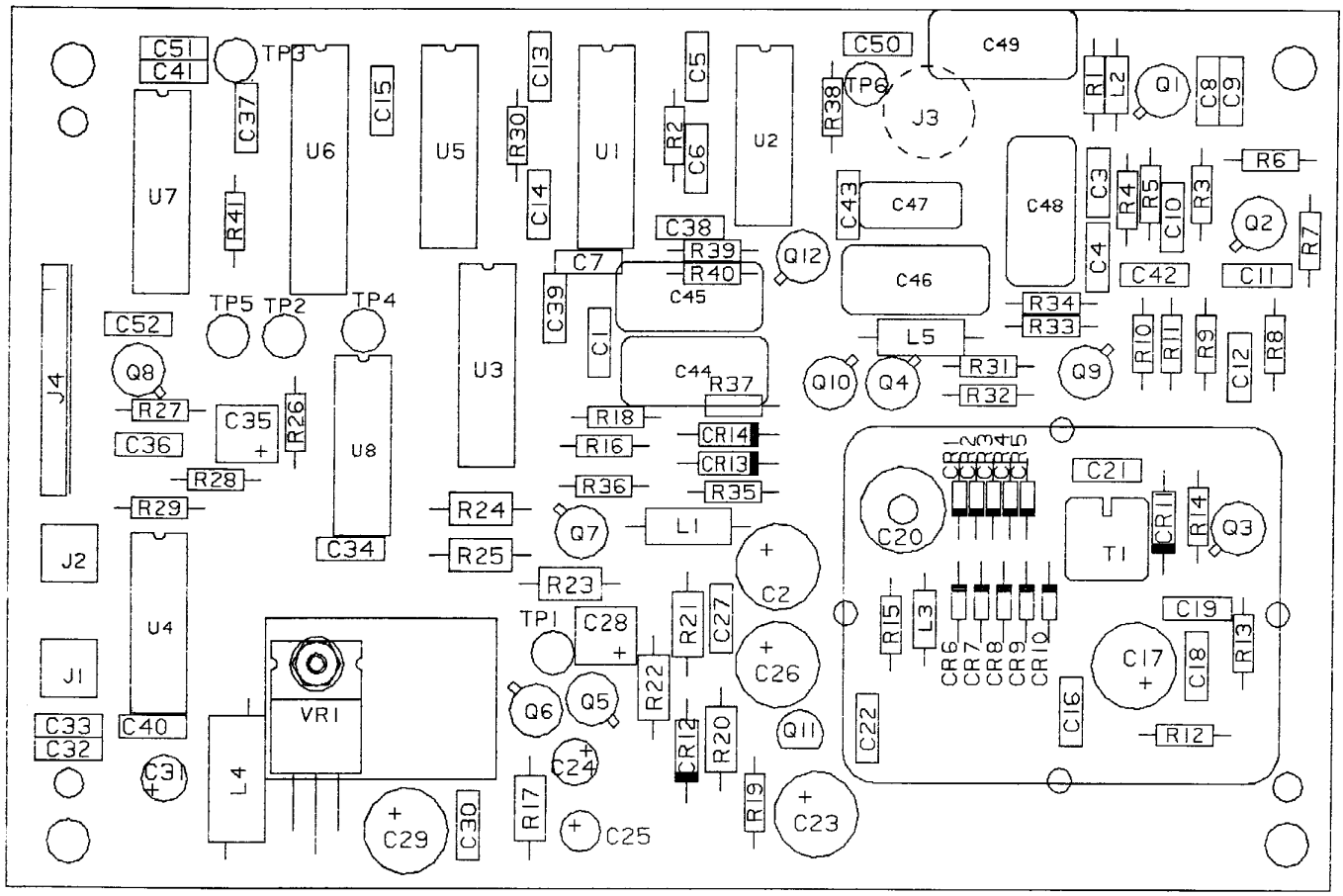


Figure 2. BFO Assembly A11 Component Location Diagram (10073-4600)

NOTE: UNLESS OTHERWISE SPECIFIED:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR A COMPLETE DESIGNATION, PREFIX WITH UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.
2. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, ±5%.
3. ALL CAPACITOR VALUES ARE IN MICROFARADS, 200V.
4. ALL INDUCTOR VALUES ARE IN MICROHENRIES.
5. VENDOR PART NO. CALLOUTS ARE FOR REFERENCE ONLY. COMPONENTS ARE SUPPLIED PER PART NO. IN PARTS LIST.
6. TTL LEVEL IS NORMALLY .6V LOW AND APPROX. 4V HIGH.
7. TOP VIEW OF VR1.

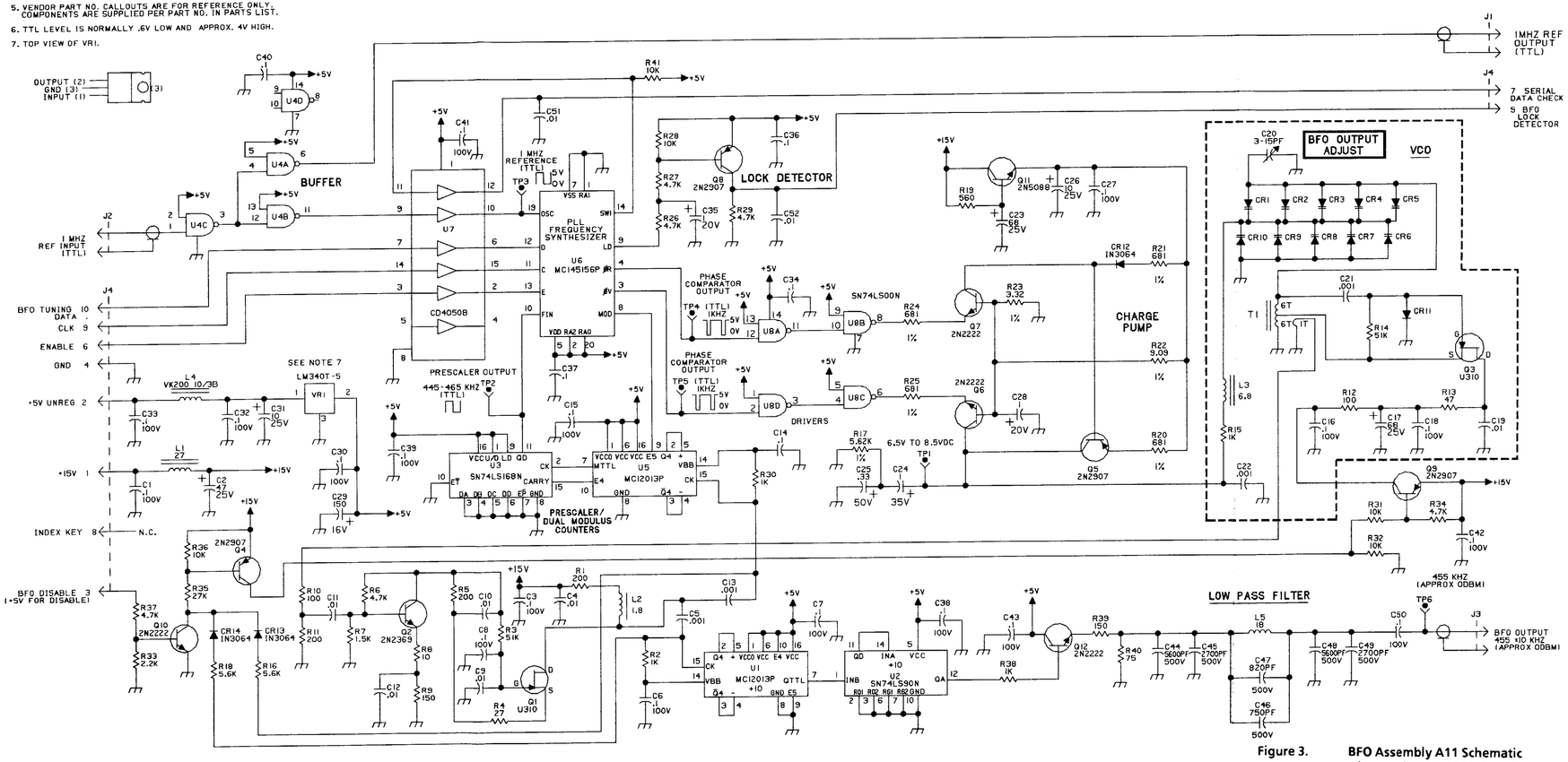
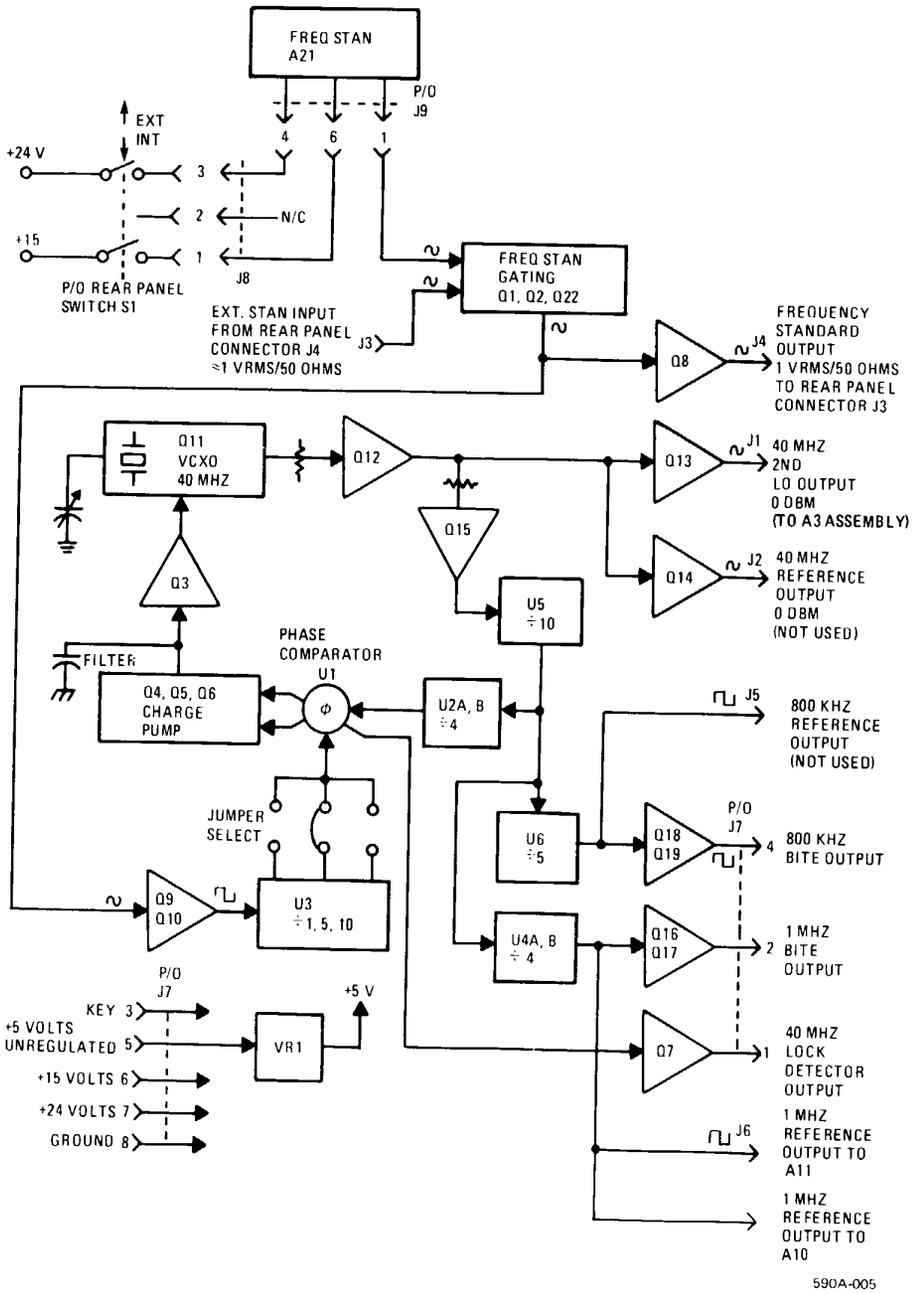


Figure 3. BFO Assembly A11 Schematic Diagram (10073-4601, Rev. G)

A12/A21

REFERENCE GENERATOR ASSEMBLY AND FREQUENCY STANDARD ASSEMBLY



590A-005

TABLE OF CONTENTS

Paragraph		Page
1.	General Description	1
2.	Interface Connections	1
3.	Circuit Description	2
3.1	Frequency Standard Assembly A21	2
3.2	PLL Reference Generation	2
3.2.1	Internal Standard Select	3
3.2.2	External Standard Select	3
3.3	Phase Comparison Circuits	3
3.4	VCXO Operation and Control	3
3.5	A12 Reference Generator Outputs	4
3.6	BITE Circuits	4
4.	Maintenance	4
4.1	40 MHz Outputs Adjustment	4
4.2	A21 Frequency Standard Adjustment	5
4.3	VCO Adjustment	5
5.	Parts List	6
6.	Schematic Diagram	6

LIST OF FIGURES

Figure		Page
1	40 MHz Outputs Adjustments	4
2	A21 Frequency Standard Adjustment	5
3	Reference Generator Assembly A12 Component Location Diagram (10073-4700)	12
4	Reference Generator Assembly A12 Schematic Diagram (10073-4701)	13

LIST OF TABLES

Table		Page
1	Reference Generator A12 Interface Connection	1
2	Reference Generator Assembly A12 Parts List (PL 10073-4700)	7

A12/A21 REFERENCE GENERATOR ASSEMBLY

1. GENERAL DESCRIPTION

Reference Generator Assembly A12 is a single phase locked loop synthesizer which locks to a highly stable frequency standard and derives the various reference frequencies required to accurately control the Receiver.

The frequency standard employed may be either an internal or external standard and is a 1 MHz source.

Frequency Standard Assembly A21 supplied with the radio is a self-contained, sealed unit which plugs directly into the A12 assembly via a nine pin connector. The unit supplied with this Receiver has a stability of $1x10^{-7}$ at 1 MHz.

Since the reference frequencies supplied by the A12 assembly are derived from the frequency standard used, they will have the same accuracy and stability as the standard. The following reference outputs are provided by the A12 assembly for Receiver operation.

- 40 MHz - to Second Converter Assembly A3, 0 dBm
- 1 MHz - to BFO Assembly A11, TTL
- 1 MHz - to Synthesizer Assembly A10, TTL

Additionally, the rear panel contains BNC type connector J6 allowing access to the buffered frequency standard output of 1 V_{rms}/50 ohms. BNC connector J5 provides a 50 ohm input for an external 1 V_{rms} frequency standard. Rear panel switch S1 (INT/EXT standard select) chooses the standard to be used.

2. INTERFACE CONNECTIONS

Table 1 details the A12 input/output connections and other relevant data.

Table 1. Reference Generator A12 Interface Connection

Connector	Function	Characteristics
J1	40 MHz Reference	40 MHz, 0 dBm, 50 ohms (Not Used)
J2	Second LO Output	40 MHz, 0 dBm, 50 ohms
J3	External Standard Input	1 V_{rms}, 50 ohms
J4	Standard Output	1 V_{rms}, 50 ohms
J5	800 kHz Reference Output	TTL (Not Used)
J6	1 MHz Reference Output	TTL
J7-1	40 MHz Lock Detector Output	0 Vdc = PLL Locked
J7-2	1 MHz BITE Output	0 Vdc = 1 MHz ok
J7-3	Key	

Table 1. Reference Generator A12 Interface Connection (Cont.)

Connector	Function	Characteristics
J7-4	800 kHz BITE Output	0 Vdc = 800 kHz ok
J7-5	+ 5 Volts Unregulated	200 mA
J7-6	+ 15 Volts	30 mA
J7-7	+ 24 Volts	10 mA
J7-8	Ground	
J8-1	A21 XTAL Oven Power	+ 24 (draws 100 mA only when 1 x 10^{-8} ppm A21 option is chosen)
J8-2	Key	
J8-3	A21 TCXO Power	+ 15 V, 100 mA
J9-1	Frequency Standard A21 Output	0.5 V_{rms}, 1, 5, or 10 MHz
J9-2	Gnd	
J9-3	Gnd	
J9-4	Same as J8-1	
J9-5	Gnd	
J9-6	Same as J8-3	
J9-7	Spare	
J9-8	Spare	
J9-9	Spare	
J10	1 MHz Reference Output	TTL

3. CIRCUIT DESCRIPTION

Voltage controlled crystal oscillator (VCXO) stage Q11 free runs at 40 MHz and provides all the outputs listed in section 1 after the required buffering and/or frequency division. The VCXO acquires its stability by providing a 1 MHz IF to one port of phase comparator U1 where phase comparison of the 1 MHz reference signal derived from the frequency standard occurs. Any difference in phase and/or frequency between these two signals produces an error signal by the phase comparator which causes the VCXO to tune in the direction which will reduce the error. In so doing, the VCXO frequency of 40 MHz acquires the stability and accuracy of the much lower frequency supplied by the frequency standard.

3.1 Frequency Standard Assembly A21

The frequency standard supplied with the Receiver is a self-contained, sealed unit and plugs directly into A12 connector J9. It has a stability of 1 x 10^{-7} at 1 MHz.

3.2 PLL Reference Generation

Phase comparator U1 obtains a 1.000000 MHz reference signal derived from either an internal or an external frequency standard whose frequency may be 1, 5, or 10 MHz. The rear panel INT/EXT standard select switch S1 chooses the desired source.

3.2.1 Internal Standard Select

When the standard select switch is in the INT position, + 24 volts and + 15 volts are applied via J8 and J9 to Frequency Standard Assembly A21. The + 24 volt line draws no current.

The + 15 volts power the A21 TCXO, and causes a 0.5 V_{rms} signal at the A21 frequency to appear at J9 (Pin 1) RF output. This signal is applied to switch Q2, which is biased on by the + 15 volts. This allows the internal standard signal to pass. Simultaneously, the + 15 volts biases PIN diode CR1 on, which provides a low impedance path to ground for any signals that might be at the J3 external standard input. The signal present at the Q1-Q2 output is applied via buffer Q8 through J4 to the rear panel at a 1 V_{rms}/50 ohm level. It is also applied to limiter stage Q9-Q10 where it is converted to a TTL level to driver U7. U7 in turn drives divide by 1, 5, or 10 counter U3 which produces a constant 1 MHz reference output to U1. The actual divisor ratio depends upon the frequency standard chosen, and is determined by the locations of a jumper wire on the A12 assembly at the U3 output. This jumper is normally factory set.

3.2.2 External Standard Select

When the standard select is in the EXT position, the + 24 and + 15 volts are removed from the A21 assembly turning it off. Simultaneously, + 15 volts is removed from Q2 and CR1 turning them both off. Since the low impedance path to ground caused by CR1 is now a high impedance, signals at J3 from an external standard may pass unattenuated through Q1.

3.3 Phase Comparison Circuits

Phase comparator U1 compares the frequency standard derived 1 MHz reference signal to a VCO derived 1 MHz IF signal. When these two signals are equal in frequency and phase, U1 outputs at TP1 and TP2 are essentially 5 Vdc. This holds all transistors in the charge pump circuit (Q4, Q5, Q6) off. The dc voltage across C16 is constant, Q3 is conducting, and the control voltage developed across R13 at TP1 is constant. This holds the VCO frequency constant and equal to a multiple of the frequency standard.

Assume that the VCO frequency decreases due to temperature variations. This causes the 1 MHz IF frequency to decrease. Comparison at U1, pins 1 and 3, cause TP2 to pulse low, and in so doing, turn on Q6 since the Q6 base-emitter circuit is now forward biased. (Q5 remains off.) Q6 collector voltage drops and forward biases the Q4 base-emitter junction turning Q4 on. Q4 now starts driving charge into C16 raising the C16 potential. This in turn causes Q3 to conduct harder, and the control voltage developed across R13 at TP1 increases. As the control voltage increases, the VCO frequency increases until the IF frequency is again equal to the reference frequency at the U1 inputs. At this point, TP2 switches to + 5 Vdc and equilibrium is obtained. C16 holds this higher dc level to maintain the new higher VCO frequency.

Assume that the VCO frequency increases. This causes the 1 MHz IF frequency to decrease. Comparison at U1, pins 1 and 3, cause TP3 to pulse low, and in so doing, bias Q5 into conduction. (Q6 and Q4 remain off.) C16 now has a low impedance discharge path and charge is drawn out. This drops its voltage. This causes Q3 to conduct less and less control voltage is developed across R13. As this voltage decreases, the VCO frequency decreases until the inputs at U1 are again equal in frequency/phase. At this point, TP3 switches to + 5 Vdc and equilibrium is obtained. C16 holds this lower dc level to maintain the new lower VCO frequency.

3.4 VCXO Operation and Control

A charge pump circuit consisting of Q4, Q5, and Q6 in conjunction with filter network C16, C17, and R14 converts the two phase comparator outputs into an analog dc control voltage. Buffer amplifier Q3 applies this control voltage to varactor diodes CR7 and CR8 in the VCXO. As the capacitance of these diodes change due to control voltage fluctuations, JFET oscillator stage Q11 shifts in frequency. This stage is crystal controlled by U1 and operates at a nominal frequency of 40.000000 MHz. VCXO output passes through

amplifier stages Q12, Q15, and onto divide by 10 counter U5. The 4 MHz from U5 is applied to divide by 4 counter U2 which applies a 1 MHz signal to the second port of phase comparator U1 to complete the feedback loop.

3.5 A12 Reference Generator Outputs

The 40.0000000 MHz from amplifier stage Q12 is amplified to 0 dBm by Q13 and applied through J1 to Second Converter Assembly A3 mixer U1 where it functions as a second local oscillator (LO) for the receiver.

Q12 also feeds amplifier stage Q14 which routes a 40.000000 MHz, 0 dBm signal to J2. This signal is not used in this application.

The 4 MHz from divider U5 is applied to divide by 5 counter U6. U6 TTL output at 800 kHz is not used in this application. U5 also feeds 4 MHz to divide by 4 counter U4. U4 TTL output at 1 MHz is fed through U6 to function as a reference signal for beat frequency oscillator (BFO) Assembly A11, and the Synthesizer Assembly A10.

3.6 BITE Circuits

Q7 monitors the phase comparator (U1) outputs. If either output goes low and remains low for a period of time exceeding the time constant of R19-C19, one of the two diodes (CR5 or CR6) will conduct. This turns Q7 on the develops a + 5 Vdc level indicating an out of lock condition. This immediately flags the BITE monitoring circuits on Control Assembly A14 to display a front panel fault light indicator.

The 800 kHz TTL signals from U6 feed detector stage Q18/Q19 and 1 MHz TTL signals from U4B feed detector stage Q16/Q17. Both these detectors will provide a 0 Vdc level when the 800 kHz and 1 MHz reference signals are present and a + 5 Vdc level when they are not. These two signals are checked only when the receiver BITE self-test is actuated.

4. MAINTENANCE

The following adjustments should not be performed as a routine maintenance procedure, but only when a failure indicates a definite need. All tests are performed with all connections in normal contact unless otherwise specified.

4.1 40 MHz Outputs Adjustment

Perform the following procedure to adjust the 40 MHz outputs.

a. Connect equipment as shown in figure 1.

590A-048

Figure 1. 40 MHz Outputs Adjustments

b. Set receiver controls to the following:

- Frequency to 10.000000 MHz
- Mode to USB
- INT/EXT Standard to INT

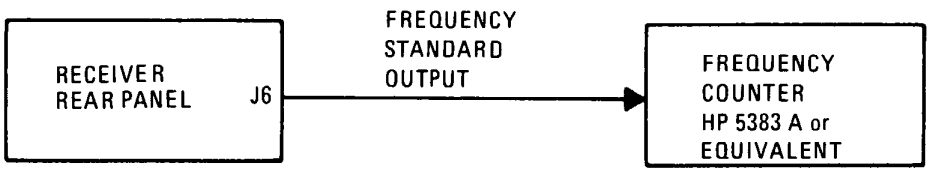
c. Monitoring J1, adjust T3 and then T4 for a peak indication at 40 MHz. (Approximately 0 dBm).

d. Disconnect the spectrum analyzer from J1, connect it to J2, and adjust T5 for a peak indication at 40 MHz. (Approximately 0 dBm.) Test is complete. Disconnect the spectrum analyzer from J2 and reconnect the coaxial cable going to A3.

4.2 A21 Frequency Standard Adjustment

Perform the following procedure to adjust the A21 frequency standard.

a. Connect equipment as shown in figure 2. Set receiver INT/EXT Standard switch to INT.



590A-049

Figure 2. A21 Frequency Standard Adjustment

NOTE

The receiver should be on for at least 60 minutes prior to this alignment.

b. Remove the screw on top of the A21 assembly to gain access to the frequency adjustment. Adjust this control (using a JFD-type nonmetallic alignment tool) to the frequency stamped on top of the assembly. (The accuracy of this setting is crucial to the VCO adjustment so perform this test carefully.)

c. Test is complete. Replace screw in A21 assembly.

4.3 VCO Adjustment

Perform the following procedure to adjust the VCO.

a. Make sure that the INT/EXT Standard switch is in the INT position and that the A21 frequency standard is properly adjusted on frequency.

b. Monitor TP1 with a digital voltmeter. Adjust C36 for 7.4 Vdc. Test is complete.

5. PARTS LIST

Table 2 is a comprehensive parts list of all replaceable components in Reference Generator Assembly A12. When ordering parts from the factory, include a full description of the part. Use figure 3, Reference Generator Assembly A12 component location diagram to identify parts.

6. SCHEMATIC DIAGRAM

Figure 4 is the Reference Generator Assembly A12 schematic diagram.

Table 2. Reference Generator Assembly A12 Parts List (PL 10073-4700, Rev. AB)

Ref. Desig.	Part Number	Description
C1	M39014/02-1320	CAP .47UF 10% 50V CER-R
C2	M39014/02-1320	CAP .47UF 10% 50V CER-R
C3	M39014/02-1310	CAP .1UF 10% 100V CER-R
C4	C26-0025-339	CAP 3.3UF 20% 25V TANT
C5	M39014/02-1310	CAP .1UF 10% 100V CER-R
C6	C26-0025-339	CAP 3.3UF 20% 25V TANT
C7	M39014/02-1310	CAP .1UF 10% 100V CER-R
C8	C26-0025-339	CAP 3.3UF 20% 25V TANT
C9	M39014/01-1535	CAP .01UF 10% 100V CER-R
C10	M39014/02-1310	CAP .1UF 10% 100V CER-R
C11	M39014/02-1310	CAP .1UF 10% 100V CER-R
C12	M39014/02-1310	CAP .1UF 10% 100V CER-R
C13	C26-0035-100	CAP 10UF 20% 35V TANT
C14	M39014/02-1310	CAP .1UF 10% 100V CER-R
C15	C26-0035-470	CAP 47UF 20% 35V TANT
C16	C26-0025-339	CAP 3.3UF 20% 25V TANT
C17	M39014/02-1310	CAP .1UF 10% 100V CER-R
C18	M39014/02-1310	CAP .1UF 10% 100V CER-R
C19	C25-0001-301	CAP 1.0UF 20% 20V TANT
C20	C26-0025-339	CAP 3.3UF 20% 25V TANT
C21	M39014/02-1310	CAP .1UF 10% 100V CER-R
C22	M39014/02-1310	CAP .1UF 10% 100V CER-R
C23	M39014/02-1310	CAP .1UF 10% 100V CER-R
C24	M39014/02-1310	CAP .1UF 10% 100V CER-R
C25	M39014/02-1310	CAP .1UF 10% 100V CER-R
C26	M39014/02-1310	CAP .1UF 10% 100V CER-R
C27	M39014/02-1310	CAP .1UF 10% 100V CER-R
C28	M39014/02-1310	CAP .1UF 10% 100V CER-R
C29	M39014/02-1310	CAP .1UF 10% 100V CER-R
C30	CK05BX102K	CAP 1000PF 10% 200V CER
C31	CK05BX102K	CAP 1000PF 10% 200V CER
C32	M39014/02-1310	CAP .1UF 10% 100V CER-R
C33	C26-0025-680	CAP 68UF 20% 25V TANT
C34	M39014/01-1535	CAP .01UF 10% 100V CER-R
C35	CM04CD150J03	CAP 15PF 5% 500V MICA
C36	C85-0001-002	CAP VAR 1-10PF PIST
C37	M39014/01-1535	CAP .01UF 10% 100V CER-R
C38	M39014/01-1535	CAP .01UF 10% 100V CER-R
C39	CM04ED470J03	CAP 47PF 5% 500V MICA
C40	M39014/01-1535	CAP .01UF 10% 100V CER-R
C41	M39014/02-1310	CAP .1UF 10% 100V CER-R
C42	M39014/01-1535	CAP .01UF 10% 100V CER-R
C43	M39014/02-1310	CAP .1UF 10% 100V CER-R
C44	M39014/01-1535	CAP .01UF 10% 100V CER-R

Table 2. Reference Generator Assembly A12 Parts List (PL 10073-4700, Rev. AA) (Cont.)

Ref. Desig.	Part Number	Description
C45	CM04ED560J03	CAP 56PF 5% 500V MICA
C46	M39014/01-1535	CAP .01UF
C47	M39014/01-1535	CAP .01UF
C48	M39014/01-1535	CAP .01UF
C49	M39014/01-1535	CAP .01UF
C50	M39014/02-1310	CAP .1 UF
C51	M39014/01-1535	CAP .01UF
C52	CM04ED560J03	CAP 56PF 5% 500V MICA
C53	M39014/01-1535	CAP .01UF
C54	M39014/01-1535	CAP .01UF
C55	M39014/02-1310	CAP .1 UF
C56	M39014/01-1535	CAP .01UF
C57	M39014/01-1535	CAP .01UF
C58	M39014/01-1535	CAP .01UF
C59	M39014/02-1310	CAP .1 UF
C60	M39014/02-1310	CAP .1 UF
C61	M39014/02-1310	CAP .1 UF
C62	M39014/02-1310	CAP .1 UF
C63	M39014/02-1310	CAP .1 UF
C64	M39014/02-1310	CAP .1 UF
C65	C26-0016-151	CAP,150UF,16V
C66	M39014/02-1310	CAP .1 UF
C67	M39014/02-1310	CAP .1 UF
C68	C26-0025-100	CAP, TANT, 10UF, 25V
C69	M39014/02-1310	CAP .1 UF
C70	M39014/02-1310	CAP .1 UF
C71	C26-0050-100	CAP,FXD,ELCTLT,10 UF,50
C72	M39014/02-1310	CAP .1 UF
C73	M39014/02-1310	CAP .1 UF
C74	C26-0025-470	CAP,TANT,47UF,25V
C75	M39014/02-1310	CAP .1 UF
C76	CK05BX102K	CAP 1000PF 10% 200V CER
C77	M39014/01-1535	CAP .01UF
C78	M39014/02-1310	CAP .1 UF
C79	CK05BX102K	CAP 1000PF 10% 200V CER
C80	M39014/01-1535	CAP .01UF
C81	M39014/01-1535	CAP .01UF
C82	M39014/02-1310	CAP .1 UF
C83	M39014/02-1310	CAP .1 UF
C84	M39014/01-1535	CAP .01UF
C85	M39014/01-1535	CAP .01UF
C86	M39014/01-1535	CAP .01UF
C87	10121-4720	CAP.,TEMP,COMP,10
CR1	D12-0007-001	DIODE UM9301
CR2	1N3064	DIODE

Table 2. Reference Generator Assembly A12 Parts List (PL 10073-4700, Rev. AB) (Cont.)

Ref. Desig.	Part Number	Description
CR3	1N3064	DIODE 75mA 75V SW
CR4	1N3064	DIODE 75mA 75V SW
CR5	1N3064	DIODE 75mA 75V SW
CR6	1N3064	DIODE 75mA 75V SW
CR7	10073-7118	DIODE VARACTOR
CR8	10073-7118	DIODE VARACTOR
CR9	1N3064	DIODE 75mA 75V SW
CR10	1N3064	DIODE 75mA 75V SW
J1	J-0031	CONN SMB VERT PCB F
J2	J-0031	CONN SMB VERT PCB F
J3	J-0031	CONN SMB VERT PCB F
J4	J-0031	CONN SMB VERT PCB F
J5	J-0031	CONN SMB VERT PCB F
J6	J-0031	CONN SMB VERT PCB F
J7	J46-0032-008	HDR 8 PIN 0.100" SR
J8	J46-0022-003	HDR 3 PIN 0.100" SR LKG
J9	10073-7045	CONNECTOR, 9 PIN
J10	J-0031	CONN SMB VERT PCB F
L1	MS75085-7	COIL 100UH 10% FXD RF
L2	MS75085-7	COIL 100UH 10% FXD RF
L3	MS75084-12	COIL 10UH 10% FXD RF
L4	MS75083-7	COIL .33UH 10% FXD RF
L5	MS75084-12	COIL 10UH 10% FXD RF
L6	MS75084-5	COIL 2.7UH 10% FXD RF
L7	MS75084-12	COIL 10UH 10% FXD RF
L8	MS75084-12	COIL 10UH 10% FXD RF
L9	MS75085-7	COIL 100UH 10% FXD RF
L10	MS75084-12	COIL 10UH 10% FXD RF
L11	L08-0001-001	CHOKE W B 50 MHZ
L12	L08-0001-001	CHOKE W B 50 MHZ
L13	L08-0001-001	CHOKE W B 50 MHZ
L14	MS75084-3	COIL 1.8UH 10% FXD RF
Q1	2N3227	XSTR SS/GP NPN TO-18
Q2	2N3227	XSTR SS/GP NPN TO-18
Q3	Q05-0001-000	XSTR JFET N-CH
Q4	2N2907	XSTR SS/GP PNP TO-18
Q5	2N2222	XSTR SS/GP NPN TO-18
Q6	2N2222	XSTR SS/GP NPN TO-18
Q7	2N2907	XSTR SS/GP PNP TO-18
Q8	2N3866	XSTR SS/RF NPN TO-39
Q9	Q-0153	XSTR SS/RF PN4258
Q10	2N2369	XSTR SS/RF NPN
Q11	Q35-0003-000	XSTR N-CH JFET U310
Q12	Q35-0003-000	XSTR N-CH JFET U310
Q13	Q35-0003-000	XSTR N-CH JFET U310

Table 2. Reference Generator Assembly A12 Parts List (PL 10073-4700, Rev. AB) (Cont.)

Ref. Desig.	Part Number	Description
Q14	Q35-0003-000	XSTR N-CH JFET U310
Q15	Q35-0003-000	XSTR N-CH JFET U310
Q16	2N2907	XSTR SS/GP PNP TO-18
Q17	2N2222	XSTR SS/GP NPN TO-18
Q18	2N2907	XSTR SS/GP PNP TO-18
Q19	2N2222	XSTR SS/GP NPN TO-18
R1	R65-0003-471	RES 470 5% 1/4W CAR FILM
R2	R65-0003-471	RES 470 5% 1/4W CAR FILM
R3	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R4	R65-0003-101	RES 100 5% 1/4W CAR FILM
R5	R65-0003-272	RES 2.7K 5% 1/4W CAR FILM
R6	R65-0003-620	RES 62 5% 1/4W CAR FILM
R7	R65-0003-561	RES 560 5% 1/4W CAR FILM
R8	R65-0003-152	RES 1.5K 5% 1/4W CAR FILM
R9	R65-0003-272	RES 2.7K 5% 1/4W CAR FILM
R10	RN55D6810F	RES 681 1% 1/8W MET FLM
R11	R65-0003-101	RES 100 5% 1/4W CAR FILM
R12	RN55D6810F	RES 681 1% 1/8W MET FLM
R13	R65-0003-272	RES 2.7K 5% 1/4W CAR FILM
R14	RN55D2211F	RES 2210 1% 1/8W MET FLM
R15	RN55D6810F	RES 681 1% 1/8W MET FLM
R16	RN55D2002F	RES 20.0K 1% 1/8W MET FLM
R17	RN55D3321F	RES 3320 1% 1/8W MET FLM
R18	RN55D6810F	RES 681 1% 1/8W MET FLM
R19	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R20	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R21	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R22	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R23	R65-0003-100	RES 10 5% 1/4W CAR FILM
R24	R65-0003-201	RES 200 5% 1/4W CAR FILM
R25	R65-0003-272	RES 2.7K 5% 1/4W CAR FILM
R26	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R27	R65-0003-180	RES 18 5% 1/4W CAR FILM
R28	R65-0003-470	RES 47 5% 1/4W CAR FILM
R29	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R30	R65-0003-562	RES 5.6K 5% 1/4W CAR FILM
R31	R65-0003-241	RES 240 5% 1/4W CAR FILM
R32	R65-0003-270	RES 27 5% 1/4W CAR FILM
R33	R65-0003-331	RES 330 5% 1/4W CAR FILM
R34	R65-0003-332	RES 3.3K 5% 1/4W CAR FILM
R35	R65-0003-391	RES 390 5% 1/4W CAR FILM
R36	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R37	R65-0003-201	RES 200 5% 1/4W CAR FILM
R38	R65-0003-201	RES 200 5% 1/4W CAR FILM
R39	R65-0003-101	RES 100 5% 1/4W CAR FILM

Table 2. Reference Generator Assembly A12 Parts List (PL 10073-4700, Rev. AB) (Cont.)

Ref. Desig.	Part Number	Description
R40	R65-0003-201	RES 200 5% 1/4W CAR FILM
R42	R65-0003-101	RES 100 5% 1/4W CAR FILM
R44	R65-0003-201	RES 200 5% 1/4W CAR FILM
R45	R65-0003-751	RES 750 5% 1/4W CAR FILM
R46	R65-0003-751	RES 750 5% 1/4W CAR FILM
R47	R65-0003-201	RES 200 5% 1/4W CAR FILM
R49	R65-0003-101	RES 100 5% 1/4W CAR FILM
R50	R65-0003-201	RES 200 5% 1/4W CAR FILM
R51	R65-0003-101	RES 100 5% 1/4W CAR FILM
R52	R65-0003-101	RES 100 5% 1/4W CAR FILM
R53	R65-0003-201	RES 200 5% 1/4W CAR FILM
R54	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R55	R65-0003-510	RES 51 5% 1/4W CAR FILM
R56	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R57	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R58	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R59	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R60	R65-0003-222	RES 2.2K 5% 1/4W CAR FILM
R61	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R62	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R63	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R64	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R65	R65-0003-222	RES 2.2K 5% 1/4W CAR FILM
R66	R65-0003-224	RES 220K 5% 1/4W CAR FILM
T1	10073-7006	TRANSFORMER, RF, FIXED
T2	10073-7007	TRANSFORMER, RF, FIXED
T3	10073-7009	TRANSFORMER, RF, VARIABLE
T4	10073-7009	TRANSFORMER, RF, VARIABLE
T5	10073-7009	TRANSFORMER, RF, VARIABLE
TP1	J-0071	TP PWB BRN TOP ACCS .080"
TP2	J-0066	TP PWB RED TOP ACCS .080"
TP3	J-0069	TP PWB ORN TOP ACCS .080"
TP4	J-0070	TP PWB YEL TOP ACCS .080"
TP5	J-0068	TP PWB GRN TOP ACCS .080"
U1	IC-0430	IC 4044 PLASTIC CMOS
U2	I05-0000-074	IC 74LS74A PLASTIC TTL
U3	I05-0000-090	IC 74LS90 PLASTIC TTL
U4	I05-0000-074	IC 74LS74A PLASTIC TTL
U5	I65-0004-001	IC PRESCALER 10/11 12013
U6	I05-0000-090	IC 74LS90 PLASTIC TTL
U7	I05-0000-000	IC 74LS00 PLASTIC TTL
VR1	I11-0001-001	IC VR 7805 +5V 1.5A 4%
Y1	10073-4720	CRYSTAL, 40 MHZ

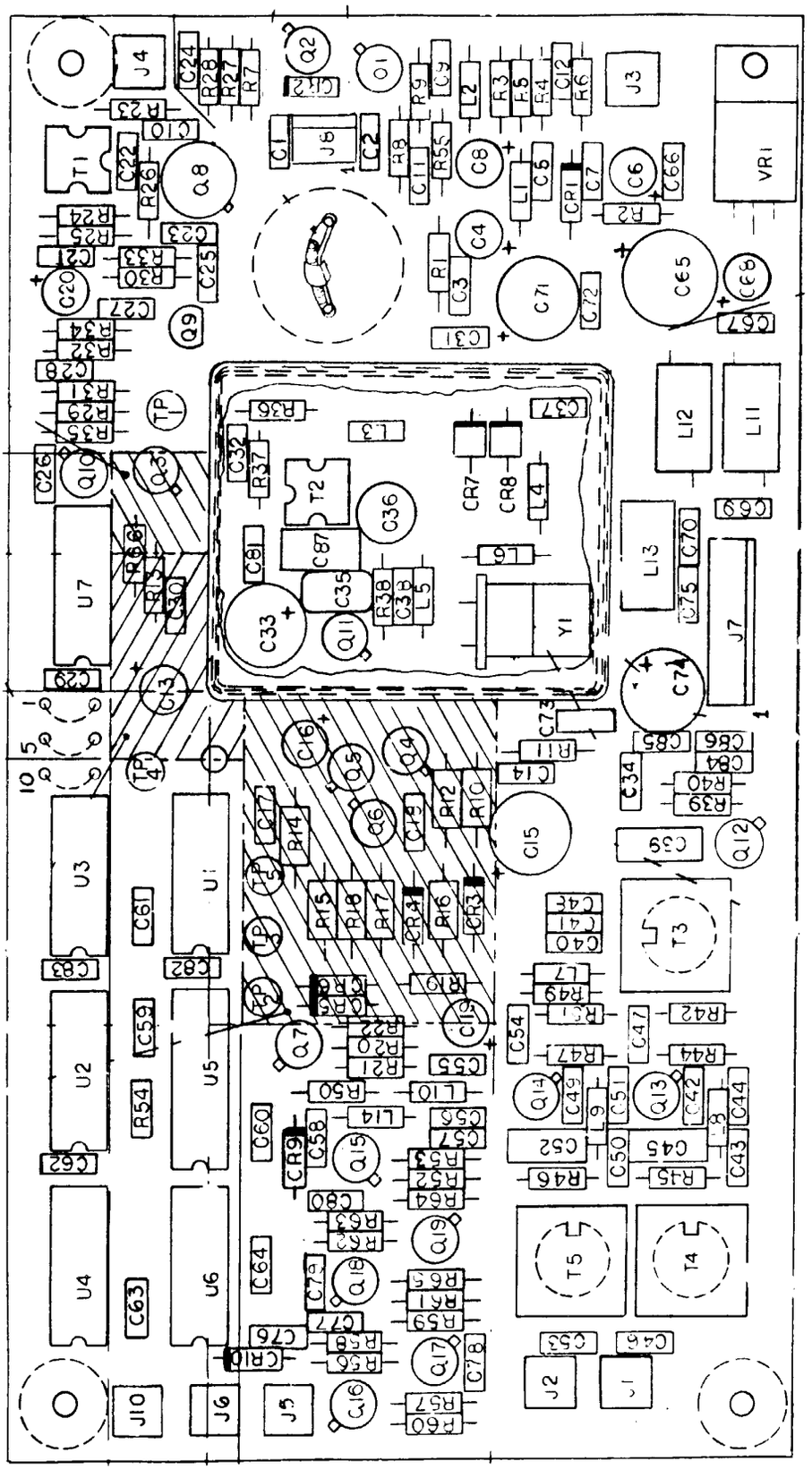
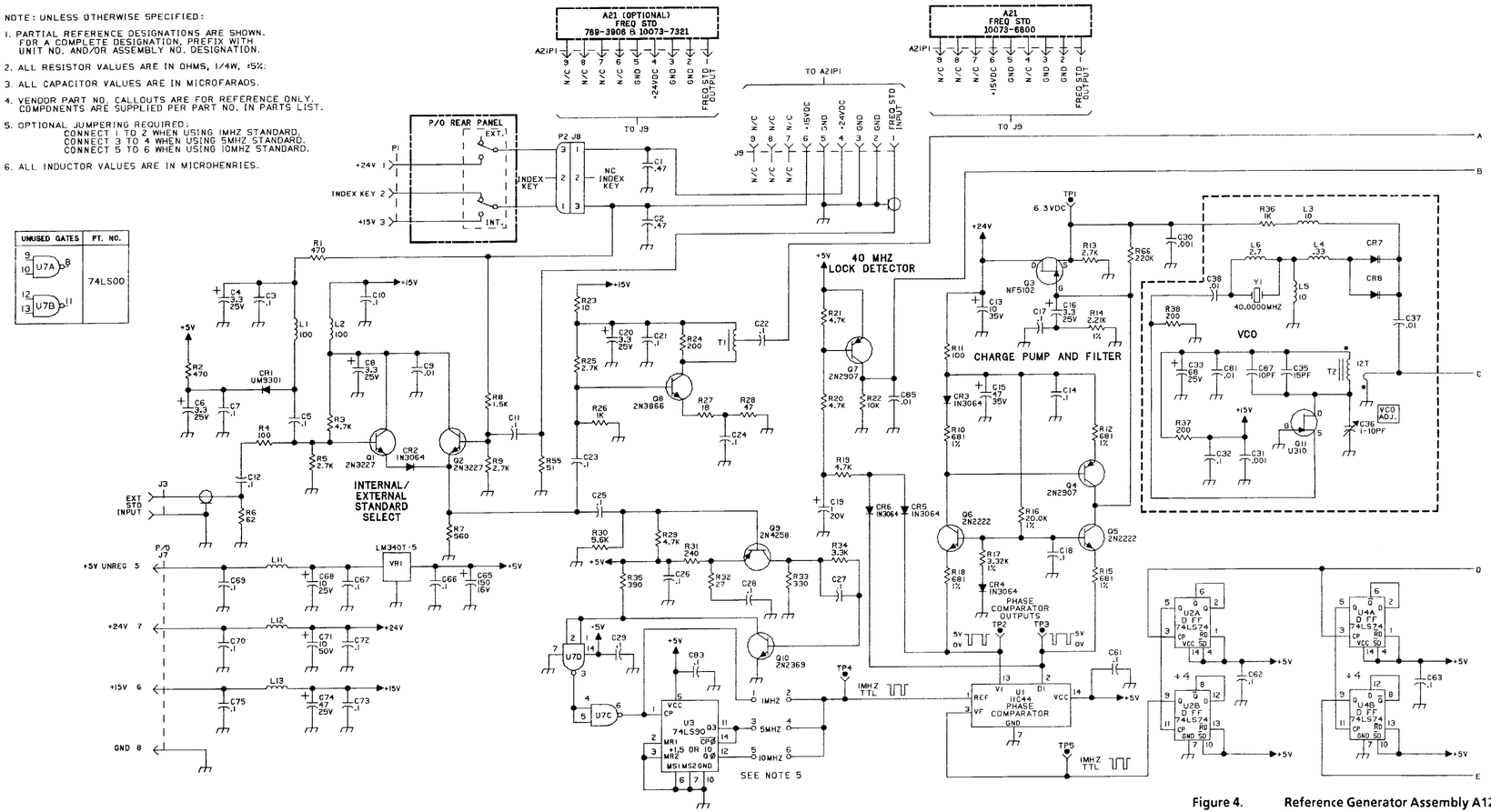


Figure 3. Reference Generator Assembly A12 Component Location Diagram (10073-4700, Rev. F)


NOTE: UNLESS OTHERWISE SPECIFIED:
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR A COMPLETE DESIGNATION, PREFIX WITH UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.
2. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, ±5%.
3. ALL CAPACITOR VALUES ARE IN MICROFARADS.
4. VENDOR PART NO. CALLOUTS ARE FOR REFERENCE ONLY. COMPONENTS ARE SUPPLIED PER PART NO. IN PARTS LIST.
5. OPTIONAL JUMPERING REQUIRED:
CONNECT 1 TO 2 WHEN USING 1MHZ STANDARD.
CONNECT 3 TO 4 WHEN USING 5MHZ STANDARD.
CONNECT 5 TO 6 WHEN USING 10MHZ STANDARD.
6. ALL INDUCTOR VALUES ARE IN MICROHENRIES.
UNUSED GATES
PT. NO.
74LS00
A21 (OPTIONAL) FREQ STD 789-3908 & 10073-7321
A21 FREQ STD 10073-6600
TO A2P1
TO J9
P/O REAR PANEL
EXT.
INT.
INDEX KEY
NC INDEX KEY
40 MHZ LOCK DETECTOR
CHARGE PUMP AND FILTER
VCO
INTERNAL/ EXTERNAL STANDARD SELECT
PHASE COMPARATOR OUTPUTS
SEE NOTE 5
Figure 4. Reference Generator Assembly A12 Schematic Diagram (10073-4701, Rev. K) (Sheet 1 of 2)

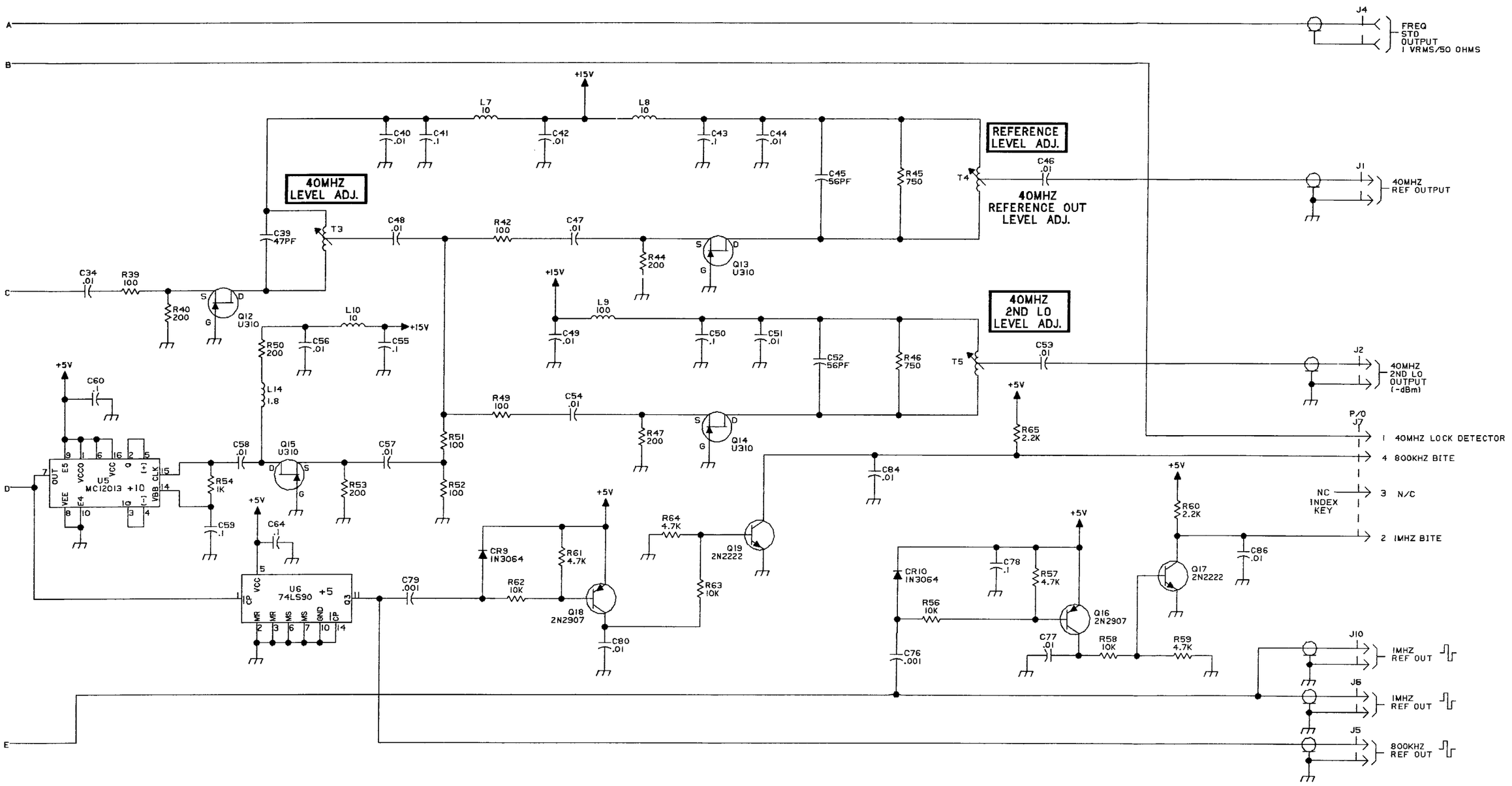
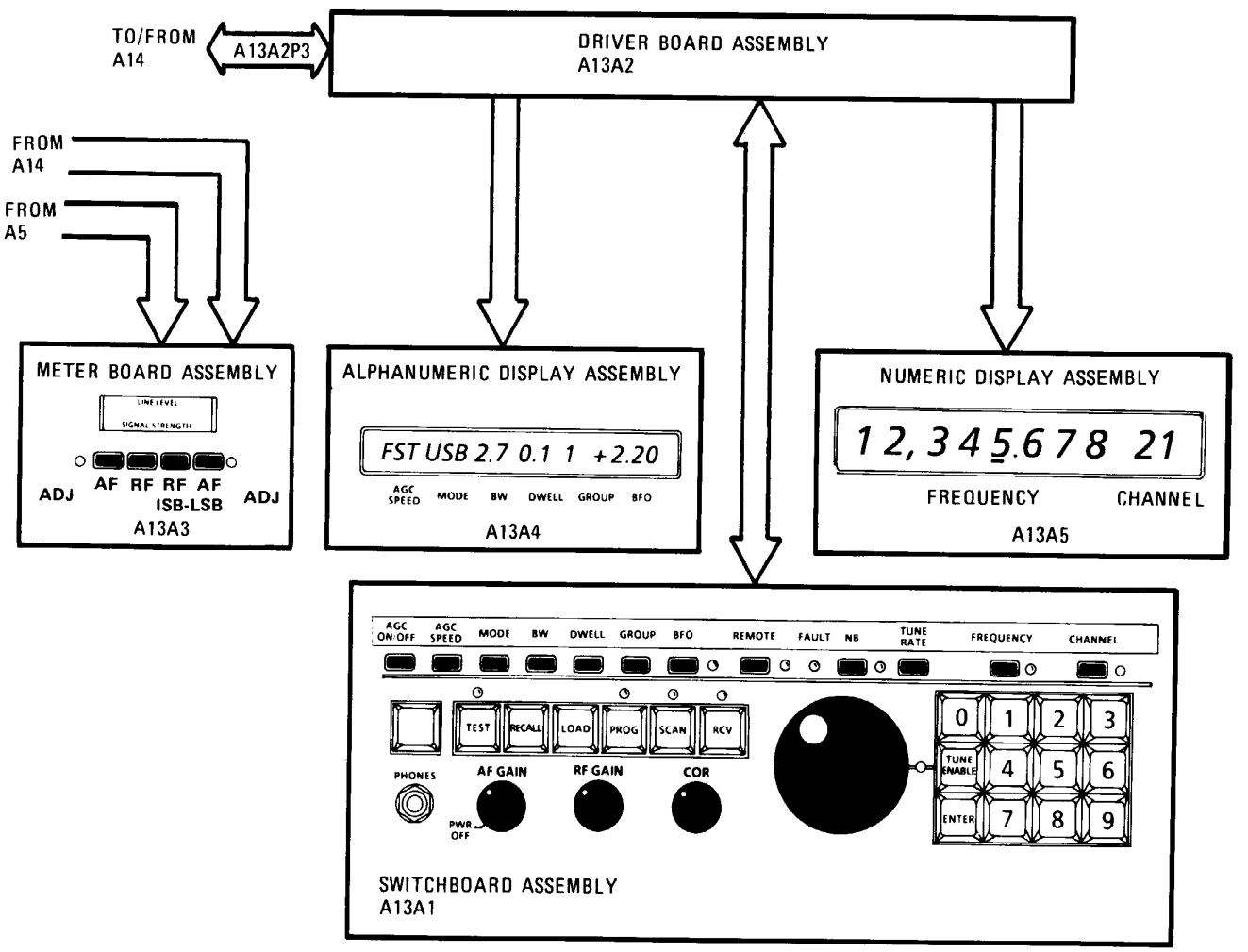


Figure 4. Reference Generator Assembly A12 Schematic Diagram (10073-4701, Rev. K) (Sheet 2 of 2)

A13
FRONT PANEL ASSEMBLY



URR-024

TABLE OF CONTENTS

Paragraph		Page
1.	Front Panel Assembly A13	1
2.	Front Panel Switchboard A13A1	4
2.1	General Description	4
2.2	Interface Connections	4
2.3	Functional Description	5
2.3.1	Switch Matrix	5
2.3.2	LED Circuits	5
2.4	Maintenance	5
3.	Front Panel Driver Board A13A2	13
3.1	General Description	13
3.2	Interface Connections	13
3.3	Circuit Description	13
3.3.1	Microprocessor Operation	13
3.3.2	Display Data Input	20
3.3.3	Vacuum Fluorescent Display Drive	20
3.3.4	LED Drive	20
3.3.5	Tuning Wheel	21
3.3.6	Pushbutton Circuitry	21
3.3.7	Converter Module	21
3.4	Maintenance	21
3.4.1	Adjustments	21
3.4.2	Troubleshooting	21
3.5	Parts List and Schematic Diagram	22
4.	Front Panel Meter Board A13A3	31
4.1	General Description	31
4.2	Interface Connections	31
4.3	Circuit Description	31
4.3.1	Meter Control	31
4.3.2	Line Level Control	31
4.3.3	Front Panel Control Signals	34
4.3.4	Parts Lists and Schematic Diagram	34
5.	Alphanumeric Display Assembly A13A4	39
5.1	General Description	39
5.2	Interface Connections	39
5.3	Functional Description	40
5.3.1	Parts List and Schematic Diagram	40
6.	Numeric Display Assembly A13A5	44
6.1	General Description	44
6.2	Interface Connections	44
6.3	Functional Description	45
6.3.1	Parts List and Schematic Diagram	45

LIST OF FIGURES

Figure		Page
1	Front Panel A13 (Front View)	1
2	Front Panel Assembly A13 (Rear View)	2
3	Front Panel Switchboard A13A1 Component Location Diagram (10073-2700)	9
4	Front Panel Switchboard A13A1 Schematic Diagram (10073-2701)	11
5	Front Panel Driver Board A13A2 Functional Block Diagram	15
6	Driver Board A13A2 Component Location Diagram (10215-2200)	25
7	Driver Board A13A2 Schematic Diagram (10215-2201)	27
8	Front Panel Meter Board A13A3 Functional Block Diagram	32
9	Front Panel Meter Board A13A3 Component Location Diagram (10073-2300)	36
10	Front Panel Meter Board A13A3 Schematic Diagram (10073-2301)	37
11	Alphanumeric Display Segment Location	41
12	Alphanumeric Display Board A13A4 Component Location Diagram (10073-2400)	42
13	Alphanumeric Display Board A13A4 Schematic Diagram (10073-2401)	43
14	Numeric Display Segment Location	45
15	Numeric Display Board A13A5 Component Location Diagram (10073-2500)	46
16	Numeric Display Board A13A5 Schematic Diagram (10073-2501)	47

LIST OF TABLES

Table		Page
1	Front Panel Assembly A13 Parts List (PL 10215-2010)	3
2	A13A1 Switchboard Interface Connections	4
3	A13A1 Switchboard LED Indicators	6
4	Front Panel Switchboard A13A1 Parts List (PL 10073-2700)	7
5	A13A2 Driver Board Interface Connections	17
6	Driver Board A13A2 Parts List (PL 10215-2200)	22
7	A13A3 Interface Connections	33
8	Front Panel Meter Board A13A3 Parts List (PL 10073-2300)	35
9	A13A4 Interface Connections	39
10	Alphanumeric Display Assembly A13A4 Parts List (PL 10073-2400)	41
11	A13A5 Interface Connections	44
12	Numeric Display Assembly A13A5 Parts List (PL 10073-2500)	45

A13 FRONT PANEL ASSEMBLY

1. FRONT PANEL ASSEMBLY A13

The Front Panel Assembly A13 contains control circuits which permit all operator-receiver local interface functions such as tuning, channel selection, AF gain, system status indications, etc.

All operator controls (AF Gain, Squelch, Keypad, tuning wheel, etc) are accessed from the front of the assembly. Paragraphs 3.2.1 through 3.2.6 of the Operations section detail the locations and functions of these controls, and figure 1 is a photograph of the front panel (included for reference).

URR-025P

Figure 1. Front Panel A13 (Front View)

Five major interface assemblies are mounted to the rear of the Front Panel Assembly. They are shown in figure 2. These assemblies are described in section 2 through 7 and listed below.

- Switch Board A13A1
- Driver Board A13A2
- Meter Board A13A3
- Display Board (Alphanumeric) A13A4
- Display Board (Numeric) A13A5

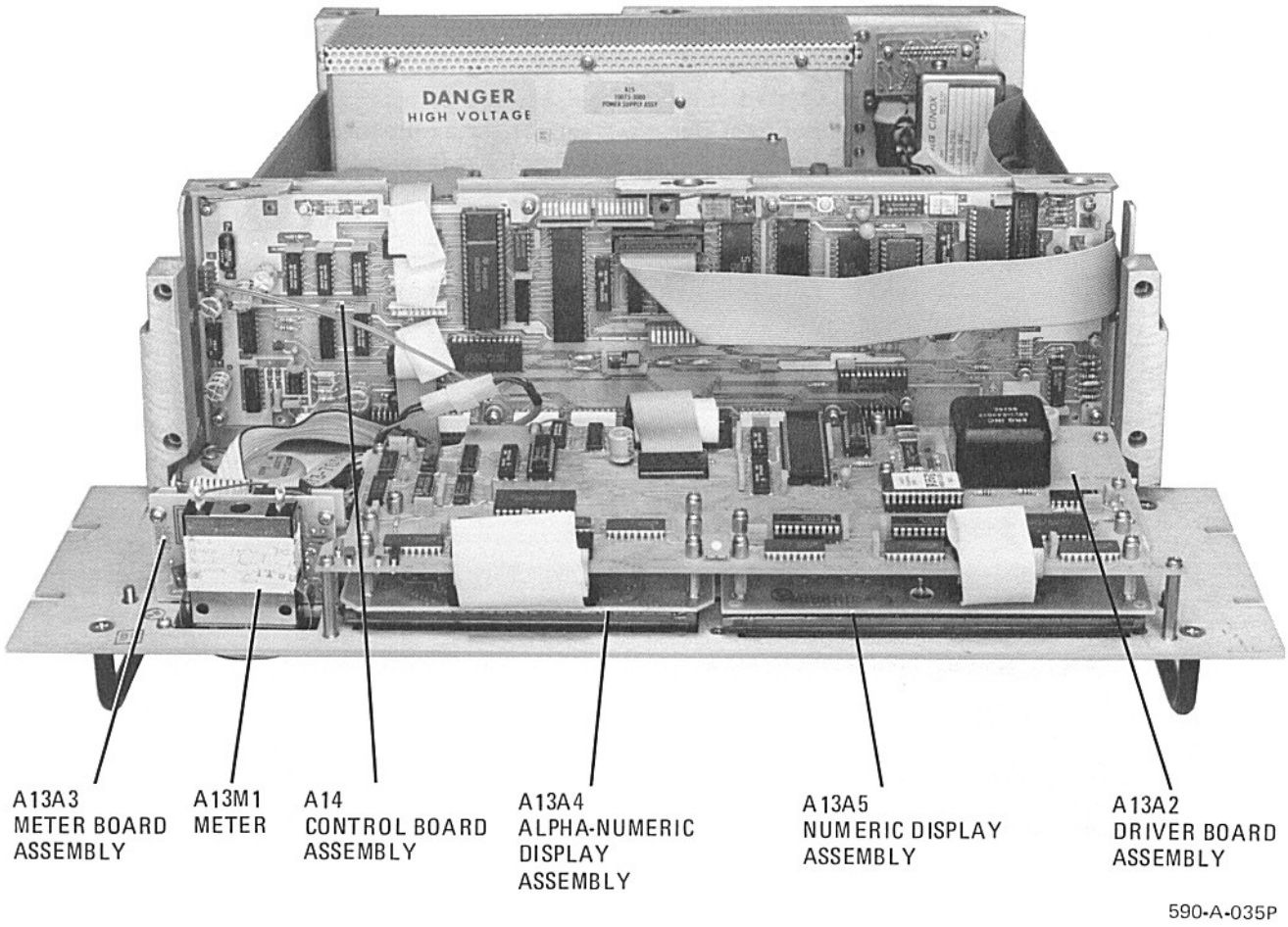


Figure 2. Front Panel Assembly A13 (Rear View)

The Front Panel Assembly is normally secured to the chassis by four front panel captive screws. Loosening these screws allows the entire assembly to pivot down on hinges (located at two corners). This permits access to any of the items listed above as well as to Control Assembly A14 which is mounted behind the front panel.

Table 1 is the Front Panel Assembly A13 parts list.

Table 1. Front Panel Assembly A13 Parts List (PL 10215-2010, Rev. K)

Ref. Desig.	Part Number	Description
--	Z03-0001-004	HDL ALUM BLK 10-32X4.00IN
--	Z03-0004-002	FER ALUM BLK .221 I.D.
--	10073-2506	KNOB
--	MP-1481	KNOB .713 DIA PLASTIC
--	10143-2007	SPEAKER GRILL
--	P05-0003-005	TAPE,FM,CL CELL,3/32X1/2
--	10215-2008	WINDOW,SHIELD
A1	10073-2700-02	SWITCH/LED ASSY
A2	10215-2200	PWB ASSY,FRONT P
A3	10073-2300	METER PWB ASSY
A4	10073-2400	ASSY ALPHNUMERIC DISPLAY
A5	10073-2500	ASSY 7 SEG DISPLAY PWB
G1	S85-0001-001	OPTICAL ENCODER
J1	J62-0001-007	JACK PHONE CLOSED CKT
M1	10215-2311	METER
P1	J46-0016-014	CONN HOUSING 14 POS 24AWG
P3	MP-0648	HOUSING CONN 5 CIRCUIT
P4	J40-0002-003	HOUSING CONN 3 CIRCUIT
P5	J40-0002-002	HOUSING CONN 2 PIN
P6	MP-0647	HOUSING CONN 6 CIRCUIT
R1	10073-2071	RES VARIABLE
R2	10073-2073	RES VAR 5K 10% LIN.TAPER
R3	10073-2072	RES VAR 5K 10% MOD.LOG

2. FRONT PANEL SWITCHBOARD A13A1

2.1 General Description

Front Panel switchboard A13A1 consists of all front panel pushbutton switches excluding the four-position meter select switch. It also includes all the discrete LED displays on the receiver front panel. Signals generated by switch closures are routed for processing to Control Assembly A14 via Front Panel Driver Board A13A2. The discrete LED displays are also driven from Front Panel Driver Board A13A2.

2.2 Interface Connections

Table 2 lists Front Panel Switchboard A13A1 interface connections.

Table 2. A13A1 Switchboard Interface Connections

Connector	Description
J1 to/from A13A2	
J1-1	Gnd
J1-2	Scan LED
J1-3	Test LED
J1-4	Program LED
J1-5	COL 7
J1-6	Receive LED
J1-7	BFO LED
J1-8	Fault LED
J1-9	PB3
J1-10	Remote LED
J1-11	TWA
J1-12	TWB
J1-13	COL 2
J1-14	COL 0
J1-15	Tune Enable LED
J1-16	PB2
J1-17	COL 3
J1-18	N/C
J1-19	COL 5
J1-20	PB1
J1-21	N/C
J1-22	N/C
J1-23	COL 1
J1-24	Frequency LED

Table 2. A13A1 Switchboard Interface Connections (Cont.)

Connector	Description
J1-25	N/C
J1-26	COL 6
J1-27	PB0
J1-28	COL 4
J1-29	Channel LED
J1-30	+ 5 V
J2 to/from Shaft Encoder	
J2-1	Gnd
J2-2	TWB
J2-3	Key
J2-4	TWA
J2-5	+ 5 V
J3 to/from A13A3	
J3-1	N/C
J3-2	N/C
J3-3	N/C
J3-4	N/C

2.3 Functional Description

2.3.1 Switch Matrix

The pushbutton switches on the Receiver front panel are arranged in a matrix of eight columns by four rows. The eight column signals (COL 0 through COL 7) are inputs from Front Panel Driver Board A13A2 while the four row signals are outputs to the Driver board. The microprocessor on the Control Assembly detects switch activity by enabling all the column outputs while reading back the row inputs (PB0-PB3) looking for a connection between any row and any column. If a closure is detected, it enables the column lines selectively while reading back the row lines again to determine the exact location of the switch closure. The microprocessor then performs the activity indicated by the closure, including display update.

2.3.2 LED Circuits

The discrete LEDs on the Switchboard are driven directly from the front panel driver board. (See the description for Driver Board A13A2.) Table 3 provides a listing of LED display by reference designator and function.

2.4 Maintenance

The advanced design of the A13A1 assembly eliminates the need for regular maintenance. However, when replacing components on this assembly, observe the following caution.

Table 3. A13A1 Switchboard LED Indicators

Indicator	Function	Description
DS1	Frequency	Indicates frequency display field will be modified by any tuning knob or keypad activity.
DS2	Fault	Indicates BITE, Power Supply, PLL Synthesizer faults, or Antenna Overhead faults.
DS3	Test	Indicates Test mode of operation.
DS4	Scan	Indicates Receiver is in Scan mode of operation.
DS5	Receive	Indicates the Receiver is in the standard Receive mode of operation.
DS6	BFO	Indicates BFO display field will be modified by any tuning wheel or keypad activity.
DS8	Program	Indicates Receiver is in Channel or Group programming mode.
DS10	Remote	Indicates Receiver is under Remote Control.
DS11	Tune	Indicates the tuning wheel is enabled. If off, tuning wheel rotation has no effect on the receiver.
DS12	Channel	Indicates the channel display field will be modified by any keypad or tuning wheel activity.

CAUTION

Cleaning fluids normally used to remove flux will damage switches used on this assembly. Cleaning of the A13A1 assembly is not recommended.

Table 4 is the Front Panel Switchboard A13A1 parts list. Figures 3 and 4 are the Front Panel Switchboard A13A1 component location diagram and schematic diagram.

Table 4. Front Panel Switchboard A13A1 Parts List (PL 10073-2700, Rev. E/-2700-02, Rev. B)

Ref. Desig.	Part Number	Description
	10073-7052	RIBBON CABLE
	10073-2705	SWITCH PLATE
	10073-2050	BUTTON,SWITCH,O
	10073-2051	BUTTON,SWITCH,1
	10073-2052	BUTTON,SWITCH,2
	10073-2053	BUTTON,SWITCH,3
	10073-2054	BUTTON,SWITCH,4
	10073-2055	BUTTON,SWITCH,5
	10073-2056	BUTTON,SWITCH,6
	10073-2057	BUTTON,SWITCH,7
	10073-2058	BUTTON,SWITCH,8
	10073-2059	BUTTON,SWITCH,9
	10073-2060	BUTTON,SWITCH,TUNE
	10073-2061	SW BTN ENTR
	10073-2062	BUTTON,TEST
	10073-2063	BUTTON,SWITCH,RECALL
	10073-2064	BUTTON,SWITCH,LOAD
	10073-2065	SW BTN PROG
	10073-2066	BUTTON,SCAN
	10073-2067	BUTTON SPK ON/OFF
	10073-2068	BUTTEN RCV
	10073-2069	BUTTON,SWITCH
	10073-2022	SHIELD SWITCH
DS1	N21-0002-000	DIODE,LED,GREEN
DS2	N21-0001-000	DIODE,LED,RED
DS3	N21-0002-000	DIODE,LED,GREEN
DS4	N21-0002-000	DIODE,LED,GREEN
DS5	N21-0002-000	DIODE,LED,GREEN
DS6	N21-0002-000	DIODE,LED,GREEN
DS8	N21-0002-000	DIODE,LED,GREEN
DS10	N21-0002-000	DIODE,LED,GREEN
DS11	N21-0002-000	DIODE,LED,GREEN
DS12	N21-0002-000	DIODE,LED,GREEN
DS14	N21-0002-000	DIODE,LED,GREEN
J2	J46-0033-006	CONNECTOR, 6 PIN
J3	J46-0033-005	CONNECTOR 5 PIN
S1	S05-0004-001	SWITCH
S2	S05-0004-001	SWITCH
S3	S05-0004-001	SWITCH
S4	S05-0004-001	SWITCH
S5	S05-0004-001	SWITCH
S6	S05-0004-001	SWITCH
S9	S05-0004-001	SWITCH
S10	S05-0004-001	SWITCH

Table 2. Reference Generator Assembly A12 Parts List (PL 10073-4700, Rev. AB) (Cont.)

Ref. Desig.	Part Number	Description
C45	CM04ED560J03	CAP 56PF 5% 500V MICA
C46	M39014/01-1535	CAP .01UF 10% 100V CER-R
C47	M39014/01-1535	CAP .01UF 10% 100V CER-R
C48	M39014/01-1535	CAP .01UF 10% 100V CER-R
C49	M39014/01-1535	CAP .01UF 10% 100V CER-R
C50	M39014/02-1310	CAP .1UF 10% 100V CER-R
C51	M39014/01-1535	CAP .01UF 10% 100V CER-R
C52	CM04ED560J03	CAP 56PF 5% 500V MICA
C53	M39014/01-1535	CAP .01UF 10% 100V CER-R
C54	M39014/01-1535	CAP .01UF 10% 100V CER-R
C55	M39014/02-1310	CAP .1UF 10% 100V CER-R
C56	M39014/01-1535	CAP .01UF 10% 100V CER-R
C57	M39014/01-1535	CAP .01UF 10% 100V CER-R
C58	M39014/01-1535	CAP .01UF 10% 100V CER-R
C59	M39014/02-1310	CAP .1UF 10% 100V CER-R
C60	M39014/02-1310	CAP .1UF 10% 100V CER-R
C61	M39014/02-1310	CAP .1UF 10% 100V CER-R
C62	M39014/02-1310	CAP .1UF 10% 100V CER-R
C63	M39014/02-1310	CAP .1UF 10% 100V CER-R
C64	M39014/02-1310	CAP .1UF 10% 100V CER-R
C65	C26-0016-151	CAP 150UF 20% 16V TANT
C66	M39014/02-1310	CAP .1UF 10% 100V CER-R
C67	M39014/02-1310	CAP .1UF 10% 100V CER-R
C68	C26-0025-100	CAP 10UF 20% 25V TANT
C69	M39014/02-1310	CAP .1UF 10% 100V CER-R
C70	M39014/02-1310	CAP .1UF 10% 100V CER-R
C71	C26-0050-100	CAP 10UF 20% 50V TANT
C72	M39014/02-1310	CAP .1UF 10% 100V CER-R
C73	M39014/02-1310	CAP .1UF 10% 100V CER-R
C74	C26-0025-470	CAP 47UF 20% 25V TANT
C75	M39014/02-1310	CAP .1UF 10% 100V CER-R
C76	CK05BX102K	CAP 1000PF 10% 200V CER
C77	M39014/01-1535	CAP .01UF 10% 100V CER-R
C78	M39014/02-1310	CAP .1UF 10% 100V CER-R
C79	CK05BX102K	CAP 1000PF 10% 200V CER
C80	M39014/01-1535	CAP .01UF 10% 100V CER-R
C81	M39014/01-1535	CAP .01UF 10% 100V CER-R
C82	M39014/02-1310	CAP .1UF 10% 100V CER-R
C83	M39014/02-1310	CAP .1UF 10% 100V CER-R
C84	M39014/01-1535	CAP .01UF 10% 100V CER-R
C85	M39014/01-1535	CAP .01UF 10% 100V CER-R
C86	M39014/01-1535	CAP .01UF 10% 100V CER-R
C87	10121-4720	CAP, CER 10PF N750
CR1	D12-0007-001	DIODE PIN ATTN 1W 9301
CR2	1N3064	DIODE 75mA 75V SW

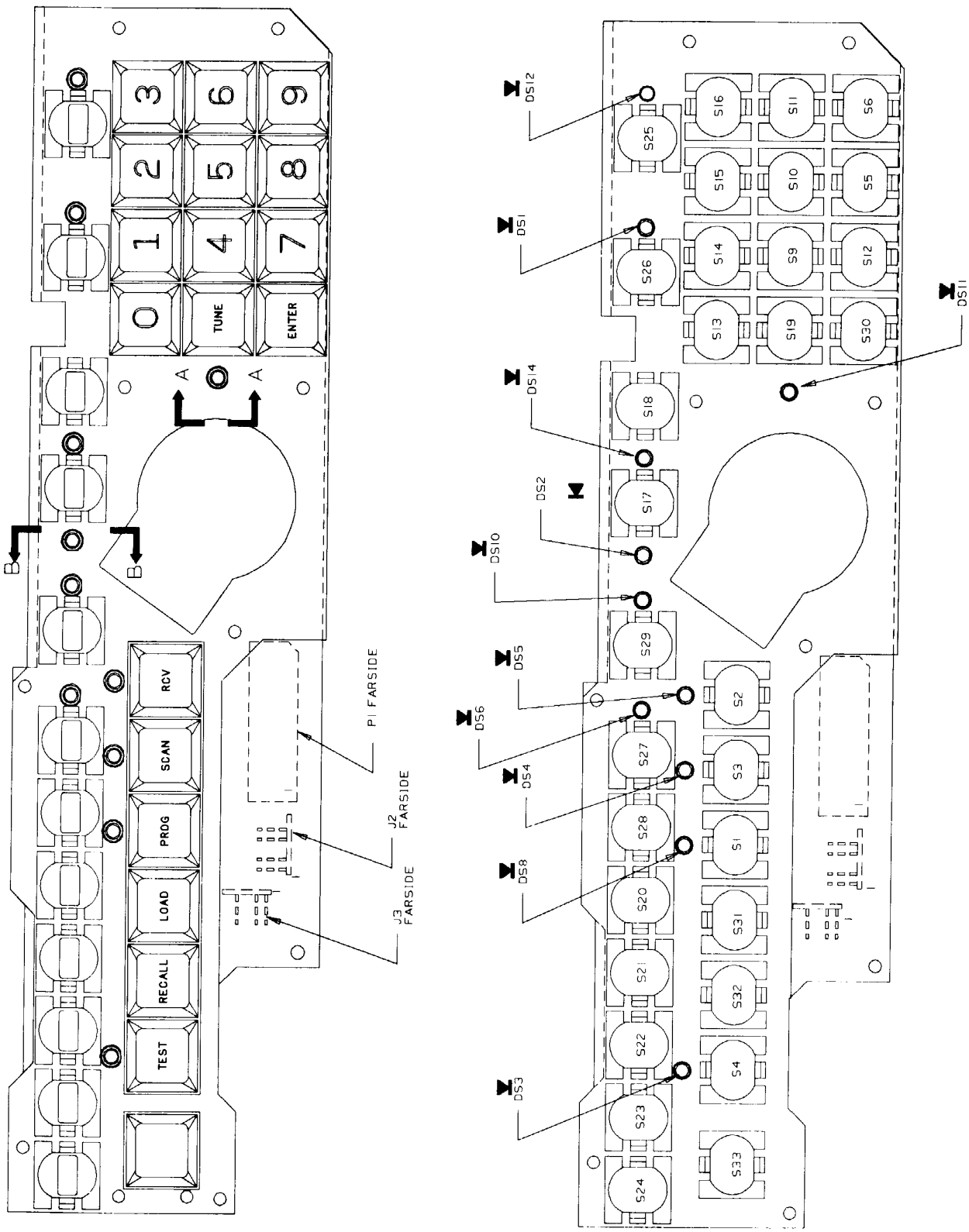


Figure 3. Front Panel Switchboard A13A1 Component Location Diagram (10073-2700)

NOTE: UNLESS OTHERWISE SPECIFIED:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR A COMPLETE DESIGNATION, PREFIX WITH UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.
2. VENDOR PART NO. CALLOUTS ARE FOR REFERENCE ONLY. COMPONENTS ARE SUPPLIED PER PART NO. IN PARTS LIST.
3. ☐ INDICATES FRONT PANEL MARKING.

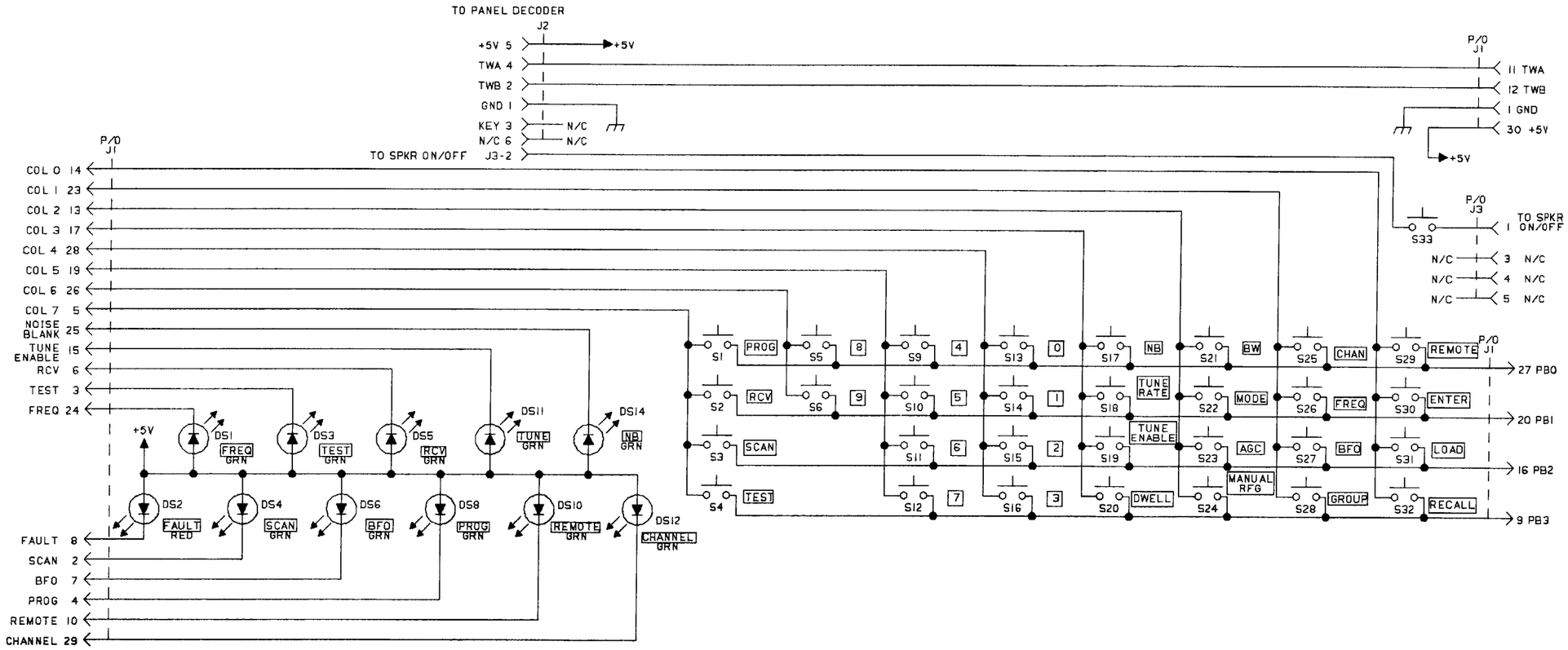


Figure 4. **Front Panel Switchboard A13A1 Schematic Diagram (10073-2701, Rev. B)**

3. FRONT PANEL DRIVER BOARD A13A2

3.1 General Description

The Front Panel Driver Board serves four basic functions, all associated with controlling the front panel of the receiver. It generates the drive signals for the vacuum fluorescent displays, drives the discrete LED displays, generates signals indicating tuning wheel rotation and routes the signals to the Front Panel Switchboard associated with detecting pushbutton activity. A block diagram of the assembly is shown in figure 5.

The Driver Board controls the vacuum fluorescent displays by providing filament voltages, display segment information, and digit select information to them. The filament voltages are generated in the Display Converter Module and routed to the display connectors. The Driver Board multiplexes the VF Displays by providing information for the segments to be lit within a character while enabling that character. This is done at a rapid rate to give the appearance of continuous illumination. (See paragraphs 5 and 6 of this section for drawings showing the display segment location.) The information to be displayed is provided to the Driver Board (A13A2) by the Control Assembly (A14) in serial fashion using the signals DATA, CLK, and DISP STR ON J1P1 pins 2, 4, and 14 respectively.

The discrete LED displays of the Front Panel are lit by the Driver Board using information provided by the Control Assembly.

Rotating the tuning wheel generates two pulsing signals which are squared up by the Driver Board, A13A2, and routed to the Control Assembly. The Control Assembly updates the display in response to the tuning wheel motion.

Driver Board A13A2 outputs eight column strobes to the switches in the front panel and inputs four row lines from the switches. The row lines are routed to the Control Assembly where a switch closure is detected as a connection from a column to a row.

3.2 Interface Connections

Table 5 summarizes the A13A2 interface connections.

3.3 Circuit Description

3.3.1 Microprocessor Operation

The heart of Front Panel Driver board A13A2 operation is the 8035 microprocessor (U12). The execution of the program stored in the 2716 type EPROM (U16) causes the microprocessor to perform the display update functions as described in paragraph 2. To execute the program, the microprocessor must continuously get instructions from U16 and process them. To accomplish this, the microprocessor (at the start of an instruction cycle) outputs the address of the instruction to be obtained into its address/data bus at pins U12-12 to U12-19. The address latch (U13) latches it to the EPROM. The EPROM (U16) outputs the instruction to the data bus which is read by the microprocessor and executed. The microprocessor uses the Address Latch Enable, active high (ALE) signal to indicate the presence of a valid address on the bus. The Program Store Enable (PSEN) signal is used to enable the EPROM to output the obtained instruction while the RD (read) and WR (write) signals are used to read from and write to other external devices. The RD signal is used to read display data sent by Control Assembly A14 from the shift registers U14 and U15 while the WR signal is used to write the display information to the VF display segment latches U8, U9, and U23. These functions are explained in greater detail in sections 3.3.2 through 3.3.7.

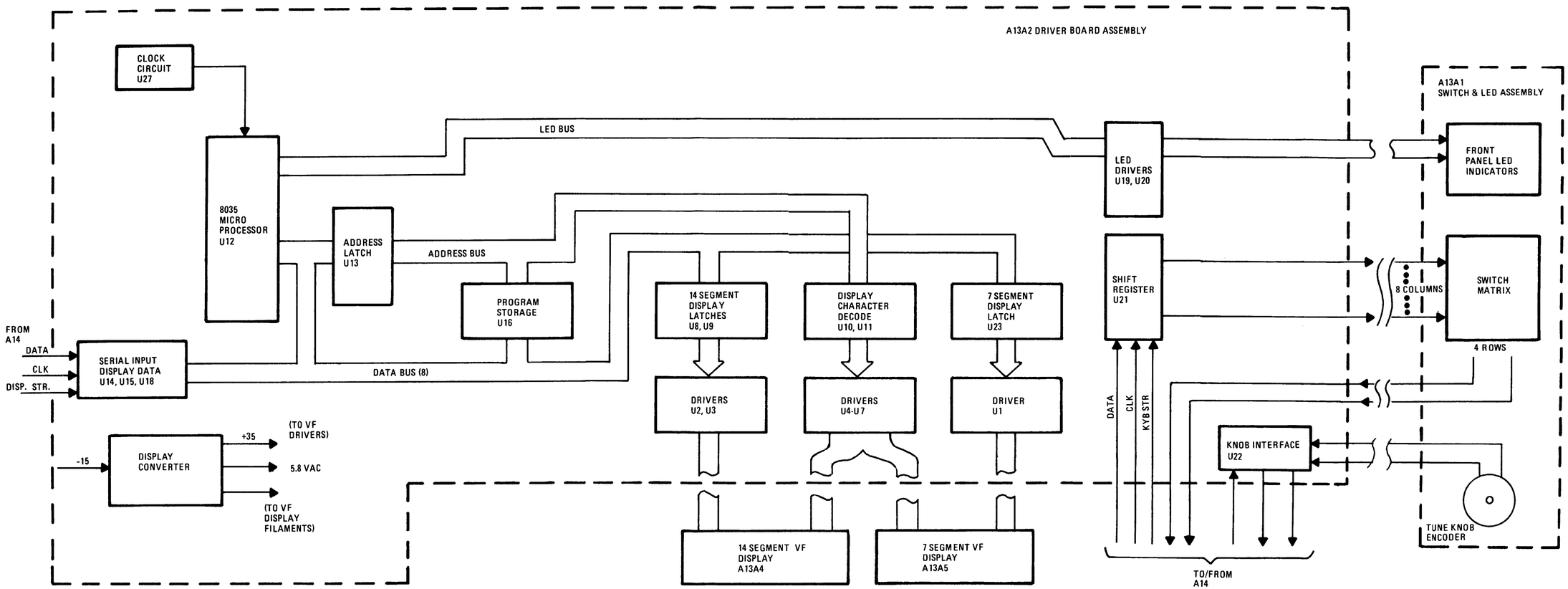


Figure 5. Front Panel Driver Board A13A2 Functional Block Diagram

Table 5. A13A2 Driver Board Interface Connections

Connector	Name	Description
J1 to/from A14		
J1-1	TWHL INT	Tune Wheel Interrupt to Control Assembly
J1-2	Data	Serial Display Data from Control Assembly
J1-3	DIR	Tune Wheel Direction to Control Assembly
J1-4	CLK	Clock for display Data from Control Assembly
J1-5	TWHL RESET	Interrupt Reset from Control Assembly
J1-6	-15 V	
J1-7	+ 5 V	
J1-8	BITE IN	Power Supply Fault Indicator
J1-9	PB3	Switch row readback to Control Assembly
J1-10	KYBSTR	Keyboard Strobe from Control Assembly
J1-11	PB2	Switch Row readback to Control Assembly
J1-12	Fault	Output to Rear Panel (via Control Assembly)
J1-13	PB1	Switch Row readback to Control Assembly
J1-14	DISP STR	Display Strobe from Control Assembly
J1-15	PB0	Switch Row readback to Control Assembly
J1-16	N/C	
J1-17	N/C	
J1-18	GND	
J1-19	N/C	
J1-20	GND	
J2 to/from A13A1		
J2-1	GND	
J2-2	Scan LED	
J2-3	Test LED	
J2-4	Program LED	
J2-5	COL 7	
J2-6	Receive LED	
J2-7	BFO LED	
J2-8	Fault LED	
J2-9	PB3	
J2-10	Remote LED	
J2-11	TWA	Tuning Wheel encoder output
J2-12	TWB	Tuning Wheel encoder output
J2-13	COL 2	
J2-14	COL 0	

Table 5. A13A2 Driver Board Interface Connections (Cont.)

Connector	Name	Description
J2-15	Tune LED	
J2-16	PB2	
J2-17	COL 3	
J2-18	N/C	
J2-19	COL 5	
J2-20	PB1	
J2-21	N/C	
J2-22	N/C	
J2-23	COL 1	
J2-24	Frequency LED	
J2-25	N/C	
J2-26	COL 6	
J2-27	PB0	
J2-28	COL 4	
J2-29	Channel LED	
J2-30	+ 5 V	
J3 to/from A13A4		
J3-1	a Segment	
J3-2	b Segment	
J3-3	c Segment	
J3-4	d Segment	
J3-5	m Segment	
J3-6	n Segment	
J3-7	e Segment	
J3-8	f Segment	
J3-9	J Segment	
J3-10	k Segment	
J3-11	g Segment	
J3-12	h Segment	
J3-13	Decimal Point	
J3-14	Comma	
J3-15	N/C	
J3-16	G1 Digit	
J3-17	p Segment	
J3-18	r Segment	
J3-19	G2 Digit	

Table 5. A13A2 Driver Board Interface Connections (Cont.)

Connector	Name	Description
J3-20	G3 Digit	
J3-21	G20 Digit	
J3-22	G4 Digit	
J3-23	G5 Digit	
J3-24	G6 Digit	
J3-25	G19 Digit	
J3-26	G7 Digit	
J3-27	G8 Digit	
J3-28	G9 Digit	
J3-29	G18 Digit	
J3-30	G10 Digit	
J3-31	G11 Digit	
J3-32	G12 Digit	
J3-33	G17 Digit	
J3-34	G13 Digit	
J3-35	G14 Digit	
J3-36	N/C	
J3-37	G16 Digit	
J3-38	G15 Digit	
J3-39	Filament	
J3-40	Filament	
J4 to/from A13A5		
J4-1	G11 10 MHz Digit	
J4-2	G10 1 MHz Digit	
J4-3	G9 100 kHz Digit	
J4-4	G3 1/2 Segments	
J4-5	G7 1 kHz Digit	
J4-6	G8 10 kHz Digit	
J4-7	Filament	
J4-8	Decimal Point	
J4-9	G5 10 Hz Digit	
J4-10	G6 100 Hz Digit	
J4-11	N/C	
J4-12	Comma	
J4-13	G4 1 Hz Digit	
J4-14	c Segment	

Table 5. A13A2 Driver Board Interface Connections (Cont.)

Connector	Name	Description
J4-15	G2 CH10 Digit	
J4-16	G1 CH1 Digit	
J4-17	b Segment	
J4-18	a Segment	
J4-19	g Segment	
J4-20	Filament	
J4-21	Underline Segments	
J4-22	d Segment	
J4-23	e Segment	
J4-24	f Segment	

3.3.2 Display Data Input

Front Panel Driver Board A13A2 at power up lights all LEDS and all segments of the vacuum fluorescent displays. After completion of the power on self-test, the display is updated to the last receive setting used before power off using display data provided by Control Assembly A14. The Control Assembly provides the information for all display updates to the driver board in serial fashion via J1-2. This information is clocked into serial shift registers U14 and U15 to be read in parallel by microprocessor U12. The clock signal is 750 kHz and is provided by the Control Assembly at J1-4 and routed to the shift registers at pin 3. When the shift registers have been loaded with display data, the Control Assembly generates an interrupt to the driver board microprocessor (U12) using the signal display strobe at J1-14. The display strobe pulse serves to trigger monostable U24, which in turn generates the interrupt, causing the microprocessor to read the display data from the shift registers U14 and U15. U18 provides buffering of the display data onto the microprocessor data bus. The act of reading the shift registers causes resetting of the interrupt by the microprocessor read control line at U24-3 which is the reset into the monostable.

3.3.3 Vacuum Fluorescent Display Drive

Display data read in from the Control Assembly is converted by microprocessor U12 into formats required for driving the VF displays. The displays are driven in multiplexed fashion so that only one character is driven at a given instant. Each character in the VF displays has a unique address which is output by the microprocessor to the bus and latched into the address latch (U13) during a display character update. The address is decoded by U10 or U11 into a character enable pulse. During the output instruction, the segment information for the character to be lit is latched into U23 for seven segment characters or into U8 and U9 for 14 segment characters. Each character is enabled for approximately 640 microseconds after which, the microprocessor processes the next character in a similar manner.

3.3.4 LED Drive

The discrete LEDs on the front panel are driven from the parallel ports on microprocessor U12. These outputs are buffered by U19 and U20 and are routed to the switchboard via J2. An LED is lit by an active low output. The information to be written to the LEDs originates in Control Assembly A14 and is input to the driver board in the manner described in paragraph 3.3.2.

3.3.5 Tuning Wheel

Rotating the front panel tuning wheel causes two pulsing signals to be generated which are 90 degrees out of phase. These are input to the driver board at J2-11 and J2-12. The pulses are squared by Schmitt Trigger Inverters (U28) and used to generate an interrupt to the Control Assembly via U22. The interrupt (active high) is output at J1-1 while J1-3 provides direction of rotation information to Control Assembly A14. When the Control Assembly receives tuning wheel interrupts indicating rotation, it outputs new display information to the driver board as described in paragraph 3.3.2, so that the indicating display field is increased or decreased.

3.3.6 Pushbutton Circuitry

The driver board serves primarily to route the signals associated with detection of pushbutton activity to and from the control assembly and the switchboard. The switches are arranged in a matrix of eight columns by four rows. Switch activity is detected by sensing a closure between a column line to a row line. The column outputs are written serially from the Control Assembly to the driver board via J1-2, clocked via J1-4, and latched into shift register U21 by the signal KYB STR (keyboard strobe) at J1-10. The parallel outputs of the shift register are routed to the switchboard via J2 signals COL 0 through COL 7. The rows are routed back to the Control Assembly as signals PB 0 to PB 3 (see J1-9, 11, 13, and 15).

3.3.7 Converter Module

The Converter is a self-contained dc to dc converter type power supply. It is powered by the -15 volts dc available to the board, and generates the anode and filament voltages for the vacuum fluorescent displays on A13A4 and A13A5. The anode voltage is 35 volts dc and the filament voltage is a 5.8 volt peak-to-peak square wave.

3.4 Maintenance

3.4.1 Adjustments

The only adjustment on the Front Panel Driver Board is the VF display brightness adjust potentiometer located at the top center of the PWB. Turn clockwise for brighter displays (single turn potentiometer).

3.4.2 Troubleshooting

To make a quick assessment of Driver Board functions, the four test points should be checked with an oscilloscope.

- TP1 - Microprocessor Write Line. Should be active low pulses repeated approximately every 600 to 700 microseconds.
- TP2 - Character strobe to U10. Active high pulse every 600 to 700 microseconds indicates display is being updated.
- TP3 - Character Strobe to U11. Same as TP2. Also indicates display being updated. Both signals are required.
- TP5 - Interrupt to microprocessor from Control Assembly. Active low approximately 50 microseconds pulse every 1 second (faster with Tuning wheel Rotating).

If the above signals are incorrect, more fundamental checks are indicated. Perform the checks in the following order.

a. Verify + 5 V at J1-7 and -15 V at J1-6.

b. Verify display filament voltages (≈ 5.8 V_{p-p} square wave with a 6.2 volt dc offset) at E3 and E6, and + 35 V Dc driver voltage at pin 10 of U1-U8.

c. Verify integrity of connections E1 through E6. The 10073-2400 alphanumeric display module requires connections E1 to E2 and E5 to E6.

d. Verify 6 MHz clock at U12-2 and U12-3.

e. Verify approximately + 5 V at U12-4. (Microprocessor reset in.)

f. Verify ALE signal, approximately 60-40 duty cycle square wave at U12-11.

g. Verify activity on bus AD0 - AD7 (zero to five volt random square waves).

h. Verify that all socketed ICs are installed correctly with no pins bent underneath the IC.

3.5 Parts List and Schematic Diagram

Table 6 is the Driver Board A13A2 parts list. Figures 6 and 7 are the Driver Board A13A2 component location diagram and schematic diagram.

Table 6. Driver Board A13A2 Parts List (PL 10215-2200)

Ref. Desig.	Part Number	Description
--	10215-2250	ASSY DC-DC CONVERTER
C1	M39014/02-1310	CAP .1UF 10% 100V CER-R
C2	M39014/02-1310	CAP .1UF 10% 100V CER-R
C3	M39014/02-1310	CAP .1UF 10% 100V CER-R
C3	M39014/02-1310	CAP .1UF 10% 100V CER-R
C4	M39014/02-1310	CAP .1UF 10% 100V CER-R
C4	M39014/02-1310	CAP .1UF 10% 100V CER-R
C5	M39014/02-1310	CAP .1UF 10% 100V CER-R
C6	M39014/02-1310	CAP .1UF 10% 100V CER-R
C7	M39014/02-1310	CAP .1UF 10% 100V CER-R
C8	M39014/02-1310	CAP .1UF 10% 100V CER-R
C10	M39014/02-1310	CAP .1UF 10% 100V CER-R
C12	M39014/02-1310	CAP .1UF 10% 100V CER-R
C14	M39014/02-1310	CAP .1UF 10% 100V CER-R
C15	M39014/02-1310	CAP .1UF 10% 100V CER-R
C19	M39014/02-1310	CAP .1UF 10% 100V CER-R
C22	M39014/02-1310	CAP .1UF 10% 100V CER-R
C23	M39014/02-1310	CAP .1UF 10% 100V CER-R
C24	M39014/02-1310	CAP .1UF 10% 100V CER-R
C25	M39014/02-1310	CAP .1UF 10% 100V CER-R
C26	M39014/02-1310	CAP .1UF 10% 100V CER-R
C27	M39014/02-1310	CAP .1UF 10% 100V CER-R
C29	M39014/01-1535	CAP .01UF 10% 100V CER-R
C31	M39014/02-1310	CAP .1UF 10% 100V CER-R
C32	CK05BX102K	CAP 1000PF 10% 200V CER
C37	C18-0125-470	CAP 47UF 25V ELEC
C38	C26-0050-479	CAP 4.7UF 20% 50V TANT

Table 6. Driver Board A13A2 Parts List (PL 10215-2200) (Cont.)

Ref. Desig.	Part Number	Description
C39	CK05BX330K	CAP 33PF 10% 200V CER
C40	CK05BX330K	CAP 33PF 10% 200V CER
C41	C18-0125-470	CAP 47UF 25V ELEC
CR1	1N4454	DIODE 200MA 75V SW
CR2	1N4454	DIODE 200MA 75V SW
CR3	1N4454	DIODE 200MA 75V SW
CR4	1N4454	DIODE 200MA 75V SW
J2	J46-0013-030	HDR 30 PIN 0.100" DR SHRD
JMP1	MP-1142	RES ZERO OHM (CKT JMPR)
JMP2	MP-1142	RES ZERO OHM (CKT JMPR)
L1	L06-0002-471	IND 470.0UH 20% AXL SHLD
P1	10073-7050	RIBBON CABLE, 24 COND
P2	10073-7051	RIBBON CABLE, 40 COND
P3	10073-7053	RIBBON CABLE, 20 COND
R3	R50-0010-472	RES 4.7K 2% 10SIP 9RES
R14	R65-0003-224	RES 220K 5% 1/4W CAR FILM
R15	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R16	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R17	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R18	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R22	R51-0010-121	RES 120 2% 10SIP 5RES
R23	R51-0010-121	RES 120 2% 10SIP 5RES
R25	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R26	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R27	R65-0003-204	RES 200K 5% 1/4W CAR FILM
R28	R65-0003-393	RES 39K 5% 1/4W CAR FILM
R29	R-2232	RES VAR 100K 10% .5W VER.
R33	R65-0003-471	RES 470 5% 1/4W CAR FILM
R34	R65-0003-471	RES 470 5% 1/4W CAR FILM
R35	R65-0003-471	RES 470 5% 1/4W CAR FILM
R36	R65-0003-471	RES 470 5% 1/4W CAR FILM
R37	R65-0003-161	RES 160 5% 1/4W CAR FILM
R38	R50-0008-103	RES 10K 2% 8SIP 7RES
R50	R65-0003-100	RES 10 5% 1/4W CAR FILM
R52	R65-0003-100	RES 10 5% 1/4W CAR FILM
R53	R65-0004-332	RES 3.3K 5% 1/2W CAR FILM
R54	R65-0003-103	RES 10K 5% 1/4W CAR FILM
TP1	J-0392	TP PWB BRN RA SIDE ACCESS
TP2	J-0387	TP PWB RED RA SIDE ACCESS
TP3	J-0390	TP PWB ORN RA SIDE ACCESS
TP5	J-0389	TP PWB GRN RA SIDE ACCESS
U1	I75-0009-001	IC NE594 DISPLAY DRIVER
U2	I75-0009-001	IC NE594 DISPLAY DRIVER
U3	I75-0009-001	IC NE594 DISPLAY DRIVER
U4	I75-0009-001	IC NE594 DISPLAY DRIVER
U5	I75-0009-001	IC NE594 DISPLAY DRIVER
U6	I75-0009-001	IC NE594 DISPLAY DRIVER
U7	I75-0009-001	IC NE594 DISPLAY DRIVER
U8	I05-0000-373	IC 74LS373 PLASTIC TTL
U9	I05-0000-373	IC 74LS373 PLASTIC TTL
U10	I01-0000-202	IC 4514B PLASTIC CMOS

Table 6. Driver Board A13A2 Parts List (PL 10215-2200) (Cont.)

Ref. Desig.	Part Number	Description
U11	I01-0000-202	IC 4514B PLASTIC CMOS
U12	IC-0374	IC MICMPTR 8-BIT 8035
U13	I15-0000-373	IC 74HC373 PLASTIC CMOS
U14	I01-0000-156	IC 4094B PLASTIC CMOS
U15	I01-0000-156	IC 4094B PLASTIC CMOS
U16	10073-8302	KIT SOFTWARE RF590 DRIVER
U17	I01-0000-362	IC 4098B PLASTIC CMOS
U18	I15-0000-244	IC 74HC244 PLASTIC CMOS
U19	I05-0000-244	IC 74LS244 PLASTIC TTL
U20	I05-0000-244	IC 74LS244 PLASTIC TTL
U21	I01-0000-156	IC 4094B PLASTIC CMOS
U22	I05-0000-074	IC 74LS74A PLASTIC TTL
U23	I05-0000-373	IC 74LS373 PLASTIC TTL
U24	I01-0000-362	IC 4098B PLASTIC CMOS
U25	I01-0056-001	IC 74C02 PLASTIC CMOS
U26	I05-0000-027	IC 74LS27 PLASTIC TTL
U27	I02-0015-000	IC 7404 PLASTIC TTL
U28	I18-0006-001	IC 74C14 PLASTIC CMOS
VR1	1N5234B	DIODE 6.2V 5% .5W ZENER
XU16	J77-0008-005	SKT IC MACH 24 PIN
Y1	Y15-0004-060	XTAL 6 MHZ

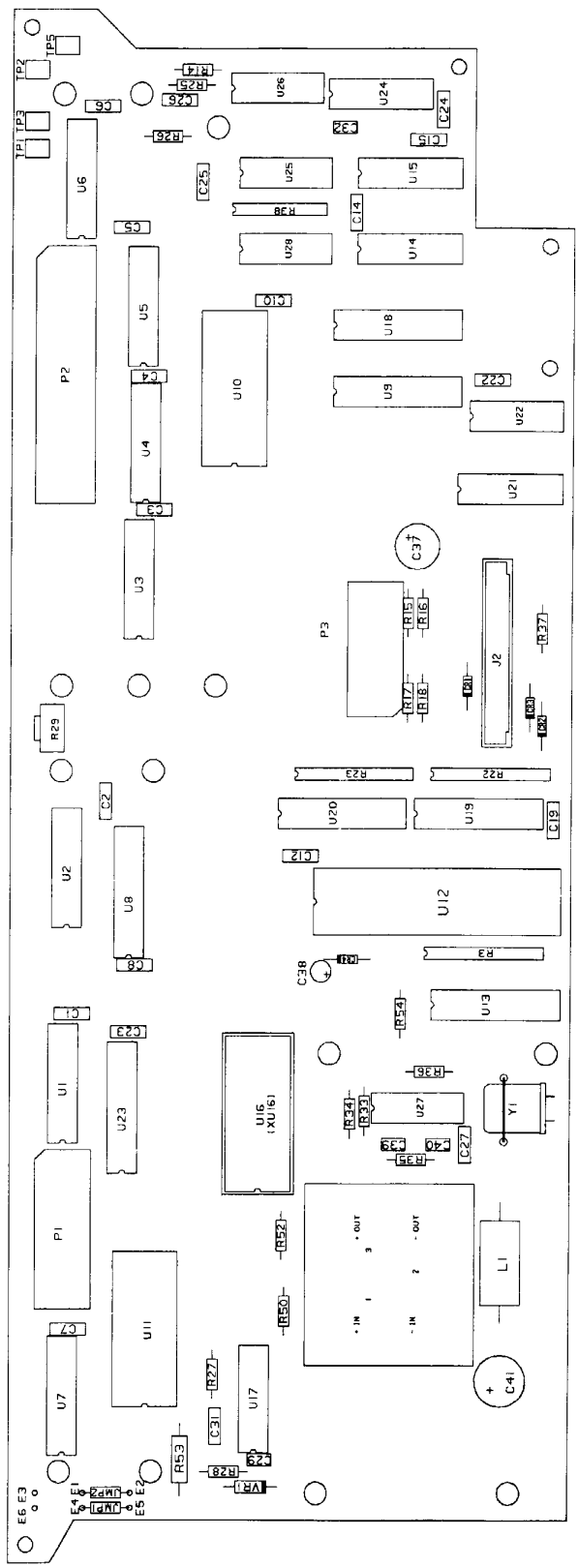


Figure 6. Driver Board A13A2 Component Location Diagram (10215-2200, Rev. C)

NOTE: UNLESS OTHERWISE SPECIFIED:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR A COMPLETE DESIGNATION, PREFIX WITH UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.
2. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, ±5%.
3. ALL CAPACITOR VALUES ARE IN MICROFARADS.
4. VENDOR PART NO. CALLOUTS ARE FOR REFERENCE ONLY. COMPONENTS ARE SUPPLIED PER PART NO. IN PARTS LIST.
5. CONNECT E4 TO E5 AND E1 TO E2 FOR FUTABA ALPHANUMERIC DISPLAY (P/N 10073-2400).
6. SIGNALS ARE PRODUCT SPECIFIC FOR THE FOLLOWING PINS:

PIN	RF-590	RF-1310	RF-7110
P3-1	TUNE WHL INT	N/C	N/C
P3-2	DATA	FR SER DATA	DATA OUT
P3-3	DIR	N/C	N/C
P3-4	CLK	FR SER CLK	DATA CLOCK
J2-2	SCAN	OPER	SQUELCH
J2-3	TEST	AMP OFF	START LQA
J2-4	PROG	STBY	SCAN
J2-6	RCV	TUNE	REMOTE
J2-7	BFO	POWER	CALL MAN
J2-10	REMOTE	READY	SILENT
J2-15	TUNE	CLIP	CALL AUTO
J2-25	NOISEBLANK	N/C	LISTEN

UNUSED GATES

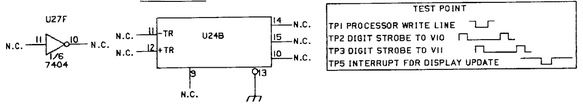


TABLE I

TEST POINT	
TP1	PROCESSOR WRITE LINE
TP2	DIGIT STROBE TO VIO
TP3	DIGIT STROBE TO VII
TP5	INTERRUPT FOR DISPLAY UPDATE

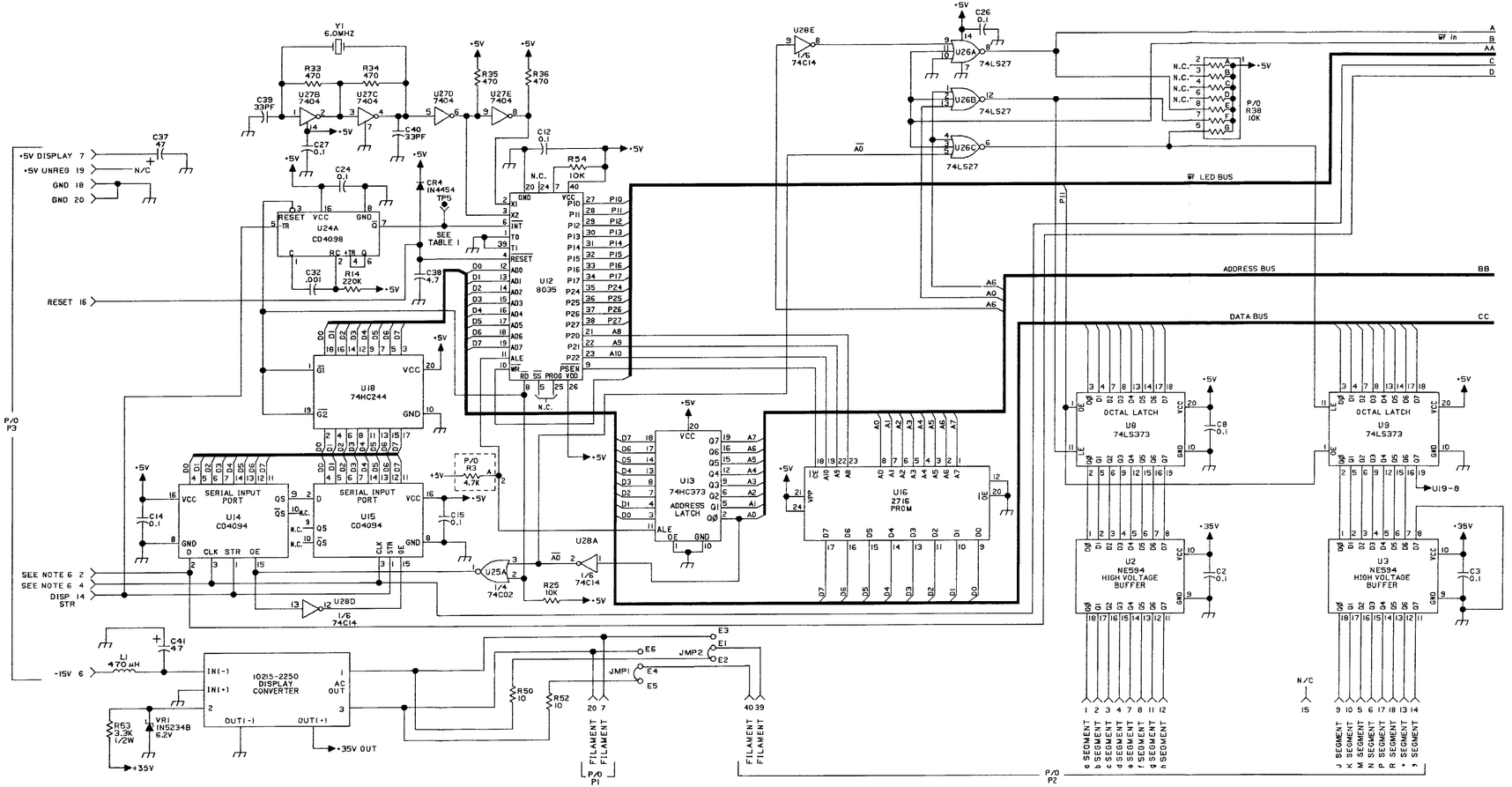


Figure 7. Driver Board A13A2 Schematic Diagram (10215-2201, Rev. F) (Sheet 1 of 2)

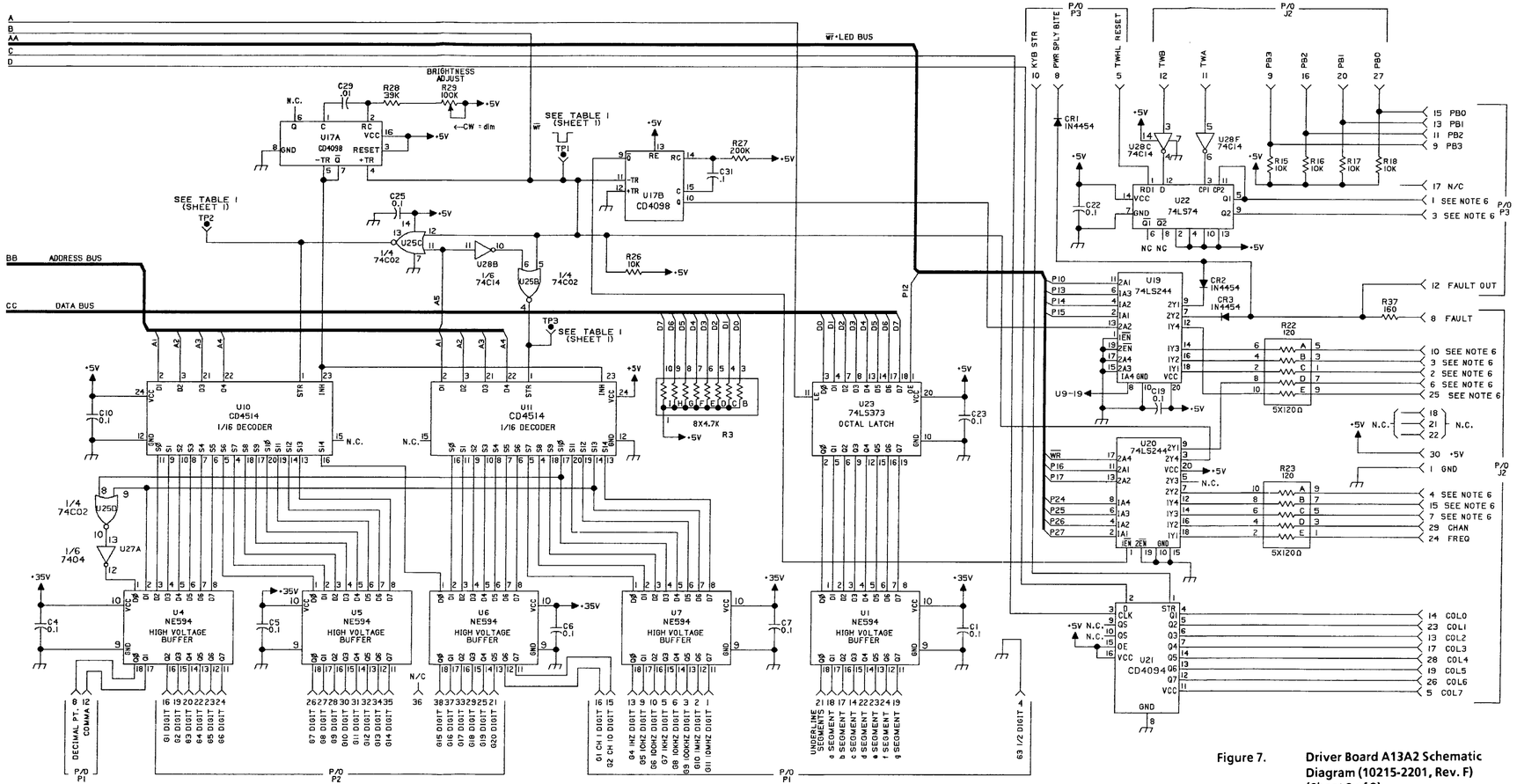


Figure 7. Driver Board A13A2 Schematic Diagram (10215-2201, Rev. F) (Sheet 2 of 2)

4. FRONT PANEL METER BOARD A13A3

4.1 General Description

Meter Board A13A3 contains the circuitry required to monitor selected RF and AF signals on the front panel meter (M1). The following signals may be monitored via pushbutton front panel control.

- RF Signal strength - all modes
- AF Line Audio Level - all modes
- ISB - LSB RF Signal strength
- ISB - LSB Line Audio Level

The four switches controlling these functions are spring loaded so that only one of them can be active at any time.

Additionally, other signal data relating to the following functions flow through this board to the following front panel controls.

- Headphone Audio
- RF Gain
- COR

A block diagram of the assembly is shown in figure 8.

4.2 Interface Connections

Table 7 summarizes the A13A3 interface connections.

4.3 Circuit Description

4.3.1 Meter Control

RF signal strength and line audio level signals are normally supplied by the IF/Audio Assembly A5. S2 connects the RF signal to the meter when pressed, and S1 connects the line audio signal. If the ISB Assembly A18 is disconnected, there will no ISB RF signal strength or ISB line audio signals present to be selected. Consequently, pressing either S3 or S4 will result in a zero meter reading.

When the ISB IF/Audio Assembly is installed and properly connected; however, the RF (S1) and AF (S2) switches channel the USB components of the ISB signal to M1. The ISB-LSB RF (S3) and ISB-LSB AF (S4) switches route the LSB components of the ISB signal to the meter. Whenever an ISB -LSB switch (S3 or S4) is selected, + 5 Vdc is switched on to the LSB select line (J1-1) which informs Control Assembly A14 that an ISB function has been selected.

4.3.2 Line Level Control

Line audio output level adjustments are provided on the A13A3 assembly. They are accessed through small front panel holes to the left of the meter (USB line audio) and to the right of the meter (ISB-LSB line audio). R1 adjusts USB adjustments under normal receiver operation, while R2 will control the LSB audio portion of

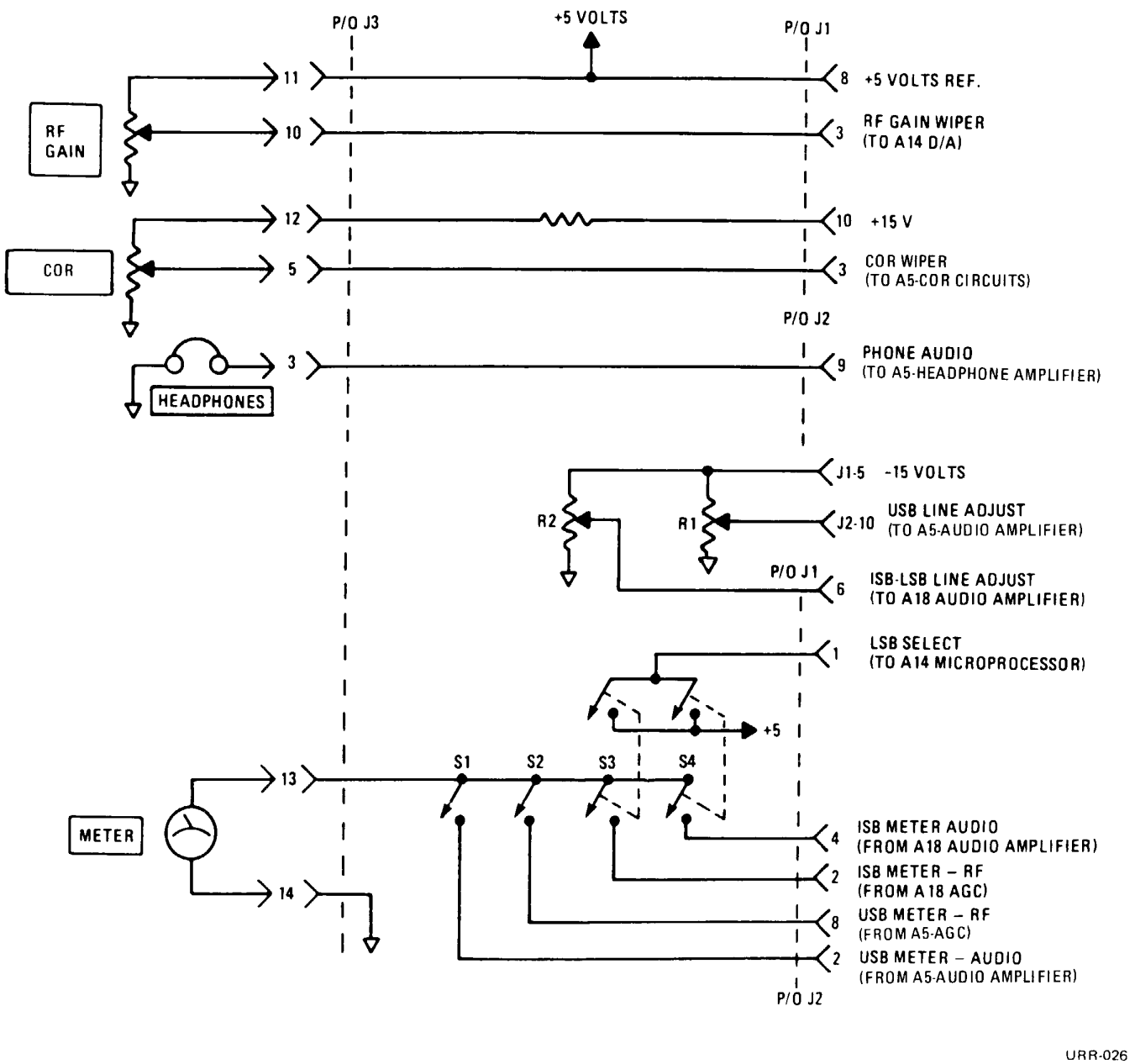


Figure 8. Front Panel Meter Board A13A3 Functional Block Diagram

Table 7. A13A3 Interface Connections

Connector	Function
J1 to/from A14	
J1-1	LSB Select
J1-2	LSB Meter - aGC
J1-3	RF Gain
J1-4	LSB Meter - Audio
J1-5	-15 V
J1-6	LSB Line Adjust
J1-7	Spare
J1-8	+ 5 Vdc
J1-9	Ground
J1-10	+ 15 Vdc
J2 to/from A5	
J2-1	N/C
J2-2	USB Meter - Audio
J2-3	COR Wiper
J2-4	Key
J2-5	Spare
J2-6	N/C
J2-7	Audio Ground
J2-8	USB Meter - AGC
J2-9	Phone Audio
J2-10	USB Line Adjust
J3 to/from Front Panel	
J3-1	Spare
J3-2	Key
J3-3	Phone Audio
J3-4	Audio Ground
J3-5	COR Wiper
J3-6	N/C
J3-7	Spare
J3-8	N/C
J3-9	Ground
J3-10	RF Gain
J3-11	+ 5 Vdc
J3-12	+ 15 Vdc
J3-13	Meter +
J3-14	Meter -

the ISB signal if the A18 ISB is installed. Either control will vary the 600 ohm line audio outputs level (available at rear panel connector TB1 and J7) from approximately -16 dBm to + 10 dBm.

The adjustment of R1 controls line audio level by adjusting the bias, and consequently the resistance across, an FET in the A5 line audio circuit. The FET therefore acts as an electronic attenuator for the line level. (See subsection A5.) R2 functions identically adjusting the bias on an FET located on the optional ISB IF/Audio Assembly A18.

4.3.3 Front Panel Control Signals

- RF GAIN

  5 Vdc is applied to the top of the front panel RF GAIN control, and a portion is fed back via the wiper to Control Assembly A14 A/D converter. This signal is used to manually control the receiver gain.

- COR

  + 15 Vdc is fed through R4, which results in 5 Vdc at the top of the front panel COR control. The wiper arm returns a portion of this to act as a COR threshold signal for COR circuits on the A5 assembly.

- HEADPHONES

  Headphone Audio from the A5 assembly is passed through the A13A3 assembly to a front panel HEADPHONE CONNECTOR. Headphone volume is adjustable via the AF GAIN control.

4.3.4 Parts Lists and Schematic Diagram

Table 8 is the Front Panel Meter Board A13A3 parts list. Figures 9 and 10 are the Front Panel Meter Board A13A3 component location diagram and schematic diagram.

Table 8. Front Panel Meter Board A13A3 Parts List (PL 10073-2300)

Ref. Desig.	Part Number	Description
J1	J-0870	CONNECTOR, 10 PIN
J2	J46-0032-010	HEADER, 10 PIN DISCRETE
J3	J46-0032-014	CONNECTOR, 14 PIN
R1	R30-0001-103	RES, VAR, 10K, 3/4W, 20%
R2	R30-0001-103	RES, VAR, 10K, 3/4W, 20%
R3	R65-0003-103	RES, 10K, 5%, 1/4, CAR FILM
R4	R65-0003-103	RES, 10K, 5%, 1/4, CAR FILM
S1	10073-2313	SWITCH, 4 POSITION

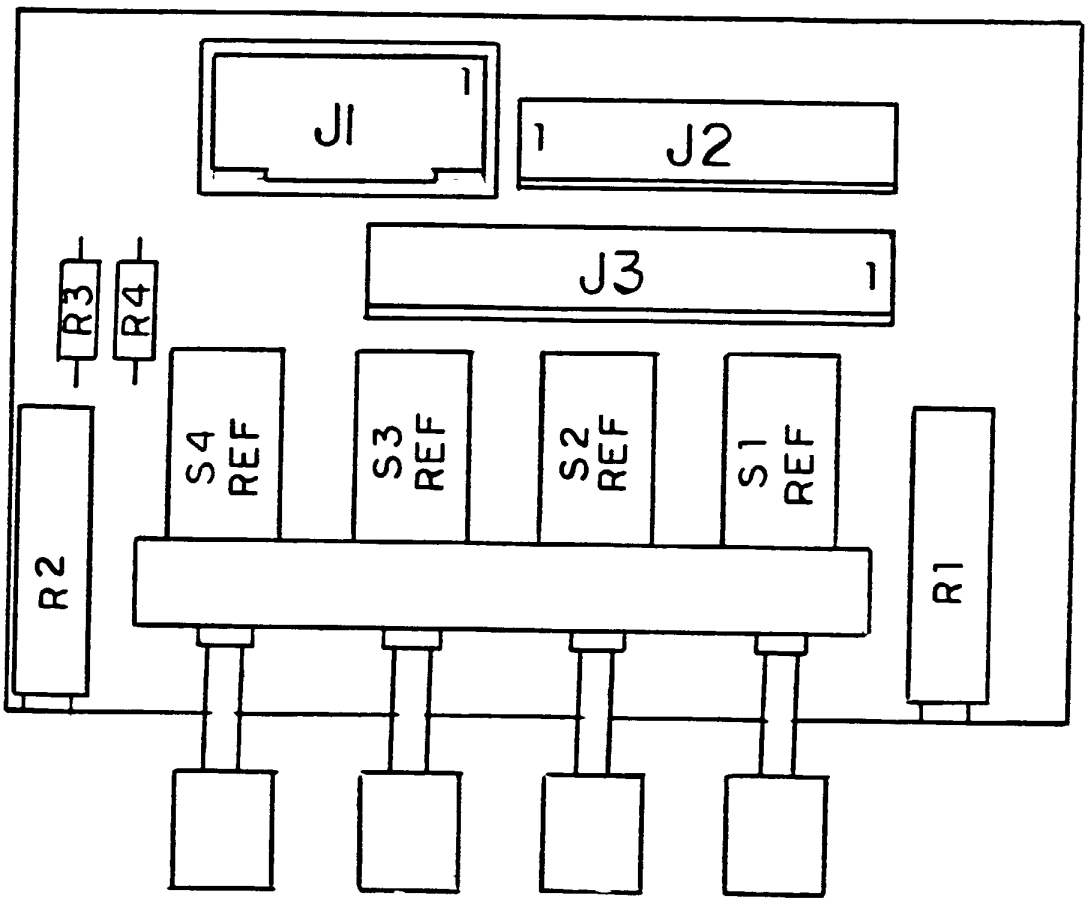


Figure 9. Front Panel Meter Board A13A3 Component Location Diagram (10073-2300)

NOTE: UNLESS OTHERWISE SPECIFIED:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR A COMPLETE DESIGNATION, PREFIX WITH UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.
2. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, ±5%.
3. VENDOR PART NO. CALLOUTS ARE FOR REFERENCE ONLY. COMPONENTS ARE SUPPLIED PER PART NO. IN PARTS LIST.
4. [ ] INDICATES FRONT PANEL MARKING.
5. S1-S4 SHOWN USB AF SELECTED.

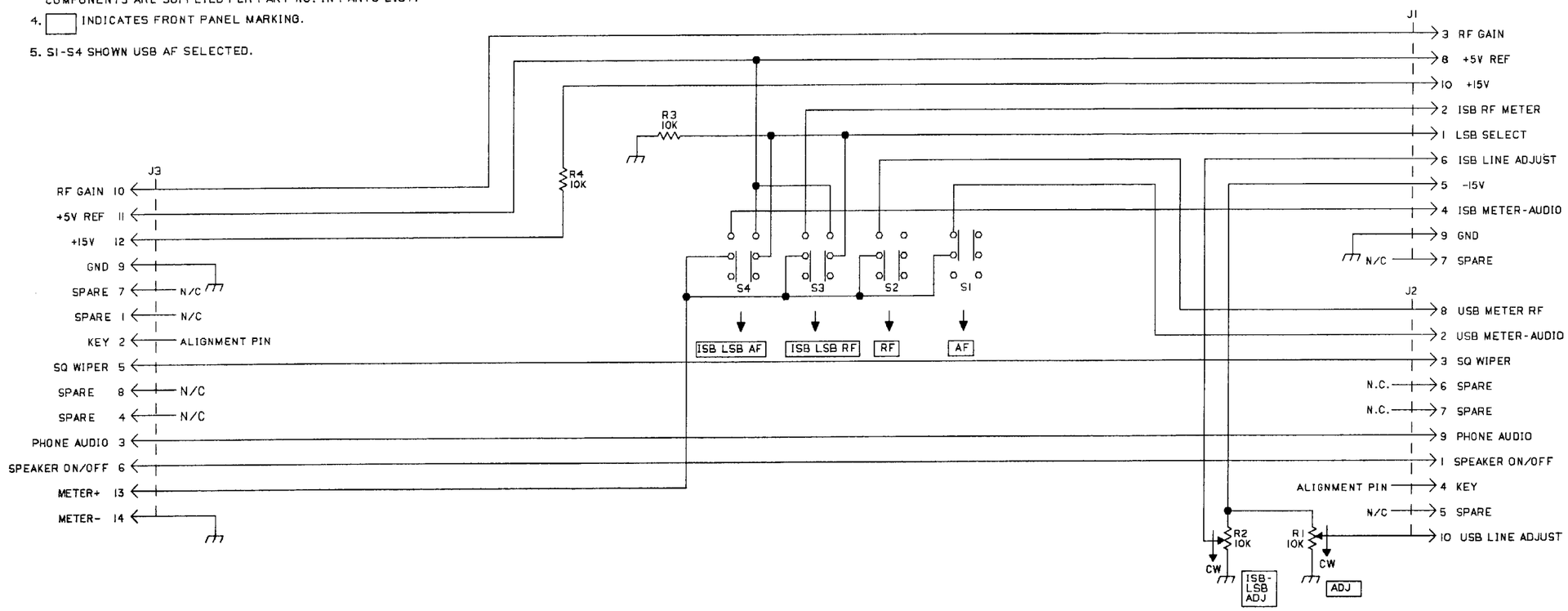


Figure 10. Front Panel Meter Board A13A3 Schematic Diagram (10073-2301, Rev. C)

5. ALPHANUMERIC DISPLAY ASSEMBLY A13A4

5.1 General Description

Alphanumeric Display Assembly A13A4 consists of a single vacuum fluorescent display which contains twenty fourteen segment (British flag) characters. The alpha display is used to provide indications of AGC, Mode, Bandwidth, and Dwell time in Scan Mode, Scan Group and BFO frequency. Additionally the alphanumeric display is used to prompt the operator for programming and scan related function selections. It is also used to provide fault indications, if any, at the completion of the BITE test.

5.2 Interface Connections

Table 9 lists the A13A4 interface connections.

Table 9. A13A4 Interface Connections

Connector	Description
J1 to/from A13A2	
J1-1	a Segment
J1-2	b Segment
J1-3	c Segment
J1-4	d Segment
J1-5	m Segment
J1-6	n Segment
J1-7	e Segment
J1-8	f Segment
J1-9	J Segment
J1-10	k Segment
J1-11	g Segment
J1-12	h Segment
J1-13	Decimal Point
J1-14	Comma
J1-15	N/C
J1-16	G1 Digit
J1-17	p Segment
J1-18	r Segment
J1-19	G2 Digit
J1-20	G3 Digit
J1-21	G20 Digit
J22	G4 Digit
J1-23	G5 Digit
J1-24	G6 Digit

Table 9. A13A4 Interface Connections (Cont.)

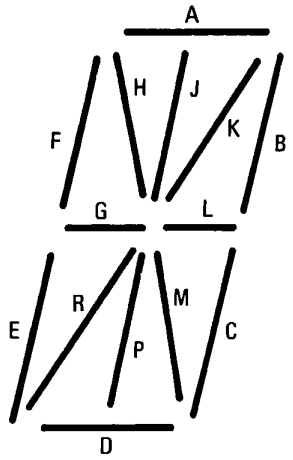
Connector	Description
J1-25	G19 Digit
J1-26	G7 Digit
J1-27	G8 Digit
J1-28	G9 Digit
J1-29	G18 Digit
J1-30	G10 Digit
J1-31	G11 Digit
J1-32	G12 Digit
J1-33	G17 Digit
J1-34	G13 Digit
J1-35	G14 Digit
J1-36	N/C
J1-37	G16 Digit
J1-38	G15 Digit
J1-39	Filament
J1-40	Filament

5.3 Functional Description

The alphanumeric vacuum fluorescent display is very similar in principle to the vacuum tube. Front Panel Driver Board A13A2 provides all required voltages and timing to properly drive the display. The 10073-2400 twenty character VF display requires a 4.7 Vac filament voltage and 35 Vdc grid and anode voltages. The grids (20 of them) are essentially character enable signals which are driven in multiplexed fashion, enabled one at a time as the segment data for that character is provided to the anode pins. The anode pins are inputs for the 14 segments plus dot and comma signals. Figure 10 shows the display's segment location. See paragraphs 3.1 and 3.3.3 for additional details.

5.3.1 Parts List and Schematic Diagram

Table 10 is the Alphanumeric Display A13A4 assembly parts list. Figures 12 and 13 are the Alphanumeric Display A13A4 component location diagram and schematic diagram.



590-102

Figure 11. Alphanumeric Display Segment Location

Table 10. Alphanumeric Display Assembly A13A4 Parts List (PL 10073-2400)

Ref. Desig.	Part Number	Description
DS1	N50-0006-001	DISPLAY,ALPHANUMERIC
J1	J46-0031-040	CONNECTOR,40 PIN

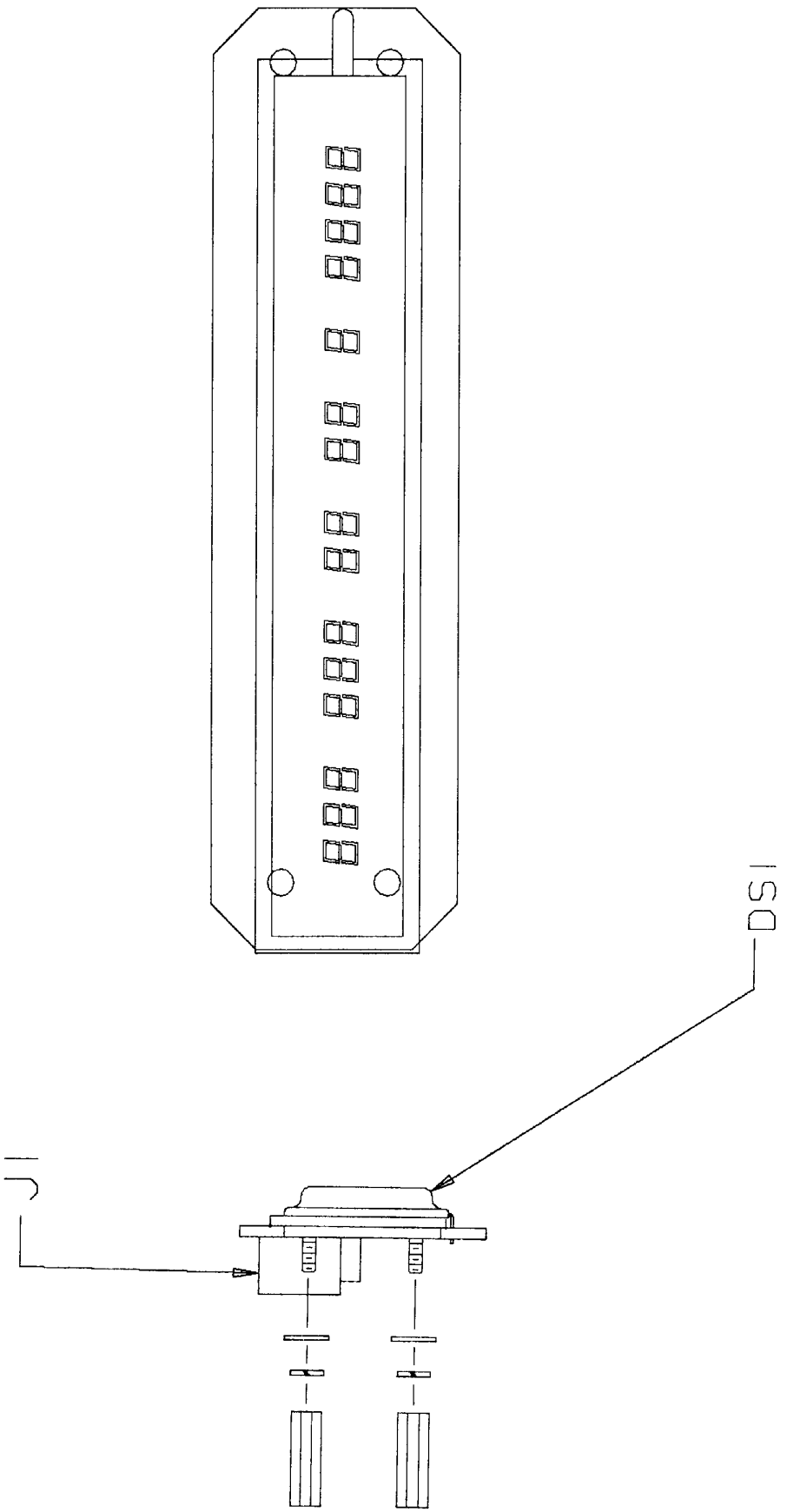


Figure 12. Alphanumeric Display Board A13A4 Component Location Diagram (10073-2400)

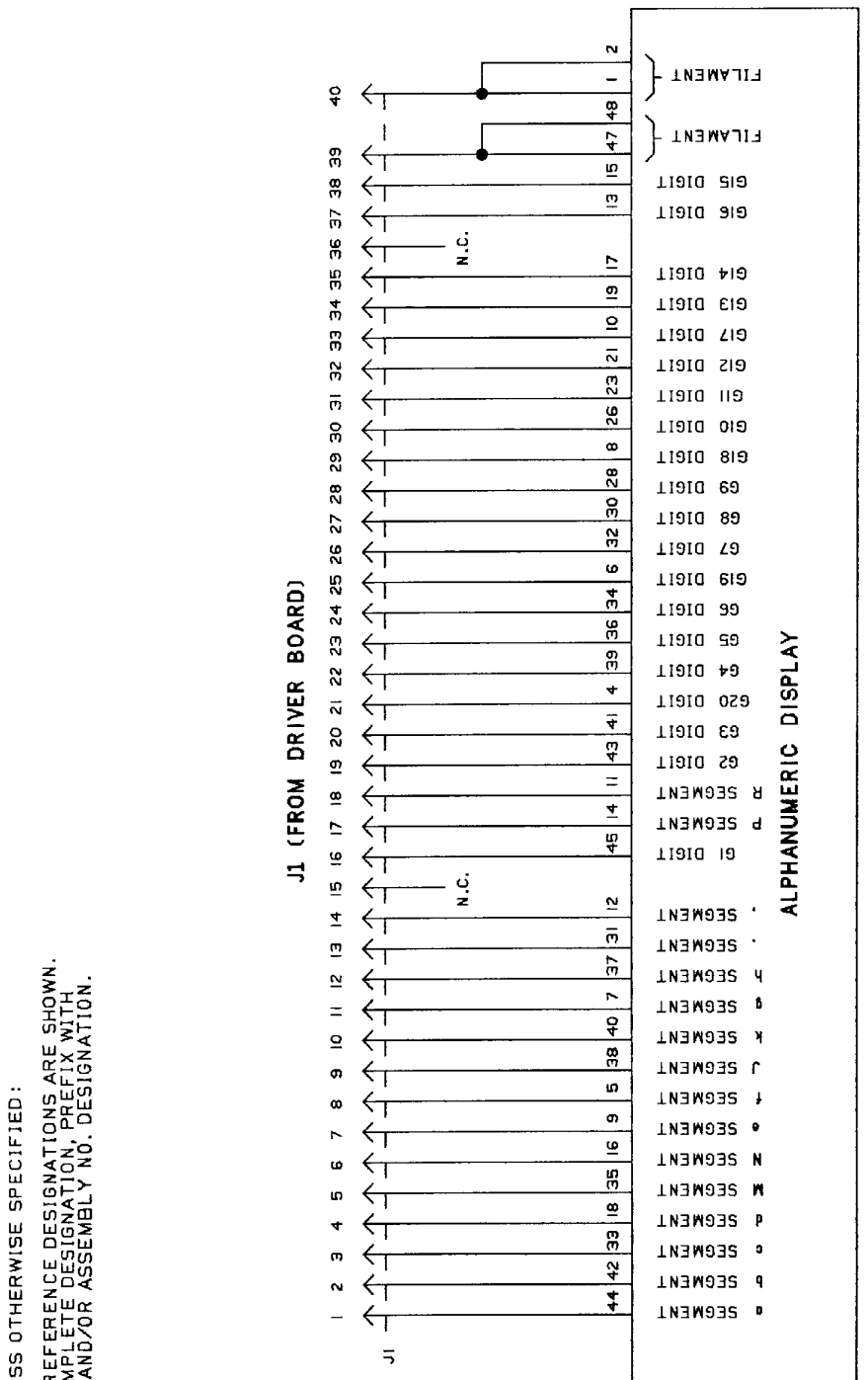


Figure 13. Alphanumeric Display Board A13A4 Schematic Diagram (10073-2401, Rev. B)

6. NUMERIC DISPLAY ASSEMBLY A13A5

6.1 General Description

Numeric Display Assembly A13A5 consists of a single vacuum fluorescent display which contains eight seven segment characters used for frequency display and two seven segment characters used for the channel display.

6.2 Interface Connections

Table 11 lists the A13A5 interface connections.

Table 11. A13A5 Interface Connections

Connector	Description
J1 to/from A13A2	
J1-1	G11 10 MHz Digit
J1-2	G10 1 MHz Digit
J1-3	G9 100 kHz Digit
J1-4	G3 1/2 Segments
J1-5	G7 1 kHz Digit
J1-6	G8 10 kHz Digit
J1-7	Filament
J1-8	Decimal Point
J1-9	G5 10 Hz Digit
J1-10	G6 100 Hz Digit
J1-11	N/C
J1-12	Comma
J1-13	G4 1 Hz Digit
J1-14	c Segment
J1-15	G2 CH10 Digit
J1-16	G1 CH1 Digit
J1-17	b Segment
J1-18	a Segment
J1-19	g Segment
J1-20	Filament
J1-21	Underline Segments
J1-22	d Segment
J1-23	e Segment
J1-24	f Segment

6.3 Functional Description

The numeric vacuum fluorescent display is very similar in principle to the vacuum tube. Front Panel Driver Board A13A2 provides all required voltages and timing signals to properly drive the display. The 10073-2500 VF display operates by using a 5.8 Vac filament voltage and 35 Vdc grid and anode voltages. The grids (ten of them) are character enable signals which are driven in a multiplexed fashion. The grids are enabled one at a time as the seven segment data plus underline, if required, are provided to the anode pins. Each digit is enabled for approximately 600 to 700 microseconds. Figure 14 shows the displays segment's location.

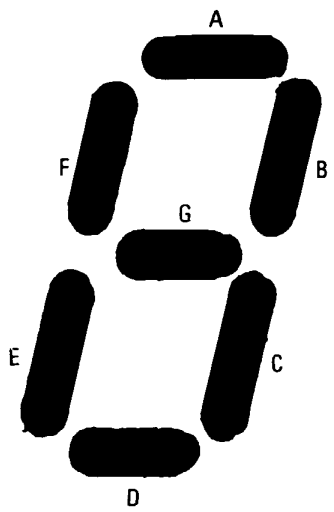


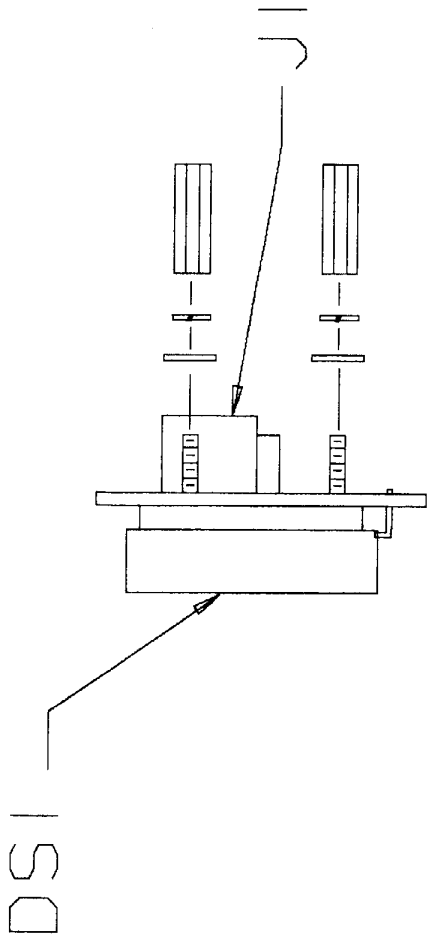
Figure 14. Numeric Display Segment Location

6.3.1 Parts List and Schematic Diagram

Table 12 is the Numeric Display Assembly A13A5 parts list. Figures 15 and 16 are the Numeric Display Assembly A13A5 component location diagram and schematic diagram.

Table 12. Numeric Display Assembly A13A5 Parts list (PL 10073-2500)

Ref. Desig.	Part Number	Description
DS1	N50-0005-001	DISPLAY,NUMERIC
J1	J46-0031-024	CONNECTOR,24 PIN



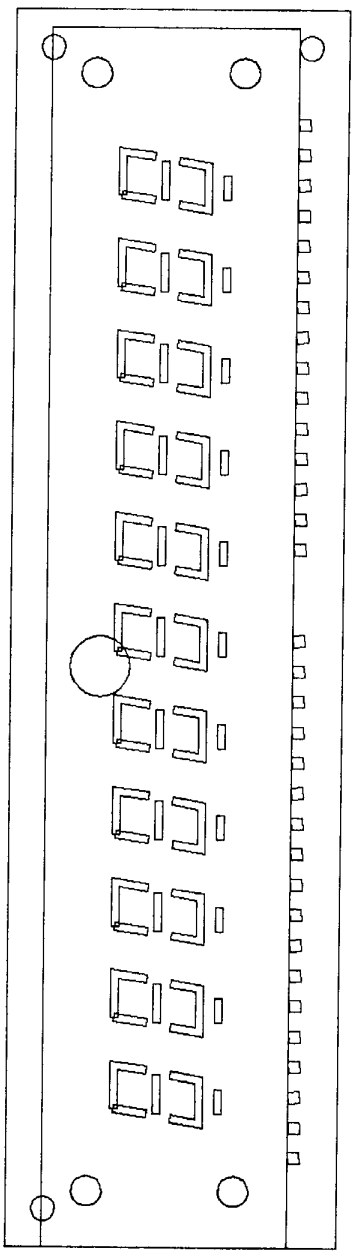


Figure 15. Numeric Display Board A13A5 Component Location Diagram (10073-2500)

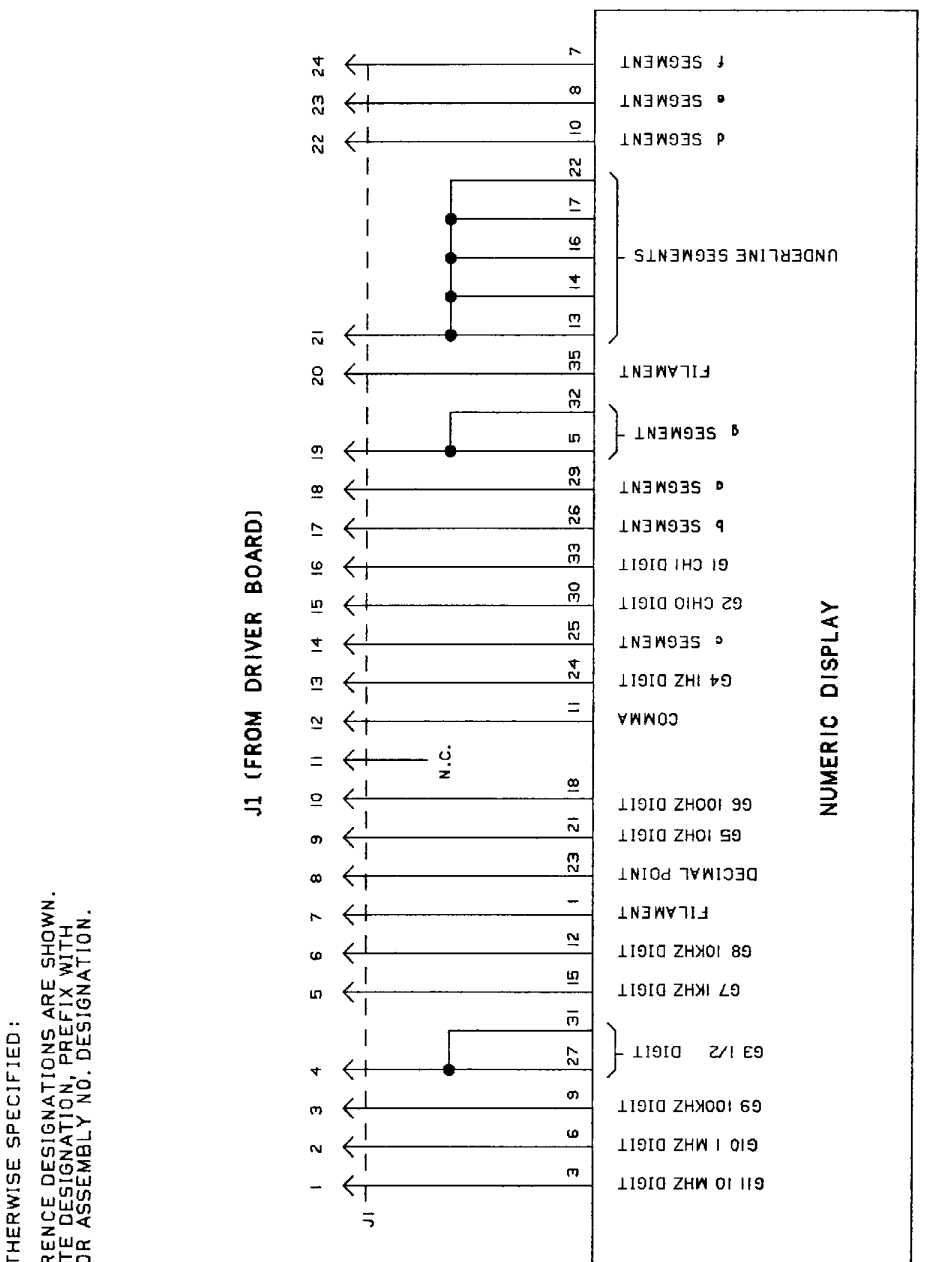


Figure 16. Numeric Display Board A13A5 Schematic Diagram (10073-2501, Rev. B)

NOTE: UNLESS OTHERWISE SPECIFIED:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR A COMPLETE DESIGNATION, PREFIX WITH UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.

A14
CONTROL BOARD ASSEMBLY

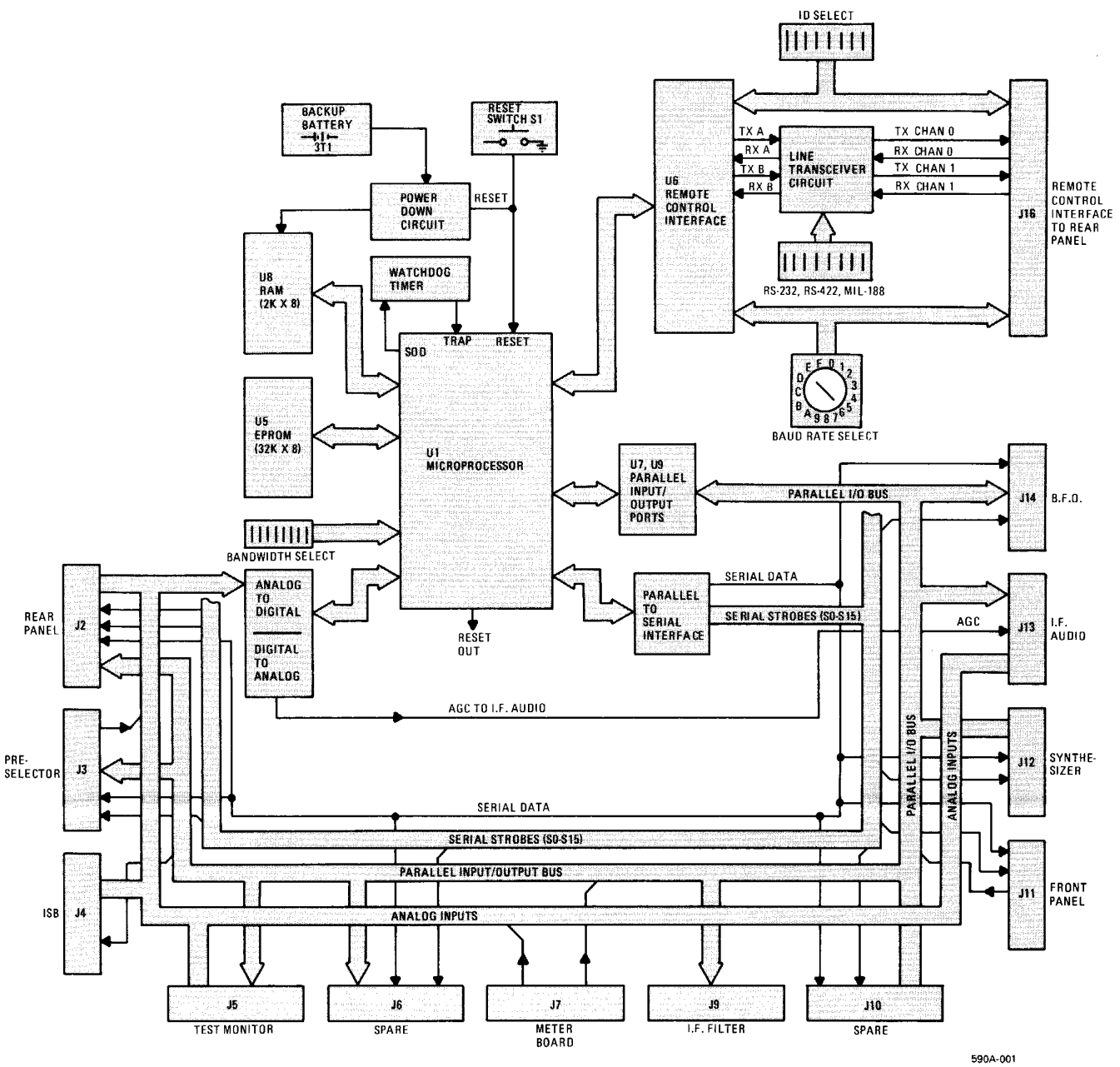


TABLE OF CONTENTS

Paragraph		Page
1.	Introduction	1
2.	Interface Connections	1
3.	Functional Description	7
3.1	CPU and Device Interfaces	7
3.2	Reset	8
3.3	Watchdog Timer	8
3.4	Memory	8
3.5	Parallel Input and Output Ports	12
3.6	Serial Input/Output	13
3.7	Analog-to-Digital and Digital-to-Analog Conversions	13
3.8	Bandwidth Selection Switches	15
3.9	Remote Control	15
4.	Maintenance	18
4.1	Alignment	18
4.2	Troubleshooting	18
4.2.1	CPU	18
4.2.2	Trap and Reset Circuits	19
4.2.3	Device Selection	19
4.2.4	Memory Circuits	20
4.2.5	Real Time Clock	20
4.2.6	Serial I/O	20
4.3	Parallel I/O	21
4.4	Analog I/O	21
4.4.1	Analog Inputs	21
4.5	Remote Control Interface	21
4.6	Faults Detected Through BITE	22
5.	Parts List	22
6.	Schematic Diagram	22

LIST OF FIGURES

Figure		Page
1	Control Assembly Functional Block Diagram	9
2	Memory Read Timing Diagram	11
3	Remote Control Serial Interface	16
4	Control Assembly A14 Component Location Diagram (10215-2800)	27
5	Control Assembly A14 Schematic Diagram (10215-2801)	29

LIST OF TABLES

Table		Page
1	Control Assembly A14 Interface Summary	2
2	U1 Terminal Assignments	7
3	Parallel Port Signal Assignments	12
4	Serial Strobe Assignments	14
5	Analog Input Assignments	14
6	Remote Control Interface Configuration Switch Settings	15
7	Serial Interface Baud Rate Switch Settings	17
8	ID Number Switch Weights	18
9	Operational Inputs for CPU	19
10	Operational Outputs for CPU	19
11	Significant Serial Data Transmission Circuits	20
12	Significant Analog Input Circuits	21
13	Fault Areas on Control Assembly A14	22
14	Control Assembly A14 Parts List (PL 10215-2800)	23

A14 CONTROL ASSEMBLY

1. INTRODUCTION

The A14 Control Assembly monitors, controls and tests most functions of the Receiver. The key component of the assembly is the eight-bit 8085A microprocessor. The microprocessor is supported by a 32-kilobyte EPROM loaded with the program, and a 8-kilobyte RAM used as a scratch pad and for semi-permanent storage of operating parameters for channelized operation. Both the EPROM and RAM can be expanded to accommodate special applications of the receiver. Other major components and circuits on the Control Assembly include:

- An 8155 RAM/Timer/I/O, and an 8255 programmable peripheral interface that provide parallel input and output ports to allow the microprocessor to monitor and control individual signals throughout the receiver. The timer in the 8155 generates a 1 kHz signal that is used to time software events. The RAM in the 8155 is not used in this application.
- An analog-to-digital converter and a digital-to-analog converter used to monitor analog functions and administrate the automatic gain control (AGC) respectively.
- A remote control interface built around a 2681 DUART.
- Assorted buffers, data transceivers, and latches to interface the microprocessor with other devices on and off the assembly.

The Control Assembly also features built-in protection against faults and glitches that would interrupt microprocessor operation, and power losses that would corrupt the memory. A watchdog timer is used to reset the microprocessor if operation is suspended or misdirected. The RAM is kept intact by a backup battery when the receiver is turned off or power is interrupted so that programmed channel parameters will not be lost.

The board is equipped with several switches that are used for maintenance functions and to define some operating parameters for the receiver. These switches are:

- A manual reset switch.
- An eight position DIP switch for identifying the bandwidth filter combination used.
- An eight position DIP switch used to set the unit ID for remote control applications.
- An eight position DIP switch and three pin jumper are used to select the interface type for remote control operation.
- A sixteen position rotary switch used to select the baud rate for the remote control interface.

2. INTERFACE CONNECTIONS

All Control Assembly interface connections are shown in table 1 and in the schematic diagram at the end of this section.

Table 1. Control Assembly A14 Interface Summary

Connector	Function	To	From
A14J1-1	N/C	--	--
A14J1-2	Index Key	--	--
A14J1-3	+ 5 V Reg	--	A15J3-9
A14J1-4	+ 5 VReg	--	A15J3-21
A14J2-1	4 ISB BITE Start	J7-1	--
A14J2-2	Serial Strobe 2	J7-20	--
A14J2-3	Gnd	J7-2	--
A14J2-4	Spare	--	--
A14J2-5	Scan Step	--	J7-3
A14J2-6	Remote Out 2	J7-22	--
A14J2-7	4 ISB Enable	J7-4	--
A14J2-8	Serial Strobe 1	J7-23	--
A14J2-9	Stop Scan	--	J7-5
A14J2-10	Serial Clock	J7-24	--
A14J2-11	4 ISB Detect	--	--
A14J2-12	Serial Data	J7-25	--
A14J2-13	Ext Mute	--	J7-7
A14J2-14	Fault	J7-26	--
A14J3-1	Noise Blank	--	A19J1-1
A14J3-2	Filter Id	--	A19J1-2
A14J3-3	Overload	--	A19J1-3
A14J3-4	Conv Id	--	A19J1-4
A14J3-5	Spare	A19J1-5	--
A14J3-6	Index Key	--	--
A14J3-7	Ext Mute	A19J1-7	--
A14J3-8	Enable	A19J1-8	--
A14J3-9	Serial Data	A19J1-9	--
A14J3-10	Serial Clock	A19J1-10	--
A14J4-1	Spare	--	--
A14J4-2	Int Mute	A18J1-9	--
A14J4-3	Det IF Input	--	A18J1-8
A14J4-4	Det Line Audio	--	A18J1-7
A14J4-5	AGC	--	A18J1-6
A14J4-6	Line Audio Adj	A18J1-5	--
A14J4-7	Ext Mute	A18J1-4	--
A14J4-8	Index Key	--	--
A14J4-9	ISB Audio Meter	--	A18J1-2
A14J4-10	ISB AGC Meter	--	A18J1-1
A15J5-1	Spare	--	--
A15J5-2	A3 Det	--	A16A2J2-3
A15J5-3	A2 Det	--	A16A2J2-4
A15J5-4	A1 Ext Mute	A16A3J3-1	--
A15J5-5	A1 Relay Control	A16A3J3-4	--
A15J5-6	A1 Relay Test	A16A3J3-5	--
A15J5-7	A1 BITE Osc Enab	A16A3J3-6	--

Table 1. Control Assembly A14 Interface Summary (Cont.)

Connector	Function	To	From
A15J5-8	A1 Ant Overload	--	A16A3J3-7
A15J5-9	A1 BITE det Out	--	A16A3J3-8
A15J5-10	A6 PLL I Lock Det	--	A16A3J3-1
A15J5-11	A9 PLL IV Lock Det	--	A16A3J3-3
A15J5-12	A12 800 kHz Det	--	A16A3J3-4
A15J5-13	A12 1 MHz Det	--	A16A3J3-5
A15J5-14	A12 PLL Lock Det	--	A16A3J3-6
A14J6-1	Serial Data	A7J1-1	--
A14J6-2	Serial Clock	A1J1-2	--
A14J6-3	Index Key	--	--
A14J6-4	Serial Check 1	--	A7J1-4
A14J6-5	Enable	A7J1-5	--
A14J6-6	PLL 2 Lock Det	--	A7J1-6
A14J6-7	Gnd	A7J1-7	--
A14J6-8	Spare	--	--
A14J7-1	LSB Select	--	A13A3J1-1
A14J7-2	ISB AGC Meter	A13A3J1-2	--
A14J7-3	RF Gain	--	A13A3J1-3
A14J7-4	ISB Audio	A13A3J1-4	--
A14J7-5	-15 V	A13A3J1-5	--
A14J7-6	LSB Audio Adj	--	A13A3J1-6
A14J7-7	+8.5 V	--	--
A14J7-8	+5 V Ref	A13A3J1-8	--
A14J7-9	Gnd	A13A3J1-9	--
A14J7-10	+15 V	A13A3J1-10	--
A14J8-1	BITE P/S	--	A15J3-22
A14J8-2	Spare	--	--
A14J8-3	+15 V Reg	--	A15J3-23
A14J8-4	-15 V Reg	--	A15J3-11
A14J8-5	Index Key	--	--
A14J8-6	+5 V Unreg	--	A15J3-12
A14J8-7	Gnd	--	A15J3-25
A14J8-8	Gnd	--	A15J3-13
A14J9-1	Spare	--	--
A14J9-2	Spare	--	--
A14J9-3	D3	A4J5-9	--
A14J9-4	D0	A4J5-8	--
A14J9-5	D2	A4J5-7	--
A14J9-6	Index Key	--	--
A14J9-7	D1	A4J5-5	--
A14J9-8	Gnd	A4J5-4	--
A14J10-1	Serial Data	--	--
A14J10-2	Serial Clock	--	--
A14J10-3	Index Key	A4J5-9	--
A14J10-4	Serial Check 1	A4J5-8	--

Table 1. Control Assembly A14 Interface Summary (Cont.)

Connector	Function	To	From
A14J10-5	Enable	A8J4-5	--
A14J10-6	PLL 3 Lock Det	--	A8J4-6
A14J10-7	Gnd	A8J4-7	--
A14J10-8	Spare	--	--
A14J11-1	Twhl Int	--	A13A2J1-1
A14J11-2	Serial Data	A13A2J1-2	--
A14J11-3	Twhl Direction	--	A13A2J1-3
A14J11-4	Serial Clock	A13A2J1-4	--
A14J11-5	Twhl Reset	A13A2J1-5	--
A14J11-6	-15 V	A13A2J1-6	--
A14J11-7	+5 V	A13A2J1-7	--
A14J11-8	BITE P/S	A13A2J1-8	--
A14J11-9	PB3	A13A2J1-9	--
A14J11-10	Kyb Strobe	A13A2J1-10	--
A14J11-11	PB2	A13A2J1-11	--
A14J11-12	Fault	--	A13A2J1-12
A14J11-13	PB1	A13A2J1-13	--
A14J11-14	Display Strobe	A13A2J1-14	--
A14J11-15	PB0	A13A2J1-15	--
A14J11-16	Reset	A13A2J1-16	--
A14J11-17	Spare	--	--
A14J11-18	GND	A13A2J1-18	--
A14J11-19	+8.5 V	A13A2J1-19	--
A14J11-20	GND	A13A2J1-20	--
A14J12-1	Serial Data	A10J1-1	--
A14J12-2	Serial Clock	A10J1-2	--
A14J12-3	Index Key	--	--
A14J12-4	Serial Check 1	--	A10J1-4
A14J12-5	Enable	A10J1-5	--
A14J12-6	PLL 5 Lock Det	--	A10J1-6
A14J12-7	Gnd	A10J1-7	--
A14J12-8	N/C	--	--
A14J13-1	Gnd	A5J6-1	--
A14J13-2	RF GAin 0-10 V	A5J6-2	--
A14J13-3	Data AGC	--	--
A14J13-4	AGC Off	A5J6-4	--
A14J13-5	C Audio Select	A5J6-5	--
A14J13-6	Int Mute	A5J6-6	--
A14J13-7	B Audio Select	A5J6-7	--
A14J13-8	Fast AGC	A5J6-8	--
A14J13-9	A Audio Select	A5J6-9	--
A14J13-10	Medium AGC	A5J6-10	--
A14J13-11	EXT Mute	A5J6-11	--
A14J13-12	Line Audio	--	--

Table 1. Control Assembly A14 Interface Summary (Cont.)

Connector	Function	To	From
A14J13-13	Mute	--	A5J6-13
A14J13-14	Line Audio Det Out	--	A4J6-14
A14J13-15	IF Input Det	--	A5J6-15
A14J13-16	Second IF AGC	--	A5J6-16
A14J14-1	Serial Data	A11J4-1	--
A14J14-2	Serial Clock	A11J4-2	--
A14J14-3	Index Key	--	--
A14J14-4	Serial Check 1	--	A11J4-4
A14J14-5	Enable	A11J4-5	--
A14J14-6	BFO Lock Detect	--	A11J4-6
A14J14-7	Gnd	A11J4-7	--
A14J14-8	BFO On/Off	A11J4-8	--
A14J15-1	+8.5 V	A17J1-1	--
A14J15-2	+8.5 V	A17J1-2	--
A14J15-3	Reset Out	A17J1-3	--
A14J15-4	HOLD	--	A17J1-4
A14J15-5	Spare	A17J1-5	--
A14J15-6	HLDA	A17J1-6	--
A14J15-7	Spare	A17J1-7	--
A14J15-8	3 MHz Clock	A17J1-8	--
A14J15-9	+15 V	A17J1-9	--
A14J15-10	Gnd	A17J1-10	--
A14J15-11	Ready	--	A17J1-11
A14J15-12	-15 V	A17J1-12	--
A14J15-13	RST 5.5	--	A17J1-13
A14J15-14	IO/M	A17J1-14	--
A14J15-15	INTR	--	A17J1-15
A14J15-16	S1	A17J1-16	--
A14J15-17	WR	A17J1-17	--
A14J15-18	RD	A17J1-18	--
A14J15-19	INTA	A17J1-19	--
A14J15-20	ALE	A17J1-20	--
A14J15-21	Spare	--	--
A14J15-22	Spare	--	--
A14J15-23	AD0	A17J2-3	Bi direc
A14J15-24	Spare	--	--
A14J15-25	AD1	A17J2-5	Bi direc
A14J15-26	A15	A17J2-6	--
A14J15-27	AD2	A17J2-7	Bi direc
A14J15-28	A14	A17J2-8	--
A14J15-29	AD3	A17J2-9	Bi direc
A14J15-30	A13	A17J2-10	--
A14J15-31	AD4	A17J2-11	Bi direc
A14J15-32	A12	A17J2-12	--
A14J15-33	AD5	A17J2-13	Bi direc
A14J15-34	A11	A17J2-14	--

Table 1. Control Assembly A14 Interface Summary (Cont.)

Connector	Function	To	From
A14J15-35	AD6	A17J2-15	Bi direc
A14J15-36	A10	A17J2-16	--
A14J15-37	AD7	A17J2-17	Bi direc
A14J15-38	A9	A17J2-18	--
A14J15-39	Gnd	A17J2-19	--
A14J15-40	A8	A17J2-20	--
A14J16-1	N/C	--	--
A14J16-2	Rx Chan 1 +	--	Rear Panel
A14J16-3	Rx Chan 0 +	--	Rear Panel
A14J16-4	Rx Chan 1 -	--	Rear Panel
A14J16-5	ID	Rear Panel	--
A14J16-6	Baud 2	Rear Panel	--
A14J16-7	Baud 0	Rear Panel	--
A14J16-8	Baud 1	Rear Panel	--
A14J16-9	Baud 3	Rear Panel	--
A14J16-10	Id	Rear Panel	--
A14J16-11	Tx Chan 1 +	Rear Panel	--
A14J16-12	ID	Rear Panel	--
A14J16-13	Tx Chan 1 -	Rear Panel	--
A14J16-14	Ground	Rear Panel	--
A14J16-15	Ground	Rear Panel	--
A14J16-16	ID	Rear Panel	--
A14J16-17	ID	Rear Panel	--
A14J16-18	N/C	--	--
A14J16-19	ID	Rear Panel	--
A14J16-20	N/C	--	--
A14J16-21	ID	Rear Panel	--
A14J16-22	Rx Chan 0 -	--	--
A14J16-23	ID	Rear Panel	--
A14J16-24	Tx Chan 0 -	Rear Panel	--
A14J16-25	Tx Chan 0 +	Rear Panel	--
A14J16-26	N/C	--	--
A14J18-1	Rx Chan 0 +	--	--
A14J18-2	Rx Chan 0 -	--	--
A14J18-3	N/C	--	--
A14J18-4	Tx Chan 0 +	--	--
A14J18-5	Tx Chan 0 -	--	--
A14J18-6	Aux 2	--	--
A14J18-7	Aux 1	--	--
A14J18-8	Ground	--	--

3. FUNCTIONAL DESCRIPTION

The following paragraphs describe the operation of the Control Assembly in general terms. The major components and circuits of the board are shown as functional blocks in figure 1. A complete schematic of the Control Assembly is included at the end of this section.

3.1 CPU and Device Interfaces

The heart of the Control Assembly is the eight-bit, 8085A microprocessor U1. The processor executes the applications program resident in the EPROM U5. Processor timing is derived from the 6.0 MHz crystal oscillator Y1. The microprocessor divides the signal by 2 to yield a processor cycle time of 333 nanoseconds and an output clock (CLK) of 3 MHz. The processor is linked to the other devices on the board and other assemblies in the receiver by a bus network. The eight data bits and the eight least significant address bits are multiplexed on one bus and the eight most significant address bits are on a second bus. The lower address bits are latched into U3 by the ALE signal. The functions of all the inputs and outputs of the microprocessor are summarized in table 2.

Table 2. U1 Terminal Assignments

Pin	Symbol	Function
1 and 2	X1 and X2	6 MHz clock crystal input from Y1
3	RESET OUT	System reset out to all devices
4	SOD	Serial Output Data Line - Reset to watchdog timer sent every millisecond
5	SID	Serial Input Data Line - Serial ID data from parallel-to-serial converter U26
6	TRAP	Interrupt from watchdog timer
7	RST 7.5	1 kHz signal from timer section of U7
8	RST 6.5	Interrupt from tuning wheel on the front panel
9	RST 5.5	Remote control interrupt from U6 or A17
10	INTR	Not used
11	INTA	Interrupt acknowledge to U2 or A17
12 thru 19	AD_0 thru AD_7	Multiplexed address and data bus
20	V_{ss}	Ground
21 thru 28	A_8 thru A_{15}	Higher order address bits
29	S0	Not used
30	ALE	Address Latch Enable - Latches lower order address bits into U3
31	WR	Write - Low active signal to all devices when data is to be written into memory or peripheral device.
32	RD	Read - Low active signal to all devices when data is to be read from memory or peripheral device
33	S1	Not used
34	IO/M	Enable Memory (low) or IO device (high) for read or write.
35	READY	Not used

Table 2. U1 Terminal Assignments (Cont.)

Pin	Symbol	Function
36	RESET IN	Reset into U1 from power up circuit, power down circuit or RESET switch (S1)
37	CLK	3 MHz clock from U1 to all devices
38	HLDA	Not used
39	HOLD	Not used
40	V_{CC}	+ 5 Volts

3.2 Reset

A microprocessor reset is initiated automatically upon power up and when the unit is powered down. Pushbutton switch S1 is provided to initiate a manual reset. All resets are initiated by pulling the RESET-NOT input to the microprocessor low. At power up, the RC network made up of R10 and C26 holds the RESET input low for about 100 milliseconds. This initializes all the hardware and sets the program counter to zero.

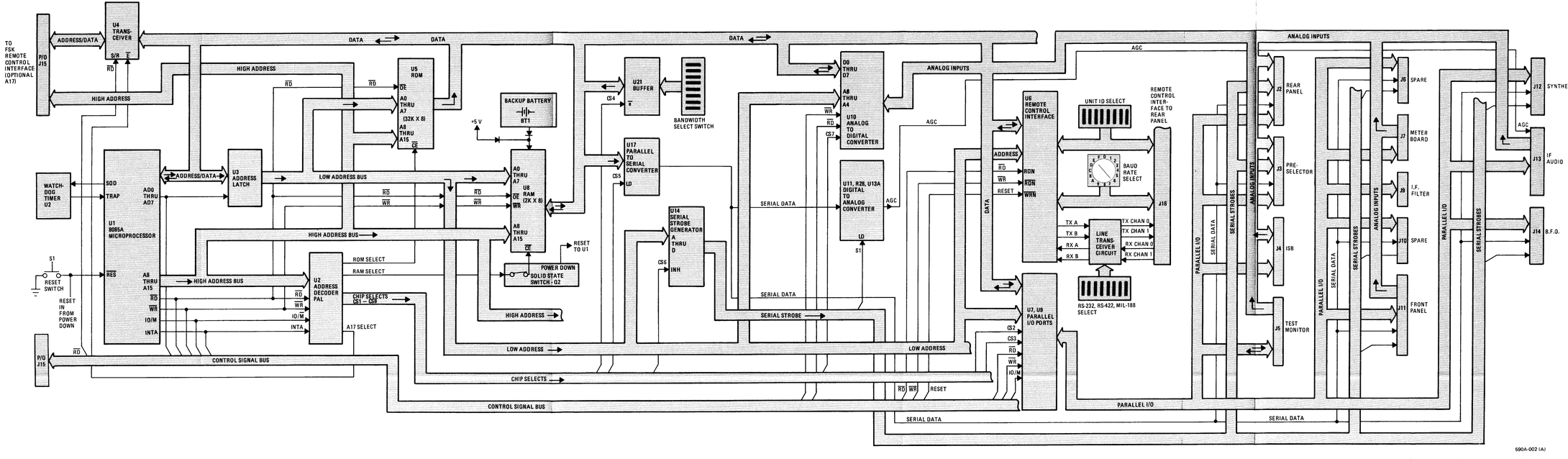
The power down circuit issues a reset command and disables the RAM at the first notice of a power failure to avoid spurious operation and corruption of the memory. U23D and U23B are comparators used to detect a low voltage condition. The non-inverting (+) input of U23D is held at 2.5 volts by diode CR6. This is compared to the voltage at the junction of R44 and R45 that is normally near 2.74 volts when the 5 volt supply is operating properly. The output of U23D is near 0 when the + 5 volt supply is functioning properly. In the event of a power failure, the voltage at the junction of R44 and R45 will drop below 2.5 volts and drive the output of U23D high (towards + 5 volts). This signal is applied to the inverting (-) input of U23B and will drive its output low to hold the microprocessor in the reset state until power is restored. At the same time the high output from U23D is applied to the inverting (-) input of U23A to drive its output low. This turns Q2 off to disable the RAM preventing corruption during the low power state. R13 and C13 introduce a short delay to ensure that the RAM is disabled after bus activity has been completed.

3.3 Watchdog Timer

The watchdog timer, U20, protects against glitches or soft errors that might misdirect or hang-up the microprocessor. The timer is essentially a monostable multivibrator that is continually retriggered by the microprocessor at regular intervals during normal operation. If there is a significant lapse in the retrigger signal, the monostable multivibrator changes state and the timer pulls the TRAP input to the microprocessor high to start a reset. The timer is initially triggered when the power up reset is applied to the microprocessor. Activation of the TRAP input starts a "watch dog time out "program that effectively resets the Receiver.

3.4 Memory

The Control Assembly is equipped with an 32K X 8 EPROM and an 8K X 8 RAM in its minimum memory configuration. The EPROM storage can be expanded to 64K X 8 and the RAM can be expanded to 32K X 8 for special applications. The EPROM is socket mounted. Note that jumpers JMP 1 thru JMP 4 must be positioned properly for the memory size supplied. Jumper positions are shown on the schematic diagram. The PAL U2 must also be programmed for the size of memory installed.



590A-002 (A)

Figure 1. Control Assembly Functional Block Diagram

CAUTION

EPROMs are ultraviolet erasable and can be erased by extended periods of exposure to fluorescent light or sunlight. Do not remove the opaque protective shield on these devices.

The microprocessor uses memory reads and writes to access the RAM and the EPROM. Chip Enables for the EPROM and the RAM are generated by U2, a PAL configured to decode high order addresses and control commands. The read command, RD-NOT, is applied directly to output enable of the EPROM, U5. The read command, RD-NOT, and the write command WR-NOT are likewise applied directly to the RAM U8.

A memory read or write begins with the microprocessor placing the address on the address bus (see figure 2). The lower order address bits are latched into U3 by the active high Address Latch Enable (ALE). U3 is a transparent latch, its outputs will reflect its inputs whenever ALE is high. The data present at the inputs when ALE goes low is retained. The PAL decodes its inputs and issues the Chip Select for the EPROM or RAM as required. After the ALE signal goes low, the lower order address bits are cleared from the Address/Data bus so that data can be sent or received on it. The read or write command is issued and data is transferred on the Address/Data bus to complete the cycle.

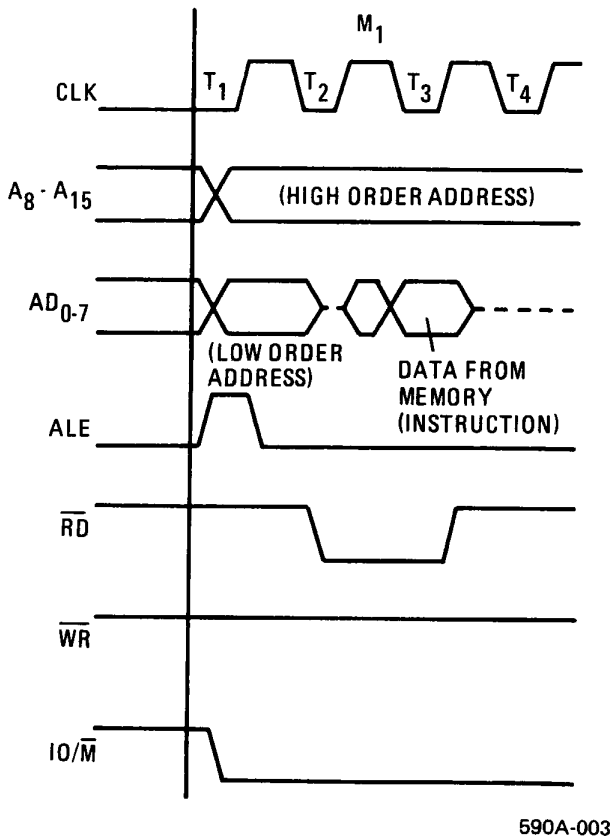


Figure 2. Memory Read Timing Diagram

The RAM is backed up with a rechargeable Ni- Cad battery so that parameters for programmed channels will not be lost when the receiver is turned off or power is interrupted. Diodes CR1 and CR2 act as a switch for the back up battery. As long as the + 5 volt supply is active, CR1 will be forward biased and CR2 will be reverse biased to keep the battery from discharging. When the + 5 volt supply fails, CR2 automatically becomes forward biased so the battery can keep the memory intact. Jumper J17 should only be installed to activate the backup battery. Care must be taken not to accidently short the leads of either battery. If the Ni-Cad battery is shorted, the memory will be erased and the battery may be damaged.

CAUTION

DO NOT short backup battery terminals. A shorted battery will overheat destroying the battery and damaging the PWB assembly.

3.5 Parallel Input and Output Ports

U7 and U9 provide a total of 46 parallel ports. U7, a 8155 type RAM/TIMER/I/O has three paralled ports that are configured as an eight-bit input port, an eight-bit output port and a six-bit output port. U9, an 8255 type programmable peripheral interface with three programmable parallel interfaces, adds two, 8-bit input ports and one eight-bit output port. Both devices are accessed by the microprocessor as input/output devices and are enabled by chip selects generated at the PAL U2. U7 is enabled by CS2 and U9 is enabled by CS3. Several receiver functions are monitored and controlled via these ports. The control signals associated with each port are listed in table 3.

Table 3. Parallel Port Signal Assignments

Device and Pin	A14 Sig. Name	Destination Signal Name	Destination
U7-21	1PA0	SCAN STEP	Rear Panel
U7-22	1PA1	STOP SCAN	Rear Panel
U7-23	1PA2	A8 PLL LOCK DET	PLL III
U7-24	1PA3	SER CHK 1	PLL III
U7-25	1PA4	A10 PLL 5 LOCK DET	Synthesizer A10
U7-26	1PA5	SER CHK 1	Synthesizer A10
U7-27	1PA6	A11 BFO LOCK DET	B.F.O.
U7-28	1PA7	SER CHK 1	B.F.O.
U7-29	1PB0	C AUDIO SEL	I.F. AUDIO
U7-30	1PB1	B AUDIO SEL	I.F. AUDIO
U7-31	1PB2	A AUDIO SEL	I.F. AUDIO
U7-32	1PB3	AGC OFF	I.F. AUDIO
U7-33	1PB4	FAST AGC	I.F. AUDIO
U7-34	1PB5	MED AGC	I.F. AUDIO
U7-35	1PB6	INT MUTE	I.F. AUDIO and ISB
U7-36	1PB7	BFO ON/OFF	B.F.O.
U7-37	1PC0	D0	I.F. AUDIO
U7-38	1PC1	D1	I.F. AUDIO
U7-39	1PC2	D2	I.F. AUDIO
U7-1	1PC3	D3	I.F. AUDIO
Y7-2	1PC4	NOT USED	
U7-3	1PC5	NOT USED	

Table 3. Parallel Port Signal Assignments (Cont.)

Device and Pin	A14 Sig. Name	Destination Signal Name	Destination
U9-4	2PA0	A1 RELAY TEST-NOT	TEST MONITOR
U9-3	2PA1	A1 BITE OSC ENABLE	TEST MONITOR
U9-2	2PA2	NOT USED	
U9-1	2PA3	A1 RELAY CONT	TEST MONITOR
U9-40	2PA4	4 ISB ENABLE	Rear Panel
U9-39	2PA5	4 ISB BITE START	Rear Panel
U9-38	2PA6	REMOTE OUT 2	Rear Panel
U9-37	2PA7	NOISE BLANK	PRESELECTOR
U9-24	2PB6	A12 1 MHz DET	TEST MONITOR
U9-25	2PB7	EOC	U10-13
U9-18	2PB0	A1 ANT OVERLOAD	TEST MONITOR
U9-19	2PB1	CONV ID	PRESELECTOR
U9-20	2PB2	A6 PLL LOCK DET	TEST MONITOR
U9-21	2PB3	A9 PLL LOCK DET	TEST MONITOR
U9-22	2PB4	A12 PLL LOCK DET	TEST MONITOR
U9-23	2PB5	A12 800 kHz DET	TEST MONITOR
U9-14	2PC0	PB0	Front Panel
U9-15	2PC1	PB1	Front Panel
U9-16	2PC2	PB2	Front Panel
U9-17	2PC3	PB3	Front Panel
U9-13	2PC4	TWHL DIR	Front Panel
U9-12	2PC5	LSB SELECT	METER BOARD
U9-11	2PC6	SER CHK 1	PLL II
U9-10	2PC7	PLL 2 LOCK DET	PLL II

3.6 Serial Input/Output

Data can be sent from the microprocessor to other assemblies in the receiver and the digital-to-analog converter on the A14 assembly via a synchronous serial data interface. The key components of the parallel to serial interface are the parallel- to-serial converter U17 and the serial strobe generator U14. Both are accessed by the microprocessor as I/O devices with CS5 enabling U17 and CS6 enabling U14. Flip-flop U16 is configured as a divider and generates 750 kHz serial clock from the 3 MHz clock signal supplied by the microprocessor. The 750 kHz clock drives U17 and is sent to all assemblies and devices that receive serial data. Parallel data is written into U17 triggering the device to shift the data out on the serial line , high order bit first. U18 keeps track of the bit count and clears U16 after 8 bits to end the data transmission. U14 decodes address bits A0 thru A3 to generate the serial strobes. Each strobe enables one assembly or device to receive the data transmitted on the common line. Table 4 lists the strobes and their destinations.

3.7 Analog-to-Digital and Digital-to-Analog Conversions

U10 is an analog-to-digital converter that is accessed as an I/O device. The device receives analog inputs from a number of sources and converts them into 8 bit wide words that are read by the microprocessor. The analog inputs are used for AGC and BITE and are listed in table 5 along with their assignments.

Table 4. Serial Strobe Assignments

Origin	Strobe	Destination	Signal at Destination
U14-11	S0	Synthesizer	ENABLE
U14-9	S1	D TO A CONV U11	LD
U14-10	S2	PLL III	ENABLE
U14-8	S3	PLL II	ENABLE
U14-7	S4	Rear Panel	STROBE 1
U14-6	S5	Rear Panel	STROBE 2
U14-5	S6	Front Panel	DISPLAY STROBE
U14-4	S7	Front Panel	KYB STROBE
I14-18	S8	B.F.O.	ENABLE
U14-17	S9	Preselector	ENABLE
U14-30	S10	Front Panel	TWHL RESET

Table 5. Analog Input Assignments

U10 Input	Signal	Origin	Signal at Origin
U10-38	ADC0	Rear Panel	4 ISB DETECT
U10-40	ADC2	U13A-1	RF GAIN (D to A Feedback)
U10-1	ADC3	Test Monitor	A3 DET
U10-3	ADC5	ISB	DET IF INPUT
U10-4	ADC6	Test Monitor	A1 BITE DET OUT
U10-5	ADC7	Test Monitor	A2 DETECT
U10-6	ADC8	Meter Board	RF GAIN
U10-7	ADC9	Preselector	FILTER ID
U10-8	ADC10	ISB	AGC
U10-10	ADC12	I.F. Audio	2ND IF AGC
U10-11	ADC13	I.F. Audio	IF INPUT DETECT
U10-12	ADC14	I.F. Audio	LINE AUDIO DET OUT
U10-14	ADC15	ISB	DET LINE AUDIO

Most of the analog inputs are used by the BITE routine to check for the presence or absence of signals. Addresses A0 thru A3 are used to select an analog input for conversion. U10 generates the End Of Conversion (EOC) signal when the analog signal gas been converted to an 8 bit digital quantity. The EOC is returned to the microprocessor via U9. The RF GAIN signal, originating on the front panel, is used to control the front end gain of the receiver. The level of the dc signal is set between 0 and 9 volts by the RF GAIN control. The signal is sampled every 50 milliseconds. The analog signal is converted to a digital equivalent and read by the

microprocessor. The microprocessor evaluates the signal and sends a corresponding control signal to the digital-to-analog converter, U11 via the parallel-to-serial converter. U11 generates a voltage that is sent to A2 via buffer amplifier U13A.

Both U10 and U11 receive their reference voltage inputs from + 5 volt low power regulator, VR1.

3.8 Bandwidth Selection Switches

Several optional combinations of IF filters are available for the Receiver. DIP switch S2 is used to define the combination of filters installed in an individual receiver. S2 is read by the microprocessor via switch buffer U21 as an I/O device. The buffer is enabled by chip select CS4. Switches S2-4 thru S2-8 are used to identify the filter combination used. Switches S2-1, S2-2, and S2-3 are used to indicate the presence or absence of filters for AM, CW and FSK modes. An open switch indicates the presence of the filter, a closed switch indicates that the filter position is empty.

The switch configurations are factory set and should not have to be altered in the field. If the A14 assembly is replaced, the switches on the new assembly should be set to match the switch settings on the old assembly. The standard setitng for S2 are:

S2-1 Closed	S2-5 Closed
S2-2 Open	S2-6 Closed
S2-3 Closed	S2-7 Open
S2-4 Open	S2-8 Closed

3.9 Remote Control

The remote control interface for the receiver is part of the A14 Assembly. The interface is built around a SCN2681 DUART, U6. The DUART features two serial channels, a seven bit input port, an eight bit output port, a timer and an interrupt controller. The DUART communicates with the microprocessor via an 8-bit bidirectional bus. The DUART is accessed by the microprocessor as an I/O device that is enabled by chip select CS6. The microprocessor can address the DUART's internal registers for read and write operations with data transferred between the devices on the eight bit A/D bus.

Dual receiver U25 and dual transmitter U24 are combined with the serial channels in the DUART to provide the two serial remote control interfaces as shown in figure 3. The serial interfaces can be configured for RS-232, RS-422 or MIL-188C standards. DIP switch S5 and jumper J19 are used to enable and configure the remote control interface. S5-1 enables and disables the interface (O = Disabled, C = Enabled). S5-2, S5-4, S5-5, S5-6, S5-7, and S5-8 are used to configure the interface. S5-3 is used with some optional software features but should be left in the closed position. For standard operations switch settings are summarized in table 6.

Table 6. Remote Control Interface Configuration Switch Settings

Interface Configuration	Chan 0 (MIL-188 or RS-232/RS-422		Chan 1 (AUX)		Both Channels A14J19
	S5-6	S5-7	S5-4	S5-5	
RS-232	O	C	O	C	2 TO 3
RS-422	O	O	O	O	1 TO 2
MIL-188	C	O	C	O	2 TO 3
MIL-188 (Balanced)	O	O	O	O	2 TO 3

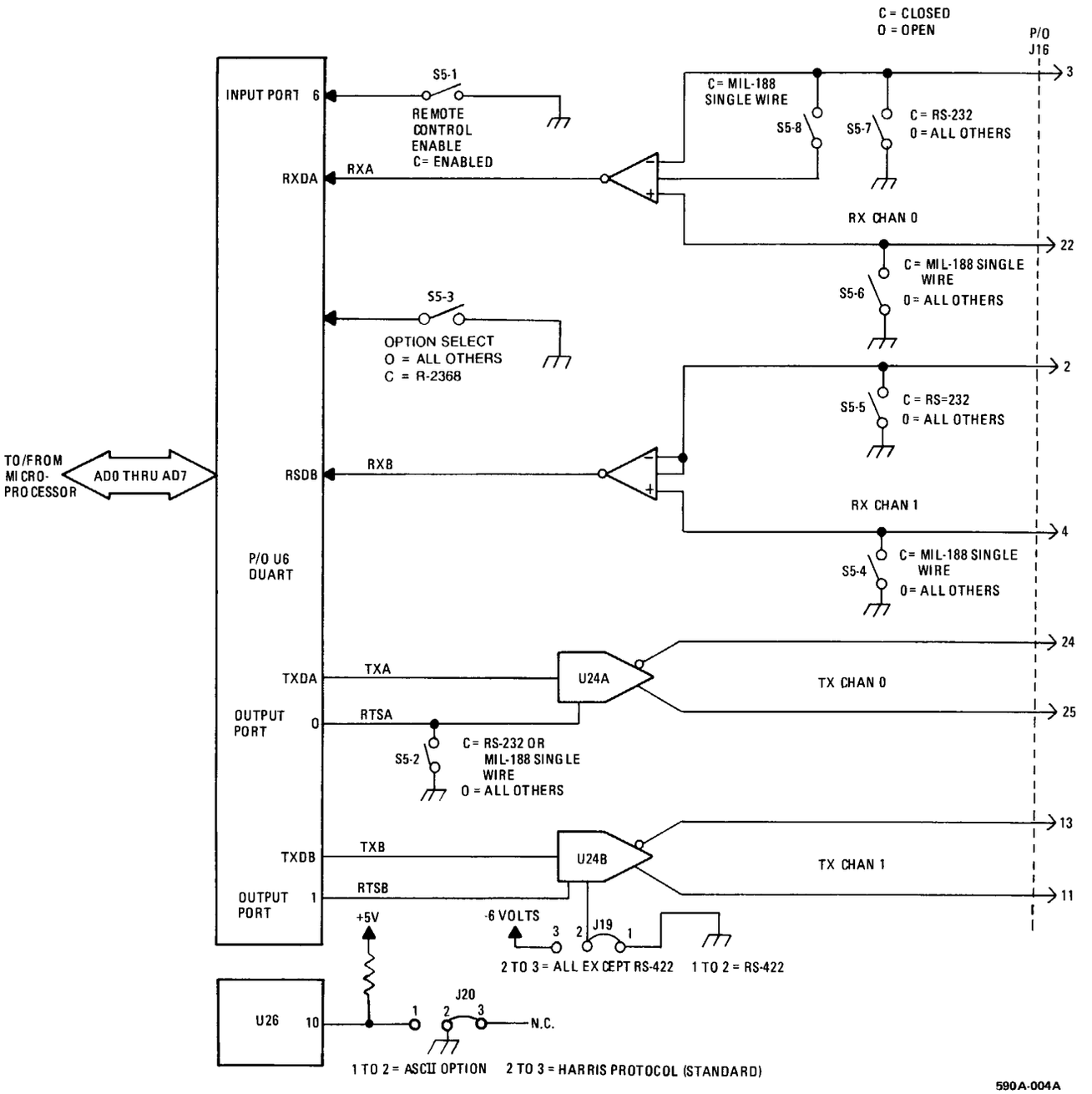


Figure 3. Remote Control Serial Interface

S5-2 and S5-8 are used to configure the serial interface when it is set for RS-422 or MIL-188 balanced operation. Both switches should be set in the open position for all except the following conditions:

- S5-2 - CLOSE for RS-232 or MIL-188 single wire.
- S5-8 - CLOSE only if the receiver is the last unit on a remote control bus.

The Output buffer for the channel 0 transmit port (RS-422 Out -, RS-422 Out +) normally operates as a tri-state device. The output of the buffer is put in a high impedance state whenever the receiver is not transmitting data on the bus. When the receiver is the only unit on the remote control bus (point-to-point operation) the high impedance state serves no purpose and may interfere with some transmissions. When S5-2 is closed, the output buffer behaves like a binary device.

S5-8 is used to terminate the Channel 0 input port (RS-422 In -, RS-422 In +). The port should be terminated only when the Receiver is the last unit on the remote control bus, that is, when it is physically located the farthest from the remote control unit. Close S5-8 to terminate the port.

The serial interface baud rate is selected by a 16 position rotary switch, S4. Most popular baud rates between 50 and 19200 are selectable. All selectable baud rates and their corresponding switch settings are listed in table 7.

Table 7. Serial Interface Baud Rate Switch Settings

S4 Position	Baud Rate
0	50
1	75
2	110
3	134.5
4	150
5	300
6	600
7	1200
8	1800
9	2000
A	2400
B	Not Used
C	4800
D	7200
E	9600
F	19200

For systems that use multiple remote-controlled receivers each receiver must have its own ID number. The ID number is selected as an eight-bit binary number by setting the switches of DIP switch S3 or by using jumper wires to configure the remote control cable connector. The connector configuration option is offered as a

maintenance aid in situations where receivers are replaced as units in the field. This eliminates the need to open up the receiver to set the ID. When the ID is set at the connector, all switches on S3 must be open. The ID is read by the microprocessor via parallel-to-serial converter U26. The converter receives its clock and load instruction via the output port of the DUART. The ID DATA is read directly by the microprocessor on the SID port. Table 8 lists the eight switches, the corresponding connector pins, and their weights.

Table 8. ID Number Switch Weights

Switch	Connector Pin	Weight
S3-1	J8-24	1
S3-2	J8-18	2
S3-3	J8-17	4
S3-4	J8-9	8
S3-5	J8-15	16
S3-6	J8-16	32
S3-7	J8-8	64
S3-8	J8-6	128

The bit is high when the corresponding switch is open or the corresponding connector pin is not tied to ground. A bit is low when the switch is closed or the corresponding pin is tied to ground. Decimal numbers between 0 and 255 are selectable. The decimal equivalent of the switch settings can be calculated by adding the weights assigned to each closed switch.

Both the units ID and the baud rate can be displayed on the front panel. To display them on the alphanumeric display, simply press and hold the ENTER pushbutton for about 10 seconds.

4. MAINTENANCE

4.1 Alignment

Control Assembly A14 requires no adjustment for proper operation.

4.2 Troubleshooting

Although most of the circuitry on this assembly is controlled directly or indirectly by the microprocessor, a practice of standard digital troubleshooting methods will isolate most faults to the component level. A logic HIGH is the level between 3 and 5 volts, and a proper logic LOW typically is between 0 and 1 volt. The circuit area involved in minor faults can typically be determined by BITE fault codes, or by using paragraph 3, Functional Description in this section. More general or major failures are best handled by proceeding in order through the checks outlines below.

4.2.1 CPU

If the microprocessor is running, it is capable of debugging several circuits on the A14 PWB by itself. However, it must first be determined if the 8085A is operating.

Table 9 lists the critical operational inputs for the CPU. If these signals are present, the CPU is running.

Table 9. Operational Inputs for CPU

Pin	Signal
U1-1, 2	Crystal inputs - 6 MHz
U1-36	Reset input - HIGH
U1-6	Trap input - LOW
U1-35	Ready - HIGH
U1-39	Hold - LOW

A14 PWB + 5 V supply should be between + 4.75 and + 5.1 volts. Table 10 lists the CPU outputs that should be present.

Table 10. Operational Outputs for CPU

Pin	Signal
U1-37	Clock out - 3 MHz square wave
U1-3	Reset out - LOW
U1-31	Write - active low pulses
U1-32	Read - active low pulses
U1-30	Address latch enable - active high pulses
U1-4	SOD - active low pulses at 1 millisecond intervals

When the CPU is running and executing the application software, its outputs will only be active a portion of each millisecond. The rest of the time it will be halted, waiting for a real time clock interrupt from U7.

4.2.2 Trap and Reset Circuits

The trap circuit is provided to restart the CPU in the software if the device loses synchronization due to high noise levels on its busses. One-shot U20 is retriggered before timeout from U1, pin 4, the SOD output. The software will generate a low active pulse every millisecond if it is executing properly and if it gets the real time clock interrupt. Low voltage on the + 5 supply to this board will cause a reset of the processor due to the reset circuit U23.

4.2.3 Device Selection

Address decoder U2 aids the access of devices through the data bus by outputting low active chip enable signals corresponding to the address on the high order bits of the CPU. During normal operation, the enables from U2 should be seen at the outputs of U2, as shown on the schematic diagram. The select on U9-6 should be active immediately following changes in the frequency entered through keyboard or tune knob. Active high selection pulses on A/D converter U10 are visible at least every 50 milliseconds in local receiver operation.

4.2.4 Memory Circuits

It can be very difficult to troubleshoot memory problems if the 8085A is not operating. If the CPU is running, it can find some problems itself. If the BITE routine indicates a PROM checksum fault, the fact that it is running indicates that the data bus buffers are operating and the PROMs are accessed. However, invalid data in these devices would require replacement of PROM U5.

If the BITE routine indicates a CMOS RAM fault, check that the enable pulse is getting to RAM U8 and check the voltage on U8-28. The chip enable for the RAM is generated at U2-15 and is gated through Q2. Check for its presence at both devices.

4.2.5 Real Time Clock

As mentioned before, the 1 kHz square wave output from 8155 (U7) is used to interrupt the CPU to synchronize and time many of the receivers' processes including the reset of the watchdog timer U20. If this digital clock is not seen at U1-7, it should be checked at U7-6. The 3 MHz input to U7-3 from U1-37 should also be present. Any improper real time clock operation can be traced to U1, U7, or their interconnection.

4.2.6 Serial I/O

Control Assembly A14 communicates with the display Control Assembly through its serial output circuit (U14, U16, U17, and U18). If this circuit fails, the display will light up but will never change from its power up lamp test.

When the Control Assembly is operating normally, it will attempt to update the complete display once every second. Every second there will be a burst of 64 bytes to the display Control PWB (two bytes of serial data sent every millisecond for a 32 millisecond total duration). There will be a strobe pulse (following every two bytes) to the display Control PWB from U14-5.

The BITE routine tests the serial output circuit by sending a test pattern to four PLLs and reading back a test bit from each. If it can set (high) and reset (low) all four test bits, it assumes that the serial output circuit on the A14 PWB is operating. If any one test bit cannot be set and reset, it assumes a problem with that PLL.

Signals of interest in the serial data transmission circuit are listed in table 11.

Table 11. Significant Serial Data Transmission Circuits

Component	Function
U16-3	Clock in - 3 MHz, square wave
U16-1, 13	Serial clock enable - High while data shifting out, 11 microseconds
U16-5, 11	1.5 MHz, square wave
U16-8, 9	750 kHz, square waves, opposite polarity
U17, 18-1	Serial port enable, narrow low active pulse
U17-9	Serial data out
U16-8	Serial clock
U14-5	Display control board strobe, 30 narrow high active pulses every second

4.3 Parallel I/O

Parallel I/O is centralized through the ports on U7 and U9. If there is a BITE or operational problem concerning the modules (listed above) that are controlled by the lines from these parallel circuits, but the module in question is not at fault, port failure may be indicated. Improper operation of front panel scanned keypad, A/D converter output U10-13, or tune knob may be caused by defective U9.

4.4 Analog I/O

4.4.1 Analog Inputs

If not in remote or test, the Control Assembly tries to update the RF gain every 50 milliseconds, using A/D converter U10. Starting the conversion consists of two writes to U10, narrow high-active pulses on U10-16. Ten microseconds later the end of conversion) line will go low. It will stay low for 100 microseconds and after it goes high again there will be one narrow high active pulse on U10-21. The above is true for all the other analog inputs sampled during the execution BITE. Signals of interest in the analog input circuit are listed in table 12.

Table 12. Significant Analog Input Circuits

Component	Function
U15-3	Clock in - 3 MHz, square wave
U15-5, 11	1.5 MHz
U15-9	Clock out - 750 kHz, square wave
U10-22	Clock in - 750 kHz, square wave
U10-16, 32	Start conversion. Two narrow high going pulses, every 50 milliseconds
U10-13	End of conversion. 85 microseconds low, every 50 milliseconds
U10-21	Output enable narrow high going pulse, every 50 milliseconds
U10-15, 18	Multiplexer out, comparator in

4.5 Remote Control Interface

The following procedure can be used to test some major functions of the remote control interface.

a. Ensure the VR2 and VR3 voltage regulator outputs are at acceptable levels. The output of VR2 should be -6 volts dc and can be measured at U24, pin 1. The output of VR3 should measure + 6 volts dc and checked at J19 pin 3. If either voltage is incorrect, replace the regulator or associated component as required.

b. Monitor pins 2 and 9 of U26 (Clock and Data respectively) with an oscilloscope.

c. Watch the oscilloscope and press and release the manual RESET switch. A short burst of pulses should be seen on the scope. The signal on the Data line will be altered by the positions of the unit identification switch settings. If the signals are observed as stated, it may be assumed that the DUART U6 and the parallel-to-serial converter U26 are functioning properly.

d. To test the serial data buffers U25 connect a data terminal or other appropriate digital signal source to the remote control interface connector. Configure the remote control interface and the terminal for the same type of interface (RS-232, RS-422, etc.)

e. Send data from the terminal to the remote control interface and observe the signal at the following points.

Device	Pin	Signal Description
U25	12, 14, or 12 and 14	Data from the terminal
U25	9	Output of data buffer, TTL level, inverted version of the input if input on pin 14.
U22	10	Inverted version of U25-9

f. To test the output buffer U24, monitor the outputs pins 14 and 15 with an oscilloscope. Turn the point-to-point select switch S52 on and off. Pin 14 will oscillate between a floating condition and + 6 volts as the switch is turned on and off. Pin 14 will oscillate between a floating condition and -6 volts. The high and low voltages assume that J19 is installed between pins 2 and 3.

4.6 Faults Detected Through BITE

The four fault areas on A14 detectable through BITE are listed in table 13.

Table 13. Fault Areas on Control Assembly A14

Fault	Failure
Fault 01:	PROM failure - The binary checksum calculated from the contents of programmed U5 do not match value programmed by the factory. Validity of firmware is doubtful, and device should be replaced.
Fault 02:	8155 RAM failure - Errors are found in the ability to store and retrieve data in the 256 byte RAM of U7. Replace U7.
Fault 03:	CMOS RAM failure - Errors are found in the ability to store and retrieve data in U8. Replace U8.
Fault 04:	Serial data failure - Faulty serial transmission is detected. Check U14 and U16 through U18.

5. PARTS LIST

Table 14 is a comprehensive parts list of all replaceable components in Control Assembly A14. When ordering parts from the factory, include a full description of the part. Use figure 4, Control Assembly A14 Component Location Diagram to identify parts.

6. SCHEMATIC DIAGRAM

Figure 5 is the Control Assembly A14 schematic diagram.

Table 14. Control Assembly A14 Parts List (PL 10215-2800, Rev. K/-2800-02, Rev. D)

Ref. Desig.	Part Number	Description
--	J65-0008-103	JMPR 2P FEM .10CNTR
--	J65-0008-103	JMPR 2P FEM .10CNTR
--	10215-8208	FIRMWARE KIT
BT1	B41-0009-004	BAT NICAD 3.6V -20/ + 70C
C1	M39014/02-1310	CAP .1UF 10% 100V CER-R
C2	M39014/02-1310	CAP .1UF 10% 100V CER-R
C3	M39014/02-1310	CAP .1UF 10% 100V CER-R
C4	M39014/02-1310	CAP .1UF 10% 100V CER-R
C5	M39014/02-1310	CAP .1UF 10% 100V CER-R
C6	M39014/02-1310	CAP .1UF 10% 100V CER-R
C7	M39014/02-1310	CAP .1UF 10% 100V CER-R
C8	C24-1025-476	CAP 47UF RDL 25V ELEC
C9	M39014/02-1310	CAP .1UF 10% 100V CER-R
C10	M39014/02-1310	CAP .1UF 10% 100V CER-R
C11	C26-0050-109	CAP 1.0UF 20% 50V TANT
C12	M39014/02-1310	CAP .1UF 10% 100V CER-R
C13	M39014/02-1298	CAP .01UF 10% 200V CER-R
C14	M39014/02-1310	CAP .1UF 10% 100V CER-R
C15	M39014/02-1310	CAP .1UF 10% 100V CER-R
C16	M39014/02-1310	CAP .1UF 10% 100V CER-R
C17	M39014/02-1310	CAP .1UF 10% 100V CER-R
C18	M39014/02-1310	CAP .1UF 10% 100V CER-R
C19	M39014/02-1310	CAP .1UF 10% 100V CER-R
C20	C26-0050-109	CAP 1.0UF 20% 50V TANT
C21	M39014/02-1310	CAP .1UF 10% 100V CER-R
C22	M39014/02-1310	CAP .1UF 10% 100V CER-R
C23	C12-0001-009	CAP 4.7PF 10% 25V CER
C24	C12-0001-009	CAP 4.7PF 10% 25V CER
C25	C18-0116-221	CAP 220UF 16V ELEC
C26	C26-0016-150	CAP 15UF 20% 16V TANT
C27	M39014/02-1310	CAP .1UF 10% 100V CER-R
C28	C26-0035-100	CAP 10UF 20% 35V TANT
C29	M39014/02-1310	CAP .1UF 10% 100V CER-R
C30	C18-0116-221	CAP 220UF 16V ELEC
C31	C18-0116-221	CAP 220UF 16V ELEC
C32	M39014/02-1310	CAP .1UF 10% 100V CER-R
C33	M39014/02-1310	CAP .1UF 10% 100V CER-R
C34	C18-0116-221	CAP 220UF 16V ELEC
C35	C18-0116-221	CAP 220UF 16V ELEC
C36	M39014/02-1310	CAP .1UF 10% 100V CER-R
C37	M39014/02-1310	CAP .1UF 10% 100V CER-R
C38	M39014/02-1310	CAP .1UF 10% 100V CER-R
C39	M39014/02-1310	CAP .1UF 10% 100V CER-R
C40	M39014/02-1310	CAP .1UF 10% 100V CER-R
C41	C11-0016-221	CAP 220PF 10% 63V CER
C42	C11-0016-221	CAP 220PF 10% 63V CER
C43	C11-0016-221	CAP 220PF 10% 63V CER
C44	C11-0016-221	CAP 220PF 10% 63V CER
C45	C11-0016-471	CAP 470PF 10% 63V CER

Table 14. Control Assembly A14 Parts List (PL 10215-2800, Rev. K/-2800-02, Rev. D) (Cont.)

Ref. Desig.	Part Number	Description
C46	C11-0016-471	CAP 470PF 10% 63V CER
C47	M39014/02-1310	CAP .1UF 10% 100V CER-R
C48	M39014/02-1310	CAP .1UF 10% 100V CER-R
C49	M39014/02-1310	CAP .1UF 10% 100V CER-R
CR1	1N6263	DIODE .40W 60V HOT CARR
CR2	1N6263	DIODE .40W 60V HOT CARR
CR3	1N4454	DIODE 200MA 75V SW
CR4	1N4454	DIODE 200MA 75V SW
CR5	1N4454	DIODE 200MA 75V SW
CR6	I14-0003-005	IC V REF 2.5V 2% LM236
J1	J46-0022-004	HDR 4 PIN 0.100" SR LKG
J2	J46-0013-014	HDR 14 PIN 0.100 DR SHRD
J3	J46-0022-010	HDR 10 PIN 0.100" SR LKG
J4	J46-0022-010	HDR 10 PIN 0.100" SR LKG
J5	J46-0013-014	HDR 14 PIN 0.100 DR SHRD
J6	J46-0034-008	HDR 8 PIN 0.100" RT ANG
J7	J46-0031-010	HDR 10 PIN 0.100" RT ANG
J8	J46-0034-008	HDR 8 PIN 0.100" RT ANG
J9	J46-0034-008	HDR 8 PIN 0.100" RT ANG
J10	J46-0034-008	HDR 8 PIN 0.100" RT ANG
J11	J46-0031-020	HDR 20 PIN 0.100" RT ANG
J12	J46-0034-008	HDR 8 PIN 0.100" RT ANG
J13	J46-0031-016	HDR 16 PIN 0.100" RT ANG
J14	J46-0034-008	HDR 8 PIN 0.100" RT ANG
J15	J46-0013-040	HDR 40 PIN 0.100" DR SHRD
J16	J46-0013-026	HDR 26 PIN 0.100" DR SHRD
J17	J46-0047-002	HDR 2 POSITION
J18	J46-0022-008	HDR 8 PIN 0.100" SR LKG
J19	J46-0047-003	HEADER 3 POS
J20	J46-0047-003	HEADER 3 POS
JMP1	MP-1142	RES ZERO OHM (CKT JMPR)
JMP2	MP-1142	RES ZERO OHM (CKT JMPR)
JMP3	MP-1142	RES ZERO OHM (CKT JMPR)
JMP4	MP-1142	RES ZERO OHM (CKT JMPR)
JMP5	MP-1142	RES ZERO OHM (CKT JMPR)
L1	L06-0002-471	IND 470.0UH 20% AXL SHLD
L2	L-0644	COIL 220UH 10% FXD RF
L3	L06-0002-471	IND 470.0UH 20% AXL SHLD
L4	L-0644	COIL 220UH 10% FXD RF
L5	L06-0002-181	IND 180.0UH 20% AXL SHLD
L6	L06-0002-471	IND 470.0UH 20% AXL SHLD
Q1	2N2222A	XSTR SS/GP NPN TO-18
Q2	2N2222A	XSTR SS/GP NPN TO-18
Q3	2N2907A	XSTR SS/GP PNP TO-18
Q4	2N2222A	XSTR SS/GP NPN TO-18
R1	R65-0003-473	RES 47K 5% 1/4W CAR FILM
R2	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R3	RN55D1002F	RES 10.0K 1% 1/8W MET FLM
R4	RN55D1001F	RES 1000 1% 1/8W MET FLM

Table 14. Control Assembly A14 Parts List (PL 10215-2800, Rev. K/-2800-02, Rev. D) (Cont.)

Ref. Desig.	Part Number	Description
R5	R50-0010-103	RES 10K 2% 10SIP 9RES
R6	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R7	R65-0003-184	RES 180K 5% 1/4W CAR FILM
R8	R65-0003-184	RES 180K 5% 1/4W CAR FILM
R9	R65-0003-114	RES 110K 5% 1/4W CAR FILM
R10	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R11	R65-0003-222	RES 2.2K 5% 1/4W CAR FILM
R12	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R13	R65-0003-104	RES 100K 5% 1/4W CAR FILM
R14	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R15	R65-0003-272	RES 2.7K 5% 1/4W CAR FILM
R16	R65-0003-105	RES 1.0M 5% 1/4W CAR FILM
R17	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R18	R65-0003-223	RES 22K 5% 1/4W CAR FILM
R19	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R20	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R21	R65-0003-223	RES 22K 5% 1/4W CAR FILM
R22	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R23	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R24	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R25	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R26	R50-0010-103	RES 10K 2% 10SIP 9RES
R27	R50-0010-103	RES 10K 2% 10SIP 9RES
R28	R53-0001-001	RES 50K 2% 16DIP 16RES
R29	R65-0003-393	RES 39K 5% 1/4W CAR FILM
R30	R65-0003-363	RES 36K 5% 1/4W CAR FILM
R31	R65-0003-512	RES 5.1K 5% 1/4W CAR FILM
R32	R65-0003-512	RES 5.1K 5% 1/4W CAR FILM
R33	R65-0003-512	RES 5.1K 5% 1/4W CAR FILM
R34	R65-0003-363	RES 36K 5% 1/4W CAR FILM
R35	R65-0003-104	RES 100K 5% 1/4W CAR FILM
R36	R50-0010-103	RES 10K 2% 10SIP 9RES
R37	R50-0010-103	RES 10K 2% 10SIP 9RES
R38	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R39	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R40	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R41	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R42	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R43	R65-0003-101	RES 100 5% 1/4W CAR FILM
R44	RN55D1002F	RES 10.0K 1% 1/8W MET FLM
R45	RN55D8251F	RES 8250 1% 1/8W MET FLM
R46	RN55D4990F	RES 499 1% 1/8W MET FLM
R47	RN55D1000F	RES 100 1% 1/8W MET FLM
R48	RN55D1000F	RES 100 1% 1/8W MET FLM
R49	RN55D4990F	RES 499 1% 1/8W MET FLM
R50	R50-0010-103	RES 10K 2% 10SIP 9RES
R51	R65-0003-222	RES 2.2K 5% 1/4W CAR FILM
R52	R65-0003-473	RES 47K 5% 1/4W CAR FILM
R53	R65-0003-103	RES 10K 5% 1/4W CAR FILM

Table 14. Control Assembly A14 Parts List (PL 10215-2800, Rev. K/-2800-02, Rev. D) (Cont.)

Ref. Desig.	Part Number	Description
R54	R65-0003-101	RES 100 5% 1/4W CAR FILM
R55	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R56	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R57	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R58	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R59	R65-0003-182	RES 1.8K 5% 1/4W CAR FILM
S1	10075-1029	SW DPST 50MA 50V PCMNT
S2	S50-0001-008	SW SPST 8SEC .1A SLD DIP
S3	S50-0001-008	SW SPST 8SEC .1A SLD DIP
S4	S27-0012-002	SW 1P 16POS BCD ROT DIP
S5	S50-0001-008	SW SPST 8SEC .1A SLD DIP
U1	I27-0006-002	IC MIPRCS 8-BIT 8085
U2	10215-8204	KIT SOFTWARE
U3	I05-0000-373	IC 74LS373 PLASTIC TTL
U4	I05-0000-245	IC 74LS245 PLASTIC TTL
U6	I61-0004-001	IC DUART
U7	I26-0003-001	IC 256X8 SRAM 8155-2
U8	I26-0021-005	IC,32KX8 S-RAM
U9	I59-0008-001	IC 8255A PROG INTERFACE
U10	I40-0010-001	IC ADC0817 PLASTIC CMOS
U11	I01-0000-156	IC 4094B PLASTIC CMOS
U12	I05-0000-004	IC 74LS04 PLASTIC TTL
U13	I30-0018-000	IC OP AMP DUAL 1458
U14	I01-0000-202	IC 4514B PLASTIC CMOS
U15	I05-0000-074	IC 74LS74A PLASTIC TTL
U16	I05-0000-074	IC 74LS74A PLASTIC TTL
U17	I05-0000-165	IC 74LS165 PLASTIC TTL
U18	I05-0000-165	IC 74LS165 PLASTIC TTL
U19	I05-0000-004	IC 74LS04 PLASTIC TTL
U20	I05-0000-122	IC 74LS122 PLASTIC TTL
U21	I05-0000-244	IC 74LS244 PLASTIC TTL
U22	I05-0000-002	IC 74LS02 PLASTIC TTL
U23	I20-0008-000	IC LM239 COMPARATOR P/C
U24	I16-0050-233	IC 3692 LINE DRVR PLA
U25	I17-0010-004	IC,RECEIVER
U26	I05-0000-165	IC 74LS165 PLASTIC TTL
VR1	I11-0008-005	IC VR 340 + 5V 0.1A 2%
VR2	I12-0006-005	IC VR 78L05A + 5V .10A 4%
VR3	I12-0010-005	IC VR 79L05A -5V .10A 4%
XU3	J77-0008-006	SKT IC MACH 28 PIN
Y1	Y15-0004-060	XTAL 6 MHZ
Y2	Y15-0004-937	XTAL 3.6864 MHZ

NOTES:
1. COMPLETED PWB ASSEMBLY SHALL CONFORM TO QC-3000

2. MARK ASSEMBLY NUMBER SUFFIX -01, -02, OR -03 TO ASSEMBLY PART NUMBER AS REQUIRED.

3. FOR KEYING PURPOSES, THE FOLLOWING PINS ARE TO BE REMOVED BY CUTTING THEM FLUSH WITH THE CONNECTOR PRIOR TO INSTALLATION.

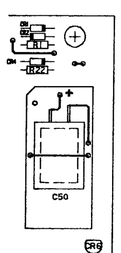
CONNECTOR	PIN # TO BE CUT
J1	2
J2	4
J3	6
J4	8
J6	3
J8	5
J9	6
J10	3
J12	3
J14	3
J18	2

4. JMP1 - JMP4 CAN BE MOVED TO ACCOMMODATE DIFFERENT SIZE ROM (U5) AND RAM (U8). SEE SCHEMATIC.

5. INSTALL ITEM 4 ON J19:
   POS. 1 & 2 SELECTS RS-422
   POS. 2 & 3 SELECTS RS-232 OR MIL 188

6. INSTALL ITEM 4 ON J20:
   POS. 2 & 3 FOR STANDARD REMOTE INTERFACE:
   POS. 1 & 2 FOR OPTIONAL REMOTE INTERFACE.

7. ON THE 10215-2800-03 ASSY,
   BT1 IS NOT INSTALLED.
   LITHIUM BATTERY IS REPLACED BY C50 AS SHOWN IN DETAIL "A".
   R2 IS NOT INSTALLED.
   ITEM 15 (WIRE) IS INSTALLED IN PLACE OF J17.
   ITEM 17 (WIRE) IS INSTALLED AS SHOWN IN DETAIL "A".



DETAIL "A"

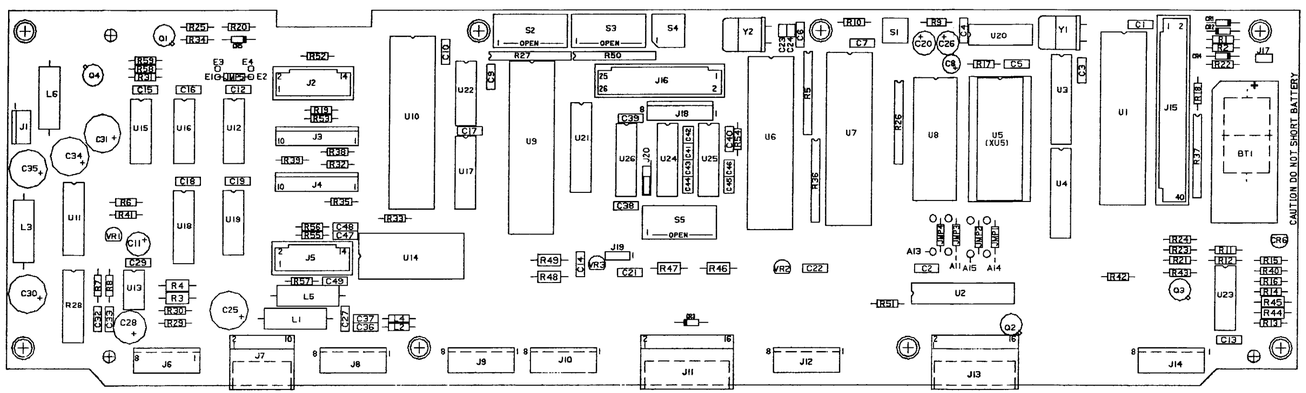
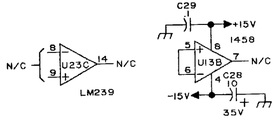


Figure 4. Control Assembly A14 Component Location Diagram (10215-2800, Rev. G)

NOTE: UNLESS OTHERWISE SPECIFIED:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR A COMPLETE DESIGNATION, PREFIX WITH UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.
2. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, ±5%.
3. ALL CAPACITOR VALUES ARE IN MICROFARADS.
4. VENDOR PART NO. CALLOUTS ARE FOR REFERENCE ONLY. COMPONENTS ARE SUPPLIED PER PART NO. IN PARTS LIST.
5. NI-CAD BATTERY SITE IS SHOWN DASHED. IF THE NI-CAD BATTERY IS USED, CONNECT J17.
6. INSTALL ITEM 4 ON J20:
   POSITION 2-3 FOR STANDARD REMOTE INTERFACE.
   POSITION 1-2 FOR OPTIONAL REMOTE INTERFACE.
7. THE CAPACITOR MEMORY BACKUP CIRCUITRY IS USED ON 10215-2800-03 ASSEMBLY AS SHOWN IN DETAIL A.

UNUSED GATES



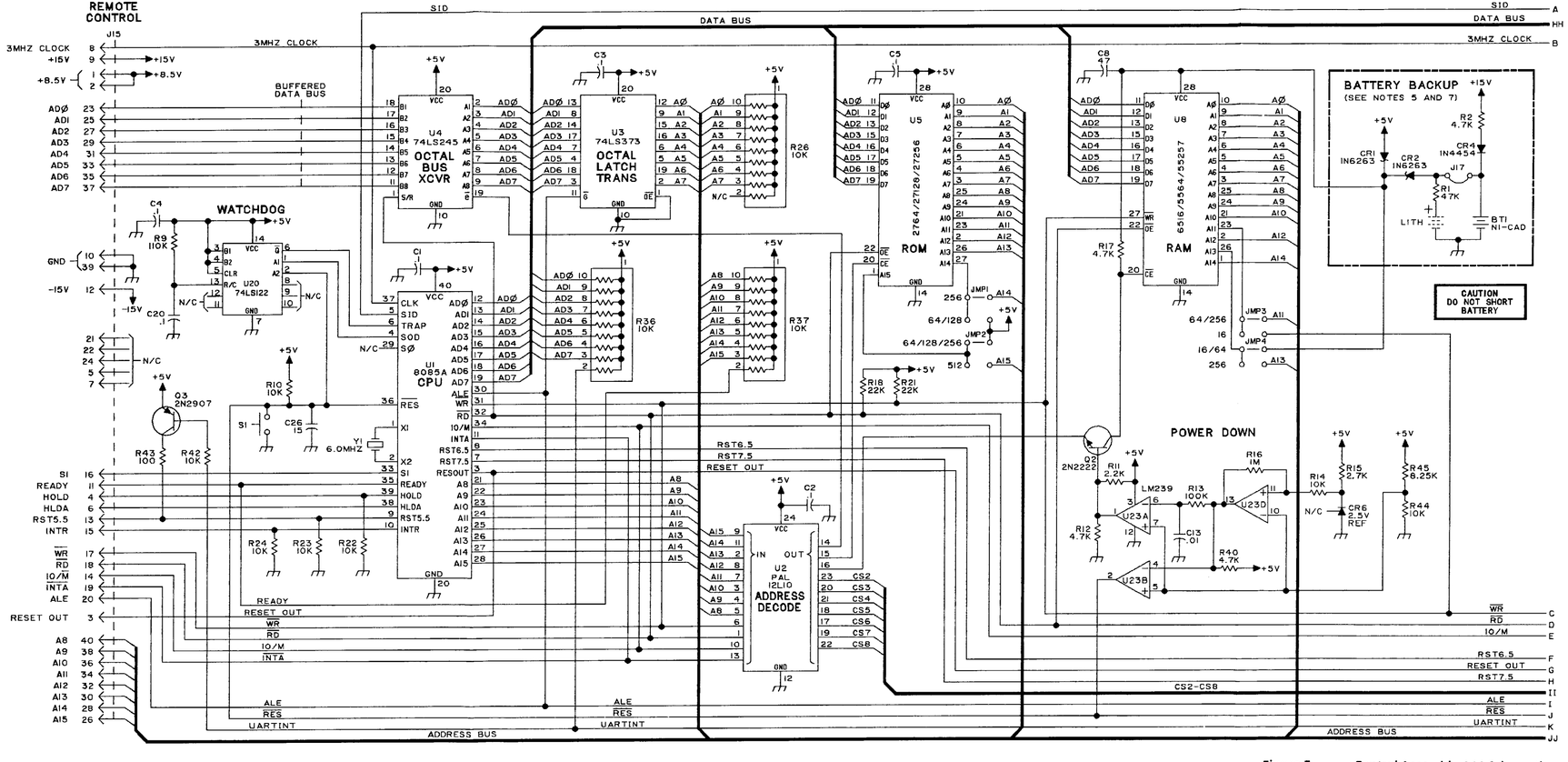


Figure 5. Control Assembly A14 Schematic Diagram (10215-2801, Rev. J) (Sheet 1 of 5)

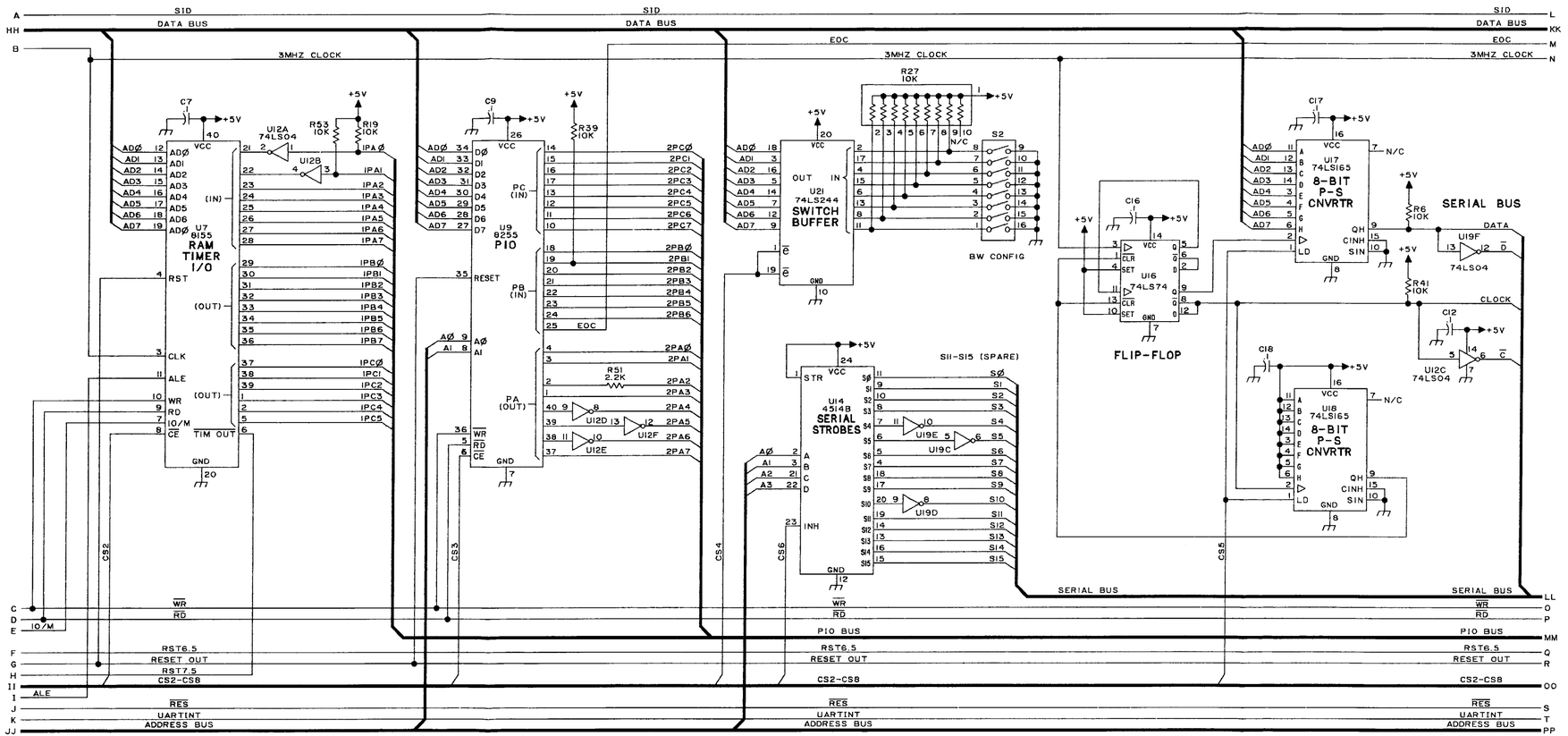


Figure 5. Control Assembly A14 Schematic Diagram (10215-2801, Rev. J) (Sheet 2 of 5)

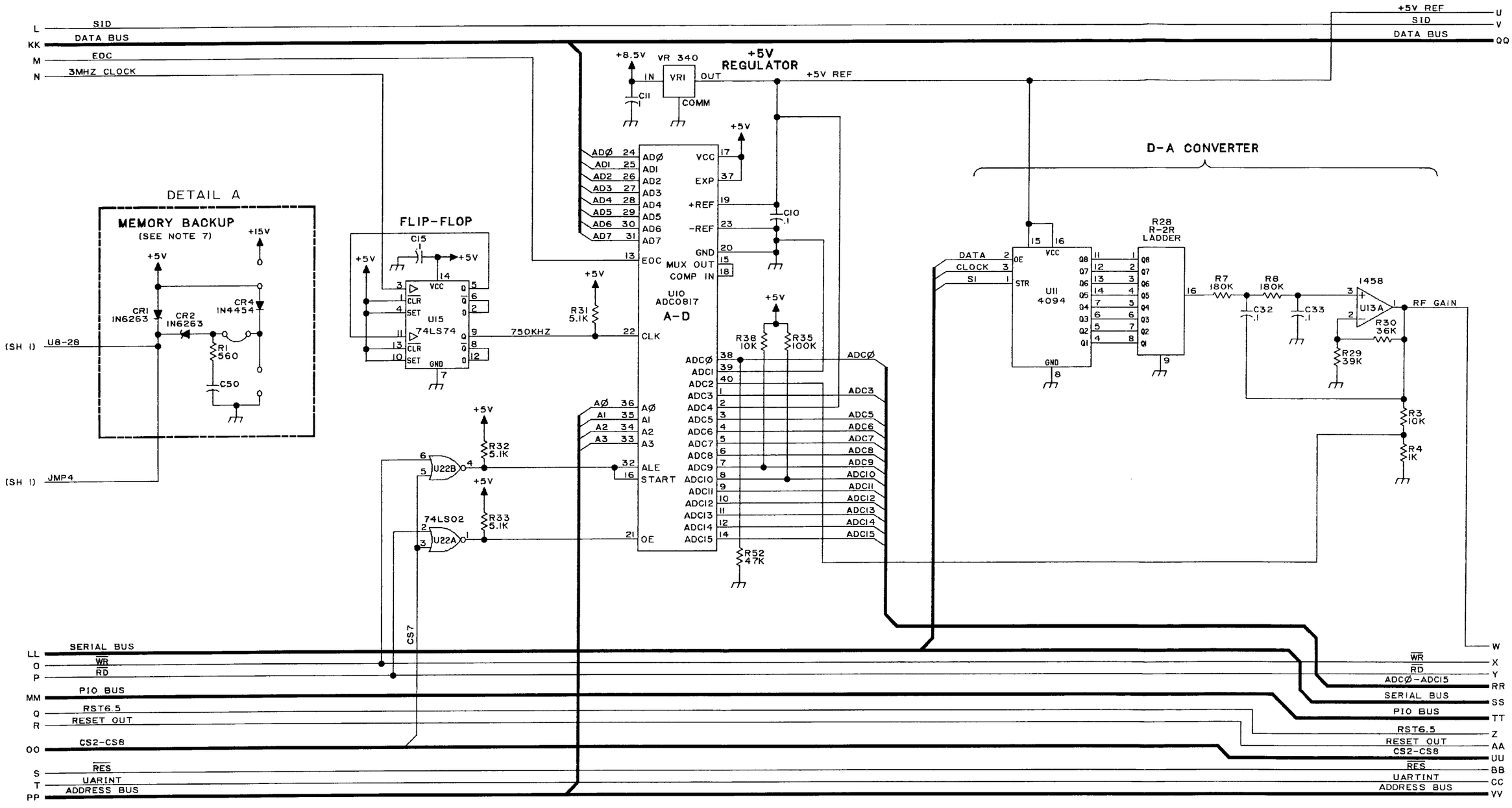


Figure 5. Control Assembly A14 Schematic Diagram (10215-2801, Rev. J) (Sheet 3 of 5)

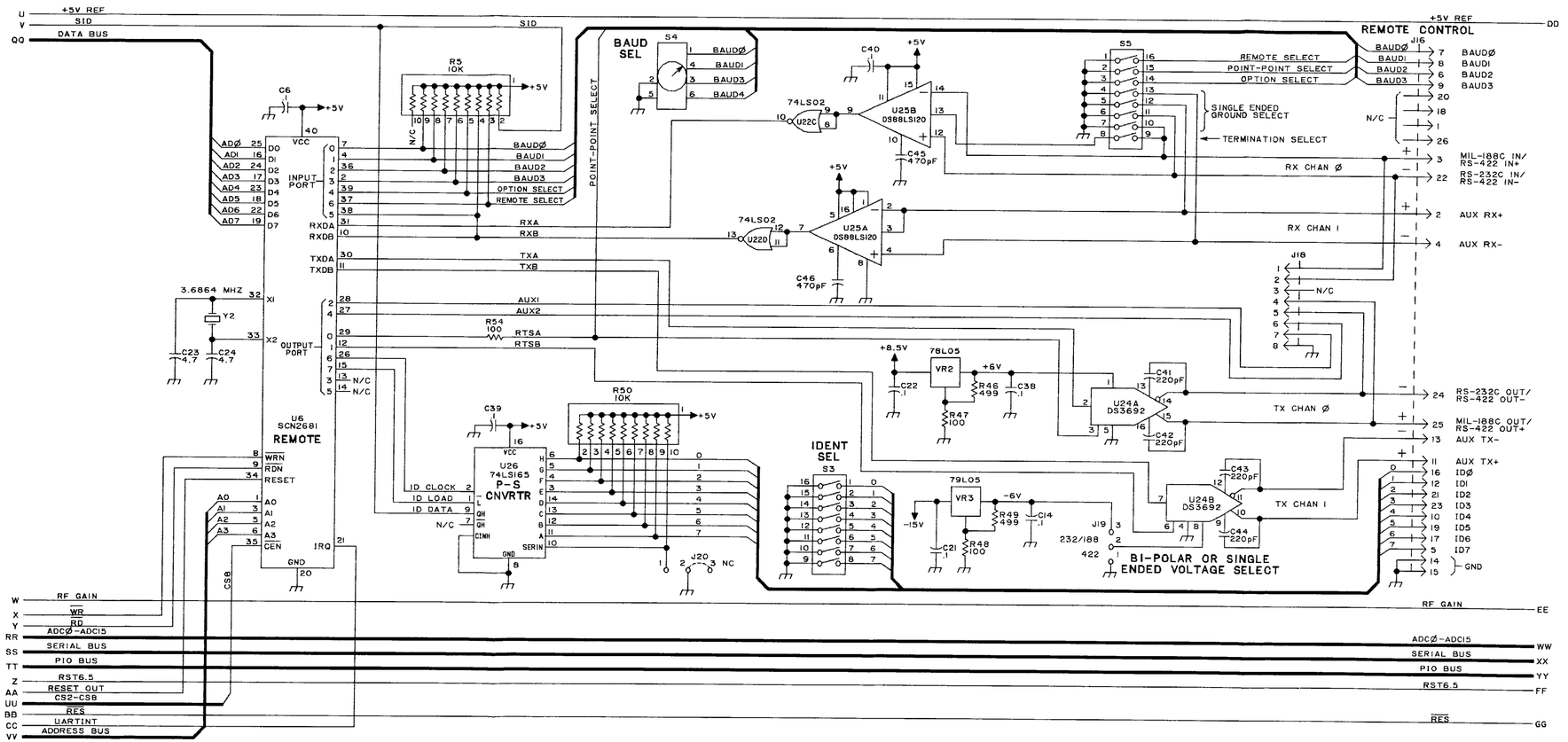


Figure 5. Control Assembly A14 Schematic Diagram (10215-2801, Rev. J) (Sheet 4 of 5)

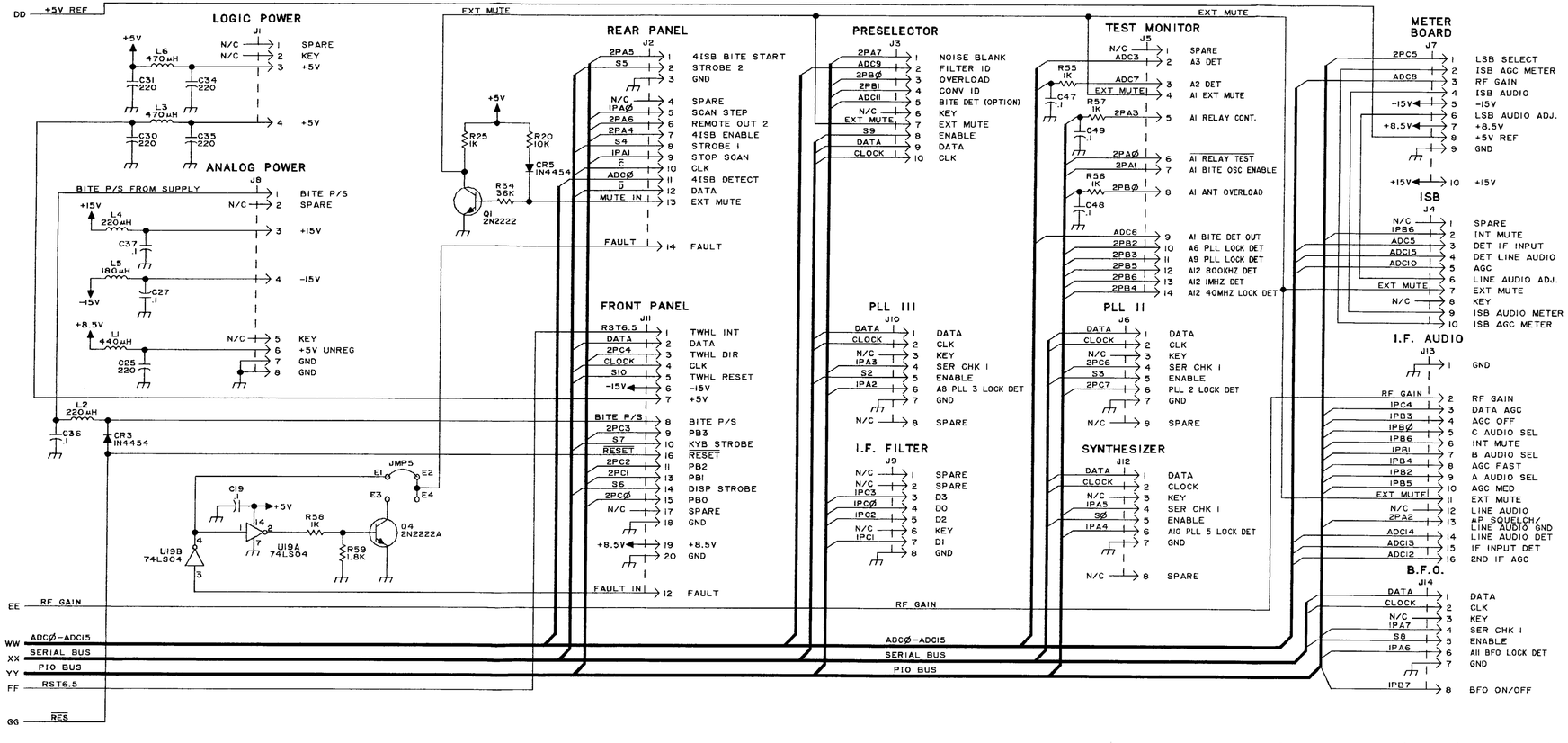


Figure 5. Control Assembly A14 Schematic Diagram (10215-2801, Rev. J) (Sheet 5 of 5)

A15
POWER SUPPLY ASSEMBLY

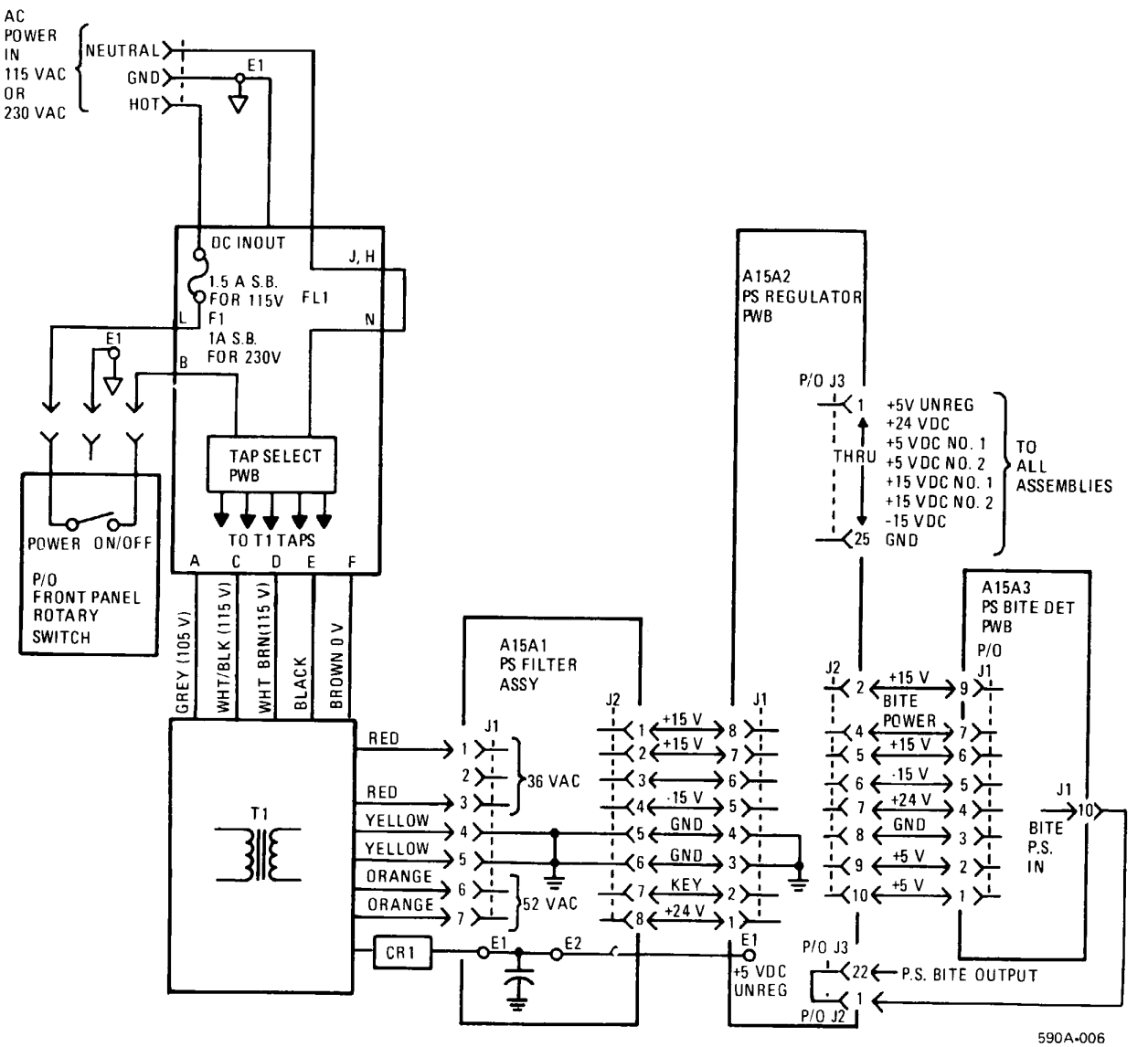


TABLE OF CONTENTS

Paragraph		Page
1.	General Description	1
2.	Interface Connections	1
3.	A15 Parts Lists, Component Locations, and Schematic Diagram	4
4.	Power Supply Filter Assembly A15A1 Circuit Description	11
5.	Power Supply Heatsink Assembly A15A2 Circuit Description	14
6.	Power Supply BITE Detector Assembly A15A3 Circuit Description	21
7.	A15 Assembly Removal	27

LIST OF FIGURES

Figure		Page
1	Power Supply Assembly A15 Location	2
2	Power Supply Assembly A15 Functional Block Diagram	5
3	Power Supply Assembly A15 Component Location Diagram (10073-3000)	7
4	Power Supply Assembly A15 Schematic Diagram (10073-3001)	9
5	Power Supply Filter A15A1 Component Location Diagram (10073-3100)	12
6	Power Supply Filter Assembly A15A1 Schematic Diagram (10073-3101)	13
7	Power Supply Heatsink Assembly A15A2 Component Location Diagram (10073-3250)	15
8	Power Supply Regulator Assembly A15A2A1 Component Location Diagram (10073-3200)	17
9	Power Supply Heatsink Assembly A15A2 and Power Supply Regulator Assembly A15A2A1 Schematic Diagram (10073-3201, Rev. D)	19
10	Power Supply BITE Assembly A15A3 Component Location Diagram (10073-3300)	23
11	Power Supply BITE Assembly A15A3 Schematic Diagram (10073-3301)	25

LIST OF TABLES

Table		Page
1	Power Supply Assembly A15 Interface Connectors	2
2	Power Supply Assembly A15 Parts List (10073-3000)	4
3	Power Supply Filter Board Assembly A15A1 Parts List (10073-3100)	11
4	A15A2 Voltage Regulator Identification	14
5	Power Supply Heatsink Assembly A15A2 Parts List (10073-3250)	14
6	Power Supply Regulator Assembly A15A2A1 Parts List (10073-3200)	16
7	A15A3 BITE Detector Trip Limits	21
8	Power Supply BITE Assembly A15A3 Parts List (10073-3300)	22

A15 POWER SUPPLY ASSEMBLY

1. GENERAL DESCRIPTION

WARNING

Potentially hazardous high voltages are present inside the A15 assembly whenever the Receiver is connected to an ac line source. Do not attempt any repair to this assembly unless the line cord is disconnected. Do not operate the Receiver without the protective cover properly installed over the assembly.

Power Supply Assembly A15 converts either 100, 120, 220, or 240 Vac input line voltages into the dc voltages required to operate all assemblies.

Input voltage selection for the A15 assembly is made by positioning a plug-in PWB that is part of A15 Line Filter FL1. It is located next to the rear panel ac power fuse.

All power supply components and assemblies are housed in a single, metal housing with cover. Major components/assemblies inside this housing are listed below:

- Input Line Filter FL1
- Power Transformer T1
- Filter PWB A15A1
- Heatsink Assembly A15A2 with Regulator PWB A15A2A1
- Power Supply BITE Detector PWB A15A3

The position of these assemblies is shown in figure 1.

FL1 provides EMI protection and A15 input voltage selection. T1 converts the ac line voltage into the required lower ac voltage levels needed to run the regulators. Filter PWB A15A1 converts the T1 ac outputs into unregulated dc voltage levels. The A15A2 assembly contains the three terminal voltage regulators which convert the unregulated dc levels into regulated dc output voltages. The voltage regulators VR1 through VR6 are mounted on Heatsink Assembly A15A2, while the remaining circuitry is on Regulator PWB Assembly A15A2A1. A15A2A1 delivers + 5 Vdc, + 15 Vdc, -15 Vdc, and + 24 Vdc to other assemblies in the Receiver.

Power Supply BITE PWB A15A3 monitors the output of Regulator PWB A15A2A1, and signals the Control PWB A14 microprocessor if these levels exceed certain prescribed limits. This in turn would cause a front panel fault indicator to light. All major components and assemblies in the A15 assembly are interconnected via ribbon cable with plug-in connectors.

2. INTERFACE CONNECTIONS

Table 1 details the various input/output connections and other relevant data.

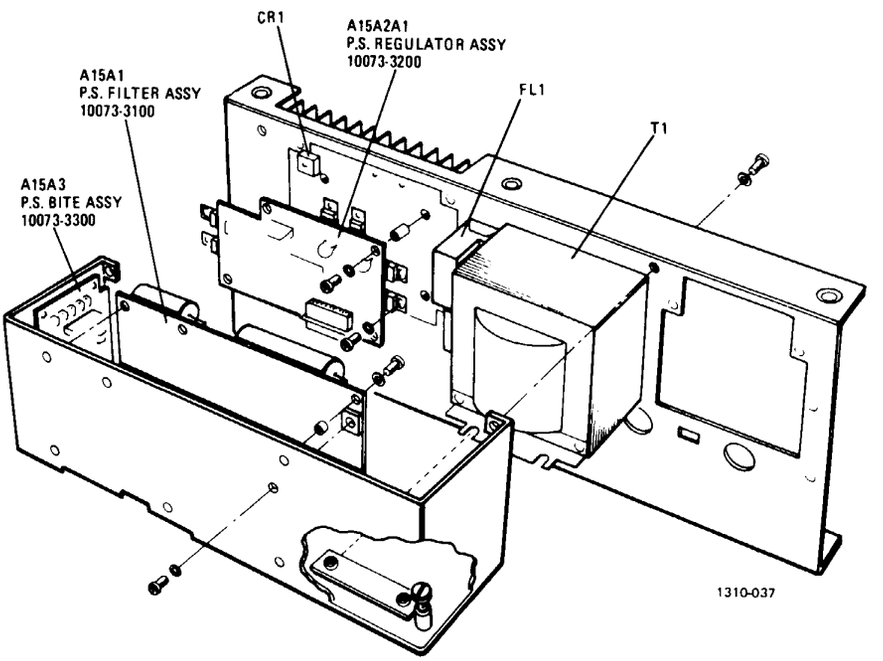


Figure 1. Power Supply Assembly A15 Location

Table 1. Power Supply Assembly A15 Interface Connectors

Connector	Function	Characteristics
A15A2A1J3-1	+ 15 V Regulated No. 1	
A15A2A1J3-2	+ 24 V Regulated	
A15A2A1J3-3	Gnd	Ground
A15A2A1J3-4	+ 5 V Unregulated	
A15A2A1J3-5, 6	+ 15 V Regulated No. 1	

Table 1. Power Supply Assembly A15 Interface Connectors (Cont.)

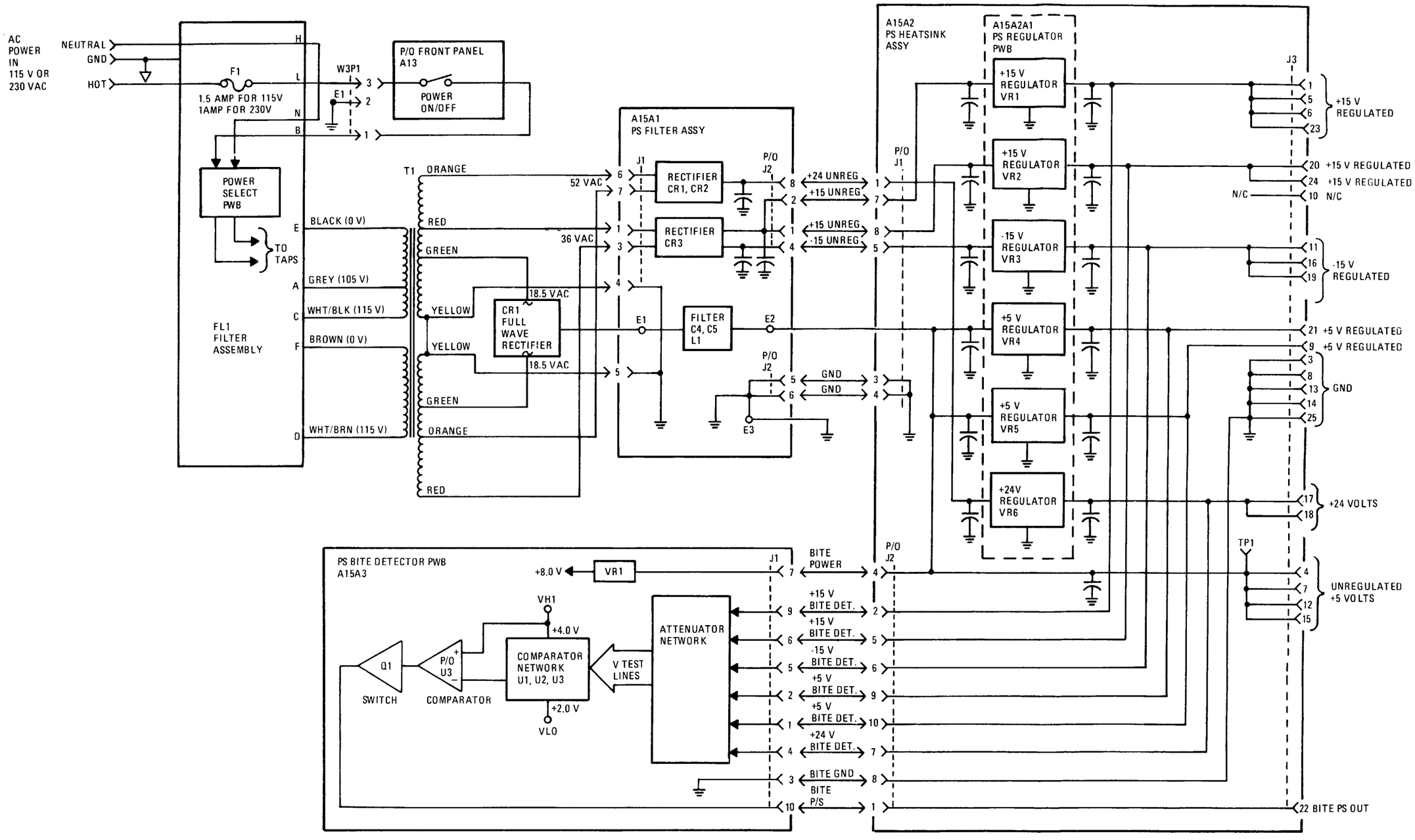
Connector	Function	Characteristics
A15A2A1J3-7	+ 5 V Unregulated	
A15A2A1J3-8	Gnd	Ground
A15A2A1J3-9	+ 5 V Regulated No. 2	
A15A2A1J3-10	No Connection	
A15A2A1J3-11	-15 V Regulated	
A15A2A1J3-12	+ 5 V Unregulated	
A15A2A1J3-13, 14	Gnd	Ground
A15A2A1J3-15	+ 5 V Unregulated	
A15A2A1J3-16	= 15 V Regulated	
A15A2A1J3-17, 18	+ 24 V Regulated	
A15A2A1J3-19	-15 V Regulated	
A15A2A1J3-20	+ 15 V Regulated No. 2	
A15A2A1J3-21	+ 5 V Regulated No. 1	
A15A2A1J3-22	BITE Power Supply	0 Vdc = Failure
A15A2A1J3-23	+ 15 V Regulated No. 1	
A15A2A1J3-24	+ 15 V Regulated No. 2	
A15A2A1J3-25	Gnd	Ground
W3P1-1	Switched Ac Hot	To Front Panel ON/OFF Switch
W3P1-2	Gnd	To Front Panel ON/OFF Switch
W3P1-3	Ac Hot	To Front Panel ON/OFF Switch
W5P1-2	Ac Neutral	To fan

3. A15 PARTS LISTS, COMPONENT LOCATIONS, AND SCHEMATIC DIAGRAM

Table 2 is the A15 assembly parts list. Figure 2 is the functional block diagram for Power Supply Assembly A15, figure 3 is the A15 assembly component location diagram, and figure 4 is the A15 assembly schematic diagram.

Table 2. Power Supply Assembly A15 Parts List (10073-3000, Rev. N)

Ref. Desig.	Part Number	Description
A1	10073-3100	PWB ASSY, FILTER
A2	10073-3250	HEATSINK ASSY
A3	10073-3300	PWB ASSY, BITE
E1	MS77068-1	LUG SOLDER #4
F1	F03-0002-022	FUSE 1-1/2A SB 125V 3AG
FL1	6919-1400	LINE FILTER
T1	10073-3052	TRANSFORMER,POWER
W1	10073-7060	RIBBON CABLE, 10 COND
W2	10073-7059	RIBBON CABLE, 8 COND
W3	10073-7250	CABLE ASSY,3 COND



590A-007

Figure 2. **Power Supply Assembly A15 Functional Block Diagram**

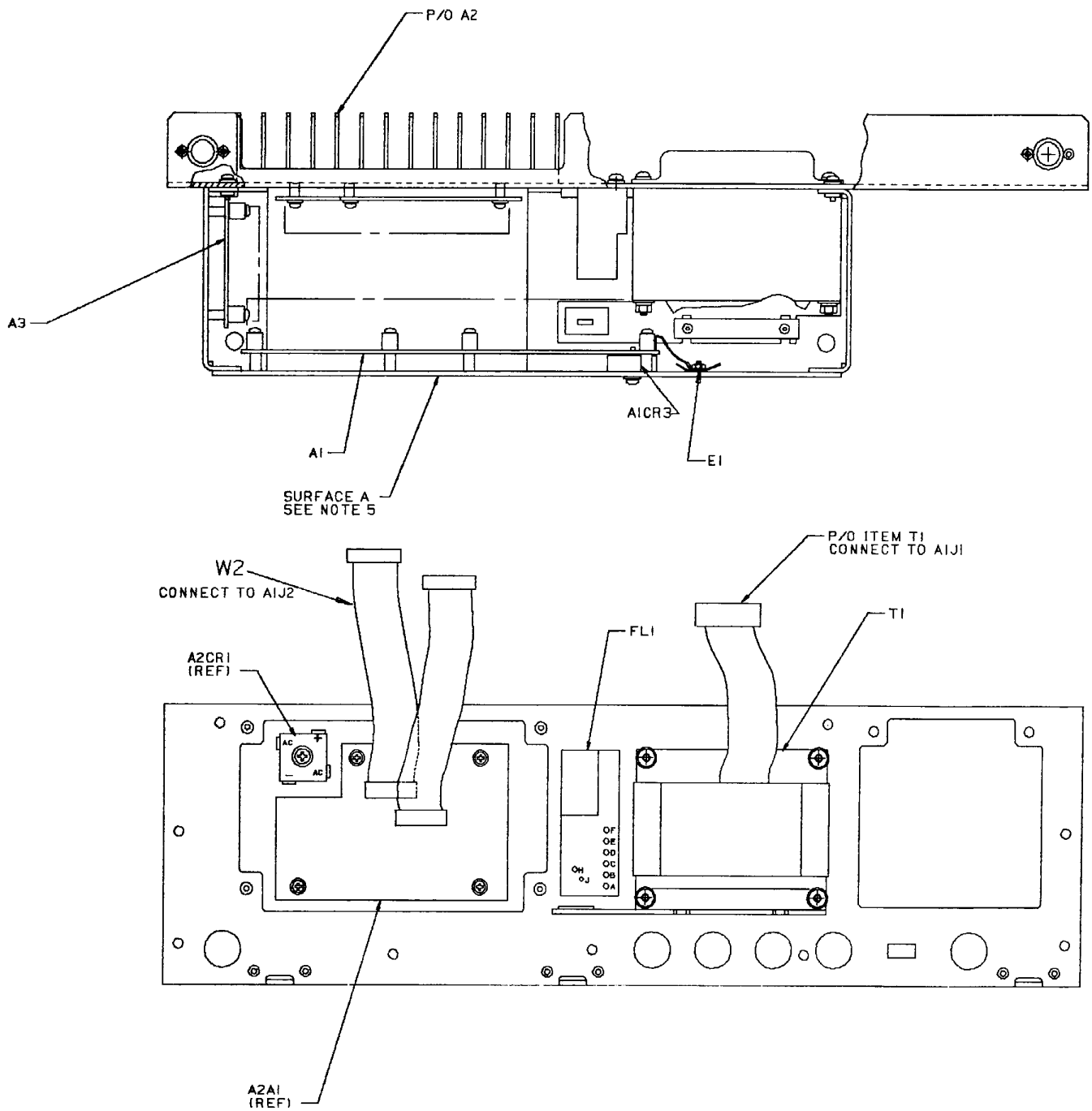


Figure 3. Power Supply Assembly A15 Component Location Diagram (10073-3000, Rev. J)

NOTE: UNLESS OTHERWISE SPECIFIED:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR A COMPLETE DESIGNATION, PREFIX WITH UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.

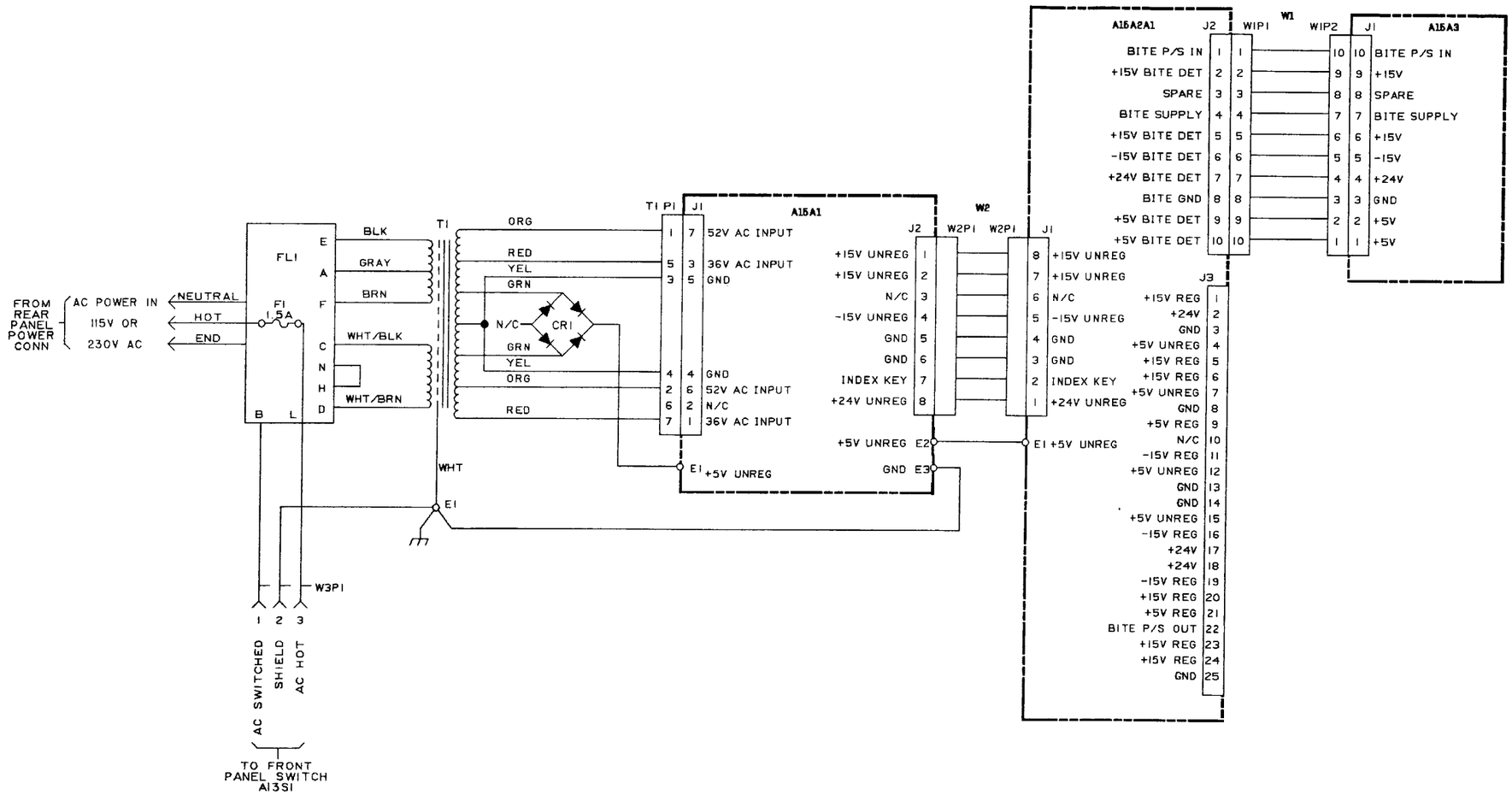


Figure 4. **Power Supply Assembly A15 Schematic Diagram (10073-3001 Rev. E)**

4. POWER SUPPLY FILTER ASSEMBLY A15A1 CIRCUIT DESCRIPTION

The A15A1 assembly contains voltage rectifiers and the large filter capacitors required to filter the input voltages from T1. The 52 Vac at J1-6 and J1-7 is full-wave rectified by CR1 and CR2 and filtered by C1 to produce an unregulated + 24 volts at J2-8.

The 36 Vac at J1-1 and J1-3 is full-wave rectified by CR3 and filtered by C2 and C3 to produce an unregulated + 15 volts at J2-1 and J2-2, and an unregulated -15 volts at J2-4. The unregulated 5 volts at E1 are heavily filtered by filter network C4-L1-C5 and made available at E2.

Table 3 is the A15A1 assembly parts list, figure 5 is the A15A1 component location diagram, and figure 6 is the A15A1 schematic diagram.

Table 3. Power Supply Filter Board Assembly A15A1 Parts List (10073-3100)

Ref. Desig.	Part Number	Description
C1	C17-0050-282	CAP,2800UF,50V
C2	C17-0035-562	CAPACITOR, 5600 UF
C3	C17-0035-212	CAP,FXD,ELCTLT,2100UF
C15	C17-0035-123	CAPACITOR 12000 UF
C19	C17-0035-123	CAPACITOR 12000 UF
CR1	D22-0006-001	DIODE
CR2	D22-0006-001	DIODE
CR3	D22-5011-200	DIODE,BRIDGE
E3	MP-0372	FAST-ON,.125
J1	J42-0004-007	CONNECTOR,7 PIN
J2	J46-0032-008	CONNECTOR,8 PIN
L1	10073-3051	INDUCTOR,1MH 4 AMP

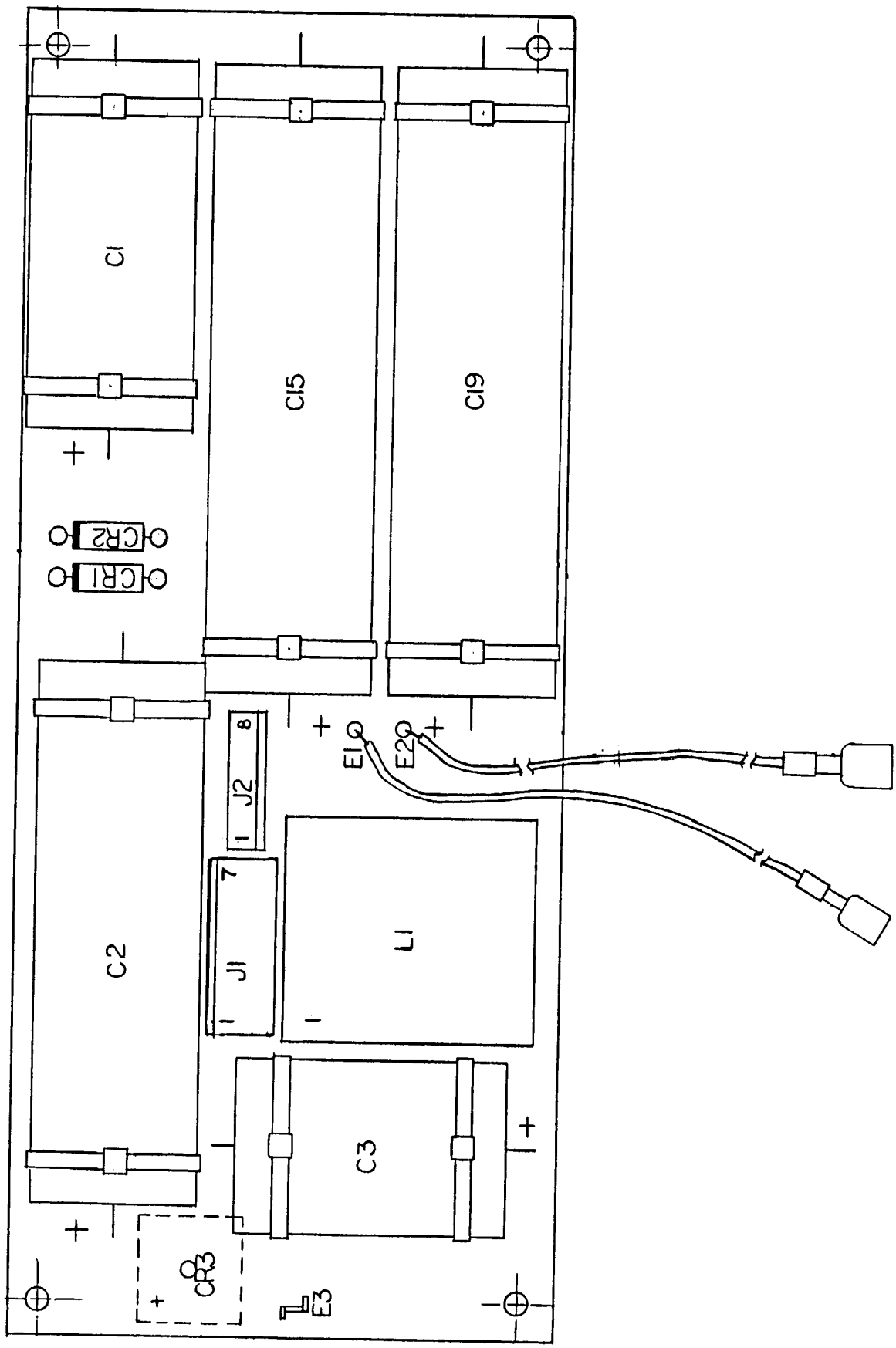


Figure 5. Power Supply Filter A15A1 Component Location Diagram (10073-3100)

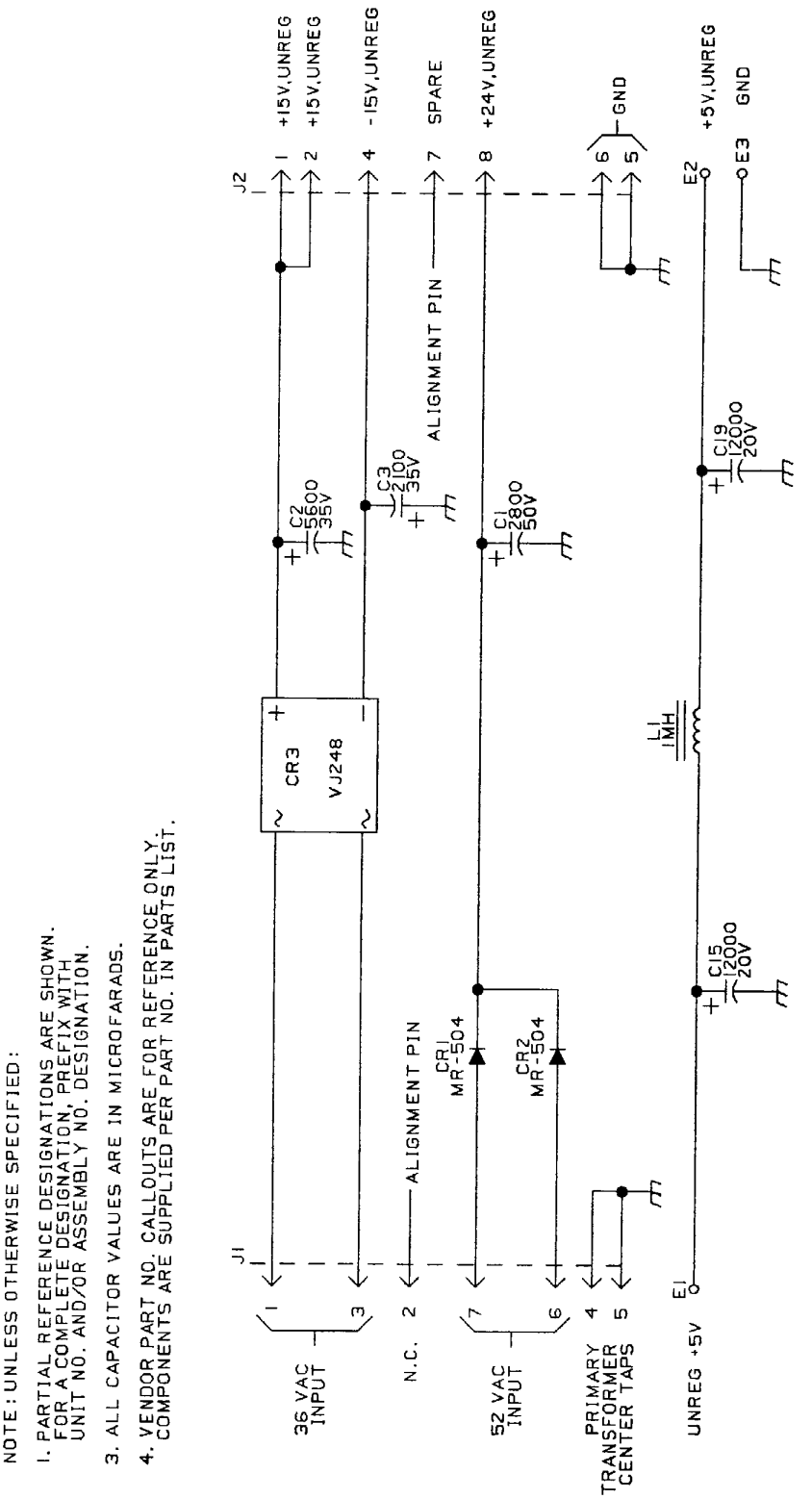


Figure 6. Power Supply Filter Assembly A15A1 Schematic Diagram (10073-3101 Rev. C)

5. POWER SUPPLY HEATSINK ASSEMBLY A15A2 CIRCUIT DESCRIPTION

Heatsink Assembly A15A2 consists of voltage regulators VR1 through VR6, CR1, and Regulator PWB A15A2A1. They are all mounted to a large heatsink bolted to the rear of the A15 assembly. Heatsink Assembly A15A2 may be removed from Power Supply Assembly A15 by removing the five mounting screws on the rear of the A15 assembly.

Regulator Assembly A15A2A1 receives the unregulated output voltages from the A15A1 assembly, and uses linear regulators mounted to Heatsink Assembly A15A2 to produce the regulated output voltages required. Table 4 lists the input voltages, the associated voltage regulator, and the output voltages.

Table 4. A15A2 Voltage Regulator Identification

Input Voltage	A15A2 Voltage Regulator	Output Voltage
+ 15 Unregulated	VR1	15 Vdc No. 1
+ 15 Unregulated	VR2	15 Vdc No. 2
-15 Unregulated	VR3	-15 Vdc
+ 5 Unregulated	VR4	+ 5 Vdc No. 1
+ 5 Unregulated	VR5	+ 5 Vdc No. 2
+ 24 Unregulated	VR6	+ 24 Vdc

All these voltages are routed through connector A15A2A1J3 (located on the bottom of the A15A2A1 PWB) for power distribution throughout the radio.

The A15A2A1 assembly also provides additional filtering to these voltages, as well as to a + 5 volt, unregulated output which does not receive any regulation. This supply voltage is regulated on the individual assemblies when used.

Table 5 is the A15A2 assembly parts list and figure 7 is the A15A2 assembly component location drawing. Table 6 is the A15A2A1 parts list and figure 8 is the A15A2A1 assembly component location drawing. Figure 9 is the A15A2 assembly and A15A2A1 assembly schematic diagram.

Table 5. Power Supply Heatsink Assembly A15A2 Parts List (10073-3250)

Ref. Desig.	Part Number	Description
	X-0814	INSULATOR, TRANSISTOR
	M10-0006-000	INSULATOR, TRANSISTOR
A1	10073-3200	REGULATOR PWB ASSY
CR1	D22-5004-001	RECTIFIER,BRIDGE
VR1	I11-0001-006	IC VR 7815 + 15V 1.5A 4%
VR2	I11-0001-006	IC VR 7815 + 15V 1.5A 4%
VR3	I12-0002-005	IC VR 7915 -15V 1.5A 4%
VR4	I11-0001-001	IC VR 7805 + 5V 1.5A 4%
VR5	I11-0001-001	IC VR 7805 + 5V 1.5A 4%
VR6	IC-0358	IC VR 317 ADJ V 1.5A

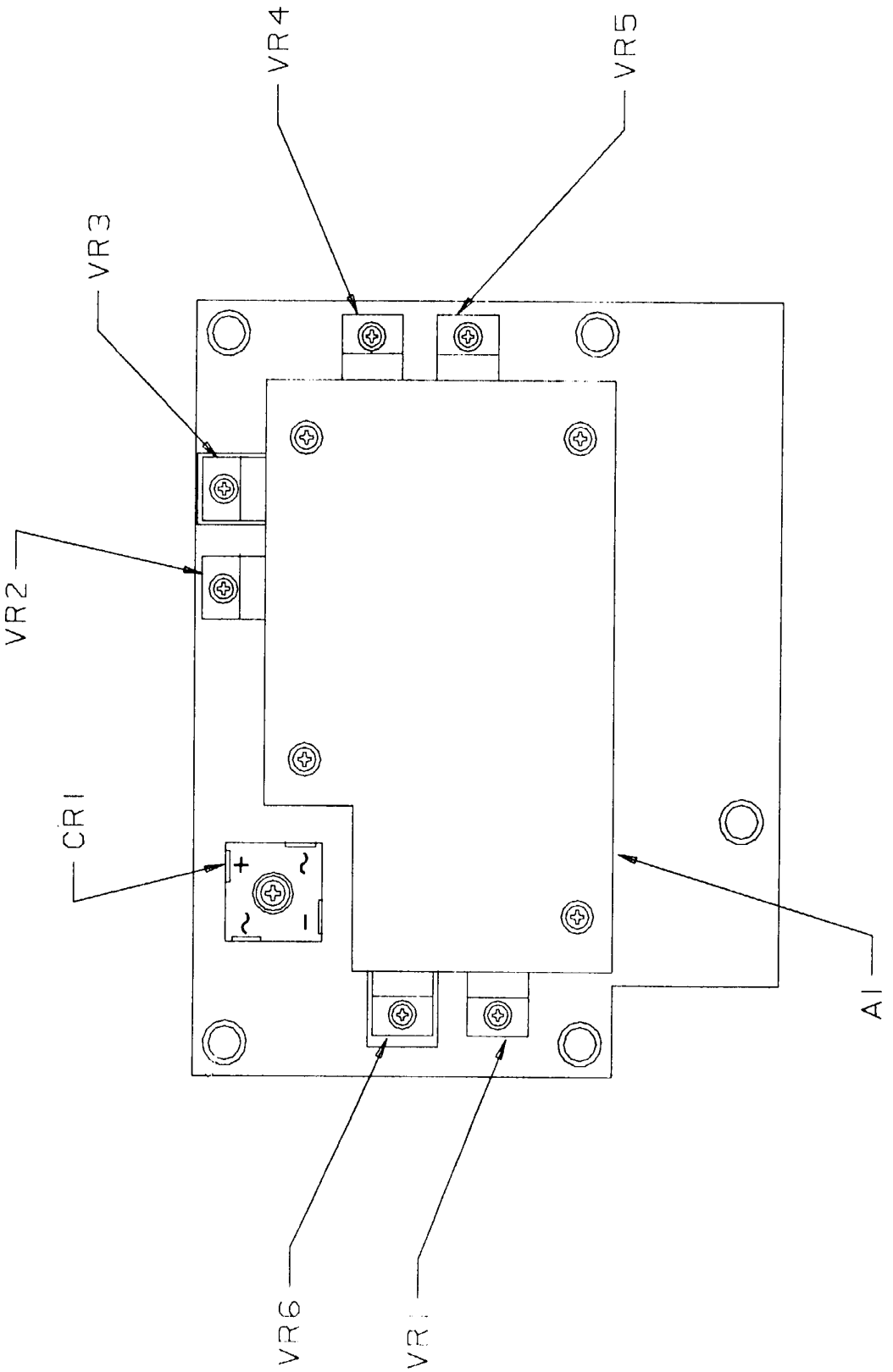


Figure 7. Power Supply Heatsink Assembly A15A2 Component Location Diagram (10073-3250)

Table 6. Power Supply Regulator Assembly A15A2A1 Parts List (10073-3200, Rev. J)

Ref. Desig.	Part Number	Description
C1	C26-0050-100	CAP 10UF 20% 50V TANT
C2	M39014/02-1320	CAP .47UF 10% 50V CER-R
C3	M39014/02-1320	CAP .47UF 10% 50V CER-R
C4	C26-0025-680	CAP 68UF 20% 25V TANT
C5	M39014/02-1310	CAP .1UF 10% 100V CER-R
C6	C26-0050-100	CAP 10UF 20% 50V TANT
C7	M39014/02-1320	CAP .47UF 10% 50V CER-R
C8	M39014/02-1320	CAP .47UF 10% 50V CER-R
C9	C26-0025-680	CAP 68UF 20% 25V TANT
C10	M39014/02-1310	CAP .1UF 10% 100V CER-R
C11	C26-0050-100	CAP 10UF 20% 50V TANT
C12	M39014/02-1320	CAP .47UF 10% 50V CER-R
C13	M39014/02-1320	CAP .47UF 10% 50V CER-R
C14	C26-0025-680	CAP 68UF 20% 25V TANT
C15	M39014/02-1310	CAP .1UF 10% 100V CER-R
C16	M39014/02-1320	CAP .47UF 10% 50V CER-R
C17	M39014/02-1310	CAP .1UF 10% 100V CER-R
C18	C26-0016-150	CAP 15UF 20% 16V TANT
C19	M39014/02-1320	CAP .47UF 10% 50V CER-R
C20	M39014/02-1310	CAP .1UF 10% 100V CER-R
C21	C26-0016-150	CAP 15UF 20% 16V TANT
C22	C25-0003-015	CAP 22UF 10% 50V TANT
C23	M39014/02-1320	CAP .47UF 10% 50V CER-R
C24	M39014/02-1320	CAP .47UF 10% 50V CER-R
C25	C25-0003-015	CAP 22UF 10% 50V TANT
C26	M39014/02-1310	CAP .1UF 10% 100V CER-R
C27	C25-0003-313	CAP 100UF 10% 20V TANT
C28	M39014/02-1310	CAP .1UF 10% 100V CER-R
E1	MP-0372	FAST-ON .125 PCB MOUNT
J1	J46-0032-008	HDR 8 PIN 0.100" SR
J2	J46-0032-010	HDR 10 PIN 0.100" SR
J3	J20-0009-425	747461-6 AMP RECEPTACLE
R1	RN55D2430F	RES 243 1% 1/8W MET FLM
R2	RN55D4421F	RES 4420 1% 1/8W MET FLM
TP1	J-0392	TP PWB BRN RA SIDE ACCESS

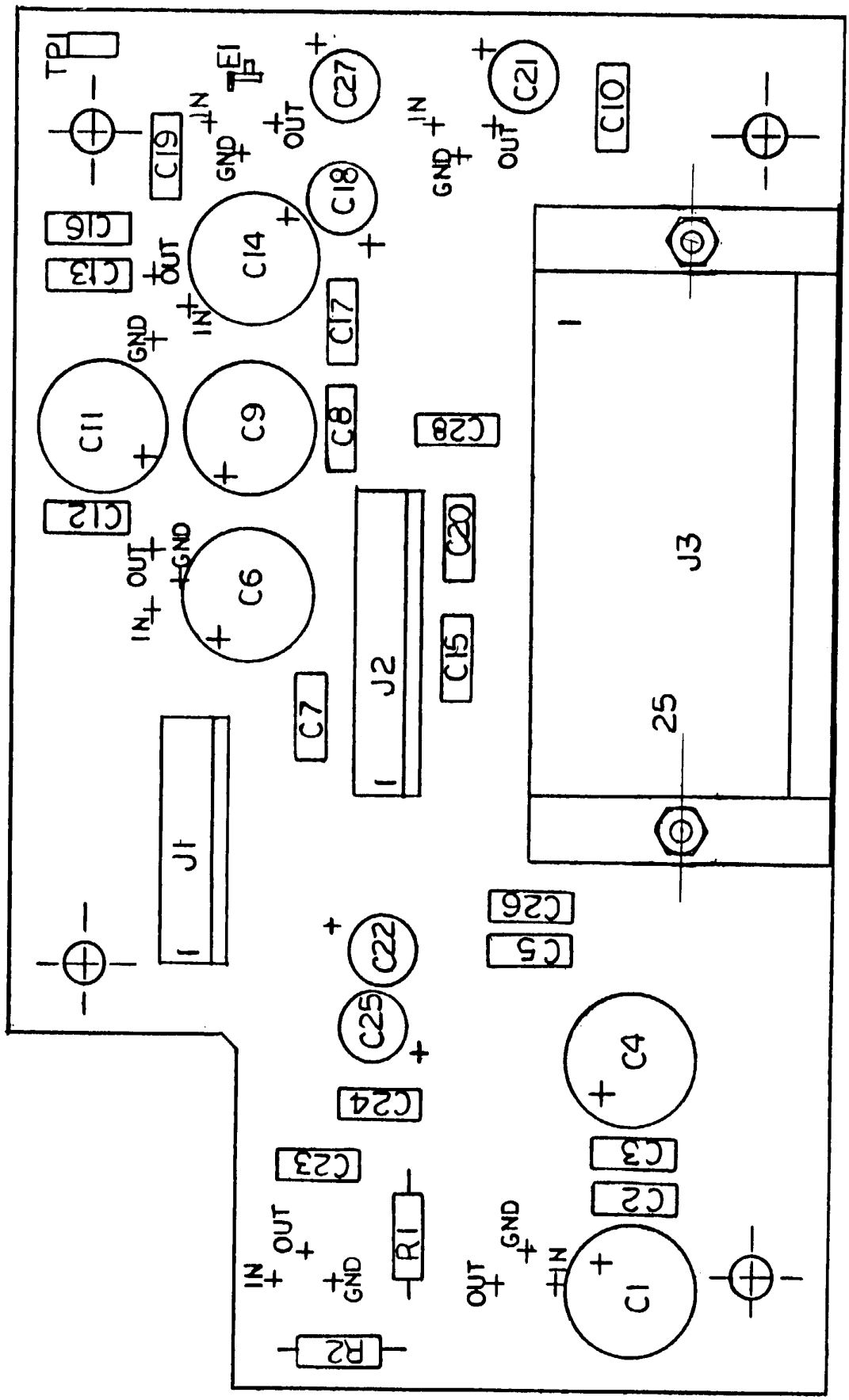


Figure 8. Power Supply Regulator Assembly A15A2A1 Component Location Diagram (10073-3200)

NOTE: UNLESS OTHERWISE SPECIFIED:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR A COMPLETE DESIGNATION, PREFIX WITH UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.
2. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, ±5%.
3. ALL CAPACITOR VALUES ARE IN MICROFARADS.
4. VENDOR PART NO. CALLOUTS ARE FOR REFERENCE ONLY. COMPONENTS ARE SUPPLIED PER PART NO. IN PARTS LIST.

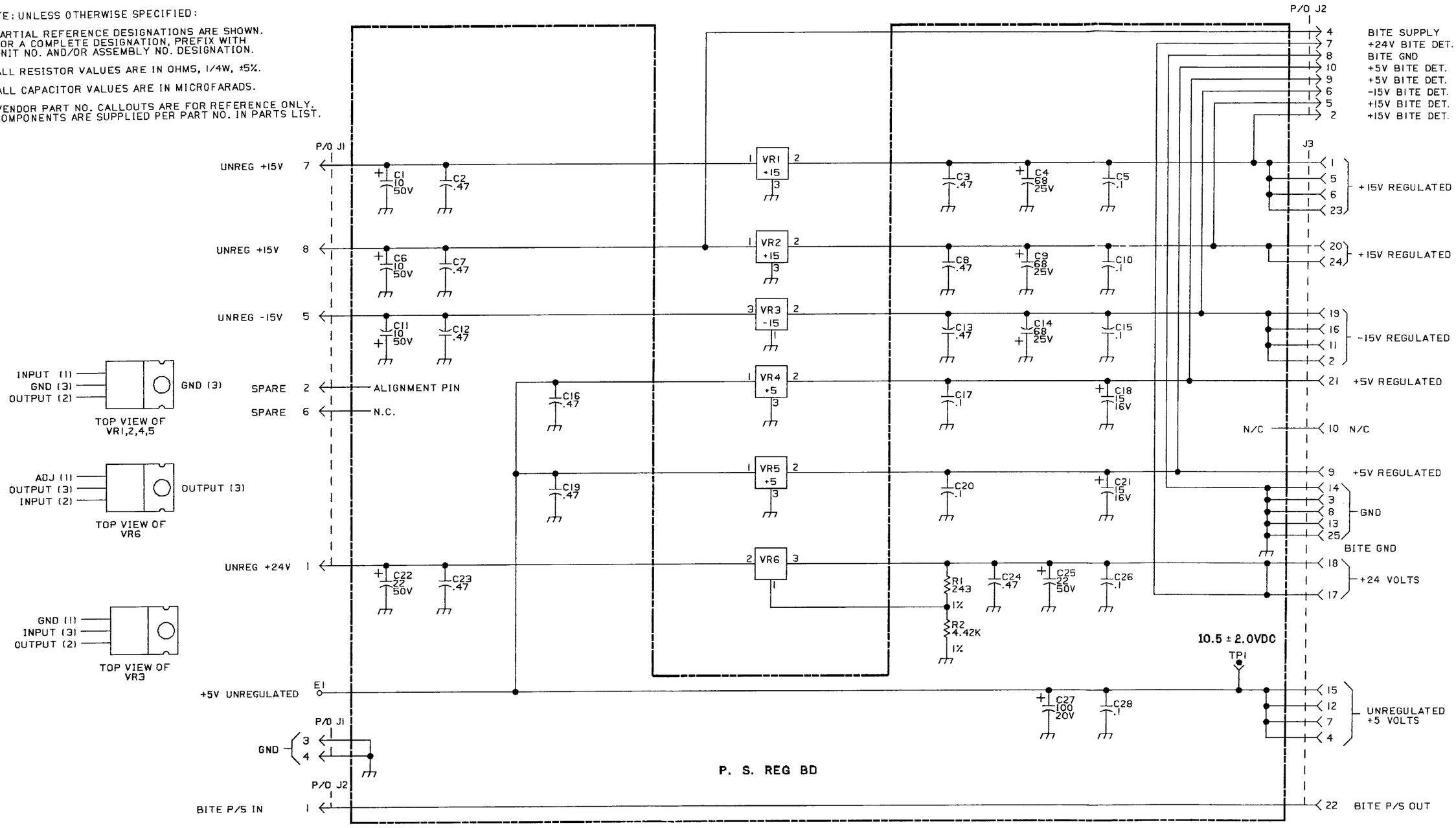


Figure 9. **Power Supply Heatsink Assembly A15A2 and Power Supply Regulator Assembly A15A2A1 Schematic Diagram (10073-3201 Rev. F)**

6. POWER SUPPLY BITE DETECTOR ASSEMBLY A15A3 CIRCUIT DESCRIPTION

The A15A3 assembly monitors all the regulated output voltages listed in table 4 and will issue a fault signal to Control Board Assembly A14 if any of them exceed a defined upper or lower limit. The A14 assembly will then issue a fault command and turn on the fault indicator on the front panel. This operation is performed continually while the receiver is operating.

The general operation scheme of the assembly is as follows, using the + 5 Vdc from the A15A2 assembly at A15A3 J1-9 as an example.

The + 5 Vdc at pin 9 is divided by resistor network R13-R14 to place a nominal 3.1 Vdc at U2D-10 (-) and U2C-9 (+). This level shall be referred to as V_{TEST}. The + 8 Vdc from VR1 is divided by R1 and R3 to place + 4 Vdc at U2D-11 (+), and by R2 and R4 to place + 2 Vdc at U2C-8 (-). The + 4 Vdc level shall be referred to as V_{HI}; the + 2 Vdc level as V_{LO}. These two levels establish the limits that V_{TEST} must not exceed.

Under conditions where V_{LO} is less than V_{TEST} is less than V_{HI}, U2C and U2D outputs are at + 8 volts. This feeds to U3C-8 (-). Since U3C-9 (+) input is always held fixed at 4 Vdc (V_{HI}), U3C output will be low (0 Vdc), Q1 will be biased off, and the BITE output signal will be at + 8 Vdc. This notifies the BITE circuits that the + 5 Vdc level is within its limits.

Assume that V_{TEST} exceeds V_{HI}. U2D output would switch 0 Vdc, causing U3C to switch to + 8 Vdc, turning on Q1. Q1 output would drag the BITE output to 0 Vdc, and notify the BITE circuits of an error condition. The same events would occur if V_{TEST} fell below V_{LO}, except that now U2C output would affect the switching of U3C.

This concept of a comparator pair providing the lower and upper limits is used to monitor the other regulated input voltages. Since all the comparator outputs are tied together, any one of them changing states would cause Q1 to issue an error signal.

Note that there are five comparator pairs, but six input voltages. The -15 Vdc input is used as a reference (instead of ground) for the two + 15 Vdc and one + 24 Vdc inputs, thereby eliminating the need for a separate comparator pair to monitor the -15 Vdc.

The approximate range of upper and lower input limits which will not trip the comparators is given in table 7.

Table 7. A15A3 BITE Detector Trip Limits

Input Voltage Vdc	Permissible Voltage Range
+ 5 Vdc No. 1	approximately 3.0 to 6.5
+ 5 Vdc No. 2	approximately 3.0 to 6.5
+ 15 vdc No. 1	approximately 13.0 to 17.0
+ 15 Vdc No. 2	approximately 13.0 to 17.0
-15 Vdc	approximately -13.0 to -17.0
+ 24 Vdc	approximately 21 to 26

Table 8 is the A15A3 assembly parts list, figure 10 is the A15A3 assembly component location diagram, and figure 11 is the A15A3 schematic diagram.

Table 8. Power Supply BITE Assembly A15A3 Parts List (10073-3300)

Ref. Desig.	Part Number	Description
C1	M39014/02-1310	CAP .1 UF
C2	C26-0025-100	CAP, TANT, 10UF, 25V
C3	M39014/02-1310	CAP .1 UF
J1	J46-0032-010	HEADER, 10 PIN DISCRETE
Q1	2N2222	XSTR, SS/GP, NPN
R1	RN55D4021F	RES,4020 1% 1/8W MET FLM
R2	RN55D7501F	RES,7500 1% 1/8W MET FLM
R3	RN55D4021F	RES,4020 1% 1/8W MET FLM
R4	RN55D2491F	RES,2490 1% 1/8W MET FLM
R5	RN55D1212F	RES,12.1K 1% 1/8W MET FLM
R6	RN55D1822F	RES,18.2K 1% 1/8W MET FLM
R7	RN55D1212F	RES,12.1K 1% 1/8W MET FLM
R8	RN55D1822F	RES,18.2K 1% 1/8W MET FLM
R9	RN55D1822F	RES,18.2K 1% 1/8W MET FLM
R10	RN55D2102F	RES,21.0K 1% 1/8W MET FLM
R11	RN55D1821F	RES,1820 1% 1/8W MET FLM
R12	RN55D3011F	RES,3010 1% 1/8W MET FLM
R13	RN55D1821F	RES,1820 1% 1/8W MET FLM
R14	RN55D3011F	RES,3010 1% 1/8W MET FLM
R16	R65-0003-472	RES,4.7K 5% 1/4W CAR FILM
R17	R65-0003-103	RES,10K 5% 1/4W CAR FILM
R18	R65-0003-103	RES,10K 5% 1/4W CAR FILM
R19	R65-0003-103	RES,10K 5% 1/4W CAR FILM
RU5	R65-0003-103	RES,10K 5% 1/4W CAR FILM
TP1	J-0392	TEST JACK,RT ANG,BRN
TP2	J-0387	TIP JACK, RED
TP3	J-0390	TEST JACK,RT ANG,ORN
TP4	J-0391	TEST JACK,RT ANG,YEL
TP5	J-0389	TEST,JACK,RT ANG,GRN
TP6	J-0393	TEST JACK,RT ANG,BLU
U1	I20-0006-000	IC LM339N COMPARATOR
U2	I20-0006-000	IC LM339N COMPARATOR
U3	I20-0006-000	IC LM339N COMPARATOR
VR1	I12-0006-008	IC VR 78L08A +8V .10A 4%

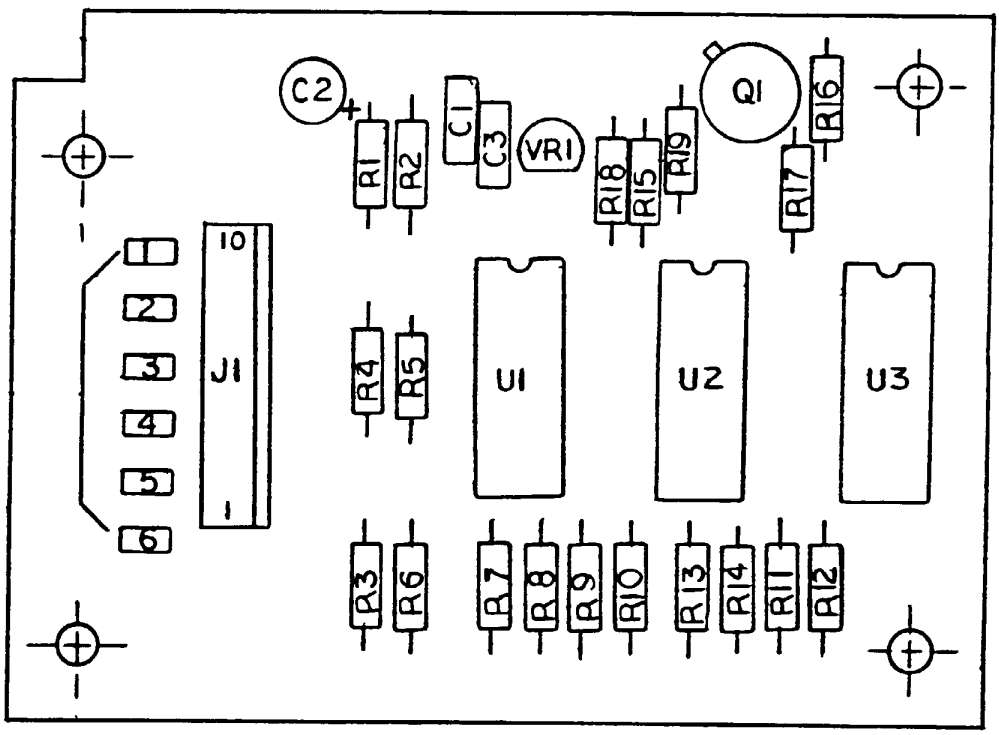
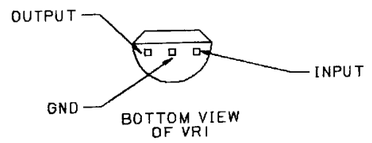


Figure 10. Power Supply BITE Assembly A15A3 Component Location Diagram (10073-3300)

NOTE: UNLESS OTHERWISE SPECIFIED:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR A COMPLETE DESIGNATION, PREFIX WITH UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.
2. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, ±5%.
3. ALL CAPACITOR VALUES ARE IN MICROFARADS.
4. VENDOR PART NO. CALLOUTS ARE FOR REFERENCE ONLY. COMPONENTS ARE SUPPLIED PER PART NO. IN PARTS LIST.
5. SEE GRAPHICS BELOW.



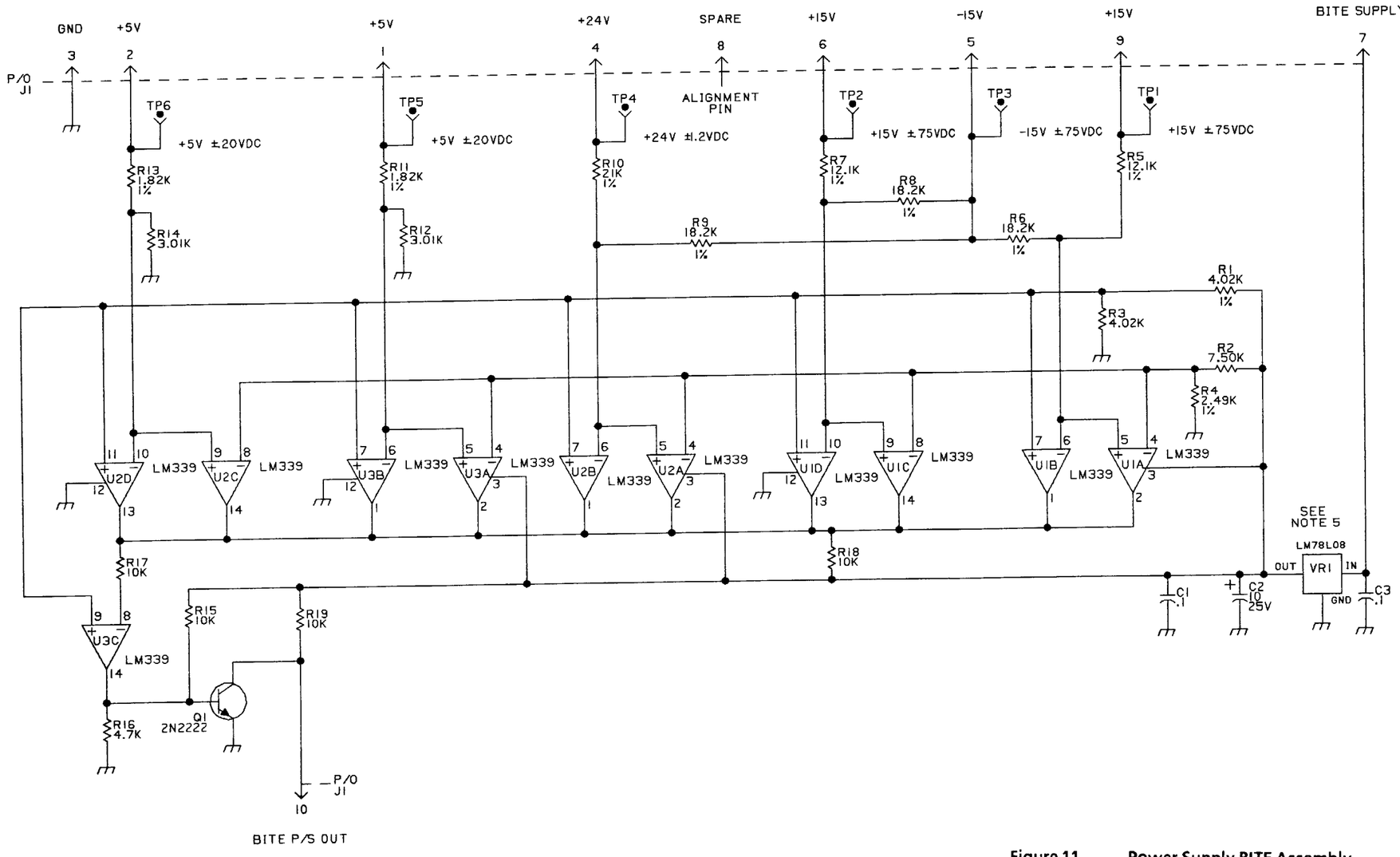


Figure 11. Power Supply BITE Assembly A15A3 Schematic Diagram (10073-3301 Rev. D)

7. A15 ASSEMBLY REMOVAL

WARNING

Potentially hazardous high voltages are present inside the A15 assembly whenever the receiver is connected to an ac line source. Do not attempt any repair to this assembly unless the line cord is disconnected. Do not operate the receiver without the protective cover properly installed over the assembly.

a. Disconnect the ac line cord.

b. Disconnect connector W3P1 in the channel on the bottom side of the receiver (underneath the A15 assembly). This carries the switched ac power to the front panel.

c. Remove mounting screws securing the A15 assembly cover, and remove cover.

d. Loosen the two captive screws inside the A15 assembly securing it to the chassis.

e. Place receiver on its side.

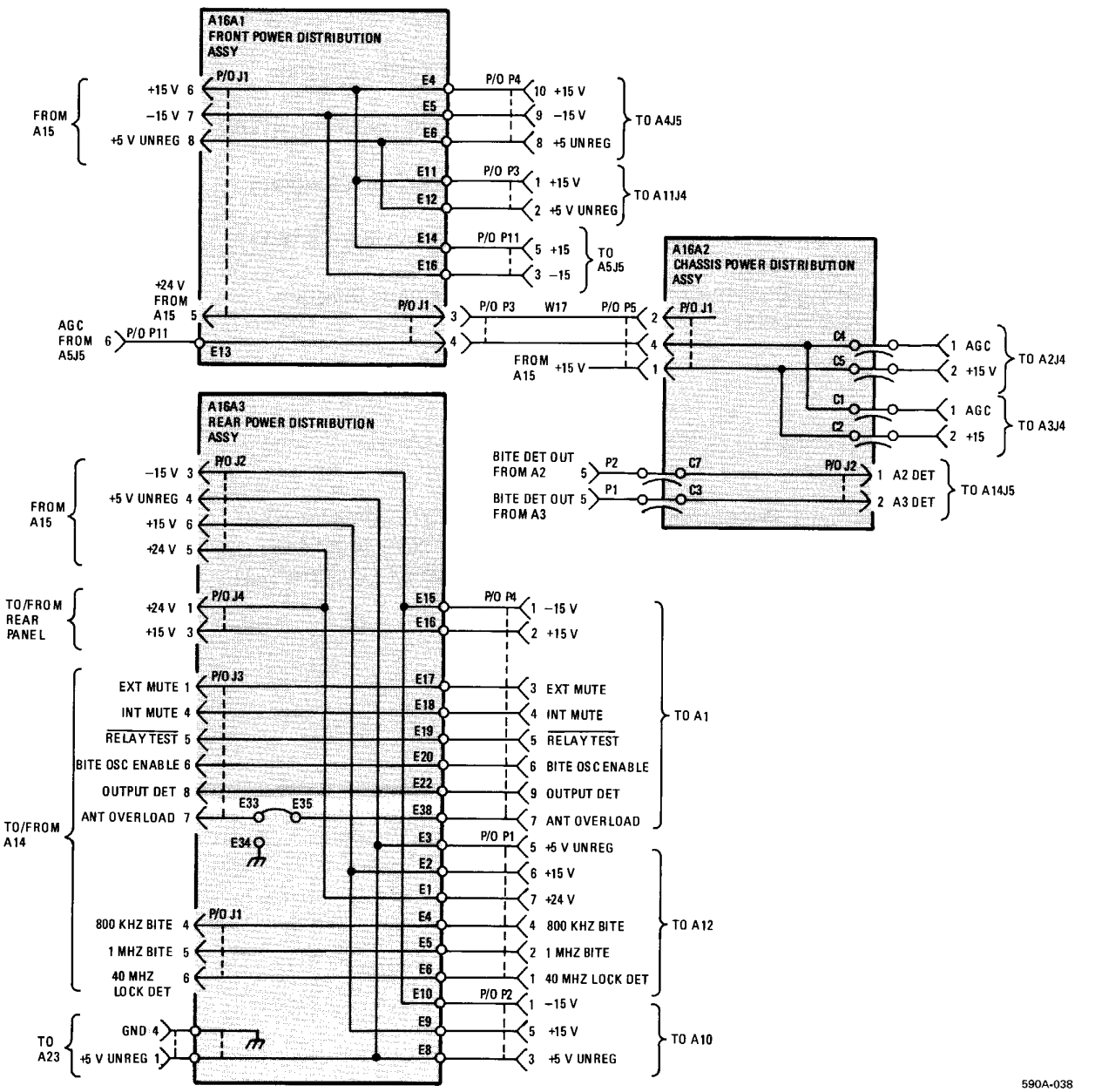
f. Remove four rear panel corner screws holding rear panel to chassis.

g. Disconnect A15J3.

h. Carefully pull the A15 assembly away from chassis. The rear portion of the chassis will not be supported after the A15 assembly is removed.

A16
POWER DISTRIBUTION ASSEMBLIES

A16A1 (FRONT): 10215-1200
A16A2 (CHASSIS): 10073-1400
A16A3 (REAR): 10215-1350



590A-038

TABLE OF CONTENTS

Paragraph		Page
1.	Introduction	1
2.	Part Lists, Component Locations, and Schematic Diagrams	1

LIST OF FIGURES

Figure		Page
1	Front Power Distribution Assembly A16A1 Component Locations (10215-1200)	3
2	Front Power Distribution Assembly A16A1 Schematic Diagram (10215-1201)	5
3	Chassis Power Distribution Assembly Component Locations A16A2 (10073-1400)	8
4	Chassis Power Distribution Assembly A16A2 Schematic Diagram (10073-1401)	9
5	Rear Power Distribution Assembly Component Locations A16A3 (10215-1350)	11
6	Rear Power Distribution Assembly A16A3 Schematic Diagram (10215-1351)	13

LIST OF TABLES

Table		Page
1	Front Power Distribution Assembly A16A1 (10215-1200) Parts List	1
2	Chassis Power Distribution Assembly A16A2 (10073-1400) Parts List	2
3	Rear Power Distribution Assembly A16A3 (10215-1350) Parts Lists	7

A16 POWER DISTRIBUTION

1. INTRODUCTION

The Front Chassis and Rear Power Distribution Assemblies A16A1, A16A2, and A16A3, as their names imply, distribute power supply outputs to other assemblies in the receiver. Some signals used control and detection pass through these assemblies going to and coming from A14. The three assemblies have no active components other than capacitors used for filtering. Locations of the assemblies are shown in the Main Chassis Interconnection section of this manual.

2. PART LISTS, COMPONENT LOCATIONS, AND SCHEMATIC DIAGRAMS

All components of the Front Power Distribution Assembly A16A1 are listed in table 1 and identified in figure 1. The circuit of the A16A1 assembly is shown schematically in figure 2. All components of the Chassis Power Distribution Assembly A16A2 are listed in table 2 and identified in figure 3. Figure 4 is the A16A2 assembly schematic diagram. All components of the Rear Power Distribution Assembly A16A3 are listed in table 3 and identified in figure 5. The circuit of the A16A3 assembly is shown schematically in figure 6.

Table 1. Front Power Distribution Assembly A16A1 (10215-1200) Parts List

Ref. Desig.	Part Number	Description
C4	CK05BX102K	CAP,1000PF 20% 200V CER
C5	CK05BX102K	CAP,1000PF 20% 200V CER
C8	CK05BX102K	CAP,1000PF 20% 200V CER
C9	CK05BX102K	CAP,1000PF 20% 200V CER
J1	J46-0033-008	CONN 8 PIN
W4	10073-7057	CABLE, RIBBON
W5	10073-7064	CABLE, RIBBON
W6	10073-7073	CABLE, RIBBON

Table 2. Chassis Power Distribution Assembly A16A2 (10073-1400) Parts List

Ref. Desig.	Part Number	Description
C1	C05-0003-102	CAP,F/T,1000PF
C2	C05-0003-102	CAP,F/T,1000PF
C3	C05-0003-102	CAP,F/T,1000PF
C4	C05-0003-102	CAP,F/T,1000PF
C5	C05-0003-102	CAP,F/T,1000PF
C6	C05-0003-102	CAP,F/T,1000PF
C7	C05-0003-102	CAP,F/T,1000PF
J1	J46-0033-004	RT ANGLE POST HEADER ASSY
J2	J46-0033-004	RT ANGLE POST HEADER ASSY
P1	J46-0016-005	CONNECTOR 5 PIN
P2	J46-0016-005	CONNECTOR 5 PIN

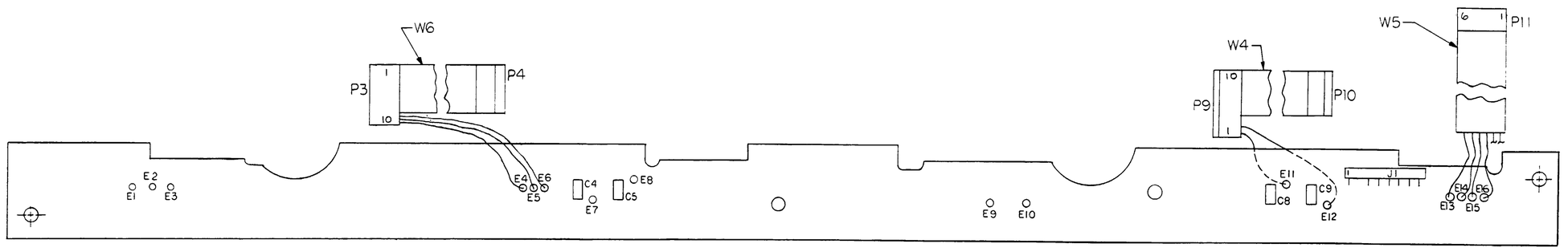


Figure 1. Front Power Distribution Assembly A16A1 Component Locations (10215-1200)

NOTE: UNLESS OTHERWISE SPECIFIED:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR A COMPLETE DESIGNATION, PREFIX WITH UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.

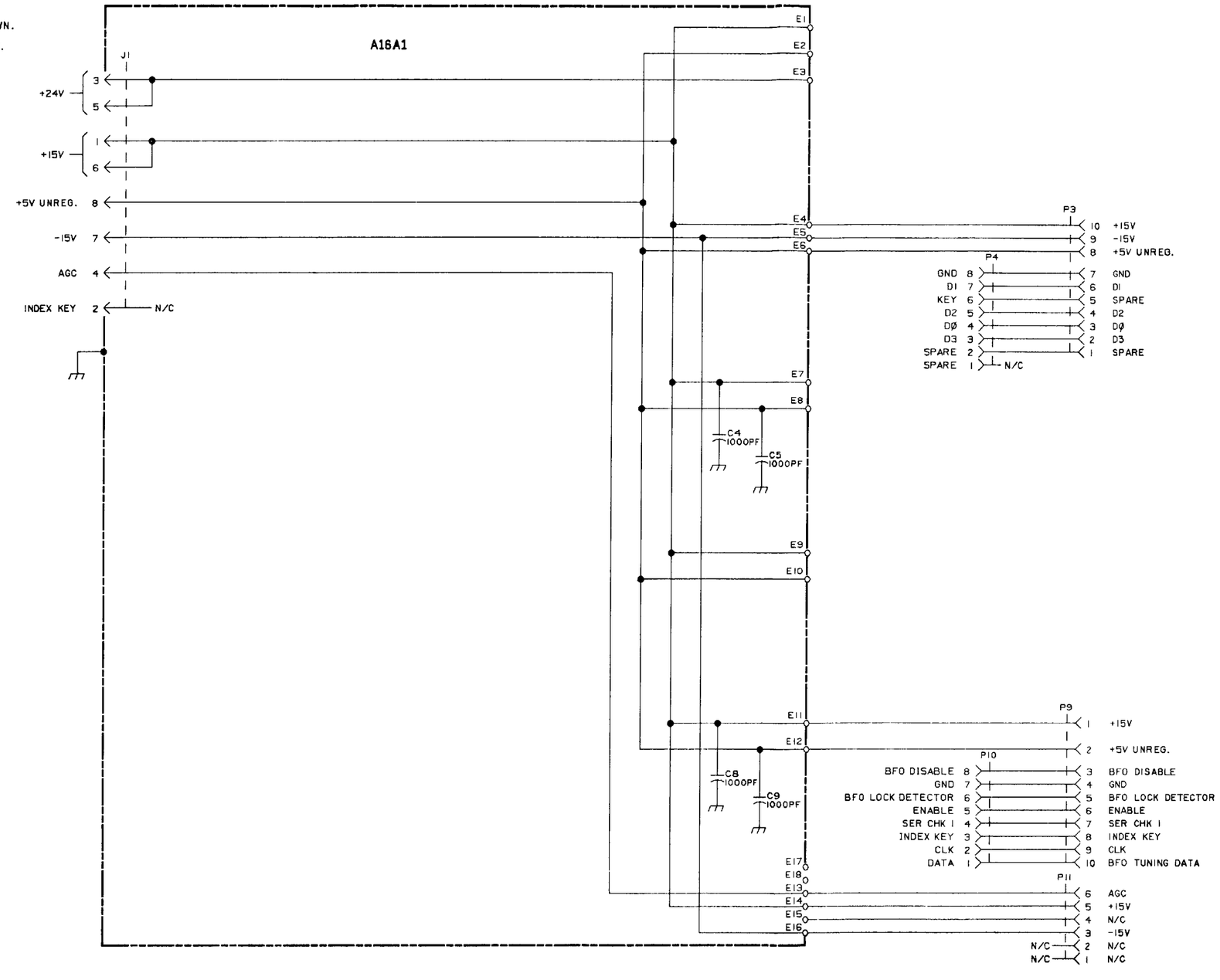


Figure 2. **Front Power Distribution Assembly A16A1 Schematic Diagram (10215-1201, Rev. B)**

Table 3. Rear Power Distribution Assembly A16A3 (10215-1350, Rev. C) Parts List

Ref. Desig.	Part Number	Description
C1	CK05BX102K	CAP 1000PF 10% 200V CER
C2	CK05BX102K	CAP 1000PF 10% 200V CER
C3	CK05BX102K	CAP 1000PF 10% 200V CER
C4	CK05BX102K	CAP 1000PF 10% 200V CER
C5	CK05BX102K	CAP 1000PF 10% 200V CER
C6	CK05BX102K	CAP 1000PF 10% 200V CER
C7	CK05BX102K	CAP 1000PF 10% 200V CER
C8	CK05BX102K	CAP 1000PF 10% 200V CER
C9	CK05BX102K	CAP 1000PF 10% 200V CER
C10	CK05BX102K	CAP 1000PF 10% 200V CER
C15	CK05BX102K	CAP 1000PF 10% 200V CER
C16	CK05BX102K	CAP 1000PF 10% 200V CER
C17	CK05BX102K	CAP 1000PF 10% 200V CER
C18	CK05BX102K	CAP 1000PF 10% 200V CER
C19	CK05BX102K	CAP 1000PF 10% 200V CER
C20	CK05BX102K	CAP 1000PF 10% 200V CER
C21	CK05BX102K	CAP 1000PF 10% 200V CER
C22	CK05BX102K	CAP 1000PF 10% 200V CER
C23	CK05BX102K	CAP 1000PF 10% 200V CER
C24	CK05BX102K	CAP 1000PF 10% 200V CER
J1	J46-0033-006	CONNECTOR, 6 PIN
J2	J46-0033-006	CONNECTOR, 6 PIN
J3	J46-0033-008	CONNECTOR 8 PIN
J4	J46-0033-003	CONNECTOR 3 PIN
JMP1	MP-1142	CIRCUIT JUMPER
JMP2	MP-1142	CIRCUIT JUMPER
P1	J46-0016-008	CONNECTOR, 8 PIN
P2	J46-0016-006	CONNECTOR, 6 PIN
P4	J46-0016-010	CONNECTOR,10 PIN
W43	10073-6915	CABLE ASSY

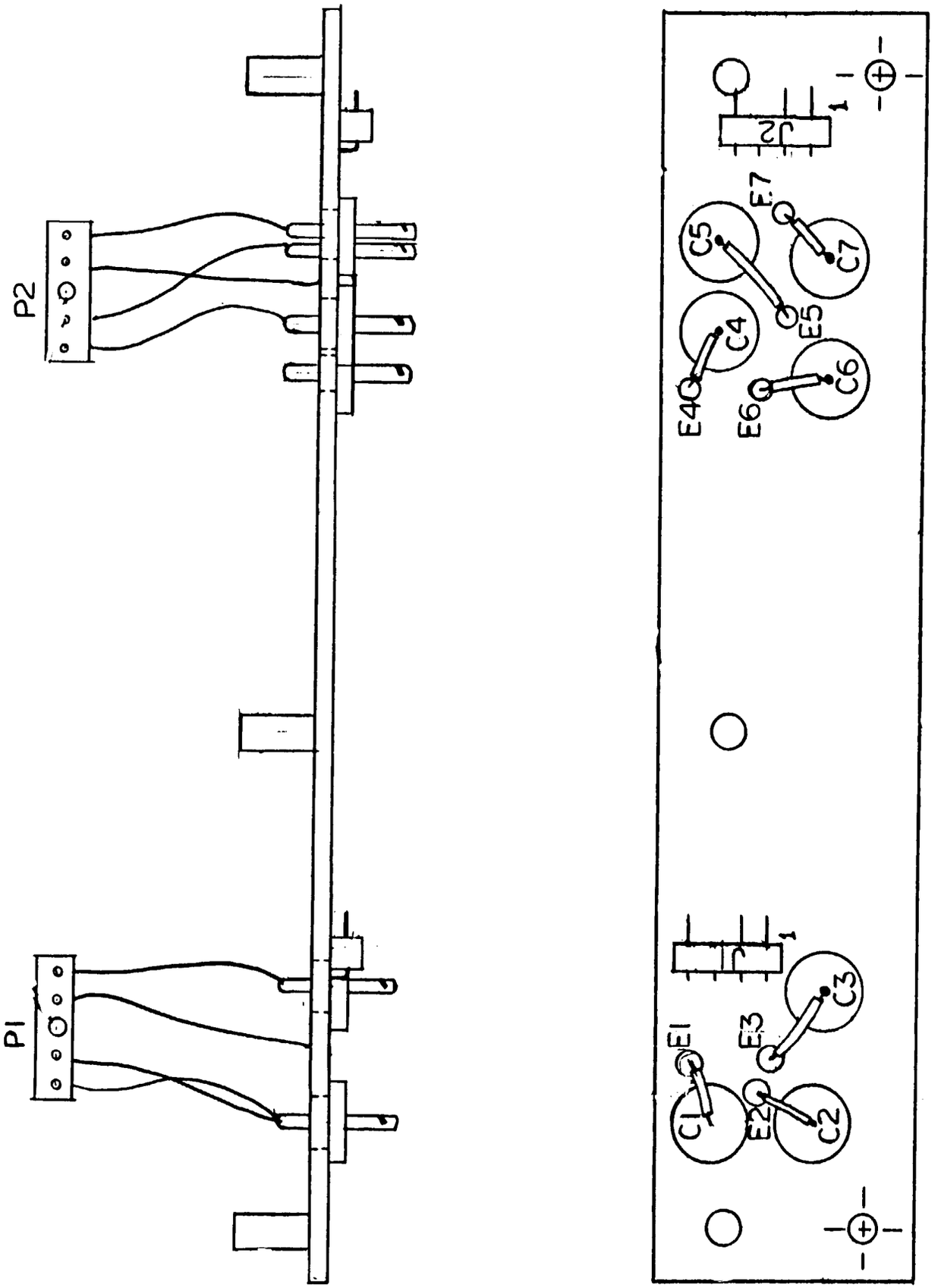


Figure 3. Chassis Power Distribution Assembly Component Locations A16A2 (10073-1400)

NOTE: UNLESS OTHERWISE SPECIFIED:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR A COMPLETE DESIGNATION, PREFIX WITH UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.
2. ALL CAPACITOR VALUES ARE IN MICROFARADS.
3. VENDOR PART NO. CALLOUTS ARE FOR REFERENCE ONLY. COMPONENTS ARE SUPPLIED PER PART NO. IN PARTS LIST.

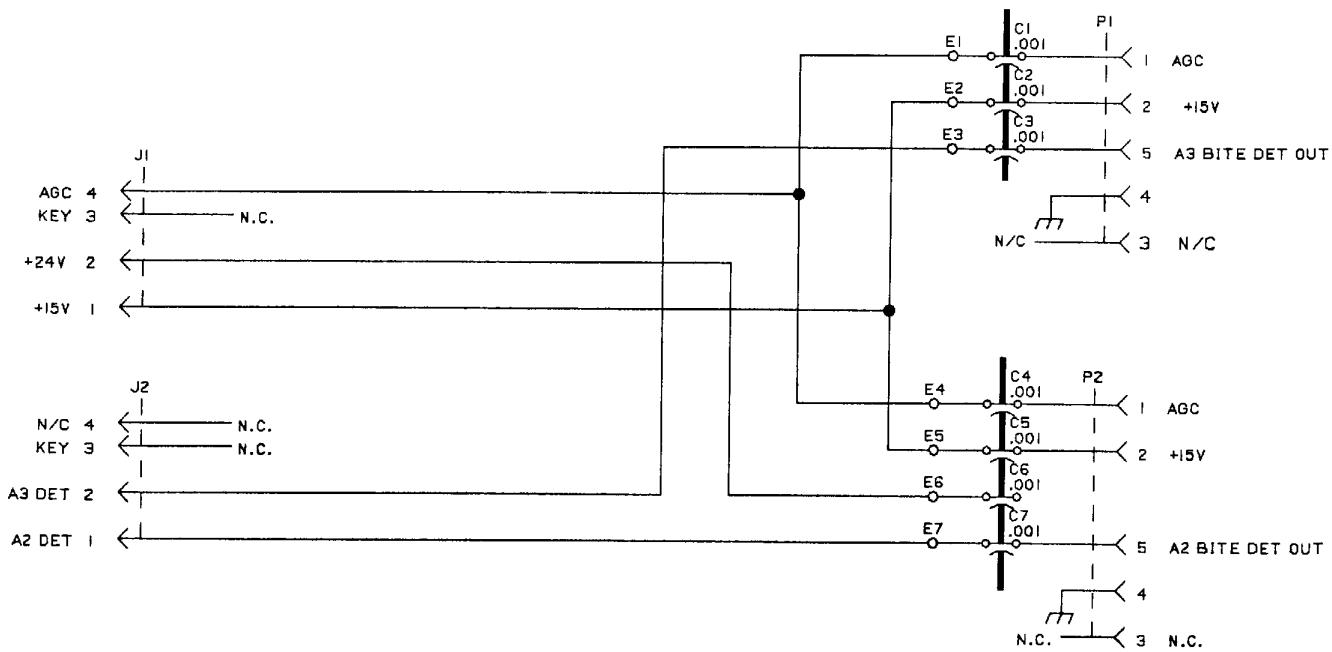
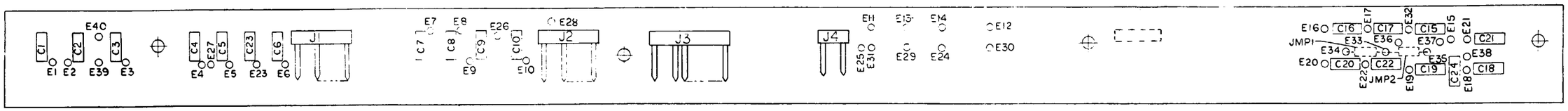


Figure 4. Chassis Power Distribution Assembly A16A2 Schematic Diagram (10073-1401, Rev. C)



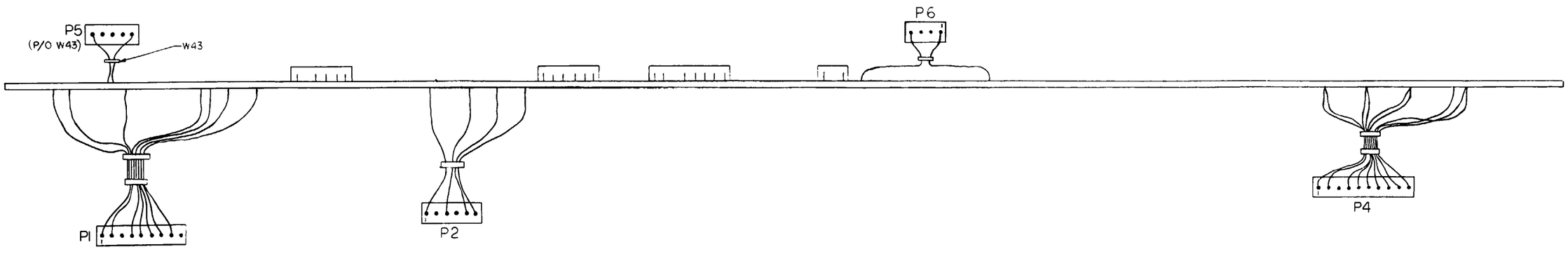


Figure 5. Rear Power Distribution Assembly Component Locations A16A3 (10215-1350, Rev. D)

NOTE: UNLESS OTHERWISE SPECIFIED:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR A COMPLETE DESIGNATION, PREFIX WITH UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.
2. ALL CAPACITOR VALUES ARE 1000 PICOFARADS.
3. THE 10121-1359 PWB IS COMMON TO THE 10121-1350-01/02, THE 10073-1350, AND THE 10215-1350. FOR APPLICATION OF THIS PWB INTO THE RF-590A (10215-1350), JMP1 IS INSTALLED E33 TO E35, JMP2 IS INSTALLED E36 TO E37 AND C24 IS ADDED.
4. P6 USED ON 10215-1350-01.

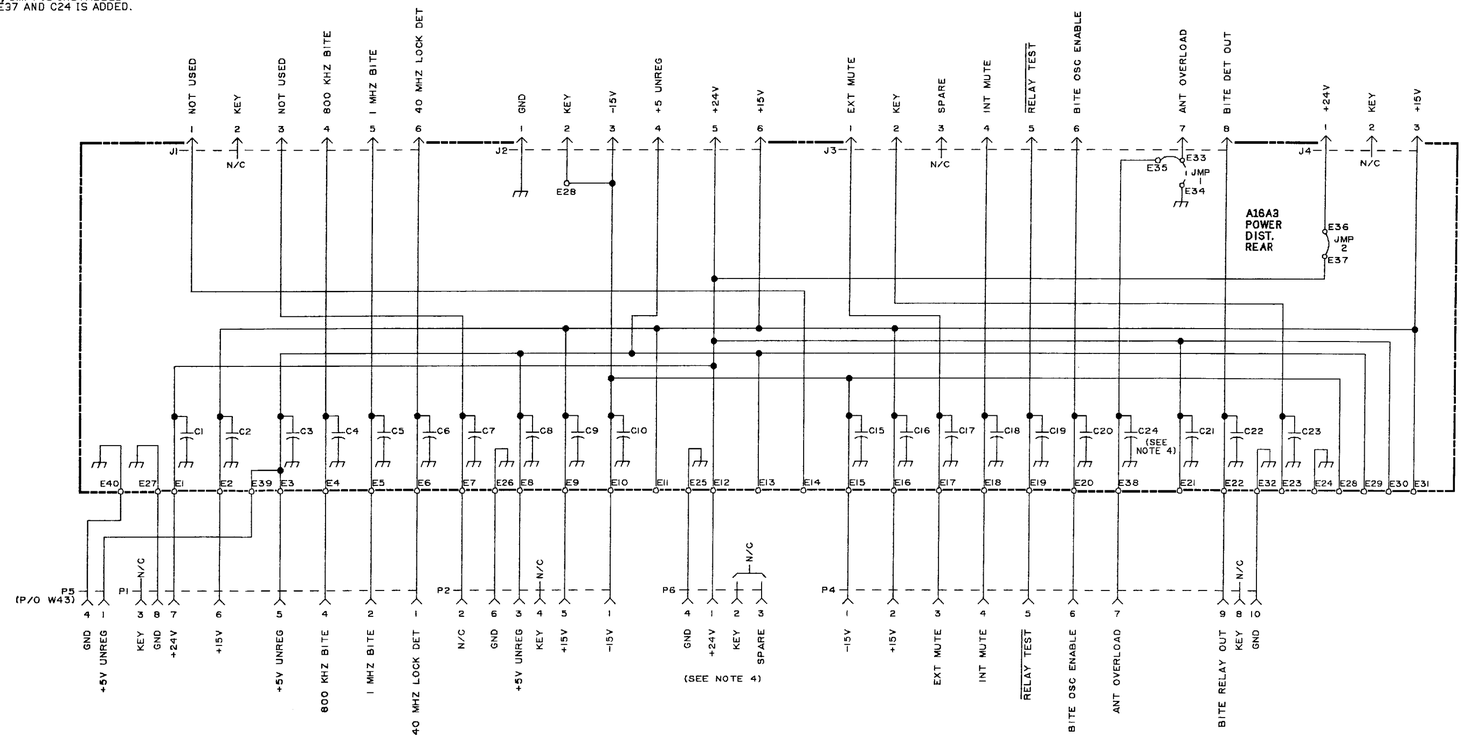


Figure 6. Rear Power Distribution Assembly A16A3 Schematic Diagram (10215-1351, Rev. C)

A18
ISB IF/AUDIO ASSEMBLY

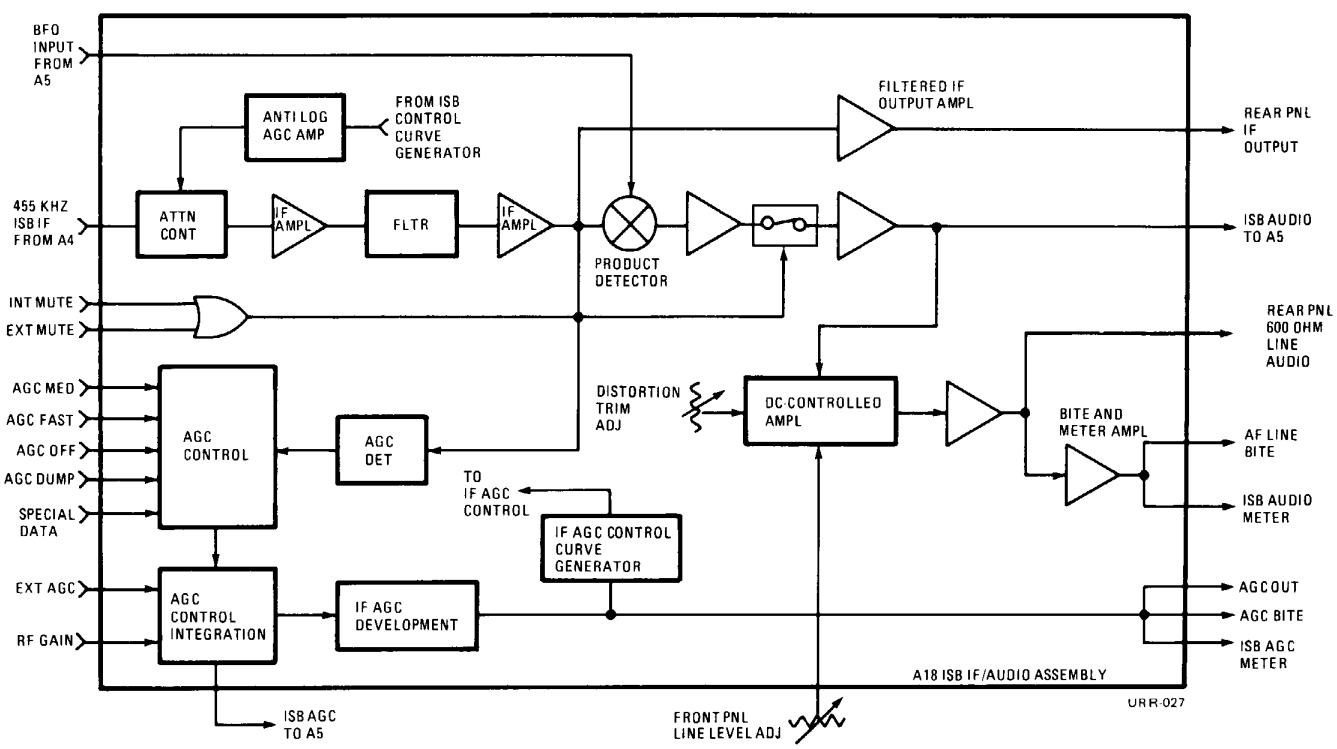


TABLE OF CONTENTS

Paragraph		Page
1.	General Description	1
2.	Interface Connections	1
3.	Circuit Description	2
3.1	455-kHz IF Circuit	2
3.2	Product Detector and ISB Audio Circuit	2
3.3	Line Output and Meter Amplifier Circuit	5
3.4	AGC Circuits	5
3.4.1	AGC Detector and Logarithmic Amplifier	6
3.4.2	Absolute Value Amplifier and pulse Width Modulator	6
3.4.3	Comparator and One-Shot Timer	6
3.4.4	AGC Charge Pump	7
3.4.5	AGC Source Selection and Curve Shaping	7
3.4.6	Antilogarithmic Amplifier and PIN Diode Attenuator	8
4.	Maintenance	8
4.1	IF Level Adjustment	8
4.2	R5 Adjustment, IF AGC Gain Set	8
4.3	R67 Adjustment, AGC 1 dB Compression Point	9
4.4	Distortion Trim Adjustment	9
4.5	R194 Adjust, Dead Zone	9
5.	Parts List, Component Locations, and Schematic Diagram	10

LIST OF FIGURES

Figure		Page
1	ISB IF/Audio Assembly A18 Functional Block Diagram	3
2	Dead Zone Adjustment Waveform	10
3	ISB IF/Audio Assembly A18 Component locations (10215-6300)	18
4	ISB IF/Audio Assembly A18 Schematic Diagram (10215-6301)	19

LIST OF TABLES

Table		Page
1	A18 ISB IF/Audio Assembly Interface Connections	1
2	AGC Charge Pump Control Truth Table	7
3	A18 ISB IF/Audio Assembly (Part No. 10215-6300-02) Parts List	11

A18 ISB IF/AUDIO ASSEMBLY

1. GENERAL DESCRIPTION

ISB IF/Audio Assembly A18 amplifies and filters the 455-kHz ISB IF signal from IF Filter Assembly A4, and detects the audio component to produce an ISB audio signal for Audio Assembly A5. The ISB IF output is available at J2 on the Receiver rear panel. The ISB line audio output is available at connectors TB1-13 through TB1-15 or J7-8 through J7-10 on the Receiver rear panel. The ISB IF/Audio Assembly also provides an ISB line level and RF indication for the front panel meter.

The ISB IF/Audio Assembly incorporates an AGC circuit that controls the IF amplifier gain over a 90-dB dynamic range. The AGC decay characteristic (slow, medium, fast, or data) is selected using the front panel AGC SPEED switch.

2. INTERFACE CONNECTIONS

Table 1 lists the various input/output connections to ISB IF/Audio Assembly A18. Refer to the Main Chassis Interconnect tab section for additional detail.

Table 1. A18 ISB IF/Audio Assembly Interface Connections

Connector	Function	Characteristics
J1	IF Input	455 kHz, -97/-5 dBm, 50 ohms
J2	BFO In	455 kHz, 0 dBm, 50 ohms
J3	ISB Output	455 kHz, -6 dBm (under AGC control), 50 ohms
J4-1	ISB AGC Meter	ISB signal strength
J4-2	ISB Audio Meter	ISB line audio level
J4-3	Index Key	
J4-4	External Mute	+ 5 Vdc = mute
J4-5	Line Audio Adjustment	0 to -15 Vdc
J4-6	AGC BITE	Typically 1.5 Vdc during BITE test
J4-7	AF Line BITE	
J4-8	IF Input BITE	
J4-9	Internal Mute	+ 5 Vdc = mute
J4-10	Spare	
J5-1	ISB Audio	To Audio Assembly A5
J5-2	ISB AGC	To AGC circuit on Audio Assembly A5
J5-3	AGC Medium	+ 5 Vdc = selected
J5-4	AGC Fast	+ 5 Vdc = selected
J5-5	AGC Off	+ 5 Vdc = AGC off
J5-6	RF Gain	0 to + 12 Vdc input

Table 1. A18 ISB IF/Audio Assembly Interface Connections (Cont.)

Connector	Function	Characteristics
J5-7	Index Key	
J5-8	-15 V	
J5-9	+ 15 V	
J5-10	Special Data	0 V = Data, + 5 V = Normal
J6-1	AGC Out	0 to + 6 Vdc output
J6-2	N/C	
J6-3	Index Key	
J6-4	Line Out	
J6-5	AGC Dump	
J6-6	Line Center Tap	
J6-7	External AGC	0 to + 6 Vdc input
J6-8	Line Return	

3. CIRCUIT DESCRIPTION

Refer to the tab section front cover, functional block diagram (shown in figure 1) and schematic diagram (shown in figure 3) during the following circuit description.

3.1 455-kHz IF Circuit

The IF Input signal from IF Filter Select Assembly A4 is applied to IF amplifier Q10 through Q12 via balun transformer T2. Q10 through Q12 amplify the IF signal level by approximately 60 dB. A PIN diode attenuator circuit (CR1, CR2, CR5, and CR8) provides a dynamic control range of over 90 dB. The PIN diode attenuator operates in response to the output current from the antilog amplifier (U5A, U5B, U3 and Q1). FL1 is a ceramic-type 455-kHz IF filter that limits the IF amplifier bandwidth to approximately 20 kHz.

Q3 and Q4 amplify the output of FL1 by approximately 20 dB to produce an overall IF gain of approximately 75 dB. Q5 is a buffer amplifier for the rear panel ISB IF output (J2). This BNC connector provides a convenient IF output for receiver testing and systems applications.

Q6 and Q7 detect the IF output from Q4. Since the output of Q6 tracks the IF envelope power, it can be used as a source voltage for AGC development. The emitter voltage of Q6 is applied to a logarithmic amplifier (U4, U5C, and U5D). The logarithmic output at U5-14 is applied to the AGC control circuit.

The IF input is also applied to IF input BITE amplifier Q2. The output voltage of Q2 is monitored by the BITE circuitry on Control Board Assembly A14.

3.2 Product Detector and ISB Audio Circuit

The ISB IF output is heterodyned with the BFO input signal by a product detector circuit. The BFO signal is applied to the (+) carrier input (pin 8) of demodulator U13 via attenuator R72 through R74. The (-) carrier input (pin 10) is connected to ground via R75. The IF output of amplifier Q4 is applied to the (+) signal (pin 1) input of U13 via attenuator R81/R126. Resistors R81 and R126 provide 26 dB attenuation to the IF signal to

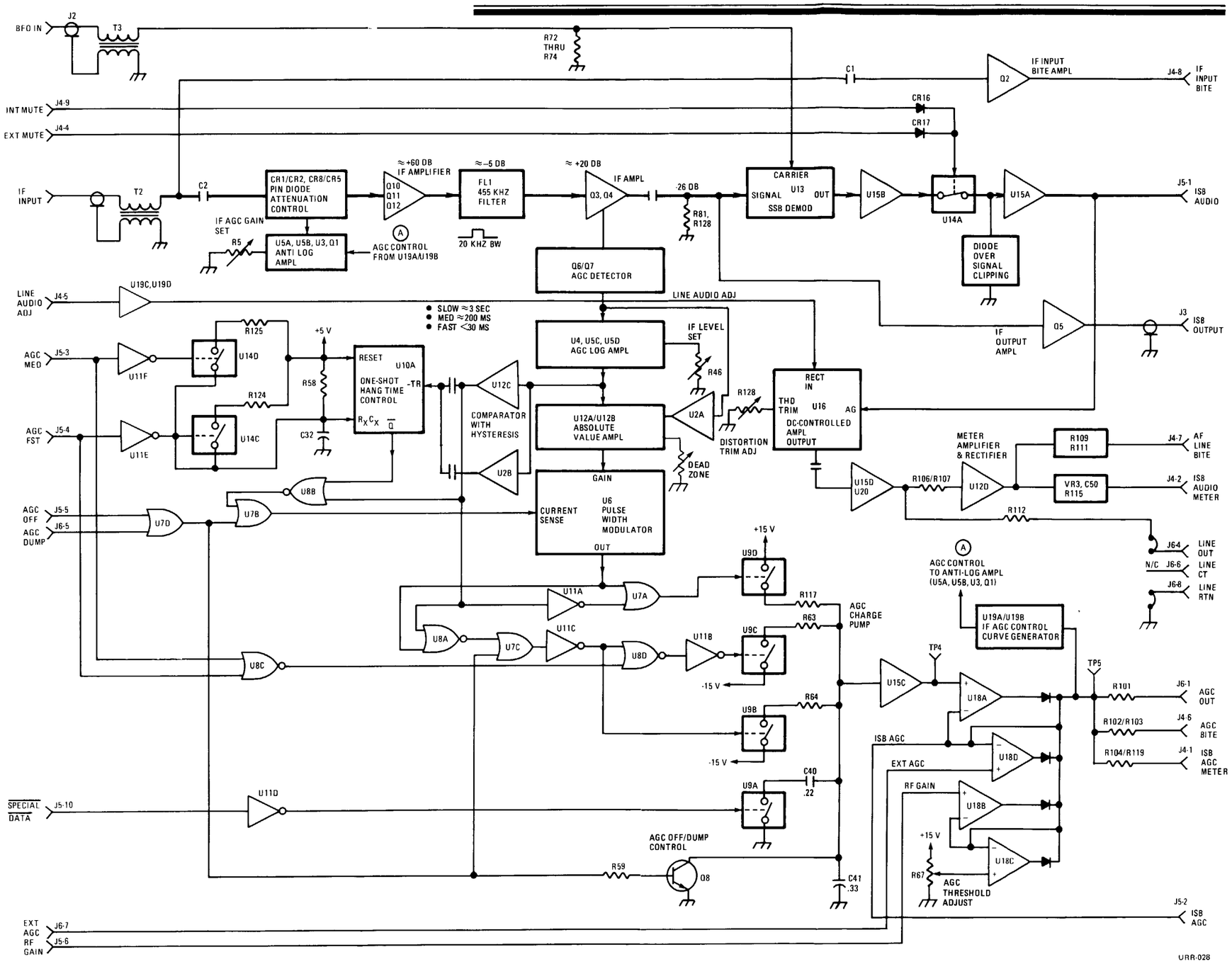


Figure 1. **ISB IF/Audio Assembly A18 Functional Block Diagram**

provide the proper audio level from the product detector. The output of U13 (pins 6 and 12) is applied to differential amplifier U15B.

Diodes CR16 and CR17 form an OR gate that controls analog switch U14A. U14A is normally closed. A high input on either the external or internal mute lines will open switch U14A, breaking the ISB audio signal path. Diodes CR19 through CR24 provide overvoltage signal clipping protection. Operational amplifier U15A buffers the ISB audio signal, which is then routed to Audio Assembly A5. The output of U15A is also applied to the variable gain input (pin 14) of dc-controlled amplifier U16B.

3.3 Line Output and Meter Amplifier Circuit

The ISB line audio output is independent of the front panel AF GAIN control. The line audio output level is set up by adjusting the ISB-LSB ADJ potentiometer on the Receiver front panel. This screwdriver-adjustable potentiometer outputs a wiper voltage between 0 Vdc and -15 Vdc. (-15 Vdc correlates with maximum line level.) The output level is normally set to produce + 10 dBm into 600 ohms, but can be changed to accommodate other system application requirements. Full power output from the line amplifier is + 15 dBm into an unbalanced 600 ohm load.

The ISB-LSB ADJ wiper voltage is applied to the gain control input (pin 15) of U16B via buffer amplifiers U19C/U19D. The ISB audio signal is applied to the variable gain input (pin 14) of U16B. The wiper voltage is used to control the output of the variable gain cell. R128 provides distortion compensation by trimming the internal offset voltages of U16B.

The output of U16B is distributed to the AF line BITE, ISB audio meter, and line output circuits via operational amplifier U15D and current amplifier U20. The front-panel line meter is driven by the meter amplifier U12D and associated circuitry. The meter is calibrated to measure line audio in dBm into a 600-ohm load. Full scale on the meter is + 15 dBm.

3.4 AGC Circuits

The AGC control loop detects any change in the IF input level and reacts to amplify or attenuate the signal in order to maintain the desired output level. The fast attack reaction characteristic is built into the system, but the decay time is selectable at the Receiver front panel. Four AGC SPEED options are available: slow (approximately 3 seconds), medium (approximately 200 ms), fast (less than 30 ms), and data (less than 20 ms). A slow or medium AGC characteristic should be selected for CW or voice communications. This will prevent pumping of the AGC system and possible loss of continuity in the intelligence during pauses in modulation or transmission. A fast AGC characteristic is desired for data communication.

When the Receiver is operating under AGC control, the input voltage to the inverting log amplifier U4, U5C, U5D from Q6 is approximately 1 V peak. Under this condition, the log amplifier produces an output voltage of 0 V. If the IF signal level increases above the AGC threshold, the log amplifier input will rise above 1 V, the log amplifier output will go negative, and comparator U12C output will go high. The pulse width modulator U6 and associated logic circuitry then switches the charge pump to increase the AGC control voltage. The AGC voltage is then scaled by the curve generator circuit U19A, U19B and applied to the antilog amplifier. The antilog amplifier controls the PIN diode attenuator, which reduces the IF gain until the signal level is at the desired output level.

When the IF output signal level falls below the desired output level, the inverting log amplifier input will fall below 1 V, the log amplifier output will go positive, and the comparator (U12C or U2B) output will go low. The pulse width modulator then switches the charge pump to decrease the AGC control voltage. The comparator also triggers the one-shot timer U10A, which controls the AGC hangtime characteristic. The pulse width modulator is shut off until the timer expires. The AGC voltage is scaled and applied to the antilog amplifier. The PIN diode attenuator the increases the IF gain until the signal level is in the AGC region.

3.4.1 AGC Detector and Logarithmic Amplifier

Transistors Q6 and Q7 detect the peak envelope power of the IF stage. When the IF signal level is at the desired output level,approximately 1 V is present at the log amplifier input. The log amplifier will accurately track an increasing AGC detector voltage up to approximately 10 V (+ 20 dB from the 1 V reference) and down to approximately 100 mV (-20 dB from the 1 V reference).

Since U5D is an inverting amplifier, its output voltage is the negative logarithm of the input voltage. Therefore, the output of U5D becomes more negative as the IF signal strength increases and more positive as it decreases. U5C provides a controlled current sink for transistor pair U4. The output of the log amplifier is the logarithm of the ratio of the current through R41 to the current through R46 and R47. R46 is the null adjustment for the log amplifier, it also sets the IF output signal level.

3.4.2 Absolute Value Amplifier and Pulse Width Modulator

The output of the log amplifier is applied to absolute value amplifier U12B and U12A. When the log amplifier output voltage is negative, CR6 and CR7 block the output of U12B so that no current flows through R53. Therefore, the only current path is through R49 and feedback resistor R50 making the output of U12A inverted and proportional to the log amplifier output.

When the log amplifier output voltage is positive, CR6 is biased off and current flows through CR7 and R53. R53 and R49 are scaled so that twice as much current flows through R53. The sum of the currents through the two resistors affect inverting amplifier U12A and feedback resistor R50 so that its output is proportional to the log amplifier output.

The absolute value output controls the duty cycle of pulse width modulator U6. The duty cycle varies from 0 to approximately 100% for a ± 0 to ± 1 volt input to the absolute value amplifier. For signal excursions in excess of + 14 dB, U2A bypasses the log amplifier and immediately drives the absolute value amplifier to maximum. When the output of comparator U12C is high, U6 switches U9D off and on (via U7A) to fill the charge pump. When the output of U12C is low, U6 switches U9B on and off (via U8A) to empty the charge pump. If medium or fast AGC is selected, U9B and U9C are switched in parallel.

The pulse width modulation is shut down when the current sense input (pin 6) is high. This occurs when one-shot timer U10A is active or when either the AGC off or AGC dump lines are high.

3.4.3 Comparator and One-shot Timer

U12C functions as a comparator with hysteresis. Resistors R56 and R57 set the upper and lower thresholds of the dead zone at approximately 10 mV and -10 mV. This means that the log amplifier output voltage must fall below -10 mV for the comparator output to change from low to high. Likewise, the log amplifier output must rise above 10 mV for the comparator to change from high to low. The comparator output state determines whether the charge pump will charge or discharge.

U2B also functions as a comparator. Its hysteresis thresholds are set to only respond to a rising voltage corresponding to a fall in the RF input signal of more than 6 dB. This comparator senses rapid consecutive drops in the RF input signal which do not trip comparator U12C. The outputs of U2B and U12C are differentiated and summed together.

One-shot timer U10A is activated by a falling-edge trigger from comparator U12C or U2B. The period of the timer is established by the resistance placed in series with capacitor C32. When slow AGC is selected, analog switches U14C and U14D are both open and C32 charges through R58 to produce a 2.7 second time constant. When medium AGC is commanded, switch U14D is closed, R125 is placed in parallel with R58, and the time

constant is reduced to 170 ms. When fast AGC is commanded, switch U14C is closed, R124 is placed in parallel with with R58, and the time constant is reduced to less than 15 ms. The one-shot timer output determines the hang time of the AGC system.

The outputs of the timer and comparator U12C are applied to NOR gate U8B. When the timer is active, the output of U8B goes high to shut down the pulse width modulator via the current sense input.

3.4.4 AGC Charge Pump

Analog switches U9A, U9B, U9C, and U9D control the operation of the charge pump in response to the output of the pulse width modulator. When an increase in AGC voltage is required, U9D is closed to allow C40 and C41 to charge through R117. To reduce the AGC voltage, U9B is closed to allow C40 to discharge through R64. If the medium or fast AGC decay characteristic is selected, R63 is connected in parallel with R64 via U9C. In the special data mode, C41 is switched out of the circuit to achieve the desired AGC attack and decay times. The operation of switches U9A through U9D is summarized in table 2.

Table 2. AGC Charge Pump Control Truth Table

Mode	U9A	U9B	U9C	U9D
Slow	1	X	1	X
Medium	1	X*	X*	X
Fast	1	X*	X*	X
Data	0	X*	X*	X

0 = Disabled (off)
1 = Enabled (on)
X = Switched in and out by pulse width modulator.
* = U9B and U9C operate in parallel in these modes

When either AGC OFF or AGC DUMP is commanded, Q8 is turned on to provide a low impedance discharge path to ground for C40 and C41.

3.4.5 AGC Source Selection and Curve Shaping

There are four sources of AGC level control: the charge pump voltage, external AGC, RF gain, and AGC Threshold (R167). AGC source selection is made by an ideal diode OR circuit consisting of U18A through U18D and CR10 through CR13. In this circuit, the AGC source with the highest voltage will dominate and shut the other sources off. In normal operation,the source is the internal AGC voltage (charge pump level), and as a consequence, the voltages at TP4 and TP5 should agree. The ISB AGC output is routed to Audio Assembly A5 via J5-2 for RF AGC processing.

The output of the diode or circuit is applied to curve generator U19A/U19B and the BITE and metering circuits. The ISB AGC voltage is available at rear panel connectors J7-29 and TB1-5. This output voltage ranges from 0 to + 6 Vdc, which corresponds to a 120 dB control range for the entire radio.

Since the Receiver AGC is a composite of the IF AGC and the RF AGC, a scaling factor must be introduced before applying the control voltage to the IF antilog amplifier. The slope of control curve generator U19A/U19B is fixed so that the IF AGC exercises primary control from the threshold of sensitivity to the approximately -50 dBm of RF input. Above this threshold, CR9 changes the scale factor so that there is less drive to the IF antilog circuit. This action reduces the IF AGC level to compensate for the increased RF AGC contribution.

3.4.6 Antilogarithmic Amplifier and PIN Diode Attenuator

The output voltage of the IF curve generator is applied to the antilog amplifier where it can exercise a 90-dB dynamic control range over the IF stage. This control voltage is applied to pin 6 of transistor pair U3. U5A and U3 function as a current sink so that the current through R12 remains constant. The current through R10 is logarithmically related to the control voltage. The collector current through current driver Q1 controls the operation of the PIN diode attenuator circuit.

PIN diodes CR1 and CR2 provide attenuation at the input of the first IF stage. PIN diodes CR5 and CR8 on Q11 and Q2 emitters establish the maximum gain of the IF circuit. The PIN diode attenuator operates on the principle that the forward RF resistance of the diode increases as the current through the diode decreases. In other words, as the AGC control voltage increases, the diode current (collector current of Q1) decreases, the diode forward resistance increases, and the IF gain is reduced.

4. MAINTENANCE

There are no routine maintenance adjustments for this assembly. All boards are made for direct replacement without adjustment. If components are replaced or if the operation of the assembly is in question, proceed with the following setup adjustments in the order shown.

4.1 IF Level Adjustment

R46 is the IF level adjustment. Proceed as follows:

a. Connect an RF signal generator to the Receiver RF input (rear panel connector J1).

b. Make sure that the AGC is operating in the FAST mode.

c. Set the signal generator output to 10 mV at the Receiver ISB operating frequency.

d. Connect an RF voltmeter to the receiver IF output (rear panel connector J3) and adjust R46 on the A18 Assembly for -6 dBm (112 mV_{rms} into 50 ohms) at this calibration setup point.

4.2 R5 Adjustment, IF AGC Gain Set

a. Tune the Receiver to 10.000 MHz, select the USB mode, and set the AGC to FAST.

b. Set the front panel meter to read the LSB RF signal level.

c. Set the signal generator to output a 9.999 MHz, 10 microvolt signal.

d. Turn A18R67 fully counterclockwise.

e. Measure the Dc voltage at A18TP5.

f. Adjust A18R5 until 1.375 V ± 25 mV is measured at TP5.

g. The front panel meter should read 10 microvolts (± a needle width).

4.3 R67 Adjustment, AGC 1 dB Compression Point

a. Set the signal generator output level to 1 microvolt.

b. Use the front panel or external meter to monitor the LSB line audio.

c. Note the USB line audio level with the AGC on.

d. Turn the AGC OFF and turn the RF GAIN control fully clockwise.

e. Adjust A18R67 until the USB audio level is 1 dB greater than it was when the AGC was on.

f. Turn the AGC back ON.

g. To check the AGC flatness, note the USB line audio level and increase the signal generator output level by 100 dB. The line level should increase by no more than 3 dB.

4.4 Distortion Trim Adjustment

R128 is the line amplifier distortion trim adjustment. Proceed as follows:

a. With a signal generator connected as in paragraph 4.1, set up for single-tone operation.

b. Connect a distortion analyzer to the line audio output and adjust A18R128 for minimum distortion at + 10 dBm output.

4.5 R194 Adjust, Dead Zone

Test Equipment required:

- RF signal generator Hewlett Packard HP8640 or equivalent
- Square wave source (1 to 5 V_{p-p}, 5 to 10 Hz output).
- Tektronix 465B oscilloscope or equivalent.

a. Connect the square wave source to the RF generator's external AM input using the DC mode if possible. Adjust the levels as required to produce modulation depth of 30 to 40 dB. Adjust the RF generator so that the peak output is -10 dBm ± 5 dB.

b. Tune the receiver to 10.000 MHz, select the LSB mode and set the AGC to FAST.

c. Set the signal generator to deliver a 9.999 MHz signal.

d. Monitor A18U5 pin 14 with the oscilloscope.

e. Adjust A18R140 so that the separation between the attack and decay waveforms is 60 mV ± 5 mV, see figure 2.

f. Disconnect the test equipment, return all cables to their original positions and replace all covers. Perform BITE testing from the front panel.

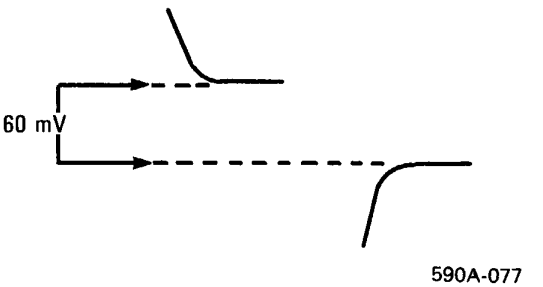


Figure 2. Dead Zone Adjustment Waveform

5. PARTS LIST, COMPONENT LOCATIONS, AND SCHEMATIC DIAGRAM

Table 3 is the parts list for ISB IF/Audio Assembly A18. Refer to figure 3 for component locations. Figure 4 is the schematic diagram for ISB IF/Audio Assembly A18.

Table 3. A18 ISB IF/Audio Assembly (Part No. 10215-6300, Rev. K/-6300-02, Rev. C) Parts List

Ref. Desig.	Part Number	Description
C1	M39014/02-1298	CAP .01UF 10% 200V CER-R
C2	M39014/02-1310	CAP .1UF 10% 100V CER-R
C3	M39014/02-1310	CAP .1UF 10% 100V CER-R
C4	M39014/02-1310	CAP .1UF 10% 100V CER-R
C5	M39014/02-1310	CAP .1UF 10% 100V CER-R
C6	M39014/02-1310	CAP .1UF 10% 100V CER-R
C7	M39014/02-1310	CAP .1UF 10% 100V CER-R
C8	C26-0025-100	CAP 10UF 20% 25V TANT
C9	C26-0025-100	CAP 10UF 20% 25V TANT
C10	M39014/02-1310	CAP .1UF 10% 100V CER-R
C11	M39014/02-1310	CAP .1UF 10% 100V CER-R
C12	M39014/02-1310	CAP .1UF 10% 100V CER-R
C13	M39014/02-1310	CAP .1UF 10% 100V CER-R
C14	CK05BX102K	CAP 1000PF 10% 200V CER
C15	CK05BX101K	CAP 100PF 10% 200V CER
C16	M39014/02-1310	CAP .1UF 10% 100V CER-R
C17	M39014/02-1298	CAP .01UF 10% 200V CER-R
C18	M39014/02-1310	CAP .1UF 10% 100V CER-R
C19	CK05BX471K	CAP 470PF 10% 200V CER
C20	C26-0025-100	CAP 10UF 20% 25V TANT
C21	M39014/02-1298	CAP .01UF 10% 200V CER-R
C22	M39014/02-1310	CAP .1UF 10% 100V CER-R
C23	M39014/02-1298	CAP .01UF 10% 200V CER-R
C24	M39014/02-1298	CAP .01UF 10% 200V CER-R
C25	M39014/02-1298	CAP .01UF 10% 200V CER-R
C26	M39014/02-1298	CAP .01UF 10% 200V CER-R
C27	CK05BX221K	CAP 220PF 10% 200V CER
C28	CK05BX221K	CAP 220PF 10% 200V CER
C29	C26-0025-100	CAP 10UF 20% 25V TANT
C30	C26-0025-339	CAP 3.3UF 20% 25V TANT
C31	M39014/02-1310	CAP .1UF 10% 100V CER-R
C32	C26-0025-339	CAP 3.3UF 20% 25V TANT
C34	M39014/02-1310	CAP .1UF 10% 100V CER-R
C35	C26-0050-109	CAP 1.0UF 20% 50V TANT
C36	C26-0035-100	CAP 10UF 20% 35V TANT
C37	C26-0050-109	CAP 1.0UF 20% 50V TANT
C38	C26-0050-109	CAP 1.0UF 20% 50V TANT
C39	C26-0035-100	CAP 10UF 20% 35V TANT
C40	C61-0001-004	CAP .22UF 5% 100V POLYE
C41	C61-0001-005	CAP .33UF 5% 100V POLYE
C42	M39014/02-1310	CAP .1UF 10% 100V CER-R
C43	M39014/02-1310	CAP .1UF 10% 100V CER-R
C44	CK06BX472K	CAP 4700PF 10% 200V CER
C45	CK06BX472K	CAP 4700PF 10% 200V CER
C46	CK05BX101K	CAP 100PF 10% 200V CER
C47	M39014/02-1310	CAP .1UF 10% 100V CER-R
C48	C26-0025-339	CAP 3.3UF 20% 25V TANT

Table 3. A18 ISB IF/Audio Assembly (Part No. 10215-6300, Rev. K/-6300-02, Rev. C) Parts List (Cont.)

Ref. Desig.	Part Number	Description
C50	C26-0025-339	CAP 3.3UF 20% 25V TANT
C51	M39014/02-1298	CAP .01UF 10% 200V CER-R
C52	CK06BX222K	CAP 2200PF 10% 200V CER
C53	M39014/02-1310	CAP .1UF 10% 100V CER-R
C54	C26-0050-109	CAP 1.0UF 20% 50V TANT
C55	M39014/02-1310	CAP .1UF 10% 100V CER-R
C56	M39014/02-1310	CAP .1UF 10% 100V CER-R
C57	M39014/02-1310	CAP .1UF 10% 100V CER-R
C58	M39014/02-1310	CAP .1UF 10% 100V CER-R
C59	M39014/02-1310	CAP .1UF 10% 100V CER-R
C60	CK05BX102K	CAP 1000PF 10% 200V CER
C61	CK05BX221K	CAP 220PF 10% 200V CER
C62	CK05BX471K	CAP 470PF 10% 200V CER
C63	M39014/02-1310	CAP .1UF 10% 100V CER-R
C64	M39014/02-1310	CAP .1UF 10% 100V CER-R
C65	M39014/02-1298	CAP .01UF 10% 200V CER-R
C66	M39014/02-1298	CAP .01UF 10% 200V CER-R
C67	M39014/02-1310	CAP .1UF 10% 100V CER-R
C68	M39014/02-1310	CAP .1UF 10% 100V CER-R
C69	CK05BX471K	CAP 470PF 10% 200V CER
CR1	D12-0007-001	DIODE PIN ATTN 1W 9301
CR2	D12-0007-001	DIODE PIN ATTN 1W 9301
CR3	1N4454	DIODE 200MA 75V SW
CR4	1N4454	DIODE 200MA 75V SW
CR5	D12-0007-001	DIODE PIN ATTN 1W 9301
CR6	1N4454	DIODE 200MA 75V SW
CR7	1N4454	DIODE 200MA 75V SW
CR8	D12-0007-001	DIODE PIN ATTN 1W 9301
CR9	1N4454	DIODE 200MA 75V SW
CR10	1N4454	DIODE 200MA 75V SW
CR11	1N4454	DIODE 200MA 75V SW
CR12	1N4454	DIODE 200MA 75V SW
CR13	1N4454	DIODE 200MA 75V SW
CR14	1N4454	DIODE 200MA 75V SW
CR15	1N4454	DIODE 200MA 75V SW
CR16	1N4454	DIODE 200MA 75V SW
CR17	1N4454	DIODE 200MA 75V SW
CR18	1N4454	DIODE 200MA 75V SW
CR19	1N4454	DIODE 200MA 75V SW
CR20	1N4454	DIODE 200MA 75V SW
CR21	1N4454	DIODE 200MA 75V SW
CR22	1N4454	DIODE 200MA 75V SW
CR23	1N4454	DIODE 200MA 75V SW
CR24	1N4454	DIODE 200MA 75V SW
CR25	1N4454	DIODE 200MA 75V SW
CR26	1N4454	DIODE 200MA 75V SW
CR27	1N4454	DIODE 200MA 75V SW
CR28	1N4454	DIODE 200MA 75V SW

Table 3. A18 ISB IF/Audio Assembly (Part No. 10215-6300, Rev. K/-6300-02, Rev. C) Parts List (Cont.)

Ref. Desig.	Part Number	Description
CR29	1N4454	DIODE 200MA 75V SW
CR30	1N4454	DIODE 200MA 75V SW
CR31	1N4454	DIODE 200MA 75V SW
FL1	G25-0003-003	CER FILTER 455KHZ 10KHZBW
J1	J-0031	CONN SMB VERT PCB F
J2	J-0031	CONN SMB VERT PCB F
J3	J-0031	CONN SMB VERT PCB F
J4	J46-0022-010	HDR 10 PIN 0.100" SR LKG
J5	J46-0022-010	HDR 10 PIN 0.100" SR LKG
J6	J46-0022-008	HDR 8 PIN 0.100" SR LKG
JMP1	MP-1142	RES ZERO OHM (CKT JMPR)
JMP2	MP-1142	RES ZERO OHM (CKT JMPR)
L1	MS75085-15	COIL 470UH 10% FXD RF
L2	MS75085-15	COIL 470UH 10% FXD RF
L3	MS75085-15	COIL 470UH 10% FXD RF
L4	MS75085-15	COIL 470UH 10% FXD RF
L5	MS75085-15	COIL 470UH 10% FXD RF
L6	MS75089-21	COIL 680UH 10% FXD RF
L7	MS75084-14	COIL 15.0UH 10% FXD RF
L8	MS75084-14	COIL 15.0UH 10% FXD RF
Q1	2N4403	XSTR SS/GP PNP TO-92
Q2	2N4401	XSTR SS/GP NPN TO-92
Q3	2N4401	XSTR SS/GP NPN TO-92
Q4	2N4403	XSTR SS/GP PNP TO-92
Q5	2N4401	XSTR SS/GP NPN TO-92
Q6	2N4401	XSTR SS/GP NPN TO-92
Q7	2N4401	XSTR SS/GP NPN TO-92
Q8	2N4401	XSTR SS/GP NPN TO-92
Q10	Q35-0003-000	XSTR N-CH JFET U310
Q11	2N4403	XSTR SS/GP PNP TO-92
Q12	2N4401	XSTR SS/GP NPN TO-92
R1	R65-0003-151	RES 150 5% 1/4W CAR FILM
R2	R65-0003-151	RES 150 5% 1/4W CAR FILM
R3	R65-0003-151	RES 150 5% 1/4W CAR FILM
R4	R65-0003-182	RES 1.8K 5% 1/4W CAR FILM
R5	R-2204	RES VAR 200 10% .5W HOR.
R6	R65-0003-751	RES 750 5% 1/4W CAR FILM
R7	R65-0003-332	RES 3.3K 5% 1/4W CAR FILM
R8	R65-0003-101	RES 100 5% 1/4W CAR FILM
R10	RN55D3922F	RES 39.2K 1% 1/8W MET FLM
R11	R65-0003-223	RES 22K 5% 1/4W CAR FILM
R12	RN55D1003F	RES 100K 1% 1/8W MET FLM
R13	R65-0003-202	RES 2.0K 5% 1/4W CAR FILM
R14	RN55D3162F	RES 31.6K 1% 1/8W MET FLM
R15	RN55D1001F	RES 1000 1% 1/8W MET FLM
R16	D40-0004-003	THERM 1K 5% @ 25DEG
R17	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R18	R65-0003-561	RES 560 5% 1/4W CAR FILM

Table 3. A18 ISB IF/Audio Assembly (Part No. 10215-6300, Rev. K/-6300-02, Rev. C) Parts List (Cont.)

Ref. Desig.	Part Number	Description
R19	R65-0003-562	RES 5.6K 5% 1/4W CAR FILM
R20	R65-0003-270	RES 27 5% 1/4W CAR FILM
R21	R65-0003-391	RES 390 5% 1/4W CAR FILM
R22	R65-0003-242	RES 2.4K 5% 1/4W CAR FILM
R23	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R24	R65-0003-152	RES 1.5K 5% 1/4W CAR FILM
R25	R65-0003-152	RES 1.5K 5% 1/4W CAR FILM
R26	R65-0003-561	RES 560 5% 1/4W CAR FILM
R27	R65-0003-561	RES 560 5% 1/4W CAR FILM
R28	R65-0003-561	RES 560 5% 1/4W CAR FILM
R29	R65-0003-152	RES 1.5K 5% 1/4W CAR FILM
R30	R65-0003-203	RES 20K 5% 1/4W CAR FILM
R31	R65-0003-152	RES 1.5K 5% 1/4W CAR FILM
R32	R65-0003-821	RES 820 5% 1/4W CAR FILM
R33	R65-0003-470	RES 47 5% 1/4W CAR FILM
R34	R65-0003-821	RES 820 5% 1/4W CAR FILM
R35	R65-0003-154	RES 150K 5% 1/4W CAR FILM
R36	R65-0003-223	RES 22K 5% 1/4W CAR FILM
R37	R65-0003-562	RES 5.6K 5% 1/4W CAR FILM
R38	R65-0003-222	RES 2.2K 5% 1/4W CAR FILM
R39	R65-0003-622	RES 6.2K 5% 1/4W CAR FILM
R40	R65-0003-752	RES 7.5K 5% 1/4W CAR FILM
R41	RN55D2002F	RES 20.0K 1% 1/8W MET FLM
R42	R65-0003-202	RES 2.0K 5% 1/4W CAR FILM
R43	RN55D3162F	RES 31.6K 1% 1/8W MET FLM
R44	RN55D1001F	RES 1000 1% 1/8W MET FLM
R45	D40-0004-003	THERM 1K 5% @ 25DEG
R46	R30-0008-104	RES VAR PCB 100K 1/2W 10%
R47	R65-0003-104	RES 100K 5% 1/4W CAR FILM
R48	RN55D8062F	RES 80.6K 1% 1/8W MET FLM
R49	RN55D2002F	RES 20.0K 1% 1/8W MET FLM
R50	RN55D8062F	RES 80.6K 1% 1/8W MET FLM
R51	RN55D2002F	RES 20.0K 1% 1/8W MET FLM
R52	RN55D2002F	RES 20.0K 1% 1/8W MET FLM
R53	RN55D1002F	RES 10.0K 1% 1/8W MET FLM
R54	R65-0003-203	RES 20K 5% 1/4W CAR FILM
R55	R65-0003-473	RES 47K 5% 1/4W CAR FILM
R56	R65-0003-394	RES 390K 5% 1/4W CAR FILM
R57	R65-0003-221	RES 220 5% 1/4W CAR FILM
R58	R65-0003-824	RES 820K 5% 1/4W CAR FILM
R59	R65-0003-562	RES 5.6K 5% 1/4W CAR FILM
R60	R65-0003-301	RES 300 5% 1/4W CAR FILM
R61	R65-0003-181	RES 180 5% 1/4W CAR FILM
R62	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R63	R65-0003-104	RES 100K 5% 1/4W CAR FILM
R64	R65-0003-515	RES 5.1M 5% 1/4W CAR FILM
R65	R65-0003-101	RES 100 5% 1/4W CAR FILM
R66	R65-0003-153	RES 15K 5% 1/4W CAR FILM

Table 3. A18 ISB IF/Audio Assembly (Part No. 10215-6300, Rev. K/-6300-02, Rev. C) Parts List (Cont.)

Ref. Desig.	Part Number	Description
R67	R-2207	RES VAR 2K 10% .5W HOR.
R68	R65-0003-242	RES 2.4K 5% 1/4W CAR FILM
R69	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R70	R65-0003-201	RES 200 5% 1/4W CAR FILM
R71	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R72	R65-0003-100	RES 10 5% 1/4W CAR FILM
R73	R65-0003-222	RES 2.2K 5% 1/4W CAR FILM
R74	R65-0003-680	RES 68 5% 1/4W CAR FILM
R75	R65-0003-680	RES 68 5% 1/4W CAR FILM
R76	R65-0003-682	RES 6.8K 5% 1/4W CAR FILM
R77	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R78	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R79	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R80	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R81	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R82	R65-0003-104	RES 100K 5% 1/4W CAR FILM
R83	R65-0003-104	RES 100K 5% 1/4W CAR FILM
R84	R65-0003-104	RES 100K 5% 1/4W CAR FILM
R85	R65-0003-104	RES 100K 5% 1/4W CAR FILM
R86	R65-0003-104	RES 100K 5% 1/4W CAR FILM
R87	R65-0003-114	RES 110K 5% 1/4W CAR FILM
R88	R65-0003-822	RES 8.2K 5% 1/4W CAR FILM
R89	R65-0003-392	RES 3.9K 5% 1/4W CAR FILM
R90	R65-0003-392	RES 3.9K 5% 1/4W CAR FILM
R91	R65-0003-154	RES 150K 5% 1/4W CAR FILM
R92	R65-0003-154	RES 150K 5% 1/4W CAR FILM
R93	R65-0003-203	RES 20K 5% 1/4W CAR FILM
R94	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R95	R65-0003-821	RES 820 5% 1/4W CAR FILM
R97	R65-0003-431	RES 430 5% 1/4W CAR FILM
R98	R65-0003-104	RES 100K 5% 1/4W CAR FILM
R99	R65-0003-104	RES 100K 5% 1/4W CAR FILM
R100	R65-0003-473	RES 47K 5% 1/4W CAR FILM
R101	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R102	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R103	R65-0003-512	RES 5.1K 5% 1/4W CAR FILM
R104	R65-0003-182	RES 1.8K 5% 1/4W CAR FILM
R105	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R106	R65-0003-104	RES 100K 5% 1/4W CAR FILM
R107	R65-0003-114	RES 110K 5% 1/4W CAR FILM
R108	R65-0003-333	RES 33K 5% 1/4W CAR FILM
R109	R65-0003-153	RES 15K 5% 1/4W CAR FILM
R110	R65-0003-152	RES 1.5K 5% 1/4W CAR FILM
R111	R65-0003-184	RES 180K 5% 1/4W CAR FILM
R112	R65-0004-330	RES 33 5% 1/2W CAR FILM
R113	R65-0003-273	RES 27K 5% 1/4W CAR FILM
R114	R65-0003-273	RES 27K 5% 1/4W CAR FILM
R115	R65-0003-333	RES 33K 5% 1/4W CAR FILM

Table 3. A18 ISB IF/Audio Assembly (Part No. 10215-6300, Rev. K/-6300-02, Rev. C) Parts List (Cont.)

Ref. Desig.	Part Number	Description
R116	R65-0003-470	RES 47 5% 1/4W CAR FILM
R117	RN55D8062F	RES 80.6K 1% 1/8W MET FLM
R118	R50-0010-473	RES 47K 2% 10SIP 9RES
R119	R65-0003-513	RES 51K 5% 1/4W CAR FILM
R121	R65-0003-473	RES 47K 5% 1/4W CAR FILM
R122	R65-0003-101	RES 100 5% 1/4W CAR FILM
R123	R65-0003-101	RES 100 5% 1/4W CAR FILM
R124	R65-0003-392	RES 3.9K 5% 1/4W CAR FILM
R125	R65-0003-563	RES 56K 5% 1/4W CAR FILM
R126	R65-0003-560	RES 56 5% 1/4W CAR FILM
R127	R65-0003-683	RES 68K 5% 1/4W CAR FILM
R128	R-2211	RES VAR 25K 10% .5W HOR.
R129	R65-0003-682	RES 6.8K 5% 1/4W CAR FILM
R130	R65-0003-473	RES 47K 5% 1/4W CAR FILM
R131	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R132	R65-0004-151	RES 150 5% 1/2W CAR FILM
R133	R65-0004-151	RES 150 5% 1/2W CAR FILM
R134	R65-0003-222	RES 2.2K 5% 1/4W CAR FILM
R135	R65-0003-331	RES 330 5% 1/4W CAR FILM
R136	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R137	R65-0003-754	RES 750K 5% 1/4W CAR FILM
R137	R65-0003-754	RES 750K 5% 1/4W CAR FILM
R138	R65-0003-104	RES 100K 5% 1/4W CAR FILM
R139	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R140	R-2205	RES VAR 500 10% .5W HOR.
R141	R65-0003-184	RES 180K 5% 1/4W CAR FILM
R142	R65-0003-392	RES 3.9K 5% 1/4W CAR FILM
R143	R65-0003-474	RES 470K 5% 1/4W CAR FILM
R144	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R145	R65-0003-153	RES 15K 5% 1/4W CAR FILM
R146	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R147	R65-0003-223	RES 22K 5% 1/4W CAR FILM
R148	R65-0003-123	RES 12K 5% 1/4W CAR FILM
R149	R65-0003-333	RES 33K 5% 1/4W CAR FILM
R150	R65-0003-333	RES 33K 5% 1/4W CAR FILM
R151	R65-0003-101	RES 100 5% 1/4W CAR FILM
R152	R65-0003-560	RES 56 5% 1/4W CAR FILM
T2	10085-5012	BALUN RF/IF
T3	10085-5012	BALUN RF/IF
TP0	J46-0047-001	HDR 1 POSITION
TP1	J46-0047-001	HDR 1 POSITION
TP2	J46-0047-001	HDR 1 POSITION
TP3	J46-0047-001	HDR 1 POSITION
TP4	J46-0047-001	HDR 1 POSITION
TP5	J46-0047-001	HDR 1 POSITION
TP6	J46-0047-001	HDR 1 POSITION
U2	I30-0035-000	IC OP AMP QUAD 072
U3	I90-0011-002	IC XSTR ARRAY NPN PR 394
U4	I90-0011-002	IC XSTR ARRAY NPN PR 394

Table 3. A18 ISB IF/Audio Assembly (Part No. 10215-6300, Rev. K/-6300-02, Rev. C) Parts List (Cont.)

Ref. Desig.	Part Number	Description
U5	I30-0038-001	IC OP AMP QUAD 347
U6	I14-0001-001	IC PS CONTROLLER 5561
U7	I01-0000-023	IC 4071B PLASTIC CMOS
U8	I01-0000-003	IC 4001B PLASTIC CMOS
U9	I06-0002-001	IC DG211 ANALOG SW QUAD
U10	I01-0000-353	IC 4538B PLASTIC CMOS
U11	I01-0000-021	IC 4069UB PLASTIC CMOS
U12	I30-0038-002	IC OP AMP QUAD 347
U13	I62-0001-000	IC 1496 BAL MODULATOR
U14	I06-0002-001	IC DG211 ANALOG SW QUAD
U15	I30-0038-001	IC OP AMP QUAD 347
U16	I24-0001-000	IC COMPANDOR NE571 PLAS
U18	I30-0003-000	IC OP AMP QUAD 324
U19	I30-0003-000	IC OP AMP QUAD 324
U20	I33-0001-101	IC CURRENT AMP LH0002
VR1	1N5231B	DIODE 5.1V 5% .5W ZENER
VR3	1N5231B	DIODE 5.1V 5% .5W ZENER
VR4	1N5235B	DIODE 6.8V 5% .5W ZENER
VR5	I12-0006-005	IC VR 78L05A +5V .10A 4%
VR6	I12-0006-008	IC VR 78L08A +8V .10A 4%
VR7	I12-0010-005	IC VR 79L05A -5V .10A 4%

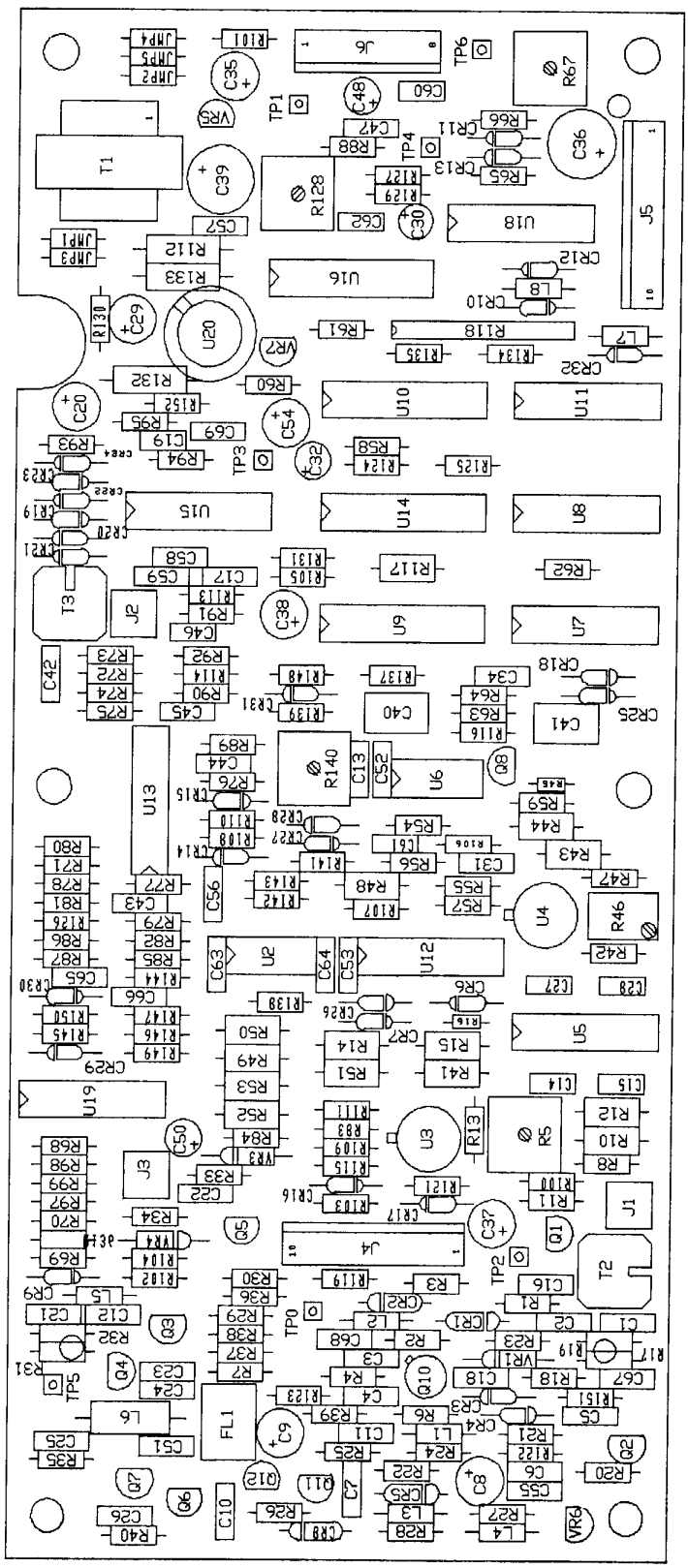


Figure 3. ISB IF/Audio Assembly A18 Component Locations (10215-6300, Rev. G)

NOTE: UNLESS OTHERWISE SPECIFIED:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR A COMPLETE DESIGNATION, PREFIX WITH UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.
2. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, ±5%.
3. ALL CAPACITOR VALUES ARE IN MICROFARADS.
4. VENDOR PART NO. CALLOUTS ARE FOR REFERENCE ONLY. COMPONENTS ARE SUPPLIED PER PART NO. IN PARTS LIST.
5. UNLESS OTHERWISE SPECIFIED ALL DIODE PART NUMBERS ARE IN4454.
6. THIS IS A TABULATED DRAWING SEE SHT 3 FOR -01 AND -02 APPLICATIONS.

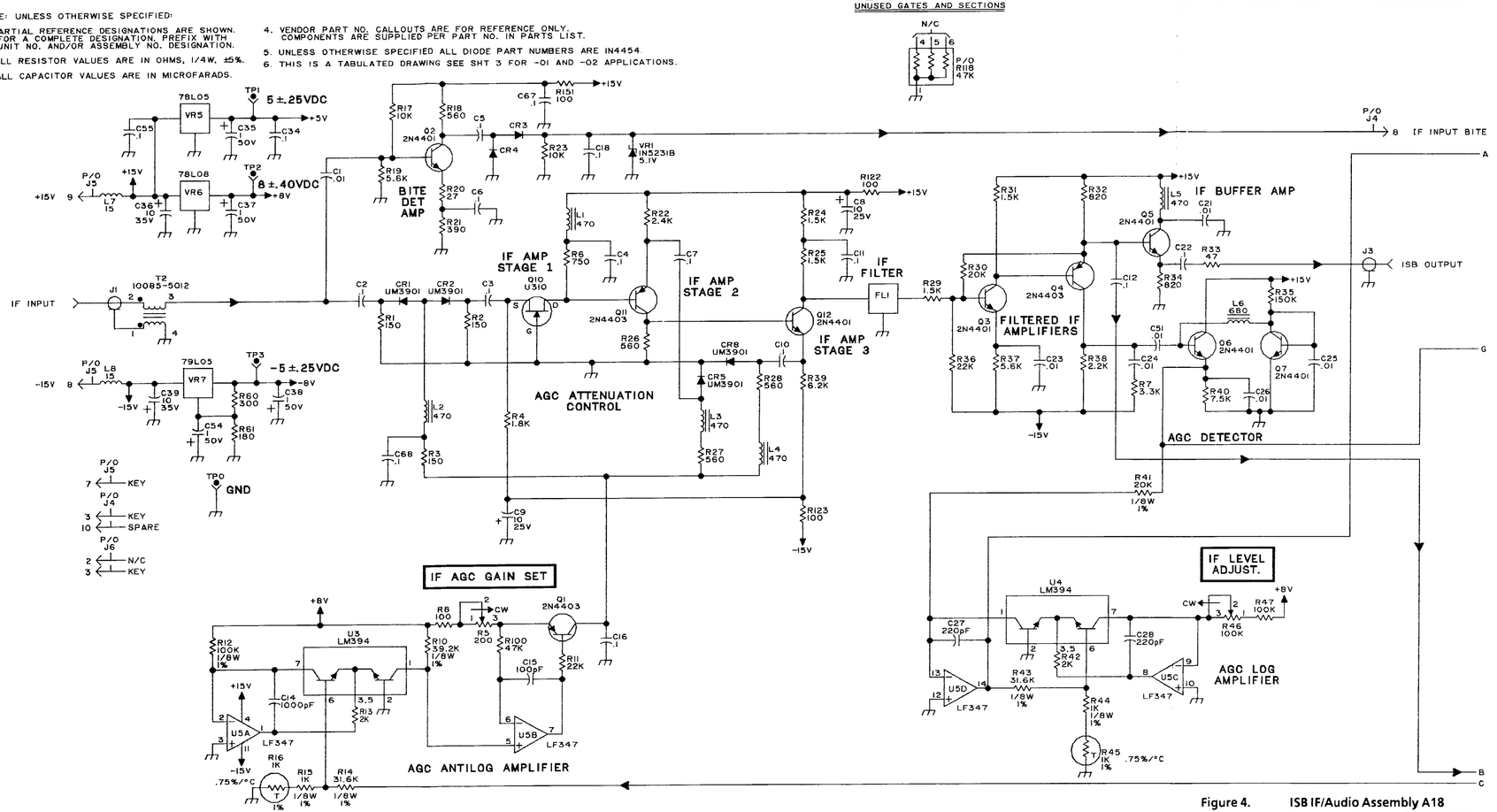


Figure 4. ISB IF/Audio Assembly A18 Schematic Diagram (10215-6301, Rev. L) (Sheet 1 of 3)

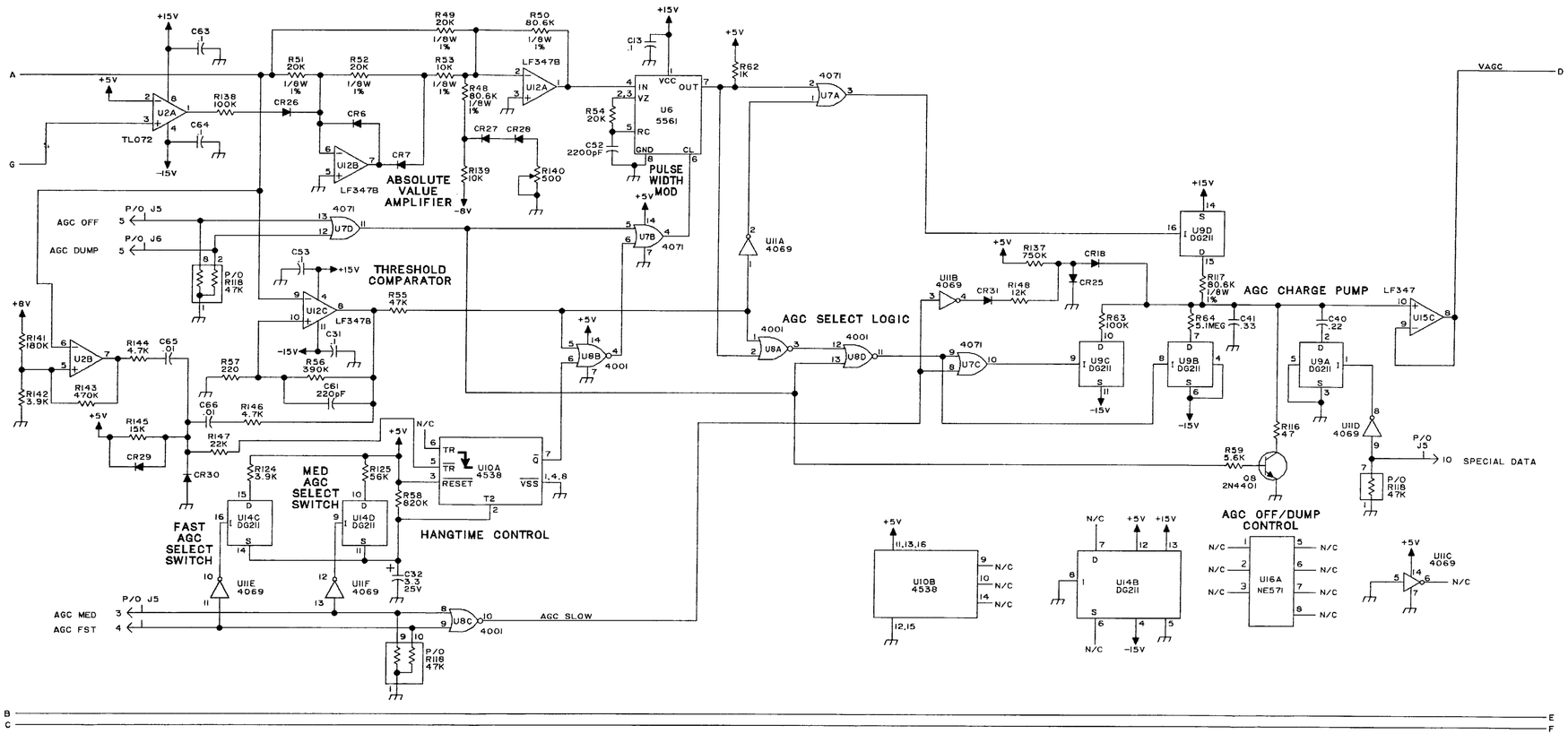
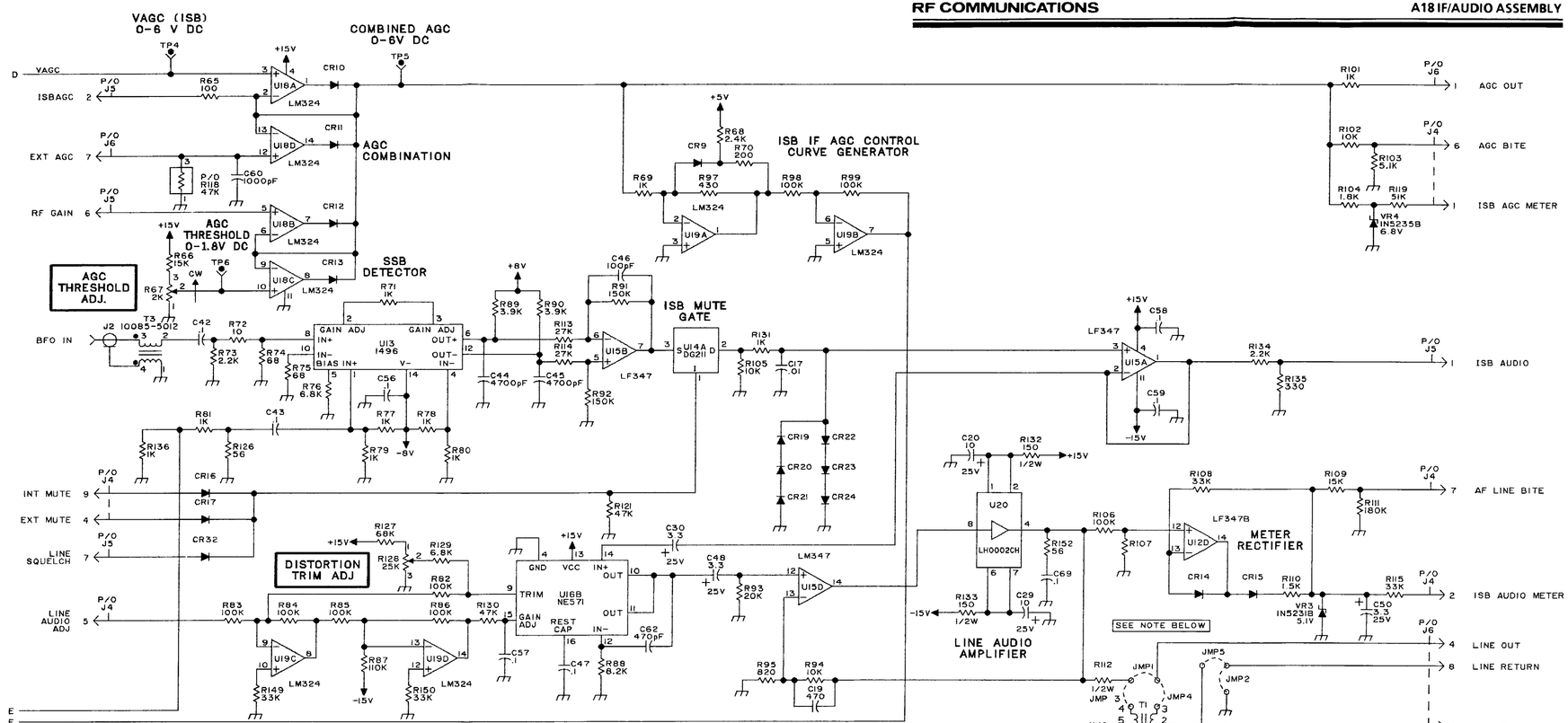


Figure 4. ISB IF/Audio Assembly A18 Schematic Diagram (10215-6301, Rev. L) (Sheet 2 of 3)



NOTE:
USE THE APPROPRIATE TABLE FOR -01, -02, -03, AND -04 APPLICATIONS

REF DES	-01 (+10dBm BALANCED LINE)	-02 (+15dBm UNBALANCED LINE)	-03 (+10dBm BALANCED LINE)	-04 (10215-6930 OPTION)
R107	300K	110K	300K	110K
R112	180 1/2W	33 1/2W	180 1/2W	180 1/2W
T1	INSTALLED	DELETED	INSTALLED	INSTALLED
JMP1	DELETED	INSTALLED	DELETED	DELETED
JMP2	DELETED	INSTALLED	DELETED	DELETED
JMP3	INSTALLED	DELETED	INSTALLED	INSTALLED
JMP4	INSTALLED	DELETED	INSTALLED	INSTALLED
JMP5	INSTALLED	DELETED	INSTALLED	INSTALLED
J5-7	REMOVED (KEY)	REMOVED (KEY)	INSTALLED	REMOVED (KEY)
CR32	DELETED	DELETED	INSTALLED	DELETED

Figure 4. ISB IF/Audio Assembly A18 Schematic Diagram (10215-6301, Rev. L) (Sheet 3 of 3)

HARRIS
RF COMMUNICATIONS

A19
PRESELECTOR ASSEMBLY

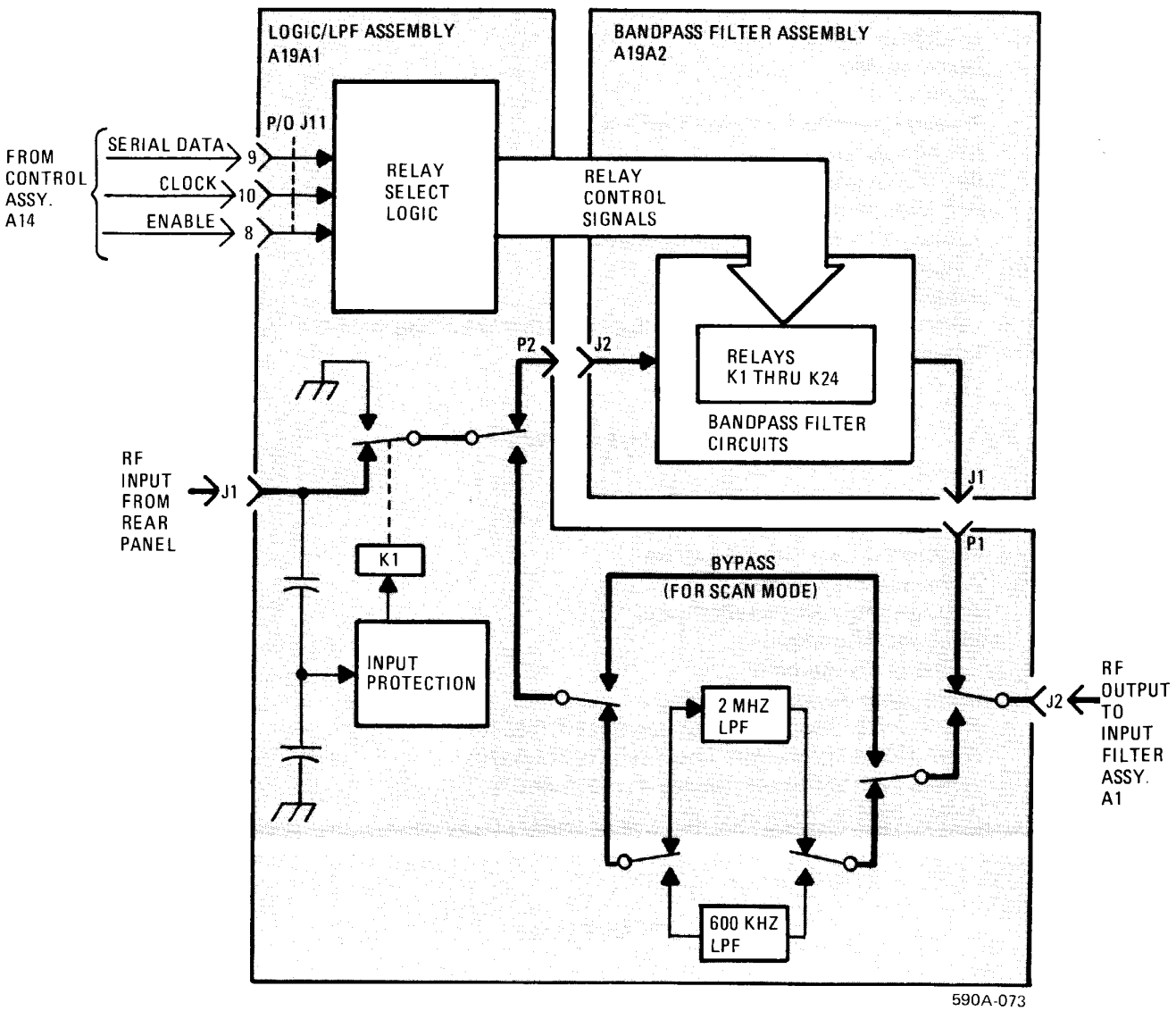


TABLE OF CONTENTS

Paragraph		Page
1	General Description	1
2	Technical Characteristics	2
3	Functional Description	2
3.1	Functional Features	2
3.2	Input Protect Circuit	2
3.3	Filter Control	2
3.4	Bypass	5
3.5	Lowpass Filter Operation	5
3.6	Relay Control	5
3.7	Bandpass Filter	5
4	Maintenance	5
4.1	Troubleshooting	5
4.2	Replacement	5
5	Alignment	6
5.1	Prealignment Performance Checks	6
5.1.1	BYPASS Check	6
5.1.2	BPF/LPF Checks	6
5.2	BPF Alignment	6
5.2.1	Required Tools and Test Equipment	6
5.2.2	Alignment Test Setup	7
5.2.3	Alignment Procedure	7
6	Parts List and Component Location and Schematic Diagrams	11
7	Schematic Drawings	11

LIST OF FIGURES

Figure		Page
1	Preselector Functional Diagram	3
2	A19 Assembly Test Setup	7
3	A19 Assembly Alignment Points	8
4	Passband Alignment	9
5	2 MHz LPF Alignment	10
6	Preselector Assembly Drawing	16
7	A19A1 PWB Component Locations (10215-6660)	17
8	A19A2 PWB Component Locations (10215-6670)	18
9	A19A1 PWB Schematic Diagram (10215-6661)	19
10	A19A2 PWB Schematic Diagram (10215-6671)	23

LIST OF TABLES

Table		Page
1	Preselector Assembly A19 Interface Summary	1
2	Alignment Specifications	9
3	Preselector Assembly A19A1 (10215-6660) Module Parts List	11
4	Bandpass Filter Assembly A19A2 Parts list (10215-6670)	14

A19 PRESELECTOR ASSEMBLY

1. GENERAL DESCRIPTION

The A19 Assembly is a digitally-tuned bandpass filter used as a preselector module. The preselector provides RF filtering to increase receiver sensitivity. The assembly also provides some input protection for the Receiver.

The Preselector mounts to the receiver chassis over the A2 and A3 assemblies. It is connected directly into the RF signal path at the receiver front end. Preselector cabling and interconnection is shown in the Chassis Interconnect Schematic Diagram and listed in table 1.

Table 1. Preselector Assembly A19 Interface Summary

Connector	Function	To	From
A19A1J1	RF Input	---	J1 Antenna Input
A19A1J2	RF Out	A1J1	---
A19A1J11-1	Noise Blank ID	---	A14J3-1
A19A1J11-2	Filter ID	---	A14J3-2
A19A1J11-3	Ant Overload	---	A14J3-3
A19A1J11-4	N/C	---	---
A19A1J11-5	N/C	---	---
A19A1J11-6	Key	---	---
A19A1J11-7	N/C	---	---
A19A1J11-8	Enable	---	A14J3-8
A19A1J11-9	Data	---	A14J3-9
A19A1J11-10	Clock	---	A14J3-10
A19A1J10-1	+ 8 V Unreg	---	A15J3-15
A19A1J10-2	-15 V	---	A15J3-2
A19A1J10-3	Key	---	---
A19A1J10-4	Gnd	--	A15J3-14
A19A1J10-5	+ 15 V	---	A15J3-1
A19A1J10-6	N/C	--	---

The Preselector assembly includes two PWBs, the Logic/LPF Assembly A19A1, and the Bandpass Filter Assembly A19A2.

2. TECHNICAL CHARACTERISTICS

The Preselector assembly provides the following filter characteristics:

Frequency Range:	
Bandpass Filter (2-29.99 MHz)	Automatically tuned Bandpass Filter provides 20 dB attenuation ± 10% from tuned frequency.
Lowpass Filter (cutoff = 2 MHz)	Provides HF attenuation when receiver is tuned below 2 MHz.
Lowpass Filter (cutoff = 600 kHz)	Provides HF and Broadcast band attenuation when the receiver is tuned below 600 kHz.
Insertion Loss:	
0.6-30 MHz	6 dB, max
<0.6 MHz	4 dB, max
Overload Protection:	5 V_{rms} (in-band) 30 V_{rms} (out-of-band)

3. FUNCTIONAL DESCRIPTION

Refer to the functional diagram shown in figure 1 and to related schematic diagrams, as necessary for the following discussions.

3.1 Functional Features

The tunable bandpass filter contains two, highly-selective, double-tuned, series-resonant filter sections which provide greater than 20 dB overall selectivity at ± 10% from the tuned frequency. The bandpass filter is tuned by switching combinations of coils which make up the resonant circuit.

Lowpass filter is used when the Receiver is tuned to frequencies below 2 MHz. Sets of elliptic lowpass filters are incorporated to accomplish the task.

3.2 Input Protect Circuit

Signal levels above approximately 30 Vrms at the antenna activate a protection circuit that opens the antenna input circuit and grounds the receiver side, protecting internal components. C27 and C28 form a capacitive voltage divider which monitors the RF input. Q1 and CR2 form a buffered peak detector which controls K1, opening up the RF input path for signals greater than 30 Vrms. A similar detector (Q3, CR4) is positioned at the bandpass filter output. This activates at signal levels of 5 Vrms to protect the preselector bandpass filter from high in-band signals. When activated, the module goes into bypass mode, with an RF path that routes directly through the preselector.

3.3 Filter Control

Serial-to-parallel data converters on the A19A1 PWB monitor the frequency data output. The parallel data output from these converters is decoded by PROMS U6 and U7 to control band selection and coil tuning. U7 controls the band select relays, while U6 controls the sections of the resonating coil used to tune the bandpass filter. Prom U7 also controls LPF selection and bypass control.

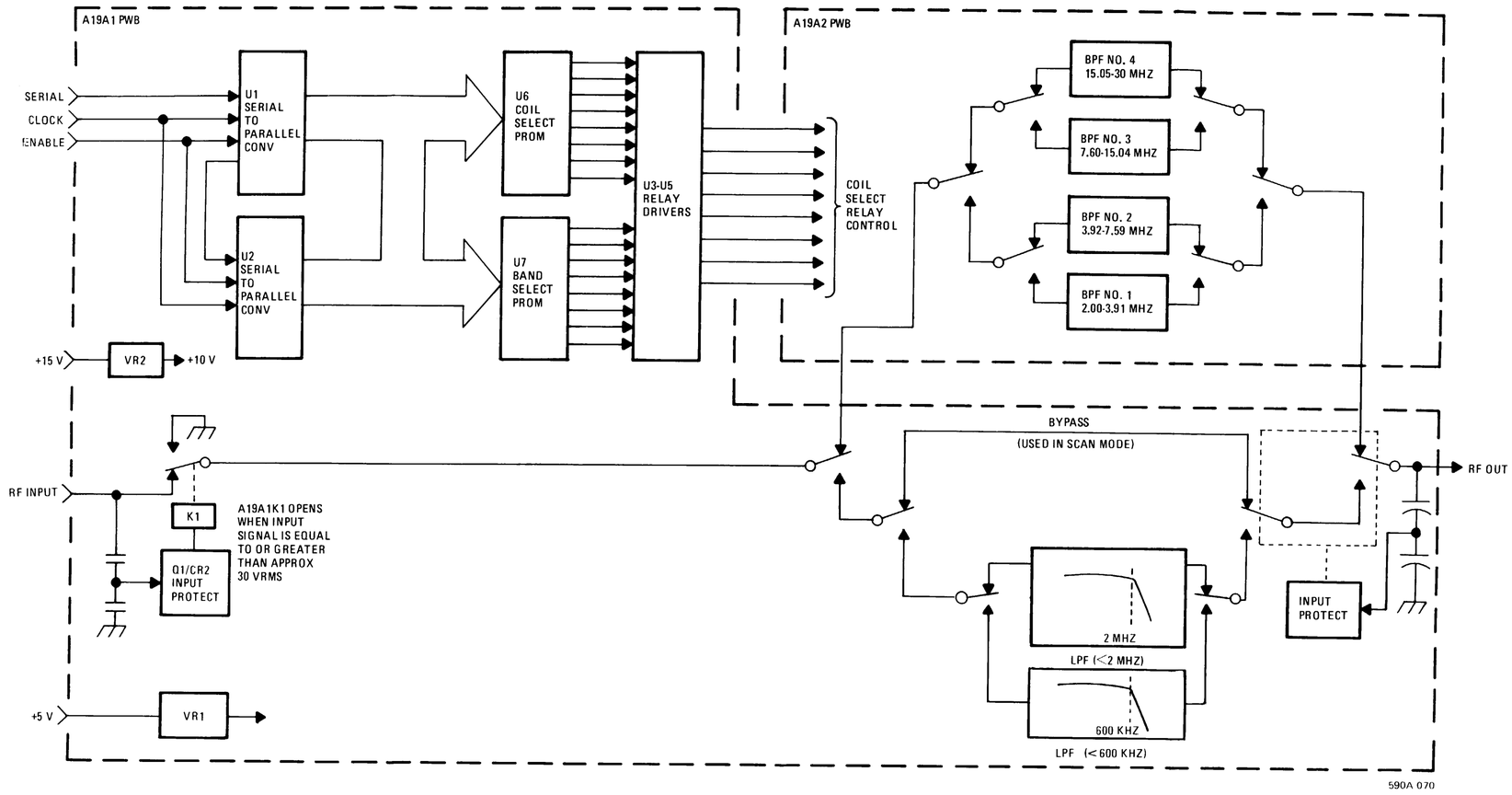


Figure 1. Preselector Functional Diagram

3.4 Bypass

The BYPASS function is automatically selected whenever the Receiver is in the SCAN mode. In the BYPASS mode, the receiver RF input is routed directly through the preselector by relay action, as shown in figure 1.

3.5 Lowpass Filter Operation

A <2 MHz Lowpass filter is activated whenever a receiver frequency between 500 kHz and 1.999 MHz is selected. This filter has a cutoff frequency of approximately 2.0 MHz and has less than 6 dB passband loss. A second lowpass filter with a cutoff at 600 kHz and a bandpass loss of less than 4 dB is selected when the Receiver is tuned to a frequency below 600 kHz.

3.6 Relay Control

The band select relays are organized into functional groups for control purposes. Band control information is shown in an inset on the A19A2 schematic diagram.

3.7 Bandpass Filter

Bandpass filtering is accomplished by a set of double tuned, capacitively coupled, series resonant filters. The bandpass sections have Q compensation provided by shunt capacitors at the filter input and output. This compensation provides a relatively constant loaded Q throughout the tuning band. The resonant coil of each filter section is varied to change the resonant frequency throughout each band. The coil is tuned by relays which short out elements in the coil. This moves the filter passband to the selected frequency. Bands are switched by changing resonant capacitive elements and Q control capacitors. The same resonant coils are used for all bands.

4. MAINTENANCE

There are no routine maintenance requirements for the preselector assembly. Adjustment of the preselector should NEVER be performed as a matter of routine. Refer to paragraph 5, and note that alignment should never be attempted unless reactive components have been changed or disturbed. The preselector is factory-aligned, and should not require realignment in normal service.

4.1 Troubleshooting

Standard troubleshooting procedures can be used to isolate faults. The assembly can be isolated by introducing a signal directly to the module input (A19A1J1) and checking the output at A19A1J2.

All inputs to the preselector are shown in figure 1, and can be tested using conventional and logical procedures. Coil and band-select relay control outputs use low logic levels to control the relays and can also be tested using conventional procedures. Refer to the paragraph on alignment for setup frequencies that will isolate the desired band and coil-select control functions.

4.2 Replacement

The complete preselector, and any of its component subassemblies can be replaced using only a screwdriver. Refer to the assembly drawings for additional detail.

5. ALIGNMENT

The Preselector Assembly has been completely aligned at the factory. The module should never require readjustment in normal service unless reactive components, or related circuit elements are changed.

If the filter does not perform to specification, obtain a complete set of symptoms by checking performance in all bands and modes (BYPASS, BPF-1, BPF-2, BPF-3, BPF-4, LPF). Isolate faults and perform repairs before attempting realignment.

5.1 Prealignment Performance Checks

5.1.1 BYPASS Check

The preselector is commanded to BYPASS whenever the Receiver is in the SCAN mode. In BYPASS mode the preselector is effectively removed from the receiver input circuit except for a 35 MHz LPF that attenuates UHF signals. Perform a SCAN operation to verify receiver performance with the preselector out of the RF input circuit.

5.1.2 BPF/LPF Checks

Accurate test and performance measurements of the BPF and LPF sections require the use of a spectrum analyzer and a tracking generator. Performing simple sensitivity checks in each of these bands, however will provide a good evaluation of overall performance. If degraded performance is found in any band, preselector performance can be checked by introducing the signal to the receiver after the preselector output.

5.2 BPF Alignment

This procedure requires skills and equipment that are not normally available at user sites, and should normally be considered a factory or depot level operation. If components have been replaced or disturbed, and realignment is required, proceed as follows:

WARNING

Do not attempt any Preselector alignment or adjustment procedures until all other possible causes for degraded performance have been checked and ruled out. Alignment should never be required unless reactive components have been changed or disturbed.

5.2.1 Required Tools and Test Equipment

a. Tools.

1. Alignment Tool, Hex.
2. Screwdriver, flatblade.

b. Test Equipment (or equivalent)

1. HP-140T Spectrum Analyzer
   (a) HP 8553B RF Section

(b) HP 8552B IF Section

2. Tracking Generator, HP 8444A

5.2.2 Alignment Test Setup

The Receiver's top cover must be removed for this procedure so that the A19 alignment adjustment holes in the top of the assembly can be reached. The Receiver should be placed on a work surface that permits power-up for normal operation, and that will accommodate positioning the required test equipment in close proximity as shown in figure 2.

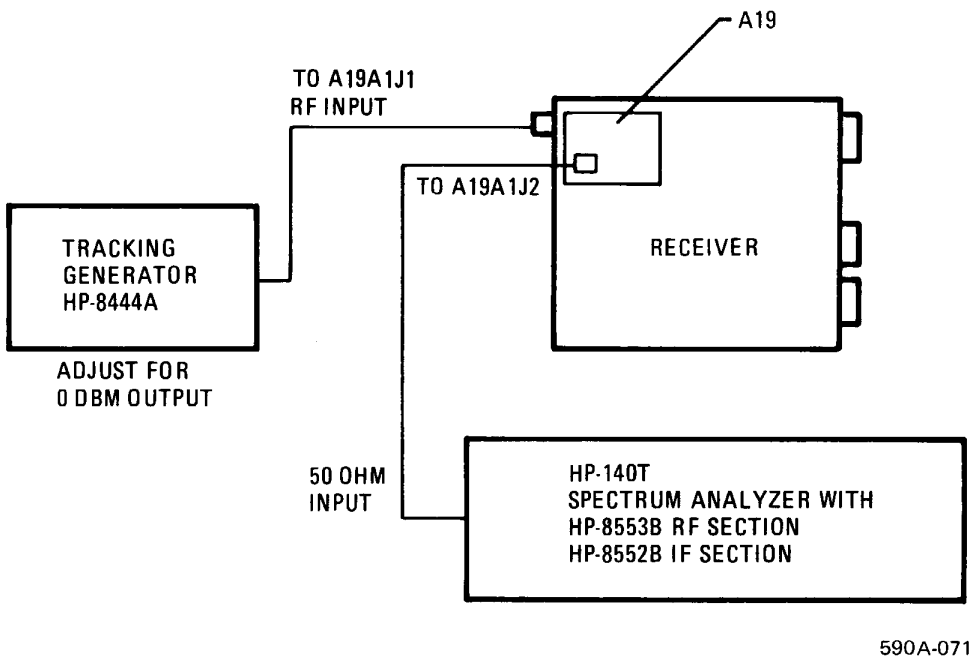
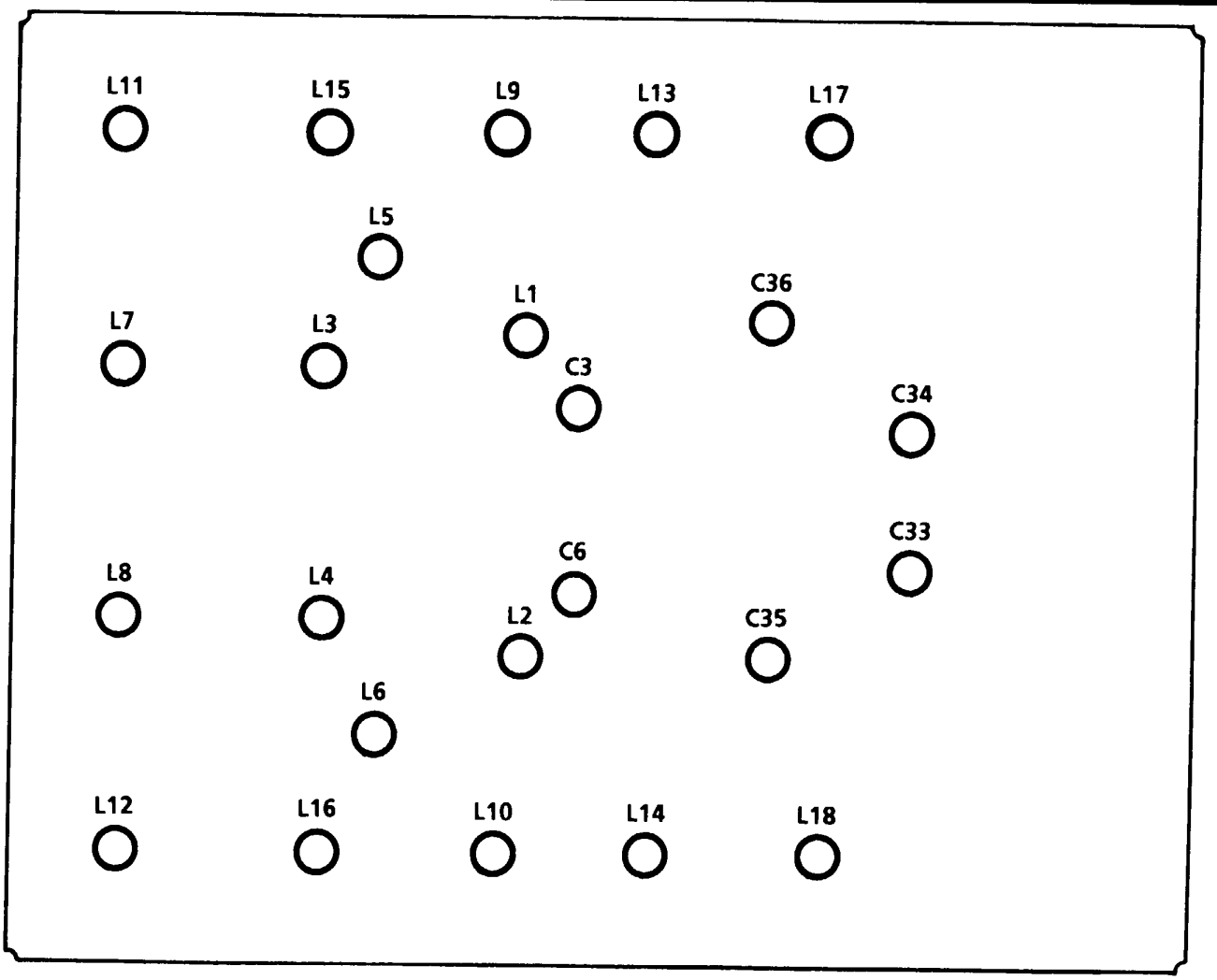


Figure 2. A19 Assembly Test Setup

5.2.3 Alignment Procedure

All adjustable reactive components are on the A19A2 Bandpass Filter PWB Assembly. These components are accessible through the top cover of the assembly as shown in figure 3. The module must be aligned with the top cover on the unit.

a. Connect preselector RF and data cables to test equipment as shown in figure 2. Set generator output level to 0 dBm.



596.04-005 (A)

Figure 3. A19 Assembly Alignment Points

b. Set the Receiver frequency to 15.00 MHz and adjust spectrum analyzer to display preselector passband as shown in figure 4. Adjust L1 and L2 so that the -3 dB passband is centered at 15.00 MHz with minimum insertion loss. Verify that the passband insertion loss is less than 6 dB at this point. Check the ± 10% bandwidth points (13.50 MHz, 16.50 MHz) for at least 20 dB attenuation.

c. Align preselector at each frequency listed in table 2 by setting the Receiver to the indicated frequency and adjusting the appropriate coils. Coils should be aligned so that the -3 dB passband is centered on frequency f as shown in figure 4. Check the ± 10% bandwidth points for at least 20 dB attenuation.

d. Set the Receiver frequency to 29.99 MHz and adjust the spectrum analyzer to display the preselector passband as shown in figure 4. Adjust C3 and C6 so that the -3 dB passband is centered at 30.00 MHz with minimum insertion loss. Verify that the passband insertion loss is less than 6 dB at this point. Check the ± 10% bandwidth points (27.00 MHz, 33.00 MHz) for at least 20 dB attenuation.

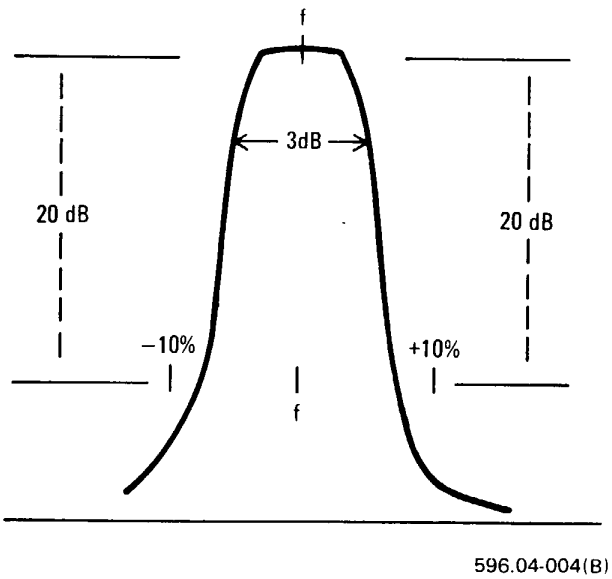


Figure 4. Passband Alignment

Table 2. Alignment Specifications

Frequency f (MHz)	Alignment Coils	U6 Data (1 = + 5 V)								10% Bandwidth (MHz)	
		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	-10%	+ 10%
14.87	L17, L18	1	1	1	1	1	1	1	0	13.41	16.39
14.73	L13, L14	1	1	1	1	1	1	0	1	13.23	16.17
14.48	L9, L10	1	1	1	1	1	0	1	1	13.02	15.92
14.11	L5, L6	1	1	1	1	0	1	1	1	12.69	15.51
13.45	L15, L16	1	1	1	0	1	1	1	1	12.22	14.80
12.55	L11, L12	1	1	0	1	1	1	1	1	11.30	13.81
11.47	L7, L8	1	0	1	1	1	1	1	1	10.31	12.61
9.95	L3, L4	0	1	1	1	1	1	1	1	8.96	10.95

e. Set the Receiver frequency to 7.50 MHz and adjust the spectrum analyzer to display the preselector passband as shown in figure 4. Adjust C33 and C34 so that the -3 dB passband is centered at 5.00 MHz with minimum insertion loss. Verify that the passband insertion loss is less than 6 dB at this point. Check the ± 10% bandwidth points (6.25 MHz, 8.75 MHz) for at least 20 dB attenuation.

f. Set the receiver or exciter frequency to 3.75 MHz and adjust the spectrum analyzer to display the preselector passband as shown in figure 4. Adjust C35 and C36 so that the -3 dB passband is centered at 3.75 MHz with minimum insertion loss. Verify that the passband insertion loss is less than 6 dB at this point. Check the ± 10% bandwidth points (3.48 MHz, 4.26 MHz) for at least 20 dB attenuation.

g. Check passband tuning in 1-MHz increments from 2.0 to 29.99 MHz. The selected frequency should be tuned within the passband with an insertion loss of ≤ 6 dB.

h. Tune the preselector to 1.99 MHz. Set the tuning slugs of A1L8 thru A1L11 fully counterclockwise. Adjust the analyzer to display a lowpass filter with a cutoff frequency of 2.1 MHz. Align the LPF coils using steps 1 thru 4 of figure 5. After alignment, verify that the insertion loss is less than 5.5 dB for frequencies below 2 MHz. Attenuation of signals between 2.7 and 4 MHz should be ≥ 80 dB.

i. Tune the preselector to 599 kHz. Adjust the analyzer to display a lowpass filter with a cutoff frequency of 630 kHz. Align A1L4 to position the filter null at 2.14 MHz. Align A1L3 for the lowest bandpass insertion loss (≤ 600 kHz). After alignment, verify that the insertion loss is less than 2 dB for signals up to 600 kHz. Attenuation of signals between 2.0 and 3.0 MHz should be greater than 60 dB.

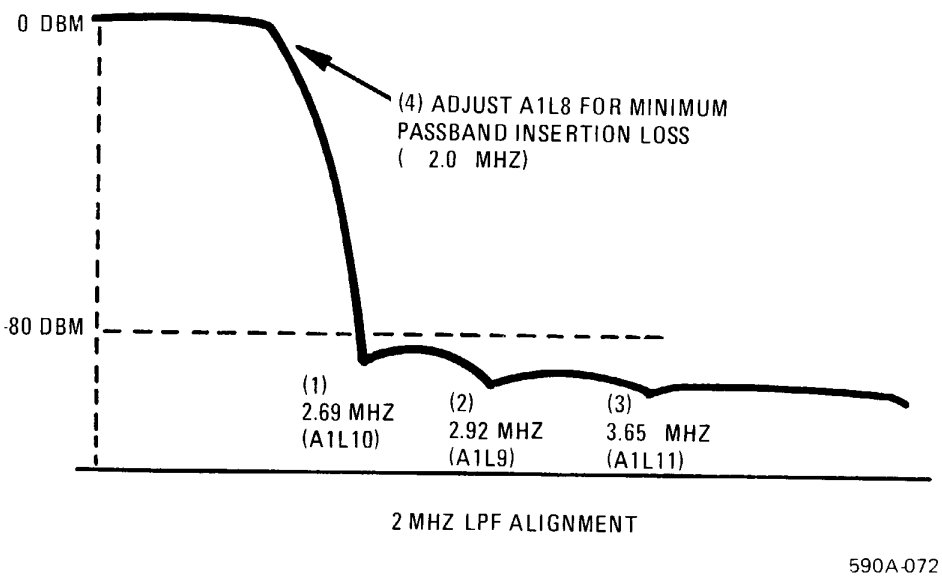


Figure 5. 2 MHz LPF Alignment

6. PARTS LISTS, AND COMPONENT LOCATION AND SCHEMATIC DIAGRAMS

The relative positions of the A19A1 and A19A2 assemblies are shown in figure 6. All components of the A19A1 assembly are listed in table 3 and identified in figure 7. All components of the A19A2 assembly are listed in table 4 and identified in figure 8. The A19A1 schematic is shown in figure 9. The A19A2 schematic is shown in figure 10.

Table 3. Preselector Assembly A19A1 (10215-6660, Rev. J) Module Parts List

Ref. Desig.	Part Number	Description
C1	M39014/02-1310	CAP .1UF 10% 100V CER-R
C2	M39014/02-1310	CAP .1UF 10% 100V CER-R
C3	C26-0035-100	CAP 10UF 20% 35V TANT
C4	M39014/02-1310	CAP .1UF 10% 100V CER-R
C5	M39014/02-1310	CAP .1UF 10% 100V CER-R
C6	M39014/02-1310	CAP .1UF 10% 100V CER-R
C7	M39014/02-1310	CAP .1UF 10% 100V CER-R
C8	M39014/02-1310	CAP .1UF 10% 100V CER-R
C9	M39014/02-1320	CAP .47UF 10% 50V CER-R
C10	C26-0025-470	CAP 47UF 20% 25V TANT
C11	M39014/02-1298	CAP .01UF 10% 200V CER-R
C12	M39014/02-1298	CAP .01UF 10% 200V CER-R
C13	M39014/02-1298	CAP .01UF 10% 200V CER-R
C14	M39014/02-1298	CAP .01UF 10% 200V CER-R
C15	M39014/02-1298	CAP .01UF 10% 200V CER-R
C16	M39014/02-1298	CAP .01UF 10% 200V CER-R
C17	M39014/02-1298	CAP .01UF 10% 200V CER-R
C18	M39014/02-1298	CAP .01UF 10% 200V CER-R
C19	M39014/02-1298	CAP .01UF 10% 200V CER-R
C20	M39014/02-1298	CAP .01UF 10% 200V CER-R
C21	M39014/02-1298	CAP .01UF 10% 200V CER-R
C22	M39014/02-1298	CAP .01UF 10% 200V CER-R
C23	M39014/02-1298	CAP .01UF 10% 200V CER-R
C24	M39014/02-1298	CAP .01UF 10% 200V CER-R
C25	M39014/02-1310	CAP .1UF 10% 100V CER-R
C26	M39014/02-1298	CAP .01UF 10% 200V CER-R
C27	CM05CD100D03	CAP 10PF + -.5PF 500V MICA
C28	CM05FD151J03	CAP 150PF 5% 500V MICA
C29	M39014/02-1310	CAP .1UF 10% 100V CER-R
C30	M39014/02-1310	CAP .1UF 10% 100V CER-R
C31	M39014/02-1310	CAP .1UF 10% 100V CER-R
C32	CK06BX332K	CAP 3300PF 10% 200V CER
C33	M39014/02-1298	CAP .01UF 10% 200V CER-R
C37	C26-0025-100	CAP 10UF 20% 25V TANT
C38	M39014/02-1310	CAP .1UF 10% 100V CER-R
C39	M39014/02-1310	CAP .1UF 10% 100V CER-R
C40	M39014/02-1310	CAP .1UF 10% 100V CER-R
C41	CM05CD100D03	CAP 10PF + -.5PF 500V MICA
C42	CM05FD151J03	CAP 150PF 5% 500V MICA
C43	C26-0050-109	CAP 1.0UF 20% 50V TANT
C44	M39014/02-1310	CAP .1UF 10% 100V CER-R
C45	CM05FD131J03	CAP 130PF 5% 500V MICA
C46	CM05FD361J03	CAP 360PF 5% 500V MICA
C47	M39014/02-1295	CAP 6800PF 10% 200V CER-R

Table 3. Preselector Assembly A19A1 (10215-6660, Rev. J) Module Parts List (Cont.)

Ref. Desig.	Part Number	Description
C48	CM06FD222J03	CAP 2200PF 5% 500V MICA
C49	CM06FD302J03	CAP 3000PF 5% 500V MICA
C50	CM06FD242J03	CAP 2400PF 5% 500V MICA
C51	CM06FD272J03	CAP 2700PF 5% 500V MICA
C52	CM06FD182J03	CAP 1800PF 5% 500V MICA
C53	CM05FD131J03	CAP 130PF 5% 500V MICA
C54	CM06FD821J03	CAP 820PF 5% 500V MICA
C55	CM06FD102J03	CAP 1000PF 5% 500V MICA
C56	CM06FD471J03	CAP 470PF 5% 500V MICA
C57	M39014/02-1298	CAP .01UF 10% 200V CER-R
C58	CK06BX332K	CAP 3300PF 10% 200V CER
C59	M39014/02-1310	CAP .1UF 10% 100V CER-R
C60	M39014/02-1310	CAP .1UF 10% 100V CER-R
CR1	1N4148	DIODE 200mA 100V SW
CR2	1N4148	DIODE 200mA 100V SW
CR3	1N5711	DIODE SCHOTTKY 70V .25W
CR4	1N4148	DIODE 200mA 100V SW
CR5	1N4148	DIODE 200mA 100V SW
CR6	1N5711	DIODE SCHOTTKY 70V .25W
CR7	1N4148	DIODE 200mA 100V SW
CR8	1N4148	DIODE 200mA 100V SW
CR9	D50-0010-070	TRANSZORB,LOW CAP,7.0V
CR10	D50-0010-070	TRANSZORB,LOW CAP,7.0V
J1	J-0086	CONN SMB RT A PCB F
J2	J-0086	CONN SMB RT A PCB F
J3	J43-0006-006	CONNECTOR
J4	J43-0006-006	CONNECTOR
J5	J43-0006-006	CONNECTOR
J6	J43-0006-006	CONNECTOR
J9	J46-0038-005	CONNECTOR, 5PIN LOCK
J10	J46-0038-006	CONNECTOR,6PIN LOCK
J11	J46-0034-010	HDR 10 PIN 0.100" RT ANG
JMP1	MP-1142	RES ZERO OHM (CKT JMPR)
JMP2	MP-1142	RES ZERO OHM (CKT JMPR)
JMP3	MP-1142	RES ZERO OHM (CKT JMPR)
JMP4	MP-1142	RES ZERO OHM (CKT JMPR)
K1	K10-0004-901	RLY DPDT 12VDC SEALED DIP
K2	K10-0004-901	RLY DPDT 12VDC SEALED DIP
K3	K10-0004-901	RLY DPDT 12VDC SEALED DIP
K4	K10-0004-901	RLY DPDT 12VDC SEALED DIP
K5	K10-0004-901	RLY DPDT 12VDC SEALED DIP
K6	K10-0004-901	RLY DPDT 12VDC SEALED DIP
K7	K10-0004-901	RLY DPDT 12VDC SEALED DIP
L1	MS18130-8	COIL 1.0UH 10% FXD RF
L2	MS18130-8	COIL 1.0UH 10% FXD RF
L3	L11-0004-027	INDUCT SH VAR 13.5-16.5UH
L4	L11-0004-027	INDUCT SH VAR 13.5-16.5UH
L7	MS18130-8	COIL 1.0UH 10% FXD RF
L8	L11-0004-021	INDUCT SH VAR 4.23-5.17UH

Table 3. Preselector Assembly A19A1 (10215-6660, Rev. J) Module Parts List (Cont.)

Ref. Desig.	Part Number	Description
L9	L11-0004-019	INDUCT SH VAR 2.97-3.63UH
L10	L11-0004-019	INDUCT SH VAR 2.97-3.63UH
L11	L11-0004-020	INDUCT SH VAR 3.51-4.29UH
P1	10085-0119	JACK COAX PCMNT
P2	10085-0119	JACK COAX PCMNT
Q1	Q35-0003-000	XSTR N-CH JFET U310
Q2	Q35-0003-000	XSTR N-CH JFET U310
R1	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R2	R65-0003-473	RES 47K 5% 1/4W CAR FILM
R3	R65-0003-821	RES 820 5% 1/4W CAR FILM
R4	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R5	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R8	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R9	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R11	R65-0003-222	RES 2.2K 5% 1/4W CAR FILM
R12	R65-0003-821	RES 820 5% 1/4W CAR FILM
R13	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R14	R65-0003-473	RES 47K 5% 1/4W CAR FILM
R15	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R16	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R17	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R18	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R19	R65-0003-152	RES 1.5K 5% 1/4W CAR FILM
R20	R65-0003-221	RES 220 5% 1/4W CAR FILM
R21	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R22	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R23	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R24	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R25	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R26	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R27	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R28	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R29	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R30	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R31	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R32	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R33	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R34	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R35	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R36	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R37	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R43	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R44	R65-0003-103	RES 10K 5% 1/4W CAR FILM
U1	I01-0000-156	IC 4094B PLASTIC CMOS
U2	I01-0000-156	IC 4094B PLASTIC CMOS
U3	I90-0006-003	IC XSTR ARRAY DARL 2003
U4	I90-0006-003	IC XSTR ARRAY DARL 2003
U5	I90-0006-003	IC XSTR ARRAY DARL 2003
U6	10215-8100	SOFTWARE KIT

Table 3. Preselector Assembly A19A1 (10215-6660, Rev. J) Module Parts List (Cont.)

Ref. Desig.	Part Number	Description
U7	10215-8300	SOFTWARE KIT
VR1	I11-0001-001	IC VR 7805 +5V 1.5A 4%
VR2	IC-0358	IC VR 317 ADJ V 1.5A
XU6	J77-0008-006	SKT IC MACH 28 PIN
XU7	J77-0008-006	SKT IC MACH 28 PIN

Table 4. Bandpass Filter Assembly A19A2 Parts List (10215-6670, Rev. E)

Ref. Desig.	Part Number	Description
C1	CM05FD221G03	CAP 220PF 2% 500V MICA
C2	CM06FD511J03	CAP 510PF 5% 500V MICA
C3	C85-0001-002	CAPACITOR .8-10 PF
C4	CM05FD910G03	CAP 91PF 2% 500V MICA
C5	CM05ED470G03	CAP 47PF 2% 500V MICA
C6	C85-0001-002	CAPACITOR .8-10 PF
C7	CM06FD911J03	CAP 910PF 5% 500V MICA
C8	CM05ED470G03	CAP 47PF 2% 500V MICA
C9	CM05FD221G03	CAP 220PF 2% 500V MICA
C10	CM06FD511J03	CAP 510PF 5% 500V MICA
C11	CM06FD751F03	CAPACITOR
C12	CM06FD272J03	CAP 2700PF 5% 500V MICA
C13	M39014/02-1310	CAP .1 UF
C14	CM06FD182J03	CAP 1800PF 5% 500V MICA
C15	M39014/02-1310	CAP .1 UF
C16	CM06FD681J03	CAP 680PF 5% 500V MICA
C17	CM06FD182J03	CAP 1800PF 5% 500V MICA
C18	CM06FD681J03	CAP 680PF 5% 500V MICA
C19	CM05ED820G03	CAP 82PF 2% 500V MICA
C20	CM06FD272J03	CAP 2700PF 5% 500V MICA
C21	CM05FD161G03	CAP 160PF 2% 500V MICA
C22	CM07FD512J03	CAPACITOR
C23	CM05FD161G03	CAP 160PF 2% 500V MICA
C24	CM07FD103J03	CAPACITOR
C25	CM07FD822J03	CAPACITOR
C26	CM06FD751F03	CAPACITOR
C27	CM05ED820G03	CAP 82PF 2% 500V MICA
C29	M39014/02-1298	CAP 01UF
C30	M39014/02-1298	CAP 01UF
C31	C-2496	CAP 470PF 2% 500V MICA
C32	C-2496	CAP 470PF 2% 500V MICA
C33	C84-0003-004	CAP,VAR,CER,9-35 PF
C34	C84-0003-004	CAP,VAR,CER,9-35 PF
C35	C84-0003-004	CAP,VAR,CER,9-35 PF
C36	C84-0003-004	CAP,VAR,CER,9-35 PF
J1	J-0031	CONNECTOR, COAX, SNAP-ON
J2	J-0031	CONNECTOR, COAX, SNAP-ON
K1	K10-0004-901	RELAY, DPDT
K2	K10-0004-901	RELAY, DPDT

Table 4. Bandpass Filter Assembly A19A2 Parts List (10215-6670, Rev. E) (Cont.)

Ref. Desig.	Part Number	Description
K3	K10-0004-901	RELAY, DPDT
K4	K10-0004-901	RELAY, DPDT
K5	K10-0004-901	RELAY, DPDT
K6	K10-0004-901	RELAY, DPDT
K7	K10-0004-901	RELAY, DPDT
K8	K10-0004-901	RELAY, DPDT
K9	K10-0004-901	RELAY, DPDT
K10	K10-0004-901	RELAY, DPDT
K11	K10-0004-901	RELAY, DPDT
K12	K10-0004-901	RELAY, DPDT
K13	K10-0004-901	RELAY, DPDT
K14	K10-0004-901	RELAY, DPDT
K15	K10-0004-901	RELAY, DPDT
K16	K10-0004-901	RELAY, DPDT
K17	K10-0004-901	RELAY, DPDT
K18	K10-0004-901	RELAY, DPDT
K19	K10-0004-901	RELAY, DPDT
K20	K10-0004-901	RELAY, DPDT
K21	K10-0004-901	RELAY, DPDT
K22	K10-0004-901	RELAY, DPDT
K23	K10-0004-901	RELAY, DPDT
K24	K10-0004-901	RELAY, DPDT
K25	K10-0004-901	RELAY, DPDT
K26	K10-0004-901	RELAY, DPDT
K27	K10-0004-901	RELAY, DPDT
K28	K10-0004-901	RELAY, DPDT
L1	L11-0005-552	COIL
L2	L11-0005-552	COIL
L3	10073-6662	INDUCTOR, VARIABLE
L4	10073-6662	INDUCTOR, VARIABLE
L5	L11-0005-297	COIL
L6	L11-0005-297	COIL
L7	10073-6663	INDUCTOR, VARIABLE
L8	10073-6663	INDUCTOR, VARIABLE
L9	L11-0005-171	COIL
L10	L11-0005-171	COIL
L11	10215-6690	COIL, VARIABLE 11.5T
L12	10215-6690	COIL, VARIABLE 11.5T
L13	L11-0005-115	COIL
L14	L11-0005-115	COIL
L15	L11-0005-466	COIL
L16	L11-0005-466	COIL
L17	L11-0005-070	COIL
L18	L11-0005-070	COIL
L19	10073-6661	INDUCTOR, VARIABLE
L20	10073-6661	INDUCTOR, VARIABLE
P1	J46-0003-006	HEADER, 6 PIN
P2	J46-0003-006	HEADER, 6 PIN
P3	J46-0003-006	HEADER, 6 PIN
P4	J46-0003-006	HEADER, 6 PIN

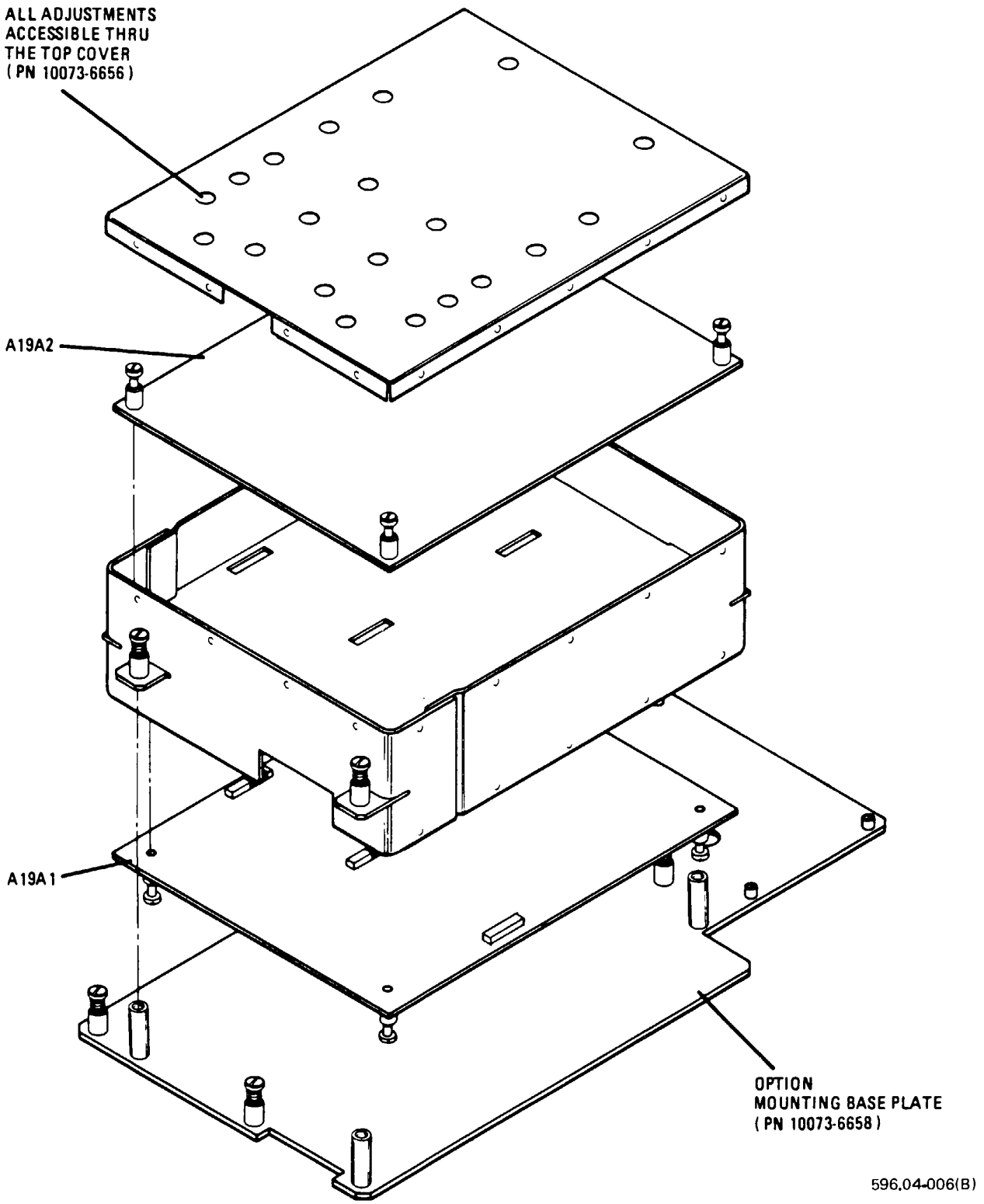


Figure 6. Preselector Assembly Drawing

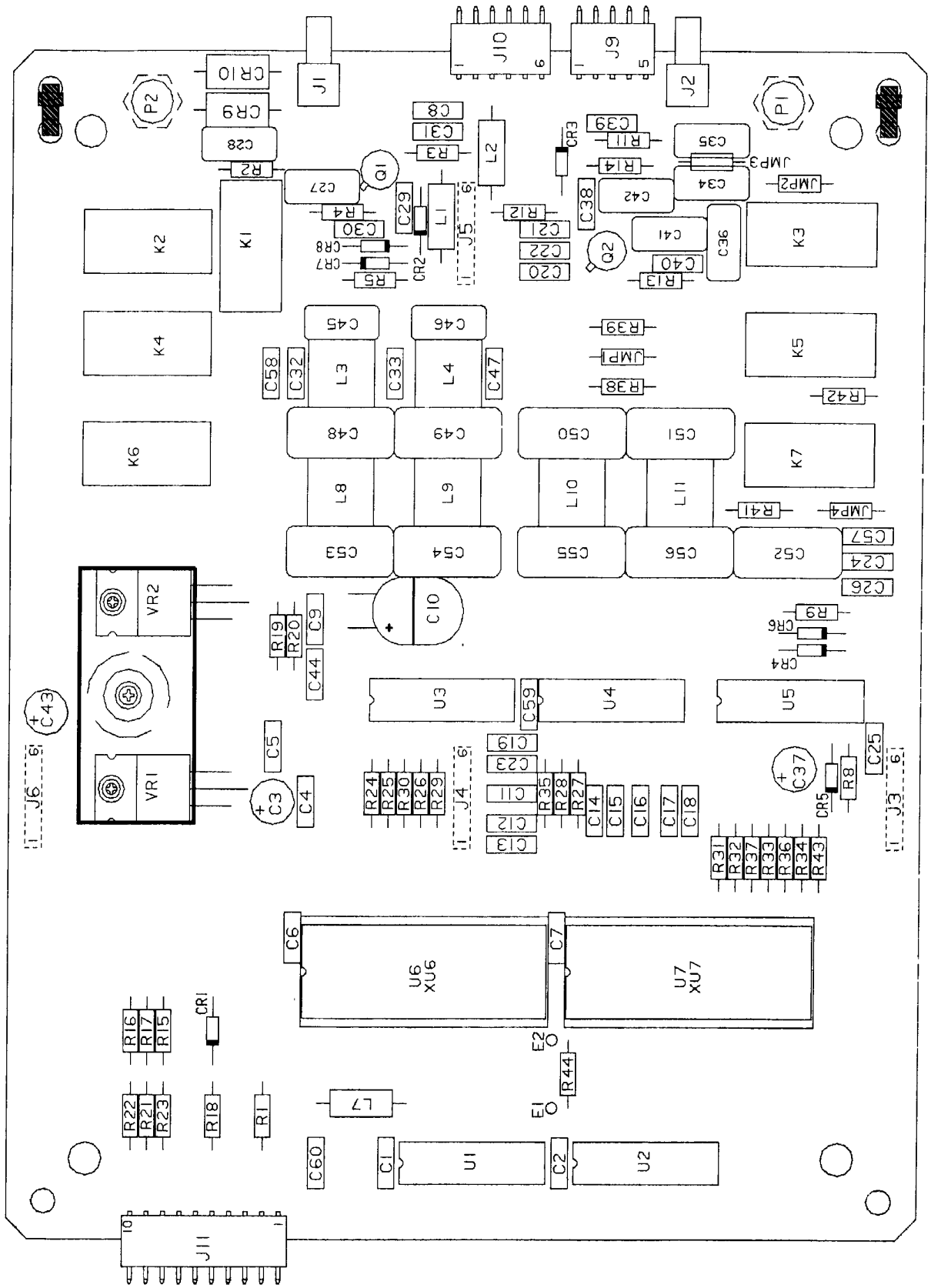


Figure 7. A19A1 PWB Component Locations (10215-6660, Rev. F)

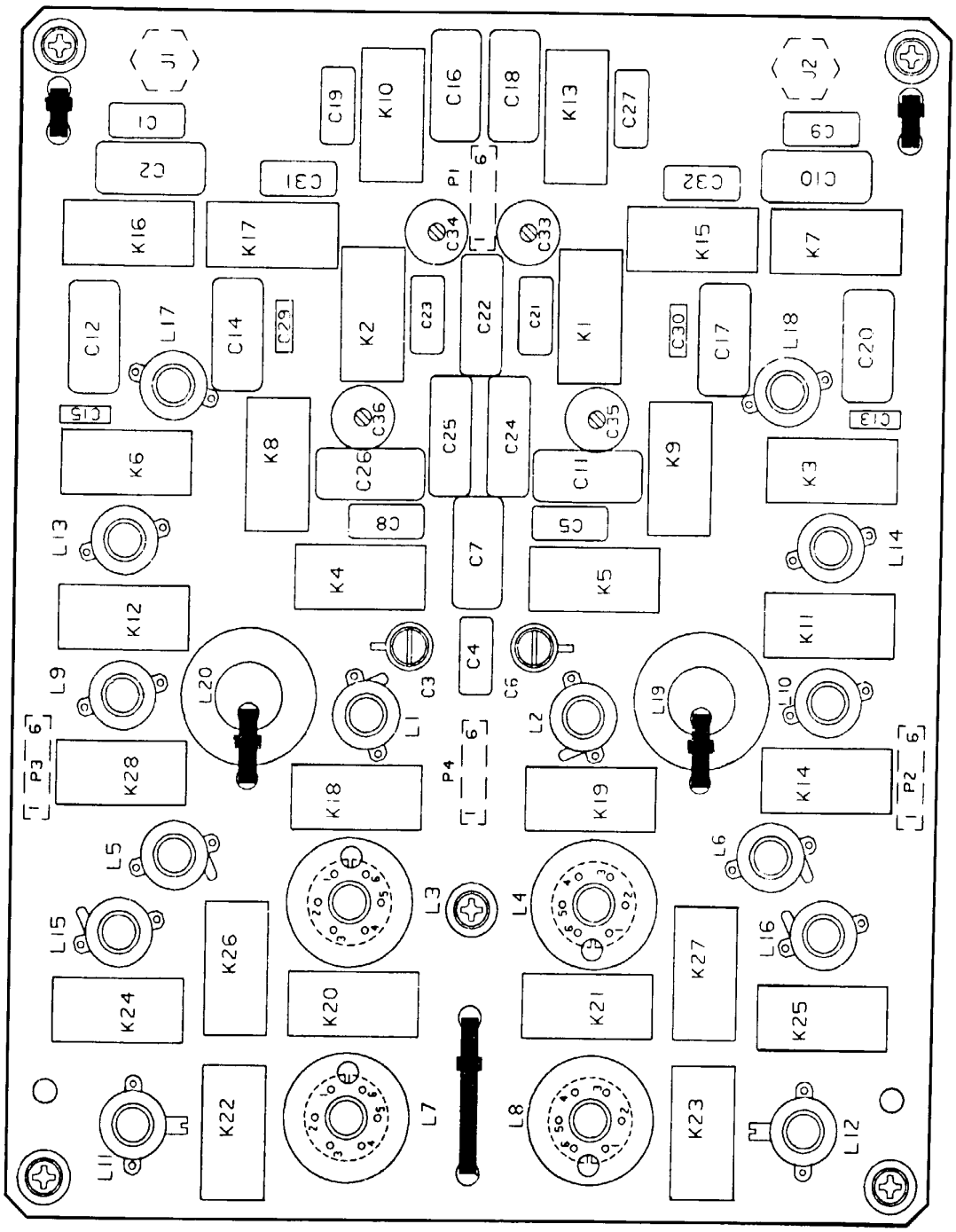


Figure 8. A19A2 PWB Component Locations (10215-6670, Rev. B)

NOTE: UNLESS OTHERWISE SPECIFIED:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR A COMPLETE DESIGNATION, PREFIX WITH UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.
2. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, ±5%.
3. ALL CAPACITOR VALUES ARE IN MICROFARADS.
4. VENDOR PART NO. CALLOUTS ARE FOR REFERENCE ONLY. COMPONENTS ARE SUPPLIED PER PART NO. IN PARTS LIST.
5. JUMPER E1 AND E2 FOR USE IN RF-590 AND RF-590A TO ACCOMODATE BYPASS FUNCTION IN SCAN MODE.
6. R38 AND R39 ARE FOR OPTIONAL USE ONLY.
7. C34-C36, R41, AND R42 ARE FOR OPTIONAL USE ONLY.

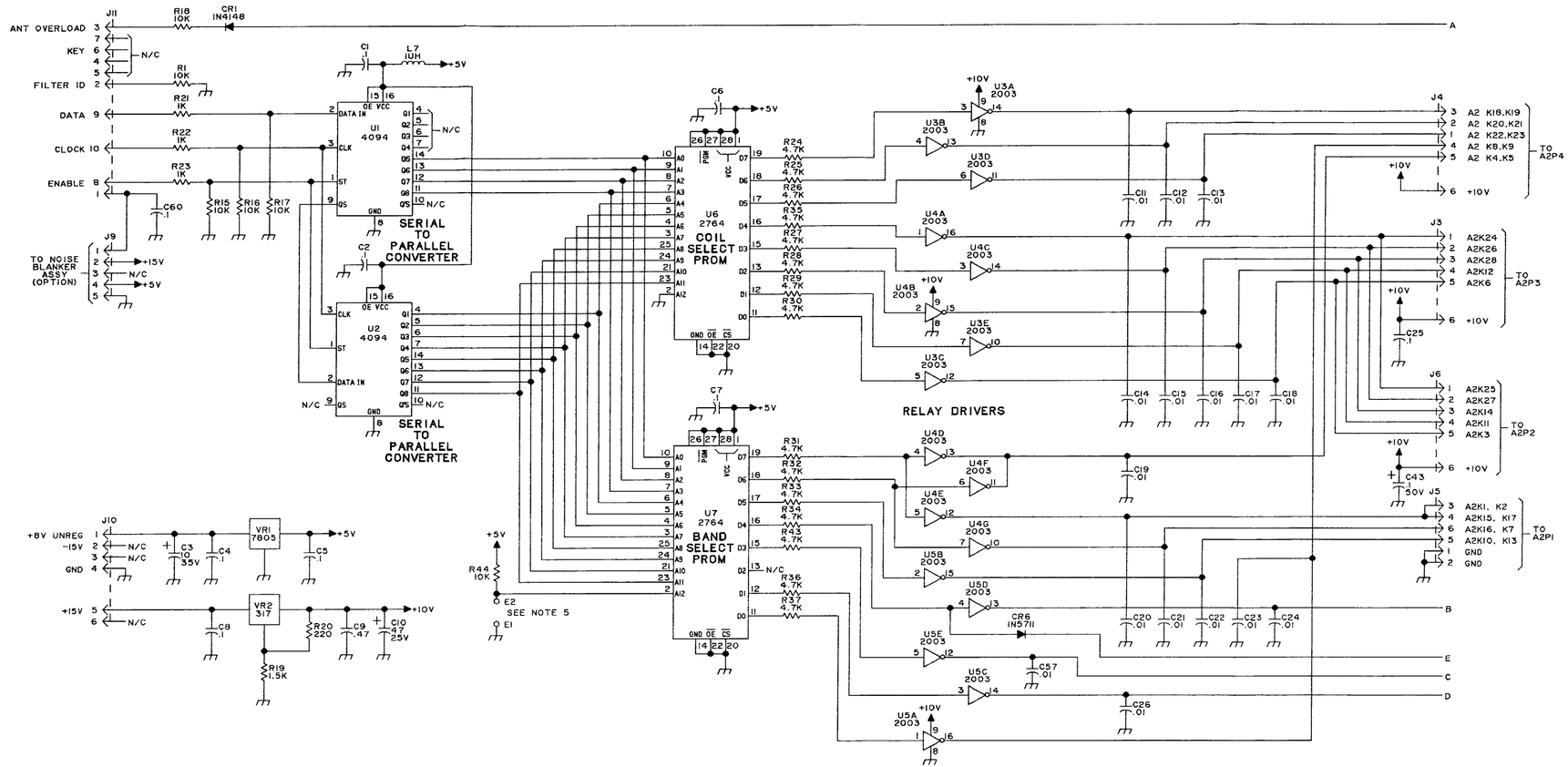


Figure 9. A19A1 PWB Schematic Diagram (10215-6661, Rev. G) (Sheet 1 of 2)

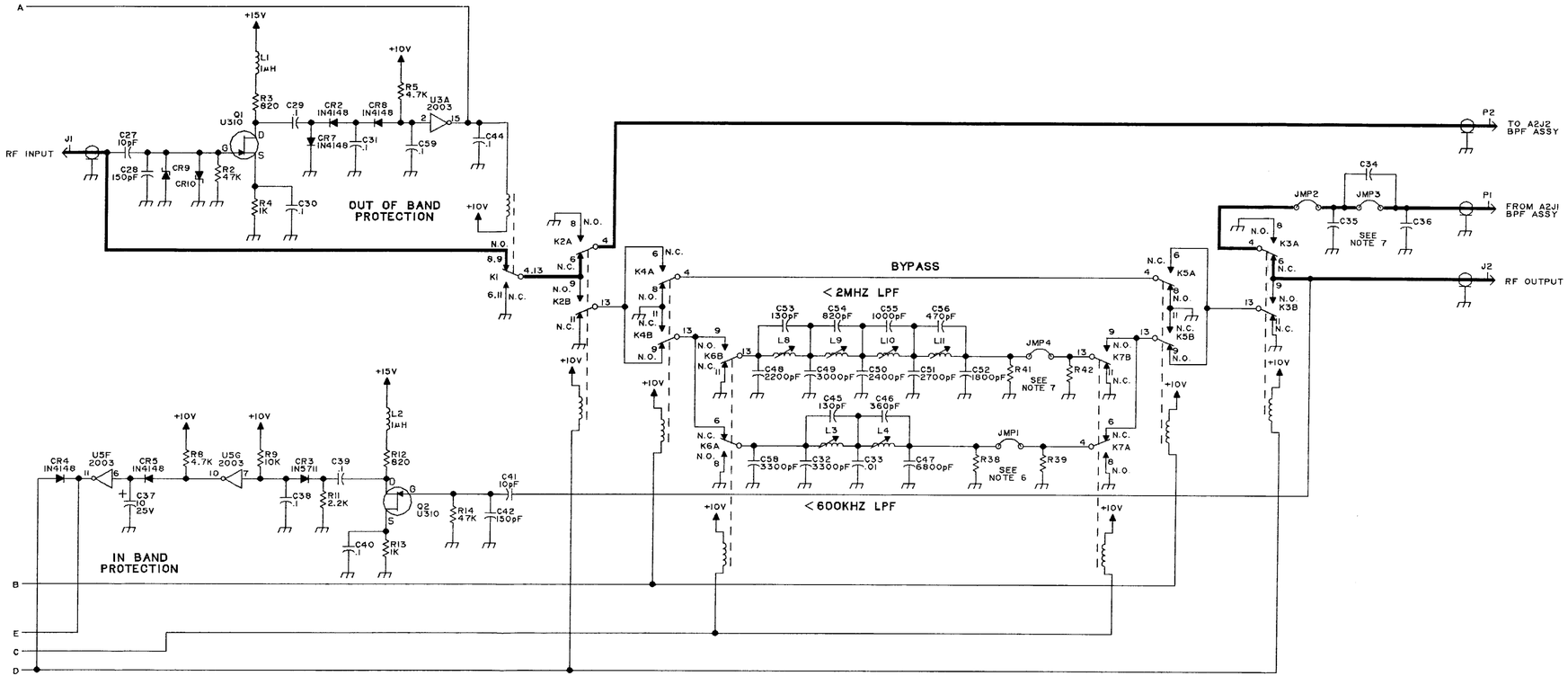
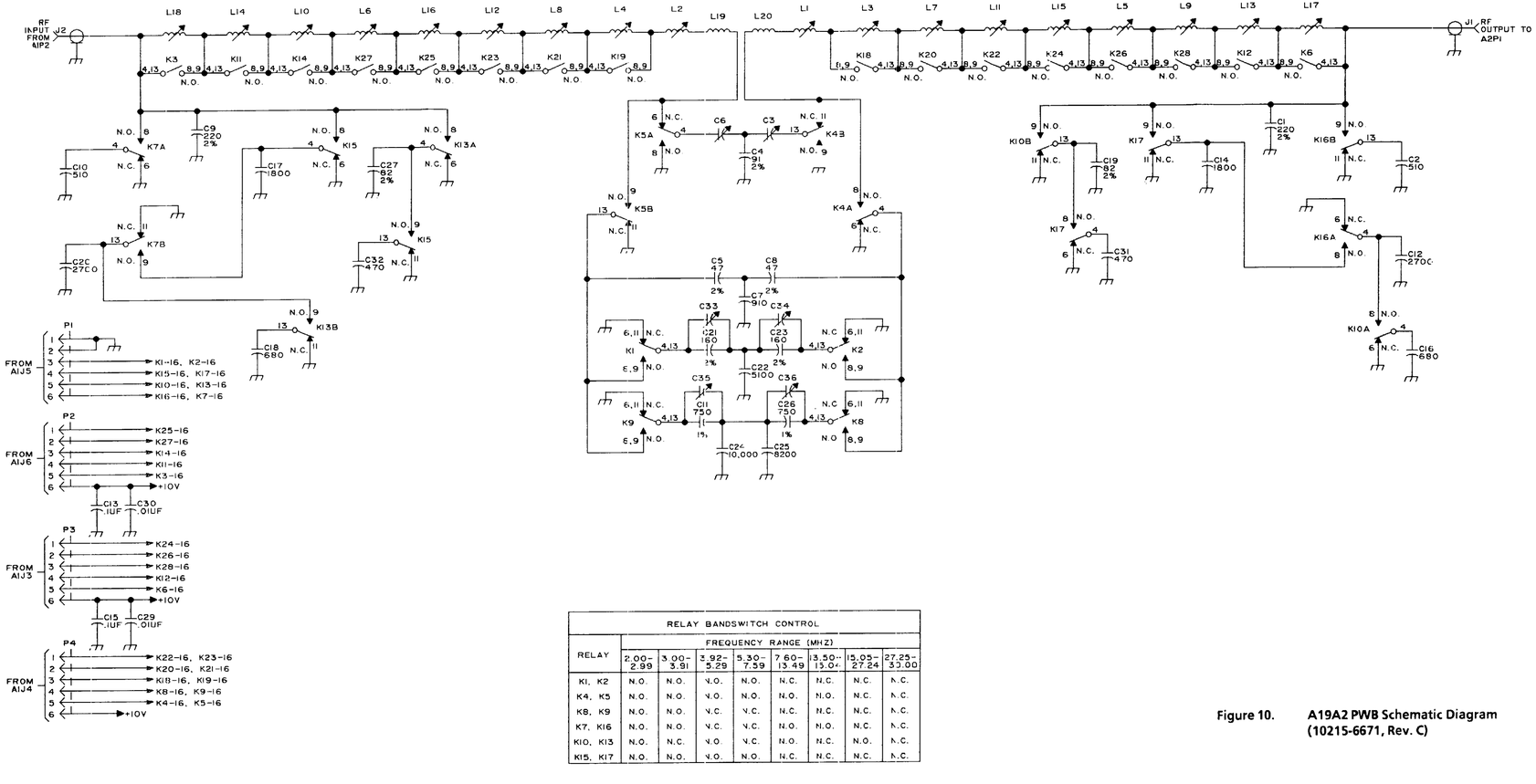


Figure 9. A19A1 PWB Schematic Diagram (10215-6661, Rev. G) (Sheet 2 of 2)

NOTE: UNLESS OTHERWISE SPECIFIED:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR A COMPLETE DESIGNATION, PREFIX WITH UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.
2. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, ±5%.
3. ALL CAPACITOR VALUES ARE IN PICOFARADS.
4. VENDOR PART NO. CALLOUTS ARE FOR REFERENCE ONLY. COMPONENTS ARE SUPPLIED PER PART NO. IN PARTS LIST.
5. ALL INDUCTOR VALUES ARE IN MICROHENRIES.
6. RELAY COILS (K1 THRU K28) RECEIVE POWER (+10V) AT PIN 1 AND ARE ACTUATED VIA PIN 16. SEE FIGURE 1.

FIGURE 1
+10V
1
K1 THRU K28 (TYPICAL)
16



RELAY BANDSWITCH CONTROL								
RELAY	FREQUENCY RANGE (MHZ)							
	2.00-2.99	3.00-3.91	3.92-5.29	5.30-7.59	7.60-13.49	13.50-15.04	15.05-27.24	27.25-30.00
K1, K2	N.O.	N.O.	N.O.	N.O.	N.C.	N.C.	N.C.	N.C.
K4, K5	N.O.	N.O.	N.O.	N.O.	N.O.	N.O.	N.C.	N.C.
K8, K9	N.O.	N.O.	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.
K7, K16	N.O.	N.O.	N.C.	N.C.	N.O.	N.O.	N.C.	N.C.
K10, K13	N.O.	N.C.	N.O.	N.C.	N.O.	N.C.	N.O.	N.C.
K15, K17	N.O.	N.O.	N.O.	N.O.	N.C.	N.C.	N.C.	N.C.

Figure 10. A19A2 PWB Schematic Diagram (10215-6671, Rev. C)

A25
EMP/EMI SUPPRESSION ASSEMBLY

TABLE OF CONTENTS

Paragraph		Page
1.	Introduction	1
2.	Circuit Description	1
3.	Parts Lists, Component Locations, and Schematic Diagrams	1

LIST OF FIGURES

Figure		Page
1	EMP/EMI Suppression Assembly A25 Component Locations (10215-6850)	3
2	EMP/EMI Suppression Assembly A25 Schematic Diagram (10215-6851)	5

LIST OF TABLES

Table		Page
1	EMP/EMI Suppression Assembly A25 Parts List (10215-6850)	2

A25 EMP/EMI SUPPRESSION ASSEMBLY

1. INTRODUCTION

The EMP/EMI Suppression assembly is mounted inside the rear panel of the main chassis as shown in figure 1 of the Main Chassis Interconnection section of this manual. Rear panel connector J7 is mounted on the assembly as is the Carrier Operated Relay (COR). Besides providing physical support for the above-mentioned devices, the assembly provides filtering and EMP/EMI protection for the remote control interface and the audio output circuits.

2. CIRCUIT DESCRIPTION

Each of the remote control interface signal lines and audio signal lines in protected against electromagnetic pulses by zener diodes. Filtering is provided by simple LC networks.

The COR provides switching between normally closed (N.C.) and normally open (N.O.) contacts accessible via rear panel connector pins J7-22 and J7-23, respectively. The relay is driven by the COR circuit on the A5 assembly.

3. PARTS LISTS, COMPONENT LOCATIONS, AND SCHEMATIC DIAGRAMS

All replaceable components of the A25 assembly are listed in table 1 and identified in figure 1. The circuits of the A25 assembly are diagrammed schematically in figure 2.

Table 1. EMP/EMI Suppression Assembly A25 Parts List (10215-6850, Rev. F)

Ref. Desig.	Part Number	Description
--	10215-6854	CABLE ASSEMBLY
C1	CK06BX472K	CAP 4700PF 10% 200V CER
C2	CK06BX472K	CAP 4700PF 10% 200V CER
C3	CK05BX472K	CAP 4700PF 10% 100V CER
C4	CK05BX472K	CAP 4700PF 10% 100V CER
C5	CK06BX472K	CAP 4700PF 10% 200V CER
C6	CK06BX472K	CAP 4700PF 10% 200V CER
C7	CK06BX472K	CAP 4700PF 10% 200V CER
C8	CK06BX472K	CAP 4700PF 10% 200V CER
CR1	1N4148	DIODE 200mA 100V SW
CR2	D50-0005-003	TRANSORB 6.63 V 1500W BI
CR3	D50-0005-003	TRANSORB 6.63 V 1500W BI
CR4	D50-0005-003	TRANSORB 6.63 V 1500W BI
CR5	D50-0005-003	TRANSORB 6.63 V 1500W BI
CR6	D50-0005-003	TRANSORB 6.63 V 1500W BI
CR7	D50-0005-003	TRANSORB 6.63 V 1500W BI
CR8	D50-0005-003	TRANSORB 6.63 V 1500W BI
CR9	D50-0005-003	TRANSORB 6.63 V 1500W BI
CR10	D50-0007-000	TRANSORB 12.8V 600W BI
CR11	D50-0005-003	TRANSORB 6.63 V 1500W BI
J1	J46-0022-003	HDR 3 PIN 0.100" SR LKG
J7	J22-0035-101	CONN-D M 25 FXD CAPT HW
JMP1	MP-1142	RES ZERO OHM (CKT JMPR)
K1	K10-0004-901	RLY DPDT 12VDC SEALED DIP
L1	MS75085-14	COIL 390UH 10% FXD RF
L2	MS75085-14	COIL 390UH 10% FXD RF
L3	MS75085-8	COIL 120UH 10% FXD RF
L4	MS75085-8	COIL 120UH 10% FXD RF
L5	MS75085-14	COIL 390UH 10% FXD RF
L6	MS75085-14	COIL 390UH 10% FXD RF
L7	L-0185	CHOKE W B 180 MHZ
L8	L-0185	CHOKE W B 180 MHZ
L9	L-0185	CHOKE W B 180 MHZ
L10	L-0185	CHOKE W B 180 MHZ
L11	MS75085-14	COIL 390UH 10% FXD RF
L12	MS75085-14	COIL 390UH 10% FXD RF
L13	L-0185	CHOKE W B 180 MHZ
L14	L-0185	CHOKE W B 180 MHZ
L15	L-0185	CHOKE W B 180 MHZ
L16	L-0185	CHOKE W B 180 MHZ
L17	L-0185	CHOKE W B 180 MHZ
L18	L-0185	CHOKE W B 180 MHZ

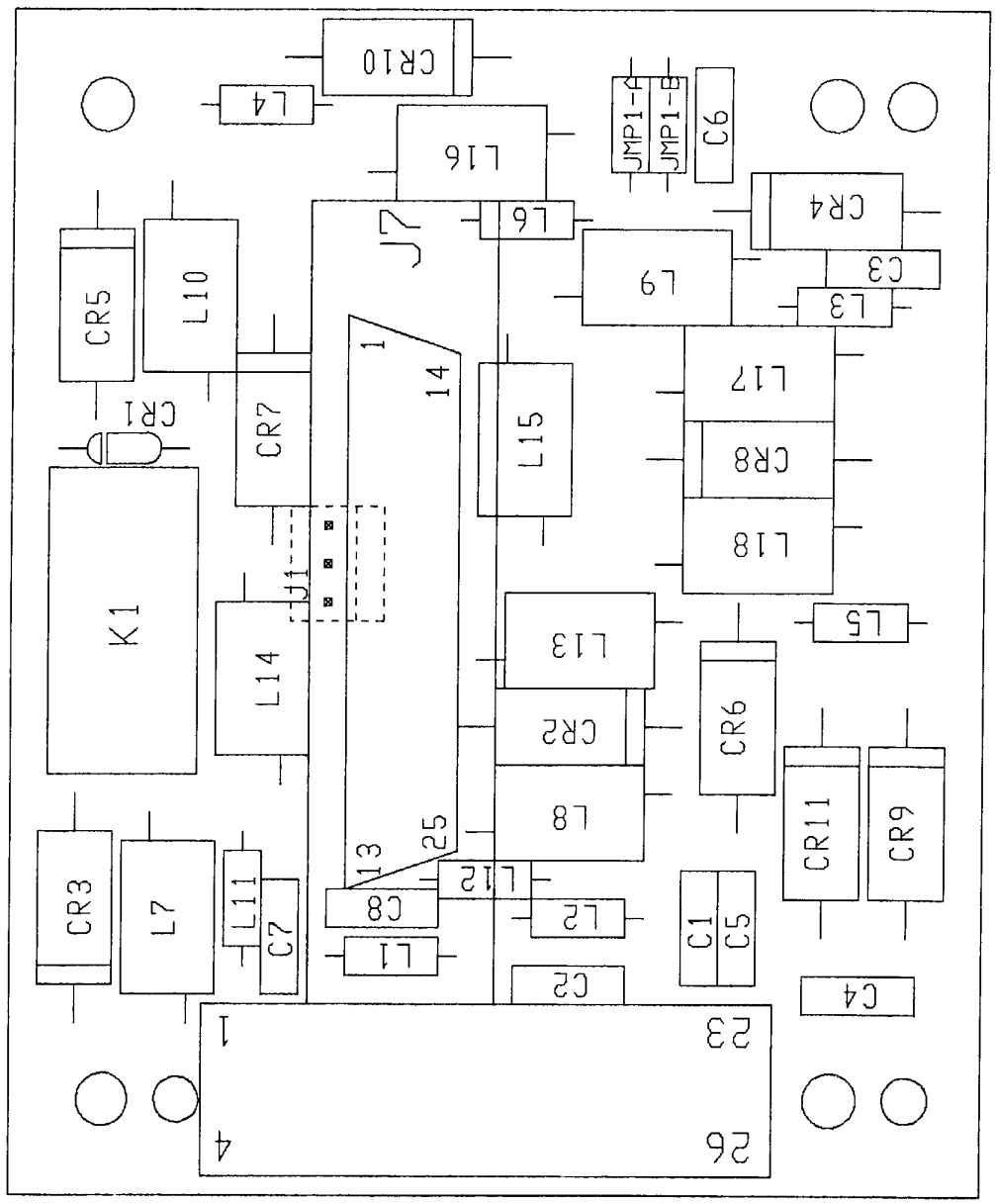


Figure 1. EMP/EMI Suppression Assembly A25 Component Locations (10215-6850, Rev. E)

NOTE: UNLESS OTHERWISE SPECIFIED:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR A COMPLETE DESIGNATION, PREFIX WITH UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.
2. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, ±5%.
3. ALL CAPACITOR VALUES ARE IN MICROFARADS.
4. VENDOR PART NO. CALLOUTS ARE FOR REFERENCE ONLY. COMPONENTS ARE SUPPLIED PER PART NO. IN PARTS LIST.
5. FOR BALANCED 600 OHM AUDIO OUTPUT MOVE JMP1 FROM POSITION 1 TO POSITION 2.

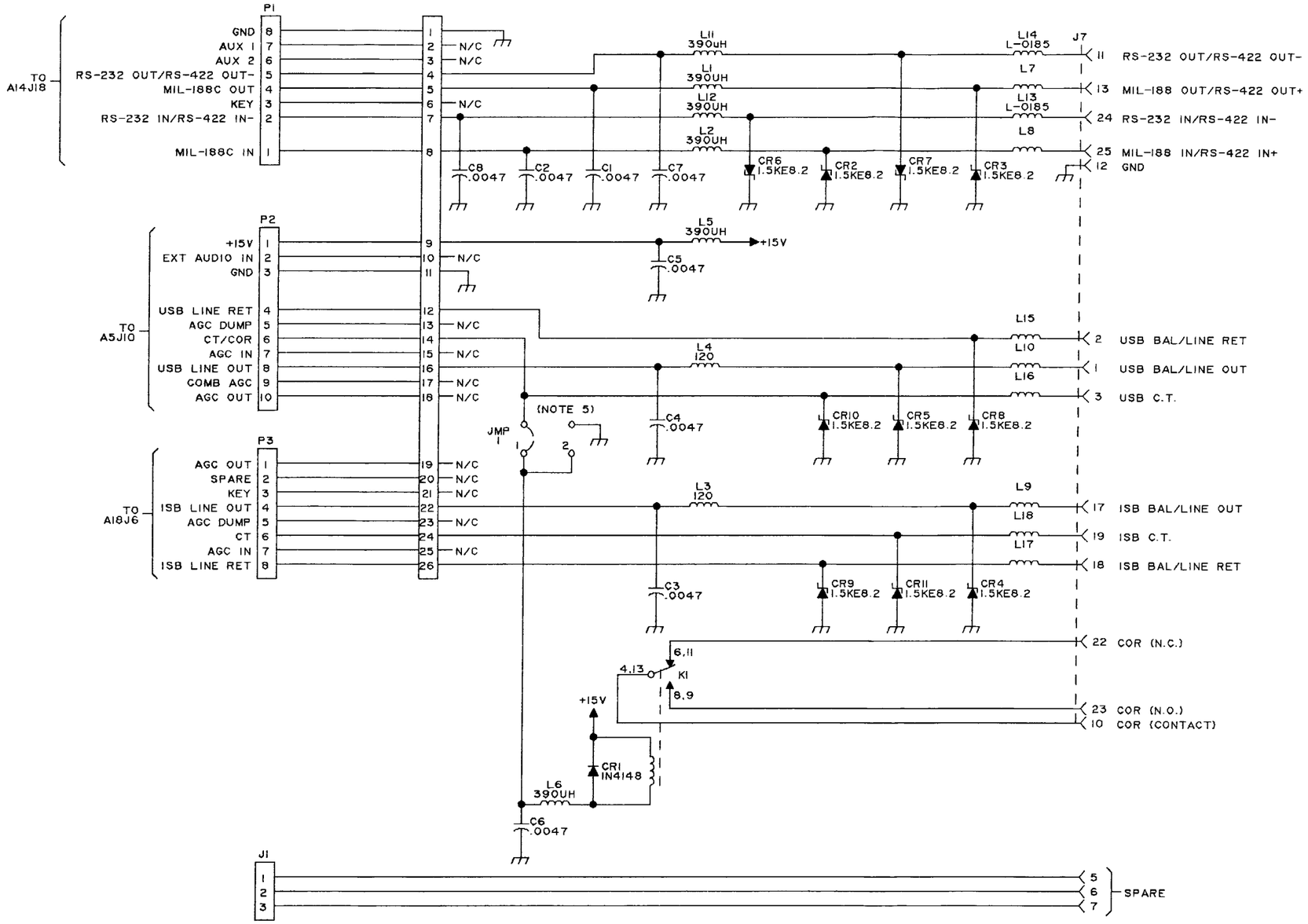


Figure 2. **EMP/EMI Suppression Assembly A25 Schematic Diagram (10215-6851, Rev. E)**

APPENDIX

DATA SHEETS

Data sheets are listed in alphanumeric order in table A-1.

Table A-1. Data Sheets

Type	Description	Page
ADC0817	8-Bit µP Compatible A/D Converters	A-3
CD4001B	COS/MOS NOR Gates	A-4
CD4011B	COS/MOS NAND Gates	A-5
CD4028A	COS/MOS BCD-to-Decimal Decoder	A-6
CD4050A	COS/MOS Hex Buffer/Converters	A-7
CD4053B	COS/MOS Analog Multiplexers/Demultiplexers	A-7
CD4069UB	COS/MOS Hex Inverter	A-8
CD4071B	COS/MOS OR Gates	A-9
CD4094B	COS/MOS 8-Stage Shift-and-Store Bus Register	A-10
CD4098B	COS/MOS Dual Monostable Multivibrator	A-11
CD4514B	COS/MOS 4-Bit Latch/4-to-16 Line Decoders	A-11
CD4538B	COS/MOS Dual Precision Monostable Multivibrator	A-12
DG211	Quad Monolithic SPST CMOS Analog Switch	A-13
LF347	Quad JFET Operation Amplifier	A-14
LH0002CH	Operational (Current) Amplifier/Buffer	A-15
LM111H	Voltage Comparator	A-16
LM324	Low Power Quad Operational Amplifiers	A-17
LM339	Low Power Low Offset Voltage Quad Comparators	A-17
LM358	Operational Amplifier	A-18
LM1458	Dual Operational Amplifier/Buffer	A-19
MC1496N	Balanced Modulator/Demodulator	A-20
MC1733	Differential Video Amplifier	A-22
MC12013	Two-Modulus Prescaler	A-23
MC145156	Serial Input PLL Frequency Synthesizer	A-24
NE571	Compander	A-25
NE-SA594	Vacuum Fluorescent Display Driver	A-26
RAY-6	Frequency Mixer	A-27
SBL-1	Standard Level (+ 7 dBm LO) Double-Balanced Mixers	A-28
SCN2681	Dual Universal Asynchronous Receiver/Transmitter (DUART)	A-29
SN74165	Parallel-Load 8-Bit Shift Registers	A-31

Table A-1. Data Sheets (Cont.)

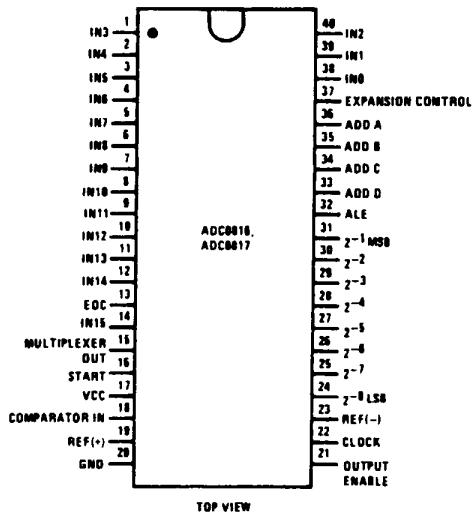
Type	Description	Page
SN74LS74N	Dual D-Type Positive-Edge-Triggered Flip-Flops with Preset and Clear	A-32
SN74L90	Decade, Divide-By-Twelve, and Binary Counter	A-32
SN74LS122	Retriggerable Monostable Multivibrators with Clear	A-33
SN74LS168A	Synchronous 4-Bit Up/Down Counters	A-34
SN74LS244	Octal Buffers and line Drivers with 3-State Outputs	A-36
SN74LS245	Octal Bus Transceivers with 3-State Outputs	A-36
SN74LS373, SN74LS374	Octal D-type Transparent Latches and Edge-Triggered Flip-Flops	A-37
TL072	Low-Noise JFET-Input Operational Amplifiers	A-38
3045	Transistor Array	A-39
74XX00	Quad 2-Input NAND	A-40
74XX02	Quad 2-Input NOR Gate	A-41
74XX04	Hex Inverter	A-42
74XX14	Hex Schmitt-Trigger Inverter	A-43
74XX27	Triple 3-Input NOR	A-44
74XX73 (74LS73 or 74HC73)	Dual JK Negative Edge-Triggered Flip-Flop	A-45
74XX109 (74LS109 or 74HC109)	Dual JK Positive Edge-Triggered Flip-Flop	A-46
74XX174 (74LS174, 74HC174)	Hex D Flip-Flop	A-47
8035	Single Component 8-Bit Microcomputer	A-48
8085	8-Bit Microprocessor	A-50
8155	RAM; Triple I/O; Timer	A-53
8255A/ 8255VA-5	Programmable Peripheral Interface	A-56

ADC0817 8-Bit μP Compatible A/D Converters with 16-Channel Multiplexer

General Description

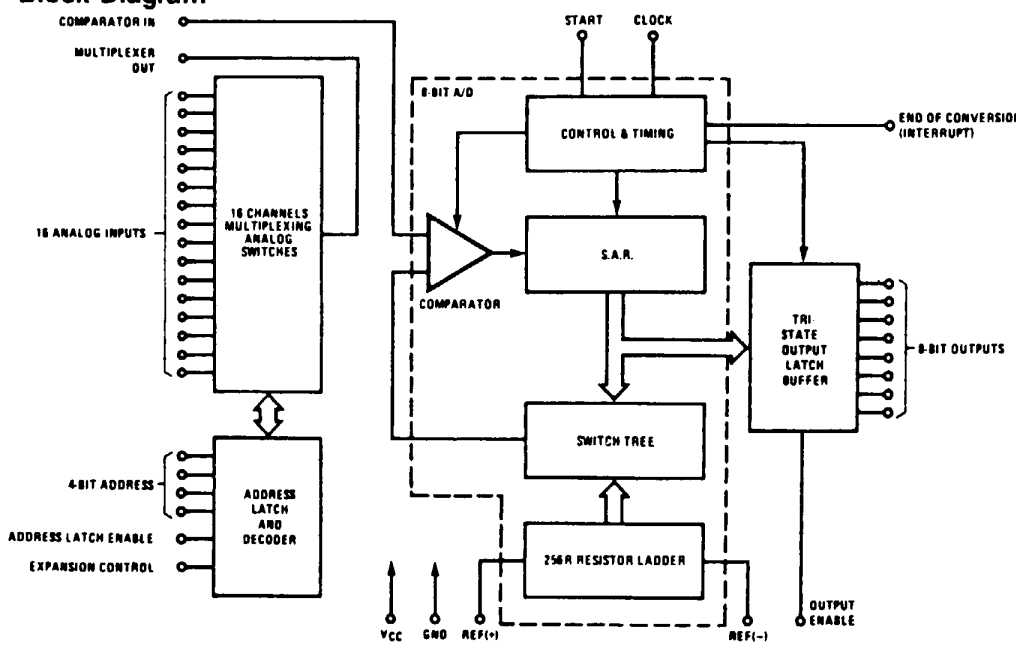
The ADC0816, ADC0817 data acquisition component is a monolithic CMOS device with an 8-bit analog-to-digital converter, 16-channel multiplexer and microprocessor compatible control logic. The 8-bit A/D converter uses successive approximation as the conversion technique. The converter features a high impedance chopper stabilized comparator, a 256R voltage divider with analog switch tree and a successive approximation register. The 16-channel multiplexer can directly access any one of 16-single-ended analog signals, and provides the logic for additional channel expansion. Signal conditioning of any analog input signal is eased by direct access to the multiplexer output, and to the input of the 8-bit A/D converter.

Dual-In-Line Package



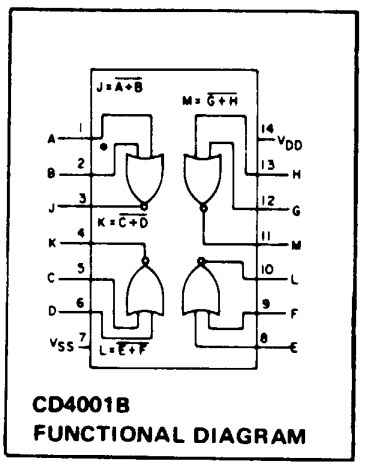
TOP VIEW

Block Diagram



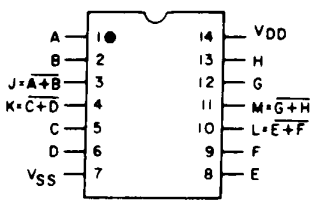
CD4001B TYPES
COS/MOS NOR GATES

High Voltage Types (20-Volt Rating)



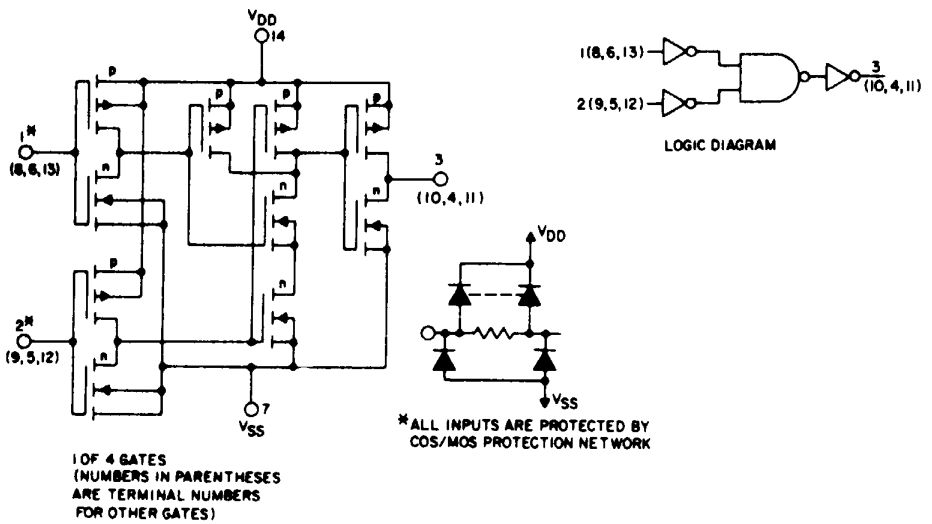
CD4001B
FUNCTIONAL DIAGRAM

TERMINAL ASSIGNMENTS (TOP VIEW)



NC = NO CONNECTION

CD4001B



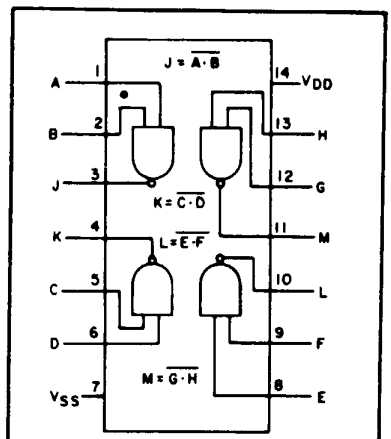
Schematic and logic diagrams for CD4001B.

CD4011B TYPES
COS/MOS NAND GATES

High Voltage Types (20-Volt Rating)

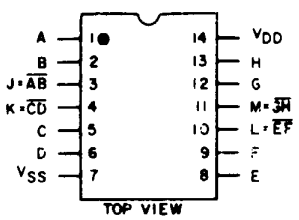
CD4011B, NAND gates provide the system designer with direct implementation of the NAND function and supplement the existing family of COS/MOS gates. All inputs and outputs are buffered.

The CD4011B, types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat packages (k suffix)and in chip form (H suffix).

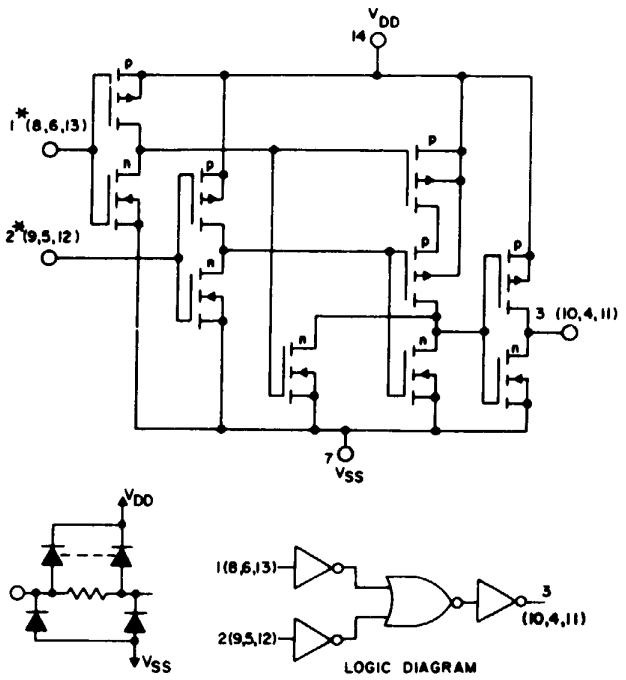


CD4011B
FUNCTIONAL DIAGRAM

TERMINAL ASSIGNMENTS



CD4011B



* ALL INPUTS ARE PROTECTED BY COS/MOS PROTECTION NETWORK

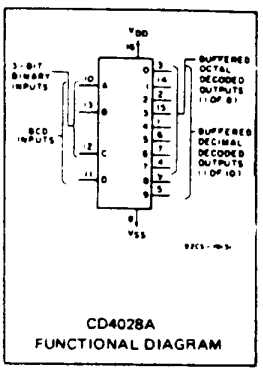
1 OF 4 GATES (NUMBERS IN PARENTHESES ARE TERMINAL NUMBERS FOR OTHER GATES)

Schematic and logic diagrams for CD4011B.

CD4028A Types
COS/MOS
BCD-to-Decimal Decoder

The RCA-CD4028A types are BCD-to-decimal or binary-to-octal decoders consisting of pulse-shaping circuits on all 4 inputs, decoding-logic gates, and 10 output buffers. A BCD code applied to the four inputs, A to D, results in a high level at the selected one of 10 decimal decoded outputs. Similarly, a 3-bit binary code applied to inputs A through C is decoded in octal code at output 0 to 7. A high-level signal at the D input inhibits octal decoding and causes outputs 0 through 7 to go low. If unused, the D input must be connected to V_{SS}. High drive capability is provided at all outputs to enhance dc and dynamic performance in high fan-out applications.

These types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), and in chip form (H suffix).



CD4028A
FUNCTIONAL DIAGRAM

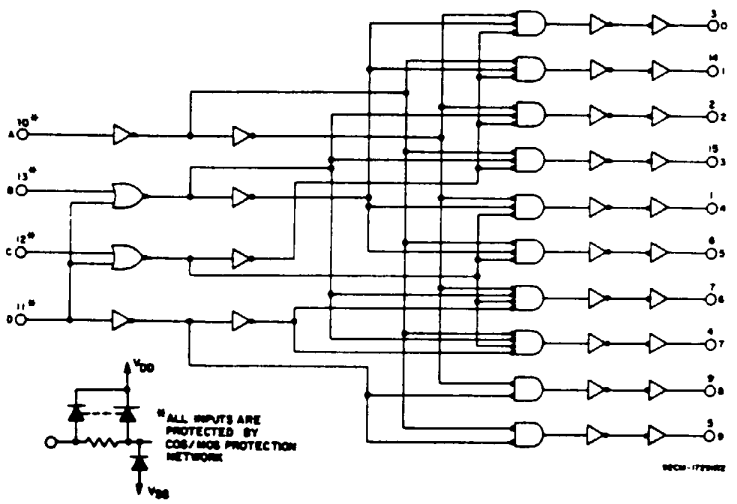


TABLE I – TRUTH TABLE

D	C	B	A	0	1	2	3	4	5	6	7	8	9	
0	0	0	0	1	0	0	0	0	0	0	0	0	0	*
0	0	0	1	0	1	0	0	0	0	0	0	0	0	*
0	0	1	0	0	0	1	0	0	0	0	0	0	0	*
0	0	1	1	0	0	0	1	0	0	0	0	0	0	*
0	1	0	0	0	0	0	0	1	0	0	0	0	0	*
0	1	0	1	0	0	0	0	0	1	0	0	0	0	*
0	1	1	0	0	0	0	0	0	0	1	0	0	0	*
0	1	1	1	0	0	0	0	0	0	0	1	0	0	*
1	0	0	0	0	0	0	0	0	0	0	0	1	0	*
1	0	0	1	0	0	0	0	0	0	0	0	0	1	*
1	0	1	0	0	0	0	0	0	0	0	0	1	0	**
1	0	1	1	0	0	0	0	0	0	0	0	0	1	**
1	1	0	0	0	0	0	0	0	0	0	0	1	0	**
1	1	0	1	0	0	0	0	0	0	0	0	0	1	**
1	1	1	0	0	0	0	0	0	0	0	0	1	0	**
1	1	1	1	0	0	0	0	0	0	0	0	0	1	**

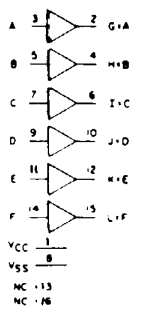
* WHERE 1 = HIGH LEVEL
0 = LOW LEVEL

** EXTRAORDINARY STATES

CD4050A

COS/MOS Hex Buffer/Converters

The CD4049A and CD4050A are inverting and non-inverting hex buffers, respectively, and feature logic-level conversion using only one supply voltage (V_{CC}). The input-signal high level (V_{IH}) can exceed the V_{CC} supply voltage when these devices are used for logic-level conversions. These devices are intended for use as COS/MOS to DTL/TTL converters and can drive directly two DTL/TTL loads. (V_{CC}=5 V, V_{OL} ≤0.4 V, and I_{ON} ≥3.2 mA.)



CD4050A

CD4053B

COS/MOS Analog Multiplexers/Demultiplexers

RCA-CD4051B, CD4052B, and CD4053B analog multiplexers/demultiplexers are digitally controlled analog switches having low ON impedance and very low OFF leakage current. Control of analog signals up to 20 V peak-to-peak can be achieved by digital signal amplitudes of 4.5 to 20 V (if V_{DD}-V_{SS} = 3 V, a V_{DD}-V_{EE} of up to 13 V can be controlled; for V_{DD}-V_{EE} level differences above 13 V, a V_{DD}-V_{SS} of at least 4.5 V is required). For example, if V_{DD} = +5 V, V_{SS} = 0, and V_{EE} = −13.5 V, analog signals from −13.5 V to +4.5 V can be controlled by digital inputs of 0 to 5 V. These multiplexer circuits dissipate extremely low quiescent power over the full V_{DD}-V_{SS} and V_{DD}-V_{EE} supply-voltage ranges, independent of the logic state of the control signals. When a logic "1" is present at the inhibit input terminal all channels are off.

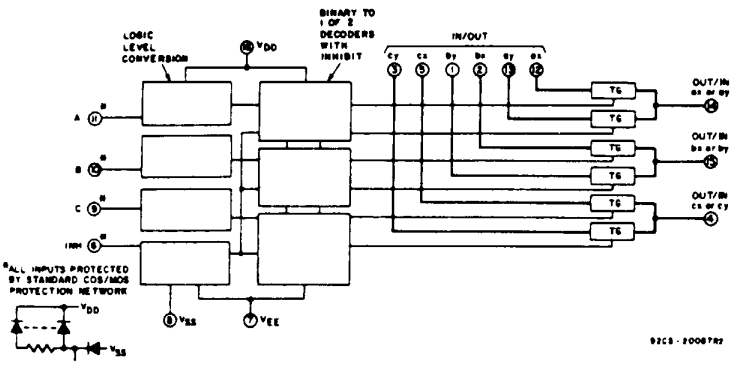
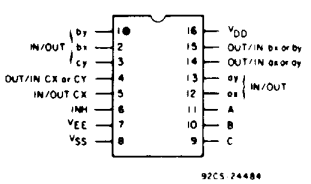


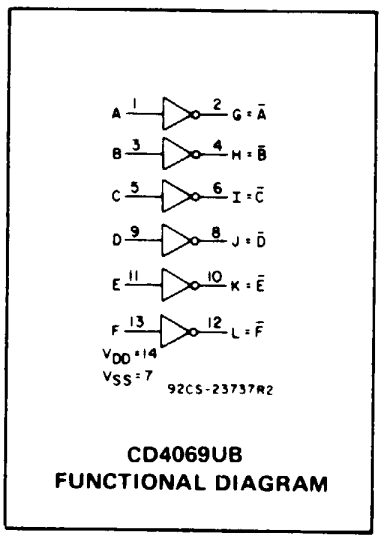
Fig. 3 – Functional diagram of CD4053B.



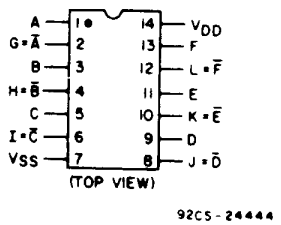
CD4053B

Terminal Assignment

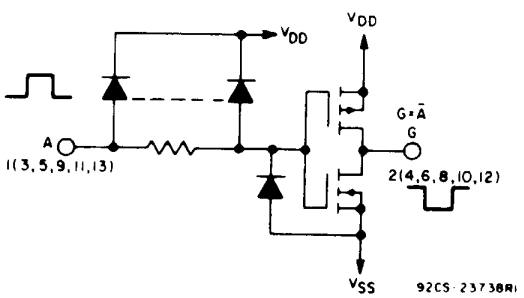
CD4069UB TYPES
COS/MOS HEX INVERTER



CD4069UB
FUNCTIONAL DIAGRAM



CD4069UB terminal assignment.

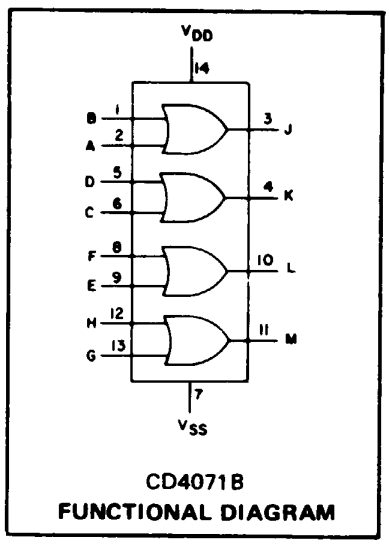


Schematic diagram of one of six identical inverters.

CD4071B TYPES
COS/MOS OR GATES

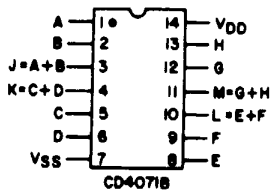
High Voltage Types (20-Volt Rating)

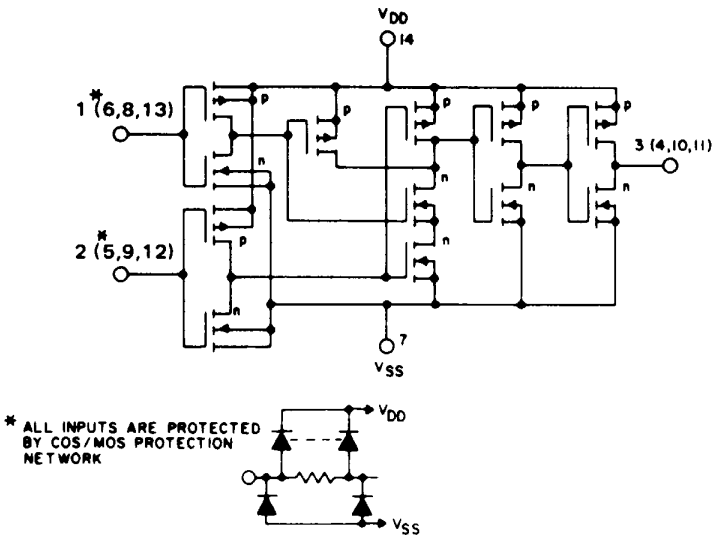
CD4071B Quad 2-Input OR Gate



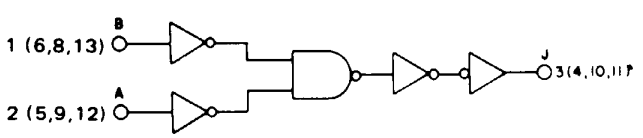
CD4071B
FUNCTIONAL DIAGRAM

TERMINAL ASSIGNMENTS (TOP VIEW)





Schematic diagram for CD4071B (1 of 4 identical gates).



Logic diagram for CD4071B (1 of 4 identical gates).

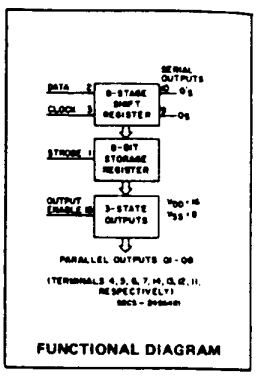
CD4094B

COS/MOS
8-Stage Shift-and-Store Bus Register

High-Voltage Types (20-Volt Rating)

The RCA-CD4094B is an 8-stage serial shift register having a storage latch associated with each stage for strobing data from the serial input to parallel buffered 3-state outputs. The parallel outputs may be connected directly to common bus lines. Data is shifted on positive clock transitions. The data in each shift register stage is transferred to the storage register when the STROBE input is high. Data in the storage register appears at the outputs whenever the OUTPUT-ENABLE signal is high.

Two serial outputs are available for cascading a number of CD4094B devices. Data is available at the Q_S serial output terminal on positive clock edges to allow for high-speed operation in cascaded systems in which the clock rise time is fast. The same serial information, available at the Q'_S terminal on the next negative clock edge, provides a means for cascading CD4094B devices when the clock rise time is slow.



FUNCTIONAL DIAGRAM

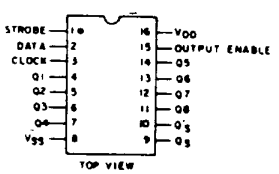


Fig. 1 – Terminal assignment.

TRUTH TABLE

CL▲	Output Enable	Strobe	Data	Parallel Outputs		Serial Outputs	
				Q1	QN	QS*	Q'S
⌐	0	X	X	OC	OC	Q7	NC
⌙	0	X	X	OC	OC	NC	Q7
⌐	1	0	X	NC	NC	Q7	NC
⌐	1	1	0	0	Q_{N-1}	Q7	NC
⌐⌙	1	1	1	1	Q_{N-1}	Q7	NC
⌙	1	1	1	NC	NC	NC	Q7

▲ = Level Change
X = Don't Care
NC = No Change
OC = Open Circuit

Logic 1 ≡ High
Logic 0 ≡ Low

* At the positive clock edge information in the 7th shift register stage is transferred to the 8th register stage and the Q_S output

CD4098B Types

COS/MOS Dual Monostable Multivibrator

High-Voltage Types (20-Volt Rating)

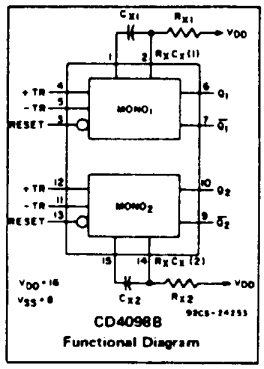
The RCA-CD4098B dual monostable multivibrator provides stable retriggerable/resettable one-shot operation for any fixed-voltage timing application.

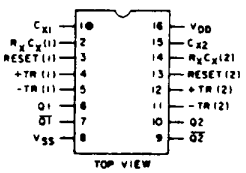
An external resistor (R_X) and an external capacitor (C_X) control the timing for the circuit. Adjustment of R_X and C_X provides a wide range of output pulse widths from the Q and $\overline{Q}$ terminals. The time delay from trigger input to output transition (trigger propagation delay) and the time delay from reset input to output transition (reset propagation delay) are independent of R_X and C_X.

Leading-edge-triggering (+TR) and trailing edge-triggering (−TR) inputs are provided for triggering from either edge of an input pulse.

In normal operation the circuit triggers (extends the output pulse one period) on the application of each new trigger pulse. For operation in the non-retriggerable mode, $\overline{Q}$ is connected to −TR when leading-edge triggering (+TR) is used or Q is connected to +TR when trailing-edge triggering (−TR) is used.

The time period (T) for this multivibrator can be approximated by: $T_X = \frac{1}{2} R_X C_X$ for $C_X \geq 0.01\ \mu F$.





TERMINALS 1, 8, 15 ARE ELECTRICALLY CONNECTED INTERNALLY

TERMINAL ASSIGNMENT

CD4514B

COS/MOS 4-Bit Latch/4-to-16 Line Decoders

High-Voltage Types (20-Volt Rating)
CD4514B Output "High" on Select

The RCA-CD4514B and -CD4515B consist of a 4-bit strobed latch and a 4-to-16-line decoder. The latches hold the last input data presented prior to the strobe transition from 1 to 0. Inhibit control allows all outputs to be placed at 0(CD4514B) or 1(CD4515B) regardless of the state of the data or strobe inputs.

The decode truth table indicates all combinations of data inputs and appropriate selected outputs.

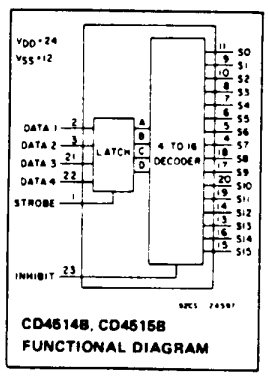
These devices are similar to industry types MC14514 and MC14515.

The CD4514B and CD4515B types are supplied in 24-lead hermetic dual-in-line ceramic packages (D and F suffixes), 24-lead dual-in line plastic packages (E suffix), and in chip form (H suffix).

DECODE TRUTH TABLE (Strobe = 1)

INHIBIT	DECODER INPUTS				SELECTED OUTPUT CD4514B = Logic 1 (High) CD4515B = Logic 0 (Low)
	D	C	B	A	
0	0	0	0	0	S0
0	0	0	0	1	S1
0	0	0	1	0	S2
0	0	0	1	1	S3
0	0	1	0	0	S4
0	0	1	0	1	S5
0	0	1	1	0	S6
0	0	1	1	1	S7
0	1	0	0	0	S8
0	1	0	0	1	S9
0	1	0	1	0	S10
0	1	0	1	1	S11
0	1	1	0	0	S12
0	1	1	0	1	S13
0	1	1	1	0	S14
0	1	1	1	1	S15
1	X	X	X	X	All Outputs = 0, CD4514B All Outputs = 1, CD4515B

X = Don't Care Logic 1 = high Logic 0 = low



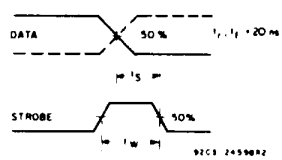


Fig. 14 – Waveforms for setup time and strobe pulse width.

CD4538B TYPES
COS/MOS DUAL PRECISION MONOSTABLE MULTIVIBRATOR

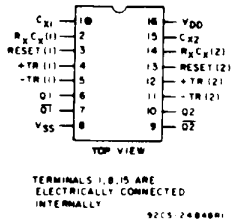
High-Voltage Types (20-Volt Rating)

The RCA-CD4538B dual precision monostable multivibrator provides stable retriggerable/resettable one-shot operation for any fixed-voltage timing application.

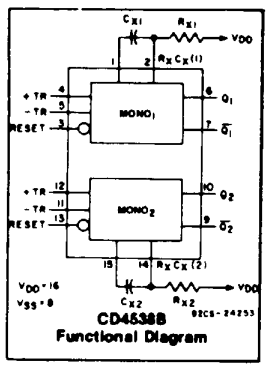
An external resistor (R_X) and an external capacitor (C_X) control the timing and accuracy for the circuit. Adjustment of R_X and C_X provides a wide range of output pulse widths from the Q and $\overline{Q}$ terminals. The time delay from trigger input to output transition (trigger propagation delay) and the time delay from reset input to output transition (reset propagation delay) are independent of R_X and C_X. Precision control of output pulse widths is achieved through linear CMOS techniques.

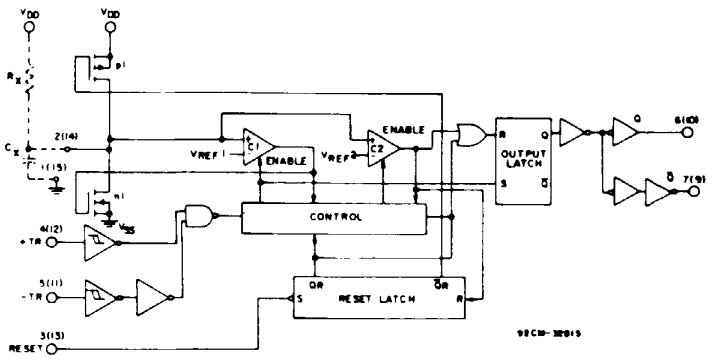
Leading-edge-triggering (+TR) and trailing-edge-triggering (−TR) inputs are provided for triggering from either edge of an input pulse. An unused +TR input should be tied to V_{SS}. An unused −TR input should be tied to V_{DD}. A RESET (on low level) is provided for immediate termination of the output pulse or to prevent output pulses when power is turned on. An unused RESET input should be tied to V_{DD}. However, if an entire section of the CD4538B is not used, its inputs must be tied to either V_{DD} or V_{SS}.

In normal operation the circuit triggers (extends the output pulse one period) on the application of each new trigger pulse.



TERMINAL ASSIGNMENT





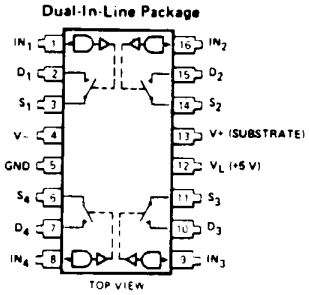
Logic diagram (½ of device shown).

DG211
Quad Monolithic SPST CMOS Analog Switch

The DG211 is a 4-channel single pole single throw analog switch which employs CMOS technology to insure low and nearly constant ON resistance over the entire analog signal range. The switch will conduct current in either direction with no offset voltage in the ON condition, and block voltages up to 30 V peak-to-peak in the OFF condition. The ON-OFF state of each switch is controlled by a driver. With a logic "0" at the input to the driver (0 V to 0.8 V) the switch will be ON, and a logic "1" (2.4 V to 15 V) will turn the switch OFF. The input can thus be directly interfaced with TTL, DTL, RTL, CMOS and certain PMOS circuits. Switch action is break-before-make. Logic inputs can directly connect to op-amp output swings.

PIN CONFIGURATION

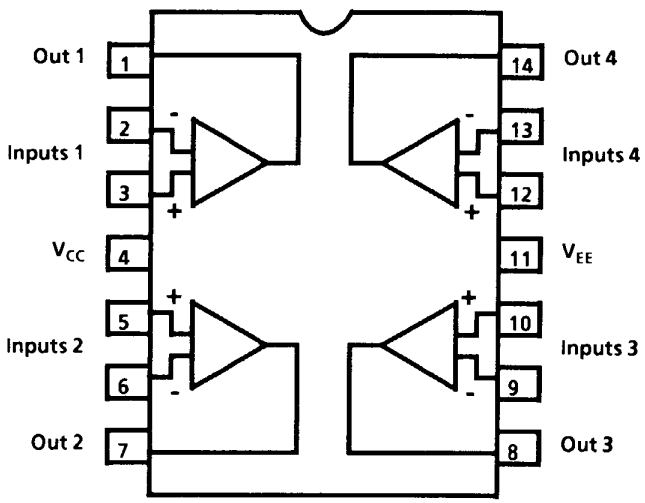
Dual-In-Line Package



LOGIC	SWITCH
0	ON
1	OFF

SWITCH OPEN FOR LOGIC "1" INPUT (POSITIVE LOGIC)

LF347
QUAD JFET OPERATION AMPLIFIER



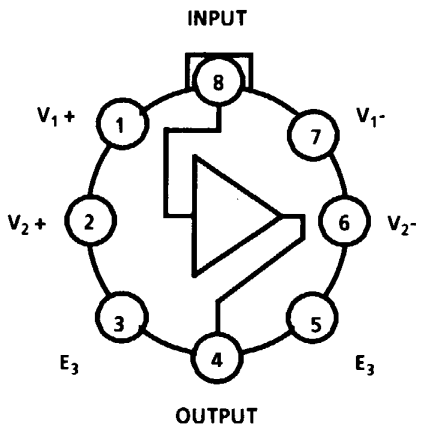
(Top View)

Maximum Ratings

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC} V_{EE}	+18 -18	V
Differential Input Voltage	V_{ID}	+/-30	V
Input Voltage Range	V_{IDR}	+/-15	V
Output Short Circuit Duration	t_S	Continuous	
Power Dissipation at T_A = +25°C	P_D	900	mW
Derate above T_A = +25°C	$1/\theta_{JA}$	10	mW/°C
Operating Ambient Temperature Range	T_A	0 to +70	°C
Operating Junction Temperature Range	T_J	115	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

LH0002CH
OPERATIONAL (CURRENT) AMPLIFIER/BUFFER

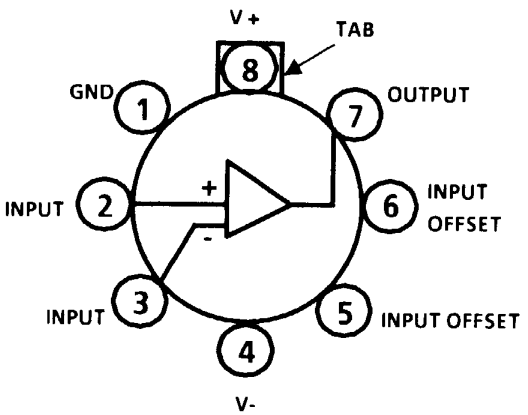
Metal Can Package



Maximum Ratings

Supply Voltage	+ 22V
Power Dissipation	600mW
Input Voltage	= to Power Supply Voltage
Storage Temperature	-65°C to + 150°C
Operating Temperature	0°C to + 85°C
Steady State Output Current	+ /-100 mA
Pulsed Output Current	+ /- 400 mA

LM111H
VOLTAGE COMPARATOR



NOTE: PIN 4 IS CONNECTED TO CASE

Maximum Ratings

Total Supply Voltage	36V
Output to Negative Supply Voltage	50V
Ground to Negative Supply Voltage	30V
Differential Input Voltage	+/-30V
Input Voltage	+/-15V
Power Dissipation	500mW
Operating Temperature Range	-55°C to 125°C
Storage Temperature Range	-66°C to 150°C

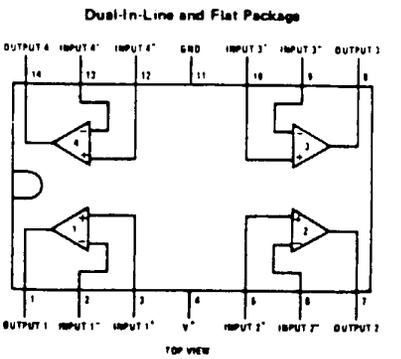
LM324
Low Power Quad Operational Amplifiers

General Description

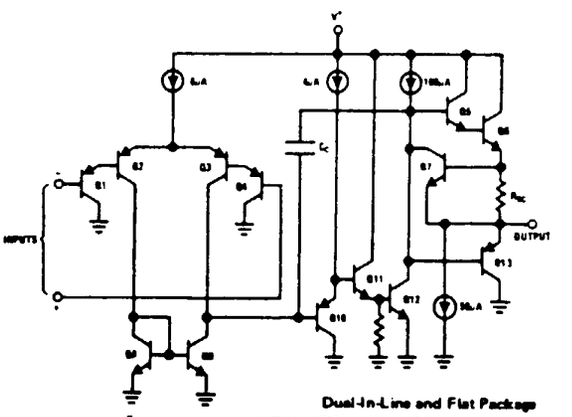
The LM124 series consists of four independent, high gain, internally frequency compensated operational amplifiers which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

Application areas include transducer amplifiers, dc gain blocks and all the conventional op amp circuits which now can be more easily implemented in single power supply systems. For example, the LM124 series can be directly operated off of the standard +5 V_{DC} power supply voltage which is used in digital systems and will easily provide the required interface electronics without requiring the additional ±15 V_{DC} power supplies.

Connection Diagram



Schematic Diagram (Each Amplifier)

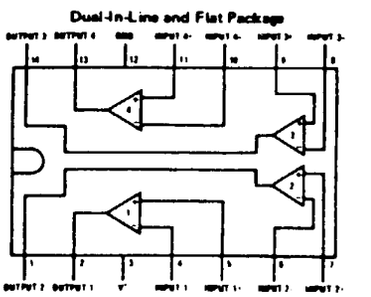


LM339
Low Power Low Offset Voltage Quad Comparators

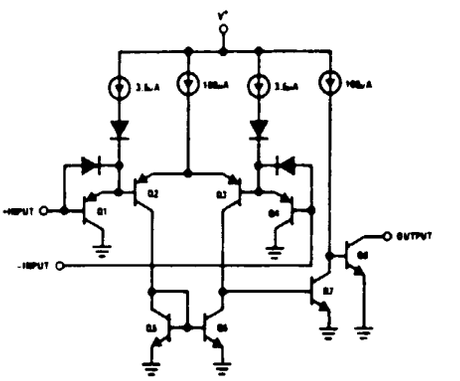
General Description

The LM139 series consists of four independent precision voltage comparators with an offset voltage specification as low as 2 mV max for all four comparators. These were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common-mode voltage range includes ground, even though operated from a single power supply voltage.

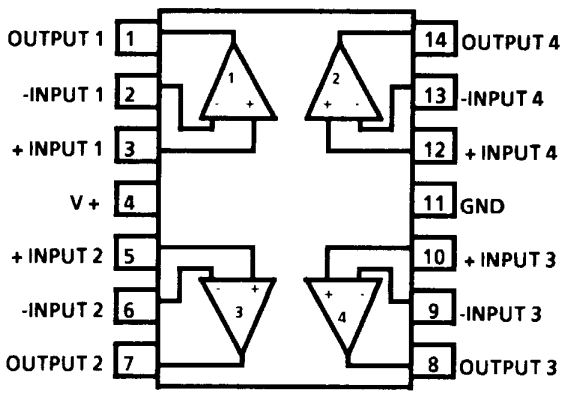
Application areas include limit comparators, simple analog to digital converters; pulse, squarewave and time delay generators; wide range VCO; MOS clock timers; multivibrators and high voltage digital logic gates. The LM139 series was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, they will directly interface with MOS logic– where the low power drain of the LM339 is a distinct advantage over standard comparators.



Schematic and Connection Diagrams



LM358
OPERATIONAL AMPLIFIER



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V +	Supply voltage	32 or +/- 16	Vdc
	Differential input voltage	32	Vdc
	Input voltage	-0.3 to +32	Vdc
	Power dissipation[1]		
	T package	680	mW
	N package	570	mW
	F package	900	mW
	Output short-circuit to GND		
	1 amplifier[2]	Continuous	
	V + < 15 Vdc and TA = 25°C		
	Input current (VIN < -0.3V)[3]	50	mA
	Oprating temperature range		
	LM324A, LM324, LM358	0 to +70	°C
	LM224A, LM224, LM258	-25 to +85	°C
	SA5334	-40 to +85	°C
	LM124A, LM124, LM158	-55 to +125	°C
	Storage temperature range	-65 to +150	°C
	Lead temperature (soldering, 10sec)	300	°C

LM1458

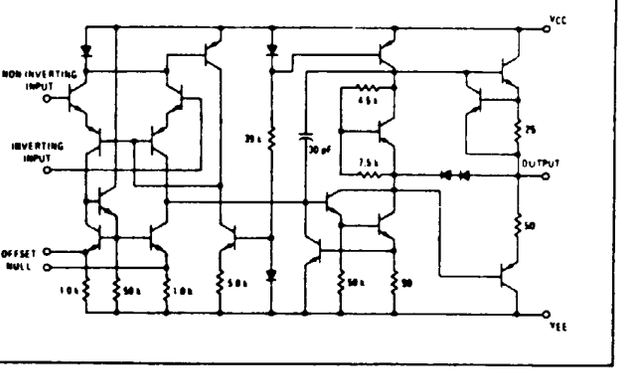
Dual Operational Amplifier/Buffer

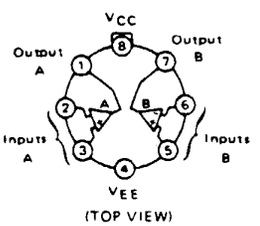
general description

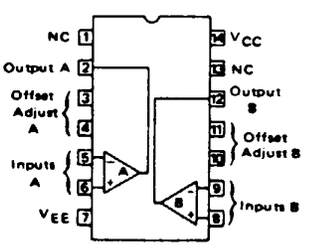
The LM1558 and the LM1458 are general purpose dual operational amplifiers. The two amplifiers share a common bias network and power supply leads. Otherwise, their operation is completely independent. Features include:

- No frequency compensation required
- Short-circuit protection
- Wide common-mode and differential voltage ranges
- Low-power consumption
- 8-lead TO-5 and 8-lead mini DIP
- No latch up when input common mode range is exceeded

EQUIVALENT CIRCUIT SCHEMATIC



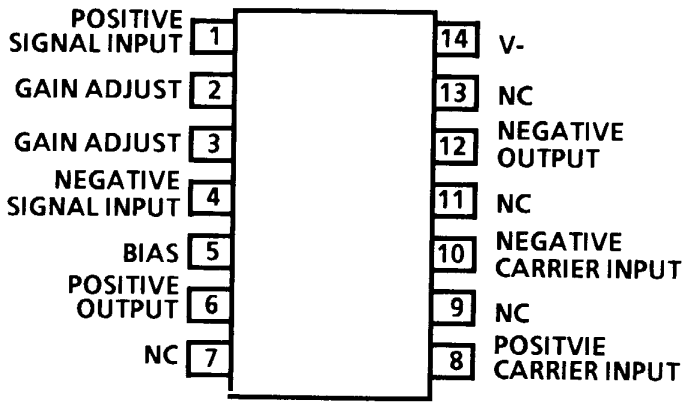




MC1496N
BALANCED MODULATOR/DEMODULATOR

DESCRIPTION

The MC1496N is a monolithic Double-Balanced Modulator/Demodulator designed for use where the output voltage is a product of an input voltage (signal) and a switched function (carrier).



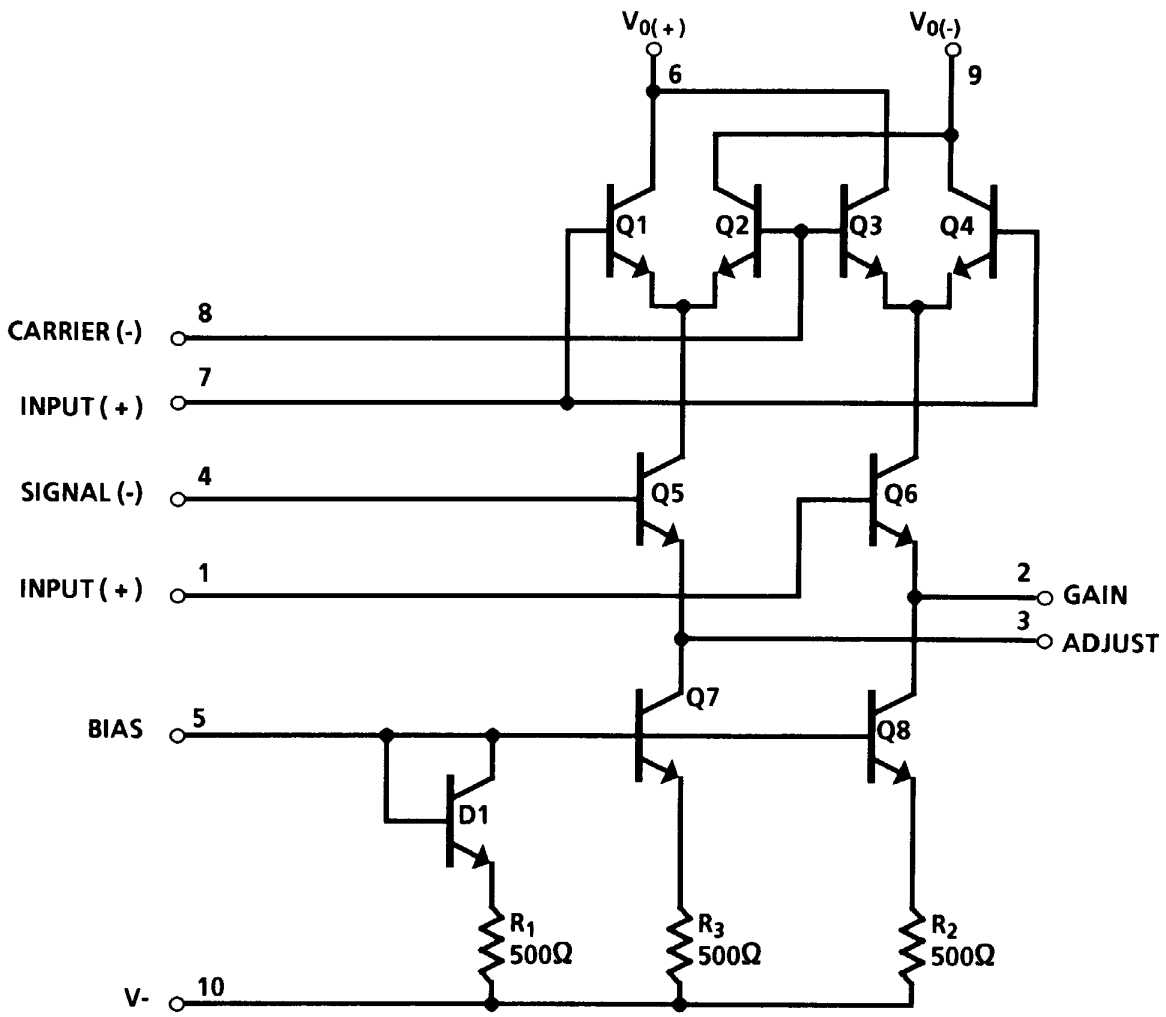
ABSOLUTE MAXIMUM RATINGS

PARAMETERS	RATING	UNIT
Applied voltage 1,2	30	V
Differential input signal (V_7-V_8)	+/- 5.0	V
Differential input signal (V_4-V_1)	(5 +/- I_5 Re)	V
Input signal (V_2-V_1, V_3-V_4)	5.0	V
Bias current (I_5)	10	mA
Power dissipation (pkg. limitation)		
K package	680	mW
Derate above 25°C	5.4	mW/°C
A package (T0-116)	900	mW
Derate above 25oC	7.2	mW/°C
Operating temperature range	-55 to + 125	°C
Storage temperature range	-65 to + 150	°C

NOTES

1. Voltage applied between pins 6-7, 8-1, 9-7, 9-8, 7-4, 7-1, 8-4, 6-8, 2-5, 3-5.
2. Pin number references pertain to K package pinout only.

MC1496N
BALANCED MODULATOR/DEMODULATOR



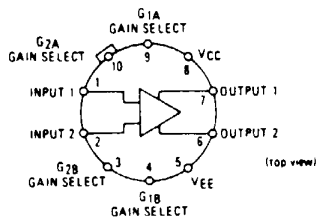
EQUIVALENT SCHEMATIC

MC1733

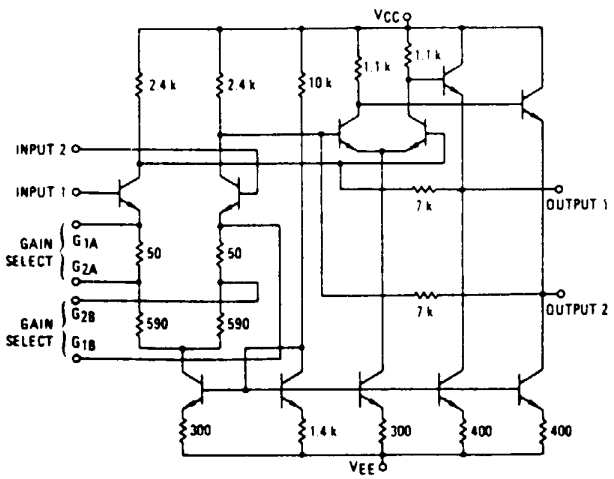
DIFFERENTIAL VIDEO AMPLIFIER

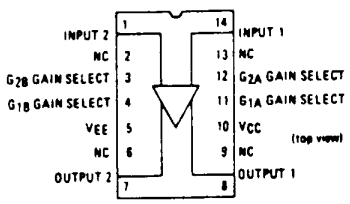
. . . a wideband amplifier with differential input and differential output. Gain is fixed at 10, 100, or 400 without external components or, with the addition of one external resistor, gain becomes adjustable from 10 to 400.

- Bandwidth – 120 MHz typical @ A_{vd} = 10
- Rise Time – 2.5 ns typical @ A_{vd} = 10
- Propagation Delay Time – 3.6 ns typical @ A_{vd} = 10



EQUIVALENT CIRCUIT SCHEMATIC



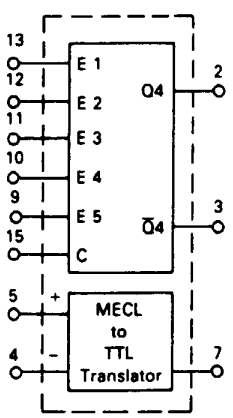


MC12013

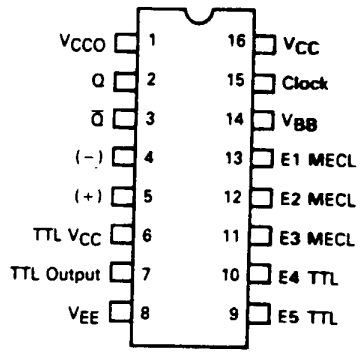
TWO-MODULUS PRESCALER

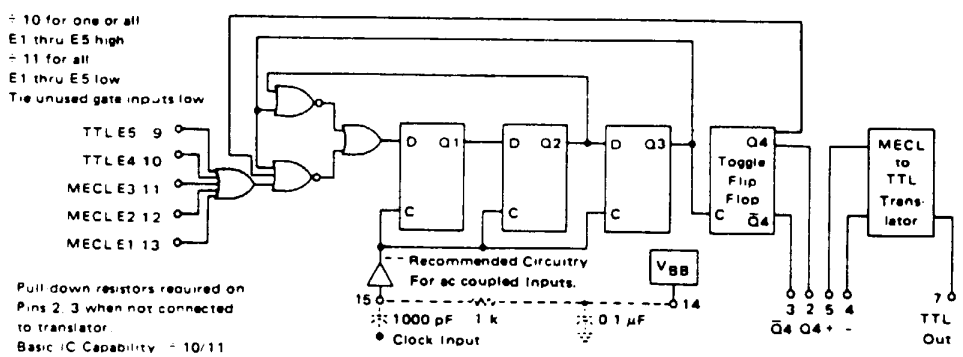
These devices are two-modulus prescalers which will divide by 5 and 6, 8 and 9, and 10 and 11, respectively. A MECL-to-TTL translator is provided to interface directly with the MC12014 Counter Control Logic. In addition, there is a buffered clock input and MECL bias voltage source.

LOGIC DIAGRAM



V_{CCO} = pin 1
V_{CC} = pin 16
V_{EE} = pin 8





MC145156

SERIAL INPUT PLL FREQUENCY SYNTHESIZER

The MC145156 is one of a family of LSI PLL frequency synthesizer parts from Motorola CMOS. The family includes devices having serial, parallel and 4-bit data bus programmable inputs. Options include single- or dual-modulus capability, transmit/receive offsets, choice of phase detector types and choice of reference divider integer values.

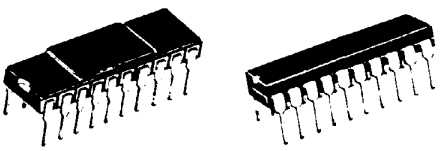
The MC145156 is programmed by a clocked, serial input, 19-bit data stream. The device features consist of a reference oscillator, selectable-reference divider, digital-phase detector, 10-bit programmable divide-by-N counter, 7-bit programmable ÷ A counter and the necessary shift register and latch circuitry for accepting the serial input data. When combined with a loop filter and VCO, the MC145156 can provide all the remaining functions for a PLL frequency synthesizer operating up to the device's frequency limit. For higher VCO frequency operation, a down mixer or a dual modulus prescaler can be used between the VCO and MC145156.

- General Purpose Applications —
  CATV — TV Tuning
  AM/FM Radios — Scanning Receivers
  Two-Way Radios — Amateur Radio
- Low Power Drain
- 3.0 to 9.0 Vdc Supply Range
- >30 MHz Typical Input Capability @ 5 Vdc
- 8 User Selectable Reference Divider Values — 8, 64, 128, 256, 640, 1000, 1024, 2048
- On- or Off-Chip Reference Oscillator Operation with Buffered Output
- Lock Detect Signal
- Two Open-Drain Switch Outputs
- Dual Modulus/Serial Programming
- ÷N Range = 3 to 1023
- "Linearized" Digital Phase Detector Enhances Transfer Function Linearity
- Two Error Signal Options —
  Single Ended (Three-State)
  Double Ended

CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

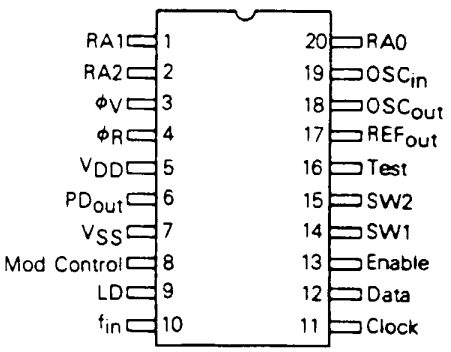
SERIAL INPUT PLL FREQUENCY SYNTHESIZER

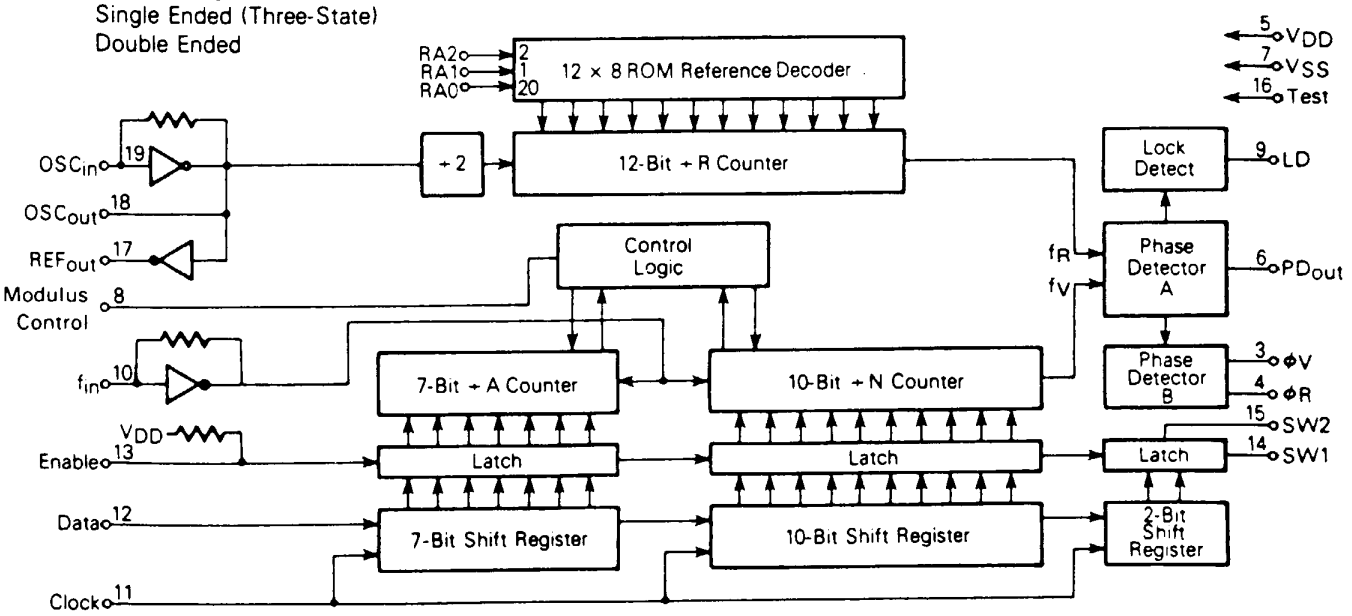


L SUFFIX
CERAMIC PACKAGE
CASE 729-01

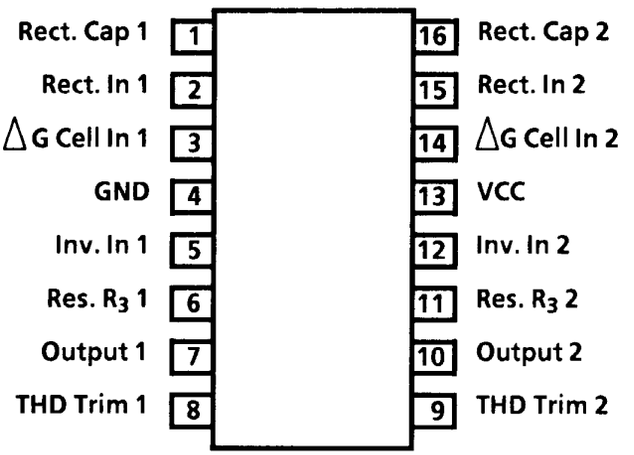
P SUFFIX
PLASTIC PACKAGE
CASE 738-02

PIN ASSIGNMENT

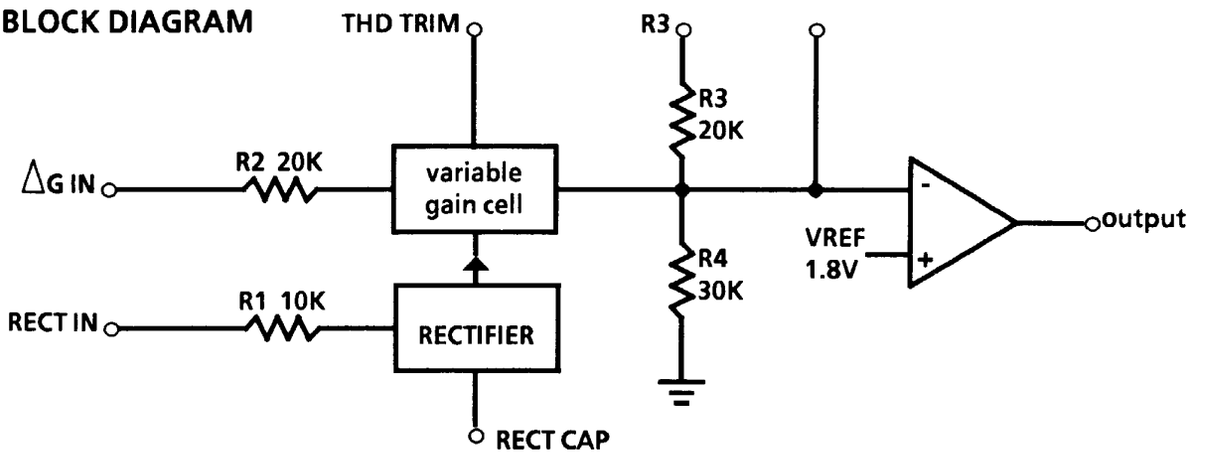




NE571
COMPANDER



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

	PARAMETERS	RATING	UNIT
	Positive supply		Vdc
	570	24	
	571	18	
T_A	Operating temperature range	-40 TO + 70	°C
P_D	Power dissipation	400	mW

NE-SA594
VACUUM FLUORESCENT DISPLAY DRIVER

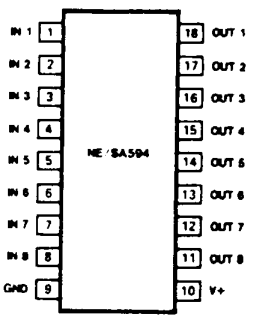
DESCRIPTION

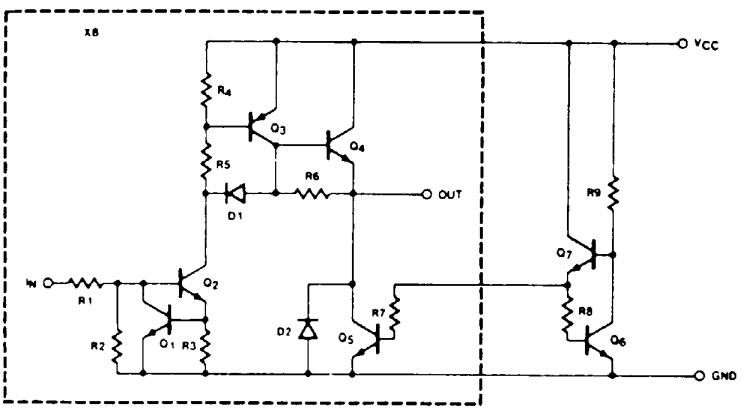
The NE/SA594 is a display driver interface for vacuum fluorescent displays. The device is comprised of 8 drivers and a bias network and is capable of driving the digits and/or segments of most vacuum fluorescent displays.

The inputs are designed to be compatible with TTL, DTL, NMOS, PMOS or CMOS output circuitry.

There is an active pull-down circuit on each output so that display ghosting is minimized and no external components are required for most fluorescent display applications.

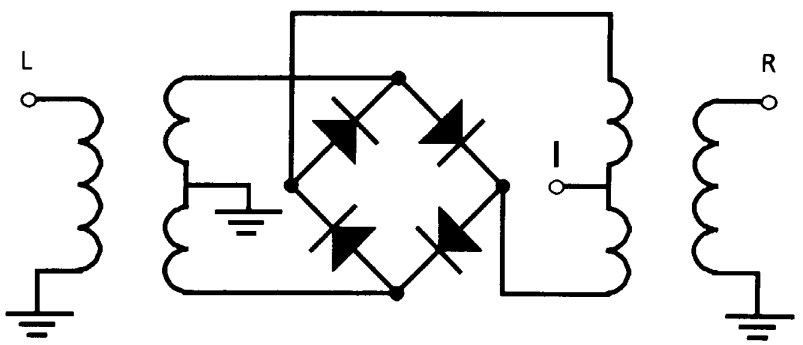
N, F PACKAGE





RAY-6
FREQUENCY MIXER

Schematic



PIN ASSIGNMENTS

FUNCTION	PIN
60	8
RF	1
IF	3,4 (connected externally)
GND	2,5,6,7

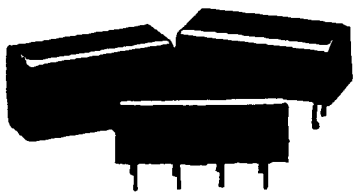
CHARACTERISTICS

Frequency (MHz)	LO/RF f_L - f_u	0.01-50
	IF	DC50
Conversion Loss (dB)	Mid-Band: Typical	5.5
	Maximum	7.5
	Total Range Typical	6.5
	Maximum	8.5
LO-RF Isolation (dB)	Low Range (f_L to $10f_L$) Typical	60
	Minimum	50
	Mid Range ($10f_L$ to $f_u/2$) Typical	45
	Minimum	30
	Upper Range ($f_u/2$ to f_u) Typical	35
	Minimum	25
LO-IF Isolation (dB)	Low Range (f_L to $10f_L$) Typical	60
	Minimum	45
	Mid Range ($10f_L$ to $f_u/2$) Typical	40
	Minimum	25
	Upper Range (f_u 2 to f_u) Typical	30
	Minimum	20

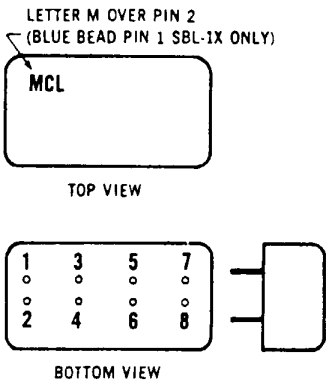
SBL-1

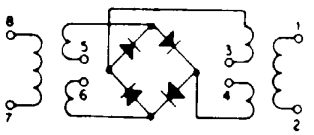
Standard Level (+7 dBm LO) DOUBLE-BALANCED MIXERS

SBL SERIES



CONNECTIONS





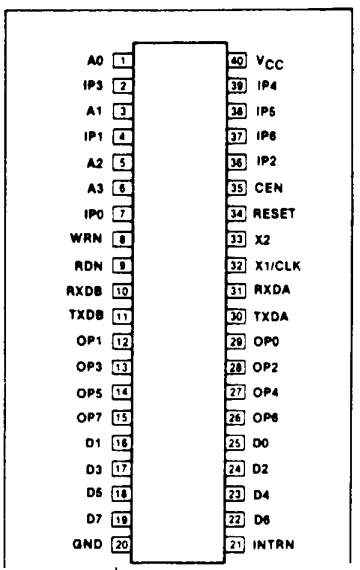
PIN LAYOUT

	Fig. 1	Fig. 2
Model No.	-1 *	-1X
LO	8	8
RF	1	3,4
IF	3,4	1
Ground	2,5,6,7	2,5,6,7
Case Ground	—	2,5,6,7

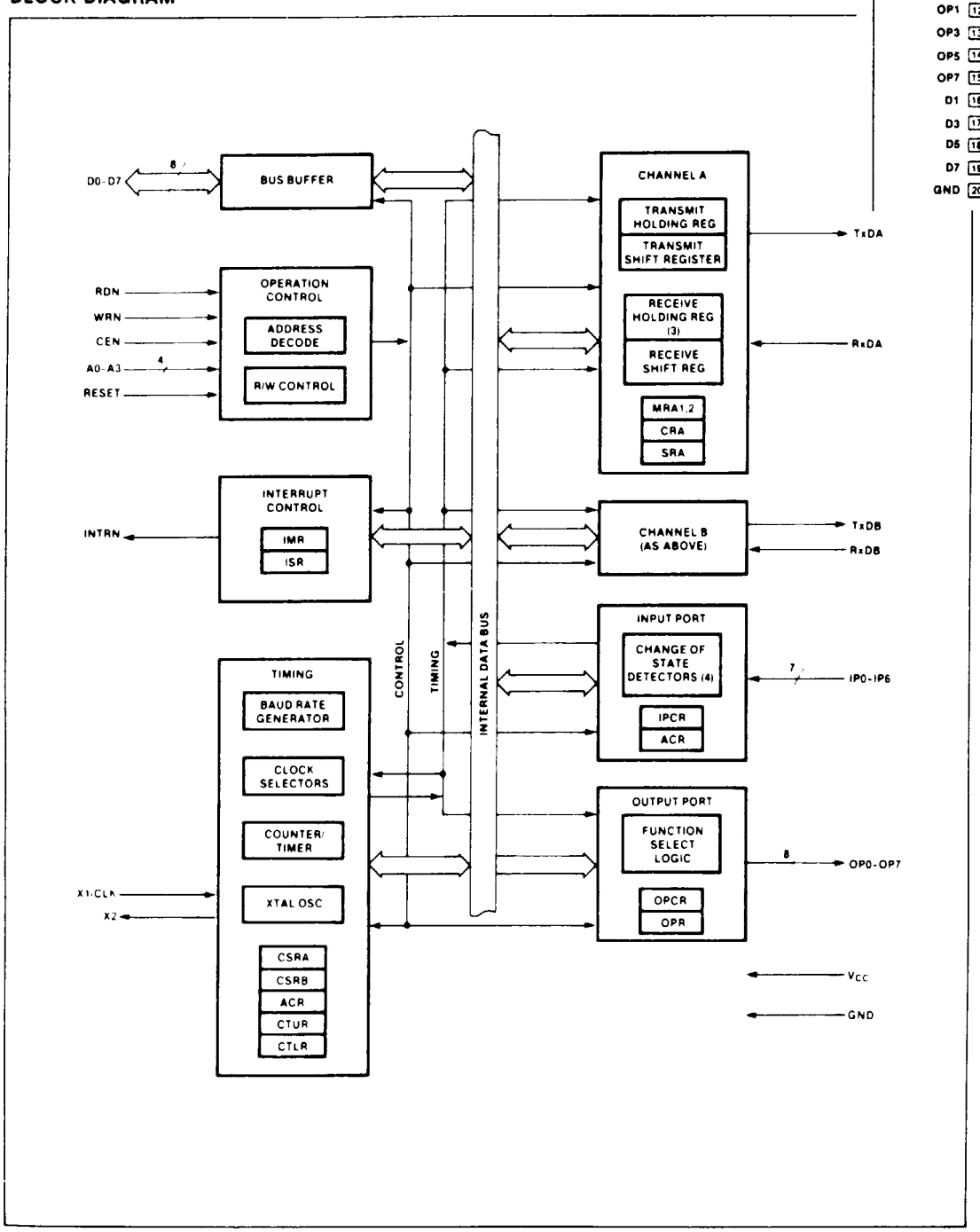
NOTE: PINS 3 AND 4 MUST BE CONNECTED TOGETHER

SCN2681
DUAL UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER (DUART)

PIN CONFIGURATION



BLOCK DIAGRAM



SCN2681 (Cont.)

PIN DESIGNATION

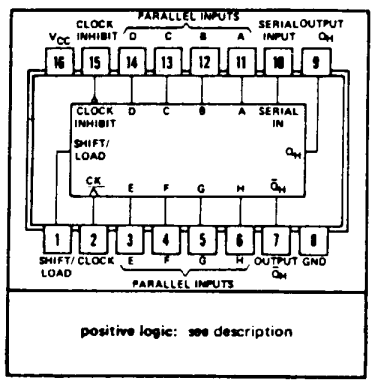
MNEMONIC	APPLICABLE			TYPE	NAME AND FUNCTION
	40	28	24		
D0-D7	X	X	X	I/O	**Data Bus:** Bidirectional 3-state data bus used to transfer commands, data and status between the DUART and the CPU. D0 is the least significant bit.
CEN	X	X	X	I	**Chip Enable:** Active low input signal. When low, data transfers between the CPU and the DUART are enabled on D0-D7 as controlled by the WRN, RDN and A0-A3 inputs. When high, places the D0-D7 lines in the 3-state condition.
WRN	X	X	X	I	**Write Strobe:** When low and CEN is also low, the contents of the data bus is loaded into the addressed register. The transfer occurs on the rising edge of the signal.
RDN	X	X	X	I	**Read Strobe:** When low and CEN is also low, causes the contents of the addressed register to be presented on the data bus. The read cycle begins on the falling edge of RDN.
A0-A3	X	X	X	I	**Address Inputs:** Select the DUART internal registers and ports for read/write operations.
RESET	X	X	X	I	**Reset:** A high level clears internal registers (SRA, SRB, IMR, ISR, OPR, OPCR), puts OP0-OP7 in the high state, stops the counter/timer, and puts channels A and B in the inactive state, with the TxDA and TxDB outputs in the mark (high) state.
INTRN	X	X	X	O	**Interrupt Request:** Active low, open drain, output which signals the CPU that one or more of the eight maskable interrupting conditions are true.
X1/CLK	X	X	X	I	**Crystal 1:** Crystal or external clock input. A crystal or clock of the specified limits must be supplied at all times. When a crystal is used, a capacitor must be connected from this pin to ground (see figure 5).
X2	X	X		O	**Crystal 2:** Connection for other side of the crystal. Should be connected to ground if a crystal is not used. When a crystal is used, a capacitor must be connected from this pin to ground (see figure 5).
RxDA	X	X	X	I	**Channel A Receiver Serial Data Input:** The least significant bit is received first. 'Mark' is high, 'space' is low.
RxDB	X	X	X	I	**Channel B Receiver Serial Data Input:** The least significant bit is received first. 'Mark' is high, 'space' is low.
TxDA	X	X	X	O	**Channel A Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is held in the 'mark' condition when the transmitter is disabled, idle, or when operating in local loopback mode. 'Mark' is high, 'space' is low.
TxDB	X	X	X	O	**Channel B Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is held in the 'mark' condition when the transmitter is disabled, idle, or when operating in local loopback mode. 'Mark' is high, 'space' is low.
OP0	X	X		O	**Output 0:** General purpose output, or channel A request to send (RTSAN, active low). Can be deactivated on receive or transmit.
OP1	X	X		O	**Output 1:** General purpose output, or channel B request to send (RTSBN, active low). Can be deactivated on receive or transmit.
OP2	X			O	**Output 2:** General purpose output, or channel A transmitter 1X or 16X clock output, or channel A receiver 1X clock output.
OP3	X			O	**Output 3:** General purpose output, or open drain, active low counter/timer output, or channel B transmitter 1X clock output, or channel B receiver 1X clock output.
OP4	X			O	**Output 4:** General purpose output, or channel A open drain, active low, RxRDYA/FFULLA output.
OP5	X			O	**Output 5:** General purpose output, or channel B open drain, active low, RxRDYB/FFULLB output.
OP6	X			O	**Output 6:** General purpose output, or channel A open drain, active low, TxRDYA output.
OP7	X			O	**Output 7:** General purpose output, or channel B open drain, active low, TxRDYB output.
IP0	X			I	**Input 0:** General purpose input, or channel A clear to send active low input (CTSAN).
IP1	X			I	**Input 1:** General purpose input, or channel B clear to send active low input (CTSBN).
IP2	X	X		I	**Input 2:** General purpose input, or counter/timer external clock input.
IP3	X			I	**Input 3:** General purpose input, or channel A transmitter external clock input (TxCA). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock.
IP4	X			I	**Input 4:** General purpose input, or channel A receiver external clock input (RxCA). When the external clock is used by the receiver, the received data is sampled on the rising edge of the clock.
IP5	X			I	**Input 5:** General purpose input, or channel B transmitter external clock input (TxCB). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock.
IP6	X			I	**Input 6:** General purpose input or channel B receiver external clock input (RxCB). When the external clock is used by the receiver, the received data is sampled on the rising edge of the clock.
V_{CC}	X	X	X	I	**Power Supply:** +5V supply input
GND	X	X	X	I	**Ground**

SN74165
PARALLEL-LOAD 8-BIT SHIFT REGISTERS

- Complementary Outputs
- Direct Overriding Load (Data) Inputs
- Gated Clock Inputs
- Parallel-to-Serial Data Conversion

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION
'165	26 MHz	210 mW
'LS165	35 MHz	105 mW

(TOP VIEW)



description

The '165 and 'LS165 are 8-bit serial shift registers that shift the data in the direction of Q_A toward Q_H when clocked. Parallel-in access to each stage is made available by eight individual direct data inputs that are enabled by a low level at the shift/load input. These registers also feature gated clock inputs and complementary outputs from the eighth bit. All inputs are diode-clamped to minimize transmission-line effects, thereby simplifying system design.

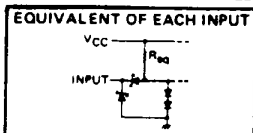
Clocking is accomplished through a 2-input positive-NOR gate, permitting one input to be used as a clock-inhibit function. Holding either of the clock inputs high inhibits clocking and holding either clock input low with the shift/load input high enables the other clock input. The clock-inhibit input should be changed to the high level only while the clock input is high. Parallel loading is inhibited as long as the shift/load input is high. Data at the parallel inputs are loaded directly into the register on a high-to-low transition of the shift/load input independently of the levels of the clock, clock inhibit, or serial inputs.

FUNCTION TABLE

INPUTS					INTERNAL OUTPUTS		OUTPUT
SHIFT/ LOAD	CLOCK INHIBIT	CLOCK	SERIAL	PARALLEL A . . . H	Q_A	Q_B	Q_H
L	X	X	X	a . . . h	a	b	h
H	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	H	X	X	X	Q_{A0}	Q_{B0}	Q_{H0}

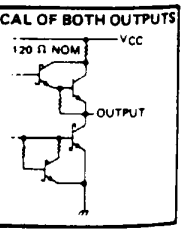
'LS165

EQUIVALENT OF EACH INPUT



Clock, clock inhibit: R_{eq} = 17 kΩ NOM
Parallel inputs,
serial input: R_{eq} = 24 kΩ NOM
Shift/load: R_{eq} = 5.7 kΩ NOM

TYPICAL OF BOTH OUTPUTS

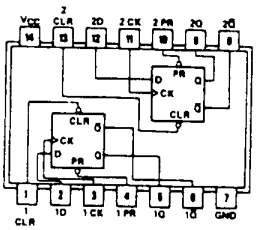


SN74LS74N

DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

FUNCTION TABLE

INPUTS				OUTPUTS	
PRESET	CLEAR	CLOCK	D	Q	$\bar{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\bar{Q}_0$



SN74L90
DECADE, DIVIDE-BY-TWELVE, AND BINARY COUNTER

description

Each of these monolithic counters contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-five for the '90A, 'L90, and 'LS90, divide-by-six for the '92A and 'LS92, and divide-by-eight for the '93A, 'L93, and 'LS93.

All of these counters have a gated zero reset and the '90A, 'L90, and 'LS90 also have gated set-to-nine inputs for use in BCD nine's complement applications.

To use their maximum count length (decade, divide-by-twelve, or four-bit binary) of these counters, the B input is connected to the Q_A output. The input count pulses are applied to input A and the outputs are as described in the appropriate function table. A symmetrical divide-by-ten count can be obtained from the '90A, 'L90, or 'LS90 counters by connecting the Q_D output to the A input and applying the input count to the B input which gives a divide-by-ten square wave at output Q_A.

'90A, 'L90, 'LS90
BCD COUNT SEQUENCE
(See Note A)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

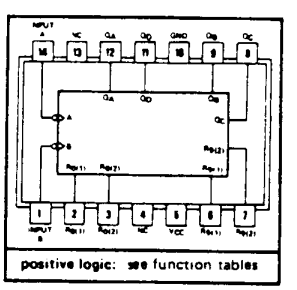
'90A, 'L90, 'LS90
BI-QUINARY (5-2)
(See Note B)

COUNT	OUTPUT			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

'90A, 'L90, 'LS90
RESET/COUNT FUNCTION TABLE

RESET INPUTS				OUTPUT			
$R_{0(1)}$	$R_{0(2)}$	$R_{9(1)}$	$R_{9(2)}$	Q_D	Q_C	Q_B	Q_A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	COUNT			
L	X	L	X	COUNT			
L	X	X	L	COUNT			
X	L	L	X	COUNT			

NOTES A. Output Q_A is connected to input B for BCD count.
B. Output Q_D is connected to input A for bi-quinary count.
C. Output Q_A is connected to input B.
D. H = high level, L = low level, X = irrelevant



positive logic: see function tables

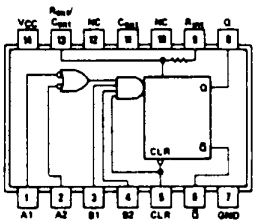
SN74LS122

RETRIGGERABLE MONOSTABLE MULTIVIBRATORS WITH CLEAR

FUNCTION TABLE

INPUTS					OUTPUTS	
CLEAR	A1	A2	B1	B2	Q	$\overline{Q}$
L	X	X	X	X	L	H
X	H	H	X	X	L	H
X	X	X	L	X	L	H
X	X	X	X	L	L	H
H	L	X	↑	H	⎍	⎎
H	L	X	H	↑	⎍	⎎
H	X	L	↑	H	⎍	⎎
H	X	L	H	↑	⎍	⎎
H	H	↓	H	H	⎍	⎎
H	↓	↓	H	H	⎍	⎎
H	↓	H	H	H	⎍	⎎
↑	L	X	H	H	⎍	⎎
↑	X	L	H	H	⎍	⎎

NOTES: 1. An external timing capacitor may be connected between C_{ext} and R_{ext}/C_{ext} (positive).
2. For accurate repeatable pulse widths, connect an external resistor between R_{ext}/C_{ext} and V_{CC} with R_{int} open-circuited.



SN54122 (J, W) **SN74122 (J, N)**
SN54L122 (J, T) **SN74L122 (J, N)**
SN54LS122 (J, W) **SN74LS122 (J, N)**
'122 . . . R_{int} = 10 kΩ NOM
'L122 . . . R_{int} = 20 kΩ NOM
'LS122 . . . R_{int} = 10 kΩ NOM

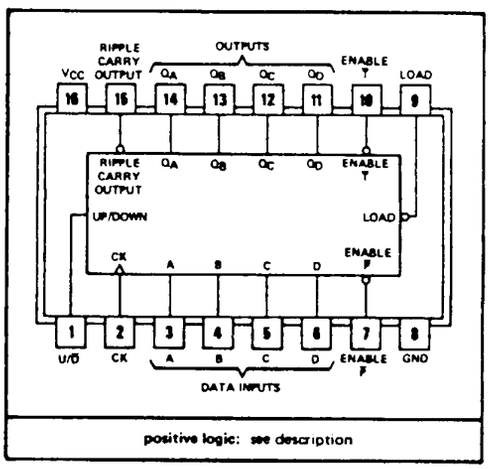
SN74LS168A
SYNCHRONOUS 4-BIT UP/DOWN COUNTERS

Programmable Look-Ahead Up/Down
Binary/Decade Counters

- Fully Synchronous Operation for Counting and Programming
- Internal Look-Ahead for Fast Counting
- Carry Output for n-Bit Cascading
- Fully Independent Clock Circuit

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY		TYPICAL POWER DISSIPATION
	COUNTING UP	COUNTING DOWN	
'LS168A, 'LS169A	35 MHz	35 MHz	100 mW
'S168, 'S169	70 MHz	55 MHz	500 mW

(TOP VIEW)



description

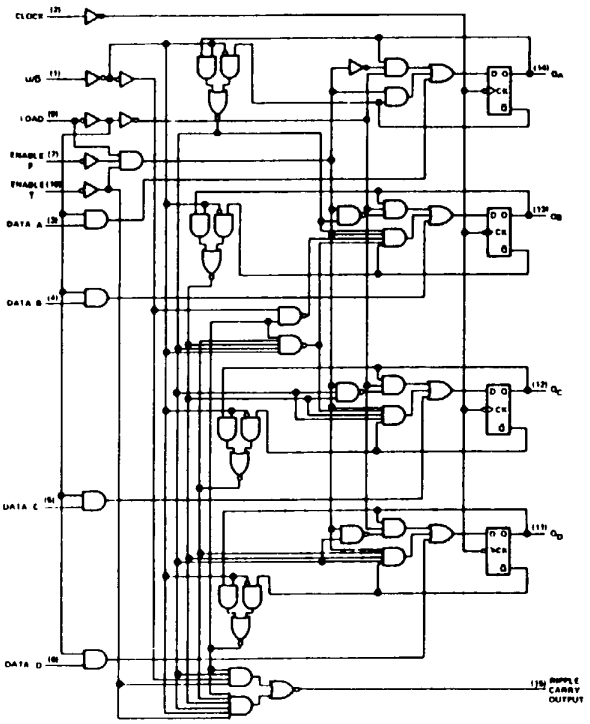
These synchronous presettable counters feature an internal carry look-ahead for cascading in high-speed counting applications. The 'LS168A and 'S168 are decade counters and the 'LS169A and 'S169 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation helps eliminate the output counting spikes that are normally associated with asynchronous (ripple-clock) counters. A buffered clock input triggers the four master-slave flip-flops on the rising (positive-going) edge of the clock waveform.

These counters are fully programmable; that is, the outputs may each be preset to either level. The load input circuitry allows loading with the carry-enable output of cascaded counters. As loading is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the data inputs after the next clock pulse.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a carry output. Both count enable inputs ($\overline{P}$ and $\overline{T}$) must be low to count. The direction of the count is determined by the level of the up/down input. When the input is high, the counter counts up; when low, it counts down. Input $\overline{T}$ is fed forward to enable the carry output. The carry output thus enabled will produce a low-level output pulse with a duration approximately equal to the high portion of the Q_A output when counting up and approximately equal to the low portion of the Q_A output when counting down. This low-level overflow carry pulse can be used to enable successive cascaded stages. Transitions at the enable $\overline{P}$ or $\overline{T}$ inputs are allowed regardless of the level of the clock input. All inputs are diode-clamped to minimize transmission-line effects.

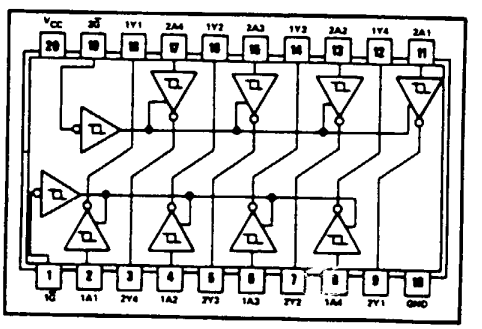
These counters feature a fully independent clock circuit. Changes at control inputs (enable $\overline{P}$, enable $\overline{T}$, load, up/down) that will modify the operating mode have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

SN74LS168A (Cont.)



SN74LS244
OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

These octal buffers and line drivers are designed specifically to improve both the performance and density of three-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The designer has a choice of selected combinations of inverting and noninverting outputs, symmetrical $\overline{G}$ (active-low output control) inputs, and complementary G and $\overline{G}$ inputs. These devices feature high fan-out, improved fan-in, and 400-mV noise-margin. The SN74LS' and SN74S' can be used to drive terminated lines down to 133 ohms.

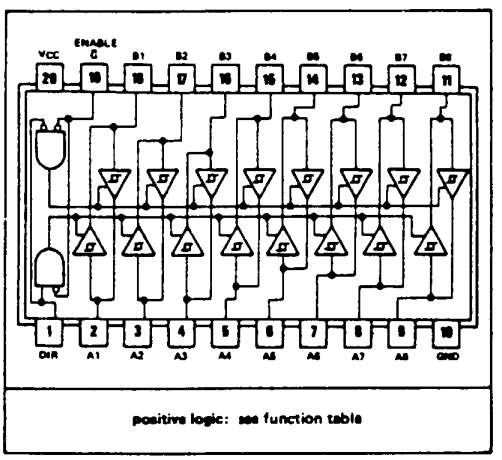


SN74LS245
OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation minimizes external timing requirements.

The device allows data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction control (DIR) input. The enable input ($\overline{G}$) can be used to disable the device so that the buses are effectively isolated.



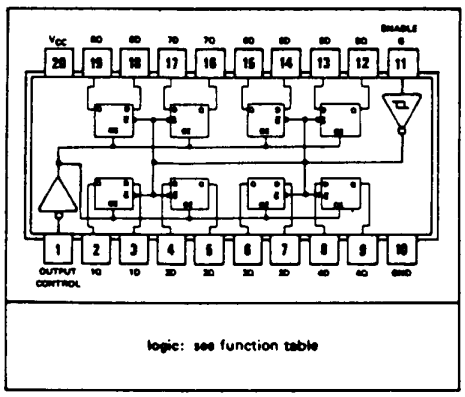
positive logic: see function table

FUNCTION TABLE

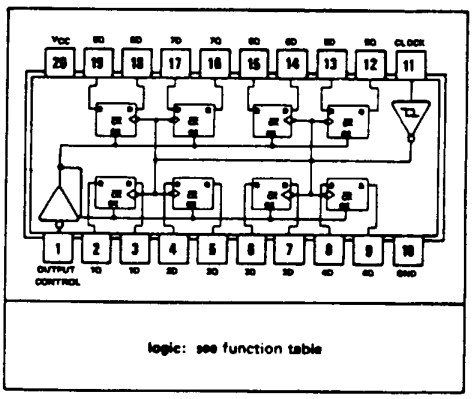
ENABLE $\overline{G}$	DIRECTION CONTROL DIR	OPERATION
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

H = high level, L = low level, X = irrelevant

SN74LS373, SN74LS374
OCTAL D-TYPE TRANSPARENT LATCHES AND EDGE-TRIGGERED FLIP-FLOPS



logic: see function table



logic: see function table

'LS373, 'S373
FUNCTION TABLE

OUTPUT CONTROL	ENABLE G	D	OUTPUT
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

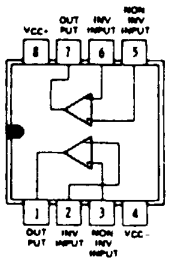
'LS374, 'S374
FUNCTION TABLE

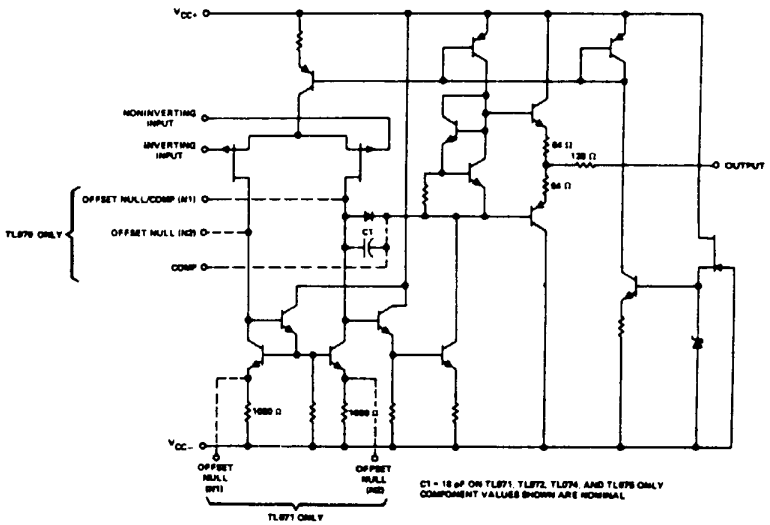
OUTPUT CONTROL	CLOCK	D	OUTPUT
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

These 8-bit registers feature totem-pole three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the 'LS373 and 'S373 are transparent D-type latches meaning that while the enable (G) is high the Q outputs will follow the data (D) inputs. When the enable is taken low the output will be latched at the level of the data that was setup.

TL072
LOW-NOISE JFET-INPUT OPERATIONAL AMPLIFIERS



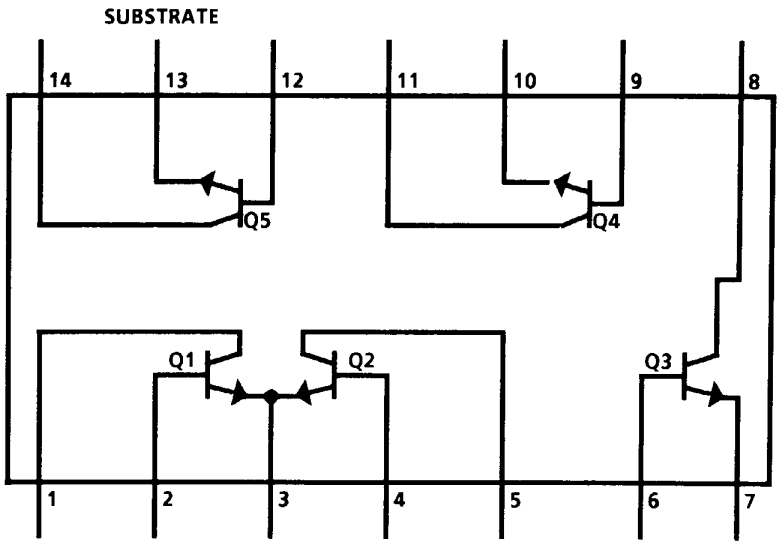


description

The JFET-input operational amplifiers of the TL071 series are designed as low-noise versions of the TL081 series amplifiers with low input bias and offset currents and fast slew rate. The low harmonic distortion and low noise make the TL071 series ideally suited as amplifiers for high-fidelity and audio preamplifier applications. Each amplifier features JFET-inputs (for high input impedance) coupled with bipolar output stages all integrated on a single monolithic chip.

3045
TRANSISTOR ARRAY

Dual-In-Line Package



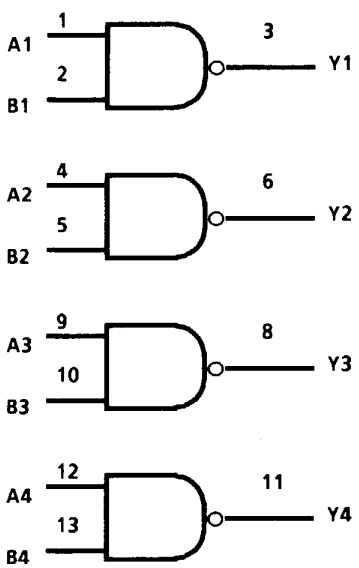
TOP VIEW

absolute maximum ratings (T_A = 25°C)

	LM3045		LM3046/LM3086		Units
	Each Transistor	Total Package	Each Transistor	Total Package	
Power Dissipation:					
T_A = 25°C	300	750	300	750	mW
T_A = 25°C to 55°C			300	750	mW
T_A > 55°C			Derate at 6.67		mW/°C
T_A = 25°C to 75°C	300	750			mW
T_A > 75°C	Derate at 8				mW/°C
Collector to Emitter Voltage, V_{CEO}	15		15		V
Collector to Base Voltage, V_{CBO}	20		20		V
Collector to Substrate Voltage, V_{CIO} (Note 1)	20		20		V
Emitter to Base Voltage, V_{EBO}	5		5		V
Collector Current, I_C	50		50		mA
Operating Temperature Range	-55°C to + 125°C		-40°C to + 85°C		
Storage Temperature Range	-65°C to + 150°C		-65°C to + 85°C		
Lead Temperature (Soldering, 10 sec)	300		300		°C

74XX00
QUAD 2-INPUT NAND

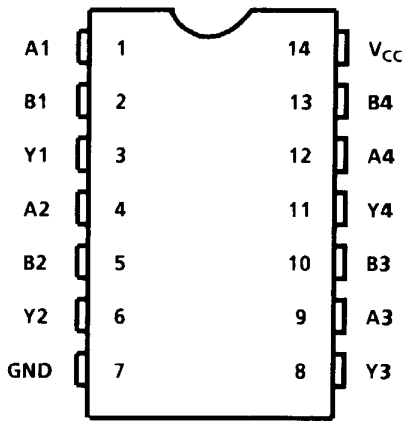
LOGIC DIAGRAM



$Y = \overline{AB}$

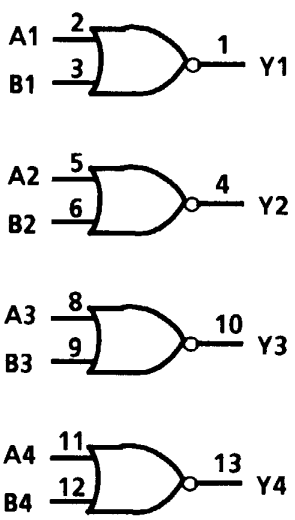
V_{CC} = Pin 14
GND = Pin 7

PIN ASSIGNMENT



74XX02
QUAD 2-INPUT NORGATE

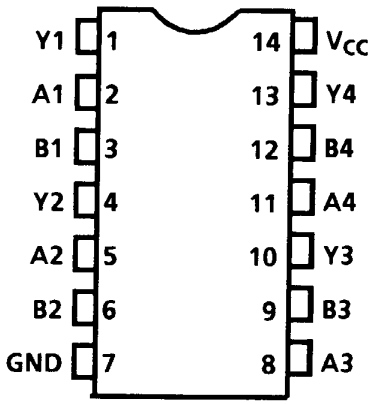
LOGIC DIAGRAM



$Y = \overline{A + B}$

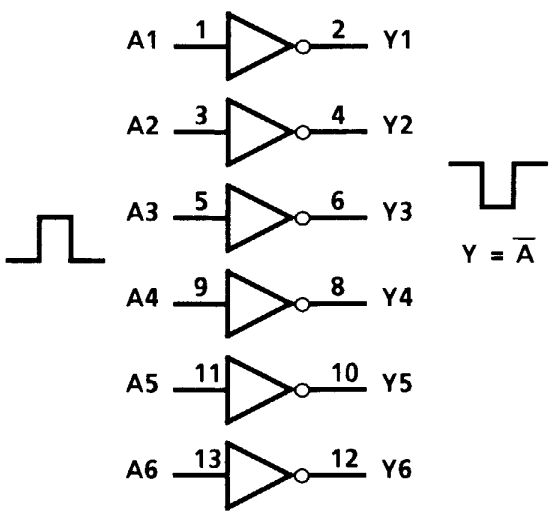
V_{CC} = Pin 14
GND = Pin 7

PIN ASSIGNMENT



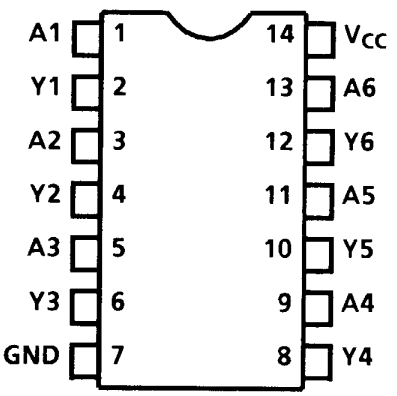
74XX04
HEX INVERTER

LOGIC DIAGRAM



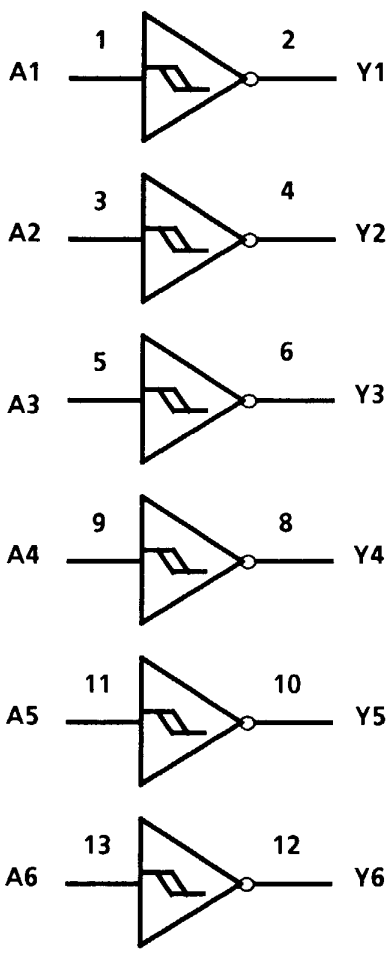
V_{CC} = Pin 14
GND = Pin 7

PIN ASSIGNMENT



74XX14 - HEX SCHMITT-TRIGGER INVERTER

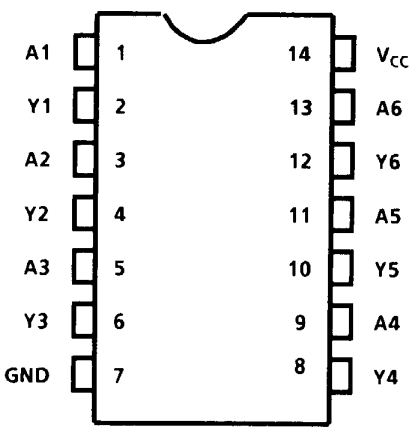
FUNCTION DIAGRAM



$Y = \bar{A}$

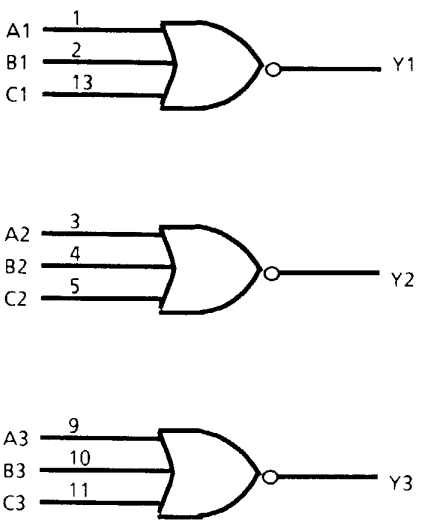
V_{CC} = Pin 14
GND = Pin 7

PIN ASSIGNMENT



74XX27
TRIPLE 3-INPUT NOR

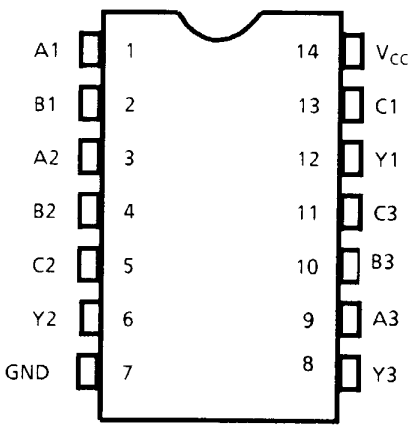
LOGIC DIAGRAM



$Y = \overline{A + B + C}$

V_{CC} = Pin 14
GND = Pin 7

PIN ASSIGNMENT



74XX73 (74LS73 or 74HC73)
DUAL JK NEGATIVE EDGE-TRIGGERED FLIP-FLOP

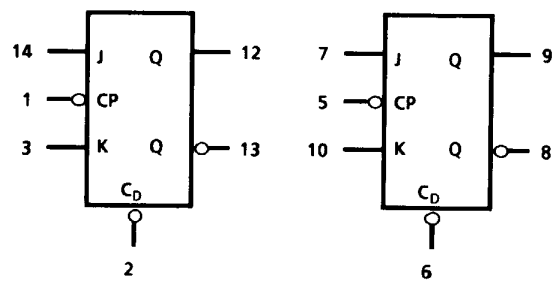
DESCRIPTION - The 74XX73 offers individual J, K, clear, and clock inputs. These dual flip-flops are designed so that when the clock goes HIGH, the inputs are enabled and data will be accepted. The logic level of the J and K inputs may be allowed to change when the clock pulse is HIGH and the bistable will perform according to the truth table as long as minimum set-up times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

MODE SELECT - TRUTH TABLE

OPERATING MODE	INPUTS			OUTPUTS	
	$\overline{C_D}$	J	K	Q	$\overline{Q}$
Reset (Clear)	L	X	X	L	H
Toggle	H	h	h	q	q
Load "0" (Reset)	H	l	h	L	H
Load "1" (Set)	H	h	l	H	L
Hold	H	l	l	q	q

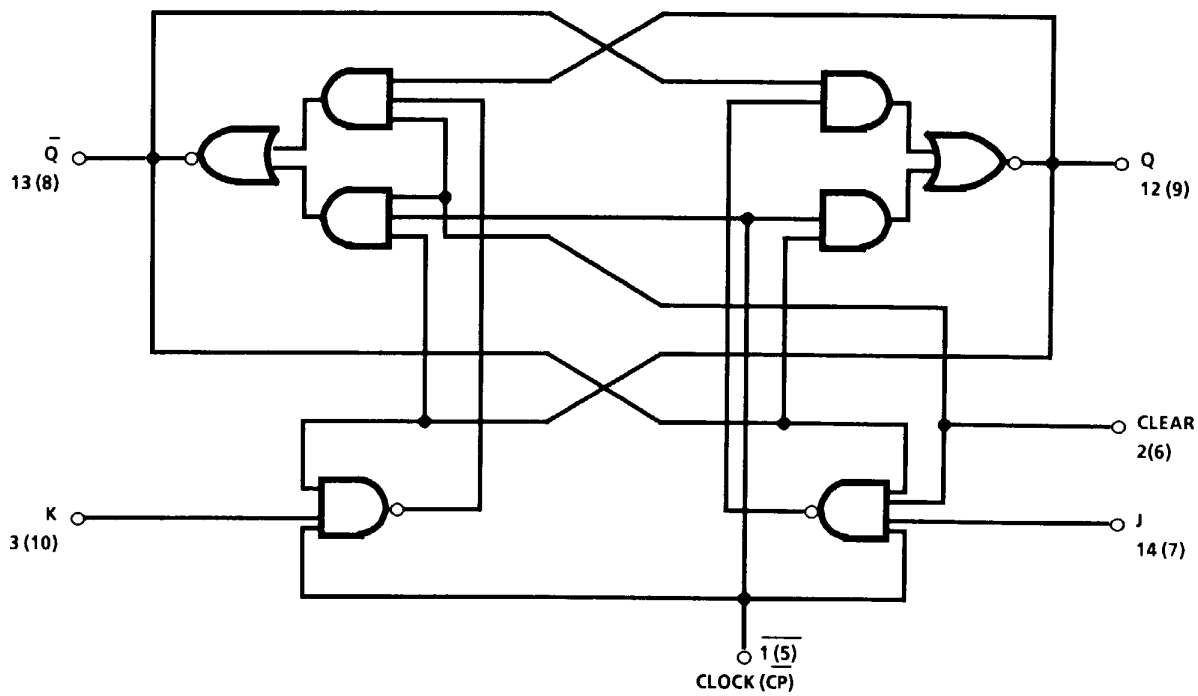
H, h = HIGH Voltage Level
L, l = LOW Voltage Level
X = Don't Care
l, h (q) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the HIGH to LOW clock transition.

LOGIC SYMBOL



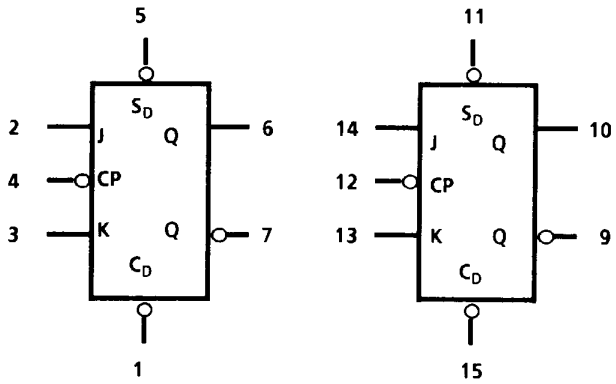
V_{CC} = Pin 4
GND = Pin 11

LOGIC DIAGRAM (Each Flip-Flop)



74XX109 (74LS109 or 74HC109)
DUAL JK POSITIVE
EDGE-TRIGGERED FLIP-FLOP

LOGIC SYMBOL



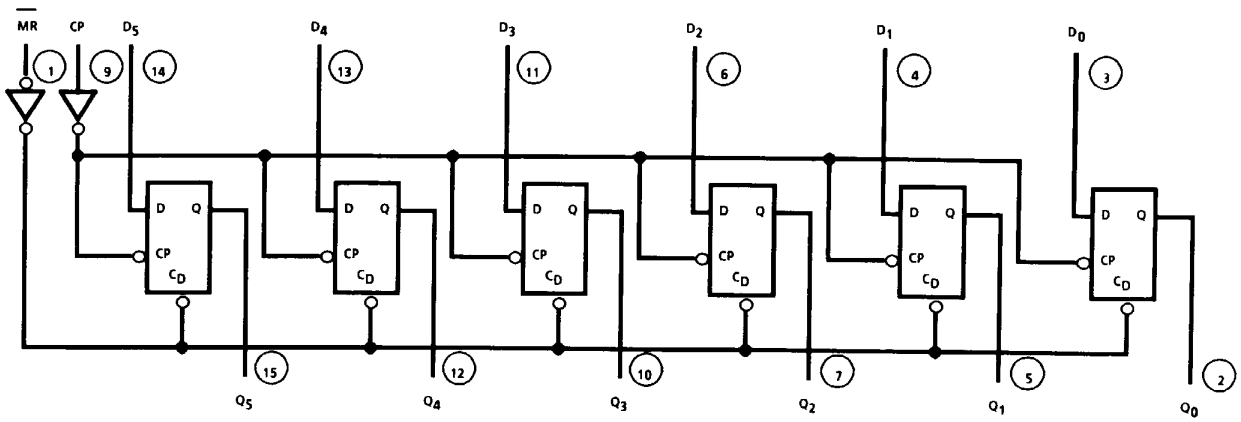
V_{CC} = Pin 16
GND = Pin 8

MODE SELECT - TRUTH TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	$\overline{S}_D$	$\overline{C}_D$	J	$\overline{K}$	Q	$\overline{Q}$
Set	L	H	X	X	H	L
Reset (Clear)	H	L	X	X	L	H
* Undetermined	L	L	X	X	H	H
Load "1" (Set)	H	H	h	h	H	$\overline{L}$
Hold	H	H	l	h	q	$\overline{q}$
Toggle	H	H	h	l	$\overline{q}$	q
Load "0" (Reset)	H	H	l	l	L	H

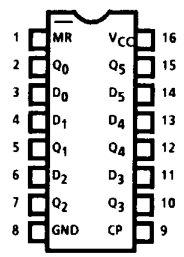
74XX174 (74LS174, 74HC174)
HEX D FLIP-FLOP

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

CONNECTION DIAGRAM
DIP (TOP VIEW)



FUNCTIONAL DESCRIPTION - The device consists of six edge-triggered D flip-flops with individual D inputs and Q outputs. The Clock (CP) and Master Reset ($\overline{MR}$) are common to all flip-flops.

Each D input's state is transferred to the corresponding flip-flop's output following the LOW to HIGH Clock (CP) transition.

A LOW input to the Master Reset ($\overline{MR}$) will force all outputs LOW independent of Clock or Data inputs.

TRUTH TABLE

Inputs (t = n, $\overline{MR}$ = H)	Outputs (t = n + 1) Note 1
D	Q
H	H
L	L

Note 1: t = n + 1 indicates conditions after next clock.

8035
SINGLE COMPONENT 8-BIT MICROCOMPUTER

***8048 Mask Programmable ROM**
***8748 User Programmable/Erasable EPROM**
***8035 External ROM or EPROM**

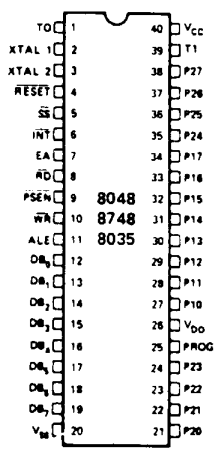
- 8-Bit CPU, ROM, RAM, I/O in Single Package
- Interchangeable ROM and EPROM Versions
- Single 5V Supply
- 2.5 µsec and 5.0 µsec Cycle Versions All Instructions 1 or 2 Cycles.
- Over 90 Instructions: 70% Single Byte
- 1K x 8 ROM/EPROM 64 x 8 RAM 27 I/O Lines
- Interval Timer/Event Counter
- Easily Expandable Memory and I/O
- Compatible with 8000 Series Peripherals
- Single Level Interrupt

The Intel® 8048/8748/8035 is a totally self-sufficient 8-bit parallel computer fabricated on a single silicon chip using Intel's N-channel silicon gate MOS process.

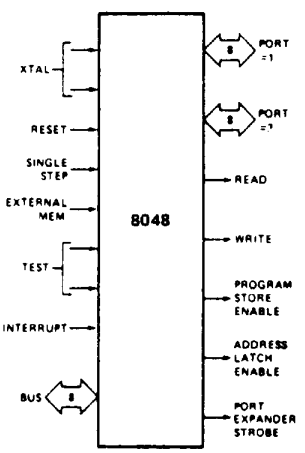
The 8048 contains a 1K x 8 program memory, a 64 x 8 RAM data memory, 27 I/O lines, and an 8-bit timer/counter in addition to on board oscillator and clock circuits. For systems that require extra capability, the 8048 can be expanded using standard memories and 8000 series peripherals. The 8035 is the equivalent of an 8048 without program memory

This microprocessor is designed to be an efficient controller as well as an arithmetic processor. The 8048 has extensive bit handling capability as well as facilities for both binary and BCD arithmetic. Efficient use of program memory results from an instruction set consisting mostly of single byte instructions and no instructions over two bytes in length.

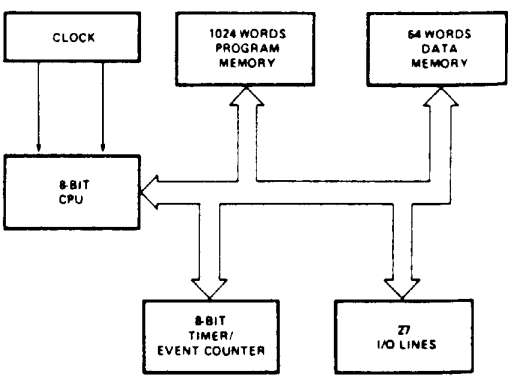
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



8035 (Cont.)

PIN DESCRIPTION

Designation	Pin #	Function
V_{SS}	20	Circuit GND potential
V_{DD}	26	Programming power supply; +25V during program, +5V during operation for both ROM and PROM. Low power standby pin in 8048 ROM version.
V_{CC}	40	Main power supply; +5V during operation and programming.
PROG	25	Program pulse (+25V) input pin during 8748 programming.
		Output strobe for 8243 I/O expander.
P10-P17 Port 1	27-34	8-bit quasi-bidirectional port.
P20-P27 Port 2	21-24 35-38	8-bit quasi-bidirectional port. P20-P23 contain the four high order program counter bits during an external program memory fetch and serve as a 4-bit I/O expander bus for 8243
DB_0-DB_7 BUS	12-19	True bidirectional port which can be written or read synchronously using the $\overline{RD}$, $\overline{WR}$ strobes. The port can also be statically latched.
		Contains the 8 low order program counter bits during an external program memory fetch, and receives the addressed instruction under the control of PSEN. Also contains the address and data during an external RAM data store instruction, under control of ALE, $\overline{RD}$, and $\overline{WR}$.
T0	1	Input pin testable using the conditional transfer instructions JT0 and JNT0. T0 can be designated as a clock output using ENT0 CLK instruction. T0 is also used during programming.
T1	39	Input pin testable using the JT1, and JNT1 instructions. Can be designated the timer/counter input using the STRT CNT instruction.
$\overline{INT}$	6	Interrupt input. Initiates an interrupt if interrupt is enabled. Interrupt is disabled after a reset. Also testable with conditional jump instruction. (Active low)

Designation	Pin #	Function
$\overline{RD}$	8	Output strobe activated during a BUS read. Can be used to enable data onto the BUS from an external device.
		Used as a Read Strobe to External Data Memory. (Active low)
$\overline{RESET}$	4	Input which is used to initialize the processor. Also used during PROM programming verification, and power down. (Active low)
$\overline{WR}$	10	Output strobe during a BUS write. (Active low)(Non TTL V_{IH})
		Used as write strobe to External Data Memory.
ALE	11	Address Latch Enable. This signal occurs once during each cycle and is useful as a clock output.
		The negative edge of ALE strobes address into external data and program memory.
$\overline{PSEN}$	9	Program Store Enable. This output occurs only during a fetch to external program memory. (Active low)
$\overline{SS}$	5	Single step input can be used in conjunction with ALE to "single step" the processor through each instruction. (Active low)
EA	7	External Access input which forces all program memory fetches to reference external memory. Useful for emulation and debug, and essential for testing and program verification. (Active high)
XTAL1	2	One side of crystal input for internal oscillator. Also input for external source. (Not TTL Compatible)
XTAL2	3	Other side of crystal input.

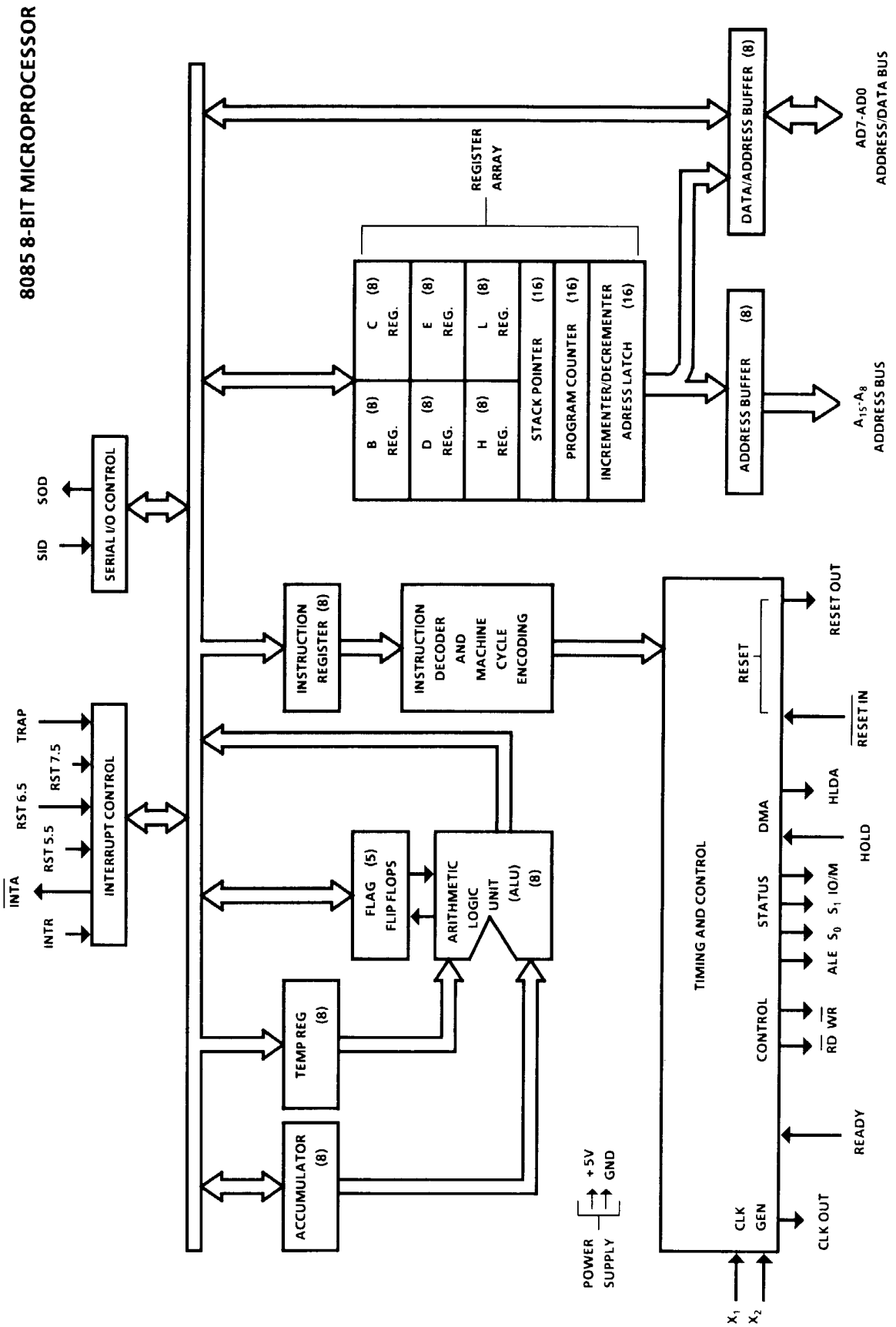


Figure 1. 8085AH CPU Functional Block Diagram

8085
8-BIT MICROPROCESSOR
(Cont.)

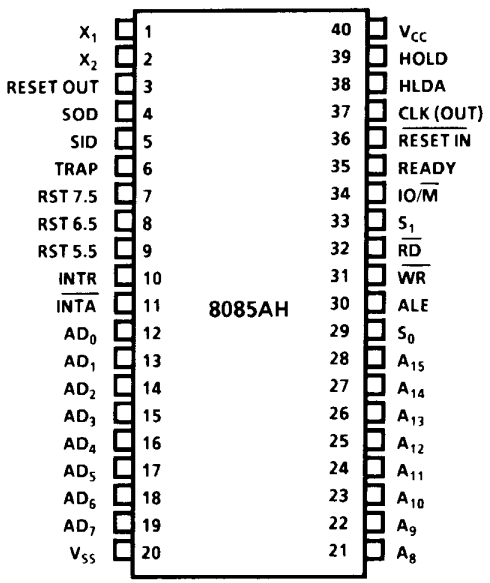


Figure 2. 8085AH Pin Configuration

8085 (Cont.)

Table 1. Pin Description

Symbol	Type	Name and Function
A_8-A_{15}	O	**Address Bus:** The most significant 8 bits of the memory address or the 8 bits of the I/O address, 3-stated during Hold and Halt modes and during RESET.
AD_{0-7}	O/I	**Multiplexed Address/Data Bus:** Lower 8 bits of the memory adress (or I/O address) appear on the bus during the first Icock cycle (T state) of a machine cycle. It then becomes the data bus during the second and third clock cycles.
ALE	O	**Address Latch Enable:** It occurs during the first clock state of a machine cycle and enables the address to get latched into the on-chip latch of peripherals. The falling edge of ALE is set to guarantee setup and hold times for the address information. The falling edge of ALE can also be used to strobe the status information. ALE is never 3-stated.
S_0,S_1, and IO/$\overline{M}$	O	**Machine Cycle Status:** IO/$\overline{M}$ S_1 S_0 Status 0 0 1 Memory write 0 1 0 Memory read 1 0 1 I/O write 1 1 0 I/O read 0 1 1 Opcode fetch 1 1 1 Opcode fetch 1 1 1 Interrupt Acknowledge * 0 0 Halt * X X Hold * X X Reset * = 3-state(high impedance) X = unspecified S_1 can be used as an advanced R/$\overline{W}$ satus. IO/$\overline{M}$, S_0 and S_1 become valid at the beginning of a machine cycle and remain stable throughout the cycle. The falling edge of ALE may be used to latch the state of these lines.

Symbol	Type	Name and Function
$\overline{RD}$	O	**Read Control:** A low level on $\overline{RD}$ indicates the selected memory or I/O device is to be read and that the Data Bus is available for the data transfer, 3-stated during Hold and Halt modes and during RESET.
$\overline{WR}$	O	**Write Control:** A low level on $\overline{WR}$ indicates the data on the Data Bus is to be written into the selected memory or I/O location. Data is set up at the trailing edge of $\overline{WR}$. 3-stated during Hold and Halt modes and during RESET.
READY	I	**Ready:** If READY is high during a read or write cycle, it indicates that the memory or peripheral is ready to send or receive data. If READY is low, the cpu will wait an integral number of clock cycles for READY to go high before completing the read or write cycle. READY must conform to specified setup and hold times.
HOLD	I	**Hold:** Indicates that another master is requesting the use of the address and data buses. The cpu, upon receiving the hold request, will relinquish the use of the bus as soon as the completion of the current bus transfer. Internal processing can continue. The processor can regain the bus only after the HOLD is removed. When the HOLD is acknowledged, the Address, Data $\overline{RD}$, $\overline{WR}$, and IO/$\overline{M}$ lines are 3-stated.
HLDA	O	**Hold Acknowledge:** Indicates that the cpu has received the HOLD request and that it will relinquish the bus in the next clock cycle. HLDA goes low after the Hold request is removed. The cpu takes the bus one half clock cycle after HLDA goes low.

8155 - RAM; Triple I/O; Timer

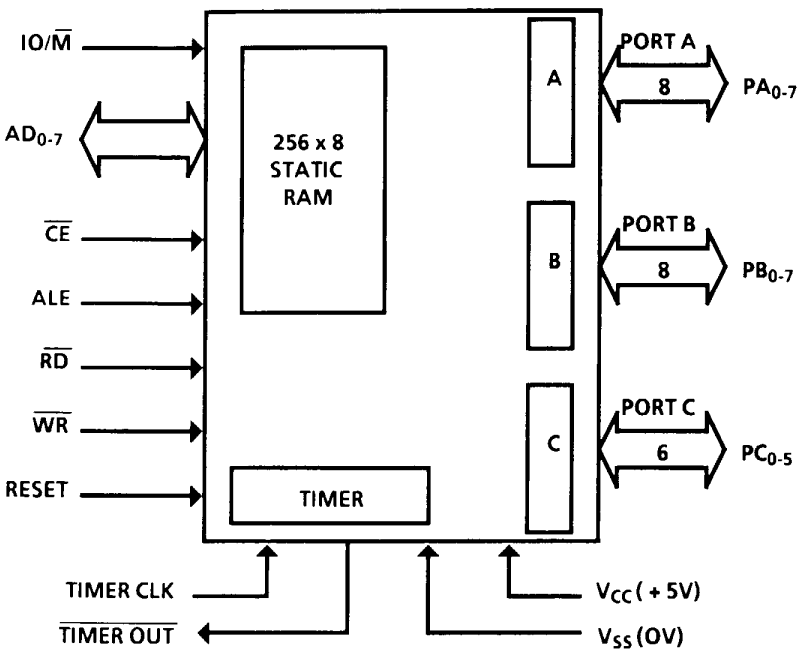


Figure 1. Block Diagram

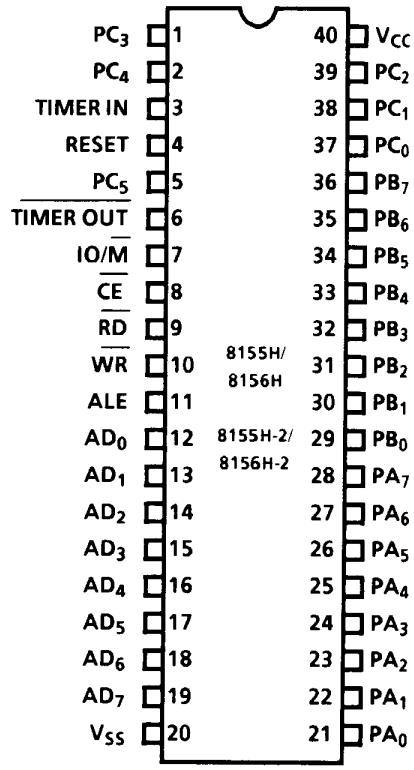


Figure 2. Pin Configuration

8155
Table 1. Pin Description

Symbol	Type	Name and Function
RESET	I	**Reset:** Pulse provided by the 8085AH to initialize the system (connect to 8085AH RESET OUT). Input high on this line resets the chip and initilaizes the three I/O ports to input mode. The width of RESET pulse should typically be two 8085AH clock cycle times.
AD_{0-7}	I/O	**Address/Data:** 3-state Address/Data lines that interface with the CPU lower 8-bit Address/Data Bus. The 8-bit address is latched into the address latch inside the 8155H/56H on the falling edge of ALE. The address can be either for the memory section or the I/O section depending on the IO/$\overline{M}$ input. The 8-bit data is eiether written into the chip or read from the chip, depending on the $\overline{WR}$ or $\overline{RD}$ input signal.
$\overline{CE}$	I	**Chip Enable:** Enable chip interface with CPU Bus.
$\overline{RD}$	I	**Read Control:** Input low on this line with the Chip Enable active enables and AD_{0-7} buffers. If IO/$\overline{M}$ pin is low, the RAM content will be read out to the AD bus. Otherwise the content of the selected I/O port or command/status registers will be read to the AD bus.
$\overline{WR}$	I	**Write Control:** Input low on this line with the Chip Enable active causes the data on the Address/Data bus to be written to the RAM or I/O ports and command/status register, depending on IO/$\overline{M}$.
ALE	I	**Address Latch Enable:** This control signal latches both the address on the AD_{0-7} lines and the state of the Chip Enable and IO/$\overline{M}$ into the chip at the falling edge of ALE.
IO/$\overline{M}$	I	**I/O Memory:** Selects memory if low and I/O and command/status registers if high.
PA_{0-7}(8)	I/O	**Port A:** These 8 pins are general purpose I/O pins. The in/out direction is selected by programming the command register.
PB_{0-7}(8)	I/O	**Port B:** These 8 pins are general purpose I/O pins. The in/out direction is selected by programming the command register.
PC_{0-5}(6)	I/O	**Port C:** These 6 pins can function as either input port, output port, or as control signals for PA and PB. Programming is done through the command register. When PC_{0-5} are used as control signals, they will provide the following: PC_0 - A INTR (Port A Interrupt) PC_1 - $\overline{ABF}$ (Port A Buffer Full) PC_2 - $\overline{A\ STB}$ (Port A Strobe) PC_3 - B INTR (Port B Interrupt) PC_4 - $\overline{B\ BF}$ (Port B Buffer Full) PC_5 - $\overline{B\ STB}$ (Port B Strobe)
TIMER IN	I	**Timer Input:** Input to the counter-timer.
$\overline{TIMER\ OUT}$	O	**Timer Output:** This output can be either a square wave or a pulse, depending on the timer mode.
V_{CC}		**Voltage:** + 5 volt supply.
V_{SS}		**Ground:** Ground reference.

Table 1. Pin Description (Cont.)

Symbol	Type	Name and Function
INTR	I	**Interrupt Request:** Is used as a general purpose interrupt. It is sampled only during the next to the last lock cycle of an instruction and during Hold and Halt states. If it is active, the Program Counter (PC) will be inhibited from incrementing and an $\overline{INTA}$ will be issued. During this cycle a RESTART or CALL instruction can be inserted to jump to the interrupt service routine. The INTR is enabled and disabled by software. It is disabled by Reset and immediately after an interrupt is accepted.
$\overline{INTA}$	O	**Interrupt Acknowledge:** Is used instead of (and has the same timing as) $\overline{RD}$ during the Instruction cycle after an INTR is accepted. It can be used to activate an 8259A Interrupt chip or some other interrupt port.
RST 5.5 RST 6.5 RST 7.5	I	**Restart Interrupts:** These three inputs have the same timing as INTR except they cause an internal RESTART to be automatically inserted. The priority of these interrupts is ordered as shown in Table 2. These interrupts have a higher priority than INTR. In addition, they may be individually masked out using the SIM instruction.
TRAP	I	**Trap:** Trap interrupt is a non-maskable RESTART interrupt. It is recognized at the same time as INTR or RST 5.5-7.5. It is unaffected by any mask or Interrupt enable. It has the highest priority of any interrupt. (See Table 2.)
$\overline{RESET\ IN}$	I	**Reset In:** Sets the Program counter to zero and resets the Interrupt Enable and HLDA flip-flops. The data and address buses and the control lines are 3-stated during RESET and

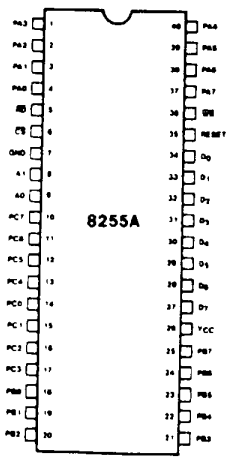
Symbol	Type	Name and Function
(Cont.)		because of the asynchronous nature of RESET, the processor's internal registers and flags may be altered by RESET with unpredictable results. $\overline{RESET\ IN}$ is a Schmitt-triggered input, allowing connection to an R-C network for power-on RESET delay (see Figure 3). Upon power-up, $\overline{RESET\ IN}$ must remain low for at least 10 ms after minimum V_{CC} has been reached. For proper reset operation after the power-up duration. $\overline{RESET\ IN}$ should be kept low a minimum of three clock periods. The CPU is held in the reset condition as long as $\overline{RESET\ IN}$ is applied.
RESET OUT	O	**Reset Out:** Reset Out indicates cpu is being reset. Can be used as a system reset. The signal is synchronized to the processor clock and lasts an integral number of clock periods.
X_1,X_2	I	**X_1 and X_2:** Are connected to a crystal, LC, or RC network to drive the internal clock generator. X_1 can also be an external clock input from a logic gate. The input frequency is divided by 2 to give the processor's internal operating frequency.
CLK	O	**Clock:** Clock output for use as a system clock. The period of CLK is twice the X_1, X_2 input period.
SID	I	**Serial Input Dat Line:** The data on this line is loaded into accumulator bit 7 whenever a RIM instruction is executed.
SOD	O	**Serial Output Data Line:** The output SOD is set or reset as specified by the SIM instruction.
V_{CC}		**Power:** + 5 volt supply.
V_{SS}		**Ground:** Reference.

8255A/8255A-5
PROGRAMMABLE PERIPHERAL INTERFACE

- MCS-85™ Compatible 8255A-5
- 24 Programmable I/O Pins
- Completely TTL Compatible
- Fully Compatible with Intel® Microprocessor Families
- Improved Timing Characteristics
- Direct Bit Set/Reset Capability Easing Control Application Interface
- 40-Pin Dual In-Line Package
- Reduces System Package Count
- Improved DC Driving Capability

The Intel® 8255A is a general purpose programmable I/O device designed for use with Intel® microprocessors. It has 24 I/O pins which may be individually programmed in 2 groups of 12 and used in 3 major modes of operation. In the first mode (MODE 0), each group of 12 I/O pins may be programmed in sets of 4 to be input or output. In MODE 1, the second mode, each group may be programmed to have 8 lines of input or output. Of the remaining 4 pins, 3 are used for handshaking and interrupt control signals. The third mode of operation (MODE 2) is a bidirectional bus mode which uses 8 lines for a bidirectional bus, and 5 lines, borrowing one from the other group, for handshaking.

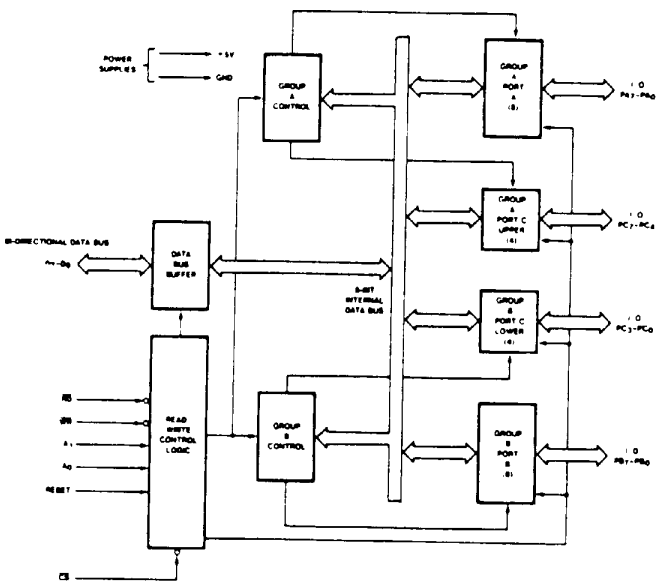
PIN CONFIGURATION



PIN NAMES

D_7-D_0	DATA BUS (BI DIRECTIONAL)
RESET	RESET INPUT
$\overline{CS}$	CHIP SELECT
$\overline{RD}$	READ INPUT
$\overline{WR}$	WRITE INPUT
A0, A1	PORT ADDRESS
PA7-PA0	PORT A (BIT)
PB7-PB0	PORT B (BIT)
PC7-PC0	PORT C (BIT)
V_{CC}	+5 VOLTS
GND	0 VOLTS

8255A BLOCK DIAGRAM



ADDENDUM

ADDENDUM NO:	APPLIES TO (RF Model or Product Name):	DATE:
L836	R-2368/URR	December 1992
ADDENDUM TO (Publication Number/Revision):	**FOR (Specific Application):**	
10215-0022B	All Manuals	

Make the following pen-and-ink changes to the manual and insert this addendum inside the front cover.

SUBSECTION A19 PRESELECTOR

On page 19/20, figure 9, change R19 as indicated in figure 1 of this addendum.

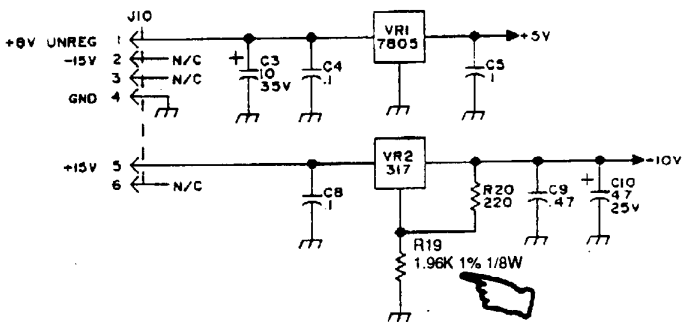


Figure 1. A19A1 PWB Schematic Diagram (10215-6661) (Sheet 1 of 2) Changes

On page 21/22, figure 9, change R5 as indicated in figure 2 of this addendum.

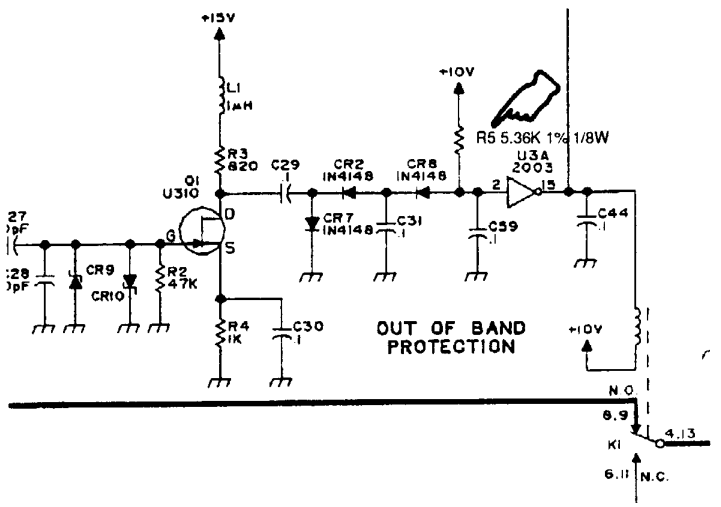


Figure 2. A19A1 PWB Schematic Diagram (10215-6661) (Sheet 2 of 2) Changes

HARRIS CORPORATION RF COMMUNICATIONS GROUP ROCHESTER, NEW YORK 14610 USA

ADDENDUM

ADDENDUM NO:	APPLIES TO (RF Model or Product Name):	DATE:
L836	R2368/URR	December 1992

On page 21/22, figure 9, change R9 as indicated in figure 3 of this addendum.

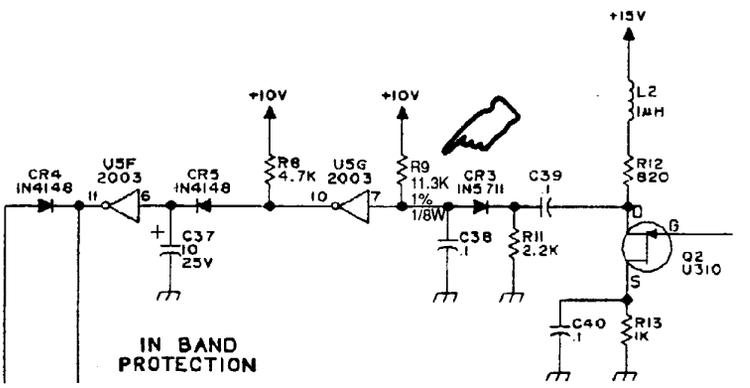


Figure 3. A19A1 PWB Schematic Diagram (10215-6661) (Sheet 2 of 2) Changes

On page 13, table 3, make the following changes:

- Change the R5 part number from R65-0003-472 to RN55D5361F, and change the description from "RES 4.7K 5% 1/4W CAR FILM" to "RES, 5.36K, 1%, 1/8W"
- Change the R9 part number from R65-0003-103 to RN55D1132F, and change the description from "RES 10K 5% 1/4W CAR FILM" to "RES, 11.3K, 1% 1/8W"
- Change the R19 part number from R65-0002-152 to RN55D1961F, and change the description from "RES 1.5K 5% 1/4W CAR FILM" to "RES, 1960, 1%, 1/8W"

ADDENDUM

FOR INSTRUCTION MANUAL:	ADDENDUM NO:	DATE:
10215-0020A and 10215-0022A	L682	March 1989
APPLIES TO: RF-590A and R-2368/URR	**FOR:** All Manuals	

OPERATION SECTION

Immediately following paragraph 3.6.2.3, add the note "See addendum L682 for Stop Scan information"

3.6.3 Stop Scan Operation

The Auto Stop Scan software allows the receiver to automatically stop scanning when a received signal exceeds a predetermined threshold. Scanning will resume automatically when the signal falls below the threshold. Paragraphs 3.6.3.1 through 3.6.3.1.6 contain operating instructions for the stop scan feature.

3.6.3.1 Initial Receiver Setup

The receiver should be powered-up and configured for non-remote operation. The left-hand RF button below the front panel meter should be depressed. The front panel SCAN button should be depressed. The following message will then be displayed: "GROUP OR CHANNEL SCAN?". See paragraph 3.6.3.1.1 for the CHANNEL scan or paragraph 3.6.3.1.2 for GROUP scan setup.

3.6.3.1.1 Channel Scan Setup

To select the CHANNEL scanning mode depress the CHANNEL button. The following message will be displayed: "FIRST CHANNEL?", followed by a two-digit channel number. Enter the lowest channel to be scanned by using the numeric keypad. After entering the channel number, depress the ENTER button. The following message will be displayed: "LAST CHANNEL?", followed by a two-digit channel number. Use the numeric keypad to select the highest channel to be scanned. After the channel number has been selected, depress the ENTER button.

3.6.3.1.2 Group Scan Setup

To select the GROUP scanning mode depress the GROUP button. The following message will be displayed: "GROUP NUMBER"?, followed by a single-digit group number. Use the numeric keypad to enter the desired group number. Depress the ENTER button. If the message "ANOTHER GROUP?" appears, the selected group has not been programmed. Refer to the equipment manual for channel and group programming instructions.

3.6.3.1.3 Auto Stop Scan ON/OFF Selection

At this point the following message will be displayed: "AUTO STOP SCAN", followed by either "ON" or "OFF". The BFO Button will switch the displayed text between "ON" and "OFF". When the desired selection has been made the ENTER button should be depressed. If Auto Stop Scan is turned off the channel scanning will begin immediately.

HARRIS CORPORATION RF COMMUNICATIONS GROUP ROCHESTER, NEW YORK 14610 USA

ADDENDUM

FOR INSTRUCTION MANUAL:	ADDENDUM NO:	DATE:
10215-0020A and 10215-0022A	L682	March 1989

3.6.3.1.4 Auto Stop Scan Threshold Selection

If Auto Stop Scan is turned on the following message will be displayed: "STOP THRESHOLD", followed by a two-digit threshold value (00 - 99). The operator may enter a threshold value by using the keypad or by turning the tuning wheel. The ENTER button should not be depressed until the desired threshold value is selected. When entering digits from the numeric keypad, the threshold display will wrap around if more than two digits are entered. The front panel meter will display the corresponding received signal strength while the threshold value is being selected. A received signal of equal or greater strength will cause the receiver to automatically stop the scanning process. When the desired threshold value has been selected the ENTER button should be depressed. At this point the receiver will begin scanning.

3.6.3.1.5 Auto Stop Scan Indication and Control

When a signal on the current channel that is equal to or greater than the programmed stop scan threshold value is detected, the receiver will remain on that channel and the SCAN light will flash. If the operator does not intervene and the channel's signal strength falls below the threshold, the receiver will resume scanning on the next channel. If the operator depresses the SCAN button while the SCAN light is flashing the SCAN light will remain on constantly and the receiver will remain on the current channel. This will happen even if the received signal strength falls below the stop scan threshold. The operator must depress the SCAN button a second time to allow the receiver to continue scanning. This feature also allows the operator to skip over a channel that is receiving a strong signal. When the SCAN button is depressed a second time the receiver will go to the next channel, regardless of the received signal strength.

3.6.3.1.6 Receivers with Internal Preselectors

When a receiver that contains an internal preselector is actively scanning, the preselector is placed into the BYPASS mode. A small amount of attenuation exists in the preselector when it is not bypassed. This should be considered when setting stop scan thresholds. When the receiver is in the RCV mode or when scanning has been halted by depressing the SCAN button, the preselector will leave the BYPASS mode. To observe the amount of attenuation present when the preselector is not bypassed, place the receiver into the SCAN mode with a long DWELL time. While observing the RF signal strength meter, depress the SCAN button once. This will cause the scanning to stop and the preselector to leave BYPASS. Note the slight drop in the RF meter indication.

RF P 1488 D

HARRIS CORPORATION RF COMMUNICATIONS GROUP ROCHESTER, NEW YORK 14610 USA

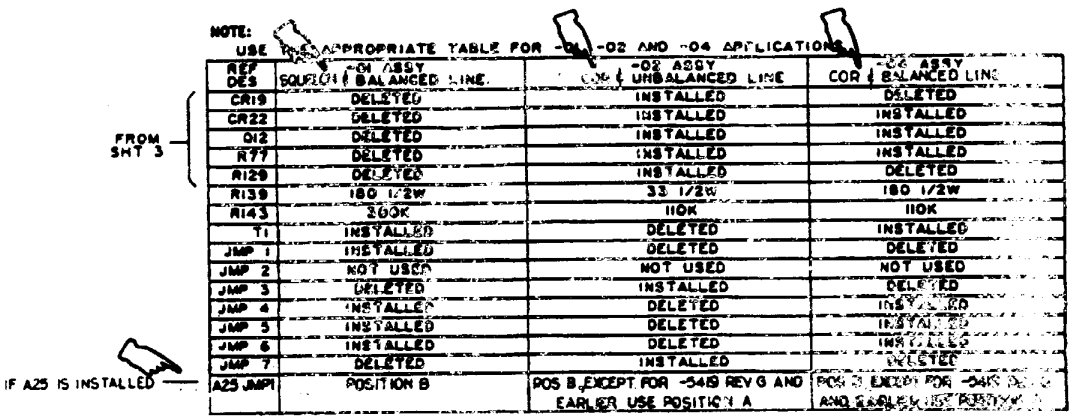
ADDENDUM

ADDENDUM NO:	APPLIES TO (RF Model or Product Name):	DATE:
L783	R-2368/URR Radio Receiver Instruction Manual	February 1992
ADDENDUM TO (Publication Number/Revision):	**FOR (Specific Application):**	
10215-0022B	All Manuals	

Make the following pen-and-ink changes to the manual, and insert this addendum inside the front cover.

A5 IF/AUDIO SECTION

- Page 31/32, figure 4, change the table in this figure as indicated in figure 1 of this addendum.



REF DES	-01 ASSY SQUELCH & BALANCED LINE	-02 ASSY COR & UNBALANCED LINE	-03 ASSY COR & BALANCED LINE
CR19	DELETED	INSTALLED	DELETED
CR22	DELETED	INSTALLED	INSTALLED
D12	DELETED	INSTALLED	INSTALLED
R77	DELETED	INSTALLED	INSTALLED
R129	DELETED	INSTALLED	DELETED
R139	180 1/2W	33 1/2W	180 1/2W
R143	330K	110K	110K
T1	INSTALLED	DELETED	INSTALLED
JMP 1	INSTALLED	DELETED	DELETED
JMP 2	NOT USED	NOT USED	NOT USED
JMP 3	DELETED	INSTALLED	DELETED
JMP 4	INSTALLED	DELETED	INSTALLED
JMP 5	INSTALLED	DELETED	INSTALLED
JMP 6	INSTALLED	DELETED	INSTALLED
JMP 7	DELETED	INSTALLED	DELETED
A25 JMP1	POSITION B	POS B EXCEPT FOR -5419 REV G AND EARLIER USE POSITION A	POS B EXCEPT FOR -5419 REV G AND EARLIER USE POSITION A

Figure 1. 10215-5411 Schematic Changes

A25 EMP/EMI SUPPRESSION SECTION

- Page 5/6, figure 2, change note 5 as indicated in figure 2 of this addendum, and change the schematic per figure 3. 10215-5419 is the revised PWB artwork etched on the board.

5.

IF AUDIO CONFIGURATION AS -(10215-5410)		JMP1 POSITION A	JMP1 POSITION B
-01	SQUELCH & BALANCED LINE		ALL REV'S
-02	COR & UNBALANCED LINE	-5419 REV G AND EARLIER. REV H AND LATER CAN BE A OR B.	
-03	COR & BALANCED LINE	-5419 REV G AND EARLIER.	-5419 REV H AND LATER.

Figure 2. 10215-6851 Note Change

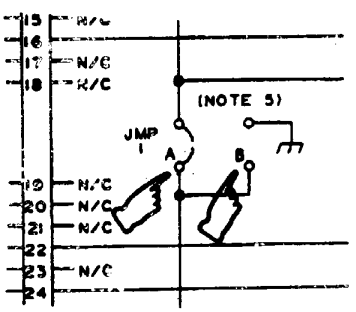


Figure 3. 10215-6851 Schematic Changes

HARRIS CORPORATION RF COMMUNICATIONS GROUP ROCHESTER, NEW YORK 14610 USA