PUBLICATION NUMBER: 10121-0120D
JANUARY 1992

HARRIS

RF COMMUNICATIONS

RF-1310A SERIES EXCITER

INSTRUCTION MANUAL

HARRIS

LIMITED ONE YEAR WARRANTY
HARRIS CORPORATION (RF COMMUNICATIONS GROUP)

FROM HARRIS TO YOU – This warranty is extended to the original buyer and applies to all Harris Corporation, RF Communications Group equipment purchased and employed for the service normally intended, except those products specifically excluded.

WHAT WE WILL DO – If your Harris Corporation, RF Communications Group equipment purchased from us for use outside the United States fails in normal use because of a defect in workmanship or materials within one year from the date of shipment, we will repair or replace (at our option) the equipment or part without charge to you, at our factory. If the product was purchased for use in the United States, we will repair or replace (at our option) the equipment or part without charge to you at our Authorized Repair Center or factory.

WHAT YOU MUST DO – You must notify us promptly of a defect within one year from date of shipment. Assuming that Harris concurs that the complaint is valid, and is unable to correct the problem without having the equipment shipped to Harris:

- Customers with equipment purchased for use outside the United States will be supplied with information for the return of the defective equipment or part to our factory in Rochester, NY, U.S.A., for repair or replacement. You must prepay all transportation, insurance, duty and customs charges. We will pay for return to you of the repaired/replaced equipment or part, C.I.F. destination; you must pay any duty, taxes or customs charges.
- Customers with equipment purchased for use in the United States must obtain a Return Authorization Number, properly pack, insure, prepay the shipping charges and ship the defective equipment or part to our factory or to the Authorized Warranty Repair Center indicated by us.

Harris Corporation
RF Communications Group
Customer Service
1680 University Avenue
Rochester, NY 14610, U.S.A.

Telephone: (716) 244-5830
Telex: 240313
Cable: RFCOM UR

Harris will repair or replace the defective equipment or part and pay for its return to you, provided the repair or replacement is due to a cause covered by this warranty.

WHAT IS NOT COVERED – We regret that we cannot be responsible for:

- Defects or failures caused by buyer or user abuse or misuse.
- Defects or failures caused by unauthorized attempts to repair or alter the equipment in any way.
- Consequential damages incurred by a buyer or user from any cause whatsoever, including, but not limited to transportation, non-Harris repair or service costs, downtime costs, costs for substituting equipment or loss of anticipated profits or revenue.
- The performance of the equipment when used in combination with equipment not purchased from Harris.
- HARRIS MAKES NO OTHER WARRANTIES BEYOND THE EXPRESS WARRANTY AS CONTAINED HEREIN. ALL EXPRESS OR IMPLIED WARRANTIES OF FITNESS FOR A PARTICULAR PURPOSE OR MERCHANTABILITY ARE EXCLUDED.

SERVICE WARRANTY – Any repair service performed by Harris under this limited warranty is warranted to be free from defects in material or workmanship for sixty days from date of repair. All terms and exclusions of this limited warranty apply to the service warranty.

IMPORTANT – Customers who purchased equipment for use in the United States must obtain a Return Authorization Number before shipping the defective equipment to us. Failure to obtain a Return Authorization Number before shipment may result in a delay in the repair/replacement and return of your equipment.

IF YOU HAVE ANY QUESTIONS – Concerning this warranty or equipment sales or services, please contact our Customer Service Department.

ADDENDUM

ADDENDUM NO:	APPLIES TO (RF Model or Product Name):	DATE:
L 874	RF-1310A Exciter	2 December 1993

ADDENDUM TO (Publication Number/Revision):	FOR (Specific Application):
10121-0120D	All manuals

Replace the following pages (17 & 18) in tab section A4 of the RF-1310A Exciter manual.

HARRIS CORPORATION RF COMMUNICATIONS GROUP ROCHESTER, NEW YORK 14610 USA

Table 4. Combiner Assembly A4 Parts List (10121-5500-03) (Cont.)

Ref. Desig.	Part Number	Description
R126, R127	R65-0003-153	RES 15K 5% 1/4W CAR FILM
R128	R65-0003-392	RES 3.9K 5% 1/4W CAR FILM
R129	R65-0003-153	RES 15K 5% 1/4W CAR FILM
R131	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R132	R65-0003-152	RES 1.5K 5% 1/4W CAR FILM
R133	R65-0003-241	RES 240 5% 1/4W CAR FILM
R134	R65-0003-101	RES 100 5% 1/4W CAR FILM
R135	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R136	R65-0003-512	RES 5.1K 5% 1/4W CAR FILM
R137	R65-0003-152	RES 1.5K 5% 1/4W CAR FILM
R138	R65-0003-510	RES 51 5% 1/4W CAR FILM
R139	R65-0003-222	RES 2.2K 5% 1/4W CAR FILM
R140	R65-0003-682	RES 6.8K 5% 1/4W CAR FILM
R141, R142	R65-0003-362	RES 3.6K 5% 1/4W CAR FILM
R143	R65-0003-512	RES 5.1K 5% 1/4W CAR FILM
R144	R65-0003-271	RES 270 5% 1/4W CAR FILM
R145	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R146	R65-0003-101	RES 100 5% 1/4W CAR FILM
R147	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R148	R65-0003-152	RES 1.5K 5% 1/4W CAR FILM
R149	R30-0008-503	RES VAR PCB 50K 1/2W 10%
T1, T2	10073-7026	TRANSFORMER, RF, FIXED
TP0	J-0067	TP PWB BLK TOP ACCS .080"
TP1	J-0071	TP PWB BRN TOP ACCS .080"
TP2	J-0066	TP PWB RED TOP ACCS .080"
TP3	J-0069	TP PWB ORN TOP ACCS .080"
TP4	J-0070	TP PWB YEL TOP ACCS .080"
TP5	J-0068	TP PWB GRN TOP ACCS .080"
U1	I01-0000-156	IC 4094B PLASTIC CMOS
U2	I30-0003-000	IC OP AMP QUAD 324
U3	I30-0003-000	IC OP AMP QUAD 324
U4	I30-0003-000	IC OP AMP QUAD 324
U5	I30-0003-000	IC OP AMP QUAD 324
U6	I30-0003-000	IC OP AMP QUAD 324
U7	I01-0000-005	IC 4002B PLASTIC CMOS
U8	I01-0000-003	IC 4001B PLASTIC CMOS
U9	I01-0000-353	IC 4538B PLASTIC CMOS
VR1	I12-0006-005	IC VR 78L05A +5V .10A 4%

Table 5. Optional Combiner Assembly A4 (10121-5500-01) Part Substitutions

Ref. Desig.	Part Number	Description
A4	10121-5500-01	COMBINER ASSEMBLY
FL1	10073-7311	FILTER, XTAL WIDE DELAY COMP., 455 KHZ LSB
FL4	10073-7310	FILTER, XTAL WIDE DELAY COMP., 455 KHZ USB

Table 6. Optional Combiner Assembly A4 (10121-5500-04) Part Substitutions

Ref. Desig.	Part Number	Description
A4	10121-5500-04	COMBINER ASSEMBLY
FL1	10073-7312	FILTER, XTAL NARROW DELAY COMP., 455 KHZ LSB
FL4	10073-7313	FILTER, XTAL NARROW DELAY COMP., 455 KHZ USB

Table 7. Optional Combiner Assembly A4 (10121-5500-09) Part Substitutions

Ref. Desig.	Part Number	Description
A4	10121-5500-09	COMBINER ASSEMBLY
FL1	10073-7337-01	FILTER, XTAL 455 KHZ USB
FL4	10073-7338-01	FILTER, XTAL 455 KHZ LSB

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RF-1310A SERIES EXCITER

INSTRUCTION MANUAL

HARRIS

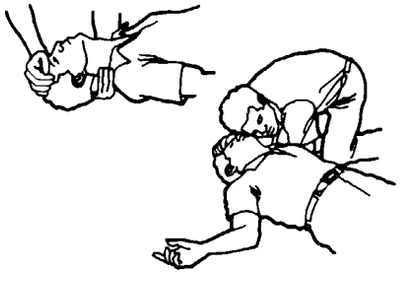
HARRIS CORPORATION RF COMMUNICATIONS GROUP
1680 University Avenue Rochester, New York 14610 USA
Tel.: 716-244-5830 Fax.: 716-244-2917, 716-325-1572 • TELEX: 240313 RFCOM UR

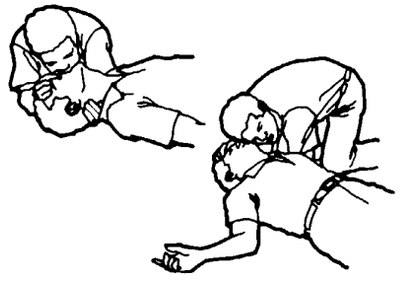
Equipment manufactured by Harris Corporation, RF Communications Group meets stringent quality and safety standards. However, high voltages are present in many radio products, and only a skilled technician should attempt to remove outer covers and make adjustments or repairs. All personnel who operate and maintain the equipment should be familiar with this page as a safety preparedness measure. Although this procedure is reproduced as a service to the personnel involved with this equipment, Harris Corporation assumes no liability regarding any injuries incurred during the operation and repair of such equipment, or the administration of this suggested procedure.

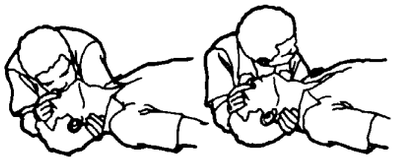
ELECTRICAL SHOCK: EMERGENCY PROCEDURE

The victim will appear unconscious and may not be breathing. If the victim is still in contact with the voltage source, disconnect the power source in a manner safe to you, or remove the victim from the source with an insulated aid (wooden pole or rope). Next, determine if the victim is breathing and has a pulse. If there is a pulse but no breathing, administer artificial respiration. If there is no pulse and no breathing, perform CPR (if you have been trained to do so). If you have not been trained to perform CPR, administer artificial respiration anyway. Never give fluids to an unconscious person.

WHEN BREATHING STOPS







FIRST, send someone to get a **DOCTOR**.
THEN, administer first aid to restore breathing (artificial respiration):

1 IF A VICTIM APPEARS TO BE UNCONSCIOUS
TAP VICTIM ON THE SHOULDER AND SHOUT, "ARE YOU OKAY?"

2 IF THERE IS NO RESPONSE
TILT THE VICTIM'S HEAD, CHIN POINTING UP. Place one hand under the victim's neck and gently lift. At the same time, push with the other hand on the victim's forehead. This will move the tongue away from the back of the throat to open the airway.

IMMEDIATELY LOOK, LISTEN, AND FEEL FOR AIR.
While maintaining the backward head tilt position, place your cheek and ear close to the victim's mouth and nose. Look for the chest to rise and fall while you listen and feel for the return of air. Check for about five seconds.

3 IF THE VICTIM IS NOT BREATHING
GIVE FOUR QUICK BREATHS.
Maintain the backward head tilt, pinch the victim's nose with the hand that is on the victim's forehead to prevent leakage of air, open your mouth wide, take a deep breath, seal your mouth around the victim's mouth, and blow into the victim's mouth with four quick but full breaths just as fast as you can. When blowing, use only enough time between breaths to lift your head slightly for better inhalation.

If you do not get an air exchange when you blow, it may help to reposition the head and try again.

AGAIN, LOOK, LISTEN, AND FEEL FOR AIR EXCHANGE.

4 IF THERE IS STILL NO BREATHING
CHANGE RATE TO ONE BREATH EVERY FIVE SECONDS.

For more information about these and other life-saving techniques, contact your Red Cross chapter for training.
"When Breathing Stops" reproduced with permission from an American Red Cross Poster.

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Frequency Range	405 kHz to 29.99999 MHz
Frequency Resolution	10-Hz increments standard
Tuning	Keypad entry
Tuning Time	Tuning time between any two frequencies is less than 20 milliseconds.
Frequency Stability (Internal)	± 1 part in 10^8 - oven
Frequency Standard I/O	Input - 1 MHz, 5 MHz, or 10 MHz, at 0.5 V_{rms} into 50 ohm load Output - frequency same as input, at 0.5 V_{rms} / 50 ohms (daisy chain feature)
Channel Memory	100-channel capacity, capable of being loaded locally or remotely with complete exciter parameters, retention of operational parameters without power is provided for one month minimum.
Readout/Display	Exciter frequency, mode, channel assignment, carrier reduction, power output reduction, self-test results (vacuum fluorescent), input line audio level (meter), and RF power output level (meter)
Modes of Operation	A1 - CW A2 - MCW A3A - Reduced Carrier (-16, -26 dB) A3H - AME (-6 dB carrier) A3J - USB, LSB A3B - 2 ISB F1 - FSK 6F3 - FM AFSK (Optional Internal Modem) 4 ISB (optional)
Power Output	Nominal 100 mW - Peak or Average Maximum Output - 400 mW
Intermodulation Distortion	-45 dB relative to either tone of a two-tone signal at 100 mW
Signal Processor	Signal clipper with internal adjustment for increased average power for voice or multitone data signals

SPECIFICATIONS FOR RF-1310 MF/HF-SSB SYNTHESIZED EXCITER (Cont.)

Spurious Outputs	-75 dB relative to rated output, except harmonics, which are -40 dB or greater, and unwanted sideband, -65 dB, carrier rejection -65 dB
Inputs	Line 600 ohms, -26 dBm to + 10 dBm; trimpot adjustment or Automatic Level Control (ALC)
Microphone Input	150 ohms, -56 dBm
Sideband Response	300 to 3000 Hz (other filters optionally available)
Built-In Test Diagnostics	Fault isolation to a replaceable module, with front panel display indication
Power Requirements	115/230 Vac, ± 15% 47-63 Hz, 125 watts
Temperature	Operating -10°C to + 55°C Nonoperating -62°C to + 71°C
Humidity	0 to 95%
Size	Rack mount or stack mount - 7 H x 19 W x 20.5 D inches maximum (17.8 H x 48.3 W x 52 D cm)
Weight	40 lbs (18.5 kg)
Remote Control	Internal module. A microprocessor-based system capable of accepting asynchronous serial data in accordance with data standards MIL-STD-188C, EIA RS-232, or RS-422. Functions include frequency, mode, keying, power output level, clipper on/off, and BITE.
4-ISB Adapter	The RF-1314 is an optional external, rack-mounted unit which adds four-channel ISB capability to the basic RF-1310 exciter. Unit includes all external interconnecting cables.

ABOUT THIS MANUAL

Section 1 gives a general description of the exciter and lists some of its key features. Section 2 covers the installation procedure. Section 3 describes the exciter operation. Section 4 covers a general explanation of the exciter circuitry. Section 5 provides BITE self-test information.

The subsections (white tabs) cover each individual exciter assembly. Each subsection covers general information, interface connections, maintenance procedures, parts list, component location diagrams, and schematic diagrams.

All references made to the RF-1310 throughout the manual apply to the RF-1310A.

This RF-1310A Exciter may be supplied with one of two different style front panels. The difference between the two front panels is cosmetic only. Control, operation, or maintenance of the exciter has not changed. The parts lists for each of the panels is supplied in Section A13 of this manual.

RF-1310A SERIES EXCITER

INSTRUCTION MANUAL

HARRIS
RF COMMUNICATIONS

1310-098P

RF-1310A MF/HF SSB Synthesized Exciter

SECTION 1

GENERAL INFORMATION

1.1 SCOPE

Users of this manual should have a basic understanding of radio and digital electronics.

1.2 INTRODUCTION

The RF-1310 is a high performance, fully synthesized, independent sideband exciter. The microprocessor-based design makes the RF-1310 easy to use and maintain while ensuring the unit will meet the needs of the future. The exciter yields a nominal 100 mW RF output over a frequency range of 405 kHz to 29.99999 MHz. It is compatible with high performance transmitter systems including the RF-130, RF-745, RF-755, and RF-1130. The RS-232 and RS-422 compatible remote control interface allows the RF-1310 to be used in computer controlled, integrated communication networks.

The RF-1310 offers fully programmable or manual operation. Up to 100 channels can be programmed with frequency, operating mode, audio source, and output power level. A front panel keypad is provided to make quick, accurate channel and frequency selection. Frequency selections can be made in 10-Hz increments across the entire frequency range. Mode, audio source, and carrier suppression levels are selected by push-buttons. Operating modes include USB, LSB, 2ISB, AME, FM, MCW, CW, FSK, AFSK (Optional Internal Modem), and 4 ISB (optional). Large front panel vacuum fluorescent displays are used to display operating parameters.

Power amplifier modes and output level are controlled from the exciter's front panel. The PA output level can be attenuated up to 50 dB in 1-dB steps from the exciter's front panel keypad. The exciter can provide automatic power control in systems where power level feedback lines are present.

The built-in test equipment (BITE) feature diagnoses and isolates faults to the module level. Easily understandable fault codes are displayed to identify faulty assemblies.

Major assemblies are easily identified and replaced. Major assembly locations are shown in the Major Assembly Location and Interconnect section of this manual.

Options for the RF-1310 include:

- Delay compensated filters; RF-1311-02
- Internal postselector; RF-1317
- 4 ISB operation; RF-1314
- Remote FSK Modem
- Internal AFSK Keyer; RF-1318

The advanced design of the RF-1310 Exciter allows it to be modified and adapted to special applications. Harris/RF Communications Systems Division specializes in developing complete system packages to meet customer needs. Questions concerning any special requirements should be directed to:

Harris Corporation/RF Communications Group
1680 University Avenue
Rochester, New York 14610, USA
Phone: (716)/244-5830
Fax: 716-244-2917, 716-325-1572
Telex: 240313 RFCOM UR

SECTION 2

INSTALLATION

2.1 INTRODUCTION

The following paragraphs provide unpacking and inspection information, equipment installation, mounting instructions, interconnection data, and initial setup and alignment procedures.

2.2 UNPACKING AND INSPECTION

Carefully open the shipping carton and check the contents against the packing list secured to the outside of the container. Inspect all items for signs of damage. Immediately notify the carrier if any damage is discovered. Save all packing material for possible reshipment.

2.3 ANCILLARY KIT

The RF-1310, when purchased as a single unit item, is supplied with an ancillary kit (P.N. 10121-0021). The items contained in the kit are listed in table 2-1. When the exciter is purchased as part of a transmitter, a separate ancillary kit is supplied which supports the entire transmitter. See the appropriate transmitter instruction manual for ancillary kit parts list.

Table 2-1. Ancillary Kit (10121-0021 Rev. K)

Quantity	Part Number	Description
5	F-0026	Fuse, 3AG 2.0 amp, slow-blow
5	F03-0002-005	Fuse, 1/8 amp, slow-blow
5	F03-0002-010	Fuse, 1/4 amp, slow-blow
5	F03-0002-019	Fuse, 1.0 amp, slow-blow
3	J65-0008-103	Jumper 2P FEM .10 CNTR
1	W-0023	Cord, Line, 6 feet
1	Z80-0001-000	Tool, Tuning
1	919-5000	Microphone Assy
1	J22-0001-001	Connector, Type D, 25 pin Fixed
1	J22-0010-000	Connector, Type D, 37 pin Fixed
1	J55-0015-825	Shell, D Connector 25 position*
1	J55-0015-837	Shell, D Connector 37 position*

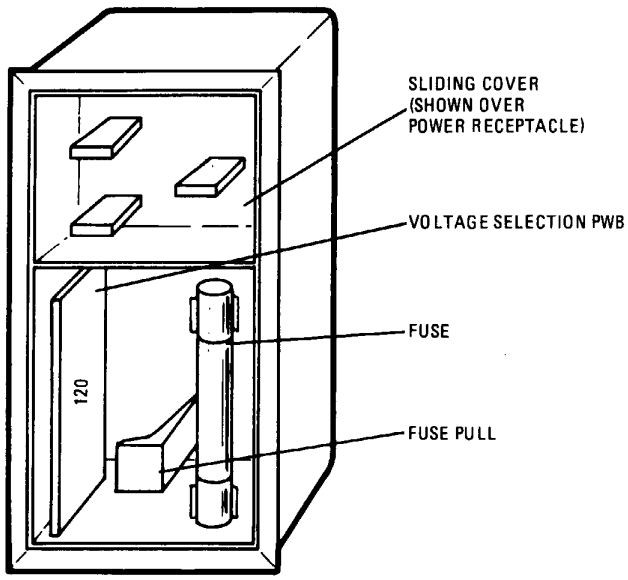
* NOTE: The two D connector shells are provided with various sized grommets to accommodate different sized cables.

2.4 POWER REQUIREMENTS

The RF-1310 requires 100, 120, 220, or 240 Vac, 47 to 420 Hz single-phase power at 125 watts, nominally. Ac power selection is normally factory set to 120 Vac. To select a different range, first turn the front panel power switch off, then remove the ac power cord at the rear panel. Slide the plastic cover out of the way to expose the fuseholder and remove the fuse by pulling on the lever labeled FUSE PULL. Grasp the small PC card (located to the left of the fuseholder) with needlenose pliers and pull the card straight out. This card will be labeled with the numbers 100, 120, 220, and 240 Vac. Orient this card so that the desired range faces the

fuseholder, and is the only number visible once the card has been reinserted. Reinsert the appropriate slow-blow fuse (2 ampere for 120 Vac operation or 1 ampere for 240 Vac operation). A switch on the A23 (+ 24 V Power Supply) assembly, if installed, must also be set for 100/120 or 220/240 Vac operation. This switch may be accessed by removing the top cover. See A23 subsection for switch location. Reconnect power cord. See figure 2-1 for the input filter assembly setup detail.

NOTE: THE INPUT FILTER ASSEMBLY IS PRESET FOR THE CORRECT OPERATING VOLTAGE FOR USE WITH THE RF-755 SET.



TO SELECT OPERATING VOLTAGE:

1. SLIDE FUSE COVER DOOR OVER THE POWER RECEPTACLE.
2. ROTATE FUSE PULL TO THE LEFT.
3. REMOVE VOLTAGE SELECTION PWB.
4. ORIENT VOLTAGE SELECTION PWB TO SHOW DESIRED VOLTAGE WHEN INSTALLED (100, 120, 220, 240 V).
5. PUSH VOLTAGE SELECTION PWB FIRMLY INTO MODULE SLOT.
6. ROTATE FUSE PULL TO ITS ORIGINAL POSITION, AND INSTALL FUSE OF CORRECT RATING.

1310-100

Figure 2-1. Input Filter Assembly Setup Detail

2.5 MECHANICAL INSTALLATION

The RF-1310 may be stack mounted or rack mounted into a standard 19-inch equipment rack. See figures 2-2 and 2-3 for mounting information. Note that two different mounting brackets are supplied for rack mounting. PN 10073-1010 fits the left side of the RF-1310 and PN 10073-1014 fits the right side. The detail drawing in figure 2-3 shows the left side bracket.

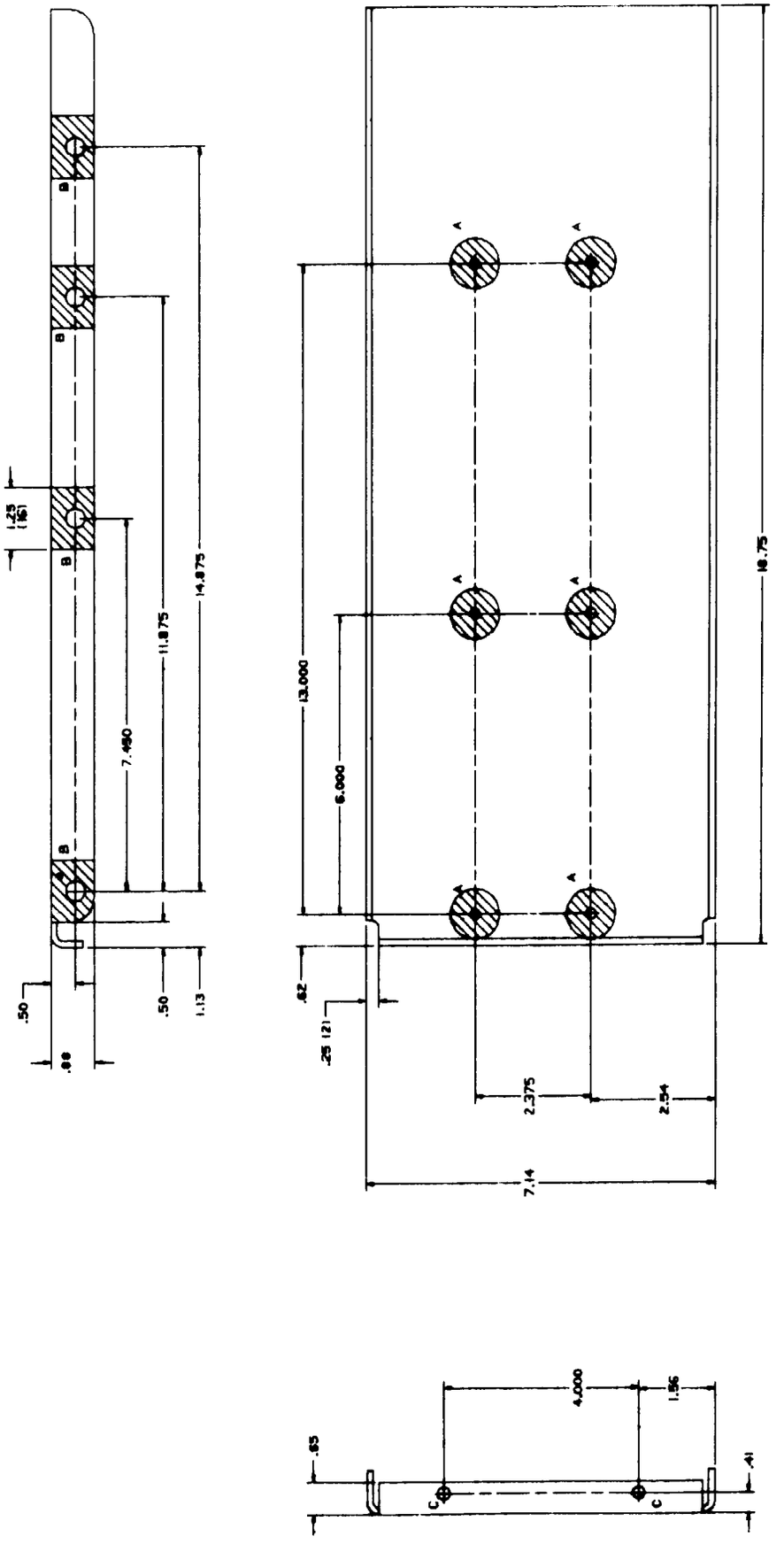


Figure 2-2. RF-1310 Stack Mount Dimensions (10121-0030/31)

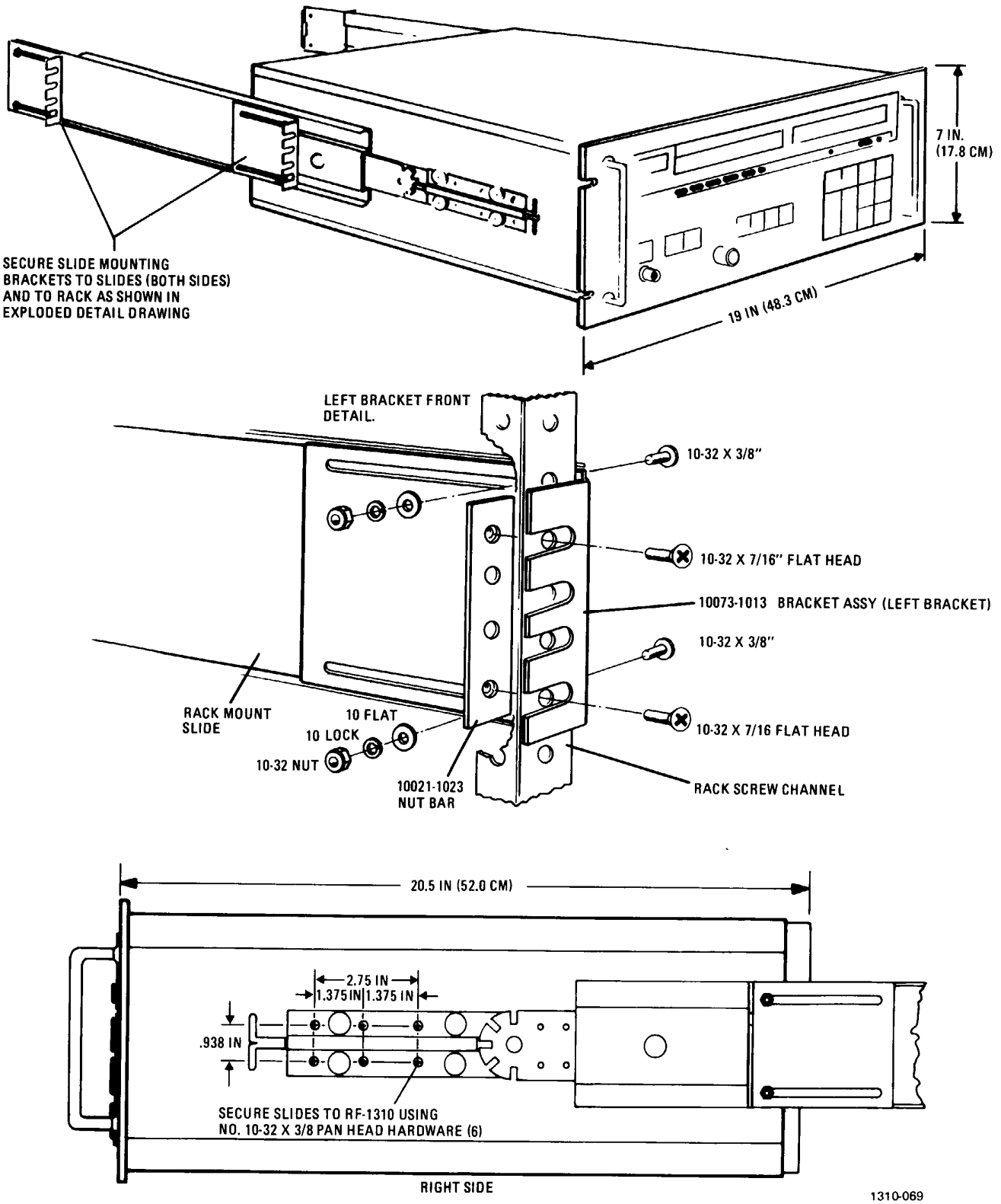


Figure 2-3. RF-1310 Rack Mounting Details

2.6 INPUT/OUTPUT CONNECTIONS

The RF-1310 Exciter is used in a transmitting system independent of all other equipment. It requires power and Exciter-to-PA connections. Other input/output connectors are used to expand and integrate features of the exciter. Input and output connectors are shown and described in figure 2-4.

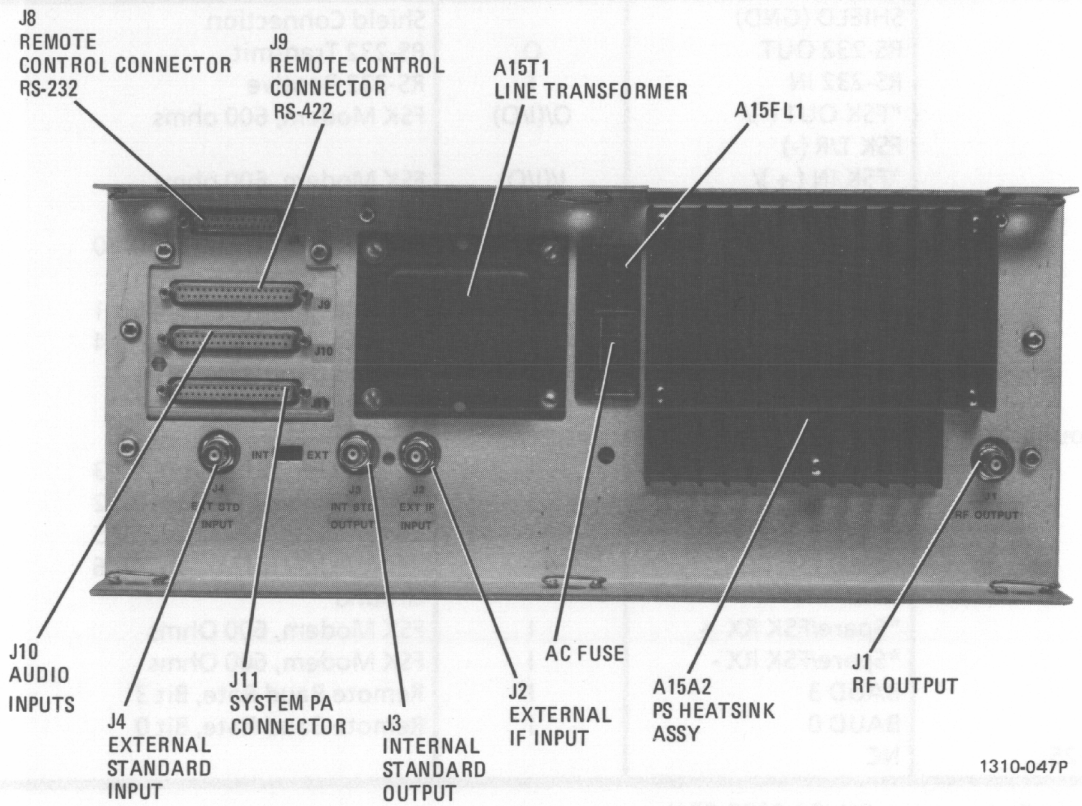


Figure 2-4. RF-1310 Rear Panel Connections

All RF connectors are standard BNC, 50-ohm connections. All rear panel connector pins are listed and described in tables 2-2 through 2-6.

Table 2-2. Coaxial Connectors

Connector	Function	Signal	Type
J1	RF Output	405 kHz - 29.99999 MHz, 100 mW PEP, 50 ohms	BNC
J2	External IF In	455 kHz, 50 ohms, 22 mV_{rms}	BNC
J3	Internal Frequency Standard Output	Approximately .5 - 1 V_{rms} /50 ohms 1, 5, or 10 MHz	BNC
J4	External Frequency Standard Input	1, 5, or 10 MHz - Depends on Internal Standard. Approximately .5 - 1 V_{rms} /50 ohms.	BNC

Table 2-3. Connector J8 - RS-232 Remote Control Signals

Connector Pin	Signal	Exciter Input or Output	Description
J8-1	SHIELD (GND)		Shield Connection
J8-2	RS-232 OUT	O	RS-232 Transmit
J8-3	RS-232 IN	I	RS-232 Receive
J8-4	*FSK OUT (-)/ FSK T/R (-)	O/(I/O)	FSK Modem, 600 ohms
J8-5	*FSK IN (+)/ FSK T/R (+)	I/(I/O)	FSK Modem, 600 ohms
J8-6	ID0	I	Remote Identification, Bit 0
J8-7	RS-232 SIG GND		Signal Ground
J8-8	ID1	I	Remote Identification, Bit 1
J8-9	ID4	I	Remote Identification, Bit 4
J8-10	BAUD 1	I	Remote Baud Rate, Bit 1
J8-11	BAUD 2	I	Remote Baud Rate, Bit 2
J8-12 through J8-14	NC		
J8-15	ID3	I	Remote Identification, Bit 3
J8-16	ID2	I	Remote Identification, Bit 2
J8-17	ID5	I	Remote Identification, Bit 5
J8-18	ID6	I	Remote Identification, Bit 6
J8-19	GND		Ground
J8-20	*Spare/FSK RX +	I	FSK Modem, 600 Ohms
J8-21	*Spare/FSK RX -	I	FSK Modem, 600 Ohms
J8-22	BAUD 3	I	Remote Baud Rate, Bit 3
J8-23	BAUD 0	I	Remote Baud Rate, Bit 0
J8-24, J8-25	NC		

(J8 is a 25 pin D connector, PN J22-0035-001)
*Signal Name is dependent on A17A1 (Remote Control PWB) version installed.

2.7 INITIAL SETUP AND ADJUSTMENTS

The advanced design of the RF-1310 Exciter minimizes initial setup and adjustment procedures. The initial setup and adjustment should include:

- Connecting memory backup battery
- Adjusting front panel display brightness
- Adjusting LSB and USB audio input levels
- Adjusting VOX sensitivity and threshold
- Adjusting maximum RF output level
- Setting system interface switches
- Setting remote control interface configuration (if used)

Table 2-4. Connector J9 - RS-449 Remote Control Signals

Connector Pin	Signal	Exciter Input or Output	Description
J9-1, J9-2	NC		
J9-3	*BUS REQUEST/AUX RS-485 OUT -	I/(O)	Tristate Request/AUX RS-485 TX
J9-4	RS-422 OUT (+)	O	RS-422 Transmit
J9-5	NC		
J9-6	*RS-422 IN (+)/ REM RS-485	I/(I/O)	RS-422 Receive/REM RS-485
J9-7 through J9-18	NC		
J9-19	GND	O	
J9-20	*RS-422 IN (-)/ REM RS-485 -	I/(I/O)	RS-422 Receive/REM RS-485
J9-21	*BUS AVAILABLE/ AUX RS-485 OUT +	O	Tristate Confirm/AUX RS-485 TX
J9-22 through J9-36	NC		
J9-37	RS-422 OUT (-)	O	RS-422 Transmit

(J9 is a 37 pin D connector, PN J22-0035-002)
*Signal Name is dependent on A17A1 (Remote Control PWB) version installed.

Some adjustments may be system specific. Consult the specific system manual for additional setup and adjustment procedures before attempting to operate the exciter in a transmitting system.

CAUTION

Do not short out the memory backup battery terminals. This could result in severe circuit damage.

2.7.1 Connecting Memory Backup Battery

A nickel-cadmium battery is used to keep the RAM memory alive when power is removed from the exciter. The backup battery is located on the A14 Control Board assembly. The backup battery jumper must be inserted between E1 and E2 on the A14 Control Board assembly to activate the keep-alive circuit. See subsection A14 for location of the assembly and the jumper.

2.7.2 Adjusting Front Panel Display Brightness

Potentiometer R29 on Front Panel Driver Board assembly A13A2 is used to adjust the brightness of the vacuum fluorescent displays. R29 can be reached by removing the chassis top cover or tilting the front panel assembly forward. R29 can be adjusted with a small screwdriver and is identified in subsection A13.

2.7.3 USB and LSB Audio Level Adjust

USB and LSB audio levels are adjustable from the front panel. Adjustment potentiometers are reached through holes located next to the USB and LSB meter select pushbutton switches on the front panel.

Table 2-5. Connector J10 - Audio and Miscellaneous Signals

Connector Pin	Signal	Exciter Input or Output	Description
J10-1	Rear Serial Data	O	TTL Levels
J10-2	4ISB Mode CMD	O	(Optional) 4ISB Enable
J10-3	Rear Serial Clock	O	TTL Levels; occurs only when data is sent
J10-4	Fault	O	TTL HI = Fault LED On
J10-5	4ISB BITE Result	I	(Optional) 4ISB BITE Readback
J10-6	INTERNAL KEY	O	TTL LO = Exciter Keyed
J10-7	AUX PTT KEY	I	LO = Key Down
J10-8	Spare		
J10-9	$\overline{\text{AUX CW KEY}}$	I	TTL LO = Key Down
J10-10	INDEX		
J10-11	TTY -	I	(Optional) AFSK Keyer Input
J10-12	AUX AUDIO 2	I	600 Ohms Balanced; 0 dBm, Nominal
J10-13	TTY +	I	(Optional) AFSK Keyer Input
J10-14	LSB AUDIO INPUT	I	600 Ohms, Balanced Transformer; 0 dBm, Nominal
J10-15	XMIT MUTE	O	TTL LOW = System Keyline Active
J10-16	REM OUT 0	O	Remotely Controlled Output, TTL
J10-17	FSK KEY	I	RS-232 FSK Data Input
J10-18	SERIAL ENABLE 1	O	Strobes Rear Serial Data into External Device
J10-19	PRIMARY FAIL	O	+ 5 V = Primary Failure
J10-20	4ISB ID	I	(Optional) 4ISB Identification
J10-21	GND		Audio Shield Ground
J10-22, J10-23	AUX AUDIO 1	I	600 Ohms Balanced; 0 dBm, Nominal
J10-24	CW SIDE TONE	O	Approximately 1200 Hz; 50 mV_{rms}/600 ohms
J10-25	GND		Audio Shield Ground
J10-26	USB AUDIO INPUT	I	600 Ohms Balanced Transformer; 0 dBm
J10-27	NC		
J10-28	USB AUDIO INPUT	I	600 Ohms Balanced Transformer; 0 dBm, Nominal
J10-29	AUX AUDIO 2	I	600 Ohms Balanced; 0 dBm, Nominal
J10-30	4ISB BITE CMD	O	(Optional) 4ISB BITE Enable
J10-31	REMOTE OUT 1	O	Remotely Controlled Output, TTL
J10-32	SERIAL ENABLE 2	O	Strobes Rear Serial Frequency Data into External Device
J10-33	LSB AUDIO IN CENTER TAP		Transformer Center Tap
J10-34	USB AUDIO IN CENTER TAP		Transformer Center Tap
J10-35	LSB AUDIO INPUT	I	600 Ohms Balanced Transformer; 0 dBm, Nominal
J10-36	AUX AUDIO 3 (RTN)	I	600 Ohms Balanced; 0 dBm, Nominal (not used when AFSK Keyer option is installed)
J10-37	AUX AUDIO 3	I	600 Ohms Balanced; 0 dBm, Nominal (not used when AFSK Keyer option is installed)

(J10 is a 37 pin D connector, PN J22-0035-002)

Table 2-6. Connector J11 - System and PA Connections

Connector Pin	A18A2 Signal Names (10121-6350 Version)	A18A2 Signal Names (10121-6370 Version)	A18A2 Signal Names (10121-6390 Version)
J11-1	PA BND SW CODE C	PA BND SW CODE C	XCTR DATA +
J11-2	NC	STANDBY READBACK	NC
J11-3	PA BND SW CODE E	PA BND SW CODE A	XCTR DATA -
J11-4	NC	NC	NC
J11-5	BYPASS REQUEST	TUNE CMD 1	NC
J11-6	SYS KEY	SYS KEY	SYS KEY
J11-7	APC	10 KW FORWARD (APC)	10 KW FORWARD (APC)
J11-8	CHASSIS GND	CHASSIS GND	CHASSIS GND
J11-9	PTT RTN	PTT RTN	PTT KEY
J11-10	NC	NC	NC
J11-11	SYSTEM KEY LINE INTLK	PA READY	AUX RS-422 TX -
J11-12	SYS TUNE PWR REQUESTS	TUNE ENABLE	AUX RS-422 TX +
J11-13	PA CLASS	NC	NC
J11-14	BYPASS	PA BYPASS	NC
J11-15	NC	PPC	PPC
J11-16	STBY CMD	STBY CMD	NC
J11-17	CHASSIS GND	CHASSIS GND	CHASSIS GND
J11-18	PA BND SW CODE B	PA BND SW CODE D	AUX RS-422 RX -
J11-19	OPER CMD	OPER CMD	MC DATA +
J11-20	INDEX	INDEX	INDEX
J11-21	NC	10 KW REFLECTED	NC
J11-22	NC	TGC	TGC
J11-23	CW KEY	CW KEY	CW KEY
J11-24	PA FAULT	FAULT	NC
J11-25 through J11-28	N/C	N/C	N/C
J11-29	NC	OPER READBACK	NC
J11-30	PTT KEY (FLOAT + 12 V)	NC	NC
J11-31	NC	NC	NC
J11-32	NC	TUNE CMD 2	NC
J11-33, J11-34	NC	NC	NC
J11-35	PA BND SW CODE D	PA BND SW CODE B	NC
J11-36	PA BND SW CODE A	PA BND SW CODE E	AUX RS-422 RX +
J11-37	SYSTEM RETUNE CMD	INHIBIT	MC DATA -

J11 is a 37 pin D connector, PN J22-0035-002)

NOTE

The signal names shown in table 2-6 are the most commonly used signal names for the three versions of the A18A2 System Interface. Some signal names may change at the exciter/ PA interface. Consult the appropriate system manual for specific system signals.

Turn the potentiometer to full clockwise (cw) for full RF power output with -26 to + 10 dBm audio input (ALC on). If ALC is off, adjusting the potentiometer counterclockwise (ccw) will reduce audio gain and RF power output level.

2.7.4 VOX Adjustments

Vox operation is an option, selectable from the front panel. See section 3 (Operation) to select VOX option.

VOX sensitivity and hangtime are adjusted on the A5A1 Audio 1 assembly. VOX sensitivity is adjusted by R41 and hangtime is adjusted by R46. See subsection A5A1 for adjustment locations and VOX circuit description.

The sensitivity adjustment (R41) sets the threshold to where the audio input will key the exciter. Sensitivity can be adjusted so that the exciter will be keyed by an audio input level between -26 and + 10 dBm. Hangtime is the length of time the exciter remains keyed after the audio input drops below the VOX threshold. The hangtime can be adjusted from 0.1 to 3.0 seconds.

2.7.5 RF Output Adjust

The maximum RF output is adjustable over an 8 dB range. R26 on the Converter assembly A2 is normally set so the exciter has a nominal 100 mW output. The location of R26 is shown in subsection A2.

2.7.6 System Interface Switches and Adjustments

All of the switch settings and adjustments on the System Interface Assembly A18 are system specific. See the specific system manual in order to determine what the switch settings and adjustments should be. Switches and adjustments are described in subsection A18.

2.7.7 Remote Control Interface Configuration

For remote control interface configuration setup procedure, see unit instruction subsection A17.

2.7.8 Signal Generator Mode

The exciter may be used as a frequency synthesized signal generator. This feature can be used to check the exciter's own performance or to troubleshoot other equipment. It provides a nominal 100 mW RF output from 0.1 to 30 MHz. Frequency and RF output power reduction are front panel selectable.

To select signal generator mode, set switch A18A1S1-4 SIG GEN/NORM to OPEN. See subsection A18A1 for the location of the switch.

SECTION 3

OPERATION

3.1 INTRODUCTION

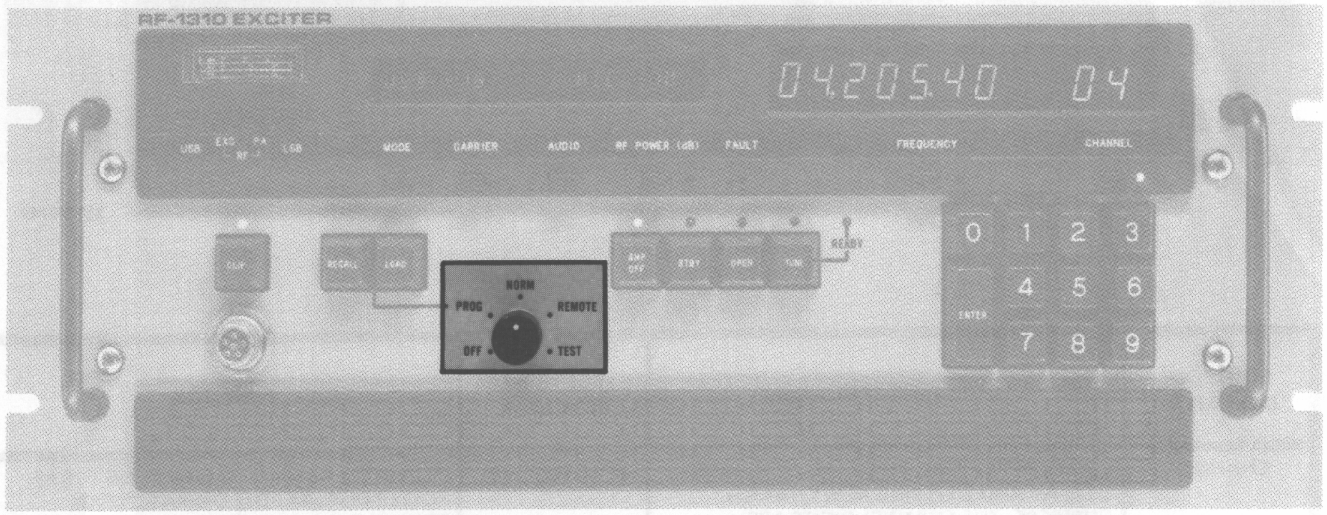
This section describes the front panel controls and indicators of the RF-1310 and their general operation. Actual operation depends on the specific application and built-in optional features. Consult the system manual before attempting to operate the exciter in an operational system.

3.2 CONTROLS AND INDICATORS

The controls and indicators are arranged in functional groups and are described in paragraphs 3.2.1 through 3.2.7.

3.2.1 Rotary Switch

The On/Off rotary switch is shown and described in figure 3-1.



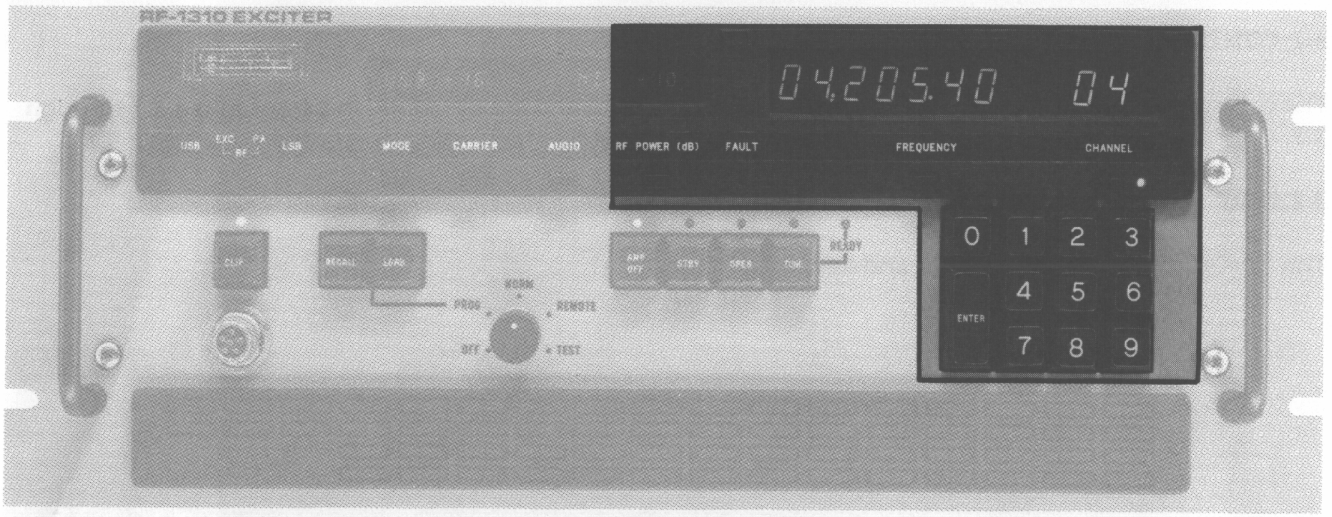
SWITCH POS.	FUNCTION	SWITCH POS.	FUNCTION
OFF	POWER IS DISCONNECTED FROM ALL ASSEMBLIES EXCEPT FREQ. STD. OVEN. POWER IS SUPPLIED TO ALL ASSEMBLIES WHEN SWITCH IS IN ANY OTHER POSITION.	NORM	PLACES EXCITER IN LOCAL OPERATING MODE.
		REMOTE	PLACES EXCITER IN REMOTE OPERATING MODE. DISABLES ALL FRONT PANEL CONTROLS.
PROG	PLACES EXCITER IN PROGRAM MODE AND ENABLES **RECALL, LOAD** AND **OPER** SWITCHES. EXCITER IS NOT OPERATIONAL WHILE IN PROGRAM MODE.	TEST	INITIATES **BITE** FEATURE.

1310-060

Figure 3-1. On/Off and Mode Select Rotary Switch

3.2.2 Keypad Entries (Channel, Frequency, and RF Power)

The keypad is used to change the channel, frequency, and RF power displays. The ENTER key is used to place the displayed data into the exciter's memory. The displays will dim as they are changed. The displays return to full brightness when the ENTER key is pressed. LED indicators next to CHANNEL, FREQUENCY, and RF POWER pushbuttons light to indicate which display will be changed by keypad entries. All three functions can be selected in normal and program operating modes. Figure 3-2 shows and describes the keypad entries.



1310-074P

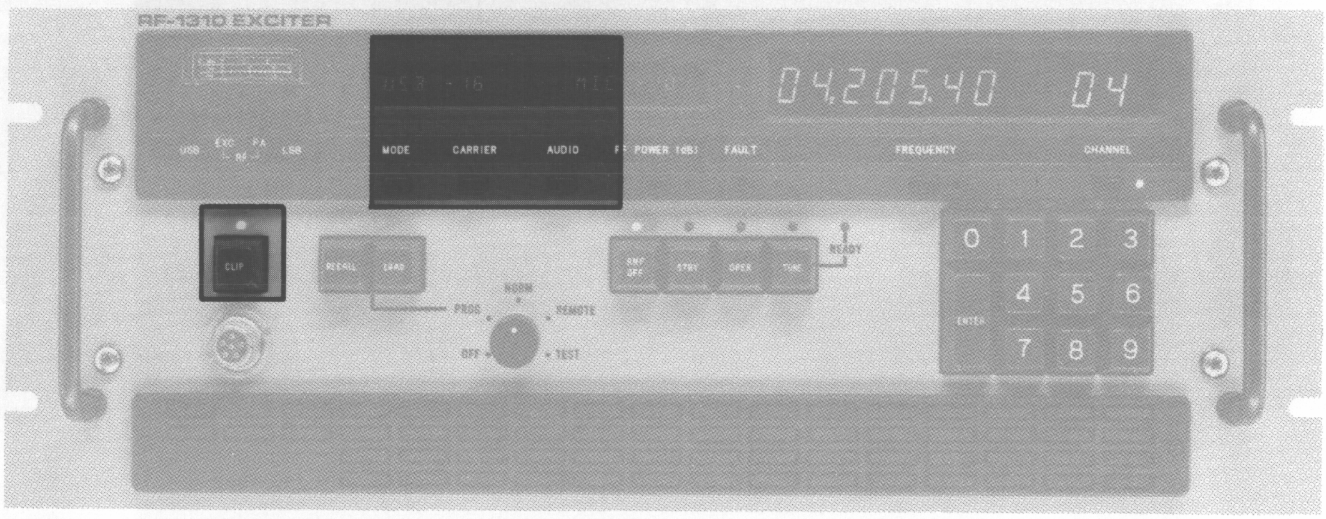
CONTROL/ INDICATOR	FUNCTION	CONTROL/ INDICATOR	FUNCTION
CHANNEL	DEDICATES KEYPAD TO CHANGING CHANNEL DISPLAY AND ENTERING NEW CHANNEL NUMBERS. THE CHANNEL DIGITS ARE ENTERED FROM LEFT TO RIGHT.	RF POWER (DB)	DEDICATES KEYPAD TO CHANGING THE RF POWER DISPLAY. THE OPERATOR CAN REDUCE THE PA OUTPUT BY UP TO 50 DB. THE DISPLAY INDICATES THE SELECTED POWER REDUCTION IN DB. THE TWO DIGITS ARE ENTERED FROM LEFT TO RIGHT.
FREQUENCY	DEDICATES KEYPAD TO CHANGING FREQUENCY DISPLAY AND ENTERING A NEW FREQUENCY SELECTION. DIGITS ARE ENTERED FROM LEFT TO RIGHT.	ENTER	ENTERS ENABLED DISPLAY INTO THE EXCITER'S RAM MEMORY. ALSO USED TO CLEAR FAULT CODES OR MESSAGES FROM DISPLAY.

1310-061

Figure 3-2. Keypad Entries

3.2.3 Mode, Carrier Suppression, Audio Input, and Clip Select

The MODE, CARRIER, and AUDIO pushbuttons are used to select the mode of operation, carrier suppression, and audio source for each channel. The operator can step through the options for each parameter by pushing and releasing the respective button. Options will appear on the display above the button. The exciter will scroll through the available options continuously when the operator holds down the button for a parameter. The CLIP pushbutton enables or disables the clip function. Figure 3-3 shows and describes the MODE, CARRIER, AUDIO, and CLIP controls.



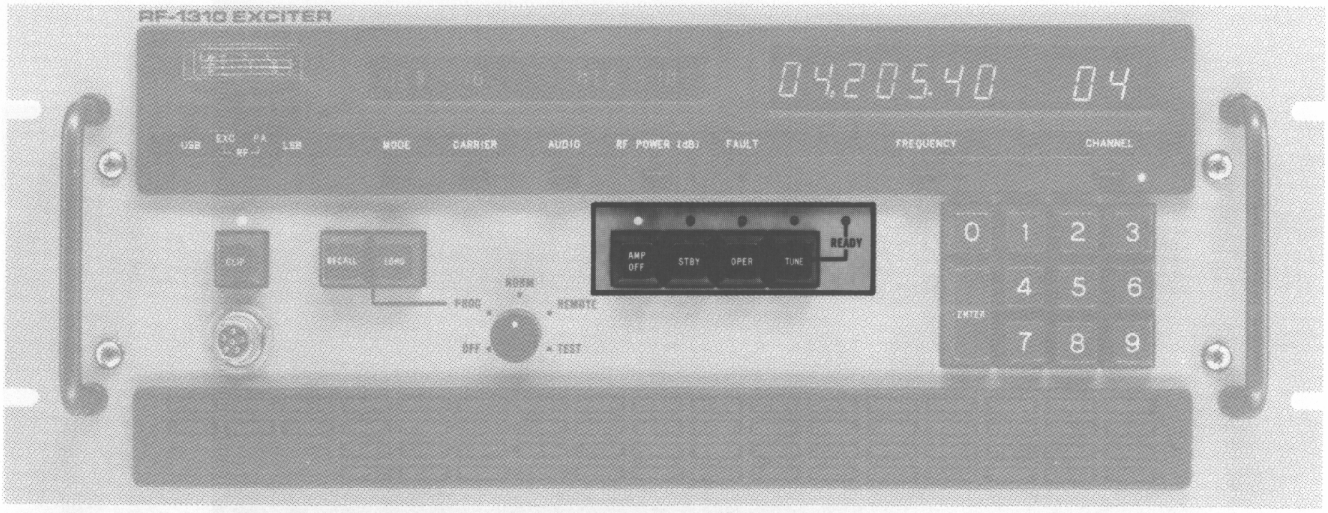
CONTROL/ DISPLAY	FUNCTION	CONTROL/ DISPLAY	FUNCTION
MODE	CONTROLS DISPLAY AND SELECTION OF EXCITER OPERATING MODE. AVAILABLE MODES ARE **USB, LSB, 2ISB (ISB), 4ISB (4SB), MCW, FM, FSK, CW, AFSK (AFK)**, AND **AM**. 4ISB AND AFSK OPERATION IS OPTIONAL.	AUDIO	CONTROLS DISPLAY AND SELECTION OF AUDIO SOURCE. REFER TO TABLE 3-1.
CARRIER	CONTROLS DISPLAY AND SELECTION OF CARRIER SUPPRESSION. SELECTIONS ARE LIMITED BY OPERATING MODE. FOR USB, LSB, 2ISB AND 4ISB, -16 DB, -26 DB AND -INFINITY (BLANK DISPLAY) ARE SELECTABLE. FOR AM LEVEL IS SET AT -6 DB AND CANNOT BE CHANGED. FOR CW, FM, FSK AND AFSK, THE DISPLAY WILL BE BLANK.	CLIP	ENABLES OR DISABLES CLIPPER CIRCUIT IN EXCITER. LED IS ON WHEN ENABLED. MAY BE ENABLED ONLY IN USB, LSB, 2ISB, 4ISB, AND AM MODES.

1310-062

Figure 3-3. MODE, CARRIER, AUDIO, and CLIP Controls

3.2.4 Power Amplifier Controls and Indicators (AMP OFF, STBY, OPER, and TUNE)

The AMP OFF, STBY, OPER, and TUNE pushbuttons are used to control the system power amplifier (PA). The LED indicators located above the switches indicate the status of the PA. The controls are shown and described in figure 3-4. The operator should refer to the specific system manual for a detailed description of PA operation.



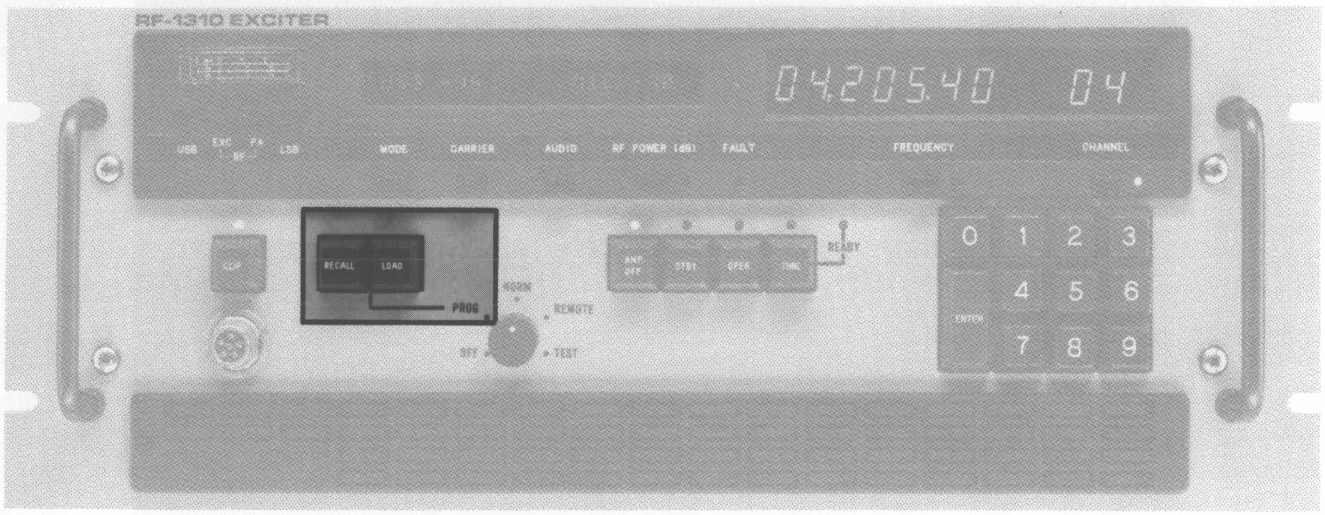
CONTROL/ INDICATOR	FUNCTION	CONTROL/ INDICATOR	FUNCTION
AMP OFF	USED TO TURN PA OFF. CAN BE ACTIVATED WHEN PA IS IN STANDBY OR OPERATE MODES. PA IS FORCED TO **AMP OFF** STATE UPON EXCITER POWER-UP.	OPER	PLACES PA IN OPERATE MODE. IN MOST SYSTEMS PA WILL NOT BECOME OPERATIONAL UNTIL WARM-UP IS COMPLETE. ALSO USED IN PROGRAM MODE TO ENABLE OPTION PARAMETERS PROGRAMMING.
STBY	PLACES PA IN STANDBY. (IN SOME SYSTEMS PA WILL NOT GO INTO STANDBY UNTIL WARM-UP IS COMPLETE.)	TUNE	SWITCH USED TO START TUNE SEQUENCE IN PA AND COUPLER. **TUNE LED** IS LIT DURING TUNING SEQUENCE OR FOR TUNE REQUEST. **READY LED** IS LIT WHEN TUNING IS COMPLETE.

1310-063

Figure 3-4. Power Amplifier Controls and Indicators

3.2.5 RECALL and LOAD

The RECALL and LOAD pushbutton switches are enabled only when the exciter is in program mode. They are used to program frequency, operating mode, carrier suppression level, audio source, clip, and RF power level for each channel. The RECALL switch is also used to recall any cancelled messages or fault codes from the display when in normal mode. The switches are shown and described in figure 3-5.



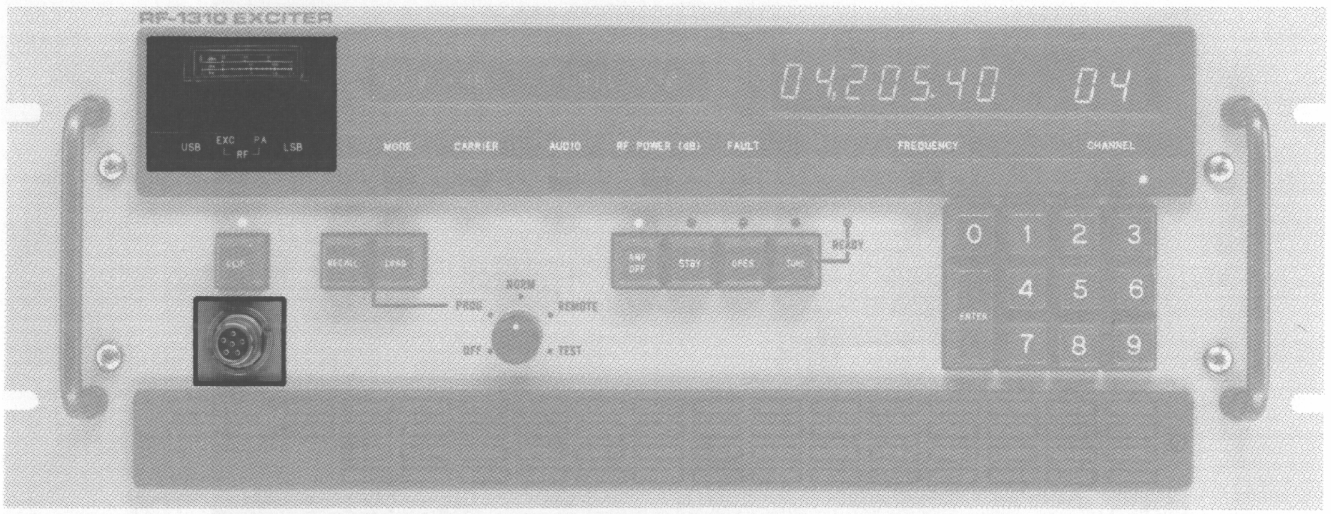
CONTROL	FUNCTION	CONTROL	FUNCTION
LOAD	LOADS ALL DISPLAYED INFORMATION INTO MEMORY.	RECALL	RECALLS AND DISPLAYS OPERATING PARAMETERS FOR SELECTED CHANNEL AND PARAMETERS FOR OPTIONS SELECTED IN PROGRAM MODE. ALSO RECALLS AND DISPLAYS MESSAGES OR FAULTS IN NORMAL MODE.

1310-064

Figure 3-5. RECALL and LOAD Controls

3.2.6 USB, EXC, PA, LSB Meter Select Switches, and Microphone Jack

The meter in the upper left hand corner of the front panel indicates audio and RF signal levels. The four meter select switches are shown and described in figure 3-6. The switches are spring loaded and interconnected so that only one function may be selected at a time.



CONTROL	FUNCTION	CONTROL	FUNCTION
USB	SELECTS METER TO INDICATE USB AUDIO SIGNAL LEVEL ON THE AUDIO ASSEMBLY A5.	AUDIO INPUT ADJUST PORTS	SCREWDRIVER-ADJUSTABLE CONTROLS FOR THE USB AND LSB AUDIO SIGNAL LEVEL ARE ACCESSED THROUGH PORTS ADJACENT TO THE USB AND LSB SWITCHES.
LSB	SELECTS METER TO INDICATE THE LSB AUDIO SIGNAL LEVEL ON THE AUDIO ASSEMBLY A5.	MICROPHONE JACK	-56 DBM NOMINAL INPUT LEVEL INTO 150 OHMS.
EXC	SELECTS METER TO INDICATE THE RF SIGNAL LEVEL AT THE EXCITER OUTPUT. (ACCURATE WHEN OPERATING INTO A 50 OHM LOAD).		
PA	SELECTS METER TO INDICATE THE RF SIGNAL LEVEL AT THE PA OUTPUT.		

1310-065

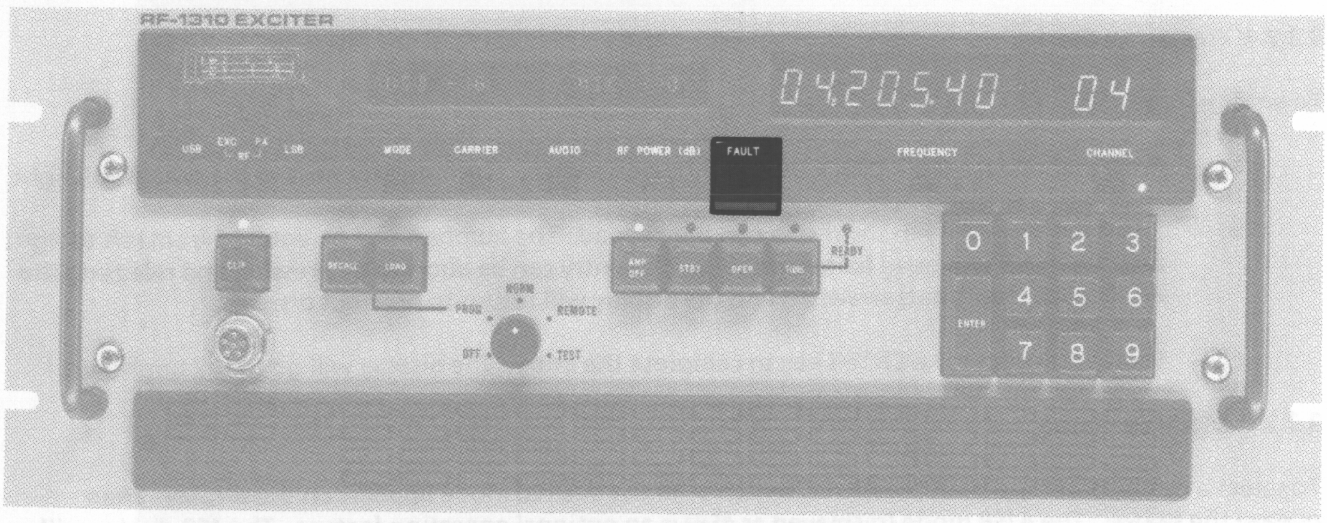
Figure 3-6. Meter Select Switches

3.2.7 FAULT Indicator

NOTE

A fault code indication or synthesizer fault message may be displayed at initial turn on and will remain until the frequency standard stabilizes.

The red FAULT LED indicates that a fault condition exists in the exciter or transmitter system. The indicator is shown and described in figure 3-7. The test mode can be used to isolate and diagnose most fault conditions.



FAULT CONDITIONS DURING NORMAL OPERATION
1. ANY PLL IS OUT-OF-LOCK. 2. POWER SUPPLY VOLTAGE IS OUT OF TOLERANCE. 3. PA FAULT (IF PA FAULT READ BACK LINES ARE PROVIDED).

1310-066

Figure 3-7. FAULT Indicator

3.3 OPERATING GUIDELINES AND CONSIDERATIONS

Operating procedures for the RF-1310 Exciter are system specific and beyond the scope of this manual. The following paragraphs describe the operation of an RF-1310 Exciter installed in a typical system.

3.3.1 Power Up

The exciter enters the power up mode when the rotary switch on the front panel is moved from the OFF position to the PROG, NORM, REMOTE, or TEST position. When the exciter is turned on, the front panel displays and indicators will all be lit while the exciter performs a brief self test. If no faults were detected, the exciter enters the mode of operation selected by the rotary switch. The displays will show the channel (if used), frequency, mode, carrier suppression level, audio source, RF power reduction level, and clip state that

were selected when the exciter was turned off (if memory contains valid data). If the data has been lost or corrupted, the frequency display will be all zeros, the mode display will be USB, the carrier display will be blank (infinity), and the RF power display will show -00.

3.3.2 Operating an Unprogrammed Exciter in Normal Mode

The exciter is in the normal mode whenever the front panel rotary switch is in the NORM position. The normal mode is used for local control of the exciter. The exciter may also be programmed.

To operate an unprogrammed exciter, or to select operating parameters not associated with a programmed channel, the operator must enter all operating parameters individually. No entries will be made in the channel display, it will be blank.

3.3.2.1 Frequency Entries

To enter a frequency:

a. Press and release the FREQUENCY pushbutton switch. The indicator next to the switch will light.

b. Enter the frequency in the display on the keypad. The numbers will be entered from left to right and the digits will be at half brightness. The entry can be aborted by pressing and releasing the FREQUENCY pushbutton switch and the display will return to previous display.

c. Press and release the ENTER key to complete the entry. The display will go to full brightness.

3.3.2.2 Mode Selection

To select a mode, press and hold the MODE switch until the desired mode appears on the display. Then release the switch. The 4 ISB mode (displayed as 4SB) is an optional operating feature. The 4SB display will appear only on exciters with the installed option. The exciter can be configured for AM or AME operation. The display will indicate AM for either configuration.

3.3.2.3 Carrier Suppression Level Selection

The operator can select one of three carrier suppression levels when in the USB, LSB, 2ISB, or 4ISB modes. The choices in these modes are -16 dB, -26 dB, and -infinity or, optionally, -10 dB, -20 dB, and -infinity. Selections are made by pressing and holding the CARRIER switch until the desired level appears on the display above the switch, and then releasing the switch. For -infinity, the operator selects the blank display. Carrier suppression is automatically set at -6 dB for the MCW and AM operating modes. The CARRIER display is blank when operating in FM, FSK, CW, or AFSK modes.

3.3.2.4 Audio Source Selection

The RF-1310 Exciter has a total of six audio inputs. They include the front panel microphone jack and five rear panel 600-ohm input ports LSB, USB, AUX 1, AUX 2, and AUX 3 (not available when A3 AFSK keyer is installed). Allowable audio sources are limited by the selected mode listed in table 3-1.

When the A3 AFSK Keyer is installed for TTY operation the AUX 3 audio input is not available and is replaced with TTN (TTY NORM) and TTR (TTY REV) selections for TTY signal loop.

To select an audio source for USB, LSB, FM, AFSK, or AM modes, simply press and hold the AUDIO switch until the desired source appears on the display above the switch. For the 2ISB and 4ISB modes, the display will list two audio sources. The source for USB will be displayed on the right, the source for LSB will be displayed on

Table 3-1. Audio Source Selection

Mode	Selectable Audio Inputs
USB	MIC, AUX 1, AUX 2, AUX 3 (TTN, TTR when A3 is installed) and USB.
LSB	MIC, AUX 1, AUX 2, AUX 3 (TTN, TTR when A3 is installed), and LSB.
2ISB, 4ISB	Same as for USB and LSB modes. Same source can be used for both side bands.
FM	MIC, AUX 1, AUX 2, AUX 3 (not available when A3 is installed), and LSB.
CW, MCW, FSK	No audio inputs are selected for these modes. Display will be blank.
AFSK	AUX 1, AUX 2, AUX 3 (TTN, TTR when A3 is installed) and USB.
AM	MIC, AUX 1, AUX 2, AUX 3 (not available when A3 is installed) and USB.

the left. The sources displayed will be those last used in the USB and LSB modes. To change the selection for the 2ISB and 4ISB modes, the operator must place the exciter in the individual operating modes.

3.3.2.5 RF Power Control

The operator can reduce the system RF output level by up to 50 dB. The amount of attenuation is displayed above the RF POWER switch. A 00 display indicates that the system output is at its nominal level. To change the display the operator must:

a. Press and release the RF POWER switch. The LED next to the indicator will light.

b. Use the keypad to change the display. Digits are entered from left to right and are dimmed to half brightness as they are changed (e.g. ENTER 06 for 6 dB output power reduction).

c. Press and release the ENTER key to complete the entry. The display will return to full brightness.

3.3.2.6 CLIP Switch

Clipping is used to limit the peak amplitude of the audio signal so the HF radio signal will have a higher average power level. The clipping feature can be selected in the USB, LSB, 2ISB, 4ISB, and AM modes. The feature may not be selected in the FM, FSK, AFSK, CW, and MCW modes. The CLIP pushbutton switch on the exciter front panel is used to enable and disable the clipping circuit. The LED above the switch is lit when the circuit is enabled.

The gain of the clipping amplifier is adjustable, thereby yielding a variable clipping level from 3 dB to 15 dB. Detailed discussion of the clipping circuit and clipping level adjustments are described in subsection A5A2.

3.3.3 Power Amplifier Control

The AMP OFF, STBY, OPER, and TUNE switches are used to control the power amplifier (PA). LEDs above the switches indicate the status of the PA. System response to these controls will depend upon the particular application. The AMP OFF switch is used to turn the PA off. The PA will be forced to AMP OFF status when the exciter is turned on. Pressing and releasing the STBY switch places the PA in standby. The OPER switch is used to change the PA status to operational. Most power amplifiers require a warmup period before they become

operational. The length of the warmup period and the way the PA responds to the OPER switch is system dependent.

The TUNE switch is used to initiate a tune sequence in the PA and antenna coupler if used. The meaning of TUNE and READY indicators is system dependent. Generally, these indicators are both off when the exciter is turned on. After a frequency has been selected and the PA is operational, the tune sequence can be initiated. In most systems, the TUNE indicator will be lit during the tuning sequence. Upon completion of the sequence, the TUNE indicator turns off and the READY indicator comes on.

In some systems, the TUNE indicator is used to show the state of the Tune Power Request Line. In these systems, the TUNE indicator will be lit during the tuning sequence and when the coupler is requesting tuning power.

3.3.4 PROGRAMMING FUNCTIONS

3.3.4.1 Programming Channels

Follow the instructions below to program channels:

a. Select PROG position on rotary switch.

b. Press CHANNEL button, select channel number with keyboard, and press ENTER.

c. Press any of the following buttons to select desired conditions in any order:

- FREQUENCY (Keyboard selectable)
- MODE (Scroll function)
- CARRIER (If valid for mode chosen, scroll function)
- AUDIO (If valid for mode chosen, scroll function)
- RF POWER (Keyboard selectable)
- CLIP (If valid for mode chosen)

For example, to program channel 4 to the following conditions, perform steps a through k:

- FREQUENCY = 10.015 MHz
- MODE = USB
- CARRIER = -16 dB
- AUDIO = MIC
- RF POWER = -5 dB
- CLIP = ON

a. Select PROG position on rotary switch.

b. Press CHANNEL button. Use keyboard to enter 04. Press ENTER.

c. Press FREQUENCY button. Use keyboard to enter 1001500. Press ENTER.

d. Press MODE button. Scroll to USB.

e. Press CARRIER button. Scroll to -16 dB.

f. Press AUDIO button. Scroll to MIC.

g. Press RF POWER button. Use keyboard to enter 05. Press ENTER.

h. Press CLIP button if LED is not already on.

i. Press LOAD button. Channel 4 has now been programmed.

j. To program another channel, press CHANNEL button, and begin process again with new parameters.

k. To conclude programming, place rotary switch in any other position.

Programmed channels are stored in a battery backed up CMOS RAM. At powerup, the microprocessor checks the validity of the RAM and alerts the operator in case of failure by displaying a message on the alphanumeric display on the exciter front panel. Loss or damage to data for any single channel can be detected on powerup, and will cause a reinitialization of that channel to a default of 00.00000 MHz, USB, carrier suppression at - infinity, power reduction 00 dB. Such a frequency will disable keylines, so that the operator will note the channel was lost.

3.3.4.1.1 Recall Function

The recall function allows the operator to view the stored parameters of any channel while programming other channels, without affecting the contents of any channel.

To use RECALL, the exciter must be in the PROG mode. To view the contents:

a. Press CHANNEL.

b. Enter the channel number via the keyboard.

c. Press RECALL.

The display will be updated to the contents of the recalled channel.

3.3.4.2 Programming VOX, ALC, and FSK

The VOX, ALC (ON or OFF), ALC (VOICE or DATA), and FSK options are programmed from the front panel as follows:

a. Select PROG position on rotary switch.

b. Press OPER button.

c. Use the buttons listed below to scroll through and select the options desired:

MODE Button	CARRIER Button	AUDIO Button
VOX	ON or OFF	(Not Active)
ALC (Select)	ON or OFF	MIC, LSB, USB, AUX 1, AUX 2, AUX 3 (not available when AFSK keyer, A3 is installed)
ALC (Function)	VOICE or DATA	LSB, USB, AUX 1, AUX 2, AUX 3 (not available when AFSK keyer, A3 is installed)
FSK	85 Hz, 170 Hz, 425 Hz, or 850 Hz*	(Not active)

*Represents total FSK shift desired.

d. Press the LOAD button to program the selection options.

e. To leave the Option Parameters Programming Mode, Press AMP OFF or move rotary switch to any other position. Using AMP OFF will return exciter to programming mode.

3.3.4.2.1 Recall Button

When programming the option parameters, the recall button allows the operator to view the previously programmed information for a particular parameter, as selected in the mode display. This button is especially useful if the parameter selection has been changed using the CARRIER button.

3.3.5 Operating a Programmed Exciter in Normal Mode

Up to one hundred channels can be programmed with all operating parameters, including frequency, mode, carrier suppression level, audio source, RF power reduction, and clip status. To operate the exciter the user must:

a. Press and release the CHANNEL pushbutton switch.

b. Enter the desired channel number on the keypad.

c. Press and release the ENTER key.

Operating parameters for the selected channel will be displayed as they were programmed (see paragraph 3.3.4.1 for programming channels). After the channel selection is complete, the operator can proceed to system tuneup per the system manual instructions.

The operator can change any of the operating parameters at any time without changing the stored channel data. If any of the parameters are changed, the channel display will go blank to indicate that the displayed parameters were not recalled from memory.

3.4 REMOTE

The REMOTE position on the rotary switch puts the exciter into remote control. When switched into REMOTE, the exciter is set up to the parameters last used in REMOTE, and put into standby. When the exciter is under remote control, all pushbuttons are ignored except the ENTER button. If the exciter is under remote control and the ENTER button is held depressed for several seconds, the alphanumeric display will momentarily show both the baud rate and address that the exciter is configured to for remote control purposes.

3.5 FAULT AND MESSAGE DISPLAY

The RF-1310 display area, located above the MODE, CARRIER, AUDIO, and RF POWER buttons (20 characters), is used to list fault codes and messages generated by the BITE of the exciter and the system in which it is installed.

The fault code display will appear as shown in the example:

XA02 FLT 01

where; X is the prefix number of the faulty unit in the specific system it is installed (see appropriate system manual), A02 indicates a fault has occurred on assembly module A2 within the faulty unit and FLT 01 indicates fault number 1 has occurred on that assembly. Refer to section 5 (maintenance) for the RF-1310 fault code listing. Fault codes for other units within the system can be found in the system manual.

3.6 RF-1310 TEST MODE

The test mode is entered by selecting the TEST position on the exciter rotary switch. Unless in Amp Off state, the exciter immediately enters standby status, then goes into self test, starts a lamp test on the front panel, and performs the following checks:

a. Processor program ROM validity

b. Processor RAM memory functionality

c. Synthesizer lock and data word tests

d. A/D measurement test

e. IF signal path checks

f. RF signal path checks

g. System interface assembly test

h. Remote test

The alphanumeric display informs the operator of test results by displaying the faulty module number and a fault code for that module, or the message TEST PASSED. If all tests pass, but the exciter is using the secondary frequency standard, the alphanumeric display shows PRI FREQ STD FAIL. The STBY or AMP OFF LEDs remain lit after execution of BITE. Turn selector switch to NORMAL to return to regular exciter operation. The Maintenance section of this manual details the BITE tests as well as the module fault codes.

SECTION 4

THEORY OF OPERATION

4.1 INTRODUCTION

This section provides a general description of the RF-1310 functional elements. The description is broken into three parts. The first part (paragraph 4.2) describes the audio, IF, and RF signal paths. The second part (paragraph 4.3) describes the frequency synthesizer. The third part (paragraph 4.4) describes the operation of some circuits and devices that are used extensively in the exciter, including phase lock loops and charge pumps. A dBm to V_{rms} conversion table is also included in this section.

Detailed description of individual assemblies are included in the unit instruction section.

4.2 EXCITER SIGNAL PATH

The primary function of the RF-1310 Exciter is to generate a high frequency radio signal that carries selected audio signals or digital data. Generally, signal processing involves mixing an internally generated 455 kHz carrier with two local oscillator signals to produce an RF output between 0.4 and 30 MHz. The 455 kHz carrier is either modulated by a selected audio input in USB, LSB, ISB, AM, or FM modes or controlled by digital inputs in CW, FSK or AFSK (optional) modes. In the CW mode, the input turns the 455 kHz carrier on and off. In the FSK mode, digital inputs using RS-232 interface, shift the carrier by up to ± 425 Hz. For AFSK mode, an internal (optional) or external keyer assembly is used as the audio source (into AUX 3 audio input) in sideband mode. Signal path filtering and automatic level control (ALC) circuits ensure that the exciter produces a spurious free output signal with a constant power level.

The signal path is shown in figure 4-1 and is made up of the following assemblies.

- Audio Assembly A5
- Combiner Assembly A4
- Converter Assembly A2
- Output Amplifier Assembly A1
- System Interface Assembly A18

The 455 kHz carrier, 40 MHz local oscillator number 2 (LO 2) signal and 40.465 to 70.455 MHz local oscillator number 1 (LO 1) signal are generated by the frequency synthesizer. Control signals and BITE features are provided by Control Assembly A14.

4.2.1 Audio Assembly A5

The role of Audio Assembly A5 depends on the exciter operating mode. In the USB, LSB, ISB, and AM modes, A5 selects and amplifies the audio inputs and then mixes it with a 455 kHz carrier. The product of this processing is a 455 kHz double sideband suppressed carrier USB or LSB IF signal at -20 dBm that is sent to Combiner Assembly A4 for filtering and amplification. The A5 assembly is equipped with two independent audio channels. One is used in USB and AM modes, the other is used in LSB and FM modes. Both are operational during ISB operation.

Both channels are equipped with automatic level control (ALC) to maintain proper audio path gain. Audio signals may be input via the front panel microphone at a nominal -56 dBm or any of the rear panel ports at levels between -26 and + 10 dBm. The 455 kHz USB and LSB IF signals can be gated through clipper networks to reduce the peak-to-average ratio and thereby increase the power output level. This feature is enabled by the CLIP switch on the front panel.

In the FM operating mode, the selected audio input is amplified by the A5 assembly and then sent to Carrier Generator Assembly A11. The carrier is modulated on the A11 assembly and sent back to A5. The modulated carrier is attenuated to -10 dBm and sent to the A4 assembly.

For CW and FSK, the audio processing circuits are not used. In these modes, the A5 assembly simply attenuates the 455 kHz carrier signal generated by the A11 assembly before it is passed to the A4 assembly.

The Audio Assembly is also equipped with a sidetone generator that can be monitored by the operator during CW transmissions.

A voice operated transmit (VOX) circuit on the A5 assembly can be used to key the radio in USB, AM, AFSK and 2ISB modes when a microphone is the source of the audio input. The VOX sensitivity and hangtime are adjusted on A5.

4.2.2 Combiner Assembly A4

Combiner Assembly A4 performs the following four main signal processing functions.

- Selects and filters the 455 kHz USB IF, 455 kHz LSB IF, or 455 kHz carrier.
- Combines USB IF and LSB IF signals for 2ISB operation. Also combines an external 455 kHz IF signal with the 2ISB signals to provide optional 4ISB operation.
- Reinserts carrier for AM signal or reduced carrier for USB and LSB signal.
- Uses an automatic level control (ALC) circuit to maintain a constant -20 dBm PEP 455 kHz IF output level.

Signal and filter selection is mode dependent. For sideband modes, filtering produces pure USB and LSB signals for broadcasting. In other modes, the filters narrow the bandwidth to reduce noise. The mode to filter relationship is summarized in table 4-1.

4.2.3 Converter Assembly A2

Converter Assembly A2 employs signal mixing and filtering to convert the filtered 455 kHz IF signal to an RF signal between 0.4 and 30 MHz. The filtered 455 kHz IF signal output by the A4 assembly is mixed with the 40 MHz LO 2 signal to produce a 40.455 MHz second IF signal. This signal is amplified and narrowband filtered before it is mixed with the variable LO 1 signal. The frequency of LO 1 is variable between 40.465 MHz and 70.455 MHz in 1 Hz steps and is 40.455 MHz above the selected transmit frequency. The mixer produces an RF signal between 0.4 and 30 MHz. The RF signal is filtered and amplified to produce an A2 assembly output signal with a nominal + 6 dBm PEP level.

4.2.4 Output Amplifier Assembly A1

Output Amplifier Assembly A1 can amplify the A2 output up to greater than + 20 dBm (100 mW) PEP, + 26 dBm (400 mW) maximum. The output of the A1 assembly normally drives the power amplifier in a transmitter system.

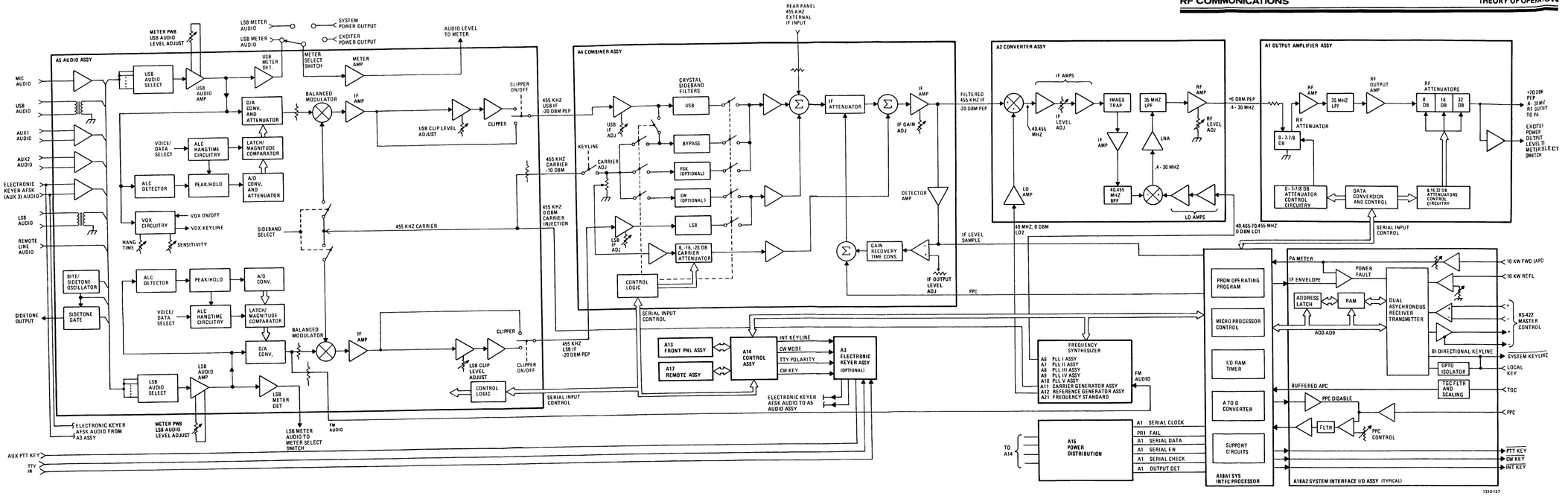


Figure 4-1. RF-1310 Signal Path Functional Block Diagram

Table 4-1. Combiner Assembly Filter Selection

Mode	Unfiltered 455 kHz First IF Source	Filter(s) Selected	Typical Filter Bandwidth
USB	Audio Assembly	USB	3.2 kHz, offset
LSB	Audio Assembly	LSB	3.2 kHz, offset
2ISB	Audio Assembly	USB and LSB	3.2 kHz (each filter), offset
AME	Audio Assembly	USB	3.2 kHz, offset
AM	Audio Assembly	Bypass	16 kHz, centered
FM	Carrier Generator Assembly	Bypass	16 kHz, centered
CW	Carrier Generator Assembly	CW	300 Hz, centered
FSK	Carrier Generator Assembly	FSK	3 kHz, centered

Two adjustable attenuators are built into the signal path on the A1 assembly. These provide up to 63-7/8 dB of attenuation in 1/8 dB steps. The attenuators can function as part of a RF ALC circuit that responds to feedback from the PA to maintain a constant transmitter output signal level. The attenuators also respond to the front panel RF POWER control to insert up to 50 dB attenuation in 1 dB steps into the RF signal path for operation at reduced output power levels. The RF signal can be diverted to an optional postselector before passing through the last attenuator stage.

4.2.5 System Interface Assembly A18

System Interface Assembly A18 monitors and supplies control signals going to and coming from the power amplifier. The A18 assembly is equipped with a microprocessor that allows it to monitor average and peak power controls (APC and PPC) produced by the PA. The average power control signal is applied to the attenuator networks on the A1 assembly to maintain a constant PA output level. The PPC is generated in response to a sudden rise in the PA output level and is applied to an attenuator network on the A4 assembly.

4.2.6 Gain Distribution

The normal gain or attenuation of each element along the signal path in the exciter is shown in figure 4-2.

4.3 FREQUENCY SYNTHESIZER

4.3.1 Introduction

This section describes the frequency synthesis scheme that is utilized to generate an RF output in the range of 400 kHz to 30 MHz with a 10-Hz resolution.

The main function of the frequency synthesizer is to provide a variable output frequency that functions as Local Oscillator (LO) 1 injection for the Converter A2 mixer. LO 1 has the following characteristics:

a. Tuning range of 40.465 MHz to 70.455 MHz.

b. Provides 10-Hz resolution over the 29,594,990 Hz tuning range.

c. Tunes in less than 20 milliseconds.

The Frequency Synthesizer consists of the following assemblies:

- PLL 1 Assembly A6
- PLL 2 Assembly A7
- PLL 3 Assembly A8
- PLL 4 Assembly A9
- PLL 5 Assembly A10
- Reference Generator Assembly A12
- Frequency Standard Assembly A21

Reference Generator Assembly A12 provides the 40.000000 MHz LO 2 injection for the A2 assembly's signal conversion of the 455 kHz first IF to a 40.455 MHz second IF.

Carrier Generator Assembly A11 is a frequency synthesizer covering a much smaller frequency range of 454 kHz to 456 kHz. The Carrier Generator Assembly generates the 455 kHz carrier, FM, and FSK signals.

Note that figure 4-3 shows a complete frequency synthesizer simplified block diagram and figure 4-4 shows how to compute the intermediate frequencies produced by the synthesizer assemblies for any given exciter output frequency. Other information which may be helpful (towards the end of this section) is the discussion of programmable divide-by-N phase locked loops and frequency resolution reduction techniques. All these assemblies are discussed in detail in their respective subsections.

4.3.2 Frequency Synthesizer Operation

The synthesizer generates LO 1 frequencies between 40.465000 MHz and 70.455000 MHz with a 1-Hz resolution.

The LO 1 signal is produced by combining the signals generated by the A7, A8, and A10 phase lock loop assemblies. The frequencies of the signals generated by these PLL assemblies are defined by specific groups of digits extracted from the transmit frequency. The frequency of the signal generated by A7 is defined by the three most significant digits (10^7, 10^6, and 10^5 places) of the transmit frequency. The frequency of the signal generated on A8 is defined by the digits in the 10^4 and 10^3 places of the transmit frequency. The frequency of the signal generated on A8 is defined by the three least significant digits (10^2, 10^1, and 10^0 places) of the transmit frequency. The least significant digit is not displayed and is always zero. Each of the three PLL assemblies employs a VCO and a programmable divide-by-N counter in a feedback loop to generate its signal.

The LO 1 frequency is determined on Control Board Assembly A14 and will always be 40.455 MHz above the transmit frequency. The digits of the desired transmit frequency (entered on the front panel frequency display) are divided into three groups. The three most significant bits are in one group, the digits in the 10^4 and 10^3 places are in the second group, and the three least significant digits are in the third group. A number, N, is derived for each group of digits. The values of N for the first, second, and third groups of digits are sent to the A7, A8, and A10 assemblies, respectively, on a serial data stream. The values of N are written into the programmable divide-by-N counters on the three PLL assemblies. The N values ultimately determine frequencies of the signals generated by the VCO on the A7, A8, and A10 assemblies. A change in the front

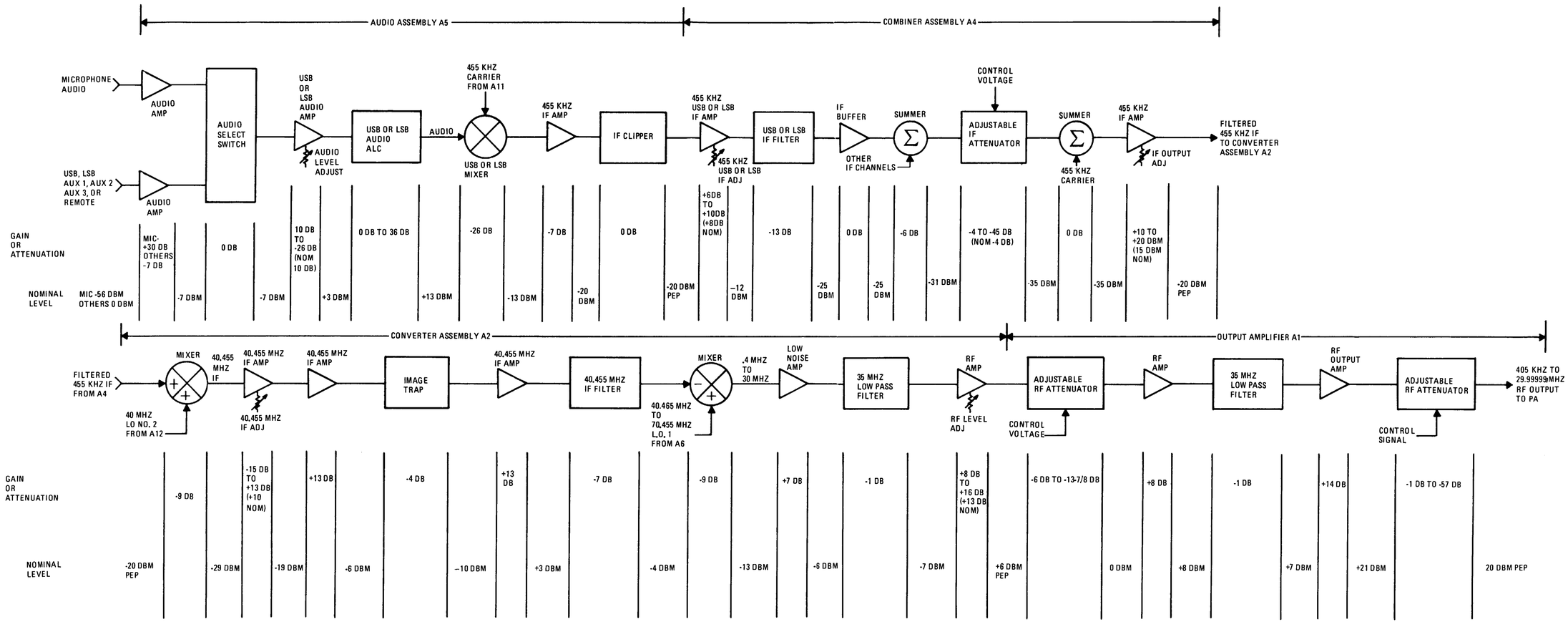
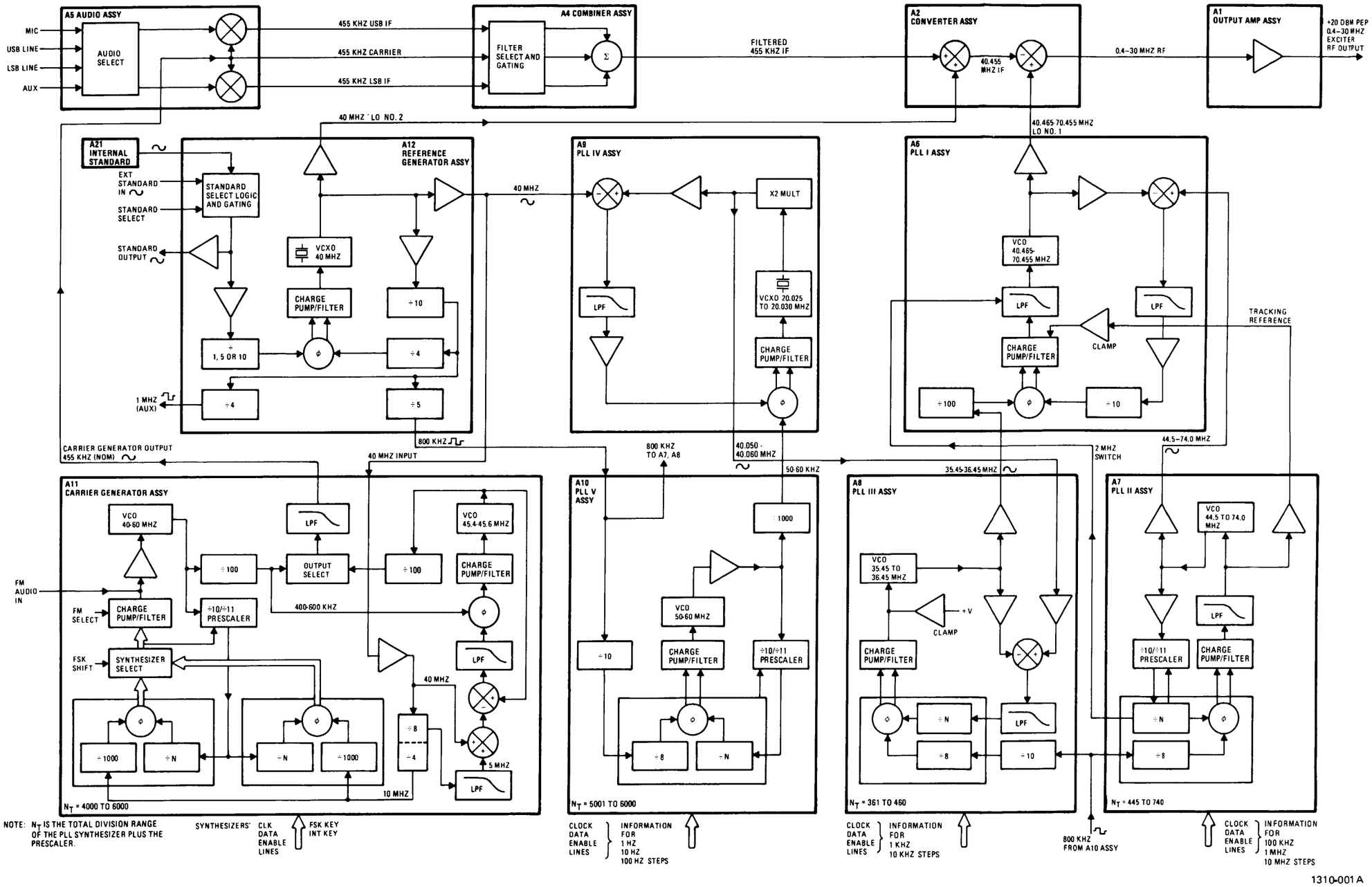


Figure 4-2. RF-1310 Signal Path Gain Distribution



1310-001 A

Figure 4-3. RF-1310 Frequency Synthesizer Functional Block Diagram

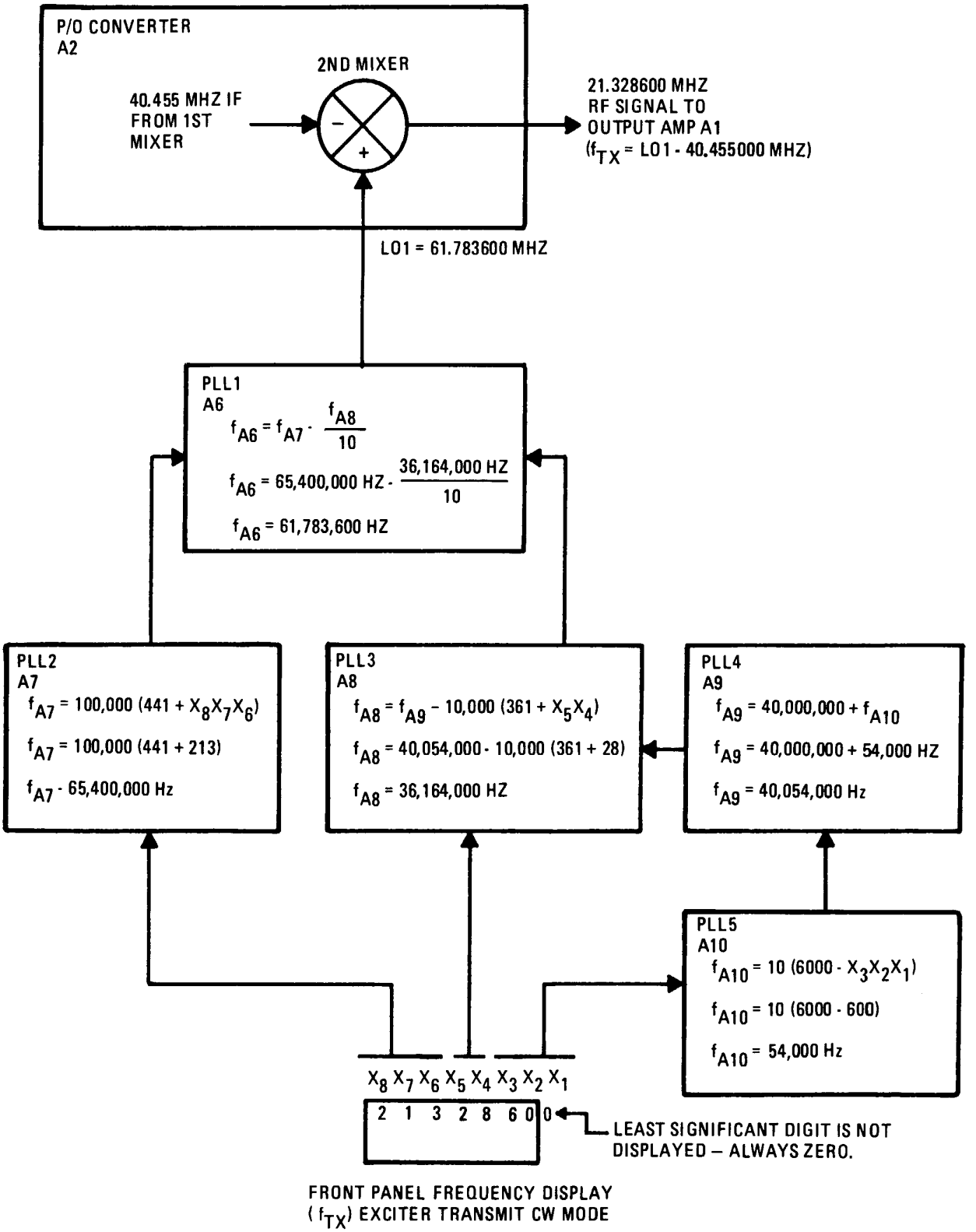


Figure 4-4. Frequency Synthesizer Tuning Example

panel frequency display will change the value of N and the VCO frequency for one or more of the PLL A7, A8, and A10 assemblies.

The outputs of the A7, A8, and A10 assemblies undergo further processing in the synthesizer chain before they are combined in the A6 assembly. The result of the combination of these three frequencies is a single frequency directly relating to the values of the exciter's displayed frequency. Furthermore, it is controllable to 1 Hz accuracy, and is used as the LO 1 injection for Converter Assembly A2 mixer U2 to tune the exciter. Note that although the synthesizer itself has 1 Hz accuracy, the actual transmit resolution is 10 Hz, since the 1 Hz tune increment is forced to zero and not displayed.

4.3.3 Reference Generator Assembly A12 and Frequency Standard Assembly A21

Frequency Standard Assembly A21 establishes the exciter's frequency stability and accuracy. The stability is 1 x 10^{-8} at either 1 MHz, 5 MHz, or 10 MHz. The frequency standard is used in a phase lock loop (PLL) on the A12 assembly to stabilize the 40 MHz voltage controlled crystal oscillator (VCXO). PLL references on all other assemblies are derived from this VCXO. The A12 assembly also provides 40 MHz LO 2 to the A2 assembly for signal path conversion of the 455 kHz IF to 40.455 MHz.

4.3.4 PLL 5 Assembly A10

The A10 assembly is a programmable divide-by-N PLL that provides the 1 Hz, 10 Hz, and 100 Hz tuning increments (the three least significant digits) in the LO 1 output signal. The A10 output is from 50 to 60 kHz in 10 Hz controllable steps. The output frequency is 10 (6000 - $X_3X_2X_1$) Hz, where $X_3X_2X_1$ are the three least significant digits of the transmit frequency. The least significant digit, X_1, is not displayed and is always zero.

4.3.5 PLL 4 Assembly A9

The A9 assembly is a translational type phase locked loop which converts the low frequency A10 output of 50 to 60 kHz in 10 Hz increments into 40.05 to 40.06 MHz in 10 Hz increments. The A9 assembly provides the intermediate signal processing required before the A10 output can be combined with the PLL 3, A8, 10 kHz, and 1 kHz tuning increments. The A9 output frequency may be computed from the formula 40,000,000 + 10 (6000 - $X_3X_2X_1$) Hz, where $X_3X_2X_1$ are the three least significant digits of the transmit frequency. The least significant digit is always zero.

4.3.6 PLL 3 Assembly A8

The A8 assembly is a programmable divide-by-N and translation PLL which performs the following two functions:

- Generation of the 10 kHz and 1 kHz tuning increments (10^4and10^3 places in the LO 1 frequency) for LO 1 output
- Combination of these increments with the 100 Hz, 10 Hz, and 1 Hz tuning increments provided by the A9 assembly

The A8 assembly output frequency can be determined by the following formula. Given that $X_3X_2X_1$ are the values of the three least significant digits of the transmit frequencies, and that X_5X_4 are the values of the 10^4 and 10^3 digits of the transmit frequency, A8 frequency = [40,000,000 + 10 (6000 - $X_3X_2X_1$)] - [10,000 (361 + X_5X_4)] Hz. The A8 output frequency range is 35.45 MHz to 36.45 MHz. X_1 is not displayed on the front panel and is always zero.

4.3.7 PLL 2 Assembly A7

The A7 assembly is a programmable divide-by-N PLL which provides the 10 MHz, 1 MHz, and 100 kHz tuning increments (three most significant digits) in the LO 1 output. The A7 assembly output is from 44.1 MHz to 74.0 MHz in 100-kHz controllable steps.

The A7 assembly output frequency is equal to 100,000 (441 + $X_8X_7X_6$), where $X_8X_7X_6$ is the value of the three most significant digits of the transmit frequency.

4.3.8 PLL 1 Assembly A6

The A6 assembly is a translation type PLL which combines the tuning increments for the LO1 output from assemblies A7, A8, A9, and A10. The output signal will be the LO 1 injection signal. It will be variable from 40.465 kHz to 70.455 MHz in 10 Hz controllable steps. Given a transmit frequency of $X_8X_7X_6X_5X_4X_3X_2X_1$ Hz where X_8 through X_2 are the digits from the front panel frequency display and X_1 is zero, the A6 assembly output and LO 1 frequency will be:

$$f_{A6} = f_{A7} - \frac{f_{A8}}{10}$$

where

$$f_{A7} = (441 + X_8X_7X_6)\ 100{,}000\ \text{Hz}$$

$$f_{A8} = [40{,}000{,}000 + 10\,(6000 - X_3X_2X_1)] - [10{,}000\,(361 + X_5X_4)]\ \text{Hz}$$

This signal will always be tuned exactly 40.455 MHz above the exciter transmit frequency.

4.3.9 Carrier Generator A11

The Carrier Generator Assembly A11has three main functions:

- Generation of a 455 kHz intermediate frequency carrier for CW mode, sideband carrier injection, or AM carrier reinsertion
- Direct narrowband (8 kHz deviation) FM modulation of 455 kHz carrier with audio from the A5 assembly
- Generation of FSK tones centered at 455 kHz with up to ± 1 kHz tone separation and 1 Hz resolution

The assembly receives control signals from the A14 assembly, a 40 MHz reference signal from the A12 assembly, and a FM audio input from A5. The nominal 455 kHz carrier generator output is sent to Audio Assembly A5. The assembly employs two interrelated phase locked loops and two VCOs to generate the carrier signals needed for the various modes of operation.

4.3.10 Frequency Synthesizer Tuning Example

The output frequencies of the A10, A9, A8, A7, and A6 assemblies at any given transmit frequency can be determined from the example shown in figure 4-4. Assume a transmit frequency f_o = 21,328,600 Hz and that $X_8X_7X_6X_5X_4X_3X_2X_1$ represent the values of the 10 MHz through 1 Hz positions. The exciter has a 10 Hz resolution so the X_1 digit is always zero and is not displayed on the front panel.

To calculate the frequency of the output signal from each assembly, start at the A10 assembly, then move on to the A9, A8, A7, and A6 in that order. The answer can always be checked since the following formula must always be true.

$$f_{LO\,1} = f_{TX} + 40.455\ MHz$$

Here,

$$f_{TX} = 21.328{,}600\ MHz$$

therefore,

$f_{LO\,1}$ = 21.328,600 MHz + 40.455 MHz
61.783,600 MHz (which agrees with the result of figure 4-4)

4.4 PHASE LOCK LOOP THEORY AND DBM TO V_{rms} CONVERSION

4.4.1 Conversion Between dBm and V_{rms}

Power levels in this manual are stated in dBm, or decibels with respect to 1 milliwatt. For example, + 6 dBm means 6 dB more than (above) 1 mW, or 4 mW. Similarly, -6 dB less than (below) 1 mW, or 0.25 mW (250 uW). Notice that every value of dBm corresponds to a particular amount of power. If the impedance in which this power is dissipated is known, the corresponding voltage and current can be determined. Table 4-2 lists 50 ohm voltage equivalents for many dBm power levels. Note that for negative values of dBm, voltages are read in either of the two left-hand columns. For positive values of dBm, voltages are read in the right-hand column. For example, -6 dBm is 0.112 V (112 mV), across 50 ohms, while + 6 dBm is 0.446 V. Similarly, -20 dBm equals 22.4 mV, while + 20 dBm equals 2.24 volts (across 50 ohms).

Table 4-2. Conversion of dBm to V_{rms} across 50 ohms (0 dBm = 1 mW)

(Negative dBm)		(Positive dBm)	
Volts	Millivolts	dBm	Volts
.224	224	0	.224
.199	199	1	.251
.178	178	2	.282
.158	158	3	.316
.141	141	4	.354
.126	126	5	.398
.112	112	6	.446
	99.9	7	.501
	89.0	8	.562
	79.3	9	.630
	70.7	10	.707
	63.0	11	.793
	56.2	12	.890
	50.1	13	.999
	44.6	14	1.12
	39.8	15	1.26
	35.4	16	1.41
	31.6	17	1.58
	28.2	18	1.78

Table 4-2. Conversion of dBm to V_{rms} across 50 ohms (0 dBm = 1 mW) (Cont.)

(Negative dBm)		(Positive dBm)	
Volts	Millivolts	dBm	Volts
	25.1	19	1.99
	22.4	20	2.24
	19.9	21	2.51
	17.8	22	2.82
	15.8	23	3.16
	14.1	24	3.54
	12.6	25	3.98
	12.0	25.41	4.17
	11.2	26	4.46
	10.0	27	5.01
	8.90	28	5.62
	7.93	29	6.30
	7.07	30	7.07
	3.98	35	12.6
	2.24	40	39.8
	0.707	50	70.7

4.4.2 Phase Locked Loops (PLL)

The basic phase locked loop (PLL) consists of the following four components:

- phase detector (or comparator)
- lowpass filter
- voltage controlled oscillator (VCO)
- divider (counter)

The counter component may be either a fixed or programmable divider.

4.4.2.1 Basic Phase Locked Loop

Figure 4-5 shows the four basic components of a phase locked loop. PLL operation involves comparing the frequency and phase of an incoming reference signal to the output of the voltage controlled oscillator (VCO). If the two signals differ in frequency and/or phase, an error voltage is generated by the phase detector and applied to the VCO. This causes the VCO output frequency to change in the direction required for decreasing the frequency/phase difference. The correction process continues until phase lock is achieved.

Dividing a VCO frequency output by two before applying it to the phase detector results in an error voltage that drives the VCO to twice the reference frequency. A divide-by-three action results in an error voltage that drives the VCO to three times the reference frequency. From this, the following relationship can be given, $f_{VCO} = N(f_{REF})$.

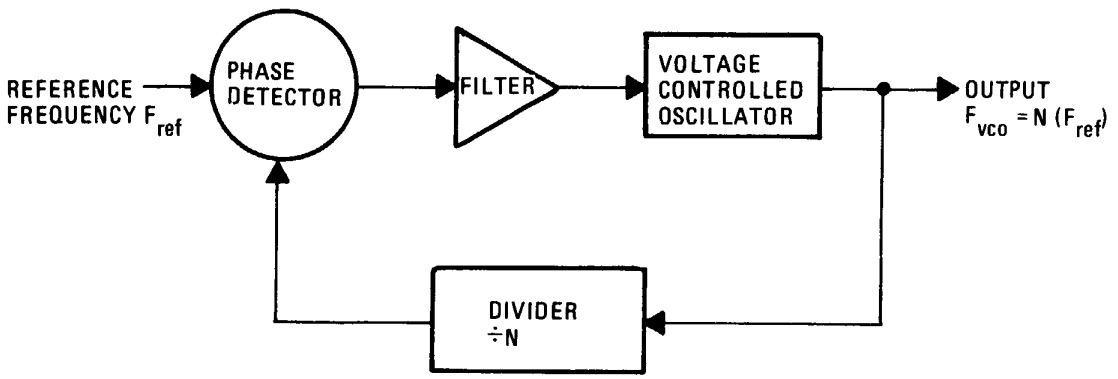


Figure 4-5. Basic Phase Locked Loop

4.4.2.2 PLL Programmable Counters

An example of the basic phase locked loop technique, using numbers, will provide an understanding of its actual operation. Referring to figure 4-6, the desired frequency is obtained by programming the variable divider through selectable inputs. Assuming the VCO is locked at the desired frequency of 1 MHz, this signal enters the input of the divide-by-100 counter (divider). The counter emits a pulse at its output each time 100 pulses enter its input. Therefore, dividing the 1 MHz input by 100 results in an output of 10 kHz. This 10 kHz signal is compared to the reference frequency of 10 kHz indicating a locked situation. If the divider's output had been less than 10 kHz, the phase detector would have produced an error voltage to drive the VCO to a higher frequency. Similarly, if the divider's output had been greater than 10 kHz, the VCO would have been driven to a lower frequency. Note that the phase lock loop output is dependent upon the selectable inputs of the variable divider. The RF-1310 provides this input to the divide-by-N counter in the form of a serial data command word. The coding of this word determines the divisor ratio of the counter, and is supplied (under microprocessor control) from the information supplied by the front panel frequency select controls.

4.4.2.3 PLL Prescaling Operation

A variation of the basic PLL which involves division of the feedback VCO signal prior to application to the divide-by-N counter is shown in figure 4-7. The total divider portion of the PLL now consists of two programmable counters and a two modulus prescaler.

The two modulus prescaler begins operation by dividing the VCO output by the higher of its two possible divisors, P + 1. The programmable divide-by-N counter counts the number of pulses from the prescaler. The swallow counter controls the number of times that the prescaler will be allowed to divide by P + 1 (to be precise, A times.) After the swallow counter reaches A counts, it instructs the prescaler to change its division ratio to P. (Note that the RF-1310 uses this scheme on the A7 and A10 assemblies, where the prescaler is a

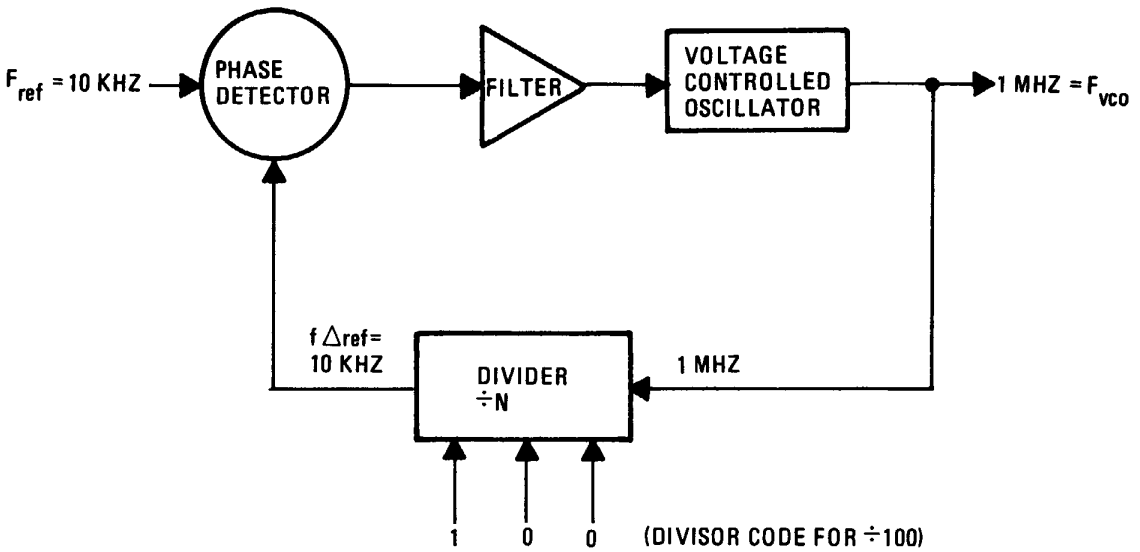


Figure 4-6. Programmable Phase Lock Loop

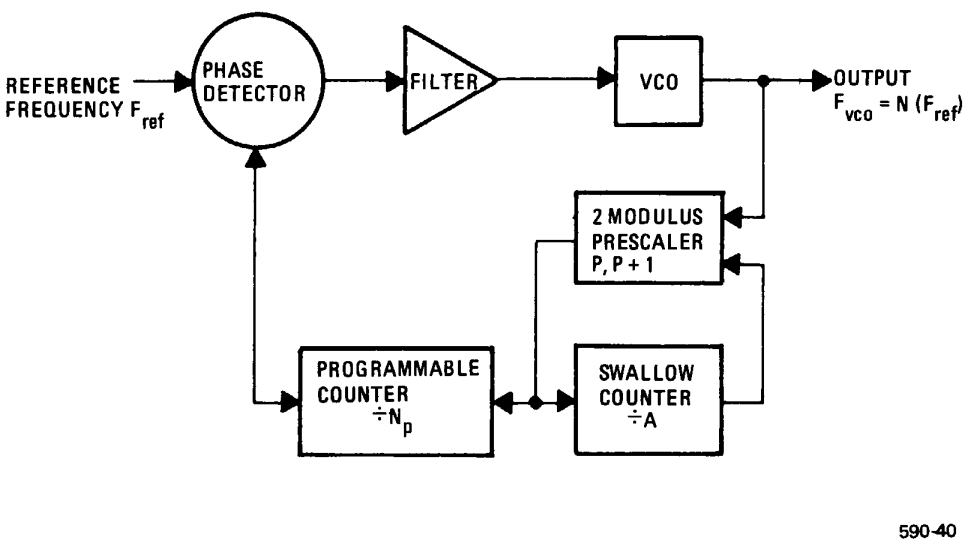


Figure 4-7. Phase Lock Loop Prescaling Technique

divide-by-10/divide-by-11 counter. The divide-by-N and swallow counter are counters internal to the PLL synthesizer IC.

In operation, the prescaler divides by P + 1, A times. For every P + 1 pulse from the prescaler, both the A counter and Np counter are decreased by 1. The prescaler divides by P + 1 until counter A reaches its zero state. At this point, the modulus of the prescaler changes to P. The prescaler then divides by P until the remaining count, (Np-A) in the Np counter, decreases to zero. At this time, the Np output emits a pulse while the A and Np counters reset. The cycle then repeats.

An example of the two modulus prescaling technique is given in figure 4-8 and table 4-3. For illustrative purposes, a VCO output of 50.7 MHz is derived.

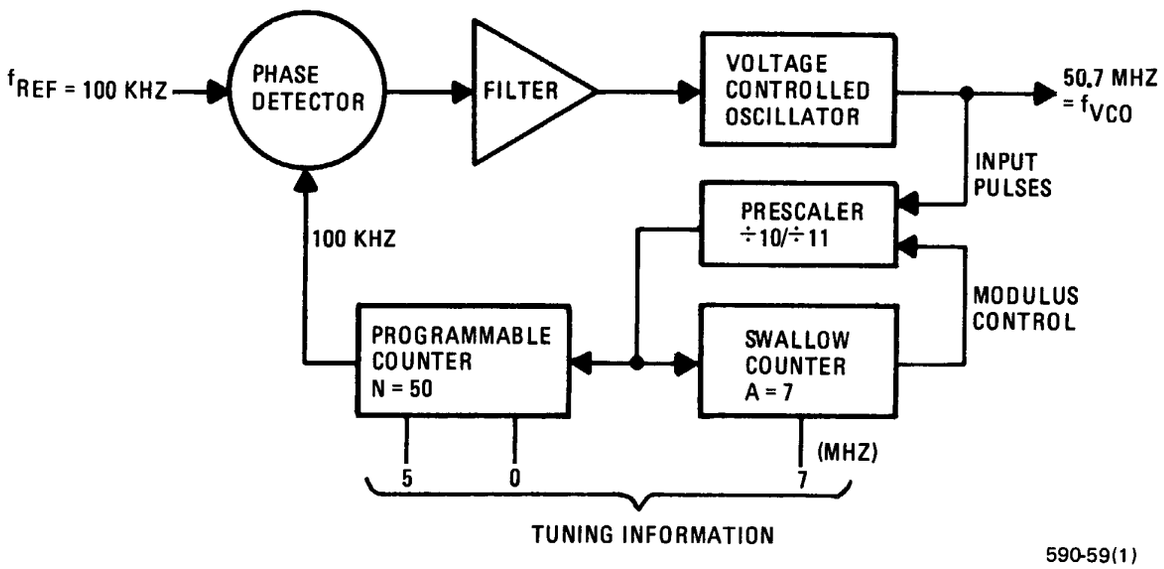


Figure 4-8. Prescaling Technique Example

Table 4-3. Prescaling Technique Example

Input Pulses	Prescaler Counts	Swallow Counter	Programmable Counter
0	0	7	50
11	11	6	49
22	11	5	48
33	11	4	47
44	11	3	46

Table 4-3. Prescaling Technique Example (Cont.)

Input Pulses	Prescaler Counts	Swallow Counter	Programmable Counter
55	11	2	45
66	11	1	44
77	11	0	43
87	10	0	42
97	10	0	41
107	10	0	40
477	10	0	3
487	10	0	2
497	10	0	1
507	10	0	0

507 input pulses = 1 output pulse

The two most significant digits, 5 and 0, are selected into the programmable counter. The least significant digit, 7, is selected into the swallow counter. Under locked conditions, the divider has an input (f_{VCO}) of 50.7 MHz, and an output of 100 kHz.

To produce a 100 kHz signal from the 50.7 MHz f_{VCO} signal, a divisor ratio of (50.7 divided by 100) or 507 is required. Table 4-3 shows a count sequence of 507 input pulses resulting in 1 output pulse. Similarly, a 50.7 MHz input results in a 100 kHz output.

The programmable divide-by-N counter emits a pulse every time it counts 50 input pulses. With the swallow counter set to seven, the prescaler divides by 11, seven times, and then switches to dividing by 10. At this point, the divide-by-N counter needs 43 input pulses before emitting an output pulse. The prescaler will now divide-by-10, 43 times, to finish the count sequence. With seven counts of 11 (7 x 11 = 77) and 43 counts of 10 (43 x 10 = 430), one pulse emits from the programmable counter every (77 + 430) or 507 input pulses.

4.4.3 Charge Pumps

The charge pump is the basic circuit employed in the RF-1310 to convert the PLL phase comparator complementary pulse output error signals into an analog dc VCO control voltage. The three basic components of a charge pump circuit are a current source, a current sink, and an output filter. Figure 4-9 shows a typical charge pump circuit.

4.4.3.1 Phase Detector Outputs

The phase detector compares the phase and/or frequency of two inputs (f_{VCO} and f_{REF}) and produces an output error signal at one of its two outputs ($\varnothing_V$ or $\varnothing_R$) whenever the inputs are not equal. The pulse widths of these output signals are directly proportional to the phase error of the two input signals.

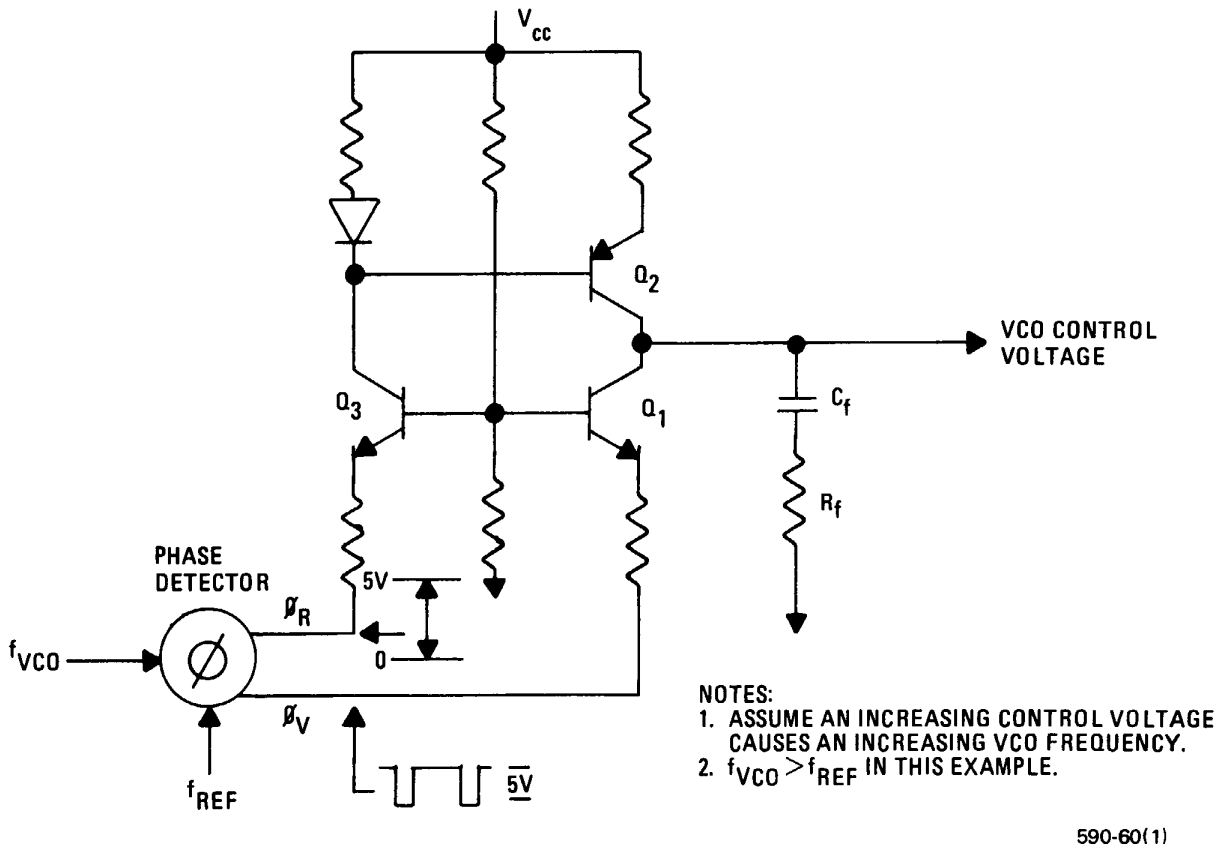


Figure 4-9. Basic Charge Pump Circuit

If the frequency f_{VCO} is greater than f_{REF} or if the phase of f_{VCO} is leading, then error information is provided by $\emptyset_V$ pulsing low. $\emptyset_R$ remains essentially high. (This is the situation shown in figure 4-9).

If the frequency f_{VCO} is less than f_{REF} or if the phase of f_{VCO} is lagging, then error information is provided by $\emptyset_R$ pulsing low. $\emptyset_V$ remains essentially high.

If the frequency of f_{VCO} = f_{REF} and both are in phase, then both $\emptyset_V$ and $\emptyset_R$ remain high, except for a short time period when both pulse low in phase. This time period is too short to affect the charge pump's lead-lag filter network C_f-R_f and is ignored.

4.4.3.2 Charge Pump Operation

The charge pump circuit functions as a current source/current sink network to lead-lag filter network C_f-R_f. Q2 and Q3 function as a current source to dump charge into the filter network, while Q1 functions as a current sink to pull charge out of the network. The net result is that the output voltage across the network rises when C_f charges and falls when C_f discharges.

Assume that f_{VCO} is greater than f_{REF} as shown in figure 4-9. Output $\varnothing_R$ remains high, holding Q3 off. Output $\varnothing_V$ pulses low, turning Q1 on. This provides a low impedance discharge path to ground for C_f. As C_f discharges, the charge pump output voltage (VCO control voltage) decreases, causing f_{VCO} to decrease.

Now assume that f_{VCO} is less than f_{REF}. $\varnothing_V$ remains high, holding Q1 off. $\varnothing_R$ pulses low, turning on Q3, and allowing Q2 to turn on and dump charge into C_f. This causes the VCO control voltage to increase, causing f_{VCO} to increase.

SECTION 5

MAINTENANCE

5.1 INTRODUCTION

This section contains general information concerning preventive and as-required maintenance of the RF-1310 Exciter. The solid state design has minimized regular maintenance. The built-in test feature has automated most troubleshooting. Procedures for testing individual assemblies are contained in the unit instruction subsections.

5.2 PREVENTIVE MAINTENANCE

The only item that requires regular maintenance is the exciter air filter. The filter should be removed and cleaned periodically at a frequency determined by the operating environment. The filter is located behind the grill on the lower part of the front panel.

To remove the filter:

a. Remove the two screws that secure the grill to the front panel.

b. Remove the grill.

c. Pull out the filter.

The filter can be washed with a diluted soap solution. Dry the filter completely before replacement.

CAUTION

Some of the assemblies in the RF-1310 contain static sensitive devices. To protect static sensitive devices from damage, follow the suggested precautions.

- Keep all static sensitive devices in their protective packaging until needed. This packaging is usually conductive and should provide adequate protection for the device. Storing or transporting static sensitive devices in conventional plastic containers could be destructive to the device.

- Disengage power prior to insertion or extraction of sensitive devices. This also applies to PWBs containing sensitive devices.

- Double check test equipment voltages and polarities prior to conducting any tests. Verify that no transients exist.

- Use only soldering irons and tools that are properly grounded. Ungrounded soldering tips will destroy these devices. SOLDERING GUNS MUST NEVER BE USED.

- Avoid contact with the leads of the device. The component should always be handled very carefully by the ends or the side opposite the leads.

- Avoid contact between PWB circuits or component leads and synthetic clothing while handling static sensitive devices or assemblies containing them.

5.3 BUILT-IN TEST EQUIPMENT (BITE) SELF-DIAGNOSTICS

The RF-1310 Exciter has the capability of extensive self testing in the event of a failure. The general types of tests and the assemblies affected are:

a. Control Circuits Tests

- Control Board Assembly A14
- Driver Board Assembly A13A2
- Display Board Assemblies A13A4 and A13A5
- System Interface Assembly A18
- Remote Control Assembly A17

b. Frequency Synthesizer Tests

- Reference Generator Assembly A12 and Frequency Standard Assembly A21
- Carrier Generator Assembly A11
- PLL 5 Assembly A10
- PLL 4 Assembly A9
- PLL 3 Assembly A8
- PLL 2 Assembly A7
- PLL 1 Assembly A6

c. Signal Path Tests

- Carrier Generator Assembly A11
- Audio Assembly A5
- Combiner Assembly A4
- Up/Down Converter A2
- Output Amplifier Assembly A1

d. Power Supply Tests

- Power Supply Assembly A15

Most of these tests can be automatically performed by turning the front panel selector switch to TEST. When the switch is in the TEST position, all exciter front panel controls become inoperative.

The normal length of the self test is approximately 8 seconds. All tests are performed sequentially in their order of importance.

If a fault exists in a particular assembly, that assembly number and the corresponding fault code (defining the type of failure) will be displayed on the exciter front panel alphanumeric display. See table 5-1 for a listing of the exciter assembly numbers and fault codes. For example, if the transmission of LSB signals became difficult (for unknown reasons), initiate the self test by rotating the selector switch to TEST. The display may indicate XA04 FLT 02. Where X is the prefix number of the exciter in the specific system it is installed. (See appropriate system manual.).

At the end of all assembly testing, a check will be made to see if the primary frequency standard has failed. If it has, the secondary standard will take over, and the front panel will display the message PRI FREQ STAN FAIL. If there is no secondary standard, BITE may have failed much earlier in the test.

If no faults were found during the self testing, the front panel will display---TEST PASSED---

NOTE

A fault indication may be displayed at initial turn on and will remain on until the frequency standard stabilizes.

When interpreting Built-In Test (BIT) fault indications, do not overlook the possibility that the fault condition at the indicated module may be caused by a failure or marginal condition in an associated module.

Table 5-1 RF-1310 Fault Code Listing (By Assembly Number)

Assembly No.	Fault Code	Description
A1	1	Output Amplifier Assembly Failure
A2	1	Up/Down Converter Failure
A3 (Optional)	1	AFSK Generator Level Fault
A4	1	Bypass Signal Path Fault
	2	LSB Filter
	3	USB Filter
	4	CW Filter
	5	FSK Filter
	6	-16 dB Insertion
	7	-26 dB Insertion
	8	PPC Failure
	9	AM Path Failure
	10	ISB Path Failure
A5	1	USB IF
	2	LSB IF
	3	USB ALC
	4	LSB ALC
	5	Serial Data

Table 5-1 RF-1310 Fault Code Listing (By Assembly Number) (Cont.)

Assembly No.	Fault Code	Description
A6	1	PLL 1 Out-Of-Lock
A7	1	Serial Data
	2	PLL 2 Out-Of-Lock
A8	1	Serial Data
	2	PLL 3 Out-Of-Lock
A9	1	PLL 4 Out-Of-Lock
A10	1	Serial Data
	2	PLL 5 Out-Of-Lock
A11	1	Carrier Generator 1 Serial Data
	2	Carrier Generator 2 Serial Data
	3	Carrier Generator 1 Out-Of-Lock
	4	Carrier Generator 2 Out-Of-Lock
	5	45 MHz Out-Of-Lock
	6	Carrier Generator Output Fail
	7	FM Mode Select
A12	1	1 MHz Reference
	2	800 kHz Reference
	3	40 MHz PLL Out-Of-Lock
	4	Primary Standard Fail This error code reported back to remote only.
A13		No Fault Codes (Converter Module)
A14	1	PROM Checksum Failure
	2	Parallel/Serial Conversions
	3	CMOS RAM Failure
	4	Serial Data Input
	5	Keyline Logic Failure
	6	8255 Output Port Failure
	7	A/D Timing Failure
	8	A/D + 5 Reference Failure
	9	A/D Ground Failure
	10	CW Key/AFSK Keyer Control Failure (Optional)
A15		No Fault Codes (Linear Power Supply)
A17	1	LCU PROM
	2	LCU Communication
	3	LCU Interface
	4	Remote FSK Modem Data Loopback Failure (Optional)
A18	1	Serial Communications
	2	ROM Failure
	3	RAM Failure
	4	I/O Failure

Table 5-1 RF-1310 Fault Code Listing (By Assembly Number) (Cont.)

Assembly No.	Fault Code	Description
A18 (Cont.)	5	Output Amp Communication
	6	A-to-D EOC Failure
	7	A-to-D Conversion Error
A22 (Optional)	1	LLSB Failure
	2	UUSB Failure
	3	4ISB (LLSB & UUSB) Failure

5.3.1 Continuous Self-Test Monitoring

Certain critical circuits which may adversely affect exciter operation or cause physical damage if they malfunction are continuously monitored. These circuits are:

a. Power Supply Assembly A15. All power lines distributed to the exciter are continuously monitored for acceptable voltage limits.

b. All Synthesizer Phase Lock Loop (PLL) Assemblies (A6, A7, A8, A9, and A10). These PLLs are continually monitored for a locked condition, indicating a stable transmitting frequency.

c. PA Readback lines, when provided, in the Interfacing System.

Failure of the A6, A7, A8, A9, A10, or A15 assemblies will cause the front panel FAULT LED to light any time the exciter is on. Additionally for faults on assemblies A6 through A10, a **SYNTHESIZER FAULT** message will appear on the display.

5.3.2 Self-Test Operation

The RF-1310 self-test procedure, performed in test mode, consists of a series of tests and measurements that verify the proper operation of the exciter. These tests are performed sequentially. If a failure is encountered, the test will stop at that failure. The test will only continue past that failure by removing the cause of that failure.

NOTE

If one failure is found, there may be other failures that will not be indicated until the first failure is corrected.

The self-test procedure is performed in three stages. First, tests involving digital levels (logic 1 and 0) are performed in order of their importance. Next, the exciter signal path is tested for performance. The first part of this performance test is accomplished using the BITE oscillator on the A5 assembly, and the second part is accomplished using the operating frequency that the exciter was last tuned to before entering BITE.

The tests performed during BITE are described in the following paragraphs. It may be necessary to refer to the specific circuit schematics under discussion. These schematics are in the assembly subsections.

5.3.2.1 Lamp Test

The first test performed is the lamp test. All LEDs and segments of the 10-and 20-character displays located on the front panel are lit. This condition is maintained for approximately 4 seconds and allows the operator to examine all front panel indicators while the remainder of the exciter testing is being accomplished.

5.3.2.2 ROM Test (A14 Assembly)

The Control Board Assembly A14 ROM test is performed next. U19 and U20 contain all the firmware used to control the main exciter functions and are tested to determine that the information they contain is correct. If any of these are found to have a problem, the corresponding fault message will be displayed on the front panel. These devices are factory programmed.

5.3.2.3 RAM Test (A14 Assembly)

The next test performed is the RAM test. This test will determine the read/write capability of the 8K CMOS RAM U18 located on Control Board Assembly A14. If a fault exists, the appropriate fault code will be displayed on the front panel.

5.3.2.4 Output Port Test (A14 Assembly)

On Control Board Assembly A14, U13 is tested for its ability to read and write, to and from its individual ports which control many functions in the exciter. Any error will cause the appropriate fault code to be displayed on the front panel.

5.3.2.5 Serial/Parallel Test (A14 Assembly)

This test determines the ability of Control Board Assembly A14 to read in the parallel lines and convert them to serial data. U6, U10, U15, U25, multiplexer U11, and the serial clock circuitry are tested. Any error will cause the appropriate fault code to be displayed on the front panel.

5.3.2.6 A-to-D Converter Test (A14 Assembly)

A-to-D converter U21 on the A14 assembly is tested for its ability to make analog-to-digital conversions properly and within acceptable time limits. Any error will cause the appropriate fault code to be displayed on the front panel.

5.3.2.7 Keyline Tests (A14 Assembly)

The circuitry involved in reading and activating the exciter keylines is tested next. In order for this test to actually verify keyline performance, either of the auxiliary keylines or the VOX keyline must be activated and held before entering BITE. If they are not, this test will simply be passed over and the rest of BITE will continue. The affected ICs are U1, U2, and U3. Any error will cause the appropriate fault code to be displayed on the front panel.

NOTE

If the CW and PTT keylines are both keyed, BITE will display **XA14 FLT 05**, Keyline Logic Failure.

5.3.2.8 Serial Data Tests (A14 Assembly)

The operation of the parallel-in/serial-out shift register U17 on Control Board Assembly A14 and the capability of all synthesizers (including the Carrier Generator) to accept serial data from the control board is now tested. If a synthesizer fails to receive data correctly, then that assembly is identified as having failed. If there is a problem with all the synthesizers reading correctly, then it is assumed that the Control Board is at fault.

The synthesizer PLLs are first loaded with all zeros and tested. They are then loaded with 00000000 00000000 00100000 binary. The one (1) bit will set the serial check lines on the PLL's to 1. This bit is then read back and tested for all PLLs. If the bit has not been set to 1, a fault has occurred, and the appropriate fault code is displayed on the front panel.

5.3.2.9 System Interface Tests (A18 Assembly)

At this point, System Interface Assembly A18 begins its own self test. If there is an error in properly receiving this start message, a communications error is generated and displayed on the front panel. If everything is received properly, the A18 BITE will run on its own and main BITE will continue. Later in the main BITE, results from the system interface test are received and interpreted.

5.3.2.10 Audio Serial Tests (A5 Assembly)

Audio Assembly A5 is tested separately for its ability to accept serial data from the control board. A check bit on A5, U26, is tested to see if it can be accurately controlled. If any problem is encountered, the appropriate fault code is displayed on the front panel.

5.3.2.11 Reference Generator Test (A12 Assembly)

Reference Generator Assembly A12 is tested next. The 40-MHz lock bit is read and tested for a locked condition (logic 0 = lock). If detected as being out of lock, the appropriate fault code and assembly number are displayed on the front panel.

The 1-MHz and 800-kHz detect lines are read, and if a logic 1 is read indicating a fault, the appropriate fault code and assembly number are displayed on the front panel.

5.3.2.12 Phase Locked Loop (PLL) Tests

PLL 5, PLL 4, PLL 3, PLL 2, PLL 1, and Carrier Generator PLLs CG I and CG II are now tested to ensure that they can be tuned over their entire range. For the synthesizer PLLs, the testing is done in three frequency ranges as listed in table 5-2.

Table 5-2. PLL Frequency Range

PLL Range	Exciter Frequency
LOW	00,000.000 kHz
MID	15,050.500 kHz
HIGH	29,999.999 kHz

Carrier Generator Assembly A11 PLLs CG I and CG II are also tested in three frequency ranges. Those ranges are listed in table 5-3.

Table 5-3. A11 Assembly Frequency Range

PLL Range	Carrier Generator Frequency
LOW	454.000 kHz
MID	455.117 kHz
HIGH	456.000 kHz

At each frequency, all PLLs are tested to determine the status of their respective lock lines. They are tested in order, starting with PLL 5 and finishing with CG II. If a fault occurs, the appropriate fault code and assembly number are displayed on the front panel.

5.3.2.13 System Interface Assembly Tests (A18 Assembly)

At this point, the results of the System Interface Assembly BITE tests are interpreted. Tested on the A18 assembly are:

- Serial communications U6 and PROM U8
- RAM contained in U9
- I/O ports of A18A2 Assembly
- Communications to Output Amp Assembly A1-U9 and associated circuitry
- A-to-D converter U11.

If any errors are found, the appropriate fault code will be displayed on the front panel.

5.3.2.14 Carrier Generator Test (A11 Assembly)

Next, Carrier Generator Assembly A11 will be tested for its ability to generate the appropriate carrier signal. It will be tested to verify its ability to generate a signal at 455 kHz and 454.55 kHz (the FM loop). If any error in generating these signals is found, the appropriate fault code is displayed on the front panel.

5.3.2.15 Audio Assembly Test (A5 Assembly)

Proper selection of signal paths are verified. The USB and LSB audio and both IF paths are tested for the ability to pass signals. The operation of the ALC on both audio paths are also tested by applying two different audio input signal levels. The test signals are supplied by the BITE oscillator.

If any error is found, the appropriate error code is displayed.

The output detect on each of the IF paths is checked. They are verified for the proper output and control. Any discrepancies result in a fault code.

5.3.2.16 Combiner Assembly Tests (A4 Assembly)

The Combiner Assembly test includes the control and passing of signals through each one of the filters and the ISB leveling loop.

First, the ability for a signal (the BITE oscillator from the previous audio tests) to be passed through both the USB and LSB filters is checked. If this is determined to be functional, then one of the filters is deselected and the output of the combiner tested to determine if the level is up to full output, indicating proper operation of the ISB leveling loop. An error in any of these steps generates the appropriate fault code on the front panel. At this point, the BITE oscillator on the A5 assembly is no longer needed, so it is disabled for the remainder of the exciter self test.

Next, the three filter paths CW, FSK, and BYPASS are tested for control and passage of the 455-kHz Carrier Generator signal. If any of the filters has a problem, that filter's fault code is displayed on the front panel.

Finally, the AM filter path and the two carrier insertion levels are tested. The AM filter is only selected and tested for its ability to pass a signal. Alternately, each carrier level is selected and the output verified for much lower levels. Any failures are displayed on the front panel.

5.3.2.17 Electronic (AFSK) Keyer Test (A3 Assembly - Optional)

After completion of the Audio Assembly Test, the audio assembly output is again evaluated using the A3 assembly (if installed) as the audio source. This verifies proper operation of the AFSK signal generation circuits. In addition, if the keyer is installed, the keyline control circuitry on the A14 Assembly is also tested.

5.3.2.18 Up/Down Converter Tests (A2 Assembly)

At this point, the exciter is tuned to the frequency which was selected on the front panel when BITE was initiated and remain there for the remainder of all tests. The up/down converter is checked for proper output as well as internal keyline response, and any problems will cause the appropriate fault code to be displayed on the front panel.

5.3.2.19 Output Amp Test (A1 Assembly)

The Output Amp Assembly test includes an output level check and the control and response of the three digital attenuators.

Initially, all three digital attenuators are switched out to remove all attenuation. This will obtain full RF output. The output level is then read and stored. Each attenuator is switched in separately and the output power is monitored and compared to the full output reading. This determines if the amount of attenuation is correct.

5.3.2.20 Frequency Standard Detect

If all exciter tests have passed to this point, then the PRI FAIL line originating from Reference Generator Assembly A12 is tested. If this line indicates the primary frequency standard has failed (fail = 1), then the message PRI FREQ STAN FAIL is displayed on the front panel. No fault code or assembly number will appear. As was stated earlier, this means that the primary frequency standard has failed and the exciter is operating on its secondary standard. If no secondary standard exists, the exciter may have failed BITE much earlier in the PLL tests.

5.3.2.21 Remote Control Assembly (LCU) Tests

The next test is on Remote Control Assembly A17. The information used to control these tests is contained within the Remote Control Assembly firmware. Once it is determined that the Remote assembly is installed, then the Remote assembly tests its DUART, PROM, and the RS-232 interface circuitry. If any of these are found

to be at fault, the corresponding fault code is displayed on the front panel. The LCU also reports any self-test pass/fail conditions that may occur as a result of running BITE to the remote site.

If the optional A17A2 Remote FSK Modem assembly is installed in the exciter the self-test routine will also perform a test on this modem. The test consists of: putting the modem in the internal loopback mode, sending it data from the Control Board (A14), and finally verifying the data looped back to the Control Board. If the data is incorrect a fault code is displayed on the front panel.

5.3.2.22 4ISB Adapter Tests (A22 Assembly - Optional)

The 4ISB Adapter option (RF-1314), if installed in the transmitter system, is tested by its internal BITE routine only after all RF-1310 tests have passed. Refer to the RF-1314 supplement (issued with the option) for details of the tests performed. If any of the tests fail, the proper fault code is displayed on the RF-1310 front panel as an A22 Assembly fault.

5.4 SELF-TEST SEQUENCE SUMMARY

The RF-1310 self tests are done in the order of assembly importance. If a fault is discovered during testing, this failure must be corrected before the remaining tests are attempted.

Table 5-4 lists the order of testing from the first to the last test.

Table 5-4. Self-Test Sequence Summary

Sequence	Summary
1.	ROM Test - Assembly A14
2.	RAM Test - Assembly A14
3.	Output Port Test - Assembly A14
4.	Parallel/Serial Conversions - Assembly A14
5.	A-to-D Converter Test - Assembly A14
6.	Keyline Tests - Assembly A14
7. 7.1 7.2 7.3 7.4 7.5	Serial Data Tests Assembly A14 Assembly A11 Assembly A7 Assembly A10 Assembly A8
8. 8.1	System Interface - Assembly A18 BITE Start-Communications Error
9.	Audio Serial Test - Assembly A5
10. 10.1 10.2 10.3	Reference Generator Tests - Assembly A12 1 MHz Reference 800 kHz Reference 40 MHz Phase-Locked-Loop

Table 5-4. Self-Test Sequence Summary (Cont.)

Sequence	Summary
11.	Phase Locked Loops
11.1	Assembly A10 - PLL V
11.2	Assembly A9 - PLL IV
11.3	Assembly A8 - PLL III
11.4	Assembly A7 - PLL II
11.5	Assembly A6 - PLL I
11.6	Assembly A11
11.6.1	CG I
11.6.2	CG II
11.6.3	45 MHz Out Of Lock
12.	System Interface Tests - Assembly A18
12.1	Serial Communication - A14
12.2	ROM
12.3	RAM
12.4	I/O Read/Write
12.5	Output Amp Communication
12.6	A-to-D Level Conversions
13.	Carrier Generator Test - Assembly A11
13.1	CG Output
13.2	FM Select
14.	Audio Tests - Assembly A5
14.1	USB ALC
14.2	LSB ALC
14.3	USB IF
14.4	LSB IF
15.	Combiner Tests - Assembly A4
15.1	ISB Path
15.2	LSB Filter
15.3	USB Filter
15.4	CW Filter
15.5	FSK Filter
15.6	Bypass Path
15.7	AM Filter
15.8	16 Carrier Insertion
15.9	26 Carrier Insertion
16.	AFSK Keyer Test - A3 Assembly (Optional)
17.	Up/Down Converter Detector Test - Assembly A2
18.	Output Amp Tests - Assembly A1
18.1	Control
18.2	32 dB Attenuator
18.3	16 dB Attenuator
18.4	8 dB Attenuator

Table 5-4. Self-Test Sequence Summary (Cont.)

Sequence	Summary
19.	Primary Fail Detect Test
20.	Remote Control Tests - Assembly A17
20.1	PROM Test
20.2	Communications Test
20.3	Interface Test
20.4	Remote Modem Loopback Test (Optional)
21.	4ISB Adapter Tests - Assembly A22 (Optional)
21.1	LLSB Test
21.2	UUSB Test
21.3	4ISB (LLSB & UUSB) Test

5.5 EXCITER CHECKOUT

The following paragraphs verify that the exciter is functional. At this point, the operator should read and understand the Operation section of this manual.

5.5.1 Exciter Output Power and Frequency Validation

a. With ac power disconnected, remove exciter top and bottom covers.

b. Lower the front panel by loosening the four captive screws behind the front panel handles, and pivoting the front panel down.

c. Check that the Control Assembly A14 backup battery jumper is properly installed between terminals E1 and E2.

d. Reinstall the front panel.

e. Configure the exciter as described in the Installation section, paragraph 2.4, Power Requirements. Connect the exciter line cord to the appropriate ac power source. Allow the frequency standard to stabilize for about 15 minutes before proceeding.

f. Check that the EXT CW KEY is open. Place the front panel rotary function switch to the NORM position. The exciter is now on and conducting a turn-on self test. The test will run for about 1 second, during which time all displays (alphanumeric VFDs and green LEDs) should turn on. If all self-tests pass, then the exciter displays reset to indicate the settings that existed the last time the exciter was on. If any tests fail, a fault code is displayed in the left side alphanumeric display. The operator should then proceed to the BITE information in the Maintenance section of this manual, and locate the indicated fault code listed in the fault code table. Any fault should be repaired before proceeding.

g. Connect the test equipment as shown in figure 5-1.

h. Place System Interface Assembly A18A1 switch S1-4 open. This places the exciter in a signal generator mode.

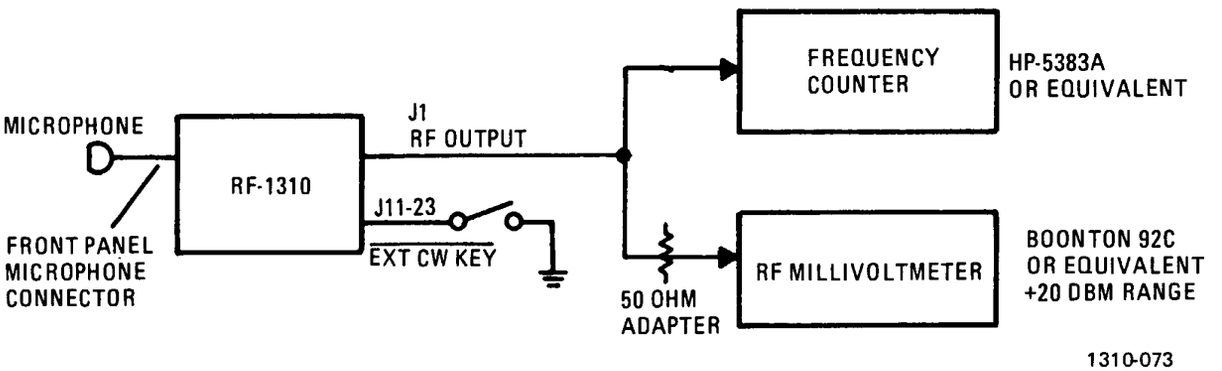


Figure 5-1. RF Output Validation

i. Press STANDBY and OPERATE buttons. OPERATE, READY, and FREQUENCY LEDs will turn on.

j. Press 0, 2, 0, 0, 0, 0, and 0 at keyboard. Press ENTER button.

k. Press the MODE button, and scroll the display to CW.

l. Press the POWER button. Using the keypad, press 0 twice. Press ENTER button. Power display will read -00, LED will be on.

m. Close the EXT CW KEY at J11-23. RF output power should appear at J1, nominally + 20 dBm, at the front panel displayed frequency (02,000.00 kHz).

n. Press the meter EXC RF switch. The front panel meter should indicate 100 mW (nominally).

o. Open the EXT CW KEY. Enter a new frequency by pressing the appropriate keypad numerals. Press ENTER. Close EXT CW KEY. The new output frequency should agree with the displayed front panel frequency. Open the EXT CW KEY.

p. The ability of the exciter to properly tune and output full power has now been verified. If a further check of other capabilities is desired, proceed.

5.5.2 Channel Programming Validation

Perform Installation section, paragraph 2.6 before proceeding. The following verifies the ability of the exciter to program channels.

5.5.2.1 Programming the First Channel

a. Select PROG position of rotary function switch.

b. Press 0 and 1 at the keyboard. Press ENTER button.

c. Press FREQUENCY button, press 1, 0, 0, 0, 0, 0, and 0 at the keyboard. Press ENTER button.

d. Press MODE button until FSK mode is scrolled.

e. Press RF POWER button. Press 1 and 0 at the keyboard, and then press ENTER button.

f. Press LOAD button.

5.5.2.2 Programming the Second Channel

a. Press CHANNEL button. Press 0 and 2 at keyboard. Press ENTER button.

b. Press FREQUENCY button. Press 2, 0, 0, 0, 0, 0, and 0 at keyboard. Press ENTER button.

c. Press MODE button until USB mode is scrolled.

d. Press CARRIER button until -10 or -16 is scrolled.

e. Press AUDIO button until MIC is scrolled.

f. Press RF POWER button. Press 0 and 5 at keyboard. Press ENTER button.

g. Press CLIP button to cause LED above button to turn on.

h. Press LOAD button to load channel information. The second channel has now been programmed.

5.5.2.3 Recalling Channels

a. Place rotary function switch to NORM position. Display should revert to values entered before channel programming validation began.

b. Press CHANNEL button. Press 0 and 1 at keyboard. Press ENTER button. Front panel displays should indicate:

Mode	Carrier	Audio	RF Power	Frequency	Channel
FSK	blank	blank	-10	10,000.00	01

The CHANNEL LED should be on.

c. Press 0 and 2 at keyboard. Press ENTER button. Front panel displays should register:

Mode	Carrier	Audio	RF Power	Frequency	Channel
USB	-10 or -16	MIC	-05	20,000.00	02

The CHANNEL and CLIP LEDs should be on.

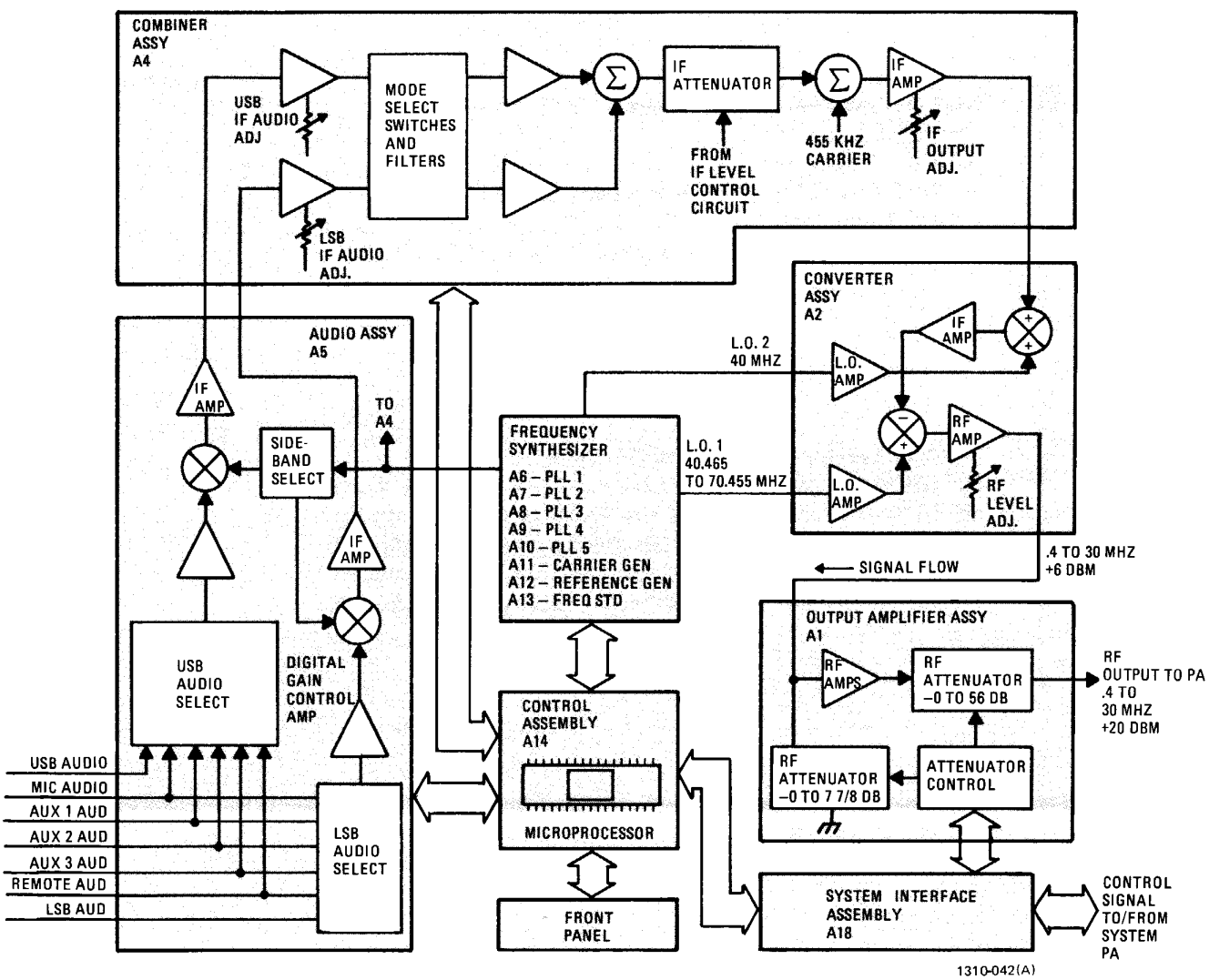
d. Programming validation has now been completed.

5.5.2.4 Full Self Test

a. To run a more comprehensive self test than exists during the power on self test, place the rotary function switch to TEST position. All displays light during self test. If no failures exist at the end of the self test (approximately 8 seconds), the displays read - - - TEST PASSED - - -. If a failure does occur, a fault code appears in the left hand display. If a fault code appears, refer to the BITE information in the Maintenance section of this manual.

b. Set rotary switch to OFF position. Set A18A1 switch S1-4 to closed position (NORM). Replace top and bottom exciter covers. All initial turn on tests are now complete.

MAJOR ASSEMBLY LOCATION AND INTERCONNECTION



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MAJOR ASSEMBLY LOCATION AND INTERCONNECTION

1. MAIN CHASSIS

The RF-1310 chassis is a rigid, one piece casting, containing compartments which house most printed wiring board assemblies. The Front Panel Assembly A13 and Power Supply Assembly A15 mount on the front and rear portions of the chassis, respectively. External top and bottom covers mount to the front Z bracket and the rear panel (part of A15 assembly).

1.1 Top Side of Chassis

The top side of the chassis is shown in figure 1 and contains the following assemblies:

- Converter Assembly A2
- Combiner Assembly A4
- Audio Assembly A5
- Power Supply Assembly A15
- Remote Control Assembly A17
- System Interface Assembly A18
- Rear Panel Filter Assembly A20
- Frequency Standard Assembly A21
- + 24 Volt Power Supply Assembly A23

Remote Control Assembly A17, sits over Audio Assembly A5 in a hinged pan that pivots out for access to A5.

1.2 Underside of Chassis

The underside of the chassis is shown in figure 2 and contains the following assemblies:

- Output Amplifier Assembly A1
- PLL 1 Assembly A6
- PLL 2 Assembly A7
- PLL 3 Assembly A8
- PLL 4 Assembly A9
- PLL 5 Assembly A10
- Fan Assembly B1 (mounted to bottom cover; not shown in figure 2)

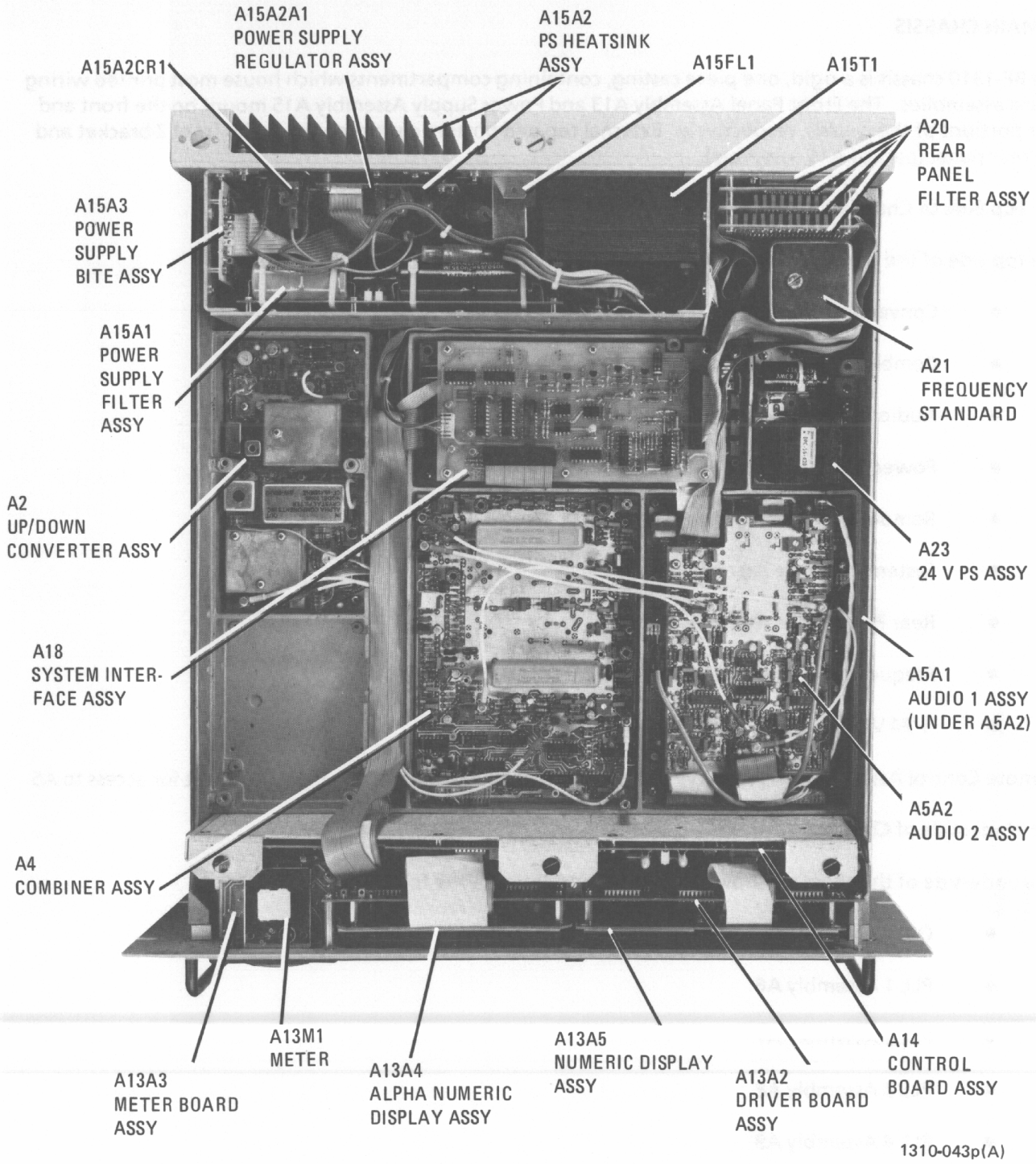


Figure 1. RF-1310 Top View Without Covers (Remote Control Assembly Removed)

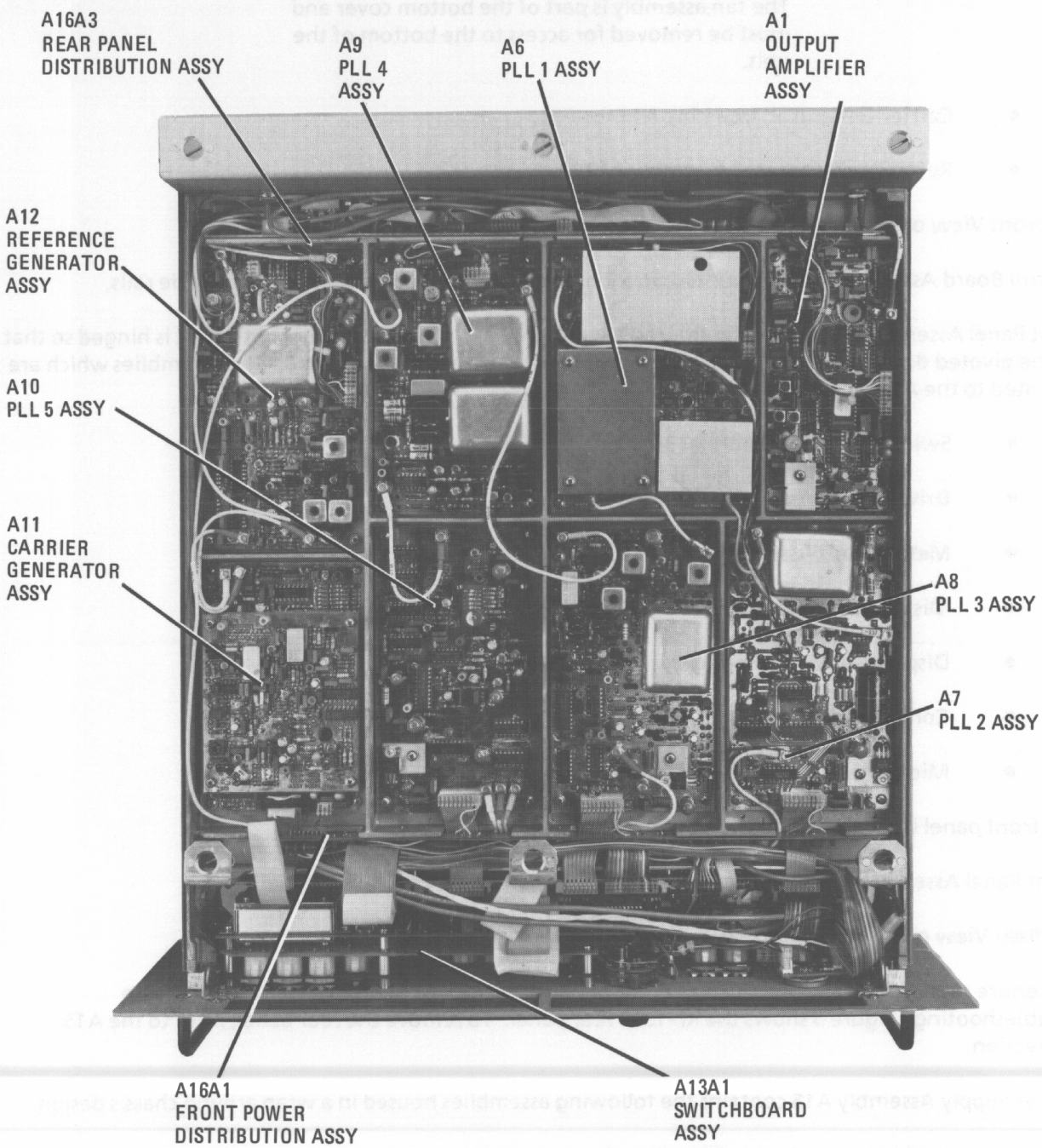


Figure 2. RF-1310 Bottom View

NOTE

The fan assembly is part of the bottom cover and must be removed for access to the bottom of the unit.

- Carrier Generator Assembly A11
- Reference Generator Assembly A12

1.3 Front View of Chassis

Control Board Assembly A14 is mounted on a Z bracket that is securely fastened to the side rails.

Front Panel Assembly A13, shown in figures 3 and 4, contains all the operator controls. It is hinged so that it can be pivoted down for easy access to the assemblies which are mounted to it. The assemblies which are mounted to the A13 assembly are:

- Switch Board Assembly A13A1
- Driver Board Assembly A13A2
- Meter Board Assembly A13A3
- Display Board (alphanumeric) Assembly A13A4
- Display Board (numeric) Assembly A13A5
- Converter Assembly A13A6
- Microphone Assembly A13A7

The front panel is securely fastened to the main chassis by four captive screws.

Front Panel Assembly A13 details may be found in subsection A13 of this manual.

1.4 Rear View of Main Chassis

The entire rear panel including the power supply can be removed as one assembly to facilitate troubleshooting. Figure 5 shows the RF-1310 rear panel. To remove the rear panel, refer to the A15 subsection.

Power Supply Assembly A15 contains the following assemblies housed in a wrap around chassis design.

- A15A1 Power Supply Filter Board
- A15A2 Power Supply Regulator Heatsink Assembly, with Regulator Board A15A2A1
- A15A3 Power Supply BITE Board
- Ac line transformer, line filter, fuse holder, etc.

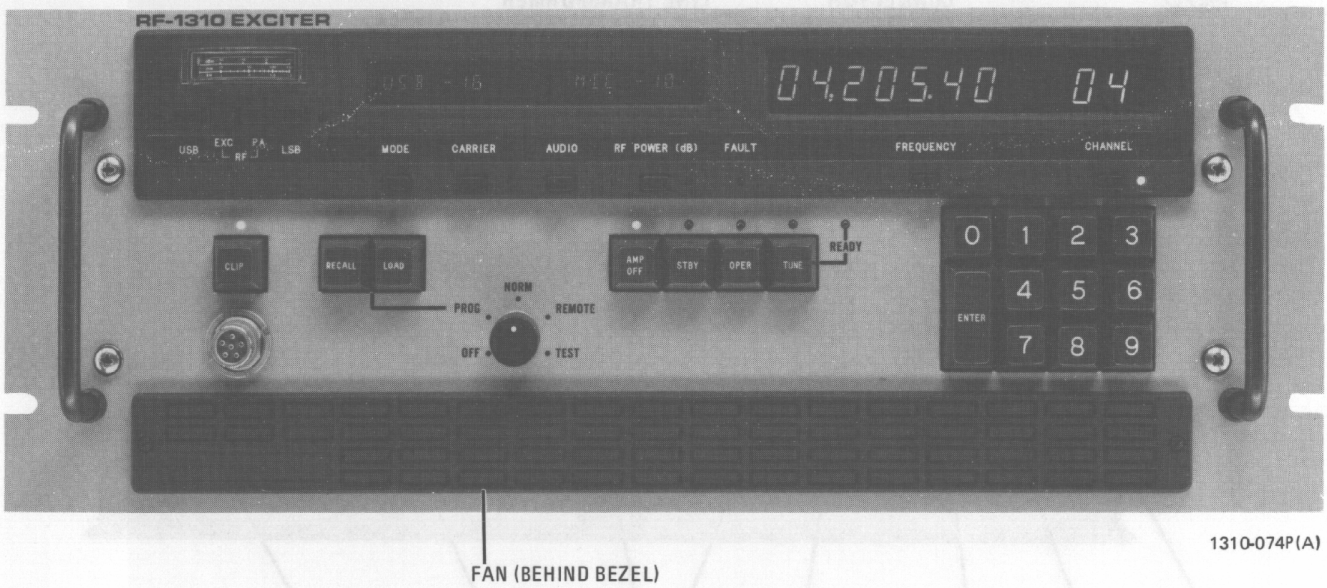


Figure 3. RF-1310 Front View

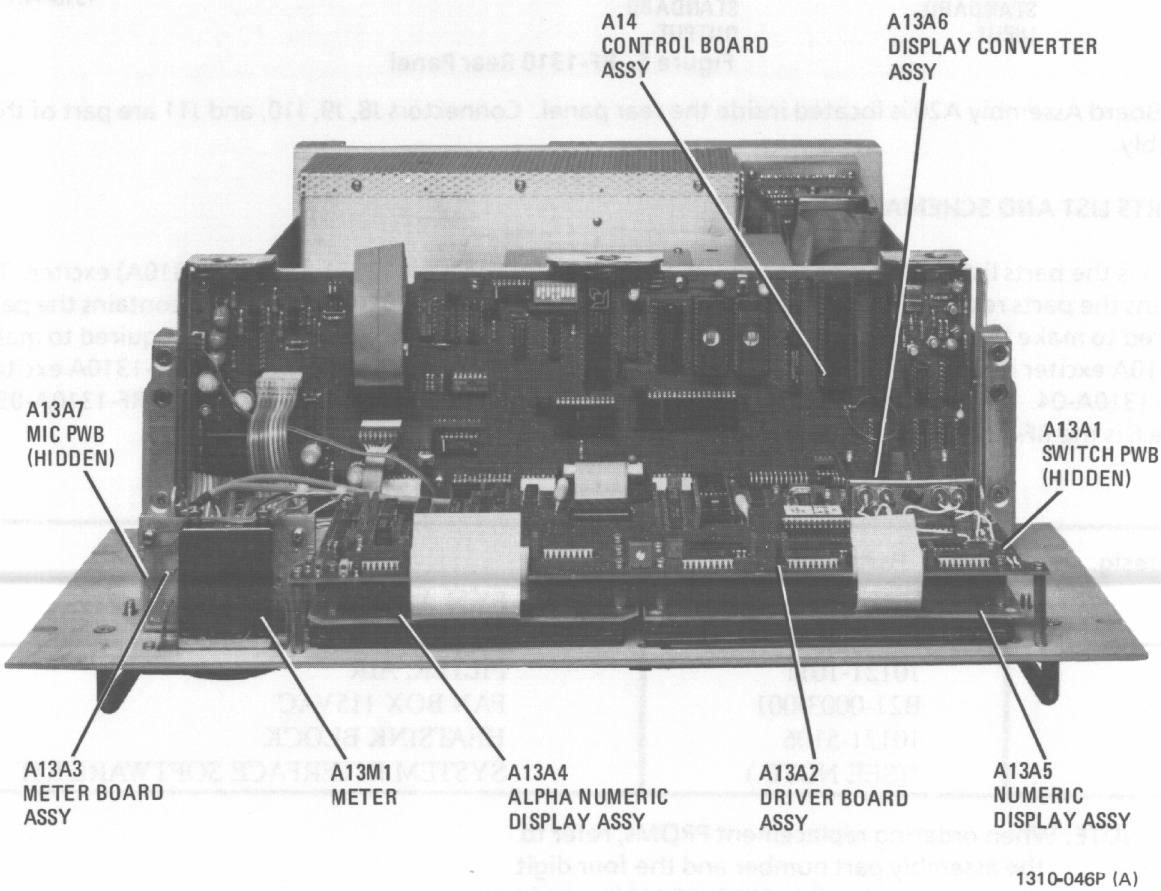


Figure 4. RF-1310 Front View With Panel Down

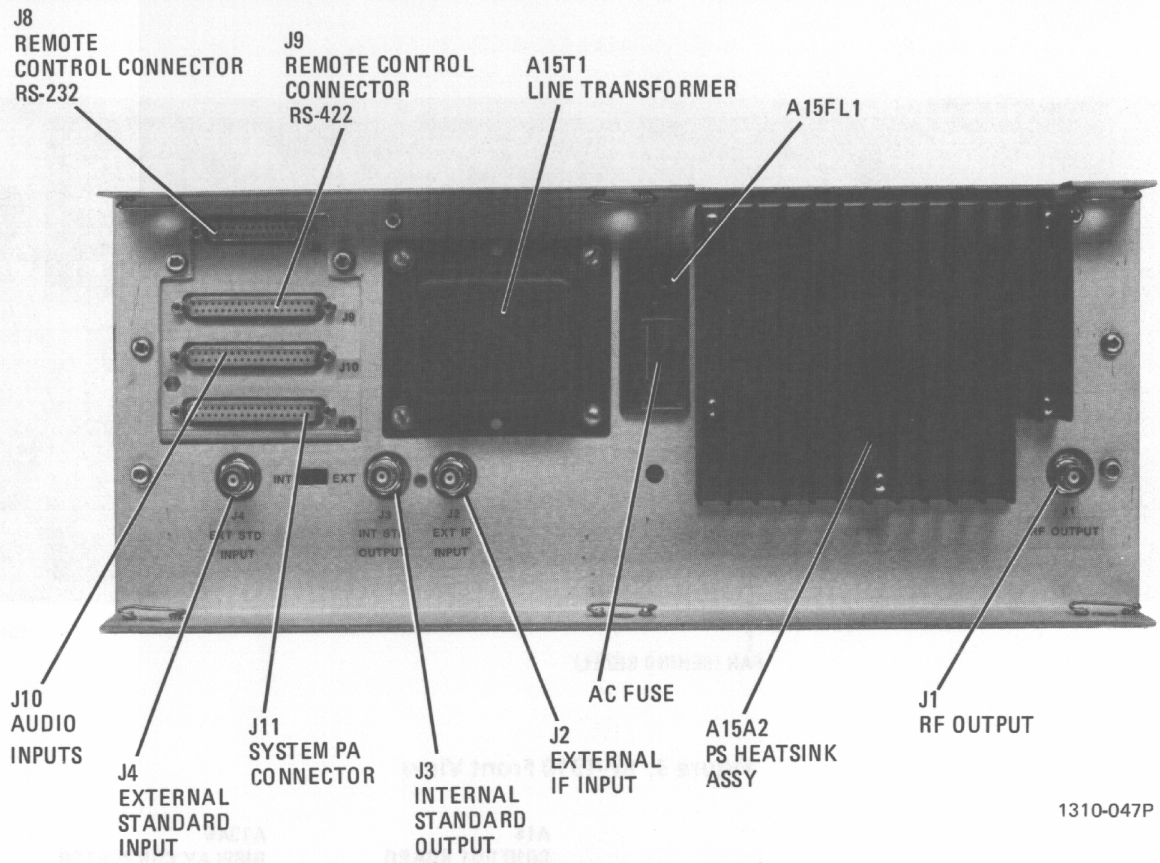


Figure 5. RF-1310 Rear Panel

Filter Board Assembly A20 is located inside the rear panel. Connectors J8, J9, J10, and J11 are part of this assembly.

2. PARTS LIST AND SCHEMATIC DIAGRAM

Table 1 is the parts list of all major assemblies and cables for the basic 10121-1030 (RF-1310A) exciter. Table 2 contains the parts required to make the RF-1310A exciter into an RF-1310A-01. Table 3 contains the parts required to make the RF-1310A exciter into an RF-1310A-02. Table 4 contains the parts required to make the RF-1310A exciter into an RF-1310A-03. Table 5 contains the parts required to make the RF-1310A exciter into an RF-1310A-04. Table 6 contains the parts required to make the RF-1310A exciter into an RF-1310A-05. Figure 6 is the RF-1310 Interconnection Schematic Diagram.

Table 1. Exciter Assembly Parts List (10121-1030 Rev. B)

Ref. Desig.	Part Number	Description
	10121-2100	PWB ASSY, SWITCH AND LED
	10121-2076	INSULATOR, FOAM
	10121-1011	FILTER, AIR
	B21-0003-001	FAN BOX 115VAC
	10121-5106	HEATSINK BLOCK
	*(SEE NOTE.)	SYSTEM INTERFACE SOFTWARE KIT

*NOTE: When ordering replacement PROMs, refer to the assembly part number and the four digit firmware number (i.e. 802A, 804A) located on the PROM label.

Table 1. Exciter Assembly Parts List (10121-1030 Rev. B) (Cont.)

Ref. Desig.	Part Number	Description
A1	10121-5100-01	PWB ASSY, OUTPUT AMPL.
A2	10121-5200	PWB ASSY, CONVERTER
A3	10121-5300	AFSK KEYER ASSEMBLY (OPTIONAL)
A4	10121-5500-XX	COMBINER ASSEMBLY (SEE NOTE 1.)
A5	10121-5400	AUDIO ASSY
A6	10073-4100-01	PWB ASSY, PLL 1 (SLOW)
A7	10073-4200	PWB ASSY, PLL 2
A8	10073-4300	PWB ASSY, PLL 3
A9	10073-4400	PWB ASSY, PLL 4
A10	10073-4500	PWB ASSY, PLL 5
A11	10121-4600	CARRIER GENERATOR ASSY
A12	10121-4750	REF. GEN. ASSEMBLY
A13	10121-2000-01	ASSY FRONT PANEL
A14	10121-2850	ASSY CONTROL PWB
A15	10121-3000	POWER SUPPLY ASSEMBLY
A16A1	10121-1200	PWB ASSY, FRONT PWR DIST
A16A3	10121-1350-01	REAR POWER DIST. PWB
A17A1	10121-6250	REMOTE BOARD ASSEMBLY
A18A1	10121-6320	LWR SYSTEM INTERFACE
A18A2	10121-63XX-XX	SYSTEM INTERFACE I/O (SEE NOTE 2.)
A20	10121-1250	FILTER ASSY, REAR PANEL
A21	759-3906	FREQ STD 1 MHZ
J7	J90-0012-001	CONN ADP SMB F'DTHRU F-F
P1	J40-0002-002	HOUSING CONN 2 PIN
W1	10121-7245	CABLE ASSY,REAR CHASSIS
W2	10121-7161	CABLE, COAX
W3	10121-7158	CABLE, COAX W3
W4	10121-7181	CABLE, COAX
W5	10121-7184	CABLE, COAX W5
W6	10121-7157	CABLE, COAX W6
W7	10121-7182	CABLE, COAX
W8	10121-7156	CABLE, COAX W8
W9	10121-7054	CABLE, RIBBON, 24 COND
W10	10121-7183	CABLE, COAX
W11	10073-7246	CABLE ASSY,AC POWER
W12	10073-7155	CABLE ASSY,COAX
W13	10073-7154	CABLE ASSY,COAX
W14	10073-7159	CABLE ASSY,COAX
W15	10073-7153	CABLE ASSY,COAX
W16	10073-7150	CABLE, COAX ASSY
W17	10121-7069	CABLE, RIBBON, PWR SUPPLY

NOTE 1: Version varies with filters purchased. See A4 tab section for complete part number.

NOTE 2: This item is system dependent. See tables 2 through 6 for part numbers.

Table 1. Exciter Assembly Parts List (10121-1030 Rev. B) (Cont.)

Ref. Desig.	Part Number	Description
W19	10121-7152	CABLE, COAX W19
W20	10121-7070	CABLE, RIBBON, 8 COND
W22	10121-7151	CABLE, COAX W22
W23	10121-7280	CABLE ASSY W23
W24	10121-7275	CABLE, RIBBON, 8 COND
W25	10073-7185	CABLE ASSY,COAX
W26	10121-7056	CABLE, RIBBON, 8 COND
W27	10121-7279	CABLE, COAX W27
W28	10121-7278	CABLE, RIBBON, 16 COND
W29	10121-7294	CABLE, RIBBON, 8COND W29
W30	10121-7162	CABLE, COAX
W31	10121-7276	CABLE, COAX W31
W32	10073-7075	RIBBON CABLE, 40 COND
W34	10121-7277	CABLE, RIBBON, 20 COND

Table 2. RF-1310A-01 Assembly and Cable Parts List (10121-6300-21 Rev. A)

Ref. Desig.	Part Number	Description
RF-1310A	10121-1030	RF-1310A SERIES EXCITER
A4	10121-5500-03	COMBINER PWB ASSY
A18A2	10121-6370-01	SYSTEM INTFC. PWB ASSY
A23	10121-5800	POWER SUPPLY ASSY
	10121-0021	ANCILLARY KIT
	10121-0120	RF-1310A SERIES MANUAL
	10121-0121	A18A2 SYST. INTFC. SUPPLEMENT
	10121-7325	CABLE ASSY
	*SEE NOTE	SYST. INTFC. SOFTWARE KIT

*NOTE: When ordering replacement PROMs, refer to the assembly part number and the four digit firmware number (i.e. 802A, 804A) located on the PROM label.

Table 3. RF-1310A-02 Assembly and Cable Parts List (10121-6300-22 Rev. A)

Ref. Desig.	Part Number	Description
RF-1310A	10121-1030	RF-1310A SERIES EXCITER
A4	10121-5500-03	COMBINER PWB ASSY
A18A2	10121-6350	SYSTEM INTFC. PWB ASSY
A23	10121-5800	POWER SUPPLY ASSY
	10121-0021	ANCILLARY KIT
	10121-0120	RF-1310A SERIES MANUAL
	10121-0122	A18A2 SYST. INTFC. SUPPLEMENT
	10121-7301	CABLE ASSY
	*SEE NOTE	SYST. INTFC. SOFTWARE KIT

Table 4. RF-1310A-03 Assembly and Cable Parts List (10121-6300-23 Rev. A)

Ref. Desig.	Part Number	Description
RF-1310A	10121-1030	RF-1310A SERIES EXCITER
A4	10121-5500-03	COMBINER PWB ASSY
A18A2	10121-6350	SYSTEM INTFC. PWB ASSY
A23	10121-5800	POWER SUPPLY ASSY
	10121-0021	ANCILLARY KIT
	10121-0120	RF-1310A SERIES MANUAL
	10121-0123	A18A2 SYST. INTFC. SUPPLEMENT
	10121-7302	CABLE ASSY
	*SEE NOTE	SYST. INTFC. SOFTWARE KIT

Table 5. RF-1310A-04 Assembly and Cable Parts List (10121-6300-24 Rev. A)

Ref. Desig.	Part Number	Description
RF-1310A	10121-1030	RF-1310A SERIES EXCITER
A4	10121-5500-03	COMBINER PWB ASSY
A18A2	10121-6350	SYSTEM INTFC. PWB ASSY
A23	10121-5800	POWER SUPPLY ASSY
	10121-0021	ANCILLARY KIT
	10121-0120	RF-1310A SERIES MANUAL
	10121-0124	A18A2 SYST. INTFC. SUPPLEMENT
	*SEE NOTE	SYST. INTFC. SOFTWARE KIT

*NOTE: When ordering replacement PROMs, refer to the assembly part number and the four digit firmware number (i.e. 802A, 804A) located on the PROM label.

Table 6. RF-1310A-05 Assembly and Cable Parts List (10121-6300-05 Rev. H)

Ref. Desig.	Part Number	Description
RF-1310A	10121-1030	RF-1310A SERIES EXCITER
A4	10121-5500-03	COMBINER PWB ASSY
A18A2	10121-6390	SYSTEM INTFC. PWB ASSY
A23	10121-5800	POWER SUPPLY ASSY
	10121-0021	ANCILLARY KIT
	10121-0120	RF-1310A SERIES MANUAL
	10121-0125	A18A2 SYST. INTFC. SUPPLEMENT
	*SEE NOTE	SYST. INTFC. SOFTWARE KIT

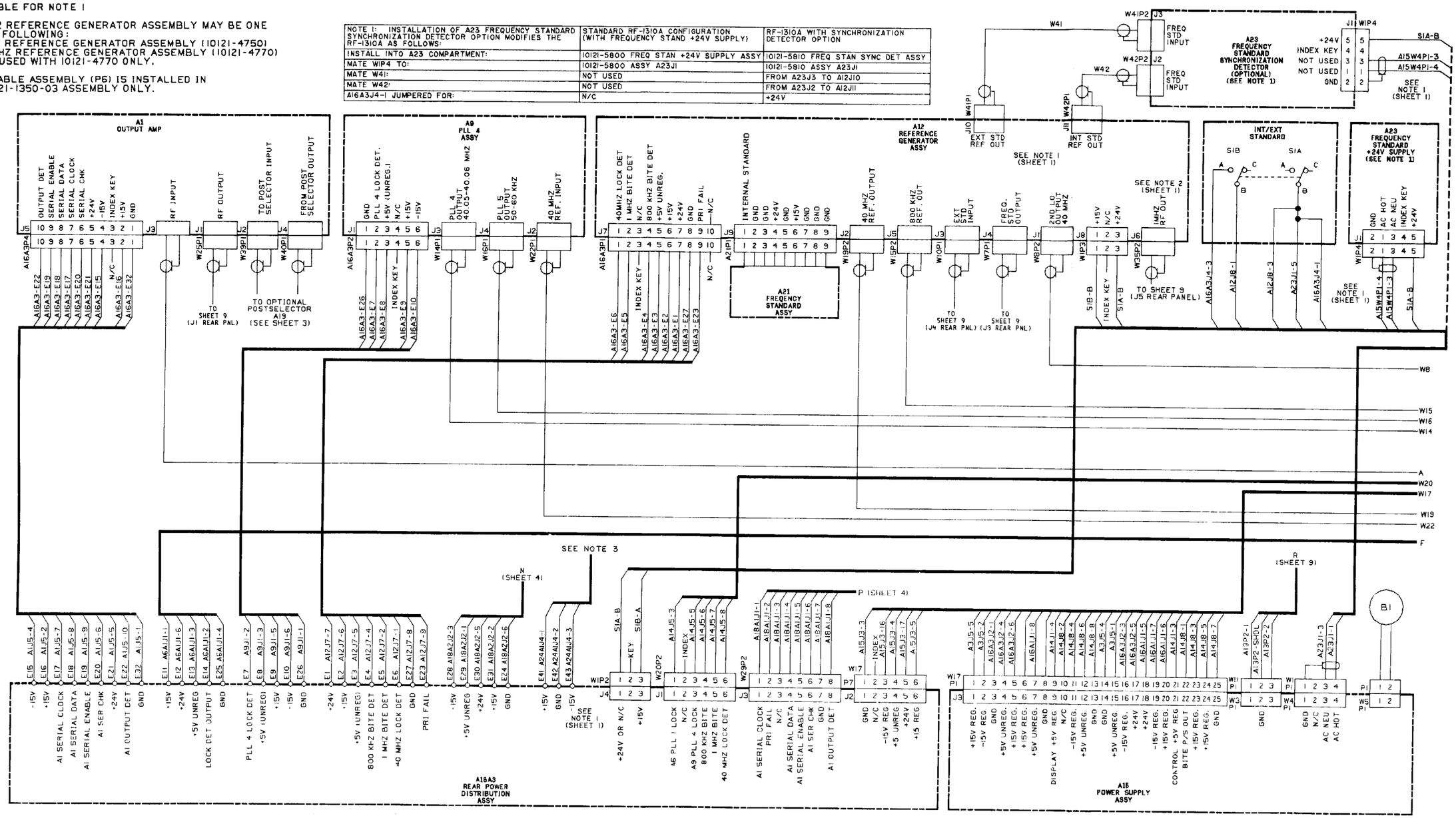
*NOTE: When ordering replacement PROMs, refer to the assembly part number and the four digit firmware number (i.e. 802A, 804A) located on the PROM label.

NOTES:
1 SEE TABLE FOR NOTE 1

2 THE A12 REFERENCE GENERATOR ASSEMBLY MAY BE ONE OF THE FOLLOWING:
I MHZ REFERENCE GENERATOR ASSEMBLY (10121-4750)
100 KHZ REFERENCE GENERATOR ASSEMBLY (10121-4770)
W35 IS USED WITH 10121-4770 ONLY.

3 THIS CABLE ASSEMBLY (P6) IS INSTALLED IN THE 10121-1350-03 ASSEMBLY ONLY.

NOTE 1: INSTALLATION OF A23 FREQUENCY STANDARD SYNCHRONIZATION DETECTOR OPTION MODIFIES THE RF-1310A AS FOLLOWS:	STANDARD RF-1310A CONFIGURATION (WITH FREQUENCY STAND +24V SUPPLY)	RF-1310A WITH SYNCHRONIZATION DETECTOR OPTION
INSTALL INTO A23 COMPARTMENT:	10121-5800 FREQ STAN +24V SUPPLY ASSY	10121-5810 FREQ STAN SYNC DET ASSY
MATE WIP4 TO:	10121-5800 ASSY A23J1	10121-5810 ASSY A23J1
MATE W41:	NOT USED	FROM A23J3 TO A12J10
MATE W42:	NOT USED	FROM A23J2 TO A12J11
A16A3J4-1 JUMPERED FOR:	N/C	+24V



PART NO.	SHEETS	USED ON
10121-1031	USES SHEETS 1-9	STANDARD VERSIONS
10121-1031-01	USES SHEETS 1-7, 9, 10 SHEET 10 REPLACES SHEET 8	RF-1310A-03D WITH RF-1135

Figure 6. **RF-1310 Interconnection Schematic Diagram (10121-1031 Rev. G) (Sheet 1 of 10)**

Assemblies A1, A9, A12, A15, A16A3, A21, A23

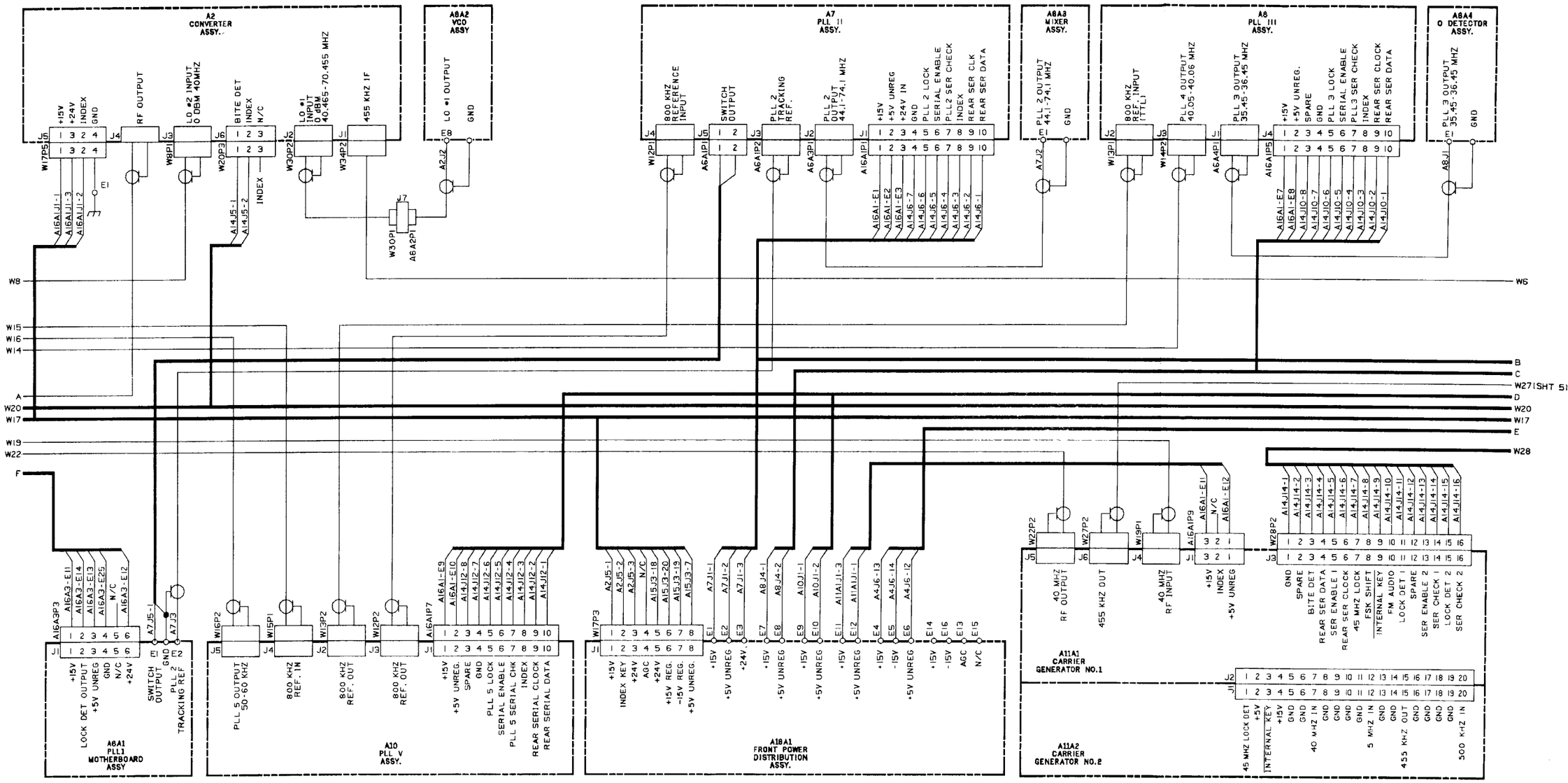


Figure 6. **RF-1310 Interconnection Schematic Diagram (10121-1031 Rev. G) (Sheet 2 of 10)**

Assemblies A2, A6A1, A6A2, A6A3, A6A4, A7, A8, A10, A11A1, A11A2, A16A1

NOTE 1: THIS CONNECTOR MATES TO THE A19 POST SELECTOR OPTION AT A19A1J10 (A19A2J2 FOR THE RF-1317 OPTION) IF THE A3 AFSK OPTION 13 NOT INSTALLED.

NOTE 2: THE VIEW SHOWN IS THE INTERCONNECTION TO THE RF-1317A POST SELECTOR OPTION. FOR CONNECTION TO THE RF-1317 POST SELECTOR REFER TO THE FOLLOWING TABLE:

W35P2 MATES TO A19A2J1
W45P2 MATES TO A19A2J2
W40P2 MATES TO A19A1A2J1
W39P2 MATES TO A19A1A2J2

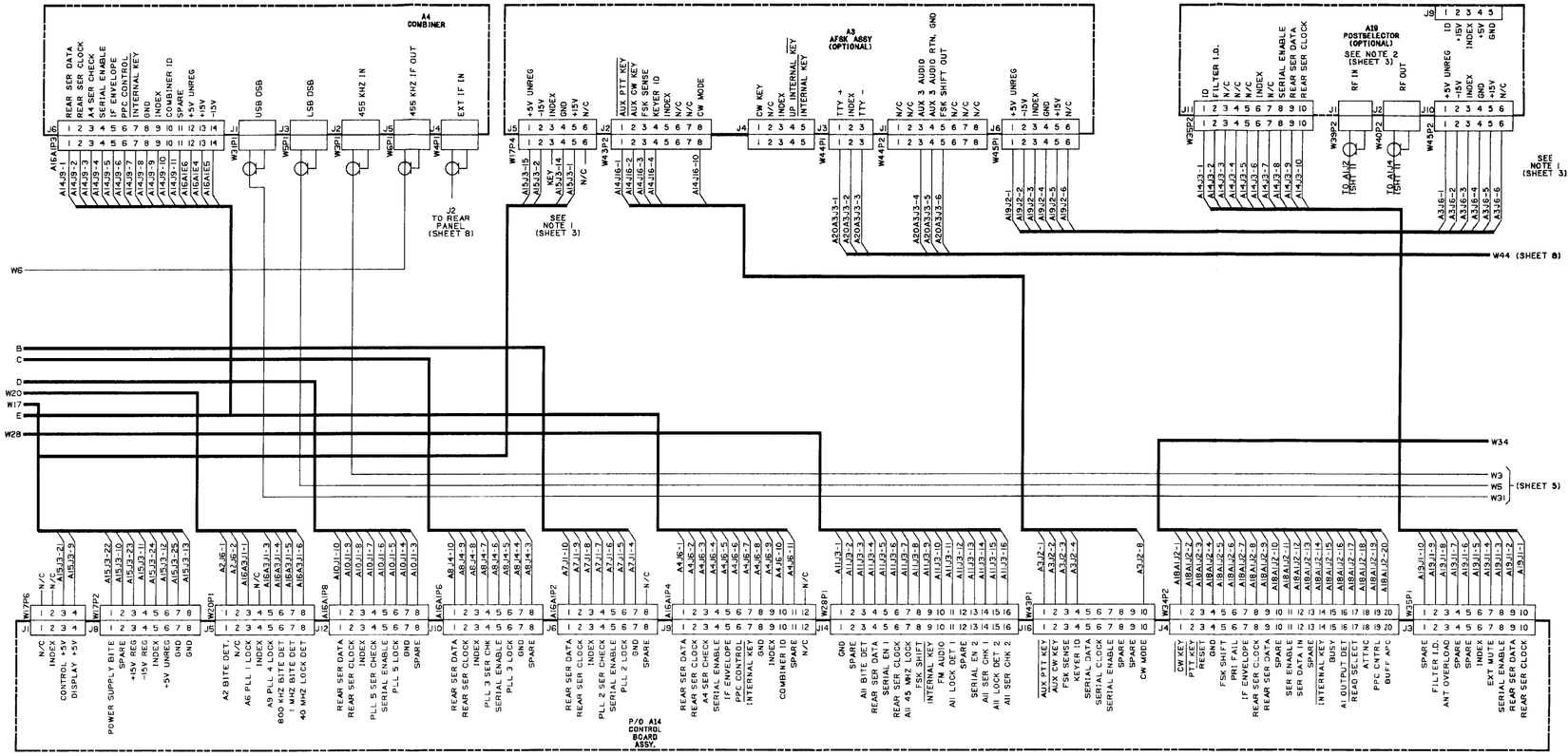
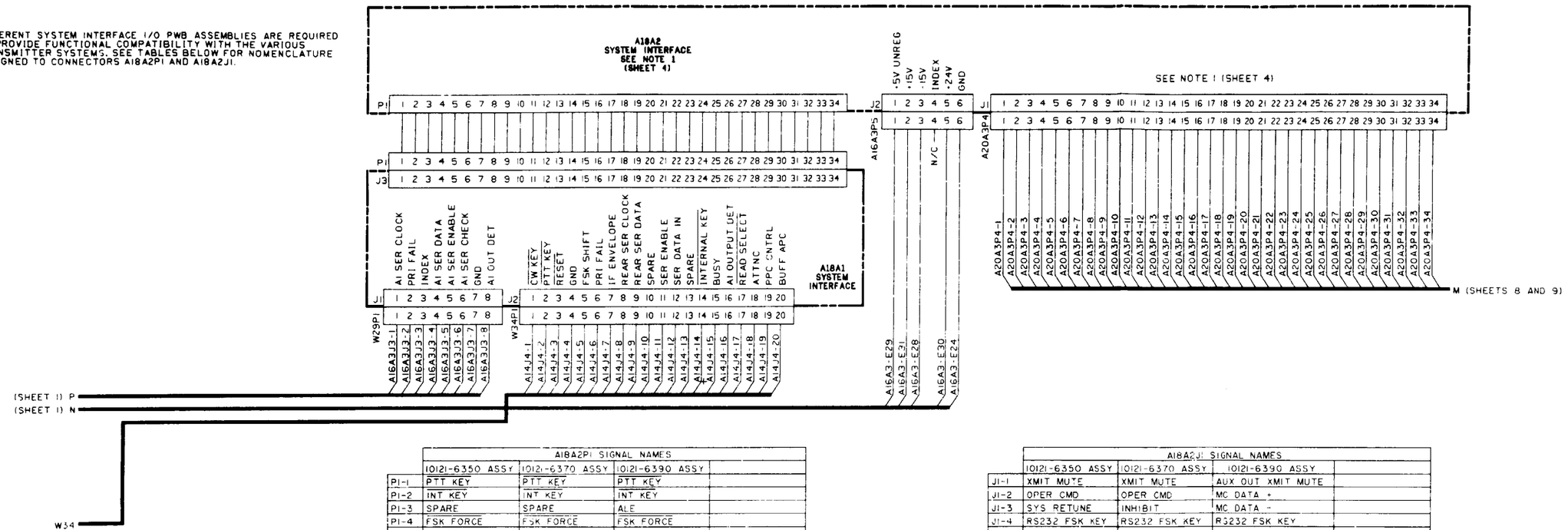


Figure 6. RF-1310 Interconnection Schematic Diagram (10121-1031 Rev. G) (Sheet 3 of 10)

Assemblies A3, A4, P/O A14, A19

NOTE 1: DIFFERENT SYSTEM INTERFACE I/O PWB ASSEMBLIES ARE REQUIRED TO PROVIDE FUNCTIONAL COMPATIBILITY WITH THE VARIOUS TRANSMITTER SYSTEMS. SEE TABLES BELOW FOR NOMENCLATURE ASSIGNED TO CONNECTORS A18A2P1 AND A18A2J1.



	A18A2P1 SIGNAL NAMES		
	10121-6350 ASSY	10121-6370 ASSY	10121-6390 ASSY
P1-1	PTT KEY	PTT KEY	PTT KEY
P1-2	INT KEY	INT KEY	INT KEY
P1-3	SPARE	SPARE	ALE
P1-4	FSK FORCE	FSK FORCE	FSK FORCE
P1-5	SPARE	SPARE	A8
P1-6	AD1	AD1	AD1
P1-7	PPC CONTROL	PPC CONTROL	PPC CONTROL
P1-8	AD2	AD2	AD2
P1-9	SPARE	SPARE	SPARE
P1-10	AD7	AD7	AD7
P1-11	FSK SHIFT	FSK SHIFT	FSK SHIFT
P1-12	AD6	AD6	AD6
P1-13	CW KEY	CW KEY	CW KEY
P1-14	AD5	AD5	AD5
P1-15	AD0	AD0	AD0
P1-16	AD4	AD4	AD4
P1-17	CS2 (N/C)	CS2 (N/C)	CS2
P1-18	AD3	AD3	AD3
P1-19	CS1	CS1	CS1
P1-20	WR	WR	WR
P1-21	RESET	RESET	RESET
P1-22	RD	RD	RD
P1-23	BUFF APC #2	PA METER	PA METER
P1-24	PPC DISABLE	PPC DISABLE	PPC DISABLE
P1-25	GND	GND	GND
P1-26	BUFF APC #1	BUFFERED APC	BUFFERED APC
P1-27	GND	GND	GND
P1-28	AI (N/C)	AI (N/C)	N/C
P1-29	SPARE	IF ENVELOPE	IF ENVELOPE
P1-30	A0	A0	N/C
P1-31	+5V	+5V	+5V
P1-32	+5V	+5V	+5V
P1-33	+5V UNREG	+5V UNREG	+5V UNREG
P1-34	+5V UNREG	+5V UNREG	+5V UNREG

	A18A2J1 SIGNAL NAMES		
	10121-6350 ASSY	10121-6370 ASSY	10121-6390 ASSY
J1-1	XMIT MUTE	XMIT MUTE	AUX OUT XMIT MUTE
J1-2	OPER CMD	OPER CMD	MC DATA +
J1-3	SYS RETUNE	INHIBIT	MC DATA -
J1-4	RS232 FSK KEY	RS232 FSK KEY	RS232 FSK KEY
J1-5	BANDSWITCH A	BANDSWITCH E	AUX RS-422 RX +
J1-6	BANDSWITCH B	BANDSWITCH D	AUX RS-422 RX -
J1-7	BANDSWITCH C	BANDSWITCH C	XCTR DATA +
J1-8	BANDSWITCH D	BANDSWITCH B	N/C
J1-9	BANDSWITCH E	BANDSWITCH A	XCTR DATA -
J1-10	SYS KEY INTLK	PA READY	AUX RS-422 RX -
J1-11	TUNE PWR REQ	TUNE ENABLE	AUX RS-422 RX +
J1-12	CW KEY	CW KEY	CW KEY
J1-13	SYS KEYLINE	SYS KEYLINE	SYS KEYLINE
J1-14	N/C	PPC	PPC
J1-15	N/C	CHASSIS GND	CHASSIS GND
J1-16	N/C	N/C	N/C
J1-17	N/C	N/C	N/C
J1-18	BYPASS REQ	TUNE CMD I	N/C
J1-19	N/C	TUNE CMD II	N/C
J1-20	PA FAULT	FAULT	N/C
J1-21	N/C	N/C	N/C
J1-22	N/C	TGC	TGC
J1-23	N/C	STBY READBACK	N/C
J1-24	N/C	OPER READBACK	N/C
J1-25	PA CLASS	N/C	N/C
J1-26	PTT KEY	N/C	N/C
J1-27	BYPASS	BYPASS	N/C
J1-28	STBY CMD	STBY CMD	N/C
J1-29	N/C	10 KW REF	10 KW REFLD
J1-30	N/C	N/C	N/C
J1-31	PTT RETURN	PTT RETURN	PTT KEY
J1-32	APC	10 KW FWD (APC)	10 KW FWD (APC)
J1-33	N/C	N/C	N/C
J1-34	INT KEY	INT KEY	INT KEY

Figure 6. **RF-1310 Interconnection Schematic Diagram (10121-1031 Rev. G) (Sheet 4 of 10)**

Assemblies A18A1, A18A2

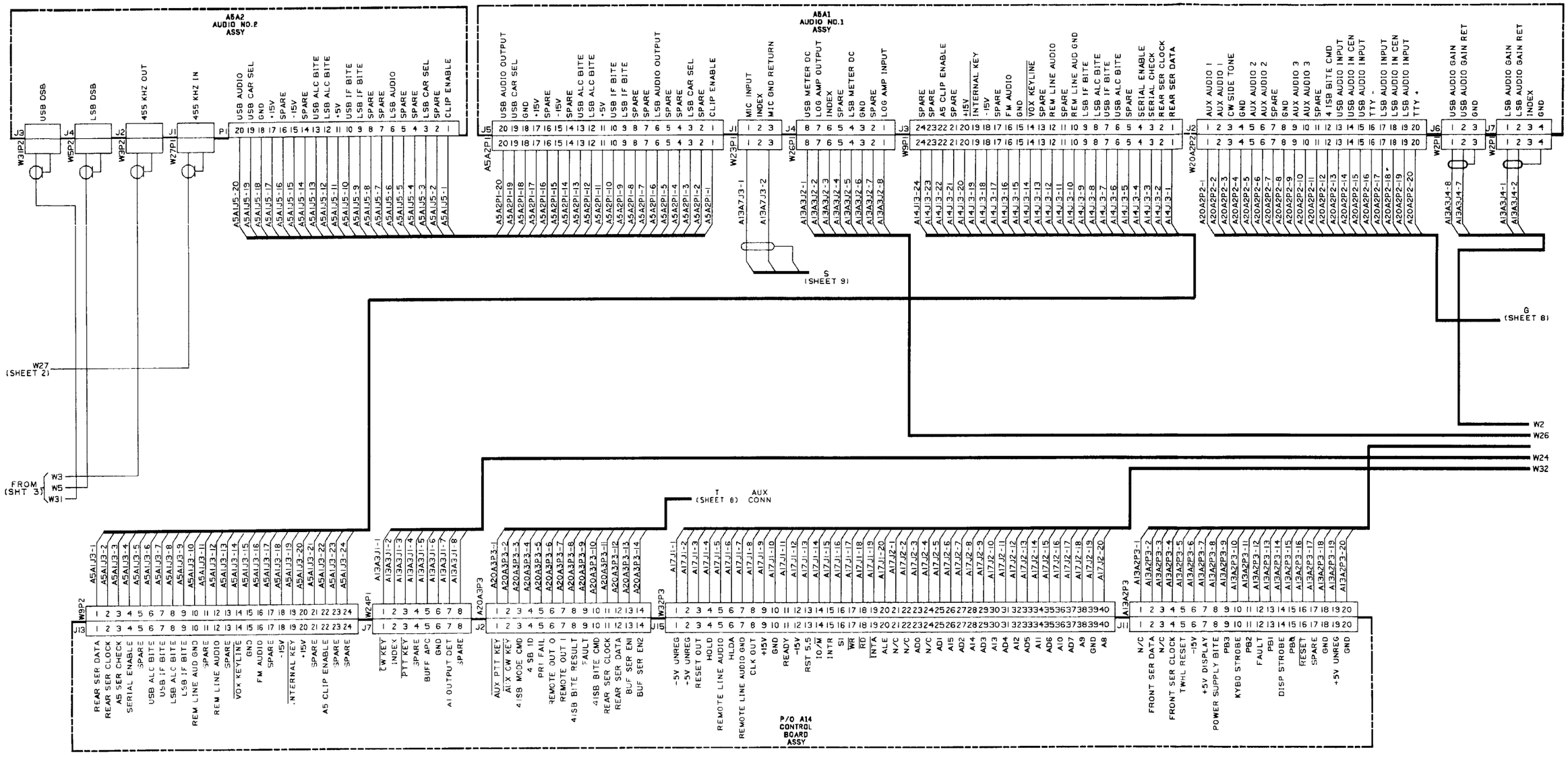


Figure 6. **RF-1310 Interconnection Schematic Diagram (10121-1031 Rev. G) (Sheet 5 of 10)**

Assemblies P/O A14, A5A1, A5A2

NOTE 1: SIGNAL NAMES IN ( ) REFER TO THE 10121-6250 VERSION ONLY OF THE A17A1 REMOTE CONTROL ASSY.

NOTE 2: A17A2 MODEM ASSY OPTION ALLOWS REMOTE FSK CAPABILITES FOR THE 10121-6250 REMOTE CONTROL ASSY ONLY.

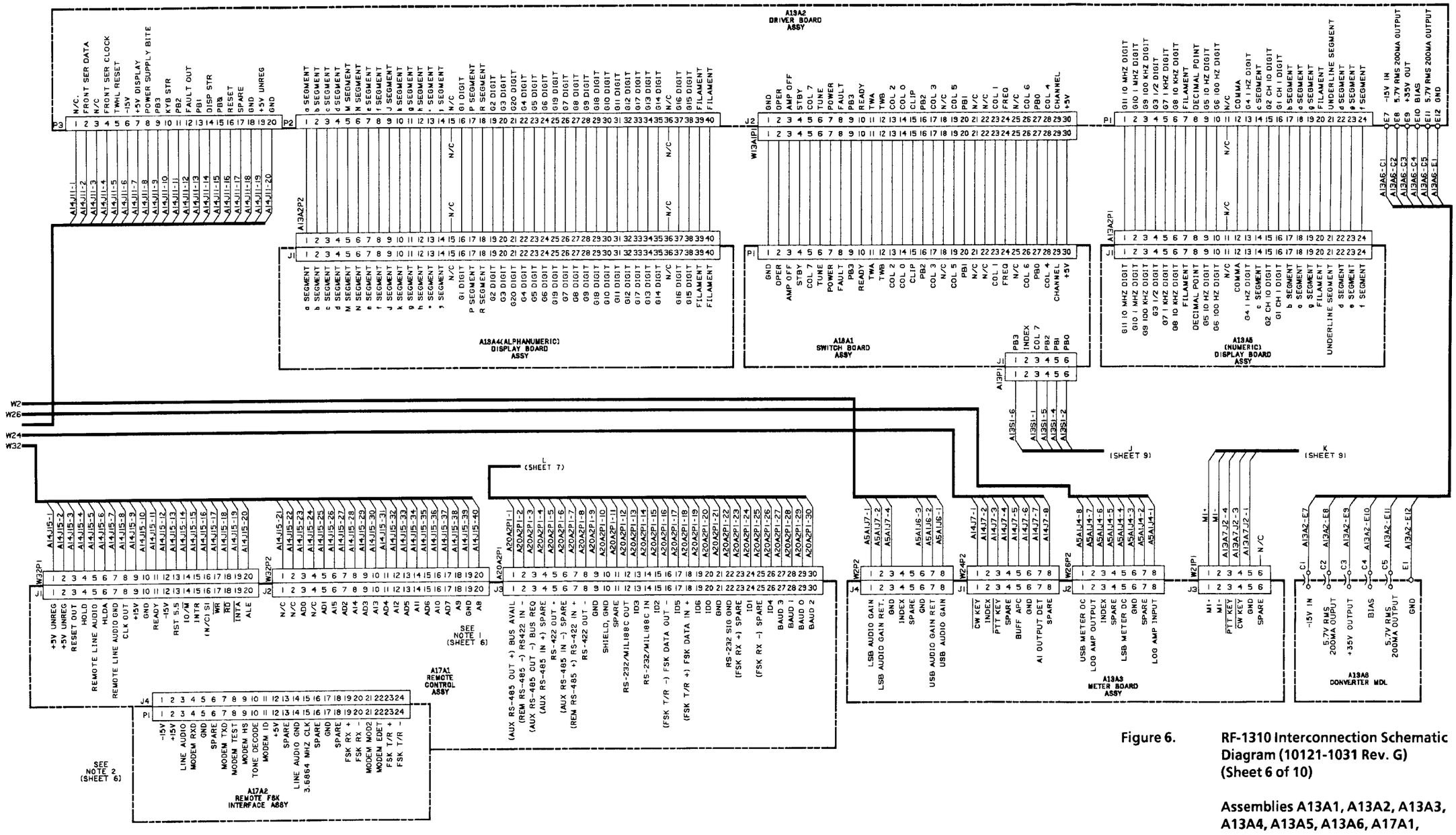


Figure 6. RF-1310 Interconnection Schematic Diagram (10121-1031 Rev. G) (Sheet 6 of 10)

Assemblies A13A1, A13A2, A13A3, A13A4, A13A5, A13A6, A17A1, A17A2

NOTE 1: SIGNAL NAMES AT A20A1J8, A20A1J9 AND A20A2P1 DEPEND UPON WHETHER A 10121-6200 OR 10121-6250 REMOTE CONTROL ASSY IS INSTALLED INTO THE RF-1310A. REFER TO TABLE 1 FOR SIGNAL NAMES.

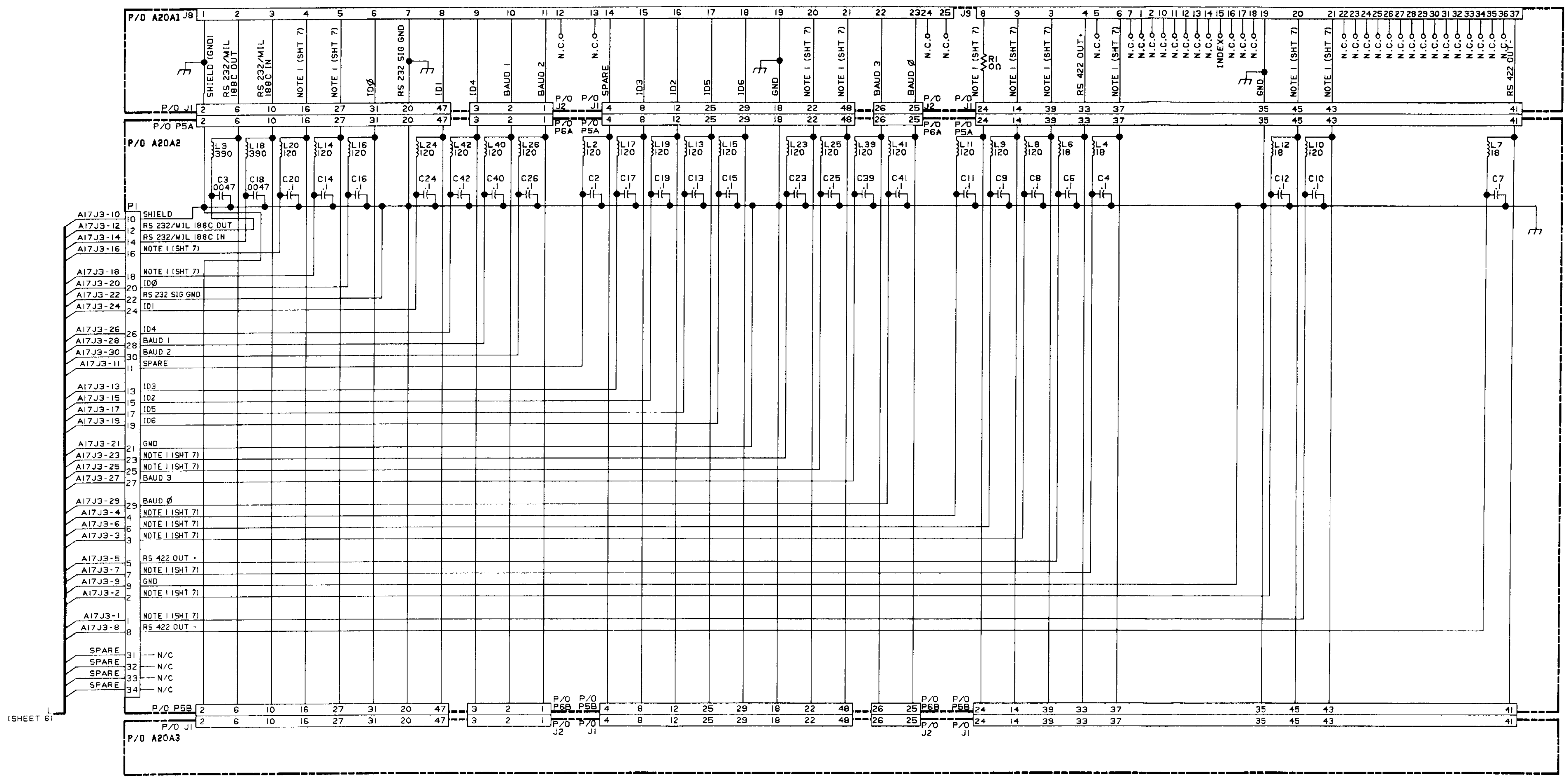


TABLE 1

A20A2P1-	A20A1J8-	A20A1J9-	A17 ASSY 10121-6200	A17 ASSY 10121-6250
16	4	-	FSK DATA OUT -	FSK T/R -
18	5	-	FSK DATA IN +	FSK T/R +
23	20	-	SPARE	FSK RX +
25	21	-	SPARE	FSK RX -
4	-	8	SPARE	AUX RS-485 IN +
6	-	9	SPARE	AUX RS-485 IN -
3	-	3	BUS REQUEST	AUX RS-485 OUT -
7	-	6	RS422 IN +	REM RS-485 +
2	-	20	RS422 IN -	REM RS-485 -
1	-	21	BUS AVAILABLE	AUX RS-485 OUT +

Figure 6. **RF-1310 Interconnection Schematic Diagram (10121-1031 Rev. G) (Sheet 7 of 10)**

Assemblies P/O A20A1, P/O A20A2, P/O A20A3

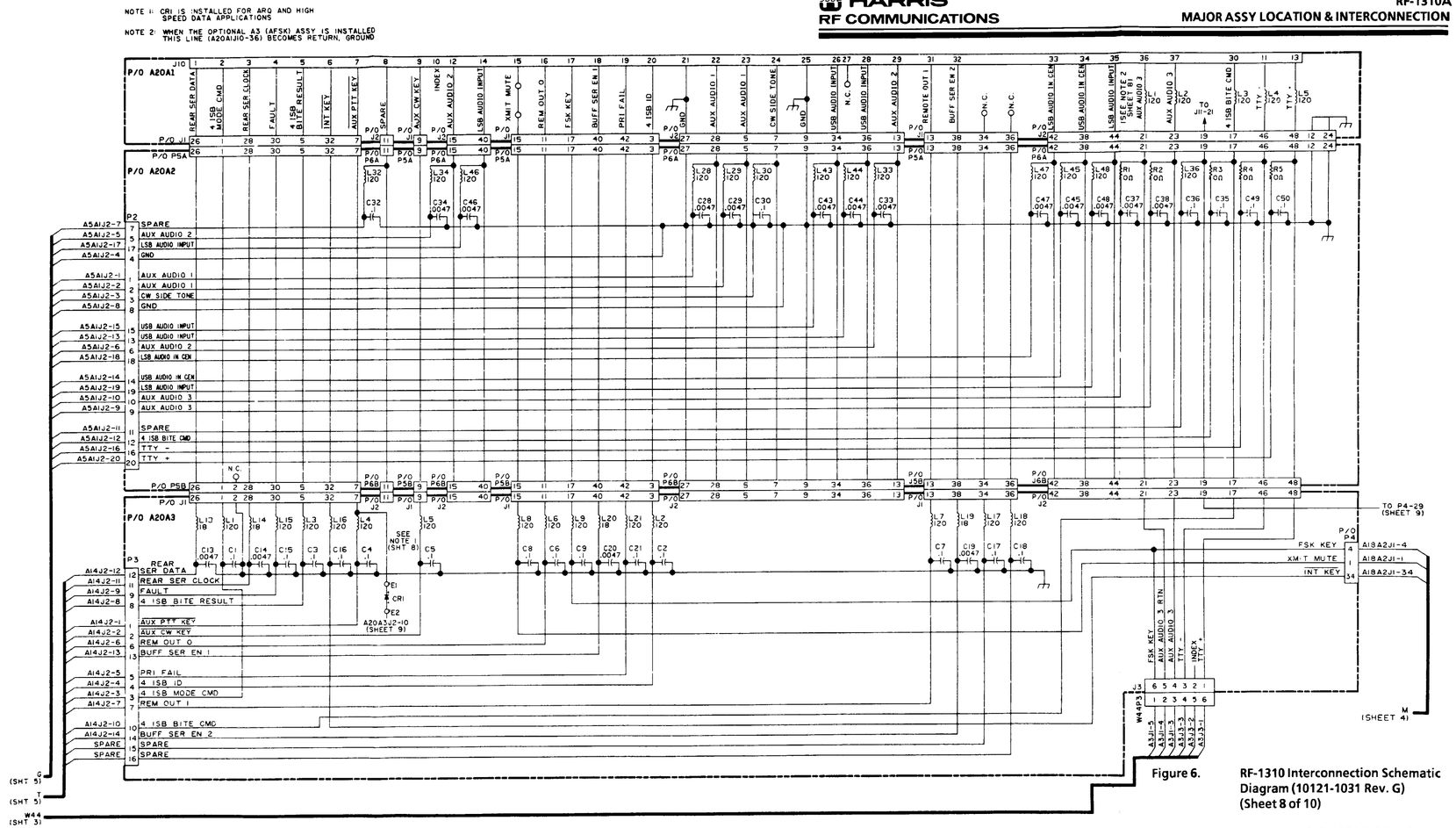


Figure 6. RF-1310 Interconnection Schematic Diagram (10121-1031 Rev. G) (Sheet 8 of 10)

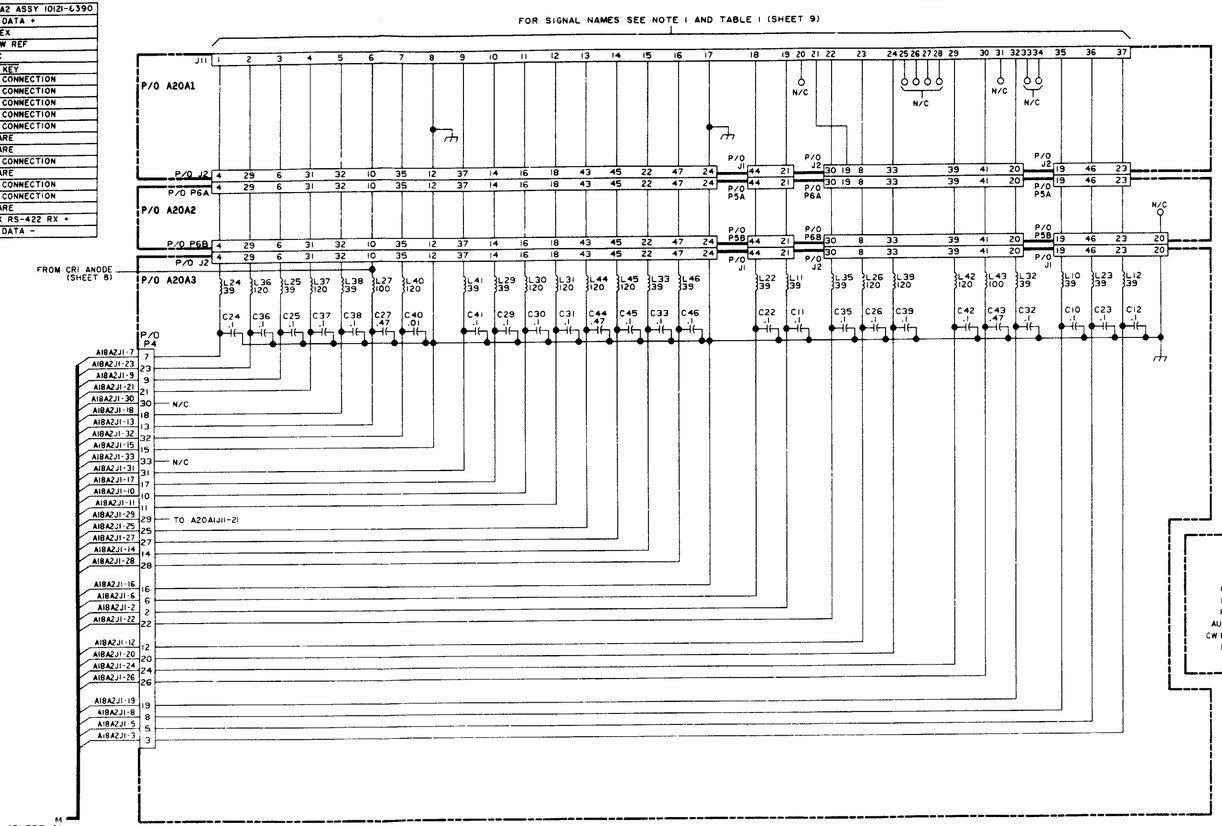
Assemblies P/O A20A1, P/O A20A2, P/O A20A3

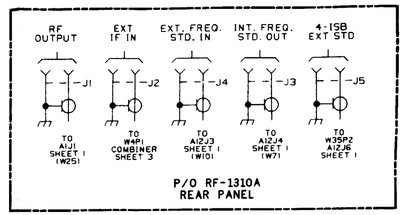
TABLE 1

	A18A2 ASSY 10121-6350	A18A2 ASSY 10121-6370	A18A2 ASSY 10121-6390
J11-1	PA BNDSW CODE C	PA BNDSW CODE C	XCTR DATA +
J11-2	SPARE	STBY READBACK	SPARE
J11-3	PA BNDSW CODE E	PA BNDSW CODE A	XCTR DATA -
J11-4	SPARE	SPARE	SPARE
J11-5	BYPASS REQUEST	TUNE CMD I	SPARE
J11-6	SYS KEYLINE	SYS KEYLINE	SYS KEYLINE
J11-7	APC	10KW FWD (APC)	10KW FWD (APC)
J11-8	CHASSIS GND	CHASSIS GND	CHASSIS GND
J11-9	PTT RETURN	PTT RETURN	PTT RETURN
J11-10	NO CONNECTION	NO CONNECTION	NO CONNECTION
J11-11	SYS KEY INTLK	PA READY	AUX RS-422 RX -
J11-12	TUNE PWR REQ	TUNE ENABLE	AUX RS-422 RX +
J11-13	PA CLASS	SPARE	SPARE
J11-14	BYPASS	BYPASS	SPARE
J11-15	SPARE	PPC	PPC
J11-16	STBY CMD	STBY CMD	SPARE
J11-17	CHASSIS GND	CHASSIS GND	CHASSIS GND
J11-18	PA BANDSW CODE B	PA BNDSW CODE D	AUX RS-422 RX -

	A18A2 ASSY 10121-6350	A18A2 ASSY 10121-6370	A18A2 ASSY 10121-6390
J11-19	OPER CMD	OPER CMD	MC DATA +
J11-20	INDEX	INDEX	INDEX
J11-21	SPARE	10KW REF	10KW REF
J11-22	SPARE	TGC	TGC
J11-23	CW KEY	CW KEY	CW KEY
J11-24	PA FAULT	FAULT	NO CONNECTION
J11-25	NO CONNECTION	NO CONNECTION	NO CONNECTION
J11-26	NO CONNECTION	NO CONNECTION	NO CONNECTION
J11-27	NO CONNECTION	NO CONNECTION	NO CONNECTION
J11-28	NO CONNECTION	NO CONNECTION	NO CONNECTION
J11-29	SPARE	OPER READBACK	SPARE
J11-30	PTT KEY	SPARE	SPARE
J11-31	NO CONNECTION	NO CONNECTION	NO CONNECTION
J11-32	SPARE	TUNE CMD II	SPARE
J11-33	NO CONNECTION	NO CONNECTION	NO CONNECTION
J11-34	NO CONNECTION	NO CONNECTION	NO CONNECTION
J11-35	PA BNDSW CODE D	PA BNDSW CODE B	SPARE
J11-36	PA BNDSW CODE A	PA BNDSW CODE E	AUX RS-422 RX +
J11-37	SYSTEM RETUNE	INHIBIT	MC DATA -

NOTE 1: J11 SIGNAL NAMES ARE SYSTEM SPECIFIC AND DEPEND UPON THE A18A2 ASSY INSTALLED INTO THE RF-1310A. REFER TO TABLE 1 FOR FUNCTION NAMES OF J11 SIGNALS.





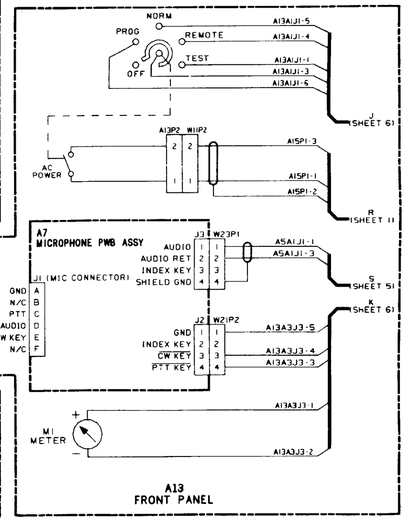


Figure 6. RF-1310 Interconnection Schematic Diagram (10121-1031 Rev. G) (Sheet 9 of 10)

Assemblies A13, P/O A20A1, P/O A20A2, P/O A20A3, P/O Rear Panel

NOTE 1: CR1 IS INSTALLED FOR ARQ AND HIGH SPEED DATA APPLICATIONS

NOTE 2: WHEN THE OPTIONAL A3 (AFSK) ASSY IS INSTALLED THIS LINE (A20AIJIO-36) BECOMES RETURN, GROUND

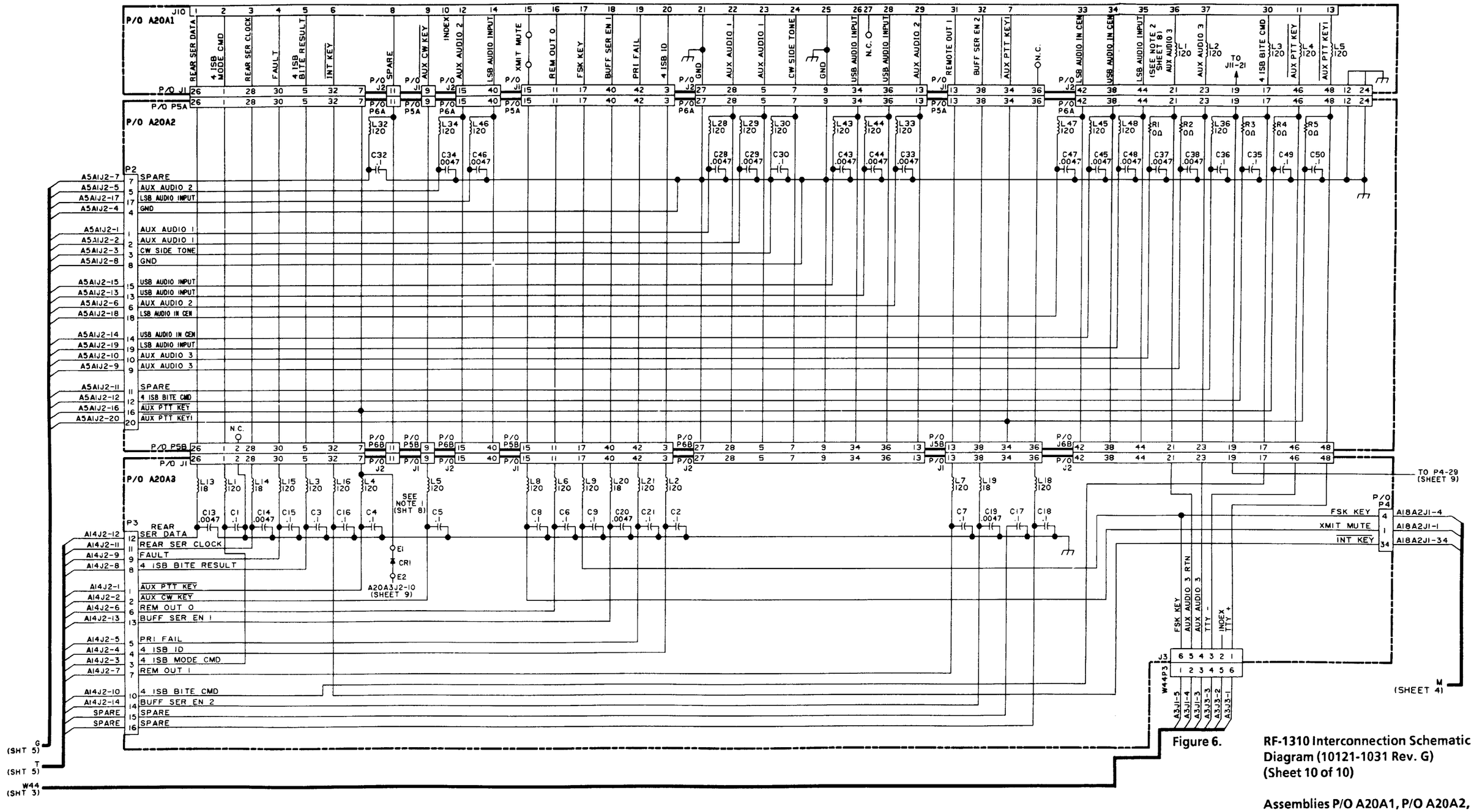
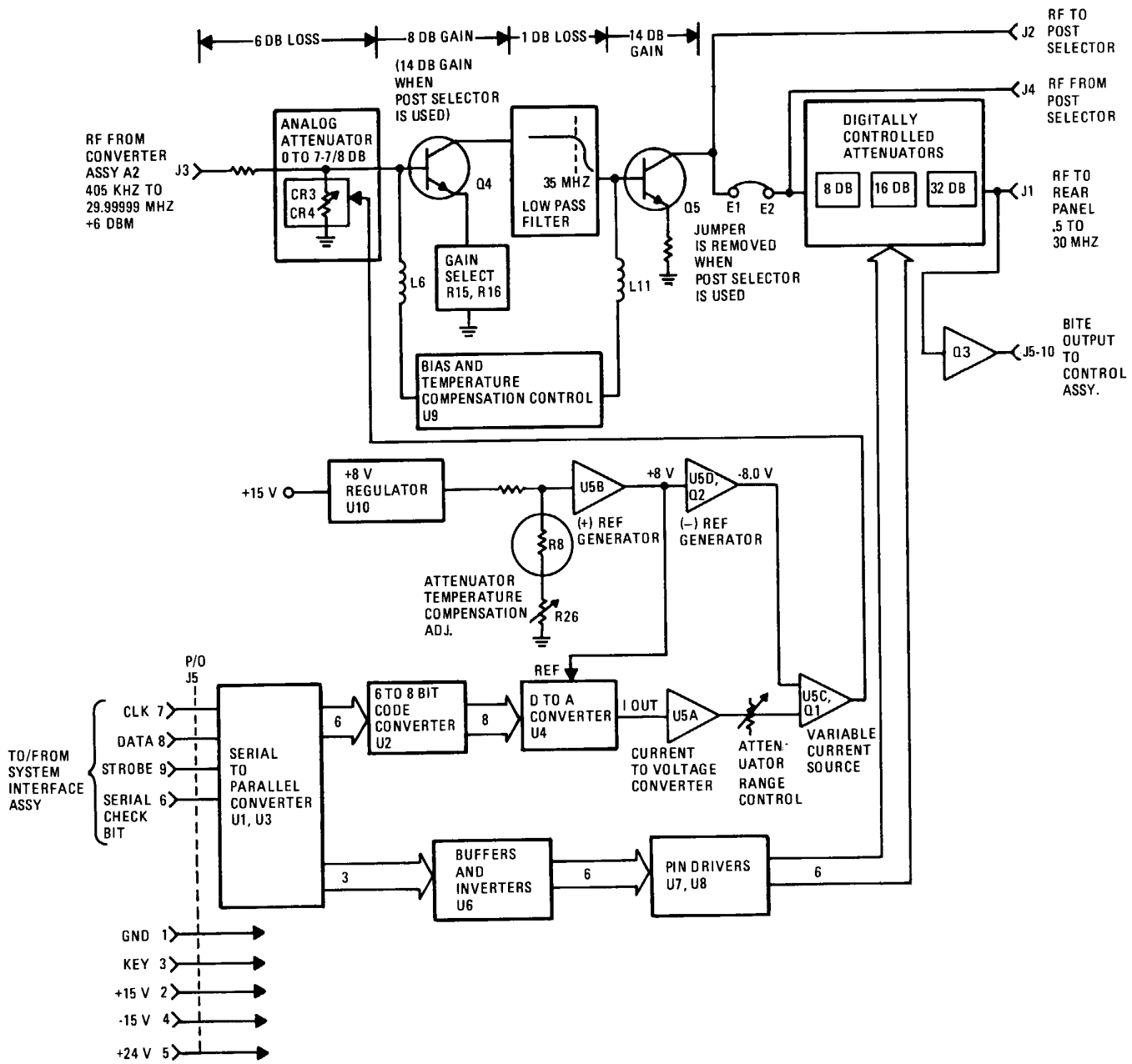


Figure 6. RF-1310 Interconnection Schematic Diagram (10121-1031 Rev. G) (Sheet 10 of 10)

Assemblies P/O A20A1, P/O A20A2, P/O A20A3

A1
OUTPUT AMPLIFIER ASSEMBLY



1310-004(A)

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OUTPUT AMPLIFIER ASSEMBLY A1

1. GENERAL DESCRIPTION

The Output Amplifier is a single PWB assembly; its position is shown in figure 1. This assembly amplifies the + 6 dBm RF signal generated by Converter Assembly A2 and controls the exciter output power level. A two-stage amplifier can boost the 405 kHz to 29.99999 MHz RF signal up to 400 mW in high-gain mode. A lowpass filter is located between the two stages to attenuate noise and spurious emissions above 35 MHz.

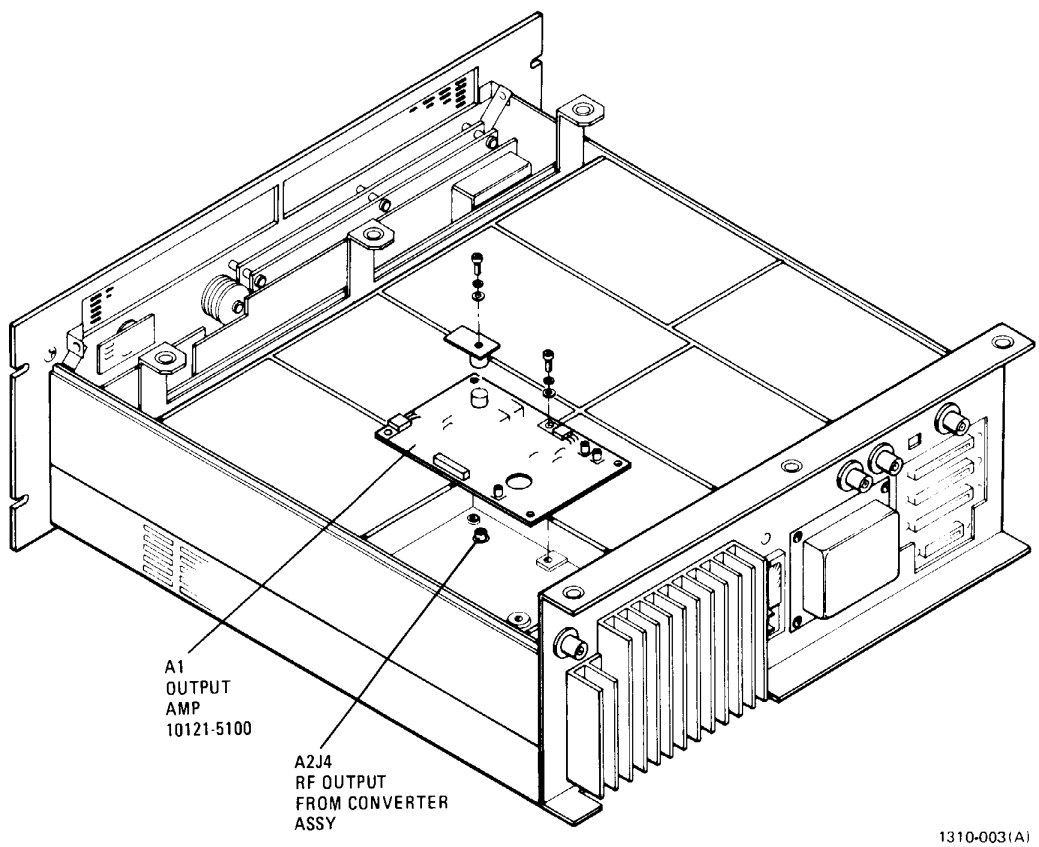


Figure 1. Output Amplifier Assembly A1 Location

Two attenuator circuits provide precise output power level control over a 63-7/8 dB range. An analog controlled attenuator can reduce the level of the incoming RF signal by 0 to 7-7/8 dB in 1/8 steps before it is introduced to the first amplifier stage. The second attenuator is digitally controlled and can reduce the level of the outgoing signal by up to 56 dB. Both attenuators are controlled by a serial data stream sent from the System Interface Assembly. The attenuator control signals are decoded and administered by digital and analog ICs.

The power control on the exciter front panel can adjust the power output over a 50 dB range in 1 dB steps. The A1 assembly can also provide automatic PA output power control in systems that have PA to exciter feedback lines.

The overall gain of the Output Amplifier Assembly can be preset to compensate for differences in system configuration. When a postselector is used, a jumper connecting E1 to E2 is removed and the gain of Q4 is set at 14 dB. For systems not using a postselector, the gain of Q4 is set at 8 dB and E1 is connected to E2.

Q3 is a driver that supplies a sample of the output signal to the exciter meter circuits and BITE circuit.

The A1 assembly mounts directly on the exciter chassis. The assembly is secured to the chassis by four mounting screws. A fifth screw secures Q5 and its mounting hardware to a heatsink built into the exciter chassis.

WARNING

Do not operate the A1 assembly unless Q5 is properly installed with a heatsink pad and insulating shoulder washer. It must be secured to the chassis or other appropriate heatsink.

A1J3 is located on the underside of the PWB. The connector cannot be accessed unless the A1 or A2 assembly is removed.

2. INTERFACE CONNECTIONS

Table 1 details the various input/output connections and other relevant data.

Table 1. Output Amplifier Assembly A1 Interface Connections

Connector	Function	Characteristics
J1	RF Output	0.5 to 30 MHz, + 20 dBm, 50 ohms
J2	Post Selector Input	0.5 to 30 MHz, + 27 dBm, 50 ohms when postselector is used
J3	RF Input	0.5 to 30 MHz, + 6 dBm, 50 ohms (nominally)
J4	Post Selector Output	0.5 to 30 MHz, + 21 dBm, 50 ohms when postselector is used
J5-1	Ground	
J5-2	Power	+ 15 Vdc, 270 mA (High Gain)/220 mA (Low Gain)
J5-3	Index Key	
J5-4	Power	-15 Vdc, 60 mA (High or Low Gain)
J5-5	Power	+ 24 V: 250 mA (High Gain); 190 mA (Low Gain)
J5-6	Serial Check Bit	P/O BITE Test, 5 Vdc = 'OK'
J5-7	Clock	TTL
J5-8	Data	Serial TTL, 0 Vdc = attenuation requested
J5-9	Strobe	+ pulse, (0 to 5 V transition) = strobe data
J5-10	BITE Output	Approximately 1 Vdc for 100 mW output

3. CIRCUIT DESCRIPTIONS

3.1 RF Signal Path

Paragraph 3.1.1 will detail circuit operation assuming that the postselector option is not installed (ie, low-gain mode is selected). Paragraph 3.1.2 will point out the differences when a postselector option is installed (high-gain mode). Note 6 of the schematic lists the circuit configurations which are applicable to the different gain modes. These configurations are preset at the factory.

3.1.1 Low Gain Mode

The A2 assembly provides + 6 dBm (into 50 ohms) at J3 from 405 kHz to 29.99999 MHz. The Analog Controlled Attenuator (ACA) network comprised of R11, R10, R12, L2, CR3, and CR4 has approximately 6 dB of initial insertion loss. PIN diodes CR3 and CR4 function as variable resistance elements, providing from 0 to 7-7/8 dB additional attenuation to the RF signal. The additional attenuation is dependent on the amount of control current supplied by Q1. (See paragraph 3.2.)

At a 0 dB ACA attenuator setting, a level of approximately 0 dBm is supplied to Q4. The low-gain configuration of Q4 provides 8 dB of gain, and the amplified signal is then applied to the low pass filter (LPF).

The LPF provides 50 dB of rejection to frequencies above 40 MHz in order to further reduce any high frequency spurious emissions. The LPF typically has 1 dB of insertion loss.

The LPF output is applied to Q5, which provides about 14 dB of signal amplification. The signal is then supplied to the discrete 8, 16, and 32 dB digitally controlled attenuator (DCA) networks.

The optimum bias points and collector currents for Q4 and Q5 are maintained by U9 and associated components. (Figure 2 shows an equivalent circuit.) Q4 and Q5 collector currents are 90 mA and 180 mA, respectively.

With the ACA set to 0 dB, approximately + 21 dBm is applied to the input of the DCA networks. Insertion loss of all three cascaded DCA networks is 1 dB, when none are selected. The nominal exciter power output is + 20 dBm (100 mW). Each DCA is configured as either a T- or pi- resistive pad which is switched in or out of the RF signal path by PIN diode switches. Potentiometers R24, R27, and R29 allow for the precise adjustment of the corresponding resistive pad. Figure 3 shows an equivalent RF circuit, in which the 16 dB DCA is the only one which has been selected. The drive current to the various PIN diode switches is supplied from drivers U7 and U8. (See paragraph 3.2.)

BITE amplifier and detector stage Q3 monitors the RF output signal level, and produces a dc output voltage proportional to this level. C51 and C52 sample the signal, Q3 amplifies it, and CR13, CR14, C37, and R43 convert it to a dc level. This BITE level is monitored by the Control Board Assembly whenever the operator chooses to perform a BITE test. At that time, a CW signal is fed through preceding signal chain assemblies and a + 6 dBm signal at the exciter's tuned frequency is presented at J3. All attenuators are set to 0 dB, and therefore the full 100 mW of output level will appear at J1. The BITE detector output will be approximately 1 Vdc for this output level under normal conditions. The Control Board Assembly will recognize this level as being valid, and will proceed in its testing. If the BITE level is significantly different, indicating a possible A1 fault, the appropriate fault code will appear on the exciter front panel.

The BITE output is also routed to the front panel meter, for use as the meter's drive signal indicating exciter output power.

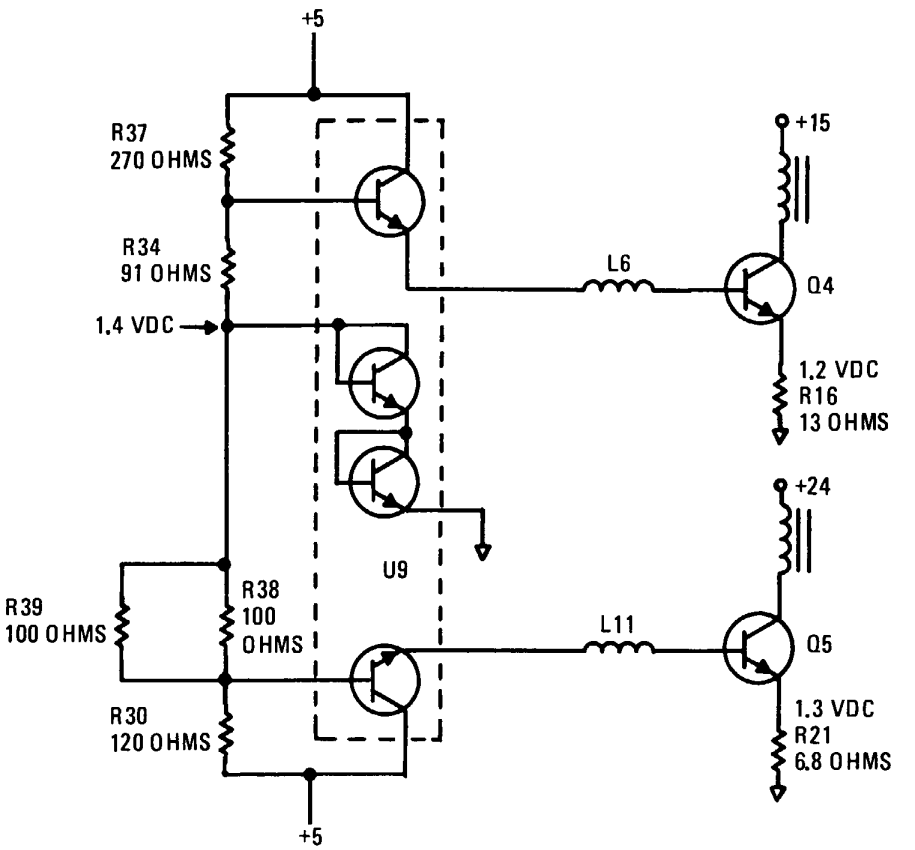


Figure 2. Q4, Q5 Equivalent Bias Circuit Low Gain Mode 1310-005

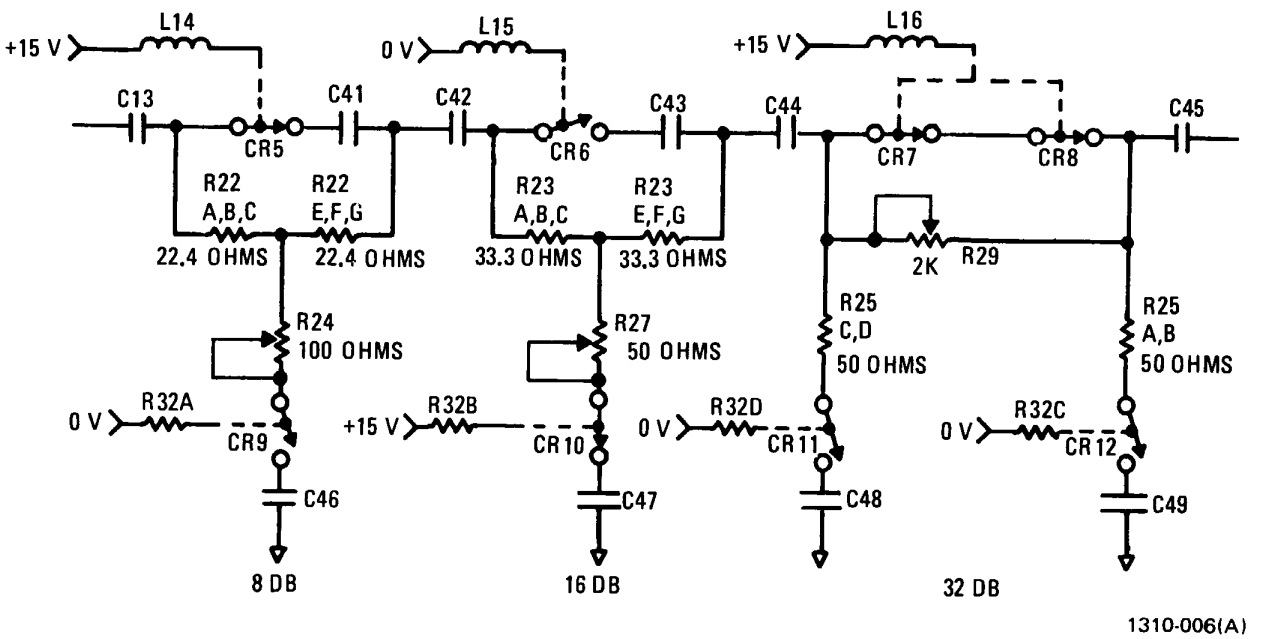


Figure 3. Digital Controlled Attenuator Equivalent Circuit

3.1.2 High Gain Mode

Exciter operation with an internal postselector option requires that the Output Amplifier Assembly gain be increased by about 6 dB to compensate for a nominal insertion loss of that option.

All circuits function as described in paragraph 3.1.1 with the following exceptions:

a. The Q4 amplifier gain is 14 dB instead of 8 dB.

b. Both Q4 and Q5 collector currents are increased to 150 mA and 250 mA respectively to accommodate the higher signal levels involved.

c. The signal path is broken at E1-E2, and the postselector is inserted in line at J2-J4.

3.2 ATTENUATION CONTROL CIRCUITRY

Data concerning the attenuation values desired are supplied from System Interface Assembly A18. Updating of the attenuator values occurs only when a change is to be made; it is not a continuous function. The System Interface Assembly receives its commands via the system PA feedback lines and/or the operator's use of the front panel power control button.

Data received at J3 pin 8 is a nine-bit data stream (MSB first) which is clocked into a serial-to-parallel converter circuit comprised of U1 and U3. All bits are clocked into and through U1 on positive clock transistions, but the outputs will not change until a strobe pulse is present. After the first eight clock pulses, the MSB is applied to U3-D1 input via U1-QS output. The ninth clock pulse places the MSB at U3-Q1 output and U3-D2 input. After the ninth clock pulse, the strobe line goes high, and the 1/8 dB bit through the 16 dB bit appears at U1-Q1 through Q8. The 32 dB bit appears at U3-Q2. The strobe line then goes low, disabling any further changes. Note that a '0' at the data input is interpreted as a request to select attenuation and a '1' as a request to remove attenuation.

U1-Q7, Q8, and U3-Q2 contain the 8, 16, and 32 dB bits, respectively. These bits are applied through signal buffer/inverter U6 to PIN diode drivers U7 and U8. The table on sheet 2 of the schematic lists the three DCA states as a function of U6 inputs. U7 and U8 provide the appropriate dc voltage levels to reverse bias the diodes and turn them off, and the necessary forward bias current to provide a low resistance to the RF signal when they are on.

U1-Q1 through Q6 outputs are applied to PROM decoder U2. U2 converts the six-bit word into an eight-bit word for digital to analog (D/A) converter U4. The binary data represents ACA values of 1/8, 1/4, 1/2, 1, 2, or 4 dB or sums of 2 or more values. U4, in turn, generates a proportional current for PIN diodes CR3 and CR4 to produce the attenuation requested. Operational amplifier U5A then converts this current into a voltage level. U5A output voltage can be determined according to the following formula:

$$V_{out}\,(U5A) = (-V_{ref}) \times \frac{\text{decimal value of binary word at U4-B1 through B8}}{256}$$

For example, if Vref = 8.0 Vdc and U2 output at U4 B1-B8 is:

B_1	B_2	B_3	B_4	B_5	B_6	B_7	B_8
1	0	1	1	0	1	1	1
MSB							LSB

Then: $10110111_2 = (128 + 32 + 16 + 4 + 2 + 1)_{10} = 183_{10}$

and V_{out} = -(8.0 Vdc) x $\frac{183}{256}$ = -5.718 Vdc

V_{ref} (+) is derived from voltage regulator U10, and is processed by (+) reference amplifier stage U5B to be nominally + 8.0 Vdc at U5B output. This voltage is used as the reference voltage for D/A converter U4. It is also applied to op amp U5D to generate a second reference voltage V_{ref}(-), which is equal in value to V_{ref}(+) but opposite in polarity.

U5A output ranges from V_{ref}(-) to 0 Vdc and is applied to one side of analog attenuation range adjust R7. The other side of R7 is connected to V_{ref}(-). A voltage will therefore be developed across R7 which is a function of the desired attenuation step requested. R7 scales this voltage and applies it to a precision current source comprised of U5C and Q1, which in turn supplies control current to PIN diodes CR3 and CR4. The resistance of CR3 and CR4 decreases, ie, attenuation increases, as the current through them is increased. R7 is factory adjusted to set the current range required by CR3 and CR4 corresponding to an analog attenuation range of 0 to 7-7/8 dB.

Analog Attenuation Control temperature compensation is provided by thermistor R8 and Analog Attenuation Compensation Control Adjust R26. This compensation network tracks and cancels the temperature induced effects due to PIN diodes CR3 and CR4. As the diodes ambient temperature increases, their attenuation value decreases. R8, however, will increase V_{ref}, which causes a larger voltage across R7 to develop. This results in a larger voltage drop across R5 so Q1 conducts more current through CR3 and CR4. When this happens, the diode's attenuation value increases back to the desired level. R26 is factory set to change the sensitivity of the temperature compensation, thereby tailoring the degree of compensation to any given diodes.

4. MAINTENANCE

The following adjustments should not be performed as routine maintenance procedures, but only when a PWB failure and subsequent repair indicates a definite need to realign the assembly outside the factory. (Note that all PWBs are purchased factory aligned.) The following assumptions are made:

a. The assembly is securely fastened to a chassis or similar test fixture; in particular Q5 is properly connected to a heatsink.

b. The assembly is configured for either low or high gain mode, per instructions on schematic diagram, figure 9. (Note that if high-gain mode is selected, a 50 ohm, 6 dB pad should be inserted in-line between J2 and J4 to simulate the insertion loss introduced by a postselector).

c. Figure 4 shows the circuit used to supply RF input power.

d. A serial data generator (SDG) test fixture or an analog attenuator switching network is available. If a serial data generator is not available, an analog attenuator switching network (AASN) may be fabricated (figure 5) and used in its place.

4.1 Analog Attenuator Adjustments

a. Set signal source output level to + 6 dBm (into 50 ohms) at 30 MHz.

b. Set R7 (Analog Attenuation Range Adjust) and R26 (Analog Attenuator Temperature Compensation Adjust) fully clockwise (cw).

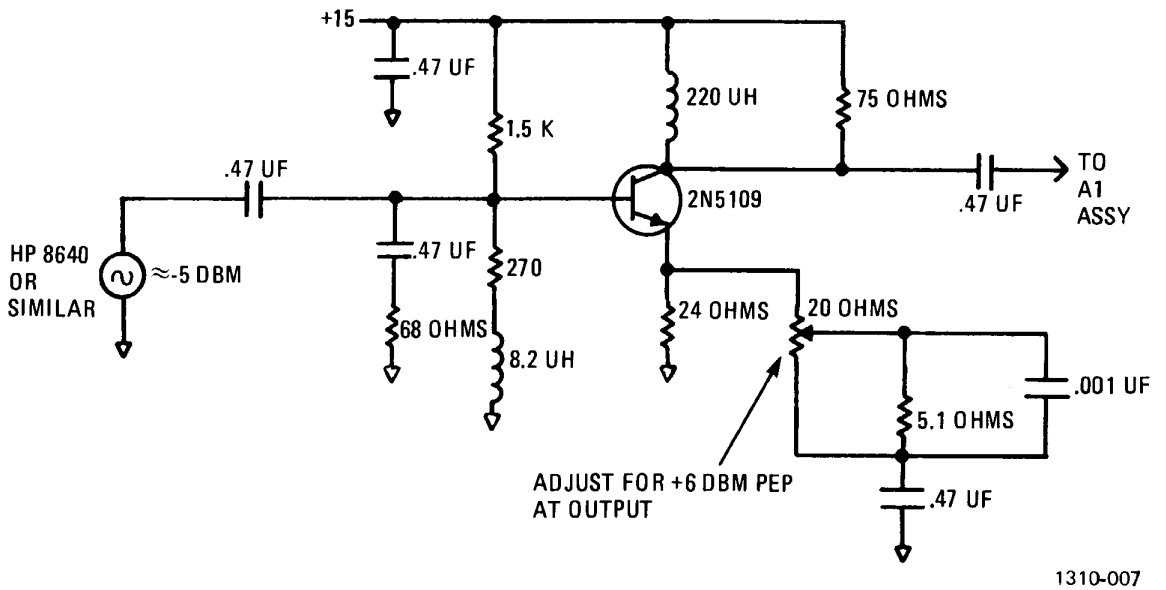


Figure 4. RF Signal Source

CAUTION

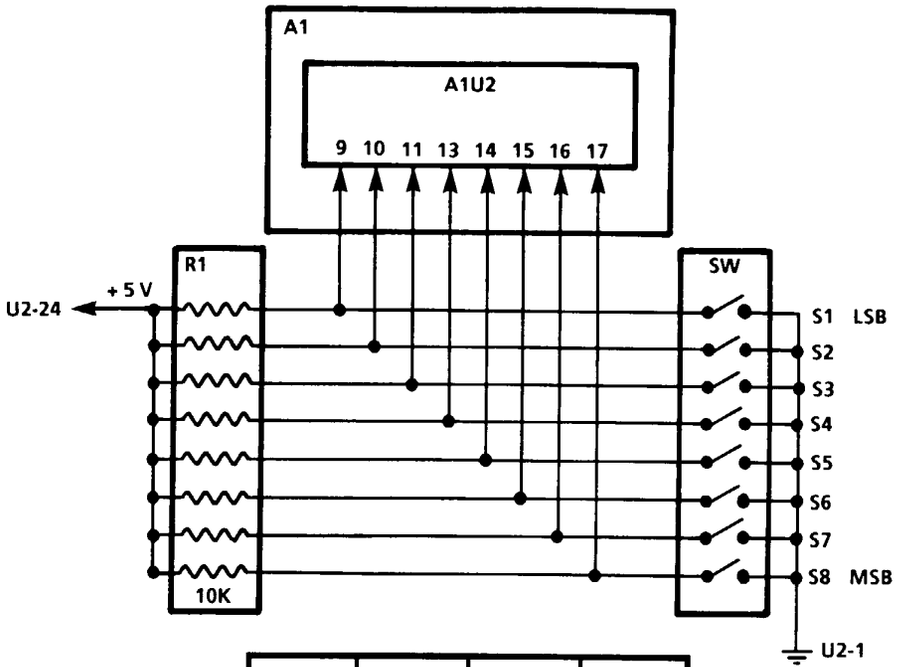
A1U2 is a static sensitive device. Precautionary measures must be taken to protect the device from static damage prior to performing the next step.

c. If a serial data generator is available, connect equipment as shown in figure 6. If an analog attenuator switching network (AASN) is to be used, and assuming that it has been fabricated per figure 5, carefully remove A1U2 from its socket. Refer to figure 7. Connect the AASN to the appropriate pins of the U2 socket as shown and connect the remaining test equipment. Allow the A1 assembly to operate for three minutes before proceeding.

d. Set serial data generator (SDG) or AASN to 0 dBm attenuation. Output level should be approximately + 21 to + 25 dBm.

e. Set SDG or AASN to 7-7/8 dB attenuation. Adjust R7 counterclockwise (ccw) for 11.5 dBm ± 0.05 dB. (Use RF voltmeter 10 dBm range for all readings around 11.5 dBm.)

f. Set SDG or AASN to 0 dB attenuation. Readjust signal source input level to obtain + 20 dBm ± 0.05 dB at output.



SW	0 dB	4 dB	7 7/8 dB
LSB S1	C	O	O
S2	O	O	C
S3	C	C	C
S4	C	C	O
S5	O	C	C
S6	O	C	O
S7	O	O	O
MSB S8	O	O	C

C = SWITCH POSITION CLOSED
O = SWITCH POSITION OPEN

PARTS REQUIRED FOR MANUFACTURE OF ANALOG ATTENUATOR SWITCHING NETWORK

QTY.	DESIG.	DESCRIPTION	HARRIS Part No.
1	SW	Switch, 8 Section, SPST DIP (or equivalent)	S50-0001-008
1	R1	Resistor, 10K 10SIP (or equivalent)	R50-0010-103

1310-120

Figure 5. Analog Attenuator Switching Network Fabrication Information

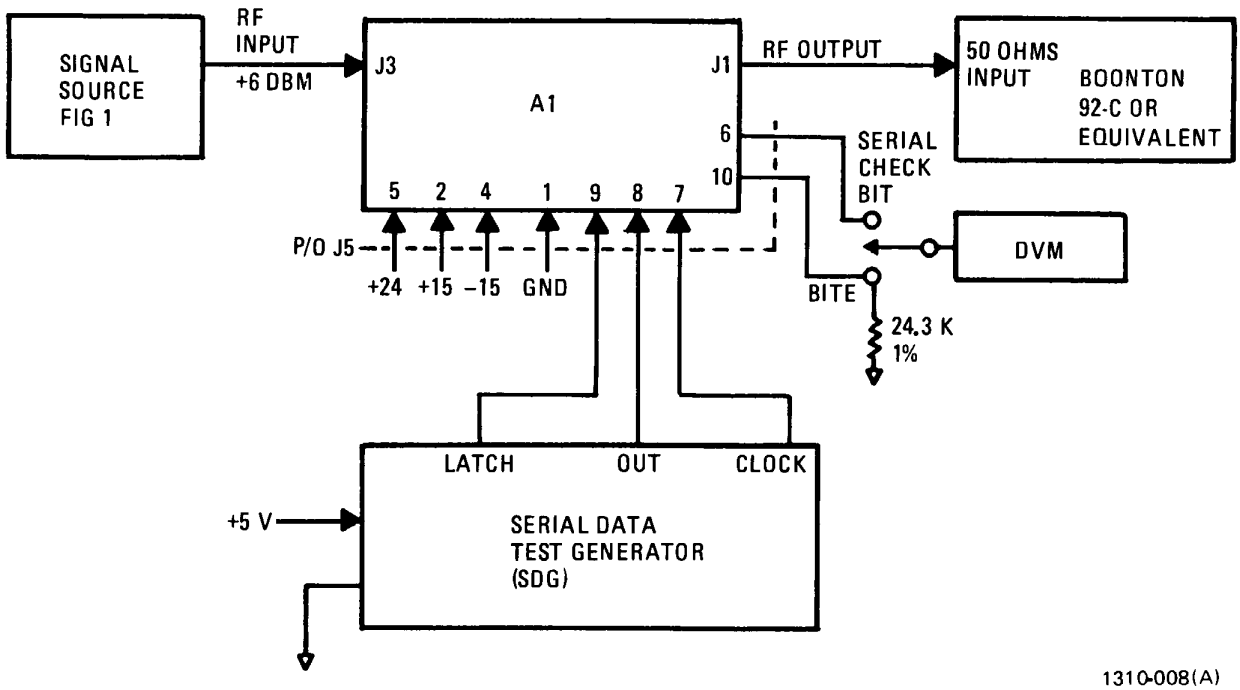


Figure 6. Output Amplifier Assembly Test Setup with a Serial Data test Generator (SDG)

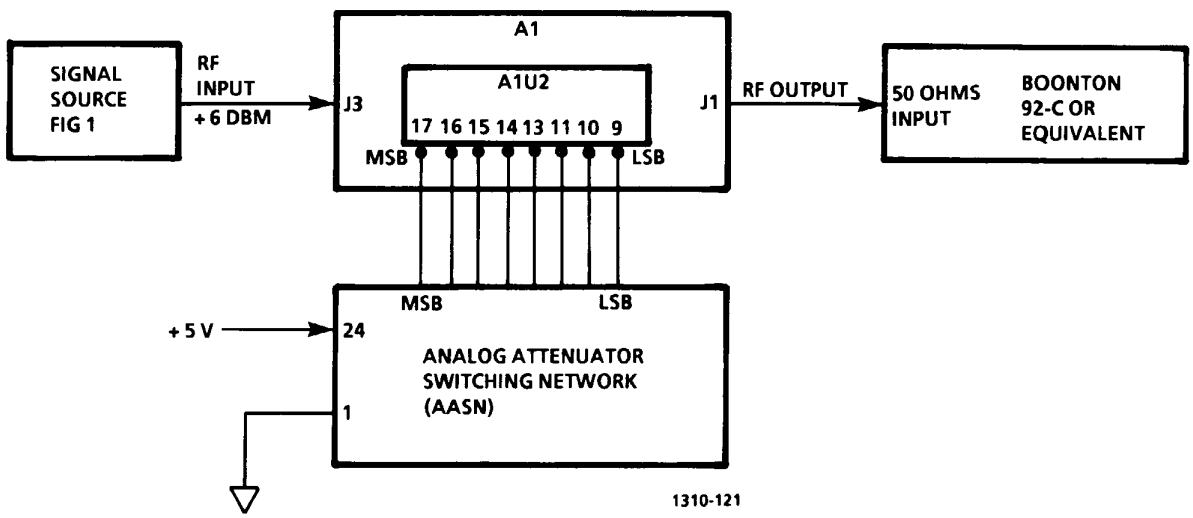


Figure 7. Alternate Output Amplifier Assembly test setup with an Analog Attenuator Switching Network (AASN)

g. Repeat steps e and f until:

1. The RF output is + 20 dBm ± 0.05 dB at 0 dB SDG or AASN setting.

and

2. The RF output is + 11.5 dBm ± 0.05 dB at 7-7/8 dB SDG or AASN setting.

h. Set SDG or AASN to 7-7/8 dB attenuation. Apply a forced-air heat source to the general area around which CR3, CR4, and thermistor R8 are located. Using a thermocoupled DVM (Fluke 2176A or equivalent), monitor the area and warm to approximately 60° C (near their surface) for at least 1 minute. (Note that steps i-l require that these components be maintained at the 60° C ambient temperature).

i. Adjust R26 to return the RF output level to 11.5 dBm.

j. Set the SDG or AASN to 0 dB attenuation. Readjust signal source input level to maintain + 20 dBm ± .05 dB RF output.

k. Set the SDG or AASN to 7-7/8 dB attenuation. Adjust R26 to return the RF output level to 11.5 dBm.

l. Repeat steps j and k until:

1. The RF output is + 20 dBm ± .05 dB at 0 dB SDG or AASN setting.

2. The RF output is 11.5 dBm ± .1 dB at 7-7/8 dB SDG or AASN setting.

m. Verify frequency response as follows:

1. Set signal source to + 6 dBm (into 50 ohm) at 30 MHz.

2. Set SDG or AASN to 0 dB, note level. Verify RF output is + 20 dBm (+ 2, -1 dBm).

3. Set SDG or AASN to 4 dB. Verify RF output is in the range of 4 to 5.25 dB below level noted in 2.

4. Set SDG or AASN to 7-7/8 dB. Verify RF output is in the range of 8.1 to 10 dB below level noted in 2.

5. Repeat steps 1-4 at 10 and .5 MHz.

n. Test is completed.

4.2 Digital Attenuator Verification

a. If a serial data generator is to be used, connect equipment as shown in figure 6. If the AASN was used for the analog attenuator alignment, disconnect the AASN from the U2 socket and carefully reinsert A1U2. If an SDG is not available, the RF power level adjustment can be set on the front panel by pressing the RF POWER control and entering the desired attenuation via the keypad.

b. Set SDG to -8, and adjust R24 to obtain a + 12 dBm RF output level.

c. Set SDG to -16, and adjust R27 to obtain a + 4 dBm RF output level.

d. Set SDG to -32, and adjust R29 to obtain a -12 dBm RF output level.

e. Set signal source level to obtain a + 20 dBm RF output at 10 MHz.

f. Set SDG to -8, -16, then -32 dB. Verify that the output level falls to 12, 4, and -12 dBm (respectively), ± 5%.

g. Repeat steps e. and f. at 0.5 MHz.

h. Test is completed.

4.3 Bite Verification

NOTE

The AASN should not be connected for this test.

a. Connect equipment as shown in figure 5. Set SDG to 0 dB. If a serial data test generator (SDG) is not available, the 0 dBm setting can be set via the front panel RF power level adjustment. Set signal source to obtain + 20 dBm RF at 10 MHz.

b. Adjust R43 until the BITE output measures 1.2 Vdc.

c. Serial data test BITE should be 0. Set SDG to 1/8 dB. Serial data test BITE should now be + 5 Vdc.

NOTE

Serial data test BITE cannot be performed without an SDG. However, the serial data test BITE line is checked automatically when running the exciter BITE routine.

d. Test is completed.

5. PARTS LIST, COMPONENT LOCATIONS, AND SCHEMATIC DIAGRAM

All replaceable components of the A1 assembly are listed in table 2. Table 3 lists the parts substitutions for the 10121-5100-02, Output Amplifier Assembly A1 with optional postselector. Component Locations are shown in figure 8. The Output Amplifier circuit is shown in figure 9.

Table 2. Output Amplifier Assembly A1 Parts List (Low Gain Option) (10121-5100-01 Rev. A)

Ref. Desig.	Part Number	Description
C1	CM05ED270J03	CAP 27PF 5% 500V MICA
C2	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C3	CM05FD161J03	CAP 160PF 5% 500V MICA
C4	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C5	M39014/01-1307V	CAP 270PF 10% 200V CER-R
C6	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C7	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C8	M39014/01-1287V	CAP 22PF 10% 200V CER-R
C9	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C10	M39014/02-1320V	CAP .47UF 10% 50V CER-R

Table 2. Output Amplifier Assembly A1 Parts List (Low Gain Option) (10121-5100-01 Rev. A) (Cont.)

Ref. Desig.	Part Number	Description
C11	M39014/02-1320V	CAP .47UF 10% 50V CER-R
C12	M39014/02-1298V	CAP .01UF 10% 200V CER-R
C13	M39014/02-1320V	CAP .47UF 10% 50V CER-R
C14	M39014/02-1320V	CAP .47UF 10% 50V CER-R
C15	C26-0035-100	CAP 10UF 20% 35V TANT
C16	CM05ED750J03	CAP 75PF 5% 500V MICA
C17	C26-0025-100	CAP 10UF 20% 25V TANT
C18	M39014/02-1320V	CAP .47UF 10% 50V CER-R
C19	M39014/02-1320V	CAP .47UF 10% 50V CER-R
C20	M39014/02-1320V	CAP .47UF 10% 50V CER-R
C21	CM05ED470J03	CAP 47PF 5% 500V MICA
C22	CM05ED620J03	CAP 62PF 5% 500V MICA
C23	CM05FD101J03	CAP 100PF 5% 500V MICA
C24	CM05ED820J03	CAP 82PF 5% 500V MICA
C25	CM05FD121J03	CAP 120PF 5% 500V MICA
C26	CM05CD150J03	CAP 15PF 5% 500V MICA
C27	CM05ED820J03	CAP 82PF 5% 500V MICA
C28	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C29	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C30	M39014/02-1320V	CAP .47UF 10% 50V CER-R
C31	M39014/02-1320V	CAP .47UF 10% 50V CER-R
C32	M39014/02-1320V	CAP .47UF 10% 50V CER-R
C33	M39014/02-1320V	CAP .47UF 10% 50V CER-R
C34	C26-0025-100	CAP 10UF 20% 25V TANT
C35	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C36	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C37	M39014/02-1298V	CAP .01UF 10% 200V CER-R
C38	M39014/02-1320V	CAP .47UF 10% 50V CER-R
C39	M39014/02-1320V	CAP .47UF 10% 50V CER-R
C40	M39014/02-1320V	CAP .47UF 10% 50V CER-R
C41	M39014/02-1320V	CAP .47UF 10% 50V CER-R
C42	M39014/02-1320V	CAP .47UF 10% 50V CER-R
C43	M39014/02-1320V	CAP .47UF 10% 50V CER-R
C44	M39014/02-1320V	CAP .47UF 10% 50V CER-R
C45	M39014/02-1320V	CAP .47UF 10% 50V CER-R
C46	M39014/02-1320V	CAP .47UF 10% 50V CER-R
C47	M39014/02-1320V	CAP .47UF 10% 50V CER-R
C48	M39014/02-1320V	CAP .47UF 10% 50V CER-R
C49	M39014/02-1320V	CAP .47UF 10% 50V CER-R
C50	M39014/02-1298V	CAP .01UF 10% 200V CER-R
C51	M39014/01-1281V	CAP 10PF 10% 200V CER-R
C52	M39014/01-1287V	CAP 22PF 10% 200V CER-R
C53	M39014/02-1298V	CAP .01UF 10% 200V CER-R
C54	M39014/02-1298V	CAP .01UF 10% 200V CER-R

Table 2. Output Amplifier Assembly A1 Parts List (Low Gain Option) (10121-5100-01 Rev. A) (Cont.)

Ref. Desig.	Part Number	Description
CR1	1N6263	DIODE .40W 60V HOT CARR
CR2	1N4454	DIODE 200MA 75V SW
CR3	D12-0007-001	DIODE PIN ATTN 1W 9301
CR4	D12-0007-001	DIODE PIN ATTN 1W 9301
CR5	D12-0008-001	DIODE PIN SW 2.5W 1001
CR6	D12-0008-001	DIODE PIN SW 2.5W 1001
CR7	D12-0008-001	DIODE PIN SW 2.5W 1001
CR8	D12-0008-001	DIODE PIN SW 2.5W 1001
CR9	D12-0008-001	DIODE PIN SW 2.5W 1001
CR10	D12-0008-001	DIODE PIN SW 2.5W 1001
CR11	D12-0008-001	DIODE PIN SW 2.5W 1001
CR12	D12-0008-001	DIODE PIN SW 2.5W 1001
CR13	1N6263	DIODE .40W 60V HOT CARR
CR14	1N6263	DIODE .40W 60V HOT CARR
E3	L50-0001-003	CORE SOFT FERRITE
J1	J-0031	CONN SMB VERT PCB F
J2	J-0031	CONN SMB VERT PCB F
J3	J90-0014-001	CONN SMB VERT PCB MT M
J4	J-0031	CONN SMB VERT PCB F
J5	J46-0032-010	HDR 10 PIN 0.100" SR
L1	MS75085-16	COIL 560UH 10% FXD RF
L2	MS75083-11	COIL .68UH 10% FXD RF
L3	82027-03	CHOKE WB 50MHZ
L4	MS75083-1	COIL .10UH 10% FXD RF
L5	10121-5104	INDUCTOR
L6	MS75085-16	COIL 560UH 10% FXD RF
L7	10121-7001	INDUCTOR .181UH
L8	10121-7002	INDUCTOR .174UH
L9	10121-7003	INDUCTOR .279UH
L10	82027-03	CHOKE WB 50MHZ
L11	MS75085-16	COIL 560UH 10% FXD RF
L12	MS75083-5	COIL .22UH 10% FXD RF
L13	10121-5105	INDUCTOR
L14	MS75085-16	COIL 560UH 10% FXD RF
L15	MS75085-16	COIL 560UH 10% FXD RF
L16	MS75085-16	COIL 560UH 10% FXD RF
L17	MS75085-16	COIL 560UH 10% FXD RF
L18	MS75085-16	COIL 560UH 10% FXD RF
L19	MS75085-16	COIL 560UH 10% FXD RF
L20	MS75084-6	COIL 3.3UH 10% FXD RF
L21	82027-03	CHOKE WB 50MHZ
Q1	2N2222A	XSTR SS/GP NPN TO-18

Table 2. Output Amplifier Assembly A1 Parts List (Low Gain Option) (10121-5100-01 Rev. A) (Cont.)

Ref. Desig.	Part Number	Description
Q2	2N2907A	XSTR SS/GP PNP TO-18
Q3	Q35-0003-000	XSTR N-CH JFET U310
Q4	Q25-0014-000	XSTR RF VHF 4W MRF237
Q5	Q25-0016-000	XSTR RF VHF 8W MRF340
R1	RN55D2001F	RES 2000 1% 1/8W MET FLM
R2	RN55D1002F	RES 10.0K 1% 1/8W MET FLM
R3	R65-0003-221	RES 220 5% 1/4W CAR FILM
R4	R65-0003-222	RES 2.2K 5% 1/4W CAR FILM
R5	RN55D1000F	RES 100 1% 1/8W MET FLM
R6	R65-0003-222	RES 2.2K 5% 1/4W CAR FILM
R7	R30-0008-502	RES VAR PCB 5K 1/2W 10%
R8	D40-0004-004	THERM 2K 5% @ 25DEG
R9	R53-0002-103	RES 10K .5% 14DIP 7RES
R10	R65-0003-309	RES 3.0 5% 1/4W CAR FILM
R11	RN55D30R1F	RES 30.1 1% 1/8W MET FLM
R12	R65-0003-309	RES 3.0 5% 1/4W CAR FILM
R13	RN55D1002F	RES 10.0K 1% 1/8W MET FLM
R16	R65-0003-130	RES 13 5% 1/4W CAR FILM
R17	R65-0003-750	RES 75 5% 1/4W CAR FILM
R18	R65-0003-430	RES 43 5% 1/4W CAR FILM
R19	R65-0003-101	RES 100 5% 1/4W CAR FILM
R20	R65-0003-331	RES 330 5% 1/4W CAR FILM
R21	RCR32G6R8JM	RES 6.8 5% 1W CAR COMP
R22	R50-0008-680	RES 68 2% 8SIP 7RES
R23	R50-0008-101	RES 100 2% 8SIP 7RES
R24	R30-0008-101	RES VAR PCB 10 1/2W 20%
R25	R51-0008-101	RES 100 2% 8SIP 4RES
R26	R30-0008-104	RES VAR PCB 100K 1/2W 10%
R27	R30-0008-500	POT,MULTI-TURN,50OHM2%1/2
R28	R65-0003-100	RES 10 5% 1/4W CAR FILM
R29	R30-0008-202	RES VAR PCB 2K 1/2W 10%
R30	R65-0003-121	RES 120 5% 1/4W CAR FILM
R31	R51-0006-330	RES 33 2% 6SIP 3RES
R32	R51-0008-151	RES 150 2% 8SIP 4RES
R33	R50-0006-104	RES 100K 2% 6SIP 5RES
R34	R65-0003-910	RES 91 5% 1/4W CAR FILM
R35	R50-0006-202	RES 2K 2% 6SIP 5RES
R36	R50-0006-202	RES 2K 2% 6SIP 5RES
R37	R65-0003-271	RES 270 5% 1/4W CAR FILM
R38	R65-0003-101	RES 100 5% 1/4W CAR FILM
R40	R65-0003-105	RES 1.0M 5% 1/4W CAR FILM
R41	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM

Table 2. Output Amplifier Assembly A1 Parts List (Low Gain Option) (10121-5100-01 Rev. A) (Cont.)

Ref. Desig.	Part Number	Description
R42	R65-0003-221	RES 220 5% 1/4W CAR FILM
R43	R30-0008-503	RES VAR PCB 50K 1/2W 10%
U1	I01-0000-156	IC 4094B PLASTIC CMOS
U2	10121-8201	KIT SOFTWARE
U3	I01-0000-050	IC 4013B PLASTIC CMOS
U4	I03-0012-000	IC 7523 D/A CONV 8BIT PLA
U5	I30-0003-000	IC OP AMP QUAD 324
U6	I01-0000-018	IC 4049UB PLASTIC CMOS
U7	I35-0009-000	IC MEM/CLK DRVR 75365
U8	I35-0009-000	IC MEM/CLK DRVR 75365
U9	I90-0001-000	IC XSTR ARRAY 3083
U10	I12-0006-008	IC VR 78L08A +8V .10A 4%
U11	I11-0001-001	IC VR 7805 +5V 1.5A 4%
XU2	J77-0008-005	SKT IC MACH 24 PIN

NOTE

The part number for U2 is 10121-8XXX-X where XXX-X is the four-character software kit code found on the PROM label. For example, if the code is 501C, the part number for the programmed PROM is 10121-8501C.

Table 3. Output Amplifier Assembly A1 High Gain Option Parts Substitutions (10121-5100-02 Rev. D)

Ref. Desig.	Part Number	Description
R14	R65-0003-430	RES, 43 OHMS, 5%, 1/4 W, CAR FILM
R15	R65-0003-110	RES, 11 OHMS, 5%, 1/4 W, CAR FILM
R38		NOT USED
R39	R65-0003-241	RES, 240 OHMS, 5%, 1/4 W, CAR FILM

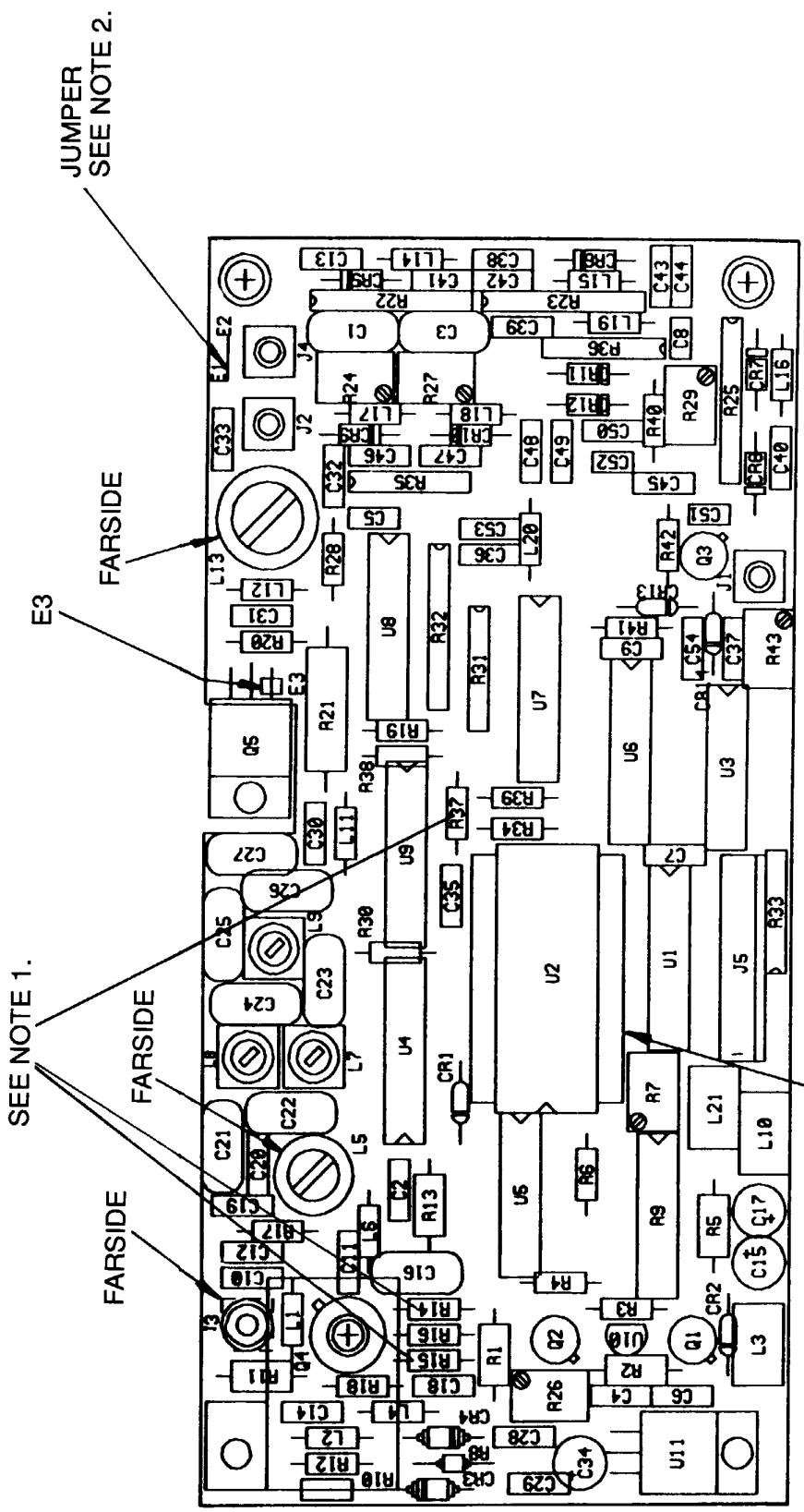


Figure 8. Output Amplifier Assembly A1 Component Location Diagram (10121-5100 Rev. H)

NOTES:

1. R14, R15 AND R39 ARE REMOVED FOR 10121-5100-01 LOW GAIN OPTION.
2. R38 AND E1 TO E2 JUMPER ARE REMOVED FOR 10121-5100-02 HIGH GAIN OPTION.

NOTE: UNLESS OTHERWISE SPECIFIED:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR A COMPLETE DESIGNATION, PREFIX WITH UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.
2. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, ±5%.
3. ALL CAPACITOR VALUES ARE IN MICROFARADS.
4. ALL INDUCTOR VALUES ARE IN MICROHENRIES.
5. VENDOR PART NO. CALLOUTS ARE FOR REFERENCE ONLY. COMPONENTS ARE SUPPLIED PER PART NO. IN PARTS LIST.

6.

	FOR ASSEMBLY 10121-5100-02 (WITH POST SELECTOR OPERATION)	FOR ASSEMBLY 10121-5100-01 (WITHOUT POST SELECTOR OPERATION)
R14	IN CIRCUIT	REMOVE
R15	IN CIRCUIT	REMOVE
R38	REMOVE	IN CIRCUIT
R39	IN CIRCUIT	REMOVE
E1-E2 JUMPER	REMOVE	IN CIRCUIT
J2	CONNECT TO POST SELECTOR INPUT	NOT USED
J4	CONNECT TO POST SELECTOR OUTPUT	NOT USED
Q4 GAIN	≈14 dB	≈8 dB

7. ALL VOLTAGES AND SIGNAL LEVELS SHOWN ARE NOMINAL VALUES.

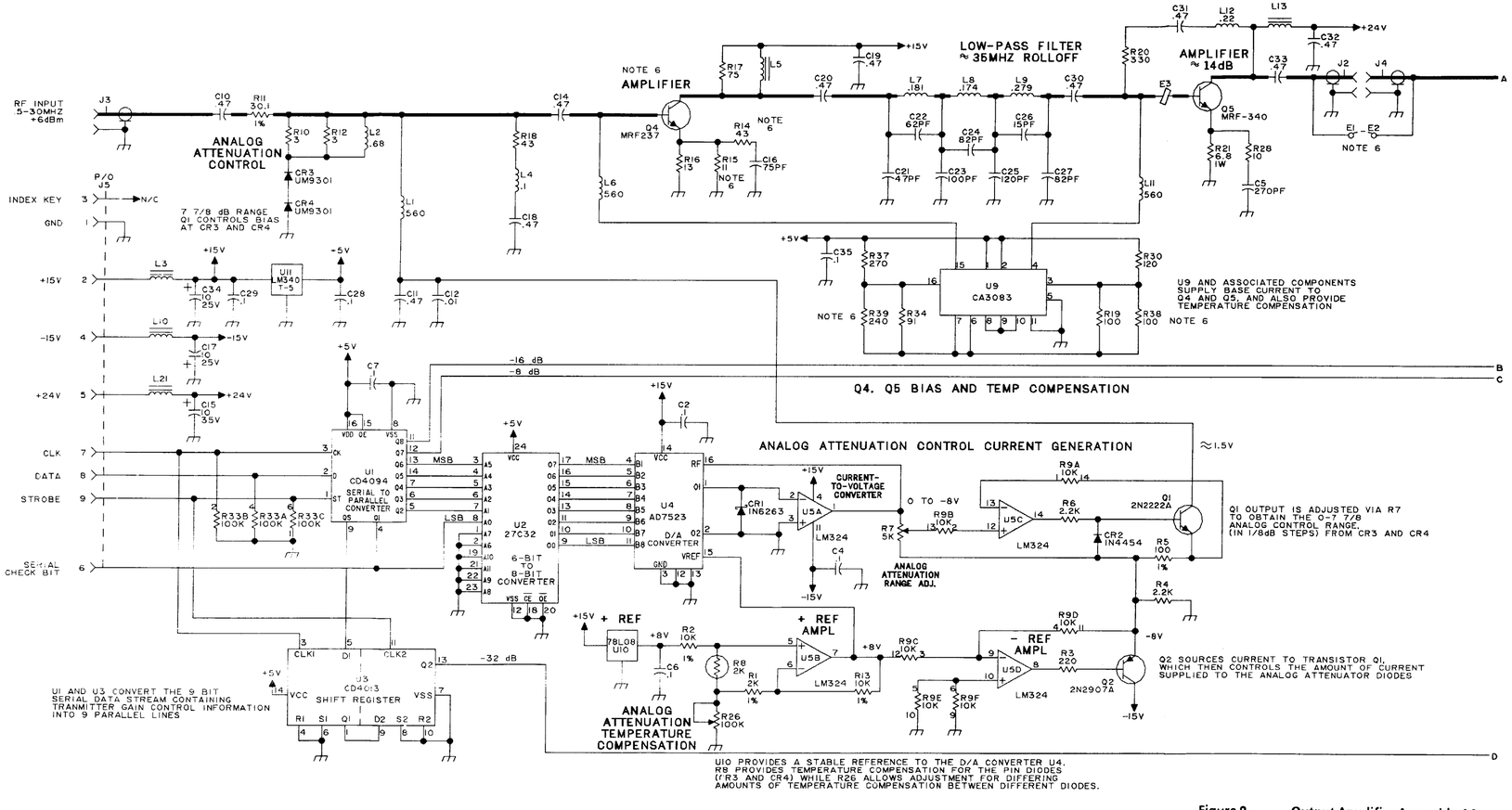


Figure 9. Output Amplifier Assembly A1 Schematic Diagram (10121-5101 Rev. D) (Sheet 1 of 2)

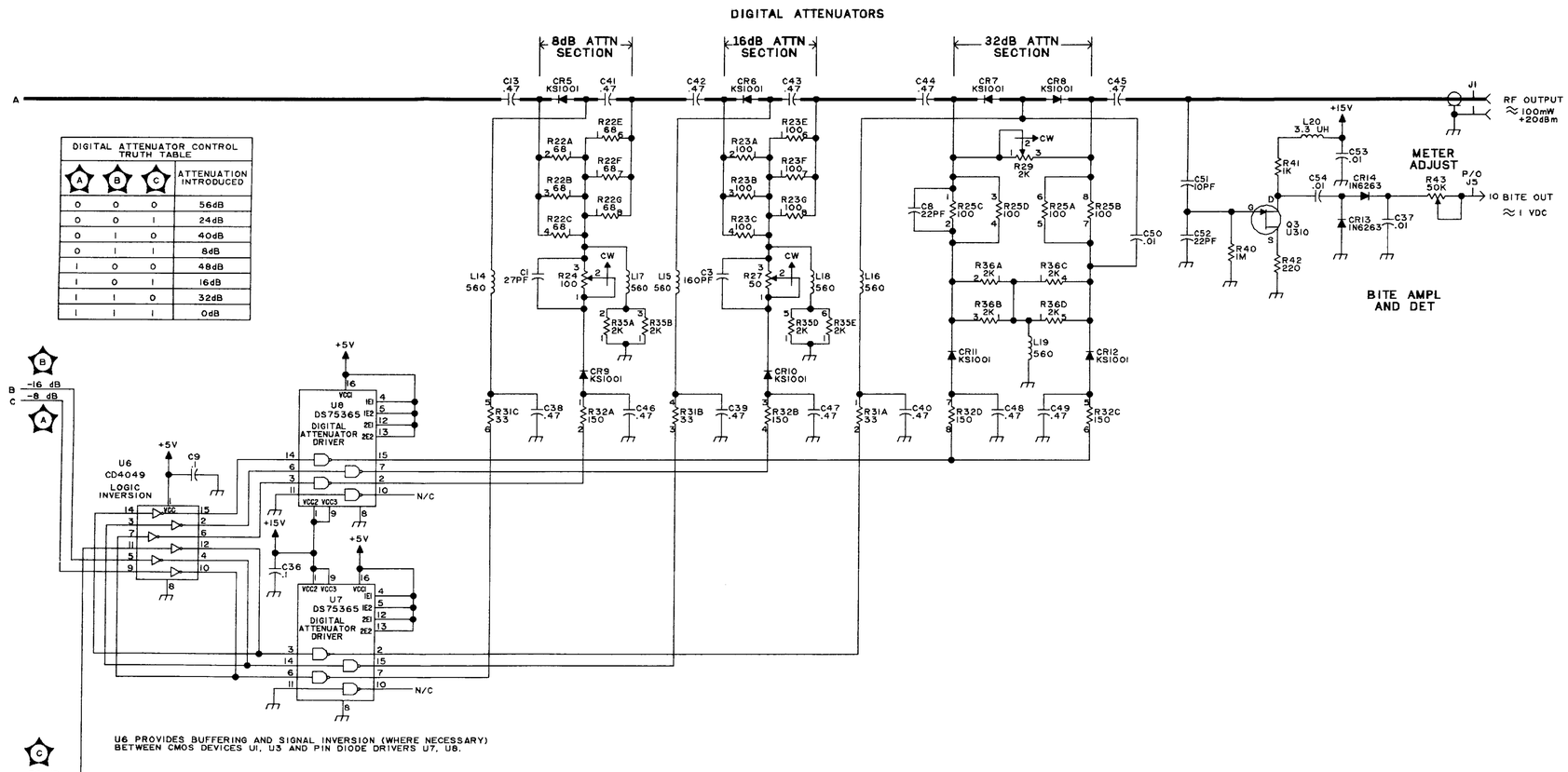
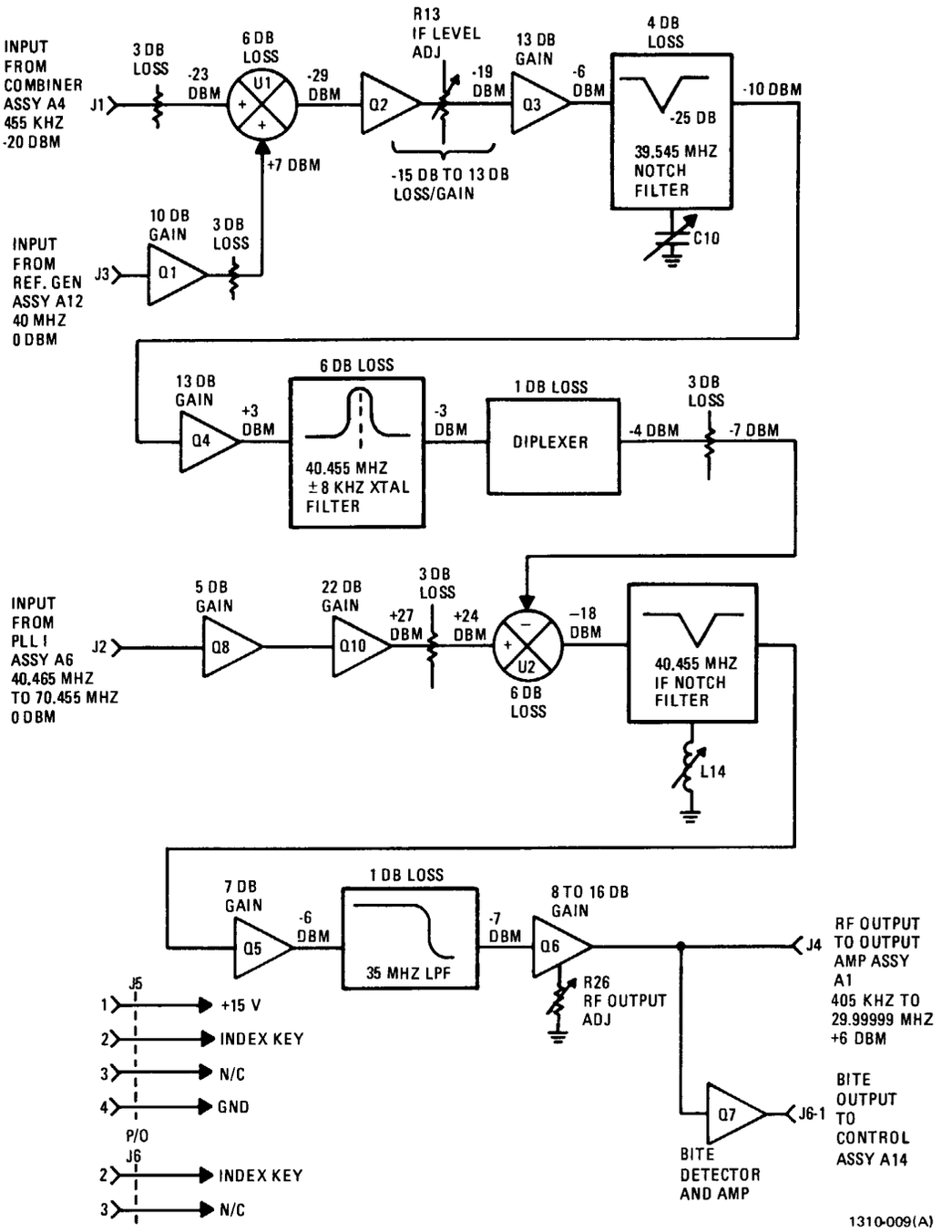


Figure 9. Output Amplifier Assembly A1 Schematic Diagram (10121-5101 Rev. D) (Sheet 2 of 2)

A2
CONVERTER ASSEMBLY



1310-009(A)

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CONVERTER ASSEMBLY A2

1. GENERAL DESCRIPTION

Converter Assembly A2 is a single PWB assembly and its position is shown in figure1. This assembly up converts the 455 kHz combiner output to an intermediate frequency (IF) of 40.455 MHz. This IF signal is then gain adjusted and processed by a 39.545 MHz notch and ± 8 kHz wide, 40.455 MHz filter to remove undesired mixing products. This processed signal is then down converted to an RF output signal in the range of 405 kHz to 29.99999 MHz. The exact output frequency is determined by the operating frequency of the variable local oscillator (LO) signal driving the down converter. This LO signal itself is a function of the operator-selected exciter output frequency.

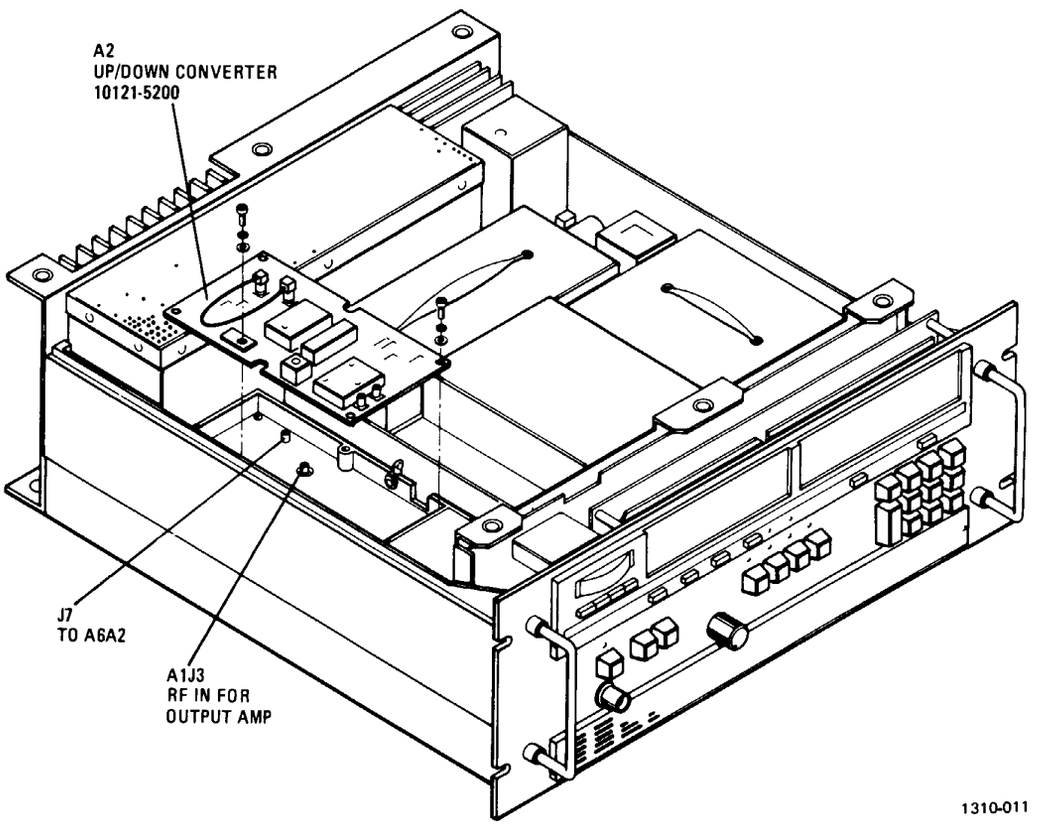


Figure 1. Converter Assembly A2 Location

Signal processing of the RF output band produces the following desired effects:

a. Removal of undesired down conversion-mixing products via the 40.455 MHz notch and the 35 MHz low pass filter (LPF)

b. Establishment of the exciter in-band noise characteristics via the low noise amplifier (LNA)

c. Amplification to a nominal PWB output level of + 6 dBm

The assembly itself is secured via four mounting screws and one heatsink plate screw. To remove assembly, remove all screws, RF and control connectors, and use the cable tie mounted through the PWB to pull the PWB away from a mating connector located under the PWB.

2. INTERFACE CONNECTIONS

Table 1 details the various input/output connections and other relevant data.

Table 1. Converter Assembly A2 Interface Connections

Connector	Function	Characteristics
J1	455 kHz Input	455 kHz information, -20 dBm PEP, 50 ohms
J2	Second LO Input	40.465 to 70.455 MHz, 0 dBm, 50 ohms
J3	First LO Input	40.000 MHz, 0 dBm, 50 ohms
J4	RF Output	405 kHz to 29.99999 MHz, + 6 dBm into 50 ohms
J5-1	Dc Power	+ 15 Vdc, approximately 550 mA
J5-2	Index Key	No connection
J5-3	Dc Power	+ 24 Vdc, no connection
J5-4	Ground	
J6-1	BITE Output	Approximately .5 to 1 Vdc for 6 dBm PEP Output
J6-2	Index Key	No connection
J6-3	Spare	No connection

3. CIRCUIT DESCRIPTION

3.1 40.455 MHz IF Chain

Up conversion of the 455 kHz information from the Combiner Assembly occurs at double balanced mixer U1. U1 has two inputs:

a. 455 kHz from the Combiner Assembly, padded by 3 dB (R9 through R11) to a -23 dBm level at the IF port.

b. 40.000000 MHz from the Reference Generator Assembly, amplified by Q1 to + 10 dBm and padded down by R6, R7, and R8 to + 7 dBm at the LO port.

U1 output is a double sideband (DSB) signal whose 40 MHz carrier is suppressed. The two sidebands are at a nominal level of -29 dBm (each) at frequencies of 40 MHz ± 455 kHz. The desired frequency is the 40.455 MHz product, and the undesired 39.545 MHz image frequency product will be removed in later processing stages.

This DSB signal is then amplified by Q2, whose output level to subsequent stages is set by IF Level Adjust R13 in order to produce a nominal -7 dBm 40.455 MHz signal to mixer U2. Q2 can provide up to + 13 dB of gain. Q2 output is nominally -19 dBm.

Note that Q2 and all preceding circuitry is shielded by top and bottom covers on the PWB. These covers prevent the 40 MHz LO and 39.545 MHz image frequencies from radiating, and must be properly secured with all mounting hardware. Metal finger-stocks located under FL1, prevent ground plane conduction around the filter by returning any signals on the PWB ground plane to chassis ground; they must be in place.

Q3 provides another + 13 dB of gain, resulting in a level of -6 dBm applied to an image trap consisting of 39.545 MHz crystal Y1 and associated circuitry. This highly selective narrow-band notch helps provide image rejection by shunting the image signal to ground.

Insertion loss of the trap is -4 dB, and is minimized by adjusting peaking capacitor C10 for a maximum output.

A -10 dBm signal from the image trap is fed to Q4, which amplifies the desired signal to + 3 dBm. Thermistor R20 provides temperature compensation for the 40.455 MHz IF chain by increasing the Q4 gain slightly as the temperature increases. 40.455 MHz crystal filter FL1 provides a nominal -65 dB rejection to undesired signals outside its ± 8 kHz bandwidth, with an inband insertion loss of 6 dB maximum.

A diplexer provides a constant 50-ohm termination at all frequencies for FL1 and down converter U2. The diplexer itself has 1 dB of inband insertion loss. The diplexer feeds a 3 dB pad (R53-R55), which provides a 40.455 MHz IF input signal to U2 with a nominal level of -7 dBm.

3.2 40.465 - 70.455 MHz LO Amplifier

40.465 - 70.455 MHz LO injection for U2 is supplied from PLL I Assembly to the Converter Assembly at J2 at 0 dBm. R36 and the low input impedance of common base stage Q8 provides a nominal 50-ohm match to the input signal. Q8 provides 5 dB of voltage gain from J2 to the T1 tap point at R42 (approximately 1.3 V_{pp}). Power amplifier Q10 supplies 22 dB of voltage gain from R42 to the output of T3, developing approximately 15 V_{pp} at the 3 dB pad (R49 - R51) input. The power level into this 50-ohm pad is nominally + 27 dBm, so that the U2 LO port is supplied with a signal level of approximately + 24 dBm.

Q9 and associated circuitry provide base current for Q10, resulting in a Q10 collector current of 300 mA. Diode CR1 provides thermal stabilization for Q9 base current. Resistor pair R46 and R47 form a series current sense circuit for the Q10 collector current. For example, if the Q10 collector current tends to increase, the voltage drop across R46 and R47 increases, and therefore emitter voltage at Q9 drops. This action drives Q9 towards cutoff, with a corresponding decrease in Q9 base and collector current. Since Q9 collector current is the same as the Q10 base current, the Q10 collector current will also decrease back towards its nominal value.

Note that although Q10 will easily withstand short operating periods during which it is not connected to the heatsink, it should normally be operated with the heatsink plate securely fastened to the chassis.

3.3 405 kHz to 29.99999 MHz

Double balanced mixer U2 down converts the 40.455 MHz information to the exciter output frequency range of 405 kHz to 29.99999 MHz. U2 is a very high level mixer (LO drive = 24 dBm) and provides a low distortion -13 dBm output at the RF port due to a -6 dB conversion loss. Like U1, U2 output contains the LO feed-through and image frequencies. These undesired products, however, are sufficiently removed in frequency from the desired .4 to 30 MHz band that they can be adequately filtered by low pass filters (LPF) on this assembly as well as the Output Amplifier Assembly.

Conversion spurious products are effectively controlled by:

a. The high quality characteristics of the mixer.

b. Shielding of the RF chain to prevent the 40.465 to 70.455 MHz high level LO from radiating into the RF chain.

c. The 40.455 MHz IF trap (L14, C27) at U2 output.

The RF output of the down converter is applied to LNA Q5 at a nominal level of -13 dBm. Q5 supplies a nominal 7 dB of gain, and should normally be operated with the RF chain shield cover and heatsink cup securely in place. Constant current source Q11 maintains Q5 drain current at 18 mA, while Q12 provides a degree of temperature compensation for Q11. Thermistor R30 provides temperature compensation for the RF chain signal level.

T4 transforms the LNA high impedance output to a lower impedance in order to drive the succeeding LPF. This LPF provides at least 25 dB attenuation to undesired signals outside its passband, with a -3 dB cutoff frequency of about 35 MHz. Passband insertion loss is less than 1 dB.

Output stage Q6 gain can be varied from 8 to 16 dB via RF output adjust R26, and is set in conjunction with R13 to provide a nominal + 6 dBm level at the PWB output. This signal is then fed via a chassis cutout hole and a mating connector directly to the RF Output Amplifier Assembly.

Note that RF output connector J4 is mounted under the PWB, and is not accessible from the top. In order to access this connector, you must:

a. Remove the PWB following the instructions listed at the end of the General Description section.

or

b. Remove all five mounting screws from the Output Amplifier Assembly as well as the Output Amplifier Assembly itself, and access J4 through the chassis cutout.

3.4 BITE Circuit

Built In Test Equipment (BITE) amplifier and detector stage Q7 monitors the RF output signal level, and produces a dc output voltage proportional to this level. C29/C30 sample the signal, Q7 amplifies it, and CR2, CR3, R35, and C34 convert it to a dc signal. The detector output is adjustable via R65 to accommodate the RF output signal levels required in various system applications of the Exciter.

This BITE level is monitored by the Control Board Assembly whenever the operator chooses to perform a BITE test. At that time, a CW signal is fed through preceding signal chain assemblies and a -20 dBm signal at 455 kHz is presented to J1. Assuming all Converter Assembly circuitry is functional and the RF output level has previously been set to + 6 dBm, a BITE level of at least .5 Vdc will appear at J6-1. The Control Board Assembly will recognize this as a valid level, and proceed to test other assemblies. If the BITE level is lower, indicating a possible A2 fault, an appropriate error message will appear on the exciter display.

4. MAINTENANCE

4.1 General Information

The following adjustments should not be performed as routine maintenance procedures, but only when a PWB failure and subsequent repair indicates a definite need to realign the assembly outside the factory. (Note that all PWBs are factory aligned prior to shipment.)

All tests described here assume the following:

a. The A2 assembly is securely mounted in the chassis with all mounting hardware and internal shield covers secured.

b. The A1 assembly has been removed to allow access to J4, the RF output connector.

c. The exciter itself is functional, and can supply:

1. + 15 Vdc power at J5
2. 40.465 to 70.455 MHz LO at 0 dBm
3. 40 MHz LO at 0 dBm
4. 455 kHz IF at -20 dBm

In order to supply the 455 kHz IF, the exciter must be set to Signal Generator mode as described in the System Interface Assembly A18 section of this manual.

4.2 Signal Path Alignment Procedure

a. Set Exciter operating frequency to 10 MHz, CW Mode, keyed.

b. Check that the 455 kHz signal level at J1 is -20 dBm and that the 40 MHz signal at J3 is 0dBm.

c. Set the RF Signal Generator (HP8640 or equivalent) to 50.455 MHz with 0 dBm output.

d. Connect equipment as shown in figure 1.

1. For steps e to i, the RF output measuring equipment may be either of the following:
   - A 50-ohm input RF voltmeter (Boonton 92C or equivalent)
   - A 50-ohm input spectrum analyzer (HP-8553B or equivalent)
2. For steps k to m, the specturm analyzer must be used.

e. Set L14 to midrange.

f. Set R13 (IF Level Adjust) and R26 (RF Output Adjust) fully clockwise (maximum output level).

NOTE

L18 and L19 are set to a specific setting at the factory. DO NOT attempt to adjust these components.

g. Adjust C10 (39.545 MHz Trap Adjust) for a peak output signal. For a -20 dBm input, the RF output should be approximately + 18 dBm.

h. Adjust R26 for a level 9 dBm lower than that noted in step g.

i. Adjust R13 for + 6 or 7 dBm output level. This provides -1 to 0 dBm to mixer U2. Do not exceed a + 7 dBm output at Q6.

j. Adjust the BITE voltage to maximum using R65. The output should be between 1.0 and 1.5 Vdc.

k. With the spectrum analyzer measuring the RF output, set the generator to 80.9 MHz with 0 dBm output.

l. Adjust the analyzer to 40.455 MHz.

m. Adjust L14 for null on the analyzer, less than -45 dBm.

j. Test is complete.

5. PARTS LIST, COMPONENT LOCATIONS, AND SCHEMATIC DIAGRAM

Parts used on Converter Assembly A2 are listed in table 2. The component locations are shown in figure 3. Figure 4 is the schematic diagram for the assembly.

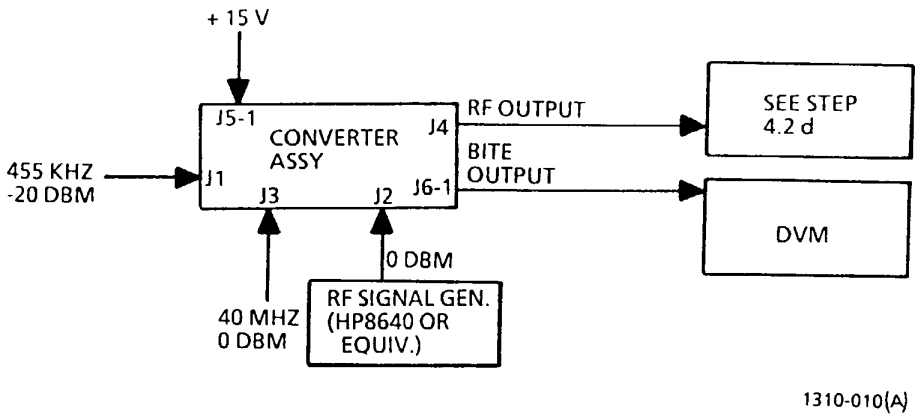


Figure 2. Signal Path Alignment

Table 2. Converter Assembly A2 Parts List (10121-5200 Rev. AD)

Ref. Desig.	Part Number	Description
C1	M39014/02-1298V	CAP .01UF 10% 200V CER-R
C2	M39014/02-1298V	CAP .01UF 10% 200V CER-R
C3	M39014/02-1298V	CAP .01UF 10% 200V CER-R
C4	M39014/02-1298V	CAP .01UF 10% 200V CER-R
C5	M39014/02-1298V	CAP .01UF 10% 200V CER-R
C6	M39014/02-1298V	CAP .01UF 10% 200V CER-R
C7	M39014/02-1298V	CAP .01UF 10% 200V CER-R
C8	M39014/02-1298V	CAP .01UF 10% 200V CER-R
C9	M39014/02-1298V	CAP .01UF 10% 200V CER-R
C10	C84-0003-008	CAP VAR 3-15PF CER
C11	M39014/02-1298V	CAP .01UF 10% 200V CER-R
C12	M39014/02-1298V	CAP .01UF 10% 200V CER-R
C13	M39014/02-1298V	CAP .01UF 10% 200V CER-R
C14	M39014/02-1298V	CAP .01UF 10% 200V CER-R
C15	M39014/02-1298V	CAP .01UF 10% 200V CER-R
C16	CM05CD150J03	CAP 15PF 5% 500V MICA
C17	CM05FD361J03	CAP 360PF 5% 500V MICA
C18	M39014/02-1320V	CAP .47UF 10% 50V CER-R

Table 2. Converter Assembly A2 Parts List (10121-5200 Rev. AD) (Cont.)

Ref. Desig.	Part Number	Description
C19	M39014/02-1320V	CAP .47UF 10% 50V CER-R
C20	M39014/02-1320V	CAP .47UF 10% 50V CER-R
C21	M39014/02-1298V	CAP .01UF 10% 200V CER-R
C22	M39014/02-1298V	CAP .01UF 10% 200V CER-R
C23	C26-0025-339	CAP 3.3UF 20% 25V TANT
C24	M39014/02-1298V	CAP .01UF 10% 200V CER-R
C25	M39014/02-1320V	CAP .47UF 10% 50V CER-R
C26	M39014/02-1320V	CAP .47UF 10% 50V CER-R
C27	CM05CD150J03	CAP 15PF 5% 500V MICA
C28	M39014/02-1320V	CAP .47UF 10% 50V CER-R
C29	CM04ED390J03	CAP 39PF 5% 500V MICA
C30	CM04CD050D03	CAP 5PF+-.5PF 500V MICA
C31	M39014/02-1298V	CAP .01UF 10% 200V CER-R
C32	M39014/02-1298V	CAP .01UF 10% 200V CER-R
C33	M39014/01-1535V	CAP .01UF 10% 100V CER-R
C34	M39014/02-1298V	CAP .01UF 10% 200V CER-R
C35	C26-0025-100	CAP 10UF 20% 25V TANT
C36	M39014/02-1298V	CAP .01UF 10% 200V CER-R
C37	M39014/02-1298V	CAP .01UF 10% 200V CER-R
C38	M39014/02-1298V	CAP .01UF 10% 200V CER-R
C39	C26-0025-339	CAP 3.3UF 20% 25V TANT
C40	M39014/02-1298V	CAP .01UF 10% 200V CER-R
C41	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C42	C26-0025-339	CAP 3.3UF 20% 25V TANT
C43	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C44	M39014/02-1298V	CAP .01UF 10% 200V CER-R
C45	M39014/02-1298V	CAP .01UF 10% 200V CER-R
C46	M39014/02-1298V	CAP .01UF 10% 200V CER-R
C47	C26-0025-339	CAP 3.3UF 20% 25V TANT
C48	M39014/02-1298V	CAP .01UF 10% 200V CER-R
C49	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C50	M39014/02-1298V	CAP .01UF 10% 200V CER-R
C51	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C52	C26-0025-339	CAP 3.3UF 20% 25V TANT
C53	CM05ED390J03	CAP 39PF 5% 500V MICA
C54	M39014/02-1298V	CAP .01UF 10% 200V CER-R
C55	CM05CD100D03	CAP 10PF+-.5PF 500V MICA
C56	CM05FD111J03	CAP 110PF 5% 500V MICA
C57	CM05FD121J03	CAP 120PF 5% 500V MICA
C58	CM05ED300J03	CAP 30PF 5% 500V MICA
C59	CM05ED430J03	CAP 43PF 5% 500V MICA
C60	M39014/02-1320V	CAP .47UF 10% 50V CER-R
C61	M39014/01-1317V	CAP,1000PF,10% 200VC

Table 2. Converter Assembly A2 Parts List (10121-5200 Rev. AD) (Cont.)

Ref. Desig.	Part Number	Description
C62	C26-0025-339	CAP 3.3UF 20% 25V TANT
C63	M39014/02-1310V	CAP .1UF 10% 100V CER-R
CR1	1N4454	DIODE 200MA 75V SW
CR2	1N6263	DIODE .40W 60V HOT CARR
CR3	1N6263	DIODE .40W 60V HOT CARR
CR4	1N5228B	DIODE 3.9V 5% .5W ZENER
E1	E-0650	BEAD, SHIELDING
FL1	10073-7000	FILTER,40.455 MHZ
J1	J-0031	CONN SMB VERT PCB F
J2	J-0031	CONN SMB VERT PCB F
J3	J-0031	CONN SMB VERT PCB F
J4	J-0031	CONN SMB VERT PCB F
J5	J46-0022-004	HDR 4 PIN 0.100" SR LKG
J6	J46-0022-003	HDR 3 PIN 0.100" SR LKG
L1	MS75084-14	COIL 15.0UH 10% FXD RF
L2	MS14046-4	COIL 10UH 10% FXD RF
L3	MS75084-12	COIL 10UH 10% FXD RF
L4	MS75084-3	COIL 1.8UH 10% FXD RF
L5	MS75084-3	COIL 1.8UH 10% FXD RF
L6	MS14046-4	COIL 10UH 10% FXD RF
L7	MS75084-12	COIL 10UH 10% FXD RF
L8	MS75084-12	COIL 10UH 10% FXD RF
L9	MS75083-13	COIL 1.0UH 10% FXD RF
L10	L05-0001-005	INDUCT MOLD .054 UH 5%
L11	MS90538-20	COIL 220UH 5% FXD RF
L12	MS90538-20	COIL 220UH 5% FXD RF
L13	MS90538-20	COIL 220UH 5% FXD RF
L14	L11-0004-013	INDUCT SH VAR .900-1.1 UH
L15	MS90538-20	COIL 220UH 5% FXD RF
L16	MS75083-13	COIL 1.0UH 10% FXD RF
L17	82027-03	CHOKE WB 50MHZ
L18	10121-7004	INDUCTOR .130UH
L19	10121-7005	INDUCTOR .247UH
L20	MS75084-12	COIL 10UH 10% FXD RF
L21	MS75083-1	COIL .10UH 10% FXD RF
L22	MS75084-12	COIL 10UH 10% FXD RF
L23	MS75084-11	COIL 8.2UH 10% FXD RF
Q1	2N5109	XSTR RF PWR NPN TO-39
Q2	2N5109	XSTR RF PWR NPN TO-39
Q3	2N5109	XSTR RF PWR NPN TO-39
Q4	Q10-0005-001	XSTR RF POWER NPN
Q5	Q35-0004-001	XSTR JFET U431
Q6	Q10-0005-001	XSTR RF POWER NPN
Q7	Q35-0003-000	XSTR N-CH JFET U310
Q8	2N3866	XSTR SS/RF NPN TO-39

Table 2. Converter Assembly A2 Parts List (10121-5200 Rev. AD) (Cont.)

Ref. Desig.	Part Number	Description
Q9	2N4037	XSTR SS/RF NPN TO-39
Q10	Q25-0014-000	XSTR RF VHF 4W MRF237
Q11	2N2222A	XSTR SS/GP NPN TO-18
Q12	2N2222A	XSTR SS/GP NPN TO-18
R1	R65-0003-162	RES 1.6K 5% 1/4W CAR FILM
R2	R65-0003-471	RES 470 5% 1/4W CAR FILM
R3	R65-0003-301	RES 300 5% 1/4W CAR FILM
R4	R65-0003-829	RES 8.2 5% 1/4W CAR FILM
R5	R65-0003-101	RES 100 5% 1/4W CAR FILM
R6	R65-0003-301	RES 300 5% 1/4W CAR FILM
R7	R65-0003-180	RES 18 5% 1/4W CAR FILM
R8	R65-0003-301	RES 300 5% 1/4W CAR FILM
R9	R65-0003-301	RES 300 5% 1/4W CAR FILM
R10	R65-0003-180	RES 18 5% 1/4W CAR FILM
R11	R65-0003-301	RES 300 5% 1/4W CAR FILM
R12	R65-0003-560	RES 56 5% 1/4W CAR FILM
R13	R-2203	RES VAR 100 10% .5W HOR.
R14	R65-0003-362	RES 3.6K 5% 1/4W CAR FILM
R15	R65-0003-112	RES 1.1K 5% 1/4W CAR FILM
R16	R65-0003-829	RES 8.2 5% 1/4W CAR FILM
R17	R65-0003-151	RES 150 5% 1/4W CAR FILM
R18	R65-0003-182	RES 1.8K 5% 1/4W CAR FILM
R19	R65-0003-621	RES 620 5% 1/4W CAR FILM
R20	D40-0004-002	THERM 510 5% @ 25DEG
R21	R65-0003-439	RES 4.352 1/4W 5%
R22	R65-0004-220	RES 22 5% 1/2W CAR FILM
R23	R65-0003-510	RES 51 5% 1/4W CAR FILM
R24	R65-0003-510	RES 51 5% 1/4W CAR FILM
R25	R65-0003-220	RES 22 5% 1/4W CAR FILM
R26	R-2202	RES VAR 50 10% .5W HOR.
R27	R65-0003-152	RES 1.5K 5% 1/4W CAR FILM
R28	R65-0003-471	RES 470 5% 1/4W CAR FILM
R29	R65-0004-270	RES 27 5% 1/2W CAR FILM
R30	D40-0004-003	THERM 1K 5% @ 25DEG
R31	R65-0003-750	RES 75 5% 1/4W CAR FILM
R32	R65-0003-473	RES 47K 5% 1/4W CAR FILM
R33	R65-0003-821	RES 820 5% 1/4W CAR FILM
R34	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R35	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R36	R65-0003-270	RES 27 5% 1/4W CAR FILM
R37	R65-0003-519	RES 5.1 5% 1/4W CAR FILM
R38	R65-0003-221	RES 220 5% 1/4W CAR FILM
R39	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM

Table 2. Converter Assembly A2 Parts List (10121-5200 Rev. AD) (Cont.)

Ref. Desig.	Part Number	Description
R40	R65-0003-272	RES 2.7K 5% 1/4W CAR FILM
R41	R65-0003-100	RES 10 5% 1/4W CAR FILM
R42	R65-0003-101	RES 100 5% 1/4W CAR FILM
R43	R65-0003-681	RES 680 5% 1/4W CAR FILM
R44	R65-0003-301	RES 300 5% 1/4W CAR FILM
R45	R65-0003-272	RES 2.7K 5% 1/4W CAR FILM
R46	RCR32G100JM	RES 10 5% 1W CAR COMP
R47	RCR32G100JM	RES 10 5% 1W CAR COMP
R48	R65-0003-201	RES 200 5% 1/4W CAR FILM
R49	R65-0003-301	RES 300 5% 1/4W CAR FILM
R50	R65-0004-180	RES 18 5% 1/2W CAR FILM
R51	R65-0003-301	RES 300 5% 1/4W CAR FILM
R52	R65-0003-680	RES 68 5% 1/4W CAR FILM
R53	R65-0003-301	RES 300 5% 1/4W CAR FILM
R54	R65-0003-180	RES 18 5% 1/4W CAR FILM
R55	R65-0003-301	RES 300 5% 1/4W CAR FILM
R56	R65-0003-222	RES 2.2K 5% 1/4W CAR FILM
R57	R65-0003-751	RES 750 5% 1/4W CAR FILM
R58	R65-0003-511	RES 510 5% 1/4W CAR FILM
R59	R65-0003-439	RES 4.352 1/4W 5%
R60	R65-0003-910	RES 91 5% 1/4W CAR FILM
R61	R65-0003-430	RES 43 5% 1/4W CAR FILM
R62	R65-0003-152	RES 1.5K 5% 1/4W CAR FILM
R63	R65-0003-680	RES 68 5% 1/4W CAR FILM
R64	R65-0003-162	RES 1.6K 5% 1/4W CAR FILM
R65	R30-0008-102	RES VAR PCB 1K 1/2W 10%
T1	10073-7005	TRANSFORMER, RF, FIXED
T2	10073-7005	TRANSFORMER, RF, FIXED
T3	10073-7010	TRANSFORMER, RF, FIXED
T4	10073-7010	TRANSFORMER, RF, FIXED
U1	I51-0003-003	MIXER DB SRA-1
U2	10075-0021	MIXER DB SRA-1H
Y1	10085-5425	CRYSTAL 39.545 MHZ

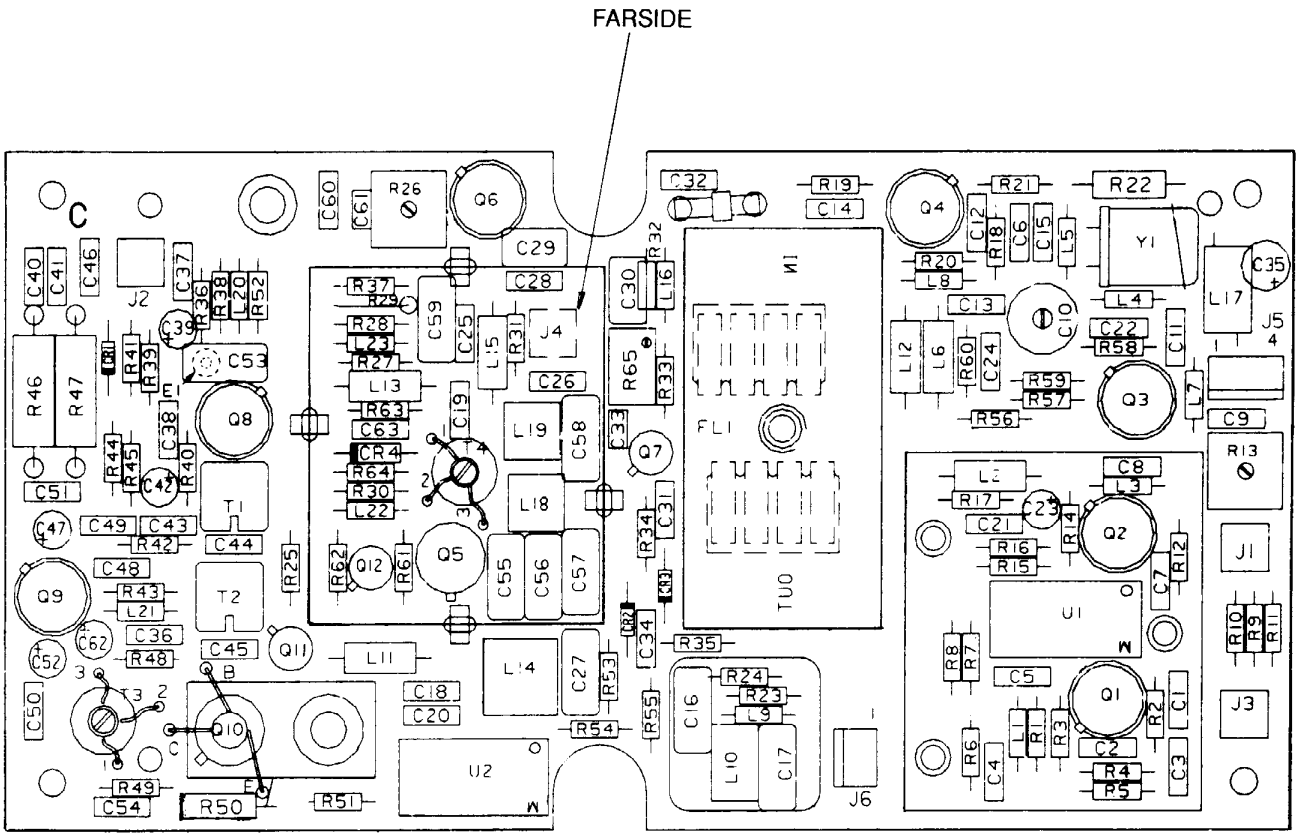
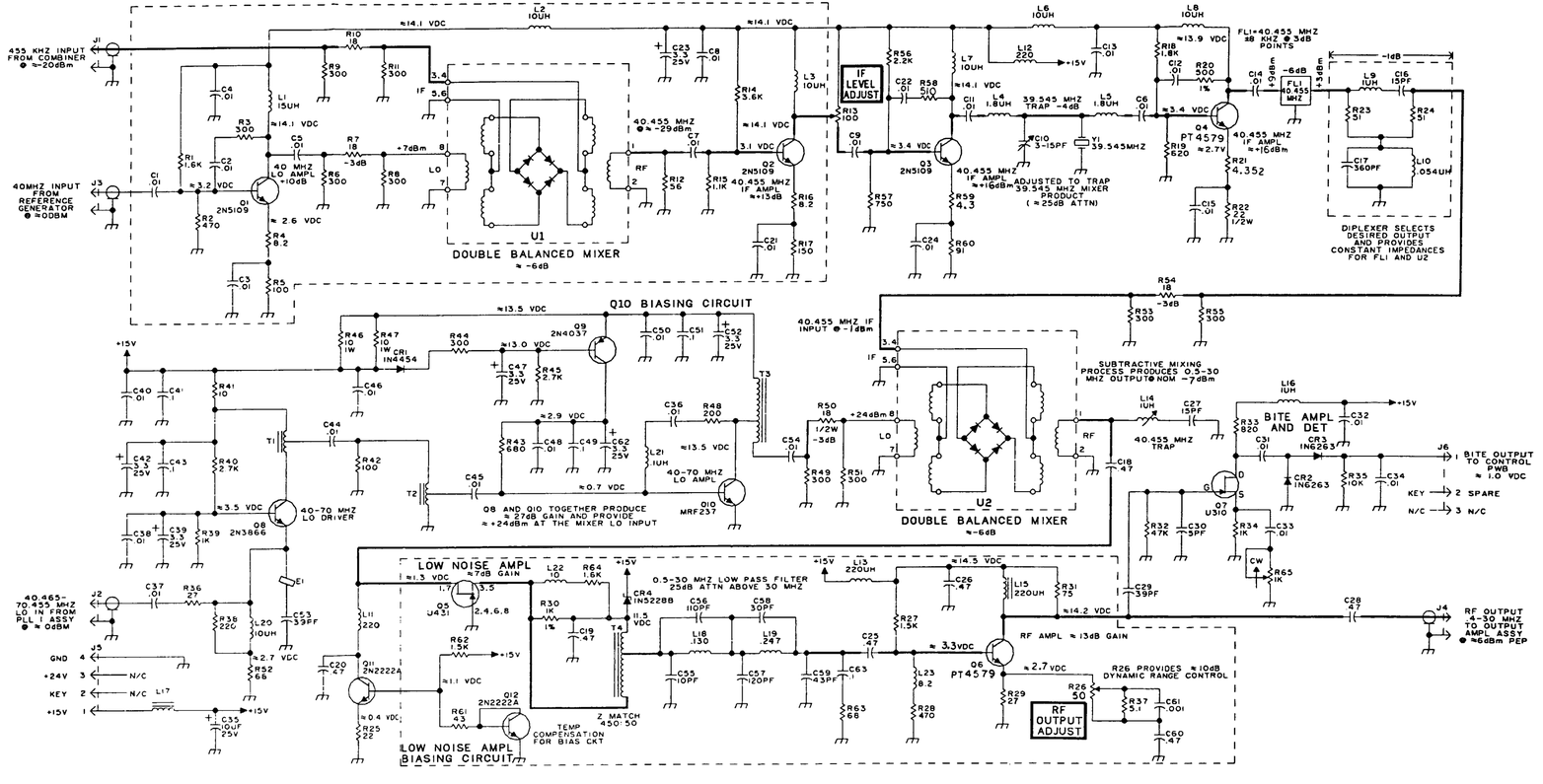


Figure 3. Converter Assembly A2 Component Location Diagram (10121-5200 Rev. L)

NOTE: UNLESS OTHERWISE SPECIFIED:

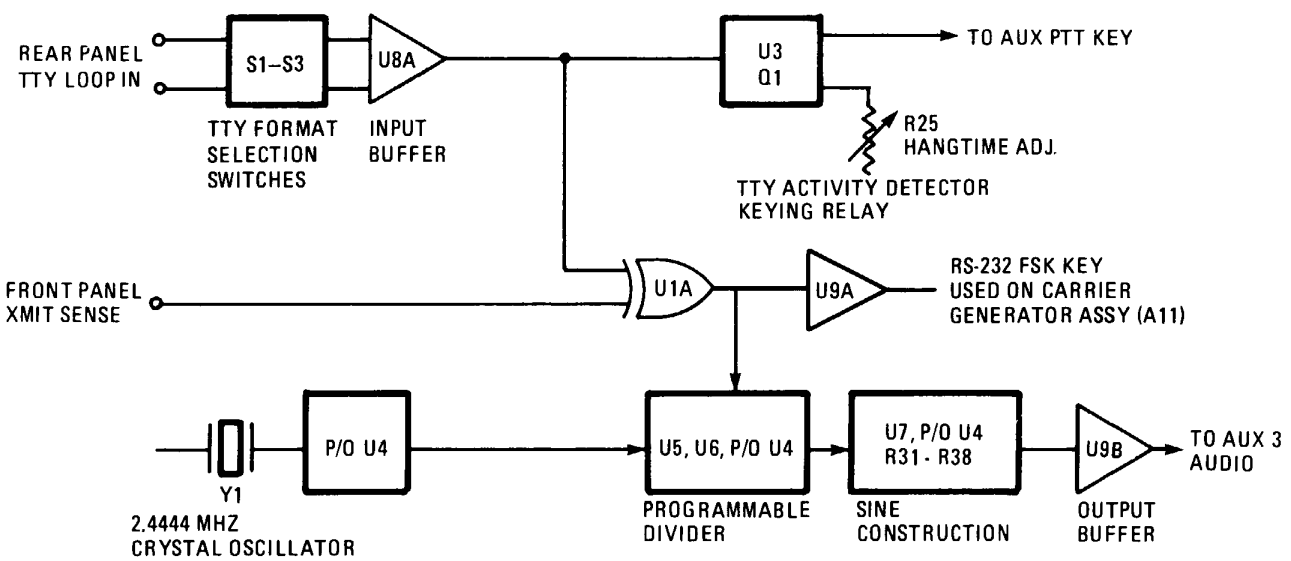
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR A COMPLETE DESIGNATION, PREFIX WITH UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.
2. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, ±5%.
3. ALL CAPACITOR VALUES ARE IN MICROFARADS.
4. VENDOR PART NO. CALLOUTS ARE FOR REFERENCE ONLY. COMPONENTS ARE SUPPLIED PER PART NO. IN PARTS LIST.
5. ALL VOLTAGES AND SIGNAL LEVELS SHOWN ARE NOMINAL VALUES.



HIGHEST REFERENCE DESIGNATION				
C63	CR4	FL1	J6	L23
Q12	R65	T4	U2	Y1
E1				
REFERENCE DESIGNATIONS NOT USED				

Figure 4. Converter Assembly A2 Schematic Diagram (10121-5201 Rev. K)

A3
ELECTRONIC KEYER



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ELECTRONIC KEYER ASSEMBLY A3

1. GENERAL DESCRIPTION

The Electronic Keyer is a single PWB Assembly containing circuits used during TTY and CW operation. Included on this assembly are the teletype loop receiver circuit, TTY activity relay, transmit sense switch, crystal oscillator, programmable divider, sine construction and buffer circuits. Figure 1 shows the location of this assembly.

2. INTERFACE CONNECTIONS

Table 1 lists the various input/output connections.

Table 1. Electronic Keyer Assembly A3 Interface Connections

Connector	Function
J1-1	N/C
J1-2	N/C
J1-3	AUX 3 AUDIO OUT
J1-4	GROUND
J1-5	N/C
J1-6	N/C
J1-7	INDEX
J1-8	N/C
J2-1	AUX PTT KEY OUT
J2-2	N/C
J2-3	NORM REV FSK XMIT SENSE IN
J2-4	KEYER IDENT IN
J2-5thru J2-7	N/C
J2-8	KEYER IDENT
J3-1	TTY (+) IN
J3-2	INDEX
J3-3	TTY (-) IN
J5-1	+ 5 V IN
J5-2	-15 V IN
J5-3	INDEX

Table 1. Electronic Keyer Assembly A3 Interface Connections (Cont.)

Connector	Function
J5-4	GROUND
J5-5	+ 15 V IN
J5-6	N/C

3. CIRCUIT DESCRIPTIONS

Refer to the schematic diagram at the end of this section for the following discussion.

3.1 Teletype Loop Receiver

The teletype loop receiver input (J3) network allows selection of the following TTY loop formats:

- 60 mA Neutral
- 20 mA Neutral
- 100 V Neutral
- 50 V Neutral
- 6 V Polar (RS-232, MIL-188C)
- Dry Contact - - -

TTY signalling inputs at J3-1, 3 are applied to S2, which routes the signals to either a diode bridge rectifier (CR8) in all neutral modes or to S3 and its associated input protection network in polar mode (RS-232, MIL-188C).

The input protection network consisting of RT1, RT2, RT3, CR9, and CR10 protects the keyer loop receiver against transients on the TTY loop lines and also protects the circuit from operator loop set-up errors.

Switches S1-S3 are used to set up the loop voltage and current formats desired as indicated in table 2.

In polar mode, S3 selects the outputs of S2 directly, while in all neutral modes it selects the output of the bridge rectifier and its associated scaling network (R2-R6), and also provides bias voltage, developed by R10 and R11, to the loop receiver operational amplifier (U8A). This bias, along with the hystersis provided by R7, R8, R9, and R14, provides the necessary mark-space transtional levels for all neutral loops. R15, R16, CR1, and CR2 convert the bipolar comparator output to CMOS logic levels.

For neutral TTY loop operation, S2 is positioned to select the rectifier bridge input, allowing the teletype loop to be hooked up with either polarity at the rear panel (J10) of the exciter, provided that the positive side of the external loop supply is not grounded.

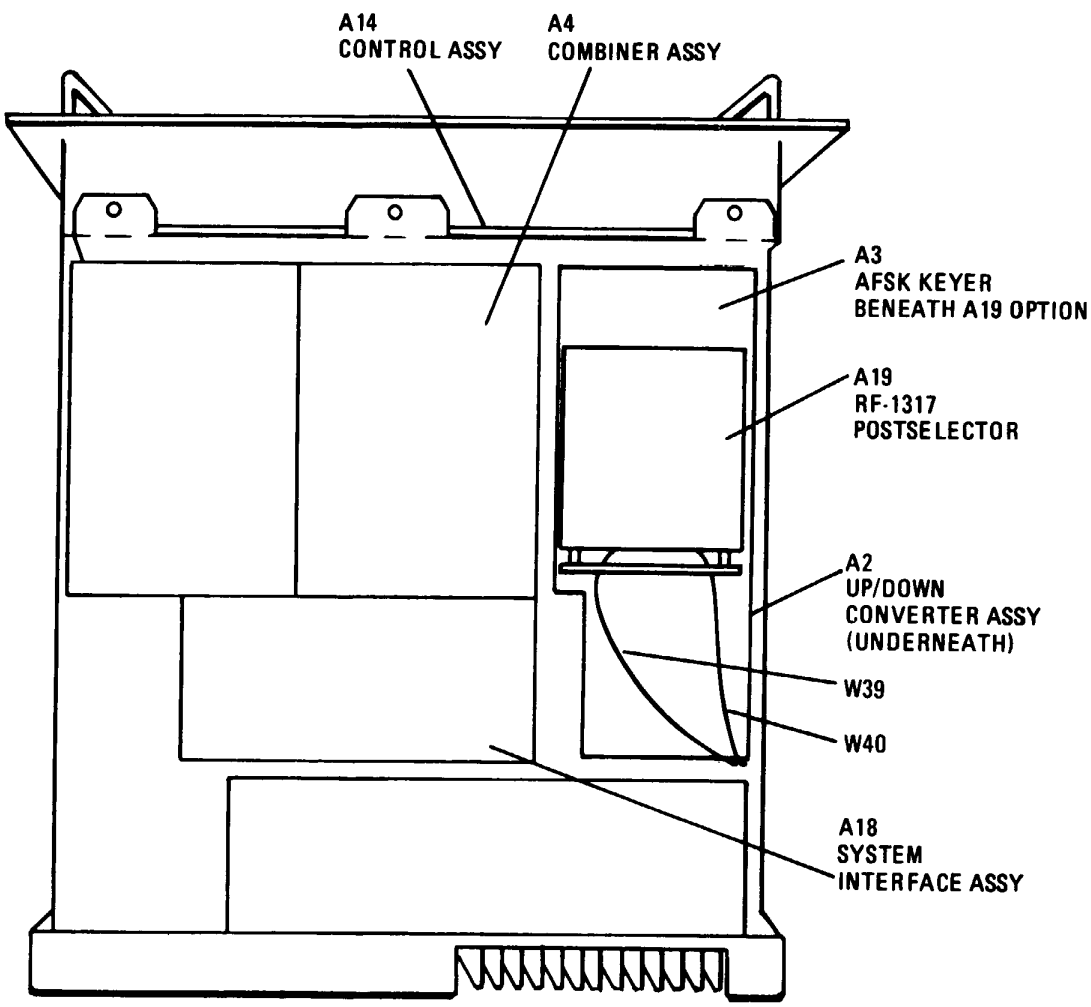


Figure 1. Electronic Keyer Assembly A3 Location Diagram

Table 2. TTY Loop Setup

Input	S2	S3	S1-1	S1-2	S1-3	S1-4	S1-5	S1-6
60 MA	C2	C2	X	X	O	---	O	O
20 MA	C2	C2	X	O	X	---	O	O
100 V	C2	C2	O	O	O	X	O	O
50 V	C2	C2	O	O	O	O	O	O
6 V POLAR	C1	C1	---	---	---	---	O	O
CRY CONT.	C2	C2	X	O	O	O	X	X

LEGEND

C1 = Straight
C2 = Bridge
O = Open
X = Closed
--- = Don't Care

NOTE

If the loop supply is inadvertently grounded the keyer may not perform to specifications.

S1-1 is used to select either voltage or current signalling loops. In the voltage loop mode resistors R2 and R5 (100 V) or R6 (50 V) form a divider circuit providing the required 2-volt potential at S3, which is connected to the input of U8A.

For current-loop operation S1-1 is closed (shorting out R2) and R3 (60 mA) or R4 (20 mA) is used so that the loop current through either one will provide the required 2-volt drop which is again applied to the input of U8A.

CAUTION

Operation with a high voltage external current loop supply requires either S1-2 or S1-3 to be closed to prevent damage to R5 or R6.

For dry-contact keying, an internal voltage is switched through S1-5 while S2 connects to the bridge rectifier and S3 is in the neutral (bridge) position. S1-6 is also closed to ground one side of the key inputs through current limiter RT3. S1-1 is closed and S1-2, 3, and 4 are open to provide maximum sensitivity. Closure of the keying contacts will then provide the proper mark-space signalling.

3.2 Teletype Activity Relay

The teletype activity relay detects transitions in the output of the teletype loop receiver. Two retriggerable monostable multivibrators (U3) are used; one triggered on low to high transitions, the other on high to low. Their outputs are sent through an OR gate to turn on transistor Q1 and the AUX PTT keyline when TTY activity is detected. Each multivibrator shares common timing components R24, R25, and C3. R25 allows hang time adjustment from the last transition of from 1 to 6 seconds before the AUX CW keyline is released.

3.3 Transmit Sense Switching

FSK transmit sense (polarity) is reversible under front panel control. A microprocessor control port line at J2-3 carries transmit sense information. OR gate U1A allows selectable data inversion for teletype data.

3.4 Crystal Oscillator

A TTL gate oscillator is used with crystal Y1 to provide the necessary reference frequency for the audio frequency shift keyed tones. This reference provides an output frequency accuracy of ± 1 Hz at 2425 Hz.

3.5 Programmable Divider

U5 and U6 are used as programmable dividers of the reference frequency. U4C and U4D load binary counts of 62 and 96 into the dividers which count down through 0, providing divide ratios of 63 and 97, for output frequencies of 2425 Hz and 1575 Hz, respectively. Actual output frequencies of the dividers will be 16 times the above frequencies. The output will be a narrow negative going pulse at U6 pin 13.

3.6 Sine Construction and Buffer

Sine construction is accomplished by an 8-stage shift register U7, U4E, and a precision resistor network R31-R38. A pseudo-sine wave output at 1/16th of the applied clock frequency is low-pass filtered and buffered by U9A and applied to the 600 ohm AUX 3 audio input.

4. MAINTENANCE

The following alignment procedure should be performed whenever a repair of the assembly indicates the need for realignment.

NOTE

Replacement PWB assemblies are factory-aligned and do not require field adjustment. However, S1-S3 must be set up for TTY loop format desired.

Refer to figure 2 for component locations with the PWB assembly installed.

a. Apply all power connections to the PWB.

b. Set up S1, S2, and S3 for dry contact keying using table 2. Apply voltmeter positive lead to TP2, negative lead to ground. Set to 10 volt range. Reading should be approximately 5 volts (Q1 off).

c. Close TTY key, shorting J3 pins 1 and 3 together. Voltmeter should read 0 volts (Q1 on) for 1-to-5 seconds, then read high (approximately 5 V) again.

d. Open TTY key. Voltmeter should again read 0 volts (Q1 on) for the same amount of time before returning to a high state (5 V).

NOTE

R25 adjusts this time delay - clockwise lengthens time, counterclockwise shortens time.

e. Apply frequency counter and oscilloscope to TP3. Verify TTL 2.4444 MHz signal present. Acceptable tolerance limits are:

- 2.44416 MHz low side
- 2.44464 MHz high side

f. Apply frequency counter and oscilloscope input to TP4.

1. Verify minimum 3.9 V_{p-p} on oscilloscope.
2. Verify 2425.0 Hz ± 1.0 Hz at TP4.

5. PARTS LISTS, COMPONENT LOCATIONS, AND SCHEMATIC DIAGRAM

Replaceable components for assembly A3 are listed in table 3. Component locations are shown in figure 2. Figure 3 is the schematic diagram.

Table 3. Electronic Keyer Assembly A3 Parts List (10121-5300 Rev. F)

Ref. Desig.	Part Number	Description
C1	M39014/01-1317V	CAP,1000PF,10% 200VC
C2	M39014/01-1317V	CAP,1000PF,10% 200VC
C3	C26-0025-100	CAP 10UF 20% 25V TANT
C4 – C6	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C7	M39014/02-1298V	CAP .01UF 10% 200V CER-R
C9	CM05FD221J03	CAP 220PF 5% 500V MICA
C10	CM05FD221J03	CAP 220PF 5% 500V MICA
C12 – C16	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C17	M39014/02-1298V	CAP .01UF 10% 200V CER-R
C18	M39014/02-1282V	CAP 1500PF 10% 200V CER-R
C21	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C22	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C23 – C25	C26-0025-100	CAP 10UF 20% 25V TANT
C26	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C27	M39014/02-1310V	CAP .1UF 10% 100V CER-R
CR1 – CR6	JAN1N4454	DIODE SWITCHING 75V 200mA
CR7	1N4007	DIODE 1A 1000V RECT GP
CR8	D22-5005-000	DIODE 1A 200V RECT BR
CR9	D50-0006-006	TRANSORB 12.0V 500W BI
CR10	D50-0006-006	TRANSORB 12.0V 500W BI
J1	J46-0032-008	HDR 8 PIN 0.100" SR
J2	J46-0032-008	HDR 8 PIN 0.100" SR
J3	J46-0032-001	HDR 3 PIN 0.100 SR
J5	J46-0032-006	HDR 6 PIN 0.100" SR
J6	J46-0032-006	HDR 6 PIN 0.100" SR
L1	MS75085-7	COIL 100UH 10% FXD RF
L2	MS75085-7	COIL 100UH 10% FXD RF

Table 3. Electronic Keyer Assembly A3 Parts List (10121-5300 Rev. F) (Cont.)

Ref. Desig.	Part Number	Description
L3	MS75085-7	COIL 100UH 10% FXD RF
Q1	JAN2N2222A	XSTR SS/GP NPN TO-18
R1	R65-0003-473	RES 47K 5% 1/4W CAR FILM
R2	R65-0003-184	RES 180K 5% 1/4W CAR FILM
R3	R65-0003-330	RES 33 5% 1/4W CAR FILM
R4	R65-0003-101	RES 100 5% 1/4W CAR FILM
R5, R6	R65-0003-752	RES 7.5K 5% 1/4W CAR FILM
R7	R65-0003-183	RES 18K 5% 1/4W CAR FILM
R8	R65-0003-105	RES 1.0M 5% 1/4W CAR FILM
R9	R65-0003-183	RES 18K 5% 1/4W CAR FILM
R10	R65-0003-333	RES 33K 5% 1/4W CAR FILM
R11	R65-0003-242	RES 2.4K 5% 1/4W CAR FILM
R14	R65-0003-105	RES 1.0M 5% 1/4W CAR FILM
R15, R16	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R17, R18	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R19	R65-0003-152	RES 1.5K 5% 1/4W CAR FILM
R20	R65-0003-473	RES 47K 5% 1/4W CAR FILM
R21	R65-0003-474	RES 470K 5% 1/4W CAR FILM
R22 – R24	R65-0003-104	RES 100K 5% 1/4W CAR FILM
R25	R30-0008-504	RES VAR PCB 500K 1/2W 10%
R26 – R30	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R31, R32	RN55D1103F	RES 110K 1% 1/8W MET FLM
R33, R34	RN55D3922F	RES 39.2K 1% 1/8W MET FLM
R35, R36	RN55D2612F	RES 26.1K 1% 1/8W MET FLM
R37, R38	RN55D2212F	RES 22.1K 1% 1/8W MET FLM
R39	R65-0003-154	RES 150K 5% 1/4W CAR FILM
R40	R65-0003-101	RES 100 5% 1/4W CAR FILM
R41 – R43	R65-0003-123	RES 12K 5% 1/4W CAR FILM
R44	R65-0003-101	RES 100 5% 1/4W CAR FILM
R45	R65-0003-103	RES 10K 5% 1/4W CAR FILM
RT1 – RT3	R76-0001-001	CURRENT LIMITER,CER,140O
S1	S50-0001-006	SW SPST 6SEC .1A SLD DIP
S2, S3	S50-0003-001	SW RCKR DIP 5 AMP 1 POS
TP1	J-0071	TP PWB BRN TOP ACCS .080"
TP2	J-0066	TP PWB RED TOP ACCS .080"
TP3	J-0069	TP PWB ORN TOP ACCS .080"
TP4	J-0070	TP PWB YEL TOP ACCS .080"
U1	I01-0000-022	IC 4070B PLASTIC CMOS
U3	I01-0000-353	IC 4538B PLASTIC CMOS
U4	I05-0000-004	IC 74LS04 PLASTIC TTL
U5, U6	I05-0000-193	IC 74LS193 PLASTIC TTL
U7	I01-0000-156	IC 4094B PLASTIC CMOS
U8, U9	I30-0035-000	IC OP AMP QUAD 072
VR1	I12-0006-005	IC VR 78L05A +5V .10A 4%
Y1	Y10-0011-001	XTAL 2.4444 MHZ.

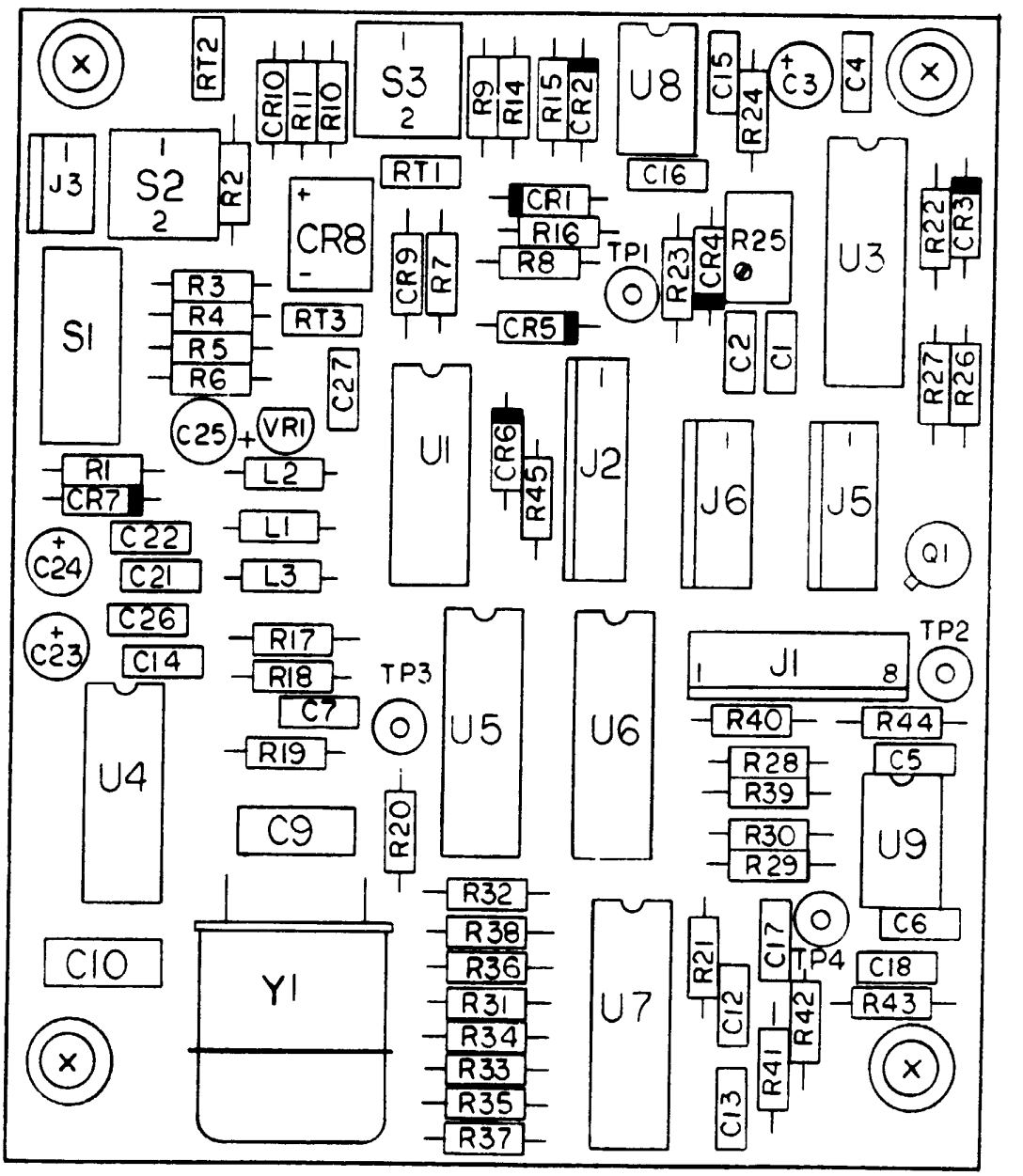


Figure 2. Electronic Keyer Assembly A3, Component Location Diagram (10121-5300, Rev. C)

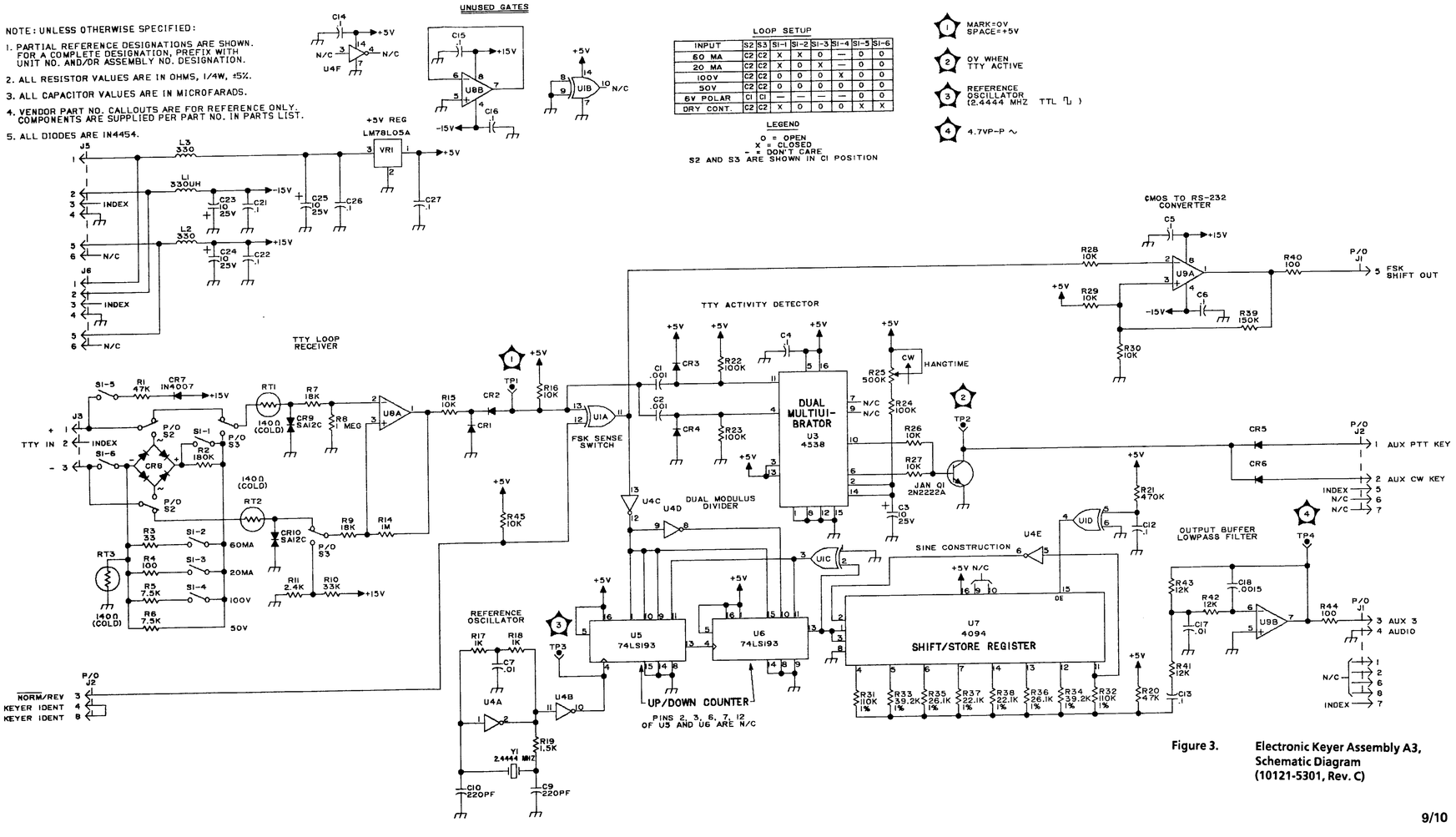
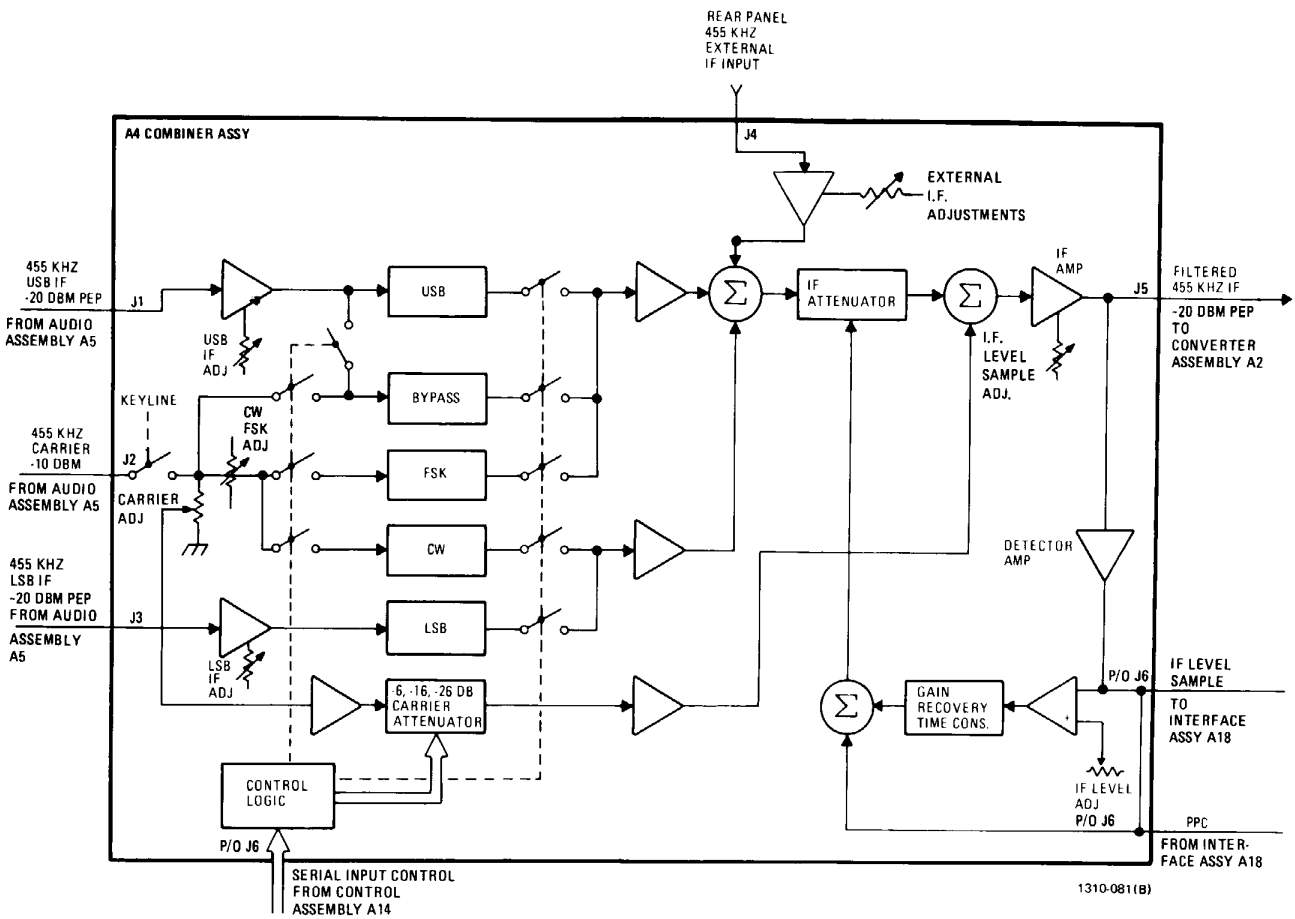


Figure 3. **Electronic Keyer Assembly A3, Schematic Diagram (10121-5301, Rev. C)**

A4
COMBINER ASSEMBLY



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COMBINER ASSEMBLY A4

1. GENERAL DESCRIPTION

Combiner Assembly A4, shown in figure 1, performs IF (455 kHz) filtering in the USB, LSB, FSK, and CW signal paths. The PWB accepts four filters. USB and LSB filters are always installed while CW and FSK filters are optional. The A4 assembly also performs 455 kHz carrier reinsertion in AM and reduced carrier modes. USB and LSB IF inputs are supplied by Audio 2 Assembly A5A2, each consisting of DSB suppressed carrier signals centered on 455 kHz. The 455 kHz carrier input is generated by Carrier Generator Assembly A11 and sent to Combiner Assembly A4 via the A5A2 assembly. An External IF Input is included, allowing postfilter injection of externally derived IF signal sources. The A4 assembly output is a -20 dBm PEP signal formed by selective combination of the USB IF, LSB IF, 455 kHz carrier, and EXT IF signal inputs. The exciter mode of transmission determines which input signals are combined to yield the composite output. The output level is maintained at -20 dBm PEP by an IF leveling loop circuit.

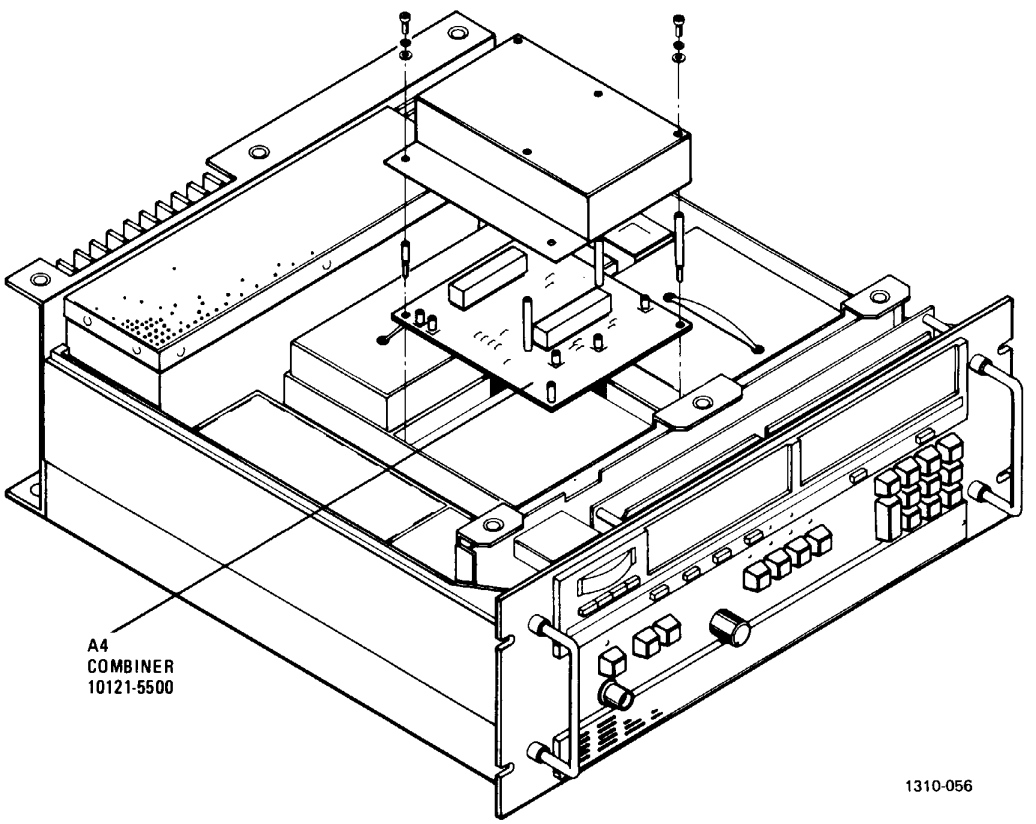


Figure 1. Combiner Assembly A4 Location

Several versions of Combiner Assembly A4 exist. The versions differ in the number and type of IF filters installed on the PWB as well as in associated parts which accommodate the various filter combinations.

2. INTERFACE CONNECTIONS

Table 1 details the various input/output connections and other relevant data.

Table 1. Combiner Assembly A4 Interface Connections

Connector	Function	Characteristics
J1	USB IF Input	-20 dBm PEP, DSB suppressed, 455 kHz carrier
J2	Carrier Input	455 kHz, -10 dBm nominal
J3	LSB IF Input	-20 dBm PEP, DSB suppressed, 455 kHz carrier
J4	External IF Input	-20 dBm PEP
J5	Combiner Output	-20 dBm PEP
J6-1	Rear Serial Data	Logic; 0 V, + 5 V
J6-2	Rear Serial Clock	Logic; 0 V, + 5 V
J6-3	Serial Check	Logic; 0 V, + 5 V
J6-4	Serial Enable	Logic; 0 V, + 5 V
J6-5	IF Envelope	4.5 Vdc at full PA Output
J6-6	PPC Control	0 to -5 Vdc, -5 Vdc yields 45 dB gain reduction
J6-7	Internal Keyline	0 V = active, + 5 Vdc = inactive
J6-8	Ground	
J6-9	Index Key	
J6-10	Combiner ID	Fixed voltage between 0 and + 5 Vdc
J6-11	Spare	
J6-12	Power, + 5 V, unregulated	+ 8 Vdc, nominal
J6-13	Power, + 15 Vdc	
J6-14	Power, -15 Vdc	

3. CIRCUIT DESCRIPTION

The circuit descriptions of Combiner Assembly A4 are grouped and described as follows:

a. Filter Circuits

- USB
- LSB
- CW
- FSK

b. USB/LSB Combiner

c. Leveling Loop Circuit

d. Carrier Reinsertion Circuit

e. First IF Input

f. PPC Control

g. Combiner PWB Function Control

3.1 Filter Circuits

The beginning of the Combiner Assembly A4 signal path consists of four selectable filter paths; the USB, LSB, CW, and FSK paths. Table 2 lists the signal path/mode selection data. Various paths are enabled depending upon exciter MODE selection and are shown in figure 2.

Table 2. T1 Combiner Modes and Inputs

Mode	Q2 Output (to T1)	Q3 Output (to T1)
CW	None	Keyed 455 kHz Carrier (via FL3)
AFSK	AFSK Tones (via FL1)	None
AME	LSB portion of USB DSB input (via FL1)	None
AM	Nonfiltered USB DSB input (Bypass)	None
USB	LSB portion of USB DSB input (via FL1)	None
LSB	None	USB portion of LSB DSB input (via FL4)
ISB	LSB portion of USB DSB input (via FL1)	USB portion of LSB DSB input (via FL4)
FM	455 kHz FM signal (Bypass)	None
FSK	FSK Tones (via FL2)	None
MCW	LSB portion of USB DSB input (via FL1)	None

3.1.1 USB Filter Circuit

The USB filter circuit provides signal paths for USB, AM, AME, MCW, and FM modes of transmission. In each of these modes, the IF signal reaches buffer Q2 by different paths. The following paragraphs describe the path for each mode.

3.1.1.1 USB Mode

Double sideband (DSB) suppressed carrier input from Audio 2 Assembly A5A2 enters J1 at a -20 dBm PEP level. R1 variably attenuates this input and applies it to amplifier Q1 which provides a nominal 8 dB gain. The amplified output at the Q1 collector is passed through FL1 which passes only the lower sideband content of the DSB input signal. In USB mode, the USB path control line is active (-15 V). This allows the filtered signal (output of FL1) to pass through CR5 to buffer Q2.

3.1.1.2 AM Mode

As in the USB mode described above, an amplified DSB signal is present at the Q1 collector. In the AM mode, both sidebands of the DSB input signal are passed (no filtering); therefore, FL1 is bypassed. The amplified DSB input signal is presented to switch CR1, CR2, and CR3. In the AM mode, the AM path control line is active (-15 V) providing a signal path through CR1 and CR3 to attenuator pad R14, R15, and R16. The $\overline{\text{BYPASS AM}}$ path control line is active (-15 V) in AM. This provides a signal path from the attenuator pad, through CR7 to buffer Q2.

3.1.1.3 AME Mode

The AME signal path is identical to the USB mode path (through FL1). USB is active in AME and the signal passes to Q2 via CR5. The carrier injection required in AME mode is described in paragraph 3.4.

3.1.1.4 MCW Mode

The MCW signal path is identical to the signal path for the USB mode. Refer to paragraph 3.1.1.1 for the signal path description.

3.1.1.5 FM Mode

The FM signal enters at 455 kHz Carrier Input J2. For FM transmission, $\overline{\text{BYPASS}}$ and $\overline{\text{BYPASS AM}}$ path control lines are active (-15 V) yielding an FM signal path through CR11, CR12, CR13, attenuator pad R14, R15, R16, and CR7 to buffer Q2.

3.1.2 LSB Filter Circuit

The LSB filter circuit path is used only in LSB mode. The LSB DSB IF input signal at J3 is variably attenuated by R75 and amplified by Q4. Q4 provides a nominal 8 dB gain. The amplified DSB signal at the Q4 collector passes through FL4 which passes only the upper sideband portion of the double sideband input signal. In the LSB mode, the $\overline{\text{LSB}}$ path control line is active (-15 V), and provides a signal path through CR25 to buffer Q3.

3.1.3 CW Filter Circuit

The 455 kHz carrier enters J2 with a level of -10 dBm. CW keying of the carrier is accomplished by switching CR11 on and off in response to $\overline{\text{INTERNAL KEYLINE}}$. The keyline waveform is modified by R48, R49, CR15, CR16, and C39 to yield proper CW output waveform shaping. When CR11 is ON ($\overline{\text{INTERNAL KEYLINE}}$ low, exciter keyed), the 455 kHz carrier passes through CR11 to CR21. In CW mode, the CW path control line is active (-15 V). This provides a signal path through CR21, FL3, and CR23 to buffer Q3. If FL3 is not installed, pad R127, R128, and R129 substitutes for the filter.

3.1.4 FSK Filter Circuit

FSK tones enter J2 at a level of -10 dBm. INTERNAL KEYLINE remains active (0 V) throughout the FSK transmission, providing a signal path through CR11 to CR17. In FSK mode, the FSK path control line is active (-15 V) and provides a signal path through CR17, FL2, and CR20 to buffer Q2. If FL2 is not installed, pad R124, R125, and R126 substitutes for the filter.

3.2 First Combiner

T1 combines the outputs of buffers Q2 and Q3 to form a composite signal which is sent to the IF leveling loop circuit. In ISB mode, both buffers supply input to T1. In the other modes, only one (Q2 or Q3) supplies input. Table 2 lists the T1 inputs for the various modes of transmission.

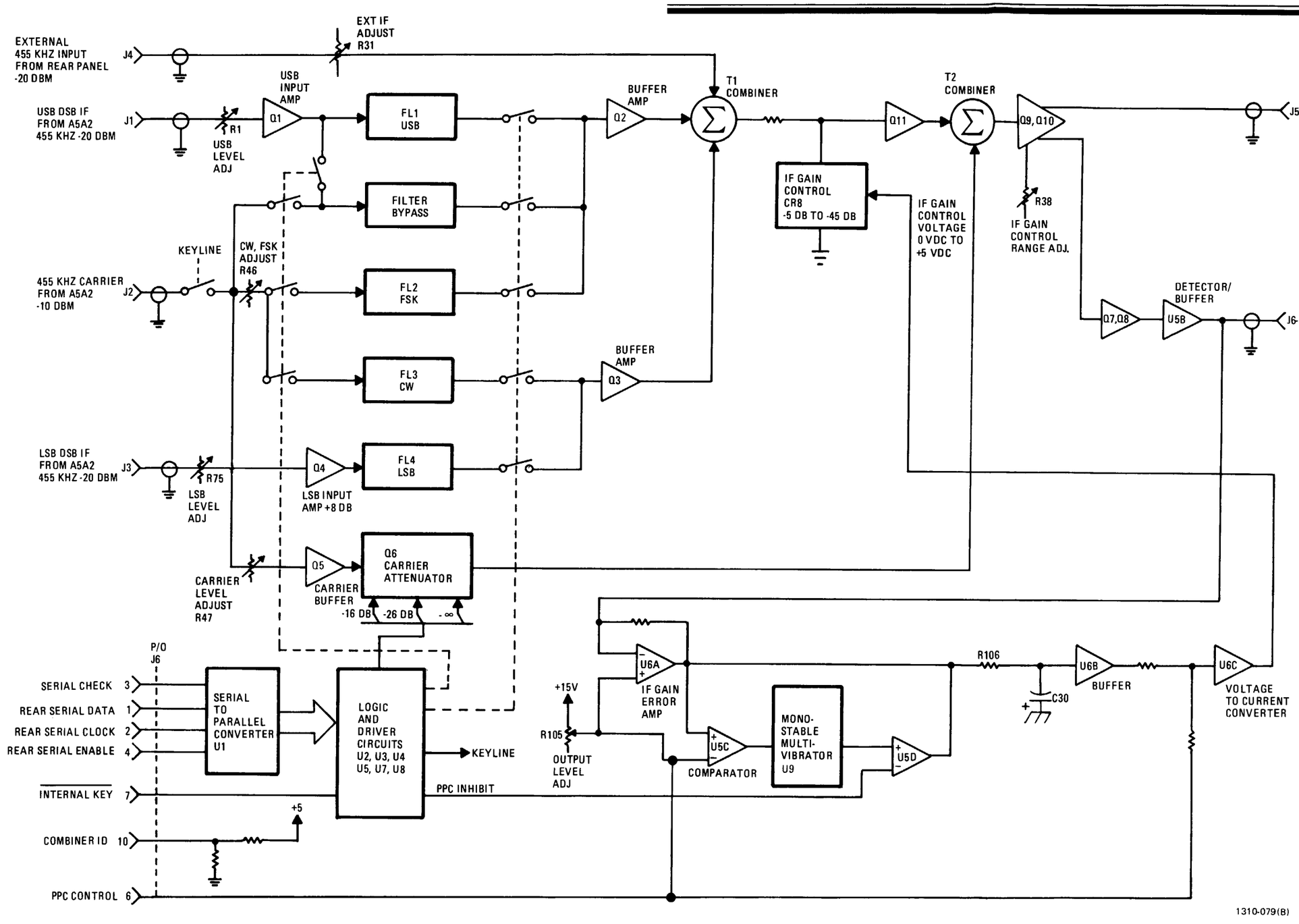


Figure 2. **Combiner Assembly A4 Functional Block Diagram**

3.3 Leveling Loop Circuit

Combiner Assembly A4 output is maintained at -20 dBm PEP, regardless of transmission mode, through action of an active hang-type gain control loop circuit. The circuit detects the Combiner output level and dynamically attenuates the T1 combiner output to maintain a proper output level at J5.

The T1 combiner output is shunted by PIN diode attenuator CR8 and applied to buffer Q11. T2 combines the Q11 output with a reduced carrier or external IF signal if either are present. The composite T2 output is amplified by feedback pair Q9 and Q10 which supply two outputs. The first, a high gain output, is applied to amplifiers Q7 and Q8. The second, a low gain output, is the Combiner Assembly A4 output, J5. CR31 detects the high gain output yielding a dc voltage at U5-10 proportional to the output level. U5B buffers the detected dc voltage into IF gain error amplifier U6A and to IF envelope J6-5. The IF envelope signal, J6-5, is sent to System Interface Assembly A18A2 where it serves as a reference voltage in the exciter/PA output gain control loop. Error amplifier U6A compares the detected dc level to an adjustable dc reference voltage at U6-12. Any detected IF level greater than the reference voltage is amplified by U6A, whose output negatively charges C30. The voltage developed across C30 is buffered by U6B and converted to a control voltage that is applied to PIN attenuator CR8. CR8 attenuates the T1 output signal in proportion to the dc control voltage applied to it. Transmitter PPC Control via CR38 will lower the threshold voltage, causing the U6A Amplifier to act sooner, thus reducing the module output.

An increase or decrease in the Combiner Assembly output (J5) yields a corresponding change in the detected dc output. This yields a change in the error voltage at C30 and therefore the current applied to PIN attenuator CR8. The Combiner Assembly output (J5) is maintained at a constant PEP level determined by the adjustable (R105) reference voltage at U6-12. R105 is normally adjusted to yield a combiner output level of -20 dBm PEP.

U5C, U9, and U5D form a hang-type gain recovery circuit. This circuit, after a delay, reduces the attenuation inserted in response to a sustained A4 output signal decrease. The circuit has a built-in 0.15-second delay called the hangtime. The action of the gain recovery circuit reduces the negative charge on C30 built up during the period of high signal level.

U5C compares the U6A output voltage to the reference voltage supplied by R105 and Transmitter PPC. A drop in the A4 output signal level will cause the U6A output to go to + 15 volts. This changes the U5C output from -15 volts to + 15 volts and triggers monostable multivibrator U9, thus starting the 0.150 second timing cycle.

The output of U9, pin 7, goes low (0 V). After 0.15-seconds, U9 resets to cause U5D to forward bias CR35 and forces C30 to discharge. This action reduces the voltage applied to CR8 and the signal attenuation. As the A4 assembly output signal level increases, U6A will start to detect amplitude above the threshold, invert it, and charge C30 in a negative direction through CR33.

3.4 Carrier Reinsertion Circuit

Reinsertion of the 455 kHz carrier in AM, AME, and reduced carrier modes occurs at combining transformer T2. Buffer Q11 supplies the sideband (intelligence) input to T2 and Q6 supplies the carrier input to T2 via CR29. In modes requiring carrier reinsertion, the 455 kHz carrier at J2 passes through switch CR11 to buffer Q5. R47 adjusts the nominal carrier level presented to Q5. The output of Q5 is presented to two selectable attenuating networks, R90, R93, and R94, R95. The networks are individually switched into the circuit by activating the -16 and -26 control lines which turn on CR27 and CR28, respectively. The R90, R93 network yields a carrier attenuation of -16 dB and the R94, R95 network yields a -26 dB attenuation. Q6 buffers the output of the attenuator network and outputs the carrier to T2 via switch CR29. CR29 is ON for all modes requiring carrier insertion.

Carrier attenuation levels other than -16 dB and -26 dB are achieved by appropriate changes of resistor values in the attenuator networks. Carrier attenuation levels of -16 dB and -26 dB are standard. The PWB can be

modified to change the levels to -10 dB and -20 dB. The Combiner ID signal (J6-10) tells Control Board Assembly A14 which levels are being used. The Control Board Assembly then sends the appropriate carrier display information to the front panel. A voltage divider made up of R116 and R117 is used to set the dc voltage of the Combiner ID signal at a level proportional to the selected attenuation levels.

3.5 External IF Input

Externally supplied 455 kHz signals may be injected into the A4 assembly signal path via access provided at the exciter rear panel. Such signals enter Combiner Assembly A4 at J4 and are injected at Q11 via R34. Externally injected IF signals should be nominally -20 dBm, 50 ohms.

3.6 PPC Control

In most transmitting systems peak power control is required. A gain controlling dc voltage is applied at the PPC INPUT (J6-6). This dc voltage is derived by sampling the system output level, current and voltage protection circuits, or other parameters. The voltage at J6-6 will change from 0 volts to -7 volts. The first portion (0 to -3 volts dc) is applied to threshold voltage through CR38 (6.8 V Zener diode). Control voltage beyond -4 volts dc is applied directly to the voltage-to-current converter (U6C), which in turn controls attenuator CR8. Attenuation of the A4 assembly output varies from 0 dB to -35 dB for the PPC input voltages of 0 to -7 volts dc respectively.

3.7 Combiner PWB Function Control

The microprocessor of Control Board Assembly A14 controls the functions of the A4 assembly by transmitting a serial data stream appearing at J6-1, Rear Serial Data. The data stream is decoded into an eight-bit control word by serial-to-parallel converter U1. The eight outputs of U1 are converted from their 0 V, 5 V logic levels to -15 V, + 15 V control voltages by comparators U2, U3, and U4. The resultant ± 15 V control signals and their effects on function selection throughout the Combiner Assembly circuitry are listed in table 3.

Table 3. Assembly Path Control Lines

Control Signal	-15 Volt	+ 15 Volt	Active (-15 V) in the following modes
$\overline{\text{LSB}}$, U3-8	Enables FL4 signal path	Disables FL4 signal path	LSB, ISB
$\overline{\text{FSK}}$, U3-1	Enables FL2 signal path	Disables FL2 signal path	FSK
$\overline{\text{CW}}$, U3-14	Enables FL3 signal path	Disables FL3 signal path	CW
-$\overline{16}$, U2-14	Selects -16 dB car. reinsertion level	Deselects -16 dB car. reinsertion level	-16
-$\overline{26}$, U2-1	Selects -26 dB car. reinsertion level	Deselects -26 dB car. reinsertion level	-26
$\overline{\text{BYPASS}}$, U2-8	Enables path from J2 to pad R14, R15, R16	Disables path from J2 to pad R14, R15, R16	FM
$\overline{\text{USB}}$, U4-1	Enables FL1 signal path	Disables FL1 signal path	USB, AME, MCW
$\overline{\text{AM}}$, U4-14	Enables path from J1 to pad R14, R15, R16	Disables path from J1 to pad R14, R15, R16	AM
$\overline{\text{CAR}}$ $\overline{\text{RNSRT}}$,U4-7	Enables carrier insertion at T2	Disables carrier insertion at T2	AM, AME, 16 and -26
$\overline{\text{BYPASS}}$ $\overline{\text{AM}}$	Enables path from pad R14, R15, R16 to Q2	Disables path from pad R14, R15, R16 to Q2	AM and FM

The position of JMP1 determines selection of AM (DSB, full carrier) versus AME (SSB, full carrier).

4. MAINTENANCE

The following adjustments should not be made as part of a routine maintenance procedure, but only when a failure indicates a definite need. Unless otherwise specified, the following adjustments are to be performed with all assemblies in normal electrical contact.

4.1 Output Level Adjustment

a. Set up the equipment as shown in figure 3. Set the exciter function switch to OFF.

b. Set R2, R76, R105, R31, R47, and R46 fully clockwise (cw position).

c. Set R38 fully counterclockwise (ccw).

d. Set exciter front panel controls as follows:

- FUNCTION: NORM
- MODE: CW
- RF PWR: -00
- FREQ: 2.0000 MHz
- CLIP: OFF

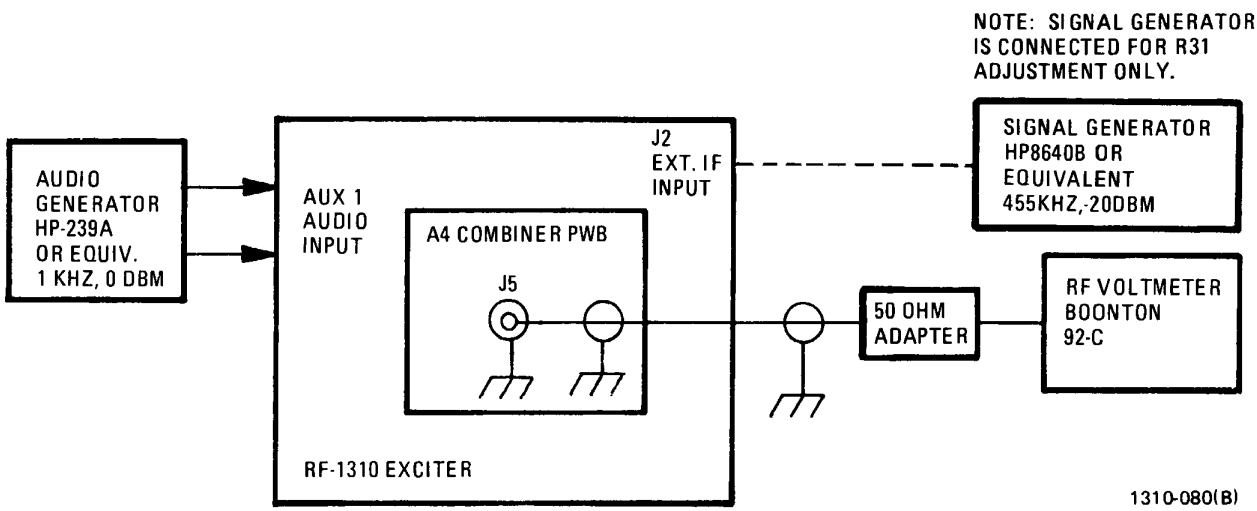


Figure 3. Combiner PWB Assembly Maintenance Setup

e. CW key the exciter and momentarily short across CR34 to ensure there is no charge on C30. Adjust R46 for -20 dBm at J5.

f. Adjust R38 for 5.75 volts at TP4.

g. Adjust R46 for -17 dBm at J5. Unkey CW keyline.

h. Set exciter MODE switch to USB and AUDIO switch to AUX 1.

i. Key PTT line and adjust R2 for -17 dBm at J5. Unkey PTT line.

j. Set exciter MODE switch to LSB and AUDIO switch to AUX 1.

k. Key PTT line and adjust R76 for -17 dBm at J5. Unkey PTT line.

l. Remove brown sleeved cable attached to J1. Set exciter MODE switch to AM.

m. Key PTT line and adjust R47 for -26 dBm at J5.

n. Reconnect brown sleeved cable to J1.

o. Apply a -20 dBm external IF signal (455 kHz) to J2 at the rear panel of exciter. Adjust R31 for -17 dBm at J5. Disconnect external IF signal, supplied by the signal generator from J2.

p. Set exciter MODE switch to CW.

q. Key CW keyline and adjust R105 for -20 dBm at J5.

r. Adjustment procedure is complete. Set up the normal connection to J5.

5. PARTS LIST, COMPONENT LOCATION, AND SCHEMATIC DIAGRAM

All replaceable components of the standard Combiner Assembly A4 are listed in table 4. (The standard Combiner Assembly supplied with RF-1310 is the 10121-5500-03.) Component substitutions for optional configurations are listed in tables 5 and 6. Figure 4 shows the locations of all components in the assembly. Figure 5 is a schematic diagram of Combiner Assembly A4.

Table 4. Combiner Assembly A4 Parts List (10121-5500-03 Rev. E)

Ref. Desig.	Part Number	Description
	J46-0047-003	HEADER 3 POS
C1	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C2	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C3	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C4	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C5	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C6	M39014/02-1310V	CAP .1UF 10% 100V CER-R

Table 4. Combiner Assembly A4 Parts List (10121-5500-03 Rev. E) (Cont.)

Ref. Desig.	Part Number	Description
C7	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C8	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C9	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C10	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C11	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C12	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C13	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C15	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C16	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C17	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C18	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C19	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C20	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C21	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C22	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C23	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C24	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C25	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C26	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C27	C26-0025-339	CAP 3.3UF 20% 25V TANT
C28	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C29	M39014/02-1292V	CAP 4700PF 10% 200V CER-R
C30	C26-0025-100	CAP 10UF 20% 25V TANT
C33	M39014/02-1302V	CAP .022UF 10% 100V CER-R
C34	C26-0035-159	CAP 1.5UF 20% 35V TANT
C35	C26-0035-339	CAP 3.3UF 20% 35V TANT
C36	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C37	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C38	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C39	C26-0025-479	CAP 4.7UF 20% 25V TANT
C40	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C41	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C42	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C43	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C44	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C45	M39014/02-1320V	CAP .47UF 10% 50V CER-R
C46	C26-0025-100	CAP 10UF 20% 25V TANT
C47	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C48	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C49	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C50	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C51	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C52	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C53	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C54	M39014/02-1310V	CAP .1UF 10% 100V CER-R

Table 4. Combiner Assembly A4 Parts List (10121-5500-03 Rev. E) (Cont.)

Ref. Desig.	Part Number	Description
C55	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C56	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C57	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C58	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C61	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C62	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C63	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C64	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C65	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C66	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C67	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C68	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C69	C26-0025-339	CAP 3.3UF 20% 25V TANT
C70	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C71	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C72	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C73	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C74	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C75	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C76	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C77	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C78	C26-0025-339	CAP 3.3UF 20% 25V TANT
C79	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C80	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C81	C26-0035-470	CAP 47UF 20% 35V TANT
C82	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C83	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C84	C26-0035-470	CAP 47UF 20% 35V TANT
C86	CM05FD271J03	CAP 270PF 5% 500V MICA
C87	CM05FD271J03	CAP 270PF 5% 500V MICA
C92	CM05FD271J03	CAP 270PF 5% 500V MICA
C93	CM05FD271J03	CAP 270PF 5% 500V MICA
C94	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C96	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C97	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C98	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C99	M39014/02-1310V	CAP .1UF 10% 100V CER-R
CR1	1N4454	DIODE 200MA 75V SW
CR2	1N4454	DIODE 200MA 75V SW
CR3	1N4454	DIODE 200MA 75V SW
CR4	1N4454	DIODE 200MA 75V SW
CR5	1N4454	DIODE 200MA 75V SW
CR6	1N4454	DIODE 200MA 75V SW
CR7	1N4454	DIODE 200MA 75V SW

Table 4. Combiner Assembly A4 Parts List (10121-5500-03 Rev. E) (Cont.)

Ref. Desig.	Part Number	Description
CR8	D12-0007-001	DIODE PIN ATTN 1W 9301
CR9	1N4454	DIODE 200MA 75V SW
CR10	1N4454	DIODE 200MA 75V SW
CR11	D10-3500-000	DIODE .25W 35V PIN BSW
CR12	1N4454	DIODE 200MA 75V SW
CR13	1N4454	DIODE 200MA 75V SW
CR14	1N4454	DIODE 200MA 75V SW
CR15	1N4454	DIODE 200MA 75V SW
CR16	1N4454	DIODE 200MA 75V SW
CR17	1N4454	DIODE 200MA 75V SW
CR18	1N4454	DIODE 200MA 75V SW
CR19	1N4454	DIODE 200MA 75V SW
CR20	1N4454	DIODE 200MA 75V SW
CR21	1N4454	DIODE 200MA 75V SW
CR22	1N4454	DIODE 200MA 75V SW
CR23	1N4454	DIODE 200MA 75V SW
CR24	1N4454	DIODE 200MA 75V SW
CR25	1N4454	DIODE 200MA 75V SW
CR26	1N4454	DIODE 200MA 75V SW
CR27	D10-3500-000	DIODE .25W 35V PIN BSW
CR28	D10-3500-000	DIODE .25W 35V PIN BSW
CR29	D10-3500-000	DIODE .25W 35V PIN BSW
CR30	D10-3500-000	DIODE .25W 35V PIN BSW
CR31	1N6263	DIODE .40W 60V HOT CARR
CR32	1N4454	DIODE 200MA 75V SW
CR33	1N4454	DIODE 200MA 75V SW
CR34	1N4454	DIODE 200MA 75V SW
CR35	1N4454	DIODE 200MA 75V SW
CR36	1N4454	DIODE 200MA 75V SW
CR38	1N5228B	DIODE 3.9V 5% .5W ZENER
CR39	1N4454	DIODE 200MA 75V SW
CR40	1N5235B	DIODE 6.8V 5% .5W ZENER
CR41	1N4454	DIODE 200MA 75V SW
CR42	1N4004	DIODE 1A 400V RECT GP
CR43	1N4454	DIODE 200MA 75V SW
FL1	10073-7300	FLTR MECH 455 KHZ LSB
FL4	10073-7301	FLTR MECH 455 KHZ USB
J1 – J5	J-0031	CONN SMB VERT PCB F
J6	J46-0032-014	HDR 14 PIN 0.100" SR
JMP1	J65-0008-103	JMPR 2P FEM .10CNTR
L1	10073-7033	INDUCTOR, 10MH
L2	MS75085-13	COIL 330UH 10% FXD RF
L3	MS75085-19	COIL 1000UH 10% FXD RF
L5	10073-7033	INDUCTOR, 10MH

Table 4. Combiner Assembly A4 Parts List (10121-5500-03 Rev. E) (Cont.)

Ref. Desig.	Part Number	Description
L7	10073-7033	INDUCTOR, 10MH
L10	MS75085-13	COIL 330UH 10% FXD RF
L11	10073-7033	INDUCTOR, 10MH
L12, L13	MS75085-13	COIL 330UH 10% FXD RF
L14, L15	MS75085-7	COIL 100UH 10% FXD RF
L17	MS75085-17	COIL 680UH 10% FXD RF
Q1	2N4123	XSTR SS/GP NPN TO-92
Q2, Q3	Q35-0003-000	XSTR N-CH JFET U310
Q4	2N4123	XSTR SS/GP NPN TO-92
Q5	2N4123	XSTR SS/GP NPN TO-92
Q6	2N4123	XSTR SS/GP NPN TO-92
Q7	2N4123	XSTR SS/GP NPN TO-92
Q8	2N4123	XSTR SS/GP NPN TO-92
Q9	2N4123	XSTR SS/GP NPN TO-92
Q10	2N4123	XSTR SS/GP NPN TO-92
Q11	2N4123	XSTR SS/GP NPN TO-92
Q12	2N4123	XSTR SS/GP NPN TO-92
Q13	2N4123	XSTR SS/GP NPN TO-92
Q14	2N4123	XSTR SS/GP NPN TO-92
R1	R65-0003-680	RES 68 5% 1/4W CAR FILM
R2	R-2204	RES VAR 200 10% .5W HOR.
R3	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R4	R65-0003-512	RES 5.1K 5% 1/4W CAR FILM
R5	R65-0003-222	RES 2.2K 5% 1/4W CAR FILM
R6	R65-0003-101	RES 100 5% 1/4W CAR FILM
R7	R65-0003-152	RES 1.5K 5% 1/4W CAR FILM
R8	R65-0003-101	RES 100 5% 1/4W CAR FILM
R9	R65-0003-362	RES 3.6K 5% 1/4W CAR FILM
R10	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R11	R65-0003-512	RES 5.1K 5% 1/4W CAR FILM
R12	R65-0003-512	RES 5.1K 5% 1/4W CAR FILM
R13	R65-0003-512	RES 5.1K 5% 1/4W CAR FILM
R14	R65-0003-153	RES 15K 5% 1/4W CAR FILM
R15	R65-0003-392	RES 3.9K 5% 1/4W CAR FILM
R16	R65-0003-153	RES 15K 5% 1/4W CAR FILM
R17	R65-0003-512	RES 5.1K 5% 1/4W CAR FILM
R18	R65-0003-104	RES 100K 5% 1/4W CAR FILM
R19	R65-0003-201	RES 200 5% 1/4W CAR FILM
R20	R65-0003-101	RES 100 5% 1/4W CAR FILM
R21	R65-0003-201	RES 200 5% 1/4W CAR FILM
R22	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R23	R65-0003-620	RES 62 5% 1/4W CAR FILM
R24	R65-0003-202	RES 2.0K 5% 1/4W CAR FILM
R25	R65-0003-101	RES 100 5% 1/4W CAR FILM
R26	R65-0003-273	RES 27K 5% 1/4W CAR FILM

Table 4. Combiner Assembly A4 Parts List (10121-5500-03 Rev. E) (Cont.)

Ref. Desig.	Part Number	Description
R27	R65-0003-203	RES 20K 5% 1/4W CAR FILM
R28	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R29	R65-0003-201	RES 200 5% 1/4W CAR FILM
R30	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R31	R-2204	RES VAR 200 10% .5W HOR.
R32	R65-0003-201	RES 200 5% 1/4W CAR FILM
R33	R65-0003-101	RES 100 5% 1/4W CAR FILM
R34	R65-0003-680	RES 68 5% 1/4W CAR FILM
R35	R65-0003-101	RES 100 5% 1/4W CAR FILM
R36	R65-0003-620	RES 62 5% 1/4W CAR FILM
R37	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R38	R30-0008-102	RES VAR PCB 1K 1/2W 10%
R39	R65-0003-182	RES 1.8K 5% 1/4W CAR FILM
R40	R65-0003-101	RES 100 5% 1/4W CAR FILM
R41	R65-0003-271	RES 270 5% 1/4W CAR FILM
R42	R65-0003-302	RES 3.0K 5% 1/4W CAR FILM
R43	R65-0003-512	RES 5.1K 5% 1/4W CAR FILM
R44	R65-0003-202	RES 2.0K 5% 1/4W CAR FILM
R45	R65-0003-560	RES 56 5% 1/4W CAR FILM
R46	R30-0008-503	RES VAR PCB 50K 1/2W 10%
R47	R-2205	RES VAR 500 10% .5W HOR.
R48, R49	R65-0003-332	RES 3.3K 5% 1/4W CAR FILM
R50	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R51	R65-0003-152	RES 1.5K 5% 1/4W CAR FILM
R52	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R53	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R54, R55	R65-0003-104	RES 100K 5% 1/4W CAR FILM
R56	R65-0003-512	RES 5.1K 5% 1/4W CAR FILM
R57, R58	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R59	RN55D3011F	RES 3010 1% 1/8W MET FLM
R60	R65-0003-363	RES 36K 5% 1/4W CAR FILM
R61	RN55D1821F	RES 1820 1% 1/8W MET FLM
R62	RN55D2742F	RES 27.4K 1% 1/8W MET FLM
R64	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R65	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R66	R65-0003-152	RES 1.5K 5% 1/4W CAR FILM
R67	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R68	R65-0003-104	RES 100K 5% 1/4W CAR FILM
R69	R65-0003-331	RES 330 5% 1/4W CAR FILM
R70	R65-0003-222	RES 2.2K 5% 1/4W CAR FILM
R71	R65-0003-512	RES 5.1K 5% 1/4W CAR FILM
R72	R65-0003-104	RES 100K 5% 1/4W CAR FILM
R73	R65-0003-201	RES 200 5% 1/4W CAR FILM
R74	R65-0003-101	RES 100 5% 1/4W CAR FILM
R75	R65-0003-680	RES 68 5% 1/4W CAR FILM

Table 4. Combiner Assembly A4 Parts List (10121-5500-03) (Cont.)

Ref. Desig.	Part Number	Description
R76	R-2204	RES VAR 200 10% .5W HOR.
R77	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R78	R65-0003-512	RES 5.1K 5% 1/4W CAR FILM
R79	R65-0003-152	RES 1.5K 5% 1/4W CAR FILM
R80	R65-0003-101	RES 100 5% 1/4W CAR FILM
R81	R65-0003-222	RES 2.2K 5% 1/4W CAR FILM
R82	R65-0003-362	RES 3.6K 5% 1/4W CAR FILM
R83	R65-0003-512	RES 5.1K 5% 1/4W CAR FILM
R84	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R85	R65-0003-243	RES 24K 5% 1/4W CAR FILM
R86	R65-0003-622	RES 6.2K 5% 1/4W CAR FILM
R87, R88	R65-0003-621	RES 620 5% 1/4W CAR FILM
R89	R65-0003-101	RES 100 5% 1/4W CAR FILM
R90	R65-0003-391	RES 390 5% 1/4W CAR FILM
R91, R92	R65-0003-392	RES 3.9K 5% 1/4W CAR FILM
R93	R65-0003-151	RES 150 5% 1/4W CAR FILM
R94	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R95	R65-0003-750	RES 75 5% 1/4W CAR FILM
R96	R65-0003-203	RES 20K 5% 1/4W CAR FILM
R97	R65-0003-682	RES 6.8K 5% 1/4W CAR FILM
R98	R65-0003-621	RES 620 5% 1/4W CAR FILM
R99	R65-0003-681	RES 680 5% 1/4W CAR FILM
R100	R65-0003-182	RES 1.8K 5% 1/4W CAR FILM
R101	R65-0003-510	RES 51 5% 1/4W CAR FILM
R102	R65-0003-392	RES 3.9K 5% 1/4W CAR FILM
R103	R65-0003-104	RES 100K 5% 1/4W CAR FILM
R104	R65-0003-432	RES 4.3K 5% 1/4W CAR FILM
R105	R-2210	RES VAR 20K 10% .5W HOR.
R106	R65-0003-222	RES 2.2K 5% 1/4W CAR FILM
R107	R65-0003-333	RES 33K 5% 1/4W CAR FILM
R108	R65-0003-473	RES 47K 5% 1/4W CAR FILM
R109	R65-0003-683	RES 68K 5% 1/4W CAR FILM
R110	R65-0003-104	RES 100K 5% 1/4W CAR FILM
R111	R65-0003-154	RES 150K 5% 1/4W CAR FILM
R112	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R113	R65-0003-302	RES 3.0K 5% 1/4W CAR FILM
R116, R117	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R118	R65-0003-101	RES 100 5% 1/4W CAR FILM
R119 – R121	R65-0003-473	RES 47K 5% 1/4W CAR FILM
R122	R65-0003-821	RES 820 5% 1/4W CAR FILM
R123	R65-0003-101	RES 100 5% 1/4W CAR FILM
R124	R65-0003-153	RES 15K 5% 1/4W CAR FILM
R125	R65-0003-392	RES 3.9K 5% 1/4W CAR FILM

Table 4. Combiner Assembly A4 Parts List (10121-5500-03) (Cont.)

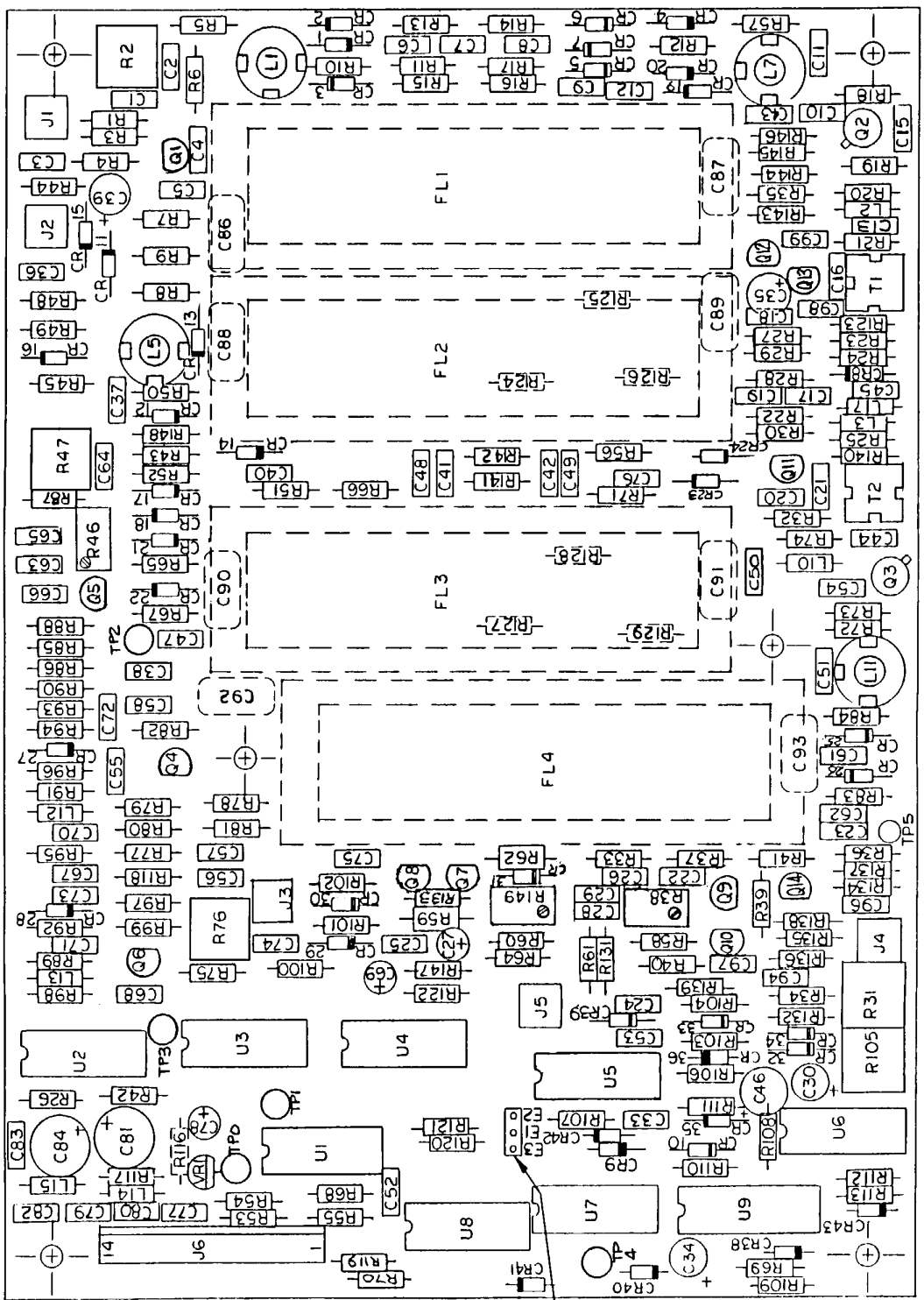
Ref. Desig.	Part Number	Description
R126, R127	R65-0003-153	RES 15K 5% 1/4W CAR FILM
R128	R65-0003-392	RES 3.9K 5% 1/4W CAR FILM
R129	R65-0003-153	RES 15K 5% 1/4W CAR FILM
R131	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R132	R65-0003-152	RES 1.5K 5% 1/4W CAR FILM
R133	R65-0003-241	RES 240 5% 1/4W CAR FILM
R134	R65-0003-101	RES 100 5% 1/4W CAR FILM
R135	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R136	R65-0003-512	RES 5.1K 5% 1/4W CAR FILM
R137	R65-0003-152	RES 1.5K 5% 1/4W CAR FILM
R138	R65-0003-510	RES 51 5% 1/4W CAR FILM
R139	R65-0003-222	RES 2.2K 5% 1/4W CAR FILM
R140	R65-0003-682	RES 6.8K 5% 1/4W CAR FILM
R141, R142	R65-0003-362	RES 3.6K 5% 1/4W CAR FILM
R143	R65-0003-512	RES 5.1K 5% 1/4W CAR FILM
R144	R65-0003-271	RES 270 5% 1/4W CAR FILM
R145	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R146	R65-0003-101	RES 100 5% 1/4W CAR FILM
R147	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R148	R65-0003-152	RES 1.5K 5% 1/4W CAR FILM
R149	R30-0008-503	RES VAR PCB 50K 1/2W 10%
T1, T2	10073-7026	TRANSFORMER, RF, FIXED
TP0	J-0067	TP PWB BLK TOP ACCS .080"
TP1	J-0071	TP PWB BRN TOP ACCS .080"
TP2	J-0066	TP PWB RED TOP ACCS .080"
TP3	J-0069	TP PWB ORN TOP ACCS .080"
TP4	J-0070	TP PWB YEL TOP ACCS .080"
TP5	J-0068	TP PWB GRN TOP ACCS .080"
U1	I01-0000-156	IC 4094B PLASTIC CMOS
U2	I30-0003-000	IC OP AMP QUAD 324
U3	I30-0003-000	IC OP AMP QUAD 324
U4	I30-0003-000	IC OP AMP QUAD 324
U5	I30-0003-000	IC OP AMP QUAD 324
U6	I30-0003-000	IC OP AMP QUAD 324
U7	I01-0000-005	IC 4002B PLASTIC CMOS
U8	I01-0000-003	IC 4001B PLASTIC CMOS
U9	I01-0000-353	IC 4538B PLASTIC CMOS
VR1	I12-0006-005	IC VR 78L05A +5V .10A 4%

Table 5. Optional Combiner Assembly A4 (10121-5500-01 Rev. H) Part Substitutions

Ref. Desig.	Part Number	Description
	10121-5505	INSULATOR, MYLAR
C86, C87		NOT USED
C92, C93		NOT USED
FL1	10073-7311	FLTR XTAL 455 KHZ LSB
FL4	10073-7310	FLTR XTAL 455 KHZ USB

Table 6. Optional Combiner Assembly A4 (10121-5500-04 Rev. B) Part Substitutions

Ref. Desig.	Part Number	Description
	10121-5505	INSULATOR, MYLAR
C86, C87		NOT USED
C92, C93		NOT USED
FL1	10073-7312	FLTR XTAL WIDE LSB
FL4	10073-7313	FLTR XTAL WIDE USB



NOTES:
INSTALL JMP-1, AM/AME JUMPER
FROM E1 - E3 FOR AM
FROM E1 - E2 FOR AME.

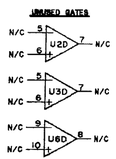
Figure 4. Combiner Assembly A4 Component Location Diagram (10121-5500 Rev. J)

NOTE: UNLESS OTHERWISE SPECIFIED:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR A COMPLETE DESIGNATION, PREFIX WITH UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.
2. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, ±5%.
3. ALL CAPACITOR VALUES ARE IN MICROFARADS.
4. VENDOR PART NO. CALLOUTS ARE FOR REFERENCE ONLY. COMPONENTS ARE SUPPLIED PER PART NO. IN PARTS LIST.
5. ALL UNMARKED DIODES ARE IN4454.
6. SEE PL10121-5500-XX (XX= 01, 02, 03, ETC.) AND 10121-5500 ASSEMBLY DRAWING FOR OPTIONAL CONFIGURATIONS.
7. ALL INDUCTOR VALUES ARE IN MICROHENRYS.

TABLE 1	
MODE	JUMPER 1
AME	E1 TO E2
AM	E1 TO E3

UNUSED GATES



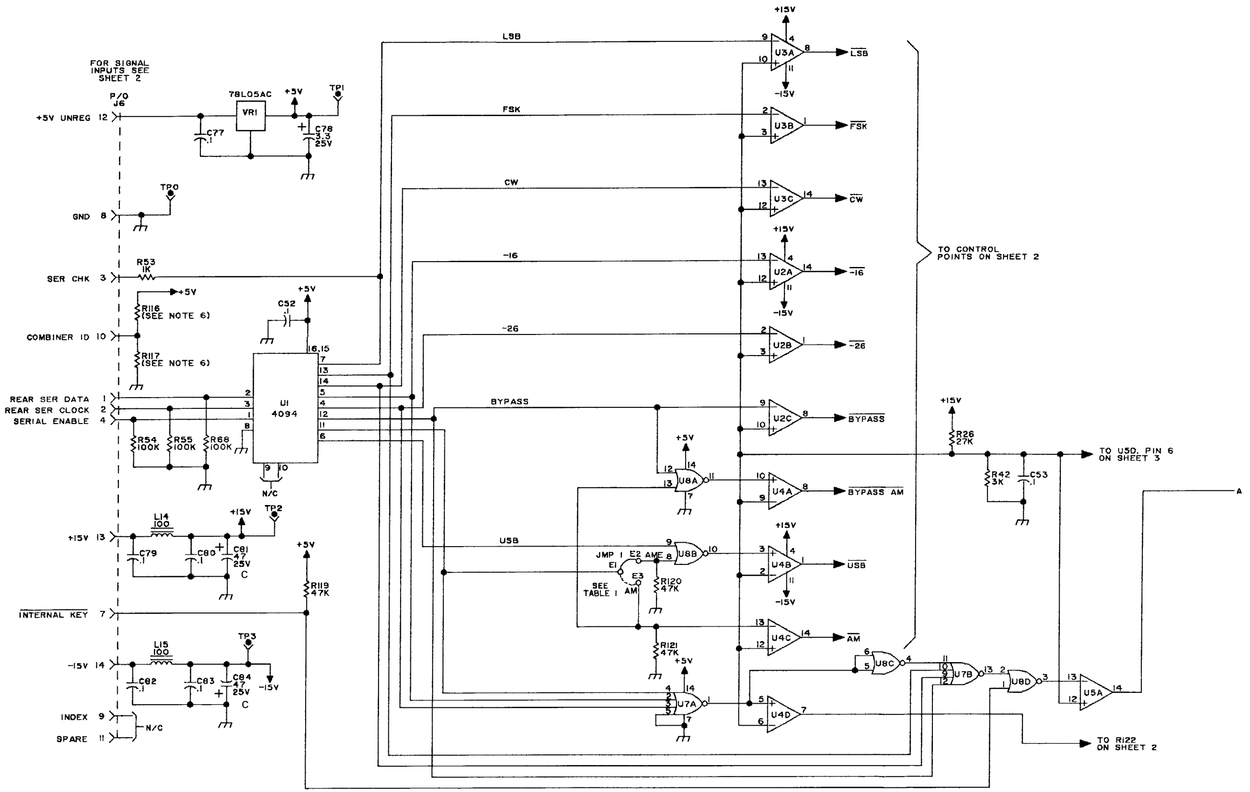


Figure 5. **Combiner Assembly A4 Schematic Diagram (10121-5501 Rev. K) (Sheet 1 of 3)**

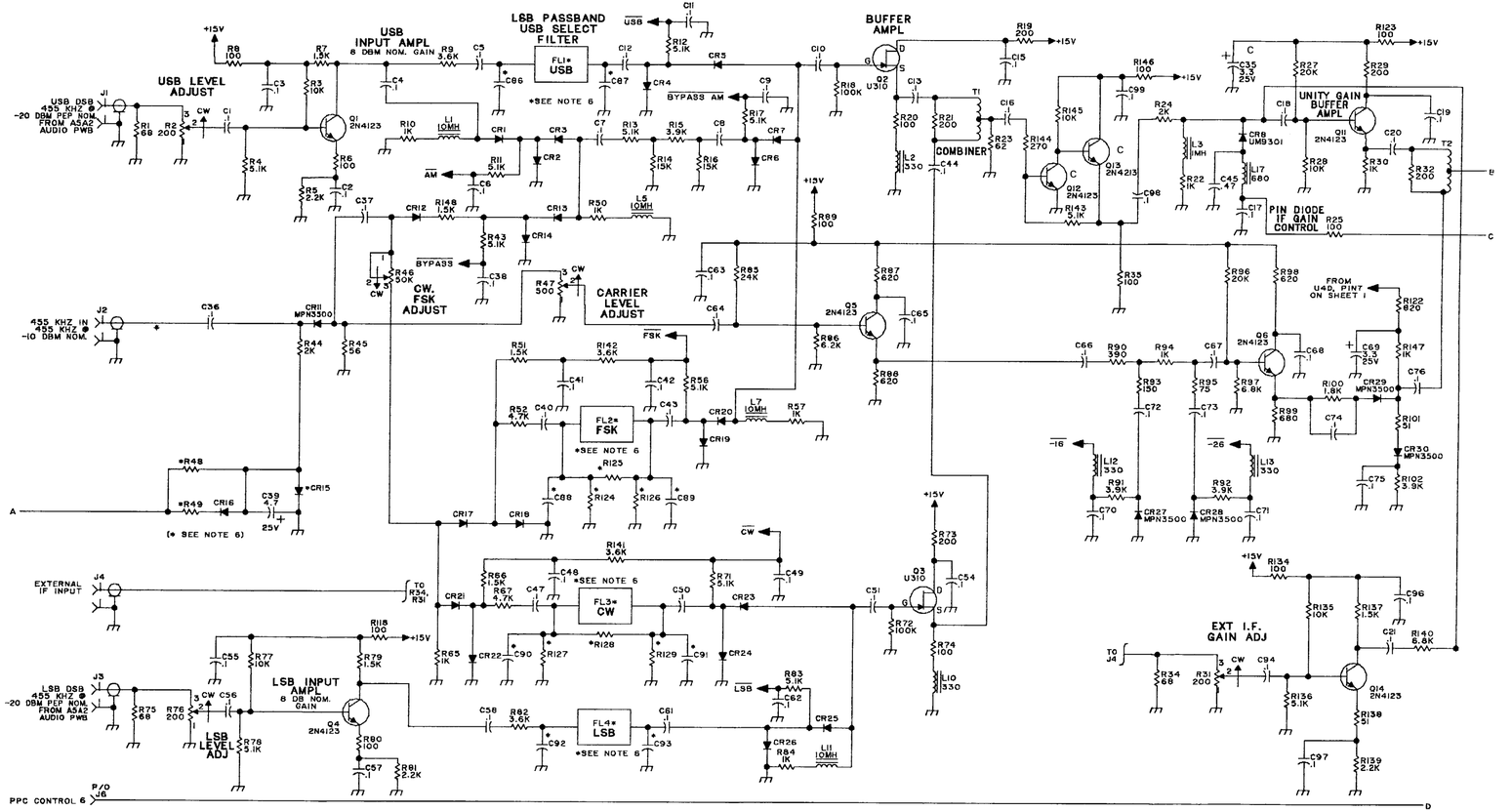


Figure 5. Combiner Assembly A4 Schematic Diagram (10121-5501 Rev. K) (Sheet 2 of 3)

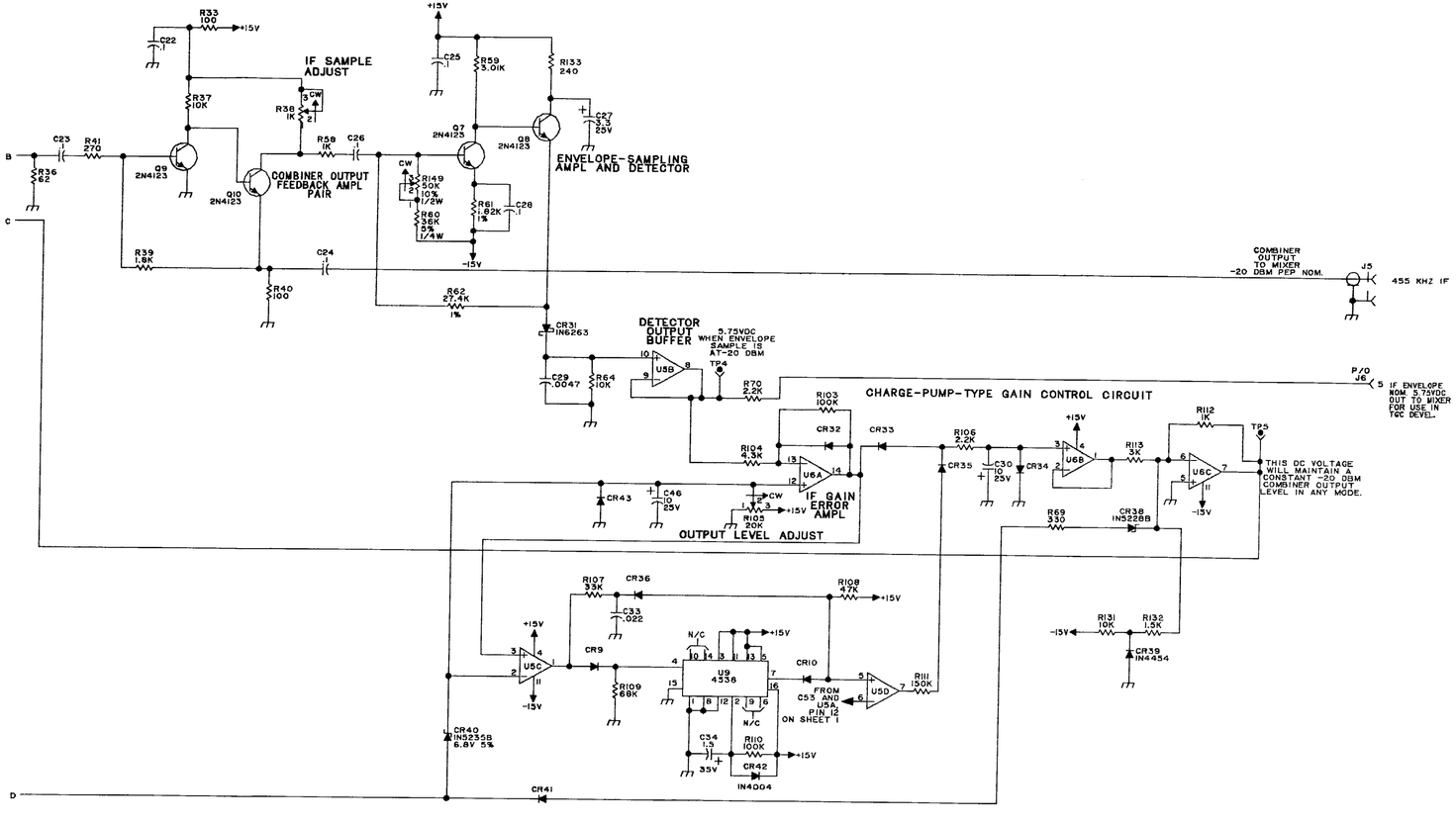
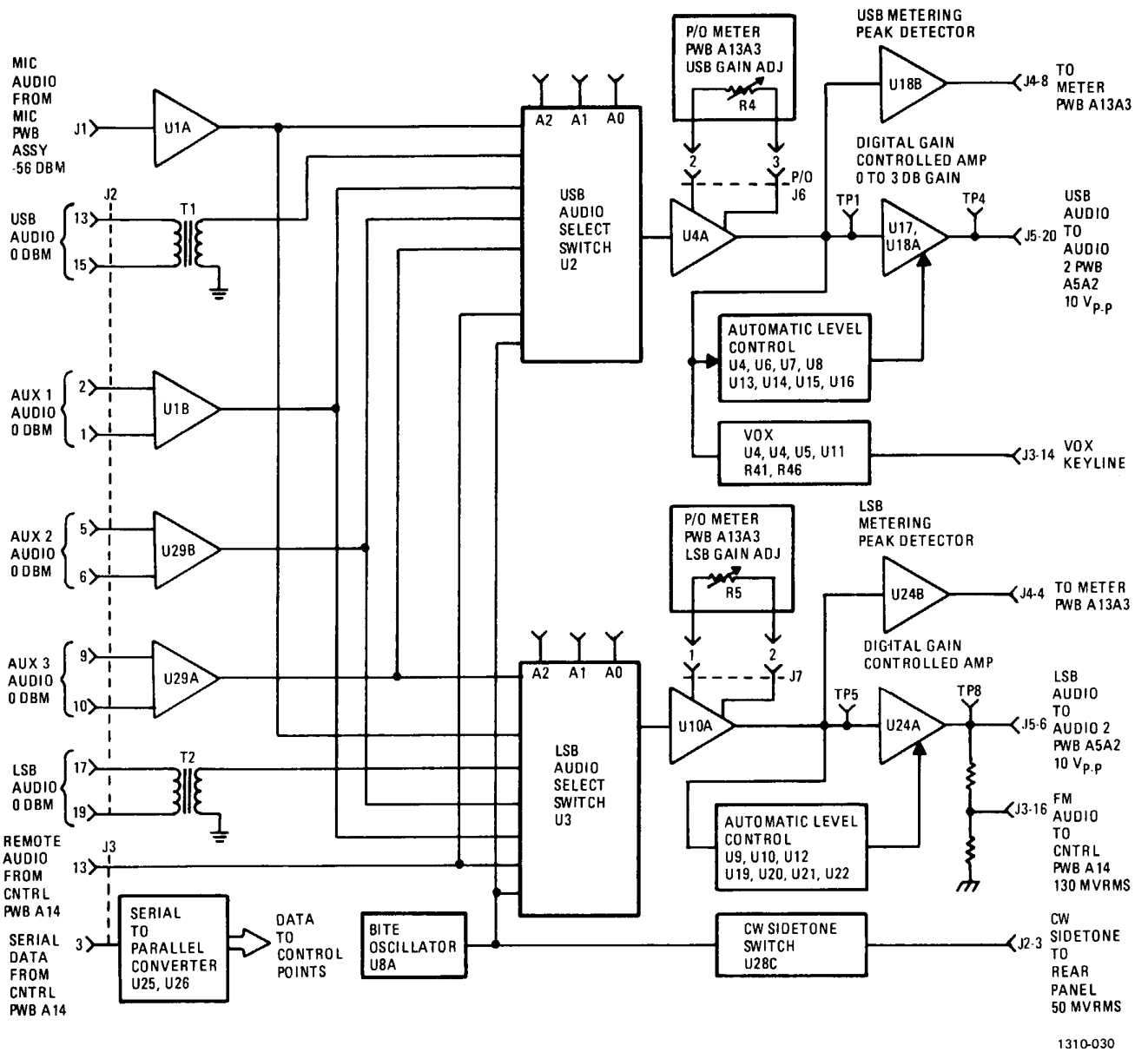


Figure 5. Combiner Assembly A4 Schematic Diagram (10121-5501 Rev. K) (Sheet 3 of 3)

A5A1
AUDIO 1 ASSEMBLY



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AUDIO 1 ASSEMBLY A5A1

1. GENERAL DESCRIPTION

Audio 1/Audio 2 Assembly A5 consists of the following two PWBs:

- Audio 1 Motherboard Assembly A5A1 (10121-5410)
- Audio 2 Assembly A5A2 (10121-5450)

Figure 1 shows the relative position of the A5A1 assembly in the exciter chassis.

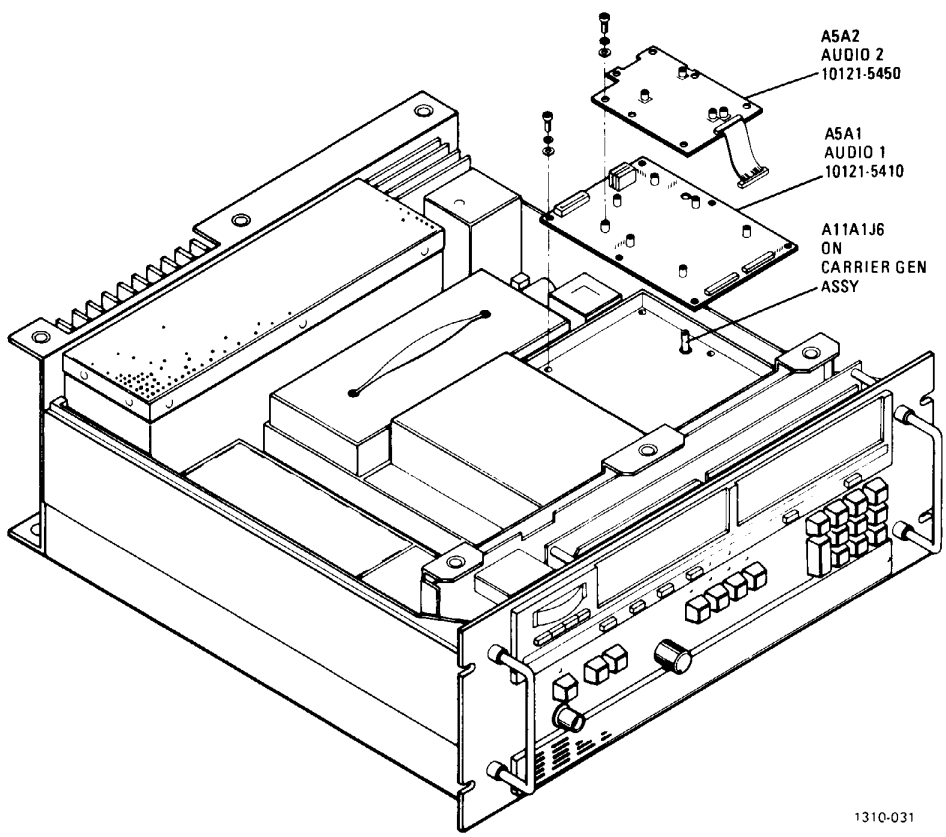


Figure 1. Audio 1 Motherboard Assembly

Audio 1 assembly A5A1 serves as the input to the exciter signal path. It supplies a processed audio output for each sideband to the balanced modulators of the A5A2 assembly. The Audio 1 assembly circuits provide the following functions:

- Audio source selection for each sideband signal path.
- ALC/Manual gain control for each sideband
- VOX operation (USB path only)
- Logarithmic detection of audio levels for metering
- BITE oscillator/CW sidetone generation
- FM audio output (LSB path only)

2. INTERFACE CONNECTIONS

Table 1 details the various input/output connections and other relevant data.

Table 1. Audio 1 Assembly A5A1 Interface Connections

Connector	Function	Characteristics
J1-1	MIC Input	150-ohm nominal; -56 dBm nominal
J1-2	Index Key	
J1-3	MIC GND Return	
J2-1	AUX 1 Audio	600-ohm balanced; 0 dBm nominal
J2-2	AUX 1 Audio	600-ohm balanced; 0 dBm nominal
J2-3	CW Sidetone	600-ohm unbalanced; 50 mV_{rms}
J2-4	Ground	
J2-5	AUX 2 Audio	600-ohm balanced; 0 dBm nominal
J2-6	AUX 2 Audio	600-ohm balanced; 0 dBm nominal
J2-7	+6 V Key	
J2-8	Ground	
J2-9	AUX 3 Audio	600-ohm balanced; 0 dBm nominal
J2-10	AUX 3 Audio	600-ohm balanced; 0 dBm nominal
J2-11	Spare	
J2-12	Spare	
J2-13	USB Audio	600-ohm balanced; 0 dBm nominal
J2-14	USB Audio CT	
J2-15	USB Audio	600-ohm balanced, Trans.; 0 dBm nominal
J2-16	AUX PTT Key	
J2-17	LSB Audio	600-ohm balanced, Trans.; 0 dBm nominal

Table 1. Audio 1 Assembly A5A1 Interface Connections (Cont.)

Connector	Function	Characteristics
J2-18	LSB Audio CT	
J2-19	LSB Audio	600-ohm balanced, Trans.; 0 dBm nominal
J2-20	Spare	
J3-1	Rear Serial Data	0 - 5 Vdc Logic
J3-2	Serial Clock	0 - 5 Vdc Logic
J3-3	A5 Serial Check	0 - 5 Vdc Logic
J3-4	Rear Serial Enable	0 - 5 Vdc Logic
J3-5	Spare	
J3-6	USB ALC BITE	
J3-7	USB IF BITE	
J3-8	LSB ALC BITE	
J3-9	LSB IF BITE	
J3-10	Rem. Line Audio GND	
J3-11	Spare	
J3-12	Spare	
J3-13	Spare	
J3-14	VOX Keyline	0 Vdc Active
J3-15	Ground	
J3-16	FM Audio	130 mV_{rms} nominal
J3-17	Spare	
J3-18	Power, -15 Vdc	
J3-19	Internal Keyline	0 Vdc Active
J3-20	Power, + 15 Vdc	
J3-21	Spare	
J3-22	Clip Enable	+ 5 Vdc Enables clipping
J3-23	Spare	
J3-24	Spare	
J4-1	Log Amp Input	
J4-2	Spare	
J4-3	Ground	
J4-4	LSB Meter Dc	
J4-5	Spare	
J4-6	Spare	
J4-7	Log Amp Output	

Table 1. Audio 1 Assembly A5A1 Interface Connections (Cont.)

Connector	Function	Characteristics
J4-8	USB Meter Dc	
J5-1	Clip Enable	+ 5 Vdc Enable clipping
J5-2	Spare	
J5-3	LSB Carrier Select	+ 5 Vdc Enables LSB carier
J5-4	Spare	
J5-5	Spare	
J5-6	LSB Audio	10 V_{p-p}, nominal
J5-7	Spare	
J5-8	Spare	
J5-9	LSB IF BITE	
J5-10	USB IF BITE	
J5-11	Power, + 5 Vdc	
J5-12	LSB ALC BITE	
J5-13	USB ALC BITE	
J5-14	Spare	
J5-15	Power, -15 Vdc	
J5-16	Spare	
J5-17	Power, + 15 Vdc	
J5-18	Ground	
J5-19	USB Carrier Select	+ 5 Vdc enables USB carrier
J5-20	USB Audio	10 V_{p-p}, nominal
J6-1	Index Key	
J6-2	USB Audio Gain	
J6-3	USB Audio Gain USB Return	
J7-1	LSB Audio Gain	
J7-2	LSB Audio Gain LSB Return	
J7-3	Index Key	

3. A5A1 CIRCUIT DESCRIPTIONS

Figure 2 is a block diagram of the Motherboard circuit.

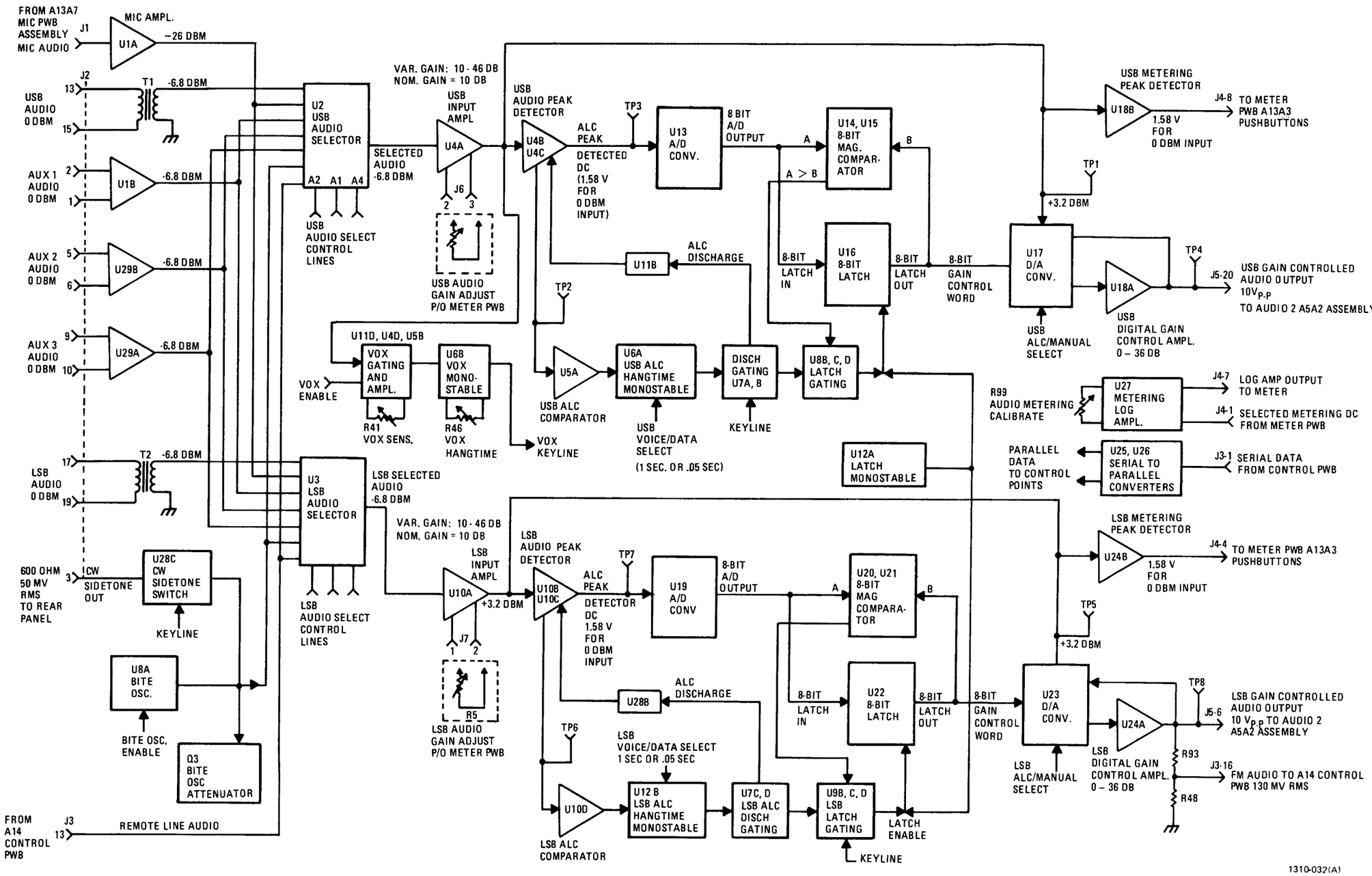


Figure 2. Motherboard Assembly A5A1 Functional Diagram

NOTE

Where circuitry of the USB and LSB signal paths are identical, the USB signal path is described with corresponding components of the LSB signal path included in parenthesis.

3.1 Audio Inputs/Audio Selection

The A5A1 assembly accepts audio signal inputs from any of seven selectable sources. Five balanced 600-ohm inputs are provided at J2. Microphone audio is applied at J1. Table 2 summarizes input characteristics. Remote Line Audio is externally derived and is applied via the Control Board to J2.

Table 2. Audio Inputs

Input	Type	Access	Nom Input
USB	600-ohm balanced; Transformer	Rear Panel	0 dBm
LSB	600-ohm balanced; Transformer	Rear Panel	0 dBm
AUX 1	600-ohm balanced; Differential Amplifier	Rear Panel	0 dBm
AUX 2	600-ohm balanced; Differential Amplifier	Rear Panel	0 dBm
AUX 3	600-ohm balanced; Differential Amplifier	Rear Panel	0 dBm
MIC	150-ohm nominal	Front Panel	-56 dBm

MIC amplifier U1A provides a nominal 30 dB gain. Differential amplifiers U1B, U29A, and U29B and audio transformers T1 and T2 each incur a nominal 6.8 dB loss. Audio selectors U2 and U3 are one of eight switches which route the desired audio source to the USB and LSB signal paths. Source selection for each sideband path is controlled by the Control Board Assembly microprocessor. Table 3 lists the required logic on audio select inputs U2-1, 16, and 15 (U3-1, 16, and 15) which allow the desired audio source to pass to the audio selector output U2-8 (U3-8).

Table 3. Audio Source Select Logic

Selected Audio Source for USB Path	Selected Audio Source for LSB Path	U2 Select Lines			U3 Select Lines		
		A0	A1	A2	A0	A1	A2
USB	LSB	0	0	0	0	0	0
MIC	MIC	0	0	1	0	0	1
AUX 1	AUX 1	0	1	0	0	1	0
AUX 2	AUX 2	0	1	1	0	1	1
AUX 3	AUX 3	1	0	0	1	0	0
BITE OSC.	BITE OSC.	1	0	1	1	0	1
REM. LINE AUD.	REM. LINE AUD.	1	1	0	1	1	0
NONE (MUTE)	NONE (MUTE)	1	1	1	1	1	1

USB Audio Input T1 is dedicated to the USB signal path and cannot be selected for LSB transmission. LSB Audio Input T2 is dedicated to the LSB path and cannot be selected for USB transmission. All other audio inputs are selectable for either or both sideband signal paths.

3.2 ALC Circuit

Each sideband audio path contains identical hang-type Automatic Level Control (ALC) circuits which establish the gain of the audio signal path. The ALC circuit sets the gain so that the audio output is 10 Vp-p for the largest input level applied. U18A (U24A) is configured with A/D converter U17 (U23) to form a digitally controlled variable gain amplifier. All other ALC circuitry controls or supports this amplifier. Audio peak detector U4B and U4C (U10B and U10C), in conjunction with Digital Peak Detector U13, U14, U15, and U16 (U19, U20, U21, and U22), establish the eight-bit digital word applied to D/A converter U17 (U23). When the input signal level falls, monostable multivibrator U6A (U12B) and gates U7A and U7B (U7C and U7D) control the ALC hangtime and gain recovery. Gates U8B, U8C, and U8D (U9B, U9C, and U9D) control latching of the eight-bit digital gain control word into latch U16 (U22). ALC circuit operation can be defeated to yield manual gain control. Directions for programming ALC vs. manual operation are included in the Control PWB Assembly A14 section of this manual.

3.2.1 Audio Input Amplifier

The selected audio signal appearing at U2-8 (U3-8) is low-pass filtered by R21 and C18 (R70 and C43) and coupled to U4A (U10A). The gain of U4A (U10A) may be adjusted over a nominal range of 10 dB to 46 dB via potentiometer R4 (R5) on Meter PWB Assembly A13A3. These potentiometers are accessed, by the operator, at the exciter front panel. When the potentiometers are adjusted fully clockwise, the ALC circuit will control audio input levels within the range of -26 dBm to + 10 dBm.

3.2.2 Audio Peak Detector

U4B and U4C (U10B and U10C) are configured as a precision halfwave rectifier circuit. C48 (C47) charges to the peak level of the audio signal present at U4-1 (U10-1) and the resulting dc voltage at TP3 (TP7) is presented to A/D converter U13 (U19). The peak detector maintains this dc output until the input signal level falls and fails to return to the previous peak level after a specific length of time called the ALC hangtime. After this hangtime is over, the gain recovery circuit is activated.

3.2.3 Gain Recovery Circuit

The gain recovery circuit is responsible for resetting audio path gain when the input signal drops below its previous peak. When the input signal level falls, gain is increased in step recovery fashion. After an initial hangtime, approximately 10 dB of audio gain is restored. The initial hangtime period may be programmed for Voice (1 second) or Data (50 milliseconds) operation as described in the Control PWB Assembly A14 section of this manual. If the input signal has fallen by more than 10 dB, full gain recovery will occur after a fixed secondary hangtime period of approximately 4 seconds.

Stepped gain restoration is achieved by partial discharge (if necessary, full discharge) of C48 (C47). Discharging is performed by activation of switch U11B (U28B). When a steady or increasing audio signal level is present, U4B (U10B) consistently recharges C48 (C47) by producing negative voltage pulses at U4-7 (U10-7). These pulses are amplified by U5A (U10D) and applied as trigger pulses to hangtime monostable multivibrator U6A (U12B). As long as the input signal level does not fall, the hangtime monostable multivibrator will be continuously triggered. Its output U6-6 (U12-6) will remain active high. This logic passes through discharge control gates U7A and U7B (U7C and U7D) and appears at ALC discharge switch U11B (U28B). When the input signal level falls, triggering of U6A (U12B) stops. If the input signal does not return to its previous peak level within the initial hangtime period, the U6A (U12B) output will go low at the end of the initial hangtime period. This causes a short pulse to be applied to ALC discharge switch U11B (U28B) via discharge gates U7A

and U7B (U7C and U7D). The discharge switch is closed only for this short pulse time and only partially discharges C48 (C47) to yield an approximate 10 dB gain recovery. R38 and C23 (R88 and C51) control the duration of the discharge pulse. If the input signal has fallen by more than 10 dB, further discharge of C48 (C47) is necessary to yield further gain recovery. Approximately 4 seconds after the partial discharge is completed, discharge switch U11B (U28B) is closed and held in that state until the gain has recovered to the level appropriate for the new lower input level. Sufficient discharge of the ALC capacitor is signalled by the reappearance of negative voltage pulses at U4-7 (U10-7) which in turn retrigger U6A (U12B). R39 and C24 (R89 and C52) set the secondary hangtime to 4 seconds.

3.2.4 Digital Peak Detector

A/D converter U13 (U19) converts the dc output of the audio peak detector to a corresponding eight-bit word which is applied to D/A converter U17 (U23) via latch U16 (U22). Latch U16 (U22) holds the largest magnitude eight-bit word produced by A/D converter U13 (U19). The latch ignores smaller A/D outputs unless an ALC discharge (gain recovery) is in progress. U14 and U15 (U20 and U21) are configured as an eight-bit magnitude comparator which compares the present latch contents to the present A/D converter output. If the A/D converter outputs a word which is larger than that in the latch, the magnitude comparator activates gate U8B (U9B) allowing clock pulses supplied by U13-19 (U19-19) to pass through U8D (U9D). These pulses clock the larger word into the latch and stop when the latched word equals the present A/D output word. If the A/D converter outputs a smaller word than that in the latch, no clock pulses are applied unless an ALC discharge is in progress. ALC discharge activity is signalled by a logic low at U7-4 (U7-11), the same signal which activates ALC discharge switch U11B (U28B) as described in paragraph 3.2.3. When ALC discharge is occurring, clock pulses are applied to latch U16 (U22) via U8D (U9D). These pulses continuously clock the present A/D converter output word into the latch regardless of its magnitude for the duration of the discharge.

Monostable multivibrator U12A applies a clock pulse to latch U16 (U22) at 2.5 second intervals thereby forcing the latch to copy the present A/D converter output word regardless of relative magnitudes or ALC discharge activity.

3.2.5 Digitally Controlled Output Amplifier

D/A converter U17 (U23) and current to voltage converter U18A (U24A) are configured as a digitally controlled amplifier whose eight-bit gain control word is supplied by latch U16 (U22). The magnitude of the eight-bit word applied to U17 (U23) determines the gain of the amplifier. The amplifier, in conjunction with the audio peak detector and digital peak detector circuits, automatically sets its gain to yield an audio output level of 10 Vp-p for the largest audio input signal level encountered. The eight-bit control word will vary from decimal values of 4 to 255 for corresponding audio input levels from -26 dBm to + 10 dBm. A control word magnitude of 255 indicates that A/D converter U13 (U19) is receiving the largest possible dc input (+ 5 V) from the audio peak detector, corresponding to an audio input level of + 10 dBm. In this case, the gain of the amplifier is set to unity and the output is 10 V_{p-p}. Smaller audio input levels will yield correspondingly smaller magnitude control words and will set the gain in inverse proportion to the smaller input level. The output of amplifier U18A (U24A) is presented to the balanced modulators of the Audio 2 Assembly A5A2 for translation to 455 kHz.

3.3 Manual Gain Control

Upon command from Control PWB Assembly A14, the outputs of latch U16 (U22) are disabled (high impedance state) by a logic high at U16-1 (U22-1). The latch outputs are pulled down by R121 (R122) yielding a gain control word of decimal magnitude 4 applied to D/A converter U17 (U23). This word increases the gain of the output amplifier to maximum, leaving the gain of the audio path to be manually set by the operator via front panel adjustments. The front panel adjustment controls the gain of U4A (U10A) as described in paragraph 3.2.1. The Audio 1 PWB may be programmed for ALC or manual gain control as described in the Control PWB Assembly A14 section of this manual.

3.4 VOX Circuit

The USB audio path contains a traffic detector consisting of U4D, U5B, U6B, and U11D. The VOX circuit is enabled and disabled according to programming as described in the Control PWB Assembly A14 section of this manual. When VOX is enabled, switch U11D is off, allowing the full magnitude of the audio signal at U4-1 to be applied to buffer U4D. The buffered audio is amplified by U5B, whose gain is adjustable by the operator at R41, VOX Sensitivity Adjust. For an audio input level in the range -26 dBm to + 10 dBm, R41 is adjusted so that the output of U5B is large enough to trigger monostable multivibrator U6B. Upon triggering, VOX Keyline U6B goes low to key the exciter. If the input signal level falls below the adjusted threshold, the VOX Keyline will remain active for a delay time period set by adjustment of R46, VOX Hangtime Adjust. The delay time is nominally adjustable from 100 milliseconds to 3.0 seconds.

3.5 Audio Metering Detector/Amplifier

The Audio 1 PWB provides metering voltages proportional to the logarithm of the audio input level in each sideband path. U18B (U24B) is a half-wave peak detector which produces a dc output equal to the peak value of the audio signal at J6-2 (J7-2). The detected dc voltages for each sideband are sent to Meter PWB Assembly A13A3 where front panel pushbutton switches select which of the two metering dc voltages (USB or LSB) is returned to logarithmic amplifier U27. Logarithmic amplifier U27 produces a dc output proportional to the log of the selected dc input and returns the processed dc to Meter PWB Assembly A13A3 to display the audio input level on the front panel meter.

3.6 BITE Oscillator

U8A produces a nominal 0 to 5 V square wave used as an audio signal source during BITE testing. The oscillator is activated from the Control PWB Assembly by a logic high at U8-1. This logic high is also applied to switch U11A (U28D) to set the output of U4A (U10A) at a fixed level (as required for BITE testing). During BITE testing, Control PWB Assembly A14 commands selection of the BITE oscillator as an audio source by applying the proper audio select logic signals as listed in table 3. Q3 is activated during BITE testing to yield a lower BITE oscillator output used in verifying proper ALC circuit gain recovery.

3.7 CW Sidetone

The BITE oscillator tone provides an audio signal which may be monitored during CW transmission. When CW mode is selected, the BITE oscillator is active and, upon keying of the exciter, its output is gated through U28C to the rear panel.

3.8 Control Circuit

U25 and U26 are eight-bit, serial-to-parallel converters which accept a serial data stream from Control PWB Assembly A14 and distribute the received data to the various Audio 1 PWB circuits. The Control PWB Assembly A14 microprocessor determines the proper data to be sent to U25 and U26 for desired programming of Audio 1 PWB operations.

3.9 FM Audio

The gain controlled output of U24A is attenuated by R93 and R48 and sent to Carrier Generator PWB Assembly A11 via Control PWB Assembly A14 for production of FM signals.

4. MAINTENANCE

The following adjustments should not be performed as routine maintenance procedures, but only when a failure indicates a definite need. All tests are performed with all assembly connections in normal contact unless otherwise specified.

4.1 Audio Metering Calibration

a. Connect equipment as shown in figure 3. Set audio generator to 1 kHz, -30 dBm.

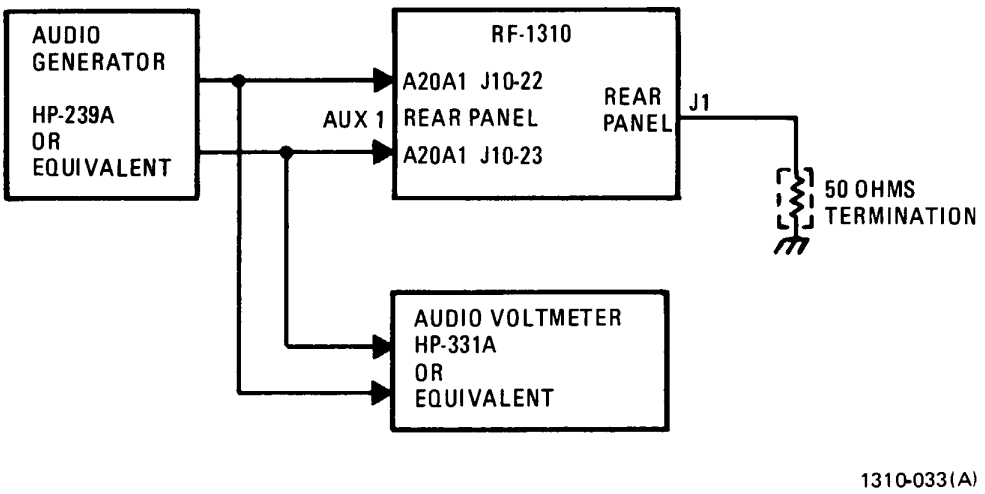


Figure 3. Audio Metering Calibration Setup

b. Set meter function front panel pushbuttons to USB.

c. Set RF-1310 front panel controls as follows:

- FUNCTION switch to NORM
- MODE to USB
- USB audio source to AUX 1
- USB Audio Level Adjust fully clockwise

d. Adjust R99 to a -30 dBm reading on front panel meter. Audio metering calibration is now complete.

4.2 BITE Test

Activate RF-1310 self test. Exciter must pass all tests associated with the A5A1 assembly. Refer to section 5 maintenance section of this manual for explanation of A5 assembly BITE fault codes. Test is now complete.

5. PARTS LIST, COMPONENT LOCATIONS, AND SCHEMATIC DIAGRAM

All replaceable components of Motherboard assembly A5A1 are listed in table 4. Component locations are shown in figure 4. The Audio 1 Motherboard assembly schematic diagram is shown in figure 5.

Table 4. Audio 1 Motherboard Assembly A5A1 Parts List (10121-5410 Rev. U)

Ref. Desig.	Part Number	Description
C1	C26-0025-100	CAP 10UF 20% 25V TANT
C2	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C3	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C4	M39014/01-1299V	CAP 100PF 10% 200V CER-R
C5	M39014/02-1320V	CAP .47UF 10% 50V CER-R
C6	M39014/02-1320V	CAP .47UF 10% 50V CER-R
C7	M39014/02-1320V	CAP .47UF 10% 50V CER-R
C8	M39014/02-1320V	CAP .47UF 10% 50V CER-R
C9	M39014/02-1320V	CAP .47UF 10% 50V CER-R
C10	M39014/02-1320V	CAP .47UF 10% 50V CER-R
C11	M39014/02-1302V	CAP .022UF 10% 100V CER-R
C12	M39014/02-1302V	CAP .022UF 10% 100V CER-R
C13	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C14	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C15	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C16	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C17	C26-0025-339	CAP 3.3UF 20% 25V TANT
C18	M39014/02-1298V	CAP .01UF 10% 200V CER-R
C19	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C20	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C21	C26-0025-339	CAP 3.3UF 20% 25V TANT
C22	C26-0025-339	CAP 3.3UF 20% 25V TANT
C23	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C24	C26-0025-100	CAP 10UF 20% 25V TANT
C25	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C26	C26-0016-689	CAP 6.8UF 20% 16V TANT
C27	C26-0025-339	CAP 3.3UF 20% 25V TANT
C28	M39014/01-1320V	CAP 1500PF 10% 100V CER-R
C29	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C30	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C31	C26-0025-339	CAP 3.3UF 20% 25V TANT
C32	C26-0025-339	CAP 3.3UF 20% 25V TANT
C33	M39014/02-1303V	CAP .033UF 10% 100V CER-R
C34	M39014/02-1298V	CAP .01UF 10% 200V CER-R

Table 4. Audio 1 Motherboard Assembly A5A1 Parts List (10121-5410 Rev. U) (Cont.)

Ref. Desig.	Part Number	Description
C35	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C36	C26-0025-100	CAP 10UF 20% 25V TANT
C37	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C38	C26-0025-100	CAP 10UF 20% 25V TANT
C39	C26-0025-100	CAP 10UF 20% 25V TANT
C40	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C41	C26-0025-100	CAP 10UF 20% 25V TANT
C42	C26-0025-100	CAP 10UF 20% 25V TANT
C43	M39014/02-1298V	CAP .01UF 10% 200V CER-R
C44	C26-0025-339	CAP 3.3UF 20% 25V TANT
C45	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C46	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C47	M39014/02-1320V	CAP .47UF 10% 50V CER-R
C48	M39014/02-1320V	CAP .47UF 10% 50V CER-R
C49	C26-0025-339	CAP 3.3UF 20% 25V TANT
C50	C26-0025-339	CAP 3.3UF 20% 25V TANT
C51	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C52	C26-0025-100	CAP 10UF 20% 25V TANT
C53	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C54	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C55	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C56	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C57	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C58	C26-0025-339	CAP 3.3UF 20% 25V TANT
C59	C26-0025-339	CAP 3.3UF 20% 25V TANT
C60	C26-0025-339	CAP 3.3UF 20% 25V TANT
C61	C26-0025-100	CAP 10UF 20% 25V TANT
C63	C26-0025-339	CAP 3.3UF 20% 25V TANT
C64	C26-0025-100	CAP 10UF 20% 25V TANT
CR1	1N6263	DIODE .40W 60V HOT CARR
CR2	1N6263	DIODE .40W 60V HOT CARR
CR3	1N4454	DIODE 200MA 75V SW
CR4	1N4454	DIODE 200MA 75V SW
CR5	1N4454	DIODE 200MA 75V SW
CR6	1N4454	DIODE 200MA 75V SW
CR7	1N4454	DIODE 200MA 75V SW
CR8	1N4454	DIODE 200MA 75V SW
CR9	1N4454	DIODE 200MA 75V SW
CR10	1N4454	DIODE 200MA 75V SW
CR11	1N4454	DIODE 200MA 75V SW
CR12	1N4454	DIODE 200MA 75V SW
CR13	1N4454	DIODE 200MA 75V SW
CR14	1N6263	DIODE .40W 60V HOT CARR
CR15	1N4454	DIODE 200MA 75V SW

Table 4. Audio 1 Motherboard Assembly A5A1 Parts List (10121-5410 Rev. U) (Cont.)

Ref. Desig.	Part Number	Description
CR16	1N4454	DIODE 200MA 75V SW
CR17	1N4454	DIODE 200MA 75V SW
CR18	1N6263	DIODE .40W 60V HOT CARR
CR19	1N6263	DIODE .40W 60V HOT CARR
CR20	1N6263	DIODE .40W 60V HOT CARR
CR21	1N4454	DIODE 200MA 75V SW
CR22	1N4454	DIODE 200MA 75V SW
CR23	1N4454	DIODE 200MA 75V SW
CR24	1N4454	DIODE 200MA 75V SW
CR25	1N4454	DIODE 200MA 75V SW
CR26	1N4454	DIODE 200MA 75V SW
CR27	1N4454	DIODE 200MA 75V SW
CR28	1N4454	DIODE 200MA 75V SW
CR29	1N4454	DIODE 200MA 75V SW
CR30	1N4454	DIODE 200MA 75V SW
CR31	1N4454	DIODE 200MA 75V SW
CR32	1N6263	DIODE .40W 60V HOT CARR
CR33	1N4454	DIODE 200MA 75V SW
CR34	1N4454	DIODE 200MA 75V SW
CR35	1N4454	DIODE 200MA 75V SW
CR36	1N6263	DIODE .40W 60V HOT CARR
CR37	1N6263	DIODE .40W 60V HOT CARR
CR38	1N5235B	DIODE 6.8V 5% .5W ZENER
CR39	1N5235B	DIODE 6.8V 5% .5W ZENER
CR40	1N5235B	DIODE 6.8V 5% .5W ZENER
CR41	1N5235B	DIODE 6.8V 5% .5W ZENER
J1	J46-0022-003	HDR 3 PIN 0.100" SR LKG
J2	J46-0013-020	HDR 20 PIN 0.100" DR SHRD
J3	J46-0013-024	HDR 24 PIN 0.100" DR SHRD
J4	J46-0032-008	HDR 8 PIN 0.100" SR
J5	J46-0013-020	HDR 20 PIN 0.100" DR SHRD
J6	J46-0022-003	HDR 3 PIN 0.100" SR LKG
J7	J46-0022-004	HDR 4 PIN 0.100" SR LKG
JMP1	MP-1142	RES ZERO OHM (CKT JMPR)
JMP2	MP-1142	RES ZERO OHM (CKT JMPR)
Q1	2N2222A	XSTR SS/GP NPN TO-18
Q2	2N2222A	XSTR SS/GP NPN TO-18
Q3	2N2222A	XSTR SS/GP NPN TO-18
R1	R65-0003-151	RES 150 5% 1/4W CAR FILM
R2	R65-0003-392	RES 3.9K 5% 1/4W CAR FILM
R3	R65-0003-681	RES 680 5% 1/4W CAR FILM
R4	R65-0003-682	RES 6.8K 5% 1/4W CAR FILM
R5	R65-0003-103	RES 10K 5% 1/4W CAR FILM

Table 4. Audio 1 Motherboard Assembly A5A1 Parts List (10121-5410 Rev. U) (Cont.)

Ref. Desig.	Part Number	Description
R6	R65-0003-133	RES 13K 5% 1/4W CAR FILM
R7	R65-0003-133	RES 13K 5% 1/4W CAR FILM
R8	R65-0003-622	RES 6.2K 5% 1/4W CAR FILM
R9	R65-0003-622	RES 6.2K 5% 1/4W CAR FILM
R10	R65-0003-133	RES 13K 5% 1/4W CAR FILM
R11	R65-0003-133	RES 13K 5% 1/4W CAR FILM
R12	R65-0003-622	RES 6.2K 5% 1/4W CAR FILM
R13	R65-0003-622	RES 6.2K 5% 1/4W CAR FILM
R14	R65-0003-133	RES 13K 5% 1/4W CAR FILM
R15	R65-0003-133	RES 13K 5% 1/4W CAR FILM
R16	R65-0003-622	RES 6.2K 5% 1/4W CAR FILM
R17	R65-0003-622	RES 6.2K 5% 1/4W CAR FILM
R18	R65-0003-181	RES 180 5% 1/4W CAR FILM
R19	R65-0003-181	RES 180 5% 1/4W CAR FILM
R20	R65-0003-473	RES 47K 5% 1/4W CAR FILM
R21	R65-0003-122	RES 1.2K 5% 1/4W CAR FILM
R22	R65-0003-104	RES 100K 5% 1/4W CAR FILM
R23	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R24	RN55D2002F	RES 20.0K 1% 1/8W MET FLM
R25	RN55D2002F	RES 20.0K 1% 1/8W MET FLM
R26	R65-0003-105	RES 1.0M 5% 1/4W CAR FILM
R27	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R28	R65-0003-101	RES 100 5% 1/4W CAR FILM
R29	R65-0003-104	RES 100K 5% 1/4W CAR FILM
R30	R65-0003-821	RES 820 5% 1/4W CAR FILM
R31	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R32	R65-0003-153	RES 15K 5% 1/4W CAR FILM
R33	R65-0003-473	RES 47K 5% 1/4W CAR FILM
R34	R65-0003-473	RES 47K 5% 1/4W CAR FILM
R35	R65-0003-334	RES 330K 5% 1/4W CAR FILM
R36	R65-0003-682	RES 6.8K 5% 1/4W CAR FILM
R37	R65-0003-101	RES 100 5% 1/4W CAR FILM
R38	R65-0003-824	RES 820K 5% 1/4W CAR FILM
R39	R65-0003-624	RES 620K 5% 1/4W CAR FILM
R40	R65-0003-333	RES 33K 5% 1/4W CAR FILM
R41	R30-0008-105	RES VAR PCB 1M 1/2W 10%
R42	R65-0003-153	RES 15K 5% 1/4W CAR FILM
R43	R65-0003-473	RES 47K 5% 1/4W CAR FILM
R44	R65-0003-473	RES 47K 5% 1/4W CAR FILM
R45	R65-0003-223	RES 22K 5% 1/4W CAR FILM
R46	R30-0008-105	RES VAR PCB 1M 1/2W 10%
R47	RN55D2493F	RES 249K 1% 1/8W MET FLM
R48	R65-0003-392	RES 3.9K 5% 1/4W CAR FILM

Table 4. Audio 1 Motherboard Assembly A5A1 Parts List (10121-5410 Rev. U) (Cont.)

Ref. Desig.	Part Number	Description
R49	R65-0003-473	RES 47K 5% 1/4W CAR FILM
R50	R65-0003-471	RES 470 5% 1/4W CAR FILM
R51	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R52	R65-0003-153	RES 15K 5% 1/4W CAR FILM
R53	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R54	R65-0003-224	RES 220K 5% 1/4W CAR FILM
R55	R65-0003-823	RES 82K 5% 1/4W CAR FILM
R56	R65-0003-473	RES 47K 5% 1/4W CAR FILM
R57	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R58	R65-0003-474	RES 470K 5% 1/4W CAR FILM
R59	R65-0003-823	RES 82K 5% 1/4W CAR FILM
R60	RN55D6192F	RES 61.9K 1% 1/8W MET FLM
R61	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R62	R65-0003-101	RES 100 5% 1/4W CAR FILM
R63	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R64	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R65	R65-0003-473	RES 47K 5% 1/4W CAR FILM
R66	R65-0003-333	RES 33K 5% 1/4W CAR FILM
R67	R65-0003-333	RES 33K 5% 1/4W CAR FILM
R68	R65-0003-333	RES 33K 5% 1/4W CAR FILM
R69	R65-0003-473	RES 47K 5% 1/4W CAR FILM
R70	R65-0003-122	RES 1.2K 5% 1/4W CAR FILM
R71	R65-0003-104	RES 100K 5% 1/4W CAR FILM
R72	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R73	RN55D2002F	RES 20.0K 1% 1/8W MET FLM
R74	RN55D2002F	RES 20.0K 1% 1/8W MET FLM
R75	R65-0003-105	RES 1.0M 5% 1/4W CAR FILM
R76	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R77	R65-0003-101	RES 100 5% 1/4W CAR FILM
R78	R65-0003-104	RES 100K 5% 1/4W CAR FILM
R79	R65-0003-821	RES 820 5% 1/4W CAR FILM
R80	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R81	R65-0003-153	RES 15K 5% 1/4W CAR FILM
R82	R65-0003-473	RES 47K 5% 1/4W CAR FILM
R83	R65-0003-473	RES 47K 5% 1/4W CAR FILM
R84	R65-0003-334	RES 330K 5% 1/4W CAR FILM
R85	R65-0003-682	RES 6.8K 5% 1/4W CAR FILM
R86	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R87	R65-0003-101	RES 100 5% 1/4W CAR FILM
R88	R65-0003-824	RES 820K 5% 1/4W CAR FILM
R89	R65-0003-624	RES 620K 5% 1/4W CAR FILM
R90	R65-0003-224	RES 220K 5% 1/4W CAR FILM
R91	R65-0003-103	RES 10K 5% 1/4W CAR FILM

Table 4. Audio 1 Motherboard Assembly A5A1 Parts List (10121-5410 Rev. U) (Cont.)

Ref. Desig.	Part Number	Description
R92	R65-0003-473	RES 47K 5% 1/4W CAR FILM
R93	R65-0003-104	RES 100K 5% 1/4W CAR FILM
R94	R65-0003-101	RES 100 5% 1/4W CAR FILM
R95 – R97	R65-0003-473	RES 47K 5% 1/4W CAR FILM
R98	R65-0003-124	RES 120K 5% 1/4W CAR FILM
R99	R30-0008-504	RES VAR PCB 500K 1/2W 10%
R100	RN55D4021F	RES 4020 1% 1/8W MET FLM
R101, R102	R65-0003-333	RES 33K 5% 1/4W CAR FILM
R103	RN55D7502F	RES 75.0K 1% 1/8W MET FLM
R104	R65-0003-303	RES 30K 5% 1/4W CAR FILM
R105	R65-0003-154	RES 150K 5% 1/4W CAR FILM
R106	R65-0003-223	RES 22K 5% 1/4W CAR FILM
R107	R65-0003-623	RES 62K 5% 1/4W CAR FILM
R108	R65-0003-622	RES 6.2K 5% 1/4W CAR FILM
R109	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R110	R65-0003-242	RES 2.4K 5% 1/4W CAR FILM
R111	R65-0003-302	RES 3.0K 5% 1/4W CAR FILM
R112, R113	RN55D7502F	RES 75.0K 1% 1/8W MET FLM
R114	R65-0003-393	RES 39K 5% 1/4W CAR FILM
R115 – R117	RN55D6040F	RES 604 1% 1/8W MET FLM
R118	R65-0003-104	RES 100K 5% 1/4W CAR FILM
R119	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R120	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R121, R122	R50-0010-104	RES 100K 2% 10SIP 9RES
R123	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R124	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R125	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R126	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R127	R65-0003-223	RES 22K 5% 1/4W CAR FILM
R128	R65-0003-511	RES 510 5% 1/4W CAR FILM
R129	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R130, R131	R65-0003-104	RES 100K 5% 1/4W CAR FILM
R132, R133	R65-0003-335	RES 3.3M 5% 1/4W CAR FILM
T1, T2	10121-5415	TRANSFORMER,AUDIO,SHIELDE
TP1	J-0071	TP PWB BRN TOP ACCS .080"
TP2	J-0066	TP PWB RED TOP ACCS .080"
TP3	J-0069	TP PWB ORN TOP ACCS .080"
TP4	J-0070	TP PWB YEL TOP ACCS .080"
TP5	J-0068	TP PWB GRN TOP ACCS .080"
TP6	J-0072	TP PWB BLU TOP ACCS .080"
TP7	J-0073	TP PWB VIO TOP ACCS .080"
TP8	J-0074	TP PWB GRA TOP ACCS .080"
U1	I30-0035-000	IC OP AMP QUAD 072

Table 4. Audio 1 Motherboard Assembly A5A1 Parts List (10121-5410 Rev. U) (Cont.)

Ref. Desig.	Part Number	Description
U2, U3	I09-0011-001	INTERGRATED CIRCUIT
U4	I30-0038-001	IC OP AMP QUAD 347
U5	I30-0035-000	IC OP AMP QUAD 072
U6	I01-0000-353	IC 4538B PLASTIC CMOS
U7	I01-0000-003	IC 4001B PLASTIC CMOS
U8	10121-5412	IC 4093 SCHMITT TRIG PLA
U9	I01-0000-351	IC 4093B PLASTIC CMOS
U10	I30-0038-001	IC OP AMP QUAD 347
U11	I06-0002-001	IC DG211 ANALOG SW QUAD
U12	I01-0000-353	IC 4538B PLASTIC CMOS
U13	I03-0011-000	IC ADC0804 A/D CONV PLA
U14, U15	I01-0000-308	IC 4585B PLASTIC CMOS
U16	I05-0019-000	IC 54C374 CERAMIC CMOS
U17	I03-0012-000	IC 7523 D/A CONV 8BIT PLA
U18	I30-0035-000	IC OP AMP QUAD 072
U19	I03-0011-000	IC ADC0804 A/D CONV PLA
U20, U21	I01-0000-308	IC 4585B PLASTIC CMOS
U22	I05-0019-000	IC 54C374 CERAMIC CMOS
U23	I03-0012-000	IC 7523 D/A CONV 8BIT PLA
U24	I30-0035-000	IC OP AMP QUAD 072
U25, U26	I01-0000-156	IC 4094B PLASTIC CMOS
U27	I30-0038-001	IC OP AMP QUAD 347
U28	I06-0002-001	IC DG211 ANALOG SW QUAD
U29	I30-0035-000	IC OP AMP QUAD 072
VR1	I12-0006-005	IC VR 78L05A +5V .10A 4%
VR2	1N5228B	DIODE 3.9V 5% .5W ZENER

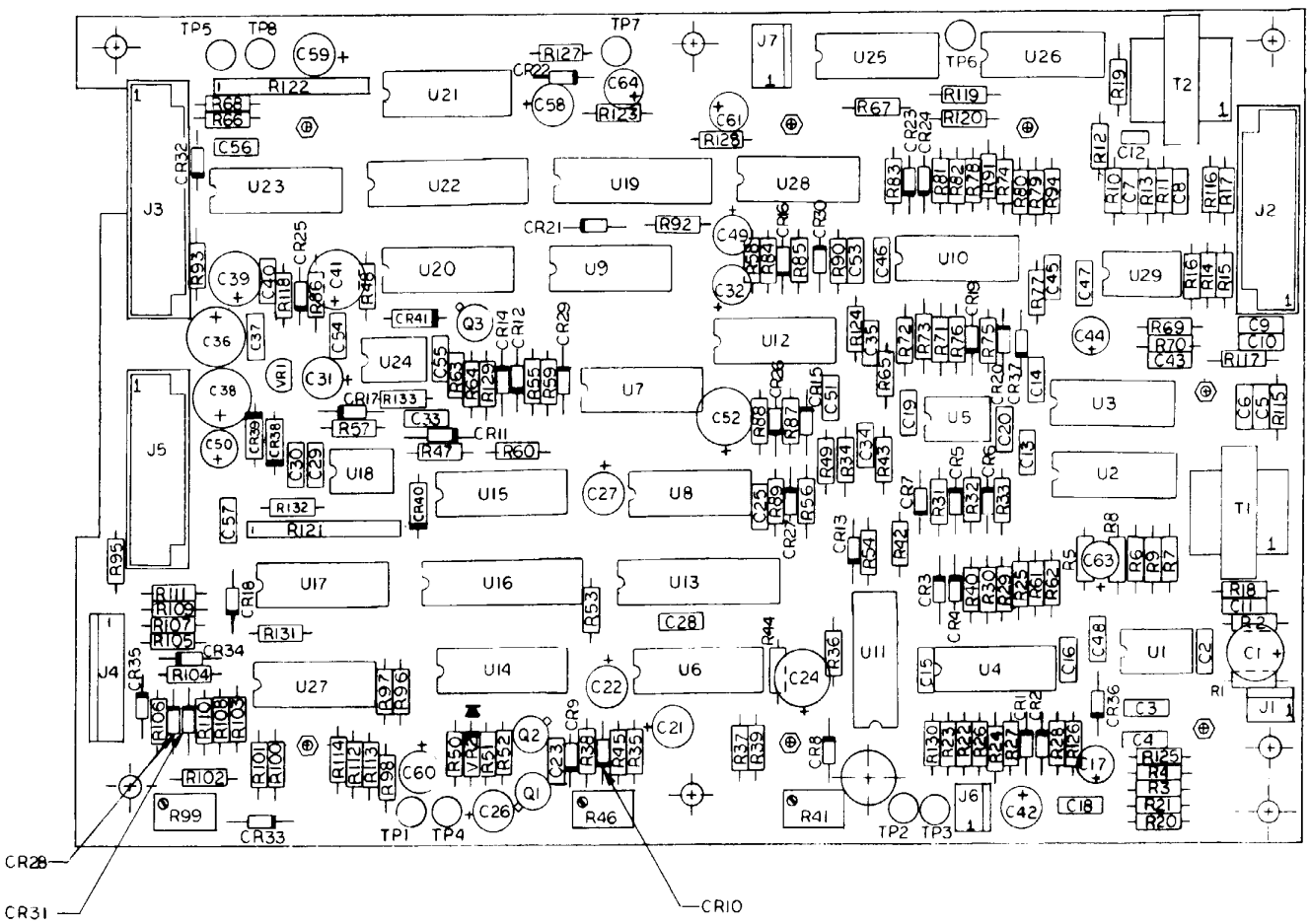
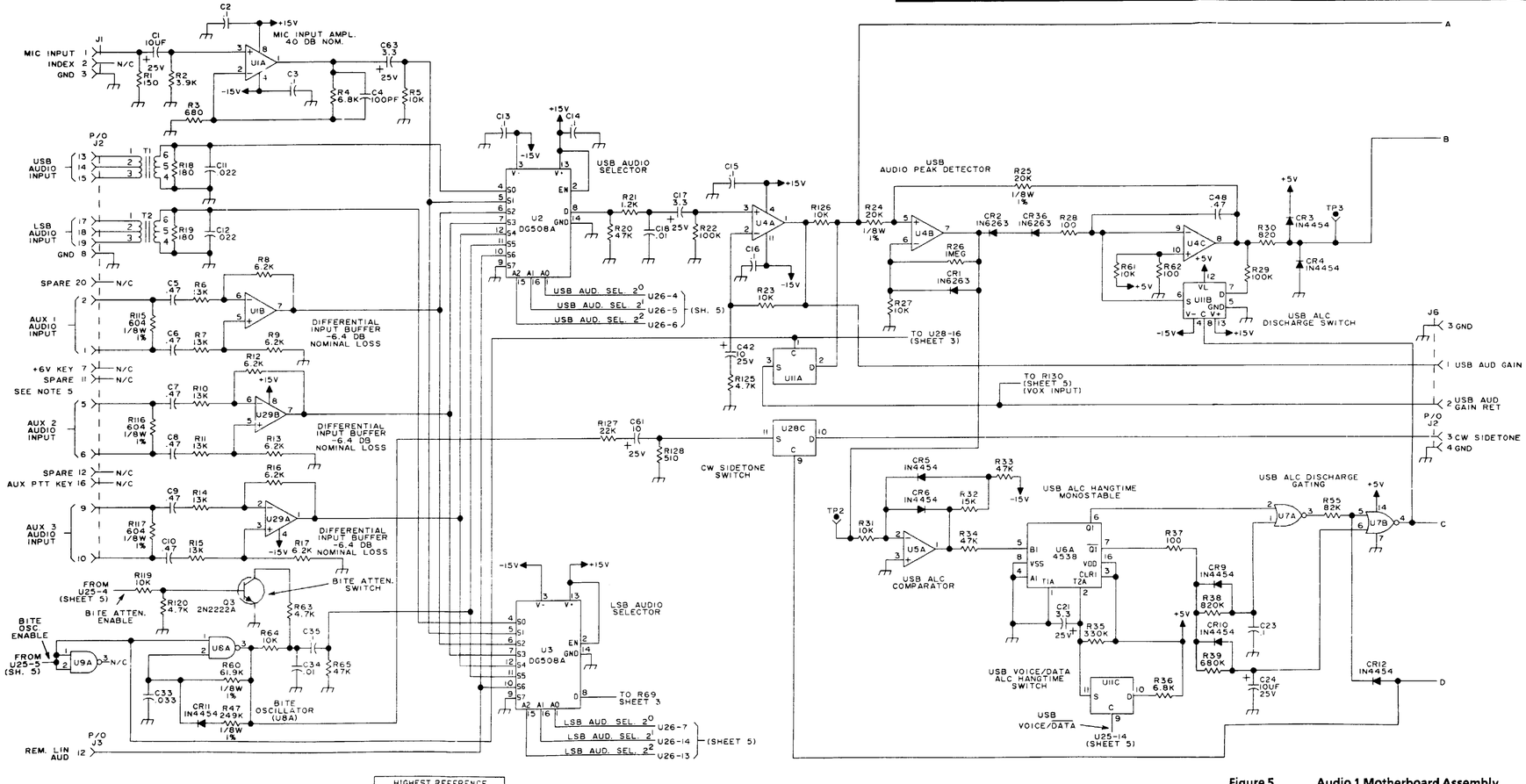


Figure 4. Audio 1 Motherboard Assembly A5A1 Component Locations (10121-5410 Rev. D)

NOTE: UNLESS OTHERWISE SPECIFIED:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR A COMPLETE DESIGNATION, PREFIX WITH UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.
2. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, ±5%.
3. ALL CAPACITOR VALUES ARE IN MICROFARADS.
4. VENDOR PART NO. CALLOUTS ARE FOR REFERENCE ONLY. COMPONENTS ARE SUPPLIED PER PART NO. IN PARTS LIST.
5. ON THE 10121-5410-12 VERSION OF THIS BOARD, J2 PIN 11 IS CONNECTED TO +5V. THIS VERSION IS INSTALLED IN RF1310A-030 EXCITERS



HIGHEST REFERENCE DESIGNATION				
C64	CR41	J7	Q3	R133
T2	TP8	U29	VR2	
REFERENCE DESIGNATIONS NOT USED				

Figure 5. Audio 1 Motherboard Assembly A5A1 Schematic Diagram (10121-5411 Rev. L) (Sheet 1 of 5)

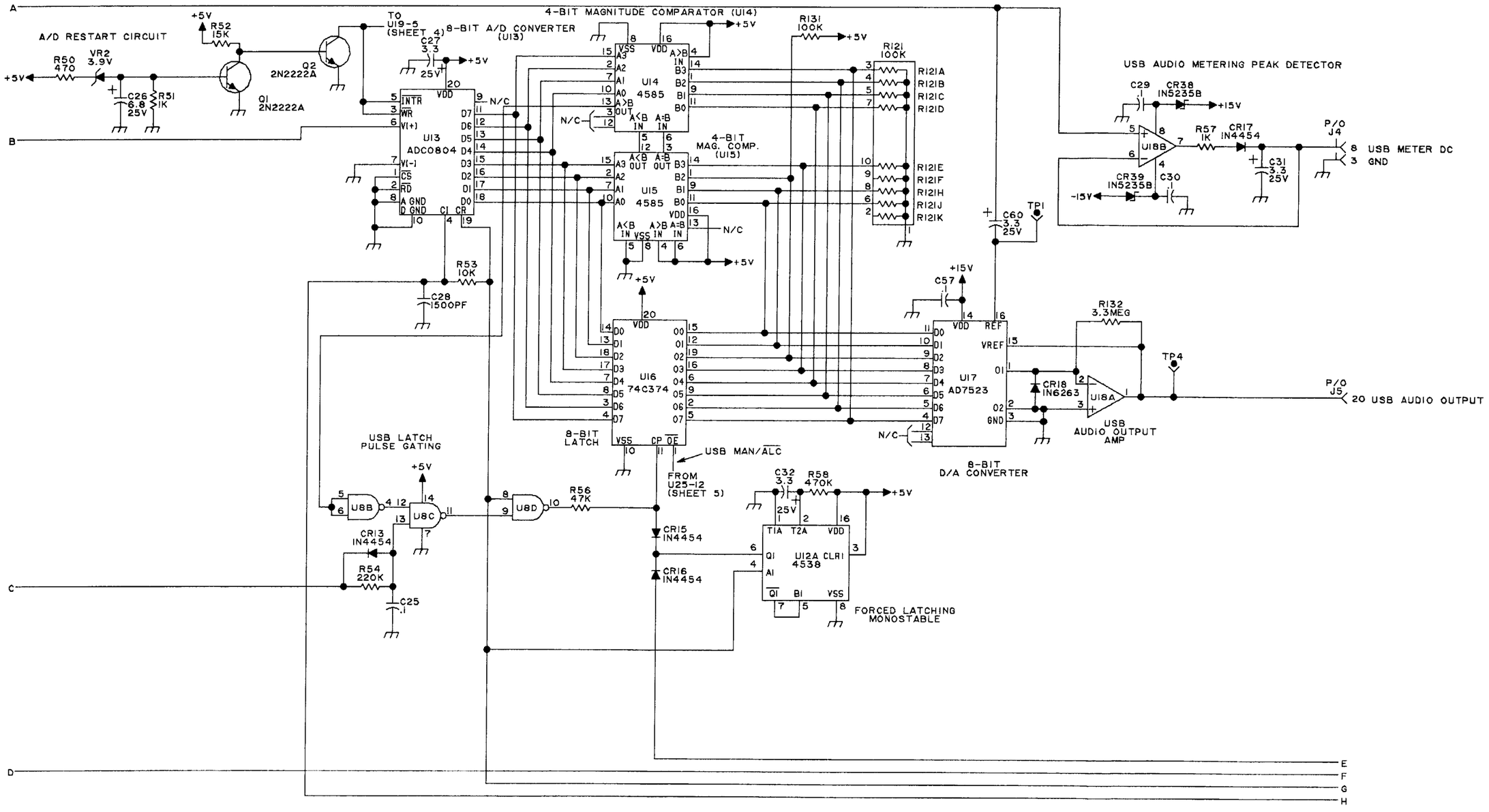


Figure 5. **Audio 1 Motherboard Assembly A5A1 Schematic Diagram (10121-5411 Rev. L) (Sheet 2 of 5)**

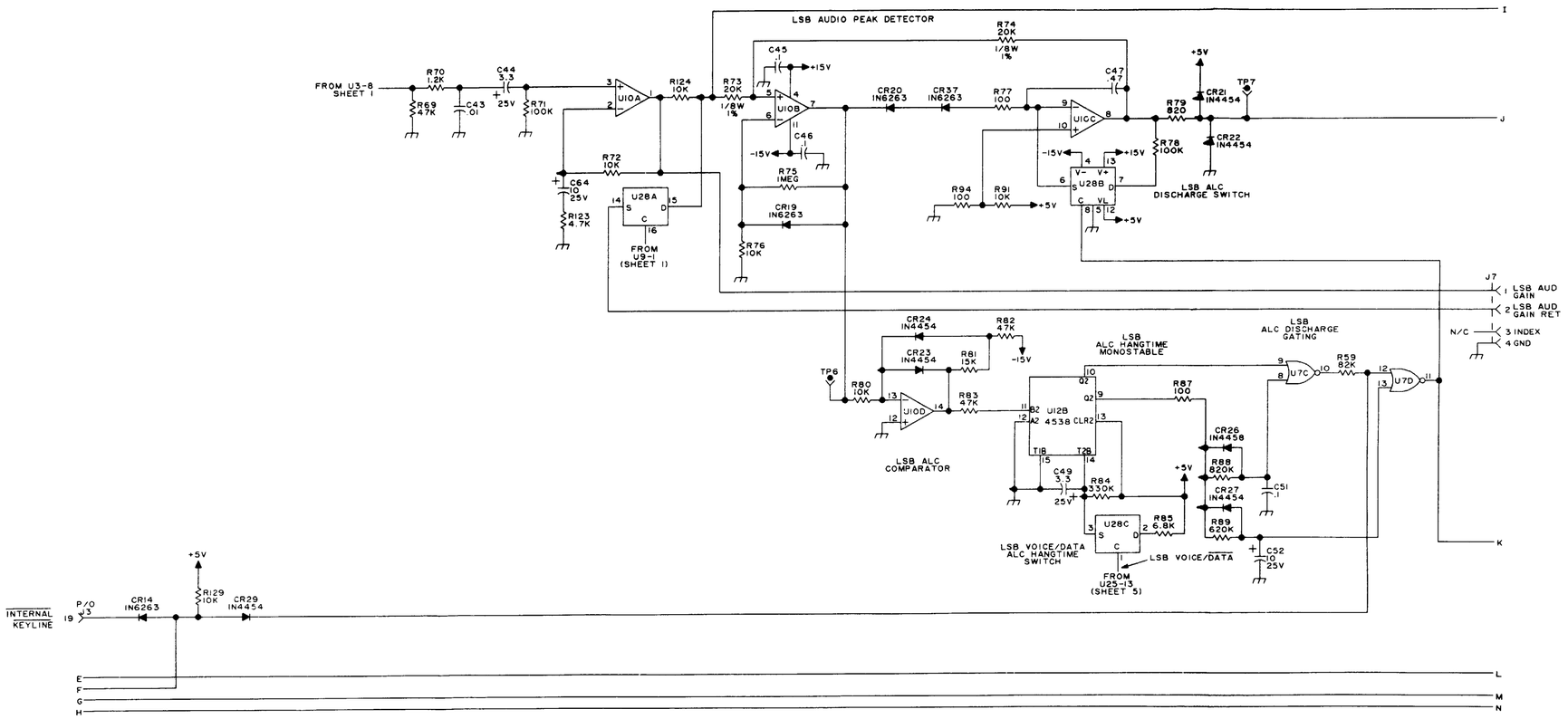


Figure 5. **Audio 1 Motherboard Assembly A5A1 Schematic Diagram (10121-5411 Rev. L) (Sheet 3 of 5)**

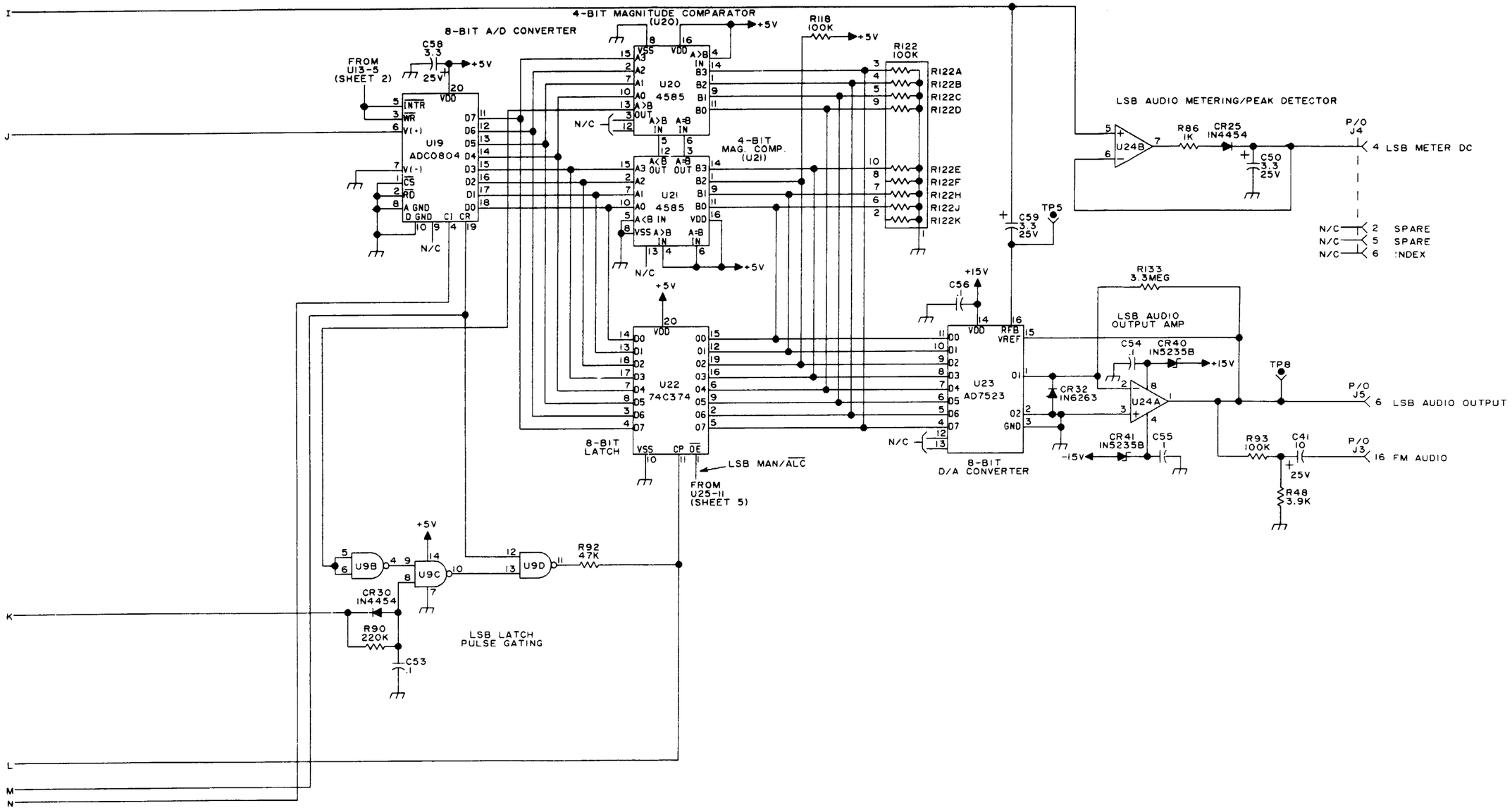


Figure 5. **Audio 1 Motherboard Assembly A5A1 Schematic Diagram (10121-5411 Rev. L) (Sheet 4 of 5)**

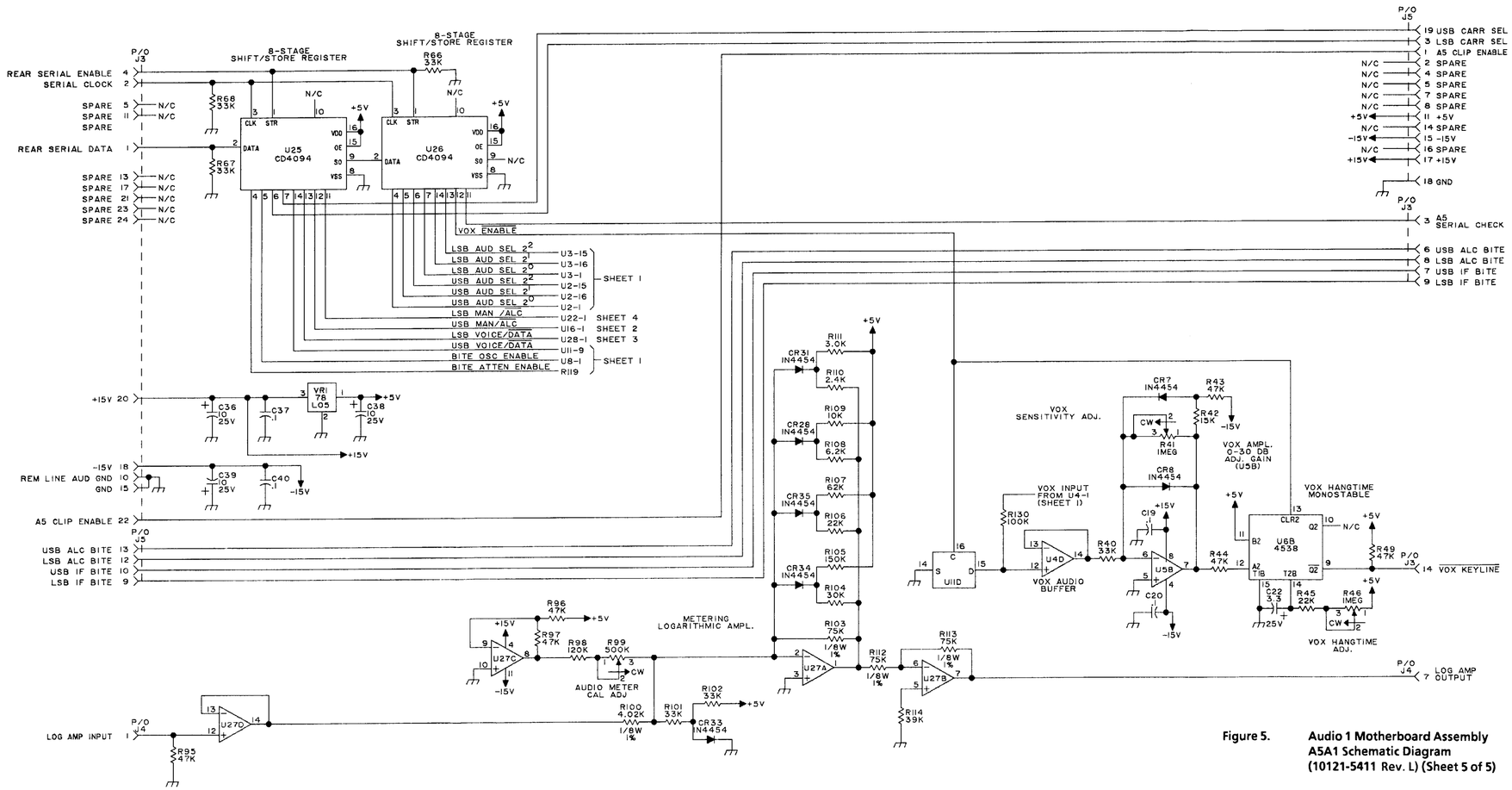
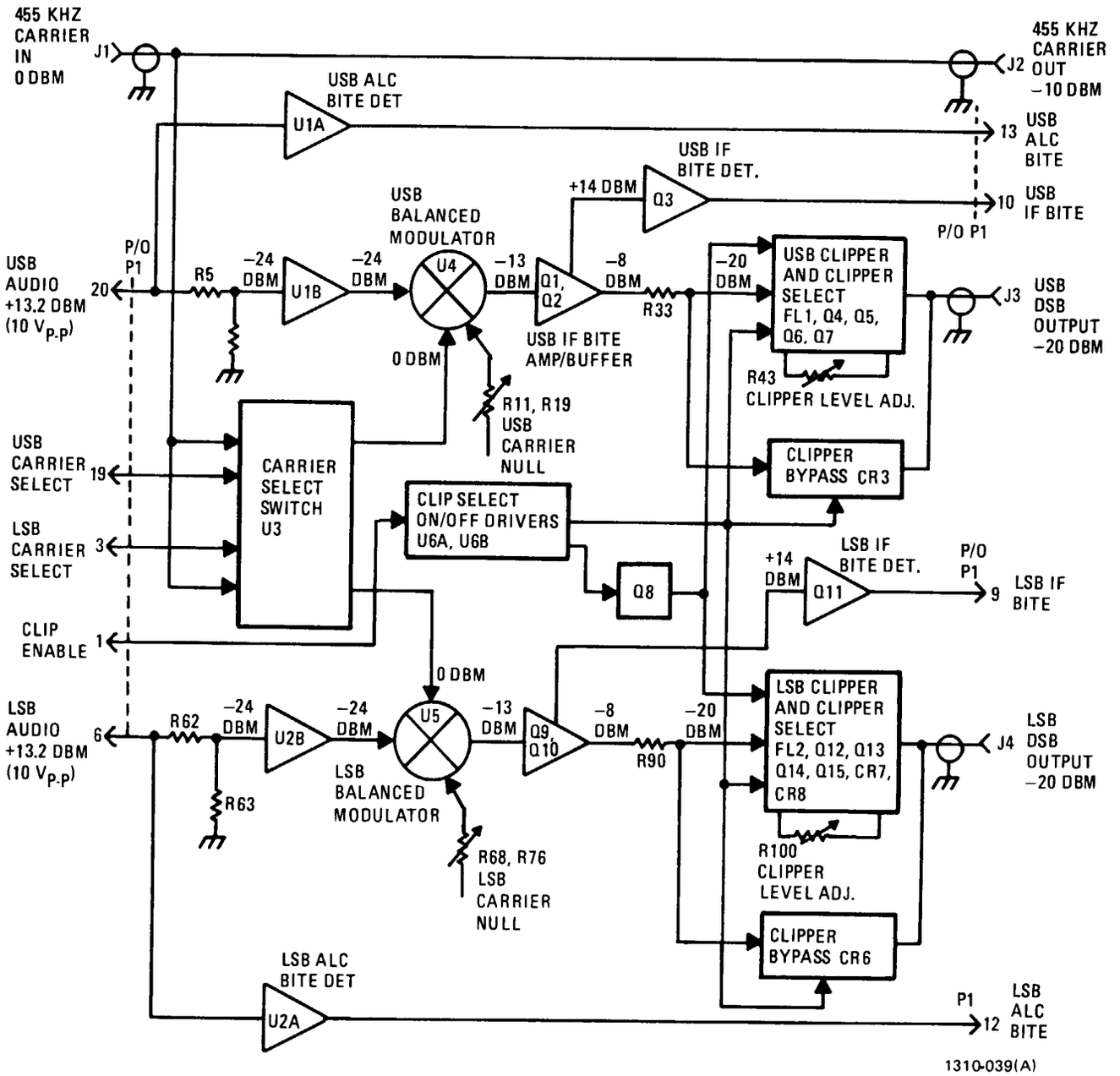


Figure 5. Audio 1 Motherboard Assembly A5A1 Schematic Diagram (10121-5411 Rev. L) (Sheet 5 of 5)

A5A2
AUDIO 2 ASSEMBLY



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AUDIO 2 ASSEMBLY A5A2

1. GENERAL INFORMATION

Audio 2 Assembly A5A2 (10121-5450) translates each of the two gain controlled audio outputs of the A5A1 assembly to 455 kHz. The output produced for each sideband path is a double sideband (DSB) suppressed carrier signal centered on 455 kHz. The two outputs are sent to the A4 assembly for filtering and further processing. The A5A2 assembly is mounted over the A5A1 assembly. Refer to figure 1 of the A5A1 subsection for the A5A2 assembly location.

A RF clipper circuit is included in each sideband path, providing an adjustable clipping level from 3 dB to 15 dB. Two versions of Audio 2 Assembly A5A2 are available. Version 10121-5450-02 includes a mechanical filter just ahead of each clipper circuit where version 10121-5450-01 substitutes a resistive pad for the filter. The -02 version is preferred for clipping voice transmissions while the -01 version should be installed for clipped data transmission. Clipping is enabled by the CLIP pushbutton on the exciter front panel.

Additionally, Audio 2 PWB Assembly A5A2 contains circuits providing the following functions:

- Automatic Level Control (ALC) BITE peak detection for each sideband
- IF BITE peak detection for each sideband
- Individual ON/OFF control of 455 kHz carrier injection to balanced modulators of each sideband path
- ON/OFF control of power supply for clipper circuits
- -10 dBm 455 kHz carrier output to A4

2. INTERFACE CONNECTIONS

Table 1 lists the various input/output connections and other relevant data.

Table 1. Audio 2 Assembly A5A2 Interface Connections

Connector	Function	Characteristics
J1	455 kHz Input	0 dBm, nominal
J2	455 kHz Output	-10 dBm, nominal
J3	USB DSB Output	-20 dBm, PEP, nominal
J4	LSB DSB Output	-20 dBm PEP, nominal
P1-1	Clip Enable	+ 5 V enables; 0 V disables
P1-2	Spare	
P1-3	LSB Carrier Select	+ 5 V selects; 0 V not selected
P1-4, P1-5	Spare	
P1-6	LSB Audio Input	10 V_{p-p}, nominal
P1-7, P1-8	Spare	

Table 1. Audio 2 Assembly A5A2 Interface Connections (Cont.)

Connector	Function	Characteristics
P1-9	LSB IF BITE	
P1-10	USB IF BITE	
P1-11	Power, + 5 Vdc	
P1-12	LSB ALC BITE	
P1-13	USB ALC BITE	
P1-14	Spare	
P1-15	Power, -15 Vdc	
P1-16	Spare	
P1-17	Power, + 15 Vdc	
P1-18	Ground	
P1-19	USB Carrier Select	+ 5 V selects; 0 V not selected
P1-20	USB Audio Input	10 V_{p-p}, nominal

3. AUDIO 2 PWB ASSEMBLY A5A2 CIRCUIT DESCRIPTION

NOTE

Where the design of circuits of the USB and LSB paths are identical, the following descriptions refer to components of the LSB path within parenthesis.

3.1 ALC BITE Detector

The nominal 10 V_{p-p} audio input signal at P1-20 (P1-6) is attenuated by R1 and R2 (R58 and R59) and applied to ALC BITE Detector U1A (U2A) whose dc output is sent to the A14 assembly via P1-13 (P1-12) for evaluation during BITE testing.

3.2 Balanced Modulator

U4 (U5) is configured as a balanced modulator operating with high level carrier injection (0 dBm). The circuit translates the audio output of the A5A1 assembly to form a DSB suppressed carrier signal centered on 455 kHz. The audio input signal enters at P1-20 (P1-6), is attenuated by R5 and R6 (R62 and R63), buffered by U1B (U2B), and coupled to the balanced modulator at U4-4 (U5-4). The 455 kHz carrier is applied at U4-8 (U5-8) via carrier select switch U3. R11 and R19 (R68 and R76) are part of a nulling circuit and are adjusted to yield maximum suppression of the 455 kHz carrier as observed at balanced modulator output U4-12 (U5-12).

3.3 Carrier Select Switch

U3 is a quad bilateral switch configured to allow individual ON/OFF control of carrier injection to the balanced modulators. USB Carrier Select (J2-19) and LSB Carrier Select (J2-3) control the switch. The logic states of these carrier select lines are controlled by the Control Board Assembly A14 microprocessor in accordance with the selected exciter mode of transmission. Table 2 details the carrier select logic states for the selected mode.

Table 2. Audio 2 PWB Assembly A5A2 Carrier Select Logic

Mode	J2-19 USB Carrier Select	J2-13 LSB Carrier Select	USB Carrier Injection	LSB Carrier Injection
CW	0	0	OFF	OFF
AFSK	1	0	ON	OFF
AM, AME	1	0	ON	OFF
USB	1	0	ON	OFF
LSB	0	1	OFF	ON
ISB	1	1	ON	ON
FM	0	0	OFF	OFF
FSK	0	0	OFF	OFF
MCW	1	0	ON	OFF

When the USB (LSB) carrier is selected, the 455 kHz carrier signal is passed through switch U3 to U3-6 (U3-14) and injected at the USB (LSB) balanced modulator at U4-8 (U5-8).

3.4 IF BITE Amplifier/Output Buffer

Q1 and Q2 (Q9 and Q10) comprise a feedback pair which amplifies the balanced modulator output U4-12 (U5-12). The amplifier provides two outputs, each yielding a different gain. The collector of Q2 (Q10) yields a nominal gain of 28 dB and is applied to IF BITE detector Q3 (Q11). The detector output is a dc voltage proportional to the signal level at the balanced modulator output and is sent to Control Board Assembly A14 via P1-10 (P1-9) for evaluation during BITE testing. The second feedback pair amplifier output is at the emitter of Q2 (Q10) and yields a gain of 5 dB. This output is coupled via C64 to the input of the clipper circuit.

3.5 Clipper Circuit

A bypassable clipper comprises the last active stage of Audio 2 Assembly A5A2 signal path. The clipper circuit is enabled/bypassed by the CLIP pushbutton on the exciter front panel. Enabling and bypassing is affected by the high/low state of Clip Enable line P1-1. When Clip Enable is low (Bypass), comparator output U6-7 is at + 15 volts, thereby turning on Clip Bypass Diode CR3 (CR6) which then provides a direct signal path from Q2 (Q10) emitter to the USB (LSB) DSB output J3 (J4). Additionally, when Clip Enable is low (Bypass), U6-1 is at + 15 volts, thereby turning off Q8. This removes + 15 volts power normally supplied to clipping amplifier Q4 and Q5 (Q12 and Q13), thereby entirely disabling the clipper circuit. Moreover, the + 15 V at U6-7 turns on CR5 (CR8), shunting any clipper output to ground and shuts off CR4 (CR7), thereby opening the clipper output path.

When clipping is selected, Clip Enable is high (+ 5 V) and U6-7 and U6-1 are at -15 volts turning off CR3 (CR6), opening the bypass path. CR5 (CR8) is off (open) and CR4 (CR7) is on (closed) ,thereby providing a signal path from the clipper output to the USB (LSB) DSB output J3 (J4). Additionally, Q8 is on, yielding + 15 volts supplied to clipping amplifier Q4 and Q5 (Q12 and Q13).

When clipping is enabled, the signal passes from Q2 (Q10) emitter, through FL1 (FL2) into clipping amplifier Q4 and Q5 (Q12 and Q13) whose output peaks are clipped by Q6 and Q7 (Q14 and Q15). The gain of the clipping amplifier is adjustable at R43 (R100), thereby yielding a variable clipping level from 3 dB to 15 dB. Clipped output passes through R42 (R99) and CR4 (CR7) to the DSB output J3 (J4).

3.6 Carrier Attenuator

R56 and R57 attenuate the 0 dBm 455 kHz carrier input (J1) to a level of -10 dBm. The attenuated carrier is output via J2 to Combiner PWB Assembly A4 where it is used for carrier reinsertion in AM, and reduced carrier modes.

4. MAINTENANCE

The following adjustments should not be made as routine maintenance procedures, but only when a failure indicates a definite need. All tests and adjustments are performed with all assembly connections in normal contact unless otherwise specified.

4.1 USB Carrier Null Adjustment

a. Refer to the Control PWB Assembly A14 subsection of this manual and program the AUX 1 Audio Input for ALC operation and voice time constant.

b. Adjust the USB audio input level potentiometer on the exciter front panel fully clockwise.

c. Connect equipment as shown in figure 1. Remove orange-sleeved cable from J3 and attach separate cable from J3 to spectrum analyzer.

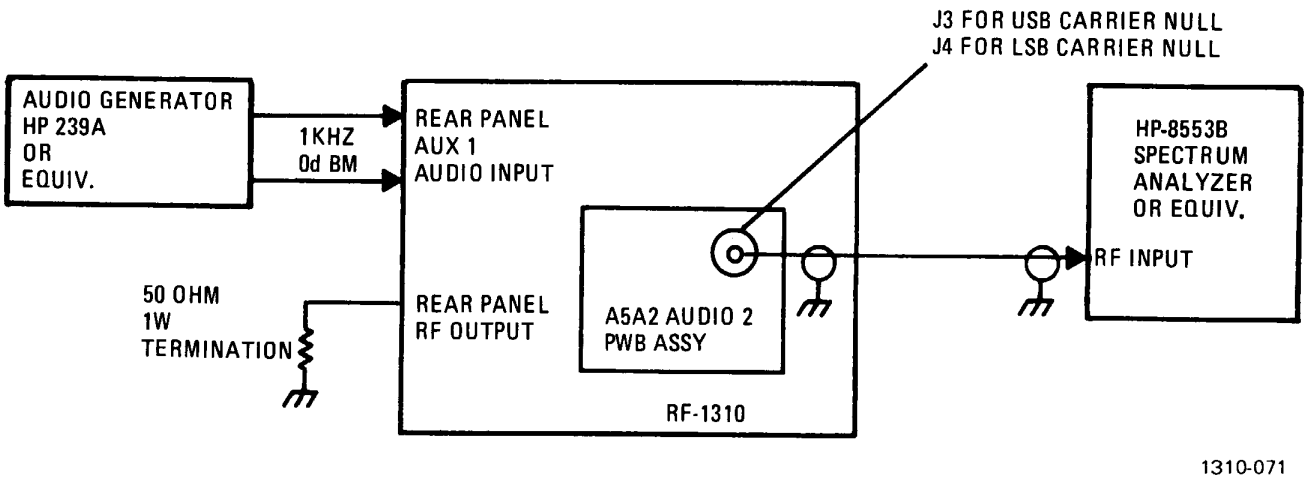


Figure 1. USB/LSB Carrier Null Setup

d. Set spectrum analyzer controls:

- Center frequency to 455 kHz

- Reference level to -26 dBm
- Scan width to 10 kHz

Set audio generator to 1 kHz, 0 dBm.

e. Set exciter front panel controls:

- Function - NORM
- Mode - USB
- Carrier - None
- Frequency - 2 MHz
- Audio - AUX 1

f. Terminate exciter rear panel RF output to a 50 ohm, 1 watt termination or equivalent.

g. Key exciter PTT line and observe spectrum analyzer display similar to that in figure 2. Adjust spectrum analyzer scan width, bandwidth, and sweep time to allow clear definition of the residual 455 kHz carrier.

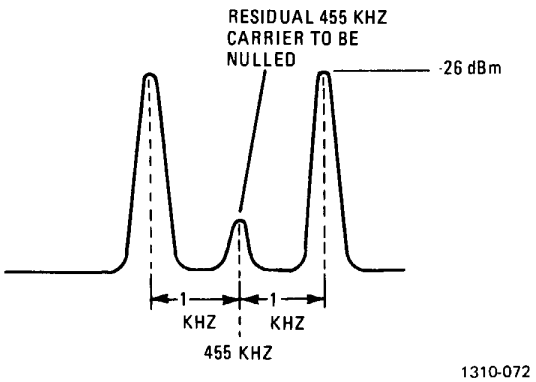


Figure 2. Typical Carrier Null Spectrum Analyzer Display

h. Alternately adjust R11 and R19 for lowest observable level of 455 kHz carrier.

i. USB carrier null complete. Disconnect spectrum analyzer from J3 and reconnect orange-sleeved cable to J3.

4.2 LSB Carrier Null Adjustment

a. Refer to the Control Board Assembly A14 subsection of this manual and program the AUX 1 Audio Input for ALC operation and voice time constant.

b. Adjust the LSB audio input level potentiometer on the exciter front panel fully clockwise.

c. Connect equipment as shown in figure 1. Remove yellow-sleeved cable from J4 and attach separate cable from J4 to spectrum analyzer.

d. Set spectrum analyzer controls:

- Center frequency to 455 kHz
- Reference level to -26 dBm
- Scan width to 10 kHz

Set audio generator to 1 kHz, 0 dBm.

e. Set exciter front panel controls:

- Function - NORM
- Mode - LSB
- Carrier - None
- Frequency - 2 MHz
- Audio - AUX 1

f. Terminate exciter rear panel RF output to a 50 ohm, 1 W termination or equivalent.

g. Key exciter PTT line and observe spectrum analyzer display similar to that of figure 2. Adjust spectrum analyzer scan width, bandwidth, and sweep time to allow clear definition of the residual 455 kHz carrier.

h. Alternately adjust R76 and R68 for lowest observable level of 455 kHz carrier.

i. LSB carrier null complete. Disconnect spectrum analyzer from J4 and reconnect yellow-sleeved cable to J4.

4.3 CLIPPER ADJUST

a. Connect equipment as shown in figure 1. Remove coax from J3 for USB or J4 for LSB. Attach separate cable from J3 (J4) to the spectrum analyzer.

b. Set R43 (R100) to full counterclockwise position.

c. Push the CLIP pushbutton switch on the front panel. A two tone signal and harmonics should appear.

d. Adjust R43 (R100) fully clockwise.

e. The two tone signal should change by no more than + 3 dB and the harmonics should increase in amplitude.

f. Adjust R43 (R100) to increase the peak to average power ratio as desired.

g. Disconnect the spectrum analyzer from J3 (J4) and reconnect the coax to J3 (J4).

h. Push the CLIP switch to off.

5. PARTS LIST, COMPONENT LOCATIONS, AND SCHEMATIC DIAGRAM

All replaceable components are listed in table 3. Component locations are shown in figure 3. Figure 4 is the schematic diagram of the Audio 2 assembly circuit.

Table 3. Audio 2 Assembly A5A2 Parts List (10121-5450 Rev. L)

Ref. Desig.	Part Number	Description
C1	C26-0025-339	CAP 3.3UF 20% 25V TANT
C2	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C3	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C4	C26-0025-339	CAP 3.3UF 20% 25V TANT
C5	C26-0025-339	CAP 3.3UF 20% 25V TANT
C6	C26-0025-339	CAP 3.3UF 20% 25V TANT
C7	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C8	C26-0025-339	CAP 3.3UF 20% 25V TANT
C9	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C10	M39014/02-1298V	CAP .01UF 10% 200V CER-R
C11	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C12	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C13	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C14	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C15	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C16	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C19	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C20	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C21	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C22	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C23	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C24	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C25	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C26	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C27	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C28	C26-0025-339	CAP 3.3UF 20% 25V TANT
C29	C26-0025-339	CAP 3.3UF 20% 25V TANT
C30	C26-0025-339	CAP 3.3UF 20% 25V TANT
C31	C26-0025-339	CAP 3.3UF 20% 25V TANT
C32	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C33	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C34	C26-0025-339	CAP 3.3UF 20% 25V TANT
C35	C26-0025-339	CAP 3.3UF 20% 25V TANT
C36	C26-0025-339	CAP 3.3UF 20% 25V TANT
C37	M39014/02-1310V	CAP .1UF 10% 100V CER-R

Table 3. Audio 2 Assembly A5A2 Parts List (10121-5450 Rev. L) (Cont.)

Ref. Desig.	Part Number	Description
C38	C26-0025-339	CAP 3.3UF 20% 25V TANT
C39	M39014/02-1298V	CAP .01UF 10% 200V CER-R
C40	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C41	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C42	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C43	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C44	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C45	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C46	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C47	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C50	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C51	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C52	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C53	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C54	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C55	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C56	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C57	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C58	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C59	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C60	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C61	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C62	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C64	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C65	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C66	M39014/02-1292V	CAP 4700PF 10% 200V CER-R
C67	M39014/02-1292V	CAP 4700PF 10% 200V CER-R
CR1	1N4454	DIODE 200MA 75V SW
CR2	1N4454	DIODE 200MA 75V SW
CR3	D12-0007-001	DIODE PIN ATTN 1W 9301
CR4	D12-0007-001	DIODE PIN ATTN 1W 9301
CR5	D12-0007-001	DIODE PIN ATTN 1W 9301
CR6	D12-0007-001	DIODE PIN ATTN 1W 9301
CR7	D12-0007-001	DIODE PIN ATTN 1W 9301
CR8	D12-0007-001	DIODE PIN ATTN 1W 9301
CR9	1N4454	DIODE 200MA 75V SW
J1	J-0031	CONN SMB VERT PCB F
J2	J-0031	CONN SMB VERT PCB F
J3	J-0031	CONN SMB VERT PCB F
J4	J-0031	CONN SMB VERT PCB F
JMP1	MP-1142	RES ZERO OHM (CKT JMPR)
JMP2	MP-1142	RES ZERO OHM (CKT JMPR)
L1	MS75085-13	COIL 330UH 10% FXD RF
L2	MS75085-13	COIL 330UH 10% FXD RF
L3	MS75085-13	COIL 330UH 10% FXD RF

Table 3. Audio 2 Assembly A5A2 Parts List (10121-5450 Rev. L) (Cont.)

Ref. Desig.	Part Number	Description
L4	MS75085-13	COIL 330UH 10% FXD RF
L5	MS75085-13	COIL 330UH 10% FXD RF
L6	MS75085-13	COIL 330UH 10% FXD RF
P1	10073-7072	RIBBON CABLE, 20 COND
Q1	2N2222A	XSTR SS/GP NPN TO-18
Q2	2N2222A	XSTR SS/GP NPN TO-18
Q3	2N2222A	XSTR SS/GP NPN TO-18
Q4	2N2222A	XSTR SS/GP NPN TO-18
Q5	2N2222A	XSTR SS/GP NPN TO-18
Q6	2N2222A	XSTR SS/GP NPN TO-18
Q7	2N2907A	XSTR SS/GP PNP TO-18
Q8	2N2907A	XSTR SS/GP PNP TO-18
Q9	2N2222A	XSTR SS/GP NPN TO-18
Q10	2N2222A	XSTR SS/GP NPN TO-18
Q11	2N2222A	XSTR SS/GP NPN TO-18
Q12	2N2222A	XSTR SS/GP NPN TO-18
Q13	2N2222A	XSTR SS/GP NPN TO-18
Q14	2N2222A	XSTR SS/GP NPN TO-18
Q15	2N2907A	XSTR SS/GP PNP TO-18
Q16	2N2222A	XSTR SS/GP NPN TO-18
Q17	2N2222A	XSTR SS/GP NPN TO-18
R1	R65-0003-333	RES 33K 5% 1/4W CAR FILM
R2	R65-0003-243	RES 24K 5% 1/4W CAR FILM
R3	R65-0003-223	RES 22K 5% 1/4W CAR FILM
R4	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R5	RN55D5362F	RES 53.6K 1% 1/8W MET FLM
R6	RN55D8250F	RES 825 1% 1/8W MET FLM
R7	R65-0003-333	RES 33K 5% 1/4W CAR FILM
R8	R65-0003-202	RES 2.0K 5% 1/4W CAR FILM
R9	R65-0003-101	RES 100 5% 1/4W CAR FILM
R10	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R11	R30-0008-101	RES VAR PCB 10 1/2W 20%
R12	R65-0003-392	RES 3.9K 5% 1/4W CAR FILM
R13	R65-0003-101	RES 100 5% 1/4W CAR FILM
R14	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R15	R65-0003-101	RES 100 5% 1/4W CAR FILM
R16	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R17	R65-0003-152	RES 1.5K 5% 1/4W CAR FILM
R18	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R19	R30-0008-503	RES VAR PCB 50K 1/2W 10%
R20	R65-0003-104	RES 100K 5% 1/4W CAR FILM
R21	R65-0003-101	RES 100 5% 1/4W CAR FILM
R22	R65-0003-242	RES 2.4K 5% 1/4W CAR FILM
R23	R65-0003-242	RES 2.4K 5% 1/4W CAR FILM
R24	R65-0003-471	RES 470 5% 1/4W CAR FILM

Table 3. Audio 2 Assembly A5A2 Parts List (10121-5450 Rev. L) (Cont.)

Ref. Desig.	Part Number	Description
R25	R65-0003-392	RES 3.9K 5% 1/4W CAR FILM
R26	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R27	R65-0003-821	RES 820 5% 1/4W CAR FILM
R28	R65-0003-682	RES 6.8K 5% 1/4W CAR FILM
R29	R65-0003-101	RES 100 5% 1/4W CAR FILM
R30	R65-0003-105	RES 1.0M 5% 1/4W CAR FILM
R31	R65-0003-101	RES 100 5% 1/4W CAR FILM
R32	R65-0003-334	RES 330K 5% 1/4W CAR FILM
R33	R65-0003-151	RES 150 5% 1/4W CAR FILM
R34	R65-0003-272	RES 2.7K 5% 1/4W CAR FILM
R35	R65-0003-272	RES 2.7K 5% 1/4W CAR FILM
R36	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R37	R65-0003-510	RES 51 5% 1/4W CAR FILM
R38	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R39	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R40	R65-0003-220	RES 22 5% 1/4W CAR FILM
R41	R65-0003-511	RES 510 5% 1/4W CAR FILM
R42	R65-0003-152	RES 1.5K 5% 1/4W CAR FILM
R43	R-2213	RES VAR 100K 10% .5W HOR.
R44	R65-0003-752	RES 7.5K 5% 1/4W CAR FILM
R45	R65-0003-151	RES 150 5% 1/4W CAR FILM
R46	R65-0003-430	RES 43 5% 1/4W CAR FILM
R47	R65-0003-392	RES 3.9K 5% 1/4W CAR FILM
R48	R65-0003-392	RES 3.9K 5% 1/4W CAR FILM
R49	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R50	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R51	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R52	R65-0003-333	RES 33K 5% 1/4W CAR FILM
R53	R65-0003-333	RES 33K 5% 1/4W CAR FILM
R54	R65-0003-473	RES 47K 5% 1/4W CAR FILM
R55	R65-0003-333	RES 33K 5% 1/4W CAR FILM
R56	R65-0003-121	RES 120 5% 1/4W CAR FILM
R57	R65-0003-680	RES 68 5% 1/4W CAR FILM
R58	R65-0003-333	RES 33K 5% 1/4W CAR FILM
R59	R65-0003-243	RES 24K 5% 1/4W CAR FILM
R60	R65-0003-223	RES 22K 5% 1/4W CAR FILM
R61	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R62	RN55D5362F	RES 53.6K 1% 1/8W MET FLM
R63	RN55D8250F	RES 825 1% 1/8W MET FLM
R64	R65-0003-333	RES 33K 5% 1/4W CAR FILM
R65	R65-0003-202	RES 2.0K 5% 1/4W CAR FILM
R66	R65-0003-101	RES 100 5% 1/4W CAR FILM
R67	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R68	R30-0008-101	RES VAR PCB 10 1/2W 20%

Table 3. Audio 2 Assembly A5A2 Parts List (10121-5450 Rev. L) (Cont.)

Ref. Desig.	Part Number	Description
R69	R65-0003-101	RES 100 5% 1/4W CAR FILM
R70	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R71	R65-0003-392	RES 3.9K 5% 1/4W CAR FILM
R72	R65-0003-101	RES 100 5% 1/4W CAR FILM
R73	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R74	R65-0003-152	RES 1.5K 5% 1/4W CAR FILM
R75	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R76	R30-0008-503	RES VAR PCB 50K 1/2W 10%
R77	R65-0003-104	RES 100K 5% 1/4W CAR FILM
R78	R65-0003-101	RES 100 5% 1/4W CAR FILM
R79	R65-0003-242	RES 2.4K 5% 1/4W CAR FILM
R80	R65-0003-242	RES 2.4K 5% 1/4W CAR FILM
R81	R65-0003-471	RES 470 5% 1/4W CAR FILM
R82	R65-0003-392	RES 3.9K 5% 1/4W CAR FILM
R83	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R84	R65-0003-682	RES 6.8K 5% 1/4W CAR FILM
R85	R65-0003-821	RES 820 5% 1/4W CAR FILM
R86	R65-0003-101	RES 100 5% 1/4W CAR FILM
R87	R65-0003-105	RES 1.0M 5% 1/4W CAR FILM
R88	R65-0003-101	RES 100 5% 1/4W CAR FILM
R89	R65-0003-334	RES 330K 5% 1/4W CAR FILM
R90	R65-0003-151	RES 150 5% 1/4W CAR FILM
R91, R92	R65-0003-272	RES 2.7K 5% 1/4W CAR FILM
R93	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R94	R65-0003-510	RES 51 5% 1/4W CAR FILM
R95, R96	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R97	R65-0003-220	RES 22 5% 1/4W CAR FILM
R98	R65-0003-511	RES 510 5% 1/4W CAR FILM
R99	R65-0003-152	RES 1.5K 5% 1/4W CAR FILM
R100	R-2213	RES VAR 100K 10% .5W HOR.
R101	R65-0003-752	RES 7.5K 5% 1/4W CAR FILM
R102	R65-0003-151	RES 150 5% 1/4W CAR FILM
R103	R65-0003-430	RES 43 5% 1/4W CAR FILM
R104, R105	R65-0003-392	RES 3.9K 5% 1/4W CAR FILM
R106 – R108	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R109	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R110	R65-0003-333	RES 33K 5% 1/4W CAR FILM
R111 – R113	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R114	R65-0003-333	RES 33K 5% 1/4W CAR FILM
R115 – R118	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R119, R120	R65-0003-202	RES 2.0K 5% 1/4W CAR FILM

Table 3. Audio 2 Assembly A5A2 Parts List (10121-5450 Rev. L) (Cont.)

Ref. Desig.	Part Number	Description
TP1	J-0071	TP PWB BRN TOP ACCS .080"
TP2	J-0066	TP PWB RED TOP ACCS .080"
U1, U2	I30-0035-000	IC OP AMP QUAD 072
U3	I06-0002-001	IC DG211 ANALOG SW QUAD
U4, U5	I62-0001-000	IC 1496 BAL MODULATOR
U6	I30-0020-004	IC OP AMP DUAL 2904
VR1	1N4732A	DIODE 4.7V 5% 1W ZENER
VR2	1N4732A	DIODE 4.7V 5% 1W ZENER
VR3	1N4732A	DIODE 4.7V 5% 1W ZENER
VR4	1N4732A	DIODE 4.7V 5% 1W ZENER

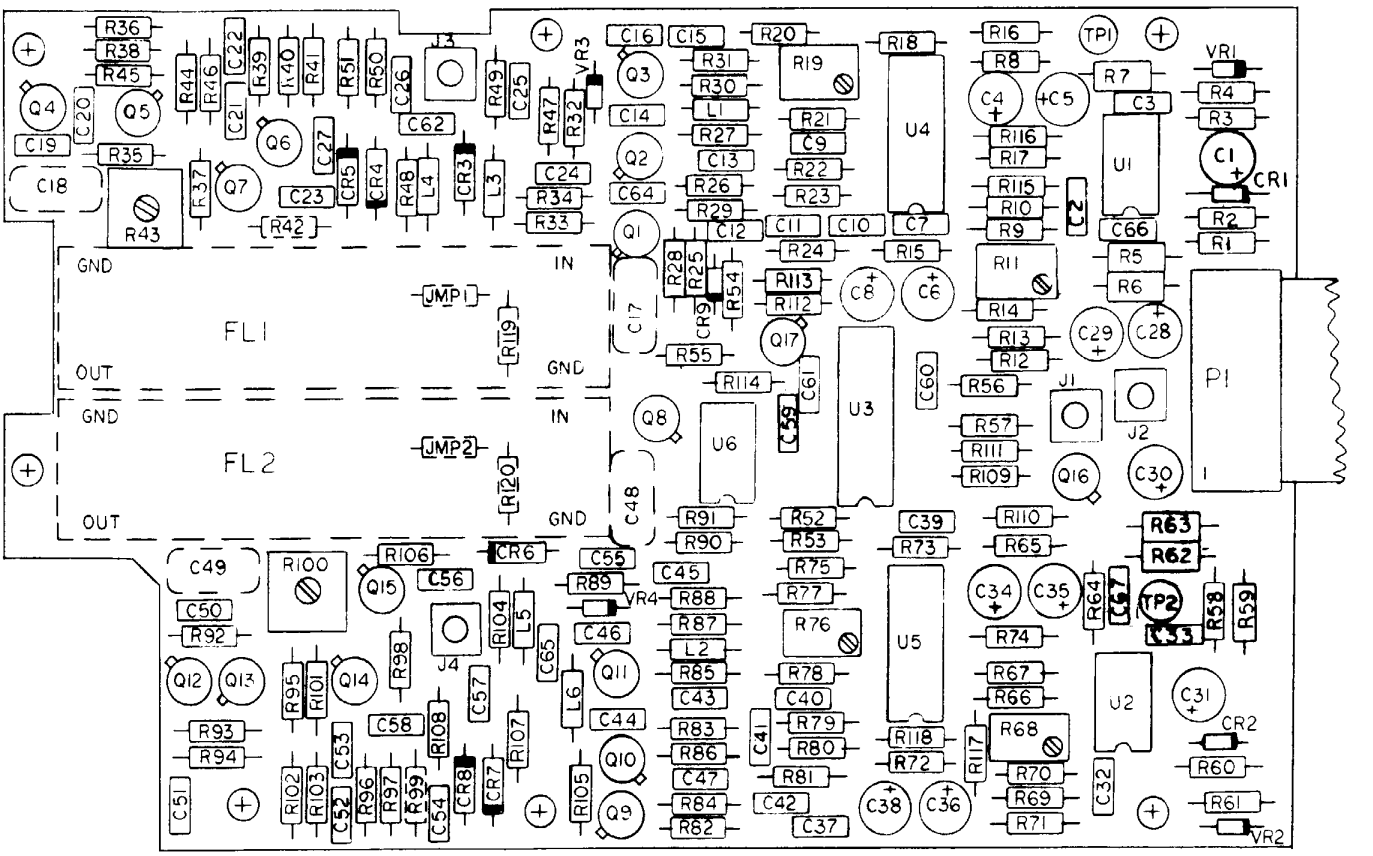


Figure 3. Audio 2 Assembly A5A2 Component Locations (10121-5450 Rev. E)

NOTE: UNLESS OTHERWISE SPECIFIED:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR A COMPLETE DESIGNATION, PREFIX WITH UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.
2. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, 5%.
3. ALL CAPACITOR VALUES ARE IN MICROFARADS.
4. VENDOR PART NO. CALLOUTS ARE FOR REFERENCE ONLY. COMPONENTS ARE SUPPLIED PER PART NO. IN PARTS LIST.
5. * WHEN THE OPTIONAL CLIPPER FILTERS FL1 & FL2 ARE INSTALLED, C17 & C18, C48 & C49 ARE ALSO INSTALLED AND JMP1 & JMP2, R118 & R120 ARE NOT USED.

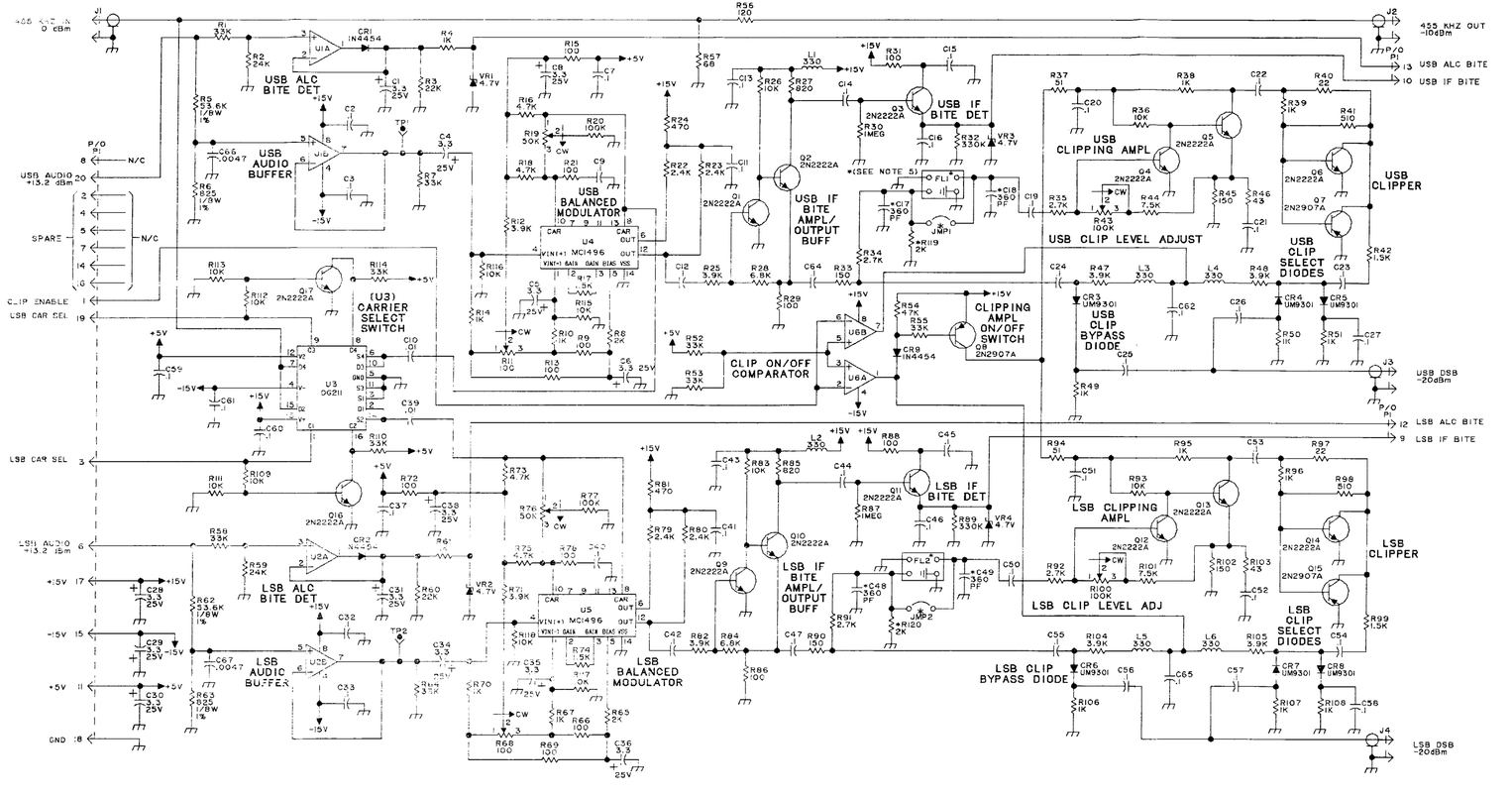
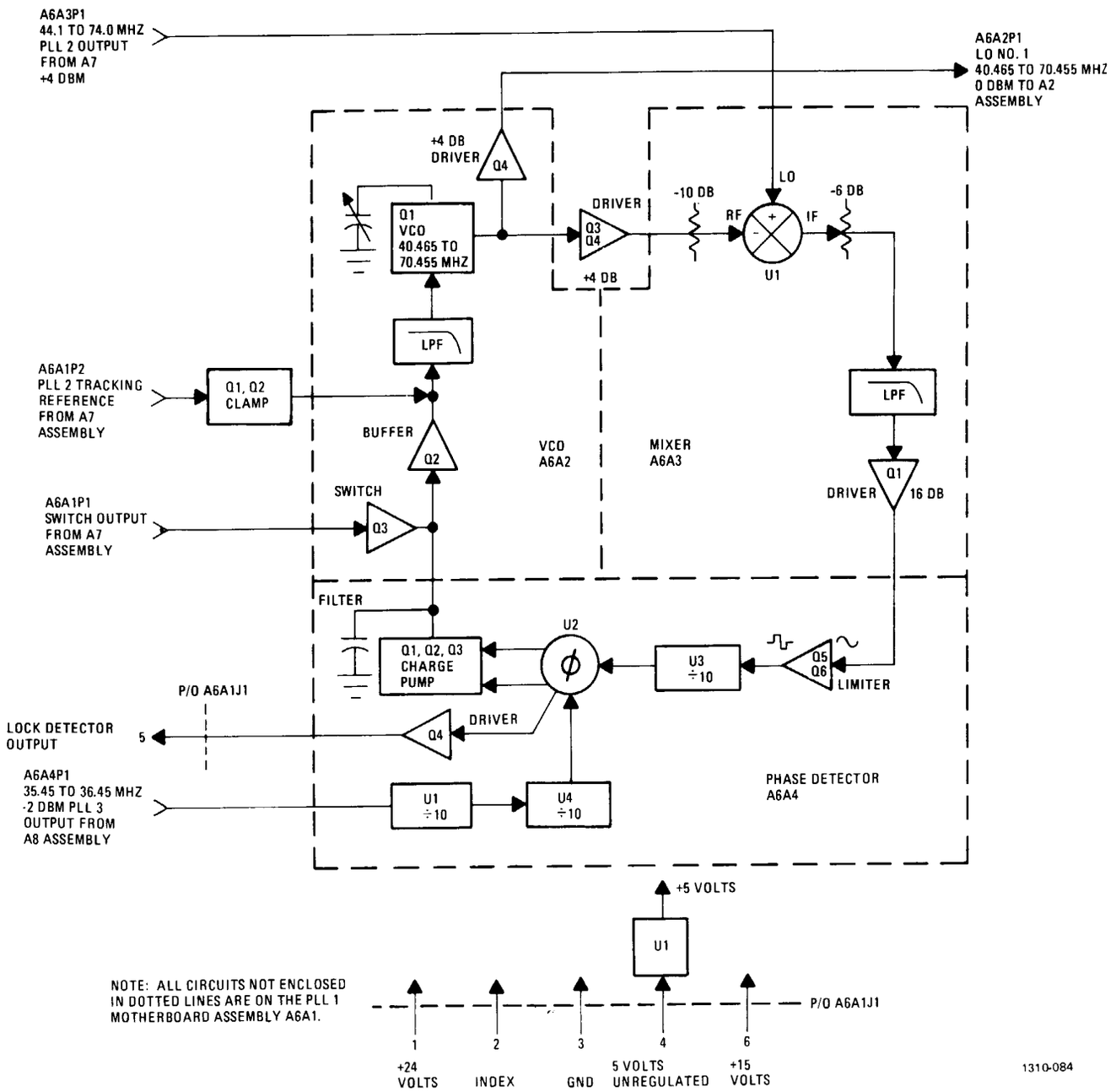


Figure 4. **Audio 2 Assembly A5A2 Schematic Diagram (10121-5451 Rev. G)**

A6
PLL 1 ASSEMBLY



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PLL 1 ASSEMBLY A6

1. GENERAL DESCRIPTION

PLL 1 Assembly A6 is a translation type phase lock loop which performs the following primary functions:

- Receives signals from the A7 and A8 assemblies that carry portions of the Local Oscillator LO 1 signal
- Frequency translates these signals to the required LO 1 range of 40.465 to 70.455 MHz

Figure 1 shows the location of PLL 1 Assembly A6 in the RF-1310 chassis.

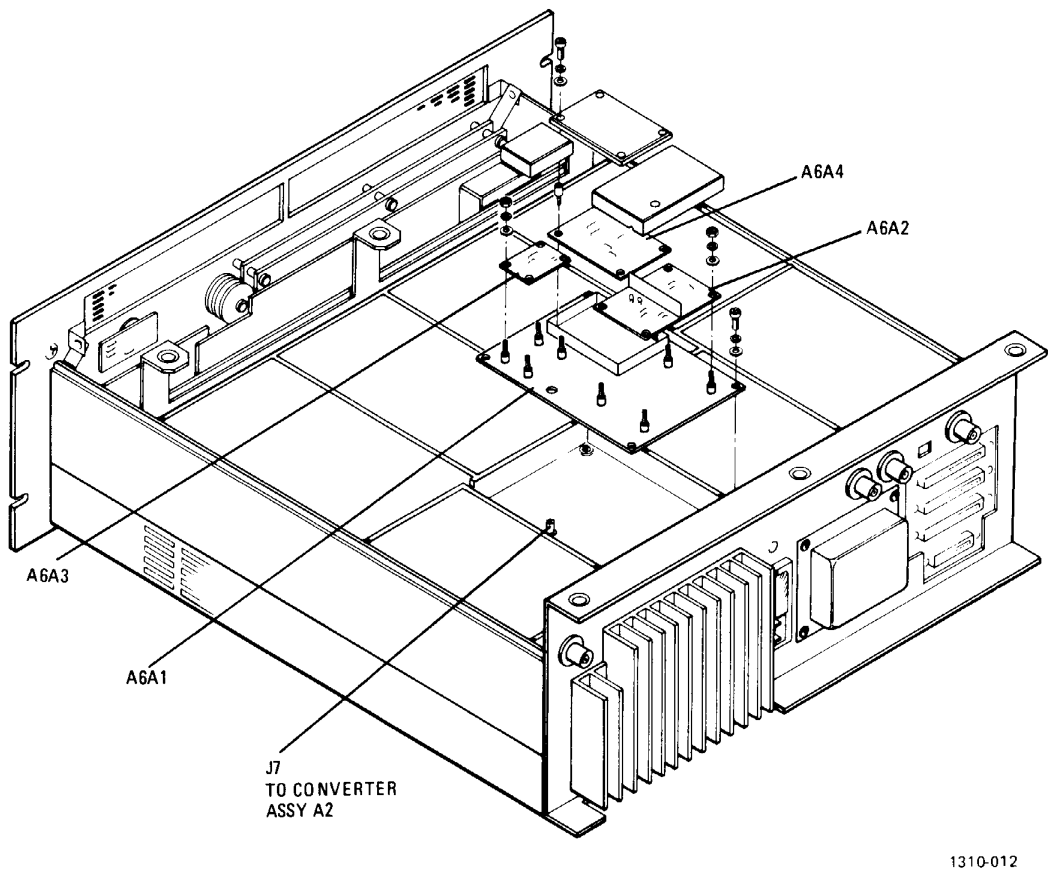


Figure 1. PLL 1 Assembly A6 Location

The signal that carries the 100 kHz, 1 MHz, and 10 MHz increments of the LO 1 frequency arrive from the A7 assembly. These are combined with the signal carrying the 1 Hz, 10 Hz, 100 Hz, 1 kHz, and 10 kHz increments from the A8 assembly. Occurring simultaneously with this combination function is frequency translation to

the LO 1 range. This signal is then applied to Converter Assembly A2, where it functions as the local oscillator no. 1 injection for A2 mixer U2. This signal which is continuously variable in 10 Hz steps, allows the RF-1310 to tune from 405 kHz to 29.99999 MHz.

PLL 1 Assembly A6 consists of the following four separate subassemblies:

- Motherboard Assembly A6A1
- VCO Assembly A6A2
- Mixer Assembly A6A3
- Phase Detector Assembly A6A4

The A6A2, A6A3, and A6A4 subassemblies are separate printed wire boards which are mounted to the A6A1 motherboard. All three subassemblies are independently shielded from each other and other circuitry on the motherboard by separate shield cans which completely surround each subassembly.

Plug-in mating connectors connect each subassembly to the others. Signals which originate or terminate off the A6 assembly are connected via coax cables and connectors or through the one main plug-in control connector, J1.

2. INTERFACE CONNECTIONS

Table 1 lists the input/output connections and other relevant data for all signals which originate or terminate off the A6 assembly. A6 subassembly interconnections are not shown.

Table 1. PLL 1 Assembly A6 Interface Connections

Connector	Function	Characteristics
A6A1J1-1	+ 24 Volts	Approximately 20 mA
A6A1J1-2	Index	
A6A1J1-3	Ground	
A6A1J1-4	+ 5 Volts Unregulated	Approximately 200 mA
A6A1J1-5	Lock Detector Output	0 V = PLL locked, + 5 V = PLL unlocked
A6A1J1-6	+ 15 Volts	Approximately 25 mA
A6A1P2	PLL 2 Tracking Reference	+ 3.5 to + 19 Vdc
A6A2P1	LO 1	0 dBm, 40.465 to 70.455 MHz (PLL output)
A6A3P1	PLL 2 Output	+ 4 dBm, 44.1 to 74.0 MHz
A6A4P1	PLL 3 Output	2 dBm, 35.45 to 36.45 MHz
A6A1P1	Switch	+ 4 V at tune frequency less than 2 MHz; 0 V at tune frequency greater than, equal to 2 MHz

3. A6 FREQUENCY GENERATION SCHEME

A PLL intermediate frequency (IF) signal in the range of 3.545 MHz to 3.645 MHz is produced at the output of mixer A6A3U1. This IF signal is a result of the subtractive mixing of the 44.1 to 74.0 MHz PLL 2 output with a VCO signal from VCO Assembly A6A2 in the range of 40.465 MHz to 70.455 MHz.

This IF signal is converted to TTL levels and divided down to a 354.5 kHz to 365.4 kHz range, and applied to one port of phase comparator A6A4U2. The second port of A6A4U2 is the reference signal, a variable 354.5 kHz to 365.4 kHz signal derived from PLL 3 Assembly A8. Any difference in frequency or phase between these two signals produces an error output from the phase comparator which forces the VCO to change its operating frequency. As the VCO frequency changes, the IF output at mixer A6A3U1 must also change. Eventually, the IF derived signal will equal the reference frequency at the phase comparator inputs, and the phase comparator will hold the VCO at the frequency which produced the correct IF.

Since the instantaneous frequencies of the PLL 2 output and the PLL 3 output are a function of the 10 MHz, 1 MHz, 100 kHz, 10 kHz, 1 kHz, 100 Hz, 10 Hz, and 1 Hz increments of the transmit frequency, the instantaneous frequency of the VCO will be a unique frequency derived from all these digits. The VCO output is applied to a mixer on the Converter Assembly and functions as that mixer's LO signal. A change in any of the digits in the frequency display will cause the LO to change to the frequency required to tune the exciter and produce the desired transmit frequency.

Given the selected transmit frequency $f_o = X_8X_7X_6X_5X_4X_3X_2X_1$ Hz where X_8 through X_2 represent the 10 MHz through 10 Hz digits shown on the frequency display and X_1 is always zero, the A6 assembly output frequency can be determined by the following formula:

$$f_{A6} = f_{A7} - \frac{1}{10} f_{A8}, \text{ Hz}$$

where

$$f_{A7} = (441 + X_8X_7X_6)(100{,}000), \text{ Hz}$$
$$f_{A8} = [40{,}000{,}000 + 10(6000 - X_3X_2X_1)] - [10{,}000(361 + X_5X_4)]\text{Hz}$$

Example:

$$f_o = 14{,}682{,}150 \text{ Hz}$$
$$f_{A7} = (441 + 146)(100{,}000) = 58{,}700{,}000 \text{ Hz}$$
$$f_{A8} = [40{,}000{,}000 + 10(6000 - 150)] - [10{,}000(361 + 82)] =$$
$$f_{A8} = [40{,}058{,}500] - [4{,}430{,}000] = 35{,}628{,}500$$
$$f_{A6} = 58{,}700{,}000 - \frac{1}{10}((35{,}628{,}500) = 55{,}137{,}150$$

Note that $f_{A6} - f_o = 40{,}455{,}000$ Hz. This relationship will be true for all exciter tune frequencies, since 40.455 MHz was chosen as the exciter's second IF.

4. CIRCUIT DESCRIPTIONS

4.1 Mixer Assembly A6A3 Operation

A variable 44.1 to 74.0 MHz, +4 dBm signal containing 100 kHz, 1 MHz, and 10 MHz tuning information from PLL 2 Assembly A7 enters the A6A3 assembly at P1 and is applied to pin 8 of mixer U1. A VCO derived signal

from the A6A2 assembly is fed through -10 dB attenuator network R1-R3 to pin 1 of the mixer. The resultant IF output is a signal in the range of 3.545 to 3.645 MHz at U1, pins 3 and 4.

This signal is attenuated by -6 dB network R4-R6 and then applied to a low pass filter network to remove all undesirable mixer products. Amplifier stage Q1 boosts this signal to approximately 300 mV_{rms} for application to Phase Detector Assembly A6A4.

4.2 Phase Detector Assembly A6A4 Operation

An IF signal from the A6A3 assembly is converted to TTL levels by high gain limiter stage Q5 and Q6 and divided down to the 354.5 kHz to 364.5 kHz range by divide-by-10 counter U3. This signal is then applied to the IF port of phase comparator U2.

The reference port of U2 is derived from the PLL 3 output, and is also in the 354.5 kHz to 364.5 kHz range after division by divide-by-10 counters U1 and U4.

When the frequency and phase of these signals are equal to the phase comparator outputs at U2, pins 2 and 13 are at + 5 Vdc. All transistors in charge pump network Q1, Q2, and Q3 are biased off. The voltage across C21 is constant, and this will bias transistor A6A2Q2 on the VCO assembly to produce a constant voltage drop across A6A2R9, at A6A2TP1. Consequently, the VCO on the A6A2 assembly is held at a constant frequency.

Assume that the A8 PLL 3 output increases in frequency due to decreasing the values of any of the 10 kHz through 10 Hz frequency display digits. Since the reference signal at the reference port of the phase comparator (pin 1) will suddenly be higher in frequency than the IF derived signal at the IF port, U1 produces an error command to lower the VCO frequency and thereby increase the IF feedback signal. This command is in the form of negative pulses at U2, pin 13. The pulse width of this signal is proportional to the difference in frequency and/or phase between the two phase comparator inputs. When these negative pulses occur, Q2 is forced on and C21 discharges. This causes A6A2Q2 to conduct less, and the level of the VCO control voltage at A6A2TP1 will fall. As it decreases, the VCO frequency decreases, causing a corresponding increase in IF frequency at the mixer A6A3U1 output. As the IF feedback signal at the phase comparator input approaches the reference frequency, the output pulses at A6A4U2, pin 13, get narrower until the signal becomes a 5 Vdc level again. At this point, the two phase comparator inputs are equal in frequency, Q2 is turned off, and the voltage across C21 is constant (but at a new lower value). Consequently, the VCO control voltage is also constant, but at a new lower value, as is the VCO output frequency.

Note that the same sequence of events would have occurred if the A7 PLL 2 output frequency had decreased due to a decrease in the 10 MHz to 100 kHz digits of the displayed frequency.

Assume that the A7 PLL 2 output frequency increases due to increasing the 10 MHz to 100 kHz digits of the frequency display. The instantaneous frequency at mixer A6A3U1 output will increase, causing a corresponding increase at the IF input port of the phase comparator. This signal will be greater in frequency than the reference signal and consequently U1 will issue an error command to raise the VCO frequency in order to lower the mixer output frequency. This time the negative pulses appear at pin 2 of the phase comparator. Q1 is forced on and turns Q3 on and charges C21. This turns A6A2Q1 on harder and a rising voltage occurs at A6A2TP1, the VCO control voltage. This voltage forces the VCO frequency to increase. Mixer A6A3U1 output (IF) frequency therefore decreases and continues to do so until the two signals at the phase comparator inputs are again equal. At that time, the output pulses at U2, pin 2, are essentially at 5 Vdc, Q1 and Q2 turn off, and the VCO control voltage stops at a new higher value (as does the VCO frequency).

Note that the same sequence of events would have occurred if the A8 PLL 3 output decreased in frequency due to increasing any of the digits in the 10 kHz through 1 kHz positions of the frequency display.

4.3 VCO/Loop Filter A6A2 Operation

A charge pump circuit on the A6A4 assembly converts the phase comparator pulse outputs into an analog dc voltage and applies it to terminal E2 of VCO/Loop Filter Assembly A6A2. Q2 generates the actual VCO control voltage across R9 at TP1, and applies the signal through a low pass filter (LPF) network to the varactor diode string in the VCO. The LPF removes any noise transients on the VCO control voltage line which could shift the VCO frequency. The VCO is a JFET Hartley Oscillator stage (Q1) whose frequency shifts as the varactor diodes capacitance changes in response to changes in VCO control voltage. A VCO control voltage range at TP1 of approximately 3.5 Vdc to 19.0 Vdc shifts the VCO frequency from 40.455 MHz to 70.455 MHz.

The VCO output is fed to two separate amplifier stages. The first, Q4, boosts the signal to 0 dBm and routes the signal through P1 to Converter Assembly A2, where it functions as the LO No. 1 injection for mixer A2U1. The second stage is on the A6A1 motherboard and consists of transistors A6A1Q3 and A6A1Q4. This signal is simply referred to as the VCO output, and is boosted to approximately -6 dBm prior to application to mixer A6A3U1. The VCO feedback loop is therefore completed.

4.3.1 Other VCO Control Circuits

There are two other circuits which can cause the VCO control voltage to change. They are the PLL 2 Tracking Reference/Clamp circuit (motherboard transistors A6A1Q1 and A6A1Q2) and the 2 MHz switch circuit (VCO/Loop Filter transistor A6A2Q3).

4.3.1.1 PLL 2 Tracking Reference/Clamp Circuit

The PLL 2 tracking reference/clamp circuit forces the PLL 1 VCO to track the PLL 2 VCO. In so doing, it shortens the exciter tuning time. It also prevents the PLL 2 VCO from running to the wrong side of the frequency conversion in the mixing process, which could cause the loop to fail or lock up.

For example, assume the PLL 2 output is at 74 MHz and the VCO output is at 70.455 MHz (the highest frequency it would normally operate at). The IF frequency produced at the A6A3U1 mixer output would then be (74-70.455 MHz = 3.545 MHz), which is in the normal PLL IF range.

Assume that the VCO exceeds its upper frequency bound, and is now at 77.545 MHz. The IF output at A6A3U1 would again be 3.545 MHz (77.545 MHz - 74 MHz = 3.545 MHz), and the phase comparator would lock, holding the VCO at the wrong frequency.

The potential problem is eliminated by forcing the A6A2 VCO to track the A7 PLL 2 VCO. The PLL 2 VCO does not have a mixer in its feedback path, and therefore does not have this problem. It does, however, contain a VCO circuit which is almost identical to the A6A2 VCO (with respect to control voltage levels and operational frequency). When the PLL 1 VCO control voltage changes from 3.5 to 19.0 Vdc, its frequency changes from 40.455 MHz to 70.455 MHz. When the PLL 2 VCO control voltage changes from 3.5 to 19.0 Vdc, its frequency changes from 44.1 to 74 MHz. Furthermore, whenever the PLL 2 control voltage and VCO frequency change, the PLL 1 control voltage and VCO frequency will always change by almost the same amount.

Knowing that the VCO control voltage levels of both VCOs should always be approximately the same, we could monitor both and know if the PLL 1 VCO frequency is incorrect. If the PLL 1 VCO is incorrect, it will have a different control voltage level than the PLL 2 VCO.

The A6A1 Tracking Reference/Clamp circuit does this monitoring function, as well as forcing the PLL 1 VCO back to the correct control voltage range, if necessary. The PLL 2 tracking reference signal at A6A1P2 is the actual value of the instantaneous A7 control voltage and is applied to the input of the circuit. The clamp's output is PLL 1 VCO control voltage at the PLL 1 VCO input. As long as the two control voltages remain within

approximately ± 1.5 Vdc of each other (due to the diode drops of CR1, CR2, and Q1 or CR3, CR4, and Q2), Q1 and Q2 are nonconducting, and the PLL 1 control voltage is in an acceptable range of ± 1.5 Vdc from the PLL 2 control voltage.

Assume that the PLL 1 control voltage took off, driving the VCO higher in frequency. As soon as the control voltage level exceeded the PLL 2 control voltage plus 1.5 Vdc, Q2 turns on, forcing the PLL 1 control voltage to stop. Simultaneously, the PLL 1 phase comparator would be reacting to this sudden increase in frequency and eventually would pull the control voltage back down to the correct level, at which time Q2 would turn off.

The Tracking Reference/Clamp circuit will act as a "quick reaction" method of holding the PLL 1 VCO to approximately the correct value until the phase comparator can react in the event of a VCO "run away" condition. (Note that Q1 would perform the controlling function if the PLL 1 control voltage dropped 1.5 Vdc below the PLL 2 control voltage.)

4.3.1.2 2 MHz Switch Circuit

At exciter output (transmit) frequencies less than approximately 2 MHz, the VCO control voltage required to drive the VCO is so low that the charge pump circuit on Phase Comparator Assembly A6A4 enters a nonlinear region of operation in an attempt to produce it. In order to correct this (at frequencies less than 2 MHz), the PLL Frequency Synthesizer A7U2 on the PLL 2 assembly outputs a 5 Vdc level to A6A1P1. This level occurs at A6A2E3 and turns Q3 on. Q3, which is connected across the control voltage input at the Q2 base, reduces the control voltage level by switching R7 into the circuit. The net result is that the charge pump on the A6A4 assembly must now force its output to increase the dc level at E2 in order to produce the proper VCO control voltage level at TP1. In so doing, the charge pump pulls itself out of its nonlinear region. At tune frequencies greater than 2 MHz, Q3 is off, and the charge pump functions normally. Note that this same scheme is used on the A7 assembly.

4.4 BITE Circuits

Lock detector A6A4Q4 on Phase Detector Assembly A6A4 monitors the status of the phase comparators outputs, A6A4U2 pins 2 and 13. If either output pulses low and remains low for a period exceeding the time constants of A6A4R10 and A6A4C4, A6A4Q4 turns on and outputs a 5 Vdc signal at (ultimately) connector A6A1J1, pin 5, Lock Detector Output. This immediately flags BITE monitoring circuits on Control Assembly A14 and a front panel fault light indicator will light.

5. MAINTENANCE

The following adjustments should not be made as part of a routine maintenance procedure but only when a failure indicates a definite need. All tests are performed with all connections in normal contact, unless otherwise specified.

5.1 VCO Tracking Adjustment

Perform the following procedures to adjust the VCO.

a. Connect equipment as shown in figure 2.

b. Set the RF-1310 to 29.90000 MHz. Note the VCO control voltage level at A6A2TP1 (should be approximately 16 - 19.0 Vdc).

c. Monitor the PLL 2 tracking reference at A6A1E2 with the DVM. The level should be the same as that noted in step b. If not, adjust PLL 2 Assembly A7C15 until the PLL 2 tracking reference is equal to the PLL 1 VCO control voltage at A6A2TP1.

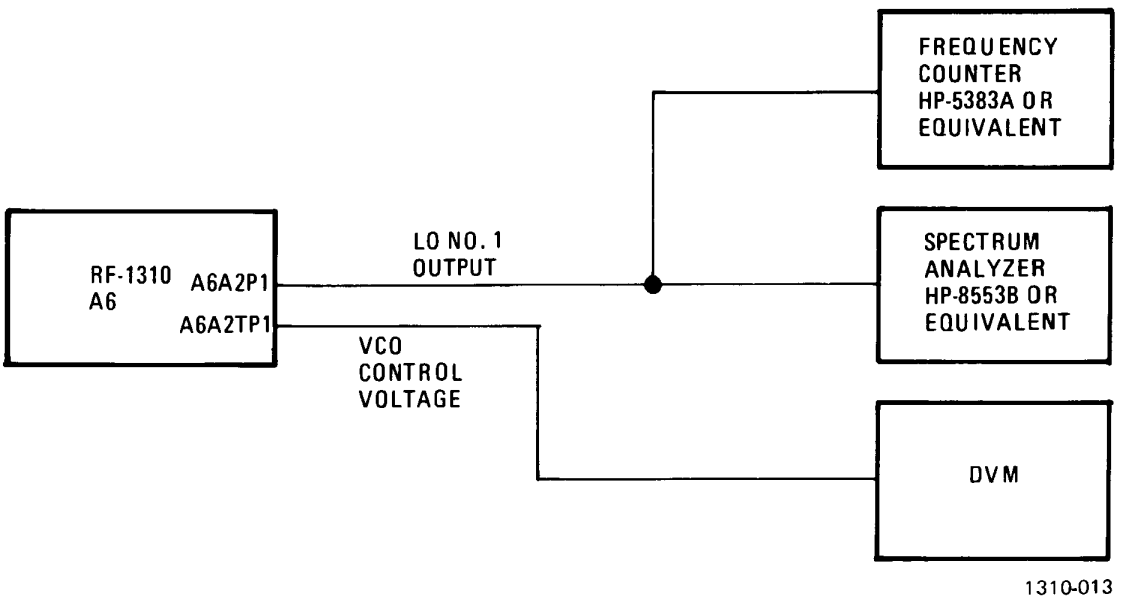


Figure 2. VCO Adjustment

d. Tune the radio to each of the frequencies listed in table 2. At each frequency, the PLL 2 tracking reference and the PLL 1 VCO control voltage should agree within ± .5 Vdc. The LO 1 output should be 0 dBm ± 3 dB at the frequencies indicated.

Table 2. VCO Frequency Range

Exciter Tune Frequency (MHz)	LO No. 1 Output Frequency (MHz)	Approximate PLL 1 VCO Control Voltage (Vdc)
29.90000	70.355000	17.75 ± 1.25
20.00000	60.455000	12.5 ± 1
10.00000	50.455000	7.5 ± 1
1.00000	41.455000	4.0 ± 1

e. Check that the switch input at A6A1E1 does change to approximately 4 ± .5 Vdc when the exciter is tuned below 2 MHz.

f. Reconnect the A6 assembly to the RF-1310 and initiate BITE self test. The exciter should not fail at any test concerning the A6 assembly. The test is now complete.

6. PARTS LISTS, COMPONENT LOCATIONS, AND SCHEMATIC DIAGRAMS

Table 3 lists major assemblies, their reference designators, and their part numbers. Table 4 lists the components of Motherboard Assembly A6A1. Figure 3 shows the component locations for the A6A1 assembly. Figure 4 is the schematic diagram for the A6A1 assembly. This schematic also shows the interconnection information for all the subassemblies that make up the entire A6 assembly. Table 5 lists the parts found in VCO Assembly A6A2. Figures 5 and 6 show the A6A2 assembly component location and schematic diagrams. Table 6 lists the parts found in Mixer Assembly A6A3. Figures 7 and 8 show the A6A3 assembly component location and schematic diagram. Table 7 lists the parts found in Phase Detector Assembly A6A4. Figures 9 and 10 show the A6A4 assembly component location and schematic diagrams.

Table 3. PLL 1 Assembly A6 Parts List (10073-4100-01 Rev. E)

Ref. Desig.	Part Number	Description
4	10073-4126	SHIELD, VCO
5	10073-4136	SHIELD, MIXER
11	10073-4155	SHIELD, PHASE DETECTOR
13	10073-7089	CABLE, COAX ASSY
A1	10073-4110	PWB ASSY, PLL 1 MOTHER BD
A2	10073-4120-01	PWB ASSY, VCO
A3	10073-4130	PWB ASSY, MIXER
A4	10073-4160-01	PWB ASSY, PHASE DETECTOR

Table 4. PLL 1 Motherboard Assembly A6A1 Parts List (10073-4110 Rev. W)

Ref. Desig.	Part Number	Description
5	10073-7214	CLIP, MOUNTING, MODIFIED
12	10073-7088	CABLE, COAX ASSY
18	E70-0002-002	PAD MNT XSTR TO-5
C1	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C3, C4	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C5	C26-0025-100	CAP 10UF 20% 25V TANT
C6	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C7 – C9	M39014/01-1535V	CAP .01UF 10% 100V CER-R
C10	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C11, C12	M39014/01-1535V	CAP .01UF 10% 100V CER-R
C13	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C14	M39014/01-1535V	CAP .01UF 10% 100V CER-R
C15	CM04ED390J03	CAP 39PF 5% 500V MICA
C16, C17	M39014/01-1535V	CAP .01UF 10% 100V CER-R
C20	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C21	C26-0025-100	CAP 10UF 20% 25V TANT
C22, C23	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C24	C26-0016-151	CAP 150UF 20% 16V TANT
C25	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C26	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C27	C26-0035-100	CAP 10UF 20% 35V TANT
C28 – C31	10073-7035	CAP,FEED-THRU 100

Table 4. PLL 1 Motherboard Assembly A6A1 Parts List (10073-4110 Rev. W) (Cont.)

Ref. Desig.	Part Number	Description
CR1	1N3064	DIODE 75mA 75V SW
CR2	1N3064	DIODE 75mA 75V SW
CR3	1N3064	DIODE 75mA 75V SW
CR4	1N3064	DIODE 75mA 75V SW
J1	J46-0022-006	HDR 6 PIN 0.100" SR LKG
L1	82027-03	CHOKE WB 50MHZ
L2	82027-03	CHOKE WB 50MHZ
L3	MS14046-9	COIL 27UH 10% FXD RF
Q1	2N2222	XSTR SS/GP NPN TO-18
Q2	2N2907	XSTR SS/GP PNP TO-18
Q3	Q35-0003-000	XSTR N-CH JFET U310
Q4	2N5109	XSTR RF PWR NPN TO-39
R1	R65-0003-473	RES 47K 5% 1/4W CAR FILM
R2, R3	R65-0003-104	RES 100K 5% 1/4W CAR FILM
R4	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R5	R65-0003-221	RES 220 5% 1/4W CAR FILM
R6	R65-0003-221	RES 220 5% 1/4W CAR FILM
R7, R8	R65-0003-101	RES 100 5% 1/4W CAR FILM
R9	R65-0003-151	RES 150 5% 1/4W CAR FILM
R10	R65-0003-470	RES 47 5% 1/4W CAR FILM
R11	R65-0003-242	RES 2.4K 5% 1/4W CAR FILM
R12	R65-0003-152	RES 1.5K 5% 1/4W CAR FILM
R13	R65-0003-101	RES 100 5% 1/4W CAR FILM
R14	R65-0003-121	RES 120 5% 1/4W CAR FILM
R15	R65-0003-100	RES 10 5% 1/4W CAR FILM
R16	R65-0003-471	RES 470 5% 1/4W CAR FILM
T1, T2	10073-7014	TRANSFORMER, RF, FIXED
VR1	I11-0001-001	IC VR 7805 +5V 1.5A 4%
VR2	1N4737	DIODE 7.5V 10% 1W ZENER

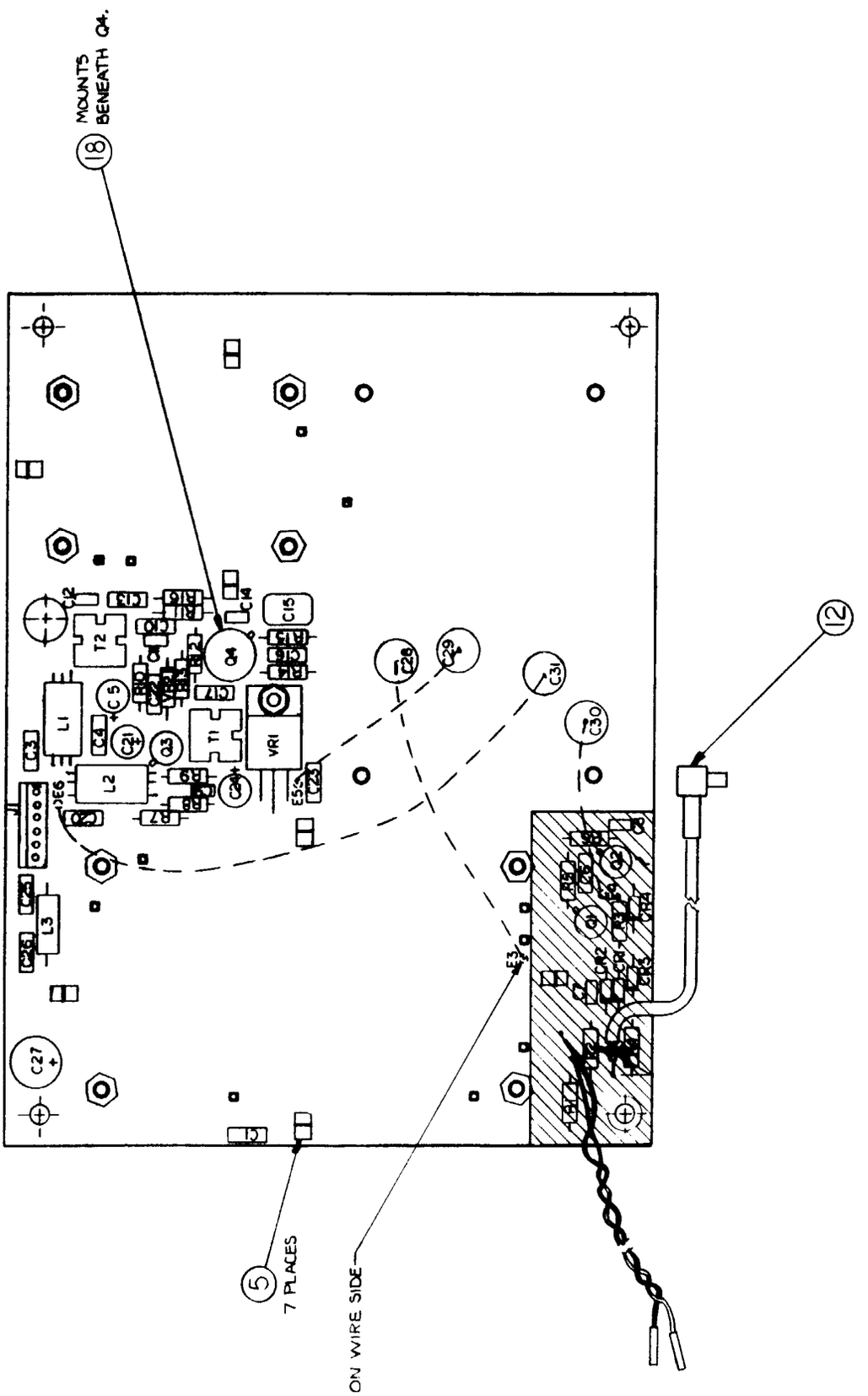


Figure 3. PLL 1 Motherboard A6A1 Component Locations (10073-4110 Rev. D)

NOTE: UNLESS OTHERWISE SPECIFIED:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR A COMPLETE DESIGNATION, PREFIX WITH UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.
2. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, ±5%.
3. ALL CAPACITOR VALUES ARE IN MICROFARADS.
4. VENDOR PART NO. CALLOUTS ARE FOR REFERENCE ONLY. COMPONENTS ARE SUPPLIED PER PART NO. IN PARTS LIST.

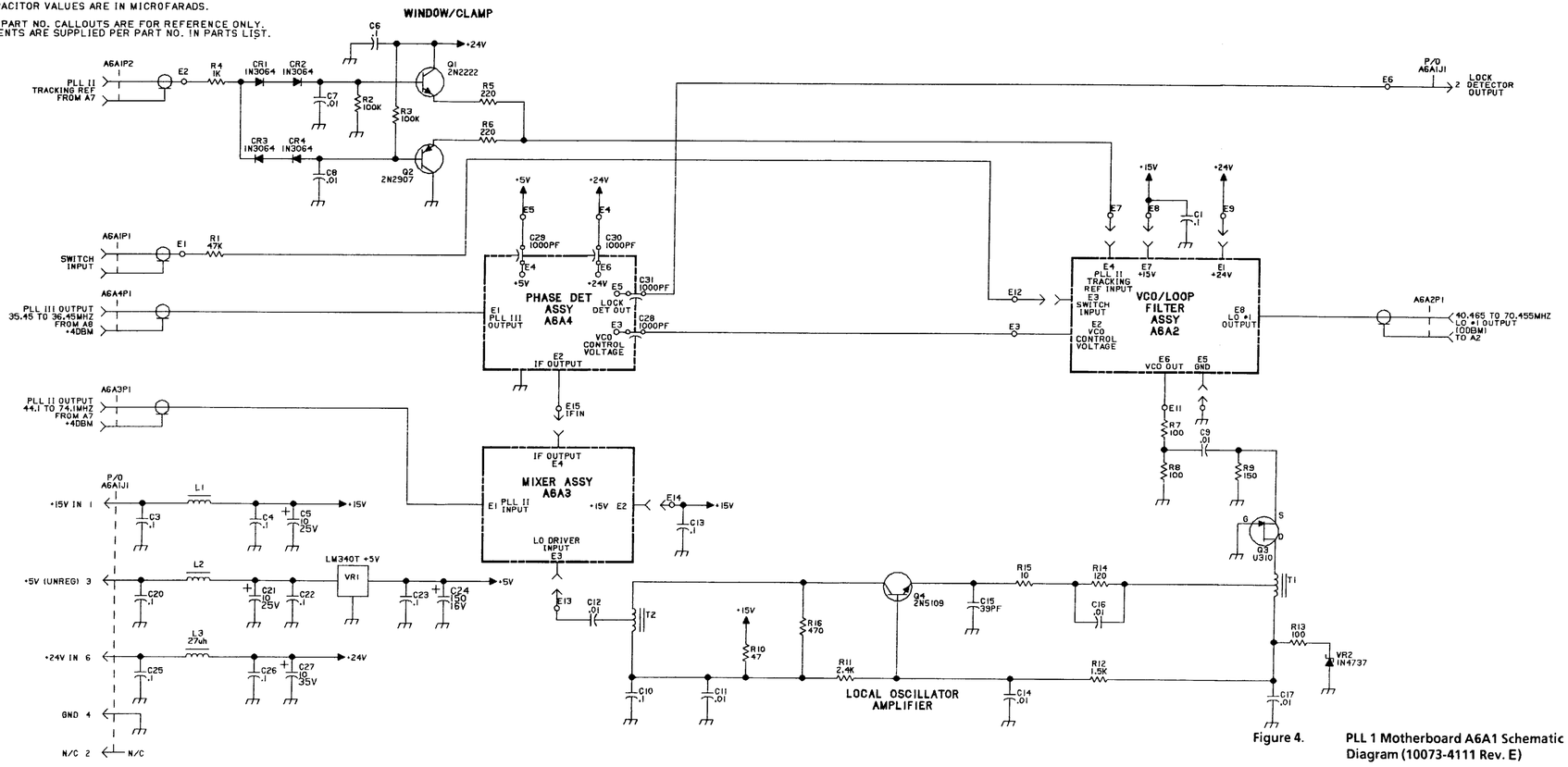


Figure 4. PLL 1 Motherboard A6A1 Schematic Diagram (10073-4111 Rev. E)

Table 5. VCO Board A6A2 Parts List (10073-4120-01 Rev. AB)

Ref. Desig.	Part Number	Description
6	10073-7089	CABLE, COAX ASSY
C1	C26-0025-100	CAP 10UF 20% 25V TANT
C2	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C3	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C4	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C5	C26-0025-100	CAP 10UF 20% 25V TANT
C6	M39014/01-1317V	CAP,1000PF,10% 200VC
C7	C26-0025-339	CAP 3.3UF 20% 25V TANT
C8	M39014/01-1535V	CAP .01UF 10% 100V CER-R
C9	C80-0001-102	CAP FXD POLY .001
C10	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C11	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C12	C26-0035-100	CAP 10UF 20% 35V TANT
C13	M39014/01-1317V	CAP,1000PF,10% 200VC
C14	C26-0035-229	CAP 2.2UF 20% 35V TANT
C15	C-2496	CAP 470PF 2% 500V MICA
C16	C-2495	CAP 430PF 2% 500V MICA
C17	C-2501	CAP 680PF 2% 300V MICA
C18	C80-0001-152	CAP,FXD,POLY .0015
C19	C80-0001-122	CAP,FXD,POLY .0012
C20	C80-0001-182	CAP FXD POLY .0018
C21	C80-0001-122	CAP,FXD,POLY .0012
C22	C80-0001-102	CAP FXD POLY .001
C23	C-2501	CAP 680PF 2% 300V MICA
C24	C-2503	CAP 820PF 2% 300V MICA
C25	C80-0001-102	CAP FXD POLY .001
C26	M39014/01-1535V	CAP .01UF 10% 100V CER-R
C27	M39014/01-1535V	CAP .01UF 10% 100V CER-R
C28	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C29	M39014/01-1317V	CAP,1000PF,10% 200VC
CR1	10073-7118	DIODE VARACTOR
CR2	10073-7118	DIODE VARACTOR
CR3	10073-7118	DIODE VARACTOR
CR4	10073-7118	DIODE VARACTOR
CR5	10073-7118	DIODE VARACTOR
CR6	10073-7118	DIODE VARACTOR
CR7	10073-7118	DIODE VARACTOR
CR8	10073-7118	DIODE VARACTOR
CR9	10073-7118	DIODE VARACTOR
CR10	10073-7118	DIODE VARACTOR
CR11	10073-7118	DIODE VARACTOR
CR12	10073-7118	DIODE VARACTOR

Table 5. VCO Board A6A2 Parts List (10073-4120-01 Rev. AB) (Cont.)

Ref. Desig.	Part Number	Description
CR13	10073-7118	DIODE VARACTOR
CR14	10073-7118	DIODE VARACTOR
CR15	1N6263	DIODE .40W 60V HOT CARR
E1	J47-0004-002	CONTACT SOCKET
E2	J47-0004-002	CONTACT SOCKET
E3 – E7	J47-0004-002	CONTACT SOCKET
JMP1	MP-1142	RES ZERO OHM (CKT JMPR)
L1	MS75084-11	COIL 8.2UH 10% FXD RF
L2	10073-7042	INDUCTOR, 2.4MH
L3	10073-7042	INDUCTOR, 2.4MH
L4	10073-7042	INDUCTOR, 2.4MH
L5	MS75084-3	COIL 1.8UH 10% FXD RF
Q1	Q35-0003-000	XSTR N-CH JFET U310
Q2	2N5088	XSTR SS/GP
Q3	2N2222	XSTR SS/GP NPN TO-18
Q4	Q35-0003-000	XSTR N-CH JFET U310
R1	R65-0003-101	RES 100 5% 1/4W CAR FILM
R2	R65-0003-470	RES 47 5% 1/4W CAR FILM
R3	R65-0003-513	RES 51K 5% 1/4W CAR FILM
R4	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R5	R65-0003-101	RES 100 5% 1/4W CAR FILM
R6	R65-0003-224	RES 220K 5% 1/4W CAR FILM
R7	R65-0003-683	RES 68K 5% 1/4W CAR FILM
R8	R65-0003-223	RES 22K 5% 1/4W CAR FILM
R9	R65-0003-202	RES 2.0K 5% 1/4W CAR FILM
R10	RN55D4641F	RES 4640 1% 1/8W MET FLM
R11	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R12	RN55D4750F	RES 475 1% 1/8W MET FLM
R13	R65-0003-270	RES 27 5% 1/4W CAR FILM
R14	R65-0003-151	RES 150 5% 1/4W CAR FILM
R15	R65-0003-101	RES 100 5% 1/4W CAR FILM
T1	10073-7002	TRANSFORMER, RF, FIXED
T2	10073-7014	TRANSFORMER, RF, FIXED
TP1	J-0071	TP PWB BRN TOP ACCS .080"
VR1	I12-0006-012	IC VR 78L12A +12V .10A 4%

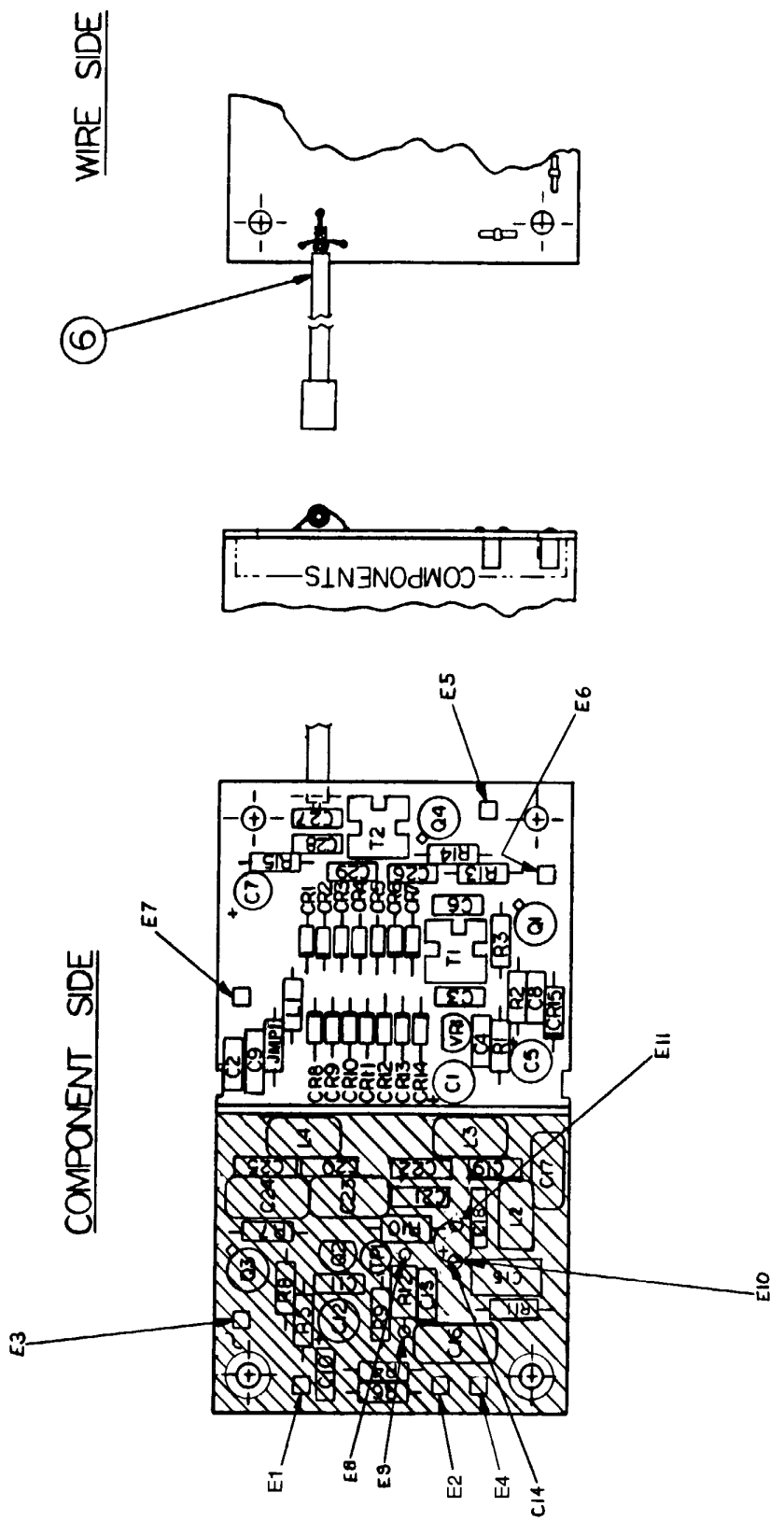


Figure 5. VCO Board A6A2 Component Location Diagram (10073-4120-01 Rev. J)

NOTE: UNLESS OTHERWISE SPECIFIED:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR A COMPLETE DESIGNATION, PREFIX WITH UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.
2. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, ±5%.
3. ALL CAPACITOR VALUES ARE IN MICROFARADS.
4. CR1-CR14 ARE KV3901.
5. VENDOR PART NO. CALLOUTS ARE FOR REFERENCE ONLY. COMPONENTS ARE SUPPLIED PER PART NO. IN PARTS LIST.
6. ON 10073-4120-02 ASSY'S : R12 = RN55D8250F, C14 = CK06BX474M
7. L5 MAY BE REQUIRED ON SOME ASSY'S TO OBTAIN THE DESIRED CONTROL VOLTAGE RANGE AND TRACKING.

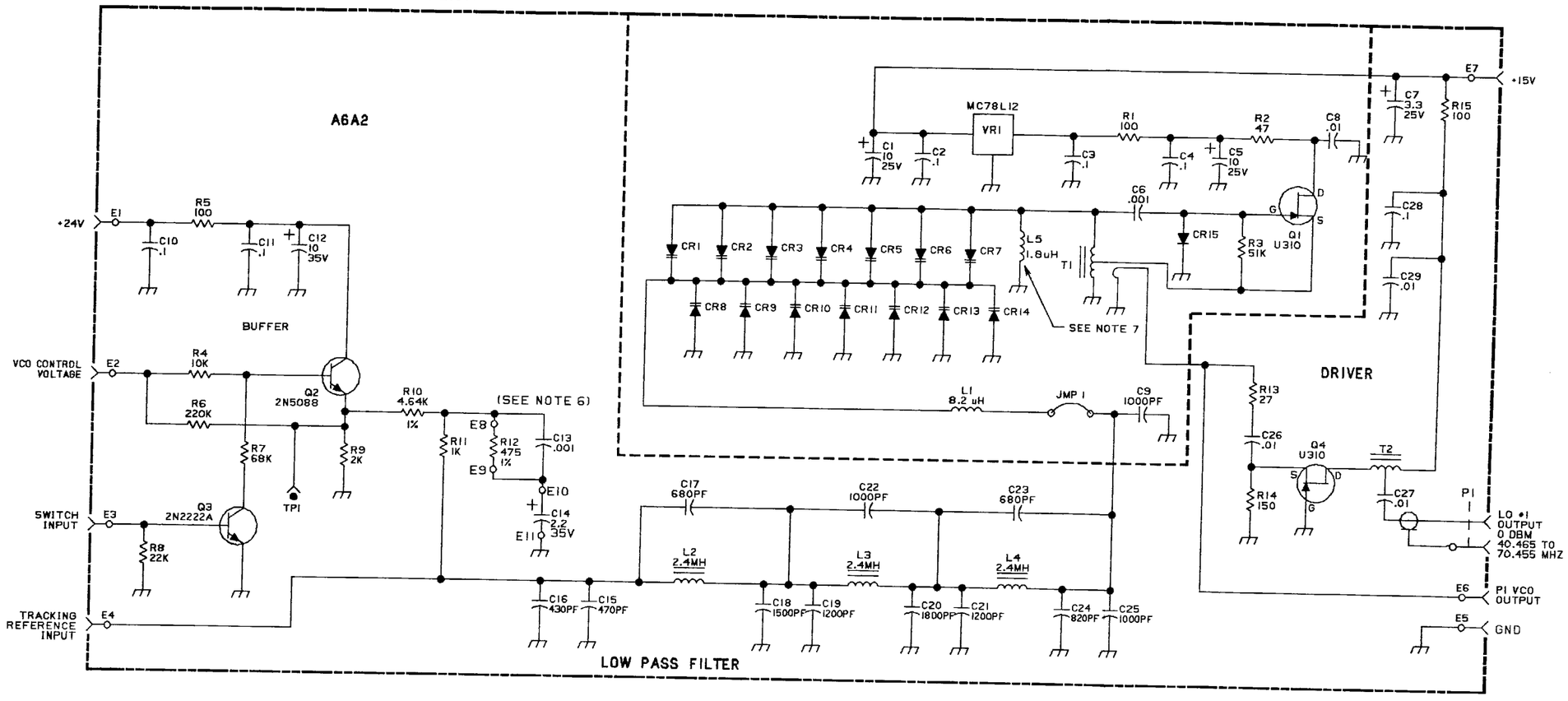


Figure 6. VCO Board A6A2 Schematic Diagram (10073-4121 Rev. J)

Table 6. Mixer Board A6A3 Parts List (10073-4130 Rev. K)

Ref. Desig.	Part Number	Description
6	10073-7087	CABLE, COAX ASSY
C1	CM04FD151J03	CAP 150PF 5% 500V MICA
C2	CM04FD151J03	CAP 150PF 5% 500V MICA
C3	CM04ED330J03	CAP 33PF 5% 500V MICA
C4	CM04FC271J03	CAP 270PF 5% 300V MICA
C5	CM04FC301J03	CAP 300PF 5% 300V MICA
C6	CM04FD151J03	CAP 150PF 5% 500V MICA
C7	CM04FC271J03	CAP 270PF 5% 300V MICA
C8	CM04FC271J03	CAP 270PF 5% 300V MICA
C9	CM04FD121J03	CAP 120PF 5% 500V MICA
C10	CM04FD111J03	CAP 110PF 5% 500V MICA
C11	CM04FD121J03	CAP 120PF 5% 500V MICA
C12	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C13	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C14	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C15	M39014/02-1310V	CAP .1UF 10% 100V CER-R
L1	MS18130-9	COIL 1.2UH 10% FXD RF
L2	MS18130-9	COIL 1.2UH 10% FXD RF
L3	MS18130-8	COIL 1.0UH 10% FXD RF
L4	MS75085-7	COIL 100UH 10% FXD RF
Q1	2N2369	XSTR SS/RF NPN
R1	R65-0002-101	RES 100 5% 1/8W CAR FILM
R2	R65-0002-750	RES 75 5% 1/8W CAR FILM
R3	R65-0002-101	RES 100 5% 1/8W CAR FILM
R4	R65-0002-151	RES 150 5% 1/8W CAR FILM
R5	R65-0002-390	RES 39 5% 1/8W CAR FILM
R6	R65-0002-151	RES 150 5% 1/8W CAR FILM
R7	R65-0002-560	RES 56 5% 1/8W CAR FILM
R8	R65-0002-103	RES 10K 5% 1/8W CAR FILM
R9	R65-0002-201	RES 200 5% 1/8W CAR FILM
R10	R65-0002-472	RES 4.7K 5% 1/8W CAR FILM
R11	R65-0002-100	RES 10 5% 1/8W CAR FILM
R12	R65-0002-471	RES 470 5% 1/8W CAR FILM
U1	I51-0003-003	MIXER DB SRA-1

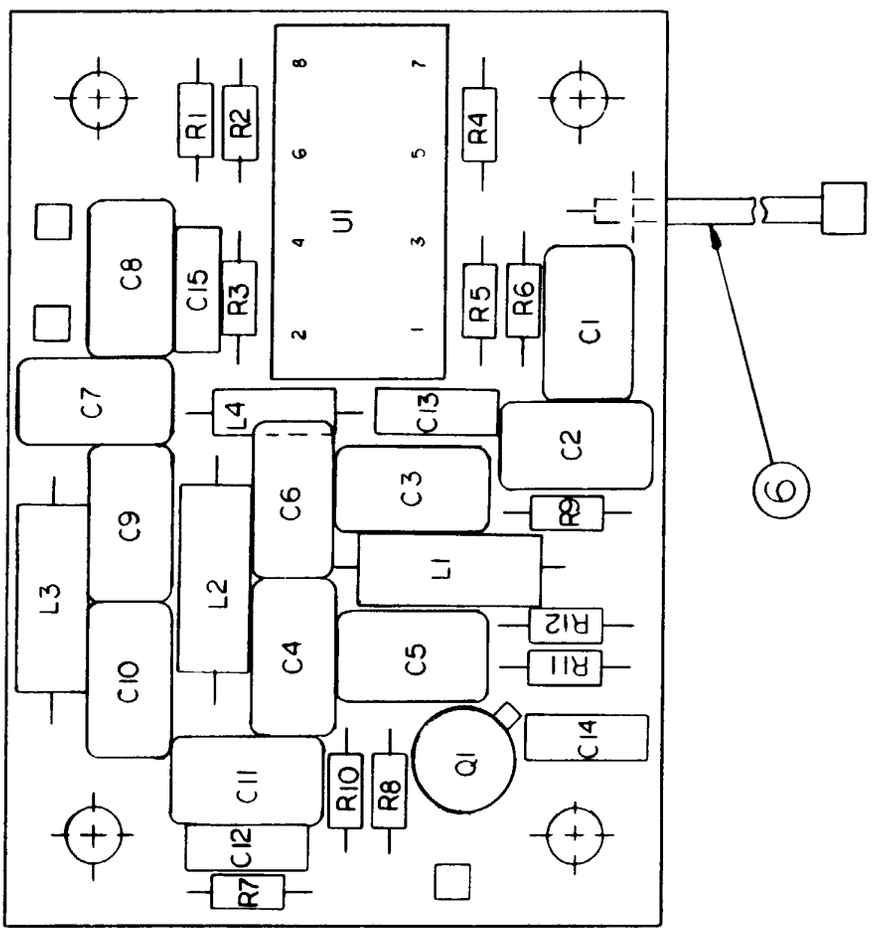


Figure 7. Mixer Board A6A3 Component Location Diagram (10073-4130 Rev. C)

NOTE: UNLESS OTHERWISE SPECIFIED:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR A COMPLETE DESIGNATION, PREFIX WITH UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.
2. ALL RESISTOR VALUES ARE IN OHMS, 1/8W, ±5%.
3. ALL CAPACITOR VALUES ARE IN MICROFARADS.
4. VENDOR PART NO. CALLOUTS ARE FOR REFERENCE ONLY. COMPONENTS ARE SUPPLIED PER PART NO. IN PARTS LIST.
5. ALL INDUCTOR VALUES ARE IN MICROHENRIES.

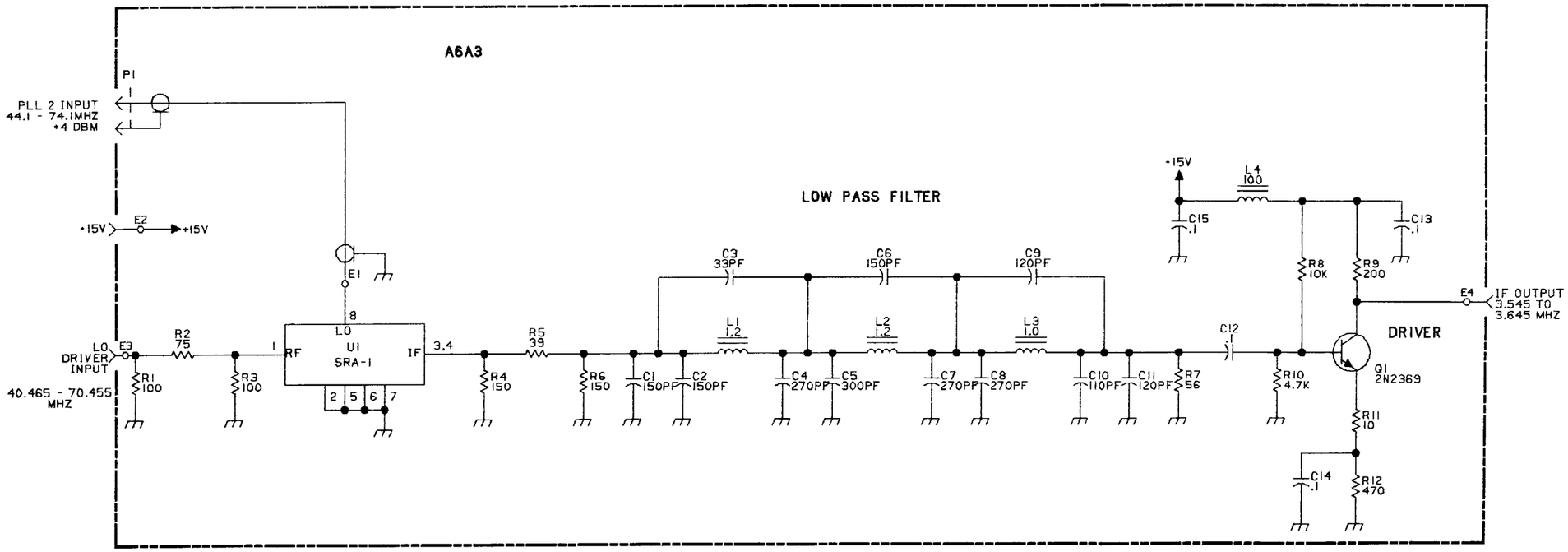


Figure 8. Mixer Board A6A3 Schematic Diagram (10073-4131 Rev. C)

Table 7. Phase Detector Board A6A4 Parts List (10073-4160-01 Rev. N)

Ref. Desig.	Part Number	Description
5	E70-0002-002	PAD MNT XSTR TO-5
6	W10-0005-888	WIRE #24 GRAY
C1	CM04ED330J03	CAP 33PF 5% 500V MICA
C2	CM04ED270J03	CAP 27PF 5% 500V MICA
C3	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C4	C26-0035-109	CAP 1.0UF 20% 35V TANT
C5	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C6	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C7	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C8	M39014/01-1535V	CAP .01UF 10% 100V CER-R
C9	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C10	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C11	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C12	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C13	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C14	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C15	C25-0003-411	CAP 150UF 10% 15V TANT
C16	C26-0025-100	CAP 10UF 20% 25V TANT
C17	C26-0035-100	CAP 10UF 20% 35V TANT
C18	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C19	C26-0035-220	CAP 22UF 20% 35V TANT
C20	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C21	C26-0035-229	CAP 2.2UF 20% 35V TANT
C22	CM04ED200J03	CAP 20PF 5% 500V MICA
CR1	1N3064	DIODE 75mA 75V SW
CR2	1N3064	DIODE 75mA 75V SW
CR3	1N3064	DIODE 75mA 75V SW
CR4	1N3064	DIODE 75mA 75V SW
L1	82027-03	CHOKE WB 50MHZ
L2	MS75084-14	COIL 15.0UH 10% FXD RF
Q1	2N3866	XSTR SS/RF NPN TO-39
Q2	2N3866	XSTR SS/RF NPN TO-39
Q3	2N5160	XSTR RFPWR PNP
Q4	2N2907	XSTR SS/GP PNP TO-18
Q5	Q-0153	XSTR SS/RF PN4258
Q6	2N2369	XSTR SS/RF NPN
R1	R65-0003-680	RES 68 5% 1/4W CAR FILM
R2	RN55D4990F	RES 499 1% 1/8W MET FLM
R3	RN55D2002F	RES 20.0K 1% 1/8W MET FLM
R4	RN55D4990F	RES 499 1% 1/8W MET FLM
R5	R65-0002-332	RES 3.3K 5% 1/8W CAR FILM
R6	RN55D1821F	RES 1820 1% 1/8W MET FLM
R7	R65-0002-332	RES 3.3K 5% 1/8W CAR FILM

Table 7. Phase Detector Board A6A4 Parts List (10073-4160-01 Rev. N) (Cont.)

Ref. Desig.	Part Number	Description
R8	RN55D4990F	RES 499 1% 1/8W MET FLM
R9	R65-0002-221	RES 220 5% 1/8W CAR FILM
R10	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R11	R65-0002-472	RES 4.7K 5% 1/8W CAR FILM
R12	R65-0002-472	RES 4.7K 5% 1/8W CAR FILM
R13	R65-0002-472	RES 4.7K 5% 1/8W CAR FILM
R14	R65-0002-391	RES 390 5% 1/8W CAR FILM
R15	R65-0003-241	RES 240 5% 1/4W CAR FILM
R16	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R17	R65-0003-332	RES 3.3K 5% 1/4W CAR FILM
R18	R65-0002-270	RES 27 5% 1/8W CAR FILM
R19	R65-0003-331	RES 330 5% 1/4W CAR FILM
R20	R65-0003-562	RES 5.6K 5% 1/4W CAR FILM
R21	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R22	R65-0002-101	RES 100 5% 1/8W CAR FILM
R23	RN55D4990F	RES 499 1% 1/8W MET FLM
U1	I65-0004-001	IC PRESCALER 10/11 12013
U2	IC-0430	IC 4044 PLASTIC CMOS
U3	I05-0000-090	IC 74LS90 PLASTIC TTL
U4	I05-0000-090	IC 74LS90 PLASTIC TTL

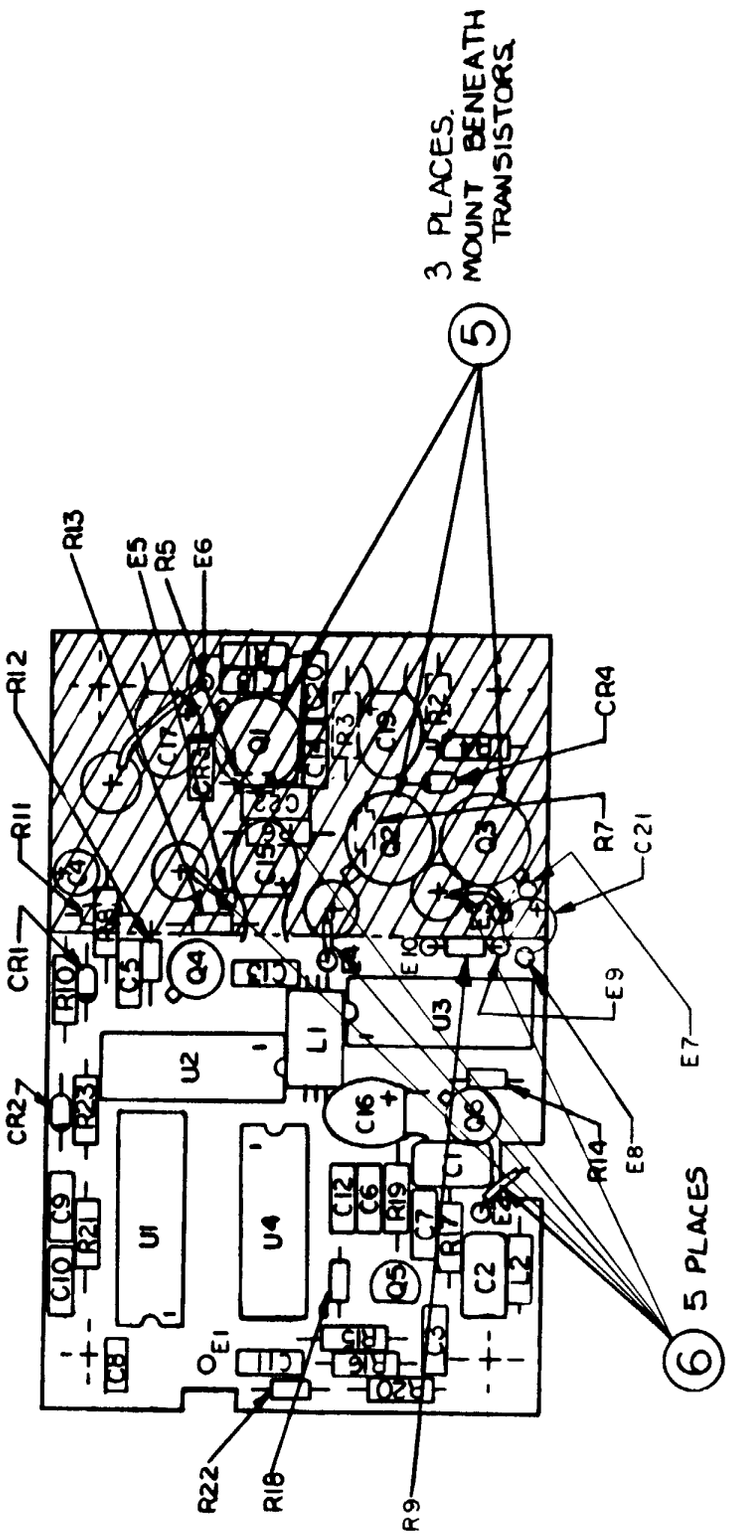


Figure 9. Phase Detector Board A6A4 Component Location Diagram (10073-4160-01 Rev. J)

NOTE: UNLESS OTHERWISE SPECIFIED:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR A COMPLETE DESIGNATION, PREFIX WITH UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.
2. ALL RESISTOR VALUES ARE IN OHMS, 1/8W, ±5%.
3. ALL CAPACITOR VALUES ARE IN MICROFARADS.
4. VENDOR PART NO. CALLOUTS ARE FOR REFERENCE ONLY. COMPONENTS ARE SUPPLIED PER PART NO. IN PARTS LIST.
5. ON 10073-4160-02 ASSY'S : R9 = R65-0002-511: C21 = CK06BX474M

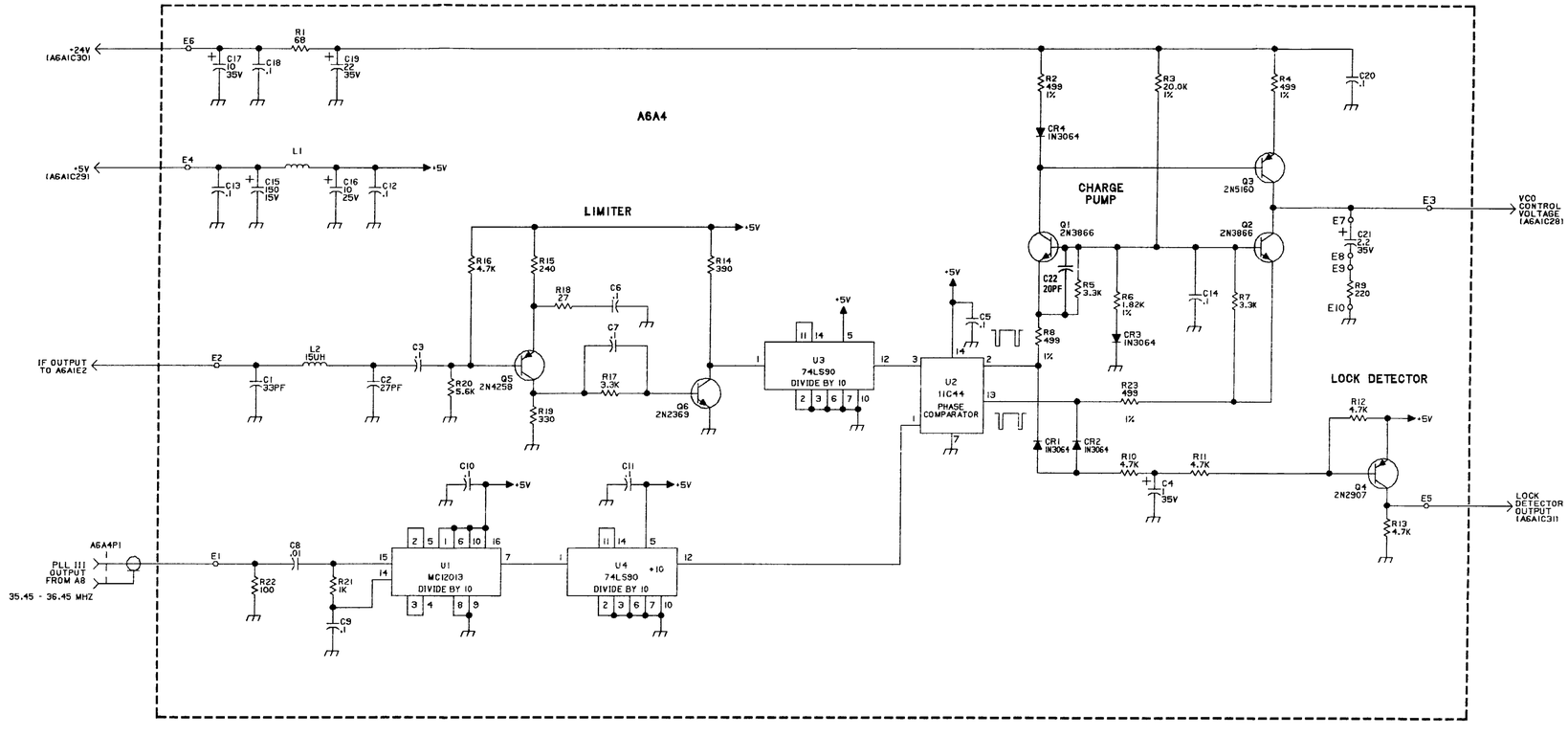
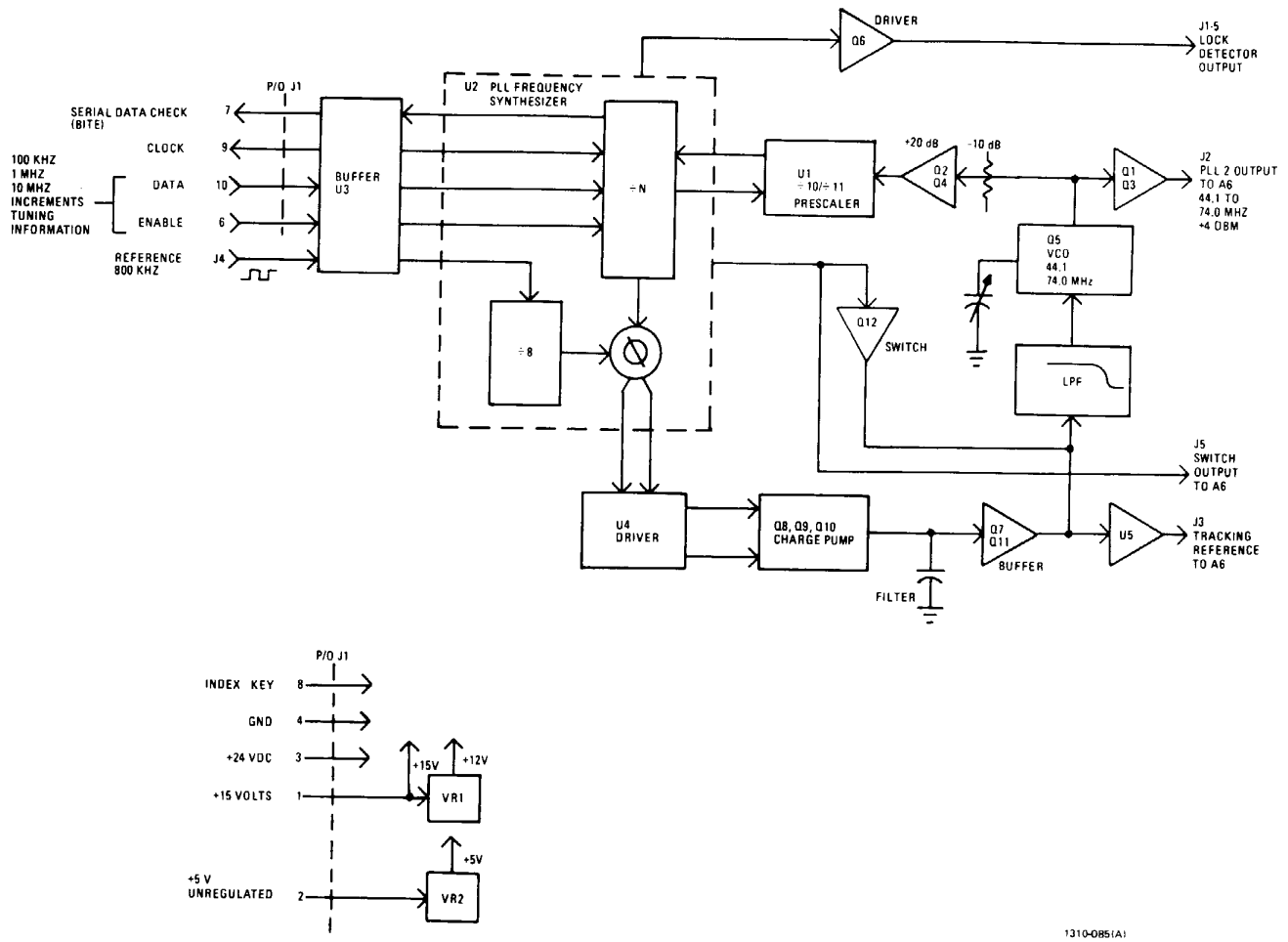


Figure 10. Phase Detector Board A6A4 Schematic Diagram (10073-4161 Rev. E)

A7
PLL 2 ASSEMBLY



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PLL 2 ASSEMBLY A7

1. GENERAL DESCRIPTION

PLL 2 Assembly A7 is a single, phase locked loop synthesizer that ultimately provides the 100 kHz, 1 MHz, and 10 MHz tuning increments of the LO 1 signal used to produce the transmit frequency selected on the front panel. Figure 1 shows the location of PLL 2 Assembly A7 in the RF-1310 chassis.

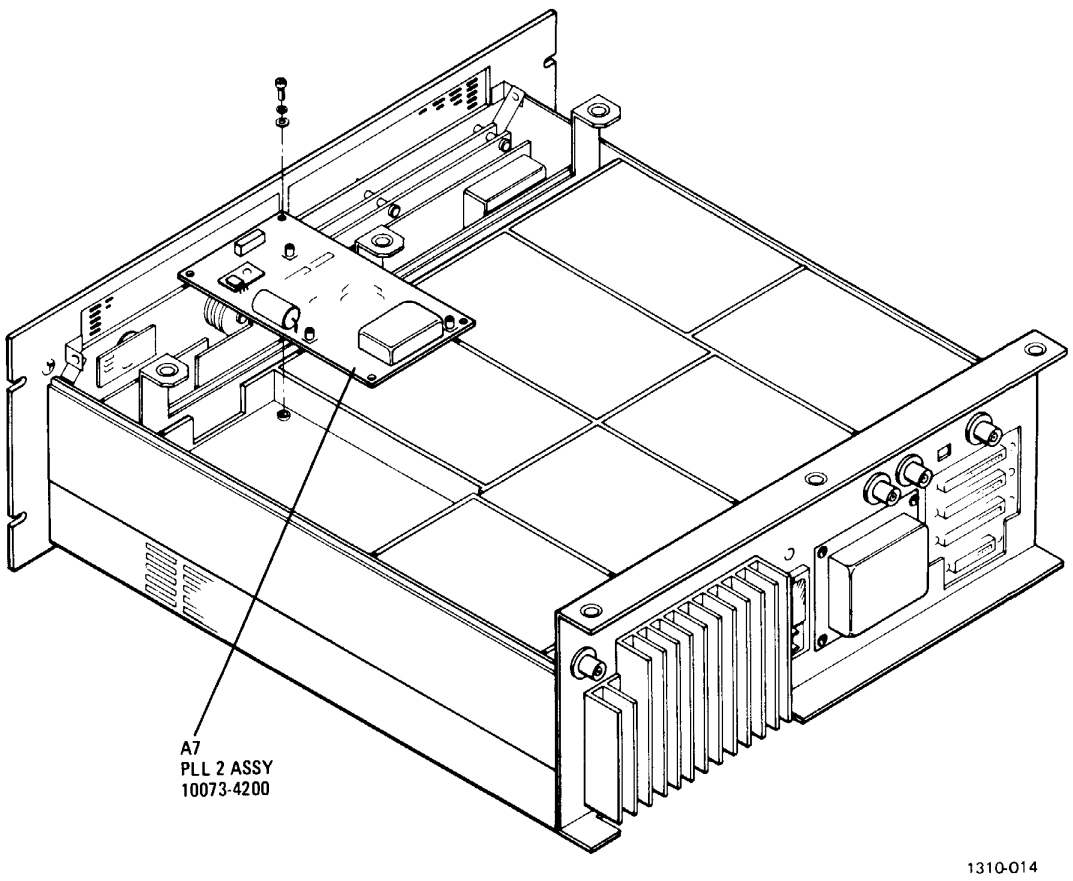


Figure 1. PLL 2 Assembly A7 Location

Frequency select input data is applied to the assembly in serial data form under Control Board Assembly A14 microprocessor control. The A7 output to PLL 1 Assembly A6 is a variable 44.1 to 74.0 MHz signal in 100 kHz controllable steps. The net result of A7 operation is to provide coarse tuning increments (100 kHz, 1 MHz, and 10 MHz) for LO 1 signal.

2. INTERFACE CONNECTIONS

Table 1 details the various input/output connections and other relevant data.

Table 1. PLL 2 Assembly Interface Connections

Connector	Function	Characteristics
J1-1	+ 15 Volts	Approximately 25 mA
J1-2	5 Volts Unregulated	Approximately 240 mA
J1-3	+ 24 Volts	Approximately 20 mA
J1-4	Ground	
J1-5	Lock Detector Output	5 Vdc = unlocked; 0 Vdc = locked
J1-6	Enable	+ going pulse = enabled
J1-7	Serial Data Check	P/O BITE Test, + 5 Vdc = ok
J1-8	Key	
J1-9	Clock	TTL, 750 kHz
J1-10	Data	Serial TTL
J2	PLL 2 (A7) Output	+ 4 dBm/50 ohms, 44.1 to 74.0 MHz
J3	PLL 2 Tracking Reference	3.5 to 19 Vdc
J4	800 kHz Reference Input	TTL
J5	Switch Output	+ 4 V for less than 2 MHz tune frequency 0 V for greater than or equal to 2 MHz tune frequency

3. CIRCUIT DESCRIPTION

NOTE

A7 operation is similar (in operation) to that of the general divide-by-N PLL and charge pump circuits described in section 4. A review of section 4 at this point would aid in the understanding of A7 assembly operation.

3.1 Reference Generation

The 800 kHz signal from Reference Generator Assembly A12 enters PLL 2 Assembly A7 at J4. This signal is applied via buffer U3 to a divide-by-eight counter internal to U2 to produce a 100 kHz reference signal. Since this has been derived ultimately from the RF-1310 crystal frequency standard via the A12 assembly, stable and accurate A7 operation is assured.

3.2 Divide-By-N Counter

Since the A7 assembly must generate a variable 44.1 to 74.0 MHz output frequency, a programmable counter has been designed into the VCO feedback path to the phase comparator. This counter consists of dual modulus divide-by-10/divide-by-11 prescaler U1 and a programmable counter internal to U2. Together, U1 and the programmable portion of U2 create a total division range of N = 441 to N = 740, where N is a function of the digits in the 10 MHz, 1 MHz, and 100 kHz positions of the frequency display.

The output of the divide-by-N counter will always attempt to equal the 100 kHz reference frequency at the Phase Comparator inputs, despite changes in the divide-by-N factor due to changing the 10 MHz, 1 MHz, and/or 100 kHz digits of the displayed frequency. The VCO frequency will change to accomplish this, in response to command signals generated by the phase comparator. The VCO frequency will always equal (N) (reference frequency), or (N) (100 kHz) = 44.1 MHz to 74.0 MHz. The exact value of N is determined by the digits in the 10 MHz, 1 MHz, and 100 kHz positions of the frequency display. This front panel selection causes Control Assembly A14 to generate a serial data code containing information pertaining to the values of the increments chosen. This code is applied synchronously with the 750 kHz system clock to U2 whenever the U2 enable line is gated open by A14. In general, N = (441 + XXX), where XXX are the digits in the 10 MHz, 1 MHz, and 100 kHz positions of the frequency display.

For example, tuning the RF-1310 to 15.789000 MHz would make N = (441 + 157) = 598. The VCO frequency will be (N) (Reference) = (598) (100 kHz) = 59.8 MHz.

Tuning the radio to 24.705000 MHz would result in a VCO output frequency of (441 + 247) (100 kHz) = 68.8 MHz. Note that increasing the tune frequency causes an increase in the A7 output frequency. The opposite will also be true.

3.3 Phase Comparator and Charge Pump Operation

Phase comparison of the 100 kHz reference and the 100 kHz divide-by-N counter VCO derived signal is accomplished by a phase comparator internal to U2. When these two signals are equal in frequency and phase, the buffered phase comparator outputs at TP2 and TP3 are essentially 5 Vdc. This 5-volt level holds charge pump transistors Q9 and Q10 on, and consequently, Q8 off. The voltage across C51 will be at a constant value, forcing buffers Q7 and Q11 to develop a stable voltage at TP1. This VCO control voltage holds the VCO frequency constant somewhere between 44.1 MHz and 74.0 MHz.

Assume that the VCO feedback signal at the divide-by-N counter output is suddenly less than the reference frequency, which is what happens at the instant the divide-by-N factor is increased. Since the two phase comparator inputs are no longer equal, the phase comparator will output a series of negative pulses at TP3. The pulse width of these pulses is a function of the difference in phase/frequency between the two inputs. Q10 turns on, and its decreasing collector voltage turns Q8 on. Q8 will start to pump charge into C51, raising its voltage. Buffer stage Q7 and Q11 will produce a corresponding increase at TP1 which forces the VCO to increase in frequency. The increasing VCO signal produces a corresponding frequency increase at the divide-by-N counter output, driving it towards the reference signal at 100 kHz. As the divide-by-N counter output approaches the reference frequency, the pulses at TP3 get narrower, until they are at an essentially constant + 5 Vdc level. Q10 and Q8 turn off, and the voltage rise across C51 stops at a new higher level, producing a stabilization of the VCO control voltage and the VCO frequency at a new higher value.

Assume that the VCO feedback signal is suddenly greater than the reference frequency, which is what occurs at the instant the divide-by-N factor is decreased. The phase comparator outputs a series of negative pulses at TP2. Q9 turns on, and starts drawing charge out of C51, dropping its voltage. A corresponding decrease in the VCO control voltage occurs, producing a decreasing VCO frequency. This causes the feedback VCO divide-by-N counter output to decrease, driving it towards the 100 kHz reference. As the divide-by-N counter output approaches the reference, the negative pulses at TP2 become narrower, until the signal becomes a 5 Vdc level. Q9 turns off, and stops any further decrease in the C51 voltage, the VCO control voltage, and therefore the VCO frequency. The VCO now generates a lower frequency.

Note that the VCO control voltage at Q7 and Q11 is sent to two places. They are the LPF and VCO on the A7 assembly and buffer stage U5. This second output is referred to as the Tracking Reference, and is routed through J3 for use on PLL 1 Assembly A6. It allows the A6 VCO to properly track the A7 VCO.

3.4 VCO Operation and Control

A charge pump circuit consisting of Q8-Q10 and associated components converts the two phase comparator pulse ouputs into an analog dc control voltage. Buffer stages Q7 and Q11 apply the VCO control voltage through a low pass filter (LPF) network to the varactor diode string in the VCO. The VCO itself is a JFET (Q5) Hartley oscillator stage whose frequency shifts as the capacitance of the varactor diodes change in response to changes in VCO control voltage. A VCO control voltage range of approximately 3.5 Vdc to 19.0 Vdc shifts the VCO from 44.1 MHz to 74.0 MHz.

The VCO output is fed to two separate amplifier stages. The first, Q4 and Q2, is a 20 dB amplifier which applies the VCO signal to the divide-by-10/divide-by-11 prescaler, U1. It is this signal which completes the feedback loop to the phase comparator. The second amplifier stage, Q3 and Q1, boosts the level to approximately 4 dBm and is called the PLL 2 output. This signal contains the 10 MHz, 1 MHz, and 100 kHz portions of the LO 1 signal, and is fed to PLL 1 Assembly A6 for further processing.

3.5 Noise Reduction Techniques

The noise characteristics of the VCO output are enhanced by the following two methods:

- Use of a sharp cutoff LPF network to filter noise off the VCO control voltage. This stage is located between charge pump buffer stage Q11 and the VCO input.

- Use of a circuit to make charge pump operation linear at exciter tune frequencies less than 2 MHz. Lower exciter tune frequencies require less VCO control voltage than higher exciter tune frequencies. At tune frequencies less than 2 MHz, the VCO control voltage required is so low that the charge pump enters a nonlinear mode of operation in an attempt to produce the output across C51 that is required. In order to correct this at frequencies less than 2 MHz, U2 outputs a 5 Vdc level which turns Q12 on. Q12, which is connected across the LPF input, reduces the control voltage level. The net result is that the charge pump is now "tricked" into forcing its output to increase the voltage across C51 required to produce the required VCO control voltage. In so doing, it pulls itself out of its nonlinear region. At frequencies greater than 2 MHz, Q12 is off and the charge pump functions normally. Note that this switch output from U2 is routed through J5 to the A6 assembly for similar purposes.

3.6 BITE Circuits

The A7 assembly contains two circuits for self-test evaluation.

- Lock detector Q6, whose output is 0 Vdc whenever the PLL is tracking properly. This line is constantly monitored by the A14 assembly. A front panel fault light will appear if the loop ever unlocks.

- Serial data check verifies that the tuning data from the A14 assembly has been received and properly translated into the correct divide-by-N factor. A serial data word is sent on the data line (J1 pin 10) and the U6 serial data check line is read back to the A14 assembly (J1 pin 7). If the word has been received and properly decoded, this line will pulse to + 5 Vdc. The serial data check occurs automatically, but only when the BITE self test is actuated.

4. MAINTENANCE

The following adjustments should not be performed as a routine maintenance procedure, but only when a failure indicates a definite need. Perform all tests with all connections in normal contact, unless otherwise specified.

4.1 VCO Frequency Adjustment

a. Connect equipment as shown in figure 2.

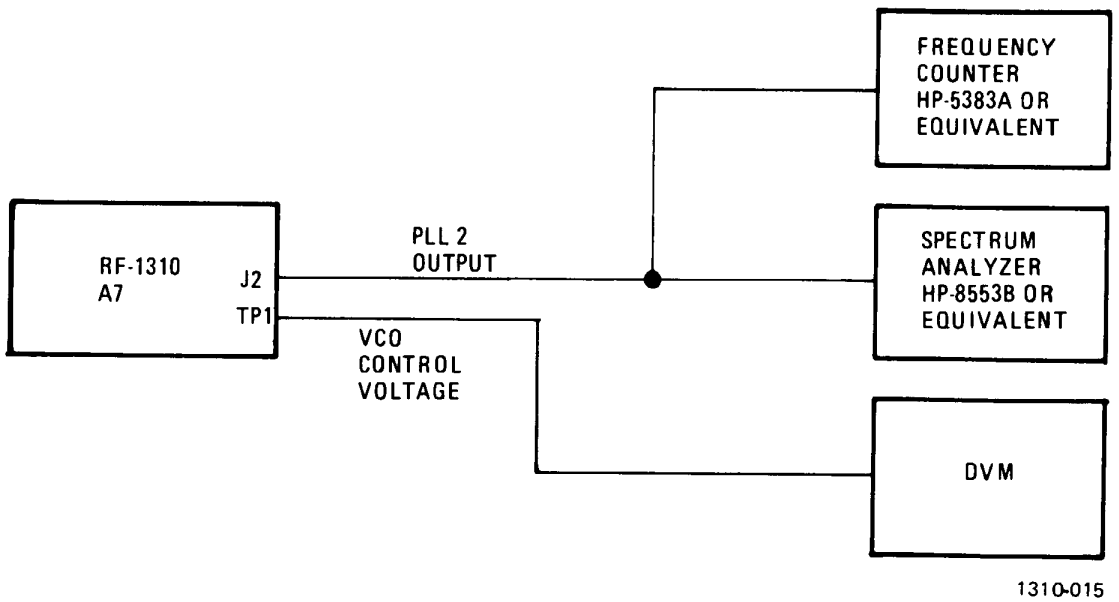


Figure 2. VCO Adjustment

b. Set RF-1310 frequency to 29.900000 MHz.

c. Adjust C15 for a nominal voltage of 16.5 - 19.0 Vdc at TP1. PLL 2 output at J2 should be 74.0 MHz, 4 dBm ± 3 dB. Check the exciter tune frequency against PLL II output frequencies listed in table 2. Output should remain at + 4 dBm ± 3 dB.

d. Check that the Tracking Reference Signal (J3) agrees within ± 1 Vdc to the control voltage at TP1 for the ranges listed in table 2.

Table 2. VCO Frequency Range

Exciter Tune Frequency, MHz	PLL 2 Output Frequency, MHz	Approximate TP1 Voltage, Vdc
29.900000	74.000000	18.0
15.000000	59.100000	9.0
00.100000	44.200000	3.5

e. Check that the switch output (J5) changes to approximately 4 Vdc when the exciter is tuned below 2.000000 MHz.

f. Fully reconnect the A7 assembly to the RF-1310 and initiate BITE test. Exciter should not fail at any test concerning the A7 assembly. These tests have verified the proper operation of the A7 assembly. Proceed to paragraph 4.2, Tracking Adjustment.

4.2 Tracking Adjustment

a. Perform VCO adjustment found in paragraph 4.1.

b. Tune the RF-1310 to 29.99999 MHz.

c. Measure the VCO control voltage at TP1 on PLL 1 VCO Assembly A6A2. Note that TP1 is located under the VCO assembly cover. This voltage should be 16 to 19.0 Vdc on a properly aligned A6 assembly.

d. Measure PLL 2 Assembly A7 VCO control voltage at TP1, and adjust C15 for a voltage equal to that of the A6 PLL 1 VCO control voltage (step c).

e. Tune the exciter to 20 MHz, then 10 MHz, and then 2 MHz, measuring the VCO control voltages on both assemblies at each frequency. The two voltages should track each other at all times, and differ by no more than ± .5 Vdc. Test is now complete.

5. PARTS LIST, COMPONENT LOCATIONS, AND SCHEMATIC DIAGRAM

All replaceable components of the A7 assembly are listed in table 3. Component locations can be found in figure 3. Figure 4 is a schematic diagram of PLL 2 Assembly A7.

Table 3. PLL 2 Assembly A7 Parts List (10073-4200 Rev. AB)

Ref. Desig.	Part Number	Description
4	10073-7214	CLIP MOUNTING,MODIFIED
5	10073-7116	CAN RECT DEEP DRAWN
6	MP-0287	CONNECTOR PIN
11	10073-7106	HEATSINK PLATE
12	E70-0002-002	PAD MNT XSTR TO-5
C1	M39014/01-1535V	CAP .01UF 10% 100V CER-R
C2	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C3	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C4	M39014/01-1535V	CAP .01UF 10% 100V CER-R
C5	M39014/01-1535V	CAP .01UF 10% 100V CER-R
C6	M39014/01-1535V	CAP .01UF 10% 100V CER-R
C7	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C8	M39014/01-1535V	CAP .01UF 10% 100V CER-R
C9	C26-0025-100	CAP 10UF 20% 25V TANT
C10	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C11	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C12	C26-0025-100	CAP 10UF 20% 25V TANT

Table 3. PLL 2 Assembly A7 Parts List (10073-4200 Rev. AB) (Cont.)

Ref. Desig.	Part Number	Description
C13	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C14	M39014/01-1535V	CAP .01UF 10% 100V CER-R
C15	C85-0001-002	CAP VAR 1-10PF PIST
C16	M39014/01-1317V	CAP,1000PF,10% 200VC
C17	M39014/01-1317V	CAP,1000PF,10% 200VC
C18	C26-0025-100	CAP 10UF 20% 25V TANT
C19	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C20	C26-0025-100	CAP 10UF 20% 25V TANT
C21	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C22	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C23	C26-0025-100	CAP 10UF 20% 25V TANT
C24	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C25	M39014/01-1535V	CAP .01UF 10% 100V CER-R
C28	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C29	M39014/01-1535V	CAP .01UF 10% 100V CER-R
C30	M39014/01-1535V	CAP .01UF 10% 100V CER-R
C31	M39014/01-1317V	CAP,1000PF,10% 200VC
C32	M39014/01-1535V	CAP .01UF 10% 100V CER-R
C33	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C34	M39014/01-1535V	CAP .01UF 10% 100V CER-R
C35	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C36	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C38	CM06FD472J03	CAP 4700PF 5% 500V MICA
C39	C-0912	CAP .015UF 5% 200V MYLAR
C40	C-0912	CAP .015UF 5% 200V MYLAR
C41	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C43	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C44	CM06FD242J03	CAP 2400PF 5% 500V MICA
C45	CM06FD432J03	CAP 4300PF 5% 500V MICA
C46	C25-0001-301	CAP 1.0UF 20% 20V TANT
C51	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C52	6628-0660	CAP 5600PF 5% 300V MICA
C53	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C54	C26-0035-470	CAP 47UF 20% 35V TANT
C55	C-8212	CAP 470UF 50V ELEC
C56	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C57	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C58	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C60	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C61	C26-0025-100	CAP 10UF 20% 25V TANT
C62	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C63	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C64	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C82	CM04ED390J03	CAP 39PF 5% 500V MICA
C83	M39014/01-1535V	CAP .01UF 10% 100V CER-R

Table 3. PLL 2 Assembly A7 Parts List (10073-4200 Rev. AB) (Cont.)

Ref. Desig.	Part Number	Description
CR1	10073-7118	DIODE VARACTOR
CR2	10073-7118	DIODE VARACTOR
CR3	10073-7118	DIODE VARACTOR
CR4	10073-7118	DIODE VARACTOR
CR5	10073-7118	DIODE VARACTOR
CR6	10073-7118	DIODE VARACTOR
CR7	10073-7118	DIODE VARACTOR
CR8	10073-7118	DIODE VARACTOR
CR9	10073-7118	DIODE VARACTOR
CR10	10073-7118	DIODE VARACTOR
CR11	10073-7118	DIODE VARACTOR
CR12	10073-7118	DIODE VARACTOR
CR13	1N6263	DIODE .40W 60V HOT CARR
CR14	1N3064	DIODE 75mA 75V SW
CR15	1N3064	DIODE 75mA 75V SW
J1	J46-0032-010	HDR 10 PIN 0.100" SR
J2	J-0031	CONN SMB VERT PCB F
J3	J-0031	CONN SMB VERT PCB F
J4	J-0031	CONN SMB VERT PCB F
L1	MS75084-3	COIL 1.8UH 10% FXD RF
L2	MS75084-11	COIL 8.2UH 10% FXD RF
L3	82027-03	CHOKE WB 50MHZ
L4	82027-03	CHOKE WB 50MHZ
L5	MS75089-21	COIL 680UH 10% FXD RF
L6	MS75089-21	COIL 680UH 10% FXD RF
L7	82027-03	CHOKE WB 50MHZ
Q1	2N5109	XSTR RF PWR NPN TO-39
Q2	Q35-0003-000	XSTR N-CH JFET U310
Q3	Q35-0003-000	XSTR N-CH JFET U310
Q4	2N3563	XSTR SS/RF
Q5	Q35-0003-000	XSTR N-CH JFET U310
Q6	2N2907	XSTR SS/GP PNP TO-18
Q7	Q60-0003-000	XSTR JFET P-CH
Q8	2N2907	XSTR SS/GP PNP TO-18
Q9	2N2222	XSTR SS/GP NPN TO-18
Q10	2N2222	XSTR SS/GP NPN TO-18
Q11	2N5088	XSTR SS/GP
Q12	2N2222	XSTR SS/GP NPN TO-18
R1	R65-0003-470	RES 47 5% 1/4W CAR FILM
R2	R65-0003-471	RES 470 5% 1/4W CAR FILM
R3	R65-0003-242	RES 2.4K 5% 1/4W CAR FILM
R4	R65-0003-470	RES 47 5% 1/4W CAR FILM
R5	R65-0003-100	RES 10 5% 1/4W CAR FILM
R6	R65-0003-152	RES 1.5K 5% 1/4W CAR FILM

Table 3. PLL 2 Assembly A7 Parts List (10073-4200 Rev. AB) (Cont.)

Ref. Desig.	Part Number	Description
R7	R65-0003-201	RES 200 5% 1/4W CAR FILM
R8	R65-0003-270	RES 27 5% 1/4W CAR FILM
R9	R65-0003-513	RES 51K 5% 1/4W CAR FILM
R10	R65-0003-201	RES 200 5% 1/4W CAR FILM
R11	R65-0003-510	RES 51 5% 1/4W CAR FILM
R12	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R13	R65-0003-151	RES 150 5% 1/4W CAR FILM
R14	R65-0003-680	RES 68 5% 1/4W CAR FILM
R15	R65-0003-101	RES 100 5% 1/4W CAR FILM
R16	R65-0003-152	RES 1.5K 5% 1/4W CAR FILM
R17	R65-0003-100	RES 10 5% 1/4W CAR FILM
R18	R65-0003-151	RES 150 5% 1/4W CAR FILM
R19	R65-0003-470	RES 47 5% 1/4W CAR FILM
R20	R65-0003-513	RES 51K 5% 1/4W CAR FILM
R21	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R22	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R23	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R24	R65-0003-201	RES 200 5% 1/4W CAR FILM
R25	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R26	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R27	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R28	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R29	R65-0003-479	RES 4.7 5% 1/4W CAR FILM
R31	R65-0003-279	RES 2.7 5% 1/4W CAR FILM
R32, R33	RN55D6810F	RES 681 1% 1/8W MET FLM
R34	RN55D1501F	RES 1500 1% 1/8W MET FLM
R35	RN55D2001F	RES 2000 1% 1/8W MET FLM
R36, R37	RN55D6810F	RES 681 1% 1/8W MET FLM
R38	RN55D1212F	RES 12.1K 1% 1/8W MET FLM
R39	R65-0003-121	RES 120 5% 1/4W CAR FILM
R40	R65-0003-101	RES 100 5% 1/4W CAR FILM
R41	R65-0003-182	RES 1.8K 5% 1/4W CAR FILM
R42	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R43	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R44	R65-0003-223	RES 22K 5% 1/4W CAR FILM
R45	R65-0003-473	RES 47K 5% 1/4W CAR FILM
R46	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R47	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R48	R65-0003-103	RES 10K 5% 1/4W CAR FILM
T1, T2	10073-7014	TRANSFORMER, RF, FIXED
T3	10073-7002	TRANSFORMER, RF, FIXED
TP1	J-0071	TP PWB BRN TOP ACCS .080"
TP2	J-0066	TP PWB RED TOP ACCS .080"
TP3	J-0069	TP PWB ORN TOP ACCS .080"

Table 3. PLL 2 Assembly A7 Parts List (10073-4200 Rev. AB) (Cont.)

Ref. Desig.	Part Number	Description
TP4	J-0070	TP PWB YEL TOP ACCS .080"
TP5	J-0068	TP PWB GRN TOP ACCS .080"
U1	I65-0004-001	IC PRESCALER 10/11 12013
U2	I70-0002-001	IC MC145156 SYNTH PLA
U3	I01-0000-019	IC 4050B PLASTIC CMOS
U4	I05-0000-000	IC 74LS00 PLASTIC TTL
U5	I30-0018-000	IC OP AMP DUAL 1458
VR1	I12-0006-012	IC VR 78L12A +12V .10A 4%
VR2	I11-0001-001	IC VR 7805 +5V 1.5A 4%
VR3	1N5236A	DIODE 7.5V 10% .5W ZENER

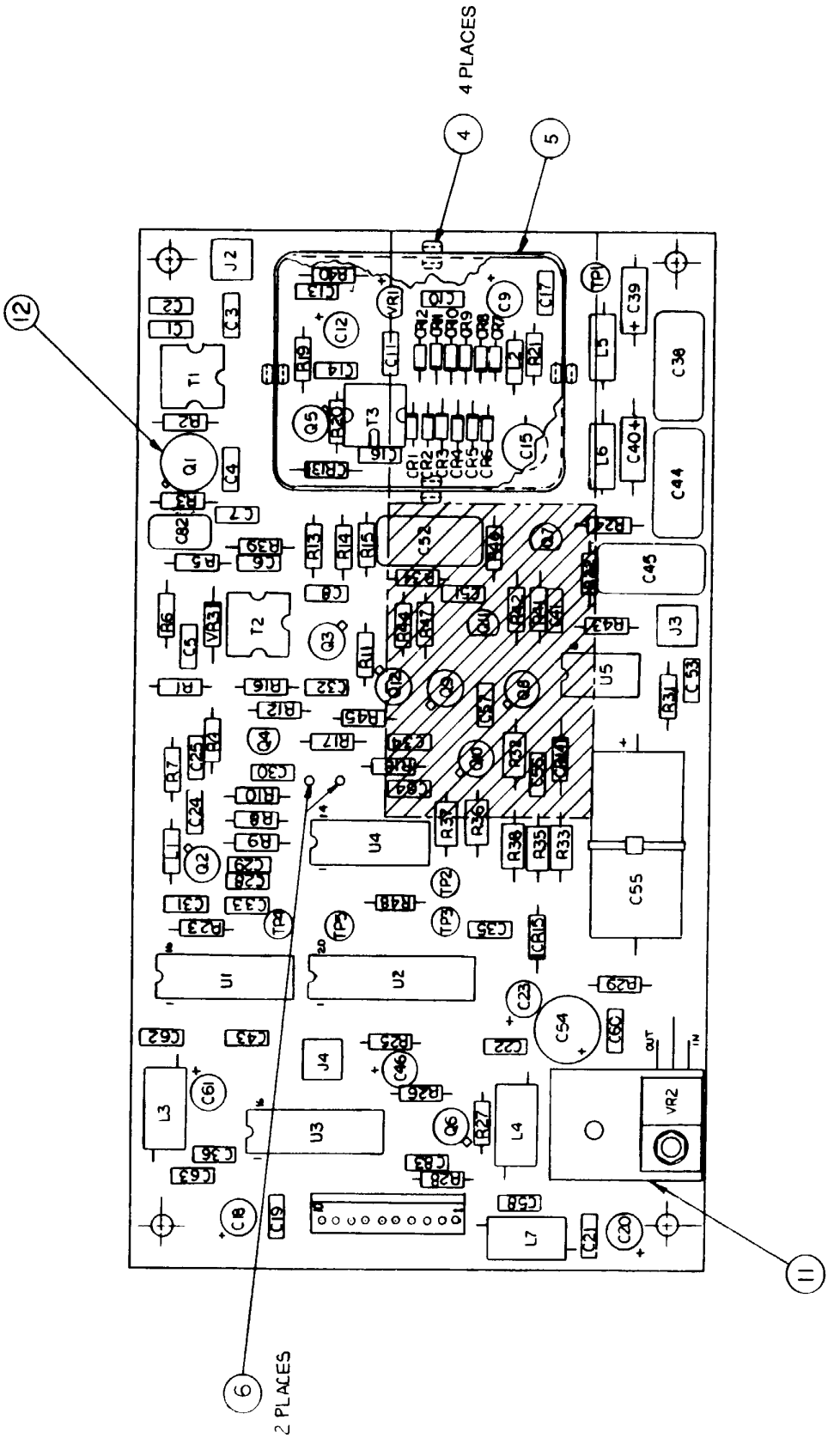


Figure 3. PLL 2 Assembly A7 Component Location Diagram (10073-4200 Rev. F)

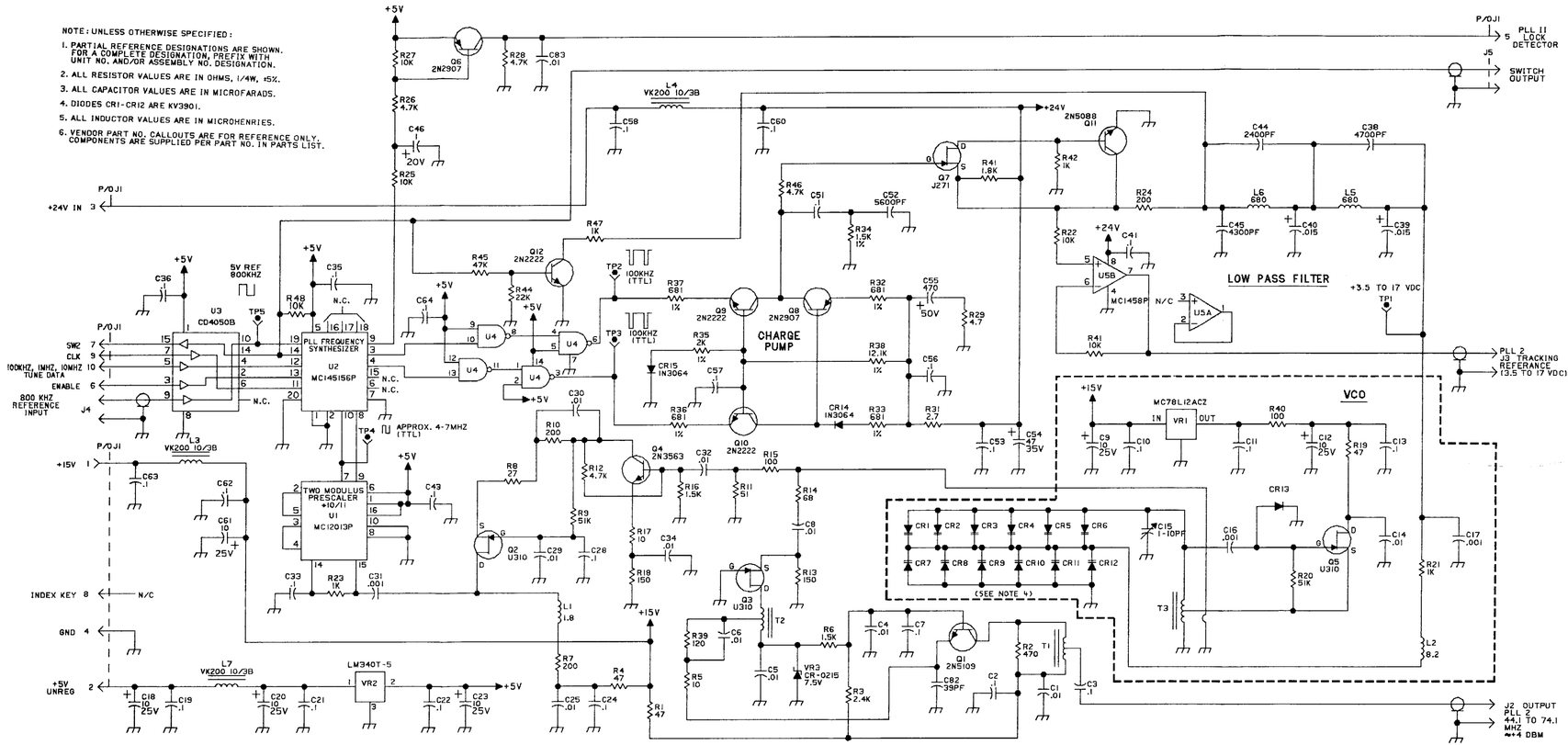
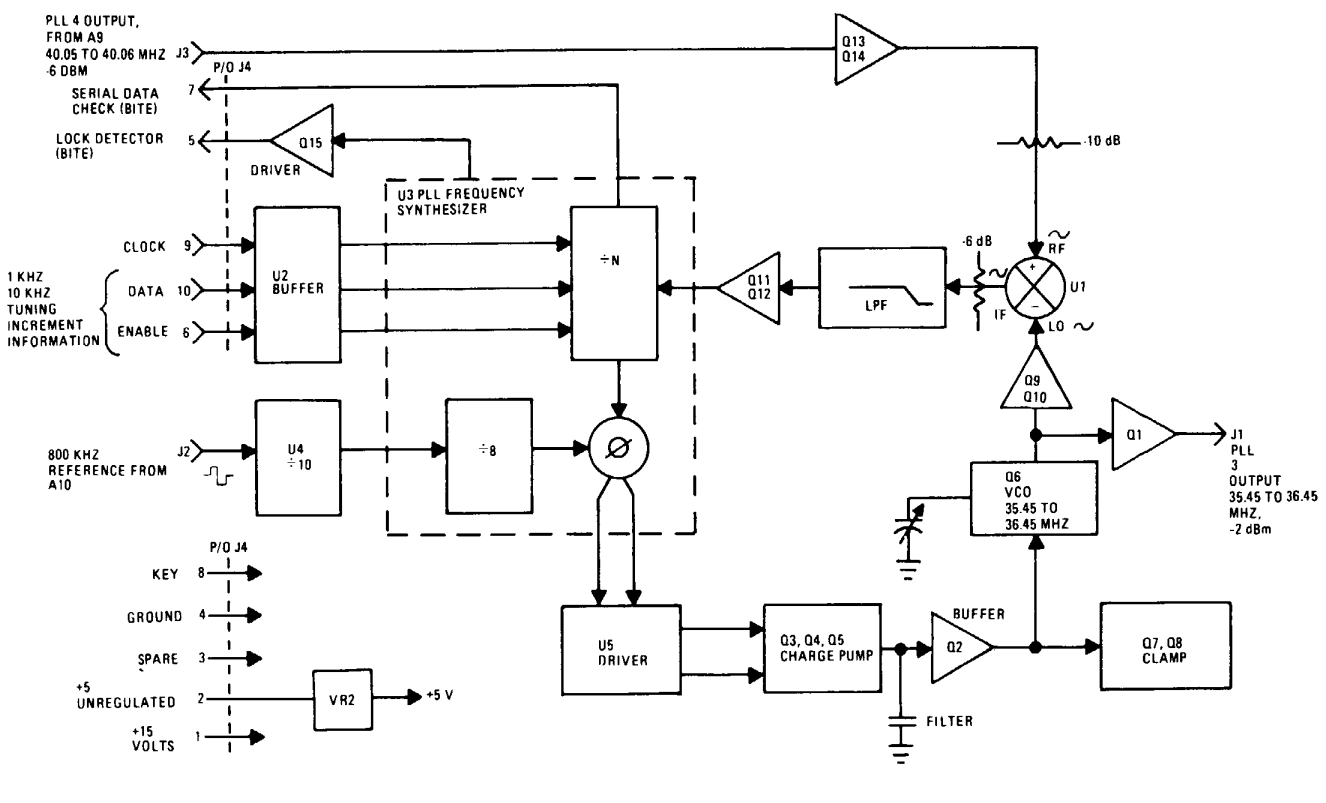


Figure 4. **PLL 2 Assembly A7 Schematic Diagram (10073-4201 Rev. J)**

A8
PLL 3 ASSEMBLY



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PLL 3 ASSEMBLY A8

1. GENERAL DESCRIPTION

PLL 3 Assembly A8 is a programmable translation loop which performs the following primary functions:

- Generation of 1 kHz and 10 kHz tuning increments of the LO 1 frequency.
- Combination of these increments with information containing the 1 Hz, 10 Hz, and 100 Hz increments of the LO 1 frequency.

Figure 1 shows the location of PLL 3 Assembly A8 in the RF-1310 chassis.

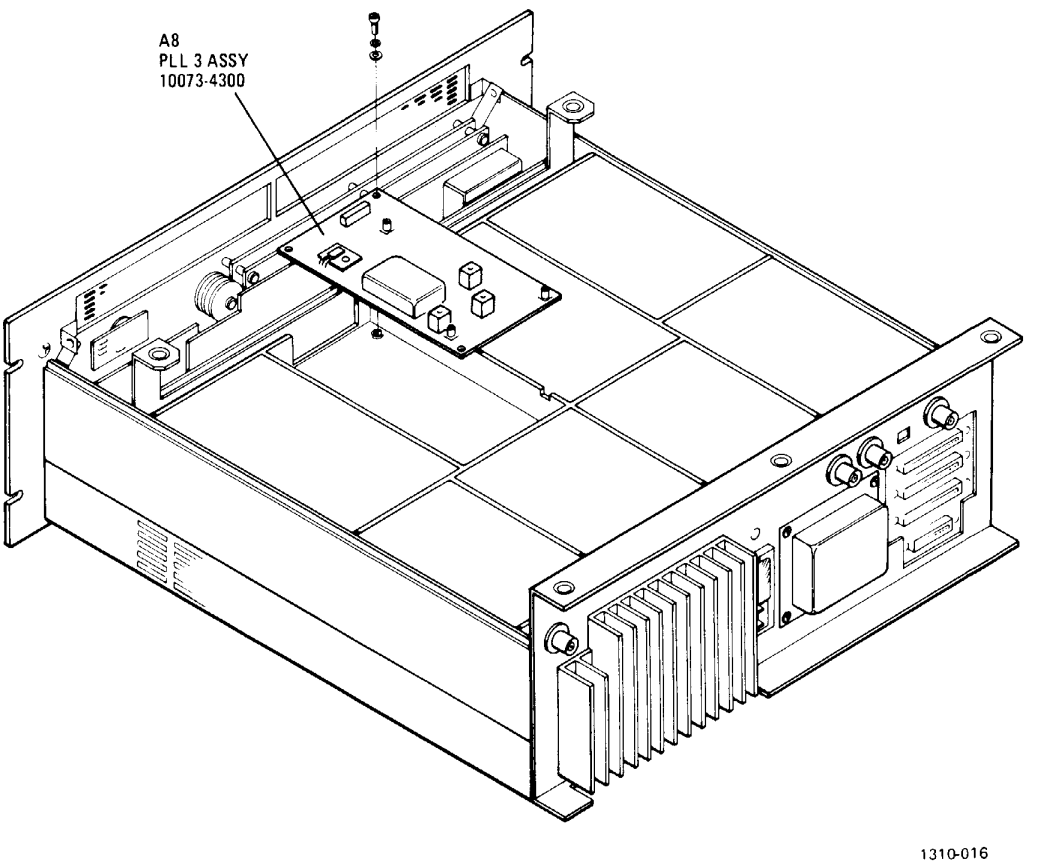


Figure 1. PLL 3 Assembly A8 Location

Frequency select input data for 1 kHz and 10 kHz tuning increments is applied to the A8 assembly in serial data format from the Control Board Assembly microprocessor. The 1 Hz, 10 Hz, and 100 Hz tuning increments information is supplied via PLL 4 Assembly A9 in the frequency range of 40.06 to 40.05 MHz. A8 assembly output to PLL 1 Assembly A6 contains 1 Hz, 10 Hz, 100 Hz, 1 kHz, and 10 kHz tuning information in the frequency range of 35.45 to 36.45 MHz.

2. INTERFACE CONNECTIONS

Table 1 details the input/output connections and other relevant data.

Table 1. PLL 3 Assembly Interface Connections

Connector	Function	Characteristics
J1	PLL 3 Output	35.45 to 36.45 MHz, approximately -2 dBm
J2	800 kHz Reference Input	TTL
J3	PLL 4 Input	40.05 to 40.06 MHz, approximately -6 dBm
J4-1	+ 15 Volts	Approximately 60 mA
J4-2	+ 5 Volts Unregulated	Approximately 30 mA
J4-3	Spare	
J4-4	Ground	
J4-5	Lock Detector Output	0 Vdc = PLL locked; + 5 Vdc = PLL unlocked
J4-6	Enable	+ going pulse = enabled
J4-7	Serial Data Check	P/O BITE test, + 5 Vdc = ok
J4-8	Key	
J4-9	Clock	750 kHz, TTL
J4-10	Data	Serial TTL

3. A8 FREQUENCY GENERATION SCHEME

A PLL intermediate frequency (IF) range of 3.61 MHz to 4.61 MHz is produced at the IF output of mixer U1. The instantaneous IF frequency is a consequence of the subtractive mixing of the following two signals:

- 40.050 to 40.060 MHz PLL 4 (RF port)
- 35.45 to 36.45 MHz VCO (LO port)

This IF signal will change in frequency to satisfy the requirement that the divide-by-N counter output will always try to equal the reference 10.000 kHz signal at the inputs to the phase comparator (P/O U3). When these two signals are not equal, the phase comparator produces an error command to drive the VCO frequency in the direction required to make them equal. If the divide-by-N output exceeds the reference 10.0000 kHz, the VCO will rise in frequency. If the divide-by-N output is less than the reference, the VCO will decrease in frequency.

The VCO output frequency is dependent upon the following two events:

- The division factor of the divide-by-N counter. N = (361 + XX), where XX represents the digits in the 10 kHz and 1 kHz positions of the displayed frequency.
- The PLL 4 output frequency. This is dependent upon the value of the digits in the 100 Hz, 10 Hz, and 1 Hz positions of the displayed frequency (section A9, PLL IV Assembly).

To illustrate this, assume that the exciter is tuned to a frequency of $X_8X_7X_6X_5X_4X_3X_2X_1$ Hz, where X_8 through X_2 represent the frequency display digits and X_1 is always zero. (See the block diagram on the section cover.)

Example 1: Assume that the $X_3X_2X_1$ value decreases.

a. As $X_3X_2X_1$ decreases the frequency of the PLL 4 output increases.

b. As a result, the frequency of the signal from U1 (the PLL 3 IF) to U3 also increases.

c. Since the N of the programmable frequency divider in U3 has not changed, the output frequency of that divider will increase, making it greater than the 10 kHz reference signal.

d. The phase detector in U3 will detect the difference between the programmable divider output and the reference signal, and the VCO frequency will increase.

e. This reduces the difference in frequency between the PLL 3 VCO output and the signal from PLL 4 to what it was before $X_3X_2X_1$ changed.

Example 2: Assume that the X_5X_4 value decreases.

a. As X_5X_4 decreases, the divide-by-N factor in U3 ($N = 361 + X_5X_4$) decreases.

b. The divide-by-N output frequency, equal to IF divide-by-N, increases. Since this now exceeds the 10.000 kHz reference at the phase comparator inputs, the phase comparator output forces the VCO (LO) frequency to increase.

c. In turn, the difference between the frequencies of the VCO output and the input from PLL 4 (the PLL 3 IF) decreases.

d. The output of the divide-by-N divider in U3 will decrease proportionally with the PLL 3 IF and continue to do so until it equals the 10 kHz reference.

The VCO of PLL 3 will decrease in frequency when $X_3X_2X_1$ or X_5X_4 are increased.

The A8 PLL 3 output frequency may be calculated from the following equation given the selected transmit frequency is X_8X_7, $X_6X_5X_4$, $X_3X_2X_1$ Hz:

$$f_{A8} = [40{,}000{,}000 + 10\,(6000\,X_3X_2X_1)]\,[10{,}000\,(361 + X_5X_4)],\ \text{Hz}$$

4. CIRCUIT DESCRIPTIONS

NOTE

A8 operation is similar to the general PLL and charge pump circuits described in section 4. A review of section 4 at this time would help in understanding A8 assembly operation.

4.1 PLL IF Generation

PLL 4 output at a -6 dBm level is applied to 10 dB gain stage Q13 and Q14. This output is attenuated by 50-ohm matching network R39, R40, and R44, and presents a -6 dBm signal ranging from 40.050 MHz to 40.060 MHz to the RF port of mixer U1.

U1 LO injection is supplied by the VCO via amplifier stage Q9 and Q10 at a + 7 dBm level. This signal ranges from 35.45 to 36.45 MHz.

U1 IF output is approximately -12 dBm (in the 3.61 to 4.61 MHz range). The 6 dB attenuator network, R41-R43, feeds a low pass filter which removes all mixer products except the desired IF range. Amplifier stage Q11 and Q12 provide a TTL level signal to a divide-by-N counter internal to U3 at pin 10.

4.2 Divide-By-N Counter

Since the A8 assembly requires a variable output frequency dependent upon the 1 kHz and 10 kHz tuning positions, a divide-by-N programmable counter has been incorporated into the VCO feedback loop. The front panel selection of a tune frequency from 00 kHz to 99 kHz causes Control Assembly A14 to generate a serial data code containing information pertaining to the values chosen. This code is applied synchronously with the 750 kHz system clock to U3, whenever the U3 enable line is gated open by A14.

N = (361 + XX) where XX represents the digits in the 10 kHz and 1 kHz positions of the displayed frequency. The divide-by-N counter output will always attempt to equal the 10.000 kHz reference frequency at the phase comparator inputs.

4.3 Phase Comparator and Charge Pump Operation

A 10.000 kHz reference signal is applied to one port of the phase comparator. This signal has been divided down from the 800 kHz TTL reference supplied by the A10 assembly. Divide-by-10 circuit U4 feeds 80 kHz to the divide-by-8 circuit internal to U3.

The second input to the phase comparator is the divide-by-N counter output. When these two signals are equal in frequency and phase, the outputs at buffer stage U5 (TP2 and TP3) are essentially at a + 5 Vdc level. This level holds Q4, Q5, and consequently Q3 off. The voltage across C8 is constant. Q2 is biased to produce a constant voltage across R12, and the dc level (VCO control) at TP1 is constant. This holds the VCO at a constant frequency.

Assuming that the divide-by-N output exceeds the reference 10.000 kHz, the phase comparator output at TP3 pulses low (the pulse width being a function of the amount of difference between the two signals). Q5 turns on, and its falling collector voltage turns Q3 on, allowing Q3 to pump charge into C8. C8 voltage increases, causing Q2 to conduct more current and develop a large voltage across R12. The VCO control voltage increases and forces the VCO to tune higher in frequency. This will lower the IF frequency, and divide-by-N counter output will decrease. As the divide-by-N counter output approaches the reference, the pulse widths will get narrower until a 5 Vdc level will again occur at TP3. At this point, Q5 turns off, Q3 stops pumping charge into C8, the VCO control voltage stops at a new higher level, and the VCO has been tuned to a higher frequency.

Assuming that the divide-by-N counter output is less than the reference, the phase comparator output at TP2 will pulse low. Q4 turns on and draws charge out of C8. Q2 conducts less current, and the VCO voltage drops, driving the VCO frequency down. The IF feedback signal frequency will increase, and consequently the divide-by-N counter output will increase. As this output approaches the reference frequency, TP2 pulses will get narrower until Q4 is turned off. The voltage across C8 halts at a lower value (as does the VCO control voltage level). This holds the VCO at a new lower frequency.

4.4 VCO Operation and Control

A charge pump circuit consisting of Q3, Q4, Q5, and associated components in conjunction with filter network C8, C9, and R14 convert the two phase comparator pulse outputs into an analog dc control voltage. Buffer

amplifier Q2 applies a VCO control voltage to the varactor diode string in the VCO. Changing diode capacitance fine tunes JFET Hartley oscillator stage Q6. The total VCO frequency range is 35.45 to 36.45 MHz. A control voltage range of approximately 6.5 to 7.5 Vdc will tune the oscillator from 35.45 MHz to 36.45 MHz.

Clamp circuit Q7, Q8, and CR2-CR5 monitors the VCO control voltage level, and will prevent the control voltage from exceeding the approximate range of 5.5 to 8.5 Vdc. This "window" is necessary to prevent the VCO from running to the wrong side of the frequency conversion during the mixing process. This could cause the exciter to lock falsely at the wrong frequency, or not lock at all. For example, assume that the control voltage could rise high enough to force the VCO to 41 MHz. Combination of the 40.05 to 40.06 MHz signal at mixer U1 would produce a loop IF in the 1 MHz region instead of the required 3.61 to 4.61 MHz range. The clamp circuit would prevent this. CR4, CR5, and Q8 would conduct and clamp the level at 8.5 volts and prevent the VCO from "running away".

The VCO output is fed through amplifier stage Q9 and Q10 to function as a + 7 dBm LO injection for U1, and to Q1, where a -2 dBm signal is passed through J1 to PLL 1 Assembly A6.

4.5 BITE Test Circuits

The A10 assembly contains two circuits for self-test evaluation. The circuits are:

- Lock detector Q15 whose output is 0 Vdc whenever the PLL is tracking properly. This line is constantly monitored by the A14 assembly. A front panel fault light will appear if the loop ever unlocks.

- Serial data check that verifies that the tune data from the A14 assembly has been received and properly translated into the correct divide-by-N factor. A serial data word is sent on the data line (J4 pin 10) and the U3 serial data check line is read back to the A14 assembly (J4 pin 7). If the word has been received and properly decoded, this line will pulse to + 5 Vdc. The serial data check occurs automatically, but only when the exciter BITE self test is actuated.

5. MAINTENANCE

The following adjustments should not be made as part of a routine maintenance procedure, but only when a failure indicates a definite need. Perform all tests with all connections in normal contact, unless otherwise specified.

5.1 VCO Alignment

Perform the following procedure to align the VCO:

a. Connect equipment as shown in figure 2.

b. Set exciter frequency to 02.05050 MHz.

c. Monitor U1, pin 8, with an oscilloscope and adjust T3 for a maximum signal (should be approximately 1.2 Vpp).

d. Monitor U1 RF input at R44 with oscilloscope and adjust T4 for a maximum signal (should be approximately 1 Vpp).

e. Monitor J1 with spectrum analyzer at approximately 35 MHz. Adjust T2 for a maximum output (approximately -2 dBm).

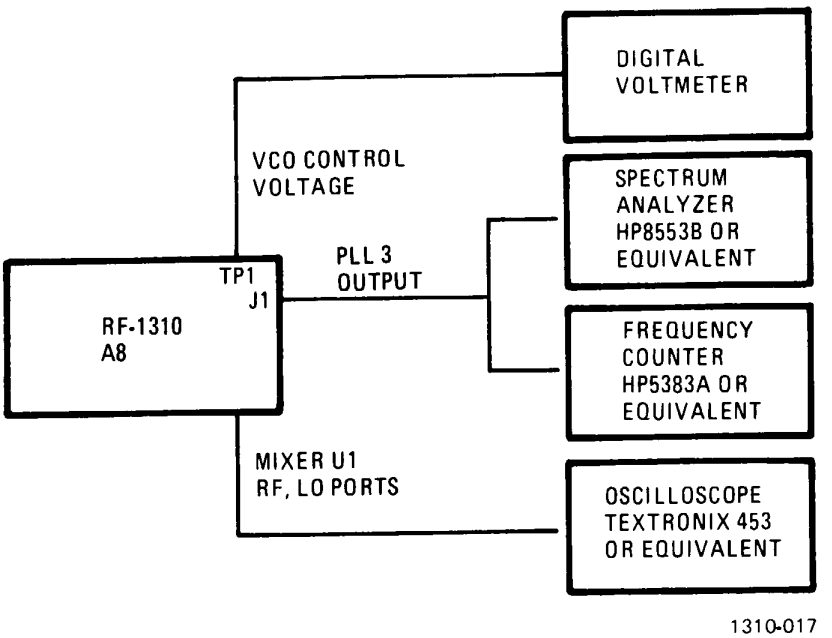


Figure 2. A8 VCO Alignment

f. Monitor TP1 with digital voltmeter (DVM). Adjust C11 for 7.0 Vdc. PLL 3 output and tune frequencies should agree with values listed in table 2.

Table 2. PLL 3 Output Range

Exciter Tune Frequency, MHz	PLL 3 Output Frequency, MHz	Approximate TP1 Voltage, Vdc
02.00000	36.450000	7.9
02.05050	35.944950	7.0
02.09999	35.450100	6.5

g. Fully reconnect the A8 assembly to the RF-1310 and initiate BITE self test. No failures should occur indicating an A8 assembly fault.

6. PARTS LIST, COMPONENT LOCATION, AND SCHEMATIC DIAGRAM

All components of the PLL 3 assembly are listed in table 3. Component locations are shown in figure 3. Figure 4 is the schematic diagram for PLL 3 Assembly A8.

Table 3. PLL 3 Assembly A8 Parts List (10073-4300 Rev. W)

Ref. Desig.	Part Number	Description
3	10073-7116	CAN RECT DEEP DRAWN
4	10073-7214	CLIP MOUNTING,MODIFIED
5	10073-7106	HEATSINK PLATE
6	918-0237	SHIELD, COIL
13	E70-0002-002	PAD MNT XSTR TO-5
C1	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C2	M39014/01-1535V	CAP .01UF 10% 100V CER-R
C3	M39014/01-1535V	CAP .01UF 10% 100V CER-R
C4	CM04ED560J03	CAP 56PF 5% 500V MICA
C5	M39014/01-1535V	CAP .01UF 10% 100V CER-R
C6	C26-0025-100	CAP 10UF 20% 25V TANT
C7	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C8	M39014/02-1318V	CAP .33UF 10% 50V CER-R
C9	M39014/01-1543V	CAP .027UF 10% 50V CER-R
C10	C26-0025-339	CAP 3.3UF 20% 25V TANT
C11	C84-0003-008	CAP VAR 3-15PF CER
C12	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C13	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C14	M39014/01-1317V	CAP,1000PF,10% 200VC
C15	M39014/01-1535V	CAP .01UF 10% 100V CER-R
C16	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C17	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C18	M39014/01-1535V	CAP .01UF 10% 100V CER-R
C19	M39014/01-1317V	CAP,1000PF,10% 200VC
C20	C26-0025-100	CAP 10UF 20% 25V TANT
C21	M39014/01-1535V	CAP .01UF 10% 100V CER-R
C22	C26-0025-100	CAP 10UF 20% 25V TANT
C23	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C24	CM04ED470J03	CAP 47PF 5% 500V MICA
C25	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C26	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C27	M39014/01-1535V	CAP .01UF 10% 100V CER-R
C28	M39014/01-1535V	CAP .01UF 10% 100V CER-R
C29	C26-0016-151	CAP 150UF 20% 16V TANT
C30	M39014/01-1535V	CAP .01UF 10% 100V CER-R
C31	M39014/01-1535V	CAP .01UF 10% 100V CER-R
C32	C26-0025-339	CAP 3.3UF 20% 25V TANT
C33	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C34	CM04ED470J03	CAP 47PF 5% 500V MICA
C35	M39014/01-1535V	CAP .01UF 10% 100V CER-R
C36	C26-0025-100	CAP 10UF 20% 25V TANT

Table 3. PLL 3 Assembly A8 Parts List (10073-4300 Rev. W) (Cont.)

Ref. Desig.	Part Number	Description
C37	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C38	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C39	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C40	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C41	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C42	CM04FD151J03	CAP 150PF 5% 500V MICA
C43	CM04FD151J03	CAP 150PF 5% 500V MICA
C44	CM04FC271J03	CAP 270PF 5% 300V MICA
C45	CM04FC301J03	CAP 300PF 5% 300V MICA
C46	CM04FC271J03	CAP 270PF 5% 300V MICA
C47	CM04FC271J03	CAP 270PF 5% 300V MICA
C48	CM04FD111J03	CAP 110PF 5% 500V MICA
C49	CM04CD120J03	CAP 12PF 5% 500V MICA
C50	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C51	CM04ED330J03	CAP 33PF 5% 500V MICA
C52	CM04FD151J03	CAP 150PF 5% 500V MICA
C53	CM04CD120J03	CAP 12PF 5% 500V MICA
C54	M39014/01-1535V	CAP .01UF 10% 100V CER-R
C55	M39014/01-1535V	CAP .01UF 10% 100V CER-R
C56	CM04ED470J03	CAP 47PF 5% 500V MICA
C57	M39014/01-1535V	CAP .01UF 10% 100V CER-R
C58	CM04ED390J03	CAP 39PF 5% 500V MICA
C59	M39014/01-1535V	CAP .01UF 10% 100V CER-R
C60	M39014/01-1535V	CAP .01UF 10% 100V CER-R
C61	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C62	C26-0025-470	CAP 47UF 20% 25V TANT
C63	C26-0025-470	CAP 47UF 20% 25V TANT
C64	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C65	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C66	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C67	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C68	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C69	C25-0001-301	CAP 1.0UF 20% 20V TANT
C70	M39014/01-1535V	CAP .01UF 10% 100V CER-R
C71	M39014/01-1535V	CAP .01UF 10% 100V CER-R
C72	M39014/01-1535V	CAP .01UF 10% 100V CER-R
CR1	1N6263	DIODE .40W 60V HOT CARR
CR2 – CR6	1N3064	DIODE 75mA 75V SW
CR7 – CR10	D25-0002-001	DIODE TUNING MV309

Table 3. PLL 3 Assembly A8 Parts List (10073-4300 Rev. W) (Cont.)

Ref. Desig.	Part Number	Description
CR11 – CR16	D25-0002-001	DIODE TUNING MV309
J1 – J3	J-0031	CONN SMB VERT PCB F
J4	J46-0032-010	HDR 10 PIN 0.100" SR
L1	MS75084-13	COIL 12UH 10% FXD RF
L2	MS75083-6	COIL .27UH 10% FXD RF
L3	MS75084-6	COIL 3.3UH 10% FXD RF
L4	MS75083-6	COIL .27UH 10% FXD RF
L5	82027-03	CHOKE WB 50MHZ
L6	MS18130-9	COIL 1.2UH 10% FXD RF
L7	MS18130-9	COIL 1.2UH 10% FXD RF
L8	MS18130-8	COIL 1.0UH 10% FXD RF
L9	82027-03	CHOKE WB 50MHZ
Q1	Q35-0003-000	XSTR N-CH JFET U310
Q2	Q05-0001-000	XSTR JFET N-CH
Q3	2N2907	XSTR SS/GP PNP TO-18
Q4	2N2222	XSTR SS/GP NPN TO-18
Q5	2N2222	XSTR SS/GP NPN TO-18
Q6	Q35-0003-000	XSTR N-CH JFET U310
Q7	2N2222	XSTR SS/GP NPN TO-18
Q8	2N2907	XSTR SS/GP PNP TO-18
Q9	Q35-0003-000	XSTR N-CH JFET U310
Q10	2N5109	XSTR RF PWR NPN TO-39
Q11	Q-0153	XSTR SS/RF PN4258
Q12, Q13	2N2369	XSTR SS/RF NPN
Q14	Q35-0003-000	XSTR N-CH JFET U310
Q15	2N2907	XSTR SS/GP PNP TO-18
R1	R65-0003-101	RES 100 5% 1/4W CAR FILM
R2	R65-0003-470	RES 47 5% 1/4W CAR FILM
R3	R65-0003-513	RES 51K 5% 1/4W CAR FILM
R4	R65-0003-101	RES 100 5% 1/4W CAR FILM
R5	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R7	R65-0003-201	RES 200 5% 1/4W CAR FILM
R8	R65-0003-202	RES 2.0K 5% 1/4W CAR FILM
R9	RN55D1501F	RES 1500 1% 1/8W MET FLM
R10	RN55D1501F	RES 1500 1% 1/8W MET FLM
R11	RN55D1002F	RES 10.0K 1% 1/8W MET FLM
R12	R65-0003-202	RES 2.0K 5% 1/4W CAR FILM
R13	RN55D3321F	RES 3320 1% 1/8W MET FLM
R14	RN55D1621F	RES 1620 1% 1/8W MET FLM
R15	RN55D2211F	RES 2210 1% 1/8W MET FLM

Table 3. PLL 3 Assembly A8 Parts List (10073-4300 Rev. W) (Cont.)

Ref. Desig.	Part Number	Description
R16	RN55D2211F	RES 2210 1% 1/8W MET FLM
R17	R65-0003-330	RES 33 5% 1/4W CAR FILM
R18	R65-0003-121	RES 120 5% 1/4W CAR FILM
R19	R65-0003-360	RES 36 5% 1/4W CAR FILM
R20	R65-0003-201	RES 200 5% 1/4W CAR FILM
R21	R65-0003-392	RES 3.9K 5% 1/4W CAR FILM
R22	R65-0003-392	RES 3.9K 5% 1/4W CAR FILM
R23	R65-0003-470	RES 47 5% 1/4W CAR FILM
R24	R65-0003-242	RES 2.4K 5% 1/4W CAR FILM
R25	R65-0003-681	RES 680 5% 1/4W CAR FILM
R26	R65-0003-182	RES 1.8K 5% 1/4W CAR FILM
R27	R65-0003-471	RES 470 5% 1/4W CAR FILM
R28	R65-0003-330	RES 33 5% 1/4W CAR FILM
R29	R65-0003-101	RES 100 5% 1/4W CAR FILM
R30	R65-0003-271	RES 270 5% 1/4W CAR FILM
R31	R65-0003-820	RES 82 5% 1/4W CAR FILM
R32	R65-0003-391	RES 390 5% 1/4W CAR FILM
R33	R65-0003-561	RES 560 5% 1/4W CAR FILM
R34	R65-0003-330	RES 33 5% 1/4W CAR FILM
R35	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R36	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R37	R65-0003-471	RES 470 5% 1/4W CAR FILM
R39	R65-0003-750	RES 75 5% 1/4W CAR FILM
R40	R65-0003-101	RES 100 5% 1/4W CAR FILM
R41, R42	R65-0003-101	RES 100 5% 1/4W CAR FILM
R43	R65-0003-750	RES 75 5% 1/4W CAR FILM
R44	R65-0003-101	RES 100 5% 1/4W CAR FILM
R45	R65-0003-101	RES 100 5% 1/4W CAR FILM
R46	R65-0003-111	RES 110 5% 1/4W CAR FILM
R47	R65-0003-471	RES 470 5% 1/4W CAR FILM
R48	R65-0003-470	RES 47 5% 1/4W CAR FILM
R49	R65-0003-242	RES 2.4K 5% 1/4W CAR FILM
R50	R65-0003-182	RES 1.8K 5% 1/4W CAR FILM
R51	R65-0003-681	RES 680 5% 1/4W CAR FILM
R52	R65-0003-201	RES 200 5% 1/4W CAR FILM
R53 – R55	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R56	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R58	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R59	R65-0003-101	RES 100 5% 1/4W CAR FILM
R60	R65-0003-560	RES 56 5% 1/4W CAR FILM
T1	10073-7004	TRANSFORMER, RF, FIXED
T2 – T4	10073-7011	TRANSFORMER, RF, VARIABLE

Table 3. PLL 3 Assembly A8 Parts List (10073-4300 Rev. W) (Cont.)

Ref. Desig.	Part Number	Description
TP1	J-0071	TP PWB BRN TOP ACCS .080"
TP2	J-0066	TP PWB RED TOP ACCS .080"
TP3	J-0069	TP PWB ORN TOP ACCS .080"
TP4	J-0070	TP PWB YEL TOP ACCS .080"
TP5	J-0068	TP PWB GRN TOP ACCS .080"
TP6	J-0072	TP PWB BLU TOP ACCS .080"
U1	I51-0003-003	MIXER DB SRA-1
U2	I01-0000-019	IC 4050B PLASTIC CMOS
U3	I70-0002-001	IC MC145156 SYNTH PLA
U4	I05-0000-090	IC 74LS90 PLASTIC TTL
U5	I05-0000-000	IC 74LS00 PLASTIC TTL
VR1	I12-0006-012	IC VR 78L12A +12V .10A 4%
VR2	I11-0001-001	IC VR 7805 +5V 1.5A 4%
VR3, VR4	1N5236A	DIODE 7.5V 10% .5W ZENER

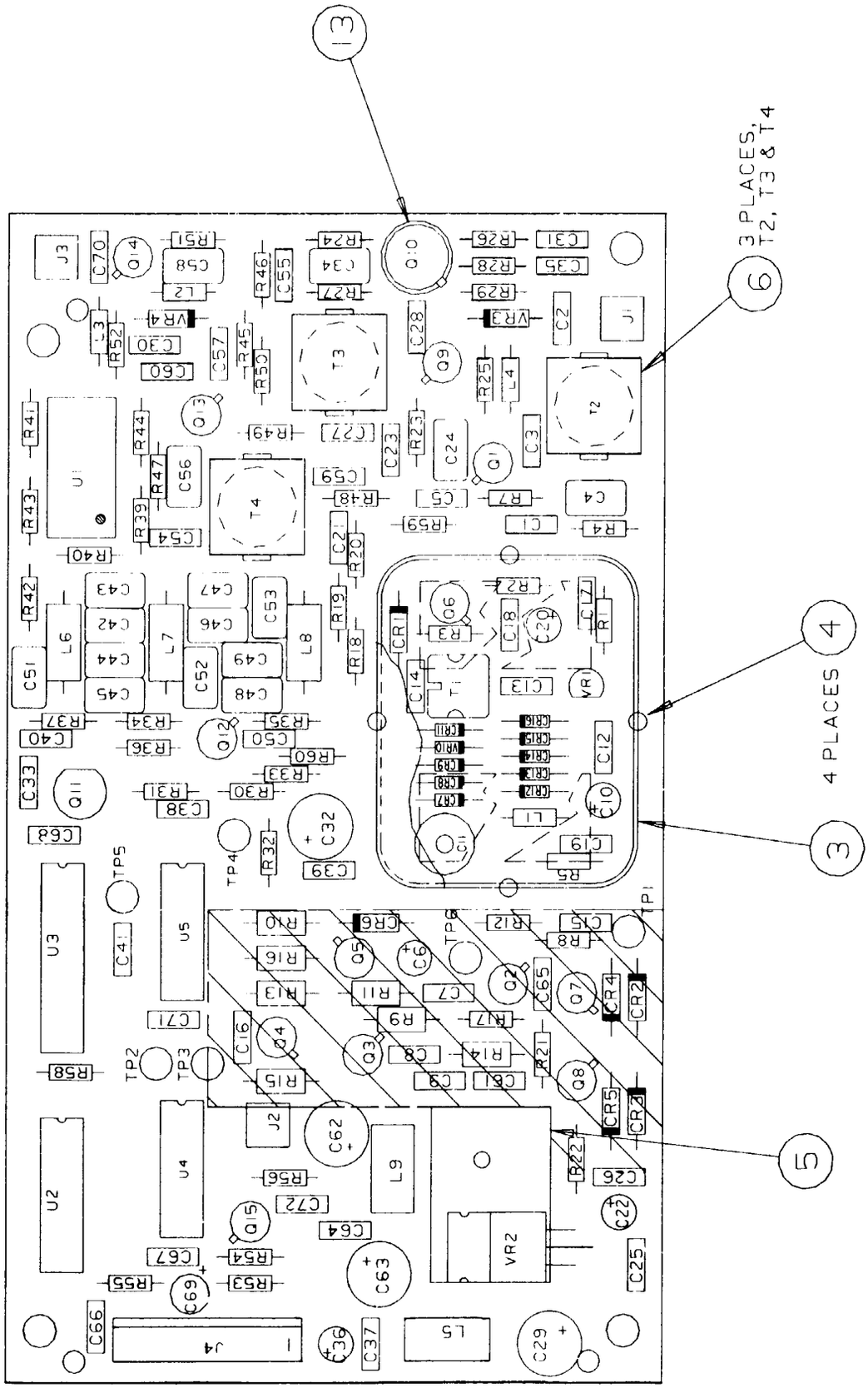


Figure 3. PLL 3 Assembly A8 Component Location Diagram (10073-4300, Rev. F)

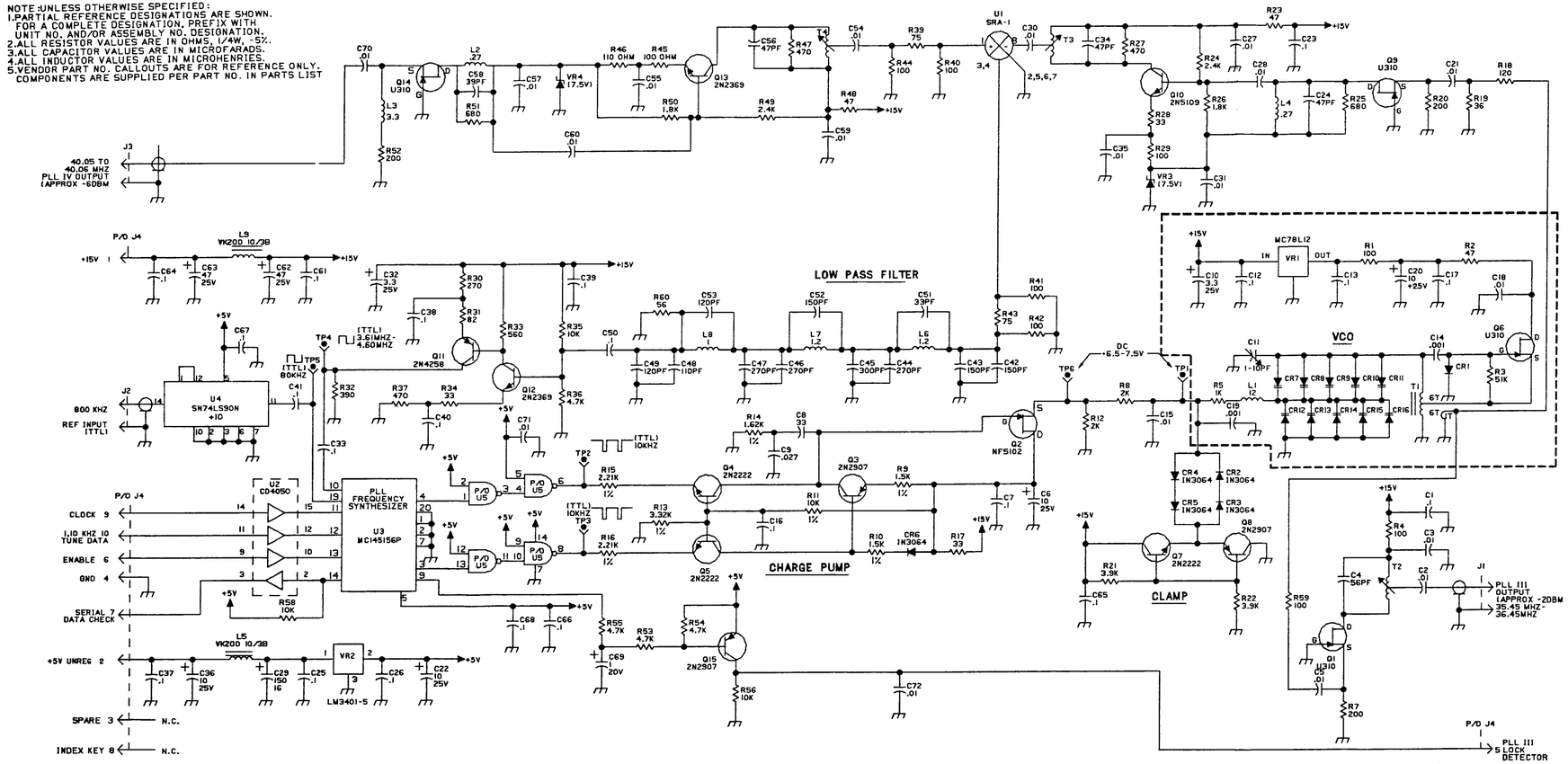
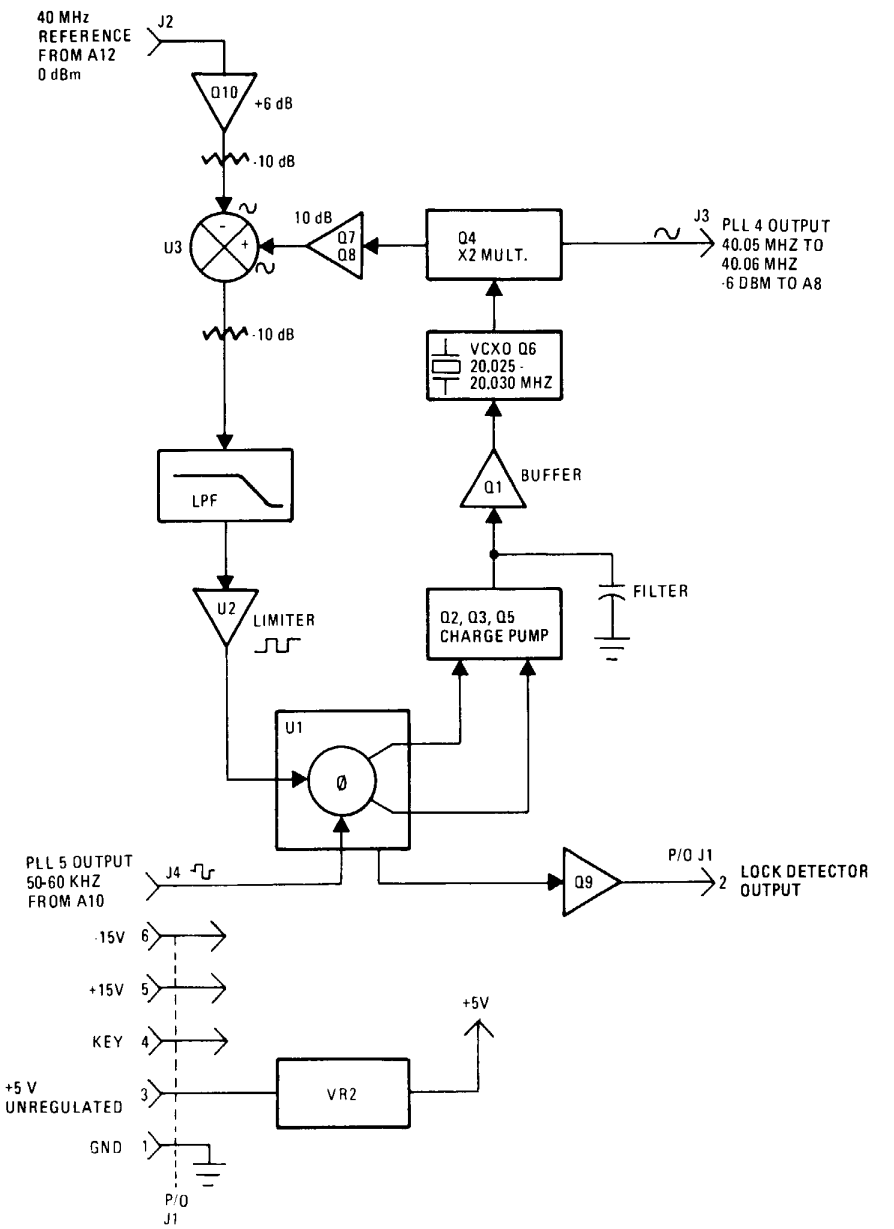


Figure 4. PLL 3 Assembly A8 Schematic Diagram (10073-4301 Rev. F)

A9

PLL 4 ASSEMBLY



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PLL 4 ASSEMBLY A9

1. GENERAL DESCRIPTION

PLL 4 Assembly A9 is a translation type phase lock loop which converts the low frequency variable PLL 5 output at 50 to 60 kHz (in 10 Hz steps) into a higher frequency signal at 40.05 to 40.06 MHz. During translation, the 10 Hz step size is preserved. This conversion process is an intermediate step leading toward the 1 Hz, 10 Hz, and 100 Hz tuning increments in the RF-1310 LO 1 frequency range of 40.465 to 70.455 MHz. The 1 Hz, 10 Hz, and 100 Hz tuning increments are defined by the digits in corresponding positions of the transmit frequency.

Figure 1 shows the location of PLL 4 Assembly A9 in the RF-1310 chassis.

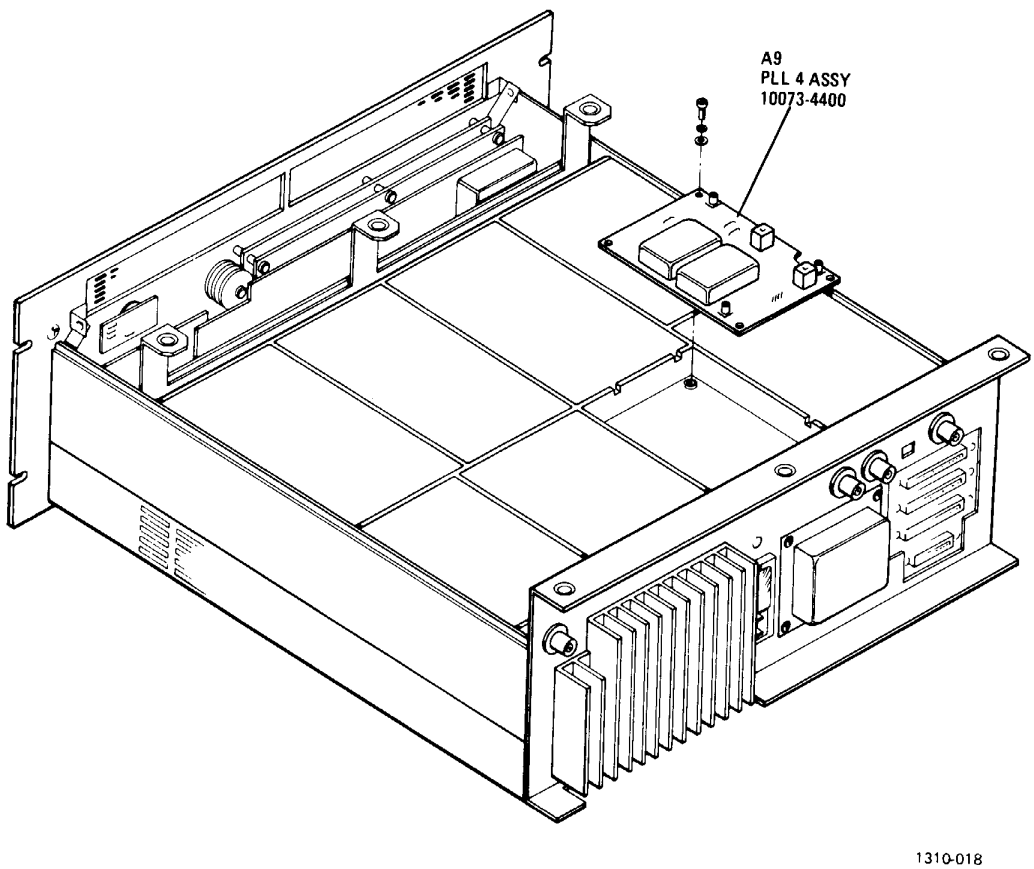


Figure 1. PLL 4 Assembly A9 Location

2. INTERFACE CONNECTIONS

Table 1 details the input/output connections and other relevant data.

Table 1. PLL 4 Assembly Interface Connections

Connector	Function	Characteristics
J1-1	Ground	
J1-2	Lock Detector Output	0 V = Locked, + 5 V = unlocked, P.O BITE Test
J1-3	+ 5 Volts Unregulated	Approximately 50 mA
J1-4	Key	
J1-5	+ 15 V	Approximately 60 mA
J1-6	-15 V	Approximately 6 mA
J2	40 MHz Reference	40.000000 MHz, 0 dBm
J3	PLL 4 Output	40.050 to 40.060 MHz, -6 dBm
J4	PLL 5 Input	50.0 to 60.0 kHz, TTL

3. CIRCUIT DESCRIPTION

3.1 PLL IF Generation

A PLL intermediate frequency (IF) signal in the range of 50 kHz to 60 kHz is produced at the output of mixer U3. This IF signal is a result of the mixing of the 40.000000 MHz reference from the A12 assembly with a VCXO derived signal in the range of 40.050 to 40.060 MHz.

This IF signal is then compared against the PLL 5 output (a signal also in the range of 50 to 60 kHz) at phase comparator U1. If there is any difference in phase or frequency between the IF and the PLL 5 output signals, U1 produces an error output which forces the VCXO to shift in frequency. The new IF produced will be equal to the A10 output frequency. The net result is that the VCXO derived frequency always equals the reference plus the A10 output frequency (even as the A10 output changes frequencies). As the A10 output changes from 50 to 60 kHz in 10 Hz increments, the A9 output will change from 40.050 MHz to 40.060 MHz (also in 10 Hz increments).

The actual value of the PLL 4 output frequency can be determined by the following formula. f = [40.000,000 + 10 (6000-XXX)] Hz, where XXX is the value of the three least significant digits of the transmit frequency. The 1 Hz digit is not displayed and is always zero.

The 40.000000 MHz reference signal from the A12 assembly enters A9 at J2 (0 dBm) and is applied to 6 dB gain amplifier stage Q10. The signal is attenuated to -4 dBm by 50-ohm matching network R28, R29, and R30. This signal is applied to the RF port of mixer U3 at pin 1.

U3 LO injection at pin 8 is a 40.05 MHz to 40.06 MHz signal derived from the VCXO, and amplified to a + 7 dBm level by LO amplifier stage Q7 and Q8.

U3 mixing action produces a 30 mVrms IF signal at pins 3 and 4 (in 50 to 60 kHz range). The -6 dB matching network R31, R32, and R34 couples this signal to a low pass filter network which removes all undesired mixer products except the IF signal. High gain amplifier U2 boosts this signal to a TTL level prior to application to one side of phase comparator U1.

3.2 Phase Comparator and Charge Pump Circuits

Phase comparator U1 compares the IF signal with PLL 5 output signals in the range of 50 to 60 kHz. When these two signals are equal in frequency and phase, U1 outputs at TP2 and TP3 are essentially 5 Vdc. All transistors in the charge pump circuit (Q2, Q3, and Q5) are turned off. The voltage across C19 is constant and Q1 is biased on producing a constant VCXO control voltage across R4. This holds the VCXO frequency constant.

Assume that PLL 5 output increases in frequency. The PLL 5 output frequency at U1, pin 1, will be higher than the IF signal frequency at pin 3. The U1 output at TP3 pulses low, turning Q5 on. Consequently, Q2 turns on as the Q5 collector voltage drops. Q2 pumps charge into C19, causing Q1 to conduct more current with a proportional increase in voltage across R4. This rising control voltage forces the VCXO to increase in frequency, producing a corresponding increase in the IF frequency. As this new IF signal approaches the PLL 5 output frequency, the phase comparator output pulse width becomes narrower, until it is essentially a constant 5 Vdc. Q5 and Q2 turn off, the voltage rise in C19 stops at a new higher level, and the VCXO frequency stabilizes. The two phase comparator inputs are again equal.

Assume that the PLL 5 output decreases in frequency. This time the U1 output at TP2 will pulse low (the pulse width being a function of the difference in frequency at the inputs.) Q3 turns on and C19 now has a low impedance discharge path to ground. As the C19 voltage drops, Q1 conduction decreases, and the voltage across R4 decreases. This forces the VCXO to decrease in frequency which causes a corresponding decrease in the IF frequency. As the two U1 inputs become equal, the negative pulses at TP2 become narrower, until an essentially 5 Vdc level exists. Q3 turns off, holding the C19 voltage and consequently the R4 voltage at a new lower level. The VCXO stops decreasing and also rests at a new lower frequency.

3.3 VCO Operation and Control

A charge pump circuit consisting of Q2, Q3, Q5, and associated components in conjunction with filter network C19-R6 convert the two phase comparator pulse outputs into an analog dc control voltage. Buffer amplifier Q1 applies this control voltage to varactor diodes CR1 and CR2 in the VCXO circuit. As the capacitance of these diodes changes due to control voltage fluctuations, JFET Hartley oscillator stage Q6 shifts in frequency. This oscillator stage is crystal controlled by Y1 and operates at 20.025 to 20.030 MHz, which is one-half the desired output frequency range. Therefore, X2 multiplier stage Q4 is used to produce the desired VCXO range of 40.050 to 40.060 MHz. A control voltage of approximately 5 Vdc will tune the VCXO to produce 40.050 MHz at J3, while a control voltage of 10 Vdc will tune it to 40.060 MHz.

VCXO output is applied through an attenuator network to J3 at a level of -6 dBm and on to PLL 3 Assembly A8. It is also applied to 10 dB amplifier stage Q7 and Q8 which functions as a local oscillator (LO) amplifier for U3. This stage provides a + 7 dBm LO injection to U3, pin 8, to complete the feedback loop.

4. BITE TEST CIRCUITS

Lock detector Q9 monitors the status of phase comparator U1 outputs at TP2 and TP3. If either output pulses low and remains low for a period exceeding the time constants of C57 and R38, the appropriate diode will conduct. Q9 will turn on and the voltage across R41 will increase from 0 to + 5 Vdc, indicating an out of lock condition. This immediately flags BITE monitoring circuits on Control Assembly A14. A front panel fault light indicator will turn on.

5. MAINTENANCE

The following adjustments should not be performed as a routine maintenance procedure, but only when a failure indicates a definite need. Perform tests with all connections in normal contact, unless otherwise specified.

5.1 X2 Multiplier, LO Amplifier, and RF Amplifier Alignment

Perform the following procedure to align the X2 multiplier, LO, and RF amplifiers:

a. Connect equipment as shown in figure 2.

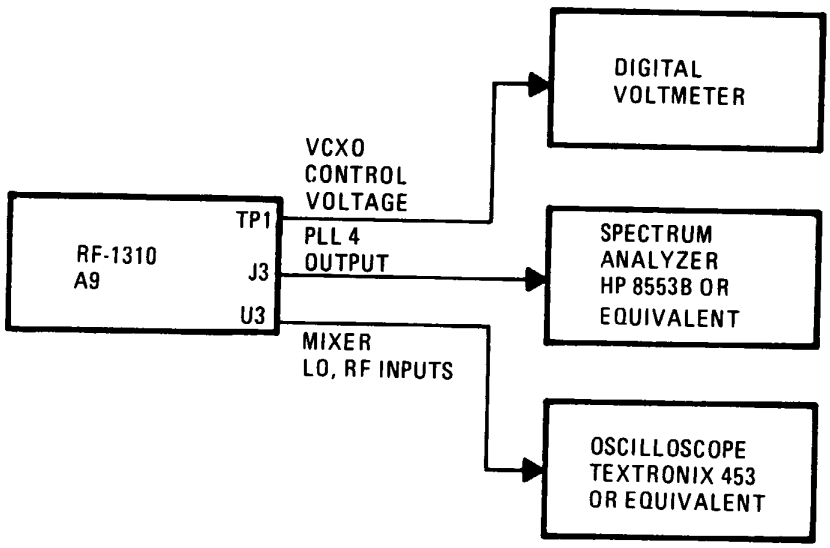


Figure 2. X2 Multiplier, LO, and RF Amplifier Alignment

b. Set exciter to 02.00050 MHz.

c. Monitoring TP1, adjust C23 for 7.5 Vdc.

d. Monitoring J3, adjust T5 and T3 for maximum output level at approximately 40.055 MHz. Level should be -6 dBm ± 3 dB.

e. Monitoring mixer U3 LO input at pin 8, adjust L10 and T4 for maximum level at approximately 40.455 MHz. Level should be approximately 1.25 Vpp ± .5 volts.

f. Monitoring mixer U3 RF input at R28, adjust T2 for a maximum level at 40.000 MHz. Level should be .75 Vpp ± .5 volts. Test is now complete.

5.2 VCXO Alignment

Perform the following procedure to align the VCXO:

a. Connect equipment as shown in figure 3.

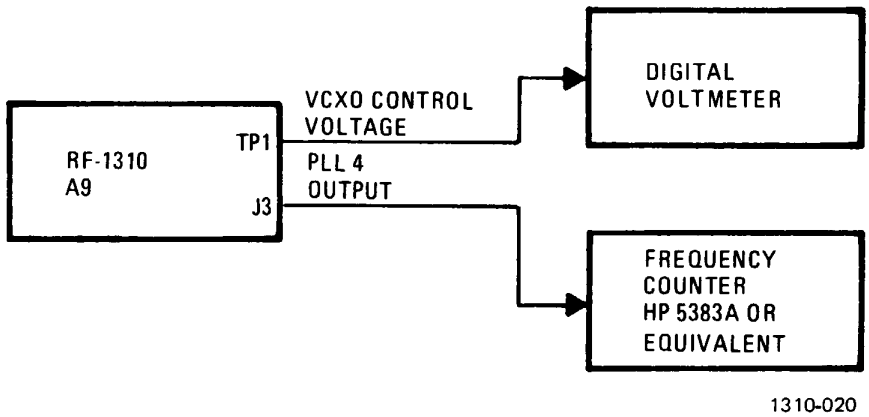


Figure 3. VCXO Alignment

b. Set exciter to 02.00050 MHz. Adjust C23 for 7.5 Vdc.

c. Check that the PLL 4 output frequency, as a function of the exciter tune frequency, agrees with table 2.

Table 2. VCXO Alignment

Exciter Tune Frequency, MHz	PLL 4 Output Frequency, MHz	Approximate TP1 Voltage, Vdc
02.00000	40.060	10.0
02.00050	40.055	7.5
02.00099	40.050	5.0

d. Fully reconnect the A9 assembly to the RF-1310. Initiate BITE self test. Exciter must pass all tests associated with A9 assembly. Test is now complete.

6. PARTS LIST, COMPONENT LOCATIONS, AND SCHEMATIC DIAGRAM

All replaceable components of the A9 assembly are listed in table 3. The component locations are shown in figure 4. Figure 5 is a schematic diagram of PLL 4 Assembly A9.

Table 3. PLL 4 Assembly A9 Parts List (10073-4400 Rev. Y)

Ref. Desig.	Part Number	Description
1	10073-7116	CAN RECT DEEP DRAWN
2	10073-7214	CLIP MOUNTING, MODIFIED
9	10073-7113	SHIELD, COIL
10	E70-0002-002	PAD MNT XSTR TO-5
C1	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C2	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C3	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C4	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C5	C26-0025-100	CAP 10UF 20% 25V TANT
C6	M39014/01-1317V	CAP,1000PF,10% 200VC
C7	M39014/01-1317V	CAP,1000PF,10% 200VC
C8	CM06FD102J03	CAP 1000PF 5% 500V MICA
C9	C26-0025-100	CAP 10UF 20% 25V TANT
C10	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C11	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C12	M39014/01-1535V	CAP .01UF 10% 100V CER-R
C13	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C14	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C15	C26-0025-100	CAP 10UF 20% 25V TANT
C16	C26-0025-100	CAP 10UF 20% 25V TANT
C17	M39014/01-1535V	CAP .01UF 10% 100V CER-R
C18	C26-0025-339	CAP 3.3UF 20% 25V TANT
C19	C25-0003-004	CAP 0.33UF 10% 50V TANT
C20	C26-0025-100	CAP 10UF 20% 25V TANT
C21	CM04ED680F03	CAP 68PF 1% 500V MICA
C22	M39014/01-1535V	CAP .01UF 10% 100V CER-R
C23	C85-0001-002	CAP VAR 1-10PF PIST
C24	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C25	M39014/01-1535V	CAP .01UF 10% 100V CER-R
C26	M39014/01-1535V	CAP .01UF 10% 100V CER-R
C27	CM04ED470J03	CAP 47PF 5% 500V MICA
C28	M39014/01-1535V	CAP .01UF 10% 100V CER-R
C29	M39014/02-1320V	CAP .47UF 10% 50V CER-R
C30	M39014/01-1317V	CAP,1000PF,10% 200VC
C31	M39014/01-1535V	CAP .01UF 10% 100V CER-R
C32	CM04CD010D03	CAP 1PF+-.5PF 500V MICA
C33	CM04ED470J03	CAP 47PF 5% 500V MICA
C34	M39014/02-1310V	CAP .1UF 10% 100V CER-R

Table 3. PLL 4 Assembly A9 Parts List (10073-4400 Rev. Y) (Cont.)

Ref. Desig.	Part Number	Description
C35	CM04ED510J03	CAP 51PF 5% 500V MICA
C36	M39014/01-1535V	CAP .01UF 10% 100V CER-R
C37	M39014/01-1535V	CAP .01UF 10% 100V CER-R
C38	M39014/01-1535V	CAP .01UF 10% 100V CER-R
C39	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C40	M39014/01-1535V	CAP .01UF 10% 100V CER-R
C41	M39014/01-1535V	CAP .01UF 10% 100V CER-R
C42	C26-0025-100	CAP 10UF 20% 25V TANT
C43	CM04ED300J03	CAP 30PF 5% 500V MICA
C44	CM04ED330J03	CAP 33PF 5% 500V MICA
C45	M39014/01-1535V	CAP .01UF 10% 100V CER-R
C46	M39014/01-1535V	CAP .01UF 10% 100V CER-R
C47	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C48	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C49	M39014/01-1535V	CAP .01UF 10% 100V CER-R
C50	C-0912	CAP .015UF 5% 200V MYLAR
C51	C-0911	CAP .01UF 5% 200V MYLAR
C52	CM06FD272J03	CAP 2700PF 5% 500V MICA
C53	CM06FD272J03	CAP 2700PF 5% 500V MICA
C54	CM06FD272J03	CAP 2700PF 5% 500V MICA
C55	C-0912	CAP .015UF 5% 200V MYLAR
C56	C-0912	CAP .015UF 5% 200V MYLAR
C57	C25-0001-301	CAP 1.0UF 20% 20V TANT
C59	CM04ED270J03	CAP 27PF 5% 500V MICA
C60	M39014/01-1535V	CAP .01UF 10% 100V CER-R
C61	M39014/01-1535V	CAP .01UF 10% 100V CER-R
CR1	D25-0002-001	DIODE TUNING MV309
CR2	D25-0002-001	DIODE TUNING MV309
CR4	1N3064	DIODE 75mA 75V SW
CR5	1N3064	DIODE 75mA 75V SW
CR6	1N3064	DIODE 75mA 75V SW
J1	J46-0022-006	HDR 6 PIN 0.100" SR LKG
J2	J-0031	CONN SMB VERT PCB F
J3	J-0031	CONN SMB VERT PCB F
J4	J-0031	CONN SMB VERT PCB F
L1	82027-03	CHOKE WB 50MHZ
L2	82027-03	CHOKE WB 50MHZ
L3	MS14046-9	COIL 27UH 10% FXD RF
L4	MS75084-17	COIL 27.0UH 10% FXD RF
L5	MS75084-3	COIL 1.8UH 10% FXD RF
L6	MS75084-17	COIL 27.0UH 10% FXD RF
L7	MS75084-6	COIL 3.3UH 10% FXD RF
L8	MS90538-8	COIL 68UH 5% FXD RF
L9	MS90538-8	COIL 68UH 5% FXD RF

Table 3. PLL 4 Assembly A9 Parts List (10073-4400 Rev. Y) (Cont.)

Ref. Desig.	Part Number	Description
L10	10073-7011	TRANSFORMER, RF, VARIABLE
Q1	Q05-0001-000	XSTR JFET N-CH
Q2	2N2907	XSTR SS/GP PNP TO-18
Q3	2N2222	XSTR SS/GP NPN TO-18
Q4	2N2369	XSTR SS/RF NPN
Q5	2N2222	XSTR SS/GP NPN TO-18
Q6	Q35-0003-000	XSTR N-CH JFET U310
Q7	2N5109	XSTR RF PWR NPN TO-39
Q8	Q35-0003-000	XSTR N-CH JFET U310
Q9	2N2907	XSTR SS/GP PNP TO-18
Q10	Q35-0003-000	XSTR N-CH JFET U310
R1	R65-0003-201	RES 200 5% 1/4W CAR FILM
R2	R65-0003-201	RES 200 5% 1/4W CAR FILM
R3	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R4	R65-0003-332	RES 3.3K 5% 1/4W CAR FILM
R5	R65-0003-201	RES 200 5% 1/4W CAR FILM
R6	RN55D1211F	RES 1210 1% 1/8W MET FLM
R7	RN55D6810F	RES 681 1% 1/8W MET FLM
R8	R65-0003-121	RES 120 5% 1/4W CAR FILM
R9	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R10	RN55D3321F	RES 3320 1% 1/8W MET FLM
R11	R65-0003-201	RES 200 5% 1/4W CAR FILM
R12	R65-0003-101	RES 100 5% 1/4W CAR FILM
R13	RN55D6810F	RES 681 1% 1/8W MET FLM
R14	RN55D6810F	RES 681 1% 1/8W MET FLM
R15	RN55D6810F	RES 681 1% 1/8W MET FLM
R16	R65-0003-911	RES 910 5% 1/4W CAR FILM
R17	R65-0003-101	RES 100 5% 1/4W CAR FILM
R18	R65-0003-101	RES 100 5% 1/4W CAR FILM
R19	R65-0003-470	RES 47 5% 1/4W CAR FILM
R20	R65-0003-470	RES 47 5% 1/4W CAR FILM
R21	R65-0003-201	RES 200 5% 1/4W CAR FILM
R22	R65-0003-242	RES 2.4K 5% 1/4W CAR FILM
R23	R65-0003-182	RES 1.8K 5% 1/4W CAR FILM
R24	R65-0003-511	RES 510 5% 1/4W CAR FILM
R25	R65-0003-471	RES 470 5% 1/4W CAR FILM
R26	R65-0003-390	RES 39 5% 1/4W CAR FILM
R27	R65-0003-121	RES 120 5% 1/4W CAR FILM
R28	R65-0003-101	RES 100 5% 1/4W CAR FILM
R29	R65-0003-750	RES 75 5% 1/4W CAR FILM
R30	R65-0003-101	RES 100 5% 1/4W CAR FILM
R31	R65-0003-101	RES 100 5% 1/4W CAR FILM
R32	R65-0003-101	RES 100 5% 1/4W CAR FILM
R33	R65-0003-510	RES 51 5% 1/4W CAR FILM
R34	R65-0003-750	RES 75 5% 1/4W CAR FILM

Table 3. PLL 4 Assembly A9 Parts List (10073-4400 Rev. Y) (Cont.)

Ref. Desig.	Part Number	Description
R35	RN55D1001F	RES 1000 1% 1/8W MET FLM
R36	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R37	R65-0003-470	RES 47 5% 1/4W CAR FILM
R38 – R41	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R42	R65-0003-471	RES 470 5% 1/4W CAR FILM
R43	R65-0003-101	RES 100 5% 1/4W CAR FILM
T1	10073-7008	TRANSFORMER, RF, FIXED
T2	10073-7012	TRANSFORMER, RF, VARIABLE
T3	10073-7015	TRANSFORMER, RF, VARIABLE
T4, T5	10073-7011	TRANSFORMER, RF, VARIABLE
TP1	J-0071	TP PWB BRN TOP ACCS .080"
TP2	J-0066	TP PWB RED TOP ACCS .080"
TP3	J-0069	TP PWB ORN TOP ACCS .080"
TP4	J-0070	TP PWB YEL TOP ACCS .080"
TP5	J-0068	TP PWB GRN TOP ACCS .080"
U1	IC-0430	IC 4044 PLASTIC CMOS
U2	I20-0005-001	IC LM211H COMPARATOR
U3	I51-0003-003	MIXER DB SRA-1
VR1	1N5236	DIODE 7.5V 20% .5W ZENER
VR2	I11-0001-001	IC VR 7805 +5V 1.5A 4%
Y1	10073-7039	CRYSTAL, 20.0275 MHZ

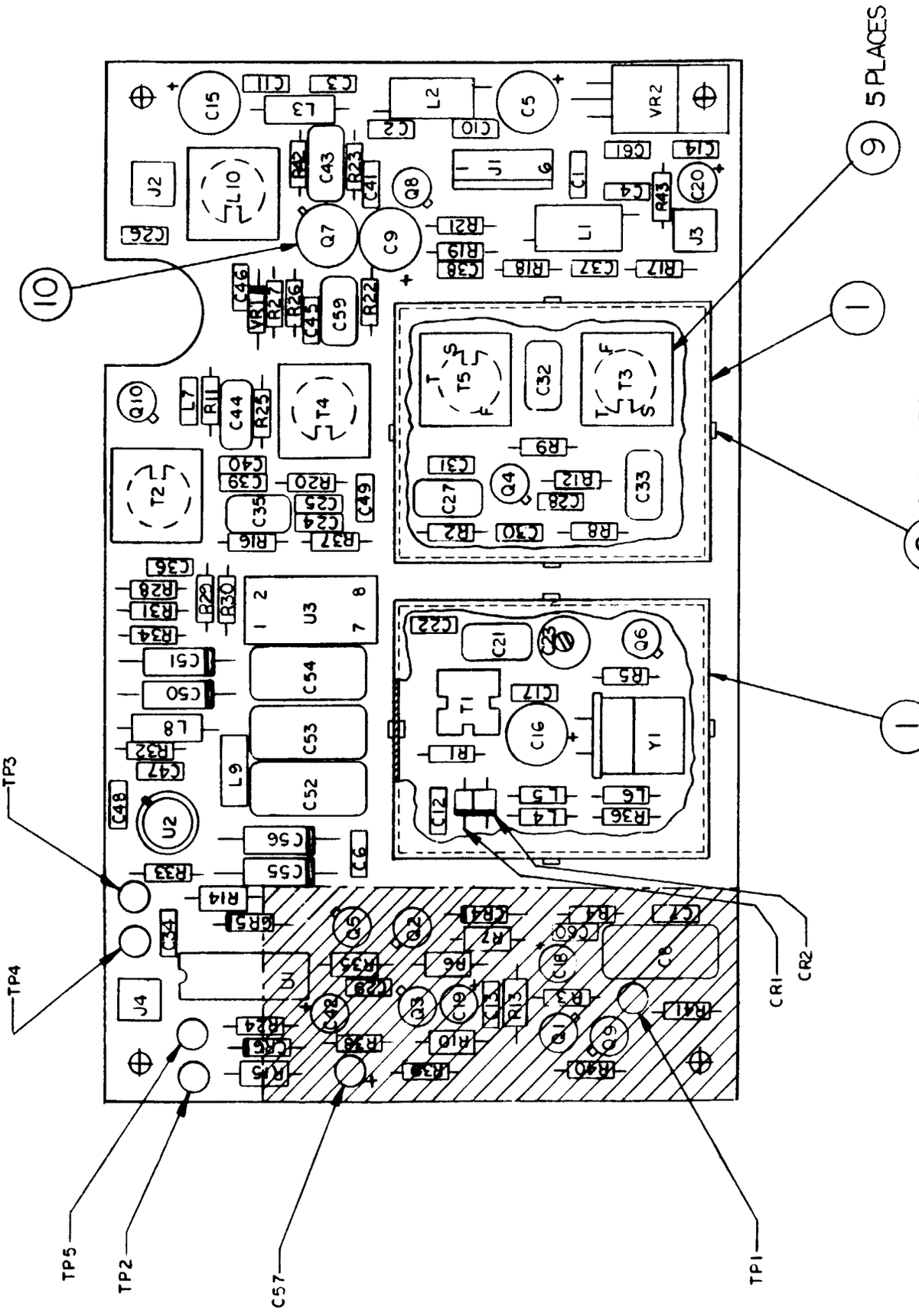


Figure 4. PLL 4 Assembly A9 Component Location Diagram (10073-4400 Rev. E)

NOTE: UNLESS OTHERWISE SPECIFIED:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR A COMPLETE DESIGNATION, PREFIX WITH UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.
2. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, ±5%.
3. ALL CAPACITOR VALUES ARE IN MICROFARADS.
4. VENDOR PART NO. CALLOUTS ARE FOR REFERENCE ONLY. COMPONENTS ARE SUPPLIED PER PART NO. IN PARTS LIST.
5. ALL INDUCTOR VALUES ARE IN MICROHENRIES.

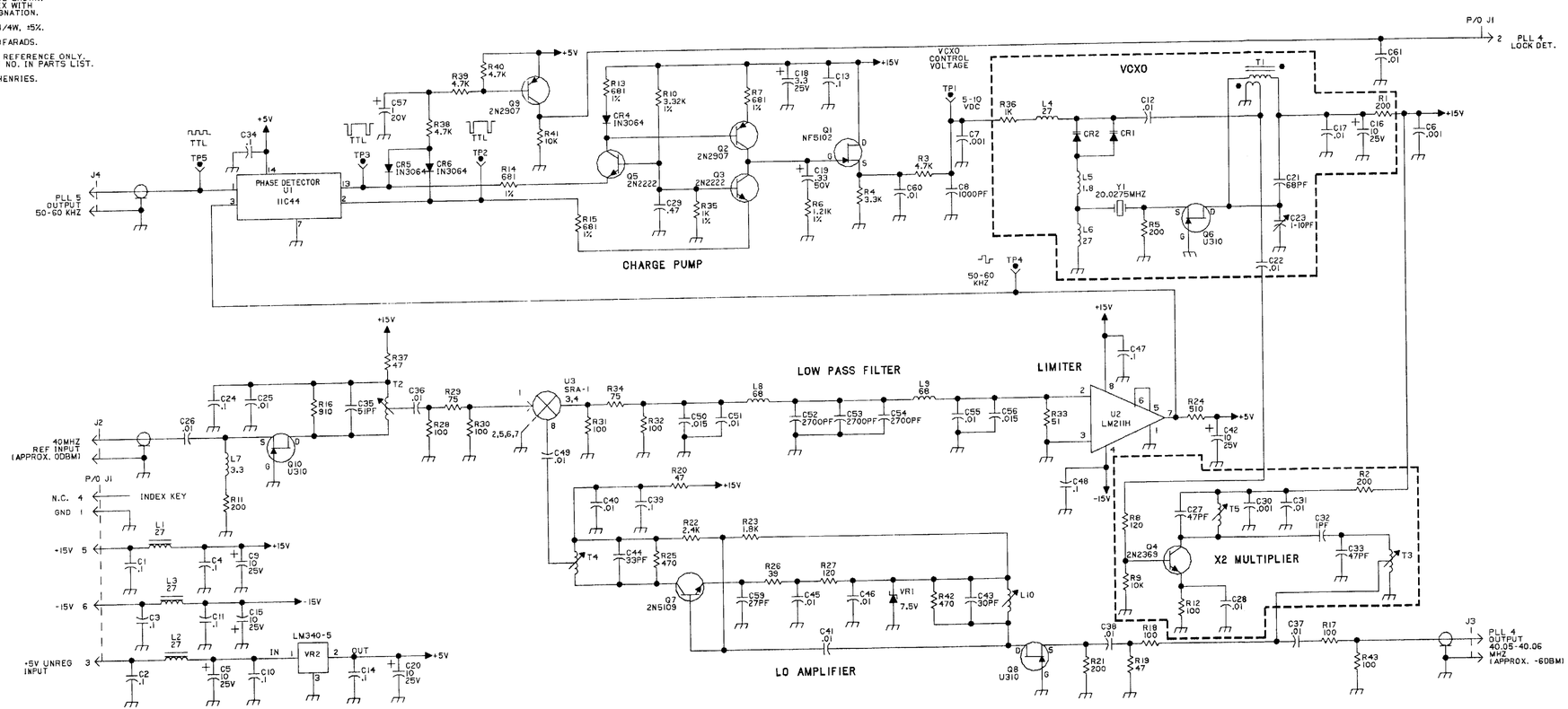
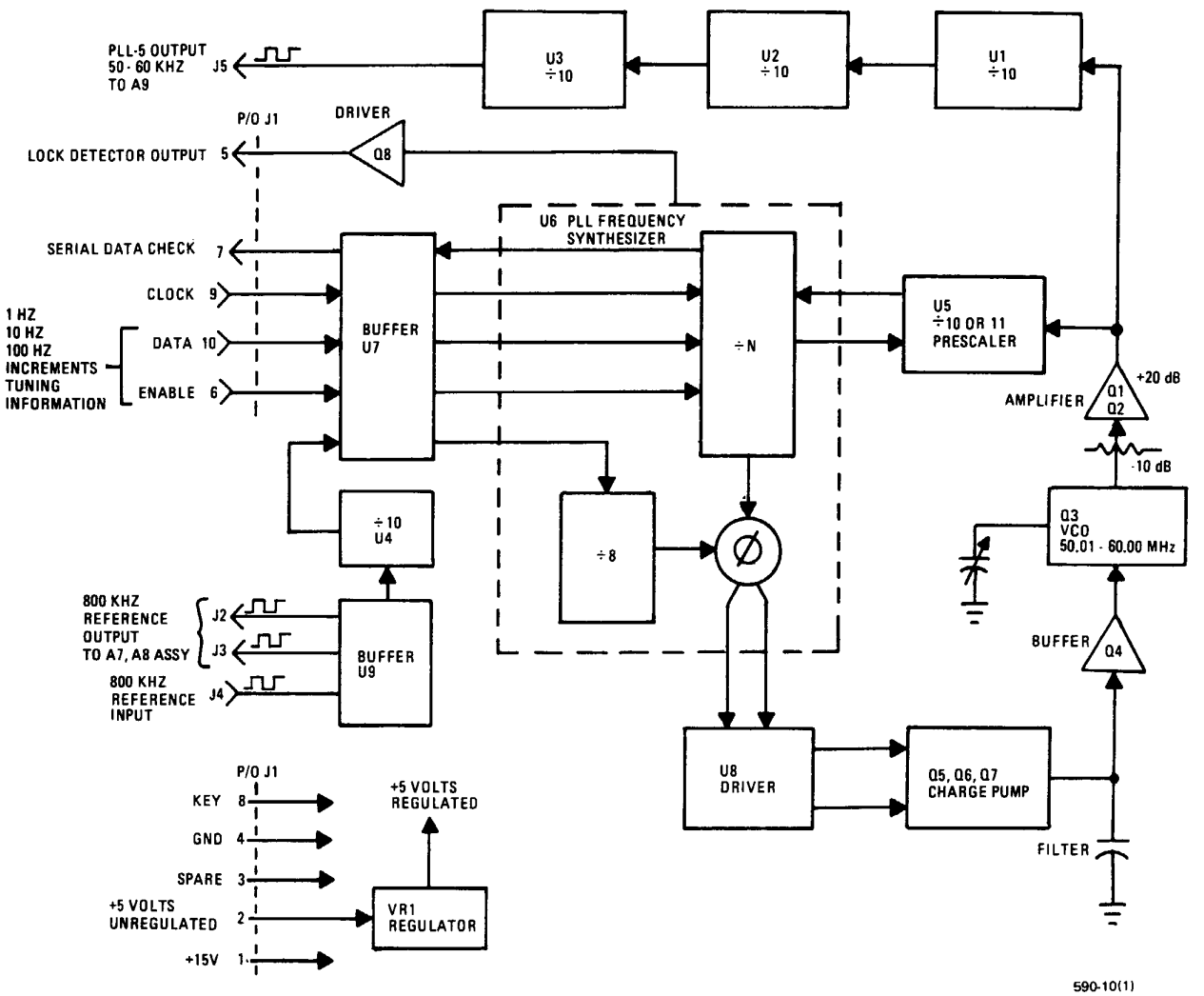


Figure 5. PLL 4 Assembly A9 Schematic Diagram (10073-4401 Rev. D)

A10
PLL 5 ASSEMBLY



590-10(1)

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PLL 5 ASSEMBLY A10

1. GENERAL DESCRIPTION

PLL 5 Assembly A10 is a single phase locked loop (PLL) synthesizer that ultimately provides the 1 Hz, 10 Hz, and 100 Hz tuning increments of the LO 1 frequency. Tuning increments are determined by the digits in the corresponding positions of the transmit frequency .

Frequency select input data is applied to the assembly in serial data form under Control Board Assembly A14 microprocessor control. A10 assembly output to PLL 4 Assembly A9 is a variable 50 to 60 kHz signal in 10 Hz controllable steps. Since 1000 frequency steps are possible, the net results of A10 operation (after further translation to 1 Hz increments in the synthesizer chain) are 1 Hz, 10 Hz, and 100 Hz tuning increments in the LO 1 output.

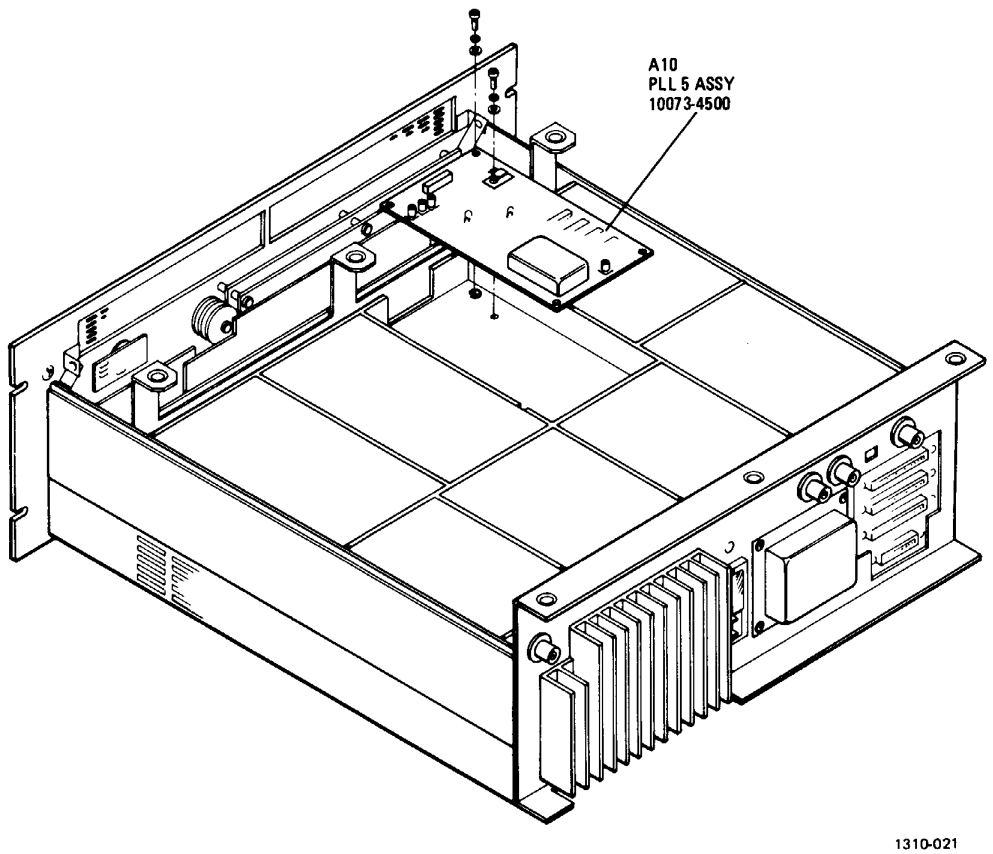


Figure 1. PLL 5 Assembly A10 Location

2. INTERFACE CONNECTIONS

Table 1 details the various input/output connections and other relevant data.

Table 1. PLL 5 Assembly Interface Connections

Connector	Function	Characteristics
J1-1	+ 15 Volts	Approximately 25 mA
J1-2	+ 5 Volts Unregulated	Approximately 240 mA
J1-3	Spare	
J1-4	Ground	
J1-5	Lock Detector Output	+ 5 Vdc = unlocked, 0 Vdc = locked, P/O BITE test
J1-6	Enable	+ going pulse = enabled
J1-7	Serial Data Check	P/O BITE test, + 5 Vdc = ok
J1-8	Key	
J1-9	Clock	TTL, 750 kHz
J1-10	Data	Serial TTL
J2	800 kHz Reference Output	TTL
J3	800 kHz Reference Output	TTL
J4	800 kHz Reference Input	TTL
J5	PLL 5 Output	TTL, 50 to 60 kHz

3. CIRCUIT DESCRIPTION

NOTE

A10 assembly operation is similar (in operation) to the general divide-by-N PLL and charge pump circuits described in section 4. A review of section 4 at this point would aid in the understanding of A10 assembly operation.

3.1 Reference Generation

The 800 kHz from Reference Generator Assembly A12 enters PLL 5 Assembly A10 at J4. This signal is buffered via TTL NAND gates in U9 and directed through J2 and J3 to the A7 and A8 assemblies. It is also routed to divide-by-10 counter U4 where it is divided down to 80 kHz. This 80 kHz signal is applied via buffer U7 to a divide-by-eight counter internal to U6 to produce a 10 kHz reference signal. Since this has been derived from

the RF-1310 crystal frequency standard via the A12 assembly, stable and accurate A10 assembly operation is assured.

3.2 Divide-by-N Counter

Since the A10 assembly requires a variable 50 to 60 kHz output frequency, a programmable counter has been designed into the VCO feedback path to the phase comparator. This counter consists of dual modulus divide-by-10/divide-by-11 prescaler U5 and a programmable divide-by-N counter internal to U6. Together, U5 and the programmable portion of U6 create a total division range of N = 5001 to N = 6000, where N is a function of the digits entered in the 1, 10, and 100 positions of the frequency display.

The output of the divide-by-N counter will always attempt to equal the 10.000 kHz reference frequency at the phase comparator inputs, despite changes in the divide-by-N factor due to changing the 1, 10, or 100 Hz exciter frequency display digits. The VCO frequency will change to accomplish this (in response to command signals generated by the phase comparator). The VCO frequency will always equal (N) (reference frequency), or (N) (10.000 kHz) = 50.01 MHz to 60.00 MHz. Division of this range by 1000 will result in the required A10 assembly output range of 50.01 kHz to 60.00 kHz.

The exact value of N is determined by the value of the digits in the 1, 10, and 100 places of the displayed frequency. These front panel selections cause the A14 assembly to generate a serial data code containing information pertaining to the values of the digits chosen. This code is applied synchronously with the 750 kHz system clock to U6 whenever the U6 enable line is gated open by the A14 assembly. In general, N = (6000-XXX), where XXX is the value of the three least significant bits of the transmit frequency. The least significant digit is not selectable and is always zero.

For example, tuning the RF-1310 to 10.401470 MHz would make N = (6000-470) = 5530. The VCO frequency will be (N) (reference) = (5530) (10.000 kHz) = 55.30 MHz. The VCO output is then divided by 1000 to produce the A10 assembly output at 55.30 kHz.

The actual frequency of the A10 assembly output may therefore be calculated from the following formula: f = 10 (6000-XXX) Hz, where XXX is the value of the exciter 100 Hz, 10 Hz, and 1 Hz digits of the transmit frequency.

3.3 Phase Comparator and Charge Pump Operation

Phase comparison of the 10 kHz reference and the 10 kHz VCO derived signal at the divide-by-N counter output is accomplished by a phase comparator internal to U6. When these two signals are equal in frequency and phase, the phase comparator outputs at TP2 and TP3 are essentially 5 Vdc. U8 functions as a buffer for the phase comparator to the input of the charge pump circuit, consisting of Q5, Q6, and Q7. This 5-volt level holds Q6 and Q7 off. Consequently, Q5 is also off and the voltage across C24 is at some constant level. This biases Q4 to some specific source current, and the voltage across R16 at TP1 is constant. This VCO control voltage holds the VCO frequency constant, somewhere between 50 and 60 MHz.

Assume that the VCO derived feedback signal at the divide-by-N counter output is suddenly less than the reference frequency. This is what will happen at the instant the divide-by-N factor is increased. Since the two phase comparator inputs are no longer equal, the phase comparator will output a series of negative pulses at TP3. Q7 will turn on, forcing Q5 on. Q5 will start to pump charge into C24, causing Q4 to conduct more current as the voltage across C24 increases. This produces a higher dc level at TP1. The VCO frequency will increase in response to it until the signals at the phase comparator inputs are again equal. As the VCO derived signal is approaching the reference frequency, the output pulse width at TP3 will get smaller until the signal is essentially + 5 Vdc again. Q7 and Q5 will turn off. The voltage at C24 will rest at this new higher dc value causing the VCO frequency to also rest at its new higher value.

Assume that the VCO feedback signal at the divide-by-N counter output is suddenly greater than the reference signal (meaning that the divide-by-N factor has just decreased). The two phase comparator inputs are again unequal, but now the phase comparator will output the negative pulses at TP2. Q6 will turn on, drawing charge out of C24, and causing the VCO control voltage to drop. Consequently, the VCO will shift lower in frequency, and the VCO derived signal at the phase comparator input will again approach the reference frequency. The output pulses will become very narrow and the signal will almost become a steady 5 Vdc level. This will turn Q6 off and the VCO will stabilize at the lower frequency.

3.4 VCO Operation and Control

A charge pump circuit consisting of Q5, Q6, Q7, and associated components in conjunction with filters C24 and C25 convert the two phase comparator pulse outputs into an analog dc control voltage. Buffer amplifier Q4 applies this control voltage to the varactor diode string in the VCO. The VCO itself is a JFET (Q3) Hartley oscillator stage whose frequency shifts as the capacitance of the varactor diodes changes with changes in control voltage. A net control voltage change of 5 Vdc to 10 Vdc produces a net VCO frequency shift of 50 MHz to 60 MHz. Note also that the 10 volt limit corresponds to N = 6000, while the 5 volt limit corresponds to N = 5001.

The VCO output is fed through 10 dB attenuator network, R10 and R11, to a + 20 dB gain amplifier stage consisting of Q1, Q2, and associated components. This output is split and sent to divide-by-N circuit U5 and U6 and to a divide-by-1000 divider chain consisting of U1, U2, and U3. This divider output is therefore at a frequency range of 50.01 to 60 kHz (in 10 Hz increments) and is the PLL 5 output. This output is fed through J5 to PLL 4 Assembly A9 where further signal processing occurs.

3.5 BITE Circuits

The A10 assembly contains two circuits for self-test evaluation:

- Lock detector Q8, whose output is 0 Vdc whenever the PLL is tracking properly. This line is constantly monitored by the A14 assembly. It will cause a front panel fault light to appear if the loop ever unlocks.

- Serial data check that verifies the tuning data from the A14 assembly has been received and properly translated into the correct divide-by-N factor. A serial data word is sent on the data line (J1 pin 10) and the U6 serial data check line is read back to the A14 assembly (J1 pin 7). If the word has been received and properly decoded, this line will pulse to + 5 Vdc. The serial data check occurs automatically, but only when the exciter BITE self test is actuated.

4. MAINTENANCE

The following adjustments should not be performed as a routine maintenance procedure, but only when a failure indicates a definite need. All tests should be performed with all connections in normal contact, unless otherwise specified.

4.1 VCO Frequency Adjustment

a. Connect equipment as shown in figure 2.

b. Set RF-1310 frequency to 02.00050 MHz.

c. Adjust C20 for 7.5 Vdc at TP1. PLL 5 output vs. exciter tune frequency should agree with table 2. The output waveform should always be a TTL signal.

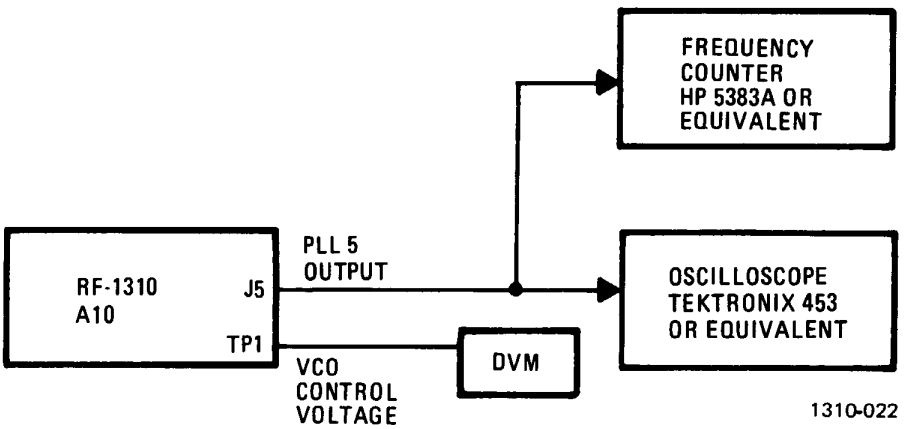


Figure 2. PLL 5 VCO Adjustment

Table 2. VCO Frequency Range

Exciter Tune Frequency, MHz	PLL 5 Output Frequency, kHz	Approximate TP1 Voltage, Vdc
02.00050	55.00	7.5
02.00000	60.00	10.0
02.00099	50.01	5.0

d. Fully reconnect the A10 assembly to RF-1310. Initiate BITE self-test. Exciter must pass all tests associated with assembly A10. Test is complete.

5. PARTS LIST, COMPONENT LOCATIONS, AND SCHEMATIC DIAGRAMS

All replaceable components of PLL 5 Assembly A10 are listed in table 3. Component locations are shown in figure 3. The PLL 5 assembly A10 schematic is shown in figure 4.

Table 3. PLL 5 Assembly A10 Parts List (10073-4500 Rev. N)

Ref. Desig.	Part Number	Description
4	10073-7214	CLIP MOUNTING, MODIFIED
5	10073-7116	CAN RECT DEEP DRAWN
C1	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C2	C26-0025-470	CAP 47UF 20% 25V TANT
C3	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C4	M39014/01-1535V	CAP .01UF 10% 100V CER-R
C5	M39014/01-1317V	CAP,1000PF,10% 200VC
C6	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C7	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C8	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C9	M39014/01-1535V	CAP .01UF 10% 100V CER-R
C10	M39014/01-1535V	CAP .01UF 10% 100V CER-R
C11	M39014/01-1535V	CAP .01UF 10% 100V CER-R
C12	M39014/01-1535V	CAP .01UF 10% 100V CER-R
C13	M39014/01-1317V	CAP,1000PF,10% 200VC
C14	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C15	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C16	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C17	C26-0025-680	CAP 68UF 20% 25V TANT
C18	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C19	M39014/01-1535V	CAP .01UF 10% 100V CER-R
C20	C84-0003-008	CAP VAR 3-15PF CER
C21	M39014/01-1317V	CAP,1000PF,10% 200VC
C22	M39014/01-1317V	CAP,1000PF,10% 200VC
C23	C26-0025-100	CAP 10UF 20% 25V TANT
C24	C25-0003-004	CAP 0.33UF 10% 50V TANT
C25	M39014/01-1546V	CAP .039UF 10% 50V CER-R
C26	C26-0025-470	CAP 47UF 20% 25V TANT
C27	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C28	C26-0035-109	CAP 1.0UF 20% 35V TANT
C29	C26-0016-151	CAP 150UF 20% 16V TANT
C30	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C31	C26-0025-100	CAP 10UF 20% 25V TANT
C32	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C33	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C34	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C35	C26-0035-109	CAP 1.0UF 20% 35V TANT
C36	M39014/02-1310V	CAP .1UF 10% 100V CER-R
CR3	D25-0002-001	DIODE TUNING MV309
CR4	D25-0002-001	DIODE TUNING MV309

Table 3. PLL 5 Assembly A10 Parts List (10073-4500 Rev. N) (Cont.)

Ref. Desig.	Part Number	Description
CR5	D25-0002-001	DIODE TUNING MV309
CR6	D25-0002-001	DIODE TUNING MV309
CR7	D25-0002-001	DIODE TUNING MV309
CR8	D25-0002-001	DIODE TUNING MV309
CR9	1N6263	DIODE .40W 60V HOT CARR
CR10	1N3064	DIODE 75mA 75V SW
CR11	D25-0002-001	DIODE TUNING MV309
CR12	D25-0002-001	DIODE TUNING MV309
J1	J46-0032-010	HDR 10 PIN 0.100" SR
J2	J-0031	CONN SMB VERT PCB F
J3	J-0031	CONN SMB VERT PCB F
J4	J-0031	CONN SMB VERT PCB F
J5	J-0031	CONN SMB VERT PCB F
L1	MS14046-9	COIL 27UH 10% FXD RF
L2	MS75084-3	COIL 1.8UH 10% FXD RF
L3	MS75084-10	COIL 6.8UH 10% FXD RF
L4	82027-03	CHOKE WB 50MHZ
Q1	Q35-0003-000	XSTR N-CH JFET U310
Q2	2N2369	XSTR SS/RF NPN
Q3	Q35-0003-000	XSTR N-CH JFET U310
Q4	Q05-0001-000	XSTR JFET N-CH
Q5	2N2907	XSTR SS/GP PNP TO-18
Q6	2N2222	XSTR SS/GP NPN TO-18
Q7	2N2222	XSTR SS/GP NPN TO-18
Q8	2N2907	XSTR SS/GP PNP TO-18
R1	R65-0003-201	RES 200 5% 1/4W CAR FILM
R2	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R3	R65-0003-513	RES 51K 5% 1/4W CAR FILM
R4	R65-0003-270	RES 27 5% 1/4W CAR FILM
R5	R65-0003-201	RES 200 5% 1/4W CAR FILM
R6	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R7	R65-0003-152	RES 1.5K 5% 1/4W CAR FILM
R8	R65-0003-100	RES 10 5% 1/4W CAR FILM
R9	R65-0003-151	RES 150 5% 1/4W CAR FILM
R10	R65-0003-101	RES 100 5% 1/4W CAR FILM
R11	R65-0003-201	RES 200 5% 1/4W CAR FILM
R12	R65-0003-101	RES 100 5% 1/4W CAR FILM
R13	R65-0003-470	RES 47 5% 1/4W CAR FILM
R14	R65-0003-513	RES 51K 5% 1/4W CAR FILM
R15	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM

Table 3. PLL 5 Assembly A10 Parts List (10073-4500 Rev. N) (Cont.)

Ref. Desig.	Part Number	Description
R16	R65-0003-272	RES 2.7K 5% 1/4W CAR FILM
R17	RN55D3651F	RES 3650 1% 1/8W MET FLM
R18	R65-0003-470	RES 47 5% 1/4W CAR FILM
R19	R65-0003-470	RES 47 5% 1/4W CAR FILM
R20	RN55D6810F	RES 681 1% 1/8W MET FLM
R21	RN55D6810F	RES 681 1% 1/8W MET FLM
R22	RN55D9091F	RES 9090 1% 1/8W MET FLM
R23	RN55D3321F	RES 3320 1% 1/8W MET FLM
R24	RN55D6810F	RES 681 1% 1/8W MET FLM
R25	RN55D6810F	RES 681 1% 1/8W MET FLM
R26	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R27	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R28	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R29	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R30	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R31	R65-0003-103	RES 10K 5% 1/4W CAR FILM
T1	10073-7002	TRANSFORMER, RF, FIXED
TP1	J-0071	TP PWB BRN TOP ACCS .080"
TP2	J-0066	TP PWB RED TOP ACCS .080"
TP3	J-0069	TP PWB ORN TOP ACCS .080"
TP4	J-0070	TP PWB YEL TOP ACCS .080"
TP5	J-0068	TP PWB GRN TOP ACCS .080"
U1	I65-0004-001	IC PRESCALER 10/11 12013
U2	I05-0000-090	IC 74LS90 PLASTIC TTL
U3	I05-0000-090	IC 74LS90 PLASTIC TTL
U4	I05-0000-090	IC 74LS90 PLASTIC TTL
U5	I65-0004-001	IC PRESCALER 10/11 12013
U6	I70-0002-001	IC MC145156 SYNTH PLA
U7	I01-0000-019	IC 4050B PLASTIC CMOS
U8	I05-0000-000	IC 74LS00 PLASTIC TTL
U9	I05-0000-000	IC 74LS00 PLASTIC TTL
VR1	I11-0001-001	IC VR 7805 +5V 1.5A 4%

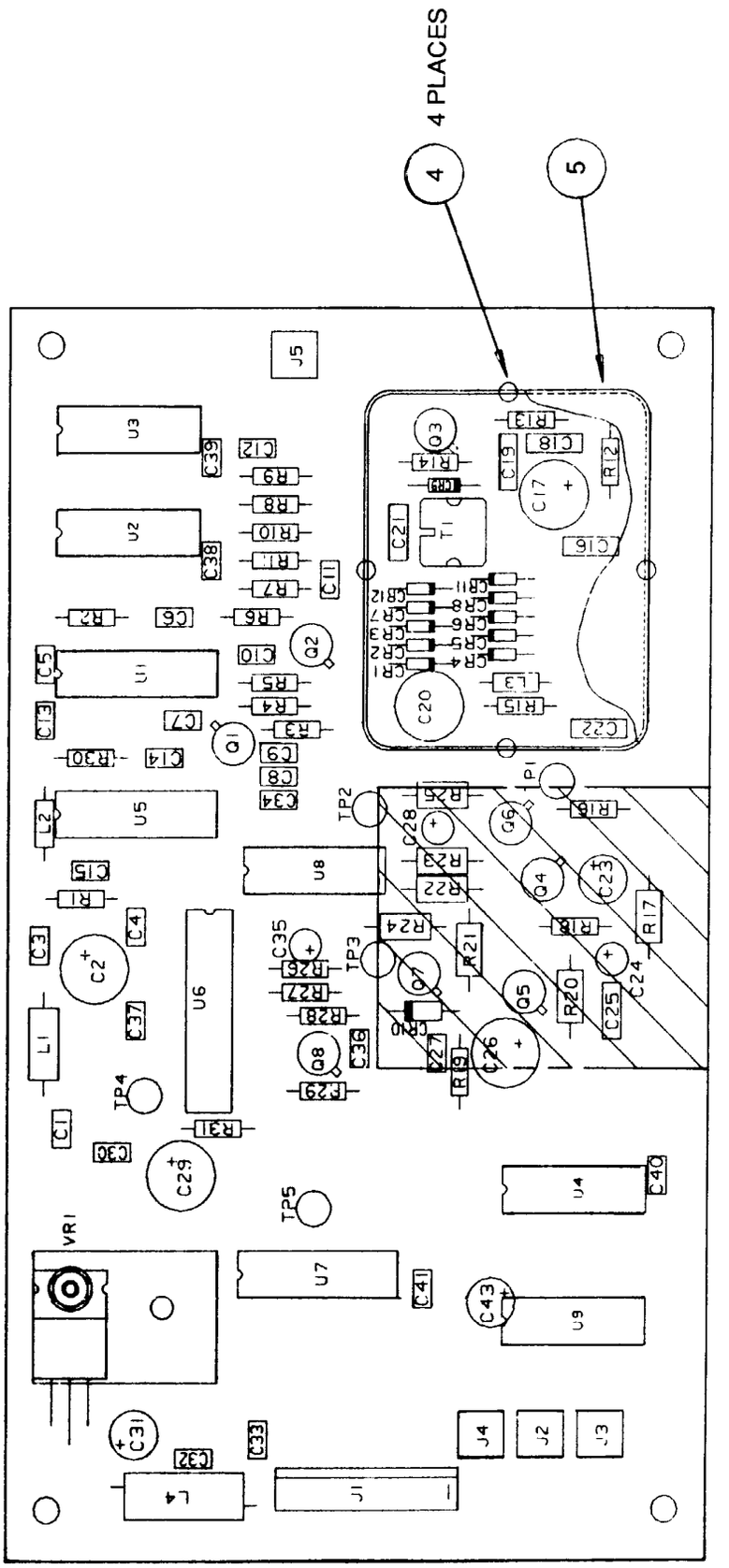


Figure 3. PLL 5 Assembly A10 Component Location Diagram (10073-4500 Rev. C)

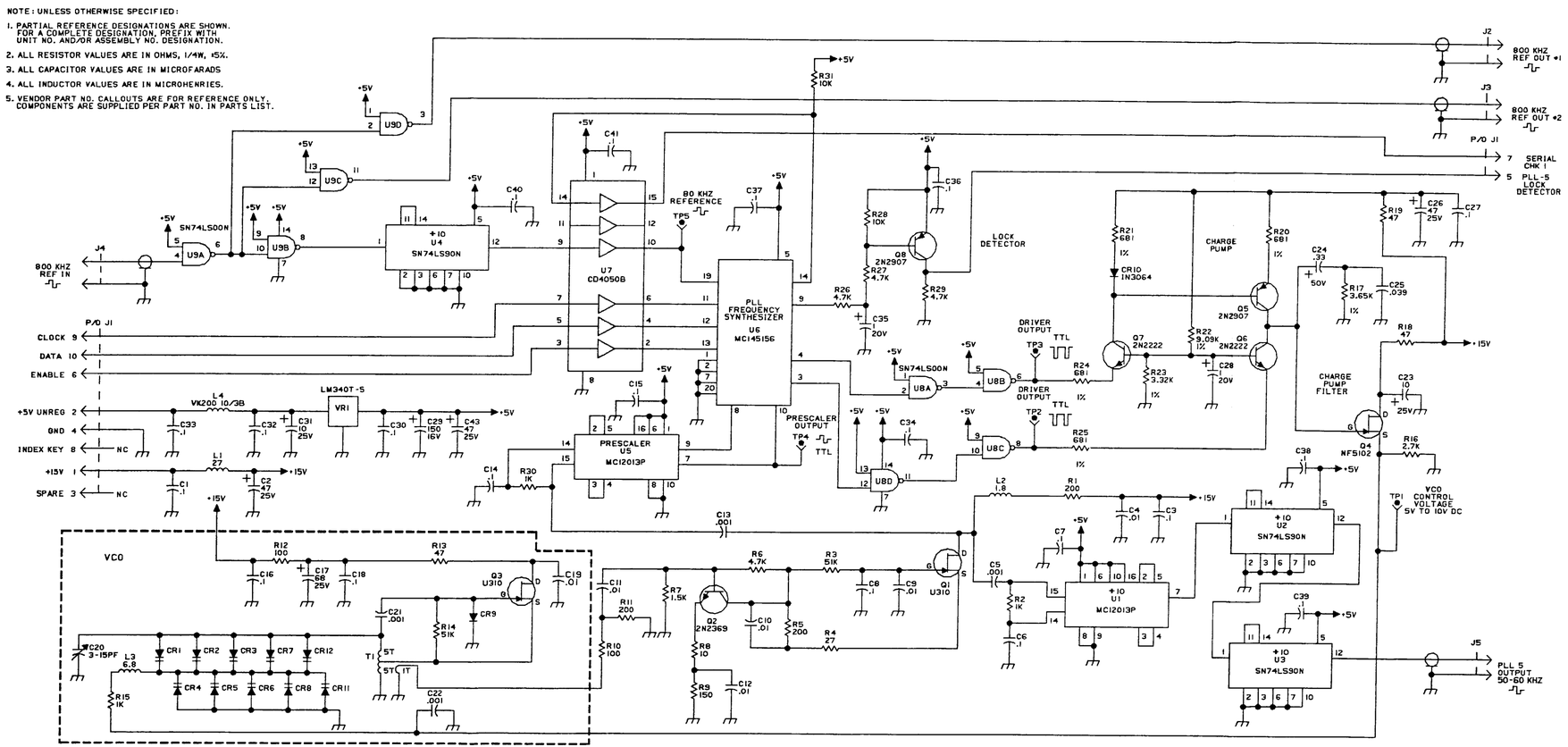
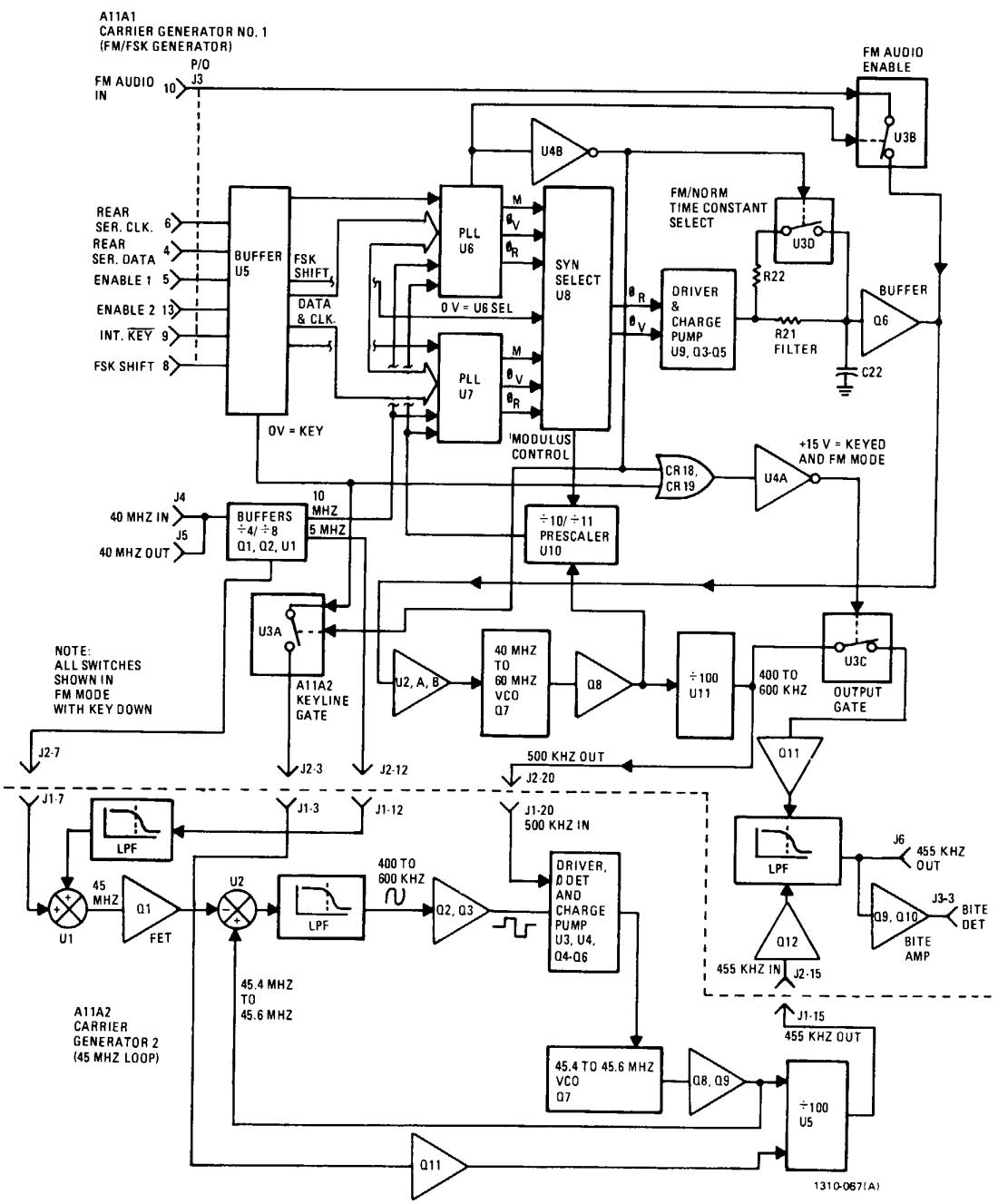


Figure 4. PLL 5 Assembly A10 Schematic Diagram (10073-4501 Rev. E)

A11
CARRIER GENERATOR ASSEMBLY



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CARRIER GENERATOR A11

1. INTRODUCTION

Carrier Generator Assembly A11 consists of the following two subassemblies mounted together in a motherboard/daughterboard combination:

- FSK/FM Generator Assembly A11A1 (motherboard)
- 45 MHz Loop Assembly A11A2 (daughterboard)

The assembly locations are shown in figure 1.

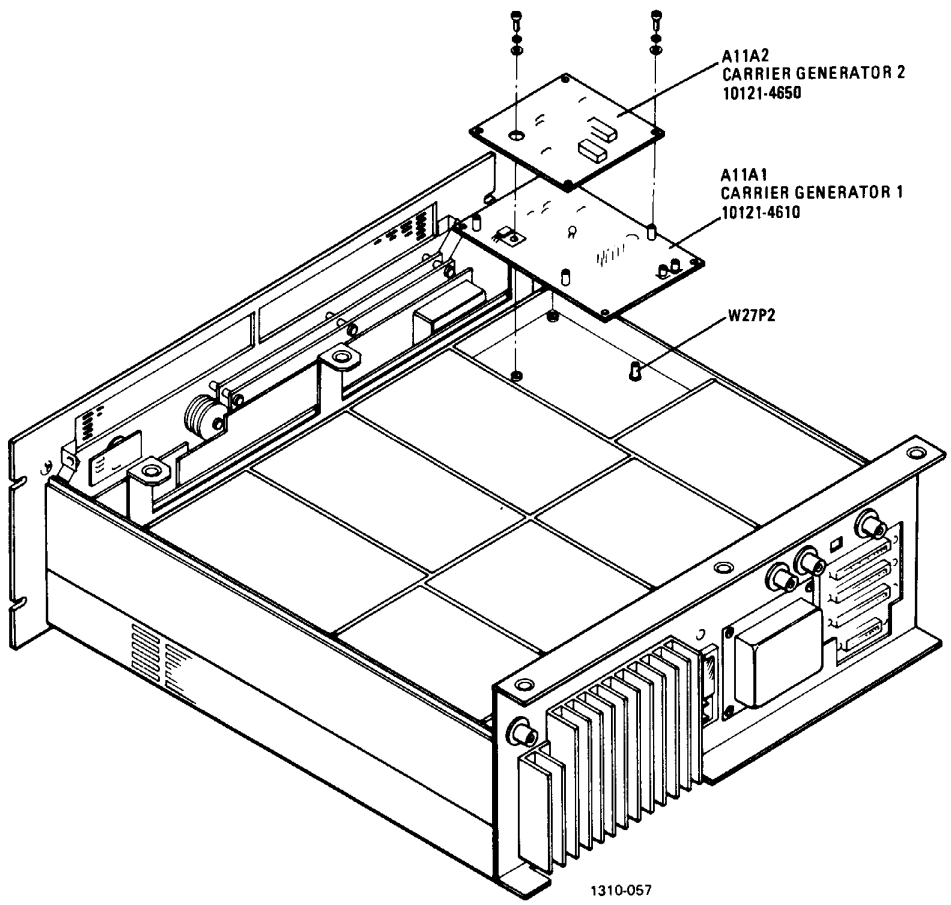


Figure 1. Carrier Generator Assembly A11 Location

The A11 assembly provides three main functions:

- Generation of a 455 kHz intermediate carrier frequency for CW mode, carrier injection for sideband modulation, or carrier reinsertion (if desired) for sideband modes
- Direct narrowband (8 kHz deviation) FM modulation of a 455 kHz carrier using audio supplied from the A5 assembly

- Frequency shift keying (FSK) tone generation centered at 455 kHz with up to ± 1 kHz tone spacing and 1 Hz resolution

2. FSK/FM GENERATOR ASSEMBLY A11A1

FSK/FM Generator Assembly A11A1 performs the following two basic functions:

a. Generates a reference signal for a PLL located on the 45 MHz Loop Assembly, when not in FM mode

- CW, AM, USB, LSB, or 2ISB modes: 500 kHz CW reference.
- MCW: 454 kHz CW reference
- FSK mode: The 500 kHz reference which shifts by an amount proportional to the FSK tone spacing selected. For the maximum transmitted FSK shift allowed (± 1 kHz), the reference will shift ± 100 kHz about 500 kHz.

  Refer to the A14 assembly subsection, table 5 of this manual for information concerning FSK frequency selection.

b. Generates a FM signal centered at 455 kHz when in FM mode.

2.1 A11A1 Interface Connections

Table 1 lists the various input/output connections and any other relevant data.

Table 1. A11A1 Assembly Interface Connections

Connector	Function	Characteristics
J1-1	Power	+ 5 V unregulated, 275 mA
J1-2	Index Key	
J1-3	Power	+ 15 Vdc, 125 mA
J2-1	45 MHz Lock Detector	0 Vdc = Locked
J2-2	Power	+ 5 Vdc
J2-3	Internal Key	0 = active
J2-4	Power	+ 15 Vdc
J2-5, J2-6	Ground	
J2-7	40 MHz Output	40 MHz, + 7 dBm
J2-8 - J2-11	Ground	

Table 1. A11A1 Assembly Interface Connections (Cont.)

Connector	Function	Characteristics
J2-12	5 MHz Output	5 MHz, TTL
J2-13, J2-14	Ground	
J2-15	455 kHz Input	455 kHz, TTL
J2-16 - J2-19	Ground	
J2-20	500 kHz Out	500 kHz, TTL
J3-1	Ground	
J3-2	Spare	
J3-3	BITE Detector	Approximately 1.1 Vdc for 2 dBm, 455 kHz output
J3-4	Rear Serial Data	TTL levels
J3-5	Serial Enable 1	Positive TTL pulse = U6 enabled
J3-6	Rear Serial Clock	TTL levels
J3-7	45 MHz Lock	See J2-1
J3-8	FSK shift	0 = + FSK shift, +5 = -FSK shift
J3-9	Internal $\overline{\text{Key}}$	0 Vdc = active
J3-10	FM Audio Input	70 mV_{rms} produces approximately 8 kHz deviation, 600 ohms
J3-11	Lock Detector 1	0 Vdc = synthesizer U7 locked
J3-12	Spare	
J3-13	Serial Enable 2	Positive TTL pulses = U7 enabled
J3-14	Serial Check Bit 1	Test bit, P/O BITE testing
J3-15	Lock Detector 2	0 Vdc = synthesizer U6 locked
J3-16	Serial Check Bit 2	Test bit, P/O BITE testing
J4	40 MHz Input	40 MHz, 0 dBm, 50 ohms
J5	40 MHz Output	40 MHz, +0 dBm, 50 ohms
J6	455 kHz Output	455 kHz, 2 dBm, 50 ohms

2.2 A11A1 Assembly Circuit Description

The majority of the A11A1 assembly consists of circuits which accurately control the 40-60 MHz VCO stage Q7. The VCO output is then divided down to provide the signals detailed in section 2. The error signal generated

by one of two selected PLL synthesizer IC (U6 or U7) will drive the VCO to a frequency determined by the values shifted into programmable divide-by-N counters (internal to U6 and U7). These divide-by-N values are supplied by Control Assembly A14. The values depend on the mode of operation selected. Table 2 lists A11A1 assembly control line status and component selections.

Table 2. A11A1 Assembly Control Line and Component Status for Selected Modes

	Signal or Component								
Mode	**Enable Line Active**	**PLL Synthe-sizer Selected**	**SW2 (U6-14)**	**U3A A11A2 Internal Key Gate**	**U3B FM Audio Gate**	**U3C Output Gate**	**Output Selected**	**U3D FM/ NORM Time Constant Select**	**Charge Pump Filter Resistor Chosen**
All except FM,FSK	Enable 1	U6	0 Vdc	Enabled	Disabled	Disabled	A11A2	Enabled	R22
FM	Enable 1	U6	15 Vdc	Disabled	Enabled	Enabled	A11A1	Disabled	R21
FSK	Enable1	U6	0 Vdc	Enabled	Disabled	Disabled	A11A2	Enabled	R22
	Enable 2	U7	0 Vdc						

NOTE

The following paragraphs apply to any mode except FM or FSK. FM operation will be covered in section 2.2.6 and FSK operation will be covered in section 2.2.7.

2.2.1 PLL Synthesizer Selection and Control

When a mode is selected, buffer U5 supplies common data and clock signals to U6 and U7. Serial data containing the divide-by-N and FM/non-FM mode selection information (from Control Assembly A14) is applied synchronously with the clock signals. This data is stored in registers internal to U6 and U7.

U6 outputs error signals $\varnothing_V$ and $\varnothing_R$ at pins 3 and 4. (Refer to section 2.2.3) These signals, along with pin 8 output, modulus control, are fed to 3PDT IC switch U8. The U8 select lines at pins 9-11 will be at logic zero, selecting the U6 output. $\varnothing_V$ and $\varnothing_R$ will then be passed via driver U9 to the charge pump, and the modulus control will determine the divide by 10/divide-by -11 prescaler U9 division factor.

2.2.2 Reference Generation

U6 (and U7 when selected) requires a stable reference signal to compare against the VCO derived feedback signal. This reference is derived from a 40 MHz signal supplied from Reference Generator Assembly A12 and which is locked to Frequency Standard Assembly A21. The 40 MHz signal at 0 dBm enters the assembly at J4, and is routed to the following:

- A11A1J5 (to be used on PLL 4 Assembly A9)
- Amplifier stage Q1

Q1 feeds -3 dB pad R7-R9, which supplies +7 dBm to the A11A2 assembly and sine-to-square-wave converter stage Q2. Q2 drives counter U1, which supplies 5 MHz (divide by 8) to the A11A2 assembly, and 10 MHz (divide by 4) to be used as the reference input for U6 (or U7). The 10 MHz input at U6, pin 19, is then divided (by the U6 divide-by-1000 counter) to produce the 10 kHz reference signal. F_r will be compared against the VCO derived signal, f_v, at the U6 phase comparator as shown in figure 2.

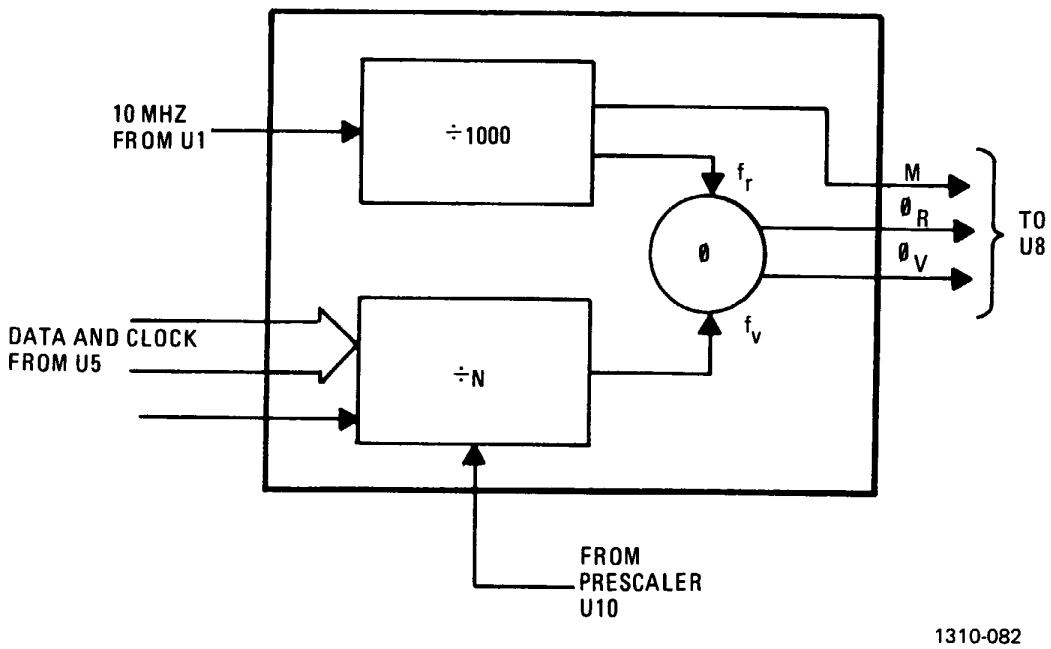


Figure 2. PLL Frequency Synthesizer U6 or U7

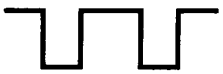
2.2.3 Phase Comparison and Charge Pump Operation

The phase comparator (internal to U6) has two inputs:

- f_r, the 10 kHz reference (paragraph 2.2.2)
- f_v, the VCO derived signal which has been scaled by divide-by-10/divide-by-11 prescaler U10, applied to U6, pin 10, and divided by the U6 divide-by-1000 counter

The U6 phase comparator supplies two outputs, $\emptyset_V$ and $\emptyset_R$, at pins 3 and 4. These signals will sit at 5 Vdc if f_r and f_v are equal in frequency and phase. If f_r and f_v are not equal, then one of the two outputs will pulse low. The pulse width of the signal will be dependent on the amount of error between f_r and f_v. Table 3 lists ØVand ØR values for various input conditions.

Table 3. Phase Comparator Output

Condition	$\varnothing_V$ (U6-3)	$\varnothing_R$ (U6-4)
$f_r = f_v$ (VCO frequency)	5 Vdc	5 Vdc
f_v is less than f_r (VCO frequency too low)	5 Vdc	
f_v is greater than f_r (VCO frequency too high)		5 Vdc

U8 routes $\varnothing_V$ and $\varnothing_R$ to driver/buffer stage U9. U9-C and D function as current sinks for transistors Q4 and Q3 in the charge pump.

If f_v is less than f_r (VCO frequency too low), $\varnothing_R$ pulses low causing U9-D to sink current from Q3 during the low transition. Q3 collector voltage drops, turning Q5 on. Current passed by Q5 charges C22 through switch U3D and R22, since U3D will be on in non-FM modes. This causes buffer Q6 to increase the voltage across R24. This increasing voltage is amplified by operational amplifier stages U2A and U2B and is applied to varactor diodes in the VCO. The VCO will be forced higher in frequency, driving f_v towards f_r. When $f_v = f_r$, $\varnothing_R$ will return to 5 Vdc. Q3 will be turned off causing Q5 to turn off. The new, higher voltage developed across C22 will maintain the VCO at the new, higher frequency.

If f_v is greater than f_r (VCO frequency too high), $\varnothing_V$ pulses low, causing Q4 to turn on and draw charge out of C22. This causes the voltage applied to the VCO diodes to fall, and the VCO frequency will drop. When $f_v = f_r$, $\varnothing_V$ returns to 5 Vdc, turning Q4 off.

2.2.4 VCO Operation and Control

VCO stage Q7 runs from 40-60 MHz. Its output frequency varies as the capacitance of varactor diode string CR5-CR11 varies in response to changes in control voltage from the charge pump. C54 sets the control voltage level at TP5 to 8.0 Vdc for the VCO midband frequency of 50 MHz (PWB output of 500 kHz). Buffer amplifier Q8 feeds the VCO output to two places:

- Divide-by-10/divide-by-11 prescaler U10. The U10 modulus (division factor) is controlled by U6, and will change as a function of the value programmed into the U6. U10 output goes to U6 to complete the feedback loop. After further division by the U6 divide-by-N counter, this signal becomes f_v.

- Divide-by-100 counter U11. (Refer to paragraph 2.2.5.)

2.2.5 Output Circuitry

Divide-by-100 counter U11 outputs a signal between 400 kHz and 600 kHz to J2-20, to be used as the Carrier Generator Assembly A11A2 reference input, and to switch U3C. The U3C control voltage at pin 6 will be 0 Vdc. This gates U3C off, and prevents the signal from reaching Q11.

Buffers Q11 and Q12 form an analog OR gate, passing either U3C output in FM mode or a signal, nominally at 455 kHz, from the A11A2 assembly in all other modes. With U3-C gated off, only the nominal 455 kHz signal (J2-15) from the A11A2 assembly will be passed by Q12.

The buffers feed low pass filter (LPF) network C42-45, L6-7, and R46. The LPF in turn provides the A11A1 455 kHz (nominal) output to the A5 assembly via J6, and to the BITE Detector circuit. (Refer to paragraph 2.2.8.)

2.2.6 FM Operation

When the FM mode is selected, circuit operation functions the same as described in paragraphs 2.2.1 through 2.2.5 except that U6 is loaded with SW2 = + 15 V. This produces the following changes:

- U3B FM audio enable is gated ON, allowing the A5 assembly supplied audio to function as a control voltage for the VCO. A FM signal at the VCO output results.
- U3D FM/NORM time constant select gate opens, selecting R21 instead of R22 to function in the PLL filter network. The net result is a decreasing PLL bandwidth to accommodate the wider frequency variations of the VCO during FM operation.
- U3A A11A2 assembly keyline gate will be disabled, preventing any A11A2 assembly output to Q12. This means that only output from Q11 can be supplied to the LPF.
- U3C A11A1 assembly output gate will be enabled to be closed by the Internal Key line via CR18 and U4A whenever a transmission is to occur. This allows the VCO output to be passed via U11, U3C, and Q11 to the LPF.

2.2.7 FSK Operation

When the FSK mode is selected, circuit operation functions the same as described in paragraphs 2.2.1 through 2.2.5 with the following exceptions:

- Both PLL synthesizer ICs will be used. The U6 divide-by-N counter will be enabled and loaded with a value corresponding to the higher FSK frequency shift, and U7 will be enabled and loaded with a value corresponding to the lower FSK frequency shift.
- FSK keying signals from the exciter rear panel will be supplied via buffer U5 to synthesizer select IC U8. The FSK Key signal at logic 0 will cause U8 to select U6 output (higher tone) while a logic 1 will select U7 (lower tone) for control of the charge pump and VCO.

The A11A1 assembly output at J2-20 will therefore be a signal whose frequency will be equal to 500 kHz ± 100 times the FSK shift selected. This signal functions as a reference for 45 MHz Loop Assembly A11A2, just as the CW 500 kHz signal did for all modes except FM.

Note that the FSK key signal at U5-8 has been processed for a 0 to 5 volt TTL level on System Interface Assembly A18. Typically, this signal would arrive at the exciter rear panel input as a ± 12 Vdc RS-232 signal. A typical FSK keying rate for this assembly would be 150 baud.

2.2.8 BITE

The A11A1 assembly performs the following types of BITE tests:

- Serial data communications validation
- PLL lock status

Both tests are performed whenever the operator chooses to select the BITE mode. These tests are described in detail in the Maintenance section of this manual. Only the hardware aspects of the BITE detectors will be considered here.

The serial data communications test consists of Control Board Assembly A14 writing a specific data bit into U6 and U7 and then reading that bit out. The readback data bit appears at the U6 and U7 SERIAL CHK 1 and SERIAL CHK 2 outputs, respectively. As long as the written and read bits agree, the serial communications capability is functional.

The PLL lock detector functions are performed by the lock detector outputs of PLL ICs U6 (U7) and monitoring c ircuit U4C (U4D). When the loop is locked, U6 (U7) lock detector output at pin 9(9) will be 5 Vdc. U4C-9 (U4D-13) will be at a higher voltage than U4C-10 (U4D-12) and the output, pin 8, (pin 14) will be zero volts. If U6 (U7) unlocks, U6-9 (U7-9) will be at a lower voltage then U4C-10 (U4D-12) and pin 8 (14) will be at + 15 Vdc. Voltage division via R72-R73 (R66-R67) reduces the unlocked voltage at TP4 (TP2) to 1.2 Vdc. Control Assembly A14 would monitor these lock lines, and record a fault during BITE testing if the loop unlocks.

2.3 A11A1 Maintenance

The following VCO alignment procedure should only be performed when a PWB repair requires realigning the PWB. All connections should be in normal contact, unless otherwise stated.

a. Remove 45 MHz Loop Assembly A11A2.

b. Set RF-1310 mode to CW.

c. Monitor TP5 with a digital voltmeter (DVM).

d. Monitor U11, pin 2, with a frequency counter. (Counter should use a high impedance input.)

e. Key exciter.

f. Adjust C54 for 7.5 Vdc at TP5. U11, pin 2, should read 500.000 kHz.

g. Test is now complete. Remove test equipment and reinstall the A11A2 assembly.

2.4 45 MHz Loop Assembly A11A2

The A11A2 45 MHz Loop Assembly provides the following functions:

- 455 kHz CW signal output for all modes except FM and FSK.
- An FSK signal centered at 455 kHz (± 1 kHz maximum) when in FSK mode.

Both functions use a signal supplied by the A11A1 assembly as a reference input to one side of a phase detector on the A11A2 assembly.

2.5 A11A2 Interface Connections

Table 1 lists the various input/output connections at A11A2J1 via A11A1 connector J2. Note that the pin number/name assignments for both connectors are identical.

2.6 A11A2 Circuit Description

The A11A2 assembly uses a PLL similar (in function) to the A11A1 assembly PLL, but without direct divide-by-N programming capability. Most of the circuits on this assembly function to accurately control the VCO stage (Q7). The VCO output is then divided down to provide the signals listed in paragraph 2.4. The error signal generated by mixer U2 is processed and compared to a nominal 500 kHz signal from the A11A1 assembly, at phase detector network U3 and U4. Any difference in phase between these two signals will cause the VCO to shift to whatever frequency is required to reduce the error to zero.

2.6.1 400-600 kHz Error Signal Generation

A 5 MHz TTL signal at J2-12 is filtered and applied to the RF port of mixer U1. A + 7 dBm 40 MHz signal is applied to the U1 LO port. The mixer output at U1, pins 3 and 4, will contain the desired 45 MHz signal plus other mixer products. Q1 provides 8 dB of gain and applies the signals to the RF port of mixer U2. The RF signal is mixed with the 45.5 MHz (-100 kHz) amplified VCO output. The VCO output is input at the mixer LO port with a level of + 7 dBm. The U2 output is passed through a 500 kHz ± 100 kHz bandpass filter before being applied to a sinewave-to-squarewave converter. The sinewave-to-squarewave converter, made up of Q2 and Q3, amplifies and clips the filtered U2 output which generates a square wave. The signal can be observed at TP6. This signal is applied to pin 11 of U3B and functions as the error signal for U3 and U4 phase comparator.

2.6.2 Phase Comparison and Charge Pump Operation

D flip-flops U3A, U3B, and NAND gate U4C function as a phase comparator. U3A, pin 3, receives the reference f_r, a 500 kHz (± 100 kHz, maximum) TTL signal. f_r will be dependent on the mode selected:

- Any mode except FM, FSK: f_r = 500 kHz
- FSK mode: f_r = 500 kHz ± (100) FSK shift frequency selected. Since FSK selection is ± 1 kHz maximum f_r could range from 400-600 kHz.
- FM mode: Do not care what state: the A11A2 assembly is bypassed in FM.

U3B, pin 11, receives error signal f_v described in paragraph 2.6.1.

Assume that f_r (U3A-3) and f_v (U3B-11) are in phase. At the positive transition of f_r and f_v, Q1 (U3A-5) and Q2 (U3B-9) go high. NAND gate U4C-8 goes low, immediately resetting Q1 and Q2 to a low state. Inverter outputs U4B ($\varnothing_R$) and U4D ($\varnothing_V$) remain high, holding charge pump transistors Q4 and Q5 off, and the VCO at a constant frequency.

If f_r and f_v are out of phase then one of the flip-flops (U3A or U3B) will be triggered before the other. The output of the flip-flop that is triggered first will go high, while the output of the other flip-flop will stay low. While this condition exists the output of U4C will remain high so the flip-flop will not reset. Consequently, a low going pulse will be generated at the output of U4B or U4D, depending upon which flip-flop was clocked first. The width of the low going pulse is determined by the phase difference between f_r and f_v. When the

second flip-flop is clocked, both flip-flops will be reset. U4B or U4D sends the error signal to Q4 or Q5 in the Charge Pump circuit. Q4 or Q5 is turned on when the corresponding signal from U4B or U4D is low.

NAND gate inverters U4B and U4D function as current sinks for the charge pump, Q4, Q5, and Q6. Charge pump operation is identical to the charge pump on the A11A1 assembly.

If f_r and f_v are in phase, U4-B ($\varnothing_R$) and U4-D ($\varnothing_V$) are high, Q4-Q6 are off, and the voltage at TP7 is held constant.

If f_v is less than f_r, (VCO frequency too low), $\varnothing_R$ pulses low, Q4 turns on causing Q6 to turn on, and C23 charges, increasing the VCO tuning voltage at TP7. This will cause the VCO frequency to increase until f_v is equal to f_r.

If f_v is greater than f_r, (VCO frequency too high), $\varnothing_V$ pulses low, and Q5 turns on, drawing charge out of C23. This causes the VCO tuning voltage to drop and the VCO frequency will decrease until f_v is equal to f_r.

Table 4 summarizes these conditions.

Table 4. Charge Pump Input Summary

Condition	$\varnothing_V$ (U4-D, pin 11)	$\varnothing_R$ U4-B, pin 6
$f_r = f_v$ (VCO frequency)	5 Vdc	5 Vdc
f_v is less than f_r (VCO frequency low)	5 Vdc	
f_v is greater than f_r (VCO frequency high)		5 Vdc

2.6.3 VCO Operation and Control

VCO stage Q7 is configured as a Hartley oscillator utilizing feedback from transformer T1. The total VCO tuning range is 45.4-45.6 MHz. Varactor diodes CR8 and CR9 change capacitance as the VCO control voltage applied to them varies. Since CR8 and CR9 are in the frequency-determining portion of the VCO, the VCO frequency will also shift. VCO Range Adjust C25 sets the VCO tuning voltage at TP7 to its midvalue of 6.0 Vdc, for a VCO frequency of 45.5 MHz.

Amplifier Q8 and Buffer stage Q9 drive two circuits:

- Mixer U2 LO amplifier stage Q10
- High speed divide by 100 IC U5

Amplifier Q10 boosts the 45.4-45.6 MHz VCO signals and supplies + 10 dBm at TP8. A 3 dB pad then feeds the LO port of mixer U2 to complete the feedback path.

High speed divider U5 provides a TTL signal in the range of 454 to 456 kHz (depending on the mode selected) to the A11A1 assembly. A low pass filter on the A11A1 assembly then converts the signal to a sinusoidal waveform whenever the A11A2 assembly output is selected by logic on the A11A1 assembly (during all modes except FM, and only when a keyline is activated). U5 is disabled by Q11, and Q11 enables U5 only during an active keyline period in the following manner:

- If Internal $\overline{Key}$ = 0 (keyline active) then CR14 turns on, the Q11 base drive returns to ground through R44 and CR14, and Q11 turns on, supplying + 5 Vdc to power U5.
- If Internal $\overline{Key}$ = 1 (keyline inactive), CR14 is off, Q11 remains off, and U5 has no supply voltage and therefore no output.

2.6.4 BITE Circuits

Lock detector Q12 monitors the state of the phase detector output signals ($\varnothing_R$ and $\varnothing_V$). If the signals are in phase, CR2 and CR3 are off, preventing Q12 from conducting. The voltage at TP5 will be 0 Vdc, indicating a locked condition.

If either $\varnothing_R$ or $\varnothing_V$ changes phase, then CR3 or CR2 (respectively) will conduct during the low transition of the error signal pulse. Q12 is turned on, and TP5 rises to 5 Vdc, indicating a fault condition.

Whenever the operator utilizes the exciter BITE mode, this line is tested for a locked condition. Refer to the Maintenance section of the manual for a description of the BITE tests.

2.7 Maintenance

The following VCO alignment procedure should only be performed when a PWB repair requires realigning the PWB. All connections should be in normal contact, unless otherwise stated.

a. Verify that the A11A1Assembly VCO is properly aligned (paragraph 2.3.1).

b. Set RF-1310 mode to CW.

c. Monitor TP7 with a digital voltmeter (DVM).

d. Monitor U5, pin 2, with a frequency counter. (Counter should use a high impedance input.)

e. Key exciter.

f. Adjust C25 for 6.0 Vdc at TP7. U5, pin 2, should read 455.000 kHz.

g. Test is now complete. Remove test equipment.

3. PARTS LISTS, COMPONENT LOCATION, AND SCHEMATIC DIAGRAM

All replaceable components of the A11A1 assembly are listed in table 5. Figure 3 is the A11A1 assembly component location diagram. Figure 4 is the A11A1 assembly schematic diagram.

All replaceable components of the A11A2 assembly are listed in table 6. Figure 5 is the A11A2 assembly component location diagram. Figure 6 is the A11A2 assembly schematic diagram.

Table 5. Carrier Generator Assembly A11A1 Parts List (10121-4610 Rev. R)

Ref. Desig.	Part Number	Description
C1	M39014/02-1298V	CAP .01UF 10% 200V CER-R
C2	M39014/02-1298V	CAP .01UF 10% 200V CER-R
C3	M39014/02-1298V	CAP .01UF 10% 200V CER-R
C4	M39014/02-1298V	CAP .01UF 10% 200V CER-R
C5	M39014/02-1298V	CAP .01UF 10% 200V CER-R
C6	M39014/02-1298V	CAP .01UF 10% 200V CER-R
C7	M39014/02-1298V	CAP .01UF 10% 200V CER-R
C8	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C9	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C10	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C11	C26-0025-100	CAP 10UF 20% 25V TANT
C12	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C13	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C14	C26-0025-100	CAP 10UF 20% 25V TANT
C15	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C16	C26-0025-100	CAP 10UF 20% 25V TANT
C17	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C18	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C19	C26-0025-100	CAP 10UF 20% 25V TANT
C20	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C21	C26-0025-339	CAP 3.3UF 20% 25V TANT
C22	C25-0003-004	CAP 0.33UF 10% 50V TANT
C23	M39014/02-1304V	CAP .039UF 10% 100V CER-R
C24	M39014/01-1317V	CAP,1000PF,10% 200VC
C25	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C26	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C27	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C28	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C29	M39014/01-1317V	CAP,1000PF,10% 200VC
C30	M39014/02-1298V	CAP .01UF 10% 200V CER-R
C31	M39014/02-1298V	CAP .01UF 10% 200V CER-R
C32	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C33	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C34	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C35	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C36	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C37	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C38	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C39	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C40	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C41	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C42	M39014/02-1310V	CAP .1UF 10% 100V CER-R

Table 5. Carrier Generator Assembly A11A1 Parts List (10121-4610 Rev. R) (Cont.)

Ref. Desig.	Part Number	Description
C43	M39014/02-1297V	CAP 8200PF 10% 200V CER-R
C44	M39014/02-1300V	CAP .015UF 10% 100V CER-R
C45	M39014/02-1297V	CAP 8200PF 10% 200V CER-R
C46	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C47	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C48	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C49	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C50	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C51	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C52	M39014/02-1298V	CAP .01UF 10% 200V CER-R
C53	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C54	C85-0005-072	CAP VAR 3.0-10PF CER
C55	M39014/02-1310V	CAP .1UF 10% 100V CER-R
CR1	1N4454	DIODE 200MA 75V SW
CR2	1N4454	DIODE 200MA 75V SW
CR3	1N3064	DIODE 75mA 75V SW
CR4	1N3064	DIODE 75mA 75V SW
CR6	10012-7188	VHF-UHF TUNING DIODE
CR7	10012-7188	VHF-UHF TUNING DIODE
CR8	10012-7188	VHF-UHF TUNING DIODE
CR9	10012-7188	VHF-UHF TUNING DIODE
CR10	10012-7188	VHF-UHF TUNING DIODE
CR12	10012-7188	VHF-UHF TUNING DIODE
CR13	10012-7188	VHF-UHF TUNING DIODE
CR14	10012-7188	VHF-UHF TUNING DIODE
CR15	10012-7188	VHF-UHF TUNING DIODE
CR16	10012-7188	VHF-UHF TUNING DIODE
CR17	1N4454	DIODE 200MA 75V SW
CR18	1N4454	DIODE 200MA 75V SW
CR19	1N4454	DIODE 200MA 75V SW
J1	J46-0022-003	HDR 3 PIN 0.100" SR LKG
J2	J46-0041-020	CONNECTOR
J3	J46-0013-016	HDR 16 PIN 0.100" DR SHRD
J4	J-0031	CONN SMB VERT PCB F
J5	J-0031	CONN SMB VERT PCB F
J6	J-0031	CONN SMB VERT PCB F
L1	MS75084-14	COIL 15.0UH 10% FXD RF
L2	MS75085-13	COIL 330UH 10% FXD RF
L3	MS75084-17	COIL 27.0UH 10% FXD RF
L4	MS75084-10	COIL 6.8UH 10% FXD RF
L5	MS75085-1	COIL 33UH 10% FXD RF
L6	MS75084-17	COIL 27.0UH 10% FXD RF

Table 5. Carrier Generator Assembly A11A1 Parts List (10121-4610 Rev. R) (Cont.)

Ref. Desig.	Part Number	Description
L7	MS75084-17	COIL 27.0UH 10% FXD RF
L8	MS75085-19	COIL 1000UH 10% FXD RF
L9	82027-03	CHOKE WB 50MHZ
L10	MS75084-1	COIL 1.2UH 10% FXD RF
Q1	2N5179	XSTR SS/RF NPN TO-72
Q2	2N2369A	XSTR SS/RF NPN TO-52
Q3	2N2222A	XSTR SS/GP NPN TO-18
Q4	2N2222A	XSTR SS/GP NPN TO-18
Q5	2N2907A	XSTR SS/GP PNP TO-18
Q6	Q25-0005-000	XSTR SS/GP NPN MPSA18
Q7	Q35-0003-000	XSTR N-CH JFET U310
Q8	Q35-0003-000	XSTR N-CH JFET U310
Q9 – Q12	2N2222A	XSTR SS/GP NPN TO-18
R1	R65-0003-681	RES 680 5% 1/4W CAR FILM
R2	R65-0003-242	RES 2.4K 5% 1/4W CAR FILM
R3	R65-0003-101	RES 100 5% 1/4W CAR FILM
R4	R65-0003-471	RES 470 5% 1/4W CAR FILM
R5	R65-0003-399	RES 3.9 5% 1/4W CAR FILM
R6	R65-0003-101	RES 100 5% 1/4W CAR FILM
R7	R65-0003-301	RES 300 5% 1/4W CAR FILM
R8	R65-0003-180	RES 18 5% 1/4W CAR FILM
R9	R65-0003-301	RES 300 5% 1/4W CAR FILM
R10	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R11	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R12	R65-0003-392	RES 3.9K 5% 1/4W CAR FILM
R13	R65-0003-273	RES 27K 5% 1/4W CAR FILM
R14	R65-0003-470	RES 47 5% 1/4W CAR FILM
R15	RN55D1210F	RES 121 1% 1/8W MET FLM
R16	RN55D9091F	RES 9090 1% 1/8W MET FLM
R17, R18	RN55D1210F	RES 121 1% 1/8W MET FLM
R19	RN55D1501F	RES 1500 1% 1/8W MET FLM
R20	RN55D1210F	RES 121 1% 1/8W MET FLM
R21	R65-0003-753	RES 75K 5% 1/4W CAR FILM
R22	R65-0003-471	RES 470 5% 1/4W CAR FILM
R23	RN55D3651F	RES 3650 1% 1/8W MET FLM
R24	R65-0003-272	RES 2.7K 5% 1/4W CAR FILM
R25	R65-0003-392	RES 3.9K 5% 1/4W CAR FILM
R26	R65-0003-182	RES 1.8K 5% 1/4W CAR FILM
R27	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R28	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R29	R65-0003-273	RES 27K 5% 1/4W CAR FILM
R30	R65-0003-222	RES 2.2K 5% 1/4W CAR FILM

Table 5. Carrier Generator Assembly A11A1 Parts List (10121-4610 Rev. R) (Cont.)

Ref. Desig.	Part Number	Description
R31	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R32	R65-0003-512	RES 5.1K 5% 1/4W CAR FILM
R33	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R34	R65-0003-470	RES 47 5% 1/4W CAR FILM
R35	R65-0003-513	RES 51K 5% 1/4W CAR FILM
R36	R65-0003-270	RES 27 5% 1/4W CAR FILM
R37	R65-0003-151	RES 150 5% 1/4W CAR FILM
R38	R65-0003-101	RES 100 5% 1/4W CAR FILM
R39	R65-0003-473	RES 47K 5% 1/4W CAR FILM
R40	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R41	R65-0003-222	RES 2.2K 5% 1/4W CAR FILM
R42	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R43	R65-0003-101	RES 100 5% 1/4W CAR FILM
R44	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R45	R65-0003-222	RES 2.2K 5% 1/4W CAR FILM
R46	R65-0003-510	RES 51 5% 1/4W CAR FILM
R47	R65-0003-511	RES 510 5% 1/4W CAR FILM
R48	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R49	R65-0003-681	RES 680 5% 1/4W CAR FILM
R50	R65-0003-512	RES 5.1K 5% 1/4W CAR FILM
R51	R65-0003-201	RES 200 5% 1/4W CAR FILM
R52	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R53	R65-0003-512	RES 5.1K 5% 1/4W CAR FILM
R54	R65-0003-432	RES 4.3K 5% 1/4W CAR FILM
R55	R65-0003-101	RES 100 5% 1/4W CAR FILM
R56 – R59	R65-0003-473	RES 47K 5% 1/4W CAR FILM
R60	R65-0003-101	RES 100 5% 1/4W CAR FILM
R61	R65-0003-682	RES 6.8K 5% 1/4W CAR FILM
R62	R65-0003-113	RES 11K 5% 1/4W CAR FILM
R63	R65-0003-392	RES 3.9K 5% 1/4W CAR FILM
R64	R65-0003-392	RES 3.9K 5% 1/4W CAR FILM
R65	R65-0003-224	RES 220K 5% 1/4W CAR FILM
R66	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R67	R65-0003-512	RES 5.1K 5% 1/4W CAR FILM
R68	R65-0003-104	RES 100K 5% 1/4W CAR FILM
R69, R70	R65-0003-154	RES 150K 5% 1/4W CAR FILM
R71	R65-0003-224	RES 220K 5% 1/4W CAR FILM
R72	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R73	R65-0003-512	RES 5.1K 5% 1/4W CAR FILM
R74	R65-0003-392	RES 3.9K 5% 1/4W CAR FILM
R75	R65-0003-104	RES 100K 5% 1/4W CAR FILM
R76	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM

Table 5. Carrier Generator Assembly A11A1 Parts List (10121-4610 Rev. R) (Cont.)

Ref. Desig.	Part Number	Description
T1	10073-7003	TRANSFORMER, RF, FIXED
T2	10073-7014	TRANSFORMER, RF, FIXED
TP1	J-0071	TP PWB BRN TOP ACCS .080"
TP2	J-0066	TP PWB RED TOP ACCS .080"
TP3	J-0069	TP PWB ORN TOP ACCS .080"
TP4	J-0070	TP PWB YEL TOP ACCS .080"
TP5	J-0068	TP PWB GRN TOP ACCS .080"
TP6	J-0072	TP PWB BLU TOP ACCS .080"
U1	I03-1000-191	IC 74F191 FAST TTL PLAS
U2	I30-0020-004	IC OP AMP DUAL 2904
U3	I01-0000-253	IC 4066B PLASTIC CMOS
U4	I30-0003-000	IC OP AMP QUAD 324
U5	I01-0000-019	IC 4050B PLASTIC CMOS
U6	I70-0002-001	IC MC145156 SYNTH PLA
U7	I70-0002-001	IC MC145156 SYNTH PLA
U8	I01-0000-252	IC 4053B PLASTIC CMOS
U9	I05-0000-000	IC 74LS00 PLASTIC TTL
U10	I65-0004-001	IC PRESCALER 10/11 12013
U11	I45-0003-000	IC PRESCALER /100 8629
VR1	I11-0001-001	IC VR 7805 +5V 1.5A 4%

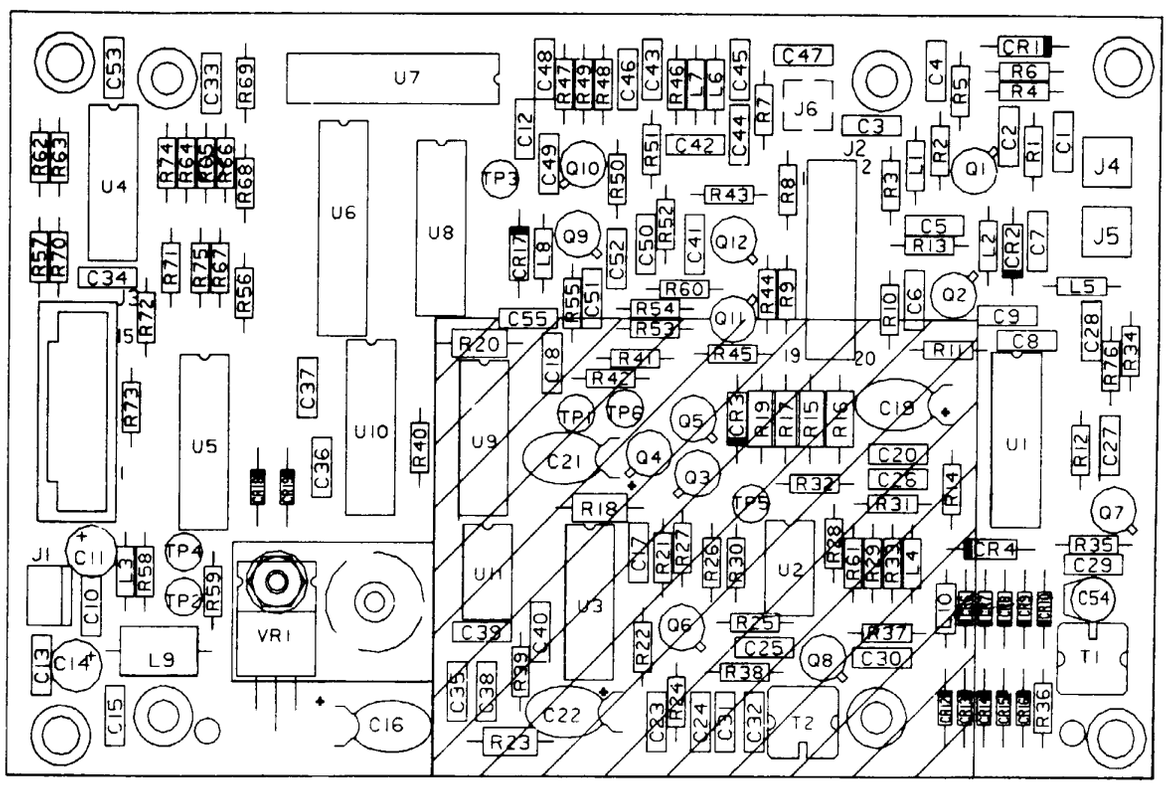


Figure 3. Carrier Generator Assembly A11A1 Component Location Diagram (10121-4610 Rev. F)

NOTE: UNLESS OTHERWISE SPECIFIED:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR A COMPLETE DESIGNATION, PREFIX WITH UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.
2. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, ±5%.
3. ALL CAPACITOR VALUES ARE IN MICROFARADS.
4. VENDOR PART NO. CALLOUTS ARE FOR REFERENCE ONLY. COMPONENTS ARE SUPPLIED PER PART NO. IN PARTS LIST.
5. CR12 MAY BE REMOVED ON SOME ASSY'S TO OBTAIN THE DESIRED FREQUENCY RANGE OF OPERATION.
6. L10 MAY BE REQUIRED ON SOME ASSEMBLIES TO OBTAIN THE DESIRED VCO VOLTAGE RANGE OF OPERATION.

HIGHEST REFERENCE DESIGNATION				
C55	CR13	J6	L9	Q12
R76	T2	U11	VR1	
REFERENCE DESIGNATIONS NOT USED				
CR5	CR11			

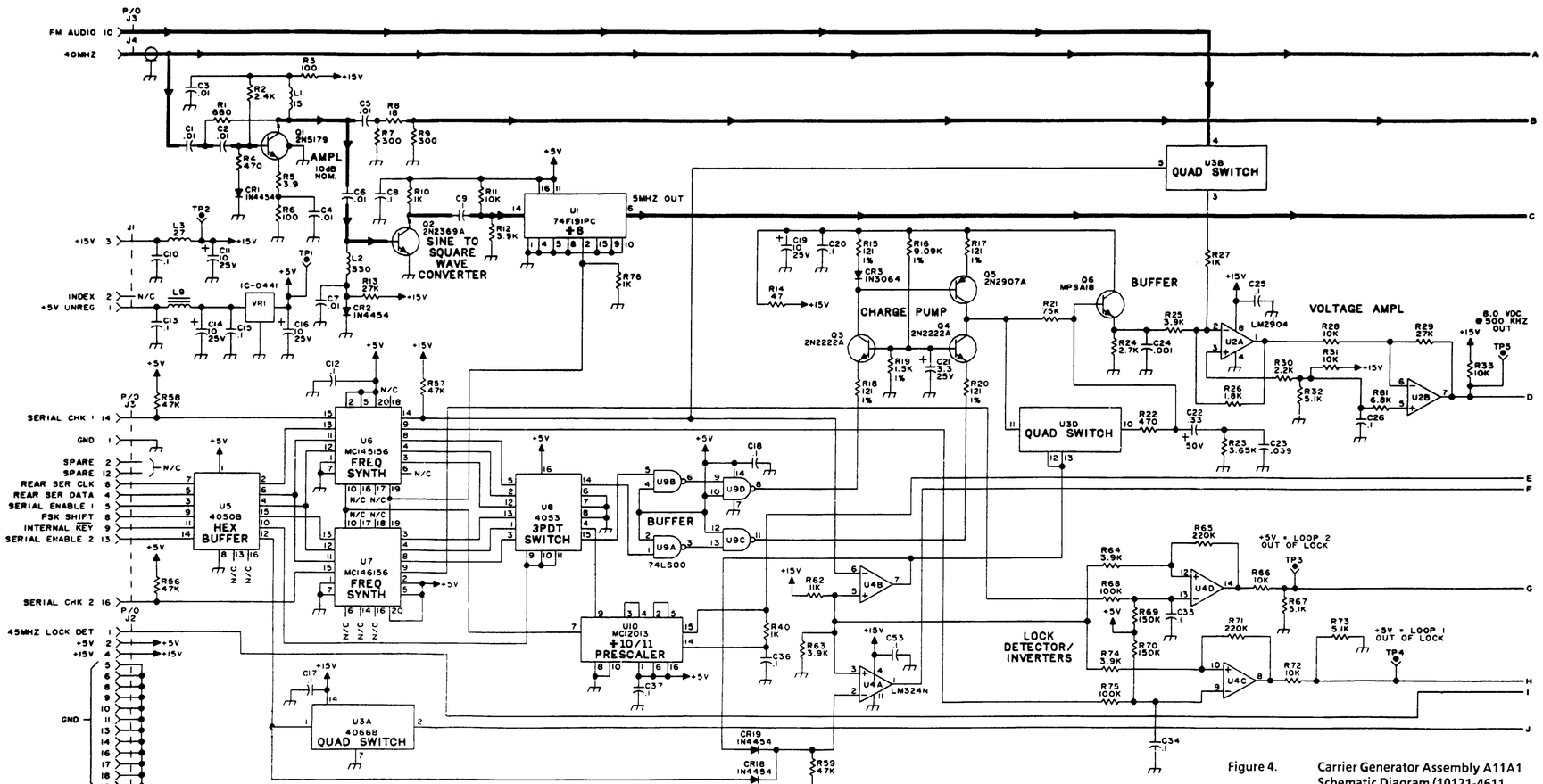


Figure 4. Carrier Generator Assembly A11A1 Schematic Diagram (10121-4611 Rev. G) (Sheet 1 of 2)

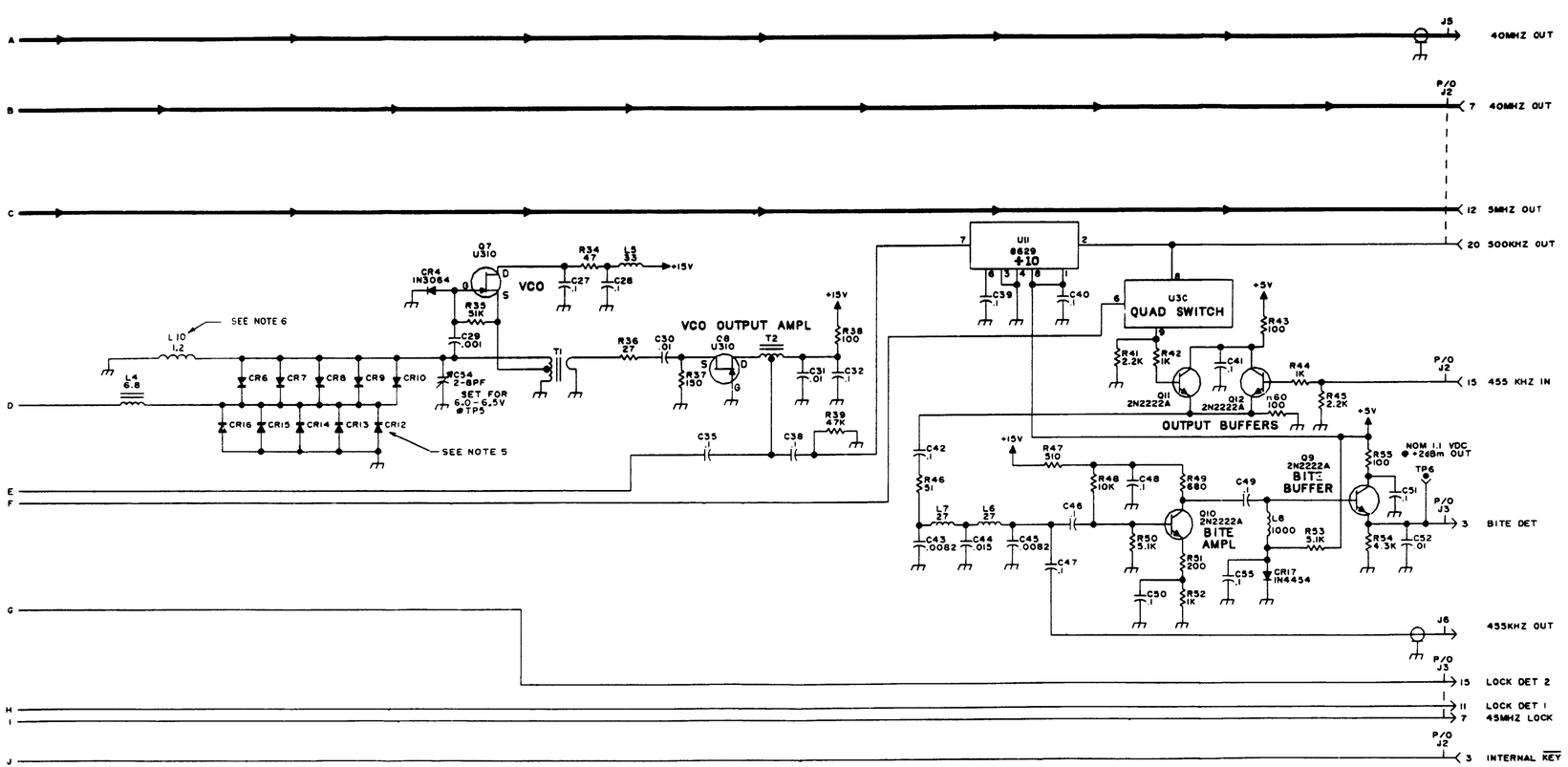


Figure 4. Carrier Generator Assembly A11A1 Schematic Diagram (10121-4611 Rev. G) (Sheet 2 of 2)

Table 6. Carrier Generator Assembly A11A2 Parts List (10121-4650 Rev. K)

Ref. Desig.	Part Number	Description
C1	M39014/01-1316V	CAP 820PF 10% 200V CER-R
C2	M39014/02-1282V	CAP 1500PF 10% 200V CER-R
C3	M39014/01-1316V	CAP 820PF 10% 200V CER-R
C4	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C5	M39014/01-1299V	CAP 100PF 10% 200V CER-R
C6	M39014/02-1298V	CAP .01UF 10% 200V CER-R
C7	CM05CD080D03	CAP 8PF+-.5PF 500V MICA
C8	M39014/01-1281V	CAP 10PF 10% 200V CER-R
C9	M39014/02-1292V	CAP 4700PF 10% 200V CER-R
C10	M39014/02-1295V	CAP 6800PF 10% 200V CER-R
C11 – C14	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C15	C26-0025-339	CAP 3.3UF 20% 25V TANT
C16	M39014/01-1317V	CAP,1000PF,10% 200VC
C17	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C18	C26-0025-339	CAP 3.3UF 20% 25V TANT
C19	M39014/02-1298V	CAP .01UF 10% 200V CER-R
C20	C26-0025-339	CAP 3.3UF 20% 25V TANT
C21	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C22	C26-0025-339	CAP 3.3UF 20% 25V TANT
C23	M39014/02-1320V	CAP .47UF 10% 50V CER-R
C24	M39014/01-1317V	CAP,1000PF,10% 200VC
C25	C85-0005-072	CAP VAR 3.0-10PF CER
C26	M39014/01-1317V	CAP,1000PF,10% 200VC
C27	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C28	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C29	M39014/02-1298V	CAP .01UF 10% 200V CER-R
C30	M39014/02-1298V	CAP .01UF 10% 200V CER-R
C31	M39014/02-1298V	CAP .01UF 10% 200V CER-R
C32	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C33	M39014/02-1298V	CAP .01UF 10% 200V CER-R
C34	M39014/02-1298V	CAP .01UF 10% 200V CER-R
C35	M39014/02-1298V	CAP .01UF 10% 200V CER-R
C36 – C40	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C42	M39014/02-1298V	CAP .01UF 10% 200V CER-R
C43	CM05ED390G03	CAP 39PF 2% 500V MICA
C44	10121-4720	CAP, CER 10PF N750
CR2	1N4454	DIODE 200MA 75V SW
CR3	1N4454	DIODE 200MA 75V SW
CR4	1N6263	DIODE .40W 60V HOT CARR
CR8	CR-0080	VARACTOR 6.1 - 7.5pF
CR9	CR-0080	VARACTOR 6.1 - 7.5pF

Table 6. Carrier Generator Assembly A11A2 Parts List (10121-4650 Rev. K) (Cont.)

Ref. Desig.	Part Number	Description
CR13	1N4454	DIODE 200MA 75V SW
CR14	1N4454	DIODE 200MA 75V SW
CR15	1N3064	DIODE 75mA 75V SW
CR16	1N3064	DIODE 75mA 75V SW
J1	J46-0040-020	RECEPTACLE 20 PIN
L1	MS75084-5	COIL 2.7UH 10% FXD RF
L2	MS75084-5	COIL 2.7UH 10% FXD RF
L3	MS75083-7	COIL .33UH 10% FXD RF
L4	MS75083-11	COIL .68UH 10% FXD RF
L5	MS75084-13	COIL 12UH 10% FXD RF
L6	MS75084-11	COIL 8.2UH 10% FXD RF
L7	MS75085-13	COIL 330UH 10% FXD RF
L8	MS75084-10	COIL 6.8UH 10% FXD RF
L9	MS75085-7	COIL 100UH 10% FXD RF
L10	MS75084-3	COIL 1.8UH 10% FXD RF
L11	MS75084-14	COIL 15.0UH 10% FXD RF
Q1	Q35-0003-000	XSTR N-CH JFET U310
Q2	2N4208	XSTR SS/GP PNP TO-18
Q3	2N2369A	XSTR SS/RF NPN TO-52
Q4	2N2369A	XSTR SS/RF NPN TO-52
Q5	2N2369A	XSTR SS/RF NPN TO-52
Q6	2N4208	XSTR SS/GP PNP TO-18
Q7	Q35-0003-000	XSTR N-CH JFET U310
Q8	2N2369A	XSTR SS/RF NPN TO-52
Q9	Q35-0003-000	XSTR N-CH JFET U310
Q10	2N5179	XSTR SS/RF NPN TO-72
Q11	2N2907A	XSTR SS/GP PNP TO-18
Q12	2N2907A	XSTR SS/GP PNP TO-18
R1	R65-0003-181	RES 180 5% 1/4W CAR FILM
R2	R65-0003-510	RES 51 5% 1/4W CAR FILM
R3	R65-0003-510	RES 51 5% 1/4W CAR FILM
R4	R65-0003-562	RES 5.6K 5% 1/4W CAR FILM
R5	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R6	R65-0003-241	RES 240 5% 1/4W CAR FILM
R7	R65-0003-150	RES 15 5% 1/4W CAR FILM
R8	R65-0003-331	RES 330 5% 1/4W CAR FILM
R9	R65-0003-332	RES 3.3K 5% 1/4W CAR FILM
R10	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R11	RN55D4990F	RES 499 1% 1/8W MET FLM
R12	RN55D4990F	RES 499 1% 1/8W MET FLM
R13	RN55D4990F	RES 499 1% 1/8W MET FLM

Table 6. Carrier Generator Assembly A11A2 Parts List (10121-4650 Rev. K) (Cont.)

Ref. Desig.	Part Number	Description
R14	RN55D4990F	RES 499 1% 1/8W MET FLM
R15	RN55D2002F	RES 20.0K 1% 1/8W MET FLM
R16	R65-0003-332	RES 3.3K 5% 1/4W CAR FILM
R17	RN55D1821F	RES 1820 1% 1/8W MET FLM
R18	R65-0003-332	RES 3.3K 5% 1/4W CAR FILM
R19	R65-0003-101	RES 100 5% 1/4W CAR FILM
R20	R65-0003-511	RES 510 5% 1/4W CAR FILM
R21	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R22	R65-0003-470	RES 47 5% 1/4W CAR FILM
R23	R65-0003-513	RES 51K 5% 1/4W CAR FILM
R24	R65-0003-101	RES 100 5% 1/4W CAR FILM
R25	R65-0003-201	RES 200 5% 1/4W CAR FILM
R26	R65-0003-152	RES 1.5K 5% 1/4W CAR FILM
R27	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R28	R65-0003-100	RES 10 5% 1/4W CAR FILM
R29	R65-0003-151	RES 150 5% 1/4W CAR FILM
R30	R65-0003-221	RES 220 5% 1/4W CAR FILM
R31	R65-0003-513	RES 51K 5% 1/4W CAR FILM
R32	R65-0003-270	RES 27 5% 1/4W CAR FILM
R33	R65-0003-201	RES 200 5% 1/4W CAR FILM
R34	R65-0003-101	RES 100 5% 1/4W CAR FILM
R35	R65-0003-242	RES 2.4K 5% 1/4W CAR FILM
R36	R65-0003-681	RES 680 5% 1/4W CAR FILM
R37	R65-0003-471	RES 470 5% 1/4W CAR FILM
R38	R65-0003-399	RES 3.9 5% 1/4W CAR FILM
R39	R65-0003-101	RES 100 5% 1/4W CAR FILM
R40	R65-0003-301	RES 300 5% 1/4W CAR FILM
R41	R65-0003-180	RES 18 5% 1/4W CAR FILM
R42	R65-0003-301	RES 300 5% 1/4W CAR FILM
R43	R65-0003-473	RES 47K 5% 1/4W CAR FILM
R44	R65-0003-202	RES 2.0K 5% 1/4W CAR FILM
R45	R65-0003-203	RES 20K 5% 1/4W CAR FILM
R46	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R47	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R48	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R49	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
T1	10121-7006	TRANSFORMER, RF, FIXED
TP1	J-0071	TP PWB BRN TOP ACCS .080"
TP2	J-0066	TP PWB RED TOP ACCS .080"
TP3	J-0069	TP PWB ORN TOP ACCS .080"

Table 6. Carrier Generator Assembly A11A2 Parts List (10121-4650 Rev. K) (Cont.)

Ref. Desig.	Part Number	Description
TP4	J-0070	TP PWB YEL TOP ACCS .080"
TP5	J-0068	TP PWB GRN TOP ACCS .080"
TP6	J-0072	TP PWB BLU TOP ACCS .080"
TP7	J-0073	TP PWB VIO TOP ACCS .080"
TP8	J-0074	TP PWB GRA TOP ACCS .080"
U1	I51-0003-001	MIXER DB SBL-1
U2	I51-0003-001	MIXER DB SBL-1
U3	I05-0000-074	IC 74LS74A PLASTIC TTL
U4	I05-0000-000	IC 74LS00 PLASTIC TTL
U5	I45-0003-000	IC PRESCALER /100 8629

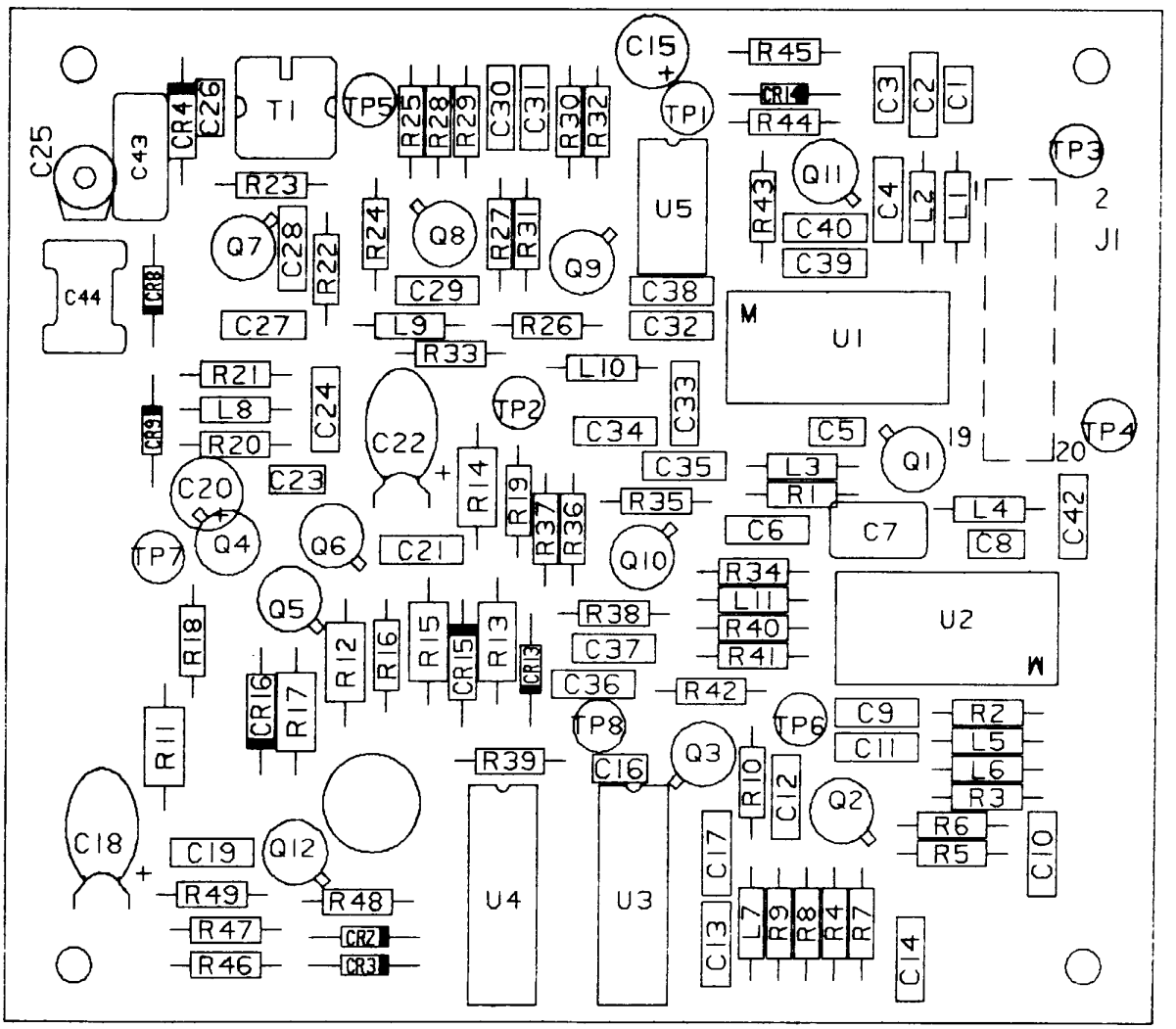


Figure 5. Carrier Generator Assembly A11A2 Component Locations Diagram (10121-4650 Rev. D)

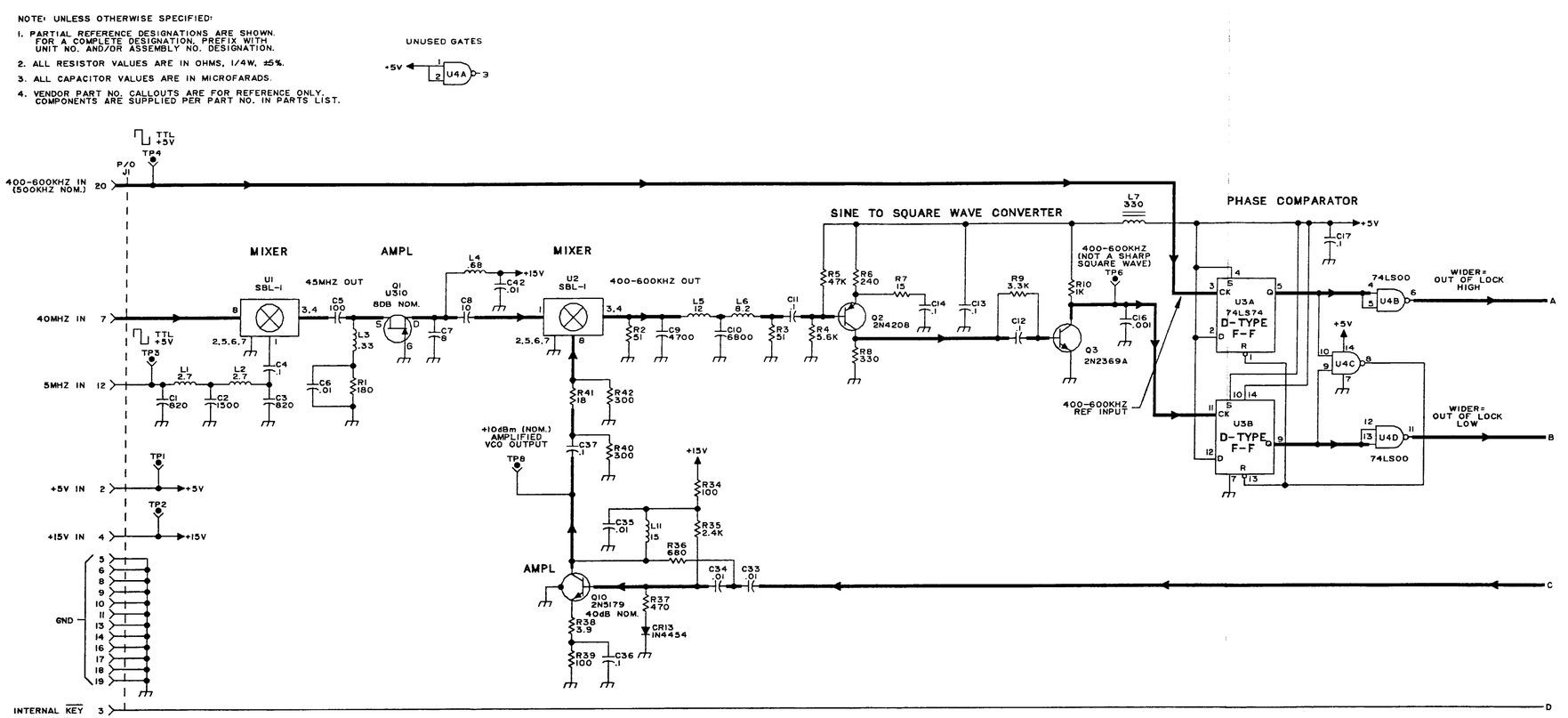
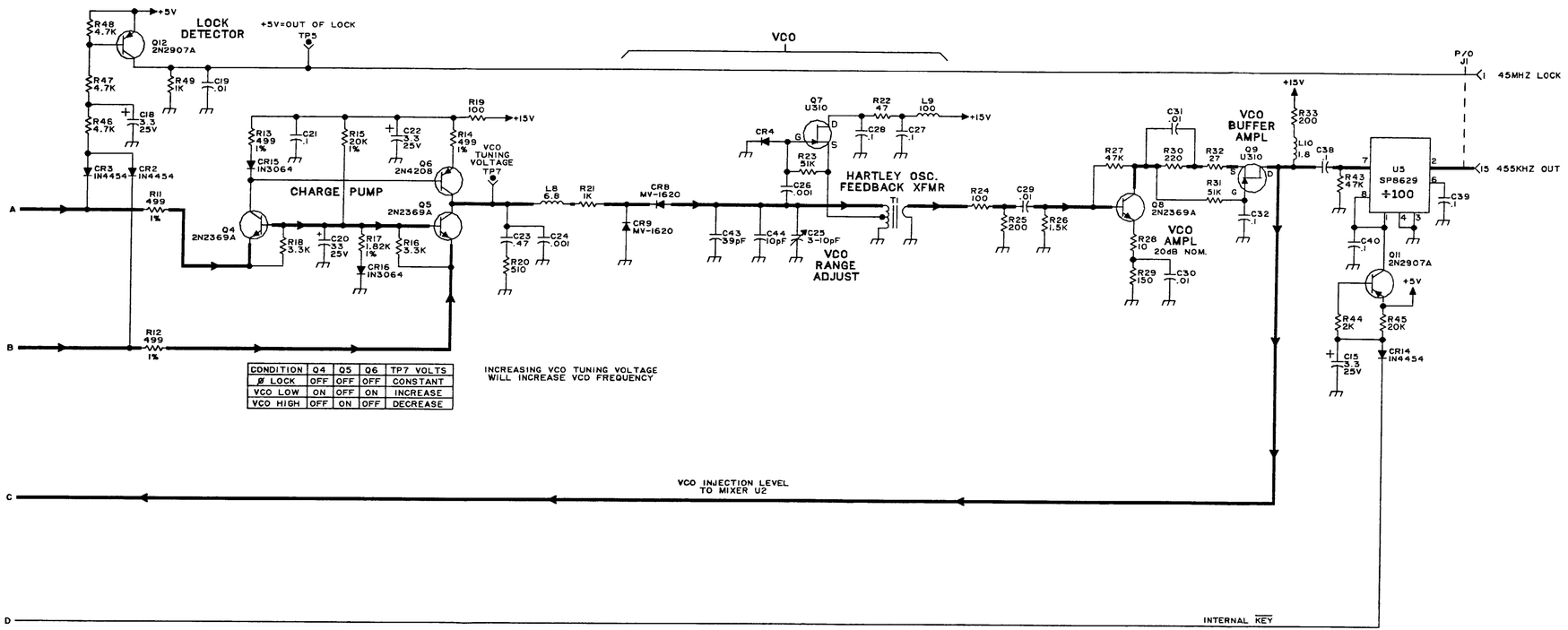


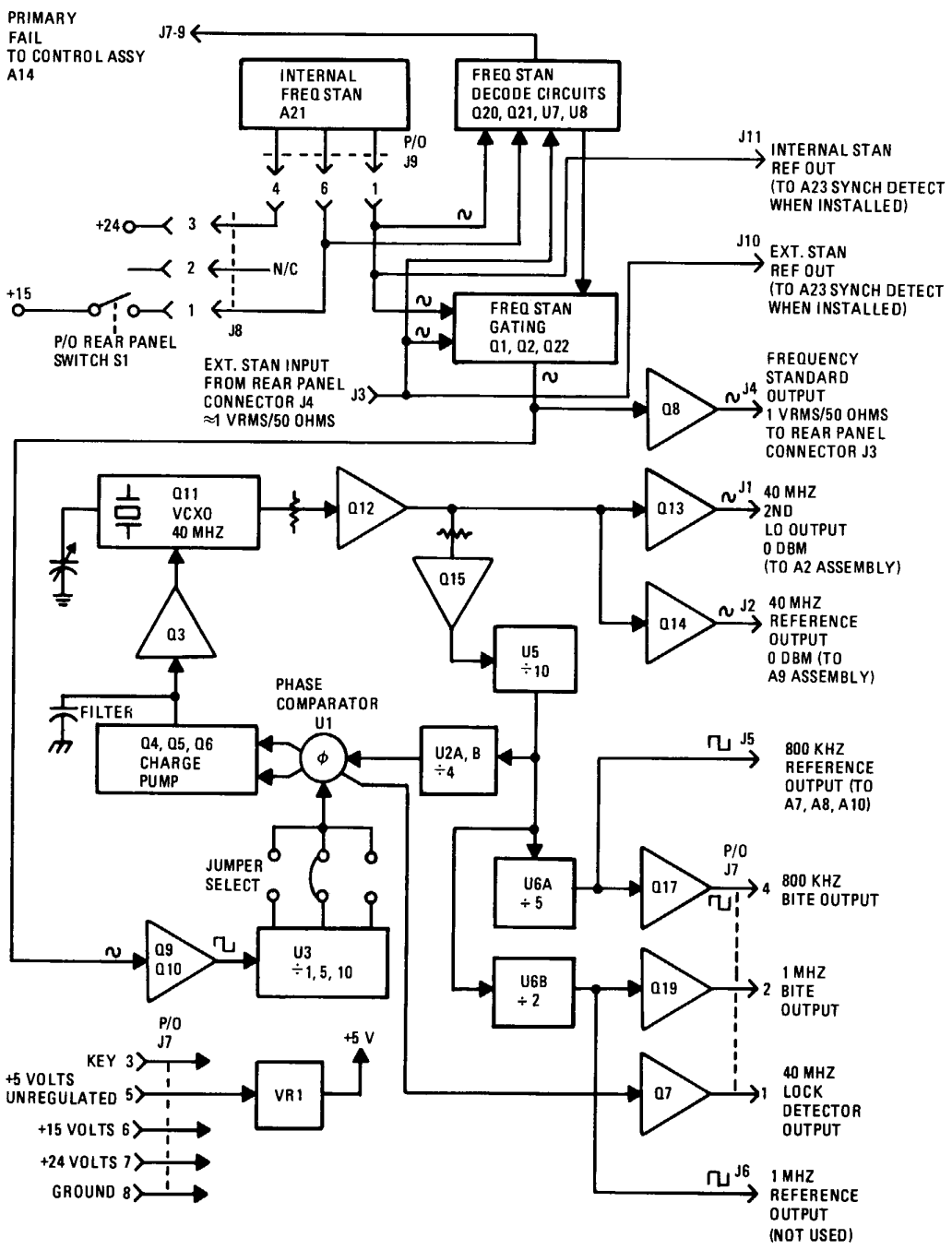
Figure 6. Carrier Generator Assembly A11A2 Schematic Diagram (10121-4651 Rev. E) (Sheet 1 of 2)



CONDITION	Q4	Q5	Q6	TP7 VOLTS
Ø LOCK	OFF	OFF	OFF	CONSTANT
VCO LOW	ON	OFF	ON	INCREASE
VCO HIGH	OFF	ON	OFF	DECREASE

Figure 6. Carrier Generator Assembly A11A2 Schematic Diagram (10121-4651 Rev. E) (Sheet 2 of 2)

A12/A21
REFERENCE GENERATOR AND FREQUENCY STANDARD ASSEMBLIES



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REFERENCE GENERATOR

AND FREQUENCY STANDARD ASSEMBLIES A12/A21

1. GENERAL DESCRIPTION

Reference Generator Assembly A12, shown in figure 1, contains a 40 MHz phase locked loop (PLL) circuit, locked to either:

- An internal standard, supplied with the exciter
- An external standard, supplied by the operator

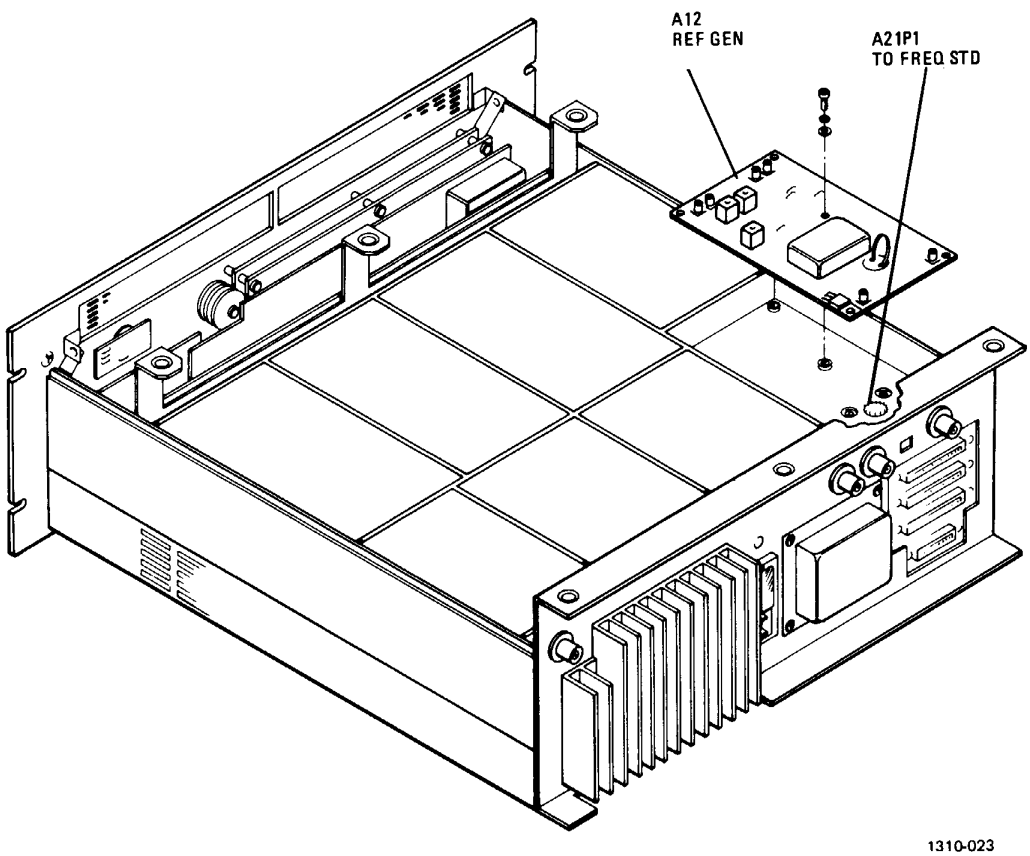


Figure 1. Reference Generator Assembly A12/Frequency Standard Assembly A21 Location

All reference signals required to tune the exciter are then derived from this assembly. These signals are:

- 40 MHz, 0 dBm to Converter Assembly A2
- 40 MHz, 0 dBm to PLL 4 Assembly A9

- 800 kHz, TTL to PLL 2 Assembly A7
- 800 kHz TTL to PLL 3 Assembly A8
- 800 kHz, TTL to PLL 5 Assembly A10

Frequency standard selection is accomplished by rear panel INT/EXT standard select switch S1. An external standard input connector (J4 on rear panel) allows for a 50-ohm, 0.5 to 1 V_{rms} external standard input. Rear panel connector J3 provides a buffered 50-ohm, 0.5 to 1 V_{rms} signal derived from the standard selected.

The standard selected by the INT/EXT switch S1 is referred to as the primary standard. The standard not selected (if connected) is referred to as the secondary standard. Automatic switchover from primary to secondary standards occurs in the event of a primary failure.

Note that both standards must be the same frequency. A jumper connection on this assembly allows either 1, 5, or 10 MHz standards to be used.

Internal Frequency Standard Assembly A21 (supplied with the exciter) is a self-contained, sealed unit which plugs directly into the A12 assembly via nine-pin connector J9. To remove the A21 assembly:

a. Remove the A12 assembly (five mounting screws).

b. Pull the A12 assembly away from the chassis using the loop provided on the assembly.

c. Remove the four mounting nuts that hold the A21 assembly to the chassis.

2. INTERFACE CONNECTIONS

Table 1 details the A12 input/output connections and other relevant data.

Table 1. Reference Generator A12 Interface Connection

Connector	Function	Characteristics
J1	Second LO Output	40 MHz, 0 dBm, 50 ohms
J2	40 MHz Reference	40 MHz, 0 dBm, 50 ohms
J3	External Standard Input	Approximately 1 V_{rms}, 50 ohms
J4	Primary Standard Output	Approximately 1 V_{rms}, 50 ohms
J5	800 kHz Reference Output	TTL
J6	1 MHz Reference Output	TTL
J7-1	40 MHz Lock Detector Output	+ 5 V = failure
J7-2	1 MHz BITE Output	+ 5 V = failure
J7-3	Spare	
J7-4	800 kHz BITE Output	+ 5 V = failure

Table 1. Reference Generator A12 Interface Connection (Cont.)

Connector	Function	Characteristics
J7-5	+ 5 Volts Unregulated	200 mA
J7-6	+ 15 Volts	30 mA
J7-7	+ 24 Volts	10 mA
J7-8	Ground	
J7-9	Primary Failure	+ 5 V = failure
J8-1	1) INT/EXT Standard Select 2) VCXO power	+ 15 V = Internal Standard. Also provides power for nonovenized internal frequency standard options.
J8-2	Index	
J8-3	A21 XTAL Oven Power	+ 24 (provides up to 300 mA; depends upon internal frequency standard option installed.)
J9-1	Frequency Standard A21 Output	0.5 V_{rms}, 1, 5, or 10 MHz
J9-2, 3	Ground	
J9-4	Same as J8-3	
J9-5	Ground	
J9-6	Same as J8-1	
J9-7, 8, 9	Ground	
J10	External Standard Ref Output	Used by A23 (Freq. Stan. Sync. Detector) when installed.
J11	Internal Standard Ref Output	Used by A23 (Freq. Stan. Sync. Detector) when installed.

3. CIRCUIT DESCRIPTION

Voltage controlled crystal oscillator (VCXO) stage Q11 free runs at 40 MHz and provides all the outputs listed in section 1 after the required buffering and frequency division. The VCXO acquires its stability by providing a 1 MHz IF signal to one port of phase comparator U1 where phase comparison of the 1 MHz reference signal derived from the frequency standard occurs. Any difference in phase or frequency between these two signals produces an error signal from the phase comparator which causes the VCXO to tune in the direction which will reduce the error. In so doing, the VCXO frequency of 40 MHz acquires the stability and accuracy of the much lower frequency supplied by the frequency standard.

3.1 Frequency Standard Assembly A21

The frequency standard supplied with the exciter is a self-contained, sealed unit which plugs directly into A12 connector J9. The following frequency standards are available:

- 1 ppm stability, 5 MHz, part number; 10073-6600
- 0.1 ppm stability, 5 MHz, part number; 10073-6700
- 0.01 ppm stability, 1 MHz, part number; 0759-3906

Reference Generator Assembly connector J9 is a nine pin socket. It provides power (+ 24 V and + 15 V) and RF output connections.

3.2 Primary/Secondary Frequency Standard Switchover Circuitry

Automatic switchover is provided from the internal standard to an external standard (and vice versa) in the event of a failure of the standard selected. A simplified block diagram of this function is provided in figure 2.

Signal detectors Q21 and Q20 monitor the internal standard and external standard signal lines, respectively, and produce a dc signal if the signals are present. Comparators U7-D and U7-B monitor the detector outputs, and produce a + 15 V output if their signal input has sufficient amplitude.

U8-D, U8-B, and U7-A perform decode functions to route the frequency standard signals through gates Q1 and Q2. This routing depends on the position of internal/external (INT/EXT) standard select switch S1 and the state of the two signal sources. The selected signal is fed to two places:

a. RF amplifier Q9, which boosts the signal level and feeds driver Q10. Q10 output is a square wave at the selected standard frequency. Phase Comparator U1 requires a 1 MHz signal, so divider U3 provides divide-by-5 and divide-by-10 factors if the frequency standard is 5 or 10 MHz, respectively. A jumper field at the U3 output allows selection for the frequency in use.

b. RF output amplifier Q8, which boosts the level to approximately 1 V_{rms} and feeds rear panel connector J3. This signal is a buffered version of the selected frequency standard, to be used by the operator (if needed) for auxiliary purposes.

The primary failure line output at J7-9 is normally 0 Vdc if the primary standard is functional. If the selected standard should fail, this line will go high (5 V) to indicate primary failure, and the decode logic will automatically switch over to the designated secondary standard. Table A on page 1 of the schematic lists the signal provided at the divider U3 input, and the primary failure status, as a function of:

- The position of the INT/EXT standard select switch
- The status of the frequency standards connected

If both an external and an internal standard are connected, and the INT/EXT switch S1 is set for internal (making the internal standard primary), operation occurs as follows:

a. Q20 and Q21 outputs will be a positive voltage, greater than + 0.2 Vdc. U7-D and U7-B outputs will therefore be + 15 V.

b. Exclusive OR gate U8-D output will be low.

c. + 15 V will be applied to both inputs of U8-B, from INT/EXT standard switch S1, (indicating internal standard selected) and the U7-B output. Exclusive OR gate U8-B output will therefore be low (0 Vdc), causing comparator U8-A output to be high (+ 15 V).

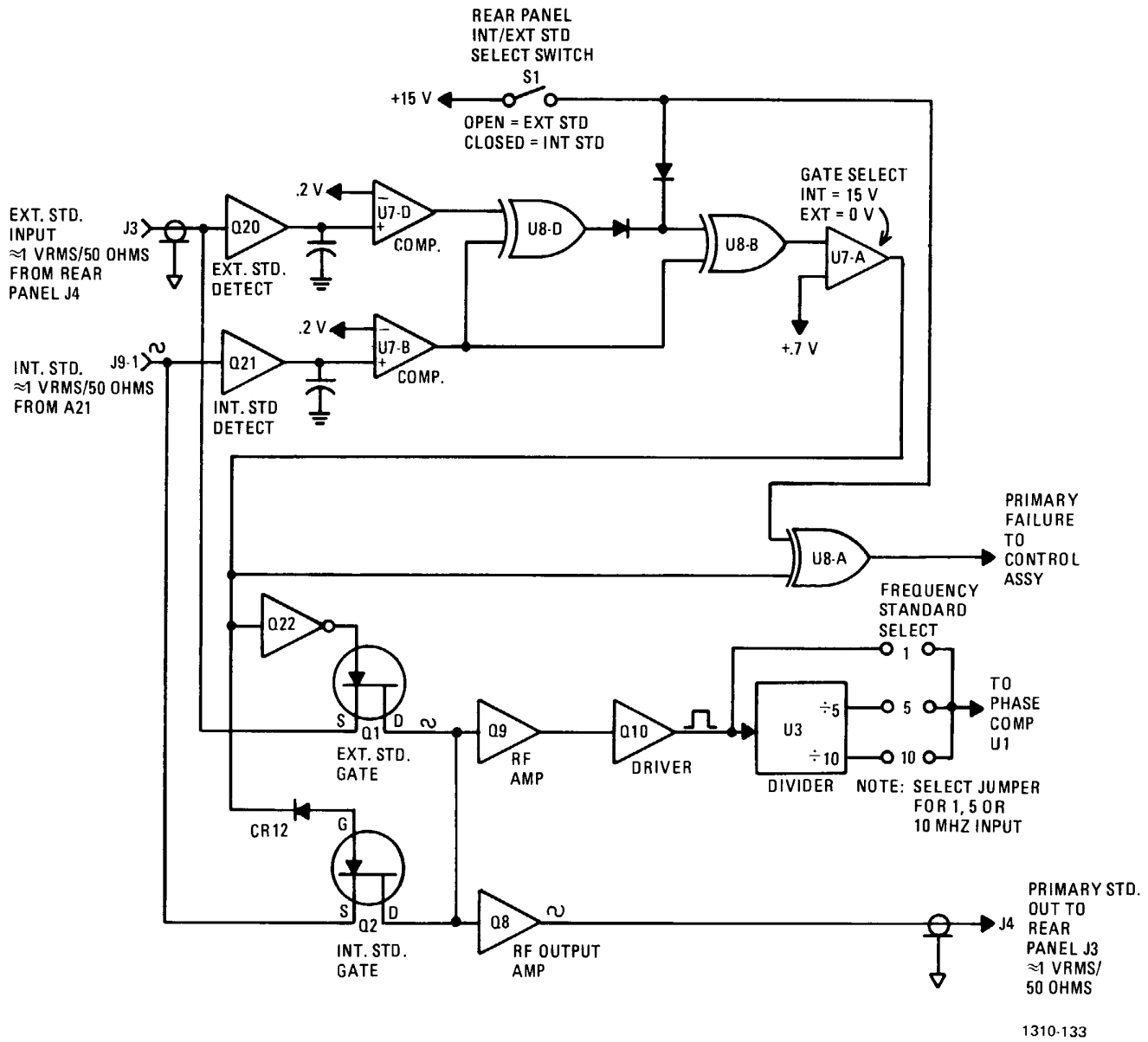


Figure 2. Frequency Standard Switchover Circuit Simplified Block Diagram

d. U7-A output at + 15 V reverse biases CR12 to cause the Q2 gate to be 6 Vdc. Q2 is biased for maximum channel conduction, and passes the internal standard signal to Q9 and Q8. Q9 drives Q10, which produces a square wave at the standard frequency. Q10 is divided by U3 (if necessary) prior to application to phase comparator U1 reference input.

e. U7-A output at + 15 V turns on Q22, which pulls the Q1 gate to approximately 0 Vdc. This causes Q1 to turn off, and the external standard signal is blocked.

f. Since both inputs of exclusive OR gate U8-A are + 15 V, the primary failure output will be 0 Vdc, indicating no failure.

If the internal standard fails:

a. The Q21 output is 0 V, and U7-B output goes to 0 Vdc.

b. U8-D output goes high.

c. Since both inputs of U8-B are different, U8-B output is high, and U7-A output goes low.

d. U7-A output at 0 Vdc forward biases CR12, pulling Q2 gate low, and turns Q2 off. No internal standard signal can now pass.

e. Q22 will turn off, placing Q1 gate at + 6 V. Q1 will pass external standard signal to Q8 and Q9.

f. Since U8-A inputs are different, the primary failure line will go to + 5 Vdc, which will be read as a failure during the BITE test.

3.3 Phase Comparison Circuits

Phase comparator U1 compares the frequency standard derived 1 MHz reference signal to a VCO derived 1 MHz IF signal. When these two signals are equal in frequency and phase, U1 outputs at TP2 and TP3 are essentially 5 Vdc. This holds all transistors in the charge pump circuit (Q4, Q5, Q6) off. The dc voltage across C16 is constant, Q3 is conducting, and the control voltage developed across R13 at TP1 is constant. This holds the VCO frequency constant and equal to a multiple of the frequency standard.

If the VCO frequency decreases due to temperature variations, this causes the 1 MHz IF frequency to decrease. Comparison at U1, pins 1 and 3, causes TP2 to pulse low, and turns on Q6 since the Q6 base-emitter circuit is now forward biased. Q5 remains off. Q6 collector voltage drops and forward biases the Q4 base-emitter junction turning Q4 on. Q4 now starts charging C16, raising the C16 potential. This in turn causes Q3 to conduct more current, and the control voltage developed across R13 at TP1 increases. As the control voltage increases, the VCO frequency increases until the IF frequency is again equal to the reference frequency at the U1 inputs. At this point, TP2 switches to + 5 Vdc and equilibrium is obtained. C16 holds this higher dc level to maintain the new higher VCO frequency.

If that the VCO frequency increases, this causes the 1-MHz IF frequency to increase. Comparison at U1, pins 1 and 3, causes TP3 to pulse low, and biases Q5 on. (Q6 and Q4 remain off.) C16 now has a low impedance discharge path. This drops its voltage. This causes Q3 to conduct less, and less control voltage is developed across R13. As this voltage decreases, the VCO frequency decreases until the inputs at U1 are again equal in frequency and phase. At this point, TP3 switches to + 5 Vdc and equilibrium is obtained. C16 holds this lower dc level to maintain the new lower VCO frequency.

3.4 VCXO Operation and Control

A charge pump circuit consisting of Q4, Q5, and Q6 in conjunction with filter network C16, C17, and R14 converts the two phase-comparator outputs into an analog dc control voltage. Buffer amplifier Q3 applies this control voltage to varactor diodes CR7 and CR8 in the VCXO. As the capacitance of these diodes change due to control voltage fluctuations, JFET oscillator stage Q11 shifts in frequency. This stage is crystal controlled by Y1 and operates at a nominal frequency of 40.000000 MHz. VCXO output passes through amplifier stages Q12, Q15, and into divide-by-10 counter U5. The 4-MHz signal from U5 is applied to divide-by-4 counter U2 which applies a 1-MHz signal to the second port (pin 3) of phase comparator U1 to complete the feedback loop.

U2A provides a 2-MHz output to divide-by-2 counter U6B. The 1-MHz output of U6B is fed through J6 to function as a reference for options which require a 1-MHz TTL signals.

3.5 A12 Reference Generator Outputs

The 40.000000-MHz signal from amplifier stage Q12 is amplified to 0 dBm by Q13 and applied through J1 to Converter Assembly A2 mixer U1 where it functions as a second local oscillator (LO) for the exciter.

Q12 also feeds amplifier stage Q14 which routes a 40.000000 MHz, 0 dBm signal to PLL 4 Assembly A9 mixer U1 as an LO injection.

The 4-MHz signal from divider U5 is applied to divide-by-5 counter U6A. U6 TTL output at 800 kHz is fed through J5 to function as a reference signal for phase comparators on the A7, A8, and A10 assemblies.

3.6 BITE Circuits

Q7 monitors the U1 phase comparator outputs. If either output goes low and remains low for a period of time exceeding the time constant of R19-C19, one of the two diodes (CR5 or CR6) will conduct. This turns Q7 on and develops a + 5 Vdc level indicating an out of lock condition. This immediately flags the BITE monitoring circuits on Control Board Assembly A14 to display a front panel fault light indicator.

The 800-kHz TTL signal from U6A feeds detector stage Q17, and the 1-MHz TTL signal from U6B feeds detector stage Q19. Both of these detectors provide a 0 Vdc level when the 800-kHz and 1-MHz reference signals are present, and a + 5 Vdc level when they are not. These two signals are checked only when the BITE self-test is actuated.

4. MAINTENANCE

The following adjustments should not be performed as a routine maintenance procedure, but only when a failure indicates a definite need. Perform all tests with all connections in normal contact unless otherwise specified. It is assumed that the rest of the exciter is functional.

4.1 40 MHz Outputs Adjustment

Perform the following procedure to adjust the 40 MHz outputs.

a. Connect equipment as shown in figure 3.

b. Set INT/EXT standard select switch to the INT position.

c. Monitor J1 and adjust T3 and then T4 for a peak indication at 40 MHz (approximately 0 dBm).

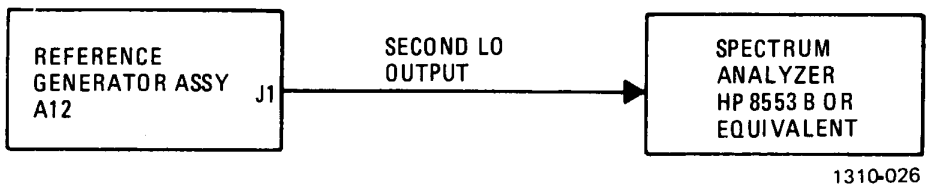


Figure 3. 40 MHz Outputs Adjustment

d. Monitor J2 and adjust T5 for a peak indication at 40 MHz. (Approximately 0 dBm). The test is now complete. Reconnect J1 and J2.

4.2 A21 Frequency Standard Adjustment

a. Connect equipment as shown in figure 4. Set INT/EXT standard switch to the INT position.

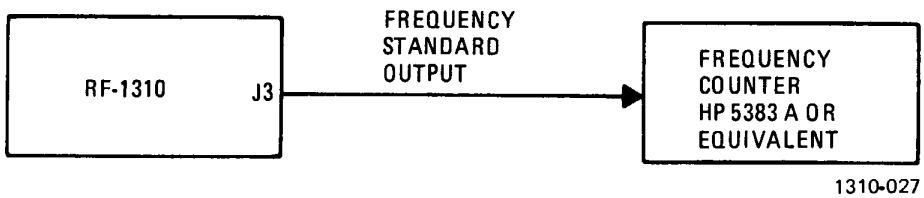


Figure 4. A21 Frequency Standard Adjustment

NOTE

The exciter should be on for at least 24 hours prior to this alignment. The frequency selection jumper field should be set for the frequency of the internal standard (1, 5, or 10 MHz).

b. Remove the screw on top of the A21 assembly to gain access to the frequency adjustment. Adjust this control (using a nonmetallic alignment tool) to the frequency stamped on top of the assembly. (The accuracy of this setting is crucial to the VCO adjustment, so perform this test carefully.)

c. The test is complete. Replace screw in A21 assembly.

4.3 VCO Adjustment

Perform the following procedure to adjust the VCO.

a. Make sure that the INT/EXT standard switch is in the INT position and that the A21 frequency standard is properly adjusted on frequency.

b. Remove the shield can over the VCO circuitry. Monitor TP1 with a digital voltmeter. Adjust C36 for 8.0 Vdc. Replace shield can. The test is now complete.

5. PARTS LIST, COMPONENT LOCATIONS, AND SCHEMATIC DIAGRAMS

All replaceable components of Reference Generator Assembly A12 are listed in table 2. Component locations are shown in figure 5. The Reference Generator Assembly is shown schematically in figure 6.

A21 is a self-contained assembly and is replaced as a unit. Therefore the parts list, component location diagram, and schematic diagram for A21 are not included in this manual.

Table 2. Reference Generator Assembly A12 Parts List (10121-4750 Rev. J)

Ref. Desig.	Part Number	Description
C1	M39014/02-1320V	CAP .47UF 10% 50V CER-R
C2	M39014/02-1320V	CAP .47UF 10% 50V CER-R
C3	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C4	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C5	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C6	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C7	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C8	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C9	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C10	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C11	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C12	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C13	C26-0035-100	CAP 10UF 20% 35V TANT
C14	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C15	C26-0035-470	CAP 47UF 20% 35V TANT
C16	C26-0025-339	CAP 3.3UF 20% 25V TANT
C17	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C18	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C19	C25-0001-301	CAP 1.0UF 20% 20V TANT
C20	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C21	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C22	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C23	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C24	M39014/02-1310V	CAP .1UF 10% 100V CER-R

Table 2. Reference Generator Assembly A12 Parts List (10121-4750 Rev. J) (Cont.)

Ref. Desig.	Part Number	Description
C25	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C26	M39014/02-1305V	CAP .047UF 10% 100V CER-R
C27	M39014/02-1305V	CAP .047UF 10% 100V CER-R
C28	C26-0025-339	CAP 3.3UF 20% 25V TANT
C29	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C30	M39014/01-1317V	CAP,1000PF,10% 200VC
C31	M39014/01-1317V	CAP,1000PF,10% 200VC
C32	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C33	C26-0025-680	CAP 68UF 20% 25V TANT
C34	M39014/02-1298V	CAP .01UF 10% 200V CER-R
C35	CM05CD150J03	CAP 15PF 5% 500V MICA
C36	C85-0001-002	CAP VAR 1-10PF PIST
C37	M39014/02-1298V	CAP .01UF 10% 200V CER-R
C38	M39014/02-1298V	CAP .01UF 10% 200V CER-R
C39	CM04ED470J03	CAP 47PF 5% 500V MICA
C40	M39014/02-1298V	CAP .01UF 10% 200V CER-R
C41	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C42	M39014/02-1298V	CAP .01UF 10% 200V CER-R
C43	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C44	M39014/02-1298V	CAP .01UF 10% 200V CER-R
C45	CM04ED560J03	CAP 56PF 5% 500V MICA
C46	M39014/02-1298V	CAP .01UF 10% 200V CER-R
C47	M39014/02-1298V	CAP .01UF 10% 200V CER-R
C48	M39014/02-1298V	CAP .01UF 10% 200V CER-R
C49	M39014/02-1298V	CAP .01UF 10% 200V CER-R
C50	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C51	M39014/02-1298V	CAP .01UF 10% 200V CER-R
C52	CM04ED560J03	CAP 56PF 5% 500V MICA
C53	M39014/02-1298V	CAP .01UF 10% 200V CER-R
C54	M39014/02-1298V	CAP .01UF 10% 200V CER-R
C55	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C56	M39014/02-1298V	CAP .01UF 10% 200V CER-R
C57	M39014/02-1298V	CAP .01UF 10% 200V CER-R
C58	M39014/02-1298V	CAP .01UF 10% 200V CER-R
C59	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C60	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C61	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C64	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C65	C26-0016-151	CAP 150UF 20% 16V TANT
C67	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C68	C26-0025-100	CAP 10UF 20% 25V TANT
C69	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C70	M39014/02-1310V	CAP .1UF 10% 100V CER-R

Table 2. Reference Generator Assembly A12 Parts List (10121-4750 Rev. J) (Cont.)

Ref. Desig.	Part Number	Description
C71	C26-0050-100	CAP 10UF 20% 50V TANT
C72	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C73	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C74	C26-0025-470	CAP 47UF 20% 25V TANT
C75	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C76	M39014/01-1317V	CAP,1000PF,10% 200VC
C77	M39014/02-1298V	CAP .01UF 10% 200V CER-R
C78	M39014/01-1317V	CAP,1000PF,10% 200VC
C79	M39014/02-1298V	CAP .01UF 10% 200V CER-R
C81	M39014/02-1298V	CAP .01UF 10% 200V CER-R
C82	M39014/02-1298V	CAP .01UF 10% 200V CER-R
C85	M39014/02-1298V	CAP .01UF 10% 200V CER-R
C87	10121-4720	CAP, CER 10PF N750
CR1	1N3064	DIODE 75mA 75V SW
CR2	1N3064	DIODE 75mA 75V SW
CR3	1N3064	DIODE 75mA 75V SW
CR4	1N3064	DIODE 75mA 75V SW
CR5	1N3064	DIODE 75mA 75V SW
CR6	1N3064	DIODE 75mA 75V SW
CR7	D25-0002-001	DIODE TUNING MV309
CR8	D25-0002-001	DIODE TUNING MV309
CR9	1N3064	DIODE 75mA 75V SW
CR10	1N3064	DIODE 75mA 75V SW
CR11	1N3064	DIODE 75mA 75V SW
CR12	1N3064	DIODE 75mA 75V SW
J1	J-0031	CONN SMB VERT PCB F
J2	J-0031	CONN SMB VERT PCB F
J3	J-0031	CONN SMB VERT PCB F
J4	J-0031	CONN SMB VERT PCB F
J5	J-0031	CONN SMB VERT PCB F
J6	J-0031	CONN SMB VERT PCB F
J7	J46-0032-010	HDR 10 PIN 0.100" SR
J8	J46-0022-003	HDR 3 PIN 0.100" SR LKG
J9	10073-7045	CONNECTOR, 9 PIN
J10	J-0031	CONN SMB VERT PCB F
J11	J-0031	CONN SMB VERT PCB F
JMP1	MP-1142	RES ZERO OHM (CKT JMPR)
L1	MS75085-19	COIL 1000UH 10% FXD RF
L2	MS75085-19	COIL 1000UH 10% FXD RF
L3	MS75084-12	COIL 10UH 10% FXD RF
L4	MS75083-7	COIL .33UH 10% FXD RF
L5	MS75084-12	COIL 10UH 10% FXD RF
L6	MS75084-5	COIL 2.7UH 10% FXD RF

Table 2. Reference Generator Assembly A12 Parts List (10121-4750 Rev. J) (Cont.)

Ref. Desig.	Part Number	Description
L7	MS75084-12	COIL 10UH 10% FXD RF
L8	MS75084-12	COIL 10UH 10% FXD RF
L9	MS75085-7	COIL 100UH 10% FXD RF
L10	MS75084-12	COIL 10UH 10% FXD RF
L11	82027-03	CHOKE WB 50MHZ
L12	82027-03	CHOKE WB 50MHZ
L13	82027-03	CHOKE WB 50MHZ
L14	MS75084-3	COIL 1.8UH 10% FXD RF
L15	MS75085-13	COIL 330UH 10% FXD RF
L16	MS75085-13	COIL 330UH 10% FXD RF
L17	MS75085-13	COIL 330UH 10% FXD RF
Q1	2N4393	XSTR JFET N-CH TO-18
Q2	2N4393	XSTR JFET N-CH TO-18
Q3	Q05-0001-000	XSTR JFET N-CH
Q4	2N2907A	XSTR SS/GP PNP TO-18
Q5	2N2222A	XSTR SS/GP NPN TO-18
Q6	2N2222A	XSTR SS/GP NPN TO-18
Q7	2N2907A	XSTR SS/GP PNP TO-18
Q8	2N3866	XSTR SS/RF NPN TO-39
Q9	Q-0153	XSTR SS/RF PN4258
Q10	2N2369A	XSTR SS/RF NPN TO-52
Q11	Q35-0003-000	XSTR N-CH JFET U310
Q12	Q35-0003-000	XSTR N-CH JFET U310
Q13	Q35-0003-000	XSTR N-CH JFET U310
Q14	Q35-0003-000	XSTR N-CH JFET U310
Q15	Q35-0003-000	XSTR N-CH JFET U310
Q17	2N2222A	XSTR SS/GP NPN TO-18
Q19	2N2222A	XSTR SS/GP NPN TO-18
Q20	2N2222A	XSTR SS/GP NPN TO-18
Q21	2N2222A	XSTR SS/GP NPN TO-18
Q22	2N2222A	XSTR SS/GP NPN TO-18
R1	R65-0003-510	RES 51 5% 1/4W CAR FILM
R2	R65-0003-101	RES 100 5% 1/4W CAR FILM
R3	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R4	R65-0003-681	RES 680 5% 1/4W CAR FILM
R6	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R7	R65-0003-123	RES 12K 5% 1/4W CAR FILM
R8	R65-0003-123	RES 12K 5% 1/4W CAR FILM
R9	R65-0003-273	RES 27K 5% 1/4W CAR FILM
R10	RN55D6810F	RES 681 1% 1/8W MET FLM
R11	R65-0003-101	RES 100 5% 1/4W CAR FILM
R12	RN55D6810F	RES 681 1% 1/8W MET FLM
R13	R65-0003-272	RES 2.7K 5% 1/4W CAR FILM
R14	RN55D2211F	RES 2210 1% 1/8W MET FLM

Table 2. Reference Generator Assembly A12 Parts List (10121-4750 Rev. J) (Cont.)

Ref. Desig.	Part Number	Description
R15	RN55D6810F	RES 681 1% 1/8W MET FLM
R16	RN55D2002F	RES 20.0K 1% 1/8W MET FLM
R17	RN55D3321F	RES 3320 1% 1/8W MET FLM
R18	RN55D6810F	RES 681 1% 1/8W MET FLM
R19	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R20	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R21	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R22	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R23	R65-0003-100	RES 10 5% 1/4W CAR FILM
R24	R65-0003-201	RES 200 5% 1/4W CAR FILM
R25	R65-0003-272	RES 2.7K 5% 1/4W CAR FILM
R26	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R27	R65-0003-330	RES 33 5% 1/4W CAR FILM
R28	R65-0003-470	RES 47 5% 1/4W CAR FILM
R29	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R30	R65-0003-562	RES 5.6K 5% 1/4W CAR FILM
R31	R65-0003-241	RES 240 5% 1/4W CAR FILM
R32	R65-0003-270	RES 27 5% 1/4W CAR FILM
R33	R65-0003-331	RES 330 5% 1/4W CAR FILM
R34	R65-0003-332	RES 3.3K 5% 1/4W CAR FILM
R35	R65-0003-391	RES 390 5% 1/4W CAR FILM
R36	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R37	R65-0003-201	RES 200 5% 1/4W CAR FILM
R38	R65-0003-201	RES 200 5% 1/4W CAR FILM
R39	R65-0003-101	RES 100 5% 1/4W CAR FILM
R40	R65-0003-201	RES 200 5% 1/4W CAR FILM
R41	R65-0003-202	RES 2.0K 5% 1/4W CAR FILM
R42	R65-0003-101	RES 100 5% 1/4W CAR FILM
R43	R65-0003-202	RES 2.0K 5% 1/4W CAR FILM
R44	R65-0003-201	RES 200 5% 1/4W CAR FILM
R45	R65-0003-751	RES 750 5% 1/4W CAR FILM
R46	R65-0003-751	RES 750 5% 1/4W CAR FILM
R47	R65-0003-201	RES 200 5% 1/4W CAR FILM
R48	R65-0003-302	RES 3.0K 5% 1/4W CAR FILM
R49	R65-0003-101	RES 100 5% 1/4W CAR FILM
R50	R65-0003-201	RES 200 5% 1/4W CAR FILM
R51	R65-0003-101	RES 100 5% 1/4W CAR FILM
R52	R65-0003-101	RES 100 5% 1/4W CAR FILM
R53	R65-0003-201	RES 200 5% 1/4W CAR FILM
R54	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R55	R65-0003-104	RES 100K 5% 1/4W CAR FILM
R56	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R57	R65-0003-473	RES 47K 5% 1/4W CAR FILM

Table 2. Reference Generator Assembly A12 Parts List (10121-4750 Rev. J) (Cont.)

Ref. Desig.	Part Number	Description
R58	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R59	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R60	R65-0003-473	RES 47K 5% 1/4W CAR FILM
R61	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R66	R65-0003-224	RES 220K 5% 1/4W CAR FILM
R67	R65-0003-304	RES 300K 5% 1/4W CAR FILM
R68	R65-0003-273	RES 27K 5% 1/4W CAR FILM
R69	R65-0003-182	RES 1.8K 5% 1/4W CAR FILM
R70	R65-0003-304	RES 300K 5% 1/4W CAR FILM
R71	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R72	R65-0003-473	RES 47K 5% 1/4W CAR FILM
R73	R65-0003-473	RES 47K 5% 1/4W CAR FILM
R74	R65-0003-473	RES 47K 5% 1/4W CAR FILM
R75	R65-0003-473	RES 47K 5% 1/4W CAR FILM
R76	R65-0003-473	RES 47K 5% 1/4W CAR FILM
R77	R65-0003-162	RES 1.6K 5% 1/4W CAR FILM
R78	R65-0003-152	RES 1.5K 5% 1/4W CAR FILM
T1	10073-7006	TRANSFORMER, RF, FIXED
T2	10073-7007	TRANSFORMER, RF, FIXED
T3	10073-7009	TRANSFORMER, RF, VARIABLE
T4	10073-7009	TRANSFORMER, RF, VARIABLE
T5	10073-7009	TRANSFORMER, RF, VARIABLE
TP1	J-0071	TP PWB BRN TOP ACCS .080"
TP2	J-0066	TP PWB RED TOP ACCS .080"
TP3	J-0069	TP PWB ORN TOP ACCS .080"
TP4	J-0070	TP PWB YEL TOP ACCS .080"
TP5	J-0068	TP PWB GRN TOP ACCS .080"
U1	IC-0430	IC 4044 PLASTIC CMOS
U2	I05-0000-074	IC 74LS74A PLASTIC TTL
U3	I05-0000-090	IC 74LS90 PLASTIC TTL
U5	I65-0004-001	IC PRESCALER 10/11 12013
U6	I05-0000-090	IC 74LS90 PLASTIC TTL
U7	I30-0003-000	IC OP AMP QUAD 324
U8	I01-0000-022	IC 4070B PLASTIC CMOS
VR1	I11-0001-001	IC VR 7805 +5V 1.5A 4%
Y1	10073-4720	CRYSTAL, 40 MHZ

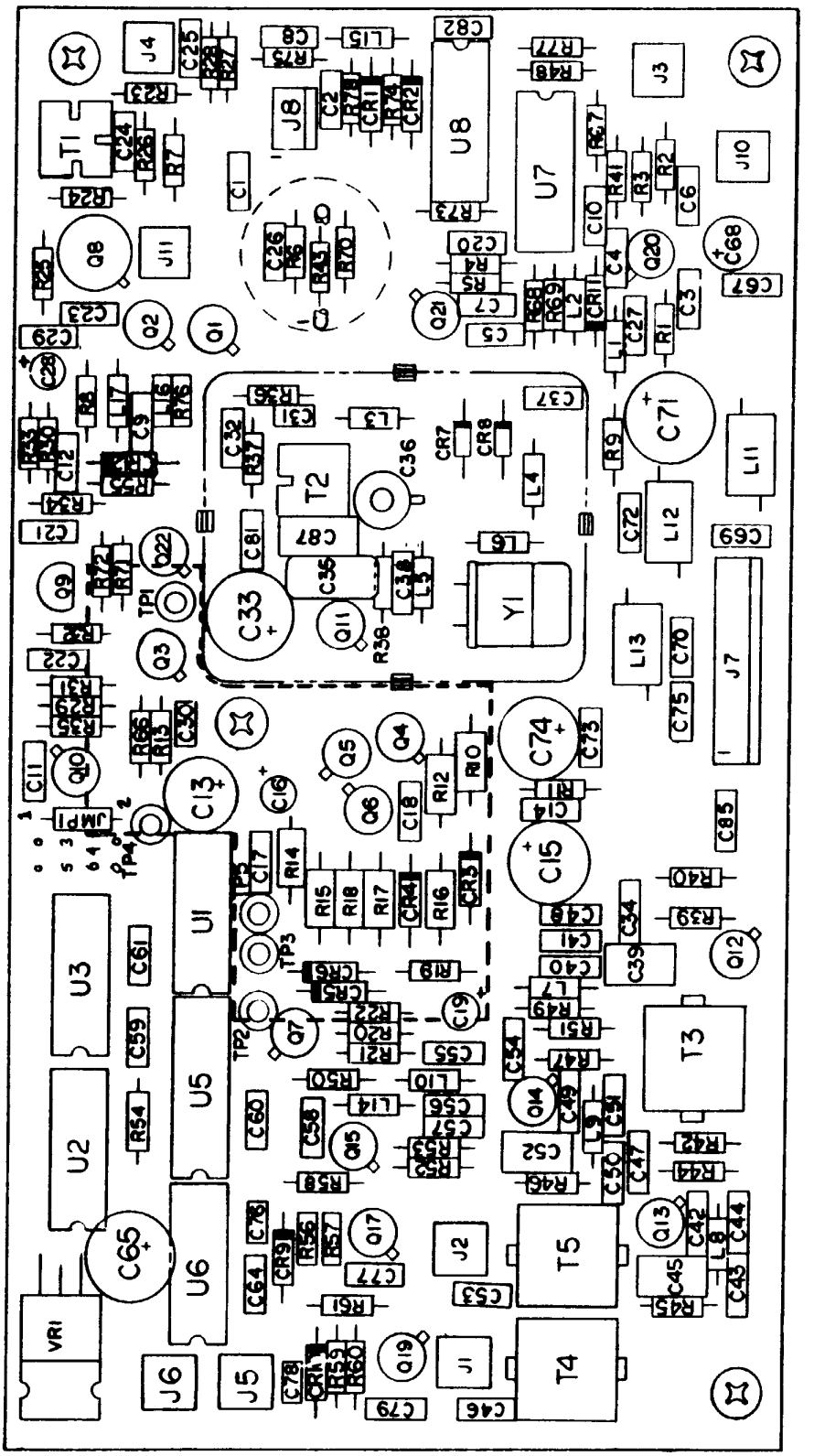


Figure 5. Reference Generator Assembly A12 Component Location Diagram (10121-4750 Rev. C)

NOTE: UNLESS OTHERWISE SPECIFIED:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR A COMPLETE DESIGNATION, PREFIX WITH UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.
2. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, ±5%.
3. ALL CAPACITOR VALUES ARE IN MICROFARADS.
4. VENDOR PART NO. CALLOUTS ARE FOR REFERENCE ONLY. COMPONENTS ARE SUPPLIED PER PART NO. IN PARTS LIST.
5. OPTIONAL JUMPERING REQUIRED:
   CONNECT 1 TO 2 WHEN USING 1MHZ STANDARD.
   CONNECT 3 TO 4 WHEN USING 5MHZ STANDARD.
   CONNECT 5 TO 6 WHEN USING 10MHZ STANDARD.
6. ALL INDUCTOR VALUES ARE IN MICROHENRIES.

UNUSED GATES	PT. NO.
	LM324

TABLE "A"

INT/EXT SW POS	STANDARD SOURCE	SIGNAL AT U3 PIN 1	PRIMARY FAIL (1=FAIL)
INT	INT ONLY	INT	0
INT	INT AND EXT	INT	0
INT	EXT ONLY	EXT	1
INT	NONE	NONE	1
EXT	EXT ONLY	EXT	0
EXT	INT AND EXT	EXT	0
EXT	INT ONLY	INT	1
EXT	NONE	NONE	1

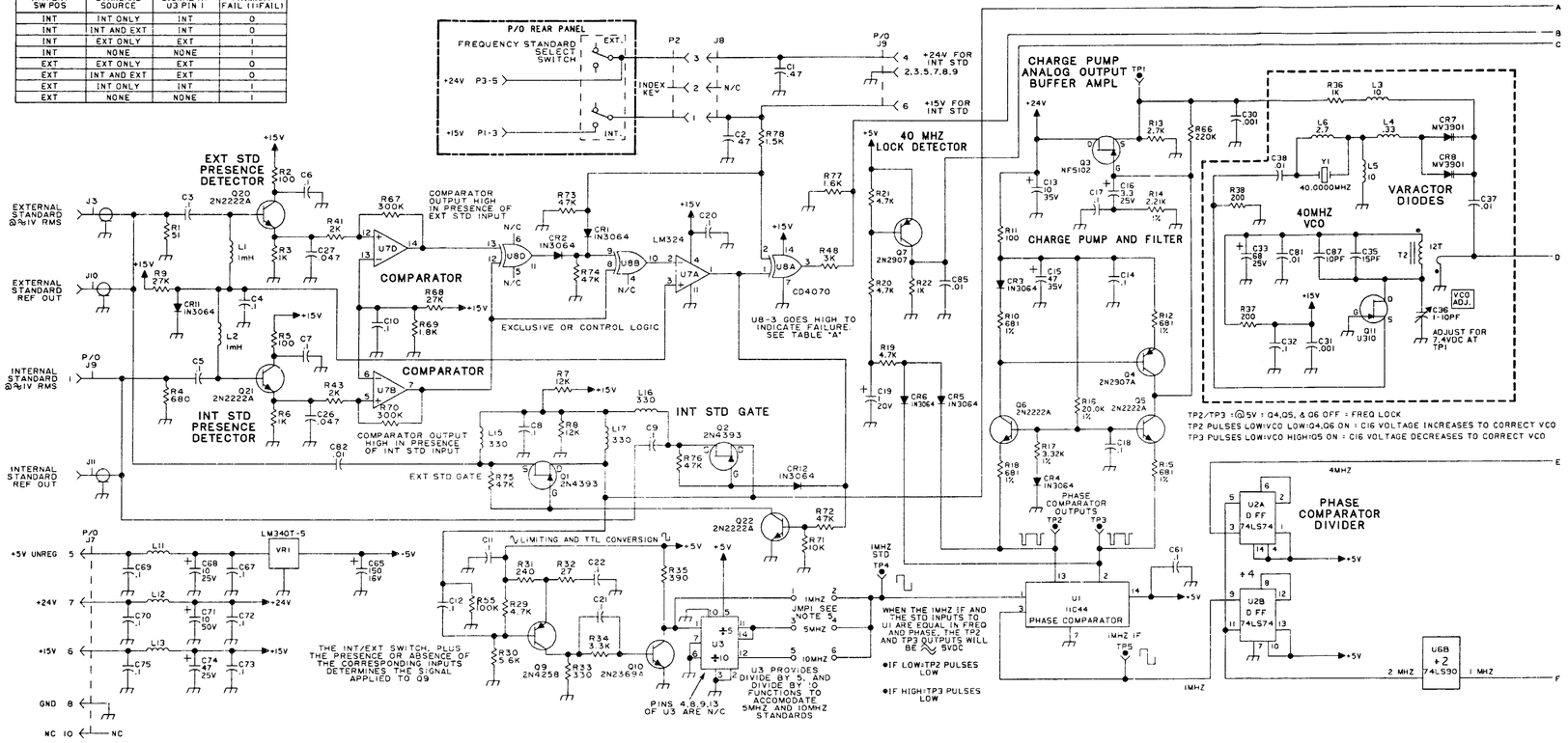


Figure 6. Reference Generator Assembly A12 Schematic Diagram (10121-4751 Rev. C) (Sheet 1 of 2)

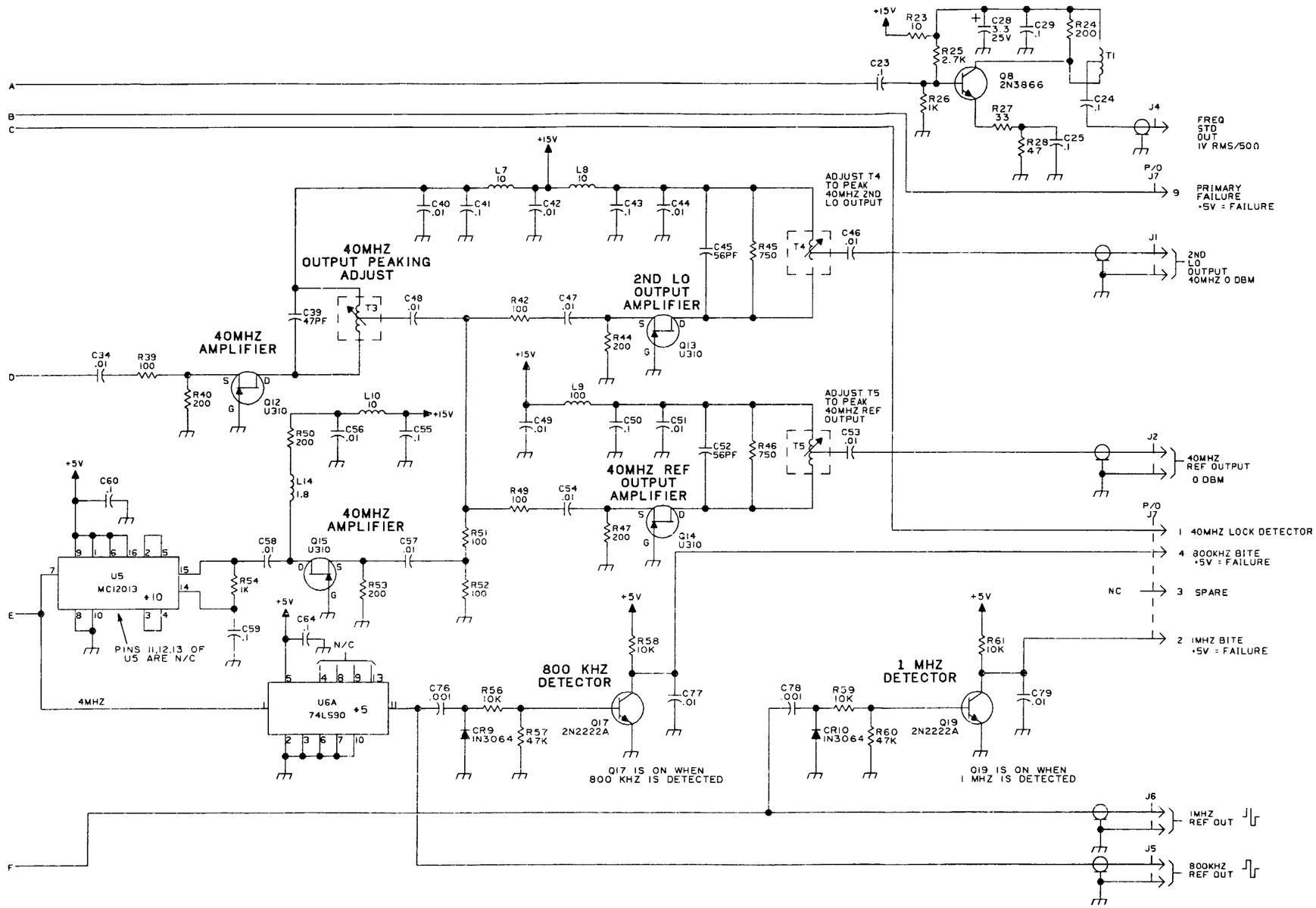
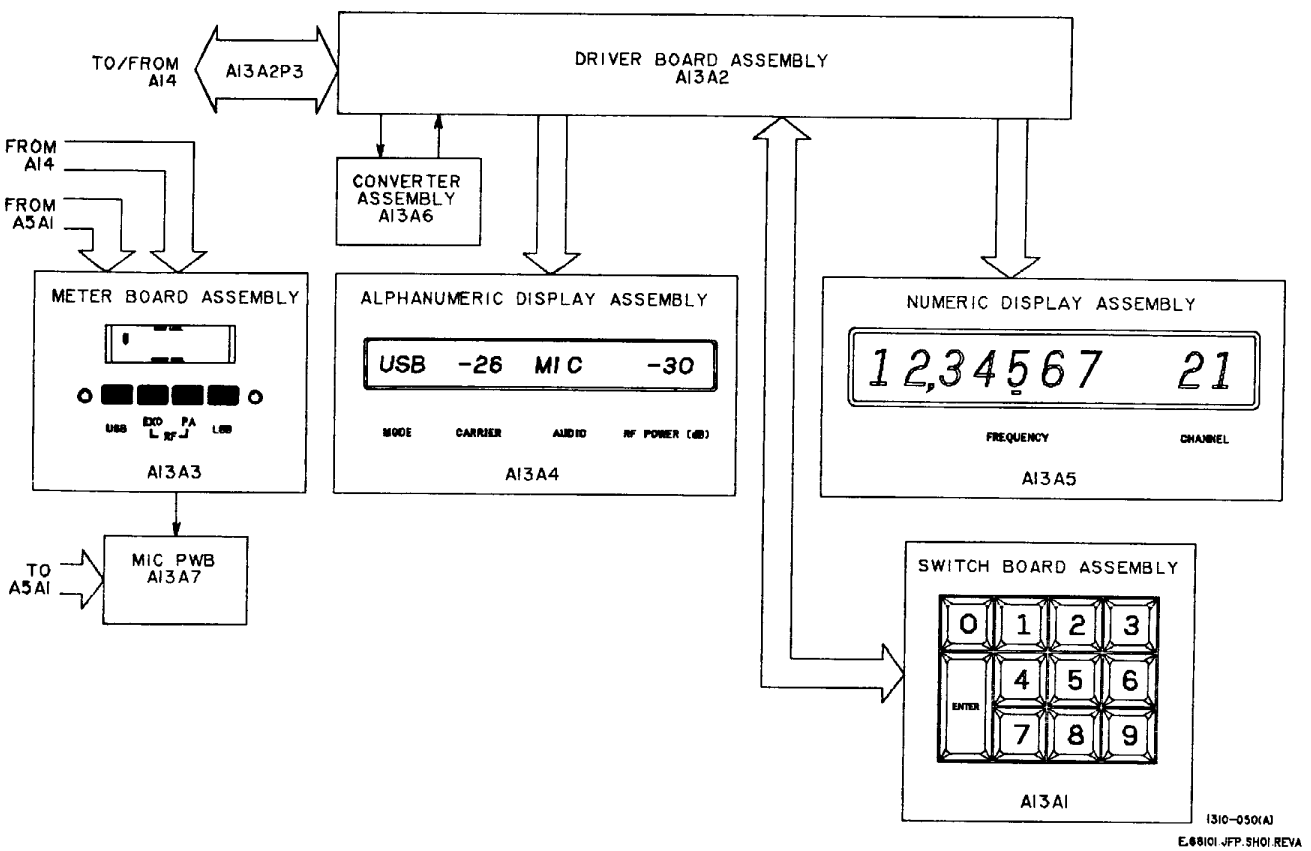


Figure 6. Reference Generator Assembly A12 Schematic Diagram (10121-4751 Rev. C) (Sheet 2 of 2)

A13
FRONT PANEL ASSEMBLY



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FRONT PANEL ASSEMBLY A13

1. GENERAL INFORMATION

Front Panel Assembly A13 contains control circuits which permit all operator local interface functions such as tuning, channel selection, system status indications, etc.

All operator controls (mode select, carrier select, audio input select, etc) are accessed from the front of the assembly. Figure 3-1 of the Operation section details the location and functions of these controls. Figure 1 shows the six subassemblies of the front panel.

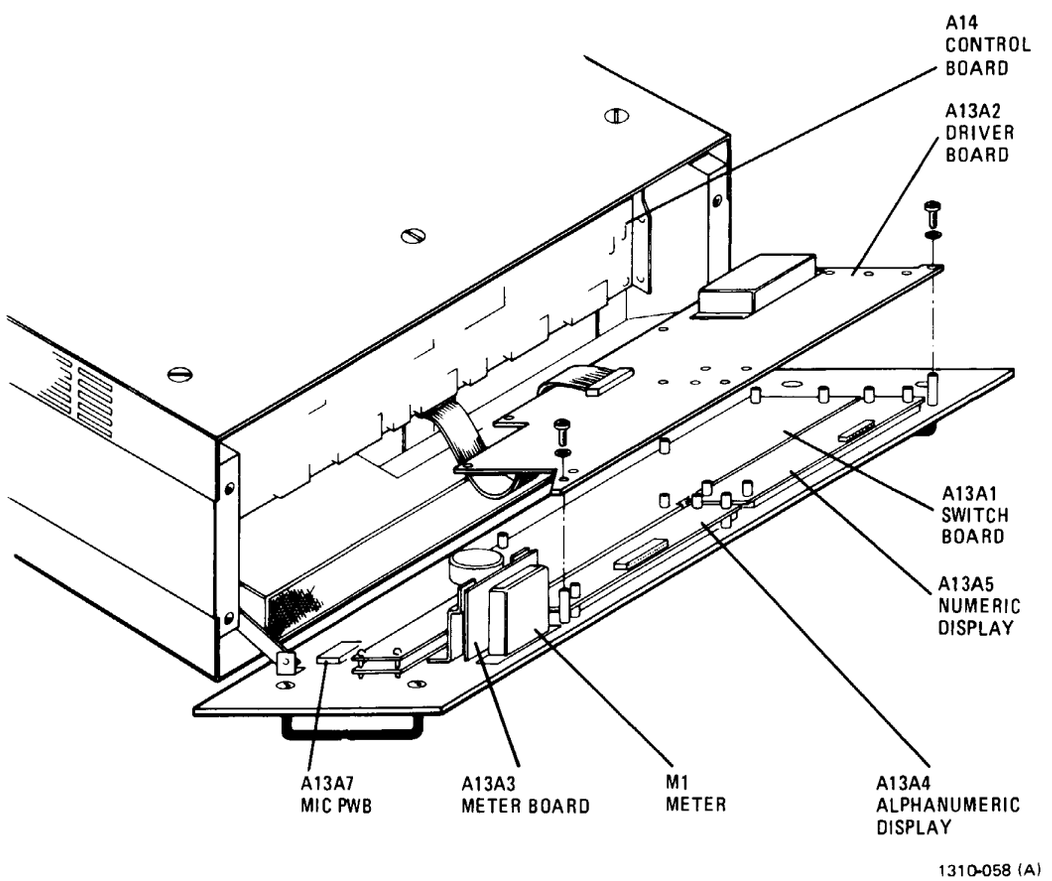


Figure 1. Front Panel Assembly A13 Exploded View

There are seven major subassemblies in Front Panel Assembly A13. They are shown in figure 2. These assemblies are:

- Switch Board Assembly A13A1
- Driver Board Assembly A13A2
- Meter Board Assembly A13A3
- Display Board (Alphanumeric) Assembly A13A4
- Display Board (Numeric) Assembly A13A5

- Converter Assembly A13A6
- Microphone PWB A13A7

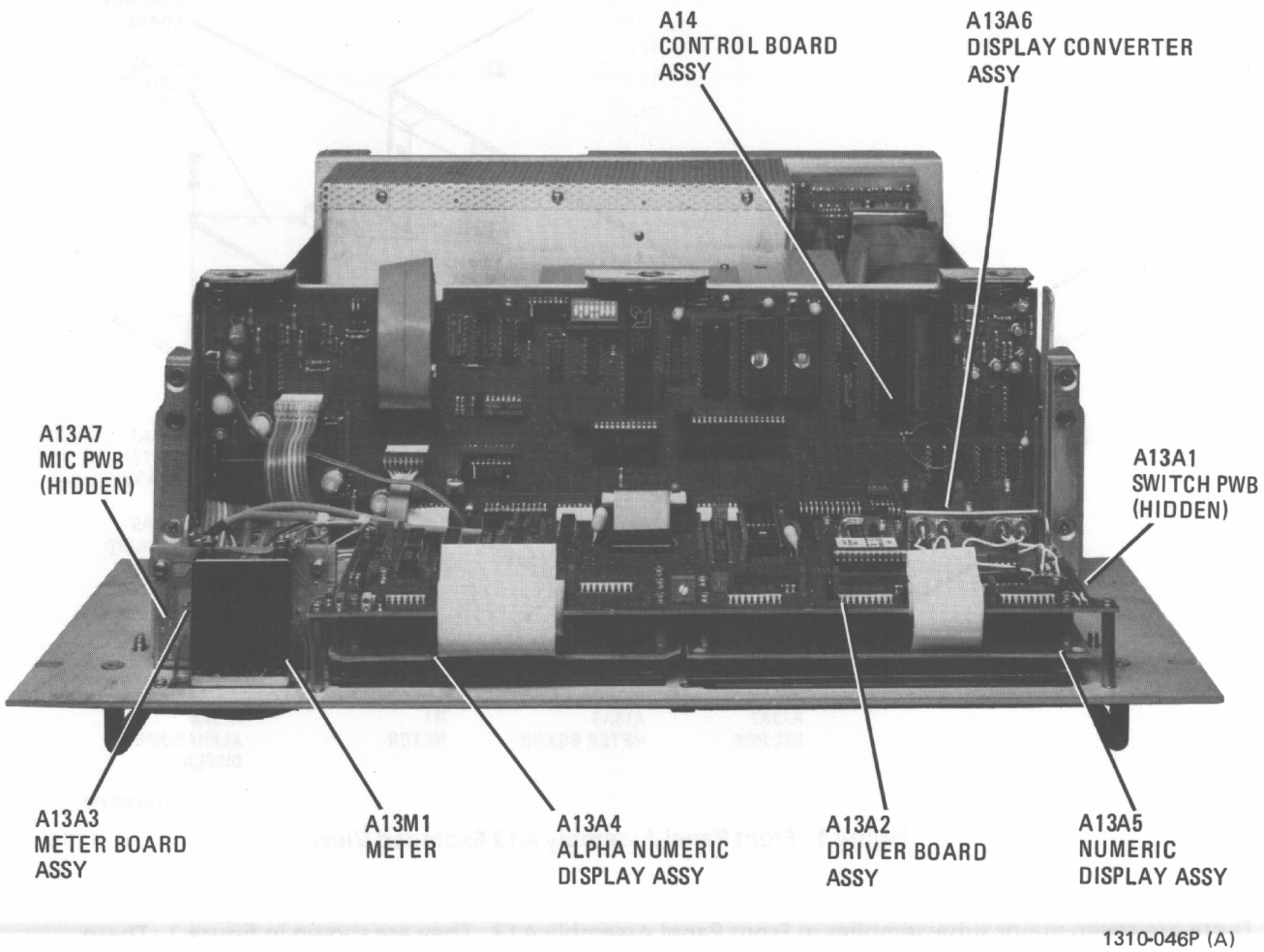


Figure 2. RF-1310 Front Panel Assembly A13 (Rear View)

The Front Panel Assembly is normally secured to the chassis by four front panel captive screws. Loosening these screws allows the entire assembly to pivot down on hinges (located at two lower corners). This permits access to any of the items listed above as well as to Control Board Assembly A14 which is mounted behind the front panel.

All major assemblies and components of Front Panel Assembly A13 are listed in table 1.

Table 1. RF-1310A Front Panel Assembly A13 Parts List (10121-2000-01 Rev. E)

Front Panel Assembly A13 Parts List		
Ref. Desig.	**Part Number**	**Description**
	10121-2001	FRONT PANEL
	10121-2004	BEZEL, LOWER FRT PNL
	10121-2007	BEZEL, UPPER MODIFIED
	10121-2019-01	HINGE, FRONT PANEL
	10121-2019-02	HINGE, FRONT PANEL
	10121-2077	INSULATOR, FOAM
	MP-1481	KNOB 0.713 DIA PLASTIC
A1	10121-2100-01	FRONT PANEL SWITCH/LED ASSY
A2	10121-2200	PWB ASSY, FRONT PANEL
A3	10121-2300	PWB ASSY, METER
A4	10073-2420	PWB ASSY, ALPHANUMERIC
A5	10073-2500	PWB ASSY, 7 SEG DISPLAY
A6	10073-2250	PWB ASSY, CONVERTER
A7	10121-2900	PWB ASSY, MIC
M1	10121-2311	METER
P1	J46-0016-006	CONNECTOR HOUSING, 6 PIN
P2	J40-0002-002	HOUSING, CONN, 2 PIN
S1	10121-2011	SW 5 POS 60 DEG
W21	10121-7281	CABLE ASSY, W21

2. FRONT PANEL SWITCHBOARD A13A1

2.1 General Description

All front panel switches and LEDs are mounted on Front Panel Switchboard Assembly A13A1 except the meter select switches. Signals generated by switch closures are routed to Control Board Assembly A14 via Front Panel Driver Board Assembly A13A2. The discrete LED displays are also driven from Front Panel Driver Board Assembly A13A2. Figure 3 is a block diagram of the A13A1 assembly.

2.2 Interface Connections

Table 2 lists Front Panel Switchboard Assembly A13A1 interface connections.

2.3 Functional Description

2.3.1 Switch Matrix

The pushbutton switches on the front panel are arranged in a matrix of eight columns by four rows. The eight column signals (COL 0 through COL 7) are inputs from Front Panel Driver Board Assembly A13A2, while the four row signals (PB0 through PB3) are outputs to the Driver Board. The microprocessor on the Control Board detects switch activity by enabling all the column outputs while reading back the row inputs (PB0 through PB3) looking for a connection between any row and any column. If a closure is detected, it enables the column lines selectively while reading back the row lines again to determine the exact location of the switch closure. The microprocessor then performs the activity indicated by the closure, including display update.

2.3.2 LED Circuits

The discrete LEDs on the switchboard are driven directly from the Front Panel Driver board. (See the description for Driver Board A13A2). Table 3 lists and describes the LED indicators.

2.4 Maintenance

The advanced design of the A13A1 assembly eliminates the need for regular maintenance. However, when replacing components on this assembly, observe the following caution:

CAUTION

Cleaning fluids normally used to remove flux will damage switches used on this assembly. Cleaning of the A13A1 assembly is not recommended.

2.5 Parts List, Component Locations, and Schematic Diagrams

Table 4 is the Front Panel Switchboard Assembly A13A1 parts list. Figures 4 and 5 are the Front Panel Switchboard Assembly A13A1 component location diagram and schematic diagram, respectively.

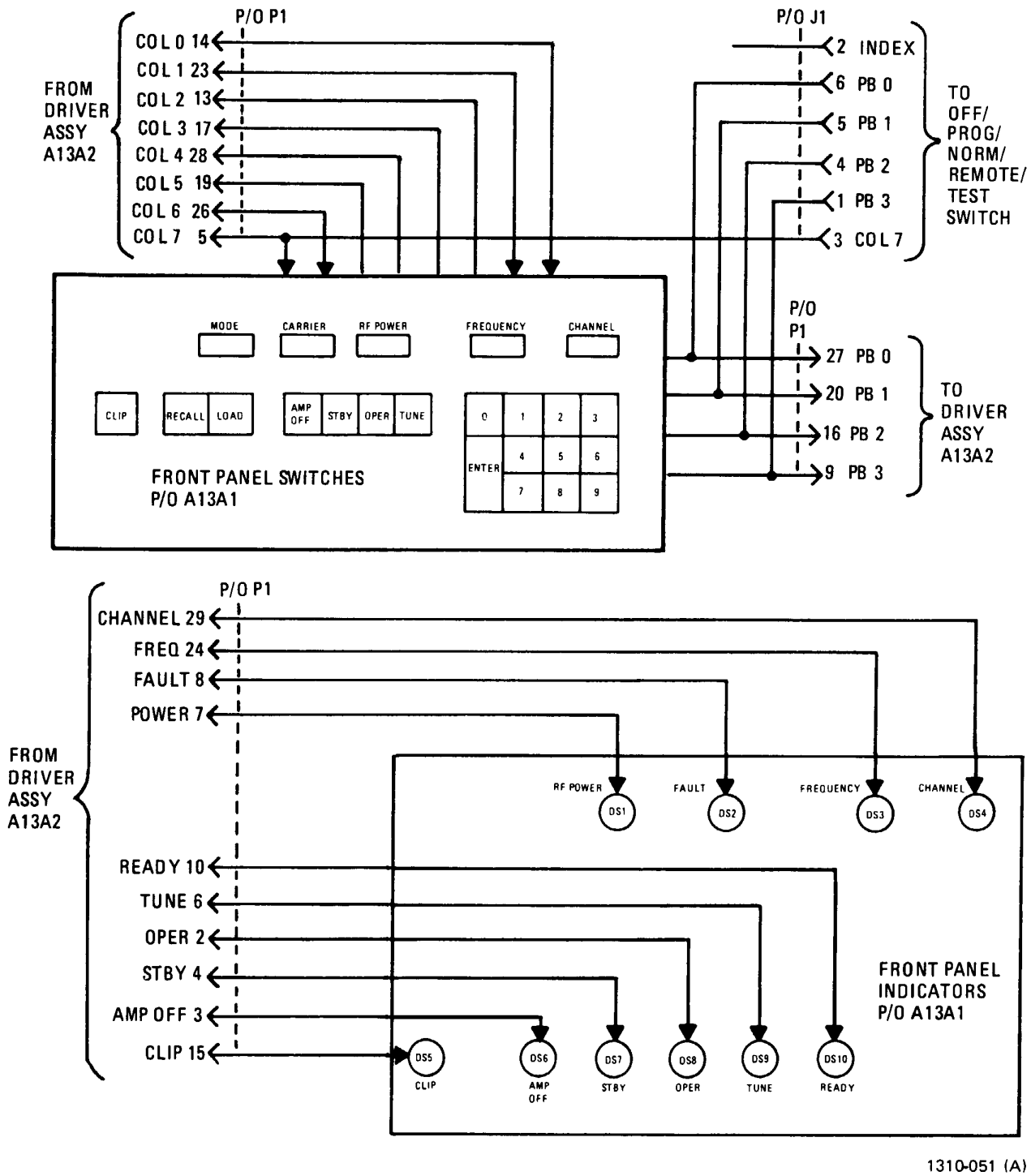


Figure 3. Front Panel Switchboard Assembly A13A1 Block Diagram

Table 2. Front Panel Switchboard Assembly A13A1 Interface Connections

Connector	Signal
P1 to/from A13A2	
P1-1	GND
P1-2	OPER
P1-3	AMP OFF
P1-4	STBY
P1-5	COL 7
P1-6	TUNE
P1-7	POWER
P1-8	Fault LED
P1-9	PB3
P1-10	READY
P1-11	TWA
P1-12	TWB
P1-13	COL 2
P1-14	COL 0
P1-15	CLIP
P1-16	PB2
P1-17	COL 3
P1-18	N/C
P1-19	COL 5
P1-20	PB1
P1-21	N/C
P1-22	N/C
P1-23	COL 1
P1-24	FREQ
P1-25	N/C
P1-26	COL 6
P1-27	PB0

Table 2. Front Panel Switchboard Assembly A13A1 Interface Connections (Cont.)

Connector	Signal
P1-28	COL 4
P1-29	CHANNEL
P1-30	+ 5 V
J1 to/from OFF/PROG/NORM/REMOTE/TEST SWITCH	
J1-1	PB3
J1-2	INDEX
J1-3	COL 7
J1-4	PB2
J1-5	PB1
J1-6	PB0

Table 3. Switchboard LED Indicator Assignments

Indicator	Function	Description
DS1	RF Power	Lights when keypad is dedicated to changing the PA power reduction value.
DS2	FAULT	Lights when BITE, power supply, or synthesizer fault is detected. Will also light briefly during powerup.
DS3	Frequency	Lights when keypad is dedicated to changing the frequency display.
DS4	Channel	Lights when keypad is dedicated to changing channel selection.
DS5	Clip	Lights when clipper is selected.
DS6	AMP OFF	Lights to indicate that the systems power amplifier is off.
DS7	STBY	Lights when the systems power amplifier is in standby mode.
DS8	OPER	Lights when the systems power amplifier is operational.
DS9	TUNE	Lights when tuning sequence is in process.
DS10	READY	Lights when tuning sequence is completed and system is ready to broadcast.

Table 4. RF-1310A Front Panel Switch/LED Assembly A13A1 Parts List (10121-2100-01 Rev. A)

Ref. Desig.	Part Number	Description
	10215-2069	BUTTON, SWITCH (6)
	10073-7052	RIBBON CABLE, 30 COND
	10121-2105	PLATE, SWITCH
	10073-2050	BUTTON,SW,0,CUSTOM MOLD
	10073-2051	BUTTON,SW,1,CUSTOM MOLD
	10073-2052	BUTTON,SW,2,CUSTOM MOLD
	10073-2053	BUTTON,SW,3,CUSTOM MOLD
	10073-2054	BUTTON,SW,4,CUSTOM MOLD
	10073-2055	BUTTON,SW,5,CUSTOM MOLD
	10073-2056	BUTTON,SW,6,CUSTOM MOLD
	10073-2057	BUTTON,SW,7,CUSTOM MOLD
	10073-2058	BUTTON,SW,8,CUSTOM MOLD
	10073-2059	BUTTON,SW,9,CUSTOM MOLD
	10073-2060	BUTTON,SW,TUNE,CUSTOM MLD
	10121-2044	BUTTON,SW,ENTER,MOLDED
	10121-2048	BUTTON,SW,CLIP, MOLDED
	10121-2047	BUTTON,SW,AMP OFF, MOLDED
	10073-2063	BUTTON,SW,RECALL,CSTM MLD
	10073-2064	BUTTON,SW,LOAD,CSTM MOLD
	10121-2046	BUTTON,SW,STBY,MOLDED
	10121-2045	BUTTON,SW,OPER,MOLDED
CR1	1N4454	DIODE 200MA 75V SW
CR2	1N4454	DIODE 200MA 75V SW
CR3	1N4454	DIODE 200MA 75V SW
CR4	1N4454	DIODE 200MA 75V SW
CR5	1N4454	DIODE 200MA 75V SW
CR6	1N4454	DIODE 200MA 75V SW
CR7	1N4454	DIODE 200MA 75V SW
CR8	1N4454	DIODE 200MA 75V SW
DS1	N21-0002-000	LED GRN T-1 2.0MCD
DS2	N21-0001-000	LED RED T-1 2.5MCD
DS3	N21-0002-000	LED GRN T-1 2.0MCD
DS4	N21-0002-000	LED GRN T-1 2.0MCD
DS5	N21-0002-000	LED GRN T-1 2.0MCD
DS6	N21-0002-000	LED GRN T-1 2.0MCD
DS7	N21-0002-000	LED GRN T-1 2.0MCD
DS8	N21-0002-000	LED GRN T-1 2.0MCD
DS9	N21-0002-000	LED GRN T-1 2.0MCD
DS10	N21-0002-000	LED GRN T-1 2.0MCD
J1	J46-0033-006	HDR 6 PIN 0.100" RT ANG
S1	S05-0004-001	SWITCH
S2	S05-0004-001	SWITCH
S3	S05-0004-001	SWITCH

Table 4. RF-1310A Front Panel Switch/LED Assembly A13A1 Parts List (10121-2100-01 Rev. A) (Cont.)

Ref. Desig.	Part Number	Description
S4	S05-0004-001	SWITCH
S5	S05-0004-001	SWITCH
S6	S05-0004-001	SWITCH
S7	S05-0004-001	SWITCH
S8	S05-0004-001	SWITCH
S9	S05-0004-001	SWITCH
S10	S05-0004-001	SWITCH
S11	S05-0004-001	SWITCH
S13	S05-0004-002	SW PB SPST NO MOM PCB
S14	S05-0004-002	SW PB SPST NO MOM PCB
S15	S05-0004-002	SW PB SPST NO MOM PCB
S16	S05-0004-002	SW PB SPST NO MOM PCB
S17	S05-0004-002	SW PB SPST NO MOM PCB
S18	S05-0004-002	SW PB SPST NO MOM PCB
S19	S05-0004-001	SWITCH
S20	S05-0004-001	SWITCH
S21	S05-0004-001	SWITCH
S22 – S25	S05-0004-001	SWITCH

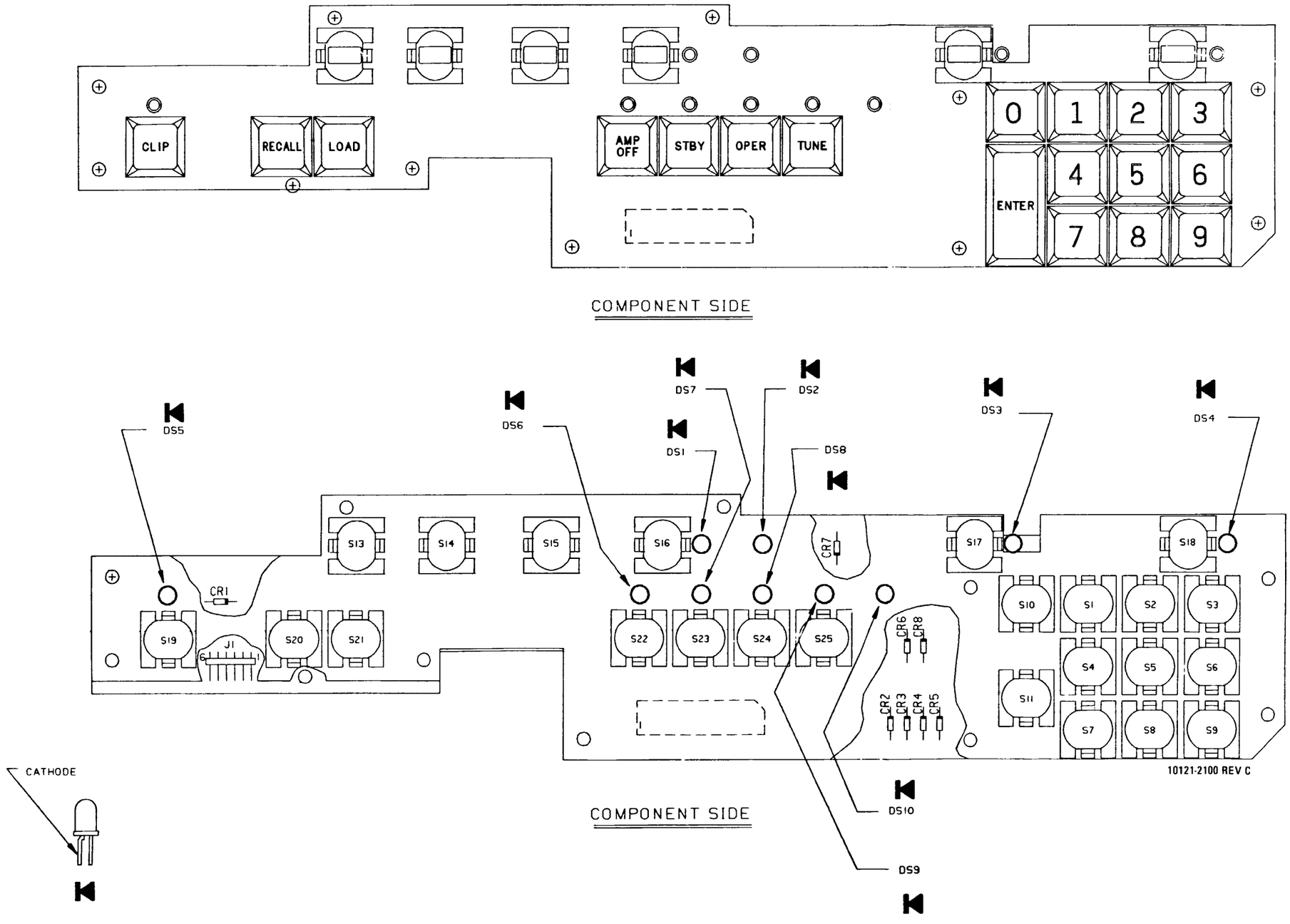


Figure 4. Front Panel Switchboard Assembly A13A1 Component Location Diagram (10121-2100 Rev. C)

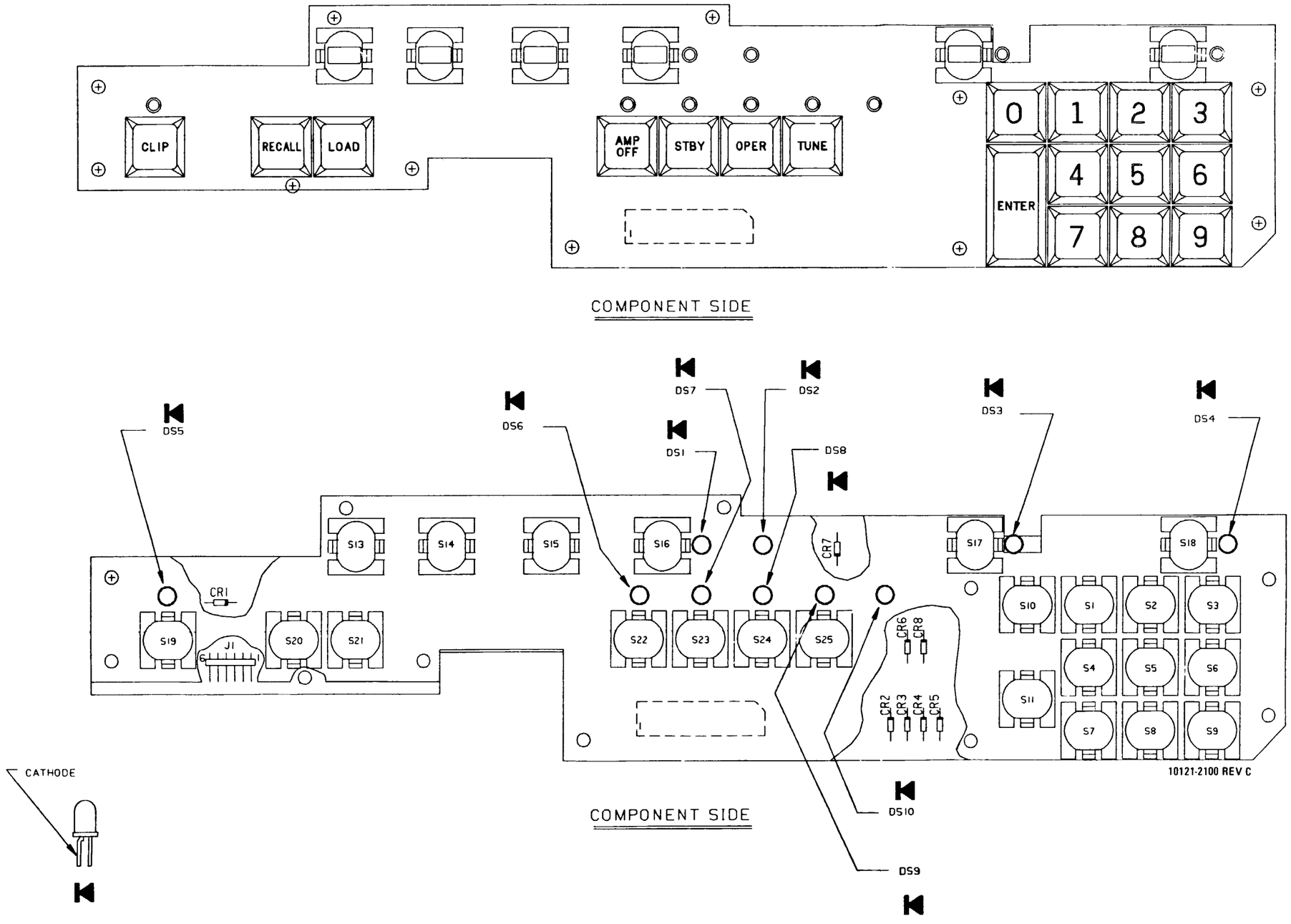


Figure 4. Front Panel Switchboard Assembly A13A1 Component Location Diagram (10121-2100 Rev. C)

NOTE: UNLESS OTHERWISE SPECIFIED:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR A COMPLETE DESIGNATION, PREFIX WITH UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.
2. VENDOR PART NO. CALLOUTS ARE FOR REFERENCE ONLY. COMPONENTS ARE SUPPLIED PER PART NO. IN PARTS LIST.
3. ☐ INDICATES FRONT PANEL MARKING.
4. CR1-CR8 ARE IN4454.

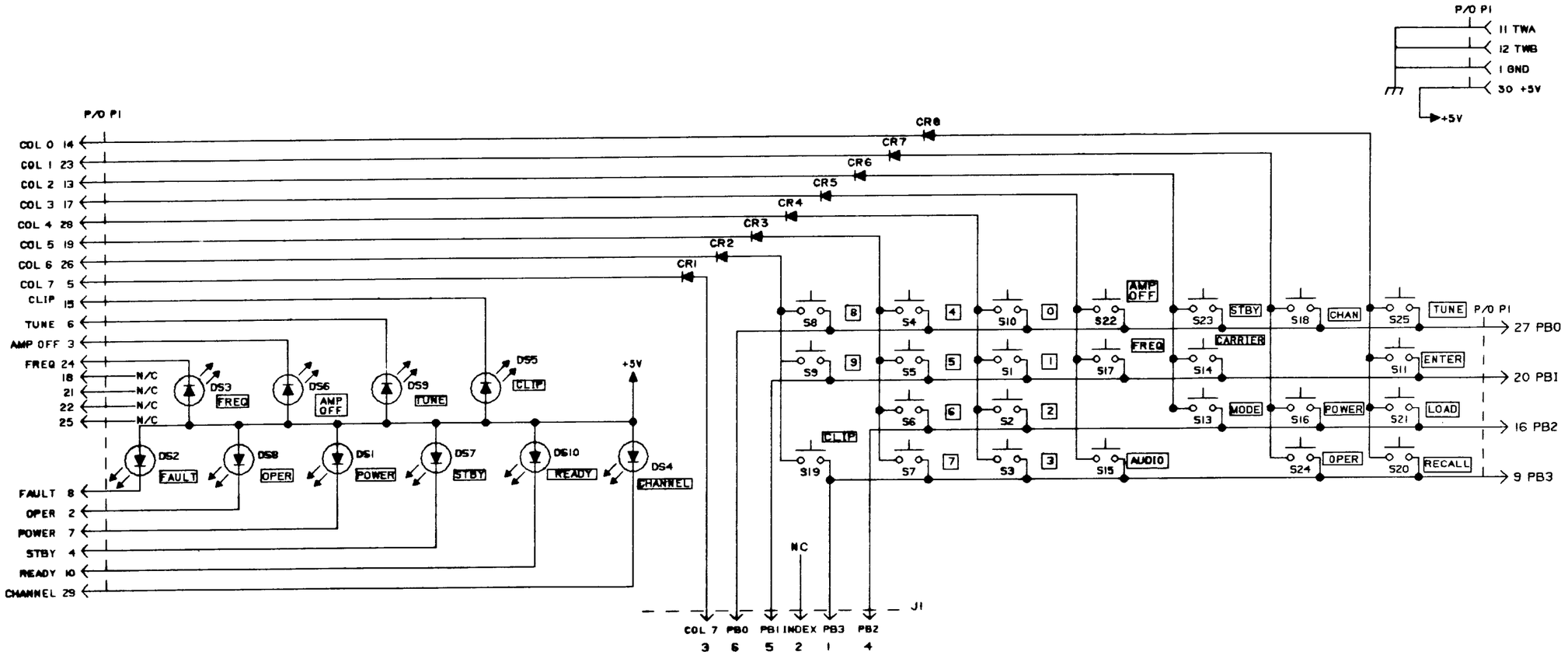


Figure 5. Front Panel Switchboard Assembly A13A1 Schematic Diagram (10121-2101 Rev. A)

3. FRONT PANEL DRIVER BOARD A13A2

3.1 General Description

Front Panel Driver Board A13A2 serves three basic front panel control functions. It generates the drive signals for the vacuum fluorescent displays, drives the discrete LED displays, and routes the signals to the front panel switchboard. Figure 6 is a block diagram of the A13A2 assembly.

The Driver Board controls the vacuum fluorescent displays by providing them with filament voltages, display segment information, and digit select information. The filament voltages are generated in Display Converter Assembly A13A6 and routed to the display connectors. The Driver Board multiplexes the VF displays by providing information for the segments to be lit within a character while enabling that character. This is done at a rapid rate to give the appearance of continuous illumination. The information to be displayed is provided to Driver Board A13A2 by Control Board Assembly A14 in serial fashion, using the Front Serial Data, Front Serial Clock, and Display Strobe signals on pins P3-2, P3-4, and P3-14, respectively.

The discrete LED displays of the front panel are lit by the Driver Board using information provided by the Control Board.

Driver Board Assembly A13A2 outputs eight column strobes to the switches in the front panel and inputs four row lines from the switches. The row lines are routed to the Control Board where a switch closure is detected as a connection from a column to a row.

3.2 Interface Connections

Table 5 summarizes the A13A2 interface connections.

3.3 Circuit Description

3.3.1 Microprocessor Operation

The heart of Front Panel Driver Board A13A2 operation is the U12 8035 microprocessor. The execution of the software program stored in the 2716-type EPROM (U16) causes the microprocessor to perform the display update functions described in paragraph 2. To execute the program, the microprocessor must continuously get instructions from U16 and process them. To accomplish this, the microprocessor (at the start of an instruction cycle) outputs the address of the instruction to be obtained into its address/data bus at pins U12-12 to U12-19. The address latch (U13) latches it to the EPROM. The U16 EPROM outputs the instruction to the data bus which is read by the microprocessor and executed. The microprocessor uses the Address Latch Enable (ALE) active high signal to indicate the presence of a valid address on the bus. The Program Store Enable (PSEN) signal is used to enable the EPROM to output the obtained instruction while the RD (read) and WR (write) signals are used to read from, and write to, other external devices. The RD signal is used to read display data sent by Control Board Assembly A14 from shift registers U14 and U15, while the WR signal is used to write the display information to VF display segment latches U8, U9, and U23. These functions are explained in greater detail below.

3.3.2 Display Data Input

Front Panel Driver Board A13A2 lights all LEDs and all segments of the vacuum fluorescent displays when the exciter is turned on. After completion of the power on self test, the display is updated to the last setting used before the exciter was turned off using display data provided by Control Board Assembly A14. The Control Board provides the information for all display updates to the Driver Board in serial fashion via P3-2. This information is clocked into serial shift registers U14 and U15 to be read in parallel by microprocessor U12. The clock signal is provided by the Control Board P4, and routed to the shift registers at pin 3. When the shift

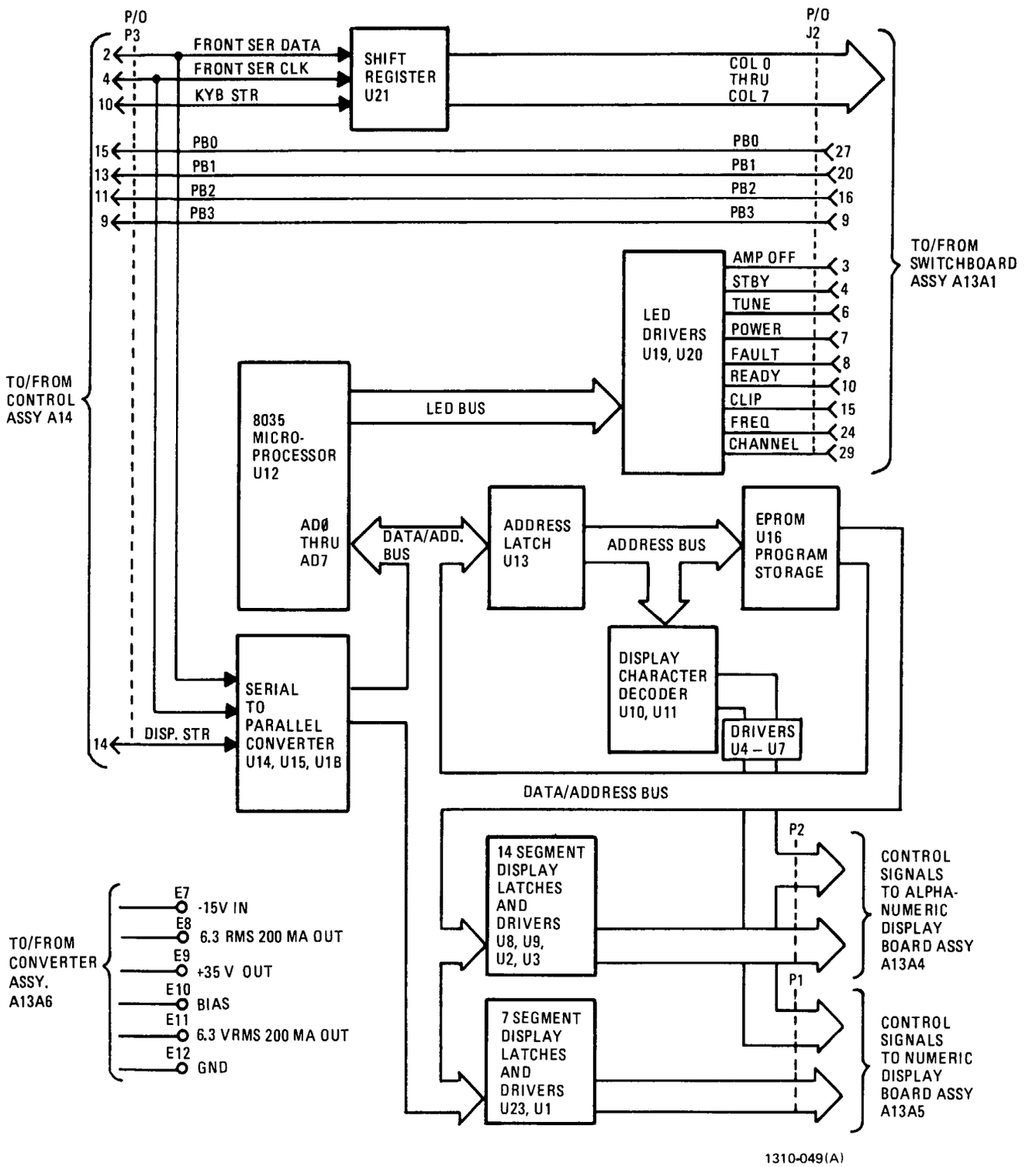


Figure 6. Front Panel Driver Board Assembly A13A2 Block Diagram

Table 5. Front Panel Driver Board Assembly A13A2 Interface Connections

Connector	Name	Description
P3 from A14 via W18		
P3-1	N/C	
P3-2	Front Serial Data	Serial display data from Control Board
P3-3	N/C	
P3-4	Front Serial CLK	Clock for display from Control Board
P3-5	N/C	
P3-6	-15 V	
P3-7	+ 5 V Display	
P3-8	Power Supply BITE	Power supply fault indicator
P3-9	PB3	Switch row readback to Control Board
P3-10	KYB STR	Keyboard strobe from Control Board
P3-11	PB2	Switch row readback to Control Board
P3-12	Fault Out	Output to rear panel (via Control Board)
P3-13	PB1	Switch row readback to Control Board
P3-14	DISP STR	Display strobe from Control Board
P3-15	PB0	Switch row readback to Control Board
P3-16	Reset	
P3-17	Spare	
P3-18	Ground	
P3-19	+ 5 V Unreg.	
P3-20	Ground	
J2 to/from A13A1		
J2-1	Ground	
J2-2	Oper	
J2-3	AMP OFF	
J2-4	STBY	
J2-5	COL 7	
J2-6	TUNE	

Table 5. Front Panel Driver Board Assembly A13A2 Interface Connections (Cont.)

Connector	Name	Description
J2-7	POWER	
J2-8	Fault	
J2-9	PB3	
J2-10	Ready	
J2-11	N/C	
J2-12	N/C	
J2-13	COL 2	
J2-14	COL 0	
J2-15	CLIP	
J2-16	PB2	
J2-17	COL 3	
J2-18	N/C	
J2-19	COL 5	
J2-20	PB1	
J2-21	N/C	
J2-22	N/C	
J2-23	COL 1	
J2-24	Freq	
J2-25	N/C	
J2-26	COL 6	
J2-27	PB0	
J2-28	COL 4	
J2-29	Channel	
J2-30	+ 5 V	
J3 to/from A13A4		
P2-1	a Segment	
P2-2	b Segment	
P2-3	c Segment	

Table 5. Front Panel Driver Board Assembly A13A2 Interface Connections (Cont.)

Connector	Name	Description
P2-4	d Segment	
P2-5	M Segment	
P2-6	N Segment	
P2-7	e Segment	
P2-8	f Segment	
P2-9	J Segment	
P2-10	k Segment	
P2-11	g Segment	
P2-12	h Segment	
P2-13	. Segment	
P2-14	, Segment	
P2-15	N/C	
P2-16	G1 Digit	
P2-17	P Segment	
P2-18	R Segment	
P2-19	G2 Digit	
P2-20	G3 Digit	
P2-21	G20 Digit	
P2-22	G4 Digit	
P2-23	G5 Digit	
P2-24	G6 Digit	
P2-25	G19 Digit	
P2-26	G7 Digit	
P2-27	G8 Digit	
P2-28	G9 Digit	
P2-29	G18 Digit	
P2-30	G10 Digit	
P2-31	G11 Digit	

Table 5. Front Panel Driver Board Assembly A13A2 Interface Connections (Cont.)

Connector	Name	Description
P2-32	G12 Digit	
P2-33	G17 Digit	
P2-34	G13 Digit	
P2-35	G14 Digit	
P2-36	N/C	
P2-37	G16 Digit	
P2-38	G15 Digit	
P2-39	Filament	
P2-40	Filament	
P1 to/from A13A5		
P1-1	G11 10 MHz Digit	
P1-2	G10 1 MHz Digit	
P1-3	G9 100 kHz Digit	
P1-4	G3 1/2 Digit	
P1-5	G7 1 kHz Digit	
P1-6	G8 10 kHz Digit	
P1-7	Filament	
P1-8	Decimal Point	
P1-9	G5 10 Hz Digit	
P1-10	G6 100 Hz Digit	
P1-11	N/C	
P1-12	Comma	
P1-13	G4 1 Hz Digit	
P1-14	c Segment	
P1-15	G2 CH10 Digit	
P1-16	G1 CH1 Digit	
P1-17	b Segment	
P1-18	a Segment	
P1-19	g Segment	

Table 5. Front Panel Driver Board Assembly A13A2 Interface Connections (Cont.)

Connector	Name	Description
P1-20	Filament	
P1-21	Underline Segment	
P1-22	d Segment	
P1-23	e Segment	
P1-24	f Segment	
E7	-15 V In	
E8	5.8 V_{rms} 200 mA Output	
E9	+ 35 V Out	
E10	Bias	
E11	5.8 V_{rms} 200 mA Output	
E12	Ground	

registers have been loaded with display data, the Control Board generates an interrupt to the U12 Driver Board microprocessor using the signal display strobe at P3-14. The display strobe pulse serves to trigger monostable multivibrator U24, which in turn generates the interrupt, causing the microprocessor to read the display data from shift registers U14 and U15. U18 buffers the display data onto the microprocessor data bus. The act of reading the shift registers causes resetting of the interrupt by the microprocessor read control line at U24-3 which is the reset in to the monostable.

3.3.3 Vacuum Fluorescent Display Drive

Display data read in from the Control Board is converted by microprocessor U12 into formats required for driving the VF displays. The displays are driven in multiplexed fashion so that only one character is driven at a given time. Each character in the VF displays has a unique address which is output by the microprocessor to the bus and latched into the U13 address latch during a display character update. The address is decoded by U10 or U11 into a character enable pulse. During the output instruction, the segment information for the character to be lit is latched into U23 for seven-segment characters or into U8 and U9 for 14-segment characters. Each character is enabled for approximately 640 microseconds after which, the microprocessor processes the next character in a similar manner.

3.3.4 LED Drive

The discrete LEDs on the front panel are driven from the parallel ports on microprocessor U12. These outputs are buffered by U19 and U20 and are routed to the switchboard via J2. An LED is lit by an active low output. The information to be written to the LEDs originates in Control Board Assembly A14 and is input to the Driver Board in the manner described in paragraph 3.3.2.

3.3.5 Pushbutton Circuitry

The Driver Board primarily routes the signals associated with detecting pushbutton activity to and from the Control Board and switchboards. The switches are arranged in a matrix of eight columns by four rows. Switch activity is detected by sensing a closure between a column line and a row line. The column outputs are written serially from the Control Board to the Driver board via P3-2, clocked via P3-4, and latched into shift register U21 by the signal KYB STR (keyboard strobe) at P3-10. The parallel outputs of the shift register are routed to the switchboard via J2 signals COL 0 through COL 7. The rows are routed back to the Control Board as signals PB0 to PB3 on pins P3-5, P3-13, P3-11, and P3-9 respectively.

3.4 Maintenance

3.4.1 Adjustments

The only adjustment on Front Panel Driver Board Assembly A13A2 is the VF display brightness, single-turn potentiometer R29, located at the top center of the PWB. Turn clockwise for brighter displays.

3.4.2 Troubleshooting

To make a quick assessment of Driver Board functions, the four test points should be checked with an oscilloscope.

- TP1 Microprocessor Write Line. Should be active low pulses repeated approximately every 600 to 700 microseconds.
- TP2 Character Strobe to U10. Active high pulse every 600 to 700 microseconds indicates display is being updated.
- TP3 Character Strobe to U11. Same as TP2. Also indicates display being updated. Both signals are required.
- TP5 Interrupt to microprocessor from Control board. Active low approximately 50 microseconds pulse every 1 second.

If the above signals are incorrect, more fundamental checks are indicated. Perform the checks in the following order.

a. Verify + 5 V at P3-7 and -15 V at P3-6.

b. Verify display converter voltages at E7-E12 of Driver Board and integrity of connections to converter module according to table 6.

c. Verify integrity of connections E1 through E6. The 10073-2400 alphanumeric display module requires connections E1 to E2 and E5 to E4.

d. Verify 6 MHz clock at U12-2 and U12-3.

e. Verify approximately + 5 V at U12-4. (Microprocessor reset in.)

f. Verify ALE signal, approximately 60-40 duty cycle square wave at U12-11.

g. Verify activity on bus AD0-AD7 (zero to five volt random square waves).

Table 6. Converter Voltages

Driver	Converter	Function
E7	C1	-15 Vdc
E8	C5	5.8 V_{rms}
E9	C3	+ 35 Vdc
E10	C4	Bias approximately 6 Vdc
E11	C2	5.8 V_{rms}
E12	E1	GND

h. Verify that all socketed ICs are installed correctly with no pins bent underneath the IC.

3.5 Parts List, Component Locations, and Schematic Diagram

Table 7 is the Front Panel Driver Board Assembly A13A2 parts list. Figures 7 and 8 are the Front Panel Driver Board Assembly A13A2 component location diagram and schematic diagram, respectively.

Table 7. Front Panel Driver Board Assembly A13A2 Parts List (10073-2200 Rev. AA)

Ref. Desig.	Part Number	Description
C1	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C2	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C3	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C4	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C5	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C6	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C7	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C8	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C10	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C12	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C14	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C15	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C19	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C22	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C23	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C24	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C25	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C26	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C27	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C29	M39014/01-1535V	CAP .01UF 10% 100V CER-R
C31	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C32	M39014/01-1317V	CAP,1000PF,10% 200VC

Table 7. Front Panel Driver Board Assembly A13A2 Parts List (10073-2200 Rev. AA) (Cont.)

Ref. Desig.	Part Number	Description
C37	C26-0025-470	CAP 47UF 20% 25V TANT
C38	C26-0050-479	CAP 4.7UF 20% 50V TANT
C39	M39014/01-1290V	CAP 33PF 10% 200V CER-R
C40	M39014/01-1290V	CAP 33PF 10% 200V CER-R
CR1	1N4454	DIODE 200MA 75V SW
CR2	1N4454	DIODE 200MA 75V SW
CR3	1N4454	DIODE 200MA 75V SW
CR4	1N4454	DIODE 200MA 75V SW
E1E2	MP-1142	RES ZERO OHM (CKT JMPR)
E4E5	MP-1142	RES ZERO OHM (CKT JMPR)
J2	J46-0013-030	HDR 30 PIN 0.100" DR SHRD
JMP1	MP-1142	RES ZERO OHM (CKT JMPR)
JMP2	MP-1142	RES ZERO OHM (CKT JMPR)
P1	10073-7050	RIBBON CABLE, 24 COND
P2	10073-7051	RIBBON CABLE, 40 COND
P3	10073-7053	RIBBON CABLE, 20 COND
R3	R50-0010-472	RES 4.7K 2% 10SIP 9RES
R14	R65-0003-224	RES 220K 5% 1/4W CAR FILM
R15	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R16	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R17	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R18	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R22	R51-0010-121	RES 120 2% 10SIP 5RES
R23	R51-0010-121	RES 120 2% 10SIP 5RES
R25	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R26	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R27	R65-0003-204	RES 200K 5% 1/4W CAR FILM
R28	R65-0003-393	RES 39K 5% 1/4W CAR FILM
R29	R-2232	RES VAR 100K 10% .5W VER.
R33	R65-0003-471	RES 470 5% 1/4W CAR FILM
R34	R65-0003-471	RES 470 5% 1/4W CAR FILM
R35	R65-0003-471	RES 470 5% 1/4W CAR FILM
R36	R65-0003-471	RES 470 5% 1/4W CAR FILM
R37	R65-0003-161	RES 160 5% 1/4W CAR FILM
R38	R50-0008-103	RES 10K 2% 8SIP 7RES
R50	R65-0003-100	RES 10 5% 1/4W CAR FILM
R52	R65-0003-100	RES 10 5% 1/4W CAR FILM
R53	R65-0004-332	RES 3.3K 5% 1/2W CAR FILM
TP1	J-0392	TP PWB BRN RA SIDE ACCESS
TP2	J-0387	TP PWB RED RA SIDE ACCESS
TP3	J-0390	TP PWB ORN RA SIDE ACCESS
TP5	J-0389	TP PWB GRN RA SIDE ACCESS

Table 7. Front Panel Driver Board Assembly A13A2 Parts List (10073-2200 Rev. AA) (Cont.)

Ref. Desig.	Part Number	Description
U1 – U4	I75-0009-001	IC NE594 DISPLAY DRIVER
U5	I75-0009-001	IC NE594 DISPLAY DRIVER
U6	I75-0009-001	IC NE594 DISPLAY DRIVER
U7	I75-0009-001	IC NE594 DISPLAY DRIVER
U8	I07-0013-001	IC 74C373 PLASTIC CMOS
U9	I07-0013-001	IC 74C373 PLASTIC CMOS
U10	I01-0000-202	IC 4514B PLASTIC CMOS
U11	I01-0000-202	IC 4514B PLASTIC CMOS
U12	IC-0374	IC MICMPTR 8-BIT 8035
U13	I07-0013-001	IC 74C373 PLASTIC CMOS
U14	I01-0000-156	IC 4094B PLASTIC CMOS
U15	I01-0000-156	IC 4094B PLASTIC CMOS
U16	10073-8302	SOFTWARE KIT,RF590 DRIVER
U17	I01-0000-362	IC 4098B PLASTIC CMOS
U18	I05-0000-244	IC 74LS244 PLASTIC TTL
U19	I05-0000-244	IC 74LS244 PLASTIC TTL
U20	I05-0000-244	IC 74LS244 PLASTIC TTL
U21	I01-0000-156	IC 4094B PLASTIC CMOS
U22	I05-0000-074	IC 74LS74A PLASTIC TTL
U23	I07-0013-001	IC 74C373 PLASTIC CMOS
U24	I01-0000-362	IC 4098B PLASTIC CMOS
U25	I01-0056-001	IC 74C02 PLASTIC CMOS
U26	I05-0000-027	IC 74LS27 PLASTIC TTL
U27	I02-0015-000	IC 7404 PLASTIC TTL
U28	I18-0006-001	IC 74C14 PLASTIC CMOS
VR1	1N5234B	DIODE 6.2V 5% .5W ZENER
XU12	J77-0008-007	SKT IC MACH 40 PIN
XU16	J77-0008-005	SKT IC MACH 24 PIN
Y1	Y15-0004-060	XTAL 6 MHZ

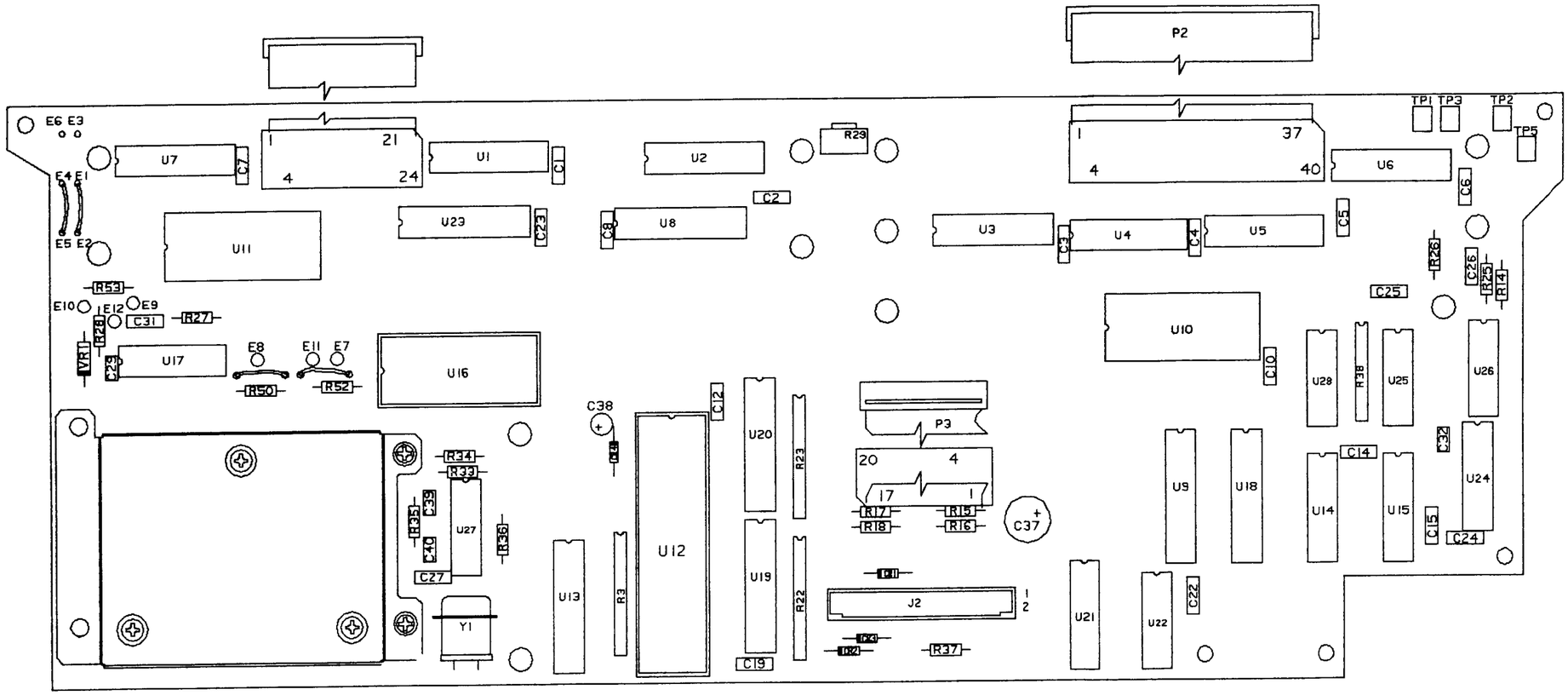


Figure 7. Front Panel Driver Board Assembly A13A2 Component Location Diagram (10073-2200 Rev. F)

NOTE: UNLESS OTHERWISE SPECIFIED:

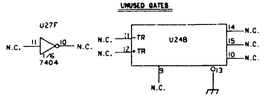
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR A COMPLETE DESIGNATION, PREFIX WITH UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.
2. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, ±5%.
3. ALL CAPACITOR VALUES ARE IN MICROFARADS.
4. VENDOR PART NO. CALLOUTS ARE FOR REFERENCE ONLY. COMPONENTS ARE SUPPLIED PER PART NO. IN PARTS LIST.
5. CONNECT E4 TO E5 AND E1 TO E2 FOR FUTABA ALPHANUMERIC DISPLAY (P/N 10073-2400).

NOTES CONTINUED:

6. SIGNALS ARE PRODUCT SPECIFIC FOR THE FOLLOWING PINS:

PIN	RF-590	RF-1310	RF-7110	RF-7405
P3-1	TUNE WHL INT	N/C	N/C	TWHLINT
P3-2	DATA	FR SER DATA	DATA OUT	DATA
P3-3	DIR	N/C	N/C	DIR
P3-4	CLK	FR SER CLK	DATA CLOCK	CLOCK
J2-2	SCAN	OPER	SQUELCH	LED SCAN 2
J2-3	TEST	AMP OFF	START LQA	LED SCAN 1
J2-4	PROG	STBY	SCAN	LED SCAN 4
J2-6	RCV	TUNE	REMOTE	LED SCAN 3
J2-7	BFO	POWER	CALL MAN	LED DATA 1
J2-10	REMOTE	READY	SILENT	LED SCAN 0
J2-15	TUNE	CLIP	CALL AUTO	LED DATA 0
J2-24	N/C	N/C	N/C	LED DATA 3
J2-25	NOISEBLANK	N/C	LISTEN	N/C
J2-29	N/C	N/C	N/C	LED DATA 2

UNUSED GATES



TEST POINT

TP1 PROCESSOR WRITE LINE
TP2 DIGIT STROBE TO V10
TP3 DIGIT STROBE TO V11
TP5 INTERRUPT FOR DISPLAY UPDATE

DISPLAY CONVERTER CONNECTIONS

PCB	CONVERTER	FCN
E7	C1	-15V IN
E8	C5	6.3 OUT
E9	C3	+35V OUT
E10	C4	BIAS
E11	C2	6.3 OUT
E12	E1	GND

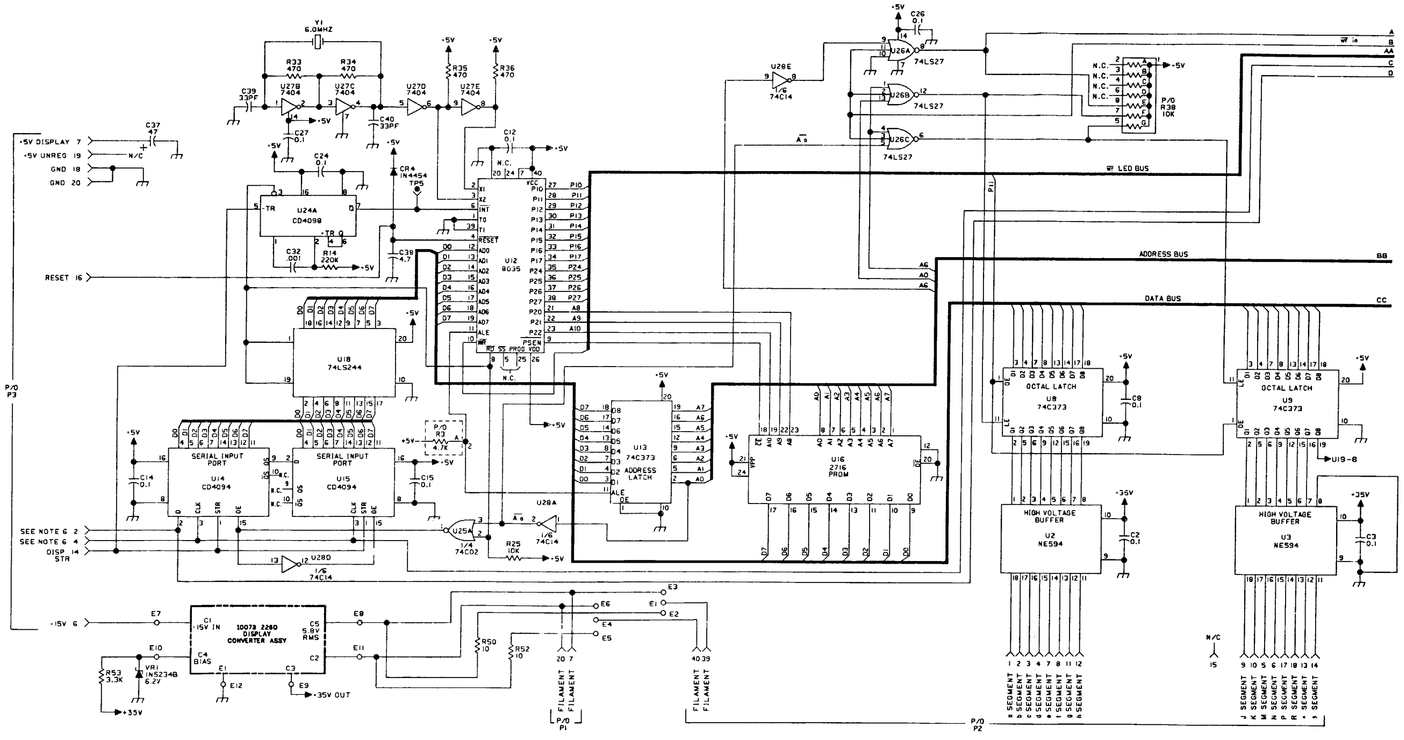


Figure 8. Front Panel Driver Board Assembly A13A2 Schematic Diagram (10073-2201 Rev. K) (Sheet 1 of 2)

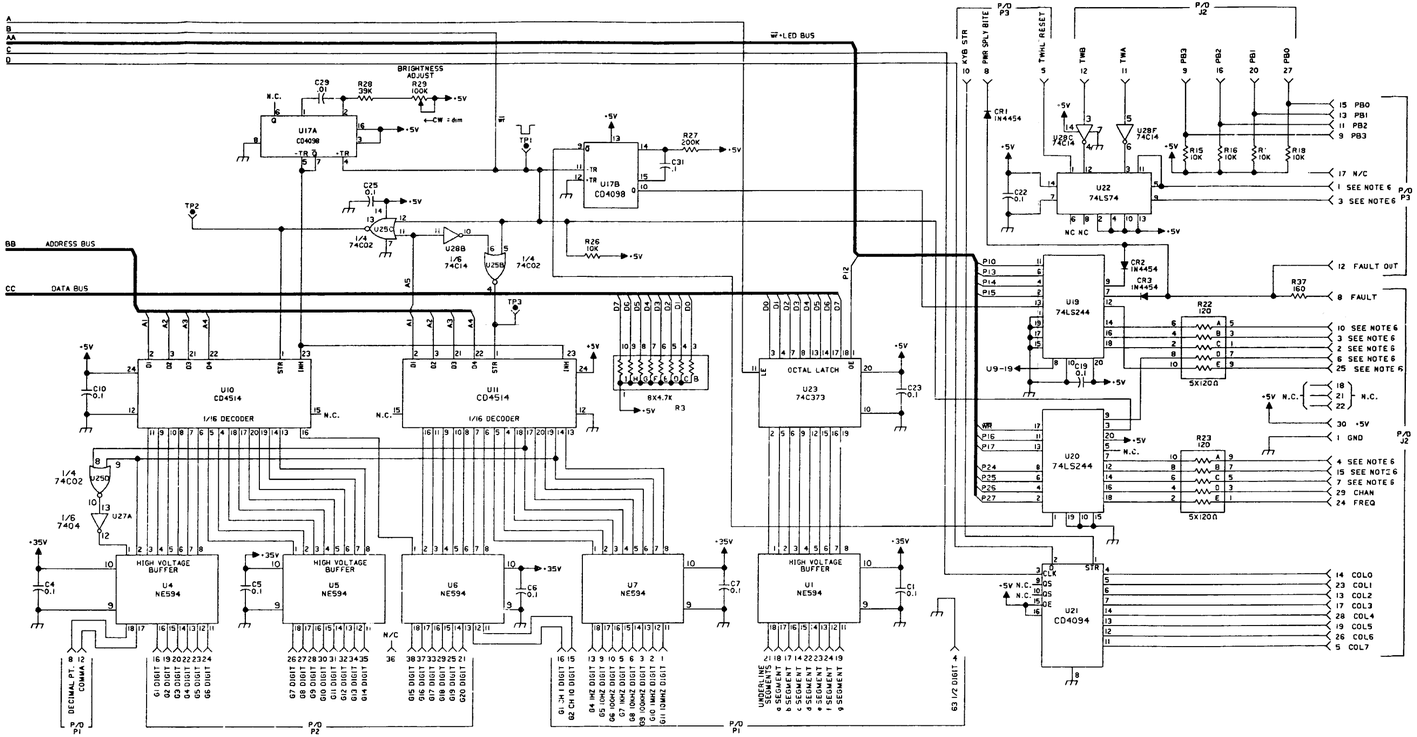


Figure 8. Front Panel Driver Board Assembly A13A2 Schematic Diagram (10073-2201 Rev. K) (Sheet 2 of 2)

4. FRONT PANEL METER BOARD ASSEMBLY A13A3

4.1 General Description

Front Panel Meter Board Assembly A13A3, shown in figure 9, contains the circuitry required to select and monitor RF and AF signals on the M1 front panel meter. The following signals may be selected for measurement via front panel pushbuttons.

- USB Audio In
- LSB Audio In
- Exciter RF Output
- PA RF Output

The USB and LSB audio signal levels are adjustable from the A13A3 assembly. Potentiometers for adjusting these levels are mounted on A13A3 and are accessible through holes in the front panel. The access holes are located next to the USB and LSB meter select switches. A13A3 is also used to route the CW KEY and PTT KEY signals from the front panel microphone jack to Control Board Assembly A14.

4.2 Interface Connections

Table 8 summarizes the A13A3 assembly interface connections.

4.3 Circuit Description

4.3.1 Meter Control

Dc signals representing the levels of RF output signals of the exciter (A1 OUTPUT DET) and power amplifier (BUFF APC) are routed to A13A3 via the Control Board Assembly A14. Likewise, USB and LSB audio signal levels are represented by dc signals that come from Audio 1 Assembly A5A1 and are labeled USB Meter Dc and LSB Meter Dc.

The signals are input to a switch network that applies one signal at a time to the front panel meter. The signals representing the exciter and PA output levels are routed directly to the meter when they are selected. When the USB or LSB switch is engaged, the USB meter dc or LSB meter dc signal is routed back to the A5A1 assembly as the Log Amp input signal. The signal is processed by a metering logarithmic amplifier on the A5A1 assembly. The A5A1 assembly returns the log amp output signal that is compatible with the front panel meter. This signal is routed through the switch network to the meter. The meter is zeroed for the audio signal level measurement by adjusting R99 on A5A1.

4.3.2 Audio Signal Level Adjustment

Potentiometers R4 and R5 on the Meter Board are used to adjust the USB and LSB audio signal levels, respectively. Both potentiometers can be accessed through holes in the front panel. The access holes are located adjacent to the USB and LSB meter select switches. Adjusting R4 or R5 will increase or decrease the gain of the first stage of the USB or LSB audio amplifier on A5A1.

4.3.3 CW KEY and PTT KEY

The CW KEY and PTT KEY signals are passively routed from the front panel microphone jack to Control Board Assembly A14 by the Meter Board.

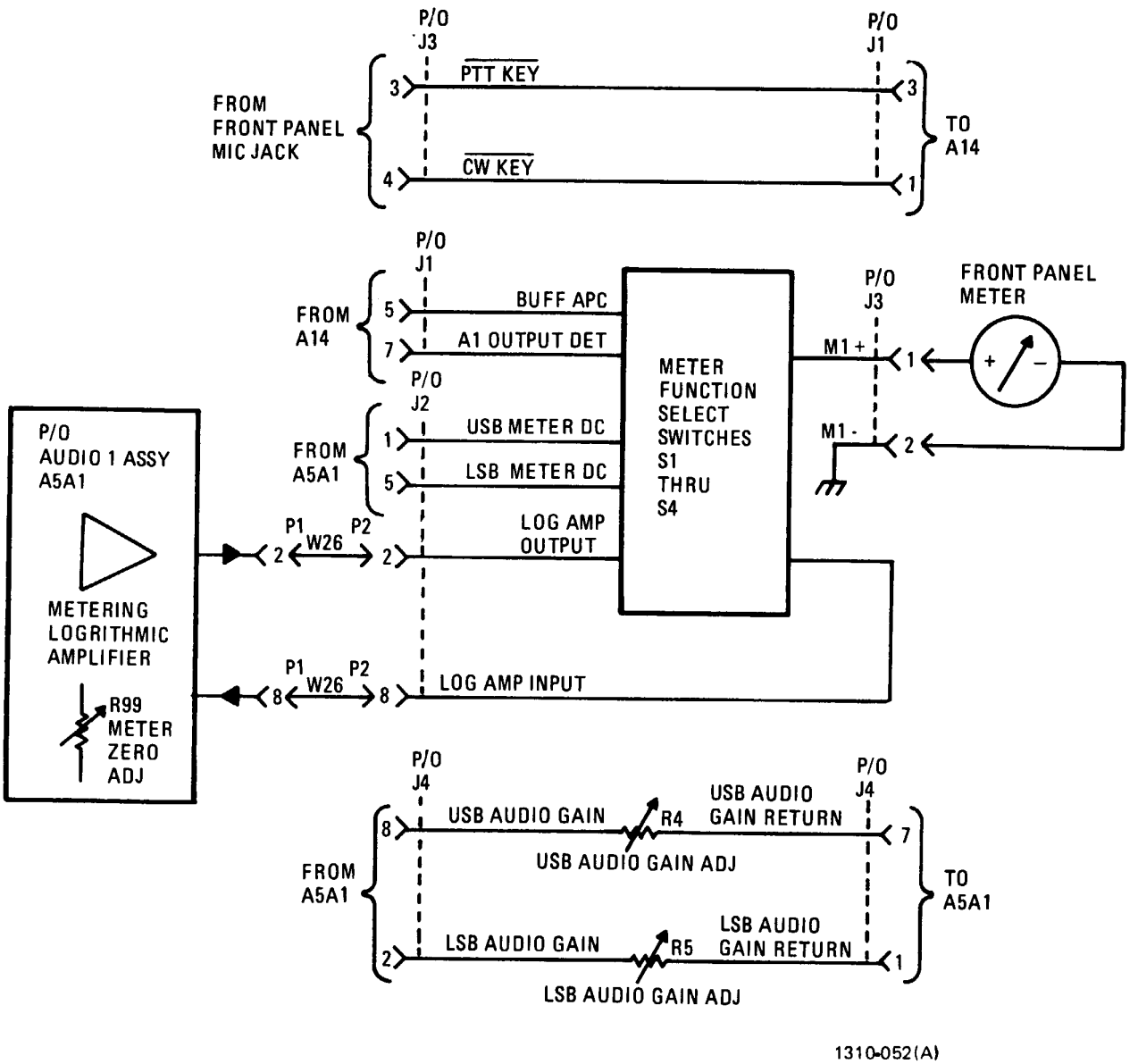


Figure 9. Front Panel Meter Board Assembly A13A3 Block Diagram

Table 8. Front Panel Meter Board Assembly A13A3 Interface Connections

Pin	Signal	Description
J1-1	CW KEY	CW KEY signal from front panel microphone jack to A14.
J1-2	INDEX	Not connected.
J1-3	PTT KEY	PTT key signal from front panel microphone jack to A14.
J1-4	Spare not connected	
J1-5	BUFF APC	PA RF output signal level to A13A3S3 (dc signal).
J1-6	GND	Ground
J1-7	A1 OUTPUT DET	RF output signal level from A1 to A13A3S1 (dc signal).
J1-8	Spare not connected	
J2-1	USB METER DC	USB audio signal level to A13A3S1.
J2-2	LOG AMP OUTPUT	
J2-3	INDEX	Not connected.
J2-4	Spare not connected	
J2-5	LSB METER DC	LSB audio signal level to A13A3S4.
J2-6	GND	Ground
J2-7	Spare not connected	
J3-1	M1 (+)	Dc signal to meter.
J3-2	M1 (-)	Meter return-ground.
J3-3	PTT KEY	PTT key signal from microphone jack.
J3-4	CW KEY	CW key signal from microphone jack.
J3-5	GND Ground	
J3-6	Spare not connected	
J4-1	LSB AUDIO GAIN RETURN	LSB audio gain control signal to A5 assembly (ground).
J4-2	LSB AUDIO GAIN	LSB audio gain control signal from A5 assembly.
J4-3	GND	Ground
J4-4	INDEX	Not connected.
J4-5	Spare not connected	
J4-6	GND	Ground
J4-7	USB AUDIO GAIN RETURN	USB audio gain control signal to A5 assembly (ground).
J4-8	USB AUDIO GAIN	USB audio gain control signal from A5 assembly.

4.4 Parts Lists, Component Locations, and Schematic Diagram

Table 9 is the Front Panel Meter Board Assembly A13A3 parts list. Figures 10 and 11 are the Front Panel Meter Board Assembly A13A3 component location diagram and schematic diagram.

Table 9. Front Panel Meter Board Assembly A13A3 Parts List (10121-2300 Rev. D)

Ref. Desig.	Part Number	Description
	10073-2313	SW DPDT 4SEC INTLOCKING
J1	J46-0032-008	HDR 8 PIN 0.100" SR
J2	J46-0032-008	HDR 8 PIN 0.100" SR
J3	J46-0022-006	HDR 6 PIN 0.100"
J4	J46-0032-008	HDR 8 PIN 0.100" SR
R1	RN55D2432F	RES 24.3K 1% 1/8W MET FLM
R2	RN55D5492F	RES 54.9K 1% 1/8W MET FLM
R3	RN55D5622F	RES 56.2K 1% 1/8W MET FLM
R4	R30-0001-102	RES VAR 1K 3/4W 20%
R5	R30-0001-102	RES VAR 1K 3/4W 20%

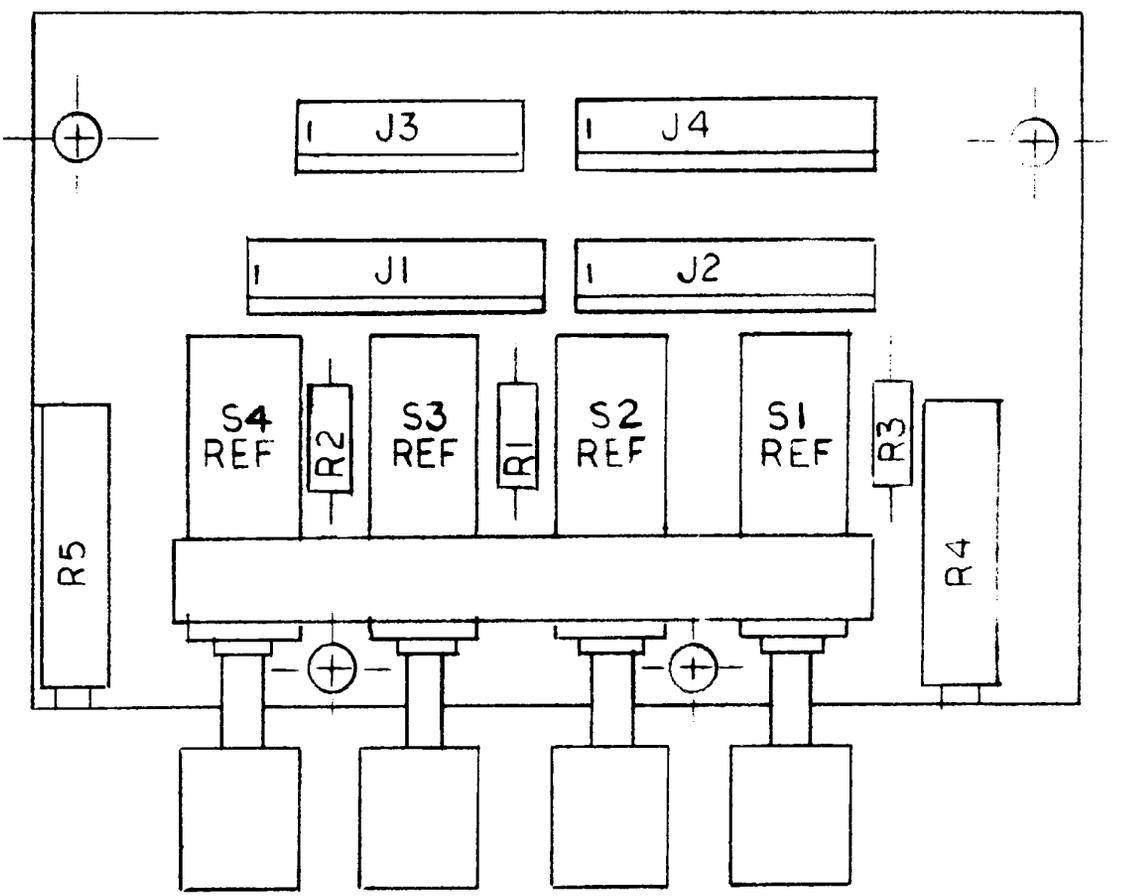


Figure 10. Front Panel Meter Board Assembly A13A3 Component Location Diagram (10121-2300 Rev. D)

NOTE: UNLESS OTHERWISE SPECIFIED:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR A COMPLETE DESIGNATION, PREFIX WITH UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.

2. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, ±5%.

3. VENDOR PART NO. CALLOUTS ARE FOR REFERENCE ONLY. COMPONENTS ARE SUPPLIED PER PART NO. IN PARTS LIST.

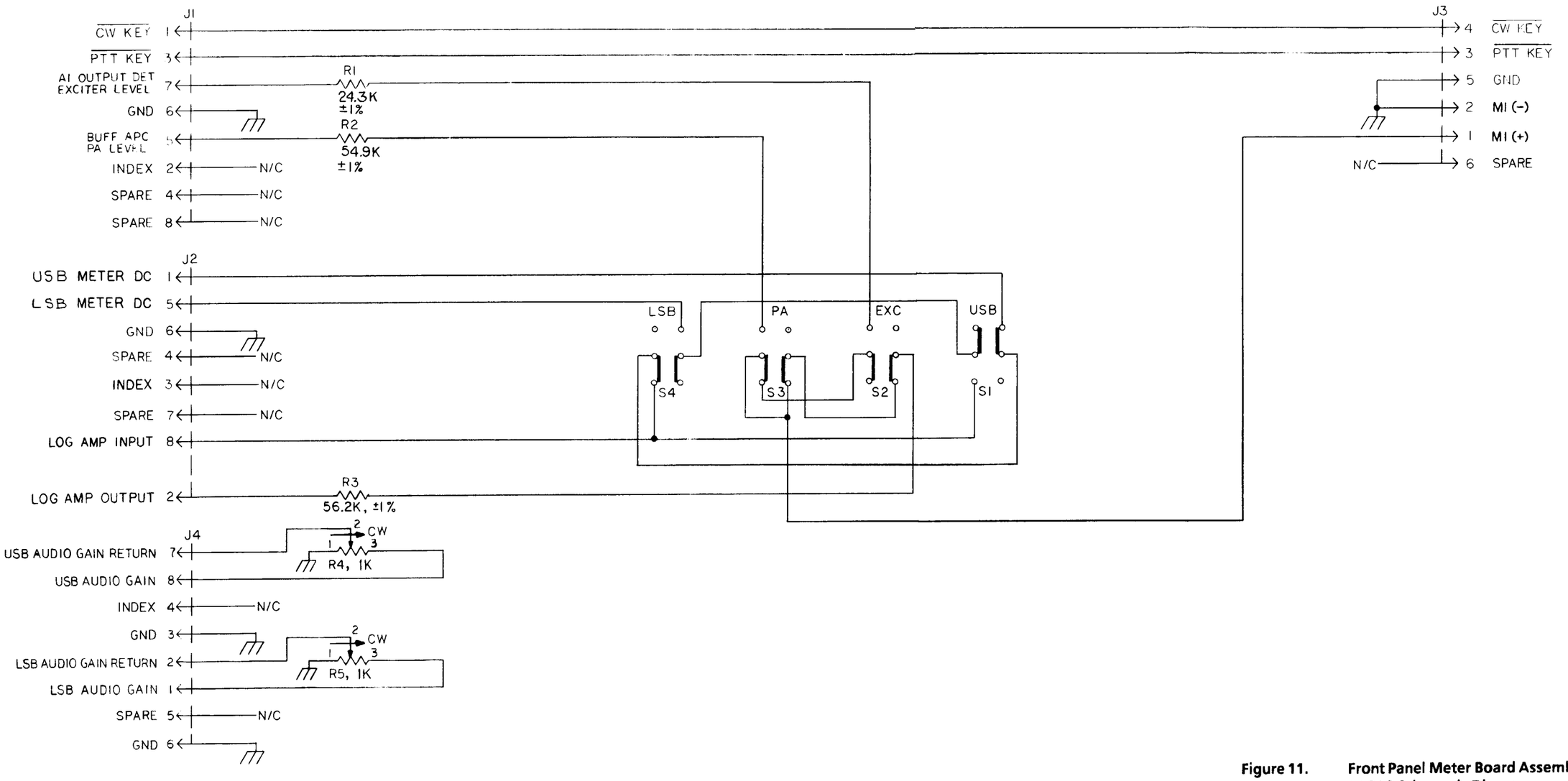


Figure 11. **Front Panel Meter Board Assembly A13A3 Schematic Diagram (10121-2301 Rev. D)**

5. FRONT PANEL ALPHANUMERIC DISPLAY ASSEMBLY A13A4

5.1 General Description

Front Panel Alphanumeric Display Assembly A13A4 consists of a single vacuum fluorescent display which contains twenty, fourteen-segment (British flag) characters. The alpha display provides indications of mode, carrier attenuation, audio source, and RF power attenuation. Additionally, the alphanumeric display is used to provide fault indications, if any, at the completion of the BITE test.

5.2 Interface Connections

Table 10 lists the A13A4 assembly interface connections.

Table 10. Front Panel Alphanumeric Display Assembly A13A4 Interface Connections

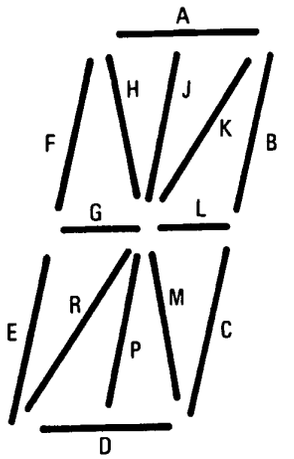
Connector	Description
J1 to/from A13A2	
J1-1	a Segment
J1-2	b Segment
J1-3	c Segment
J1-4	d Segment
J1-5	m Segment
J1-6	n Segment
J1-7	e Segment
J1-8	f Segment
J1-9	J Segment
J1-10	k Segment
J1-11	g Segment
J1-12	h Segment
J1-13	Decimal Point
J1-14	Comma
J1-15	N/C
J1-16	G1 Digit
J1-17	p Segment
J1-18	r Segment
J1-19	G2 Digit

Table 10. Front Panel Alphanumeric Display Assembly A13A4 Interface Connections (Cont.)

Connector	Description
J1-20	G3 Digit
J1-21	G20 Digit
J1-22	G4 Digit
J1-23	G5 Digit
J1-24	G6 Digit
J1-25	G19 Digit
J1-26	G7 Digit
J1-27	G8 Digit
J1-28	G9 Digit
J1-29	G18 Digit
J1-30	G10 Digit
J1-31	G11 Digit
J1-32	G12 Digit
J1-33	G17 Digit
J1-34	G13 Digit
J1-35	G14 Digit
J1-36	N/C
J1-37	G16 Digit
J1-38	G15 Digit
J1-39	Filament
J1-40	Filament

5.3 Functional Description

The alphanumeric vacuum fluorescent display is very similar in principle to the vacuum tube. Front Panel Driver Board A13A2 provides all required voltages and timing to properly drive the display. The 10073-2400 twenty-character VF display requires a 4.7 Vac filament voltage and 35 Vdc grid and anode voltages. The grids (20 of them) are essentially character enable signals which are driven in multiplexed fashion, enabled one at a time as the segment data for that character is provided to the anode pins. The anode pins are inputs for the 14 segments plus dot and comma signals. Figure 12 shows the display's segment location. See paragraphs 3.1 and 3.3.3 for additional details.



590-102

Figure 12. Alphanumeric Display Segment Location

5.3.1 Parts List and Schematic Diagram

Table 11 is the Front Panel Alphanumeric Display Assembly A13A4 parts list. Figures 13 and 14 are the Front Panel Alphanumeric Display Assembly A13A4 component location diagram and schematic diagram.

Table 11. Front Panel Alphanumeric Display Assembly A13A4 Parts List (10073-2420 Rev. -)

Ref. Desig.	Part Number	Description
DS1 J1	N50-0006-002 J46-0031-040	DSPL FLR VAC 14 SEG HDR 40 PIN 0.100"

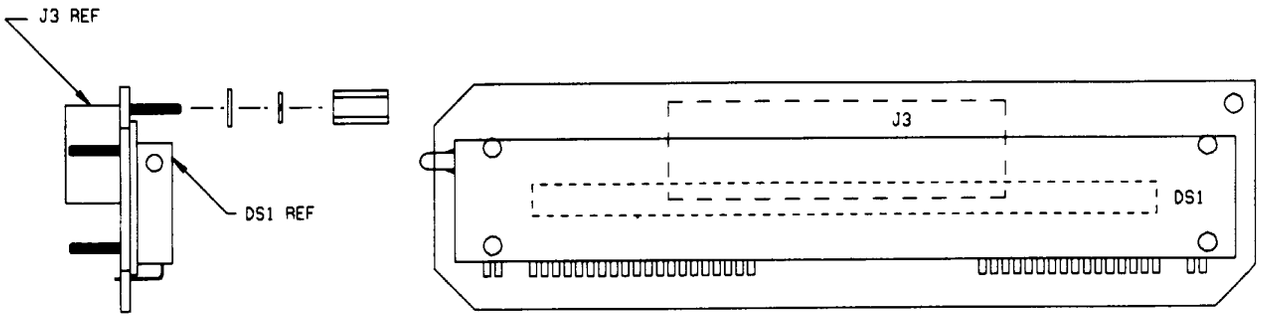


Figure 13. Front Panel Alphanumeric Display Assembly A13A4 Component Location Diagram (10073-2420 Rev. A)

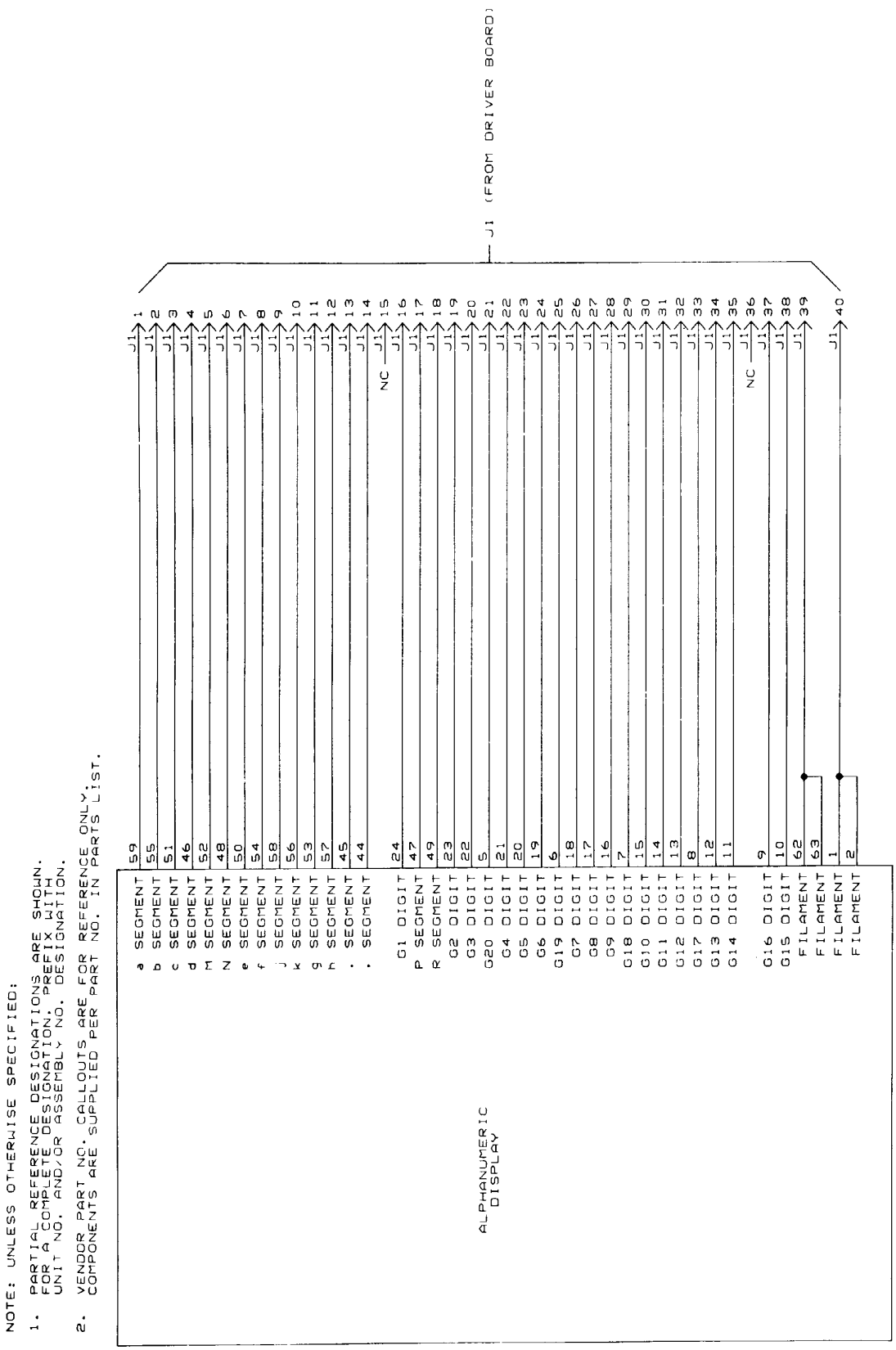


Figure 14. Front Panel Alphanumeric Display Board A13A4 Schematic Diagram (10073-2421 Rev. -)

6. FRONT PANEL NUMERIC DISPLAY ASSEMBLY A13A5

6.1 General Description

Front Panel Numeric Display Assembly A13A5 consists of a single vacuum fluorescent display which contains eight, seven-segment characters used for frequency display and two, seven-segment characters used for the channel display.

6.2 Interface Connections

Table 12 lists the A13A5 assembly interface connections.

Table 12. Front Panel Numeric Display Assembly A13A5 Interface Connections

Connector	Description
J1 to/from A13A2	
J1-1	G11 10 MHz Digit
J1-2	G10 1 MHz Digit
J1-3	G9 100 kHz Digit
J1-4	G3 1/2 Segments
J1-5	G7 1 kHz Digit
J1-6	G8 10 kHz Digit
J1-7	Filament
J1-8	Decimal Point
J1-9	G5 10 Hz Digit
J1-10	G6 100 Hz Digit
J1-11	N/C
J1-12	Comma
J1-13	G4 1 Hz Digit
J1-14	c Segment
J1-15	G2 CH10 Digit
J1-16	G1 CH1 Digit
J1-17	b Segment
J1-18	a Segment
J1-19	g Segment

Table 12. Front Panel Numeric Display Assembly A13A5 Interface Connections (Cont.)

Connector	Description
J1-20	Filament
J1-21	Underline Segments
J1-22	d Segment
J1-23	e Segment
J1-24	f Segment

6.3 Functional Description

The numeric vacuum fluorescent display is very similar in principle to the vacuum tube. Front Panel Driver Board A13A2 provides all required voltages and timing signals to properly drive the display. The 10073-2500 VF display operates by using a 5.8 Vac filament voltage and 35 Vdc grid and anode voltages. The grids (eleven of them; nine are used) are character enable signals which are driven in a multiplexed fashion. The grids are enabled one at a time as the seven segment data plus underline, if required, are provided to the anode pins. Each digit is enabled for approximately 600 to 700 microseconds. Figure 15 shows the display's segment's location.

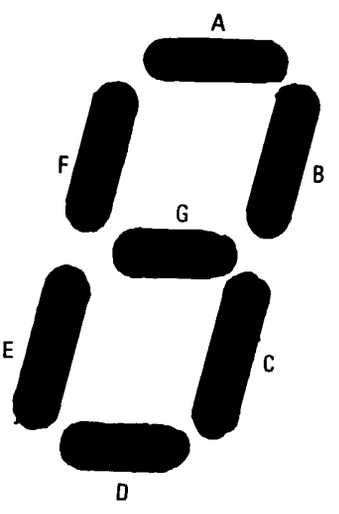


Figure 15. Numeric Display Segment Location

6.3.1 Parts List and Schematic Diagram

Table 13 is the Front Panel Numeric Display Assembly A13A5 parts list. Figures 16 and 17 are the Front Panel Numeric Display Assembly A13A5 component location diagram and schematic diagram.

Table 13. Front Panel Numeric Display Assembly A13A5 Parts List (10073-2500 Rev. C)

Ref. Desig.	Part Number	Description
DS1	N50-0005-001	DSPL FLR VAC 7SEG 11-DIG
J1	J46-0031-024	HDR 24 PIN 0.100" RT ANG

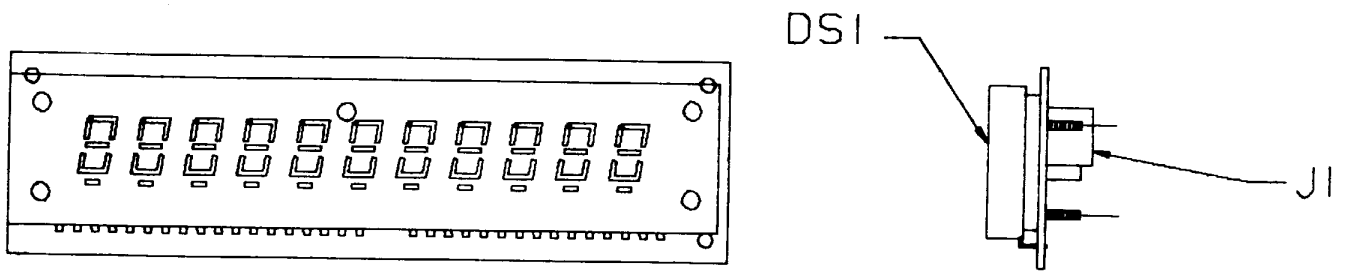


Figure 16. Front Panel Numeric Display Board A13A5 Component Location Diagram (10073-2500 Rev. B)

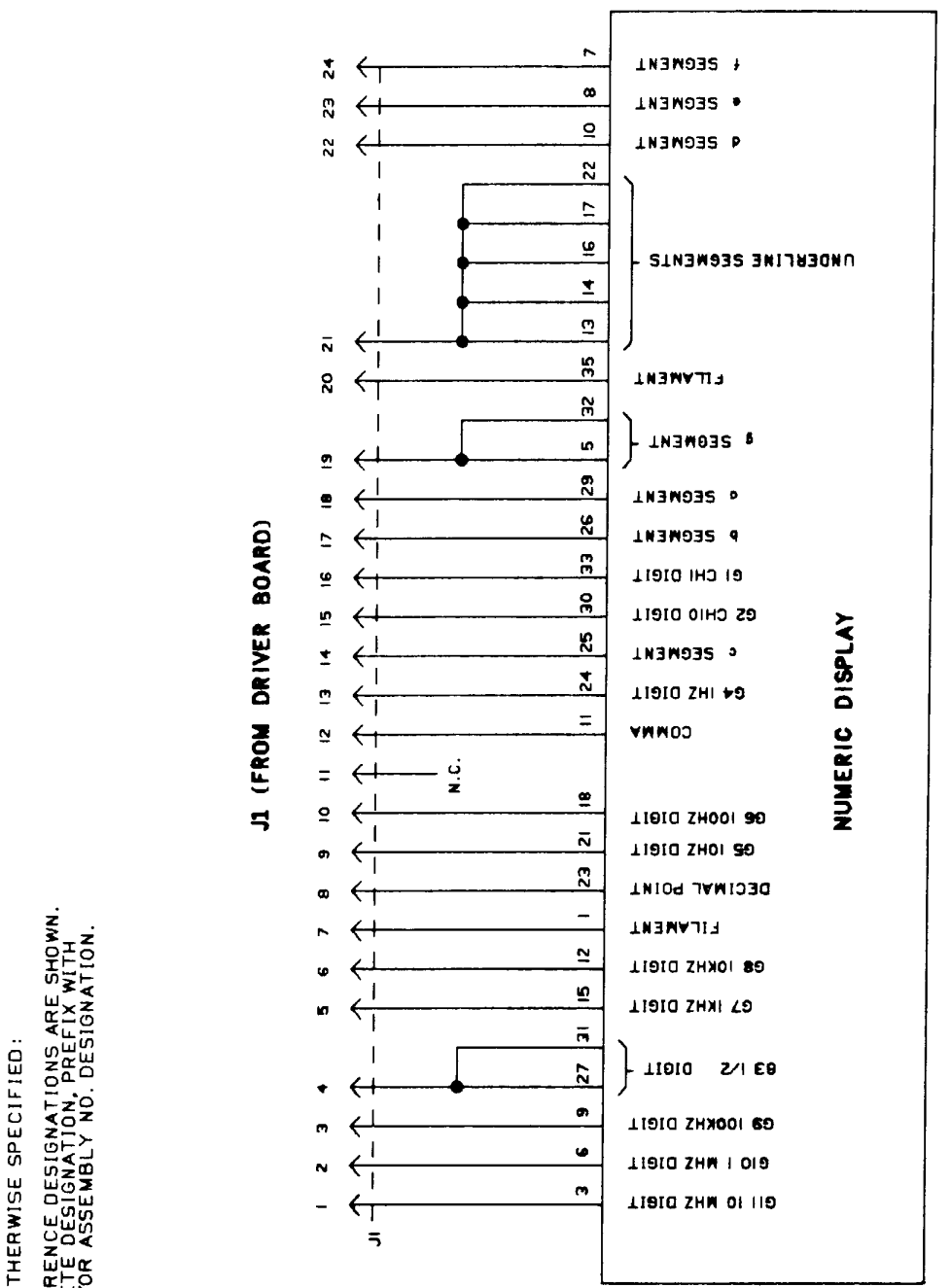


Figure 17. Front Panel Numeric Display Assembly A13A5 Schematic Diagram (10073-2501 Rev. B)

7. FRONT PANEL DISPLAY CONVERTER ASSEMBLY A13A6

7.1 General Description

Front Panel Display Converter Assembly A13A6 is a self contained dc-to-dc converter type power supply. It supplies anode and filament voltages to the A13A4 and A13A5 front panel vacuum fluorescent displays from the available -15 Vdc supply. Anode voltage output is 35 Vdc at 100 mA, and filament output voltage is 5.8 Vac at 200 mA.

The A13A6 assembly is a sealed unit (to provide EMI protection). Input/output connections to the internal A13A6A1 PWB is via feedthrough capacitors.

7.2 Circuit Description

The -15 Vdc is applied to push/pull square wave oscillator Q1 and Q2 operating at approximately 15 kHz. T1 is a saturating transformer used to provide feedback and two output voltages. One output is rectified by fullwave bridge CR2-CR5 and filtered by pi-network C2-L1-C3 to provide 35 Vdc at 100 mA for display anode power. The second output is filtered by L2, C5, T2, and C6 to provide 5.8 Vac at 200 mA for display filament power. A bias voltage of approximately 6 Vdc is also supplied to the filaments. This bias voltage originates on Front Panel Driver Board Assembly A13A2 and is applied via a center tap at T2.

7.2.1 Parts List and Schematic

Table 14 is the Front Panel Display Converter Assembly A13A6 parts list. Figure 18 is the Front Panel Display Converter Assembly A13A6 component location diagram. Table 15 is the Display Converter Board Assembly A13A6A1 parts list. Figure 19 is the Display Converter Board Assembly A13A6A1 component location diagram, and figure 20 is the A13A6 and A13A6A1 schematic diagram.

Table 14. Front Panel Display Converter Assembly A13A6 Parts List (10073-2250 Rev. J)

Ref. Desig.	Part Number	Description
A1	10073-2260	PWB ASSY, CONVERTER
C1	10073-7035	CAP,FEED-THRU 100
C2	10073-7035	CAP,FEED-THRU 100
C3	10073-7035	CAP,FEED-THRU 100
C4	10073-7035	CAP,FEED-THRU 100
C5	10073-7035	CAP,FEED-THRU 100
E1	E58-0004-000	LUG SLDR RIGHT ANGLE

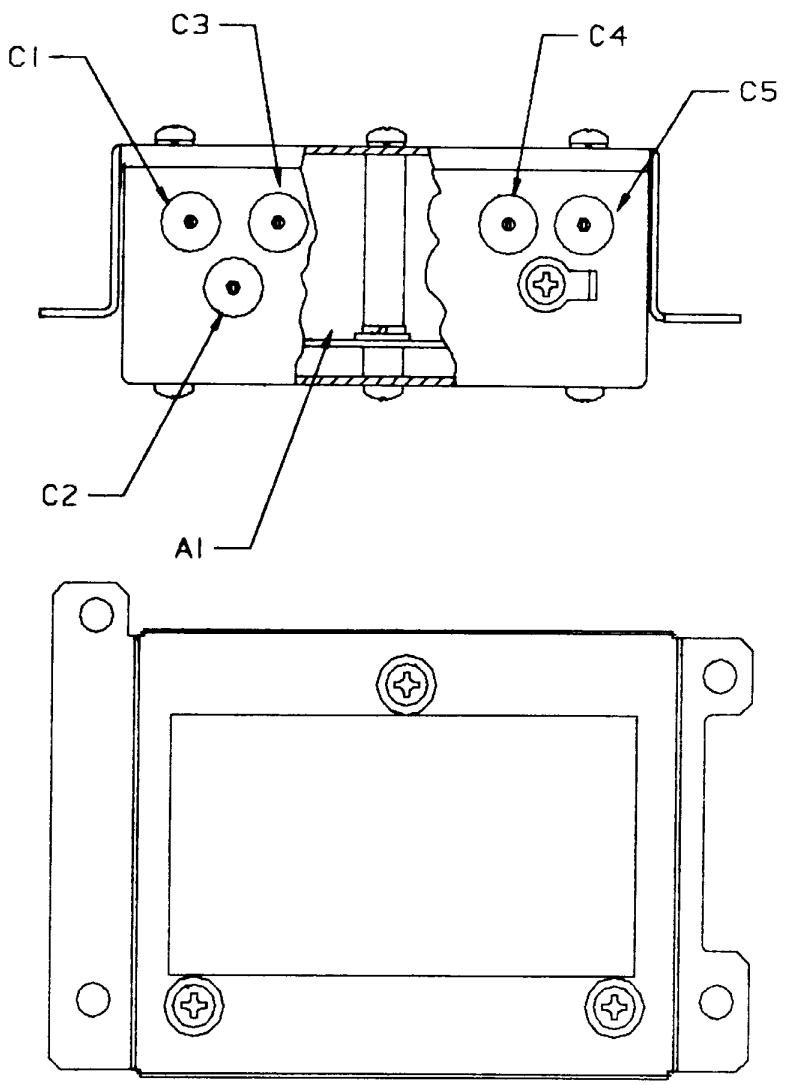


Figure 18. Front Panel Display Converter Assembly A13A6 Component Location Diagram (10073-2250 Rev. E)

Table 15. Display Converter Board Assembly A13A6A1 Parts List (10073-2260 Rev. T)

Ref. Desig.	Part Number	Description
C1	M39014/02-1305V	CAP .047UF 10% 100V CER-R
C2	C26-0050-100	CAP 10UF 20% 50V TANT
C3	C26-0050-100	CAP 10UF 20% 50V TANT
C4	C18-0035-101	CAP 100UF AXL 35V ELEC
C5	M39014/02-1318V	CAP .33UF 10% 50V CER-R
C6	M39014/02-1318V	CAP .33UF 10% 50V CER-R
C7	C26-0025-680	CAP 68UF 20% 25V TANT
CR1	1N4007	DIODE 1A 1000V RECT GP
CR2	1N4937	DIODE 1A 600V RECT GP
CR3	1N4937	DIODE 1A 600V RECT GP
CR4	1N4937	DIODE 1A 600V RECT GP
CR5	1N4937	DIODE 1A 600V RECT GP
CR6	1N4937	DIODE 1A 600V RECT GP
CR7	1N4937	DIODE 1A 600V RECT GP
L1	MS90538-12	COIL 100UH 5% FXD RF
L2	10073-7029	INDUCTOR, FILTER CHOKE
L3	10073-7029	INDUCTOR, FILTER CHOKE
Q1	2N5193	XSTR POWER PNP TO-205AA
Q2	2N5193	XSTR POWER PNP TO-205AA
R1	R65-0003-272	RES 2.7K 5% 1/4W CAR FILM
R2	R65-0003-270	RES 27 5% 1/4W CAR FILM
R3	R65-0003-101	RES 100 5% 1/4W CAR FILM
R4	R65-0003-223	RES 22K 5% 1/4W CAR FILM
T1	10073-7027	TRANSFORMER, POWER
T2	10073-7028	TRANSFORMER, RF, FIXED

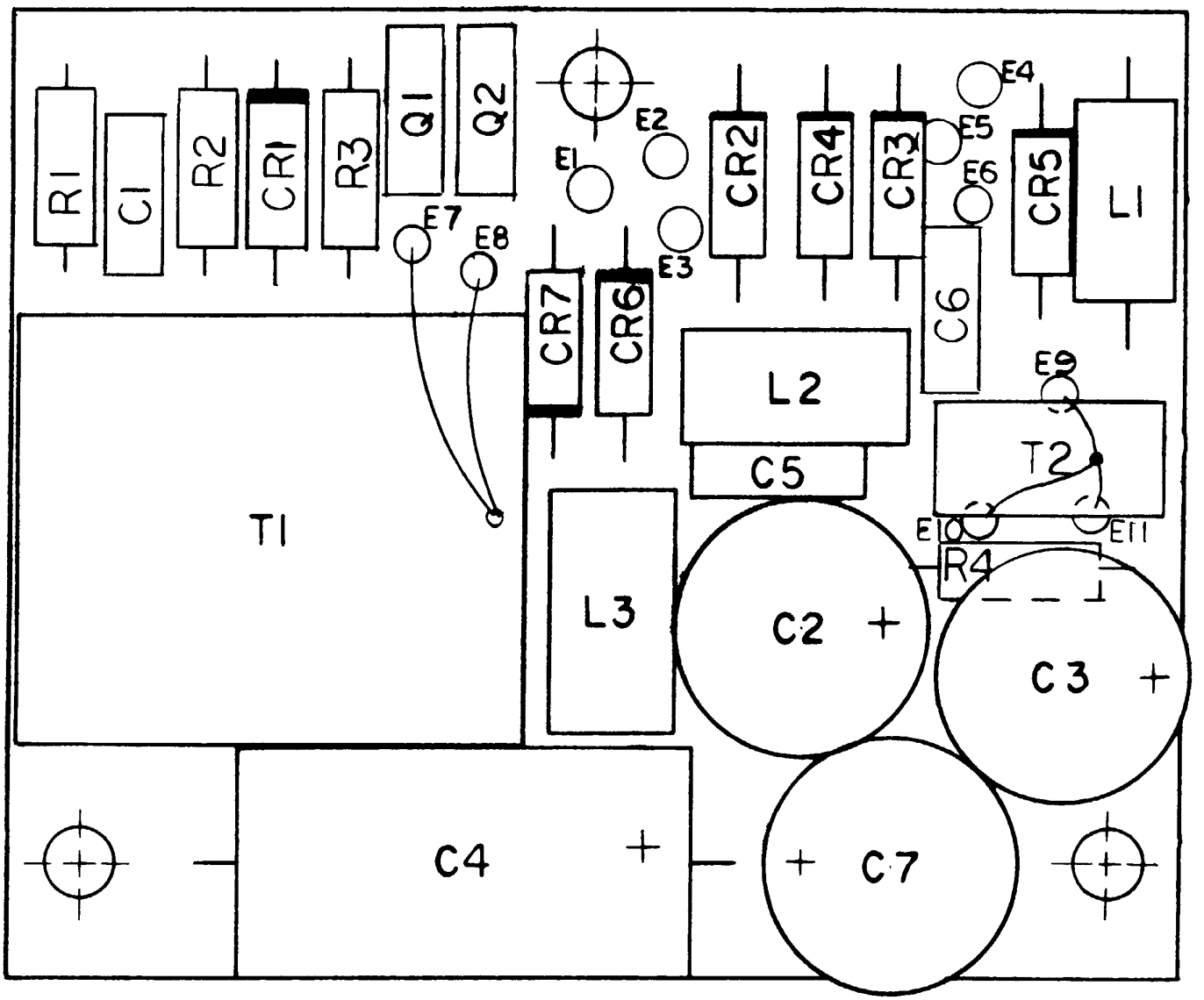


Figure 19. Display Converter Board Assembly A13A6A1 Component Location Diagram (10073-2260 Rev. D)

NOTE: UNLESS OTHERWISE SPECIFIED:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR A COMPLETE DESIGNATION, PREFIX WITH UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.
2. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, ±5%.
3. ALL CAPACITOR VALUES ARE IN MICROFARADS.
4. VENDOR PART NO. CALLOUTS ARE FOR REFERENCE ONLY. COMPONENTS ARE SUPPLIED PER PART NO. IN PARTS LIST.

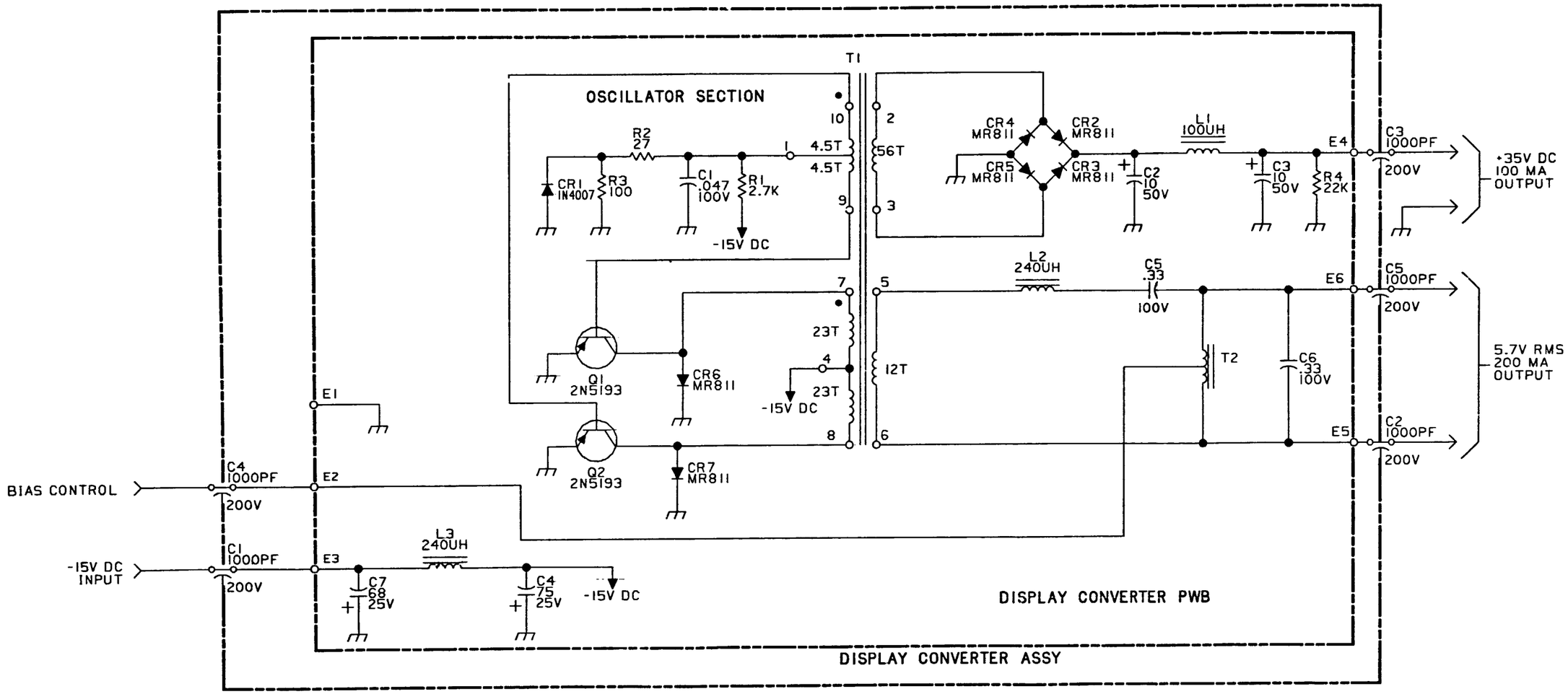


Figure 20. Front Panel Display Converter Assembly A13A6 and Display Converter Board Assembly A13A6A1 Schematic Diagram (10073-2251 Rev. F)

8. MICROPHONE ASSEMBLY A13A7

8.1 General Description

Microphone Assembly A13A7 includes the front panel microphone jack and three simple LC filter circuits. Filtering is provided for the AUDIO, CW KEY, and PTT signals. Two connectors on the PWB accept cables that carry the AUDIO signal to the A5A1 assembly and the CW KEY and PTT signals to the A13A3 assembly.

8.2 Interconnection

The interconnections of the A13A7 assembly with the other assemblies in the exciter are summarized in table 16.

Table 16. Microphone Assembly A13A7 Interconnections

Connector and Pin	Signal Name	Description
J1-A	GND	Ground
J1-B	N/C	Not connected
J1-C	PTT	PTT key signal
J1-D	AUDIO	Microphone audio in
J1-E	CW KEY	CW key signal
J1-F	N/C	Not connected
J2-1	GND	Ground
J2-2	INDEX KEY	Connector alignment key
J2-3	CW KEY	CW key signal to Meter Board
J2-4	PTT	PTT key signal to Meter Board
J3-1	AUDIO	Audio to A5A1 assembly (-56 dB nominal)
J3-2	AUDIO KEY	Audio ground
J3-3	INDEX KEY	Connector alignment key

8.3 Circuit Description

Microphone Assembly A13A7 circuit includes three separate LC filters; one each for the AUDIO, CW KEY, and PTT signals.

8.4 Parts List, Component Locations, and Schematic Diagram

All replaceable components of the microphone Assembly A13A7 are listed in table 17. Component locations are shown in figure 21. The Microphone Assembly schematic diagram is shown in figure 22.

Table 17. Microphone Assembly A13A7 Parts List (10121-2900 Rev. E)

Ref. Desig.	Part Number	Description
C1	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C2	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C3	M39014/02-1310V	CAP .1UF 10% 100V CER-R
J1	J-0339	CONN AUDIO 6 PIN
J2	J46-0022-004	HDR 4 PIN 0.100" SR LKG
J3	J46-0022-004	HDR 4 PIN 0.100" SR LKG
L1	MS75085-8	COIL 120UH 10% FXD RF
L2	MS75085-2	COIL 39UH 10% FXD RF
L3	MS75085-2	COIL 39UH 10% FXD RF

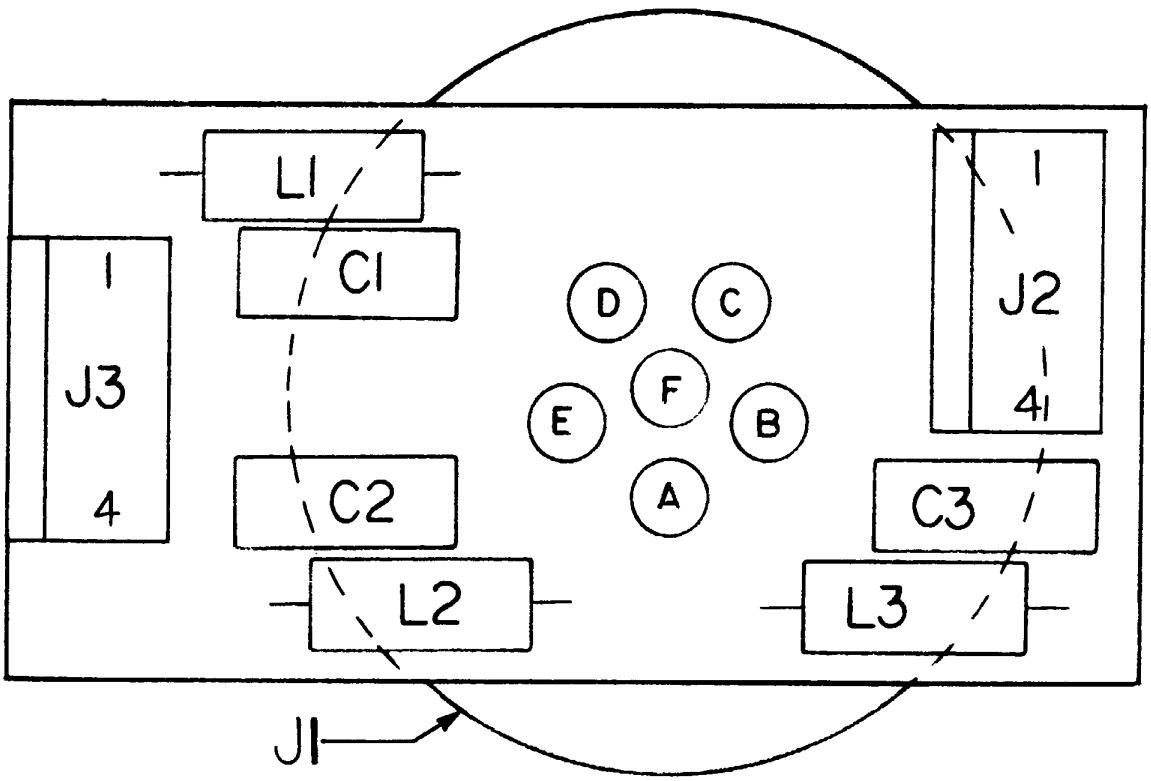


Figure 21. Microphone Assembly A13A7 Component Locations Diagram (10121-2900 Rev. D)

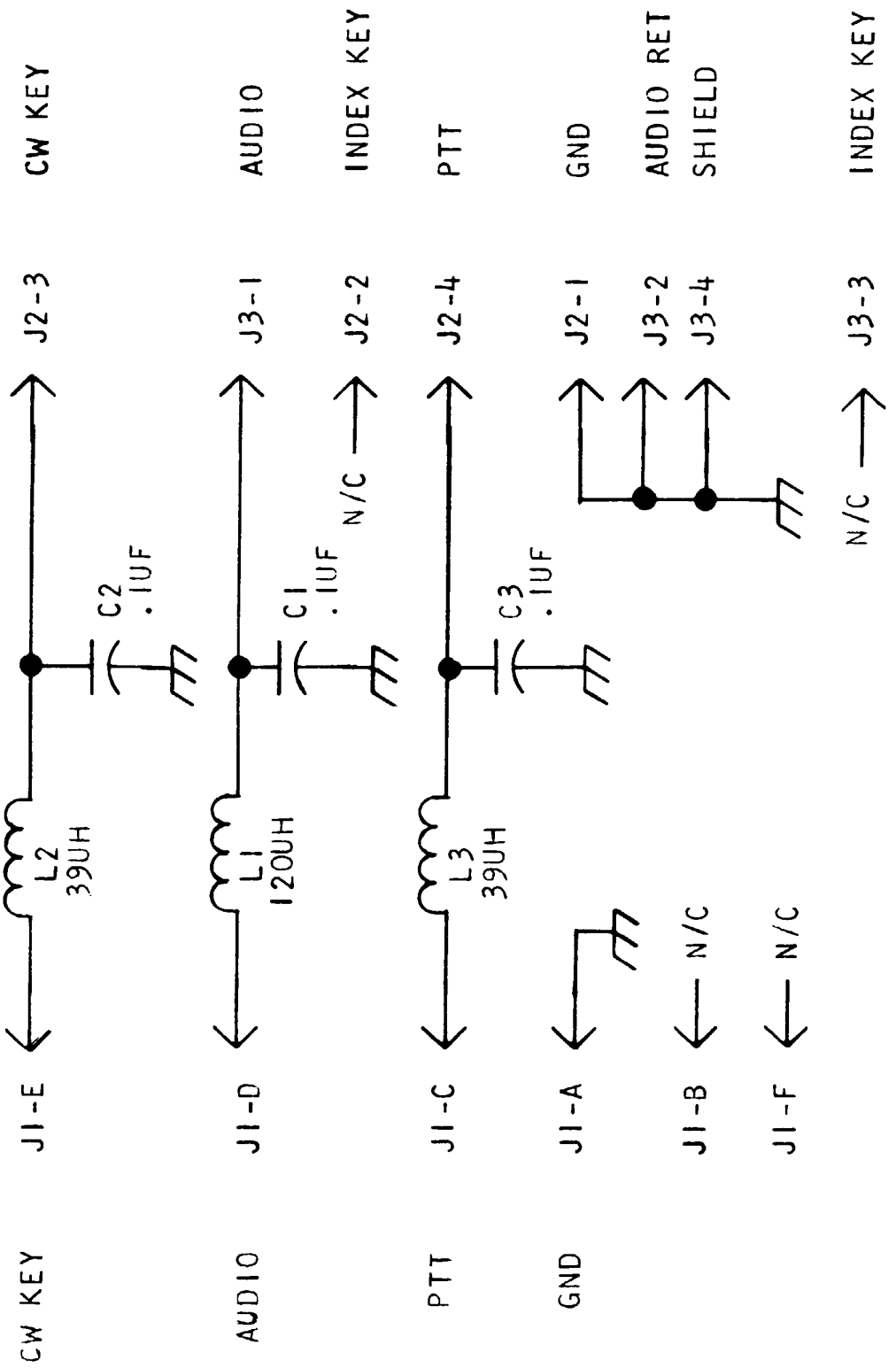


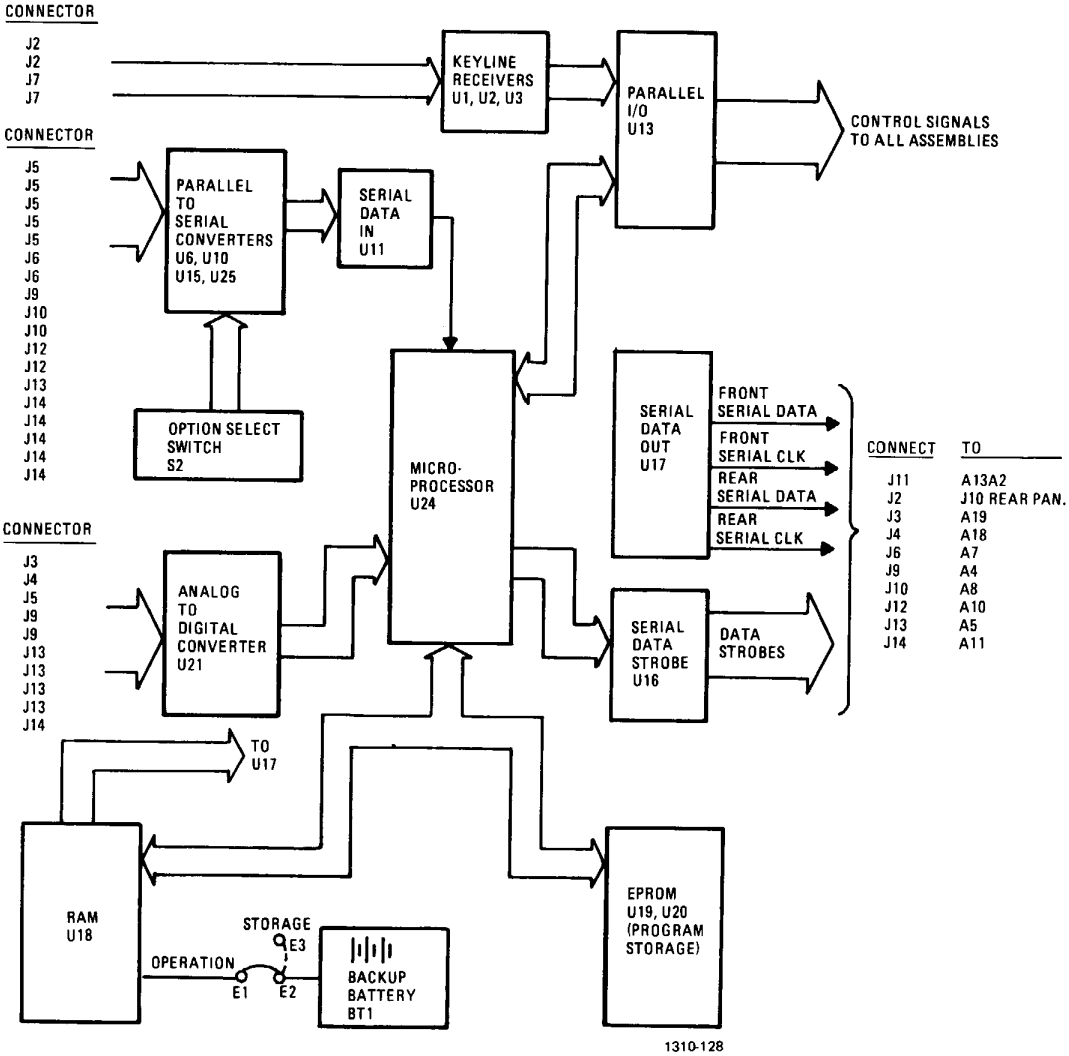
Figure 22. Microphone Assembly A13A7 Schematic Diagram (10121-2901 Rev. B)

A14
CONTROL BOARD ASSEMBLY

SIG	FROM	CONNECTOR
AUX PTT	J10	J2
AUX CW	J10	J2
PTT KEY	A13A3	J7
CW KEY	A13A3	J7

SIG	FROM	CONNECTOR
PLL 1 LOCK	A6	J5
PLL 4 LOCK	A9	J5
800 KHZ DET	A12	J5
1 MHZ DET	A12	J5
40 MHZ DET	A12	J5
PLL 2 LOCK	A7	J6
PLL 2 SER CHK	A7	J6
A4 SER CHK	A4	J9
PLL 3 LOCK	A8	J10
PLL 3 SER CHK	A8	J10
PLL 5 LOCK	A10	J12
PLL 5 SER CHK	A10	J12
A5 SER CHK	A5	J13
A11 45 MHZ LOCK	A11	J14
A11 LOCK DET 1	A11	J14
A11 LOCK DET 2	A11	J14
A11 SER CHK 1	A11	J14
A11 SER CHK 2	A11	J14

SIG	FROM	CONNECTOR
FILTER I.D.	A19	J3
A1 OUTPUT DET	A1	J4
A2 BITE DET	A2	J5
IF ENVELOPE	A4	J9
COMBINER I.D.	A4	J9
USB ALC BITE	A5	J13
LSB ALC BITE	A5	J13
USB IF BITE	A5	J13
LSB IF BITE	A5	J13
A11 BITE DET	A11	J14



CONNECT	TO
J11	A13A2
J2	J10 REAR PAN.
J3	A19
J4	A18
J6	A7
J9	A4
J10	A8
J12	A10
J13	A5
J14	A11

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CONTROL BOARD ASSEMBLY A14

1. GENERAL DESCRIPTION

Control Board Assembly A14 contains the 8085AH-2 CPU and associated peripheral circuits, serial data transmission circuits, parallel-to-serial reception circuits, parallel I/O circuits, keyline processing circuits, and analog-to-digital converter circuitry. The A14 assembly controls the RF-1310, accepts input from the front panel and exciter assemblies, and generates the digital signals necessary to control the exciter. Software contained within two, 16K byte EPROMs is executed to supervise, control, and in the BITE process, test the display, control, and signal generating circuitry. Random access read/write memory (RAM) is used to temporarily store the software program and store battery-backed exciter setups and programmed channels. Figure 1 shows the location of this assembly.

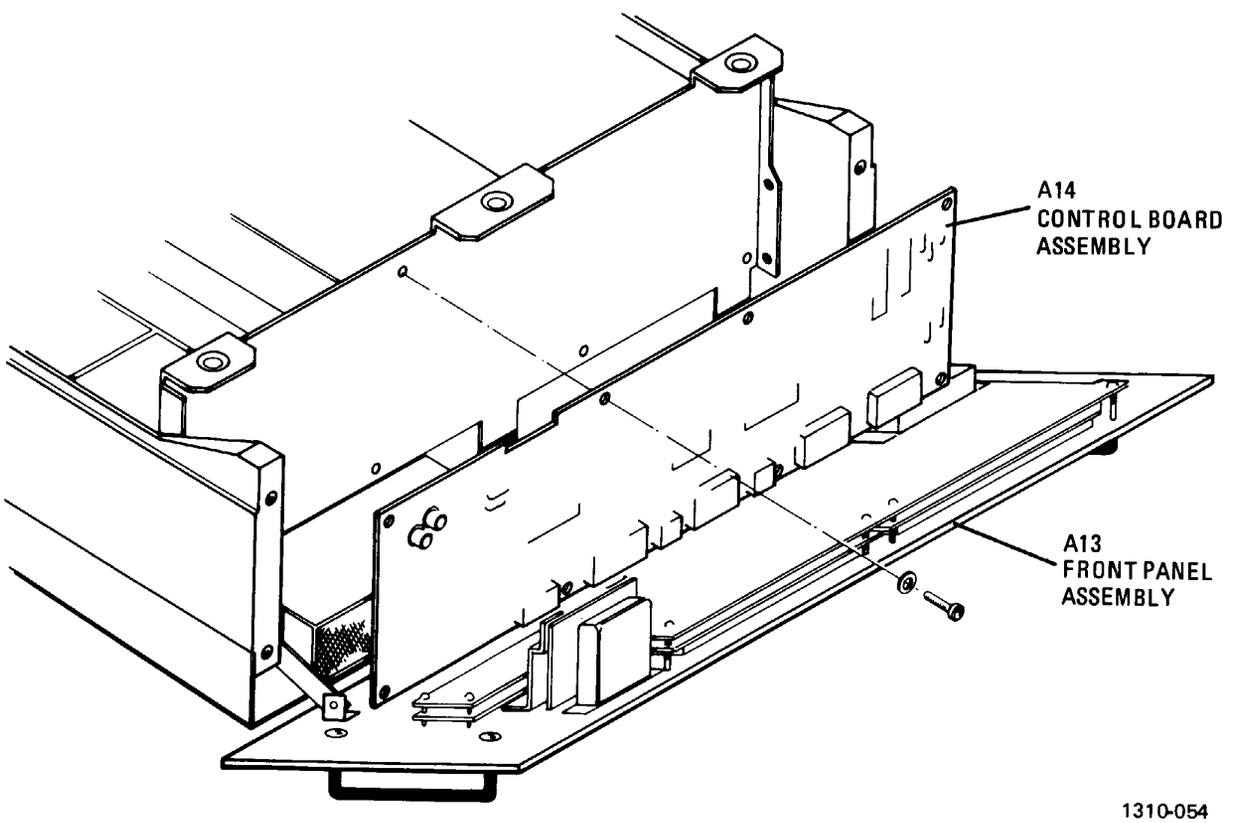


Figure 1. Control Board Assembly Exploded View

2. INTERFACE CONNECTIONS

All Control Board Assembly A14 interface connections are shown in table 1 and on the schematic diagram.

Table 1. RF-1310 Control Board Interface Lines

Connector	Function	To	From
A14J1	NC	----	----
A14J1-2	INDEX	----	----
A14J1-3	CONTROL + 5 V	----	A15J3-21
A14J1-4	DISPLAY + 5 V	----	A15J3-9
A14J2-1	$\overline{\text{AUXILIARY PTT KEY}}$	J10-7	----
A14J2-2	$\overline{\text{AUXILIARY CW KEY}}$	J10-9	----
A14J2-3	4 ISB MODE CMD	J10-2	----
A14J2-4	4 ISB ID	----	J10-20
A14J2-5	PRI FAIL	J10-19	----
A14J2-6	REMOTE OUT 0	J10-16	----
A14J2-7	REMOTE OUT 1	J10-31	----
A14J2-8	4 ISB BITE RESULT	----	J10-5
A14J2-9	FAULT	J10-4	----
A14J2-10	4 ISB BITE CMD	J10-30	----
A14J2-11	REAR SERIAL CLOCK	J10-3	----
A14J2-12	REAR SERIAL DATA	J10-1	----
A14J2-13	BUFFERED SERIAL ENABLE 1	J10-18	----
A14J2-14	BUFFERED SERIAL ENABLE 2	J10-32	----
A14J3-1	SPARE	----	----
A14J3-2	FILTER, ID	----	A19J1-9
A14J3-3	SPARE	----	----
A14J3-4	SPARE	----	----
A14J3-5	SPARE	----	----
A14J3-6	INDEX	----	----
A14J3-7	EXTERNAL MUTE	----	A19J1-4
A14J3-8	SERIAL ENABLE	A19J1-3	----
A14J3-9	REAR SERIAL DATA	A19J1-2	----
A14J3-10	REAR SERIAL CLOCK	A19J1-1	----
A14J4-1	$\overline{\text{CW KEY}}$	A18A1J2-1	----
A14J4-2	$\overline{\text{PTT KEY}}$	A18A1J2-2	----
A14J4-3	$\overline{\text{RESET}}$	A18A1J2-3	----
A14J4-4	GROUND	A18A1J2-4	----
A14J4-5	FSK SHIFT	----	A18A1J2-5
A14J4-6	PRI FAIL	----	A18A1J2-6
A14J4-7	IF ENVELOPE	A18A1J2-7	----
A14J4-8	REAR SERIAL CLOCK	A18A1J2-8	----
A14J4-9	REAR SERIAL DATA	A18A1J2-9	----
A14J4-10	SPARE	----	----

Table 1. RF-1310 Control Board Interface Lines (Cont.)

Connector	Function	To	From
A14J4-11	SERIAL ENABLE	A18A1J2-11	----
A14J4-12	SERIAL DATA IN	----	A18A1J2-12
A14J4-13	SPARE	----	----
A14J4-14	$\overline{\text{INTERNAL KEY}}$	A18A1J2-14	----
A14J4-15	BUSY	----	A18A1J2-15
A14J4-16	A1 OUTPUT DETECT	----	A18A1J2-16
A14J4-17	$\overline{\text{READ SELECT}}$	A18A1J2-17	----
A14J4-18	ATTNC	----	A18A1J2-18
A14J4-19	PPC CONTROL	----	A18A1J2-19
A14J4-20	BUFFERED APC	----	A18A1J2-20
A14J5-1	A2 BITE DET	----	A2J6-1
A14J5-2	NC	----	----
A14J5-3	A6 PLL 1 LOCK	----	A16A3J1-1
A14J5-4	INDEX	----	----
A14J5-5	A9 PLL 4 LOCK	----	A16A3J1-3
A14J5-6	A12 800 KHZ BITE DET	----	A16A3J1-4
A14J5-7	A12 1 MHZ BITE DET	----	A16A3J1-5
A14J5-8	A12 40 MHZ BITE DET	----	A16A3J1-6
A14J6-1	REAR SERIAL DATA	A7J1-10	----
A14J6-2	REAR SERIAL CLOCK	A7J1-9	----
A14J6-3	INDEX	----	----
A14J6-4	PLL 2 SERIAL CHECK	----	A7J1-7
A14J6-5	SERIAL ENABLE	A7J1-6	----
A14J6-6	PLL 2 LOCK	----	A7J1-5
A14J6-7	GROUND	A7J1-4	----
A14J6-8	SPARE	----	----
A14J7-1	$\overline{\text{CW KEY}}$	----	A13A3J1-1
A14J7-2	INDEX	----	----
A14J7-3	$\overline{\text{PTT KEY}}$	----	A13A3J1-3
A14J7-4	SPARE	----	----
A14J7-5	BUFFERED APC	A13A3J1-5	----
A14J7-6	GROUND	A13A3J1-6	----
A14J7-7	A1 OUTPUT DET	A13A3J1-7	----
A14J7-8	SPARE	----	----
A14J8-1	POWER SUPPLY BITE	----	A15J3-22
A14J8-2	SPARE	----	----
A14J8-3	+ 15 V REGULATED	----	A15J3-23
A14J8-4	-15 V REGULATED	----	A15J3-11
A14J8-5	INDEX	----	----
A14J8-6	+ 5 V UNREGULATED	----	A15J3-12
A14J8-7	GROUND	----	A15J3-25
A14J8-8	GROUND	----	A15J3-13

Table 1. RF-1310 Control Board Interface Lines (Cont.)

Connector	Function	To	From
A14J9-1	REAR SERIAL DATA	A4J6-1	----
A14J9-2	REAR SERIAL CLOCK	A4J6-2	----
A14J9-3	A4 SERIAL CHECK	----	A4J6-3
A14J9-4	SERIAL ENABLE	A4J6-4	----
A14J9-5	IF ENVELOPE	----	A4J6-5
A14J9-6	PPC CONTROL	A4J6-6	----
A14J9-7	$\overline{\text{INTERNAL KEY}}$	A4J6-7	----
A14J9-8	GROUND	A4J6-8	----
A14J9-9	INDEX	----	----
A14J9-10	COMBINER ID	A4J6-12	----
A14J9-11	SPARE	----	----
A14J9-12	NC	----	----
A14J10-1	REAR SERIAL DATA	A8J4-10	----
A14J10-2	REAR SERIAL CLOCK	A8J4-9	----
A14J10-3	INDEX	----	----
A14J10-4	PLL 3 SERIAL CHECK	----	A8J4-7
A14J10-5	SERIAL ENABLE	A8J4-6	----
A14J10-6	PLL 3 LOCK	----	A8J4-5
A14J10-7	GROUND	A8J4-4	----
A14J10-8	SPARE	----	----
A14J11-1	NC	----	----
A14J11-2	FRONT SERIAL DATA	A13A2J1-2	----
A14J11-3	NC	----	----
A14J11-4	FRONT SERIAL CLOCK	A13A2J1-4	----
A14J11-5	NC	----	----
A14J11-6	-15 V	A13A2J1-6	----
A14J11-7	DISPLAY +5 V	A13A2J1-7	----
A14J11-8	POWER SUPPLY BITE	A13A2J1-8	----
A14J11-9	PB3	A13A2J1-9	----
A14J11-10	KEYBOARD STROBE	A13A2J1-10	----
A14J11-11	PB2	A13A2J1-11	----
A14J11-12	FAULT	----	A13A2J1-12
A14J11-13	PB1	A13A2J1-13	----
A14J11-14	DISPLAY STROBE	A13A2J1-14	----
A14J11-15	PB0	A13A2J1-15	----
A14J11-16	$\overline{\text{RESET}}$	A13A2J1-16	----
A14J11-17	NC	----	---
A14J11-18	GROUND	A13A2J1-18	----
A14J11-19	+5 V UNREGULATED	A13A2J1-19	----
A14J11-20	GROUND	A13A2J1-20	----
A14J12-1	REAR SERIAL DATA	A10J1-10	----
A14J12-2	REAR SERIAL CLOCK	A10J1-9	
A14J12-3	INDEX	----	----
A14J12-4	PLL 5 SERIAL CHECK	----	A10J1-7
A14J12-5	SERIAL ENABLE	A10J1-6	----

Table 1. RF-1310 Control Board Interface Lines (Cont.)

Connector	Function	To	From
A14J12-6	PLL 5 LOCK	----	A10J1-5
A14J12-7	GROUND	A10J1-4	----
A14J12-8	SPARE	----	----
A14J13-1	REAR SERIAL DATA	A5A1J3-24	----
A14J13-2	REAR SERIAL CLOCK	A5A1J3-23	----
A14J13-3	A5 SERIAL CHECK	----	A5A1J3-22
A14J13-4	SERIAL ENABLE	A5A1J3-21	----
A14J13-5	SPARE	----	----
A14J13-6	USB ALC BITE DET	----	A5A1J3-19
A14J13-7	USB IF BITE DET	----	A5A1J3-18
A14J13-8	LSB ALC BITE DET	----	A5A1J3-17
A14J13-9	LSB IF BITE DET	----	A5A1J3-16
A14J13-10	REM LINE AUDIO GRD	A5A1J3-15	----
A14J13-11	SPARE	----	----
A14J13-12	REMOTE LINE AUDIO	A5A1J3-13	----
A14J13-13	SPARE	----	----
A14J13-14	$\overline{\text{VOX KEYLINE}}$	A5A1J3-11	----
A14J13-15	GROUND	A5A1J3-10	----
A14J13-16	FM AUDIO	A5A1J3-9	----
A14J13-17	SPARE	----	----
A14J13-18	-15 V	A5A1J3-7	----
A14J13-19	$\overline{\text{INTERNAL KEY}}$	A5A1J3-6	----
A14J13-20	+ 15 V	A5A1J3-5	----
A14J13-21	SPARE	----	----
A14J13-22	CLIP ENABLE	A5A1J3-3	----
A14J13-23	SPARE	----	----
A14J13-24	SPARE	----	----
A14J14-1	GROUND	A11A1J3-1	----
A14J14-2	SPARE	----	----
A14J14-3	A11 BITE DET	----	A11A1J3-3
A14J14-4	REAR SERIAL DATA	A11A1J3-4	----
A14J14-5	SERIAL ENABLE 1	A11A1J3-5	----
A14J14-6	REAR SERIAL CLOCK	A11A1J3-6	----
A14J14-7	A11 45 MHZ LOCK	----	A11J3-7
A14J14-8	FSK SHIFT	A11A1J3-8	----
A14J14-9	INTERNAL KEY	A11A1J3-9	----
A14J14-10	FM AUDIO	A11A1J3-10	----
A14J14-11	A11 LOCK DET 1	----	A11A1J3-11
A14J14-12	SPARE	----	----
A14J14-13	SERIAL ENABLE 2	A11A1J3-13	----
A14J14-14	A11 SERIAL CHECK 1	----	A11A1J3-14
A14J14-15	A11 LOCK DET 2	----	A11A1J3-15
A14J14-16	A11 SERIAL CHECK 2	----	A11A1J3-16
A14J15-1	+ 5 V UNREGULATED	A17A1J1-1	----

Table 1. RF-1310 Control Board Interface Lines (Cont.)

Connector	Function	To	From
A14J15-2	+ 5 V UNREGULATED	A17A1J1-2	----
A14J15-3	RESET OUT	A17A1J1-3	----
A14J15-4	HOLD	----	A17A1J1-4
A14J15-5	REMOTE LINE AUDIO	A17A1J1-5	----
A14J15-6	HLDA	A17A1J1-6	----
A14J15-7	REMOTE LINE AUDIO GROUND	A17A1J1-7	----
A14J15-8	CLOCK OUT	A17A1J1-8	----
A14J15-9	+ 15 V	A17A1J1-9	----
A14J15-10	GROUND	A17A1J1-10	----
A14J15-11	READY	----	A17A1J1-11
A14J15-12	-15 V	A17A1J1-12	----
A14J15-13	RST 5.5	----	A17A1J1-13
A14J15-14	IO/$\overline{M}$	A17A1J1-14	----
A14J15-15	INTR	----	A17A1J1-15
A14J15-16	S1	A17A1J1-16	----
A14J15-17	$\overline{WR}$	A17A1J1-17	----
A14J15-18	$\overline{RD}$	A17A1J1-18	----
A14J15-19	$\overline{INTA}$	A17A1J1-19	----
A14J15-20	ALE	A17A1J1-20	----
A14J15-21	NC	----	----
A14J15-22	NC	----	----
A14J15-23	AD0	A17A1J2-3	BIDIRECTIONAL
A14J15-24	NC	----	BIDIRECTIONAL
A14J15-25	AD1	A17A1J2-5	BIDIRECTIONAL
A14J15-26	A15	A17A1J2-6	----
A14J15-27	AD2	A17A1J2-7	BIDIRECTIONAL
A14J15-28	A14	A17A1J2-8	----
A14J15-29	AD3	A17A1J2-9	BIDIRECTIONAL
A14J15-30	A13	A17A1J2-10	----
A14J15-31	AD4	A17A1J2-11	BIDIRECTIONAL
A14J15-32	A12	A17A1J2-12	----
A14J15-33	AD5	A17A1J2-13	BIDIRECTIONAL
A14J15-34	A11	A17A1J2-14	----
A14J15-35	AD6	A17A1J2-15	BIDIRECTIONAL
A14J15-36	A10	A17A1J2-16	----
A14J15-37	AD7	A17A1J2-17	BIDIRECTIONAL
A14J15-38	A9	A17A1J2-18	----
A14J15-39	GROUND	A17A1J2-19	----
A14J15-40	A8	A17A1J2-20	----
A14J16-1	$\overline{AUX\ PTT\ KEY}$	A3J2-1	----
A14J16-2	$\overline{AUX\ CW\ KEY}$	A3J2-2	----
A14J16-3	$\overline{NORM}$/REV FSK SENSE	A3J2-3	----
A14J16-4	KEYER ID	----	A3J2-4
A14J16-5	SERIAL DATA	A3J2-5	----
A14J16-7	SERIAL ENABLE	A3J2-7	----
A14J16-8	SPARE	----	----
A14J16-9	SPARE	----	----
A14J16-10	CW MODE	A3J2-10	----

3. FUNCTIONAL DESCRIPTION

3.1 CPU and Interface

Figure 2 is a functional block diagram of the Control Board Assembly A14. The U24 8085AH-2 microprocessor executes the application program. The 6.0 MHz frequency of crystal Y1 is divided-by-two within U24 to yield the 3.0 MHz processor timing (333 nanosecond cycle time). This 3.0 MHz signal is further divided by binary counter U8 and divide-by-12 counter U9 to produce the real time clock frequency of 977 Hz and the A-to-D clock frequency of 750 kHz. The high order address bits, RD, WR, and IO/$\overline{M}$ pulses of the CPU are inputs to the PAL U28, which functions as an address decoder to produce the active low chip selects to peripheral circuits. The multiplexed low address/data (AD) bus from U24 is input to low address latch U22 and to the data bus transceiver U23.

The control lines RD and WR are buffered by two gates of U26, and the interrupt line is gated through U29 to control the enabling of U23. As mentioned earlier, the RD and WR signals are combined with several of the enable outputs of U30 as well as U26 to produce chip selects for various chips and control serial data operations. The major outputs of the microprocessor are also run to connector J15 for access to the installed remote, with R31, R32, R36, and R37 holding the lines at their proper logic levels. Lines of address and data busses are pulled up through resistor pack R26 and R25, respectively. The active high interrupt lines of the CPU are dedicated as follows:

- RST 7.5 uses the real-time clock
- RST 6.5 is used by the system interface assembly
- RST 5.5 is used by the remote control option

3.2 Reset and Trap

When the power is turned on, the RC network (formed by R38 and C31) holds the processor RESET IN input low for about 100 milliseconds. This allows the power supplies time to stabilize before the CPU starts running. Diode CR9 and Q4 detect a falling + 5 V supply and pull the RESET IN input low to avoid spurious operation on exciter power down or loss. At such times, the chip select to the CMOS RAM U18 is disabled (FET Q2), before the RAM enters its battery-backed condition.

During normal program execution, the microprocessor SOD output sends a low active pulse to the retriggerable one-shot U27 every millisecond. If the CPU is affected by noise on the busses or some other failure, the one-shot will time out and restart the microprocessor through the 8085AH-2 TRAP input. Components C34 and R43 set this one-shot timeout to 50 milliseconds. The one-shot is also reset on powerup.

3.3 Memory

The firmware program is stored in two, 27128 16K byte EPROMs, U19 and U20. The program steps and data contained in these devices are accessed by the chip selects from U28 to each EPROM, gated onto the data bus with an output enable from the RD signal.

The information stored in the EPROMs is part of the RF-1310 software and cannot be altered by the customer.

CAUTION

EPROMs are ultraviolet erasable over extended periods of exposure to fluorescent light or sunlight which can erase the memory information. Do not remove the opaque protective shield on these devices.

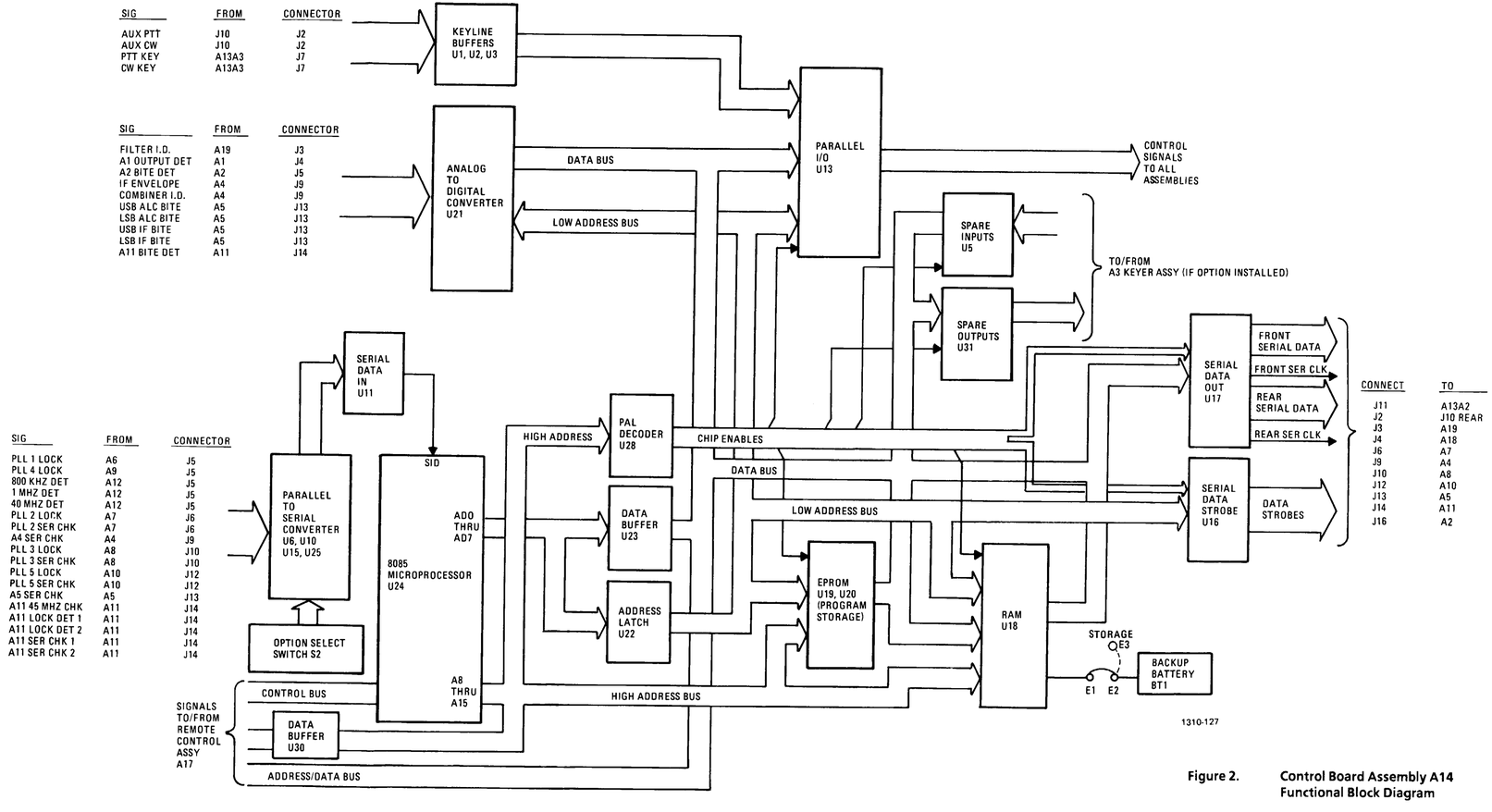


Figure 2. **Control Board Assembly A14 Functional Block Diagram**

The 6264 8K byte static CMOS RAM (U18) contains the channel storage. A fully charged battery, BT1, in the backup power supply should maintain channel storage for one month. In normal exciter operation, the trickle charge circuit will recharge a dead battery in 24 hours. Terminals E1-E2, left unjumpered, isolate the battery from the board circuitry for prolonged storage without maintaining channel memory to prevent battery discharge. However, E1 and E2, must be connected prior to operating the exciter to provide the battery backup provision, and to avoid damage to U18.

3.4 Parallel Input/Output

The 8255A U13 provides 22 lines of interface through two output ports and one input port which handle a variety of exciter controls and functions. The functions and modules associated with each port are shown in table 2.

Table 2. 8255A Port to Module Correlation

Port	Associated Module
PA OUTPUT	Post Selector, Rear Panel, System Interface, Carrier Generator, Combiner, Audio Assembly, and A14 Serial Data Generation Circuitry.
PB INPUT	Rear Panel, System Interface, A14 Keyline Circuitry, and A14 A-to-D Converter (U21).
PC OUTPUT	Rear Panel and A14 Parallel/Serial Conversion Circuitry.

Buffer U5 (74LS244) and Latch U31 (74LS374) provide eight additional parallel input and output ports respectively. U5 monitors the keyer identification line from the Keyer Assembly A3 (if installed) and also the A14 internal keyline circuitry. The CW mode and FSK sense of the Keyer Assembly are outputs from the data latch U31.

3.5 Parallel/Serial Conversions

Four, 4021 type parallel-to-serial converters, U6, U10, U15, and U25 handle the parallel-to-serial conversions that take place on Control Board Assembly A14. When one group of eight parallel inputs needs to be read in, the appropriate converter is selected by multiplexer U11. A pulse is then generated through U17 to that converter to latch the parallel information into its buffers. The front serial clock is then used to clock the eight bits of information from that 4021 into the processor through the CPU SID line. Converters U6, U15, and U25 are used to read in BITE status lines and U10 reads in the options select switch S2. (See paragraph 4.) Table 3 lists the modules affected by each parallel-to-serial converter.

3.6 Serial Output

Most of the control signals within the RF-1310 Exciter are sent serially from the A14 assembly. The serial data transmission circuitry consists of U12, U17, and U28. The data to be written out is loaded into U17 and clocked out as either front data or rear data by a clock generated by the PAL U28. Front serial data and clock signals control the front panel and display assembly functions. All other assemblies are controlled by the rear serial data and clock. All assemblies controlled by each serial control line receive the same data simultaneously. Address signals and strobe pulses generated by U16 are used to gate the data into the individual assemblies.

Table 3. Parallel/Serial Converter Modules

Converter	Module Affected
U10	Options Switch S2
U15	Front Panel Signals, PB0 through PB4 Combiner, Serial Check, and PLL 3 - Serial Check/Lock
U6	PLL 1 Lock, PLL 4 Lock Reference Generator 800 kHz, 1 MHz, 40 MHz Locks PLL 2 Serial Check/Lock
U25	Carrier Generator - 45 MHz Lock/Lock 1 Lock 2 Serial Check 1/Serial Check 2 Audio Assembly/Serial Check PLL 5 Serial Check/Lock

3.7 Analog Inputs

Analog-to-digital (A/D) converter U21 handles all the analog inputs to the A14 assembly. With a few exceptions, the majority of these inputs are used for BITE testing. Most are generated on the assemblies involved with audio and RF signal processing and reflect the signal level at the output of the individual assemblies. Two other lines are used as a postselector indicator line and a line which indicates the combiner assembly option as installed. In order to maintain a high degree of accuracy, the A/D converter is powered off its own + 5 volt reference VR1. The EOC line of the A/D converter is read back through an input port of the 8255A U13 and is used during BITE to verify the conversion time of the A/D converter.

4. PROGRAMMABLE OPTIONS SELECTIONS

The easiest way to select the programmable options is by Front Panel Entry. This method is described in the Operation section. An alternate method of option entry is to use switches S1 and S2 on the A14 assembly.

Automatic Level Control (ALC), Voice Activated Keying (VOX), and the desired FSK shift are selected at the options selection switch S2. S2 is located near the top edge of the A14 assembly. The desired selections are then programmed into the exciter via pushbutton switch S1. S1 is also located near the top edge of the A14 PWB. ALC operation is enabled or disabled individually at S2 for each of the six audio inputs. ALC Hangtime is programmed for VOICE (one second) or DATA (fifty milliseconds) on AUX 1 and AUX 2. VOX operation is available for USB, AM, AFSK, and 2ISB. The FSK shift can be set for 85 Hz, 170 Hz, 425 Hz, or 850 Hz.

The options are selected by setting the individual switches of S2 to the desired positions as described in the following tables and example procedure. The selected parameters are retained in the exciter's CMOS RAM. Memory protection is provided by a back up battery.

Switch S2, positions 1 and 2 are used to select the ALC, ALC Hangtime/VOX or FSK frequency shift option group as summarized in table 4. When programming the ALC option group, positions 3 through 8 of S2 are used to select ALC on or off for each of the audio inputs as listed in table 5. For ALC Hangtime/VOX option, positions 4 and 5 select VOICE or DATA operation for AUX 1 and/or AUX 2 inputs. VOX operation for all USB audio inputs is turned on or off at S2 position 8, as shown in table 6. To select the desired FSK frequency shift, S2 positions 3 and 4 should be set as shown in table 7. (NOTE: For all frequency shift options, S2 positions 5 through 8 are in the closed position.)

Table 4. General Options Available

Options Group	S2 Positions		Description
	S2-1	S2-2	
ALC	C	C	When the ALC option group is selected, switches S2-3 through S2-8 control whether the ALC operation for a particular audio input is on or off.
ALC HANGTIME/VOX	C	O	Switches S2-4 and S2-5 select an ALC HANGTIME for VOICE or DATA operation on inputs AUX 1 and AUX 2 (Closed = DATA; Open = VOICE). S2-8 enables or disables the VOX option for all USB audio inputs. (S2-8; Closed = VOX OFF; Open = VOX ON)
FSK FREQUENCY SHIFT	O	C	S2 positions -3, and -4 select FSK Freq. Shift option per Table 7.

O = Switch section in open position
C = Switch section in closed position

Table 5. ALC Options

Note: S2-1 and S2-2 closed

Switch Position	S2-3	S2-4	S2-5	S2-6	S2-7	S2-8
O = ALC OFF C = ALC ON	AUX 3	AUX 2	AUX 1	LSB	USB	MIC

O = Switch section in open position
C = Switch section in closed position

Table 6. ALC Hangtime (Aux 1 and Aux 2)/VOX Options (All USB Inputs)

Note: S2-1 Closed, S2-2 Open

Switch Position	S2-3	S2-4	S2-5	S2-6	S2-7	S2-8
O = VOICE C = DATA	----	AUX 2	AUX 1	----	----	VOX available for all Audio Inputs: On = Open Off = Closed

O = Switch section in open position
C = Switch section in closed position

Table 7. FSK Frequency Shift

Note: S2-1 Open, S2-2 Closed

Switch Position	S2-3	S2-4	S2-5	S2-6	S2-7	S2-8
Shift Frequency						
85 Hz (± 42 Hz)	C	C	C	C	C	C
170 Hz (± 85 Hz)	O	C	C	C	C	C
425 Hz (± 212 Hz)	C	O	C	C	C	C
850 Hz (± 425 Hz)	O	O	C	C	C	C

O = Switch section in open position
C = Switch section in closed position

4.1 Programming Options

4.1.1 Programming for ALC Operation:

a. Close S2-1 and S2-2. This will place you in the ALC mode.

b. Select desired audio inputs. Close or open the applicable switch(es) per table 5.

S2-3 = AUX 3
S2-4 = AUX 2
S2-5 = AUX 1
S2-6 = LSB
S2-7 = USB
S2-8 = MIC

c. Depress S1 to enter the selection into memory.

4.1.2 Programming ALC Hangtime/VOX Operation:

a. To set the ALC Hangtime on Aux 1 and Aux 2, position S2-1 to the closed position and open S2-2.

b. Select ALC Hangtimes required for programming:

VOICE (1 second = switch position open)
DATA (50 milliseconds = switch position closed)
Close or open the applicable switch positions per table 6.

AUX 1 = S2-5
AUX 2 = S2-4

Note: VOX operation is available for USB, AM, AFSK, and 2ISB.

c. Select VOX operation on the above selected audio inputs;

S2-8 open = VOX on

S2-8 closed = VOX off

d. Depress S1 to enter the selection into memory.

4.1.3 Setting the FSK Frequency Shift Options:

a. Position S2-1 open and S2-2 closed.

b. Using table 7, determine the desired shift frequency and position S2-3 and S2-4 to the proper settings.

Note: S2-5, -6, -7, and -8 should be in the closed position when setting frequency options.

c. Depress S1 to enter the selection into memory.

NOTE

If data in the CMOS RAM is lost or corrupted, all options should be reprogrammed to ensure desired selections are used.

5. MAINTENANCE

CAUTION

Battery BT1 is in the circuit. Shorting this battery could result in severe circuit damage.

5.1 Alignment

Control Board Assembly A14 requires no adjustment to properly operate.

5.2 Troubleshooting

Although most of the circuitry on this assembly is controlled directly or indirectly by the microprocessor, a practice of standard digital troubleshooting methods alone will isolate most faults to the component level. A logic high is the level between 3 and 5 volts, and a proper logic low is typically between 0 and 1 volt. The circuit area involved in minor faults can be determined by BITE fault codes or by using paragraph 3 of this subsection. More general or major failures are best handled by following the instructions outlined in the following paragraphs.

5.2.1 CPU

If the microprocessor is running, it is capable of debugging several circuits on the A14 assembly by itself. However, first determine if the 8085AH-2 is operating.

These CPU input signals must be present in order for the device to run:

- U24-1, 2 Crystal inputs - 6 MHz
- U24-36 Reset input - High
- U24-6 Trap input - Low

- U24-35 Ready - High
- U24-39 Hold - Low

The A14 assembly + 5 volt supply should be between + 4.75 and + 5.1 volts. The following CPU outputs should be present:

- U24-37 Clock Out 3 MHz square wave
- U24-3 Reset out low
- U24-31 Write active-low pulses
- U24-32 Read active-low pulses
- U24-30 Address latch enable active-high pulses
- U24-4 SOD active-low pulses at 1 millisecond intervals

When the CPU is running and executing the application software, its outputs will only be active a portion of each millisecond. The rest of the time it will stop, waiting for a real-time clock interrupt from U9.

5.2.2 Trap and Reset Circuits

The trap circuit is provided to restart the CPU in the software if the device loses synchronization due to high noise levels on its busses. One-shot U27 is retriggered before timeout from U24, pin 4, the SOD output. The software will generate a low-active pulse every millisecond if it is working properly and if it gets the real-time clock interrupt. Low voltage on the + 5 supply to this board will cause the processor to reset due to the reset circuit Q2-Q5.

5.2.3 Device Selection

Address decoding by PAL U28 aids in the access of devices through the data bus by outputting active-low chip enable signals corresponding to the address on the high-order bits of the CPU. The equations programmed into the PAL, U28, are given in table 8. During normal operation, the enables from U28 should be seen on pin 20 of U19, U20, U18, U13-6, U5-1, and U31-11.

5.2.4 Memory Circuits

It can be very difficult to troubleshoot memory problems if the 8085AH-2 is not operating. If the CPU is running, it can find some problems itself. If the BITE routine indicates a PROM checksum fault, the fact that it is running indicates that the data bus buffers are operating and the PROMs are accessed. However, invalid data in these devices would require replacement of PROMs U19 and U20.

If the BITE routine indicates a CMOS RAM fault, check that the enable pulse is getting to RAM U18, and check the voltage on U18-24. FET Q2 is driven by an enable from U30 as a switch to select U18. The chip enable should put the U2 gate at + 5 V unregulated to turn on the switch. The CMOS RAM is not connected directly to the + 5 V supply, and E1-E2 must be jumpered to avoid damaging the RAM when the power is turned on.

Table 8. U28 PAL Chip Select Programmed Lines

Device Selected	Control Lines							Function
	IOM	A15	A14	A13	A12	WR	RD	
U19-20	0	0	0					PROM 1
U20-20	0	1	0					PROM 2
U18-22	0	0	1	0				CMOS RAM
U21-16	0	0	1	1	1	0		A/D START
U21-21	0	0	1	1	1		0	A/D READ
U13-6	1	0	0	1				8255
U17-2	0	0	1	1	0	0		SER CLOCK
U17-1	1	0	1	0				SER DATA
U16-22	1	0	1	1				SER STROBE
U31-11	1	1	0					SPARE OUT *1
U5-1	1	1	0					SPARE IN *2

Notes: A logic HIGH = 1 and a logic LOW = 0.
All of the above are additionally controlled with INTA = 0 and ALE = 0.
*1 This select is enabled externally from the PAL with WR = 0 through U4-1.
*2 This select is enabled externally from the PAL with RD = 0 through U4-4.

5.2.5 Real-Time Clock

The real time clock circuitry originates from the 3 MHz clock output of CPU U24-37. This is first divided down to 11.72 kHz by counter U8, then fed into U9 to reach the final frequency of 977 Hz. This 977 Hz has become the real time clock and is fed back to the processor as an interrupt through U24-7. Any problems with the real time clock operation can be isolated to a check of this circuitry.

5.2.6 Serial Out

The A14 assembly communicates with the display control board through its serial output circuit (U12, U13, U17, and U28). If this circuit fails, the display will light up but will never change from its power up lamp test.

When the A14 assembly is operating normally, it will attempt to update the complete display once every second. Every second there will be a burst of 64 bytes to the display control board. (2 bytes of serial data sent every millisecond for a 32 millisecond total duration). Following every 2 bytes will be a strobe pulse to the display control board from U16-13.

The BITE routine tests the serial output circuit by sending a test pattern to the four PLLs and the two carrier generator PLLs, and then reading back a test bit from each. If it can set (high) and reset (low) all these test bits, it assumes that the serial output circuit on the A14 assembly is operating. If any one test bit cannot be set and reset, it assumes a problem with that PLL. Table 9 lists the serial data transmission circuit signals.

Table 9. Serial Data Transmission Circuit Signals

Signal	Description
U12-6	Rear serial clock
U12-11	Front serial clock
U13-17	Clock Frequency (software generated)
U13-38	Serial clock select: • High when sending rear serial data • Low when sending front serial data
U17-7, U12-8	Rear serial data
U17-9	Front serial data
U16-4 through 19	Assembly serial strobes, narrow active high pulses clock data on to the assembly being controlled

5.2.7 Serial In

All parallel/serial conversions take place through U6, U10, U16, U25, U11, U13, U24, and U28. Converter U10 is used to read the options select switch, and the remaining converters are used to read in the BITE lines. If any of the logic lines that are read on the parallel sides of these converters end up showing as an error in BITE and are correct as inputs, then this parallel/serial conversion circuitry can be suspected. Signals involved in this circuitry are listed in table 10.

Table 10. Serial In Signals

Signal	Description
U11-9, 10, 11	MUX select - Active high determines which converter will be read in
U6-10, U15-10, U25-10, U10-10	Front serial clock - Clocks data out of converters and into MUX
U6-9, U15-9, U25-9, U10-9	Read line - Active high latches parallel information into 4021 buffers
U6-3, U15-3, U25-3, U11-2, U11-12, U11-14	Serial data in - 8 bits of serial data corresponding to parallel information

5.3 Keylines

All exciter keylines are handled through optoisolators U1 and U3, gate U2, and U13. No signals in the circuitry will be observed unless one of the keylines external to the exciter is activated. If a specific keyline has failed, its corresponding diode CR1 through CR4 should be checked. From there, a low on the opto output should be observed, and then the proper level on the corresponding output gate of U2, followed all the way into U13. If none of the keylines are functioning, there may be a problem with the internal keyline, making U13 suspect.

5.4 Parallel I/O

Parallel I/O is centralized through the ports on U13. If there is a BITE or operation problem concerning the modules controlled by the lines from these parallel circuits, but the module in question is not at fault, there may be a failure in the ports. Failure of proper A/D conversions or lack of any Internal Key signals are just a few signs that could indicate a defective U13.

5.5 Analog Conversions

A/D converter U21 is used primarily during BITE to read in and test the analog output levels of individual signal path assemblies. Starting any conversion consists of two writes to U21, narrow high-active pulses on U21-16. Ten microseconds (or less) later, the end-of-conversion (EOC) line will go low. It will stay low for 100 microseconds and after it goes high again there will be one narrow high-active pulse on U21-21. At that point, the digital version of the input signal read will be transferred on the data bus to the CPU. The above is true for all the other analog inputs sampled during the execution of BITE. Table 11 lists signals of the analog input circuit.

Table 11. Analog Input Circuit Signals

Signal	Description
U8-1	Clock in - 3 MHz TTL square wave
U8-4	Clock Out - 750 kHz TTL square wave
U21-22	Clock in - 750 kHz TTL square wave
U21-16, 32	Start conversion - Two narrow high going pulses, every time a conversion is initiated
U21-13	End of Conversion - 85 microseconds low, at the completion of a conversion
U21-21	Output enable - narrow high going pulse.
U21-15, 18	Multiplexer out, comparator in

5.6 BITE Detected Faults

The faulting areas on the A14 assembly detectable through BITE are listed in table 12.

6. PARTS LIST, COMPONENT LOCATIONS, AND SCHEMATIC DIAGRAM

All replaceable components of Control Board Assembly A14 are listed in table 13. Component locations are shown in figure 3. Figure 4 is a schematic of the control board circuit.

Table 12. BITE Detected Faults

Fault	Description
Fault 01	PROM failure: The binary checksum calculated from the contents of programmed U19 and U20 do not match the value programmed by the factory. Validity of firmware is doubtful, and after some initial checks, consideration should be given to replacing both devices.
Fault 02	Parallel/Serial conversion error: Error was detected in the reading in and shift of the test level (0 Vdc) at pin 8 of U6, U10, U15, and U25. Check these and U11 and U13.
Fault 03	CMOS RAM failure: Errors are found in the ability to store and retrieve data in U18. Check U18, check E1-E2 jumpering, BT1, Q2, and associated circuits.
Fault 04	Serial data input failure: Faulty serial input is detected. Check U12, U13, and U17.
Fault 05	Keyline logic failure: Error reading in the proper keyline closure. Check U1, U2, U12, and U13.
Fault 06	I/O Failure: Error detected in controlling U13. Replace U13.
Faults 07, 08, and 09	A/D failure: Failure in correctly making A-to-D conversions. Check U21, VR1, and U13. Check that all analog inputs to U21 are between 0 volts and 5 volts.

Table 13. Control Board Assembly A14 Parts List (10121-2850 Rev. E)

Ref. Desig.	Part Number	Description
4	J65-0008-103	JMPR 2P FEM. .10 CNTR
5	J46-0042-103	JUMPER HEADER
BT1	B41-0009-004	BAT NICAD 3.6V -20/+70C
C1	C26-0010-221	CAP 220UF 20% 10V TANT
C2	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C3	C26-0010-221	CAP 220UF 20% 10V TANT
C4	C26-0010-221	CAP 220UF 20% 10V TANT
C5	C26-0010-221	CAP 220UF 20% 10V TANT
C6	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C7	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C8	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C9	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C10	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C11	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C12	M39014/02-1310V	CAP .1UF 10% 100V CER-R

Table 13. Control Board Assembly A14 Parts List (10121-2850 Rev. E) (Cont.)

Ref. Desig.	Part Number	Description
C13	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C14	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C15	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C16	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C17	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C18	C26-0010-680	CAP 68UF 20% 10V TANT
C19	C26-0010-680	CAP 68UF 20% 10V TANT
C20	C26-0010-680	CAP 68UF 20% 10V TANT
C21	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C22	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C23	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C24	M39014/01-1553V	CAP .1UF 10% 50V CER-R
C25	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C26	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C27	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C29	C25-0001-313	CAP 100UF 20% 20V TANT
C30	C26-0035-159	CAP 1.5UF 20% 35V TANT
C31	C26-0016-150	CAP 15UF 20% 16V TANT
C32	C26-0050-479	CAP 4.7UF 20% 50V TANT
C33	C26-0050-479	CAP 4.7UF 20% 50V TANT
C34	C26-0050-109	CAP 1.0UF 20% 50V TANT
C35	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C36	M39014/02-1310V	CAP .1UF 10% 100V CER-R
CR1	1N4454	DIODE 200MA 75V SW
CR2	1N4454	DIODE 200MA 75V SW
CR3	1N4454	DIODE 200MA 75V SW
CR4	1N4454	DIODE 200MA 75V SW
CR5	1N4454	DIODE 200MA 75V SW
CR6	1N4454	DIODE 200MA 75V SW
CR7	1N4454	DIODE 200MA 75V SW
CR8	1N4454	DIODE 200MA 75V SW
CR9	1N4454	DIODE 200MA 75V SW
CR10	1N4454	DIODE 200MA 75V SW
CR11	1N4454	DIODE 200MA 75V SW
J1	J46-0032-004	HDR 4 PIN 0.100" SR
J2	J46-0013-014	HDR 14 PIN 0.100 DR SHRD
J3	J46-0032-010	HDR 10 PIN 0.100" SR
J4	J46-0013-020	HDR 20 PIN 0.100" DR SHRD
J5	J46-0032-008	HDR 8 PIN 0.100" SR
J6	J46-0034-008	HDR 8 PIN 0.100" RT ANG
J7	J46-0032-008	HDR 8 PIN 0.100" SR
J8	J46-0034-008	HDR 8 PIN 0.100" RT ANG
J9	J46-0034-012	HDR.12 PIN 0.100" RT ANG

Table 13. Control Board Assembly A14 Parts List (10121-2850 Rev. E) (Cont.)

Ref. Desig.	Part Number	Description
J10	J46-0034-008	HDR 8 PIN 0.100" RT ANG
J11	J46-0031-020	HDR 20 PIN 0.100" RT ANG
J12	J46-0034-008	HDR 8 PIN 0.100" RT ANG
J13	J46-0031-024	HDR 24 PIN 0.100" RT ANG
J14	J46-0031-016	HDR 16 PIN 0.100" RT ANG
J15	J46-0013-040	HDR 40 PIN 0.100" DR SHRD
J16	J46-0013-010	HDR 10 PIN 0.100 DR SHRD
L1	10073-7034	INDUCTOR, 440UH
L2	10073-7034	INDUCTOR, 440UH
L3	10073-7029	INDUCTOR, FILTER CHOKE
L4	L-0644	COIL 220UH 10% FXD RF
L5	10073-7034	INDUCTOR, 440UH
Q1	2N2222A	XSTR SS/GP NPN TO-18
Q2	3N170	XSTR MOSFET
Q3	2N2907A	XSTR SS/GP PNP TO-18
Q4	2N2907A	XSTR SS/GP PNP TO-18
Q5	2N2222A	XSTR SS/GP NPN TO-18
Q6	2N2222A	XSTR SS/GP NPN TO-18
Q7	2N2222A	XSTR SS/GP NPN TO-18
R1	RCR32G561JM	RES 560 5% 1W CAR COMP
R2	R65-0004-331	RES 330 5% 1/2W CAR FILM
R3	R65-0004-561	RES 560 5% 1/2W CAR FILM
R4	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R5	R65-0004-331	RES 330 5% 1/2W CAR FILM
R6	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R7	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R8	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R9	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R10	R65-0003-102	RES 1.0K 5% 1/4W CAR FILM
R11	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R12	R50-0010-104	RES 100K 2% 10SIP 9RES
R13	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R14	R65-0003-512	RES 5.1K 5% 1/4W CAR FILM
R15	R65-0003-154	RES 150K 5% 1/4W CAR FILM
R16	R65-0003-512	RES 5.1K 5% 1/4W CAR FILM
R17	R50-0010-103	RES 10K 2% 10SIP 9RES
R18	R50-0010-103	RES 10K 2% 10SIP 9RES
R19	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R20	R65-0003-184	RES 180K 5% 1/4W CAR FILM
R21	R65-0003-184	RES 180K 5% 1/4W CAR FILM
R22	R65-0003-512	RES 5.1K 5% 1/4W CAR FILM
R23	R50-0010-104	RES 100K 2% 10SIP 9RES

Table 13. Control Board Assembly A14 Parts List (10121-2850 Rev. E) (Cont.)

Ref. Desig.	Part Number	Description
R24	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R25	R50-0010-103	RES 10K 2% 10SIP 9RES
R26	R50-0010-103	RES 10K 2% 10SIP 9RES
R27	R65-0003-223	RES 22K 5% 1/4W CAR FILM
R28	R65-0003-223	RES 22K 5% 1/4W CAR FILM
R29	R65-0003-223	RES 22K 5% 1/4W CAR FILM
R30	R50-0010-104	RES 100K 2% 10SIP 9RES
R31	R50-0010-103	RES 10K 2% 10SIP 9RES
R32	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R33	R65-0003-473	RES 47K 5% 1/4W CAR FILM
R34	R65-0003-333	RES 33K 5% 1/4W CAR FILM
R35	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R36	R65-0003-272	RES 2.7K 5% 1/4W CAR FILM
R37	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R38	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R39	R65-0003-473	RES 47K 5% 1/4W CAR FILM
R40	R65-0003-122	RES 1.2K 5% 1/4W CAR FILM
R41	R65-0003-204	RES 200K 5% 1/4W CAR FILM
R42	R65-0003-243	RES 24K 5% 1/4W CAR FILM
R43	R65-0003-114	RES 110K 5% 1/4W CAR FILM
R44	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R45	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R46	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R47	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R48	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R49	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R50	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R51	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R52	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R53	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R54	R65-0003-223	RES 22K 5% 1/4W CAR FILM
R55	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R56	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R57	R65-0003-103	RES 10K 5% 1/4W CAR FILM
S1	S06-0002-116	SW PB SPST NO MOM RA PCMT
S2	S50-0001-008	SW SPST 8SEC .1A SLD DIP
U1	I75-0007-000	OPTOISOLATOR DUAL MCT6
U2	I01-0000-012	IC 4023B PLASTIC CMOS
U3	I75-0007-000	OPTOISOLATOR DUAL MCT6
U4	I15-0000-032	IC 74HC32 PLASTIC CMOS
U5	I05-0000-244	IC 74LS244 PLASTIC TTL
U6	I01-0000-153	IC 4021B PLASTIC CMOS
U7	I05-0000-004	IC 74LS04 PLASTIC TTL
U8	I15-0000-393	IC 74HC393 PLASTIC CMOS

Table 13. Control Board Assembly A14 Parts List (10121-2850 Rev. E) (Cont.)

Ref. Desig.	Part Number	Description
U9	I05-0000-092	IC 74LS92 PLASTIC TTL
U10	I01-0000-153	IC 4021B PLASTIC CMOS
U11	I15-0000-151	IC 74HC151 PLASTIC CMOS
U12	I15-0000-000	IC 74HC00 PLASTIC CMOS
U13	I59-0008-001	IC 8255A PROG INTERFACE
U14	I05-0000-004	IC 74LS04 PLASTIC TTL
U15	I01-0000-153	IC 4021B PLASTIC CMOS
U16	I01-0000-202	IC 4514B PLASTIC CMOS
U17	I15-0000-165	IC 74HC165 PLASTIC CMOS
U18	I26-0017-001	IC 8KX8 SRAM 6264
U19	10121-8511	SOFTWARE KIT
U20	10121-8511	SOFTWARE KIT
U21	I40-0010-001	IC ADC0817 PLASTIC CMOS
U22	I05-0000-373	IC 74LS373 PLASTIC TTL
U23	I05-0000-245	IC 74LS245 PLASTIC TTL
U24	I27-0006-001	IC MIPRCS 8-BIT 8085
U25	I01-0000-153	IC 4021B PLASTIC CMOS
U26	I01-0017-000	IC 7432 PLASTIC TTL
U27	I05-0000-122	IC 74LS122 PLASTIC TTL
U28	10121-8301	KIT FIRMWARE CONTROL
U29	I05-0000-000	IC 74LS00 PLASTIC TTL
U30	I15-0000-244	IC 74HC244 PLASTIC CMOS
U31	I05-0000-374	IC 74LS374 PLASTIC TTL
VR1	I12-0006-005	IC VR 78L05A +5V .10A 4%
VR2	1N5223B	DIODE 2.7V 5% .5W ZENER
VR3	1N5223B	DIODE 2.7V 5% .5W ZENER
XU19	J77-0008-006	SKT IC MACH 28 PIN
XU20	J77-0008-006	SKT IC MACH 28 PIN
XU24	J77-0008-007	SKT IC MACH 40 PIN
Y1	Y15-0004-060	XTAL 6 MHZ

NOTE

Part numbers for U19 and U20 are 10121-8XXX-X, where XXX-X is the four character software kit code found on the PROM label. For example, if the code is 501C, the part number for the programmed PROM is 10121-8501C. The kit includes both PROMs.

NOTES:

1. BATTERY BACKUP JUMPER :
   CONNECT E1-E2 BEFORE NORMAL OPERATION TO PRESERVE MEMORY.
   CONNECT E2-E3 TO ISOLATE BATTERY FOR EXTENDED STORAGE.
2. INSTALL CONNECTOR J4 IN POSITIONS 1-20.

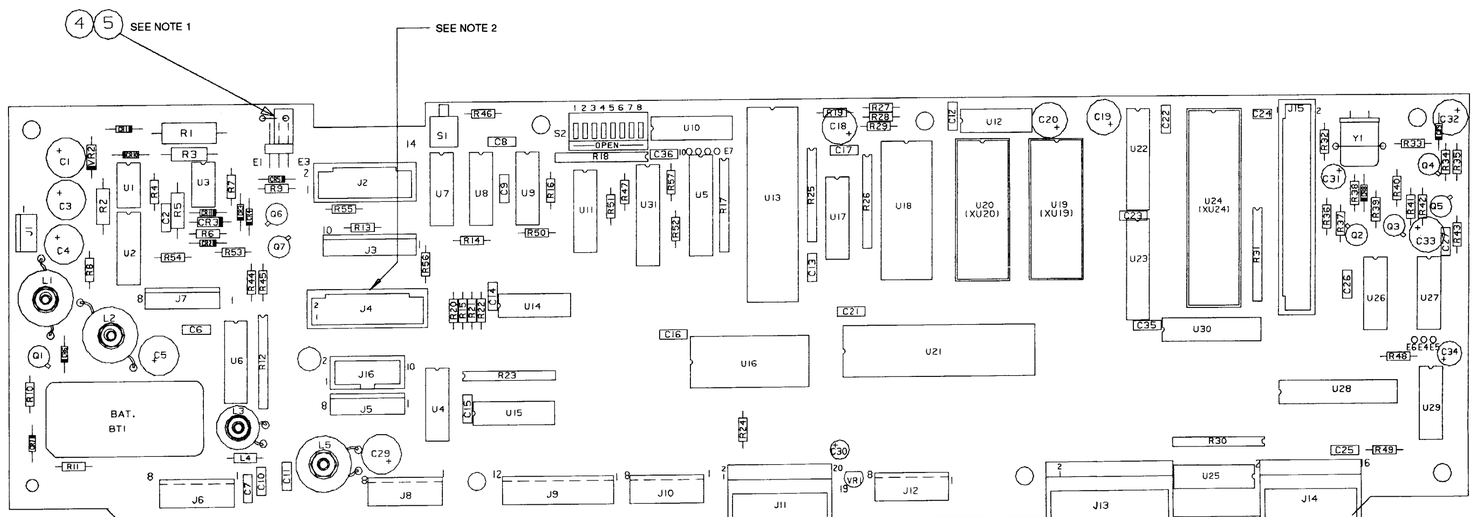


Figure 3. **Control Board Assembly A14 Component Location Diagram (10121-2850, Rev. C)**

NOTE: UNLESS OTHERWISE SPECIFIED:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR A COMPLETE DESIGNATION, PREFIX WITH UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.
2. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, ±5%.
3. ALL CAPACITOR VALUES ARE IN MICROFARADS.
4. VENDOR PART NO. CALLOUTS ARE FOR REFERENCE ONLY. COMPONENTS ARE SUPPLIED PER PART NO. IN PARTS LIST.
   U26 7432
   U29 74LS00
   U12 74HC00
   U7 74LS04
   U14 74LS04

UNUSED GATES

74HC32 U4D N/C

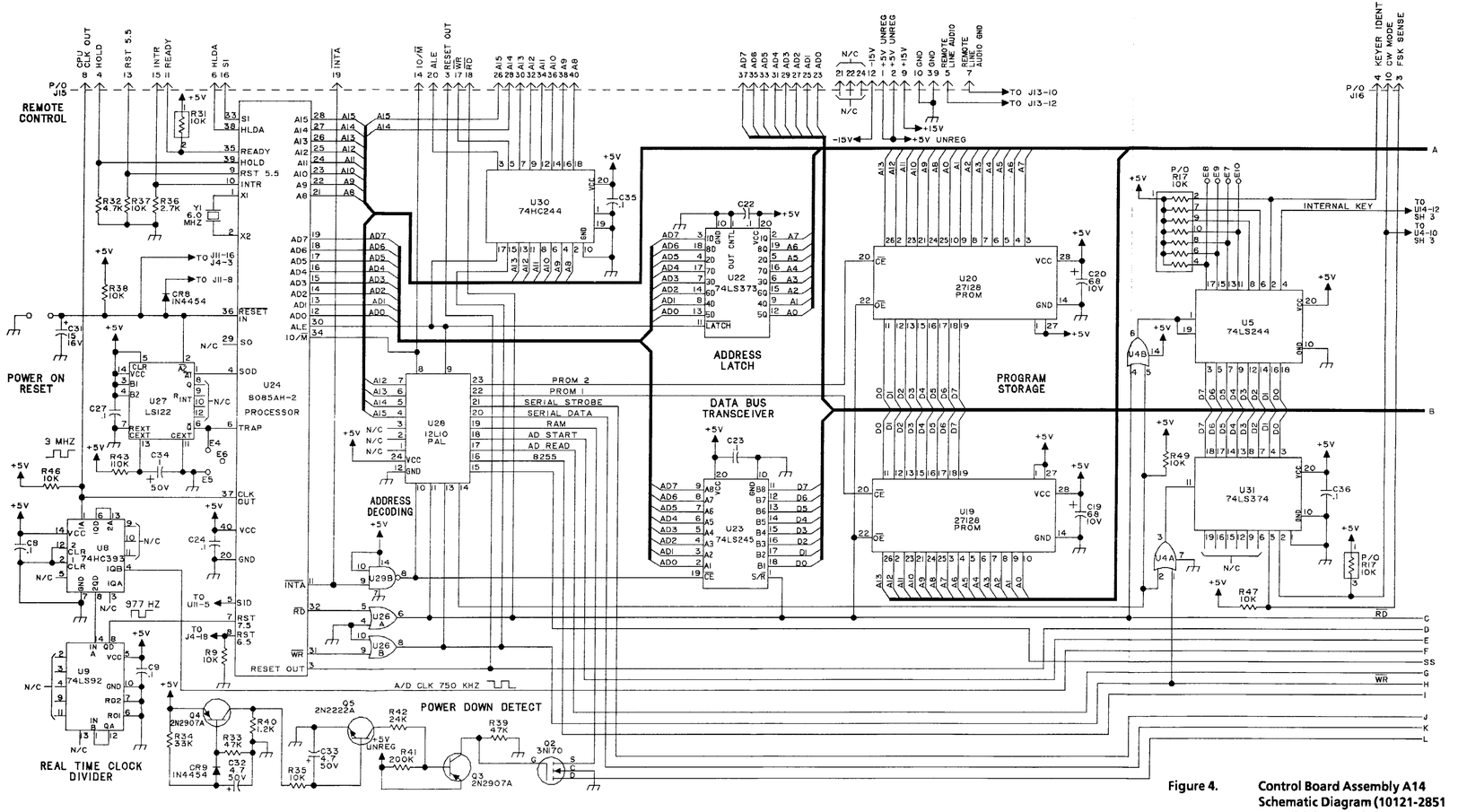


Figure 4. Control Board Assembly A14 Schematic Diagram (10121-2851 Rev. D) (Sheet 1 of 4)

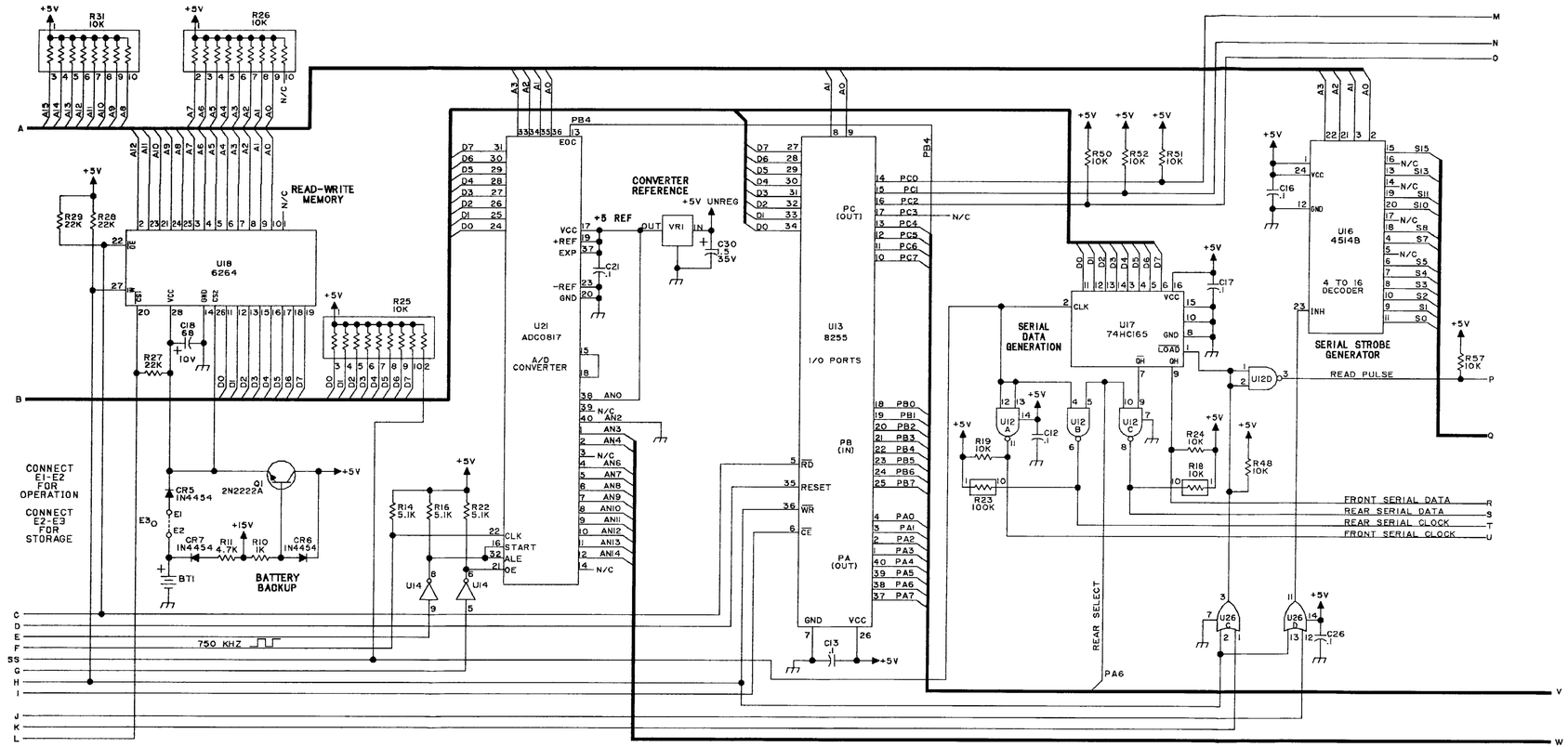


Figure 4. Control Board Assembly A14 Schematic Diagram (10121-2851 Rev. D) (Sheet 2 of 4)

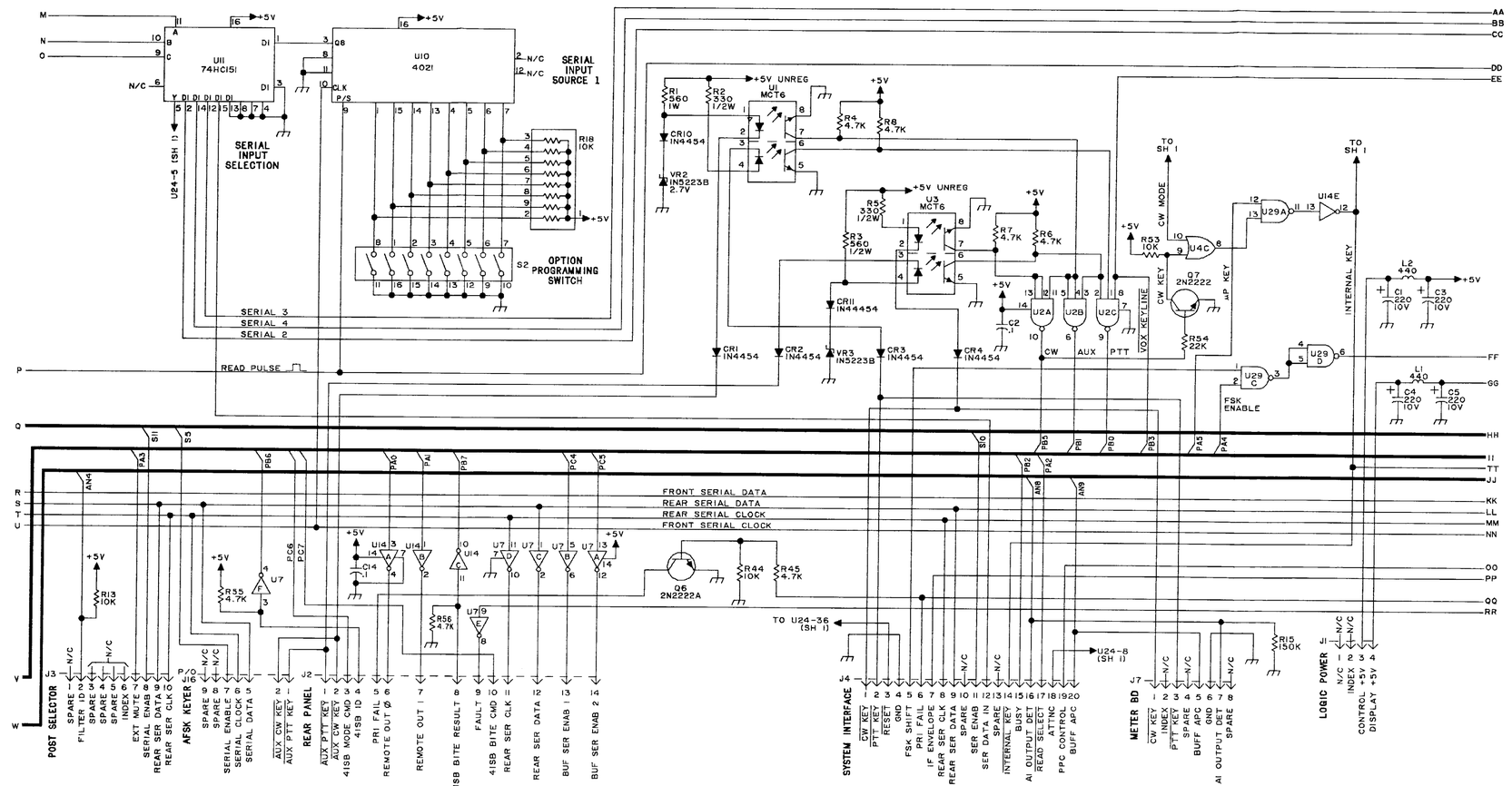


Figure 4. Control Board Assembly A14 Schematic Diagram (10121-2851 Rev. D) (Sheet 3 of 4)

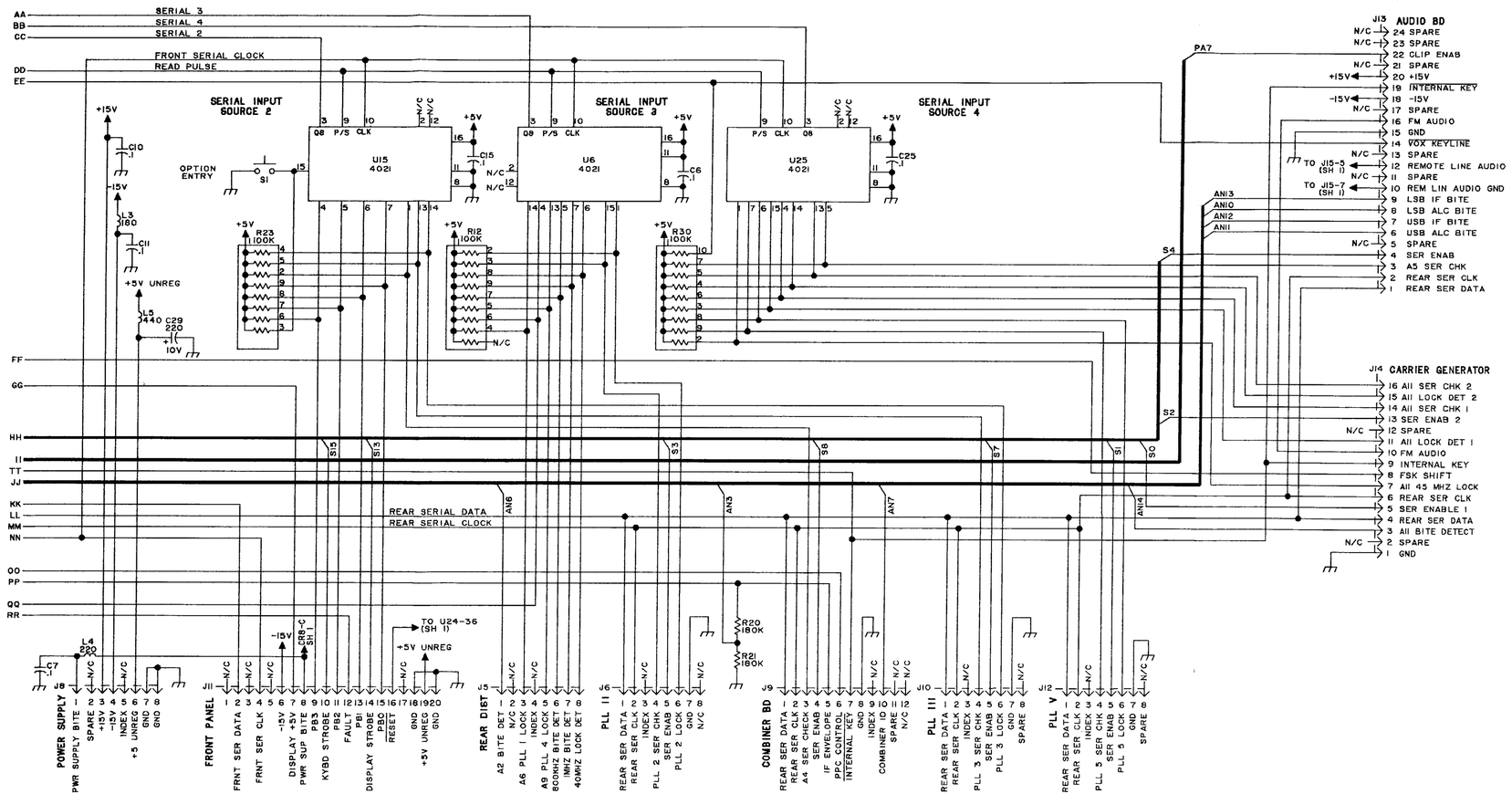
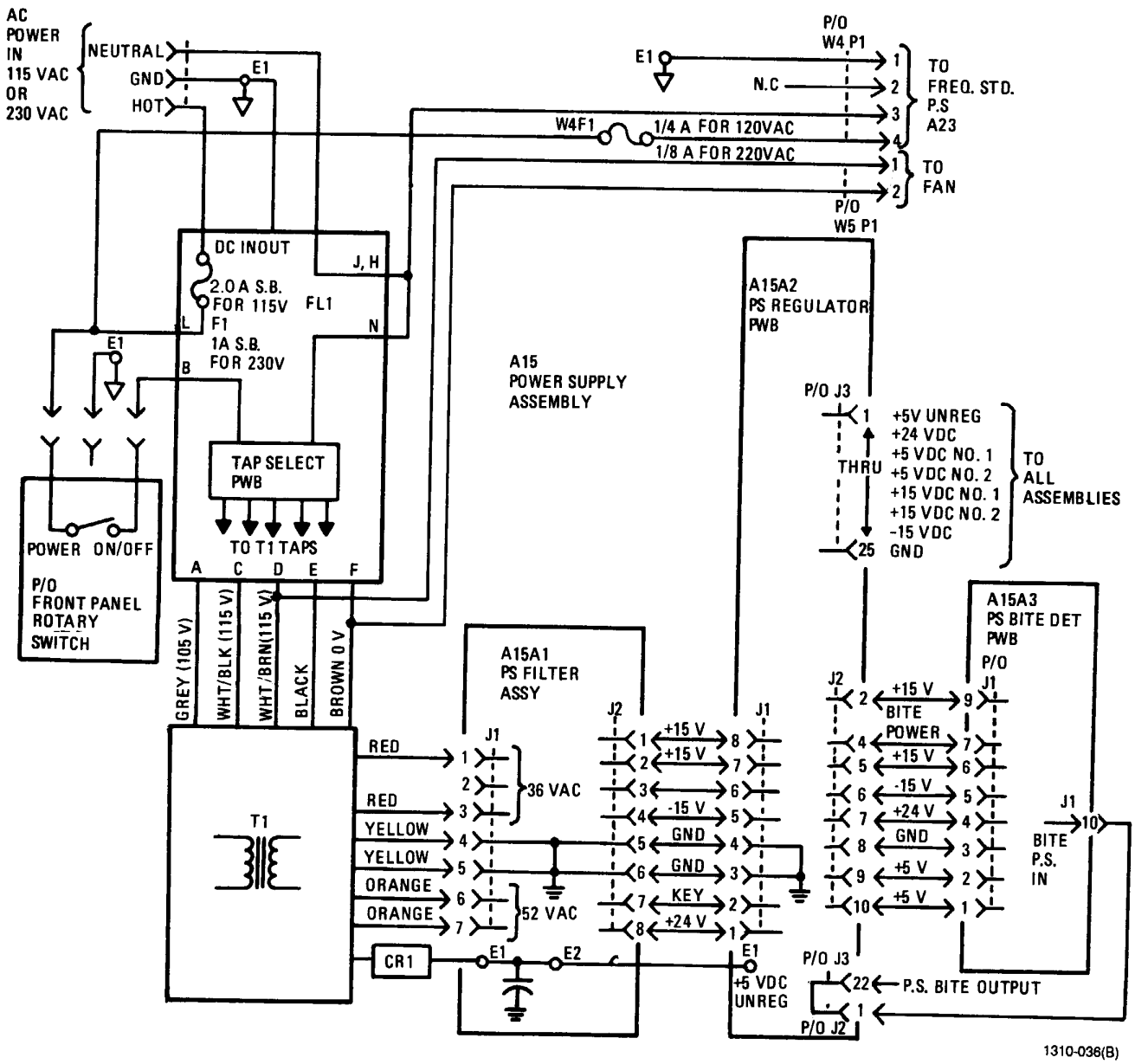


Figure 4. Control Board Assembly A14 Schematic Diagram (10121-2851 Rev. D) (Sheet 4 of 4)

A15
POWER SUPPLY ASSEMBLY



1310-036(B)

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POWER SUPPLY ASSEMBLY A15

1. GENERAL DESCRIPTION

WARNING

Potentially hazardous high voltages are present inside the A15 assembly whenever the exciter is connected to an ac line source. Do not attempt any repair to this assembly unless the line cord is disconnected. Do not operate the exciter without the protective cover properly installed over the assembly.

Power Supply Assembly A15 converts either 100, 120, 220, or 240 Vac input line voltages into the dc voltages required to operate all RF-1310 assemblies except Frequency Standard Assembly A21. The + 24 Vdc Power Supply Assembly A23 provides power to the Frequency Standard Assembly.

Input voltage selection for the A15 assembly is made by positioning a plug-in PWB that is part of A15 Line Filter FL1. It is located next to the rear panel ac power fuse. Input voltage selection for the A23 assembly is made by switch S1 on the A23 assembly and the FL1 power select PWB. Both must be changed to affect proper line voltage selection. Refer to the Installation section of this manual for further information.

All power supply components and assemblies are housed in a single, metal housing with cover. Major components/assemblies inside this housing are listed below:

- Input Line Filter FL1
- Power Transformer T1
- Filter PWB A15A1
- Heatsink Assembly A15A2 with Regulator PWB A15A2A1
- Power Supply BITE Detector PWB A15A3

The position of these assemblies is shown in figure 1.

FL1 provides EMI protection and A15 input voltage selection. T1 converts the ac line voltage into the required lower ac voltage levels needed to run the regulators. Filter PWB A15A1 converts the T1 ac outputs into unregulated dc voltage levels. The A15A2 assembly contains the three terminal voltage regulators which convert the unregulated dc levels into regulated dc output voltages. The voltage regulators VR1 through VR6 are mounted on Heatsink Assembly A15A2, while the remaining circuitry is on Regulator PWB Assembly A15A2A1. A15A2A1 delivers + 5 Vdc, + 15 Vdc, -15 Vdc, and + 24 Vdc to other assemblies in the exciter.

Power Supply BITE PWB A15A3 monitors the output of Regulator PWB A15A2A1, and signals the Control PWB A14 microprocessor if these levels exceed certain prescribed limits. This in turn causes a front panel fault indicator to light. All major components and assemblies in the A15 assembly are interconnected by ribbon cable with plug-in connectors.

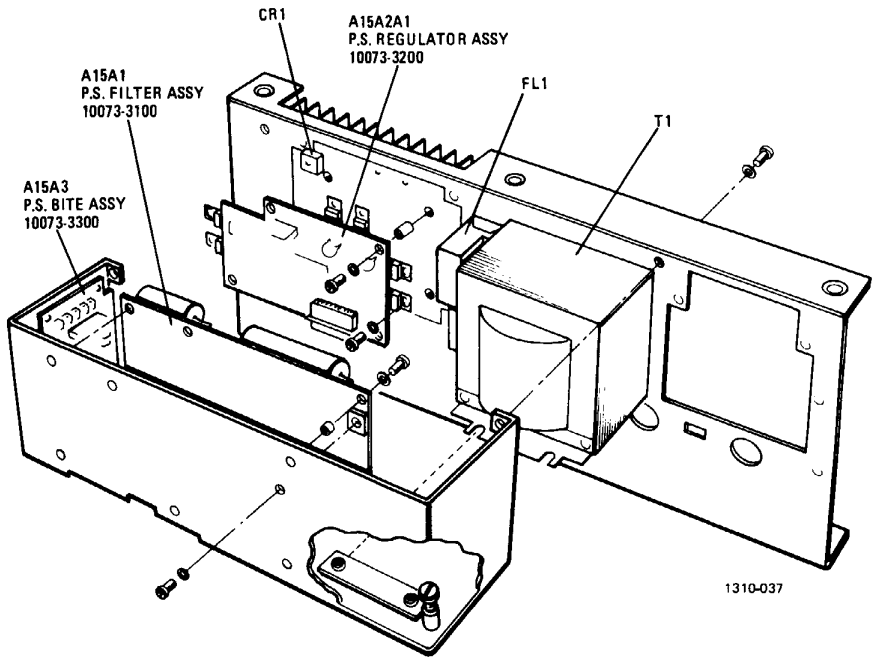


Figure 1. Power Supply Assembly A15 Location

2. INTERFACE CONNECTIONS

Table 1 details the various input/output connections and other relevant data.

Table 1. Power Supply Assembly A15 Interface Connectors

Connector	Function	Characteristics
A15A2A1J3-1	+ 15 V Regulated No. 1	
A15A2A1J3-2	+ 24 V Regulated	
A15A2A1J3-3	Gnd	Ground
A15A2A1J3-4	+ 5 V Unregulated	
A15A2A1J3-5, 6	+ 15 V Regulated No. 1	
A15A2A1J3-7	+ 5 V Unregulated	
A15A2A1J3-8	Gnd	Ground
A15A2A1J3-9	+ 5 V Regulated No. 2	
A15A2A1J3-10	No Connection	

Table 1. Power Supply Assembly A15 Interface Connectors (Cont.)

Connector	Function	Characteristics
A15A2A1J3-11	-15 V Regulated	
A15A2A1J3-12	+ 5 V Unregulated	
A15A2A1J3-13, 14	Gnd	Ground
A15A2A1J3-15	+ 5 V Unregulated	
A15A2A1J3-16	-15 V Regulated	
A15A2A1J3-17, 18	+ 24 V Regulated	
A15A2A1J3-19	-15 V Regulated	
A15A2A1J3-20	+ 15 V Regulated No. 2	
A15A2A1J3-21	+ 5 V Regulated No. 1	
A15A2A1J3-22	BITE Power Supply	0 Vdc = Failure
A15A2A1J3-23	+ 15 V Regulated No. 1	
A15A2A1J3-24	+ 15 V Regulated No. 2	
A15A2A1J3-25	Gnd	Ground
W3P1-1	Switched Ac Hot	To Front Panel ON/OFF Switch
W3P1-2	Gnd	To Front Panel ON/OFF Switch
W3P1-3	Ac Hot	To Front Panel ON/OFF Switch
W4P1-1	Ac Neutral	To + 24 V Power Supply A23
W4P1-2	Ac Hot	To + 24 V Power Supply A23
W4P1-3	Ground	To + 24 V Power Supply A23
W5P1-1	Switched Ac Hot	To fan
W5P1-2	Ac Neutral	To fan

3. A15 PARTS LISTS, COMPONENT LOCATIONS, AND SCHEMATIC DIAGRAM

Table 2 is the A15 assembly parts list. Figure 2 is the functional block diagram for Power Supply Assembly A15, figure 3 is the A15 assembly component location diagram, and figure 4 is the A15 assembly schematic diagram.

Table 2. Power Supply Assembly A15 Parts List (10121-3000-01 Rev. B)

Ref. Desig.	Part Number	Description
	10121-3005	PANEL, REAR
	10073-3006	CHASSIS, POWER SUPPLY
	10073-3011	PLATE,NUT
	10073-7193	BRACKET,PWR SUPPLY
	10121-1134	LABEL, POWER SUPPLY
	Z10-0010-000	LABEL, WARNING
	10121-3009	LABEL, F2 FUSEHOLDER
A1	10073-3100	PWB ASSY,PWR SUPPLY XFMR
A2	10073-3250	HEATSINK ASSY
A3	10073-3300	PWB ASSY, BITE
E1	MS77068-1	LUG SOLDER #4
F1	F-0026	FUSE 2.0A SB 125V 3AG
FL1	6919-1400	LINE FILTER
T1	10073-3052	LEAD PREP,PWR SUPPLY XFMR
W1	10073-7060	RIBBON CABLE, 10 COND
W2	10073-7059	RIBBON CABLE, 8 COND
W3	10073-7250	CABLE ASSY,A15W3
W4	10121-7247	CABLE,PS/SYNC DET
W5	10121-7185	CABLE, FAN

*This part no. becomes 10121-7247 for 10121-3000-02 version.

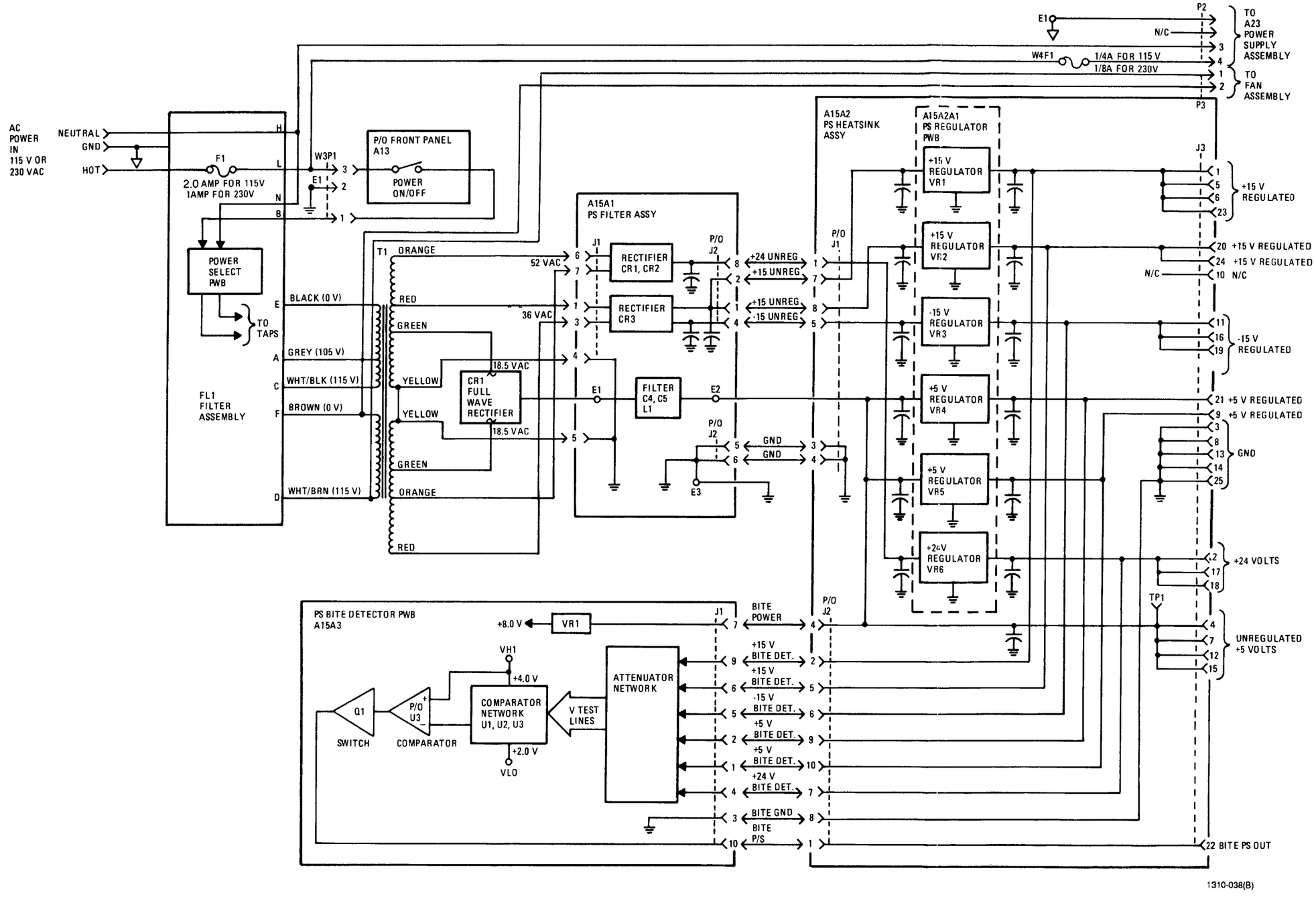


Figure 2. **Power Supply Assembly A15 Functional Block Diagram**

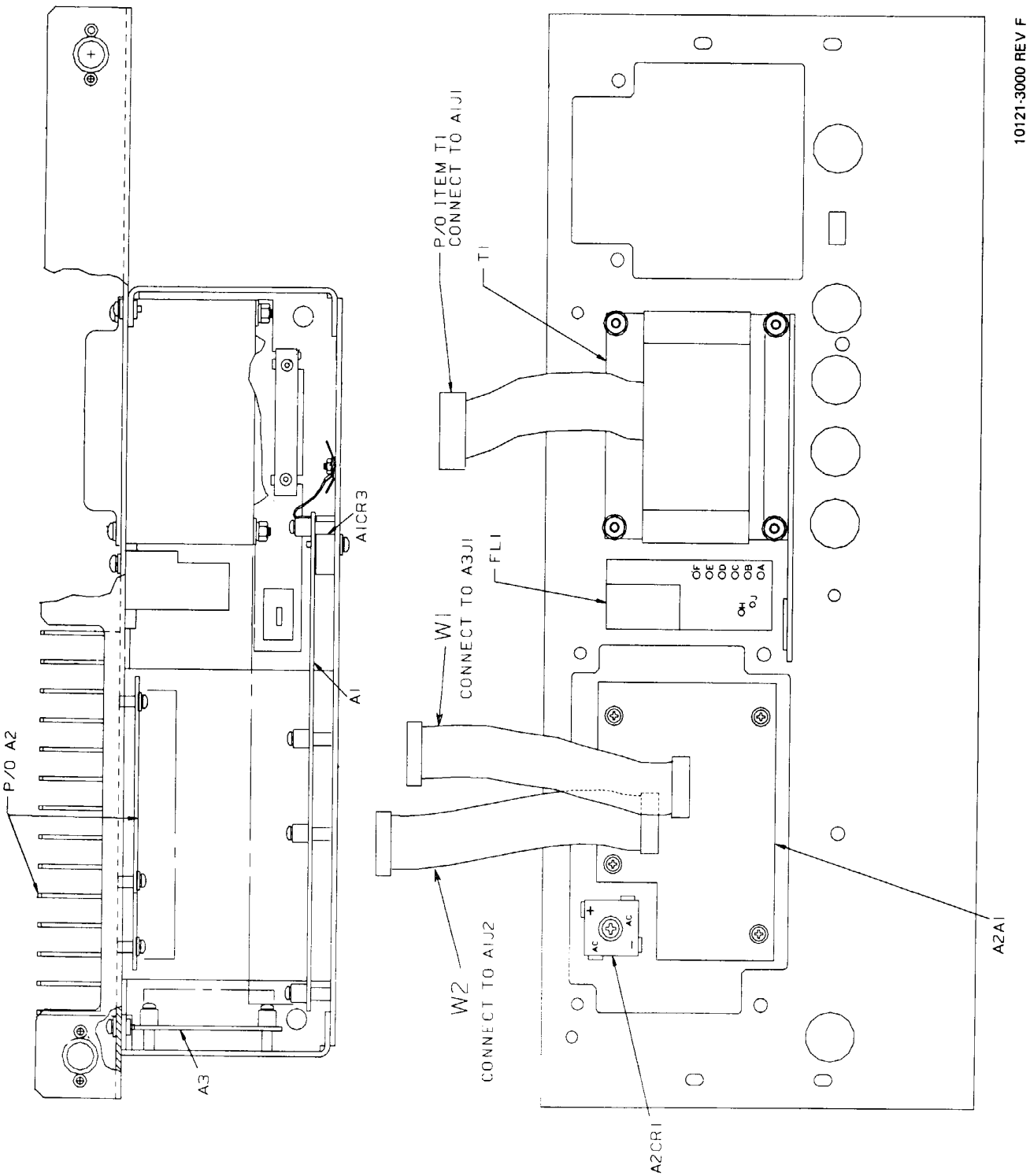


Figure 3. Power Supply Assembly A15 Component Location Diagram (10121-3000 Rev. K)

NOTE: UNLESS OTHERWISE SPECIFIED:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR A COMPLETE DESIGNATION, PREFIX WITH UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.

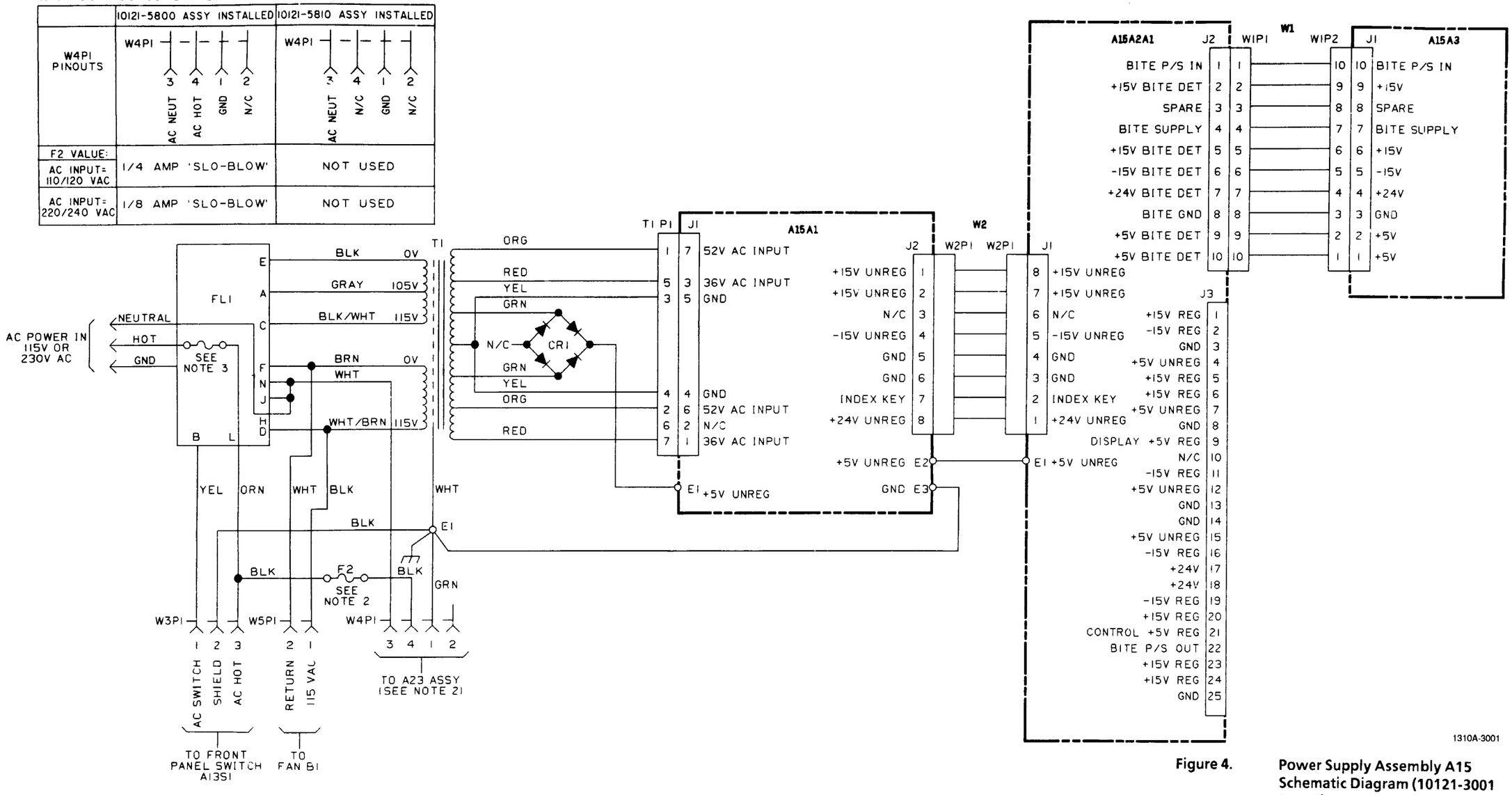
2. A23 ASSY MAY BE EITHER:
   10121-5800, FREQUENCY STANDARD +24V POWER SUPPLY OR
   10121-5810, FREQUENCY STANDARD SYNCHRONIZATION DETECTOR ASSY.

   W4P1 CONNECTIONS AND F2 VALUE ARE CHOSEN AS SHOWN BELOW:

	10121-5800 ASSY INSTALLED	10121-5810 ASSY INSTALLED
W4P1 PINOUTS	W4P1: 3 AC NEUT, 4 AC HOT, 1 GND, 2 N/C	W4P1: 3 AC NEUT, 4 N/C, 1 GND, 2 N/C
F2 VALUE:		
AC INPUT= 110/120 VAC	1/4 AMP 'SLO-BLOW'	NOT USED
AC INPUT= 220/240 VAC	1/8 AMP 'SLO-BLOW'	NOT USED

3.

AC INPUT	FLI FUSE RATING
110/120 VAC	2.0 AMP "SLOW-BLOW" FUSE
220/240 VAC	1.0 AMP "SLOW-BLOW" FUSE



1310A-3001

Figure 4. **Power Supply Assembly A15 Schematic Diagram (10121-3001 Rev. G)**

4. POWER SUPPLY FILTER ASSEMBLY A15A1 CIRCUIT DESCRIPTION

The A15A1 assembly contains voltage rectifiers and the large filter capacitors required to filter the input voltages from T1. The 52 Vac at J1-6 and J1-7 is full-wave rectified by CR1 and CR2 and filtered by C1 to produce an unregulated + 24 volts at J2-8.

The 36 Vac at J1-1 and J1-3 is full-wave rectified by CR3 and filtered by C2 and C3 to produce an unregulated + 15 volts at J2-1 and J2-2, and an unregulated -15 volts at J2-4. The unregulated 5 volts at E1 is heavily filtered by filter network C4-L1-C5 and made available at E2.

Table 3 is the A15A1 assembly parts list, figure 5 is the A15A1 component location diagram, and figure 6 is the A15A1 schematic diagram.

Table 3. Power Supply Filter Board Assembly A15A1 Parts List (10073-3100 Rev. J)

Ref. Desig.	Part Number	Description
6	J03-0001-029	FML FASTON 3/16 22-18AWG
7	J03-0004-002	LUG SOLDERLESS SLIP-ON
C1	C17-0050-282	CAP 2800UF 50V ELEC
C2	C17-0035-562	CAP 5600UF 35V ELEC
C3	C17-0035-212	CAP 2100UF 35V ELEC
C15	C17-0035-123	CAP 12000UF 35V ELEC
C19	C17-0035-123	CAP 12000UF 35V ELEC
CR1	D22-0006-001	DIODE 3A 600V RECT GP
CR2	D22-0006-001	DIODE 3A 600V RECT GP
CR3	D22-5011-200	DIODE 10A 200V RECT BR
E3	MP-0372	FAST-ON .125 PCB MOUNT
J1	J42-0004-007	CONN 7 PIN
J2	J46-0032-008	HDR 8 PIN 0.100" SR
L1	10073-3051	INDUCTOR,1MH 4 AMP

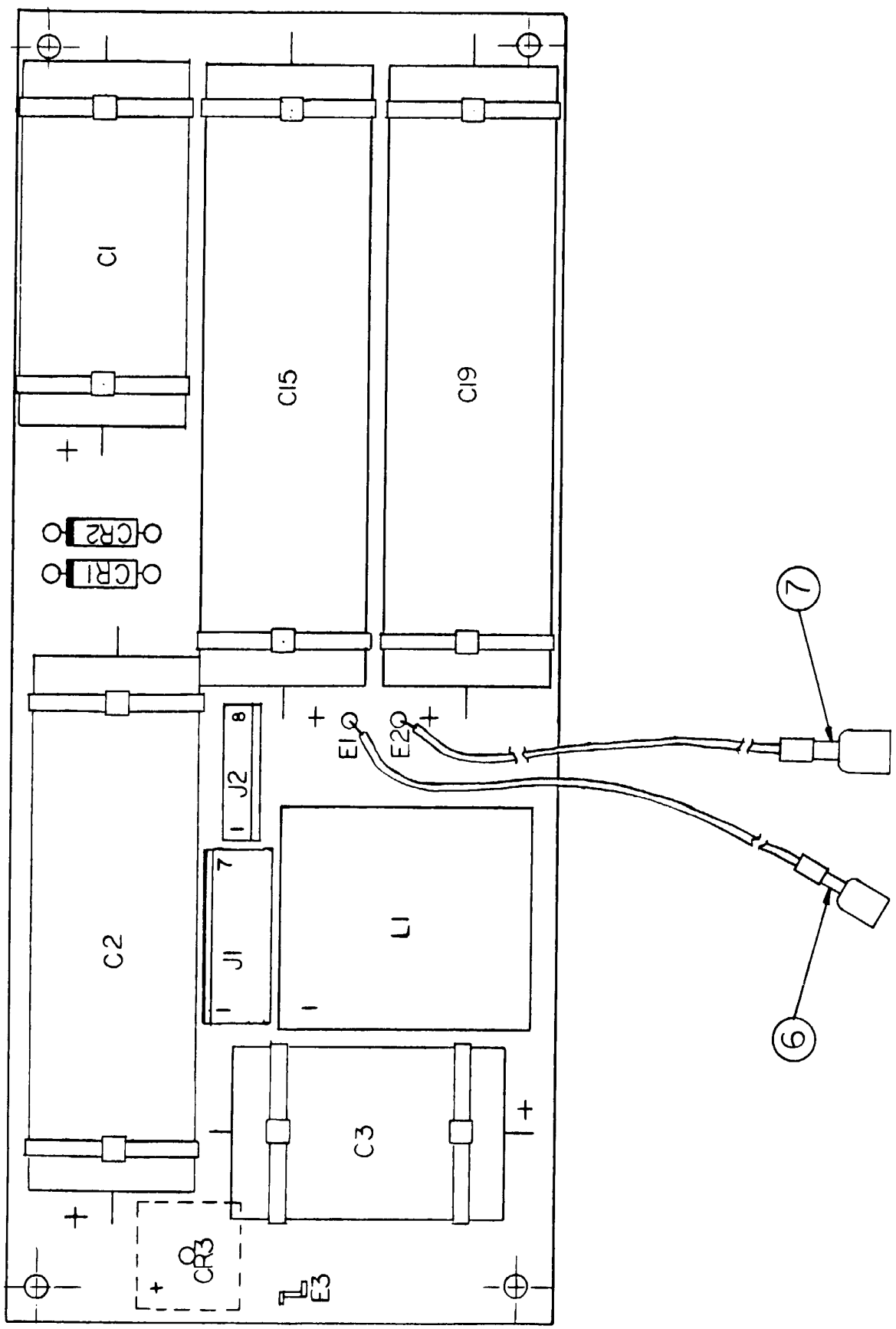


Figure 5. Power Supply Filter Board Assembly A15A1 Component Location Diagram (10073-3100 Rev. D)

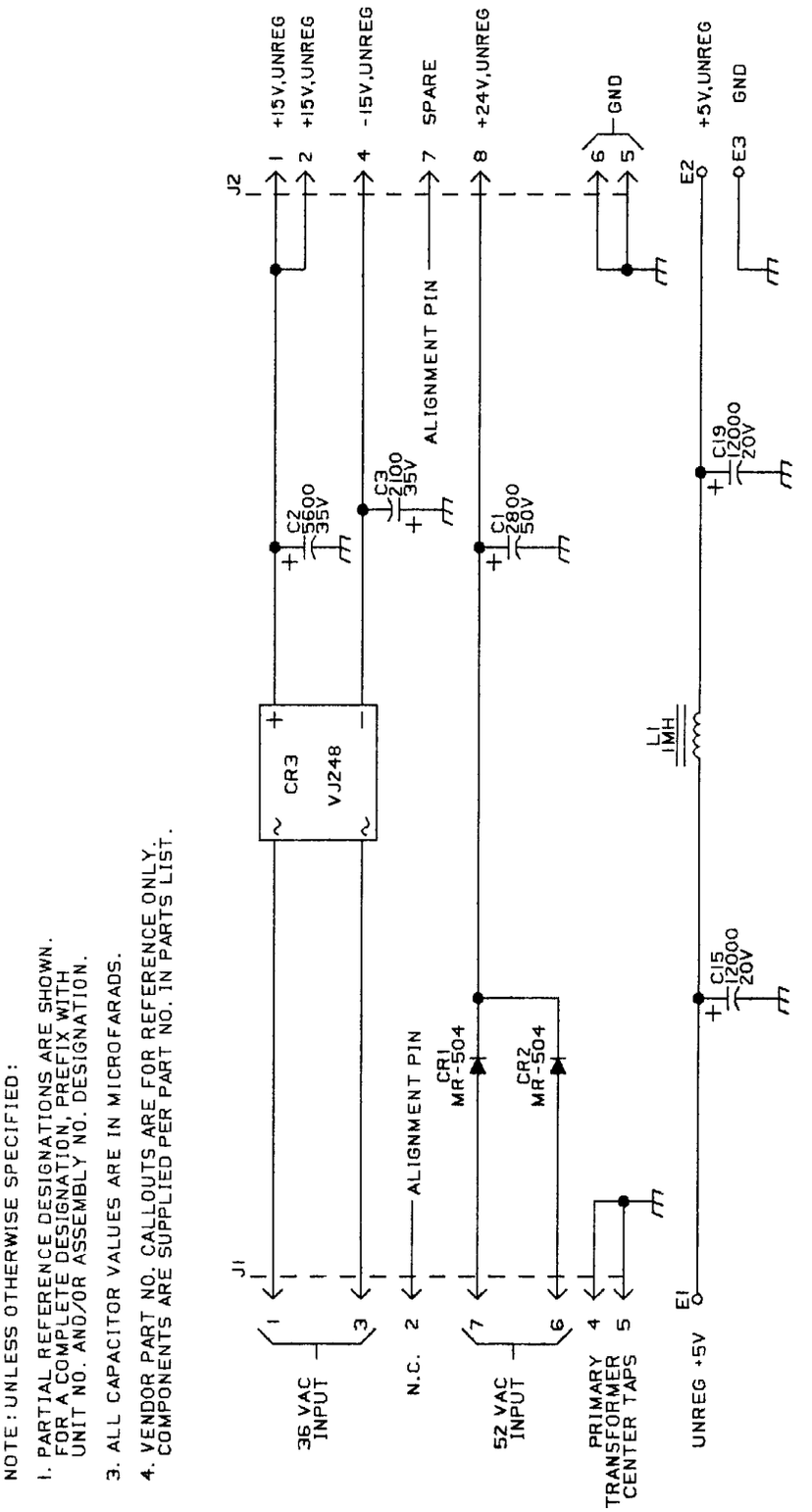


Figure 6. Power Supply Filter Assembly A15A1 Schematic Diagram (10073-3101 Rev. C)

5. POWER SUPPLY HEATSINK ASSEMBLY A15A2 CIRCUIT DESCRIPTION

Heatsink Assembly A15A2 consists of voltage regulators VR1 through VR6, CR1, and Regulator PWB A15A2A1. They are all mounted to a large heatsink bolted to the rear of the A15 assembly. Heatsink Assembly A15A2 may be removed from Power Supply Assembly A15 by removing the five mounting screws on the rear of the A15 assembly.

Regulator Assembly A15A2A1 receives the unregulated output voltages from the A15A1 assembly, and uses linear regulators mounted to Heatsink Assembly A15A2 to produce the regulated output voltages required. Table 4 lists the input voltages, the associated voltage regulator, and the output voltages.

Table 4. A15A2 Voltage Regulator Identification

Input Voltage	A15A2 Voltage Regulator	Output Voltage
+ 15 Unregulated	VR1	15 Vdc No. 1
+ 15 Unregulated	VR2	15 Vdc No. 2
-15 Unregulated	VR3	-15 Vdc
+ 5 Unregulated	VR4	+ 5 Vdc No. 1
+ 5 Unregulated	VR5	+ 5 Vdc No. 2
+ 24 Unregulated	VR6	+ 24 Vdc

All these voltages are routed through connector A15A2A1J3 (located on the bottom of the A15A2A1 PWB) for power distribution throughout the radio.

The A15A2A1 assembly also provides additional filtering to these voltages, as well as to a + 5 volt, unregulated output which does not receive any regulation. This supply voltage is regulated on the individual assemblies when used.

Table 5 is the A15A2 assembly parts list and figure 7 is the A15A2 assembly component location drawing. Table 6 is the A15A2A1 parts list and figure 8 is the A15A2A1 assembly component location drawing. Figure 9 is the A15A2 assembly and A15A2A1 assembly schematic diagram.

Table 5. Power Supply Heatsink Assembly A15A2 Parts List (10073-3250 Rev. K)

Ref. Desig.	Part Number	Description
	MO8-0001-051	INSL RUBBER/PLSTC FOR REG
A1	10073-3200	PWB ASSY, REGULATOR
CR1	D23-0001-201	DIODE 25A 200V RECT BR
VR1	I11-0001-006	IC VR 7815 +15V 1.5A 4%
VR2	I11-0001-006	IC VR 7815 +15V 1.5A 4%
VR3	I12-0002-005	IC VR 7915C -15V 1.5A 4%
VR4	I11-0001-001	IC VR 7805 +5V 1.5A 4%
VR5	I11-0001-001	IC VR 7805 +5V 1.5A 4%
VR6	IC-0358	IC VR 317 ADJ V 1.5A

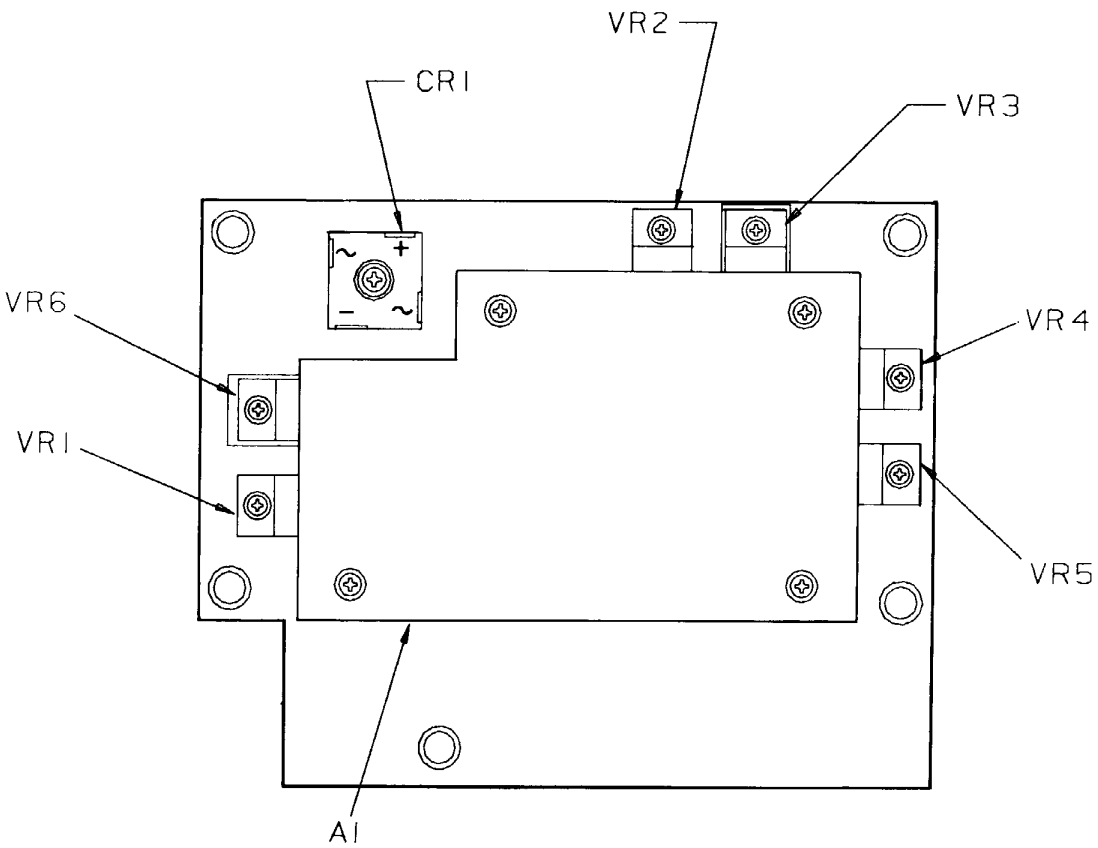
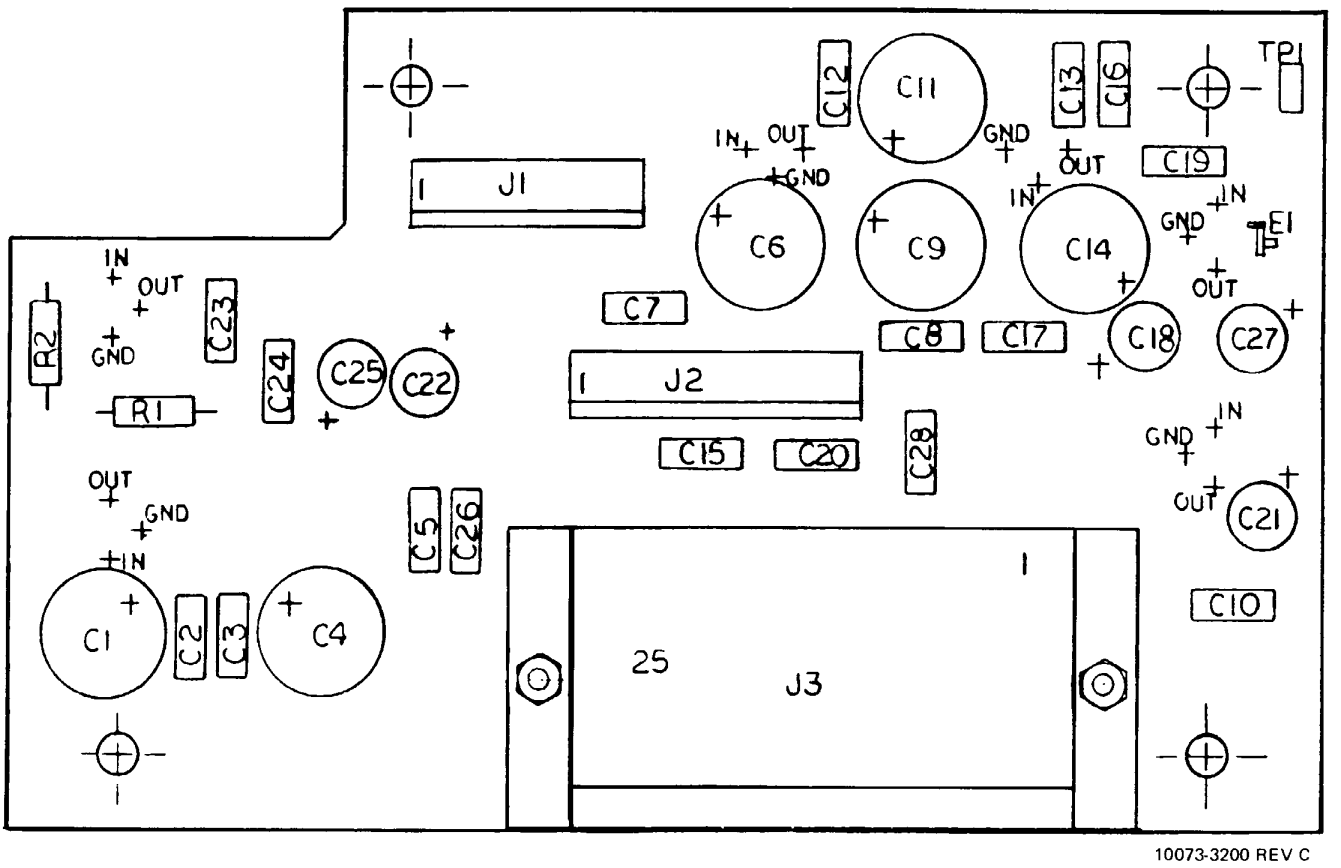


Figure 7. Power Supply Heatsink Assembly A15A2 Component Location Diagram (10073-3250 Rev. D)

Table 6. Power Supply Regulator Assembly A15A2A1 Parts List (10073-3200 Rev. K)

Ref. Desig.	Part Number	Description
C1	C26-0050-100	CAP 10UF 20% 50V TANT
C2	M39014/02-1320V	CAP .47UF 10% 50V CER-R
C3	M39014/02-1320V	CAP .47UF 10% 50V CER-R
C4	C26-0025-680	CAP 68UF 20% 25V TANT
C5	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C6	C26-0050-100	CAP 10UF 20% 50V TANT
C7	M39014/02-1320V	CAP .47UF 10% 50V CER-R
C8	M39014/02-1320V	CAP .47UF 10% 50V CER-R
C9	C26-0025-680	CAP 68UF 20% 25V TANT
C10	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C11	C26-0050-100	CAP 10UF 20% 50V TANT
C12	M39014/02-1320V	CAP .47UF 10% 50V CER-R
C13	M39014/02-1320V	CAP .47UF 10% 50V CER-R
C14	C26-0025-680	CAP 68UF 20% 25V TANT
C15	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C16	M39014/02-1320V	CAP .47UF 10% 50V CER-R
C17	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C18	C26-0016-150	CAP 15UF 20% 16V TANT
C19	M39014/02-1320V	CAP .47UF 10% 50V CER-R
C20	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C21	C26-0016-150	CAP 15UF 20% 16V TANT
C22	C25-0003-015	CAP 22UF 10% 50V TANT
C23	M39014/02-1320V	CAP .47UF 10% 50V CER-R
C24	M39014/02-1320V	CAP .47UF 10% 50V CER-R
C25	C25-0003-015	CAP 22UF 10% 50V TANT
C26	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C27	C25-0003-313	CAP 100UF 10% 20V TANT
C28	M39014/02-1310V	CAP .1UF 10% 100V CER-R
E1	MP-0372	FAST-ON .125 PCB MOUNT
J1	J46-0032-008	HDR 8 PIN 0.100" SR
J2	J46-0032-010	HDR 10 PIN 0.100" SR
J3	J20-0009-425	747461-6 AMP RECEPTACLE
R1	RN55D2430F	RES 243 1% 1/8W MET FLM
R2	RN55D4421F	RES 4420 1% 1/8W MET FLM
TP1	J-0392	TP PWB BRN RA SIDE ACCESS



10073-3200 REV C

Figure 8. Power Supply Regulator Assembly A15A2A1 Component Location Diagram (10073-3200 Rev. C)

NOTE: UNLESS OTHERWISE SPECIFIED:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR A COMPLETE DESIGNATION, PREFIX WITH UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.
2. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, ±5%.
3. ALL CAPACITOR VALUES ARE IN MICROFARADS.
4. VENDOR PART NO. CALLOUTS ARE FOR REFERENCE ONLY. COMPONENTS ARE SUPPLIED PER PART NO. IN PARTS LIST.

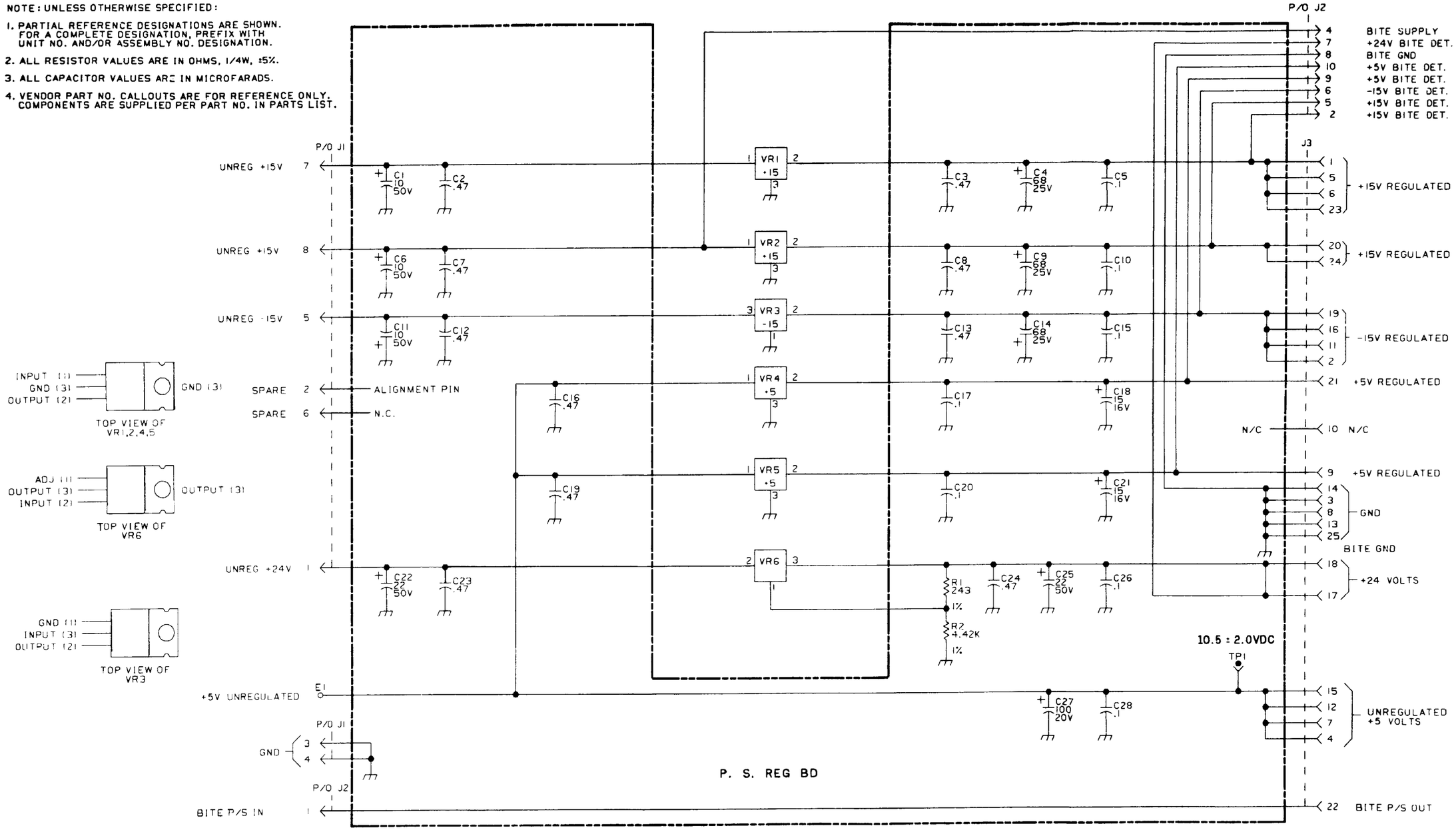


Figure 9. **Power Supply Heatsink Assembly A15A2 and Power Supply Regulator Assembly A15A2A1 Schematic Diagram (10073-3201 Rev. F)**

6. POWER SUPPLY BITE DETECTOR ASSEMBLY A15A3 CIRCUIT DESCRIPTION

The A15A3 assembly monitors the regulated output voltages listed in table 4 and will issue a fault signal to Control Board Assembly A14 if any of them exceeds a defined upper or lower limit. The A14 assembly will then issue a fault command and turn on the RF-1310 front panel fault indicator. This operation is performed continually while the exciter is operating.

The general operation scheme of the assembly is as follows, using the + 5 Vdc from the A15A2 assembly at A15A3 J1-2 as an example.

The + 5 Vdc at pin 2 is divided by resistor network R13-R14 to place a nominal 3.1 Vdc at U2D-10 (-) and U2C-9 (+). This level will be referred to as V_{TEST}. The + 8 Vdc from VR1 is divided by R1 and R3 to place + 4 Vdc at U2D-11 (+), and by R2 and R4 to place + 2 Vdc at U2C-8 (-). The + 4 Vdc level will be referred to as V_{HI}; the + 2 Vdc level as V_{LO}. These two levels establish the limits that V_{TEST} must not exceed.

Under conditions where V_{LO} is less than V_{TEST} is less than V_{HI}, U2C and U2D outputs are at + 8 volts. This feeds to U3C-8 (-). Since U3C-9 (+) input is always held fixed at 4 Vdc (V_{HI}), U3C output will be low (0 Vdc), Q1 will be biased off, and the BITE output signal will be at + 8 Vdc. This notifies the BITE circuits that the + 5 Vdc level is within its limits.

If V_{TEST} exceeds V_{HI}. U2D output switches 0 Vdc, causing U3C to switch to + 8 Vdc, turning on Q1. Q1 output drags the BITE output to 0 Vdc, and notifies the BITE circuits of an error condition. The same events occur if V_{TEST} falls below V_{LO}, except that now U2C output affects the switching of U3C.

This concept of a comparator pair providing the lower and upper limits is used to monitor the other regulated input voltages. Since all the comparator outputs are tied together, any one of them changing states would cause Q1 to issue an error signal.

Note that there are five comparator pairs, but six input voltages. The -15 Vdc input is used as a reference (instead of ground) for the two + 15 Vdc and one + 24 Vdc inputs, thereby eliminating the need for a separate comparator pair to monitor the -15 Vdc.

The approximate range of upper and lower input limits which will not trip the comparators is given in table 7.

Table 7. A15A3 BITE Detector Trip Limits

Input Voltage Vdc	Permissible Voltage Range
+ 5 Vdc No. 1	approximately 3.0 to 6.5
+ 5 Vdc No. 2	approximately 3.0 to 6.5
+ 15 vdc No. 1	approximately 13.0 to 17.0
+ 15 Vdc No. 2	approximately 13.0 to 17.0
-15 Vdc	approximately -13.0 to -17.0
+ 24 Vdc	approximately 21 to 26

Table 8 is the A15A3 assembly parts list, figure 10 is the A15A3 assembly component location diagram, and figure 11 is the A15A3 schematic diagram.

Table 8. Power Supply BITE Assembly A15A3 Parts List (10073-3300 Rev. H)

Ref. Desig.	Part Number	Description
C1	M39014/02–1310V	CAP .1UF 10% 100V CER–R
C2	C26-0025-100	CAP 10UF 20% 25V TANT
C3	M39014/02-1310V	CAP .1UF 10% 100V CER-R
J1	J46-0032-010	HDR 10 PIN 0.100" SR
Q1	2N2222	XSTR SS/GP NPN TO-18
R1	RN55D4021F	RES 4020 1% 1/8W MET FLM
R2	RN55D7501F	RES 7500 1% 1/8W MET FLM
R3	RN55D4021F	RES 4020 1% 1/8W MET FLM
R4	RN55D2491F	RES 2490 1% 1/8W MET FLM
R5	RN55D1212F	RES 12.1K 1% 1/8W MET FLM
R6	RN55D1822F	RES 18.2K 1% 1/8W MET FLM
R7	RN55D1212F	RES 12.1K 1% 1/8W MET FLM
R8	RN55D1822F	RES 18.2K 1% 1/8W MET FLM
R9	RN55D1822F	RES 18.2K 1% 1/8W MET FLM
R10	RN55D2102F	RES 21.0K 1% 1/8W MET FLM
R11	RN55D1821F	RES 1820 1% 1/8W MET FLM
R12	RN55D3011F	RES 3010 1% 1/8W MET FLM
R13	RN55D1821F	RES 1820 1% 1/8W MET FLM
R14	RN55D3011F	RES 3010 1% 1/8W MET FLM
R15	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R16	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
R17	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R18	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R19	R65-0003-103	RES 10K 5% 1/4W CAR FILM
TP1	J-0392	TP PWB BRN RA SIDE ACCESS
TP2	J-0387	TP PWB RED RA SIDE ACCESS
TP3	J-0390	TP PWB ORN RA SIDE ACCESS
TP4	J-0391	TP PWB YEL RA SIDE ACCESS
TP5	J-0389	TP PWB GRN RA SIDE ACCESS
TP6	J-0393	TP PWB BLU RA SIDE ACCESS
U1	I20-0006-000	IC LM339 COMPARATOR PL
U2	I20-0006-000	IC LM339 COMPARATOR PL
U3	I20-0006-000	IC LM339 COMPARATOR PL
VR1	I12-0006-008	IC VR 78L08A +8V .10A 4%

7. A15 ASSEMBLY REMOVAL

WARNING

Potentially hazardous high voltages are present inside the A15 assembly whenever the exciter is connected to an ac line source. Do not attempt any repair to this assembly unless the line cord is disconnected. Do not operate the exciter without the protective cover properly installed over the assembly.

a. Disconnect the ac line cord.

b. Disconnect connectors W3P1, W4P1, and W5P1 in the channel on the bottom side of the exciter (underneath the A15 assembly). These carry the switched ac power to the front panel, the a23 ac power input, and the switched ac power to the fan, respectively. Cut the tywrap for the fan cable.

c. Remove mounting screws securing the A15 assembly cover, and remove cover.

d. Loosen the two captive screws inside the A15 assembly securing it to the chassis.

e. Place exciter on its side.

f. Remove four rear panel corner screws holding rear panel to chassis.

g. Disconnect A15J3.

h. Carefully pull the A15 assembly away from chassis. The rear portion of the chassis will not be supported after the A15 assembly is removed.

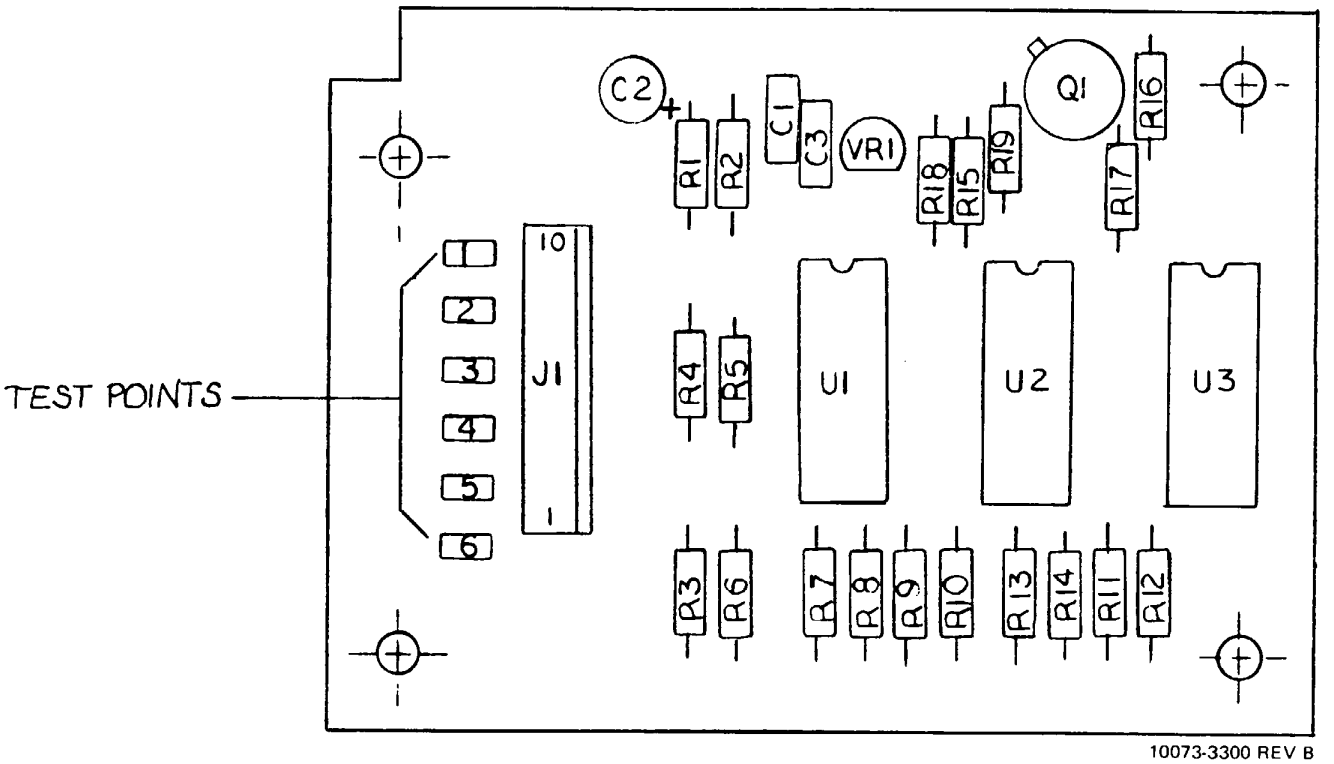
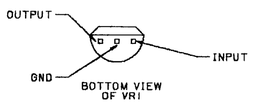


Figure 10. Power Supply BITE Assembly A15A3 Component Location Diagram (10073-3300 Rev. B)

NOTE: UNLESS OTHERWISE SPECIFIED:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR A COMPLETE DESIGNATION, PREFIX WITH UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.
2. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, ±5%.
3. ALL CAPACITOR VALUES ARE IN MICROFARADS.
4. VENDOR PART NO. CALLOUTS ARE FOR REFERENCE ONLY. COMPONENTS ARE SUPPLIED PER PART NO. IN PARTS LIST.
5. SEE GRAPHICS BELOW.



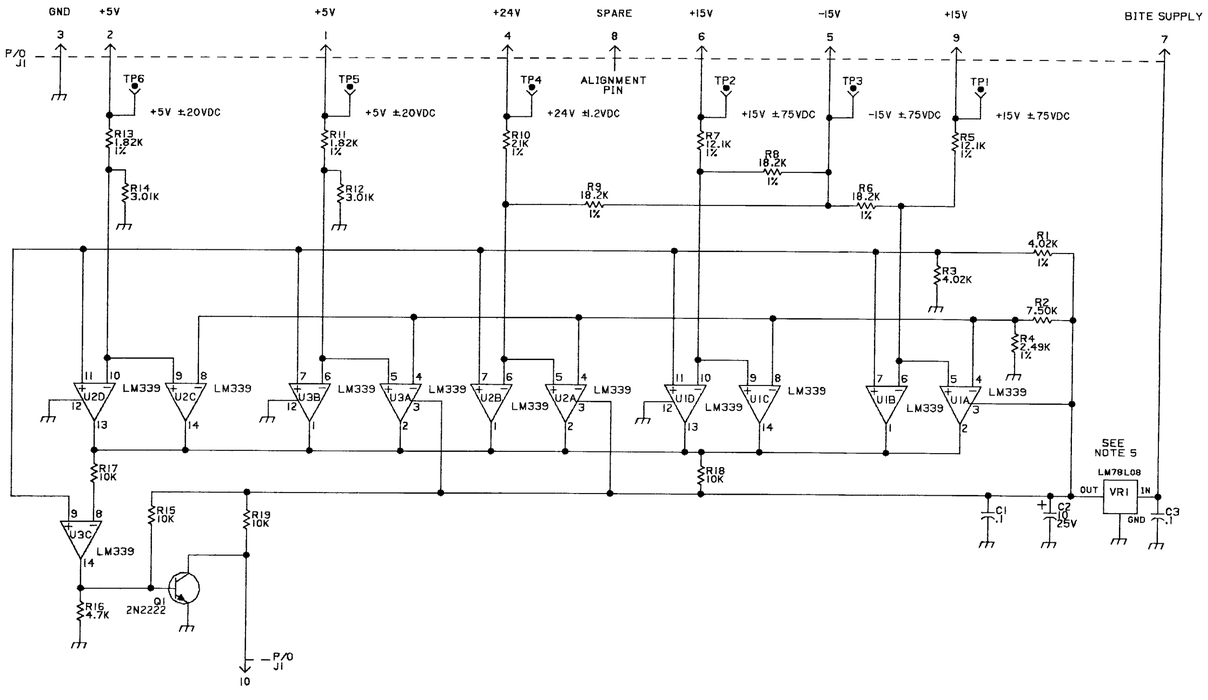
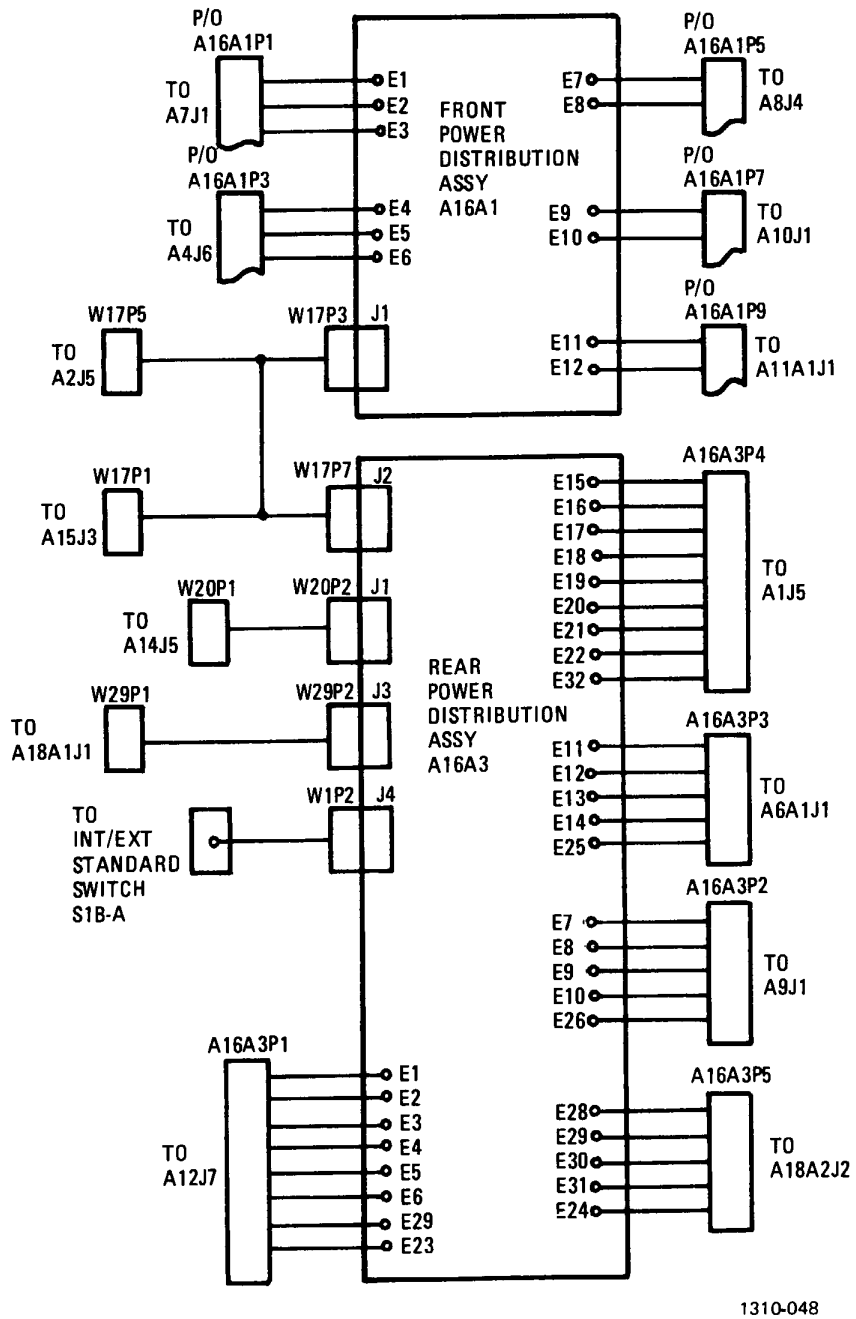


Figure 11. **Power Supply BITE Assembly A15A3 Schematic Diagram (10073-3301 Rev. D)**

A16

POWER DISTRIBUTION ASSEMBLIES



1310-048

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LIST OF FIGURES

LIST OF TABLES

POWER DISTRIBUTION ASSEMBLIES A16

1. GENERAL INFORMATION

Power distribution assemblies A16A1 and A16A3 are used to interface the power supply with other assemblies in the exciter. The two boards also distribute nonpower signals. Front Power Distribution Assembly A16A1 is located behind the front panel on the bottom side of the main chassis. Rear Power Distribution Assembly A16A3 is mounted on the bottom side of the main chassis inside the rear panel assembly. Figure 1 shows the locations of the two assemblies. The assemblies provide some filtering and have several connectors for making connections to other assemblies.

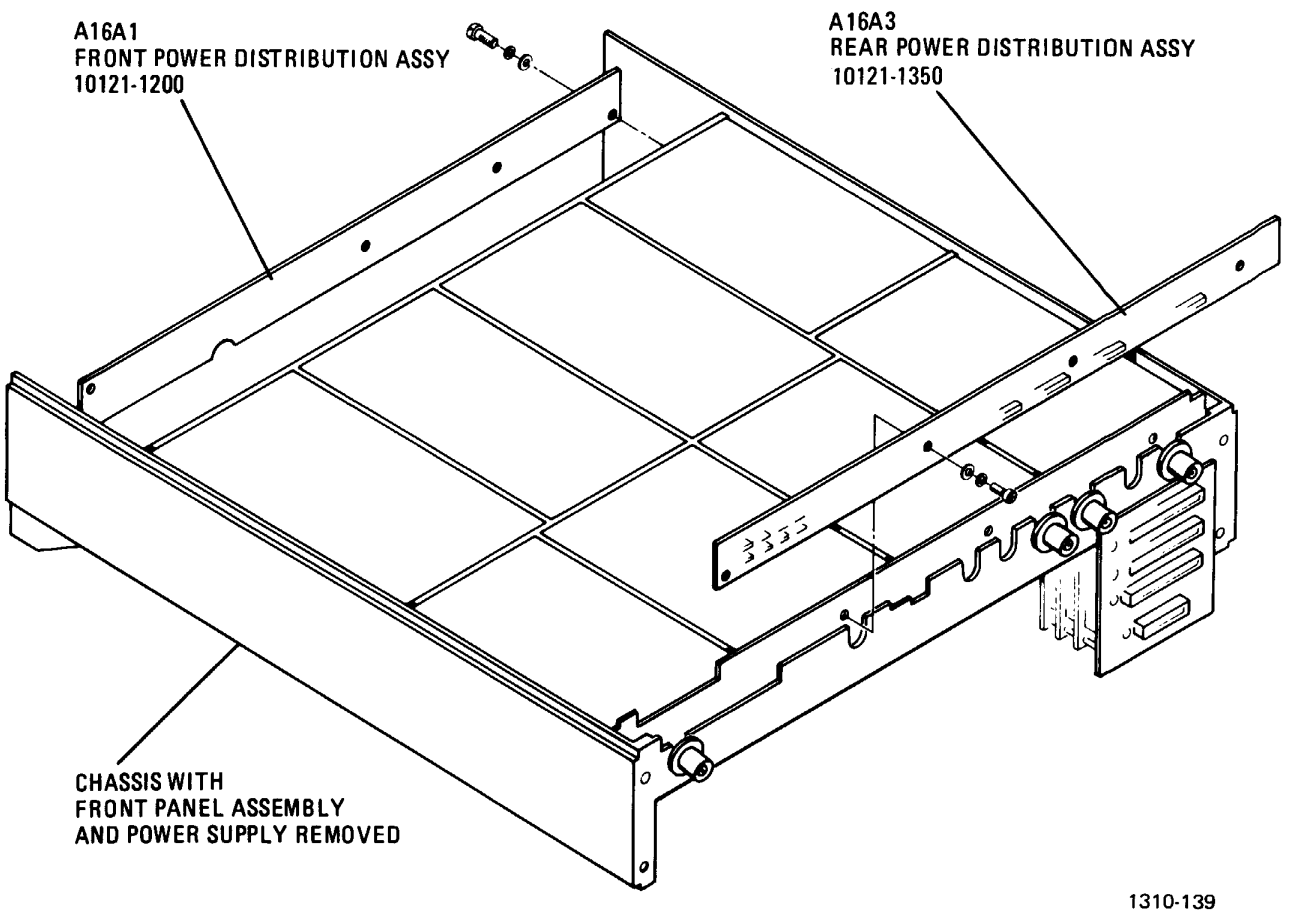


Figure 1. Power Distribution Board Location

2. INTERCONNECTIONS

Connections with the power supply and the other assemblies are shown in figure 6 of the Major Assembly Location subsection.

3. PARTS LISTS, COMPONENT LOCATIONS, AND SCHEMATIC DIAGRAMS

Table 1 lists components of the A16A1 assembly. These components are shown in figure 2. The Front Power Distribution Assembly circuit is shown in figure 3. Table 2 lists the components of the A16A3 assembly. The components are shown in figure 4. The Rear Power Distribution circuit is shown in figure 5.

Table 1. Front Power Distribution Assembly A16A1 Parts List (10121-1200 Rev. D)

Ref. Desig.	Part Number	Description
C1	M39014/01-1317V	CAP,1000PF,10% 200VC
C2	M39014/01-1317V	CAP,1000PF,10% 200VC
C3	M39014/01-1317V	CAP,1000PF,10% 200VC
C4	M39014/01-1317V	CAP,1000PF,10% 200VC
C5	M39014/01-1317V	CAP,1000PF,10% 200VC
C6	M39014/01-1317V	CAP,1000PF,10% 200VC
C7	M39014/01-1317V	CAP,1000PF,10% 200VC
C8	M39014/01-1317V	CAP,1000PF,10% 200VC
C9	M39014/01-1317V	CAP,1000PF,10% 200VC
J1	J46-0033-008	HDR 8 PIN 0.100" RT ANG
P9	J46-0016-003	CONN HOUSING 3 POS 24AWG
W1	10073-7061	RIBBON CABLE, 7 COND
W2	10073-7057	RIBBON CABLE, 24 COND
W3	10073-7057	RIBBON CABLE, 24 COND
W6	10121-7282	CABLE, CONTROL/COMBINER

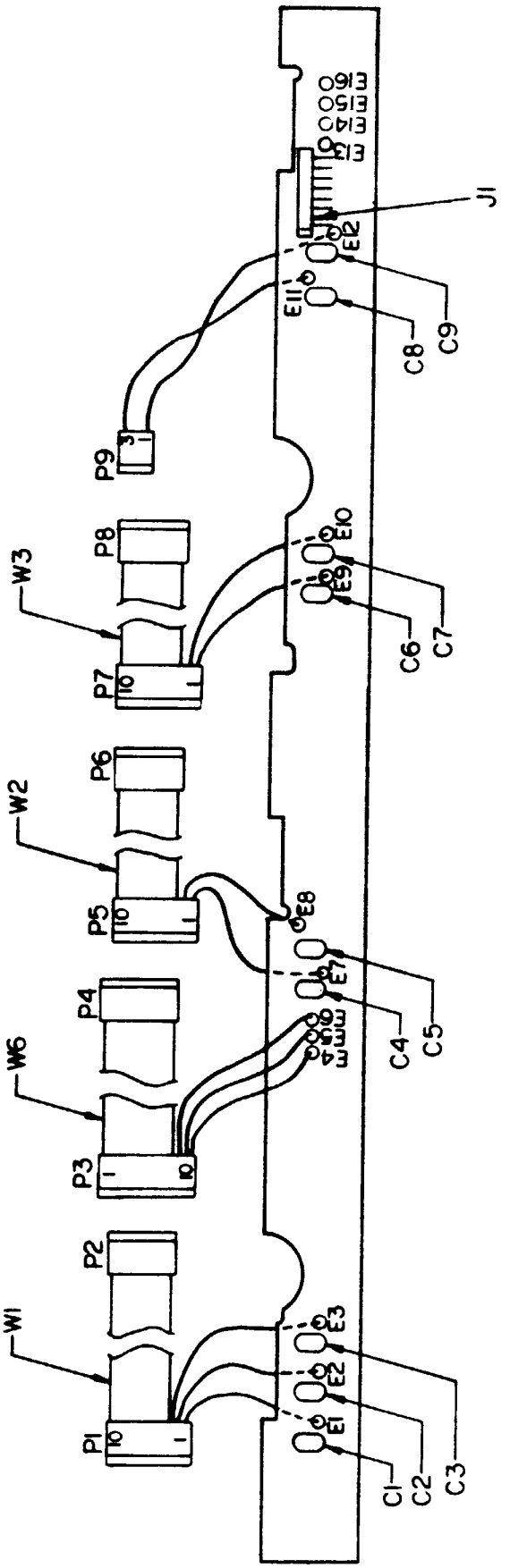


Figure 2. Front Power Distribution Assembly A16A1 Component Location Diagram (10121-1200 Rev. C)

NOTE: UNLESS OTHERWISE SPECIFIED:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR A COMPLETE DESIGNATION, PREFIX WITH UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.
2. ALL CAPACITOR VALUES ARE .001 MICROFARADS.

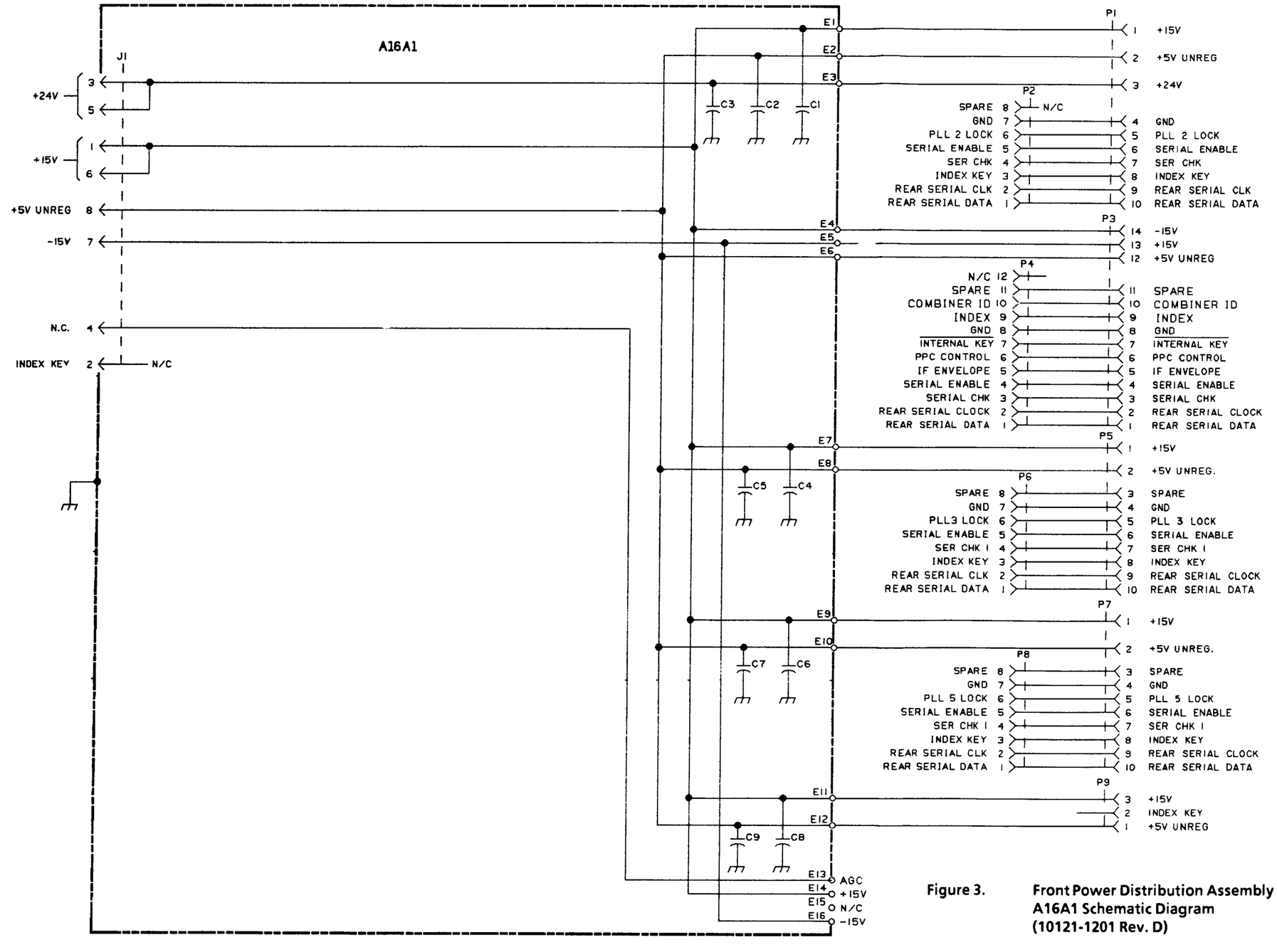


Figure 3. **Front Power Distribution Assembly A16A1 Schematic Diagram (10121-1201 Rev. D)**

Table 2. Rear Power Distribution Assembly A16A3 Parts List (10121-1350-01 Rev. B)

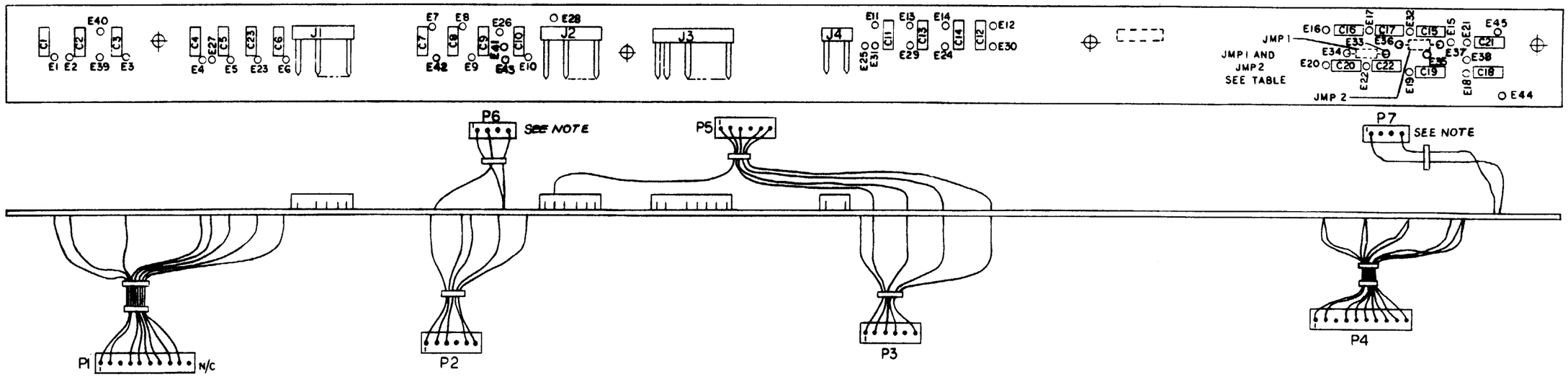
Ref. Desig.	Part Number	Description
6	J45-0039-000	KEYING PLUG
C1	M39014/01-1317V	CAP,1000PF,10% 200VC
C2	M39014/01-1317V	CAP,1000PF,10% 200VC
C3	M39014/01-1317V	CAP,1000PF,10% 200VC
C4	M39014/01-1317V	CAP,1000PF,10% 200VC
C5	M39014/01-1317V	CAP,1000PF,10% 200VC
C6	M39014/01-1317V	CAP,1000PF,10% 200VC
C7	M39014/01-1317V	CAP,1000PF,10% 200VC
C8	M39014/01-1317V	CAP,1000PF,10% 200VC
C9	M39014/01-1317V	CAP,1000PF,10% 200VC
C10	M39014/01-1317V	CAP,1000PF,10% 200VC
C11	M39014/01-1317V	CAP,1000PF,10% 200VC
C12	M39014/01-1317V	CAP,1000PF,10% 200VC
C13	M39014/01-1317V	CAP,1000PF,10% 200VC
C14	M39014/01-1317V	CAP,1000PF,10% 200VC
C15	M39014/01-1317V	CAP,1000PF,10% 200VC
C16	M39014/01-1317V	CAP,1000PF,10% 200VC
C17	M39014/01-1317V	CAP,1000PF,10% 200VC
C18	M39014/01-1317V	CAP,1000PF,10% 200VC
C19	M39014/01-1317V	CAP,1000PF,10% 200VC
C20	M39014/01-1317V	CAP,1000PF,10% 200VC
C21	M39014/01-1317V	CAP,1000PF,10% 200VC
C22	M39014/01-1317V	CAP,1000PF,10% 200VC
C23	M39014/01-1317V	CAP,1000PF,10% 200VC
J1	J46-0033-006	HDR 6 PIN 0.100" RT ANG
J2	J46-0033-006	HDR 6 PIN 0.100" RT ANG
J3	J46-0033-008	HDR 8 PIN 0.100" RT ANG
J4	J46-0033-003	HDR 3 PIN 0.100" RT ANG
JMP1	MP-1142	RES ZERO OHM (CKT JMPR)
P1	J46-0016-010	CONN HOUSING 10 POS 24AWG
P2	J46-0016-006	CONN HOUSING 6 POS 24AWG
P3	J46-0016-006	CONN HOUSING 6 POS 24AWG
P4	J46-0016-010	CONN HOUSING 10 POS 24AWG
P5	J46-0016-006	CONN HOUSING 6 POS 24AWG

NOTES:

1. COMPLETED ASSY SHALL BE IN ACCORDANCE WITH QC-3000.
2. REMOVE THE FOLLOWING PINS FROM CONNECTOR BODY:
   - J1 PIN 2
   - J2 PIN 2 (USE PIN 2 MOUNTING HOLE FOR E28)
   - J3 PIN 3

WIRE RUN LIST

FROM	TO	COLOR	ITEM #	LENGTH TOL=±.25	FROM	TO	COLOR	ITEM #	LENGTH TOL=±.25	FROM	TO	COLOR	ITEM #	LENGTH TOL=±.25
P5-1	E29	BRN	8	12.00	P1-8	E27	GRY	15	6.50	P3-5	KEY	-	6	-
P5-2	E31	RED	9	12.00	P1-9	E23	WHT	16	5.25	P3-6	E12	BLU	13	6.75
P5-3	E28	ORN	10	14.75										
P5-4	KEY	-	6	-	P2-1	E26	BRN	8	3.20	P4-1	E32	BRN	8	5.50
P5-5	E30	GRN	12	11.75	P2-2	E7	RED	9	3.20	P4-2	E16	RED	9	6.00
P5-6	E24	BLU	13	11.75	P2-3	E8	ORN	10	3.20	P4-3	KEY	-	6	-



NOTE:
P6 AND P7 ARE INSTALLED IN THE 10121-1350-03 ASSY ONLY. SEE TABLE BELOW.

CONNECT JMP1 AND JMP2 AS FOLLOWS

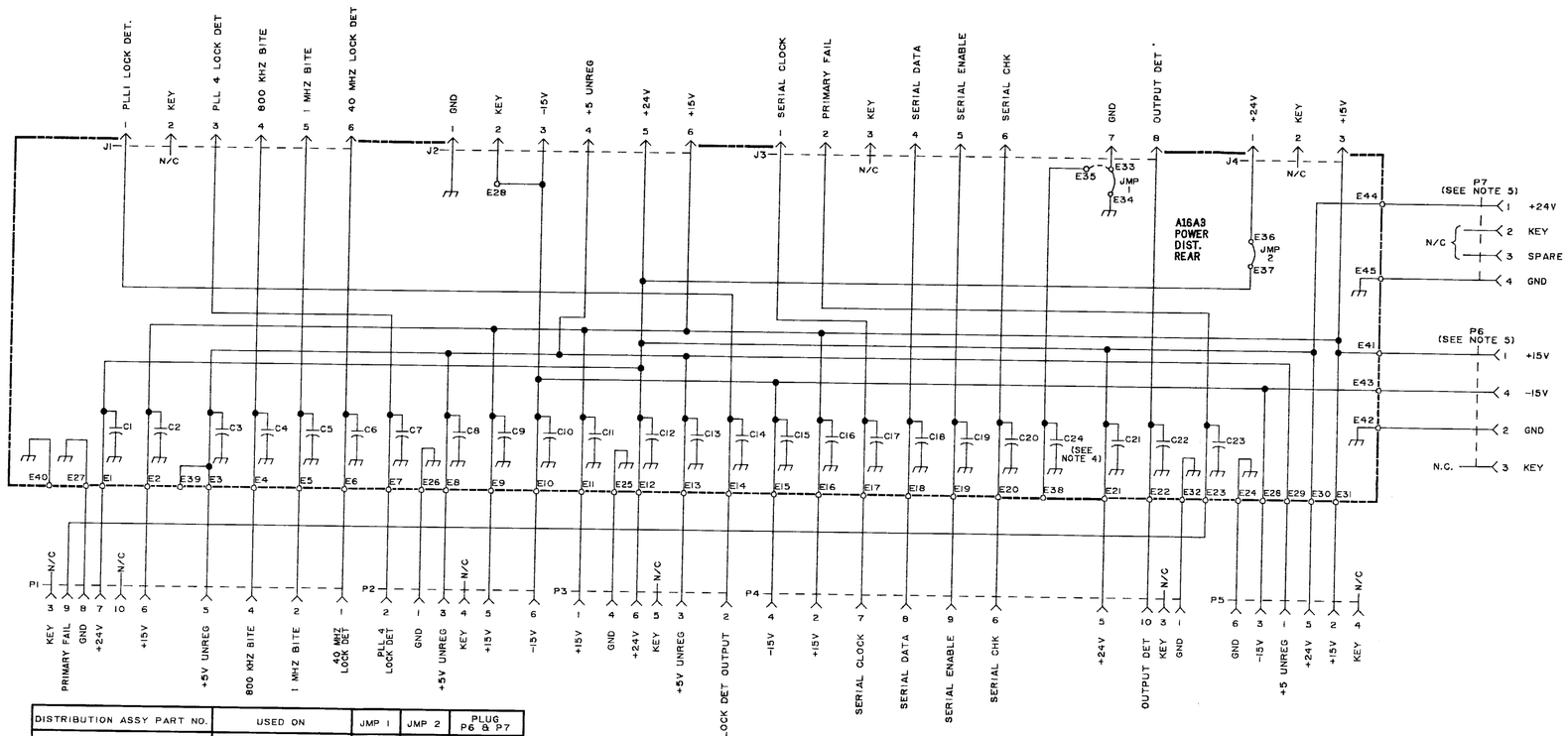
DISTRIBUTION ASSY PART NO.	USED ON	JMP 1	JMP 2	PLUG P6 & P7
10121-1350-01	RF-1310 WITH A23 424V POWER SUPPLY ASSY	E33 TO E34	DO NOT INSTALL	DO NOT INSTALL
10121-1350-02	RF-1310A WITH A23 FREQUENCY STANDARD SYNCHRONIZATION DETECTOR ASSY	E33 TO E34	E36 TO E37	DO NOT INSTALL
10121-1350-03	RF-1310 WITH A25 AUDIO/KEY PWB ASSY, A24 INTERNAL RF-601A COUPLER CONTROL ASSY, AND A27 INTERSELECTOR AMPLIFIER ASSY.	E33 TO E34	E36 TO E37	INSTALLED

TABLE I

Figure 4. Rear Power Distribution Assembly A16A3 Component Location Diagram (10121-1350 Rev. F)

NOTE: UNLESS OTHERWISE SPECIFIED:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR A COMPLETE DESIGNATION, PREFIX WITH UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.
2. ALL CAPACITOR VALUES ARE 1000 PICOFARADS.
3. SEE TABLE I FOR JMP1 & JMP2 CONNECTION.
4. THE 10121-1359 PWB IS COMMON TO THE 10121-1350-01/02/03 AND THE 10073-1350. FOR APPLICATION OF THIS PWB INTO THE RF-590 (10073-1350), JMP 1 IS INSTALLED E33 TO E35 AND C24 IS ADDED.
5. INSTALL P6 AND P7 IN THE 10121-1350-03 ASSEMBLY ONLY. SEE TABLE I BELOW.

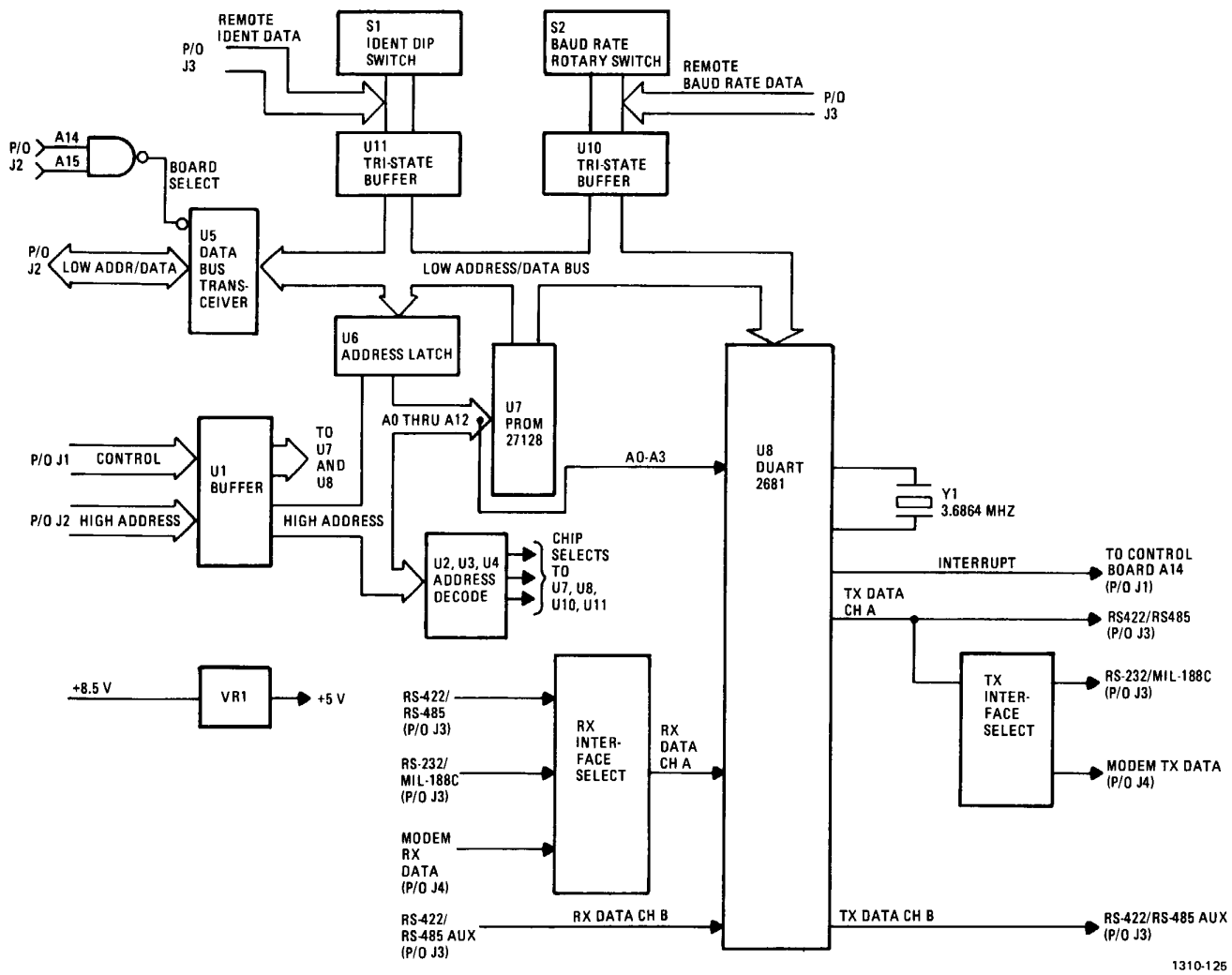


DISTRIBUTION ASSY PART NO.	USED ON	JMP 1	JMP 2	PLUG P6 & P7
10121-1350-01	RF-1310 WITH A23 +24V POWER SUPPLY ASSY	E33 TO E34	DO NOT INSTALL	DO NOT INSTALL
10121-1350-02	RF-1310A WITH A23 FREQUENCY STANDARD SYNCHRONIZATION DETECTOR ASSY	E33 TO E34	E36 TO E37	DO NOT INSTALL
10121-1350-03	RF-1310 WITH A25 AUDIO/KEY PWB ASSY, A24 INTERNAL RF-601A COUPLER CONTROL ASSY, AND A27 INTERSELECTOR AMPLIFIER ASSY.	E33 TO E34	E36 TO E37	INSTALLED

TABLE 1

Figure 5. Rear Power Distribution Assembly A16A3 Schematic Diagram (10121-1351 Rev. E)

A17A1
REMOTE CONTROL ASSEMBLY



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REMOTE CONTROL ASSEMBLY A17A1

1. GENERAL DESCRIPTION

Remote Control Assembly A17A1 permits control of the RF-1310 Exciter from a remote site. Connected to the microprocessor controlling the RF-1310, this assembly contains interface buffering to Control Board Assembly A14, additional program memory, and circuits for parallel I/O and serial I/O controls. It works as a local control unit (LCU) for the exciter, providing RS-232C, MIL-STD-188C, RS-422, and FSK (using the optional A17A2 Modem Assembly) interface options to a distant remote control unit (RCU). The software programming using one, 16K byte EPROM interfaces the A17A1 assembly control and provides communications to the main control software on the A14 assembly. Electrical connection to the exciter from the A17A1 assembly is through ribbon cables to the A14 assembly and to interface connectors J8 and J9 on the RF-1310 rear panel.

2. INTERFACE CONNECTIONS

Assembly A17A1 interface connections are listed in table 1.

Table 1. Remote Control Assembly A17A1 Interface Summary

Connector	Function	To	From
A17A1J1-1	+ 5 V UNREG.	----	A14J15-1
A17A1J1-2	+ 5 V UNREG.	----	A14J15-2
A17A1J1-3	RESET OUT	----	A15J15-3
A17A1J1-4	HOLD	A14J15-4	----
A17A1J1-5	REMOTE LINE AUDIO	A14J15-5	----
A17A1J1-6	HLDA	----	A14J15-6
A17A1J1-7	REMOTE LINE AUDIO GND	A14J15-7	----
A17A1J1-8	CPU CLK OUT	----	A14J15-8
A17A1J1-9	+ 15 V	----	A14J15-9
A17A1J1-10	GND	----	A14J15-10
A17A1J1-11	READY	A14J15-11	----
A17A1J1-12	-15 V	----	A14J15-12
A17A1J1-13	RST 5.5	A14J15-13	----
A17A1J1-14	IO/M	----	A14J15-14
A17A1J1-15	INTR	A14J15-15	----
A17A1J1-16	S1	----	A14J15-16
A17A1J1-17	$\overline{WR}$	----	A14J15-17
A17A1J1-18	$\overline{RD}$	----	A14J15-18
A17A1J1-19	INTA	----	A14J15-19
A17A1J1-20	ALE	----	A14J15-20
A17A1J2-1	N/C	----	----
A17A1J2-2	N/C	----	----
A17A1J2-3	AD0	BIDIRECTIONAL	A14J15-23
A17A1J2-4	N/C	----	----
A17A1J2-5	AD1	BIDIRECTIONAL	A14J15-25
A17A1J2-6	A15	----	A14J15-26
A17A1J2-7	AD2	BIDIRECTIONAL	A14J15-27

Table 1. Remote Control Assembly A17A1 Interface Summary (Cont.)

Connector	Function	To	From
A17A1J2-8	A14	----	A14J15-28
A17A1J2-9	AD3	BIDIRECTIONAL	A14J15-29
A17A1J2-10	A13	----	A14J15-30
A17A1J2-11	AD4	BIDIRECTIONAL	A14J15-31
A17A1J2-12	A12	----	A14J15-32
A17A1J2-13	AD5	BIDIRECTIONAL	A14J15-33
A17A1J2-14	A11	----	A14J15-34
A17A1J2-15	AD6	BIDIRECTIONAL	A14J15-35
A17A1J2-16	A10	----	A14J15-36
A17A1J2-17	AD7	BIDIRECTIONAL	A14J15-37
A17A1J2-18	A9	----	A14J15-38
A17A1J2-19	Gnd	----	A14J15-39
A17A1J2-20	A8	----	A14J15-40
A17A1J3-1	BUS AVAILABLE(AUX RS-485 OUT +)	----	J9-21
A17A1J3-2	RS-422 IN (REM RS-485 -)	----	J9-20
A17A1J3-3	BUS REQUEST (AUX RS-485 OUT -)	J9-3	----
A17A1J3-4	SPARE (AUX RS-485 IN +)	----	J9-8
A17A1J3-5	RS-422 OUT +	J9-4	----
A17A1J3-6	SPARE (AUX RS-485 IN -)	----	J9-9
A17A1J3-7	RS-422 IN + (REM RS-485 +)	----	J9-6
A17A1J3-8	RS-422 OUT-	J9-37	----
A17A1J3-9	GND	J9-19	----
A17A1J3-10	SHIELD (GND)	J8-1	----
A17A1J3-11	SPARE	----	----
A17A1J3-12	RS-232C/MIL-188 OUT	J8-2	----
A17A1J3-13	ID3	----	J8-15
A17A1J3-14	RS-232C/MIL-188 IN	----	J8-3
A17A1J3-15	ID2	----	J8-16
A17A1J3-16	FSK DATA OUT- (FSK T/R -)	J8-4	----
A17A1J3-17	ID5	----	J8-17
A17A1J3-18	FSK DATA IN + (FSK T/R +)	----	J8-5
A17A1J3-19	ID6	----	J8-18
A17A1J3-20	ID0	----	J8-6
A17A1J3-21	GND	J8-19	----
A17A1J3-22	RS-232 SIG. GND	J8-7	----
A17A1J3-23	SPARE (FSK RX +)	J8-20	----
A17A1J3-24	ID1	----	J8-8
A17A1J3-25	SPARE (FSK RX -)	J8-21	----
A17A1J3-26	ID4	----	J8-9
A17A1J3-27	BAUD 3	----	J8-22
A17A1J3-28	BAUD 1	----	J8-10
A17A1J3-29	BAUD 0	----	J8-23
A17A1J3-30	BAUD 2	----	J8-11

3. FUNCTIONAL DESCRIPTION

3.1 Control and Data Transfer

The A17A1 assembly appears as an electrical extension of the address/data bus of the microprocessor on the A14 assembly. This bus is buffered by tristate bidirectional buffer U5 and high-order address and control inputs buffered by U1. Selection of IC devices on the LCU for data transfer to and from the CPU is done using three-to-eight decoder U3 with high-order address bits. Interface signals RD, WR, and S1 from the A14 assembly determine the direction of data flow after addresses have been loaded into latch U6 by ALE, the address latch enable.

The information stored in the EPROM is part of the system software and cannot be changed by the customer.

3.2 Serial Data Transmission/Reception

Upon power up reset, the controlling CPU (A14U24) detects the presence of the LCU option, and initializes all IC devices on the A17A1 assembly. Using the software in the LCU EPROM, the CPU conditions the DUART U8 to receive incoming signals according to user-selected options. When response to a distant RCU is required by this RF-1310 LCU, the transmit interface is enabled. Appropriate parallel data sent via address/data bus AD0-AD7 from the CPU is converted to serial data by DUART U8. Completed reception/transmission of message characters by U8 is signaled to the CPU by interrupt line RST 5.5, generated by U8 and U12. The baud rate generation is done internally to U8 by using the 3.6864 MHz crystal Y1.

3.3 Serial Interfaces

The A17A1 assembly provides all standard data communication interfaces. Each is individually selectable. For RS-232C/MIL-STD-188C interfaces, transceiver chip U14 is used. The main RS-422/RS-485 interface utilizes transmitter U13 and receiver U9. In addition, for future expansion, a second RS-422/RS-485 interface channel is provided using the remaining portions of U13 and U9. All RS-422/RS-485 interface lines have full transient suppresison protection.

3.4 Parallel Data I/O

Parallel data input is accomplished through data buffers U10 and U11. Buffer U11 reads DIP switch S1 determining the remote's identification number. Buffer U10 reads rotary switch S2 which determines the operating baud rate. A portion of switch S3 is read by U10 and is reserved for future options.

DUART U8 provides an additional 8 spare input and output lines for modem use and future options. Three sections of switch S3 are read into these lines for future use. Chip selects from U3, as well as appropriate RD and WR signals, manage the control of these I/O devices.

3.5 Modem I/O

The A17A1 assembly provides all necessary control lines neded to utilize the optional A17A2 FSK Modem assembly. This option provides full FSK operation and is interfaced to A17A1 through connector A17A1J4. For the modem's functional description, refer to the A17A2 Modem Assembly section. (If purchased with the exciter.)

3.6 BITE (Self-Test)

When installed, the A17A1 hardware is tested along with all other RF-1310 functions during execution of the built-in-test (BITE) feature of the exciter. These tests are performed if the exciter is in either Local or Remote operation. Specifically, three LCU tests are made: a test of DUART U8 function, a checksum test to ensure

correct EPROM function, and a test of parallel I/O and RS-422 receivers. The corresponding BITE fault codes are:

- Fault 01 - EPROM (U7) fault
- Fault 02 - Communications (DUART U8) fault
- Fault 03 - Interface (DUART U8, U14) fault

3.7 Dc Distribution

The A17A1 assembly receives three supply voltages from the A14 assembly. The + 8.5 volt input is regulated by VR1 to yield the + 5 V logic supply. The + 15 V and -15 V inputs are regulated down to 6.8 V, for use by the driver portion of U14, using Zener diodes CR1 and CR2.

4. MAINTENANCE

4.1 Setup

4.1.1 Identification Number

For use in a remote control system consisting of many RF-1310s or other compatible units, each LCU must be setup to have a unique identification number. This number, an eight-bit binary code, is set up on DIP switch S1 and allows 255 individual unit codes (1 to 255) according to table 2.

Table 2. Identification Number Setup

Switch	Binary Weight
S1-1	128 (highest order bit)
S1-2	64
S1-3	32
S1-4	16
S1-5	8
S1-6	4
S1-7	2
S1-8	1 (lowest order bit)

0 = switch closed
1 = switch open

For example, leaving only S1-4 and S1-7 open and all other S1 switches closed forms the binary identification number 00010010, which is 16 + 2 = 18 (in decimal format).

4.1.2 Baud Rate Selection

The RF-1310 LCU allows any of fifteen popular baud rates to be used in communication through the DUART U8. The baud rate is selectable by setting rotary switch S2 to the position indicated in table 3. Users should change the baud rate switch only when the RF-1310 is turned off, so that the A17A1 assembly will be set up correctly when power is again applied.

Table 3. Baud Rate Setup

S2 Position	Baud Rate
0	50
1	75
2	110
3	134.5
4	150
5	300
6	600
7	1200
8	1800
9	2000
A	2400
B	Not Used
C	4800
D	7200
E	9600
F	19200

4.1.3 Signaling Interface Selection

The standard A17A1 assembly allows any of three signaling interfaces to be used. If the optional A17A2 assembly is included, a fourth FSK modem interface may be used. Typically, the desired interface will be preset at the factory. If a different interface is required, configure the jumpers as shown in table 4. Use only the jumpers as specified and remove all others.

4.2 Troubleshooting

There are three test points located on A17A1 Assembly. Table 5, used together with the schematic diagram and the component location drawing, should help in locating most A17A1 assembly problems.

Table 4. Jumper Selection of Interface

Selected Interface	Jumper Configuration
RS-232C Interface	
RS-232C TX	E11 - E13 E3 - E14
RS-232C RX	E4 - E6
MIL-188C Interface	
MIL-188C TX	E11 - E13 E14 - E15
MIL-188C RX	E4 - E7
RS-422485 Interface	
RS-422/485 RX & TX	E4 - E5
Optional FSK Modem	
FSK TX	E12 - E13
FSK RX	E4 - E8

Table 5. Test Point Indications

Test Point	Indicates
TP1	A17A1 address/data buffer enable A17A1U5
TP2	Chip enable for LCU EPROM A17A1U7
TP3	RST 5.5 interrupt from A17A1U8

Data transfer to or from the microprocessor on Control Board Assembly A14 takes place when a logic low is seen at TP1. A simultaneous low at TP2 indicates the exchange is that of program steps from the EPROM containing software to manage the A17A1 assembly. When a controlling unit is operating, its communication with the RF-1310 will result in intermittent active high pulses on the interrupt line (TP3), again regardless of the local or remote operation of the exciter.

Absence of activity on points TP1 - TP3 indicate a failure in the connection of A17A1 assembly to Control Board Assembly A14. If the A17A1 assembly is not properly installed, an operator placing the function switch to REMOTE will note that the front panel display blanks, then reads NO REMOTE. After 4 seconds, the displays will read the values last used in local operation, but the front panel will be locked out. The operator must return to NORM using the function switch. If activity is seen on TP1 - TP3 and the exciter can be placed into remote operation (but no remote control/readback seems to be functioning), the fault lies in the setup of the A17A1 assembly (baud rate or interface jumpering), or in the controller or link between controller and RF-1310.

If activity is seen on all three test points during operation with a controller, but the RF-1310 cannot be remotely commanded, check that the LCU identification number is properly selected. Also check that this LCU is the one being commanded from the controller. As an aid to checking desired baud rate and identification

number setups, apply power to the exciter after the corresponding switches S1 and S2 have been set on the A17A1 assembly. With the exciter selected to remote transmit operation, depress and hold in the front panel ENTER button. Within ten seconds, the lefthand display of the RF-1310 will show the identification number and baud rate selected on A17S1 and A17S2 in a format such as REMOTE # 04 2400 BPS. This is for LCU identification number 4, and a communication rate of 2400 bits per second (baud).

5. PARTS LIST, COMPONENT LOCATIONS, AND SCHEMATIC DIAGRAM

Table 6 lists the parts in Remote Control Assembly A17A1. Figure 1 shows the components in the A17A1 assembly, and figure 2 is the schematic diagram for the A17A1 assembly.

Table 6. Remote Control Assembly A17A1 Parts List (10121-6250 Rev. D)

Ref. Desig.	Part Number	Description
C1 – C5	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C6	C26-0050-109	CAP 1.0UF 20% 50V TANT
C7	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C9	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C10	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C11	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C12	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C13	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C14	C12-0001-009	CAP 4.7PF 10% 25V CER
C15 – C18	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C19	C12-0001-009	CAP 4.7PF 10% 25V CER
C20	M39014/02-1310V	CAP .1UF 10% 100V CER-R
CR1, CR2	1N5235B	DIODE 6.8V 5% .5W ZENER
CR3	D50-0005-003	TRANSORB 6.63 V 1500W BI
CR4	D50-0005-003	TRANSORB 6.63 V 1500W BI
CR5	D50-0005-003	TRANSORB 6.63 V 1500W BI
CR6	D50-0005-003	TRANSORB 6.63 V 1500W BI
CR7	D50-0005-003	TRANSORB 6.63 V 1500W BI
CR8	D50-0005-003	TRANSORB 6.63 V 1500W BI
CR9	D50-0005-003	TRANSORB 6.63 V 1500W BI
CR10	D50-0005-003	TRANSORB 6.63 V 1500W BI
CR11	D50-0005-003	TRANSORB 6.63 V 1500W BI
CR12	D50-0005-003	TRANSORB 6.63 V 1500W BI
CR13	D50-0005-003	TRANSORB 6.63 V 1500W BI
CR14	D50-0005-003	TRANSORB 6.63 V 1500W BI
J1, J2	J46-0013-020	HDR 20 PIN 0.100" DR SHRD
J3	J46-0031-030	HDR 30 PIN 0.100" RT ANG
J4	J46-0029-024	BD MT DBL ROW RECEPTACLE
R1	R50-0010-103	RES 10K 2% 10SIP 9RES
R2	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R3	R65-0004-100	RES 10 5% 1/2W CAR FILM
R4	R65-0004-100	RES 10 5% 1/2W CAR FILM
R5	R50-0010-103	RES 10K 2% 10SIP 9RES
R6	R50-0010-103	RES 10K 2% 10SIP 9RES

Table 6. Remote Control Assembly A17A1 Parts List (10121-6250 Rev. D) (Cont.)

Ref. Desig.	Part Number	Description
R7	R50-0010-103	RES 10K 2% 10SIP 9RES
R8	R65-0004-102	RES 1.0K 5% 1/2W CAR FILM
R9	R65-0004-102	RES 1.0K 5% 1/2W CAR FILM
R10	R65-0004-100	RES 10 5% 1/2W CAR FILM
R11	R65-0004-100	RES 10 5% 1/2W CAR FILM
R12	R65-0004-331	RES 330 5% 1/2W CAR FILM
R13	R65-0004-331	RES 330 5% 1/2W CAR FILM
R14	R65-0004-102	RES 1.0K 5% 1/2W CAR FILM
R15	R65-0004-102	RES 1.0K 5% 1/2W CAR FILM
R16	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R17	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R18	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R19	R65-0003-103	RES 10K 5% 1/4W CAR FILM
S1	S50-0001-008	SW SPST 8SEC .1A SLD DIP
S2	S27-0012-002	SW 1P 16POS BCD ROT DIP
S3	S50-0001-008	SW SPST 8SEC .1A SLD DIP
TP1	J-0071	TP PWB BRN TOP ACCS .080"
TP2	J-0066	TP PWB RED TOP ACCS .080"
TP3	J-0069	TP PWB ORN TOP ACCS .080"
U1	I15-0000-244	IC 74HC244 PLASTIC CMOS
U2	I15-0000-008	IC 74HC08 PLASTIC CMOS
U3	I15-0000-138	IC 74HC138 PLASTIC CMOS
U4	I15-0000-032	IC 74HC32 PLASTIC CMOS
U5	I05-0000-245	IC 74LS245 PLASTIC TTL
U6	I15-0000-373	IC 74HC373 PLASTIC CMOS
U7	10121-8811	KIT SOFTWARE REMOTE
U8	I61-0004-001	IC DUART
U9	I17-0008-001	IC 75173 LINE RCVR X4 PLA
U10	I15-0000-244	IC 74HC244 PLASTIC CMOS
U11	I15-0000-244	IC 74HC244 PLASTIC CMOS
U12	I15-0000-004	IC 74HC04 PLASTIC CMOS
U13	I16-0012-000	IC 75174 LINE DRVR PLA
U14	I17-0007-001	IC 145406 DRVR/RCVR PLA
U15	I15-0000-000	IC 74HC00 PLASTIC CMOS
VR1	I11-0001-001	IC VR 7805 +5V 1.5A 4%
XU7	J77-0008-006	SKT IC MACH 28 PIN
Y1	Y15-0004-937	XTAL 3.6864 MHZ

NOTE

The part number for U7 is 10121-8XXX-X, where XXX-X is the four character software kit code found on the PROM label. For example, if the code is 501C, the part number for the programmed PROM is 10121-8501-C.

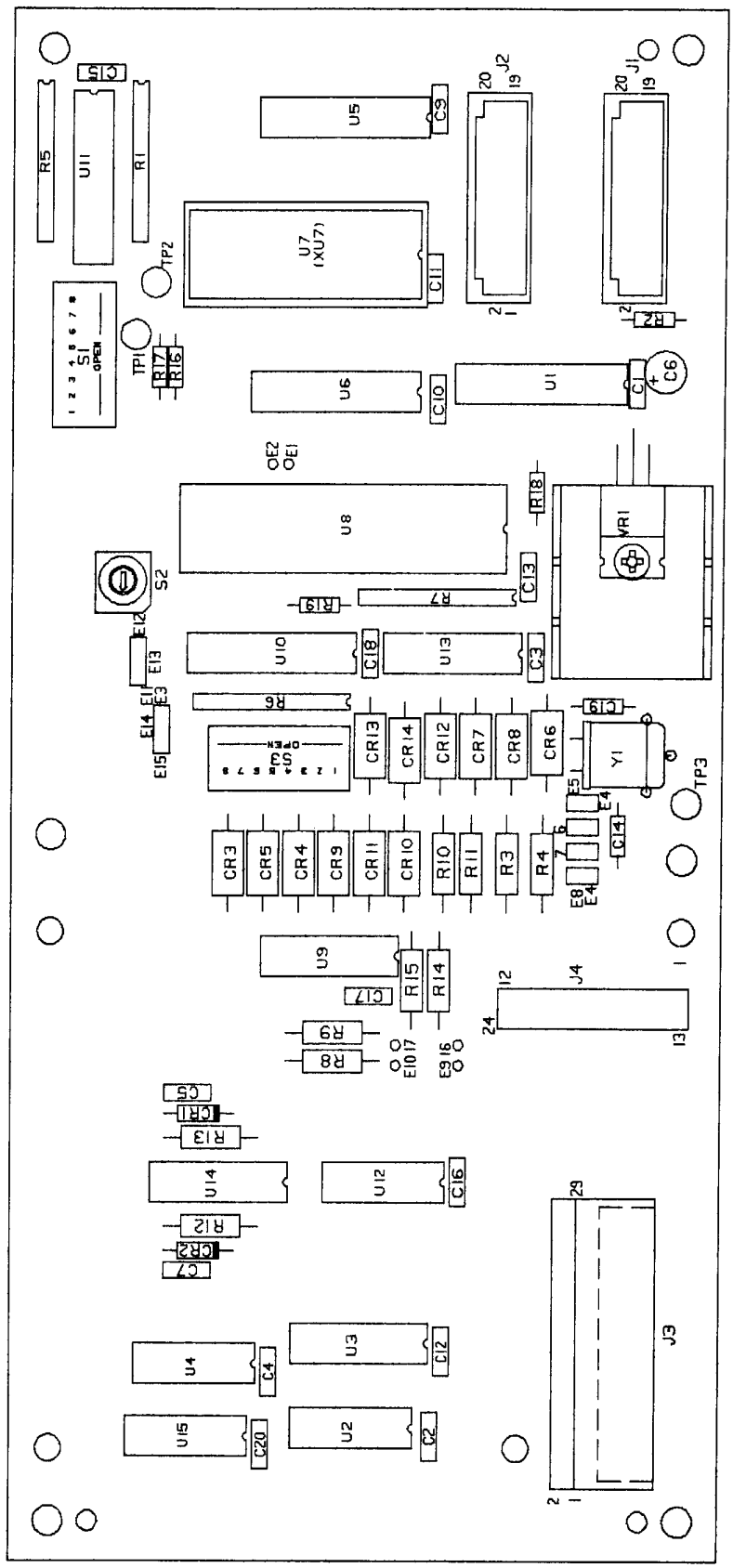
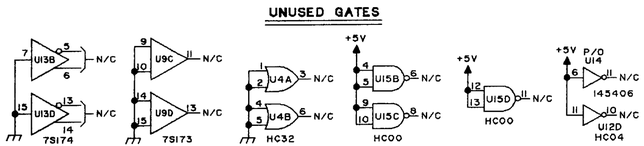


Figure 1. Remote Control Assembly A17A1 Component Location Diagram (10121-6250 Rev. D)

NOTE: UNLESS OTHERWISE SPECIFIED:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR A COMPLETE DESIGNATION, PREFIX WITH UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.
2. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, ±5%.
3. ALL CAPACITOR VALUES ARE IN MICROFARADS.
4. VENDOR PART NO. CALLOUTS ARE FOR REFERENCE ONLY. COMPONENTS ARE SUPPLIED PER PART NO. IN PARTS LIST.



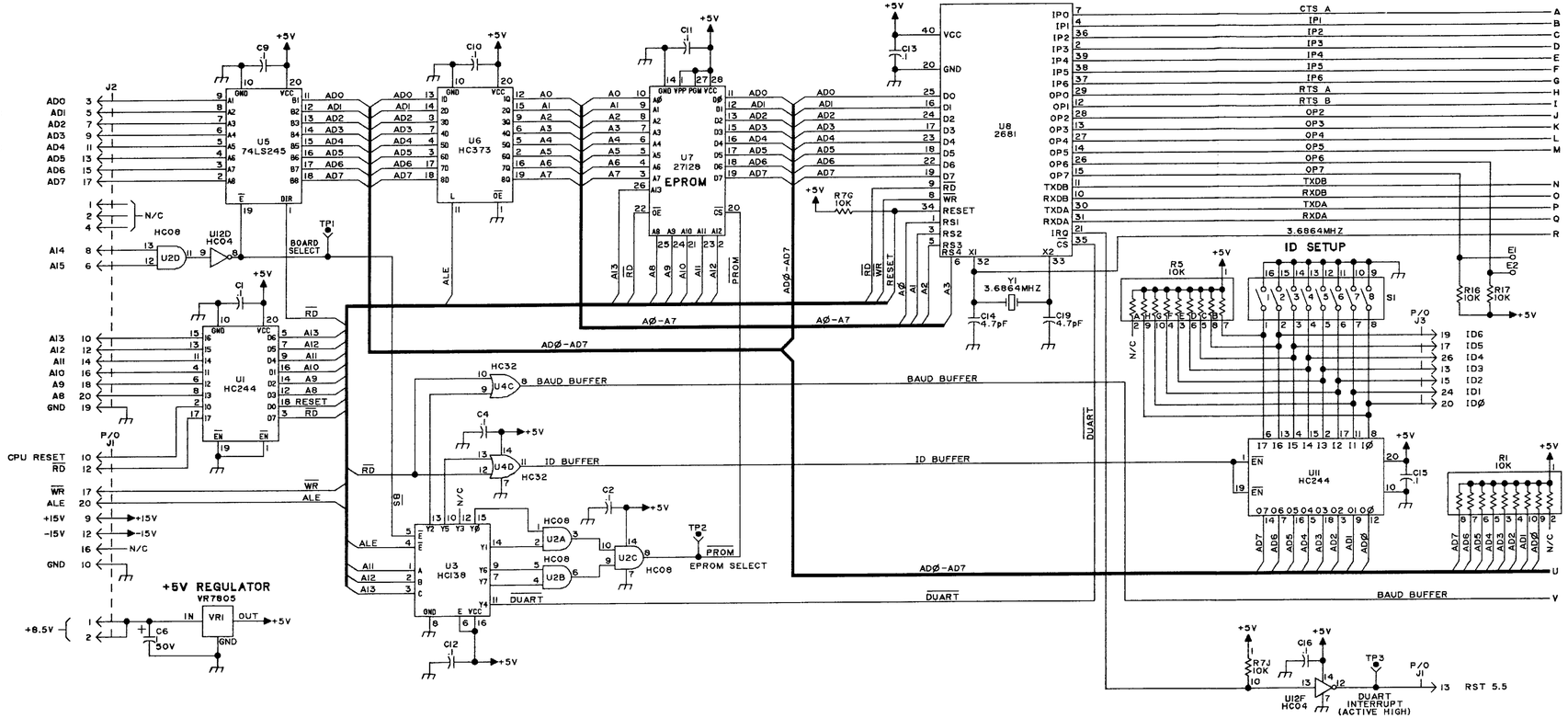


Figure 2. Remote Control Assembly A17A1 Schematic Diagram (10121-6251 Rev. D) (Sheet 1 of 2)

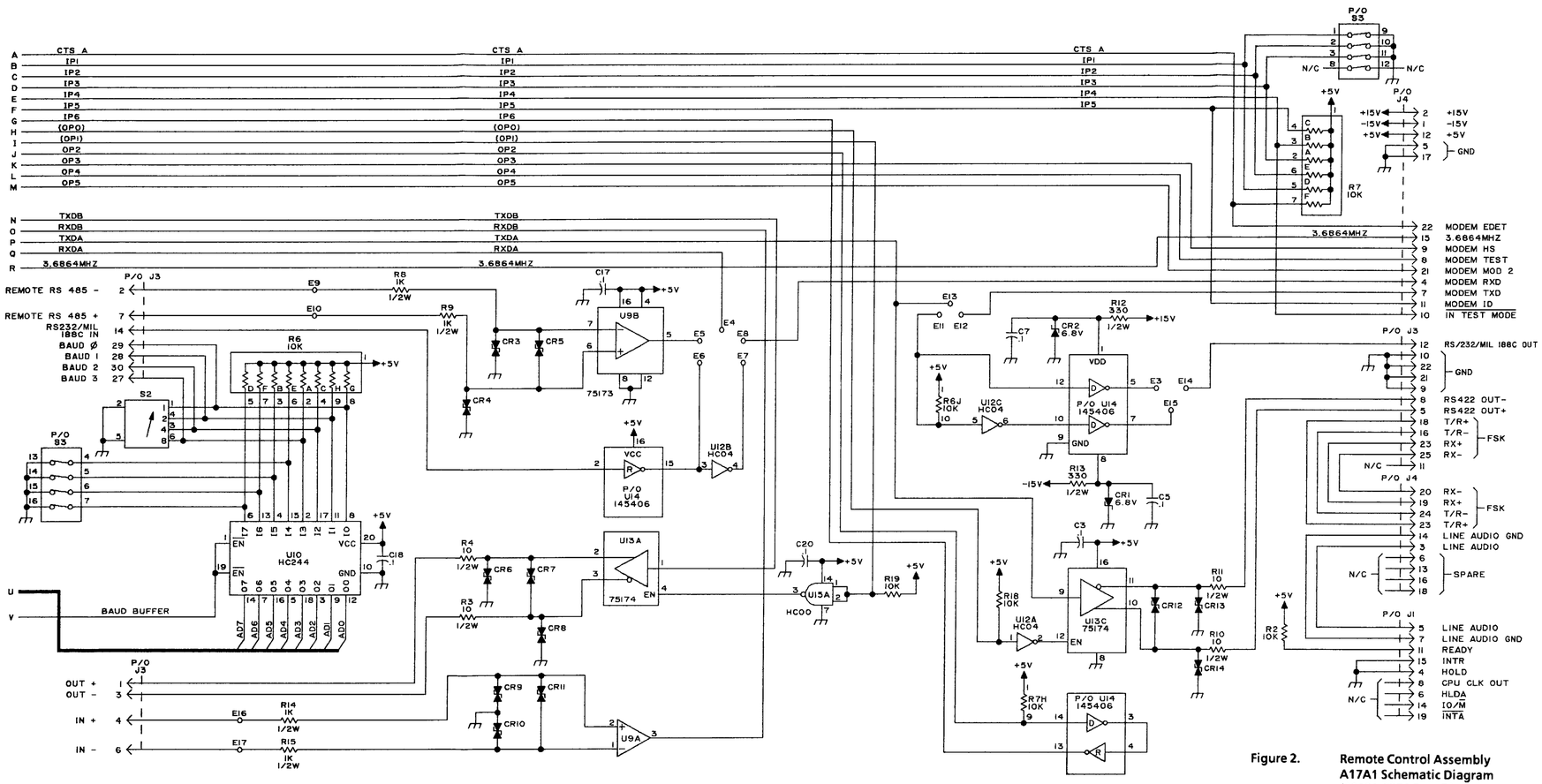
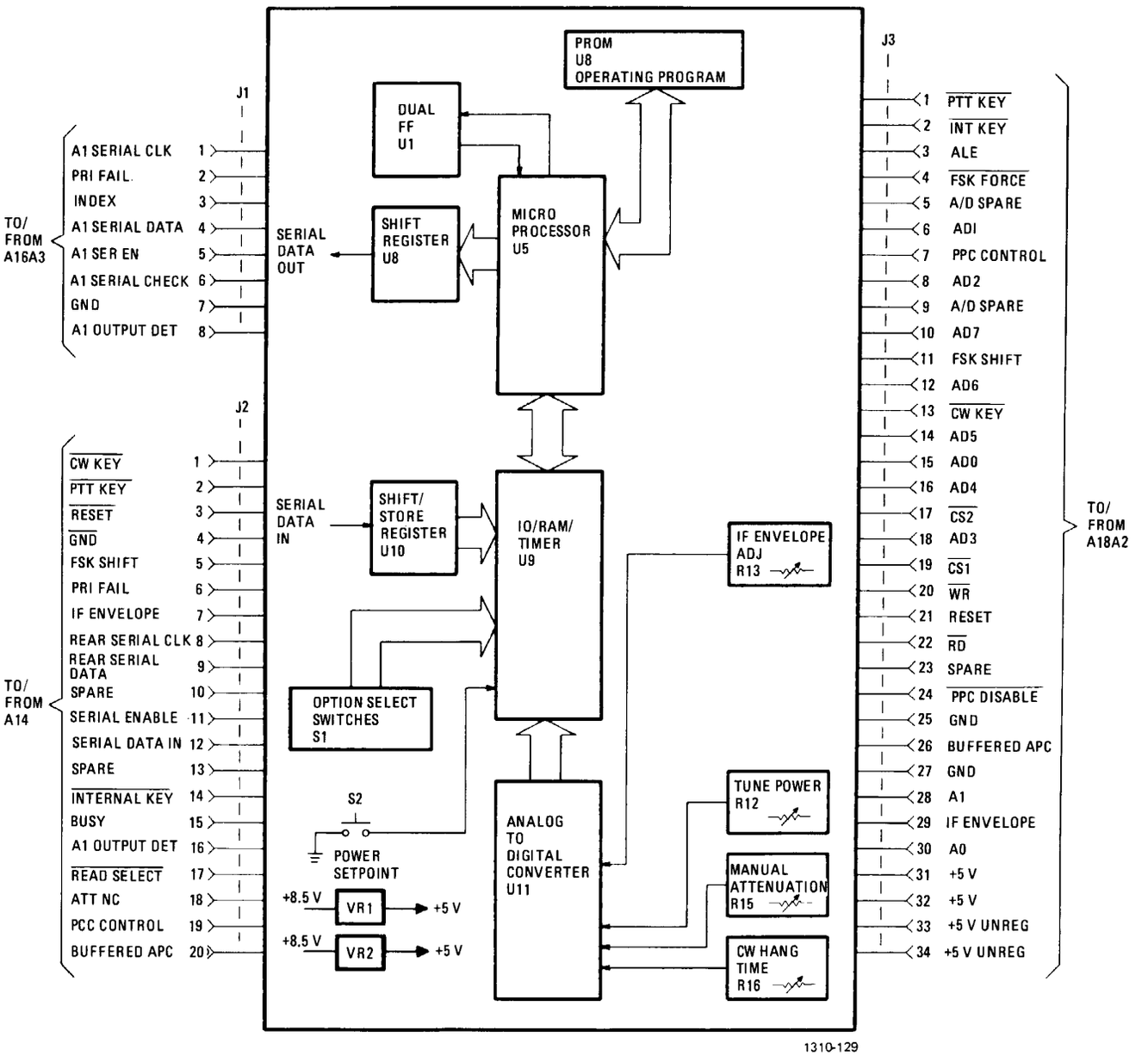


Figure 2. Remote Control Assembly A17A1 Schematic Diagram (10121-6251 Rev. D) (Sheet 2 of 2)

A17A2
REMOTE FSK MODEM ASSEMBLY

THIS SECTION IS INCLUDED ONLY IN REMOTE FSK MODEM VERSIONS OF THE RF-1310 EXCITER.

A18A1
SYSTEM INTERFACE PROCESSOR BOARD ASSEMBLY



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SYSTEM INTERFACE ASSY A18A1

1. GENERAL DESCRIPTION

System Interface Assembly A18A1 is a self-contained processor unit with its own 8085A processor, RAM, and EPROM. The A18A1 and A18A2 assemblies are shown in figure 1. Its primary functions are to accept PA control commands from the A14 assembly, translate these commands to the A18A2 I/O assembly, and provide readbacks from the A18A2 I/O assembly. The A18A1 assembly contains its own CPU, an 16K byte EPROM, 2K bytes of RAM memory, serial-to-parallel conversion circuits, parallel-to-serial conversion circuits, analog-to-digital conversion abilities, and a multiport I/O. Note that with the exception of serial communications with the A14 assembly, this processor board runs independently using software stored in its own EPROM. It performs its own self testing (BITE) when requested to by the exciter's BITE procedure.

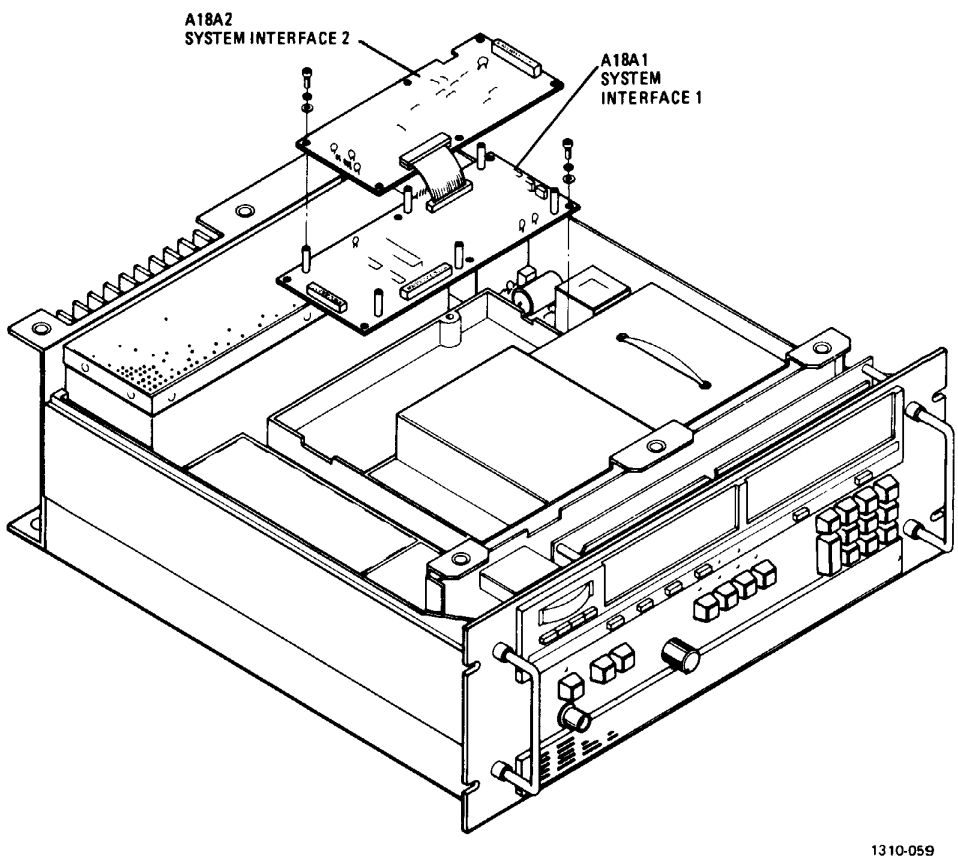

Figure 1. A18 Assembly Location

2. INTERFACE CONNECTIONS

System Interface Assembly A18A1 interface connections are shown in table 1.

Table 1. RF-1310 System Interface Assembly A18A1 Interface Lines

Connector	Function	To	From
A18A1J1-1	A1 SERIAL CLOCK	A16A3J3-1	----------
A18A1J1-2	PRIMARY FAIL	----------	A16A3J3-2
A18A1J1-3	INDEX	----------	----------
A18A1J1-4	A1 SERIAL DATA	A16A3J3-4	----------
A18A1J1-5	A1 SERIAL ENABLE	A16A3J3-5	----------
A18A1J1-6	A1 SERIAL CHECK	----------	A16A3J3-6
A18A1J1-7	GROUND	A16A3J3-7	A16A3J3-8
A18A1J1-8	A1 OUTPUT DETECT	----------	A16A3J3-8
A18A1J2-1	$\overline{\text{CW KEY}}$	----------	A14J4-1
A18A1J2-2	$\overline{\text{PTT KEY}}$	----------	A14J4-2
A18A1J2-3	$\overline{\text{RESET}}$	----------	A14J4-3
A18A1J2-4	GROUND	----------	A14J4-4
A18A1J2-5	FSK SHIFT	A14J4-5	----------
A18A1J2-6	PRIMARY FAIL	A14J4-6	----------
A18A1J2-7	IF ENVELOPE	----------	A14J4-7
A18A1J2-8	REAR SERIAL CLOCK	----------	A14J4-8
A18A1J2-9	REAR SERIAL DATA	----------	A14J4-9
A18A1J2-10	SPARE	----------	----------
A18A1J2-11	SERIAL ENABLE	----------	A14J4-11
A18A1J2-12	SERIAL DATA IN	A14J4-12	----------
A18A1J2-13	SPARE	----------	----------
A18A1J2-14	$\overline{\text{INTERNAL KEY}}$	----------	A14J4-14
A18A1J2-15	BUSY	A14J4-15	----------
A18A1J2-16	A1 OUTPUT DETECT	A14J4-16	----------
A18A1J2-17	$\overline{\text{READ SELECT}}$	----------	A14J4-17
A18A1J2-18	ATTNC	A14J4-18	----------
A18A1J2-19	PPC CONTROL	A14J4-19	----------
A18A1J2-20	BUFFERED APC	A14J4-20	----------
A18A1J3-1	$\overline{\text{PTT KEY}}$	A18A2P1-1	----------
A18A1J3-2	$\overline{\text{INTERNAL KEY}}$	A18A2P1-2	----------
A18A1J3-3	ALE	A18A2P1-3	----------
A18A1J3-4	$\overline{\text{FSK FORCE}}$	A18A2P1-4	----------
A18A1J3-5	A/D SPARE	A18A2P1-5	----------
A18A1J3-6	AD1	A18A2P1-6	BIDIRECTIONAL

Table 1. RF-1310 System Interface Assembly A18A1 Interface Lines (Cont.)

Connector	Function	To	From
A18A1J3-7	PPC CONTROL	----------	A18A2P1-7
A18A1J3-8	AD2	A18A2P1-8	BIDIRECTIONAL
A18A1J3-9	A/D SPARE	A18A2P1-9	----------
A18A1J3-10	AD7	A18A2P1-10	BIDIRECTIONAL
A18A1J3-11	FSK SHIFT	----------	A18A2P1-11
A18A1J3-12	AD6	A18A2P1-12	BIDIRECTIONAL
A18A1J3-13	$\overline{\text{CW KEY}}$	A18A2P1-13	----------
A18A1J3-14	AD5	A18A2P1-14	BIDIRECTIONAL
A18A1J3-15	AD0	A18A2P1-15	BIDIRECTIONAL
A18A1J3-16	AD4	A18A2P1-16	BIDIRECTIONAL
A18A1J3-17	$\overline{\text{CS2}}$	A18A2P1-17	----------
A18A1J3-18	AD3	A18A2P1-18	BIDIRECTIONAL
A18A1J3-19	$\overline{\text{CS1}}$	A18A2P1-19	----------
A18A1J3-20	$\overline{\text{WR}}$	A18A2P1-20	----------
A18A1J3-21	RESET	A18A2P1-21	----------
A18A1J3-22	$\overline{\text{RD}}$	A18A2P1-22	----------
A18A1J3-23	BUFFERED APC #2	----------	A18A2P1-26
A18A1J3-24	$\overline{\text{PPC DISABLE}}$	A18A2P1-24	----------
A18A1J3-25	GROUND	A18A2P1-25	----------
A18A1J3-26	BUFFERED APC #1	----------	A18A2P1-26
A18A1J3-27	GROUND	A18A2P1-27	----------
A18A1J3-28	A1	A18A2P1-28	----------
A18A1J3-29	IF ENVELOPE	----------	----------
A18A1J3-30	A0	A18A2P1-30	----------
A18A1J3-31	+ 5 V	A18A2P1-31	----------
A18A1J3-32	+ 5 V	A18A2P1-32	----------
A18A1J3-33	+ 5 V UNREGULATED	----------	A18A2P1-33
A18A1J3-34	+ 5 V UNREGULATED	----------	A18A2P1-34

3. FUNCTIONAL DESCRIPTION

Figure 2 is a block diagram of the A18A1 assembly and figure 4 is the schematic diagram.

3.1 CPU and Clock Generation

The 8085A microprocessor executes the application program stored in EPROM U8. The CPU operates off the 6.0 MHz crystal Y1, internally divides this frequency to 3.0 MHz and outputs it on pin 37. The 3.0 MHz is fed to U9 where it is internally divided down to 1 kHz, the frequency of the real time clock, which returns to the processor as the RST 7.5 input. The 3.0 MHz is also fed to U2 and is divided by four to achieve 750 kHz, the

operating frequency of the A/D converter U11. The five high order address bits of U5 (A11, A12, A13, A14, and A15) are inputs to PAL U4. U4 produces active low chip selects for the peripheral circuits on the A18 assembly. The remaining high address bits (A8 through A12) are used to address the EPROM U8 and RAM U12. The multiplexed low address/data bus of U5 is input to address latch U7, serial out register U6, EPROM U8, I/O memory chip U9, RAM U12 and the A18A2 assembly via J3. The low address side of U7 provides the addressing for U8, A/D converter U11, and RAM U12. The microprocessor is reset simultaneously with the U24 processor on Control Board Assembly A14 any time a RESET is initiated on the A14 assembly. Dual flip-flop U1 and NOR gate U3D provide communications control between the system interface board and the control board. Resistor pack R5 provides the pull-up termination for the low address/data bus. The active high interrupt lines of the CPU are assigned as follows:

- RST 5.5 and RST 6.5 are used for communications control between the assemblies
- RST 7.5 is used for the real time clock

3.2 Memory

The firmware program to run the system interface assembly is independent of that used on the A14 assembly and is stored in its own EPROM U8. A chip select from U4 enables the EPROM. Terminals E2 and E3 are reserved for future EPROM expansion.

The information stored in U8 is part of the RF-1310 system interface software and cannot be altered by the customer.

CAUTION

Do not remove the opaque protective shield on the EPROMs. EPROMs are ultraviolet erasable over extended periods of exposure to fluorescent light or sunlight. Extended exposure can erase the memory information.

There are 2K bytes of RAM provided by device U12 for the 8085 processor. Additionally there are 256 bytes of RAM in I/O timer device U9. U9 is selectable as either a memory device, or an I/O device depending on the status of its control line IO/M pin 7. Data is accessed when it is a memory device by using the RD and WR lines in conjunction with the low address/data bus. Unlike the RAM on the control assembly, the memory devices on the system interface assembly do not have battery backed storage capabilities.

3.3 Serial Communications

System Interface Assembly A18A1 communicates with Control Board Assembly A14 by serial data transmissions. Data is transferred serially, eight bits at a time. Varying numbers of eight bit groups (bytes) are needed to properly relay messages back and forth. Data is transmitted in one direction at a time (simplex). While data is being relayed, the receiving assembly is inhibited from further transmission activity until all bytes are received. These messages are formatted in a structured manner and may consist of command or readback information, message start and finish flags, total number of bytes in message count, or message data integrity codes (checksums).

3.3.1 Serial Reception Circuit

The serial reception circuit receives data from the control board as rear serial data and is input to the shift/store register U10. It is clocked into U10 by the rear serial clock, and since the READ SELECT line from the control board is being held high by the A14 Assembly CPU, this clock only affects U10. A serial enable is then

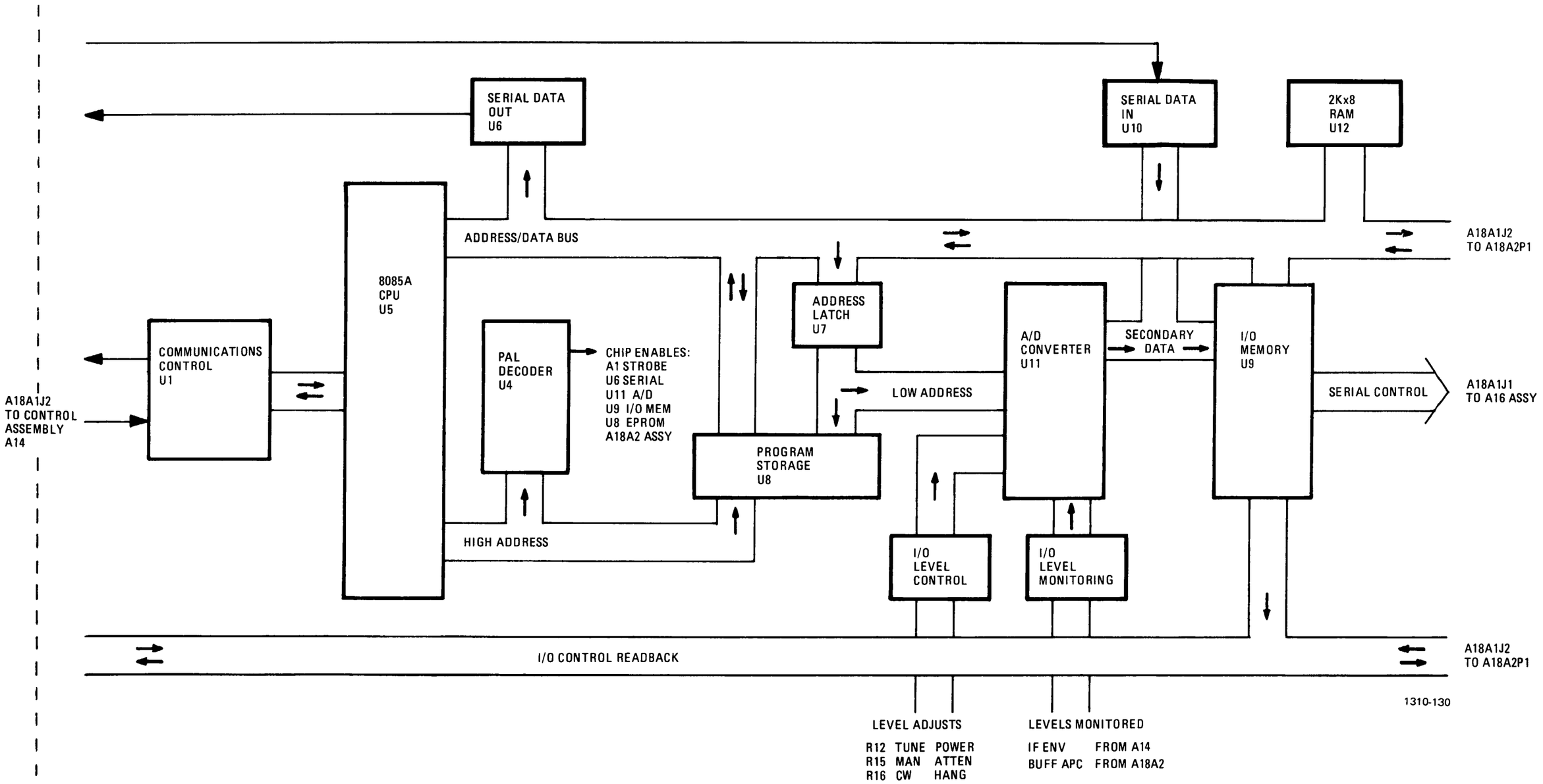

Figure 2. System Interface Assembly A18A1 Block Diagram

sent to the control board and two things happen. The serial data inputted to U10 is strobed into its output registers, and the clock input to flip-flop U1-11 pulses high, forcing U1-9 output high. This is the RST 6.5 input to the CPU, signalling the processor that a byte is being received. This signal also goes back to the control board as the line labeled BUSY. This signals the control board processor that the system interface is processing the received byte. When the system interface has accepted this byte, the CPU pulses its SOD line. This pulse clears U1, which clears the BUSY line to signal the control board that all reception is complete and the process can be repeated. This will continue until all the bytes of the received message have been interpreted. The data in U10 is read in to U9. The data bus connecting U10 to U9 is shared with A/D U11. Pin 39 of U9 provides the output enable control for U10 and U11 to control this data bus.

3.3.2 Serial Transmission Circuit

Data is transmitted from the A18 assembly to the A14 assembly in the following manner. The byte to be transmitted is put on the data bus (AD0 through AD7). Shift register U6 is enabled by a pulse sent from U4, via U3. I/O device U9 sets the attention line (ATTNC) to Control Board Assembly A14, indicating a message is ready to be sent. The control board in turn lowers the READ SELECT line to the system interface assembly. This READ SELECT line is gated through U3 to enable the rear serial clock input to register U6. The data is shifted out of U6 to the control board. When the control board receives this byte, it raises the READ SELECT line to remove the clock from U6 and force the Q8 output of U1-5 high. This tells the CPU that the control board has received the byte. The ATTNC line is forced low and a pulse is sent on the SOD line to clear the RST 5.5 line. This enables the transmission process to be repeated.

3.4 Parallel I/O

Programmable I/O timer U9 provides a variety of input/output control and monitoring on System Interface Assembly A18A1. This device has three I/O ports. Two are used as inputs and one as an output. Table 2 lists the three port assignments.

Table 2. 8155A Port Dedication

Port	Function
PA Input	Secondary data bus receives serial data or A/D conversion data.
PB Input	PA setup switch and pushbutton S2 (See paragraph 4, TGC Select Switch), internal key, and A1 serial check.
PC Output	A1 serial control lines, FSK force (used during BITE), ATTNC, PPC disable, and secondary data bus control.

3.5 Analog Inputs

A/D converter U11 handles the analog-to-digital conversions on the system interface assembly. Four of the analog inputs are from potentiometers R12, R13, R15, and R16 and set various PA system operational parameters. (See paragraph 6.1, Alignment.) One input is reserved for system interface BITE, while one additional line monitors the average power control (APC) level coming from the A18A2 assembly. One line monitors the IF sample voltage. A/D U11 operates off its own reference voltage, ensuring a high degree of accuracy in its measurements.

4. TRANSMITTER GAIN CONTROL (TGC) SELECT SWITCH

DIP switch S1 along with pushbutton S2 are used on the system interface processor board to select various TGC operating parameters for the RF-1310 Exciter and transmitting system. Table 3 lists the S1 switch assignments.

Table 3. Options Switches

Switch Function	Description	
S1-1	TGC Learn Enable	Determines if full power attenuation value used is the one stored in the A14 RAM or if a new one is learned and stored at the end of a PA tune cycle. **Closed** = Learn Disable - attenuation value is the one stored in A14 RAM **Open** = Learn - a new value of attenuation needed for full power out will be learned and stored in A14 RAM
S1-2	Attenuation Control	Determines if attenuator control values are a function of what is read from potentiometer R15 or if normal TGC operation is in effect. **Closed** = Attenuation Manual - control value is read directly from R15 and TGC is disabled. This value may be stored in the A14 RAM as the learned value for a particular frequency by checking that S1-1 is closed and depressing S2. **Open** = Attenuation Auto - normal attenuation control under TGC.
S1-3	Coupler Control	Tells exciter to include coupler in tune cycle. **Closed** = no coupler/all couplers **Open** = RF-601 coupler only
S1-4	Signal Generator	Allows exciter to be operated as a signal generator. In this mode, attenuation is set to front panel value. Exciter is ready when placed in operate and exciter must be keyed for output. PA is disabled from keying. **Closed** = exciter is in normal operating mode **Open** = exciter is in generator mode

5. SYSTEM INTERFACE BITE

The self-testing procedure performed on System Interface Assembly A18A1 is done in a similar manner to that of Control Board Assembly A14. The tests are done sequentially in order of importance. If a test fails, the test will stop and the appropriate error code will be displayed on the front panel. The order in which these tests are performed is as follows:

- Communication Test
- EPROM Test
- RAM Test
- I/O Test
- A1 Output Amp Communication Test
- A/D Converter Test

A failure in any of these tests will generate the appropriate error code listed in table 4. This error code is sent to Control Board Assembly A14. The error code will be displayed on the front panel of the exciter along with the System Interface Assembly (A18A1) number. If there were no errors in any of the system interface assembly tests, nothing would be displayed on the front panel, and the control assembly BITE procedure would continue.

Table 4. System Interface BITE Codes

Code	Fault
01	Serial Communications
02	ROM Failure
03	RAM Failure
04	I/O Failure
05	Output Amp Communication
06	A-to-D EOC Failure
07	A-to-D Conversion Failure

5.1 Communications

This test ensures proper serial communication between System Interface Assembly A18A1 and the Control Board Assembly A14. The A14 assembly sends a checksum byte code as part of the BITE start message. This code is verified by System Interface Assembly A18A1 and sent back to the control board where it is verified. Any discrepancies will cause the fault code to be displayed.

5.2 ROM Test

The ROM test is performed next. EPROM U8 contains all the firmware used to control the system interface and is tested to ensure that the information it contains is correct. This information is factory programmed; if an error is determined in this test, preliminary operational checks should be made. If no problems are found, the device should be replaced by ordering a new one from the factory.

5.3 RAM Test

After the ROM test, the read/write capabilities of the 2K bytes of RAM memory available in RAM chip U12 and in the 8155 chip U9 are checked. If any faults are found, the proper fault code will be displayed.

5.4 I/O Test

The ability of the microprocessor to read and write to the A18A2 assembly is tested next. A bit pattern is written to a latch on the A18A2 assembly. The data in the latch is then read and compared to the original bit pattern. A fault code is displayed if the two patterns are not the same.

5.5 A1 Serial Test

Following the I/O test, the ability of the system interface assembly to serially communicate with output amplifier A1 is tested. This serial communications is necessary to control the output attenuators. The test is performed by toggling the lowest bit in the serial attenuator command stream from high to low and checking to see that the A1 serial check bit changes. Any problem will display the proper fault code.

5.6 A to D Test

A/D converter U11 is tested after all other A18 assembly tests have been passed. The microprocessor reads the digital representation of the fixed voltage present at U11-1. A failure to generate the proper analog-to-digital conversion will be indicated by the appropriate fault code.

6. MAINTENANCE

6.1 Alignment

There are four potentiometers on the A18A1 assembly that require adjustments. They are primarily used in TGC operations. Table 5 lists the potentiometers and brief description of their functions. Alignment depends on the particular application and is covered in the appropriate system manual.

Table 5. A18A1 Assembly Potentiometers

Potentiometer	Description	
R12	Tune Power	Adjusts the amount of exciter drive to the PA during a tune cycle.
R13	IF Envelope	Sets the exciter RF signal level to the normalized value for TGC operation. Normally set = 4.5 Vdc at TP1 while keyed and in CW.
R15	Manual Attenuation	Varies the range of manual output attenuation from 0 to 8 dB. Clockwise = maximum 8 dB Counterclockwise = minimum 0 dB
R16	CW Hang Time	Sets amount of time system key is held after exciter input key is released. Clockwise = 1.25 second delay Counterclockwise = no delay

6.2 Troubleshooting

Most of the circuitry on the system interface assembly is controlled directly or indirectly by the microprocessor. Standard digital troubleshooting methods will isolate most faults to the component level. Circuit areas involved in minor faults can be determined by BITE fault codes. General or major failures are best handled by proceeding, in order, through the checks outlined below.

6.2.1 Communications

The first and most important item to check is the ability of the system interface to communicate with the control board and vice versa. The easiest way to verify communications is to depress the AMP OFF and STBY buttons on the exciter front panel. If the LED above each button lights when the respective button is pressed, the two boards are communicating properly. If this does not happen, then the system interface board must be checked by using the procedures listed below.

6.2.2 CPU

If the microprocessor U5 is running, it can be used to debug several circuits on the A18A1 assembly. However, it must first be determined that the 8085A is running.

The following inputs must be present in order for the device to run.

- U5-1, 2 Crystal inputs - 6.0 MHz
- U5-36 Reset input - HIGH

The A18A2 assembly + 5 volt supply should measure between + 4.75 and + 5.1 volts. Following is a list of CPU outputs that should be present.

- U5-37 Clock out - 3 MHz square wave
- U5-3 Reset out - low
- U5-31 Write - active low pulses
- U5-32 Read - active low pulses
- U5-30 Address latch enable - active high pulses

When the CPU is running and executing the application software, its outputs will only be active a portion of each millisecond. The rest of the time it will be waiting for the real time clock interrupt on pin 7.

6.2.3 Device Selection

PAL decoder U4 aids in the access of peripheral devices through the data bus, by providing active-low chip enable signals corresponding to the high order bits of the CPU. The equations programmed into the PAL (U4) which determine the chip enable selections are given in table 6. During normal operation, the enables can be measured (as logic high) at U3-1, U4-16, U4-17, U6-9, U8-20, U9-8, U11-6, and U12-18.

6.2.4 Memory

Problems in the memory circuitry can be difficult to isolate. If BITE indicates a PROM failure, the fact that BITE even runs indicates that the address and data bus are operating properly and the PROM is being accessed. However, invalid data in device U8 is probably causing this error and it should be replaced.

If a RAM failure is indicated, some checks are in order. Check for high going pulses on the IO/M line U9-7 and on the ALE line U9-11. Also check to see that the memory chips are being enabled by low going pulses on U9-8 and U12-18. Make sure that the RESET line U9-4 is low.

6.2.5 Timing

The timing circuits on the A18A1 assembly are easy to check. Look for the following TTL square wave signals at the noted locations.

- U9-3, U2-3 3.0 MHz
- U5-7 1.0 kHz - output of U9

Table 6. U4 PAL Chip Programmed Select Lines

Device Selected	Control Lines						Function
	IOM	A15	A14	A13	A12	A11	
U8-20	0	0					PROM
U12-18	0	1	0	0			CMOS RAM
U11-6, 22	0	1	0	1	0	0	A/D START *1
U9-8		1	0	1	1	1	8155
U6-9	1	1	0	1	0	1	SER DATA *2
J1-5	1	1	0	1	1	0	A1 STROBE *3
J3-19		1	1	0			CS1
J3-17	1	1	1	1			CS2

Notes: A logic HIGH = 1 and a logic LOW = 0.
*1 This select is qualified externally from the PAL with WR = 0 through W3-9.
*2 This select is qualified externally from the PAL with WR = 0 through U3-11.
*3 This select is qualified externally from the PAL with S1 = 0 through U3-3.

- U11-10 750 kHz - output of U2

6.2.6 Serial Transmission Circuitry

As stated in paragraph 6.2.1, the easiest way to verify interboard communication is to move the front panel switches back and forth between AMP OFF and STBY.

When messages are being sent, high-going pulses of TTL levels should be seen at the following locations:

- U6-3 Serial Data In
- U6-10 and U10-3 Rear Serial Clock
- U10-2 Rear Serial Data
- U5-8 and U5-9 Communications Interrupts
- U6-9 Data Out Load Pulse

In addition, a low-going pulse should be seen on U5-4.

6.2.7 Parallel I/O

Three ports of I/O are used on this assembly through I/O timer U9. By going through the checks for U9 outlined in 6.2.4, the general operation of U9 can be verified. If it is found that a particular port is being handled improperly, then U9 may be at fault.

6.2.8 Analog Conversions

A/D converter U11 is used primarily to read the potentiometer settings of R12, R13, R15 and R16. Starting any conversion consists of writing two narrow active high pulses to U11-6. After 10 microseconds (or less), the end of conversion line (EOC) will go low (U11-7). It will stay low for 100 microseconds, and after it goes high again there will be one active high pulse on U11-9. At this point, the digital version of the input signal read will be transferred to the secondary data bus and into U9. Signals of interest in the analog conversion circuit are:

- U2-3 — Clock in - 3 MHz TTL square wave
- U2-9 — A/D clock - 750 kHz TTL square wave
- U11-6, 22 — Start Conversion - two narrow high going pulses every time a conversion is initiated
- U11-7 — End of Conversion - 85 microseconds low at the completion of a conversion
- U11-9 — Output enable - narrow high going pulse after a conversion has been made
- IN0 through IN7 — All analog inputs should be between 0 and + 5 Vdc.

7. PARTS LIST, COMPONENT LOCATIONS, AND SCHEMATIC DIAGRAM

All replaceable components of the A18A1 assembly are listed in table 7. Figure 3 shows the component locations of the A18A1 assembly. Figure 4 is the schematic diagram of the assembly.

Table 7. System Interface Processor Assembly A18A1 Parts List (10121-6320 Rev. C)

Ref. Desig.	Part Number	Description
C1	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C2	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C3	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C4	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C5	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C6	C26-0016-150	CAP 15UF 20% 16V TANT
C7	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C8	C26-0010-680	CAP 68UF 20% 10V TANT
C9	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C10	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C11	C26-0035-159	CAP 1.5UF 20% 35V TANT
C12	C26-0035-159	CAP 1.5UF 20% 35V TANT
C13	C26-0025-339	CAP 3.3UF 20% 25V TANT
C14	C26-0010-680	CAP 68UF 20% 10V TANT
CR1	1N6263	DIODE .40W 60V HOT CARR
CR2	1N6263	DIODE .40W 60V HOT CARR
CR3	1N5231B	DIODE 5.1V 5% .5W ZENER
J1	J46-0032-008	HDR 8 PIN 0.100" SR
J2	J46-0013-020	HDR 20 PIN 0.100" DR SHRD
J3	J46-0013-034	HDR 34 PIN 0.100" DR SHRD

Table 7. System Interface Processor Assembly A18A1 Parts List (10121-6320 Rev. C) (Cont.)

Ref. Desig.	Part Number	Description
Q1	2N2222A	XSTR SS/GP NPN TO-18
R1	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R2	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R3	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R4	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R5	R50-0010-103	RES 10K 2% 10SIP 9RES
R6	R65-0003-512	RES 5.1K 5% 1/4W CAR FILM
R7	R65-0003-222	RES 2.2K 5% 1/4W CAR FILM
R8	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R9	R50-0010-103	RES 10K 2% 10SIP 9RES
R10	R65-0003-104	RES 100K 5% 1/4W CAR FILM
R12	R30-0008-203	RES VAR PCB 20K 1/2W 10%
R13	R30-0008-203	RES VAR PCB 20K 1/2W 10%
R14	R65-0003-392	RES 3.9K 5% 1/4W CAR FILM
R15	R30-0008-203	RES VAR PCB 20K 1/2W 10%
R16	R30-0008-203	RES VAR PCB 20K 1/2W 10%
R17	R65-0003-103	RES 10K 5% 1/4W CAR FILM
R18	R65-0003-562	RES 5.6K 5% 1/4W CAR FILM
S1	S50-0001-004	SW SPST 4SEC .1A SLD DIP
S2	S06-0002-100	SW PB SPST NO MOM BLK PCT
TP1	J-0071	TP PWB BRN TOP ACCS .080"
TP2	J-0066	TP PWB RED TOP ACCS .080"
U1	I05-0000-074	IC 74LS74A PLASTIC TTL
U2	I15-0000-074	IC 74HC74 PLASTIC CMOS
U3	I05-0000-002	IC 74LS02 PLASTIC TTL
U4	10121-8401	KIT FIRMWARE SYS INT
U5	I27-0006-001	IC MIPRCS 8-BIT 8085
U6	I01-0000-153	IC 4021B PLASTIC CMOS
U7	I15-0000-373	IC 74HC373 PLASTIC CMOS
U8	(SEE NOTE.)	PROGRAMMED PROM
U9	I26-0003-001	IC 256X8 SRAM 8155-2
U10	I01-0000-156	IC 4094B PLASTIC CMOS
U11	I40-0011-001	IC ADC0809 PLASTIC CMOS
U12	I26-0010-001	IC 2KX8 SRAM 6116
VR1	I11-0001-001	IC VR 7805 +5V 1.5A 4%
VR2	I11-0008-005	IC VR 340 +5V 0.1A 2%
XU5	J77-0008-007	SKT IC MACH 40 PIN
XU8	J77-0008-006	SKT IC MACH 28 PIN
Y1	Y15-0004-060	XTAL 6 MHZ

NOTE

The part number for U8 is 10121-8XXX-X, where XXX-X is the four character software kit code found on the PROM label. For example, if the code is 501C, the part number for the programmed PROM is 10121-8501-C.

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R12 Tune power CW increases, CCW decreases

R16 CW delay CW = "0" CCW = 1.25 second to dropout

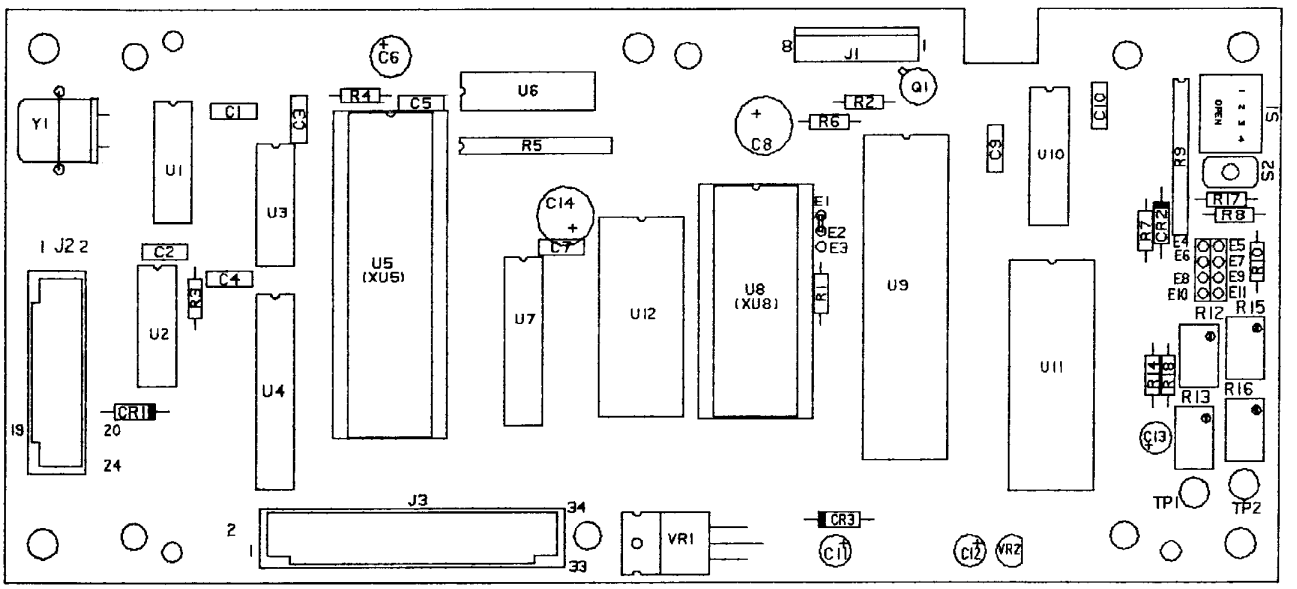

Figure 3. System Interface Processor Board Assembly A18A1 Component Location Diagram (10121-6320 Rev. B)

NOTE: UNLESS OTHERWISE SPECIFIED:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR A COMPLETE DESIGNATION, PREFIX WITH UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.
2. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, ±5%.
3. ALL CAPACITOR VALUES ARE IN MICROFARADS.
4. VENDOR PART NO. CALLOUTS ARE FOR REFERENCE ONLY. COMPONENTS ARE SUPPLIED PER PART NO. IN PARTS LIST.
5. FOR ALTERNATE PROM TYPES: CUT TRACE RUNNING FROM E1 TO E2, AND JUMPER E2 TO E3 FOR 27256.
6. SWITCH S1 OPTIONS:
   S1-1 TGC PRESET (CLOSED)
   TGC LEARN (OPEN)
   S1-2 MANUAL ATTENUATION (CLOSED)
   NORMAL (OPEN)
   S1-3 COUPLER ATTACHED (OPEN)
   NO COUPLER (CLOSED)
   S1-4 SIGNAL GENERATOR MODE (OPEN)

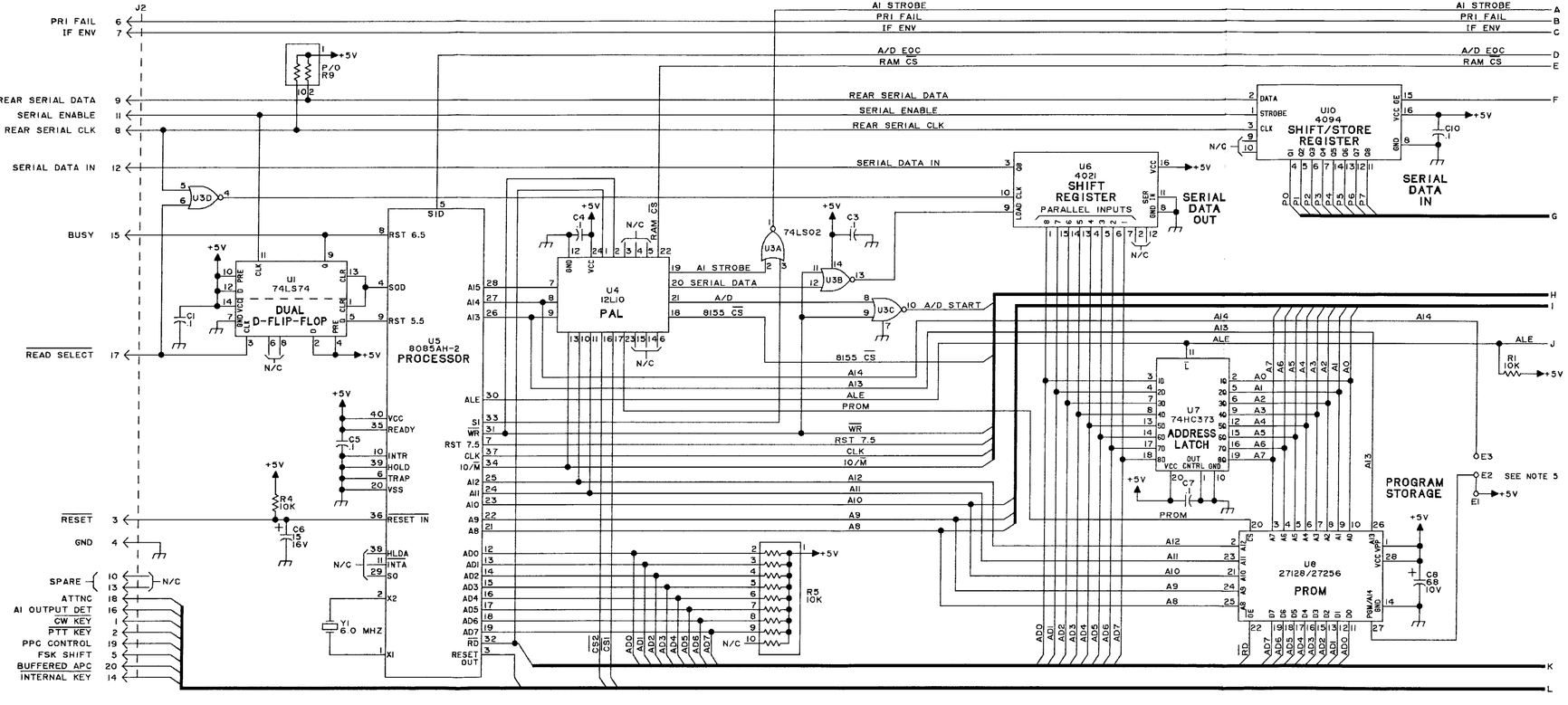

Figure 4. System Interface Processor Assembly, A18A1 Schematic Diagram (10121-6321 Rev. B) (Sheet 1 of 2)

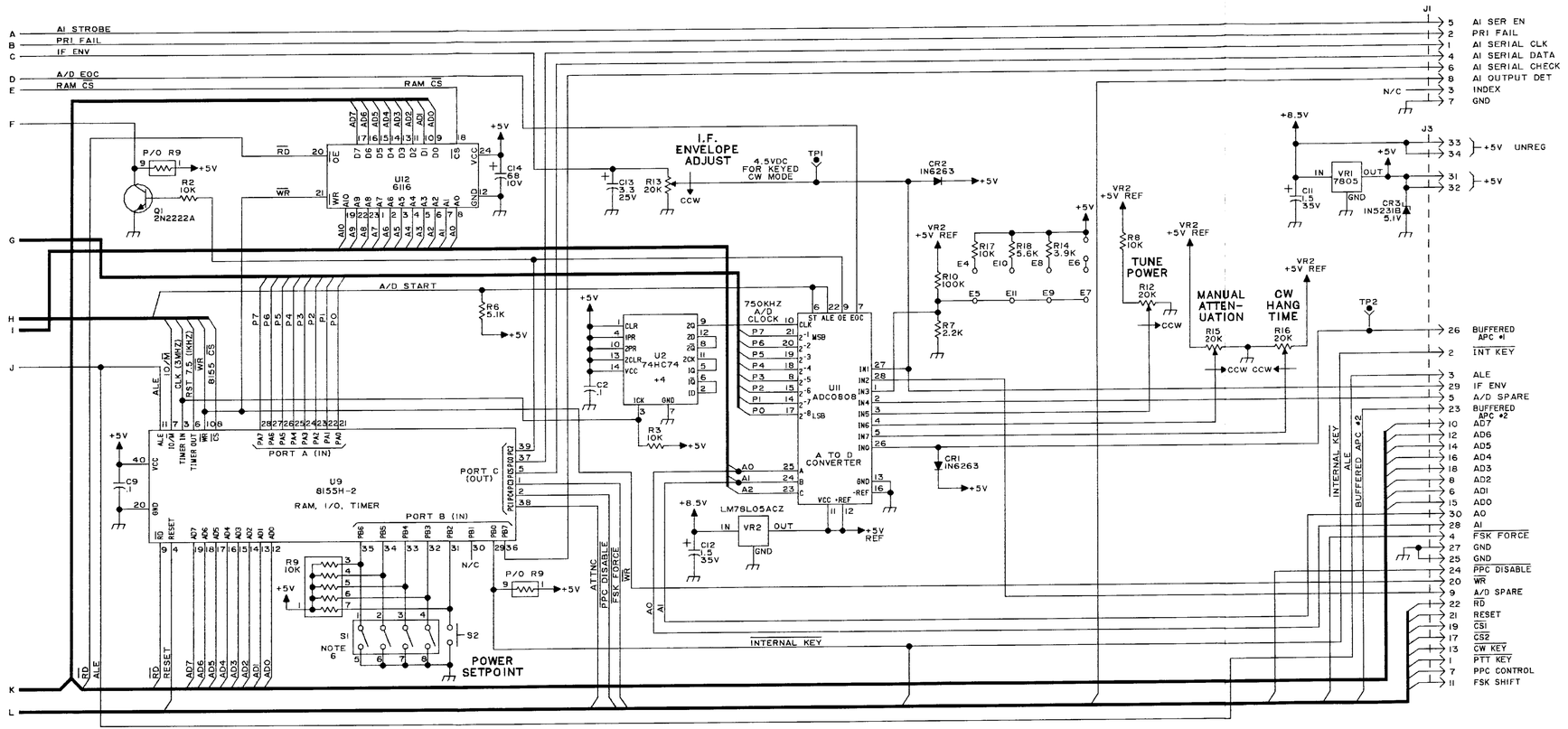

Figure 4. System Interface Processor Assembly, A18A1 Schematic Diagram (10121-6321 Rev. B) (Sheet 2 of 2)

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A18A2
INTERFACE SUPPLEMENT FOR RF-1310A-02, TO INTERFACE WITH THE RF-130A-01/02 AND RF-745A-02

This supplement contains information for the A18A2 unit instruction section of the RF-1310A Instruction Manual. This supplement documents the System Interface I/O Assembly supplied with the RF-1310A-02 Exciter. This exciter is configured to be used in the RF-130A-01/02 and RF-745A-02 Transmitter Systems.

The following are instructions for converting the RF-1310A to an RF-1310A-02 manual:

a. Open the supplement package and verify that all contents are present as follows:

   Qty. 1 - 10-1/2" x 11" RF-1310A-02 front cover insert

   Qty. 1 - 2-1/2" x 11" spine art insert

   Qty. 1 - 10121-0122, A18A2 System Interface Supplement (insertable section)

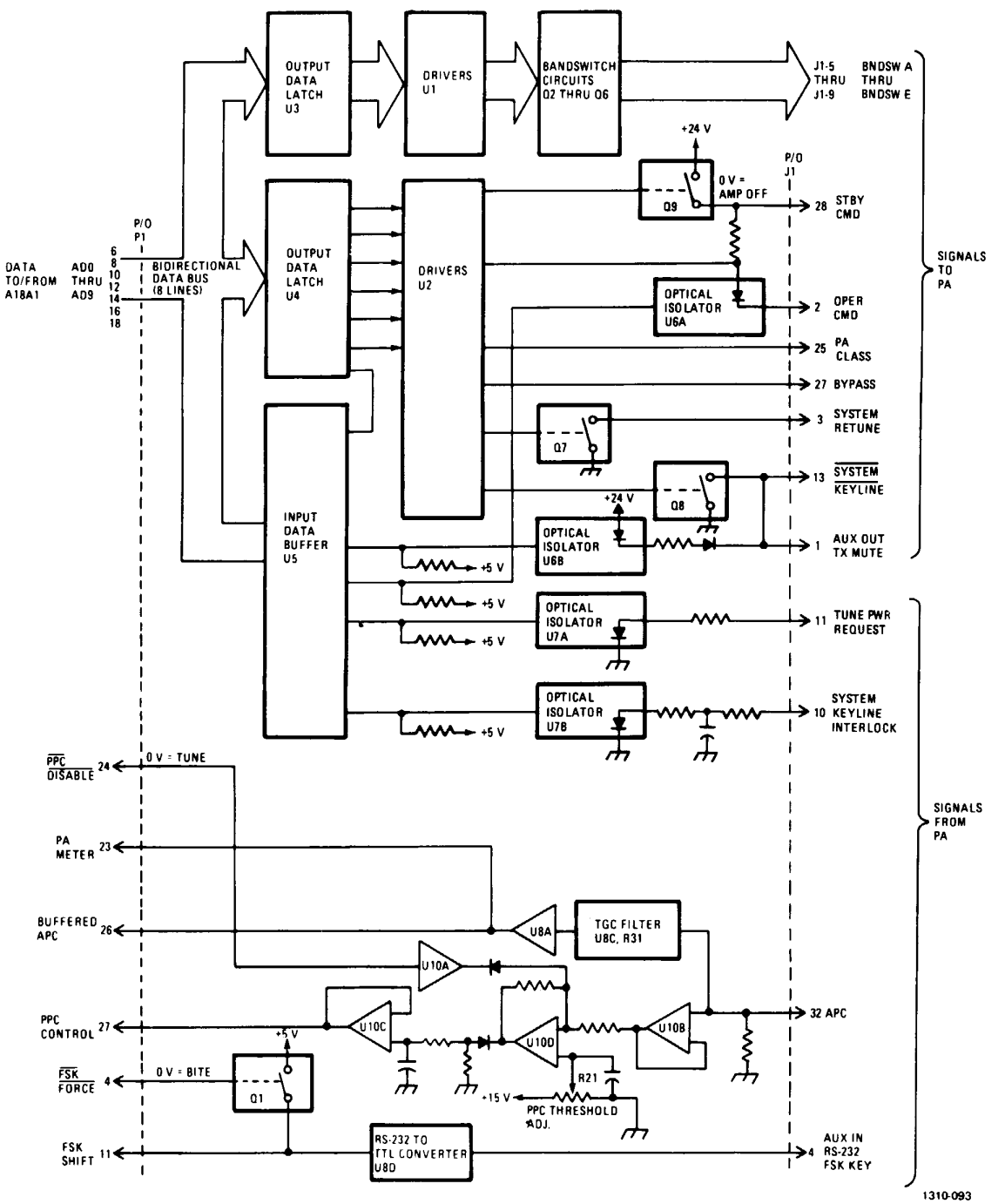
b. A "temporary" cover was supplied with your manual. Remove this cover from the clear plastic envelope on the face of the binder, and replace it with the supplied cover.

c. Remove the temporary spine art from the clear plastic envelope at the back of the binder, and replace it with the supplied spine art.

d. Open the manual to the A18A2 tab section. Remove the temporary page immediately following the section tab and replace it with the supplied A18A2 supplement.

e. Discard this sheet.

A18A2
SYSTEM INTERFACE I/O BOARD ASSY. FOR RF-1310A-02



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SYSTEM INTERFACE I/O BOARD ASSEMBLY A18A2

1. GENERAL DESCRIPTION

The System Interface I/O Board Assembly A18A2 acts as a buffer between the RF-1310A and the transmitter's power amplifier (PA). Control signals and data are received from the System Interface as TTL compatible levels. A18A2 converts these logic levels into high level current signals that can control the PA. Likewise, fault and readback signals generated by the PA are converted to levels that can be read by A18A1. A simplified schematic of the A18A2 Assembly is shown on the front cover of this unit instruction section. Circuit elements include:

- An 8-bit bidirectional bus to transfer data between A18A1 and A18A2
- Two eight-bit latches to receive data from A18A1
- An eight-bit tristate buffer to receive fault and readback signals from the PA
- Several operational amplifiers configured to monitor, detect, or condition analog signals generated by the PA

The relative position of A18A2 in the exciter's chassis is shown in figure 1 of the A18A1 unit instruction section.

2. INTERFACE CONNECTIONS

Table 1 lists all A18A2 System Interface I/O Assembly (10121-6350) interface connections for the RF-130A-01/02 and RF-745A-02 systems. The pins of connector A18A2P1 carry signals to and from A18A1. Signals going to and coming from the PA pass through A18A2J1. Power supply connections are made via A18A2J2. Some signal names change at the Exciter/PA Interface. Specific system signal names are included in table 2.

Table 1. RF-1310A A18A2 System Interface Assembly Interface Lines for RF-130A-01/02 and RF-745A-02

Connector	Function	To	From
A18A2P1-1	PTT KEY	---	A18A1J3-1
A18A2P1-2	INTERNAL KEY	---	A18A1J3-2
A18A2P1-3	SPARE	---	---
A18A2P1-4	FSK FORCE	---	A18A1J3-4
A18A2P1-5	SPARE	---	---
A18A2P1-6	AD1	BIDIRECTIONAL	A18A1J3-6
A18A2P1-7	PPC CONTROL	A18A1J3-7	---
A18A2P1-8	AD2	BIDIRECTIONAL	A18A1J3-8
A18A2P1-9	SPARE	---	---
A18A2P1-10	AD7	BIDIRECTIONAL	A18A1J3-10
A18A2P1-11	FSK SHIFT	A18A1J3-11	---
A18A2P1-12	AD6	BIDIRECTIONAL	A18A1J3-12
A18A2P1-13	CW KEY	---	A18A1J3-13
A18A2P1-14	AD5	BIDIRECTIONAL	A18A1J3-14
A18A2P1-15	AD0	BIDIRECTIONAL	A18A1J3-15
A18A2P1-16	AD4	BIDIRECTIONAL	A18A1J3-16

Table 1. RF-1310A A18A2 System Interface Assembly Interface Lines for RF-130A-01/02 and RF-745A-02 (Cont.)

Connector	Function	To	From
A18A2P1-17	CS2	---	A18A1J3-17
A18A2P1-18	AD3	BIDIRECTIONAL	A18A1J3-18
A18A2P1-19	CS1	---	A18A1J3-19
A18A2P1-20	WR	---	A18A1J3-20
A18A2P1-21	Reset	---	A18A1J3-21
A18A2P1-22	RD	---	A18A1J3-22
A18A2P1-23	PA METER	A18A1J3-23	---
A18A2P1-24	PPC DISABLE	---	A18A1J3-23
A18A2P1-25	GROUND	---	A18A1J3-25
A18A2P1-26	BUFFERED APC	A18A1J3-26	---
A18A2P1-27	GROUND	---	A18A1J3-27
A18A2P1-28	A1	---	A18A1J3-28
A18A2P1-29	SPARE	---	A18A1J3-29
A18A2P1-30	A0	---	A18A1J3-30
A18A2P1-31	+ 5 V	---	A18A1J3-31
A18A2P1-32	+ 5 V	---	A18A1J3-32
A18A2P1-33	+ 5 V UNREG	A18A1J3-33	---
A18A2P1-34	+ 5 V UNREG	A18A1J3-34	---
A18A2J2-1	+ 5 V UNREG	---	A16A3-E29
A18A2J2-2	+ 15 V	---	A16A3-E31
A18A2J2-3	-15 V	---	A16A3-E28
A16A2J2-4	INDEX	---	---
A18A2J2-5	+ 24 V	---	A16A3-E30
A18A2J2-6	GROUND	---	A16A3-E24

Table 2. A18A2/PA Interface Signals

A18A2 Connector J1	To/From RF-1310A Rear Panel	Signal Name at A18A2 Pc Board	Signal at RF-130A-01 System	Signal at RF-745A-02 System
J1-1	J10-15	XMIT MUTE	XMIT MUTE	XMIT MUTE
J1-2	J11-19	OPER COMMAND	+ 20V OPERATE	OPER CMD
J1-3	J11-37	SYSTEM RETUNE	GROUND PULSE	SYS RETUNE CMD
J1-4	J10-17	RS-232 FSK KEY	RS-232 FSK	RS-232 FSK
J1-5	J11-36	BNDSW A	BAND CODE LINE 1	PA BANDSWITCH CODE A
J1-6	J11-18	BNDSW B	BAND CODE LINE 2	PA BANDSWITCH CODE B
J1-7	J11-1	BNDSW C	BAND CODE LINE 3	PA BANDSWITCH CODE C
J1-8	J11-35	BNDSW D	BAND CODE LINE 4	PA BANDSWITCH CODE D
J1-9	J11-3	BNDSW E	BAND CODE LINE 5	PA BANDSWITCH CODE E
J1-10	J11-11	SYS KEYLINE INTLK	+ 28V INTERLOCK	SYS KEYLINE INTLK
J1-11	J11-12	TUNE PWR REQUEST	+ 20 CARRIER INSERT	SYS TUNE PWR REQUEST

Table 2. A18A2/PA Interface Signals (Cont.)

A18A2 Connector J1	To/From RF-1310A Rear Panel	Signal Name at A18A2 Pc Board	Signal at RF-130A-01 System	Signal at RF-745A-02 System
J1-12	J11-23	CW KEY	CW/RATT KEY	EXT CW/RATT KEYLINE
J1-13	J11-6	SYSTEM KEYLINE	GND KEYLINE	SYS KEYLINE
J1-14	J11-15	SUMMARY	N/C	N/C
J1-15	J11-8	N/C	CHASSIS GND	CHASSIS GND
J1-16	J11-17	N/C	SHIELD GROUND	SHIELD (FOR APC)
J1-17	J11-10	N/C	SPARE	SPARE
J1-18	J11-5	BYPASS REQUEST	SPARE	LOCAL BYPASS REQUEST
J1-19	J11-32	N/C	SPARE	SPARE
J1-20	J11-24	PA FAULT	SPARE	FAULT
J1-21	J11-4	N/C	SPARE	LOCAL OVERRIDE CONTROL
J1-22	J11-22	N/C	SPARE	TGC
J1-23	J11-2	N/C	SPARE	STBY READBACK
J1-24	J11-29	N/C	SPARE	SPARE
J1-25	J11-13	PA CLASS	CW/RATT GROUND	PA CLASS
J1-26	J11-30	PTT KEY (FLOAT + 12V)	PTT + 12V KEY	PTT KEY (+ 12V IN)
J1-27	J11-14	BYPASS	SPARE	BYPASS COMMAND
J1-28	J11-16	STBY CMD	+ 28V STBY AND OPER	STBY CMD
J1-29	J11-21	N/C	N/C	N/C
J1-30	-----	N/C	N/C	N/C
J1-31	J11-9	PTT RETURN	FLOATING 12 VDC	EXT PTT RET
J1-32	J11-7	APC	APC	APC
J1-33	-----	N/C	N/C	N/C
J1-34	J10-6	INT KEY	INT KEY	INT KEY

3. FUNCTIONAL DESCRIPTION

The following paragraphs describe the circuits of A18A2 assemblies that are installed in exciters used in the RF-130A-01/02 and RF-745A-02 transmitting systems. A block diagram of the circuit is shown on the front cover of this section. The System Interface I/O Assembly A18A2 schematic diagram is located at the end of this section.

One of the primary functions of the A18A2 Assembly is to translate the TTL compatible signals, sent by the A18A1 Assembly, into the high current level signals needed to control the PA. The A18A2 Assembly is also equipped to receive readback and fault signals from the PA, and relay corresponding signals to A18A1.

3.1 PA Control Commands

The PA control commands include:

- System Keyline
- Standby Command
- Operate Command
- System Retune
- PA Class
- PA Bypass
- 5-Wire Bandswitch Code

The commands are generated on the A18A1 Assembly and sent to A18A2 via an eight-bit bidirectional data bus. The data is latched into U3 and U4. U3 holds the 5-wire bandswitch code control signals and U4 holds the other six PA control commands. The data is latched into U3 and U4 by signals generated by address decoder U9, in response to the CS1, WR, RD, and A0 signals received from A18A1.

3.1.1 System Keyline (RF-745A-02) or Ground Keyline (RF-130A-01/02)

The System Keyline signal is used to key the PA. Transistor Q8 is used as a solid-state switch to set the state of the active low signal. The key command is sent from A18A1 on line AD1 of the data bus. The data on that line is clocked into U4 and appears at the 2Q output (pin 5) of that integrated circuit. The level at 2Q is inverted by a driver in U2. When the U2 input is high, Q8 is biased off and the System Keyline Signal will be inactive (high). When the U2 input is low, Q8 is turned on to make the System Keyline Signal active (low). The state of the circuit elements for this signal are summarized in table 3.

Table 3. Logic Levels for System Keyline Command

Level from A18A1 (AD1)	Level at U4-5 (2Q)	Level at U2-14	State of Q8	System Keyline
H	H	L	OFF	High (Inactive)
L	L	H	ON	Low (Active)

3.1.2 Standby Command

The Standby Command is used to place the PA in Standby. The standby state is used to warm up the PA prior to transmission. The Standby Command remains active when the PA is placed in operate. Transistor Q9 is used as a solid-state switch to control the current and voltage level of the Standby Command signal. Q9 is biased on and off in response to commands sent from A18A1. The initial command is sent from A18A1 on AD2 of the data bus and clocked into U4. The clocked-in level appears at output 3Q of U4.

The output of U4 is inverted by a driver in U2. When the U2 is high, Q9 is biased on. When the U2 input is low, Q9 is biased off. When Q9 is on, the Standby Command signal will be pulled to approximately + 24 V. This will supply enough current to activate the standby relay in the PA. The states of the circuit elements that are involved with the Standby command are summarized in table 4.

Table 4. Logic Levels for Standby Command

Level from A18A1 (AD2)	Level at U4-6 (3Q)	Level at U2-15	State of Q9	Standby Command
H	H	L	ON	High (+ 24 V) - Active
L	L	H	OFF	Low (0 V) - Inactive

3.1.3 System Retune (RF-745A-02) or Ground Pulse (RF-130A-01/02)

The System Retune command is used to initiate a transmitter tune cycle. The signal to the PA is output directly from an inverting driver of U2. The state of the binary signal is controlled by the microprocessor on A18A1. The signal is sent to A18A2 on the AD5 line of the data bus and latched into the 6Q output of U4. The output at U4 pin 15 drives transistor Q7. A 40 to 45 millisecond low-going pulse is sent to the antenna coupler, which causes the tuning elements to return to the home position.

3.1.4 Bypass Command (RF-745A-02 only)

The RF-745A-02 can be configured for either 10-kW, or 1-kW operation. The configuration is accomplished by the placement or removal of specific jumpers on the Control PWB Assembly 7A3 into the system I-Box. When the system is set for 10-kW operation and the SYSTEM SELECT switch on the I-Box front panel is actuated, an active-low LOCAL BYPASS REQUEST signal is sent to the exciter. The exciter responds to the LOCAL BYPASS REQUEST signal by sending an active-low BYPASS COMMAND to the I-Box. When the BYPASS COMMAND line goes low, the + 28 volts on the BYPASS RELAY line is removed to de-energize the relays of the 1-kW/10-kW Switchover Assembly. When the system is set for 1-kW operation, the LOCAL BYPASS REQUEST is switched to + 15 volts to disable bypass operation.

This signal is not used in the RF-130A-01/02.

3.1.5 PA Bandswitch Codes for RF-130A-01/02

PA Bandswitch Code 1 through PA Bandswitch Code 5 are used to request the operating frequency bands for the PA. Together, the five PA Bandswitch Code signals are called the "five-wire-code". The five-wire-codes are not conventional digital signals, but instead are unique combinations of current paths called images. A motor-controlled rotary switch in the PA is used to decode the images and select the requested frequency band.

Bandswitch circuit elements and an example image (current path) are shown in figure 1. Circuit elements in the exciter include five drivers of U1, transistors Q2 through Q6, and diodes CR3 through CR12. Circuit elements in the PA include the PA Bandswitch relay and two sections of a motor-controlled rotary switch called the Master decoder and Image decoder. The drivers in U1 are used to open and close the path to ground for each of the PA BNDSW code lines. Q2 through Q6, along with their associated diodes CR3, CR5, CR7, CR11, and CR9, provide bidirectional current paths for PA BNDSW code lines that are not grounded through U1. Current paths in the PA are open and closed by the Master decoder and Image decoder. The PA Bandswitch relay is energized by any current flow in the circuit. The energized relay turns on the bandswitch motor in the PA.

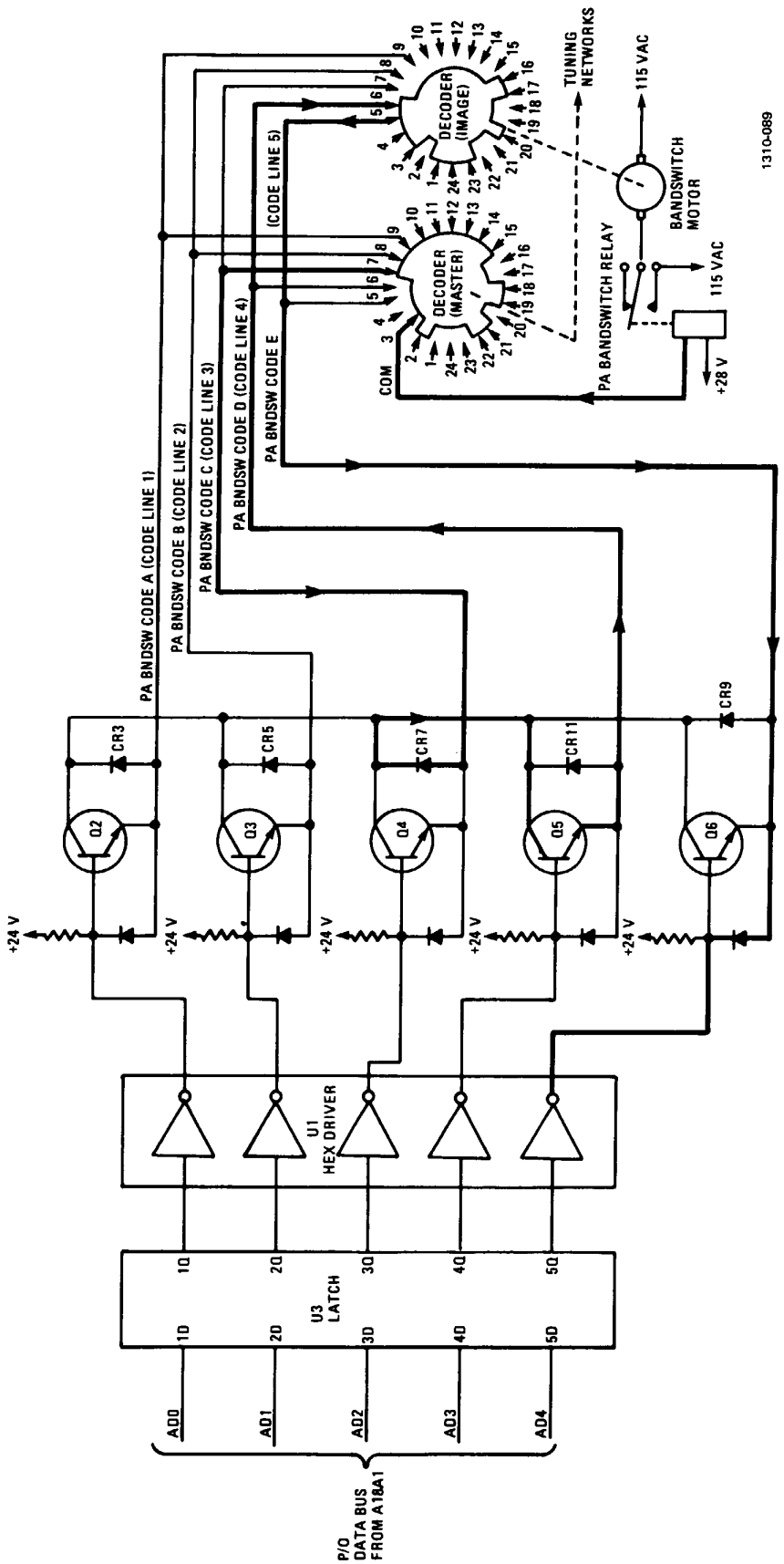

Figure 1. PA Bandswitch Circuit in RF-130A-01/02

A tuning change request initiated by the exciter creates a current in the circuit. This current energizes the PA Bandswitch relay and turns on the motor. The motor rotates the switch until all possible current paths are opened. Sections of the switch not shown in figure 1 select the requested tuning network as the image is decoded.

Tuning commands originate on the A18A1 Assembly. The command is sent to A18A2 as a five-bit binary code on data buslines AD0 through AD4. The five bits are latched into U3.

Outputs 1Q through 5Q of U3 control drivers of U1. A logic high at a drivers input will ground its output. A logic low at a driver's input will open the output of the driver and allow the base of the associated transistor to be pulled up to 24 volts.

Table 5 summarizes the binary commands sent from A18A1 and the states of the U1 drivers for the 19 possible frequency bands. The current flow in the circuit at any given time is dependent upon the position of the Decoders in the PA. In figure 1, the exciter is requesting the 2.0 MHz tuning band.

Table 5. Bandswitch Code Logic Summary

Exciter Frequency Band in MHz	U3 Outputs 0 = 0 V; 1 = 3.5 V					U1 Outputs 0 = 0 V; 1 = 24 V				
	1Q	2Q	3Q	4Q	5Q	U1-10	U1-11	U1-12	U1-14	U1-13
2.0 to 2.5	0	0	0	0	1	1	1	1	1	0
2.5 to 3.0	0	0	0	1	1	1	1	1	0	0
3.0 to 3.5	0	0	1	1	1	1	1	0	0	0
3.5 to 4.0	0	1	1	1	1	1	0	0	0	0
4.0 to 5.0	1	1	1	1	0	0	0	0	0	1
5.0 to 6.0	1	1	1	0	1	0	0	0	1	0
6.0 to 7.0	1	1	0	1	1	0	0	1	0	0
7.0 to 8.0	1	0	1	1	1	0	1	0	0	0
8.0 to 10.0	0	1	1	1	0	1	0	0	0	1
10.0 to 12.0	1	1	1	0	0	0	0	0	1	1
12.0 to 14.0	1	1	0	0	1	0	0	1	1	0
14.0 to 16.0	1	0	0	1	0	0	1	1	0	1
16.0 to 18.0	0	0	1	0	0	1	1	0	1	1
18.0 to 20.0	0	1	0	0	1	1	0	1	1	0
20.0 to 22.0	1	0	0	1	1	0	1	1	0	0
22.0 to 24.0	0	0	1	1	0	1	1	0	0	1
24.0 to 26.0	0	1	1	0	0	1	0	0	1	1
26.0 to 28.0	1	1	0	0	0	0	0	1	1	1
28.0 to 30.0	1	0	0	0	0	0	1	1	1	1

3.1.6 PA Bandswitch Codes for RF-745A-02

The bandswitch circuit for the RF-745A-02, as shown in figure 2, is the same as the RF-130A-01 with the following exceptions:

- The exciter five-wire-code is routed from the exciter A18A2 board to the I-Box.
- If the transmitter is in the 10 kW mode, the five-wire- code is routed through the Band Repeater Assembly. The Band Repeater Assembly sends a repeated five-wire-code to the Driver PA via the I-Box.
- If the transmitter is in the 1 kW mode (bypass), the five-wire-code is routed directly to the Driver PA via the I-Box.

3.1.7 Operate Command Line

The Operate Command line is used to activate the high voltage circuitry in the PA. When the Standby Command line is active, + 24 volts is supplied to the Operate Command line through resistors R8 and R45. When the Operate Command line is not active, the current through this resistor is diverted to pin 10 of U2, causing the Operate Command line to remain inactive and preventing the high voltage from being turned on in the PA. When the exciter activates the Operate Command line, pin 10 of U2 becomes an open collector. The resulting current is supplied to the PA, sending the PA into operate.

3.1.8 Operate Readback

The current supplied to the PA on the Operate Command line is sent through opto-isolator U6 to generate an Operate Readback. When the Operate Command line is active, but the warm up timer has not yet timed out, the Operate Command line sees an open circuit and no current is drawn by this line. Once the timer times out, the Operate Command line will now have a load and the current drawn will activate the opto-isolator. This tells the exciter that the PA has actually gone into operate.

3.1.9 PA Class Select (RF-745A-02) or CW/RATT Ground (RF-130A-01/02)

The PA class select line changes the bias on the PA to select the more efficient amplifier class for the modes which do not require high linearity.

3.2 Power Amplifier Readbacks

The PA sends digital and analog readback signals to the exciter. The digital signals include Tune Power Request and System Keyline interlock. The only analog readback signal is the APC signal. A tri-state buffer (U5) is used to interface the digital readback signals with the bidirectional data bus. Analog signals are detected or processed and passed to A18A1.

3.2.1 Tune Power Request (RF-745A-02) or + 20 V Carrier Insert (RF- 130A-01/02)

Tune Power Request is a digital signal used to tell the exciter that the antenna coupler requires tuning or the PA is requesting tune power. The TUNE key on the PA front panel controls the PA's tune request. The high current signal is converted to a TTL signal by an optical isolator.

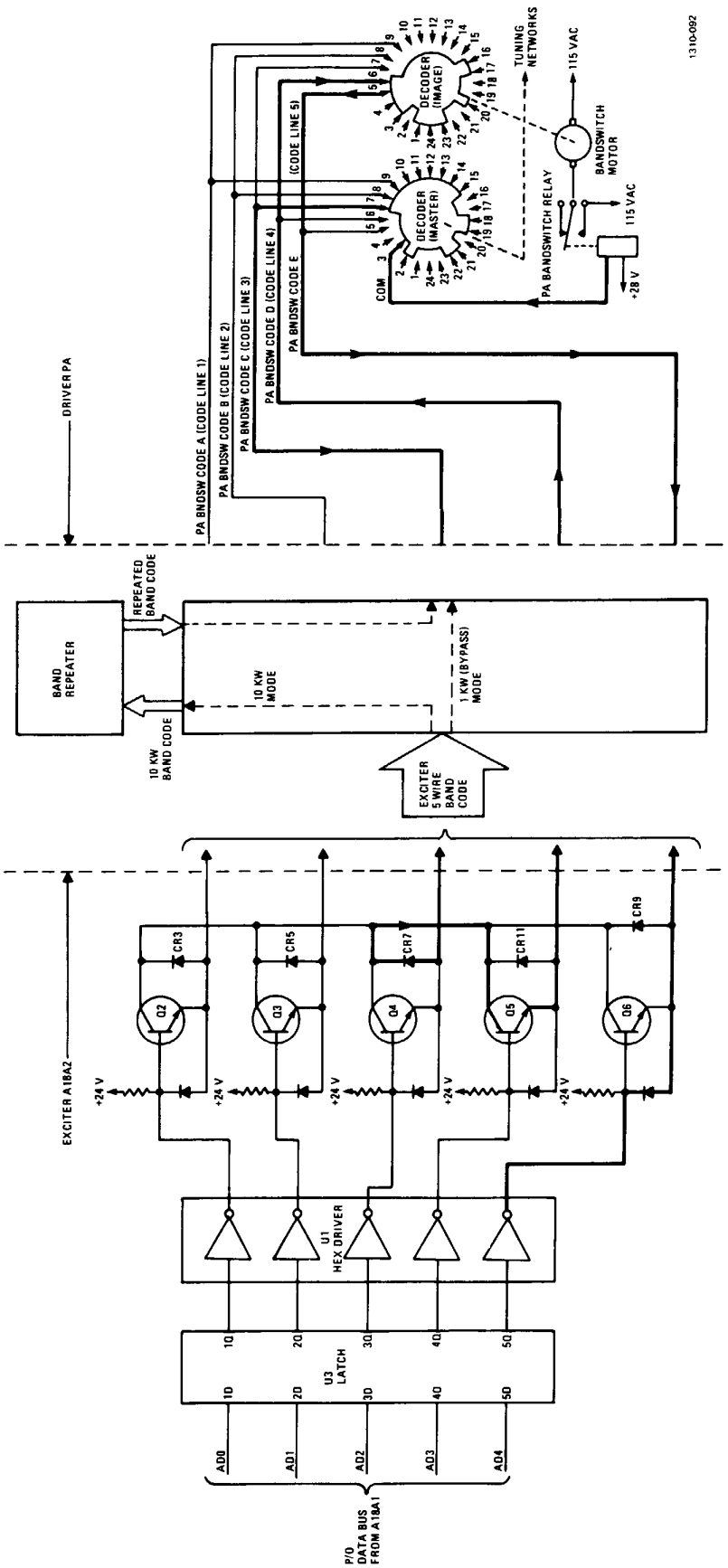

Figure 2. PA Bandswitch Circuit in the RF-745A-02

3.2.2 APC (Average Power Control)

APC is an analog signal that is the result of combining various transmitter power and current indications in the PA. The signal is used by the exciter to regulate gain. The signal is filtered by U11A and scaled down by U11C before being passed to an A-to-D converter on the A18A1 Assembly.

3.2.3 PPC (Peak Power Control)

The PPC signal is derived from the APC signal on the A18A2 Assembly. The PPC signal is used by the exciter to limit the peak output power. The PPC signal is processed on the A18 Assembly, and then used to control the PPC attenuator on Combiner Assembly A4.

On the A18A2 Assembly, the signal from the PA is buffered by U10B and then applied to the inverting input of U10D. At U10D, the signal is compared to the threshold voltage set by R21. The U10D output will be a positive dc level as long as the PPC signal does not exceed the threshold voltage (the PPC Control Signal going to A18A1 will be approximately 0 volts). When the PPC signal level exceeds the threshold voltage, the U10D output will be a negative dc signal, resulting from the difference between the two U10D inputs. The negative signal is passed by CR17 to charge C14 and drive the noninverting input of U10C. U10C delivers a negative voltage to A18A1 that is proportional to the PA output signal level. As the PPC control signal becomes more negative, the attenuation on the Combiner Assembly will increase. When the PPC signal level drops below the threshold level, the U10D output will become positive and CR17 will no longer conduct current. C14 will discharge through R32 and R33 and the U10C output will return to approximately 0 volts. The PPC Control Signal is disabled by the PPC Disable TTL signal during tuning. The active low PPC Disable signal is applied to the noninverting input of U10A. The output of U10A pulls the inverting input of U10D to approximately -15 Vdc, to disable the PPC loop.

3.2.4 RS-232 FSK KEY, TX Mute, CW KEY, PTT Return, and Internal Keyline

The RS-232 FSK key is converted to a TTL compatible signal by U11D. The converted signal is sent to Control Assembly A14 as the FSK shift signal.

The FSK Shift signal can be forced high during the BITE routine by setting the FSK Force line low, to turn on Q1. The FSK Force line is controlled by the Microprocessor on the A18A1 Assembly.

The Transmit Mute signal is an output that can be used to mute a receiver if required. The CW Key signal is passed from the rear panel to the Control Assembly A14.

The PTT KEY and PTT RETURN signals provide an alternative means of keying the system. The method uses the PTT lines in the PA. Optical isolator U8 passes the signal to the A14 Assembly.

The Internal Keyline is an output signal used with the optional 4 ISB Assembly.

3.2.5 System Keyline Interlock

The System Keyline Interlock is an input to the exciter which indicates to the exciter when the system is ready to output power. Fault and Ready information are derived from this line by the exciter system interface software. Opto-isolator U7B is used to isolate the TTL hardware from the voltages present on this input. A filter consisting of R14, R23, and C7 provides short delays required for proper system operation.

4. MAINTENANCE

The PPC Threshold level (R21) must be adjusted with the exciter installed in an operating system. Procedures for adjusting this level can be found in the RF-130A-01/02 and RF-745A-02 Instruction Manuals.

5. PARTS LIST, COMPONENT LOCATIONS, AND SCHEMATIC DIAGRAM

Table 6 lists all replaceable components of the A18A2 Assembly. Component locations are shown in figure 3. The A18A2 circuits are shown schematically in figure 4.

Table 6. System Interface I/O Assembly A18A2 Parts List (10121-6350, Rev. J)

Ref. Desig.	Part Number	Description
A18A2	10121-6350	SYSTEM INTERFACE I/O ASSEMBLY
	E70-0002-002	PAD, TRANSISTOR MOUNTING
C1	C26-0035-220	CAP, 22UF 20% 35V TANT
C2	C26-0035-220	CAP, 22UF 20% 35V TANT
C3	M39014/02-1310V	CAP .1 UF 10% 100V
C4	M39014/02-1310V	CAP .1 UF 10% 100V
C5	M39014/02-1310V	CAP .1 UF 10% 100V
C6	C26-0035-220	CAP, 22UF 20% 35V TANT
C7	C26-0050-339	CAP, 3.3UF 20% 50 V TANT
C8	M39014/02-1310V	CAP .1 UF 10% 100V
C9	M39014/02-1310V	CAP .1 UF 10% 100V
C10	M39014/02-1310V	CAP .1 UF 10% 100V
C11	M39014/02-1310V	CAP .1 UF 10% 100V
C12	M39014/02-1310V	CAP .1 UF 10% 100V
C13	M39014/02-1310V	CAP .1 UF 10% 100V
C14	C26-0025-339	CAP, 3.3 UF 20% 25V TANT
C15	M39014/02-1310V	CAP .1 UF 10% 100V
C16	M39014/02-1310V	CAP .1 UF 10% 100V
CR1	1N5230B	DIODE 4.7V 5% 0.5W ZENER
CR2	1N4007	DIODE, 1A 1000V
CR3	1N4007	DIODE, 1A 1000V
CR4	1N4007	DIODE, 1A 1000V
CR5	1N4007	DIODE, 1A 1000V
CR6	1N4007	DIODE, 1A 1000V
CR7	1N4007	DIODE, 1A 1000V
CR8	1N4007	DIODE, 1A 1000V
CR9	1N4007	DIODE, 1A 1000V
CR10	1N4007	DIODE, 1A 1000V
CR11	1N4007	DIODE, 1A 1000V
CR12	1N4007	DIODE, 1A 1000V
CR13	1N4007	DIODE, 1A 1000V
CR14	1N4454	DIODE, 200MA 75V
CR15	1N5228B	DIODE 3.9V 5% 0.5W ZENER
CR16	1N4454	DIODE, 200MA 75V
CR17	1N4454	DIODE, 200MA 75V
CR18	1N4007	DIODE, 1A 100V
CR19	1N4454	DIODE, 200MA 75V
CR20	1N4454	DIODE, 200MA 75V
CR21	1N4007	DIODE, 1A 1000V
J1	J46-0013-034	HEADER, 34 PIN 0.100"
J2	J46-0022-006	HEADER, 6 PIN 0.100"
P1	10121-7288	CABLE, RIBBON, 34 COND
Q1	2N2907A	XSTR, SS/GP, PNP
Q2	Q25-0001-000	XSTR, SS/GP, NPN
Q3	Q25-0001-000	XSTR, SS/GP, NPN

Table 6. System Interface I/O Assembly A18A2 Parts List (10121-6350, Rev. J) (Cont.)

Ref. Desig.	Part Number	Description
Q4	Q25-0001-000	XSTR, SS/GP, NPN
Q5	Q25-0001-000	XSTR, SS/GP, NPN
Q6	Q25-0001-000	XSTR, SS/GP, NPN
Q7	2N2222A	XSTR, SS/GP, NPN
Q8	2N4239	TRANSISTOR
Q9	2N4236	XSTR, SS/GP, PNP
R1	R65-0003-473	RES,47K 5% 1/4W CAR FILM
R2	R65-0003-332	RES,3.3K 5% 1/4W CAR FILM
R3	R65-0003-103	RES,10K 5% 1/4W CAR FILM
R4	R65-0003-103	RES,10K 5% 1/4W CAR FILM
R5	R65-0003-103	RES,10K 5% 1/4W CAR FILM
R6	R65-0003-103	RES,10K 5% 1/4W CAR FILM
R7	R65-0003-103	RES,10K 5% 1/4W CAR FILM
R8	RCR32G102JM	RES,1.0K 5% 1W CAR COMP
R9	R65-0003-103	RES,10K 5% 1/4W CAR FILM
R10	R65-0003-103	RES,10K 5% 1/4W CAR FILM
R11	R65-0003-103	RES,10K 5% 1/4W CAR FILM
R12	R65-0003-103	RES,10K 5% 1/4W CAR FILM
R13	R65-0003-123	RES,12K 5% 1/4W CAR FILM
R14	R65-0004-222	RES,2.2K 5% 1/2W CAR FILM
R15	R65-0003-471	RES,470 5% 1/4W CAR FILM
R16	R65-0003-222	RES,2.2K 5% 1/4W CAR FILM
R17	R65-0003-472	RES,4.7K 5% 1/4W CAR FILM
R18	R65-0003-472	RES,4.7K 5% 1/4W CAR FILM
R19	R65-0003-512	RES,5.1K 5% 1/4W CAR FILM
R20	R65-0003-183	RES,18K 5% 1/4W CAR FILM
R21	R30-0008-203	RES,VAR,PCB 20K 1/2W 10%
R22	RN55D2611F	RES,2610 1% 1/8W MET FLM
R23	R65-0004-102	RES,1.0K 5% 1/2W CAR FILM
R24	R65-0004-222	RES,2.2K 5% 1/2W CAR FILM
R25	R65-0004-222	RES,2.2K 5% 1/2W CAR FILM
R26	R65-0003-103	RES,10K 5% 1/4W CAR FILM
R27	R65-0003-221	RES,220 5% 1/4W CAR FILM
R28	R65-0003-102	RES,1.0K 5% 1/4W CAR FILM
R29	R65-0003-224	RES,220K 5% 1/4W CAR FILM
R30	R65-0003-182	RES,1.8K 5% 1/4W CAR FILM
R31	RN55D4641F	RES,4640 1% 1/8W MET FLM
R32	R65-0003-303	RES,30K 5% 1/4W CAR FILM
R33	R65-0003-103	RES,10K 5% 1/4W CAR FILM
R34	R65-0003-102	RES,1.0K 5% 1/4W CAR FILM
R35	R65-0003-102	RES,1.0K 5% 1/4W CAR FILM
R36	R65-0003-103	RES,10K 5% 1/4W CAR FILM
R37	R65-0003-102	RES,1.0K 5% 1/4W CAR FILM
R38	RN55D6812F	RES,68.1K 1% 1/8W MET FLM
R39	RN55D6812F	RES,68.1K 1% 1/8W MET FLM
R40	R65-0003-222	RES,2.2K 5% 1/4W CAR FILM
R41	R65-0003-332	RES,3.3K 5% 1/4W CAR FILM
R42	R65-0003-103	RES,10K 5% 1/4W CAR FILM

Table 6. System Interface I/O Assembly A18A2 Parts List (10121-6350, Rev. J) (Cont.)

Ref. Desig.	Part Number	Description
R43	R65-0003-512	RES,5.1K 5% 1/4W CAR FILM
R44	R65-0003-821	RES,820 5% 1/4W CAR FILM
R45	R76-0001-001	CURRENT LIMITER,CER,140O
R46	R65-0003-103	RES,10K 5% 1/4W CAR FILM
R47	R65-0003-103	RES,10K 5% 1/4W CAR FILM
R48	R65-0003-103	RES,10K 5% 1/4W CAR FILM
U1	I90-0006-003	IC XSTR ARRAY DARL
U2	I90-0006-003	IC XSTR ARRAY DARL
U3	I05-0000-374	IC 74LS374 PLASTIC TTL
U4	I05-0000-374	IC 74LS374 PLASTIC TTL
U5	I05-0000-244	IC 74LS244 PLASTIC TTL
U6	I75-0007-000	OPTOISOLATOR DUAL
U7	I75-0007-000	OPTOISOLATOR DUAL
U8	I75-0007-000	OPTOISOLATOR DUAL
U9	I05-0000-138	IC 74LS138 PLASTIC TTL
U10	I30-0038-001	IC OP AMP QUAD
U11	I30-0038-001	IC OP AMP QUAD

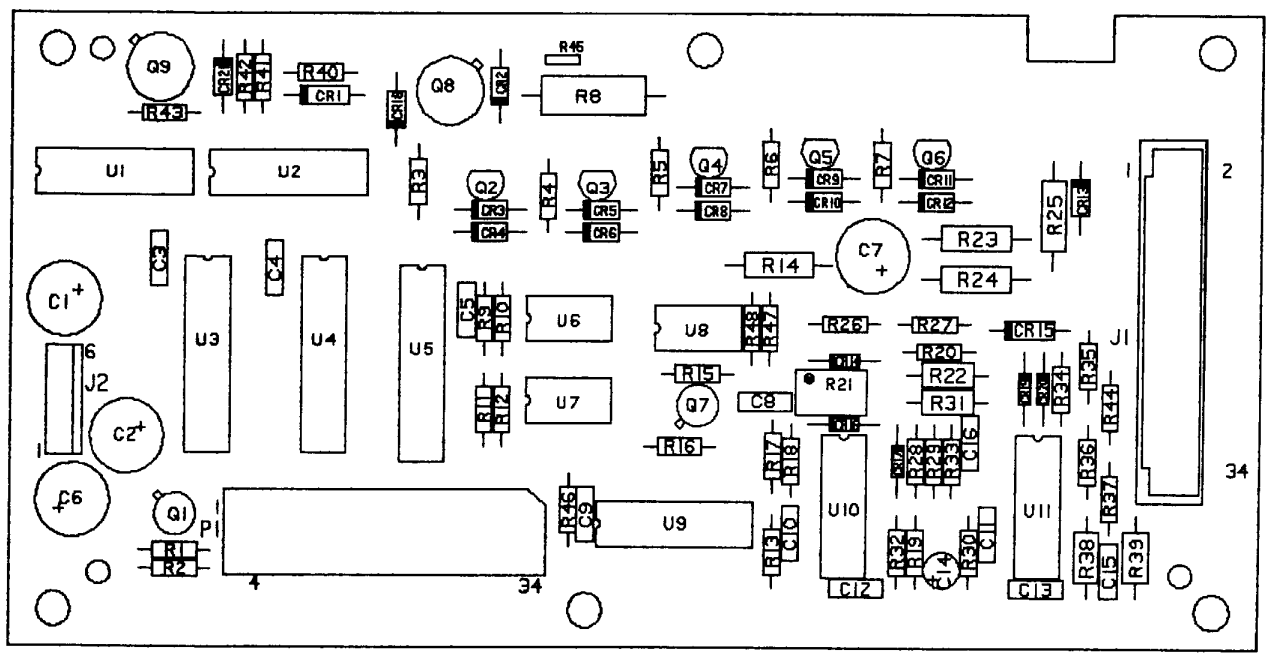

Figure 3. System Interface I/O Assembly A18A2 Component Location (10121-6350, Rev. E)

NOTE: UNLESS OTHERWISE SPECIFIED:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR A COMPLETE DESIGNATION, PREFIX WITH UNIT NO. AND/OR ASSEMBLY NO. DESIGNATION.
2. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, ±5%.
3. ALL CAPACITOR VALUES ARE IN MICROFARADS.
4. VENDOR PART NO. CALLOUTS ARE FOR REFERENCE ONLY. COMPONENTS ARE SUPPLIED PER PART NO. IN PARTS LIST.

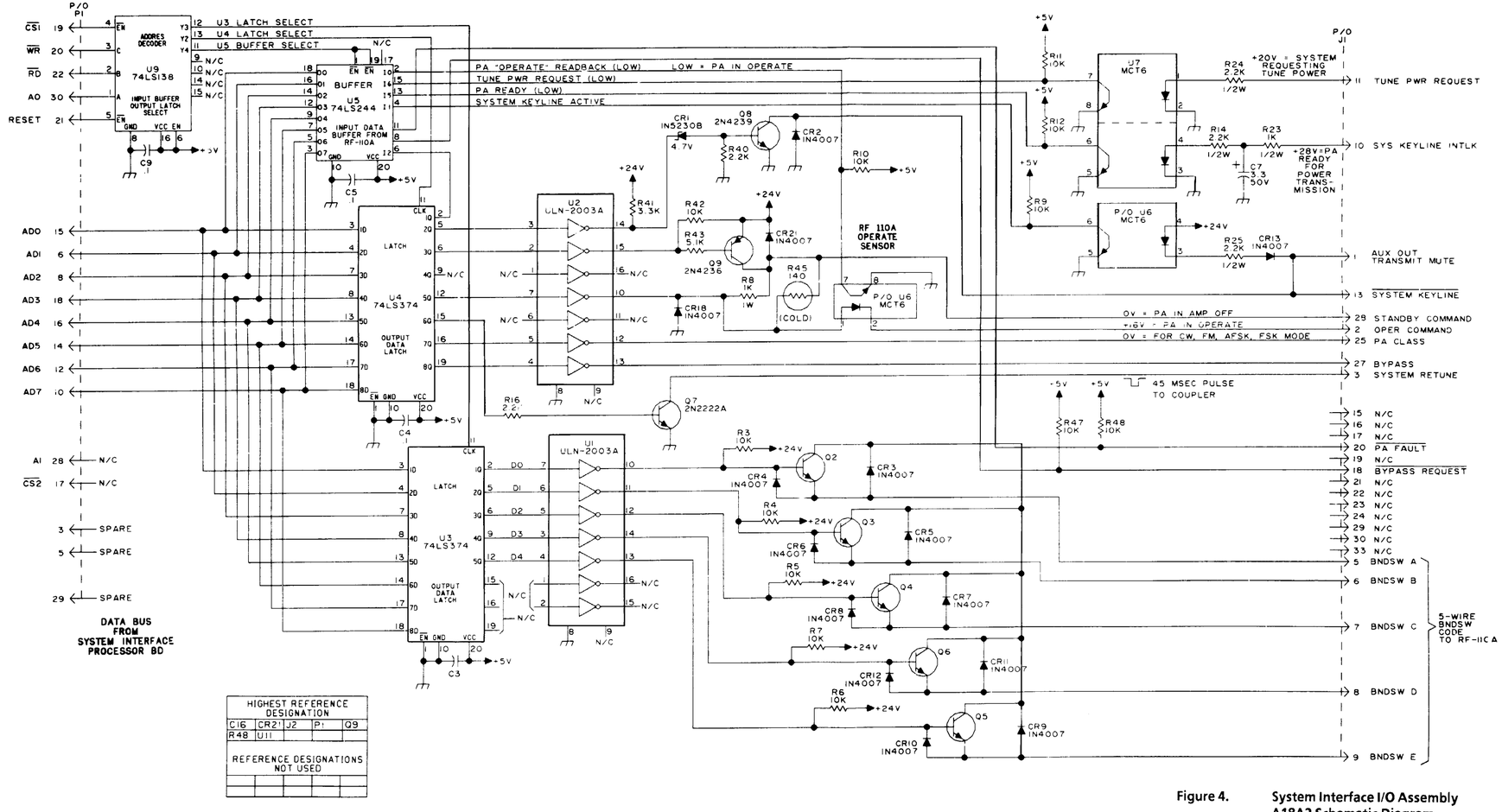

Figure 4. System Interface I/O Assembly A18A2 Schematic Diagram (10121-6351 Rev. H) (Sheet 1 of 2)

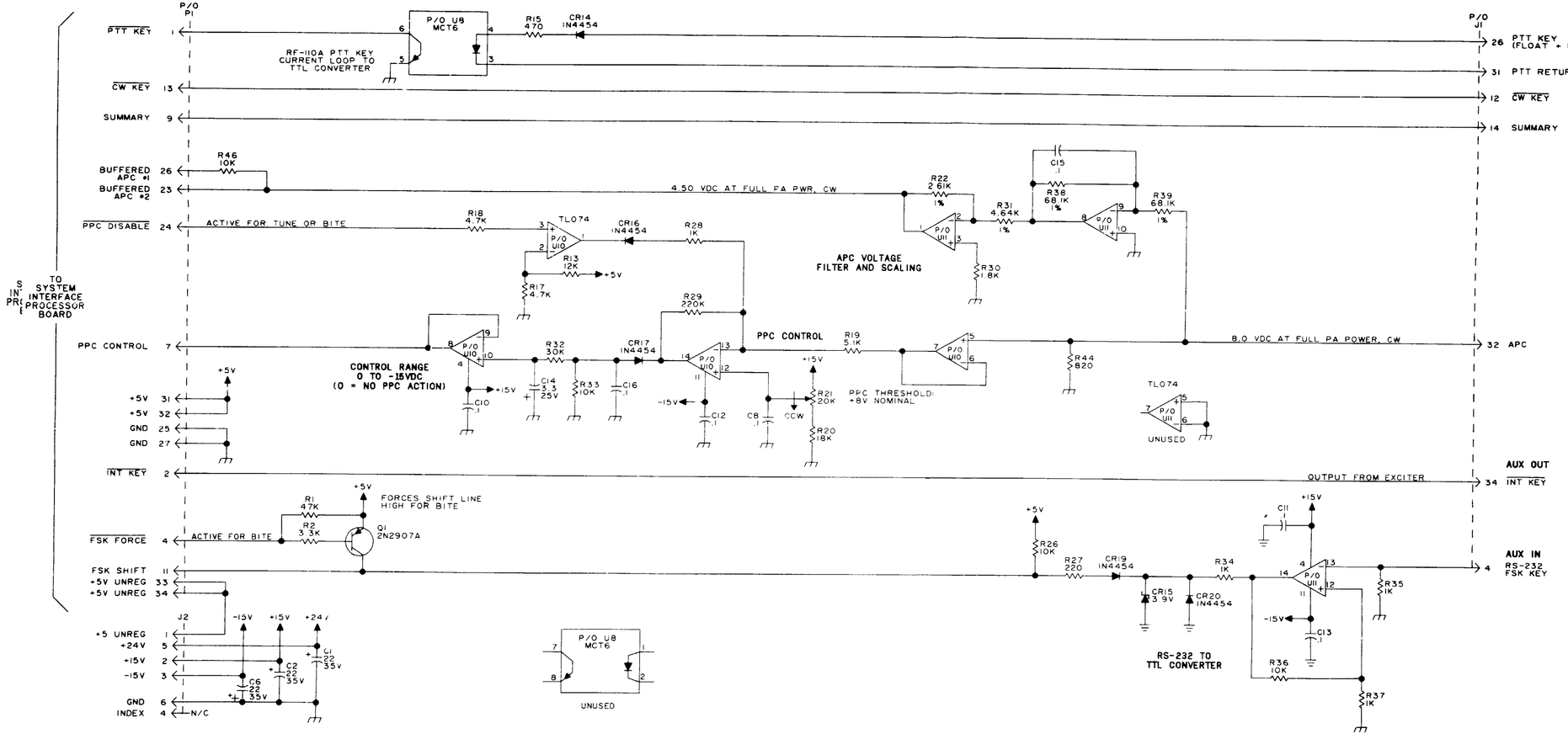

Figure 4. System Interface I/O Assembly A18A2 Schematic Diagram (10121-6351 Rev. H) (Sheet 2 of 2)

A20
FILTER ASSY

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LIST OF FIGURES

LIST OF TABLES

FILTER ASSEMBLY A20

1. PARTS LISTS AND COMPONENT LOCATION DIAGRAMS

Tables 1 through 3 are parts lists for the A20A1, A20A2, and A20A3 subassemblies. Figure 1 shows the overall locations of the A20 subassemblies. Figures 2 through figure 4 show the component locations of the A20A1, A20A2, and A20A3 subassemblies.

2. SCHEMATIC DIAGRAMS

A20 schematic diagrams are included in the RF-1310 Interconnection Schematic Diagram (10121-1031) located in the Major Assembly Location and Interconnection section of this manual.

Table 1. Filter Board Assembly A20A1 Parts List (10121-1260 Rev. B)

Ref. Desig.	Part Number	Description
A20A1	10121-1260	FILTER BOARD #1
J1	J46-0040-048	CONN, 48 PIN
J2	J46-0040-048	CONN, 48 PIN
J8	J22-0035-001	CONNECTOR,25 PIN
J9	J22-0035-002	CONNECTOR,37 PIN
J10	J22-0035-002	CONNECTOR,37 PIN
J11	J22-0035-002	CONNECTOR,37 PIN
L1	MS75085-8	COIL, RF 120 UH 10%
L2	MS75085-8	COIL, RF 120 UH 10%
L3	MS75085-8	COIL, RF 120 UH 10%
L4	MS75085-8	COIL, RF 120 UH 10%
L5	MS75085-8	COIL, RF 120 UH 10%
R1	MP-1142	CIRCUIT JUMPER

Table 2. Filter Board Assembly A20A2 Parts List (10121-1270 Rev. C)

Ref. Desig.	Part Number	Description
C2	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C3	M39014/02-1292V	CAP 4700PF 10% 200V CER-R
C4	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C6	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C7	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C8	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C9	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C10	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C11	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C12	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C13	M39014/02-1310V	CAP .1UF 10% 100V CER-R

Table 2. Filter Board Assembly A20A2 Parts List (10121-1270 Rev. C) (Cont.)

Ref. Desig.	Part Number	Description
C14	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C15	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C16	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C17	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C18	M39014/02-1292V	CAP 4700PF 10% 200V CER-R
C19	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C20	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C23	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C24	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C25	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C26	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C28	M39014/02-1292V	CAP 4700PF 10% 200V CER-R
C29	M39014/02-1292V	CAP 4700PF 10% 200V CER-R
C30	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C32	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C33	M39014/02-1292V	CAP 4700PF 10% 200V CER-R
C34	M39014/02-1292V	CAP 4700PF 10% 200V CER-R
C35	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C36	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C37	M39014/02-1292V	CAP 4700PF 10% 200V CER-R
C38	M39014/02-1292V	CAP 4700PF 10% 200V CER-R
C39	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C40	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C41	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C42	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C43	M39014/02-1292V	CAP 4700PF 10% 200V CER-R
C44	M39014/02-1292V	CAP 4700PF 10% 200V CER-R
C45	M39014/02-1292V	CAP 4700PF 10% 200V CER-R
C46	M39014/02-1292V	CAP 4700PF 10% 200V CER-R
C47	M39014/02-1292V	CAP 4700PF 10% 200V CER-R
C48	M39014/02-1292V	CAP 4700PF 10% 200V CER-R
C49	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C50	M39014/02-1310V	CAP .1UF 10% 100V CER-R
L2	MS75085-8	COIL 120UH 10% FXD RF
L3	MS75085-14	COIL 390UH 10% FXD RF
L4	MS75084-15	COIL 18.0UH 10% FXD RF
L6	MS75084-15	COIL 18.0UH 10% FXD RF
L7	MS75084-15	COIL 18.0UH 10% FXD RF
L8	MS75085-8	COIL 120UH 10% FXD RF
L9	MS75085-8	COIL 120UH 10% FXD RF
L10	MS75085-8	COIL 120UH 10% FXD RF
L11	MS75085-8	COIL 120UH 10% FXD RF
L12	MS75084-15	COIL 18.0UH 10% FXD RF

Table 2. Filter Board Assembly A20A2 Parts List (10121-1270 Rev. C) (Cont.)

Ref. Desig.	Part Number	Description
L13	MS75085-8	COIL 120UH 10% FXD RF
L14	MS75085-8	COIL 120UH 10% FXD RF
L15	MS75085-8	COIL 120UH 10% FXD RF
L16	MS75085-8	COIL 120UH 10% FXD RF
L17	MS75085-8	COIL 120UH 10% FXD RF
L18	MS75085-14	COIL 390UH 10% FXD RF
L19	MS75085-8	COIL 120UH 10% FXD RF
L20	MS75085-8	COIL 120UH 10% FXD RF
L23	MS75085-8	COIL 120UH 10% FXD RF
L24	MS75085-8	COIL 120UH 10% FXD RF
L25	MS75085-8	COIL 120UH 10% FXD RF
L26	MS75085-8	COIL 120UH 10% FXD RF
L28	MS75085-8	COIL 120UH 10% FXD RF
L29	MS75085-8	COIL 120UH 10% FXD RF
L30	MS75085-8	COIL 120UH 10% FXD RF
L32	MS75085-8	COIL 120UH 10% FXD RF
L33	MS75085-8	COIL 120UH 10% FXD RF
L34	MS75085-8	COIL 120UH 10% FXD RF
L36	MS75085-8	COIL 120UH 10% FXD RF
L39	MS75085-8	COIL 120UH 10% FXD RF
L40	MS75085-8	COIL 120UH 10% FXD RF
L41	MS75085-8	COIL 120UH 10% FXD RF
L42	MS75085-8	COIL 120UH 10% FXD RF
L43	MS75085-8	COIL 120UH 10% FXD RF
L44	MS75085-8	COIL 120UH 10% FXD RF
L45	MS75085-8	COIL 120UH 10% FXD RF
L46	MS75085-8	COIL 120UH 10% FXD RF
L47	MS75085-8	COIL 120UH 10% FXD RF
L48	MS75085-8	COIL 120UH 10% FXD RF
P1	10121-7292	CABLE,REMOTE/FILTER BD
P2	10121-7293	CABLE,AUDIO/FILTER BD.
P5	J46-0043-048	CONN 48 PIN
P6	J46-0043-048	CONN 48 PIN
R1	MP-1142	RES ZERO OHM (CKT JMPR)
R2	MP-1142	RES ZERO OHM (CKT JMPR)
R3	MP-1142	RES ZERO OHM (CKT JMPR)
R4	MP-1142	RES ZERO OHM (CKT JMPR)
R5	MP-1142	RES ZERO OHM (CKT JMPR)

Table 3. Filter Board Assembly A20A3 Parts List (10121-1280 Rev. C)

Ref. Desig.	Part Number	Description
C1	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C2	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C3	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C4	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C5	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C6	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C7	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C8	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C9	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C10	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C11	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C12	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C13	M39014/02-1292V	CAP 4700PF 10% 200V CER-R
C14	M39014/02-1292V	CAP 4700PF 10% 200V CER-R
C15	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C16	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C17	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C18	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C19	M39014/02-1292V	CAP 4700PF 10% 200V CER-R
C20	M39014/02-1292V	CAP 4700PF 10% 200V CER-R
C21	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C22	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C23	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C24	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C25	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C26	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C27	M39014/02-1320V	CAP .47UF 10% 50V CER-R
C29	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C30	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C31	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C32	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C33	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C35	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C36	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C37	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C38	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C39	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C40	M39014/02-1298V	CAP .01UF 10% 200V CER-R
C41	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C42	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C43	M39014/02-1320V	CAP .47UF 10% 50V CER-R
C44	M39014/02-1320V	CAP .47UF 10% 50V CER-R
C45	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C46	M39014/02-1310V	CAP .1UF 10% 100V CER-R
CR1*	1N4004	DIODE, 1A, 400V, RECT.

*CR1 is installed for ARQ and High Speed Data applications.

Table 3. Filter Board Assembly A20A3 Parts List (10121-1280 Rev. C) (Cont.)

Ref. Desig.	Part Number	Description
J1	J46-0029-048	CONN 48 PIN
J2	J46-0029-048	CONN 48 PIN
J3	J46-0022-006	HDR 6 PIN 0.100" SR LKG
L1	MS75085-8	COIL 120UH 10% FXD RF
L2	MS75085-8	COIL 120UH 10% FXD RF
L3	MS75085-8	COIL 120UH 10% FXD RF
L4	MS75085-8	COIL 120UH 10% FXD RF
L5	MS75085-8	COIL 120UH 10% FXD RF
L6	MS75085-8	COIL 120UH 10% FXD RF
L7	MS75085-8	COIL 120UH 10% FXD RF
L8	MS75085-8	COIL 120UH 10% FXD RF
L9	MS75085-8	COIL 120UH 10% FXD RF
L10	MS75085-2	COIL 39UH 10% FXD RF
L11	MS75085-2	COIL 39UH 10% FXD RF
L12	MS75085-2	COIL 39UH 10% FXD RF
L13	MS75084-15	COIL 18.0UH 10% FXD RF
L14	MS75084-15	COIL 18.0UH 10% FXD RF
L15	MS75085-8	COIL 120UH 10% FXD RF
L16	MS75085-8	COIL 120UH 10% FXD RF
L17	MS75085-8	COIL 120UH 10% FXD RF
L18	MS75085-8	COIL 120UH 10% FXD RF
L19	MS75084-15	COIL 18.0UH 10% FXD RF
L20	MS75084-15	COIL 18.0UH 10% FXD RF
L21	MS75085-8	COIL 120UH 10% FXD RF
L22	MS75085-2	COIL 39UH 10% FXD RF
L23	MS75085-2	COIL 39UH 10% FXD RF
L24	MS75085-2	COIL 39UH 10% FXD RF
L25	MS75085-2	COIL 39UH 10% FXD RF
L26	MS75085-8	COIL 120UH 10% FXD RF
L27	MS75085-7	COIL 100UH 10% FXD RF
L29	MS75085-2	COIL 39UH 10% FXD RF
L30	MS75085-8	COIL 120UH 10% FXD RF
L31	MS75085-8	COIL 120UH 10% FXD RF
L32	MS75085-2	COIL 39UH 10% FXD RF
L33	MS75085-2	COIL 39UH 10% FXD RF
L35	MS75085-2	COIL 39UH 10% FXD RF
L36	MS75085-8	COIL 120UH 10% FXD RF
L37	MS75085-8	COIL 120UH 10% FXD RF
L38	MS75085-2	COIL 39UH 10% FXD RF
L39	MS75085-8	COIL 120UH 10% FXD RF
L40	MS75085-8	COIL 120UH 10% FXD RF
L41	MS75085-2	COIL 39UH 10% FXD RF

Table 3. Filter Board Assembly A20A3 Parts List (10121-1280 Rev. C) (Cont.)

Ref. Desig.	Part Number	Description
L42	MS75085-8	COIL 120UH 10% FXD RF
L43	MS75085-7	COIL 100UH 10% FXD RF
L44	MS75085-8	COIL 120UH 10% FXD RF
L45	MS75085-8	COIL 120UH 10% FXD RF
L46	MS75085-2	COIL 39UH 10% FXD RF
P3	10121-7290	CABLE,CONTROL/FILTER
P4	10121-7291	CABLE,FILTER/SYS INTERFCE

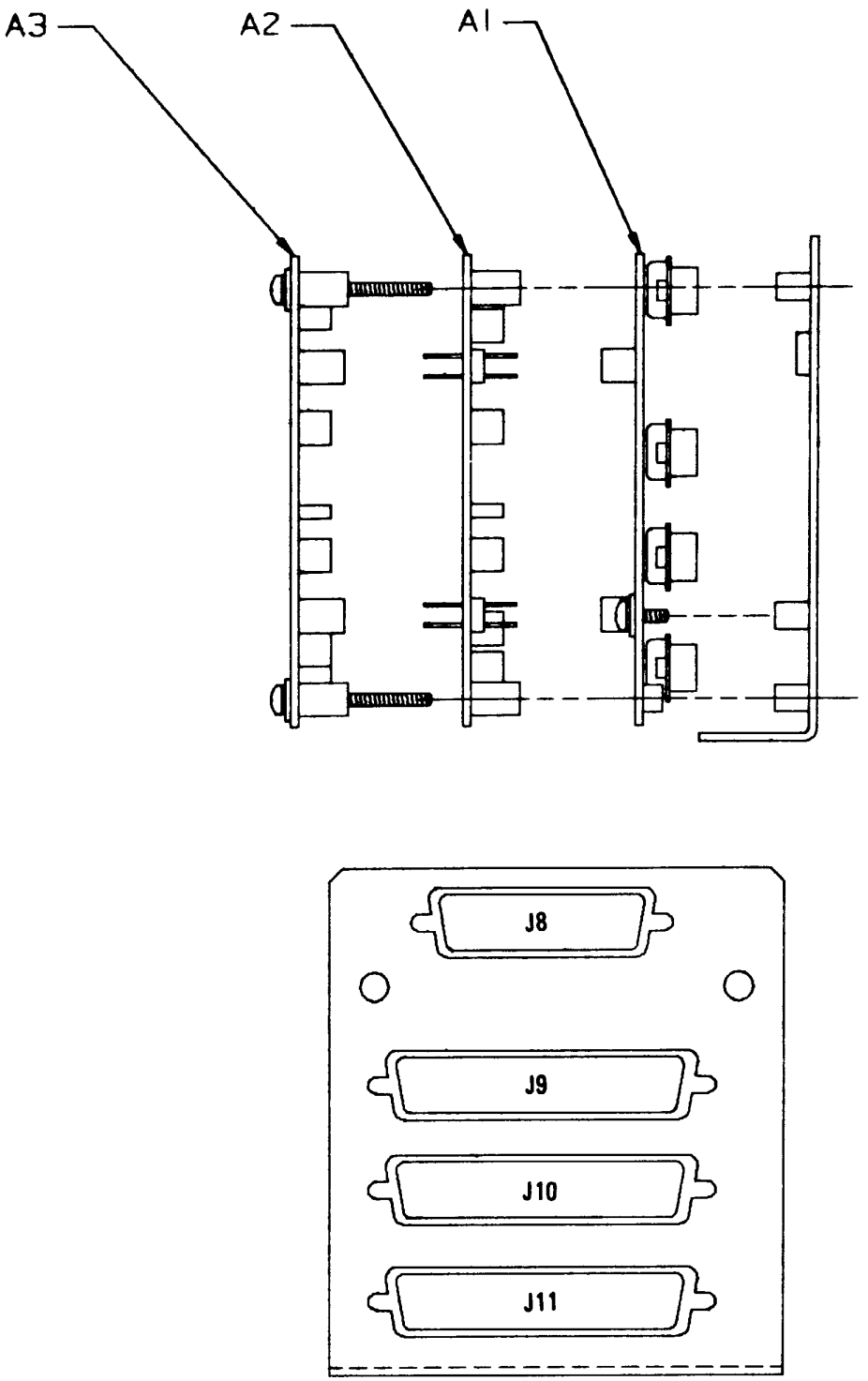


Figure 1. Filter Board Assembly A20 Subassembly Location Diagram (10121-1250 Rev. C)

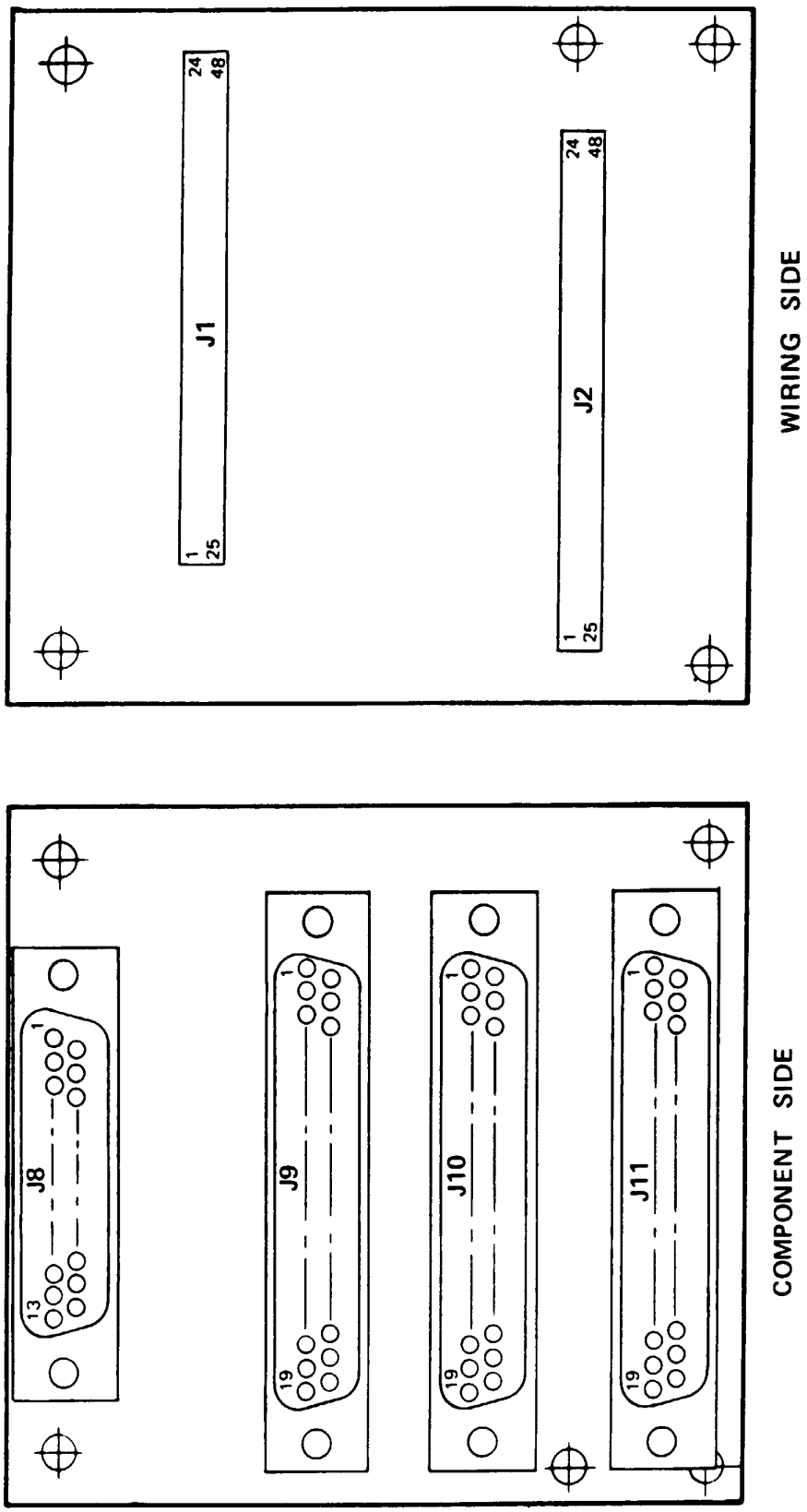


Figure 2. Filter Board Assembly A20A1 Component Location Diagram (10121-1260 Rev. C)

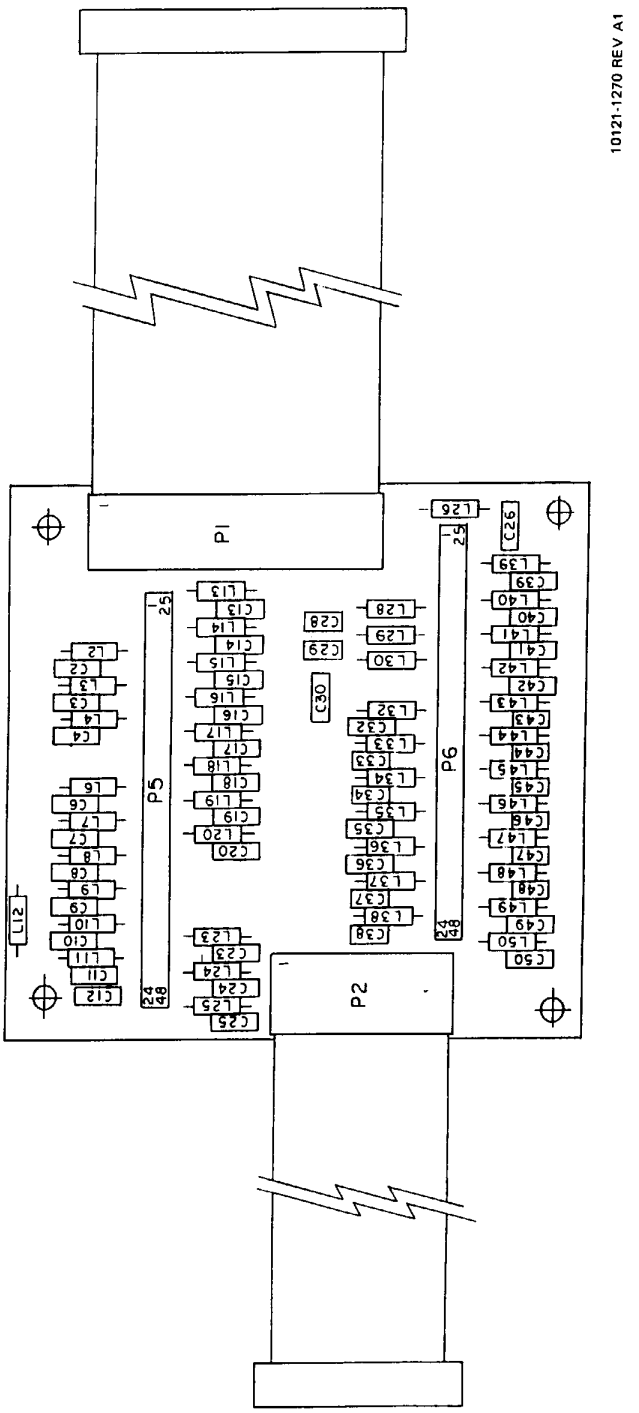
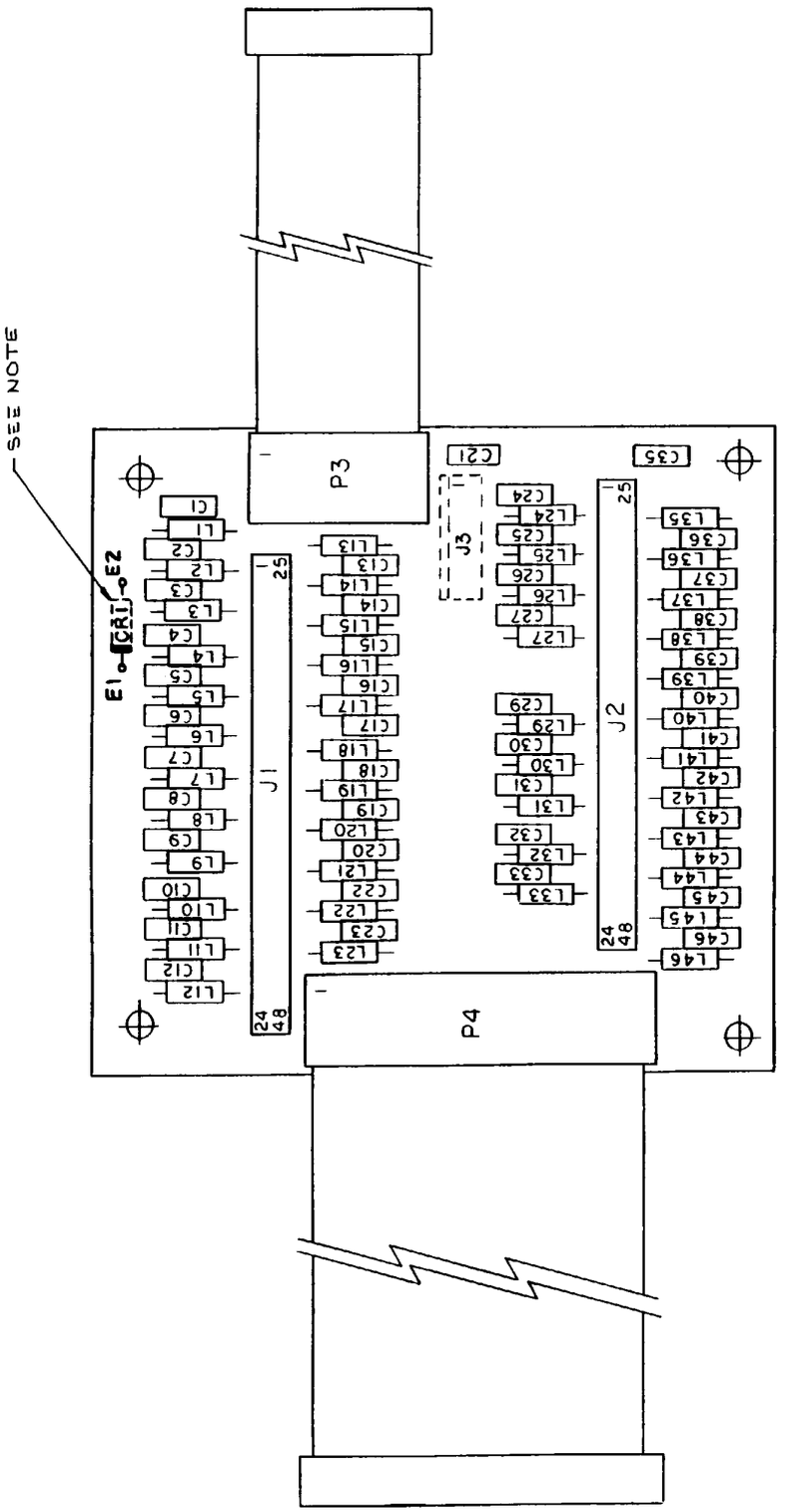


Figure 3. Filter Board Assembly A20A2 Component Location Diagram (10121-1270 Rev. B)



NOTE:
CR1 IS INSTALLED, FARSIDE, FOR ARQ AND HIGH SPEED DATA APPLICATIONS

Figure 4. Filter Board Assembly A20A3 Component Location Diagram (10121-1280 Rev. B)

A23
+24-VOLT POWER SUPPLY ASSEMBLY

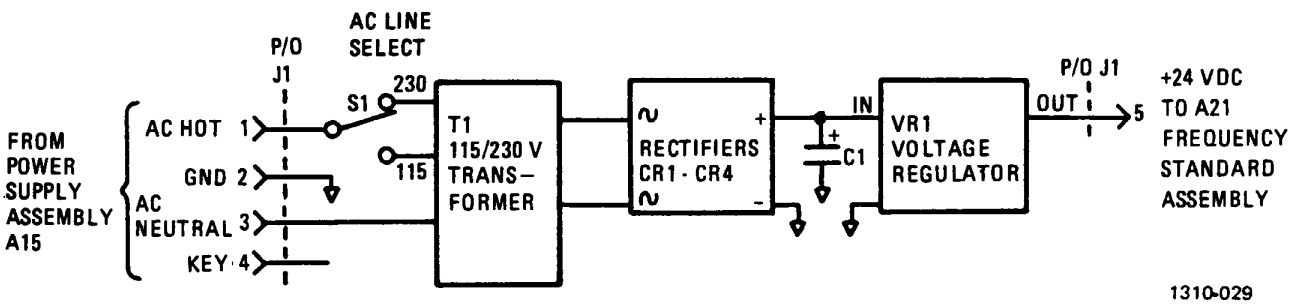


TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

+ 24-VOLT POWER SUPPLY ASSEMBLY A23

WARNING

115 Vac or 230 Vac is applied to the A23 assembly whenever the exciter ac input line cord is connected to an ac source, regardless of the exciter ON/OFF power switch setting.

Do not attempt to remove this assembly or replace its input line fuse until the exciter ac power line cord is disconnected. Setting the ON/OFF power switch to OFF is insufficient to prevent a shock hazard.

Be certain that the protective cover over J1's mating connector is properly installed, since 115/230 Vac is present on that connector.

See paragraph 1 for 115/230 Vac selection and/or fuse replacement instructions.

1. GENERAL DESCRIPTION

Power Supply Assembly A23 provides + 24 Vdc at up to 300 mA to power the Frequency Standard Assembly A21. Figure 1 shows the position of Power Supply Assembly A23 in the chassis.

Ac input to this assembly comes directly from the exciter ac input connector that is part of Power Supply Assembly A15 line filter FL1. The power is tapped off before the exciter main fuse and power ON/OFF switch. Ac voltage is present at the assembly's input at all times when the exciter is plugged in. Frequency Standard Assembly A21 will always receive + 24 Vdc power, and remain constantly on, even when the exciter ON/OFF power switch is OFF. Frequency standard warm up and setting times are eliminated.

Switch S1 allows selection of 115 Vac or 230 Vac. An in-line fuse located in main Power Supply Assembly A15 must be changed when operating at 115 Vac, 230 Vac, or when replacing a blown fuse.

To select 115 Vac, 230 Vac, and/or replace fuse, follow the procedure listed below:

a. Disconnect exciter ac line cord.

b. Select desired ac line voltage to A23 Assembly with A23 switch S1 (115 Vac or 230 Vac), if not already selected.

c. Remove top cover of main Power Supply Assembly A15.

d. Locate the A15 assembly in line fuseholder W4F1.

e. Replace fuse as follows:

   1. For 115 Vac operation, use 1/4 ampere, 125 Vac slow-blow fuse.

   2. For 230 Vac operation, use 1/8 ampere, 250 Vac slow-blow fuse.

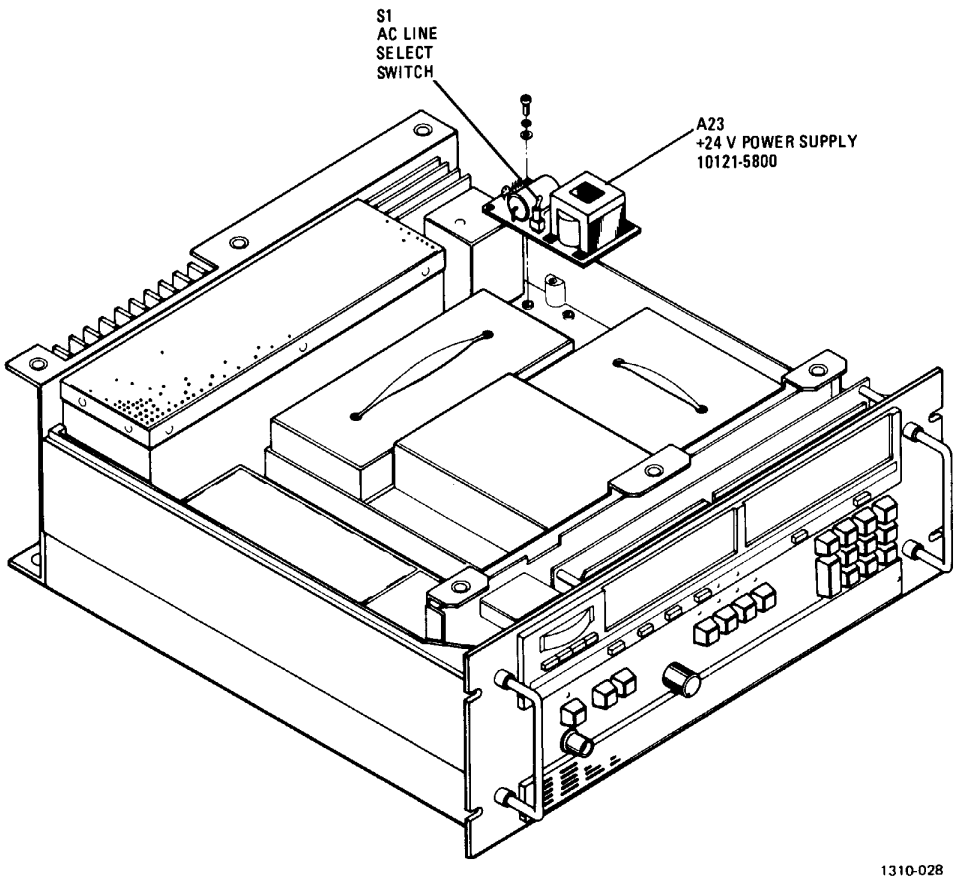


Figure 1. Power Supply Assembly A23 Location

f. Replace the A15 assembly cover and hardware.

g. Select desired ac line voltage to main Power Supply Assembly A15 (same value as step b), if not already selected. This is accomplished via respositioning the pc card and using the correct fuse in A15 assembly line filter FL1. Refer to subsection A15 of this manual.

h. Reconnect exciter ac line cord. Ac power will now be applied to the A23 assembly, regardless of the exciter ON/OFF switch position. Power for the rest of the exciter will be applied when the ON/OFF switch is set to ON.

2. INTERFACE CONNECTIONS

Table 1 details the various input/output connections and other relevant data.

Table 1. Power Supply Assembly A23 Interface Interconnections

Connector	Function	Characteristics
J1-1	Ac Hot	115 Vac or 220 Vac
J1-2	Ground	
J1-3	Ac Neutral	
J1-4	Index Key	Not used
J1-5	Dc Power	+ 24 Vdc at 300 mA maximum

3.CIRCUIT DESCRIPTIONS

Ac line voltage from J1 is supplied to ac line select switch S1 prior to application to the primary of transformer. The voltage across the T1 secondary is 28 V_{rms} under nominal line voltage. The ac signal is rectified by CR1 through CR4 to produce approximately 34 Vdc across filter capacitor C1. Voltage regulator VR1 regulates the output voltage to + 24 Vdc, over a wide range of ac line input voltages.

Note that generally, the full 300 mA capability is required only until the Frequency Standard Assembly has warmed up and stabilized. After that, current draw typically falls to about one-third of its warmup value of approximately 100 mA.

4. MAINTENANCE

4.1 General Information

In order to remove the A23 assembly for servicing:

a. Disconnect the exciter ac line cord.

b. Disconnect the J1 mating connector.

c. Remove the assembly's four mounting screws and heatsink block screw.

See paragraph 1, General Description, for replacement of fuses and/or 115/230 Vac line input selection.

WARNING

The heatsink block under VR1 should be secured to the chassis (or similar heatsink) whenever power is applied to the A23 assembly.

4.2 Output Voltage Test

a. Disconnect exciter ac line cord, and disconnect Reference Generator Assembly A12 connector J8.

b. Connect an 80-ohm, 7.5 watt (minimum) load to J1-5. At 24 Vdc output, the supply will then deliver 300 mA.

c. Configure FL1, A23 assembly, and fuses for 115 Vac as described in paragraph 1. Plug exciter into 115 Vac source.

d. With ac power applied, A23 assembly output should be 24 Vdc.

e. Configure FL1, A23 assembly, and fuses for 230 Vac as described in paragraph 1. Plug exciter into 230 Vac source.

f. With ac power applied, the output should be 24 Vdc.

g. Disconnect line cord, reconfigure FL1, A23 assembly, and fuses to desired operational input ac level.

h. Reconnect A12 J8 connector.

i. Test is now complete.

5. PARTS LIST, COMPONENT LOCATIONS, AND SCHEMATIC DIAGRAM

All replaceable components of Power Supply Assembly A23 are listed in table 2. Component locations are shown in figure 2. The schematic is shown in figure 3.

Table 2. Power Supply Assembly A23 Parts List (10121-5800 Rev. L)

Ref. Desig.	Part Number	Description
8	10121-5804	SHIELD, POWER SUPPLY
11	M10-0006-000	WSHR, SHLDR NYLON
12	M08-0001-051	INSL RUBBR/PLSTIC FOR XSTR
C1	C17-0063-521	CAP 520UF 63V ELEC
C2	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C3	M39014/02-1310V	CAP .1UF 10% 100V CER-R
C4	C26-0050-159	CAP 1.5UF 20% 50V TANT
CR1 – CR4	1N4007	DIODE 1A 1000V RECT GP
J1	J46-0022-005	HDR 5 PIN 0.100" SR LKG
R1	RN55D4421F	RES 4420 1% 1/8W MET FLM
R2	RN55D2430F	RES 243 1% 1/8W MET FLM
R3	R65-0003-472	RES 4.7K 5% 1/4W CAR FILM
S1	S10-0011-111	SW SP ON-NONE-ON TOG PCMT
T1	T40-0003-001	TRANSFORMER
VR1	IC-0358	IC VR 317 ADJ V 1.5A

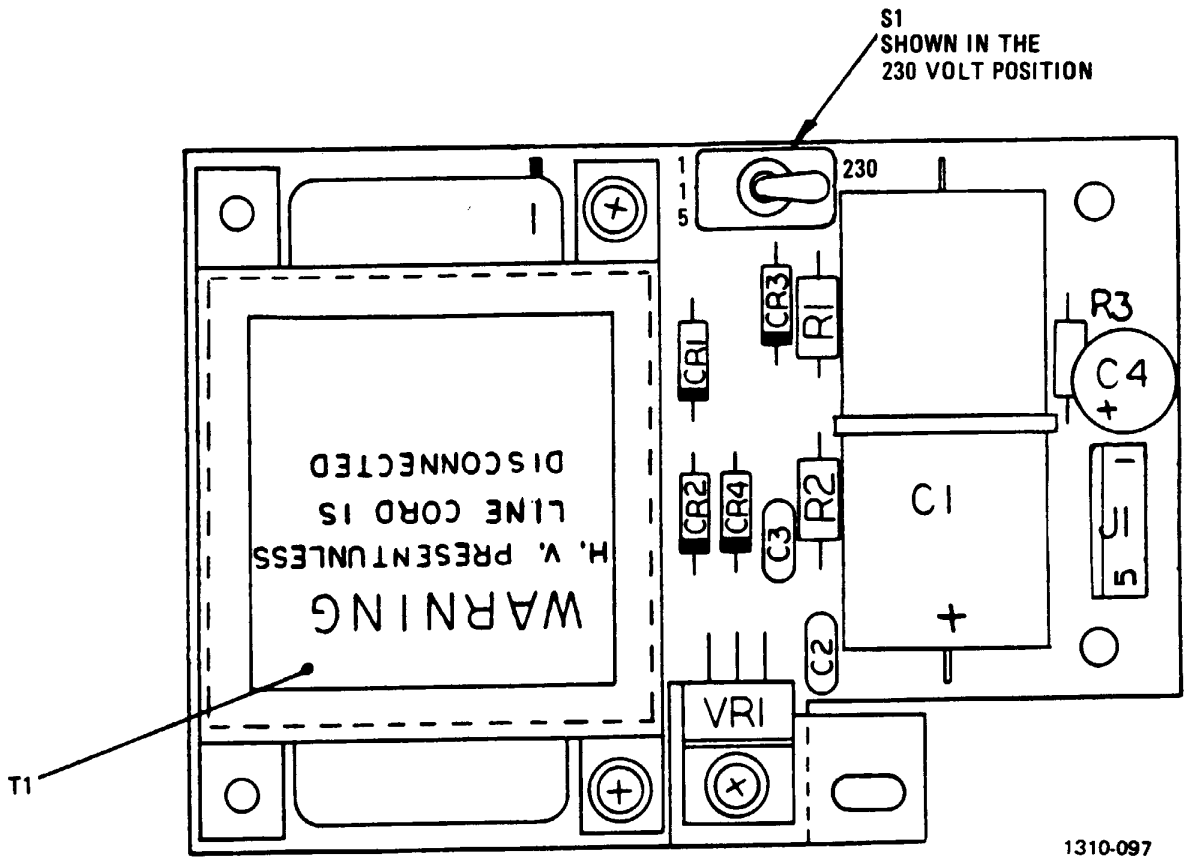


Figure 2. Power Supply Assembly A23 Component Location Diagram (10121-5800 Rev. E)

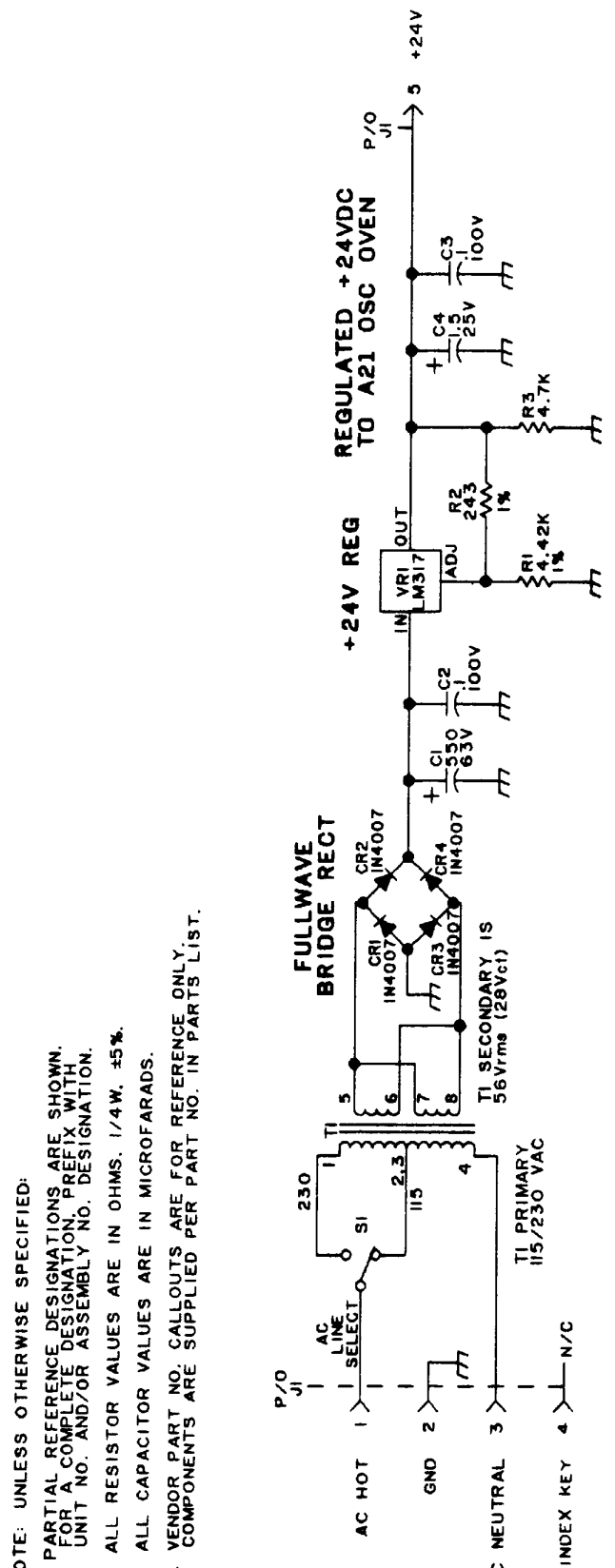


Figure 3. Power Supply Assembly A23 Schematic Diagram (10121-5801 Rev. A)

APPENDIX

DATA SHEETS

Data sheets are listed in alphanumeric order in table A-1.

Table A-1. Data Sheets

Table A-1. Data Sheets (Cont.)

Type	Description	Page
MC12013	Two-Modulus Prescaler	A-23
MC145156	Serial Input PLL Frequency Synthesizer	A-24
MC145406	RS-232-C/V.28 Driver/Receiver	A-25
MC14585B	CMOS MSI (Low Power Complementary MOS) 4-Bit Magnitude Comparator	A-26
MC1458	Dual Operational Amplifier Silicon Monolithic Integrated Circuit	A-27
MC1496	Balanced Modulator - Demodulator Silicon Monolithic Integrated Circuit	A-27
MC3358	Dual Differential Input Operational Amplifiers Silicon Monolithic Integrated Circuit	A-28
MC7800C, AC	Series Three-Terminal Positive Voltage Regulators	A-29
MC7900C	Series Three-Terminal Negative Voltage Regulators	A-30
MCT6	Dual Phototransistor Optoisolators	A-31
MM54C02/ MM74C02	Quad 2-Input NOR Gate	A-32
MM74C14	Hex Schmitt Trigger	A-32
MM74C373	Octal Latch	A-32
NE-SA594	Vacuum Fluorescent Display Driver	A-33
SAY-1	Super High Level (+ 23 dBm LO) Double-Balanced Mixers	A-34
SBL-1	Standard Level (+ 7 dBm LO) Double-Balanced Mixers	A-35
SCN2681	Dual Universal Asynchronous Receiver/Transmitter (DUART)	A-36
SN74165	Parallel-Load 8-Bit Shift Registers	A-38
SN74L90	Decade, Divide-by-Twelve, and Binary Counter	A-38
SN54LS/ 74LS92	Decade Counter; Divide-by-Twelve Counter; 4-Bit Binary Counter Low Power Schottky	A-39
SN54LS/ 74LS393	Dual Decade Counter; Dual 4-Stage Binary Counter Low Power Schottky	A-40
SN54LS151/ SN74LS151	8-Input Multiplexer Low Power Schottky	A-41
SN54LS02/ SN74LS02	Quad 2-Input NOR Gate Low Power Schottky	A-42
SN54LS04/ SN74LS04	Hex Inverter Low Power Schottky	A-42
SN54LS32/ SN74LS32	Quad 2-Input OR Gate Low Power Schottky	A-42
SN54LS139/ SN74LS139	Dual 1-of-4 Decoder/Demultiplexer Low Power Schottky	A-43
SN54LS245/ SN74LS245	Octal Bus Transceiver Low Power Schottky	A-44
SN74LS42	4-Line-to-10-Line Decoders (1-of-10)	A-44

Table A-1. Data Sheets

AD7523
8-BIT MONOLITHIC
MULTIPLYING D/A CONVERTERS

FEATURES

- **8, 9 and 10 bit linearity**
- **Low gain and linearity Tempcos**
- **Full temperature range operation**
- **Full input static protection**
- **DTL/TTL/CMOS compatible**
- **+5 to +15 volts supply range**
- **Fast settling time: 100 nS**
- **Four quadrant multiplication**
- **883B Processed versions available**

GENERAL DESCRIPTION

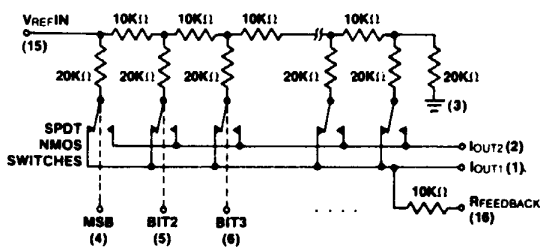
The Intersil AD7523 is a monolithic, low cost, high performance, 10 bit accurate, multiplying digital-to-analog converter (DAC), in a 16-pin DIP.

Intersil's thin-film resistors on CMOS circuitry provide 8-bit resolution (8, 9 and 10-bit accuracy), with DTL/TTL/CMOS compatible operation.

Intersil AD7523's accurate four quadrant multiplication, full military temperature range operation, full input protection from damage due to static discharge by clamps to V+ and GND and very low power dissipation make it a very versatile converter.

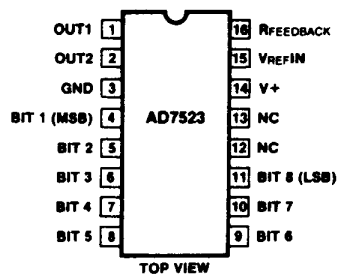
Low noise audio gain control, motor speed control, digitally controlled gain and attenuators are a few of the wide number of applications of the 7523.

FUNCTIONAL DIAGRAM



(Switches shown for Digital Inputs "High")

PIN CONFIGURATION



TOP VIEW

OUTLINE DRAWINGS
DE,PE

ADC0801 – ADC0804
8-BIT MICROPROCESSOR COMPATIBLE A/D CONVERTERS

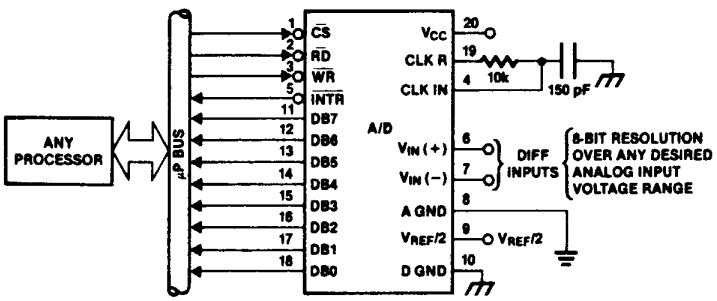
GENERAL DESCRIPTION

The ADC0801 family are CMOS 8-bit successive approximation A/D converters which use a modified potentiometric ladder, and are designed to operate with the 8080A control bus via three-state outputs. These converters appear to the processor as memory locations or I/O ports, hence no interfacing is required.

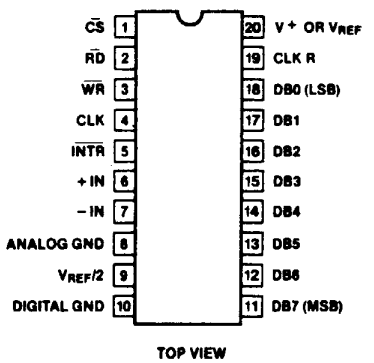
A differential analog voltage input allows increasing the common-mode-rejection and offsetting the analog zero input voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8 bits of resolution.

The ADC0801 family is available in the industry standard 20 pin CERDIP packages.

TYPICAL APPLICATION



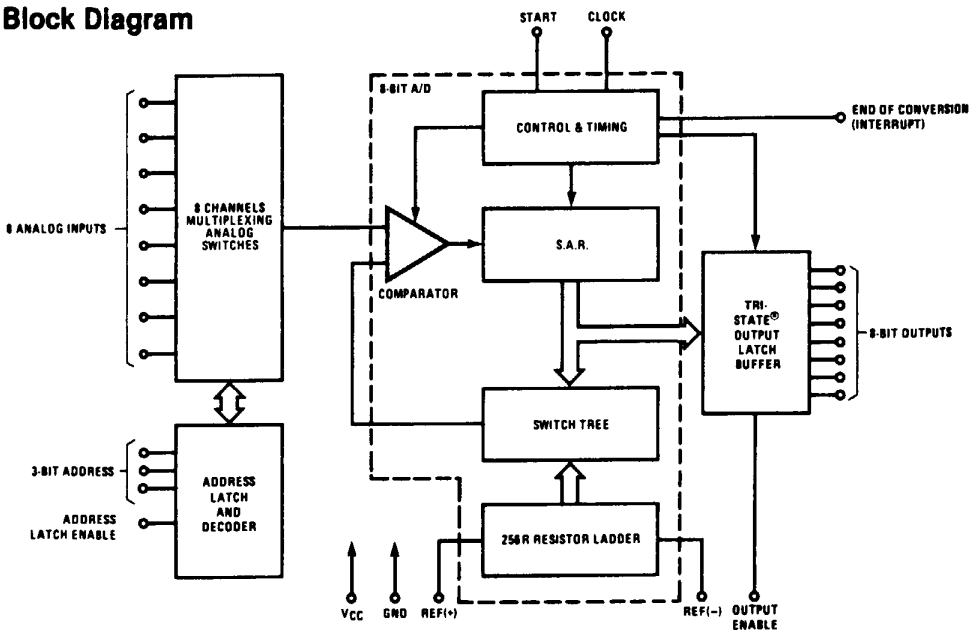
PIN CONFIGURATION



TOP VIEW

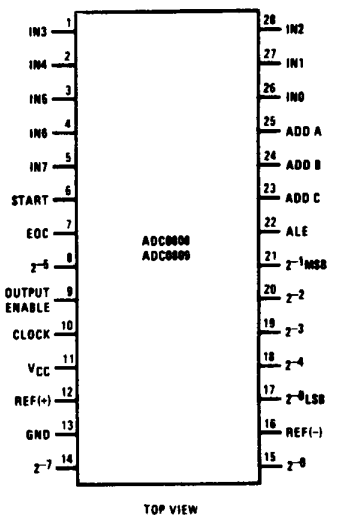
ADC0809
8-BIT uP COMPATIBLE AD/ CONVERTERS WITH 8-CHANNEL MULTIPLEXER

Block Diagram



SELECTED ANALOG CHANNEL	ADDRESS LINE		
	C	B	A
IN0	L	L	L
IN1	L	L	H
IN2	L	H	L
IN3	L	H	H
IN4	H	L	L
IN5	H	L	H
IN6	H	H	L
IN7	H	H	H

Dual-In-Line Package



TOP VIEW

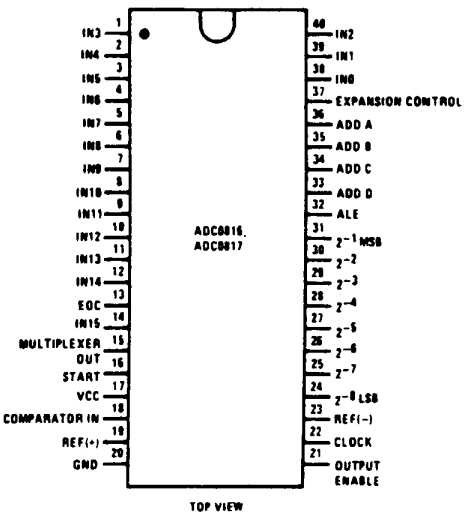
ADC0817
8-BIT uP COMPATIBLE A/D CONVERTERS WITH 16-CHANNEL MULTIPLEXER

General Description

The ADC0816, ADC0817 data acquisition component is a monolithic CMOS device with an 8-bit analog-to-digital converter, 16-channel multiplexer and microprocessor compatible control logic. The 8-bit A/D converter uses successive approximation as the conversion technique. The converter features a high impedance chopper stabilized comparator, a 256R voltage divider with analog switch tree and a successive approximation register. The 16-channel multiplexer can directly access any one of 16-single-ended analog signals, and provides the logic for additional channel expansion. Signal conditioning of any analog input signal is eased by direct access to the multiplexer output, and to the input of the 8-bit A/D converter.

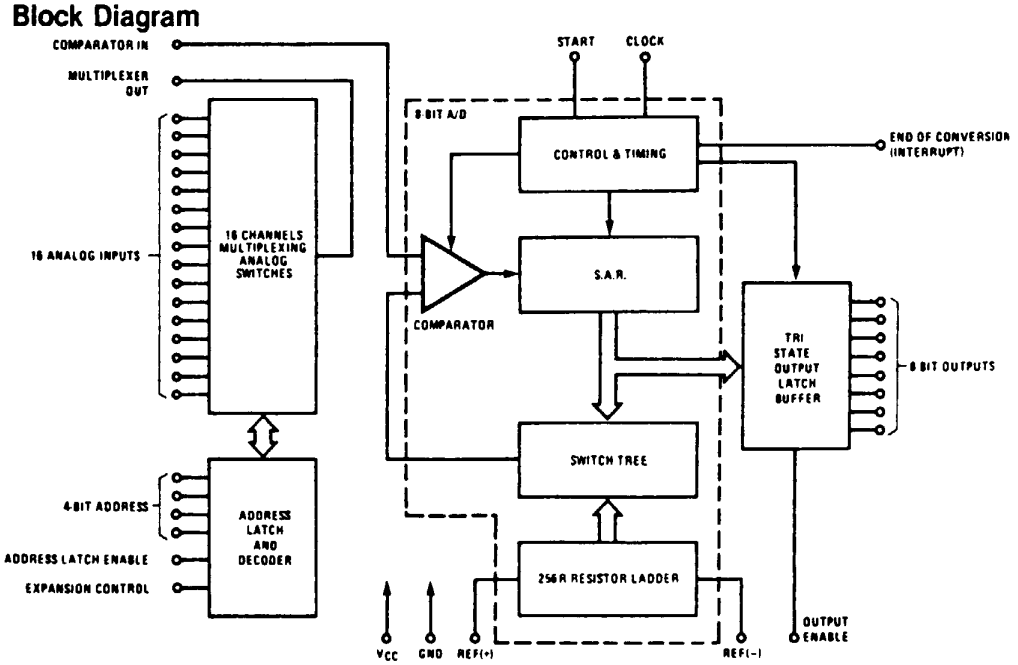
The device eliminates the need for external zero and full-scale adjustments. Easy interfacing to microprocessors is provided by the latched and decoded multiplexer address inputs and latched TTL TRI-STATE® outputs.

Dual-In-Line Package



TOP VIEW

Block Diagram



CA3083
GENERAL-PURPOSE HIGH-CURRENT N-P-N TRANSISTOR ARRAY

RCA-CA3083 is a versatile array of five high-current (to 100mA) n-p-n transistors on a common monolithic substrate. In addition, two of these transistors (Q1 and Q2) are matched at low currents (i.e. 1mA) for applications in which offset parameters are of special importance.

Independent connections for each transistor plus a separate terminal for the substrate permit maximum flexibility in circuit design. The CA3083 is supplied in a 16-lead dual-in-line plastic package, and the CA3083F in a 16-lead dual-in-line frit-seal ceramic package.

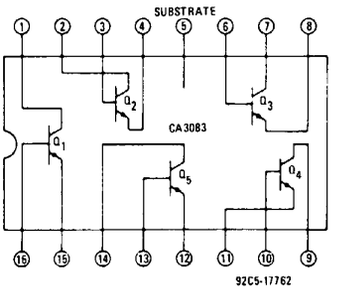
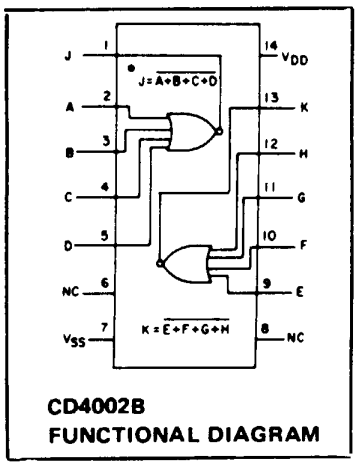


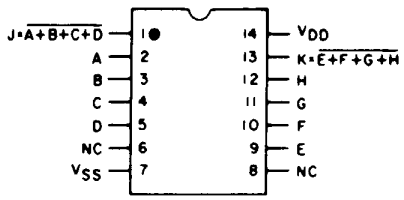
FIG. 1 – FUNCTIONAL DIAGRAM OF THE CA3083

CD4002B TYPES
COS/MOS NOR GATES



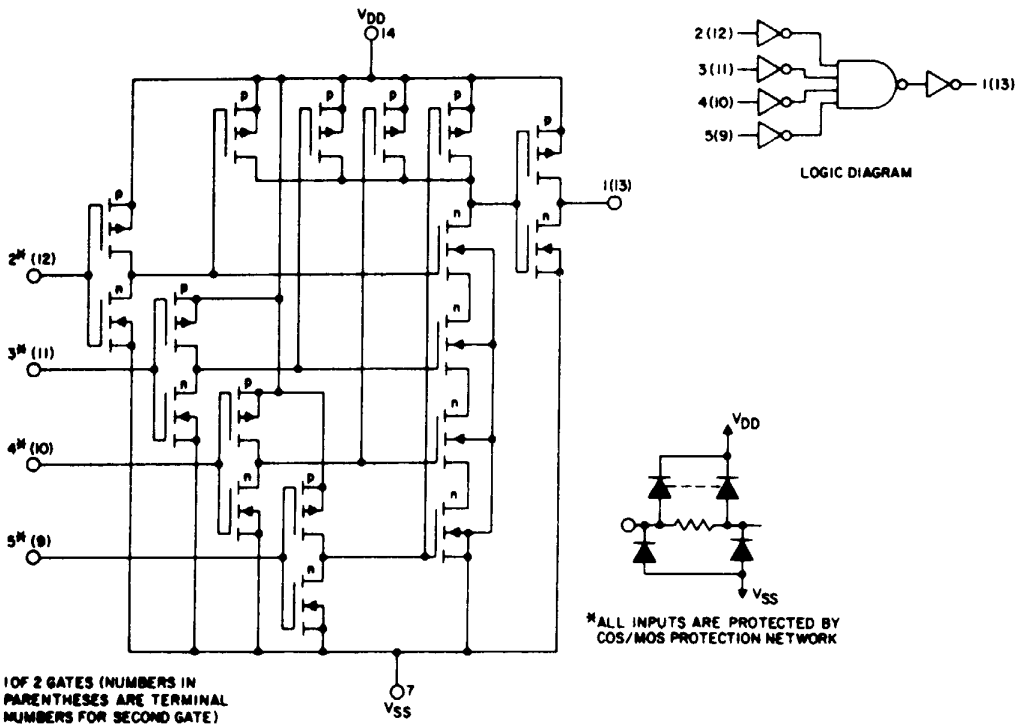
CD4002B
FUNCTIONAL DIAGRAM

TERMINAL ASSIGNMENTS (TOP VIEW)



NC = NO CONNECTION

CD4002B



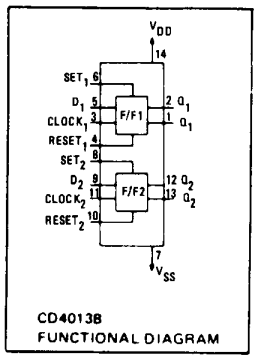
Schematic and logic diagrams for CD4002B.

CD4013B TYPES
COS/MOS DUAL
'D'-TYPE FLIP-FLOP

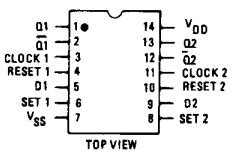
High-Voltage Types (20-Volt Rating)

The RCA-CD4013B consists of two identical, independent data-type flip-flops. Each flip-flop has independent data, set, reset, and clock inputs and Q and $\overline{Q}$ outputs. These devices can be used for shift register applications, and, by connecting $\overline{Q}$ output to the data input, for counter and toggle applications. The logic level present at the D input is transferred to the Q output during the positive-going transition of the clock pulse. Setting or resetting is independent of the clock and is accomplished by a high level on the set or reset line, respectively.

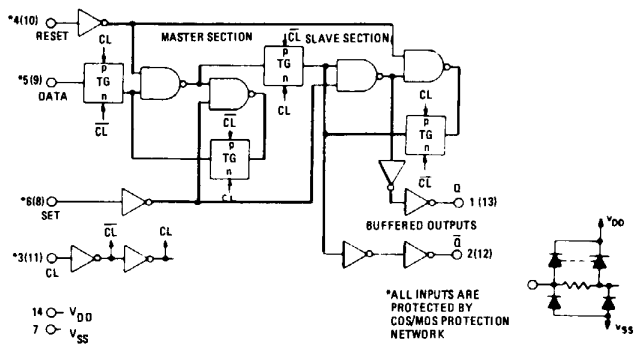
The CD4013B types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).



CD4013B
FUNCTIONAL DIAGRAM

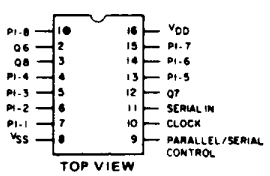


TERMINAL ASSIGNMENT

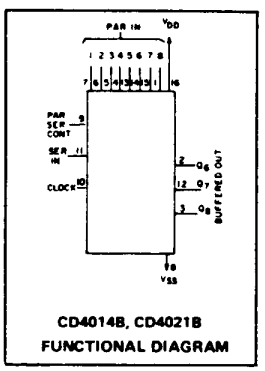


CD4021B TYPE
COS/MOS 8-STAGE
STATIC SHIFT REGISTERS

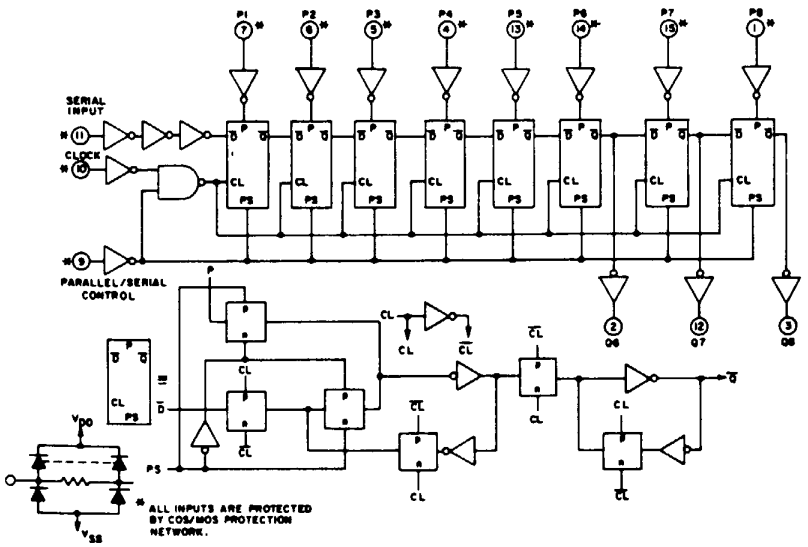
Asynchronous Parallel Input or
Synchronous Serial Input/Serial Output



TERMINAL DIAGRAM



CD4014B, CD4021B
FUNCTIONAL DIAGRAM

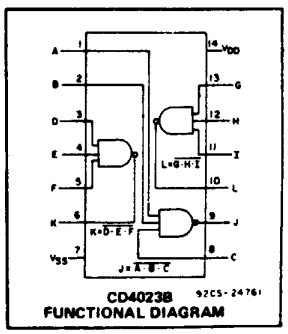


TRUTH TABLE – CD4021B

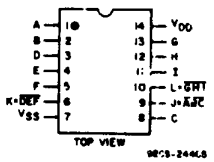
CL	Serial Input	Parallel/ Serial Control	P1-1	P1-n	Q1 (internal)	Qn
X	X	1	0	0	0	0
X	X	1	0	1	0	1
X	X	1	1	0	1	0
X	X	1	1	1	1	1
↑	0	0	X	X	0	Qn-1
↑	1	0	X	X	1	Qn-1
↓	X	0	X	X	Q1	Qn

X - DON'T CARE CASE

CD4023B TYPES
COS/MOS NAND GATES
TRIPLE 3 INPUT



FUNCTIONAL DIAGRAM



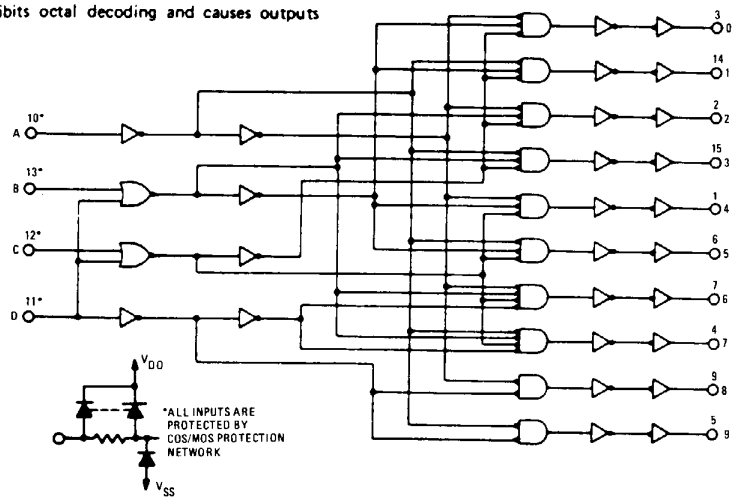
CD4023B

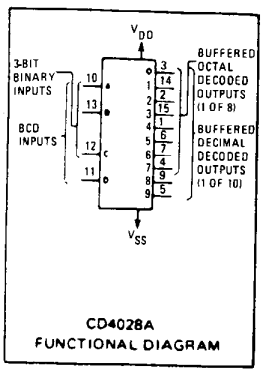
TERMINAL ASSIGNMENTS

CD4028A TYPES
COS/MOS
BCD-TO-DECIMAL DECODER

The RCA-CD4028A types are BCD-to-decimal or binary-to-octal decoders consisting of pulse-shaping circuits on all 4 inputs, decoding-logic gates, and 10 output buffers. A BCD code applied to the four inputs, A to D, results in a high level at the selected one of 10 decimal decoded outputs. Similarly, a 3-bit binary code applied to inputs A through C is decoded in octal code at output 0 to 7. A high-level signal at the D input inhibits octal decoding and causes outputs 0 through 7 to go low. If unused, the D input must be connected to V_{SS}. High drive capability is provided at all outputs to enhance dc and dynamic performance in high fan-out applications.

These types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), and in chip form (H suffix).





CD4028A
FUNCTIONAL DIAGRAM

TABLE I – TRUTH TABLE

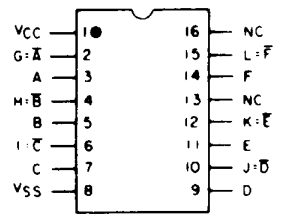
D	C	B	A	0	1	2	3	4	5	6	7	8	9	
0	0	0	0	1	0	0	0	0	0	0	0	0	0	*
0	0	0	1	0	1	0	0	0	0	0	0	0	0	
0	0	1	0	0	0	1	0	0	0	0	0	0	0	
0	0	1	1	0	0	0	1	0	0	0	0	0	0	
0	1	0	0	0	0	0	0	1	0	0	0	0	0	
0	1	0	1	0	0	0	0	0	1	0	0	0	0	
0	1	1	0	0	0	0	0	0	0	1	0	0	0	
0	1	1	1	0	0	0	0	0	0	0	1	0	0	
1	0	0	0	0	0	0	0	0	0	0	0	1	0	
1	0	0	1	0	0	0	0	0	0	0	0	0	1	
1	0	1	0	0	0	0	0	0	0	0	0	1	0	**
1	0	1	1	0	0	0	0	0	0	0	0	0	1	
1	1	0	0	0	0	0	0	0	0	0	0	1	0	
1	1	0	1	0	0	0	0	0	0	0	0	0	1	
1	1	1	0	0	0	0	0	0	0	0	0	1	0	
1	1	1	1	0	0	0	0	0	0	0	0	0	1	

* WHERE 1 = HIGH LEVEL
0 = LOW LEVEL

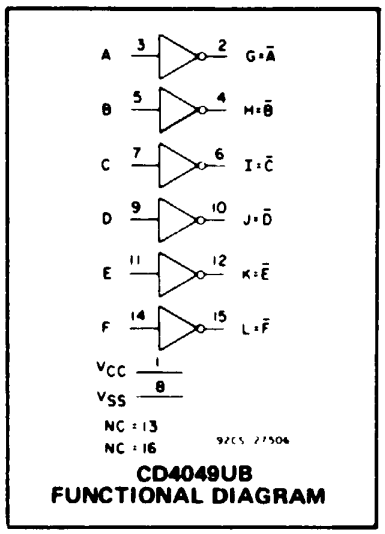
** EXTRAORDINARY STATES

CD4049B TYPE
INVERTING
COS/MOS HEX BUFFER/CONVERTER

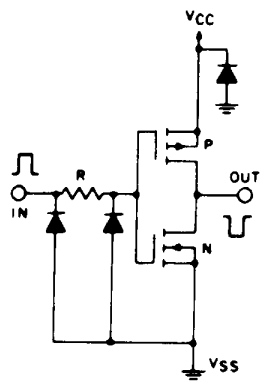
TERMINAL ASSIGNMENTS



NC = NO CONNECTION 92CS-24480RI



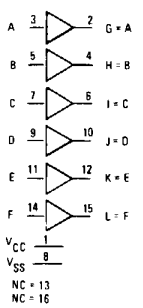
CD4049UB
FUNCTIONAL DIAGRAM



Schematic diagram of CD4049UB, 1 of 6 identical units

CD4050A
COS/MOS HEX BUFFER/CONVERTERS

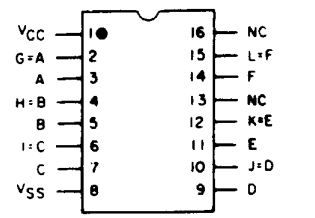
The CD4049A and CD4050A are inverting and non-inverting hex buffers, respectively, and feature logic-level conversion using only one supply voltage (V_{CC}). The input-signal high level (V_{IH}) can exceed the V_{CC} supply voltage when these devices are used for logic-level conversions. These devices are intended for use as COS MOS to DTL, TTL converters and can drive directly two DTL/TTL loads. (V_{CC}=5 V, $V_{OL} \geq$0.4 V, and $I_{ON} \geq$3.2 mA.)



CD4050A

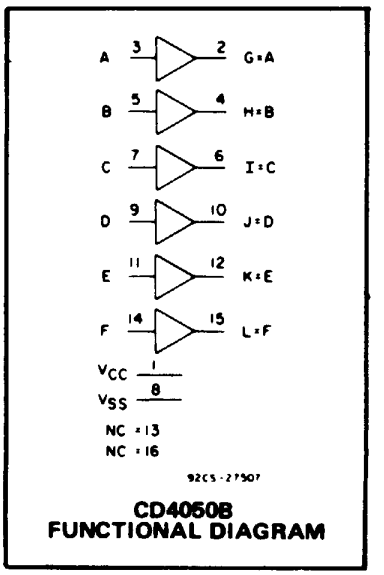
CD4050B TYPES
COS/MOS HEX BUFFER/CONVERTERS

TERMINAL ASSIGNMENTS

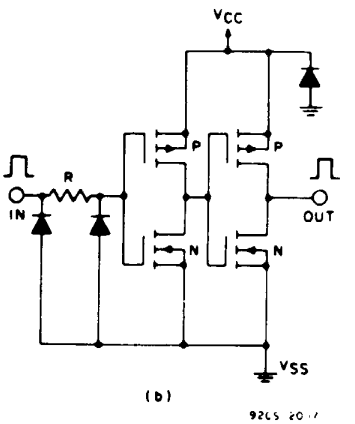


NC = NO CONNECTION 92CS-24481R1

CD4050B

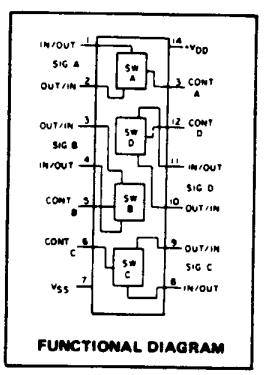


CD4050B
FUNCTIONAL DIAGRAM



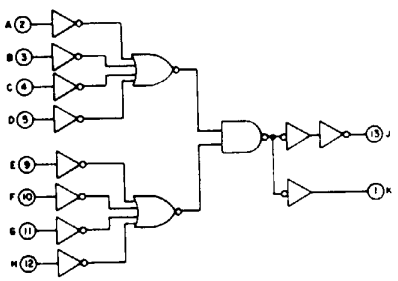
CD4066B TYPES
COS/MOS QUAD BILATERAL SWITCH
(For transmission or multiplexing of Analog or Digital Signals)

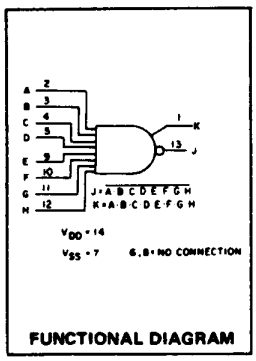
The CD4066B consists of four independent bilateral switches. A single control signal is required per switch. Both the p and the n device in a given switch are biased on or off simultaneously by the control signal. The well of the n-channel device on each switch is either tied to the input when the switch is on or to V_{SS} when the switch is off. This configuration eliminates the variation of the switch-transistor threshold voltage with input signal, and thus keeps the on-state resistance low over the full operating-signal range.

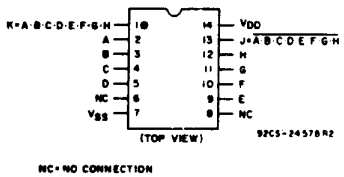


FUNCTIONAL DIAGRAM

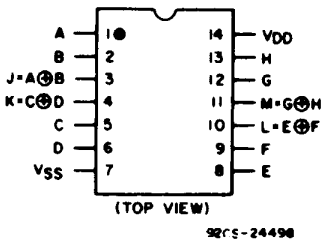
CD4068B TYPES
COS/MOS 8-INPUT
NAND/AND GATE



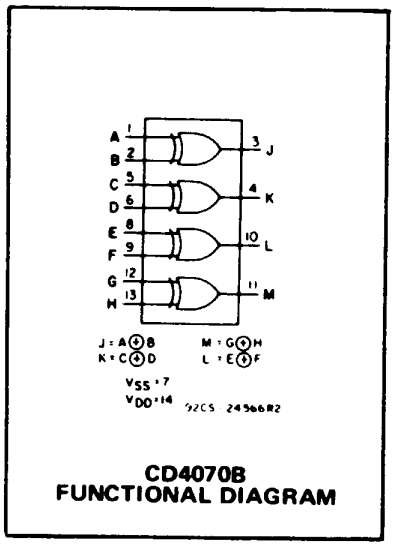


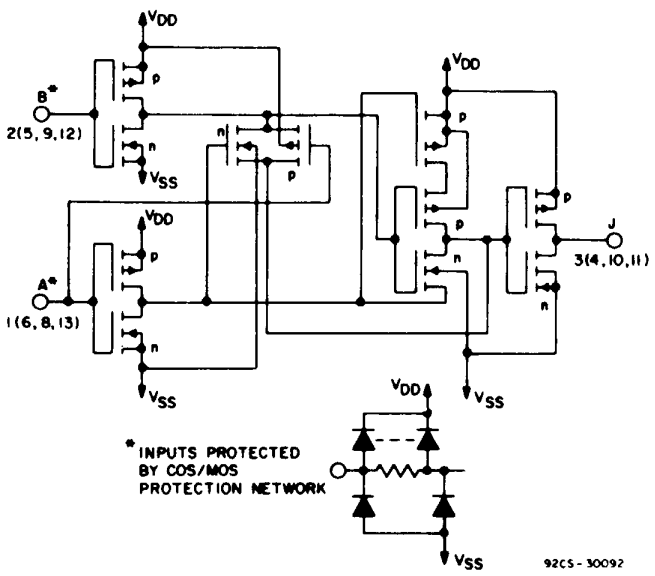


CD4070B TYPES
COS/MOS QUAD EXCLUSIVE–OR AND
EXCLUSIVE–NOR GATES



TERMINAL ASSIGNMENT
CD4070B





TRUTH TABLE CD4070B
1 of 4 Gates

A	B	J
0	0	0
1	0	1
0	1	1
1	1	0

1 = HIGH LEVEL
0 = LOW LEVEL
J = A ⊕ B

Fig. 1 – Schematic diagram for CD4070B (1 of 4 identical gates).

CD4094B
COS/MOS
8-STAGE SHIFT-AND-STORE BUS REGISTER

High-Voltage Types (20-Volt Rating)

The RCA-CD4094B is an 8-stage serial shift register having a storage latch associated with each stage for strobing data from the serial input to parallel buffered 3-state outputs. The parallel outputs may be connected directly to common bus lines. Data is shifted on positive clock transitions. The data in each shift register stage is transferred to the storage register when the STROBE input is high. Data in the storage register appears at the outputs whenever the OUTPUT-ENABLE signal is high.

Two serial outputs are available for cascading a number of CD4094B devices. Data is available at the Q_S serial output terminal on positive clock edges to allow for high-speed operation in cascaded systems in which the clock rise time is fast. The same serial information, available at the Q'_S terminal on the next negative clock edge, provides a means for cascading CD4094B devices when the clock rise time is slow.

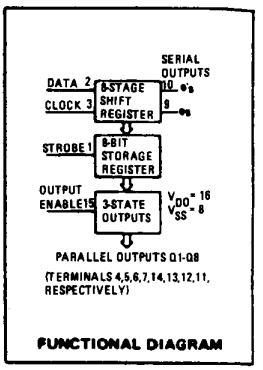
TRUTH TABLE

CL▲	OUTPUT ENABLE	STROBE	DATA	PARALLEL OUTPUTS Q1	PARALLEL OUTPUTS QN	SERIAL OUTPUTS QS	SERIAL OUTPUTS QS
⌐¬	0	X	X	OC	OC	Q7	NC
¬⌐	0	X	X	OC	OC	NC	Q7
⌐¬	1	0	X	NC	NC	Q7	NC
⌐¬	1	1	0	0	Q_{N-1}	Q7	NC
⌐¬	1	1	1	1	Q_{N-1}	Q7	NC
¬⌐	1	1	1	NC	NC	NC	Q7

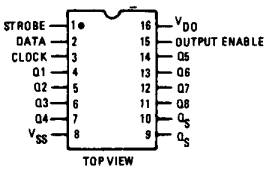
▲= LEVEL CHANGE
X = DON'T CARE
NC = NO CHANGE
OC = OPEN CIRCUIT

LOGIC 1 = HIGH
LOGIC 0 = LOW

AT THE POSITIVE CLOCK EDGE INFORMATION IN THE 7TH SHIFT REGISTER STAGE IS TRANSFERRED TO THE 8TH REGISTER STAGE AND THE Q_S OUTPUT



FUNCTIONAL DIAGRAM



TOP VIEW

CD4098B TYPES
COS/MOS DUAL MONOSTABLE MULTIVIBRATOR

High-Voltage Types (20-Volt Rating)

The RCA-CD4098B dual monostable multivibrator provides stable retriggerable/resettable one-shot operation for any fixed-voltage timing application.

An external resistor (R_X) and an external capacitor (C_X) control the timing for the circuit. Adjustment of R_X and C_X provides a wide range of output pulse widths from the Q and $\overline{Q}$ terminals. The time delay from trigger input to output transition (trigger propagation delay) and the time delay from reset input to output transition (reset propagation delay) are independent of R_X and C_X.

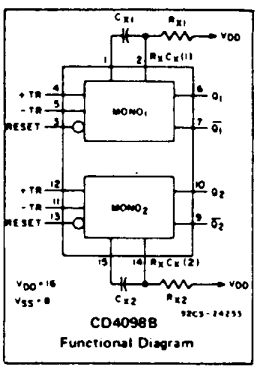
Leading-edge-triggering (+TR) and trailing-edge-triggering (−TR) inputs are provided for triggering from either edge of an input pulse. An unused +TR input should be tied to V_{SS}. An unused −TR input should be tied to V_{DD}. A RESET (on low level) is provided for immediate termination of the output pulse or to prevent output pulses when power is turned on. An unused RESET input should be tied to V_{DD}. However, if an entire section of the CD4098B is not used, its RESET should be tied to V_{SS}.

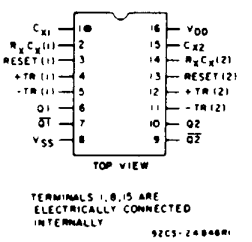
In normal operation the circuit triggers (extends the output pulse one period) on the application of each new trigger pulse. For operation in the non-retriggerable mode, $\overline{Q}$ is connected to −TR when leading-edge triggering (+TR) is used or Q is connected to +TR when trailing-edge triggering (−TR) is used.

The time period (T) for this multivibrator can be approximated by: $T_X = \frac{1}{2} R_X C_X$ for $C_X \geq 0.01\ \mu F$.

Values of T vary from unit to unit and as a function of voltage, temperature, and $R_X C_X$.

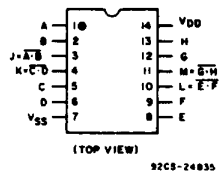
The minimum value of external resistance, R_X, is 5 kΩ. The maximum value of external capacitance, C_X, is 100 μF.



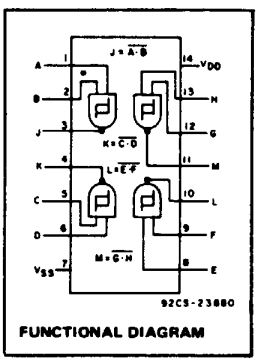


TERMINAL ASSIGNMENT

CD4093B TYPES
COS/MOS
QUAD 2-INPUT NAND
SCHMITT TRIGGERS



TERMINAL ASSIGNMENT

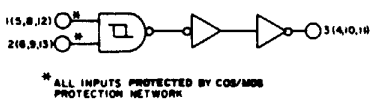


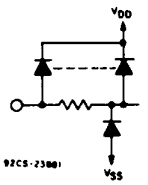
FUNCTIONAL DIAGRAM

High-Voltage Types (20 Volt Rating)

The RCA-CD4093B consists of four Schmitt-trigger circuits. Each circuit functions as a two-input NAND gate with Schmitt-trigger action on both inputs. The gate switches at different points for positive- and negative-going signals. The difference between the positive voltage (V_P) and the negative voltage (V_N) is defined as hysteresis voltage (V_H)

The CD4093B types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic package (E suffix), 14-lead ceramic flat package (K suffix), and in chip form (H suffix).





CD4514B
COS/MOS 4-BIT LATCH/4-TO-16
LINE DECODERS

The RCA-CD4514B and -CD4515B consist of a 4-bit strobed latch and a 4-to-16-line decoder. The latches hold the last input data presented prior to the strobe transition from 1 to 0. Inhibit control allows all outputs to be placed at 0(CD4514B) or 1(CD4515B) regardless of the state of the data or strobe inputs.

The decode truth table indicates all combinations of data inputs and appropriate selected outputs.

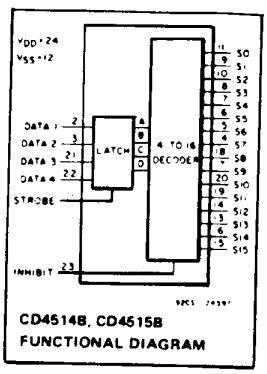
These devices are similar to industry types MC14514 and MC14515.

The CD4514B and CD4515B types are supplied in 24-lead hermetic dual-in-line ceramic packages (D and F suffixes), 24-lead dual-in line plastic packages (E suffix), and in chip form (H suffix).

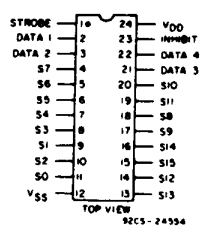
DECODE TRUTH TABLE (Strobe = 1)

INHIBIT	DECODER INPUTS				SELECTED OUTPUT CD4514B = Logic 1 (High) CD4515B = Logic 0 (Low)
	D	C	B	A	
0	0	0	0	0	S0
0	0	0	0	1	S1
0	0	0	1	0	S2
0	0	0	1	1	S3
0	0	1	0	0	S4
0	0	1	0	1	S5
0	0	1	1	0	S6
0	0	1	1	1	S7
0	1	0	0	0	S8
0	1	0	0	1	S9
0	1	0	1	0	S10
0	1	0	1	1	S11
0	1	1	0	0	S12
0	1	1	0	1	S13
0	1	1	1	0	S14
0	1	1	1	1	S15
1	X	X	X	X	All Outputs = 0, CD4514B All Outputs = 1, CD4515B

X = Don't Care Logic 1 = high Logic 0 = low



CD4514B, CD4515B
FUNCTIONAL DIAGRAM



CD4514B

TERMINAL ASSIGNMENT

CD4538B TYPES
COS/MOS DUAL PRECISION MONOSTABLE MULTIVIBRATOR

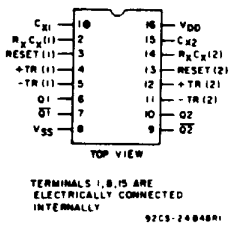
High-Voltage Types (20-Volt Rating)

The RCA-CD4538B dual precision monostable multivibrator provides stable retriggerable/resettable one-shot operation for any fixed-voltage timing application.

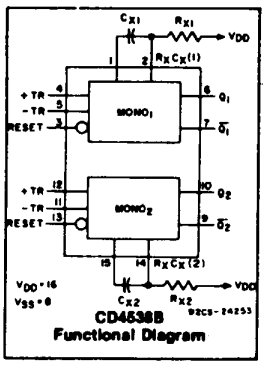
An external resistor (R_X) and an external capacitor (C_X) control the timing and accuracy for the circuit. Adjustment of R_X and C_X provides a wide range of output pulse widths from the Q and $\overline{Q}$ terminals. The time delay from trigger input to output transition (trigger propagation delay) and the time delay from reset input to output transition (reset propagation delay) are independent of R_X and C_X. Precision control of output pulse widths is achieved through linear CMOS techniques.

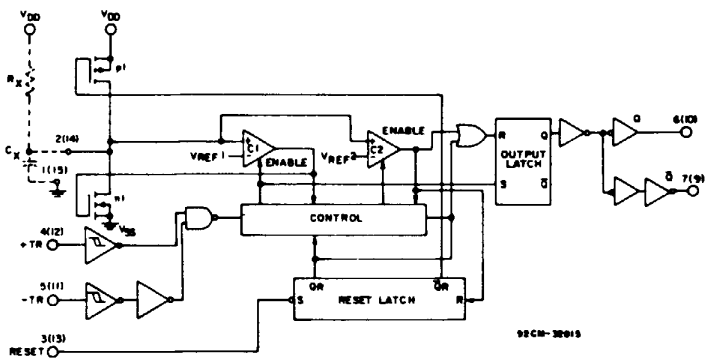
Leading-edge-triggering (+TR) and trailing-edge-triggering (−TR) inputs are provided for triggering from either edge of an input pulse. An unused +TR input should be tied to V_{SS}. An unused −TR input should be tied to V_{DD}. A RESET (on low level) is provided for immediate termination of the output pulse or to prevent output pulses when power is turned on. An unused RESET input should be tied to V_{DD}. However, if an entire section of the CD4538B is not used, its inputs must be tied to either V_{DD} or V_{SS}.

In normal operation the circuit triggers (extends the output pulse one period) on the application of each new trigger pulse.



TERMINAL ASSIGNMENT



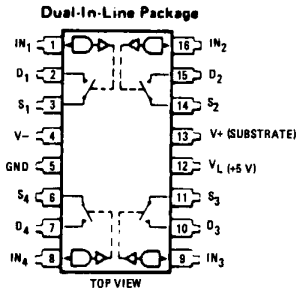


Logic diagram (½ of device shown).

DG211
QUAD MONOLITHIC SPST CMOS ANALOG SWITCH

The DG211 is a 4-channel single pole single throw analog switch which employs CMOS technology to insure low and nearly constant ON resistance over the entire analog signal range. The switch will conduct current in either direction with no offset voltage in the ON condition, and block voltages up to 30 V peak-to-peak in the OFF condition. The ON-OFF state of each switch is controlled by a driver. With a logic "0" at the input to the driver (0 V to 0.8 V) the switch will be ON, and a logic "1" (2.4 V to 15 V) will turn the switch OFF. The input can thus be directly interfaced with TTL, DTL, RTL, CMOS and certain PMOS circuits. Switch action is break-before-make. Logic inputs can directly connect to op-amp output swings.

PIN CONFIGURATION



LOGIC	SWITCH
0	ON
1	OFF

SWITCH OPEN FOR LOGIC "1" INPUT (POSITIVE LOGIC)

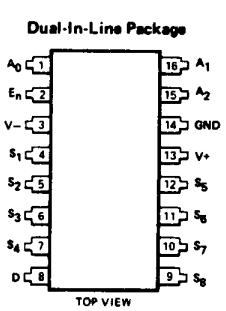
DG508
8-CHANNEL/4-CHANNEL DIFFERENTIAL CMOS ANALOG MULTIPLEXER

DESCRIPTION

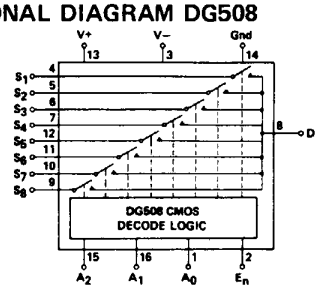
The DG508 is a single-pole 8-position (plus OFF) electronic switch array [DG509 double-pole, 4-position (plus OFF)], which employs 8 pairs of complementary MOS (CMOS) field-effect transistors designed to function as analog switches. In the ON condition each switch will conduct current in either direction, and in the OFF position each switch will block voltages up to 30 V peak-to-peak. The ON-OFF state of each switch is controlled by drivers, which are in turn controlled by a 3-bit binary word input plus an Enable-Inhibit input. The truth table below shows the binary word required to select any one of the 8 switch positions, provided a positive logic "1" is present at the Enable Input. With logic "0" at the Enable input all switches will be OFF. The logic decoder and the Enable inputs will recognize as logic "0" any voltage between 0 and 0.8 V, and any voltage between 2.4 and 15 V as logic "1" inputs. The inputs can thus be directly interfaced with TTL, DTL, RTL, CMOS and certain PMOS circuits. Delays are designed into logic decode and driver circuits to insure that switch action is break-before-make.

DECODE TRUTH TABLE

	A_2	A_1	A_0	En	ON SWITCH	DG509
DG508	X	X	X	0	NONE	
	0	0	0	1	1	
	0	0	1	1	2	
	0	1	0	1	3	
	0	1	1	1	4	
	1	0	0	1	5	Logic "1" = $V_{AH} \geq 2.4$ V
	1	0	1	1	6	
	1	1	0	1	7	Logic "0" = $V_{AL} \leq 0.8$ V
	1	1	1	1	8	



FUNCTIONAL DIAGRAM DG508

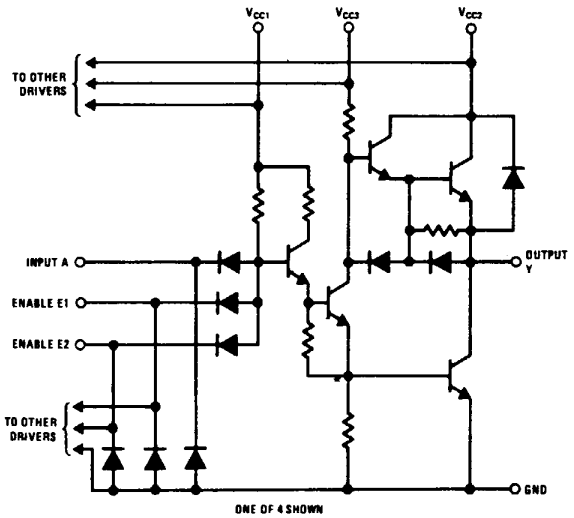


DS75365
QUAD TTL-TO-MOS DRIVER

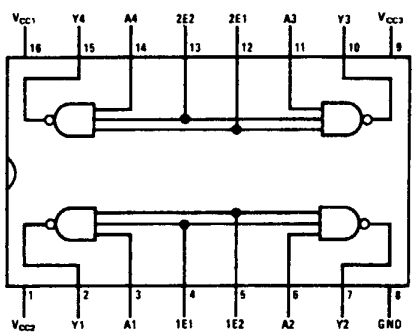
General Description

The DS75365 is a quad monolithic integrated TTL-to-MOS driver and interface circuit that accepts standard TTL and DTL input signals and provides high-current and high-voltage output levels suitable for driving MOS circuits. It is used to drive address, control, and timing inputs for several types of MOS RAMs including the 1103.

Schematic and Connection Diagrams



Dual-In-Line Package



TOP VIEW

Positive Logic: $Y = \overline{A \cdot E1 \cdot E2}$

LF347
WIDE BANDWIDTH QUAD JFET INPUT OPERATIONAL AMPLIFIER

General Description

The LF347 is a low cost, high speed quad JFET input operational amplifier with an internally trimmed input offset voltage (BI-FET II™ technology). The device requires a low supply current and yet maintains a large gain bandwidth product and a fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF347 is pin compatible with the standard LM348. This feature allows designers to immediately upgrade the overall performance of existing LM348 and LM324 designs.

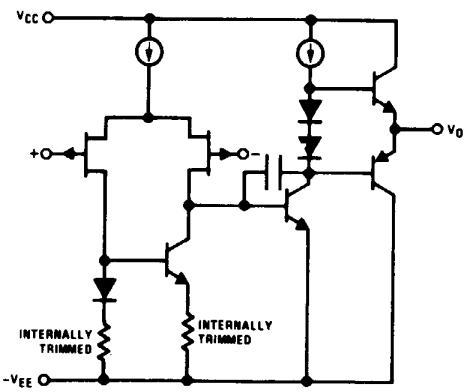
The LF347 may be used in applications such as high speed integrators, fast D/A converters, sample-and-hold circuits and many other circuits requiring low input offset voltage, low input bias current, high input impedance, high slew rate and wide bandwidth. The device has low noise and offset voltage drift.

Features

- Internally trimmed offset voltage — 2 mV
- Low input bias current — 50 pA
- Low input noise voltage — 16 nV/$\sqrt{Hz}$
- Low input noise current — 0.01 pA/$\sqrt{Hz}$
- Wide gain bandwidth — 4 MHz
- High slew rate — 13 V/μs
- Low supply current — 7.2 mA
- High input impedance — $10^{12}\Omega$
- Low total harmonic distortion A_V = 10, R_L = 10k, V_O = 20 Vp-p, BW = 20 Hz–20 kHz — <0.02%
- Low 1/f noise corner — 50 Hz
- Fast settling time to 0.01% — 2 μs

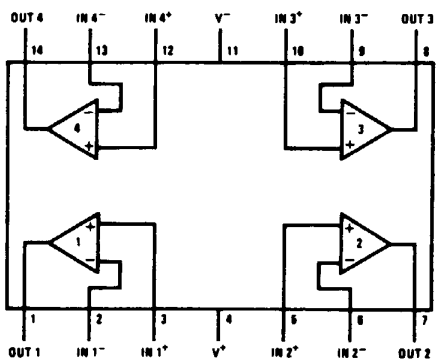
Simplified Schematic

1/4 Quad



Connection Diagram

Dual-In-Line Package



TOP VIEW

LM211
VOLTAGE COMPARATOR

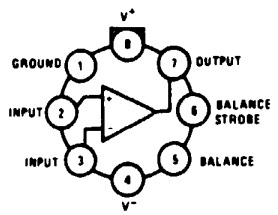
The LM111 and LM211 are voltage comparators that have input currents nearly a thousand times lower than devices like the LM106 or LM710. They are also designed to operate over a wider range of supply voltages: from standard ±15V op amp supplies down to the single 5V supply used for IC logic. Their output is compatible with RTL, DTL and TTL as well as MOS circuits. Further, they can drive lamps or relays, switching voltages up to 50V at currents as high as 50 mA. Outstanding characteristics include:

- Operates from single 5V supply
- Input current: 150 nA max. over temperature
- Offset current: 20 nA max. over temperature
- Differential input voltage range: ±30V
- Power consumption: 135 mW at ±15V

Both the inputs and the outputs of the LM111 or the LM211 can be isolated from system ground, and the output can drive loads referred to ground, the positive supply or the negative supply. Offset balancing and strobe capability are provided and outputs can be wire OR'ed. Although slower than the LM106 and LM710 (200 ns response time vs 40 ns) the devices are also much less prone to spurious oscillations. The LM111 has the same pin configuration as the LM106 and LM710.

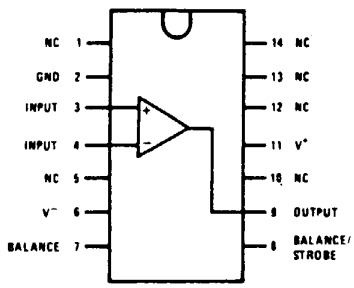
The LM211 is identical to the LM111, except that its performance is specified over a −25°C to 85°C temperature range instead of −55°C to 125°C.

Metal Can Package



NOTE: Pin 4 connected to case.
TOP VIEW

Dual-In-Line Package



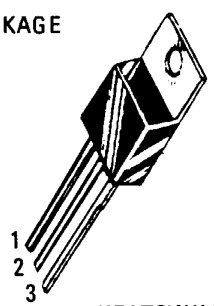
Note: Pin 5 connected to bottom of package.
TOP VIEW

LM317T
THREE-TERMINAL
ADJUSTABLE POSITIVE
VOLTAGE REGULATOR

SILICON MONOLITHIC
INTEGRATED CIRCUIT

The 317 is an adjustable three-terminal positive voltage regulator capable of supplying 1.5 A over an output range of 1.2 V to 37 V. Internal current limiting, thermal shutdown, and safe area compensation make the regulator almost blow-out proof.

T SUFFIX
PLASTIC PACKAGE
CASE 221A
(TO-220)



PIN 1 ADJUST
PIN 2 V_{OUT}
PIN 3 V_{IN}

HEATSINK SURFACE CONNECTED
TO PIN 2

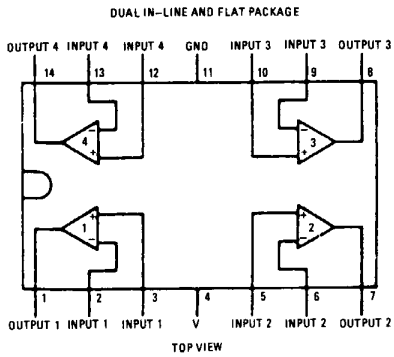
LM324
LOW POWER QUAD OPERATIONAL AMPLIFIERS

General Description

The LM124 series consists of four independent, high gain, internally frequency compensated operational amplifiers which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

Application areas include transducer amplifiers, dc gain blocks and all the conventional op amp circuits which now can be more easily implemented in single power supply systems. For example, the LM124 series can be directly operated off of the standard +5 V_{DC} power supply voltage which is used in digital systems and will easily provide the required interface electronics without requiring the additional ±15 V_{DC} power supplies.

Connection Diagram

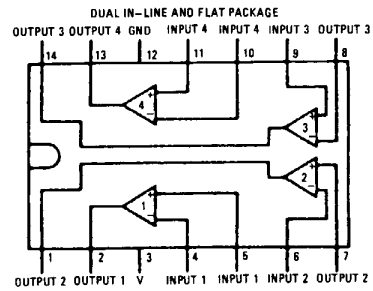


LM339
LOWER POWER LOW OFFSET VOLTAGE QUAD COMPARATORS

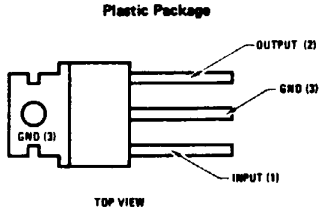
General Description

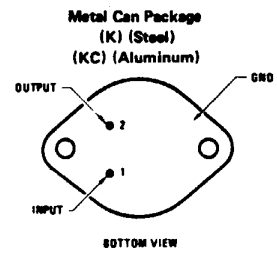
The LM139 series consists of four independent precision voltage comparators with an offset voltage specification as low as 2 mV max for all four comparators. These were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common-mode voltage range includes ground, even though operated from a single power supply voltage.

Application areas include limit comparators, simple analog to digital converters; pulse, squarewave and time delay generators; wide range VCO, MOS clock timers; multivibrators and high voltage digital logic gates. The LM139 series was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, they will directly interface with MOS logic– where the low power drain of the LM339 is a distinct advantage over standard comparators.



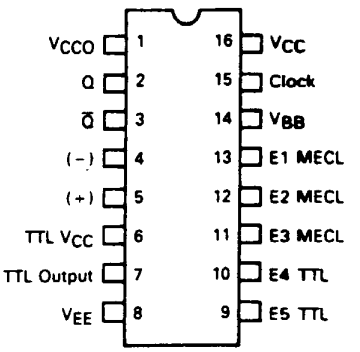
LM340 SERIES
VOLTAGE REGULATORS



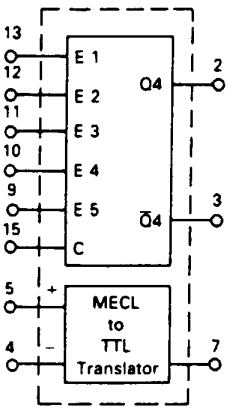


MC12013
TWO-MODULUS PRESCALER

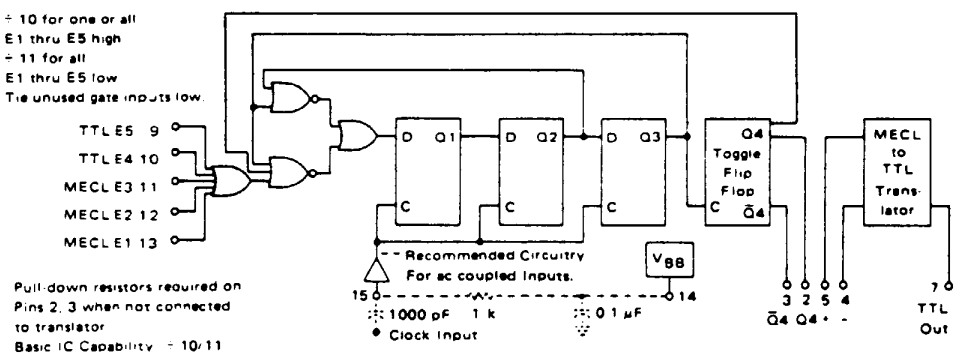
These devices are two-modulus prescalers which will divide by 5 and 6, 8 and 9, and 10 and 11, respectively. A MECL-to-TTL translator is provided to interface directly with the MC12014 Counter Control Logic. In addition, there is a buffered clock input and MECL bias voltage source.



LOGIC DIAGRAM



V_{CCO} = pin 1
V_{CC} = pin 16
V_{EE} = pin 8



MC145156
SERIAL INPUT PLL FREQUENCY SYNTHESIZER

The MC145156 is one of a family of LSI PLL frequency synthesizer parts from Motorola CMOS. The family includes devices having serial, parallel and 4-bit data bus programmable inputs. Options include single- or dual-modulus capability, transmit/receive offsets, choice of phase detector types and choice of reference divider integer values.

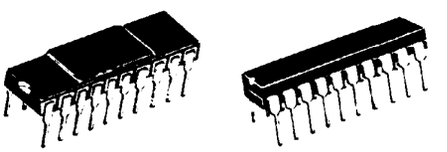
The MC145156 is programmed by a clocked, serial input, 19-bit data stream. The device features consist of a reference oscillator, selectable-reference divider, digital-phase detector, 10-bit programmable divide-by-N counter, 7-bit programmable ÷ A counter and the necessary shift register and latch circuitry for accepting the serial input data. When combined with a loop filter and VCO, the MC145156 can provide all the remaining functions for a PLL frequency synthesizer operating up to the device's frequency limit. For higher VCO frequency operation, a down mixer or a dual modulus prescaler can be used between the VCO and MC145156.

- General Purpose Applications –
  CATV TV Tuning
  AM/FM Radios Scanning Receivers
  Two-Way Radios Amateur Radio
- Low Power Drain
- 3.0 to 9.0 Vdc Supply Range
- >30 MHz Typical Input Capability @ 5 Vdc
- 8 User Selectable Reference Divider Values – 8, 64, 128, 256, 640, 1000, 1024, 2048
- On- or Off-Chip Reference Oscillator Operation with Buffered Output
- Lock Detect Signal
- Two Open-Drain Switch Outputs
- Dual Modulus/Serial Programming
- ÷N Range = 3 to 1023
- "Linearized" Digital Phase Detector Enhances Transfer Function Linearity
- Two Error Signal Options –
  Single Ended (Three-State)
  Double Ended

CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

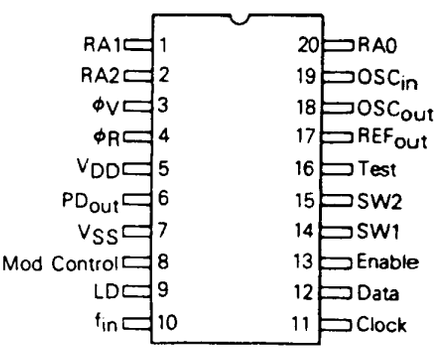
SERIAL INPUT PLL FREQUENCY SYNTHESIZER

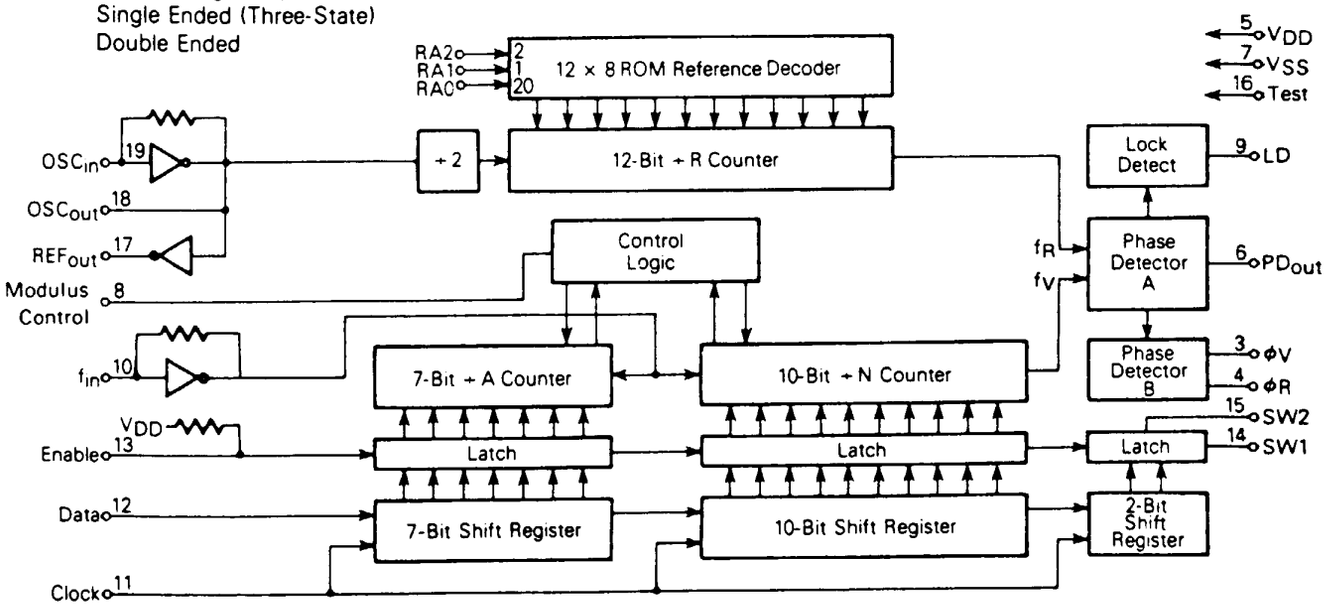


L SUFFIX
CERAMIC PACKAGE
CASE 729-01

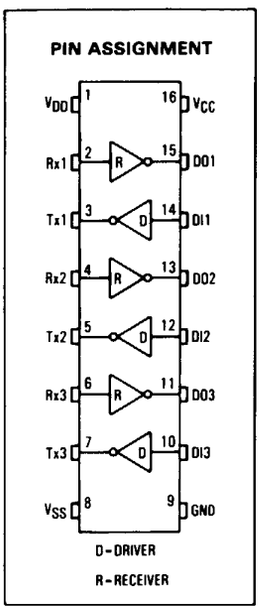
P SUFFIX
PLASTIC PACKAGE
CASE 738-02

PIN ASSIGNMENT

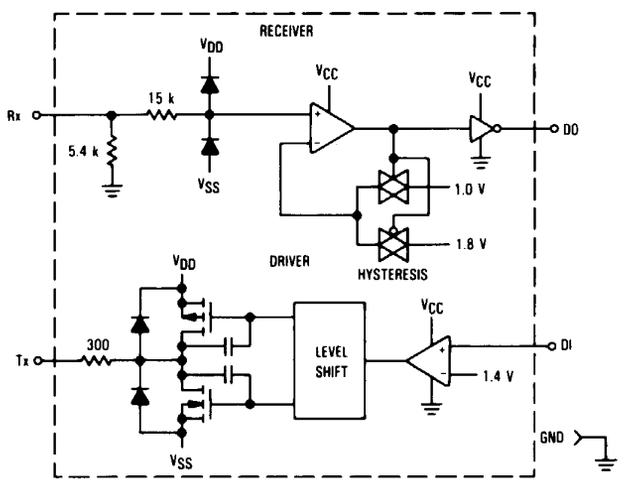




MC145406
RS-232-C/V.28 DRIVER/RECEIVER



FUNCTION DIAGRAM



PIN DESCRIPTIONS

V_{DD} – POSITIVE POWER SUPPLY (PIN 1)

The most positive power supply pin, which is typically 5 to 12 volts.

V_{SS} – NEGATIVE POWER SUPPLY (PIN 8)

The most negative power supply pin, which is typically – 5 to – 12 volts.

V_{CC} – DIGITAL POWER SUPPLY (PIN 16)

The digital supply pin, which is connected to the logic power supply (maximum + 5.5 volts). V_{CC} *must* be less than or equal to V_{DD}.

GND – GROUND (PIN 9)

Ground return pin is typically connected to the signal ground pin of the RS-232-C connector (connector pin 7) as well as to the logic power supply ground.

Rx1, Rx2, Rx 3 – RECEIVE DATA INPUT (PINS 2, 4, 6)

These are the RS-232-C receive signal inputs whose voltages can range from + 25 to – 25 volts. A voltage between + 3 and + 25 is decoded as a space and causes the corresponding DO pin to swing to ground (0 V); a voltage between – 3 and – 25 volts is decoded as a mark and causes the DO pin to swing up to V_{CC}. The actual turn-on input switchpoint is typically biased at 1.8 volts above ground, and includes 800 millivolts of hysteresis for noise rejection. The nominal input impedance is 5 kilohm. An open or grounded input pin is interpreted as a mark, forcing the DO pin to V_{CC}.

DO1, DO2, DO3 – DATA OUTPUT (PINS 11, 13, 15)

These are the receiver digital output pins which swing from V_{CC} to ground. A space on the Rx pin causes DO to produce a logic zero, a mark, a logic one. Each output pin is capable of driving one LSTTL input load.

DI1, DI2, DI3 – DATA INPUT (PINS 10, 12 14)

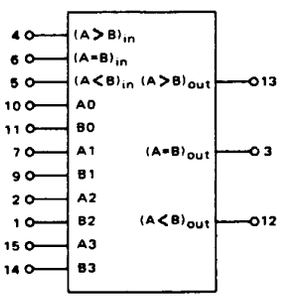
These are the high-impedance digital input pins to the drivers. TTL compatibility is accomplished by biasing the input switchpoint at 1.4 volts above ground. Input voltage levels on these pins must be between V_{CC} and ground.

Tx1, Tx2, Tx3 – TRANSMIT DATA OUTPUT (PINS 3, 5, 7)

These are the RS-232-C transmit signal output pins which swing from V_{DD} to V_{SS}. A logic one at a DI input causes the corresponding Tx output to swing to V_{SS}. A logic zero causes the output to swing to V_{DD} (the output voltages will be slightly less than V_{DD} or V_{SS} depending upon the output load). Output slew rates are limited to a maximum of 30 volts per microsecond. These outputs are protected from short circuits to a worst case RS-232-C driver of ± 15 volts. When the MC145406 is off ($V_{DD} = V_{SS} = V_{CC} = GND$), the minimum output impedance is 300 ohms.

MC14585B
CMOS MSI
(LOW POWER COMPLEMENTARY MOS)
4-BIT MAGNITUDE COMPARATOR

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8

4-BIT MAGNITUDE COMPARATOR

The MC14585B 4-Bit Magnitude Comparator is constructed with complementary MOS (CMOS) enhancement mode devices. The circuit has eight comparing inputs (A3, B3, A2, B2, A1, B1, A0, B0), three cascading inputs (A<B, A=B, and A>B), and three outputs (A<B, A=B, and A>B). This device compares two 4-bit words (A and B) and determines whether they are "less than", "equal to", or "greater than" by a high level on the appropriate output. For words greater than 4-bits, units can be cascaded by connecting outputs (A<B), and (A=B) to the corresponding inputs of the next significant comparator (input A>B is connected to a high). Inputs (A<B), (A=B), and (A>B) on the least significant (first) comparator are connected to a low, a high, and a high, respectively.

Applications include logic in CPU's, correction and/or detection of instrumentation conditions, comparator in testers, converters, and controls.

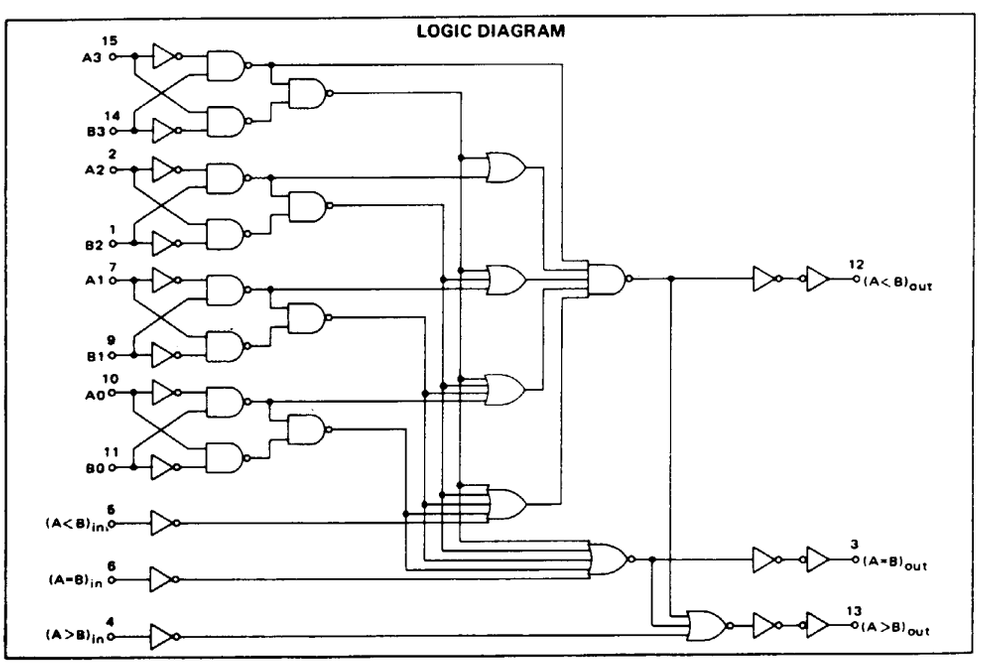
- Diode Protection on All Inputs
- Noise Immunity = 45% of V_{DD} typical
- High Fanout > 50
- Quiescent Current = 5.0 nA/package typical @ 5 Vdc
- Expandable
- Applicable to Binary or 8421-BCD Code
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads, One Low-power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range

TRUTH TABLE

INPUTS							OUTPUTS		
COMPARING				CASCADING					
A3, B3	A2, B2	A1, B1	A0, B0	A<B	A=B	A>B	A<B	A=B	A>B
A3>B3	X	X	X	X	X	1	0	0	1
A3=B3	A2>B2	X	X	X	X	1	0	0	1
A3=B3	A2=B2	A1>B1	X	X	X	1	0	0	1
A3=B3	A2=B2	A1=B1	A0>B0	X	X	1	0	0	1
A3=B3	A2=B2	A1=B1	A0=B0	0	0	1	0	0	1
A3=B3	A2=B2	A1=B1	A0=B0	0	1	1	0	1	0
A3=B3	A2=B2	A1=B1	A0=B0	1	0	1	1	0	0
A3=B3	A2=B2	A1=B1	A0<B0	X	X	X	1	0	0
A3=B3	A2=B2	A1<B1	X	X	X	X	1	0	0
A3=B3	A2<B2	X	X	X	X	X	1	0	0
A3<B3	X	X	X	X	X	X	1	0	0

X = Don't Care

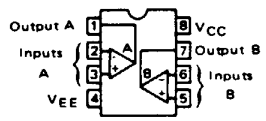
LOGIC DIAGRAM



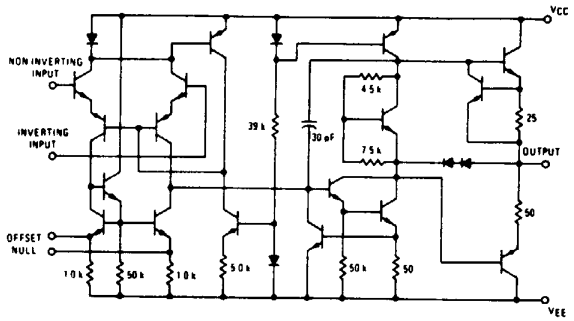
MC1458
DUAL OPERATIONAL AMPLIFIER
SILICON MONOLITHIC INTEGRATED CIRCUIT

P1 SUFFIX
PLASTIC PACKAGE
CASE 626
(MC1458,MC1458C,MC1458N)

U SUFFIX
CERAMIC PACKAGE
CASE 693



EQUIVALENT CIRCUIT SCHEMATIC



MC1496
BALANCED MODULATOR – DEMODULATOR
SILICON MONOLITHIC INTEGRATED CIRCUIT

VOLTAGE GAIN AND OUTPUT FREQUENCIES

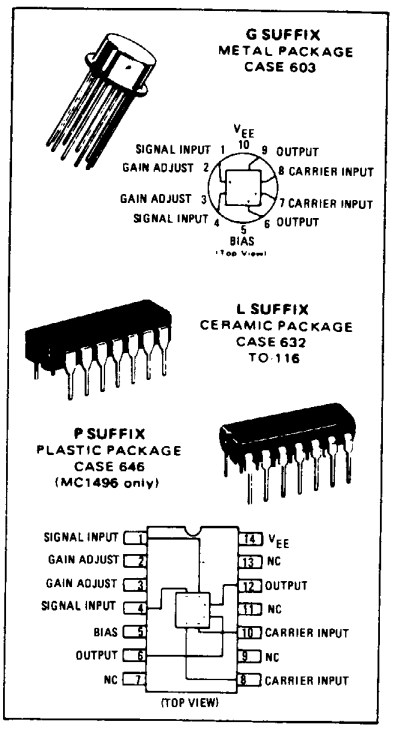
Carrier Input Signal (V_C)	Approximate Voltage Gain	Output Signal Frequency(s)
Low-level dc	$\frac{R_L V_C}{2(R_E + 2r_e)\left(\frac{KT}{q}\right)}$	f_M
High-level dc	$\frac{R_L}{R_E + 2r_e}$	f_M
Low-level ac	$\frac{R_L V_C(rms)}{2\sqrt{2}\left(\frac{KT}{q}\right)(R_E + 2r_e)}$	$f_C \pm f_M$
High-level ac	$\frac{0.637\, R_L}{R_E + 2r_e}$	$f_C \pm f_M$, $3f_C \pm f_M$, $5f_C \pm f_M$, . . .

NOTES:
1. Low-level Modulating Signal, V_M, assumed in all cases. V_C is Carrier Input Voltage.
2. When the output signal contains multiple frequencies, the gain expression given is for the output amplitude of each of the two desired outputs, $f_C + f_M$ and $f_C - f_M$.
3. All gain expressions are for a single-ended output. For a differential output connection, multiply each expression by two.
4. R_L = Load resistance.
5. R_E = Emitter resistance between pins 2 and 3.
6. r_e = Transistor dynamic emitter resistance, at +25°C;

$$r_e \approx \frac{26\ mV}{I_5\ (mA)}$$

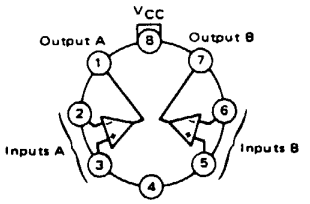
7. K = Boltzmann's Constant, T = temperature in degrees Kelvin, q = the charge on an electron.

$$\frac{KT}{q} \approx 26\ mV \text{ at room temperature}$$



MC3358
DUAL DIFFERENTIAL INPUT OPERATIONAL AMPLIFIERS
SILICON MONOLITHIC INTEGRATED CIRCUIT

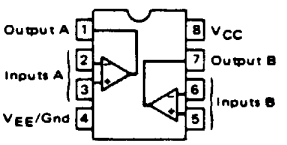
G SUFFIX
METAL PACKAGE
CASE 601



(TOP VIEW)

P1 SUFFIX
PLASTIC PACKAGE
CASE 626
(MC3458, MC3358 only)

U SUFFIX
CERAMIC PACKAGE
CASE 693



(TOP VIEW)

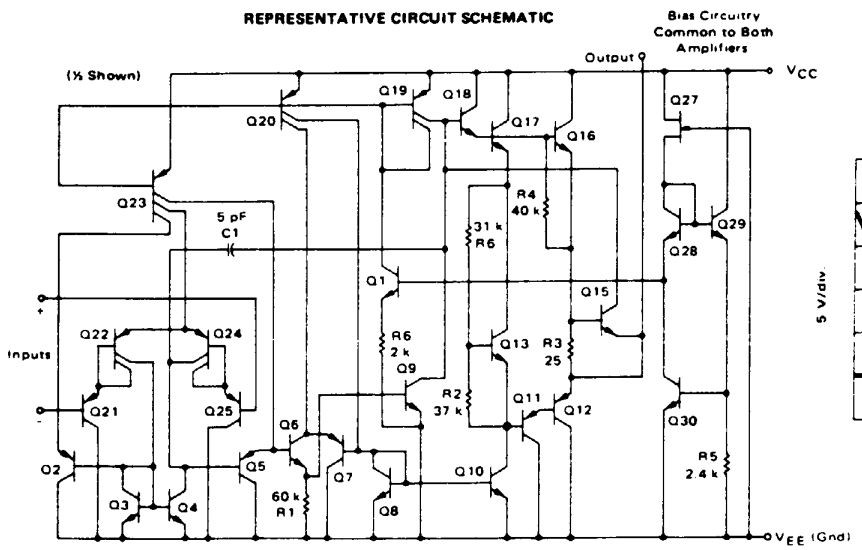
CIRCUIT DESCRIPTION

The MC3358 Series is made using two internally compensated, two-stage operational amplifiers. The first stage of each consists of differential input devices Q24 and Q22 with input buffer transistors Q25 and Q21 and the differential to single ended converter Q3 and Q4. The first stage performs not only the first stage gain function but also performs the level shifting and transconductance reduction functions. By reducing the transconductance a smaller compensation capacitor (only 5 pF) can be employed, thus saving chip area. The transconductance reduction is accomplished by splitting the collectors of Q24 and Q22. Another feature of this input stage is that the input common-mode range can include the negative supply or ground, in single supply operation, without saturating either the input devices or the differential to single-ended converter. The second stage consists of a standard current source load amplifier stage.

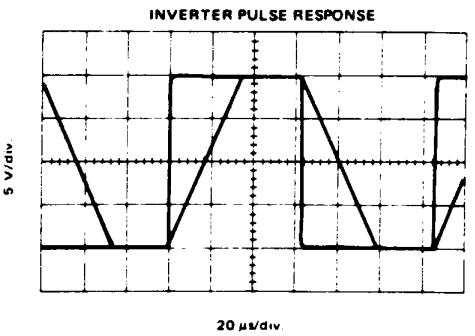
The output stage is unique because it allows the output to swing to ground in single supply operation and yet does not exhibit any crossover distortion in split supply operation. This is possible because class AB operation is utilized.

Each amplifier is biased from an internal-voltage regulator which has a low temperature coefficient thus giving each amplifier good temperature characteristics as well as excellent power supply rejection.

REPRESENTATIVE CIRCUIT SCHEMATIC



INVERTER PULSE RESPONSE



MC7800C, AC SERIES
THREE-TERMINAL POSITIVE VOLTAGE REGULATORS

The MC78L00 Series of positive voltage regulators are inexpensive, easy-to-use devices suitable for a multitude of applications that require a regulated supply of up to 100 mA. Like their higher powered MC7800 and MC78M00 Series cousins, these regulators feature internal current limiting and thermal shutdown making them remarkably rugged. No external components are required with the MC78L00 devices in many applications.

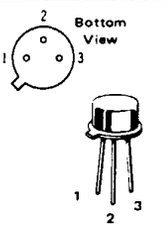
These devices offer a substantial performance advantage over the traditional zener diode-resistor combination. Output impedance is greatly reduced and quiescent current is substantially reduced.

- Wide Range of Available, Fixed Output Voltages
- Low Cost
- Internal Short-Circuit Current Limiting
- Internal Thermal Overload Protection
- No External Components Required
- Complementary Negative Regulators Offered (MC79L00 Series)
- Available in Either ±5% (AC) or ±10% (C) Selections

THREE-TERMINAL POSITIVE FIXED VOLTAGE REGULATORS

P SUFFIX
CASE 29
TO-92

Pin 1. Output
2. Ground
3. Input

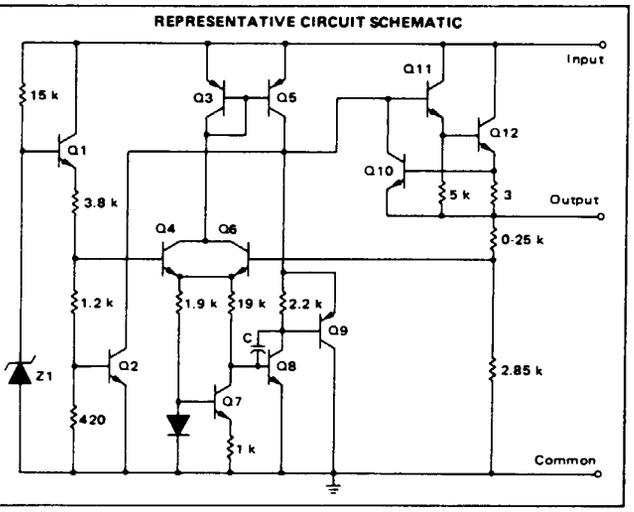


G SUFFIX
CASE 79
TO-39

Pin 1. Input
2. Output
3. Ground

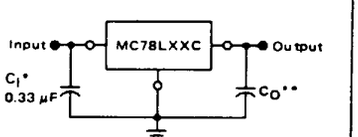
(Case connected to pin 3)

REPRESENTATIVE CIRCUIT SCHEMATIC



Device No. ±10%	Device No. ±5%	Nominal Voltage
MC78L05C	MC78L05AC	5.0
MC78L08C	MC78L08AC	8.0
MC78L12C	MC78L12AC	12
MC78L15C	MC78L15AC	15
MC78L18C	MC78L18AC	18
MC78L24C	MC78L24AC	24

STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.0 V above the output voltage even during the low point on the input ripple voltage.

* = C_I is required if regulator is located an appreciable distance from power supply filter.

** = C_O is not needed for stability; however, it does improve transient response.

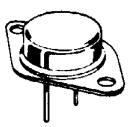
MC7900C SERIES
THREE-TERMINAL NEGATIVE VOLTAGE REGULATORS

The MC7900C Series of fixed output negative voltage regulators are intended as complements to the popular MC7800C Series devices. These negative regulators are available in the same seven-voltage options as the MC7800C devices. In addition, two extra voltage options commonly employed in MECL systems are also available in the negative MC7900C Series.

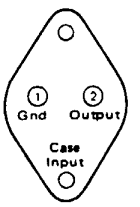
Available in fixed output voltage options from -2.0 to -24 volts, these regulators employ current limiting, thermal shutdown, and safe-area compensation – making them remarkably rugged under most operating conditions. With adequate heat-sinking they can deliver output currents in excess of 1.0 ampere.

- No External Components Required
- Internal Thermal Overload Protection
- Internal Short-Circuit Current Limiting
- Output Transistor Safe-Area Compensation
- Packaged in the Plastic Case 221A and Case 1 (TO-220 and Hermetic TO-3)

THREE-TERMINAL NEGATIVE FIXED VOLTAGE REGULATORS



K SUFFIX
METAL PACKAGE
CASE 1
(TO-3 TYPE)



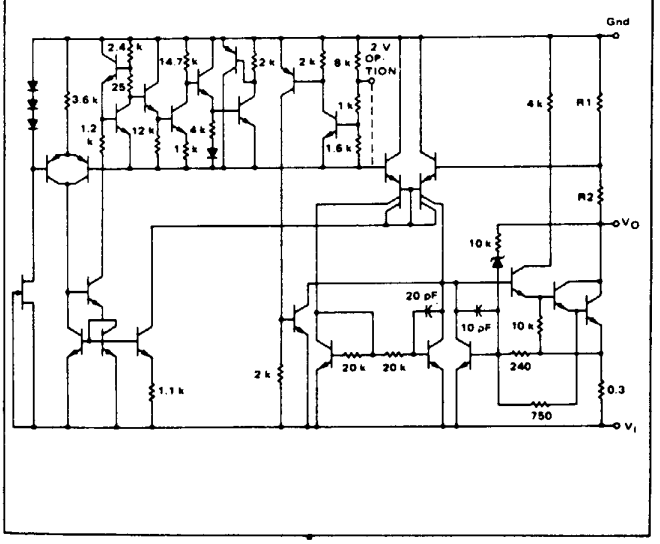
(bottom view)

T SUFFIX
PLASTIC PACKAGE
CASE 221A

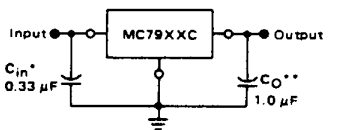
Pin 1. Ground
2. Input
3. Output

(Heatsink surface connected to Pin2)

SCHEMATIC DIAGRAM



STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.0 V more negative even during the high point on the input ripple voltage.

XX = these two digits of the type number indicate voltage.

* = C_{in} is required if regulator is located an appreciable distance from power supply filter.

** = C_O improves stability and transient response.

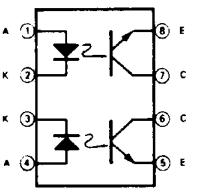
DEVICE TYPE/NOMINAL OUTPUT VOLTAGE

MC7902C - 2.0 Volts	MC7906C - 6.0 Volts	MC7915C - 15 Volts
MC7905C - 5.0 Volts	MC7908C - 8.0 Volts	MC7918C - 18 Volts
MC7905.2C – 5.2 Volts	MC7912C - 12 Volts	MC7924C - 24 Volts

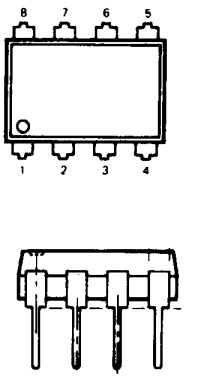
MCT6
DUAL PHOTOTRANSISTOR OPTOISOLATORS

DESCRIPTION

The MCT6 and MCT66 optoisolators have two channels for high density applications. For four channel applications, two-packages fit into a standard 16-pin DIP socket. Each channel is an NPN silicon planar phototransistor optically coupled to a gallium arsenide diode.



PACKAGE DIMENSIONS

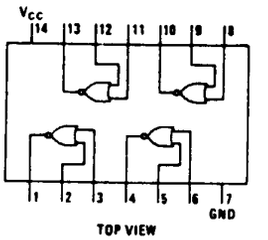


MM54C02/MM74C02
QUAD 2-INPUT NOR GATE

These logic gates employ complementary MOS (CMOS) to achieve wide power supply operating range, low power consumption, high noise immunity and symmetric controlled rise and fall times. With features such as this the 54C/74C logic family is close to ideal for use in digital systems. Function and pin out compatibility with series 54/74 devices minimizes design time for those designers already familiar with the standard 54/74 logic family.

All inputs are protected from damage due to static discharge by diode clamps to V_{CC} and GND.

MM54C02/MM74C02

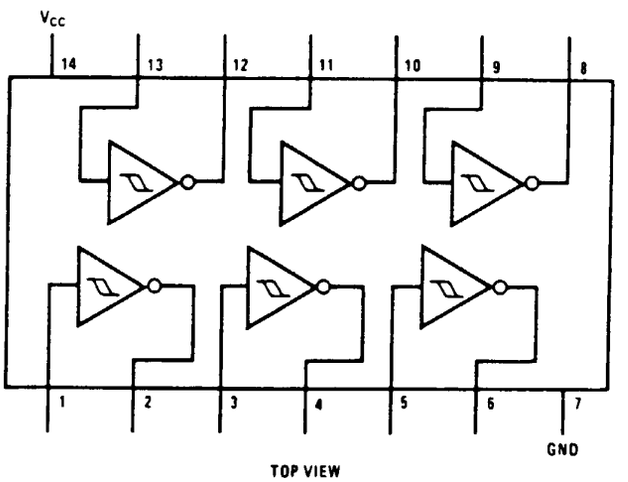


TOP VIEW

MM74C14
HEX SCHMITT TRIGGER

The MM54C14/MM74C14 Hex Schmitt Trigger is a monolithic complementary MOS (CMOS) integrated circuit constructed with N and P-channel enhancement transistors. The positive and negative going threshold voltages, V_{T+} and V_{T-}, show low variation with respect to temperature (typ. 0.0005 V/°C at V_{CC} = 10 V), and hysteresis, $V_{T+} - V_{T-} \geq 0.2V_{CC}$ is guaranteed.

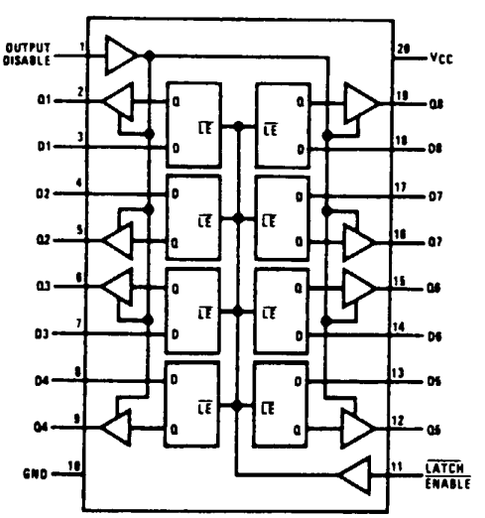
All inputs are protected from damage due to static discharge by diode clamps to V_{CC} and GND.



TOP VIEW

MM74C373
OCTAL LATCH

Connection Diagram



TOP VIEW

General Description

The MM54C373/MM74C373, MM54C374/MM74C374 are integrated, complementary MOS (CMOS), 8-bit storage elements with TRI-STATE® outputs. These outputs have been specially designed to drive highly capacitive loads, such as one might find when driving a bus, and to have a fan-out of 1 when driving standard TTL. When a high logic level is applied to the OUTPUT DISABLE input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

The MM54C373/MM74C373 is an 8-bit latch. When $\overline{\text{LATCH ENABLE}}$ is high, the Q outputs will follow the D inputs. When $\overline{\text{LATCH ENABLE}}$ goes low, data at the D inputs, which meets the set-up and hold time requirements, will be retained at the outputs until $\overline{\text{LATCH ENABLE}}$ returns high again.

NE-SA594
VACUUM FLUORESCENT DISPLAY DRIVER

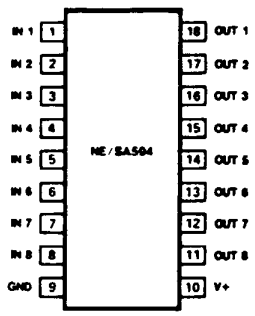
DESCRIPTION

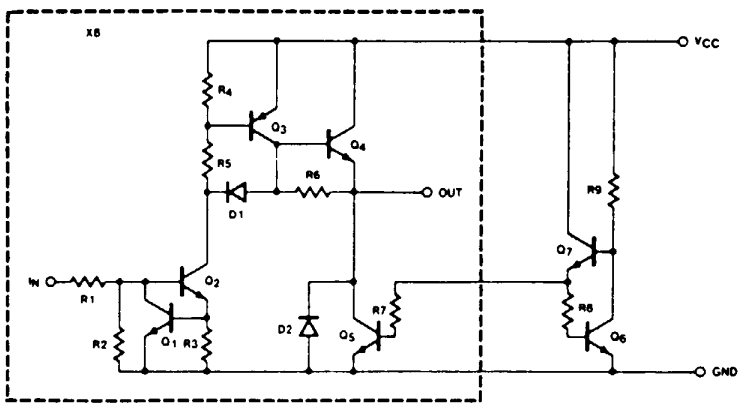
The NE/SA594 is a display driver interface for vacuum fluorescent displays. The device is comprised of 8 drivers and a bias network and is capable of driving the digits and/or segments of most vacuum fluorescent displays.

The inputs are designed to be compatible with TTL, DTL, NMOS, PMOS or CMOS output circuitry.

There is an active pull-down circuit on each output so that display ghosting is minimized and no external components are required for most fluorescent display applications.

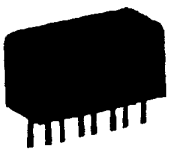
N, F PACKAGE





SAY-1
SUPER HIGH LEVEL (+23 DBM LO) DOUBLE-BALANCED MIXERS

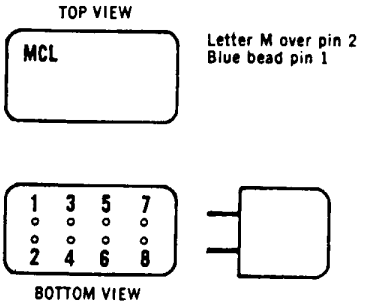
SAY SERIES

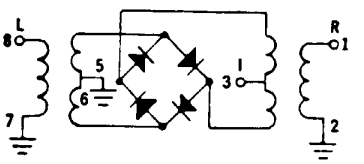


DESCRIPTION — High-level RF input capability coupled with ultra-low distortion, octaves of bandwidth, and reasonably good conversion loss make the SAY series obvious choices for applications in ECM receivers, spectrum analyzers, and field radios.

These mixers offer two-tone, third order intermodulation products that are typically 70 dB below the desired IF level (each tone is set at 0 dBm and the LO drive is at +23 dBm). The 1 dB conversion compression point occurs at an RF level of +20 dBm.

CONNECTIONS

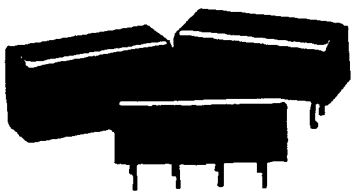




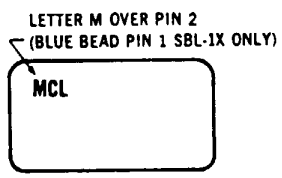
Model No.	-1 -2 -11
LO	8
RF	1
IF	3
Ground	2,5,6,7
Case Ground	2,5,6,7

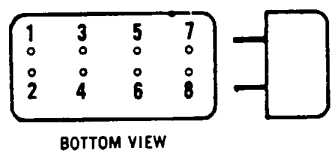
SBL-1
STANDARD LEVEL (+7 DBM LO)
DOUBLE-BALANCED MIXERS

SBL SERIES

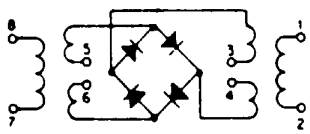


CONNECTIONS





BOTTOM VIEW



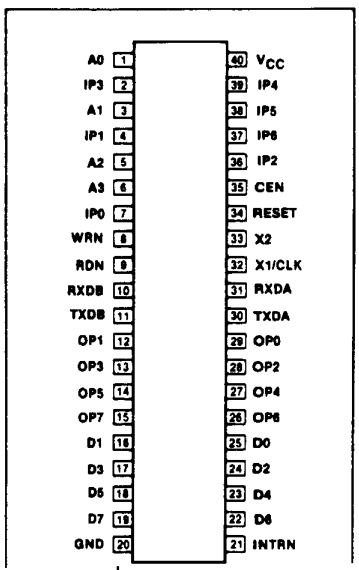
PIN LAYOUT

	Fig. 1	Fig. 2
Model No.	-1 *	-1X
LO	8	8
RF	1	3,4
IF	3,4	1
Ground	2,5,6,7	2,5,6,7
Case Ground	—	2,5,6,7

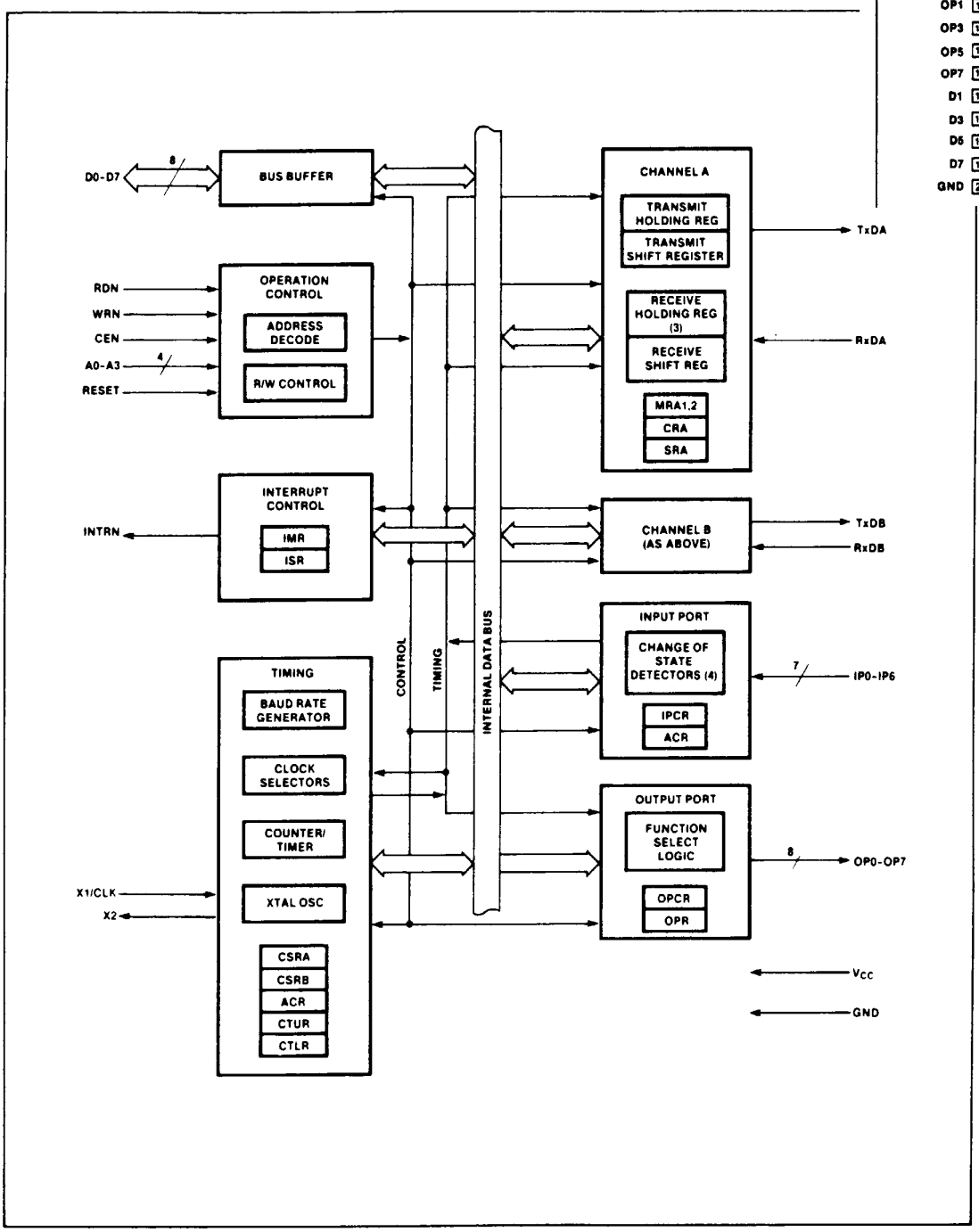
NOTE: PINS 3 AND 4 MUST BE CONNECTED TOGETHER

SCN2681
DUAL UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER (DUART)

PIN CONFIGURATION



BLOCK DIAGRAM



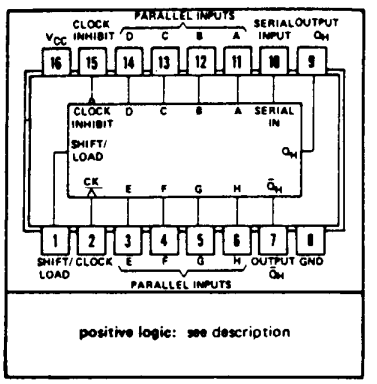
SCN2681 (Cont.)

PIN DESIGNATION

MNEMONIC	APPLICABLE			TYPE	NAME AND FUNCTION
	40	28	24		
D0-D7	X	X	X	I/O	**Data Bus:** Bidirectional 3-state data bus used to transfer commands, data and status between the DUART and the CPU. D0 is the least significant bit.
CEN	X	X	X	I	**Chip Enable:** Active low input signal. When low, data transfers between the CPU and the DUART are enabled on D0-D7 as controlled by the WRN, RDN and A0-A3 inputs. When high, places the D0-D7 lines in the 3-state condition.
WRN	X	X	X	I	**Write Strobe:** When low and CEN is also low, the contents of the data bus is loaded into the addressed register. The transfer occurs on the rising edge of the signal.
RDN	X	X	X	I	**Read Strobe:** When low and CEN is also low, causes the contents of the addressed register to be presented on the data bus. The read cycle begins on the falling edge of RDN.
A0-A3	X	X	X	I	**Address Inputs:** Select the DUART internal registers and ports for read/write operations.
RESET	X	X	X	I	**Reset:** A high level clears internal registers (SRA, SRB, IMR, ISR, OPR, OPCR), puts OP0-OP7 in the high state, stops the counter/timer, and puts channels A and B in the inactive state, with the TxDA and TxDB outputs in the mark (high) state.
INTRN	X	X	X	O	**Interrupt Request:** Active low, open drain, output which signals the CPU that one or more of the eight maskable interrupting conditions are true.
X1/CLK	X	X	X	I	**Crystal 1:** Crystal or external clock input. A crystal or clock of the specified limits must be supplied at all times. When a crystal is used, a capacitor must be connected from this pin to ground (see figure 5).
X2	X	X		O	**Crystal 2:** Connection for other side of the crystal. Should be connected to ground if a crystal is not used. When a crystal is used, a capacitor must be connected from this pin to ground (see figure 5).
RxDA	X	X	X	I	**Channel A Receiver Serial Data Input:** The least significant bit is received first. 'Mark' is high, 'space' is low.
RxDB	X	X	X	I	**Channel B Receiver Serial Data Input:** The least significant bit is received first. 'Mark' is high, 'space' is low.
TxDA	X	X	X	O	**Channel A Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is held in the 'mark' condition when the transmitter is disabled, idle, or when operating in local loopback mode. 'Mark' is high, 'space' is low.
TxDB	X	X	X	O	**Channel B Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is held in the 'mark' condition when the transmitter is disabled, idle, or when operating in local loopback mode. 'Mark' is high, 'space' is low.
OP0	X	X		O	**Output 0:** General purpose output, or channel A request to send (RTSAN, active low). Can be deactivated on receive or transmit.
OP1	X	X		O	**Output 1:** General purpose output, or channel B request to send (RTSBN, active low). Can be deactivated on receive or transmit.
OP2	X			O	**Output 2:** General purpose output, or channel A transmitter 1X or 16X clock output, or channel A receiver 1X clock output.
OP3	X			O	**Output 3:** General purpose output, or open drain, active low counter/timer output, or channel B transmitter 1X clock output, or channel B receiver 1X clock output.
OP4	X			O	**Output 4:** General purpose output, or channel A open drain, active low, RxRDYA/FFULLA output.
OP5	X			O	**Output 5:** General purpose output, or channel B open drain, active low, RxRDYB/FFULLB output.
OP6	X			O	**Output 6:** General purpose output, or channel A open drain, active low, TxRDYA output.
OP7	X			O	**Output 7:** General purpose output, or channel B open drain, active low, TxRDYB output.
IP0	X			I	**Input 0:** General purpose input, or channel A clear to send active low input (CTSAN).
IP1	X			I	**Input 1:** General purpose input, or channel B clear to send active low input (CTSBN).
IP2	X	X		I	**Input 2:** General purpose input, or counter/timer external clock input.
IP3	X			I	**Input 3:** General purpose input, or channel A transmitter external clock input (TxCA). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock.
IP4	X			I	**Input 4:** General purpose input, or channel A receiver external clock input (RxCA). When the external clock is used by the receiver, the received data is sampled on the rising edge of the clock.
IP5	X			I	**Input 5:** General purpose input, or channel B transmitter external clock input (TxCB). When the external clock is used by the transmitter, the transmitted data is clocked on the falling edge of the clock.
IP6	X			I	**Input 6:** General purpose input or channel B receiver external clock input (RxCB). When the external clock is used by the receiver, the received data is sampled on the rising edge of the clock.
V_{CC}	X	X	X	I	**Power Supply:** + 5V supply input
GND	X	X	X	I	**Ground**

SN74165
PARALLEL-LOAD 8-BIT SHIFT REGISTERS

(TOP VIEW)



The '165 and 'LS165 are 8-bit serial shift registers that shift the data in the direction of Q_A toward Q_H when clocked. Parallel-in access to each stage is made available by eight individual direct data inputs that are enabled by a low level at the shift/load input. These registers also feature gated clock inputs and complementary outputs from the eighth bit. All inputs are diode-clamped to minimize transmission-line effects, thereby simplifying system design.

Clocking is accomplished through a 2-input positive-NOR gate, permitting one input to be used as a clock-inhibit function. Holding either of the clock inputs high inhibits clocking and holding either clock input low with the shift/load input high enables the other clock input. The clock-inhibit input should be changed to the high level only while the clock input is high. Parallel loading is inhibited as long as the shift/load input is high. Data at the parallel inputs are loaded directly into the register on a high-to-low transition of the shift/load input independently of the levels of the clock, clock inhibit, or serial inputs.

FUNCTION TABLE

INPUTS					INTERNAL OUTPUTS		OUTPUT
SHIFT/ LOAD	CLOCK INHIBIT	CLOCK	SERIAL	PARALLEL A . . . H	Q_A	Q_B	Q_H
L	X	X	X	a . . . h	a	b	h
H	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	H	X	X	X	Q_{A0}	Q_{B0}	Q_{H0}

SN74L90
DECADE, DIVIDE-BY-TWELVE, AND BINARY COUNTER

Each of these monolithic counters contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-five for the '90A, 'L90, and 'LS90, divide-by-six for the '92A and 'LS92, and divide-by-eight for the '93A, 'L93, and 'LS93.

All of these counters have a gated zero reset and the '90A, 'L90, and 'LS90 also have gated set-to-nine inputs for use in BCD nine's complement applications.

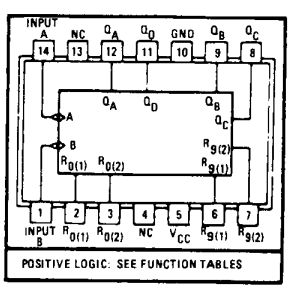
To use their maximum count length (decade, divide-by-twelve, or four-bit binary) of these counters, the B input is connected to the Q_A output. The input count pulses are applied to input A and the outputs are as described in the appropriate function table. A symmetrical divide-by-ten count can be obtained from the '90A, 'L90, or 'LS90 counters by connecting the Q_D output to the A input and applying the input count to the B input which gives a divide-by-ten square wave at output Q_A.

'90A, 'L90, 'LS90
BCD COUNT SEQUENCE
(See Note A)

COUNT	OUTPUT Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

'90A, 'L90, 'LS90
BI-QUINARY (5-2)
(See Note B)

COUNT	OUTPUT Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

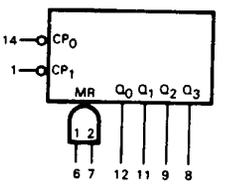


'90A, 'L90, 'LS90
RESET/COUNT FUNCTION TABLE

RESET INPUTS $R_{0(1)}$	$R_{0(2)}$	$R_{9(1)}$	$R_{9(2)}$	OUTPUT Q_D	Q_C	Q_B	Q_A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	COUNT			
L	X	L	X	COUNT			
L	X	X	L	COUNT			
X	L	L	X	COUNT			

NOTES A. Output Q_A is connected to input B for BCD count.
B. Output Q_D is connected to input A for bi-quinary count.
C. Output Q_A is connected to input B.
D. H = high level, L = low level, X = irrelevant

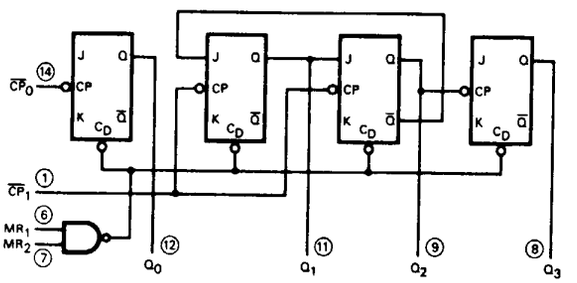
SN54LS/74LS92
DECADE COUNTER; DIVIDE-BY-TWELVE COUNTER; 4-BIT BINARY COUNTER
LOW POWER SCHOTTKY



V_{CC} = Pin 5
GND = Pin 10
NC = Pins 2, 3, 4, 13

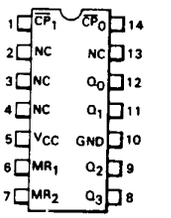
LOGIC DIAGRAM

LS92



○ = Pin Numbers
V_{CC} = Pin 5
GND = Pin 10

CONNECTION DIAGRAM
DIP (TOP VIEW)



NC = No Internal Connection

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION — The LS90, LS92, and LS93 are 4-bit ripple type Decade, Divide-By-Twelve, and Binary Counters respectively. Each device consists of four master/slave flip-flops which are internally connected to provide a divide-by-two section and a divide-by-five (LS90), divide-by-six (LS92), or divide-by-eight (LS93) section. Each section has a separate clock input which initiates state changes of the counter on the HIGH-to-LOW clock transition. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes. The Q_0 output of each device is designed and specified to drive the rated fan-out plus the $\overline{CP}_1$ input of the device.

A gated AND asynchronous Master Reset ($MR_1 \bullet MR_2$) is provided on all counters which overrides and clocks and resets (clears) all the flip-flops. A gated AND asynchronous Master Set ($MS_1 \bullet MS_2$) is provided on the LS90 which overrides the clocks and the MR inputs and sets the outputs to nine (HLLH).

Since the output from the divide-by-two section is not internally connected to the succeeding stages, the devices may be operated in various counting modes.

A. Modulo 12, Divide-By-Twelve Counter — The $\overline{CP}_1$ input must be externally connected to the Q_0 output. The $\overline{CP}_0$ input receives the incoming count and Q_3 produces a symmetrical divide-by-twelve square wave output.

B. Divide-By-Two and Divide-By-Six Counter — No external interconnections are required. The first flip-flop is used as a binary element for the divide-by-two function. The $\overline{CP}_1$ input is used to obtain divide-by-three operation at the Q_1 and Q_2 outputs and divide-by-six operation at the Q_3 output.

MODE SELECTION

RESET INPUTS		OUTPUTS			
MR_1	MR_2	Q_0	Q_1	Q_2	Q_3
H	H	L	L	L	L
L	H	Count			
H	L	Count			
L	L	Count			

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

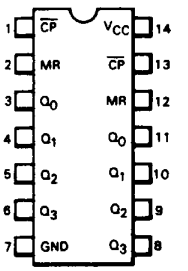
TRUTH TABLE

COUNT	OUTPUT			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	L	L	H
7	H	L	L	H
8	L	H	L	H
9	H	H	L	H
10	L	L	H	H
11	H	L	H	H

Note: Output Q_0 connected to input $\overline{CP}_1$

SN54LS/74LS393
DUAL DECADE COUNTER; DUAL 4-STAGE BINARY COUNTER
LOW POWER SCHOTTKY

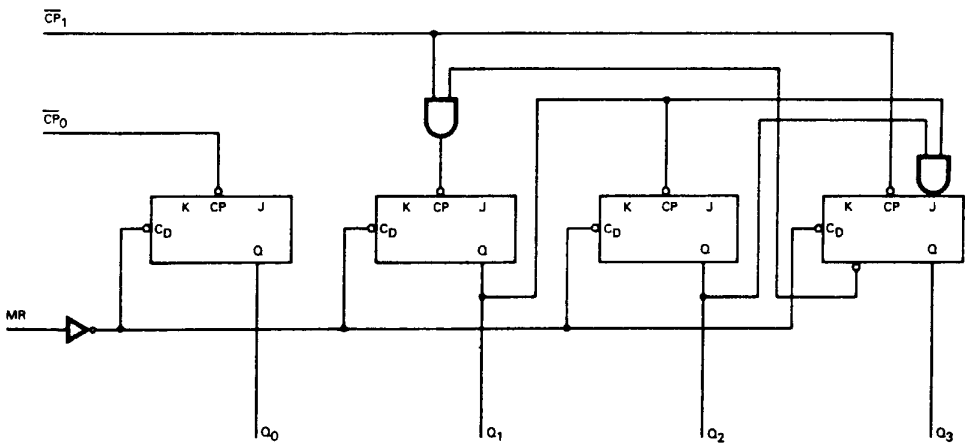
SN54LS/74LS393



J Suffix — Case 632-06 (Ceramic)
N Suffix — Case 646-05 (Plastic)

FUNCTIONAL DESCRIPTION—Each half of the SN54LS/74LS393 Operates in the Modulo 16 binary sequence, as indicated in the ÷16 Truth Table. The first flip-flop is triggered by HIGH-to-LOW transitions of the CP input signal. Each of the other flip-flops is triggered by a HIGH-to-LOW transition of the Q output of the preceding flip-flop. Thus state changes of the Q outputs do not occur simultaneously. This means that logic signals derived from combinations of these outputs will be subject to decoding spikes and, therefore, should not be used as clocks for other counters, registers or flip-flops. A HIGH signal on MR forces all outputs to the LOW state and prevents counting.

SN54LS/74LS393 LOGIC DIAGRAM (one half shown)



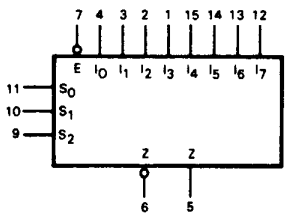
SN54LS/74LS393
TRUTH TABLE

COUNT	OUTPUTS			
	Q_3	Q_2	Q_1	Q_0
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

H = HIGH Voltage Level
L = LOW Voltage Level

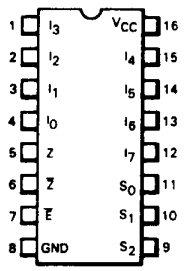
SN54LS151/SN74LS151
8-INPUT MULTIPLEXER
LOW POWER SCHOTTKY

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



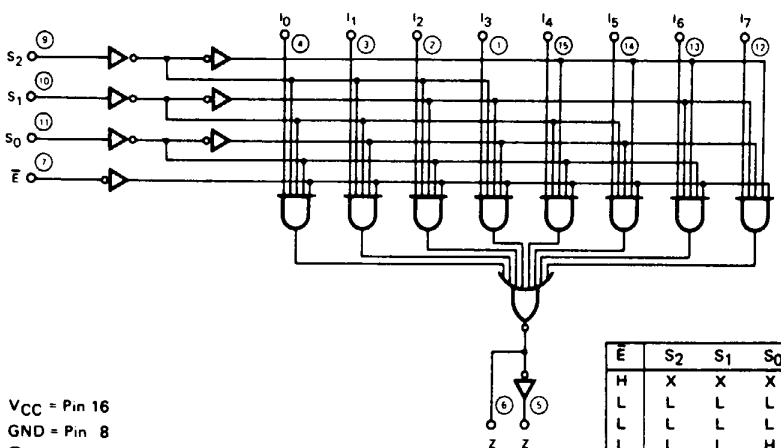
J Suffix — Case 620-06
(Ceramic)
N Suffix — Case 648-05
(Plastic)

FUNCTIONAL DESCRIPTION — The LS151 is a logical implementation of a single pole, 8-position switch with the switch position controlled by the state of three Select inputs, S_0, S_1, S_2. Both assertion and negation outputs are provided. The Enable input (E) is active LOW. When it is not activated, the negation output is HIGH and the assertion output is LOW regardless of all other inputs. The logic function provided at the output is:

$$Z = \overline{E} \cdot (I_0 \cdot \overline{S}_0 \cdot \overline{S}_1 \cdot \overline{S}_2 + I_1 \cdot S_0 \cdot \overline{S}_1 \cdot \overline{S}_2 + I_2 \cdot \overline{S}_0 \cdot S_1 \cdot \overline{S}_2 + I_3 \cdot S_0 \cdot S_1 \cdot \overline{S}_2 + I_4 \cdot \overline{S}_0 \cdot \overline{S}_1 \cdot S_2 + I_5 \cdot S_0 \cdot \overline{S}_1 \cdot S_2 + I_6 \cdot \overline{S}_0 \cdot S_1 \cdot S_2 + I_7 \cdot S_0 \cdot S_1 \cdot S_2).$$

The LS151 provides the ability, in one package, to select from eight sources of data or control information. By proper manipulation of the inputs, the LS151 can provide any logic function of four variables and its negation.

LOGIC DIAGRAM



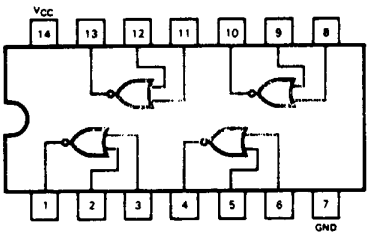
V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

TRUTH TABLE

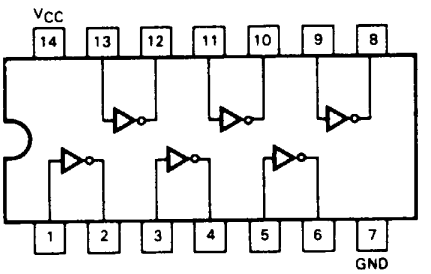
$\overline{E}$	S_2	S_1	S_0	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	$\overline{Z}$	Z
H	X	X	X	X	X	X	X	X	X	X	X	H	L
L	L	L	L	L	X	X	X	X	X	X	X	H	L
L	L	L	L	H	X	X	X	X	X	X	X	L	H
L	L	L	H	X	L	X	X	X	X	X	X	H	L
L	L	L	H	X	H	X	X	X	X	X	X	L	H
L	L	H	L	X	X	L	X	X	X	X	X	H	L
L	L	H	L	X	X	H	X	X	X	X	X	L	H
L	L	H	H	X	X	X	L	X	X	X	X	H	L
L	L	H	H	X	X	X	H	X	X	X	X	L	H
L	H	L	L	X	X	X	X	L	X	X	X	H	L
L	H	L	L	X	X	X	X	H	X	X	X	L	H
L	H	L	H	X	X	X	X	X	L	X	X	H	L
L	H	L	H	X	X	X	X	X	H	X	X	L	H
L	H	H	L	X	X	X	X	X	X	L	X	H	L
L	H	H	L	X	X	X	X	X	X	H	X	L	H
L	H	H	H	X	X	X	X	X	X	X	L	H	L
L	H	H	H	X	X	X	X	X	X	X	H	L	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

SN54LS02/SN74LS02
QUAD 2-INPUT NOR GATE
LOW POWER SCHOTTKY

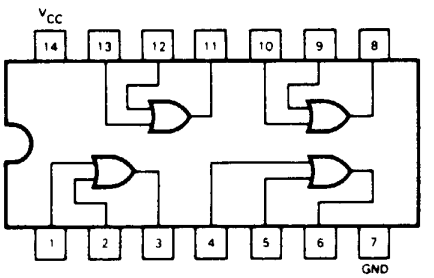


SN54LS04/SN74LS04
HEX INVERTER
LOW POWER SCHOTTKY



J Suffix — Case 632-06 (Ceramic)
N Suffix — Case 646-05 (Plastic)

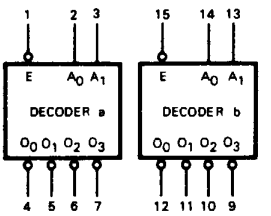
SN54LS32/SN74LS32
QUAD 2-INPUT OR GATE
LOW POWER SCHOTTKY



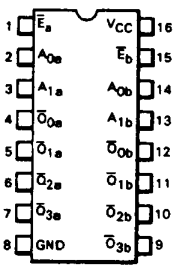
J Suffix — Case 632-06 (Ceramic)
N Suffix — Case 646-05 (Plastic)

SN54LS139/SN74LS139
DUAL 1-OF-4 DECODER/DEMULTIPLEXER
LOW POWER SCHOTTKY

LOGIC SYMBOL



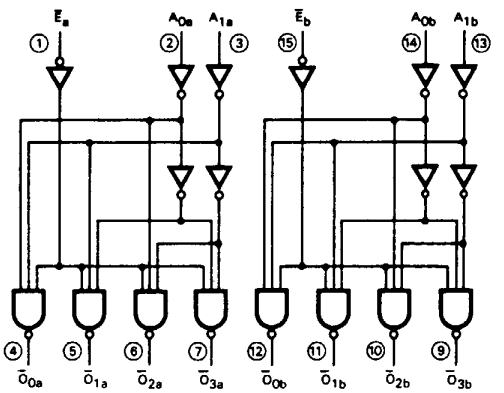
CONNECTION DIAGRAM
DIP (TOP VIEW)



J Suffix — Case 620-06
(Ceramic)
N Suffix — Case 648-05
(Plastic)

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

LOGIC DIAGRAM



VCC = Pin 16
GND = Pin 8
○ = Pin Numbers

VCC = Pin 16
GND = Pin 8

FUNCTIONAL DESCRIPTION — The LS139 is a high speed dual 1-of-4 decoder/demultiplexer fabricated with the Schottky barrier diode process. The device has two independent decoders, each of which accept two binary weighted inputs (A_0, A_1) and provide four mutually exclusive active LOW outputs ($\overline{O}_0$-$\overline{O}_3$). Each decoder has an active LOW Enable ($\overline{E}$). When $\overline{E}$ is HIGH all outputs are forced HIGH. The enable can be used as the data input for a 4-output demultiplexer application.

Each half of the LS139 generates all four minterms of two variables. These four minterms are useful in some applications, replacing multiple gate functions as shown in Fig. a, and thereby reducing the number of packages required in a logic network.

TRUTH TABLE

INPUTS			OUTPUTS			
$\overline{E}$	A_0	A_1	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

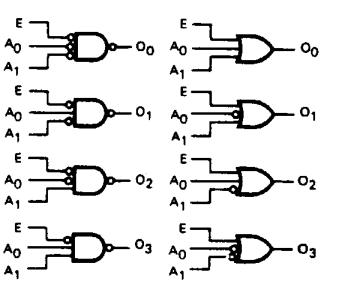


Fig. a

SN54LS245/SN74LS245
OCTAL BUS TRANSCEIVER
LOW POWER SCHOTTKY

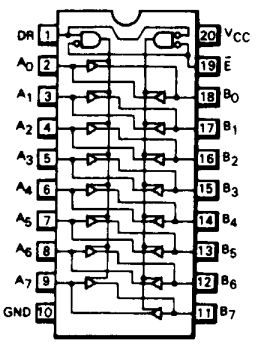
DESCRIPTION — The SN54LS/74LS245 is an Octal Bus Transmitter/Receiver designed for 8-line asynchronous 2-way data communication between data buses. Direction Input (DR) controls transmission of Data from bus A to bus B or bus B to bus A depending upon its logic level. The Enable input ($\overline{E}$) can be used to isolate the buses.

TRUTH TABLE

INPUTS		OUTPUT
$\overline{E}$	DR	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	Isolation

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

LOGIC AND CONNECTION DIAGRAM
DIP (TOP VIEW)

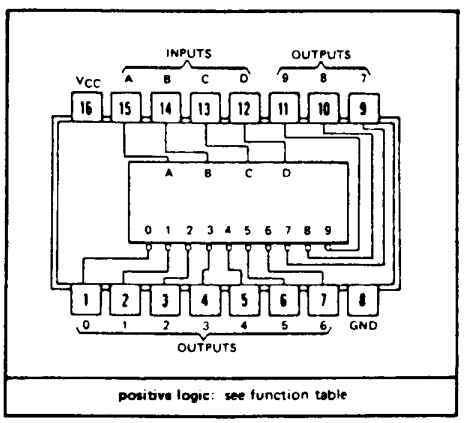


J Suffix — Case 732-03 (Ceramic)
N Suffix — Case 738-01 (Plastic)

SN74LS42
4-LINE-TO-10-LINE DECODERS (1-OF-10)

These monolithic decimal decoders consist of eight inverters and ten four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid input logic ensures that all outputs remain off for all invalid input conditions.

The '42A, 'L42, and 'LS42 BCD-to-decimal decoders, the '43A and 'L43 excess-3-to-decimal decoders, and the '44A and 'L44 excess-3-gray-to-decimal decoders feature inputs and outputs that are compatible for use with most TTL and other saturated low-level logic circuits. D-c noise margins are typically one volt.



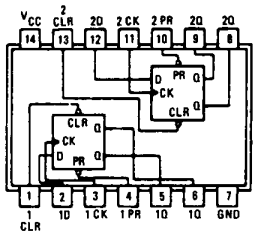
positive logic: see function table

ALL TYPES DECIMAL OUTPUT									
0	1	2	3	4	5	6	7	8	9
L	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H
H	H	H	L	H	H	H	H	H	H
H	H	H	H	L	H	H	H	H	H
H	H	H	H	H	L	H	H	H	H
H	H	H	H	H	H	L	H	H	H
H	H	H	H	H	H	H	L	H	H
H	H	H	H	H	H	H	H	L	H
H	H	H	H	H	H	H	H	H	L
H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H

SN74LS74N
DUAL D-TYPE POSITIVE EDGE TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

FUNCTION TABLE

INPUTS				OUTPUTS	
PRESET	CLEAR	CLOCK	D	Q	$\bar{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\bar{Q}_0$

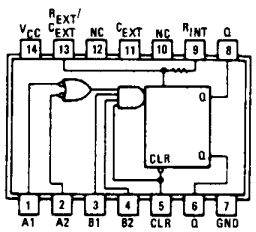


SN74LS122
RETRIGGERABLE MONOSTABLE MULTIVIBRATORS WITH CLEAR

FUNCTION TABLE

INPUTS					OUTPUTS	
CLEAR	A1	A2	B1	B2	Q	$\bar{Q}$
L	X	X	X	X	L	H
X	H	H	X	X	L	H
X	X	X	L	X	L	H
X	X	X	X	L	L	H
H	L	X	↑	H	⎍	⎎
H	L	X	H	↑	⎍	⎎
H	X	L	↑	H	⎍	⎎
H	X	L	H	↑	⎍	⎎
H	H	↓	H	H	⎍	⎎
H	↓	↓	H	H	⎍	⎎
H	↓	H	H	H	⎍	⎎
↑	L	X	H	H	⎍	⎎
↑	X	L	H	H	⎍	⎎

NOTES:
1. AN EXTERNAL TIMING CAPACITOR MAY BE CONNECTED BETWEEN C_{EXT} AND R_{EXT}/C_{EXT} (POSITIVE).
2. FOR ACCURATE REPEATABLE PULSE WIDTHS, CONNECT AN EXTERNAL RESISTOR BETWEEN R_{EXT}/C_{EXT} AND V_{CC} WITH R_{INT} OPEN-CIRCUITED.

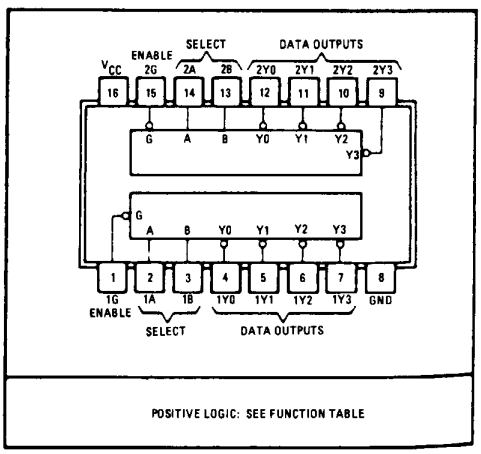


SN54122 (J, W) **SN74122 (J, N)**
SN54L122 (J, T) **SN74L122 (J, N)**
SN54LS122 (J, W) **SN74LS122 (J, N)**
'122 . . . R_{int} = 10 kΩ NOM
'L122 . . . R_{int} = 20 kΩ NOM
'LS122 . . . R_{int} = 10 kΩ NOM

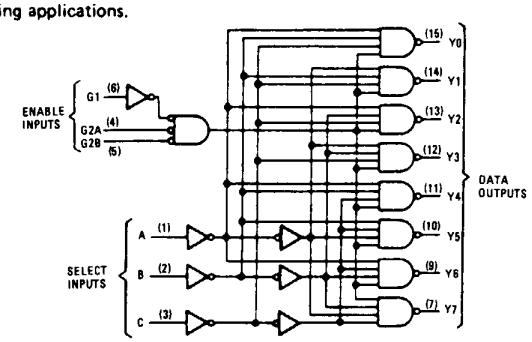
SN74LS138
DECODER/DEMULTIPLEXER

These Schottky-clamped TTL MSI circuits are designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems these decoders can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast-enable circuit the delay times of these decoders and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the Schottky-clamped system decoder is negligible.

The 'LS138 and 'S138 decode one-of-eight lines dependent on the conditions at the three binary select inputs and the three enable inputs. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.



'LS138, 'S138



'LS138, 'S138
FUNCTION TABLE

INPUTS					OUTPUTS							
ENABLE		SELECT										
G1	G2*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

G2 = G2A + G2B
H = HIGH LEVEL, L = LOW LEVEL, X = IRRELEVANT

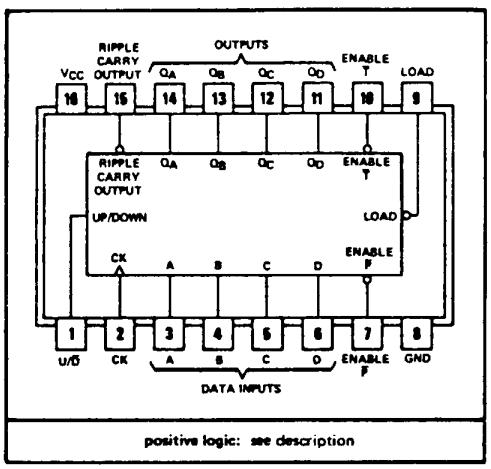
SN74LS168A
SYNCHRONOUS 4-BIT UP/DOWN COUNTERS

Programmable Look-Ahead Up/Down Binary/Decade Counters

- Fully Synchronous Operation for Counting and Programming
- Internal Look-Ahead for Fast Counting
- Carry Output for n-Bit Cascading
- Fully Independent Clock Circuit

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY		TYPICAL POWER DISSIPATION
	COUNTING UP	COUNTING DOWN	
'LS168A, 'LS169A	35 MHz	35 MHz	100 mW
'S168, 'S169	70 MHz	55 MHz	500 mW

(TOP VIEW)



description

These synchronous presettable counters feature an internal carry look-ahead for cascading in high-speed counting applications. The 'LS168A and 'S168 are decade counters and the 'LS169A and 'S169 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation helps eliminate the output counting spikes that are normally associated with asynchronous (ripple-clock) counters. A buffered clock input triggers the four master-slave flip-flops on the rising (positive-going) edge of the clock waveform.

These counters are fully programmable; that is, the outputs may each be preset to either level. The load input circuitry allows loading with the carry-enable output of cascaded counters. As loading is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the data inputs after the next clock pulse.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a carry output. Both count enable inputs ($\overline{P}$ and $\overline{T}$) must be low to count. The direction of the count is determined by the level of the up/down input. When the input is high, the counter counts up; when low, it counts down. Input $\overline{T}$ is fed forward to enable the carry output. The carry output thus enabled will produce a low-level output pulse with a duration approximately equal to the high portion of the Q_A output when counting up and approximately equal to the low portion of the Q_A output when counting down. This low-level overflow carry pulse can be used to enable successive cascaded stages. Transitions at the enable $\overline{P}$ or $\overline{T}$ inputs are allowed regardless of the level of the clock input. All inputs are diode-clamped to minimize transmission-line effects, thereby simplifying system design.

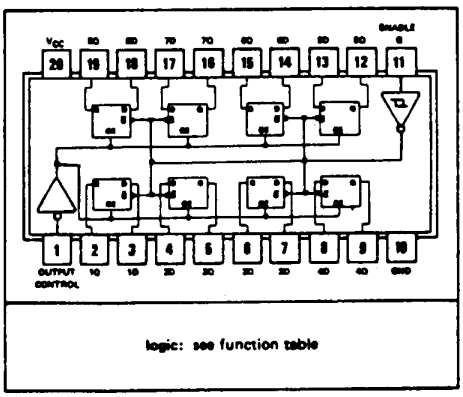
These counters feature a fully independent clock circuit. Changes at control inputs (enable $\overline{P}$, enable $\overline{T}$, load, up/down) that will modify the operating mode have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

The 'LS168A and 'LS169A are completely new designs. Compared to the original 'LS168 and 'LS169, they feature 0-nanosecond minimum hold time and reduced input currents I_{IH} and I_{IL}.

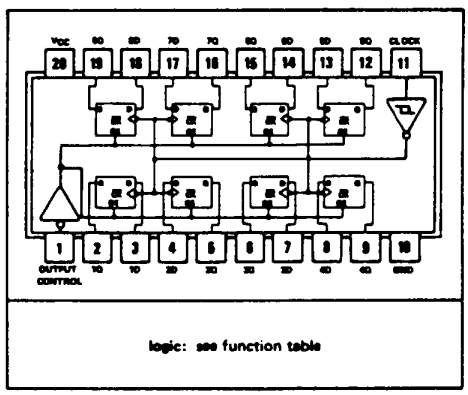
SN74LS373, SN74LS374
OCTAL D-TYPE TRANSPARENT LATCHES AND EDGE-TRIGGERED FLIP-FLOPS

These 8-bit registers feature totem-pole three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the 'LS373 and 'S373 are transparent D-type latches meaning that while the enable (G) is high the Q outputs will follow the data (D) inputs. When the enable is taken low the output will be latched at the level of the data that was setup.



logic: see function table



logic: see function table

'LS373, 'S373
FUNCTION TABLE

OUTPUT CONTROL	ENABLE G	D	OUTPUT
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

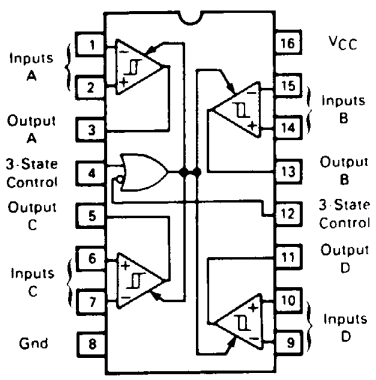
'LS374, 'S374
FUNCTION TABLE

OUTPUT CONTROL	CLOCK	D	OUTPUT
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

SN75173
QUAD RS-485 LINE RECEIVER WITH 3-STATE OUTPUTS

PIN CONNECTIONS

SN75173



SN75173

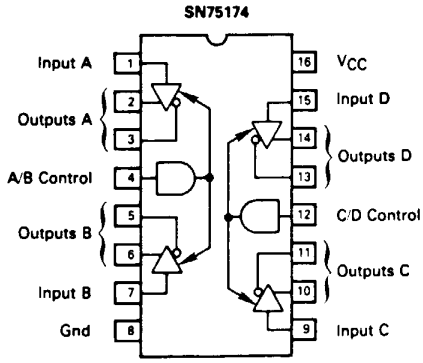
FUNCTION TABLE (EACH RECEIVER)

Differential Inputs	3-State Control		Output Y
	4	12	
$V_{ID} \geq 0.2$ V	H	X	H
	X	L	H
-0.2 V < V_{ID} < 0.2 V	H	X	?
	X	L	?
$V_{ID} \leq$ -0.2 V	H	X	L
	X	L	L
X	L	H	Z

SN75174
QUAD RS-485 LINE DRIVER WITH 3-STATE OUTPUTS

PIN CONNECTIONS

SN75174



SN75174

TRUTH TABLE			
Input	Control Input	Noninverting Output	Inverting Output
H	H	H	L
L	H	L	H
X	L	Z	Z

L = Low Logic State
H = High Logic State
X = Irrelevant
Z = Third-State (High Impedance)

SP8629
150 MHz ÷ 100

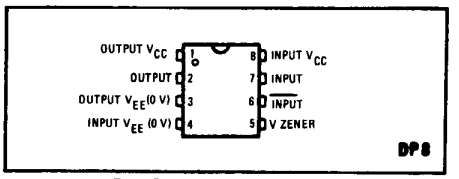
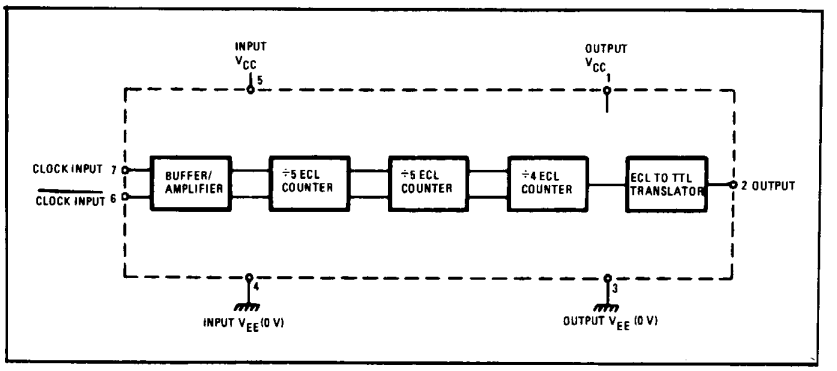
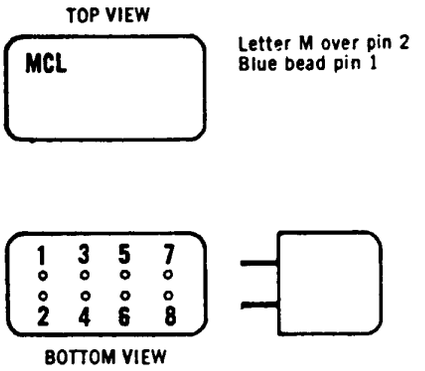


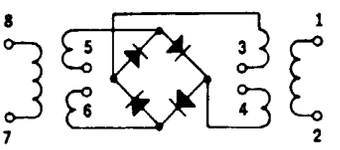
Fig.1 Pin connections - top view



SRA-1
STANDARD LEVEL (+7 DBM LO)
DOUBLE-BALANCED MIXERS

CONNECTIONS

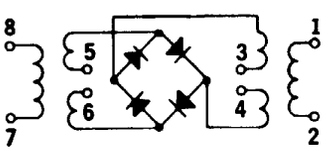


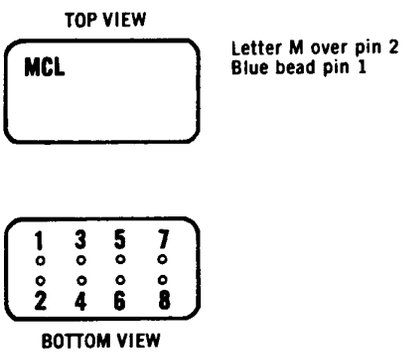


PIN LAYOUT

	Fig. 1
Model No.	-1 -1-1 -3 -1TX
LO	8
RF	1
IF	3,4
Ground	2,5,6,7
Case Ground	2

SRA-1H
0.5 MHz - 500 MHz
HIGH LEVEL (+17 dBm LO)
DOUBLE-BALANCED MIXERS





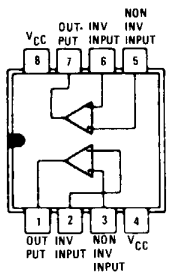
PIN LAYOUT

LO	8
RF	1
IF	3,4
Ground	2,5,6,7
Case Ground	2

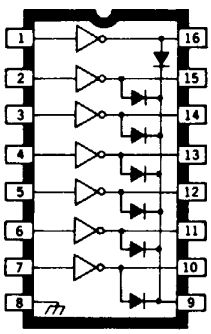
TL072
LOW-NOISE JFET-INPUT OPERATIONAL AMPLIFIERS

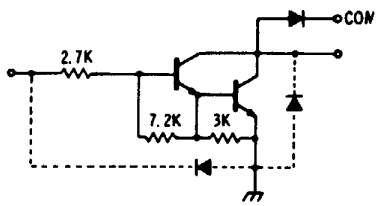
description

The JFET-input operational amplifiers of the TL071 series are designed as low-noise versions of the TL081 series amplifiers with low input bias and offset currents and fast slew rate. The low harmonic distortion and low noise make the TL071 series ideally suited as amplifiers for high-fidelity and audio preamplifier applications. Each amplifier features JFET-inputs (for high input impedance) coupled with bipolar output stages all integrated on a single monolithic chip.

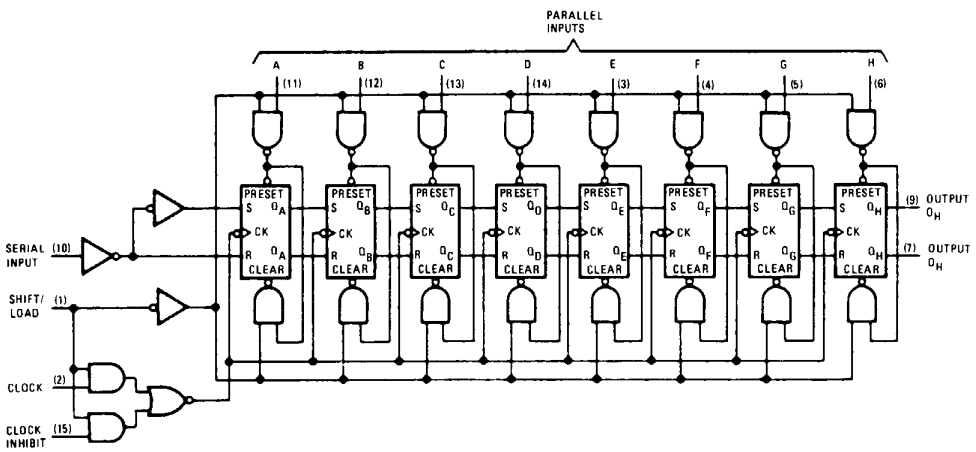


SERIES ULN-2000A
HIGH-VOLTAGE, HIGH-CURRENT
DARLINGTON TRANSISTOR ARRAYS





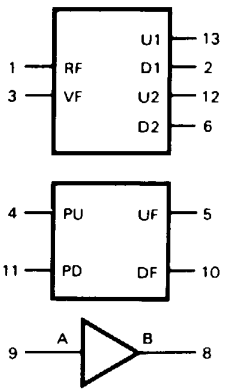
Series ULN-2003A
(each driver)



11C44
PHASE/FREQUENCY DETECTOR

GENERAL DESCRIPTION — The 11C44 contains a Phase/Frequency Detector, a Phase Detector, a Charge Pump, and an Amplifier. The Phase/Frequency Detector accepts TTL signals representing a Reference Frequency (RF) and a Variable Frequency (VF), compares the relative timing of their negative going transitions, and generates either an UP (U1) or a DOWN (D1) signal whose duration is equal to the RF-VF timing difference. When the RF and VF signals have the same frequency, the Phase Detector outputs U2 and D2 provide binary signals whose duty cycles are proportional to the phase angle between RF and VF. The Charge Pump can be driven from U1 and D1 or U2 and D2, and has three possible output states representing CHARGE, DISCHARGE, and HOLD instructions when applied to an integrator. The Amplifier is a Darlington transistor with grounded emitter and uncommitted collector and base. The 11C44 thus contains several of the functional elements used in phase-locked loop applications. It is pin compatible with the Motorola MC4044/4344, but has better discrimination capability for small phase differences.

LOGIC SYMBOL

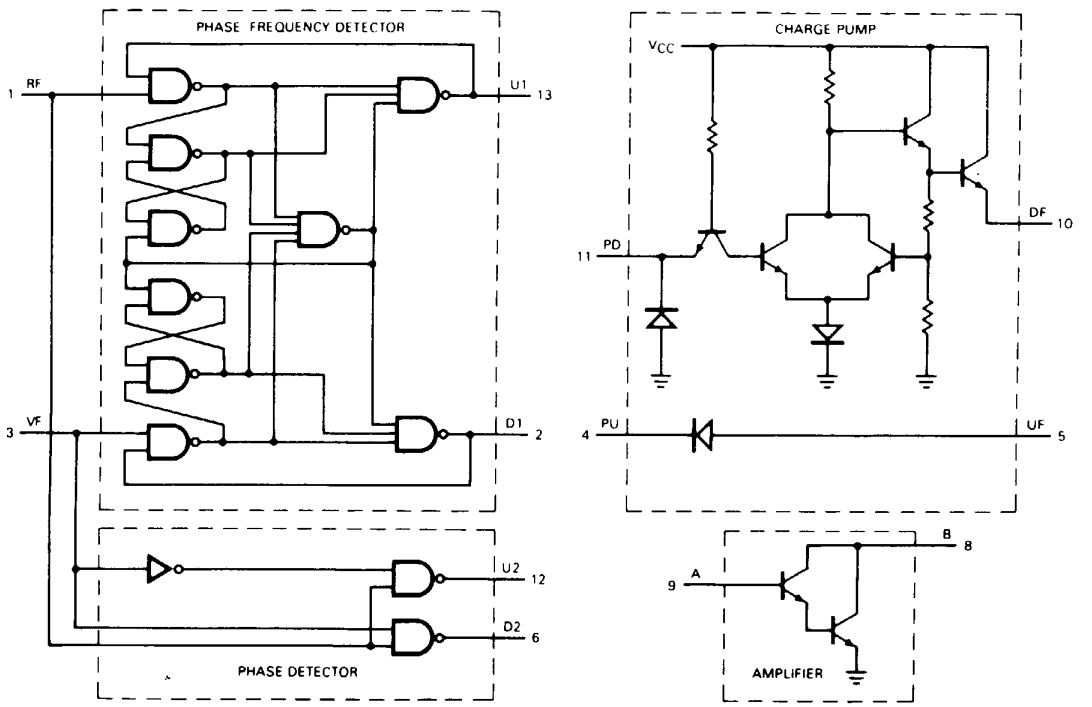


V_{CC} = Pin 14
GND = Pin 7

FUNCTIONS

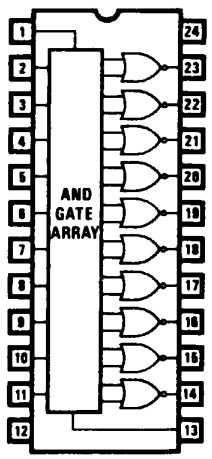
RF — Reference Frequency Input
VF — Variable Frequency Input
U1, D1 — Phase/Frequency Detector Outputs
U2, D2 — Phase Detector Outputs
PU, PD — Charge Pump Inputs
UF, DF — Charge Pump Outputs
A — Amplifier Input
B — Amplifier Output

LOGIC DIAGRAM AND SCHEMATIC



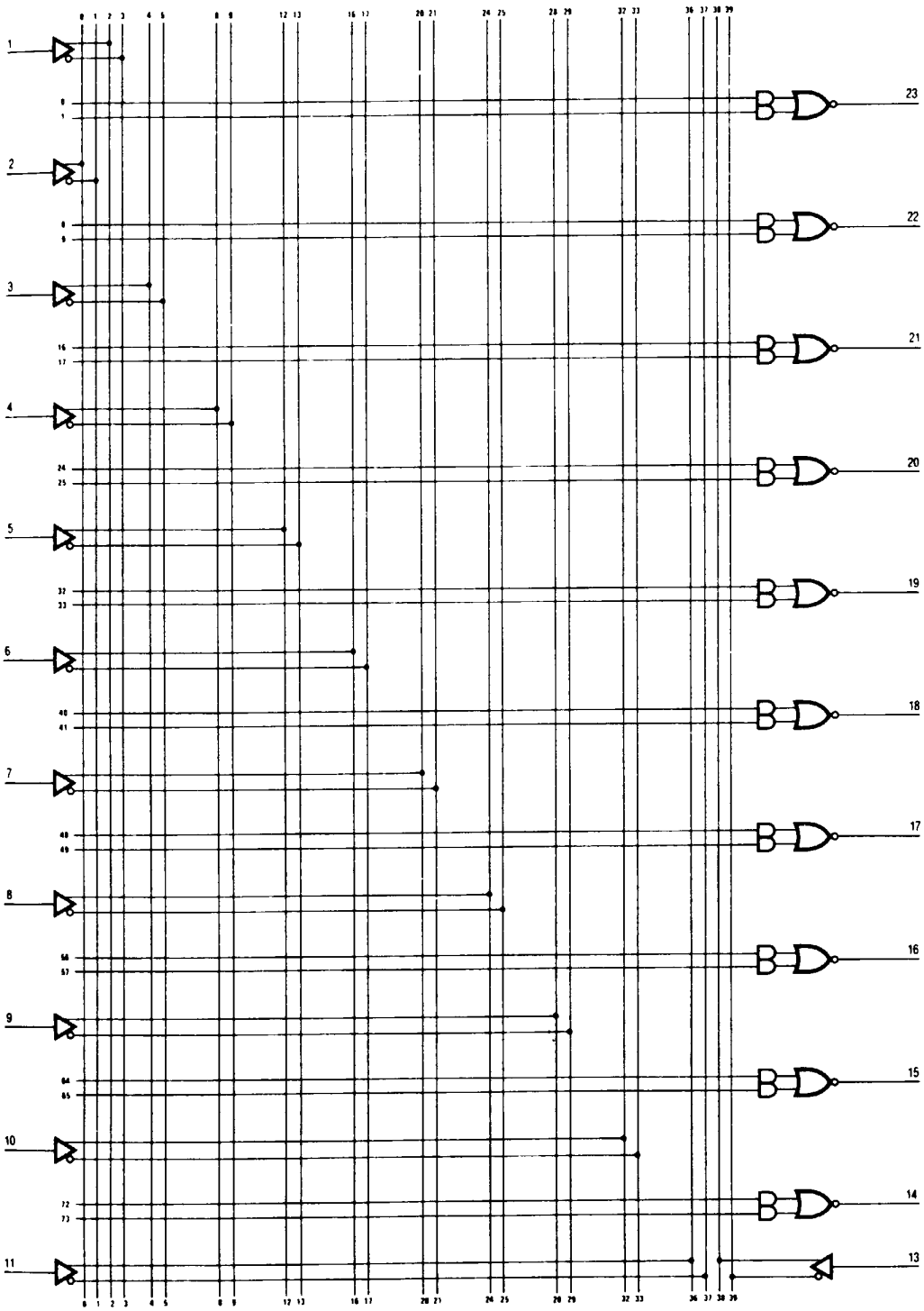
12L10
PROGRAMMABLE ARRAY LOGIC (PAL)

Logic Symbol
12L10



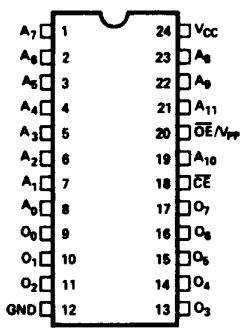
DECA 12 INPUT
AND-OR-INVERT GATE ARRAY

Logic Diagram



27C 32
32K (4K X 8) UV ERASABLE PROM

PIN CONFIGURATION



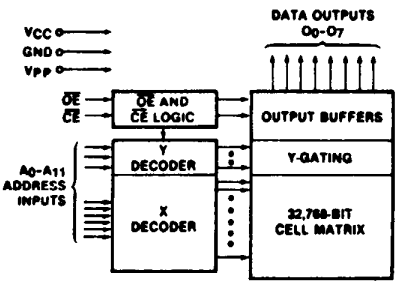
MODE SELECTION

MODE \ PINS	$\overline{CE}$ (18)	$\overline{OE}/V_{PP}$ (20)	V_{CC} (24)	OUTPUTS (9-11,13-17)
Read	V_{IL}	V_{IL}	+5	D_{OUT}
Standby	V_{IH}	Don't Care	+5	High Z
Program	V_{IL}	V_{PP}	+5	D_{IN}
Program Verify	V_{IL}	V_{IL}	+5	D_{OUT}
Program Inhibit	V_{IH}	V_{PP}	+5	High Z

PIN NAMES

A_0-A_{11}	ADDRESSES
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
O_0-O_7	OUTPUTS

BLOCK DIAGRAM



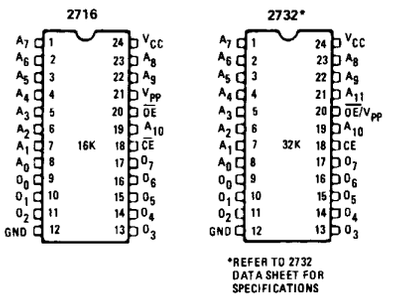
2716
16K (2K x 8) UV ERASABLE PROM

The Intel® 2716 is a 16,384-bit ultraviolet erasable and electrically programmable read-only memory (EPROM). The 2716 operates from a single 5-volt power supply, has a static standby mode, and features fast single address location programming. It makes designing with EPROMs faster, easier and more economical.

The 2716, with its single 5-volt supply and with an access time up to 350 ns, is ideal for use with the newer high performance +5V microprocessors such as Intel's 8085 and 8086. The 2716 is also the first EPROM with a static standby mode which reduces the power dissipation without increasing access time. The maximum active power dissipation is 525 mW while the maximum standby power dissipation is only 132 mW, a 75% savings.

The 2716 has the simplest and fastest method yet devised for programming EPROMs – single pulse TTL level programming. No need for high voltage pulsing because all programming controls are handled by TTL signals. Program any location at any time—either individually, sequentially or at random, with the 2716's single address location programming. Total programming time for all 16,384 bits is only 100 seconds.

PIN CONFIGURATION



*REFER TO 2732 DATA SHEET FOR SPECIFICATIONS

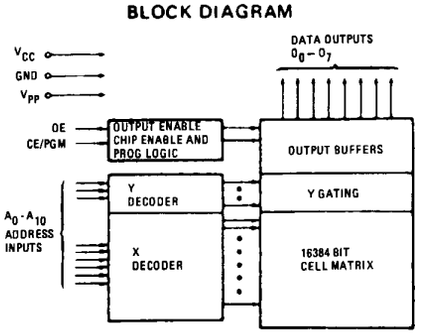
MODE SELECTION

MODE \ PINS	$\overline{CE}$/PGM (18)	$\overline{OE}$ (20)	V_{PP} (21)	V_{CC} (24)	OUTPUTS (9-11, 13-17)
READ	V_{IL}	V_{IL}	+5	+5	D_{OUT}
STANDBY	V_{IH}	DON'T CARE	+5	+5	HIGH Z
PROGRAM	PULSED V_{IL} TO V_{IH}	V_{IH}	+25	+5	D_{IN}
PROGRAM VERIFY	V_{IL}	V_{IL}	+25	+5	D_{OUT}
PROGRAM INHIBIT	V_{IL}	V_{IH}	+25	+5	HIGH Z

PIN NAMES

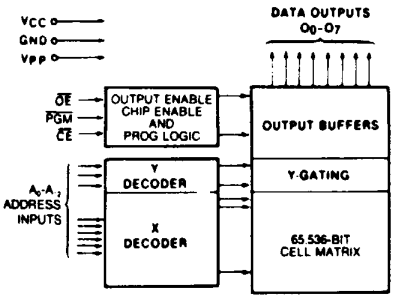
$A_0 - A_{10}$	ADDRESSES
$\overline{CE}$/PGM	CHIP ENABLE/PROGRAM
$\overline{OE}$	OUTPUT ENABLE
$O_0 - O_7$	OUTPUTS

BLOCK DIAGRAM



2764
(8K X 8) UV ERASABLE PROM

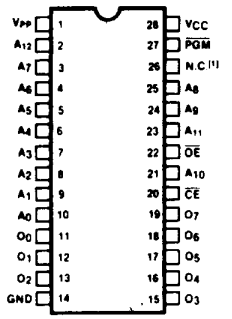
BLOCK DIAGRAM



PIN NAMES

A_0-A_{12}	ADDRESSES
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
O_0-O_7	OUTPUTS
$\overline{PGM}$	PROGRAM
N.C	NO CONNECT

2764
PIN CONFIGURATION



DEVICE OPERATION

The five modes of operation of the 2764 are listed in Table 1. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP}.

TABLE 1. MODE SELECTION

MODE \ PINS	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{PGM}$ (27)	V_{PP} (1)	V_{CC} (28)	Outputs (11-13, 15-19)
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	D_{OUT}
Standby	V_{IH}	x	x	V_{CC}	V_{CC}	High Z
Program	V_{IL}	x	V_{IL}	V_{PP}	V_{CC}	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	D_{OUT}
Program Inhibit	V_{IH}	x	x	V_{PP}	V_{CC}	High Z

x can be either V_{IL} or V_{IH}

READ MODE

The 2764 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output ($t_{\overline{CE}}$). Data is available at the outputs after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

Standby Mode

The 2764 has a standby mode which reduces the active power current from 150mA to 50mA. The 2764 is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output OR-Tieing

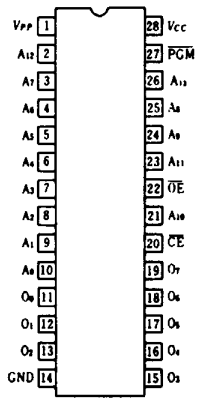
Because EPROMs are usually used in larger memory arrays, Intel has provided a 2 line control function that accommodates this use of multiple memory connection. The two line control function allows for:

a) the lowest possible memory power dissipation, and
b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ (pin 20) be decoded and used as the primary device selecting function, while $\overline{OE}$ (pin 22) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is desired from a particular memory device.

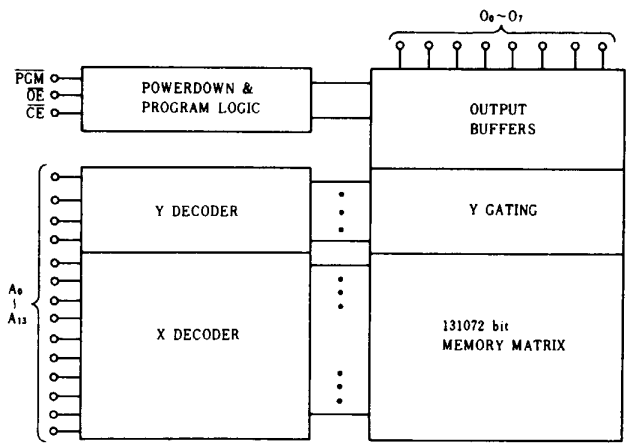
27128
(16K x 8) UV ERASABLE PROM

■PIN ARRANGEMENT



(Top View)

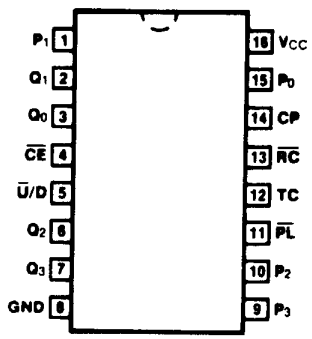
■BLOCK DIAGRAM



54F/74F191
UP/DOWN BINARY COUNTER
(WITH PRESET AND RIPPLE CLOCK)

Pin Names	Description
$\overline{CE}$	Count Enable Input (Active LOW)
CP	Clock Pulse Input (Active Rising Edge)
$P_0 - P_3$	Parallel Data Inputs
$\overline{PL}$	Asynchronous Parallel Load Input (Active LOW)
$\overline{U}/D$	Up/Down Count Control Input
$Q_0 - Q_3$	Flip-flop Outputs
$\overline{RC}$	Ripple Clock Output (Active LOW)
TC	Terminal Count Output (Active HIGH)

Connection Diagram



Mode Select Table

INPUTS				MODE
$\overline{PL}$	$\overline{CE}$	$\overline{U}/D$	CP	
H	L	L	⌐¬	Count Up
H	L	H	⌐¬	Count Down
L	X	X	X	Preset (Asyn.)
H	H	X	X	No Change (Hold)

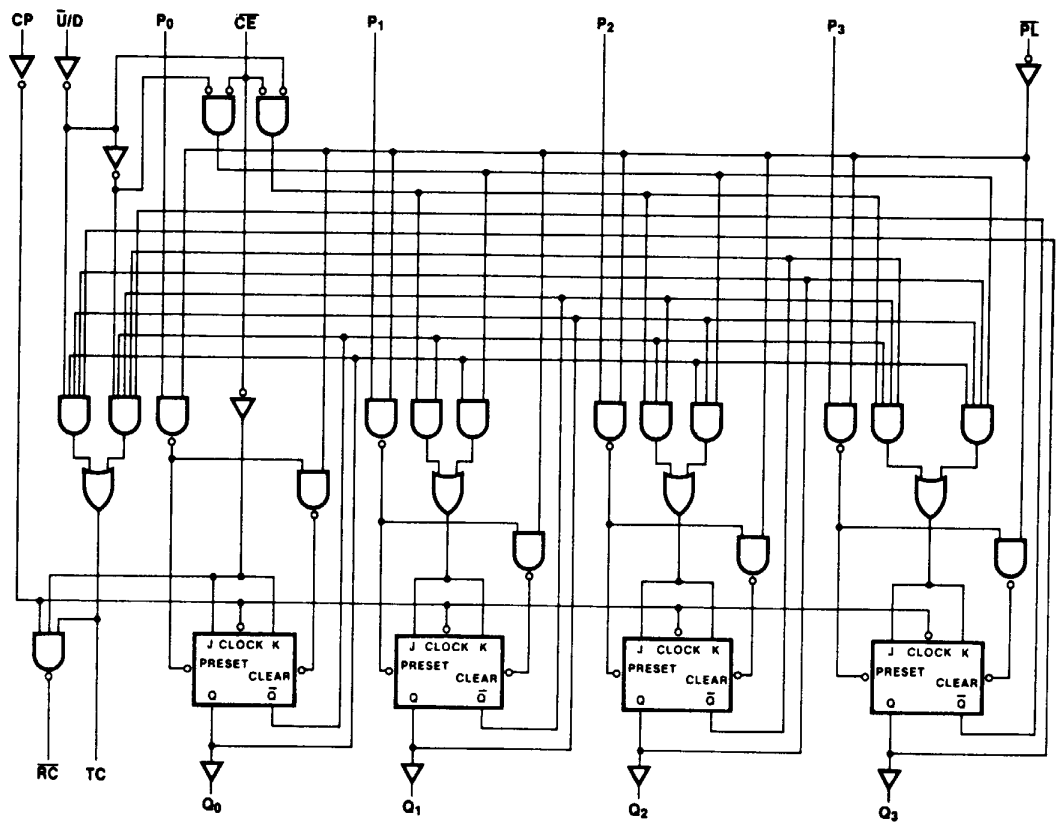
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

$\overline{RC}$ Truth Table

INPUTS			OUTPUT
$\overline{CE}$	TC*	CP	$\overline{RC}$
L	H	⌐¬	⌐¬
H	X	X	H
X	L	X	H

*TC is generated internally

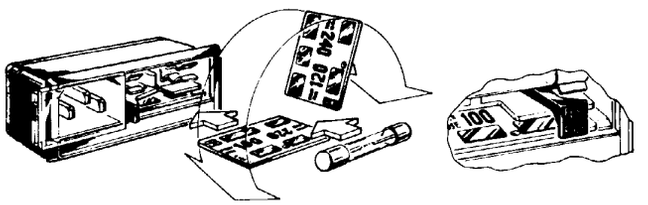
Logic Diagram

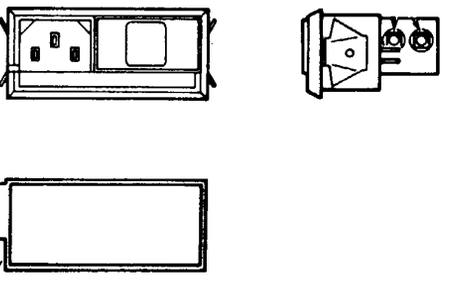


Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

CORCOM
J SERIES
VOLTAGE SELECTING AND FUSED CONNECTOR
6J4

Voltage Selection

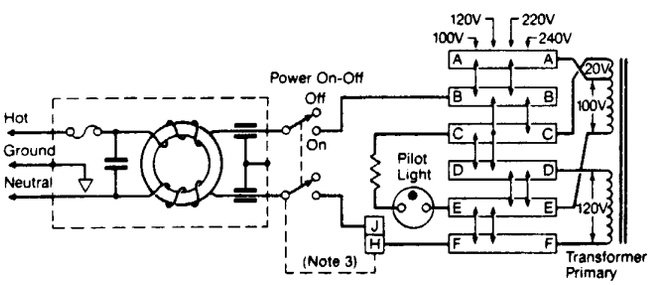




Open cover door and rotate fuse pull to left.

Select operating voltage by orienting PC Board to position desired voltage on top left side. Push board firmly into module slot.

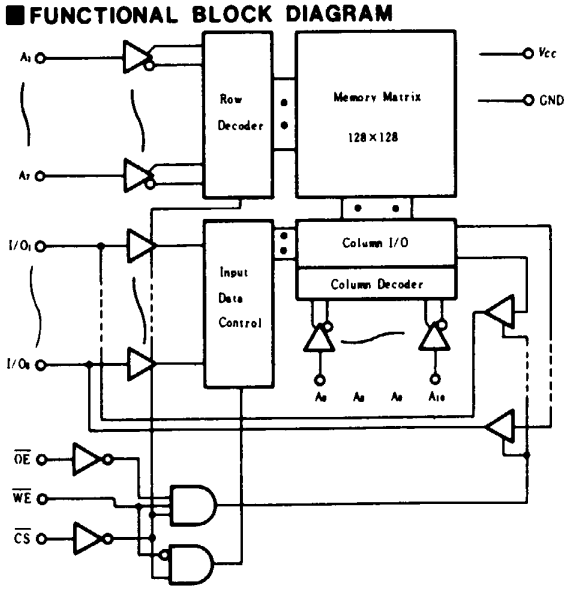
Rotate fuse-pull back into normal position and re-insert fuse into holders, using caution to select correct fuse value.



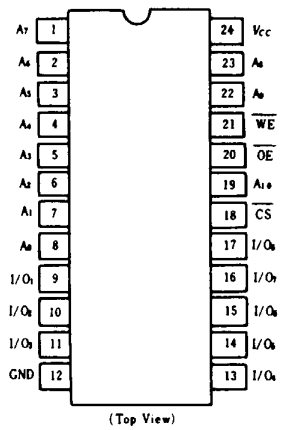
Note 3: Jumper required if only SPST Power Switch is used.
Note 4: Jumpers required if no input filtering is used.

6116
(2K x 8) HIGH SPEED STATIC CMOS RAM

■ FUNCTIONAL BLOCK DIAGRAM



■ PIN ARRANGEMENT



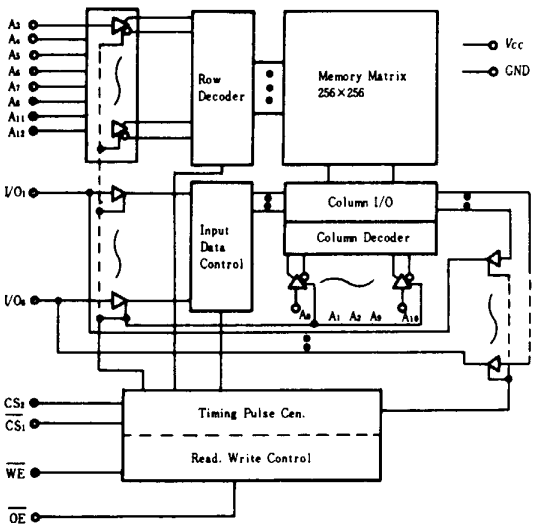
(Top View)

■ TRUTH TABLE

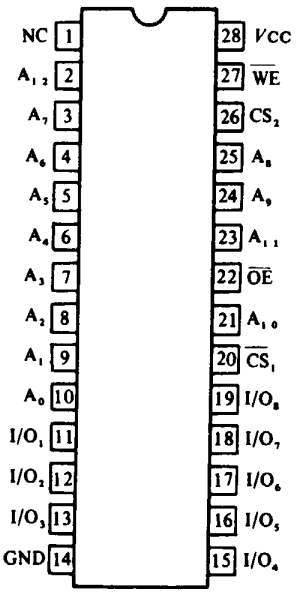
$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode
H	×	×	Not Selected
L	L	H	Read
L	H	L	Write
L	L	L	Write

6264
(8K x 8) HIGH SPEED STATIC CMOS RAM

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

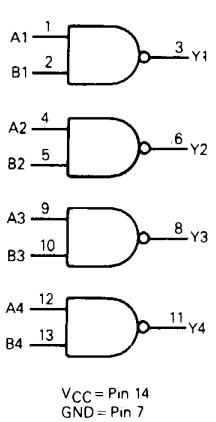
■ TRUTH TABLE

$\overline{WE}$	$\overline{CS_1}$	CS_2	$\overline{OE}$	Mode
X	H	X	X	Not Selected (Power Down)
X	X	L	X	
H	L	H	H	Output Disabled
H	L	H	L	Read
L	L	H	H	Write
L	L	H	L	

X: H or L

74HC00
QUAD 2 INPUT NAND GATE

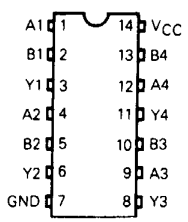
LOGIC DIAGRAM



$Y = \overline{AB}$

V_{CC} = Pin 14
GND = Pin 7

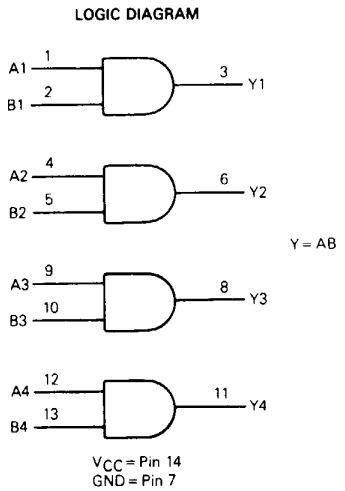
PIN ASSIGNMENT



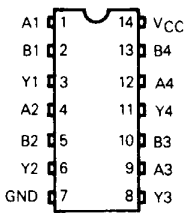
This document contains information on a new product. Specifications and information herein are subject to change without notice.

74HC08
QUAD 2 INPUT AND GATE

LOGIC DIAGRAM

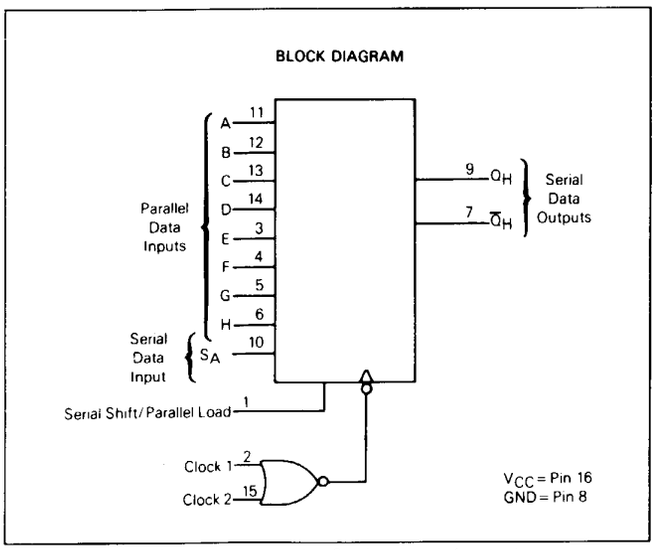


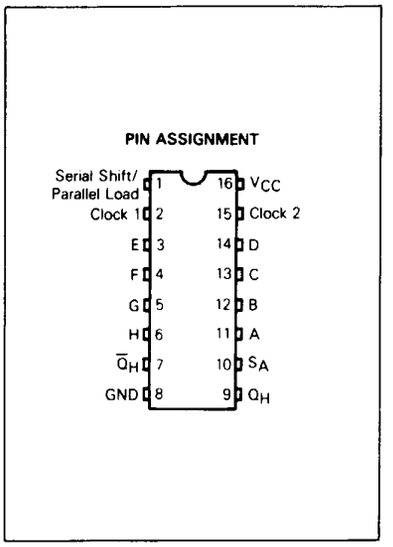
PIN ASSIGNMENT



This document contains information on a new product. Specifications and information herein are subject to change without notice.

74HC165
8 BIT SERIAL OR PARALLEL-INPUT/SERIAL-OUTPUT SHIFT REGISTER





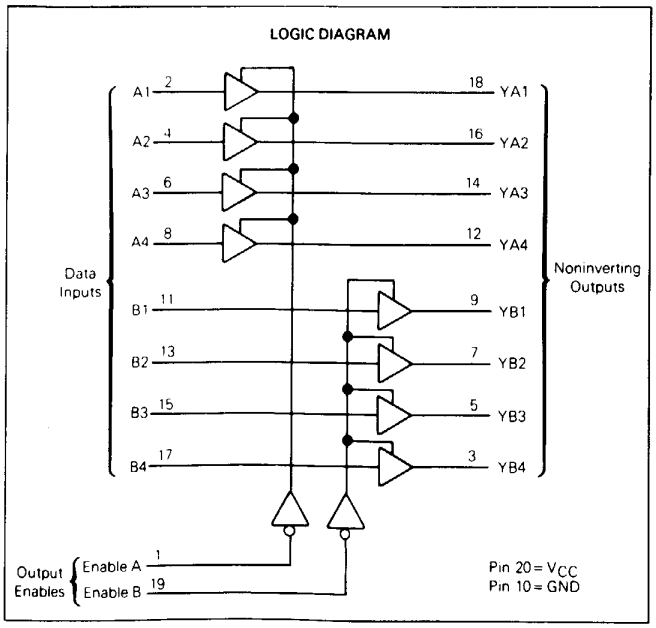
This document contains information on a new product. Specifications and information herein are subject to change without notice.

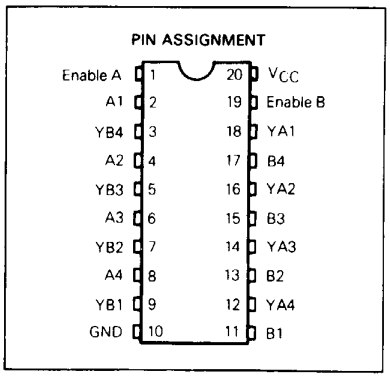
FUNCTION TABLE

Inputs					Internal Stages		Output	
Serial Shift/ Parallel Load	Clock 1	Clock 2	S_A	A-H	Q_A	Q_B	Q_H	Operation
L	X	X	X	a...h	a	b	h	Asynchronous Parallel Load
H	↑	L	L	X	L	Q_{An}	Q_{Gn}	Serial Shift via Clock 1
H	↑	L	H	X	H	Q_{An}	Q_{Gn}	
H	L	↑	L	X	L	Q_{An}	Q_{Gn}	Serial Shift via Clock 2
H	L	↑	H	X	H	Q_{An}	Q_{Gn}	
H	X	H	X	X	no change			Inhibited Clock
H	H	X	X	X				
H	L	L	X	X	no change			No Clock

X = don't care
↑ = transition from low to high
Q_{An}-Q_{Gn} = Data shifted from the preceding stage

74HC244
OCTAL 3-STATE NONINVERTING BUFFER/LINE DRIVER/LINE RECEIVER





FUNCTION TABLE

Inputs		Outputs
Enable A, Enable B	A, B	YA, YB
L	L	L
L	H	H
H	X	Z

Z = High Impedance

This document contains information on a new product. Specifications and information herein are subject to change without notice.

8035
SINGLE COMPONENT 8-BIT MICROCOMPUTER

***8048 Mask Programmable ROM**
***8748 User Programmable/Erasable EPROM**
***8035 External ROM or EPROM**

- 8-Bit CPU, ROM, RAM, I/O in Single Package
- Interchangeable ROM and EPROM Versions
- Single 5V Supply
- 2.5 µsec and 5.0 µsec Cycle Versions All Instructions 1 or 2 Cycles.
- Over 90 Instructions: 70% Single Byte
- 1K x 8 ROM/EPROM
  64 x 8 RAM
  27 I/O Lines
- Interval Timer/Event Counter
- Easily Expandable Memory and I/O
- Compatible with 8000 Series Peripherals
- Single Level Interrupt

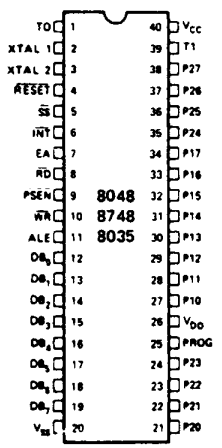
The Intel® 8048/8748/8035 is a totally self-sufficient 8-bit parallel computer fabricated on a single silicon chip using Intel's N-channel silicon gate MOS process.

The 8048 contains a 1K x 8 program memory, a 64 x 8 RAM data memory, 27 I/O lines, and an 8-bit timer/counter in addition to on board oscillator and clock circuits. For systems that require extra capability, the 8048 can be expanded using standard memories and 8000 series peripherals. The 8035 is the equivalent of an 8048 without program memory.

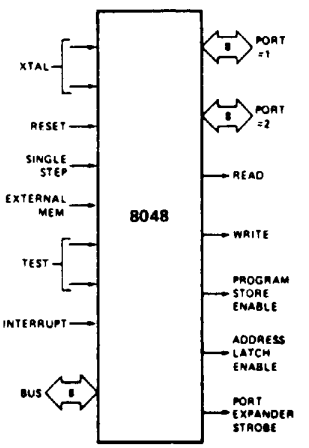
To reduce development problems to a minimum and provide maximum flexibility, three interchangeable pin-compatible versions of this single component microcomputer exist: the 8748 with user-programmable and erasable EPROM program memory for prototype and preproduction systems, the 8048 with factory-programmed mask ROM program memory for low-cost high volume production, and the 8035 without program memory for use with external program memories.

This microprocessor is designed to be an efficient controller as well as an arithmetic processor. The 8048 has extensive bit handling capability as well as facilities for both binary and BCD arithmetic. Efficient use of program memory results from an instruction set consisting mostly of single byte instructions and no instructions over two bytes in length.

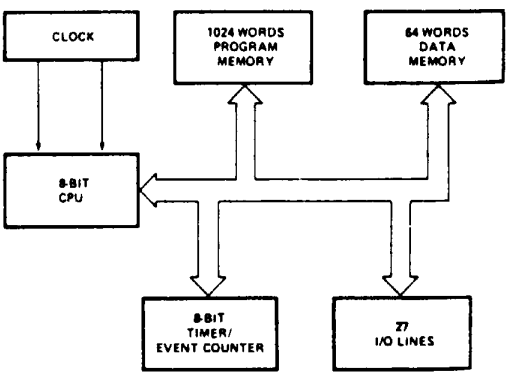
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



8035 (Cont.)

PIN DESCRIPTION

Designation	Pin #	Function
V_{SS}	20	Circuit GND potential
V_{DD}	26	Programming power supply; +25V during program, +5V during operation for both ROM and PROM. Low power standby pin in 8048 ROM version.
V_{CC}	40	Main power supply; +5V during operation and programming.
PROG	25	Program pulse (+25V) input pin during 8748 programming.
		Output strobe for 8243 I/O expander.
P10-P17 Port 1	27-34	8-bit quasi-bidirectional port.
P20-P27 Port 2	21-24 35-38	8-bit quasi-bidirectional port. P20-P23 contain the four high order program counter bits during an external program memory fetch and serve as a 4-bit I/O expander bus for 8243
DB_0-DB_7 BUS	12-19	True bidirectional port which can be written or read synchronously using the $\overline{RD}$, $\overline{WR}$ strobes. The port can also be statically latched.
		Contains the 8 low order program counter bits during an external program memory fetch, and receives the addressed instruction under the control of PSEN. Also contains the address and data during an external RAM data store instruction, under control of ALE, $\overline{RD}$, and $\overline{WR}$.
T0	1	Input pin testable using the conditional transfer instructions JT0 and JNT0. T0 can be designated as a clock output using ENT0 CLK instruction. T0 is also used during programming.
T1	39	Input pin testable using the JT1, and JNT1 instructions. Can be designated the timer/counter input using the STRT CNT instruction.
$\overline{INT}$	6	Interrupt input. Initiates an interrupt if interrupt is enabled. Interrupt is disabled after a reset. Also testable with conditional jump instruction. (Active low)

Designation	Pin #	Function
$\overline{RD}$	8	Output strobe activated during a BUS read. Can be used to enable data onto the BUS from an external device.
		Used as a Read Strobe to External Data Memory. (Active low)
$\overline{RESET}$	4	Input which is used to initialize the processor. Also used during PROM programming verification, and power down. (Active low)
$\overline{WR}$	10	Output strobe during a BUS write. (Active low)(Non TTL V_{IH})
		Used as write strobe to External Data Memory.
ALE	11	Address Latch Enable. This signal occurs once during each cycle and is useful as a clock output.
		The negative edge of ALE strobes address into external data and program memory.
$\overline{PSEN}$	9	Program Store Enable. This output occurs only during a fetch to external program memory. (Active low)
$\overline{SS}$	5	Single step input can be used in conjunction with ALE to "single step" the processor through each instruction. (Active low)
EA	7	External Access input which forces all program memory fetches to reference external memory. Useful for emulation and debug, and essential for testing and program verification. (Active high)
XTAL1	2	One side of crystal input for internal oscillator. Also input for external source. (Not TTL Compatible)
XTAL2	3	Other side of crystal input.

8085A/8085A-2
SINGLE CHIP 8-BIT N-CHANNEL MICROPROCESSORS

FUNCTIONAL DESCRIPTION

The 8085A is a complete 8-bit parallel central processor. It is designed with N-channel depletion loads and requires a single +5 volt supply. Its basic clock speed is 3 MHz (8085A) or 5 MHz (8085A-2), thus improving on the present 8080A's performance with higher system speed. Also it is designed to fit into a minimum system of three IC's: The cpu (8085A), a RAM/IO (8156), and a ROM or EPROM/IO chip (8355 or 8755A).

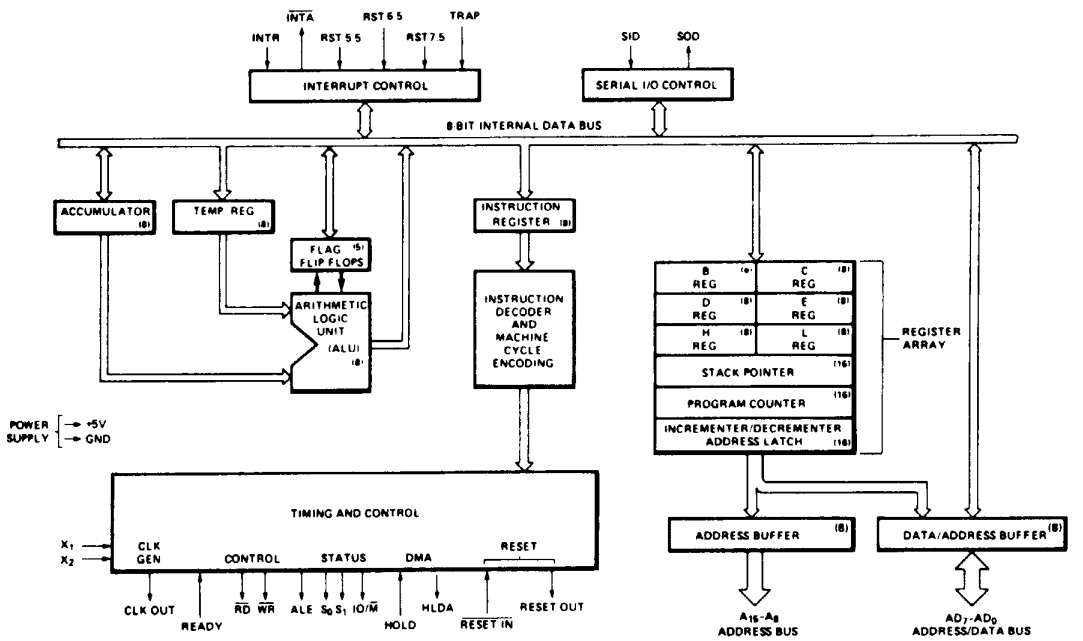
The 8085A has twelve addressable 8-bit registers. Four of them can function only as two 16-bit register pairs. Six others can be used interchangeably as 8-bit registers or as 16-bit register pairs. The 8085A register set is as follows:

Mnemonic	Register	Contents
ACC or A	Accumulator	8 bits
PC	Program Counter	16-bit address
BC,DE,HL	General-Purpose Registers; data pointer (HL)	8 bits x 6 or 16 bits x 3
SP	Stack Pointer	16-bit address
Flags or F	Flag Register	5 flags (8-bit space)

The 8085A uses a multiplexed Data Bus. The address is split between the higher 8-bit Address Bus and the lower 8-bit Address/Data Bus. During the first T state (clock cycle) of a machine cycle the low order address is sent out on the Address/Data bus. These lower 8 bits may be latched externally by the Address Latch Enable signal (ALE). During the rest of the machine cycle the data bus is used for memory or I/O data.

The 8085A provides $\overline{RD}$, $\overline{WR}$, S_0, S_1, and IO/$\overline{M}$ signals for bus control. An Interrupt Acknowledge signal ($\overline{INTA}$) is also provided. HOLD and all Interrupts are synchronized with the processor's internal clock. The 8085A also provides Serial Input Data (SID) and Serial Output Data (SOD) lines for simple serial interface.

In addition to these features, the 8085A has three maskable, vector interrupt pins and one nonmaskable TRAP interrupt.



8085A CPU Functional Block Diagram

8085A/8085A-2 (Cont.)

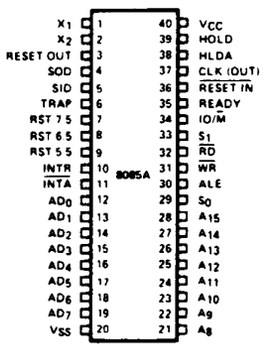


Figure 2. 8085A Pinout Diagram

8085A FUNCTIONAL PIN DEFINITION

The following describes the function of each pin:

Symbol — **Function**

A_8–A_{15} (Output, 3-state)
Address Bus: The most significant 8 bits of the memory address or the 8 bits of the I/O address, 3-stated during Hold and Halt modes and during RESET.

AD_{0-7} (Input/Output, 3-state)
Multiplexed Address/Data Bus: Lower 8 bits of the memory address (or I/O address) appear on the bus during the first clock cycle (T state) of a machine cycle. It then becomes the data bus during the second and third clock cycles.

ALE (Output)
Address Latch Enable: It occurs during the first clock state of a machine cycle and enables the address to get latched into the on-chip latch of peripherals. The falling edge of ALE is set to guarantee setup and hold times for the address information. The falling edge of ALE can also be used to strobe the status information. ALE is never 3-stated.

S_0, S_1, and IO/$\overline{M}$ (Output)
Machine cycle status:

IO/$\overline{M}$	S_1	S_0	Status
0	0	1	Memory write
0	1	0	Memory read
1	0	1	I/O write
1	1	0	I/O read
0	1	1	Opcode fetch
1	1	1	Interrupt Acknowledge
*	0	0	Halt
*	X	X	Hold
*	X	X	Reset

* = 3-state (high impedance)
X = unspecified

Symbol — **Function**

S_1 can be used as an advanced R/$\overline{W}$ status. IO/$\overline{M}$, S_0 and S_1 become valid at the beginning of a machine cycle and remain stable throughout the cycle. The falling edge of ALE may be used to latch the state of these lines.

$\overline{RD}$ (Output, 3-state)
READ control: A low level on $\overline{RD}$ indicates the selected memory or I/O device is to be read and that the Data Bus is available for the data transfer, 3-stated during Hold and Halt modes and during RESET.

$\overline{WR}$ (Output, 3-state)
WRITE control: A low level on $\overline{WR}$ indicates the data on the Data Bus is to be written into the selected memory or I/O location. Data is set up at the trailing edge of $\overline{WR}$. 3-stated during Hold and Halt modes and during RESET.

READY (Input)
If READY is high during a read or write cycle, it indicates that the memory or peripheral is ready to send or receive data. If READY is low, the cpu will wait an integral number of clock cycles for READY to go high before completing the read or write cycle. READY must conform to specified setup and hold times.

HOLD (Input)
HOLD indicates that another master is requesting the use of the address and data buses. The cpu, upon receiving the hold request, will relinquish the use of the bus as soon as the completion of the current bus transfer. Internal processing can continue. The processor can regain the bus only after the HOLD is removed. When the HOLD is acknowledged, the Address, Data, $\overline{RD}$, $\overline{WR}$, and IO/$\overline{M}$ lines are 3-stated.

HLDA (Output)
HOLD ACKNOWLEDGE: Indicates that the cpu has received the HOLD request and that it will relinquish the bus in the next clock cycle. HLDA goes low after the Hold request is removed. The cpu takes the bus one half clock cycle after HLDA goes low.

INTR (Input)
INTERRUPT REQUEST: is used as a general purpose interrupt. It is sampled only during the next to the last clock cycle of an instruction and during Hold and Halt states. If it is active, the Program Counter (PC) will be inhibited from incrementing and an $\overline{INTA}$ will be issued. During this cycle a RESTART or CALL instruction can be inserted to jump to the interrupt service routine. The INTR is enabled and disabled by software. It is disabled by Reset and immediately after an interrupt is accepted.

8085A/8085A-2 (Cont.)

8085A FUNCTIONAL PIN DESCRIPTION (Continued)

Symbol	Function
$\overline{\text{INTA}}$ (Output)	INTERRUPT ACKNOWLEDGE: Is used instead of and has the same timing as $\overline{\text{RD}}$ during the Instruction cycle after an INTR is accepted. It can be used to activate the 8259 Interrupt chip or some other interrupt port.
RST 5.5 RST 6.5 RST 7.5 (Inputs)	RESTART INTERRUPTS: These three inputs have the same timing as INTR except they cause an internal RESTART to be automatically inserted. The priority of these interrupts is ordered as shown in Table 1. These interrupts have a higher priority than INTR. In addition, they may be individually masked out using the SIM instruction.
TRAP (Input)	Trap interrupt is a nonmaskable RESTART interrupt. It is recognized at the same time as INTR or RST 5.5-7.5. It is unaffected by any mask or Interrupt Enable. It has the highest priority of any interrupt. (See Table 1.)
$\overline{\text{RESET IN}}$ (Input)	Sets the Program Counter to zero and resets the Interrupt Enable and HLDA flip-flops. The data and address buses and the control lines are 3-stated during RESET and because of the asynchronous nature of RESET, the processor's internal registers and flags may be altered by RESET with unpredictable results. $\overline{\text{RESET IN}}$ is a Schmitt-triggered input, allowing connection to an R-C network for power-on RESET delay. The cpu is held in the reset condition as long as $\overline{\text{RESET IN}}$ is applied.
RESET OUT (Output)	Indicates cpu is being reset. Can be used as a system reset. The signal is synchronized to the processor clock and lasts an integral number of clock periods.
X_1, X_2 (Input)	X_1 and X_2 are connected to a crystal, LC, or RC network to drive the internal clock generator. X_1 can also be an external clock input from a logic gate. The input frequency is divided by 2 to give the processor's internal operating frequency.
CLK (Output)	Clock Output for use as a system clock. The period of CLK is twice the X_1, X_2 input period.
SID (Input)	Serial input data line. The data on this line is loaded into accumulator bit 7 whenever a RIM instruction is executed.
SOD (Output)	Serial output data line. The output SOD is set or reset as specified by the SIM instruction.
V_{CC}	+5 volt supply.
V_{SS}	Ground Reference.

TABLE 1. INTERRUPT PRIORITY, RESTART ADDRESS, AND SENSITIVITY

Name	Priority	Address Branched To (1) When Interrupt Occurs	Type Trigger
TRAP	1	24H	Rising edge AND high level until sampled.
RST 7.5	2	3CH	Rising edge (latched).
RST 6.5	3	34H	High level until sampled.
RST 5.5	4	2CH	High level until sampled.
INTR	5	See Note (2).	High level until sampled.

NOTES:

(1) The processor pushes the PC on the stack before branching to the indicated address.
(2) The address branched to depends on the instruction provided to the cpu when the interrupt is acknowledged.

8155/8156/8155-2/8156-2
2048 BIT STATIC MOS RAM
WITH I/O PORTS AND TIMER

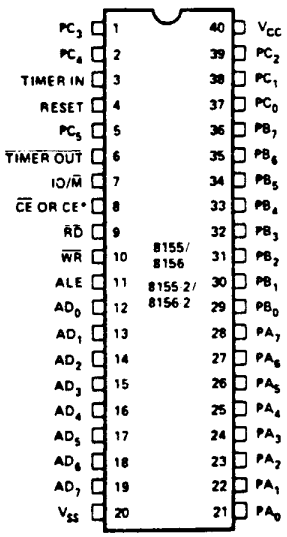
- 256 Word x 8 Bits
- Single +5V Power Supply
- Completely Static Operation
- Internal Address Latch
- 2 Programmable 8 Bit I/O Ports
- 1 Programmable 6-Bit I/O Port
- Programmable 14-Bit Binary Counter/ Timer
- Compatible with 8085A and 8088 CPU
- Multiplexed Address and Data Bus
- 40 Pin DIP

The 8155 and 8156 are RAM and I/O chips to be used in the 8085A and 8088 microprocessor systems. The RAM portion is designed with 2048 static cells organized as 256 x 8. They have a maximum access time of 400 ns to permit use with no wait states in 8085A CPU. The 8155-2 and 8156-2 have maximum access times of 330 ns for use with the 8085A-2 and the full speed 5 MHz 8088 CPU.

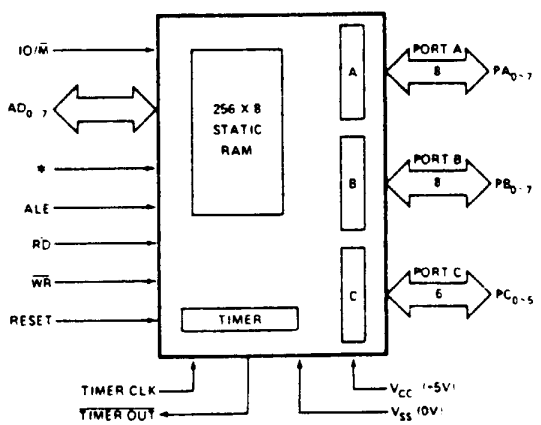
The I/O portion consists of three general purpose I/O ports. One of the three ports can be programmed to be status pins, thus allowing the other two ports to operate in handshake mode.

A 14-bit programmable counter/timer is also included on chip to provide either a square wave or terminal count pulse for the CPU system depending on timer mode.

PIN CONFIGURATION



BLOCK DIAGRAM



* 8155/8155-2 = $\overline{CE}$, 8156 8156-2 = CE

8155/8156/8155-2/8156-2 (Cont.)

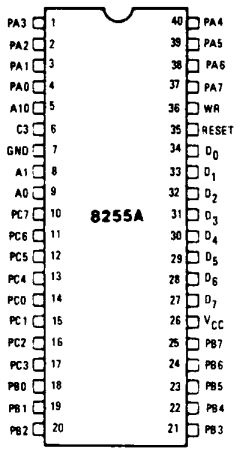
8155/8156 PIN FUNCTIONS

Symbol	Function
RESET (input)	Pulse provided by the 8085A to initialize the system (connect to 8085A RESET OUT). Input high on this line resets the chip and initializes the three I/O ports to input mode. The width of RESET pulse should typically be two 8085A clock cycle times.
AD_{0-7} (input)	3-state Address/Data lines that interface with the CPU lower 8-bit Address/Data Bus. The 8-bit address is latched into the address latch inside the 8155/56 on the falling edge of ALE. The address can be either for the memory section or the I/O section depending on the IO/$\overline{M}$ input. The 8-bit data is either written into the chip or read from the chip, depending on the $\overline{WR}$ or $\overline{RD}$ input signal.
CE or $\overline{CE}$ (input)	Chip Enable: On the 8155, this pin is $\overline{CE}$ and is ACTIVE LOW. On the 8156, this pin is CE and is ACTIVE HIGH.
$\overline{RD}$ (input)	Read control: Input low on this line with the Chip Enable active enables and AD_{0-7} buffers. If IO/$\overline{M}$ pin is low, the RAM content will be read out to the AD bus. Otherwise the content of the selected I/O port or command/status registers will be read to the AD bus.
$\overline{WR}$ (input)	Write control: Input low on this line with the Chip Enable active causes the data on the Address/Data bus to be written to the RAM or I/O ports and command/status register depending on IO/$\overline{M}$.
ALE (input)	Address Latch Enable: This control signal latches both the address on the AD_{0-7} lines and the state of the Chip Enable and IO/$\overline{M}$ into the chip at the falling edge of ALE.
IO/$\overline{M}$ (input)	Selects memory if low and I/O and command/status registers if high.
PA_{0-7} (8) (input/output)	These 8 pins are general purpose I/O pins. The in/out direction is selected by programming the command register.
PB_{0-7} (8) (input/output)	These 8 pins are general purpose I/O pins. The in/out direction is selected by programming the command register.
PC_{0-5} (6) (input/output)	These 6 pins can function as either input port, output port, or as control signals for PA and PB. Programming is done through the command register. When PC_{0-5} are used as control signals, they will provide the following: PC_0 — A INTR (Port A Interrupt) PC_1 — ABF (Port A Buffer Full) PC_2 — $\overline{A\ STB}$ (Port A Strobe) PC_3 — B INTR (Port B Interrupt) PC_4 — $\overline{B\ BF}$ (Port B Buffer Full) PC_5 — B STB (Port B Strobe)
TIMER IN (input)	Input to the counter-timer.
$\overline{TIMER\ OUT}$ (output)	Timer output. This output can be either a square wave or a pulse depending on the timer mode.
V_{CC}	+5 volt supply.
V_{SS}	Ground Reference.

8255A/8255A-5
PROGRAMMABLE PERIPHERAL INTERFACE

The Intel® 8255A is a general purpose programmable I/O device designed for use with Intel® microprocessors. It has 24 I/O pins which may be individually programmed in 2 groups of 12 and used in 3 major modes of operation. In the first mode (MODE 0), each group of 12 I/O pins may be programmed in sets of 4 to be input or output. In MODE 1, the second mode, each group may be programmed to have 8 lines of input or output. Of the remaining 4 pins, 3 are used for handshaking and interrupt control signals. The third mode of operation (MODE 2) is a bidirectional bus mode which uses 8 lines for a bidirectional bus, and 5 lines, borrowing one from the other group, for handshaking.

PIN CONFIGURATION



PIN NAMES

$D_7 - D_0$	DATA BUS (BIDIRECTIONAL)
RESET	RESET INPUT
$\overline{CS}$	CHIP SELECT
$\overline{RD}$	READ INPUT
$\overline{WR}$	WRITE INPUT
A0, A1	PORT ADDRESS
PA7 – PA0	PORT A (BIT)
PC7 – PB0	PORT B (BIT)
PC7 – PC0	PORT C (BIT)
V_{CC}	+5 VOLTS
GND	5 VOLTS

8255A BLOCK DIAGRAM